InAs avalanche photodiode linear array for low photon applications

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Glossary – List of Abbreviations

ADAS	Advanced driver assistance systems
APD	Avalanche photodiode
BCB	B-staged benzocyclobutene
BER	Bit error rate
C-V	Capacitance-voltage
DFT	Discrete Fourier transform
DIAL	Differential absorption LiDAR
DIW	De-ionised water
DUT	Device-under-test
e-APD	Electron avalanche photodiode
EHP	Electron-hole pair
FFT	Fast Fourier transform
GBP	Gain-bandwidth product
G-R	Generation-recombination
HDVIP	High-density vertically integrated photodiode
HF	Hydrofluoric acid
I2E	Impact ionisation engineering
ICP	Inductively coupled plasma
ICPCVD	Inductively coupled plasma chemical vapour deposition
I-V	Current-voltage
LED	Light-emitting diode
LIA	Lock-in amplifier
LiDAR	Light detection and ranging
LPE	Liquid phase epitaxy
LWIR	Long-wave infrared
MBE	Molecular beam epitaxy
MCT	Mercury cadmium telluride
MEMS	Micro-electro-mechanical systems
MLA	Mesa linear array
MOVPE	Metalorganic vapour phase epitaxy
MPE	Maximum permissible exposure

MWIR	Mid-wave infrared
NFM	Noise figure meter
NIR	Near infrared
PECVD	Plasma-enhanced chemical vapour deposition
PLA	Planar linear array
RIE	Reactive ion etching
RTA	Rapid thermal annealing
SAGCM	Separate absorption, grading, charge and multiplication
SAM-APD	Separate absorption and multiplication avalanche photodiode
SCM	Single carrier multiplication
SiPM	Silicon photomultiplier
SIMS	Secondary ion mass spectroscopy
SMU	Source-measure unit
SNR	Signal-to-noise ratio
SPAD	Single photon avalanche diode
SRH	Shockley-Read-Hall
SWIR	Short-wave infrared
TLM	Transmission line measurement
ToF	Time of flight
TRIM	Transport of Ions in Matter
VCSEL	Vertical cavity surface emitting laser
VLWIR	Very long-wave infrared

Glossary – List of Symbols

A	Area of device/receiver
$\forall$	Pre-exponential factor of Arrhenius equation
α	Electron impact ionisation coefficient
β	Hole impact ionisation coefficient
c_0	Speed of light
C_d	Junction capacitance per unit area
CMOS	Complementary metal-oxide-semiconductor
$d_{p,n}$	Depletion width in p- and n-type material
$D_{p,n}$	Diffusion constant of minority electron/hole
Δ_{SO}	Spin-orbit split-off energy
Δf	Bandwidth
Δt	lag/return time of returning laser pulse
E_A	Activation energy
E_g	Band gap energy
$E_{th(e,h)}$	Ionisation threshold energy for electron/hole
ε_0	Vacuum permittivity
ε_r	Relative permittivity of material
ε_s	Material permittivity
ξ	Electric field
$F(M)$	Excess noise factor
G	Multiplication of a particular trial
γ	Tunnelling parameter
h	Planck's constant
$\hbar$	Reduced Planck's constant
I_d	Dark current
i_n^2	Diode shot noise
I_{ph}	Photocurrent
I_{pri}	Primary photocurrent
i_{th}	Thermal noise of amplifier
J	Current density

J_0	Saturation current density
J_{bulk}	Bulk contribution dark current
J_{SRH}	Current density due to Shockley-Read-Hall
J_{surf}	Surface contribution dark current
J_{tunn}	Current density due to tunnelling
k	Ratio of hole to electron ionisation coefficient
k_b	Boltzmann's constant
$L_{p,n}$	Minority carrier diffusion length of minority electron/hole
λ	Wavelength
λ_{off}	Off-line wavelength
λ_{on}	On-line wavelength
λ_{peak}	Peak wavelength of blackbody source
ℓ	Range to target gas species
M	Multiplication factor
M_e	Electron-initiated multiplication
$M(0)$	Pure electron injected multiplication
$M(x)$	Average total number of electrons and holes
$M(W)$	Pure hole injected multiplication
m^*	Effective carrier mass
n	Ideality factor
$N_{A,D}$	Acceptor/hole doping concentration
N_B	Background doping concentration
n_i	Intrinsic carrier concentration
η	Quantum efficiency
η_{ext}	External quantum efficiency
η_{sys}	Optical system efficiency
P_0	Transmitted power from laser
P_{opt}	Incident optical power
$P_{rec}(\ell)$	Received signal power as a function of range
r	Radius of device
R	Responsivity
R_{eq}	Equivalent resistance at amplifier input

R_{ideal}	Theoretical maximum responsivity
R_{meas}	Measured responsivity
R_s	Series resistance
q	Elementary charge
τ	Carrier lifetime
φ	Atmospheric backscattering coefficient
T	Temperature
TLM	Transmission line measurement
V_{bias}	Applied bias voltage
V_{bi}	Built-in voltage
V_r	Reverse bias voltage
ν	Frequency of light
W	Depletion width
χ	Extinction coefficient

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Abstract

Avalanche photodiodes (APDs) are used in photon-starved applications for their ability to amplify low levels of incoming signals. A special class of APDs, known as electron APDs (e-APDs), can significantly improve the signal-to-noise ratio of an optical receiver system due to single carrier multiplication and the lack of hole feedback. InAs is one of such material with a band gap of 0.36 eV which makes InAs an attractive material of choice for low photon, infrared applications such as LiDAR and active imaging. Conventional mesa structure InAs APDs face many problems such as lateral side etching and the need for sidewall passivation. Planar topology InAs APDs previously developed using a high energy ion implantation scheme have shown performance comparable to the mesa structure APDs.

In this thesis, planar InAs APDs with a shallow implant depth of 100 nm are investigated. Long duration anneals have been employed to promote dopant diffusion to form the p-type region. The dark current and responsivity of the planar APDs show improvement over as processed samples following a shallow surface etch, indicating the removal of surface damage induced by ion implantation.

Linear arrays of mesa and planar InAs APDs are fabricated and the array uniformity is evaluated to show that superior homogeneity of diode performance, from current-voltage and responsivity measurements, in the planar linear array. The challenges faced during semiconductor processing of mesa linear arrays are detailed and discussed to illustrate low device yield in mesa linear arrays.

Finally, the planar linear array is characterised in detail at the temperature range of 300 – 77 K. Good uniformity in dark current and gain characteristics are demonstrated at the temperatures measured. At 77 K, the signal-to-noise ratio increases with bias voltage (and gain) with a maximum of 62.8 dB at -22 V before the diode shot noise dominates. Current-voltage characteristics of the diode array before and after multiple thermal cycles show minimal degradation, highlighting the robustness of the fabricated planar array.

List of Publications

Journal Papers

L. W. Lim, P. Patil, I. P. Marko, E. Clark, S. J. Sweeney, J. S. Ng, J. P. R. David, and C. H. Tan, "Electrical and optical characterisation of low temperature grown InGaAs for photodiode applications", *Semicond. Sci. Technol.*, vol. 35, no. 9, 095031, 2020.

X. Yi, S. Xie, B. Liang, **L. W. Lim**, J. S. Cheong, M. C. Debnath, D. L. Huffaker, C. H. Tan, and J. P. R. David, "Extremely low excess noise and high sensitivity AlAs0.56Sb0.44 avalanche photodiodes", *Nat. Photonics*, vol. 13, pp. 683-686, 2019.

L. W. Lim, C. H. Tan, J. S. Ng, J. D. Petticrew, and A. B. Krysa, "Improved Planar InAs Avalanche Photodiodes With Reduced Dark Current and Increased Responsivity", *J. Lightw. Technol.*, vol. 37, no. 10, pp. 2375-2379, 2019.

C. H. Tan, A. Velichko, **L. W. Lim**, and J. S. Ng, "Few-photon detection using InAs avalanche photodiodes", *Opt. Express*, vol. 27, no. 4, pp. 5835-5842, 2019.

X. Yi, S. Xie, B. Liang, **L. W. Lim**, X. Zhou, M. C. Debnath, D. L. Huffaker, C. H. Tan, and J. P. R. David, "Demonstration of large ionization coefficient ratio in AlAs0.56Sb0.44 lattice matched to InP", *Sci Rep*, vol. 8, pp. 9107, 2018.

Conference

X. Yi, S. Xie, B. L. Liang, **L. W. Lim**, D. L. Huffaker, C. H. Tan, and J. P. R. David, "Extremely low-noise avalanche photodiodes based on $AlAs_{0.56}Sb_{0.44}$", *SPIE Security + Defence 2020*, Edinburgh, UK, Sept 2020.

X. Yi, S. Xie, B. L. Liang, **L. W. Lim**, D. L. Huffaker, C. H. Tan, and J. P. R. David, "High performance $AlAs_{0.56}Sb_{0.44}$ avalanche photodiodes", *SPIE Photonics West 2020*, San Francisco, California, United States, Feb 2020.

S. Xie, X. Yi, B. L. Liang, **L. W. Lim**, D. L. Huffaker, C. H. Tan, and J. P. R. David, "High speed and high sensitivity $AlAs_{0.56}Sb_{0.44}$ avalanche photodiodes", *Asia Communication Photonics*, Chengdu, China, Nov 2019.

L. W. Lim, M. Kesaria, I. P. Marko, P. Patil, E. Clarke, S. J. Sweeney, J. P. R. David, and C. H. Tan, "Optical and electrical performance of low temperature MBE-grown

InGaAs and InGaAsBi photodetectors", *10th International Workshop on Bismuth-Containing Semiconductors*, Toulouse, France, Jul 2019.

D. L. Huffaker, S. Xie, X. Yi, B. L. Liang, **L. W. Lim**, C. H. Tan, and J. P. R. David, "Large ionisation coefficient ratio in $AlAs_{0.56}Sb_{0.44}$ avalanche photodiodes", *Compound Semiconductor Week 2019*, Kasugano International Forum, Nara, Japan, May 2019.

L. W. Lim, J. D. Petticrew, A. B. Krysa, J. S. Ng, and C. H. Tan, "Investigation of low energy Be implantation and annealing conditions in InAs avalanche photodiodes", *44th Freiburg Infrared Colloquium*, Freiburg, Germany, Mar 2019.

X. Yi, S. Xie, B. L. Liang, **L. W. Lim**, X. Zhou, M. C. Debnath, D. L. Huffaker, C. H. Tan, and J. P. R. David, "Avalanche multiplication in $AlAs_{0.56}Sb_{0.44}$", *Asia Communications and Photonics Conference*, Hangzhou, China, Oct 2018.

S. Xie, X. Yi, B. L. Liang, **L. W. Lim**, X. Zhou, M. C. Debnath, C. H. Tan, J. P. R. David, and D. L. Huffaker, "Breakdown voltages in $AlAs_{0.56}Sb_{0.44}$ avalanche photodiodes", *UK Semiconductors*, Sheffield, UK, Jul 2018.

L. W. Lim, J. D. Petticrew, A. B. Krysa, and C. H. Tan, "Investigation of low energy Be implantation in InAs photodiodes", *UK Semiconductor*, Sheffield, UK, Jul 2017.

V. Shulyak, **L. W. Lim**, C. H. Tan, and J. S. Ng, "Sensitivity of High-Speed Optical Receivers with InAs Avalanche Photodiodes", *UK Semiconductor*, Sheffield, UK, Jul 2017.

Chapter 1 Introduction

1.1 Light detection and ranging (LiDAR)

Light detection and ranging is a metrological technique for distance measurement by illuminating a target or scene with laser light and detecting the reflected signal. LiDAR is particularly useful as a non-destructive tool to form 3-D environmental maps in geological or archaeological sites [1], [2], monitoring of foliage growth for crop maintenance and harvesting in agriculture [3] and atmospheric observations for metrological and climate research purposes [4], to name a few. With the advent of lasers, ranging experiments such as the measurement of the Earth-Moon distance has been conducted (ongoing to improve accuracies down to sub-millimetre resolution) by measuring the time taken for laser light from the Earth surface to arrive at and reflect from the Moon's surface [5]. The same method has also been used to profile the surface topography of the Moon [6].

1.1.1 Atmospheric LiDAR

LiDAR systems used for remote atmospheric measurements can be influenced by aerosol particles, dust, water vapour, various gas molecules [7]. Interactions between laser light and atmospheric constituents can involve absorption [8] as well as elastic [9] and inelastic [10] scattering, leading to several LiDAR techniques that are effective for different applications. The first published use of LiDAR was for the purpose of measuring the height of clouds in 1946 [11]. Beginnings of the modern LiDAR technique started shortly after the invention of the ruby laser in 1960 [12] and subsequently used in atmospheric studies by Fiocco *et al.* in 1963 [13]. Since then, LiDAR systems and instrumentation has developed rapidly to cope with requirements to make the technique more accurate and sensitive.

With increasing concerns mounting over rising global temperatures and climate changes, the detection and monitoring of greenhouse gases and atmospheric pollutants are vital. LiDAR system development in observatories and satellites around the globe are used to measure, observe, and predict changes in the atmosphere. For example, NASA's continual involvement in the field of remote sensing has led to the development of the G-LiHT airborne imager [14]. The European space program, MERLIN, is a joint collaboration between France and Germany for atmospheric

methane monitoring [15]. Several ground-based observatories such as the ALOMAR in Norway [16], SIRTA site in Paris [17] and HALO in California [18] are used for taking vast LiDAR measurements of the atmosphere. The detection of toxic atmospheric gases such as CO_2, CH_4, and NO_x has been long studied via optical means [19]. The molecular structure of a gas molecule gives rise to unique absorption characteristics at specific infrared wavelengths (or frequencies). This is due to the absorption of photons at these resonant frequencies that causes vibrational or rotational transitions in the molecules [20]. This leads to a characteristic infrared signature for different gas species which forms the basis of infrared absorption spectroscopy.

In LiDAR measurements, these known vibrational modes of different molecules are exploited by using laser light of specific wavelengths to interact with the gas of interest following the subsequent measurement to characteristic changes to the transmitted laser light. This has been well studied with many published works in the detection of trace concentration of gases in the atmosphere such as O_3 at <3 μm [21], [22], CH_4 at 1.6 [23], [24] and 3.4 μm [25], CO_2 at 2 μm [26], [27] and 4.8 μm [28], N_2O [29] and H_2O [30]. The most commonly employed LiDAR technique for trace gas sensing is different absorption LiDAR (DIAL). The DIAL technique works by emitting two different wavelengths, one that is on the absorption line (λ_{on}) of the target gas species and another away from the absorption line (λ_{off}) as a reference signal. Both backscattered signals are collected at the receiver and the difference in power due to absorption gives a measure of the gas concentration [7]. The backscattered signal for a LiDAR system is governed by the following equation [31].

$$P_{rec}(\ell) = P_0 \eta_{sys} \frac{A}{\ell^2} \frac{c_0 \Delta t}{2} \varphi(\ell) \exp\left[\int_0^{\ell} -2\chi(l)dl\right] \tag{1.1}$$

where $P_{rec}(\ell)$ is the received signal power as a function of range, P_0 is the transmitted power from laser, η is the optical system efficiency, A is the area of the receiver, ℓ is the range to the target gas species, c_0 is the speed of light in air, Δt is the return time of the received laser pulse, φ and χ is the atmospheric backscattering and extinction coefficient. The equation assumes only a single scattering element is present in the atmosphere, however in reality, there can be a number of trace gases as well as particles of various sizes present in the atmosphere, complicating the gas sensing analysis by DIAL.

Another widely used LiDAR technique for remote gas sensing applications is Raman LiDAR [32] which relies on the shift in frequency of laser light upon scattering inelastically (also known as Raman scattering) with the target gas. From a molecular point of view, light scattering occurs when photons of a particular excitation energy are absorbed and re-emitted. When the final energy level of the molecule is the same as the initial level and by extension, the re-emitted photon has the same energy as the incident photon (wavelength of light remains the same) but a different propagation direction, the scattering is considered elastic. Inelastic scattering occurs when the final state of the molecule is changed from the initial state. If the final molecular state is at a higher energy level, some of the photon energy is absorbed and the re-emitted photon will be of a lower energy, corresponding to a longer wavelength [33]. Again, the Raman phenomenon is specific to gas species therefore characteristic Raman spectra exist for different gas molecules. In comparison to the DIAL technique, Raman LiDAR signals are considerably weaker (for example water vapour Raman signals are four orders magnitude lower than backscattered signals [34]) and is therefore used for measuring gases at high concentrations. Furthermore, Raman LiDAR systems require intricate optics design to suppress any signal contamination from elastic backscattered signals [7]. Raman LiDAR, unlike the DIAL technique, can be performed using a wide range of wavelengths ranging from visible to NIR [35].

1.1.2 Automotive LiDAR

While the effectiveness of LiDAR has been exploited in many areas, interest in employing LiDAR in the field of automotive applications has been rising in the past decade in the hope to achieve fully autonomous self-driving vehicles. Statistics have shown that in the United Kingdom, there were more than 100 thousand reported incidents of road casualties, with 1% of the listed resulting in death [36]. Modern cars have been outfitted with an increasing amount of electronics as part of various advanced driver assistance systems (ADAS) aimed at parsing road information, detecting early warning signs to alert drivers into taking precautionary measures, or to sometimes automatically apply direct countermeasures such as emergency braking for collision prevention [37]. ADAS such as blind spot detection, vehicular and pedestrian collision warnings, rear-view parking camera, in general enhances the driving experience and ensures driving, as a mode of transport, is safe for both the driver and other road users. These safety features installed on cars are enabled by a multitude of

sensors based on electromagnetic signals, image capture or ultrasound [38], [39]. Each technology is useful in its own domain but has limitations that require another method to complement. One such example is the use of optical cameras to identify traffic signage and imageries under daytime conditions but would falter under low light night time conditions. Between sensors, overlaps are sometimes necessary to ensure that all road information are accounted for to form a comprehensive map of the 3-D environment, which is essential to attain Level 5 autonomous vehicles, i.e. self-driving cars without need of any driver intervention.

Automotive LiDARs are mainly aimed at the identification of human or wildlife targets at least from a range of 100 metres (to account for the braking distance required when travelling at speed) and the detection and tracking of nearby vehicles. A commonality shared between LiDAR and long range radar is the range factor where both methods are able to identify large objects up to hundreds of metres away. However, a downside to radar is the poor angular resolution, limiting the ability to recognise relatively smaller objects such as humans at a distance away [40]. Distance information can be extracted from the time delay between the transmitted and received signals, using a simple relation of $d = \frac{c_0 \cdot \Delta t}{2}$, where d is the distance, c_0 is the speed of light in air (as the transmission medium) and Δt is the travel time for a roundtrip, hence this method is also known as time-of-flight (ToF) LiDAR. The first demonstration of automotive LiDAR on a ground-based vehicle was a rotating disc unit that houses 64 lasers at DARPA‘s Grand Challenge in 2005, which was aimed at encouraging technological innovations and developments in the field of autonomous vehicles [41]. The inventors of that particular LiDAR module went on to establish Velodyne Lidar, the pioneering company in the automotive LiDAR industry and one of the most dominant in the current market. Commercially available Velodyne LiDAR units operate at a wavelength of 905 nm and uses a mechanical scanning method to provide a complete 360° horizontal field-of-view surrounding the vehicle.

Besides Velodyne, an increasing number of budding companies are tackling the automotive LiDAR industry, each with key aspects of technological innovation and individual approaches to improve LiDAR performance. To list a few, Luminar uses an illumination wavelength of 1550 nm coupled with a mechanical mirror beam steering system, AEye focuses on a software-based approach using an onboard artificial

intelligence to learn and adapt to ever-changing driving conditions and Ouster employs a flash illumination technique at a wavelength of 850 nm. There are others opting for more unconventional methods such as Baraja using tunable lasers and an optical prism to manipulate beam direction and Quanergy working on controlling the laser beam with optical phased arrays.

Only a narrow selection of wavelengths, namely 905, 940 and 1550 nm, are commonly used for automotive LiDAR. This is largely due to two reasons: one, the local minima in the solar spectrum reflected from the Earth's surfaces after attenuation through atmospheric water vapour [42]; and two, the availability of mature laser and detector technologies for a fully solid-state system. For comparison, the solar photon flux at the unconventional LiDAR wavelength of 850 nm is 2, 10 and 3 times higher than at 905, 940 and 1550 nm respectively [43]. It is argued in Ouster's case that the poor water vapour absorption at 850 nm can instead be advantageous to ensure consistent LiDAR performance in humid weather and foggy conditions. For near-infrared (NIR) LiDAR operation in the range of 850 – 940 nm, GaAs-based laser diodes and vertical cavity surface emitting lasers (VCSELs) are widely available while cheap, mature Si-based sensors can be used as detectors. Similarly, in the 1550 nm short-wave infrared (SWIR) wavelength, InP-based technologies are commercially available for laser diodes and photodetectors.

The choice of operation wavelength is weighed not only on the aspect of component cost (which heavily favours the shorter wavelengths) but also eye-safety considerations and thereby the performance. Eye safety poses an inherent limit to the maximum laser power a LiDAR system can output (and therefore the maximum range) since automotive LiDAR functions in environments where human eyes are exposed to laser light and infrared wavelengths cannot trigger eye-blinking reflexes. Exposure over the maximum permissible exposure (MPE), which is a function of laser power and exposure time, will cause retinal damage and therefore a method of mitigation is the use of short laser pulses. 1550 nm lasers are generally considered eye-safe as compared to 905 or 940 nm [44] which allows higher laser output powers for superior range performance. The dispersal, scattering and attenuation of laser light under harsh weather conditions such as foggy, rainy or snowy conditions can severely impact the transmittance of laser and degrade LiDAR performance [45]–[47]. Higher output

powers (up to 10 times more than shorter wavelength options) allowable on 1550 nm systems is therefore a more attractive choice under adverse weathers [48].

The emitted laser can be attenuated by both external factors and internal system imperfections from equation 1.1 [49], for example atmospheric transmission, target reflectivity, optics transmission efficiency and distance, such that the returning signal becomes extremely limited down to a few or even a single photon, necessitating the use of highly sensitive photodetectors such as avalanche photodiodes (APDs) [50], [51]. APDs are devices with an internal gain mechanism that is able to boost the received signal, thus increasing the signal-to-noise ratio (SNR) of a detection system. Furthermore, APDs can be operated in linear mode or Geiger mode, where the former produces signal amplification that is proportional to the applied voltage bias while the latter produces binary signals depending on the detection (or absence) of an incoming photon. Devices of the latter design are also sometimes known as single photon avalanche diodes (SPADs). For Si-based technologies, Si APDs and silicon photomultipliers (SiPM) [52] are used as the detector of choice for the NIR range while InGaAs-on-InP linear mode APDs and SPADs [53]–[55] are used in 1550 nm LiDAR systems, albeit at a higher cost than Si. Signal detection can be complicated in an automotive LiDAR system due to the exposure and detection of external ambient light sources from the environment (including laser light from other vehicular lasers and the Sun). Despite having narrow bandwidth bandpass filters incorporated to reject ambient light from background solar radiation, background photocurrent is unavoidable and depending on the detector field of view, size, and other factors, may contribute nWs (at 1.5 μm wavelength) of power into the detector [56], considering state-of-the-art InGaAs may only have dark currents in the range of nA (depending on the bias voltage) [57]. In the case of SPAD detectors, background signals can create false avalanche pulses that will hinder the correct detection of return signals [51]. Furthermore, reflected signals stronger than expected (either from retroreflectors on the road or a fast-moving vehicle crossing the laser path) can result in signal contamination or worse, damage to the detectors [58]. Hence, dedicated data processing units with signal identification and rejection algorithms are required as part of a LiDAR system [59].

Depending on the MPE to maintain eye safety standards and the laser pulse energy required for signal detection [60], the sensitivity required from the detector varies, going from the most sensitive SPADs to linear mode APDs and finally to unity gain

photodiodes. Considering the relation between operating wavelength and laser pulse energy, using higher power at 1550 nm wavelength signals (6 orders of magnitude higher MEP than 905 nm) also offers benefits in the choice of detector, allowing smaller area, large format arrays (advantageous for noise suppression) [61]. For example, a simple p-i-n InGaAs photodiode array (useful for their low dark current at low bias and lack of cooling hardware needed) has demonstrated a range of 51 m and 159 m using laser pulse energies of 300 μJ and 3 mJ respectively [62]. When comparing APD and SPAD performances for LiDAR, there are clear strengths and weaknesses of each option, some of which has been mentioned along the texts [51]. Admittedly, while both detector choices require some form of cooling for different reasons (reduced dark counts in SPADs and temperature stability of gain in APDs); in SPADs, the generated current pulses are more uniform than in APDs due to the stochastic nature of the avalanche process which also results in a long timing jitter. However, SPADs have a dead time after detection and APDs are advantageous in 3D ranging because the signal amplitude is proportional to the distance travelled by the return signal [51].

Hamamatsu features room temperature SiPM-based LiDAR sensor with a total of 2668 pixels and a pixel pitch of 25 μm, with a capacitance of 65 pF, 6% crosstalk and a dark count rate of 500 kHz [63]. Voxtel has demonstrated a 256 x 256 Si-based SPAD image sensor with pixel pitch of 30 μm, a low dark count rate of 55 Hz and a 0.4 V variation in breakdown voltage (of 18.75 V), though this is not yet commercially available [64]. The Voxtel portfolio also boasts arrays of sub-50 μm pixel pitch, high gain InGaAs-based APDs with array sizes up to 128 x 128 [65]. 1 x 16 SiPM linear arrays with pixel sizes of 10 μm by ON Semiconductors has capacitances of 59 pF, 25% crosstalk and dark count rate of 30 kHz [66]. Taking HgCdTe, another electron-APD material (discussed in more detail in Section 1.4) as a benchmark for comparison, HgCdTe APD arrays for LiDAR applications have been demonstrated [67]. The 4x4 array with a pixel pitch of 80 μm was reported to show uniform gain, quantum efficiency and dark current performances. When used in conjunction with a ROIC, bandwidths up to 7 MHz were obtained and the operating temperature is controlled by an integrated Stirling cooler, providing an integrated detector module. Similar to HgCdTe, InAs is also an electron-APD material with a narrow bandgap; while InAs in

LiDAR applications have yet to be demonstrated, it is expected that in the future, with more development InAs APDs will achieve similar performances.

1.2 Infrared imaging

Imaging in infrared wavelengths can provide information that is otherwise invisible, or hidden when using conventional visible light imaging systems. Furthermore, visible light imaging can become limited by the lack of an illumination source, such as imaging during nighttime. Visible light ranging from roughly 400 to 700 nm, is perceivable by the human eyes. Hence, it is no surprise that is the most common imaging wavelengths available to humans as information can be conveyed without any need of further interpretation. The first coloured still image was captured by James Clerk Maxwell back in 1861 [68], followed by the invention of coloured motion pictures roughly four decades later in 1899 by Edward Raymond Turner [69]. The analogue techniques, since then, have been replaced by solid-state technology and digital image processing methods. Beyond the visible light wavelengths is the infrared regime spanning from 700 nm up to 1 mm and is generally split into a number of bands: 1) the near-infrared band from 700 nm to 1.4 μm, 2) the short-wave infrared band from 1.4 to 3 μm, 3) the mid-wave infrared (MWIR) band from 3 to 8 μm, 4) the long-wave infrared (LWIR) band from 8 to 15 μm and 5) the very long-wave infrared (VLWIR) territory after 15 μm.

One form of infrared source, and perhaps the most prominent, is black-body radiation, that is a characteristic spectrum of electromagnetic radiation emitted by any object of a given temperature [70]. Black-body radiation is also sometimes known as thermal radiation due to the dependence on the object's temperature, where a higher temperature corresponds to a shorter peak wavelength, and is described by Planck's law [70]. These natural occurring infrared radiation can be detected such as in thermal imaging of the human body for temperature monitoring. The peak wavelength of a black-body source, λ_{peak}, is given by $\lambda_{peak} = {2.898 * 10^{-3}}/{T}\ (\mu m)$, where T is the temperature, from Wien's displacement law [71]. For the case of the human body temperature, the peak wavelength lies approximately at 9.5 μm in the LWIR region which can be picked up by a microbolometer [72]. Disease diagnostics in biomedical applications from the black-body principle have been demonstrated, such as observing temperature gradients around acute inflammations in arthritic patients [73].

Unlike visible light imaging which is rendered useless in the absence of sunlight under night time conditions, SWIR imaging can function due to night illumination, otherwise known as nightglow, that has a peak emission around 1.6 μm [74]. Imaging can be performed by detecting nightglow reflections from objects in the scene [75], [76] or by actively illuminating the scene with a laser source and detecting the reflected signals [77], [78], akin to ToF LiDAR operation. When operating in the active sensing mode, gated viewing operation is normally employed where the camera is switched on with a delay after the laser pulse is sent. As a result, imageries from backscattered signals due to fog and dust are ignored and only signals from a set distance away will be registered [79]. An added advantage that infrared imaging possesses is the ability for infrared light to better penetrate through obscurants such as fog, smoke and haze over visible light [80]. Light traversing through an atmosphere laced with tiny particles can be scattered and dispersed, leading to low amounts of return signals and diminished image quality. This form of elastic scattering, Rayleigh scattering, has an inverse relation with the fourth power of wavelength and therefore can be mitigated by using longer wavelength light in the infrared regions [81]. Due to the lack of colour information in an infrared system, image formation instead requires extensive image processing algorithms to reconstruct the large amounts of data for image acquisition [82].

1.3 Telecommunication systems

With the birth of optical fibres, long distance communication using electrical signals via copper telegraph cables were made obsolete. Today, a dense network of hundreds of undersea fibre optic cables form the backbone of modern telecommunications [cite undersea cable website]. Early generations of optical data transmission functioned at the wavelength range of 800 – 900 nm, using GaAs/AlGaAs based laser diodes and LEDs paired with Si detectors [83]. With improvements towards the manufacturing of high purity silica fibres [84], the operational wavelength shifted towards infrared wavelengths of 1.3 and 1.5 μm where the losses (due to absorption and scattering in silica) are the lowest. To meet increasing demands for high data rate, modern engineers utilise techniques such as wavelength division multiplexing (WDM) to combine signals of different (but closely spaced) wavelengths into a single optical fibre for

transmission. An optical communication system typically consists of laser diodes, modulators, (de-)multiplexer, optical fibres, photodetectors, and readout electronics.

The bandwidth of a photodetector is determined by the transit time, that is the time it takes for photogenerated carriers to exit the high field junction, and the RC time constant that arises from the diode series resistance and junction capacitance. For a fast response, the carriers are ideally absorbed in the depletion region where the built-in electric field is present. The junction capacitance is inversely proportional to the depletion width, which is dependent on the doping concentrations in a p-n diode. To minimise the capacitance, small area p-i-n detectors with a thick, low background doping concentration intrinsic region are used. This, however, compromises the carrier transit time by creating a larger distance for carriers to traverse and also a smaller light sensitive area. There are also trade-offs to be made with the detector quantum efficiency which require a long depletion width due to the exponential relation of light absorption. Hence, the design of photodetectors is complicated by a number of competing factors to consider. There are, therefore, a number of engineered methods to produce high speed photodiodes, namely the resonant cavity structure photodiode (increased quantum efficiency by reflecting unabsorbed light back into a thin depletion region) [85], the uni-travelling carrier photodiode (bandgap engineered to only allow electron drift) [86] and waveguide photodiodes (side-illuminated so that the direction of carrier movement and light propagation are different) [87]. Other than the aforementioned factors affecting the detector bandwidth, the bandwidth of APDs is also governed by carrier feedback and build up during the avalanche process where a higher gain generally increases the avalanche build up time and lowers the bandwidth [88].

For a typical photodetector-amplifier receiver system, utilising an APD over a p-i-n photodiode is more advantageous in improving the receiver sensitivity as the amplifier noise generally dominates over a p-i-n photodiode (discussed further in Section 2.2) [89]. There are a number of constraints that limit the sensitivity of an APD such as dark current, carrier ionisation rates and avalanche excess noise factor [90]. To assess the receiver sensitivity, it is common to evaluate the minimum signal power required to produce a bit error rate (BER) of typically, 10^{-12}, where the BER refers to the probability of an incorrect measurement of "1" or "0" will be made. In order to satiate the rapid growth of transmission capacity, APDs capable of 25 Gb/s [91] and 50 Gb/s

[92] operation have been demonstrated. The most dominant material for telecommunications wavelength is InGaAs which has a bandgap energy of 0.75 eV at room temperature, corresponding to a cutoff wavelength of 1.7 μm which adequately covers the telecommunications bands from 1.3 to 1.6 μm. This provides a natural advantage to using InGaAs without incurring deficits (such as high dark currents) when using materials with narrower bandgap, for example InAs, that is able to cover a similar wavelength range. To circumvent the issue of high dark currents, one can reduce the active device area, typically to radii of 10 to 30 μm (which also carries along an added advantage of lowered junction capacitance suited for high speed operations), however, InAs devices with small dimensions have not yet been demonstrated. Another strategy to adopt InAs as telecommunications APD is to couple incoming signal through side illumination using an integrated packaging solution with lensed fibre since thick intrinsic region widths of up to 10 μm is generally sought for in InAs for high gain at low operating voltages.

1.4 Literature review

Solid-state solutions are favoured in modern technologies for their compactness and mass-manufacturability. Imaging sensors made with CMOS technology are able to keep up with Moore's law, reducing in pixel sizes to allow a greater packing density [93]. In a modern digital camera, millions of pixels, each an individual semiconductor device, can be packed into an area less than 1 cm^2 [94]. Semiconductor devices are widely used in the aforementioned applications and in the heart of these systems, a light-sensitive photodetector is required.

1.4.1 InAs

InAs is one such photodetector material from the III-V semiconductor family that is suitable and attractive for its narrow band gap of 0.36 eV, translating to a detection wavelength of 3.4 μm in the MWIR region. This section will mainly focus on InAs photodiodes and APDs, an extensive review on other facets of the InAs material can be found in Ref. [95].

One of the earliest report of InAs photodiode is by Lucovsky [96], where a p-n junction diode is formed via Cd diffusion into an n-type InAs with its forward and reverse current characteristics behaving as expected from conventional diode theory. Further

probing reveals the onset of avalanche multiplication at a reverse bias of -0.9 V in these InAs photodiodes, obtaining a multiplication factor of 10 at -10 V [97]. Fundamental properties such as the absorption coefficients at the InAs band edge as a function of donor and acceptor impurities were also investigated by Dixon and Ellis [98] as well as minority carrier diffusion lengths and surface recombination velocity in photovoltaic InAs p-n junctions by Mikhailova *et al.* [99]. Mikhailova went on to be the first to attempt to derive ionisation coefficients of InAs to show that indeed a relatively low electric field strength is needed to obtain carrier multiplication in InAs [100]. In the same work, it was also concluded that the hole ionisation coefficient is an order magnitude larger than the electron ionisation coefficient which is attributed to a resonance effect of holes in the spin-orbit split-off valence band.

Hereafter, developments in InAs photodiodes slowed down despite showing promise as a mid IR photodetector as compared to InSb which possesses a smaller band gap that covers the entire MWIR band. One reason perhaps, is due to the Fermi level lying above the conduction band minimum at InAs surfaces, resulting in an accumulation of electrons in the conduction band at the surface-bulk boundary [101]. These surface charges are thought to originate from an excess of anions, from antisite defects and dangling bonds, giving donor-like properties and contributing to excess electrons [102]. The phenomenon is observed in both In-rich and As-rich surfaces [103], [104] and detailed experimentally as well [105], [106]. This resulted in difficulties in producing practical InAs devices due to the lack of surface passivation techniques to remove these surface accumulation charges and suppress surface leakage currents. Lin *et al.* demonstrated suppressed leakage currents in unpassivated InAs p-i-n photodiodes as opposed to regular p-n junction photodiodes [107]. A further systematic study by the same authors with temperature dependent current-voltage (I-V) characteristics revealed that an increasing i-layer thickness from 0 to 720 nm effectively suppresses tunnelling currents, explaining the advantages of p-i-n InAs diodes compared to a simple p-n junction [108]. Around a similar time period, Iwamura and Watanabe produced InAs p-n diodes by diffusion of Zn atoms [109] with a peak responsivity of 0.28 A/W at 3.2 μm but with dark currents roughly 100 times higher than in [108]. Zn-diffusion in InAs diodes were studied in [110], comparing the leakage currents as a function of diffusion temperature and time. Despite having poor diode characteristics and potentially surface-limited currents at low temperatures, the

work demonstrated an InAs array capable of detection of alpha particles. Several authors have also reported homojunction and heterojunction (with a lattice matched p-type InAsSbP grown on InAs substrate) InAs photodiodes while investigating the temperature dependent I-Vs, in particular trap-assisted tunnelling currents [111]–[113].

Dobbelaere *et al.* investigated InAs photodiodes grown heteroepitaxially on GaAs and GaAs-on-Si substrates in hopes of realising monolithic integration of InAs infrared detectors with read-out electronics [114]. Unsurprisingly, the device performance degrades due to large amounts of dislocations at the highly mismatched interface as compared to homoepitaxial InAs diodes. Even so, the authors demonstrated the monolithic integration of InAs photodiode with a GaAs MESFET in a separate publication [115]. Shi *et al.* also demonstrated high speed operation up to 20 GHz from Zn-diffused InAs photodiodes grown on semi-insulating GaAs substrates that is limited by the inherent electron transit [116]. Over the years, growth of InAs epilayers have been demonstrated via various techniques ranging from liquid phase epitaxy (LPE) [117] to molecular beam epitaxy (MBE) [118] and also metal-organic vapour phase epitaxy (MOVPE) [119].

The drought on InAs based detector research persisted until Marshall *et al.* demonstrated bulk-dominated leakage currents using a combination of etchants, namely phosphoric acid : hydrogen peroxide : de-ionised water (H_3PO_4:H_2O_2:DIW) in a 1:1:1 ratio followed by sulphuric acid : hydrogen peroxide : de-ionised water (H_2SO_4: H_2O_2:DIW) in a 1:8:80 ratio (which will now be referred to as the standard etching recipe for InAs) [120]. Prior to this work, the same authors have also shown multiplication in a number of p-i-n and n-i-p InAs diodes where it was observed that multiplication due to electrons are larger than multiplication due to holes [121], directly in contrary to the reports by Mikhailova *et al.* in 1976 [100]. Further experimental work shows multiplication due to mixed injection of absorbed excitation light in the intrinsic region to be greater than hole initiated multiplication in n-i-p diodes [122] and the avalanche excess noise under pure electron injection condition to be less than 2 (the theoretical minimum according to McIntyre's ionisation theory [123] which will be further discussed in chapter 2) [124]. The latter is characteristic of single carrier multiplication (SCM), i.e. $k = 0$, where k is the ratio of hole (β) to electron (α) ionisation coefficient, which is also seen in HgCdTe APDs [125].

Theoretical calculations on impact ionisation in InAs by Monte Carlo methods have been performed separately by Brennan [126] and Satyanadh [127] where the parameterised electron ionisation coefficients from the former are similar to the experimental findings of Marshall. A series of p-i-n and n-i-p diodes characterised in [128] showed that electron impact ionisation is confined within the Γ valley due to the very low electric field required for multiplication and β is negligible in InAs within the studied range of electric field.

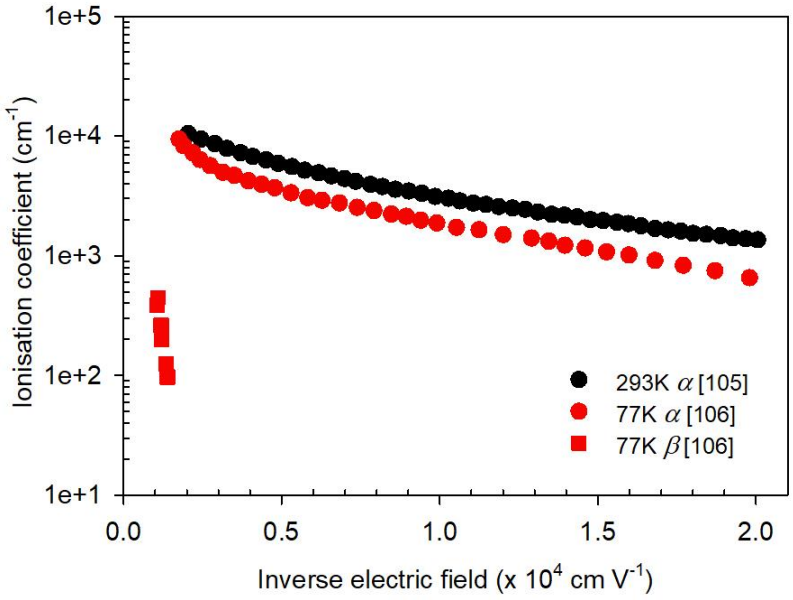

Figure 1.1 Electron and hole ionisation coefficients of InAs at 293 [105] and 77 K [106]

Single carrier multiplication promises several unique properties in e-APDs. Following multiplication theory in a device with uniform electric field, the multiplication due to electrons, M_e is given by $M_e = \exp(\alpha W)$ where W is the depletion width. That is to say, multiplication scales exponentially with the depletion width at a given α. In addition, the electron ionisation coefficient of InAs remains relatively constant under low electric field range as seen from Fig. 1.1, resulting in a strong dependence of multiplication on the depletion width. For a p-i-n diode, given a sufficiently low background carrier concentration in the intrinsic region, the APD gain will increase with the i-region thickness. This has been observed at room temperature [128] and at 77 K [129]. Interestingly, in [129], it was found that the electron ionisation coefficient has a positive temperature dependence, i.e. the obtainable multiplication at a given electric field is lower at reduced temperatures and this contradicts with other known III-V APDs. The absence of (or lack of) hole-initiated impact ionisation gives rise to

a more deterministic occurrence of impact ionisation, thereby generating lower avalanche excess noise and also removes any carrier feedback in the depletion width. The maximum avalanche build-up time, which is the total duration for all charges created by the avalanche process to leave the high field region, therefore has a maximum limit that is the sum of the transit time of electron and that of hole. Again, this is different from conventional APD materials where the device bandwidth is influenced by the avalanche gain [130]. Gain-independent bandwidth in InAs has been demonstrated in [131] where a gain-bandwidth product (GBP) of 580 GHz at a bandwidth of 3 GHz, the highest in any III-V APDs at the time, has been achieved. Ranging experiments at MWIR wavelengths also show picosecond time resolution [132], further attesting to short avalanche pulses in InAs. To obtain a large GBP for telecommunication applications using InAs APDs, there is likely a trade-off between the gain and bandwidth as the former relies on a long depletion width for a large build-up of avalanche carriers and the latter requires a distance as short as possible for carriers to exit. Recent sensitivity analysis on InAs APDs however, does point that at data rates of 10 and 25 Gb/s at 1550 nm wavelength, InAs APDs offer superior performance over InAlAs APDs but falter against Si/Ge alternatives at 1330 nm. To remain competitive, the dark current performance of InAs APDs requires further improvement [133].

To digress slightly, one main reason for the prominence of Silicon devices amongst the many different semiconductor materials is the ease to form SiO_2 layers as encapsulants for exposed semiconductor surfaces. Unfortunately for III-V compound semiconductors, the lack of a simple and effective method of passivation presents a major barrier to producing stable, robust practical devices. In InAs, oxide formation mechanisms are complicated by the fact that various composition of In_xO_y, As_xO_y and even ternary oxides of In-As-O can exist [134]. Following the works by Kim to suppress leakage currents in InAs/GaSb superlattice detectors [135], a passivation scheme using spin-coated SU-8 photoresist on InAs APDs was employed to give reduced leakage currents [136]. This allowed a systematic study on the temperature dependence of dark I-Vs, the analysis of dominant current mechanisms and the origin of said mechanisms [137], [138] along with detailed measurements on the temperature dependence of avalanche gain and excess noise in InAs [139]. An analytical band Monte Carlo model [140] developed to model impact ionisation in InAs explains that

the positive temperature dependence of avalanche gain in InAs is due to a more dominant effect temperature has on the ionisation threshold energy, E_{th}, than the that of phonon scattering. The reasoning given is that due to the large intervalley (Γ-L and Γ-X) separation energies in InAs, carriers capable of initiating impact ionisation (i.e. with energies exceeding the E_{th}) are largely confined to low scattering Γ and L valleys which are influenced to a greater degree by increased E_{th} at reduced temperatures.

Separate from the Sheffield group, Bank's group in University of Texas has also demonstrated InAs APDs [141], [142] with similar gain and excess noise characteristics, proving that early work by Mikhailova *et al.* was anomalous. Monte Carlo simulations in [141] argues that due to decreased absorption of optical phonons at 77 K, carriers gain energy at a much slower rate. At the same time, E_{th} for impact ionisation, that is proportional to the band gap, increases at lower temperatures, hence the overall carrier multiplication decreases at reduced temperatures.

Further work sees more polished fabrication techniques applied to develop InAs APDs in producing a uniform linear array of 128 diodes [143] as well as reports that are geared towards different applications of the mid-infrared APD such as in radiation thermometry [144] and X-ray detection [145]. One teething problem with the development of InAs APDs thus far, is the use of mesa structure devices fabricated via chemical wet etching. Whilst the standard etch recipe along with SU-8 passivation shows sufficiently suppressed surface leakage current, the APDs were not sufficiently robust to withstand repeated measurements under low temperatures due to thermal cycling that leads to eventual degradation in device performance. Furthermore, from the array work, it is apparent that current InAs APD designs, relying on thick i-layers to achieve high gains, poses difficulties during device fabrication. Namely, necessitating the need for careful passivation of the huge amounts of exposed sidewall surface area and also the reduced fill factors in an array from the isotropic wet etch process. To circumvent these issues, planar InAs diodes were developed by Be-ion implantation [146] where the authors developed the implantation process and the accompanying annealing conditions. The APDs produced showed dark currents comparable to mesa InAs APDs at cryogenic temperatures, high gain up to 330 and no edge breakdown effects [147]. Preliminary work on extending the detection wavelength in InAs further into the MWIR region has also been performed by incorporating Bi atoms into InAs. Early works showed that the presence of Bi atoms

by X-ray diffraction [148] and photoluminescence [149], [150] where band gap reductions of 55 and 38 meV/%Bi was observed in [149] and [150] respectively. Sandall *et al.* then demonstrated InAsBi photodiodes with 1.5% Bi incorporation, successfully increasing the cutoff wavelength to 3.95 μm at 225 K [151]. This remains a field to be explored due to the difficulties associated with Bi-related growth.

1.4.2 Mercury Cadmium Telluride (MCT)

The material, MCT (also commonly known as $Hg_{1-x}Cd_xTe$ or simply HgCdTe), is perhaps the most dominant material in the field of infrared detection from the SWIR to LWIR range. This is because the band gap of $Hg_{1-x}Cd_xTe$ can be varied from 0 to 1.5 eV since HgTe is a semimetal and CdTe has a band gap of 1.5 eV. Lawson *et al.* was the first to discover the unique properties of HgCdTe by mixing HgTe and CdTe crystals where it was observed that the absorption wavelength extends to more than 15 μm with increasing Hg concentration [152]. Decades long of development in MCT dug deep into the fundamentals of the material system to aid future design and device optimisation as well as studies into crystal growth on various substrate, going from CdTe and ZnCdTe to sapphire or Si substrate to bring the overall production cost down and also for hybridisation with Si-based readout circuitries. MCT infrared detector technologies are now well-established, with up to large format 2-D arrays (up to megapixel-count) fully integrated with readout chips available [153]–[157]. Numerous authors have also reviewed MCT detectors in encyclopaedic details as in [158]–[161]. In this review, the focus will instead be placed on MCT APDs which is a comparatively younger technology.

The main motivation for early works on $Hg_{1-x}Cd_xTe$ APD was targeted for telecommunication applications in the SWIR around the 1.3 and 1.55 μm bands. It was known that by varying the ratio of HgTe-CdTe, the band structure of the alloy can be altered, along with the cutoff wavelength. In Cd-rich compositions, HgCdTe can be used for SWIR detection and the band structure exhibits a resonance effect between the band gap, E_g, and spin-orbit split-off band, Δ_{SO} [162]. As a result, hole impact ionisation is significantly enhanced such that a large ratio of β/α exists and potentially low-noise APDs can be attained with the MCT system. Lecoy studied the range of Cd compositions from $x \approx 0.6 - 0.7$, showing $E_g > \Delta_{SO}$ for $x \approx 0.7$ and impact ionisation due to holes from the spin-orbit band is favourable while the highest hole ionisation

coefficients and maximum β/α ratio can be obtained at a composition of $x \approx 0.6$ [163]. The theoretical calculations are backed up by a number of experimentalists where indeed multiplication due to holes are found to be greater than electron initiated multiplication [164]–[166]. $Hg_{0.3}Cd_{0.7}Te$ with a bandgap of 0.84 eV shows absorption up to 1.45 μm, hole multiplication greater than electron multiplication and $k = 10$ from excess noise measurements [164]. In a separate work, planar $Hg_{0.3}Cd_{0.7}Te$ photodiodes with a responsivity of 0.8 A/W at 1.3 μm exhibited a large discrepancy in multiplication characteristics with different carrier injection profiles where hole multiplication of 30 as compared to electron multiplication of 3 was obtained at -105 V [165]. de Lyon *et al.* demonstrated a separate absorption and multiplication (SAM) APD grown via MBE with the absorption and multiplication layer consisting of HgCdTe of different compositions, $x \approx 0.65$ and 0.73 for respectively. Avalanche gains more than 30 was obtained at -90 V with this structure [166]. Theoretical calculations by Leveque *et al.* showed with clarity that the ionisation coefficient ratio can be generally split into two regions depending on the Cd content. The first with high percentage of Cd where hole ionisation is significantly enhanced with a maximum at $x \approx 0.6$ due to the previously mentioned resonance effect and another where avalanche noise can remain low due to the dominant electron ionisation in small band gap, high Hg content alloys [167].

The works cited above have been focused on SWIR HgCdTe from the first regime Leveque *et al.* presented. The first LWIR HgCdTe APD with a cutoff wavelength of 11 μm was demonstrated by Elliott where a gain up to 5 at -1.3 V was obtained before eventually becoming limited by tunnelling currents [168]. The advantages of an electron-initiated avalanche process in MCT was made obvious by Beck *et al.* where an alloy composition of $Hg_{0.7}Cd_{0.3}Te$ with a cutoff wavelength of 5 μm grown by LPE was shown to produce high gains of 230 at -8 V with a near-unity avalanche excess noise and rise times around 1 ns [169]. Further works by Beck *et al.* demonstrated top-illuminated HgCdTe APDs with a p-around-n architecture from compositions ranging from 2 μm to 11 μm cutoff wavelengths. The SWIR, MWIR and LWIR APDs were able to produce gains of up to 20, 1000 and 100 respectively [125], [170]. The p-around-n cylindrical geometry refers to a common MCT device architecture known as high-density vertically integrated photodiode (HDVIP) with a detailed description of the design available in [171]. Separately, Vaidyanathan *et al.* also reported MWIR and

LWIR HgCdTe grown via MBE to produce gains of 1000 and 100 at voltage biases of -10 and -3 V [172]. Reine *et al.* reported back-illuminated planar APDs with 4.06 μm cutoff with gains up to 648 at -11.7 V, 160 K [173] as well as detailing various performance metrics of MCT APD such as spatial uniformity and temperature dependence of gain [174]. APDs with a GBP of 2.1 THz (gain = 3500, bandwidth = 600 MHz) have been demonstrated by Perrais *et al.* and the rise time was found to be limited by the diode capacitance [175].

Theoretical models explaining the unique multiplication process in HgCdTe were put forth by Kinch [176] and Ma [177]. The theories relate the near-ideal APD characteristics of MCT to the band structure. The much lower electron effective mass means that the scattering is weak and there is a net energy gain from the applied electric field as compared to the large effective mass and low mobility of holes. Furthermore, electrons are confined to the Γ valley due to large intervalley separation energies of 1.5 and 2.5 eV for the L and X valleys respectively, thereby electrons experience reduced intervalley scattering effects. The band structure of $Hg_{0.7}Cd_{0.3}Te$ can be therefore, be simplified to only the Γ valley and the heavy hole band. As a result of a large difference in effective masses, the electron ionisation threshold energy, $E_{th(e)}$, can be approximated as $\sim E_g$ while the hole ionisation threshold energy, $E_{th(h)}$, is roughly $\sim 2E_g$. Kinch [178] and Rothman [179], [180] have shown that the gain behaviour as a function of alloy composition and device geometry of HgCdTe e-APDs can be accurately predicted.

Having obtained thorough understanding of fundamental material properties coupled with the wide range of tunable infrared wavelengths has led to a number of application-oriented developments by exploiting the low noise signal amplification in HgCdTe APDs. The high gains of HgCdTe APDs can be relied upon in passive or active imaging systems. HgCdTe APD camera operating at a gain of 20 in a 320 x 256 pixel format has been demonstrated to successfully capture thermal images in passive mode and also carry out ToF measurements in active imaging mode, creating 2D and 3D images with depth information [181]. Imaging at long range up to 1.3 km and through smoke obscurants was demonstrated by Breiter *et al.* with a n-on-p design SWIR HgCdTe APD array made of 640 x 512 pixels [182]. Atmospheric and space LiDAR is one field where HgCdTe APD arrays flourish. A number of authors have reported the use of HgCdTe as the detector of choice for remote gas sensing such as at 1.57

[183] and 2 μm for CO_2 [184], [185] as well as at 1.65 μm the detection of CH_4 [183]. High sensitivity down to single or few photon levels [186] offered by MCT APDs makes for good photon counting detector arrays as demonstrated in the SAPHIRA linear mode APD arrays for astronomy [187], [188]. Vojetta *et al.* demonstrated linear mode APDs that can produce output signals proportional to the number of detected photons [189]. Sun *et al.* also demonstrated a custom-built receiver assembly, consisting of MWIR HgCdTe APDs in a 2 x 8 array with an integrated cooler for low temperature operation down to 80 K, that is capable of single photon detection [67].

1.4.3 Other SWIR and MWIR APD materials

1.4.3.1 InP-based APDs

The low loss transmission windows around 1300 and 1550 nm for long distance optical communications [190] prompted the use of InGaAs as the detector material, with a cutoff wavelength up to 1.65 μm. InGaAs p-i-n photodiodes offer high quantum efficiency due to high absorption coefficients [191]. However, substantial tunnelling currents due to the narrow band gap exist at high electric fields required for impact ionisation hinders APD performance of InGaAs [192]. The idea to use a wider band gap material such as InP or InAlAs (also lattice matched to InP with $In_{0.52}Al_{0.48}As$) as the multiplication region while keeping a narrow band gap material as the absorber region marked the birth of the separate absorption and multiplication avalanche photodiode (SAM-APD) [193], [194]. The SAM design enables higher sensitivity provided by avalanche multiplication, a uni-carrier injection profile to maintain low-noise multiplication while confining the high electric fields to the multiplication region thus limiting tunnelling currents. A low doping concentration is maintained in the absorber and multiplication region and in between, a highly-doped charge sheet layer (or otherwise known as a field control layer) is employed to adjust the high electric field from the multiplication region to a low electric field in the absorber region. One problem in the original design is carrier trapping at the hetero-interface between InGaAs and InP. To circumvent this, intermediate layers of varying quarternary compositions for a gradual transition in band gap are introduced [195], [196]. Therefore modern implementations of SAM-APDs are more accurately known as separate absorption, grading, charge and multiplication (SAGCM) [197].

To meet more stringent requirements in operation speed and bandwidth, the multiplication region thickness continued to shrink which inadvertently allowed the exploitation of dead space effects. As a result, more deterministic impact ionisation can be achieved and excess noise in SAM-APDs is reduced [198]. In spite of this, limitations due to the onset of tunnelling currents in devices with thin multiplication widths persist. $In_{0.52}Al_{0.48}As$ (hereinafter InAlAs) emerged as a material candidate for the multiplication layer with a number of advantages over InP. InAlAs has larger ionisation coefficient ratios at any given electric field when compared to InP, which by McIntyre's local model theory will result in lower excess noise [199], [200]. The larger band gap in InAlAs will manifest comparatively lower tunnelling currents [199], [200]. Furthermore, it has been shown that the ionisation coefficients of InAlAs is more temperature-insensitive than that of InP [201]. From a practical device processing viewpoint, edge breakdown in planar InAlAs APDs can be avoided without implementing guard ring structures [202]. Even so, SAM-APDs are unable to achieve high GBP due to the small disparity between the ionisation coefficients [92], [203], [204].

The quest in search of a material with large α/β ratio while maintaining lattice matching to the InP platform led to the $Al_xGa_{1-x}As_ySb_{1-y}$ (hereinafter AlGaAsSb) alloy system. Early reports of $AlAs_{0.56}Sb_{0.44}$ (from here on known as AlAsSb) observed low tunnelling current, attributed to the indirect band gap nature of the material, and very low temperature coefficient of breakdown voltage of 0.95 mV/K, superior to that of InP and InAlAs at 3.9 and 2.5 mV/K respectively [205]. Of particular note, excess noise measurements in p-i-n diodes with intrinsic region widths of 80 and 230 nm demonstrated k of 0.1 and 0.05, lower than those of InP and InAlAs [206]. By introducing Ga into the alloy, the dark currents were observed to be decreasing in p-i-n diodes with increasing Ga content [207]. Low excess noise from AlAsSb is also observed in diodes varying from 0 to 15% Ga [208], [209]. A record high GBP of 424 GHz at 1550 nm wavelength was obtained from an InGaAs/AlGaAsSb SAM-APD with a multiplication region width of 100 nm [210], further cementing the possibility of AlGaAsSb replacing InP and InAlAs. A meticulous investigation into a wider range of ionisation coefficients in AlAsSb reveals very dissimilar ionisation coefficients at relatively low electric fields that are present in thick multiplication widths [211] and therefore extremely low excess noise, close to $k = 0$, can be achieved

with an avalanche region thickness of 1.55 μm [212]. While no SAM structure incorporating very thick avalanche region of AlAsSb has been reported, it is worth mentioning this for the findings are in contrast to conventional knowledge of III-V APD materials.

The standard ternary alloy of $In_{0.53}Ga_{0.47}As$ on InP substrate cannot meet increasing needs for operation at wavelengths beyond 2 μm. One method is to increase the In content, thus reducing the band gap and increasing the cutoff wavelength. However, the lattice mismatch between an In-rich composition and InP brings about undesirable increases to dark currents and APD characteristics cannot be realised [213]. An alternative approach is to form a superlattice using $In_{0.53}Ga_{0.47}As$ and $GaAs_{0.51}Sb_{0.49}$ lattice matched to InP. Sidhu *et al.* demonstrated photodiodes with 43% quantum efficiency at 2.23 μm [214] and also APDs employing the superlattice as absorber (and InP as the avalanche material) with photoresponse up to 2.4 μm and gain exceeding 30 at room temperature [215]. Similarly, Ong *et al.* demonstrated SAM-APDs operating up to 2.5 μm with gains > 50 at room temperature using the $In_{0.53}Ga_{0.47}As/GaAs_{0.51}Sb_{0.49}$ superlattice as the absorber, however, with InAlAs as the multiplication region material instead [216]. Extending the photoresponse in the SWIR region can be achieved by incorporating bismuth into $In_xGa_{1-x}As$ to form $In_xGa_{1-x}As_{1-y}Bi_y$. It is known that the introduction of Bi induces a band gap reduction, of approximately 56 meV per percent of Bi in InGaAs [217], the material system can also maintain lattice matching on InP given the In/Ga ratio is adjusted [218]. The material remains in early research stages, however, preliminary works in photodiodes have shown promise in extending the cutoff wavelength of $In_xGa_{1-x}As_{1-y}Bi_y$ up to 2.6 μm while maintaining lattice matching [219], [220].

1.4.3.2 Si APDs

One contender for InP-based telecommunication APDs is silicon. While Si is known as a low-noise material with α/β ratios typically in the range of 10 – 100 [221], the band gap of Si limits its use in NIR operation. In fact, Si APD devices with a reach-through architecture (high-field multiplication region with a lightly-doped, low field absorber region [222]) was first used in the 800 – 900 nm telecommunication band [223]. To make use of the low noise and versatility of Si-based technology, SAM-APD devices using Ge as the absorber region and Si as the multiplication region were developed. A number of reports have demonstrated Ge/Si APD to operate at the 1.3 μm

telecommunication band [224]–[228]. Kang *et al.* demonstrated GBP up to 340 GHz, higher than most other InP-based APDs, with a sensitivity of -28 dBm at 10 Gbps and a bit-error rate (BER) of 10^{-12} [225]. Downsides to the Ge/Si include lattice mismatch between Ge and Si [229] leading to undesirable dark current characteristics as well as the weak absorption of Ge at 1550 nm due to its indirect band gap nature. Ge/Si waveguide APDs with Si thickness of 150 nm and 400 nm thick Ge absorber was shown to produce sensitivities, at a wavelength of 1550 nm, of -25 and -16 dBm at 12.5 and 25 Gbps respectively [228].

1.4.3.3 GaSb-based APDs

Infrared devices using GaSb substrate has mostly revolved around the fields of T2SL photodetectors [230] and interband or quantum cascade lasers [231]. Maddox *et al.* has shown that the $Al_xIn_{1-x}As_ySb_{1-y}$ (hereinafter AlInAsSb unless specific compositions are stated) alloy system can be grown lattice matched on GaSb and a large range of band gap tunability from 0.25 eV ($x = 0$) to 1.24 eV ($x \approx 0.75$) can be achieved, the largest of any III-V compound semiconductor [232]. Woodson reported excess noise measurements showing a k of 0.015 from a wide band gap composition with $x = 0.7$, demonstrating the feasibility of achieving low-noise APDs with this alloy [233]. A SAM structure utilising an $Al_{0.4}In_{0.6}As_{0.3}Sb_{0.7}$ absorber and an $Al_{0.7}In_{0.3}As_{0.3}Sb_{0.7}$ multiplication region was shown to produce APDs with k of 0.01 and gain of up to 50 [234]. The advantage of a tunable band gap in AlInAsSb SAM-APDs is apparent where band gap grading layers can be grown by varying the growth flux ratio directly. Varying compositions from $x = 0.3 - 0.7$ grown has shown experimentally the shift in cutoff wavelength (wavelengths beyond 1.6 μm possible with $x = 0.3$), increases in dark current and changes to the gain characteristics ($k \sim 0.01$ from compositions of $x = 0.5 - 0.7$) as the Al composition decreases [235]. As such, optimised APD designs can be realised with absorption further into SWIR wavelengths while maintaining low-noise multiplication characteristics using the AlInAsSb material system. Craig *et al.* also demonstrated a SAM-APD structure that employs a different alloy system on GaSb substrates using $Al_{0.9}Ga_{0.1}As_{0.08}Sb_{0.92}$ as the multiplication region and $In_{0.22}Ga_{0.78}As_{0.19}Sb_{0.81}$ as the absorber region with cutoff wavelength up to 2.75 μm [236].

1.5 Motivation and thesis layout

Mesa topology devices are usually employed for ease in device processing via wet chemical etching. In thick InAs APD structures, the standard etch recipe has been able to suppress surface leakages and provide sufficiently bulk properties at temperatures above 200 K. Leakage currents due to mid-gap G-R centres [138] remain a limiting factor to achieving lower dark currents. Continual increments to the intrinsic region thickness in InAs APDs is necessary to obtain higher gain and sensitivity at any given voltage bias, leading to an increase in exposed surfaces of the high field avalanche region and risk of device failure. As such, planar InAs APDs were developed in the hope of reducing surface leakage currents by having a decreased ratio of exposed surfaces to the device bulk. Initial work on planar APDs were produced using beryllium ion implantation at two energies, 70 and 200 keV, to achieve a p-doped region of 1 μm. Results achieved were comparable to reported works in mesa APDs and mid-gap defect states were observed in these APDs as well [147] which was thought to be due to the implant-induced damage. This, therefore, formed the basis of an investigation into whether ion implantation at low energies can yield APDs with reduced leakage currents.

Wet etching of InAs using a phosphoric acid mixture is known to produce a bevel angle approximately 45°, meaning every micron of material removed vertically results in roughly a micron of lateral etching as well. It is apparent then for an InAs mesa diode array, the photosensitive area will be reduced. Further difficulties posed by mesa arrays lie in device fabrication where tall, uneven structures causes non-uniformity in processing. This can be mitigated, or avoided, on a surface that is mostly flat with planar topology devices. The uniformity in terms of the electrical and optical characteristics of an array is a key figure of merit to the quality of array. It has been previously observed that dark current, responsivity and gain uniformity can be achieved to a certain extent in linear arrays of mesa InAs APD [143]. The uniformity of a planar linear array, with a newly developed mask set and fabrication processes adapted from previous planar APD development, are investigated.

Chapter 1 has given brief introductions to various real world applications where InAs APD arrays are applicable and can be attractive choices, a detailed review on InAs photodetectors, key competitors in HgCdTe APDs as well as other APD materials. The

following is an overview for the remainder of this thesis. In chapter 2, discussions about the theory of avalanche photodiodes, in particular on existing e-APDs materials, as well as ion implantation technology and photodiode array design will be given. The methodologies employed throughout this work in terms of the experimental setups and insights to various basic semiconductor theories are provided in chapter 3. Chapter 4 lists key results obtained from producing InAs APD using a relatively low energy Be-ion implantation at 34 keV where the work has contributed to a publication [237]. A comparison between mesa and planar linear arrays are made in chapter 5 with arguments from a device processing point-of-view provided on the cons of mesa linear array fabrication. Chapter 6 sees detailed analyses on the temperature dependence of optical and electrical characteristics as well as the optical sensitivity of the planar linear array. Results on small area diodes, isolation trench implementation and temperature cycling on the array are also be included. The conclusion and discussions on the future direction this work can take on are given in chapter 7.

1.6 References

[1] M. Franceschi, M. Martinelli, L. Gislimberti, A. Rizzi, and M. Massironi, 'Integration of 3D modeling, aerial LiDAR and photogrammetry to study a synsedimentary structure in the Early Jurassic Calcari Grigi (Southern Alps, Italy)', *Eur. J. Remote Sens.*, vol. 48, no. 1, pp. 527–539, Jan. 2015, doi: 10.5721/EuJRS20154830.

[2] J. U. Eitel *et al.*, 'Beyond 3-D: The new spectrum of lidar applications for earth and ecological sciences', *Remote Sens. Environ.*, vol. 186, pp. 372–392, 2016.

[3] J. Selbeck, V. Dworak, and D. Ehlert, 'Testing a vehicle-based scanning lidar sensor for crop detection', *Can. J. Remote Sens.*, p. 13, 2010.

[4] R. T. H. Collis, 'Lidar', *Appl. Opt.*, vol. 9, no. 8, pp. 1782–1788, 1970.

[5] P. L. Bender *et al.*, 'Accurate ranges have given a large improvement in the lunar orbit and new selenophysical informatic)n.', *Proc Conf Exp Tests Gravit. Theor.*, vol. 182, p. 11, 1971.

[6] J. L. Bufton and J. B. Garvin, 'Multi-Beam Surface Lidar for Lunar and Planetary Mapping', 1998.

[7] A. I. Carswell, 'Lidar measurements of the atmosphere', *Can. J. Phys.*, vol. 61, no. 2, pp. 378–395, Feb. 1983, doi: 10.1139/p83-049.

[8] W. B. Grant, R. H. Kagann, and W. A. McClenny, 'Optical Remote Measurement of Toxic Gases', *J. Air Waste Manag. Assoc.*, vol. 42, no. 1, pp. 18–30, Jan. 1992, doi: 10.1080/10473289.1992.10466965.

[9] Y. Sasano, E. V. Browell, and S. Ismail, 'Error caused by using a constant extinction/backscattering ratio in the lidar solution', *Appl. Opt.*, vol. 24, no. 22, p. 3929, Nov. 1985, doi: 10.1364/AO.24.003929.

[10] A. Ansmann, M. Riebesell, and C. Weitkamp, 'Measurement of atmospheric aerosol extinction profiles with a Raman lidar', *Opt. Lett.*, vol. 15, no. 13, p. 746, Jul. 1990, doi: 10.1364/OL.15.000746.

[11] R. Bureau, 'Altimétrie des nuages par impulsions lumineuses', *Meteorologie*, 1946.

[12] T. H. Maiman, 'Stimulated optical radiation in ruby', *Nature*, vol. 187, no. 4736, pp. 493–494, 1960.

[13] G. Fiocco and L. D. Smullin, 'Detection of scattering layers in the upper atmosphere (60–140 km) by optical radar', *Nature*, vol. 199, no. 4900, pp. 1275–1276, 1963.

[14] B. Cook *et al.*, 'NASA Goddard's LiDAR, Hyperspectral and Thermal (G-LiHT) Airborne Imager', *Remote Sens.*, vol. 5, no. 8, pp. 4045–4066, Aug. 2013, doi: 10.3390/rs5084045.

[15] G. Ehret *et al.*, 'MERLIN: A French-German Space Lidar Mission Dedicated to Atmospheric Methane', *Remote Sens.*, vol. 9, no. 10, p. 1052, Oct. 2017, doi: 10.3390/rs9101052.

[16] K. Hallgren, P. Hartogh, and C. Jarchow, 'Climatology of middle atmospheric water vapour above the ALOMAR observatory in northern Norway', *Atmospheric Chem. Phys. Discuss.*, vol. 12, no. 12, pp. 31531–31560, Dec. 2012, doi: 10.5194/acpd-12-31531-2012.

[17] M. Chiriaco *et al.*, 'ReOBS: a new approach to synthesize long-term multi-variable dataset and application to the SIRTA supersite', *Earth Syst. Sci. Data*, vol. 10, no. 2, pp. 919–940, May 2018, doi: 10.5194/essd-10-919-2018.

[18] F. Fitzpatrick, J. Hansell, T. Shuman, J. Young, and F. E. Hovis, ‘Laser transmitter development for a methane DIAL system (Conference Presentation)’, presented at the Novel Optical Systems, Methods, and Applications XXII, San Diego, California, United States, 2019. [Online]. Available: https://doi.org/10.1117/12.2532032
[19] R. L. Byer, ‘Remote air pollution measurement’, *Opt. Quantum Electron.*, vol. 7, no. 3, pp. 147–177, 1975.
[20] X. Liu, S. Cheng, H. Liu, S. Hu, D. Zhang, and H. Ning, ‘A Survey on Gas Sensing Technology’, *Sensors*, vol. 12, no. 7, pp. 9635–9665, Jul. 2012, doi: 10.3390/s120709635.
[21] E. V. Browell, S. Ismail, and S. T. Shipley, ‘Ultraviolet DIAL measurements of O 3 profiles in regions of spatially inhomogeneous aerosols’, *Appl. Opt.*, vol. 24, no. 17, pp. 2827–2836, 1985.
[22] S. Kuang, J. F. Burris, M. J. Newchurch, S. Johnson, and S. Long, ‘Differential Absorption Lidar to Measure Subhourly Variation of Tropospheric Ozone Profiles’, *IEEE Trans. Geosci. Remote Sens.*, vol. 49, no. 1, pp. 557–571, Jan. 2011, doi: 10.1109/TGRS.2010.2054834.
[23] K. Ikuta *et al.*, ‘Differential Absorption Lidar at 1.67 μm for Remote Sensing of Methane Leakage’, *Jpn. J. Appl. Phys.*, vol. 38, no. Part 1, No. 1A, pp. 110–114, Jan. 1999, doi: 10.1143/JJAP.38.110.
[24] N. Menyuk and D. K. Killinger, ‘Atmospheric remote sensing of water vapor, HCI and CH4 using a continuously tunable Co:MgF2 laser’, *Appl. Opt.*, vol. 26, no. 15, pp. 3061–3065, 1987.
[25] A. Minato, MD. M. A. Joarder, S. Ozawa, M. Kadoya, and N. Sugimoto, ‘Development of a Lidar System for Measuring Methane Using a Gas Correlation Method’, *Jpn. J. Appl. Phys.*, vol. 38, no. Part 1, No. 10, pp. 6130–6132, Oct. 1999, doi: 10.1143/JJAP.38.6130.
[26] T. F. Refaat *et al.*, ‘Backscatter 2-$\mu\hbox{m}$ Lidar Validation for Atmospheric $\hbox{CO}_{2}$ Differential Absorption Lidar Applications’, *IEEE Trans. Geosci. Remote Sens.*, vol. 49, no. 1, pp. 572–580, Jan. 2011, doi: 10.1109/TGRS.2010.2055874.
[27] N. Sugimoto and A. Minato, ‘Long-path absorption measurement of CO_2 with a Raman-shifted tunable dye laser’, *Appl. Opt.*, vol. 32, no. 33, p. 6827, Nov. 1993, doi: 10.1364/AO.32.006827.
[28] J. L. Bufton, T. Itabe, L. L. Strow, C. L. Korb, B. M. Gentry, and C. Y. Weng, ‘Frequency-doubled CO_2 lidar measurement and diode laser spectroscopy of atmospheric CO_2’, *Appl. Opt.*, vol. 22, no. 17, p. 2592, Sep. 1983, doi: 10.1364/AO.22.002592.
[29] G. Ehret, C. Kiemle, M. Wirth, A. Amediek, A. Fix, and S. Houweling, ‘Space-borne remote sensing of CO2, CH4, and N2O by integrated path differential absorption lidar: a sensitivity analysis’, *Appl. Phys. B*, vol. 90, no. 3–4, pp. 593–608, Mar. 2008, doi: 10.1007/s00340-007-2892-3.
[30] G. A. Wagner and D. F. Plusquellic, ‘Ground-based, integrated path differential absorption LIDAR measurement of CO_2, CH_4, and H_2O near 16 μm’, *Appl. Opt.*, vol. 55, no. 23, p. 6292, Aug. 2016, doi: 10.1364/AO.55.006292.
[31] G. G. Gimmestad, ‘Differential-Absorption Lidar for Ozone and Industrial Emissions’, in *Lidar*, vol. 102, C. Weitkamp, Ed. New York: Springer-Verlag, 2005, pp. 187–212. doi: 10.1007/0-387-25101-4_7.

[32] S. H. Melfi and D. Whiteman, ‘Observation of lower-atmospheric moisture structure and its evolution using a Raman lidar’, *Bull. Am. Meteological Soc.*, vol. 66, no. 10, pp. 1288–1292, 1985.
[33] U. Wandinger, ‘Raman Lidar’, in *Lidar*, vol. 102, C. Weitkamp, Ed. New York: Springer, 2005, pp. 241–271. [Online]. Available: https://doi.org/10.1007/0-387-25101-4_9
[34] W. B. Grant, ‘Differential absorption and Raman lidar for water vapor profile measurements: a review’, *Opt. Eng.*, vol. 30, no. 1, p. 40, 1991, doi: 10.1117/12.55772.
[35] G. S. Bumbrah and R. M. Sharma, ‘Raman spectroscopy – Basic principle, instrumentation and selected applications for the characterization of drugs of abuse’, *Egypt. J. Forensic Sci.*, vol. 6, no. 3, pp. 209–215, Sep. 2016, doi: 10.1016/j.ejfs.2015.06.001.
[36] D. Robineau, ‘Reported road casualties in Great Britain: main results 2018’, Department for Transport, 2019.
[37] T. Ogawa, H. Sakai, Y. Suzuki, K. Takagi, and K. Morikawa, ‘Pedestrian detection and tracking using in-vehicle lidar for automotive application’, in *2011 IEEE Intelligent Vehicles Symposium (IV)*, Baden-Baden, Germany, Jun. 2011, pp. 734–739. doi: 10.1109/IVS.2011.5940555.
[38] C. I. Rablau, ‘Lidar: a new self-driving vehicle for introducing optics to broader engineering and non-engineering audiences’, in *Fifteenth Conference on Education and Training in Optics and Photonics: ETOP 2019*, Quebec City, Canada, Jul. 2019, p. 138. doi: 10.1117/12.2523863.
[39] J. Hecht, ‘Lidar for self-driving cars’, *Opt. Photonics News*, vol. 29, no. 1, pp. 26–33, 2018.
[40] R. H. Rasshofer and K. Gresser, ‘Automotive Radar and Lidar Systems for Next Generation Driver Assistance Functions’, *Adv. Radio Sci.*, vol. 3, pp. 205–209, May 2005, doi: 10.5194/ars-3-205-2005.
[41] M. E. Warren, ‘Automotive LIDAR Technology’, in *2019 Symposium on VLSI Circuits*, Kyoto, Japan, Jun. 2019, pp. C254–C255. doi: 10.23919/VLSIC.2019.8777993.
[42] C. A. Gueymard, D. Myers, and K. Emery, ‘Proposed reference irradiance spectra for solar energy systems testing’, *Sol. Energy*, vol. 73, no. 6, pp. 443–467, 2002.
[43] A. Pacala, ‘How Multi-Beam Flash Lidar Works’, *Ouster*, Nov. 08, 2018. https://ouster.com/blog/how-multi-beam-flash-lidar-works/ (accessed Apr. 13, 2020).
[44] X. Sun, L. Zhang, Q. Zhang, and W. Zhang, ‘Si Photonics for Practical LiDAR Solutions’, *Appl. Sci.*, vol. 9, no. 20, p. 4225, Oct. 2019, doi: 10.3390/app9204225.
[45] M. Kutila, P. Pyykonen, W. Ritter, O. Sawade, and B. Schaufele, ‘Automotive LIDAR sensor development scenarios for harsh weather conditions’, in *2016 IEEE 19th International Conference on Intelligent Transportation Systems (ITSC)*, Rio de Janeiro, Brazil, Nov. 2016, pp. 265–270. doi: 10.1109/ITSC.2016.7795565.
[46] M. Bijelic, T. Gruber, and W. Ritter, ‘A Benchmark for Lidar Sensors in Fog: Is Detection Breaking Down?’, in *2018 IEEE Intelligent Vehicles Symposium (IV)*, Changshu, Jun. 2018, pp. 760–767. doi: 10.1109/IVS.2018.8500543.
[47] M. Jokela, M. Kutila, and P. Pyykönen, ‘Testing and Validation of Automotive Point-Cloud Sensors in Adverse Weather Conditions’, *Appl. Sci.*, vol. 9, no. 11, p. 2341, Jun. 2019, doi: 10.3390/app9112341.

[48] M. Kutila, P. Pyykonen, H. Holzhuter, M. Colomb, and P. Duthon, ‘Automotive LiDAR performance verification in fog and rain’, in *2018 21st International Conference on Intelligent Transportation Systems (ITSC)*, Maui, HI, Nov. 2018, pp. 1695–1701. doi: 10.1109/ITSC.2018.8569624.
[49] W. Koechner, ‘Optical ranging system employing a high power injection laser diode’, *IEEE Trans. Aerosp. Electron. Syst.*, vol. 1, pp. 81–91, 1968.
[50] T. Fersch, R. Weigel, and A. Koelpin, ‘Challenges in miniaturized automotive long-range lidar system design’, Anaheim, California, United States, May 2017, p. 102190T. doi: 10.1117/12.2260894.
[51] P. F. McManamon, P. Banks, J. Beck, A. S. Huntington, and E. A. Watson, ‘A comparison flash lidar detector options’, Baltimore, Maryland, United States, May 2016, p. 983202. doi: 10.1117/12.2229068.
[52] S. Gnecchi and C. Jackson, ‘A 1 × 16 SiPM Array for Automotive 3D Imaging LiDAR Systems’, in *Proceedings of the 2017 International Image Sensor Workshop (IISW)*, Hiroshima, Japan, 2017, p. 4.
[53] T. Baba *et al.*, ‘Development of an InGaAs SPAD 2D array for flash LIDAR’, in *Quantum Sensing and Nano Electronics and Photonics XV*, San Francisco, United States, Jan. 2018, p. 19. doi: 10.1117/12.2289270.
[54] P. A. Hiskett *et al.*, ‘Performance and design of InGaAs⁄InP photodiodes for single-photon counting at 1.55 □m’, p. 12.
[55] A. McCarthy *et al.*, ‘Kilometer-range depth imaging at 1550 nm wavelength using an InGaAs/InP single-photon avalanche diode detector’, *Opt. Express*, vol. 21, no. 19, p. 22098, Sep. 2013, doi: 10.1364/OE.21.022098.
[56] G. M. Williams and A. Huntington, ‘Laser Rangefinder Effective Range’, p. 7, 2018.
[57] Voxtel, ‘Voxtel APD Product Catalog’. 2016.
[58] M. Shand, ‘Origins and mitigations of some automotive pulsed lidar artifacts’, in *AI and Optical Data Sciences*, San Francisco, United States, Feb. 2020, p. 22. doi: 10.1117/12.2546976.
[59] M. Beer *et al.*, ‘SPAD-based flash LiDAR sensor with high ambient light rejection for automotive applications’, in *Quantum Sensing and Nano Electronics and Photonics XV*, San Francisco, United States, Jan. 2018, p. 85. doi: 10.1117/12.2286879.
[60] P. F. McManamon, ‘Design considerations for an auto LiDAR’, in *ODS 2019: Industrial Optical Devices and Systems*, San Diego, United States, Aug. 2019, p. 16. doi: 10.1117/12.2531442.
[61] G. M. Williams, ‘Optimization of eyesafe avalanche photodiode lidar for automobile safety and autonomous navigation systems’, *Opt. Eng.*, vol. 56, no. 3, p. 031224, Mar. 2017, doi: 10.1117/1.OE.56.3.031224.
[62] C. Bradley, S. Mukherjee, A. Reinhardt, P. F. McManamon, A. Lee, and V. Dhulla, ‘3D imaging with 128x128 eye safe InGaAs p-i-n lidar camera’, in *Laser Radar Technology and Applications XXIV*, Baltimore, United States, May 2019, p. 36. doi: 10.1117/12.2521981.
[63] Hamamatsu Photonics, ‘Multi-Pixel Photon Counter’. Nov. 2020.
[64] V. H. Dhulla, S. S. Mukherjee, A. O. Lee, N. Dissanayake, B. Ryu, and C. Myers, ‘256 x 256 dual-mode CMOS SPAD image sensor’, in *Advanced Photon Counting Techniques XIII*, Baltimore, United States, May 2019, p. 26. doi: 10.1117/12.2523084.
[65] Voxtel, ‘Detector Arrays—InGaAs APD’. 2021. Accessed: Feb. 24, 2021. [Online]. Available: https://voxtel-llc.com/products/detector-arrays-ingaas-apd/

[66] ON Semiconductor, 'Silicon Photomultipliers (SiPM), RDM-Series 1x16 Monolithic Array'. Dec. 2020.
[67] X. Sun, J. B. Abshire, J. D. Beck, P. Mitra, K. Reiff, and G. Yang, 'HgCdTe avalanche photodiode detectors for airborne and spaceborne lidar at infrared wavelengths', *Opt. Express*, vol. 25, no. 14, p. 16589, Jul. 2017, doi: 10.1364/OE.25.016589.
[68] G. Pelosi, 'James Clerk Maxwell: his journey to Italy; and the first color photograph', *IEEE Antennas Propag. Mag.*, vol. 50, no. 1, pp. 240–243, Feb. 2008, doi: 10.1109/MAP.2008.4494562.
[69] BBC, 'World's first colour film footage viewed for first time', Sep. 12, 2012. https://www.bbc.co.uk/news/uk-england-19557914 (accessed Apr. 13, 2020).
[70] M. Planck, *The Theory of Heat Radiation*. Courier Corporation, 2013.
[71] W. Wien, 'XXX. *On the division of energy in the emission-spectrum of a black body*', *Lond. Edinb. Dublin Philos. Mag. J. Sci.*, vol. 43, no. 262, pp. 214–220, Mar. 1897, doi: 10.1080/14786449708620983.
[72] M.-S. Han *et al.*, 'Low-cost compact thermal imaging sensors for body temperature measurement', Baltimore, Maryland, USA, Jun. 2013, p. 87041O. doi: 10.1117/12.2015662.
[73] E. F. J. Ring and K. Ammer, 'Infrared thermal imaging in medicine', *Physiol. Meas.*, vol. 33, no. 3, pp. R33–R46, Mar. 2012, doi: 10.1088/0967-3334/33/3/R33.
[74] R. H. Vollmerhausen and T. Maurer, 'Night illumination in the visible, NIR, and SWIR spectral bands', Orlando, FL, Aug. 2003, p. 60. doi: 10.1117/12.487189.
[75] F. Guellec *et al.*, 'A low-noise 15-µm pixel-pitch 640×512 hybrid InGaAs image sensor for night vision', in *Proc. SPIE 8298*, Burlingame, California, United States, 2012, p. 82980C.
[76] A. D. Hood, M. H. MacDougal, J. Manzo, D. Follman, and J. C. Geske, 'Large-format InGaAs focal plane arrays for SWIR imaging', Baltimore, Maryland, May 2012, pp. 83530A-83530A–7. doi: 10.1117/12.921475.
[77] O. Steinvall, M. Elmqvist, K. Karlsson, H. Larsson, and M. Axelsson, 'Laser imaging of small surface vessels and people at sea', Orlando, Florida, Apr. 2010, p. 768417. doi: 10.1117/12.849388.
[78] F. Rutz *et al.*, 'InGaAs SWIR photodetectors for night vision', in *Infrared Technology and Applications XLV*, Baltimore, United States, May 2019, p. 37. doi: 10.1117/12.2518634.
[79] D. Malchow, J. Battaglia, R. Brubaker, and M. Ettenberg, 'High speed short wave infrared (SWIR) imaging and range gating cameras', Orlando, Florida, USA, Apr. 2007, p. 654106. doi: 10.1117/12.721747.
[80] R. G. Driggers, V. Hodgkin, and R. Vollmerhausen, 'What good is SWIR? Passive day comparison of VIS, NIR, and SWIR', Baltimore, Maryland, USA, Jun. 2013, p. 87060L. doi: 10.1117/12.2016467.
[81] R. Penndorf, 'Tables of the refractive index for standard air and the Rayleigh scattering coefficient for the spectral region between 0.2 and 20.0 µ and their application to atmospheric optics', *J. Opt. Soc. Am.*, vol. 47, no. 2, pp. 176–182, 1957.
[82] R. Tobin, A. Halimi, A. McCarthy, M. Laurenzis, F. Christnacher, and G. S. Buller, 'Depth imaging through obscurants using time-correlated single-photon counting', in *Proc. SPIE 10659*, Orlando, United States, May 2018, p. 9. doi: 10.1117/12.2305369.

[83] H. Melchior and A. R. Hartman, ‘Epitaxial silicon n+-p-π-p+ avalanche photodiodes for optical fiber communications at 800 to 900 nanometers’, *IEEE Int. Electron Device Meet.*, pp. 412–415, 1976.
[84] C. K. Kao, ‘Nobel Lecture: Sand from centuries past: Send future voices fast’, *Rev. Mod. Phys.*, vol. 82, no. 3, pp. 2299–2303, Aug. 2010, doi: 10.1103/RevModPhys.82.2299.
[85] I. Kimukin, N. Biyikli, B. Butun, O. Aytur, S. M. Unlu, and E. Ozbay, ‘InGaAs-based high-performance p-i-n photodiodes’, *IEEE Photonics Technol. Lett.*, vol. 14, no. 3, pp. 366–368, Mar. 2002, doi: 10.1109/68.986815.
[86] T. Ishibashi, S. Kodama, N. Shimizu, and T. Furuta, ‘High-Speed Response of Uni-Traveling-Carrier Photodiodes’, *Jpn. J. Appl. Phys.*, vol. 36, no. Part 1, No. 10, pp. 6263–6268, Oct. 1997, doi: 10.1143/JJAP.36.6263.
[87] K. Kato, S. Hata, A. Kozen, J.-I. Yoshida, and K. Kawano, ‘High-efficiency waveguide InGaAs pin photodiode with bandwidth of over 40 GHz’, *IEEE Photonics Technol. Lett.*, vol. 3, no. 5, pp. 473–474, May 1991, doi: 10.1109/68.93883.
[88] J. C. Campbell, ‘Recent Advances in Telecommunications Avalanche Photodiodes’, *J. Light. Technol.*, vol. 25, no. 1, pp. 109–121, Jan. 2007, doi: 10.1109/JLT.2006.888481.
[89] M. Nada *et al.*, ‘High-speed III-V based avalanche photodiodes for optical communications—the forefront and expanding applications’, *Appl. Phys. Lett.*, vol. 116, no. 14, p. 140502, Apr. 2020, doi: 10.1063/5.0003573.
[90] D. S. G. Ong, Jo Shien Ng, M. M. Hayat, Peng Sun, and J. David, ‘Optimization of InP APDs for High-Speed Lightwave Systems’, *J. Light. Technol.*, vol. 27, no. 15, pp. 3294–3302, Aug. 2009, doi: 10.1109/JLT.2009.2020303.
[91] S.-L. Wu *et al.*, ‘High-Speed In $_{0.52}$ Al $_{0.48}$ As Based Avalanche Photodiode With Top-Illuminated Design for 100 Gb/s ER-4 System’, *J. Light. Technol.*, vol. 36, no. 23, pp. 5505–5510, Dec. 2018, doi: 10.1109/JLT.2018.2876168.
[92] M. Nada, T. Yoshimatsu, Y. Muramoto, H. Yokoyama, and H. Matsuzaki, ‘Design and Performance of High-Speed Avalanche Photodiodes for 100-Gb/s Systems and Beyond’, *J. Light. Technol.*, vol. 33, no. 5, pp. 984–990, Mar. 2015, doi: 10.1109/JLT.2014.2377034.
[93] E. R. Fossum, ‘CMOS Image Sensors: Electronic Camera-On-A-Chip’, *IEEE Trans. ELECTRON DEVICES*, vol. 44, no. 10, p. 10, 1997.
[94] U. Muehlmann, M. Ribo, P. Lang, and A. Pinz, ‘A new high speed cmos camera for real-time tracking applications’, in *IEEE International Conference on Robotics and Automation, 2004. Proceedings. ICRA ’04. 2004*, New Orleans, LA, USA, 2004, pp. 5195–5200. doi: 10.1109/ROBOT.2004.1302542.
[95] A. G. Milnes and A. Y. Polyakov, ‘Indium arsenide: a semiconductor for high speed and electro-optical devices’, *Mater. Sci. Eng. B*, vol. 18, no. 3, pp. 237–259, Apr. 1993, doi: 10.1016/0921-5107(93)90140-I.
[96] G. Lucovsky, ‘Electrical characteristics of diffused InAs p-n junctions’, *Br. J. Appl. Phys.*, vol. 12, no. 6, pp. 311–312, Jun. 1961, doi: 10.1088/0508-3443/12/6/111.
[97] G. Lucovsky and R. B. Emmons, ‘Avalanche multiplication in InAs photodiodes’, *Proc. IEEE*, vol. 53, no. 2, pp. 180–180, 1965.
[98] J. R. Dixon and J. M. Ellis, ‘Optical Properties of n -Type Indium Arsenide in the Fundamental Absorption Edge Region’, *Phys. Rev.*, vol. 123, no. 5, pp. 1560–1566, Sep. 1961, doi: 10.1103/PhysRev.123.1560.

[99] M. P. Mikhailova, D. N. Nasledov, and S. V. Slobodchikov, ‘Spectral Response of the Photoeffects in InAs’, *Phys. Status Solidi B*, vol. 11, no. 2, pp. 529–534, 1965, doi: 10.1002/pssb.19650110204.
[100] M. P. Mikhailova, N. N. Smirnova, and S. V. Slobodchikov, ‘Carrier multiplication in InAs and InGaAs p-n junctions and their ionization coefficients’, *Sov. Phys.-Semicond.*, vol. 10, no. 5, pp. 509–513, 1976.
[101] D. C. Tsui, ‘Observation of Surface Bound State and Two-Dimensional Energy Band by Electron Tunneling’, *Phys. Rev. Lett.*, vol. 24, no. 7, pp. 303–306, Feb. 1970, doi: 10.1103/PhysRevLett.24.303.
[102] L. F. J. Piper, T. D. Veal, M. J. Lowe, and C. F. McConville, ‘Electron depletion at InAs free surfaces: Doping-induced acceptorlike gap states’, *Phys. Rev. B*, vol. 73, no. 19, p. 195321, May 2006, doi: 10.1103/PhysRevB.73.195321.
[103] L. Ö. Olsson, C. B. M. Andersson, M. C. Håkansson, J. Kanski, L. Ilver, and U. O. Karlsson, ‘Charge Accumulation at InAs Surfaces’, *Phys. Rev. Lett.*, vol. 76, no. 19, pp. 3626–3629, May 1996, doi: 10.1103/PhysRevLett.76.3626.
[104] N. Tomaszewska, L. Walczak, J. Lis, and J. J. Kolodziej, ‘Surface states and charge accumulation states on reconstructed InAs (001) surfaces’, *Surf. Sci.*, vol. 632, pp. 103–110, 2015.
[105] K. Kajiyama, Y. Mizushima, and S. Sakata, ‘Schottky barrier height of n-InxGa1−xAs diodes’, *Appl. Phys. Lett.*, vol. 23, pp. 458–459, 1973.
[106] H. H. Wieder, ‘Transport coefficients of InAs epilayers’, *Appl. Phys. Lett.*, vol. 25, no. 4, pp. 206–208, Aug. 1974, doi: 10.1063/1.1655441.
[107] Ray-Ming Lin *et al.*, ‘Room temperature unpassivated InAs p-i-n photodetectors grown by molecular beam epitaxy’, *IEEE Trans. Electron Devices*, vol. 44, no. 2, pp. 209–213, Feb. 1997, doi: 10.1109/16.557708.
[108] R.-M. Lin, S.-F. Tang, and C. H. Kuan, ‘Study of current leakage in InAs p–i–n photodetectors’, *J. Vac. Sci. Technol. B Microelectron. Nanometer Struct.*, vol. 18, no. 6, p. 2624, 2000, doi: 10.1116/1.1319693.
[109] Y. Iwamura and N. Watanabe, ‘InAs Planar Diode Fabricated by Zn Diffusion’, *Jpn. J. Appl. Phys.*, vol. 39, no. Part 1, No. 10, pp. 5740–5745, Oct. 2000, doi: 10.1143/JJAP.39.5740.
[110] A. Säynätjoki *et al.*, ‘InAs pixel matrix detectors fabricated by diffusion of Zn in a metal-organic vapour-phase epitaxy reactor’, *Nucl. Instrum. Methods Phys. Res. Sect. Accel. Spectrometers Detect. Assoc. Equip.*, vol. 563, no. 1, pp. 24–26, Jul. 2006, doi: 10.1016/j.nima.2006.01.060.
[111] A. Sukach, V. Tetyorkin, G. Olijnuk, V. Lukyanenko, and A. Voroschenko, ‘Cooled InAs photodiodes for IR applications’, Warsaw, Poland, Sep. 2005, p. 59571A. doi: 10.1117/12.622195.
[112] V. V. Tetyorkin *et al.*, ‘p^+-InAsSbP/ n -InAs photodiodes for IR optoelectronic sensors’, Warsaw, Poland, Sep. 2005, p. 59570Z. doi: 10.1117/12.622181.
[113] V. V. Tetyorkin *et al.*, ‘Performance of InAs-based infrared photodiodes’, Prague, Czech Republic, May 2007, p. 658520. doi: 10.1117/12.723016.
[114] W. Dobbelaere *et al.*, ‘InAs p-n diodes grown on GaAs and GaAs-coated Si by molecular beam epitaxy’, *Appl. Phys. Lett.*, vol. 60, p. 868, 1992.
[115] W. Dobbelaere, W. De Raedt, J. De Boeck, R. Mertens, and G. orghs, ‘Monolithic integration of InAs photodiode and GaAs MESFET’, *Electron. Lett.*, vol. 28, no. 4, pp. 273–274, 1992.
[116] J.-W. Shi, F.-M. Kuo, and B.-R. Huang, ‘Zn-Diffusion InAs Photodiodes on a Semi-Insulating GaAs Substrate for High-Speed and Low Dark-Current

Performance', *IEEE Photonics Technol. Lett.*, vol. 23, no. 2, pp. 100–102, Jan. 2011, doi: 10.1109/LPT.2010.2091679.
[117] A. Krier and X. L. Huang, 'Design considerations for uncooled InAs mid-infrared light emitting diodes grown by liquid phase epitaxy', *J. Phys. Appl. Phys.*, vol. 39, no. 2, pp. 255–261, Jan. 2006, doi: 10.1088/0022-3727/39/2/004.
[118] S. Kalem, 'Molecular-beam epitaxial growth and transport properties of InAs epilayers', *J. Appl. Phys.*, vol. 66, pp. 3097–3103, 1989.
[119] S. K. Haywood, R. W. Martin, N. J. Mason, and P. J. Walker, 'Growth of InAs by MOVPE: A comparative study using arsine, tertiarybutylarsine and phenylarsine', *J. Cryst. Growth*, vol. 97, no. 2, pp. 489–496, Sep. 1989, doi: 10.1016/0022-0248(89)90231-5.
[120] A. R. J. Marshall, C. H. Tan, J. P. R. David, J. S. Ng, and M. Hopkinson, 'Fabrication of InAs photodiodes with reduced surface leakage current', Florence, Italy, Oct. 2007, p. 67400H. doi: 10.1117/12.740700.
[121] A. R. J. Marshall, C. H. Tan, J. S. Ng, J. P. R. David, and M. Hopkinson, 'Mid infrared avalanche photodiodes', in *EMRS DTC 3th Annual Conf. Proc. B*, 2006, vol. 11.
[122] A. R. J. Marshall, C. H. Tan, M. J. Steer, and J. P. R. David, 'Electron dominated impact ionization and avalanche gain characteristics in InAs photodiodes', *Appl. Phys. Lett.*, vol. 93, no. 11, p. 111107, Sep. 2008, doi: 10.1063/1.2980451.
[123] R. J. McIntyre, 'Multiplication noise in uniform avalanche diodes', *IEEE Trans. Electron Devices*, vol. 1, pp. 164–168, 1966.
[124] A. R. J. Marshall, Chee Hing Tan, M. J. Steer, and J. P. R. David, 'Extremely Low Excess Noise in InAs Electron Avalanche Photodiodes', *IEEE Photonics Technol. Lett.*, vol. 21, no. 13, pp. 866–868, Jul. 2009, doi: 10.1109/LPT.2009.2019625.
[125] J. D. Beck *et al.*, 'The HgCdTe electron avalanche photodiode', in *Proc. SPIE 5564*, Denver, CO, Oct. 2004, p. 44. doi: 10.1117/12.565142.
[126] K. F. Brennan and N. S. Mansour, 'Monte Carlo calculation of electron impact ionization in bulk InAs and HgCdTe', *J. Appl. Phys.*, vol. 69, no. 11, pp. 7844–7847, Jun. 1991, doi: 10.1063/1.347516.
[127] G. Satyanadh, R. P. Joshi, N. Abedin, and U. Singh, 'Monte Carlo calculation of electron drift characteristics and avalanche noise in bulk InAs', *J. Appl. Phys.*, vol. 91, no. 3, pp. 1331–1338, Feb. 2002, doi: 10.1063/1.1429771.
[128] A. R. J. Marshall, J. P. R. David, and C. H. Tan, 'Impact Ionization in InAs Electron Avalanche Photodiodes', *IEEE Trans. Electron Devices*, vol. 57, no. 10, pp. 2631–2638, Oct. 2010, doi: 10.1109/TED.2010.2058330.
[129] A. R. J. Marshall, P. Vines, P. J. Ker, J. P. R. David, and C. H. Tan, 'Avalanche Multiplication and Excess Noise in InAs Electron Avalanche Photodiodes at 77 K', *IEEE J. Quantum Electron.*, vol. 47, no. 6, pp. 858–864, Jun. 2011, doi: 10.1109/JQE.2011.2128299.
[130] R. B. Emmons, 'Avalanche-photodiode frequency response', *J. Appl. Phys.*, vol. 38, no. 9, pp. 3705–3714, 1967.
[131] A. R. J. Marshall, P. J. Ker, A. Krysa, J. P. R. David, and C. H. Tan, 'High speed InAs electron avalanche photodiodes overcome the conventional gain-bandwidth product limit', *Opt. Express*, vol. 19, no. 23, p. 23341, Nov. 2011, doi: 10.1364/OE.19.023341.

[132] S. Butera, P. Vines, C. H. Tan, I. Sandall, and G. S. Buller, 'Picosecond laser ranging at wavelengths up to 2.4 μm using an InAs avalanche photodiode', *Electron. Lett.*, vol. 52, no. 5, pp. 385–386, 2016.
[133] V. Shulyak, M. M. Hayat, and J. S. Ng, 'Sensitivity Calculations of High-Speed Optical Receivers Based on Electron-APDs', *J. Light. Technol.*, vol. 38, no. 4, pp. 989–995, Feb. 2020, doi: 10.1109/JLT.2019.2950804.
[134] G. P. Schwartz, J. E. Griffiths, and G. J. Gualtieri, 'Thermal oxidation and native oxide-substrate reactions on InAs and InxGa1− xAs', *Thin Solid Films*, vol. 94, no. 3, pp. 213–222, 1982.
[135] H. S. Kim *et al.*, 'Reduction of surface leakage current in InAs/GaSb strained layer long wavelength superlattice detectors using SU-8 passivation', *Appl. Phys. Lett.*, vol. 97, no. 14, p. 143512, Oct. 2010, doi: 10.1063/1.3499290.
[136] P. J. Ker, A. R. J. Marshall, C. H. Tan, and J. P. R. David, 'Surface passivation of InAs avalanche photodiodes for low-noise infrared imaging', *IEEE 6th Int. Conf. Photonics*, p. 3, 2016.
[137] P. J. Ker, A. R. J. Marshall, J. P. R. David, and C. H. Tan, 'Low noise high responsivity InAs electron avalanche photodiodes for infrared sensing', *Phys. Status Solidi C*, vol. 9, no. 2, pp. 310–313, Feb. 2012, doi: 10.1002/pssc.201100277.
[138] P. J. Ker, A. R. J. Marshall, A. B. Krysa, J. P. R. David, and C. H. Tan, 'Temperature Dependence of Leakage Current in InAs Avalanche Photodiodes', *IEEE J. Quantum Electron.*, vol. 47, no. 8, pp. 1123–1128, Aug. 2011, doi: 10.1109/JQE.2011.2159194.
[139] P. J. Ker, J. P. R. David, and C. H. Tan, 'Temperature dependence of gain and excess noise in InAs electron avalanche photodiodes', *Opt. Express*, vol. 20, no. 28, p. 29568, Dec. 2012, doi: 10.1364/OE.20.029568.
[140] I. C. Sandall, J. S. Ng, S. Xie, P. J. Ker, and C. H. Tan, 'Temperature dependence of impact ionization in InAs', *Opt. Express*, vol. 21, no. 7, p. 8630, Apr. 2013, doi: 10.1364/OE.21.008630.
[141] W. Sun *et al.*, 'High-Gain InAs Avalanche Photodiodes', *IEEE J. Quantum Electron.*, vol. 49, no. 2, pp. 154–161, Feb. 2013, doi: 10.1109/JQE.2012.2233462.
[142] S. J. Maddox, W. Sun, Z. Lu, H. P. Nair, J. C. Campbell, and S. R. Bank, 'Enhanced low-noise gain from InAs avalanche photodiodes with reduced dark current and background doping', *Appl. Phys. Lett.*, vol. 101, no. 15, p. 151124, Oct. 2012, doi: 10.1063/1.4757424.
[143] I. C. Sandall, S. Zhang, and C. H. Tan, 'Linear array of InAs APDs operating at 2 μm', *Opt. Express*, vol. 21, no. 22, p. 25780, Nov. 2013, doi: 10.1364/OE.21.025780.
[144] X. Zhou, X. Meng, A. B. Krysa, J. R. Wilmott, J. S. Ng, and C. H. Tan, 'InAs Photodiodes for 3.43 μm Radiation Thermometry', *IEEE Sens. J.*, vol. 15, no. 10, p. 5555, 2015.
[145] R. B. Gomes, C. H. Tan, P. J. Ker, J. P. R. David, and J. S. Ng, 'InAs avalanche photodiodes for X-ray detection', *J. Instrum.*, vol. 6, no. 12, pp. P12005–P12005, Dec. 2011, doi: 10.1088/1748-0221/6/12/P12005.
[146] B. S. White, I. C. Sandall, J. P. R. David, and Chee Hing Tan, 'InAs Diodes Fabricated Using Be Ion Implantation', *IEEE Trans. Electron Devices*, vol. 62, no. 9, pp. 2928–2932, Sep. 2015, doi: 10.1109/TED.2015.2456434.

[147] B. S. White *et al.*, 'High-Gain InAs Planar Avalanche Photodiodes', *J. Light. Technol.*, vol. 34, no. 11, pp. 2639–2644, Jun. 2016, doi: 10.1109/JLT.2016.2531278.
[148] H. Okamoto and K. Oe, 'Growth of metastable alloy InAsBi by low-pressure MOVPE', *Jpn. J. Appl. Phys.*, vol. 37, no. 3S, p. 1608, 1998.
[149] Z. M. Fang, K. Y. Ma, D. H. Jaw, R. M. Cohen, and G. B. Stringfellow, 'Photoluminescence of InSb, InAs, and InAsSb grown by organometallic vapor phase epitaxy', *J. Appl. Phys.*, vol. 67, no. 11, pp. 7034–7039, Jun. 1990, doi: 10.1063/1.345050.
[150] S. P. Svensson, H. Hier, W. L. Sarney, D. Donetsky, D. Wang, and G. Belenky, 'Molecular beam epitaxy control and photoluminescence properties of InAsBi', *J. Vac. Sci. Technol. B Nanotechnol. Microelectron. Mater. Process. Meas. Phenom.*, vol. 30, no. 2, p. 02B109, Mar. 2012, doi: 10.1116/1.3672023.
[151] I. C. Sandall *et al.*, 'Demonstration of InAsBi photoresponse beyond 3.5 μ m', *Appl. Phys. Lett.*, vol. 104, no. 17, p. 171109, 2014.
[152] W. D. Lawson, S. Nielsen, E. H. Putley, and A. S. Young, 'Preparation and properties of HgTe and mixed crystals of HgTe-CdTe', *J. Phys. Chem. Solids*, vol. 9, no. 3–4, pp. 325–329, 1959.
[153] P. Thorne, J. Gordon, L. G. Hipwood, and A. Bradford, '16 megapixel 12um array developments at Selex ES', in *Infrared Technology and Applications XXXIX*, 2013, vol. 8704, p. 87042M.
[154] R. Breiter, H. Figgemeier, H. Lutz, J. Wendler, S. Rutzinger, and T. Schallenberg, 'Improved MCT LWIR modules for demanding imaging applications', Baltimore, Maryland, United States, Jun. 2015, p. 945128. doi: 10.1117/12.2178538.
[155] K. Vural *et al.*, '2048x2048 HgCdTe focal plane arrays for astronomy applications', Orlando, FL, Jul. 1999, p. 24. doi: 10.1117/12.354532.
[156] S. Hanna *et al.*, 'Low dark current LWIR and VLWIR HgCdTe focal plane arrays at AIM', Edinburgh, United Kingdom, Oct. 2016, p. 100000P. doi: 10.1117/12.2244514.
[157] Y. Reibel *et al.*, 'Update on 10μm pixel pitch MCT-based focal plane array with enhanced functionalities', in *Infrared Technology and Applications XLI*, 2015, vol. 9451, p. 94512E.
[158] A. Rogalski, 'HgCdTe infrared detector material: history, status and outlook', *Rep. Prog. Phys.*, vol. 68, no. 10, pp. 2267–2336, Oct. 2005, doi: 10.1088/0034-4885/68/10/R01.
[159] A. Rogalski, 'Recent progress in third generation infrared detectors', *J. Mod. Opt.*, vol. 57, no. 18, pp. 1716–1730, Oct. 2010, doi: 10.1080/09500340.2010.486485.
[160] P. Norton, 'HgCdTe infrared detectors', vol. 3, p. 16, 2002.
[161] R. K. Bhan and V. Dhar, 'Recent infrared detector technologies, applications, trends and development of HgCdTe based cooled infrared focal plane arrays and their characterization', *Opto-Electron. Rev.*, vol. 27, no. 2, pp. 174–193, Jun. 2019, doi: 10.1016/j.opelre.2019.04.004.
[162] C. Verie, F. Raymond, J. Besson, and T. Nguyen Duy, 'Bandgap spin-orbit splitting resonance effects in Hg1-xCdxTe alloys', *J. Cryst. Growth*, vol. 59, no. 1–2, pp. 342–346, 1982.
[163] G. Lecoy, B. Orsal, and R. Alabedra, 'Impact ionization resonance and auger recombination in Hg 1-x Cd x Te (0.6≤ x≤ 0.7)', *IEEE J. Quantum Electron.*, vol. 23, no. 7, pp. 1145–1154, 1987.

[164] B. Orsal, R. Alabedra, M. Valenza, G. Pichard, and J. Meslage, 'Impact ionization rates for electrons and holes in Hg0. 3Cd0. 7Te in avalanche photodiodes for optical fiber transmission systems at λ= 1.3 μm', *J. Cryst. Growth*, vol. 72, no. 1–2, pp. 496–503, 1985.
[165] T. Duy Nguyen, J. Meslage, and G. Pichard, 'CMT: the material for fiber optical communication devices', *J. Cryst. Growth*, vol. 72, no. 1–2, pp. 490–495, 1985.
[166] T. J. de Lyon *et al.*, 'Epitaxial growth of HgCdTe 1.55-um avalanche photodiodes by molecular beam epitaxy', in *Proc. Vol. 3629*, San Jose, CA, 1999, vol. 3629.
[167] G. Leveque, M. Nasser, D. Bertho, B. Orsal, and R. Alabedra, 'Ionization energies in Cd $_{x}$ Hg $_{1-x}$ Te avalanche photodiodes', *Semicond. Sci. Technol.*, vol. 8, no. 7, pp. 1317–1323, Jul. 1993, doi: 10.1088/0268-1242/8/7/021.
[168] C. T. Elliott, N. T. Gordon, R. S. Hall, and G. Crimes, 'Reverse breakdown in long wavelength lateral collection Cd x Hg1− x Te diodes', *J. Vac. Sci. Technol. Vaccum Surf. Films*, vol. 8, no. 2, pp. 1251–1253, 1990.
[169] J. D. Beck, C.-F. Wan, M. A. Kinch, and J. E. Robinson, 'MWIR HgCdTe avalanche photodiodes', San Diego, CA, USA, Nov. 2001, p. 188. doi: 10.1117/12.448174.
[170] J. Beck *et al.*, 'The HgCdTe Electron Avalanche Photodiode', *J. Electron. Mater.*, vol. 35, no. 6, p. 8, 2006.
[171] P. D. LeVan *et al.*, 'HDVIP for low-background-flux and high-operating-temperature applications', Denver, CO, Oct. 2004, p. 1. doi: 10.1117/12.566370.
[172] M. Vaidyanathan *et al.*, 'High performance ladar focal plane arrays for 3D range imaging', in *2004 IEEE Aerospace Conference Proceedings (IEEE Cat. No.04TH8720)*, Big Sky, MT, USA, 2004, pp. 1776–1781. doi: 10.1109/AERO.2004.1367957.
[173] M. B. Reine *et al.*, 'HgCdTe MWIR Back-Illuminated Electron-Initiated Avalanche Photodiode Arrays', *J. Electron. Mater.*, vol. 36, no. 8, pp. 1059–1067, Aug. 2007, doi: 10.1007/s11664-007-0172-y.
[174] M. B. Reine *et al.*, 'Characterization of HgCdTe MWIR Back-Illuminated Electron-Initiated Avalanche Photodiodes', *J. Electron. Mater.*, vol. 37, no. 9, pp. 1376–1386, Sep. 2008, doi: 10.1007/s11664-008-0420-9.
[175] G. Perrais *et al.*, 'Study of the Transit-Time Limitations of the Impulse Response in Mid-Wave Infrared HgCdTe Avalanche Photodiodes', *J. Electron. Mater.*, vol. 38, no. 8, pp. 1790–1799, Aug. 2009, doi: 10.1007/s11664-009-0802-7.
[176] M. A. Kinch, J. D. Beck, C.-F. Wan, F. Ma, and J. Campbell, 'HgCdTe electron avalanche photodiodes', *J. Electron. Mater.*, vol. 33, no. 6, pp. 630–639, Jun. 2004, doi: 10.1007/s11664-004-0058-1.
[177] F. Ma, X. Li, J. C. Campbell, J. D. Beck, C.-F. Wan, and M. A. Kinch, 'Monte Carlo simulations of Hg0.7Cd0.3Te avalanche photodiodes and resonance phenomenon in the multiplication noise', *Appl. Phys. Lett.*, vol. 83, p. 4, 2003.
[178] M. A. Kinch, 'A Theoretical Model for the HgCdTe Electron Avalanche Photodiode', *J. Electron. Mater.*, vol. 37, no. 9, pp. 1453–1459, Sep. 2008, doi: 10.1007/s11664-008-0439-y.
[179] J. Rothman, L. Mollard, S. Goût, L. Bonnefond, and J. Wlassow, 'History-Dependent Impact Ionization Theory Applied to HgCdTe e-APDs', *J. Electron. Mater.*, vol. 40, no. 8, pp. 1757–1768, Aug. 2011, doi: 10.1007/s11664-011-1679-9.

[180] J. Rothman *et al.*, 'Short-Wave Infrared HgCdTe Avalanche Photodiodes', *J. Electron. Mater.*, vol. 41, no. 10, pp. 2928–2936, Oct. 2012, doi: 10.1007/s11664-012-1970-4.
[181] E. D. De Borniol, J. Rothman, F. Guellec, G. Vojetta, G. Destéfanis, and O. Pacaud, 'Active three-dimensional and thermal imaging with a 30-μm pitch 320× 256 HgCdTe avalanche photodiode focal plane array', *Opt. Eng.*, vol. 51, no. 6, p. 061305, 2012.
[182] R. Breiter *et al.*, 'MCT SWIR modules for active imaging', in *Infrared Technology and Applications XLV*, Baltimore, United States, May 2019, p. 38. doi: 10.1117/12.2519891.
[183] J. Beck, T. Welch, P. Mitra, K. Reiff, X. Sun, and J. Abshire, 'A highly sensitive multi-element HgCdTe e-APD detector for IPDA lidar applications', *J. Electron. Mater.*, vol. 43, no. 8, pp. 2970–2977, 2014.
[184] A. Dumas *et al.*, 'Evaluation of a HgCdTe e-APD based detector for 2 μm CO_2 DIAL application', *Appl. Opt.*, vol. 56, no. 27, p. 7577, Sep. 2017, doi: 10.1364/AO.56.007577.
[185] T. F. Refaat, U. N. Singh, M. Petros, and R. Remus, 'MCT Avalanche Photodiode Detector FOR Two-MICRON Active Remote Sensing Applications', in *IGARSS 2018 - 2018 IEEE International Geoscience and Remote Sensing Symposium*, Valencia, Jul. 2018, pp. 1865–1868. doi: 10.1109/IGARSS.2018.8518933.
[186] W. Sullivan *et al.*, 'Linear-Mode HgCdTe Avalanche Photodiodes for Photon-Counting Applications', *J. Electron. Mater.*, vol. 44, no. 9, pp. 3092–3101, Sep. 2015, doi: 10.1007/s11664-015-3824-3.
[187] I. M. Baker *et al.*, 'Linear-mode avalanche photodiode arrays in HgCdTe at Leonardo, UK: the current status', in *Image Sensing Technologies: Materials, Devices, Systems, and Applications VI*, Baltimore, United States, May 2019, p. 20. doi: 10.1117/12.2519830.
[188] D. E. Atkinson, D. N. B. Hall, S. M. Jacobson, I. M. Baker, and S. B. Goebel, 'Observatory deployment and characterization of SAPHIRA HgCdTe APD arrays', in *High Energy, Optical, and Infrared Detectors for Astronomy VIII*, Austin, United States, Jul. 2018, p. 54. doi: 10.1117/12.2311814.
[189] G. Vojetta, F. Guellec, L. Mathieu, K. Foubert, P. Feautrier, and J. Rothman, 'Linear photon-counting with HgCdTe APDs', Baltimore, Maryland, May 2012, pp. 83750Y-83750Y–18. doi: 10.1117/12.921869.
[190] E. Smith, 'Two Revolutionary Optical Technologies', *AAPPS Bull.*, vol. 19, no. 6, p. 11, 2009.
[191] F. R. Bacher and J. S. Blakemore, 'Optical-absorption coefficient of In 1− x Ga x As/InP', *Phys. Rev. B*, vol. 37, no. 5, p. 2551, 1988.
[192] S. R. Forrest, R. F. Leheny, R. E. Nahory, and M. A. Pollack, 'In0. 53Ga0. 47As photodiodes with dark current limited by generation-recombination and tunneling', *Appl. Phys. Lett.*, vol. 37, no. 3, pp. 322–325, 1980.
[193] K. Nishida, K. Taguchi, and Y. Matsumoto, 'InGaAsP heterostructure avalanche photodiodes with high avalanche gain', *Appl. Phys. Lett.*, vol. 35, no. 3, pp. 251–253, Aug. 1979, doi: 10.1063/1.91089.
[194] O. K. Kim, S. R. Forrest, W. A. Bonner, and R. G. Smith, 'A high gain $In_{0.53}Ga_{0.47}As$/InP avalanche photodiode with no tunneling leakage current', *Appl. Phys. Lett.*, vol. 39, no. 5, pp. 402–404, Sep. 1981, doi: 10.1063/1.92752.
[195] J. C. Campbell, A. G. Dentai, W. S. Holden, and B. L. Kasper, 'High-performance avalanche photodiode with separate absorption "grading" and

multiplication regions', *Electron. Lett.*, vol. 19, no. 20, p. 818, 1983, doi: 10.1049/el:19830558.
[196] H. Kuwatsuka, Y. Kito, T. Uchida, and T. Mikawa, 'High-speed InP/InGaAs avalanche photodiodes with a compositionally graded quaternary layer', *IEEE Photonics Technol. Lett.*, vol. 3, no. 12, pp. 1113–1114, Dec. 1991, doi: 10.1109/68.118019.
[197] L. E. Tarof, J. Yu, R. Bruce, D. G. Knight, T. Baird, and B. Oosterbrink, 'High-frequency performance of separate absorption grading, charge, and multiplication InP/InGaAs avalanche photodiodes', *IEEE Photonics Technol. Lett.*, vol. 5, no. 6, pp. 672–674, Jun. 1993, doi: 10.1109/68.219706.
[198] K. F. Li *et al.*, 'Low Avalanche Noise Characteristics in Thin InP p -i-n Diodes with Electron Initiated Multiplication', *IEEE PHOTONICS Technol. Lett.*, vol. 11, no. 3, p. 3, 1999.
[199] Y. L. Goh *et al.*, 'Excess Avalanche Noise in $\hbox{In}_{0.52}\hbox{Al}_{0.48}\hbox{As}$', *IEEE J. Quantum Electron.*, vol. 43, no. 6, pp. 503–507, Jun. 2007, doi: 10.1109/JQE.2007.897900.
[200] L. J. J. Tan, J. S. Ng, C. H. Tan, and J. P. R. David, 'Avalanche Noise Characteristics in Submicron InP Diodes', *IEEE J. Quantum Electron.*, vol. 44, no. 4, pp. 378–382, Apr. 2008, doi: 10.1109/JQE.2007.914771.
[201] L. J. J. Tan *et al.*, 'Temperature Dependence of Avalanche Breakdown in InP and InAlAs', *IEEE J. Quantum Electron.*, vol. 46, no. 8, pp. 1153–1157, Aug. 2010, doi: 10.1109/JQE.2010.2044370.
[202] E. Yagyu, E. Ishimura, M. Nakaji, T. Aoyagi, and Y. Tokuda, 'Simple planar structure for high-performance AlInAs avalanche photodiodes', *IEEE Photonics Technol. Lett.*, vol. 18, no. 1, pp. 76–78, Jan. 2006, doi: 10.1109/LPT.2005.860399.
[203] L. E. Tarof, 'Planar InP-InGaAs avalanche photodetectors with n-multiplication layer exhibiting a very high gain-bandwidth product', *IEEE Photonics Technol. Lett.*, vol. 2, no. 9, pp. 643–646, 1990.
[204] F. Nakajima, M. Nada, and T. Yoshimatsu, 'High-Speed Avalanche Photodiode and High-Sensitivity Receiver Optical Subassembly for 100-Gb/s Ethernet', *J. Light. Technol.*, vol. 34, no. 2, pp. 243–248, Jan. 2016, doi: 10.1109/JLT.2015.2464710.
[205] Shiyu Xie and Chee Hing Tan, 'AlAsSb Avalanche Photodiodes With a Sub-mV/K Temperature Coefficient of Breakdown Voltage', *IEEE J. Quantum Electron.*, vol. 47, no. 11, pp. 1391–1395, Nov. 2011, doi: 10.1109/JQE.2011.2165051.
[206] J. Xie, S. Xie, R. C. Tozer, and C. H. Tan, 'Excess Noise Characteristics of Thin AlAsSb APDs', *IEEE Trans. Electron Devices*, vol. 59, no. 5, pp. 1475–1479, May 2012, doi: 10.1109/TED.2012.2187211.
[207] X. Zhou, S. Zhang, J. P. R. David, J. S. Ng, and C. H. Tan, 'Avalanche Breakdown Characteristics of $Al_{1-x}Ga_xAs_{0.56}Sb_{0.44}$ Quaternary Alloys', *IEEE Photonics Technol. Lett.*, vol. 28, no. 22, pp. 2495–2498, Nov. 2016, doi: 10.1109/LPT.2016.2601651.
[208] X. Zhou, L. L. G. Pinel, S. J. Dimler, S. Zhang, J. S. Ng, and C. H. Tan, 'Thin Al1−xGaxAs0.56Sb0.44 Diodes With Low Excess Noise', *IEEE J. Sel. Top. QUANTUM Electron.*, vol. 24, no. 2, p. 5, 2018.
[209] L. L. G. Pinel *et al.*, 'Effects of carrier injection profile on low noise thin $Al_{085}Ga_{015}As_{056}Sb_{044}$ avalanche photodiodes', *Opt. Express*, vol. 26, no. 3, p. 3568, Feb. 2018, doi: 10.1364/OE.26.003568.

[210] S. Xie *et al.*, ‘InGaAs/AlGaAsSb avalanche photodiode with high gain-bandwidth product’, *Opt. Express*, vol. 24, no. 21, p. 24242, Oct. 2016, doi: 10.1364/OE.24.024242.
[211] X. Yi *et al.*, ‘Demonstration of large ionization coefficient ratio in AlAs0.56Sb0.44 lattice matched to InP’, *Sci. Rep.*, vol. 8, no. 1, p. 9107, Dec. 2018, doi: 10.1038/s41598-018-27507-w.
[212] X. Yi *et al.*, ‘Extremely low excess noise and high sensitivity AlAs0.56Sb0.44 avalanche photodiodes’, *Nat. Photonics*, vol. 13, no. 10, pp. 683–686, Oct. 2019, doi: 10.1038/s41566-019-0477-4.
[213] X. Ji *et al.*, ‘Deep-level traps induced dark currents in extended wavelength InxGa1− xAs/InP photodetector’, *Appl. Phys.*, vol. 114, no. 22, p. 224502, 2013.
[214] R. Sidhu, Ning Duan, J. C. Campbell, and A. L. Holmes, ‘A long-wavelength photodiode on InP using lattice-matched GaInAs-GaAsSb type-II quantum wells’, *IEEE Photonics Technol. Lett.*, vol. 17, no. 12, pp. 2715–2717, Dec. 2005, doi: 10.1109/LPT.2005.859163.
[215] R. Sidhu, L. Zhang, N. Tan, N. Duan, J. C. Campbell, and A. L. Holmes, ‘2.4 μm cutoff wavelength avalanche photodiode on InP substrate’, *Electron. Lett.*, vol. 42, no. 3, p. 2, 2006.
[216] D. S. G. Ong, J. S. Ng, Y. L. Goh, C. H. Tan, S. Zhang, and J. P. R. David, ‘InAlAs Avalanche Photodiode With Type-II Superlattice Absorber for Detection Beyond 2 $\mu\hbox{m}$’, *IEEE Trans. Electron Devices*, vol. 58, no. 2, pp. 486–489, Feb. 2011, doi: 10.1109/TED.2010.2090352.
[217] J. P. Petropoulos, Y. Zhong, and J. M. O. Zide, ‘Optical and electrical characterization of InGaBiAs for use as a mid-infrared optoelectronic material’, *Appl. Phys. Lett.*, vol. 99, no. 3, p. 031110, Jul. 2011, doi: 10.1063/1.3614476.
[218] X. Y. Chen *et al.*, ‘Characteristics of InGaAsBi with various lattice mismatches on InP substrate’, *AIP Adv.*, vol. 6, no. 7, p. 075215, Jul. 2016, doi: 10.1063/1.4959896.
[219] Y. Gu *et al.*, ‘Nearly lattice-matched short-wave infrared InGaAsBi detectors on InP’, *Appl. Phys. Lett.*, vol. 108, no. 3, p. 032102, Jan. 2016, doi: 10.1063/1.4940201.
[220] B. Du *et al.*, ‘Wavelength Extended InGaAsBi Detectors with Temperature-Insensitive Cutoff Wavelength’, *Chin. Phys. Lett.*, vol. 35, no. 7, p. 078501, Jul. 2018, doi: 10.1088/0256-307X/35/7/078501.
[221] W. N. Grant, ‘Electron and hole ionization rates in epitaxial silicon at high electric fields’, *Solid-State Electron.*, vol. 16, no. 10, pp. 1189–1203, 1973.
[222] H. W. Ruegg, ‘An optimized avalanche photodiode’, *IEEE Trans. Electron Devices*, vol. 14, no. 5, pp. 239–251, May 1967, doi: 10.1109/T-ED.1967.15937.
[223] H. Melchior, A. R. Hartman, D. P. Schinke, and T. E. Seidel, ‘Atlanta Fiber System Experiment: Planar Epitaxial Silicon Avalanche Photodiode’, *Bell Syst. Tech. J.*, vol. 57, no. 6, pp. 1791–1807, Jul. 1978, doi: 10.1002/j.1538-7305.1978.tb02127.x.
[224] Y. Kang *et al.*, ‘Epitaxially-grown Ge/Si avalanche photodiodes for 1.3 μm light detection’, *Opt. Express*, vol. 16, no. 13, p. 9365, Jun. 2008, doi: 10.1364/OE.16.009365.
[225] Y. Kang *et al.*, ‘Monolithic germanium/silicon avalanche photodiodes with 340 GHz gain–bandwidth product’, *Nat. Photonics*, vol. 3, no. 1, pp. 59–63, Jan. 2009, doi: 10.1038/nphoton.2008.247.
[226] Y. Kang *et al.*, ‘High Performance Ge/Si Avalanche Photodiodes Development in Intel’, in *Optical Fiber Communication Conference/National Fiber Optic*

Engineers Conference 2011, Los Angeles, California, 2011, p. OWZ1. doi: 10.1364/OFC.2011.OWZ1.

[227] Daoxin Dai, M. Piels, and J. E. Bowers, 'Monolithic Germanium/Silicon Photodetectors With Decoupled Structures: Resonant APDs and UTC Photodiodes', *IEEE J. Sel. Top. Quantum Electron.*, vol. 20, no. 6, pp. 43–56, Nov. 2014, doi: 10.1109/JSTQE.2014.2322443.

[228] Z. Huang *et al.*, '25 Gbps low-voltage waveguide Si–Ge avalanche photodiode', *Optica*, vol. 3, no. 8, p. 793, Aug. 2016, doi: 10.1364/OPTICA.3.000793.

[229] H.-C. Luan *et al.*, 'High-quality Ge epilayers on Si with low threading-dislocation densities', *Appl. Phys. Lett.*, vol. 75, no. 19, pp. 2909–2911, Nov. 1999, doi: 10.1063/1.125187.

[230] A. M. Hoang, G. Chen, A. Haddadi, S. Abdollahi Pour, and M. Razeghi, 'Demonstration of shortwavelength infrared photodiodes based on type-II InAs/GaSb/AlSb superlattices', *Appl. Phys. Lett.*, vol. 100, no. 21, p. 211101, May 2012, doi: 10.1063/1.4720094.

[231] R. Q. Yang *et al.*, 'High power mid-infrared interband cascade lasers based on type-II quantum wells', *Appl. Phys. Lett.*, vol. 71, no. 17, pp. 2409–2411, Oct. 1997, doi: 10.1063/1.120076.

[232] S. J. Maddox, S. D. March, and S. R. Bank, 'Broadly Tunable AlInAsSb Digital Alloys Grown on GaSb', *Cryst. Growth Des.*, vol. 16, no. 7, pp. 3582–3586, Jul. 2016, doi: 10.1021/acs.cgd.5b01515.

[233] M. E. Woodson, M. Ren, S. J. Maddox, Y. Chen, S. R. Bank, and J. C. Campbell, 'Low-noise AlInAsSb avalanche photodiode', *Appl. Phys. Lett.*, vol. 108, no. 8, p. 081102, Feb. 2016, doi: 10.1063/1.4942372.

[234] M. Ren, S. J. Maddox, M. E. Woodson, Y. Chen, S. R. Bank, and J. C. Campbell, 'AlInAsSb separate absorption, charge, and multiplication avalanche photodiodes', *Appl. Phys. Lett.*, vol. 108, no. 19, p. 191108, May 2016, doi: 10.1063/1.4949335.

[235] S. R. Bank *et al.*, 'Avalanche Photodiodes Based on the AlInAsSb Materials System', *IEEE J. Sel. Top. Quantum Electron.*, vol. 24, no. 2, pp. 1–7, Mar. 2018, doi: 10.1109/JSTQE.2017.2737880.

[236] A. P. Craig *et al.*, 'Extended short-wave infrared linear and Geiger mode avalanche photodiodes, based on 6.1 Å materials', *Appl. Phys. Lett.*, vol. 114, no. 5, p. 053501, Feb. 2019, doi: 10.1063/1.5054753.

[237] L. W. Lim, C. H. Tan, J. S. Ng, J. D. Petticrew, and A. B. Krysa, 'Improved Planar InAs Avalanche Photodiodes With Reduced Dark Current and Increased Responsivity', *J. Light. Technol.*, vol. 37, no. 10, pp. 2375–2379, May 2019, doi: 10.1109/JLT.2019.2905535.

Chapter 2 Background Information

2.1 Impact ionisation and avalanche gain

Avalanche multiplication, or avalanche gain, in APDs is enabled by the impact ionisation process where a carrier, be it an electron or a hole, upon attaining sufficiently high energy under the effects of an electric field can create new electron-hole pairs (EHP). The primary (original) and secondary (new) carriers continue travelling within the electric field, causing successive events of impact ionisation that increase the total number of carriers than initially present in the multiplication region, thus providing amplification to the initial signal.

An electron-initiated impact ionisation involving a single transition from the valence to the conduction band is depicted in the form of an E-k diagram in Fig. 2.1. The primary carrier, e_1, loses a minimum amount of energy that must be greater than E_g for impact ionisation to occur, which is known as the electron threshold energy, $E_{th(e)}$. The energy is transferred to an electron in the valence band which promotes it to the conduction band, becoming e_2 and leaving behind a hole, h_1. The transitions are symmetrical as energy and momentum are conserved during the impact ionisation process. This simplified depiction of impact ionisation is applicable only for transitions between the gamma valley and heavy hole band such as in InAs and HgCdTe due to the large intervalley separation energies. In most other APD materials, the overall impact ionisation process is more complicated, involving transitions from different energy bands while conserving energy and momentum.

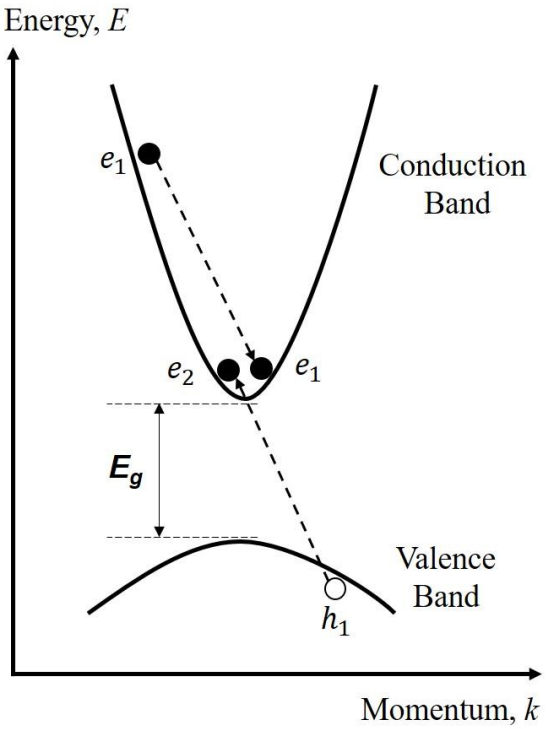

Figure 2.1 E-k diagram of an impact ionisation initiated by an electron

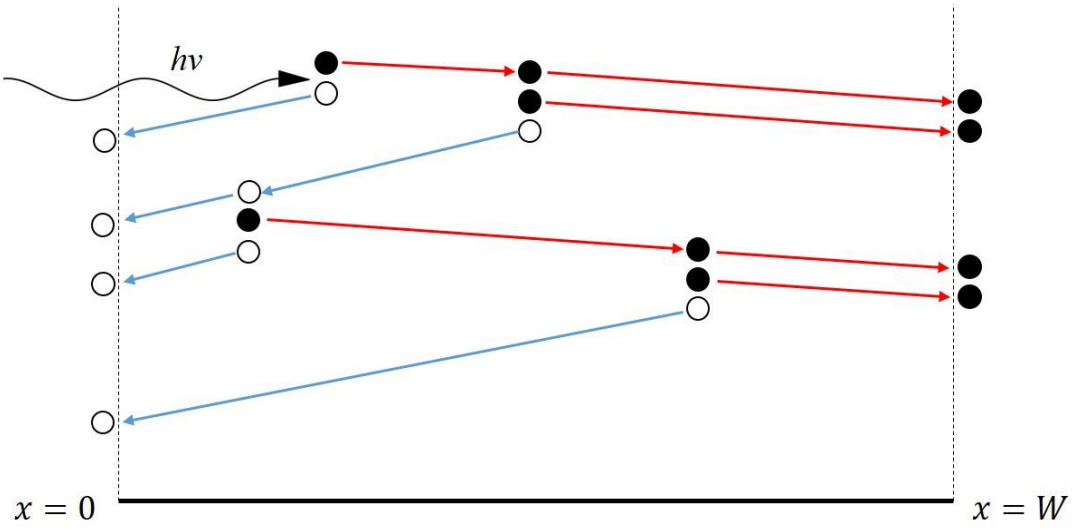

Figure 2.2 Schematic diagram of a chain of impact ionisation events with initial carriers generated via absorption of a photon

With reference to Fig. 2.2 above, consider an electron and hole pair at an injected position of x (through means such as carrier generation from the absorption of a photon with energy $hv \geq E_g$) in a high electric field multiplication region with a width of W. Under the influence of electric field, the electron will travel to the right and produce αdx number of ionising collisions while the hole travelling to the left will create βdx

ionisation events within a distance *dx*. α and β are the electron and hole ionisation coefficients respectively, that is defined as the number of secondary carrier pairs generated within a unit length travelled at a given electric field. The reciprocal of the ionisation coefficients gives the mean ionising path length travelled between each ionisation event. The secondary EHPs traverse in a similar fashion within the electric field and contribute to additional cascading events of impact ionisation that gives rise to an average total number of electrons and holes, *M(x)*, that is given by the following equation [1].

$$M(x) = \frac{\exp\left[-\int_x^w (\alpha - \beta) dx'\right]}{1 - \int_0^w \alpha \exp\left[-\int_{x'}^w (\alpha - \beta) dx''\right] dx'} \tag{2.1}$$

From equation 2.1, it can be seen that avalanche gain is sensitive to the injection position or profile of the initial carrier. For the case of a uniform electric field (such as in a p-i-n diode with sufficiently low background doping concentration in the i-layer), *M(x)* can be further simplified to *M(0)* and *M(w)* for pure electron and pure hole injection scenario respectively as below.

$$M(0) = M_e = \frac{1}{1 - \frac{\alpha}{\alpha - \beta}\{\exp[(\beta - \alpha)w] - 1\}} \tag{2.2}$$

$$M(w) = M_h = \frac{1}{1 - \frac{\beta}{\beta - \alpha}\{\exp[(\alpha - \beta)w] - 1\}} \tag{2.3}$$

For materials with $\alpha > \beta$, the largest gain can be obtained under a pure electron injection condition, for example by absorbing >99% of incident photons in the p-region in a p-i-n design APD, and vice versa for materials with $\beta > \alpha$. Consider two unique scenarios of one, $\alpha = \beta$ and the second where $\beta = 0$. In the former scenario, electrons and holes have equal probability of ionisation such that successive ionisation events can be triggered by either carrier. Failure to initiate impact ionisation by some carriers causes large fluctuations in gain. However, the avalanche process seeded by both electrons and holes produces a sharp breakdown characteristic. In this case, gain is given by

$$M = \frac{1}{1 - \alpha W} \tag{2.4}$$

Hence, avalanche breakdown will occur when $\alpha W = 1$ which can be understood as the rate of carrier generation is faster than the rate where carriers are leaving the high field region. For the latter scenario, the gain is given by

$$M = \exp(\alpha W) \tag{2.5}$$

In the case where holes are assumed to be incapable of triggering impact ionisation, the chain of impact ionisation events is built up by electrons as these electrons travel to the right of the electric field. The avalanche gain in such a material can therefore be optimised, either by increasing the electric field which affects the electron ionisation coefficient, or by increasing the multiplication region width. The SCM property also implies that the avalanche build-up time is limited to the sum of the transit times of electron and hole of the material for all generated carriers to exit the electric field. This is illustrated in Fig. 2.3 with more clarity. The bandwidth is therefore transit time limited, ignoring the effects of gain as Emmons predicted [2]. As such, the gain-bandwidth product of APDs with SCM is, in principle, infinite. Without feedback of carriers from impact ionisation due to holes, the classical avalanche breakdown mechanism becomes invalid and SCM APDs usually show soft breakdown characteristics due to the weak increase of α with voltage.

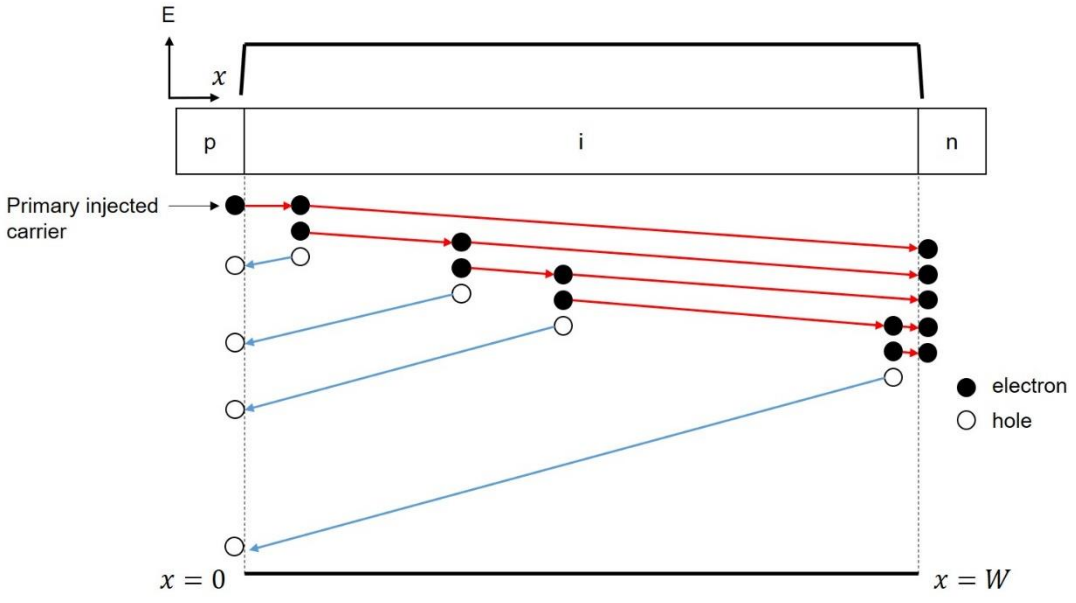

Figure 2.3 An impact ionisation chain with pure electron injection and β = 0

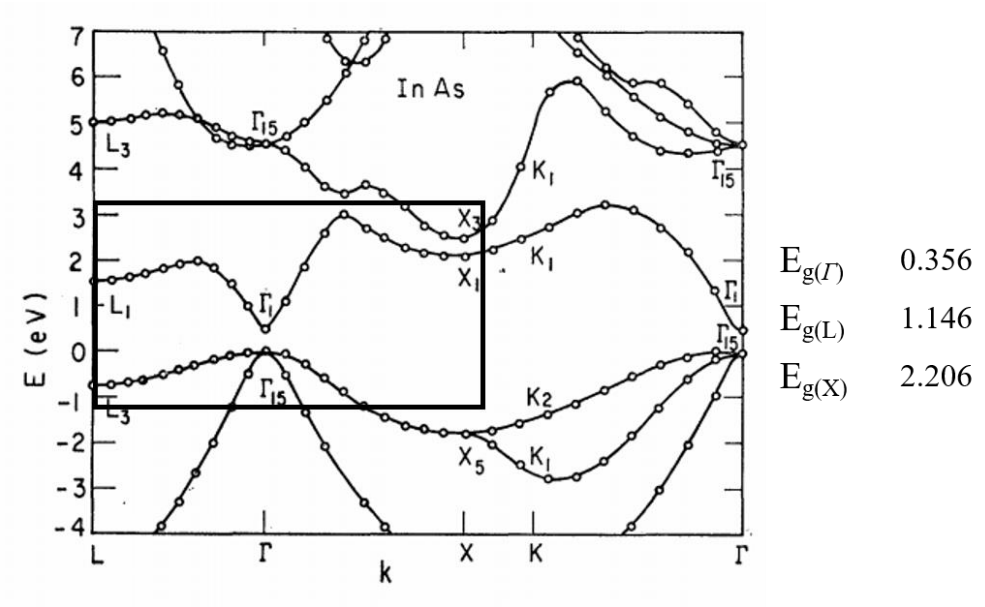

Figure 2.4 The band structure of InAs [3] and valley separation energy with respect to the valence band maxima obtained from [4]

The single carrier multiplication properties of InAs can be qualitatively explained using the band structure diagrams in Fig. 2.4. Due to the narrow band gap of InAs, impact ionisation in InAs can occur at relatively low threshold energy (as compared to other III-V materials). Using the Anderson and Crowell approximation [5], the electron threshold energy is approximately equal to the band gap due to the disparate electron and hole effective mass [6]. Furthermore, electrons with sufficient energy for impact ionisation are confined in the Γ valley due to the large intervalley separation energy in InAs where the phonon scattering effects are weak [7]. Comparatively, a flat heavy hole band (relative to the Γ valley) requires phonons interaction for holes to gain energy and the large hole effective mass hinders the rate of energy gain from an applied electric field. It was suggested that the factors for impact ionisation are much more favourable for electrons than for holes, thus creating a false illusion of suppressed hole ionisation; it is perhaps more accurate to say that the hole ionisation can occur but only at high electric fields where the tunnelling current will manifest in such a narrow band gap material and is therefore irrelevant in the electric fields considered [8]. Detailed theoretical modelling invoking the electron-scattering interactions and electron and hole densities of state is used to explain the electron ionisation properties seen in MCT e-APDs [9].

2.2 Avalanche excess noise

The avalanche process is stochastic in nature as the position where impact ionisation occurs and the total number of carriers produced per injected primary carrier are random. This inherent fluctuation around the mean avalanche gain gives rise to an avalanche excess noise, *F(M)*, that can be expressed as the following equation.

$$F(M) = \frac{< G^2 >}{< G >^2} \tag{2.6}$$

where $< G >$ is the mean avalanche gain, and $< G^2 >$ is the mean square.

McIntyre further derived in a general expression relating excess noise to the ionisation coefficients as in equation 2.7 and concluded that to achieve avalanche process with low excess noise, the carrier type with greater ionising capability should be injected into the high field region [10].

$$F(M) = kM + (2 - \frac{1}{M})(1 - k) \tag{2.7}$$

where $k = \beta/\alpha$ for pure electron injection. It is obvious then to obtain a low *F*, there should be large disparity between α and β and that, for a material with $k = 0$, the excess noise reaches a minimum value of 2.

One advantage of using an APD over standard photodiodes is the ability to improve the *SNR* in a receiver system by avalanche gain, provided that the excess noise is not disproportionately large. The shot noise, i_n^2, in an APD is given by

$$i_n^2 = 2qFM^2(I_d + I_{ph})\Delta f \tag{2.8}$$

where q is the elementary charge, I_d and I_{ph} are the dark current and photocurrent respectively, and Δf is the bandwidth. For a receiver system employing an APD in conjunction with an amplifier, the overall SNR of the receiver can be expressed as follows.

$$SNR = \frac{I_{ph}^2}{i_n^2 + i_{th}^2} = \frac{(\frac{q\eta P_{opt}}{h\nu})^2 M^2}{2qFM^2\big(I_d + I_{ph}\big)\Delta f + \frac{4k_b T\Delta f}{R_{eq}}} \tag{2.9}$$

where i_{th}^2 is the amplifier noise, η is the quantum efficiency, P_{opt} is the incident optical power, h is Planck's constant, ν is the frequency of light, k is Boltzmann's constant,

T is the temperature and R_{eq} is the equivalent resistance at the amplifier input. Equation 2.9 can be simplified further to give

$$SNR = \frac{(\frac{q\eta P_{opt}}{h\nu})^2}{2qF(I_d + I_{ph})B + \frac{4k_bTB}{R_{eq}M^2}} \tag{2.10}$$

It can be seen that to fully benefit from utilising an APD, the excess noise of the APD must be kept low such that the APD shot noise is less than the amplifier noise. For APDs with $k \neq 0$, excess noise increases with gain so the maximum *SNR* occurs at an optimum gain point before the diode shot noise becomes dominant. Whereas APDs with $k = 0$ have a maximum excess noise factor of 2 so the *SNR* can in principle increase indefinitely with gain.

2.3 APDs with low noise performance

From the above discussions on impact ionisation and its related noise, it is clear that APD materials with very disparate ionisation coefficients are most desirable. Most III-V materials have comparable values for α and β as can be seen in Fig. 2.5 where common APD materials are listed. Amongst these bulk materials, Si exhibits the largest difference in ionisation coefficients therefore promises high speed and low noise performance. However, low noise in APDs can be artificially induced by two methods, namely by exploiting the dead space effects or by engineering device structures that can manipulate the impact ionisation properties.

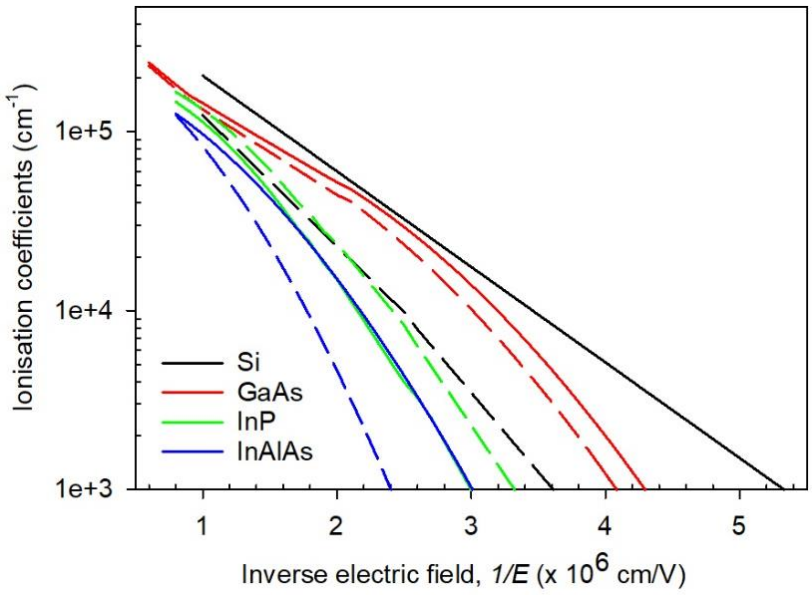

Figure 2.5 Impact ionisation coefficients of key materials. Solid and dashed lines represent the electron and hole ionisation coefficients respectively.

2.3.1 Dead space effects in thin multiplication region

Okuto and Crowell [11] first proposed that the classical view of impact ionisation does not paint a realistic picture as it is assumed that the ionising probability of a secondary carrier immediately after generation is non-zero. McIntyre's model describes the ionisation coefficients as a function of the local electric field without considering the history of the carrier. To obtain sufficient energy for an ionisation event, a carrier must travel a minimum distance within the electric field. The ionisation probability before an electron traverses said distance is therefore zero. This is known as the dead space effect and is given by

$$d_{e,h} = \frac{E_{th(e,h)}}{q\xi} \tag{2.11}$$

The effects of dead space are negligible when either the multiplication region width or the mean distance between successive ionisation events is significantly longer. However, when the dead space is of a magnitude comparable to the mean ionising path length (such as at high electric fields present in submicron devices), the multiplication process begins to deviate from the local model. It has been shown experimentally in GaAs [12], the effective ionisation coefficients are reduced which can be understood as the decreased counts of ionisation events as the dead space accounts for a substantial portion of the multiplication region. However, excess noise performance is observed

to improve in devices with a thin intrinsic region width, generally <1 μm, as shown in GaAs [13], Si [14], InP [15] and InAlAs [16] which points towards an obvious benefit in using thin multiplication widths to produce low noise APDs. This can be understood as the dead space introducing more deterministic multiplication processes despite the α/β ratio converging at high fields. It should, however, be noted that tunnelling currents can be significant in thin devices, putting a lower limit on the multiplication width.

2.3.2 APDs employing impact ionisation engineering (I^2E)

I^2E APDs are reported to utilise heterostructures to confine impact ionisation processes spatially to areas where favourable characteristics can be obtained. One early design proposed by Chin *et al.* uses a multilayered quantum well structure to introduce asymmetrical band discontinuities at the conduction and valence band as an effective method to localise the occurrence of impact ionisation at the barrier/well interface [17]. Using a suitable combination of semiconductors, one can achieve discontinuities at the interfaces such that carriers travelling from one material to the other can obtain an energy equivalent to the band offset (ideally larger than the ionisation threshold energy) and is able to trigger impact ionisation upon crossing the boundary. This APD design is known as staircase APD and an example with graded band gap is illustrated in Fig. 2.6. Under reverse bias conditions, an electron upon traversing from the wide to narrow band gap material gains an energy equal to the discontinuity at the conduction band whereas the valence band discontinuity presents an energy barrier for holes. As such, impact ionisation is favourable for electrons but suppressed for holes and a large α/β ratio can be easily achieved in a staircase APD. Multiplication would ideally occur at the abrupt discontinuities where an additional electron will be produced by a parent electron after each step and the overall gain is determined by the number of steps throughout the structure, akin to a photomultiplier tube. The noise in the APD is therefore minimised due to the well-controlled (in terms of position and total gain) ionisation processes.

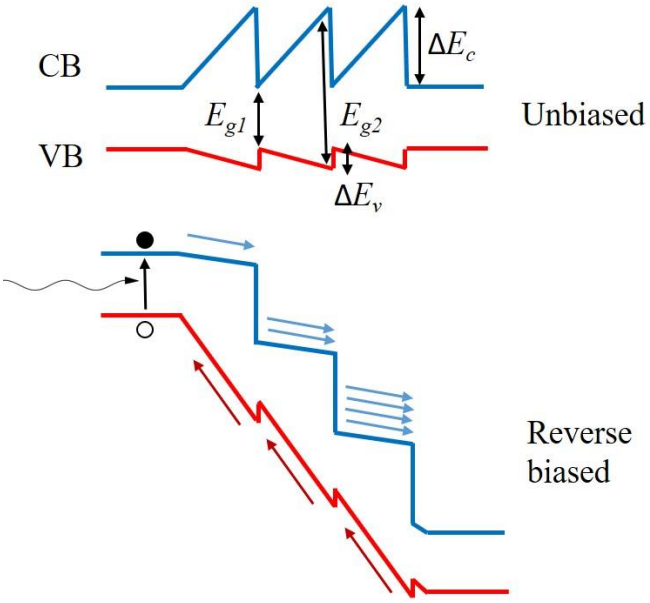

Figure 2.6 The band diagram of the staircase APD concept under zero and reverse bias conditions

Capasso *et al.* [18] were first to demonstrate the staircase APD using $Al_{0.45}Ga_{0.55}As$/GaAs quantum wells with an enhanced α/β ratio of 10 (as compared to a $k < 3$ in GaAs [19]). Although several authors do later dispute, by theoretical calculations [20] and experimental findings [21], that any enhancements to α in the $Al_{0.45}Ga_{0.55}As$/GaAs material system are not possible as the discontinuities between the satellite valleys of GaAs and $Al_{0.45}Ga_{0.55}As$ are in fact, small. Nevertheless, other material systems such as InGaAs/InAlAs (α/β ratio of 20) [22], InGaAsP/InAlAs (α/β ratio of 5) [23] and more recently AlInAsSb/GaSb (k of 0.015 or α/β ratio of >60) [24] adopting a staircase structure have shown some degree of enhanced α/β ratios.

2.4 Ion implantation

Ion implantation is a process where specific ions of interest are accelerated and embedded via physical collision inside a target sample. In semiconductor device fabrication, ion implantation is a useful low temperature tool to introduce controlled amounts of impurities as dopants into specific locations within the semiconductor in three dimensions and is widely used in modern integrated circuit technologies [25]. Shockley, in a patent dated back to 1954 [26], described the doping of n-type germanium with boron ions via ionic bombardment to form a p-n junction. In addition to the use of ion implantation for semiconductor doping, Shockley also mentioned a post-implant annealing process to repair damage to the crystal structure made by the

energetic bombardment and to thermally activate the implanted dopants. A typical ion implanter consists of an ion generating source, ionic optics to manipulate the acceleration or path of the ion beam and a housing chamber for the target specimen.

The projected range of implanted dopants, or the depth of penetration of ions in the target material, is determined by the implantation energy, ion mass, composition, density, and orientation of the target material. To selectively dope semiconductors only in the intended areas, soft (photoresist) or hard (dielectric or metal) masks, with sufficient thickness to fully impede the movement of energetic ions into unwanted regions, are used to define the implantation windows. Channelling occurs when the incident ion beams are aligned to particular orientations of the crystal plane such that the periodic ordering of the atomic lattice offers little to no resistance to the stopping of incoming ions. The stopping of an implanted ion relies on the transfer of energy from the energetic ion to the atoms in the target lattice via elastic collisions. Channelled ions propagate along a path with a smaller density of atoms, and therefore only interacts with adjacent planes of atoms by Coulombic repulsions, resulting only in small angle scattering events. A channelled ion therefore does not displace the host atoms in the lattice and penetrates deeper into the crystal, producing a tail of ions which negatively affects the intended projected range for shallow implants and also the process reproducibility. The channelling effects is exacerbated when implanting dopants of low atomic mass, such as boron into silicon as the trajectory of light ions in the crystal lattice can be influenced more easily by the lattice atoms [27]. The effects of channelling can be altered depending on the wafer growth orientation and also the relative tilt angle of the sample against the incident beam of ions since the periodic arrangement of atoms are different whether the wafer is grown in the (100) or the (111) direction [28]. Another method to minimise channelling effects during the implantation process is to tilt the samples at a 7° angle with respect to the ion beam direction for III-V materials grown in the (100) plane.

The ion implantation process can be simulated by a Monte Carlo based program known as Transport of Ions in Matter (TRIM) [29]. The program calculates the interactions between the ion and the target on an individual ion basis to provide the overall picture of the implantation profile as well as any accompanying damage done to the target with statistical quantities such as straggling, skewness and kurtosis where straggling refers to the square root of variance. Energetic ions upon entering the solid target loses

its kinetic energy via collisions with lattice atoms and electrons (termed as nuclear and electronic loss respectively).

An amount of kinetic energy from the ion is transferred to the target atoms to knock the lattice atom out of its original site. To illustrate the interaction of an incident ion within the solid, let us define a framework where the incident ion is of a mass Z_1 with energy of E_1 and the lattice is made of an element with mass Z_2. A lattice binding energy of E_b is defined as the energy required to break electronic bonds to release the lattice atom from its site and a displacement energy of E_d is defined as the energy required to move the lattice atom at least a distance of one atomic spacing away from its site. When struck by the incident ion, the lattice atom is transferred an energy of E_2 and several scenarios can occur. If E_1 is less than E_d, the incident ion of Z_1 becomes an interstitial and the energy imparted will be released as phonons in the form of lattice vibrations. If E_2 is greater than E_d, then the lattice atom is moved out of its site (displaced) with an energy reduced by E_b and the atom now becomes part of the recoil cascade. Otherwise, the struck lattice atom of Z_2 will simply release the energy of E_2 as phonons and stay in its lattice site. If the incident ion, Z_1, has remaining energy to move within the lattice, it will continue amongst the recoil cascade and cause further collisions. If not, the incident ion will come to a rest within the lattice as an interstitial or in the lattice site of the displaced atom. Further collisions caused by Z_2 can displaced other lattice atoms and if the energy E_2 becomes depleted, the atom will either sit in a lattice site as a replacement atom or become an interstitial, in a similar fashion as Z_1. While this provides a general idea of the ion implantation process, implantation in III-V semiconductor is complicated by the different displacement and lattice binding energies of the group III and V constituents.

2.5 Annealing

Damage to the crystal lattice form point defects such as vacancies and interstitials. Furthermore, clustering of point defects can form extended defects and at high implant doses, amphorisation can occur. These are undesirable side effects of the implantation process. By subjecting the sample to an annealing cycle, lattice damages can be repaired to some degree and the implanted ions can be promoted into empty lattice sites. However, the annealing scheme required is distinguished by the type of defect formation. An extensive review of defect production and damage distributions from

ion implantation can be found in [30]. Parameters to optimise annealing include the temperature and duration of anneal, environment in the annealing chamber as well as the annealing technique itself. For example in GaAs [31], recrystallisation of amorphous regions occurs at anneal temperatures below 500 °C but the process introduces stacking faults and dislocation loops. These extended defects can be eradicated at temperatures around 700 °C. Temperatures of above 750 °C (depending on the dopant species) are required to obtain significant electrical activity in GaAs which is significantly higher than the epitaxial growth temperatures of GaAs. The issue of annealing is convoluted in III-V semiconductors due to the low temperatures where decomposition begins, typically 500 – 600 °C, thereafter dissociation of volatile group V elements is likely to occur. To protect the semiconductor, several techniques to encapsulate the sample surface can be employed namely by deposition of a thin dielectric layer on the surface, clamping the sample with substrates of the same material or by providing a suitable ambient partial vapour pressure of the group V element within the chamber.

The ion implantation process introduces a significant amount of dopant impurities locally distributed at a depth which forms a concentration gradient. The application of an annealing treatment provides dopants with thermal energy to diffuse within the crystal lattice and Fick's law can be used to describe the motion of mobile atoms in one dimension [32]. The Frank-Turnbull mechanism models diffusion for dopant species that are able to exist in interstitial and substitutional sites [33]. Using Zn in GaAs as an example, interstitial Zn possesses diffusivity higher than that of substitutional Zn. Hence, Zn diffuses in GaAs in the form of an interstitial which upon encountering Ga vacancies, will become enter the lattice site as a substitutional atom and contribute hole carriers. Another diffusion model proposed by Gösele and Morehead [34] is the kick-out mechanism where Zn interstitials are able to remove Ga atoms off their lattice sites to produce Ga interstitials. In both examples, the production of Ga vacancies is a crucial factor in determining the diffusivity of Zn and van Ommen found that the kick-out mechanism to more accurately describe diffusion of Zn in GaAs due to the more effective creation of Ga vacancies from Frenkel defects [35].

The activation of dopants in GaAs, donors and acceptors alike, has been observed to depend more critically on the annealing temperature over the annealing duration [36]. Annealing at 950 °C for 5 seconds shows higher electrical activation of silicon in

GaAs than annealing at 850 °C for 15 minutes and that a long duration anneal of 15 minutes offers diminishing improvements over a 10 seconds anneal at 850 °C [37]. The long annealing durations that comes with conventional furnace anneals exposes the semiconductor sample to chamber contaminants and places stringent requirements on the thermal stability of encapsulants. Aside from that, unwanted dopant diffusion can occur during long duration anneals, altering the intended distribution profile of dopants. Rapid thermal annealing (RTA) is therefore widely adopted as an alternative to furnace annealers to achieve high temperature anneals within short durations down to the order of seconds. In an RTA system, the sample wafer is heated uniformly via infrared radiation from incandescent lamps with thermocouples or pyrometers to monitor the wafer temperature and provide feedback to the lamp control. An RTA system offers several advantages as the ramp up and ramp down time can be significantly shortened from direct heating of the wafer and the thermal gradient within the wafer is minimised by applying radiant energy uniformly.

2.6 Edge breakdown in planar devices

Ion implanted dopants tend to form abrupt junction geometries with well-defined vertical depth by the projected range of the ions and lateral spread by the thick blocking mask within device structures. If the p-n junction is located at the implanted boundary, electric field crowding at the p-n interface increases the likelihood of premature device breakdown. The formation of localised electric field hotspots impedes APD performance as avalanche breakdown will occur before meaningful gain can be obtained from the bulk material and breakdown will take place at a reduced voltage. A similar effect of local electric hotspots is observed in early investigations into non-uniform avalanche breakdowns in p-n junctions which was attributed to microplasmas in poor quality crystals [38]. Although the breakdown mechanism in InAs is soft, localised hotspots will result in poor spatial uniformity of gain and potentially large leakage currents (such as band to band tunnelling current).

The key to suppress edge breakdown is to decrease the intensity of electric around the junction edges which can be performed either by redistributing the equipotential lines around the junction edge or manipulating the radius of curvature at the junction. The former can be achieved is by forming an annular floating guard ring structure with the same doping type and concentration as the implant window during the same

implantation process [39]. As the voltage bias increases, equipotential lines extend outwards. Upon contacting the inner edge of guard ring(s), the equipotential lines are extended to the outer guard ring edge because of the equipotential surface at the highly doped guard ring. The equipotential lines are spread across in the lateral direction and the electric field at the junction edge is therefore, reduced. Guard rings are commonly employed in the fabrication of planar InGaAs/InP SAM-APD structures for telecommunication applications [39]–[42]. The guard rings can also be biased with an applied voltage or grounded to ensure a low field region at the junction edge or to redirect the flow of surface currents [43]. For planar devices formed using the diffusion of Zn for p-type doping, a double diffusion process in combination with floating guard rings has shown to reduce edge breakdown characteristics in InGaAs/InP SAM-APDs [40]. The second diffusion process with a smaller diffusion window is used to drive-in Zn dopants deeper in the active region to form an overall curved junction edge in conjunction with the initial diffusion process and the guard rings are shown to suppress edge breakdown (by lowering the surface electric field) from measurements of the spatial gain profile at fixed biases [40]. The use of floating guard rings, however, do present an issue in diode arrays in that the effective diode area increases as the lateral field extends to the guard ring edge [39]. An advantage for incorporating floating guard rings is that the device will not see an increase in capacitance (despite the lateral increase in depletion region) because the guard ring capacitance is added as a series capacitance and is much larger than the device capacitance [39]. However, in floating guard ring design, the implanted dopants may diffuse and reduce the effective guard ring-junction distance, hence an initial optimisation of the structure is required [40].

In Si complementary metal-oxide-semiconductor (CMOS) SPADs, virtual guard rings are seeing an increase in replacing p-well guard rings in order to meet demands for scaling down of device active area [44]–[46]. The conventional p-well guard rings around the periphery of the active device region function in a similar fashion as floating guard rings mentioned above, however, due to continued scaling in CMOS devices, the p-well guard rings eventually limit the minimum device diameter by merging the depletion region away from the intended active region [47]. A virtual guard ring is implemented by introducing a buried n-well below the p^+-anode, so the active region and maximum electric field is formed at this particular junction [48]. Low doping levels in the buried n-well acts to spread the depletion region laterally and

lower the electric field at the surface, reducing breakdown and surface dark counts. The virtual guard ring implementation boasts a few flexibilities in structure design in that additional p-wells and n-wells can be introduced between the p^+-anode and buried n-well to 1) control maximum field strength (to reduce tunnelling dark counts), 2) adjust the depth of the active region (to enhance absorption of longer wavelength photons) and 3) manipulate the doping profile (to suppress tunnelling dark counts) [48].

2.7 Planar array design considerations

In the design of planar arrays, crosstalk becomes a major issue to overcome which is less of a concern in mesa arrays due to the physical isolation between devices. Crosstalk refers to the contamination of signal collected in one diode that does not originate from said diode. In image sensing photodiode arrays, crosstalk decreases the pixel-to-pixel contrast [49]. More worryingly in APD or SPAD arrays, the occurrence of crosstalk can trigger avalanche breakdown events and register as false detection of incoming optical signals [50]. Much like afterpulsing issues in SPADs, crosstalk presents a limit to the pulsing rate in arrays [51].

Crosstalk in an array can be classified into two categories, electrical and optical crosstalk. Electrical crosstalk is a result of the lateral diffusion or drift of generated carriers from neighbouring diodes. Depending on the design and operation in terms of applied bias and absorption wavelengths of interest, the extent of electrical crosstalk in photodiode arrays varies. On the other hand, optical crosstalk arises due to factors such as the bending of light at the air-semiconductor interface from adjacent areas of illumination, the angled reflection of light at the substrate-metal interface back into the semiconductor material and even the recombination of carriers can create photons within the semiconductor which leads to photon recycling events.

The extent of electrical crosstalk in arrays is affected by a few factors such as the minority carrier diffusion length, the absorption coefficient at the wavelength of interest, the direction of incident light whether the array is of a front-illuminated or a back-illuminated design, and the junction depth. The former is self-explanatory in that the non-equilibrium photogenerated carriers in a high quality crystalline material possess a long lifetime and hence allows for possible lateral diffusion into adjacent

diodes. The latter three factors play different roles to manipulate the absorption profile in a diode array. The more common configuration of two-dimensional arrays is to connect the array anodes to an external Si-based read-out circuitry by flip-chip bonding. This then requires the array to be orientated substrate side up such that the incident optical signals are entering through the back of the array. The substrate material would need to be optically transparent in the wavelength of interest to avoid any attenuation of optical signals and this is known as back-illumination. For a back-illuminated array with the p-n junction boundary at the opposite end of the substrate, following the exponential relation of absorption with penetration depth, the main source of carrier generation will be away from the depletion region. This not only limits the collection efficiency of the diode itself, but also hinders the performance of neighbouring pixels due to the lateral diffusion of the photogenerated carriers. Crosstalk in back-illuminated arrays is aggravated if the junction formation in a thick structure is shallow and if the material has a large absorption coefficient [52].

The mitigation of crosstalk can be achieved by increasing the diode to diode spacing, however, such a simple method incurs losses in the array fill factor which limits the resolution of image sensors. This problem is exacerbated in small area diodes in that the active photoactive area to lateral area ratio is lower and any carriers generated in adjacent areas can contribute to a large percentage of current [53]. More effective methods of crosstalk reduction include the introduction of an intentionally high defect concentration zones to encourage carrier recombination [54] or a highly doped wall/guard ring structure around a pixel to block carrier diffusion [55]–[57]. Trench designs surrounding individual pixels to terminate the lateral propagation of carriers have also been incorporated and tested in arrays using additional dielectric deposition as isolation [58] or metal layers [59] to block lateral carriers. In such trench designs, problems in the uniformity of deep trench etching and filling can arise, again depending on the junction depth and trench depth required [60]. These methods are targeted at minimising electrical crosstalk; for optical crosstalk, one method to reduce the back-reflection of optical signals at the bottom substrate-metal interface can be realised by growing semiconductor layers sensitive to the wavelength interested to attenuate the residual unabsorbed light signal [61].

For the design of a planar InAs APD array, there currently remains a number of uncertainty with regards to methods to control edge breakdown, suppress surface dark currents and reduce pixel crosstalk. To obtain high gain performance, a pure electron injection into the depletion region is required by absorbing most of the incident photons in the p-type region. In [62], this was achieved by a double implant of Be ions at 70 and 200 keV to produce a 1 μm thick p-type region. Guard rings implemented in [62] show little improvement to suppressing edge breakdown effects and was not found to decrease the diode dark current at 200 K. Due to the nature of guard rings, the effective diode area increases which is not desirable in an array with small area diodes. The effects of guard rings in Si CMOS APD showed that devices with shallow trench isolation produce the largest electric field (and highest gain) at the active junction and lowest peripheral electric field [63]. While trench isolation is promising in confining the electric field to the active junction, the trench depth required is dependent on the junction depth [64] and for InAs may introduce a large, exposed surface area. Deep levels introduced from He ions has been shown to produce highly resistive regions in GaAs [65]. Similarly, deep He implantation followed by annealing in a p-i-n structure InAs was shown to produce an increased sheet resistivity and provide electrical isolation but causes high peripheral electric field that inhibits APD operation [66].

2.8 Reference

[1] G. E. Stillman and C. M. Wolfe, ‘Avalanche photodiodes’, in *Semiconductors and semimetals*, vol. 12, Elsevier, 1977, pp. 291–393.

[2] R. B. Emmons, ‘Avalanche-photodiode frequency response’, *J. Appl. Phys.*, vol. 38, no. 9, pp. 3705–3714, 1967.

[3] M. L. Cohen and T. K. Bergstresser, ‘Band Structures and Pseudopotential Form Factors for Fourteen Semiconductors of the Diamond and Zinc-blende Structures’, *Phys. Rev.*, vol. 141, no. 2, pp. 789–796, Jan. 1966, doi: 10.1103/PhysRev.141.789.

[4] I. C. Sandall, J. S. Ng, S. Xie, P. J. Ker, and C. H. Tan, ‘Temperature dependence of impact ionization in InAs’, *Opt. Express*, vol. 21, no. 7, p. 8630, Apr. 2013, doi: 10.1364/OE.21.008630.

[5] C. L. Anderson and C. R. Crowell, ‘Threshold Energies for Electron-Hole Pair Production by Impact Ionization in Semiconductors’, *Phys. Rev. B*, vol. 5, no. 6, pp. 2267–2272, Mar. 1972, doi: 10.1103/PhysRevB.5.2267.

[6] W. Nakwaski, ‘Effective masses of electrons and heavy holes in GaAs, InAs, AlAs and their ternary compounds’, p. 25.

[7] K. Brennan and K. Hess, ‘High field transport in GaAs, InP, InAs’, *Solid-State Electron.*, vol. 27, no. 4, pp. 347–357, 1984.

[8] A. R. J. Marshall, J. P. R. David, and C. H. Tan, ‘Impact Ionization in InAs Electron Avalanche Photodiodes’, *IEEE Trans. Electron Devices*, vol. 57, no. 10, pp. 2631–2638, Oct. 2010, doi: 10.1109/TED.2010.2058330.

[9] M. A. Kinch, J. D. Beck, C.-F. Wan, F. Ma, and J. Campbell, ‘HgCdTe electron avalanche photodiodes’, *J. Electron. Mater.*, vol. 33, no. 6, pp. 630–639, Jun. 2004, doi: 10.1007/s11664-004-0058-1.

[10] R. J. McIntyre, ‘Multiplication noise in uniform avalanche diodes’, *IEEE Trans. Electron Devices*, vol. 1, pp. 164–168, 1966.

[11] Y. Okuto and C. R. Crowell, ‘Ionization coefficients in semiconductors: A nonlocalized property’, *Phys. Rev. B*, vol. 10, no. 10, pp. 4284–4296, Nov. 1974, doi: 10.1103/PhysRevB.10.4284.

[12] S. A. Plimmer *et al.*, ‘Investigation of impact ionization in thin GaAs diodes’, *IEEE Trans. Electron Devices*, vol. 43, no. 7, pp. 1066–1072, Jul. 1996, doi: 10.1109/16.502416.

[13] K. F. Li, D. S. Ong, J. P. R. David, R. C. Tozer, P. N. Robson, and R. Grey, ‘Avalanche Multiplication Noise Characteristics in Thin GaAs p -i-n Diodes’, *IEEE Trans. ELECTRON DEVICES*, vol. 45, no. 10, p. 6, 1998.

[14] C. H. Tan *et al.*, ‘Avalanche noise measurement in thin Si p+-i-n+ diodes’, *Appl. Phys. Lett.*, vol. 76, p. 4, 2000.

[15] L. J. J. Tan, J. S. Ng, C. H. Tan, and J. P. R. David, ‘Avalanche Noise Characteristics in Submicron InP Diodes’, *IEEE J. Quantum Electron.*, vol. 44, no. 4, pp. 378–382, Apr. 2008, doi: 10.1109/JQE.2007.914771.

[16] Y. L. Goh *et al.*, ‘Excess Avalanche Noise in $\hbox{In}_{0.52}\hbox{Al}_{0.48}\hbox{As}$’, *IEEE J. Quantum Electron.*, vol. 43, no. 6, pp. 503–507, Jun. 2007, doi: 10.1109/JQE.2007.897900.

[17] R. Chin, N. Holonyak, G. E. Stillman, J. Y. Tang, and K. Hess, ‘Impact ionisation in multilayered heterojunction structures’, *Electron. Lett.*, vol. 16, no. 12, p. 467, 1980, doi: 10.1049/el:19800329.

[18] F. Capasso, W. T. Tsang, A. L. Hutchinson, and G. F. Williams, ‘Enhancement of electron impact ionization in a superlattice: A new avalanche photodiode with a large ionization rate ratio’, *Appl. Phys. Lett.*, vol. 40, no. 1, pp. 38–40, Jan. 1982, doi: 10.1063/1.92910.
[19] G. E. Bulman and G. E. Stillman, ‘The Determination of Impact Ionization Coefficients in (100) Gallium Arsenide Using Avalanche Noise and Photocurrent Multiplication Measurements’, *IEEE Trans. ELECTRON DEVICES*, vol. ED-32, no. 11, p. 13, 1985.
[20] I. K. Czajkowski, J. Allam, and A. R. Adams, ‘Role of satellite valleys in ionisation rate enhancement in multiple quantum well avalanche photodiodes’, *Electron. Lett.*, vol. 26, no. 16, p. 1311, 1990, doi: 10.1049/el:19900843.
[21] C. K. Chia *et al.*, ‘Multiplication and excess noise in AlxGa1-xAs/GaAs multilayer avalanche photodiodes’, *J. Appl. Phys.*, vol. 94, p. 2631, 2003.
[22] T. Kagawa, Y. Kawamura, H. Asai, M. Naganuma, and O. Mikami, ‘Impact ionization rates in an InGaAs/InAlAs superlattice’, *Appl. Phys. Lett.*, vol. 55, no. 10, pp. 993–995, Sep. 1989, doi: 10.1063/1.101699.
[23] T. Kagawa, Y. Kawamura, and H. Iwamura, ‘InGaAsP-InAlAs Superlattice Avalanche Photodiode’, *IEEE J. Quantum Electron.*, vol. 28, no. 6, p. 1419, 1992.
[24] M. Ren, S. Maddox, Y. Chen, M. Woodson, J. C. Campbell, and S. Bank, ‘AlInAsSb/GaSb staircase avalanche photodiode’, *Appl. Phys. Lett.*, vol. 108, no. 8, p. 081101, Feb. 2016, doi: 10.1063/1.4942370.
[25] R. B. Fair, ‘History of some early developments in ion-implantation technology leading to silicon transistor manufacturing’, *Proc. IEEE*, vol. 86, no. 1, pp. 111–137, Jan. 1998, doi: 10.1109/5.658764.
[26] W. Shockley, ‘Forming semiconductive devices by ionic bombardment’, 2787564, Apr. 02, 1957.
[27] K. Cho, W. R. Allen, T. G. Finstad, Chu W. K., J. Liu, and J. J. Wortman, ‘Channeling effect for low energy ion implantation in Si’, *Nucl. Instrum. Methods Phys. Res.*, vol. B7/8, pp. 265–272, 1985.
[28] J. F. Gibbons, ‘Ion implantation in semiconductors—Part I: Range distribution theory and experiments’, *Proc. IEEE*, vol. 56, no. 3, pp. 295–319, 1968, doi: 10.1109/PROC.1968.6273.
[29] J. P. Biersack and L. G. Haggmark, ‘A Monte Carlo computer program for the transport of energetic ions in amorphous targets’, *Nucl. Instrum. Methods*, vol. 174, no. 257–269, p. 1980.
[30] J. F. Gibbons, ‘Ion Implantationin Semiconductors-Part II: Damage Productionand Annealing’, *ION Implant. Semicond.*, p. 45, 1972.
[31] W. Wesch, ‘Ion implantation in III-V compounds’, *Nucl. Instrum. Methods Phys. Researcb*, vol. B68, pp. 342–354, 1992.
[32] B. Tuck, ‘Mechanisms of atomic diffusion in the III-V semiconductors’, *J. Phys. Appl. Phys.*, vol. 18, no. 4, pp. 557–584, Apr. 1985, doi: 10.1088/0022-3727/18/4/002.
[33] F. C. Frank and D. Turnbull, ‘Mechanism of Diffusion of Copper in Germanium’, *Phys. Rev.*, vol. 104, no. 3, pp. 617–618, Nov. 1956, doi: 10.1103/PhysRev.104.617.
[34] U. Gösele and F. Morehead, ‘Diffusion of zinc in gallium arsenide: A new model’, *J. Appl. Phys.*, vol. 52, p. 4617, 1981.
[35] A. H. van Ommen, ‘Examination of models for Zn diffusion in GaAs’, *J. Appl. Phys.*, vol. 54, no. 9, pp. 5055–5058, Sep. 1983, doi: 10.1063/1.332777.

[36] B. J. Sealy, ‘Rapid thermal annealing of ion-implanted GaAs’, *Semicond. Sci. Technol.*, vol. 3, no. 5, pp. 448–451, May 1988, doi: 10.1088/0268-1242/3/5/004.
[37] N. Morris and B. J. Sealy, ‘Diffusion and activation mechanism in ion-implanted GaAs’, *Nucl. Instrum. Methods Phys. Res. B*, vol. 39, pp. 453–456, 1989.
[38] R. H. Haitz, A. Goetzberger, R. M. Scarlett, and W. Shockley, ‘Avalanche Effects in Silicon *p—n* Junctions. I. Localized Photomultiplication Studies on Microplasmas’, *J. Appl. Phys.*, vol. 34, no. 6, pp. 1581–1590, Jun. 1963, doi: 10.1063/1.1702639.
[39] Y. Liu *et al.*, ‘Simple, very low dark current, planar long-wavelength avalanche photodiode’, *Appl. Phys. Lett.*, vol. 53, p. 1311, 1988.
[40] Y. Liu, S. R. Forrest, J. Hladky, M. J. Lange, G. H. Olsen, and D. E. Ackley, ‘A planar InP/InGaAs avalanche photodiode with floating guard ring and double diffused junction’, *J. Light. Technol.*, vol. 10, no. 2, pp. 182–193, Feb. 1992, doi: 10.1109/50.120573.
[41] T. Shirai, S. Yamazaki, H. Kawata, and K. Nakajima, ‘A Planar I n P h G a A s P Heterostructure Avalanche Photodiode’, p. 4.
[42] K. Taguchi *et al.*, ‘Planar InP/InGaAs avalanche photodiodes with preferential lateral extended guard ring’, *IEEE Electron Device Lett.*, vol. 7, no. 4, pp. 237–258, 1986.
[43] V. Mishra, V. D. Srivastava, and S. K. Kataria, ‘Role of guard rings in improving the performance of silicon detectors’, *Pramana*, vol. 65, no. 2, pp. 259–272, Aug. 2005, doi: 10.1007/BF02898614.
[44] T. Leitner *et al.*, ‘Measurements and Simulations of Low Dark Count Rate Single Photon Avalanche Diode Device in a Low Voltage 180-nm CMOS Image Sensor Technology’, *IEEE Trans. Electron Devices*, vol. 60, no. 6, pp. 1982–1988, Jun. 2013, doi: 10.1109/TED.2013.2259172.
[45] D. Shin, B. Park, Y. Chae, and I. Yun, ‘The Effect of a Deep Virtual Guard Ring on the Device Characteristics of Silicon Single Photon Avalanche Diodes’, *IEEE Trans. Electron Devices*, vol. 66, no. 7, pp. 2986–2991, Jul. 2019, doi: 10.1109/TED.2019.2913714.
[46] J. A. Richardson, L. A. Grant, and R. K. Henderson, ‘Low Dark Count Single-Photon Avalanche Diode Structure Compatible With Standard Nanometer Scale CMOS Technology’, *IEEE Photonics Technol. Lett.*, vol. 21, no. 14, pp. 1020–1022, Jul. 2009, doi: 10.1109/LPT.2009.2022059.
[47] N. Faramarzpour, M. J. Deen, S. Shirani, and Q. Fang, ‘Fully Integrated Single Photon Avalanche Diode Detector in Standard CMOS 0.18- μm Technology’, *IEEE Trans. Electron Devices*, vol. 55, no. 3, pp. 760–767, Mar. 2008, doi: 10.1109/TED.2007.914839.
[48] J. A. Richardson, E. A. G. Webster, L. A. Grant, and R. K. Henderson, ‘Scaleable Single-Photon Avalanche Diode Structures in Nanometer CMOS Technology’, *IEEE Trans. Electron Devices*, vol. 58, no. 7, pp. 2028–2035, Jul. 2011, doi: 10.1109/TED.2011.2141138.
[49] Ji Soo Lee, R. I. Hornsey, and D. Renshaw, ‘Analysis of cmos photodiodes-part II: lateral photoresponse’, *IEEE Trans. Electron Devices*, vol. 50, no. 5, pp. 1239–1245, May 2003, doi: 10.1109/TED.2003.813233.
[50] I. Rech *et al.*, ‘A New Approach to Optical Crosstalk Modeling in Single-Photon Avalanche Diodes’, *IEEE Photonics Technol. Lett.*, vol. 20, no. 5, pp. 330–332, 2008, doi: 10.1109/LPT.2007.915654.

[51] A. Ficorella *et al.*, 'Crosstalk mapping in CMOS SPAD arrays', in *2016 46th European Solid-State Device Research Conference (ESSDERC)*, Lausanne, Switzerland, Sep. 2016, pp. 101–104, doi: 10.1109/ESSDERC.2016.7599598.
[52] S. Hinckley, P. V. Jansz, E. A. Gluszak, and K. Eshraghian, 'Modelling of device structure effects on electrical crosstalk in back illuminated CMOS compatible photodiodes', in *2002 Conference on Optoelectronic and Microelectronic Materials and Devices. COMMAD 2002. Proceedings (Cat. No.02EX601)*, Sydney, NSW, Australia, 2002, pp. 397–400, doi: 10.1109/COMMAD.2002.1237274.
[53] B. Blanco-Filgueira, P. López, and J. B. Roldán, 'Analytical modelling of size effects on the lateral photoresponse of CMOS photodiodes', *Solid-State Electron.*, vol. 73, pp. 15–20, 2012.
[54] C. N. Anagnostopoulos, E. T. Nelson, J. P. Lavine, K. Y. Wong, and D. N. Nichols, 'Latch-up and image crosstalk suppression by internal gettering', *IEEE Trans. Electron Devices*, vol. 31, no. 2, pp. 225–231, Feb. 1984, doi: 10.1109/T-ED.1984.21505.
[55] I. Goushcha, B. Tabbert, and A. O. Goushcha, 'Optical and electrical crosstalk in pin photodiode array for medical imaging applications', in *2007 IEEE Nuclear Science Symposium Conference Record*, Honolulu, HI, USA, 2007, pp. 4348–4353, doi: 10.1109/NSSMIC.2007.4437077.
[56] F. Ji, M. Juntunen, and I. Hietanen, 'Electrical crosstalk in front-illuminated photodiode array with differentguard ring designs for medical CT applications.pdf', *Nucl. Instrum. Methods Phys. Res. A*, vol. 607, pp. 150–153, 2009.
[57] X. Li *et al.*, 'Crosstalk study of near infrared InGaAs detectors', Baltimore, Maryland, United States, May 2016, p. 98192A, doi: 10.1117/12.2222736.
[58] E. Sciacca *et al.*, 'Arrays of Geiger mode avalanche photodiodes', *IEEE Photonics Technol. Lett.*, vol. 18, no. 15, pp. 1633–1635, Aug. 2006, doi: 10.1109/LPT.2006.879576.
[59] N. Calandri, M. Sanzaro, L. Motta, C. Savoia, and A. Tosi, 'Optical Crosstalk in InGaAs/InP SPAD Array: Analysis and Reduction With FIB-Etched Trenches', *IEEE Photonics Technol. Lett.*, vol. 28, no. 16, pp. 1767–1770, Aug. 2016, doi: 10.1109/LPT.2016.2570278.
[60] B. J. Park *et al.*, 'Deep Trench Isolation for Crosstalk Suppression in Active Pixel Sensors with 1.7 μm Pixel Pitch', *Jpn. J. Appl. Phys.*, vol. 46, no. 4B, pp. 2454–2457, Apr. 2007, doi: 10.1143/JJAP.46.2454.
[61] R. D. Younger *et al.*, 'Crosstalk analysis of integrated Geiger-mode avalanche photodiode focal plane arrays', Orlando, Florida, USA, May 2009, p. 73200Q, doi: 10.1117/12.819173.
[62] B. S. White, 'Planar InAs avalanche photodiodes for infrared sensing: Towards a true solid state photomultiplier', University of Sheffield, Sheffield, U. K., 2016.
[63] M.-J. Lee, H. Rucker, and W.-Y. Choi, 'Effects of Guard-Ring Structures on the Performance of Silicon Avalanche Photodetectors Fabricated With Standard CMOS Technology', *IEEE Electron Device Lett.*, vol. 33, no. 1, pp. 80–82, Jan. 2012, doi: 10.1109/LED.2011.2172390.
[64] W. Zhi, Q. Quan, P. Yu, and Y. Jiang, 'A 45 nm CMOS Avalanche Photodiode with 8.4-GHz Bandwidth', *Micromachines*, vol. 11, no. 1, p. 65, Jan. 2020, doi: 10.3390/mi11010065.

[65] S. Ahmed, R. Gwilliam, and B. J. Sealy, ‘Ion-beam-induced isolation of GaAs layers by $^{4}He^{+}$ implantation: effects of hot implants’, *Semicond. Sci. Technol.*, vol. 16, no. 10, pp. L64–L67, Oct. 2001, doi: 10.1088/0268-1242/16/10/102.
[66] I. Sandall, C. H. Tan, A. Smith, and R. Gwilliam, ‘Planar InAs photodiodes fabricated using He ion implantation’, p. 9, 2012.

Chapter 3 Experimental methodology

To assess the performance of an APD, electrical and optical measurements such as current-voltage, capacitance-voltage (C-V), responsivity and gain are required. Key performance parameters of APDs include the reverse breakdown voltage, pre-breakdown reverse dark current, tunnelling current, contact resistance, responsivity at unity gain, carrier multiplication characteristics, bandwidth, excess noise factor and their temperature dependence characteristics. The on-wafer measurement techniques and details of interpretation are presented in this chapter.

3.1 Current-voltage measurement

I-V measurements are the most fundamental characterisation of an APD and usually performed as the first measurement post-fabrication. I-V curves give information about diode properties such as the ideality factor, series resistance, dominant bulk current mechanism, presence of surface currents and breakdown properties (whether by tunnelling or avalanche). I-V measurements are performed using the HP4104 picoammeter or the Keithley 236 Source-Measure Unit (SMU) with the equipment applying a DC bias voltage and measuring the current.

The total current flowing through an ideal diode can be described by Shockley's diode equation [1] as in equation 3.1. For a practical device, the influence of series resistance at large current conditions is included as in equation 3.2.

$$J = J_0[\exp(\frac{qV_{bias}}{nk_bT}) - 1] \tag{3.1}$$

$$J = J_0[\exp(\frac{q(V_{bias} - JR_s)}{nk_bT}) - 1] \tag{3.2}$$

where J is the total current density, J_0 is the saturation current density, q is the elementary charge, V_{bias} is the applied voltage, n is the ideality factor, k_b is the Boltzmann's constant, T is the temperature and R_s is the series resistance. The current increases exponentially with forward bias voltage but quickly saturates to the value of J_0 with a small increment of reverse voltage.

By fitting the measured forward I-V characteristics to the ideal diode equation, the ideality factor and series resistance can be extracted. The ideality factor ranges from 1 to 2, where a value close to 1 indicates diffusion dominated current and a value close

to 2 indicates generation-recombination (G-R) dominated current. In most high quality devices, the ideality factor approaches 1 at high injection conditions from an initial value closer to 2. This is explained as the carriers filling up trap states (recombination centres) initially until diffusion current dominates at large current flow conditions. For narrow bandgap materials, diffusion current easily dominates at room temperature due to a large intrinsic carrier concentration, n_i. The JR product refers to the voltage drop across the contact resistance at the metal-semiconductor junction. A low series resistance is desirable to minimise the unintended voltage drop during high gain measurements and to increase the RC response time of the diode. To obtain a low series resistance, metals are deposited onto high conductivity (high doping concentration, narrow bandgap) contact layers and annealed to promote intermixing at the metal-semiconductor interface. The selection of metals (of suitable work function relative to the semiconductor's electron affinity) is also important to ensure the formation of an ohmic junction.

Deviations from the ideal diode equation in the reverse direction occurs due to generation-recombination current, tunnelling current, surface shunt currents [2]. Therefore the total dark current observed in p-i-n diodes is a superposition of the individual current transport mechanisms and each current component may dominate at different bias voltage and temperature ranges.

The reverse saturation current, J_0, of a p-n junction refers to the diffusion of minority carriers in the p- and n-type material which is described as follows.

$$J_0 = qn_i^2 \frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A} \tag{3.3}$$

where D, and L refers to the diffusion constant and minority carrier diffusion length respectively; the subscripts p, n refers to the minority carriers electron and hole; N_D is the donor concentration in the n-type material and N_A is the acceptor concentration in the p-type material. The n_i term is dependent on the band gap of the semiconductor material and temperature, hence, high reverse saturation currents are commonly found in narrow band gap materials at room temperature.

Carrier generation and recombination processes happen when the equilibrium state is perturbed. These processes can involve direct band to band transitions or trap assisted transitions, also known as Shockley-Read-Hall (SRH) recombination. In real

semiconductor devices, the dominant recombination process is the SRH process due to defects introduced by imperfect crystal growth. SRH currents are described by the following equation where W is the depletion width and τ is the carrier lifetime.

$$J_{SRH} = \frac{qn_iW}{\tau} \tag{3.4}$$

The SRH current is proportional to the depletion width and inversely proportional to the carrier lifetime which is affected by impurities and defects in the semiconductor. For materials with short minority carrier lifetime, one method to minimise SRH currents would be to have a shorter depletion width, in a p-i-n photodiode, that would mean having a narrower intrinsic region thickness. However, this may then incur losses in the quantum efficiency of the photodiode.

Under high electric field conditions, the tunnelling phenomenon can become the dominant current mechanism. Tunnelling is a quantum mechanical process where electrons can 'penetrate' through the potential barrier [3]. Under high reverse voltages in a p-n or p-i-n diode, significant band bending occurs. Therefore, electrons from the valence band of the p-type material can tunnel through the barrier into the conduction band of the n-type material, if there are unoccupied energy states of the same energy level (for the conservation of energy). The tunnelling phenomenon for a p-n diode under reverse bias is illustrated in Fig. 3.1. The band-to-band tunnelling current in a p-i-n junction follows equation 3.5 [4].

$$J_{tunn} = \frac{(2m^*)^{1/2}q^3\xi V_r}{4\pi^2\hbar^2E_g^{1/2}}\exp\left(-\frac{\gamma m^{*1/2}E_g^{3/2}}{q\hbar\xi}\right) \tag{3.5}$$

where m^* is the carrier effective mass, ξ is the electric field, V_r is the applied reverse voltage, $\hbar$ is reduced Planck's constant, E_g is the bandgap, γ is the tunnelling parameter dependent on the barrier shape (ranging from 1.11 for a parabolic barrier to 1.88 for a triangular barrier) [5]. The main parameters affecting tunnelling current are the electric field strength, band gap (hence temperature) and barrier shape. The tunnelling probability is inversely proportional to the barrier width so the tunnelling current in a narrow band gap material (like in InGaAs, InAs) will be significant. In indirect band gap semiconductor materials, an additional E_{phonon} term is added to account for the need of a phonon to allow the indirect transition of electrons from the valence band to the conduction band for the conservation of momentum [1].

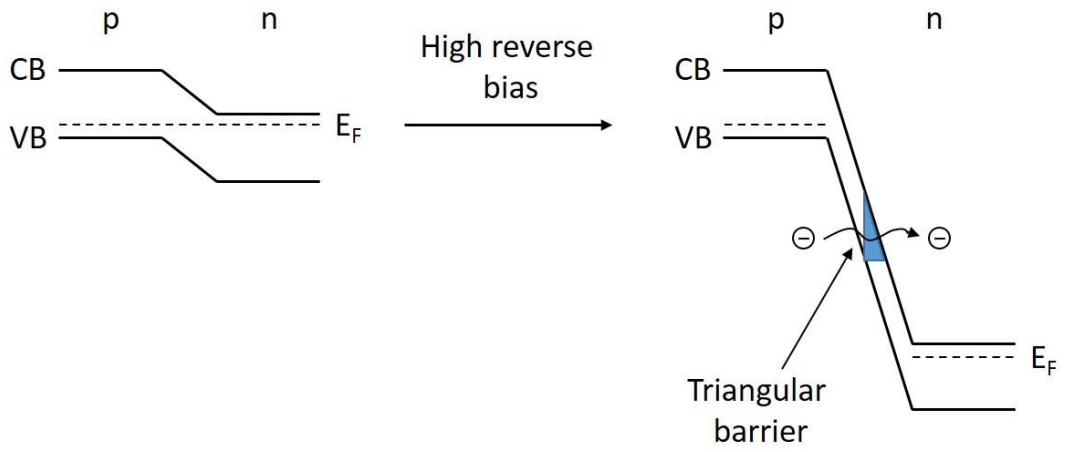

Figure 3.1 Tunnelling in p-n junction with a triangular barrier under high reverse bias

The bulk current mechanisms in a semiconductor material scale with the device area. To distinguish between bulk and surface mechanisms, the raw current data is normalised by the device area and perimeter to obtain the current density, J, and the peripheral current I/P, where P is the device perimeter. This gives information about the quality of the fabrication process. If surface leakage current contributes considerably to the total current, the wet etching and passivation scheme would require improvement and optimisation. Defect states due to abrupt interfaces, lack of passivation, dangling bonds contributes as recombination sites, allowing surface current paths along the diode periphery. Dielectric breakdown at high electric fields also poses as an additional parallel current path which increases the diode current unintentionally. One method to extract the bulk and surface leakage currents is by fitting the total measured current of devices of various radii, r, to equation 3.6 to obtain the J_{bulk} and $J_{surface}$ terms where the former refers to the bulk current contribution and the latter indicates the surface contribution to the total current.

$$I_{total} = \pi r^2 J_{bulk} + 2\pi r J_{surface} \tag{3.6}$$

A comparison of the current-voltage characteristics of an InGaAs p-i-n diode in the dark and under white light illumination is shown in Fig. 3.2. At forward bias, an initial decrease in the total current is apparent and is caused by the flow of photogenerated minority carriers (minority electrons from p- to n- and minority holes from n- to p-) and the majority carriers (majority electrons from n- to p- and majority holes from p- to n-) in the opposite direction. Whereas in the reverse bias regime, the increase in current is due to the contribution of photogenerated minority carriers. This effect is commonly

seen in diodes operating in the photovoltaic mode such as solar cells. For infrared detectors, this phenomenon can be observed due to background radiation emitted from warm objects.

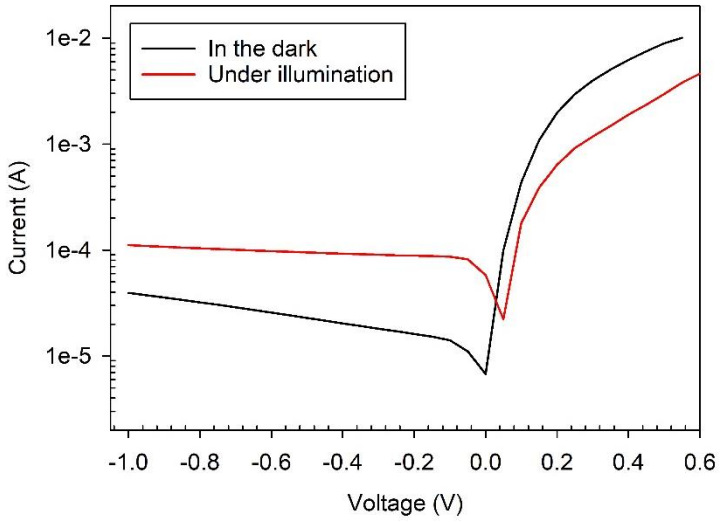

Figure 3.2 Current-voltage characteristics of a photodiode in dark and illuminated conditions

3.2 Capacitance-voltage measurement

The capacitance as a function of applied voltage can reveal information about the background doping concentration, intrinsic region width and built-in voltage of a p-i-n diode.

Room temperature C-V measurements were performed in the dark room using a probe station and a HP4275A LCR meter. The LCR meter supplies a DC bias onto the device-under-test (DUT) and superimposes an AC test signal of a known magnitude and fixed frequency (commonly ranging from 10 kHz to 10 MHz). The impedance and phase angle is then derived from the measured AC current. For accurate C-V measurements, the test signal amplitude must be kept small to ensure no significant variations in the DC bias. C-V measurements require the selection of an equivalent circuit model (parallel or series) of the DUT. Most semiconductor materials are characterised with the parallel model due to a negligible series resistance as compared to the bulk resistance in the diode. The junction capacitance of a diode is usually in the picofarad range, resulting in a small AC current signal that may be difficult to measure. To increase the signal, one can increase the oscillation frequency to reduce the reactance and subsequently increase the AC current. As most measurements are

performed on-wafer using a probe station designed for DC measurements, there are complications during high frequency characterisation which includes inadequately shielded connections, increased cable inductances and limited bandwidth (<10 MHz) of tungsten probe tip. Furthermore the lack of impedance matching from device metal contact design and cable lengths causes further challenges to obtaining accurate C-V measurements at high frequencies.

When a p-type and a n-type semiconductor is put into contact, majority holes from the p-type will diffuse to the n-type material and vice versa for majority electrons from the n-type material. The movement of carriers leaves behind immobile negatively charged acceptor ions and positively charged donor ions in the p- and n-type materials respectively, forming a region of opposite space charge (known as the depletion region) and induces a junction capacitance. From the aspect of charge neutrality at an equilibrium state, it is clear the depletion width is dependent on the doping concentration such that $N_a d_p = N_d d_n$ where N and d refers to the doping concentration and depletion width respectively while the subscripts a, p and d, n refers to the p- and n-type material respectively.

As an external bias voltage is applied, excess charges flow into/out of the p-n junction depending on the direction of applied voltage. With a forward bias, the flow of holes (electrons) into the p- (n-) type material compensates the negative (positive) charges thereby decreasing the depletion width and causing an increase in capacitance. The opposite holds true with a reverse bias voltage where the depletion width increases and the resulting capacitance decreases. For an abrupt p-n junction (as it is at the p-i or i-n interface of a p-i-n junction), most of the depletion will appear in the lightly doped side and varies as a function of the doping concentration, dielectric constant and most importantly the sum of the built-in voltage and applied bias voltage ($-V_{bias}$ for reverse voltage) as in equation 3.7.

$$W = \sqrt{\frac{2\varepsilon_s(V_{bi} - V_{bias})}{qN_b}} \tag{3.7}$$

where W is the depletion width, ε_s is the material permittivity, V_{bi} is the built-in potential, V_{bias} is the applied bias voltage, q is the elementary charge and N_b is the background doping concentration of the lightly doped material.

From the depletion width, the junction capacitance per unit area can be obtained as

$$C_d = \frac{\varepsilon_s}{W} = \sqrt{\frac{q\varepsilon_s N_b}{2(V_{bi} - V_{bias})}} \tag{3.8}$$

By taking the reciprocal squared of equation 3.8,

$$\frac{1}{C_d^2} = \frac{2(V_{bi} - V_{bias})}{q\varepsilon_s N_b} \tag{3.9}$$

A linear relation between $1/C_d^2$ versus V_{bias} is obtained where the slope is equals to $\frac{2}{q\varepsilon_s N_b}$, giving the background doping concentration and by extrapolating the term $1/C_d^2$ to 0, we can obtain V_{bi} as the x-intercept. In practice, for an accurate extrapolation, a small applied forward bias is required, however, due to large forward currents it may be difficult for to obtain accurate readings.

In a typical p-i-n diode, the capacitance falls rapidly with an initial increase of reverse bias voltage due to the low doping concentration in the intrinsic region. As the voltage bias increases, the intrinsic region eventually becomes fully depleted and the space charge region enters the n-layer. Due to the high doping concentration in the p- and n-layer, the depletion region expands more slowly, and the rate of change of capacitance per unit voltage decreases. Given a wide i-region, it can therefore be assumed that the depletion width is approximately equal to the thickness of the intrinsic region in a p^+-i-n^+ (+ superscript denotes high doping concentration) diode. The measured junction capacitance can be represented as in equation 3.10 where C is the junction capacitance, ε_0 is the permittivity in vacuum, ε_r is the relative permittivity of the semiconductor, A is the area and W is the depletion region thickness.

$$C = \frac{\varepsilon_0 \varepsilon_r A}{W} \tag{3.10}$$

As the junction capacitance is related to the bulk properties of a semiconductor wafer, the device capacitance of different sizes should scale with the device area. However, capacitances in semiconductor can be extremely small (<1 pF), reaching the measurement limit of an LCR meter and increasingly difficult for high accuracy measurements. Therefore capacitances of large device areas (>10 pF) are more reliable for further calculations and fitting purposes. By varying the doping concentrations of individual layers and intrinsic region thickness, the depletion width can be obtained to

fit the measured capacitance-voltage data. The problem is further exacerbated due to wet etch undercutting, causing a more significant percent reduction in small area devices as compared to large area devices. It is important to calibrate the LCR meter to account for the stray capacitances of the cables and probe connections. In the event that the equipment is unable to do so, the stray capacitance can be directly subtracted from the measured total capacitance. For narrow bandgap materials like InAs, the high bulk leakage current at room temperature hinders accurate reading of the relatively smaller AC current.

3.3 Photomeasurements (responsivity and gain)

To assess the optical performance of an APD, two optical measurements, namely responsivity and photomultiplication, are performed. Melles Griot He-Ne lasers were used as laser sources when the measurements were done at room temperature and a HP8168C tunable laser source was used in conjunction with a cryogenic probe station for low temperature characterisation. The room temperature experimental setup is shown in the Fig. 3.3 below. The bias voltage is provided using a Keithley 236 SMU and the optical signal is externally modulated by a mechanical chopper before falling incident onto the DUT. The output photocurrent is converted to a voltage signal by a sense resistor and the resultant photovoltage is detected by a SR830 digital lock-in amplifier (LIA).

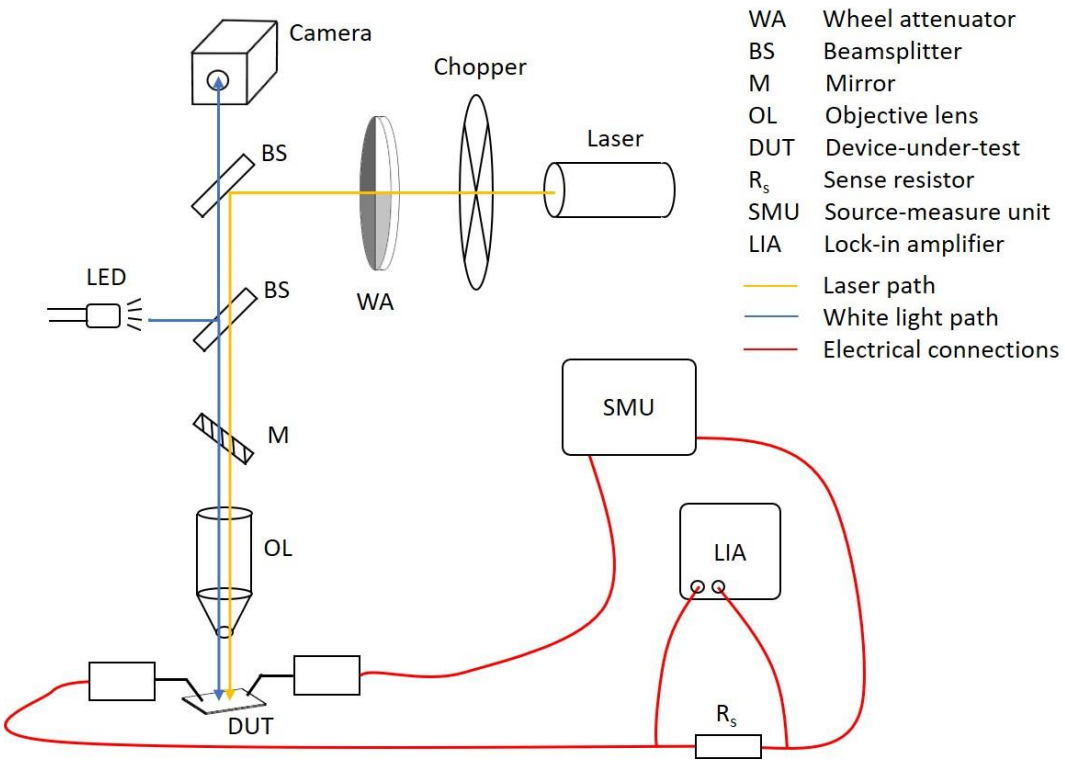

Figure 3.3 Experimental setup for gain and responsivity measurements

Responsivity is the measure of how effective a detector is at converting input light into electrical current, as in equation 3.11 where R is the responsivity, I_{ph} is the photocurrent, P_{opt} is the incident optical power. It can be related to the external quantum efficiency, η, by equation 3.12. The term R_{ideal} can be obtained from equation 3.13 where h is Planck's constant, c is the speed of light and q is the elementary charge.

$$R_{meas}(\lambda) = \frac{I_{ph}}{P_{opt}} \tag{3.11}$$

$$\eta_{ext} = \frac{R_{meas}}{R_{ideal}} \tag{3.12}$$

$$R_{ideal} = \frac{\lambda\ (in\ um)}{hc/_q} \tag{3.13}$$

The impact ionisation properties of electrons and holes can be characterised by photomultiplication measurements. Suppose a packet of photons is absorbed in the p-layer of a p-i-n diode, holes generated will be collected at the p-contact while the minority electrons are required to diffuse towards the opposite end of the diode. If no recombination occurs during diffusion to the i-layer, the electrons will be injected into

the i-layer and contribute as the primary photocurrent. While in the intrinsic region, the electrons are accelerated by the electric field. Upon gaining sufficient energy, the electrons initiate impact ionisation events and secondary carriers are created. The chain of impact ionisation events continues until all carriers exit the high field intrinsic region and contribute as photocurrent. Multiplication, or gain, of the diode is therefore given as follows where $M(V_{bias})$ is the multiplication as a function of voltage, $I_{ph}(V_{bias})$ is the multiplied photocurrent and $I_{pri}$is the primary photocurrent, assuming no impact ionisation occurs.

$$M(V_{bias}) = \frac{I_{ph}(V_{bias})}{I_{pri}} \tag{3.14}$$

In a simple p-i-n diode, the photocurrent varies with reverse bias voltage due to two changes in the electric field profile. One is the vertical increase in field strength that increases the rate of energy gain of electrons and holes, directly relating to the impact ionisation properties of the diode. And the other relates to the lateral movement of electric field (depletion width) into and beyond the cladding layers which contributes to an increased charge collection efficiency, i.e. a shorter diffusion distance is required by the carriers before arriving at the electric field. The increase in photocurrent by the latter mechanism can be approximated with a linear relationship with voltage after full depletion has been achieved [6]. Therefore, by extrapolating I_{pri} for each voltage point, the gain can be calculated by normalising the multiplied photocurrent to the primary photocurrent.

To extract the photocurrent, two techniques can be used. One simple method is by directly subtracting the dark reverse I-V curve from the reverse I-V curve under illumination. However, this method is only reliable if the photocurrent is at least two orders of magnitude larger to avoid the fluctuations of dark current affecting the accuracy of measurement. The second method relies on the use of a lock-in amplifier (LIA) to extract signals buried within the dark current and is detailed in Appendix D.

3.3.1 Multiplication measurements

For an accurate derivation of the multiplication characteristics of electrons [7], a pure injection of electrons into the high field region is required by absorbing all the light within the p-layer. This can be achieved by either growing a thick p-cladding layer or

by using a short illumination wavelength because the absorption coefficient is higher at shorter wavelengths. The same applies to pure hole injection for a n-i-p diode. Further to this, side injection of the illumination beam should be avoided to prevent the direct absorption of light in the intrinsic layer, which contaminates the intended carrier injection profile. Therefore, diodes with a photosensitive area larger than the beam diameter should be used when performing multiplication measurements. This is also important to ensure the complete absorption of incident light to obtain an accurate responsivity.

In most APD materials, thermal runaway can become an issue as dark current increases with device temperature. The rise in temperature further increases the dark currents, essentially forming a positive feedback cycle and causing eventual junction breakdown. Besides that, the ionisation characteristics of electrons and holes are temperature dependent. Therefore, it is important to verify the measurements using different optical power settings. At high injection conditions (by large optical power or at extremely high gain), an opposite electric field induced by the photogenerated minority carrier can collapse the electric field induced by the bias voltage, causing diode saturation and non-linearity.

In the presence of localised electric field hotspots due to abrupt junction geometries in ion implanted planar devices, the measured gain can appear unusually high. In a practical system, light falling onto the hot spots will produce abnormally high currents and with sufficient current, leads to catastrophic device breakdown. To ensure the reliability of measurement, the spatial uniformity of gain can be assessed.

The LIA requires a sense resistor to read the induced photovoltage. At high reverse bias and high leakage currents, the voltage drop across the sense resistor may become significant and result in an underestimation of the measured gain due to lowered voltage drop across the DUT. To prevent this, a resistor with an appropriate value should be used while maintaining a good signal to noise ratio for LIA measurements.

3.4 Temperature dependence (300K – 77K) studies

Since the electrical and optical properties of an APD show varying extents of temperature dependence, characterisation at different temperature can provide more information about the APD material. The temperature dependence studies in this thesis

are conducted with a Model ST-500 continuous flow cryogenic probe station with liquid nitrogen source by Janis Research Company, LLC. The cryostat system has four micromanipulator probe arms for two DC probes, a single mode fibre and a multi-mode fibre. Upon sample loading, the chamber is evacuated to a pressure in the range of 1e-5 mbar using a turbopump then cooled by liquid nitrogen. The rate of cooling is determined by the flow rate of liquid nitrogen and the sample temperature is controlled by a PID temperature controller and heater stage system. To ensure the accuracy of temperature reading at device level, the temperature reading should be allowed half an hour to stabilise.

The temperature dependence of dark current can be fitted with the Arrhenius equation as in equation 3.15 where I_d is the dark current, ∀ is a pre-exponential factor, E_A is the activation energy, k_b is Boltzmann's constant and T is the temperature. By taking the natural logarithm, a linear plot between $\ln I$ vs $^1/_T$ can be obtained where E_A can be determined.

$$I = \forall \exp\left(-\frac{E_A}{k_b T}\right) \tag{3.15}$$

The value of activation energy reflects on the dominant mechanism of action. In an APD prior to the onset of tunnelling and multiplication, the competing bulk current mechanisms are the diffusion current and G-R current (equation 3.3 and 3.4 respectively). It is evident that the former is proportional to n_i^2 while the latter is proportional to n_i. And the intrinsic carrier concentration of a semiconductor material has an inverse exponential relation to temperature as seen in equation 3.16 below. Therefore, for an activation energy close to E_g, the dominant leakage current mechanism is the diffusion current, whereas an activation energy close to $^{E_g}/_2$ suggests the presence of mid gap trap levels.

$$n_i \propto \exp\left(-\frac{E_g}{2k_b T}\right) \tag{3.16}$$

To refine the analysis, the bulk and surface current components can be extracted as in equation 3.6 for each temperature point and the Arrhenius plot of the bulk component can reveal more accurate activation energies without contamination of surface current effects.

The temperature dependence of tunnelling current is derived from the band gap which follows Varhsni's law [8]. Fig. 3.4 illustrates the temperature dependence of tunnelling current of InAs p-i-n diodes with a 2 and 3 µm intrinsic region thickness. It is clear that lowering the electric field by a wider intrinsic region has more impact in suppressing the tunnelling current than raising the band gap by reducing the temperature in a narrow band gap material.

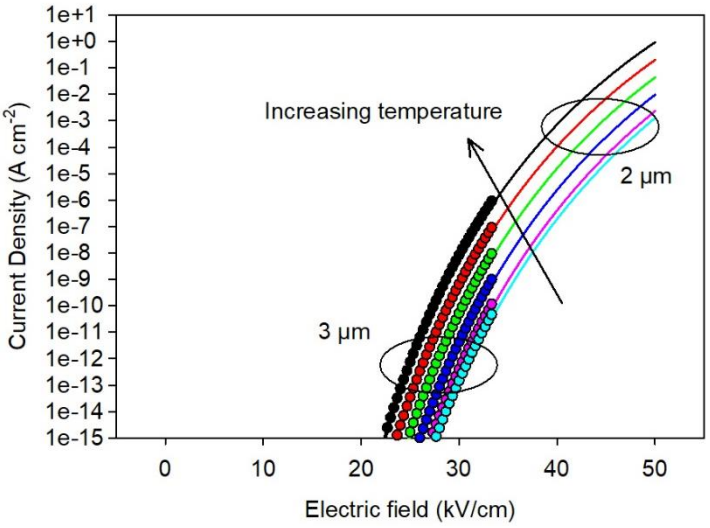

Figure 3.4 Tunnelling current as a function of temperature from 300 to 77 K

Carrier scattering mechanisms such as lattice and impurity scattering are temperature dependent where scattering rates typically decrease with temperature. Therefore electron and hole ionisation coefficients have an inversely proportional relationship with temperature. This can be interpreted as follows, carriers gain energy under an electric field and lose energy during collisions with the atomic lattice or impurities; by decreasing the rate of energy loss, carriers are able to obtain sufficient energy for impact ionisation with more ease and impact ionise. However, it must be known that the band gap increases as temperature decreases, which brings about an increase in the threshold energy for impact ionisation. In most semiconductor materials, the ionisation coefficients increases with reduced temperature, benefiting more from the decreased scattering than the larger threshold energy required for impact ionisation. As a result from the larger ionisation coefficients at low temperature, the onset of multiplication is earlier and breakdown occurs at a lower voltage [9], [10]. In InAs, however, it has been observed that the electron ionisation coefficient has a positive temperature coefficient. The rate of change of breakdown voltage as a function of temperature is

known as the temperature coefficient of breakdown. An APD material with a small temperature coefficient of breakdown is desirable for gain stability. For a p-i-n configuration diode, a small temperature coefficient of breakdown can be artificially induced using a thin intrinsic region as the change in ionisation coefficients at high electric fields is less noticeable.

3.4.1 Low light level measurements

For extremely small optical signals, the APD by itself may not provide sufficient signal amplification so an external transimpedance amplifier (TIA) is utilised to increase the signal strength. The noise floor is therefore determined by the combined APD and TIA noise. It can be difficult to distinguish the signal from the noise by time-varying measurement techniques such as using an oscilloscope if the overall broadband noise amplitude is dominant. In such cases, it may be advantageous to instead analyse the signal in the frequency spectrum. This can be done using a Fast Fourier Transform (FFT) spectrum analyser.

Broadband white noise sources such as diode shot noise and resistor Johnson noise are then represented by individual peaks at different frequencies and the signal, if modulated, will appear only at the modulation frequency (and the integer multiples of said frequency). Much like a lock-in amplifier, by observing particular operating frequencies of interests, the actual signal can be differentiated from the noise using a spectrum analyser. However, a spectrum analyser offers an additional benefit in that the noise at various frequencies (noise floor) can be clearly displayed along with the signal peak. The analog input signal is discretised by first sampling at a frequency at least twice the highest frequency component present in the signal by Nyquist's theorem [11] and then converted to the frequency domain by taking the discrete Fourier transform (DFT). Fast Fourier transform refers to an implementation of the DFT that is widely used in digital signal processing for its speed. To prevent aliasing effects, an anti-aliasing filter is implemented before the sampling circuitry to heavily attenuate all signals above a certain frequency.

Assume a spectrum analyser has a sampling frequency of 256 kHz and takes 1024 points to discretise a time domain signal, the total time needed to sample the spectrum, i.e. the time record, would be 4 ms (1024 points divided by 256 kHz). Due to Nyquist's theorem, there are only 512 frequency points (half the frequency samples

as there would be for time samples). The frequency range starts at 0 Hz and increases to the highest frequency component of 128 kHz (half the sampling frequency). The frequency resolution between each frequency bin is 250 Hz (from 128 kHz divided by 512 points) which is the reciprocal of the time record. Suppose a 400 Hz signal is detected, the spectrum analyser will place part of the signal in the 250 Hz bin and part in the 500 Hz bin. Instead of changing the sampling rate or increasing the number of samples taken, the time record can be increased to reduce the frequency resolution, thereby increasing the measurement time. The frequency range can be offset by multiplying the frequency spectrum with a sine wave to shift the spectrum by the frequency of the sine wave in a process known as heterodyning. By changing the span and shifting the frequency range, any signal frequency of interest can be analysed.

Fig. 3.5 shows the connection of the measurement set-up using the Janis low temperature probe station to cool and reduce the APD noise, a SR570 low-noise current pre-amplifier and a SR760 FFT spectrum analyser. The modulated input light from a HP8168C tunable laser source is coupled into the APD by the single mode fibre on the probe station. The APD current including the fixed-frequency photocurrent produced and the inherent noise are amplified before displayed on the FFT spectrum analyser. The pre-amplifier operation should be selected with care to obtain a desired sensitivity (amplification) with sufficient bandwidth and low input noise level. The FFT spectrum analyser can be set to display the frequency data of a specific range by adjusting the span and centre frequency. The magnitude (vertical axis) can be displayed in units of *Volts* or *dBVolts* and the power spectral density, i.e. the signal magnitude normalised to a 1 Hz bandwidth, can be selected. Averaging can be enabled (and the number of averages can be selected) to obtain a smoother noise floor. The photocurrent produced in the APD will be displayed at a frequency set by the internal modulation frequency of the laser.

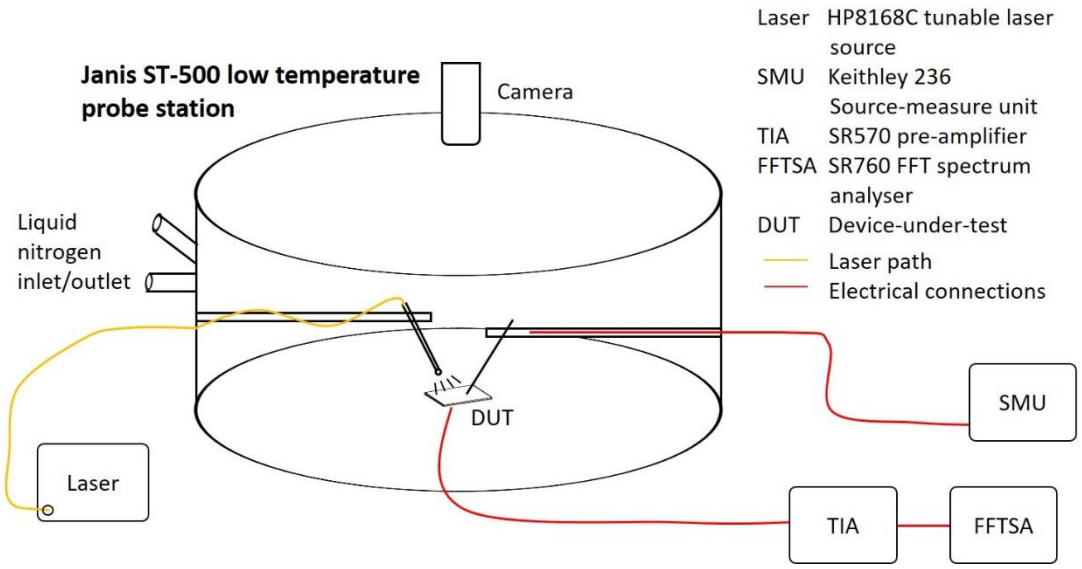

Figure 3.5 Experimental setup using a liquid nitrogen cooled Janis probe station for temperature dependence and low signal measurements

3.5 Secondary Ion Mass Spectroscopy

Secondary ion mass spectroscopy (SIMS) is a tool to analyse materials down to its atomic, isotropic or molecular composition. This is done by sputtering the sample surface with a primary ion beam of few keV in energy and detecting the secondary ions released due to the ion bombardment under a high vacuum. The common primary ions used are oxygen and caesium ions to investigate positive and negative ions, respectively. The detection of secondary ions is performed via a mass analyser to distinguish between the sputtered ions and a detector that generates electrical current when hit by the secondary ions. The secondary ions are subjected to a combination of electric field and magnetic field of known magnitudes to accelerate and to alter the ion paths. Only ions with a specific trajectory (depending on the deflection of ions due to the effects of the electromagnetic field on the ionic mass and charge) will be able pass through the detector aperture. Ions incident onto the detector produces an electric current due to the neutralisation of the ionic charge and the magnitude of generated current is proportional to the quantity of ions. An illustration of the basic components of a SIMS system [12] is shown in Fig. 3.6.

The SIMS technique is destructive only for a small area on the sample and provides knowledge about the material composition, giving accurate information about the layer widths and also doping concentrations across the entire sample depth. There are also

downsides and complications to SIMS analysis mainly due to the reactions between the primary ions and sample surface under favourable conditions such as the formation of oxides when oxygen primary ions are used, mass interference between ions and molecules that have identical masses, signal contamination of ions with similar mass-to-charge ratio, chamber contamination and also charging effects that modify the surface chemistry.

For semiconductor analysis, a reference beam, commonly one of the elements of the host semiconductor material, is also tracked concurrently to determine the layer investigated and also to define the layer interfaces as different materials have varying erosion rate which complicates the depth profiling. The doping concentration is obtained by calibrating the electrical signal to a reference sample of a known concentration and the depth profile is obtained by measuring the crater depth using a profilometer assuming a constant erosion rate. SIMS results presented in this thesis are carried out by Loughborough Surface Analysis Ltd, with a Cameca IMS-4f.

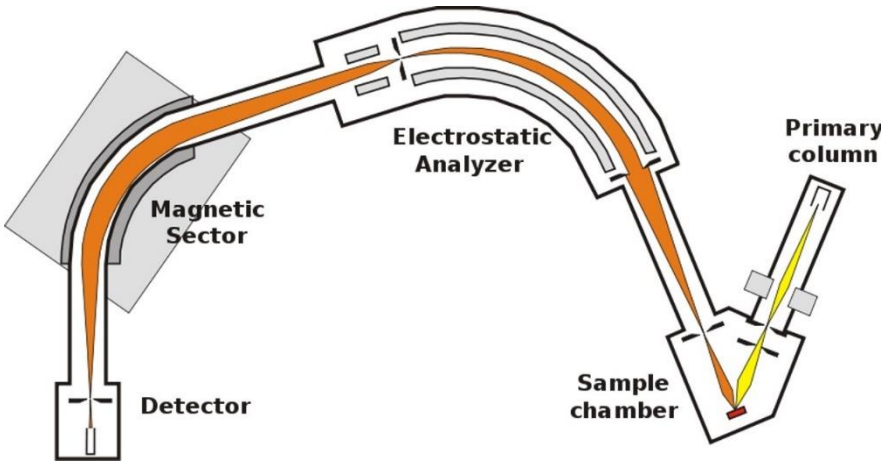

Figure 3.6 Typical components in a SIMS instrument [12]. The primary ion path is denoted by the yellow areas while the path in orange represents the trajectory of secondary sputtered ions. The ions of interest of a specific charge and mass are isolated before the detector by an applied electric field and magnetic field.

3.6 References

[1] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 3rd ed. John Wiley & Sons, Inc., 2007.

[2] S. R. Forrest, F. Leheny, R. E. Nahory, and M. A. Pollack, 'In_0.53Ga_0.47As photodiodes with dark current limited by generation-recombination and tunneling', *Appl. Phys. Lett.*, vol. 37, p. 322, 1980.

[3] L. Esaki and Y. Miyahara, 'A new device using the tunneling process in narrow pn junctions', *Solid-State Electron.*, vol. 1, no. 1, pp. 13–21, 1960.

[4] E. O. Kane, 'Zener Tunneling in Semiconductors', *J. Phys. Chem. Solids*, vol. 12, no. 2, pp. 181–188, 1960.

[5] D. K. Roy, *Quantum Mechanical Tunnelling And Its Applications*. World Scientific Publishing Co. Pte. Ltd., 1986.

[6] M. H. Woods, W. C. Johnson, and M. A. Lampert, 'Use of a Schottky barrier to measure impact ionization coefficients in semiconductors', *Solid-State Electron.*, vol. 16, pp. 381–394, 1973.

[7] G. E. Stillman and C. M. Wolfe, 'Avalanche photodiodes', in *Semiconductors and semimetals*, vol. 12, Elsevier, 1977, pp. 291–393.

[8] Z. M. Fang, K. Y. Ma, D. H. Jaw, R. M. Cohen, and G. B. Stringfellow, 'Photoluminescence of InSb, InAs, and InAsSb grown by organometallic vapor phase epitaxy', *J. Appl. Phys.*, vol. 67, no. 11, pp. 7034–7039, Jun. 1990, doi: 10.1063/1.345050.

[9] C. H. Tan, G. J. Rees, P. A. Houston, J. S. Ng, W. K. Ng, and J. P. R. David, 'Temperature dependence of electron impact ionization in In0.53Ga0.47As', p. 4.

[10] I. C. Sandall, J. S. Ng, S. Xie, P. J. Ker, and C. H. Tan, 'Temperature dependence of impact ionization in InAs', *Opt. Express*, vol. 21, no. 7, p. 8630, Apr. 2013, doi: 10.1364/OE.21.008630.

[11] H. Nyquistt, 'Certain topics in telegraph transmission theory', *Trans. Am. Inst. Electr. Eng.*, vol. 47, no. 2, pp. 617–644, 1928.

[12] 'Sensitive high-resolution ion microprobe'. https://en.wikipedia.org/wiki/Sensitive_high-resolution_ion_microprobe (accessed Feb. 23, 2020).

Chapter 4 Planar InAs photodiodes by 34 keV Be-ion implantation

The bulk of past work has been focused on obtaining low leakage dark currents in InAs APDs as the dark current directly determines the noise floor of the system. SU-8 negative photoresist was found to work as a passivation layer for mesa topology InAs [1] and APDs with low leakage current operating at high gain level have been produced successfully [2]. With the most recent achievement being the detection of down to 15 photons at 1550 nm wavelength using InAs APD at 77 K operating in conjunction with a transimpedance amplifier [3]. Despite the best efforts in optimising the passivation scheme, surface leakage at low temperatures and eventual device failure from temperature cycling remains a limiting factor to mesa InAs APD operation.

In pursuit of improvements to diode performance, planar diodes developed in recent works show promise in simplifying fabrication procedures and providing superior diode characteristics [4]. From published reports on other more mature photodiode materials, planar designs demonstrate outstanding performances in life tests and high temperature stress tests [5], [6]. In real world applications such as undersea fibre communications systems or space applications, the long term reliability and stability down to component level becomes a major concern [7], [8].

A relatively low energy Be-ion implantation at 34 keV (in comparison to previous work using a double implant scheme of 70 and 200 keV) is used to create the p-type region in InAs. The hypothesis is that the implant-induced damage due to low energy implantation will be comparatively less than the higher implant energies used in [9]. The estimated junction depth from SRIM simulations with a 34 keV implantation energy is approximately 100 nm. To achieve a thicker p-type region (for a carrier injection profile to be closer to that of pure electron), long annealing durations are utilised to attempt to promote Be dopant diffusion into the bulk material in this work. Diffusion of Be dopants has been reported in delta-doped GaAs where a drop in peak concentration and broadening of dopant distribution is observed after annealing at 800 °C for 4 hours [10]. In a separate work, the peak concentration drops almost an order magnitude and the peak broadens from 34 to 440 Å as the annealing temperature is raised from 600 to 1000 °C for an annealing duration of 5 seconds [11]. McLevige

et al. reported diffusion of Be ions to a depth of 2 μm when annealed at 900 °C for 60 minutes from a projected range of 0.8 μm, in Be-implanted GaAs [12].

In this chapter, an initial optimisation of annealing time is tested on blanket implanted samples (i.e. ion implantation carried out without photoresist mask) which are fabricated into mesa type diodes. The current-voltage characteristics and responsivity were assessed. The dopant depth distribution were investigated by SIMS. The optimal annealing duration was subsequently applied onto planar samples. On these planar diodes, the spatial uniformity of responsivity and diode isolation were studied alongside standard I-V and responsivity measurements. Finally, different surface treatment methods were attempted to improve the diode performance. Most results discussed in this chapter are published in [13].

4.1 Fabrication of planar InAs diodes

Results reported in this chapter are produced with a MOVPE grown InAs wafer with a 7 μm i-layer and 1 μm n-layer grown on a (001) n-type substrate. The wafer was grown by Dr. Andrey Krysa from the National Epitaxy Facility in Sheffield.

In general, the samples were first prepared with a 3-stage solvent clean, followed by the deposition of a 35 nm silicon dioxide layer at 300 °C via PECVD. The dielectric layer serves as an encapsulating layer to protect the InAs surface from damage induced from sample processing as well as to prevent the outgassing of As atoms during the annealing process [14]–[16].

The ion implantation process is carried out by Cutting Edge Ions, LLC with an implantation energy of 34 keV at room temperature and a dosage of 2×10^{14} cm^{-2} with the sample tilted 7° against the incident ion beam to prevent channelling effects. The sample is then furnace or RTA annealed at 500°C. The encapsulating dielectric is removed using a buffered hydrofluoric acid solution (HF) and standard photolithography techniques are used to pattern the top contact metals. 20/200 nm of Ti/Au are used as the top and bottom metal contacts. The diodes are finally passivated with SU-8 to preserve the surface conditions.

The annealing temperature of 500 °C was chosen based on annealing trials performed previously by Ben White [9] which was found to give diode rectification characteristics. A high temperature anneal is required to not only electrically activate

the implanted dopant (by substituting the host atoms), but also to remove the damage sustained by the crystal lattice during the energetic implant process [17]. An annealing temperature that is too high, while in theory should provide sufficient thermal energy to rearrange the damaged lattice, causes other issues in compound semiconductors such as loss of stoichiometry due to differences in vapour pressure of the constituent elements, migration and subsequent nucleation of intrinsic point defects and the formation of extended defects such as dislocation loops [18].

The following results can be split into three distinct sections where the first is the optimisation of post-implant annealing procedures on mesa diodes fabricated from blanket implanted wafers; the second where the appropriate anneal cycle is used to produce planar InAs diodes and the third, where various surface treatment methods were tested to improve the planar diode characteristics.

4.2 Blanket Be-ion implanted mesa InAs diodes

To assess the effects of annealing duration on the diffusion of Be dopants and subsequent diode characteristics, a piece of InAs sample is blanket implanted with Be ions at the aforementioned energy and dosage. The sample is cleaved into 4 smaller pieces where three pieces are furnace annealed at 500°C for 15, 30 and 60 minutes while the last is kept as an unannealed control sample. The samples are then processed using a standard mask set that produces mesa diodes of 420, 220, 120, 70 μm in diameter using the standard InAs wet etch recipe.

The room temperature J-V characteristics of each sample is shown in Fig. 4.1 (left). Though all samples show clear bulk dominated current-voltage characteristics, only the annealed samples display diode rectification while the reference unannealed sample is symmetrical across the y-axis. Using J-Vs from nominally 220 μm diameter diodes as a comparison, the dark current densities measured at -0.2 V are 1.01, 1.06 and 1.41 Acm^{-2} for the 15, 30 and 60 minutes annealed samples, respectively. The results are unsurprising as ion implanted dopants generally require thermal energy from a high temperature anneal process to substitute the original atom in the lattice site, thereby electrically activating the dopant.

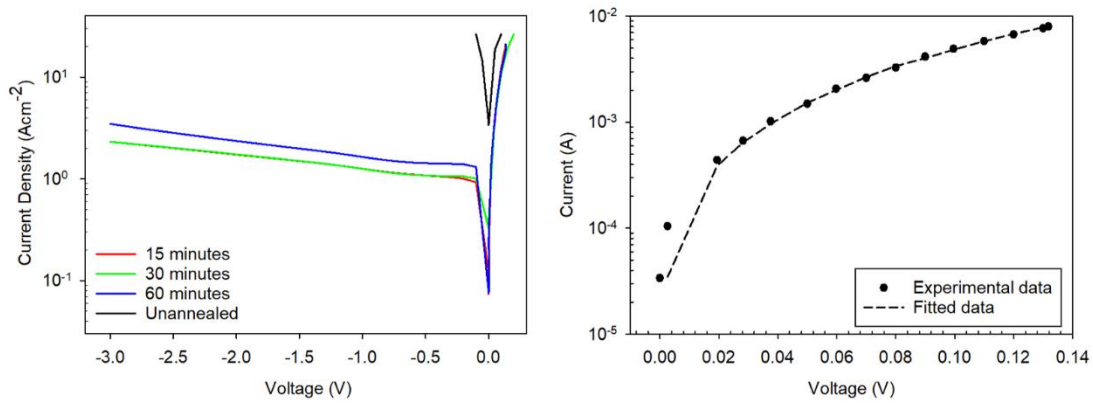

Figure 4.1 Current density-voltage characteristics at room temperature of samples annealed at 500°C for different durations of 15, 30, 60 minutes and a control unannealed sample. (left) Forward current-voltage fitting to ideal Shockley diode equation of a 220 μm diameter device from the 500°C, 15 minutes annealed sample. An ideality factor 1.14 and a series resistance of 6.3 Ω is obtained. (right)

The forward current-voltage properties of the 3 annealed samples show near-identical characteristics. By fitting the forward curves to the ideal Shockley diode equation as shown in Fig. 4.1 (right), an ideality factor of 1.14 and a series resistance of 6.3 Ω is obtained, suggesting that the room temperature forward current is dominated by the majority carrier diffusion process and good quality metal-semiconductor junctions are formed. There are little discrepancies between the 3 samples despite the difference in annealing times, verifying that the fabrication process for each sample was consistent and did not contribute an external factor in our analysis.

The diode responsivity measured at -0.2 V using an illumination wavelength of 1520 nm are 0.77, 0.71, 0.75 A/W for the 15, 30 and 60 minutes annealed sample respectively, corresponding to external quantum efficiencies of 62.8, 57.9 and 61.2 % as shown in Table 4-I. The external quantum efficiencies obtained from these diodes are comparable to published mesa InAs APDs [19]. This is not surprising considering that absorption of 1520 nm wavelength light as the combined layer thickness of 8 μm will absorb up to 99% of the light. The absorption profiles of incident light of 543, 633, 1520 nm wavelength are illustrated in Fig. 4.2. The absorption coefficients used are 2.28×10^5, 1.2×10^5, and 1.1×10^4 cm^{-1} for the respective wavelengths, obtained from [20].

Table 4-I Responsivity and external quantum efficiency of diodes from samples of different annealing duration

Annealing duration of sample (mins)	**Responsivity (A/W)**	**External quantum efficiency (%)**
15	0.77	62.8
30	0.71	57.9
60	0.75	61.2

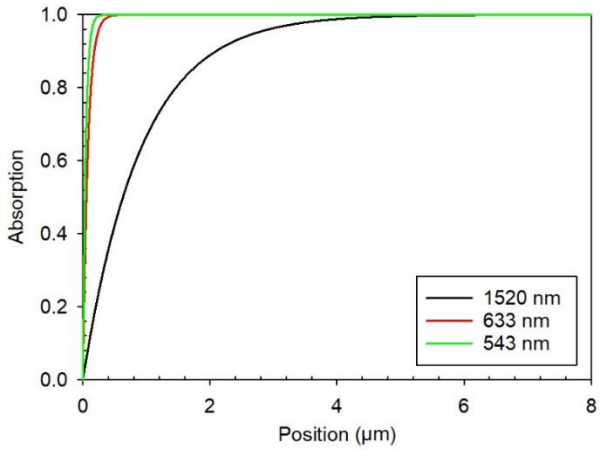

Figure 4.2 Absorption profile of different wavelengths of light on InAs

4.3 Dopant profile by SIMS

The Be doping concentration versus sample depth of all samples studied by the SIMS technique is shown in Fig. 4.3. From Fig. 4.3, samples of different annealing duration show similar levels of doping concentration across all depths analysed which suggests an inherent limit to the diffusion of Be dopants in InAs at the temperature used regardless of the annealing duration. Slight discrepancies between the simulated profile obtained from SRIM and the unannealed sample can be due to several reasons such as the difference in thickness of screening oxide as deposited and as simulated, calibration errors introduced during SIMS analysis and the accuracy of SRIM simulation parameters.

Comparing the unannealed and annealed samples, there is a drop in peak level as well as shifting of the overall curve to the left, which suggests that there is a significant decrease of Be dopants after annealing near the sample surface. Integrating under the SIMS curves gives an area 44% that is smaller in the 15 minutes annealed sample as

compared to the unannealed sample. Implanted Be dopants in GaAs crystals with high temperature anneals have been observed to display significant out-diffusion towards the surface from SIMS measurements [18], [21]. In Pearton's study of implanted Be dopants in GaAs [18], a capless annealing at 1000 °C for 3 s produced a peak concentration roughly a factor of 2 lower than the unannealed sample with little to no diffusion towards the bulk while obtaining an electrical activation >95% for the remaining Be dopants. The loss of Be ions was attributed to a gettering effect due to surface defects and damage. McLevige *et al.* [21] demonstrated that the implanted Be dopants in GaAs, after annealing at 900 °C for 30 minutes, out-diffuses into the silicon nitride encapsulant and this effect is dependent on implant dose as well as the peak dopant concentration.

While the annealing temperatures used are higher (in the range of 600 to 1000 °C) in the referenced works as compared to this work, there may be a difference in the dissociation threshold of Be dopants in InAs and GaAs crystal lattices. From the works by Pearton *et al.* on investigating the effects of implant damages in various III-V materials including InAs, it was found that implanted Mg post-RTA (annealing temperatures of 500 °C onwards) shows an increase in concentration closer to the surface, indicating significant dopant out-diffusion [22].

There are noticeable differences in the signal tail after annealing where the tail levels are slightly higher than that of the unannealed sample. Evidence suggests that implanted Be dopants show very little diffusion into bulk GaAs [21]. However, the SIMS measurements as seen in Fig. 4.3 has reached the detection limit at the mid $\times 10^{16}$ cm^{-3} level therefore it is difficult to ascertain if the tail level is indeed due to Be diffusion or simply measurement noise. A positive note to take away from this set of data is that there is indeed little difference in the p-type region thickness and doping concentration between samples annealed for 15, 30 and 60 minutes, supporting the observations made from the current-voltage and responsivity measurements. The differences between samples of different anneal duration are marginal, therefore a 15 minutes anneal is sufficient for subsequent processing.

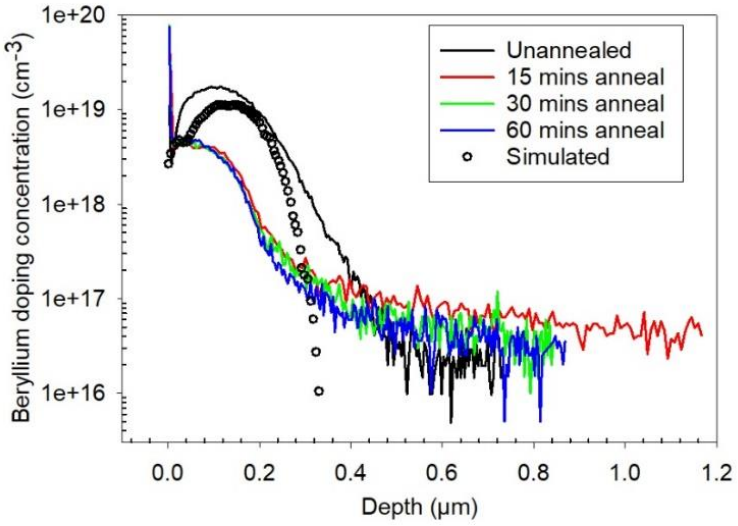

Figure 4.3 Beryllium dopant concentration vs. depth of samples annealed for different durations. The simulation results using a 34 keV Be-ion energy is included.

4.4 Be-ion implanted planar InAs diodes

Following the investigation for an optimal annealing condition, a 15 minutes RTA is applied to the samples patterned with implantation windows to produce planar InAs diodes using a mask set designed by Dr Benjamin White as shown in the Fig. 4.4 [9]. In addition to the thin encapsulating dielectric, a 4 μm thick layer of SPR220 positive photoresist was used as a masking layer to prevent penetration of Be ions into unintended areas. The design details of the mask are illustrated in Fig. 4.4. Diodes of diameters 400, 200, 100 and 50 μm are available for current density-voltage comparison. Guard ring designs are also incorporated into 200 and 50 μm diameter diodes. An example of the device cross-sectional view is shown in Fig. 4.9.

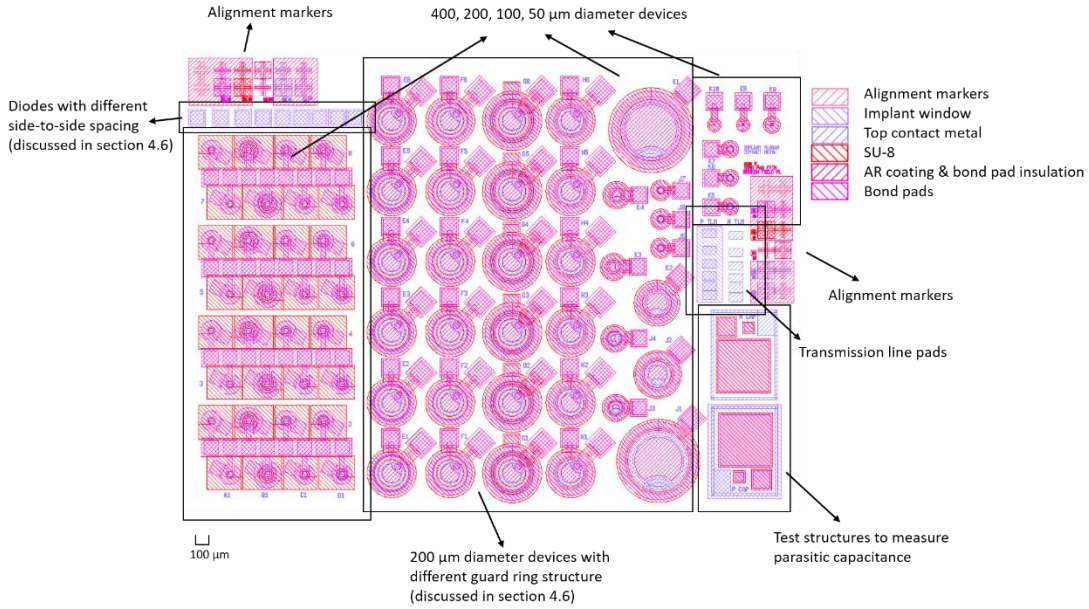

Figure 4.4 Mask set used to produce planar InAs diodes with device sizes of 400, 200 and 100 µm diameter

Similar analyses in terms of I-V and responsivity were conducted on the planar diodes. It can be observed in Fig. 4.5 that the current scales more closely with area than with perimeter, showing that the bulk characteristics are again, dominant. The ideality factor and series resistance extracted from the forward I-V curves are 1.42 and 4.1 Ω respectively, suggesting that it is a mix between diffusion and generation-recombination currents in the forward regime of the planar diodes. The measured responsivity at -0.2 V with 1520 nm wavelength of light is 0.49 A/W.

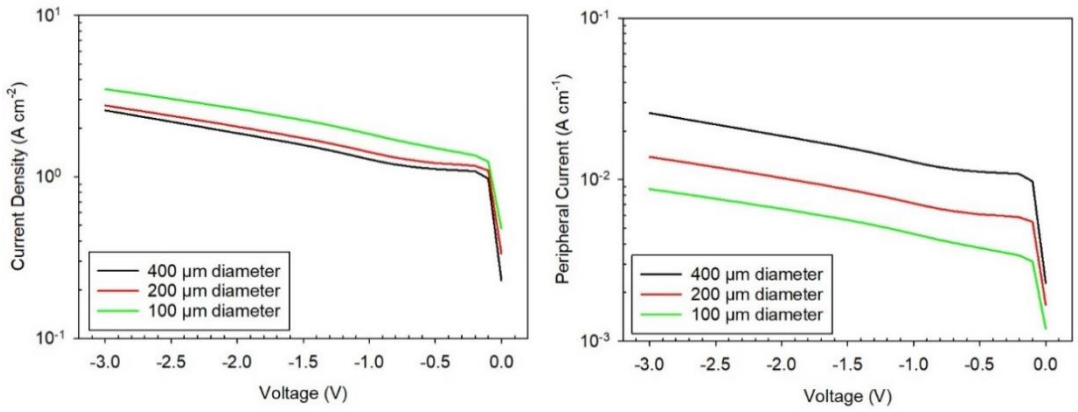

Figure 4.5 Current density (left) and peripheral current (right) versus voltage for planar InAs diodes of different sizes at room temperature

4.5 Spatial uniformity of planar InAs photodiode

The spatial responsivity map at room temperature of a 400 μm diameter diode is obtained by raster-scanning a probed device using a motorised micromanipulator stage with an illumination wavelength of 633 nm as shown in Fig. 4.6. The laser spot size is roughly 80 μm, hence the measurement is performed only using the largest diameter devices. The largest responsivity comes from areas nearest to the metal contacts and an area close to the centre of the optical window sees a 20% drop in responsivity. The poor responsivity in the blue regions are due to light blocking by the probe tip and metal contact. While the exact reason of this non-uniformity is unclear, there are several possible explanations.

One is the incomplete or perhaps, sporadic activation of Be dopants of the diode post annealing [23]. This might cause differences in p-type doping concentration across the diode and different recombination rates. In GaN-based light emitting diodes, current crowding where current flow is congregated near the metal edges, is an issue that limits the uniformity of light extraction across the active diode area. This is often explained to be an artefact of the low carrier mobility and poor conductivity across the topmost layer in GaN LEDs [24]. In Be-implanted GaAs and InP, a substantial increase in Be activation can be achieved by increasing the annealing temperature up to 750 °C [25], [26]. The differences between these published results from [9] could be due to extended defect formation when annealing InAs at temperatures >550 °C.

Another possible explanation is the shunting effect in narrow band gap photodiodes [27]. When connected to an external load (e.g. a read-out integrated circuit to extract the optical signal information), a photodiode can be represented as a current source (magnitude dependent on the optical signal), having a shunt resistance in parallel with the source and a series resistance in a separate branch in series with the load. When the series resistance is negligible in comparison to the shunt resistance, photocurrent generated can be collected through the series resistance path at the metal contacts. However, narrow band gap materials generally have small shunt resistances at room temperature, comparable to their series resistances, such that a portion of

carriers generated will go through the shunt path instead, leading to a decrease in the collected photocurrent.

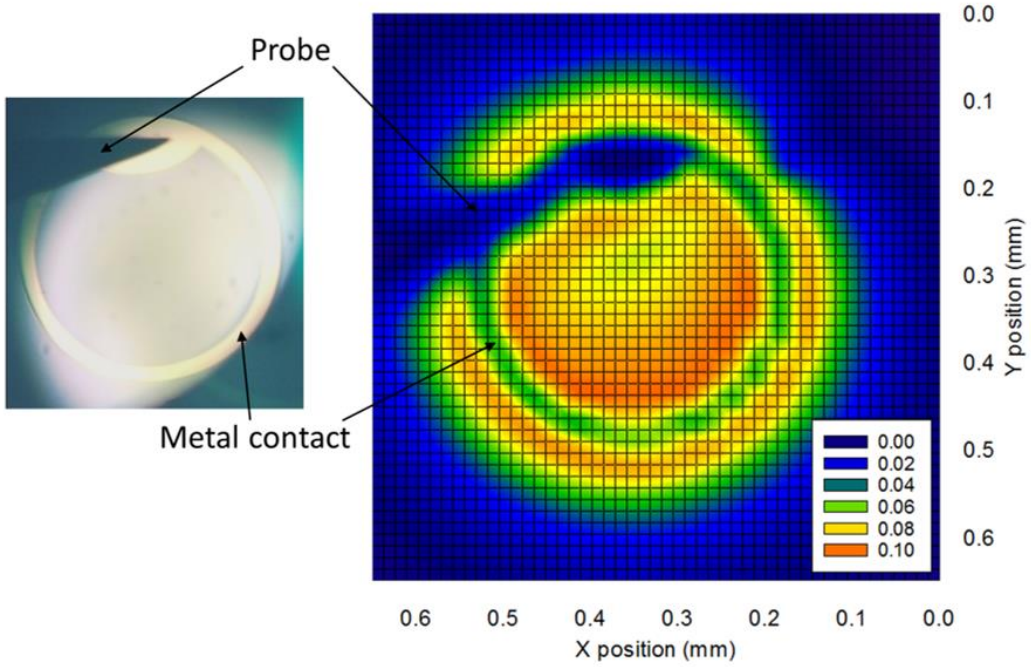

Figure 4.6 Spatial variation of responsivity at -0.1 V at room temperature using an illumination wavelength of 633 nm on a 400 μm diameter diode

Fig. 4.7 (left) shows the comparison of spatial uniformity of responsivity between commercial InAs photodiodes as well as diodes from this work, included in the figure is also an example from a standard MOVPE grown p-i-n InAs mesa diode. The Judson photodiodes [28] test wavelength was not specified while the Hamamatsu photodiodes [29] were tested at 1550 nm and the in-house InAs diodes were tested at 633 nm. It can be observed that non-uniformity is an issue faced even in commercial InAs photodiodes and the MOVPE grown mesa InAs diodes on the other hand, show superior performance in this aspect. This could be caused by the combination of reasons as explained above.

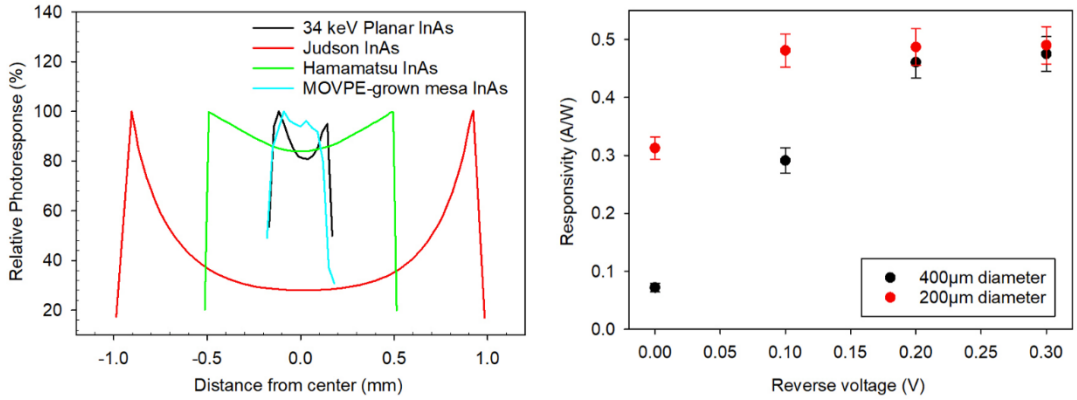

Figure 4.7 Comparison of normalised spatial variation in photoresponse across the optical window of commercial, in-house mesa and planar (this work) InAs photodiodes. (left) Responsivity at 1520 nm as a function of reverse bias with increments of 0.1 V. Error bars displayed are the standard deviation of the experiment. (right)

With reference to Fig. 4.7 (right), where the responsivity versus voltage of 400 and 200 µm diameter diodes at 1520 nm wavelength are plotted, it can be observed that the responsivity increases gradually as the voltage rises from 0 to -0.3 V. Typically, the increase in photoresponse in a p-i-n diode is attributed to the manifestation of additional carriers by impact ionisation or the increased charge collection efficiency from the expansion of the depletion region due to the applied reverse bias. The former is considered negligible at biases less than -0.5 V in InAs and the latter while probable, does not account for the difference in percent increase seen in the 400 µm diameter diodes and the 200 µm diameter diodes. An explanation offered is the increase in lateral charge collection efficiency. This observation lends credence to the shunt resistance hypotheses made regarding the drop in photoresponse as the diode shunt resistance is inversely proportional to the diode area [30]. These findings suggest that the design for large area photodiodes will require further optimisations. One approach to increase the charge collection can be done by adopting interdigitated finger designs from metal-semiconductor-metal photodetectors [31] or from solar cell devices [32] for more efficient collection of photogenerated carriers.

4.6 Lateral diffusion of Be dopants due to long annealing duration

With a planar diode design, the resistivity of the intrinsic layer plays an important role in providing isolation between adjacent diodes. For imaging arrays where it is ideal to pack the largest possible number of pixels into the least amount of space for maximum

fill factor, the pixel pitch and therefore the pixel-to-pixel isolation becomes a critical parameter. The diffusion of Be dopants in the crystal lattice during the annealing process occurs in all directions with no known data on the diffusion of Be in InAs. With a significant amount of Be dopants moving outwards of the implantation window, the effective diode area would increase and, in an array, would result in the interconnection between adjacent pixels, creating a large area diode instead of a diode array.

To investigate the extent of electrical isolation between diodes, a series of diodes with varying separation distances between adjacent diodes is fabricated. The I-Vs of the array of diodes are shown in Fig. 4.8 along with the schematic of the array. In general, as the gap between diodes increases, the dark current decreases. With a separation distance of less than 7.5 μm as in from diodes S1 to S3, the dark current suggests there is partial or no isolation between these diodes. As the separation distance increases, the dark current levels drop and reaches a consistent level beyond a gap of 15 μm whereby diodes S6 to S9 have similar dark current levels. Upon scrutiny, diodes S1 to S3 have dark currents larger than that of diode S9 which does suggest that diodes S1 to S3 are interconnected and the effective area have increased.

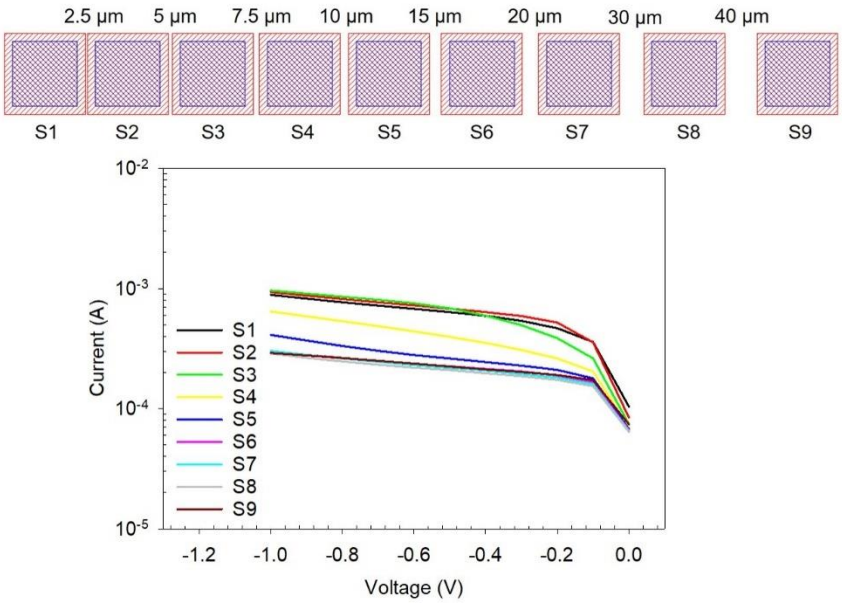

Figure 4.8 Variation in separation distance and the current-voltage characteristics at room temperature of a series of 9 adjacent diodes. Schematic of the array is shown and the dimensions for the square diode are 100 μm by 100 μm.

The findings above are in part supported by the increased dark currents in diodes with guard ring designs. While guard rings in planar APDs are intended for the mitigation of localised electric field hotspot formation by spreading the electric field laterally, the inclusion of guard rings would inevitably result in an increased diode area as well. Lateral diffusion of dopants can be observed especially in fast-diffusing ions such as Zn where lateral diffusions of up to 20 times the junction depth [33]. However there is a lack of data available on the lateral diffusion characteristics of implanted Be dopants in III-V semiconductors with only preliminary findings in GaAs showing minimal lateral diffusion [34], [35]. It is difficult to then rule out the possibility of lateral diffusion of Be dopants in InAs which may be one reason to the increase in diode area or another might be the poor confinement of lateral electric fields in undoped InAs layers.

A schematic of the 200 μm diameter diodes with various guard ring designs is shown in Fig. 4.9. Since the guard rings are only 6 μm distance away from the diode, it is possible that the effective diode areas are increased. Table 4-II lists the corrected diameters of the 200 μm diameter diodes having considered the addition of guard rings and Fig. 4.10 shows the dark current density comparison between the different designs. The current density plots of the diodes show a closer bunch after correcting the diameter as compared to considering the diodes to all be nominally 200 μm in diameter, which suggests that current guard ring designs are unoptimised and the increase of diode size is unavoidable. While it is currently difficult to pinpoint if the increased dark currents are due to the poor isolation of the intrinsic InAs, the diffusion of dopants increasing the effective area or perhaps a combination of both factors, it is clear that a minimum spacing of at least 15 μm between adjacent diodes will be required in the design of a linear array of planar InAs diodes. Guard rings have been shown to have little effect in the breakdown voltage in planar InAs APDs [9] and therefore may require more optimisation.

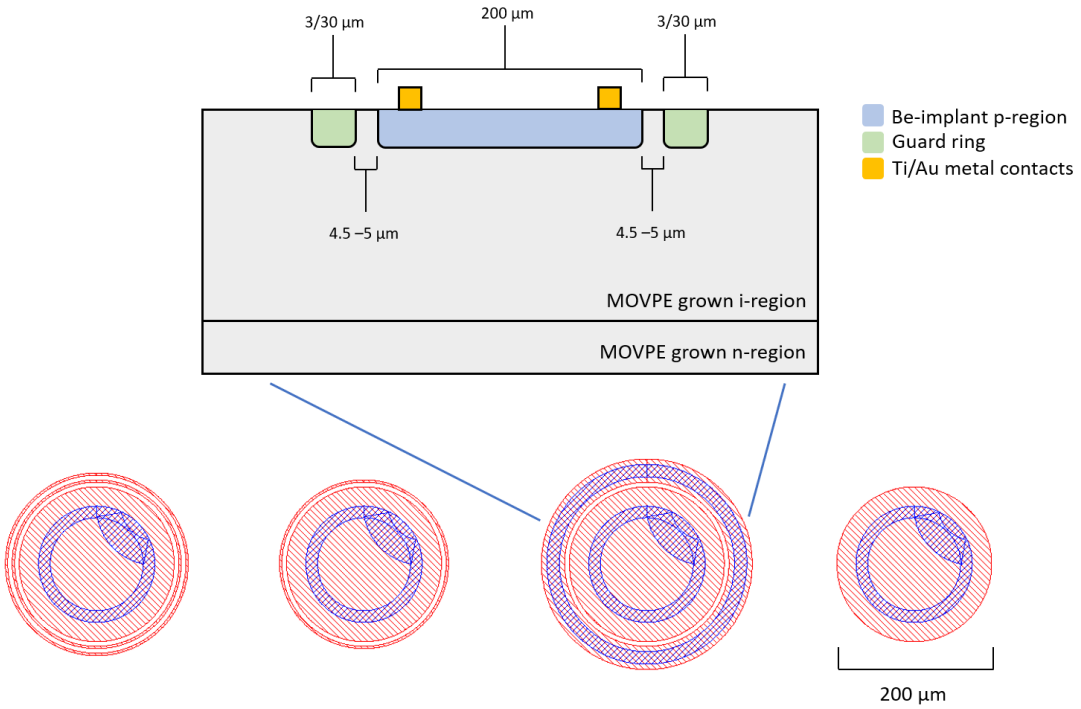

Figure 4.9 200 µm diameter diodes with different guard ring designs and a cross sectional drawing of one of the 200 µm diameter diodes with wide guard rings

Table 4-II Corrected diameters (addition of guard rings) of 200 µm diameter diodes

Diode design	**Corrected diameters (µm)**
2x guard rings	236
1x guard ring	218
1x wide guard ring	272
No guard ring	200

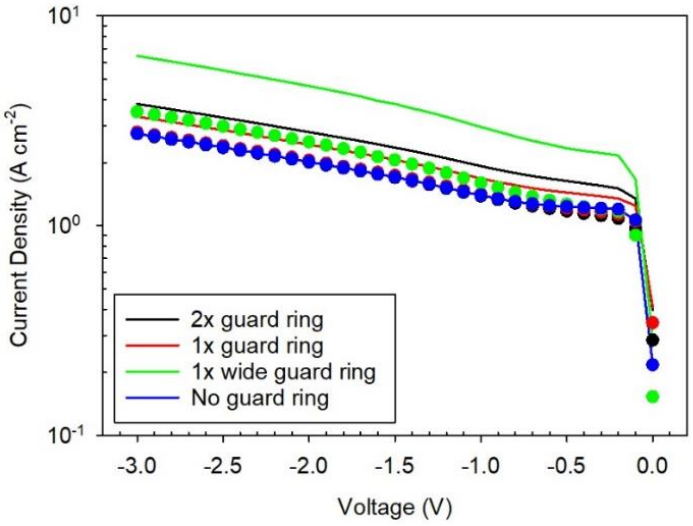

Figure 4.10 Dark current density of 200 μm diameter diodes at room temperature with uncorrected (solid lines) and corrected (circles) areas

4.7 Surface treatment processes on planar diodes

Despite a lower implantation energy used, there is no noticeable improvements in dark currents or responsivity in planar InAs diodes so far, as compared to the high energy implantation process, which is surprising in contrary to initial expectations. It is argued that a surface inversion layer forms post-annealing in Be and Mg implanted planar InSb diodes and a 400 nm deep etch sufficiently removes this layer, improving the resistivity of the diodes [36].

Mesa diodes with the blanket Be-ion implantation and planar InAs diodes discussed in this chapter, have near-identical fabrication processes (bar the addition of a photoresist mask to define implant windows in the planar sample). These diodes have been fabricated in a similar time period, and as a result, should have little deviations in sample surface conditions, in terms of damage, contaminations and general handling. However, the responsivity at 1520 nm of the planar diode is approximately 50% lower than that of the blanket implanted mesa diodes. To investigate if the cause is related to the surface condition of the planar diodes, different surface treatment methods are employed, namely by removal of native oxides on the surface with a 30 s HF clean or by etching a thin surface layer using standard acid mixtures (HPO_3: H_2O_2:H_2O in a ratio of 1:1:1 and H_2SO_4:H_2O_2: H_2O in a ratio of 1:8:80) for producing mesa InAs diodes.

In Fig. 4.11, dark current density comparison of untreated and surface treated planar diodes are shown, with plots of the blanket implant mesa diodes, standard MOVPE-grown mesa InAs and high energy implantation planar diodes (labelled as White *et al.*) included for reference. The HF treatment shows no improvement in dark current density but the diodes with a 417 nm etched surface show a factor of 3 reduced dark current density at -0.2 V from 1.46 A/cm^2 to 0.48 A/cm^2. Furthermore, the 1520 nm responsivity in the HF-treated diodes and the surface etched diodes improves to 0.53 and 0.62 A/W respectively. An interesting note is that the blanket implanted mesa InAs sample has similar levels of I-V as the planar InAs sample which does suggest that the room temperature I-Vs, being one order of magnitude larger than regular MOVPE grown InAs diodes, are likely to be an artefact of implant damage.

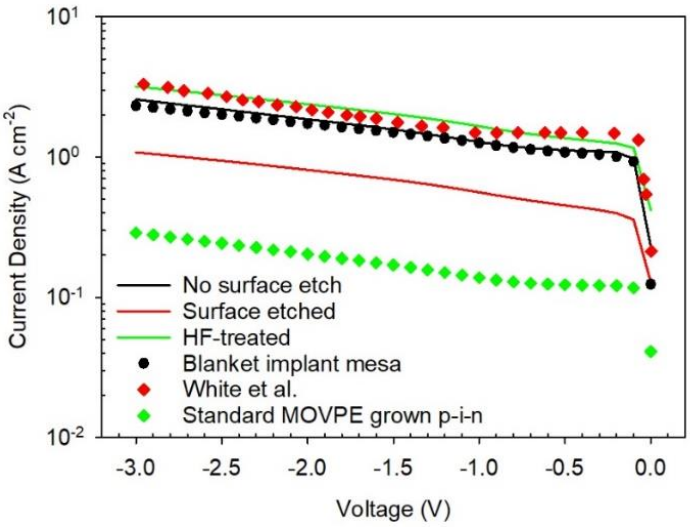

Figure 4.11 Comparison of dark current densities at room temperature of InAs planar diodes with and without surface treatment. Results from previous planar InAs APDs by White *et al.* and standard MOVPE grown mesa InAs APDs as reference are included.

The improvements in diode performance from surface etching is clearly more significant than from a HF surface clean. The surface etch was performed to an approximate depth of 417 nm without any photoresist mask and considering the depth of Be dopant diffusion from Fig. 4.3, the effective p-type region (with a doping concentration greater than 1x10^{17} cm^{-3}) is approximately 400 nm. This would mean that the observed reduction in dark I-V could be a consequence of removing the bulk of p-type layer (top contact metal will act as mask), thus reducing the diffusion component of dark current.

To verify this, a sample is cleaved into 3 parts to test the effects of varying surface etch depths on the photodiode characteristics. Similarly, the sample were dipped into a mixture of HPO_3:H_2O_2:H_2O then immediately into a mixture of H_2SO_4:H_2O_2:H_2O for fixed durations. The etch depths are estimated from the etch rates of InAs in the acid solutions, 1 μm/min for HPO_3:H_2O_2:H_2O and 500 nm/min for H_2SO_4:H_2O_2:H_2O. A summary of the samples tested with the calculated etch depths and responsivity are shown in Table 4-III. The I-V characteristics of diodes with a diameter of 400 μm from each sample are plotted in Fig. 4.12.

Table 4-III A summary of etch durations in phosphoric acid mixture and sulphuric acid mixture, the corresponding etch depth calculated from estimated etch rates and the responsivity at 0.2 V with 1520 nm wavelength light

HPO_3:H_2O_2:H_2O etch duration (s)	**H_2SO_4:H_2O_2:H_2O etch duration (s)**	**Etch depth (nm)**	**Responsivity (A/W)**
0	0	0	0.49
5	5	125	0.61
5	10	167	0.64
10	10	250	0.61
10	30	417	0.62

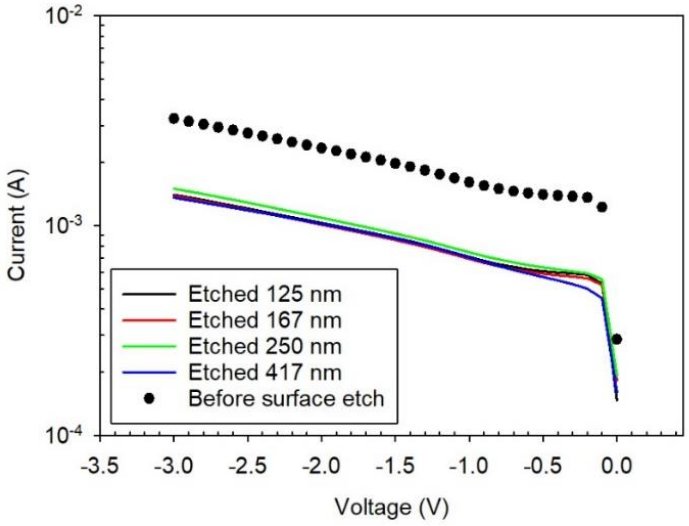

Figure 4.12 Current-voltage characteristics at room temperature of 400 μm diameter diodes from samples with different surface etch depths with an unetched sample as reference

The dark currents drop by a factor of 3 and the responsivity increases by a factor of 1.4 following a surface etch (regardless of the etch depth). The I-Vs and responsivities

indicate that there is no direct correlation to the etch depth. These results may suggest that surface recombination of the carriers are mitigated, leading to an increased responsivity and that the contribution to dark currents from the diffusion component is not affected greatly by the remaining thickness of Be-doped layer.

Consider only the electron flow in the p-layer, the reverse saturation current from equation 3.3 can be modified to become the following.

$$J_P = \frac{qD_n n_i^2}{L_n N_a} \tag{4.1}$$

The minority carrier diffusion length of electrons, L_n, for epitaxial grown InAs lies in the range of 30 – 60 μm [20]. The dark current density of standard MOVPE grown p-i-n mesa diodes are an order magnitude lower than Be-implanted planar InAs diodes, regardless of the implantation energy as seen in Fig. 4.11. One possible reason for the higher dark current levels seen is the diffusion of electrons from surface in ion implanted samples and the removal of these implant damage near the surface that leads to the improved performance independent of the surface etch depth.

A similar investigation was performed by White on diodes with an as-implanted junction depth of 1 μm [9]. It was found that etching 70 nm of the surface reduces the dark currents slightly to give a better fit for the area-scaled I-Vs, implying the removal of surface leakage currents. Removing >500 nm of the surface results in poor diode current-voltage characteristics and in the extreme case of etching up to 780 nm, diodes begin to show a lack of rectifying behaviour. This suggests that surface etch after a certain point, affects diode performance negatively, possibly from the re-introduction of significant surface leakage components from the exposed sidewall areas and should only be employed to remove a thin surface layer. However, it is interesting to note, the 70 nm shallow etch in White's work did not contribute to significant reductions in dark current such as in this work, indicating that the implant damage remain deep in the junction depth, beyond the reach of a simple shallow etch. In this work, it is clear that applying a shallow surface etch is beneficial to the performance of planar InAs diodes with shallow implant depths, but it should be noted that this adds a layer of complication during fabrication to passivate the now exposed surfaces.

4.8 Conclusions

Planar InAs APDs fabricated in this work have demonstrated superior performance post-surface etching with a 3x reduction in dark current from 1.46 Acm^{-2} to 0.47 Acm^{-2} and 1.4x improvement in responsivity from 0.49 A/W to 0.62 A/W at 1520 nm. These diodes were produced with a combination of 34 keV Be-ion implantation, 15 minutes long anneal at 500°C and a shallow surface etch of 100 nm. These results show a marked improvement from previous work with high energy implantation, in particular the reduced dark current and improved responsivity after surface etching which suggests the implant damage is close to the surface and can be more easily modified. The intentional long annealing duration creates a dopant diffusion profile with a graded p-type region of 400 nm as verified by SIMS. For an InAs planar APD array, a 15 µm distance between adjacent diodes is required to provide sufficient diode-to-diode isolation.

4.9 Reference

[1] P. J. Ker, A. R. J. Marshall, C. H. Tan, and J. P. R. David, 'Surface passivation of InAs avalanche photodiodes for low-noise infrared imaging', *IEEE 6th Int. Conf. Photonics*, p. 3, 2016.

[2] P. J. Ker, J. P. R. David, and C. H. Tan, 'Temperature dependence of gain and excess noise in InAs electron avalanche photodiodes', *Opt. Express*, vol. 20, no. 28, p. 29568, Dec. 2012, doi: 10.1364/OE.20.029568.

[3] C. H. Tan, A. Velichko, L. W. Lim, and J. S. Ng, 'Few-photon detection using InAs avalanche photodiodes', *Opt. Express*, vol. 27, no. 4, p. 5835, Feb. 2019, doi: 10.1364/OE.27.005835.

[4] B. S. White *et al.*, 'High-Gain InAs Planar Avalanche Photodiodes', *J. Light. Technol.*, vol. 34, no. 11, pp. 2639–2644, Jun. 2016, doi: 10.1109/JLT.2016.2531278.

[5] C. P. Skrimshire *et al.*, 'Reliability of mesa and planar InGaAs PIN photodiodes', *IEE Proc. J Optoelectron.*, vol. 137, no. 1, p. 74, 1990, doi: 10.1049/ip-j.1990.0015.

[6] E. Ishimura *et al.*, 'Degradation Mode Analysis on Highly Reliable Guardring-Free Planar InAlAs Avalanche Photodiodes', *J. Light. Technol.*, vol. 25, no. 12, pp. 3686–3693, Dec. 2007, doi: 10.1109/JLT.2007.909357.

[7] M. Brilman, 'High reliability photodiodes for space applications', *Microelectron. Reliab.*, vol. 14, pp. 305–308, 1975.

[8] H. Sudo, Y. Nakano, and G. Iwane, 'Reliability of germanium avalanche photodiodes for optical transmission systems', *IEEE Trans. Electron Devices*, vol. 33, no. 1, pp. 98–103, Jan. 1986, doi: 10.1109/T-ED.1986.22444.

[9] B. S. White, 'Planar InAs avalanche photodiodes for infrared sensing: Towards a true solid state photomultiplier', University of Sheffield, Sheffield, U. K., 2016.

[10] M. Ilegems, 'Beryllium doping and diffusion in molecular-beam epitaxy of GaAs and Al_xGa_1-xAs', *J. Appl. Phys.*, vol. 48, p. 1278, 1977.

[11] E. F. Schubert, J. M. Kuo, R. F. Kopf, H. S. Luftman, L. C. Hopkins, and N. J. Sauer, 'Beryllium δ doping of GaAs grown by molecular beam epitaxy', *J. Appl. Phys.*, vol. 67, p. 1969, 1990.

[12] W. V. McLevige, M. J. Helix, K. V. Vaidyanathan, and B. G. Streetman, 'Electrical profiling and optical activation studies of Be-implanted GaAs', *J. Appl. Phys.*, vol. 48, p. 3342, 1977.

[13] L. W. Lim, C. H. Tan, J. S. Ng, J. D. Petticrew, and A. B. Krysa, 'Improved Planar InAs Avalanche Photodiodes With Reduced Dark Current and Increased Responsivity', *J. Light. Technol.*, vol. 37, no. 10, pp. 2375–2379, May 2019, doi: 10.1109/JLT.2019.2905535.

[14] R. C. Clarke and G. W. Eldridge, 'Transient capless annealing of ion-implanted GaAs', *IEEE Trans. Electron Devices*, vol. 31, no. 8, pp. 1077–1082, Aug. 1984, doi: 10.1109/T-ED.1984.21664.

[15] J. P. Donnelly, 'The Electrical Characteristics of Ion Implanted Compounds Semiconductors', *Nucl. Instrum. Methods*, vol. 182/183, pp. 553–571, 1981.

[16] S. J. Pearton and R. Caruso, 'Rapid thermal annealing of GaAs in a graphite susceptor—comparison with proximity annealing', *J. Appl. Phys.*, vol. 66, no. 2, pp. 663–665, Jul. 1989, doi: 10.1063/1.343534.

[17] S. J. Pearton, K. D. Cummings, and G. P. Vella-Coleiro, ‘Electrical activation of implanted Be, Mg, Zn, and Cd in GaAs by rapid thermal annealing’, *J. Appl. Phys.*, vol. 58, no. 8, pp. 3252–3254, Oct. 1985, doi: 10.1063/1.335782.
[18] S. J. Pearton, R. Hull, D. C. Jacobson, J. M. Poate, and J. S. Williams, ‘Relationship between secondary defects and electrical activation in ion-implanted, rapidly annealed GaAs’, *Appl. Phys. Lett.*, vol. 48, p. 38, 1986.
[19] X. Zhou, X. Meng, A. B. Krysa, J. R. Wilmott, J. S. Ng, and C. H. Tan, ‘InAs Photodiodes for 3.43 µm Radiation Thermometry’, *IEEE Sens. J.*, vol. 15, no. 10, p. 5555, 2015.
[20] M. P. Mikhailova, ‘Indium Arsenide (InAs)’, in *Handbook Series On Semiconductor Parameters, Vol. 1: Si, Ge, C (Diamond), GaAs, GaP, GaSb, InAs, InP, InSb.*, vol. 1, World Scientific Publishing Co. Pte. Ltd., 1996, pp. 147–167.
[21] W. V. McLevige, K. V. Vaidyanathan, B. G. Streetman, J. Comas, and L. Plew, ‘Diffusion Studies of Be-implanted GaAs by SIMS and Electrical Profiling’, *Solid State Commun.*, vol. 25, pp. 1003–1008, 1978.
[22] S. J. Pearton, A. R. Von Neida, J. M. Brown, K. T. Short, L. J. Oster, and U. K. Chakrabarti, ‘Ion implantation damage and annealing in InAs, GaSb, and GaP’, *J. Appl. Phys.*, vol. 64, no. 2, pp. 629–636, Jul. 1988, doi: 10.1063/1.341952.
[23] K. D. Cummings, S. J. Pearton, and G. P. Vella-Coleiro, ‘Rapid annealing of GaAs: Uniformity and temperature dependence of activation’, *J. Appl. Phys.*, vol. 60, p. 163.
[24] C.-K. Li and Y.-R. Wu, ‘Study on the Current Spreading Effect and Light Extraction Enhancement of Vertical GaN/InGaN LEDs’, *IEEE Trans. Electron Devices*, vol. 59, no. 2, pp. 400–407, Feb. 2012, doi: 10.1109/TED.2011.2176132.
[25] Y. Lu, ‘Activation of Be-Implanted GaAs by Using RTA with Proximity Contact’, *J. Electrochem. Soc.*, vol. 137, no. 6, p. 1904, 1990, doi: 10.1149/1.2086828.
[26] J. P. Donnelly and C. A. Armiento, ‘Beryllium-ion implantation in InP and In_1-xGa_xAs_yP_1-y’, *Appl. Phys. Lett.*, vol. 34, p. 96, 1979.
[27] Teledyne Judson Technologies, ‘Indium Arsenide Detectors’, *Indium Arsenide Detectors*. http://www.teledynejudson.com/products/indium-arsenide-detectors (accessed Feb. 24, 2020).
[28] Teledyne Judson Technologies, ‘J12 series InAs detectors operating instructions’. [Online]. Available: http://www.teledynejudson.com/prods/Documents/PB220.pdf.
[29] Hamamatsu Photonics, ‘InAs photovoltaic detectors - P10090 series and P7163’. [Online]. Available: https://www.hamamatsu.com/resources/pdf/ssd/p10090-01_etc_kird1099e.pdf.
[30] R. Rickenbach and P. Wendland, ‘Germanium Photodiodes - Temperature And Uniformity Effects’, San Diego, United States, Nov. 1985, p. 198, doi: 10.1117/12.949608.
[31] J. Burm, K. I. Litvin, W. J. Schaff, and L. F. Eastman, ‘Optimization of high-speed metal-semiconductor-metal photodetectors’, *IEEE Photonics Technol. Lett.*, vol. 6, no. 6, pp. 722–724, Jun. 1994, doi: 10.1109/68.300174.
[32] M. D. Lammert and R. J. Schwartz, ‘The Interdigitated Back Contact Solar Cell: A Silicon Solar Cell for Use in Concentrated Sunlight’, *IEEE Trans. Electron Devices*, vol. ED-24, no. 4, p. 337, 1977.

[33] B. J. Baliga and S. K. Ghandhi, ‘Lateral Difusion of Zinc and Tin in Gallium Arsenide’, *IEEE Trans. Electron Devices*, vol. ED-21, no. 7, 1974.
[34] P. M. Campbell, ‘Beryllium Ion-Implanted Junctions in GaAs with Submicron Lateral Diffusion’, *J. Electrochem. Soc.*, vol. 132, no. 1, p. 186, 1985, doi: 10.1149/1.2113758.
[35] M. J. Helix, K. V. Vaidyanathan, B. G. Streetman, and P. K. Chatterjee, ‘Planar GaAs p-n Junctions by Be Ion Implantation’, *1977 Int. Electron Devices Meet. IEEE*, pp. 195–197, 1977.
[36] C. E. Hurwitz and J. P. Donelly, ‘Planar InSb Photodiodes Fabricated by Be and Mg Ion Implantation’, *Solid-State Electron.*, vol. 18, pp. 753–756, 1975.

Chapter 5 Mesa InAs and planar InAs linear arrays

It is clear that performance-wise planar InAs diodes from Be-ion implantation is currently beneath mesa InAs diodes. However, a planar structure device still holds promise as the path moving forward to producing stable InAs avalanche photodiodes for practical system usage due to the various issues plaguing mesa structure devices. The danger of catastrophic device breakdown when applying a high voltage bias required for high gain operation remains a longstanding issue due to the exposed junction in InAs mesa structures after etching. Despite best efforts from developing an etch recipe [1] to exploring different surface passivation schemes [2], [3], the presence of surface current components persists. For small area devices intended to produce individual pixels on a focal plane array, the surface leakage will be exacerbated due to the significant ratio of sidewall area to device area. Not only that, the isotropic wet etch coupled with the deep etching required for thick InAs structures inevitably produces diode area less than the intended nominal area, which means a reduced fill factor for an imaging array.

Furthermore, there is a lack of available publications to demonstrate avalanche photodiode arrays that can operate beyond 1.55 µm. To date, only Sandall *et al.* have reported linear arrays of mesa InAs APDs operating at 2004 nm [4]. In the published work, highly uniform dark current and gain (up to 90 % of pixels have deviations less than 10 % of the mean) were measured from a 1 × 128 pixels array with anomalous data near the array edges, attributed to sample damage during device processing.

Tall features or uneven surfaces on wafers are generally avoided during device fabrication due to the added complications to fabrication processes for example turbulent gas flows in vapour deposition processes, non-uniform etching and decreased bond pad yield. An irregular surface after etching processes is inevitable, hence, it is best for the step following after to not only passivate the exposed surfaces, but also to planarise the wafer to simplify subsequent processing. This can be achieved to different extents by polymer films like B-staged benzocyclobutene (BCB), polyimide or dielectric deposition like SiN_x or SiO_2.

This is an especially tricky problem in InAs APDs due to the thick intrinsic region required for high gain and the resulting tall mesas created. From work by

Marshall *et al.* [2], dielectric deposition by PECVD at a temperature range of 100 – 300 °C has shown to be ineffective as passivation, perhaps due to sidewall damage from high density plasma bombardment. BCB passivated diodes showed dark currents lower than unpassivated diodes only at low reverse bias voltages. Later, SU-8 was found to passivate InAs diodes sufficiently without much device degradation [3] as the polymer is also used to passivate narrow band gap type-II superlattice detectors [5].

SU-8 is an epoxy-based negative photoresist, popular in the micro-electro-mechanical systems (MEMS) field to fabricate high aspect ratio, rigid microsensor structures [6]. The mechanical hardness, chemical resistance and optical transparency above 400 nm wavelength are desirable properties of SU-8. The application of SU-8 by spin coating, similar to other photoresist polymers, is simple and economical to scale towards wafer-level fabrication. In addition, the thickness of SU-8 film can be controlled by the spin speed and viscosity from various commercially available mixtures [7]. An advantage of SU-8 passivation for InAs APDs is the relatively low curing temperatures required, minimising risk of device degradation. However, SU-8 faces difficulties when applied onto closely spaced features, giving rise to major issues in mesa array fabrication as will be discussed further in this chapter.

In this chapter, linear arrays of mesa and planar InAs photodiodes are fabricated. The fabrication process of the mesa diode arrays will be discussed to provide an understanding to the difficulties faced. The work done on this chapter expands upon planar structure InAs APDs as presented in chapter 4 into an array format. The uniformity and average values of I-V and responsivity are evaluated as performance parameters to compare the mesa and planar arrays.

5.1 Fabrication of mesa and planar linear arrays

The samples discussed in this chapter are processed from different wafers and mask sets. From here on, the samples will be denoted as MLA and PLA for the mesa and planar linear array samples, respectively. The MLA mask set was designed by Dr Manoj Kesaria to produce two adjacent arrays of 128 individual 80 μm×80 μm diodes with a 4 μm gap in between diodes (in reality the pixel size will reduce and the diode spacing increases due to the deep, isotropic wet etch profile). The metal contacts on

the device top surface act as individual anodes which are then probed one at a time and a common cathode is shared by a bottom metal on substrate side. Included in the mask are diodes of different sizes for bulk properties characterisation and transmission line measurement (TLM) pads.

The planar linear arrays are designed with identical pixel counts and sizes as the MLA mask except with a pixel gap of 15 μm (following the analysis of diode-to-diode isolation in chapter 4). Similar to the MLA design, a common cathode is shared through a bottom metal contact and anodes are on the individual pixel top contacts. Square pixels are selected to maximise the fill factor and the pixel size is chosen for a few reasons. One, the characteristics of small area devices are poorly understood, which may pose a problem if the surface is not well-maintained during the fabrication process. Two, to accommodate for the minimum ball size of 80 μm available on the ball bonder. This allows for a simpler design of the bond pad fan-out, avoiding more complicated arrangements of staggered bond pad that may reduce liftoff yield. Third, it also allows for ease of comparison to the mesa linear arrays.

The mask design includes diodes of varying sizes ranging from 200 μm×100 μm to 50 μm×25 μm to compare bulk and surface characteristics of planar InAs APDs. Surface leakage in diode sizes typical of image sensing arrays are investigated through the inclusion of mini arrays of small area diodes (30 μm×30 μm, 20 μm×20 μm and 10 μm×10 μm) with small area/perimeter ratios. The radius of curvature on the small area diodes varies from 0 to 5 μm. This is to investigate changes in edge breakdown, if any, from the junction profile produced after a shallow implant along with a long anneal time.

Furthermore, trenches are introduced in a mini array of small area diodes with identical sizes as the above mentioned diodes. These trenches act to investigate if a smaller pixel pitch is achievable and may be useful to shed light on crosstalk experienced by small area diodes. The trenches are 3 μm wide, to ensure process uniformity in the formation of trenches via ICP etching and the diode to trench spacing ranges from 2 to 5 μm. Characterisation of the small area diodes with and without isolation trenches are discussed in Chapter 6.

Details for the linear array samples are listed in the table below and the mask sets are shown in Fig. 5.1 along a schematic (not to scale) of two adjacent diodes in the planar array mask.

Table 5-I Details of linear array samples

Name	Sample	Mask set	Wafer structure
MLA	Mesa linear array	MK_2017	p-i-n (1/6/1 µm)
PLA	Planar linear array	LWL_2018	(p)-i-n (Be-ion implant/10/1 µm)

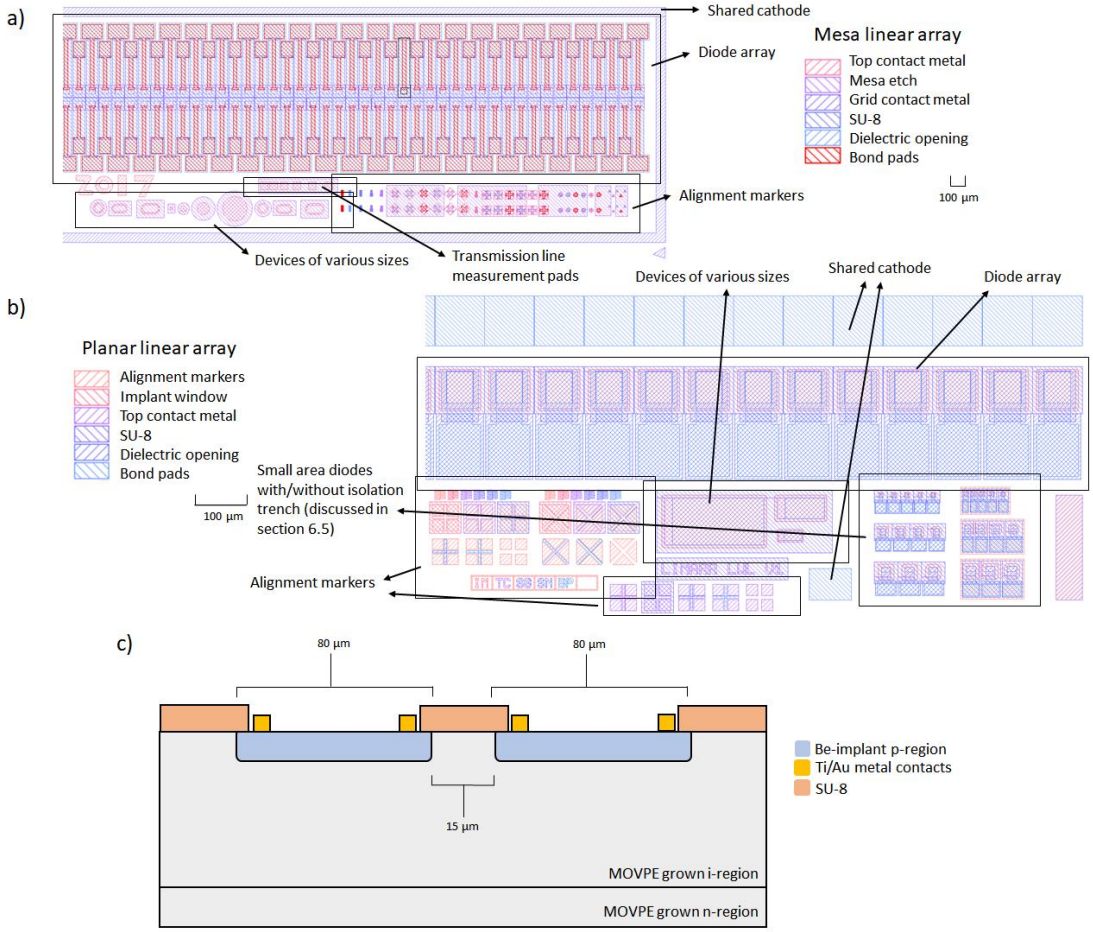

Figure 5.1 Mask set for mesa (a) and planar (b) linear array as well as schematic (c) of two adjacent diodes from planar linear array mask

The main difference in the fabrication process between the two types of linear arrays is the method in which the individual pixels are defined. For the MLA sample, pixel separation is achieved by wet etching whereas for the PLA sample selective area doping by Be-ion implantation is employed. The standard InAs wet etch recipe is used for etching the MLA followed by immediate spin coating of SU-8 post etching without

removing the sample from the cleanroom and investigating the post-etch current-voltage characteristics. This is to ensure the preservation of the InAs surfaces by minimising the exposure of etched surfaces to ambient air and the consequent formation of oxides. The PLA sample preparation for ion implantation and implantation conditions are identical from chapter 4, however, this implantation campaign was instead conducted by the Ion Beam Centre in the University of Surrey. The step-by-step detailed fabrication procedures for the PLA sample can be found in Appendix C.

Using these two mask sets, mesa and planar diode arrays are fabricated and compared. However, it should be noted that the results presented in this chapter are from part-fabricated samples where the MLA sample was processed up to the SU-8 passivation step whereas the PLA sample was processed until the metal deposition step.

5.2 Fabrication issues with mesa linear array

In this section, issues facing SU-8 passivation are investigated and a brief overview of the fabrication process of the mesa InAs linear array is given with illustrations at key processing steps. The SU-8 process is optimised and found to produce fairly consistent results when applied onto partially etched InAs mesa diodes. However, irregularities in the dark current performance are observed in the partially etched InAs diodes.

5.2.1 Fabrication issues caused by SU-8

SU-8 is widely reported as a viable photoresist for constructing complicated multilayer structures for MEMS applications [8], [9]. Each layer of SU-8 is processed up to the post-bake stage before spin coating the next layer. The entire process ends with a single development step to create the final multi-layered structure. The application of SU-8 onto flat wafer substrates is relatively simple and one such example is shown in Fig. 5.2 where aspect ratio more than 10:1 can be easily achieved. Tall mesa features unfortunately, impede the coating process and it is found that SU-8 tends to form a tall bump at the mesa or sometimes an uneven coating at the top of the mesa. This does not necessarily affect device development with the standard mask set as SU-8 passivation is the final processing step, however, for mesa linear array development, this creates a problem for subsequent processes such as bonding (as will be discussed later).

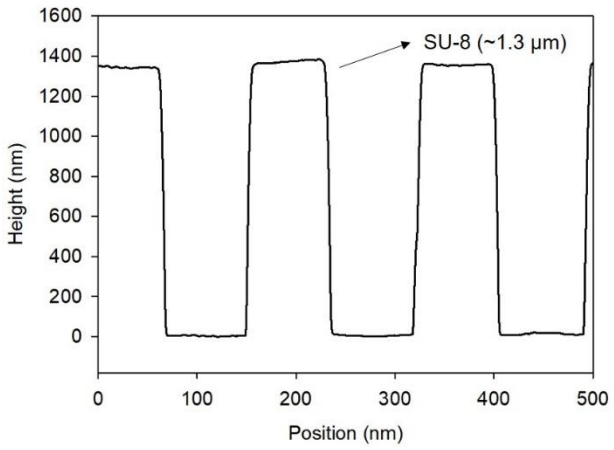

Figure 5.2 Uniform high aspect ratio (roughly 1300 nm : 70 nm) features can be obtained easily with SU-8 2 on flat wafers

SU-8 is available in various viscosity (by controlling the solids to solvent ratio) to achieve the desired thickness either by diluting a high solid concentration formulation or by purchasing ready-made commercially available mixtures. Obviously, the former allows more flexibility for the desired viscosity but will require additional processing to prepare the mixture. It is thought that SU-8 5, a commercially available version that produces a final thickness of 5 µm (when spun at 3000 rpm), is not compatible with the linear array development due to its viscosity and difficulty in achieving a uniform coating of closely packed mesa structures. In this work, SU-8 2 (final thickness of 2 µm when spun at 3000 rpm) is used instead unless stated otherwise. Fig. 5.3 shows profilometer scans of SU-8 2 when applied onto etched mesa structures, highlighting the formation of tall bumps, uneven coating of the mesas top and also trenching issue at the base of the mesa.

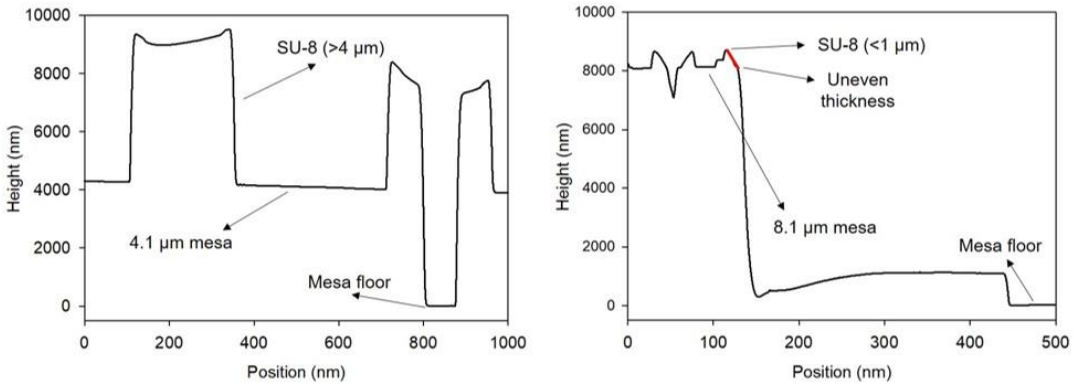

Figure 5.3 SU-8 2 tends to form tall bumps of varying heights around mesa boundaries. (left) SU-8 2 forms an uneven coating of tall features on mesa top and trenches at the base of mesa. (right)

Micrographs of the mesa linear array fabrication at each key step are shown below in Fig. 5.4. The initial wet etch shows excellent uniformity and the SU-8 coating process initially appears to be acceptable. However, the reactive ion etching process used to open up metal contact (after a blanket deposition of SiN_x dielectric for bond pad connection) shows incomplete and non-uniform opening. This could be an effect of reactant by-products becoming trapped within the tall SU-8 bump which hinders the dielectric-plasma reactions. Furthermore, due to the overall irregular shape of the sample, the bond pad yield is reduced due to the need to subject the sample to an ultrasonic bath for liftoff, which risks breakage at several points, one at the mesa top, one at the mesa boundary and one at the SU-8 and SiN_x boundary. It was found that out of the initial 120 tested devices only 7 had bond pads intact with unacceptable I-V characteristics.

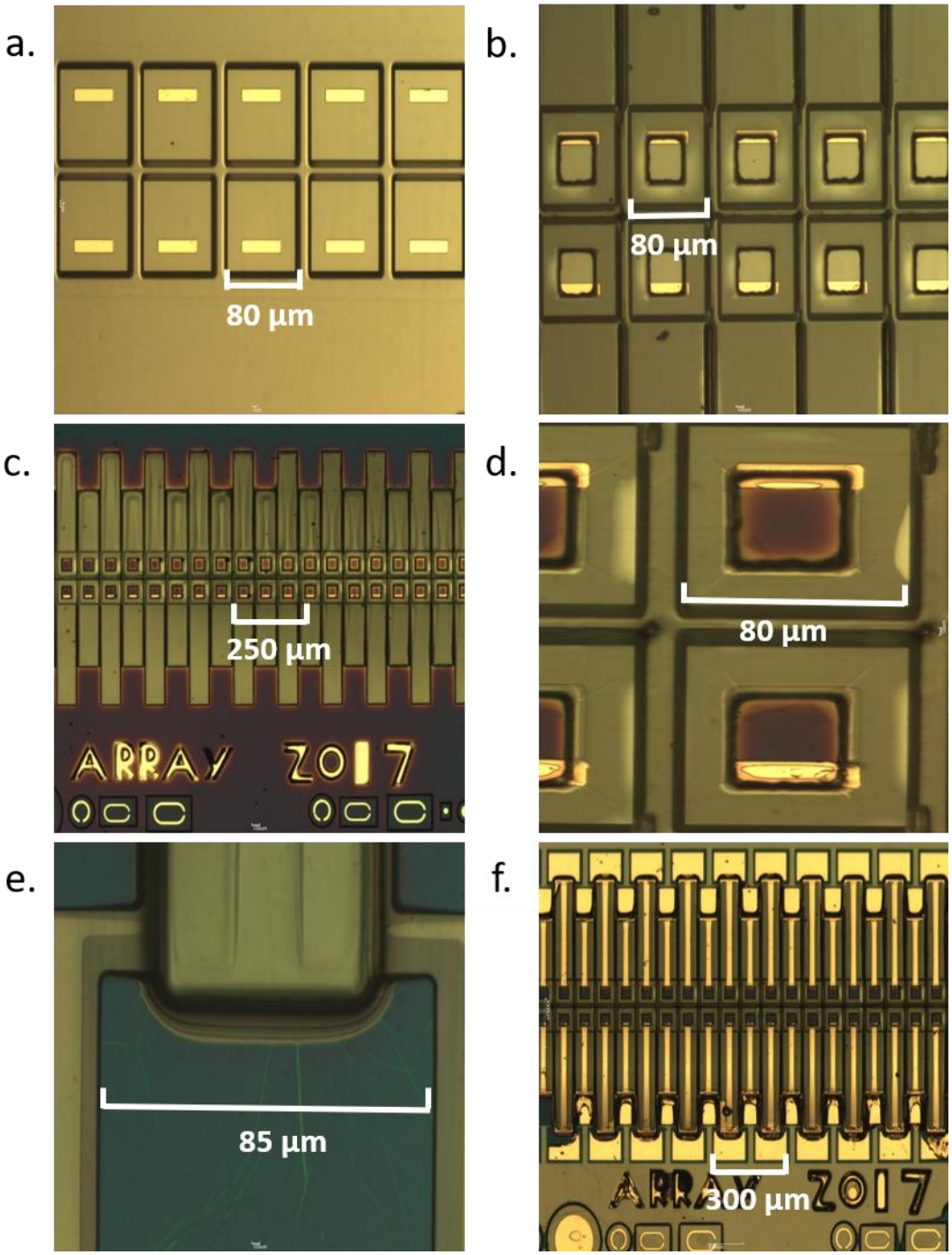

Figure 5.4 Micrographs of MLA sample at various processing stages. (a) Formation of individual devices post wet etching. (b) Application of SU-8 by spin coating. (c) 200 nm of SiN_x deposition by PECVD. (d) Removal of dielectric on the contact metals by reactive ion etching (RIE). (e) Alignment of photoresist prior to bond pad deposition. (f) Final step of bond pad deposition and liftoff.

5.2.2 Optimised SU-8 passivation

To optimise the application of SU-8 on mesa samples, a series of trials involving GaAs substrates etched to varying depths (using a 1:8:80 mixture of H_2SO_4:H_2O_2:DIW) followed by applying SU-8 is tested. It was found that consistent SU-8 height is obtainable with an improved process with 4 – 5 μm tall mesas. Table 5-II lists the old and new SU-8 procedures as a side-by-side comparison.

Table 5-II Comparison of old and improved SU-8 procedures

Old SU-8 procedures	**Improved SU-8 procedures**
1) Bake sample on hotplate at 100°C for 1 minute to drive off any residual moisture.	1) Bake sample on hotplate at 100°C for 1 minute to drive off any residual moisture.
2) Mount sample on blue tacky paper and dispense SU-8 over the entire surface.	2) Mount sample onto quartz glass with wax. Dispense SU-8 over sample surface and leave for 1 minute.
3) Spin at 4000 rpm for 30 seconds.	3) Spin initially at 500 rpm for 5 seconds then at 4000 rpm for 30 seconds.
4) Bake the sample at 65°C for 1 minute and then at 95°C for 3 minutes.	4) Bake the sample at 65°C for 1 minute and then at 95°C for 3 minutes.
5) Align and expose sample for 2 seconds using UV300 mask aligner.	5) Allow sample to cool for 5 minutes. Align and expose sample for 2 seconds using UV300 mask aligner.
6) Bake the sample at 65°C for 1 minute and then at 95°C for 1 minutes.	6) Bake the sample at 65°C for 1 minute and then at 95°C for 1 minutes.
7) Develop in Microposit EC solvent for 1 minute and rinse in isopropyl alcohol (IPA) for 1 minute.	7) Develop in Microposit EC solvent for 1 minute with strong agitation and rinse in separate beaker of Microposit EC solvent for 1 minute (rinsing in IPA is also acceptable).
8) Blanket expose sample using UV300 mask aligner for 240 seconds.	8) Remove sample from quartz glass by melting wax on hotplate. Clean wax off bottom of sample by soaking in warm n-butyl acetate. Rinse in warm IPA and blow dry.

The idea behind switching to mounting samples onto quartz glass is so that samples can be moved from station to station more quickly without intermittent pauses which may lead to more process uncertainties. For example, when the sample is spin coated,

the large SU-8 edge bead will begin to collapse towards the centre of the sample. Also, an unintended drop in temperature occurs when transporting the sample from hotplate to hotplate. Allowing the sample to cool before UV light exposure minimises risk of resist cracking when putting sample in contact with the photomask. The development of SU-8 requires vigorous agitation to achieve the high aspect ratios. Normally a post-development bake at >100 °C is required to permanently harden the SU-8 resist rather than a prolonged UV exposure, however, to prevent the possibility of device degradation, this step is avoided.

To test the improved SU-8 procedures, new MLA samples are fabricated with a total etch depth of only 4.5 μm. A reference sample using the NEWPIN mask is also fabricated for comparison. Fig. 5.5 illustrates the profile of the NEWPIN sample using the optimised SU-8 process where a bump approximately 1 μm in height is achieved.

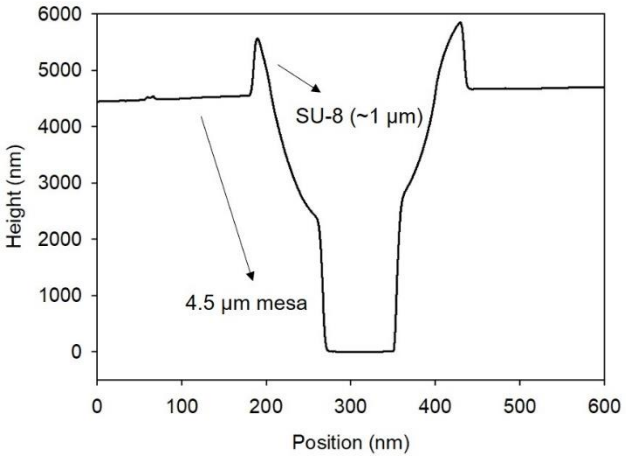

Figure 5.5 Profilometer scan on a NEWPIN device after improved SU-8 passivation procedures

Conventionally, a p-i-n or n-i-p diode is etched to the bottom layer to ensure diode-to-diode isolation as devices may still be connected due to the lack of electric field confinement in the vertical direction. Indeed, this was a technique used by Ker [3] to verify the background doping type of undoped InAs grown by MOVPE. By comparing the dark current level between fully and partially etched InAs diodes, it was found that partially etched p-i-n structures exhibit lower dark current levels than partially etched n-i-p structures which shows that the intrinsic layer is n-doped. A simple test by etching mesa InAs diodes to depths of 4 – 5 μm is performed, to assess the feasibility of applying the new SU-8 procedures.

From Fig. 5.6 (right), it can be seen that the current density of the partially etched 420 µm diameter diode from -0.1 to -2 V is slightly higher than its fully etched counterpart and the dark current eventually converges to similar levels. This is found to agree qualitatively with Ker's results [3]. It is also apparent that the current densities do not agree on both mask sets, especially in diodes of smaller sizes. Ker's work was focused on comparing the differences between partially etched p-i-n and n-i-p diodes so did not include any notes on the overall current density agreement. However, these results do suggest that a partial etch does not fully isolate diodes and there remains a slight spread of electric field in the n-layer that connects adjacent diodes. Furthermore, the benefit of partial etching for uniform application of SU-8 would be negated when attempted on n-i-p configuration diodes (potentially used for flip-chip bonded 2D arrays) due to the n-type background doping of undoped InAs layers. Thus, partially etched diodes are not considered in the following sections.

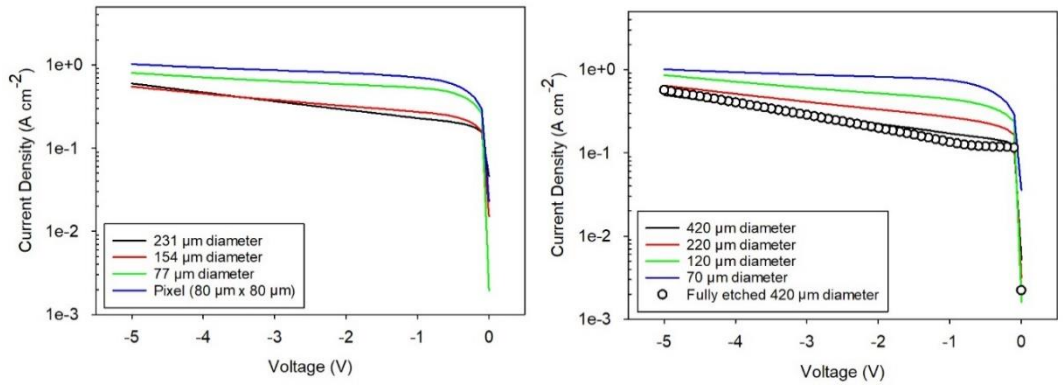

Figure 5.6 Dark current densities of devices fabricated from MLA (left) and NEWPIN (right) mask

5.3 Comparison of mesa and planar InAs linear array photodiodes

In this section, the linear arrays are compared in terms of the magnitude and uniformity of dark current and responsivities at various wavelengths.

5.3.1 Dark current comparisons

The dark current density-voltage curves of each sample is plotted in Fig. 5.7. The J-V of a single pixel is shown in comparison to devices of 231, 154, and 77 µm diameter from the same mask set. The good agreement in current densities indicate that bulk

current mechanisms are dominant. As reference, a device of 420 µm diameter fabricated with the NEWPIN mask from the same wafer is shown. The dark current levels are similar, suggesting that the standard etch recipe is sufficient to produce diodes of the same quality on the MLA mask set. On the other hand, current densities in the PLA sample does not conform. The current density increases as the device size decreases which suggests that the actual device sizes are larger than the nominal device sizes.

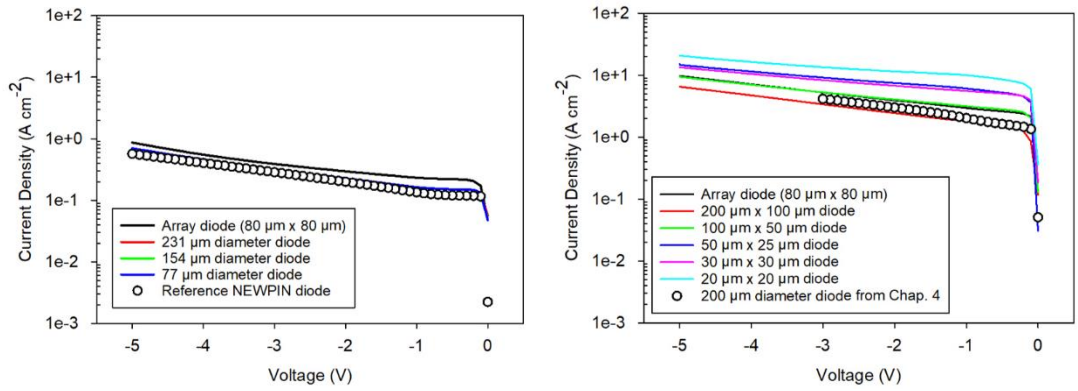

Figure 5.7 Dark current density versus voltage plots for MLA (left) and PLA (right) devices

Various size increments are tested to fit the current density plots and the area corrected J-V plots are shown in Fig. 5.8 where an additional 10 µm length has been added to all sides. It should then be noted that, the array pixels are spaced only 15 µm apart in the mask design which suggests that isolation between pixels are compromised. This is attributed to the low resistivity in the intrinsic layer. The mean J-V from the as-annealed planar InAs diodes of chapter 4 is included for comparison. It can be observed that the dark current level of ion implanted planar InAs diodes does not differ much wafer to wafer.

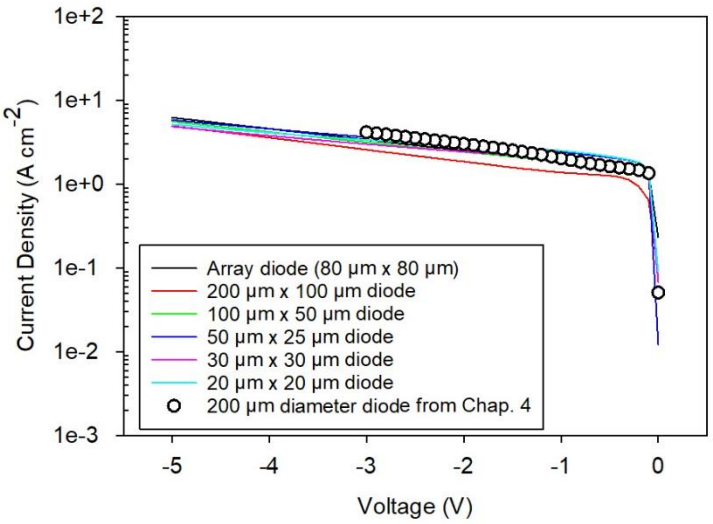

Figure 5.8 Area-corrected (added 10 µm to each side) dark current density plots for PLA devices

To assess the uniformity of dark currents in the arrays, the reverse I-V characteristics from 0 to -5 V of both samples are shown in Fig. 5.9. The displayed plots consist of an average of 91 and 49 devices for the MLA and PLA sample respectively and the standard deviation is presented as the error bar. It was not possible to assess a full row of 128 devices due to the length of sample used for device fabrication. As such, the devices presented were selected randomly across the entire sample area. While this does not provide us information regarding the row-by-row uniformity of the arrays, it does however, reveal information on the overall uniformity of the fabrication process.

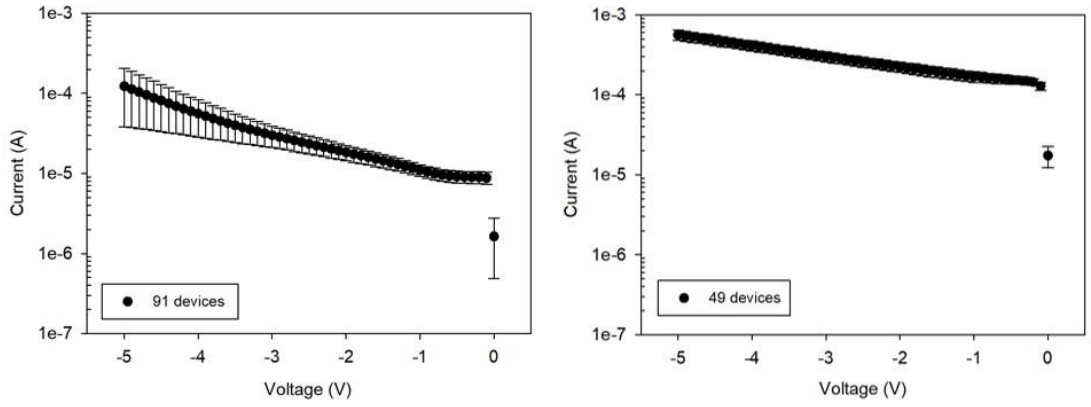

Figure 5.9 Average dark current versus voltage plot for MLA (left) and PLA (right) devices. The standard deviation is presented as the error bars.

It is clear that the dark current levels in the planar devices are an order of magnitude larger than mesa devices, consistent with observations made in chapter 4. It is

interesting to note that the spread in dark current appears to be comparatively smaller in the PLA, demonstrating a higher uniformity. Although it must be mentioned that the high uniformity in the PLA could be a result of the dominance of bulk dark currents over surface leakage. The dark current distribution at reverse biases of -0.1 and -5 V are shown as histogram plots as in Figs. 5.10 and 5.11, respectively.

At -0.1 V, the dark current of the MLA sample has a bimodal distribution with a peak at 9.75×10^{-6} A and a smaller peak at 7.25×10^{-6} A. The data ranges from 5.75×10^{-6} to 1.125×10^{-5} A. On the contrary, the distribution of the PLA sample is rather symmetrical around a peak at 1.225×10^{-4} A. The distribution of the MLA sample at -5 V is skewed heavily towards the right with a distinct peak at 7.5×10^{-5} A. This suggests that if a dark current of 2×10^{-4} A were set as the pass/fail threshold for a given pixel then a handful of devices would be considered as failed. Also to note is that the equipment used for I-V characterisation automatically stops the experiment when compliance (normally set to 1 mA for reverse bias InAs APDs) is reached. In that regard, anomalies have been excluded from this set of data. The -5 V distribution of the PLA sample shows two clusters of dark current centred at 4.9×10^{-4} A and 6.6×10^{-4} A. This could be due to devices selected from an area that is slightly damaged from sample handling.

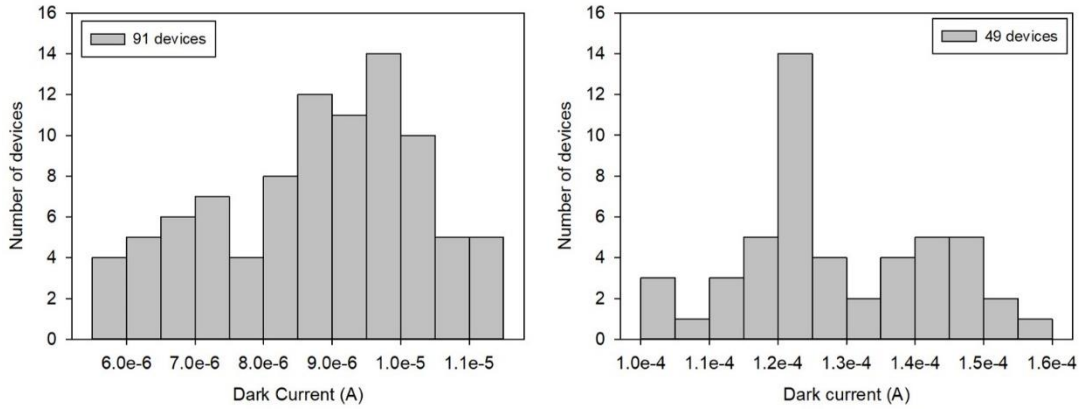

Figure 5.10 The distribution of dark current at -0.1 V for the MLA (left) and PLA (right) sample

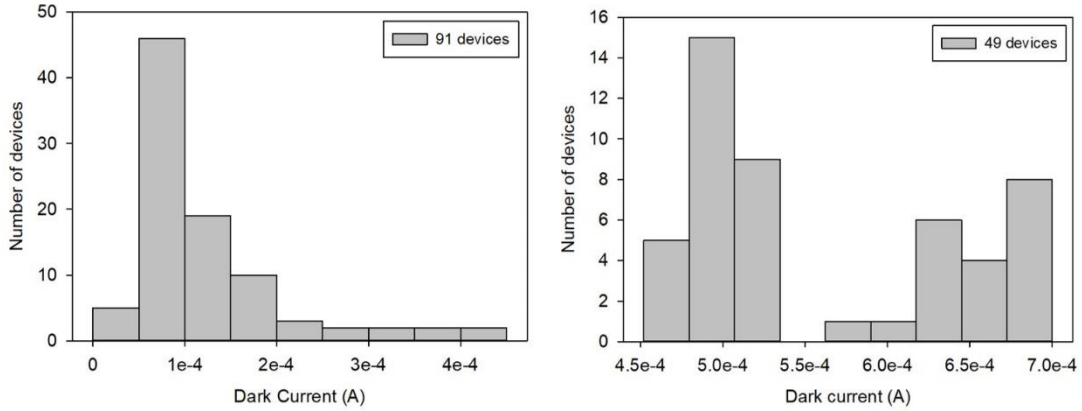

Figure 5.11 The distribution of dark current at -5 V for the MLA (left) and PLA (right) sample

5.3.2 Responsivity at 1520 and 2004 nm comparisons

The responsivity at reverse bias of -0.1 V of both samples for illumination wavelengths of 1520 and 2004 nm are shown in Figs. 5.12 and 5.13, respectively. The number of devices tested for each measurement is labelled within the plot. At an illumination wavelength of 1520 nm, the responsivity across 72 devices in the MLA sample is 0.57 ± 0.029 A/W, corresponding to a mean external quantum efficiency of 46.5 % whereas for the PLA sample, across 50 devices, a responsivity of 0.49 ± 0.017 A/W and a mean external quantum efficiency of 40.1 % is obtained. With a laser wavelength of 2004 nm, the mean responsivities are 0.91 ± 0.035 and 0.89 ± 0.024 A/W for the MLA and PLA samples respectively, corresponding to external quantum efficiencies of 56.3 % and 55.1 %. To ensure the variance in the presented data is not caused by external factors such as the laser spot alignment, reference diodes with large optical window from the NEWPIN mask set and the original planar mask set are tested as well that was found to give similar results as the smaller array diodes. Gain uniformity of the PLA sample is assessed and presented in Chapter 6.

The absorption coefficients of InAs at 1520 and 2004 nm are 1.1×10^4 and 1×10^4 cm^{-1} respectively [10]. 99% of the incident light will be absorbed by 4.2 and 4.6 μm of InAs at 1520 and 2004 nm respectively, so most, if not all the incident light will be absorbed by the samples used in this work. The poor external quantum efficiencies of the mesa diode array can be explained as the following (see section 4.5 for explanation on responsivity of planar diode). The laser spot size used in the measurement is roughly equal to the diode size. Hence, for the mesa diode array, some

of the light will be incident onto the sidewall areas due to the etch undercut producing a sloped sidewall profile and surface recombination could reduce the responsivity.

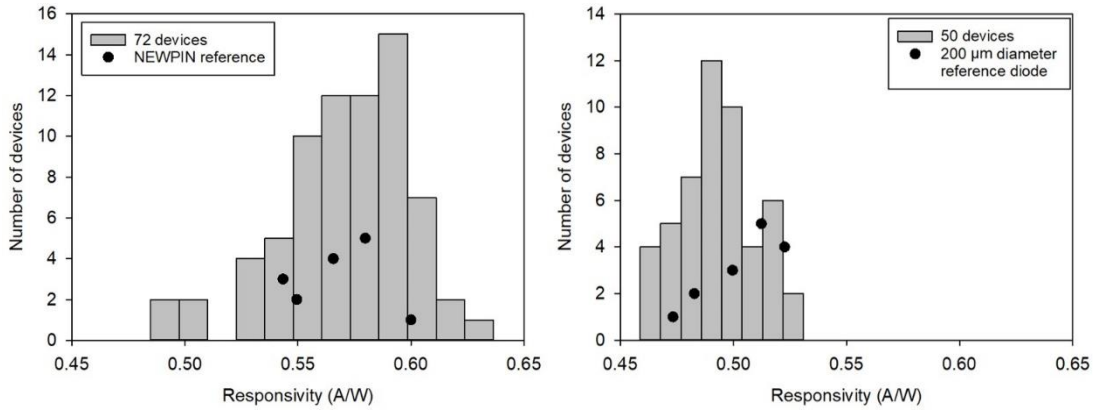

Figure 5.12 Responsivity at -0.1 V with 1520 nm incident light for MLA (left) and PLA sample (right)

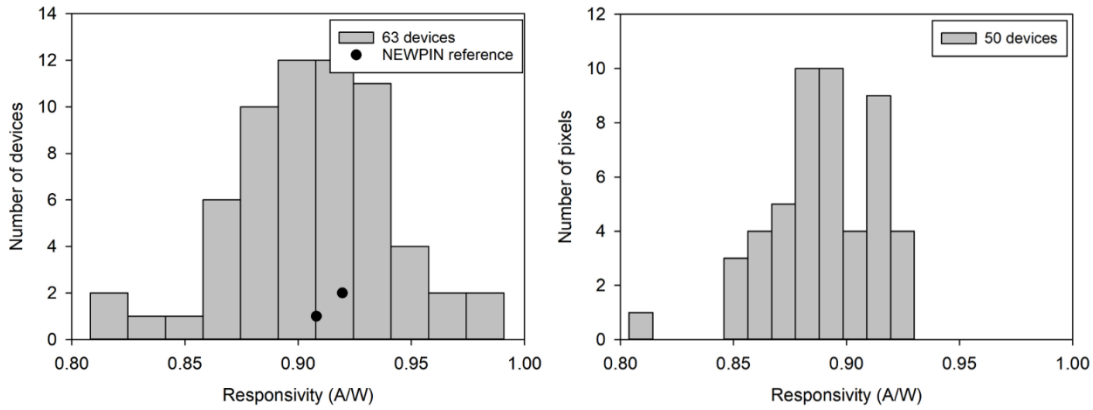

Figure 5.13 Responsivity at -0.1 V with 2004 nm incident light for MLA (left) and PLA sample (right)

5.4 Conclusions

Comparisons between the dark current and responsivity of mesa and planar configuration linear arrays of InAs diodes have been made in this chapter. The mean dark current levels are unsurprisingly higher in the planar sample than the mesa sample, however the standard deviation is found to be considerably smaller in the planar samples. Responsivity at 1520 and 2004 nm are not vastly in favour of the mesa diodes, showing only a mean responsivity 0.07 A/W higher than the planar samples. In addition, when the fabrication of mesa linear arrays is put under scrutiny, problems are highlighted and it is found that the difficulty of obtaining a uniform profile of SU-8

results in poor yield of arrayed diodes. The partial etching of mesa diodes to accommodate for the optimised SU-8 procedures creates complications in achieving complete diode isolation.

Considering the issues faced in mesa array fabrication, it is clear that the inferior performance of planar diodes can be overlooked and focused on for further work in producing linear arrays of InAs diodes. The large dark currents in planar devices can be reduced by operating at a lower temperature although that will limit practical applications where size and power consumption are major concerns.

5.5 References

[1] A. R. J. Marshall, C. H. Tan, J. P. R. David, J. S. Ng, and M. Hopkinson, 'Fabrication of InAs photodiodes with reduced surface leakage current', Florence, Italy, Oct. 2007, p. 67400H, doi: 10.1117/12.740700.

[2] A. R. J. Marshall, 'The InAs electron avalanche photodiode and the influence of thin avalanche photodiodes on receiver sensitivity', University of Sheffield, Sheffield, U. K., 2009.

[3] P. J. Ker, 'Development of high speed low noise InAs electron avalanche photodiodes', University of Sheffield, Sheffield, U. K., 2012.

[4] I. C. Sandall, S. Zhang, and C. H. Tan, 'Linear array of InAs APDs operating at 2 μm', *Opt. Express*, vol. 21, no. 22, p. 25780, Nov. 2013, doi: 10.1364/OE.21.025780.

[5] P. J. Ker, A. R. J. Marshall, A. B. Krysa, J. P. R. David, and C. H. Tan, 'Temperature Dependence of Leakage Current in InAs Avalanche Photodiodes', *IEEE J. Quantum Electron.*, vol. 47, no. 8, pp. 1123–1128, Aug. 2011, doi: 10.1109/JQE.2011.2159194.

[6] H. Lorenz, M. Despont, N. Fahrni, N. LaBianca, P. Renaud, and P. Vettiger, 'SU-8: a low-cost negative resist for MEMS', *J. Micromechanics Microengineering*, vol. 7, no. 3, pp. 121–124, Sep. 1997, doi: 10.1088/0960-1317/7/3/010.

[7] Kayaku Advanced Materials, 'SU-8 photoresists', *SU-8*. https://kayakuam.com/products/su-8-photoresists/ (accessed Feb. 25, 2020).

[8] B. Bohl, R. Steger, R. Zengerle, and P. Koltay, 'Multi-layer SU-8 lift-off technology for microfluidic devices', *J. Micromechanics Microengineering*, vol. 15, no. 6, pp. 1125–1130, Jun. 2005, doi: 10.1088/0960-1317/15/6/002.

[9] Z.-C. Peng, Z.-G. Ling, J. Goettert, J. Hormes, and K. Lian, 'Interconnected multilevel microfluidic channels fabricated using low-temperature bonding of SU-8 and multilayer lithography', San Jose, CA, Jan. 2005, p. 209, doi: 10.1117/12.592244.

[10] J. R. Dixon and J. M. Ellis, 'Optical Properties of n -Type Indium Arsenide in the Fundamental Absorption Edge Region', *Phys. Rev.*, vol. 123, no. 5, pp. 1560–1566, Sep. 1961, doi: 10.1103/PhysRev.123.1560.

Chapter 6 Low light detection with planar InAs avalanche photodiode array

With increasing demand for high sensitivity photodetectors in photon-starved applications such as LiDAR whether for atmospheric detection [1], imaging through obscurants [2] or to enable autonomous vehicular control [3], it is known that the use of an APD in the receiver system can offer benefits in detection of small signals by increasing the signal-to-noise ratio [4]. The increase in *SNR* does not scale infinitely with increasing APD gain due to the presence of the APD avalanche excess noise (F) in materials with $k \neq 0$. This results in a maximum *SNR* at an optimal gain that is dependent on F [5]. However, in InAs, it is known that only electrons can initiate impact ionisation and therefore the excess noise is limited to 2 by McIntyre's local theory, meaning that in theory, the *SNR* can continuously increase with gain. In practice, the *SNR* will eventually become limited by the APD dark currents [6], which can increase by various mechanisms, be it from tunnelling current at high reverse bias or from the total multiplied dark current. In a recent publication, mesa InAs APDs have demonstrated the capability to detect down to 19 – 40 fW of average power at a wavelength of 1550 nm, corresponding to the detection of less than 30 photons [7] within a 50 μs pulse. The findings suggest that it is possible to detect fewer photons had the system noise been lower, making InAs a promising material for high sensitivity applications, possibly down to single photon detection.

In this chapter, planar arrays of InAs APDs have been fabricated and characterised at low temperatures. The temperature dependence of current-voltage characteristics are assessed to identify the dominant dark current mechanisms. In chapter 5, the low bias responsivity of the diode array has been evaluated. This chapter will expand further on the uniformity of the optical characteristics of the array by gain measurements at 200 and 77 K. For the detection of low level light signals, the APD array is connected to a pre-amplifier and spectrum analyser as described in section 3.4.1. The *SNR* of the APDs at different biases are also extracted using this measurement setup to show the effects of increasing signal amplification and diode noise concurrently.

The InAs wafer used in this chapter has a 6 μm thick i-layer and a 1 μm thick n-type layer. To form the p-type region, a 34 keV Be-ion implantation and annealing

conditions similar to previous chapters were used. To facilitate low temperature characterisation with the Janis probe station, the array is fabricated with bond pads. Oxide formation on the surface (after a prolonged period of storage in ambient environment) is removed by a 40% HF clean for 30 s (without any photoresist), followed by the immediate application of 1.4 µm thick layer of SU-8 as passivation. For bond pads, a 520 nm layer of SiN_x is first deposited at 100 °C using an Oxford Instruments PlasmaPro100 ICPCVD system. Low temperature deposition is employed to prevent sample degradation at higher temperatures and a relatively thick SiN_x film was targeted to provide insulation between the bond pads and the sample intrinsic layer, considering the reduced permittivity of dielectric films deposited at low temperatures. Ti/Au bond pads with nominal thicknesses of 40/500 nm (to account for shadowing effect during evaporation) are deposited. The details of fabrication are described in Appendix A.

6.1 Temperature dependence of current-voltage characteristics

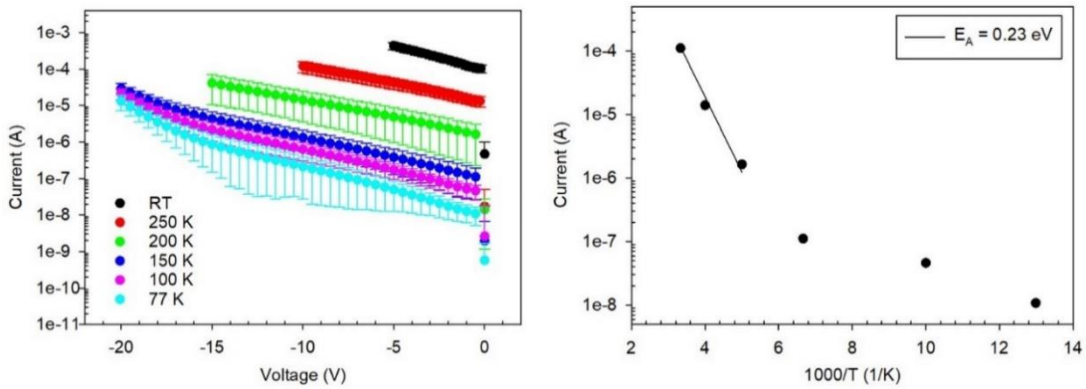

Figure 6.1 Temperature dependence of dark current characteristics from room temperature to 77 K (left). Arrhenius plot of dark current at -0.5 V (right)

Fig. 6.1 (left) shows the mean reverse dark I-V characteristics obtained from 87 devices in a planar linear array (PLA) and the error bars represent the standard deviations. The dark I-V at a bias of -0.5 V show approximately 4 orders of magnitude drop from 1.10×10^{-4} to 1.08×10^{-8} A as the temperature reduces from 295 to 77 K which corresponds to dark current densities of 1.72 and 1.69×10^{-4} A/cm^2 respectively, using the nominal device size of 80 µm by 80 µm. There is a clear increase in standard deviation in the 77 K I-Vs, suggesting that the surface current component could be more dominant at low temperatures. The spread is comparatively larger from -3

to -16 V in the 77 K plot; as tunnelling current becomes dominant beyond -16 V, the standard deviation decreases. From the reverse dark I-V plots, it can be seen that the gradient of dark currents in the 150 – 77 K plots agree well in the high voltage bias range above -15 V. Tunnelling as a leakage current mechanism has a weak temperature dependence since only the band gap changes with temperature. Breakdown in InAs APDs will therefore be 'soft' due to the gradual increase in tunnelling currents, which is in line with previous understanding of InAs APDs.

The changes in the standard deviation over the measured voltage range can therefore be explained as the competing effects between the surface leakage, depending on the surface condition of the diode array at different parts of the sample, and the tunnelling current, which is a bulk mechanism that affects all diodes more equally. It is then clear that the surface condition remains a delicate issue to solve despite attempts to minimise the duration of exposure of the InAs sample to ambient air during the fabrication process.

The activation energy of the dark current is extracted from the dark current at a reverse bias of 0.5 V versus the inverse of temperature plot as shown in Fig. 6.1 (right). By fitting the curve to the Arrhenius equation in chapter 3.15, an activation energy of 0.23 eV from room temperature to 200 K can be obtained. The value is close to half the band gap of InAs, which indicates that the dark current contributions from G-R processes are more dominant. The activation energy obtained here deviates from reported bulk activation energies for mesa and planar InAs APDs [8], [9]. Due to the difficulty to maneuver the probe tip to probe the smaller metal contact regions on diodes of other sizes in the cryogenic probe station, it was not possible to obtain the bulk and surface components of the dark current and fit to the Arrhenius equation separately.

A comparison of dark current density at different temperatures between the APD array and APDs from [8] is presented in Table 6-I. At 77 K, planar InAs APDs from [8] have dark current density of 4×10^{-7} A/cm^2 at -0.5 V which is 3 orders of magnitude lower than the APD array in this work. Other than the possible contribution of surface leakage current, another additional path of leakage current can come from the bond pads where the combination of metal and SiN can potentially form a metal-insulator-semiconductor junction. Unoptimised SiN_x films deposited at low

temperatures in general are of a lower density with a higher concentration of hydrogen present [10], giving rise to reduced dielectric constant. Tunnelling leakage currents are known to manifest through trap states in poor quality dielectric films. This is supported by a qualitative comparison in current densities between the array (80 μm×80 μm) and small area devices (30 μm×30 μm) as in Fig. 6.2. Given the current density analysis at room temperature done in Fig. 5.8 for devices of various sizes, using the nominal device sizes, the current density of the small area diodes should be larger than that of the diode array. However, it is quite the contrary under low temperature conditions and this may be explained by the difference in the area of metal contact region (12 times larger in the array diodes than the 30 μm by 30 μm devices) which will induce larger leakage currents from the bond pad/dielectric interface.

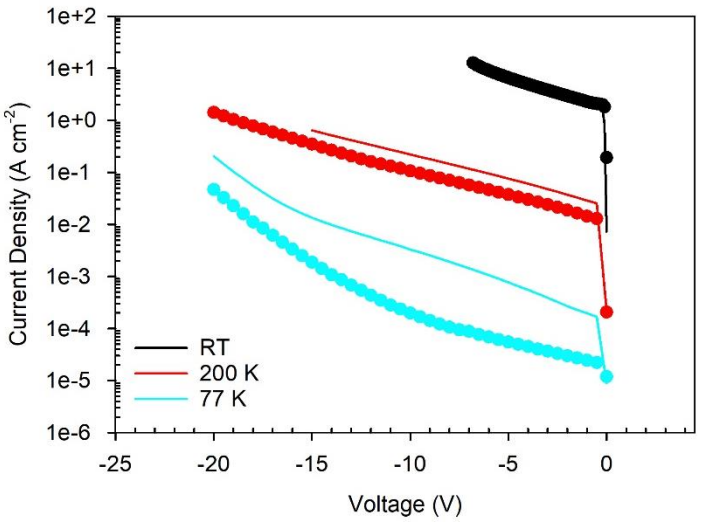

Figure 6.2 Current density comparison between 80 by 80 μm (solid lines) and 30 by 30 μm (symbols). The different colours indicate the various temperature points.

Table 6-I Comparison of dark current density of planar diodes at 0.5 V at different temperatures

Nominal temperature (K)	Average dark current density from planar array diodes at -0.5 V (A/cm^2)	Dark current density from Ref [8] at -0.5 V (A/cm^2)
295	1.72	1.46
250	0.22	0.046
200	0.03	3.87e-4
150	1.74e-3	4.57e-6

100	7.21e-4	5.66e-7
77	1.69e-4	4.16e-7

Fig. 6.3 (right) shows the forward I-V as a function of temperature typical of diodes within the array. Similar levels of reduction in dark current as in the reverse bias region are observed in the forward bias regime and the presence of an open circuit voltage at 77 K suggests background radiation limits the leakage currents. The photocurrent due to background radiation may also be a contributing factor to the high reverse currents as observed in Figs. 6.1 and 6.2.

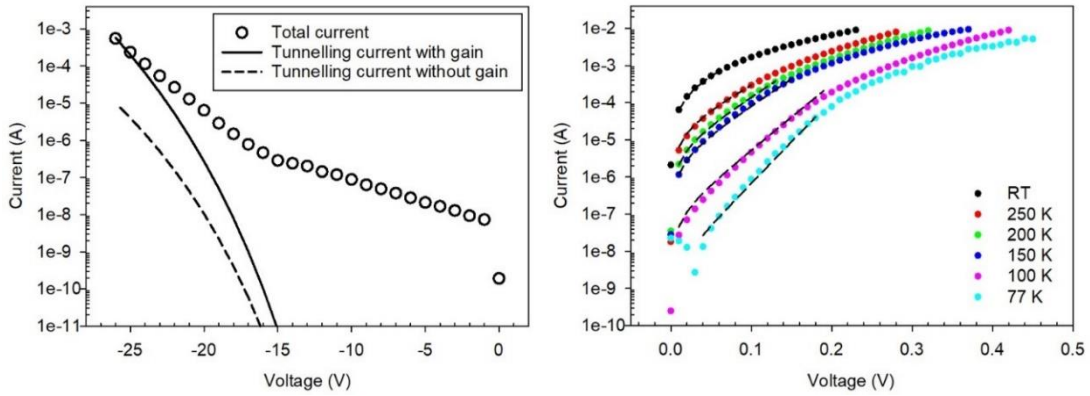

Figure 6.3 Fitting of the reverse dark current at high reverse biases to the band-to-band tunneling current in a p-i-n diode (left). Forward I-V as a function of temperature. Dashed lines show the region fitting to extract ideality factor. (right)

Fig. 6.3 (right) shows the forward I-V as a function of temperature typical of diodes within the array. Similar levels of reduction in dark current as in the reverse bias region are observed in the forward bias regime and the presence of an open circuit voltage at 77 K suggests background radiation limits the leakage currents. The photocurrent due to background radiation may also be a contributing factor to the high reverse currents as observed in Figs. 6.1 and 6.2.

In the temperature range of 295 to 200 K, the extracted ideality factor of 1.68 – 1.77 suggests that the total forward current is contributed from both diffusion and SRH recombination processes. Below 200 K, the ideality factor increases beyond the theoretical maximum of 2 with a n = 2.94 at 77 K. Increasing ideality factor with reduced temperatures have been observed in InAs photodiodes, although in these works the ideality factor does not exceed the theoretical maximum of 2 [11], [12].

From classical diode theory, the ideality factor is expected to fall within the range between 1 and 2. In some early works on crystalline Si solar cells, it is not uncommon to obtain ideality factors >2. This is often explained to be due to artefacts of trap-assisted tunnelling or multi-level recombination due to saturated amounts of localised defects [13]. In heterostructure diodes, such as AlGaAs/GaAs [14] and AlGaN/GaN [15], large ideality factors are often attributed to rectification caused by large band discontinuities at unipolar heterojunction interfaces and Schottky junction formation at non-ideal metal-semiconductor boundaries [16]. In the case of the InAs diodes investigated in this work, the wafer structure is rather simple, with an i-layer and an n-layer grown homoepitaxially on InAs substrate. Therefore it is expected to not behave as the examples mentioned above.

One possible reason to account for the deviation in ideality factor is the inaccuracy of the nominal temperature reading from the temperature controller. The cold fingers from the temperature controller for temperature monitoring of the Janis probe station is located underneath the sample positioning chuck where it is closest to the liquid nitrogen flow. Therefore the temperature reading does not accurately reflect the true temperature at device level as the system relies on thermal conduction and good thermal contact between the chuck and the sample. Since the product of ideality factor and device temperature forms the denominator in the exponential term of the Shockley I-V equation (the k term is a constant), it is possible that the real device temperature is higher than the reading obtained from the temperature controller, resulting in a larger ideality factor from forward I-V fitting.

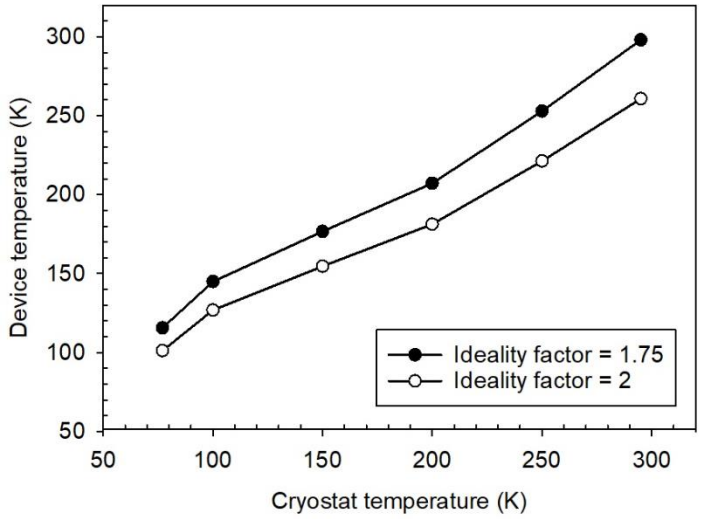

Figure 6.4 The fitted device temperature vs. cryostat temperature obtained from the temperature controller

The analysis in Fig. 6.4 illustrates a set of plausible device temperature by assuming fixed ideality factors (at n = 1.75 and n = 2) to fit the forward current curves. It is clear that above 200 K the device and cryostat temperature are in close agreement for n = 1.75. However, below 200 K, the difference in temperature becomes larger when for n = 1.75 as compared to η = 2. For example when the temperature controller reads 77 K, using an assumed ideality factor of 2, the device temperature is 101 K as compared to 115 K for an assumed ideality factor of 1.75. The analysis shows only the possibility of a temperature differential between the real device temperature and temperature controller. To improve on low temperature device characterisation, a silicon diode with known forward current characteristics at various temperatures can be positioned near the DUT to calibrate for the real device temperature.

6.2 Calibration of optical system

A HP8168C tunable laser source that is fibre coupled into a standard single mode fibre on the low temperature probe station is used as the APD's illumination source. The operation wavelength used in this work is 1550 nm and the laser output power (as specified on the equipment) ranges from 1.6 mW to 1 nW when modulated. A fixed attenuator of -20.5 dB at 1550 nm is placed at the laser output to reach levels below 1 nW. A reference InGaAs photodiode of 1.8 mm diameter with a known responsivity is used to evaluate the actual optical power coming from the fibre at device level within the probe station and Fig. 6.5 shows the actual measured optical power from the fibre

after attenuation and coupling losses from the laser output settings. As seen in Fig. 6.5, the laser output response is linear over a wide range of optical power.

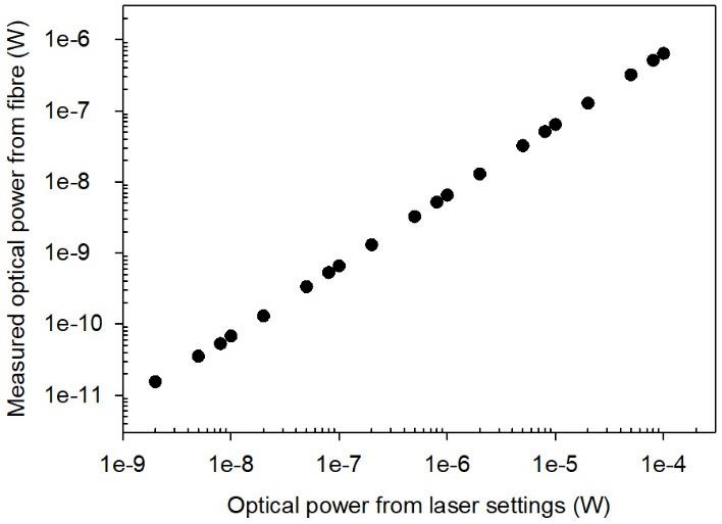

Figure 6.5 The laser output power settings and its corresponding actual optical power exiting the fibre in the Janis probe station chamber

Although standard single mode fibres typically have core diameters ranging from 8 to 10 µm which is significantly smaller than the nominally 80 µm by 80 µm diode area, the divergence of the laser beam which is dependent on the fibre height (judged solely based on the camera focus) will likely result in a large laser spot on the device. It is therefore difficult to know the exact spot size because the fibre is positioned at an angle (less than 90°) incident to the device plane.

However, it is possible to deduce the optical power falling onto the diode by measuring the coupling efficiency. To do so, the diode responsivity is first obtained from a top-illumination optical setup. The diode is then loaded into the Janis chamber and the fibre is positioned until a maximum photocurrent is obtained. The optical power falling onto the device window corresponding to the measured photocurrent can be calculated from the known responsivity. The ratio of this measured power and the optical power obtained from the reference diode is the coupling efficiency and it was found that the coupling efficiency was close to 100 %. With knowledge of the coupling efficiency and the real optical power available from the fibre as in Fig. 6.5, the actual laser power at 1550 nm falling onto the device during optical characterisations is known.

6.3 Gain characteristics of APD array

Gain measurements are performed to assess the level of signal amplification provided by an APD's internal gain mechanism using the measurement setup as described in chapter 3.3. The mean gain characteristics out of 15 randomly selected diodes from the array at 295, 200 and 77 K are shown in Fig. 6.6 (left) by normalising the photocurrent at varying bias voltage to the photocurrent at -0.5 V. The injection wavelength used is at 1550 nm, which undoubtedly creates a mixed carrier injection profile in the high field region, considering the thin p-region with the implant and anneal conditions as discussed in chapter 4.2. It is clear that from reverse voltages of 0 to -7 V gain rises exponentially with voltage (straight line in a semilog plot) and tapers off beyond -7 V at 200 and 77 K. Gain measurements were limited at -7 V for room temperature measurements due to excessive dark currents and the resultant self-heating in the devices. The maximum measured gains are 8, 22.5 and 26 at voltage biases of -7, -15 and -20 V for the temperatures of 295, 200 and 77 K, respectively. The gain obtained in a number of epitaxially grown p-i-n mesa InAs APDs with nominally 6 μm intrinsic region from Ker's work [17] varies from a gain of 4 at -7 V reverse biased at room temperature to gains of 30 and 40 at a bias of -20 V at 77 K. The discrepancies between the measured gain in this work and previous results of similar intrinsic region thickness is likely to be due to factors such as carrier injection profile and background doping concentration.

The change in gradient beyond a bias voltage of -7 V can be explained by a change in electric field profile. Epitaxially grown intrinsic InAs by MOVPE is n-type as shown in past works by Ker [17]. The intrinsic and n-type regions in the wafer used in this work is similarly grown via the MOVPE technique and the assumption that the intrinsic region is also n-type should hold valid. Therefore the peak electric field is at the p-i junction and the external bias extends the depletion region towards the n-layer. As the depletion width increases, the APD gain increases as the electron-initiated impact ionisation chain becomes longer and produces a larger net concentration of carriers at the depletion edge near the n-region. It is possible that the intrinsic region becomes fully depleted at -7 V and further voltage increments only increases the peak electric field. As the electron ionisation coefficient of InAs has been shown to have a weak electric field dependence, the rate of increase of gain becomes reduced.

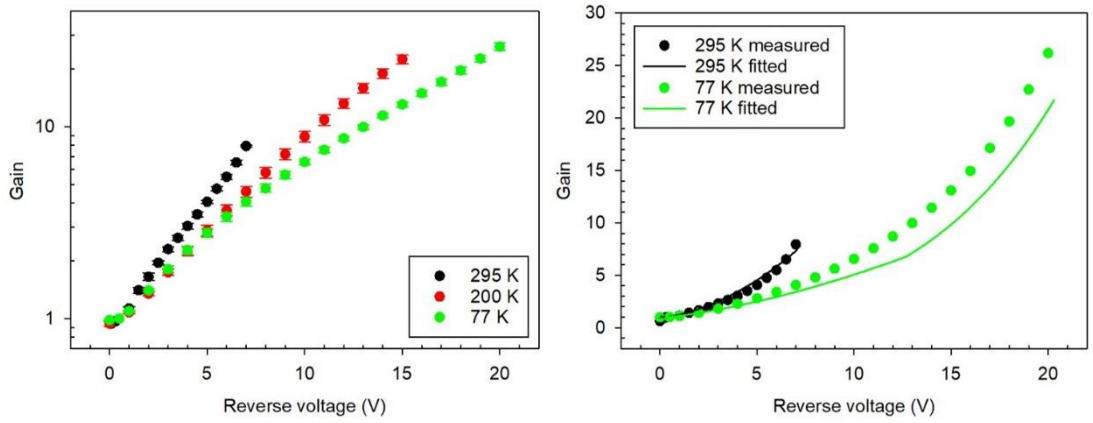

Figure 6.6 The measured (left) gain at temperatures of 295, 200 and 77 K and the modelled gain at 295 and 77 K (right) using McIntyre's equation

Another observation to be made for Fig. 6.6 (left) is that the gain at a particular voltage reduces with temperature. At a bias of -7 V, the measured gains are 8, 4.6 and 4 for the respective temperatures of 295, 200 and 77 K. This is consistent with past findings on the temperature variation of gain characteristics in InAs APDs. This is commonly explained as the effect of change in temperature to the band gap, and therefore the threshold energy for impact ionisation, is larger than the effect of change in scattering. In a simplistic manner, impact ionisation can be thought of as an eventual release of kinetic energies from a hot carrier to create secondary pair of carriers when energy exceeding a certain threshold (related to the band gap) is obtained. And that the original carrier can be impeded by the vibrations of the crystal lattice which causes it to prematurely lose its kinetic energy. Reduced temperature has an effect in raising the band gap of most semiconductor materials as well as decreasing the scattering likelihood. Although it may appear counterintuitive then to operate InAs at low temperatures due to the lower gain achievable however, it should be noted that the reduction in dark currents is more significant than the loss of gain at reduced temperatures, thus resulting in a net increase in *SNR*.

For a single carrier multiplication material, the gain has an exponential relation with the depletion width as in equation 2.5. Using this equation and electron ionisation coefficient as established in past works [18], [19], the modelled gain at 295 and 77 K is shown in Fig. 6.6 (right). The modelled gain conforms agreeably within the voltage range of the measured gain at room temperature. However, at biases above 7 V at 77 K, the fit begins to deviate from the measured results, showing theoretical values lower

than the measured data. The model assumes a uniform electric field profile, however, a tapered field profile is likely to be present in the diode due to the thick intrinsic region width. Furthermore, localised hotspot formation at junction boundaries in planar devices are not uncommon where a higher electric field may exist. TCAD simulations using the Sentaurus software package of a planar InAs APD at -10 V voltage bias is shown in Fig. 6.7. The simulated structure consists of a 10 μm thick intrinsic region with a background doping of 1×10^{15} cm^{-3} on a 1 μm thick n-type region with a doping level of 5×10^{18} cm^{-3}. A 400 nm p-type well region that is 40 μm wide with a doping concentration of 4×10^{18} cm^{-3} is embedded in the intrinsic layer to simulate the ion implanted region. The simulated lateral electric field profile is non-uniform and significantly higher near the p-i interface, therefore any carrier generated in the vicinity of hotspots may experience a higher probability of impact ionisation, causing larger gain and raising the overall gain. Due to the lack of a comprehensive fundamental parameter list for InAs (unlike other mature semiconductor platforms such as silicon and GaAs which often relies on TCAD design and modelling of devices prior to wafer growth and fabrication), TCAD modelling was not pursued extensively in this work.

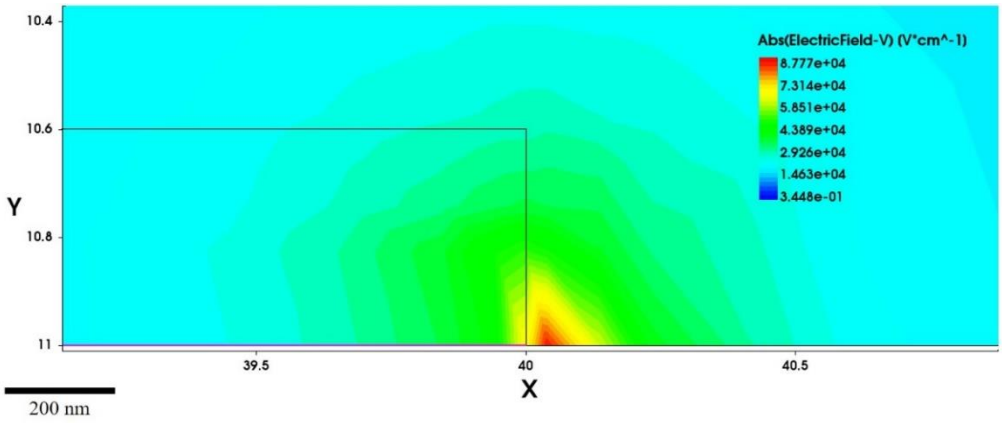

Figure 6.7 Simulation of a planar InAs APD with an implant depth of 400 nm at a voltage bias of -10 V

6.4 Low-light level measurements with linear APD array

To study the response to light under different voltage bias and illumination power as well as the sensitivity of the APD array, the sample was tested with the measurement setup described in chapter 3.4.1 at the nominal temperature of 77 K. The pre-amplifier was set to operate with a gain of 10^5 in low-noise mode where the cutoff frequency is

>10 kHz and the input noise current according to specifications is 2 pA/Hz$^{1/2}$. The spectrum analyser is set to a span of 24.4 Hz with 8 averages.

The signal spectra at varying bias voltage from 0 to -22.8 V in the frequency domain is illustrated in Fig. 6.8. The maximum voltage bias applied is limited by the input current overload on the pre-amplifier. Furthermore, a low optical power of approximately 3 nW is used to avoid a high total current at high gain (multiplied dark and photocurrent) overloading the pre-amplifier input. The operating frequency of the laser is set to around 10 kHz to avoid any contributions of 1/f flicker noise. A signal peak at around 10004.15 Hz corresponding to the laser operation frequency is seen to increase with bias voltage. The noise floor from 0 to -21 V remains fairly constant, indicating that system noise is greater than the device noise. Beyond -21 V, the noise floor is raised signifying the dominance of APD noise (due to the total current, i.e. sum of multiplied dark current and photocurrent) over the system noise.

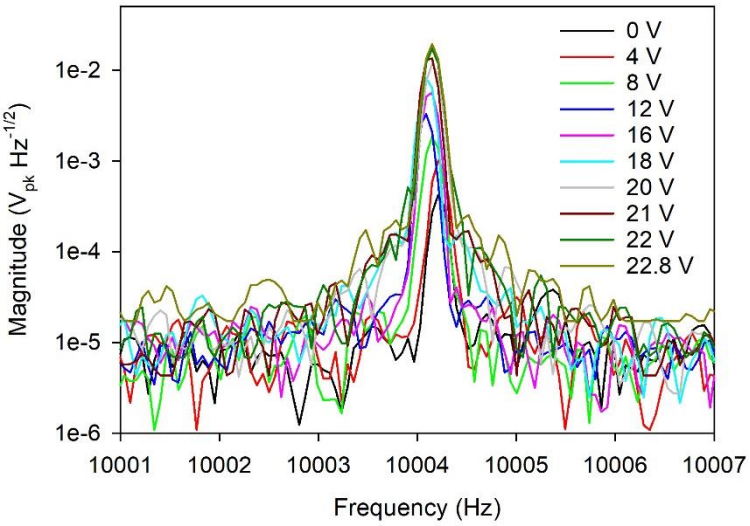

Figure 6.8 The frequency response spectra at varying voltage biases at a fixed laser injection power

The typical dark current and gain characteristics in the APDs tested for low-light level measurements are shown in Fig. 6.9. From equation 2.8, a dark current of 1 µA at -18 V translates to 0.64 pA/Hz$^{1/2}$ of shot noise. With comparison to the pre-amplifier input noise of 2 pA/Hz$^{1/2}$, the diode dark current cannot be considered negligible past a certain point. The gain is obtained from the peak signal magnitudes on the spectrum analyser (verified against the conventional method with a LIA to show similar levels of gain) and a maximum gain of 38 is obtained at -22.8 V bias.

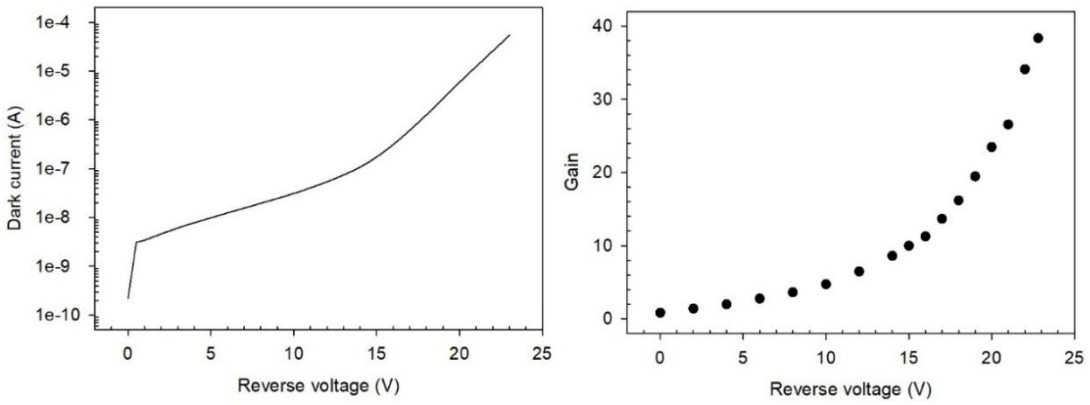

Figure 6.9 Typical dark current (left) and gain (right) characteristics at 77 K of APDs tested

The *SNR* is calculated by taking the square of the ratio of signal peak magnitude to the noise floor where the noise floor is calculated as the mean noise level without the signal peak and its associated spectral leakages to adjacent signal bins. A plot of *SNR* to gain is shown in Fig. 6.10 where it can be seen clearly that the *SNR* increases with the gain. The observed trend is in line with the excess noise theory of materials with $k = 0$ as discussed in chapter 2.2. In other conventional APD materials such as InP [20] and InAlAs [21], the increase in gain is accompanied with increase in the avalanche noise due to the random occurrence of impact ionisation events in the high field region. This is not the case for InAs as the excess noise is limited to a theoretical maximum of 2 by McIntyre's local model [22] (while experimental results suggest it is in actual fact less than 2 due to dead space effects [23]). Hence, from a *SNR* point of view, using a material with only a single ionising carrier can further minimise the APD noise while still providing signal amplification. A noise figure meter (NFM) can be used to measure the excess noise of an APD. The noise contribution from photocurrent (as a function of bias voltage) can be extracted by subtracting the dark current shot noise from the total shot noise measured by the equipment. By modifying equation 2.8 to consider only shot noise due to photocurrent, the excess noise, *F*, can be determined. Additionally, for noise measurements, impedance matching is critical in ensuring the measurement accuracy and it is not possible to implement GSG probing pads onto the linear array. Hence, the excess noise of the APD array was not measured in this work. Here, instead of the above mentioned method to derive the excess noise quantitatively, the *SNR* at different bias voltages is calculated using equation 2.8 by assuming $F = 2$ and a TIA noise of 2 pA/Hz$^{1/2}$. The calculated *SNR* is shown to agree qualitatively with the *SNR* derived from the spectrum analyser. In this set of measurements, the

photocurrent is intentionally set to be lower (by using a low laser power) than the device dark current such that the main shot noise contributor is the dark current.

Beyond a gain of 16 (at a reverse bias of 18 V), the rate of increment drops off significantly and the maximum *SNR* obtained is 62.8 dB at -22 V, after which the *SNR* begins to deteriorate. From Fig. 6.8, it can be seen that the overall noise floor on the spectrum analyser is raised by almost an order magnitude at -22.8 V as compared to the lower biases. Therefore, the deterioration in *SNR* is attributed to the dominance of shot noise from APD dark current over the system noise. Further increments in voltage bias offer no additional advantage when operating with high dark currents. Hence a structure with thicker intrinsic region (for a larger gain) or improved fabrication procedure to reduce the leakage current is required to improve the APD performance.

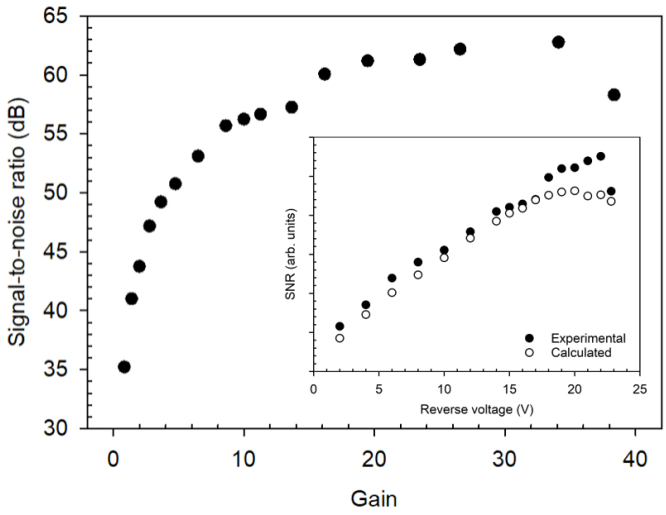

Figure 6.10 The signal-to-noise ratio as a function of APD gain. The inset shows the comparison between the *SNR* derived from spectrum analyser measurements and calculated from equation 2.8, using the photocurrent, gain, dark current data presented in the previous sections and assuming $F = 2$

The APD characteristics at varying optical power, ranging from 1 mW to 1 nW, under different voltage biases from 0 to -20 V are shown in Fig. 6.11. The optical powers denoted in the legends are the optical power from the laser settings for clear visual indication of the signal spectrum as a function of the optical power variation. As can be seen clearly, the lowest detectable power decreases as the applied bias increases due to the effects of APD gain. The lowest detectable power possible from the APD at a bias of -20 V combined with the measurement setup is approximately 7 pW (1 nW

from the laser settings) and the limiting factor in this set of measurement (up to -20 V, with *SNR* of 61.3 dB) is the system noise floor.

The dynamic range of a photodetector refers to the range of input optical power of which the output response is linear. In photodiodes, the photocurrent may become saturated and non-linear at high optical power levels and the lowest power measurable is limited by the diode noise. An array pixel with a large dynamic range will be able to discern between large variations in optical intensity to improve the image quality. The dynamic range of the APD used in the measurement setup in this work is 40 dB at unity gain and increases to 50 dB at a gain of 23.5. The upper limit is determined by the TIA input and the lower limit is determined by the overall system noise floor at low biases.

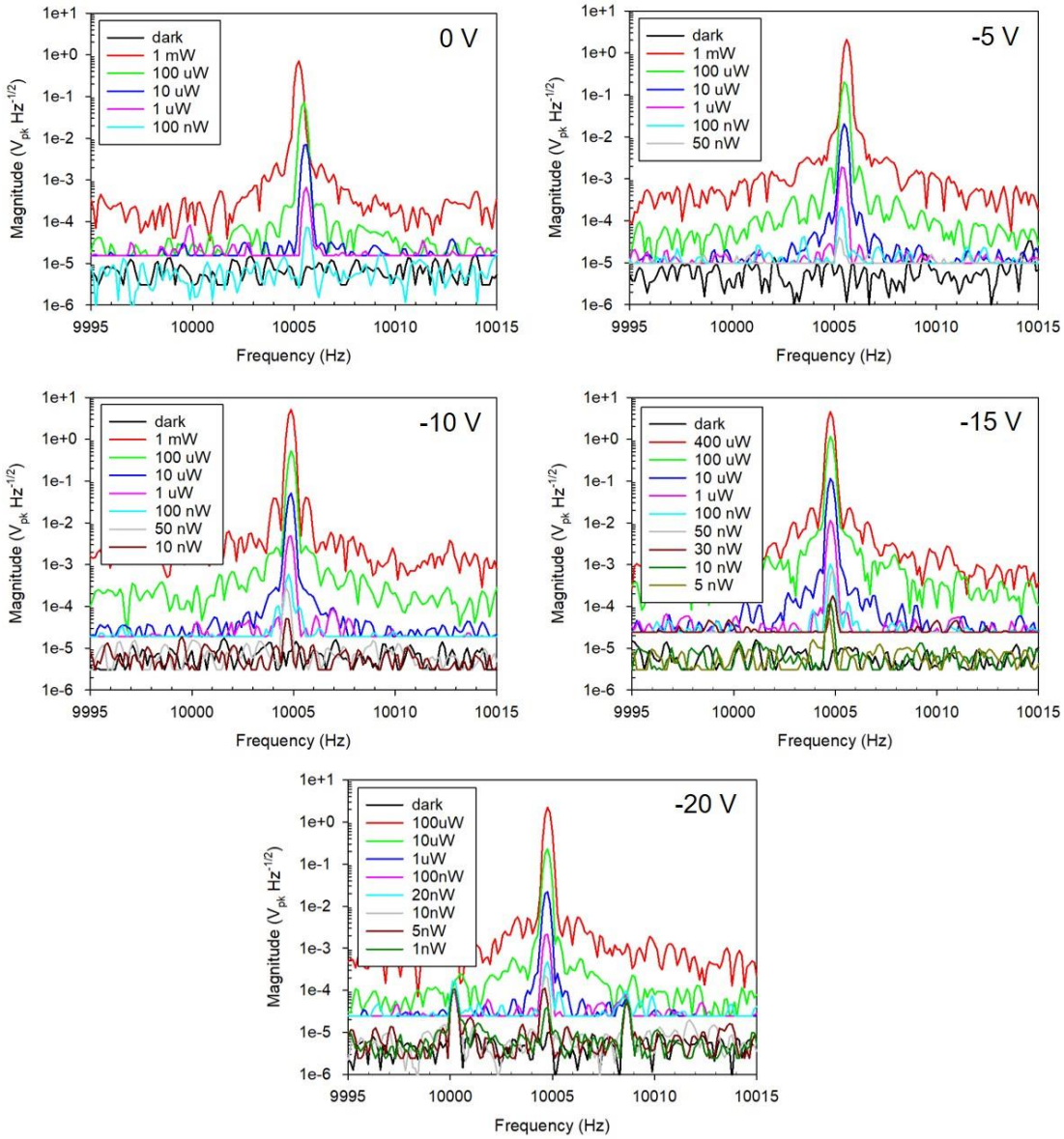

Figure 6.11 The signal spectra at varying optical power level (as noted from the laser settings) with the operating voltage bias denoted at the top right corner of each plot

The linearity of the system is illustrated more clearly in Fig. 6.12. The magnitude refers to the signal amplitude obtained by subtracting the signal peak by the noise floor. The noise floor is determined by taking a spectrum sweep in the dark, without the laser signal. The APDs show a linear trend between the peak signal magnitude and input optical power at various voltage bias. As mentioned previously, the lowest detectable power from the measurements is 7 pW and this corresponds to a photon count of roughly 2700.

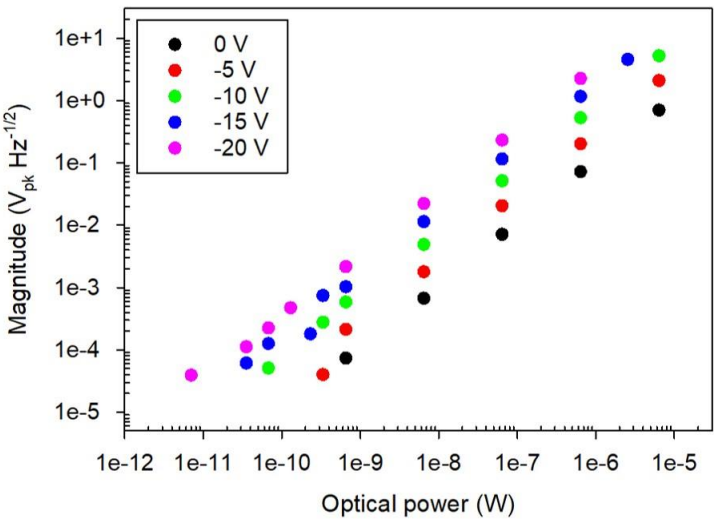

Figure 6.12 The linearity of response to light at varying voltage bias

6.5 Small area diodes with isolation trench design

One method to lower the diode noise induced by diode leakage currents is to reduce the size of the diode. However in doing so, the diode photosensitive area will reduce and subsequently the photocurrent signal generated will decrease. Furthermore, surface currents become a major concern in small area devices due to the decreased area to perimeter ratio. Therefore there is a tradeoff between the signal-to-noise ratio. To circumvent the problem effectively, while the number of diodes can be increased, the pixel pitch should also be minimised to maximise the coverage area of incident light. Isolation trenches etched between adjacent diodes can be used to provide diode-to-diode isolation with a smaller spacing in-between to improve the packing yield of the diodes in a fixed area.

Two sets of small area diodes, nominally 30 µm by 30 µm in length and width, are fabricated. In one set, the radius of curvature of the implanted area is varied from 0 to 5 and 10 µm with a diode spacing of 15 µm as per the APD array to investigate breakdown characteristics. In the other set, the radius of curvature varies similarly to the first set, but a 3µm wide isolation trench was etched in between adjacent diodes and the diode-to-trench distance is varied. This is illustrated in Fig. 6.13 where the specific distances are detailed and is also presented in Table 6-II. The first and second set of diodes are denoted with the letters ‘D’ and ‘T’ respectively. The isolation trenches are produced by ICP dry etching for 4 minutes to an approximate depth of

1 µm using a combination of 15 sccm of Cl_2, 15 sccm of CH_4 and 15 sccm of H_2 at an RF and ICP power of 150 and 1500 W, respectively.

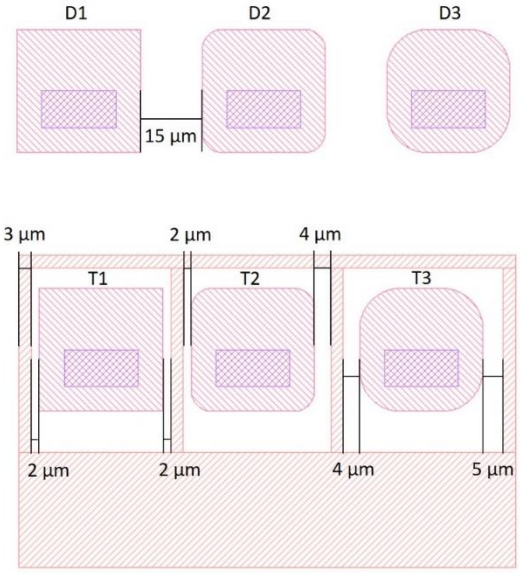

Figure 6.13 Mini array of 3 small area diodes of 30 µm 30 µm with 15 µm spacing (top). Detailed diode to trench spacing on mini array with isolation trench incorporated (bottom)

Table 6-II Details of mini arrays

Set	Diode	Radius of curvature (µm)	Spacing to isolation trench (left/right) (µm)	Total spacing to adjacent diode (left/right) (µm)
D	D1	0	-	15
	D2	5	-	15
	D3	10	-	15
T	T1	0	2 / 2	- / 7
	T2	5	2 / 4	7 / 11
	T3	10	4 / 5	11 / -

The room temperature and 77 K I-V characteristics are shown in Fig. 6.14 (left) and Fig. 6.14 (right), respectively. The diodes from set D, regardless of the radius of curvature, appears to have very similar and uniform (from the small error bar) I-V characteristics up to -5 V at room temperature. In set T, three randomly selected T1 and T2 diodes show premature edge breakdown at various applied bias. However, the I-V performance of T3 diodes appears to conform to the I-V characteristics of set D diodes at room temperature.

At 77 K, set D diodes, again show rather uniform I-V characteristics, which indicates that the surface current contribution may be minimal. However, in contrast to the I-Vs from the APD array, the error bars become larger at high voltage bias. Significant degradation in I-V characteristics are seen in set T diodes, with a rapid increase in current from 0 to -2 V followed by a slight, gradual increase until -20 V, signifying dominant surface leakage. The origin of the surface leakage component is likely to be due to damages to the crystal lattice from the dry etching process [24]. For InAs, a material with low resistivity due to a narrow band gap, the electric field may extend laterally to the vicinity of the etched sidewalls, thereby having increased current contributions from shunt paths along the plasma-damaged sidewalls.

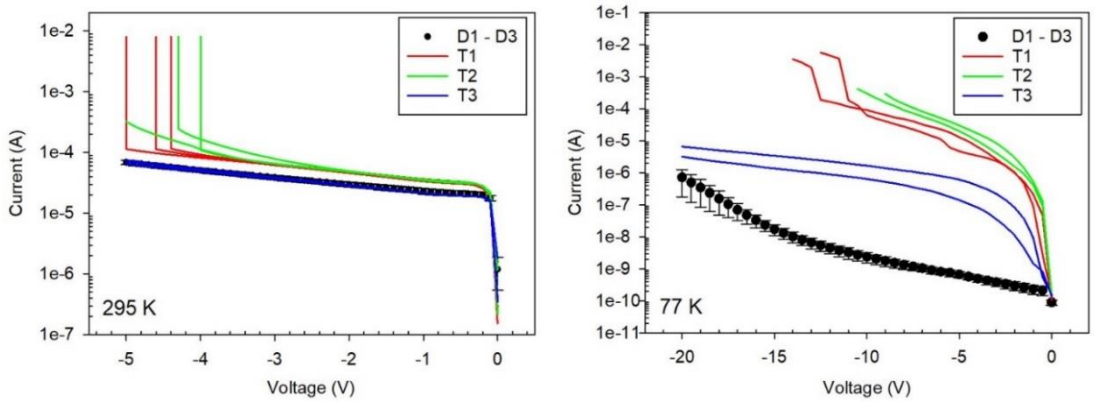

Figure 6.14 Reverse current-voltage characteristics at room temperature (left) and 77 K (right) of diodes from mini array with (D) and without (T) isolation trench

Fig. 6.15 highlights the difference in I-V characteristics from a D3 and a T3 diode at different temperatures from room temperature to 200 and 77 K. The T3 diode shows higher levels of dark current and premature edge breakdown (except for 77 K) when compared to D3. While the results show significant deterioration in I-V characteristics brought on by etching isolation trenches, it is still early at this stage to rule out the benefits isolation trenches might bring. Further design iterations on the trenches are required in changing the width of the trench as well as testing different diode to trench spacing. Undesirable surface damage in InAs is known to occur from low temperature PECVD (even at 100 °C), it is therefore unsurprising to see the negative effects from ICP dry etching in the diodes tested. A potential implementation of isolation trench could include a wet etch process and subsequent passivation after the dry etch process,

however the lateral etch undercut should be accounted for when designing such structures in the future.

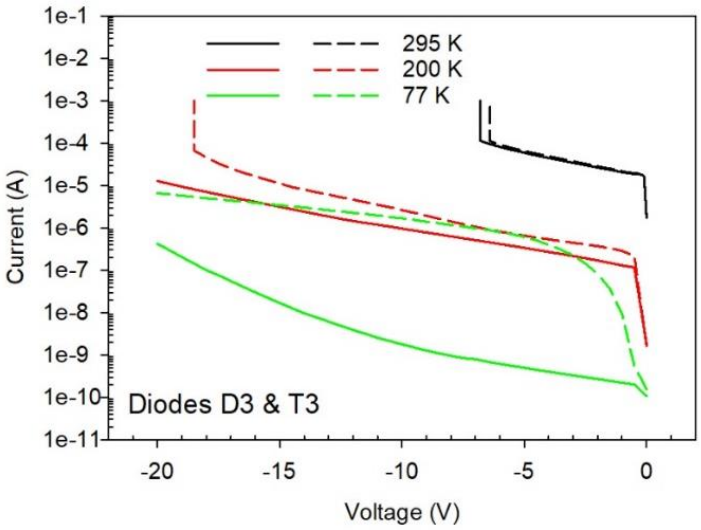

Figure 6.15 Temperature dependence of current-voltage characteristics of selected D3 and T3 diodes

6.6 APD array characteristics after thermal cycles

A major concern in practical semiconductor devices is the failure rate and lifetime of devices. Typically, a burn-in test is conducted by manufacturers to detect early failures among a set of devices by subjecting to a combination of stress tests such as operating at high currents and temperatures over prolonged periods up to hundreds of hours or ramping the temperature at a certain rate for a number of cycles [25], [26]. These failure analyses aim to not only screen out defective products but also to understand mechanisms in which devices would deteriorate and to rectify such problems in subsequent growth or fabrication procedures.

In this work, the robustness of the APD array is tested by investigating the device I-V performance before and after devices going under stress. The reverse I-V characteristics of 15 devices before and after going through multiple measurements and a total of 20 thermal cycle events down to 77 K over a period of 1 month are shown in Fig. 6.16. The cooling rate is set to roughly 2 K/min and warming rate is roughly 12.3 K/hour. A slow cooling/warming rate is used to reduce the likelihood of device degradation due to the difference in thermal expansion coefficient between the various films and materials. It should be noted however, each device is tested to different

extents, either from repeated I-V sweeps and gain measurements or high biases over a period of 30 to 60 minutes during low light measurements using the spectrum analyser.

It can be seen that initial I-Vs prior to any stress tests from -1 to -10 V are a few factors lower than the I-Vs post-stress tests and that the difference in both plots reduces, eventually converging at high voltage biases. The standard deviations of the device I-V post-stress test are also more consistent. While the sample size is not significant and the failure mode test is not extensive, it does however indicate that the planar InAs APD array is sufficiently robust to withstand the multiple thermal cycles without device failures.

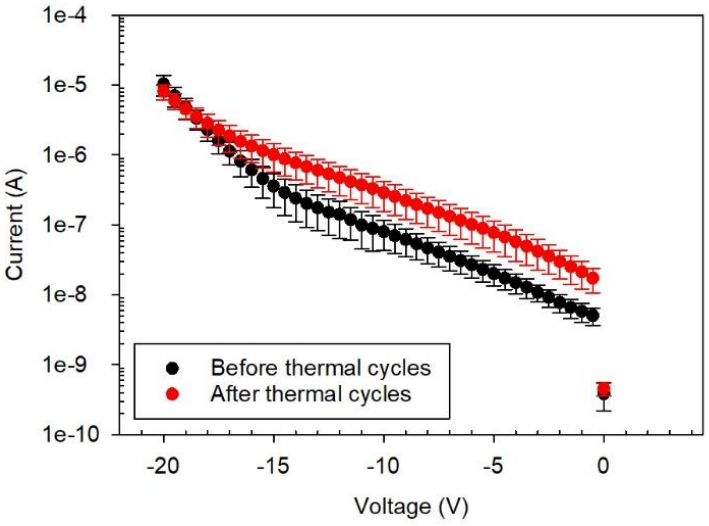

Figure 6.16 Comparison of reverse current-voltage characteristics at 77 K before and after multiple thermal cycles

6.7 Conclusion

A linear array of planar InAs APDs has been demonstrated with good uniformity in terms of dark current and gain characteristics. The dark currents reduces with temperature and at high voltage biases are limited by tunnelling current breakdown due to a thin intrinsic region. From the Arrhenius plot at -0.5 V, an activation energy of 0.23 eV is extracted from 295 to 200 K, which indicates the current mechanisms may be a mix between diffusion and generation-recombination current.

At temperatures of 200 and 77 K, gains of 22.5 at -15 V and 26 at -20 V are measured, respectively. The temperature dependence characteristics of gain follows past observations made in InAs APDs in which gain at a fixed voltage reduces with

temperature. However, it is accompanied by reductions in the dark currents therefore low temperature operation can still be beneficial for an improved *SNR*. The highest gain obtained in the APD array is 38 (at a voltage bias of -22.8 V) at 77 K. The maximum *SNR* achieved is 62.8 dB at -22 V as the diode noise begins to dominate over the system noise at larger voltage biases. The lowest detectable optical power of 7 pW (corresponding to a total number of 2700 photons) and a dynamic range of 50 dB is obtained at -20 V.

Small area diodes of nominally 30 µm by 30 µm in size, more inclined towards pixel sizes found in commercially available FPAs, were found to exhibit uniform I-V characteristics without much contribution from surface leakage. Isolation trenches etched between the small area diodes appear to result in non-ideal I-V such as inconsistent edge breakdown and increased dark current which is attributed to dry etch damage. I-V characteristics of the APD array show devices are sufficiently robust as minimal degradation has been observed after a month of testing with up to 20 thermal cycle events.

6.8 References

[1] X. Sun, J. B. Abshire, J. D. Beck, P. Mitra, K. Reiff, and G. Yang, 'HgCdTe avalanche photodiode detectors for airborne and spaceborne lidar at infrared wavelengths', *Opt. Express*, vol. 25, no. 14, p. 16589, Jul. 2017, doi: 10.1364/OE.25.016589.

[2] R. Tobin, A. Halimi, A. McCarthy, M. Laurenzis, F. Christnacher, and G. S. Buller, 'Three-dimensional single-photon imaging through obscurants', *Opt. Express*, vol. 27, no. 4, p. 4590, Feb. 2019, doi: 10.1364/OE.27.004590.

[3] G. M. Williams, 'Optimization of eyesafe avalanche photodiode lidar for automobile safety and autonomous navigation systems', *Opt. Eng.*, vol. 56, no. 3, p. 031224, Mar. 2017, doi: 10.1117/1.OE.56.3.031224.

[4] J. A. Overbeck, M. S. Salisbury, M. B. Mark, and E. A. Watson, 'Required energy for a laser radar system incorporating a fiber amplifier or an avalanche photodiode', *Appl. Opt.*, vol. 34, no. 33, p. 7724, Nov. 1995, doi: 10.1364/AO.34.007724.

[5] F. Laforce, 'Low noise optical receiver using Si APD', San Jose, CA, Feb. 2009, p. 721210, doi: 10.1117/12.809071.

[6] N. Z. Hakim, B. E. A. Saleh, and M. C. Teich, 'Signal-to-noise ratio for lightwave systems using avalanche photodiodes', *J. Light. Technol.*, vol. 9, no. 3, pp. 318–320, Mar. 1991, doi: 10.1109/50.70006.

[7] C. H. Tan, A. Velichko, L. W. Lim, and J. S. Ng, 'Few-photon detection using InAs avalanche photodiodes', *Opt. Express*, vol. 27, no. 4, p. 5835, Feb. 2019, doi: 10.1364/OE.27.005835.

[8] B. S. White *et al.*, 'High-Gain InAs Planar Avalanche Photodiodes', *J. Light. Technol.*, vol. 34, no. 11, pp. 2639–2644, Jun. 2016, doi: 10.1109/JLT.2016.2531278.

[9] P. J. Ker, A. R. J. Marshall, A. B. Krysa, J. P. R. David, and C. H. Tan, 'Temperature Dependence of Leakage Current in InAs Avalanche Photodiodes', *IEEE J. Quantum Electron.*, vol. 47, no. 8, pp. 1123–1128, Aug. 2011, doi: 10.1109/JQE.2011.2159194.

[10] V. K. Surana, N. Bhardwaj, A. Rawat, Y. Yadav, S. Ganguly, and D. Saha, 'Realization of high quality silicon nitride deposition at low temperatures', *J. Appl. Phys.*, vol. 126, no. 11, p. 115302, Sep. 2019, doi: 10.1063/1.5114927.

[11] A. Sukach, V. Tetyorkin, G. Olijnuk, V. Lukyanenko, and A. Voroschenko, 'Cooled InAs photodiodes for IR applications', Warsaw, Poland, Sep. 2005, p. 59571A, doi: 10.1117/12.622195.

[12] V. V. Tetyorkin *et al.*, 'p^+-InAsSbP/ n -InAs photodiodes for IR optoelectronic sensors', Warsaw, Poland, Sep. 2005, p. 59570Z, doi: 10.1117/12.622181.

[13] O. Breitenstein, P. Altermatt, K. Ramspeck, M. A. Green, J. Zhao, and A. Schenk, 'Interpretation of the Commonly Observed I-V Characteristics of C-SI Cells Having Ideality Factor Larger Than Two', in *2006 IEEE 4th World Conference on Photovoltaic Energy Conference*, Waikoloa, HI, 2006, pp. 879–884, doi: 10.1109/WCPEC.2006.279597.

[14] A. Chandra and L. F. Eastman, 'Rectification at n-n GaAs:(Ga, Al)As heterojunctions', *Electron. Lett.*, vol. 15, no. 3, pp. 90–91, 1979.

[15] J. M. Shah, Y. L. Li, T. Gessmann, and E. F. Schubert, 'Experimental analysis and theoretical model for anomalously high ideality factors ($n \gg 2.0$) in

AlGaN/GaN pn junction diodes', *J. Appl. Phys.*, vol. 94, no. 4, pp. 2627–2630, 2003.
[16] A. Chitnis *et al.*, 'High-quality p – n junctions with quaternary AlInGaN/InGaN quantum wells', p. 4.
[17] P. J. Ker, 'Development of high speed low noise InAs electron avalanche photodiodes', University of Sheffield, Sheffield, U. K., 2012.
[18] A. R. J. Marshall, J. P. R. David, and C. H. Tan, 'Impact Ionization in InAs Electron Avalanche Photodiodes', *IEEE Trans. Electron Devices*, vol. 57, no. 10, pp. 2631–2638, Oct. 2010, doi: 10.1109/TED.2010.2058330.
[19] A. R. J. Marshall, P. Vines, P. J. Ker, J. P. R. David, and C. H. Tan, 'Avalanche Multiplication and Excess Noise in InAs Electron Avalanche Photodiodes at 77 K', *IEEE J. Quantum Electron.*, vol. 47, no. 6, pp. 858–864, Jun. 2011, doi: 10.1109/JQE.2011.2128299.
[20] L. J. J. Tan, J. S. Ng, C. H. Tan, and J. P. R. David, 'Avalanche Noise Characteristics in Submicron InP Diodes', *IEEE J. Quantum Electron.*, vol. 44, no. 4, pp. 378–382, Apr. 2008, doi: 10.1109/JQE.2007.914771.
[21] Y. L. Goh *et al.*, 'Excess Avalanche Noise in $\hbox{In}_{0.52}\hbox{Al}_{0.48}\hbox{As}$', *IEEE J. Quantum Electron.*, vol. 43, no. 6, pp. 503–507, Jun. 2007, doi: 10.1109/JQE.2007.897900.
[22] B. E. A. Saleh, M. M. Hayat, and M. C. Teich, 'Effect of dead space on the excess noise factor and time response of avalanche photodiodes', *IEEE Trans. Electron Devices*, vol. 37, no. 9, pp. 1976–1984, Sep. 1990, doi: 10.1109/16.57159.
[23] P. J. Ker, J. P. R. David, and C. H. Tan, 'Temperature dependence of gain and excess noise in InAs electron avalanche photodiodes', *Opt. Express*, vol. 20, no. 28, p. 29568, Dec. 2012, doi: 10.1364/OE.20.029568.
[24] Z. H. Ye *et al.*, 'Investigations on a Multiple Mask Technique to Depress Processing-Induced Damage of ICP-Etched HgCdTe Trenches', *J. Electron. Mater.*, vol. 42, no. 11, pp. 3164–3167, Nov. 2013, doi: 10.1007/s11664-013-2697-6.
[25] J. Jung, Y. H. Kwon, K. S. Hyun, and I. Yun, 'Reliability testing of single diffused planar InP/InGaAs avalanche photodiodes', in *27th Annual IEEE/SEMI International Electronics Manufacturing Technology Symposium*, pp. 193–194.
[26] M. Kobayashi, T. Shirai, and T. Kaneda, 'High reliability planar InGaAs avalanche photodiodes', in *International Technical Digest on Electron Devices Meeting*, Washington, DC, USA, 1989, pp. 729–732, doi: 10.1109/IEDM.1989.74158.

Chapter 7 Conclusion

InAs has been established as one of the APD materials, other than HgCdTe, to have the single carrier multiplication property where only electrons initiate impact ionisation events. This brings about remarkable APD properties where high gain (that is exponentially proportional to the depletion width), high bandwidth (due to the absence of avalanche feedback from holes) and low noise (more deterministic impact ionisation events) can be achieved. Past work in InAs APDs by Marshall and Ker focused on producing and optimising mesa diode devices. Numerous etch recipes and sidewall passivation schemes have been investigated and mesa diodes with bulk properties have been demonstrated. However, at low temperatures, surface leakage suppression remains an unresolved issue where mid-gap defect states acting as G-R centres are found. Not only that, it is often experimentally observed that device failure was imminent after a number of thermal cycle events. It may be possible due to delamination of dielectrics and SU-8 from differences in thermal expansion coefficients, leading to the fact that temperature ramping must be controlled at a slow rate which may be impractical in application.

To circumvent the issues in mesa diodes, planar design diodes can be implemented which in principle should promise simpler fabrication processes from having a relatively flat sample surface during processing and also the suppression of surface leakage from mesa sidewalls. This can be achieved by diffusion or ion implantation where the latter has been investigated extensively in the works by White *et al*. A double implantation scheme of Be-ions at 70 and 200 keV to achieve the desired dopant distribution profile and its accompanying post-implant anneal at various temperatures were tested to produce high gain planar InAs APDs with performance, in terms of I-V and gain, comparable to mesa devices.

One downside to the planar APDs is the dark currents that are an order magnitude larger than that in mesa APDs, which was thought to be an artefact of implant damage from the high energy implantation. Therefore, in this work, a relatively low Be-ion implantation carried out with an energy of 34 keV was used to form p-doping in InAs. Simulations carried out by SRIM shows that the implantation conditions used will yield a peak dopant concentration at approximately 100 nm. Long duration anneals at 500 °C of 15, 30 and 60 minutes on blanket implanted samples were assessed. SIMS

measurements were conducted to determine the actual dopant profile post-annealing. It was found that the distribution of dopants was similar regardless of the annealing duration and that the peak concentration reduced post-annealing, which can be explained by the out-diffusion of Be ions through the SiO_2 encapsulant. The results from SIMS corroborate findings from I-V and responsivity measurements performed on mesa diodes fabricated from the different duration annealed samples where the dark current densities and responsivities from each sample are near identical. A 15 minutes anneal was deemed sufficient to manifest diode rectification characteristics and applied to a sample with implantation windows.

Planar diodes produced show sufficiently bulk-dominated I-V characteristics at room temperature, comparable in magnitude to mesa diodes from the blanket implanted sample. However, the responsivity was found to be lower and surface treatment by HF or shallow etching was employed in an attempt to recover the surface condition. A factor of 3 reduction in dark current and 1.4 times increase in responsivity can be attained by shallow etches to various depths ranging from 100 to 417 nm. The planar diodes (prior to surface treatment) show spatial responsivity that is comparable to commercial photodiodes from Hamamatsu and Judson Teledyne. To evaluate the possibility of producing arrays of planar diodes, a series of diodes with varying spacings to adjacent diodes was tested to find that the dark currents reaches an asymptotic minimum beyond a 15 μm spacing.

Using the findings above, a planar array mask set and the subsequent fabrication procedures was designed and developed as a preliminary study to array format InAs planar APDs. Mesa APD arrays have previously been demonstrated [1], and this was repeated to compare against the planar APD array. Various issues plaguing the fabrication of mesa arrays, especially in SU-8 passivation, have been documented. In terms of dark currents, while the planar diode array show magnitudes almost an order higher than that of mesa diode array, the standard deviations at any voltage biases are significantly smaller. Moving forward towards the practical applications of InAs APDs, the benefits offered from the simplicity and consistency in planar diodes possibly outweigh the performance benefit of mesa diodes as the higher dark currents of planar diodes can be reduced by means of low temperature operation.

The linear array of planar InAs APDs is subsequently tested at low temperatures where the I-V uniformity of up to 87 diodes are evaluated at various temperatures, gain of 15 diodes were measured at 200 and 77 K and the optical response linearity is tested on a number of devices. An activation energy of 0.23 eV was extracted from the total dark current, indicating a combination of bulk diffusion and G-R currents. Average gains of 22.5 at -15 V and 26 at -20 V are obtained at 200 and 77 K, respectively. The SNR is found to increase with voltage bias (and gain) up until -22 V, beyond that, becomes limited due to the high dark currents. The overall system response is linear across 50 dB of input optical power, ranging from 7 μW (limited by the maximum laser power with -20 dB attenuator) to 7 pW (lowest detectable optical power). The lower limit of measurement is found to be constrained by the system noise. Mini arrays of 30 μm by 30 μm diodes (also with isolation trenches) were also fabricated to investigate the dark currents in devices with a high perimeter-to-area ratio and isolation trenches are incorporated into diodes in an attempt to reduce the pixel separation distances. The I-Vs show close uniformity in small area diodes with no isolation trenches and the diodes with trenches show significantly increased I-Vs, possibly due to dry etch damages near the diodes. APDs from the array show minor degradations in I-Vs after up to 20 thermal cycles and multiple high voltage measurements. While simple in design of experiment, this does show that planar InAs APD array is sufficiently robust for repeated measurements.

7.1 Future work

7.1.1 Experimental work

The laser spot, estimated to be less than 80 μm by 80 μm (from measuring the coupling efficiency of diodes to a reference diode in section 6.2), prevented measurements of crosstalk behaviour in the linear array. To characterise the crosstalk effects more precisely, an optical setup with a laser spot size smaller than the device size is required which can be achieved by incorporating lensed fibres into the cryogenic probe station to give spot sizes <5 μm. This will be able to provide insights to the collection of lateral diffused photogenerated carriers outside the implanted region, thereby establishing more accurate effective diode area after the annealing procedure. Furthermore, the spatial uniformity of gain can be evaluated to assess any local electric field hotspots for future optimisation of the planarisation process. Localised electric field hotspots

can be determined by raster scanning across *xy* space using a short wavelength laser which will be absorbed near the p-i interface. This is possible since the carrier multiplication process depends on the electric field and given that the localised electric fields near junction edges are higher than the active absorption window, the measured gain near the junction edges may be higher, thus revealing the presence of electric field hotspots.

7.1.2 Improvements to mask design

With regards to the array mask set, diodes of varying sizes are required to assess the leakage currents as a function of area-to-perimeter ratio and to distinguish the bulk and surface components more accurately from the total combined dark currents. In pursuit of fast signal read-out with ROIC integration, test structures for bond pad designs can be implemented to measure the parasitic capacitance; especially since the device capacitance scales with device area and for small area array pixels, the bond pad capacitance may become the limiting factor in speed performance.

Active dopants introduced into the semiconductor lattice can give rise to mid-gap defect states, useful for carrier trapping and to produce semi-insulating behaviour [2]. One of such example is Fe-doped semi-insulating InP substrate [3] commonly used for high speed photodiodes [4]. This effect may be useful in providing isolation between devices without compromising the planarity. Implantation-induced device isolation has been demonstrated in in AlGaN/GaN HEMTs [5] and GaAs/AlGaAs HBTs [6]. For a narrow band gap material like InAs, the sheet resistance is thought to be small due to the high intrinsic carrier concentration in the i-region, resulting in poor diode-to-diode isolation in a planar topology. Following a multi-energy He-ion implantation and annealing scheme, the sheet resistivity in the p-type InAs has been shown to increase [7]. Similarly, this technique could be adopted to improve the diode isolation in a planar array and the sheet resistance can be measured by a series of transmission line measurement pads of varying distances. Aside from that, the inclusion of a lattice matched wide band gap material such as $Al_xGa_{1-x}As_ySb_{1-y}$, $Ga_xIn_{1-x}As_ySb_{1-y}$ or $In_xAl_{1-x}As_ySb_{1-y}$ on InAs can in principle, offer a high resistivity layer that can reduce the lateral spread of electric field in planar devices. For example, a mobility of 3800 $cm^2/V^{-1}s^{-1}$ in undoped $In_{0.5}Al_{0.5}As_{0.56}Sb_{0.44}$/InAs heterostructures has been

reported [8] which is approximately 6 to 7 times lower than the electron mobility of InAs and therefore, a higher resistivity can be expected.

The preliminary design of planar diode array used in this work can be further improved through various methods. Instead of changing the pixel-to-pixel spacing, isolation trenches of different widths and distance to adjacent pixels can be optimised to minimise leakage currents from ICP dry-etched sidewalls. Various aspect ratio between the trench width and etched depth should be examined to test the process limitations by dry etching. While dry etching in InAs has been tested [9] and shown to give reasonably vertical sidewall profiles, but for high aspect ratio features as in isolation trenches, the etching process may become diffusion-limited and result in undesirable sidewall profile. Alternatively, to avoid plasma-induced damages from dry etching, wet etching is an option for isolation trench etching. However, the pixel pitch will be compromised due to the lateral etching. In either case, to reduce carrier crosstalk, the etched sidewalls will require passivation to terminate dangling bonds. Mini arrays, rather than a large linear array, should be employed to investigate test structures incorporating various trench designs. Unlike silicon which enjoys the luxury of reliable TCAD models (which can range from modelling accurate electrical behaviour of silicon-based devices with optical stimulations to process simulation of fabrication steps for semiconductor devices), InAs like many other III-V optoelectronic materials are currently built upon using a trial-and-error approach due to the lack of scrutiny in the validity of physical models employed in TCAD simulations for less known semiconductor materials.

In order to package linear arrays onto PCB-friendly headers, the bond pads need to adopt a fan-out pattern with relatively long bond pad track designs. Couple the long tracks and a connecting wire running from the bond pads to the header pins, additional RC components will need to be factored in, further slowing down signal acquisition speeds. Also, from an imaging system perspective, linear arrays add a layer of complexity due to the need for a scanning system to form coherent images. To circumvent these issues, 2-D arrays can be implemented. Instead of typical ball bonding techniques, 2-D arrays are integrated with a ROIC by flip-chip bonding. This bypasses the need for a connecting wire and instead relies on direct interfacing to the external circuitry via indium bumps, which can reduce the system capacitance [10]. Not only will the device layout require slight modifications, for InAs, the device

structure will require significant overhaul as well. A back illumination scheme is usually used for flip-chip hybridised arrays. For infrared materials like HgCdTe that is grown on CdZnTe or Si substrates and T2SL structures grown on GaSb or InAs substrates, the substrate is usually optically transparent to the wavelengths of interest. Therefore any long wavelength light will pass through the substrate and be absorbed only in the intended layers. However, for homo-epitaxial InAs APDs, incoming signals from substrate side will be attenuated due to absorption in the substrate. To minimise the signal reduction, a substrate removal process involving mechanical lapping and chemical polishing of relatively brittle InAs substrates needs to be developed and a wide band gap blocking layer lattice matched to InAs such as $Al_xGa_{1-x}As_ySb_{1-y}$ will be required to block out photogenerated minority carriers from the substrate. $AlAs_{0.16}Sb_{0.84}$ blocking layers have been incorporated into early designs of InAs APDs to mitigate leakage current from thermionic emissions. Further to that, a n-on-p design is needed for electron-initiated impact ionisation in the high field region, meaning instead of selective area p-doping via Be-implantation or Zn-diffusion, an n-type dopant such as Si is required.

7.1.3 Surface passivation of InAs APDs

Despite having made numerous efforts in recent works to minimise the surface currents in InAs [9], [11], [12], surface leakage mechanisms remain a bane to optimising InAs APD performance. As demonstrated in this work, surface currents can cause variations in pixel-to-pixel dark current performance in an array at low temperatures despite having attempted to minimise the time of exposure of the sample surface post native oxide removal. Chalcogenide-based (group-VI elements) passivation on III-V semiconductors, in particular sulphur, has been extensively tested as a means to decrease III-V semiconductor surface states by replacing III-O and V-O with III-S and V-S bonds instead [13]. Sulphur passivation has been demonstrated successfully on InAs and InAs-containing superlattices [14], [15], showing effective removal of native oxides and a reduction in dark current. The choice of using inorganic or organic sulphur-containing is up for debate as it is generally believed that organic –thiol type self-assembling sulphide layers are more stable than inorganic forms of sulphur such as ammonium sulphide and sodium sulphide [16]–[18]. Whilst the benefits of sulphur passivation are well-established, it is also known that the effects are not last-lasting, where surface re-oxidation occurs after long term exposure to ambient environment

thermal treatments, or illumination [19], [20] and the time period varies laboratory to laboratory. One method to counteract the eventual loss of sulphide bonds is to perhaps encapsulate the sulphur-terminated surfaces with a polymer coating [21] such as SU-8 or polyimide coatings.

An alternative option for passivation of III-V semiconductor materials is by atomic layer deposition (ALD) of high-κ dielectrics, such as Al_2O_3, TiO_2 and HfO_2. ALD functions by alternately filling and purging the process chamber of precursor gases to form a thin self-limiting layer [22]. The ALD process relies on the dissociative adsorption of CH_3-metal atom and the subsequent chemisorption of oxides on the metal at the surface. Hence, a relatively low temperature can be used and high energy plasmas are not required which makes it suitable to passivate InAs surfaces. Furthermore, it has been reported that the ALD process produces a 'self-cleaning' effect, reducing surface states due to native oxides at the semiconductor edge interface by formation of wide band gap metal-oxides instead [23], [24]. The formation of high-κ oxides by the ALD process has been explored in InAs metal-oxide-semiconductor devices in hopes to achieve a suitable insulator-semiconductor interface for high speed, low power transistor operation [25]–[27]. Aside from that, in InAs-containing superlattice structures, ALD of Al_2O_3, TiO_2 and HfO_2 have been demonstrated to suppress dark currents in photodetectors [28].

A concept of wide band gap material as a passivation material was demonstrated by Rehm *et al.* in InAs/(GaIn)Sb T2SL by epitaxial growth of a layer of relatively wide band gap $Al_xGa_{1-x}As_ySb_{1-y}$ after device mesa etching to suppress the surface currents [29]. The conceived idea is known as epitaxial overgrowth which promises reduction in surface leakage currents. However, in practice, the passivation scheme is difficult to implement with limited literature available due to the need of careful surface treatment prior to epitaxial overgrowth and the selection of complicated ternary or quaternary III-V materials to ensure lattice matching [30]. An alternate approach is to apply the epitaxial overgrowth technique using II-VI semiconductor materials with small differences in lattice constants to III-V semiconductors. This is one major theme in Butera's work on InAs APDs, where binary and ternary II-VI materials such as ZnSe, CdS, ZnTe, CdMgSe and ZnSeTe were investigated and agreeable current densities at room temperature were observed in ZnSe and ZnTe-passivated APDs [31].

It is thought that the larger resistivity in the II-VI layer suppresses surface leakage currents similar to observations in T2SL materials.

7.2 Reference

[1] I. C. Sandall, S. Zhang, and C. H. Tan, 'Linear array of InAs APDs operating at 2 μm', *Opt. Express*, vol. 21, no. 22, p. 25780, Nov. 2013, doi: 10.1364/OE.21.025780.

[2] S. J. Pearton, 'Ion Implantation for Isolation in III-V Semiconductors', *Mater. Sci. Rep.*, vol. 4, pp. 313–367, 1990.

[3] J. P. Donelly and C. E. Hurwitz, 'High-resistivity layers in n-InP produced by Fe ion implantation', *Solid-State Electron.*, vol. 21, pp. 475–478, 1978.

[4] K. Li, E. Rezek, and H. D. Law, 'InGaAs pin photodiode fabricated on semi-insulating InP substrate for monolithic integration', *Electron. Lett.*, vol. 20, no. 5, p. 196, 1984, doi: 10.1049/el:19840130.

[5] J.-Y. Shiu *et al.*, 'Oxygen Ion Implantation Isolation Planar Process for AlGaN/GaN HEMTs', *IEEE Electron Device Lett.*, vol. 28, no. 6, pp. 476–478, Jun. 2007, doi: 10.1109/LED.2007.896904.

[6] R. G. Elliman *et al.*, 'Single-energy, MeV implant isolation of multilayer III-V device structures', *J. Appl. Phys.*, vol. 71, no. 2, pp. 1010–1013, Jan. 1992, doi: 10.1063/1.350436.

[7] I. Sandall, C. H. Tan, A. Smith, and R. Gwilliam, 'Planar InAs photodiodes fabricated using He ion implantation', p. 9, 2012.

[8] M. Kudo and T. Mishima, 'MBE growth of Si-doped InA1AsSb layers lattice-matched with InAs', *J. Cryst. Growth*, p. 5, 1997.

[9] A. R. J. Marshall, 'The InAs electron avalanche photodiode and the influence of thin avalanche photodiodes on receiver sensitivity', University of Sheffield, Sheffield, U. K., 2009.

[10] M. Makiuchi, M. Norimatsu, C. Sakurai, K. Kondo, N. Yamamoto, and M. Yano, 'Flip-Chip Planar GaInAs/InP p-i-n Photodiodes Fabrication and Characteristics', *J. Light. Technol.*, vol. 13, no. 11, p. 6, 1995.

[11] P. J. Ker, 'Development of high speed low noise InAs electron avalanche photodiodes', University of Sheffield, Sheffield, U. K., 2012.

[12] B. S. White, 'Planar InAs avalanche photodiodes for infrared sensing: Towards a true solid state photomultiplier', University of Sheffield, Sheffield, U. K., 2016.

[13] V. N. Bessolov and M. V. Lebedev, 'Chalcogenide passivation of III–V semiconductor surfaces', *Semiconductors*, vol. 32, no. 11, pp. 1141–1156, Nov. 1998, doi: 10.1134/1.1187580.

[14] E. Papis-Polakowska *et al.*, 'Novel approach to passivation of InAs/GaSb type II superlattice photodetectors', *Appl. Phys. B*, vol. 125, no. 12, p. 223, Dec. 2019, doi: 10.1007/s00340-019-7336-3.

[15] O. Salihoglu, A. Muti, and A. Aydinli, 'Thiol passivation of MWIR type II superlattice photodetectors', Baltimore, Maryland, USA, Jun. 2013, p. 87040T, doi: 10.1117/12.2015521.

[16] R. V. Ghita, C. C. Negrila, C. Cotirlan, and C. Logofatu, 'ON THE PASSIVATION OF GaAs SURFACE BY SULFIDE COMPOUNDS', p. 10.

[17] L. Zhou, B. Bo, X. Yan, C. Wang, Y. Chi, and X. Yang, 'Brief Review of Surface Passivation on III-V Semiconductor', *Crystals*, vol. 8, no. 5, p. 226, May 2018, doi: 10.3390/cryst8050226.

[18] D. K. Petrovykh, J. M. Sullivan, and L. J. Whitman, 'Quantification of discrete oxide and sulfur layeres on sulfur-passivated InAs by XPS', *Surf. Interface Anal.*, vol. 37, pp. 989–997, 2005.

[19] D. Y. Petrovykh, J. C. Smith, T. D. Clark, R. Stine, L. A. Baker, and L. J. Whitman, 'Self-Assembled Monolayers of Alkanethiols on InAs', *Langmuir*, vol. 25, no. 20, pp. 12185–12194, Oct. 2009, doi: 10.1021/la804314j.
[20] K. Banerjee, S. Ghosh, E. Plis, and S. Krishna, 'Study of Short- and Long-Term Effectiveness of Ammonium Sulfide as Surface Passivation for InAs/GaSb Superlattices Using X-Ray Photoelectron Spectroscopy', *J. Electron. Mater.*, vol. 39, no. 10, pp. 2210–2214, Oct. 2010, doi: 10.1007/s11664-010-1298-x.
[21] N. C. Henry *et al.*, 'Chemical and physical passivation of type II strained-layer superlattice devices by means of thiolated self-assembled monolayers and polymer encapsulates', *Infrared Phys. Technol.*, vol. 70, pp. 48–52, 2015.
[22] T. Gougousi, 'Atomic layer deposition of high-k dielectrics on III-V semiconductor surfaces', *Prog. Cryst. Growth Charact. Mater.*, vol. 62, pp. 1–21, 2016.
[23] C. L. Hinkle *et al.*, 'GaAs interfacial self-cleaning by atomic layer deposition', *Appl. Phys. Lett.*, vol. 92, no. 7, p. 071901, Feb. 2008, doi: 10.1063/1.2883956.
[24] C. Mittag *et al.*, 'Passivation of edge states in etched InAs sidewalls', *Appl. Phys. Lett.*, vol. 111, no. 8, p. 082101, Aug. 2017, doi: 10.1063/1.4986614.
[25] N. Li *et al.*, 'Properties of InAs metal-oxide-semiconductor structures with atomic-layer- deposited Al2O3 Dielectric', *Appl Phys Lett*, p. 4.
[26] R. Timm *et al.*, 'Reduction of native oxides on InAs by atomic layer deposited Al2O3 and HfO2', *Appl Phys Lett*, p. 4.
[27] J. Wu, E. Lind, R. Timm, M. Hjort, A. Mikkelsen, and L.-E. Wernersson, 'Al_2O_3/InAs metal-oxide-semiconductor capacitors on (100) and (111)B substrates', *Appl. Phys. Lett.*, vol. 100, no. 13, p. 132905, Mar. 2012, doi: 10.1063/1.3698094.
[28] O. Salihoglu, A. Muti, and A. Aydinli, 'A Comparative Passivation Study for InAs/GaSb Pin Superlattice Photodetectors', *IEEE J. Quantum Electron.*, vol. 49, no. 8, pp. 661–666, Aug. 2013, doi: 10.1109/JQE.2013.2267553.
[29] R. Rehm, M. Walther, F. Fuchs, J. Schmitz, and J. Fleissner, 'Passivation of InAs/(GaIn)Sb short-period superlattice photodiodes with 10 um cutoff wavelength by epitaxial overgrowth with Al_xGa_1-xAs_ySb_1-y', *Appl. Phys. Lett.*, vol. 86, p. 173501, 2005.
[30] E. A. Plis, M. N. Kutty, and S. Krishna, 'Passivation techniques for InAs/GaSb strained layer superlattice detectors: Passivation Techniques for InAs/GaSb SLS detectors', *Laser Photonics Rev.*, vol. 7, no. 1, pp. 45–59, Jan. 2013, doi: 10.1002/lpor.201100029.
[31] S. Butera, 'InAs avalanche photodiodes', Heriot-Watt University, Edinburgh, U.K., 2015.

Appendix A: Fabrication of InAs planar linear array

The fabrication procedures for producing planar InAs diodes can be categorised to several key processes, namely, to create alignment markers and prepare the sample for ion implantation, performing the implantation process and post-implant annealing, metal deposition, surface passivation with SU-8 and finally bond pad deposition. Each step is further detailed below and schematic diagrams for key steps are presented in Fig. A.1.

Step A: Creating alignment markers

A.1. Cleave a quarter section of a wafer.

A.2. Clean by immersing the wafer in warm n-butyl acetate followed by acetone and warm isopropyl alcohol (IPA) for 3 minutes each.

A.3. Deposit 35 nm of SiO_2 via plasma enhanced chemical vapour deposition (PECVD) as an encapsulating layer.

A.4. Pre-bake sample for 1 minute. Then spin hexamethyldisilazane (HMDS) followed by SPR220 on the surface. Bake the sample for at least 1.5 minutes. SPR220 is used to achieve a thick mask as plasma dry etching attacks photoresist at a fast rate.

A.5. Pattern with the 'Alignment Markers' layer. Then expose and develop for an appropriate duration.

A.6. Etch the alignment markers and isolation trenches using the InAs recipe on the inductively-coupled plasma (ICP) dry etching tool.

A.7. Clean the hardened photoresist using EKC830 photoresist remover. Warm EKC830 on a 100 °C hotplate if the photoresist is difficult to remove. If the photoresist persists, expose the sample to oxygen plasma with the barrel asher for 3 – 5 minutes then soak in EKC830, repeat until all photoresist is removed.

Step B: Preparing sample for ion implantation

B.1. Pre-bake sample for 1 minute. Then spin HMDS followed by SPR220 on the surface. SPR220 is used to ensure a mask thickness greater than the ion penetration depth.

B.2. *(optional)* For ease of aligning within tiny tolerances, perform photoresist edge bead removal. Expose one edge of the wafer at a time to UV light for at least 3 times the duration used for standard exposure. This is because the edge bead thickness can be 2 times or more taller than the intended photoresist thickness. Once all edges are exposed, immerse the sample in the developer solution until the edge bead is mostly removed. Edge beads in the corners may remain but should be shorter in height.

B.3. Pattern with the 'Implant Region' layer. Then expose and develop for an appropriate duration.

B.4. Package the sample tightly in a plastic membrane box and send the sample by post for ion implantation at selected vendor.

Step C: Metallisation

C.1. Upon receiving the sample, remove the hardened photoresist using EKC830. If difficulties in photoresist removal arise, refer to step A.7.

C.2. Anneal the sample using an appropriate annealing recipe.

C.3. Deposit 20 nm of Ti and 200 nm of Au as the back contact.

C.4. Remove the SiO_2 layer using a 10% HF clean for 30 seconds.

C.5. Pre-bake sample for 1 minute. Spin on PMGI and bake for 5 minutes followed by spinning SPR350 and baking for 1 minute. The bilayer photoresist stack ensures a cleaner liftoff for the top contact.

C.6. Pattern with the 'Top Contact' layer. Then expose and develop for an appropriate duration. For edge bead removal, refer to the optional step B.2.

C.7. Perform a plasma clean using the barrel asher.

C.8. Deposit 20 nm of Ti and 200 nm of Au as the top contact.

C.9. Soak the sample in acetone. Using a pipette, agitate the sample in the acetone bath for a clean liftoff.

C.10. Once a satisfactory liftoff has been achieved, remove the remaining PMGI layer with EKC830.

C.11. The sample can be now be characterised in the laboratory.

Step D: SU-8 passivation

D.1. Subject the sample to a 40% HF clean for 30 seconds to remove any native oxides. Immerse the sample in a beaker of DIW to prevent oxidation due to ambient air while transporting to the yellow room.

D.2. Blow dry and pre-bake the sample at 100 °C in the yellow room.

D.3. Dispense SU-8 2 and leave for 30 seconds. Spin at 500 rpm for 5 seconds then at 4000 rpm for 30 seconds.

D.4. Soft-bake the sample at 65 °C for 1 minute and then at 95 °C for 3 minutes.

D.5. Pattern with the 'SU8' layer and expose the sample for 2 seconds on the UV300 mask aligner. Edge bead removal is not performed for SU-8.

D.6. Post-exposure bake at 65 °C for 1 minute, then at 95 °C for 1 minute.

D.7. Develop the sample in EC solvent for 1 minute. Stir the sample during this step.

D.8. Rinse the sample with a separate beaker of EC solvent or IPA for 1 minute.

Step E: Bond pad deposition

E.1. Deposit an appropriate thickness of SiN_x. The SiN_x functions both as an insulating layer for the bond pads and anti-reflection coating (ARC).

E.2. Pre-bake sample for 1 minute. Spin HMDS followed by SPR220 on the surface. Bake the sample for at least 1.5 minutes.

E.3. Pattern with the 'SiN etch' layer. Then expose and develop for an appropriate duration. For edge bead removal, refer to the optional step B.2.

E.4. Etch away SiN_x in unwanted regions using the reactive ion etcher (RIE).

E.5. Clean the hardened photoresist using EKC830 photoresist remover. If difficulties in photoresist removal arise, refer to step A.7.

E.6. Pre-bake sample for 1 minute. Apply HMDS followed by a bilayer photoresist stack of PMGI and SPR350 on the sample.

E.7. Pattern with the 'Bondpad' layer. Then expose and develop for an appropriate duration. For edge bead removal, refer to the optional step B.2.

E.8. Perform a plasma clean using the barrel asher.

E.9. Deposit 40 nm of Ti and 400 nm of Au for the bond pads. To achieve a high bond pad yield, position the sample in the evaporation chamber such that the metal vapour has a direct line of sight on areas hard to reach (see ‘metal deposition and liftoff’ section in Appendix B).

E.10. Soak the sample in acetone. Using a pipette, agitate the sample in the acetone bath for a clean liftoff.

E.11. Once a satisfactory liftoff has been achieved, remove the remaining PMGI layer with EKC830.

E.12. Array fabrication is now complete.

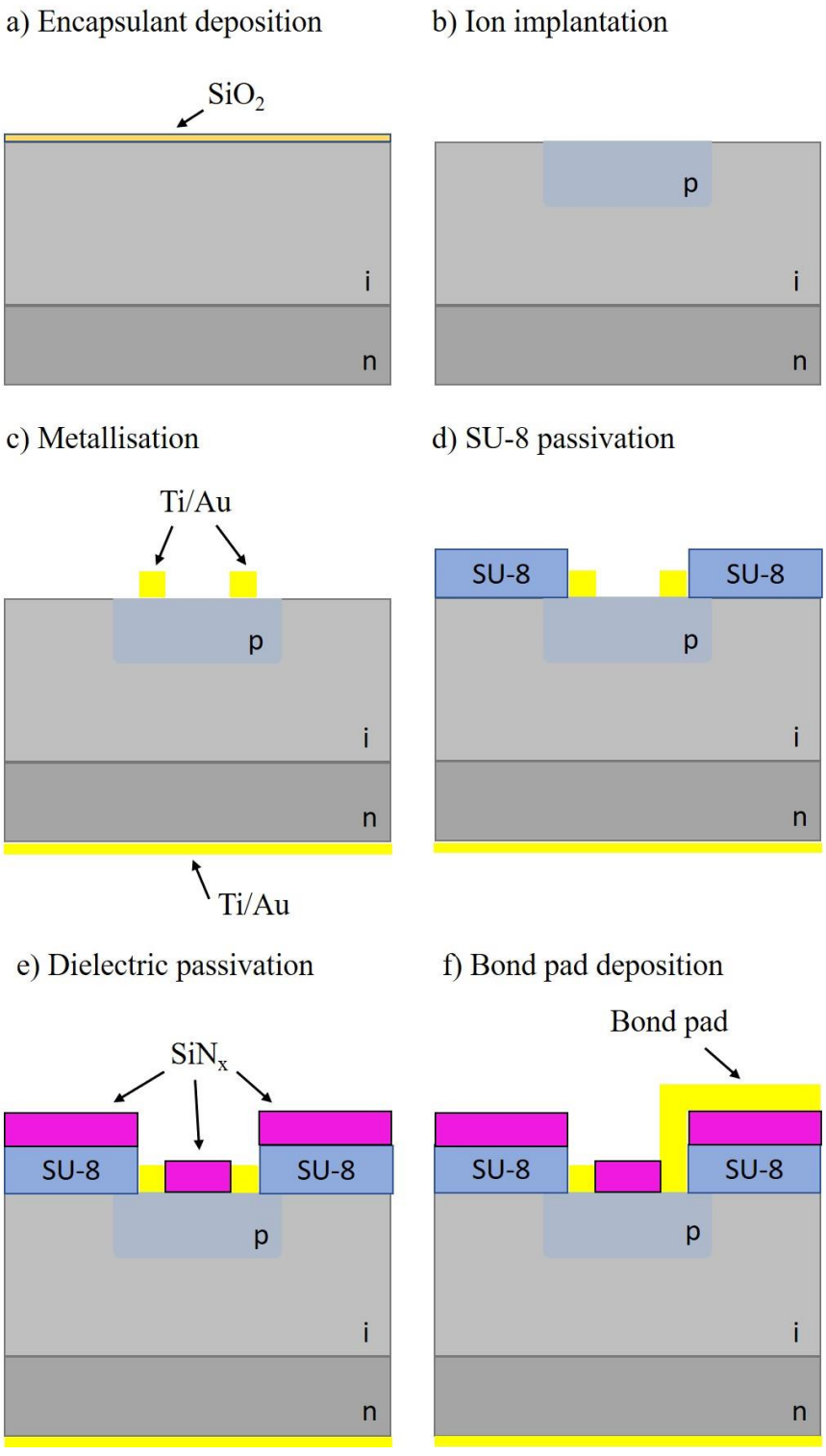

Figure A.1 Schematic diagrams for several key steps in the fabrication of planar InAs linear array diodes

Appendix B: Cleanroom fabrication methods and techniques

Brief descriptions of the working principles and mechanism behind cleanroom equipment and processes are provided to gain an understanding in device fabrication within a cleanroom environment. A cleanroom is a facility where the cleanliness (number of particulates within a cubic metre), humidity, temperature and pressure are controlled to carry out specialised scientific processes sensitive to environmental factors such as semiconductor manufacturing.

Cleaving and 3 stage cleaning:

Semiconductor surfaces can be easily contaminated through atmospheric exposure leaving behind particles and residues attached by electrostatic and intermolecular forces and lowering the final yield. Prior to any processing, solvent cleaning should be carried out to remove contaminants from sample surfaces. Solvent cleaning is performed in a number of stages, with each solvent targeting different types of contaminant. To remove organic contaminants and oil residues, n-butyl acetate and acetone is used. Further to that, acetone can also strip most photoresists. Due to the fast evaporation rate of acetone, the sample should be rinsed in isopropyl alcohol (IPA) to prevent acetone drying streaks. While acetone is miscible in both water (water is also a good solvent) and IPA, IPA is preferred to water due to lower surface tension forces to leave behind a residue and solvent-free surface.

Photolithography:

Photolithography is the process of transferring an intended pattern from a photomask onto the sample by exposing a coating of photosensitive polymer (photoresists) to ultraviolet (UV) wavelengths. The sample is then submerged in a developer solution to remove the photoresist. Photoresists can be classed into positive or negative photoresists, where exposed positive photoresists become soluble in developer solutions while negative photoresists become insoluble in developer solutions upon exposure.

A photolithography process for patterning metal contacts is shown in Fig. B.1. The process of photolithography starts off with cleaning the semiconductor surfaces of organic and inorganic contaminants. The sample is then heated to remove any surface moisture as any adsorbed water molecules will decrease the adhesion of photoresists onto wafer samples. This causes lifting during the development process. Also, dielectric layers become polar surfaces after exposure to ambient air. To improve the adhesion, the surface can be primed by applying adhesion promoters, such as hexamethyldisilazane (HMDS). The HMDS-treated surface becomes hydrophobic by bonding with the surface oxygen atoms, leaving the non-polar methyl group chain exposed for superior photoresist adhesion.

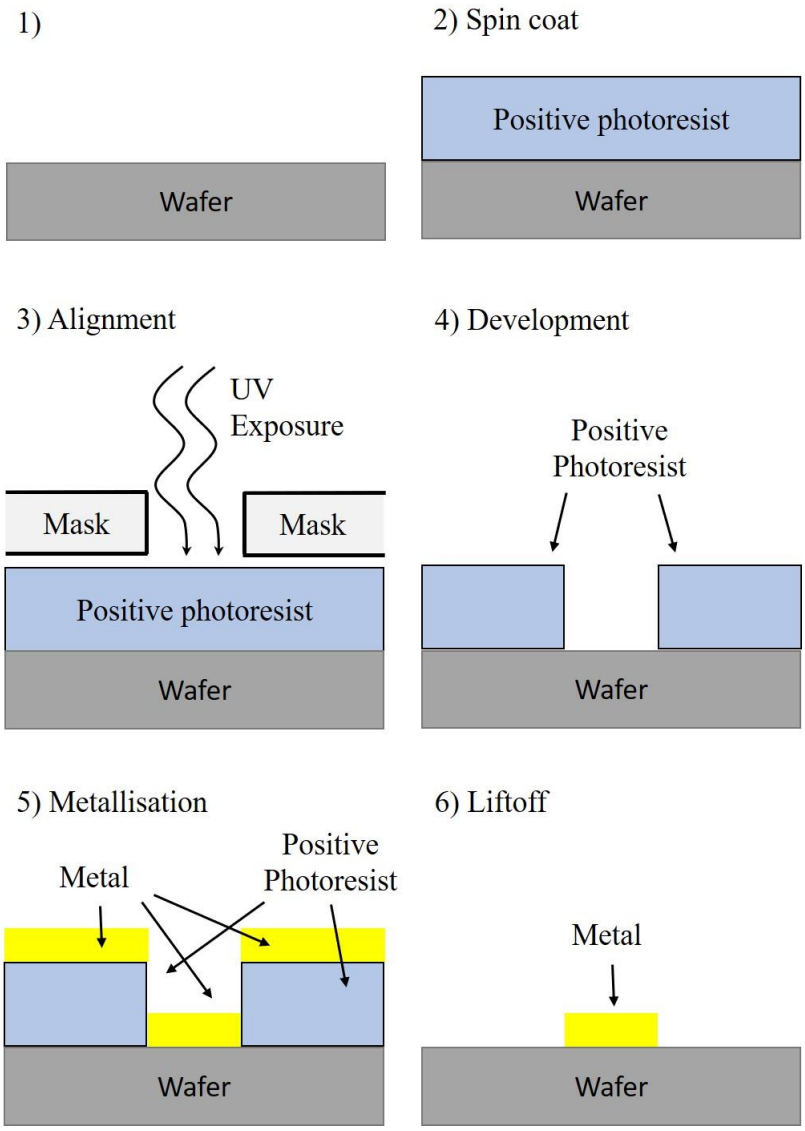

Figure B.1 A standard photolithography procedure from spin coating to metal liftoff on a wafer sample

Photoresist is dispensed and spread over the surface by spin coating. The final thickness of the photoresist is dependent to varying degrees by parameters such as viscosity of photoresist, spin duration, spin speed and solvent evaporation. The sample is subsequently placed on a contact hotplate for pre-baking to harden the photoresist by evaporating excess solvents bottom-up in the photoresist.

After baking, the sample is then loaded into a mask aligner and exposed to UV light upon contact with a photomask. To obtain a high precision and resolution of features, samples should be placed as close as possible to the photomask to prevent diffraction of light into areas unintended for exposure. Also, to maintain a good contrast across the depth of photoresist, a suitable exposure dosage (depending on UV bulb irradiance and exposure duration) must be used while avoiding over-exposure and the resultant widening or narrowing of features. The sample is then submerged in a developer solution to remove the unwanted areas of photoresists. For positive photoresists, photoacids created initiates a dissolution process in the exposed areas and become soluble in the developer solution. On the other hand, photoacids in negative photoresists initiate cross-linking between polymers and become insoluble post-exposure.

Edge bead formation is a phenomenon caused by the intrinsic surface tension of fluids where photoresists will form a bump at the edge of the sample (can be more than 10 times the nominal thickness). Edge bead causes issues in subsequent photolithography procedures such as loss of feature resolution by hindering tight contact between sample and photomask and ‘slipping’ due to uneven contact with the photomask due to irregular edge bead heights across the sample. The edge bead can be removed by covering the bulk of the sample and exposing the edges to UV light, followed by a developing process. Alternatively, solvents can be used to dissolve away the edge bead. The former is time consuming and the latter is difficult to control.

For permanent photoresist structures or for photoresists acting as a protection layer for subsequent processes, a post-exposure bake (PEB) can be performed to stabilise and harden the photoresist. However, disadvantages of a PEB include increased difficulty in resist removal, introduction of stress during baking, alteration of resist shape due to resist reflow. Certain processes such as ion implantation, plasma etching, and high

temperature exposure can harden photoresists therefore requiring photoresist strippers to dissolve highly cross-linked photoresists.

Metal deposition and liftoff:

Thermal evaporation is a thin film deposition method where the material for deposition (evaporant) is heated to its melting point and forms a cloud of vapour which moves across a vacuum chamber to coat the sample. The technique is commonly used to deposit metal contacts on semiconductor materials. Evaporants are loaded into coils or boats made of tungsten or molybdenum, used for their high melting point and subsequently heated by passing a large current. To monitor the deposition rate or final thickness, a quartz crystal thickness monitor is used.

Ultra-pure metals (purity >99.9%) are used as the evaporation source. The evaporant when used in a coil or basket can be thought of as a point source with the metal vapour emitted across the chamber radially where the deposited thickness is dependent on the angle between the source and sample plane and holds an inverse square relation with distance. This is illustrated in Fig. B.2. The liquid evaporants are able to vaporise more easily due to the high vacuum. Furthermore, a high vacuum in the chamber ensures a mean free path longer than the radial distance between the source and the sample plane for uniform coating and also mitigates the inclusion of impurities onto the sample.

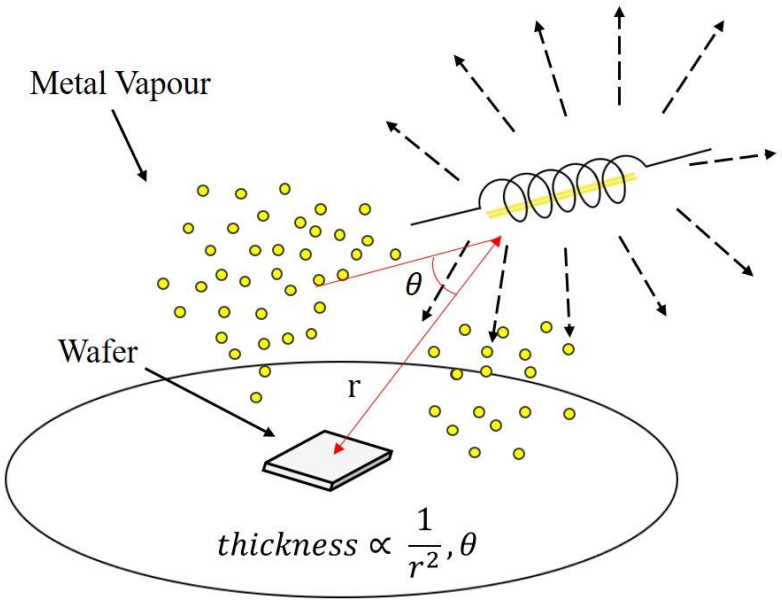

Figure B.2 A schematic diagram for a metal evaporation process

The most desirable metal contacts are low resistance ohmic contacts. Low resistance metal contacts are preferred for low power dissipation during high current measurements. For example, a high current is inevitable at near-breakdown voltages in an avalanche photodiode so a large resistance will not only limit the current but also produce a large voltage drop, resulting in erroneous measurements. To achieve an ohmic contact, the electron affinity of the semiconductor should ideally be larger than the work function of the metal. Alternatively, it is possible to artificially form an ohmic junction by doping the contact layer to degeneracy, commonly above 1×10^{19} cm^{-3}. The large amounts of dopants not only increases the conductivity due to a high concentration of carriers but also reduces the barrier width in a metal-semiconductor junction. The reduced barrier width increases the tunnelling probability of carriers and allows current flow in the forward and reverse direction, similar to an ohmic junction. Annealing post-evaporation can be utilised to improve the adhesion and quality of metal contacts.

For high quality metal contacts, the cleanliness of the deposition surface is of key importance. This can be achieved by exposing the sample to energetic oxygen radicals in a barrel asher to sputter off photoresist residuals and organic contaminants. Furthermore, the formation of thin metal-insulator-semiconductor junctions are possible due to native oxide present on the semiconductor surface. To avoid this, removal of native oxide can be performed via chemical etching prior to sample loading in the evaporation chamber. Similarly to achieve a high yield of bond pads, the dielectric surface should be kept as clean as possible.

Transmission line measurement is a method to determine the contact resistance of the metal-semiconductor junction and sheet resistance of the semiconductor surface layer. A series of metal pads with varying distances between adjacent pads are deposited and a resistance (that is the sum of two times the contact resistance, sheet resistance and system resistance) can be extracted by probing and measuring the current-voltage characteristics of adjacent pads. A plot of the resistance versus the separation distance of adjacent pads can be obtained where the gradient is the sheet resistance and the y-intercept is two times the contact resistance.

The diffusion of metal vapours onto the intended deposition area can be inhibited by tall features on the sample. This is known as the shadowing effect. This issue can be

alleviated by placing the sample directly underneath the evaporant source or arranging the metal coils at specific angles for greater coverage. To achieve a high liftoff yield, a combination of photoresists can be used such that the first photoresist layer forms an undercut due to isotropic developing. Solvents can then attack and liftoff the top photoresist layer with relative ease, leaving the intended areas of metallisation. Alternatively, photoresists which forms a negative bevel upon developing can improve the liftoff yield.

Chemical wet etching:

Chemical wet etching refers to the dissolution of semiconductor layers by means of immersing the semiconductor sample in a mixture of an acid/base, an oxidising agent and diluted with de-ionized water (DIW). The etching process is used to remove unwanted layers of semiconductor, for example native or surface oxide layers, narrow bandgap contact layer prone to high leakage currents, or to provide isolation between individual devices. The etching process involves a set of redox reactions, where the surface is first oxidised by the oxidising agent, followed by a reaction between the oxide and the acidic or basic reactant. The DIW acts as a diluting agent and also a medium to transport the etchants and by-products to and away from the sample.

Key figure of merits of etching include anisotropicity, etch rate and selectivity. The ideal etch is highly directional where the exposed semiconductor material is removed only top-down, creating vertical sidewalls and well-controlled features. However, most wet etches are isotropic, attacking the masked semiconductor areas horizontally as well, which creates an undercutting of the photoresist mask. This limits the feature sizes and must be accounted for during mask designing. Etch anisotropicity can be varied by exposing different crystallographic planes due to the difference in bonding energy. The etch rate is the etch depth per unit time and it can be controlled by varying the concentration of active reagents. Selectivity refers to the difference in etch rate between materials and is useful when designing etch stop layers where the vertical etching will be slowed down significantly upon reaching into the underlying layer (lateral etching will continue) and the process can be terminated. Wet etching will inevitably produce a variety of sidewall profiles as a combination of these factors.

Etching consists of three steps where chemical and physical interactions between the etch solution and semiconductor material occur. The slowest step becomes the rate-limiting factor of the etching process.

1. The etchants are transported to the semiconductor surface via diffusion due to a concentration gradient and adsorption occurs.
2. Chemical reactions occur on the surface and etch by-products in gaseous or aqueous state are formed.
3. Reaction products desorbed from the surface and are transported away from the surface by diffusion. Gaseous by-products may be carried away by convection (redox reactions are exothermic processes and releases heat).

A diffusion boundary layer forms between the bulk of the etchant solution and the semiconductor surface where etchants must diffuse through to move towards/away from the semiconductor. The etching process will be reaction rate limited if the diffusion boundary layer is small. The rate of reaction can be altered by changing the temperature and are described by the Arrhenius equation. For viscous solutions with high concentration of acid, diffusivity and mobility of etchants are low, causing the process to be diffusion limited. External agitation becomes necessary to assist the movement of etch reactants and products. The formation of air bubbles on the surface due to gaseous by-products can locally inhibit etch reactions and overall transport mechanics.

In a diffusion limited etch, a high concentration of reactants is trapped at the mask edge, producing a spatial variation in the etch profile where the mask boundary is etched deeper. Varying feature sizes and gaps between the mask can result in etch non-uniformity across the semiconductor sample due to different rate of reactants and products entering and leaving the reaction sites. Acidic reagents are preferred over basic reagents as photoresists are more easily attacked in basic solutions. Furthermore, the active reagent involved in the etch process can affect the choice of photoresists. For example fluoride ions in HF solutions can penetrate photoresists and attack the underlying surface which results in delamination of the photoresist, therefore a thicker photoresist film is required.

Passivation:

Semiconductor surfaces are saturated with dangling bond post etching and exposure to ambient air gives rise to surface oxidation, creating an unstable surface with a high concentration of surface states. Passivation involves applying a protective outer layer of material onto devices to prevent environmental degradation and increase long term reliability. Ideal passivation layers are thermally stable, chemically inert, have good electrical and mechanical properties and good adhesion to the semiconductor surface.

Passivation layers can serve other purposes such as planarising the sample surface, act as antireflection coating (ARC) and to provide electrical insulation. Tall or uneven structures can lead to process non-uniformity by impeding the movement of fluids such as photoresist and plasma tool gases. Bond pad tracks are also at risk of breakage at sharp interfaces or abrupt vertical steps. Hence, processing is simplified when working on a flat sample with little to no change in feature heights. Dielectric deposition such as SiN_x and SiO_2 can create an encapsulating layer for the exposed surfaces and also act as ARC to increase the transmission of specific wavelengths of light at the air-semiconductor interfaces. Furthermore, an insulating dielectric layer with good metal adhesion is required for bond pad deposition.

Dielectric deposition:

Plasma enhanced chemical vapour deposition (PECVD) is a process to deposit dielectric films on semiconductors. Precursor gases are fed into the deposition chamber and ionized using a high voltage RF (radio frequency) excitation to generate highly reactive plasmas. Chemical reactions between the active species of plasma occur and form film growth on the semiconductor. The use of plasma is advantageous to conventional thermal CVD processes due to the lower operating temperature (300°C compared to 600 - 800°C) possible for reactions to occur, leading to minimal degradation of semiconductor samples. Common examples of material deposited via PECVD are silicon dioxide (SiO_2) and silicon nitride (SiN_x) using silane (SiH_4) and nitrous dioxide (N_2O) or ammonia (NH_3) for dioxide and nitride respectively. Dielectric deposition in microfabrication serves several purposes such as isolation in multi-layer interconnects, surface passivation, encapsulating film for harsh processing environments, capacitor and hard mask, to name a few.

Dielectric films from PECVD can exhibit a wide range of optical (e.g. refractive index) and electrical properties (e.g. dielectric constant, breakdown voltage) depending various process parameters such as gas flow rates, ratios, RF power and frequency, chamber pressure and substrate temperature. PECVD systems vary from one to another and are therefore optimised upon installation. The substrate temperature, however, can be changed process to process and often reduced (to 100 - 150°C) to prevent device degradation. A low temperature process tends to create films with lower density due to decreased reaction rates and diffusion of radicals. This leads to higher porosity, faster etch rate, lower dielectric breakdown field, lower refractive index and higher mechanical stress.

The PECVD chamber should be prepared by pre-running the deposition process in an empty chamber and the sample surface should be solvent cleaned prior to minimise contamination to the dielectric film. For encapsulating films intended as a physical barrier in high temperature processing, a native oxide removal etch before deposition is advised to avoid thermal stress, cracking and dielectric film peeling due to differences in thermal expansion coefficient of different materials. In cases where it is undesirable for high temperature depositions, measures must be taken to prevent device failure such as to deposit a thicker film intended for insulation.

Ellipsometry is commonly used to measure the final film thickness. An ellipsometer typically comprises of a light source, polarisation generator, sample under investigation, polarisation analyser and detector. The sample's refractive index and thickness is indirectly determined by measuring the amplitude and phase change of the reflected polarised light (using the known incident polarised light as reference) after interacting at the sample surface. A model is then used to describe the measured data by calculating a predicted curve with estimated thicknesses and optical constants. The difference of the measured and calculated curve are presented as a Mean Squared Error (MSE), with a small MSE indicating a good model fit. A quick PECVD process run on a test sample followed by an ellipsometry measurement can be performed to determine the deposition rate for an accurate deposition thickness on the actual sample.

Plasma dry etching:

Plasma dry etching refers to the etching of exposed semiconductor materials by bombardment of reactive plasmas to dissociate the chemical bonds between surface atoms. A common type of dry etching is the capacitive coupled plasma reactive ion etching (CCP-RIE). The system typically consists of a vacuum chamber with an anode and a cathode plate. The plasma is generated by applying a RF voltage across the plates that leads to further ionisations when excited electrons collide with slow moving heavy ions. Positive ions accelerate towards the bottom negatively charged plate due to the difference in potential difference and carry out the etching process. Another type of dry etching is the inductively coupled plasma reactive ion etching (ICP-RIE) where high density plasma is generated by a separate source via electron-induced ionisations in a varying magnetic field. The ion densities can be controlled independent of the incident ion energy, giving more uniform etch. In general, dry etching processes can be varied by changing the gas flow ratios, RF power and chamber pressure.

This form of etching is more anisotropic, in contrast to wet etching, producing vertical sidewalls and high aspect ratio features, suitable for device size less than <1 μm. The directionality of etching is imparted from the strong unidirectional electric field effects on the positive ions. The presence of a vacuum ensures a long mean free path and minimal collisions in transit towards the surface, maintaining the directionality of incident collisions. The etch mechanism is a combination of chemical reactions by neutral atoms (isotropic) as well as the physical sputtering of materials by accelerated ions colliding with the surface (anisotropic). The physical aspect of etching by the ionic species consists of sputtering of surface materials as well as enhancing the chemical etching by breaking the chemical-surface bonds of the reactive neutral atoms.

A common problem with dry etching is the lack of selectivity between different materials. This causes an issue when using photoresist masks as the hydrocarbon bonds are easily broken, resulting in inaccurate pattern transfer and chamber contamination. Dielectrics or metals can be deposited as hard masks for better mechanical properties and etch selectivity but require complicated steps to produce a mask. During etching, the top of the trench is usually wider due to longer exposure to the etchants as compared to the bottom. To counteract this, the etched surface can be passivated by an inhibiting layer such as the formation of SiO_x in Si dry etching which protects the

underlying silicon from further etching. Due to the physical bombardment of high energy ions, the semiconductor post-etching is highly damaged and may require annealing or subsequent wet etching to recover the surface.

Packaging and bonding:

The purpose of bonding is to create a wire interconnect between the device metal contacts or bond pads to an external pin on a header. The process can be performed with a ball wire bonder using high purity gold as the bonding wire. The ball bonder brings the wire held in place by a ceramic capillary to the intended area of bonding and applies ultrasonic energy to melt and form a ball-shaped connection between the bonding wire and bonding pad. The capillary is then moved to the package pins and a wedge bond is created to complete the bonding process. To prepare for the subsequent bond, the electronic flame-off function melts and forms a spherical ball of a controlled diameter (known as the free air ball size, which determines the ball diameter of the first bond) at the end of the tail (length of wire spooled out of the capillary) using a high voltage.

Process parameters such as the sample holder temperature, ultrasonic power and duration, physical downward force of capillary and the free air ball size can be controlled to produce a reliable bond. The thermosonic (temperature and ultrasonic energy) bonding process creates a robust bond by deforming and encouraging interdiffusion of metals between the free air ball and bond pad. Bond failures such as ball-neck fractures, bond pad peeling, wire sagging, large ball size, non-sticking bond are complicated to resolve due to the various bonder parameters, environmental factor and sample preparation and different methods for rectification will be required. Hence, it is advised to keep good practices when processing devices intended for bonding as it is the final and most crucial step.

Ultrasonic energy from the bonding process poses a risk of device degradation hence metal pads intended for bonding should be deposited away from the device active area. For high quality bonding pads, surface cleanliness is of key importance, followed by the evaporation technique. The vacuum chamber condition and rate of deposition plays a more crucial role in obtaining good quality contacts. While thick bond pads are not required for successful bonding, it is encouraged to aim for a thickness of at least 400

nm of Au. This is to mitigate breakage of bond pad tracks along the features on the sample and to circumvent the shadowing effect during metal deposition. The sample when ready, can be mounted onto packages such as TO headers or ceramic packages by applying epoxy resins and hard curing in a convection oven.

Appendix C: Standard operating procedure for Janis 2 low temperature probe station

This section provides detailed instructions on the operation of a Janis low temperature probe station.

Step A: Filling liquid nitrogen dewar (can be performed while chamber is evacuated, will require help from another member of the laboratory)

A.1. The liquid nitrogen dewar requires refilling after roughly 70 hours of use at 77 K. There is also a constant leak rate of liquid nitrogen even without any use.

A.2. Unscrew the KF40 wing nut clamp at the dewar inlet. Place the clamp on a clean surface.

A.3. Unscrew and remove the transfer line at the chamber inlet. Place the tightening nut and O-ring on a clean surface.

A.4. Loosen the transfer line slowly to release the nitrogen gas. Beware of cold gas rushing out of dewar. Alternatively, open the pressure relief valve to slowly evacuate the nitrogen gas while removing the transfer line. Remember to close the pressure relief valve when done.

A.5. Remove the transfer line from chamber side. Then remove the transfer line from the dewar. Place the transfer line on the drying rack.

A.6. Blow dry and warm up the transfer line at the dewar side for at least 30 minutes or leave overnight. It is imperative to have the transfer line completely dry to prevent icing formation in the inner tube when the transfer line is re-inserted into the dewar.

A.7. While waiting for the transfer line to warm up, push the dewar to the liquid nitrogen tank outside the building and unlock the cage.

A.8. Equip all personal protective equipment (PPE) including face shield, an outer coat and insulated gloves.

A.9. Insert the transfer tube from the tank into the dewar and fill liquid nitrogen into the dewar.

A.10. When maximum capacity is reached, place the transfer tube back into the cage and lock it up. Push the dewar back into the laboratory carefully.

A.11. Insert the transfer line back into the dewar and tighten the clamp as quickly as possible. If the pressure builds up too quickly, open the pressure relief valve. A safety relief valve will also be triggered from excessive pressure built up. Insert the other end of the transfer line into the Janis chamber nitrogen inlet with the tightening nut and O-ring.

A.12. Allow the pressure to build up to roughly 4 psi on the pressure gauge at the liquid nitrogen dewar.

Step B: Sample loading and chamber evacuation

B.1. The chamber should be under a low vacuum by the previous user. This is the standby state of the Janis chamber to prevent contamination if kept at room pressure. Ensure the isolation valve between the chamber and pump is closed. Open the air admit valve and allow the chamber pressure to rise.

B.2. Close the air admit valve when the hissing sound has stopped completely as the hissing sound is an indication of air entering the chamber.

B.3. Unscrew the chamber windows (outer and inner) and place securely on the table with their respective screws and washers.

B.4. Load samples onto the copper chuck. Ensure that probe tips and optical fibres are far away to prevent accidental damage. Additional training are required before users are allowed to replace probe tips and optical fibres.

B.5. Make sure the probe tips and fibre has an adequate range of motion across the sample.

B.6. Once satisfied, secure the chamber windows to their respective positions. If needed, apply a thin layer of vacuum grease on the outer chamber window.

B.7. Assuming the pump has stopped operating for a long time and has cooled down, open the vent port at the turbopump to equalise the pressure at both ends of the isolation valve.

B.8. When done, close the vent port and open the isolation valve.

B.9. Switch on the turbo pump. The displayed pressure should be around 1e+3 mbar.

B.10. Press the second button (from the left) on the second row to enter the 'System Control' page.

B.11. Press the same button to activate the pump. To return to the home screen, press the first button on the second row.

B.12. The display screen should now show a decreasing pressure. This pressure gauge is located at the chamber side. Wait for the pressure to reach and stabilise at 2e+0 mbar. If the pressure is not decreasing, check if all vent ports/air admit valves/chamber window are tightly closed.

B.13. After 10 minutes, the turbopump will activate and the pressure should reduce quickly to 2 to 5e-5 mbar.

B.14. Turn on the penning gauge that is connected to the pump side when the turbopump is activated. It should read a value close to the pressure gauge on the pump.

Step C: Chamber cooling

C.1. The chamber pressure should be in the order of 1e-5 mbar before commencing cooling. To achieve this, it is best to leave the vacuum pump running overnight. The vacuum pump can be left to operate over prolonged periods of time.

C.2. Switch on the temperature controller.

C.3. Start the liquid nitrogen flow by turning the needle valve on the transfer line clockwise for 1.5 turns. This should give a cooling rate of roughly 1.2 K/min. Slow ramp rates are preferred to avoid damages to sample due to different thermal expansion coefficients between the semiconductor and any dielectric/polymer coatings or metal contacts.

C.4. On the temperature controlled, set a desired temperature and the heater will become active to maintain the temperature at setpoint. Note that the needle valve on the transfer line may require slight adjustments to ensure the cooling rate is less than the heater output at maximum.

C.5. Keep a periodic record of temperature and pressure readings in the logbook in case any situation out of the norm arises.

C.6. Carry out measurements needed at any temperature point. Remember to adjust the needle valve accordingly at any temperature point to avoid ice formation at the nitrogen outlet of the chamber.

C.7. For measurements over a prolonged duration (more than a day), close the needle valve at the end of the day. Switch off the temperature controller but leave the pump running.

C.8. Note down the total cooling time to provide a reference for when the liquid nitrogen dewar requires a refill.

Step D: Completing the measurements and removing sample

D.1. Close the needle valve on the transfer line when measurements are completed. Do not overtighten the valve. Also switch off the penning gauge.

D.2. Warm up the chamber either by using the heater or allow to warm gradually over time. Again, a controlled ramping time is preferred to avoid sample degradation. Leave the pump to be running during warm up. This is so that any outgassed contaminants can be evacuated by the pump.

D.3. Allow the chamber to stabilise at room temperature (read from the temperature controller) for 2 – 3 hours before venting the chamber. This is to ensure every part of the chamber has reached room temperature, not just where the thermocouple is connected to.

D.4. Switch off the pump and leave the pump to cool down. Close the isolation valve. Do not open the vent port at the pump or switch off the power at this time. It will cause damage to the pump.

D.5. Follow steps B.1 to B.6 to vent, open and then close the chamber (skipping B.4 and instead remove the samples from the chamber).

Step E: Standby state for Janis chamber

E.1. Follow steps B.7 to B.13 to evacuate the chamber to less than 1e-4 mbar.

E.2. Close the isolation valve and switch off the pump (when the turbopump comes to a halt).

Operating precautions

- Move probe tips and fibre far away from sample chuck when loading and positioning samples.
- Allow chamber to stabilise at room temperature (after operating at low temperature) for 2 – 3 hours before opening the chamber window. This is to avoid formation of condensation around parts of the chamber that are further from the temperature sensor.
- Leave the turbopump on when heating up the chamber. This is so any outgassed material can be removed by the pump.
- Never open air admit valve at pump side immediately after power off. Allow 1 – 2 hours for the blades to cool down.
- Do not switch off the mains power when turbopump (both Pfeiffer and Edward turbopumps) is slowing down. It will trigger an error message.
- Do not work alone when handling liquid nitrogen transfer arm and refilling dewar.

Troubleshoot

Issue	**Recommended solution**
Poor device contact when using back contact (I-V sweep not smooth or SMU reading is not stable)	Use the other probe arm to push the sample down. *or* Probe tip may be bent. Replace with a new tip.
Drop in pressure is slow after switching pump on	Check for hissing sounds around air admit valves/vent ports and chamber window. Close the valves or re-apply vacuum grease (only a thin layer is required) around o-rings and perimeter of the window plate.
Broken fibre (verify with a 633 nm laser)	Cleave fibre using appropriate tools. Beware of glass sharps. Dispose into sharps bin.
Pfeiffer HiCube turbopump cannot reach maximum speed	Purge moisture out of pump by following instructions from Appendix A on Janis I standard operating procedure.

Appendix D: Operating principle of a lock-in amplifier

The LIA utilises a method known as phase-sensitive detection (PSD) which requires a reference signal, generated from a phase-locked-loop circuit and an external modulation frequency. Given two signals, the input as $V_{sig}\ \sin(\omega_s t + \theta_{sig})$ and the reference as $V_{ref}\ \sin(\omega_r t + \theta_{ref})$, both signals are multiplied to obtain a product with two frequency components where one is the difference in frequency and the other is the sum of frequency as seen below.

$$V_{PSD} = \frac{1}{2} V_{sig} V_{ref} \cos\big([\omega_s - \omega_{ref}]t + \theta_{sig} - \theta_{ref}\big) - \frac{1}{2} V_{sig} V_{ref} \cos\big([\omega_s + \omega_{ref}]t + \theta_{sig} + \theta_{ref}\big) \quad \text{(D.1)}$$

By passing this signal through a low pass filter and since $\omega_s = \omega_{ref}$, the PSD output simplifies to the following where a DC signal directly proportional to the amplitude is obtained.

$$V_{PSD} = \frac{1}{2} V_{sig} V_{ref} \cos\big(\theta_{sig} - \theta_{ref}\big) \quad \text{(D.2)}$$

Broadband noise signals are processed similarly by the LIA. However, the generated signals corresponding to frequencies of $\omega_{noise} - \omega_{ref}$ and $\omega_{noise} + \omega_{ref}$ are easily eliminated by the low pass filter. Only noise close to the reference frequency will appear as small signals attenuated by the filter with the attenuation factor dependent on the bandwidth and roll-off. To remove the phase dependence, a second PSD circuit with a 90° phase-shifted reference signal is used to generate an output of $V_{PSD2} = \frac{1}{2} V_{sig} V_{ref} \sin\big(\theta_{sig} - \theta_{ref}\big)$. The outputs from both PSDs represent a vector where the vector magnitude is the signal amplitude and is phase independent.

The modulated optical signal can be represented by a train of rectangular pulses with 50/50 duty cycle. By Fourier transform, any square wave is comprised of a series sum of sine waves with frequencies that are odd multiples of the fundamental frequency, which in this case is the modulation frequency. The LIA reference signal is multiplied onto all the sine waves. However, since only a signal of frequency equivalent to the reference will produce a DC output signal, the LIA will ignore the other sine components. As a result, the measured signal will have an amplitude that is a factor of $2/\pi$ (by Fourier transform of the pulse train waveform) smaller than the amplitude

of the square wave. Furthermore, the LIA displays the magnitude in units of rms voltage. Therefore, the relation between the lock-in amplifier reading and the peak photovoltage can be expressed as in equation D.3. The photocurrent produced by the diode is subsequently derived as equation D.4.

$$V_{LIA} = \frac{1}{\sqrt{2}} \times V_{input} = \frac{1}{\sqrt{2}} \times \frac{2}{\pi} \times V_{pk} \tag{D.3}$$

$$I_{ph} = \frac{V_{LIA}}{0.45 \times R_{sense}} \tag{D.4}$$

Appendix E: Supplementary Results for Chapter 6

The following results are supplementary to the representative array data presented in Chapter 6.

The measurements are performed with the following settings on various equipment: SR570 transimpedance amplifier on low noise mode with a sensitivity of 10 μA/V, with no filters, SR760 FFT spectrum analyser with 24.4 Hz span, 8 averages, PSD and auto-range are on, HP8164A tunable laser source of 1550 nm operating at 10 kHz and 500 nW of optical power with a 20.5 dB fixed attenuator attached to the laser output port.

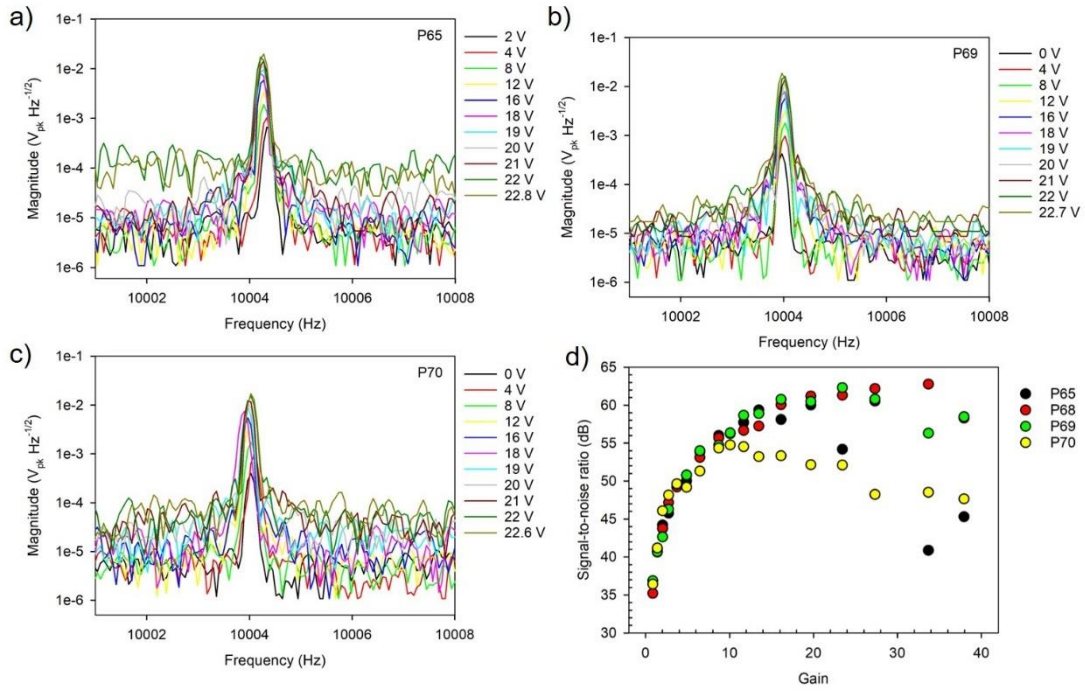

Figure E.1 (a) – (c) Spectrum analyser plots with a fixed incident optical power at varying voltage biases. (d) SNR vs gain plot where P68 is the data presented in chapter 6