Next Generation Silicon MOS-gated Bipolar Power Devices

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ABSTRACT

This thesis is devoted towards the development of next-generation silicon-based MOS-gated bipolar power devices. It focusses on reducing power losses and increasing power density of a MOS-gated thyristor device, namely the Clustered Insulated Gate Bipolar Transistor (CIGBT), taking due account of its device physics and modern optimisation techniques such as 3-D scaling rules presented for IGBTs.

The 3-D scaling rules for the cathode and gate regions of both trench and planar CIGBT structures are proposed and investigated using numerical simulations. Scaling down results in an enhancement of inherent thyristor action which reduces the forward voltage drop by 30 % at 125 °C. Most importantly, the short-circuit capability is maintained in the scaled CIGBTs. Moreover, an approach to enable the short-circuit capability of narrow-mesa IGBTs is demonstrated through TCAD simulations.

A hybrid power switch combining the bipolar current conducting capability of a MOS-gated thyristor device with the superior switching performance of a SiC MOSFET is demonstrated through experiments. Compared to the conventional trench CIGBT, a 45 % reduction in turn-off losses can be achieved by the hybrid device at 150 °C.

The on-state performance limits of silicon IGBTs and 4H-SiC IGBTs are investigated through theoretical analysis. Silicon IGBTs have potential to outperform the 4H-SiC unipolar limit beyond 3 kV under high-current density operations. However, current IGBT technologies are limited in performance due to Dynamic Avalanche (DA), which also results in reliability issues. Therefore, next generation silicon-based MOS-gated bipolar devices must be DA free and provide high current density operation capabilities with low power losses. This requirement is successfully demonstrated in the trench CIGBTs in Non-Punch-Through technology through experiments and in the 3D-scaled TCIGBTs through simulations. The measurement results show that CIGBTs remain DA free operations with low power losses even at a current density of 300 A/cm^2 at 125 °C.

Contents

Chapter 1 INTRODUCTION

1.1 Context

Nowadays human life and modern civilisation are largely dependent on energy for human mobilities, economic growths and industrial productions. According to the newly released International Energy Outlook 2019, it was projected that the world energy consumption will grow by nearly 50 % between 2018 and 2050 [1]. However, fossil fuels are the main energy source used today and will still account for 69 % of the total energy source in 2050 [1]. Replacing the fossil fuels with renewable energy source is crucial to counter the significant increase in energy demand and climate change for a future sustainable society. Among the several types of renewable source, electricity is the most widely-used renewable energy source because it is clean, safe and convenient for human life. Therefore, it is important to improve the efficiency of electrical energy to extend its applications.

More energy efficient and reliable power electronics play a critical role in energy savings because the electricity has to go through power converters from generation to the end use. It has been predicted that the widespread energy efficiency improvement by advanced power electronics technologies can save the global energy waste by 20 % [2]. In the power electronics systems, power semiconductor devices with advanced technologies are considered as the main drivers and enablers for improving converter efficiency. Even 1 % increase in converter efficiency can result in significant energy savings. For example, almost half of the worldwide electricity (~27600 TWh in 2019) is consumed by industrial motor drives in power electronics applications [3]. Assuming that the motor efficiency is 90 % and 30 % of the losses come from power switches, the total energy losses from power semiconductor devices are 414 TWh, which can fulfil the whole electricity consumption in UK (294 TWh in 2019) [4]. The ever-increasing demand for energy efficiency in power electronics necessitates reduction in the on-state and switching losses in power semiconductor devices because the increase of

power converter efficiency enabled by reduction in device losses can result in 25-40 % savings of worldwide electrical energy consumption per annum [5].

From a performance over cost as well as reliability perspective, silicon-based power devices will continue to play a crucial role in current and future power electronics systems. Wide Band-Gap (WBG) power devices such as SiC MOSFETs and GaN HEMTs have shown some superior performances in terms of low losses and high switching frequencies due to inherent advantages. However, replacing the silicon-based power devices with WBG devices requires the full systems to be redesigned, which is too expensive from the cost-effective point of view. In addition, high voltage (> 3.3 kV) WBG devices are not commercially available due to poor reliability and low yield [6]. Therefore, the silicon-based power devices will still dominate the power semiconductors market in the next few decades. Among the silicon-based power devices, Insulated Gate Bipolar Transistor (IGBT) is the main component used in medium to high power applications, such as Electric Vehicle (EV), industrial motor drives, transportations and high-power transmissions. During the past two decades, IGBT-based power electronics has saved 33.4 billion tons CO_2-emission, which is the emission amount of 390 large power plants of 1 GW in 20 years [7]. Therefore, the IGBT technology plays an important role in the worldwide energy savings.

To further improve the efficiency and compete with WBG devices, the IGBTs require continuous reduction in power losses as well as higher power density and switching frequency. This is because higher power density and switching frequency can reduce the system size, as passive components can be scaled down by increasing operating frequency. However, current IGBT technologies are limited in performance due to dynamic avalanche, which also results in reliability issues. As an innovative silicon technology to replace conventional IGBTs, Clustered IGBT (CIGBT) can provide much lower power dissipations with higher power density and reliability. Therefore, this thesis is devoted towards the development of more energy efficient and reliable MOS-gated bipolar devices to achieve energy savings in power electronics applications.

1.2 Thesis Organisation

This thesis is organised as follows:

Chapter 1 presents an overview of the importance of power semiconductor technologies in worldwide energy savings. The silicon-based power devices still play a crucial role in improving the energy efficiency of power conversions.

Chapter 2 describes the fundamentals of IGBT technologies, the state-of-the-art IGBT technologies and future perspectives. The evolution of CIGBT and its unique features are explained in detail.

In Chapter 3, 3D scaling rules for planar and trench CIGBTs are proposed and investigated through 3D numerical simulations. The scaling concept is aimed to improve on-state voltage drop versus switching losses trade-off due to enhancement of thyristor effect. Moreover, the short-circuit capability is maintained in the scaled devices due to enhanced self-clamping feature.

Chapter 4 presents the simulation results of a novel approach for suppressing the Collector Induced Barrier Lowering (CIBL) effect in the narrow mesa trench IGBTs. The novel cathode design aims to enable current saturation characteristics and short-circuit capability of the narrow mesa trench IGBTs.

In Chapter 5, a hybrid switch which combines the on-state behaviour of a MOS-gated thyristor device with the switching performance of a SiC MOSFET is demonstrated through experiments for the first time.

Chapter 6 presents the theoretical analysis of the on-state performance limits of silicon IGBTs and 4H-SiC IGBTs. The calculation results are examined with numerical simulations and also compared with the state-of-the-art power semiconductor devices.

In Chapter 7, the Dynamic Avalanche (DA), a major factor that limits the development of current IGBT technologies is analysed in detail. Moreover, a DA free solution is successfully demonstrated in the trench CIGBT with simulations and experiments. High current density operations and high supply voltage turn-off behaviour are also evaluated.

Following the DA phenomenon shown in Chapter 7, Chapter 8 analyses its influence on the dV/dt controllability of trench IGBTs. Extensive experiments are undertaken to demonstrate the high dV/dt controllability of trench CIGBT due to DA free.

Chapter 9 concludes the work in this thesis and discusses future research directions.

Chapter 2 MOS-GATED BIPOLAR POWER SEMICONDUCTOR DEVICES

2.1 Introduction of Power Semiconductor Devices

A power semiconductor device is defined as a power switch that delivers more than 1 watt of power to the load. An ideal power switch can operate between on-state and off-state with zero power losses at any frequency, as shown in Figure 2.1(a). However, the real power semiconductor devices have power losses during on-state, off-state and switching transients, which affects the energy efficiency and limits the switching frequency.

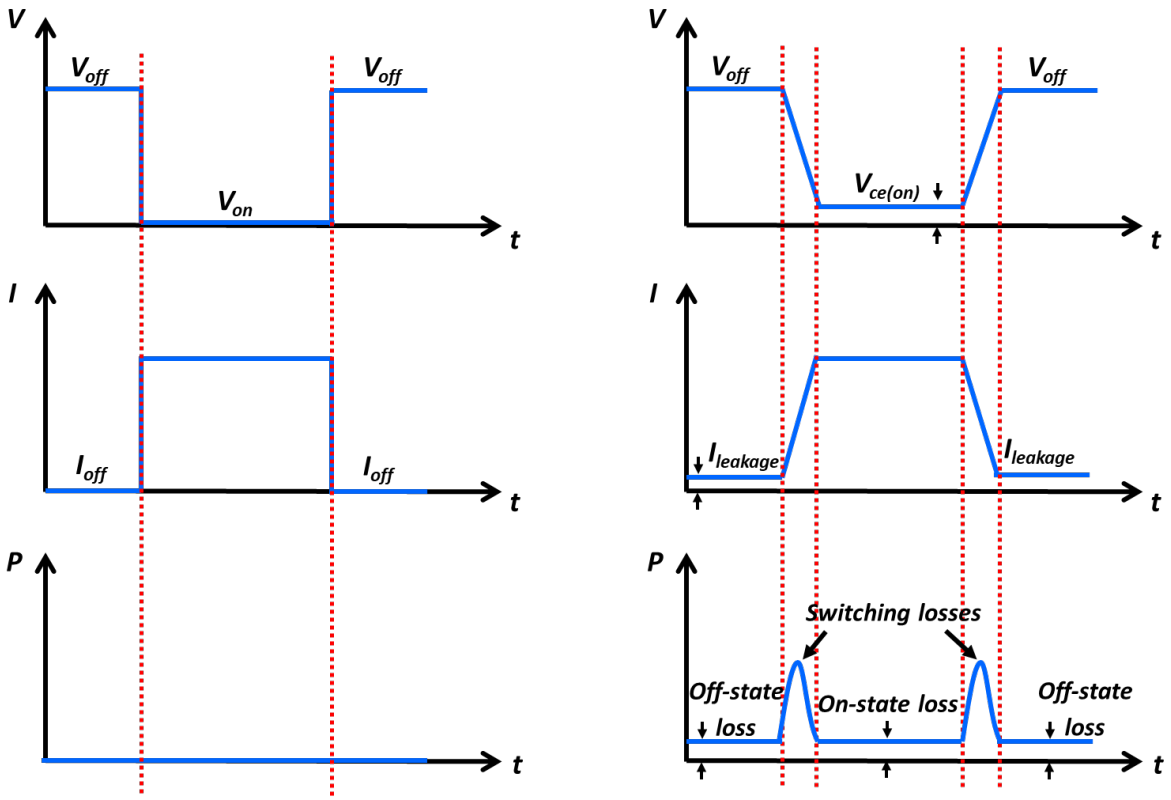


Figure 2.1 Comparison of switching waveforms of (a) ideal power switches and (b) real power switches.

To achieve controllable turn-on and turn-off transitions, three terminal power devices are preferable as the third terminal can be used as a switch to control the switching frequency. The process used for turning off a power switch is called as commutation. As per the commutation technologies, power semiconductor devices can be classified into two main groups, as specified in Figure 2.2. The natural commutated devices require a reverse-biased voltage across the devices to turn off whereas the forced commutated devices require either a current signal or a voltage signal to switch the devices between on-state and off-state. Within the forced commutated group, voltage-controlled devices such as Power MOSFET and IGBT are more favoured owing to the lower gate power requirements.

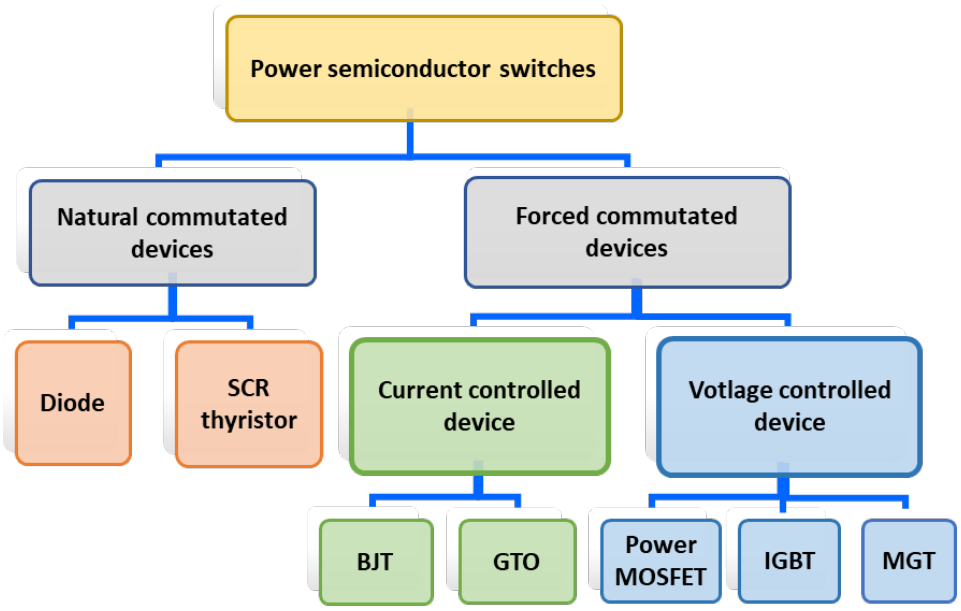


Figure 2.2 Classification of power semiconductor devices.

As per power capability and switching frequency, the applications of power semiconductor devices are shown in Figure 2.3. In the applications of low power and high frequency such as power supplies and microwave ovens, silicon-based Power MOSFETs are widely used due to low switching losses as a result of unipolar conduction. However, in the medium to high voltage (600 V – 6.5 kV) applications such as motor drives and Electric Vehicle (EV), IGBTs are dominant due to the low

conduction losses as a result of bipolar conduction. For high power and low frequency applications such as smart power grid and transportations, Gate Turn-Off thyristors (GTOs) are preferred due to high current handling capability and low on-state losses.

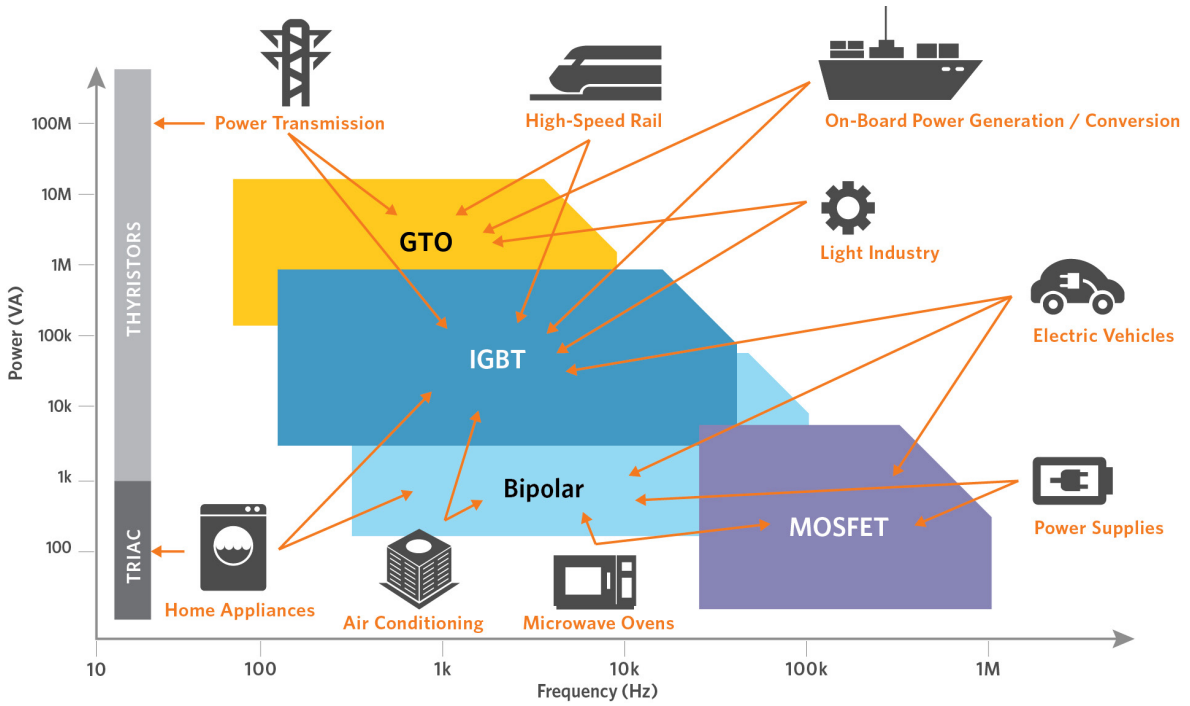


Figure 2.3 Applications of power semiconductor devices.

Since power semiconductor devices have been playing an indispensable role in power electronics field, where requires power conversion, control and conditioning, the continuous developments of power semiconductor devices are essential to counter the increasing energy demand.

2.1.1 Evolution of IGBT

The concept of the Insulated Gate Bipolar Transistor (IGBT) that uses a MOSFET to drive a BJT structure was first proposed in 1972 [8]. It combines the high input impedance of MOSFET with the high current carrying capability of BJT. The first experimental results of a lateral MOS-gated thyristor structure were published in 1978 [9], followed by the measurement results of a vertical MOS-gated thyristor structure in 1979 [10]. The first successfully fabricated MOS-gated bipolar transistor was the Insulated Gate Rectifier (IGR), which was published in 1982 [11]. However, the device

suffered from parasitic thyristor action, which had a significant impact on switching behaviour and Safe Operating Area (SOA). To suppress turn-on of the parasitic thyristor, a Non-latch-up IGBT structure that has a heavily doped p^+ region at the surface side was proposed in 1984 [12]. This type of MOS-gated bipolar device became commercialized in 1985 and it was named as IGBT [13]. Since then, the IGBTs have been widely used in many power electronics applications and play an important role in energy saving.

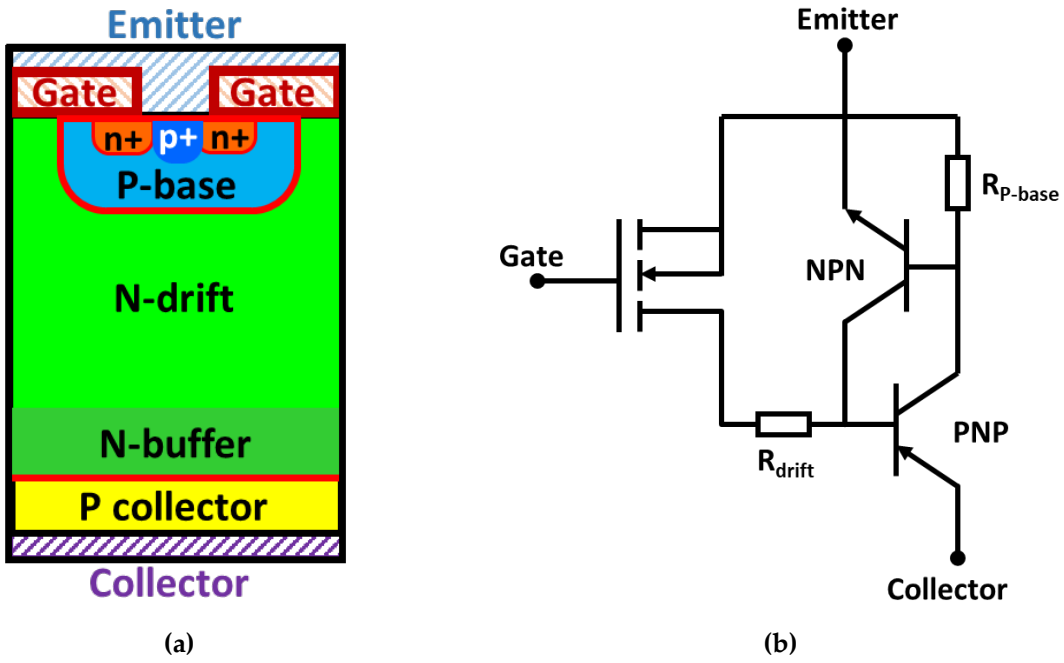


Figure 2.4 (a) Simplified cross-section of the IGBT and (b) it equivalent circuit.

2.1.2 On-state Operation

Figure 2.4 shows the unit cell structure of an IGBT device and its equivalent circuit. The IGBT is a three terminal device which consists of gate, emitter (cathode) and collector (anode). As shown in the equivalent circuit, the on-state operation can be simplified as a MOSFET providing base drive current for a BJT structure (P-base/N-drift/P-collector). To turn on the device, a positive voltage beyond the threshold voltage is applied to the gate terminal to form an inversion layer within the P-base region. The N-drift region is connected to the n^+-emitter through the channels and the potential is identical to the emitter potential, which is usually grounded in the

applications. Once the collector potential is sufficient to forward bias the P-collector/N-buffer junction, holes are injected into the drift region and electrons are injected from the n^+-emitter. Therefore, conductivity modulation occurs within the N-drift region and significantly reduces the resistance. Higher on-state carrier densities are always desirable to achieve lower on-state voltage drops ($V_{ce(sat)}$).

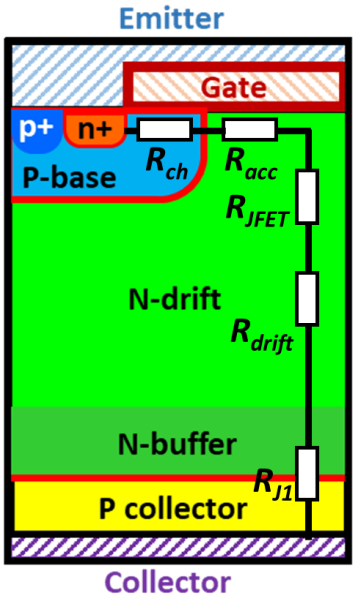


Figure 2.5 Specification of the on-state resistance of the half unit cell of an IGBT.

$$V_{ce(sat)} = V_{ch} + V_{acc} + V_{JFET} + V_{drift} + V_{J1} \qquad (2.1)$$

As shown in Figure 2.5 and equation (2.1), the $V_{ce(sat)}$ consists of the voltage drops across 1) the channel resistance (R_{ch}), 2) the accumulation layer beneath gate oxide (R_{acc}), 3) the JFET resistance (R_{JFET}) due to the depletion of P-base/N-drift junction, 4) the drift region (R_{drift}) and the 5) built-in potential of P-collector/N-buffer junction (R_{J1}). In addition to the structural parameters, another important factor to affect the on-state resistance (R_{on}) is the temperature coefficient of each component. From the application point of view, a positive temperature coefficient of the device is desired because the devices can be easily paralleled to scale up the output current. However, each resistance component features different temperature coefficient. For the channel resistance component, although more carriers are generated in the inversion layers at

high temperatures which reduces the threshold voltage, the channel resistance increases with increasing temperature due to significant decrease in channel mobility [14]. In terms of the built-in potential (knee voltage) of the P-collector/N-buffer junction, increasing temperature will reduce the potential barrier. For example, the built-in potential decreases from ~ 0.8 V at 25 °C to ~ 0.6 V at 150 °C for a silicon P-N junction [14]. The temperature coefficient of the drift region depends on the current gain of P-collector/N-drift/P-base transistor. This is because the carrier mobilities at different concentrations are dominated by different scattering mechanisms. Therefore, whether the device shows a positive or negative temperature coefficient depends on which mechanism is dominant within the structure. For example, for the structures with thick N-drift regions, such as the Non-Punch-Though (NPT) IGBT, the current gain of the internal transistor is very low compared to that of the Punch-Trough (PT) IGBT which owns a much thinner N-drift region. Therefore, the voltage drop across the R_{drift} rises up with increasing temperature and the device shows a positive temperature coefficient. However, for the PT-IGBT, the current gain is very high due to the thinner N-drift region and high P-collector injection efficiency. In addition, the carrier lifetime of PT-IGBT is dramatically reduced compared to that of NPT-IGBT. Hence, the on-state voltage drop is more sensitive to the variation in temperature. With increasing temperature, the current gain is increased due to increased carrier lifetime. The voltage drop across the R_{drift} is therefore reduced so that the device shows a negative temperature coefficient.

In addition, note that there exists a parasitic NPN transistor (n^+-emitter/P-base/N-drift) structure at the cathode side. During on-state, the injected holes are flowing into the P-base region to the emitter. If the potential in the P-base is sufficient to forward bias the n^+-emitter/P-base junction, the parasitic NPN transistor will turn on and the device will enter into thyristor conduction mode. As a result, the gate loses control and the device is latched up. One effective method to suppress the turn-on of parasitic NPN transistor is to implant a deep p^+ to lower the sheet resistance of P-base layer.

2.1.3 Dynamic Operation

a) Capacitances in the IGBT

The switching behaviour of the IGBT is largely dependent on the internal capacitances formed between three terminals, as shown in Figure 2.6. The gate-emitter capacitance (C_{ge}) is determined by the gate voltage as well as the gate oxide thickness. The gate-collector capacitance (C_{gc}) is mainly determined by the gate area and the depleted depth in the N-drift region due to collector potentials. The collector-emitter capacitance (C_{ce}) depends on the device area and the P-base/N-drift junction capacitance. In the IGBT data sheets, the capacitances are classified as:

$$\text{Input Capacitance:} \quad C_{ies} = C_{ge} + C_{gc} \tag{2.2}$$

$$\text{Output Capacitance:} \quad C_{oes} = C_{gc} + C_{ce} \tag{2.3}$$

$$\text{Reverse Transfer Capacitance:} \quad C_{res} = C_{gc} \tag{2.4}$$

During turn-on and turn-off transients, the capacitances have to be charged and discharged. Therefore, the values of these capacitances have a great impact on switching delay-time and waveforms slopes (dV/dt and dI/dt). The detailed switching performance of the IGBT is analysed using the chopper circuit shown in Figure 2.6. The DC voltage is half of the device rated voltage and the current is the device rated current. A double-pulse signal is applied to the gate input voltage to obtain the turn-on and turn-off waveforms of the IGBT.

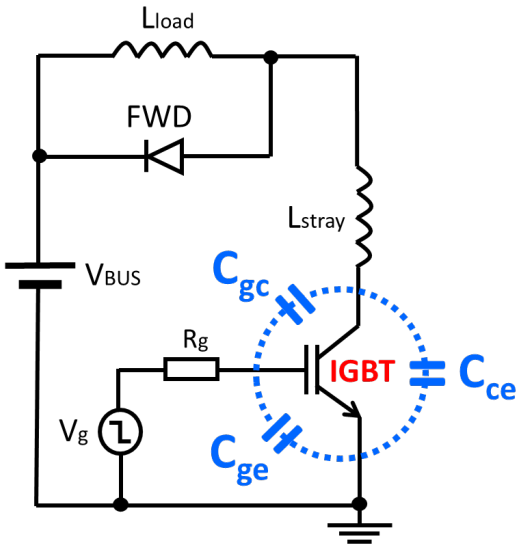


Figure 2.6 IGBT capacitance model and chopper circuit used for dynamic characterization.

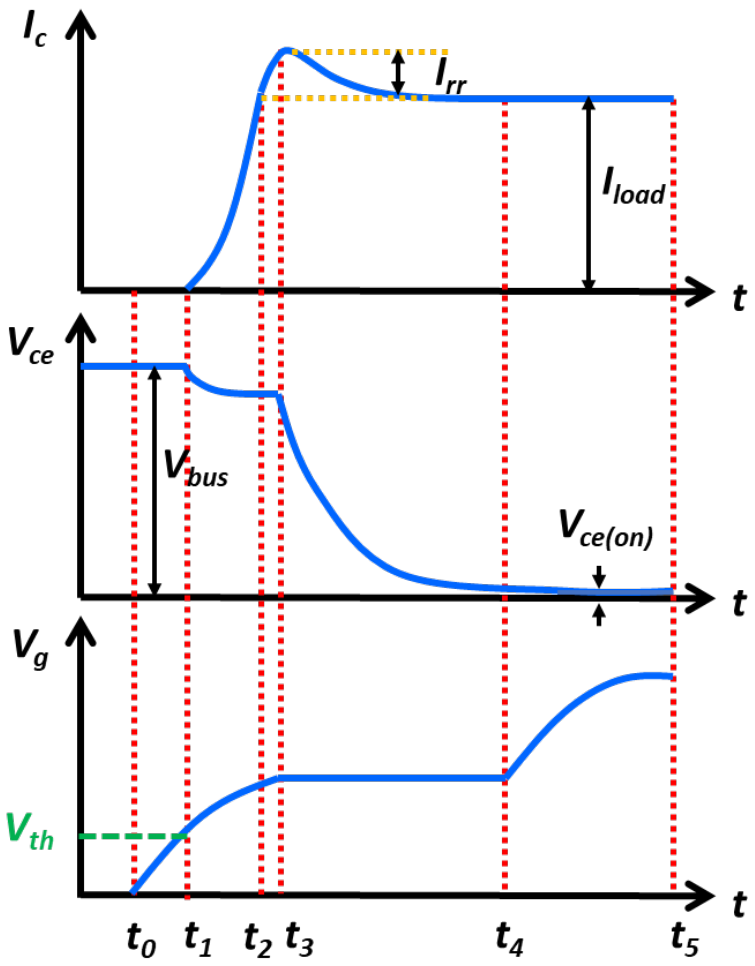


Figure 2.7 Turn-on waveforms of the IGBT.

b) Turn-on of the IGBT

Figure 2.7 shows the turn-on characteristics of the IGBT. The detailed turn-on transient can be explained as follows:

Phase I (t_0 - t_1): To turn on the IGBT, a positive bias (V_{g_in}) beyond the threshold voltage (V_{th}) is applied to the gate terminal through the gate resistance (R_g). The gate voltage (V_g) starts to rise exponentially with time and the positive gate current (I_g) starts to charge the input capacitance (C_{ies}). As the gate-collector capacitance (C_{gc}) is small at the beginning of turn-on, the C_{ies} is mainly contributed by the gate-emitter capacitance (C_{ge}). The turn-on delay time in this phase is expressed as:

$$t_{d\_on} = R_g \times C_{ies} \times \ln\left(1 - \frac{V_{th}}{V_{g\_in}}\right)^{-1} \qquad (2.5)$$

As the gate voltage (V_g) has not reached the V_{th} in this phase, the MOSFET is still off-state so that there is no current following in the IGBT.

Phase II ($t_1 - t_2$): After V_g increases to the V_{th}, the MOSFET is turned on and electron current is injected into the drift region through the inversion layers. The electron current serves as the base current of the PNP transistor and holes are injected from the P-anode. Hence, conductivity modulation occurs within the drift region and the collector current (I_c) increases at a rate of:

$$\frac{dI_c}{dt} = g_m \frac{dV_g}{dt} = \frac{g_m(V_{g\_in} - V_g)}{R_g \times C_{GC}} \tag{2.6}$$

As the collector voltage (V_{ce}) does not decrease significantly in this phase, the C_{gc} remains small so that the turn-on dI/dt is usually higher than that of turn-off.

Phase III ($t_2 - t_3$): When the I_c rises to the load current level, the current in the FWD reduces to zero. If the FWD is a PiN diode, the reverse recovery current of the FWD caused by excessive carriers within the FWD will be added to the I_c of the IGBT. Meanwhile, the IGBT has to experience high V_{ce}. Therefore, high losses are generated in this phase. Improving the reverse recovery performance or using unipolar diodes such as Schottky Barrier Diode (SBD) can effectively reduce the turn-on losses of the IGBT.

Phase IV ($t_3 - t_4$): After the reverse recovery current is transferred to the IGBT, the V_{ce} decreases dramatically and the output capacitance (C_{oes}) increases due to the reduction of depletion region. The collector-emitter capacitance (C_{ce}) is charged by the internal current (I_c) while the C_{gc} is charged by the external current (I_g), which is referred as miller effect [14]. The V_g and the I_g remain constant in this phase and this phase is also called as miller plateau. The fall rate of the V_{ce} in this phase is expressed as:

$$\frac{dV_{CE}}{dt} = \frac{I_g}{C_{GC}} = \frac{V_{g\_in} - V_{th} - I_c/g_m}{R_g \times C_{GC}} \tag{2.7}$$

Phase V ($t_4 - t_5$): After the miller plateau, the V_g further rises to the V_{g_in} and the I_g charges the C_{ge}. The V_{ce} falls slowly in this phase and reduces to the on-state voltage drop ($V_{ce(sat)}$).

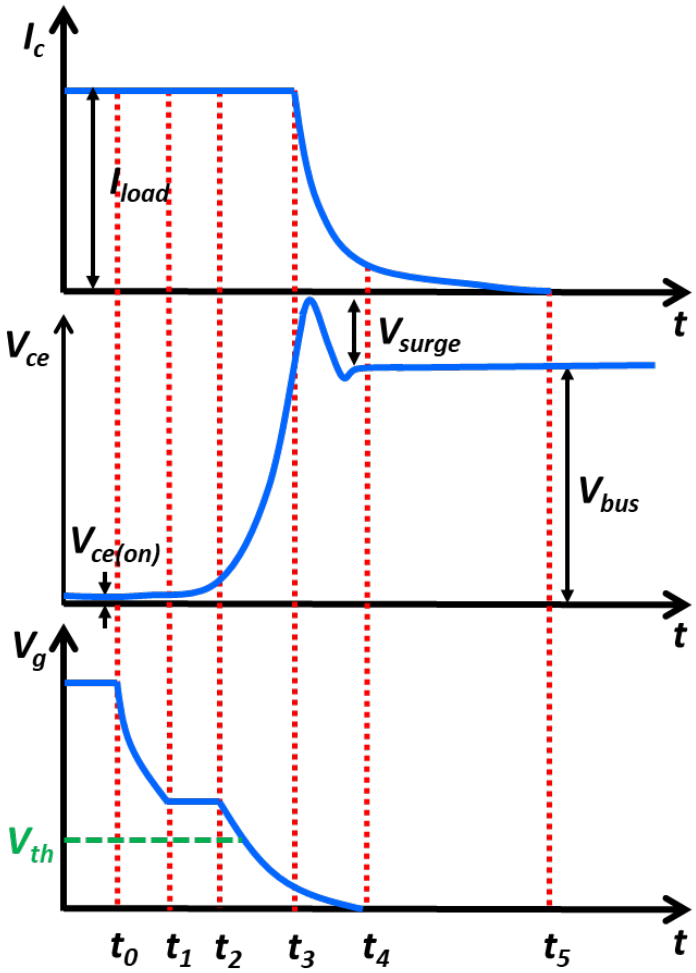


Figure 2.8 Turn-off waveforms of the IGBT.

c) Turn-off of the IGBT

Figure 2.8 shows the turn-off characteristics of the IGBT. The detailed turn-off transient can be explained as follows:

Phase I (t_0 - t_1): To turn off the IGBT, a zero bias or a negative bias is applied to the gate terminal through the gate resistance (R_g). The gate voltage (V_g) starts to decrease exponentially with time. The input capacitance (C_{ies}) is discharged by the negative gate current (I_g) and the turn-off delay time in this phase is expressed as:

$$t_{d\_off} = R_g \times C_{ies} \times \ln\left(\frac{V_g}{V_{th} + I_c/g_m}\right) \quad (2.8)$$

where V_{th} is the threshold voltage, and g_m is the transconductance of the IGBT. Compared to the turn-on transient, the delay time of turn-off is longer due to larger gate-collector capacitance (C_{gc}) at the beginning of turn-off.

Phase II ($t_2 - t_3$): After V_g falls to the level required to maintain the collector current (I_c) at the load current level, the V_g remains constant and the I_g discharges the C_{gc}.

$$I_g = \frac{V_{th} + I_c/g_m}{R_g} \quad (2.9)$$

Phase III ($t_2 - t_3$): The collector-emitter voltage (V_{ce}) start to rise up at a rate of

$$\frac{dV_{ce}}{dt} = \frac{I_g}{C_{GC}} = \frac{V_{th} + I_c/g_m}{R_g \times C_{GC}} \quad (2.10)$$

As expressed, the C_{gc} and the R_g have significant impact on the collector voltage slope (dV/dt). In terms of the design of an IGBT structure, low C_{gc} is expected to achieve low switching losses. Since the depletion region within the TIGBT expands as V_{ce} increases, the dV/dt increases with time due to the decrease in C_{gc}.

Phase IV ($t_3 - t_4$): After V_{ce} increases to the supply voltage (V_{bus}), the Free-Wheeling Diode (FWD) turns on and the load current starts to divert from TIGBT to FWD. Therefore, the I_c decreases immediately and induces a surge voltage (V_{surge}) due to stray inductance (L_{stray}) in the circuit.

$$V_{surge} = L_{stray} \times \frac{dI_c}{dt} \quad (2.11)$$

Phase V (t_4 - t_5): As the IGBT employs bipolar on-state conduction, the stored minority carriers have to evacuate or recombine within the drift region during turn-off. Therefore, a current tail appears in the collector current waveform, which results in higher losses compared to a unipolar device such as Power MOSFET.

2.1.4 Cathode Engineering

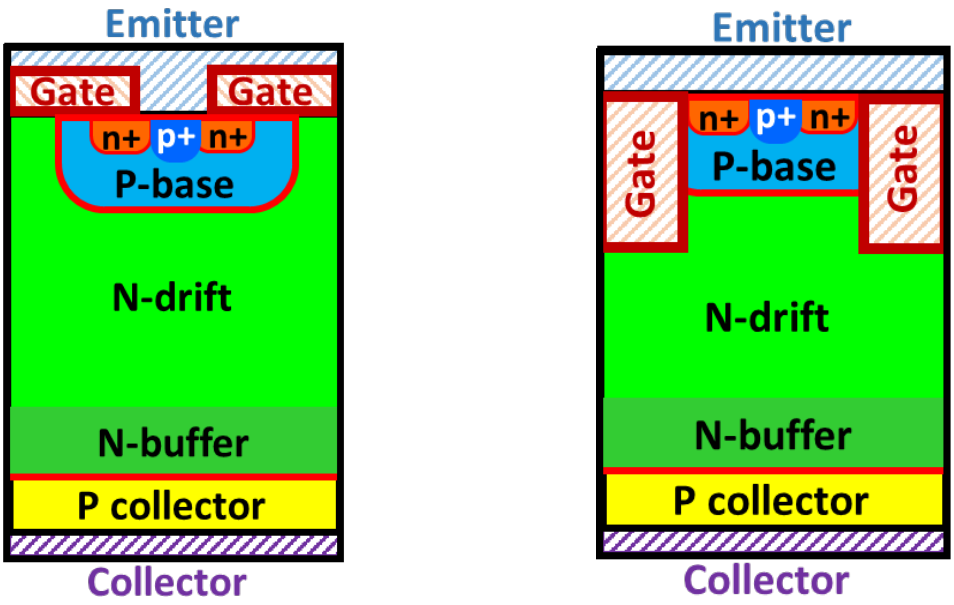


Figure 2.9 Simplified cross-sections of (a) planar IGBT and (b) trench IGBT.

a) Planar Gate IGBT

Figure 2.9(a) shows the unit cell of an IGBT with a planar gate. The gate oxide layer is sandwiched between poly gate and silicon. During on-state, electrons are injected from the n^+-emitter and flow laterally through the channel inversion layer and then vertically towards the collector. When the collector voltage exceeds the built-in potential of the P-anode/N-drift junction, holes are injected from the P-anode and move up to the emitter side. Due to charge neutrality, hole current flows beneath the n^+-emitter and then evacuates through the p^+ region. As the collector voltage is supported by the P-base/N-drift junction, the depletion boundary within N-drift expands with increasing collector voltage, which leads to JFET effect between P-base regions and restricts the flow of current. Increasing the distance between P-base to P-base can effectively suppress the JFET effect and lower the R_{JFET}, whereas this will reduce channel density within the active area of the IGBT device. Another method to minimise the JFET effect is the JFET implant [15], which increases the concentration of the drift region beneath the planar gate to lower the surface resistance.

b) Trench Gate IGBT

To eliminate the JFET effect, trench gated IGBT shown in Figure 2.9(b) was proposed in 1987 [16]. As the P-base regions are isolated by the deep trenches, both electron and hole current flow vertically within the device, which eliminate the R_{JFET} in the R_{on}. Moreover, compared to the planar IGBT, the trench IGBT provides higher channel density due to closely packed cells. Therefore, the on-state behaviour of trench IGBT is superior to that of planar IGBT. However, the trench IGBT also displays a higher saturation current density due to higher transconductance as a result of shorter channel length. Therefore, the short-circuit withstand capability of trench IGBT is worse than that of planar IGBT. Many efforts have been devoted to lowering the saturation current density without affecting the on-state performance. One common way to reduce saturation current density is to employ dummy cells within the active area. However, this method may enhance the negative gate capacitance effect during device turn-on. This is because the current density beneath trench gate is enhanced, which induces more negative charge in the gate oxide during turn-on. Therefore, the dummy cell design has to compromise both saturation current levels and switching behaviour.

Another important concept in trench IGBT design is the Injection Enhancement (IE) effect, which was introduced in 1993 and named as Injection Enhancement Gate Transistor (IEGT) [17]. Deep and wide trenches are employed to constrict the flow of holes into mesa region. Hence, holes concentrate at trench corners, which increases the potential in the N-drift and attracts more electrons to be injected from the cathode cell. As a result, the on-state carrier density at the emitter side is enhanced compared to the conventional trench IGBT, as shown in Figure 2.10. A lower $Vce_{(sat)}$ is therefore achieved by the IE effect. However, it should be noted that wide and deep trenches will increase the C_{gc} and switching losses. In addition, it was found that the large negative gate capacitance effect of IEGT can induce an gate overshoot voltage during turn-on [18], which enhances the EMI noise and affects the dV/dt controllability.

Therefore, the employment of IE effect has to compromise both on-state performance and switching behaviour.

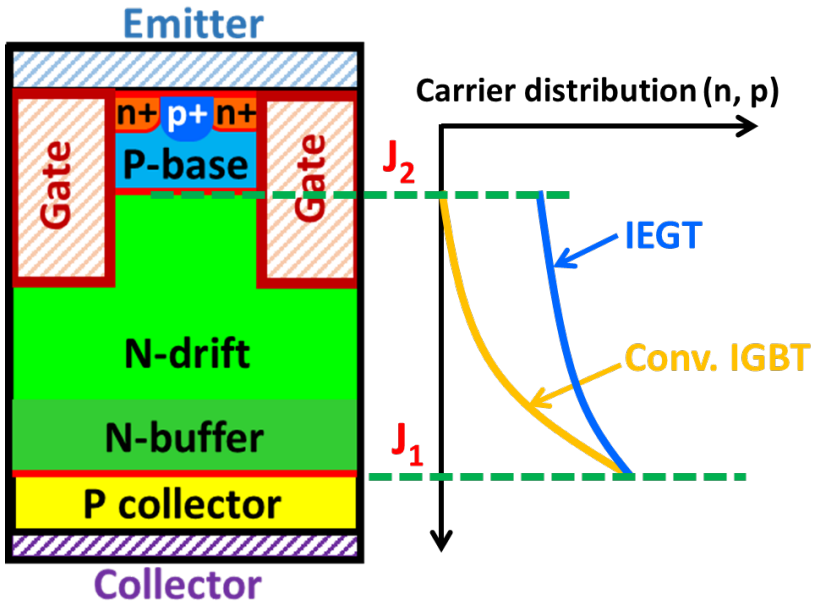


Figure 2.10 Cross-section view and carrier distribution of IEGT.

2.1.5 Drift Region Engineering

As the forward blocking voltage is supported by the P-base/N-drift junction, the thickness and doping concentration of N-drift region are designed to support the target blocking voltage. There are three main technologies for N-drift region designs, as summarized in Figure 2.11.

a) Punch Through (PT) Technology

The PT technology is mainly used in the early fabricated IGBTs. Two n-type epitaxial layers are grown on a thick p^+ substrate. The first layer is a heavily doped N-buffer layer, which acts as the electric field stopper during blocking state and reduces the anode injection efficiency during on-state. The second layer is a thick lightly doped N-drift layer, which is completely depleted to support the blocking voltage during off-state. The electric field features a trapezoidal shape in the PT-IGBTs. As the current gain of the PNP transistor is very high due to thick P^+-anode, the device exhibits a low switching speed and high switching losses. To suppress this issue, lifetime killing

process is employed to reduce the on-sate carrier density. In addition, the high on-state carrier density results in a negative temperature coefficient of the device, which makes the devices difficult to paralleled operation.

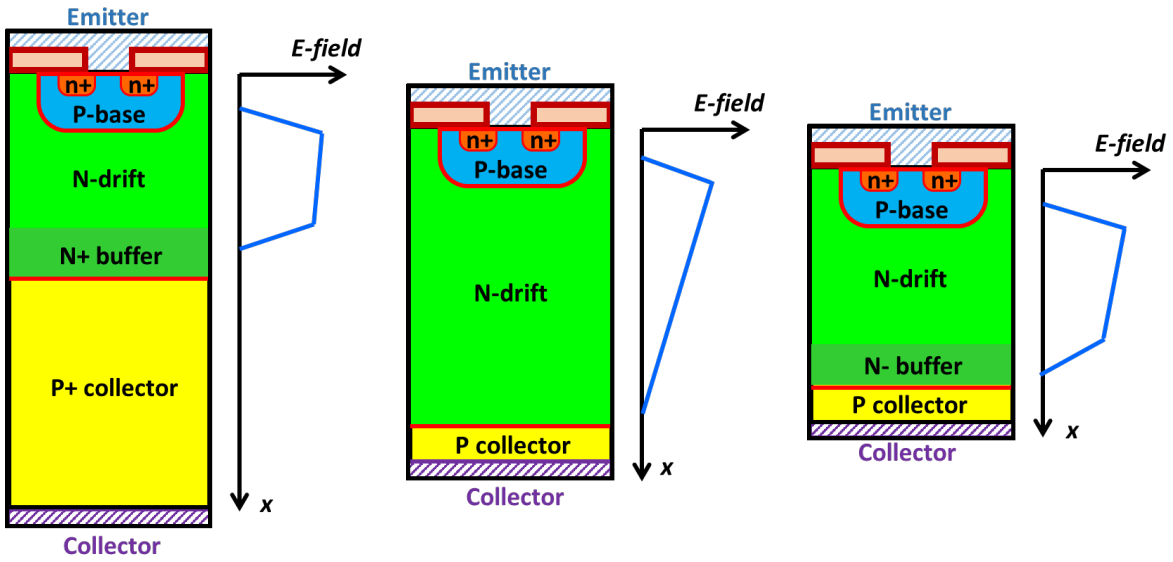


Figure 2.11 Simplified cross-sections and electric field distributions of (a) PT IGBT, (b) NPT IGBT and (c) FS IGBT.

b) Non-Punch Through (NPT) Technology

To improve the switching behaviour and overcome the negative temperature coefficient, the NPT concept was introduced to IGBTs in 1989 [19]. The NPT IGBT is fabricated on a n-type starting wafer with a thin lightly doped P-anode. The electric field features a triangular distribution and the N-drift thickness must be sufficient to prevent punch-through of the PNP transistor. Since the current gain of the NPT-IGBT is reduced compared to that of the PT-IGBT, the NPT-IGBT exhibits a positive temperature coefficient and faster switching speed.

c) Field-Stop (FS) Technology

The FS concept was first proposed in 1995 and called as homogeneous base [20]. It combines the advantages of both PT and NPT advantages. The N-buffer layer doping

concentration is usually in the range of 10^{15} to 10^{16} cm^{-3}, which is lower than that in the PT structure. Compared to the NPT structure, a similar transparent P-anode is employed to lower the anode injection efficiency so that lifetime control is not needed for FS technology. As the electric field features a trapezoidal distribution, the device thickness can be significantly reduced through wafer thinning technologies. As a result, both on-state losses and switching losses are reduced compared to PT-IGBT. However, the high switching slopes (dI/dt) enhance the oscillations in the switching curves.

The comparison of the three types of drift region structures are summarized in the Table 2.1 below.

Structure	***PT-IGBT***	***NPT-IGBT***	***FS-IGBT***
Drift layer thickness	Thin	Thick	Thin
Buffer layer	Thick and highly doped	N/A	Thin and lowly doped
P-collector	Thick and highly doped	Transparent	Transparent
Bipolar gain control	Lifetime killing	Injection efficiency	Injection efficiency
On-state losses	Low	Medium	Low
Switching losses	High	Medium	Low
Turn-off tail	Short	Long	Short
Temperature coefficient	Negative	Positive	Positive
SCSOA	Medium	Large	Large
RBSOA	Narrow	Large	Large
Device in parallel	Hard	Easy	easy

Table 2.1 Comparison of three types of drift region structures.

2.1.6 Anode Engineering

In the IGBT, the anode injection efficiency has a significant influence on the off-state leakage levels, which affects the maximum operating temperature. In addition to the conventional P-anode design, there are two novel anode designs to control the anode injection efficiency.

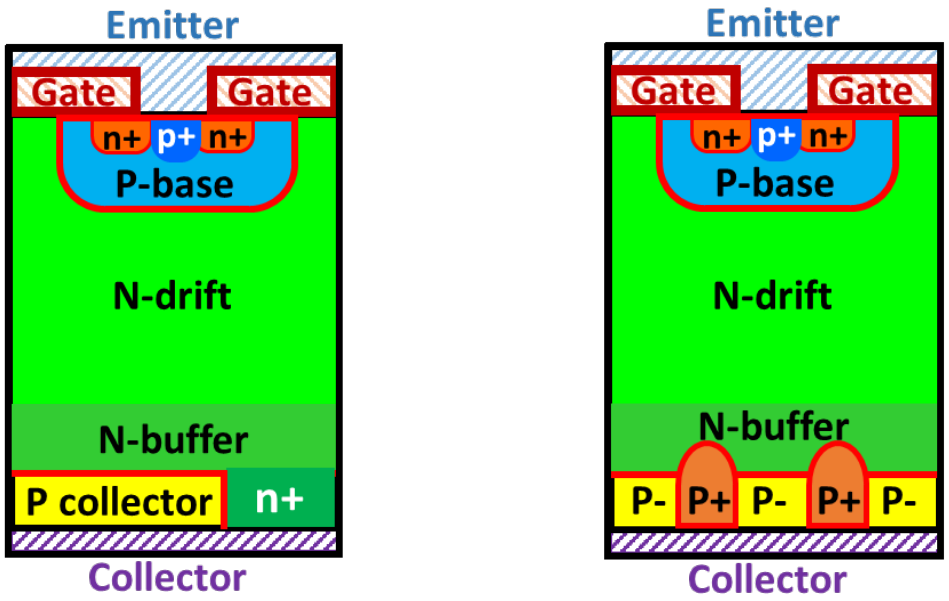


Figure 2.12 IGBT structures with (a) shorted-anode and (b) stripped anode.

a) Shorted-anode Design

One method is to replace part of P-anode with N-anode, as shown in Figure 2.12(a). It was proposed in 1995 and called as N-anode short [20]. The anode injection efficiency can be controlled by adjusting the width ratio between P-anode and N-anode. However, this design suffers from snap-back I -V performance during turn-on. This is because the P-anode/N-drift junction is "shorted" by the N-anode. Therefore, the IGBT behaves like a MOSFET at the beginning of turn-on. Once the potential drop across the P-anode/N-drift junction due to lateral flow of electron current is sufficient to forward bias the PN junction, holes are injected from the P-anode and the device operates as a conventional IGBT. The snap-back phenomenon can be effectively

suppressed by increasing P-anode width. Moreover, the N-anode provides a direct path for the excessive electrons during device turn-off. Therefore, the switching losses are reduced compared to a conventional IGBT.

b) Stripped-anode Design

To eliminate the snap-back I-V performance, the stripped-anode concept was proposed in 2002 [21]. A number of P^+ anode pillars are implanted into a thin lightly doped P^- anode layer, as shown in Figure 2.12(b). The anode injection efficiency can be controlled by the number of anode pillars within the active area. A significantly improved trade-off between turn-off energy losses and on-state voltage drop can be achieved by this design in a 6.5 kV IGBT [21].

2.1.7 State-of-the-art IGBT Technologies

Over the past three decades, several generations of IGBT technology have been developed through innovation and industrialization. One major factor to evaluate the improvement of IGBT technology is the turn-off energy loss (E_{off}) versus forward voltage drop ($V_{ce(sat)}$) trade-off. The continuous improvements of the E_{off}-$V_{ce(sat)}$ trade-off have resulted in not only low loss operations but also increases in current densities and improved cost performance of IGBT modules. Some other factors such as Safe Operating Area (SOA) and long-term reliability are also needed to be considered.

a) IGBT with narrow mesa width

As trench gate IGBTs have shown superior performances in terms of higher current density and lower losses compared to planar IGBTs, the trench gate geometry is widely used in current IGBT technologies with rated voltages from 650 V to 6.5 kV [13, 22]. The on-state performances of trench IGBTs can be significantly improved by enhancing IE effect. From the device design point of view, one direct solution to enhance the IE effect is to scale down the mesa width. Figure 2.13 shows an example of a narrow mesa trench IGBT [23]. Several IGBT structures with respect to the narrow mesa design have been reported, including Micro-Pattern Trench IGBT (MPT-IGBT)

[24], Ultra-narrow-mesa Fin P-body IGBT (U-Fin-P IGBT) [25], Partially Narrow Mesa IGBT (PNM-IGBT) [26], Recessed Emitter Trench IGBT (RET-IGBT) [27] and 3-D scaled trench IGBTs [28-30]. A $V_{ce(sat)}$ of 1.65 V can be achieved at a current density of 500 A/cm^2 with a mesa width of 30 nm [26]. However, the narrow mesa trench IGBTs suffer from poor short-circuit performance due to non-saturated I-V characteristics [31]. This is because, during on-state, conductivity modulation occurs in the channel inversion layers when the mesa is too narrow, resulting in Collector Induced Barrier Lowering (CIBL) effect [32]. The detailed physics and an effective solution to suppress CIBL effect will be explained in Chapter 4. Therefore, the scaling work on mesa region must take the SCSOA into account.

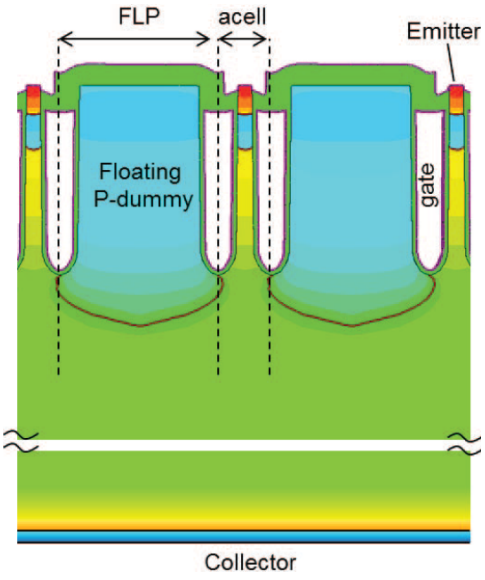


Figure 2.13 Narrow mesa trench IGBT [31].

b) IGBT with hole barrier layer

In addition to the IE effect in trench IGBTs, another approach to increase the emitter side carrier density is the employment of a N-type barrier layer beneath P-base layer to prevent holes from entering into P-base region during on-state, as shown in Figure 2.14(a). Hence, the conductivity modulation at the emitter side is enhanced, resulting in a lower forward voltage drop. This concept was first reported in a trench IGBT structure in 1996, called as Carrier Store Trench-Gate Bipolar Transistor (CSTBT) [33],

as shown in Figure 2.14(b). Following that, this concept was applied to the planar IGBT structure in 1998, named as High-Conductivity IGBT (HiGT) [34] and the trench HiGT was reported in 2007 [35]. The experimental results showed that the HiGT can achieve much lower $V_{ce(sat)}$ without any increase in saturation current and E_{off}. Therefore, this concept is widely used in current IGBT technologies to achieve lower losses and larger SOA, such as the Soft Punch Through Enhanced-Planar IGBT (SPT$^+$ IGBT) with breakdown voltage up to 6.5kV [36]. Increasing hole barrier layer concentration can lower the $V_{ce(sat)}$ due to enhanced on-state carrier density. However, this may cause premature breakdown due to higher peak electric field at the P-base/hole barrier layer junction. Therefore, the concentration and depth of the hole barrier layer must compromise both on-state performance and breakdown characteristics.

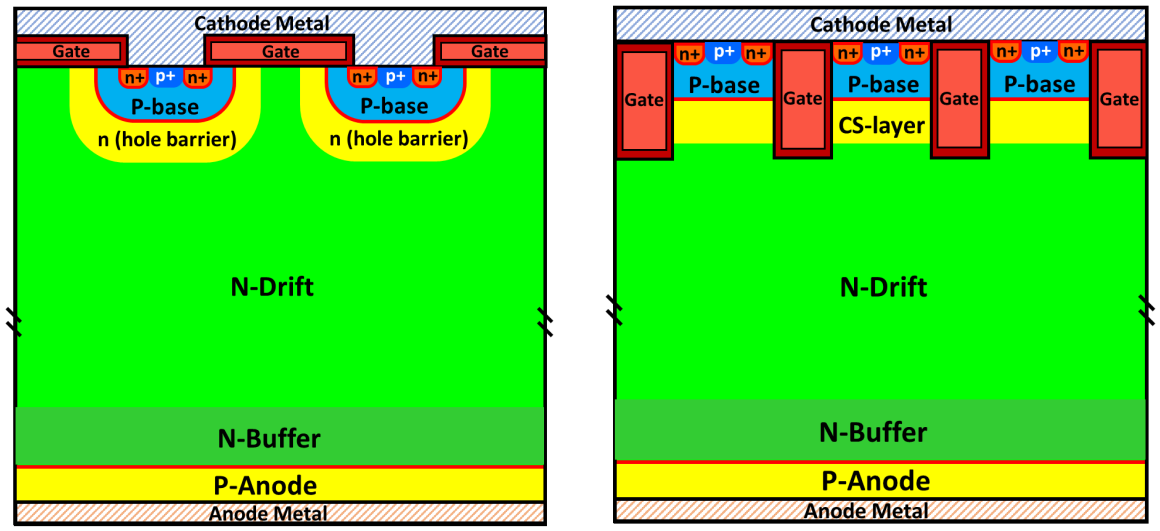


Figure 2.14 Simplified cross-section views of (a) Planar HiGT and (b) CSTBT.

c) IGBT with reverse conducting capability

As IGBTs are used in medium to high voltage power converters, unlike the vertical Power MOSFET which has an intrinsic diode structure, the IGBT requires an external anti-parallel Freewheeling Diode (FWD) to protect against reverse conducting currents in various power circuit configurations, as shown in Figure 2.15(a). Recently,

several Reverse Conducting IGBT (RC-IGBT) devices which integrate both IGBT and FWD functionalities have been reported [37-39]. Figure 2.15(b) shows a simplified cross-section of a RC-IGBT structure. As the IGBT and diode are conducting on a single chip, the thermal resistance is significantly reduced due to larger chip area. Therefore, the operating current density and maximum junction temperature can be increased. In addition, the footprint of the IGBT modules can be significantly reduced by the RC-IGBT chips for the same output current, resulting in a higher power density and cost reduction. The challenges of RC-IGBTs are to eliminate the snap-back phenomenon in the I-V characteristics and to improve the reverse recovery performance of the integrated diode. One approach to improve the diode reverse recovery performance is the employment of MOS channels [40], which has been used in the MOS controlled diode [41].

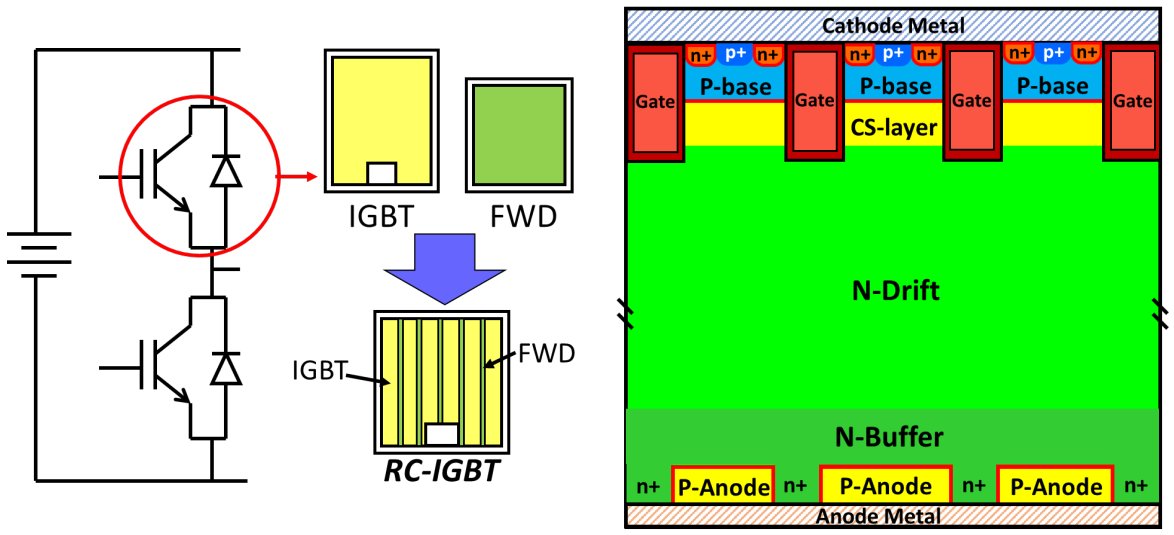


Figure 2.15 (a) RC-IGBT concept and (b) simplified cross-section of the RC-IGBT.

d) IGBT with dual gate control

Intelligent gate driving is always a promising perspective for the development of IGBT technologies. One excellent implementation of advanced gate control is the HiGT structure with dual-side gate control [42], as shown in Figure 2.16 . The device

operation is divided into three modes, conductive mode, switching mode and blocking (off-state) mode. As one side-gate has turned off prior to the turn-off of the device, the on-state carrier density and feedback capacitance (C_{res}) are significantly reduced. Therefore, the device exhibits much lower switching losses compared to the conventional IGBTs.

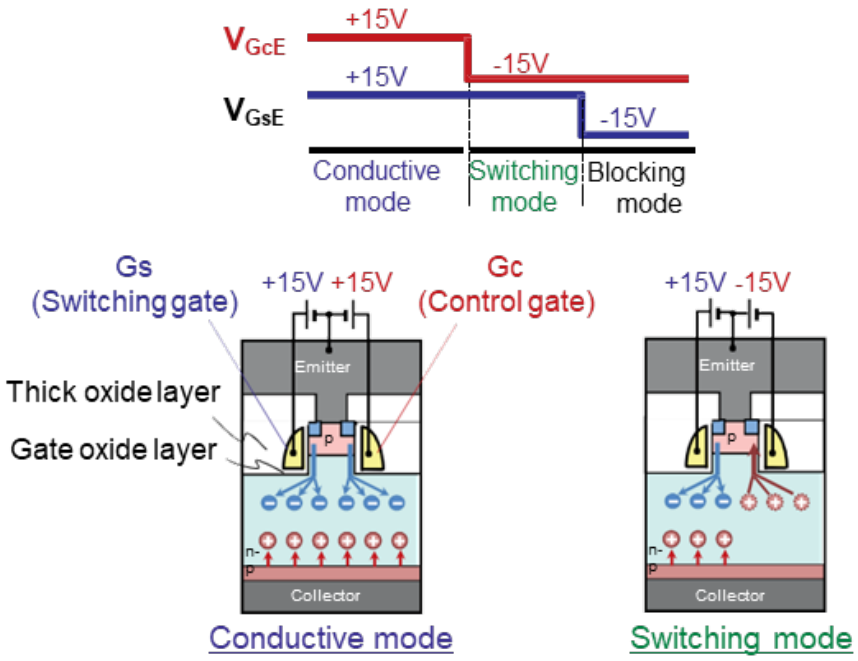


Figure 2.16 Concept and structure of dual side gate HiGT [42].

2.1.8 Future Perspectives

a) Higher power density

The motivation of increasing current density per chip area is to either improve the output power for a given module footprint or reduce the package size for a given power. Therefore, the development of IGBT is always targeting higher power density for design optimization and cost reduction. To improve the operating current densities, it is crucial to further improve the E_{off}-$V_{ce(sat)}$ trade-off of IGBTs and to implement novel IGBT technologies in a given module footprint to upgrade the power efficiency of converter systems. However, current IGBT technologies are limited in terms of on-state performances and further increase in power density. This can be

attributed to the Dynamic Avalanche (DA) phenomenon during turn-off, which poses a fundamental limit upon the power density capability. Therefore, the future development of IGBT must be DA free to further improve the power density.

b) Higher switching frequency

High switching frequency is also an important factor for modern power converters. This is because high switching frequencies (high dV/dt) can improve the dynamic response capability and reduce the passive components by smaller system size. The maximum switching frequency is mainly determined by the switching losses during turn-on and turn-off. For bipolar power devices, the switching losses are related to the build-up and removal of excessive carriers within drift layers. One common way to reduce the switching losses is to use small gate resistances to speed up the charging and discharging of the input and out capacitances. As a result, the devices exhibit a higher dV/dt as well as lower switching losses. However, in the turn-off of trench IGBTs, the DA can be triggered at small gate resistances [43, 44], which results in additional switching losses and affects the gate stability [45]. Therefore, DA free solutions are crucial to meet the requirement of high frequency operations. In addition, inherent innovations on device design are also needed to minimise the feedback capacitance (C_{res}) and speed up the removal of stored excess carriers.

c) Higher controllability

For IGBT modules, variable speed drives with Pulsed Width Modulated (PWM) control is one of the most important applications. One major requirement in the driving systems is the limitation of switching speed due to the inherent limitation of the motor insulation system [46, 47]. Therefore, switching slopes (dV/dt) are usually restricted to the range of 2 to 10 kV/μs [47]. As the switching slopes (dV/dt) have a direct impact on switching losses, high controllability of gate resistances on the maximum dV/dt is important to meet the requirement of driving systems and achieve high switching frequency.

d) Advanced Thermal Management

To increase the power density, the maximum operating temperature must be increased as well to meet the requirement of higher current density operations. With the optimized buffer design, the 1.2 kV planar IGBTs can operate at 200 °C with low leakage currents, rugged Reverse-Bias Safe Operating Area (RBSOA) and 10 μs short-circuit withstand capability [48]. Therefore, advanced packaging technologies and cooling systems are needed to meet the high temperature operations of IGBT devices.

2.2 MOS-gated Thyristor – Clustered IGBT

2.2.1 Evolution of MOS-gated Thyristor

During the development of medium to high voltage power semiconductor technologies, the thyristor operation is always desirable due to low conduction losses as a result of highly conductivity modulated drift regions. Several devices have been developed using this concept such as Integrated Gate Commutated Thyristor (IGCT) and Gate Turn-Off thyristor (GTO). However, these devices require current control so that the control circuit needs to be complex and consumes additional power. Compared to the current-controlled thyristor devices, voltage controlled IGBTs can provide much higher switching frequency with smaller converter footprint and higher reliability [49]. Consequently, the voltage controlled converter technologies that use high voltage IGBTs are gradually replacing the line commutated converter options which are based on thyristor technologies in the HVDC transmissions [49]. However, the high voltage IGBTs exhibit higher on-state losses than thyristor devices due to lower on-state carrier densities as a result of lower current gains. Therefore, they have to be operated under lower current densities which results in higher cost per ampere. Under this context, the MOS-Controlled Thyristor (MCT) devices are highly desirable to combine the simple gate control of IGBTs and low on-state losses of thyristors.

The first MCT structure was reported in 1984 [50]and then a Base Controlled Thyristor (BRT) was developed in 1991 [51]. Owing to thyristor operation, low forward voltage

drops can be achieved. However, these devices show very poor short circuit performance because they do not have current saturation feature. Therefore, they were not commercialized and IGBTs are still dominant in the market. Another MCT device is the Emitter Switch Thyristor (EST) proposed in 1991 [52]. It exhibits gate controlled current saturation behaviour, but the forward voltage drop is higher than other thyristors because the thyristor current is controlled by a dual channel MOSFET in series. In addition, the breakdown of the series MOSFET at high gate voltages cannot be avoided when the control MOSFET has reached saturation.

2.2.2 Evolution of Clustered IGBT

As an alternative technology, the Clustered IGBT (CIGBT) belongs to a new family of MOS-controlled power devices with thyristor operations and excellent current saturation characteristics. The unique self-clamping feature enables not only low current saturation levels but also low switching losses. After two decades of continuous development, the CIGBTs have been experimentally demonstrated from 1.2 kV to 3.3 kV [53-56] and they have shown superior performances in terms of low forward voltage drops, low switching losses and larger safe operating areas compared to state-of-the-art IGBTs. The comparison between the IGBT, CIGBT and EST has been numerically studied in [57]. Figure 2.17 summarises the technology roadmap of the CIGBT family. The first planar CIGBT structure was proposed in 1999 [58] and the Trench CIGBT (TCIGBT) was reported in 2000 [59]. The PMOS CIGBT [60] employs a PMOS trench gate in a conventional planar CIGBT structure. The PMOS gate is only active during turn-off to provide a direct path for excessive holes to evacuate. Moreover, the PMOS gate can lower the current saturation levels by reducing the self-clamping voltage [61]. Hence, the PMOS exhibits a significant improvement of short-circuit performance without degrading the on-state behaviour. To further improve the dynamic characteristics, Super-Junction (SJ) concept is incorporated into the PMOS TCIGBT [62]. Different from the SJ-IGBTs which suffer from poor short-circuit performance and turn-off failures, the SJ-TCIGBT can eliminate these drawbacks and

show significant improvement of turn-off speeds. The detailed principles will be explained in the later section. Recently, the PMOS structure was fully integrated into the conventional 1.2 kV TCIGBT in Non-Punch Through (NPT) technology [56], as shown in Figure 2.17(d). This device employs high density of MOS cells in a ladder design with fine pattern process. A low forward voltage of 1.8 V can be achieved at a current density of 140 A/cm^2 at 25 °C. Due to the self-clamping feature, the device also shows 10 μs short-circuit capability at a bus voltage of 800 V at 125 °C. Furthermore, even in the NPT technology, the on-state voltage drop versus switching losses trade-off relationship of the TCIGBT is superior to the state-of-the-art trench IGBT in Field Stop (FS) technology [56]. With the employment of FS technology and SJ structure, the electrical characteristics of the TCIGBTs can be further improved. Therefore, the TCIGBT technology is a more efficient and reliable replacement of the trench IGBT technologies for energy savings in medium-high power applications.

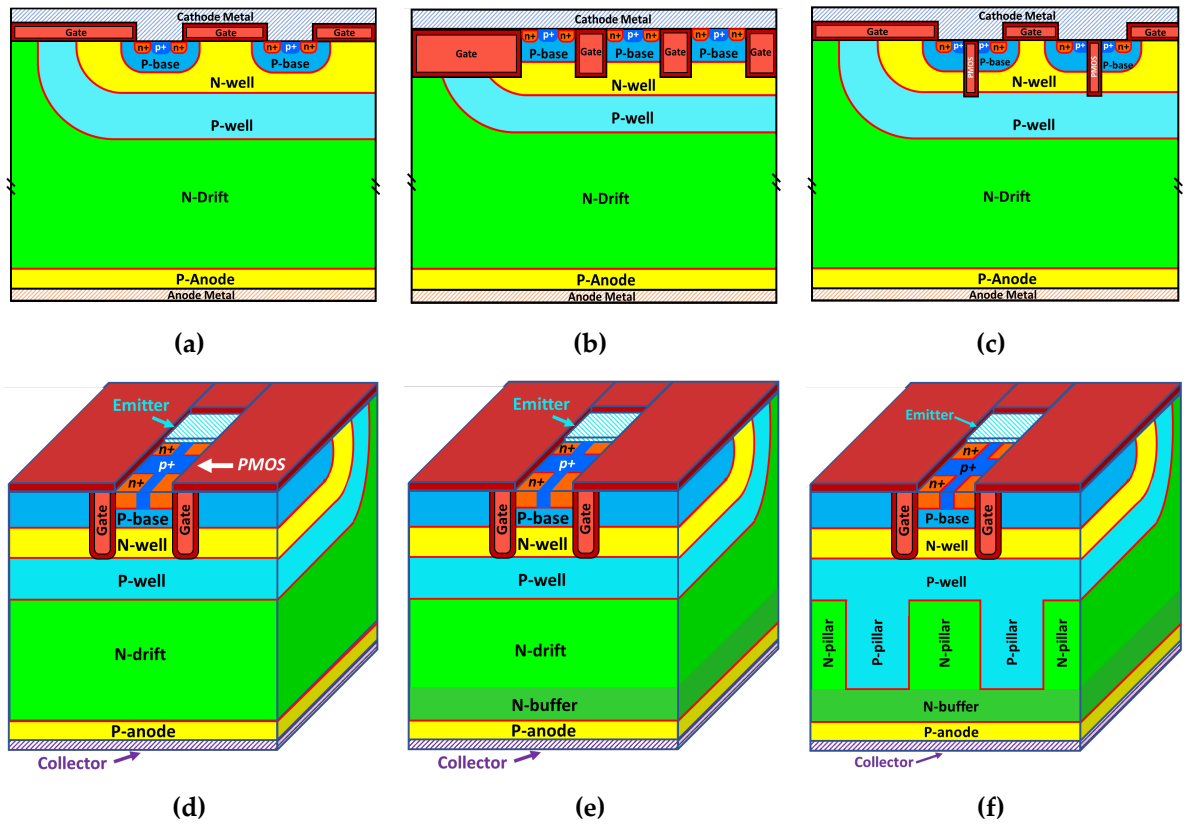
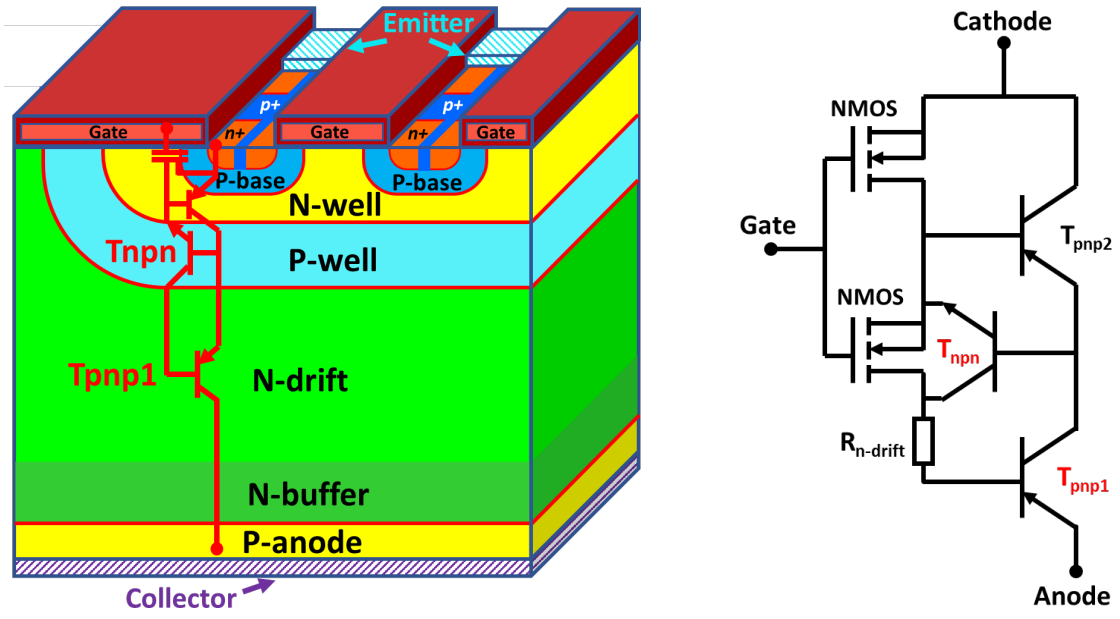


Figure 2.17 CIGBT family: (a) NPT planar CIGBT, (b) NPT TCIGBT, (c) NPT planar CIGBT with PMOS, (d) NPT TCIGBT with PMOS, (e) FS TCIGBT, and (f) SJ-TCIGBT.

2.2.3 On-state Operation of CIGBT

Figure 2.18 shows the 3-D cross-section view of a planar CIGBT structure and its equivalent circuit. The CIGBT is a three terminals device which employs a MOSFET to control a thyristor structure. The thyristor structure consists of N-well, P-well, N-drift and P-anode. To turn the device ON, a positive gate voltage above the threshold voltage is applied to form inversion layers in both P-well and P-base regions. The inversion layers formed in the P-base connect the N-well to the ground potential. In addition, the inversion layer formed in the P-well connects the N-well with the N-drift and lead to the floating of the P-well region. Therefore, during conduction, the potential in the P-well increases with anode voltage. Once the potential drop across the P-well/N-well junction is sufficient to forward bias the junction barrier, the main thyristor turns on without snap-back in the I-V characteristics. High-level injection of minority carriers results in removal of the potential barrier across the P-well junction. The conductivity modulation is significantly enhanced because of thyristor action. Hence, the on-state loss can be reduced in comparison to an equivalent IGBT structure [56, 63].



(a) (b)

Figure 2.18 (a) Simplified cross-section of the CIGBT and (b) the equivalent circuit.

2.2.4 Self-clamping Feature of CIGBT

After the CIGBT structure turns on, current is continuously controlled by the MOS gate. As the P-base/N-well junction is reverse biased, with increase in the anode voltage, the depletion boundary within the n-well region moves towards the P-well junction. Finally, the N-well region will punch through at a pre-defined voltage, termed as "self-clamping" voltage. Any further increase of the anode voltage is supported by the P-well/N-drift junction, as shown in Figure 2.19. Under this condition, the cathode cells are protected from exposure to high anode voltages. More importantly, since the MOS cells are clamped, the saturation current is largely independent of collector voltage and therefore wider Safe Operating Area (SOA) can be achieved. It should be noted that the N-well dose poses a trade-off relationship between the on-state behaviour and the SOA [64]. Increasing N-well dose can improve the on-state performance due to higher current gain of the internal NPN (N-well/P-well/N-drift) transistor. However, this method will also impair the short-circuit capability due to increased self-clamping voltage.

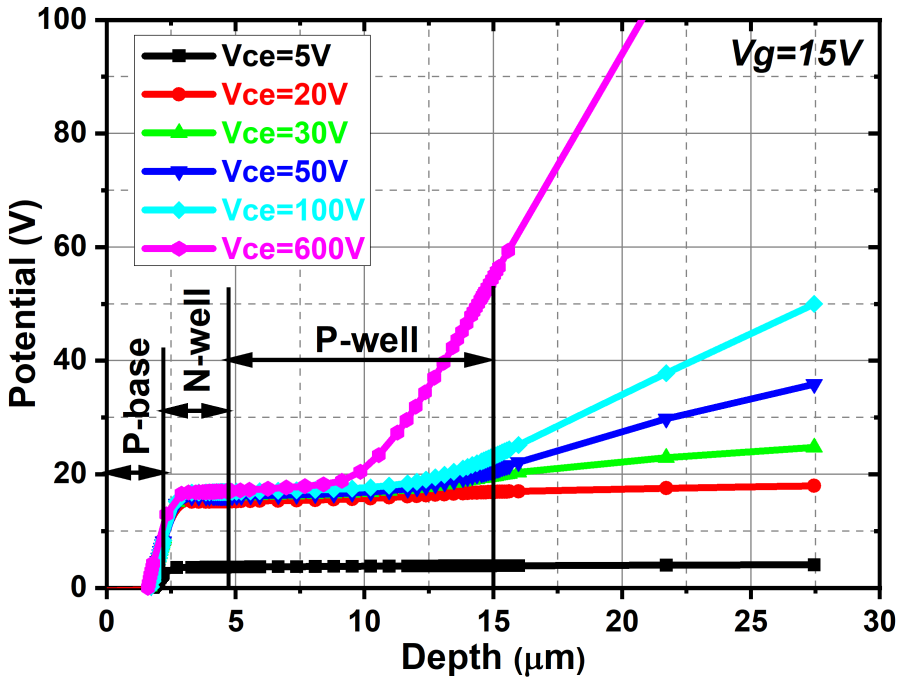
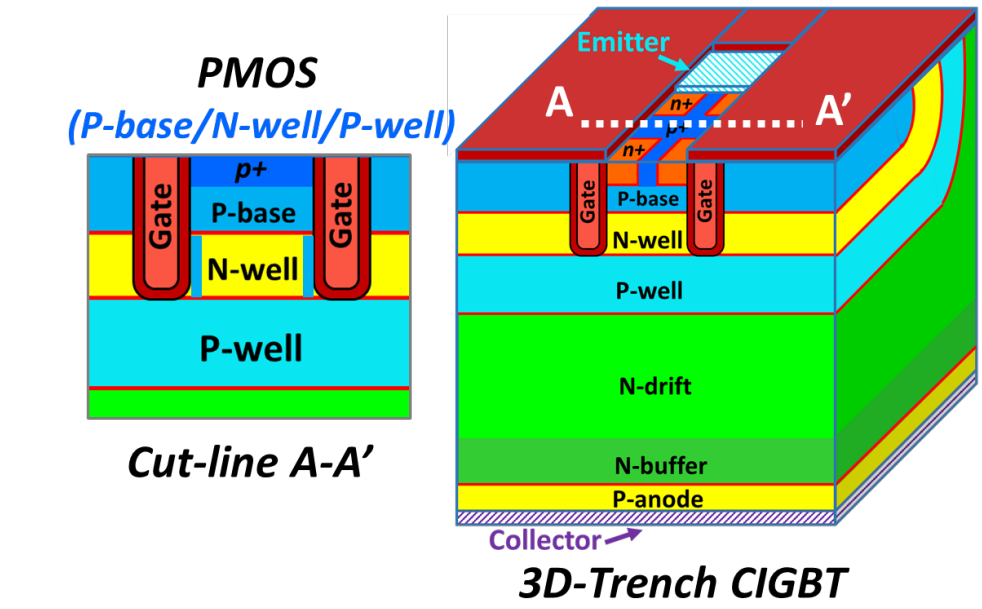
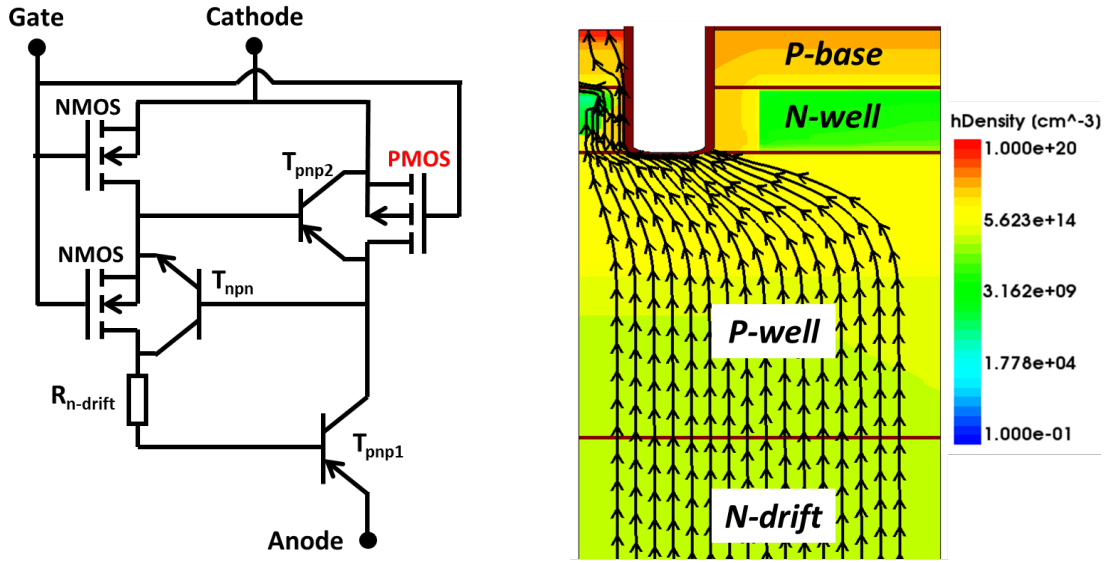


Figure 2.19 Self-clamping feature of the CIGBT.



(a)



(b) (c)

Figure 2.20 (a) PMOS structure in the TCIGBT, (b) equivalent circuit of TCIGBT and (c) the hole current flow lines during turn-off.

2.2.5 PMOS Actions of TCIGBT

The PMOS structure in the planar CIGBT (see Figure 2.17(c)) can be integrated into the TCIGBT which features ladder design of the cathode cells, as shown in Figure 2.20(a) and (b). The PMOS structure consists of P-well, N-well and P-base. During device turn-off, the gate voltage is switched to 0 or -15 V. When the collector potential increases to a value beyond the self-clamping voltage, the N-well layer is fully

depleted and the PMOS structure turns on without the necessity of channels. The excessive holes are collected by the deep P-well and swept out by the PMOS actions, as shown in Figure 2.20(c). Therefore, the turn-on of PMOS structure provides a direct evacuation path for excessive holes and the switching energy loss is therefore significantly reduced. Such an option does not exist in conventional IGBTs.

2.2.6 Super-Junction Concept in TCIGBT

Recently, the Super Junction Trench CIGBT (SJ-TCIGBT) shown in Figure 2.17(f) was demonstrated through numerical simulations [62]. The simulation results have shown significant reduction in turn-off losses due to the deep p-pillars, which act as the extension of p-well and therefore increase the efficiency of collecting excessive holes within the drift region, during turn-off transient. Furthermore, the issues of turn-off failures as well as poor short circuit capability of conventional SJ-IGBTs are effectively eliminated in the SJ-TCIGBT structure. This is due to: 1) the deep p-pillars connected to the p-well are actually floating and PMOS is introduced for hole currents pass during turn-off process, and 2) the unique self-clamping feature of TCIGBT can clamp n-well potential to a pre-defined value (typically < 20 V) and therefore help to control the saturation current density.

Figure 2.21 depicts the carrier flow lines and depletion edges movement during turn-off process. As shown, the deep P-pillars provide a direct path for excess holes to evacuate to the cathode side, and then the excess holes are collected by the PMOS structure. Thus, the turn-off speed is dramatically improved compared to the conventional TCIGBT.

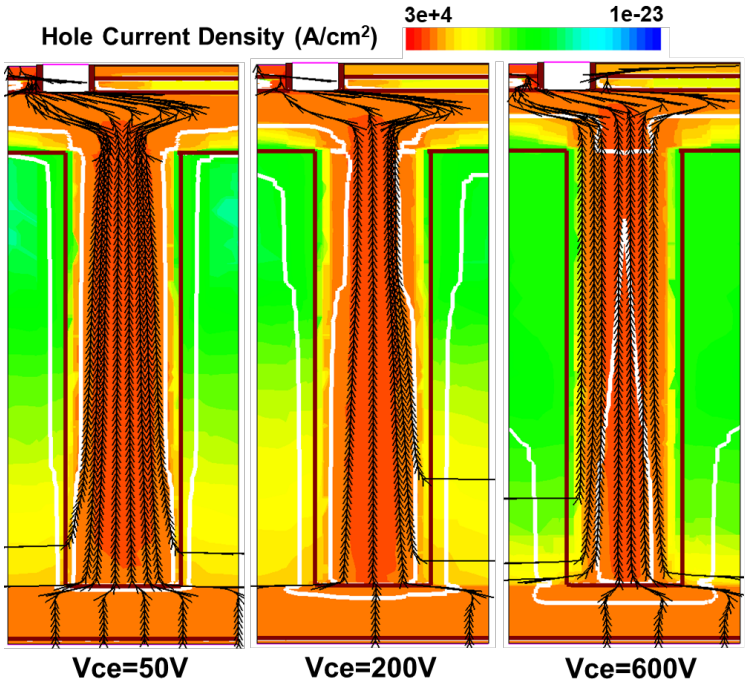


Figure 2.21 Current flow lines during different phases of the turn-off of the SJ-TCIGBT. (White lines indicate the depletion boundaries.)

2.3 Summary

In this chapter, the history and fundamentals of IGBT technologies and MOS-controlled thyristors are explained in detail. The state-of-the-art IGBT technologies and future perspectives are also presented. Following that, the evolution and device physics of the Clustered IGBT are shown with diagrams.

The main body of this thesis will now focus on improving the power efficiency and density of the MOS-gated bipolar devices to meet the future perspectives of IGBTs.

Chapter 3 3-D SCALING RULES ON CLUSTERED IGBT

In this chapter, an approach for design optimization of medium voltage (≤ 1700 V) trench Clustered IGBT and high voltage (≥ 3300 V) planar Clustered IGBT is proposed and investigated through TCAD simulations. Novel 3-D scaling rules are employed in this approach to improve the electrical characteristics. Scaling down results in an enhancement of current gain of the inherent thyristor action which reduces the forward voltage drop. In addition, the self-clamping feature is enhanced in the scaled devices, which help control the current saturation levels. Finally, by integrating the 3D scaling rules with the trench Clustered IGBTs, the on-state performance shows significant improvement compared to the state-of-the-art IGBT technologies and also exhibits great potential to outperform the high voltage SiC unipolar devices. Therefore, scaling rules on Clustered IGBTs is a highly promising approach for enhancing the converter efficiency in medium to high voltage applications.

3.1 Introduction

IGBTs are the main power switching devices used today for voltages up to 6.5 kV. For medium voltage (≤ 1700 V) power electronics applications, IGBTs are widely used in Electric Vehicle (EV), Pulse Width Modulated (PWM) servo and three-phase motor drives requiring high dynamic range control and low harmonics. Significant efforts have been made to reduce their on-state and switching power losses because of their direct impact on energy savings. For high voltage (≥ 3300 V) power electronics applications, due to high current handling capability and high reliability, IGBTs are widely used in industrial motor drives, transportations and smart power grids. Compared to the current-controlled thyristor devices such as Integrated Gate Commutated Thyristor (IGCT) and Gate Turn-Off thyristor (GTO), voltage controlled IGBTs can provide much higher switching frequency with smaller converter footprint and higher reliability [49]. Hence, the voltage controlled converter technologies that utilize high voltage IGBTs are gradually replacing the line commutated converter

options which are based on thyristor technologies in the HVDC transmissions [49]. However, the IGBTs exhibit higher on-state losses than thyristor devices due to lower on-state carrier densities as a result of lower current gains. Therefore, the MOS-Controlled Thyristor (MCT) devices are highly desirable to combine the advantages of both IGBTs and thyristors. Among the proposed MCT concepts, the Clustered IGBT (CIGBT) is the only MCT technology that has been experimentally demonstrated to show low on-state losses due to thyristor conduction, excellent current saturation behaviour due to inherent self-clamping feature, and also fast switching speed due to PMOS actions [57]. Therefore, the CIGBT is a highly promising technology for medium-high voltage power applications.

Most recently, a "More-than-Moore" concept [65] has been extended to IGBTs to enhance their power densities and ensure compatibility with nanometric CMOS technology. The scaling concept proposed for the Trench gated IGBT [28, 66] showed significant lowering of the on-state voltages ($V_{ce(sat)}$) due to the Injection Enhancement (IE) effect [17]. The IE effect can be defined as a mechanism to enhance electron concentration within the drift region of an IGBT beyond that realized purely by MOS channel conduction. This effect increases the drift region cathode side carrier concentration and enables a p-i-n diode like carrier profile. The same effect is used in 1D scaling of mesa width [25], 2D and 3D scaling of cathode cells [28, 66] as well as deep sub-micron designs [24]. However, the IE effect also results in non-saturation of the MOS channel current, leading to significant degradation of short circuit withstand capability [23, 32]. During the short-circuit mode, devices need to sustain simultaneously high voltage and high current, causing a significant increase in the local device temperature due to high-power dissipation. The device must survive under such abnormal conditions until the system protection circuit shuts down the driving signal. The reduction in short circuit capability in scaled TIGBT is attributed to the Collector Induced Barrier Lowering (CIBL) effect [23], which is caused by conductivity modulation in the MOS channels [32].

In this chapter, different 3-D scaling rules are proposed for trench CIGBT and planar CIGBT, respectively. 3-D TCAD tools are employed to investigate the electrical characteristics in depth. Finally, the on-state performances of the scaled CIGBTs are compared with the scaled IGBTs, the theoretical IGBT performance limit and also state-of-the-art IGBT technologies.

3.2 3-D Scaling Rules for Medium Voltage Trench CIGBT

3.2.1 Device Structure and Operation

The top view of the Trench CIGBT (TCIGBT) topology design and a 3-D cross section view of a 1.2 kV TCIGBT unit cell are shown in Figure 3.1. The unique designed ladder structure features several stripe shaped trenches running in parallel across the active cluster cells. The device thickness is 100 μm to achieve a 1.2 kV blocking capability. The turn-on mechanism has been explained in Chapter 2.2.3.

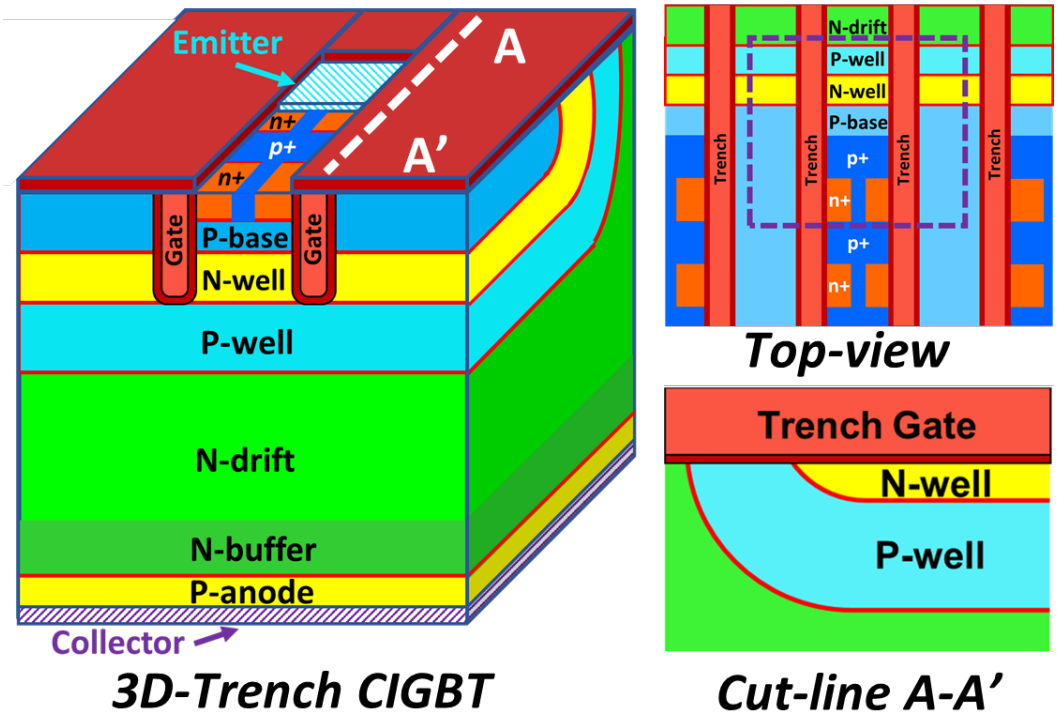


Figure 3.1 Top view of the TCIGBT ladder design at the edge of the cluster cell and a 3-D unit cell of the TCIGBT structure.

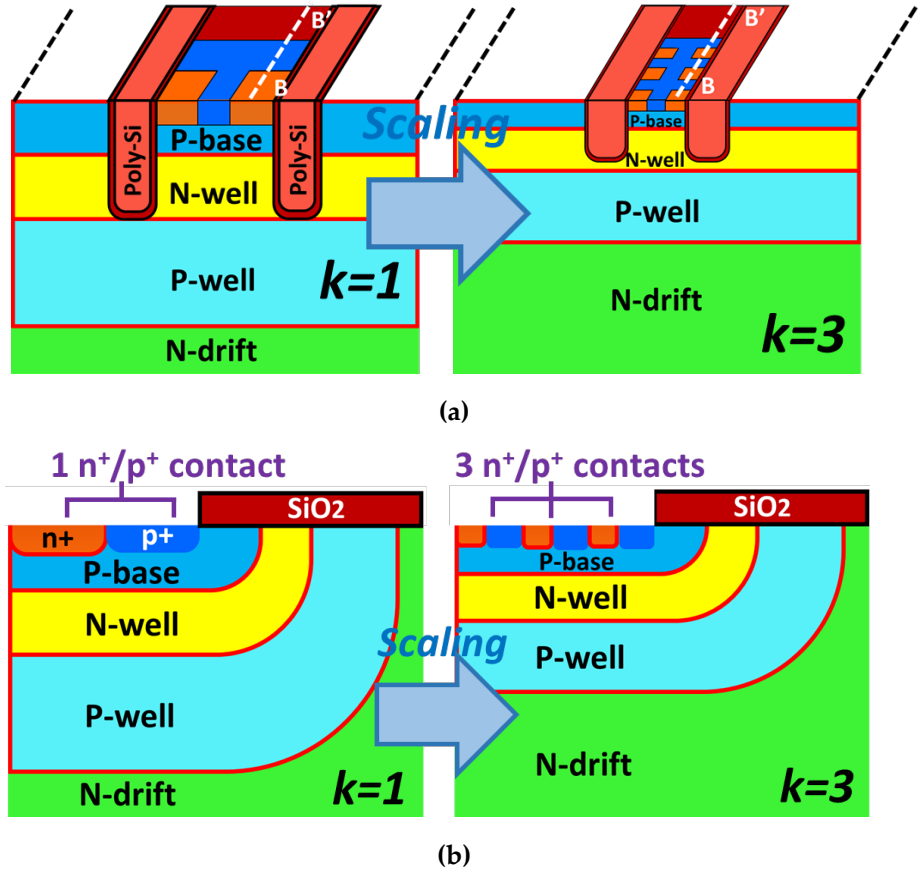


Figure 3.2 (a) Scaling principle on 3D TCIGBT. (b) Cross-sectional view of cut-line B-B′.

3.2.2 3-D Scaling Concept for Trench CIGBT

Figure 3.2 shows the concept of 3-D scaling rules on the TCIGBT. More details regarding the structural parameters and scaling rule are shown in Figure 3.3 and Table 3.1. The cell width is kept identical in all cases for comparison. However, the structural parameters of cathode cells are shrunk as a factor of k. The n^+/p^+ lengths which are perpendicular to the cross-section are shrunk as factor k as well to avoid latch-up. Hence, the scaling rule is applied in all the three dimensions. Moreover, it should be noted that additional scaling rule for the N-well and P-well depths are carefully selected as a factor of $k/2$. This is because the scaling rule on the n-well and p-well regions is determined by the blocking capability as well as current saturation characteristics.

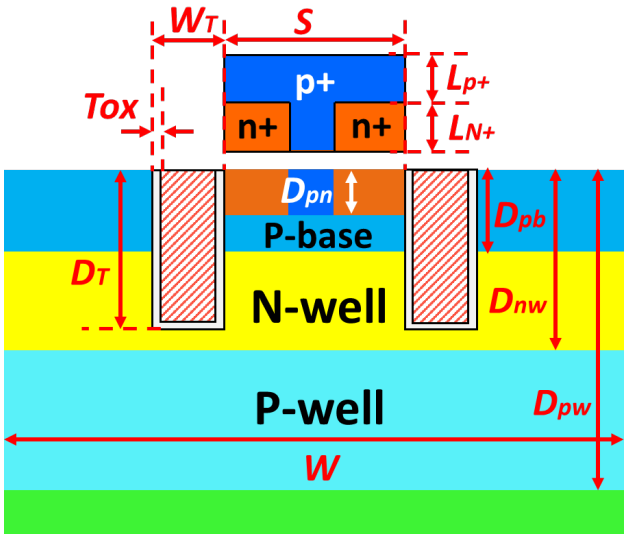


Figure 3.3 Parameters specified in TABLE 5.1.

Parameters & Characteristics	*Symbol (Unit)*	*k=1*	*k=2*	*k=3*	*k=4*	*k=5*	*Scaling factor*
Cell Width	$W\ (\mu m)$	10	10	10	10	10	*1*
Trench Width	$W_T\ (\mu m)$	1	1	1	1	1	*1*
Trench Depth	$D_T\ (\mu m)$	4.5	2.25	1.5	1.12	0.9	*k*
Mesa Width	$S\ (\mu m)$	3	1.5	1	0.75	0.6	*k*
n+/p+ Depth	$D_{pn}\ (\mu m)$	0.5	0.25	0.17	0.12	0.1	*k*
n+ Length	$L_{n+}\ (\mu m)$	1.5	0.75	0.5	0.37	0.3	*k*
p+ Length	$L_{p+}\ (\mu m)$	4.5	2.25	1.5	1.12	0.9	*k*
Gate Oxide Thickness	$T_{ox}\ (\mu m)$	0.1	0.05	0.03	0.025	0.02	*k*
P-base Depth	$D_{pb}\ (\mu m)$	2	1	0.67	0.5	0.4	*k*
N-well Depth	$D_{nw}\ (\mu m)$	4.5	4.5	3	2.25	1.8	*k/2*
P-well Depth	$D_{pw}\ (\mu m)$	15	15	10	7.5	6	*k/2*
P-base Doping	cm^{-3}	2×10^{17}	2.4×10^{17}	2.8×10^{17}	3.2×10^{17}	3.6×10^{17}	-
Gate Voltage	$V_g\ (V)$	15	7.5	5	3.75	3	*k*
Threshold Voltage (25°C)	$V_{th}\ (V)$	4.3	2.1	1.4	1.1	0.9	*k*
Self-clamping Voltage	$V_{scl}\ (V)$	18	15	7	5	4	-
Electron injection efficiency	γ_E	72%	72%	72%	72%	72%	*1*

Scaling rule: *Parameters of scaled (k=2,3,4,5) devices = Parameters of conventional (k=1) device ÷ Scaling factor*

Table 3.1 Parameters and characteristics applied for scaling rules on trench CIGBT.

Figure 3.4 shows the influence of the N-well/P-well depths scaling factors upon breakdown voltages, saturation current densities and self-clamping voltages of the *k3*-TCIGBT. As the P-well/N-drift junction is the main junction to support blocking voltage, the thickness of the scaled P-well must be sufficient to avoid punch-through before avalanche breakdown. If the p-well depth is scaled with *k*, the P-well region is completely depleted before the electric field reaches its critical value under blocking state. This causes cathode cells to be exposed to high voltages and induces premature breakdown. Saturation current density can be reduced by lowering the punch-through voltage and reducing the n-well depth is a direct solution to achieve this. However, the reduction of N-well depth is limited by the turn-on mechanism of TCIGBT. During turn-on process, the n-well layer must provide a sufficient barrier to prevent holes from flowing into the cathode before the thyristor is triggered. Otherwise, the I-V characteristics will display a snap-back. Consequently, the scaling factor for the n-well/p-well depths are chosen as *k*/2. This will ensure that the scaled devices meet the required blocking capability as well as enable large SOA.

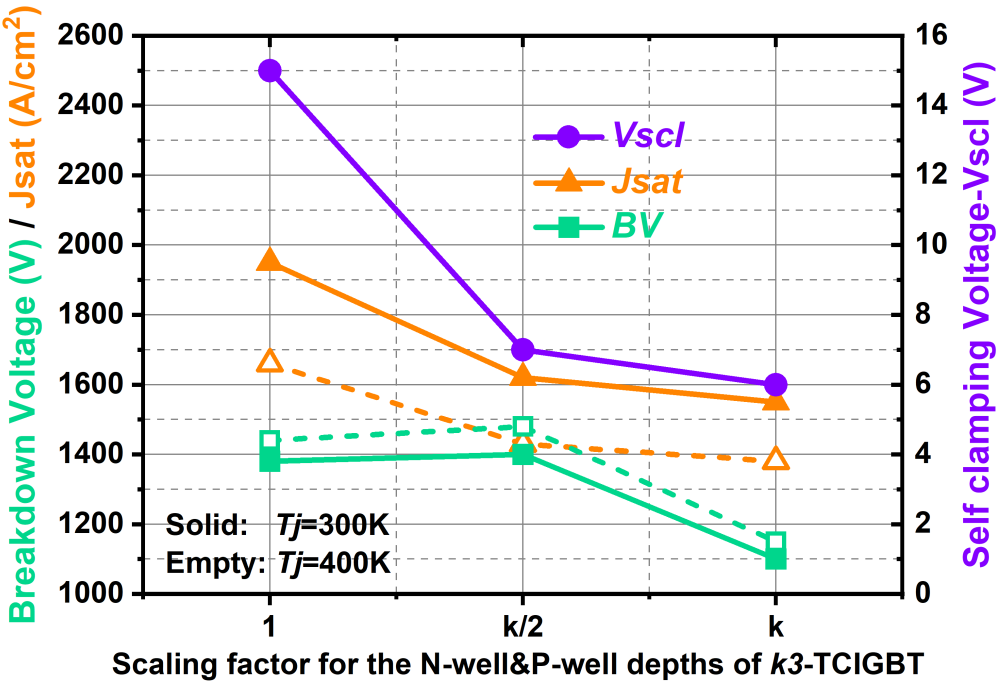


Figure 3.4 Influence of N-well/P-well depths scaling factors upon the breakdown voltages, saturation current densities and self-clamping voltages of *k3*-TCIGBT.

3.2.3 Simulation Setup

The electrical characteristics of the scaled devices are demonstrated by using the 3-dimensional TCAD tools within Synopsys Sentaurus Device [67]. A minority carrier ambipolar lifetime of 10 μs is considered as default. In addition, the IGBT models used in this work are calibrated with the experimental results in [28], as shown in Figure 3.5. In a 3-dimensional TCIGBT, as shown in Figure 3.2(b), due to existence of the n-well and p-well margins, the number of n^+/p^+ contacts employed within a cluster cell influences the electrical characteristics. For the conventional device (k = 1), the variations in forward voltage drops and saturation current densities as a function of number of n^+/p^+ contacts are shown in Figure 3.6. It shows that the $V_{ce(sat)}$ reduces with increasing number of n^+/p^+ contacts while the J_{sat} increases with increased number of contacts. However, both $V_{ce(sat)}$ and J_{sat} saturate when contact number exceeds four. Therefore, the simulated *k1*-TCIGBT involves four n^+/p^+ contacts to provide a more accurate simulation result. Similarly, for an identical device area the *k3*-TCIGBT employs twelve n^+/p^+ contacts.

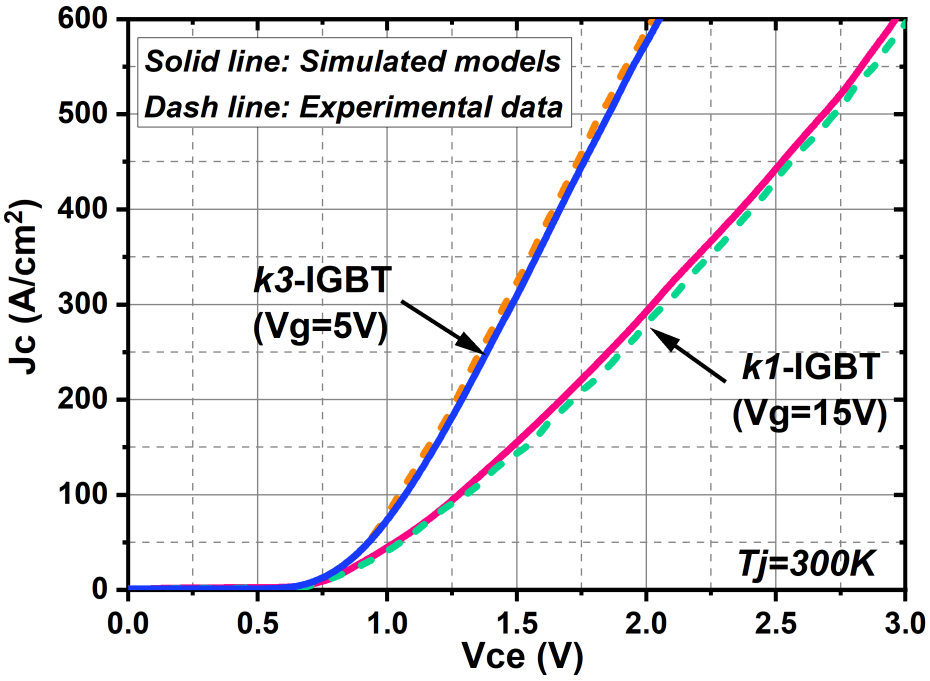


Figure 3.5 Comparison of IV characteristics between calibrated models and experimental data in [28]. The models are then used in the analysis of TCIGBT.

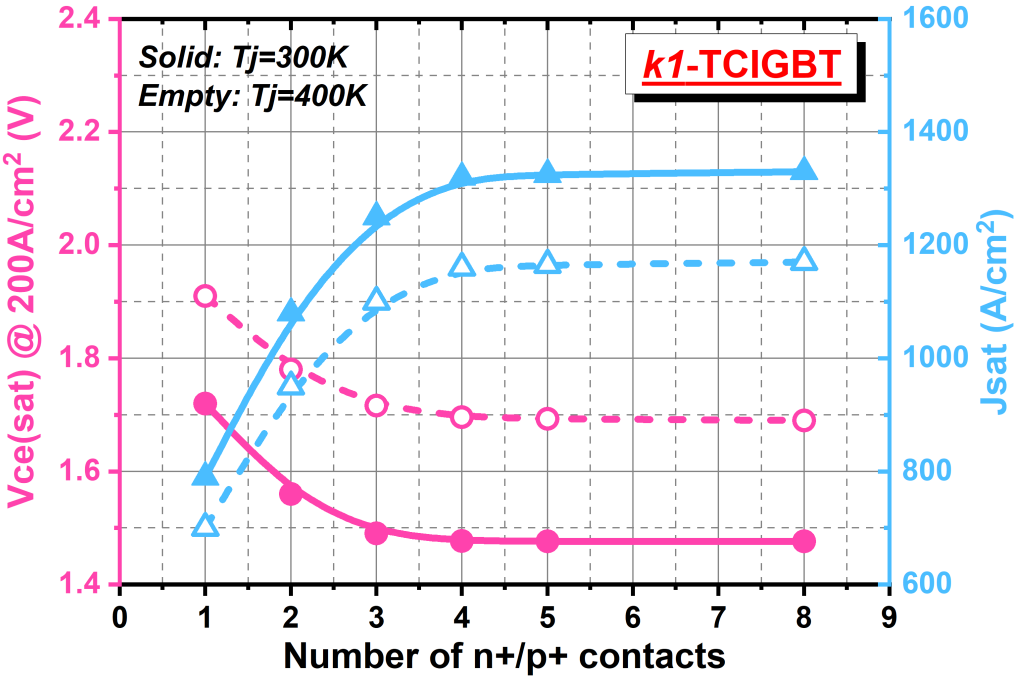


Figure 3.6 Influence of number of n⁺/p⁺ contacts of *k1*-TCIGBT on $V_{ce(sat)}$ and J_{sat}.

3.2.4 Input Characteristics

To reduce the gate voltage with scaling factor k, the threshold voltage V_{th} should also be adjusted by changing P-base doping concentration. As shown in Table 3.1, the V_{th} is scaled as a factor of k by increasing the P-base doping concentration. Hence, the various gate voltages enable the scaled TCIGBT devices tend to be suitable for different digital integrated circuits. Figure 3.7 shows the input characteristics of the conventional and scaled devices. The transconductance of the scaled devices are improved compared to the conventional device as a result of reduced channel length as well as scaled gate oxide thickness. Moreover, the reduction of gate oxide thickness is beneficial to improve the I-V characteristics because of the significantly reduced channel resistance R_{ch}, as expressed in (3.1), where L_{ch} is the vertical channel length, Z is the sum of n⁺ length, μ_{ni} is the inversion layer mobility, and C_{ox} is the gate oxide capacitance.

$$R_{ch}{}' = \frac{L_{ch}/k}{Z \cdot \mu_{ni} \cdot (k \cdot C_{ox}) \cdot [(V_g - V_{th})/k]} = R_{ch}/k \qquad (3.1)$$

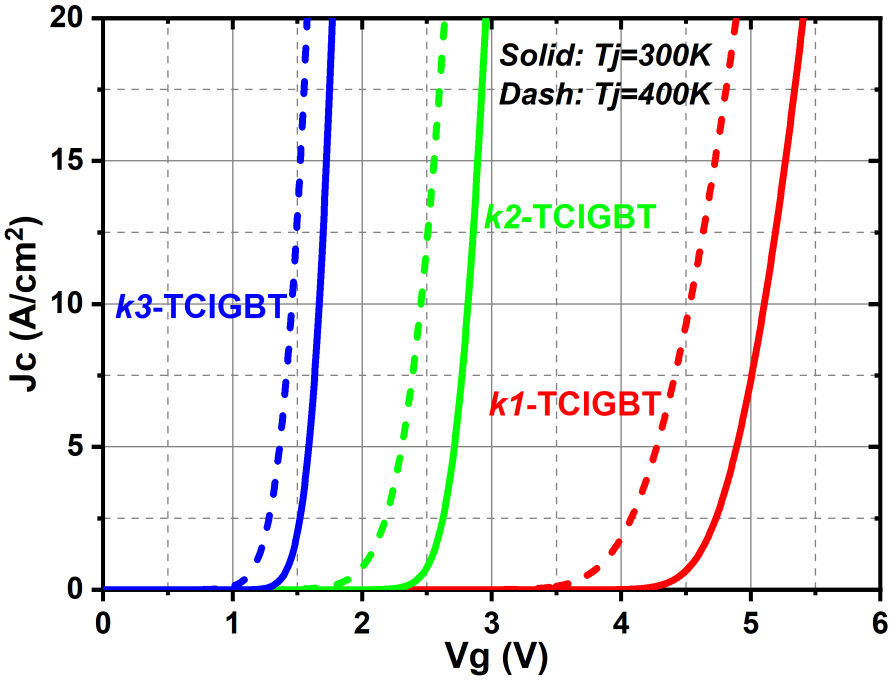
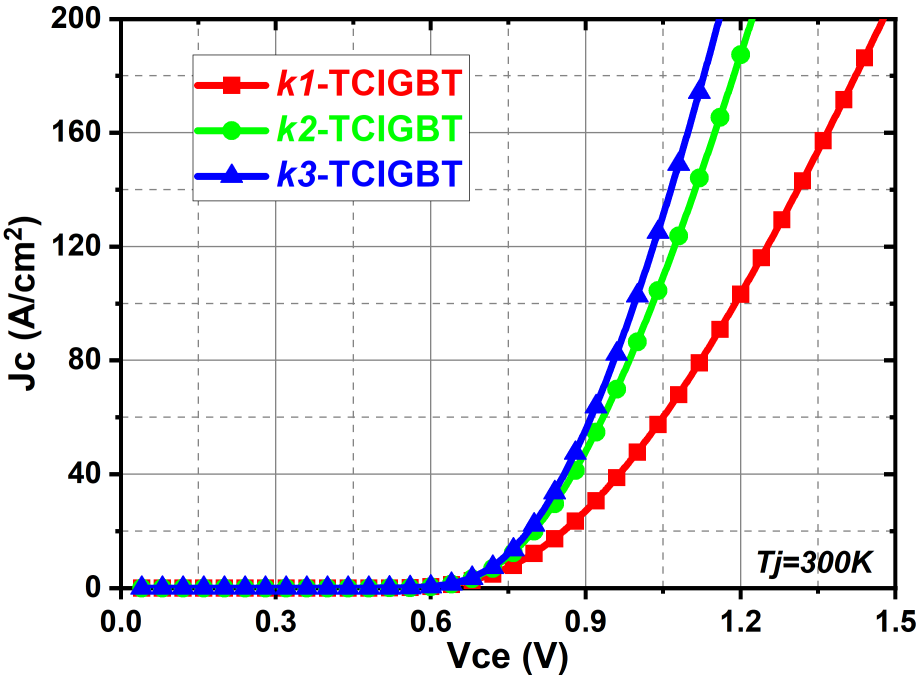


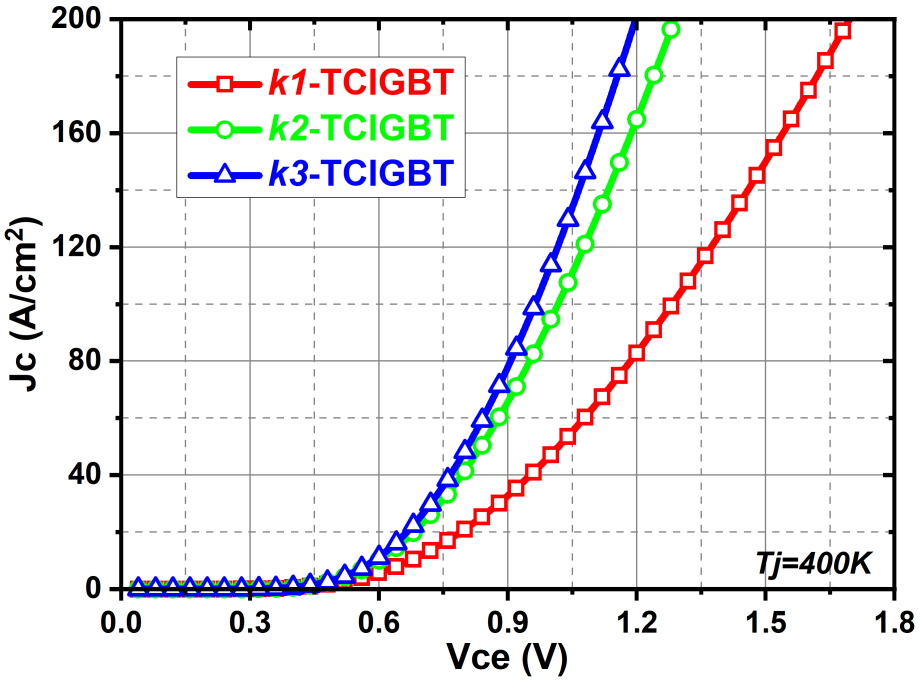
Figure 3.7 Input characteristics of the conventional and scaled TCIGBTs.

3.2.5 I-V Characteristics

Figure 3.8 shows the linear I-V characteristics of conventional and scaled TCIGBTs. The linear I-V characteristics of the *k3*-TCIGBT is significantly improved because of the enhancement of thyristor action, which is discussed further in the later paragraph. Therefore, the *k3*-TCIGBT can achieve a very low $V_{ce(sat)}$ of 1.15 V and 1.19 V at T_j =300 K and T_j =400 K, respectively at a current density of 200 A/cm^2. It should also be noted that, as shown in Table 3.1, the electron injection efficiency does not change with scaling of the device. Hence, IE effect is not presented in the TCIGBT structure. This is further substantiated from Figure 3.9 because the $V_{ce(sat)}$ of conventional and scaled devices increase linearly with increase in cell widths. In fact, the improvement of on-state performance is mainly contributed by enhancement of thyristor effect.



(a)



(b)

Figure 3.8 I-V characteristics of the conventional and scaled TCIGBTs at (a) T_j = 300 K and (b) T_j = 400 K.

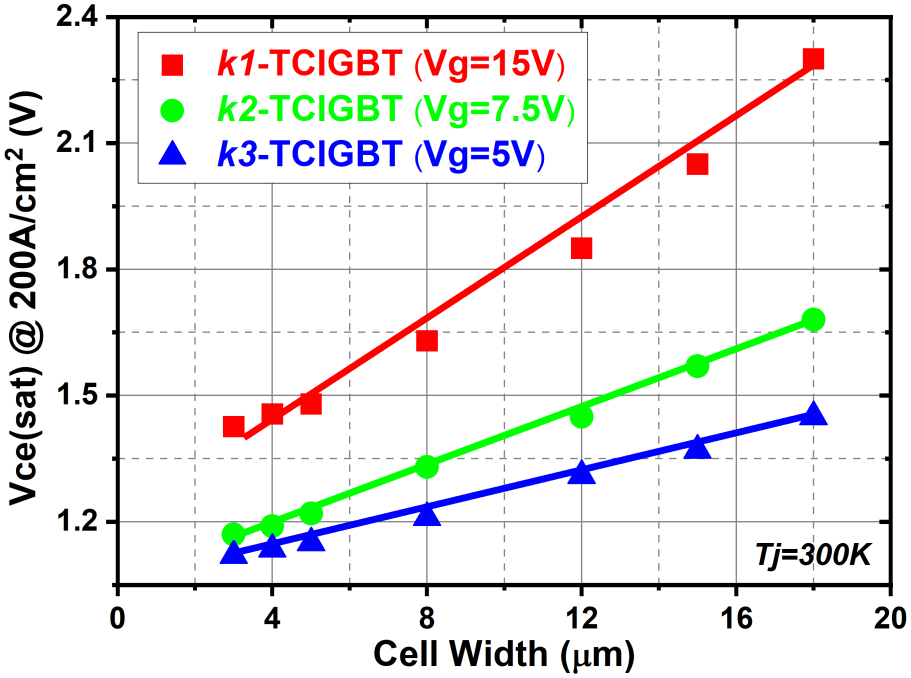


Figure 3.9 $V_{ce(sat)}$ **dependence on cell width of the conventional and scaled TCIGBTs.**

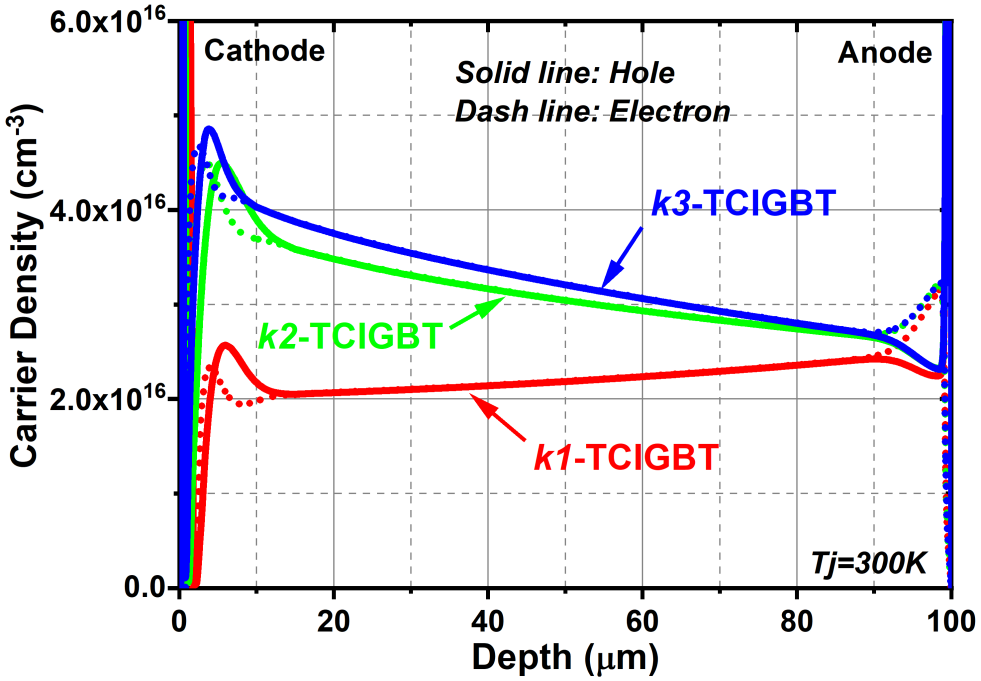


Figure 3.10 Carrier distributions within conventional and scaled TCIGBTs at J **= 200 A/cm².**

Figure 3.10 shows the on-state carrier distributions by comparing the scaled TCIGBT devices to the conventional TCIGBT (k = 1). A much higher carrier concentration is seen in $k3$ because of the enhanced thyristor action. The junction injection efficiency of

the N-well/P-well junction can be expressed as in (3.2), where D_p and D_n are the minority carrier diffusion coefficient, which are constant, while Q_p and Q_n are the effective charge of the p-well and n-well regions, respectively. For the *k3*-TCIGBT, the significant decrease of the Q_p/Q_n ratio results in a higher γ [see (3.3) and (3.4)]. Hence, the current gain of the n-well/p-well/n-drift transistor β is increased due to higher emitter injection efficiency [see (3.5) and (3.6)]. In the *k3*-TCIGBT structure, the thyristor effect is significantly enhanced, due to increased current gain as well as reduction in MOS channel resistance, which results in the improvement of its on-state performance.

$$\gamma \cong \frac{1}{1+\frac{D_p Q_p}{D_n Q_n}} \tag{3.2}$$

$$k1\text{: } \frac{Q_p}{Q_n} = 1.51 > \ k3\text{: } \frac{Q_p}{Q_n} = 0.56 \tag{3.3}$$

$$\gamma_{k1} < \gamma_{k3} \tag{3.4}$$

$$\beta = \frac{\gamma}{1-\gamma} = \frac{1}{(1/\gamma)-1} \tag{3.5}$$

$$\beta_{k1} < \beta_{k3} \tag{3.6}$$

Figure 3.11 shows the comparison of on-state voltage drops as a function of *k* between TCIGBTs and benchmark TIGBTs. In both TIGBT and TCIGBT devices, significant decrease in on-state voltage drop are observed because of scaling rules and tend to saturate when *k* exceeds 3. However, in conventional and scaled cases, the TCIGBTs show approximately 15 % reduction in the on-state voltage drops when compared to the equivalent TIGBTs at T_j = 300 K and T_j = 400 K. This is because the thyristor effect offers enhanced conductivity modulation in the TCIGBT. Furthermore, the forward voltage drops of the TCIGBTs are less sensitive to the increase in temperature compared to that of the TIGBTs.

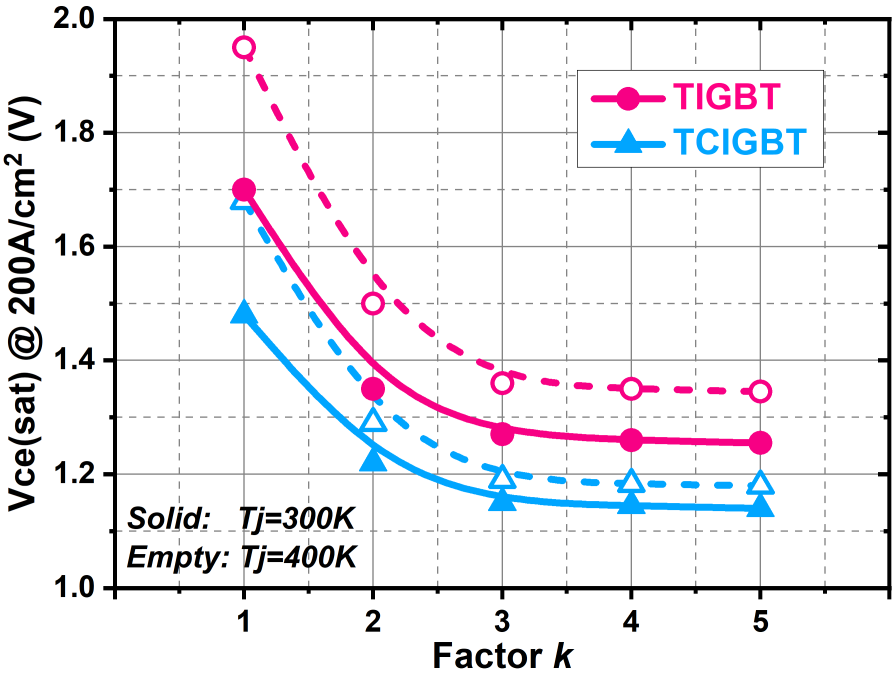
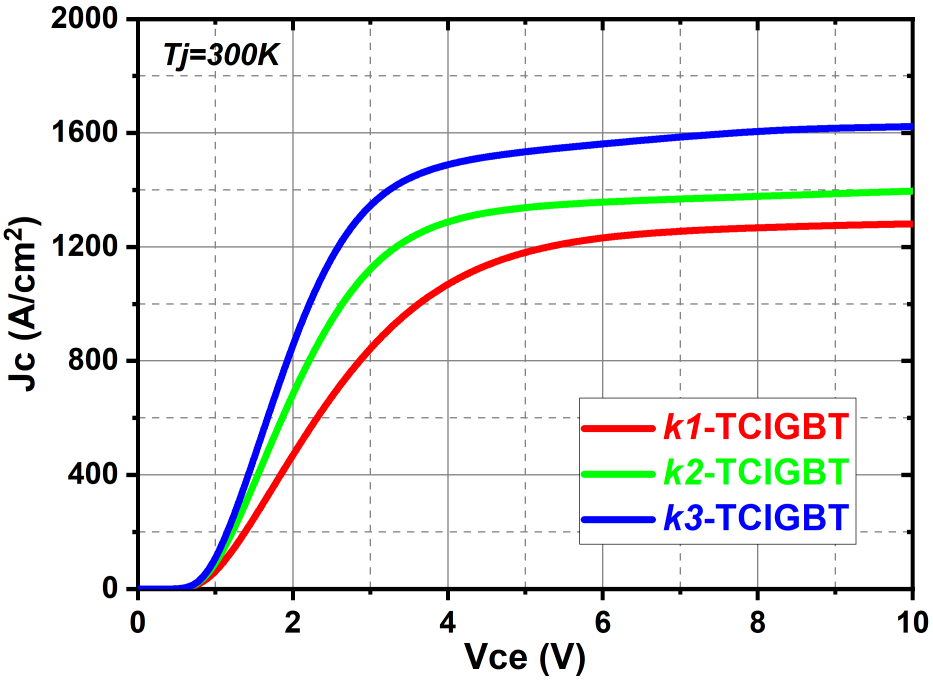


Figure 3.11 $V_{ce(sat)}$ **dependence on scaling factor** k **of TIGBT and TCIGBT.**

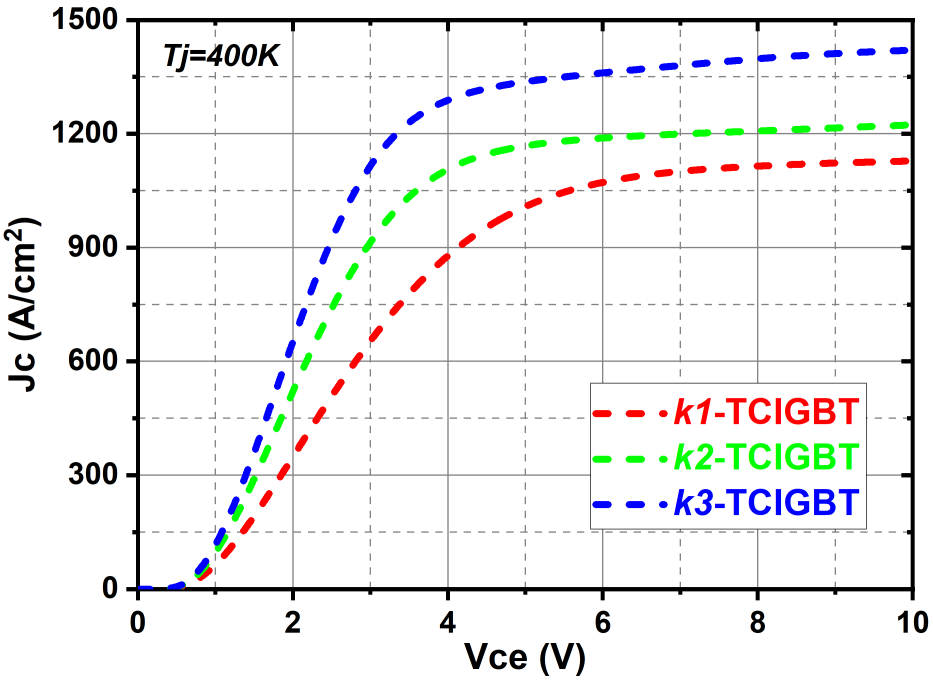
3.2.6 Current Saturation Characteristics

Figure 3.12 shows the current saturation characteristics of the conventional TCIGBT and scaled devices. The self-clamping feature in the TCIGBT technology ensures that current saturation levels do not increase significantly as k increases. In contrast, the scaling work on IGBT technology suffers from the absence of current saturation, as shown in Figure 3.13. This is originated by the potential barrier lowering in the middle of mesa regions [31]. Figure 3.14 depicts the on-state potential distributions within the mesa regions of the $k3$-TCIGBT device compared to a $k3$-IGBT device. As shown, the potential barrier of the n^+/P-base junction in an IGBT reduces significantly with increased collector voltage. Under this condition, the bipolar carriers flow is enhanced, and the current does not show clear saturation, as shown in Figure 3.13. This will finally degrade the short circuit robustness and reduce the SOA of an IGBT. This problem can be effectively suppressed with TCIGBT technology due to the self-clamping feature. The potential in the n-well region is clamped and the potential barrier of the n^+/P-base junction shows no obvious increase and tends to be independent of collector voltages. This is one major attractive feature over the TIGBT.

It should also be noted from Figure 3.13 that despite the *k3*-TCIGBT shows lower $V_{ce(sat)}$ in the linear I-V characteristics, 1/3 reduction in saturation current density can be achieved compared to that of the *k3*-TIGBT.



(a)



(b)

Figure 3.12 Current saturation characteristics of the conventional and scaled TCIGBTs at (a) T_j = 300 K and (b) T_j = 400 K.

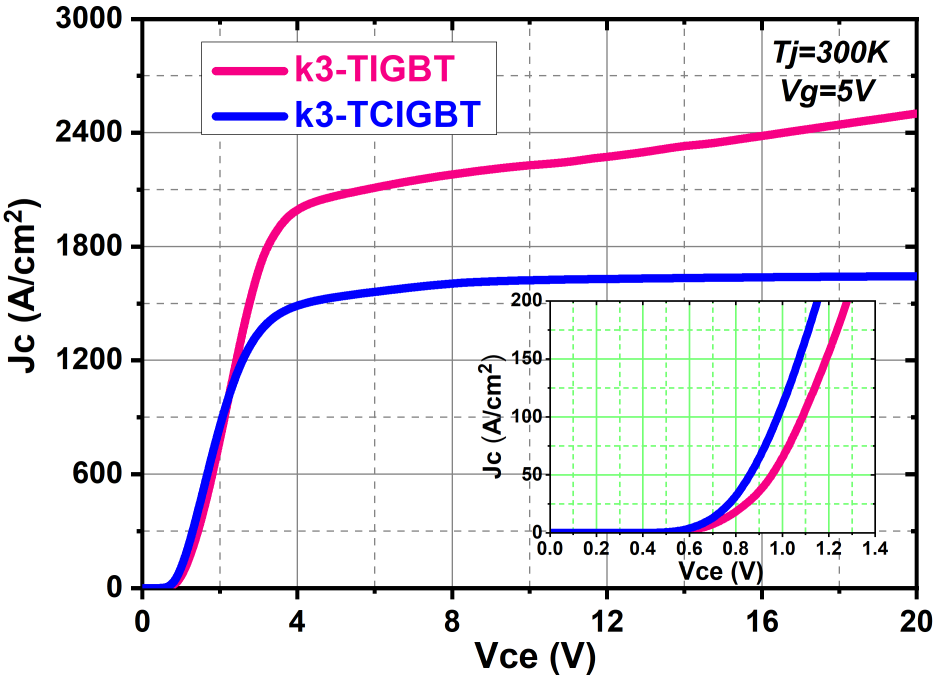
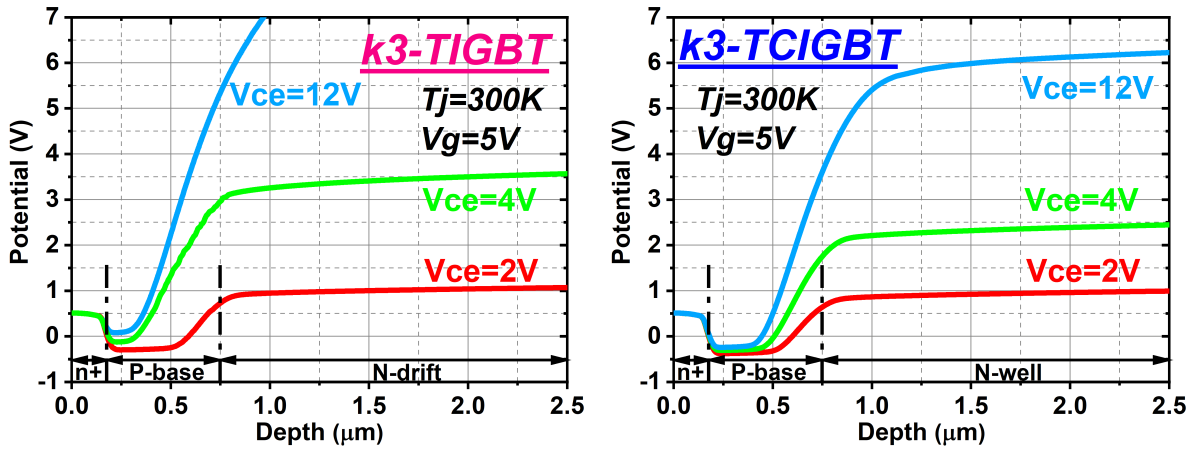


Figure 3.13 Comparison of I-V characteristics between *k3*-TIGBT and *k3*-TCIGBT.



(a) (b)

Figure 3.14 Comparison of potential distributions within the middle of mesa regions between (a) *k3*-TIGBT and (b) *k3*-TCIGBT.

3.2.7 Dynamic Characteristics

The dynamic characteristics of the conventional and scaled devices are investigated by using inductive switching simulations. In the inductive switching test circuit as shown in Figure 3.15, the DC bias is 600 V, the rated current is 100 A (at J = 200 A/cm²) and the stray inductance is 100 nH. Figure 3.16 shows the $V_{ce(sat)}$-E_{off} trade-off

relationships of comparing the scaled devices to the conventional device as well as benchmark *k*3-TIGBT, from which much-improved trade-off in comparison to conventional device (k = 1) is clear. For an identical E_{off}, *k*3-TCIGBT can reduce the $V_{ce(sat)}$ by 20 % and 30 % at T_j = 300 K and T_j = 400 K, respectively. Moreover, *k*3-TCIGBT even displays a 10 % reduction in $V_{ce(sat)}$ compared to the calibrated *k*3-TIGBT.

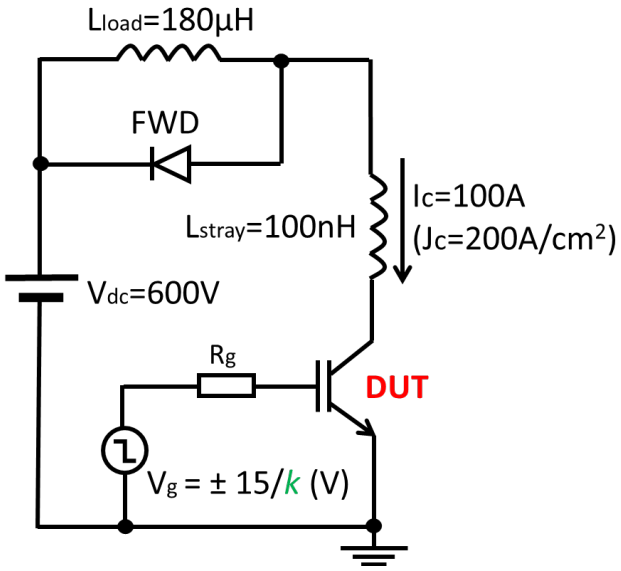


Figure 3.15 Inductive switching test circuit.

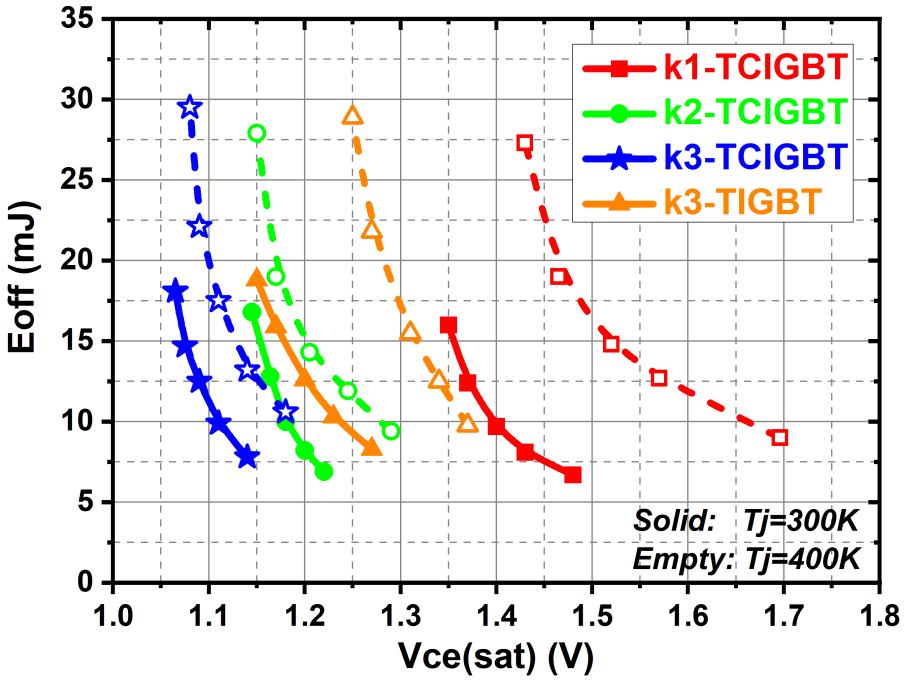


Figure 3.16 Comparison of $V_{ce(sat)}$-E_{off} trade-off at J = 200 A/cm². Each line is a variation of P-anode doping concentration from 5×10¹⁷ cm⁻³ to 1×10¹⁹ cm⁻³.

3.2.8 Short-circuit Characteristics

The short-circuit withstand time prior to failure is directly related to the saturation current level. The device is expected to withstand short-circuit condition for at least 10 μs. Figure 3.17 shows the simulated short-circuit collector current waveforms. As the scaled IGBT does not show current saturation behaviour, the short-circuit performance of the scaled IGBT is not shown herein. The initial junction temperature is set as 400 K while the thermal resistance from the collector electrode to ambient is set as 0.8 cm^2 K/W. It clearly shows that the scaled devices can achieve more than 10 μs short-circuit performance. This short circuit robustness is contributed by self-clamping feature which helps to maintain the saturation current levels.

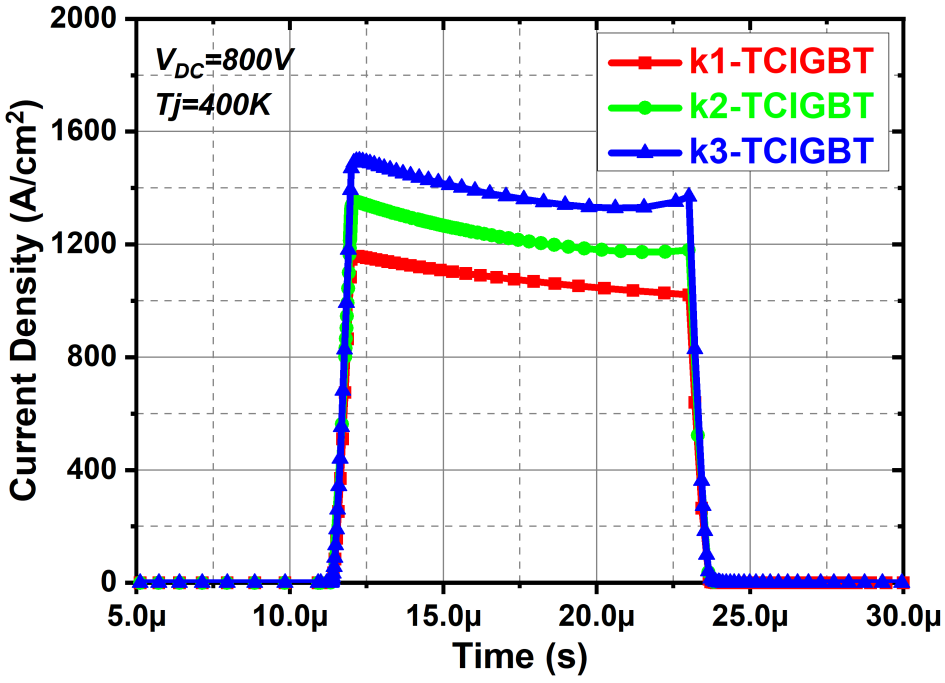


Figure 3.17 Short circuit characteristics of the conventional and scaled devices.

3.3 3-D Scaling Rules for High Voltage Planar CIGBT

In this section, 3-D scaling rules for high voltage planar CIGBTs are proposed to improve the electrical characteristics and widen the safe operating area. A 4.5 kV field-stop planar CIGBT device is analyzed in detail to demonstrate the proposed 3-D scaling rules through 3-D TCAD tools [67]. Different from the previous scaling concept

for trench CIGBT, the scaling rules proposed herein aim to achieve simultaneous reduction in on-state voltage drop and current saturation level.

3.3.1 Device Structure and Operation

Figure 3.18 shows the cross-section view of the 4.5 kV planar CIGBT device and its equivalent circuit. The CIGBT device employs a MOSFET to control a thyristor structure, which consists of N-well/P-well/N-drift transistor (T_{npn}) and P-well/N-drift/P-anode transistor (T_{pnp}). Its turn-on mechanism is identical to the trench CIGBT. The cathode cells feature ladder design and the n^+ cathodes are penetrated by the p^+ cathodes. This unique design is used to suppress the turn-on of the parasitic n^+/P-base/N-well transistor at high current levels. The premature latch-up is therefore avoided during forward conduction.

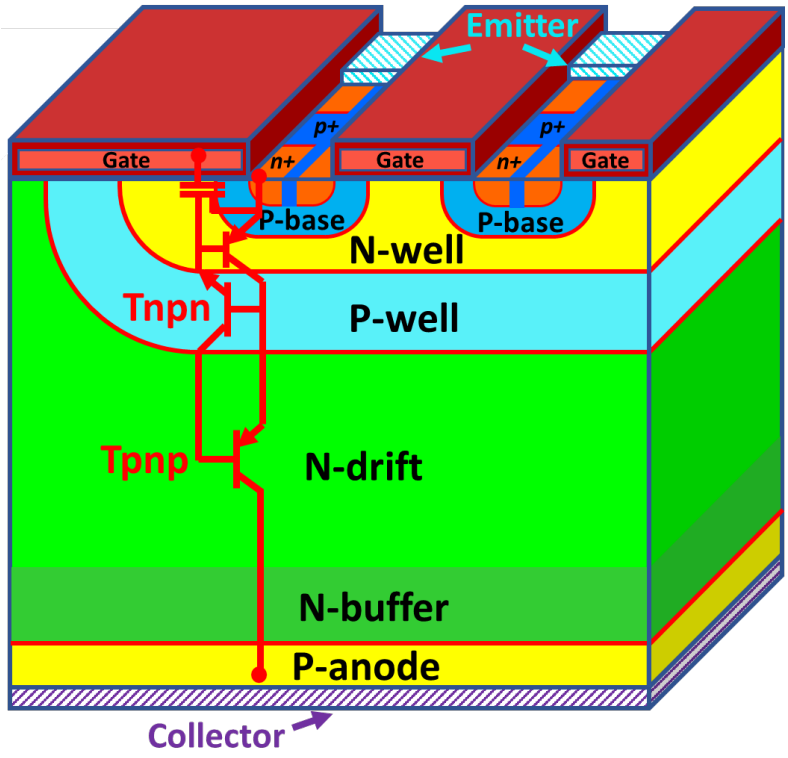


Figure 3.18 3-D cross section view of the planar CIGBT and its equivalent circuit.

3.3.2 3-D Scaling Concept for Planar CIGBT

The proposed 3-D scaling rules and structural parameters are shown in Figure 3.19 and Table 3.2 respectively. As shown, the cell width and device thickness are kept identical for comparison whereas the main structure parameters of the MOS cells are shrunk as a factor of *k*. As the P-well thickness must be sufficient to support at least 5 kV blocking voltage for 4.5 kV device, and the N-well layer must provide a sufficient barrier to prevent holes from entering cathode cells prior to the turn-on of the thyristor, the N-well and P-well depths herein are not scaled and kept constant as conventional values.

Parameters & Characteristics	*Unit*	*k=1*	*k=2*	*k=3*	*Scaling factor*
Cell Width	*μm*	32.7	32.7	32.7	*1*
n^+/p^+ Width	*μm*	1.8	0.9	0.6	*k*
P-base Width	*μm*	6.6	3.3	2.2	*k*
Channel Length	*μm*	2.4	1.2	0.8	*k*
p^+ Length	*μm*	4.5	2.25	1.5	*k*
n^+ Length	*μm*	1.5	0.75	0.5	*k*
Gate oxide thickness	*μm*	0.1	0.05	0.03	*k*
n^+/p^+ Depth	*μm*	0.5	0.25	0.17	*k*
P-base Depth	*μm*	2.5	2	1.5	-
N-well Depth	*μm*	4.5	4.5	4.5	*1*
P-well Depth	*μm*	15	15	15	*1*
P-base doping concentration	cm^{-3}	2×10^{17}	3.2×10^{17}	4.7×10^{17}	-
Gate Voltage (V_g)	*V*	15	7.5	5	*k*
Gate Resistance (R_g)	*V*	7.5	5	3.3	*0.75k*
Threshold Voltage (*25°C*)	*Ω*	22	11	7.3	*k*
Self-clamping Voltage	*V*	21	18	15	-
Electron injection efficiency	-	72%	72%	72%	1

Scaling rule: *Parameters of scaled (k=2,3,) devices = Parameters of conventional (k=1) device ÷ Scaling factor*

Table 3.2 Parameters and characteristics applied for scaling rules on planar CIGBT.

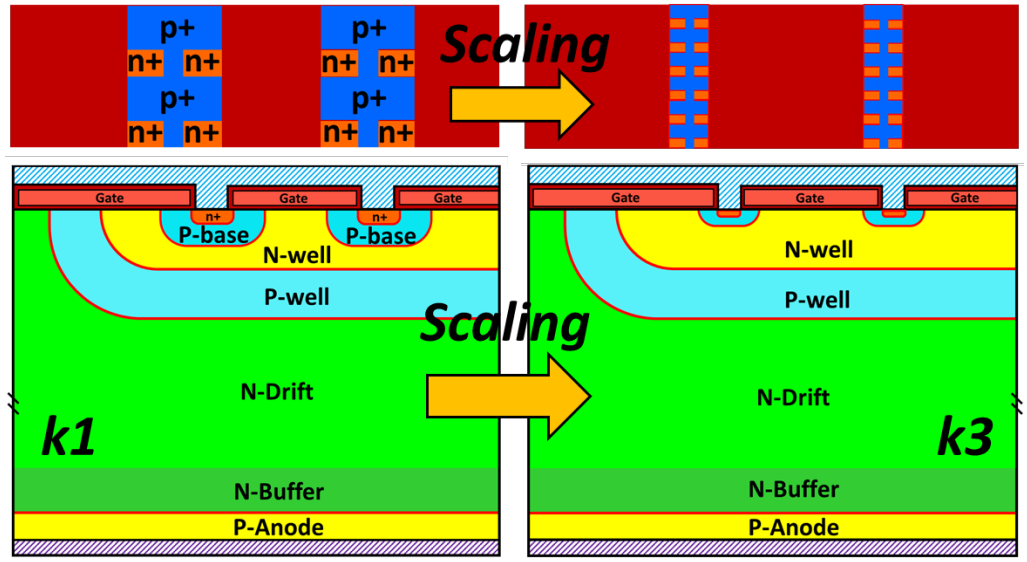


Figure 3.19 3-D scaling concept on the planar CIGBT.

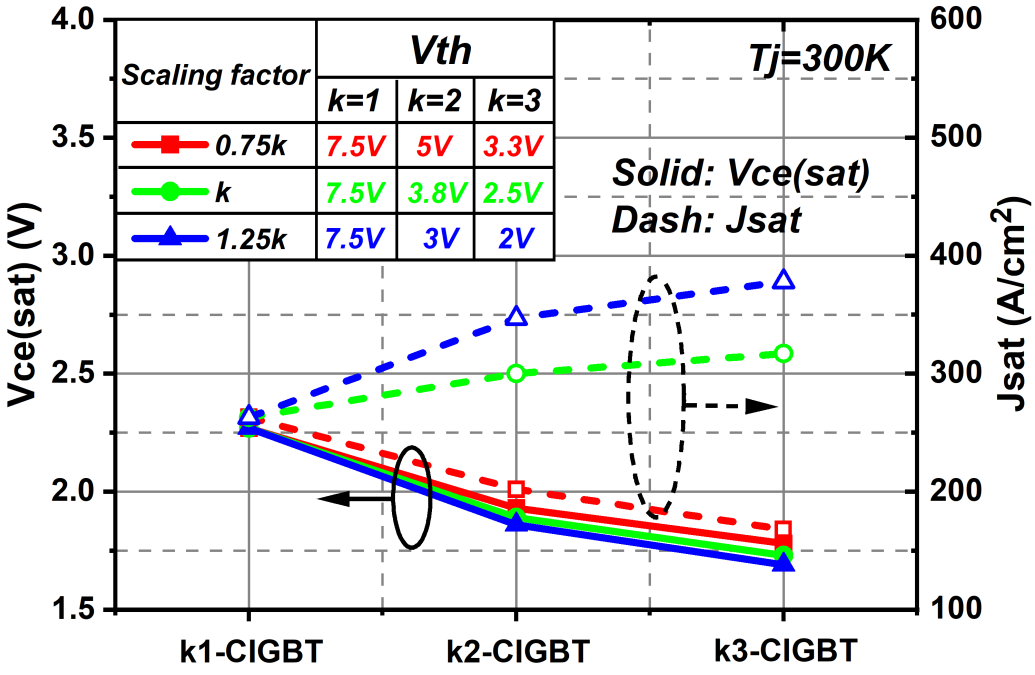


Figure 3.20 Influence of scaling factors for V_{th} upon $V_{ce(sat)}$ and J_{sat}.

In addition, it should be noted that the gate voltage (V_g) is scaled down as k whilst the threshold voltage (V_{th}) is scaled as a factor of $0.75k$. Figure 3.20 shows the influence of different scaling factors for V_{th} upon the $V_{ce(sat)}$ at J_c = 50 A/cm² and the saturation current density (J_{sat}). The J_{sat} is defined as the current density when dI/dV is zero in the I-V characteristics. A carrier lifetime of 50 μs is specified for holes and elections in the

simulations. As shown, the variation of scaling factors for V_{th} has no significant influence upon the decrease of $V_{ce(sat)}$ whilst only the factor $0.75k$ can achieve a decreasing trend of J_{sat}. This is because the P-base doping concentrations of the scaled devices are increased to achieve a factor $0.75k$ for the V_{th}, and the increased P-base doping concentration can reduce the self-clamping voltage (V_{scl}) in the scaled CIGBTs, as shown in Table 3.2.

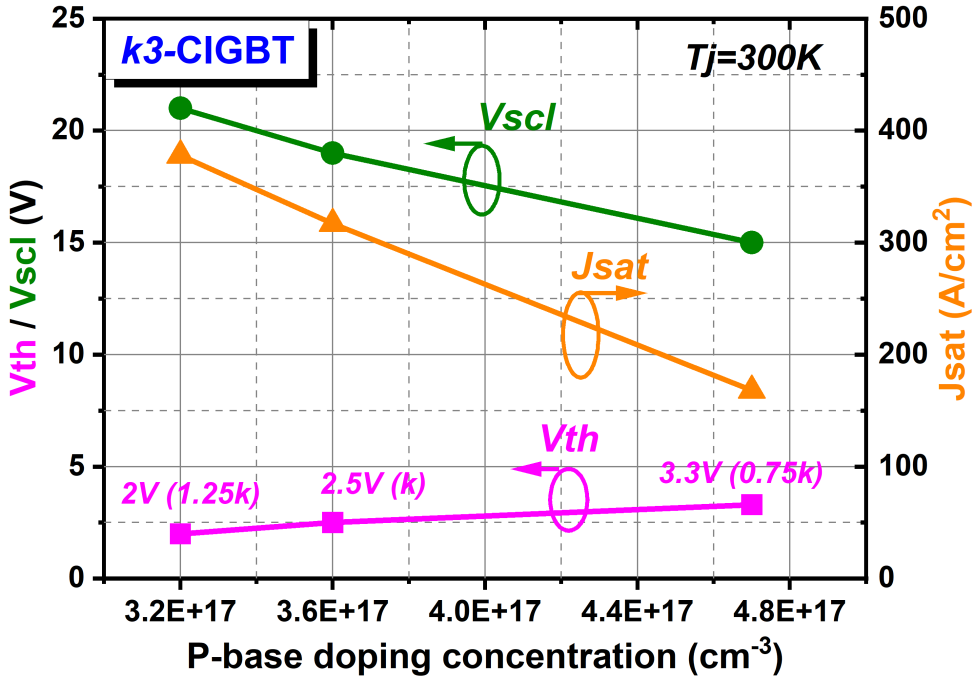


Figure 3.21 Influence of P-base doping concentration upon V_{scl}, V_{th} and J_{sat} in k=3. (V_g-V_{th} = 1.7 V)

In the CIGBT operation, lower V_{scl} can result in a lower J_{sat} [68]. To lower the V_{scl}, increasing P-base doping concentration is a direct solution. Figure 3.21 shows the influence of P-base doping concentration on V_{th}, V_{scl} and J_{sat} in the case of k3-CIGBT. Note that the V_g-V_{th} and the P-base depth are kept identical and the only variation is the P-base peak doping concentration. As shown, the V_{th} is increased with increasing P-base doping concentration whereas the V_{scl} is decreased with increased P-base doping concentration. As the V_g-V_{th} is kept identical, the reduction in J_{sat} is only because of the reduced V_{scl}. The detail reason can be explained as follows: The V_{scl} is essentially the punch-through voltage of the P-base/N-well/P-well transistor. During forward

conduction, the increasing collector voltage is first supported by the P-base/N-well junction. As the collector voltage increases, the depletion boundary within the P-base moves upwards whereas the depletion boundary within the N-well moves downwards. Higher P-base doping concentration can suppress the extension of depletion within the P-base layer. As a result, the N-well layer can be easily depleted with a lower V_{scl} and the J_{sat} is therefore reduced without affecting the $V_{ce(sat)}$. In addition, as shown in Figure 3.22, other scaling factors (*0.6k*, *0.7k*, *0.8k*, *0.9k*) for scaling the V_{th} of *k3*-CIGBT can also result in a reduced J_{sat} compared to the case at a scaling of *k*. However, the $V_{ce(sat)}$ increases dramatically when the scaling factor less than *0.75k*. Therefore, *0.75k* is finally selected for scaling the V_{th} to achieve simultaneous reduction in $V_{ce(sat)}$ and J_{sat}.

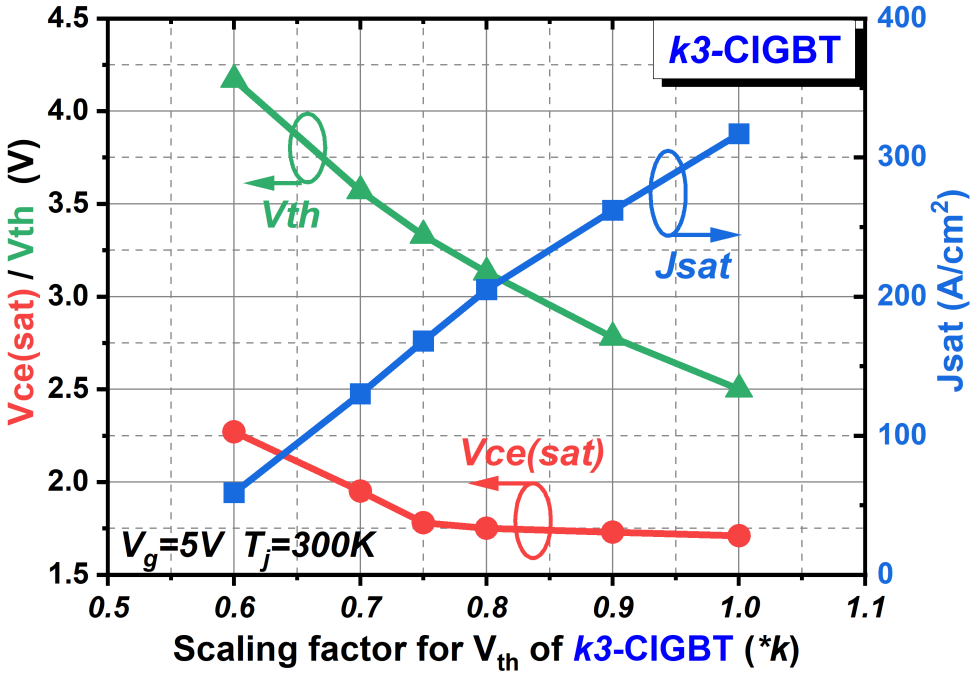


Figure 3.22 Influence of scaling factors for scaling V_{th} upon $V_{ce(sat)}$ and J_{sat} in *k3*-CIGBT. (V_g = 5 V)

3.3.3 Breakdown Characteristics

Figure 3.23 shows the off-state breakdown characteristics of the conventional and scaled devices. During blocking operation, the increasing collector potential is firstly supported by the P-base/N-well junction. After the N-well layer is punched through, the further increase in collector potential is supported by the P-well/N-drift junction.

The MOS cells are protected from high electric field, as shown in Figure 3.24. As the collector voltage is mainly supported by the P-well/N-drift junction, scaling down cathode cells has no influence on the breakdown characteristics.

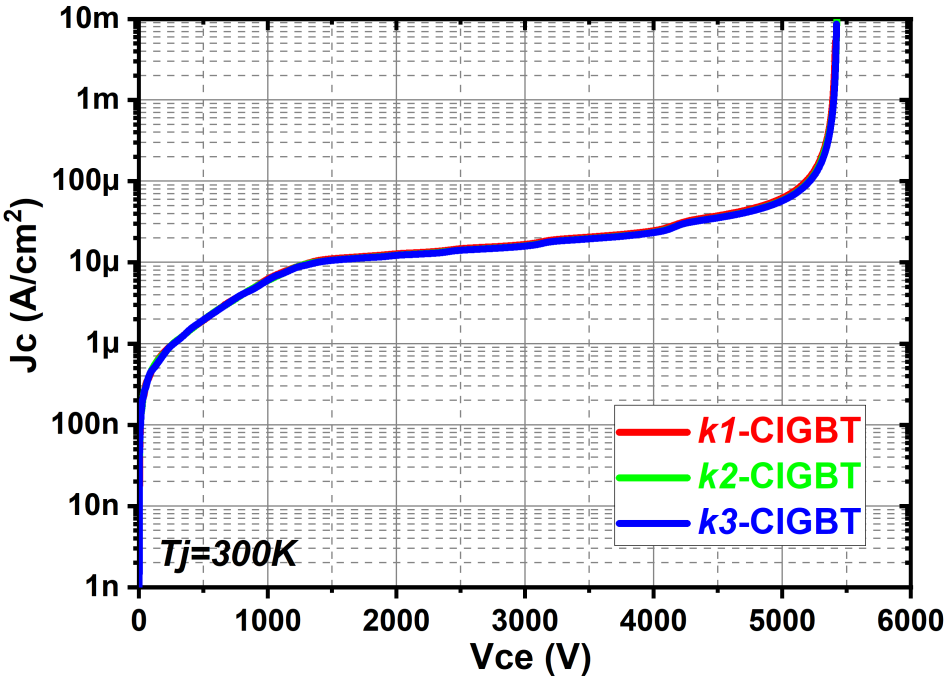


Figure 3.23 Influence of P-base doping concentration upon V_{scl}, V_{th} and J_{sat} in k=3. (V_g-V_{th} = 1.7 V)

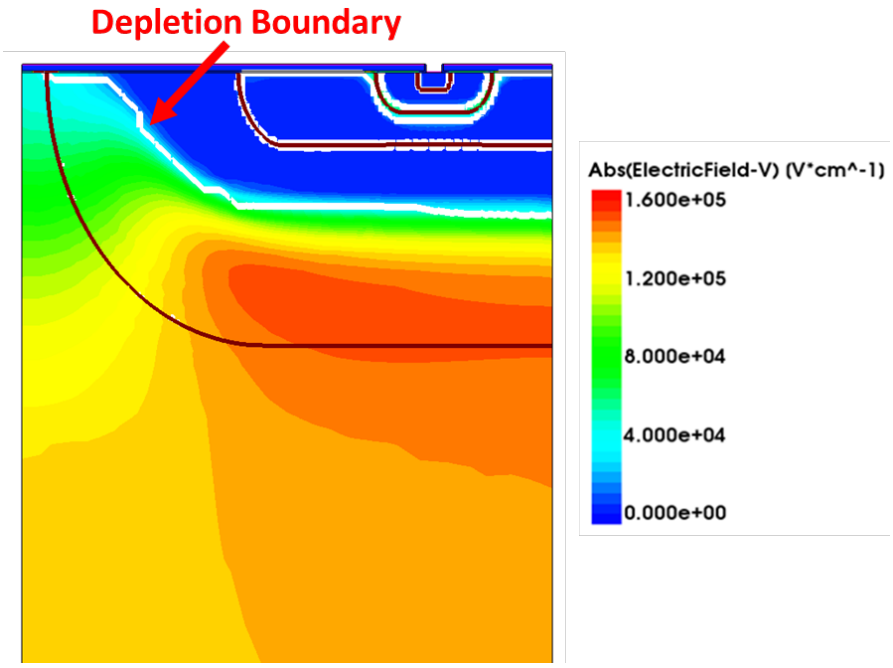


Figure 3.24 Electric field distribution of the cathode side of k1-CIGBT at breakdown voltage.

3.3.4 Transfer Characteristics

Figure 3.25 compares the transfer characteristics of the conventional and scaled devices. The threshold voltages measured at J_c = 100 mA/cm² are shown in Table 3.2. Due to the scaled gate oxide thickness and the channel length, the transconductance of the *k3*-CIGBT shows improvement compared to that of the *k1*-CIGBT.

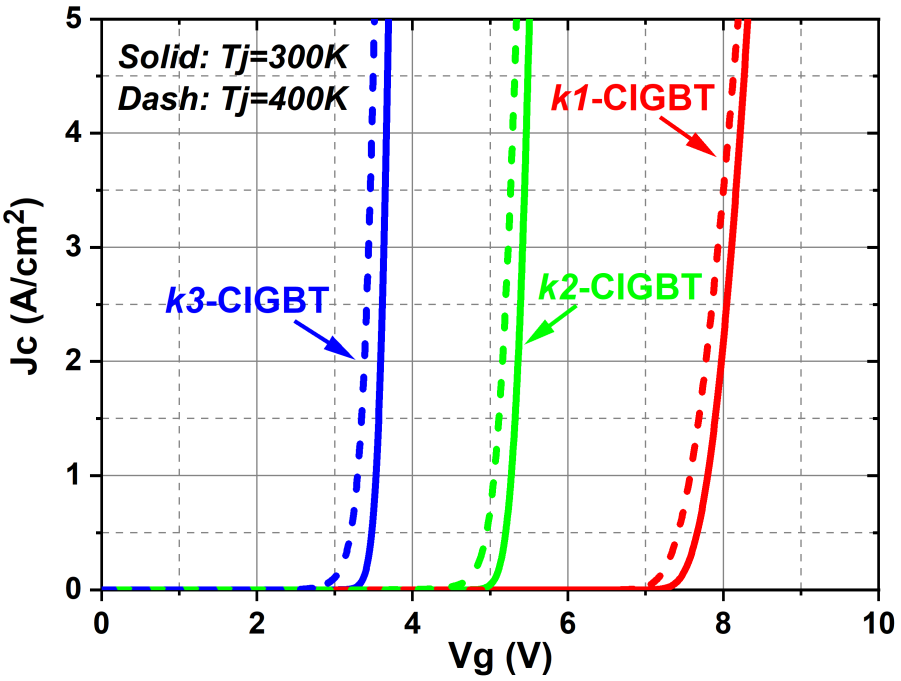
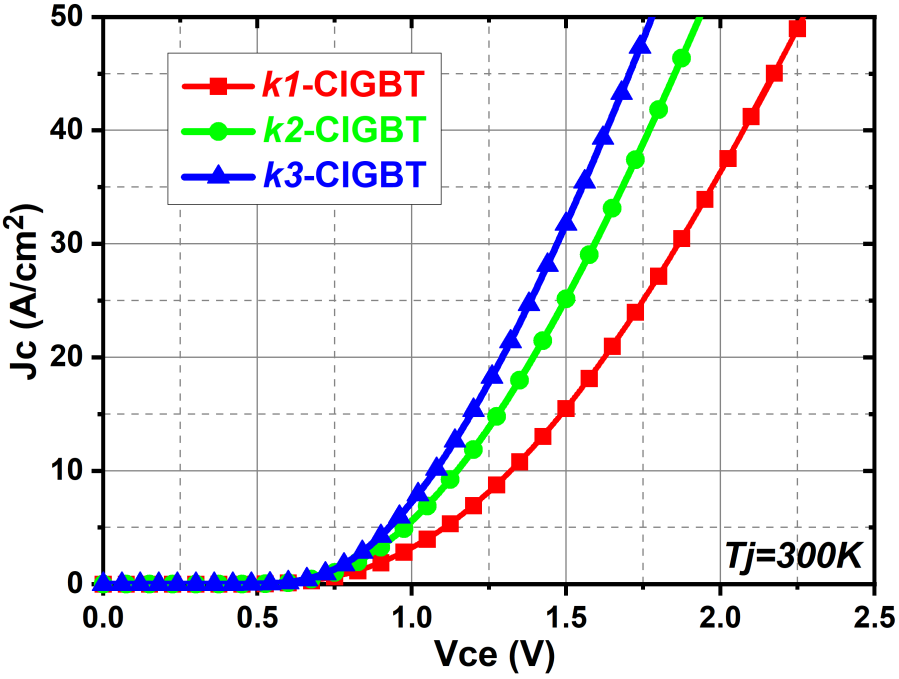


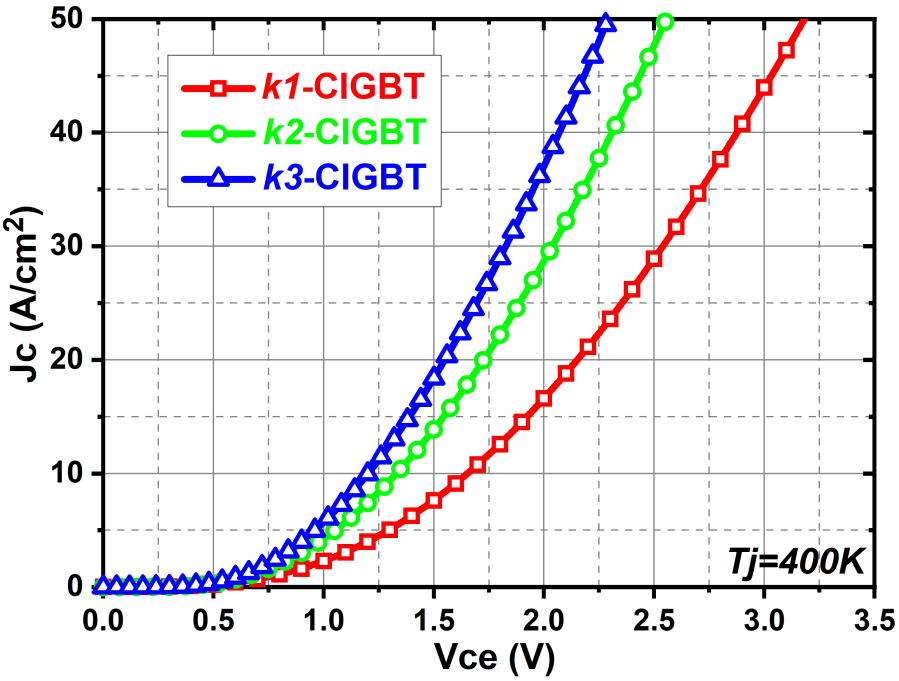
Figure 3.25 Transfer characteristics of the conventional and scaled CIGBTs.

3.3.5 I-V Characteristics

The comparison of the I-V characteristics is shown in Figure 3.26. The carrier lifetime is specified as 50 μs in the simulations. The *k3*-CIGBT can achieve low $V_{ce(sat)}$ (J_{rated} = 50 A/cm²) of 1.78 V and 2.28 V at T_j = 300 K and T_j = 400 K, respectively, which are 22 % and 28 % lower than that of the conventional CIGBT.



(a)



(b)

Figure 3.26 I-V characteristics of the conventional and scaled devices at (a) T_j = 300 K and (b) T_j = 400 K.

Furthermore, the individual components contributing to the on-state voltage drops are specified in Table 3.3. The MOSFET voltage drop is considered to be the potential drop up to 15 μm from the surface. As shown, the MOSFET resistance is reduced in the scaled devices due to lower channel resistance and JFET resistance as a result of

scaling rules on MOS structure. The significant improvement of the on-state performance is mainly contributed by the reduction of voltage drop across N-drift region, which can be attributed to the increased current gain of the N-well/P-well/N-drift transistor (T_{npn}), enhancing the conductivity modulation within the N-drift layer. As the P-base depth is scaled down whereas the N-well depth is constant in the scaled CIGBTs, the N-well layer effective charge is dramatically increased, resulting in a greater emitter injection efficiency of the T_{npn}. Therefore, the thyristor effect is significantly enhanced during on-state, leading to a much higher carrier distribution within the scaled devices, as shown in Figure 3.27.

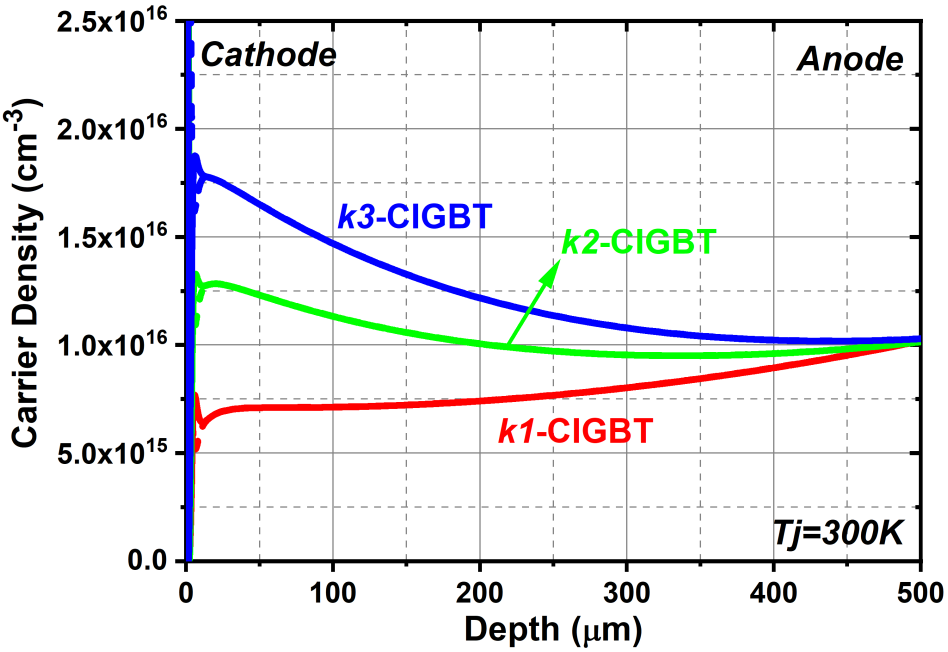


Figure 3.27 Carrier distributions within the drift regions during on-state.

T_j = 300 K	V_{MOSFET}	V_{drift}	V_{jun}	$V_{ce(sat)}$
***k1*-CIGBT (V_g = 15 V)**	0.36	1.21	0.7	2.27
***k2*-CIGBT (V_g = 7.5 V)**	0.27	0.96	0.7	1.93
***k3*-CIGBT (V_g = 5 V)**	0.24	0.84	0.7	1.78

V_{MOSFET}: Voltage drop across MOSFET structure, consisting of channel layer, accumulation layer and JFET region.

V_{drift}: Voltage drop across N-drift region.

V_{jun}: Built in potential of P-anode/N-buffer junction.

Table 3.3 Components of on-state voltage drops.

It is worth mentioning that as specified in Table 3.3, the electron injection efficiency (γ_e) does not vary in the conventional and scaled devices. Therefore, IE effect is not involved in the improvement of on-state behavior. In addition, as depicted in Figure 3.28, due to the optimization of the scaling factor for V_{th}, the J_{sat} of the *k*3-CIGBT is reduced to ~ 3 times of the rated current density. Therefore, compared to the conventional CIGBT, a simultaneous reduction in $V_{ce(sat)}$ and J_{sat} can be achieved by the scaling rules on planar CIGBTs.

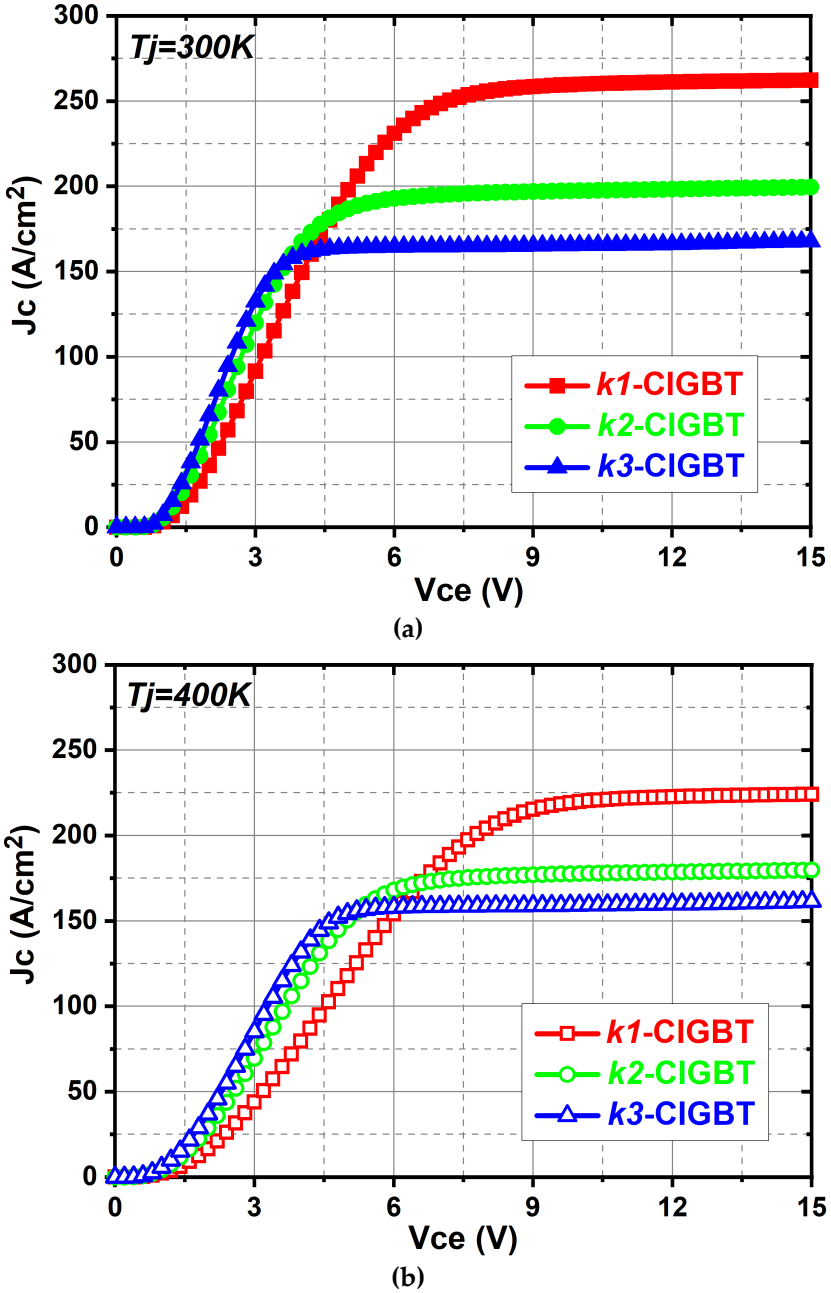


Figure 3.28 Current Saturation characteristics of the conventional and scaled devices at (a) T_j = 300 K and (b) T_j = 400 K.

3.3.6 Dynamic Characteristics

The switching characteristics are investigated with the mix-mode simulations and the circuit configuration is shown in Figure 3.29. The $V_{ce(sat)}$ versus E_{off} trade-offs of the scaled CIGBTs with state-of-the-art commercial 4.5 kV IGBTs [69, 70] are depicted in Figure 3.30. For identical E_{off}, the *k3*-CIGBT can achieve 20 % and 25 % reductions in on-state voltage drop compared to that of the conventional *k1*-CIGBT device at T_j =300 K and T_j = 400 K, respectively. Moreover, the scaled CIGBTs show significant improvement of $V_{ce(sat)}$-E_{off} trade-offs even compared to the commercial IGBTs in trench and field-stop technologies. Therefore, the scaling work of the 4.5 kV CIGBT provides a more energy-efficient solution for the power electronics applications.

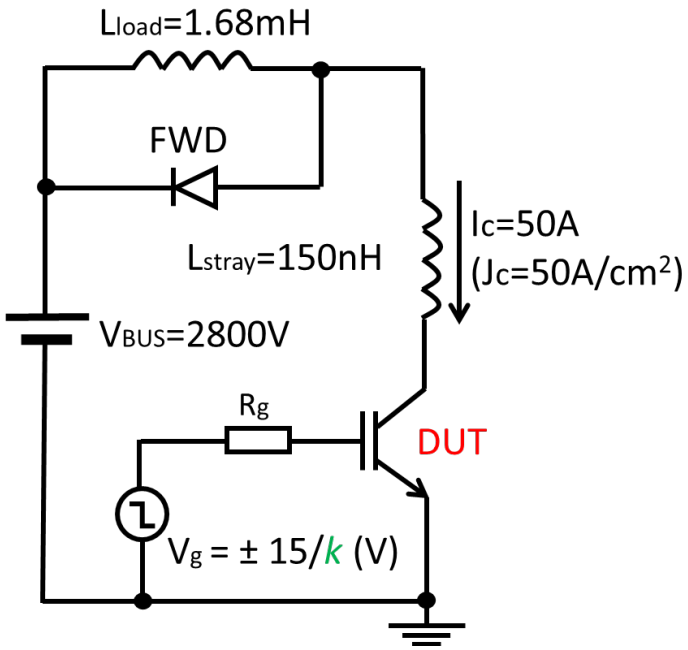


Figure 3.29 Inductive switching test circuit.

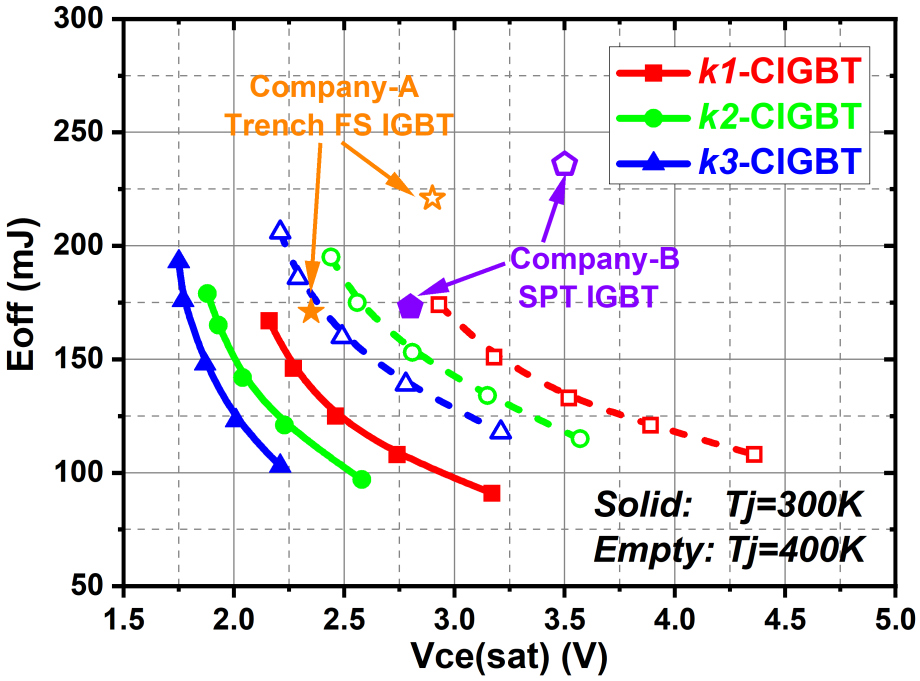


Figure 3.30 $V_{ce(sat)}$-E_{off} **trade-offs of the CIGBT devices and commercial IGBTs.**

In addition, the Reverse Bias Safe Operating Area (RBSOA) characteristics are shown in Figure 3.31. The devices are turned off at T_j = 400 K and a current level of 150 A (~3 times of rated current). As shown, the scaled devices turn-off successfully without occurrence of Switching Self-Clamping Mode (SSCM). In the conventional high-voltage field-stop IGBTs, dynamic avalanche can be triggered during high currents turn-off [71]. The collector voltage is clamped after it raises to the peak value. This is due to the occurrence of dynamic avalanche at emitter side. The device will enter into SSCM after dynamic avalanche occurs, which is considered as a dangerous operation [72]. Increasing P-anode injection efficiency can compensate the excessive electrons caused by dynamic avalanche and suppress the turn-on of SSCM. However, this will increase the E_{off} and affect the short-circuit capability due to higher J_{sat} as a result of greater current gain of the internal PNP transistor. In contrast, CIGBTs can suppress the dynamic avalanche phenomenon during turn-off. This is because the increasing collector voltage is supported by the P-well/N-drift junction so that the MOS cells are isolated to the high electric field. The high ruggedness of the scaled CIGBTs enables

the possibility to operate the devices under lower R_g, resulting in shorter switch-off delay time and lower E_{off}.

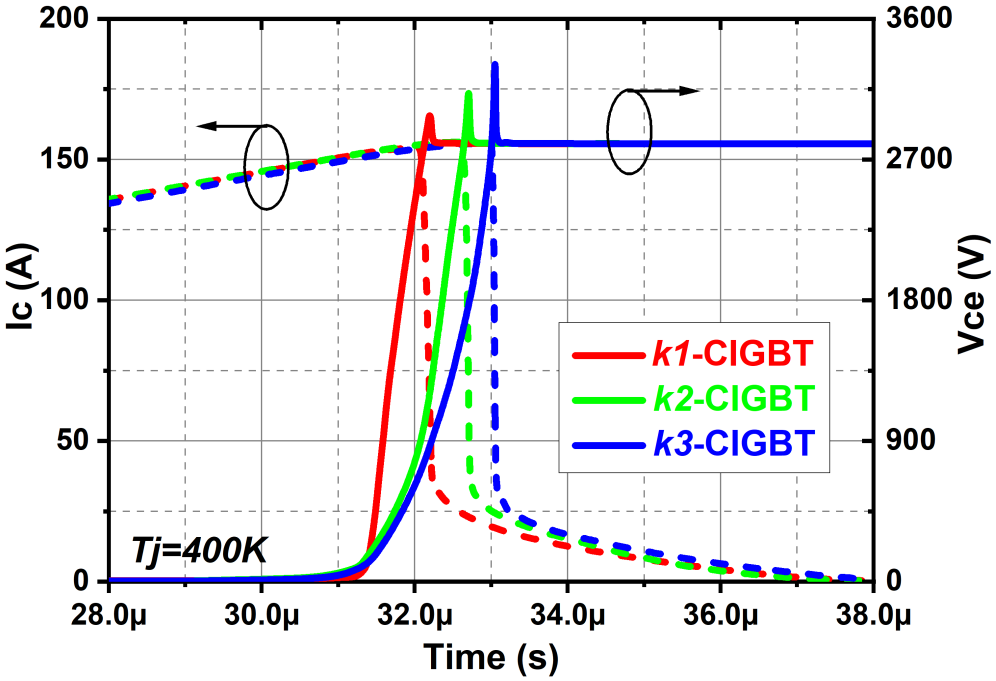


Figure 3.31 RBSOA characteristics of the conventional and scaled devices.

3.3.7 Short-circuit Characteristics

Figure 3.32 shows the comparison of the short-circuit performance under high temperature. The DC bus voltage is raised to 3600 V and self-heating effect is considered in the simulations. During short circuit condition, the device has to support simultaneously high supply voltage and its saturation current for a defined period. As a result, the junction temperature increases dramatically with time due to excessive power dissipation. To improve the short-circuit withstand duration and reduce the power dissipation, one effective solution is reducing the saturation current level. As shown, the *k*3-CIGBT significantly improves the short-circuit withstand duration due to the reduced J_{sat}. Therefore, a wider Short-Circuit Safe Operating Area (SCSOA) is achieved by the proposed 3-D scaling rules without penalizing $V_{ce(sat)}$.

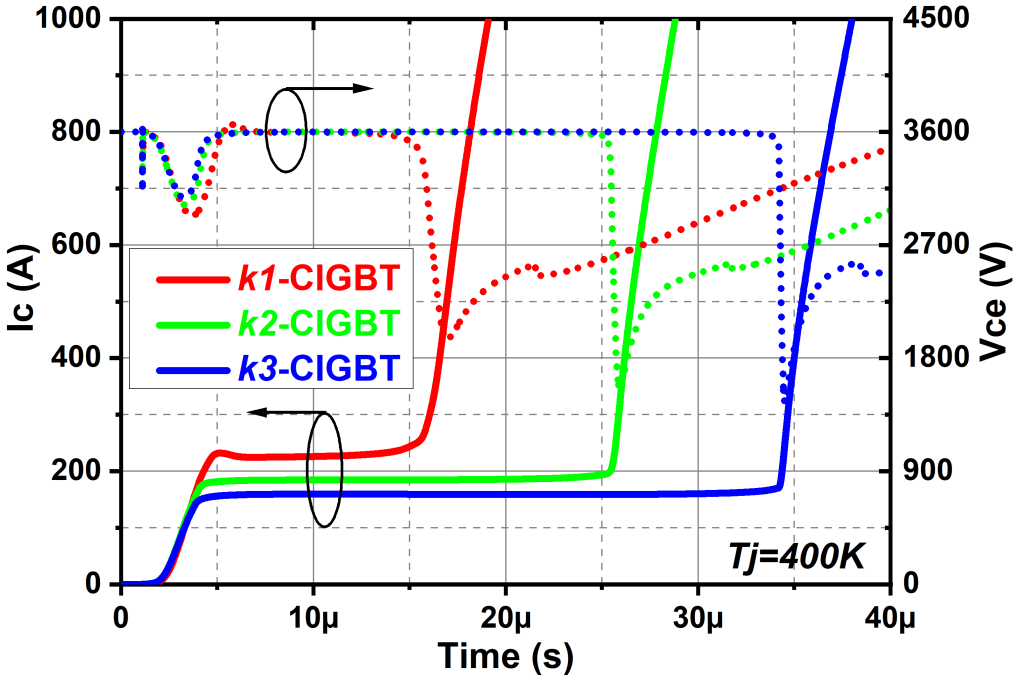


Figure 3.32 Short-circuit performance of the conventional and scaled devices.

3.4 Comparison of CIGBTs with State-of-the-art IGBT Technologies

Figure 3.33 compares the I-V characteristics of the 4.5 kV planar CIGBT and the 4.5 kV trench-gate CIGBT (TCIGBT). Compared to the trench IGBTs, planar IGBTs can provide higher switching frequencies due to lower E_{off} and also wider Forward Bias SOA (FBSOA) and SCSOA due to lower J_{sat}. However, in terms of on-state behavior, trench IGBTs are superior to planar IGBTs due to elimination of JFET resistance and IE effect. Therefore, the on-state voltage drops are expected to be further reduced by applying the 3D scaling rules to high voltage (> 3300 V) trench CIGBTs. Figure 3.33 summarizes the $V_{ce(sat)}$ of the conventional and scaled CIGBTs in both planar and trench technologies. The $V_{ce(sat)}$ for medium voltage (≤ 1700 V) CIGBTs are the voltage drops at J_c = 200 A/cm² whilst the $V_{ce(sat)}$ for high voltage (≥ 3300 V) CIGBTs are the voltage drops at J_c = 50 A/cm². The planar CIGBTs employ the scaling rules proposed in this work while the trench CIGBTs use the scaling rules proposed in Chapter 3.2. To support the rated breakdown voltage, the N-well and P-well depths of high voltage (> 3300 V) trench CIGBTs are kept constant. As shown in Figure 3.33, a 20 % reduction of $V_{ce(sat)}$ can be achieved by the scaling rules for both planar and trench CIGBTs. In

addition, the trench *k3*-CIGBTs display a 10 % improvement in forward voltage drop compared to the planar *k3*-CIGBTs.

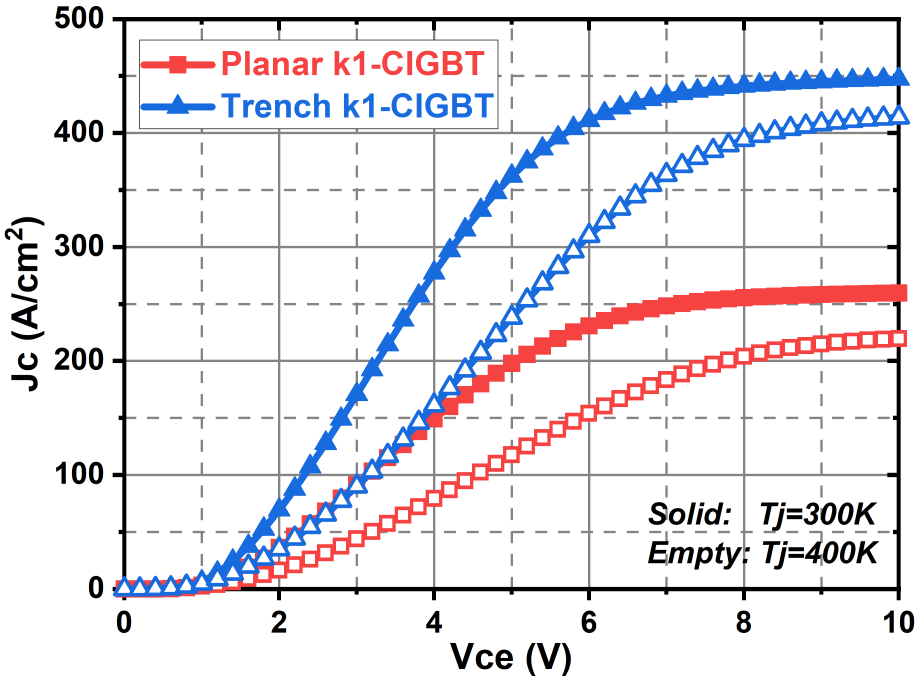


Figure 3.33 Comparison of I-V characteristics between 4.5 kV planar CIGBT and 4.5 kV trench CIGBT. (V_g = 15 V, τ = 50 μs)

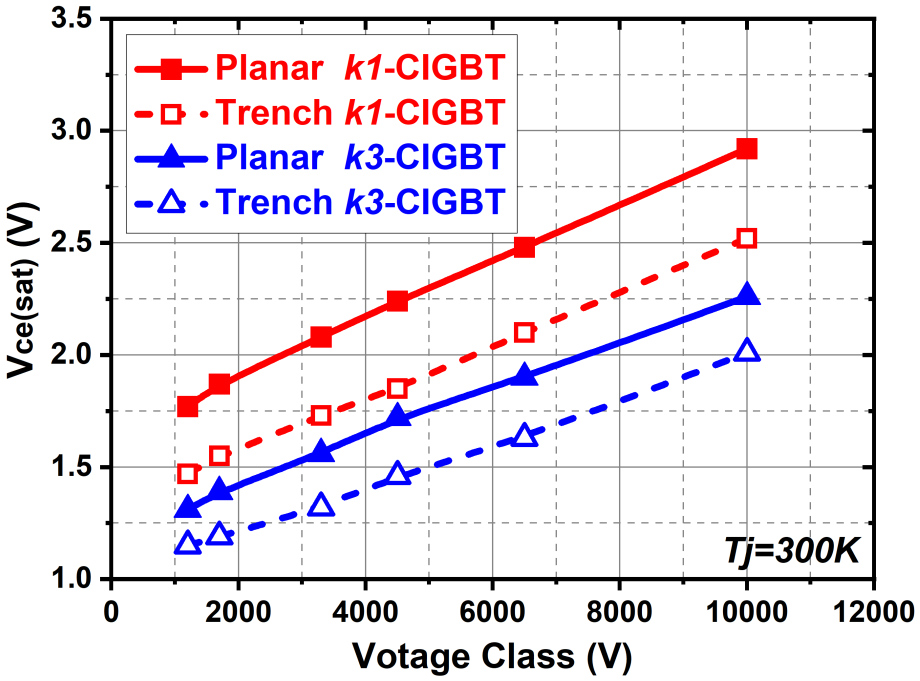


Figure 3.34 On-state voltage drops of the conventional and k3-CIGBTs in both planar and trench technologies.

The theoretical IGBT performance limit proposed in [73] assumes that the ideal on-state performance is when the γ_E is 1, which represents all the current is delivered by electrons whilst holes only contribute to the conductivity modulation within the N-drift region. Figure 3.35 compares the specific on-resistances ($R_{sp,on}$) of the *k*3-TCIGBTs with the state-of-the-art IGBT technologies [25, 27, 74-76], scaled trench IGBTs [28, 30] and the IGBT theoretical limit [73]. As shown, the *k*3-TCIGBTs exhibit significant improvement in $R_{sp,on}$ compared to the latest IGBT technologies. The $R_{sp,on}$ of the *k*3-TCIGBTs are close to the theoretical limit in the cases of medium voltages (< 3300 V) while the difference at high voltages (> 3300 V) is mainly due to recombination of carriers within thick N-drift layers. Furthermore, Figure 3.35 shows that the $R_{sp,on}$ of the *k*3-TCIGBTs can outperform the 1-D 4H-SiC unipolar limit when breakdown voltage is higher than 5 kV.

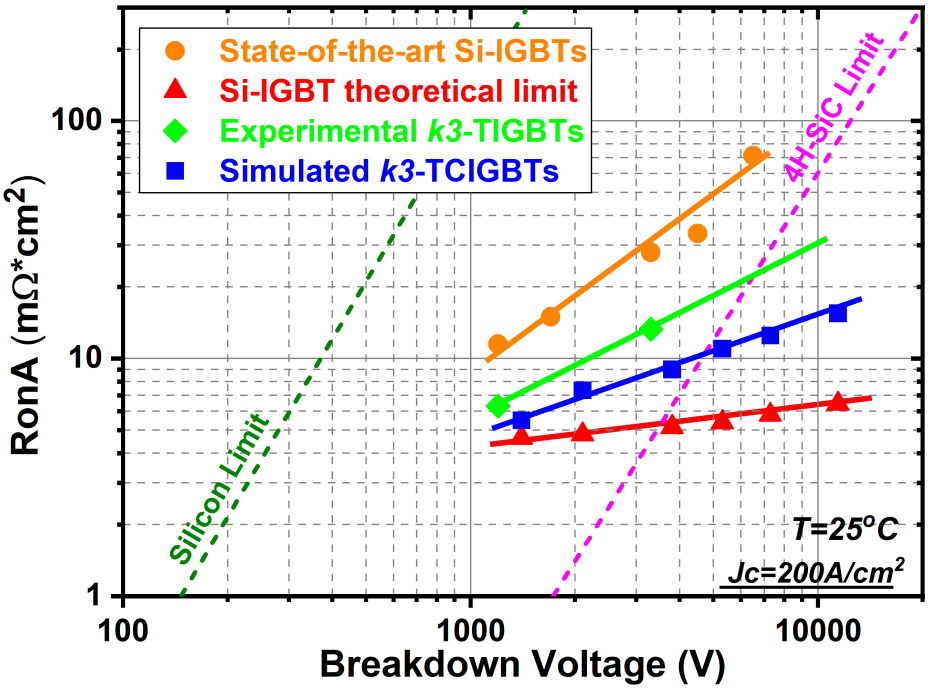


Figure 3.35 Comparison of k3-TCIGBTs with state-of-the-art IGBT technologies and IGBT performance limit.

3.5 Summary

In this chapter, the 3-D scaling rules for medium voltage trench CIGBT and high voltage planar CIGBTs are proposed and investigated through TCAD simulations. Detailed simulation results show that the scaling rules result in significant improvement in on-state behavior and $V_{ce(sat)}$-E_{off} trade-off. Moreover, the short-circuit withstand capability is maintained by enhancing the self-clamping voltage. More importantly, compared to the state-of-the-art IGBT technologies, the scaled TCIGBTs exhibit significant improvement of on-state performance. Therefore, the 3-D scaling rules provide an excellent approach of design optimization for improving the power efficiency of CIGBTs.

Chapter 4 A NOVEL APPROACH TO SUPPRESS THE NON-SATURATED IV BEHAVIOUR OF NARROW MESA IGBTS

As shown in previous chapter, the scaled trench IGBTs suffer from the non-saturated IV characteristics, which degrades the short-circuit robustness. In this chapter, a novel cathode design is suggested to restrain the Collector Induced Barrier Lowering (CIBL) effect of the very narrow mesa IGBTs without degrading on-state performance. 3-D TCAD tools in Synopsys Sentaurus Device are used to investigate the electrical characteristics of the proposed structure with calibrated models.

4.1 Introduction

Most recent developments on trench gated IGBTs are focussed upon scaling down mesa regions sandwiched between the gates to reduce on-state losses by enhancing the Injection Enhancement (IE) effect [24, 25, 28]. With the development of fabrication process, the mesa width (feature size) can be reduced to below 1 μm [24]. However, the IGBTs with very narrow mesa suffer from poor short circuit robustness due to non-saturated IV behaviour [31]. This is because of the Collector Induced Barrier Lowering (CIBL) effect [31], which occurs at the P-base/n^+-cathode junction. The detailed physics is similar to the turn-on mechanism of trench Inversion Layer Emitter Thyristor (ILET) [77]. During on-state of narrow mesa IGBTs, conductivity modulation tends to occur in the channel inversion layers [32], reducing the P-base/n^+-cathode junction barrier and resulting in a continuous increase in electron current. As a result, the collector current increases with the increasing electron current and does not show saturation behaviour. This phenomenon may destroy the device under short-circuit condition due to thermal runaway. Therefore, suppressing the CIBL effect is important for ensuring the Safe Operating Area (SOA) of the narrow mesa IGBTs.

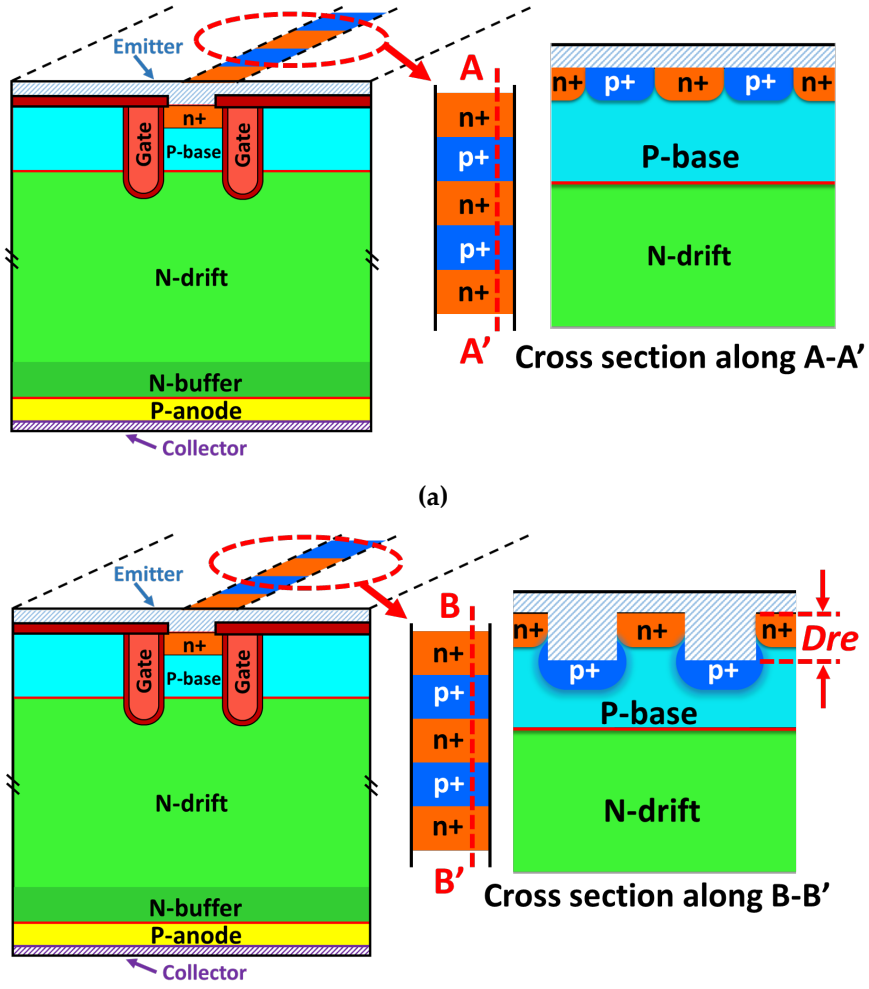


Figure 4.1 Schematic cross-sections of (a) the conventional narrow mesa IGBT and (b) the proposed RP-IGBT structure.

4.2 Device Structure

The single cell schematic cross-sections of the conventional narrow mesa IGBT and the proposed RP-IGBT structure are shown in Figure 4.1(a) and (b), respectively. It can be seen from the top view that both structures feature ladder design of the mesa regions and trench gates run across the active areas. Major structural parameters are kept identical for comparison and summarized in Table 4.1. The cell pitch is 10 μm and the mesa width is 400 nm. A carrier lifetime of 10 μs is set as default. Both conventional IGBT-A and IGBT-B are benchmarks while the P-base peak doping concentration of IGBT-B is significantly increased to lower its J_{sat} to ~1100 A/cm² at T_j = 300 K. In the RP-IGBT structure, after the implantation of n⁺-cathode, 0.5 μm of

silicon is etched prior to the implantation of the recessed p^+-cathode. The lateral diffusion of the recessed p^+-cathode moves into the P-base region below n^+-cathode regions, which helps to maintain the P-base/n^+-cathode junction barrier and suppresses the CIBL effect. More importantly, as the P-base region is not penetrated by the p^+-cathodes, there is no influence upon threshold voltage as well as on-state voltage.

Parameters (Unit:μm)	*Conv. IGBT-A*	*Conv. IGBT-B*	*RP-IGBT*
Cell Pitch	10	10	10
Mesa width	0.4	0.4	0.4
Gate oxide thickness	0.03	0.03	0.03
n^+ cathode length	1	1	1
p^+ cathode length	1	1	1
P-base depth	1.3	1.3	1.3
n^+ cathode depth	0.3	0.3	0.3
p^+ cathode depth	0.3	0.3	0.3
Trench depth	2.5	2.5	2.5
Recess depth (D_{re})	N.A.	N.A.	0.5
P-base peak doping (cm^{-3})	7×10^{17}	1.1×10^{18}	7×10^{17}

Table 4.1 Major structural parameters.

4.3 Static Characteristics

Figure 4.2 depicts the I-V characteristics of the conventional and proposed devices, while Figure 4.3 and Figure 4.4 compare the carrier distributions and on-state potential distributions within the mesa regions between conventional IGBT-A and RP-IGBT, respectively. It can be observed from Figure 4.2 that the conventional IGBT-A shows non-saturated tendency of I-V characteristics due to CIBL effect [31]. The CIBL mechanism can be explained as follows: during forward conduction, the whole mesa region becomes conductivity modulated, which is caused by the hole current flowing into the inversion layers and n^+-cathode, as shown in Figure 4.3(a). As a result, it can be seen from Figure 4.4(a) that the P-base/n^+-cathode junction barrier reduces

significantly with increased collector voltage resulting in non-saturation behaviour of the collector current, which will cause premature latch-up and degrade the short circuit capability.

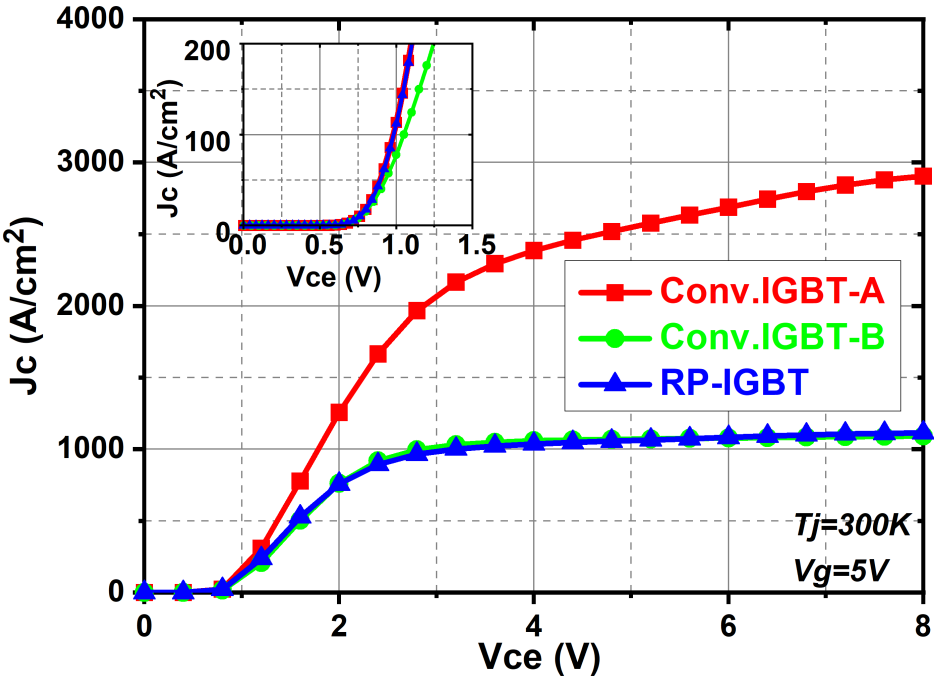
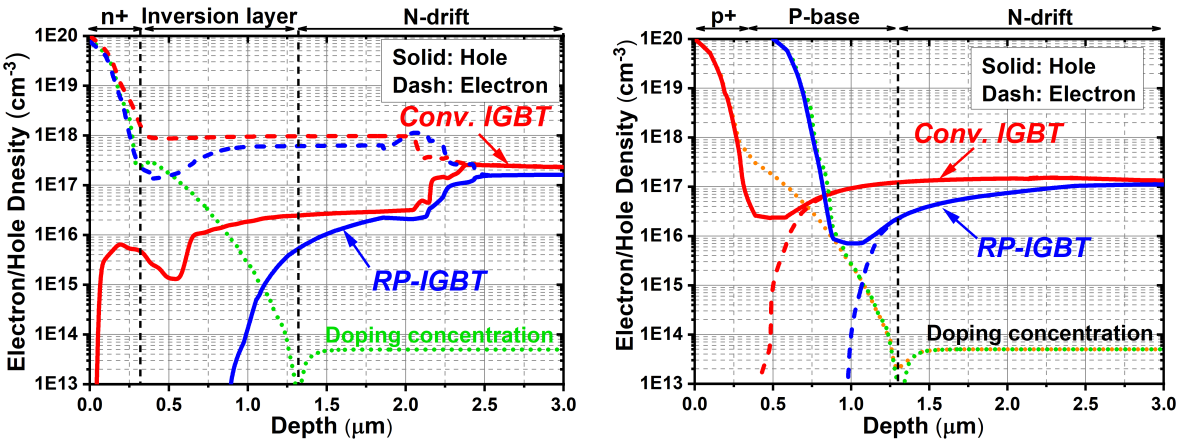
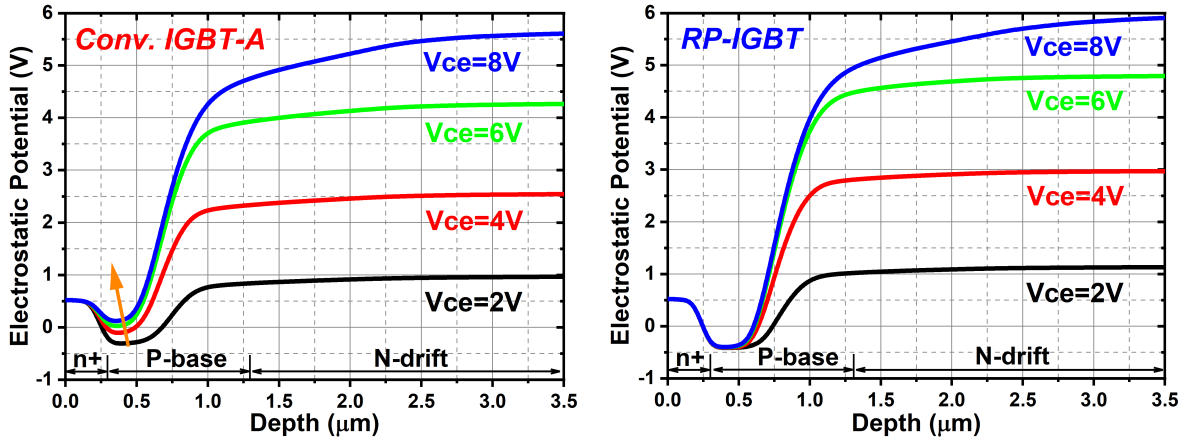


Figure 4.2 I-V characteristics of conventional IGBTs and RP-IGBT.



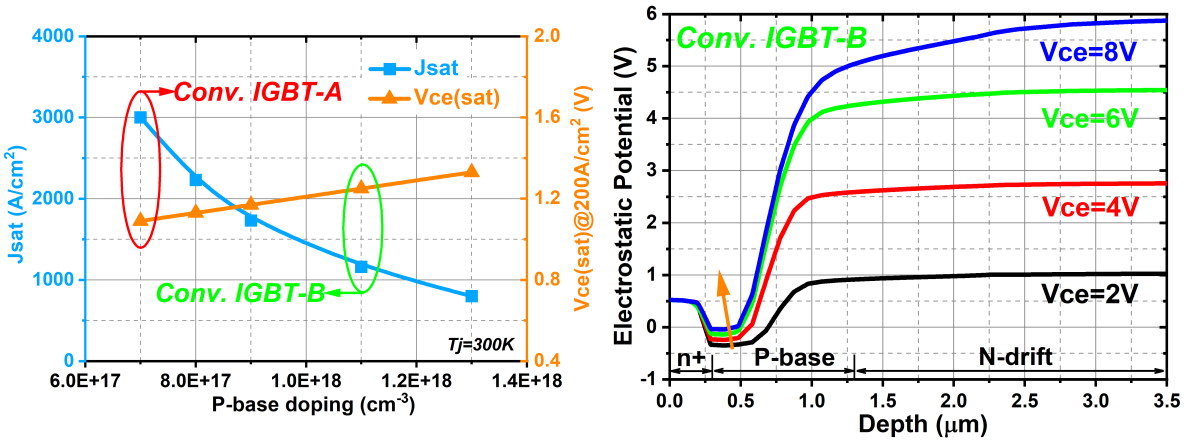
(a) (b)

Figure 4.3 Comparison of carrier distributions within mesa regions between conventional IGBT-A and RP-IGBT. (a) Across n⁺-cathode/inversion layer/ N-drift, (b) across p⁺-cathode/P-base/N-drift. (V_g = 5 V, J_c = 500 A/cm²)



(a) (b)

Figure 4.4 Comparison of potential distributions within the middle of mesa regions between (a) conventional IGBT-A and (b) RP-IGBT. (V_g = 5 V, T_j = 300 K)



(a) (b)

Figure 4.5 (a) Dependence of P-base doping concentration upon $V_{ce(sat)}$ and J_{sat} of the conventional narrow mesa IGBT. (b) Potential distributions within the mesa region of the conventional IGBT-B device. (V_g = 5 V, T_j = 300 K)

Increasing P-base doping concentration is a potential solution to lower J_{sat} at the expense of increase in the threshold voltage, which will influence the on-state performance, as illustrated in Figure 4.5(a). Moreover, it can be observed from Figure 4.5(b) that the CIBL effect continues to exist to cause conductivity modulation in the P-base region of the conventional IGBT-B device. In contrast, it should be noted from Figure 4.2 that the proposed RP-IGBT can reduce the J_{sat} to ~1100 A/cm² at T_j = 300 K without increase of P-base doping concentration. Significant reduction in J_{sat} can be

explained by the fact that the recessed p^+-cathode diverts the flow of holes into the p^+-cathode rather than the channel inversion layers. It is evident from Figure 4.3(a) that the hole density in the inversion layer of the RP-IGBT is significantly reduced compared to that of conventional IGBT. Therefore, the conductivity modulation is effectively suppressed in the P-base region, as shown in Figure 4.3(b). Furthermore, the lateral diffusion of the p^+-cathode increases the acceptor concentration beneath the P-base/n^+-cathode junction and contributes to maintain the P-base/n^+-cathode junction barrier during conduction. Due to the suppression of conductivity modulation in the mesa region, the P-base/n^+-cathode junction barrier does not decrease with increased collector voltage, as illustrated in Figure 4.4(b). Consequently, the current saturation characteristics are significantly improved compared to that of the conventional narrow mesa IGBT. Moreover, note that RP-IGBT structure can suppress the conductivity modulation in the channels and enable current saturation behaviour even though the mesa width is reduced to 20 nm, as shown in Figure 4.6 and Figure 4.7.

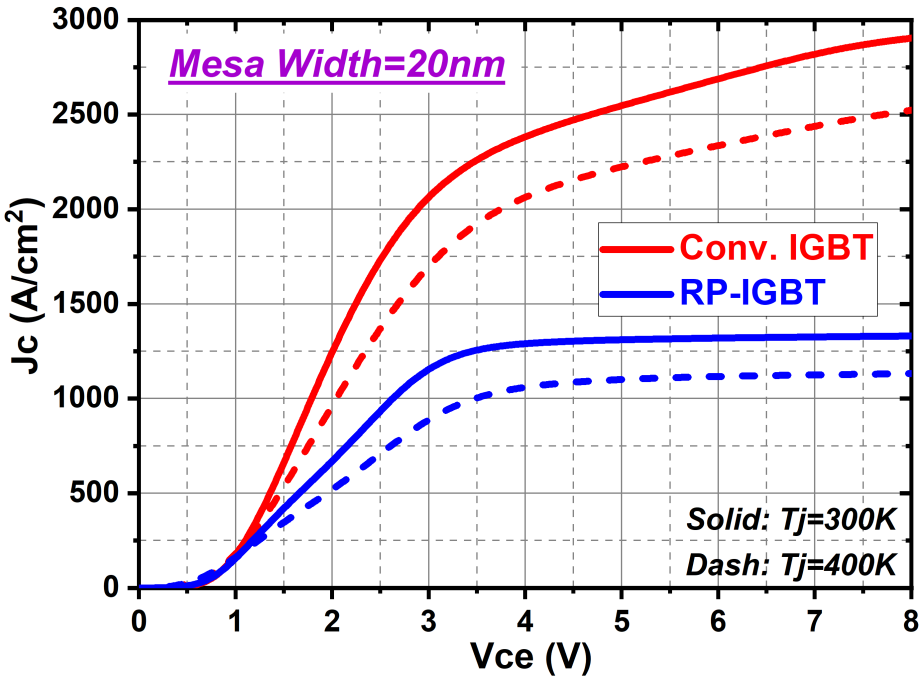


Figure 4.6 Comparison of I-V characteristics for the case of 20 nm mesa structures. (V_g= 1.2 V)

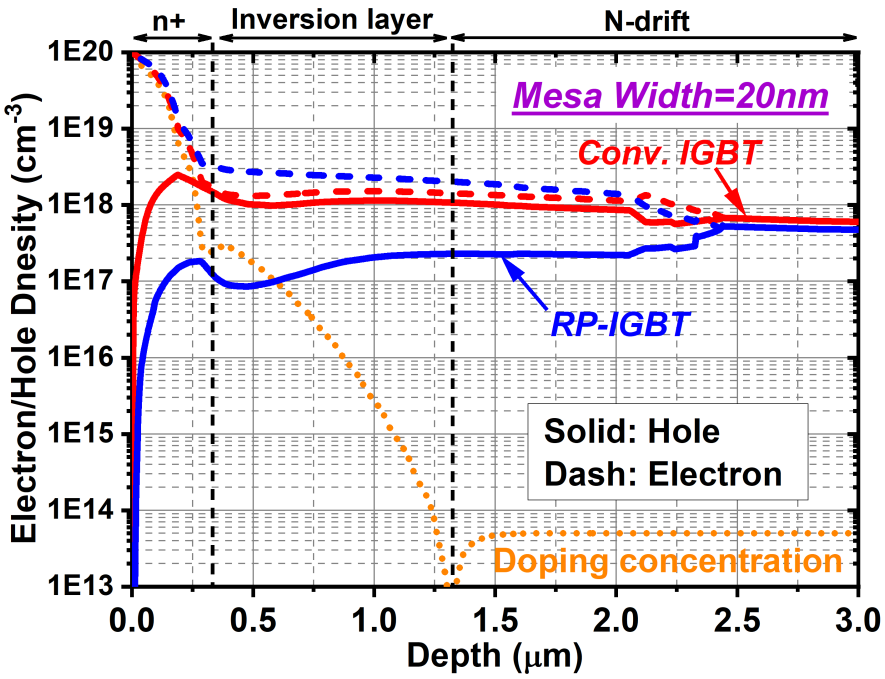


Figure 4.7 Comparison of carrier distributions within mesa regions for the case of 20 nm mesa structures. (V_g = 1.2 V)

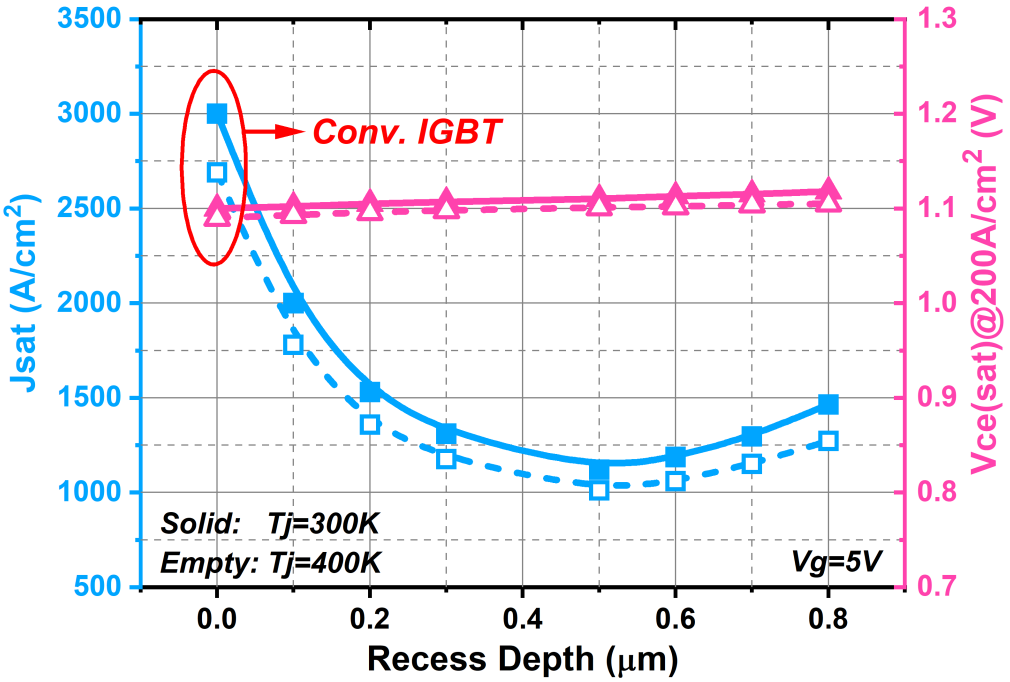


Figure 4.8 Influence of recess depth upon $V_{ce(sat)}$ and J_{sat}. (V_g = 5 V)

Figure 4.8 shows the influence of the recess depth of the p⁺-cathode upon the $V_{ce(sat)}$ and J_{sat} of RP-IGBT. As shown, the recess depth does not affect the on-state performance. This is because the lateral diffusion of the p⁺-cathode does not affect the threshold

voltage as well as the channel resistance of the RP-IGBT. However, its saturation current density shows significant reduction as the recessed depth increases and tends to increase when the recessed depth exceeds 0.5 μm. This is because the lateral diffusion of the p^+-cathode has less influence on the P-base/n^+-cathode junction barrier when the recessed depth is deeper and away from this junction.

4.4 Short-circuit Characteristics

The short-circuit withstand capability of the proposed RP-IGBT is shown in Figure 4.9. The DC bias is 800 V, the rated current is 100 A at a current density of 200 A/cm^2. In addition, self-heating effect is considered herein, and the initial junction temperature is set as 400 K. Unlike the conventional IGBT-A device which fails immediately after the device turns-on, the RP-IGBT device clearly shows more than 10 μs short-circuit withstand capability, which is also superior to that of the conventional IGBT-B device. This short-circuit robustness is contributed by the recessed p^+-cathode which suppresses the CIBL effect and maintains the saturation current level.

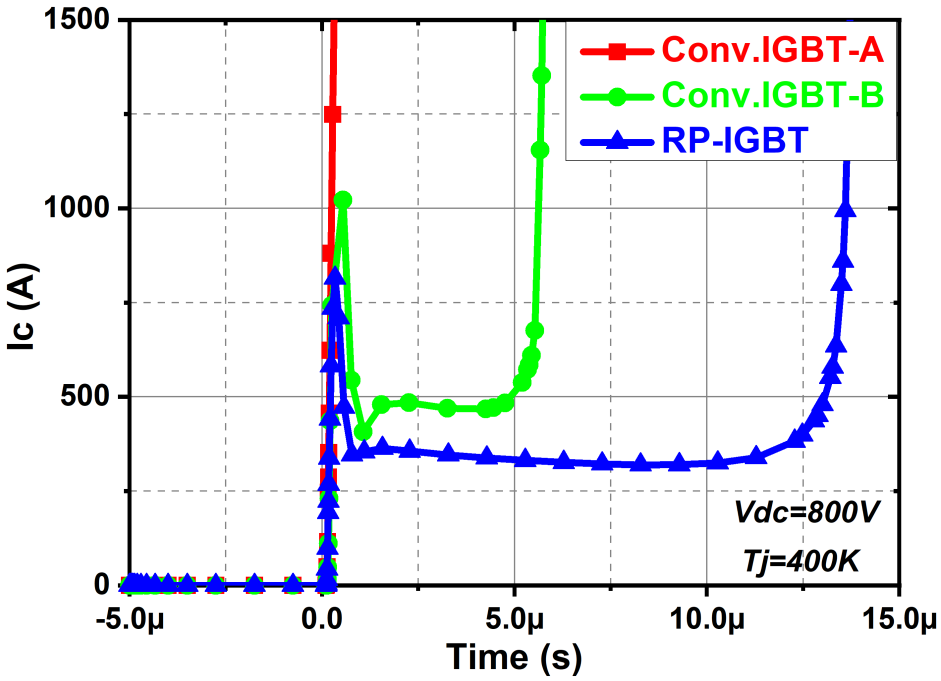


Figure 4.9 Comparison of short-circuit characteristics between the conventional devices and the RP-IGBT device. (V_g = 5 V, R_g = 22 Ω)

4.5 Sensitivity Analysis

From a fabrication point of view, a robust process compatibility is essential to meet the commercially available technologies. The sensitivity of the recessed trench depth is shown in Figure 4.8, while Figure 4.10 shows the sensitivity analysis of the recessed p⁺-cathode. As shown, even with a tolerance of plus or minus 20 %, there is no significant influence upon electrical characteristics. Therefore, RP-IGBT structure is fully compatible with narrow mesa IGBT processing technologies.

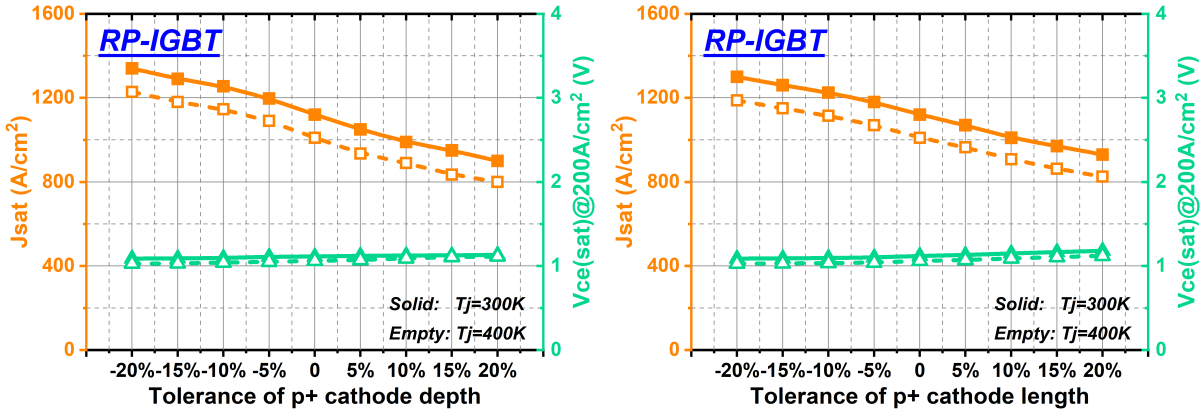


Figure 4.10 Influence of the tolerance of (a) p⁺-cathode depth and (b) p⁺-cathode length upon $V_{ce(sat)}$ and J_{sat}. (V_g = 5 V)

4.6 Summary

A method to suppress the CIBL effect in a narrow mesa IGBT is proposed and analysed through 3-D simulations. Compared with the conventional narrow mesa IGBT, the 3-D simulation results show that the recessed p⁺-cathode in an IGBT can significantly reduce the saturation current level while maintaining the on-state performance. Due to the suppression of CIBL effect, the short-circuit capability is enabled. Therefore, the RP-IGBT structure can provide a much wider short circuit safe operating area (SCSOA) than the conventional narrow mesa IGBTs.

Chapter 5 CHARACTERISATION OF A SILICON MOS-GATED THYRISTOR AND SILICON CARBIDE MOSFET HYBRID SWITCH

In this chapter, a 1.2 kV 40 A hybrid power switch combining the excellent bipolar current conduction capability of a MOS-gated thyristor device with the superior switching characteristics of a SiC Power MOSFET is experimentally investigated. In order to demonstrate the benefits of this hybrid arrangement, full silicon Clustered IGBTs as well as full silicon carbide MOSFETs are also evaluated as benchmark samples. Experimental results indicate that the proposed structure could achieve potential improvements in terms of low conduction and switching losses.

5.1 Introduction

Silicon-based MOS-gated bipolar devices are widely used in power electronics applications with rated voltages of 600 V – 6.5 kV due to combination of easy gate control and high current handling capability. However, the switching frequency is limited by the carrier storage effects via conductivity modulation. In contrast, owing to the inherent advantages of Wide Band-Gap (WBG) semiconductor materials such as Silicon Carbide (SiC) and Gallium Nitride (GaN), WBG-based power semiconductor devices such SiC MOSFET and GaN HEMT have demonstrated superior electrical performances over silicon-based power devices, especially in terms of the high switching frequency. Whereas the extremely high cost of substrate material and fabrication processes is still a major challenge for widespread adoption of WBG-based power devices. Therefore, the combination of silicon devices and WBG devices becomes to be a cost-effective solution. The hybrid arrangements aim to provide an optimum choice in terms of power efficiency and device costs for power converters. Recently, a hybrid switch configuration of a silicon IGBT and a SiC MOSFET has been demonstrated at rated voltages of 1.2 kV, 3.3 kV and 6.5 kV [78-80]. Since the trench Clustered IGBT (CIGBT) has demonstrated superior on-state performance over

conventional IGBT due to thyristor conduction [56], the combination of silicon CIGBT and SiC MOSFET is expected to further enhance the energy efficiency.

5.2 Hybrid Switch Configuration

The hybrid switch is a hybrid connection of several CIGBT dies in parallel to SiC MOSFET dies, as shown in Table 5.1. In order to demonstrate its performances under different operating conditions, the parallel configuration is assembled on a single substrate. The bonding diagram of the hybrid switch upon an aluminium substrate is shown in Table 5.1. The wires used for wire bonding are aluminium wires with a diameter of 200 μm. The gates of these dies are connected to a common terminal making the hybrid switch a three terminals device. The bare dies used in the hybrid and benchmark samples are 1200 V / 8 A Trench CIGBT [56] and 1200 V / 20 A SiC MOSFET [81]. For the purpose of comparison, the rated current is defined as 40 A, which is approximately the sum of the individual die rated current. The specific allocation of these chips in hybrid switch and reference samples are shown in Table 5.1. The full CIGBT device has five CIGBT dies in parallel on a single substrate. Similarity, the full MOSFET has two SiC MOSFET dies in parallel on a single substrate to obtain a current rating of approximately 40 A.

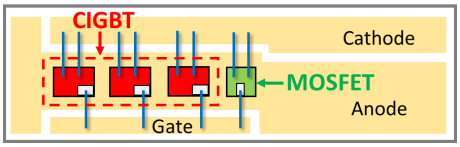
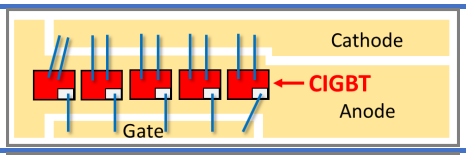
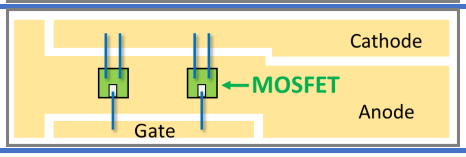
Device	Device Configuration	Device Area
Hybrid Switch		71.64 mm²
Full CIGBT		91.65 mm²
Full MOSFET		33.3 mm²

Table 5.1 Device configurations of hybrid switch and benchmarks.

5.3 Experimental Results and Analysis

5.3.1 Breakdown Characteristics

The static electrical characterisations of the hybrid switch and benchmark samples are carried out using Tektronix 371B High Power Curve Tracer. Figure 5.1 shows the measured results of the breakdown characteristics of the hybrid switch at room temperature and 150 °C. As shown, a breakdown voltage of more than 1400 V can be achieved by the proposed hybrid switch even at T_j = 150 °C, although the leakage current shows some increase compared with level at room temperature.

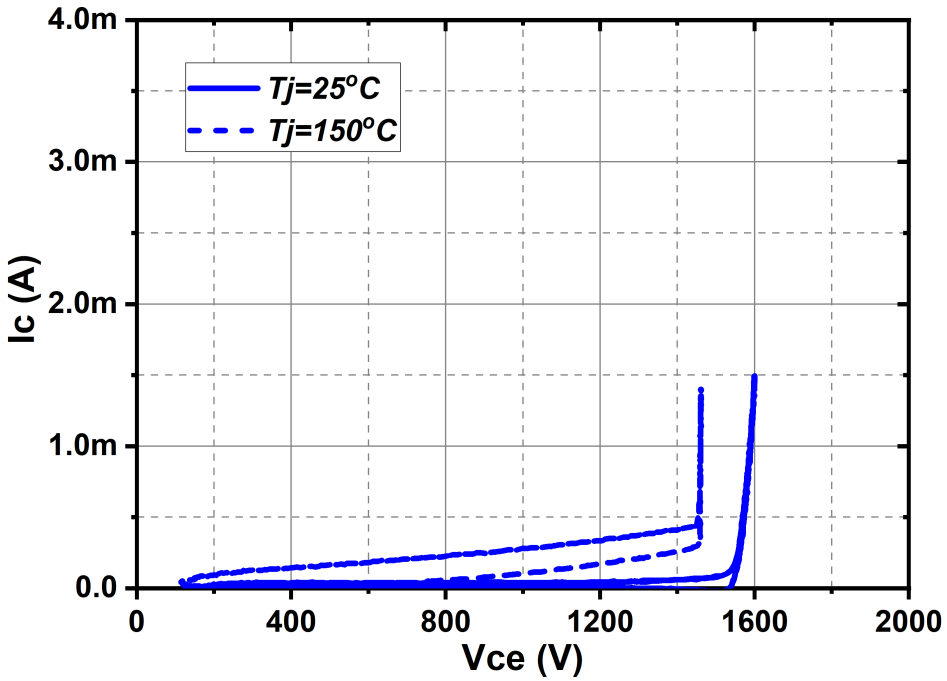


Figure 5.1 Breakdown characteristics of the hybrid switch.

5.3.2 Input Characteristics

Figure 5.2 shows the input characteristics of the hybrid switch and benchmark samples at both room temperature and 150 °C. As expected, the input current-voltage curves of the hybrid switch lie in between the full MOSFET and the full CIGBT samples. Its threshold voltage is approximately 4.8 V at 25 °C which reduces to 3.3 V at 150 °C. Hence, the gate drivers for CIGBTs or MOSFETs are also suitable for this hybrid switch.

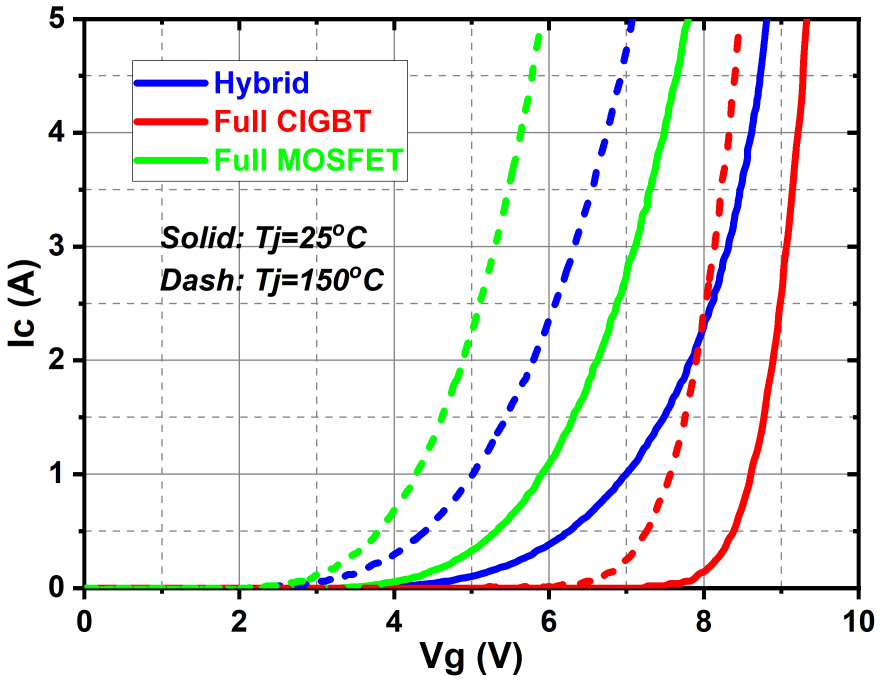


Figure 5.2 Input characteristics of the hybrid switch and benchmarks.

5.3.3 I-V Characteristics

The measured I-V characteristics of the hybrid switch and benchmark samples are shown in Figure 5.3. For the hybrid switch, all the gates are connected and controlled by a same gate voltage signal, 15 V in this case. For the full SiC sample the gate voltage is increased to 20 V, as per the device datasheet [81]. As shown, compared to the CIGBT sample, the hybrid switch shows low conduction losses when collector current is lower than rated current. The $V_{ce(sat)}$ of the hybrid switch is as low as that of full CIGBT at both 25 °C and 150 °C. Furthermore, compared to the full SiC MOSFET, the hybrid sample shows a significantly lower forward voltage drop when collector current exceeds rated current. Therefore, the proposed hybrid switch exhibits MOSFET characteristics at low current levels while still performing the superior current carrying capability of CIGBT at high current levels.

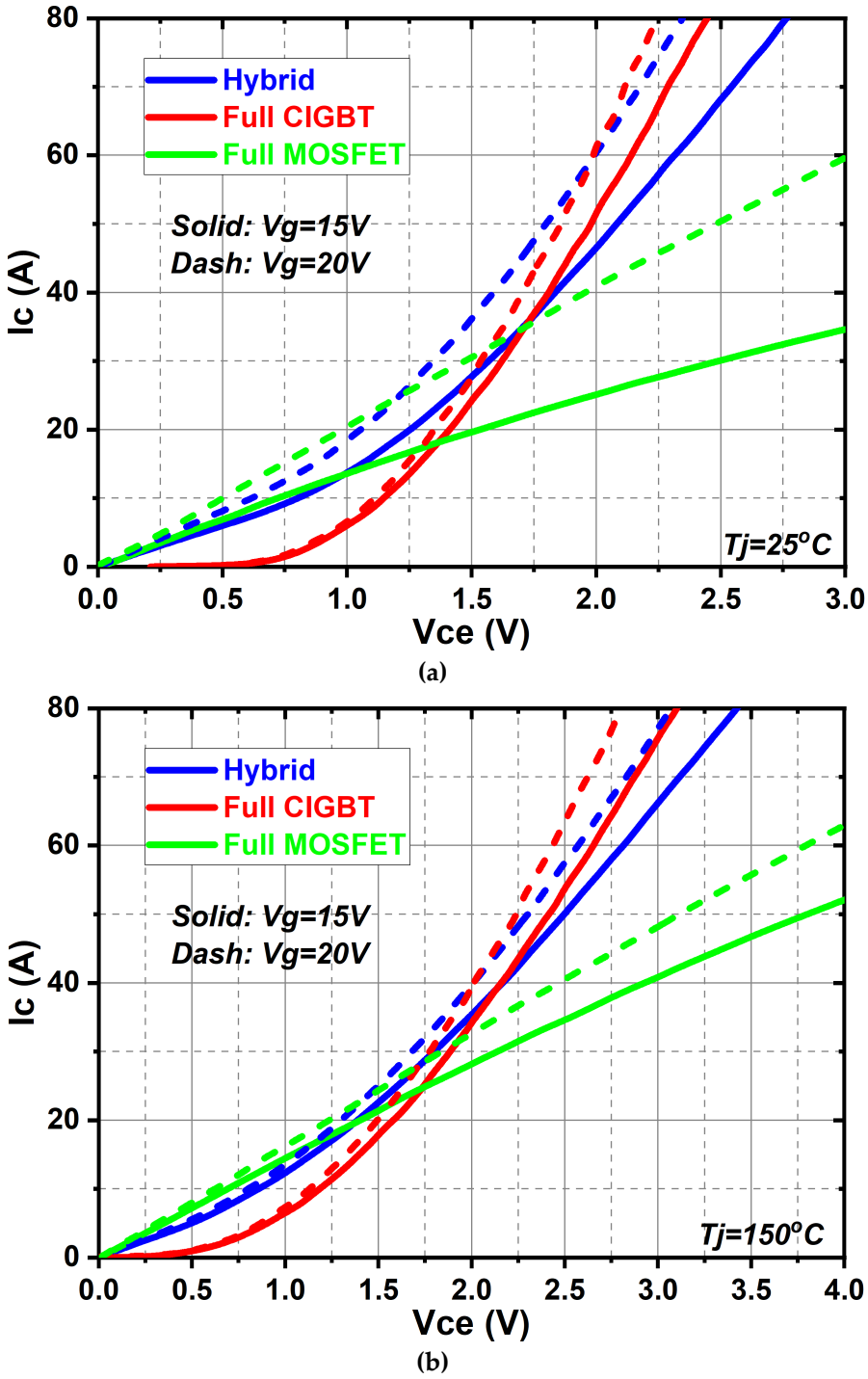


Figure 5.3 Comparison of I-V characteristics at (a) T_j = 25 °C and (b) T_j = 150 °C.

The $V_{ce(sat)}$ as a function of junction temperature at V_g = 15 V and V_g = 20 V are shown in Figure 5.4. The hybrid switch shows positive temperature coefficients at both V_g = 15 V and V_g = 20 V. Therefore, the demonstrated hybrid switch can be easily paralleled to scale up the output current. However, the SiC MOSFET shows negative temperature coefficient at V_g = 15 V. This is because the channel resistance is dominant

in the total on-state resistance when V_g = 15 V. The on-resistance of a power MOSFET mainly consists of channel resistance which has a negative temperature coefficient and body resistance which has positive temperature coefficient. If the channel resistance is not low enough, it will dominate the on-resistance and result in a negative temperature coefficient of the on-resistance. Therefore, the gate voltage for power MOSFETs is usually higher than that of IGBTs to lower the channel resistance.

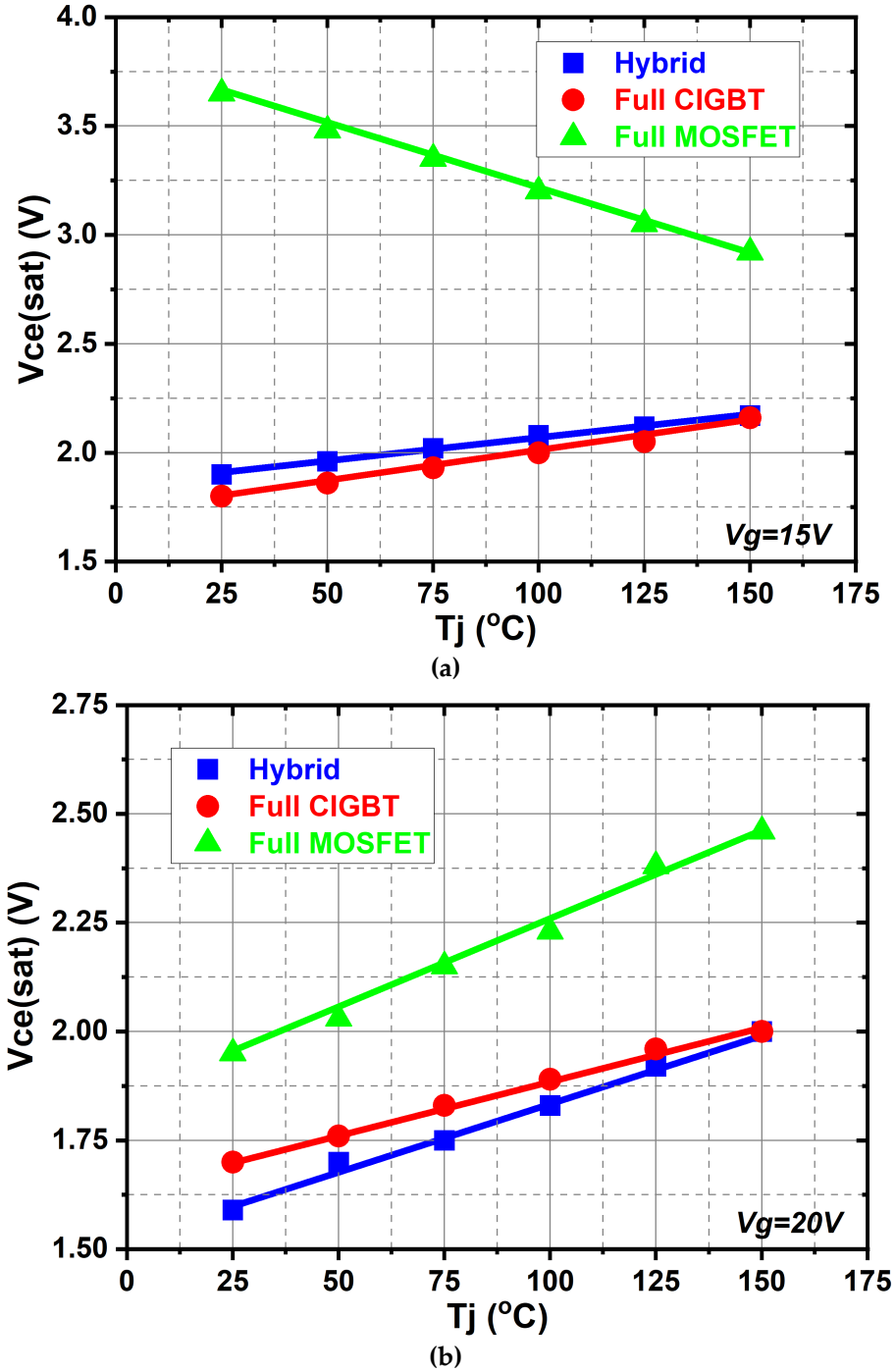


Figure 5.4 Dependence of $V_{ce(sat)}$ on junction temperature at (a) V_g = 15 V and (b) V_g = 20 V.

5.3.4 Switching Characteristics

The switching performances of the hybrid switch and the benchmark samples are investigated with the traditional double gate pulse clamped inductive load as shown in Figure 5.5. Figure 5.6 shows the turn-off waveforms of the hybrid switch and the benchmark devices. All these devices have been tested at 25 °C and 150 °C under rated current and half rated voltage. As shown, at both room and high temperatures, the switching current of the full SiC MOSFET falls significantly earlier compared to the hybrid switch and full CIGBT samples while displaying the greatest voltage overshoot. This is a direct result of the unipolar current flow mechanism of the structure. The switching current of the hybrid switch drops earlier compared to that of the full CIGBT sample and whilst still maintaining a soft current tail due to the recombination of excess carriers within the drift region of the CIGBT structure.

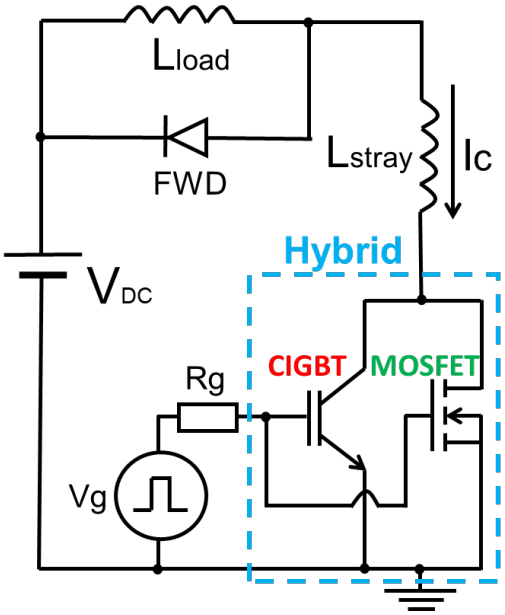


Figure 5.5 Inductive switching test circuit. (V_{DC} = 600 V, I_C = 40 A, V_g = +/- 15 V, L_{load} = 385 µH)

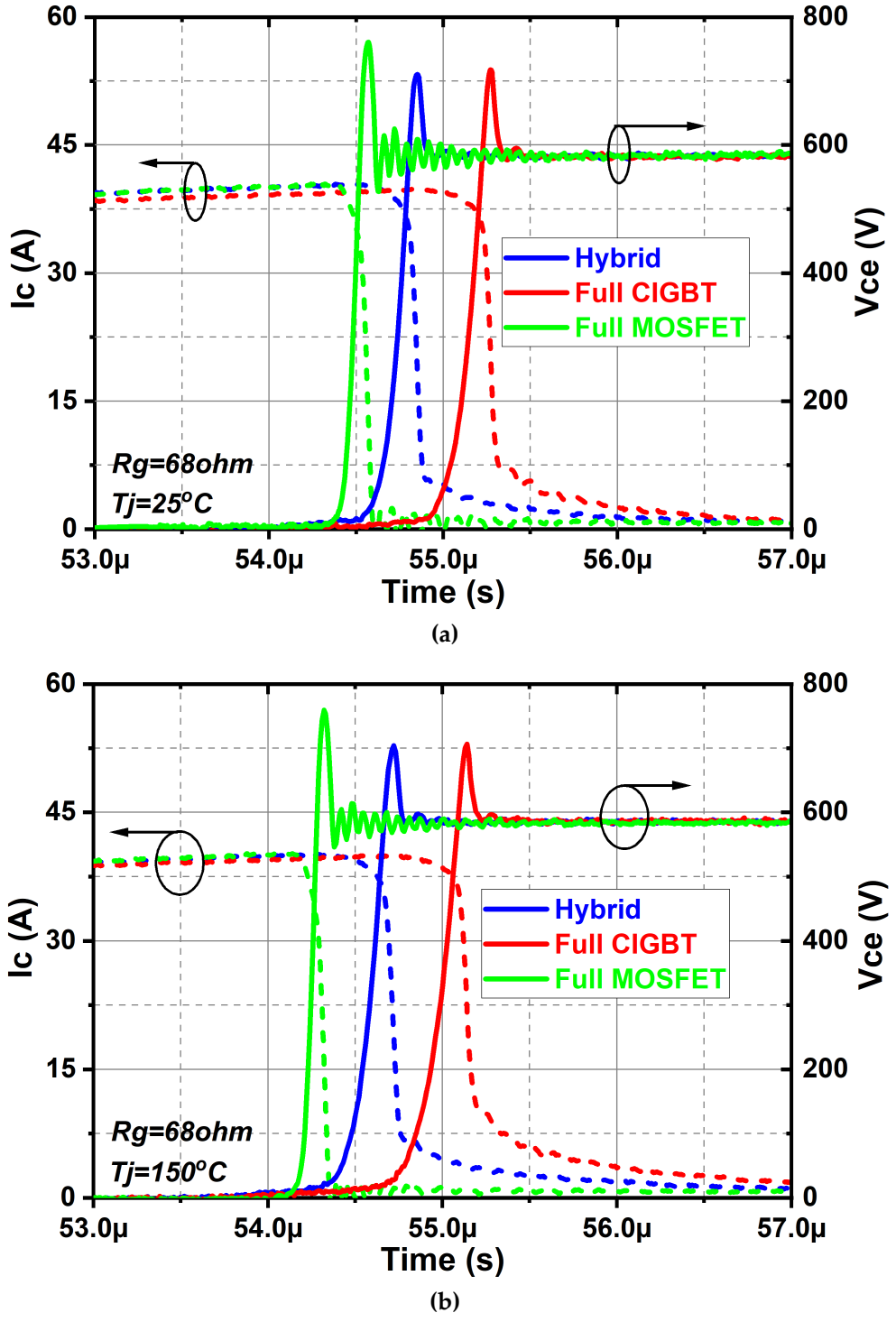


Figure 5.6 Comparison of turn-off characteristics at (a) T_j = 25 °C and (b) T_j = 150 °C.

Figure 5.7 shows the comparison of turn-off energy loss (E_{off}) as a function of gate resistance (R_g) at 25 °C and 150 °C. As shown, all the tested devices show linear decreases with reducing R_g. Compared to the full CIGBT device, the hybrid device shows approximately 30 % and 45 % reduction in E_{off} at 25 °C and 150 °C respectively.

The full MOSFET shows the lowest E_{off} due to unipolar conduction. However, the surge voltage (V_{surge}) is much higher than that of hybrid switch and full CIGBT device, especially when R_g is small due to the high turn off current slope, as shown in Figure 5.8. Moreover, it should be noted that the most extensive applications of 1200 V-class power switches are the variable speed motor drives, which require limitation of switching speed due to inherent limitation of motor insulation system [47]. To meet the requirement of motor-insulation stress, the switching slopes (dV/dt) are usually restricted to the range of 2 to 10 kV/μs [47]. As shown in Figure 5.9, the SiC MOSFET device exhibits the highest turn-off dV/dt compared with hybrid switch and full CIGBT device. Increasing R_g is a direct solution to reduce the dV/dt. However, this method will significantly scarify the E_{off}. As shown in Figure 5.7, the E_{off} of SiC MOSFET is increased by 3 times when R_g increases from 4.7 Ω to 68 Ω. In contrast, the hybrid switch shows much lower dV/dt and the E_{off} is less sensitive to the variation in R_g.

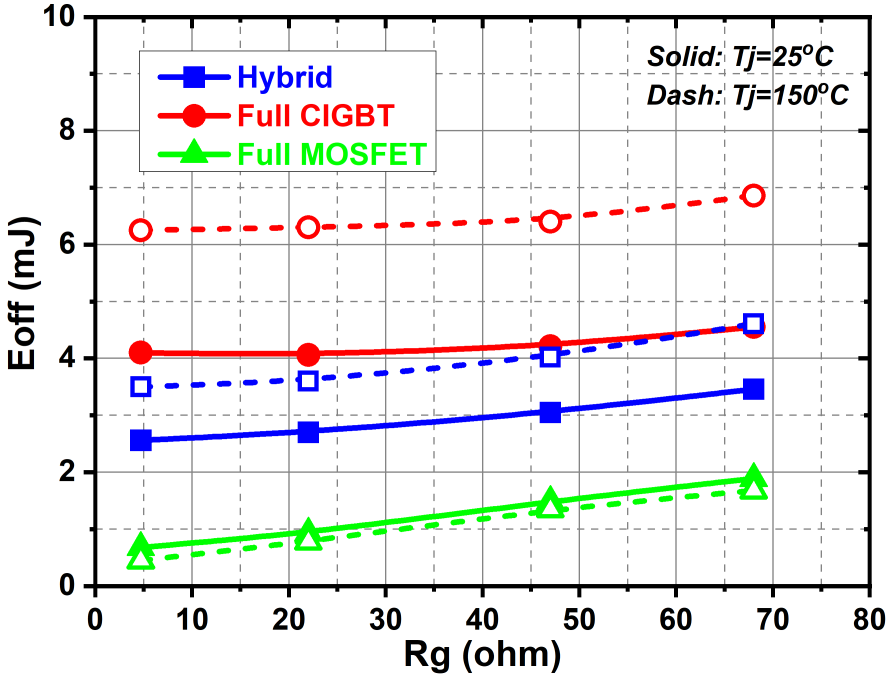


Figure 5.7 Dependence of E_{off} on R_g at T_j = 25 °C and T_j = 150 °C.

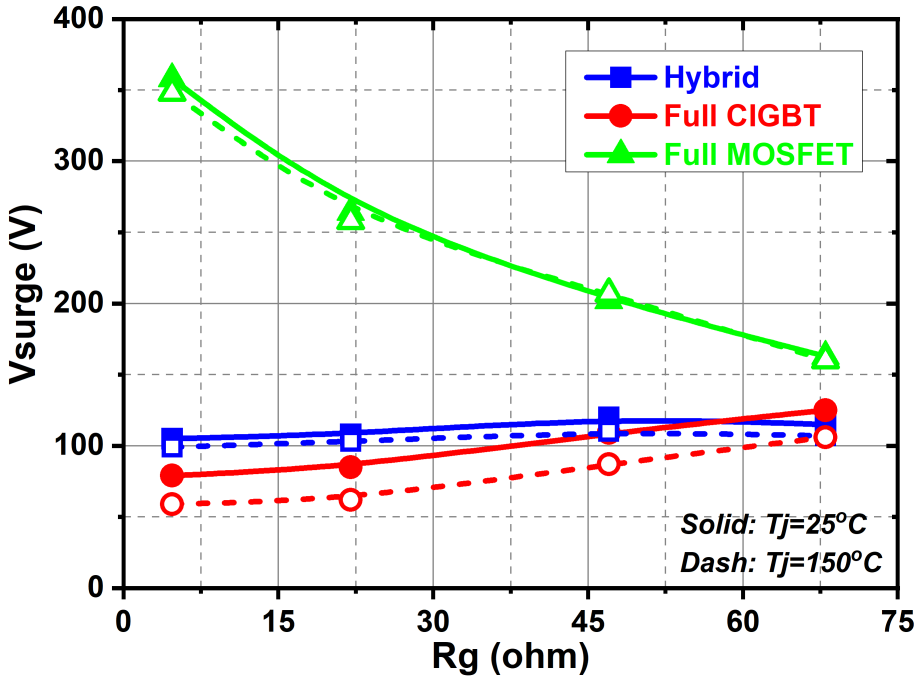


Figure 5.8 Dependence of V_{surge} on R_g at T_j = 25 °C and T_j = 150 °C.

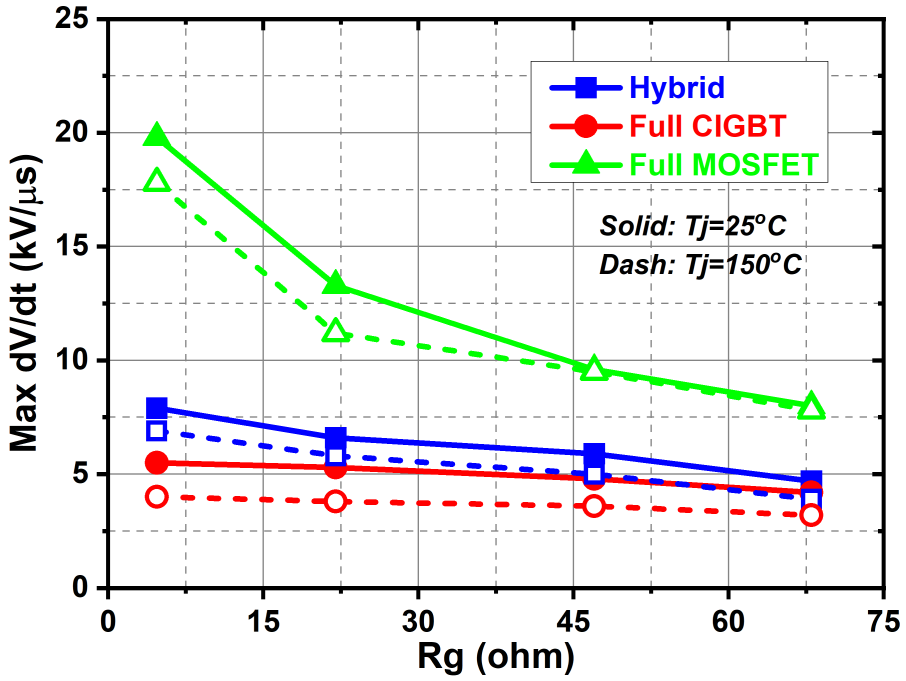


Figure 5.9 Dependence of maximum dV/dt on R_g at T_j = 25 °C and T_j = 150 °C.

Figure 5.10 compares the trade-off between E_{off} and $V_{ce(sat)}$ of all devices considered. As shown, compared to the full CIGBT device, the hybrid switch exhibits a 35 % reduction in E_{off} compared to a 1 % increase in $V_{ce(sat)}$ at 25 °C. Moreover, the turn off losses can

be reduced by 45 % without any increase in $V_{ce(sat)}$ when the junction temperature is increased to 150 °C. Therefore, the hybrid switch can provide a much higher energy efficiency in comparison to the full CIGBT device.

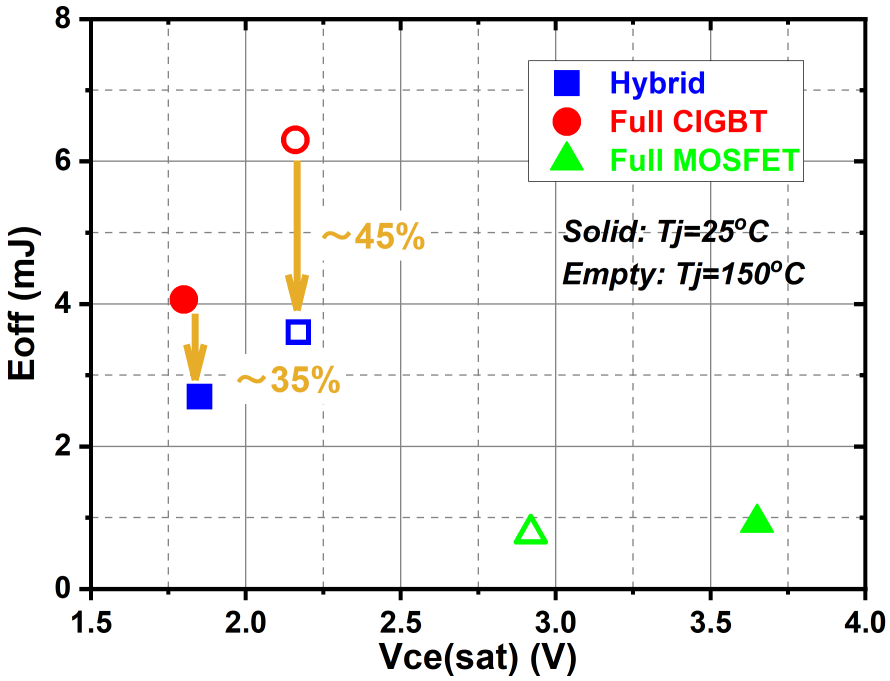


Figure 5.10 Comparison of E_{off} – $V_{ce(sat)}$ trade-off at T_j = 25 °C and T_j = 150 °C. (V_g = 15 V)

5.3.5 Short-Circuit Characteristics

The short circuit capability of the hybrid switch is evaluated at a bus voltage of 600 V and a gate voltage of 15 V at T_j = 150 °C. Figure 5.11 shows the short-circuit waveforms of the hybrid switch. Due to the self-clamping feature in the CIGBTs, the saturation current can be effectively controlled at a level of 4 times of the rated current. Therefore, the hybrid switch can survive for more than 10 μs under short circuit condition.

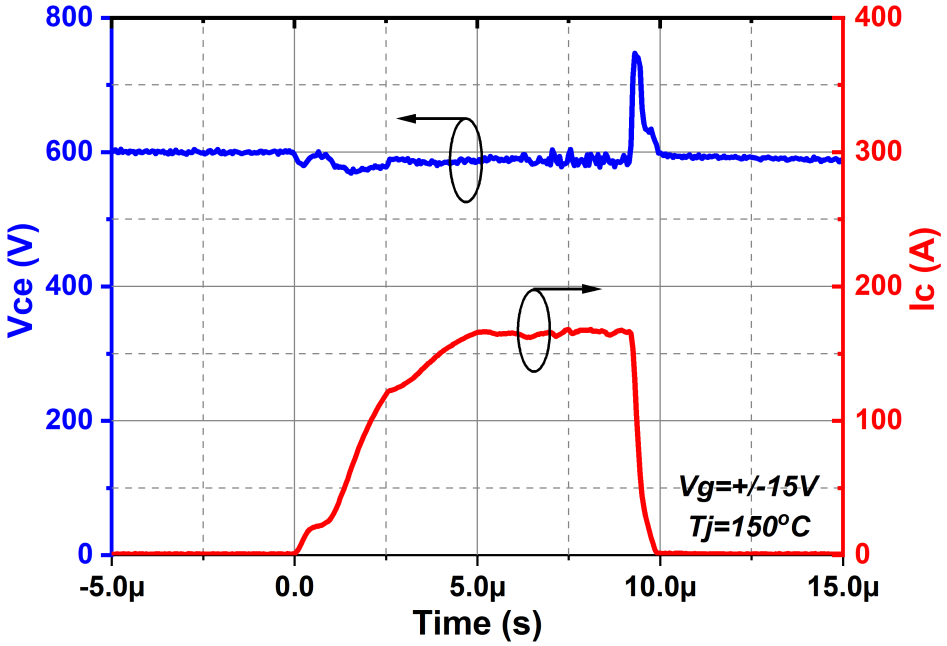


Figure 5.11 Short-circuit performance of the hybrid switch at T_j = 150 °C.

5.4 Summary

In this chapter, a 1200 V / 40 A hybrid switch concept is proposed and demonstrated through experiments. Compared to full CIGBT device, significant reduction of switching energy losses can be achieved by the hybrid switch. Therefore, the excellent performances enable the hybrid switch to be a promising candidate for medium voltage power semiconductor applications.

Chapter 6 COMPARISON OF ON-STATE PERFORMANCE LIMITS OF SILICON IGBTS AND 4H-SIC IGBTS

In this chapter, the ideal on-state performance of an IGBT is analysed through static modelling of a high current PiN diode. The on-state performance limits of silicon IGBTs and 4H-SiC IGBTs in field-stop technology are compared under identical current densities. The channel resistances are considered in the calculations. Furthermore, TCAD simulations are employed to examine the proposed theoretical performance limits.

6.1 Introduction

Silicon Carbide (SiC) based power devices are well suited for high voltage power electronics by taking the advantages of its superior physical and electrical properties, such as high critical electric field, high electron velocity and high thermal conductivity. Owing to the remarkable progress in material growth and device technologies, SiC unipolar devices have been introduced commercially from 600 V to 1700 V [82-84]. The first commercial SiC power device was a Schottky Barrier Diode (SBD), which was released in 2001 [85]. After the improvement of channel mobility and gate oxide reliability, a 1.2 kV planar type SiC MOSFET became commercially available in 2011 [84] and the trench type SiC MOSFET was reported in 2015 [86]. The highest blocking voltage reported so far is the 15 kV SiC MOSFETs [87], which have been used in developing high frequency solid-state transformers [88]. Although the SiC MOSFETs have exhibited superior high frequency switching performance in comparison to Si-IGBTs, the on-state losses increase dramatically when blocking voltage is higher than 10 kV. Moreover, the specific on-resistance ($R_{on,\,sp}$) further increases with increasing junction temperature due to reduced carrier mobility. Therefore, using ultra-high voltage (> 10 kV) unipolar devices for high power applications is not a cost-effective solution from the practical point of view.

To operate beyond the 1-D material limit for SiC unipolar devices, SiC bipolar devices such as 4H-SiC IGBTs with blocking voltages from 5.8 kV to 27 kV have been developed to achieve a much higher current density [89-113]. The first 4H-SiC IGBT was reported in 1999 [89] and the early fabricated SiC IGBTs were mostly p-channel type due to easy availability and low resistance of n^+ substrates [111]. After SiC epitaxial growth and fabrication technologies became mature, n-channel SiC IGBTs were developed with thick free-standing SiC epitaxial layers and various substrate removal/grinding processes [100, 105, 108, 110]. As the electron mobility is nearly 8 times higher than the hole mobility in 4H-SiC, n-channel IGBTs are more favored than p-channel IGBTs due to lower on-state voltage drops and faster switching speeds [102, 114]. However, the large built-in potential induced by the wide bandgap of SiC (3.26 eV) is still a primary limitation to the on-state performance. Another challenge is the low ambipolar lifetime which is generally on the order of 1 μs [109]. Without high ambipolar lifetime, the diffusion lengths of the carriers are not sufficient to generate high levels of conductivity modulation within the drift regions. Recent efforts on lifetime enhancement procedures have confirmed that long time (10~15 hours) thermal oxidation at 1300 ºC can improve the as-grown drift ambipolar lifetime to more than 10 μs [109, 115, 116]. Such high carrier lifetime can result in a higher level of conductivity modulation in the SiC bipolar devices and enable the blocking voltages of 4H-SiC IGBTs to be further increased. In the meantime, the developments on silicon-based power devices have shown significant progress in terms of power efficiency as well as blocking capability. For example, a silicon IGBT device in planar gate and Soft-Punch-Through (SPT) technologies has shown a breakdown voltage of 8.4 kV with superior on-state performance and short-circuit capability [117]. In addition, the silicon Light-Triggered Thyristors (LTT) with conventional field-stop layers can yield a blocking capability of more than 13 kV [118, 119]. Recently, the feasibility study of a 13 kV silicon IGBT was discussed [120]. The proposed device can be operated under a DC voltage of 6.6 kV and at a switching frequency of 150 Hz.

Therefore, it becomes imperative to investigate the on-state performance limit of 4H-SiC IGBTs with comparison to the theoretical limit of IGBTs (Si-IGBTs) [73].

6.2 Ideal On-state Performance of an IGBT

Figure 6.1 shows the on-state charge distributions within an IGBT. The theory of achieving the lowest forward voltage drops in a PiN diode or an IGBT has been proposed in [73, 121]. As per this model, electrons are injected from channel inversion layers and accumulated beneath the trench gate, a PiN diode structure is thus formed within the IGBT. Since the channel resistance of an IGBT is largely dependent on the MOS structure design and the channel mobility, the improvement of the on-state behaviour of an IGBT is mainly focused on improving the carrier distribution within the N-drift layer. For a definite current density, a higher carrier density within the drift region is desirable to obtain a lower forward voltage drop ($V_{ce(sat)}$). The electron injection efficiency (γ_E) is defined as the ratio of the electron current density to the total current density, as shown in (6.1). Assuming bipolar condition ($n \approx p$) is satisfied within the drift layer and eliminating the parameter of electric field (E) from (6.2) - (6.4), the slope of the excess carrier profiles at the cathode side can be expressed as (6.5). Therefore, it can be concluded that the IGBT structure performs the lowest $V_{ce(sat)}$ when the γ_E is close to 1.

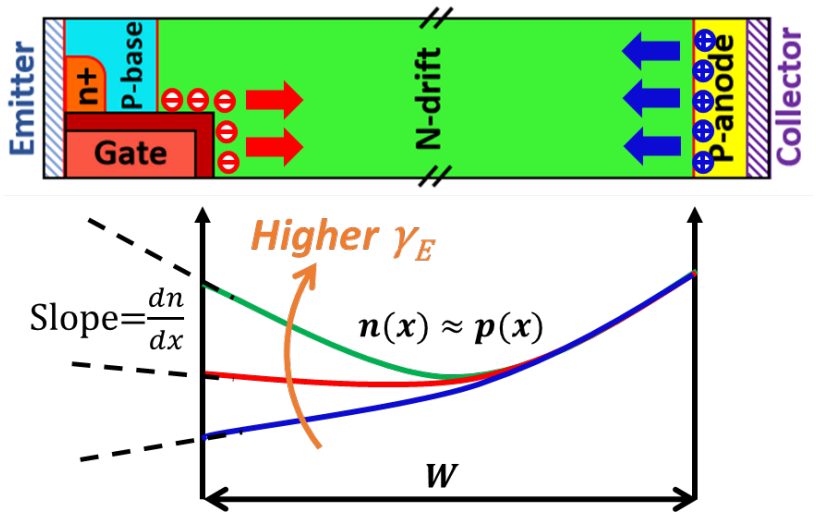


Figure 6.1 Charge distributions within an IGBT.

$$\gamma_E = \frac{J_n}{J} = \frac{J_n}{J_p + J_n} \tag{6.1}$$

$$J_p = qp\mu_p E - qD_p \frac{dp}{dx} \tag{6.2}$$

$$J_n = qn\mu_n E + qD_n \frac{dn}{dx} \tag{6.3}$$

$$D_{n,p} = \left(\frac{kT}{q}\right)\mu_{n,p} \tag{6.4}$$

$$\frac{dn}{dx} = \frac{J(\mu_n + \mu_p)}{2kT\mu_n\mu_p} \cdot (\gamma_E - \frac{\mu_n}{\mu_n + \mu_p}) \tag{6.5}$$

6.3 Static Modelling of an IGBT

The $V_{ce(sat)}$) of a trench IGBT structure consists of three components:

1) junction voltage (V_J);

2) drift voltage (V_{drift});

3) the voltage drop (V_{ch}) across the channel resistance (R_{ch}).

As per the analysis in previous section, the ideal on-state performance can be assumed that all the current is conducted by electrons (γ_E = 1) and the excess carrier profile within the i-layer/drift-layer features a linear decrease from cathode side to anode side, as depicted in Figure 6.2. It is also assumed herein that the carrier lifetimes are long enough and there is no recombination within the N-drift region. As the hole current is absent (J_p = 0), the electric field can be expressed as (6.6). Thus, the V_{drift} can be obtained by integrating the electric field within the N-drift region, as shown in (6.7). In addition, the V_J consists of the voltage across the P-anode/N-drift junction (J_1) and the voltage across the accumulation layer/N-drift interface (J_2), as expressed in (6.8) - (6.10), where the p_0' and n_W' are the hole and electron concentration at J_1 and J_2 under equilibrium, respectively. Therefore, the minimum $V_{ce(sat)}$ can be derived with the distributed carrier concentration (n_0 and n_W), which can be calculated by integrating

(6.11). According to the assumption in [121], the n_0 can be expressed as (6.12), where Q_{pa} and D_{n0} are the P-anode dose and electron diffusion coefficient in the P-anode, respectively. $D_n(n)$ can be described with the carrier-carrier scattering mobility proposed for a germanium diode [122, 123], as shown in (6.13) -(6.15), where m_n and m_p are the density-of-state effective masses for electron and hole, respectively. As described in [121], the $D_n(n)$ can be further simplified as (3.16) -(3.18), where n_m is the maximum electron concentration within the N-drift region. At last, the carrier distribution ($n(x)$) shown in (6.19) is calculated with (6.11), (6.12) and (6.16). The minimum $V_{ce(sat)}$ of an IGBT device considered V_{ch} is finally expressed in (6.20).

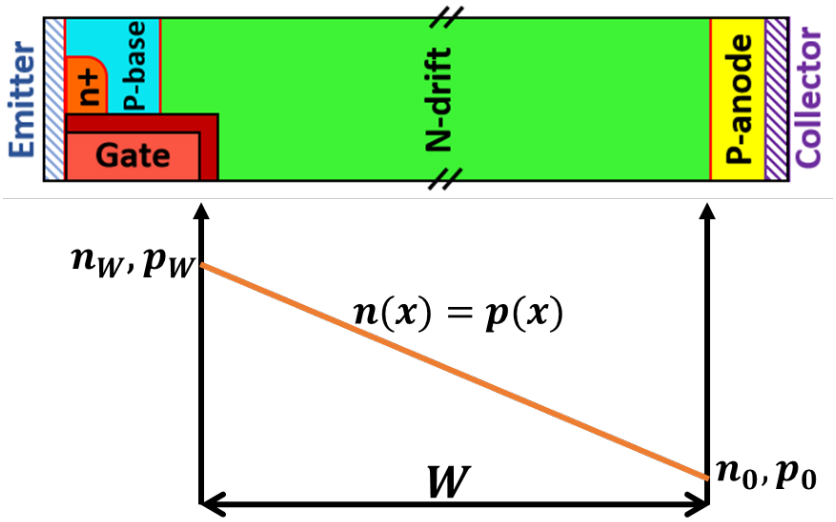


Figure 6.2 Ideal on-state carrier distribution within an IGBT.

$$E = \frac{kT}{q}\frac{1}{n}\frac{dn}{dx} \tag{6.6}$$

$$V_{drift} = \int_0^W E\,dx = \frac{kT}{q}\ln\frac{n_W}{n_0} \tag{6.7}$$

$$V_{J1} = \frac{kT}{q}\ln\frac{p_o}{p_0'} \tag{6.8}$$

$$V_{J2} = \frac{kT}{q} \ln \frac{n_W}{n'_W} \tag{6.9}$$

$$V_J = V_{J1} + V_{J2} = \frac{kT}{q} \ln \frac{n_o n_W}{n_i^2} \tag{6.10}$$

$$D_n(n) \frac{dn}{dx} = \frac{J_n}{2q} = \frac{J}{2q} \tag{6.11}$$

$$n_0 = \sqrt{Q_{pa} J / q D_{n0}} \tag{6.12}$$

$$\mu_n = \frac{q}{kT} D_n = \frac{q}{kT} \frac{B}{n \ln (A/n)} \tag{6.13}$$

$$A = \frac{2.07 \times 10^{15} \times T^2}{m_n^{-1} + m_p^{-1}} \tag{6.14}$$

$$B = 2.16 \times 10^{13} \times (m_n^{-1} + m_p^{-1})^{1/2} \times T^{5/2} \tag{6.15}$$

$$D_n(n) = a/(n + b) \tag{6.16}$$

$$a = B / \left\{ \left(1 + \ln \frac{A}{n_m}\right) + \left(1 + \ln \frac{A}{n_m}\right)^{-1} \right\} \tag{6.17}$$

$$b = a/D_n(0) = a/D_{n0} \tag{6.18}$$

$$n(x) = \left(\sqrt{\frac{Q_{pa} J}{q D_{n0}}} + b \right) e^{\left(\frac{Jx}{2qa}\right)} - b \tag{6.19}$$

$$\begin{aligned} V_{ce(sat)} &= V_{drift} + V_J + V_{ch} = \frac{2kT}{q} \ln \frac{n_W}{n_i} + R_{ch} J \\ &= \frac{2kT}{q} \ln \left[\frac{1}{n_i} \left\{ \left(\sqrt{\frac{Q_{pa} J}{q D_{n0}}} + b \right) e^{\left(\frac{Jx}{2qa}\right)} - b \right\} \right] + R_{ch} J \end{aligned} \tag{6.20}$$

6.4 Performance Limits of Si IGBTs and 4H-SiC IGBTS

To calculate the on-state performance limits of Si-IGBTs and 4H-SiC IGBTs, the electrical properties of silicon and 4H-SiC are listed in Table 6.1. The N-drift thickness (W) used for calculation is considered as the drift layer thickness of field-stop IGBTs. Figure 6.3 shows the dependence of breakdown voltage on W and N-drift doping concentration (N_d). As the critical electric field strength of the 4H-SiC is almost 10 times higher than that of silicon, the 4H-SiC IGBT can achieve an equivalent breakdown voltage with only 1/10 of the drift thickness of a Si-IGBT. In addition, it should be noted that the N_d required for Ultra-High Voltage (UHV) Si-IGBTs (> 10 kV) is lower than the silicon intrinsic carrier concentration (n_i) at T_j = 125 °C, as shown in Table 6.1. Therefore, the n_i poses a fundamental limit on the maximum operating temperature of UHV Si-IGBTs. In contrast, 4H-SiC IGBTs do not suffer from this issue owing to the much lower n_i as a result of wider energy bandgap. Hence, 4H-SiC IGBTs can achieve a much higher operating temperature from the blocking capability point of view.

Properties (T_j = 25 °C / 125 °C)	***Silicon***	***4H-SiC***
Energy Bandgap (eV)	1.12 / 1.09 [124]	3.26 / 3.23 [85]
Intrinsic carrier concentration n_i (cm^{-3})	1×10^{10} / 6.16×10^{12} [124]	1.73×10^{-8} / 0.24 [85]
Electron mobility μ_n (cm^2/Vs)	1450 / 715 [125]	950 / 476 [126]
Electron diffusion coefficient D_{n0} (cm^2/s)	37.4 / 24.6	24.5 / 16.37
Electron density-of-state effective mass m_n (m_0^{-1})	1.18 / 1.22 [124]	0.4 / 0.41 [127]
Hole density-of-state effective mass m_p (m_0^{-1})	0.81 / 0.85 [124]	2.64 / 2.65 [127]
Maximum electron concentration n_m (cm^{-3})	1×10^{18}	1×10^{17}
P-anode dose Q_{pa} (cm^{-2})	5×10^{13}	3×10^{15}

Table 6.1 Electrical properties of silicon and 4H-SiC.

On the other hand, the Auger recombination and band-to-band (radiative) recombination have a significant impact on the effective carrier lifetime at high injection levels [128]. Therefore, the maximum excess carrier density within the PiN model must take Auger recombination and band-to-band recombination into account. In the theoretical investigation of Si-IGBT performance limit [73], the excess carrier density is in the range of 1×10^{17} to 1×10^{18} cm^{-3} at high current densities, and the diffusion coefficient value is significantly reduced compared with the simulation results when the carrier density is higher than 1×10^{18} cm^{-3}. Thus, the maximum electron density considered herein is 1×10^{18} cm^{-3} for the analysis of Si-IGBT performance limits. However, in the ultra-high voltage 4H-SiC PiN diodes, the band-to-band recombination significantly reduces the effective carrier lifetime when the excess carrier concentration is higher than 1×10^{17} cm^{-3} [128], which poses an inherent limit on the on-state performance. As shown in Figure 6.7 and Figure 6.8, the excess carrier density within a 110 μm drift layer is in the range of 1×10^{16} to 1×10^{17} cm^{-3} at J_c = 100 A/cm^2, the estimated ambipolar diffusion length in this case is about 100 μm [128], which is sufficient to highly modulate a drift layer below 200 μm [14]. Therefore, the maximum electron density used for 4H-SiC IGBTs is 1×10^{17} cm^{-3}.

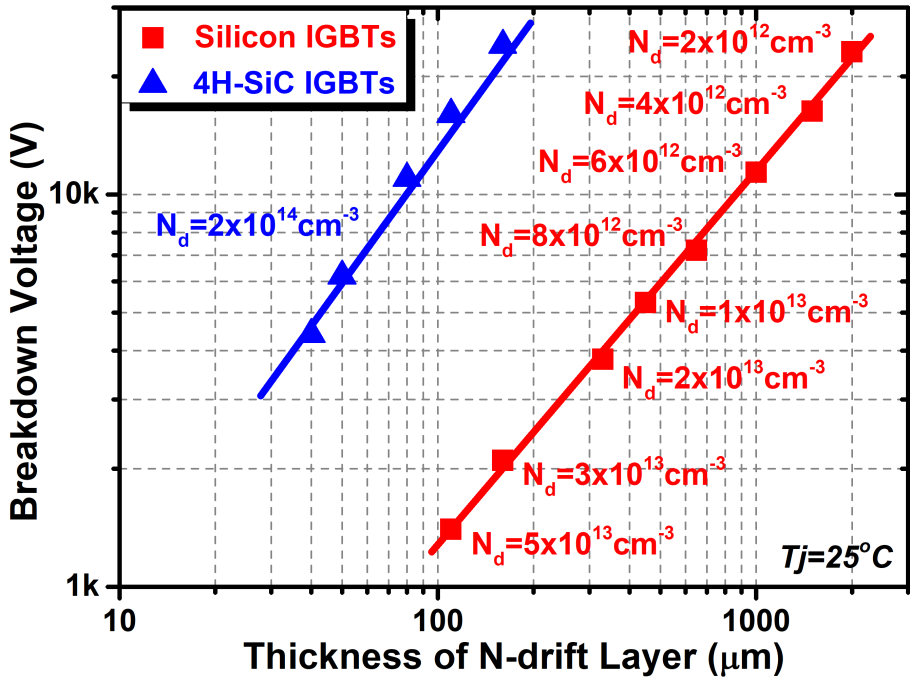


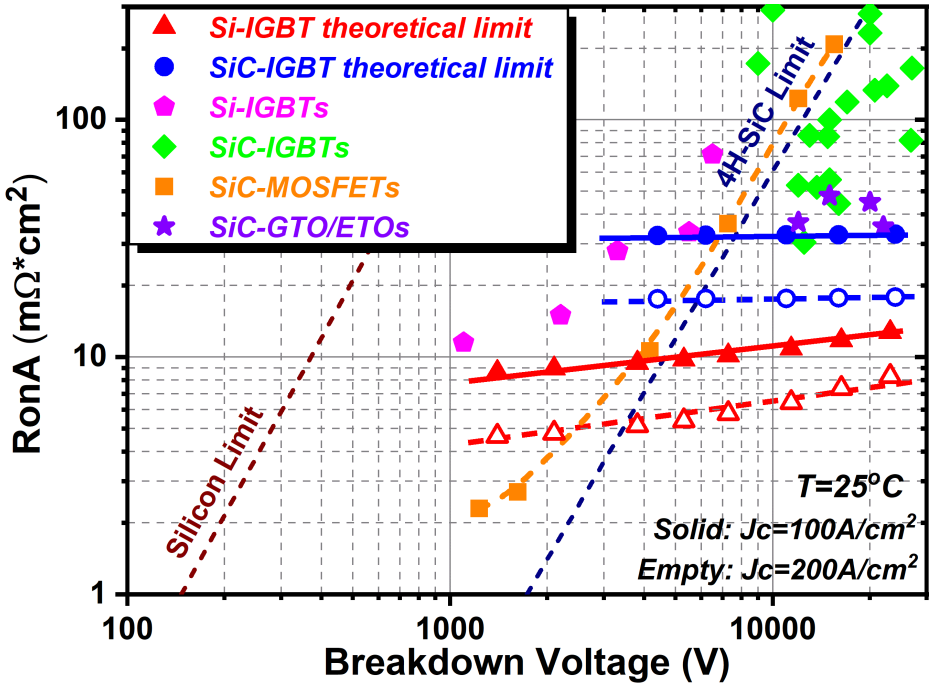
Figure 6.3 Dependence of breakdown voltage on N-drift thickness and doping concentration.

Moreover, the low channel mobility of 4H-SiC IGBTs results in a high channel resistance [95, 96, 98], which cannot be ignored in the analysis of on-state performance. The reason for low channel mobility can be explained by the high density of interface traps, which leads to strong Coulomb scattering at the interface of SiC/SiO_2. The channel resistance can be calculated with (6.21), assuming that channel parameters are constant across the voltage range considered, and the channel layers are not conductivity modulated even in the narrow mesa IGBTs [32, 129]. Table 6.2 summarizes the channel parameters for Si-IGBTs and 4H-SiC IGBTs. Note that the channel parameters for 4H-SiC IGBTs are from the experimental data in [98], and the main parameters are kept constant for comparison. Due to the lower channel mobility, the R_{ch} of 4H-SiC IGBTs is 10 times higher than that of Si-IGBTs.

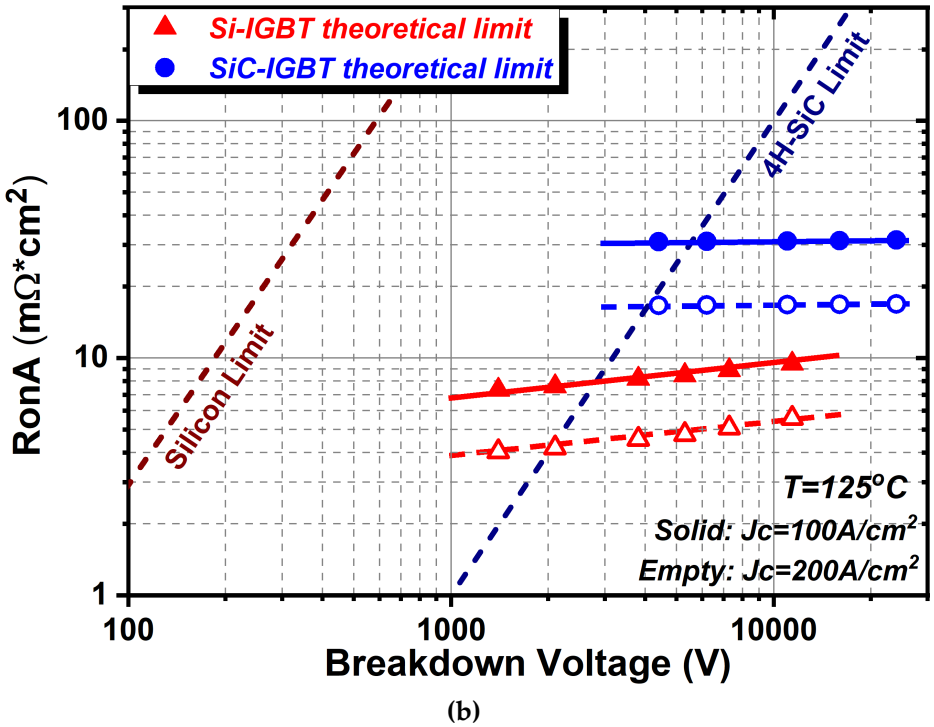
$$R_{ch} = \frac{W_{cell} L_{ch}}{2\mu_{ch} C_{ox} (V_g - V_{th})} \tag{6.21}$$

Parameters ***(T_j = 25 °C / 125 °C)***	***Si-IGBTs***	***4H-SiC IGBTs***
Channel mobility μ_{ch} (cm^2/Vs)	300 / 200 [130]	18 / 20 [98]
Cell pitch W_{cell} (μm)	14.5	14.5 [98]
Channel length L_{ch} (μm)	0.7	0.7 [98]
Gate oxide thickness t_{ox} (nm)	50	50 [98]
Gate voltage V_g (V)	20	20 [98]
Threshold voltage V_{th} (V)	3 / 2	3 / 2 [98]
Channel resistance R_{ch} ($m\Omega*cm^2$)	0.14 / 0.2	2.37 / 2.01

Table 6.2 Channel parameters.



(a)



(b)

Figure 6.4 Theoretical limits of Si-IGBT and 4H-SiC IGBT at (a) T_j = 25 °C and (b) T_j = 125 °C.

Figure 6.4 (a) and (b) compare the on-state performance limits between Si-IGBTs and 4H-SiC IGBTs at T_j = 25 °C and T_j = 125 °C, respectively. The absolute specific on-resistances ($R_{on,\,sp}$) are calculated at J_c = 100 A/cm² and J_c = 200 A/cm², respectively. In

addition, the experimental data of the Si-IGBTs [25, 27, 74-76], SiC IGBTs [89-111], SiC MOSFETs [82] and SiC GTOs/ETOs [131-134] are also plotted in Figure 6.4 (a). In comparison to the unipolar devices, the $R_{on,\,sp}$ of Si-IGBTs and 4H-SiC IGBTs are not sensitive to the variation in breakdown voltage owing to the conductivity modulated drift layers. Although both 4H-SiC IGBT experimental data and performance limits have shown significant improvement of $R_{on,\,sp}$ compared to that of SiC MOSFETs for UHV (> 10 kV) cases, the theoretical limits of 4H-SiC IGBTs are still much higher than that of Si-IGBTs when BV < 30 kV due to the large built-in potential (knee voltage). This is the case even at T_j = 125 °C although the built-in potential has decreased at high temperature. However, the UHV Si-IGBTs (> 10 kV) are lack of high temperature operation (T_j > 125 ºC) capability due to the inherent limit on breakdown voltage. In contrast, owing to the much lower intrinsic carrier densities at high temperatures, 4H-SiC IGBTs can remain high temperature operation capability without any impact on the blocking stability. Note that some experimental data of SiC IGBTs shown in Figure 6.4 (a) are close to the SiC-IGBT limit at J_c = 100 A/cm^2, because they are operated at current densities of more than 100 A/cm^2. However, they are still much higher than the theoretical limit at J_c = 200 A/cm^2. Therefore, there is still large room for SiC IGBTs to be further improved. Moreover, recent research showed that the channel mobility of a lateral trench SiC MOSFET can be significantly increased to 276 cm^2/V·s due to FinFET effect [135]. Hence, the on-state performance of trench SiC IGBTs is expected to be further improved by utilizing the technology in [135].

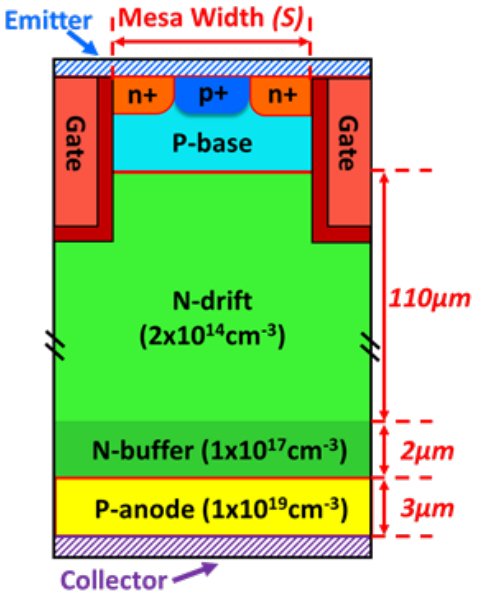


Figure 6.5 Cross-section view of a 15 kV 4H-SiC IGBT.

6.5 Simulation Study of a 15 kV 4H-SiC IGBT

A 15 kV 4H-SiC IGBT in field-stop and trench technologies is simulated through Silvaco TCAD [136] to examine the proposed performance limits. The cross-section of the simulated device and the structural parameters are shown in Figure 6.5. The thickness of the N-drift region is designed to be 110 μm in order to support more than 16 kV blocking voltage. Physical models including bandgap narrowing model, Shockley-Read-Hall (SRH) recombination and direct recombination (Auger) models [136] are specified within the simulations. Figure 6.6 and Figure 6.7 show the influence of various carrier lifetimes upon I -V characteristics and on-state carrier distributions within the N-drift region, respectively. The carrier lifetime specified in the simulations is the SRH lifetime, which is independent of excess carrier density [128]. As expected, increasing carrier lifetime can effectively improve the I-V performance due to the increase of excess carrier density within the N-drift layer. However, the I-V characteristics do not exhibit any further improvement when the carrier lifetime is increased to more than 10 μs. This is because the direct recombination limits the effective carrier lifetime at high level injection.

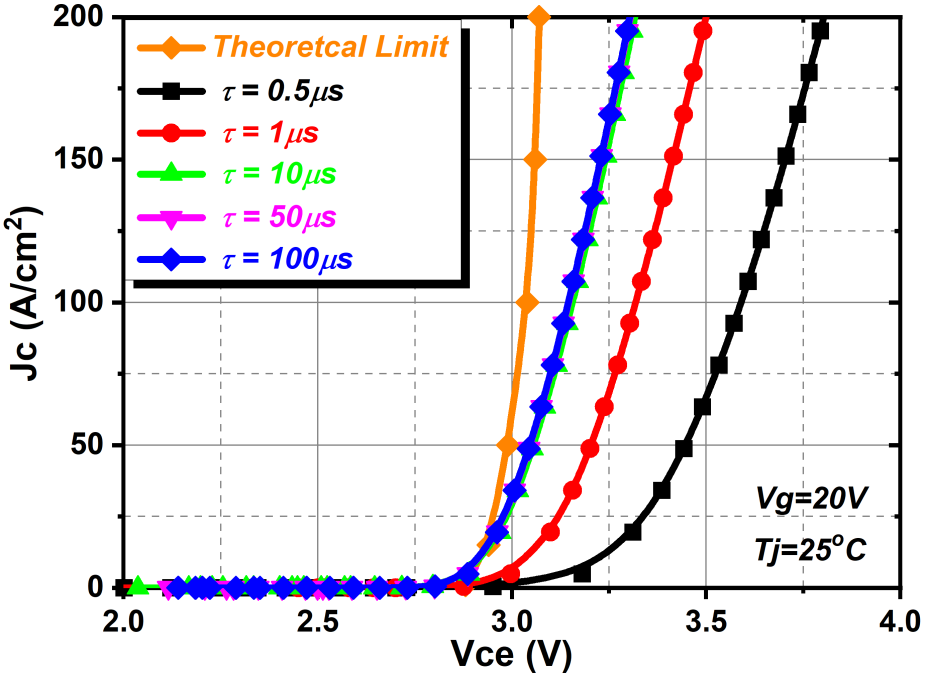


Figure 6.6 Influence of carrier lifetime upon I -V characteristics, mesa width S = 0.1 μm.

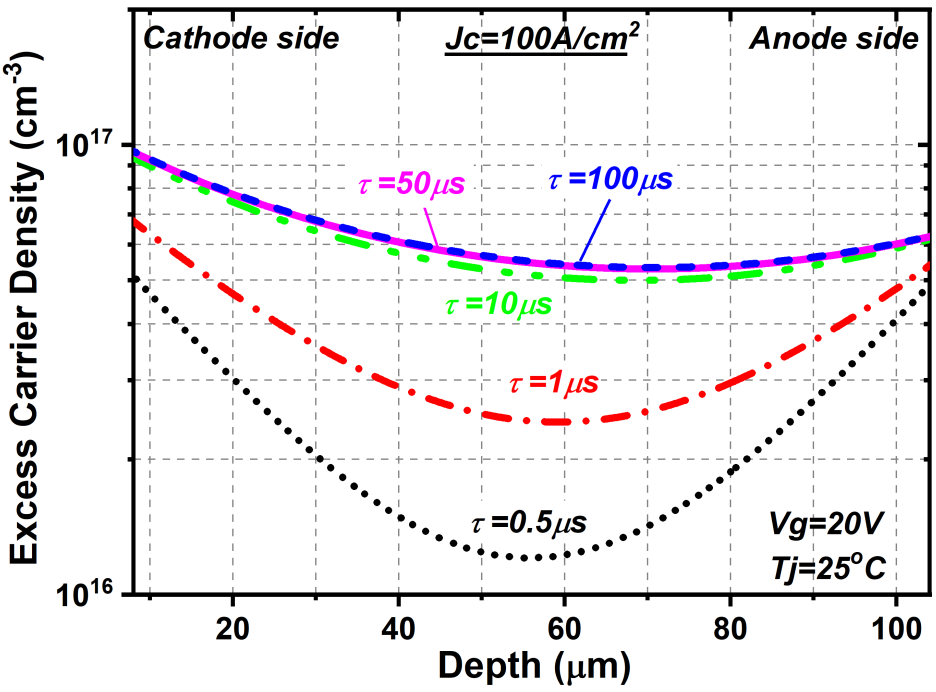


Figure 6.7 Influence of carrier lifetime on on-state carrier distributions, mesa width S = 0.1 μm.

Figure 6.8 shows the influence of γ_E on the on-state carrier density. The cathode side carrier density increases significantly with the increase in γ_E. The increase of γ_E is due

to the Injection Enhancement (IE) effect [17], which is achieved by scaling down the mesa width in this case. Smaller mesa width can constrict the flow of hole current into the emitter. Hence, more excessive holes pile up beneath trench corners, which increases the drift layer potential and enhances the electron current from the inversion layers. In addition, the influence of the γ_E upon $V_{ce(sat)}$ is depicted in Figure 6.9. It can be seen that the $V_{ce(sat)}$ decreases dramatically with increased γ_E and approaches the theoretical limit when γ_E is close to 1. The calculated $V_{ce(sat)}$ is 3.04 V at J_c = 100 A/cm² and T_j = 25 °C, which is slightly lower than the minimum $V_{ce(sat)}$ (3.09 V) obtained from simulation results. The slight difference is due to the occurrence of direct recombination in the simulations. However, if the direct recombination model is disabled in the simulations, the minimum simulated $V_{ce(sat)}$ will decrease to 3.04 V, which is closely matched with the theoretical calculation. Therefore, it can be concluded that the theoretical analysis regarding to the on-state performance limits of 4H-SiC IGBTs is consistent with the numerical simulation results.

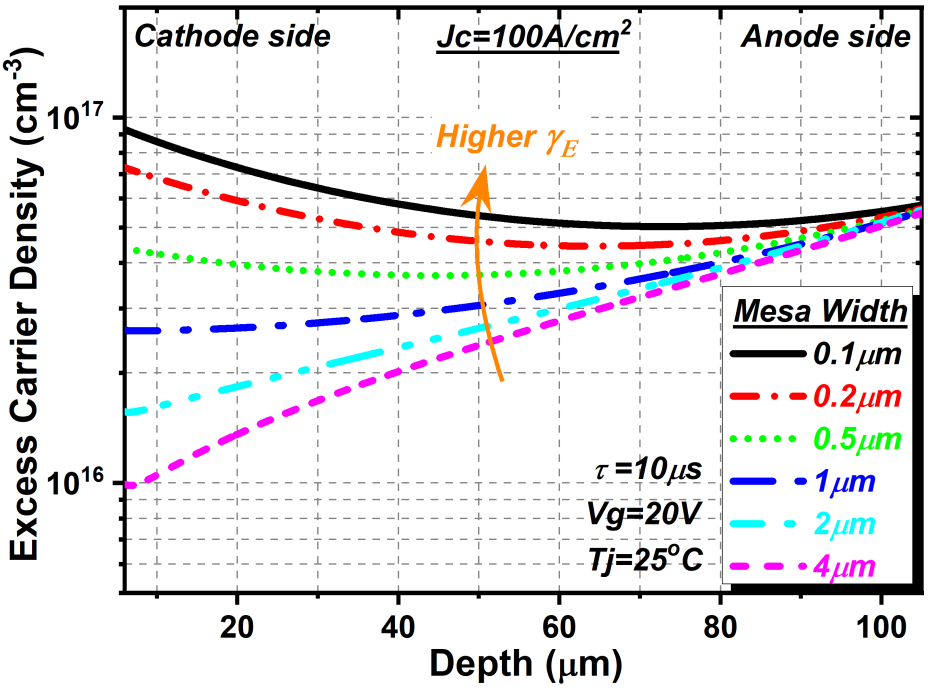


Figure 6.8 Influence of γ_E upon the on-state carrier density within the N-drift layer, trench width is kept identical for comparison.

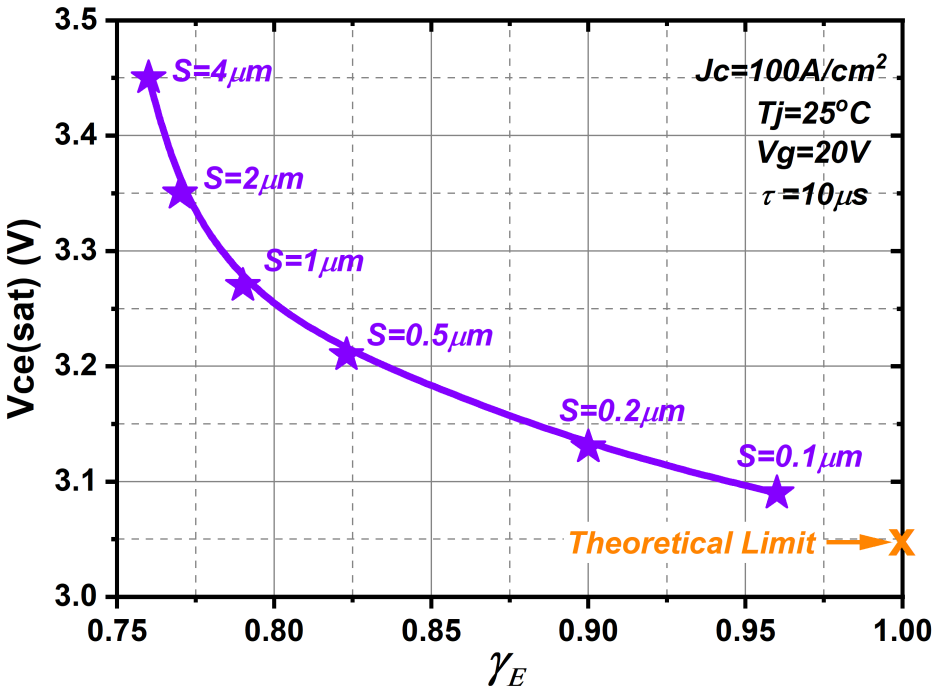
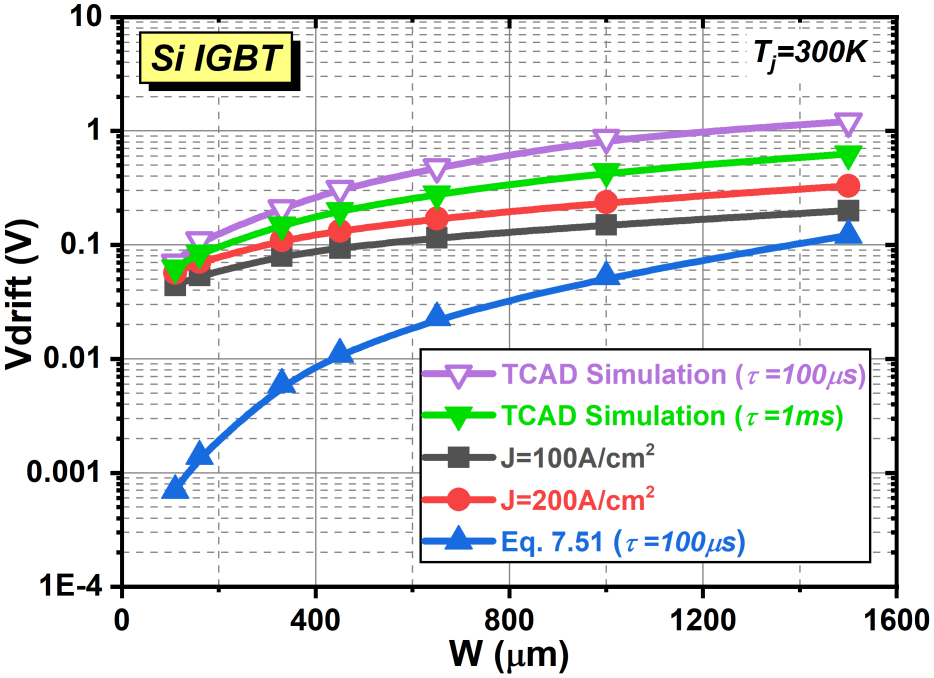
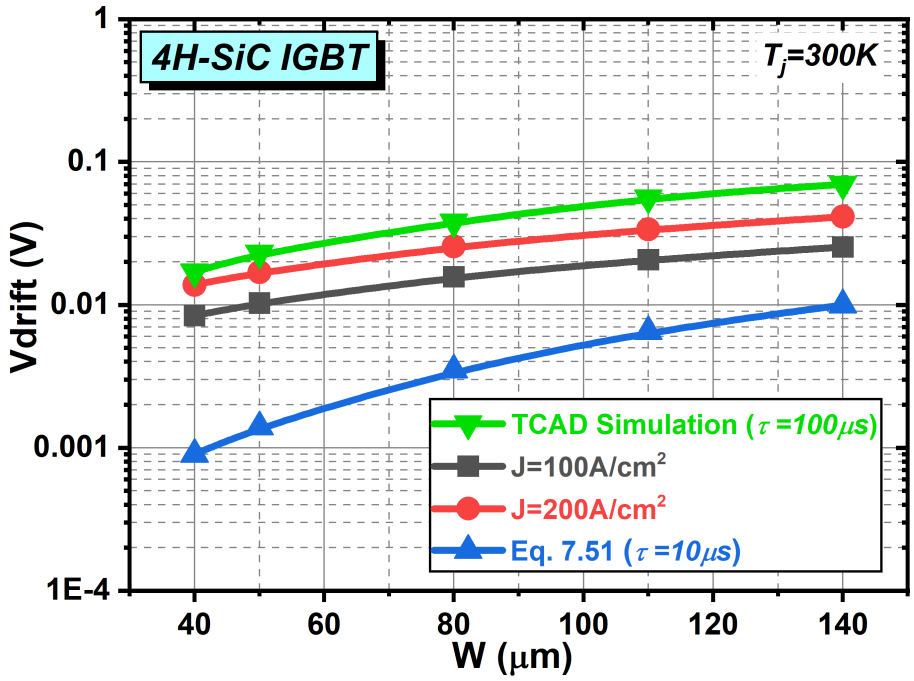


Figure 6.9 Influence of γ_E upon the $V_{ce(sat)}$ of the 15 kV 4H-SiC IGBT. The theoretical limit is calculated with a N-drift thickness of 110 μm.

Figure 6.10 (a) and (b) compare the theoretical analysis of V_{drift} in this paper with the theoretical analysis of Vdrift (Equation 7.51) in the textbook [85]. TCAD simulation results are used as benchmark to examine the proposed on-state limits herein and the theoretical analysis (Equation 7.51) in [85]. Note that the Equation 7.51 in [85] assumes unity injection efficiency at both cathode and anode sides, and the analysis is independent of current density. As shown in Figure 6.10, the calculation results in this paper are close to the simulation results and the estimated Vdrift increases with increasing current density. However, the Eq. 7.51 results are at least one order of magnitude lower than the simulation results, which are over low to estimate the on-state performance limits. This is because unity injection efficiency at anode side is difficult to realize because the field-stop layer limits the P-anode injection efficiency. Therefore, the theoretical analysis herein provides a more accurate method to estimate the on-state performance limits of IGBTs in field-stop technology.



(a)



(b)

Figure 6.10 Comparison of calculated V_{drift} with TCAD simulation results and the theoretical analysis in [85] of (a) Si-IGBT and (b) 4H-SiC IGBT. The simulation results are the V_{drift} of a PiN structure at J_c = 200 A/cm².

6.6 Summary

The on-state performance limits of silicon IGBTs and 4H-SiC IGBTs in field-stop technology are presented and investigated through theoretical analysis. Owing to the superior material properties, 4H-SiC IGBTs can provide high temperature operations at UHV conditions and the $R_{on,\ sp}$ does not show any significant increase with the increase in breakdown voltage due to conductivity modulation effect. However, the large built-in potential of 4H-SiC is the major limitation to the on-state performance in the temperature range considered. Simulation results show that the $V_{ce(sat)}$ of 4H-SiC IGBT can be reduced with increased carrier lifetime and tends to be saturated when carrier lifetime is longer than 10 μs. In addition, the on-state behaviour can be improved by increasing γ_E. In comparison to the 4H-SiC IGBTs, silicon IGBTs show much lower performance limit at room temperature, although their N-drift thicknesses are 10 times higher than that of 4H-SiC IGBTs. Consequently, the silicon-based IGBTs are still competitive in the applications below 13 kV, due to the superior on-state behaviour and much lower material cost, particularly as many of the UHV applications which do not require fast switching and high temperature operation capabilities. In addition, note that the $R_{on,\ sp}$ of the state-of-the-art silicon IGBTs are still much higher than the theoretical limit at a current density of 200 A/cm^2. Therefore, there is still great potential for silicon IGBTs to be further improved.

Chapter 7 DYNAMIC AVALANCHE IN MOS-GATED BIPOLAR DEVICES

It is well known that Dynamic Avalanche (DA) phenomenon poses fundamental limits on the power density, turn-off power loss, dV/dt controllability and long-term reliability of MOS-bipolar devices. Therefore, overcoming this phenomenon is essential to meet the requirements of future IGBT technologies. In this chapter, detailed analysis of 1.2 kV MOS-Bipolar devices are undertaken through both calibrated TCAD simulations and experiments to show the fundamental cause of DA and the impact of current density, supply voltage as well as 3D scaling rules on the DA performance. Furthermore, the dynamic avalanche performance of a 1.2 kV NPT Trench Clustered IGBT is evaluated for high current density and low power loss operations. The results indicate that this device configuration is free of DA and can be used for ultra-high current density operation in an energy efficient manner.

7.1 Introduction

Recent development of Trench IGBTs (TIGBTs) is focused on increasing power densities and switching frequencies with the aims to compete with Wide Band Gap (WBG) power devices and achieve design optimization and cost reduction for power conversion systems [137]. Several novel technologies have been implemented to continuously improve the switching loss (E_{off}) and on-state voltage drop ($V_{ce(sat)}$) trade-off through emitter side Injection Enhancement (IE) effect [24, 25, 28]. The improvements in the E_{off}-$V_{ce(sat)}$ trade-off have resulted in not only low loss operations but also increases in current densities and improved cost performance of TIGBT modules. Low E_{off} (high dV/dt) can reduce the system size, because passive components can be shrunk with high frequency operation. However, it is found that high current density and high dV/dt during switching can induce Dynamic Avalanche (DA) within the TIGBTs, which poses fundamental limits on the power density, turn-

off power loss, dV/dt controllability as well as long-term reliability of the IGBT modules [43, 45, 71, 138]. Tremendous efforts have been devoted to suppressing DA and eliminating associated reliability concerns. Using p-layers to protect the trench bottoms can suppress but not eliminate DA in the TIGBTs [43], and the holes evacuation is not enhanced. Moreover, an asymmetric gate oxide approach with a designed variable thickness to realize stable long-term operation in TIGBTs and to reduce the switching delay and gate charge without sacrificing the electrical performance has been reported [75, 139]. However, this design cannot suppress DA and no effective designs have been proposed to eliminate DA so far.

In this chapter, an in-depth analysis of the TIGBT switching behavior focusing on DA is presented through calibrated 3D TCAD models to show that removal of the high electric field concentration beneath the trench gates was the most important solution to manage the DA in TIGBTs. Moreover, a DA free design with high current density operation capability is demonstrated in a Trench Clustered IGBT (TCIGBT), through in both simulations and experiments. The influence of current density and supply voltage on the DA performance of TIGBTs is experimentally investigated. Finally, the impact of 3-D scaling rules of TIGBTs [29] on the DA behavior is evaluated in detail.

7.2 Dynamic Avalanche in TIGBTs

7.2.1 Schematic of DA in TIGBTs

Figure 7.1 shows the schematic of DA in the turn-off transient of trench gated IGBTs. During on-state, the carrier density ($p \approx n$) is typically in the range of 10^{16} to 10^{17} cm^{-3} due to conductivity modulation, which is at least two or three orders of magnitude higher than the background doping concentration (N_D). When the device turns off, an increase in the potential drop occurs within a small space charge region of the device with a large part of stored carriers still present. The electric field distribution within the device can be expressed as (7.1).

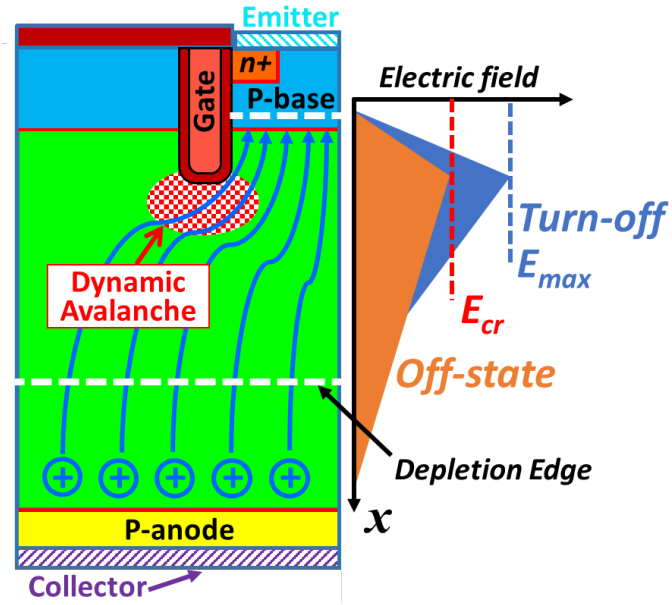


Figure 7.1 Schematic of DA during turn-off of TIGBT.

$$\frac{dE}{dx} = \frac{q}{\varepsilon}(N_D + p - n). \tag{7.1}$$

As depicted in Figure 7.1, the stored excess holes evacuate through the P-base region, resulting in a peak electric field (E_{max}) which is much higher than the off-state electric field strength. As electric field crowds beneath trench gates, the E_{max} appears at trench bottom rather than at the P-base/N-drift junction. If the resulting E_{max} exceeds the concentration dependent critical electric field (E_{cr}), DA will be triggered even when the collector voltage is well below the off-state breakdown voltage. More excessive carriers are thus generated to result in additional E_{off} and lower dV/dt. Moreover, the excessive carriers generated due to Impact Ionization (I.I.) can have enough energy to be injected into the trench oxide to affect the gate stability and cause associated reliability concerns.

7.2.2 Influence of DA on the TIGBTs Electrical Performance

To analyze the DA in silicon TIGBTs, the 3D Sentaurus Device [67] is utilized to simulate the switching behavior, with a circuit configuration for mix-mode simulation

as specified in Figure 7.2. The dependence of switch-off characteristics of a 1.2 kV TIGBT in Field-Stop (FS) technology on gate resistance (R_g) is shown in Figure 7.3.

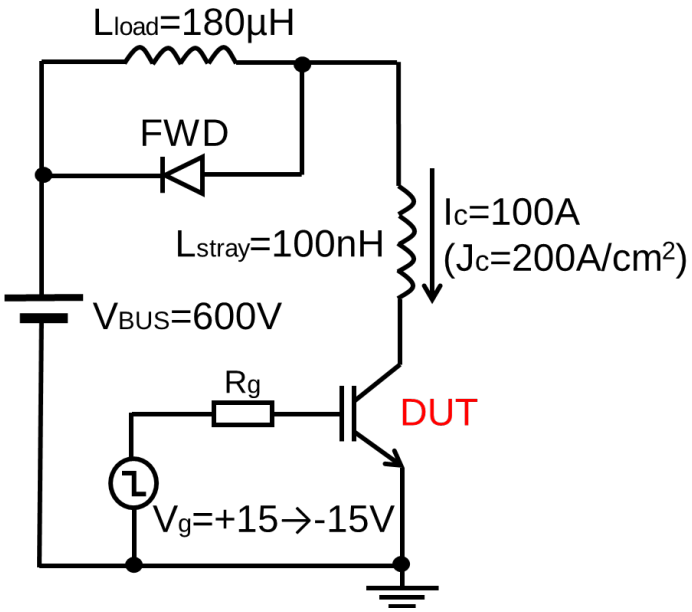


Figure 7.2 Test circuit configuration.

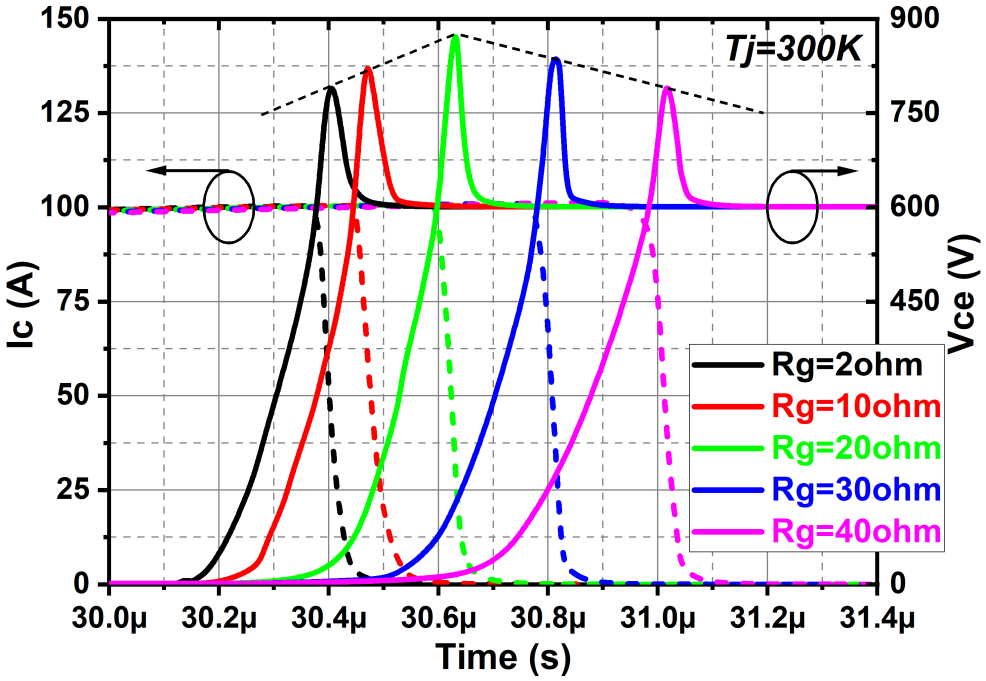


Figure 7.3 Simulated switch-off characteristics of TIGBT at various R_g.

In practice, smaller R_g should induce larger dV/dt during turn-off, the relationship between R_g and dV/dt can be expressed as

$$I_g = \frac{V_{th} + I_c/g_m}{R_g} \tag{7.2}$$

$$\frac{dV_{CE}}{dt} = \frac{I_g}{C_{GC}} \tag{7.3}$$

where I_g is the gate current, V_{th} is the threshold voltage, g_m is the transconductance of the IGBT structure, I_c is the collector current, and C_{GC} is the miller capacitance. However, the DA decreases the dV/dt, which results in decrease in surge voltage even with small R_g conditions, as shown in Figure 7.3. This clearly indicates that DA occurs in the cases of $R_g < 20\ \Omega$.

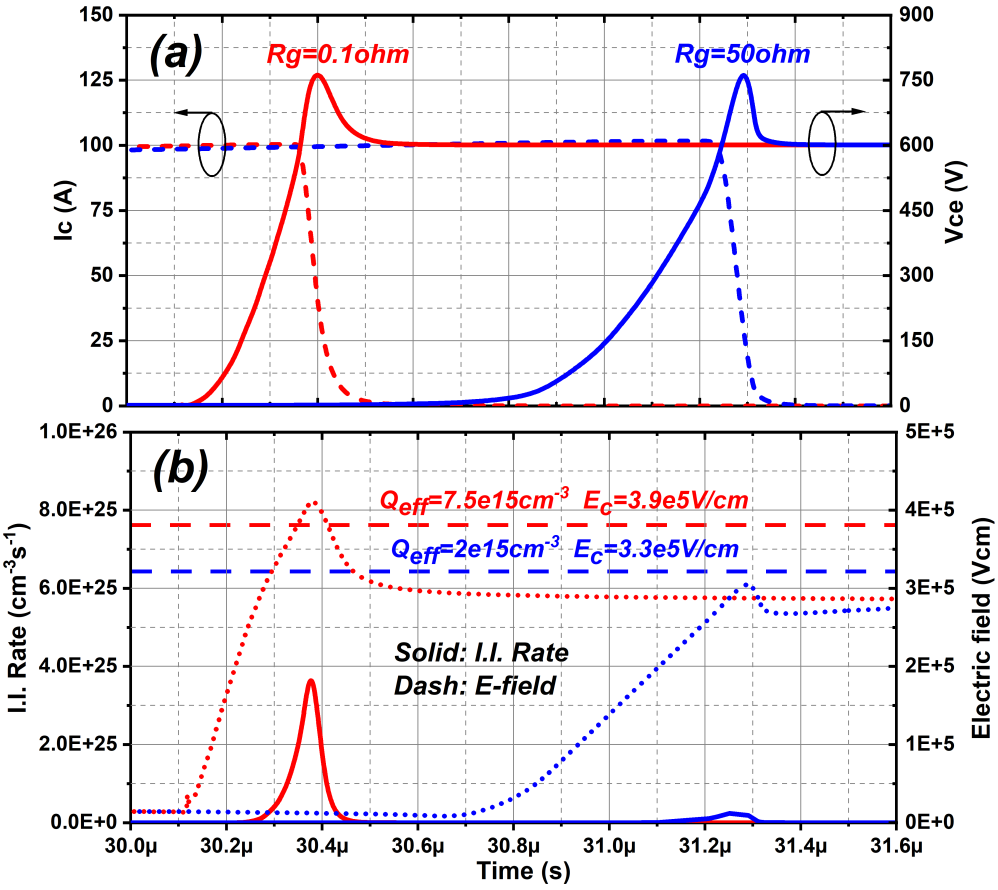


Figure 7.4 Comparison of (a) Turn-off curves and (b) I.I. rates and E_{max} of a TIGBT at $R_g = 0.1\ \Omega$ and $R_g = 50\ \Omega$.

Figure 7.4(a) compares the turn off curves while Figure 7.4(b) compares the maximum electric fields (E_{max}) and maximum I.I. rates in the cases of R_g = 0.1 Ω and R_g = 50 Ω, respectively. In the case of R_g = 0.1 Ω, due to faster increase in collector voltage (higher dV/dt), the stored excessive holes do not have enough time to be evacuated from the device and flow along the trench bottom, leading to a peak electric field strength which exceeds the critical value, as shown in Figure 7.4(b). The critical electric field strength is calculated with (7.4) and (7.5), where Q_{eff} is the space charge at trench corner.

$$E_{cr}(Silicon) = 4010 \times {Q_{eff}}^{1/8} \text{ [12]} \tag{7.4}$$

$$Q_{eff} \approx N_D + p \tag{7.5}$$

As a result, DA occurs and generates more excessive charge to lower the dV/dt. In contrast, under large R_g conditions, the time to reach supply voltage takes longer, during which most stored charges are removed and DA does not materialize. However, this comes at the expense of increased switching loss and longer turn-off delay time. Moreover, Figure 7.5 shows the simulated E_{off} with and without Avalanche Generation (AG) model. The saturation trend of E_{off} with AG model at small R_g conditions is due to DA.

In summary, DA can be triggered by high current density operation, high dV/dt condition, and current filamentation [140]. This phenomenon poses fundamental limits on operating current density, switching frequency, dV/dt controllability, and leads to reliability issues due to hot carrier effect. Therefore, eliminating DA is essential for the development of TIGBTs.

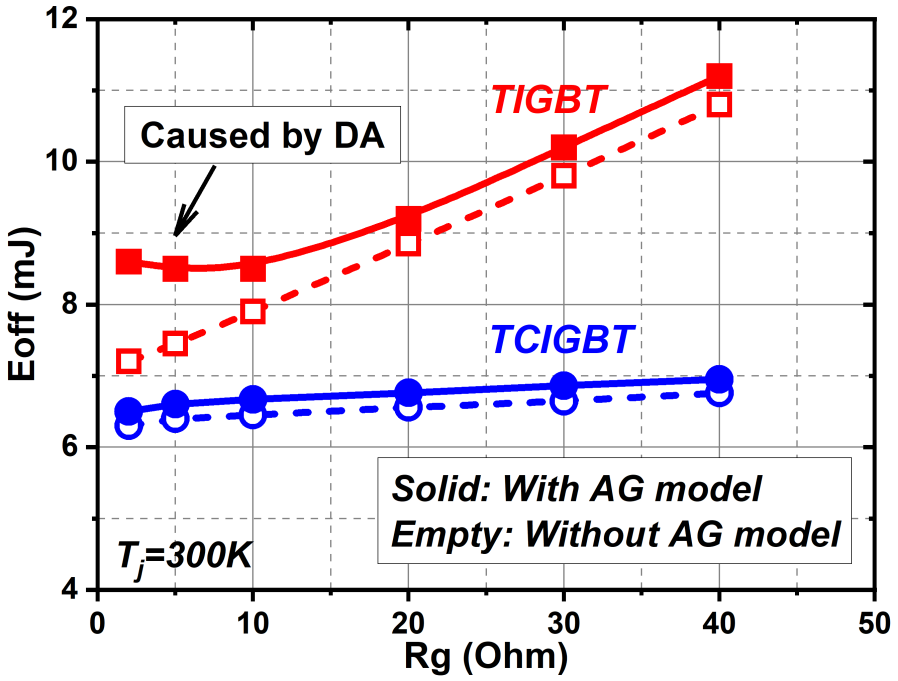


Figure 7.5 Dependence of E_{off} on R_g with AG model and without AG model.

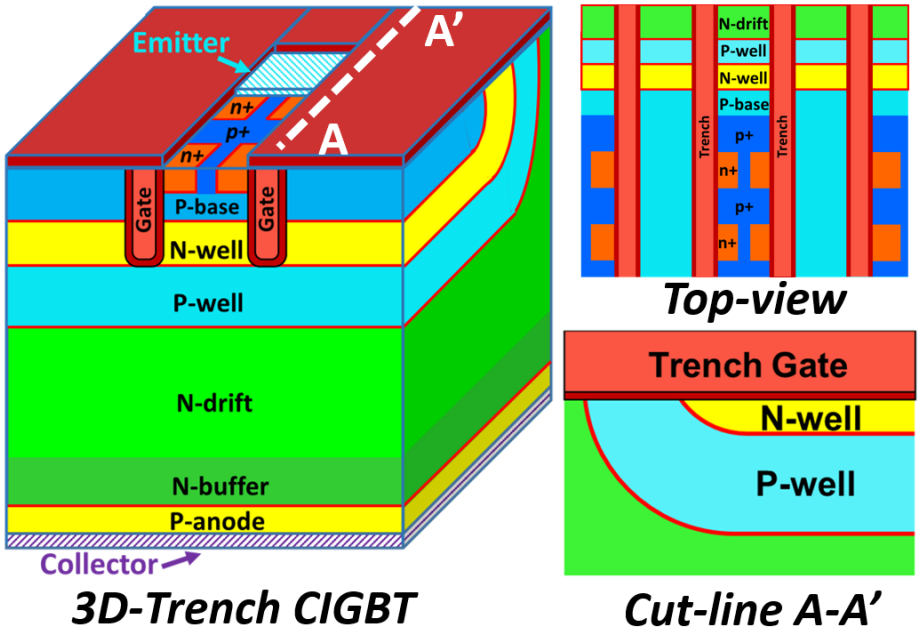
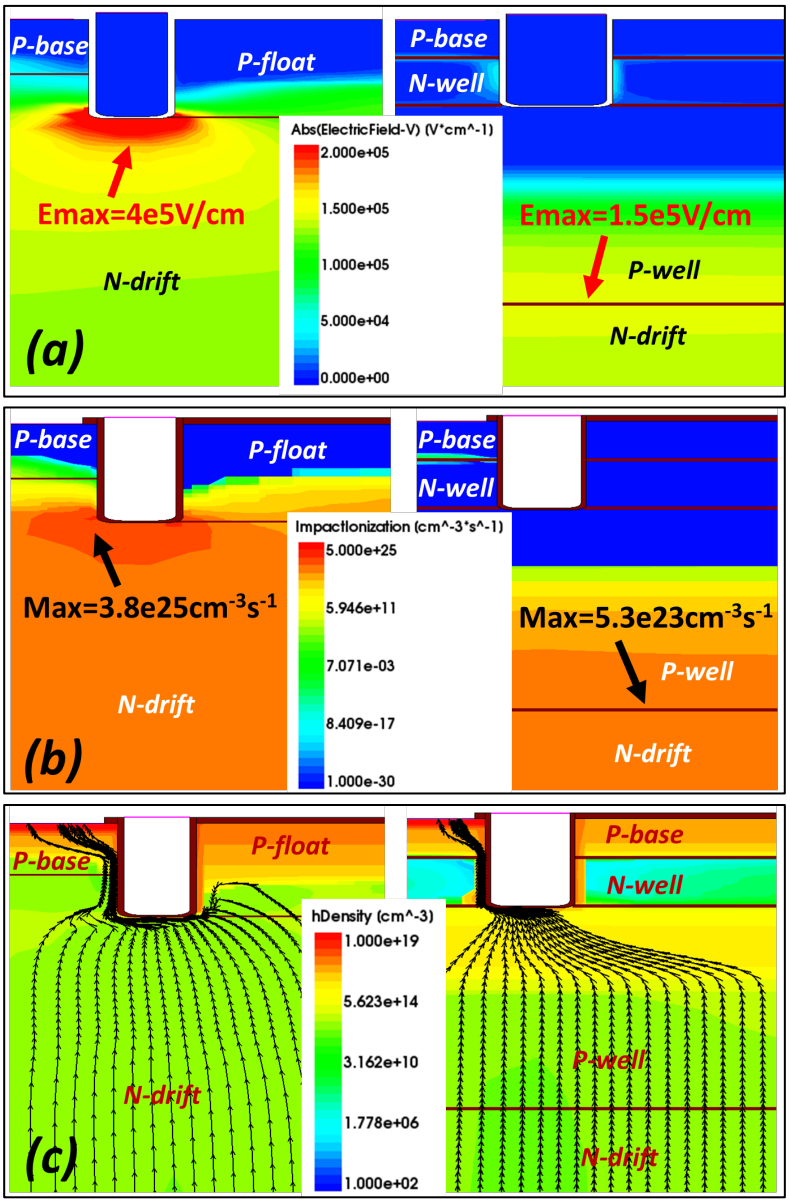


Figure 7.6 3-D cross-sectional view of TCIGBT.

7.3 Dynamic Avalanche Free Design: TCIGBT

Figure 7.6 shows the 3D cross-section view of the TCIGBT. The TCIGBT features a MOS-gated thyristor structure, which consists of P-anode, N-drift, P-well and N-well. In the on-state, the N well and P well are conductivity modulated and the device

undergoes self-clamping. During turn-off, when the collector voltage is increasing to a value higher than the self-clamping voltage, the potential of the N-well layer, which acts as the body of the PMOS will be held at a fixed potential of less than 20 V, which is the self-clamping voltage of TCIGBT. When the gate voltage decreases below its threshold voltage, because of the increase in body potential, holes are formed along the sidewall of trench gates to connect the P-well layer with P-base region through PMOS action, as shown in Figure 7.7(c).



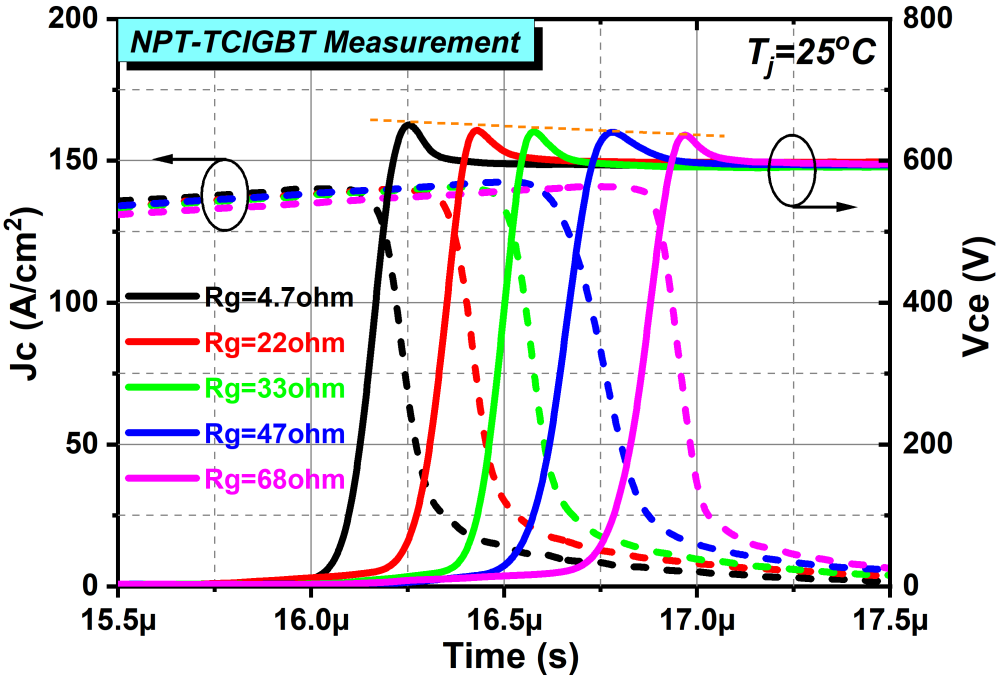
TIGBT TCIGBT

Figure 7.7 Comparison of (a) electric field distributions, (b) I.I. rate distributions and (c) hole densities when V_{ce} raises to 600V (R_g = 0.1 Ω).

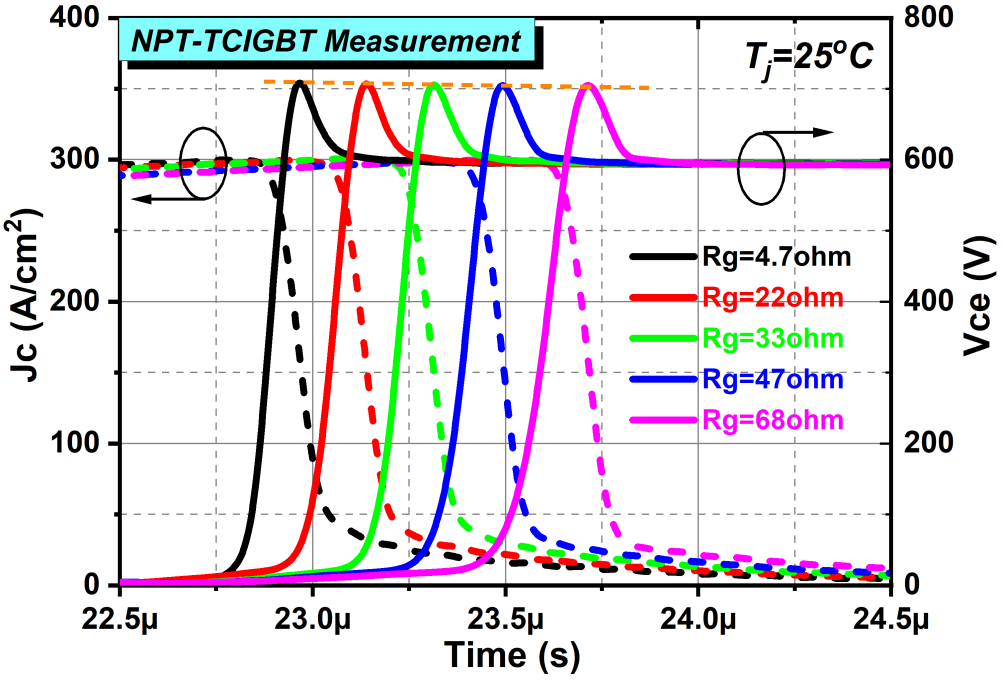
Therefore, whether the gate potential goes negative or not during turn-off has no impact on the turn-off behavior. Such a unique design, not available in TIGBTs, provides a direct evacuation path for excess holes to be collected within emitter region. The E_{off} is thus significantly reduced compared to the TIGBT, as shown in Figure 7.5. Moreover, as the collector voltage is supported by the P-well/n-drift junction, the trench gates are protected from high electric field so that there is no electric field crowding effect in TCIGBT, as shown in Figure 7.7(a). Thus, it provides a fundamentally simple solution for electric field management at trench regions to prevent occurrence of DA, as shown in Figure 7.5.

Figure 7.7(a), (b) and (c) show a comparison of the electric field distributions, I.I. rates and hole densities at the time point of V_{ce} increases to 600 V between TIGBT and TCIGBT under R_g = 0.1 Ω and identical $V_{ce(sat)}$ conditions, respectively. As can be seen, the trench gates of TCIGBT are protected from high electric field concentrations during turn-off. In comparison, the TIGBT shows a strong electric field crowding in excess of the E_{cr} under the trench bottom and leads to a high I.I. rate.

Absence of DA in TCIGBT is clear from the experimental results of the switching waveforms of 1.2 kV TCIGBTs measured as a function of R_g, as shown in Figure 7.8(a) and (b). These devices show a $V_{ce(sat)}$ of 1.8 V at 140 A/cm^2 at Room Temperature (R.T.) and can support 1.6 kV and are short circuit proof [56]. The device design is shown in [56]. Although the demonstrated devices were made in Non-Punch-Through (NPT) technology, moving to a thinner FS technology has no impact on the DA, as discussed later. Fig. 8(b) shows that TCIGBT does not show DA even at J_c = 300 A/cm^2. This confirms that TCIGBT can be operated at high current density without DA and associated reliability concerns and with very low power losses.



(a)



(b)

Figure 7.8 Experimental switch-off curves of TCIGBT at various R_g at (a) J_c = 140 A/cm² and (b) J_c = 300 A/cm².

7.4 Impact of Current Density on DA Performance

The continuous increase of power density is crucial for the development of IGBTs to achieve low cost and design optimization for power electronic systems. Higher power density requires higher operating current density as well as low power loss per chip area. However, Figure 7.9 shows that DA is significantly enhanced at high current density operations, which poses a limit on the operating current density of TIGBTs.

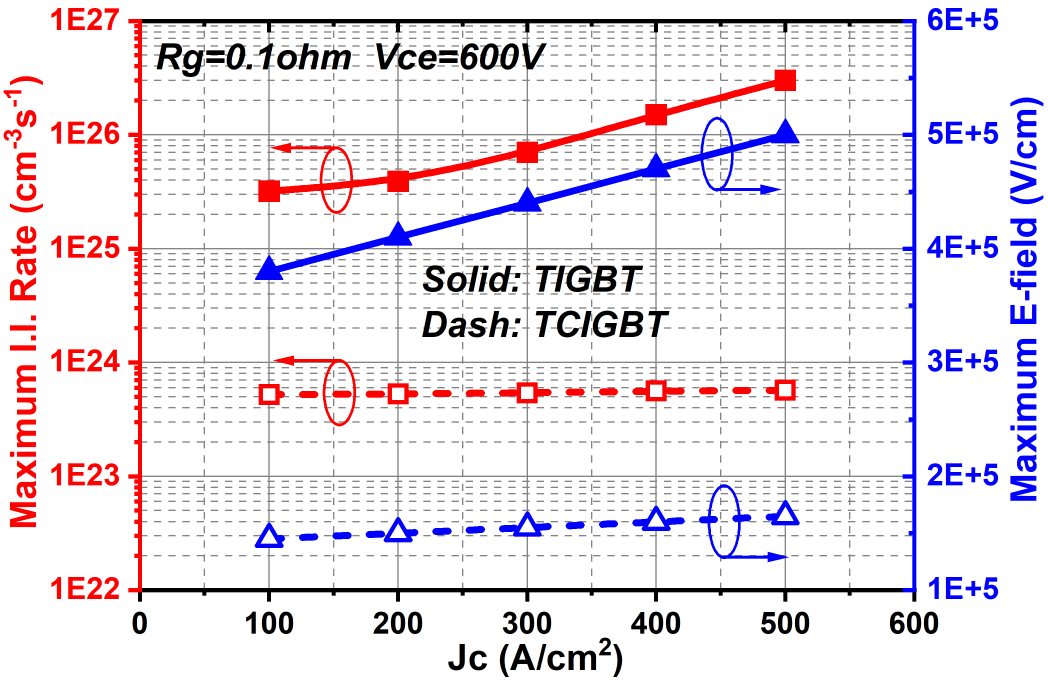


Figure 7.9 Impact of current density on E-field and I.I. rate during turn-off.

In order to clarify the influence of current density on the DA performance, a 1.2 kV 25 A TIGBT device in FS technology [141] was investigated in detail and compared with the measured results of a 1.2 kV NPT TCIGBT. Figure 7.10 shows the comparison of the measured IV characteristics at 25 ºC and 125 ºC. Despite the fact that the FS TIGBT (device thickness = 115 μm) features a much thinner device thickness than the NPT TCIGBT (device thickness = 200 μm), the TCIGBT shows much lower on-state losses in comparison to that of TIGBT at both rated current density (J_c = 140 A/cm²) and high current densities due to thyristor conduction.

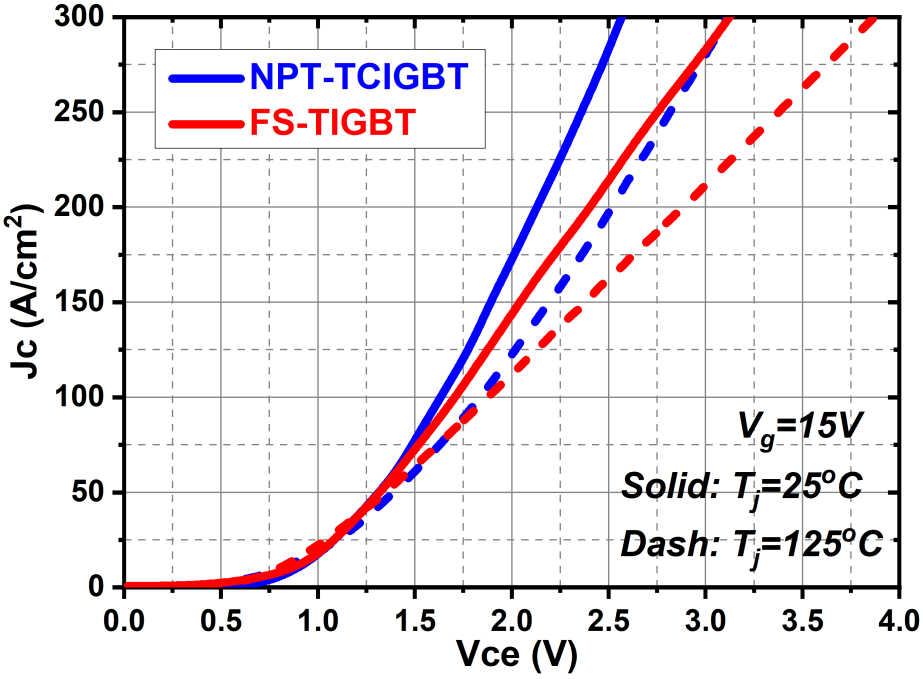


Figure 7.10 Experimental results of the I-V curves of TIGBT and TCIGBT.

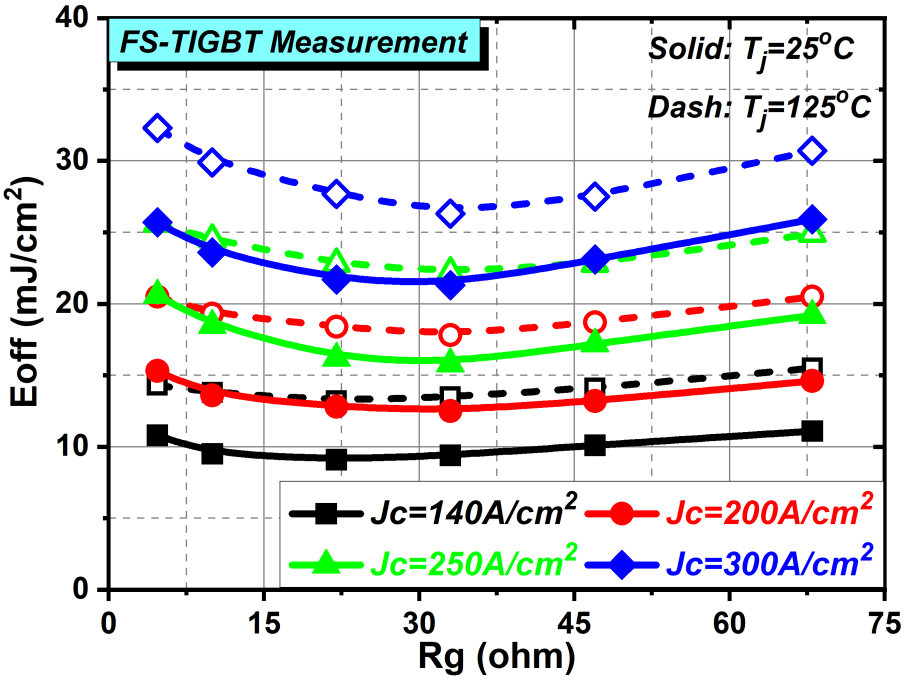


Figure 7.11 Impact of current density on the E_{off} of TIGBT.

Figure 7.11 shows the measured E_{off} of the TIGBT as a function of R_g at various operating current densities. The E_{off} increases more significantly at small R_g in the case of high current density operations due to enhanced DA. In contrast, the self-clamping feature ensures TCIGBTs to remain DA free performance at high current density

operations, as shown in Figure 7.12. The E_{off} shows linear decreases as R_g reduces at both R.T. and 125 ºC. Therefore, TCIGBTs are well suited for operating at high current densities without DA effects.

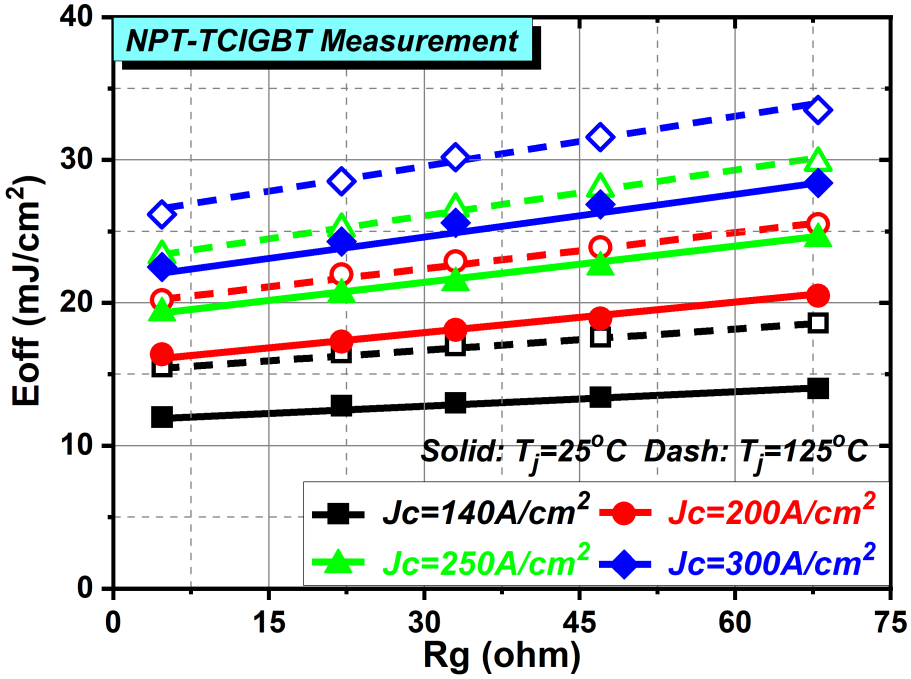


Figure 7.12 Impact of current density on the E_{off} of TCIGBT.

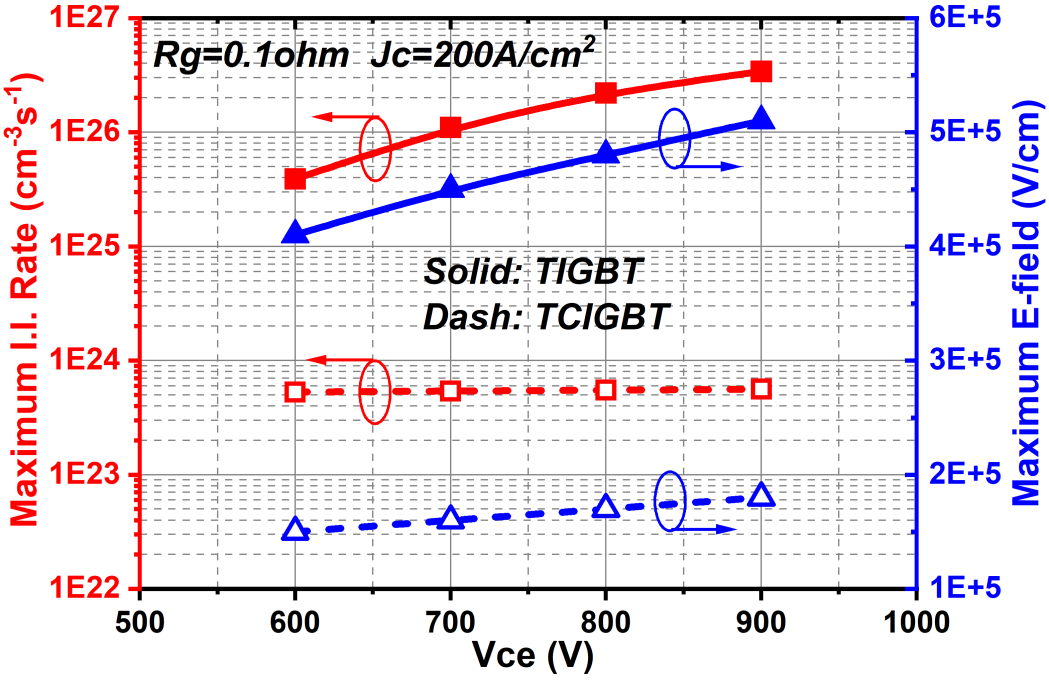


Figure 7.13 Impact of supply voltage on E-field and I.I. rate during turn-off.

7.5 Impact of Supply Voltage on DA Performance

As the collector voltage has a direct impact on the electric field strength within the TIGBT during turn-off, the DA phenomenon is enhanced as supply voltage increases, as shown in Figure 7.13.

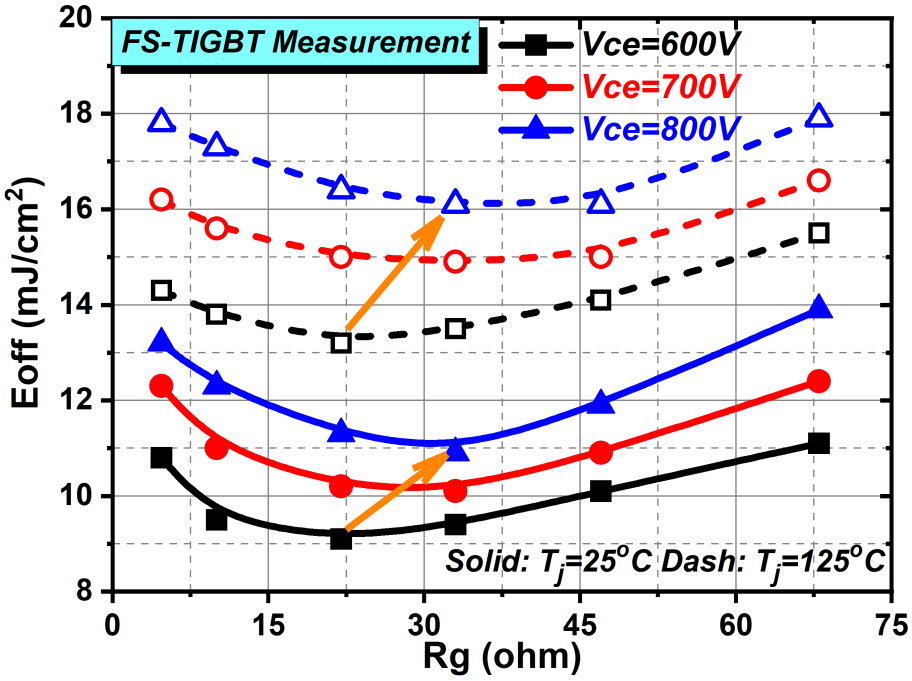


Figure 7.14 Impact of supply voltage on the E_{off} of TIGBT.

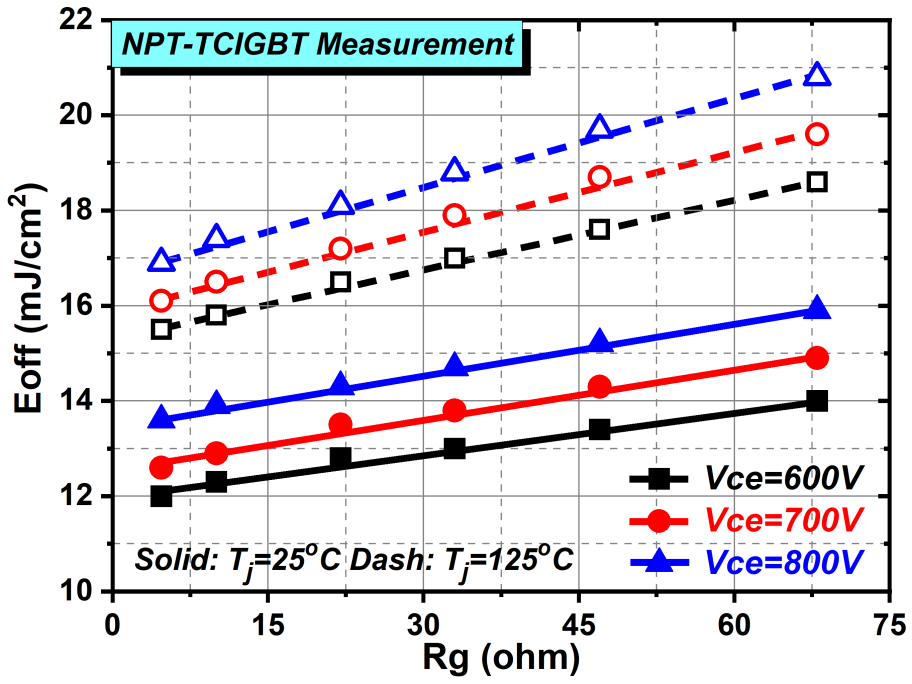


Figure 7.15 Impact of supply voltage on the E_{off} of TCIGBT.

The measured E_{off} of the TIGBT as a function of R_g at various supply voltages is shown in Figure 7.14. Note that the minimum E_{off} at V_{ce} = 800 V appears at a larger R_g in comparison to the case of V_{ce} = 600 V, which confirms that higher supply voltage enhances the DA performance of TIGBTs. In contrast, the supply voltage has no impact on the DA free performance of TCIGBT, as shown in Figure 7.15.

7.6 Impact of 3D Scaling Rules on DA Performance

To understand the impact of the 3D scaling rules on the DA performance of the devices, scaled TIGBTs [29] as well as scaled TCIGBTs in FS technologies are considered, as shown in Figure 7.16 and Figure 7.17, respectively.

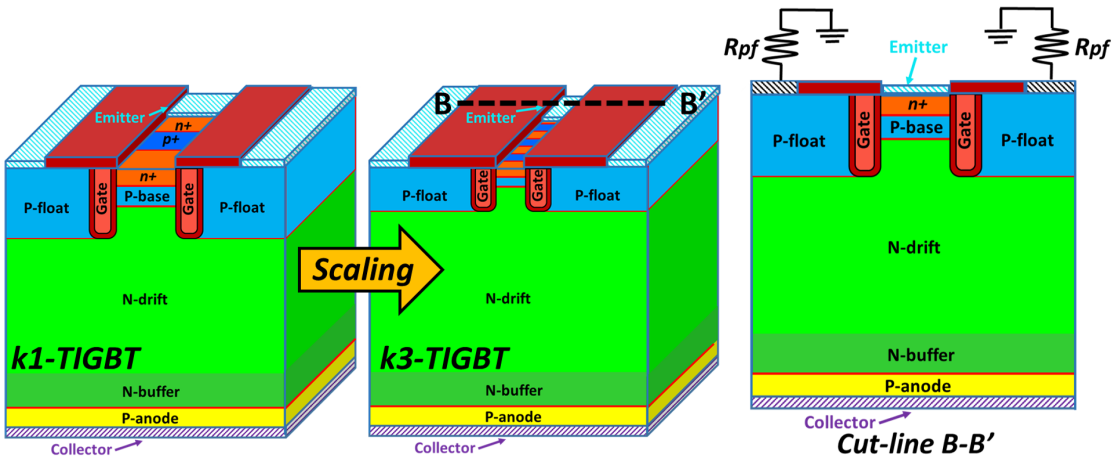


Figure 7.16 3-D scaling rules of TIGBT.

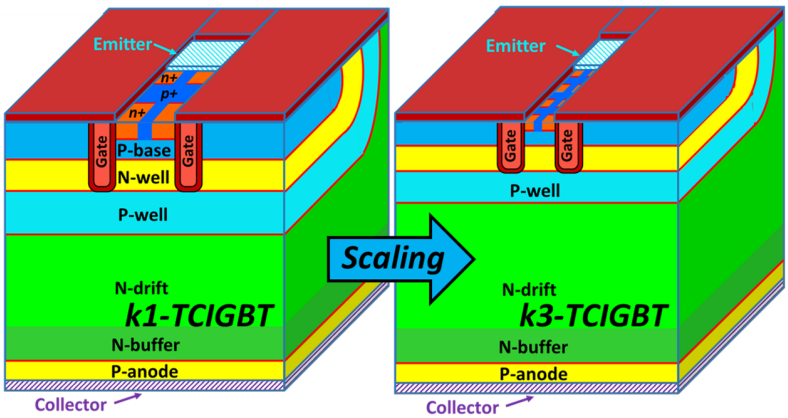


Figure 7.17 3-D scaling rules of TCIGBT.

The structures were evaluated through 3D modelling with models calibrated against measured data, as shown in Figure 7.18. Note that the device thickness in all structures are identical as in [29] in order to compare the electrical characteristics.

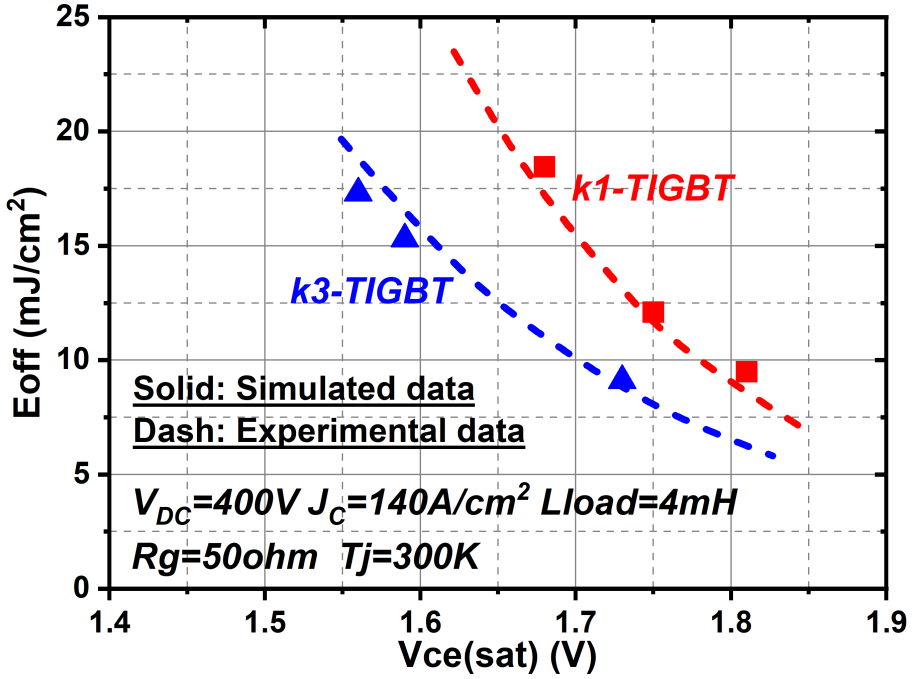


Figure 7.18 Calibration of simulated models with experimental data in [29].

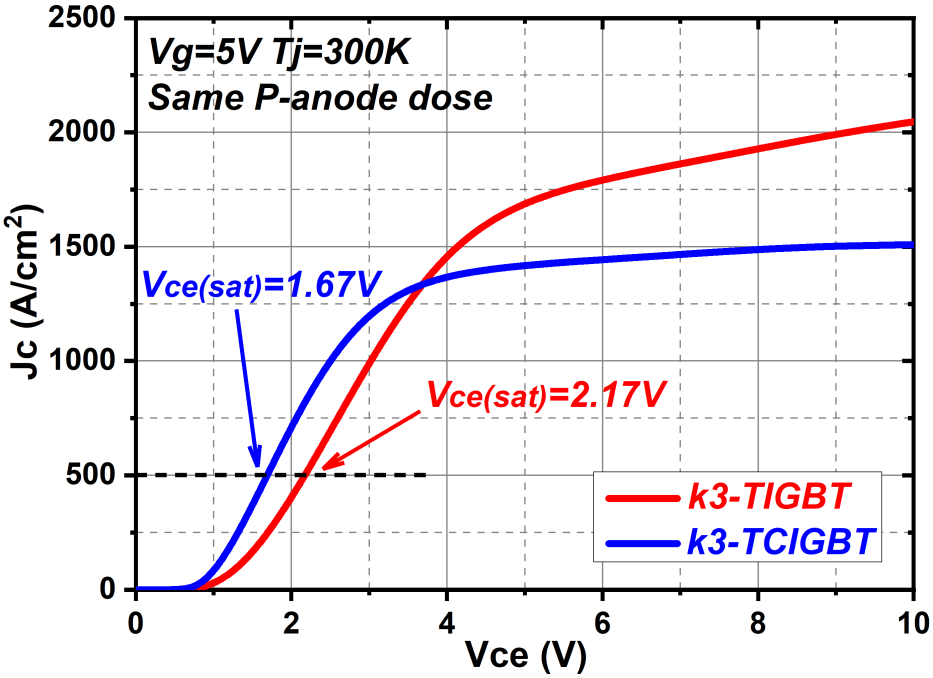


Figure 7.19 Comparison of I-V curves between k3-TIGBT and k3-TCIGBT.

Figure 7.19 compares the *I-V* curves of *k*3-TIGBT and *k*3-TCIGBT under identical threshold voltage and same P-anode conditions. The *k*3-TCIGBT yields a low $V_{ce(sat)}$ of 1.67 V even at J_c = 500 A/cm² at R.T., which is 23 % lower than that of *k*3-TIGBT. Furthermore, the non-saturated *I-V* behavior of narrow mesa TIGBTs is effectively suppressed in *k*3-TCIGBT due to enhanced self-clamping feature.

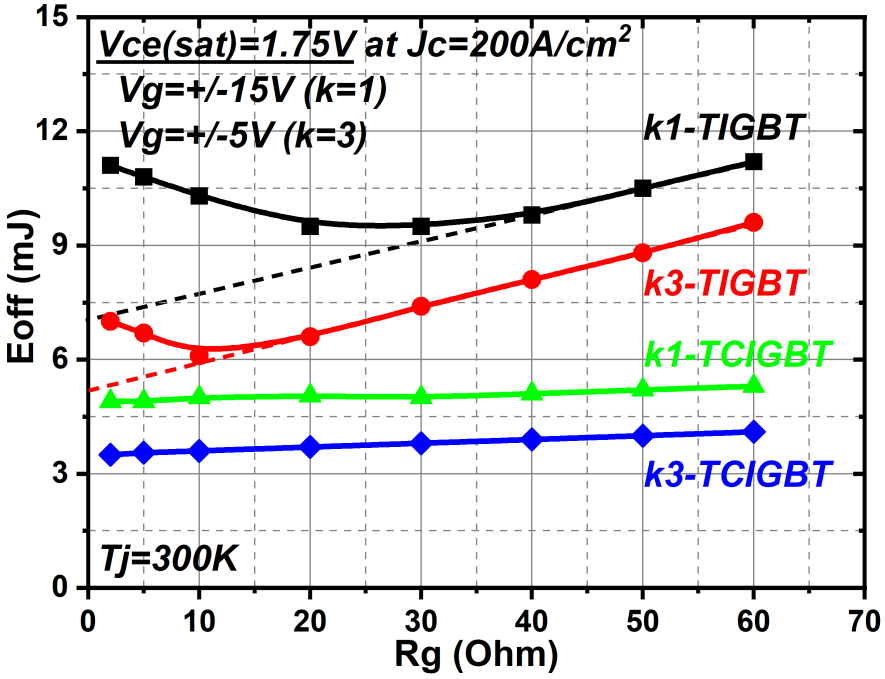


Figure 7.20 Impact of E_{off} versus R_g with scaling in TIGBTs and TCIGBTs under same $V_{ce(sat)}$ condition.

The E_{off} dependence on R_g between scaled TIGBTs and TCIGBTs were compared under same $V_{ce(sat)}$ conditions, as shown in Figure 7.20, which is achieved by adjusting P-anode concentration. The low switching losses of both devices decrease as a function of scaling rule. Moreover, the lower losses of *k*3-TCIGBT is clear as shown in Figure 7.20. Note that *k*3-TCIGBT remains DA free performance even at J_c = 500 A/cm², as shown in Figure 7.21.

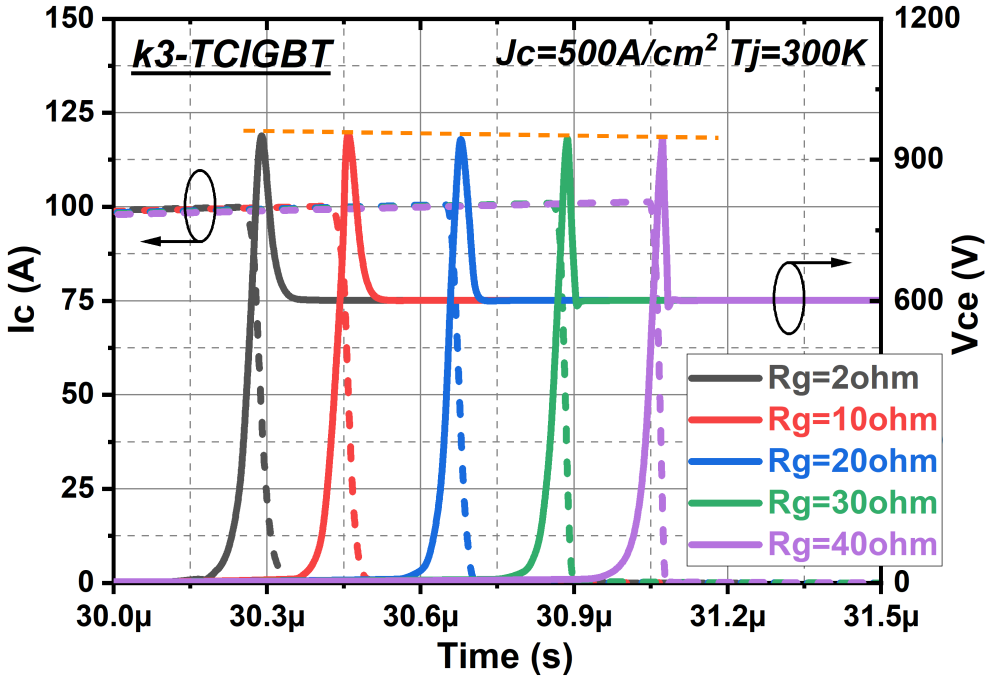


Figure 7.21 Simulated switch-off waveforms of *k3*-TCIGBT at J_c = 500 A/cm².

However, in the TIGBT, 3D-scaling rule does not suppress DA, because enhanced IE effect influences are stronger than relaxation of electric field concentration. Figure 7.22 shows the comparison of electric field distributions, I.I. rates and hole densities when V_{ce} raises to 600 V between *k1*-TIGBT and *k3*-TIGBT. As shown, the maximum electric field strength and maximum I.I. rate of *k3*-TIGBT are not reduced compared to that of *k1*-TIGBT. Therefore, scaling down the cathode cells of TIGBTs cannot suppress DA. However, as shown in Figure 7.20, *k3*-TIGBT does not show any obvious increase in E_{off} at small gate resistances, which is due to fast hole evacuation by shallow trench. In any case, care must be taken to address reliability concerns with thinner gate oxides in scaled TIGBTs.

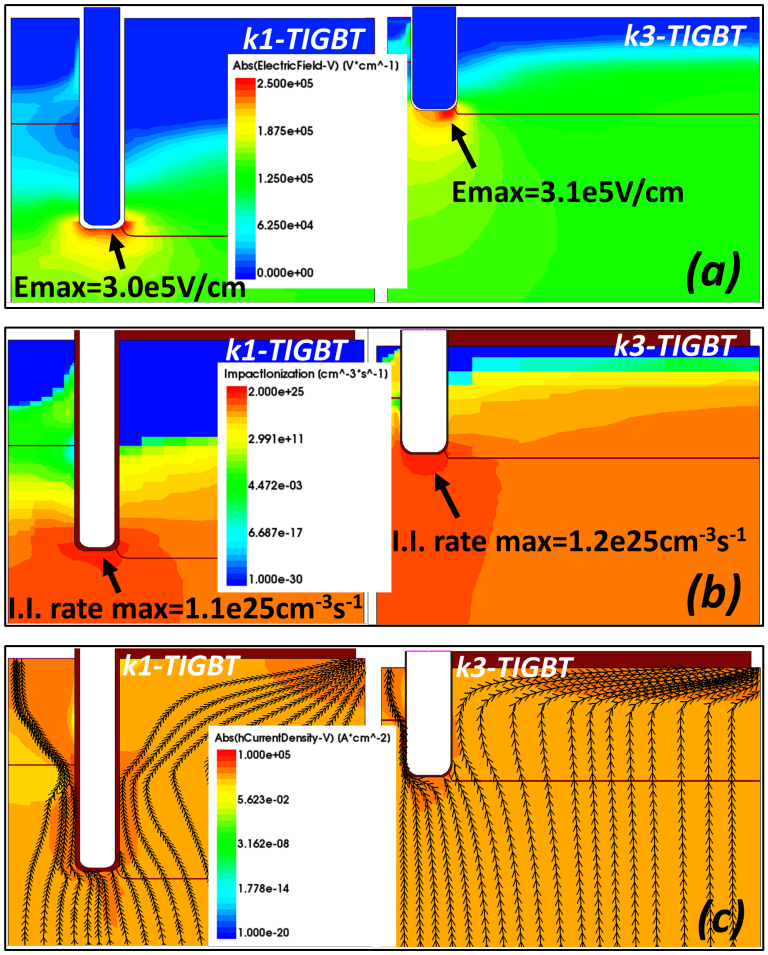


Figure 7.22 Comparison of (a) electric field distributions, (b) I.I. rates and (c) hole densities when V_{ce} raises to 600 V between *k1*-TIGBT and *k3*-TIGBT. (R_g = 20 Ω)

The impact of the on-state carrier profile on DA in *k3*-TIGBT is analyzed by changing the resistance R_{pf} between the p-float region and the emitter, as shown in Figure 7.23(a). The carrier concentration at the emitter-side can be increased with high R_{pf} due to IE effect. The rate of change of voltage (dV/dt) is increased with decrease in R_{pf} (Figure 7.23(b)). Both I.I. rates and E_{max} are enhanced by the positive charge of excess holes around the trench gate bottom (Figure 7.23(c)). Most importantly, these results shown in Figure 7.23 demonstrate that diversion of holes away from the trench bottom alone does not suppress DA. In Figure 7.24(a), (b) and (c) are shown some analysis of DA due to the increase in carrier concentration at the collector-side. Although the turn-off time can be increased by increasing P-anode concentration (Figure 7.24(b)), the collector-side carrier concentration has no influence on the DA performance of *k3*-TIGBT (Figure 7.24(c)).

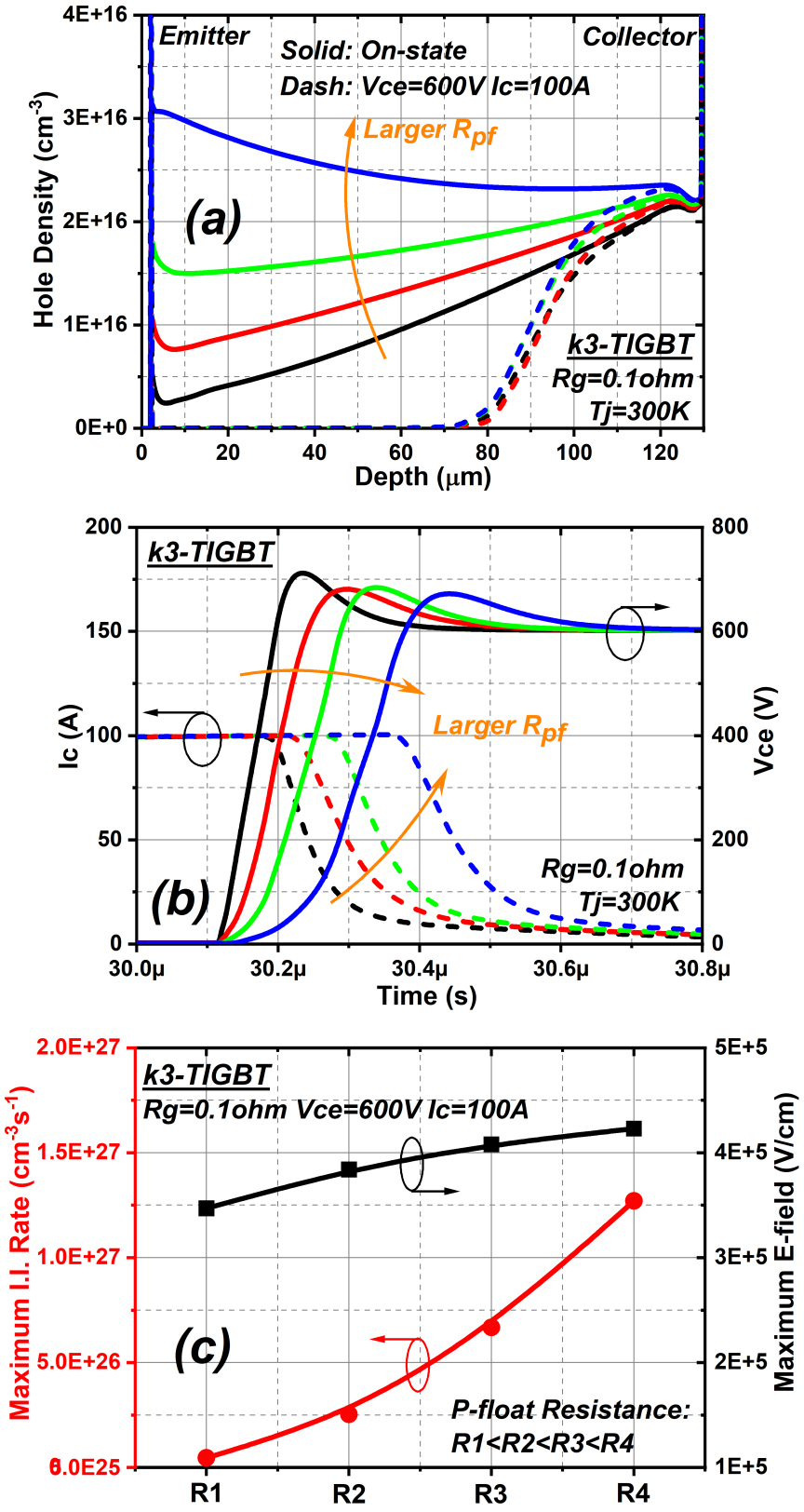


Figure 7.23 Influence of R_{pf} on (a) on-state hole density and excess hole density when V_{ce} raises to 600 V, (b) switch-off characteristics, and (c) maximum electric field and maximum I.I. rate when V_{ce} raises to 600 V in the case of *k3*-TIGBT. (V_g = +/- 5 V)

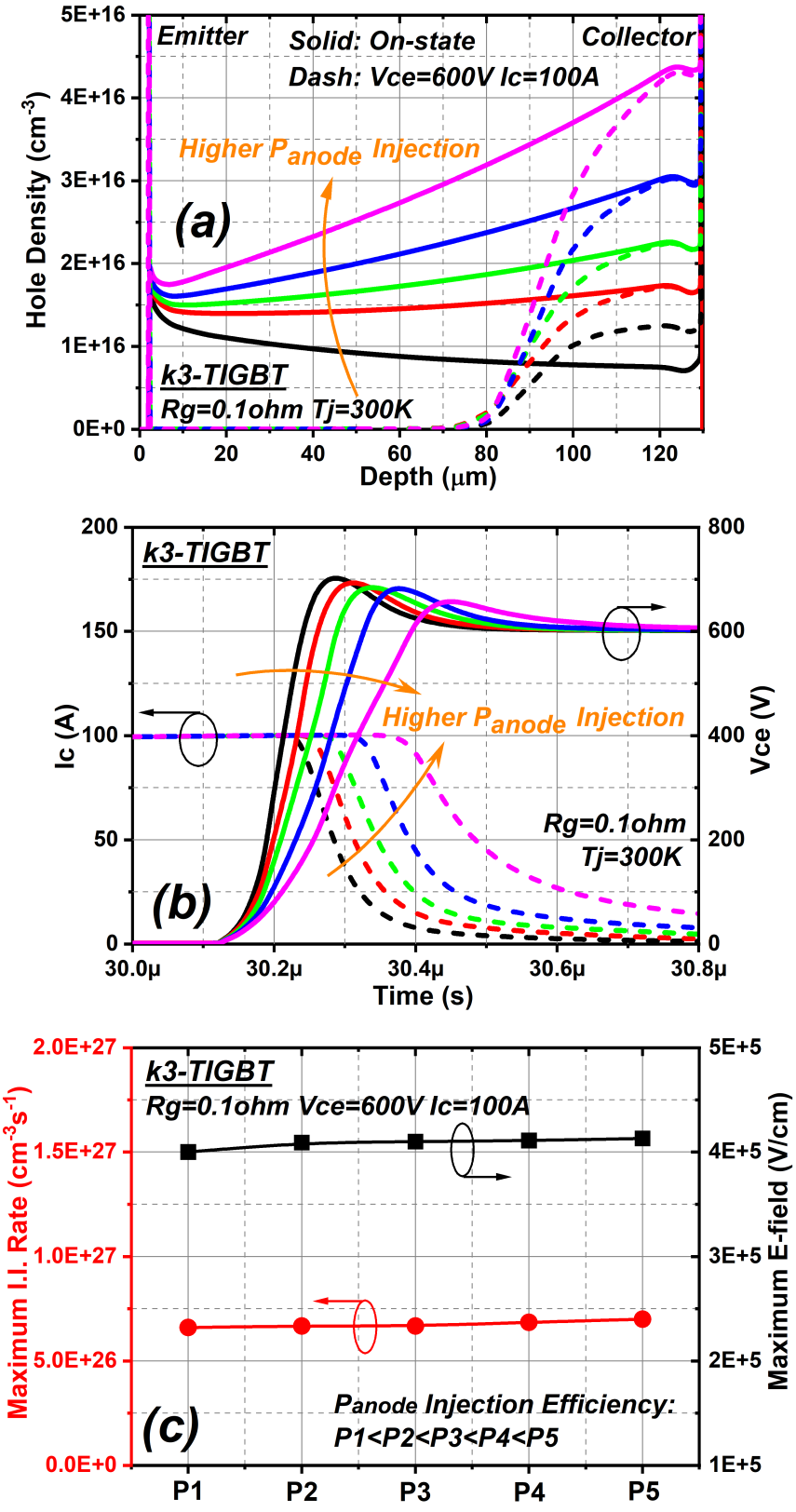


Figure 7.24 Influence of anode injection efficiency on (a) on-state hole density and excess hole density when V_{ce} raises to 600 V, (b) switch-off characteristics, and (c) maximum electric field and maximum I.I. rate when V_{ce} raises to 600 V in the case of *k3*-TIGBT. (V_g = +/-5 V)

7.7 Summary

The 1.2 kV Trench IGBT (TIGBT) switching behavior focusing on the DA was analyzed through calibrated 3D TCAD models. Management of the electric field concentration beneath trench gates is the most critical way to minimize the DA. In addition, a DA free turn-off operation is demonstrated in a Trench Clustered IGBT (TCIGBT), through in both simulations and experiments. As a MOS controlled thyristor device, TCIGBT can be operated with very low power losses at high current densities without DA and associated reliability concerns. This is because of the its PMOS action, which eliminates electric field crowding at trench bottom during turn-off transients. Moreover, experimental results confirm that DA is enhanced at high current densities and high supply voltages and results in significant increase in E_{off} in the TIGBTs. In comparison, TCIGBTs remain DA free performance at high current density operations and high supply voltage conditions. Low turn-off energy loss can be easily achieved by reducing gate resistance. Finally, the impact of device scaling design on the DA has also been analyzed with calibrated models.

Chapter 8 TURN-OFF DV/DT CONTROLLABILITY OF MOS-GATED BIPOLAR DEVICES

Turn-off dV/dt controllability is an essential feature in IGBTs for flexible design in power switching applications. However, the occurrence of Dynamic Avalanche (DA) during the turn-off transients plays a key role on the turn-off power loss, dV/dt controllability and safe operating area of IGBTs. This chapter is aimed to clarify the impact of DA on the turn-off characteristics of 1.2 kV trench IGBTs through 3-D TCAD simulations as well as experimental demonstrations. Measurement results show that DA is enhanced at high current density and high supply voltage conditions, which aggravates its influence on the dV/dt controllability as well as turn-off power loss. In order to eliminate the DA for high current density and low loss operations, a DA free design has been experimentally demonstrated in the Trench Clustered IGBT (TCIGBT) in previous chapter. Due to effective management of electric field and unique PMOS actions during turn-off, TCIGBT can retain high dV/dt controllability and low power loss at high current density operations.

8.1 Introduction

In comparison to the conventional planar IGBTs, Trench-gated IGBTs (TIGBTs) with blocking voltages from 600 V up to 6.5 kV have achieved significant improvements in the switching loss (E_{off}) and on-state voltage drop ($V_{ce(sat)}$) trade-off due to higher channel density and Injection Enhancement (IE) effect [17, 142-144]. The remarkable progress in E_{off}-$V_{ce(sat)}$ trade-off have resulted in not only higher energy efficiency but also increase in power density and cost reduction of IGBT modules. In order to increase the switching frequency of IGBT modules, high switching slopes (high dV/dt and dI/dt) are required to minimize the switching losses and delay time. However, high dV/dt can induce Electro-Magnetic Interference (EMI) noise in the electric systems due to parasitic components. Therefore, high levels of dV/dt controllability

are required to meet power efficiency and EMI noise requirements in power electronic systems. Recently, it was found that high current densities and high dV/dt can induce Dynamic Avalanche (DA) during switching, which can lead to current filamentations [43, 71, 138, 140]. The resulting excessive carriers have a significant impact on the switching slopes, power losses as well as gate stability. Since the development of TIGBTs is aimed at applications demanding ever so increasing power density, switching frequency as well as long-term reliability, the DA phenomena must be eliminated to meet these requirements. Several approaches such as deep P-float [45] and emitter gate with additional P-layer [43] have been reported to suppress but not eliminate DA in the TIGBTs. More recently, a DA free design has been experimentally demonstrated in the Trench Clustered IGBT (TCIGBT) [145]. Due to self-clamping feature and PMOS actions, the TCIGBT shows DA free performance with low power losses. Moreover, in comparison to the TIGBT, high dV/dt controllability can be maintained by TCIGBT at high operating current densities [146].

In this chapter, the turn-off behavior of TIGBTs considering DA effect is explained through theoretical analysis and 3D TCAD simulations. 3D Sentaurus Device [67] within Synopsys is utilized to simulate the switching characteristics. Moreover, the turn-off transient of TCIGBT is studied in detail to explain its high dV/dt controllability. Finally, for the first time, the influence of current density and supply voltage on the turn-off dV/dt controllability of TIGBTs is investigated through experiments.

8.2 dV/dt Limitation by Dynamic Avalanche in TIGBTs

8.2.1 Analysis of DA in the turn-off of TIGBTs

Figure 8.1 shows the simulated turn-off characteristics of a TIGBT and the circuit configuration is specified in Figure 8.2.

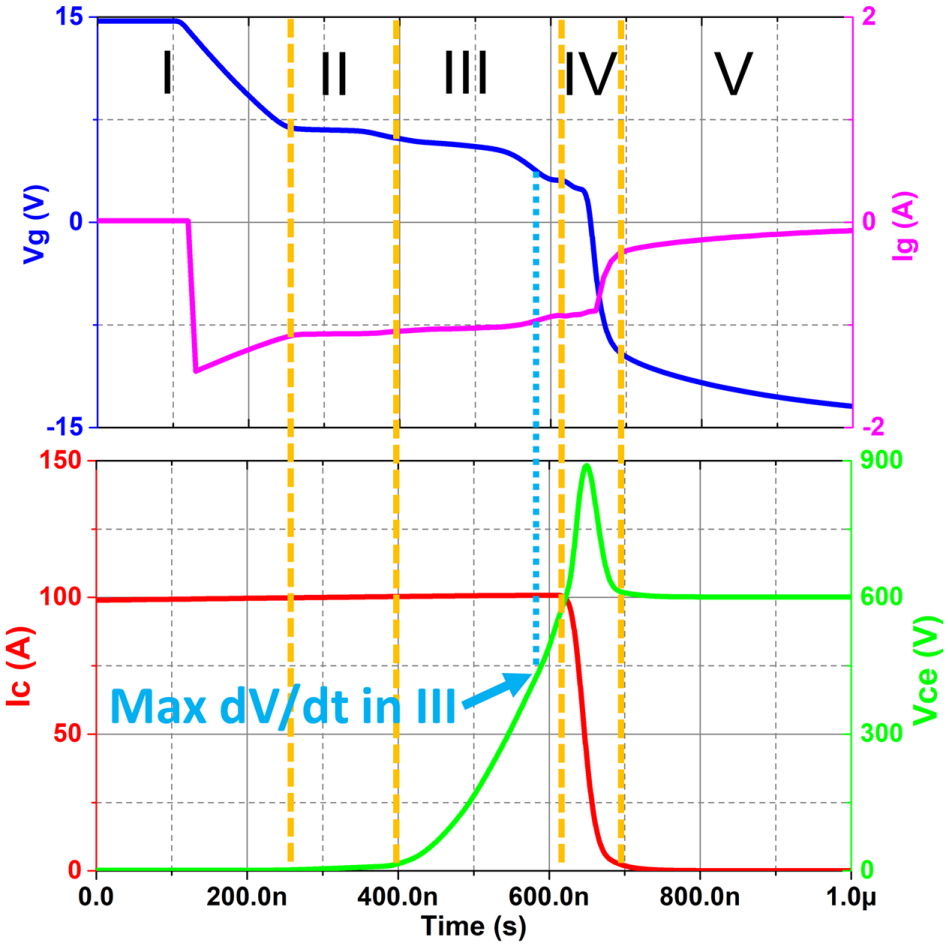


Figure 8.1 Turn-off characteristics of a TIGBT. (R_g = 20 Ω)

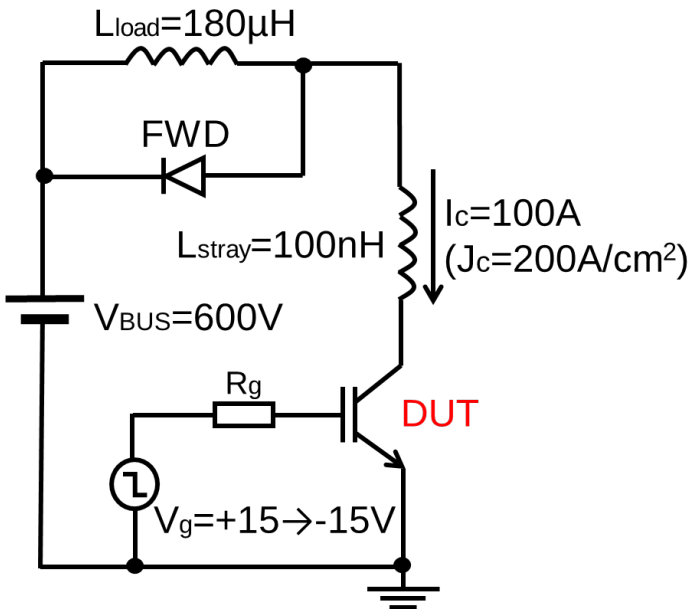


Figure 8.2 Test circuit configuration.

The detailed turn-off transient can be explained as follows:

Phase I: At the beginning of turn-off, the gate voltage (V_g) falls exponentially with time. The gate current (I_g) flows along the gate resistance (R_g) and discharges the gate-emitter capacitance (C_{ge}). The turn-off delay time in this phase is:

$$t_{d\_off} = R_g \times C_{ies} \times \ln\left(\frac{V_g}{V_{th} + I_c/g_m}\right) \tag{8.1}$$

where C_{ies} is the input capacitance, V_{th} is the threshold voltage, and g_m is the transconductance of the IGBT. As shown, larger R_g results in longer delay time.

Phase II: After V_g falls to the level required to maintain the collector current (I_c) at the load current level, the V_g remains constant and the I_g discharges the gate-collector capacitance (C_{gc}).

$$I_g = \frac{V_{th} + I_c/g_m}{R_g} \tag{8.2}$$

Phase III: The collector-emitter voltage (V_{ce}) start to rise up at a rate of

$$\frac{dV_{ce}}{dt} = \frac{I_g}{C_{GC}} = \frac{V_{th} + I_c/g_m}{R_g \times C_{GC}}. \tag{8.3}$$

As expressed, the dV/dt rate can be simply controlled by the R_g. The depletion region within the TIGBT expands as V_{ce} increases and the stored excessive carriers are swept out by the internal electric field. Moreover, the C_{gc} decreases due to the extension of depletion region and results in an increase in dV/dt. The maximum dV/dt appears at the point when V_g and I_g start to show a slight decrease at the end of this phase. The decrease in I_g is due to the consumption in the discharging of C_{ge} [147].

Phase IV: After V_{ce} increases to the supply voltage (V_{bus}), the Free-Wheeling Diode (FWD) turns on and the load current starts to divert from TIGBT to FWD. Therefore,

the I_c decreases immediately and induces a surge voltage (V_{surge}) due to stray inductance (L_{stray}) in the circuit.

$$V_{surge} = L_{stray} \times \frac{dI_c}{dt} \tag{8.4}$$

If the L_{stray} is not low enough, it will result in a high dV/dt which may be even higher than that of Phase III.

Phase V: As the MOSFET structure has turned off and most of the excessive carriers have been swept out, the tail current is mainly contributed by the recombination current.

In Phases IV and V, the expanding depletion boundary is obstructed by the stored on-state carriers as depicted in Figure 8.3. DA will take place if the resulting electric field (E_{max}) exceeds the critical electric field (E_{cr}), which can occur even at a voltage well below the static breakdown voltage. The detailed schematic of DA in the turn-off transient of trench gated IGBTs has been explained in previous chapter. The occurrence of DA results in additional excess carriers within the device, which slows down the discharging of C_{gc} (expansion of depletion region) and affects the dV/dt.

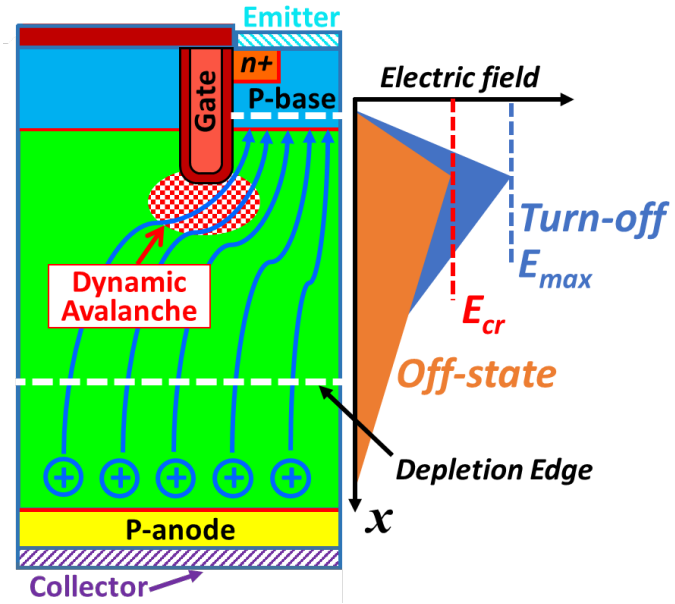


Figure 8.3 Schematic of DA during turn-off of TIGBT.

8.2.2 Influence of DA on the dV/dt Controllability

Figure 8.4 shows the simulated turn-off waveforms of a 1.2 kV TIGBT in Field-Stop (FS) technology. In practice, smaller R_g should induce larger dV/dt. However, the DA decreases the V_{surge} as well as the dV/dt at small R_g conditions, as shown in Figure 8.5.

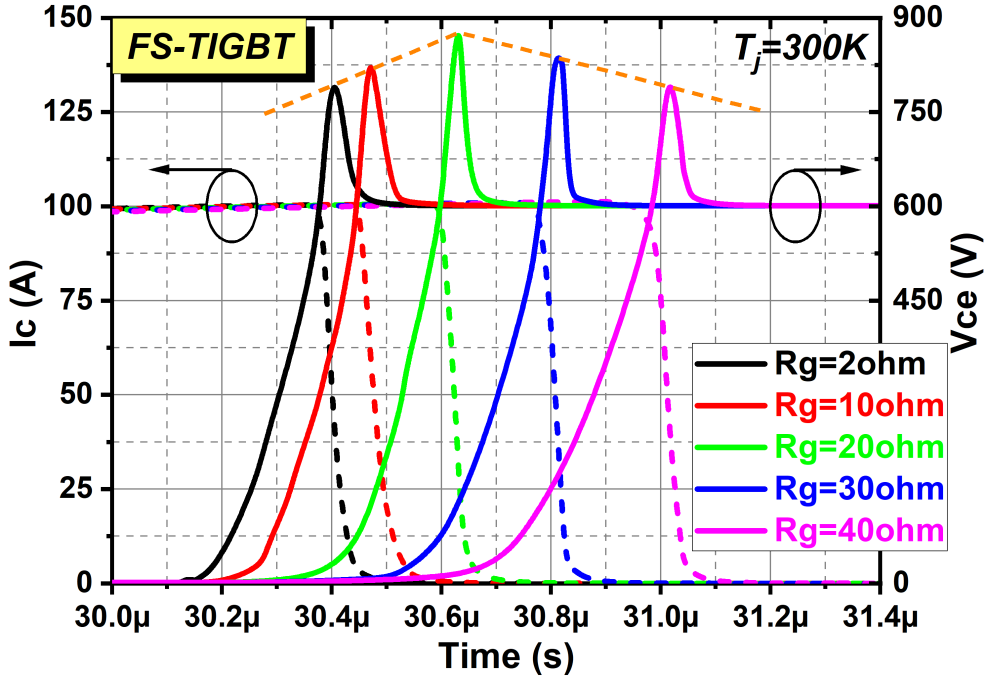


Figure 8.4 Influence of R_g on switch-off characteristics of a conventional TIGBT.

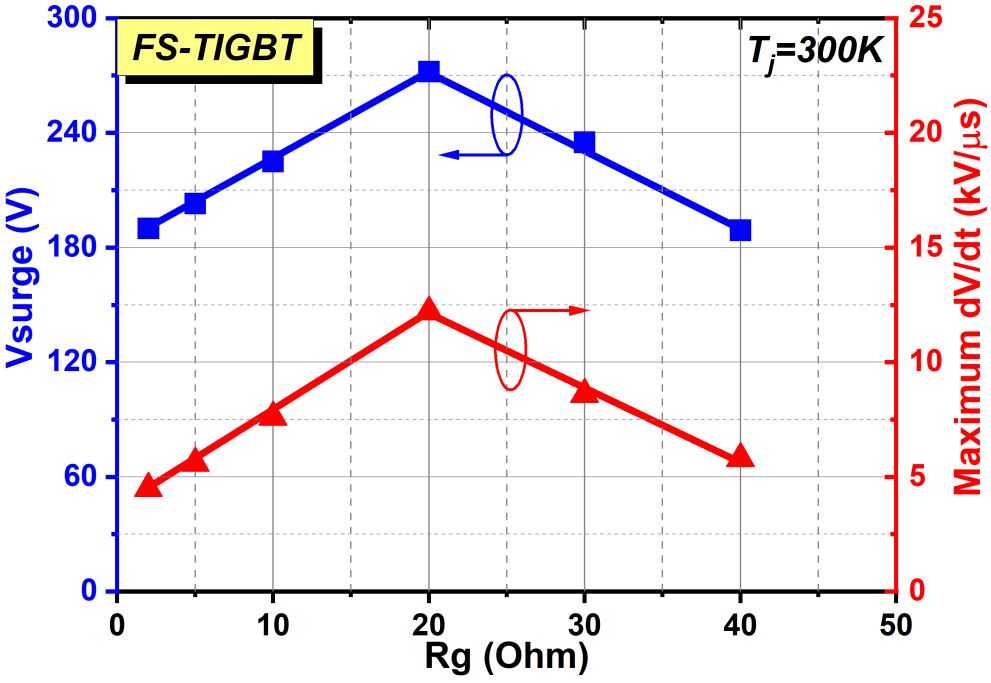


Figure 8.5 Influence of R_g on surge voltage (V_{surge}) and maximum dV/dt of a conventional TIGBT

This clearly indicates that DA occurs in the cases of R_g < 20 Ω and that the dV/dt is limited by DA. Therefore, in order to meet the development of TIGBTs to satisfy various power applications, DA must be eliminated to achieve high dV/dt controllability and high switching frequency.

8.3 DA Free Solution – High dV/dt Controllability by TCIGBT

As a fundamental solution towards the DA elimination, TCIGBT is attractive because of its design for electric field management and unique PMOS actions [145]. Figure 8.6 shows the 3D cross-sectional view of the TCIGBT. During turn-off transient, due to the internal self-clamping feature of the TCIGBT, the N-well layer is punched through at a collector voltage of less than 20 V and the further increase in collector voltage is supported by the P-well/N-drift junction. Thus, the maximum electric field is shifted away from the trench regions. This results in effective control of the DA and dV/dt as depicted in Figure 8.7. Note that the turn-off dV/dt of TCIGBT can be easily controlled by adjusting the P-anode dose without the occurrence of DA.

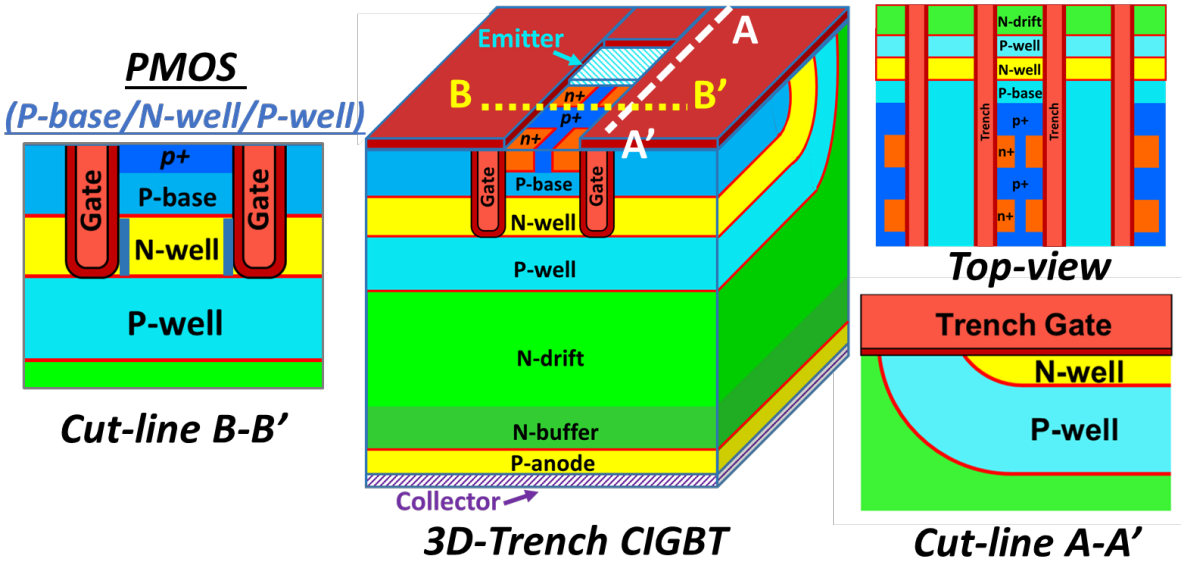


Figure 8.6 3-D cross-sectional view of TCIGBT.

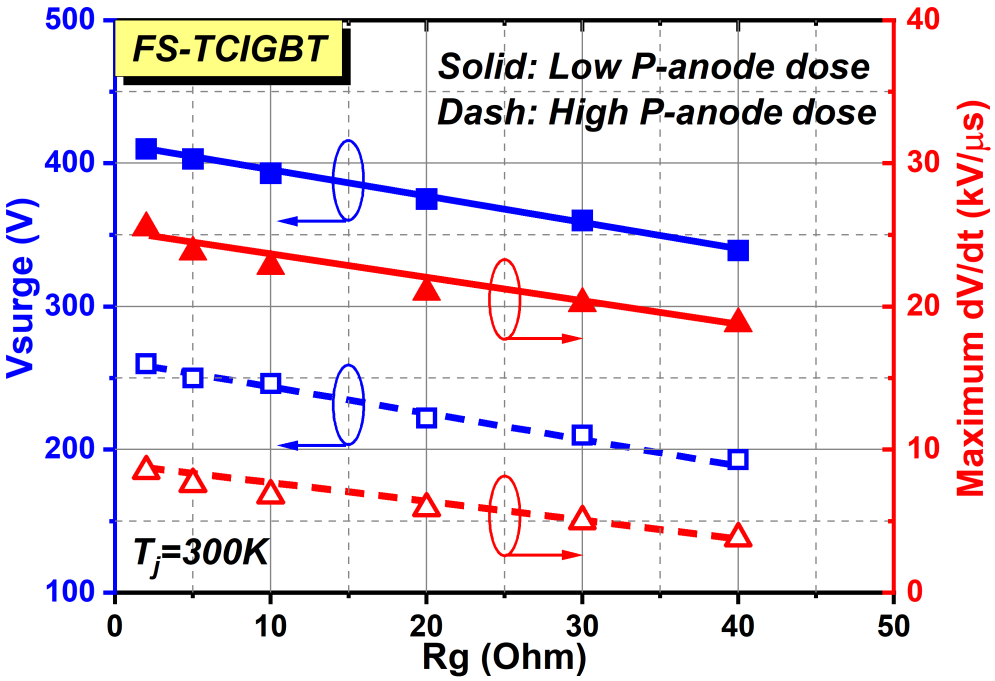


Figure 8.7 V_{surge} **and maximum dV/dt during turn-off of the TCIGBT.**

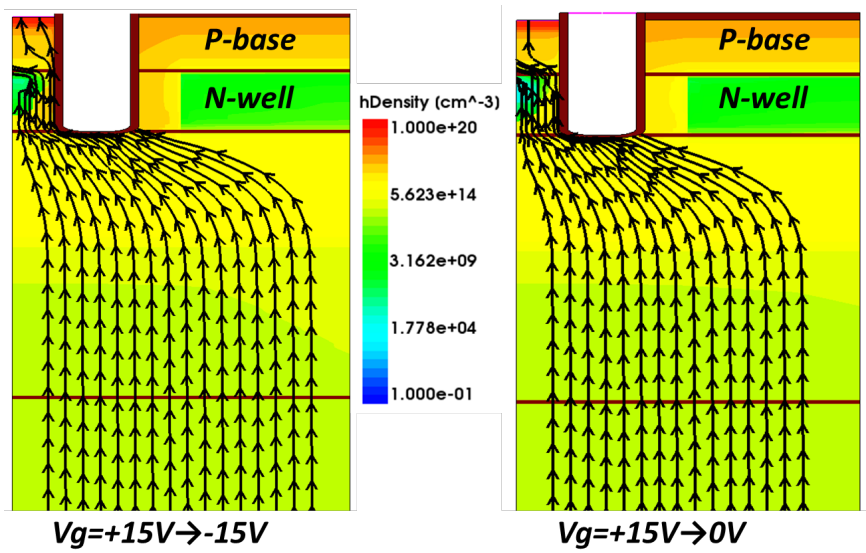


Figure 8.8 Comparison of hole current flowlines at various off-state gate voltages when V_{ce} **raises to 600V during turn-off of the TCIGBT.**

Figure 8.8 shows the hole current flowlines within the TCIGBT during turn-off. When the collector potential increases to a value beyond the self-clamping voltage, the N-well layer is fully depleted and the PMOS structure which consists of P-well, N-well and P-base turns on without the necessity of channels. Therefore, the off-state gate

bias (0 V or -15 V) has no influence on the turn-off behavior of TCIGBT. Moreover, the turn-on of PMOS structure provides a direct evacuation path for excessive holes to be swept out. The E_{off} is therefore significantly reduced compared to that of a TIGBT.

High dV/dt controllability of TCIGBT with DA free performance is confirmed from the measurement results of the maximum dV/dt as a function of R_g of a 1.2 kV TCIGBT device [56] as shown in Figure 8.9. The dV/dt can be controlled even at low R_g conditions. The demonstrated devices were made in Non Punch-Through (NPT) technology. Since the DA is determined by the cathode structure design, moving from NPT technology to a thinner FS technology for improving E_{off}-$V_{ce(sat)}$ trade-off has no impact on the DA performance.

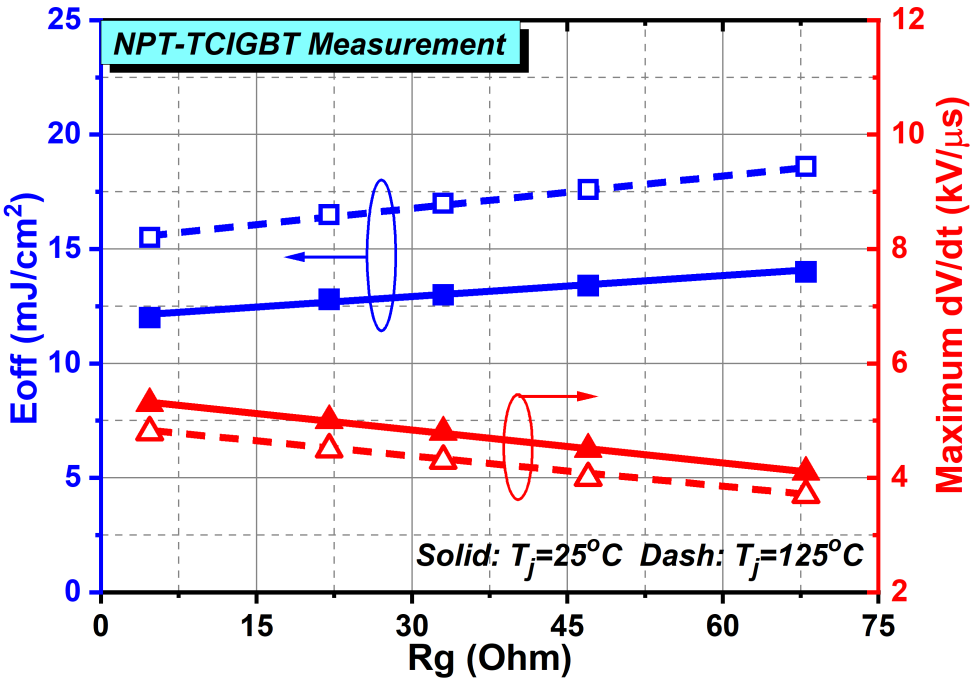


Figure 8.9 Experimental results of E_{off} and maximum dV/dt during turn-off as a function R_g of the TCIGBT.

8.4 Impact of Stray Inductance on dV/dt Controllability

High L_{stray} can induce a high surge voltage as well as a high dV/dt during device turn-off, as expressed in Equation (8.4). Therefore, the L_{stray} has a significant impact on the turn-off dV/dt controllability. Figure 8.10 and Figure 8.11 show the simulation results

of the influence of L_{stray} on the maximum dV/dt of TIGBT and TCIGBT, respectively. As shown, higher L_{stray} results in a higher maximum dV/dt in both TIGBT and TCIGBT. However, in the TIGBT, the maximum dV/dt shows decreasing trends when R_g is reduced to less than 20 Ω. This is because DA occurs at small R_g conditions, resulting in excessive charge to lower dV/dt at various L_{stray} conditions. In contrast, the dV/dt shows linear increases as R_g reduces in TCIGBT due to DA free.

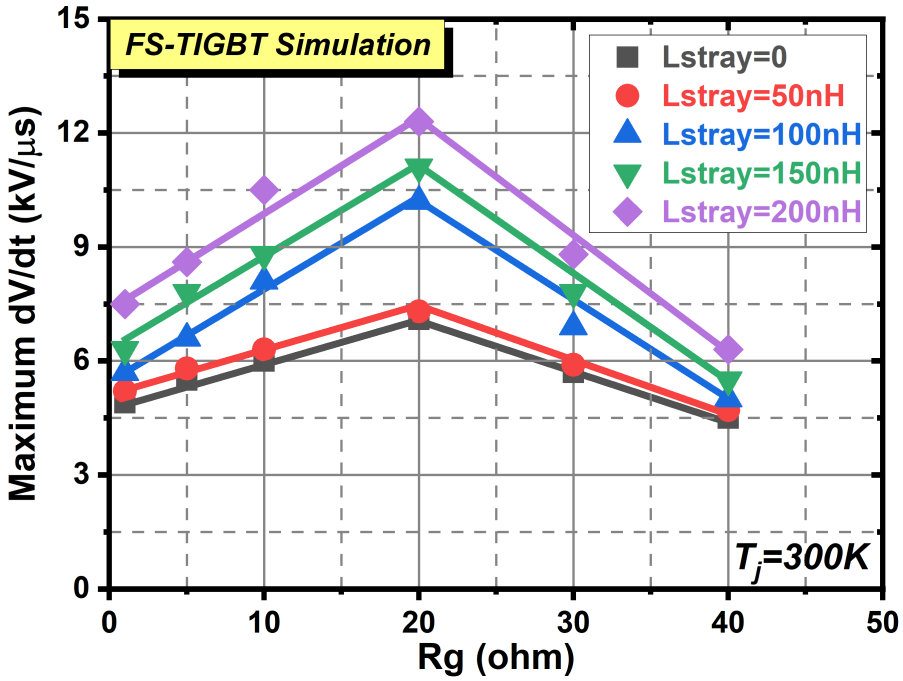


Figure 8.10 Impact of stray inductance on the maximum dV/dt during turn-off of TIGBT.

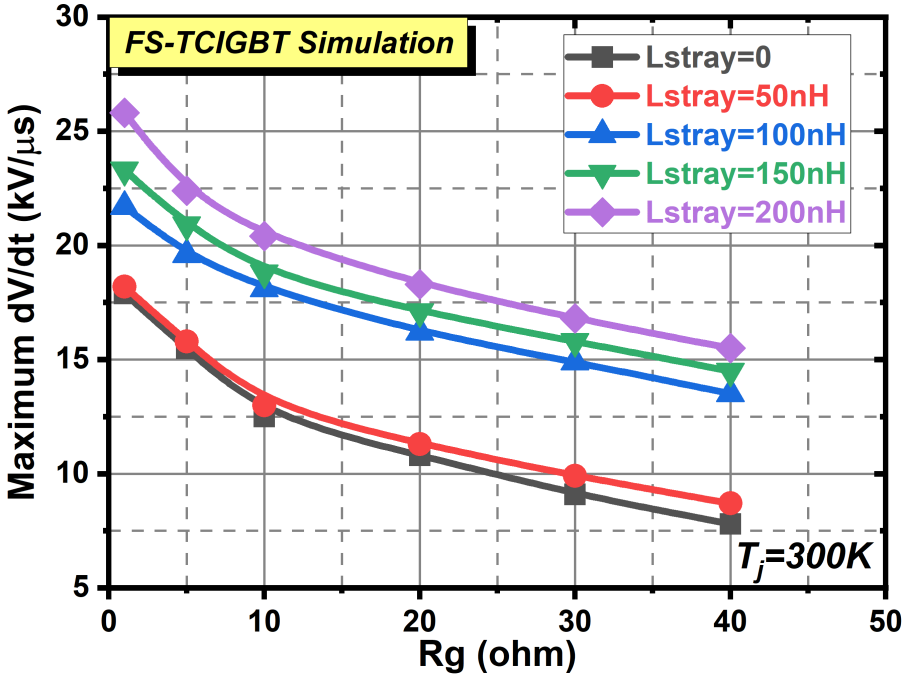


Figure 8.11 Impact of stray inductance on the maximum dV/dt during turn-off of TCIGBT.

8.5 Impact of Current Density on dV/dt Controllability

The development of IGBT modules have been devoted towards increasing power density to achieve cost reduction and flexible design for power converter systems. The requirement of higher power density is directly associated with increased operating current density with low power losses per chip area. Moreover, high dV/dt controllability at high operating current densities is also essential to satisfy various IGBT applications. In order to clarify the impact of DA on the dV/dt controllability of TIGBTs at high current densities, a 1.2 kV, 25 A TIGBT device in FS technology [141] was investigated in detail and compared with the experimental results of an NPT TCIGBT [56]. Figure 8.12 compares the measured on-state voltage drops between the FS-TIGBT and the NPT-TCIGBT at various current densities at 25 °C and 125 °C. At both rated current density (J_c = 140 A/cm²) and high current densities, due to thyristor conduction, the NPT TCIGBT (device thickness = 200 μm) shows much lower on-state voltage drops compared to that of FS TIGBT, which owns a much thinner device thickness of 115 μm.

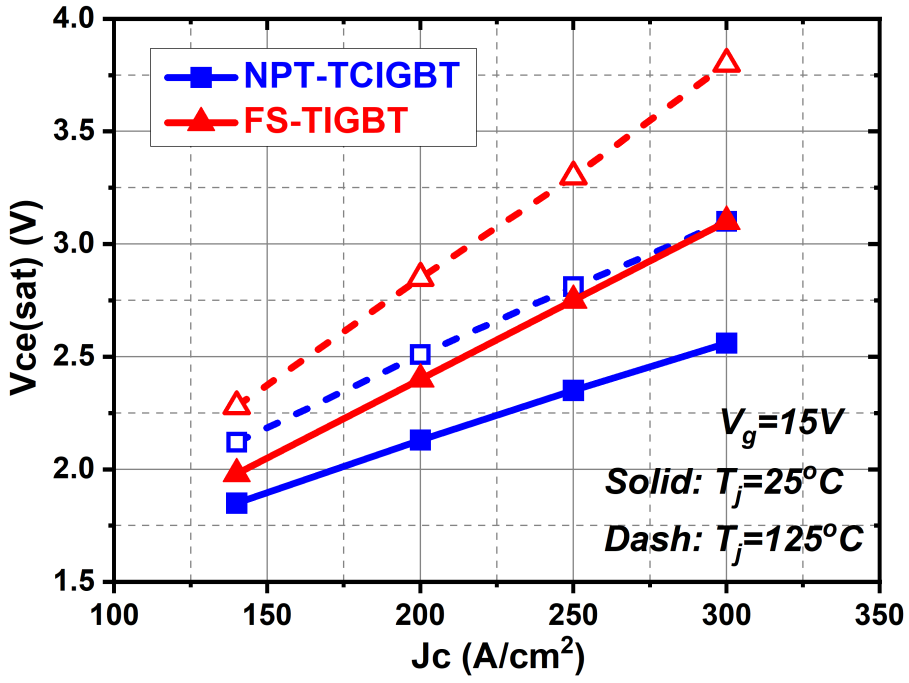


Figure 8.12 Experimental results of the on-state voltage drop as a function of current density of TIGBT and TCIGBT.

Figure 8.13 and Figure 8.14 show the turn-off waveforms as a function of R_g of TIGBT and TCIGBT at J_c = 300 A/cm², respectively. A decreasing trend of V_{surge} and a lower dI/dt at small R_g can be clearly observed from the case of TIGBT, which confirms the occurrence of DA. Since the surge voltage is largely independent of temperature [43], the temperature has no significant impact on the DA performance.

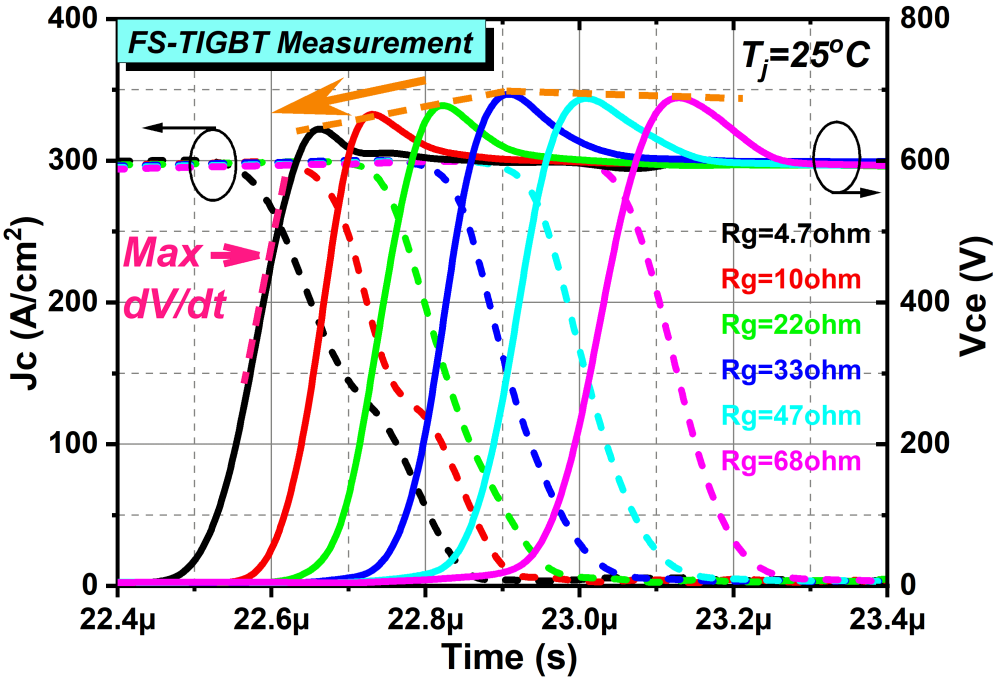


Figure 8.13 Measured switch-off waveforms as a function R_g of the TIGBT at J_c = 300 A/cm².

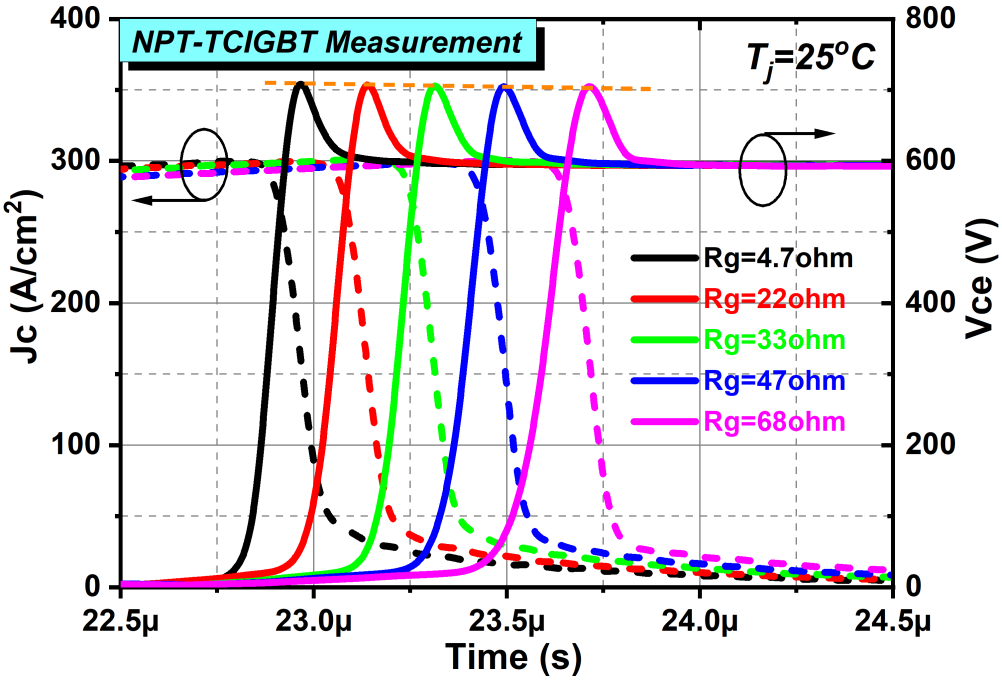


Figure 8.14 Measured switch-off waveforms as a function R_g of the TCIGBT at J_c = 300 A/cm².

Figure 8.15 and Figure 8.16 show the impact of current density on the maximum dV/dt of TIGBT and TCIGBT at T_j = 125 °C, respectively. As shown in Figure 8.16, absence of DA in TCIGBT is maintained at low as well as high current densities. This is because low electric field strength beneath trench gates and high carrier evacuation speed are maintained in both conditions. Therefore, high dV/dt controllability can be achieved by TCIGBT even at high current densities and low on-state losses conditions, which provides high design flexibility with ultra-high current density operation as well as low power losses for power electronics applications. However, it is clear evident from Figure 8.15 that the DA performance is enhanced at high current densities in TIGBT as the peak dV/dt value appears at a larger R_g at high current densities. Note that the maximum dV/dt shows an increase with the increase of current density in both TIGBT and TCIGBT, as shown in Figure 8.15 and Figure 8.16. This is because high operating current densities in the experiments are achieved by increasing load currents (I_c). Therefore, the dV/dt shows increases at high current densities due to larger I_g, as expressed in equation (8.3).

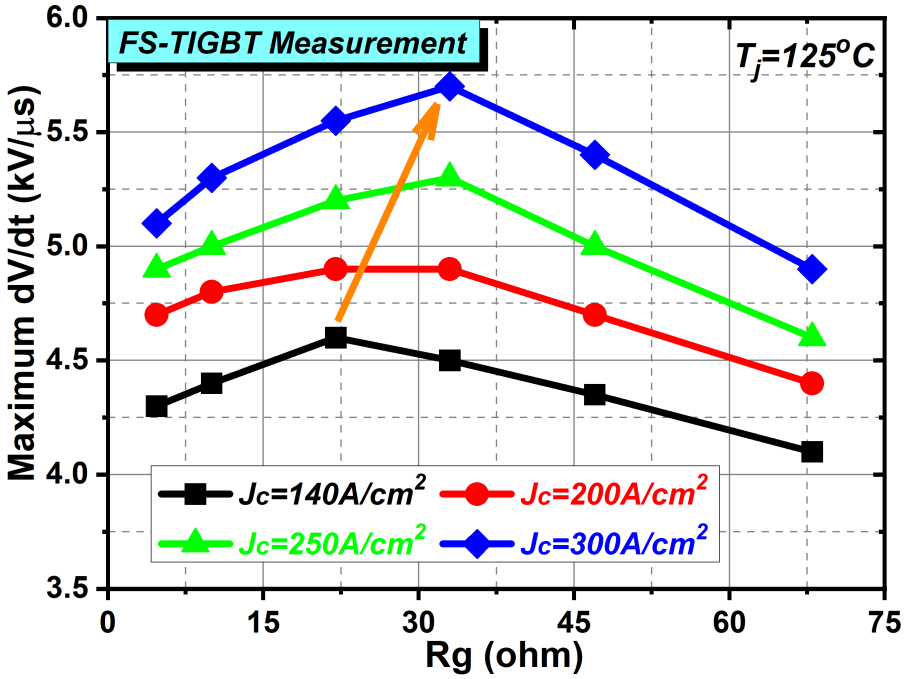


Figure 8.15 Impact of current density on the maximum dV/dt during turn-off of TIGBT.

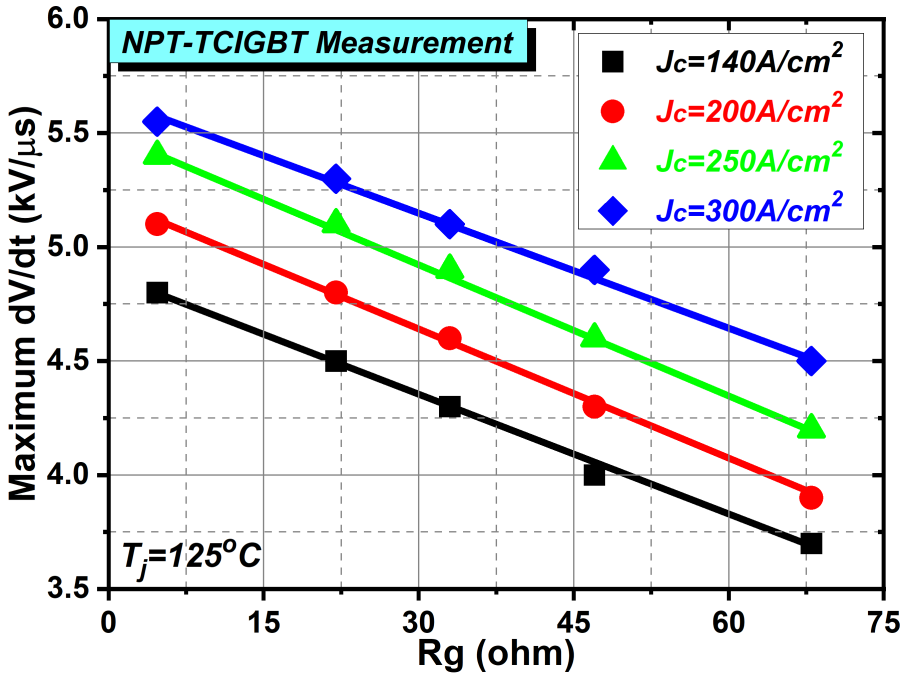


Figure 8.16 Impact of current density on the maximum dV/dt during turn-off of TCIGBT.

8.6 Impact of Supply Voltage on dV/dt Controllability

As the collector voltage has a direct impact on the electric field strength within the TIGBT during turn-off, the DA phenomenon is enhanced as supply voltage increases. Figure 8.17 shows the measured maximum dV/dt of the TIGBT as a function of R_g at various supply voltages. As shown, the peak dV/dt value at V_{ce} = 800 V appears at a larger R_g in comparison to the case of V_{ce} = 600 V, which confirms that higher supply voltage enhances the DA performance of TIGBTs. In contrast, the supply voltage has no impact on the high dV/dt controllability of TCIGBT, as shown in Figure 8.18.

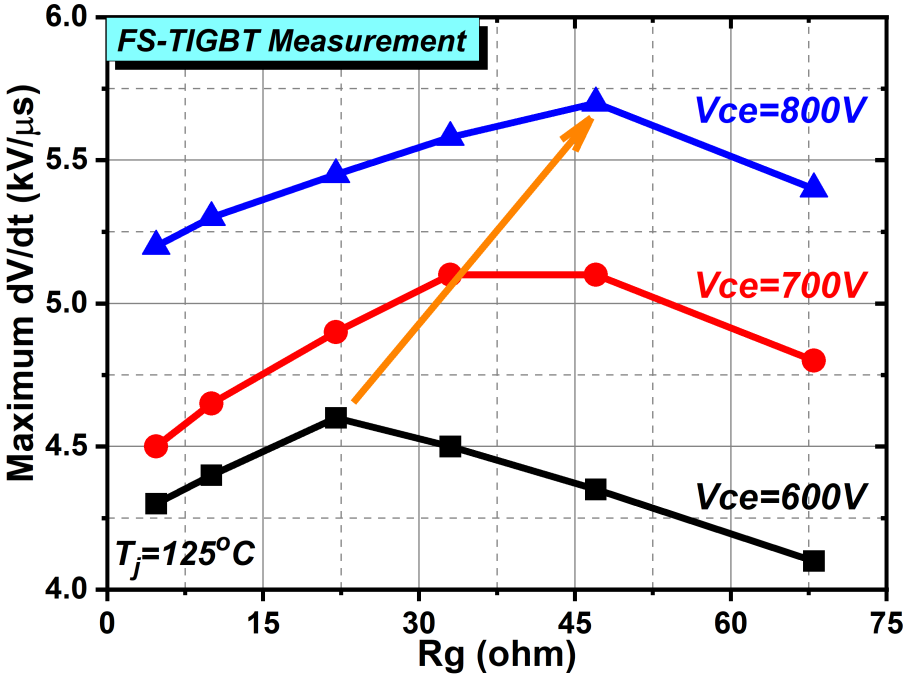


Figure 8.17 Impact of supply voltage on the maximum dV/dt during turn-off of TIGBT.

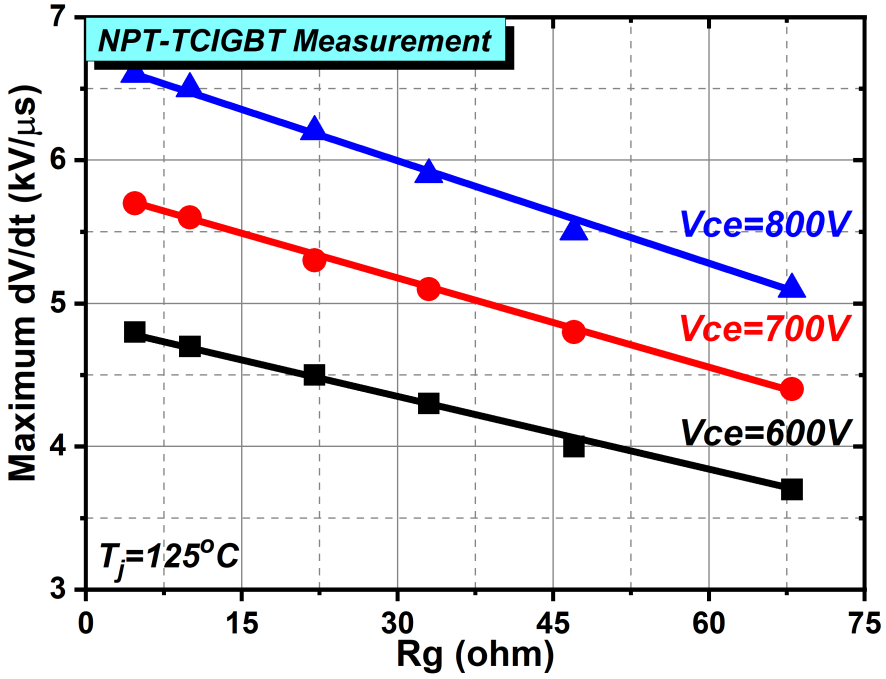


Figure 8.18 Impact of supply voltage on the maximum dV/dt during turn-off of TCIGBT.

8.7 Summary

Detailed analysis has been undertaken to explain the impact of DA effects on the switching behavior of the 1.2 kV trench IGBT. Both simulations and experimental

results confirm that DA poses fundamental limits on the reduction of switching losses as well as the dV/dt controllability of TIGBTs. In order to eliminate this phenomenon, a DA free turn-off operation is demonstrated in a TCIGBT through simulations and experiments. Absence of DA is clearly evident from the experimental results of the switching waveforms and maximum dV/dt of a TCIGBT device. Moreover, experimental results confirm that DA is enhanced at high current densities and high supply voltages, which further degrades the turn-off dV/dt controllability of TIGBTs. In contrast, TCIGBTs remain high dV/dt controllability even at high current density operations and high supply voltage conditions. Therefore, as a MOS controlled thyristor device, TCIGBT can be reliably operated with very low power losses at high current densities without DA and provides high design flexibility for power electronics systems as a result of high dV/dt controllability.

Chapter 9 CONCLUSIONS AND FUTURE WORK

9.1 Conclusions

To enhance the energy efficiency and reliability of power electronics, power semiconductor technologies must be continuously improved to achieve lower power dissipation and larger safe operating area. This thesis has demonstrated the modern optimisation technologies employed to improve the power losses of a MOS-gated thyristor device and the technological developments towards the future perspectives of IGBTs.

The 3-D scaling rules for medium voltage trench CIGBT and high voltage planar CIGBTs are proposed and investigated through TCAD simulations and calibrated models. Detailed simulation results show that the scaling rules result in significant improvement in on-state behavior and $V_{ce(sat)}$-E_{off} trade-off. Compared to the scaled 1.2 kV trench IGBT, the scaled TCIGBT shows an even lower $V_{ce(sat)}$ as well as current saturation behavior. Due to the enhanced self-clamping feature as a result of scaling rules, the short-circuit withstand capability is maintained in the scaled devices. More importantly, compared to the state-of-the-art IGBT technologies, the scaled TCIGBTs exhibit significant improvement of on-state performance. Therefore, the 3-D scaling rules provide an excellent approach of design optimization for improving the power efficiency of CIGBTs.

To suppress the collector induced barrier lowering effect in the narrow mesa trench IGBTs, a novel approach for design optimisation is demonstrated through 3-D simulations. Due to the proposed cathode design, the short-circuit capability is enabled without impact on $V_{ce(sat)}$.

Another optimisation technology that combining the advantages of silicon devices and WBG devices is applied to trench CIGBT. A hybrid configuration that integrates a silicon MOS-gated thyristor device with a SiC MOSFET is demonstrated through

experiments for the first time. Significant reduction in the switching losses can be achieved by the hybrid switch compared to the conventional TCIGBT device.

The on-state performance limits of silicon IGBTs and 4H-SiC IGBTs are estimated through theoretical analysis. Owing to the superior material properties, 4H-SiC IGBTs can provide high temperature operations at UHV conditions and the $R_{on,\,sp}$ does not show any significant increase with the increase in breakdown voltage due to conductivity modulation effect. However, the large built-in potential of 4H-SiC is the major limitation to the on-state performance in the temperature range considered. Simulation results show that the $V_{ce(sat)}$ of 4H-SiC IGBT can be reduced with increased carrier lifetime and tends to be saturated when carrier lifetime is longer than 10 μs. In addition, the on-state behaviour can be improved by increasing γ_E. Compared to the 4H-SiC IGBTs, silicon IGBTs show much lower performance limit at room temperature, although their N-drift thicknesses are 10 times higher than that of 4H-SiC IGBTs. Consequently, the silicon IGBTs are still competitive in the applications below 13 kV, due to the superior on-state behaviour and much lower material cost, particularly as many of the UHV applications which do not require fast switching and high temperature operation capabilities. Moreover, the silicon IGBTs performance limit shows that they have great potential to outperform the SiC unipolar limit at high current density operations when breakdown voltage is higher than 3 kV.

The detailed physics of the Dynamic Avalanche (DA) in the trench IGBTs was analyzed through calibrated 3D TCAD models. Management of the electric field concentration beneath trench gates is the most critical way to minimize the DA. In addition, a DA free turn-off operation is demonstrated in a Trench Clustered IGBT (TCIGBT), through in both simulations and experiments. As a MOS controlled thyristor device, TCIGBT can be operated with very low power losses at high current densities without DA and associated reliability concerns. This is because of the its PMOS action, which eliminates electric field crowding at trench bottom during turn-off transients. Moreover, experimental results confirm that DA is enhanced at high

current densities and high supply voltages and results in significant increase in E_{off} in the TIGBTs. In comparison, TCIGBTs remain DA free performance at high current density operations and high supply voltage conditions. Furthermore, the impact of DA on the turn-off dV/dt controllability of TIGBTs is analyzed through experiments. Due to DA free, the TCIGBTs show high dV/dt controllability even at high current density operations and high supply voltage conditions. Therefore, as a MOS controlled thyristor device, TCIGBT can be reliably operated with very low power losses at high current densities without DA and provides high design flexibility for power electronics systems as a result of high dV/dt controllability.

9.2 Future Work

The research work presented on the development of next generation silicon-based MOS-gated bipolar devices could be as the basis for future investigations. Several future work can start from the following points:

a) Impact of scaling rules on the Negative Gate Capacitance (NGC) effect of trench IGBTs

As the study on the scaling work of trench IGBTs is mainly focused on improving the on-state performance and turn-off performance, the impact of scaling rules on the turn-on performance is lack of study. Higher emitter side carrier density will enhance the NGC effect during turn-on, resulting in EMI noise. In addition, one common way to lower the current saturation levels in the narrow mesa IGBTs is to increase the dummy cells width, which will also enhance the NGC effect. Therefore, it becomes important to figure out the influence of scaling rules on the turn-on performance of trench IGBTs.

b) Comparison of turn-on behaviour between hybrid switch and the TCIGBT with silicon diode

As the SiC MOSFET in the hybrid switch has an embedded anti-paralleled diode, which can be used as the freewheeling diode during switching. Therefore, the turn-on performance of the hybrid switch should be improved compared to the conventional TCIGBT with external silicon diode.

c) Comparison of turn-on behaviour between trench IGBT and TCIGBT

The conventional trench IGBTs use deep p-float regions in the dummy cells to enhance the IE effect during on-state. However, this design suffers from poor turn-on dV/dt controllability due to the NGC effect. This is because the hole current flows along the wall side of the trench gate during tun-on. Several methods have been reported to suppress the gate overshoot voltage such as p-float resistors [148] and separated P-float [149]. However, these methods will affect the on-state performance due to degraded IE effect. In the TCIGBT structure, the hole current flows from P-well into mesa region directly during turn-on. Therefore, the TCIGBT is expected to show higher turn-on dV/dt controllability compared to the trench IGBTs.

d) High temperature operation capability of TCIGBT

Currently some 1.2 kV IGBTs have been reported to show high temperature operation capability at 200 °C [48, 150]. This is mainly contributed by the optimized buffer designs, which result in low leakage current levels at high temperatures. Implementing the superior buffer designs into TCIGBT technology, the TCIGBT devices are expected to have the high temperature operation capability as well. Moreover, due to the inherent advantages over trench IGBTs, TCIGBTs can remain low power losses even at 200 °C.

APPENDIX-1: LIST OF PUBLICATIONS

Conference Publications:

1. P. Luo, M. R. Sweet, and E. M. S. Narayanan, "A Snap-back Free Shorted Anode Super-Junction CIGBT," in *2016 13th International Seminar on Power Semiconductors (ISPS)*, Aug. 2016.

2. P. Luo, H. Y. Long, M. R. Sweet, M. M. D. Souza, and E. M. S. Narayanan, "Analysis of a clustered IGBT and silicon carbide MOSFET hybrid switch," in *2017 IEEE 26th International Symposium on Industrial Electronics (ISIE)*, Jun. 2017, pp. 612-615.

3. P. Luo, H. Y. Long, and E. M. S. Narayanan, "Scaling up 3-D Scaling Rules to 4.5kV CIGBT," in *2018 14th International Seminar on Power Semiconductors (ISPS)*, Aug. 2018.

4. P. Luo, E. M. S. Narayanan, S. Nishizawa, and W. Saito, "Dynamic Avalanche Free Design in 1.2kV Si-IGBTs for Ultra High Current Density Operation," in *IEDM Tech. Dig.*, Dec. 2019, pp. 12.3.1-12.3.4.

5. P. Luo, E. M. S. Narayanan, S. Nishizawa, and W. Saito, "High dV/dt controllability of 1.2kV Si-TCIGBT for high flexibility design with ultra-low loss operation," in *Proc. Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2020, pp. 686-689.

6. P. Luo, E. M. S. Narayanan, S. Nishizawa, and W. Saito, "Dynamic Avalanche Free Super Junction-TCIGBT for High Power Density Operation," in *Proc. 32nd Int. Symp. Power Semiconductor Devices and IC's (ISPSD)*, Sep. 2020, pp. 470-473.

7. P. Luo, E. M. S. Narayanan, S. Nishizawa, and W. Saito, "High dV/dt Controllability of 1.2kV TCIGBT through Dynamic Avalanche Elimination," in *PCIM Asia*, Nov. 2020, pp. 176-180.

Journal Publications:

1. P. Luo, M. Sweet, and E. M. S. Narayanan, “Snap-back Free Shorted-Anode Super-Junction TCIGBT,” *IET Power Electronics*, vol. 11, no. 4, pp. 654-659, 2018.

2. P. Luo, H. Y. Long, M. R. Sweet, M. M. D. Souza, and E. M. S. Narayanan, "Numerical Analysis of 3-D Scaling Rules on a 1.2-kV Trench Clustered IGBT," *IEEE Transactions on Electron Devices*, vol. 65, no. 4, pp. 1440-1446, 2018.

3. P. Luo, H. Y. Long, and E. M. S. Narayanan, "A Novel Approach to Suppress the Collector-Induced Barrier Lowering Effect in Narrow Mesa IGBTs," *IEEE Electron Device Letters*, vol. 39, no. 9, pp. 1350-1353, 2018.

4. P. Luo, E. M. S. Narayanan, S. -I. Nishizawa and W. Saito, "Evaluation of Dynamic Avalanche Performance in 1.2-kV MOS-Bipolar Devices," *IEEE Transactions on Electron Devices*, vol. 67, no. 9, pp. 3691-3697, 2020.

5. P. Luo and E. M. S. Narayanan, "3-D Scaling Rules for High-Voltage Planar Clustered IGBTs," *IEEE Transactions on Electron Devices*, vol. 67, no. 12, pp. 5613-5620, 2020.

6. P. Luo and E. M. S. Narayanan, "Theoretical Analysis of on-State Performance Limit of 4H-SiC IGBT in Field-Stop Technology," *IEEE Transactions on Electron Devices*, vol. 67, no. 12, pp. 5621-5627, 2020.

7. P. Luo, E. M. S. Narayanan, S. -I. Nishizawa and W. Saito, "Turn-OFF dV/dt Controllability in 1.2-kV MOS-Bipolar Devices," *IEEE Transactions on Power Electronics*, vol. 36, no. 3, pp. 3304-3311, 2021.

APPENDIX-2: LIST OF FIGURES

APPENDIX-3: LIST OF TABLES

APPENDIX-4: SIMULATED MODEL-3D-TCIGBT

```
;-----------------------------------------------------------------
; Structure definition
;-----------------------------------------------------------------;
(sdegeo:set-default-boolean "BAB")
(define Xmax 5)
(define Ymax 30)
(define Zmax -110)
(define Dnp 0.25)
(sdegeo:create-cuboid (position 1.6 0.0 0.3 ) (position 2.6 Ymax -4.5 ) "PolySi" "R.PolyGate")
(sdegeo:fillet (list (car (find-edge-id (position 1.6 3.0 -4.5)))) 0.3)
(sdegeo:fillet (list (car (find-edge-id (position 2.6 3.0 -4.5)))) 0.3)
(sdegeo:create-cuboid (position 1.5 0.0 0.3 ) (position 2.7 Ymax -4.6 ) "Oxide" "R.Gox")
(sdegeo:fillet (list (car (find-edge-id (position 1.5 3.0 -4.6)))) 0.3)
(sdegeo:fillet (list (car (find-edge-id (position 2.7 3.0 -4.6)))) 0.3)
(sdegeo:create-cuboid (position 0.0 0.0 0.0 ) (position Xmax Ymax Zmax ) "Silicon" "SubsSilicon")
(sdegeo:create-cuboid (position 0.0 24.0 0.3 ) (position 1.5 Ymax 0.0 ) "Oxide" "R.Spacer")
(sdegeo:create-cuboid (position 2.7 0.0 0.3 ) (position Xmax Ymax 0.0 ) "Oxide" "R.Spacer")
;-----------------------------------------------------------------
; Doping Profiles
;-----------------------------------------------------------------;
; ------ PolyGate ------
(sdedr:define-constant-profile "Const.PolyGate"
 "PhosphorusActiveConcentration" 1e+21 )
(sdedr:define-constant-profile-material "PlaceCD.PolyGate"
 "Const.PolyGate" "PolySi" )

; ------ Substrate ------
(sdedr:define-constant-profile "Const.Bulk"
 "PhosphorusActiveConcentration" 5e+13 )
(sdedr:define-constant-profile-region "PlaceCD.Bulk"
 "Const.Bulk" "SubsSilicon" )

; ------ P-well ------
(sdedr:define-refinement-window "Win.Pwell" "Rectangle"
 (position -5.0 -5.0 0.0)
 (position 10.0 25.2 0.0) )
```

```
(sdedr:define-gaussian-profile "Gauss.Pwell"
 "BoronActiveConcentration"
 "PeakPos" 0.0  "PeakVal" 5e16
 "ValueAtDepth" 7e15 "Depth" 8.0
 "Gauss"  "Factor" 0.3)
(sdedr:define-analytical-profile-placement "PlaceAP.Pwell"
 "Gauss.Pwell" "Win.Pwell" "Both" "NoReplace" "Eval")

; ------ N-well ------
(sdedr:define-refinement-window "Win.Nwell" "Rectangle"
 (position -5.0 -5.0 0.0)
 (position 10.0 25.2 0.0) )
(sdedr:define-gaussian-profile "Gauss.Nwell"
 "ArsenicActiveConcentration"
 "PeakPos" 0.0  "PeakVal" 8e16
 "ValueAtDepth" 1e16 "Depth" 6.2
 "Gauss"  "Factor" 0.32)
(sdedr:define-analytical-profile-placement "PlaceAP.Nwell"
 "Gauss.Nwell" "Win.Nwell" "Both" "NoReplace" "Eval")

; ------ P-base ------
(sdedr:define-refinement-window "Win.Pbase" "Rectangle"
 (position -5.0 -5.0 0.0)
 (position 10.0 25.0 0.0) )
(sdedr:define-gaussian-profile "Gauss.Pbase"
 "BoronActiveConcentration"
 "PeakPos" 0.0  "PeakVal" 2.3e17
 "ValueAtDepth" 2.3e16 "Depth" 2.0
 "Gauss"  "Factor" 0.4)
(sdedr:define-analytical-profile-placement "PlaceAP.Pbase"
 "Gauss.Pbase" "Win.Pbase" "Both" "NoReplace" "Eval")

; ------ N-plus ------
(sdedr:define-refinement-window "BaseLine.nplus1" "Rectangle"
 (position -0.5 -0.5 0.0)
 (position 1.8 1.5 0.0) )
(sdedr:define-gaussian-profile "Impl.nplus1prof"
 "ArsenicActiveConcentration"
 "PeakPos" 0.0  "PeakVal" 1e20
 "ValueAtDepth" 2e19  "Depth" Dnp
 "Erf"  "Length" 0.02)
(sdedr:define-analytical-profile-placement "Impl.nplus1"
 "Impl.nplus1prof" "BaseLine.nplus1" "Both" "NoReplace" "Eval")
```

```
(sdedr:define-refinement-window "BaseLine.nplus2" "Rectangle"
 (position -0.5 6.0 0.0)
 (position 1.8 7.5 0.0) )
(sdedr:define-gaussian-profile "Impl.nplus2prof"
 "ArsenicActiveConcentration"
 "PeakPos" 0.0  "PeakVal" 1e20
 "ValueAtDepth" 2e19  "Depth" Dnp
 "Erf"  "Length" 0.02)
(sdedr:define-analytical-profile-placement "Impl.nplus2"
 "Impl.nplus2prof" "BaseLine.nplus2" "Both" "NoReplace" "Eval")

(sdedr:define-refinement-window "BaseLine.nplus3" "Rectangle"
 (position -0.5 12.0 0.0)
 (position 1.8 13.5 0.0) )
(sdedr:define-gaussian-profile "Impl.nplus3prof"
 "ArsenicActiveConcentration"
 "PeakPos" 0.0  "PeakVal" 1e20
 "ValueAtDepth" 2e19  "Depth" Dnp
 "Erf"  "Length" 0.02)
(sdedr:define-analytical-profile-placement "Impl.nplus3"
 "Impl.nplus3prof" "BaseLine.nplus3" "Both" "NoReplace" "Eval")

(sdedr:define-refinement-window "BaseLine.nplus4" "Rectangle"
 (position -0.5 18.0 0.0)
 (position 1.8 19.5 0.0) )
(sdedr:define-gaussian-profile "Impl.nplus4prof"
 "ArsenicActiveConcentration"
 "PeakPos" 0.0  "PeakVal" 1e20
 "ValueAtDepth" 2e19  "Depth" Dnp
 "Erf"  "Length" 0.02)
(sdedr:define-analytical-profile-placement "Impl.nplus4"
 "Impl.nplus4prof" "BaseLine.nplus4" "Both" "NoReplace" "Eval")

; ------ P-plus ------
(sdedr:define-refinement-window "BaseLine.pplus1" "Rectangle"
 (position -0.5 1.5 0.0)
 (position 1.8 6.0 0.0) )
(sdedr:define-gaussian-profile "Impl.pplus1prof"
 "BoronActiveConcentration"
 "PeakPos" 0.0  "PeakVal" 1e20
 "ValueAtDepth" 2e19  "Depth" Dnp
 "Erf"  "Length" 0.02)
```

```
(sedr:define-analytical-profile-placement "Impl.pplus1"
 "Impl.pplus1prof" "BaseLine.pplus1" "Both" "NoReplace" "Eval")

(sedr:define-refinement-window "BaseLine.pplus2" "Rectangle"
 (position -0.5 7.5 0.0)
 (position 1.8 12.0 0.0) )
(sedr:define-gaussian-profile "Impl.pplus2prof"
 "BoronActiveConcentration"
 "PeakPos" 0.0  "PeakVal" 1e20
 "ValueAtDepth" 2e19  "Depth" Dnp
 "Erf"  "Length" 0.02)
(sedr:define-analytical-profile-placement "Impl.pplus2"
 "Impl.pplus2prof" "BaseLine.pplus2" "Both" "NoReplace" "Eval")

(sedr:define-refinement-window "BaseLine.pplus3" "Rectangle"
 (position -0.5 13.5 0.0)
 (position 1.8 18.0 0.0) )
(sedr:define-gaussian-profile "Impl.pplus3prof"
 "BoronActiveConcentration"
 "PeakPos" 0.0  "PeakVal" 1e20
 "ValueAtDepth" 2e19  "Depth" Dnp
 "Erf"  "Length" 0.02)
(sedr:define-analytical-profile-placement "Impl.pplus3"
 "Impl.pplus3prof" "BaseLine.pplus3" "Both" "NoReplace" "Eval")

(sedr:define-refinement-window "BaseLine.pplus4" "Rectangle"
 (position -0.5 19.5 0.0)
 (position 1.8 24.0 0.0) )
(sedr:define-gaussian-profile "Impl.pplus4prof"
 "BoronActiveConcentration"
 "PeakPos" 0.0  "PeakVal" 1e20
 "ValueAtDepth" 2e19  "Depth" Dnp
 "Erf"  "Length" 0.02)
(sedr:define-analytical-profile-placement "Impl.pplus4"
 "Impl.pplus4prof" "BaseLine.pplus4" "Both" "NoReplace" "Eval")

; ------ N-buffer ------
(sedr:define-refinement-window "Win.Nbuffer" "Rectangle"
 (position -5.0 -5.0 Zmax)
 (position 8.0 50.0 Zmax) )

(sedr:define-gaussian-profile "Gauss.Nbuffer"
 "ArsenicActiveConcentration"
```

```
 "PeakPos" 0.0  "PeakVal" 1e16
 "ValueAtDepth" 1e15 "Depth" 7.0
 "Gauss"  "Factor" 0.1)
(sedr:define-analytical-profile-placement "PlaceAP.nbuffer"
 "Gauss.Nbuffer" "Win.Nbuffer" "Both" "NoReplace" "Eval")

; ------ P-anode ------
(sedr:define-refinement-window "Win.Panode" "Rectangle"
 (position -5.0 -5.0 Zmax)
 (position 8.0 50.0 Zmax) )
(sedr:define-gaussian-profile "Gauss.Panode"
 "BoronActiveConcentration"
 "PeakPos" 0.1  "PeakVal" 5e17
 "ValueAtDepth" 5e16 "Depth" 0.7
 "Gauss"  "Factor" 0.1)
(sedr:define-analytical-profile-placement "PlaceAP.Panode"
 "Gauss.Panode" "Win.Panode" "Both" "NoReplace" "Eval")

;-----------------------------------------------------------------;
; Electrodes
;-----------------------------------------------------------------;
(sdegeo:define-contact-set "Emitter"   4  (color:rgb 1 0 0 ) "##" )
(sdegeo:define-contact-set "Collector" 4  (color:rgb 1 0 0 ) "==" )
(sdegeo:define-contact-set "Gate"      4  (color:rgb 1 0 0 ) "<><>" )

(sdegeo:define-3d-contact (find-face-id (position 1.0 3.0 0.0)) "Emitter")
(sdegeo:define-3d-contact (find-face-id (position 1.5 6.0 Zmax)) "Collector")
(sdegeo:define-3d-contact (find-face-id (position 1.9 3.0 0.3)) "Gate")

;-----------------------------------------------------------------
; Meshing
;-----------------------------------------------------------------;
(sdedr:define-refinement-window "RW.SiTop"
 "Cuboid"
 (position 0.0 0.0 0.0 )
 (position Xmax Ymax -20.0 ))
(sdedr:define-refinement-size "Ref.SiTop"
  1.50  2.00  1.00
  0.05  0.05  0.05)
(sdedr:define-refinement-function "Ref.SiTop"
 "DopingConcentration" "MaxTransDiff" 1)
(sdedr:define-refinement-placement "RefPlace.SiTop"
 "Ref.SiTop" "RW.SiTop" )
```

```
(sdedr:define-refinement-window "RW.SiMid"
 "Cuboid"
 (position 0.0  0.0 -20.0 )
 (position Xmax Ymax -100.0 ))
(sdedr:define-refinement-size "Ref.SiMid"
  2.00  3.00  5.00
  0.10  0.10  0.10 )
(sdedr:define-refinement-function "Ref.SiMid"
 "DopingConcentration" "MaxTransDiff" 1)
(sdedr:define-refinement-placement "RefPlace.SiMid"
 "Ref.SiMid" "RW.SiMid" )

(sdedr:define-refinement-window "RW.SiBot"
 "Cuboid"
 (position 0.0 0.0 -100.0 )
 (position Xmax Ymax Zmax ))
(sdedr:define-refinement-size "Ref.SiBot"
  1.50  3.00  1.00
  0.05  0.05  0.05)
(sdedr:define-refinement-function "Ref.SiBot"
 "DopingConcentration" "MaxTransDiff" 1)
(sdedr:define-refinement-placement "RefPlace.SiBot"
 "Ref.SiBot" "RW.SiBot" )

(sdedr:define-refinement-window "RW.Mesa"
 "Cuboid"
 (position 0.0 0.0 0.0 )
 (position 2.0 26.0 -5.0 ))
(sdedr:define-refinement-size "Ref.Mesa"
  0.10  0.50  0.50
  0.03  0.05  0.05)
(sdedr:define-refinement-function "Ref.Mesa"
 "DopingConcentration" "MaxTransDiff" 1)
(sdedr:define-refinement-placement "RefPlace.Mesa"
 "Ref.Mesa" "RW.Mesa" )
;-----------------------------------------------------------------
; Saving BND file
(sdeio:save-tdr-bnd (get-body-list) "@tdrboundary/o@")

; Save CMD file
(sdedr:write-cmd-file "@commands/o@")
(system:command "snmesh -offset n@node@_msh")
```

APPENDIX-5: REFERENCES

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