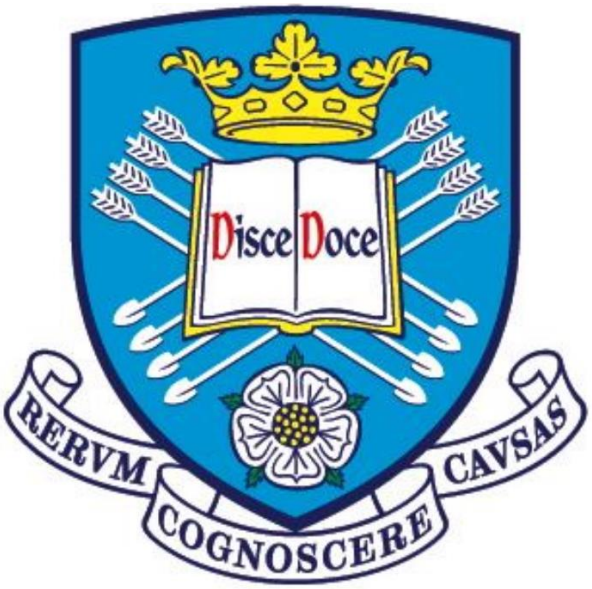


# High Efficiency GaN Power Converters

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# Abstract

Industries have been exploring Gallium Nitride (GaN) as a candidate of material choice for the next-generation power semiconductor device technologies due to their superior material properties compared to Silicon (Si) that has been the predominant choice in conventional power electronics applications.

One of the main focus of the research work presented in this thesis is the performance evaluation of a new lateral GaN-based semiconductor device technology referred to as 'Polarisation Super Junction' (PSJ). The large-area PSJ samples with the breakdown capability of > 3 kV from POWDEC K.K. were used for this work. Their static on-state and off-state current-voltage characteristics at temperatures up to $150^0$C were extracted and presented. According to the results, they can offer much lower specific on-state resistance compared to commercial GaN devices of much lower breakdown capability. Also, their typical turn-on and turn-off switching performances under 900V dc link with various load current levels and device temperatures of up to $150^0$C were evaluated using a double pulse test circuit with an inductive load configuration. The criteria for the selection of voltage and current measurement techniques for switching test are discussed thoroughly as well. The same tests were carried out for cascode GaN devices that were realized via bare GaN PSJ and Si-MOSFET dies attached to a direct copper bond substrate and bonded wires for electrical connections between them.

Despite its advantage it can offer in terms of enhanced breakdown voltage and significantly reduced area-specific on-state resistance, the PSJ transistors are inherently depletion-mode (D-mode) or normally-on devices due to the spontaneous formation of 2-dimensional electron gas (2DEG) via polarisation

present at the GaN/AlGaN heterointerface and thus negative gate drive voltage is required for them to be turned off. Hence, critical safety concerns arise if the gate drive voltage supplies fail. Also, short-circuit issues may arise even during normal operation as the controller may send a false command signal due to electromagnetic interference (EMI). In order to mitigate these issues, a refined version of the protection circuit proposed in a previous work was proposed, simulated and implemented onto a printed circuit board for demonstration. From both simulation and hardware results, it has been confirmed that the prototyped circuit is capable of providing protection necessary during the normal operation and gate drive supply failure event of D-mode power devices in power converters.

Finally, the design process for the bi-directional DC-to-DC converter with efficiency target of >98% using D-mode GaN PSJ transistors is discussed in detail. The converter consists of the 2$^{nd}$ prototype of the gate drive failure protection scheme, a forced convection heatsink for cooling the power devices and passive elements including an inductor and output side capacitor (s) that provides dc current and dc voltage. However, due to the conducted EMI that arised from high dV/dt during the device turn-on, the controller was falsely toggled to command the converter operation to be halted during normal operation at dc supply voltages above 300 V. Nevertheless, the fail-safe operation of the converter under the supply failure event and its system requirement were verified using PSpice simulator with the behavioural model of the large-area PSJ transistor that was fitted to its measurement parameters and the same operating conditions as for its hardware prototype. Potential mitigation strategies on the controller side and the circuit side are proposed, which will pave the way for future high-efficiency power converter design and hardware validation using the latest PSJ device technology.

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# 1 Introduction

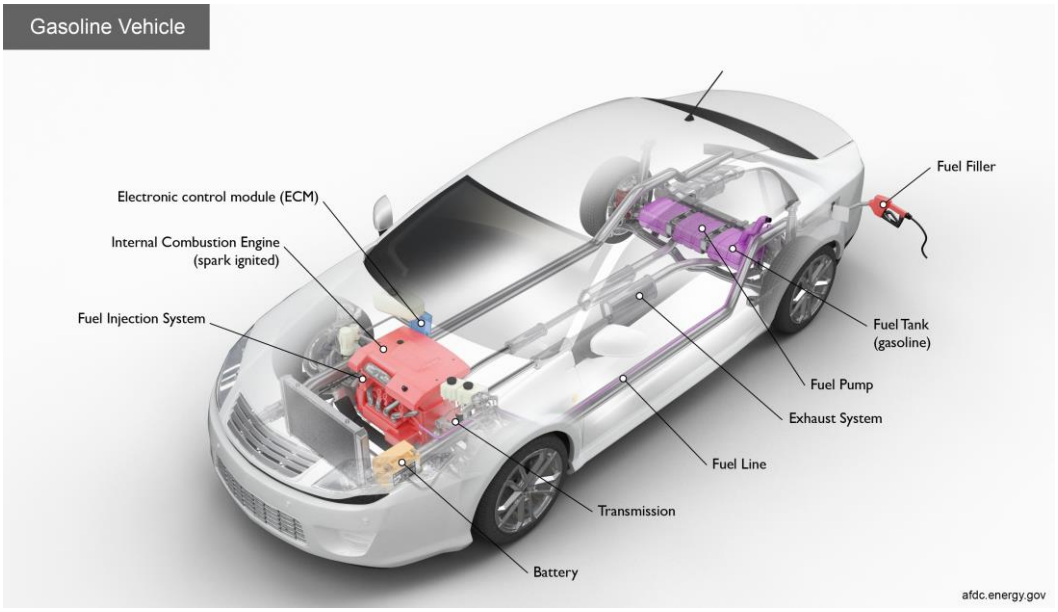
## *1.1. Overview*

For powering conventional aircrafts, Kerosene, a carbon-based fuel derived from crude oil, has been used predominantly for several decades mainly due to their high energy density that allows long-distance journey [1]. Likewise, for automotive industry, diesel and petrol, which are both derived from crude oil, have been the most dominant fuel for their operation due to the same reason [2]. However, the awareness in environmental impact of greenhouse gas (mainly Carbon Dioxide, $CO_2$) emissions due to fuel burns from aviation and transportation has been raised since the total amount of greenhouse gas emission have risen due to significant increase in air and road traffics worldwide for the last two decades [1, 3]. In year 2001, the Advisory Council for Aviation Research and innovation in Europe (ACARE) has presented a 'Vision 2020' resolution that demands 50% and 80% reduction of $CO_2$ per passenger kilometer (hence fuel consumption) and Nitrogen Oxide (NO) emissions of the aircrafts, respectively [4]. This has imposed a lot of pressure for the aerospace industry to exploit alternative aviation fuels for powering the aircrafts. The resolution also demands the aircrafts to become lighter in weight by using advanced composite materials to manufacture them that yields lower fuel consumption.

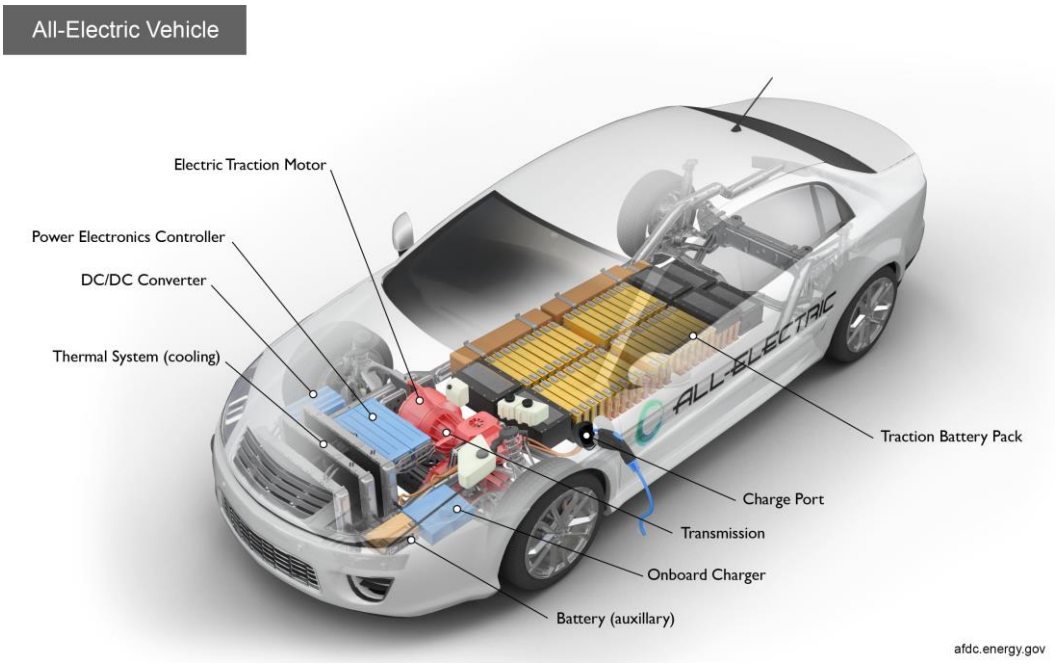
Similarly, the UK government has recently released its 'Air quality plan for nitrogen dioxide ($NO_2$)' to put the sale of petrol and diesel cars and vans to an end and to ensure that they have zero emission by 2040 [5], which strongly demands the electric car manufacturers to expand their market for electric vehicles (EVs) that may be powered using batteries, hydrogen fuel cells or hybrid configuration with

conventional diesel / petrol combustion engines. In particular, if battery powered EVs (BEVs), which is illustrated in Figure 1-1(b), can fully replace the road vehicles currently powered by fossil fuels in the future, and renewable energy sources are used solely for charging the EV batteries, then zero emission can be achieved with a significantly reduced fuel cost compared to fossil fuels.

The BEV system involves the use of power converters that serves to transfer power from the traction battery pack to the electric traction motors for running the vehicle and to the lower voltage DC network to run vehicle accessories [6]. These power converters consist of passive elements including inductors and/or capacitors that store energy in the form of magnetics and electrical charges, respectively. Also, certain amount of power will be lost by the power semiconductor devices during the power conversion process, which leads to a need for sufficient cooling via heatsinks to prevent overheating and thus failure. These elements, passive components and heatsinks, are the major contributing factors to the overall volume and weight of power electronics that determines the vehicle weight and size and thus its overall fuel efficiency. The main driving factor for heatsink sizing is the power loss of the switching devices and hence the converter's efficiency; the more efficient the converter is, the less power is lost by heat and thus less cooling effort is required that often leads to smaller heatsinks. The passive elements' sizes are usually driven by switching frequency ($f_{sw}$) of the devices; as the $f_{sw}$ becomes higher, then passive components can be reduced in volume and weight. However, the power loss level will increase with $f_{sw}$ that will lead to larger heatsink size required and thus trade-off exists.




(a)




(b)

*Figure 1-1: Diagram of (a) conventional diesel cars and (b) battery-powered EVs with the key components highlighted [6, 7]*

Meanwhile, the aerospace industry have been exploring into alternative sustainable fuel sources including biomass-derived synthetic paraffinic fuel (synfuel) [8, 9], Ethanol [10, 11] and biofuels made by seed oils [12, 13], used

cooking oils, animal fats, and vegetable oils [9]. A blend of conventional crude oil-based JP-8 fuel and synthetic fuel made by Fischer-Tropsch (FT) chemistry has been tested extensively in C-17 cargo jets since 2007 [14, 15]. Along with continuous research into alternative aviation fuels, the aerospace industry has also been striving to improve the fuel efficiency of the aircraft engines in order to reduce the amount of fuel consumption and its emission.

The conventional "Fly-by-Wire" (FBW) aircraft system was first introduced in Airbus A320 aircrafts in 1980s. It replaced mechanical and hydro-mechanical control systems (that were controlled manually) for controlling flight surface control actuators with their electrical counterparts incorporating computers [16], which made the control easier and safer and reduced the weight of the aircraft. The conventional FBW-based aircraft system is illustrated in Figure 1-2 [17]. The generators generate a constant three-phase 400Hz, 115V AC for electrical loads including avionics and cabin systems such as lighting and in-flight entertainment systems etc [18]. The pneumatic air bleed system controls the cabin pressure and provides cabin air-conditioning and wing de-icing. Hydraulic pumps are used for powering flight surface control actuators, landing gear and braking systems.

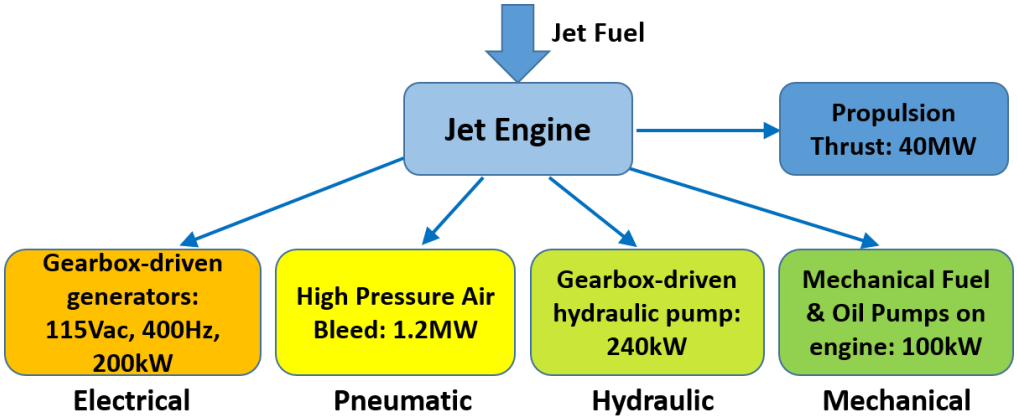



*Figure 1-2: Block diagram of conventional aircraft system [17]*

The conventional aircrafts are controlled electrically but powered hydraulically. A mixture of hydraulic and pneumatic systems tends to be very heavy, inefficient and require frequent maintenances. This leads to heavier aircraft, poorer fuel efficiency and thus more fuel consumption and greenhouse gas emissions [19]. Therefore, effort has been devoted to realise a new "More Electric Aircraft" (MEA) architecture in aircrafts, which is illustrated in Figure 1-3. It aims to replace hydraulic and pneumatic systems that controlled core aircraft systems including flight control surface actuators (elevators, ailerons, spoilers and rudders), landing gears, engine generators and wing de-icing system with their electrical counterparts [18, 20].

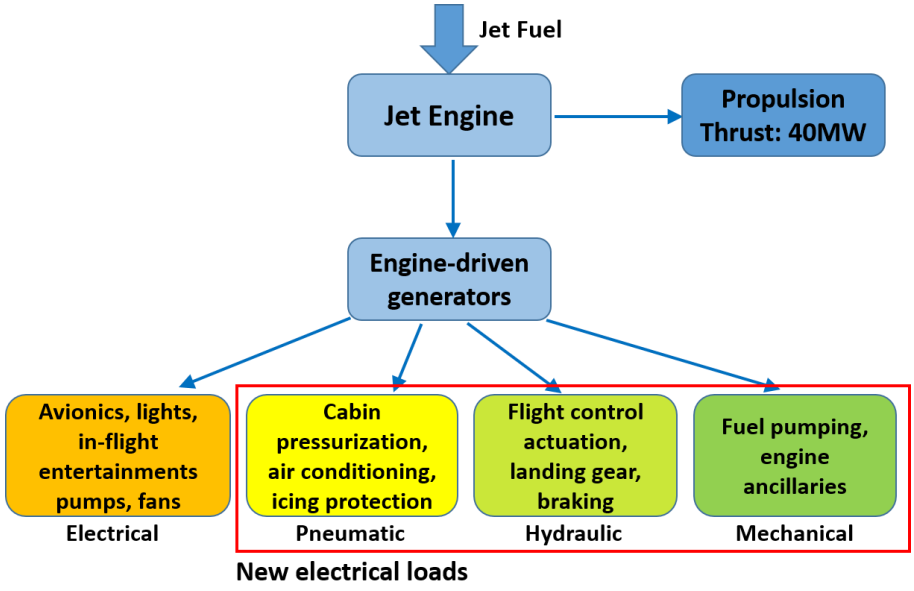



*Figure 1-3: Block diagram of the More Electric Aircraft (MEA) system [17]*

As according to the study conducted by NASA, electrical systems are relatively lighter in weight, quieter and more efficient compared to hydraulic and pneumatic systems and hence can potentially reduce the aircraft weight, noise and fuel consumption [19]. The MEA was achieved in commercial aircrafts including

Boeing 787 where fuel burn was reduced by 20% compared to previous Boeing 767 aircraft [21]. In fact, reduced mechanical complexity and enhanced fuel efficiency and thrust output were realised in Boeing 787 due to the elimination of hydraulic actuators and pneumatic air bleed system for deicing, respectively [22].

The electrical power distribution system of the Boeing 787 MEA architecture is illustrated in Figure 1-4. Apparent power of 250kVA is generated from each of the four Variable Frequency Starter Generators (VFSG), providing a total of 1MVA to the airframe that is at least double of the Boeing 747. The main 230V AC bus is fed by four VFSGs, and is distributed to provide appropriate voltage and power levels to AC and DC loads via rectifiers and transformers [22]. Unlike conventional aircraft power distribution system, by using 235V AC and ±270V DC bus, which are larger than the conventional 115V AC and 28V DC, heavier loads including compressors, cabin air pressurisation and air-conditioning systems can be powered electrically. Furthermore, the cables in dc systems are lighter in weight and smaller in size required than the ones in ac systems due to their lack of reactive power and skin and proximity effects that leads to an increase in cable resistance [23].

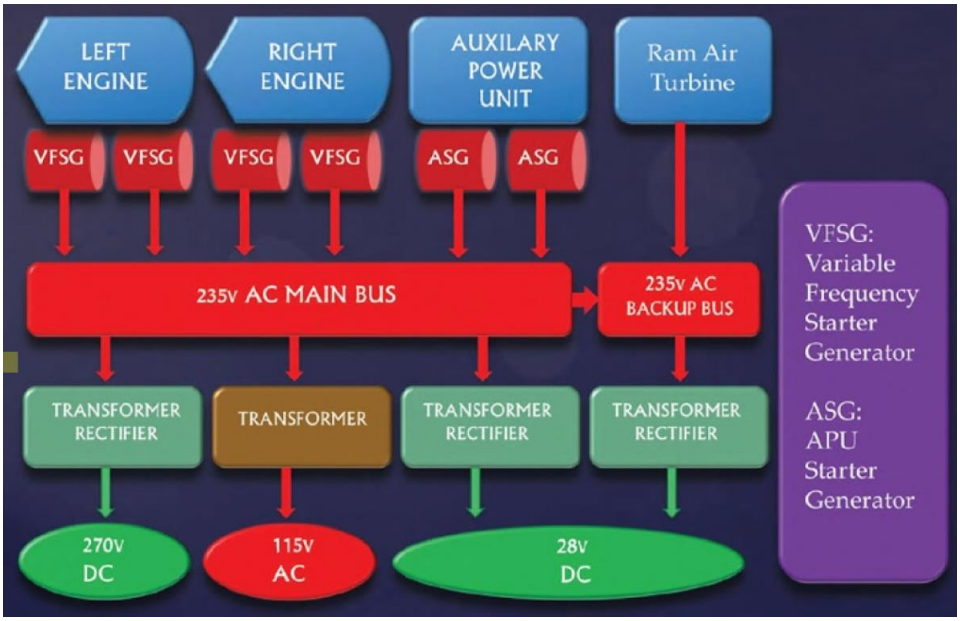



*Figure 1-4: The Electrical Distribution System of Boeing 787 [22]*

During takeoff and landing of the aircraft, the flight surface control actuator draws significant amount of transient load power. Hence, the generator designs must be tailored to meet this transient load demand, which increases the overall cost and weight of the system. This dynamic change in the load can also lead to torque pulsations on the generator shafts, causing failures in load management system [24]. In order to mitigate this issue, introduction of energy storage systems (ESS) eliminates the transient load effect on the generator shaft and hence improve the future aircraft load management. Figure 1-5 illustrates the MEA architecture with energy storage systems. The most common electrical energy storage methods are lithium ($L^-$) ion batteries and supercapacitors (SCs). Batteries, in general, exhibit much higher energy density compared to SCs but are shorter in lifetime [25]. Also, SCs have their electric charges being built up electrically, whereas charges in batteries are produced by relatively slower chemical reactions [26, 27]. Therefore, SCs are more capable of supplying a burst of large yet very short-

transient powers compared to batteries, and yet are used in conjunction with batteries due to their low energy densities [27].

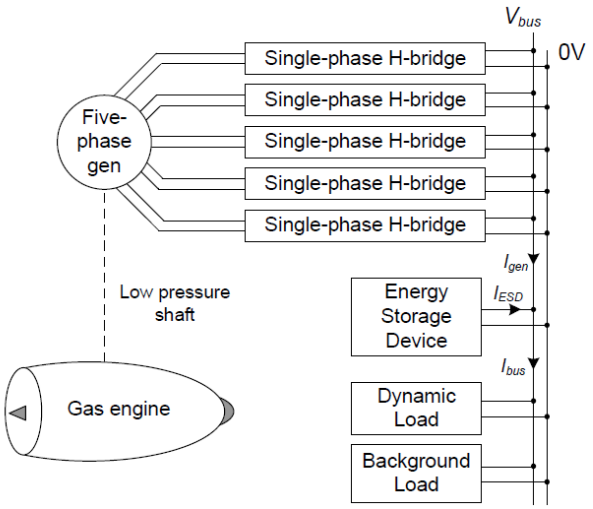



*Figure 1-5: Block diagram of a MEA system with ESS [24]*

Unfortunately, many challenges arise with future MEA with ESS. First of all, electrical load power demand in MEA becomes much higher as hydraulic and pneumatic driven systems are replaced by their electrical counterparts. This requires more cooling effort and dynamic control of power converters to maintain stable DC-link voltage under varying load. Also, the size and weight of current-carrying conductors in power distribution network is required to be larger as they need to carry more load current [28]. Secondly, the energy density of electrical energy storage systems, including L-ion batteries and super-capacitors, are far lower than that of conventional aviation fuels. The energy density of L-ion batteries and Kerosene are 1MJ/kg and 43MJ/kg, respectively [29]. Hence, replacing the liquid fuel tank with large number of conventional batteries may not be a viable option. Although many research on development of high energy density batteries with longer lifetime and better reliability using advanced battery materials have been

carried out, they are still at their developing phase [30]. Nevertheless, it is expected that continuous development of electrical ESS with high energy density and power converter designs with high power density and efficiency will ultimately yield remarkable reduction in size and weight of the aircraft and thus fuel consumption, noise and $CO_2$ emission.

The system voltage level was increased from 270 V DC for conventional aircrafts to +/-270 V (540 V) for Boeing 787 aircrafts [28]. Should the power demand rise to a higher level in future aerospace applications, the level electrical current and hence the size and weight of the cables would need to be increased significantly for the same AC and DC voltage levels so that the total voltage drop across the cables is minimised. The general trend in future aircraft development is to increase the voltage level above 540 V DC for larger power demand handling capability [31, 32]. This, in turn, implies that the current level and hence cable weight and volume can be reduced. Nevertheless, this also leads to thicker cable insulation requirement and give rise to 'partial discharge' and thereby counterbalance the decrease in cable weight, which fundamentally limits the maximum DC voltage level [28]. With an optimum increase in system voltage for minimum cable weight and high energy density ESS, the weight of the future aircrafts can be reduced and hence their environmental impact can be minimised. In order to achieve this, the power semiconductor devices that can withstand DC voltages in the range of few kilovolts would be required for use in power converters, which is where the use of power devices based on wide band-gap materials would be considered beneficial.

## *1.2. Need for Wide Band-gap (WBG) Semiconductor Materials*

To utilize the ESS in MEA and BEV systems, suitable DC to DC converters are required as means of interface between ESS and the DC-link grid. The size and weight of this converter must be reduced so that the weight, power loss and thus fuel consumption of the future aircraft and EV can be reduced. In order to achieve this, the converter's passive filtering components (consisting of inductor and capacitor) and heatsink requirement of power semiconductor devices must be reduced as they are known to be the heaviest and bulkiest components in power converters. The passive filtering element sizes can be reduced by increasing the switching frequency of the semiconductor devices as the current and voltage ripples are reduced. However, this will lead to increased power losses of the devices due to increased switching power loss and thus increased heatsink requirement and decreased converter efficiency. In contrast, reducing the switching frequency leads to smaller power loss and hence heatsink size at the expense of larger passive filtering components. The switching frequency and hence converter's power density are limited by this trade-off.

The vast majority of commercial power semiconductor devices nowadays are manufactured using Silicon (Si). The electrical performance of Si-based power devices have been evolving and improving continuously over time. Nevertheless, Si-based device technologies have reached a stage where performance improvements are very incremental with increased cost of fabrication. In addition, their operation at high ambient temperatures above $100^0$C is extremely difficult since an increase of internal device junction temperature leads to larger off-state leakage current and hence power loss that can compromise the device reliability. As a result, many research works have been carried out to realise novel

semiconductor devices using alternative semiconductor materials to Si to realise power converters with less power loss and thus better efficiency.

The WBG materials including Silicon Carbide (SiC) and Gallium Nitride (GaN) have been recently identified as popular candidates for the next-generation power devices due to the superiority of their intrinsic material properties that leads to reduced power losses and hence better efficiency. Fundamental intrinsic material properties of Si and WBG materials are presented in Table 1-1. The band-gap energy of GaN is larger than Si and SiC, which yields enhancements in breakdown voltage and operating temperature and reduction in the on-state resistance ($R_{ds,on}$) of power devices. Although Diamond has the largest bandgap energy value amongst the semiconductor materials enlisted in Table 1-1, their substrates are considerably limited in size and quality compared to other materials due to their relative immaturity [33].

| Properties | Si | SiC | GaN | Diamond |
|---|---|---|---|---|
| Bandgap Energy, $E_g$ (eV) | 1.12 | 3.26 | 3.45 | 5.45 |
| Breakdown Electric Field, $E_c$ (kV/cm) | 300 | 2200 | 3300 | 10000 |
| Electron Mobility, $u_n$ ($cm^2/V*sec$) | 1500 | 1250 | 800 (Bulk)<br>1700 (2DEG) | 2200 |
| Intrinsic carrier concentration, $n_i$ ($cm^{-3}$) | $1 \times 10^{10}$ | $8 \times 10^{-9}$ | $2 \times 10^{-10}$ | $1 \times 10^{-20}$ |
| Thermal Conductivity, λ (W/cm*K) | 1.5 | 4.9 | 1.3 | 22 |
| Saturated electron velocity, $v_{sat}$ ($*10^7$cm/sec) | 1 | 2 | 2.2 | 2.7 |

*Table 1-1: Intrinsic material properties of Si and WBG materials [34]*

With wider band gap between conduction and valence bands of the semiconductor, larger electric field and hence voltage level needs to be applied for

the free electrons and holes to gain sufficient kinetic energy to collide with crystal atoms to create free electron-hole (e-h) pairs that also gains sufficient energy to create more e-h pairs subsequently, which leads to significant increase in off-state leakage current and thus cause 'avalanche breakdown' [35]. Also, as the band-gap is increased, larger thermal energy for electrons in valence band (i.e. electrons tied to the nucleus of the solid-state material) to move towards conduction band (i.e. for electrons to move freely) is required; hence, GaN devices can operate at higher temperatures than their Si and SiC counterparts [36]. The on-state resistance ($R_{ds,on}$) of the device is proportional to the length of its drift region ($L_{drift}$), through which the current flows, that supports the full dc voltage when the device is 'off'. In order to increase the breakdown voltage, the $L_{drift}$ Hence, the specific on-state resistance ($R_{ds,on}$*$mm^2$) of GaN devices are smaller than their Si counterparts by three orders of magnitude as illustrated in Figure 1-6. As a result, the $R_{ds,on}$ and the required device area of GaN devices can be reduced significantly compared to Si devices with same current rating. Due to these reasons, GaN devices are considered to be the most feasible candidate for future aerospace systems with larger DC-link voltage levels where devices with larger breakdown voltages and minimal power losses are required as discussed in Section 1.1.

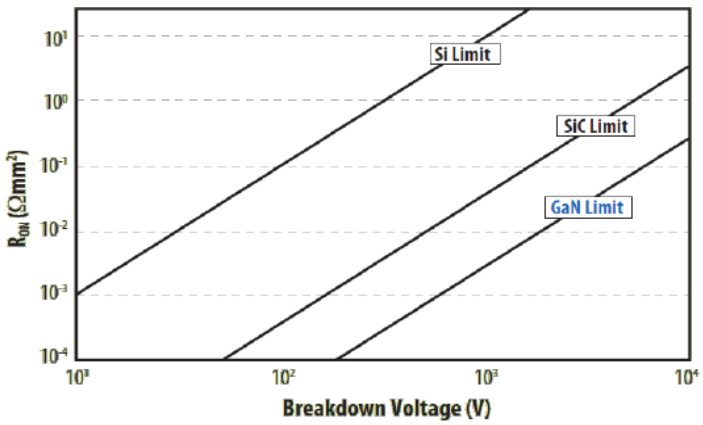
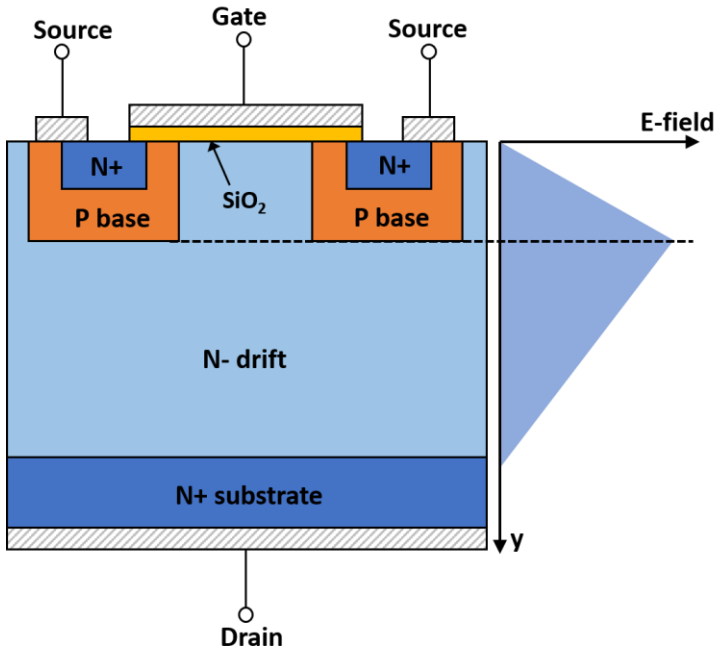



*Figure 1-6: Specific $R_{ds,on}$ ($R_{ds,on}$*$mm^2$) limit of intrinsic Si, SiC and GaN [37]*

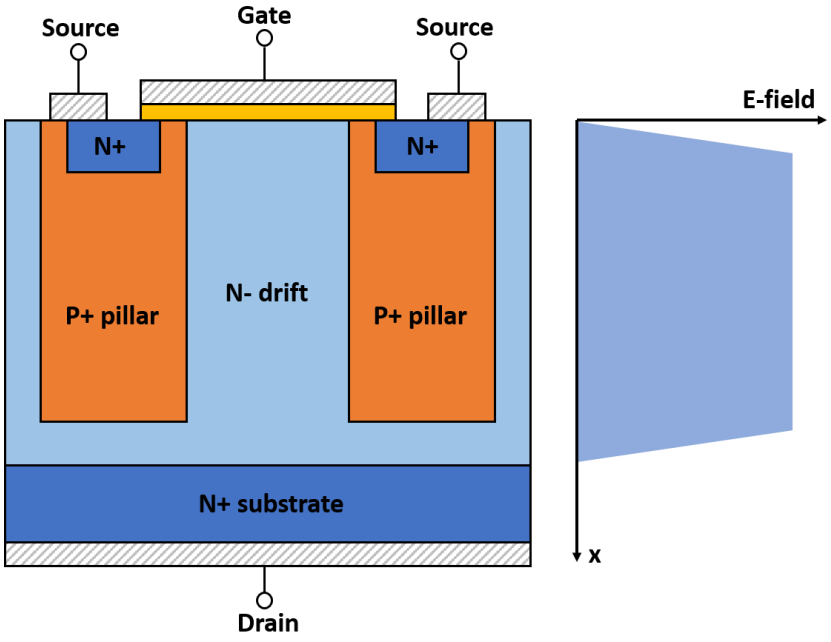
The $R_{ds,on}$*$mm^2$ figure is obtained by multiplying on-state resistance and active area of the device. With smaller $R_{ds,on}$*$mm^2$, the unipolar devices can carry same amount of current with smaller die area and hence smaller intrinsic device capacitances, which leads to much faster switching and lower switching energy losses than their Si counterparts. Furthermore, higher thermal energy is required for electron-hole pairs to be generated and thus off-state leakage current to increase in WBG devices. Therefore, the maximum operating temperature of WBG devices are much higher (i.e. over $500^0$C) compared to Si. It is worth noting that the electron mobility values in GaN can change depending on whether electrons flow in bulk GaN or at the AlGaN/GaN heterointerface as a two-dimensional electron gas (2DEG). The electron mobilities in 2DEG is generally higher compared to that in bulk GaN, as will be discussed in Section 1.4.

Conventional Si-based vertical planar MOSFETs, shown in Figure 1-7(a), are only used in low-voltage applications due to their exponential increase of $R_{ds,on}$ as thicker drift region with lighter extrinsic doping concentration is required for larger BVs; the drift region resistance take up to 95% of the total $R_{ds,on}$ of the 600 V device [38]. This is due to the triangular E-field profile along the drift region, for which its peak occurs at the p-base and n-drift junction. However, the electrical performances of Si-based power MOSFETs have been dramatically improved via introduction of a novel technology, referred to as "Superjunction MOSFETs" (SJ-MOSFETs), which is illustrated in Figure 1-7(b). The fundamental difference between SJ-MOSFETs and vertical planar MOSFETs is their off-state electric field profile. The SJ-MOSFETs utilize charge balance between the n-drift and p-pillar regions throughout the vertical drift length, which flattens out the E-field at the virtue of their breakdown. Hence, its E-field profile becomes rectangular, and BV

increases linearly with drift length [38, 39]. The commercial SJ-based, 650 V-rated CoolMOS devices have exhibited specific $R_{ds,on}$ values that are lower than the theoretical intrinsic Si material limit [40].




(a)




(b)

*Figure 1-7: Cross-sectional view and off-state electric field profile of (a) vertical planar MOSFET, and (b) vertical SJ-MOSFET*

Despite the efforts to enhance the device BV using SJ technology, there are no SJ-MOSFETs with BVs exceeding 900V that are commercially available nowadays. This is primarily due to the increased complexity, time and cost of fabrication of SJ-MOSFETs at higher BVs as p and n columns in SJ structure gets longer in their vertical lengths and number of process steps increase accordingly [41]. As a result, the BV of commercial Si-MOSFETs still remain below 900V. For applications where BV > 900V is required, Si-based Insulated Gate Bipolar Transistors (Si-IGBTs) becomes dominant since its current carrying capability is much higher compared to unipolar Si devices due to the presence of conductivity modulation [42]. When the device is 'on', a large number of majority carriers (electrons) is injected from the n+ emitter via MOSFET channel below the gate into the n-drift region, which lowers the potential of n-drift and hence the junction between P+ substrate and n-drift regions is forward biased. This leads to the injection of minority carriers (holes) from p+ substrate into the same drift region as in BJTs, which leads to a drastic decrease in its forward on-state voltage drop at high current density level (termed as 'conductivity modulation') [43]. Hence, it is widely adopted in applications with multi-kV and few 100 A current where the use of Si-MOSFETs become unfeasible.

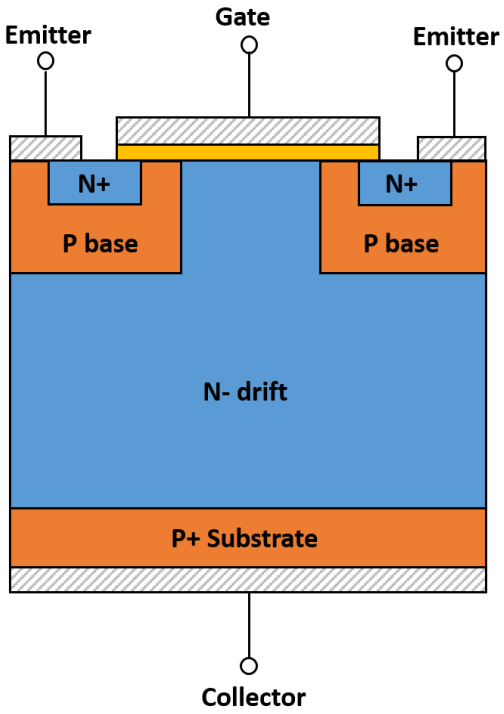



*Figure 1-8: Planar IGBT cross-section and its equivalent circuit*

However, the major drawback of IGBTs is the tail current at its turn-off process. At the initial phase of its turn-off, the internal MOSFET channel is cut off and the collector current falls rapidly. Then the remaining excess electrons will be recombined with the excess minority holes in the drift region, as there are no physical paths available through which carriers can escape. The collector current will decay slowly as according to the minority carrier recombination lifetime in n-drift region, which leads to slow turn-off process and high switching energy loss [44, 45]. As a result, the typical switching frequency range of Si-IGBTs is by an order of magnitude lower than Si-MOSFETs [46].

As discussed earlier, with the use of GaN, the unipolar power devices with higher BV and lower $R_{ds,on}$ and thus power loss by few orders of magnitude than their Si counterparts can be realized. Although large-area GaN power devices are commercially available, their breakdown voltage is limited up to 650 V and hence

they are deemed to be unsuitable for future aerospace systems with dc-link voltage range of few kVs. Recently, a new GaN-based device technology referred to as "Polarisation Super Junction Field Effect Transistors" (PSJ-FETs) that shows similar off-state E-field profile to SJ-MOSFETs have been developed. The operating principles of the PSJ devices are qualitatively explained in Section 2.5. The world's first D-mode large-area GaN PSJ-FETs on Sapphire substrate with a breakdown voltage exceeding 3 kV were manufactured by POWDEC Inc. for the research work presented in this thesis. The BV of GaN power devices were significantly enhanced and they exhibited $R_{ds,on}$*$mm^2$ that were much lower and hence closer to the theoretical $R_{ds,on}$*$mm^2$ limit of intrinsic GaN compared to the commercialized Si and GaN devices [47]; their $R_{ds,on}$*$mm^2$ value is presented and compared against other commercial devices in Section 3.1.1. As a result, the power loss incurred via on-state conduction of the device and hence heatsink requirement are reduced significantly, which paves the way to the high voltage, high-efficiency and high power density converter designs for future aerospace systems.

## *1.3. Research objective and scope*

Despite many potential benefits that GaN can offer, there are challenges to be addressed in order to fully replace Si devices in power converters. One of the major issues that GaN devices face is that they are inherently normally-on or depletion-mode (D-mode) devices. In a half-bridge (HB) configuration, if both top and bottom devices are D-mode, then both of them will be turned on in case their gate drive power supplies are lost. This leads to massive shoot-through current through the HB circuit under high-voltage DC-link and thus destroy the devices, from which safety concerns arise, which will be discussed in Section 4.1. Hence, normally-off or

enhancement-mode (E-mode) devices are more favorable in power electronics field due to their inherent safety.

The main objectives of the research are three-fold:

The first objective is to experimentally assess the switching and on-state current-voltage (I-V) characteristics of POWDEC's large-area PSJ transistors at various device temperatures. These are the key characteristics that determines the total power loss dissipated as heat from the power device and hence the efficiency of the power converter. Since these characteristics are dependent upon the device junction temperature, they were evaluated at various temperature values for accurate prediction of converter efficiency.

The second objective is to design and build a fail-safe gate driving circuit for D-mode GaN devices. As discussed previously, D-mode devices are not preferable in power electronics field due to their inherent safety issues. Nevertheless, they can be used if their safety is fully guaranteed under gate drive supply failure (GDSF) events, which can be achieved by designing gate driving circuits that will keep both devices in HB off when GDSF occurs and eventually isolate the converter from high-voltage (HV) DC-link.

The third objective is to realise the E-mode cascode GaN configuration using low-voltage Si-MOSFET and the large-area GaN PSJ bare dies and compare its on-state and switching performances against its standalone D-mode GaN counterpart. By configuring the device as E-mode, inherent safety concerns of adopting D-mode devices in power electronics can be avoided and thus makes GaN devices preferable for power electronics and simplifies the future converter design.

## *1.4. Thesis Outline*

This thesis is organized as follows:

In *Chapter 1,* a brief overview of the Battery-powered Electric Vehicles (BEVs), More Electric Aircraft (MEA) concept with energy storage system and the need for high-efficiency power electronics are presented. This is then followed by limitations in conventional Si devices and thus the need for next-generation power semiconductor devices using wide bandgap materials (including GaN and SiC) in aerospace applications are highlighted.

In *Chapter 2,* the fundamental properties and physics of GaN-based High Electron Mobility Transistors (GaN-HEMTs) are thoroughly discussed. The device architecture and its limitations are discussed, highlighting the need for an alternative device technology to enhance the breakdown voltage of GaN power devices. In addition, challenges associated with their implementation in power converter circuits are explained in detail.

In *Chapter 3,* the static and dynamic characteristics of a new 3kV GaN-PSJ sample will be presented, including the on-state I-V curves and turn-on/off switching waveforms and energy losses under various junction temperatures. The procedures for obtaining static I-V curves and performing switching tests for GaN will be discussed in detail. Then, the very first cascode GaN-PSJ transistor samples are presented as a E-mode option for voltage-sourced power converters. Its static and dynamic characteristics are obtained by following similar procedures and are compared against their D-mode GaN counterparts.

In *Chapter 4,* a new fail-safe gate drive topology for D-mode GaN transistors is proposed and demonstrated via simulation and experiment. This proves that they

can be applied onto voltage-sourced half-bridge converters with no critical safety concerns during normal operation and gate drive power supply failure condition. The limitations and improvements made from the previous works are clearly identified and discussed in detail.

In *Chapter 5*, detailed procedures of bidirectional DC-to-DC converter design including power loss calculation and selection of passive component values for D-mode PSJ-FETs are presented. The performance validation was carried out using a PSpice simulator that verified the fail-safe operation of the converter under various fault scenarios. An EMI-induced false controller operation during steady-state converter operation at dc-link voltages of up to 300 V was identified and some possible solutions are proposed.

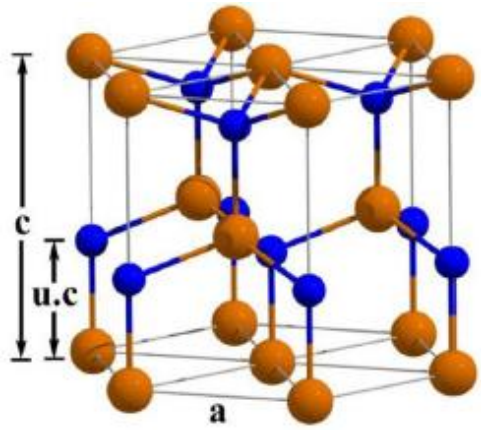
Finally, in *Chapter 6*, concluding remarks are presented and various aspects for future research are identified and discussed in detail.

# 2 Fundamentals of GaN-based Device Technologies

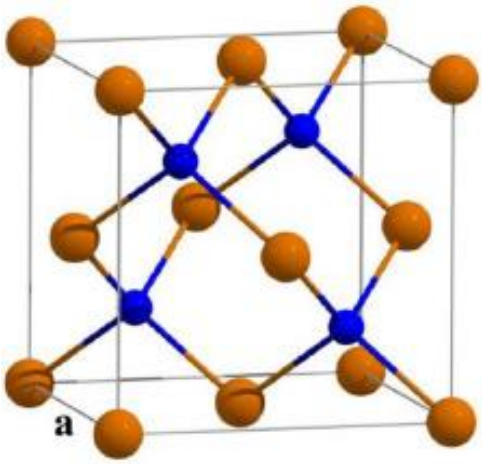
In order to gain fundamental understanding of GaN material properties, physics of GaN device operation and ways to fully exploit their benefits in several applications, several literatures have been reviewed prior to carrying out research. The intrinsic material structure and polarization properties of GaN will be discussed thoroughly first. Then, the conventional AlGaN/GaN High Electron Mobility Transistors (HEMTs) technology will be introduced, and its operating principles and main electrical parameters will be presented. This will be followed by its limitations and an introduction to a recent device technology referred to as "polarization super junction field-effect transistors" (PSJ-FETs). Finally, the effects of parasitic inductances in power converter circuits and ways to mitigate them will be reviewed.

## *2.1. GaN material structure and spontaneous polarisation*

GaN is one of the most extensively researched binary III-V compound semiconductor materials, along with SiC. It has three different crystal structures: wurtzite, zinc blende and rock salt structures. These structures are illustrated in Figure 2-1(a)~(c). Amongst these structures, wurtzite structure is the most thermodynamically stable structure under standard ambient condition [48].




(a)

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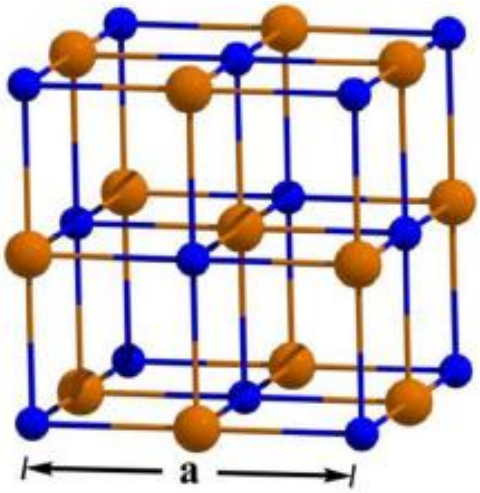



(c)

*Figure 2-1: Common GaN crystal structures: (a) wurtzite, (b) zinc-blende, and (c) rock-salt; the Ga and N atoms are indicated in brown and blue, respectively [48]*

When two distinct atoms form crystal bonds in III-V binary compound materials, their differences in electronegativities (defined as the measure of tendency of the material to attract electrons towards itself) leads to a net polarization. If the crystal is non-centrosymmetric, a net macroscopic polarization will be induced via the dipole [49, 50]. In a cubic crystal structure, the dipole moments in the bonds will cancel each other out, which yields net polarization of zero when no strain is applied externally. The same applies to an ideal III-V compound wurtzite and zinc blende crystal structures where net dipole moments become zero. In real III-V semiconductor materials, on the other hand, the atoms are arranged such that net dipole moment exists even when no external strain is applied due to deviation from its ideal crystal structure; this is referred to as "spontaneous polarisation" [49, 50]. The direction of this net polarization depends on the direction of the material crystal growth indicated in Figure 2-2. For Ga-faced GaN layer, the polarisation will be oriented along [0001] direction whereas it will be directed in [000-1] direction in N-faced GaN [51].

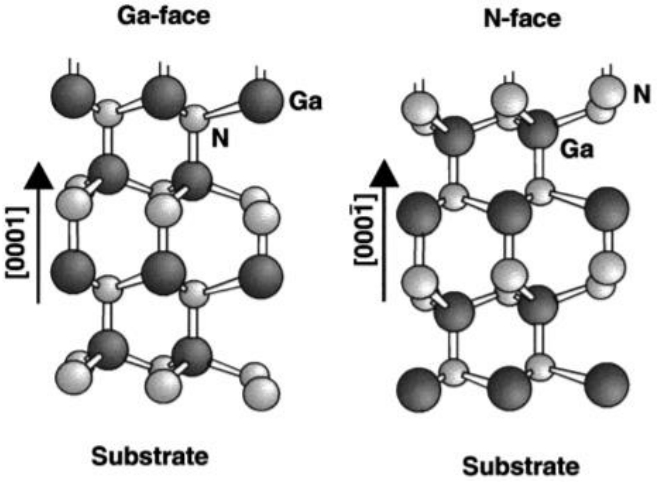



*Figure 2-2: Schematics of crystal structure of wurtzite GaN with spontaneous polarization vector orientation for Ga-faced and N-faced GaN [51]*

The spontaneous polarization inherently present in the real III-V nitrides' wurtzite crystals has strong dependence on alloy composition (x). This is due to variations in cell-internal parameters such as band-gap, which may be attributed to variations in anion-cation electronegativities, disorder effects due to random distribution of chemical elements on cation side and internal strain effects arising from variations in anion-cation bond length [52]. The magnitude of induced spontaneous polarization (in $C/m^2$) as a function of x in ternary compound nitride materials can be interpolated using the following second-order quadratic equation and plotted in Figure [49, 53]:

$$P_{A_xB_{1-x}N}{}^{SP}(x) = P_{AN}{}^{SP}x + P_{BN}{}^{SP}(1-x) + b_{ABN}x(1-x) \qquad \ldots(2\text{-}1)$$

Where A and B are group-III elements and $b_{ABN}$ is the bowing parameter defined as the following [53]:

$$b_{ABN} = 4P_{A_{0.5}B_{0.5}N}{}^{SP} - 2\left(P_{AN}{}^{SP} + P_{BN}{}^{SP}\right) \qquad \ldots(2\text{-}2)$$

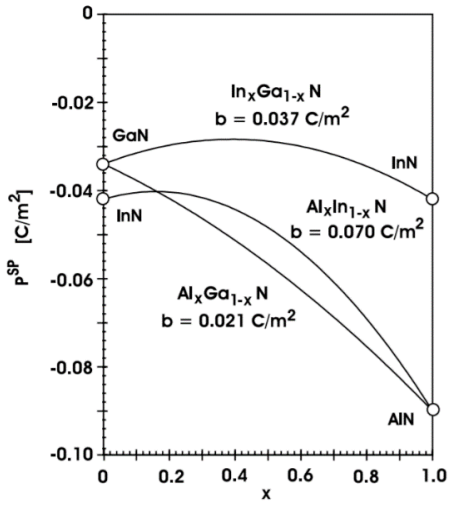



*Figure 2-3: Spontaneous polarization present vs. Al/In mole fraction (x) for AlGaN, InGaN and AlInN [49]*

## *2.2. Piezoelectric polarization in AlGaN/GaN heterostructure*

The net polarisation in III-V nitride materials will also be altered when they are subject to mechanical strain, which may occur when two materials with different lattice constants are pseudomorphically grown onto one another. This component of polarization is referred to as "piezoelectric polarization", calculated as [54]:

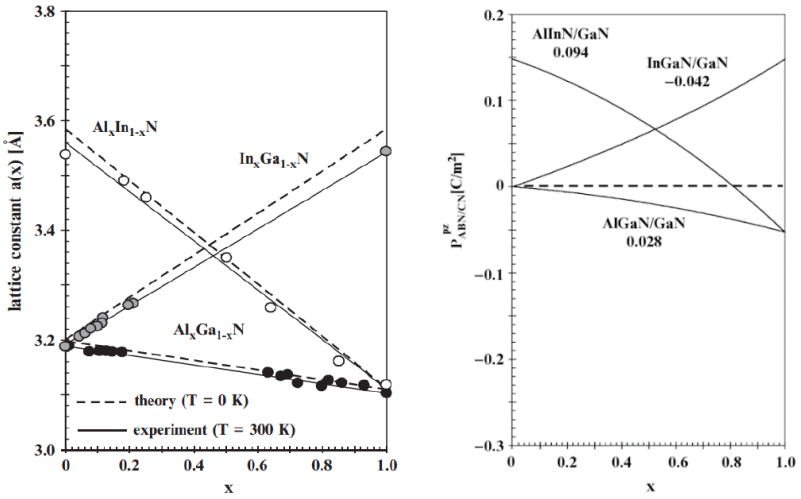
$$P_{pz} = 2\left(e_{31} - e_{33}\frac{C_{13}}{C_{33}}\right)\cdot\varepsilon \qquad \ldots(2\text{-}3)$$

Where $C_{13}$ and $C_{33}$ are elastic constants, $e_{31}$ and $e_{33}$ are piezoelectric moduli and ε is the in-plane strain in the crystal expressed as

$$\varepsilon = \frac{a-a_0}{a_0} \qquad \ldots(2\text{-}4)$$

Where a and $a_0$ are the lattice constants of the strained and originally relaxed material layer, respectively.

As according to the equation, the magnitude of piezoelectric polarization is proportional to the in-plane strain that is dependent on lattice constant mismatch. The lattice constant varies with alloy composition of ternary compound materials such as AlGaN, InAlN and InGaN, as plotted in Figure 2-4(a). Accordingly, the piezoelectric polarization induced via lattice mismatch also varies with mole fraction as shown in Figure 2-4(b) [52]. In AlGaN/GaN heterostructure, for instance, the AlGaN layer experiences tensile strain as its lattice constant is smaller than the underlying GaN layer.




(a) (b)

*Figure 2-4: (a) Lattice constant vs. AlN/InN mole fraction for random ternery alloys of group-III Nitride materials, (b) Piezoelectric polarization magnitude vs. AlN/InN mole fraction of ternery alloys grown on relaxed GaN buffer layers [52]*

The direction of piezoelectric polarization is dependent upon direction of crystal growth. For Ga-faced GaN layer, the cumulative z-component of the polarization in [0001] direction will decrease and thus net polarization is oriented towards [000-1] direction; For N-faced GaN, it will be the opposite. These are illustrated in Figure 2-5. The exact opposite will occur when compressive strain is applied.

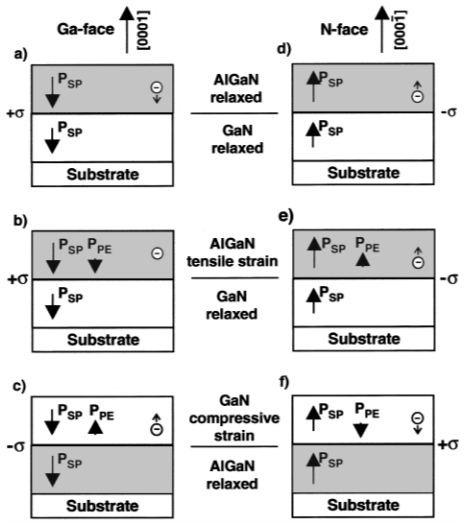



*Figure 2-5: Directions of spontaneous and piezoelectric polarization ($P_{SP}$ and $P_{PE}$) in Ga-faced and N-faced AlGaN/GaN heterostructures [54]*

## *2.3. Polarisation charge formation in AlGaN/GaN heterointerface*

A fixed charge is induced at the AlGaN/GaN heterointerface via combination of spontaneous and piezoelectric polarization in AlGaN/GaN heterostructures. The lattice constant of AlGaN layer is primarily dependent upon Al mole fraction. This, in turn, alters the lattice mismatch between AlGaN and GaN layers and thus mechanical strain and magnitude of piezoelectric polarization. This yields difference in magnitude of polarization between two layers of the heterostructure and thus abrupt change in polarization from one layer to another at the interface. As a result, a fixed charge is induced at the interface, and its density can be expressed as the following [51]:

$$\sigma = P_{top} - P_{bottom} = \left(P_{SP,top} + P_{PE,top}\right) - \left(P_{SP,bottom} + P_{PE,bottom}\right) \quad \ldots(2\text{-}5)$$

Where $P_{SP,top(bottom)}$ and $P_{PE,top(bottom)}$ are spontaneous and piezoelectric polarization present in top (bottom) layer, respectively.

If the polarization induced sheet charge density (σ) is positive, then free electrons can be accumulated and thus form 2DEG at the heterointerface in order to maintain net charge neutrality. By same principle, 2DHG may be formed when GaN is grown on a relaxed AlGaN layer as compressive strain is applied at the GaN layer and thus the net σ becomes negative [55].

## *2.4. GaN High Electron Mobility Transistors (HEMTs)*

The first heterostructure-based semiconductor device was introduced using AlGaAs and GaAs few decades ago [56]. As illustrated in Figure 2-6, it consists of Si-doped n-type AlGaAs, undoped AlGaAs spacer and undoped GaAs layers grown

on top each other. The 2-dimensional electron gas (2DEG) is formed at undoped AlGaAs/GaAs heterointerface as electrons at n-AlGaAs layer is transferred to and confined at the quantum well present at the interface. The undoped AlGaAs spacer layer serves to isolate the 2DEG from dopant impurities at n-AlGaAs and therefore reduce the Coulombic scattering and hence lead to extremely high electron mobility. The 2DEG density is primarily controlled by changing the doping concentration in n-AlGaAs layer and can also be adjusted by varying the spacer layer thickness. According to the analysis using Poisson's equation with an assumption that the spacer layer is completely depleted in [57, 58], the sheet 2DEG charge density can be expressed in terms of spacer layer thickness and n-doping concentration as:

$$en_s = \sqrt{2e\varepsilon_0\varepsilon_s N_D v + e^2 {N_D}^2 (d_0 + \Delta d)^2} - eN_D(d_0 + \Delta d) \quad \ldots(2\text{-}6)$$

Where $N_D$ = doping concetration in n-AlGaAs layer, e = electron charge, $d_0$ = spacer layer thickness, Δd = modified constant (80Å approx.) when changes in Fermi level with respect to sheet 2DEG density is taken into account and v = band bending = $\frac{\Delta E_c - \delta - E_F}{e}$ in which $\delta$ = energy difference between conduction band edge of AlGaAs and Fermi level ($E_F$) and $\Delta E_c$ = conduction band offset [59].

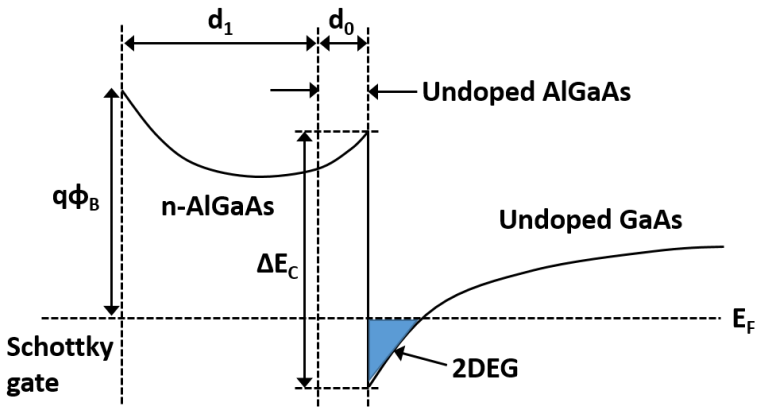



*Figure 2-6: Conduction band energy diagram in AlGaAs/GaAs heterostructure*

As according to the equation, the 2DEG density decreases as the spacer layer thickness increases. As a result, there exists a tradeoff between enhancing electron mobility and reducing 2DEG density while increasing the spacer thickness and thus a certain value of thickness can be found for achieving optimum performance.

Nevertheless, AlGaAs/GaAs HEMTs were deemed unsuitable for high-power or high-voltage applications as the bandgap of GaAs and thus their breakdown voltage is limited. As shown in Table 1-1, GaN has ~2.4 times wider bandgap and thus 10 times higher breakdown electric field and higher operating temperature compared to GaAs, which makes it suitable for high-voltage applications and potentially high temperature applications. With the development of wide band-gap III-V compound materials such as GaN, the AlGaN/GaN heterostructure became one of the steps towards realizing WBG semiconductor devices with good electrical performances. Although this is analogous to the AlGaAs/GaAs heterostructure developed previously, its operating physics are fundamentally different, which will be discussed in the following section.

### *2.4.1. Source of 2DEGs in GaN-HEMTs*

In order to optimize the performance of GaN-HEMTs, it is crucial to thoroughly understand and control the source of electrons in the device. A theoretical analysis of the origin of 2DEG and its density and comparison with experimental Hall data was carried out in [60]. The study has identified the 'surface states' in AlGaN as a major source of electrons based on electrostatics analysis in AlGaN/GaN energy band diagram in Figure 2-8. It revealed that sheet 2DEG density ($n_s$) starts to be formed only when the AlGaN barrier thickness exceeds critical thickness of 3nm. If the surface states are sufficiently deep, then its energy

level will lie below $E_F$ and thus they are fully occupied and $n_s$=0. As a result, a constant electric field exists in AlGaN due to unscreened polarization dipole. The critical AlGaN barrier thickness ($t_{cri}$) for 2DEG formation can be obtained as following [60]:

$$t_{crit} = \frac{(E_D - \Delta E_C) \cdot \varepsilon}{q\sigma_{PZ}}$$

…(2-7)

Where $E_D$ = surface donor energy, $\Delta E_C$ = conduction band offset between AlGaN and GaN and $\varepsilon$ is the absolute permittivity of AlGaN.

When $t_{AlGaN}=t_{crit}$, the surface donor level reaches the $E_F$ and thus electrons can be transferred from surface states to the empty conduction band states at AlGaN/GaN heterointerface, leaving partially empty surface states with positive charge. The surface states may arise from alloy disorder and nitrogen vacancies [61, 62]. This hypothesis is well illustrated in Figure 2-7(a)~(c).

As $t_{AlGaN}$ exceeds $t_{crit}$, the 2DEG density can be expressed as:

$$n_s = \frac{\sigma_{PZ}(1 - t_{crit}/t_{AlGaN})}{q}$$

…(2-8)

Where q=electronic charge and $\sigma_{PZ}$ is piezoelectric charge induced at AlGaN/GaN. With further increase in $t_{AlGaN}$, the 2DEG density will saturate towards $\frac{\sigma_{PZ}}{q}$. In other words, the electric field in AlGaN layer, which is proportional to $qn_s - \sigma_{PZ}$, approaches to zero for $t_{AlGaN} >> t_{crit}$ as the polarization dipole is steadily screened via ionized surface states and electrons in 2DEG. However, an upper limit exists in increasing $t_{AlGaN}$ as 2DEG density and mobility starts to drop at a certain thickness

due to strain relaxation via crack formations in AlGaN/GaN heterointerface [63]. The thickness at which this occurs is inversely proportional to the Al mole fraction [64].

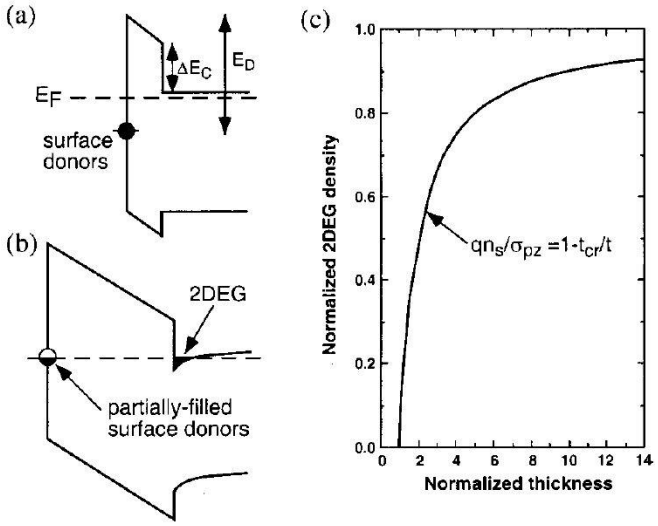



*Figure 2-7: Energy band diagram illustrating the surface donor model in AlGaN/GaN heterostructure with AlGaN barrier thickness (a) less than, (b) greater than the critical thickness for 2DEG formation and (c) Calculated 2DEG density vs. AlGaN thickness using the surface donor model [60]*

As discussed earlier, the polarization-induced charges form a dipole and thus their net contribution to the net charge is zero. The sum of all space charges within the structure must be zero to maintain charge neutrality, which yields the following equation [60]:

$$\sigma_{surface} + \sigma_{AlGaN} - en_s = 0 \qquad \ldots(2\text{-}9)$$

Where $\sigma_{surface}$ is the charge due to ionized surface states, $\sigma_{AlGaN}$ is the charge due to ionized donors in AlGaN, e is the electron charge and $n_s$ is 2DEG sheet electron density.

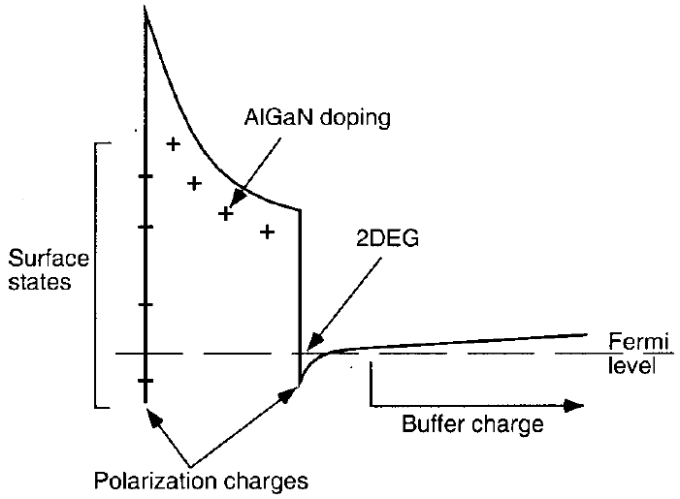



*Figure 2-8: Conduction band diagram for AlGaN/GaN heterostructure with various space charge components [60]*

### *2.4.2. Operating principles of GaN-HEMTs*

The polarisation property in AlGaN/GaN heterostructure is the foundation of realizing conventional GaN-HEMT devices; its schematic diagram is shown in Figure 2-9(a). It consists of a non-native substrate, nucleation layer to avoid cracks due to large lattice mismatch between undoped GaN layer and substrate material, GaN/AlGaN heterojunction at which 2DEG is formed via polarization, ohmic drain and source contacts and a Schottky gate contact with a Schottky barrier height, $\Phi_B$, which determines the turn-on threshold gate voltage ($V_{gs,th}$). The nucleation layer consists of multiple layers of AlGaN with different Al mole fraction or a single GaN/AlN layer, depending on the type of substrate material onto which GaN is to be grown. Based on the polarization theory discussed in previous section, the operating principles of GaN-HEMTs can be described as following:

1. When no gate voltage supply is present (i.e. $V_{gs}$=0V), the device is in its 'on' state due to the spontaneous formation of 2DEG at AlGaN/GaN heterointerface

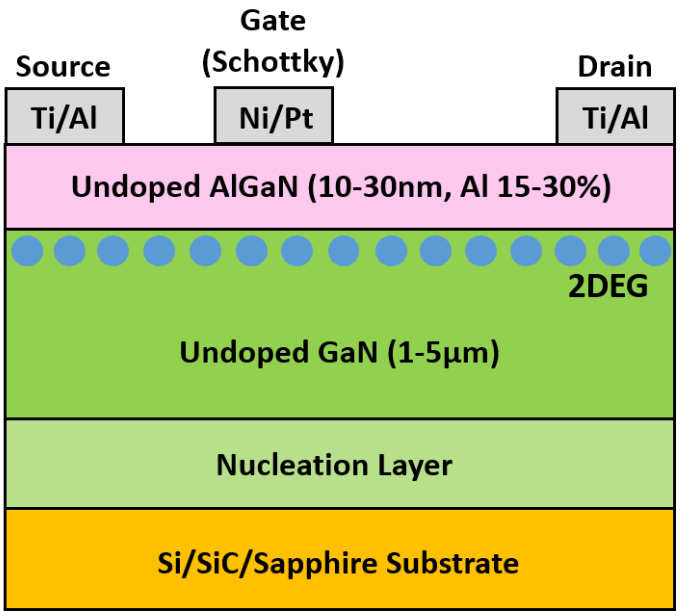
as shown in the conduction energy band diagram in Figure 2-9(b) and thus current can flow from drain to source and it operates as a D-mode device.

2. When positive gate bias is applied (i.e. $V_{gs} > 0$ V), the conduction energy band is pulled further down towards the Fermi level ($E_F$) and thus the 2DEG concentration and drain current would increase.
3. When negative gate bias is applied (i.e. $V_{gs} < 0$ V), the conduction energy band shifts further up above the $E_F$ as shown in Figure 2-10 and thus 2DEG concentration and drain current output would decrease. If $V_{gs} < V_{gs,th}$, then the 2DEG will be depleted below the Schottky gate region and thus the device is now turned OFF.
4. When the gate is 'floating' i.e. disconnected from the gate drive voltage, then the gate drive loop becomes an open-loop circuit. Since extremely high impedances are present in the internal gate-to-source and gate-to-drain junctions of the device, the $dV_{ds} / dt$ noise that occurs when the $V_{ds}$ rises up to a fixed dc-link voltage ($V_{dc}$) during the initial start-up of the power converter would be coupled via gate-to-drain capacitance, $C_{gd}$. Therefore, assuming that $C_{gd}$ and gate-to-source capacitance ($C_{gs}$) values remain constant with $V_{ds}$ and $V_{gs}$ biases, the gate-to-source voltage would float to a value determined by the capacitive voltage divider network and initial $V_{gs}$ value when the gate starts to float ($V_{gs,init}$):

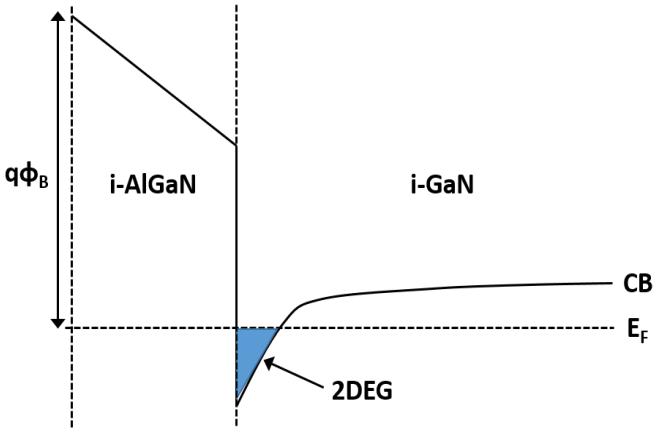
$$V_{gs,float} = \frac{V_{dc} \cdot C_{gd}}{C_{gd} + C_{gs}} + V_{gs,init} \quad \ldots(2\text{-}10)$$

Hence, even if the $V_{gs}$ of the device is initialised to a negative value to hold the device to its 'off' state, the $V_{gs}$ will float up to a value that would exceed its turn-on threshold gate voltage and hence the device would inadvertently be turned on [65]. As the device is subject to a high $V_{dc}$ and it cannot be turned off due to the floating gate terminal, the device would eventually fail destructively unless the

other means of device over-current protection are present. Therefore, leaving the gate terminal floating must always be avoided.

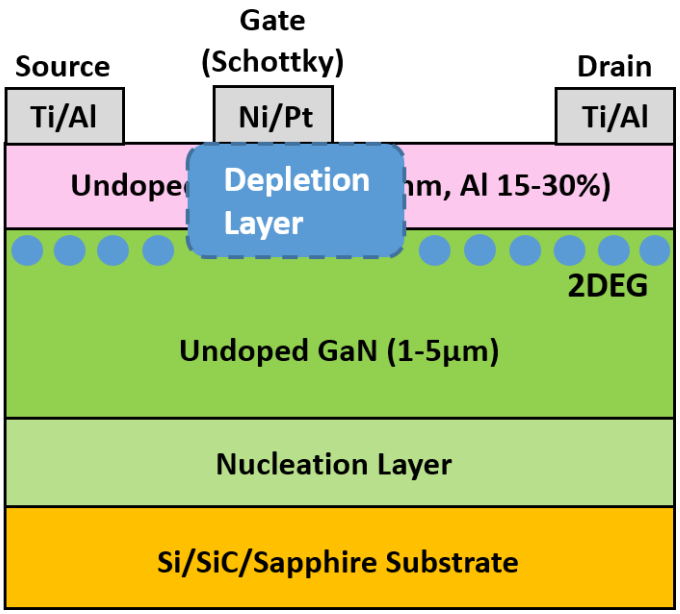



(a)

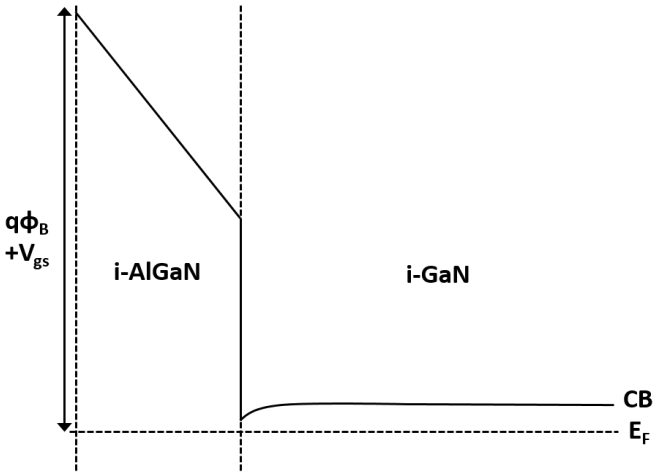



(b)

*Figure 2-9: (a) Schematic diagram of conventional GaN-HEMT and (b) Conduction energy band diagram in conventional GaN-HEMT under zero gate bias*




(a)




(b)

*Figure 2-10: (a) Schematic diagram of conventional GaN-HEMT and (b) Conduction energy band diagram in conventional GaN-HEMT under off-state with negative gate bias*

### *2.4.3. Substrate material selection*

Currently, there is a lack of high quality, large-scale and affordable bulk GaN wafers and therefore GaN devices on GaN substrates are not available in the semiconductor market today [60]. The substrate materials can be any of the following: Si, SiC, GaN, Sapphire or Diamond. The most widely used substrate material for GaN-HEMTs is Si, due to affordable, high quality large-dimension Si

wafer production technologies [66, 67]. The SiC exhibits higher thermal conductivity than Si or GaN, as can be observed in Table 1. Therefore, GaN-on-SiC is used in applications (such as RF devices for satellite and radar communications etc.) where good thermal dissipation becomes crucial for smaller cooling system. It also has the least lattice mismatch with GaN, which significantly reduces the defects within the device and thus better device reliability [68]. However, manufacturing cost of SiC wafers is much more expensive than that of Si. Should GaN epitaxial layers be grown on foreign substrate materials including Si, Sapphire and Diamond, then lattice mismatch becomes inevitable and thus larger number of defects compared to GaN grown on GaN substrate is present [69].

### *2.4.4. Electric field management issues*

During its off-state, the electric field is crowded at the drain side of the gate edge, as shown in Figure 2-11. This is due to the charge accumulation at the gate edge and presence of positive polarization charges at the heterointerface. Since the breakdown voltage (BV) of the device under off-state is equivalent to the integral of electric field along channel direction and electric field must not exceed a critical value to prevent avalanche breakdown, the achievable BV of lateral AlGaN/GaN HEMTs is severely limited.

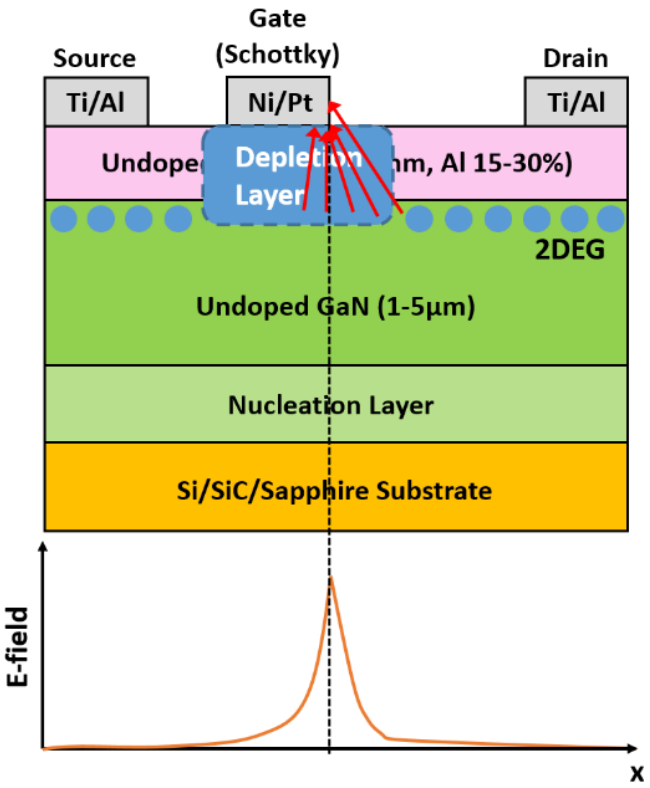
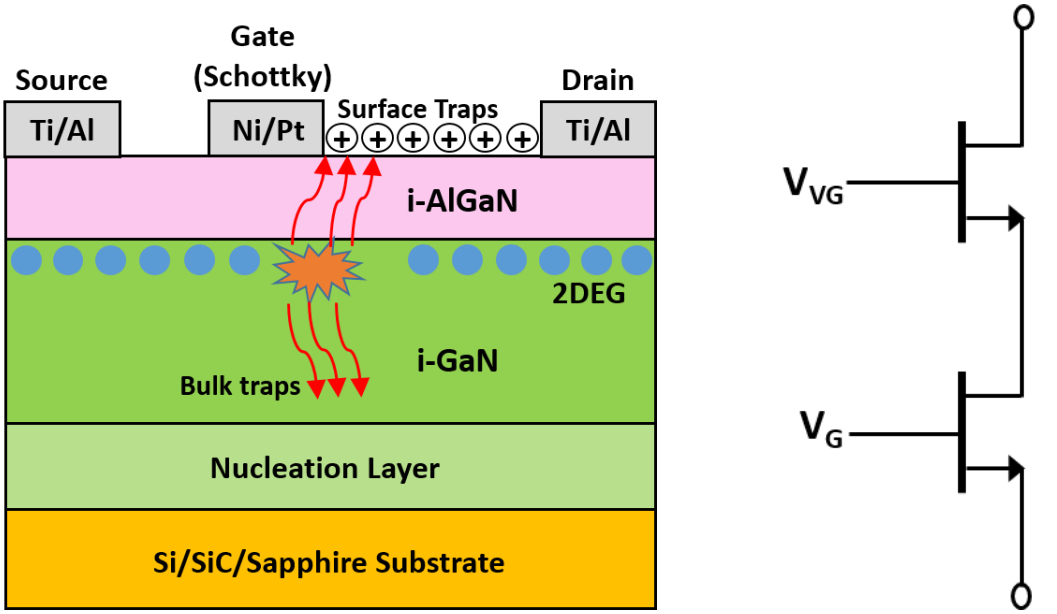



*Figure 2-11: Electric field crowding in lateral GaN-HEMTs under off-state*

### *2.4.5. Current collapse issues*

The current collapse phenomenon is illustrated in Figure 2-11. Due to the high electric field present at the drain side of the gate edge, the electrons in 2DEG will be accelerated and thus highly energized during switching operations under high voltages. Therefore, they will be captured by bulk and surface traps, which makes the surface charge negative and thus depletes the 2DEG channel due to charge neutrality [70]; this is well illustrated in Figure 2-12. The depletion region under the gate will thus be extended as negative surface charge (represented as $-\sigma_{trapped}$ in Figure 2-12) behaves as a negatively biased "virtual gate" and thus the $R_{on}$ of GaN-HEMT is increased temporarily even when the device is 'on' after a high-voltage DC bias stress. The time required for its $R_{on}$ to be recovered is solely dependent upon surface electron detrapping time, $T_{detrap}$ and hence its change in

drain current output depends on the relationship between input signal frequency and $T_{detrap}$ [71]. This affects the reliability of the device operation in power converters and therefore must be addressed.




(a) (b)

*Figure 2-12: (a) Current collapse phenomenon in lateral GaN-HEMTs due to the presence of peak electric-field at drain side of the gate edge and traps at unpassivated AlGaN surface, (b) Schematic representation of GaN-HEMT including the series virtual gate*

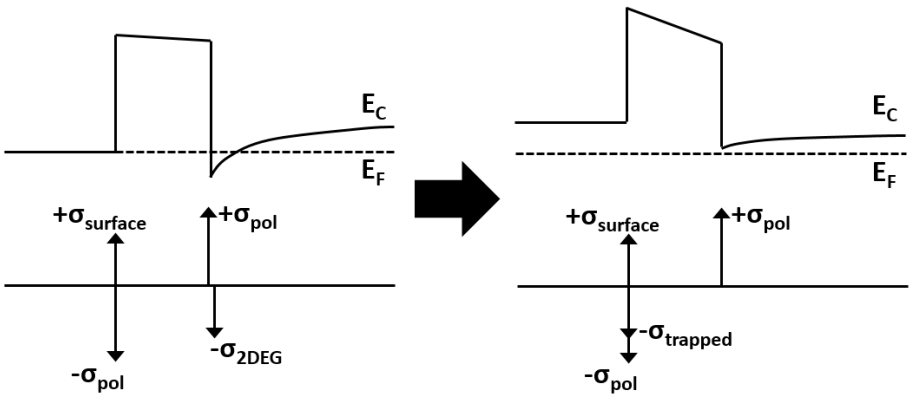



*Figure 2-13: Energy band diagram of AlGaN/GaN heterostructure indicating a transition to a negatively charged virtual gate causing current collapse phenomenon*

### *2.4.6. Field-Plate structure*

In order to address the current collapse issue and enhance the BV of lateral GaN-HEMTs, a field-plate (FP) structure has been implemented as according to Figure 2-14. The source FP is designed so that its edge is closer to the drain than the gate so that the peak electric field at the gate edge is alleviated [72]. The source and drain ohmic contacts are realised via mesa etching using reactive ion beam etching that is followed by electron beam evaporation of Ti/Al [72] or Ti/Al/Ni/Au [73] multilayers. The FP metals consist of either Ti/Al [72] or Ti/Au [73]. With the presence of FPs, E-field crowding at the drain side of gate edge is mitigated and thus current collapse is suppressed. Also, the BVs of GaN-HEMTs can be controlled by scaling the FP length.

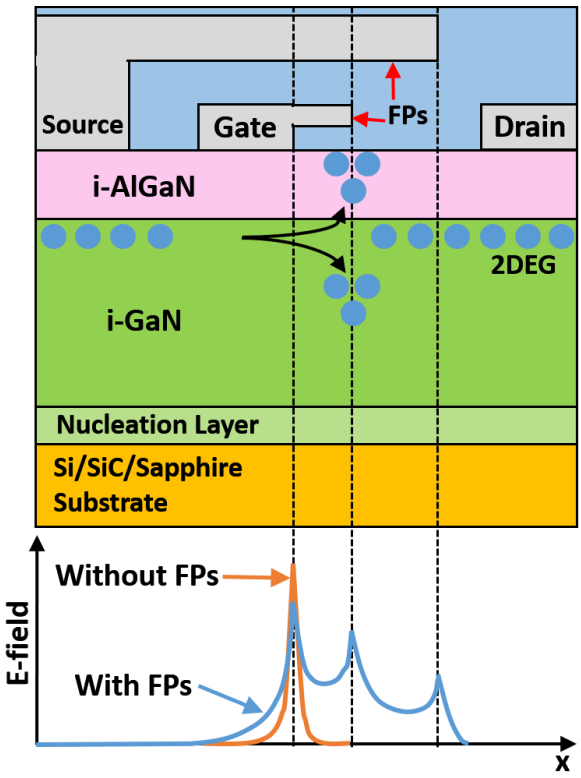



*Figure 2-14: GaN-HEMT with field plate structure and its off-state electric field profile*

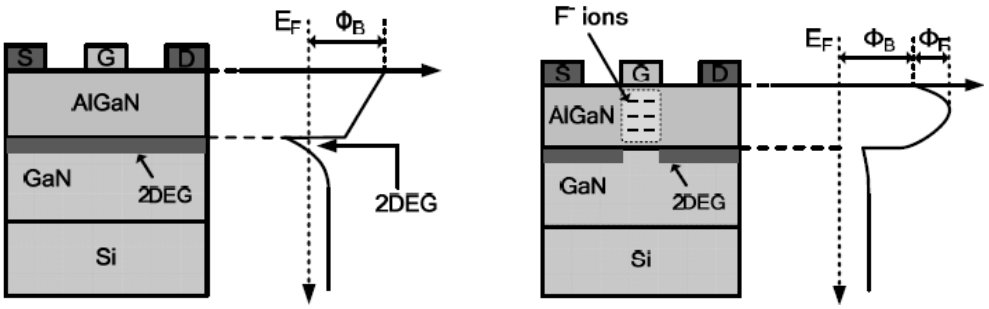
However, the peak E-field is not eliminated completely and thus a limit exists in enhancing their BVs. Also, as FP becomes longer, it becomes closer to the drain

electrode and thus the BV is limited by dielectric breakdown of the surface passivation material [74]. In addition, larger device terminal capacitances will be present and thus high-frequency performance of the device will be compromised [73, 75].

### *2.4.7. E-mode GaN device technologies*

Due to the spontaneous 2DEG formation polarization-induced charge in AlGaN/GaN heterostructure, the GaN-HEMTs are inherently "normally on" or depletion-mode (D-mode) device. However, in power electronics applications, normally-off or enhancement-mode (E-mode) operation is much more preferable due to safety concerns in D-mode operation. Therefore, many research have been carried out to realise E-mode operation with GaN-HEMTs using four different technologies:

1. Flouride ($F^-$) ion implantation: The E-mode operation can be achieved by implanting $F^-$ ions beneath the gate region via $CF_4$ plasma treatment [76]. As $F^-$ ions have higher electronegativity than any chemical elements and thus captures free electrons and form immobile negative charges in the AlGaN barrier layer, the 2DEG beneath the gate is depleted under zero bias. This is illustrated in Figure 2-15. The shift in turn-on threshold gate voltage is dependent upon implantation time and RF plasma treatment power. There exists a compromise between increasing RF plasma power for significant $V_{th}$ shift and minimising plasma-induced lattice damages [77].




(a) (b)

*Figure 2-15: Cross-sectional view of (a) conventional D-mode GaN-HEMTs, and (b) E-mode GaN-HEMTs with $F^-$ ion implantation [77]*

However, $F^-$ ions can reach the 2DEG channel region and deep into the GaN bulk layer; thus, they can cause significant scattering of electrons and thus electron mobility is decreased. This leads to a compromise in its on-state performance of the device including transconductance and on-state resistance [78, 79].

2. Recessed Gate: The E-mode operation of GaN-HEMTs can also be achieved by selectively etching the AlGaN barrier layer beneath the gate [80]. As barrier layer becomes thinner, the 2DEG under the gate region is depleted and thus positive gate voltage is required for the device to be turned on. However, E-mode operation is realised at the cost of reduced electron mobility under recessed gate due to etching-induced lattice damages that leads to more electron scattering [81, 82]. Also, precise control of etching rate uniformity on a large area becomes critical for good reproducibility.

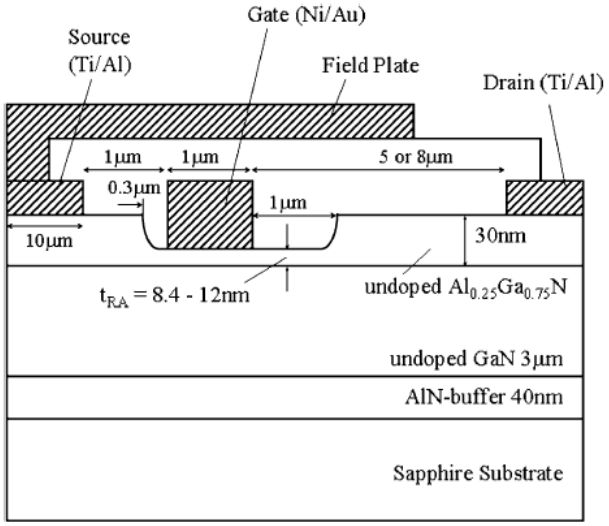



*Figure 2-16: Cross-sectional view of lateral GaN-HEMT with recessed gate [80]*

3. Metal-Insulator-Semiconductor (MIS) HEMT: The E-mode operation of GaN-HEMT may also be achieved by using MIS structure illustrated in Figure 2-17. The AlGaN barrier layer beneath the gate is completely removed and an insulating material ($SiO_2$ or SiN) for surface passivation is deposited on its surface [83, 84]. Therefore, the device operates as E-mode MOSFET. The quality of insulator/ semiconductor interface plays a critical role in transistor's performance. However, no native oxides for III-V nitride materials have been present to date [85]. The etching-induced defects and interface states leads to increased 2DEG scattering and thus reduced 2DEG mobility and larger $R_{on}$ [86].

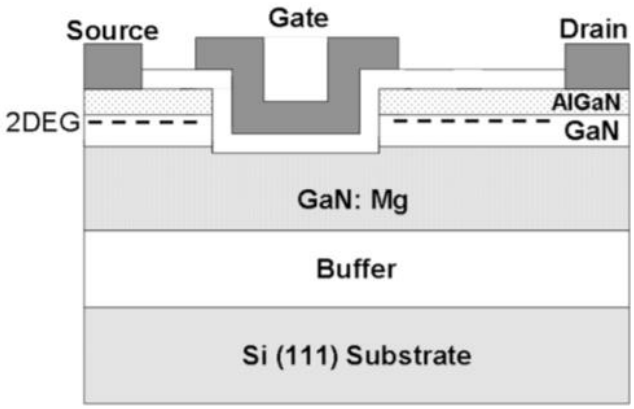
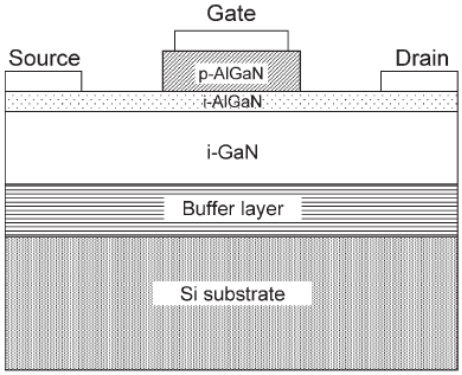
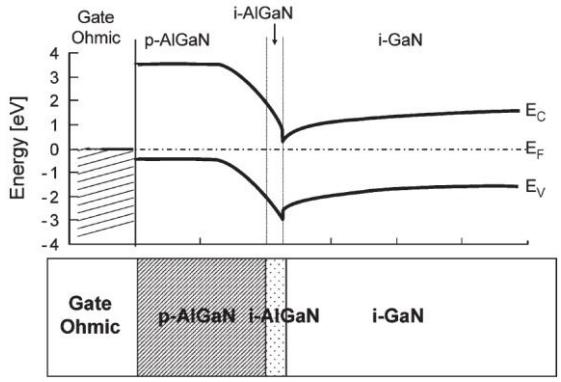


*Figure 2-17: Cross-sectional view of GaN MIS-HEMT structure [84]*

4. Gate Injection Transistor (GIT): Instead of etching the gate region, growing an additional p-type GaN or AlGaN onto the AlGaN barrier layer will raise the conduction band energy and thus deplete the 2DEG under the gate; thus, the GaN-HEMT becomes E-mode device [87]. The cross-sectional view of GIT and energy band diagram are shown in Figure 2-18. This E-mode device GaN technology is adopted in the commercial large-area GaN-HEMT products of GaN Systems Inc [88]. However, this requires selective removal of p-(Al)GaN region via plasma etching, which may damage the AlGaN surface and thus degrade electrical properties of 2DEG in the device access region [89]. Furthermore, a high doping acceptor concentration of p-type AlGaN or GaN layer is required, but achieving p-type conductivity in GaN or AlGaN has been a major challenge. The reference p-type dopant for GaN and AlGaN is Magnesium (Mg) as it substitutes Ga lattice and behaves as an acceptor when incorporated in N lattice. Nevertheless, their activation / ionisation energy is relatively high and thus it becomes difficult to obtain high hole concentration in GaN or AlGaN [90, 91].




*(a)*




*(b)*

*Figure 2-18: (a) Cross-sectional view of GIT structure, (b) GIT energy band diagram under zero gate bias [87]*

5. Cascode GaN: As according to the previous discussions, the device performance may get compromised for modifying D-mode GaN-HEMT structure to become E-mode device. Alternatively, the device may be arranged as cascode with E-mode, low-voltage Si-MOSFETs according to Figure 2-19. By this method, the threshold gate voltage value is solely dependent upon the Si-MOSFET characteristics [92]. Also, the GaN-HEMT performance is not compromised as no etching or ion implantation is involved. Nevertheless, this configuration requires extra bonding wires for packaging two devices onto one substrate, which leads to additional parasitic inductances and thus compromise in device switching reliability [93]. In addition, as D-mode GaN gate is connected to Si-MOSFET source, less flexibility in controlling the device's switching speed exists as its slew rate cannot be controlled by adjusting the total gate resistance present at its gate drive loop [94].

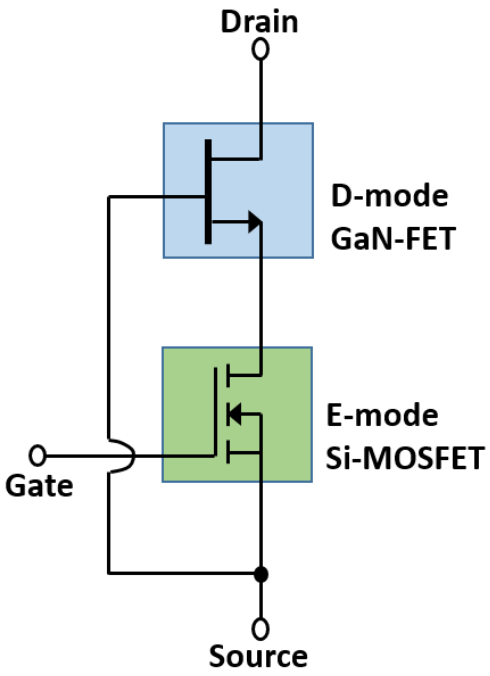


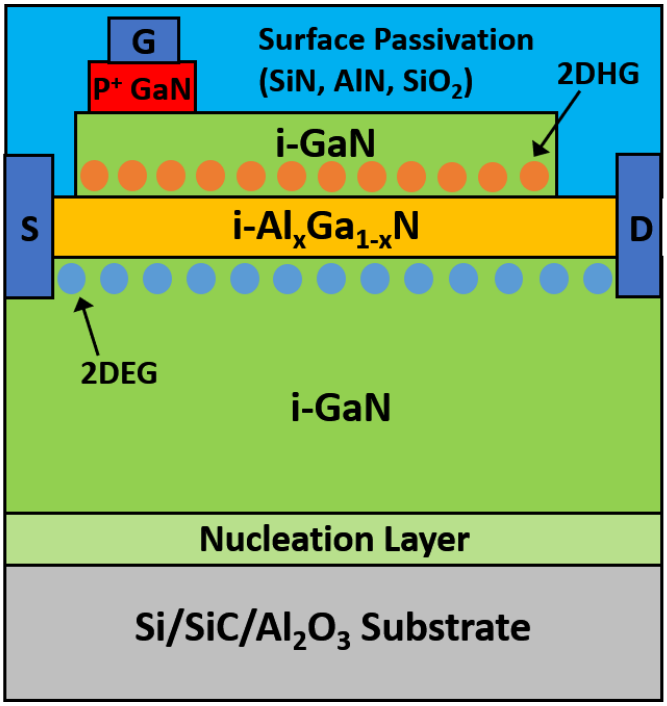

*Figure 2-19: Schematic of E-mode Cascode GaN configuration*

## *2.5. GaN Polarisation Super Junction Field Effect Transistors*

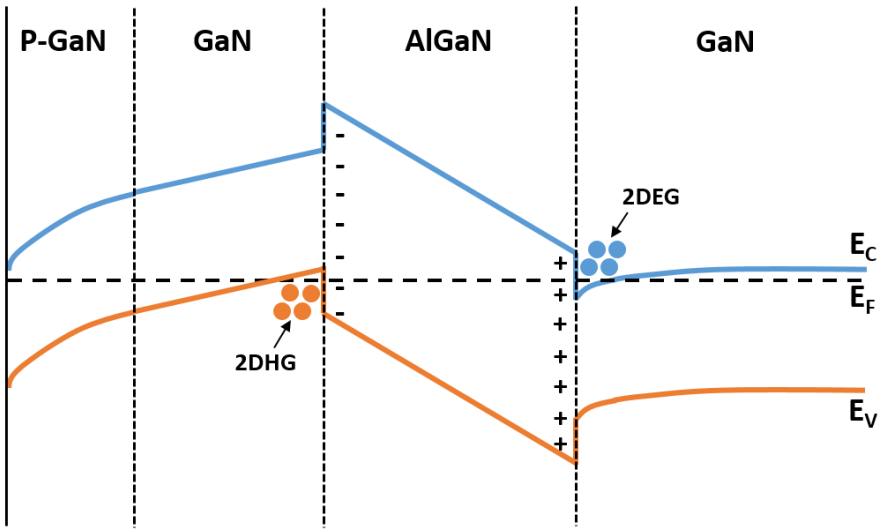
As discussed previously, GaN-HEMTs face non-uniform E-field distribution issues that limits their BVs and facilitates current collapse. Although the FP structure illustrated in Figure 2-14 has partially mitigated this issue, the peak E-field at the gate edge still exists and therefore the full potential that GaN offer is still yet realised. Theoretically, this can be overcome by adopting SJ structure in GaN-HEMTs just like Si SJ-MOSFETs. This requires precise control of p-pillar and n-drift doping densities. However, precise p-type doping control in GaN has been extremely difficult due to the high activation of Mg typically used for its p-dopant [91]. To overcome this issue, a new GaN device technology referred to as "Polarisation Super-junction Field Effect Transistor" (PSJ-FET) was proposed in [95] and its cross-sectional view is shown in Figure 2-20. The superjunction is

formed by GaN/AlGaN/GaN double heterostructure throughout the lateral channel. Without any intentional doping, the 2-dimensional hole gas (2DHG) and 2DEG are formed via negative and positive polarization charge at heterointerfaces, respectively, as per energy band diagram in Figure 2-20(b). When the device is 'on', the current will flow from drain to source via 2DEG as in conventional HEMTs. As the current can flow under the absence of gate voltage supply (i.e. 0V), this is a D-mode device. Thus, to turn the device off, a negative $V_{gs}$ is required so that 2DEG channel gets depleted.

The base or gate electrode forms an ohmic contact to the top p-GaN cap layer. As the densities of positive and negative charges can be perfectly matched, a high charge balance condition could be achieved [96]. As a result, the whole drift region gets depleted under off-state and increase in drain voltage and thus uniform E-field distribution can be achieved as illustrated in Figure 2-21 [47]. As a result, the BV capability is remarkably enhanced compared to conventional lateral GaN-HEMTs, as illustrated by off-state I-V curves in Figure 2-22 [97].




(a)




(b)

*Figure 2-20: (a) Schematic of PSJ-FET structure, (b) Energy band diagram*

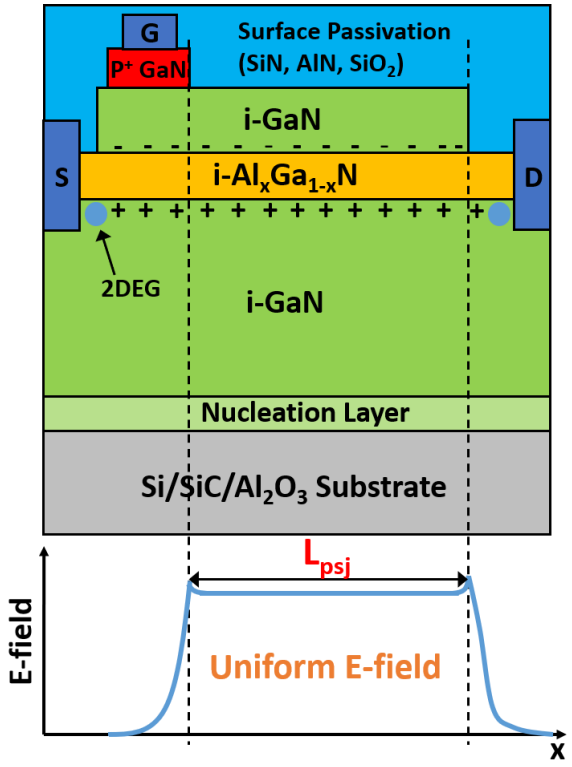



*Figure 2-21: Off-state electric field profile in PSJ-FET*

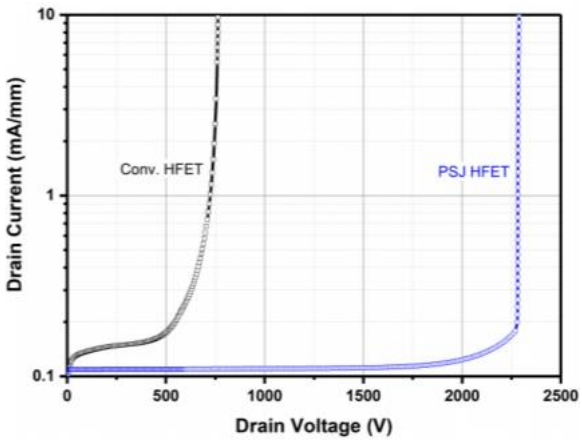



*Figure 2-22: Simulated off-state current-voltage characteristics of conventional GaN-HEMT and PSJ-FET structures in [97]*

With a uniform E-field distribution assumed, the theoretical BV of a lateral SJ device can be approximated as:

$$V_B = E_{crit} \cdot L_{ch} \quad \cdots(2\text{-}11)$$

Where $L_{ch}$ = lateral electron channel length and $E_{crit}$ = critical E-field of the semiconductor material. The on-state resistance can be expressed as:

$$R_{on} = R_{sheet} \cdot \frac{L_{ch}}{W} = \frac{L_{ch}}{q \cdot \mu_{ch} \cdot n_s \cdot W}$$

…(2-12)

Where $R_{sheet}$ = sheet resistance of electron channel in $\Omega \cdot cm^{-2}$, q = electron charge = $1.6x10^{-19}C$, $\mu_{ch}$ = channel electron mobility in $cm^2/Vs$, $n_s$ = sheet electron density in $cm^{-2}$ and W = channel width.

The specific on-state resistance ($R_{on,spec}$) of the lateral SJ device is obtained via multiplication of $R_{on}$ and active device area (A), which can be derived as [98]:

$$R_{on,spec(lat)} = R_{on} \cdot A = R_{on} \cdot W \cdot L_{ch} = \frac{{L_{ch}}^2}{q \cdot \mu_{ch} \cdot n_s}$$

…(2-13)

Note that the plane of the active area is parallel to the current flow direction rather than perpendicular to it as in vertical devices. By combining all equations, the $R_{on,spec}$ and thereby lateral device figure of merit (LFOM) can also be expressed in terms of BV as:

$$R_{on,spec(lat)} = \frac{{V_B}^2}{q \cdot \mu_{ch} \cdot n_s \cdot {E_c}^2}$$

…(2-14)

$$LFOM = \frac{{V_B}^2}{R_{on,spec(lat)}} = q \cdot \mu_{ch} \cdot n_s \cdot {E_c}^2$$

…(2-15)

This FOM can be used for comparing the large area PSJ-FET performance against its ideal (theoretical) counterparts.

## *2.6. Effects of parasitic inductances in circuit layout*

As discussed in the previous section, the GaN transistors exhibit lower on-state conduction loss and faster switching speed than their Si counterparts. Nevertheless, they are more susceptible to unwanted parasitic effects in a printed circuit board (PCB) layout as their dV/dt and di/dt values are higher than conventional Si devices. The copper traces in PCB store magnetic energies as they carry the current and thus they present finite values of inductances in the circuit. These inductances interact with the internal device capacitances that leads to oscillations in the turn-on and turn-off voltage and current waveforms or time delays in their transitions and thus degrade their switching reliability.

The parasitic inductance elements in a half-bridge converter circuit including common source inductance ($L_{CS}$), gate loop and power loop inductances ($L_{GL}$ and $L_{PL}$) are labelled in Figure 2-23. Their effects upon turn-on and turn-off waveforms of a power device are mathematically analysed in detail in Appendix (Section 7.2). The $L_{CS}$ is present on the source pin of the device and is common to both the gate drive loop and power loop. During the switching device (SW) turn-on phase, a rising drain current (i.e. positive di/dt) will induce positive voltage drop across $L_{CS}$ and hence the gate potential is risen. Consequently, less gate current will be available for charging the input capacitance of the device during drain current rise time interval; thus, turn-on transition time and energy loss are increased [99].

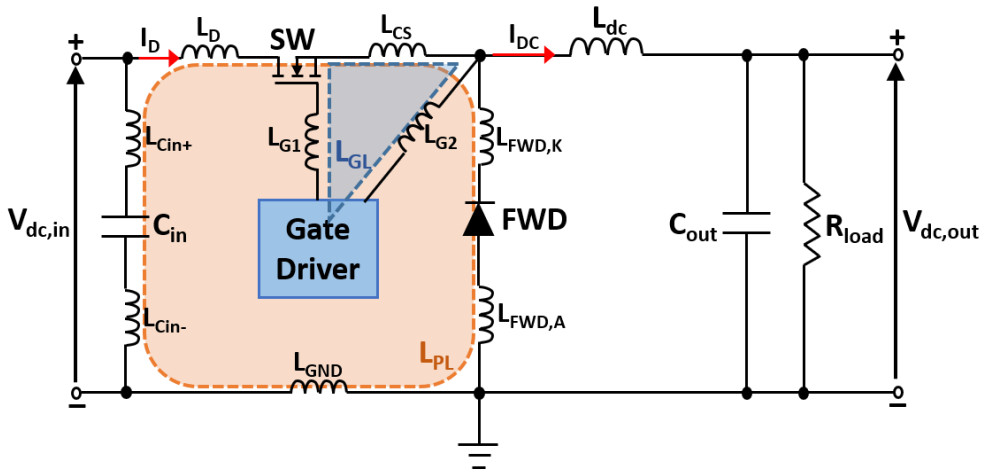



*Figure 2-23:Circuit schematic of synchronous buck converter with parasitic inductances*

The $L_{PL}$, on the other hand, does not directly affect the di/dt during SW turn-on and turn-off current commutation intervals. The di/dt is mainly governed by the input capacitance present at the gate terminal of the SW and total resistance present at the gate drive loop, as will be discussed in Section 3.1.3. It is a combination of all parasitic inductances in the turn-on and turn-off current commutation loop, which can be mathematically expressed as:

$$L_{PL} = L_{D,SW} + L_{CS} + L_{FWD,K} + L_{FWD,K} + L_{GND} + L_{Cin+} + L_{Cin-} \quad \ldots(2\text{-}16)$$

Where $L_{D,SW}$ = the SW drain side inductance (between $C_{in+}$ and SW drain), $L_{FWD,K(A)}$ = FWD cathode (anode) side inductance, $L_{GND}$ = ground loop inductance (between $C_{in}$ and FWD anode) and $L_{Cin+(-)}$ = inductance present within the $C_{in}$ +(-) side.

During turn-on current rise interval, a positive voltage is dropped across $L_{PL}$ and thus $V_{ds}$ across the device is reduced and turn-on loss is reduced. During the turn-off, however, a negative voltage is dropped across $L_{PL}$ due to negative di/dt, which causes $V_{ds}$ overshoot above the dc-link voltage level and thereby increase turn-off switching loss [100]. For fast-switching devices (i.e. high dV/dt), the magnitude of this overshoot will become higher. Therefore, if $L_{PL}$ becomes

excessively high, then the voltage overshoot during turn-off may damage the device, which limits the maximum dc-link voltage at which the device can operate.

The $L_{GL}$ is a combination of the parasitic inductances present in the gate drive loop of the SW device as illustrated in Figure 2-23 and can be expressed as:

$$L_{GL} = L_{G1} + L_{G2} + L_{CS}$$

Where $L_{G1}$ = parasitic inductance between gate driver output and SW gate, and $L_{G2}$ = parasitic inductance in the gate drive return path between SW common source (CS) node and gate driver's ground reference point.

The $L_{GL}$ is of least importance amongst parasitic inductance components as it does not directly affect dV/dt and dI/dt of SW and thus its switching losses. However, with an increase in $L_{GL}$, higher resistance in the gate drive loop ($R_{GL}$) is required to achieve critical damping and thus avoid excessive $V_{gs}$ overshoot and undershoot that leads to instability in the device's switching, which can be mathematically expressed as [99, 101]:

$$R_{GL,crit} = 2\sqrt{\frac{L_{GL}}{C_{iss,SW}}} \quad \ldots(2\text{-}17)$$

Where $C_{iss,SW}$ = input capacitance of SW device as defined in Section

With an increase in $R_{GL}$, the turn-on and turn-off transition times will become longer and thus switching losses are increased. Therefore, it is recommended to minimise $R_{GL}$ as well as $L_{GL}$ and $L_{PL}$ for optimum device switching performance.

# 3 GaN PSJ-FET Performance Evaluation

## *3.1. D-mode PSJ-FET performance*

During the converter operation, certain amount of heat will be dissipated from the switching power devices due to their power losses incurred during repetitive switching events and on-state current conduction. Therefore, it must be ensured that the device junction temperature ($T_j$) does not exceed the maximum limit at which the reliability of the bond wire connections within the device packages may be degraded [102] or the devices may enter thermal runaway and fail due to excessive leakage current during its off-state [103]. Therefore, before commencing onto the power converter design, it becomes necessary to accurately evaluate the electrical performance of the power devices to be used in order to ensure their reliable steady-state operation.

The new large-area PSJ on sapphire samples were manufactured by Japanese firm POWDEC K.K. and were packaged with Kyocera's KO-PWR121297 package with copper-bonded Silicon Nitride (SiN) substrate as shown in Figure 3-1. The device width is 148mm and the PSJ channel length ($L_{psj}$) is 40µm. With this $L_{psj}$ value, according to [47], the device is capable of withstanding $V_{ds}$ exceeding 3 kV at room temperature but its exact avalanche breakdown voltage is yet to be determined due to the limitations in the measurement instrument. The materials, thicknesses and dopants of the epi-layers within the large-area devices investigated in this work are presented in Appendix (Section 7.1).

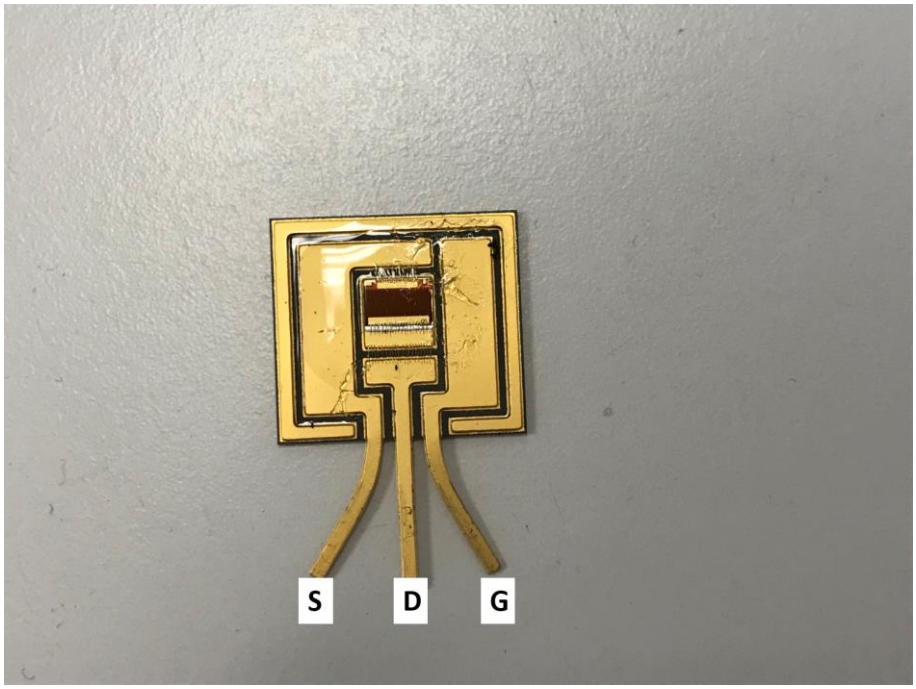
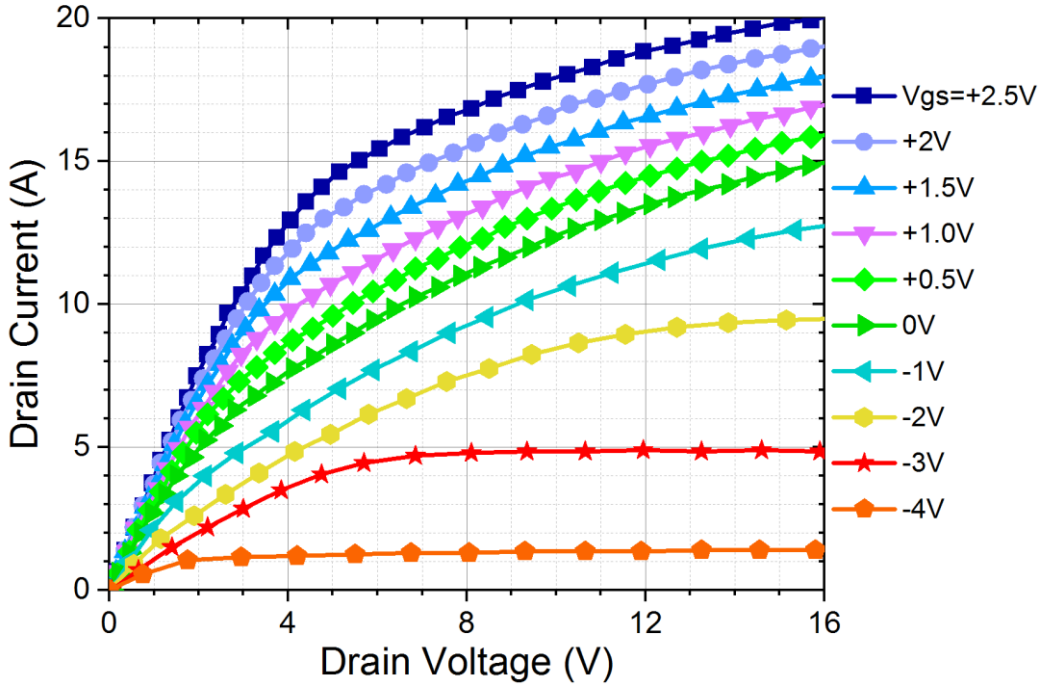



*Figure 3-1: Packaged large-area 3 kV PSJ-FET sample*

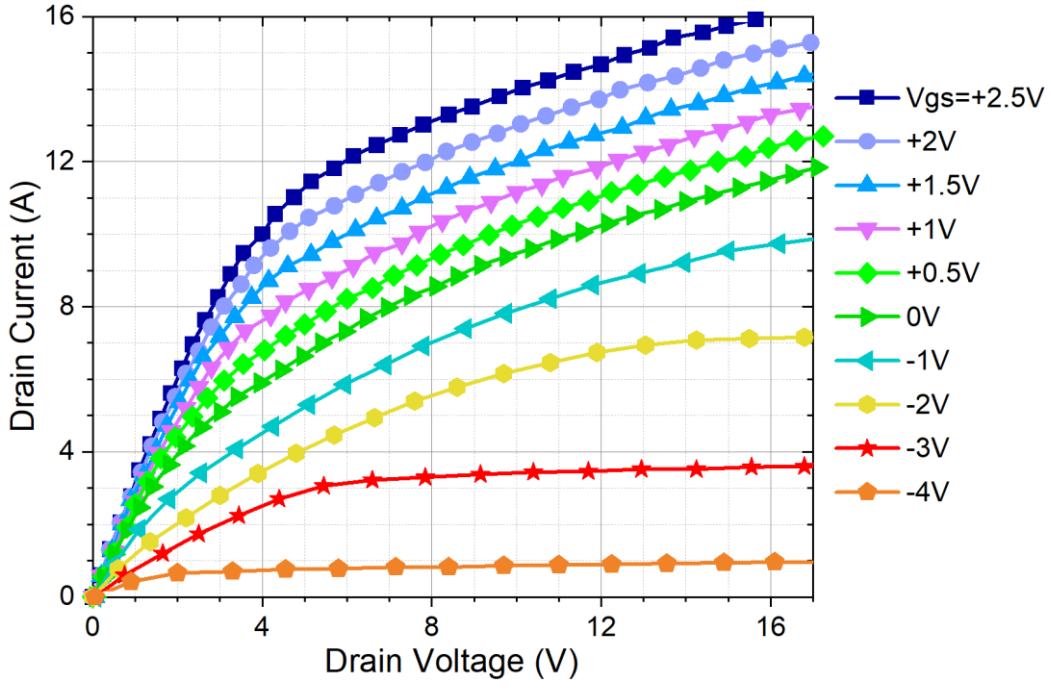
### *3.1.1. Static current-voltage characteristics*

The on-state drain current vs. drain voltage ($I_d$ – $V_{ds}$) characteristics of the PSJ sample must be evaluated at high temperatures in order to take increase in on-state conduction and turn on/off losses into account during its operation in power converters. For its measurement, the Tektronix 371B curve tracer connected to Heraeus heating oven was used. The static forward $I_d$ - $V_{ds}$ characteristics of the device sample under various device temperatures ($150^0$C maximum) are shown in Figure 3-2(a)~(f). The maximum $V_{gs}$ applied was limited to +2.5V in order to avoid excessive gate leakage current due to forward conduction of the internal gate-to-drain diode. As shown from the six figures, the $I_d$ output is reduced as temperature rises. This occurs due to the reduction in electron mobility via rise in phonon scattering as lattice temperature is increased. Also, it is important to observe change in turn-on threshold gate voltage ($V_{gs,th}$) with device temperature as this determines

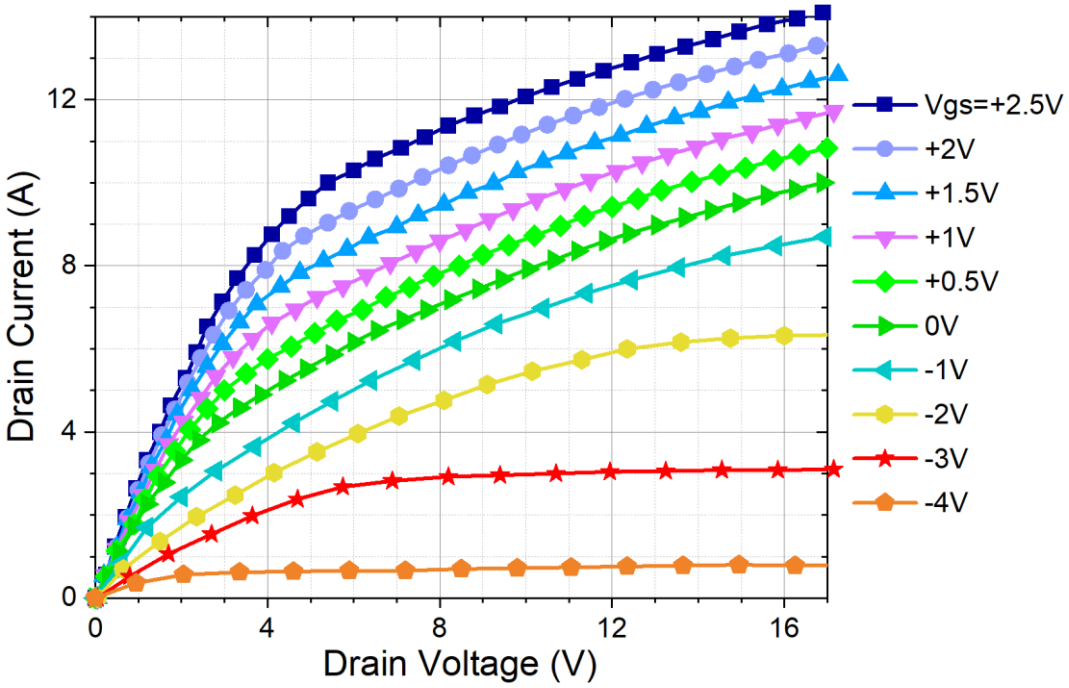
gate drive required to turn the device 'off'. As shown in Figure 3-3, the $V_{gs,th}$ of the 3 kV PSJ sample stayed constant at ~ -5 V regardless of the device temperature.



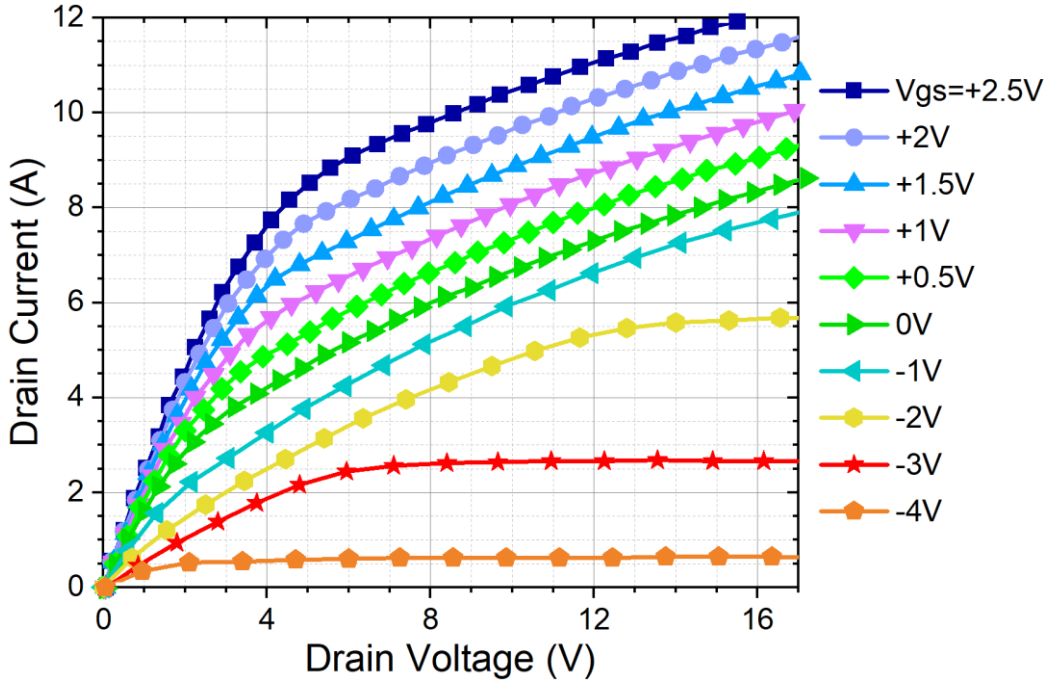

(a)



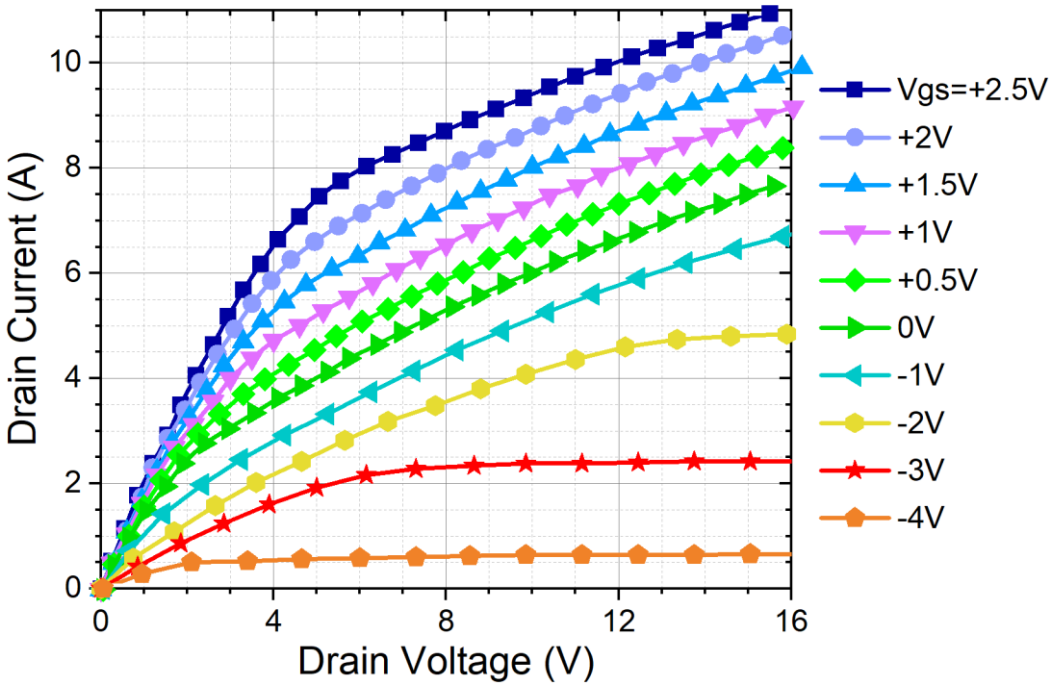

(b)


Drain Current (A)
Drain Voltage (V)
0
4
8
12
16
Vgs=+2.5V
+2V
+1.5V
+1V
+0.5V
0V
-1V
-2V
-3V
-4V

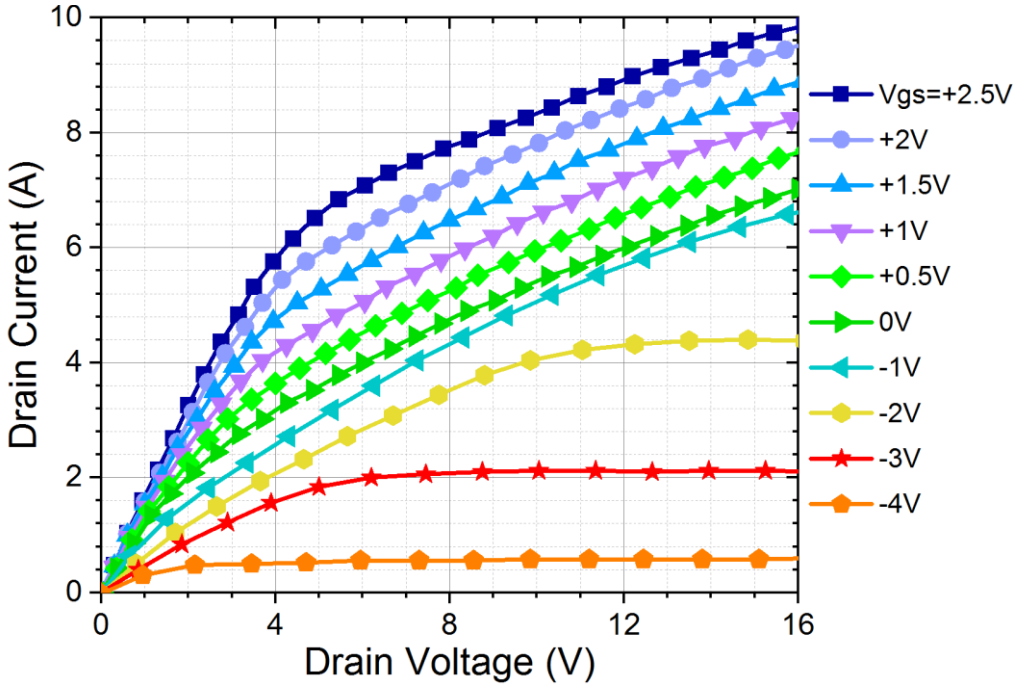
(c)


Drain Current (A)
Drain Voltage (V)
0
2
4
6
8
10
12
0
4
8
12
16
Vgs=+2.5V
+2V
+1.5V
+1V
+0.5V
0V
-1V
-2V
-3V
-4V

(d)




(e)




(f)

*Figure 3-2: Typical $I_d - V_{ds}$ characteristic curves of >3 kV PSJ-FET at device temperatures of (a) $25^0$C, (b) $50^0$C, (c) $75^0$C, (d) $100^0$C, (e) $125^0$C and (f) $150^0$C*

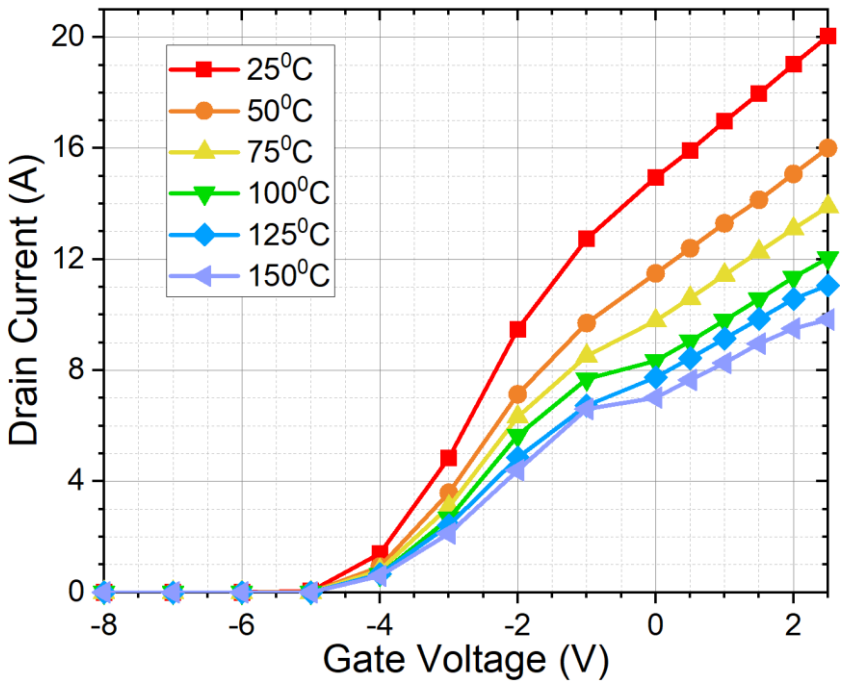



*Figure 3-3: Large-area >3 kV PSJ-FET $I_d$ – $V_{gs}$ characteristic curves at device temperatures $25^0$C~$150^0$C and $V_{ds}$ = 16V*

The reverse I-V characteristics of large-area PSJ transistors, on the other hand, are not presented in this chapter. This is primarily due to the device failures that were observed when the $V_{ds}$ < 0 V and $V_{gs}$ < -5 V were applied onto them at the same time. Hence, these large-area devices are not capable of reverse current conduction, which leads to the requirement for anti-parallel diodes to provide freewheeling paths for the current to flow through in half-bridge power converters. With further improvements of the device performance, the reverse conduction may be enabled and thus need for external anti-parallel diodes can be eliminated.

The change in forward $R_{ds,on}$ measured at $V_{ds}$ = +1.0 V and $V_{gs}$ = +2.5 V with $T_j$ for five large-area PSJ devices are presented in Figure 3-4. At low temperatures of below $75^0$C, the maximum $R_{ds,on}$ discrepancy is within 5% of its mean value. However, at temperatures exceeding $100^0$C, the discrepancy grown up with $T_j$; the maximum standard deviation in $R_{ds,on}$ was measured to be ~11.26% of its mean value at $150^0$C. Therefore, a relatively large error in calculation of power converters'

efficiency would be present as the devices may operate at high $T_j$ close to its maximum limit under the full-load operating condition.

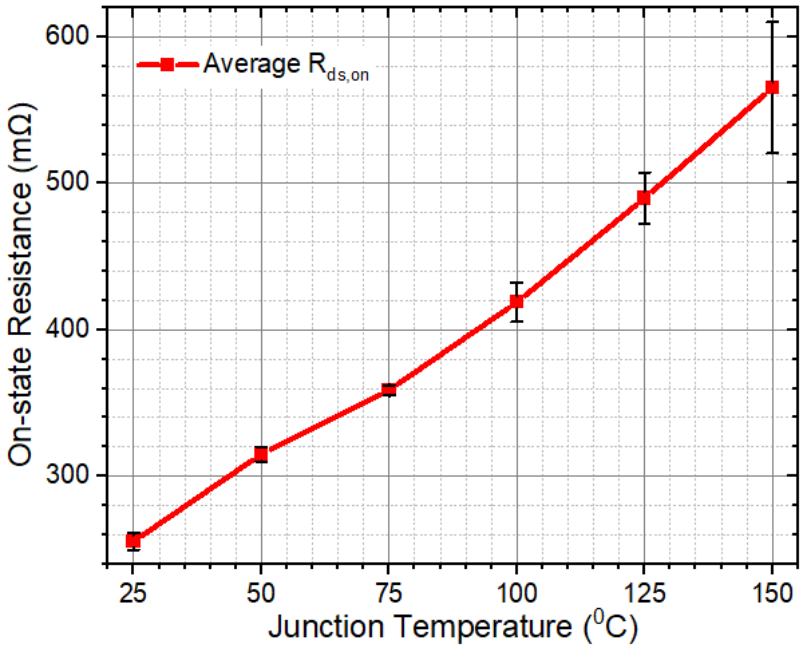
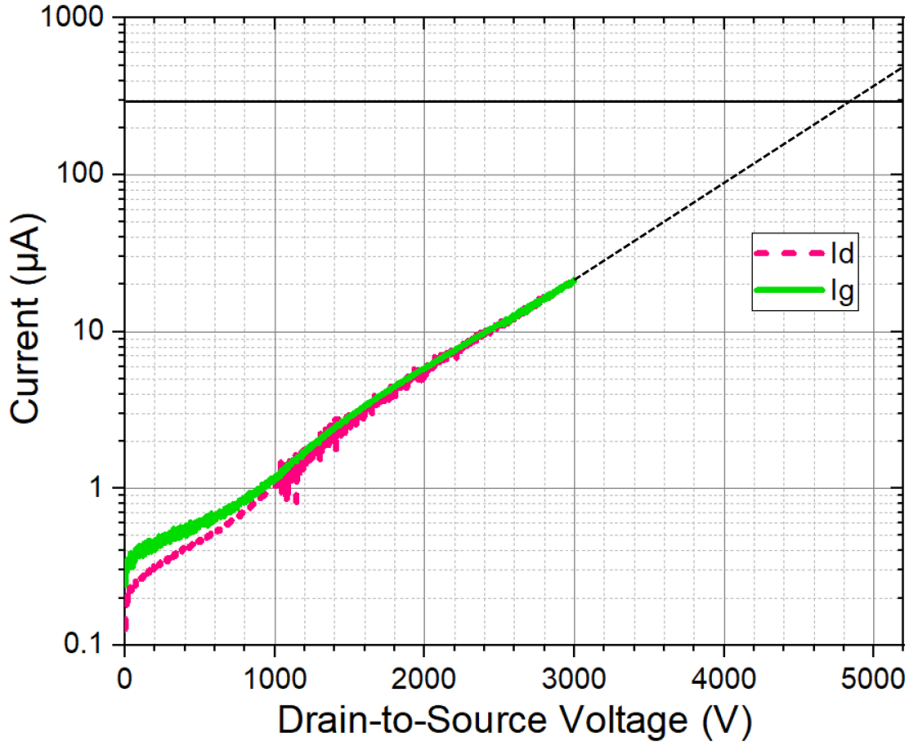


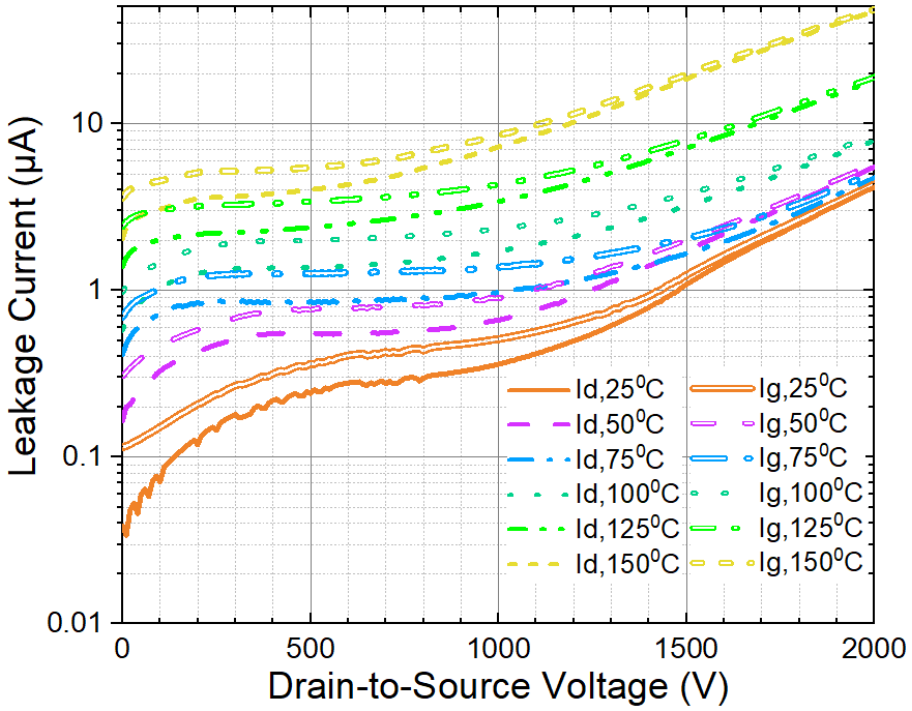

*Figure 3-4: Average $R_{ds,on}$ vs. $T_j$ for five large-area PSJ samples at $V_{ds}$ = +1.0 V and $V_{gs}$ = +2.5 V with the error bars indicating standard deviations*

In addition, the off-state leakage $I_d$ – $V_{ds}$ characteristics is the key measurement data as this determines the off-state power loss and breakdown characteristics of the device. The typical drain and gate leakage currents ($I_d$ and $I_g$) of the scaled up PSJ transistor versus drain-to-source voltage of up to 3 kV at room temperature were measured and plotted in Figure 3-5(a). With a linear extrapolation of the leakage $I_d$, the breakdown voltage of the PSJ devices ($L_{psj}$ = 40 µm, $W_g$ = 1 mm) is expected to be ~4.8 kV with a leakage current of 300 µA. The leakage currents were also measured using B1505A power device analyser interfaced with Heraeus heating oven into which the device sample is placed. The typical off-state $I_d$ and $I_g$ densities versus $V_{ds}$ characteristic curves were obtained up to 2 kV dc and under device temperatures ranging from 25$^0$C to 150$^0$C and are shown in Figure 3-5(b). The test voltage was limited to 2 kV as the device availability was limited

for this work. It can be observed that at $V_{ds}$ > 1 kV, $I_d$ and $I_g$ are approximately equal, which implies that the dominant leakage current path is from drain to gate electrode. The leakage current density of the PSJ-FET is by two orders of magnitude smaller than the lateral GaN-HEMTs with field-plates (FPs) presented in [104]. Although FPs can suppress E-field crowding to some extent, they cannot eliminate it and therefore high level of leakage currents still occur at relatively low $V_{ds}$. Also, it can be observed from Figure 3-5(b) that the leakage currents are flattened at $V_{ds}$ < 1 kV, which can be attributed to the uniform electric-field distribution along the lateral PSJ channel due to the charge balance. Therefore, it is proven that the lateral PSJ technology is more effective in suppressing the peak electric field and thus leakage current compared to its conventional counterparts.




(a)




(b)

*Figure 3-5: Off-state leakage drain and gate current ($I_d$ and $I_g$) vs. $V_{ds}$ characteristic curves at device temperatures of 25$^0$C, 50$^0$C, 75$^0$C, 100$^0$C, 125$^0$C and 150$^0$C of the large-area PSJ-FET ($L_{psj}$ = 40 μm, $W_g$ = 148 mm)*

The specific $R_{ds,on}$ of the large-area PSJ device and intrinsic Si, SiC and GaN material limit curves are plotted in Figure 3-6. The material limit curves were drawn based on Baliga's device Figure of Merit (FoM) in [105]. The specific $R_{ds,on}$ of the commercial SJ Si-MOSFET (IPW65R045C7) [106], SiC-MOSFET (CPM2-1700-0045B) [107] and GaN-HEMT (GS-065-120-1-D) [108] were also plotted on the same figure for comparison. The PSJ transistor's specific $R_{ds,on}$ was determined to be much lower than the commercial devices when drawing a tangent line parallel to the materials' figure of merit curves. Nevertheless, it can be seen from the figure that its specific $R_{ds,on}$ is by an order magnitude higher than what is achievable by intrinsic GaN material properties. Hence, there is a room for improving PSJ device's performance via finer lithography and optimization of electrode metal layouts and thicknesses.

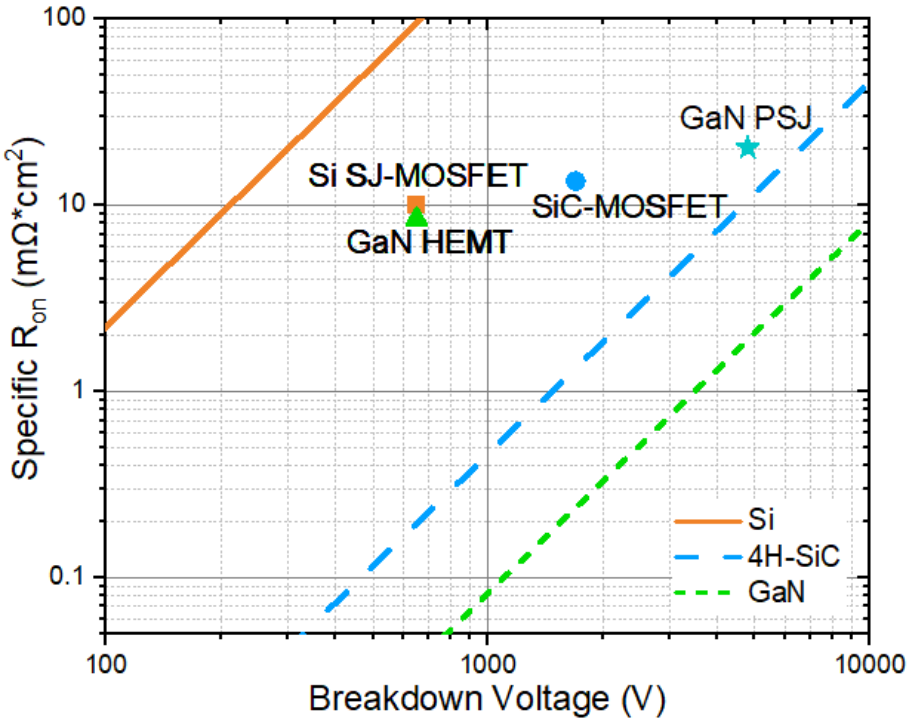



*Figure 3-6: Specific $R_{ds,on}$ of large-area GaN PSJ transistor and commercial 650V Si SJ-MOSFET, 1.7 kV SiC-MOSFET and 650V GaN-HEMT*

### *3.1.2. Terminal capacitance-voltage (C-V) characteristics*

Internal device terminal capacitances are key parameters that determines the dynamic behavior of power devices. The three terminal capacitances of a typical power device are gate-to-source capacitance ($C_{gs}$), gate-to-drain capacitance ($C_{gd}$) and drain-to-source capacitance ($C_{ds}$), which are clearly labelled and presented in Figure 3-7. The $C_{gd}$ is also commonly referred to as 'Reverse transfer capacitance' ($C_{rss}$) and determines the drain voltage slew rate ($dV_{ds}/dt$) during the turn-on and turn-off transients. The combination of $C_{gs}$ and $C_{gd}$ is referred to as the 'Input capacitance' ($C_{iss}$), which determines the drain current slew rate ($dI_d/dt$) during the switching transients, respectively. The combination of $C_{gd}$ and $C_{ds}$, commonly referred to as the 'Output capacitance' ($C_{oss}$), determines the stored charge to be discharged by the transistor's channel current during its turn-on process and to be charged by load current ($I_{load}$) during its turn-off. As the PSJ device was made on

an insulating Sapphire substrate, the effect of parasitic terminal-to-substrate capacitance is minimal and hence can be neglected.

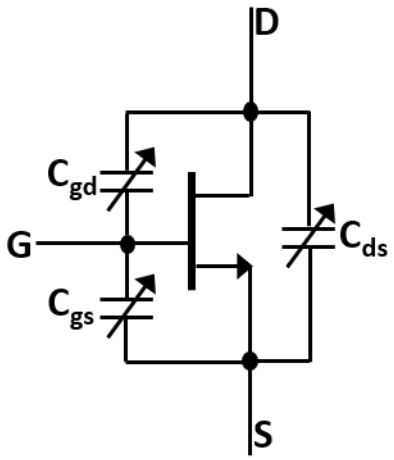



*Figure 3-7: Device terminal capacitances with labels ($C_{ds}$, $C_{gd}$, and $C_{gs}$)*

The terminal capacitances of the large-area PSJ device were measured using B1505A device analyser with a multi-frequency capacitance measurement unit (MFCMU) and N1260A high-voltage bias tee. The detailed schematic of the N1260A bias tee and MFCMU is presented in Figure 3-8. The four output ports from MFCMU, including high potential (HP), high current (HC), low current (LC) and low potential (LP), are connected to four inputs of the N1260A bias tee via BNC connectors. The capacitance is measured by sending small-signal AC voltage to the device under test (DUT) and measuring the induced current through LC port. The outer metallic shields of the four BNC cables are tied to the AC guard port of N1260A bias tee and are fixed to be a 'virtual ground', which is a floating reference set via auto-balancing bridge that can be conceptualized as an operational amplifier (op-amp); its circuit schematic is shown in Figure 3-9. If the Capacitance meter low (CML) potential is left floating, then the AC current through the resistor $R_2$ ($I_2$) will

be equal to the induced current through DUT ($I_1$) and thus the measured capacitive impedance can be expressed as:

$$Z_{DUT} = \frac{V_1}{I_2} = \frac{V_1 R_2}{V_2} \quad \ldots(3\text{-}1)$$

As a result, both the voltage and current are balanced due to the presence of auto-balancing bridge. However, if the CML terminal is tied to the earth (ground), then the induced AC current will be directly shorted to ground and thus an imbalance in the auto-balancing circuit and measurement error will occur.

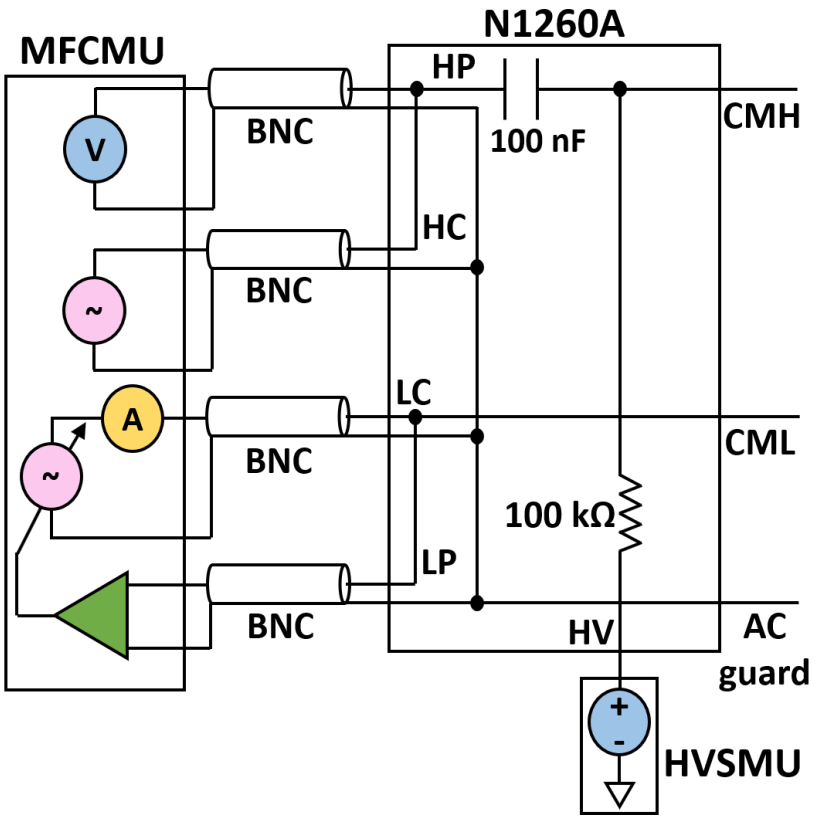



*Figure 3-8: Detailed schematic of MFCMU in B1505A device analyser and N1260A high-voltage bias tee for C-V measurement setup*

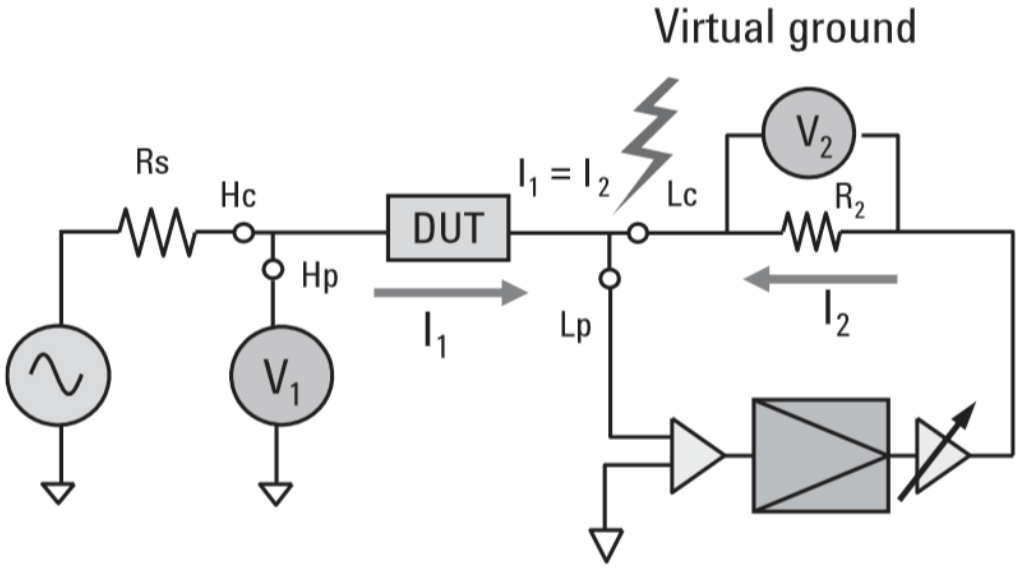
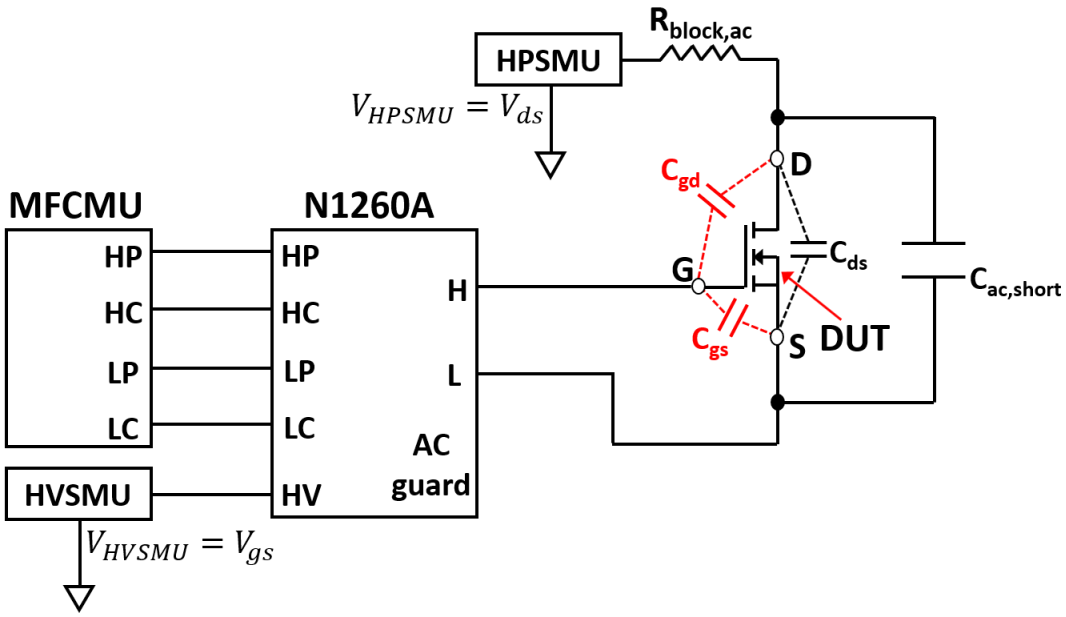



*Figure 3-9: Auto-balancing bridge circuit for capacitance measurement*

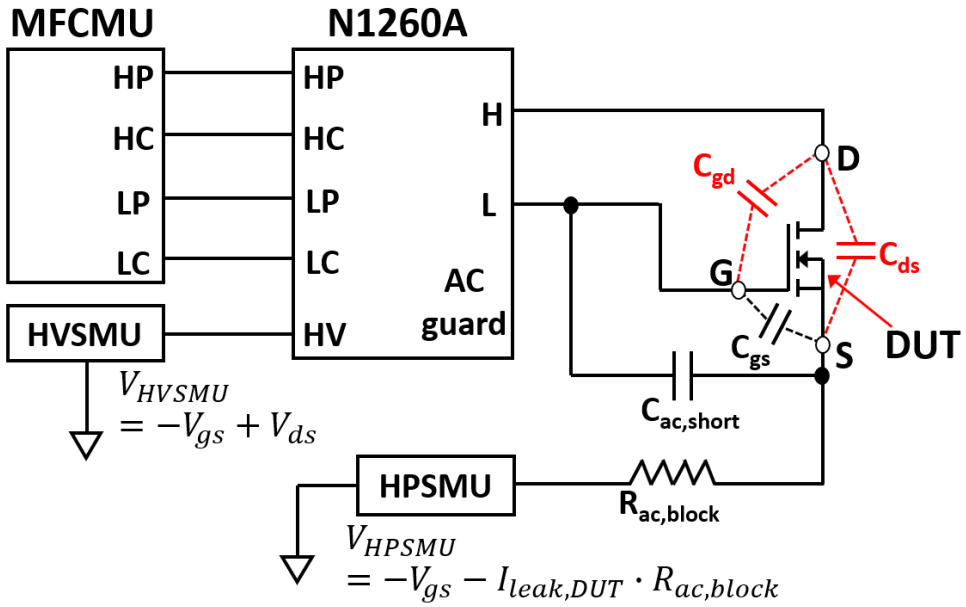
The schematic of the $C_{iss}$ / $C_{oss}$ / $C_{rss}$ vs. $V_{ds}$ and $C_{iss}$ / $C_{rss}$ vs. $V_{gs}$ measurement circuit used for D-mode PSJ transistors is presented in Figure 3-10(a)~(d). The small-signal AC voltage with a frequency of 100kHz and amplitude of 200mV was applied using B1505A power device analyser and the $V_{gs}$ bias of -10V was applied to the DUT in order to hold it in its 'off' state during its measurement. The frequency of 100 kHz was chosen instead of 1 MHz (that is the standard C-V measurement frequency) as negative capacitance values were measured at 1 MHz that occurred due to the parasitic inductances present in the contacts and leads of the measurement circuit. As the small-signal AC frequency is increased, the impedance of these parasitic inductances would dominate over the impedance of the capacitance to be measured and thereby the capacitance value measured by the instrument becomes negative [109].

The phase and load compensation were performed prior to the measurement in order to obtain accurate results using the B1505A instrument. The resultant C-V curves with respect to drain and gate biases are presented in Figure 3-11(a) and (b), respectively. As with conventional Si-MOSFETs, it can be observed from Figure

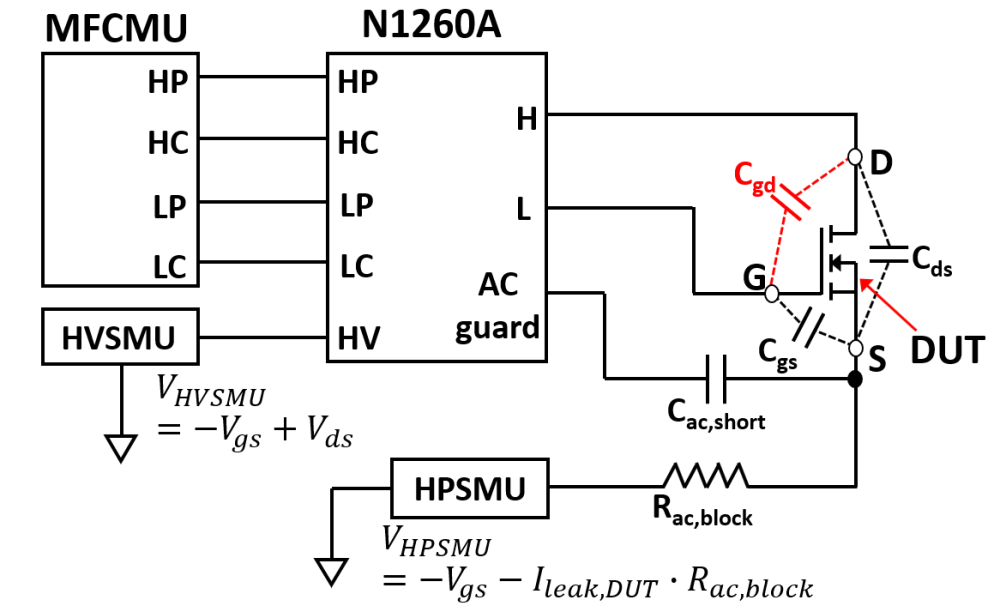
3-11(a) that the terminal capacitances decay with an increase in $V_{ds}$. In addition, under $V_{ds}$ = 0 V, both $C_{gd}$ and $C_{gs}$ increased remarkably at $V_{gs} = V_{gs,th}$, which will be qualitatively explained later.



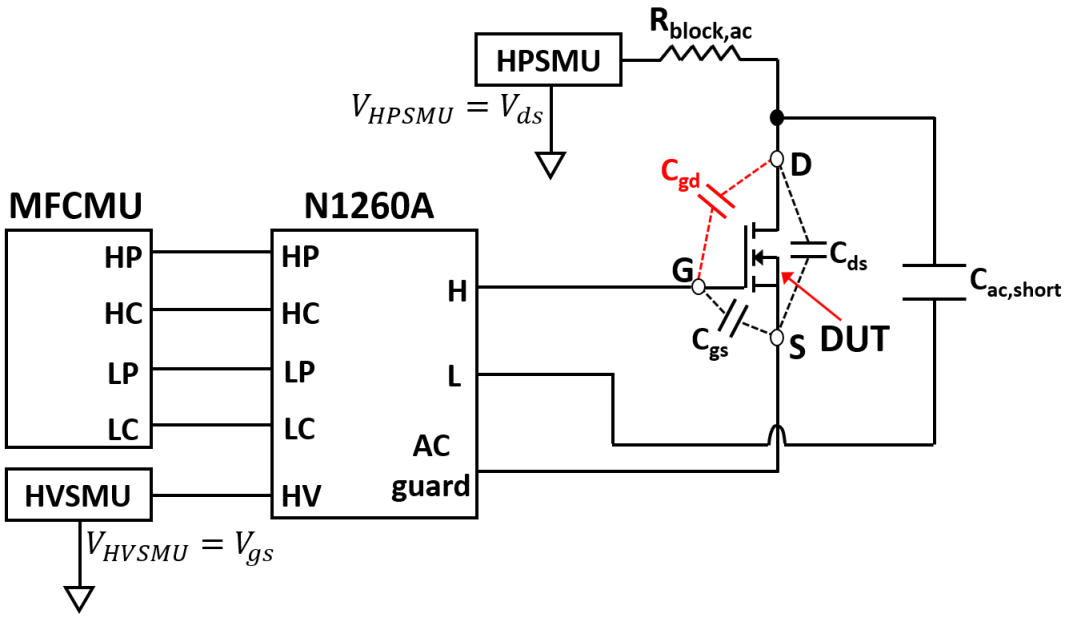

(a)




(b)

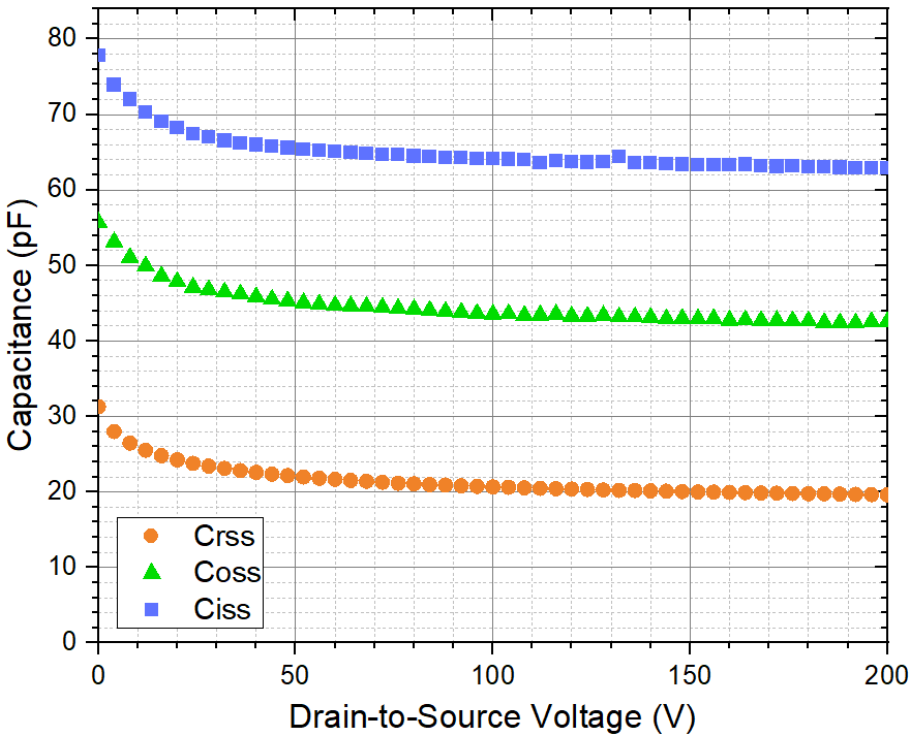



(c)

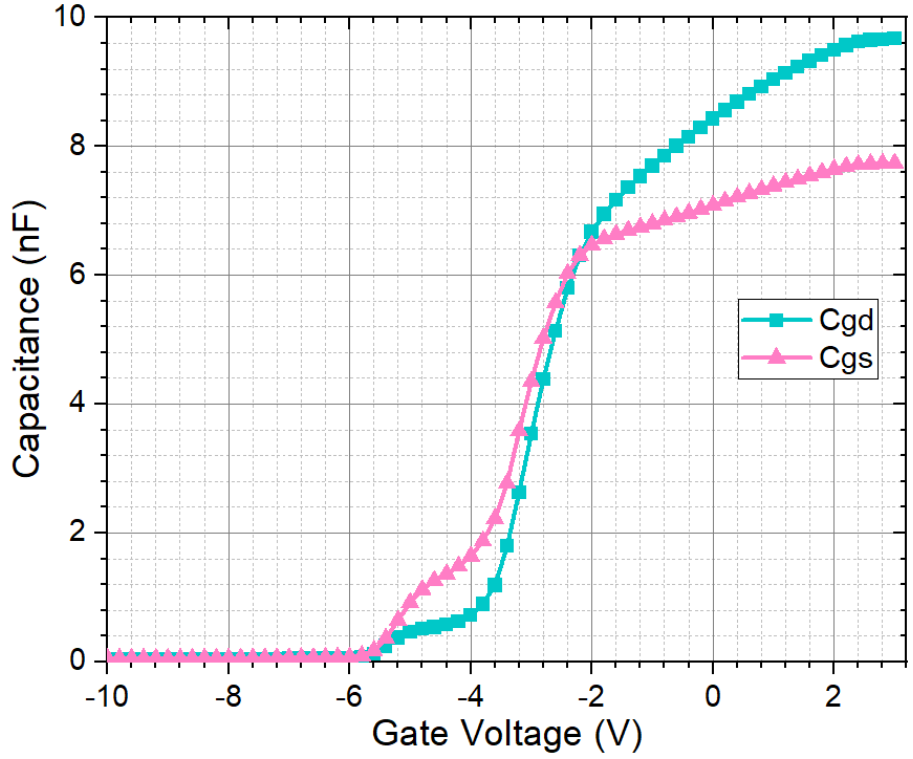



(d)

*Figure 3-10: (a) $C_{iss}$ – $V_{ds}$ / $C_{iss}$ – $V_{gs}$, (b) $C_{oss}$ - $V_{ds}$, (c) $C_{rss}$ – $V_{ds}$ and (d) $C_{rss}$ - $V_{gs}$ measurement circuit schematics for D-mode power devices*




(a)




(b)

*Figure 3-11: Average (a) $C_{iss}$, $C_{rss}$ and $C_{oss}$ vs. $V_{ds}$ curves at $V_{gs}$ = -10V and (b) $C_{gd}$ and $C_{gs}$ vs. $V_{gs}$ curves at $V_{ds}$ = 0V obtained using B1505A device analyser at AC frequency = 100kHz*

In order to observe the change in $C_{rss}$ with respect to both $V_{gs}$ and $V_{ds}$ at the same time, another measurement circuit for its characterization using Hioki IM3533-01 LCR meter (its schematic presented in Figure 3-12) was used. The circuit consisted of two DC power supplies for gate and drain biases, an LCR meter, AC blocking resistors and DC blocking capacitors. A small sinusoidal signal with a fixed frequency was sent from the LCR meter to the device under test (DUT), which will induce a sinusoidal current through it and thus capacitive impedance can be measured accordingly.

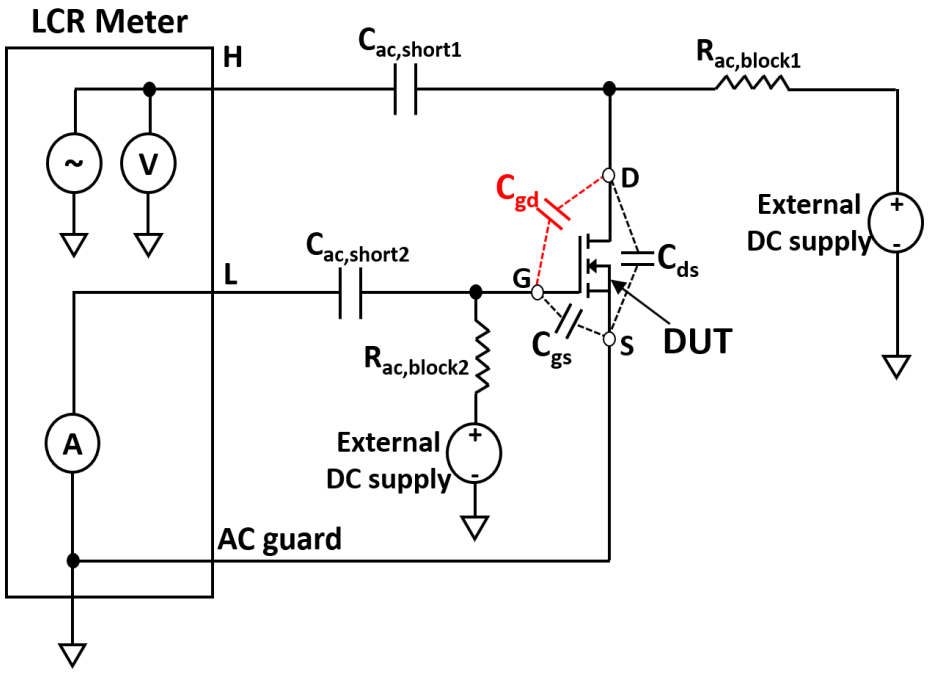



*Figure 3-12: Schematic of $C_{rss}$ ($C_{gd}$) vs. $V_{ds}$ / $V_{gs}$ measurement circuit for D-mode power devices using an LCR meter*

The resultant $C_{gd}$ vs. $V_{ds}$ curves at $V_{gs}$ =-6V to -2V obtained from the measurement are presented in Figure 3-13. The maximum $V_{ds}$ was limited to 2V in order to prevent overheating of the DUT as the device is in its on state and the measurement is carried out under dc condition. From the figure, it can be observed that the Miller capacitance increases with $V_{gs}$ and decreases with $V_{ds}$. This

phenomenon can be explained qualitatively with Figure 3-14(a)~(c) where the components of $C_{gd}$ within the PSJ-FET are clearly labelled for when the device is off and on. When the device is on and operates in an ohmic region, 2DEG and 2DHG will be formed at the bottom and top GaN/AlGaN heterojunctions, respectively. As a result, a parallel plate capacitance ($C_{AlGaN,pp}$) is formed throughout the lateral PSJ channel with a thin AlGaN between them, which leads to a large $C_{gd}$ value. The $C_{gd}$ will increase with the PSJ channel length ($L_{psj}$) as the effective capacitor plate area is scaled up accordingly. As $V_{ds}$ becomes higher, the 2DEG and 2DHG at the drain side will be depleted as illustrated in Figure 3-14(b), which forms a depletion region capacitance ($C_{dep}$). As $C_{dep}$ is effectively much smaller in value and in series with $C_{AlGaN,pp}$, it will dominate the total $C_{gd}$ and thus $C_{gd}$ will decrease sharply. On the other hand, when the PSJ-FET is in its 'off' state, the 2DEG and 2DHG are depleted throughout the whole channel and thus $C_{dep}$ is formed between gate and drain electrodes and therefore $C_{gd}$ stays at a very low value.

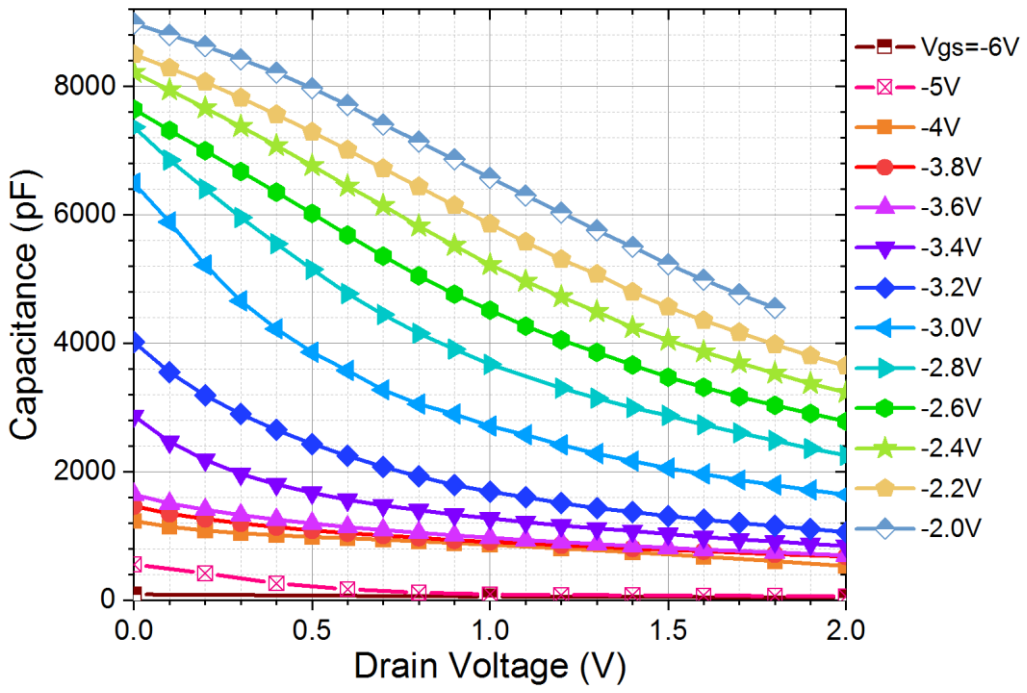
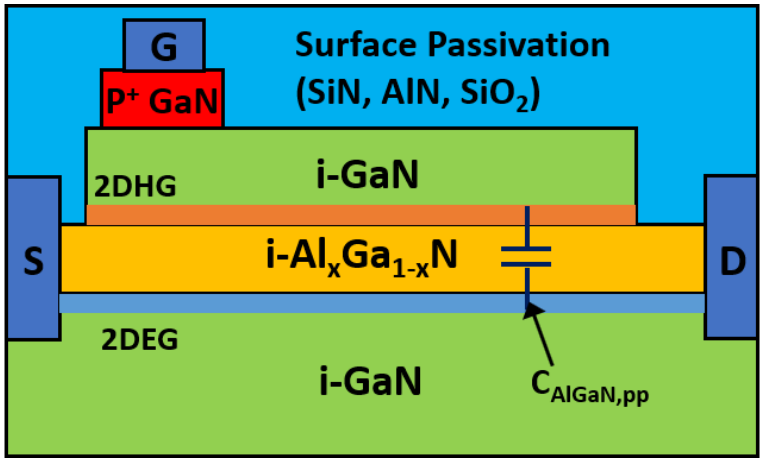
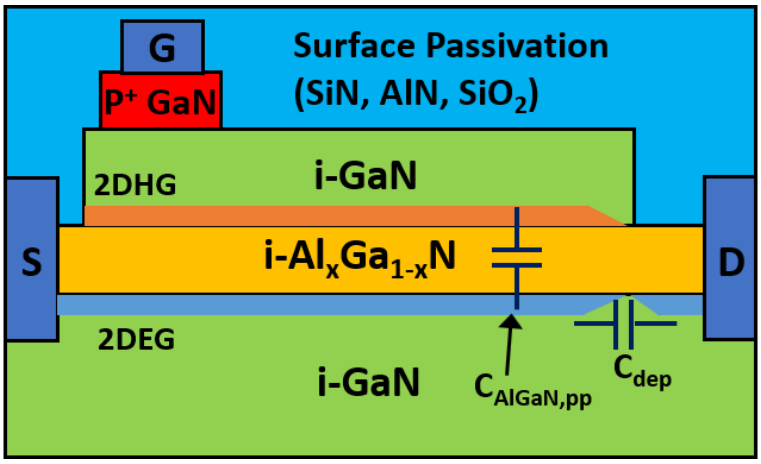


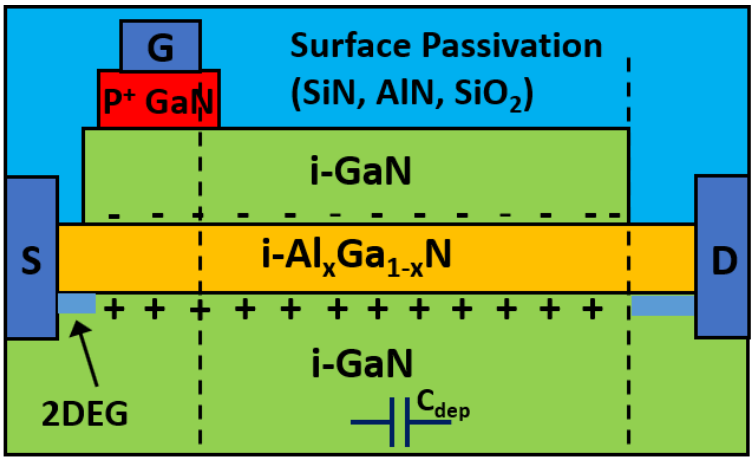
*Figure 3-13: Typical $C_{gd}$ vs. $V_{ds}$ / $V_{gs}$ curves of the large-area PSJ-FET obtained using Hioki IM3533-01 LCR meter (AC frequency = 100 kHz)*




(a)




(b)




(c)

*Figure 3-14: Miller capacitance ($C_{gd}$) components within the PSJ-FET when (a) the transistor is in its 'on' state and operates in an ohmic region, (b) the transistor is in its 'on' state and operates in saturation region and (c) the transistor is 'off'*

### *3.1.3. Switching characteristics*

The switching characteristics of the power devices become important due to their switching energy losses and thus the degradation in the efficiency of power converters. In order to obtain hard turn-on and turn-off switching characteristics of the large-area PSJ-FETs, a double pulse tester (DPT) circuit layout was designed using Proteus professional software and its schematic is shown in Figure 3-15. The layout was optimized so that parasitic inductances in the power loop and gate loop are minimised in order to minimize the $V_{ds}$ overshoot and $V_{gs}$ ringing. This was achieved by using traces with their widths as wide as possible and shortening trace lengths by placing the components close to each other. The double pulse signal output from the Digilent Basys2 Field Programmable Gate Array (FPGA) controller is fed into a 5MBd optical receiver via 5MBd optical transmitter connected to a fibre optic cable. This optical link serves to provide a galvanic isolation required for the user's safety at the controller side during high-voltage testing.

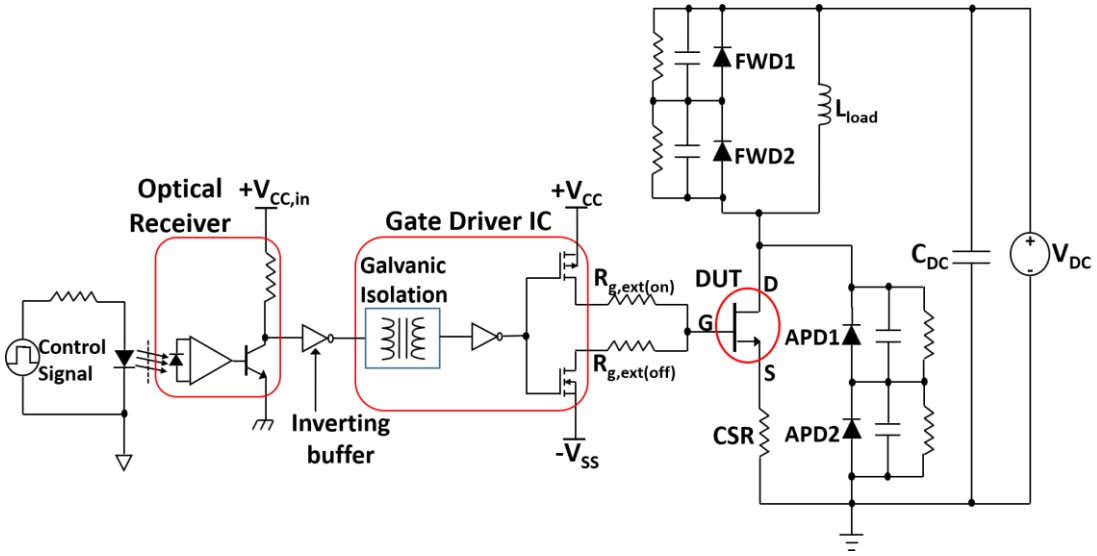
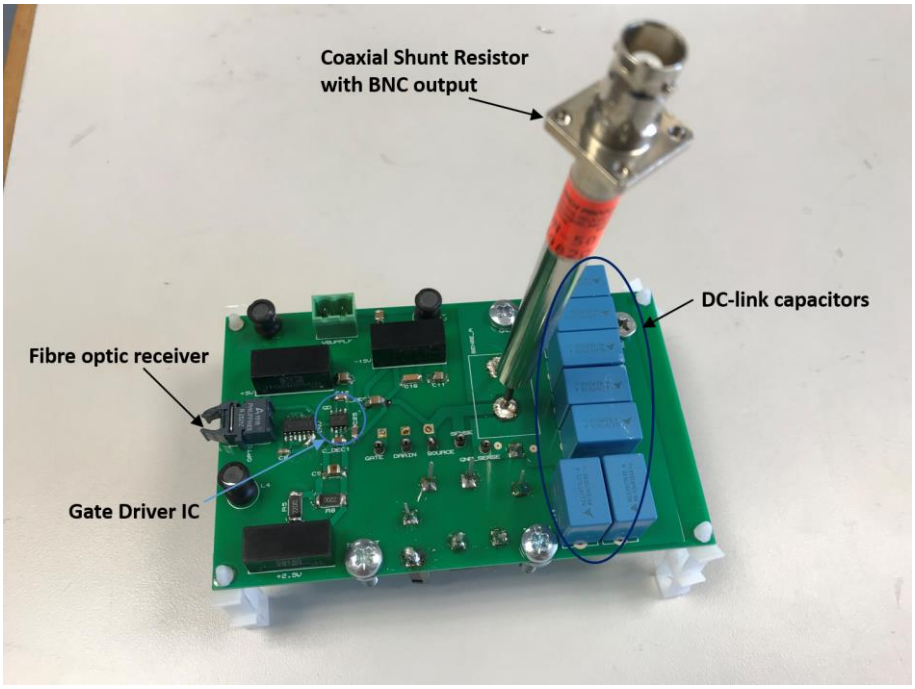
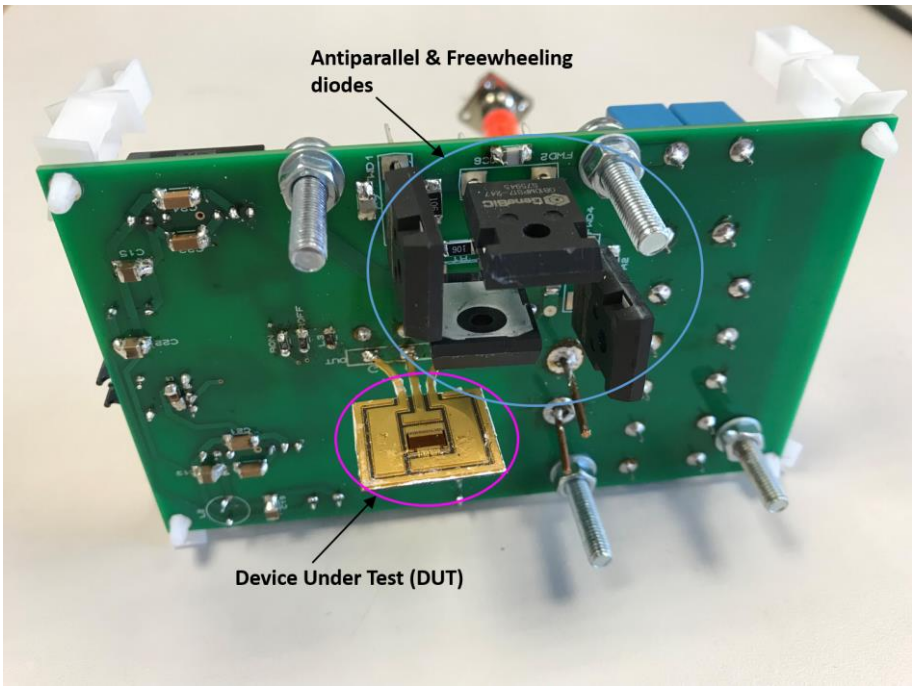



*Figure 3-15: DPT circuit schematic*

The main power loop of the DPT circuit consists of an antiparallel diode (APD), coaxial shunt resistor (CSR), dc-link decoupling capacitor ($C_{DC}$), device under test (DUT), freewheeling diode (FWD) and a load inductor ($L_{load}$). The APD was added in parallel to the DUT in order to measure the effect of its junction capacitance upon turn-on and turn-off switching loss calculations. Both the APD and FWD consists of two series connected 1.7 kV SiC Schottky diodes in order to support a dc-link voltage of 3 kV as no fast recovery diodes and rectifiers with their breakdown voltages exceeding 3 kV and similar dc current ratings to the DUT were commercially available. Also, snubber capacitors and resistors of 100 pF and 5 MΩ were added in parallel to each diode in order to achieve transient and static voltage sharing, respectively. The top and bottom views of the fabricated DPT circuit board are shown in Figure 3-16(a) and (b), respectively. The DUT, which is the large area PSJ-FET for this work, was soldered onto the opposite side to the gate drive circuitries in order to let sufficient space for the Aluminium heating plate onto which the DUT was mounted to be placed for high-temperature switching test.




(a)




(b)

*Figure 3-16: Fabricated DPT printed circuit board: (a) top side and (b) bottom side*

#### *3.1.3.1 Selection of current measurement method*

For the DUT current measurement in this work, a 0.5 Ω CSR (SDN-50) and an oscilloscope with bandwidths of 800MHz and 1GHz were used, respectively.

For current measurements with fast transient edges, a sufficient bandwidth is required for the measurement tool so that transient edges can be captured with high fidelity. The total bandwidth of the measurement system including probes and oscilloscopes can be approximated as [110]:

$$BW_{system} = \frac{1}{\sqrt{\frac{1}{BW_{oscil}{}^2} + \frac{1}{BW_{probe}{}^2}}} \quad \ldots(3\text{-}2)$$

The system bandwidth implies the limitation of the measurement to accurately capture the phase and magnitude of the measured signal. The effective bandwidth of a signal with a transient rise time $t_r$ and fall time $t_f$ can be mathematically expressed as [110]:

$$f_{sw} = \frac{0.35}{min(t_r, t_f)} \quad \ldots(3\text{-}3)$$

At the measurement bandwidth, the magnitude of the signal is attenuated to approximately 70.7% (-3dB) of its original value. In order to provide accurate representation of the non-sinusoidal signal magnitude, the measurement bandwidth must be five times higher than the effective bandwidth of the measured signal. However, it must also be noted that there already exists a $45^0$ phase shift at the measurement bandwidth, which will cause time delay errors to the signal when the bandwidth is not sufficient. Thus, in order to accurately represent signal magnitude and phase, the measurement system bandwidth must be more than ten times higher the effective bandwidth of the measured signal.

There exist many options for current measurements, including coaxial shunt resistors (CSR), surface mount resistors, current transformers (CTs) and Rogowski coils. The surface mount chip resistors provide simple means of current measurement but their series inductance will cause significant distortion in the

measurement due to the high di/dt during turn-on and turn-off transients and hence the accuracy will be degraded [111]. For CSR, the current flowing into and out of the resistor are designed to be in opposite direction to each other, the magnetic flux fields are cancelled and thereby total series inductance becomes nearly zero. Therefore, the measured signal does not contain any inductive elements and will be of high fidelity. Then, the primary factor limiting its bandwidth will be the skin effect of the resistive element and the distributed capacitance of the coaxial structure [112]. However, the main drawback of CSR is its lack of galvanic isolation as the outer shield of BNC connector is tied to the ground of the oscilloscope; thus, it can only be used for low-side measurements [113].

The CTs can be used as a means of current measurement, but their bandwidths are limited to 200 MHz max [114], which is much lower than that of coaxial shunt resistors of 2 GHz max [115]. Also, CTs are very bulky in size and therefore will occupy a large circuit board area [116], which will yield longer copper traces required for larger separation between the components and thus larger power loop inductances. Alternatively, Rogowski coils can be used, but their bandwidths are severely limited to 30MHz and their measurement results are very sensitive to the position of the conductor within the coil area [116, 117]. Consequently, they were deemed unsuitable for precise switching energy measurements. In overall, the CSR was deemed to be the most viable candidate for the DUT current measurement in the switching test; a 0.5 Ω (SDN-50) CSR with 800MHz bandwidth [115] was used.

#### *3.1.3.2 Selection of voltage measurement method*

The similar principle was applied for selecting a method for the DUT drain voltage measurement. Two common types of voltage measurement probes are differential probes, singled-ended passive probes. As the source potential of the DUT is floating due to the presence of CSR, a differential probe may be used as an option. However, the high-voltage differential probes with voltage ratings exceeding 2.5 kV are limited in bandwidth (70MHz max) [118] and thus they were not chosen as a means of voltage measurement for this work. The single-ended passive probes, on the other hand, have much higher bandwidths in comparison to differential probes. For the DUT drain voltage measurement in this work, a 2.5 kV rated 300MHz single-ended passive probe with an attenuation ratio of 100:1 (RS-HV250) was used. For the DUT gate-to-source voltage measurement, a Pintek DP-25 differential voltage probe with a bandwidth of 25MHz was used as the source potential was floating due to CSR.

#### *3.1.3.3 Probe de-skewing*

For an accurate measurement of switching energy losses, it is crucial to ensure that the probes connected to different oscilloscope channels are properly de-skewed as different time delays are introduced for each channel and probe. The circuit presented in Figure 3-17 was used to de-skew the voltage probes and thus synchronise the signals. Initially, the manual latch-type switch is open and thus $V_{DC,out}$ stays at 0 V and the $C_{DC}$ is charged up to $V_{DC}$. When the switch is manually closed, a current starts to flow through $R_{DC}$ and $V_{DC,out}$ gradually rises to $V_{DC}$. Therefore, by measuring the rising edge of $V_{DC,out}$, the propagation delay of differential probe relative to single-ended voltage probes can be determined. By

using this method, the Pintek DP-25 differential probe was skewed by 17 ns with respect to RS-HV250 probe.

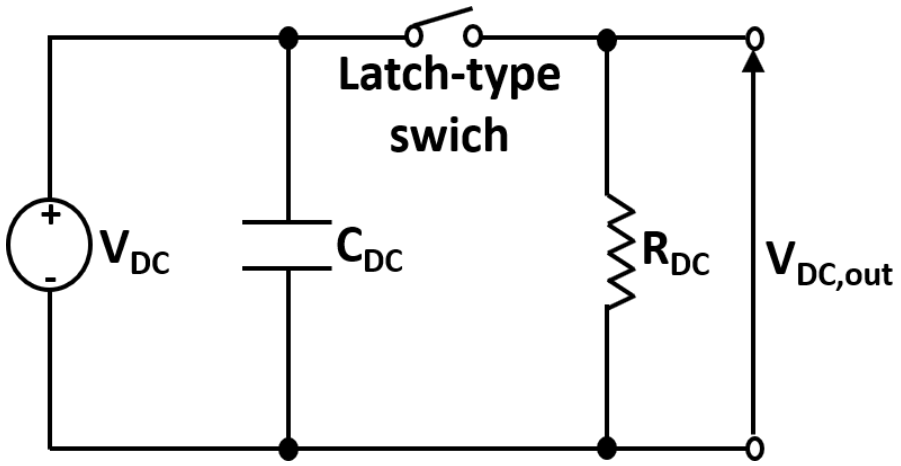



*Figure 3-17: Voltage probe de-skew circuit*

For the CSR with BNC output, the method presented in [116] was used. The CSR output de-skew was adjusted so that its rising edge is aligned with the $V_{ds}$ falling edge when the first gate drive pulse is applied. This occurs due to the discharging of $C_{oss}$ of DUT and junction capacitances of APD and FWD at the first turn-on event [116]. The CSR was skewed by 2 ns with respect to the RS-HV250 probe for synchronized signal measurements.

#### *3.1.3.4 High-temperature setup*

In order to assess the changes in turn-on and turn-off switching performances of the new large-area PSJ-FET with its $T_j$, the DUT was mounted onto an Aluminium heating plate with two 18 Ω heating resistors mounted on its opposite side as shown in Figure 3-18. The temperature of the heating plate was monitored via Testo 925 digital thermometer with a thermocouple wire inserted into a small hole drilled onto the plate beneath the DUT. The current through the heating resistors was then controlled manually in order to adjust the heating temperature. A

single layer of copper wires was wounded onto each of the two C26 powdered iron cores to form a load inductor with a total inductance of 1.3mH. The testbench was stored within a polycarbonate enclosure with safety features installed including an interlock and emergency stop button in order to ensure full safety of the user during the high-voltage test.

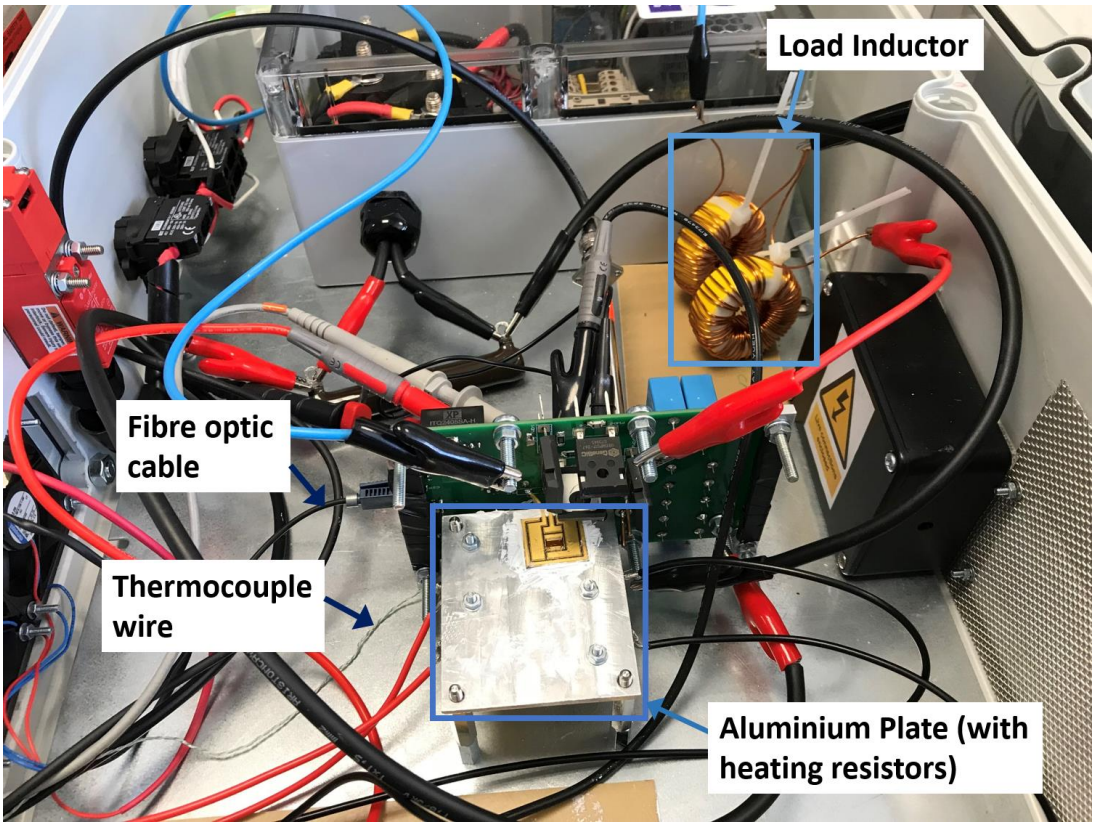



*Figure 3-18: High temperature switching test setup for GaN-PSJ device*

### *3.1.3.5 Switching behaviours at room temperature*

The turn-on and turn-off switching waveforms of the large-area PSJ sample extracted from the switching test are presented in Figure 3-19(a) and (b), respectively. The turn-on transition time consists of $I_d$ rise time ($t_{Id,rise}$) and $V_{ds}$ fall time ($t_{Vds,fall}$) whilst the turn-off transition time ($t_{off,total}$) consists of turn-off delay time ($t_{off,delay}$) and $V_{ds}$ rise time ($t_{Vds,rise}$). This is because the drop in $I_d$ and rise in

$V_{ds}$ occurred at the same time during turn-off as shown in Figure 3-19(b). Its Miller capacitance ($C_{gd}$) was estimated using the equation (3-4) during turn-on and turn-off transients and are shown in Figure 3-20. The equation was derived based on an assumption that the total gate current is used for discharging $C_{gd}$ during the $V_{ds}$ fall period.

$$C_{gd,est} \approx \frac{V_{gs,miller} - V_{drive}}{R_{g,tot(on)} \cdot \frac{\Delta V_{ds}}{\Delta t}} \quad \ldots(3\text{-}4)$$

Where $R_{g,tot(on)}$ = total resistance present in the turn-on gate drive loop, $V_{drive}$ = turn-on / off gate drive voltage, $V_{gs,miller}$ = $V_{gs}$ value during the $V_{ds}$ fall / rise intervals and $\Delta V_{ds} / \Delta t = V_{ds}$ slew rate. The $V_{gs,miller}$ values were extracted from the I-V curves in Figure 3-2(a), and assuming that the device transconductance ($g_m$) is constant, it can be mathematically expressed as:

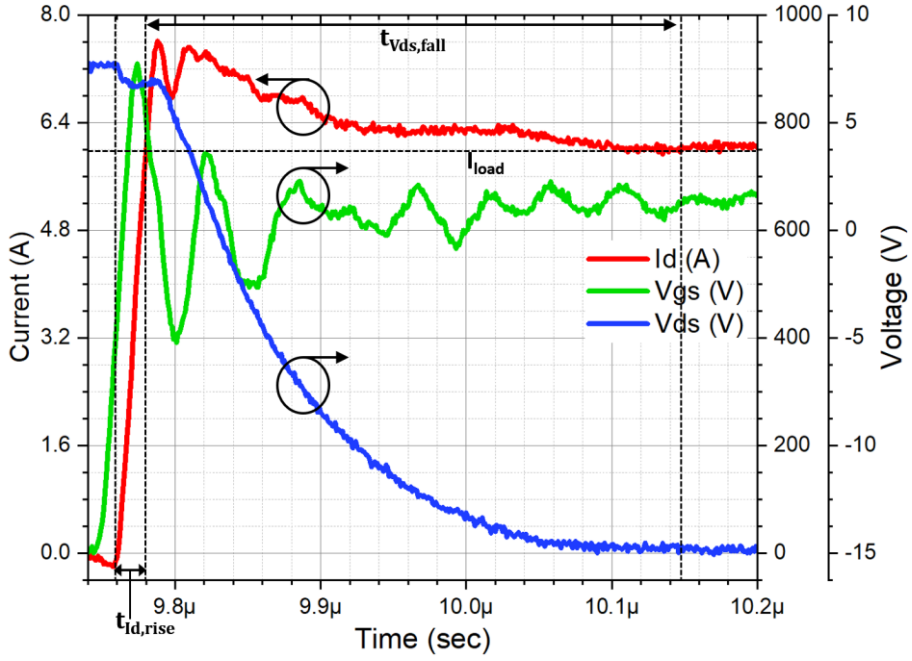
$$V_{gs,miller} = \frac{I_{ch,sat}}{g_m} + V_{gs,th} \quad \ldots(3\text{-}5)$$

Where $I_{ch,sat}$ = saturated channel current of the power device.

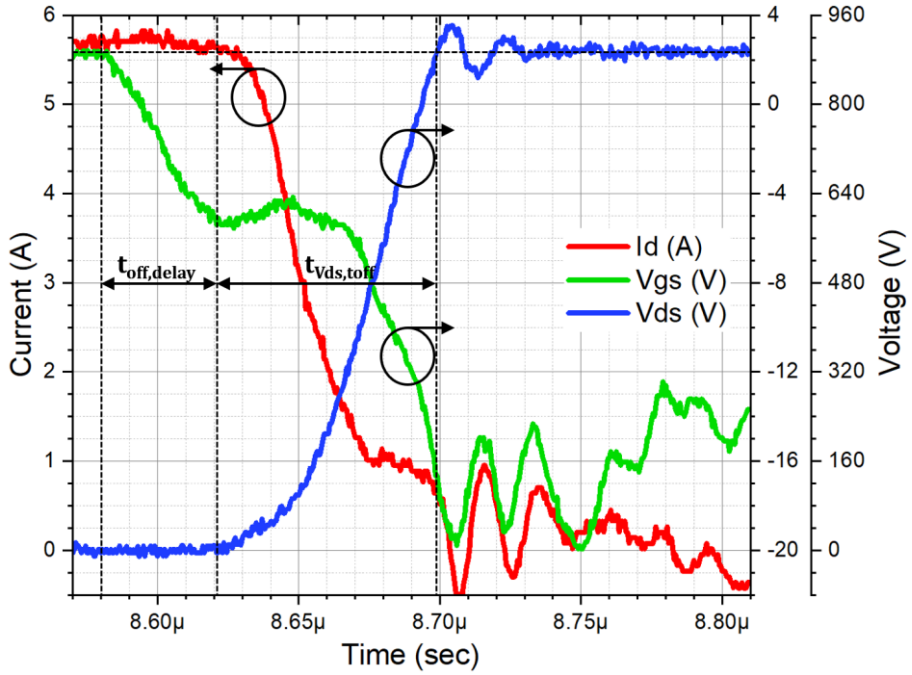
For this work, the external gate resistances ($R_{g,ext}$) of 3.3 Ω and 12 Ω were used for the turn-on and turn-off gate drives of the PSJ-FET, respectively. The minimum value of turn-off $R_{g,ext}$ was chosen using the equation (2-16) with the $C_{iss}$ value measured and presented in Figure 3-11(a) and lumped $L_{GL}$ value for the PSJ device packaging and gate drive PCB traces extracted via Ansys Q3D tool. The smaller $R_{g,ext}$ value was used for its turn-on gate drive loop compared to its turn-off counterpart since the $C_{iss}$ increased significantly to nFs range when the device is turned on i.e. $V_{gs}$ > -5 V and hence much less resistance is required for critical damping. During the turn-on transient, the $I_d$ rise time and $V_{ds}$ fall time (both from

10% to 90% of its final value) were determined as 15 ns and 180 ns, respectively. It can also be observed from Figure 3-19(a) that the slope $dV_{ds}/dt$ decreased as $V_{ds}$ becomes lower, which implied that $C_{gd}$ increased exponentially with the decrease in $V_{ds}$ (as shown in Figure 3-20) when the PSJ-FET is in its 'on' state and carries the full load current. This led to a prolonged turn-on transition time and thus increase in turn-on energy loss of the device.

During the turn-off transition, on the other hand, the $V_{ds}$ rise time was measured as 42.5 ns and $I_d$ decreased to the value much smaller than the load current during the $V_{ds}$ transition as the load current was partially diverted to charge and discharge the junction capacitances of APDs and FWDs ($C_{j,APD}$ and $C_{j,FWD}$). Also, according to Figure 3-20, the $C_{gd}$ values during turn-off were estimated to be much smaller than its turn-on counterparts, which has led to a much shorter $V_{ds}$ transition time and thus smaller turn-off energy loss compared to its turn-on energy loss. As $I^2R$ conduction loss decreases for lower $I_{load}$, the turn-on switching loss will become the dominant factor in the power loss analysis of the PSJ-FETs operating in high-voltage, low-current power converters and increase linearly with its switching frequency.




(a)




(b)

*Figure 3-19: Typical (a) turn-on and (b) turn-off $V_{ds}$, $V_{gs}$ and $I_d$ waveforms of the large area PSJ-FET under 900V dc-link and $I_{load}$ = 6 A with $R_{g,ext(on)}$ = 3.3Ω and $R_{g,ext(off)}$ = 12Ω at room temperature*

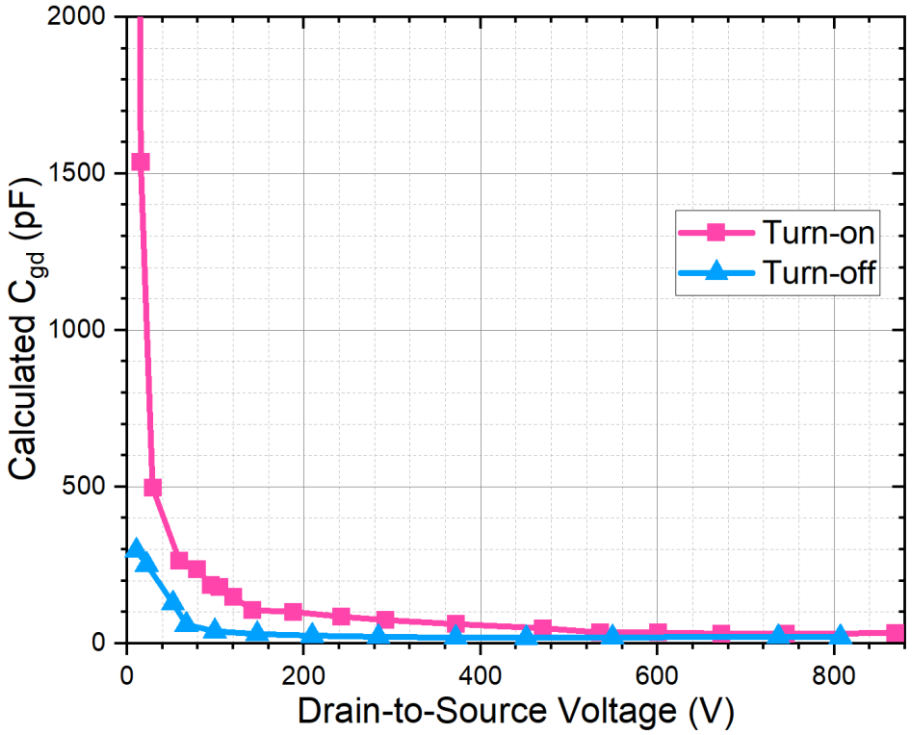



*Figure 3-20: Estimated $C_{gd}$ vs. $V_{ds}$ of the large area PSJ-FET obtained from typical turn-on and turn-off waveforms in Figure 3-18(a) and (b)*

The PSJ-FET switching performance was also evaluated for various external gate resistances at room temperature; 6.8 Ω, 10 Ω, 12 Ω and 15 Ω for turn-on and 15 Ω, 18 Ω and 22 Ω for turn-off. The turn-on voltage and current waveforms for $R_{g,ext(on)}$ = 3.3 Ω and 15 Ω at $I_{load}$ = 6 A are compared to each other in Figure 3-21. The turn-off waveforms for $R_{g,ext(off)}$ = 12 Ω and 22 Ω at $I_{load}$ = 2 A and 6 A were synchronised and presented for comparison in Figure 3-22(a) and (b), respectively. The $dV_{ds}/dt$ measured from 10% to 90% of its target value (i.e. DC-link voltage) or vice versa for two different $R_{g,ext(off)}$ and $I_{load}$ values were extracted and presented in Table 3-1. From the table, it can be seen that the turn-off dV/dt did not change remarkably with an increase in $R_{g,ext(off)}$ for both $I_{load}$ values. However, the dI/dt has decreased by 22.32% as $R_{g,ext(off)}$ increased from 12 Ω to 22 Ω, which led to a slight increase in $E_{off}$ as will be discussed later.

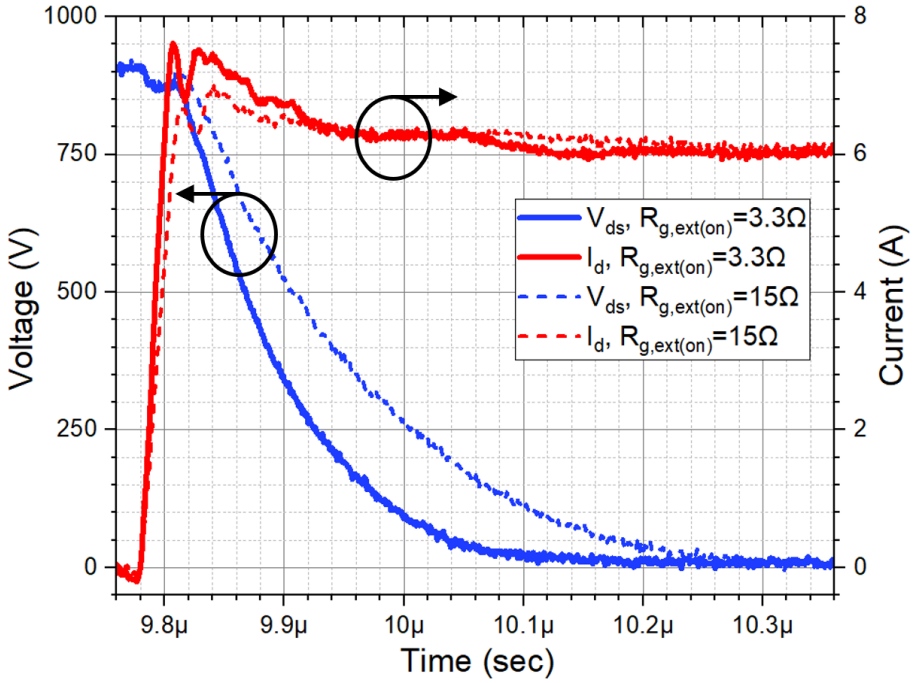
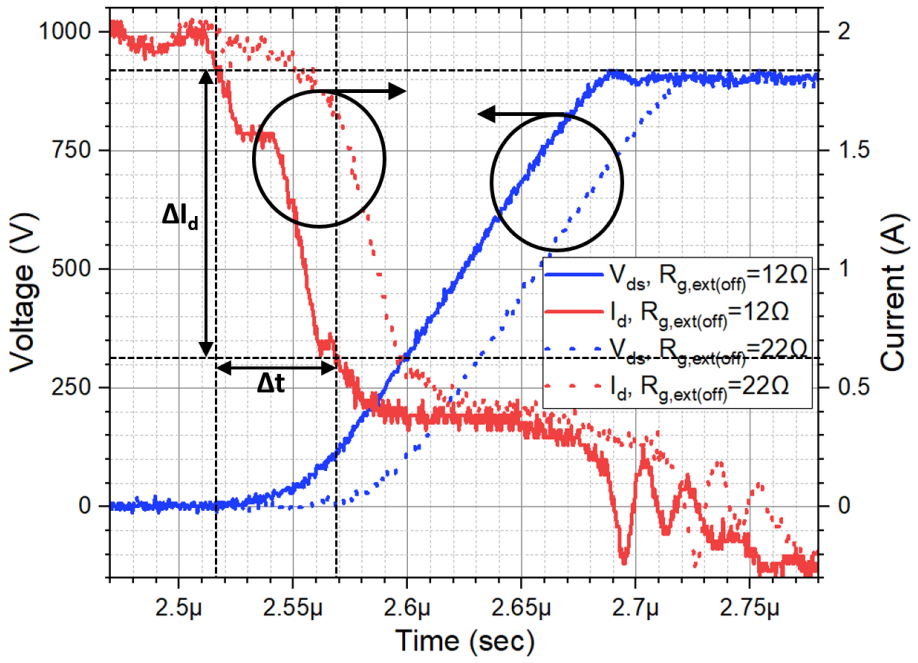
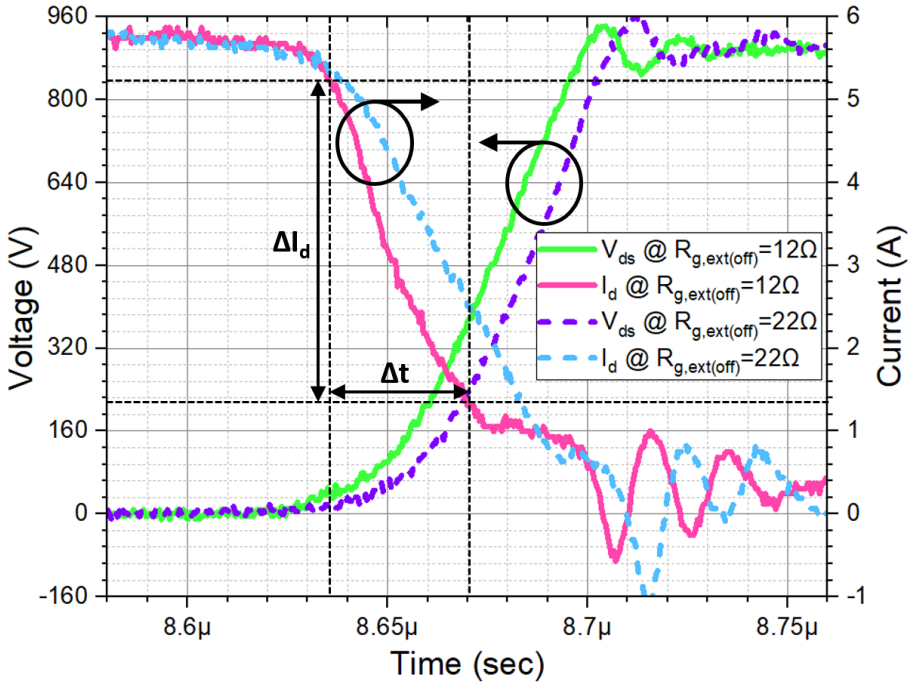



*Figure 3-21: Comparison of typical turn-on $V_{ds}$ and $I_d$ waveforms of the large-area PSJ-FET for $R_{g,ext(on)}$ = 3.3Ω and 15Ω at $I_{load}$ = 6 A*




(a)




(b)

*Figure 3-22: Comparison of typical turn-off $V_{ds}$ rise and $I_d$ fall waveforms of the large-area PSJ-FET for Rg,ext(off) = 12 Ω and 22 Ω at $I_{load}$ =(a) 2 A and (b) 6 A*

| Paramaters | $dV_{ds}$ / dt (turn-off) | | $dI_d$ /dt (turn-off) | |
|---|---|---|---|---|
| | $I_{load}$ = 2 A | $I_{load}$ = 6 A | $I_{load}$ = 2 A | $I_{load}$ = 6 A |
| $R_{g,ext(off)}$ = 12 Ω | 6.805 | 18.173 | 0.023 | 0.112 |
| $R_{g,ext(off)}$ = 22 Ω | 6.797 | 17.227 | 0.027 | 0.087 |

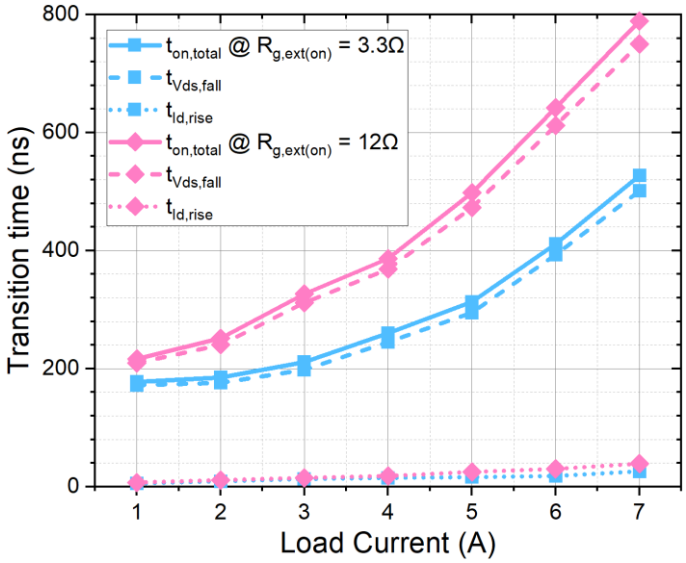
*Table 3-1: Typical turn-off dV/dt and dI/dt of the scaled up PSJ transistor for $I_{load}$ = 2 A and 6 A and $R_{g,ext(off)}$ = 12 Ω and 22 Ω at room temperature*

The total turn-on and turn-off transition times of the large-area PSJ device for two different external resistance values were calculated from the measured waveforms and are presented in Figure 3-23(a) and (b), respectively. The resultant $dV_{ds}/dt$ and $dI_d/dt$ values for turn-on and turn-off transients are plotted as a function of $R_{g,ext}$ in Figure 3-24. The turn-on transition time ($t_{on,total}$) consists of drain current rise time ($t_{Id,rise}$) and drain voltage fall time ($t_{Vds,fall}$). The detailed derivation of voltage and current waveforms at each switching time interval are included in the

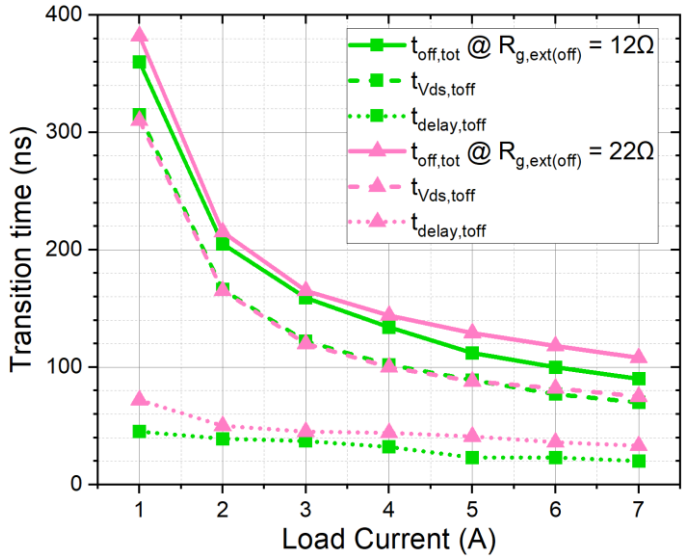
appendix (Section 7.2). From Figure 3-23(a), it can be observed that the $t_{on,total}$ increases exponentially with the $I_{load}$ and is dominated by $t_{Vds,fall}$. This is due to an increase in $V_{gs,miller}$ (defined in equation (3-5)) with $I_{load}$ that yields less gate current for charging $C_{gd}$ and lower dV/dt slew as according to the equation:

$$\left|\frac{dV_{ds}}{dt}\right| = \frac{V_{drv,on} - V_{gs,miller}}{R_{g,tot(on)} \cdot C_{gd}} \quad \ldots(3\text{-}6)$$

Also, the $t_{Id,rise}$ and $t_{Vds,fall}$ at $I_{load}$ = 6 A increased by 66.67% and 63.36% as $R_{g,ext(on)}$ increased from 3.3 Ω to 12 Ω. On the other hand, the $t_{Id,rise}$ and $t_{Vds,fall}$ at $I_{load}$ < 2 A for both $R_{g,ext(on)}$ are very close to each other, which implies that the discharging of $C_{j,APD}$, $C_{j,FWD}$ and $C_{oss,DUT}$ was the dominant factor of the turn-on transition at $I_{load}$ < 2 A. These transition time values are dependent upon the type of diodes used for APD and FWD (i.e. Schottky or p-i-n rectifiers), their junction capacitances and the value of snubber capacitors placed in parallel to them. For the turn-off transition, on the other hand, it can be observed from Figure 3-23(b) that both the $t_{Vds,rise}$ and turn-off delay time ($t_{off,delay}$) decreased remarkably by factor of 4.13 and 2.18, respectively, as the $I_{load}$ increased from 1 A to 7 A. In addition, the $t_{Vds,rise}$ did not change remarkably with an increase in $R_{g,ext(off)}$ value from 12 Ω to 22 Ω at $I_{load}$ < 5 A.




(a)




(b)

*Figure 3-23: (a) Turn-on transition time vs. load inductor current for $R_{g,ext(on)}$ = 3.3 Ω and 12 Ω and (b) turn-off transition time vs. load inductor current for $R_{g,ext(off)}$ = 12 Ω and 22 Ω of the large-area PSJ-FET under 900V dc-link*

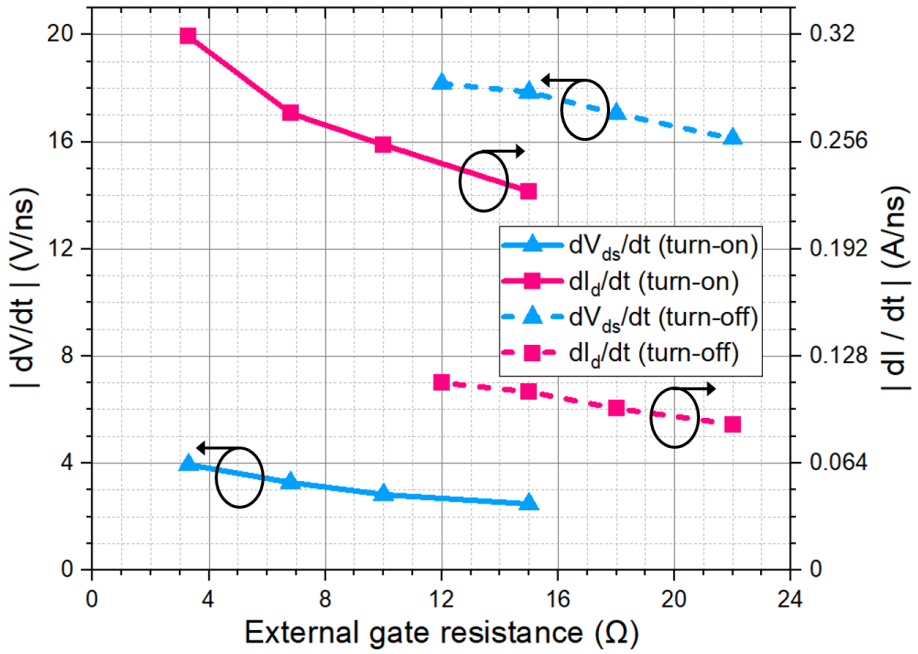



*Figure 3-24: Typical turn-on and turn-off $dV_{ds}/dt$ and $dI_d/dt$ vs. $R_{g,ext(on)}$ / $R_{g,ext(off)}$ of large area PSJ transistor at room temperature and $I_{load}$ = 6 A*

The typical turn-on and turn-off switching energy losses ($E_{on}$ and $E_{off}$) of the large-area PSJ transistor were calculated by integrating the $V_{ds}$ and $I_d$ waveforms for various $R_{g,ext(on/off)}$ values versus $I_{load}$ ranging from 1 A to 7 A and are plotted in Figure 3-24.

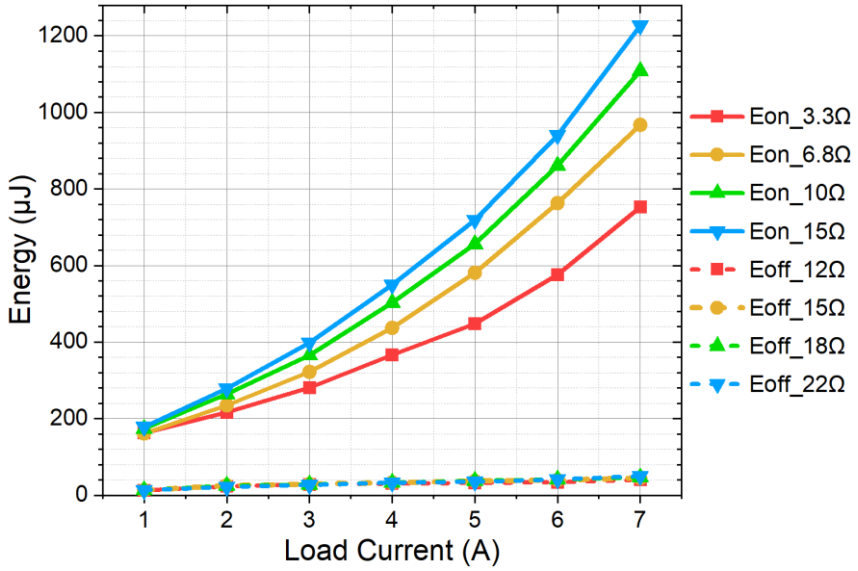



*Figure 3-25: Typical switching energy vs. Load current of the large-area PSJ-FET for $R_{g,ext(on)}$ = 3.3Ω, 6.8Ω, 10Ω and 15Ω and $R_{g,ext(off)}$ = 12 Ω, 15 Ω, 18 Ω and 22 Ω at room temperature and DC-link voltage of 900 V*

From Figure 3-25, it is also observed that turn-on energy ($E_{on}$) increased exponentially with the load current due to an exponential increase in $t_{Vds,fall}$ with $I_{load}$ as discussed previously. The $E_{on}$ also increased with $R_{g,ext(on)}$ value as dV/dt and dI/dt are proportional to the $I_g$ available during $I_d$ rise and $V_{ds}$ fall and $I_d$ rise intervals, respectively. The $E_{off}$, on the other hand, did not exhibit a remarkable increase with $R_{g,ext(off)}$ values because the transition time remained constant regardless of the variance in gate resistances. This implies that the $V_{ds}$ rise transition was dominated by the charging of APD, FWD and DUT junction capacitances via $I_{load}$ and hence zero current switching (ZCS) as illustrated in Figure 3-26. During the $V_{ds}$ rise period, the currents through the junction capacitances of APDs and FWDs are proportional to the available gate current that charges the $C_{gd}$ of DUT and will be diverted away from the DUT channel current ($I_{ch,DUT}$). The detailed mathematical derivation steps of the $V_{ds}$ and $I_d$ waveforms during this period are presented in the appendix (Section 7.2). For a fixed $I_{load}$, the minimum $V_{ds}$ rise time during the turn-off occurs when the whole $I_{load}$ is used for charging the total capacitance present at the switching node ($C_{node,tot}$) and thus the $I_{ch,DUT}$ decreases to zero during $V_{ds}$ rise interval (i.e. the DUT turns off in zero current switching (ZCS) mode), which can be expressed as:

$$t_{Vds,rise(min)} = \frac{Q_{gd} + Q_{ds} + Q_{j,APD} + Q_{j,FWD}}{I_{load}} \quad \ldots(3\text{-}7)$$

$Q_{gd}$ = Miller charge stored in $C_{gd}$ of DUT

$Q_{ds}$ = charge stored in drain-to-source junction of the DUT

$Q_{j,APD(FWD)}$ = charge stored in the APD and FWD junctions (depletion regions)

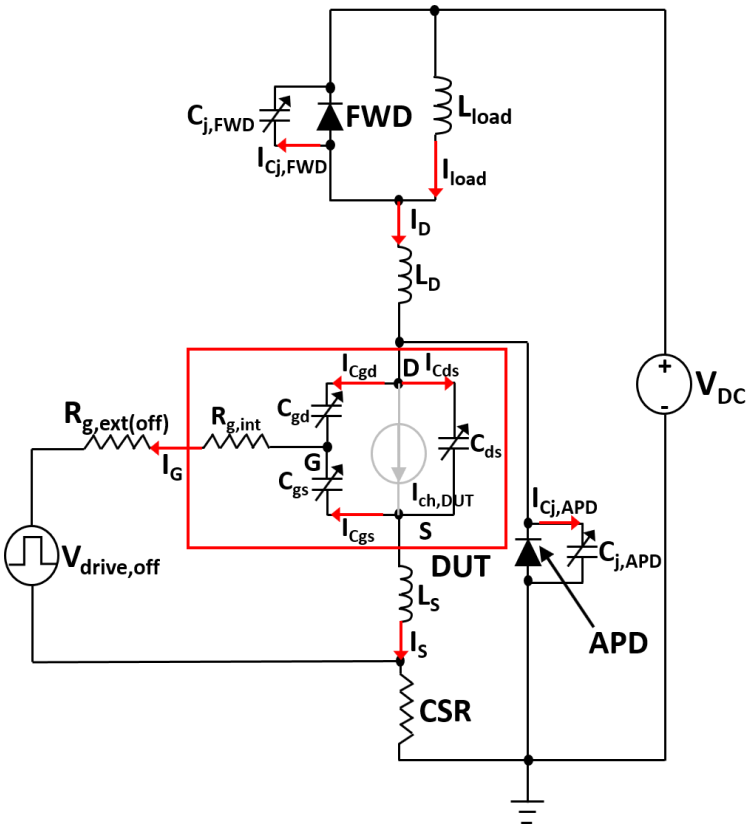


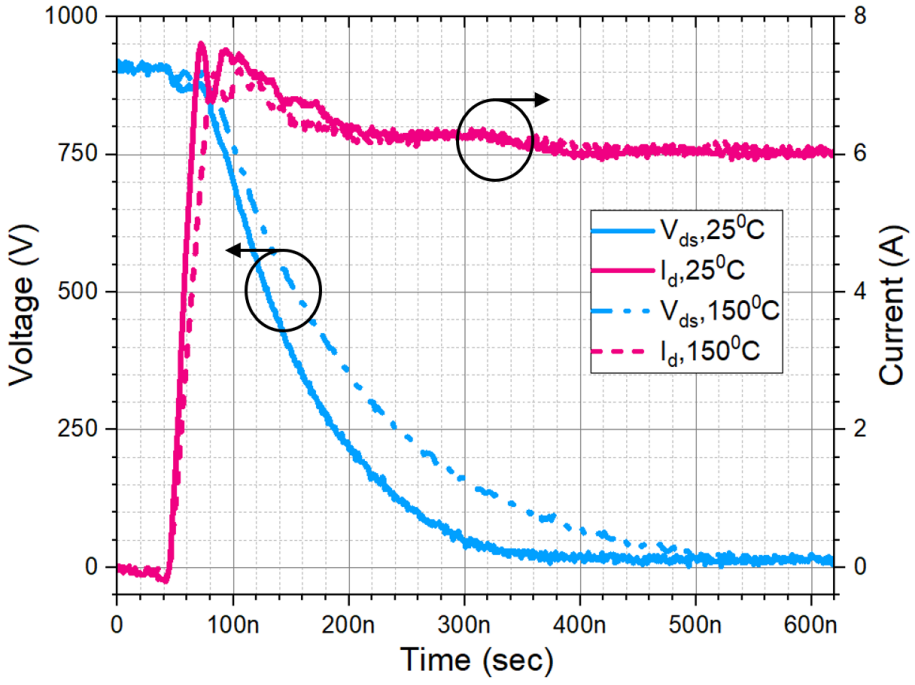

*Figure 3-26: DPT circuit schematic with current flow directions labelled and DUT turn-off at zero current switching (ZCS) mode*

### *3.1.3.6 Switching behaviours at high temperatures*

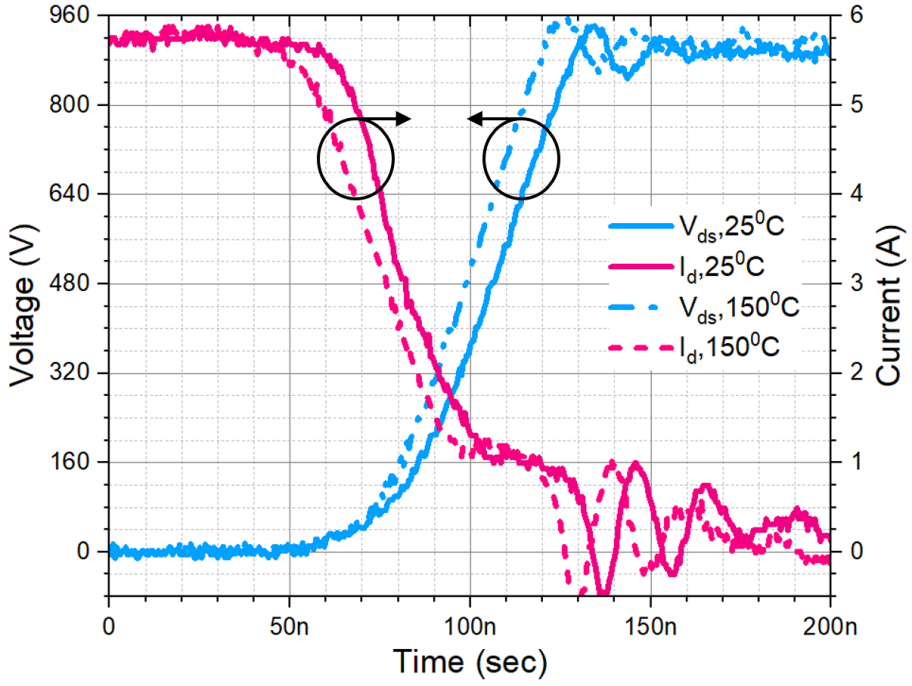
The effect of an increase in $T_j$ to the turn-on and turn-off performances of the scaled up PSJ device can be clearly observed in the switching $V_{ds}$ and $I_d$ waveforms in Figure 3-27(a) and (b), respectively. The typical turn-on and turn-off $|dV_{ds}/dt|$ and $|dI_d/dt|$ values were extracted for various external gate resistance values and plotted in Figure 3-28. As $T_j$ increased, its $g_m$ was reduced and therefore higher $V_{gs,miller}$ (defined in (3-5)) is required for the same $I_{load}$ compared to its room temperature counterpart. Therefore, the gate current for charging the $C_{iss}$ of the DUT has decreased, which led to 33% and 31.62% reduction in $|dV_{ds}/dt|$ and $|dI_d/dt|$ during its turn-on when $T_j$ has increased from room temperature to $150^0$C, respectively. This led to a remarkable increase in $E_{on}$ with $T_j$ as shown in the switching energy

vs. load current curves for various $T_j$ in Figure 3-29. As can be observed from the plotted curves, the $E_{on}$ increased exponentially with $I_{load}$ and its rate of increase has risen with $T_j$. At $I_{load}$ = 3 A and 6 A, the $E_{on}$ increased by 32.88% and 65.43%, respectively, as $T_j$ increased from $25^0$C to $150^0$C.

On the other hand, the total $t_{off,total}$ decreased slightly as the time delay $t_{delay,toff}$ (defined in Section 3.1.3.5) was shortened since $g_m$ has decreased with $T_j$ and hence the decrease in $I_d$ took place at an earlier point of time compared to when $T_j$ =$25^0$C. Nevertheless, as shown in Figure 3-28, the typical $dV_{ds}/dt$ and $dI_d/dt$ was determined to be independent of $T_j$, which proves that the turn-off behaviour of the PSJ transistor was dominated by the capacitances of diode junction and DUT $C_{oss}$ that are charged and/or discharged via $I_{load}$ as illustrated in Figure 3-26. Consequently, minimal change in $E_{off}$ with $T_j$ was observed as presented in Figure 3-29. The $E_{off}$ value is dependent upon FWD and APD junction capacitances and hence must be re-evaluated if alternative diode parts are to be used in the future.




(a)




(b)

*Figure 3-27: Comparison of (a) turn-on and (b) turn-off $V_{ds}$ and $I_d$ waveforms for $T_j$ = 25$^0$C and 150$^0$C at $V_{dc}$ = 900 V and $I_{load}$ = 6 A*

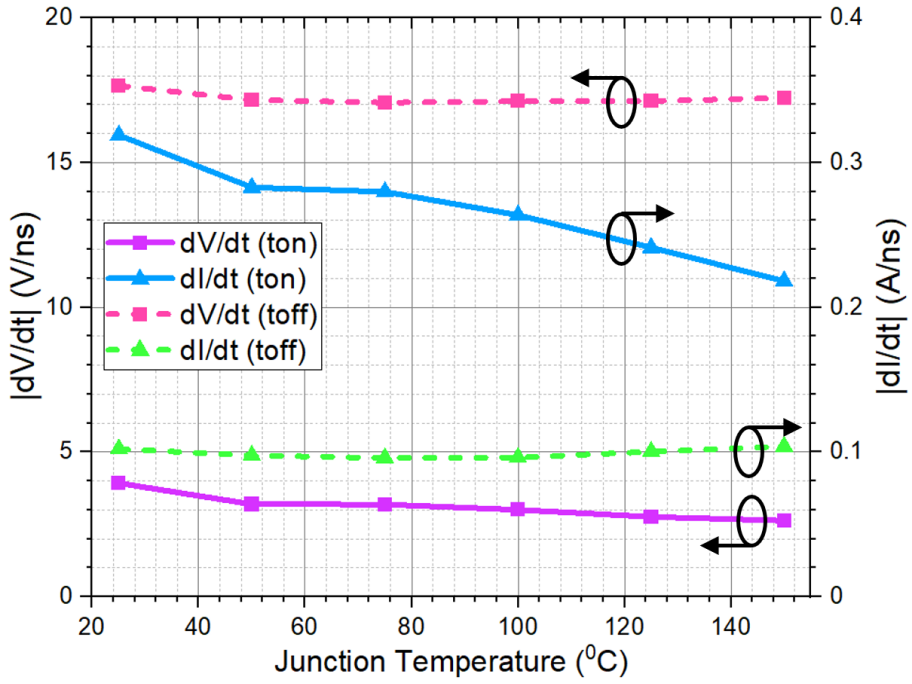



*Figure 3-28: Typical turn-on and turn-off |dV/dt| and |dI/dt| vs. junction temperature of large area PSJ transistors ($W_g$ = 148mm, $L_{psj}$ = 40 µm) at $V_{dc}$ = 900 V and $I_{load}$ = 6 A*

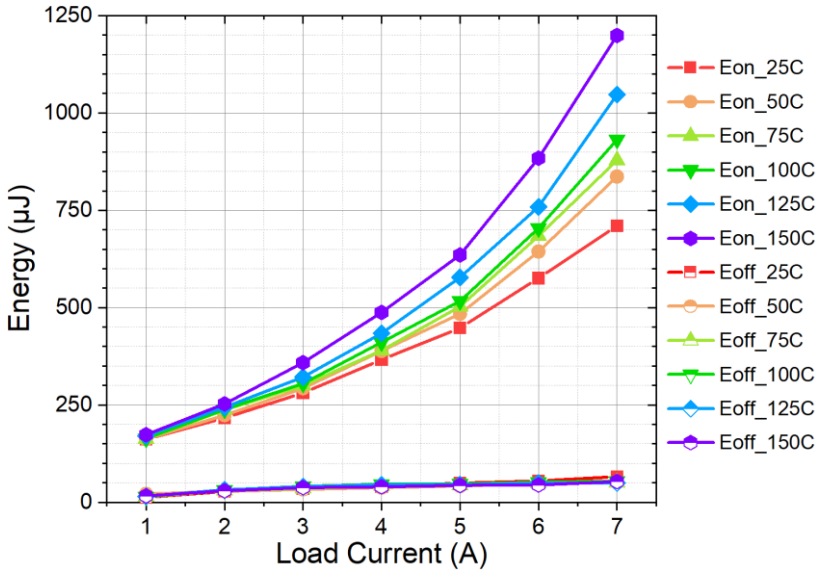


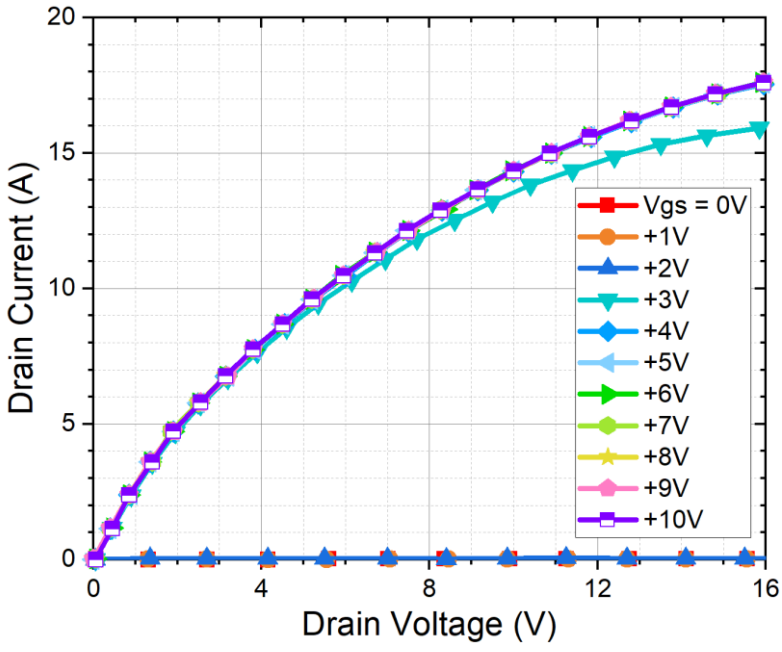

*Figure 3-29: PSJ-FET switching energy loss vs. load current at 900 V dc-link and $T_j$ = $25^0$C, $50^0$C, $75^0$C, $100^0$C, $125^0$C and $150^0$C*

## *3.2. E-mode cascode PSJ performance and comparison*

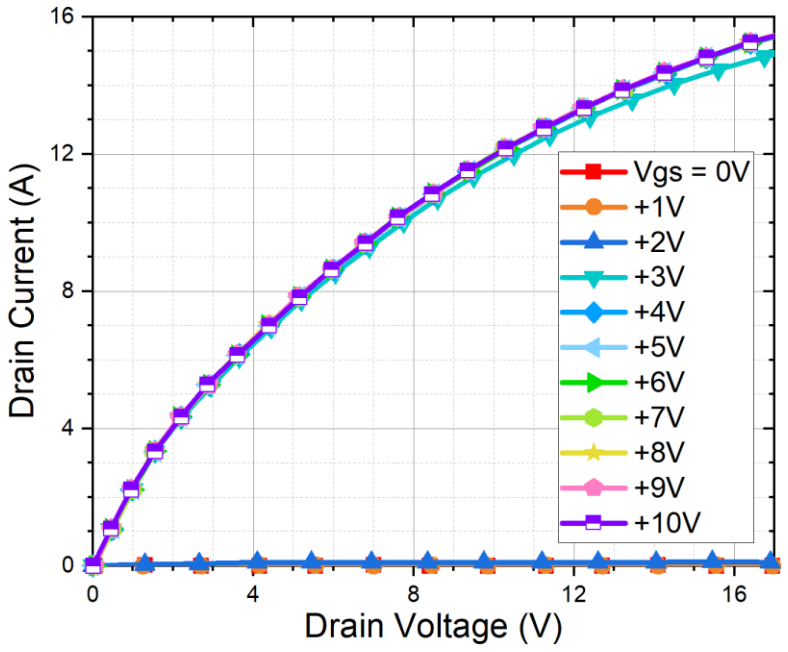
As per static I-V characteristic curves in Figure 3-2(a)~(f), the PSJ-FETs are inherently depletion-mode (D-mode) devices, which makes them unsuitable for fail-safe operation of power converters. Therefore, it is necessary to modify the device structure or configuration to achieve E-mode functionality using the E-mode GaN device technologies in Chapter 2. Amongst these options, cascode GaN was chosen for this work as it does not require any etching or ion implantation in D-mode GaN device active area and thus yields minimum compromise in its on-state performance. The bare dies of D-mode PSJ-FET were mounted onto the direct copper bond (DCB) substrate and co-packed with 30 V, 4 mΩ Si-MOSFET dies (IPC042N03L3) using FEK Delvotec 5410 wire bonder machine. The Si-MOSFET was chosen so that the $R_{ds,on}$ of cascode structure is kept minimal. The static and dynamic characteristics of the cascode PSJ device were measured using the same method as for its D-mode counterpart and compared against it.

### *3.2.1. Static I-V characteristics*

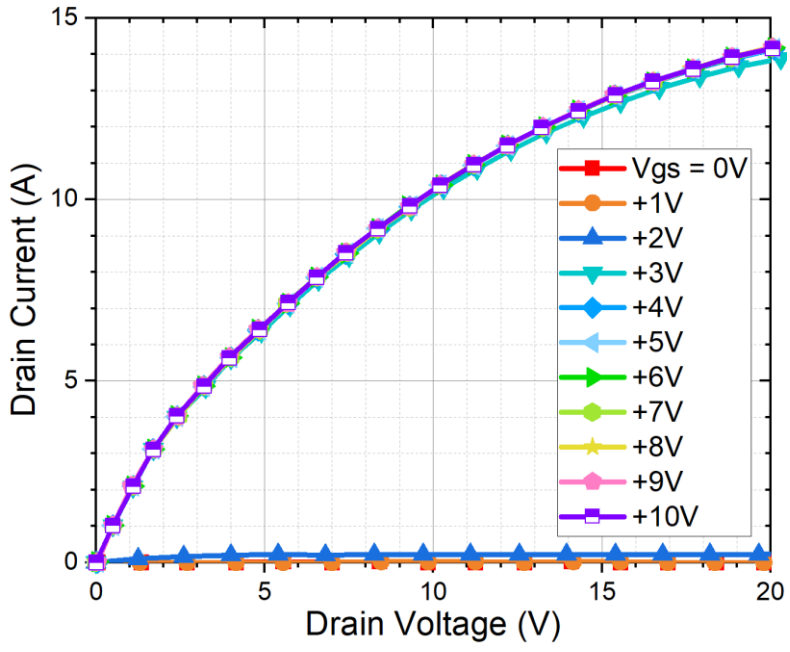
The static forward I-V characteristics of the cascode PSJ device at device temperatures ranging from room temperature to $150^0$C were measured using Tektronix 371B curve tracer and Heraeus oven and presented in Figure 3-30(a) to (f). As observed from Figure 3-30(a), (b) and (c), the on-state I-V characteristic curves for the range $V_{gs} > 4$ V are identical to each other. The $V_{gs} = 3$ V corresponds to the $V_{gs,th}$ of the Si-MOSFET at room temperature. This shows that the $R_{ds,on}$ of the Si-MOSFET is extremely small so that negligible on-state voltage drop is present across it and thus the effective $V_{gs}$ of the D-mode PSJ device in the cascode structure is maintained as ~0 V. It is also notable that the drain current output at $V_{gs}$ = +2 V increased remarkably with $T_j$. Also, as observed from Figure 3-30(d), (e) and (f), the characteristic curve for $V_{gs}$ = +3 V became identical to the curves for $V_{gs}$ = +4 V to +10 V. These phenomena occurred due to the negative shift in $V_{gs,Si}$ of Si-MOSFET with $T_j$, which is coherent with the data in its datasheet [119].



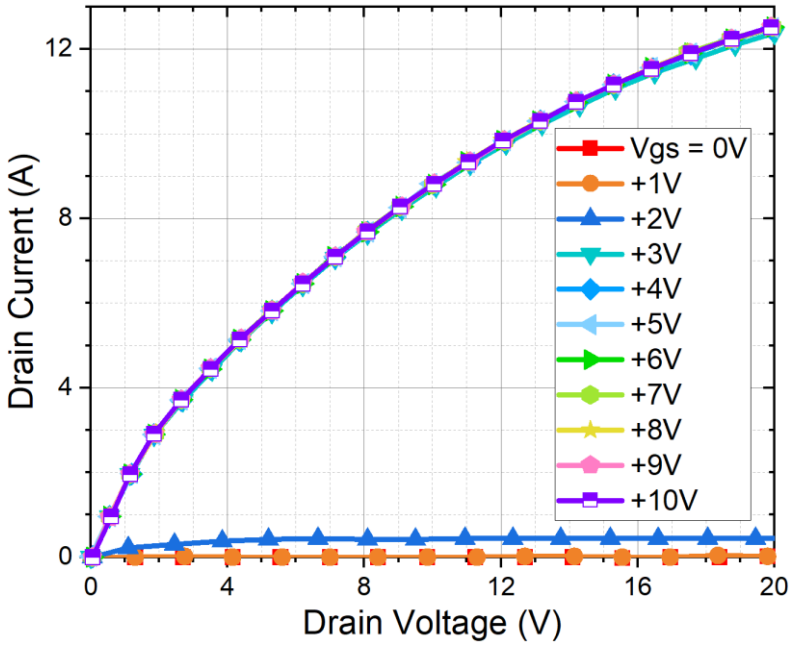
(a)


Drain Current (A)
Drain Voltage (V)
Vgs = 0V
+1V
+2V
+3V
+4V
+5V
+6V
+7V
+8V
+9V
+10V
0
4
8
12
16

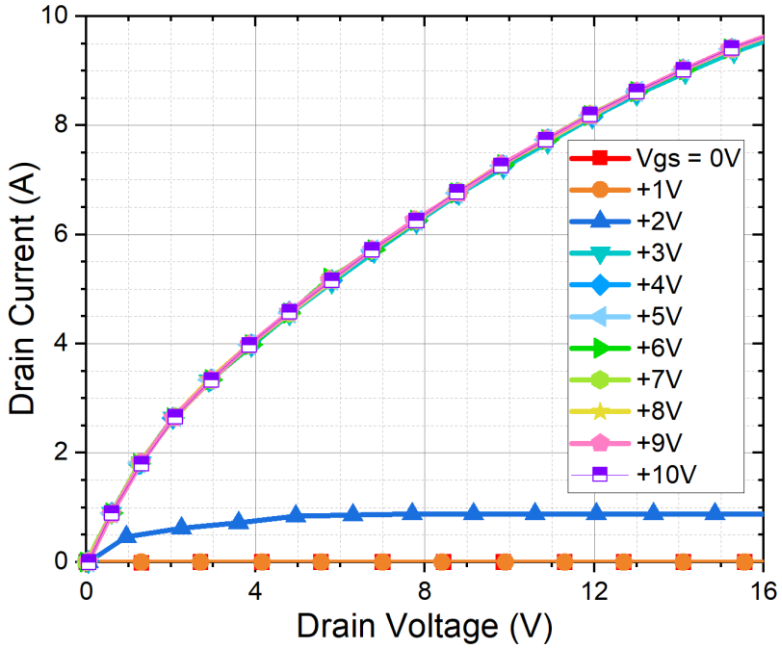
(b)


Drain Current (A)
Drain Voltage (V)
Vgs = 0V
+1V
+2V
+3V
+4V
+5V
+6V
+7V
+8V
+9V
+10V
0
5
10
15
20

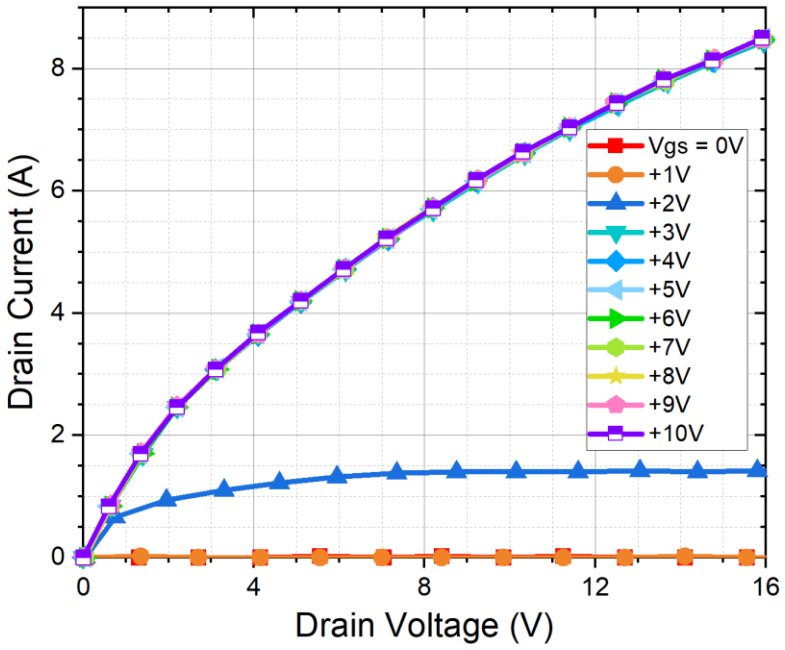
(c)


Drain Current (A)
Drain Voltage (V)
Vgs = 0V
+1V
+2V
+3V
+4V
+5V
+6V
+7V
+8V
+9V
+10V
0
4
8
12
16
20

(d)


Drain Current (A)
Drain Voltage (V)
Vgs = 0V
+1V
+2V
+3V
+4V
+5V
+6V
+7V
+8V
+9V
+10V
0
2
4
6
8
10
12
16

(e)




(f)

*Figure 3-30: Typical on-state I-V characteristics curves of E-mode cascode PSJ-FET at device temperatures of (a) 25$^0$C, (b) 50$^0$C, (c) 75$^0$C, (d) 100$^0$C, (e) 125$^0$C and (f) 150$^0$C.*

### *3.2.2. Internal capacitance-voltage characteristics*

Similar to its D-mode counterpart, the switching performance of the E-mode cascode GaN device is determined by its terminal capacitance characteristics. The small-signal ac current flow directions in a cascode GaN device for $C_{iss}$, $C_{oss}$ and $C_{rss}$ measurements when $V_{ds} < |V_{gs,th(GaN)}|$ and $V_{ds} > |V_{gs,th(GaN)}|$ are clearly indicated in Figure 3-31 and Figure 3-32. For $C_{rss}$ and $C_{oss}$ measurements, the small signal current flows through the D-mode GaN channel when $V_{ds} < |V_{gs,th(GaN)}|$ as the HV GaN stays on and LV Si-MOSFET is in off state; thus, Si-MOSFET withstands the full $V_{ds}$ in this case. Thus, the terminal capacitances in the cascode GaN in this case can be mathematically represented as following:

$$C_{oss,cascode} = C_{gd,GaN} + C_{gs,GaN} + C_{gd,Si} + C_{ds,Si} \quad \ldots(3\text{-}8)$$

$$C_{rss,cascode} = C_{gd,Si} \quad \ldots(3\text{-}9)$$

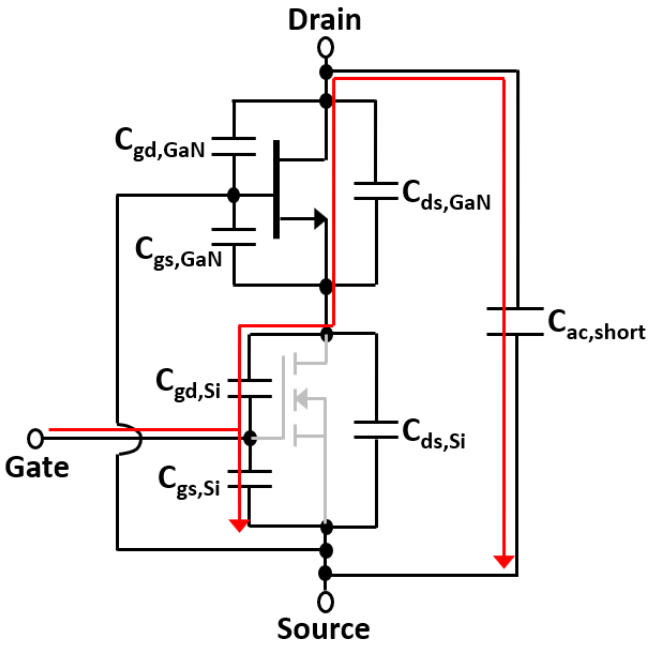
$$C_{iss,cascode} = C_{gs,Si} + C_{gd,Si} \quad \ldots(3\text{-}10)$$

However, when $V_{ds} \geq |V_{gs,th(GaN)}|$, the HV D-mode GaN device will be turned off and thus start to block the forward $V_{ds}$ bias applied. Also, the $V_{gs,GaN}$, equivalent $V_{ds,Si}$, will be clamped to a certain value determined by the off-state resistance of HV GaN and LV MOSFET placed in series. At the point where $V_{ds} = V_{gs,th(GaN)}$, both the $C_{rss}$ and $C_{oss}$ of cascode GaN decrease drastically as the GaN channel becomes pinched off and thus $C_{ds,GaN}$ is now in series with $C_{oss}$ of the LV MOSFET. The $C_{iss}$ will also decrease with $V_{ds}$ due to the same reason but to a much less extent if $C_{gs,Si}$ is the dominant factor of $C_{iss}$. Thus, the effective terminal capacitances of cascode GaN device when $V_{ds} \geq |V_{gs,th(GaN)}|$ can be mathematically expressed as:

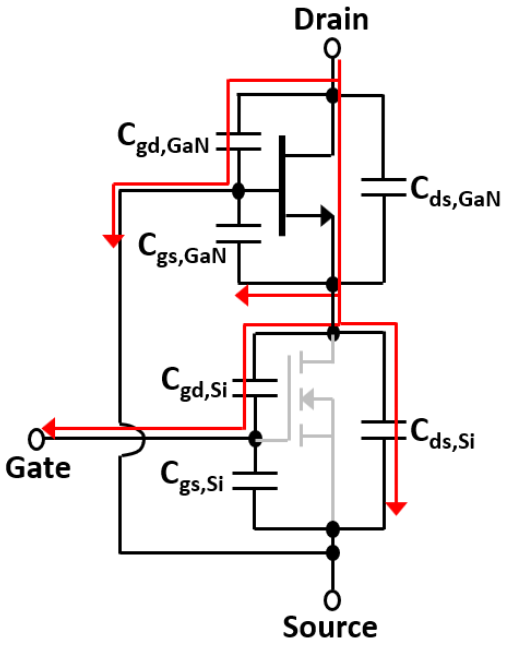
$$C_{oss,cascode} = C_{gd,GaN} + \frac{C_{ds,GaN} \cdot \left(C_{gs,GaN} + C_{ds,GaN} + C_{ds,Si}\right)}{C_{gd,Si} + C_{gs,GaN} + C_{ds,GaN} + C_{ds,Si}} \quad \ldots(3\text{-}11)$$

$$C_{rss,cascode} = \frac{C_{ds,GaN} \cdot C_{gd,Si}}{C_{gd,Si} + C_{gs,GaN} + C_{ds,GaN} + C_{ds,Si}} \quad \ldots(3\text{-}12)$$

$$C_{iss,cascode} = C_{gs,Si} + \frac{C_{gd,Si} \cdot \left(C_{gs,GaN} + C_{ds,GaN} + C_{ds,Si}\right)}{C_{gd,Si} + C_{gs,GaN} + C_{ds,GaN} + C_{ds,Si}} \quad \ldots(3\text{-}13)$$

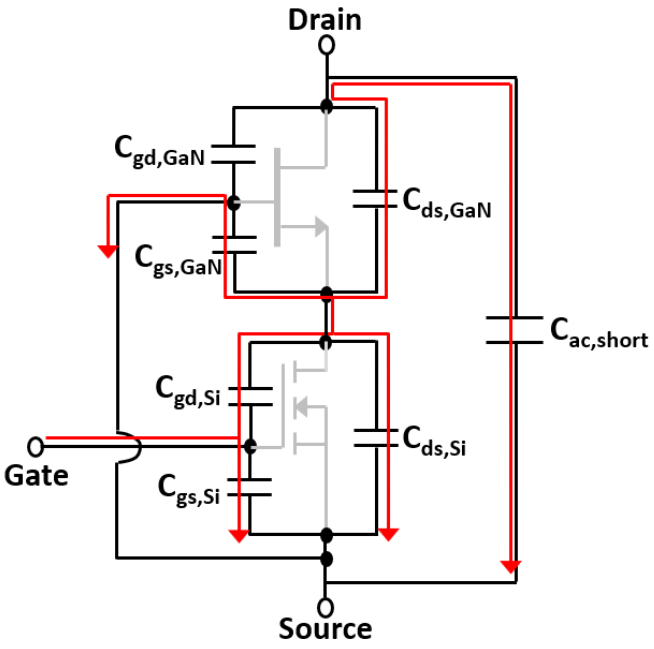



(a)

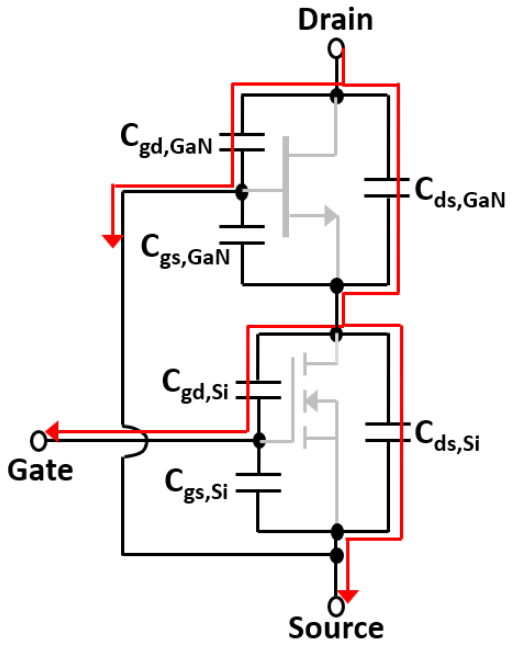



(b)

*Figure 3-31: Terminal capacitances in cascode GaN device with small signal ac current flow directions for (a) $C_{iss}$ and (b) $C_{oss}$ and $C_{rss}$ vs $V_{ds}$ measurements when $V_{ds} < |V_{gs,th(GaN)}|$*




(a)




(b)

*Figure 3-32: Terminal capacitances in cascode GaN device with small signal ac current flow directions for (a) $C_{iss}$ and (b) $C_{oss}$ and $C_{rss}$ vs $V_{ds}$ measurements when $V_{ds} > |V_{gs,th(GaN)}|$*

The C-V characteristics of a packaged cascode PSJ-FET was obtained using B1505A device analyser with the same circuit configurations in Figure 3-10. The resultant C-V characteristic curves are plotted in Figure 3-33. From the C-V curves,

a drastic fall in $C_{oss}$ and $C_{rss}$ is observed at $V_{ds}$ = 5 V, which corresponds to the absolute value of $V_{gs,th}$ of the D-mode PSJ-FET. On the other hand, the $C_{iss}$ was kept constant with $V_{ds}$ as $C_{iss,Si}$ >> $C_{rss,Si}$ as per datasheet and thus becomes the dominant factor. As the $C_{iss,cascode}$ is much higher than its D-mode PSJ counterpart, longer turn-on and turn-off delay times are expected. The measured typical $C_{oss,cascode}$ and $C_{oss,GaN}$ values at $V_{ds}$ = 200 V were 28.55 pF and 23.85 pF, respectively; hence, the measured $C_{oss,cascode}$ is larger than $C_{oss,GaN}$. However, the typical $C_{rss,cascode}$ and $C_{rss,GaN}$ at $V_{ds}$ = 200 V were measured as 2.6 pF and 18.82 pF, respectively, which led to a much shorter $V_{ds}$ transition times during turn-on and turn-off.

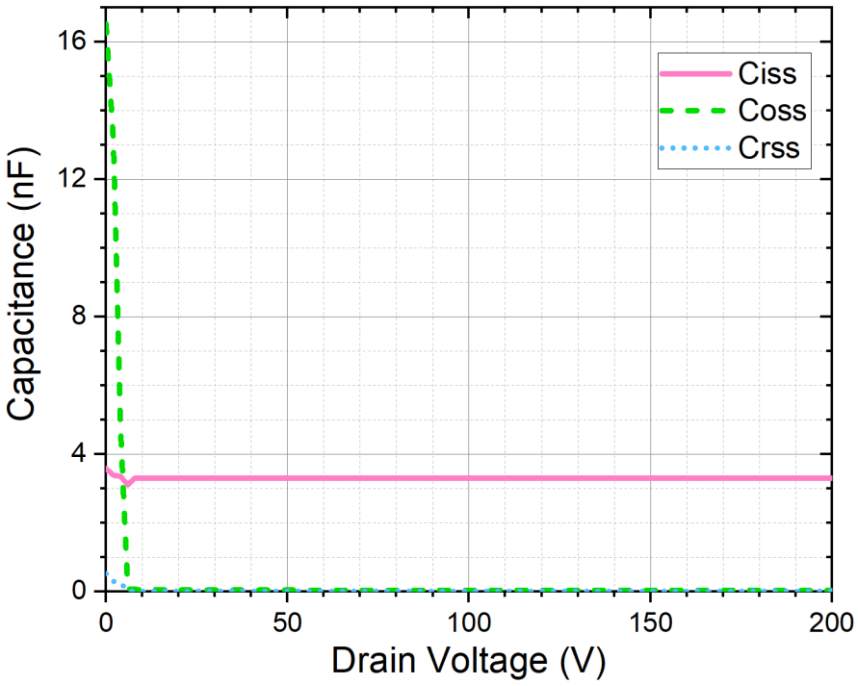



*Figure 3-33: Typical C-V characteristic curves of cascode PSJ-FET at AC frequency = 100 kHz, small signal magnitude = 50 mV and $V_{gs}$ = - 15V*

### *3.2.3. Switching characteristics*

The schematic of the DPT circuit for the cascode PSJ-FET is shown in Figure 3-34. Due to the connections to the DUT made via wires with crocodile clips and presence of bonded wires in its packaging, larger parasitic inductances were present

in the gate drive loop and main power loop compared to its standalone D-mode counterpart. Hence, in order to prevent excessive ringing in the $V_{gs}$ and thus gate drive instability, a ferrite bead was used in series with $R_{g,ext(on)}$ and $R_{g,ext(off)}$. For the DUT voltage and current measurements, the same voltage probes and CSR (SDN-50) as for D-mode PSJ-FET DPT were used and their de-skewing was performed using the same methodology described in section 3.1.3.3. In this circuit, the $I_{load}$ freewheels through the body diode of Si-MOSFET and the reverse-conducting 2DEG channel of PSJ-FET of the synchronous rectifier (SR) device. Therefore, reverse recovery of the Si-MOSFET will take place during the DUT turn-on process, which will have an impact on $E_{on}$ calculation for the cascode device.

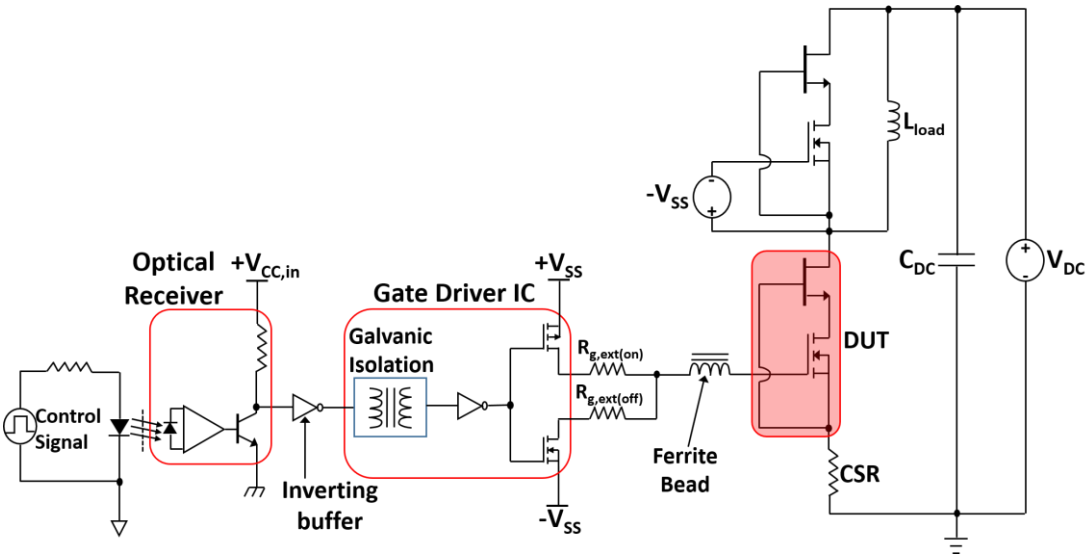
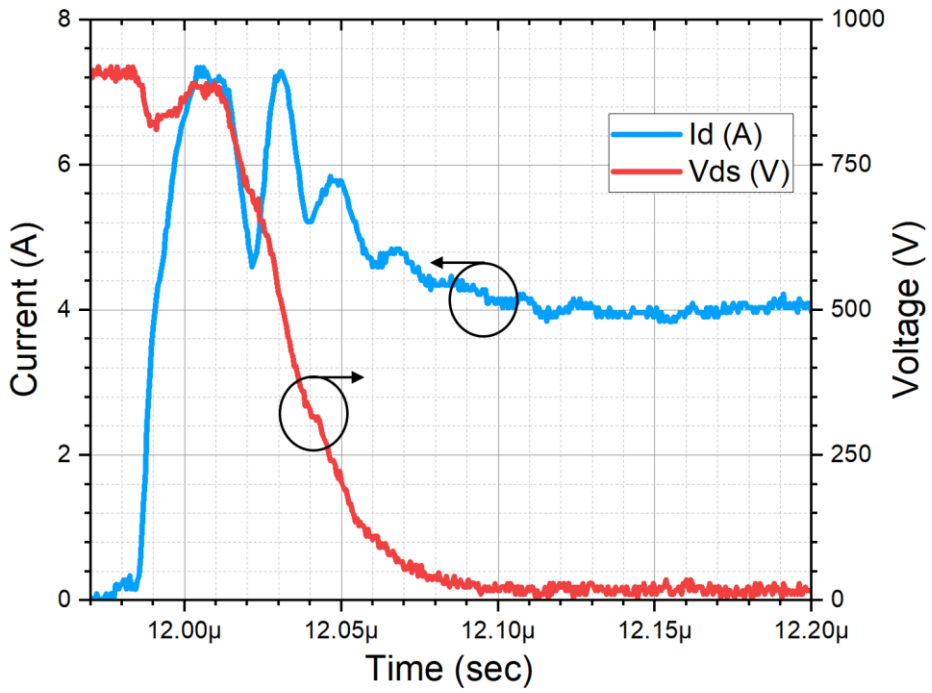


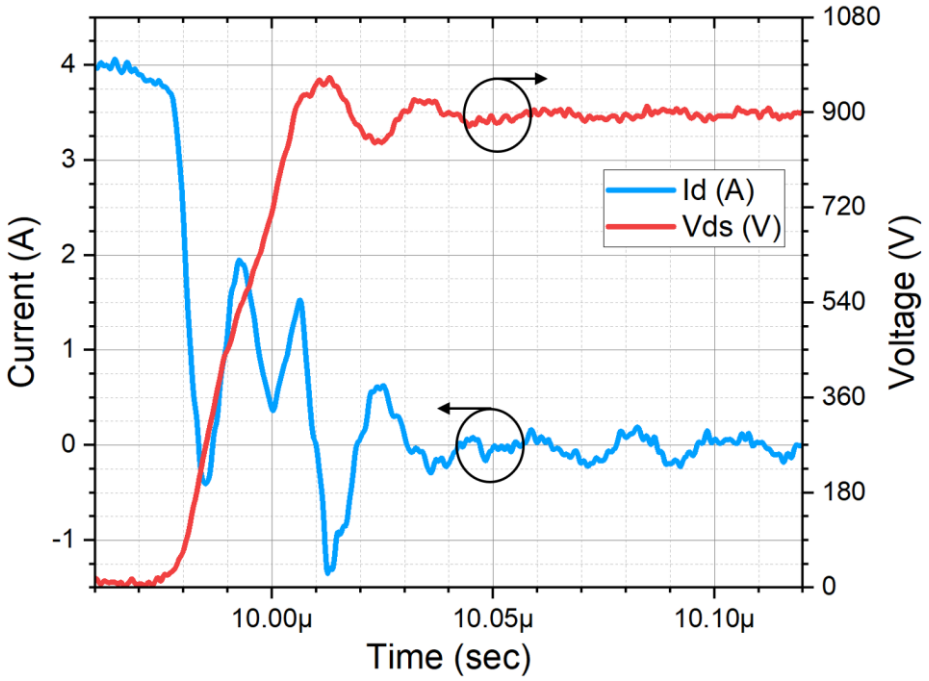

*Figure 3-34: Cascode GaN PSJ-FET DPT circuit schematic*

The DPT of cascode GaN was carried out under dc-link voltage of 900 V at room temperature and the resultant turn-on and turn-off waveforms at $I_{load}$ = 4 A are shown in Figure 3-35(a) and (b), respectively. The turn-on and turn-off waveforms were also compared against their standalone D-mode counterparts as

shown in Figure 3-36 and Figure 3-37, respectively. According to these figures, the rate of change of $V_{ds}$ and $I_d$ for cascode GaN were much larger than its D-mode counterpart but with much larger oscillations present in its turn-on and turn-off waveforms. Despite having $C_{oss,cascode} > C_{oss,GaN}$, much slower turn-off transition was observed in D-mode GaN compared to its cascode counterpart, which is primarily due to additional $C_{j,FWD}$, $C_{j,APD}$ and $C_{snub}$ that were placed in parallel to the D-mode DUT as presented in Figure 3-15. For instance, at $I_{load}$ = 4 A, the total turn-on and turn-off transition time of E-mode cascode GaN decreased by 56.7% and 65.7% from its D-mode counterpart, respectively. However, if the Schottky diodes with smaller junction capacitances and smaller $C_{snub}$ are used for D-mode GaN switching characterisation, then its turn-off transition time will become shorter as according to the equation (3-7).

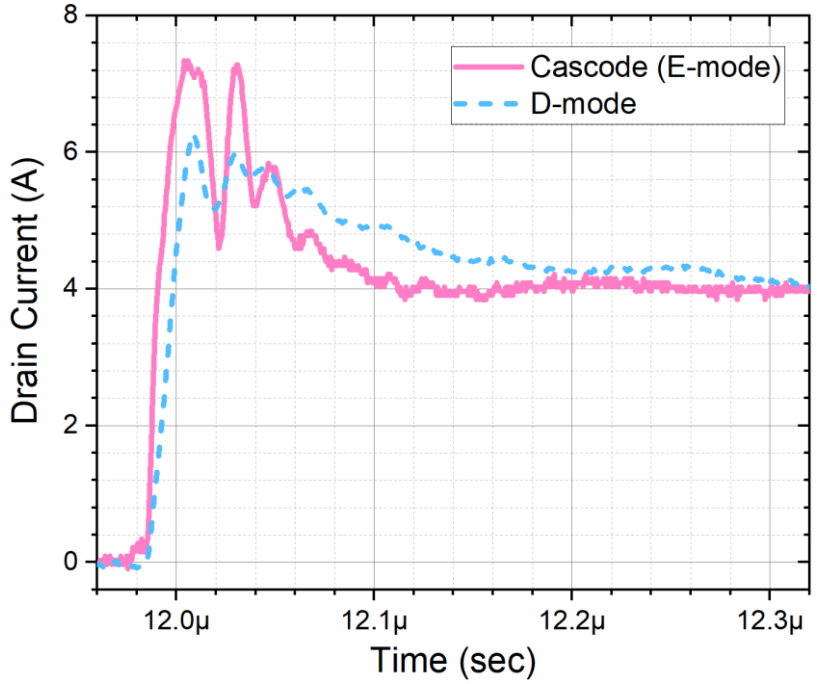



(a)

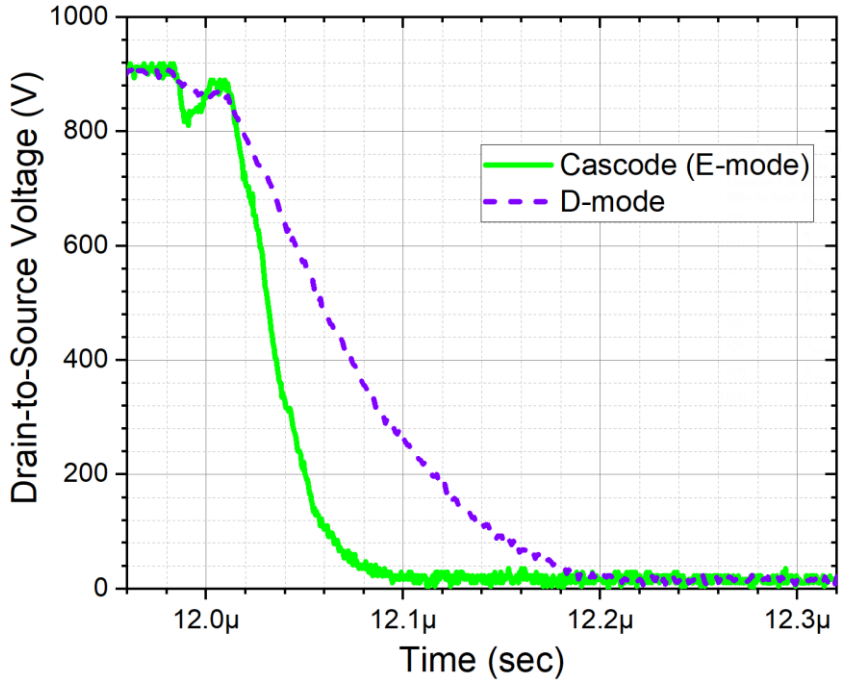



(b)

*Figure 3-35: (a) Turn-on and (b) turn-off voltage and current waveforms for cascode PSJ-FET under 900V dc-link at room temperature*

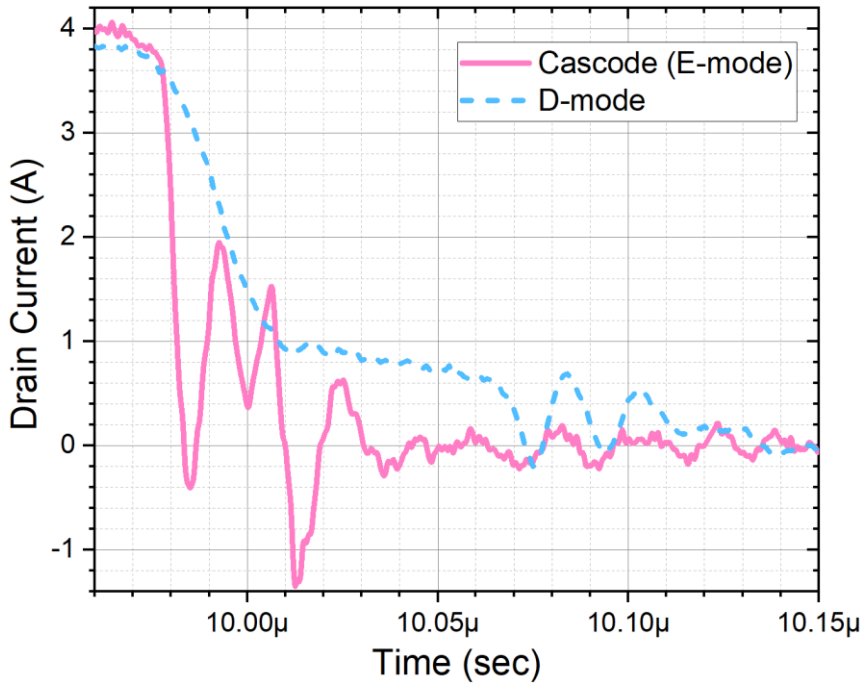



(a)

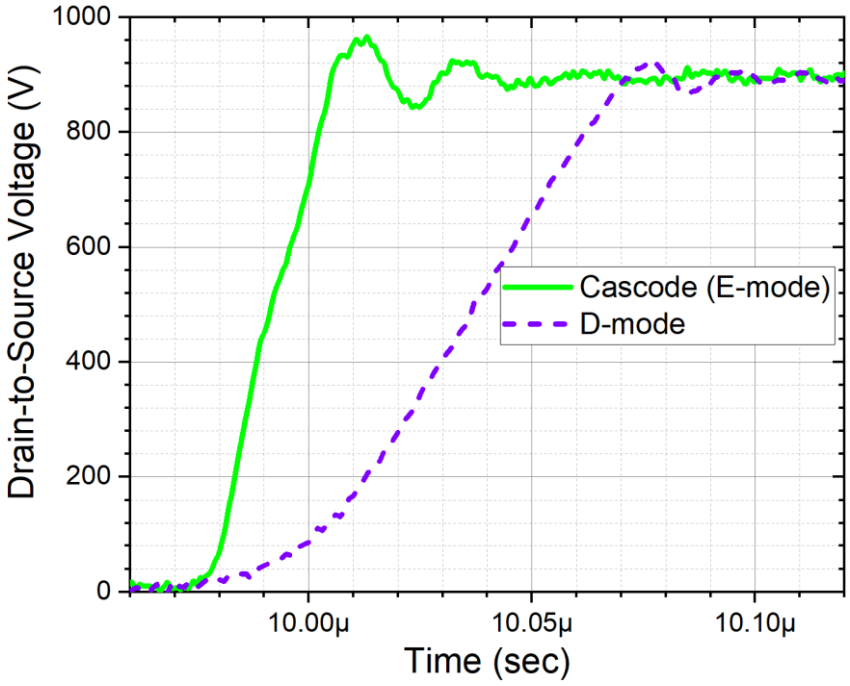



(b)

*Figure 3-36: Comparison of (a) $V_{ds}$ and (b) $I_d$ waveforms during turn-on transient of E-mode cascode GaN PSJ-FET under 900V dc link and 4 A load current*



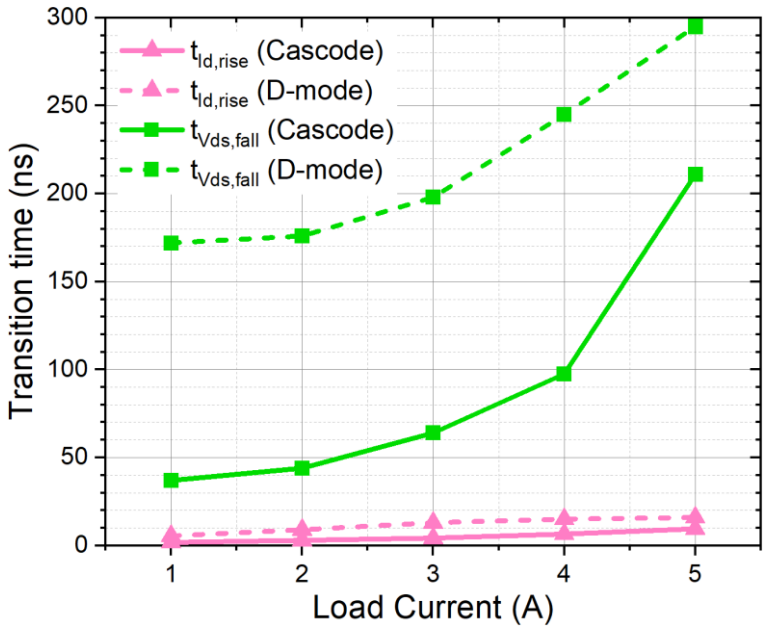

(a)



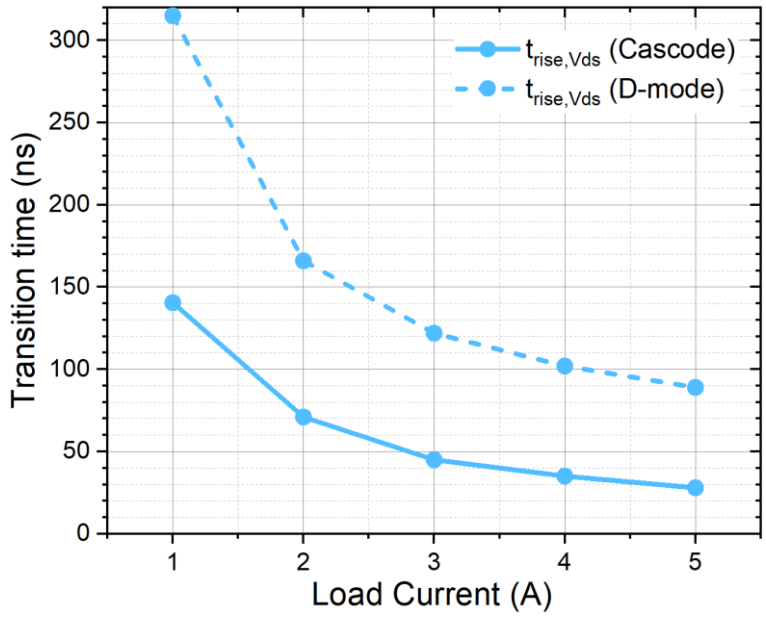

(b)

*Figure 3-37: Comparison of (a) $V_{ds}$ and (b) $I_d$ waveforms during turn-on transient of E-mode cascode GaN PSJ-FET at $I_{load}$ = 4 A*

The turn-on and turn-off transition times of cascode GaN were extracted and compared against the D-mode counterpart as presented in Figure 3-38(a) and (b), respectively. The resultant switching energy losses of the cascode GaN and standalone D-mode GaN vs. load current curves were plotted in Figure 3-39. The effective on-state $V_{gs}$ bias of the D-mode GaN transistor decreased from +2.5 V (for D-mode DPT) to < 0 V (for cascode GaN DPT) as its gate terminal was shorted to the source node of cascaded Si-MOSFET; this led to an increase in the $R_{ds,on}$ by at least 35% and reduction in saturated $I_d$ output. As a result, for constant $g_m$, $V_{th}$ and thus $V_{gs,mil}$ at room temperature, the $t_{Vds,fall}$ $V_{ds}$ fall transition time during turn-on increased at a much sharper rate compared to D-mode GaN with the rise in $I_{load}$ as shown in Figure 3-38. As $I_{load}$ increased from 4 A to 5 A, the $t_{Vds,fall}$ increased by 116.41% and 20.41% for cascode GaN and standalone D-mode GaN, respectively.




(a)




(b)

*Figure 3-38: (a) $V_{ds}$ fall and $I_d$ rise times ($t_{Vds,fall}$ and $t_{Id,rise}$) during turn-on event (b) $V_{ds}$ rise and fall transition times ($t_{Vds,rise}$) vs. load current for cascode GaN PSJ device and standalone D-mode GaN PSJ device at room temperature and 900 V dc-link*

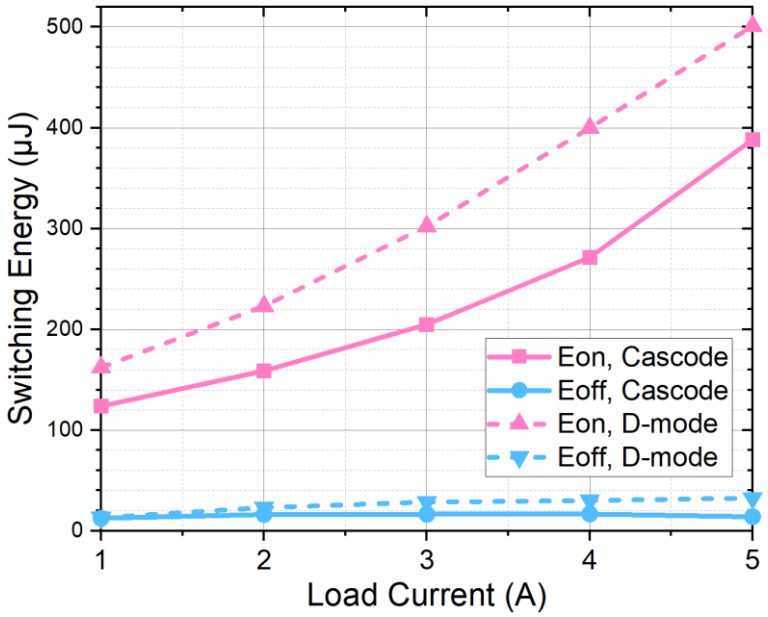



*Figure 3-39: Turn-on and turn-off switching energy losses vs, load current for the standalone D-mode and cascode E-mode GaN PSJ-FET*

## *3.3. Summary*

In this chapter, the static and dynamic (typical) performances of POWDEC's large-area D-mode PSJ transistor and E-mode cascode PSJ device under various conditions were evaluated, discussed in detail and compared against each other.

The chapter commenced with the change in static I-V characteristics of the D-mode device with $T_j$. It was clearly seen that its $g_m$ decreased and thus $R_{ds,on}$ has increased by a factor larger than 2 when the temperature increased from $25^0$C to $150^0$C. However, its $V_{gs,th}$ stayed constant with an increase in $T_j$.

Then, the terminal capacitances of the PSJ-FET with respect to $V_{ds}$ and $V_{gs}$ were extracted using the B1505A device analyser and Hioki LM3533-01 LCR meter. Both $C_{gs}$ and $C_{gd}$ increased exponentially as $V_{gs}$ exceeds $V_{gs,th}$ and thus the device is turned on. This is due to the 2DEG and 2DHG carrier buildup throughout the PSJ channel region, which forms a parallel plate capacitor where thin i-AlGaN layer behaves as a dielectric material between the two carriers.

Subsequently, the turn-on and turn-off switching characteristics of the PSJ device under various $T_j$ and gate drive resistor values were evaluated using a DPT circuit. Due to an exponential increase in $C_{gd}$ with a decrease in $V_{ds}$ when the PSJ device is 'on', the turn-on dV/dt became considerably slow. On the other hand, its turn-off dV/dt was much larger than its turn-on counterpart since the $C_{gd}$ became considerably low as the device entered its off state. Also, it remained relatively constant with an increase in $R_{g,ext(off)}$ and $T_j$ as the $V_{ds}$ rise time determined via capacitance present in the switching node as majority of $I_{load}$ was diverted away from DUT for charging the APD and FWD junction capacitances.

Lastly, the static and dynamic performances of E-mode cascode PSJ device packaged in DCB substrate with bonded wires were evaluated and then compared against its D-mode counterpart. From the comparison, it was shown that the cascode PSJ devices can switch much faster than their standalone D-mode counterpart, which leads to significantly reduced turn-on and turn-off energy losses. On the other hand, as the gate of the cascode PSJ is tied to the source, the maximum $V_{gs}$ present in the GaN device is reduced and thus its $R_{ds,on}$ is increased by 35% of D-mode PSJ transistors.

# 4 Fail-Safe Operation of D-mode GaN Power Devices

## *4.1. Safety concerns with D-mode devices in power converters*

As discussed in chapters 2 and 3, lateral GaN transistors inherently operate under depletion-mode (D-mode), implying that they cannot be turned off unless negative bias voltage is applied to their gate. Therefore, in the event of gate drive supply loss i.e. voltage supply decreasing to 0 V due to failures or instabilities in the external power supplies, they will be always in 'on' state. This will result in both power devices in a half-bridge converter being turned on and thus significant amount of shoot-through current occurs due to short-circuit through the DC-link as illustrated in Figure 4-1. Unless external means of isolating the converter from the input dc supply to prevent the shoot-through is provided, the devices will be overheated and ultimately damaged. Thus, critical safety issues arise when using D-mode power devices and must be addressed before implementing them.

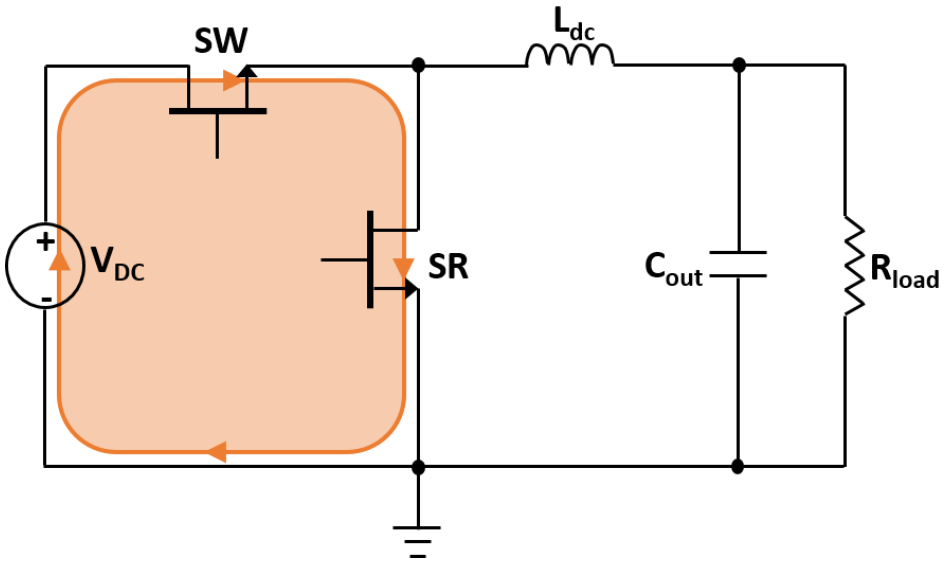



*Figure 4-1: Shoot-through current in a half-bridge dc-to-dc converter due to gate drive supply failure for D-mode power devices*

## *4.2. Literature reviews*

### *4.2.1. Inherently safe power converter with D-mode power devices*

The means of detecting gate drive supply failure and preventing subsequent short-circuit event is required for D-mode devices to operate under voltage-sourced converters without being damaged. Many efforts have been devoted in order to achieve this in many ways at the cost of increased circuit complexity and cost of implementation. In [120], the secondary winding, which is connected to the gate of the switching device, was added to the choke inductor and an autotransformer to the controller output for generating positive and negative gate voltages for turning the device on and off; this is presented in Figure 4-2. The main drawback of this method is that it relies on the converter's output voltage ($V_{out}$) for generating gate drive voltage and thus only works for extremely low $V_{out}$ (+12V output in [120]). In [121] and [122], alternative protection schemes for D-mode SiC-JFETs were proposed where high-voltage dc-link voltage is utilised for generating negative gate voltages and thus activate the gate drive circuitries; this is illustrated in Figure 4-3. Despite their simplicity, their response time were determined as 45µs and 130µs in [122] and [121], respectively. This may lead to excessive shoot-through current and significant energy dissipation and ultimately thermal failure of the devices during the initial start-up.

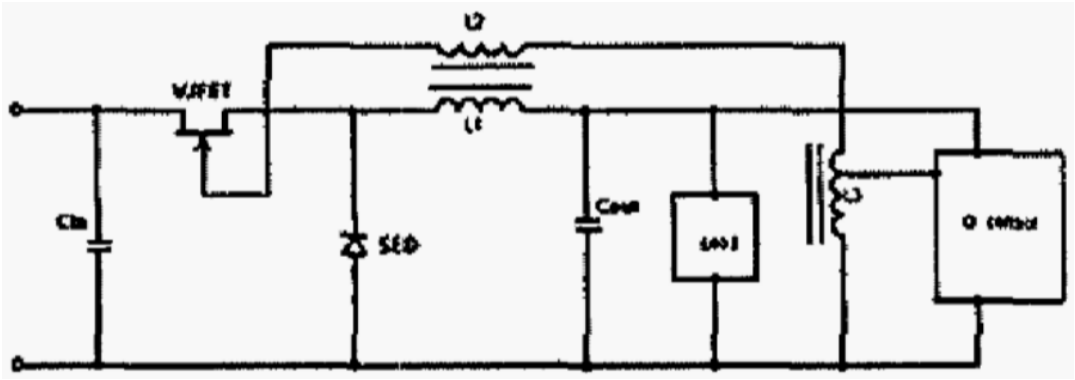


*Figure 4-2: Inherently safe step-down dc-to-dc converter made with D-mode Semisouth SiC HEL²FET™ and SiC-SBD [120]*

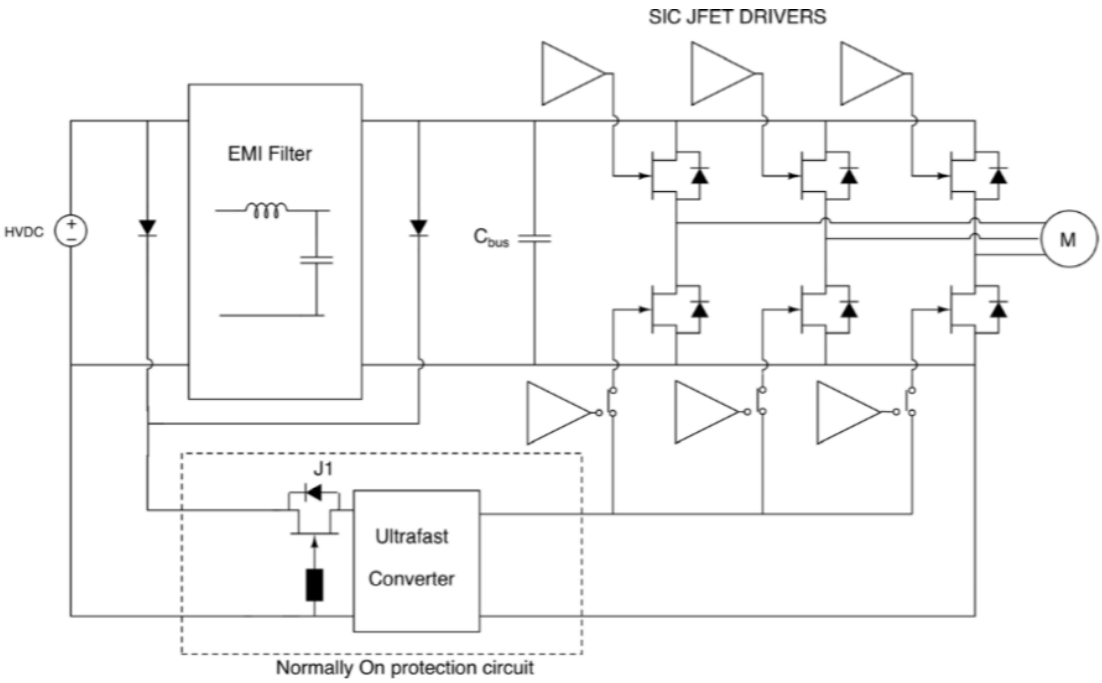



*Figure 4-3: Three-phase inverter with D-mode SiC-JFETs and an ultrafast converter generating negative gate drive voltage from the DC-bus [122]*

An alternative scheme has been proposed and demonstrated in [123] where the negative gate drive voltage is supplied via forward converter parallel to the switching devices consisting of transformer and a diode and output capacitor at the secondary side when a shoot-through current is present at the half-bridge converter during start-up phase as illustrated in Figure 4-4. The initial shoot-through current is limited by placing a resistor in parallel to a relay switch that is turned on once

gate drive supply is fully powered on. However, there exists a trade-off between allowing large initial shoot-through current for sufficient negative voltage to be generated to turn OFF the D-mode devices at the start-up and limiting the shoot-through current to prevent thermal failure of the devices. In addition, the response time of the circuit designed with the parameters in [123] at the initial start-up was determined as 20µs, which is excessively long and thus the power devices excluding SiC-JFETs are likely to fail before the converter enters its normal operating state.

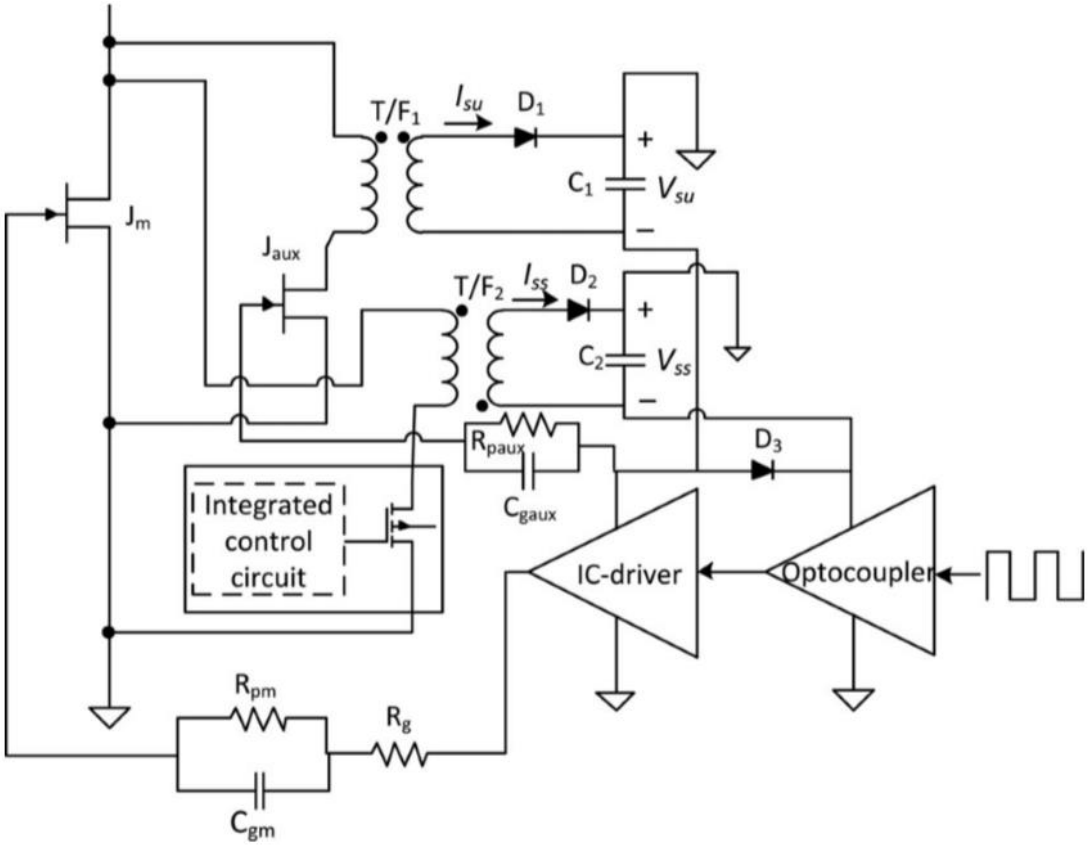



*Figure 4-4: Self-powered gate drive scheme for D-mode SiC-JFETs [123]*

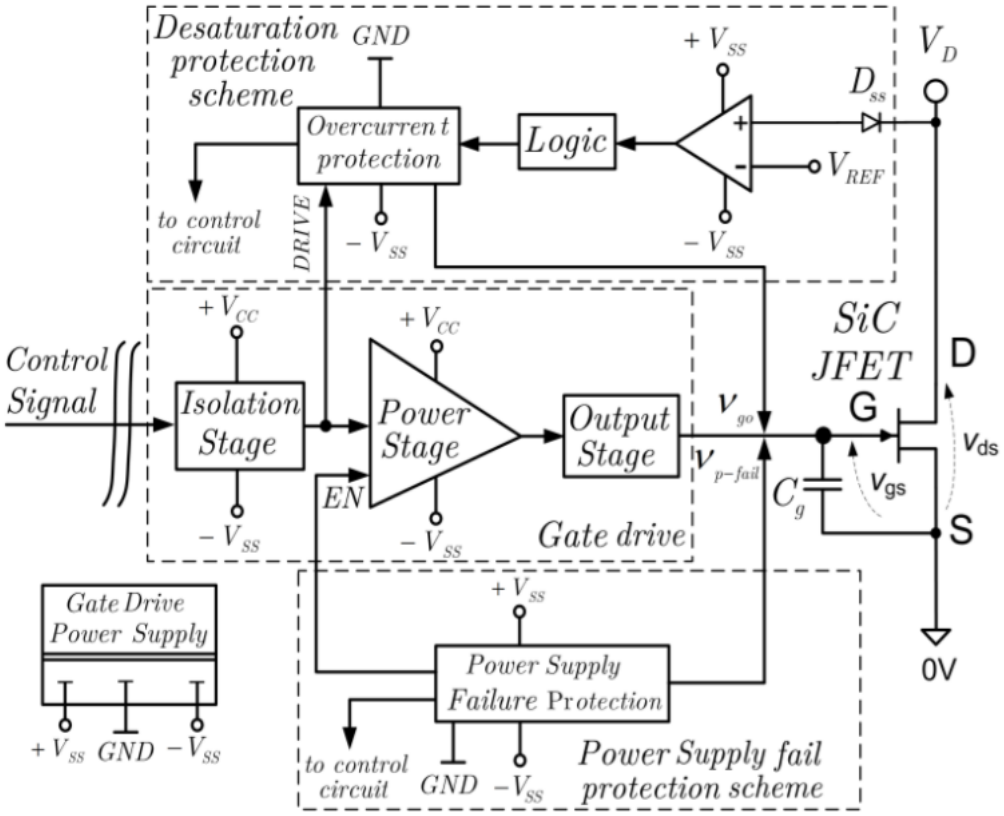
### *4.2.2. Gate driver supply failure protection (GDSFP) scheme*

The circuits proposed so far have been utilizing shoot-through current at the initial start-up in order to activate the gate driver circuit for D-mode power devices. This may cause permanent damage to the devices as the circuit response is not fast

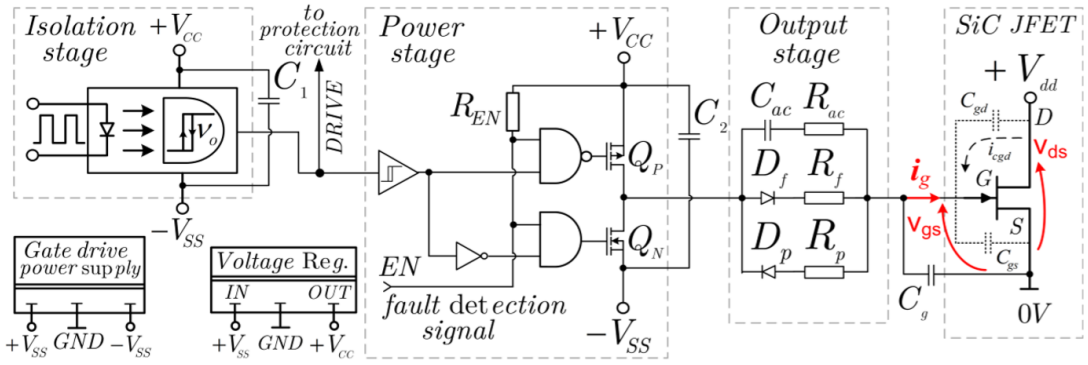
enough and thus rendering it unreliable. Therefore, a new self-protection circuit for D-mode SiC-JFETs was proposed in [124] to inherently prevent shoot-through current and thus device failure from occurring during the startup, normal operation and gate driver power supply failure event. The block diagram of this fail-safe topology is clearly illustrated in Figure 4-5(a). The only failure scenario that is taken into consideration in protections schemes proposed in [124] and this work is the loss of gate drive supply i.e. supply voltage decreasing to 0 V either instantaneously or gradually over time. Other means of device protection mechanisms such as over-voltage protection and under-voltage lock-out (UVLO) protection were not considered in both [124] and this work.

The fail-safe protection topology consists of desaturation-based protection scheme for preventing device failures due to overload or shoot-through current during normal operation and GDSFP scheme for protecting the power devices (SiC-JFETs in this case) in a half-bridge converter when the gate driver supply fails. Schematic of the gate driver circuit for D-mode SiC-JFETs is presented in Figure 4-5(b). The EN input at its power stage is driven by the output of GDSFP so that the gate driver is disabled when the power supply failure is detected by GDSFP scheme. The DRIVE signal at the isolation stage output is also sent to the desaturation-based protection scheme during normal operation.

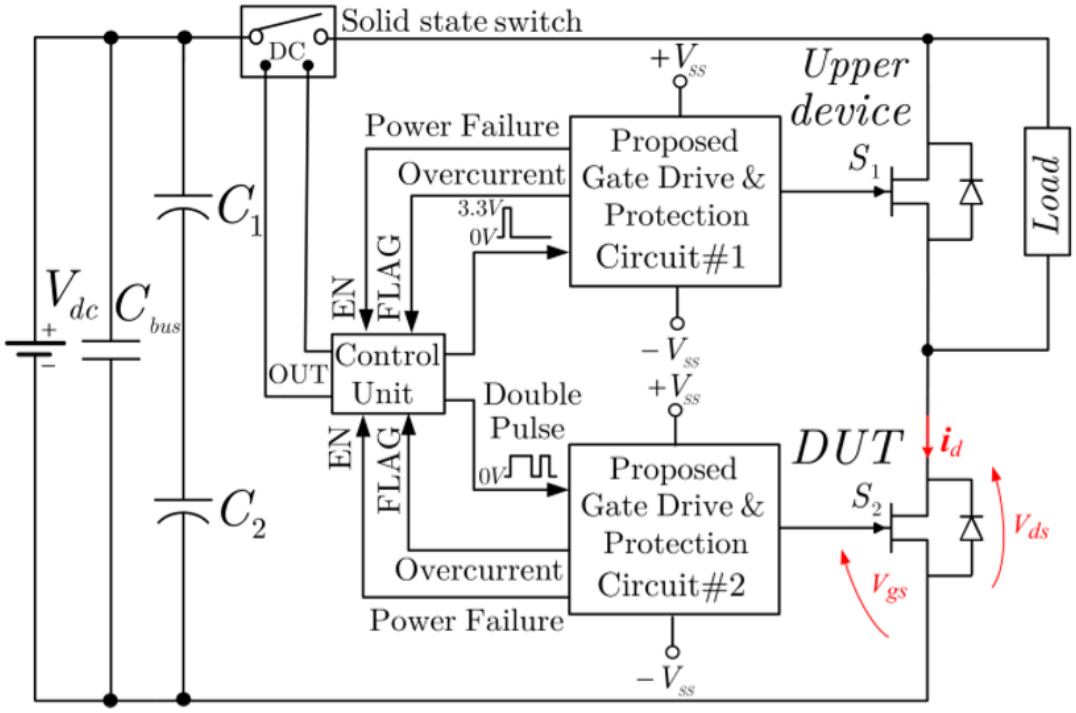
A detailed schematic of the test setup and GDSFP circuit that were proposed in [124] are presented in Figure 4-5(c) and (d), respectively. This protection scheme ensures that the D-mode power devices are kept in their ‘off’ state for sufficient periods of time, and hence the converter could be isolated from the DC-link without experiencing shoot-through currents. Its operating principle is described in the following paragraphs.


Desaturation protection scheme
GND
+ V_SS
V_D
D_ss
Overcurrent protection
Logic
V_REF
to control circuit
DRIVE
- V_SS
- V_SS
+ V_CC
+ V_CC
SiC JFET
D
Control Signal
Isolation Stage
Power Stage
Output Stage
v_go
G
V_ds
v_p-fail
C_g
V_gs
EN
- V_SS
- V_SS
Gate drive
S
+ V_SS
Gate Drive Power Supply
Power Supply Failure Protection
0V
+ V_SS GND - V_SS
to control circuit
GND - V_SS
Power Supply fail protection scheme

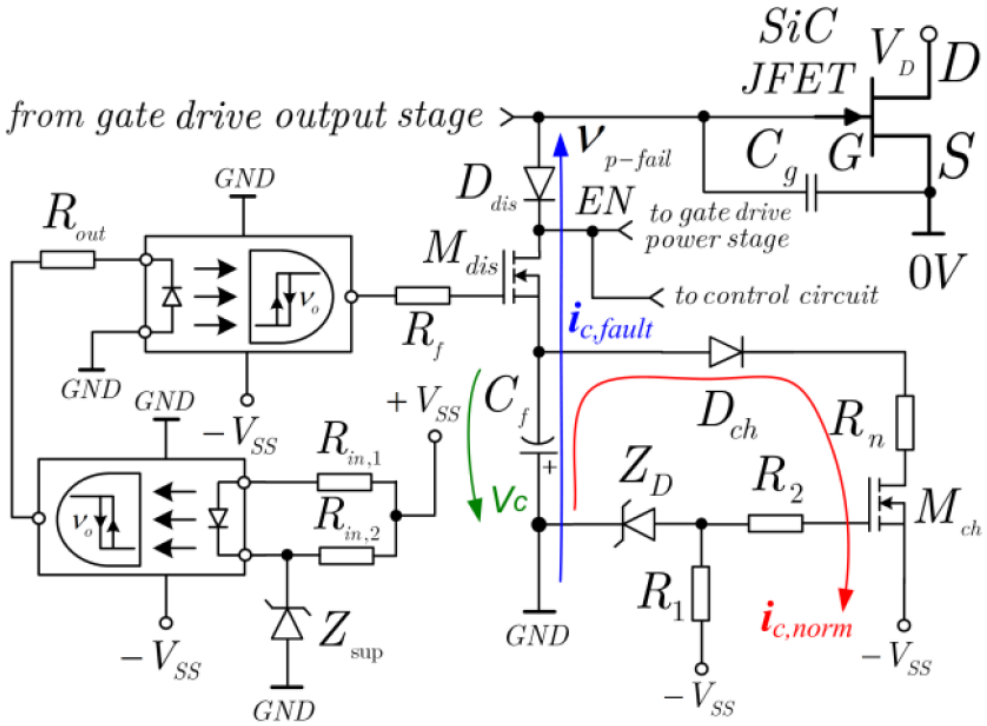
(a)


Isolation stage
+V_CC
to protection circuit
C_1
DRIVE
Power stage
+V_CC
Output stage
SiC JFET
+ V_dd
R_EN
C_2
C_ac R_ac
C_gd
D
Q_P
D_f R_f
i_g
V_ds
G
i_cgd
V_gs
S
Q_N
D_p R_p
C_gs
-V_SS
Gate drive power supply
Voltage Reg.
IN OUT
EN
fault detection signal
-V_SS
C_g
0V
+V_SS GND -V_SS
+V_ss GND +V_cc

(b)




(c)




(d)

*Figure 4-5: (a) Layout of the fail-safe gate drive scheme, (b) Detailed schematic of the gate drive circuit, (c) Experimental tester set-up circuit schematic and (d) GDSFP scheme proposed for D-mode SiC-JFETs [124]*

Initially, the capacitor $C_f$ is not charged and gate driver supply voltage, $-V_{SS}$, is deactivated. When $-V_{SS}$ is activated and thus startup process is initiated, the $V_{gs}$ of the N-channel MOSFET $M_{ch}$ is regulated by Zener diode $Z_D$ so that $M_{ch}$ is turned on and thus $C_f$ is charged exponentially towards $-V_{SS}$ via diode $D_{ch}$ and $M_{ch}$ with the following time constant:

$$\tau_{Cres,ch} = (R_{Dch} + R_n + R_{Mch}) \cdot C_f \quad \dots (4\text{-}1)$$

Under normal operating conditions, the input to the first optocoupler is regulated via Zener diode $Z_{sup}$ so that its output becomes logic low ($-V_{SS}$) and MOSFET $M_{dis}$ is turned off. Should the power supply $+V_{SS}$ fail, its failure will be detected by $Z_{sup}$ so that the optocoupler output becomes logic HIGH and thus switching device will be turned off via $M_{dis}$ and $D_{dis}$ in the GDSFP circuit as its gate voltage will be discharged towards $-V_C$ across the capacitor $C_f$ with the following time constant:

$$\tau_{Cf,disc} = R_{Mdis} \cdot C_f \quad \dots (4\text{-}2)$$

This gives a total time frame during which the device is kept in an 'off' state before turning on and the $S_{dc,link}$ must be turned off, expressed as:

$$t_{frame,gsf} = \tau_{Cf,disc} \cdot ln\left(\frac{-V_{SS}+V_{f,Ddis}}{V_{gs,th}}\right) \quad \dots (4\text{-}3)$$

Where $V_{gs,th}$ = turn-on threshold voltage of the power device and $V_{f,Ddis}$ = forward voltage drop of the diode $D_{dis}$. The EN signal output becomes clamped to $-V_C$, which will be sent to the enable input of the gate driver IC so that the PWM control signal is blocked and thus gate driver output is fixed to logic low. The EN signal is also sent to the converter control unit from which control signal is sent to the power

stage of the gate driver. Therefore, the command signal to turn off the solid-state dc-link switch is sent to its input drive stage and thus converter becomes isolated from the high-voltage dc-link. Thereby, the power converters made with D-mode SiC-JFETs or any other power devices can be operated in fail-safe modes.

## *4.3. Simulation of the previously proposed GDSFP scheme*

In order to verify its functionality, a step-down DC-to-DC converter with GDSFP circuit previously proposed in [124] was implemented in a TINA-TI PSpice simulation software. The schematic of the simulated circuit is shown in Figure 4-6. In order to emulate the D-mode device behavior, a 500 V, 17 A rated D-mode N-channel MOSFET (IXTT20N50D) was used. A 650 V, 16 A rated SiC Schottky barrier diode (UJ3D06516TS) was used as a freewheeling diode (FWD) in the converter circuit. The components of the proposed GDSFP circuit and electrical parameters of the step-down converter and GDSFP circuit used for the simulation are clearly presented in Table 4-1(a) and (b), respectively. The ideal time-controlled switches are used in the totem-pole output stage of the gate drive circuit. The dc-link switch ($S_{dc,link}$) is assumed to an ideal time-controlled switch and the EN output signal is sent directly to the control side of $S_{dc,link}$. Thus, the turn-off time delay time of $S_{dc,link}$ and propagation delay of a gate drive controller IC is not considered.

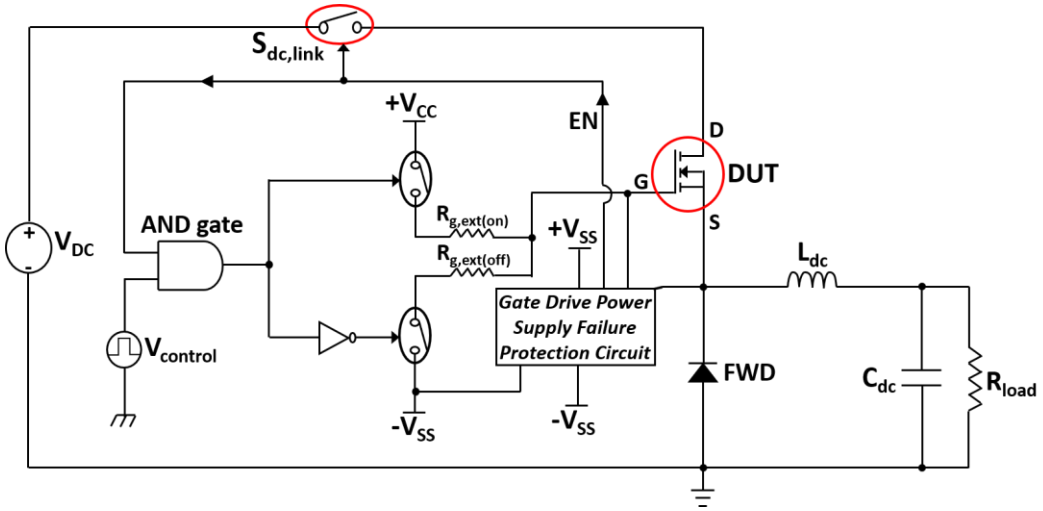



*Figure 4-6: Schematic of a step-down DC-to-DC converter with a D-mode power device and gate drive power supply failure protection scheme proposed in [124] under simulation*

| Components | Part Number |
|---|---|
| AND gate | SN74LV08A |
| $D_{ch}$ and $D_{dis}$ | UF4002 |
| $M_{ch}$ and $M_{dis}$ | IPD220N06L3 |
| Optocouplers | HCPL-2231L |
| $Z_D$ and $Z_{sup}$ | 1N4740 |

(a)

| Parameters | Values |
|---|---|
| $C_{dc}$ | 1 µF |
| $C_f$ | 560 µF |
| $L_{dc}$ | 1.5 mH |
| $R_1$ and $R_2$ | 1 kΩ and 8 Ω |
| $R_f$ | 5 Ω |
| $R_{g,ext(on)}$ and $R_{g,ext(off)}$ | 5 Ω |
| $R_{in,1}$ and $R_{in,2}$ | 1 kΩ and 200 Ω |
| $R_{load}$ | 30 Ω |
| $R_n$ | 0 Ω |
| $R_{out}$ | 1 kΩ |
| $+V_{CC}$ | + 10 V |
| $V_{DC}$ | 300 V |

| | |
|---|---|
| +/- $V_{SS}$ | +/- 15 V |

(b)

*Table 4-1: (a) GDSFP circuit components and (b) GDSFP and the converter's electrical parameters used for simulation*

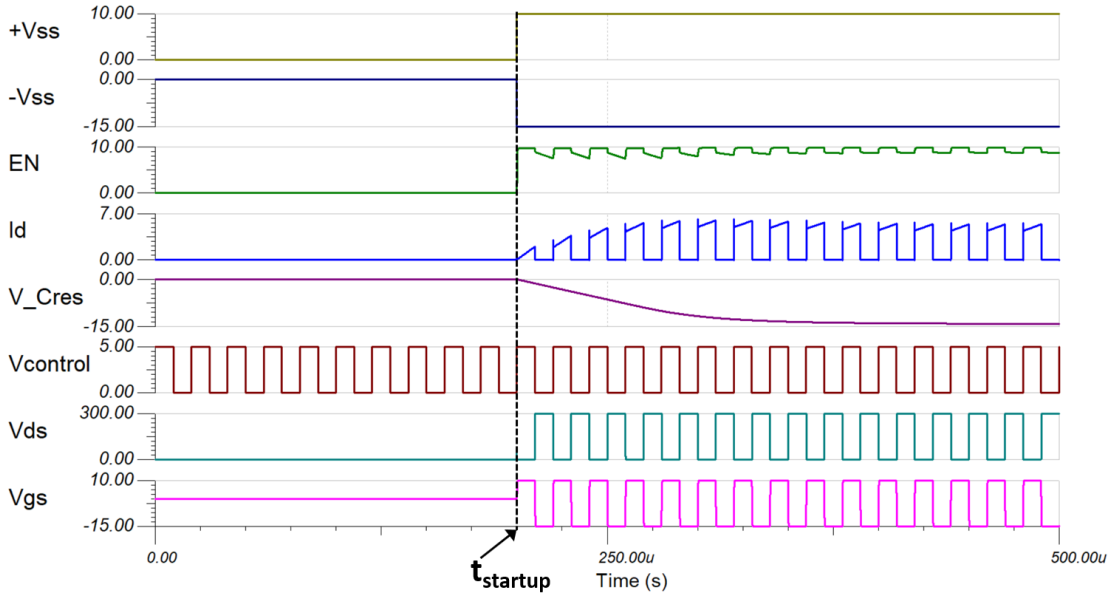
The simulation waveforms during the initial startup, normal operation and gate drive supply failure event are shown in Figure 4-7(a), (b) and (c), respectively. From the point where the startup occurs, the voltage across the capacitor $C_f$ (labelled as V_$C_{res}$ in Figure 4-7) is charged towards -$V_{SS}$. At the rising edge of the first control signal pulse, the EN node is immediately pulled up towards +$V_{CC}$ as $D_{dis}$ is forward biased. Hence the converter now enters its normal operation state as shown in Figure 4-7(b). At the point of time t=2ms, the +$V_{CC}$, +$V_{SS}$ and -$V_{SS}$ supplies are removed and therefore the output of the second optocoupler ultimately becomes logic high (GND) after a certain propagation delay imposed by two optocouplers in series. According to the simulation, this propagation delay was determined as 550ns, during which the DUT is in its 'on' state due to the power supply failure. Although this delay time is not significant to cause device failure due to shoot-through current in a half-bridge circuit, it is still desirable to keep it shorter than the turn-on delay time of the device, which can be expressed as:

$$\tau_{on,delay} = \left(R_{g,ext(off)} + R_{g,int}\right) \cdot C_{iss,dut} \quad \ldots(4\text{-}4)$$

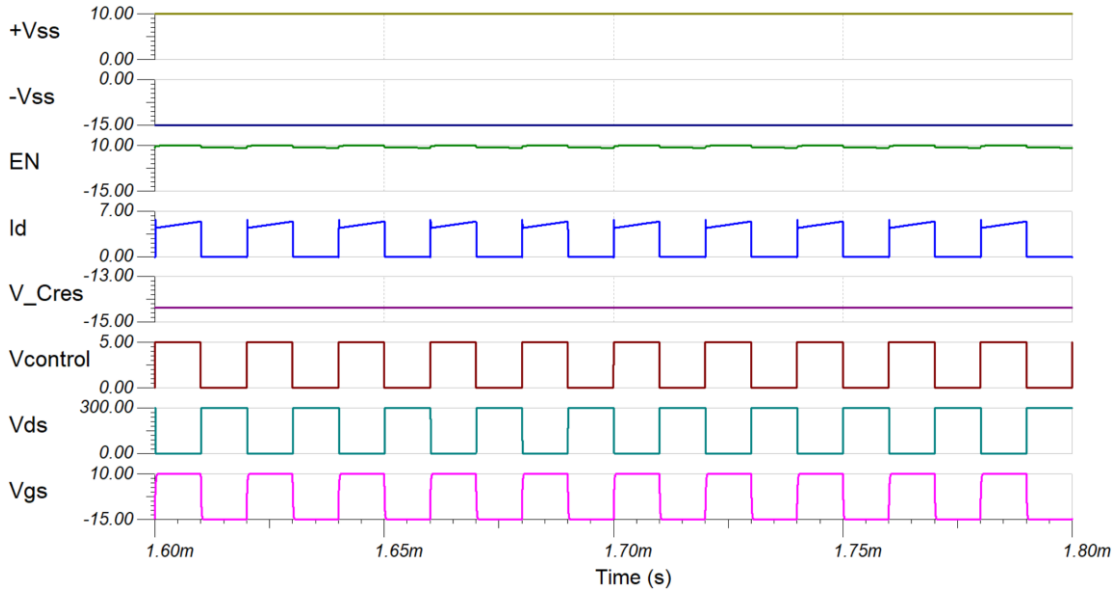
Where $R_{g,int}$ = internal gate resistance and $C_{iss,dut}$ = input capacitance of the DUT. The propagation delay will thus become a major criterion to the selection of optocouplers so that the signals can propagate through them with minimum time delay and thereby the probability of device failure is minimised. Then, $M_{dis}$ is turned on and the gate of the DUT is pulled towards -$V_C$ so that it is maintained to be in its

off-state for some time frame given. Meanwhile, as $M_{dis}$ in Figure is in its 'on' state, the EN node is clamped to $-V_C$ and thus sends a logic low signal to the input of the AND gate so that gate driver circuit is disabled. This signal is also sent to the $S_{dc,link}$ drive stage so that it is turned off. Therefore, the D-mode power device can operate in a fail-safe manner without critical safety issues.

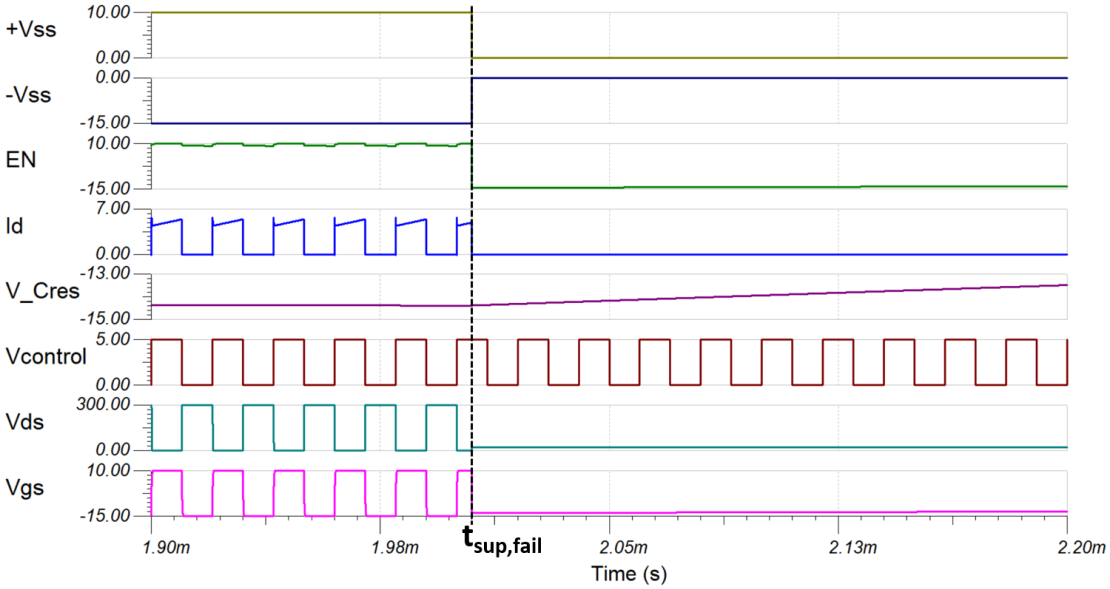
Nevertheless, the GDSFP topology causes an error when the power supplies are recovered as shown in the simulation waveforms in Figure 4-7(d). In the simulation, the power supply recovery event was set to occur at 500μs after its failure. As discussed previously, $V_C$ and thus the voltage at the EN node will be discharged exponentially with the time constant expressed in equation (4-2). If the supply recovery event occurs at a point where the EN voltage has still not reached the logic high level, the gate drive circuit will remain deactivated and thus the converter will not be able to enter its normal operation mode for an indefinite period of time even after the power supplies are recovered. The only way to restore the normal operation of the converter is to manually remove the gate drive power supplies and activate the supplies again when $V_C$ and EN have reached 0V. However, the gate driver IC must be capable of accepting 0V (or GND in Figure) as a logic high EN input for a set values for $+V_{CC}$ and $-V_{SS}$; otherwise, the gate driver will never be enabled. Hence, this topology also faces limitations in terms of acceptable range of recovery time and gate driver IC selection to avoid erroneous operation.


+Vss
10.00
0.00
-Vss
0.00
-15.00
EN
10.00
0.00
Id
7.00
0.00
V_Cres
0.00
-15.00
Vcontrol
5.00
0.00
Vds
300.00
0.00
Vgs
10.00
-15.00
0.00
250.00u
500.00u
Time (s)
t startup

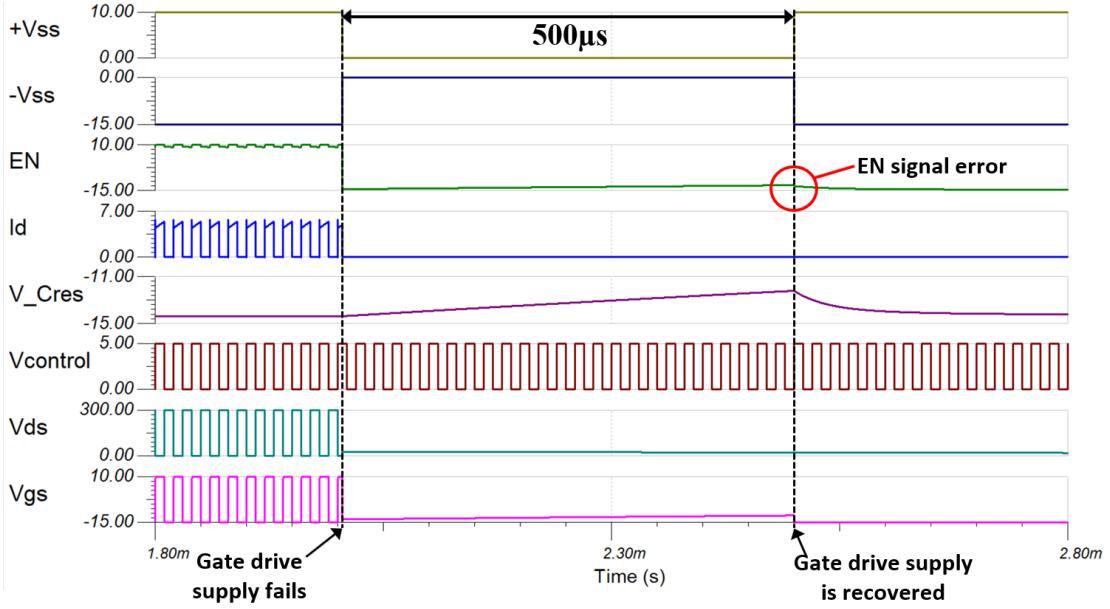
(a)


+Vss
10.00
0.00
-Vss
0.00
-15.00
EN
10.00
-15.00
Id
7.00
0.00
V_Cres
-13.00
-15.00
Vcontrol
5.00
0.00
Vds
300.00
0.00
Vgs
10.00
-15.00
1.60m
1.65m
1.70m
1.75m
1.80m
Time (s)

(b)




(c)




(d)

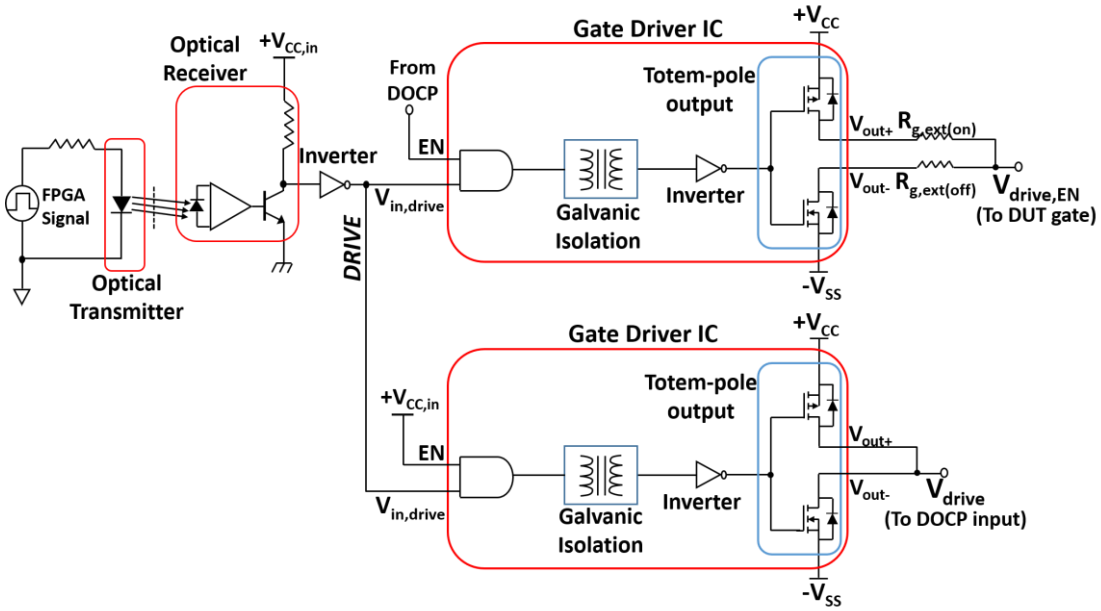
*Figure 4-7: Simulation waveforms of step-down DC-to-DC converter with previous GDSFP topology proposed in [124] during (a) start-up, (b) normal operation, (c) gate driver power supply failure event and (d) gate driver power supply recovery event*

## *4.4. Modified protection topology used in this work*

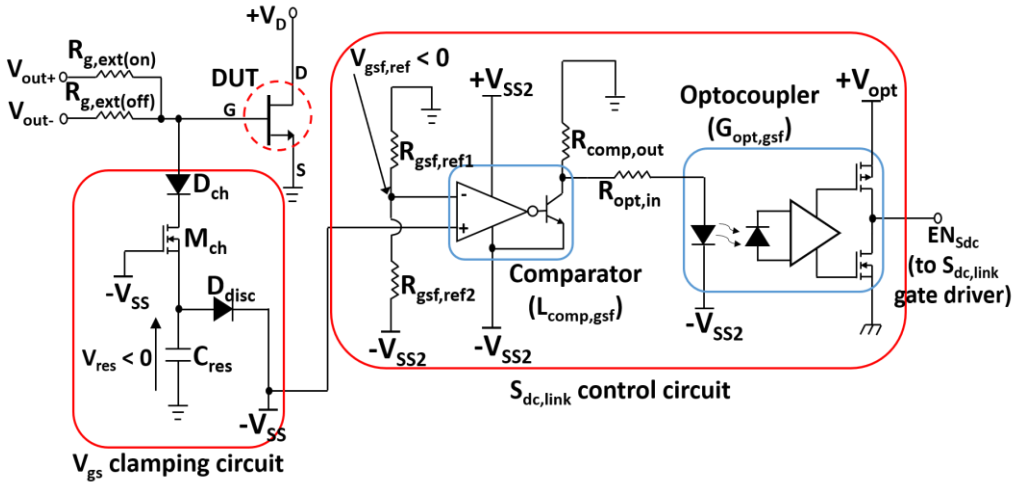
A modified gate drive circuit, a refined GDSFP topology and its half-bridge test circuit for D-mode GaN devices used and tested for this work are presented in Figure 4-8(a), (b) and (c), respectively. The gate driver ICs used for this work have

galvanic isolation between input and output internally and thus no additional components for isolation are required. For this work, the GDSFP topology was improved compared to its previous counterpart in several ways. First of all, the that number of component counts are reduced and thereby cost of implementation and circuit board area occupied can be minimised. This was achieved by removing two series-connected optocouplers driving $M_{dis}$ gate, $Z_D$, $M_{ch}$, $R_1$, $R_2$ $R_{in,1}$, $R_{in,2}$, $R_n$ and $Z_{sup}$ in Figure 4-5(d) as the same circuit functionality can be achieved without them. Also, as the two optocouplers in Figure 4-5(d) are removed, the power devices can be turned off with minimum propagation delay when the $-V_{SS}$ supply fails.

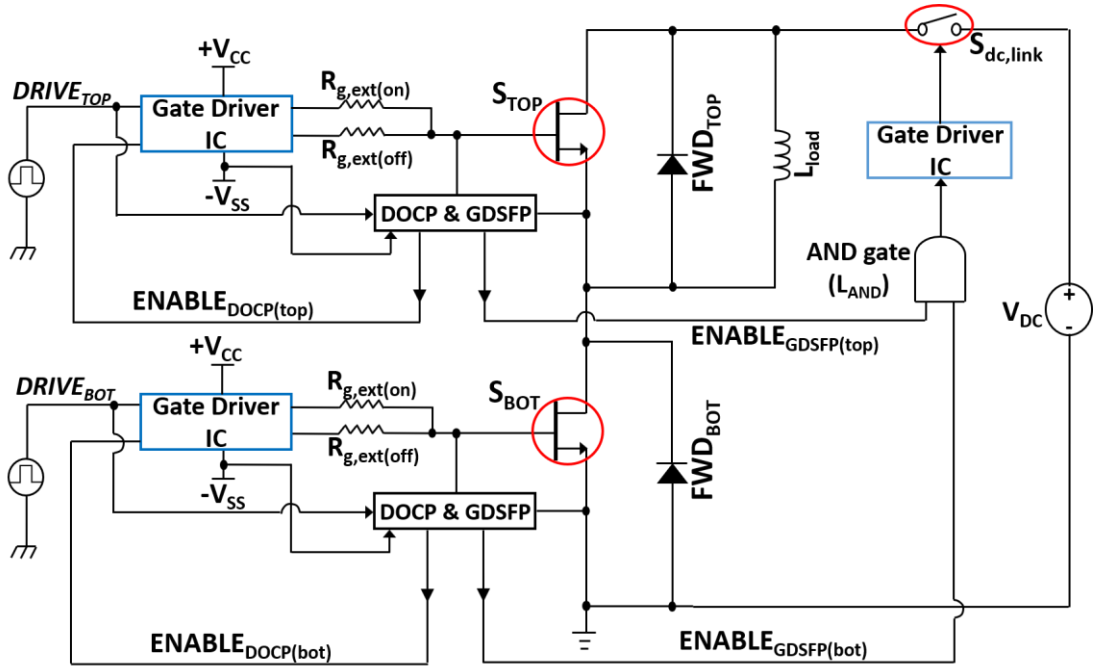
Furthermore, unlike EN output in the previous GDSFP scheme, an optocoupler is placed between the DUT gate clamping circuit and ENABLE output signal, which serves to provide galvanic isolation between them. For the previous solution in Figure 4-5, due to the floating ground reference of the gate drive circuit for high-side switching devices in half-bridge converters, galvanic isolation is required between the EN output and the controller IC or input side of gate drive circuit; this is not shown nor discussed in [124]. In addition, the aforementioned false EN signal triggering in the previous GDSFP scheme under a power supply recovery event is resolved so that ENABLE output is driven by the value of $-V_{SS}$ only regardless of the initial value of $V_C$ (or $V_{res}$ in Figure 4-8(b)). This was verified using the SPICE circuit simulation and its results will be discussed in the following section in more detail.


Optical Receiver
+V_CC,in
From DOCP
Gate Driver IC
+V_CC
Totem-pole output
V_out+
R_g,ext(on)
V_out-
R_g,ext(off)
V_drive,EN
(To DUT gate)
FPGA Signal
Inverter
EN
V_in,drive
Galvanic Isolation
Inverter
-V_SS
Optical Transmitter
DRIVE
Gate Driver IC
+V_CC
+V_CC,in
Totem-pole output
V_out+
EN
V_out-
V_drive
(To DOCP input)
V_in,drive
Galvanic Isolation
Inverter
-V_SS

(a)


+V_D
R_g,ext(on)
V_out+
R_g,ext(off)
V_out-
DUT
D
G
S
D_ch
M_ch
-V_SS
D_disc
V_res < 0
C_res
-V_SS
V_gs clamping circuit
V_gsf,ref < 0
+V_SS2
R_gsf,ref1
R_comp,out
R_opt,in
Optocoupler (G_opt,gsf)
+V_opt
EN_Sdc
(to S_dc,link gate driver)
Comparator (L_comp,gsf)
R_gsf,ref2
-V_SS2
-V_SS2
-V_SS2
S_dc,link control circuit

(b)




(c)

*Figure 4-8: Schematic of the (a) proposed gate drive circuit, (b) refined GDSFP scheme and (c) fail-safe gate drive tester circuit with D-mode devices proposed for this work*

For this protection scheme, two power supplies are required; one for activating $-V_{SS}$ and the other one for activating $-V_{SS2}$ and $+V_{opt}$. The operating principle of the new GDSFP circuit in Figure 4-8 can be described as follows. When both power supplies are inactive, the ENABLE output signal that drives the dc-link switch ($S_{dc,link}$) as shown in Figure 4-9 becomes low and hence the $S_{dc,link}$ is maintained to be in OFF-state, thereby isolating the converter from the high-voltage dc-link. When the $-V_{SS}$ supply is activated, the reservoir capacitor, $C_{res}$, is discharged towards $-V_{SS}$ via discharging diode, $D_{disc}$. The time taken for $C_{res}$ to be fully charged is dependent upon the $C_{res}$ value and the effective resistance of $D_{disc}$. Since the gate supply failure reference value, $V_{gsf,ref}$, is set to be $V_{gsf,ref} > -V_{SS}$, the comparator output will then be LOW and thus the infrared LED on the input side of the optocoupler is turned off. Thereby, the ENABLE output becomes HIGH and

thus $S_{dc,link}$ is in its on state and converter can operate normally. Meanwhile, the E-mode charging MOSFET $M_{ch}$ is in off state as its $V_{gs}$ is below 0V.

Should the $-V_{SS}$ supply fail during the converter operation, the $M_{ch}$ is turned on and the gate voltage of DUT is pulled towards $C_{res}$ voltage, $V_{res}$, via charging diode $D_{ch}$ and $M_{ch}$. Therefore, both devices in a half-bridge converter will be turned off immediately. Also, $C_{res}$ will be charged towards 0V with an associated time constant:

$$\tau_{Cres,ch} = \left(R_{g,ext(off)} + R_{Mch,on}\right) \cdot C_{res} \quad \ldots(4\text{-}5)$$

Where $R_{g,ext(off)}$ = external turn-off gate resistor and $R_{Mch,on}$ = on-state resistance of $M_{ch}$. It is notable that $R_{Mch,on}$ changes over time as $V_{gs}$ of $M_{ch}$ changes due to $C_{res}$ charging. The $V_{gs}$ of DUT during this period and thus the total $t_{frame}$ determined by GDSFP components can be expressed as:

$$V_{gs}(t) = \left(V_{f,Dch} - V_{SS}\right) \cdot e^{-\frac{t}{\tau_{Cres,ch}}} \quad \ldots(4\text{-}6)$$

$$t_{frame} = \tau_{Cres,ch} \cdot ln\left(\frac{V_{f,Dch} - V_{SS}}{V_{gs,th}}\right) \quad \ldots(4\text{-}7)$$

Simultaneously, the $-V_{SS}$ supply will rise above the reference value $V_{gsf,ref}$ so that the comparator output becomes HIGH, the optocoupler LED is turned on and thus ENABLE output becomes LOW. Consequently, the $S_{dc,link}$ will be turned off and the converter is isolated from the dc-link voltage supply. By this principle, the D-mode power devices can be operated in a fail-safe manner.

### *4.4.1. GDSFP Simulation*

In order to verify the functionality of the proposed circuit, a step-down dc-to-dc converter with the GDSFP scheme as shown in Figure 4-9 was implemented in TINA-TI PSpice simulation software with the components and parameters enlisted in Table 4-2(a) and (b), respectively. The same 500V D-mode Si-MOSFET (IXTT20N50D) and 650V SiC Schottky barrier diode were used as the switching DUT and FWD, respectively; therefore, the $V_{dc}$ was limited to 300 V in the simulation. The device was driven by a PWM signal with a frequency of 50kHz and duty cycle of 50%. The comparator and optocoupler with minimum propagation delay were used for fast circuit response.

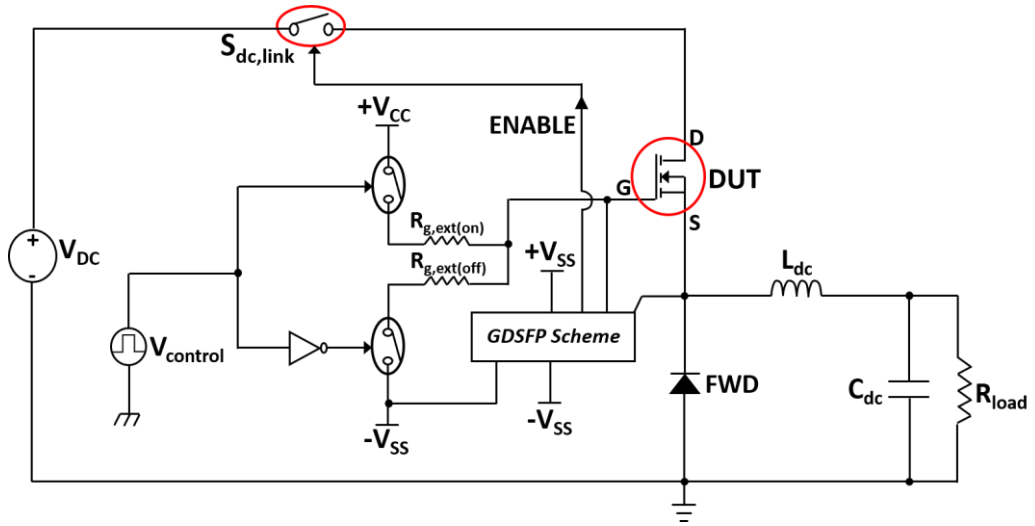



*Figure 4-9: Step-down DC-DC converter with GDSFP scheme driving a dc-link switch for fail-safe operation of D-mode power devices under PSpice simulation*

| Components | Part Number |
|---|---|
| $D_{ch}$ and $D_{disc}$ | UF4002 |
| $L_{comp}$ | LM311 |
| $G_{opt,gsf}$ | ACPL-H61L |
| DUT | IXTT20N50D |

| FWD | UJ3D06516TS |
|---|---|

(a)

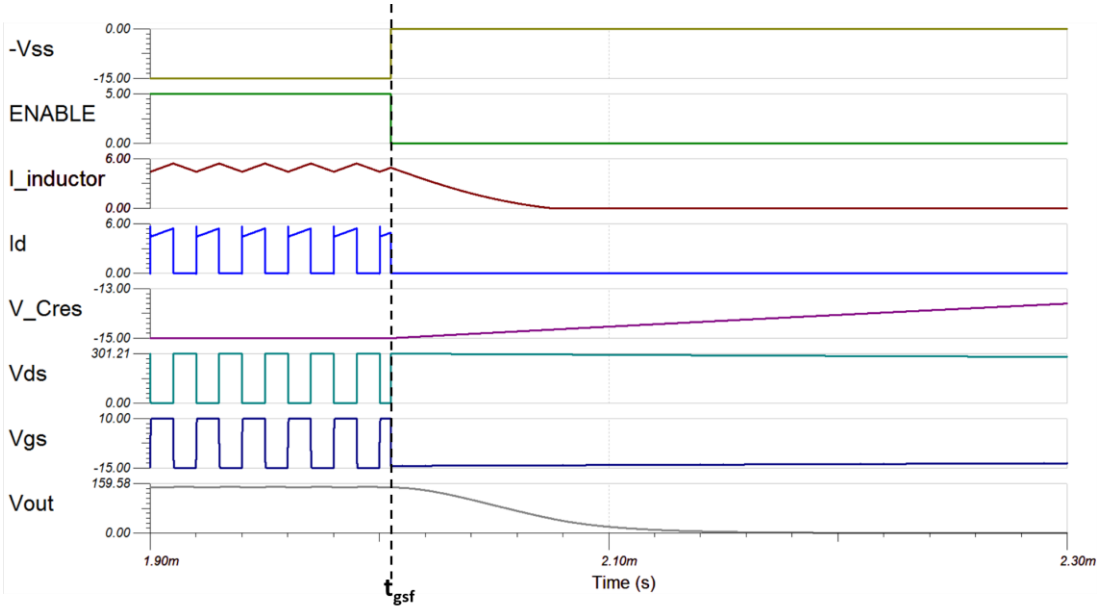
| Parameters | Value | Unit |
|---|---|---|
| $C_{res}$ | 560 | µF |
| $R_{comp,out}$ | 1 | kΩ |
| $R_{g,ext(on)}$ and $R_{g,ext(off)}$ | 5 | Ω |
| $R_{gsf,ref1}$ | 750 | Ω |
| $R_{gsf,ref2}$ | 1.5 | kΩ |
| $R_{out,en}$ | 402 | Ω |
| $R_{opt,in}$ | 915 | Ω |
| $V_{dc}$ | 300 | V |
| $+V_{opt}$ | +5 | V |
| $+V_{cc}$ | +10 | V |
| +/- $V_{ss}$ and +/- $V_{ss2}$ | +/-15 | V |

(b)

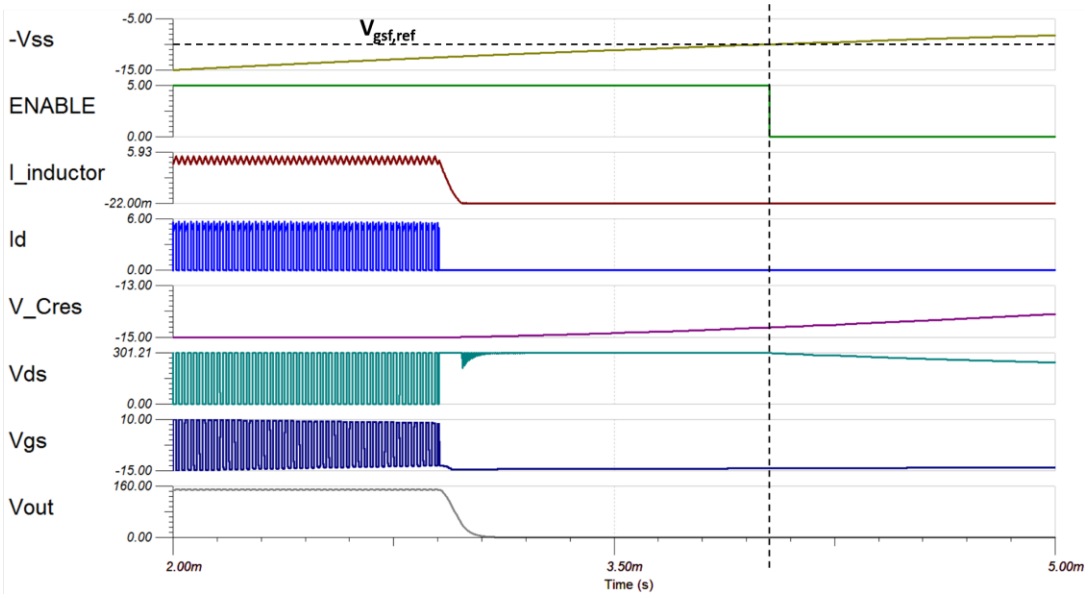
*Table 4-2: (a) Component selection and (b) circuit parameters for simulation of step-down dc-dc converter with GDSFP circuit in Figure 4-5(b)*

The circuit was simulated for both instantaneous and gradual -$V_{SS}$ failure and the resultant simulation waveforms are shown in Figure 4-10(a) and (b), respectively. The $S_{dc,link}$ is assumed to be an ideal switch. In case the -$V_{SS}$ is removed instantaneously as a worst-case scenario, the $M_{ch}$ in Figure 4-8(b) is turned on so that the power device in the converter circuit is turned off at the same time. From this point, $C_{res}$ is charged towards 0V via $R_{g,ext(off)}$, $D_{ch}$ and $M_{ch}$. At the same time, the comparator output becomes HIGH and thus ENABLE signal becomes LOW so that $S_{dc,link}$ is turned off within very short period of time as shown in Figure 4-10(a). Without the presence of $S_{dc,link}$, the D-mode power device is kept off for 17.4ms before its $V_{gs}$ exceeds the turn-on threshold value of -2V. In other words,

the D-mode power devices can be kept safe as long as the $S_{dc,link}$ is switched off within this period of time.




(a)




(b)

*Figure 4-10: Simulation waveforms of DC-DC converter with GDSFP scheme for (a) instantaneous, (b) gradual gate drive supply ($-V_{SS}$) failure events*

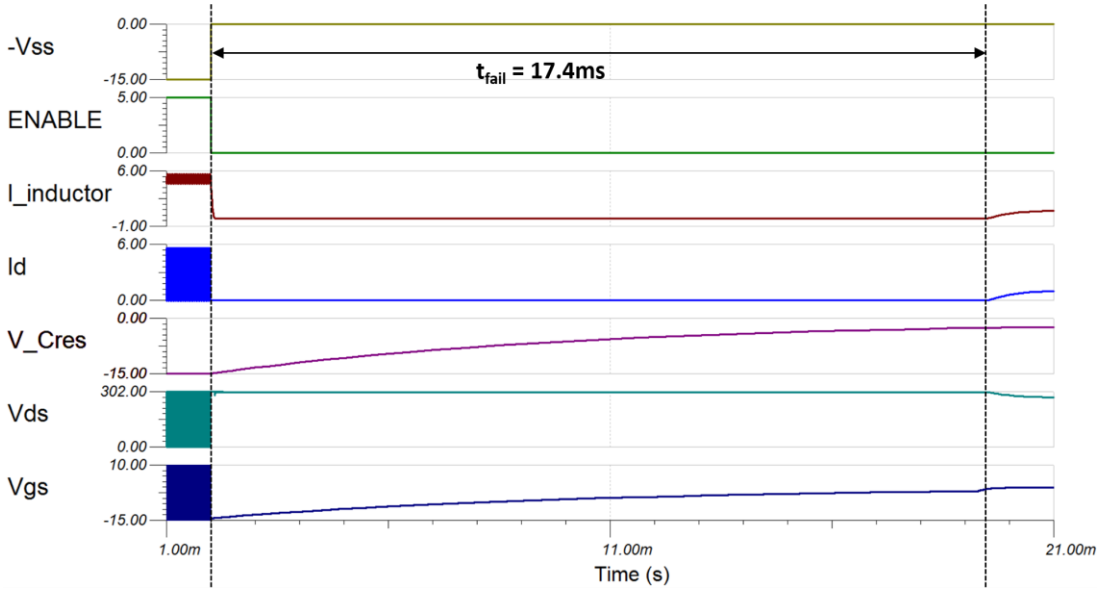



*Figure 4-11: GDSFP circuit response under instantaneous gate drive supply failure without the presence of $S_{dc,link}$*

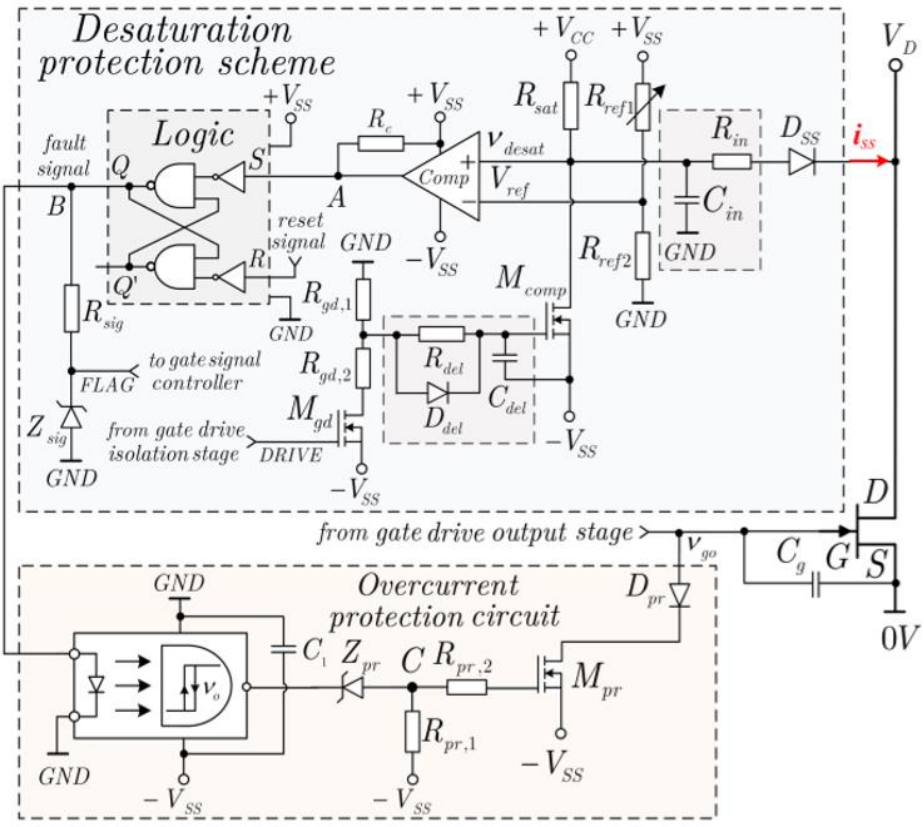
In a real system, however, the voltage supply may not fail instantaneously but fail gradually over a long period of time as represented in the simulation waveforms in Figure 4-10(b). In this case, the failure in $-V_{SS}$ supply will not be detected instantaneously; rather, it will be detected when it exceeds the reference value $V_{gsf,ref}$ at which the failure is detected by the GDSFP circuit. At this point, the ENABLE signal output will be LOW and thus the converter is isolated from the dc-link. Consequently, it is proven that the GDSFP scheme can ensure fail-safe operation of D-mode power devices for any $-V_{SS}$ failure characteristics.

## *4.5. Desaturation-based overcurrent protection (DOCP) scheme*

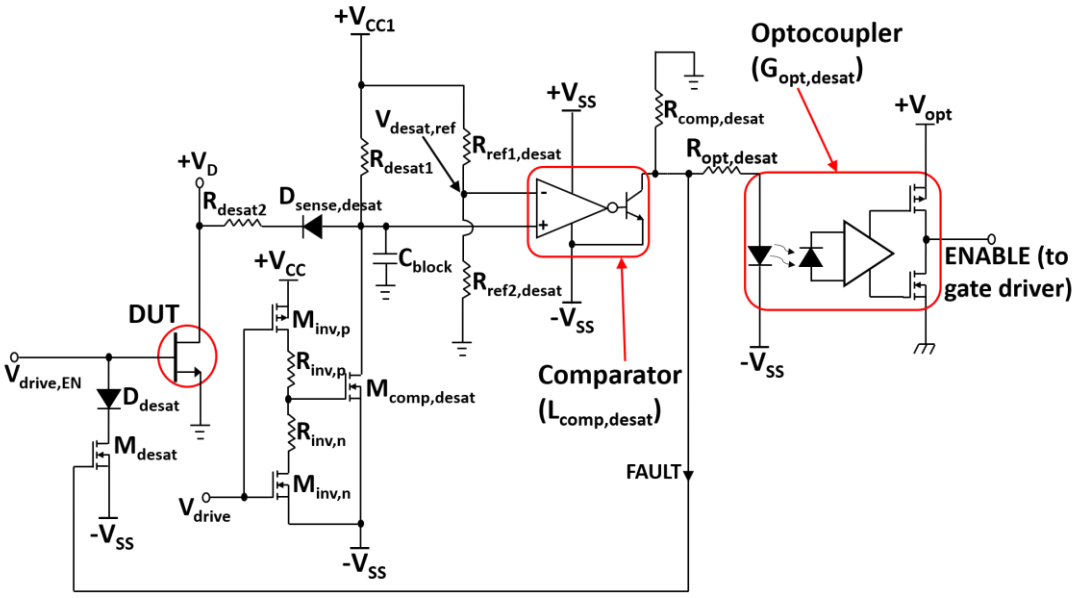
### *4.5.1. Circuit schematic and operating principles*

The shoot-through current may occur not only under gate drive supply failure events, but also during normal operating conditions due to overload or controller faults. This current must be cleared within a very short period of time in order to

prevent thermal damage of the switching power devices. One of the well-established methods to achieve this is the desaturation method by which an overcurrent is detected, and the command signal is sent to the gate driver IC so that the devices are held in their 'off' state until next gate drive pulse is applied. An experimental demonstration of the DOCP prototype and its operating principle were presented in [124] and its circuit schematic is shown in Figure 4-12(a). For this work, a refined DOCP circuit with reduced component counts and minimum propagation delay for faster circuit response was proposed as presented in Figure 4-12(b). This was achieved by removing the SR latch logic and an optocoupler in Figure 4-12(a) that introduced signal propagation delays.




(a)




(b)

*Figure 4-12: (a) Previously proposed DOCP scheme in [124] and (b) refined DOCP scheme under PSpice simulation*

The operating principle can be described as follows. During the normal operation, the gate drive signal is sent to the input of the inverting stage consisting of p-type and n-type MOSFETs, $M_{inv,p}$ and $M_{inv,n}$. When the $V_{drive}$ signal is low, the DUT will start its turn-off process and simultaneously $M_{inv,p}$ is turned on and the MOSFET connected to the non-inverting output of the comparator, $M_{comp,desat}$, is turned on. Thus, the non-inverting input of the comparator is clamped to $-V_{SS}$, and comparator output becomes low since $-V_{SS} < V_{ref,desat}$. It should be noted that $M_{comp,desat}$ must be turned on before the DUT is fully turned off in order to avoid false triggering of the FAULT signal. The time required for $M_{comp,desat}$ to be turned on is determined by the time constant $\left(R_{inv,p} + R_{Minv,p}\right) * C_{iss,Mcomp}$ where $R_{Minv,p}$ = on-state resistance of the MOSFET $M_{inv,p}$ and $C_{iss,Mcomp}$ = input capacitance of the MOSFET $M_{comp,desat}$.

When the $V_{drive}$ signal input is HIGH, the DUT starts to turn on and $M_{comp,desat}$ will start turning off at the same time. The $V_{desat}$ will rise to the following value when the $M_{comp,desat}$ is fully turned off:

$$V_{comp,in+} = \frac{R_{desat1} \cdot (V_{D,desat} + V_{ds,on})}{R_{desat1} + R_{desat2}} + \frac{R_{desat2} \cdot V_{CC1}}{R_{desat1} + R_{desat2}} \quad \ldots(4\text{-}8)$$

Where $V_{D,desat}$ = forward on-state knee voltage drop across $D_{sense,desat}$ and $V_{ds,on}$ = on-state drain-to-source forward voltage drop across the DUT. The time taken for the $V_{comp,in+}$ to reach steady state value $V_{desat}$ and thus for $M_{comp,desat}$ to be fully turned off is determined by the following time constant:

$$\tau_{blank} = R_{desat1} \cdot (C_{oss,Mcomp} + C_{blank}) \quad \ldots(4\text{-}9)$$

Where $C_{oss,Mcomp}$ = output capacitance of the MOSFET $M_{comp,desat}$. For $V_{comp,in+}$ to reach 98% of its final value, approximately 4 times $\tau_{blank}$ of time is required. This time interval is defined as 'blanking time', which is required to prevent false triggering of overcurrent detection signals by the comparator during device turn-on. Should the $M_{comp,desat}$ be fully turned off before DUT is fully turned on, then comparator will output FAULT signal to turn the DUT off even when overcurrent event is not present and thereby causing erroneous converter operation.

Should the two power devices be turned on at the same time during normal operation, a large shoot-through current will occur and thus $V_{ds}$ of the DUT and $V_{comp,in+}$ will start to rise up at a very fast rate. At some point, the $V_{comp,in+}$ will rise above the reference value ($V_{desat,ref}$) at the inverting input of the comparator ($L_{comp,desat}$) and thus the output FAULT signal of $L_{comp,desat}$ will become logic high. The on-state $V_{ds}$ drop value at which overcurrent is detected and hence desaturation circuit is activated can be mathematically expressed as:

$$V_{ds,on(desat)} = V_{comp,in-} \cdot \left(1 + \frac{R_{desat2}}{R_{desat1}}\right) - V_{CC1} \cdot \frac{R_{desat2}}{R_{desat1}} - V_{D,desat} \quad \ldots(4\text{-}10)$$

Where $V_{comp,in-} = V_{CC1} \cdot \frac{R_{ref2,desat}}{R_{ref1,desat}+R_{ref2,desat}}$

Subsequently, the input capacitance of the desaturation MOSFET ($M_{desat}$) will be charged up via $R_{comp,desat}$ with the time constant $R_{comp,desat}$*$C_{iss,Mdesat}$. The time required for the $V_{gs}$ of $M_{desat}$ to reach turn-on threshold voltage and thus $M_{desat}$ to be turned on can be expressed as the following:

$$t_{on,Mdesat} = R_{comp,desat} \cdot C_{iss,Mdesat} \cdot ln\left(\frac{V_{SS}}{V_{SS}-V_{gs,th}}\right) \quad \ldots(4\text{-}11)$$

After this period of time, $M_{desat}$ will be turned on and therefore DUT will be turned off and shoot-through current will be cleared out. Meanwhile, the LED at the input side of the optocoupler ($G_{opt,desat}$) will be turned on and thus the output ENABLE becomes logic low, which will be sent to the input side of the gate driver IC so that it is disabled. When the $V_{drive}$ signal becomes low, the ENABLE signal will be recovered high as the $L_{comp,desat}$ output becomes low; thus, the gate driver IC is enabled.

### *4.5.2. Component selection and simulation*

In order to validate the DOCP circuit performance without false logic triggering under normal operating conditions, the circuit was implemented in TINA-TI PSpice simulator. The electrical parameters and components used for circuit simulation are clearly presented in Table 4-3(a) and (b), respectively. The previous D-mode Si-MOSFET (IXTT20N50D) were used as power devices in the half-bridge circuit. For the diode $D_{sense,desat}$, a 2 kV rectifier with low junction capacitance and reverse recovery charge (BY203-20S) was used in order to prevent

excessive voltage spike at the non-inverting input of the comparator during the DUT turn-off transition. The same parts were used for comparator and optocoupler as in GDSFP circuit simulation in order to achieve minimum time delay and thus fast circuit response.

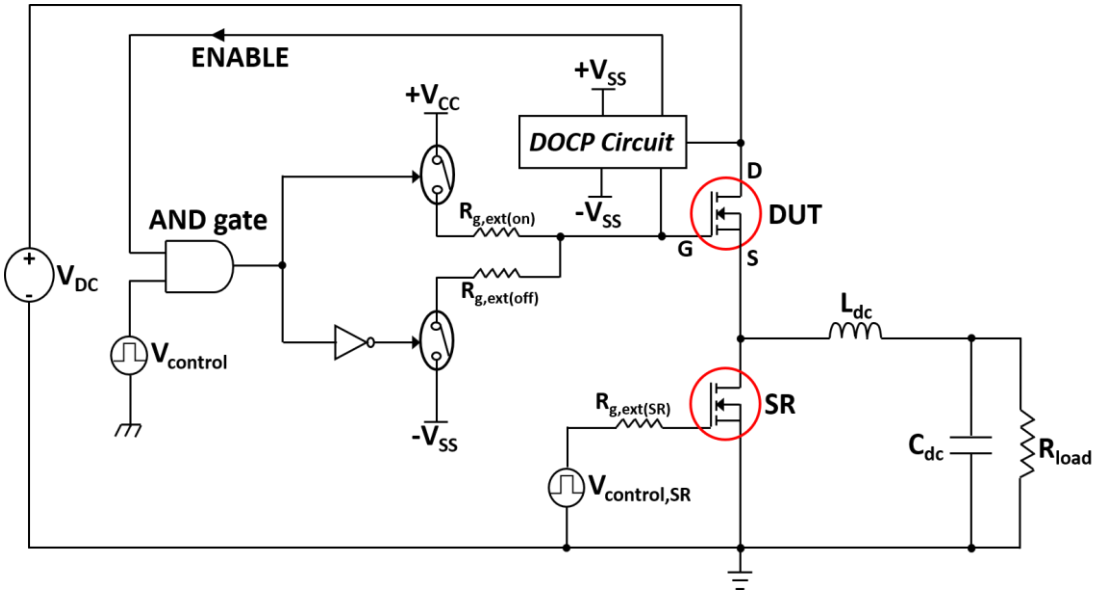



*Figure 4-13: Schematic of step-down dc-dc converter with the refined DOCP circuit proposed*

| Components | Part Number |
|---|---|
| AND gate | SN74LV08A |
| $D_{disc,desat}$ | RS1A |
| $D_{sense,desat}$ | BY203-20S |
| $G_{opt,desat}$ | ACPL-H61L |
| $L_{comp,desat}$ | LM311P |
| $M_{disc,desat}$ | IPD220N06L3 |
| $M_{inv,p}$ | IRFR5305PbF |
| $M_{inv,n}$ | IRFR3806PbF |
| $M_{comp,desat}$ | IPD220N06L3 |

(a)

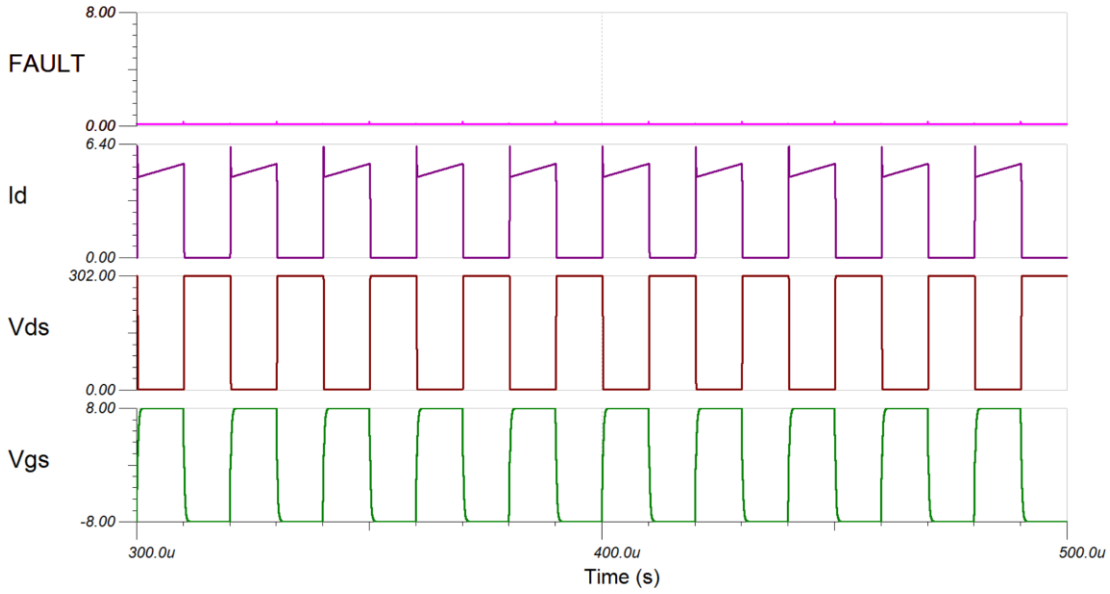
| Parameters | Values |
|---|---|
| $C_{block}$ | 200 pF |
| $R_{ref1,desat}$ and $R_{ref2,desat}$ | 10 Ω and 490 Ω |

| | |
|---|---|
| $R_{desat1}$ and $R_{desat2}$ | 500 Ω |
| $R_{comp,desat}$ | 500 Ω |
| $R_{g,ext(on)}$ and $R_{g,ext(off)}$ | 5 Ω |
| $R_{inv,p}$ and $R_{inv,n}$ | 4 Ω and 40 Ω |
| $+V_{cc1}$ and $+V_{opt}$ | +5 V |
| $+V_{cc}$ | +8 V |
| +/- $V_{SS}$ | +/- 8 V |

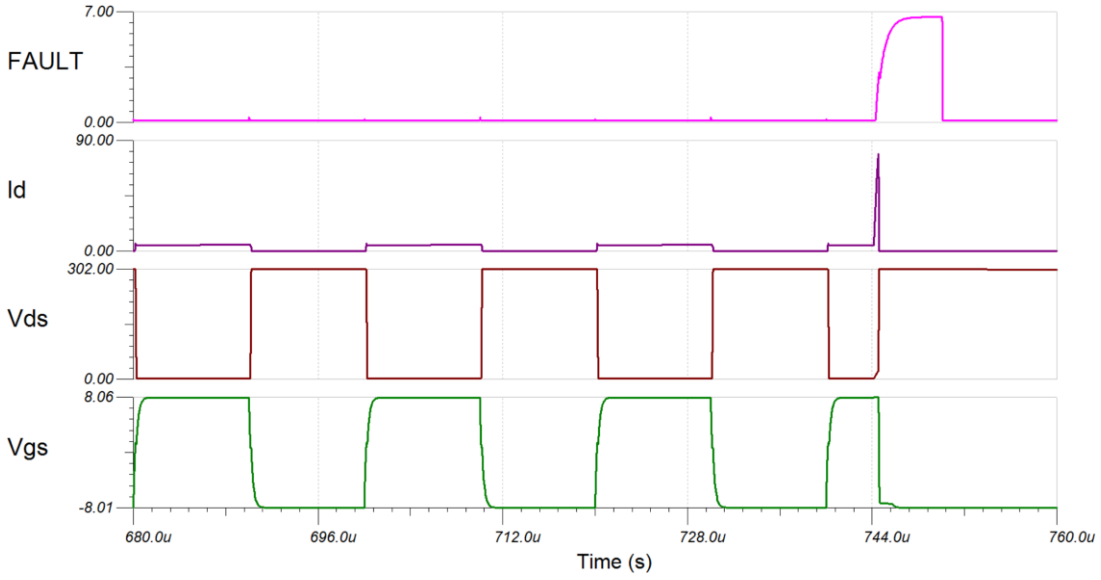
(b)

*Table 4-3: (a) Components and (b) electrical parameters for the simulation of step-down dc-dc converter with the refined DOCP circuit in Figure 4-12(b)*

The resistor and capacitor values were selected so that $t_{blank}$ = 2us to leave sufficient time for Si-MOSFETs to be fully turned on. The simulation waveforms under normal operation and short-circuit event are clearly labelled and shown in Figure 4-14(a) and (b), respectively. According to the figure, it is shown that the shoot-through current is cleared out within 500ns of its occurrence. Also, as shown in Figure, the dc-dc converter can operate normally as expected without FAULT signal triggered HIGH erroneously during the power devices' turn-off transients. Therefore, it can be expected that power devices in half-bridge converters are capable of normal switching operation independent of the DOCP circuit when shoot-through current is not present.




(a)




(b)

*Figure 4-14: (a) Normal operation of step-down dc-dc converter with DOCP scheme and (b) DOCP circuit response to a short-circuit event*

## *4.6. Fail-safe gate drive circuit prototype demonstration*

In order to emulate the gate supply failure event using the FPGA controller, the circuit in Figure 4-15 was implemented onto a solderable breadboard as a means of interfacing the controller with the dc voltage regulators in the tester circuit board. The pulse output from the controller, $V_{pulse}$, is applied to the base electrode of the

NPN bipolar junction transistor, $B_{npn1}$. When $V_{pulse}$ is logic HIGH, $B_{npn1}$ turns on, which turns on the PNP-BJT ($B_{pnp1}$) and thus the NPN transistor at the push-pull output stage ($B_{npn,pp}$). As a result, the 24V DC voltage is supplied to the input stage of isolated dc voltage regulators in the half-bridge tester circuit board, which then supplies the required voltages for gate drivers. When $V_{pulse}$ logic level goes LOW, all the transistors in the logic level shift circuit are turned off and thus input to DC/DC voltage regulators goes to zero; consequently, the gate drive voltage supplies are removed.

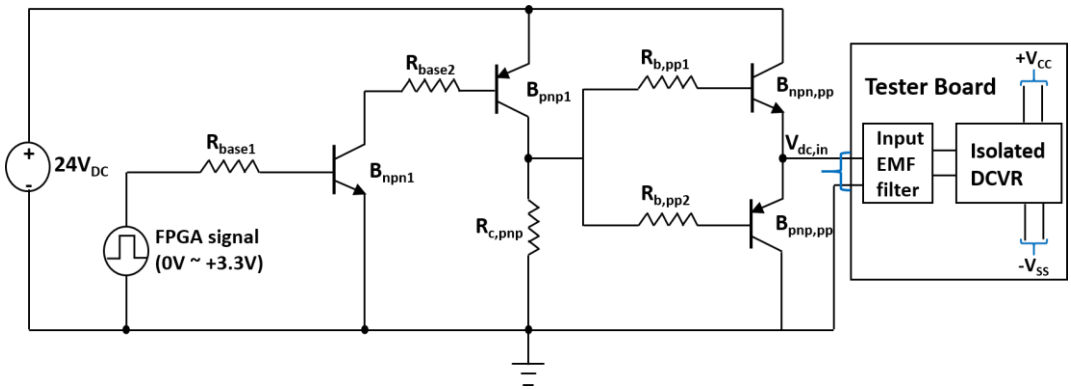



*Figure 4-15: Schematic of logic level shifter circuit interfacing between FPGA controller and input stage of isolated dc voltage regulators for gate drivers in half-bridge tester board*

To demonstrate the functionalities of the protection schemes proposed so far, DOCP and GDSFP, in half-bridge converter hardware, a layout of prototype tester circuit was designed using Proteus Professional software as according to the schematic in Figure 4-16. The circuit layout was designed so that gate loop and power loop inductances are minimised whilst parasitic capacitances between the input and output sides of the gate driver ICs are minimised. A top view of the fabricated circuit board is presented in Figure 4-17. The 3 kV, 8 A rated GaN PSJ samples were used as switching power devices in the prototype tester circuit.

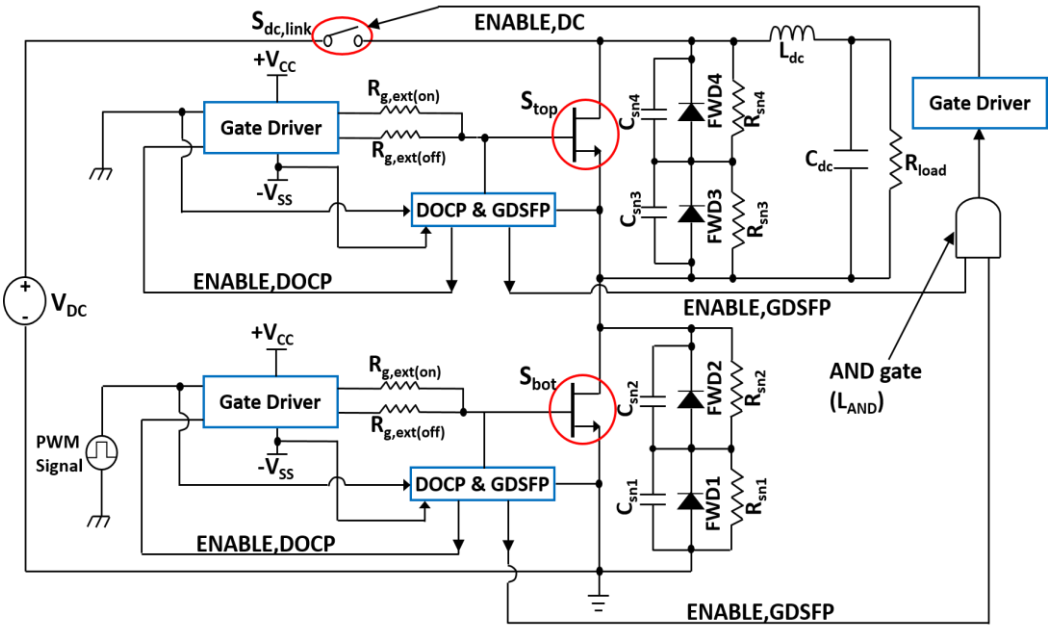



*Figure 4-16: Schematic of fail-safe gate drive tester circuit prototype*

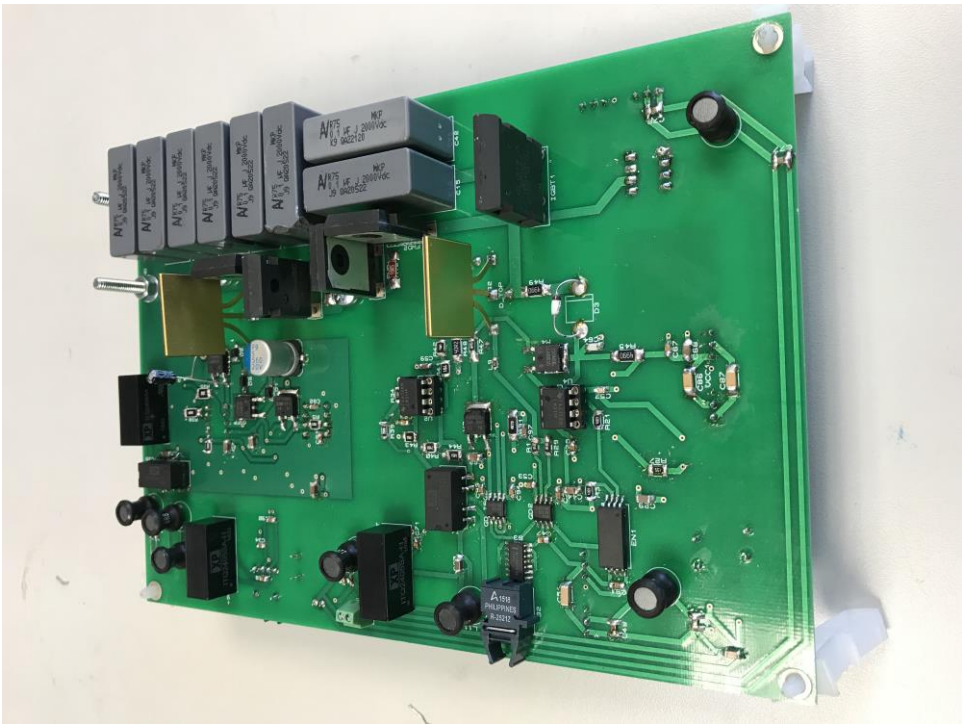


*Figure 4-17: Prototype fail-safe gate drive tester circuit board*

### *4.6.1. Prototype GDSFP hardware demonstration*

The components selected and electrical parameters for GDSFP prototype circuit demonstration are shown in Table 4-4(a) and (b), respectively. For $S_{dc,link}$, 4

kV / 40 A rated IGBT (IXEL40N400) device was used for sufficient voltage blocking capability; unipolar devices with breakdown voltage of > 3 kV and low $R_{ds,on}$ are not commercially available. As power semiconductor devices such as MOSFETs and IGBTs that exhibit fast response time in the range of 100s of ns, In contrast, electromechanical switches such as relays or contactors typically exhibit response times in the range of few milliseconds (ms), which is by few orders of magnitude slower than power devices. In addition, their footprints and weights are typically much larger than the packaged power devices and thus were deemed inappropriate for this application.

The snubber capacitors and resistors ($C_{sn}$ and $R_{sn}$) of 100 pF and 5 MΩ were chosen based on the equations in [125] so that the dynamic and static voltage mismatches between the two series-connected diodes are kept within 400 V for a dc-link voltage of 3 kV assumed. The IGBT gate driver with input-to-output (IO) galvanic isolation (IX3120G) that has a typical propagation delay of 300 ns and maximum I-O insulation voltage of 3750 $V_{rms}$ was implemented in the hardware prototype. For gate driver power supplies, $V_{cc}$ and $-V_{ss}$, isolated dc voltage regulators with significantly smaller input-to-output capacitance values than the ones in [124] were used to prevent false logic triggering due to the coupled dV/dt noise during switching events.

| Components | Part Number |
|---|---|
| $D_{ch}$ and $D_{disc}$ | US1AFA |
| $L_{comp}$ | LM311P |
| Gate Driver IC | Si8271BB-IS |
| $G_{opt,gsf}$ | ACPL-H61L |
| $L_{AND}$ | SN74LV08A |
| $M_{ch}$ | IPD220N06L3 |

| | |
|---|---|
| $S_{dc,link}$ Gate Driver IC | IX3120G |
| $S_{dc,link}$ | IXEL40N400 |
| $+V_{CC}$ regulator | ITQ2405SA |
| $+/-V_{SS}$ regulator | ISA2415-H |

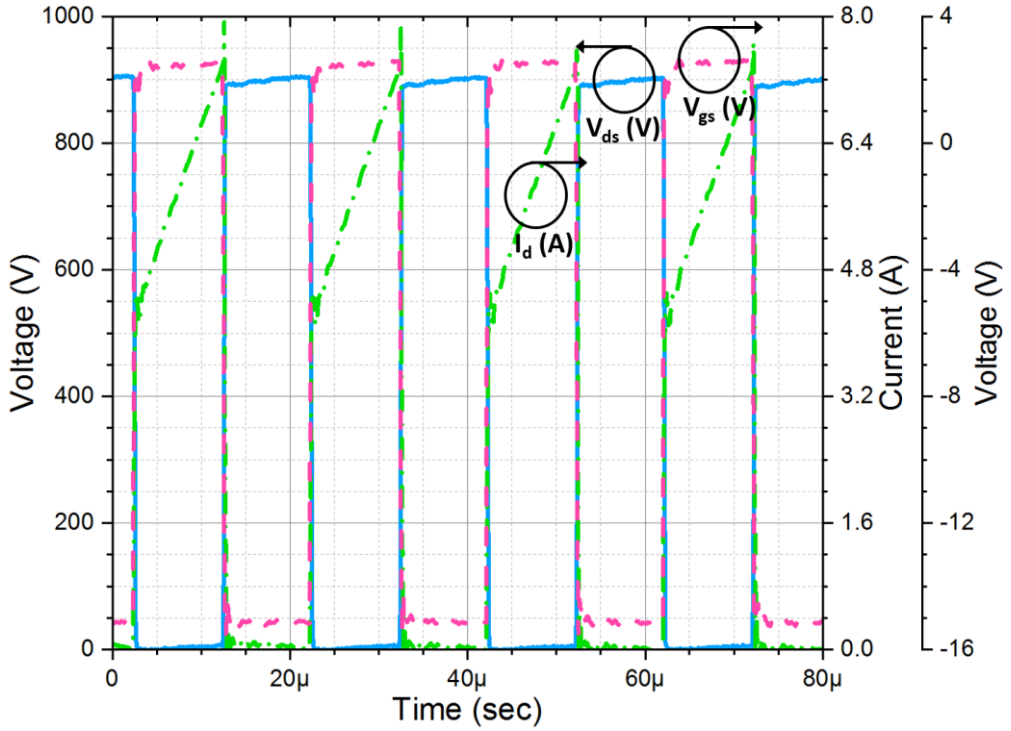
(a)

| Parameters | Values |
|---|---|
| $C_{res}$ | 560 µF |
| $C_{sn1} \sim C_{sn4}$ | 100 pF |
| $R_{comp,out}$ | 1 kΩ |
| $R_{gsf,ref1}$ and $R_{gsf,ref2}$ | 750 Ω and 1.5 kΩ |
| $R_{out,en}$ | 402 Ω |
| $R_{opt,in}$ | 915 Ω |
| $R_{sn1} \sim R_{sn4}$ | 5 MΩ |
| $V_{dc}$ | 900 Ω |
| $+V_{opt}$ | +5 V |
| $+/- V_{ss}$ and $+/- V_{ss2}$ | +/-15 V |

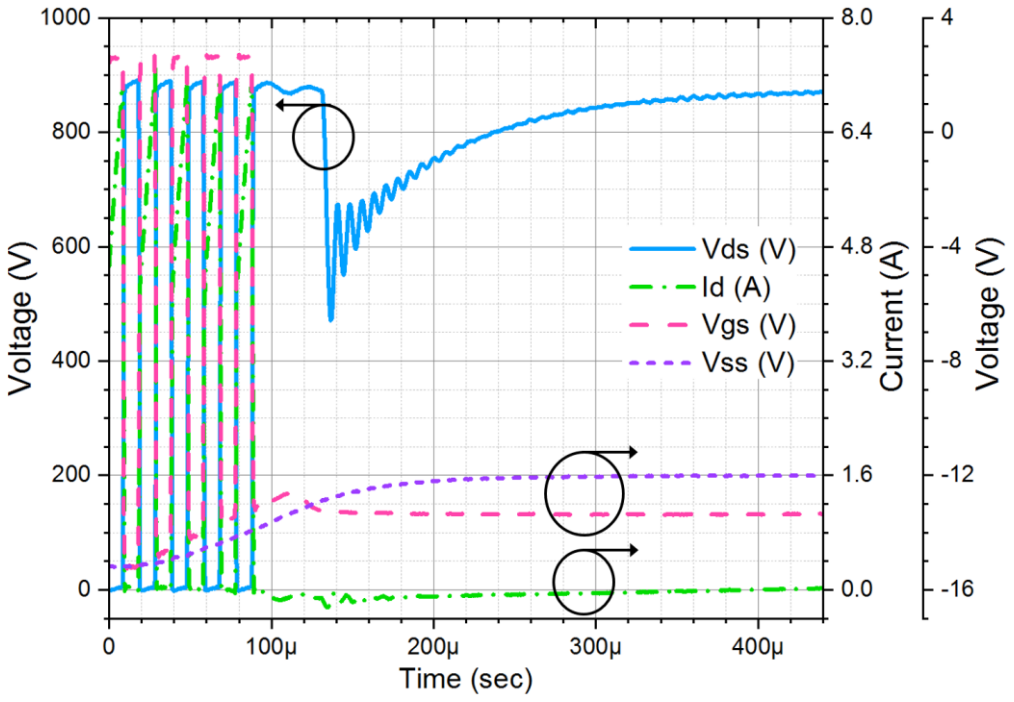
(b)

*Table 4-4: (a) Components and (b) electrical parameters used in experimental validation of the refined GDSFP circuit prototype*

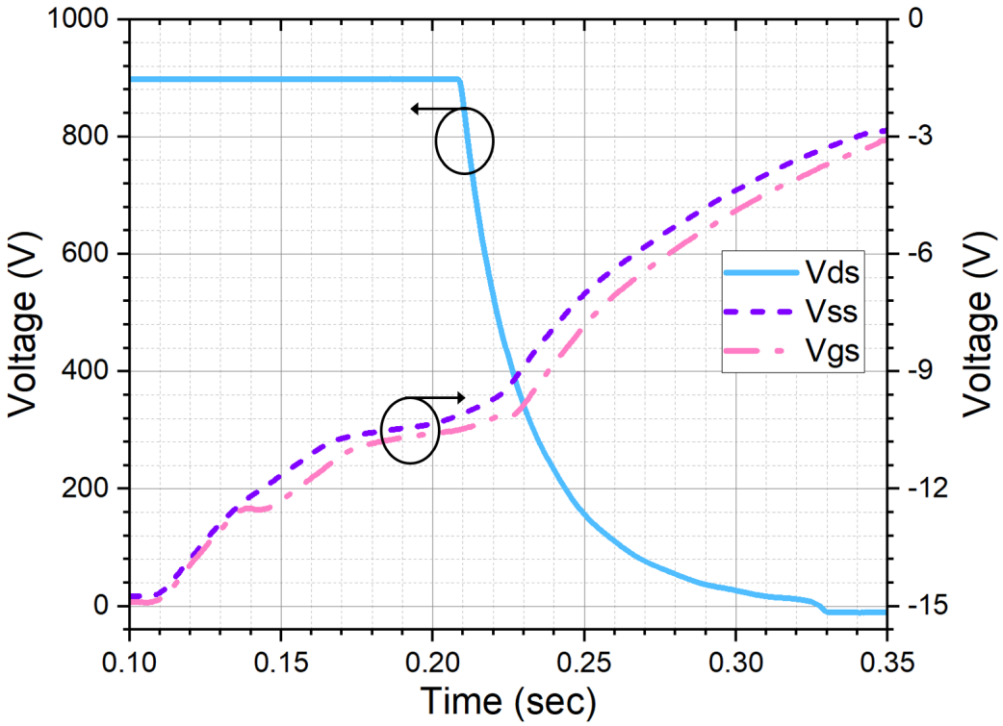
For its demonstration, a PWM signal with frequency of 50kHz and duty cycle of 50% was applied for the first 3.2ms for the circuit to reach steady-state converter operation point. The dc power supply input to the gate drive voltage supply regulators were removed 3 ms via FPGA command signal after the PWM signal is applied. The drain voltage and current were measured using single-ended voltage probe with 250 MHz bandwidth and CWT Rogowski coil with 30 MHz bandwidth, respectively. The load resistor of 75 Ω was placed on the output side, which induced an average load current of 6 A. The steady-state voltage and current waveforms of the tester circuit in Figure 4-16 are clearly labelled and presented in Figure 4-18(a).


Voltage (V)
Current (A)
Voltage (V)
Time (sec)
$V_{ds}$ (V)
$V_{gs}$ (V)
$I_d$ (A)
1000
800
600
400
200
0
8.0
6.4
4.8
3.2
1.6
0.0
4
0
-4
-8
-12
-16
0
20µ
40µ
60µ
80µ

(a)


Voltage (V)
Current (A)
Voltage (V)
Time (sec)
Vds (V)
Id (A)
Vgs (V)
Vss (V)
1000
800
600
400
200
0
8.0
6.4
4.8
3.2
1.6
0.0
4
0
-4
-8
-12
-16
0
100µ
200µ
300µ
400µ

(b)




(c)

*Figure 4-18: (a) Voltage and current waveforms under steady-state operation of the converter, and circuit response under gate drive supply failure event at (b) short (c) long time scale*

### *4.6.2. Prototype DOCP Demonstration*

Along with its simulation, the DOCP circuit in Figure 4-12(b) was also demonstrated experimentally to validate its capability to prevent failure of the GaN PSJ-FETs due to shoot-through current during normal operation. The components used for DOCP scheme and its electrical parameters are enlisted in Table 4-5(a) and (b), respectively. Due to the limited availability of the diode (BY203-20S) used for simulation, a 3 kV rectifier with low reverse recovery charge (F30) was used as an alternative. The values of resistors $R_{ref1}$ and $R_{ref2}$ were set so that $V_{ds,on(desat)}$ = 4V.

| Components | Part Number |
|---|---|
| $D_{disc,desat}$ | US1AFA |
| $D_{desat,sense}$ | F30 |
| Gate Driver IC | Si8271BB-IS |

| | |
|---|---|
| $G_{opt,desat}$ | ACPL-H61L |
| $L_{comp,desat}$ | LM311P |
| $M_{comp,desat}$ and $M_{disc,desat}$ | IPD220N06L3 |
| $M_{inv,p}$ and $M_{inv,n}$ | IRFR5305PbF and IRFR3806PbF |
| $+V_{CC1}$ regulator | ITQ2405SA |
| $+V_{CC}$ and $+/-V_{SS}$ regulators | ISA2415-H |

(a)

| Parameters | Values |
|---|---|
| $C_{block}$ | 200 pF |
| $R_{comp,desat}$, $R_{desat1}$ and $R_{desat2}$ | 500 Ω |
| $R_{g,ext(off)}$ | 15 Ω |
| $R_{inv,p}$ and $R_{inv,n}$ | 4 Ω and 40 Ω |
| $R_{ref1}$ and $R_{ref2}$ | 10 Ω and 487 Ω |
| $+V_{cc1}$ and $+V_{opt}$ | +5 V |
| $+V_{cc}$ | +2.5 V |
| $+/-V_{SS}$ | +/- 15 V |

(b)

*Table 4-5: (a) Components and (b) electrical parameters used in experimental validation of the prototype DOCP circuit*

For the demonstration of DOCP circuit under short-circuit events, the double pulse and single pulse signals were applied to the $S_{bot}$ and $S_{top}$ in Figure 4-5(b), respectively. The resultant voltage and current waveforms of the DUT ($S_{bot}$) during the shoot-through event under dc-link voltage of 700V are clearly labelled and shown in Figure 4-19. From the figure, it can be observed that the drain current rises rapidly towards current levels of > 30 A, which corresponds to the saturated drain current of the 8 A rated large area GaN PSJ-FETs. shoot-through current is cleared out 1.48μs after its occurrence. The shoot-through current decreases slightly over time, which is very likely due to the lattice heating of the device and thus degradation in electron mobility. The shoot-through current is cleared away at

1.48µs after its occurrence, which is much shorter than the response time of 3.5µs for the previous solution proposed in [124]. Hence, the refined DOCP proposed for this work has showed superior performance compared to its previous counterpart and that any power devices can operate reliably without thermal failure. Nevertheless, the response time extracted from hardware test is much longer than its simulation counterpart of 500 ns, which is very likely due to an offset in the Si-MOSFET models' capacitance values and comparator I/O propagation delay time from their actual values.

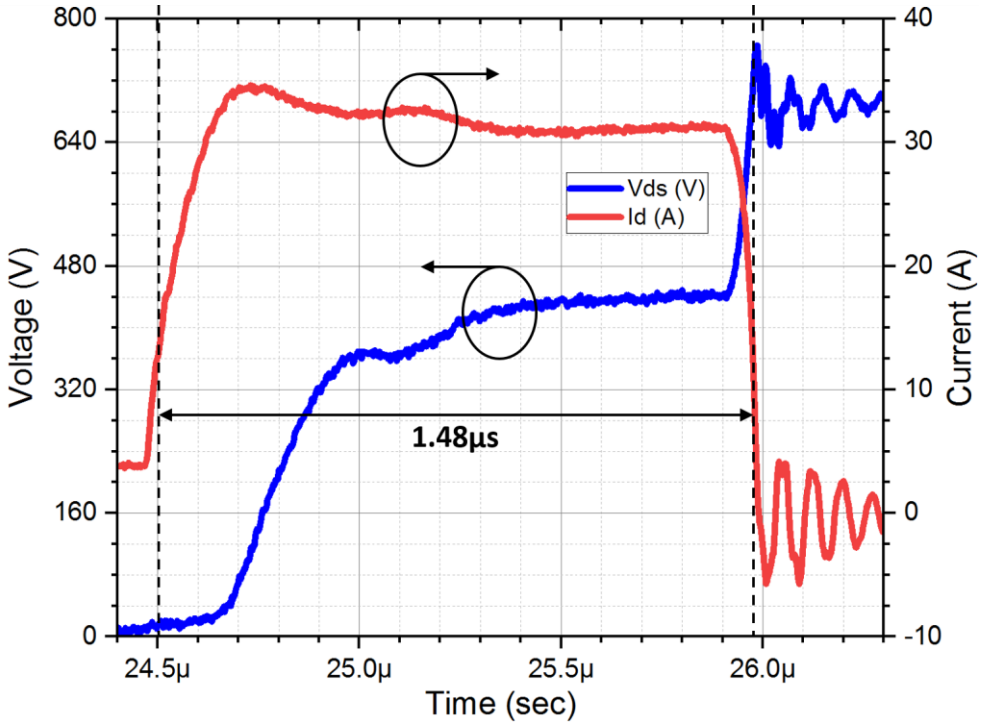



*Figure 4-19: DOCP circuit response under shoot-through event for large area PSJ-FETs under 700V dc-link*

## *4.7. Fail-safe gate drive circuit: limitations and improvement*

### *4.7.1. Limitations in the refined GDSFP solution*

The fail-safe gate driver scheme proposed and validated in Chapter 4 has mitigated a critical safety concerns associated with shoot-through event during normal operation and D-mode device behaviour under gate driver supply failure event. However, the GDSFP schemes in Figure 4-8 and Figure 4-9 are capable of detecting the failure of turn-off gate drive voltage ($-V_{SS}$) supply whilst uncapable of detecting GDSFP drive voltage ($\pm V_{SS2}$) failure. Should the $\pm V_{SS2}$ supplies fail before the $-V_{SS}$ for the gate driver is removed, then the ENABLE output will remain logic HIGH even when $-V_{SS}$ supply is removed. Hence, the GDSFP circuit cannot detect the failure and send a command signal to the DC-link switch ($S_{dc,link}$) to isolate the half-bridge circuit from DC-link and thus the power devices will be turned on at some point and be driven into saturation at time $t = t_{sw,sat}$ as shown in the waveforms in Figure 4-20, which is regarded as an unsafe region to operate as the full DC-link voltage is dropped across the device.

Also, in Figure 4-8(b), the ENABLE output from $G_{opt}$ is directly fed into the $S_{dc,link}$ gate driver input. Although this configuration did not cause an issue for circuit operation, it resulted in long copper traces crossing all the way from $G_{opt}$ output side to the $S_{dc,link}$ and thus extra PCB area required for its implementation. For a three-phase voltage-sourced converter, this means that large number of traces will need to be fed into the $S_{dc,link}$ gate driver, which may lead to excessively large PCB area and cost of implementation. Furthermore, as the input of gate driver ICs remain enabled even when $-V_{SS}$ exceeds the failure detection threshold, the gate driver output will swing from $+V_{CC}$ to $-V_{SS}$ unless $V_{CC} - V_{SS}$ has reached the undervoltage lockout (UVLO) threshold of the gate driver. As a result, D-mode

power device will still be driven by the incoming control signal even after -$V_{SS}$ failure is detected, which is not a desirable feature for the protection circuit.

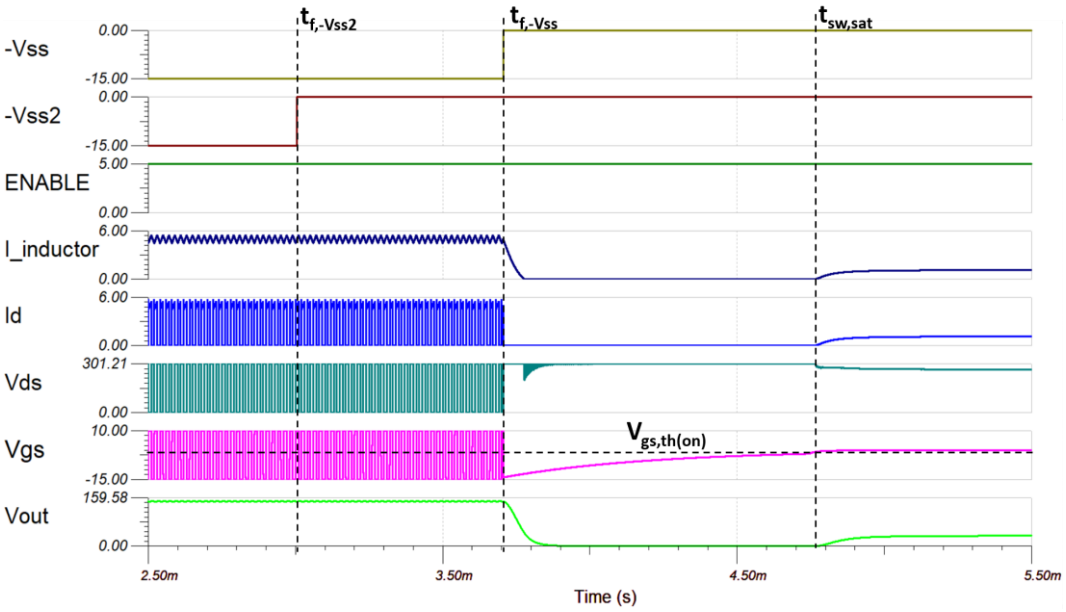



*Figure 4-20: Unsafe mode of operation of the refined GDSFP scheme (Figure 4-8(b)) under -$V_{SS2}$ supply failure*

### *4.7.2. The 2nd GDSFP prototype scheme*

A schematic of the 2nd GDSFP prototype circuit with which shortcomings of the previous prototype were overcome is presented in Figure 4-21. In this circuit, the output of $G_{opt,gsf}$ is fed into the one of the two inputs of an logic AND gate, which feeds its output to the enable (EN) input pin of the gate driver IC. Therefore, the gate driver will be disabled when either overcurrent fault or negative gate drive (-$V_{SS}$) supply failure is detected, which then prevents any incoming PWM signals from driving the D-mode power devices. In addition, the ENABLE output from $G_{opt,gsf}$ is fed to the controller IC, which then sends a command signal to the DC-link switch. With this approach, the number of long copper traces trespassing through the power circuit may be minimised, which yields the reduction in the PCB area required and capacitive coupling from logic circuit side to the power circuit

side. Also, the voltage supplies for input stage of gate driver IC and output stage of $G_{opt,gsf}$ are now all tied to a common supply, $+V_{CC,in}$, which is being fed via negative voltage supply for GDSFP comparator ($L_{comp}$), $-V_{SS2}$. Thereby, should the $-V_{SS2}$ supply fail, so does the $+V_{CC,in}$ supply; thus, the false triggering of $G_{opt,gsf}$ output logic under $-V_{SS2}$ failure event, as discussed in Chapter 4, is inherently prevented.

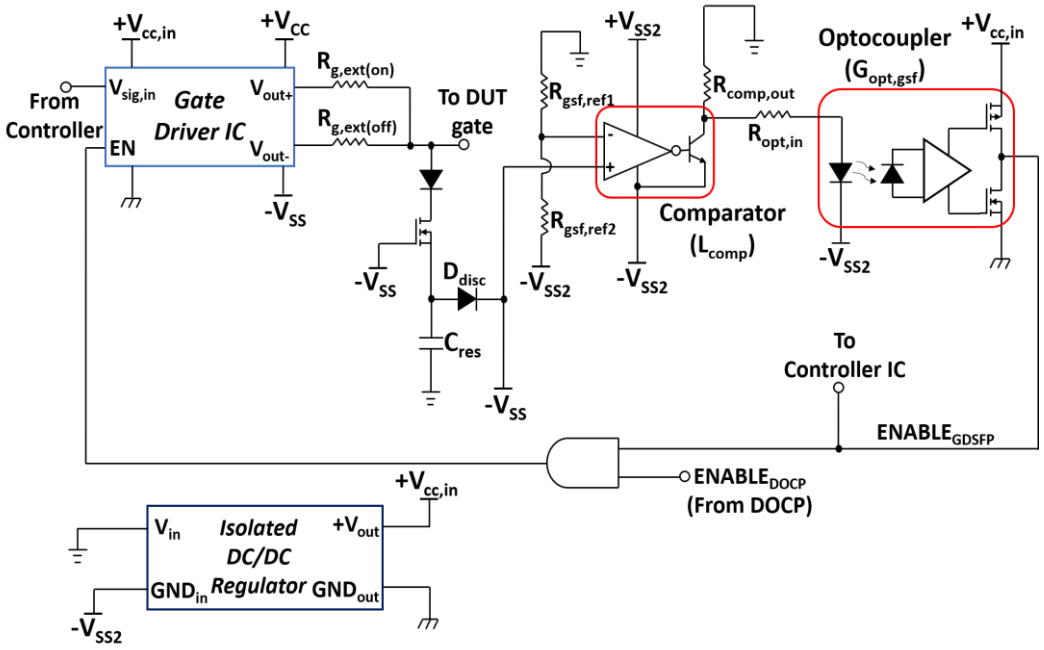



*Figure 4-21: 2nd GDSFP prototype circuit schematic*

The 2nd prototype GDSFP scheme was simulated using the PSpice models of the circuit components enlisted in Table 4-1(a) under the TINA-TI simulator with the same buck dc-to-dc converter configuration as in Figure 4-9. For this simulation, the $+V_{cc,in}$ supply (for the input side logic circuit) was modelled as an ideal voltage source controlled by $-V_{SS}$; the value of $+V_{cc,in}$ was made proportional to the potential difference between ground and $-V_{SS}$. The electrical parameters used for the simulation are clearly presented in Table 4-6. In the simulation, it was assumed that all power supplies fail instantaneously at the same point of time in order to emulate the worst-case scenario. The resultant simulation waveforms under fail-

safe mode are shown in Figure 4-22. From the simulation waveforms, it has been verified that the fail-safe operation of half-bridge converters is guaranteed by the 2nd prototype of GDSFP scheme even when all of the power supplies to the circuitries are removed instantaneously.

| Components | Part Number |
|---|---|
| AND gate | SN74LV08A |
| $D_{ch}$ and $D_{disc}$ | UF4002 |
| DUT | IXTT20N50D |
| FWD | UJ3D06516TS |
| $G_{opt,gsf}$ | ACPL-H61L |
| $L_{comp}$ | LM311 |

(a)

| Parameters | Value | Unit |
|---|---|---|
| $C_{res}$ | 560 | µF |
| $R_{comp,out}$ | 1 | kΩ |
| $R_{gsf,ref1}$ | 750 | Ω |
| $R_{gsf,ref2}$ | 1.5 | kΩ |
| $R_{out,en}$ | 402 | Ω |
| $R_{opt,in}$ | 915 | Ω |
| $V_{dc}$ | 300 | V |
| $+V_{cc,in}$ | +5 | V |
| $+V_{cc}$ | +10 | V |
| +/- $V_{ss}$ and +/- $V_{ss2}$ | +/-15 | V |

(b)

*Table 4-6: (a) Components and (b) electrical parameters for PSpice simulation of the improved GDSFP scheme (Figure 4-20)*

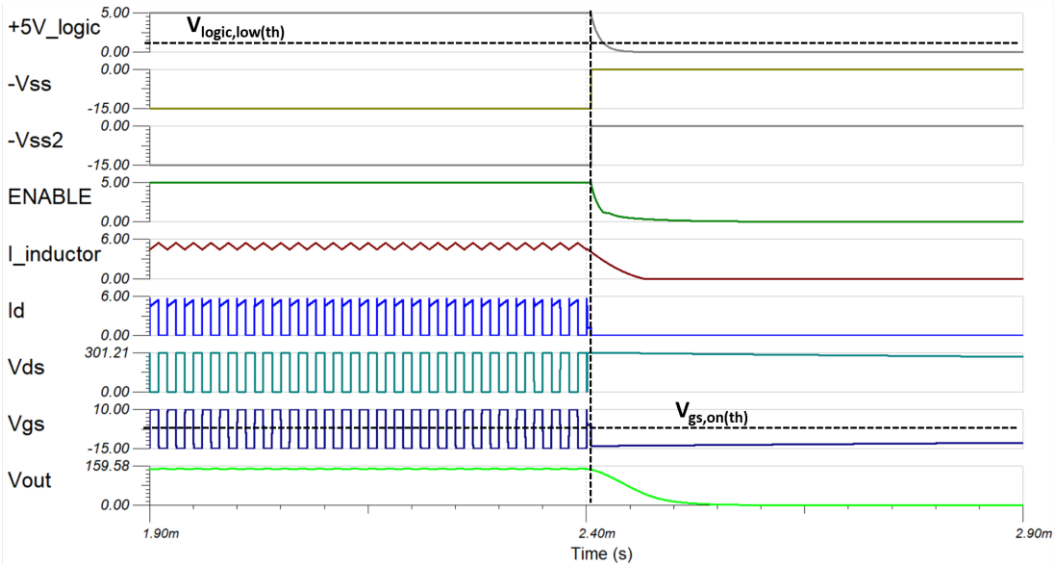
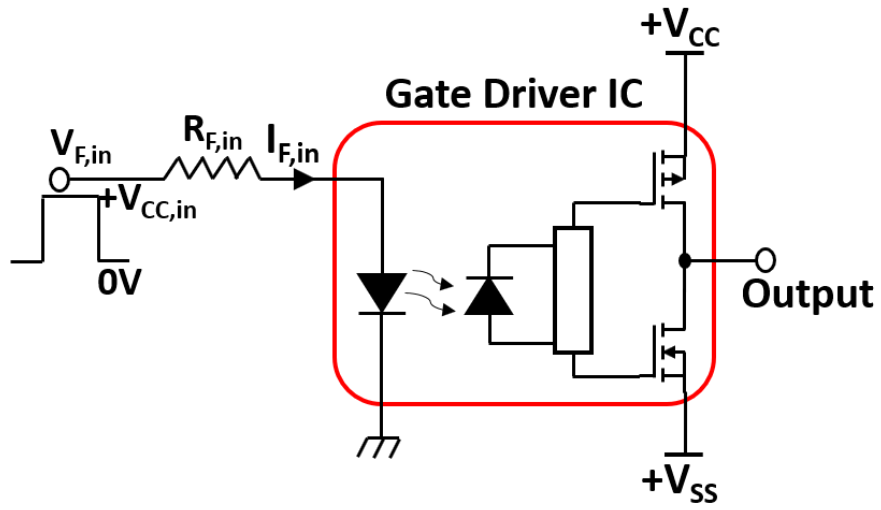
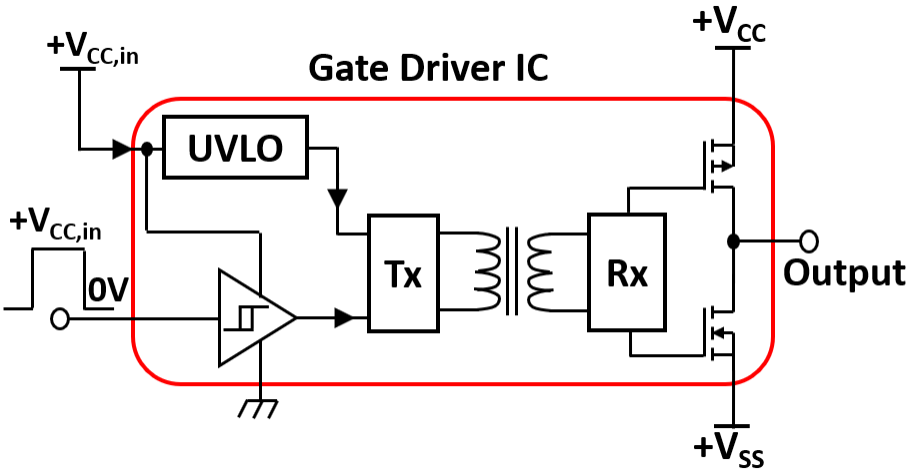



*Figure 4-22: Simulated voltage and current waveforms of the step-down dc-dc converter under simultaneous supply failure (worst case) in the 2nd GDSFP prototype scheme*

The logic low threshold voltage ($V_{logic,low(th)}$) of $S_{dc,link}$ gate driver input will be dependent upon the threshold input current value for logic LOW detection in case of an optocoupler isolation or the input undervoltage lockout (UVLO) detection voltage in case of CMOS compatible logic input with UVLO detection that will guarantee that $S_{dc,link}$ is turned 'off' whenever $+V_{cc,in}$ falls below UVLO detection level. Whether its value depends on the input drive current or voltage threshold value for logic state detection is dependent upon the type of isolated gate driver's input configuration for driving $S_{dc,link}$ presented in Figure 4-23(a) and (b).




(a)




(b)

*Figure 4-23: Typical isolated gate driver IC configuration with (a) optical coupling input with LED and (b) CMOS-compatible input with UVLO detection*

## *4.8. Summary*

In this chapter, verification of the performance of new protection scheme for fail-safe operation of D-mode power devices in voltage-sourced converters were presented and discussed in detail.

The discussion commenced with an overview of previous works on fail-safe operation of D-mode power devices in power converters. Majority of the previous

solutions proposed so far relied upon shoot-through current of D-mode devices in power converters during their initial start-up phase to generate negative gate drive voltages required for their turn-off. Their response time were determined to be in order of 10s of μs, which is long enough for the power devices to potentially fail during the initial start-up. Another solution, on which this work is based, serves to send a command signal to the controller to isolate converter circuit from the dc-link using a solid-state switch whilst holding the D-mode devices off and disabling gate driver ICs when the gate drive supply failure is detected. This solution also included desaturation scheme for clearing out overcurrent under short-circuit events during normal operation. The major drawback of this solution was that the gate driver ICs are kept disabled even after power supplies are recovered and thus the converter cannot operate normally.

Subsequently, a gate drive supply failure protection circuit, which is a refined version of its previous counterpart [124] with less component counts, minimum propagation delay and flawless operation under gate drive supply recovery events, was proposed, simulated and experimentally validated for this work. It was verified by the simulation and experimental results that the D-mode devices are always kept safe as long as the dc-link switch can be switched off within a time frame given by the product of turn-off gate resistor and charge reservoir capacitor.

Then, a refined version of the previous desaturation-based overcurrent protection scheme was proposed. The mathematical analysis of the critical parameters for its design were carried out, and criteria for its component selection was discussed in detail. The PSpice simulation of the proposed circuit was then carried out in order to validate its functionality. A prototype hardware of the circuit was also implemented for testing and from its experimental result its response time

was determined as 1.48 µs, which is much shorter than the response time of 3.5 µs for the previous solution. Therefore, this circuit can be used for clearing out short-circuit events during normal operation of D-mode and E-mode power devices.

Finally, the limitations of the refined GDSFP were clearly identified and overcome by the new improved GDSFP scheme. The functionality of this circuit was verified by the PSpice simulation.

# 5 High-Efficiency GaN Converter Design

## *5.1. Fail-safe dc-dc converter with D-mode power devices*

### *5.1.1. Hardware prototype*

The schematic diagram of the prototype fail-safe dc-to-dc converter with D-mode GaN power devices demonstrated for this work is presented in Figure 5-1. In this circuit, two dc-link switches are included; one for high-voltage side ($S_{dc,HV}$) and the other for low-voltage side ($S_{dc,LV}$). These switches serve to isolate the converter from the DC voltage supplies in case the negative gate drive supply voltage ($-V_{SS}$) becomes inadequate for D-mode power devices to be turned off; thereby, the shoot-through event and thus device failure are prevented. On the LV side, a means through which inductor current can freewheel when $S_{dc,LV}$ is left open was provided via additional freewheeling diode, $FWD_{dc,LV}$. The $S_{dc,HV}$ and $S_{dc,LV}$ were controlled via Digilent Basys 2 FPGA development board, which was configured as a finite state machine such that the two dc-link switches can be closed back again only when $-V_{SS}$ supply becomes active again and the reset switch (RST_SW) is toggled by the user. The FSM logic circuit diagram to which the FPGA was configured and its logic truth table are presented in the appendix (Section 7.2).

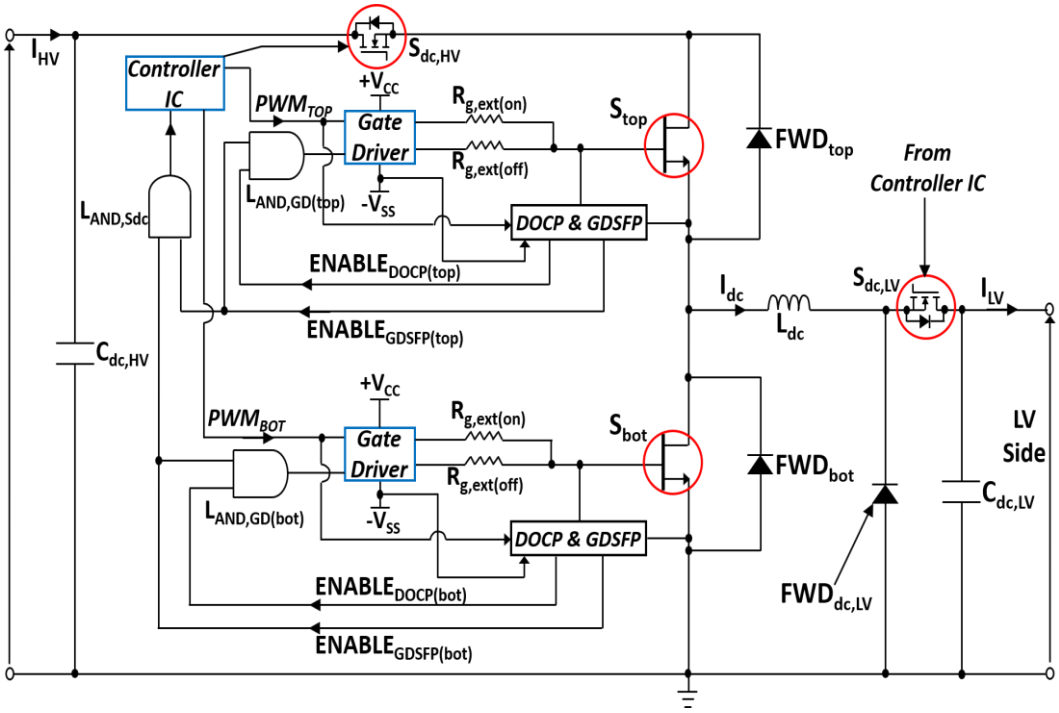



*Figure 5-1: Bidirectional dc-dc converter with DOCP and GDSFP scheme for D-mode GaN power devices*

The components and circuit parameters used for implementing the DOCP and 2nd prototype GDSFP circuits are enlisted in Table 5-1 and Table 5-2, respectively. Same components were used as in Chapter 4 but the isolated DC voltage regulators with lower input-to-output capacitances ($C_{IO}$) were selected to minimise the possibility of conducted EMI between the control logic side and power circuit side that may disturb the control circuit operation. Also, the circuit layout was designed so that the input and output sides are far apart from each other for the same reason. In addition, a blanking capacitance ($C_{blank}$) of 100 pF was used instead of 200 pF for the DOCP implementation so that the blanking time is reduced and hence maximum time taken to remove the short-circuit is shortened for faster circuit response.

| Components | Part Number |
|---|---|
| $D_{disc,desat}$ | US1AFA |
| $D_{desat,sense}$ | F30 |
| Gate Driver IC | Si8271BB-IS |
| $G_{opt,desat}$ | ACPL-H61L |
| $L_{comp,desat}$ | LM311P |
| $M_{comp,desat}$ and $M_{disc,desat}$ | IPD220N06L3 |
| $M_{inv,p}$ and $M_{inv,n}$ | IRFR5305PbF and IRFR3806PbF |
| $+V_{CC1}$ regulator | ITQ2405SA |
| $+V_{CC}$ and $+/-V_{SS}$ regulators | R05P215D |

(a)

| Parameters | Values |
|---|---|
| $C_{block}$ | 100 pF |
| $R_{comp,desat}$, $R_{desat1}$ and $R_{desat2}$ | 500 Ω |
| $R_{g,ext(off)}$ | 15 Ω |
| $R_{inv,p}$ and $R_{inv,n}$ | 3.9 Ω and 40 Ω |
| $R_{ref1}$ and $R_{ref2}$ | 10 Ω and 487 Ω |
| $+V_{cc}$ | +2.5 V |
| $+/-V_{SS}$ | +/- 15 V |

(b)

*Table 5-1: DOCP (a) components and (b) circuit parameters used for the dc-dc power converter hardware demonstration*

| Components | Part Number |
|---|---|
| $D_{ch}$ and $D_{disc}$ | US1AFA |
| $FWD_{dc,LV}$ | GC20MPS12-247 |
| $L_{comp}$ | LM311P |
| Gate Driver IC | Si8271BB-IS |
| $G_{opt,gsf}$ | ACPL-H61L |
| $L_{AND,GD}$ | SN74LV08A |
| $L_{AND,Sdc}$ | SN74LVC1G11 |
| $M_{ch}$ | IPD220N06L3 |
| $S_{dc,link}$ Gate Driver IC | IX3120G |
| $S_{dc,HV}$ | C2M0045170D |

| | |
|---|---|
| $S_{dc,LV}$ | C3M0016120D |
| $+V_{CC,in}$ / $+V_{opt}$ regulator | R05P205S |
| $+/-V_{SS2}$ regulator | R05P15D |

(a)

| Parameters | Values |
|---|---|
| $C_{res}$ | 560 µF (nominal) |
| $R_{comp,out}$ | 1 kΩ |
| $R_{gsf,ref1}$ and $R_{gsf,ref2}$ | 750 Ω and 1.5 kΩ |
| $R_{out,en}$ | 402 Ω |
| $R_{opt,in}$ | 1000 Ω |
| $V_{dc}$ | 900 V |
| $+V_{opt}$ | +5 V |
| $+/- V_{ss}$ and $+/- V_{ss2}$ | +/-15 V |

(b)

*Table 5-2: 2nd prototype GDSFP (a) components and (b) circuit parameters used for power converter hardware demonstration*

## *5.2. Principles of dc-to-dc converter operation*

As shown in the circuit schematic in Figure 5-2, the step-down (buck) dc-to-dc converter circuit consists of two switching devices and passive components including an inductor ($L_{dc}$) and an output capacitor ($C_{out}$) that stores energy in the form of magnetic flux and electric charge, respectively, and thus deliver constant dc current and voltage during normal operation. The waveforms of the step-down converter during steady-state operation are illustrated in Figure 5-3. From the inductor current ($I_{Ldc}$) waveform, it can be observed that a certain amount of ripple exists due to the switching events that cause change in voltage drop present across the inductor in each switching cycle. The voltage across the inductor ($V_{Ldc}$) when the main switch (SW) is turned on and off can be mathematically expressed as the following:

$$V_{Ldc(on)} = \begin{cases} V_{HV,in} - V_{LV,DC} \; when \; SW \; is \; 'on' \\ -V_{LV,out} \; when \; SW \; is \; 'off' \end{cases} \quad \ldots(5\text{-}1)$$

Where $V_{HV,in}$ = input voltage on HV side and $V_{LV,out}$ = output voltage on LV side.

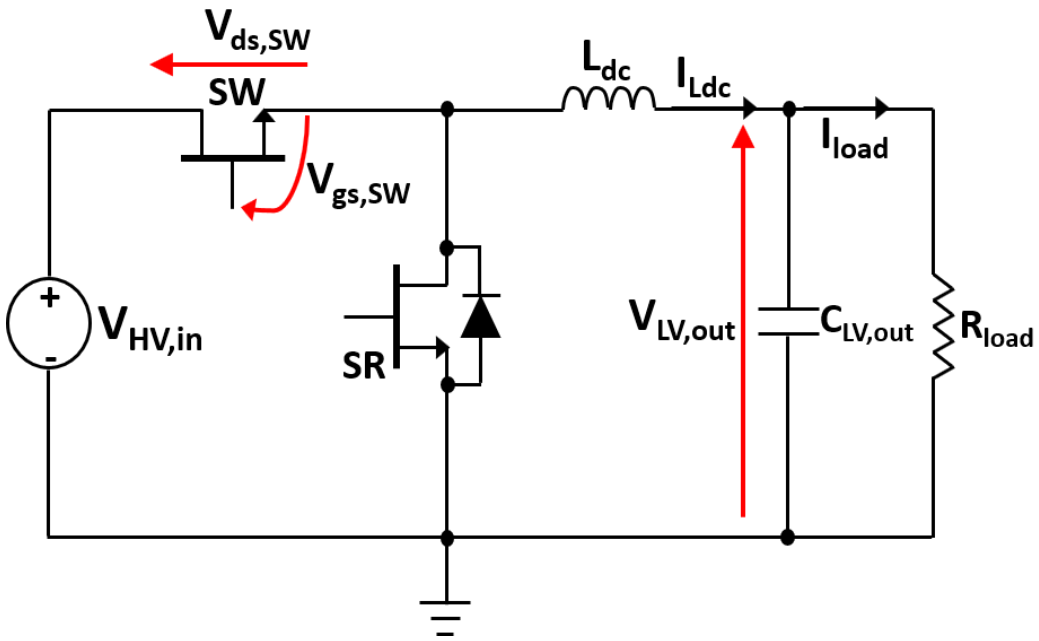



*Figure 5-2: Synchronous step-down DC-to-DC converter*

As a result, the inductor current ripple ($\Delta I_{dc}$) during steady-state operation can be expressed as:

$$|\Delta I_{dc}| = \frac{D \cdot T \cdot \left(V_{HV,in} - V_{LV,DC}\right)}{L_{dc}} = \frac{(1-D) \cdot T \cdot V_{LV,DC}}{L_{dc}} \quad \ldots(5\text{-}2)$$

Where D = duty cycle and T = switching period.

$$\therefore L_{dc(min)} = \frac{D \cdot T \cdot \left(V_{HV,in} - V_{LV,DC}\right)}{|\Delta I_{dc}|_{max}} \quad \ldots(5\text{-}3)$$

$$\therefore V_{LV,DC} = D \cdot V_{HV,in} \quad \ldots(5\text{-}4)$$

In addition, a ripple in the output voltage exists as the ripple current flows through the output capacitor. Assuming that the constant dc current flows through

the output load, the $\Delta V_{dc}$ and thus minimum $C_{out}$ required to keep the $\Delta V_{dc}$ to the design specification can be expressed as:

$$\therefore C_{out(min)} = \frac{\Delta I_{dc}}{8 \cdot \Delta V_{dc(max)}} \cdot T \quad \ldots(5\text{-}5)$$

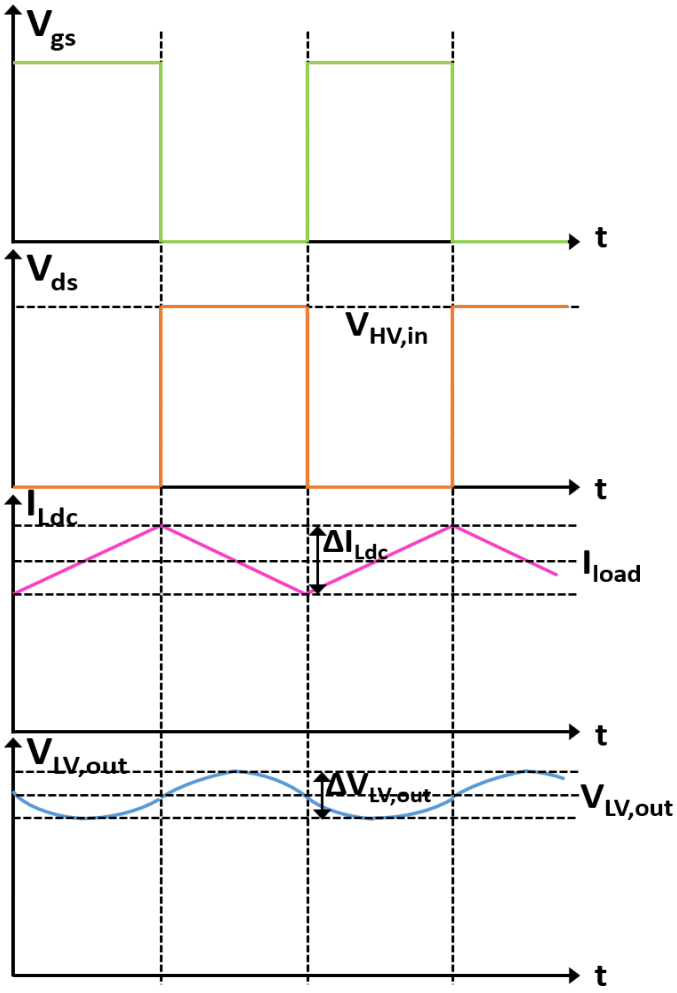



*Figure 5-3: Steady-state voltage and current waveforms in step-down dc-dc converter*

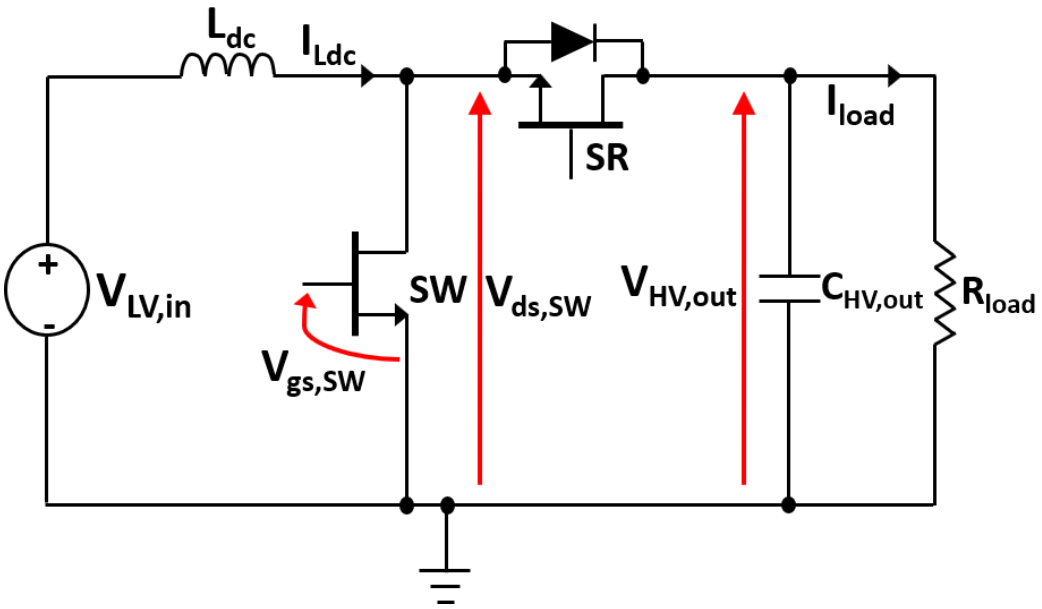



*Figure 5-4: Synchronous step-up dc-dc converter*

The typical waveforms of the step-up (boost) converter during steady-state operation are presented in Figure 5-5. When the SW is in its 'on' state, the energy stored in $L_{dc}$ is increased. When the SW is turned 'off', the $L_{dc}$ will release its energy to the output HV side via synchronous rectifier (SR) or freewheeling diode.

$$V_{Ldc(on)} = \begin{cases} V_{LV,in} \; when \; SW \; is \; 'on' \\ V_{LV,in} - V_{HV,out} \; when \; SW \; is \; 'off' \end{cases} \quad \ldots(5\text{-}6)$$

Hence, the $\Delta I_{dc}$ and $V_{HV,out}$ can be derived as:

$$\therefore |\Delta I_{dc}| = \frac{D \cdot T \cdot V_{LV,DC}}{L_{dc}} = \frac{(1-D) \cdot T \cdot \left(V_{HV,DC} - V_{LV,DC}\right)}{L_{dc}} \quad \ldots(5\text{-}7)$$

$$\therefore V_{HV,DC} = \frac{V_{LV,in}}{1-D} \quad \ldots(5\text{-}8)$$

From equation (5-6) the minimum $L_{dc}$ value required to keep the $\Delta I_{dc}$ within a specific limit can be derived as:

$$\therefore L_{dc(min)} = \frac{D \cdot T \cdot V_{LV,DC}}{|\Delta I_{dc}|_{max}} \quad \ldots(5\text{-}9)$$

When the main switch is 'off', the full load current will flow through the HV-side output capacitor ($C_{out,HV}$), which leads to much larger capacitance value required to keep the output voltage ripple to be low when compared to its LV side counterpart and can be expressed as:

$$\therefore C_{HV,out(min)} = \frac{I_{load} \cdot D \cdot T}{\left|\Delta V_{HV,out}\right|_{max}} = \frac{\left(I_{Ldc,av} - I_{load}\right) \cdot (1 - D) \cdot T}{\left|\Delta V_{HV,out}\right|_{max}} \quad \ldots(5\text{-}10)$$

From which:

$$\therefore I_{Ldc,av} = \frac{I_{HV,dc}}{1-D} \quad \ldots(5\text{-}11)$$

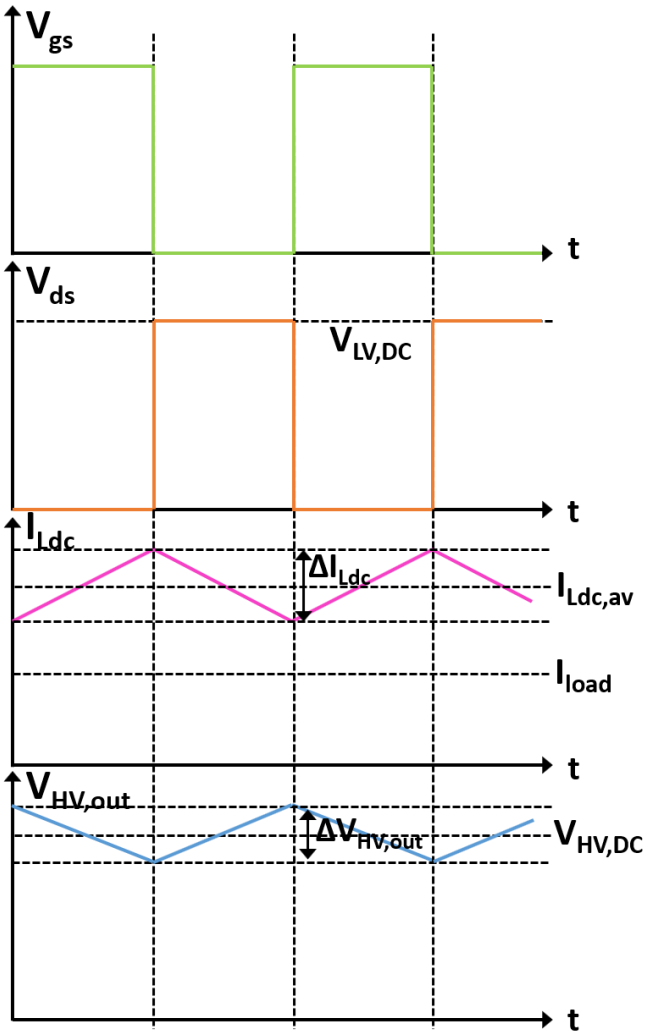



*Figure 5-5: Steady-state voltage and current waveforms in step-up dc-dc converter*

## *5.3. Passive component design and selection*

The converter's design specification parameters are presented in Table 5-3.

| Parameter | Value | Unit |
|---|---|---|
| $\Delta I_{Ldc}$ / $I_{Ldc,av(max)}$ | ± 10 | % |
| $I_{Ldc,av(max)}$ | 5.56 | A |
| $\Delta V_{HV,DC}/V_{HV,DC}$ and $\Delta V_{LV,DC}/V_{LV,DC}$ | ± 1 | % |
| $V_{HV,DC}$ | 900 | V |
| $V_{LV,DC}$ | 500 | V |
| $P_{out}$ (in both directions) | 2.778 | kW |

*Table 5-3: Voltage and current specifications of the GaN converter*

By substituting the parameter values in Table 5-3 to the equations (5-6), (5-10) and (5-11), the minimum $L_{dc}$ and $C_{LV(HV),out}$ values required to meet the current and voltage ripple specifications can be derived and are enlisted in Table 5-4.

| Parameter | Value (Unit) | Part number |
|---|---|---|
| $L_{dc}$ | 4.96 (mH) | T225-52 (core) |
| $C_{LV,out}$ | 1 (µF) x 1 | MKP1848C51012JK2 |
| $C_{HV,out}$ | 1.5 (µF) x 3 | C4AQSBU4150A1XJ |

*Table 5-4: Passive element values and part number used for converter demonstration*

The inductor consists of a magnetic core with multiple number of wires wounded around itself. The basic principle of inductor is that when a current flows through a wire that is wounded around a ferromagnetic core, then a circulatory magnetising force (H) and magnetic field (B) are induced around the wire, which then induces a voltage (commonly referred to as 'back emf') that impedes the change in current. The relationship between B and H can be expressed mathematically as:

$$B = \mu_r \cdot \mu_0 \cdot H \quad \ldots(5\text{-}12)$$

Where $\mu_r$ = relative permeability of the magnetic core and $\mu_0$ = permeability of free space. However, there is a maximum limit to the flux density that can be stored by the magnetic core material without saturating ($B_{sat}$); once B exceeds this value, the core will saturate and thus will not be able to store any more magnetic energy. As a result, the coil will behave as a short circuit, which must be avoided and thus taken into account in the converter design phase.

The inductance (L) value is determined by the geometric and material properties of the magnetic core including cross-sectional area, magnetic flux loop length, saturated magnetic flux and relative permeability. The geometric parameters of the toroidal magnetic core are clearly labelled and illustrated in Figure 5-9. In electromagnetics, the following equation applies:

$$E = N \cdot \frac{d\varphi}{dt} = L \cdot \frac{di}{dt} \quad \ldots(5\text{-}13)$$

Where E = back-emf generated due to the change in magnetic flux, N = number of coil turns and φ = magnetic flux = B*$A_c$. Hence, L can be expressed as:

$$\therefore L = \frac{N \cdot \varphi}{I} \quad \ldots(5\text{-}14)$$

The H is proportional to the product of N and I and can be expressed as:

$$H = \frac{0.4\pi \cdot N \cdot I}{MPL} \quad \ldots(5\text{-}15)$$

Typically, an air-gap is inserted in the iron or ferrite cores to achieve higher saturation flux density. With this, according to [126], the inductance per (number of turns)$^2$ can be expressed as:

$$A_L = \frac{0.4\pi A_c}{l_g + \frac{MPL}{\mu_m}}$$

…(5-16)

Where N = number of winding turns, $A_c$ = magnetic core cross-sectional area, $l_g$ = air gap length, MPL = magnetic path length of the core and $\mu_m$ = absolute permeability of the core material. Hence, L is proportional to $N^2$ and $A_c$.

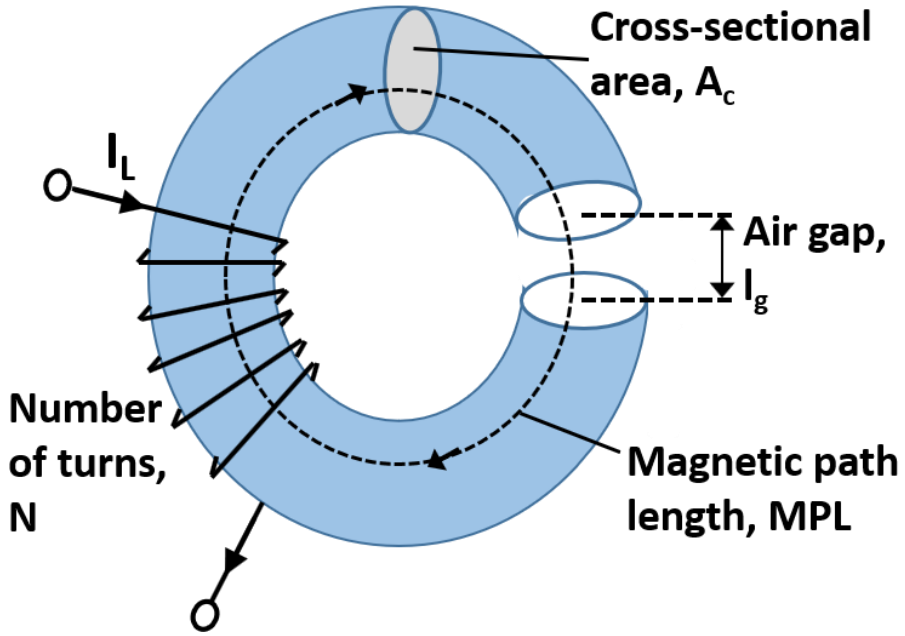



*Figure 5-6: Toroidal magnetic core with its geometric properties*

The core geometry must have sufficient 'window area' to accommodate the several turns and layers of coil turns required to realise a certain inductance value as illustrated in Figure 5-11. Also, it is equally important to ensure that it does not saturate for the amount of current flow through the coils that determines the amount of flux; the saturated flux density is labelled as $B_S$ in Figure 5-10. The maximum current at which the core saturates is given as:

$$I_{L,sat} = \frac{B_S \cdot A_c}{\sqrt{L \cdot A_L}}$$

…(5-17)

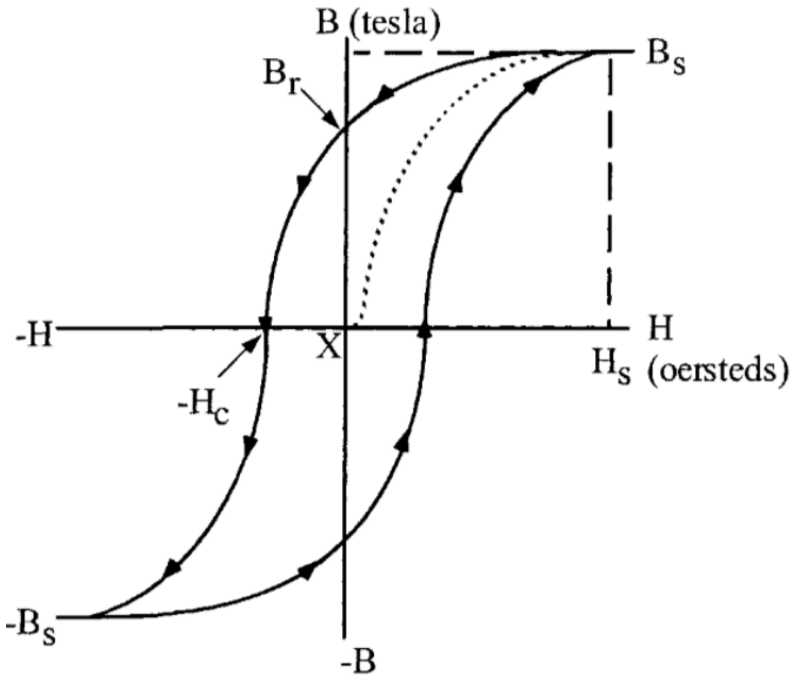



*Figure 5-7: Typical B-H curve of a magnetic material [126]*

For this work, a 5 mH inductor was designed using T225-52 ferrite powder core with distributed air gap and 233 turns of enamel-coated copper wire with a diameter of 1.6 mm mm and general purpose AT4 0.1mm thick PVC tape to provide an insulation barrier between the layer of coils. The core material has a saturation flux density of 1.85T and $A_L$ of 92nH/$N^2$.

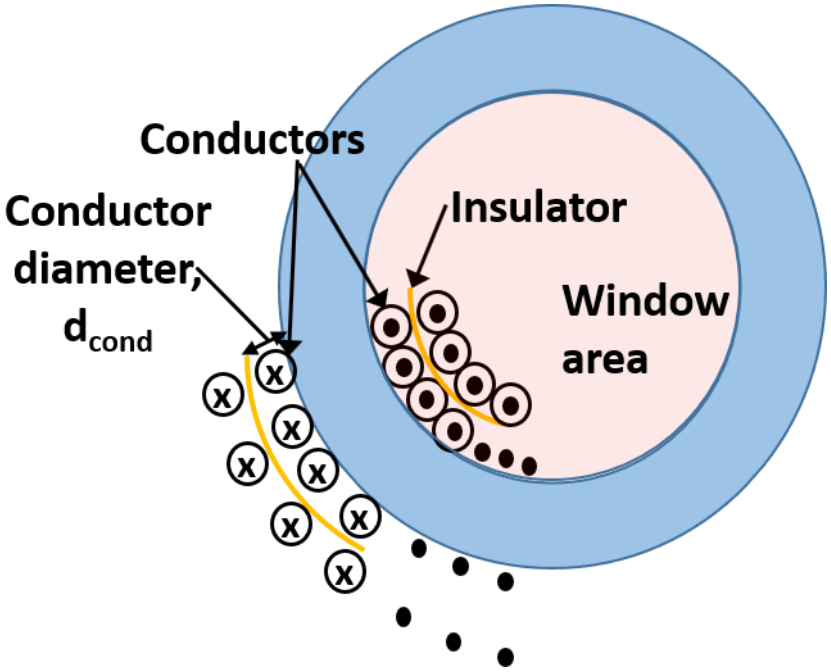



*Figure 5-8: Illustration of magnetic core window area for inductor design*

## *5.4. Heatsink selection*

Due to the switching and on-state conduction events, there will be certain amount of power loss dissipated in the form of heat. Therefore, sufficient means of cooling the device under normal operation must be provided in order to ensure that its junction temperature do not exceed a maximum value (typically $150^0$C), which is limited by the degradation in bond wire reliability due to the intermetallic growth and diffusion at the bond interface that creates brittle and weaker bonds within the packages [127]. In addition, the exterior of the device packages and heatsink surfaces are not completely flat and thus when they are in direct contact to each other, very poor thermal dissipation path is created via air gap between them. In order to prevent this, a thermal interface material (TIM) is required to be placed between them so that they are firmly in contact.

For this work, the PSJ transistors were cooled using two Wakefield-vette OMNI-32 heatsinks and a Sanyo Denki DC fan (9GAX0412P3S0011) that provides maximum airflow of 30 m/s to the heatsink fins and a case-to-ambient thermal resistance of $1^0$C/W for the heatsink. Also, the thermal resistance of the TIM sheet with an adhesive on a single side, Kerafol 86/82K, was provided by the manufacturer to be $0.14^0$C/W. Thus, when the thermal resistance of the PSJ device packaging and TIM is combined, a total $R_{th}$ of $1.894^0$C/W was present in the heat dissipation path. The dc-link switches and FWDs were mounted onto natural convection cooled heatsink with a thermal resistance of $18.4^0$C/W using Wacker Silicone heatsink paste P 12.

## *5.5. Converter power loss calculation*

The switching power loss of a device is proportional to the PWM switching frequency ($f_{sw}$) and can be expressed as:

$$P_{sw,total} = \left(E_{on} + E_{off}\right) \cdot f_{sw} \quad \ldots(5\text{-}18)$$

The on-state conduction loss for a given duty cycle D, average current of $I_{Ldc}$ and current ripple $\Delta I_L$ can be expressed as [128]:

$$P_{on} = \left({I_{Ldc,av}}^2 + \frac{(\Delta I_L)^2}{12}\right) \cdot R_{ds,on} \cdot D \quad \ldots(5\text{-}19)$$

As the inductor current will flow through the antiparallel freewheeling diode (FWD) when the SW is off, the power is dissipated in the FWD or SR switch. Without the presence of SR switch, the power loss in FWD would simply be

$$P_{FWD,on} = V_f \cdot I_{Ldc,av} \cdot (1 - D) \quad \ldots(5\text{-}20)$$

Where $V_f$ = forward knee voltage drop of the diode. Assuming that SR switch is present and dead time is extremely short compared to the switching period, the conduction loss in SR can be obtained as:

$$P_{SR,on} = \left(I_{Ldc,av}{}^2 + \frac{(\Delta I_L)^2}{12}\right) \cdot R_{ds,on} \cdot (1 - D) \quad \ldots(5\text{-}21)$$

In addition, the DC $I^2R$ losses in the inductor winding must also be considered as multiple number of turns leads to a large series resistance and thus power loss:

$$P_{I^2R,Ldc} = \frac{\rho \cdot l_{tot}}{A_c} \quad \ldots(5\text{-}22)$$

Where $\rho$ = resistivity of the conductor = 1.72 x $10^{-8}$ Ωm, $l_{tot}$ = total length of the conductor and $A_c$ = cross-sectional area of the conductor. From Figure 5-10, the $l_{tot}$ can be mathematically expressed as:

$$l_{tot} = 2\sum_{i=1}^{n}\left(N_i \cdot \left(t_c + t_d + 4(n-1) \cdot (t_{ins} + d_{cond})\right)\right) \quad \ldots(5\text{-}23)$$

Where $N_i$ = number of conductor turns on i-th coil layer and for the toroidal core can be expressed as:

$$N_i \leq \frac{(ID - d_{cond} - 2(i-1)\cdot(d_{cond} + t_{ins}))\times\pi}{d_{cond}} \quad \ldots(5\text{-}24)$$

However, it must be noted that $E_{on}$, $E_{off}$ and $R_{ds,on}$ are dependent upon the device junction temperature ($T_j$). Therefore, in order to take the effect of change in $T_j$ to the power loss into account, an electrothermal power loss calculation model was built using Simulink as illustrated by the block diagram in Figure 5-9. The total thermal resistance present in the power dissipation path will govern the $T_j$ rise of the switching device during steady-state operation. Hence, a relatively accurate estimation of converter's efficiency can be obtained when compared to estimation using $E_{on}$, $E_{off}$ and $R_{ds,on}$ at a fixed temperature value.

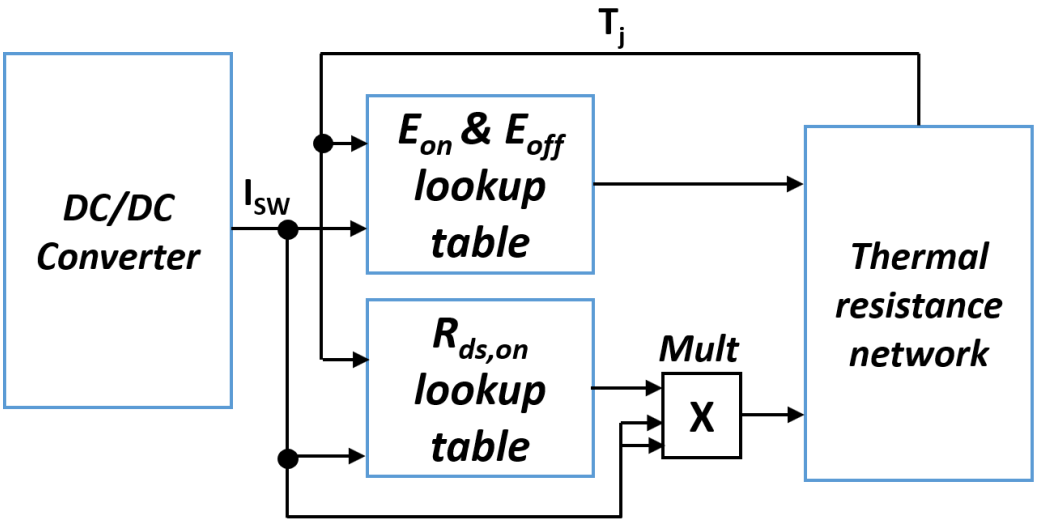



*Figure 5-9: Electrothermal switching device power loss calculation model*

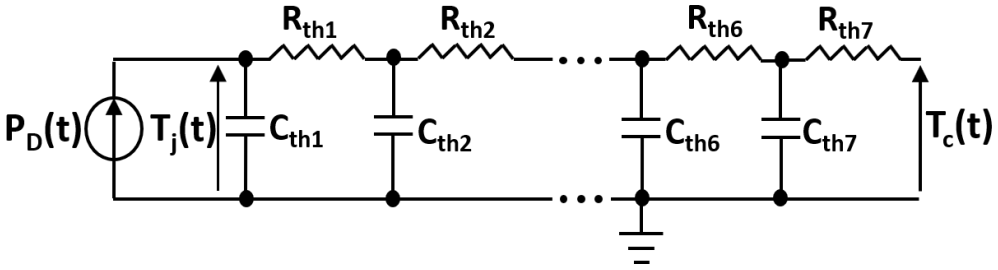



*Figure 5-10: Cauer thermal impedance network diagram*

The R and C values of the Cauer network were fitted using the thermal properties of each individual material layer and the conventional approach that assumes heat spreading angle of $45^0$ that leads to a slight increase in the area of heat spreading; the fitted values are presented in Table 5-5. The transient thermal response of Cauer network with the fitted values have shown excellent agreement with its FEA counterpart as shown in Figure 5-11.

| Cauer network parameter | Value |
|---|---|
| $C_{th1}$ | 0.01078 |
| $C_{th2}$ | 0.00478 |
| $C_{th3}$ | 0.05325 |
| $C_{th4}$ | 0.00651 |
| $C_{th5}$ | 0.0273 |
| $C_{th6}$ | 0.00772 |
| $C_{th7}$ | 0.07764 |
| $R_{th1}$ | 0.2218 |
| $R_{th2}$ | 0.016 |
| $R_{th3}$ | 0.045 |
| $R_{th4}$ | 0.15 |
| $R_{th5}$ | 0.3077 |
| $R_{th6}$ | 0.004 |
| $R_{th7}$ | 0.017 |

*Table 5-5: Fitted Cauer network parameters of Kyocera KO-PWR121297 packaging*

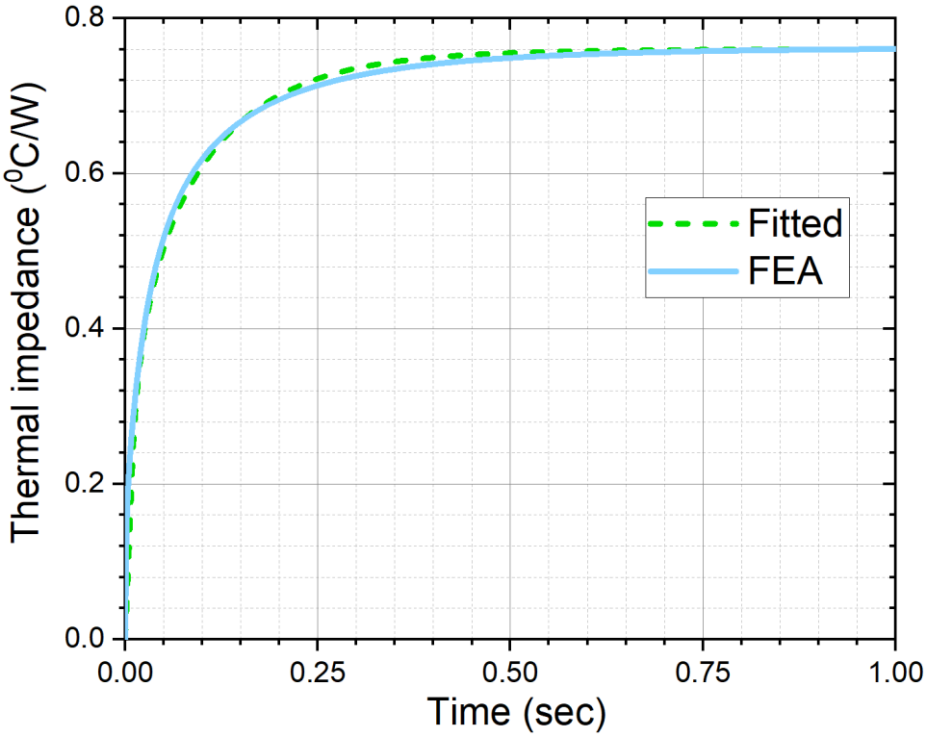



*Figure 5-11: Comparision of transient thermal impedance curves of Kyocera KO-PWR121297 packaging obtained via ANSYS FEA and fitted RC values in Cauer network*

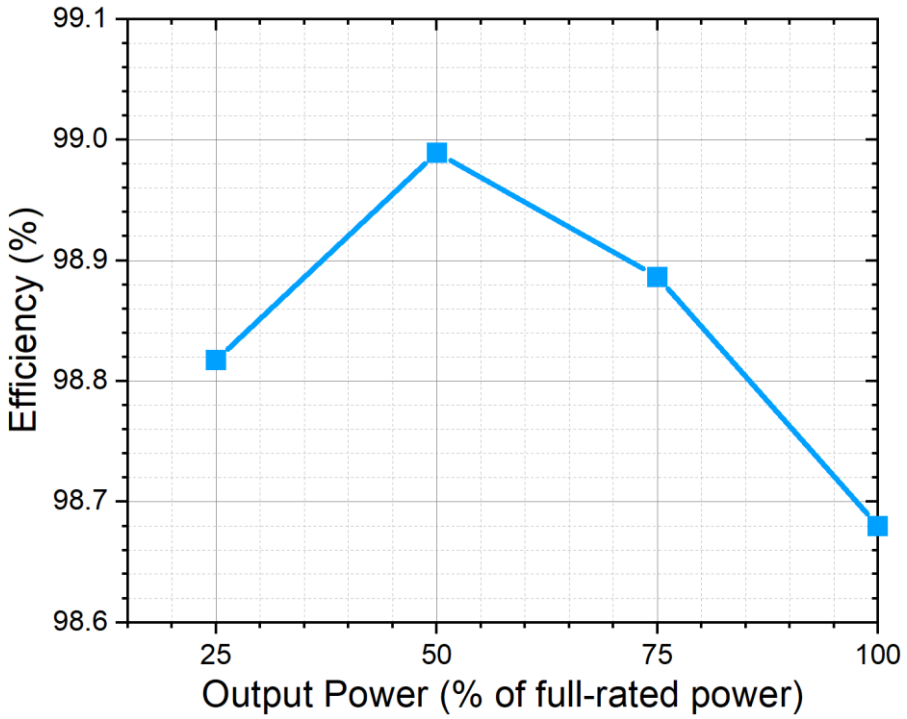
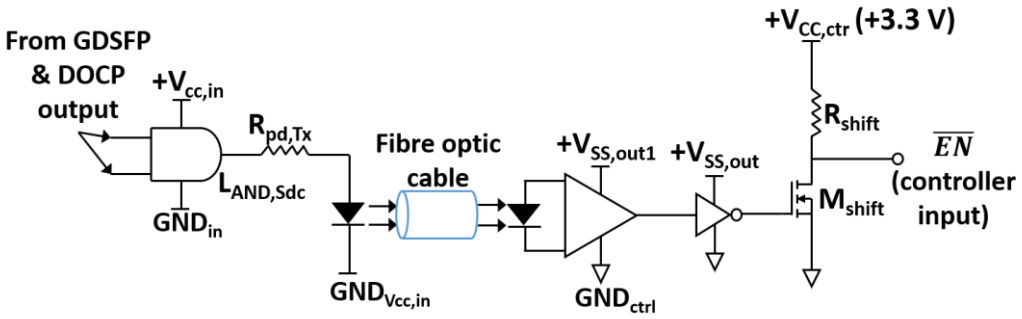


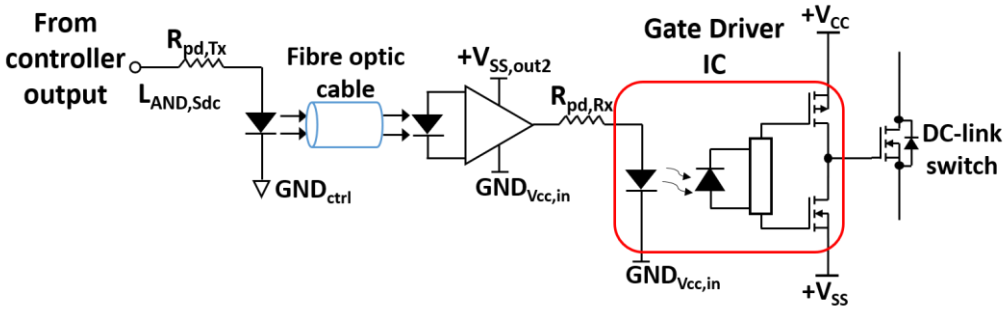

*Figure 5-12: D-mode GaN power converter efficiency vs. Output load power curve*

## *5.6. EMI issues and possible mitigations*

The converter was running in a step-down configuration so that the LV side becomes the output. The LV output was connected to a 180 Ω load resistor that is equivalent to 50% load output. The interfacing circuits between the controller side and converter's input side in one way and the other are presented in Figure 5-13(a) and (b). The controller IC was galvanically isolated from the converter control circuit so that noise coupling to the controller is minimised and the end user's safety is guaranteed.




(a)




(b)

*Figure 5-13: (a) Converter input side to controller and (b) Controller to the converter input side interface circuit schematic*

Nevertheless, the EMI noise was coupled onto the EN input during the turn-on transient of the PSJ transistor as presented and labelled in Figure 5-16. This common mode dV/dt induced noise was coupled through the input-to-output capacitance of the isolation barrier in the gate drivers, optocouplers and isolated dc voltage regulators as illustrated in Figure 5-15 [119]. The magnitude of the noise was pronounced with an increase in the dc-link voltage input and have triggered the $\overline{EN}$ input to be in unknown logic state or logic HIGH and thus falsely toggled the controller to command $S_{dc,link(HV)}$ and $S_{dc,link(LV)}$ to be turned off to halt the converter operation. This occurred most likely because the ground of the input side was tied to the same ground point for $+V_{cc,in}$ (labelled as $GND_{Vcc,in}$ in Figure 5-13) that was susceptible to dV/dt coupled noise via PCB FR4 material and parasitic I/O capacitances of the gate drive components and thus EMI current conducted.

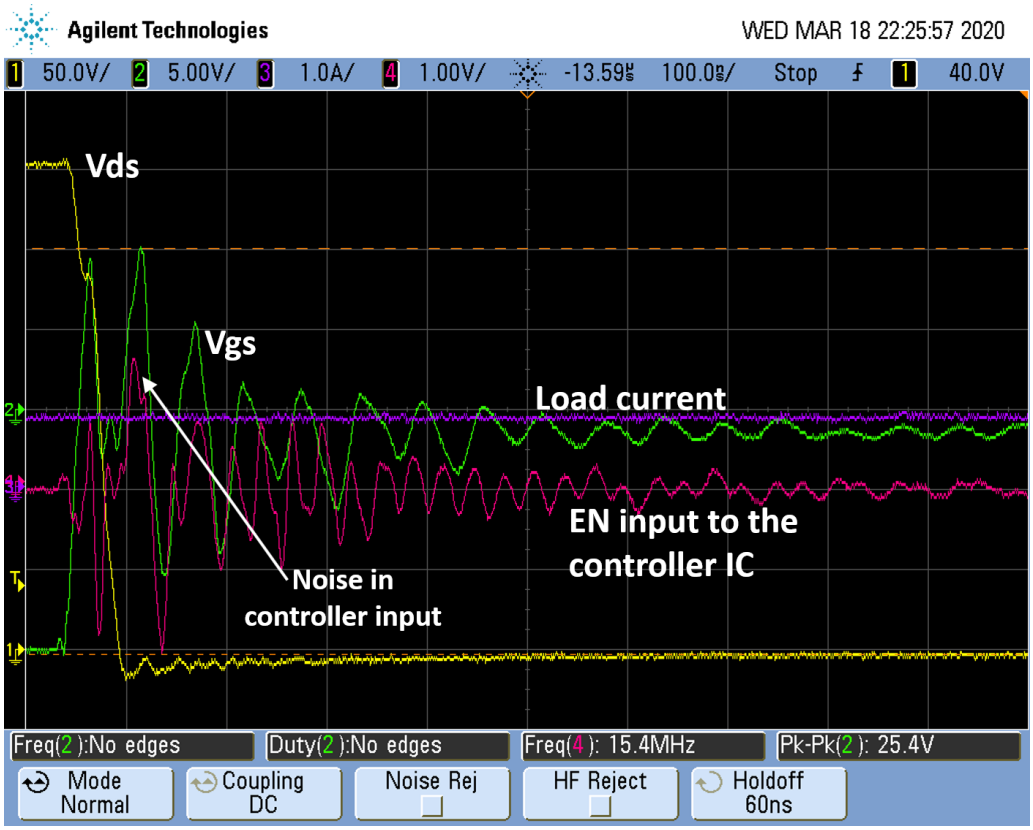



*Figure 5-14: Coupled dv/dt noise from the power converter to the controller EN input at $V_{HV,DC}$ = 300V*

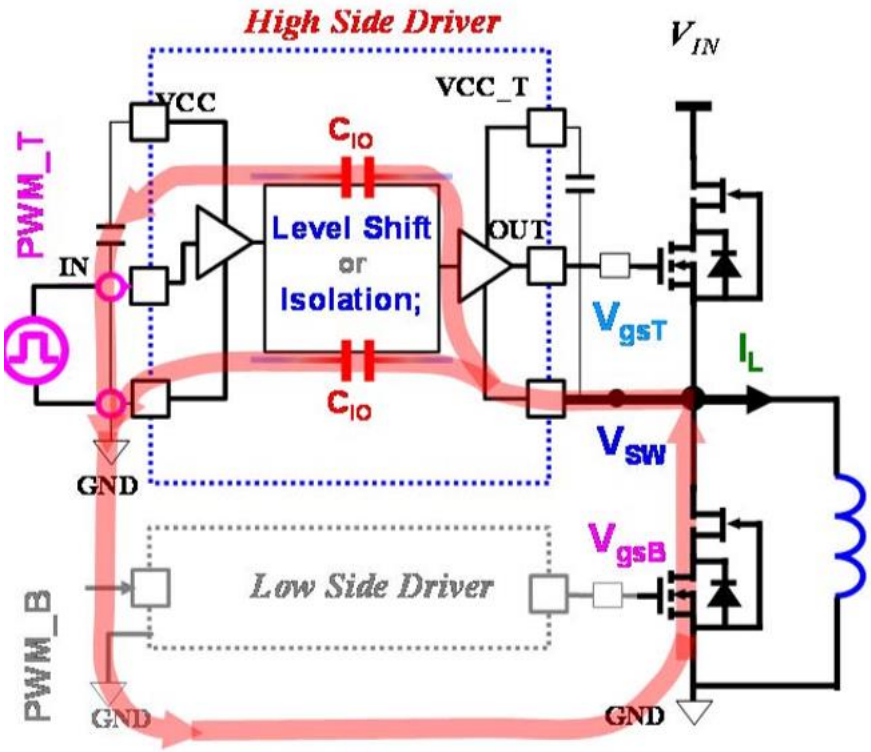



*Figure 5-15: Common-mode dV/dt induced noise path in a half-bridge circuit [129]*

This problem may be mitigated by isolating the ground reference of the input side of IX3120G from the $+V_{cc,in}$ ground ($GND_{Vcc,in}$) so that no EMI is conducted through the input side of IX3120G. Also, differential and/or common-mode filters with a sufficiently low cutoff frequency (in kHz range) may be added to the AND gate output and controller input in Figure 5-13 to minimise the noise magnitude. Another possible solution is to modify the controller's FSM configuration. The controller's input stage can be modified so that the controller holds the previous $\overline{EN}$ input during the turn-on transient of the power device and starts to take the $\overline{EN}$ input samples after a certain length of 'blanking time' as presented in Figure 5-13. By this way, the controller will not take the noisy signal at the transient edge that causes false triggering of controller output.

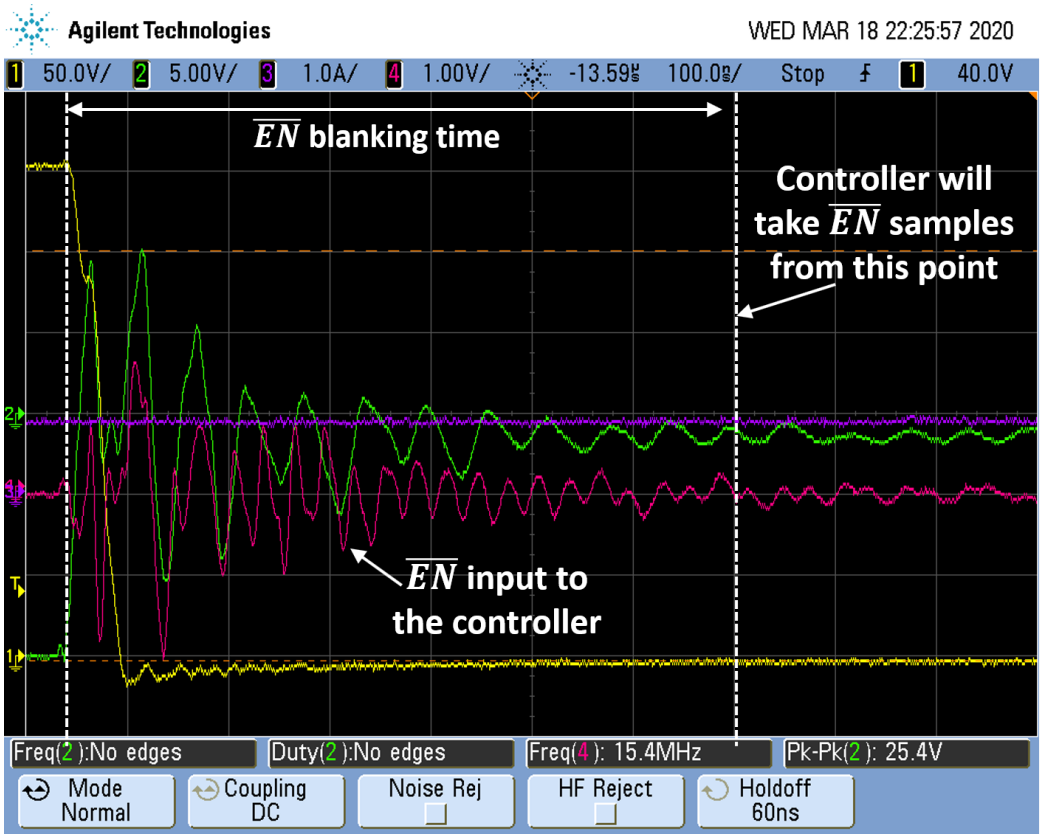



*Figure 5-16: Illustration of EN blanking time proposal for EMI mitigation*

Moreover, further work in the filter inductor design would be required. In particular, the capacitances are present between each winding and are effectively in parallel to the inductor winding as shown in Figure 5-17. These LC components would give rise to a 'self-resonant frequency' at which the impedance of the inductor reaches its maximum value and starts to decrease as frequency rises. At this particular frequency value, its impedance is limited only via finite equivalent series resistance (ESR) of its windings. As the frequency increases, the impedance of $C_{winding}$ would become dominant over its inductive counterpart and hence the inductor behaves as a capacitor [130]. Hence, the layout of the winding must be altered so that $C_{winding}$ is minimized.

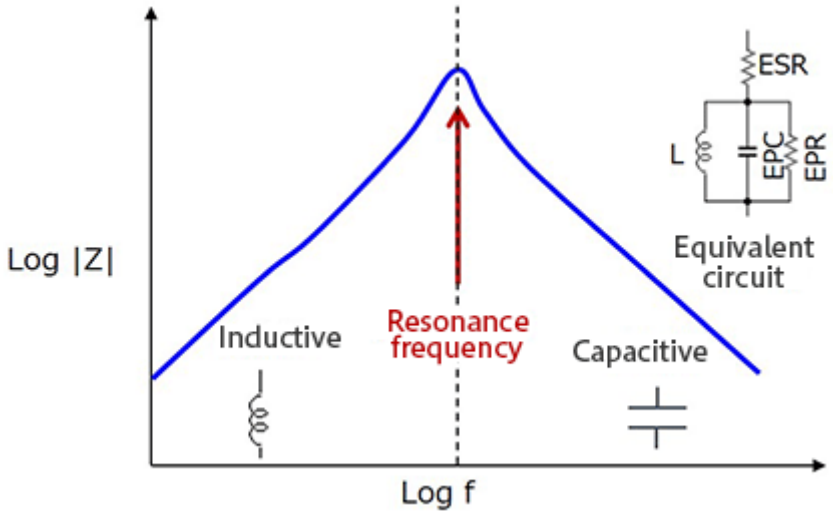



*Figure 5-17: Impedance vs. frequency characteristics of an inductor and its equivalent circuit diagram [130]*

## *5.7. Behavioural model of the large-area PSJ transistor*

### *5.7.1. Static I-V characteristics*

Despite the EMI issue that hindered the practical demonstration of the GaN converter, its fail-safe operation can be verified using a SPICE simulation. To achieve this, a behavioural SPICE model of the large-area PSJ device was created

based on its static I-V and C-V characteristics that were extracted in Chapter 3. The behavioural PSpice macro model of the PSJ-FET is presented in Figure 5-18. The model consists of non-linear terminal capacitances ($C_{gs}$, $C_{gd}$ and $C_{ds}$) that varies with the gate and/or drain biases, internal channel current modelled as a non-linear current source ($I_{ch}$) and parasitic inductances present in gate ($L_g$), drain ($L_d$) and source ($L_s$). The $I_{ch}$ was modelled as a function of $V_{gs}$ and $V_{ds}$ using the equation based on Angelov I-V model in [131], which is presented as the following:

$$I_{ch} = I_{pkth} \cdot (P_{th1} \cdot e^{\alpha_{th1} \cdot T_j} + P_{th2} \cdot e^{\alpha_{th2} \cdot T_j}) \cdot \left(1 + M_{ipk}(V_{ds}, V_{gs}) \cdot \tanh\left(\Psi(V_{ds}, V_{gs})\right)\right) \cdot \tanh(\alpha(V_{ds}, V_{gs}) \cdot V_{ds}) \quad \ldots(5\text{-}25)$$

Where:

$$M_{ipk}(V_{ds}, V_{gs}) = 1 + 0.5 \cdot (M_{ipkb}(V_{ds}) - 1) \cdot (1 + tanh(\varphi_m)) \quad \ldots(5\text{-}26)$$

$$\varphi_m = Q_m(V_{ds}) \cdot (V_{gs} - V_{gsm}) \quad \ldots(5\text{-}27)$$

$$Q_m(V_{ds}) = P_{Qm0} \cdot tanh\left(\alpha_{Qm0}(V_{ds} + \beta_{Qm0})\right) + P_{Qm1} \cdot tanh\left(\alpha_{Qm1}(V_{ds} + \beta_{Qm1})\right) + P_{Q2} \cdot tanh\left(\alpha_{Qm2}(V_{ds} + \beta_{Qm2})\right) + P_{Qmo} \quad \ldots(5\text{-}28)$$

$$\Psi(V_{ds}, V_{gs}) = P_1(V_{ds}) \cdot (V_{gs} - V_{pk1}) + P_2 \cdot (V_{gs} - V_{pk1})^2 + P_3 \cdot (V_{gs} - V_{pk1})^3 \quad \ldots(5\text{-}29)$$

$$P_1(V_{ds}) = P_{1o} + P_{10} \cdot tanh(\alpha_{P10} \cdot (V_{ds} + \beta_{P10})) + P_{11} \cdot tanh(\alpha_{P11} \cdot (V_{ds} + \beta_{P11})) + P_{12} \cdot tanh(\alpha_{P12} \cdot (V_{ds} + \beta_{P12})) \quad \ldots(5\text{-}30)$$

$$M_{ipkb}(V_{ds}) = (P_{Mo} + P_{M0} \cdot tanh(\alpha_{M0} \cdot (V_{ds} + a_0)) + P_{M2} \cdot {V_{ds}}^2 + P_{M3} \cdot {V_{ds}}^3) + P_{Mo}$$

…(5-31)

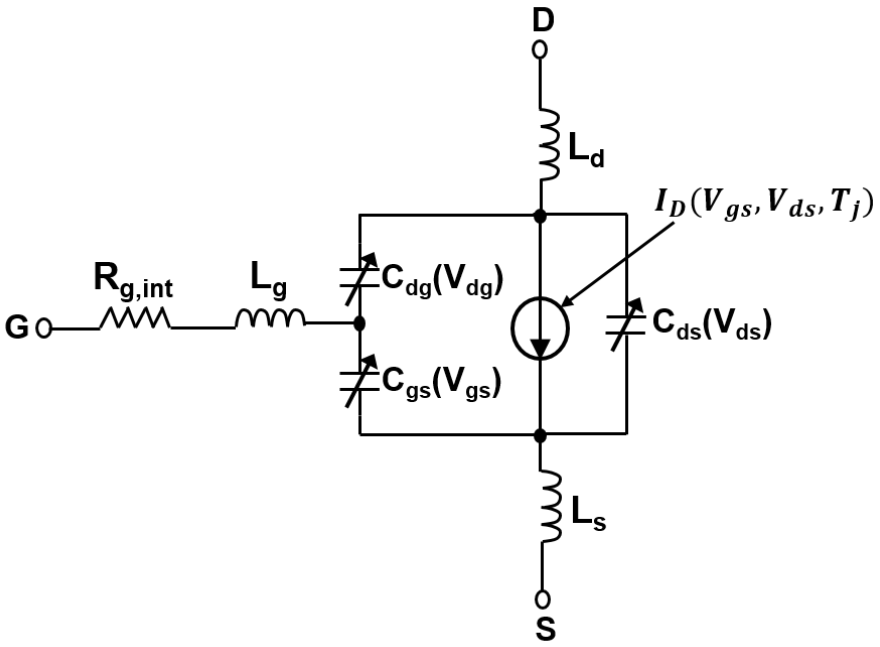



*Figure 5-18: Behavioural SPICE model of a 3-terminal device*

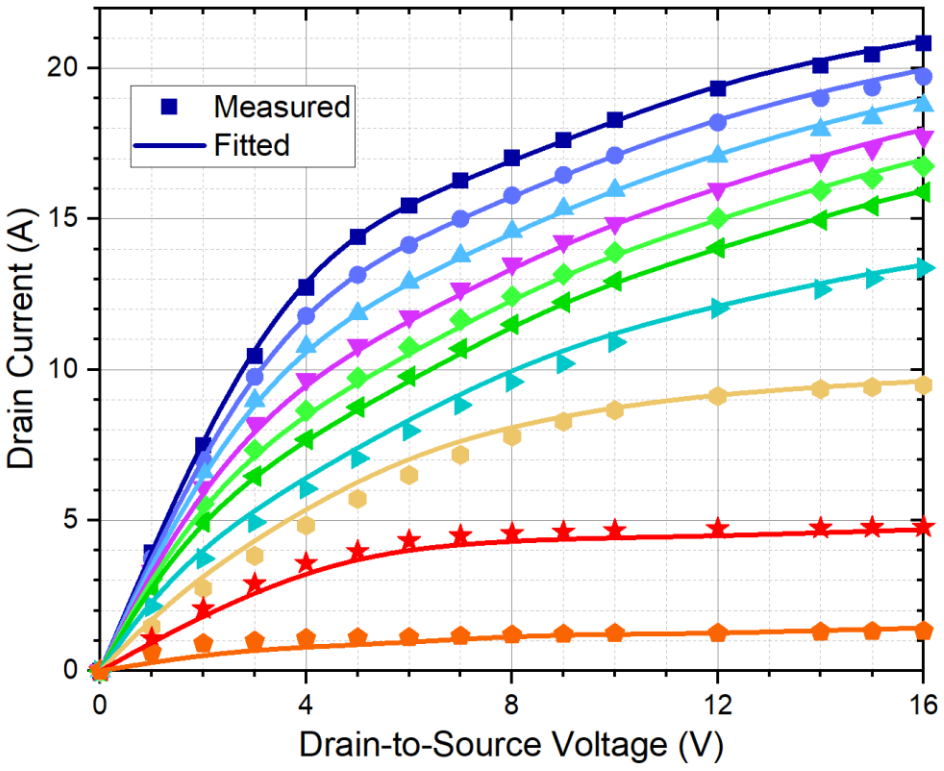
The values of the fitting parameters in equations (5-25) to (5-31) were extracted using the MATLAB's curve fitting tool. The temperature-related parameters ($P_{th1}$, $P_{th2}$, $\alpha_{th1}$ and $\alpha_{th2}$) are marked with the suffix 'th'. The term $M_{ipk}$ ($V_{ds}$, $V_{gs}$) is the hyperbolic tangent-based multiplication factor of the drain current and the term $\varphi_m$ controls the shape of the $M_{ipk}$ curve. The extracted fitting parameter symbols and their values are enlisted in Table 5-6.

| Parameters | Values |
|---|---|
| $\alpha_{P10}$ | 0.1752 |
| $\alpha_{P11}$ | 0.153 |
| $\alpha_{P12}$ | 0.1313 |
| $\alpha_{Qm0}$ | 0.1109 |
| $\alpha_{Qm1}$ | 0.1618 |

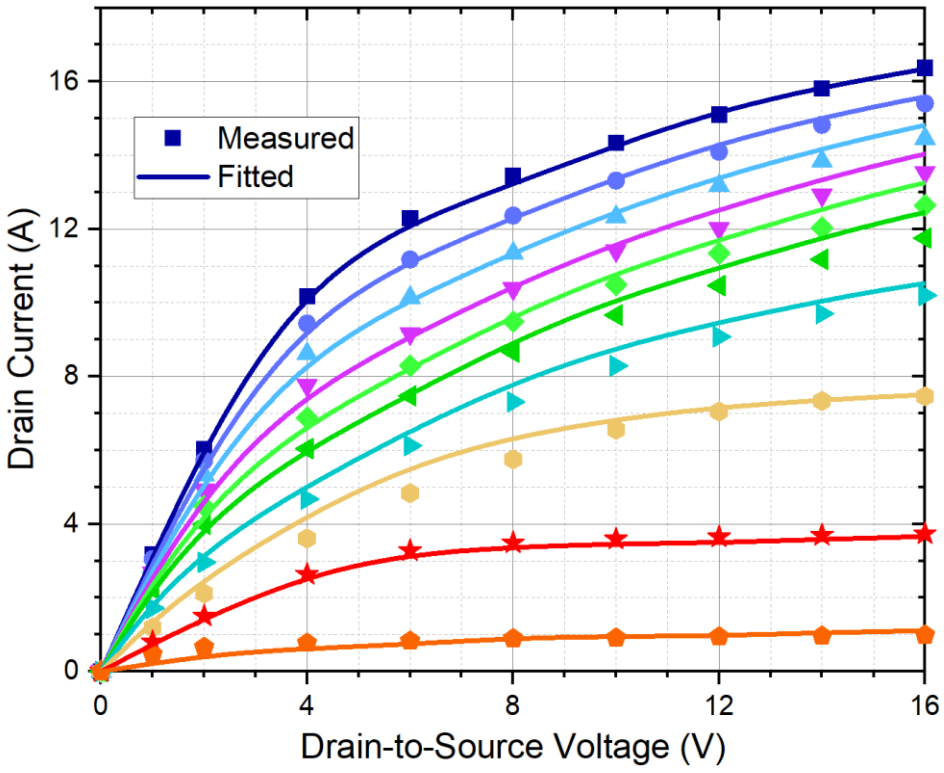
| | |
|---|---|
| $\alpha_{Qm2}$ | 0.2131 |
| $\alpha_{th1}$ | -0.02417 |
| $\alpha_{th2}$ | -0.002466 |
| $\beta_{P10}$ | -8.52 |
| $\beta_{P11}$ | -7.752 |
| $\beta_{P12}$ | -6.488 |
| $\beta_{Qm0}$ | -6.975 |
| $\beta_{Qm1}$ | -9.631 |
| $\beta_{Qm2}$ | -10.03 |
| $P_{1o}$ | -0.267 |
| $P_{10}$ | 14.65 |
| $P_{11}$ | -32.47 |
| $P_{12}$ | 18.76 |
| $P_{Mo}$ | 6.4036 |
| $P_{M0}$ | 0.4324 |
| $P_{M1}$ | -2.566 |
| $P_2$ | 0.01653 |
| $P_3$ | 0.0008023 |
| $P_{Qmo}$ | -0.0647 |
| $P_{Qm0}$ | 2.48 |
| $P_{Qm1}$ | -3.616 |
| $P_{Qm2}$ | 1.508 |
| $P_{th1}$ | 0.7389 |
| $P_{th2}$ | 0.634 |
| $V_{gse}$ | 1.836 |

*Table 5-6: I-V characteristic curve fitting parameter values for the large-area PSJ-FET*

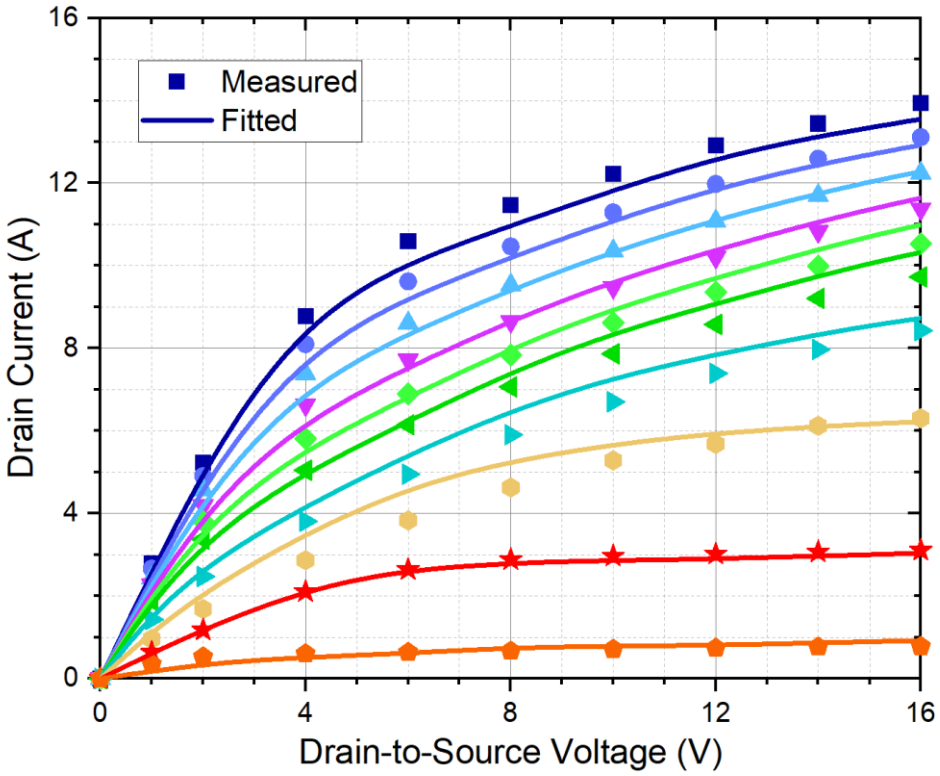
The fitted I-V curve shows an excellent agreement with the average I-V characteristic data extracted from the curve tracer at temperatures up to $150^0$C as shown in Figure 5-17(a)~(f) and Figure 5-18.


Measured
Fitted
Drain Current (A)
Drain-to-Source Voltage (V)
0
5
10
15
20
0
4
8
12
16

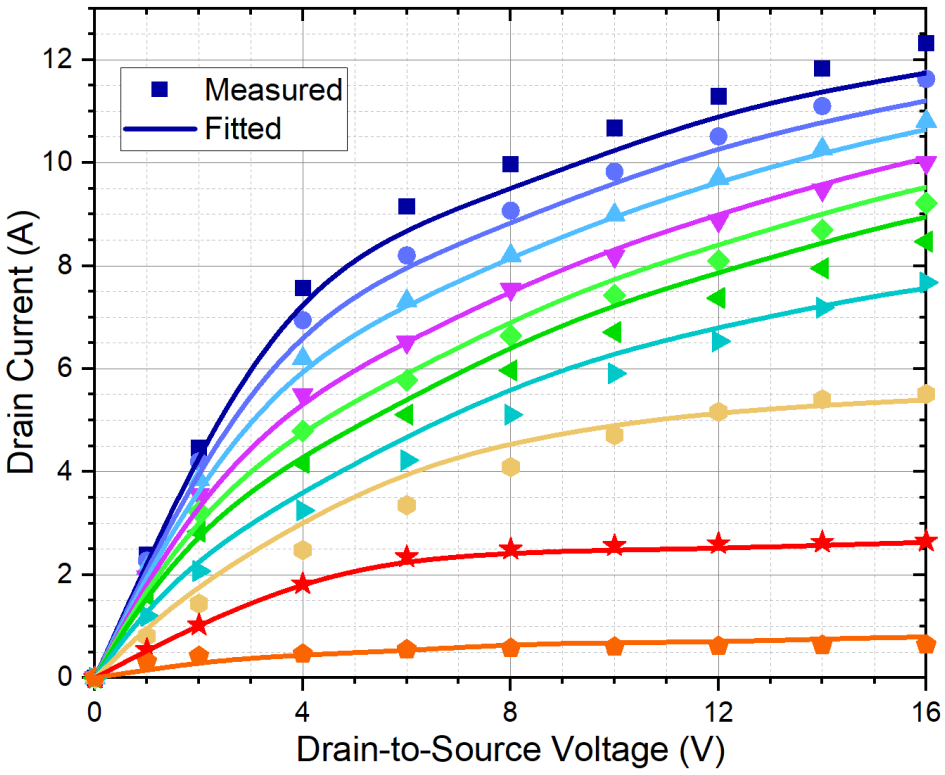
(a)


Measured
Fitted
Drain Current (A)
Drain-to-Source Voltage (V)
0
4
8
12
16
0
4
8
12
16

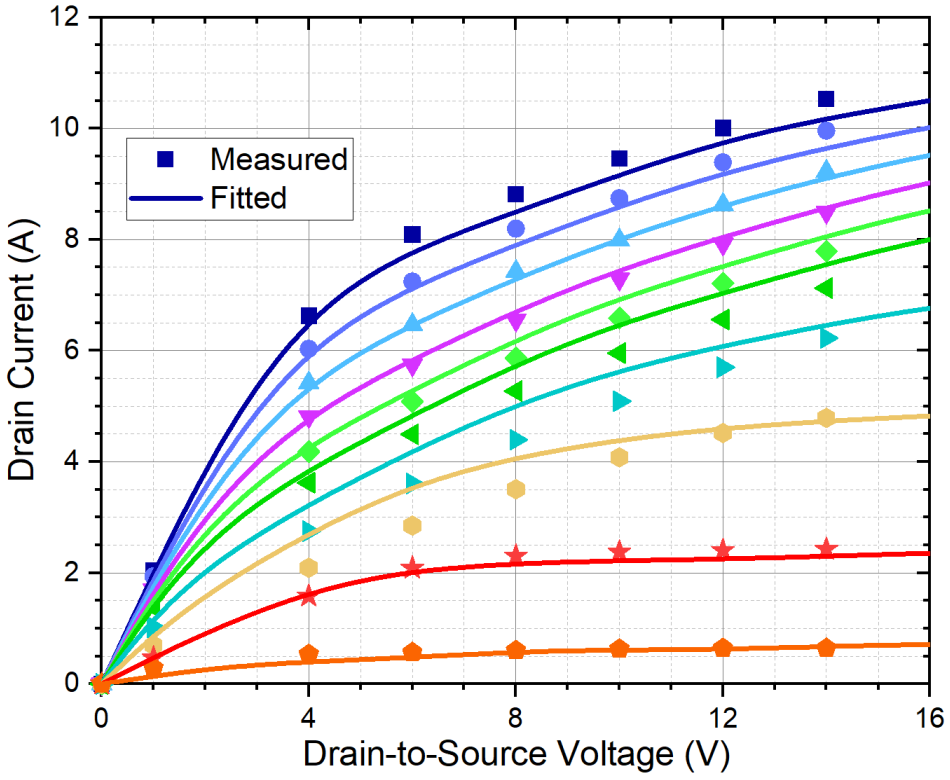
(b)


Measured
Fitted
Drain Current (A)
Drain-to-Source Voltage (V)
0
4
8
12
16

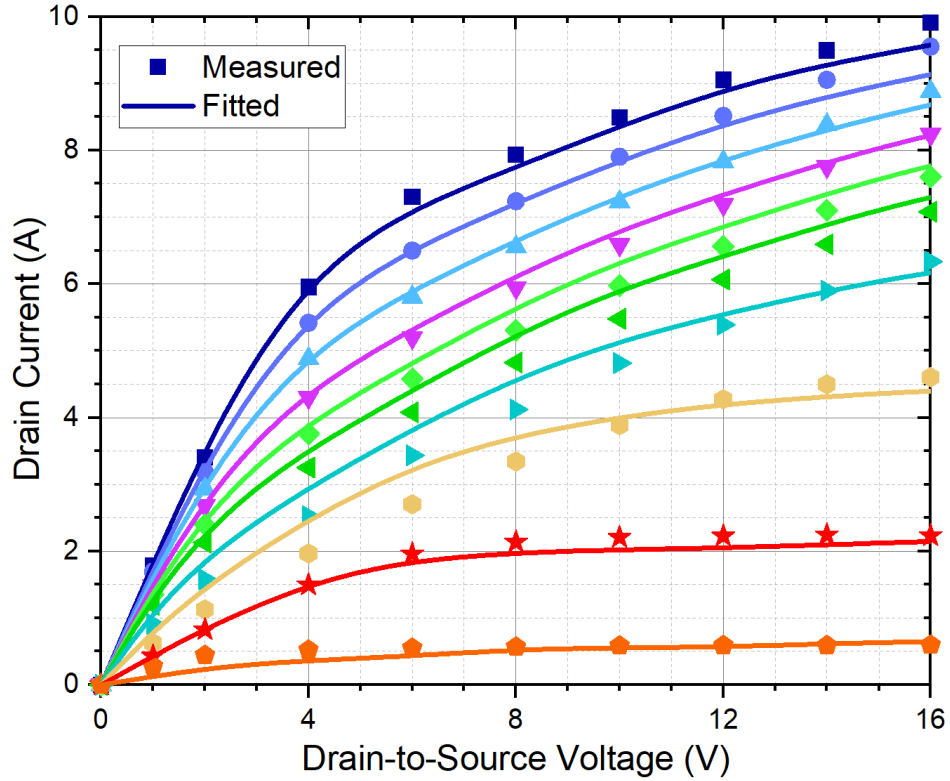
(c)


Measured
Fitted
Drain Current (A)
Drain-to-Source Voltage (V)
0
2
4
6
8
10
12
16

(d)




(e)




(f)

*Figure 5-19: $I_d$ – $V_{ds}$ characteristic curves of the PSJ-FET behavioural model compared against the average values of measurement data at $T_j$ = (a) $25^0$C, (b) $50^0$C, (c) $75^0$C, (d) $100^0$C, (e) $125^0$C and (f) $150^0$C*

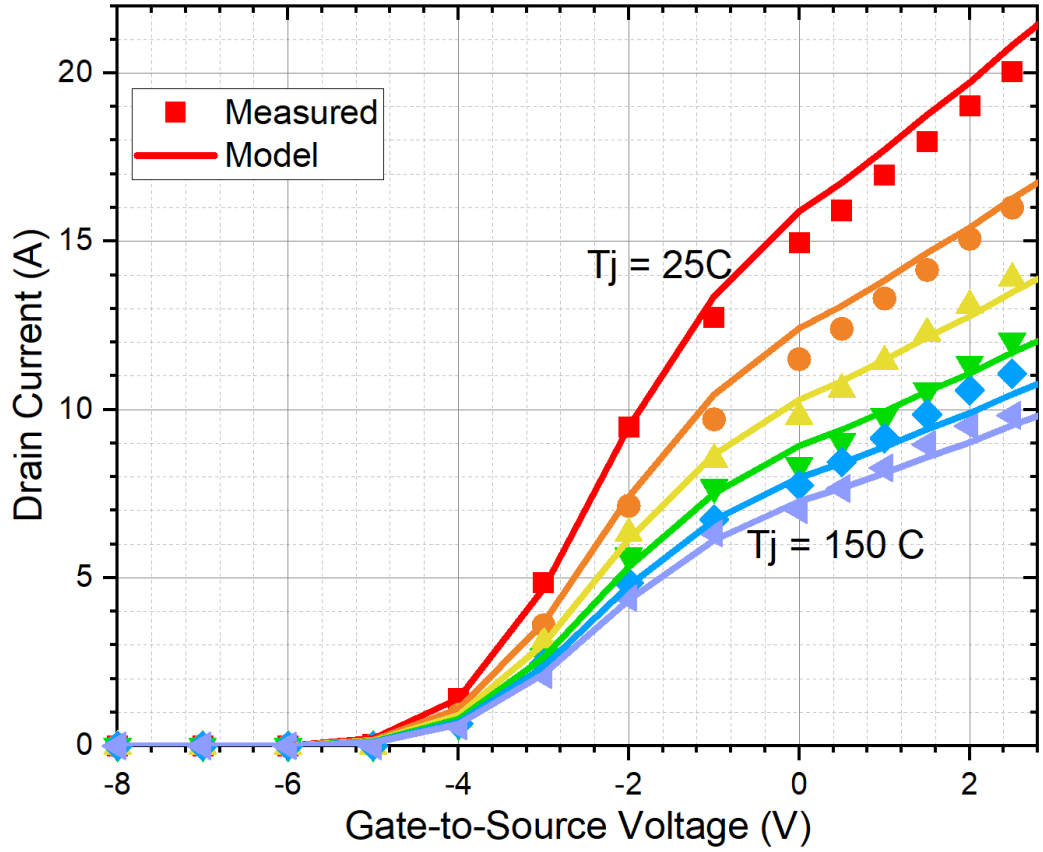



*Figure 5-20: $I_d$ – $V_{gs}$ characteristic curves of the PSJ-FET behavioural model compared against the average values of measured data at $T_j$ = 25$^0$C, 50$^0$C, 75$^0$C, 100$^0$C, 125$^0$C and 150$^0$C and $V_{ds}$ = +16 V*

### *5.7.2. Device terminal-to-terminal capacitances*

The non-linear terminal capacitances of the PSJ-FET were modelled using the following equations and average measurement data in Figure 3-10(b):

$$C_{gd}(V_{dg}) = C_{gd0} + M_{Cgd} \cdot \left(1 + \tanh\left(\alpha_{Cgd} \cdot V_{dg} + \beta_0\right)\right)$$

$$C_{gs}(V_{gs}) = C_{gs0} + M_{Cgs1} \cdot \left(1 + \tanh\left(\alpha_{Cgs1} \cdot V_{gs} + \beta_1\right)\right)$$

$$+ M_{Cgs2} \cdot \left(V_{gs} + V_{gsp}\right) \cdot \left(1 + \tanh\left(\alpha_{Cgs2} \cdot V_{gs} + \beta_2\right)\right)$$

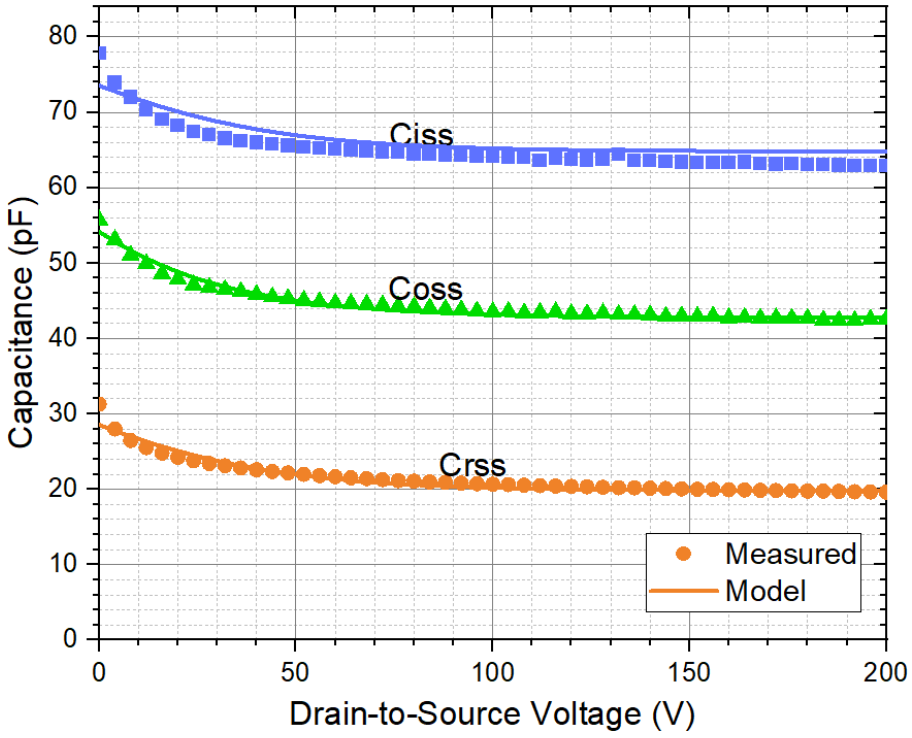
$$C_{ds}(V_{ds}) = C_{ds0} + M_{Cds} \cdot \left(1 + \tanh\left(\alpha_{Cds} \cdot V_{ds} + \beta_3\right)\right)$$

The values of the fitting parameters were obtained using the MATLAB curve fitting tool and presented in Table 5-7. The modelled C-V curves were compared

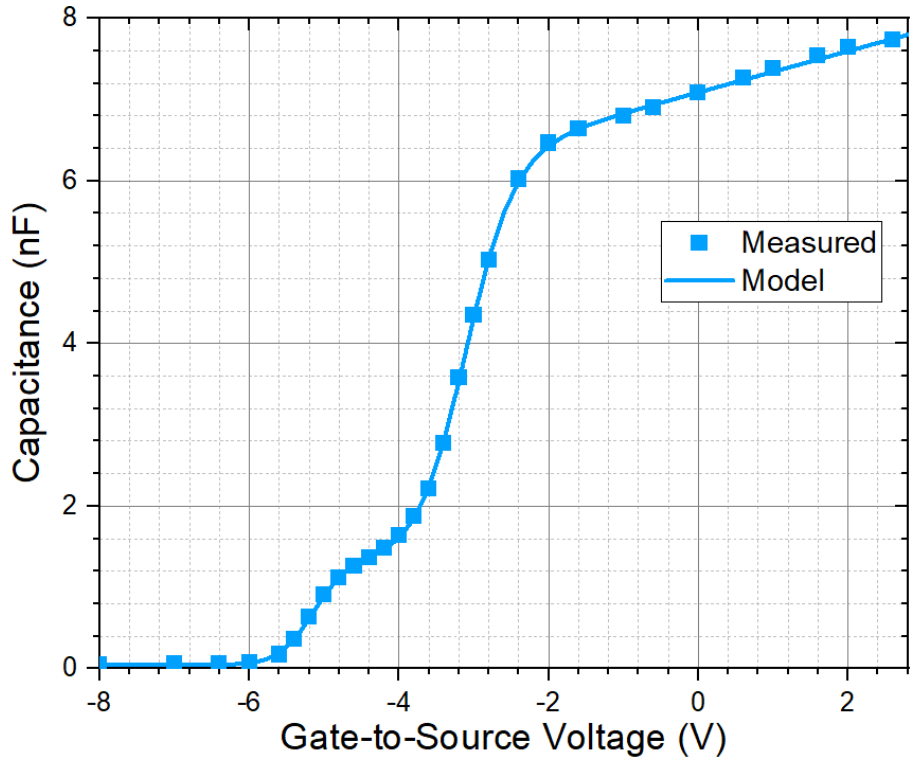
against their measured counterparts in Figure 5-19(a) and (b); they exhibited an excellent match to each other.

| Parameters | Values |
|---|---|
| $\alpha_{Cds}$ | -0.03558 |
| $\alpha_{Cgd}$ | 0.01738 |
| $\alpha_{Cgs1}$ | 2.282 |
| $\alpha_{Cgs2}$ | 1.555 |
| $\beta_0$ | 0.1419 |
| $\beta_1$ | 11.75 |
| $\beta_2$ | 4.867 |
| $\beta_3$ | -0.5187 |
| $C_{ds0}$ | 22.96 |
| $C_{gd0}$ | 45 |
| $C_{gs0}$ | 52 |
| $M_{Cds}$ | 5 |
| $M_{Cgs1}$ | 636.6 |
| $M_{Cgs2}$ | 126.6 |
| $M_{Cgd}$ | -12.6 |
| $V_{gsp}$ | 22.79 |

*Table 5-7: PSJ-FET capacitance fitting parameters used in its behavioural model*




(a)

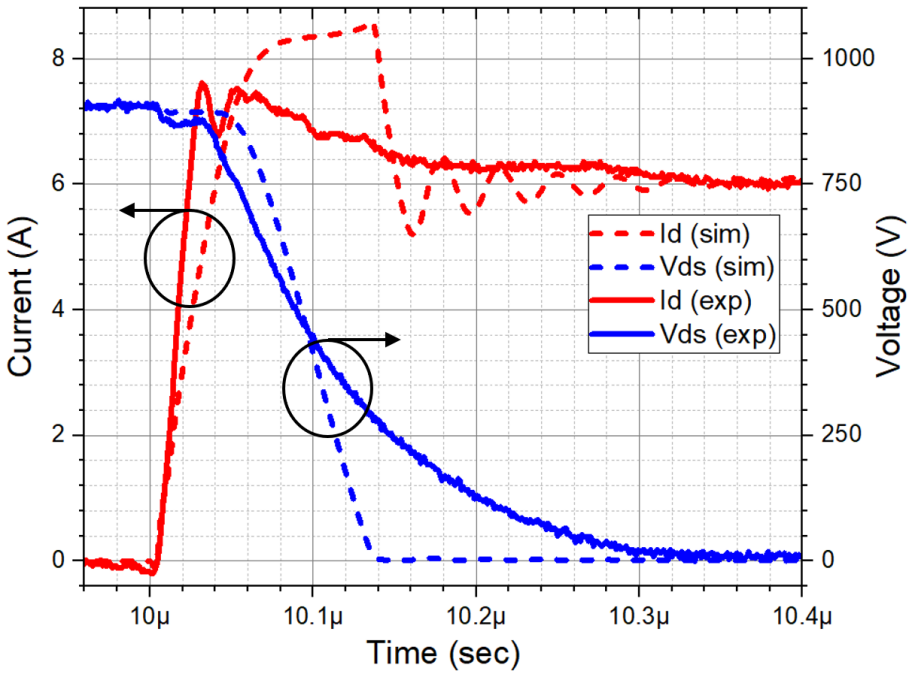



(b)

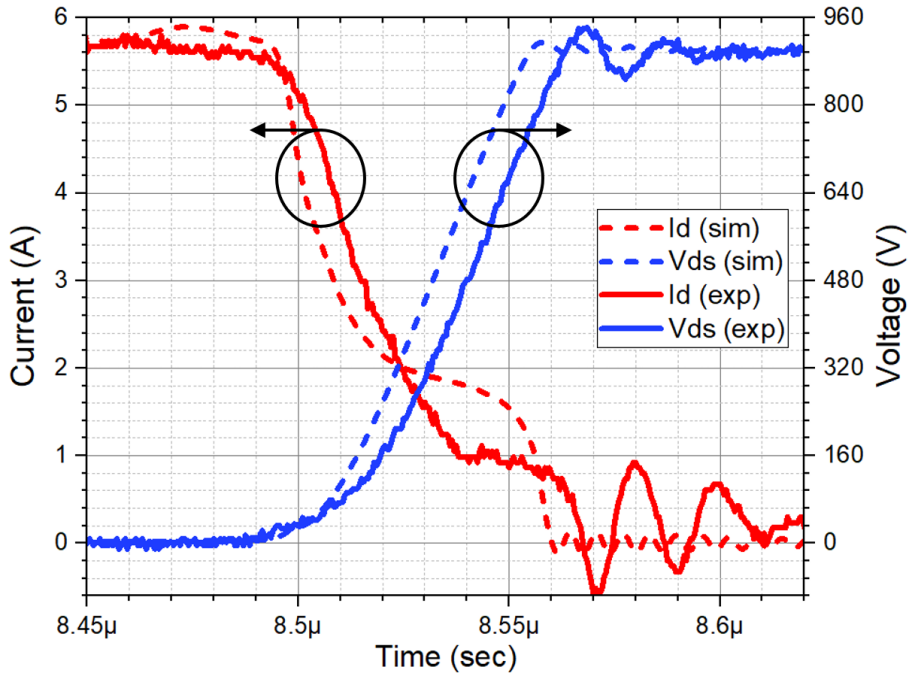
*Figure 5-21: (a) $C_{iss}$, $C_{rss}$ $C_{oss}$ vs. $V_{ds}$ characteristic curves and (b) $C_{gs}$ vs. $V_{gs}$ characteristic curve fitted against the average measurement data*

### *5.7.3. Model limitations*

Although the static I-V and C-V characteristics of the PSJ transistor's behavioural model showed good agreement with its measured average values, its turn-on switching waveforms showed remarkable discrepancies to their measured counterparts. The turn-on and turn-off waveforms obtained from simulation and experiment at dc-link voltage of 900 V and load current of 6 A in DPT configuration (in Figure 3-15) were synchronised using the rising and falling edges of their $V_{gs}$ waveforms and are compared to each other in Figure 5-20(a) and (b), respectively. It is notable that the slope $dV_{ds}/dt$ during the device turn-on that was extracted from the experimental results were significantly lower than its simulation model counterpart; the turn-on $dV_{ds}/dt$ measured from 10% to 90% of its initial value for simulation and experiment were determined as 10.34V/ns and 3.94V/ns, respectively. Also, the shape of the experimental $V_{ds}$ fall waveform exhibited a characteristic of an exponential decay unlike its simulation counterpart with a linear characteristic. The estimated $C_{gd}$ - $V_{ds}$ curve presented in Section that was extracted from turn-on waveforms was compared against its measured average counterpart in Figure 5-22. As the Miller capacitance ($C_{gd}$) plays a critical role in determining the $V_{ds}$ fall and rise characteristics, this mismatch implies that the $C_{gd}$ characteristics of the model that were fitted against the average $C_{gd}$ vs. $V_{ds}$ measurement data for the device 'off' state plotted in Figure 5-19(a) is grossly underestimated compared to its actual value when the device enters its 'on' state as discussed in Section 3.1.2.




(a)

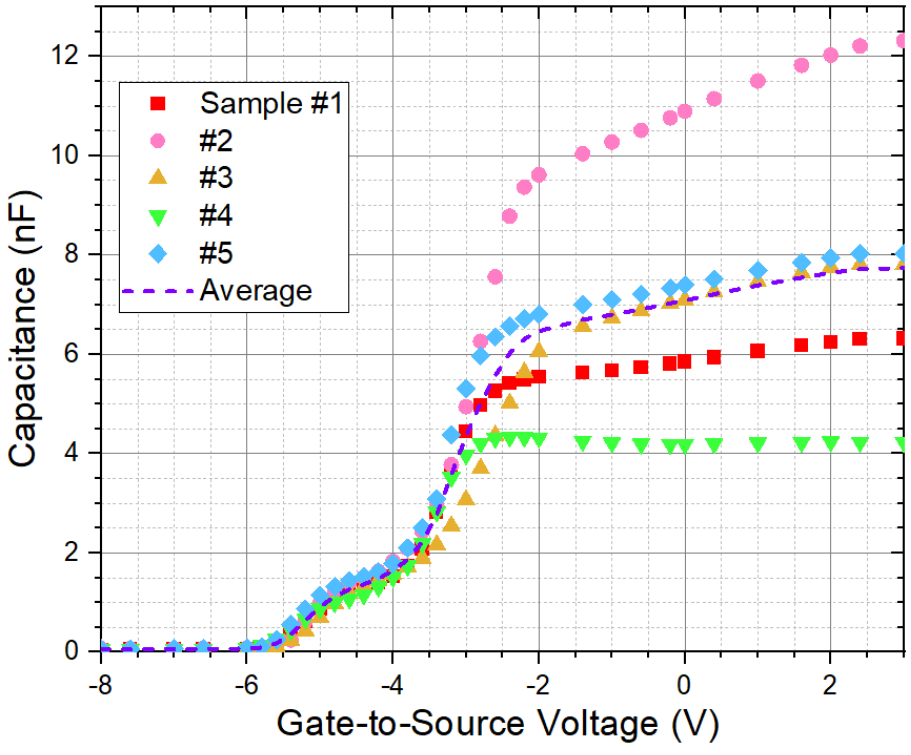



(b)

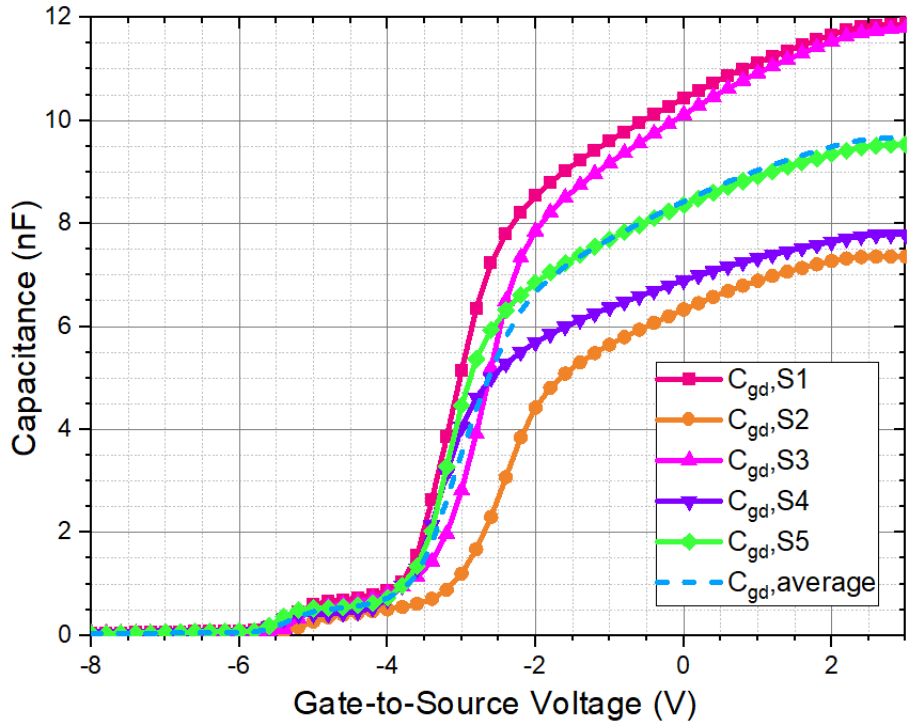
*Figure 5-22: Comparison of simulation and experimental (typical) waveforms of the large-area PSJ-FET during its (a) turn-on and (b) turn-off transients at 900 V, 6 A*

In addition, the typical $dI_d/dt$ slope of the large area PSJ transistor during $I_d$ rise interval was determined to be 1.96 times higher than its simulation model. This is due to an overestimation of the measured average $C_{gs}$ values compared to the

actual $C_{gs}$ characteristics of the device that was specifically tested for this work. In fact, the typical $C_{gs}$ vs. $V_{gs}$ and $C_{gd}$ vs. $V_{gs}$ characteristic curves for 5 device samples showed a significant device-to-device variation as shown in Figure 5-21(a) and (b), respectively; at $V_{gs}$ = -2 V, the standard deviation of $C_{gs}$ was determined to be 27.38% of its mean value. This implies that the $I_d$ rise and $V_{ds}$ fall intervals during the turn-on process of PSJ devices could show remarkable deviation from each other, which ought to be investigated in the future work. Furthermore, the mismatch in the turn-on $dI_d/dt$ slope may also be explained by an error in the $R_{g,int}$ measurement. As the maximum AC frequency of the Hioki 3522 LCR meter that was used for $R_{g,int}$ was limited to 200 kHz, there is a possibility that the impedance of the $C_{iss}$ in series with $R_{g,int}$ dominated the total impedance of the AC current path during the measurement and thus $R_{g,int}$ could be overestimated. In the future, $R_{g,int}$ measurements with frequencies > 1MHz shall be used as this will minimize the series capacitive impedance and thus yield $R_{g,int}$ extraction with better accuracy [132].




(a)




(b)

*Figure 5-23: Variations in (a)$C_{gs}$ vs. $V_{gs}$ and (b) $C_{gd}$ vs. $V_{gs}$ measurement data at $V_{ds}$ = 0V for 5 large-area PSJ-FETs at $V_{ds}$ = 0V, $f_{ac}$ = 100 kHz*

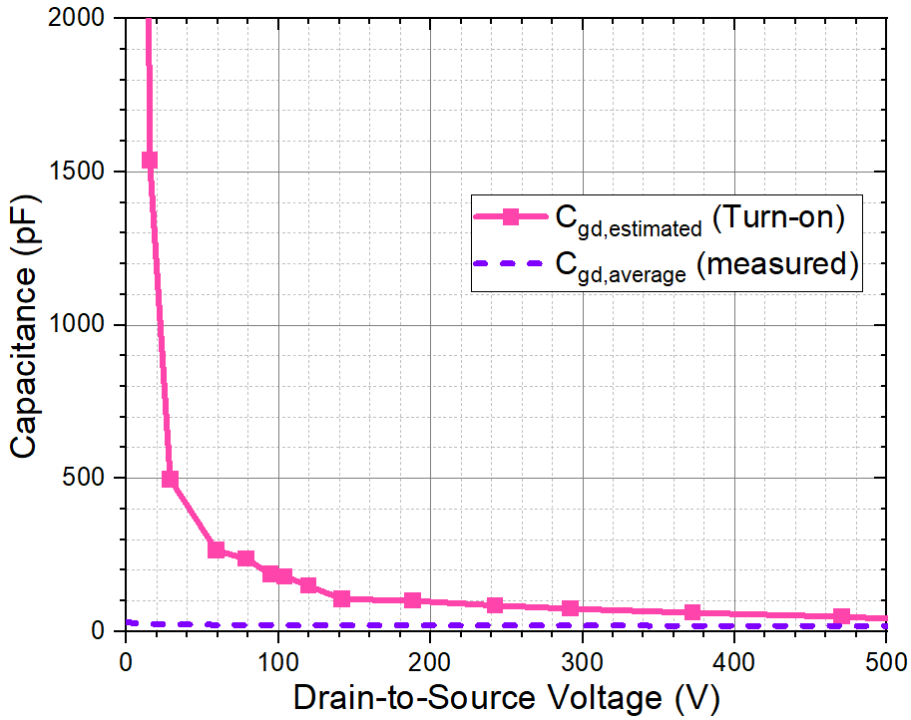



*Figure 5-24: Estimated $C_{gd}$ vs. $V_{ds}$ extracted from the typical turn-on waveforms in Figure 3-19(a) and measured average $C_{gd}$ vs. $V_{ds}$ values of the large area PSJ transistor*

Similarly, the turn-off $I_d$ and $V_{ds}$ waveforms and of the average PSJ-FET model exhibited noticeable mismatch to its experimental counterpart as shown in Figure 5-20(b). The average $dV_{ds}/dt$ of the $V_{ds}$ rise waveform obtained from the simulation and DPT experiment were determined to be 16.32V/ns and 18.173V/ns, respectively; hence, a relative error of 10.2% is present. Furthermore, the simulated $I_d$ waveform showed significant discrepancy to its experimental counterpart as its value during the $V_{ds}$ rise interval was higher than the measured waveforms in Figure 5-20(b) and thus the turn-off energy will be overestimated. This may imply that the modelled junction capacitances of APD and FWD (indicated in the circuit diagram Figure 3-26) are inaccurate. In overall, the dynamic behaviour of the average behavioural model of the PSJ transistor lacks accuracy.

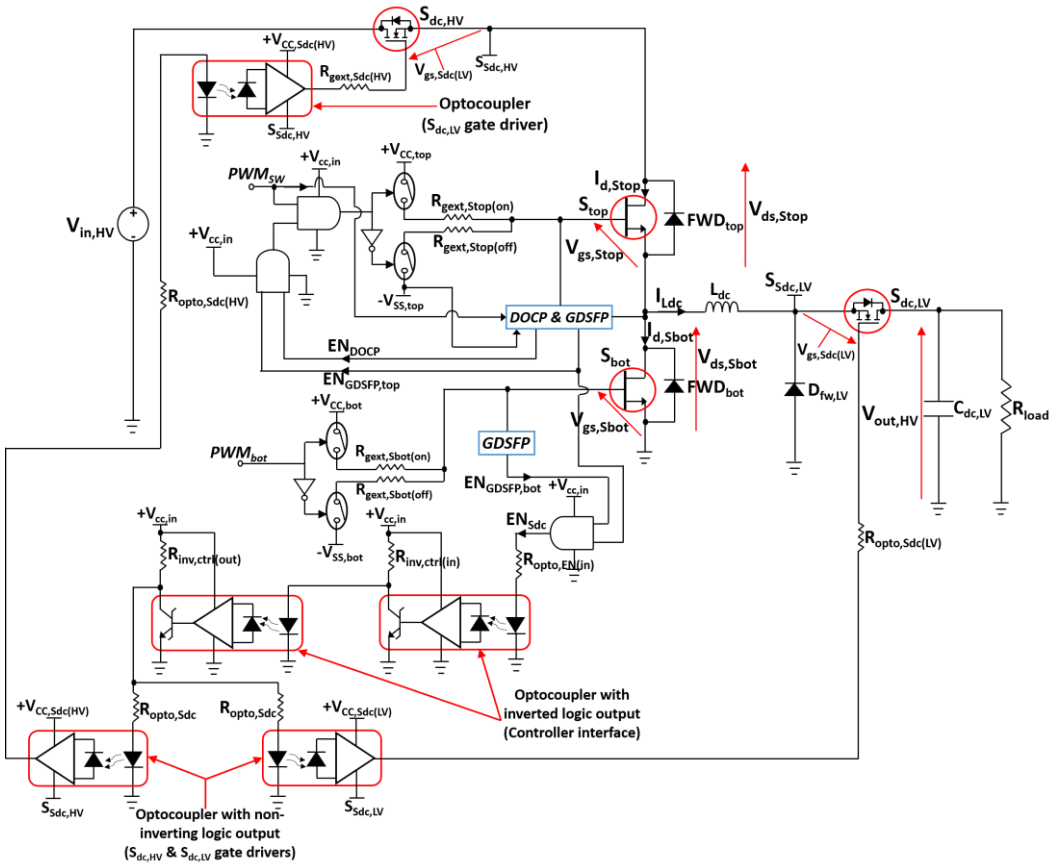
As the dynamic characteristics of the proposed average behavioural model exhibited poor agreement with the typical waveforms of the large-area PSJ transistor, a precise modelling of switching behaviour of PSJ devices will remain as one of the major future work, which will make a significant contribution towards the optimisation of the PSJ device performances in the power converters for various applications. Nevertheless, the proposed model would suffice for a qualitative analysis of the circuit behaviour during fault events, which is the main topic of discussion for this chapter.

## *5.8. Converter circuit simulation*

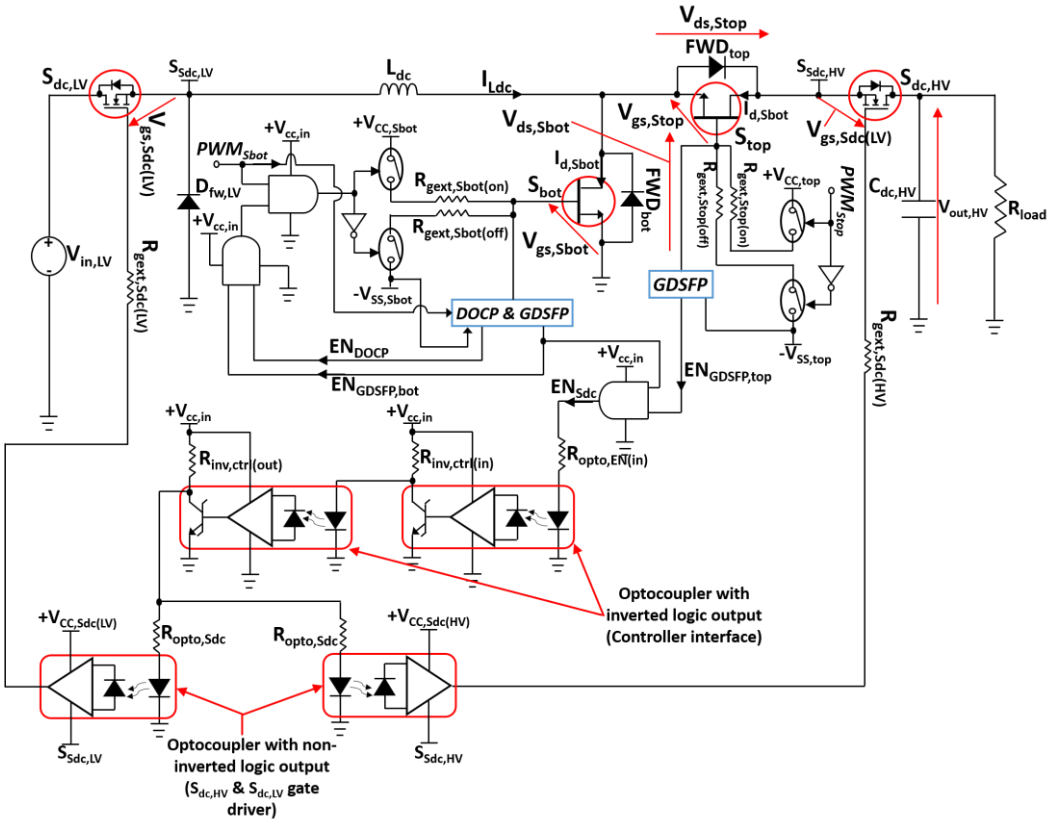
### *5.8.1. Circuit schematic and component selection*

In order to verify the fail-safe operation of the bidirectional dc-dc converter with D-mode PSJ devices during normal operation and gate drive supplies failure

modes, two PSpice circuit models were built using TINA-TI simulator; one for step-down conversion and the other one for step-up conversion. The schematics for the simulated circuits for buck and boost dc-dc conversion modes are shown in Figure 5-23(a) and (b).




(a)




(b)

*Figure 5-25: Schematic of DC-DC converter with DOCP (Figure 4-12(b)) and refined GDSFP (Figure 4-20) schemes in (a) step-down and (b) step-up conversion mode simulated under TINA-TI PSpice simulation software*

The components and parameters used for this simulation are enlisted in Table 5-8(a) and (b), respectively. Due to the lack of PSpice model for the $S_{dc,HV}$ and $S_{dc,LV}$ gate drivers part (IX3120G) used for hardware demonstration, a 5MBd optocoupler (ACPL-2231) with a similar range of propagation delay (150 ns typical) to IX3120G (300 ns typical) was used in the simulation as an alternative. The same GDSFP and DOCP circuit components as in the converter hardware prototype were used in order to replicate the whole system for simulation. The same SiC Schottky diode part (GB10MPS17) and parallel snubber capacitor value (100 pF) in hardware implementation were used for simulation.

For the converter-to-controller IC and controller-to-converter interfacing circuits in Figure 5-13(a) and (b), the behavioural SPICE models for optical transmitter and receiver pairs (HFBR-1521Z and HFBR-2521Z) in Figure 5-13 are currently not available. As an alternative to these, a SPICE model of 10MBd optocoupler (ACNT-H61T) exhibiting similar range of typical propagation delay and same output logic to HFBR-2521Z receiver was selected and implemented in the simulation circuit in Figure 5-23. In order to exemplify the effects of mismatched $C_{res}$ values, the $C_{res}$ values for GDSFP schemes on the $S_{top}$ and $S_{bot}$ switches were set to be 448 µF and 672 µF, respectively; these values correspond to +/- 20% tolerance band with a nominal capacitance value of 560 µF of the EEEFT1V561AP capacitors [133] that were implemented in the converter hardware. Under this condition, the minimum (worst-case) $t_{frame}$ provided for the GDSFP system to isolate the converter from an external voltage can be derived based on equation (4-7) and expressed as:

$$t_{frame,min} = R_{g,extoff(nom)} \cdot C_{res(nom)} \cdot \left(1 - Tol_{Rg}\right) \cdot (1 - Tol_{Cres}) \cdot \ln\left(\frac{V_{f,Dch} - V_{SS}}{V_{gs,th}}\right) \quad \ldots(5\text{-}32)$$

Where:

$R_{g,extoff(nom)}$ = nominal $R_{g,ext(off)}$ value

$C_{res(nom)}$ = nominal $C_{res}$ value

$Tol_{Rg}$ = maximum tolerance swing of $R_{g,extoff(nom)}$ value

$Tol_{Cres}$ = maximum tolerance swing of $C_{res(nom)}$ value

$V_{f,Dch}$ = forward knee voltage drop across the diode $D_{ch}$ (refer to Figure 4-21)

$V_{gs,th}$ = turn-on threshold $V_{gs}$ of the DUT

The external turn-off gate resistors ($R_{g,ext(off)}$) were also assumed to have +/- 20% tolerance (9.6 Ω for $S_{top}$ and 14.4 Ω for $S_{bot}$) for this simulation work. The operating principles of the two protection schemes are explained thoroughly in Section 4.4 and 4.5. The simulation parameters and components are clearly labelled and enlisted in Table 5-8(a)~(e).

| Components | Part Number |
|---|---|
| AND logic gates | SN74LV08A |
| $D_{disc,desat}$ | US1AFA |
| $D_{desat,sense}$ | BY203-20S |
| $G_{opt,desat}$ | ACPL-H61L |
| $L_{comp,desat}$ | LM311 |
| $M_{comp,desat}$ & $M_{disc,desat}$ | IPD220N06L3 |
| $M_{inv,p}$ | IRFR5305PbF |
| $M_{inv,n}$ | IRFR3806PbF |

(a)

| Components | Part Number |
|---|---|
| $D_{ch}$ & $D_{disc}$ | UF4002 |
| $D_{fw,LV}$ | GC20MPS12 |
| $G_{opt,gsf}$ | ACPL-H61L |
| $L_{comp,gsf}$ | LM311 |
| $M_{ch}$ | IPD220N06L3 |
| $S_{dc,HV}$ | C2M0045170D |
| $S_{dc,LV}$ | C3M0016120D |
| $G_{opt,ctrl(in)}$ & $G_{opt,ctrl(out)}$ | ACPL-M61T |
| $S_{dc,link(HV)}$ & $S_{dc,link(LV)}$ gate drivers | HCPL-2231 |

(b)

| Parameters | Values |
|---|---|
| $C_{block}$ | 100 pF |

| | |
|---|---|
| $R_{comp,desat}$, $R_{desat1}$ and $R_{desat2}$ | 500 Ω |
| $R_{g,ext(on)}$ and $R_{g,ext(off)}$ | 3.3 Ω and 12 Ω |
| $R_{gext,Sdc(HV)}$ & $R_{gext,Sdc(V)}$ | 10 Ω |
| $R_{inv,p}$ and $R_{inv,n}$ | 4 Ω and 40 Ω |
| $R_{ref1}$ and $R_{ref2}$ | 10 Ω and 487 Ω |
| $+V_{cc1}$ and $+V_{cc,in}$ | + 5 V |
| $+V_{cc}$ | + 2.5 V |
| $+V_{cc,Sdc(HV)}$ & $+ V_{cc,Sdc(LV)}$ | + 15 V |
| $+/-V_{SS}$ | +/- 15 V |

(c)

| Parameters | Values |
|---|---|
| $C_{res(Sbot)}$ & $C_{res(Stop)}$ | 448 µF and 672 µF |
| $R_{comp,out}$ | 1 kΩ |
| $R_{gsf,ref1}$ | 750 Ω |
| $R_{gsf,ref2}$ | 1.5 kΩ |
| $R_{inv,ctrl(in)}$ & $R_{inv,ctrl(out)}$ | 450 Ω |
| $R_{opto,EN(in)}$ | 450 Ω |
| $R_{opt,in}$ | 915 Ω |
| $+/- V_{ss2}$ | +/-15 V |

(d)

| Parameters | Values |
|---|---|
| $C_{dc,HV}$ | 4.5 µF |
| $C_{dc,LV}$ | 1 µF |
| $I_{Ldc}$ | 5.567 A (nominal) |
| $R_{load(HV)}$ | 291 Ω |
| $R_{load(LV)}$ | 90 Ω |
| $V_{in,HV}$ / $V_{out,HV}$ | 900 V |
| $V_{in,LV}$ / $V_{out,LV}$ | 500 V |

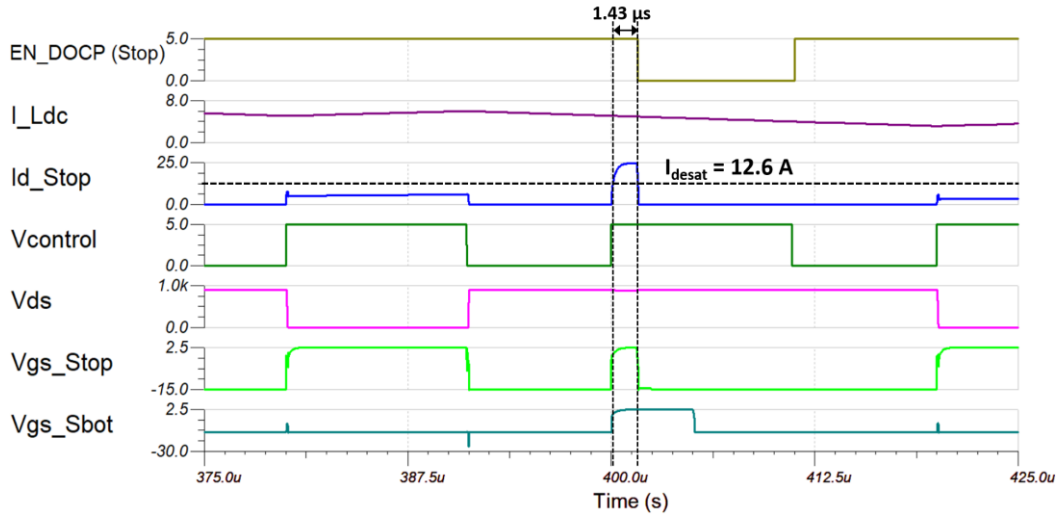
(e)

*Table 5-8: Simulation of buck and boost DC-DC power converters (Figure 5-2(a) and (b)): (a) DOCP (Figure 4-12(b)) components, (b) 2nd prototype GDSFP (Figure 4-21) components, (c) DOCP parameters, (d) 2nd GDSFP prototype parameters and (e) converter circuit parameters*

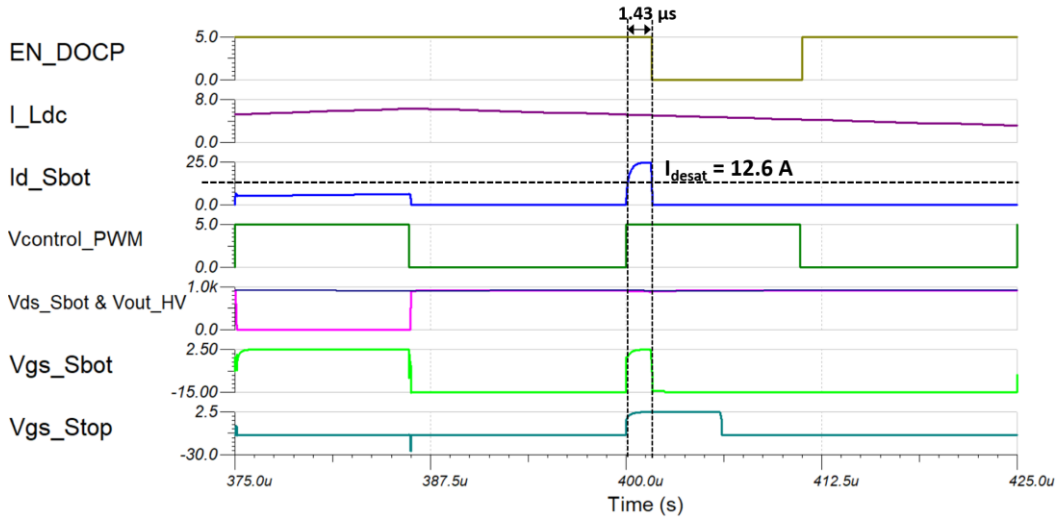
### *5.8.2. Fail-safe operation during steady state*

In this simulation, the short-circuit fault event during steady-state operation was set to occur at time t = 400 µs that is the onset of the main switch ($S_{top}$ for buck conversion and $S_{bot}$ for boost conversion) turn-on before the blanking time ($t_{blank}$) of the DOCP scheme has passed and thus longest period of time taken for the protection scheme to clear out the fault current can be determined as discussed in Section 4.5. The resultant waveforms for buck and boost converters (in Figure 5-23(a) and (b)) are clearly presented and labelled in Figure 5-24(a) and (b), respectively.

From the waveforms, it can be observed that the shoot-through current in both buck and boost converters were cleared away within 1.43 µs of its occurrence. However, as discussed previously in Section 4.6.2, the actual response time of the DOCP prototype was determined as 980 ns longer than the simulation, and thus worst-case response time in a real hardware is expected to be 2.41 µs, which is still shorter than the response time of the prototype circuit demonstrated in [124]. However, if this exceeds the safe operating area (SOA) boundary of the PSJ transistors, then the devices will not be able to withstand the fault current under high DC voltage and thus may fail even before the DOCP clears out the fault. The SOA boundary of the PSJ transistors under DC and transient current flow were not determined in this research as the availability of the large-area device samples for testing was limited.




(a)




(b)

*Figure 5-26: DC-to-DC converter waveforms in the SPICE simulation under a single shoot-through event during steady-state operation: (a) buck and (b) boost conversion*

### *5.8.3. Fail-safe operation on -$V_{SS}$ supply fault event*

The values of $C_{res}$ and $R_{g,off(ext)}$ used in GDSFP schemes for top and bottom switches ($S_{bot}$ and $S_{top}$) are critical elements determining the time frame within which the converter must be isolated from the input dc voltage source by turning off the dc-link switch(es) to prevent shoot-through under -$V_{SS}$ failure. In reality, as their values vary for every unit with a certain tolerance band, if the -$V_{SS}$ supplies for both devices fail, either $S_{bot}$ or $S_{top}$ that has a smaller $C_{res}$ x $R_{g,off(ext)}$ product value

will be turned on first and hence it is unlikely for $S_{bot}$ and $S_{top}$ to be turned 'on' simultaneously. As long as the circuit is fully isolated from the DC-link voltage sources on the input side within the minimum time frame i.e. $t_{frame}^{min} > t_{dc,iso}^{max}$, the fail-safe operation of D-mode devices is guaranteed. The maximum (worst-case) length of time required for the circuit to be isolated from the DC-link supply on HV / LV side under $-V_{SS}$ supply failure event ($t_{dc,iso}^{max}$) can be expressed as:

$$t_{dc,iso(LV/HV)}^{max} = t_{pd,comp(GDSFP)}^{max} + t_{pd,opto(GDSFP)}^{max} + t_{pd,AND}^{max} + t_{pd,control(int)}^{max} + t_{pd,opto(Sdc,LV/HV)}^{max} + t_{Sdc,toff(LV/HV)} \quad \ldots(5\text{-}33)$$

Where:

$t_{pd,comp}^{max}$ = maximum input-to-output propagation delay of the GDSFP comparator

$t_{pd,opto(GDSFP)}^{max}$ = maximum input-to-output propagation delay of the GDSFP optocoupler

$t_{pd,AND}^{max}$ = maximum input-to-output propagation delay of the AND logic gate

$t_{pd,ctrl\_to\_opto(Sdc)}^{max}$ = maximum propagation delay of the signal from the controller IC output to $S_{dc,HV}$ / $S_{dc,LV}$ gate driver input stage

$t_{pd,opto(Sdc)}^{max}$ = maximum input-to-output propagation delay of the isolated $S_{dc,LV}$ / $S_{dc,HV}$ gate driver with an opto-coupling stage

$t_{Sdc,toff(LV/HV)}$ = turn-off delay time of $S_{dc,LV}$ / $S_{dc,HV}$

In this section, the case in which the protection system is designed in a conservative manner such that $t_{frame}^{min} \gg t_{dc,iso}^{max}$ is considered. For the simulation, it was assumed that the converter operates in a steady state under full output load for the first 2.6 ms after which the $-V_{SS,top}$ and $-V_{SS,bot}$ supplies fail instantaneously. The

critical waveforms of the buck and boost converters under the fault condition are presented and clearly labelled in Figure 5-25(a) and (b), respectively.

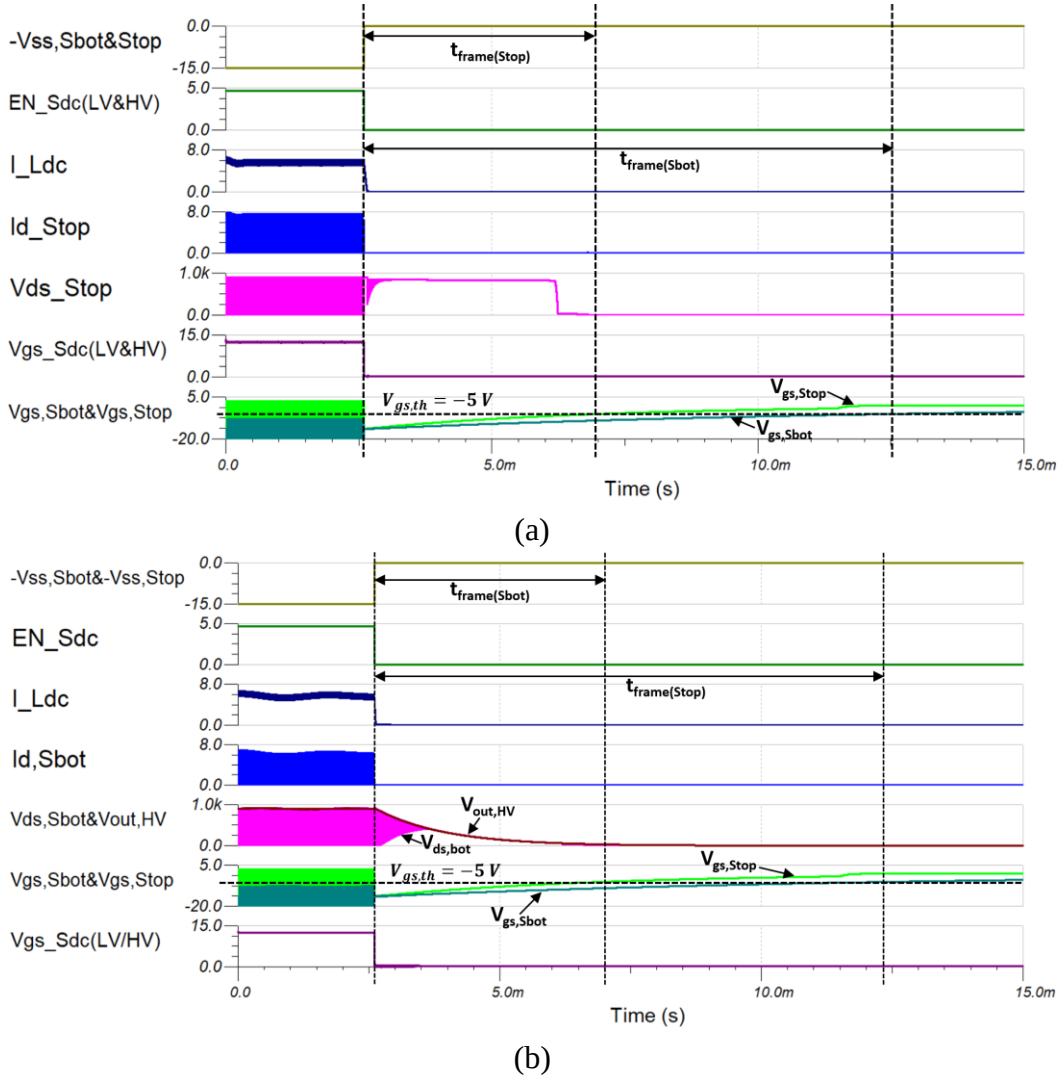



*Figure 5-27: DC-to-DC converter simulation waveforms under -$V_{SS}$ failure event in (a) buck and (b) boost conversion modes*

When the failure occurs, both $S_{bot}$ and $S_{top}$ devices are turned off instantaneously via $V_{gs}$ clamping circuit within the GDSFP schemes (refer to Figure 4-21) on top and bottom sides. The inductor current then freewheels through top FWD and $S_{dc,HV}$ (for boost conversion) or bottom FWD and $S_{dc,LV}$ (for buck

conversion) and decrease towards zero. Meanwhile, the fault signal is propagated through the AND gate so that its output $EN_{Sdc}$ signal will become logic LOW, which will then be propagated through the two controller interface optocouplers () in series and $S_{dc,HV}$ and $S_{dc,LV}$ gate drivers. The input capacitances of $S_{dc,HV}$ and $S_{dc,LV}$ will then start to be discharged. After the time length of $t_{Sdc,toff(HV)}$ (for buck) or $t_{Sdc,toff(LV)}$ (for boost) has passed from this point, the two switches will be turned off and thus converter will be fully isolated from the dc voltage source on the input (i.e. HV-side and LV-side for buck and boost conversion modes, respectively).

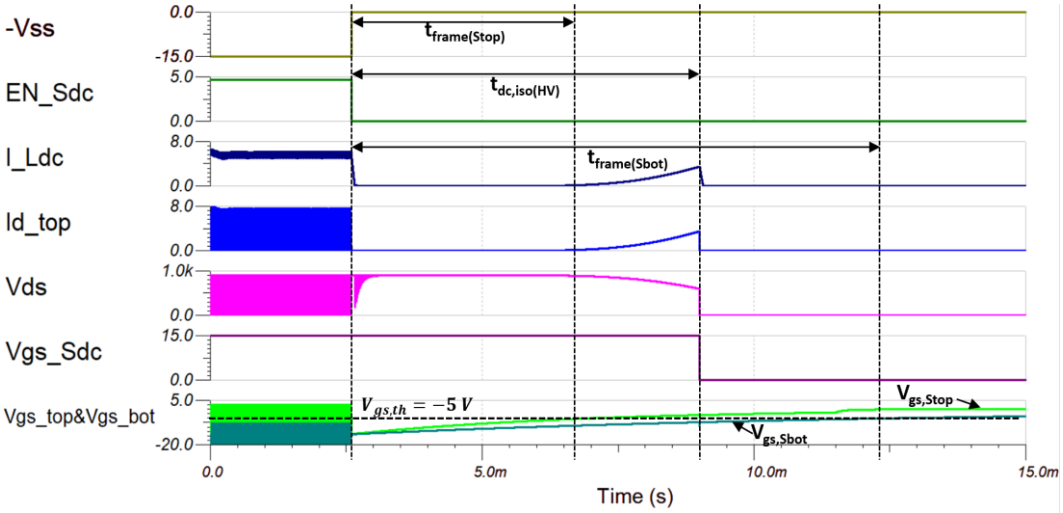
For both simulation, the minimum $t_{frame}$ is determined by the least $R_{g,ext(off)}$ and $C_{res}$ values that deviated -20% from their nominal values (i.e. 12 Ω and 560 μF) in the top-side GDSFP circuit. In this case, the $t_{frame,min}$ can be calculated using the equation as 4.4 ms. The total $t_{dc,iso(HV)}$ and $t_{dc,iso(LV)}$ for both simulation were determined as 790 ns and 935 ns, respectively, whilst the $t_{frame(min)}$ was calculated using the equation (5-32) to be 4.459 ms. Since the protection circuit was designed in a very conservative manner such that $t_{dc,iso(HV)} \ll t_{frame(\min)}$ and $t_{dc,iso(LV)} \ll t_{frame(\min)}$, the D-mode switching power devices are immune to critical failure due to $-V_{SS}$ supply failure for both buck and boost conversion.

### *5.8.4. Device failure in a poor system design*

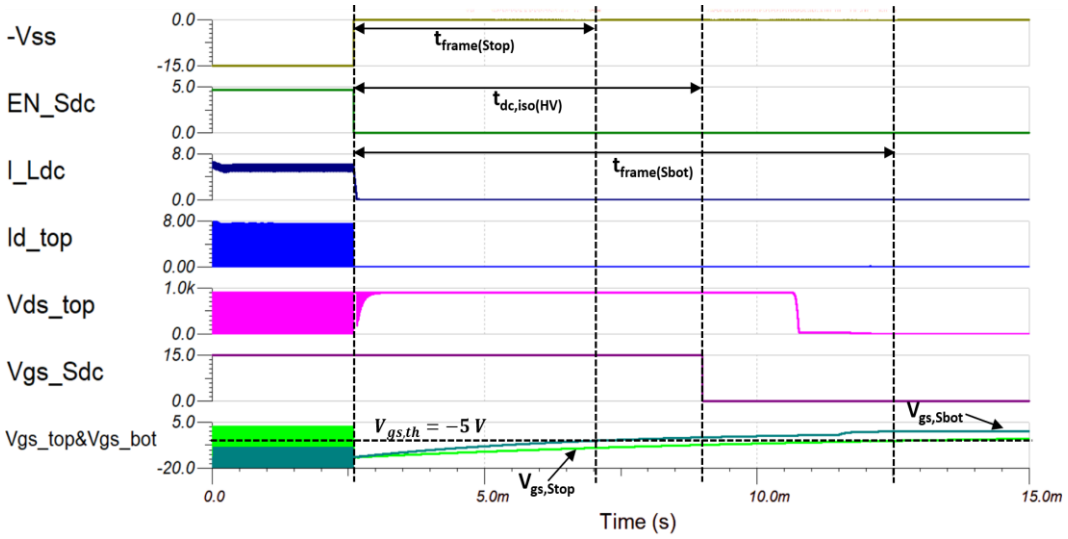
The minimum value of $C_{res}$ x $R_{g,ext(off)}$ in GDSFP scheme for either $S_{bot}$ and $S_{top}$ will determine the minimum time frame ($t_{frame,min}$) within which the $S_{dc,link}$ on HV and LV sides must be turned off to ensure that the D-mode devices do not operate at deep saturation region and thus fail in certain fault scenarios. Should either the $S_{top}$ or $S_{bot}$ be turned on first before the other after the $-V_{SS}$ failure event

has occurred, it will operate in a deep I-V saturation region and thus be damaged if the propagation delay between the controller and $S_{dc,link}$ switches is excessively long.

In order to demonstrate the importance of the protection system design for D-mode power devices, the cases of poor system design that leads to device failure are considered. For the step-down conversion i.e. power flow from HV-side to LV-side, the $t_{frame,top}$ provided by the $C_{res}/R_{g,ext(off)}$ pair values of the $S_{top}$ becomes critical in determining whether the system can operate in a fail-safe mode or not. The resultant simulation waveforms for step-down converter with two cases are plotted in Figure 5-26. Under the case $t_{frame(bot)} > t_{frame(top)}$, if the $t_{dc,iso}$ becomes excessively long due to poor controller-to-power circuit interface circuit design so that $t_{dc,iso} > t_{frame(top)}$, then the $S_{top}$ will enter into its deep saturation region as shown in Figure 5-26(a) that leads to excessive power dissipation and thus potentially failure. For the case $t_{frame(bot)} < t_{frame(top)}$, on the other hand, the $I_{Ldc}$ will remain zero as long as $S_{top}$ is in its 'off' state as observed from Figure 5-26(b). If the $S_{dc,HV}$ and $S_{dc,LV}$ are turned off within the given $t_{frame(top)}$, then the power devices will be isolated from the DC power supplies and kept safe. The $I_{Ldc}$ will keep decreasing towards zero and will eventually resonate with DC-link output capacitor bank and device and FWD junction capacitances.




(a)

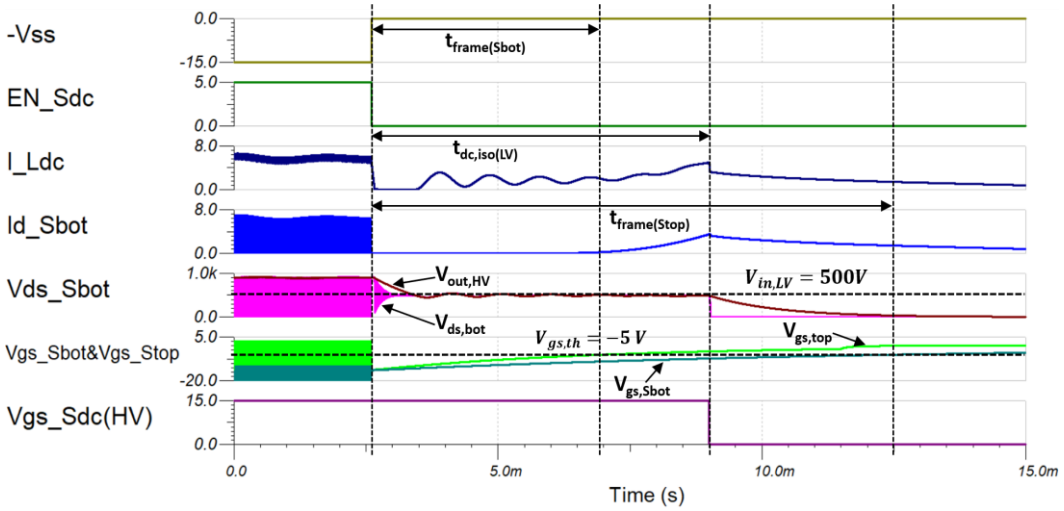



(b)

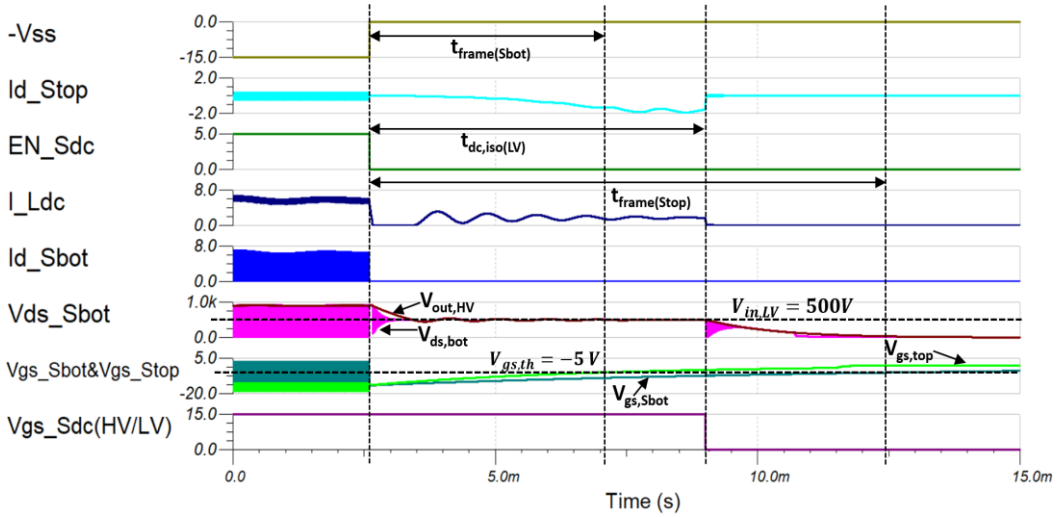
*Figure 5-28: Buck DC-to-DC converter simulation waveforms under -$V_{SS}$ fault event: (a) $t_{frame(Stop)} < t_{dc,iso} < t_{frame(Sbot)}$ and (b) $t_{frame(Sbot)} < t_{dc,iso} < t_{frame(Stop)}$*

For the step-up conversion, on the other hand, the critical $t_{frame,min}$ is determined by the GDSFP parameters in $S_{bot}$. Should the $S_{dc,link}$ switches are not turned off within the provided $t_{frame,min}$ value, the bottom switch will enter into its deep saturation region and thus may potentially fail. The same simulation was carried out for step-up converter with $t_{frame(Sbot)} < t_{dc,iso} < t_{frame(Stop)}$ and $t_{frame(Stop)} < t_{dc,iso} < t_{frame(Sbot)}$ and their waveforms are clearly labelled and presented in Figure

5-27(a) and (b). For both figures, it can be observed that the oscillations in the $V_{ds}$ waveform exist after the power devices are turned off by the GDSFP scheme as the inductor current falls to zero and subsequently resonates with FWD and device capacitances as it crosses zero and changes polarity at a certain resonant frequency. Should the $S_{top}$ be turned on first, then the $I_{Ldc}$ would flow through top FWD and $S_{top}$ that are in parallel to each other. As the $V_{ds,Stop}$ is clamped by the presence of FWDs and the $S_{bot}$ device is still in 'off' state, the D-mode power devices will be guaranteed their fail-safe operation as long as the converter is isolated from LV-side voltage supply before the $S_{bot}$ is turned 'on'. On the other hand, if the $t_{frame(min)}$ is determined by the GDSFP parameters on $S_{bot}$ and the $S_{dc,HV}$ and $S_{dc,LV}$ switches are not turned off within $t_{frame(min)}$, then the $S_{bot}$ device will be driven into deep I-V saturation mode that may lead to catastrophic device failure if the converter is not isolated within a short period of time.




(a)




(b)

*Figure 5-29: Boost DC-DC converter waveforms under -$V_{SS}$ fault events for (a) $t_{frame(Sbot)} < t_{dc,iso(HV/LV)} < t_{frame(Stop)}$ and (b) ) $t_{frame(Stop)} < t_{dc,iso(HV/LV)} < t_{frame(Sbot)}$*

## *5.9. Summary*

In this chapter, the fail-safe operation of bidirectional DC-DC converter with the DOCP and revised GDSFP topologies when shoot-through occurs and all power supplies fail was fully verified using PSpice simulation results.

The chapter then commenced with a mathematical analysis of the converter operation in both buck and boost-mode operation that led to the passive LC value required for a given current and voltage ripple specifications. This was followed by a detailed design procedure of an inductor with illustrations of magnetic core geometries that affects its design.

Subsequently, the calculation of power losses within the DC-DC converter, including switching loss, on-state conduction loss of the switching device and dc-link switches and DC copper loss within the inductor winding, were discussed in detail. In order to take the effect of device's junction temperature to its switching

and on-state conduction losses into account, an electrothermal simulation model that contained Cauer thermal network of the heat dissipation path was used for calculation of the converter's efficiency, which was determined to be higher than 98% at full load.

However, for its experimental demonstration, a significant level of noise introduced at the controller's input during normal operation has disrupted the circuit operation at a DC-link voltage level of above 300 V. This was directly attributed to the high dV/dt during the turn-on of the switching device that led to a considerable level of conducted EMI at the converter's input side logic circuit. Also, the ground potential of the input stage of dc-link switch gate drivers was tied to the same potential as the converter's input side logic circuit susceptible to dV/dt noise. To ensure reliable converter operation without halting unexpectedly, two possible mitigation strategies were proposed: to isolate the ground point of input stage of dc-link gate drivers from that of the converter's logic circuit and to re-configure the controller to hold the previous input signal from the controller during the 'blanking time' period corresponding to the device turn-on and then receive the signal after that period has passed.

As an alternative option to hardware demonstration, a PSpice simulator was used for replicating the circuit parameters and protection circuitry designs and simulating the circuit behaviours and thus verifying fail-safe operation of D-mode PSJ devices under gate supply removal / failure events. For building the circuit model with PSJ devices, an average GaN-PSJ behavioural model was created, implemented in the circuit simulation and compared against its typical experimental waveforms. The comparison has clearly shown that the proposed model lacks accuracy in its transient turn-on and turn-off behaviours. The possible reasons for

this discrepancy and scope for future work has also been addressed in the chapter. Also, the fault cases where the fail-safe operation of D-mode DC-to-DC power converters is guaranteed or not were clearly identified and addressed.

# 6 Concluding Remarks and Future Work

## *6.1. Concluding remarks*

This thesis has covered the material physics of GaN and fundamentals of lateral GaN-HEMT power device technology in order to establish the physical context of GaN devices before proceeding onto the detailed discussion of PSJ device technology.

The first introduction chapter of the thesis provides a brief overview of the key driving factors towards more electric aircraft (MEA) system and exploitation of wide band-gap semiconductor device technologies including SiC and GaN for next-generation power electronics applications.

The second chapter discusses intrinsic material properties of GaN including spontaneous and piezoelectric polarization and their origins in detail. Then, the operating principles of the conventional lateral GaN-HEMTs was presented. The current collapse phenomenon present in conventional GaN-HEMTs and its mitigation via Field-plate structure were discussed in detail. This was then followed by an overview of conventional E-mode GaN device technologies adopted so far including p-type GaN, recessed-gate and Flouride ($F^-$)-ion implantation and cascode configuration. The chapter also gives introduction to a recently adopted Polarisation Super-junction (PSJ) concept that yields lateral GaN transistors with much higher breakdown voltage compared to its conventional counterparts.

In third chapter, the static on-state and switching characteristics of the new large-area PSJ-FET samples are presented. The discussion commenced with the evaluation of on-state I-V characteristics of the PSJ sample at temperatures ranging from room temperature to $150^0$C. This was followed by discussion of methodology

used for extracting the Capacitance – Voltage (C-V) characteristics of PSJ device, qualitative reasoning to the change in its Miller capacitance with $V_{gs}$ and $V_{ds}$ and its effect towards the switching performance. Due to the formation of 2DEG and 2DHG along the top GaN/AlGaN and bottom AlGaN/GaN heterointerfaces, a parallel plate capacitor is formed along the channel between gate and drain electrodes, which led to a remarkable increase in $C_{gd}$ with $V_{gs}$ when $V_{ds}$ = 0V. As $V_{ds}$ increases, the 2DEG and 2DHG are depleted at the drain edge and thus a depletion-layer capacitor is formed; therefore, $C_{gd}$ decreases drastically. The experimental setup of double pulse test (DPT) for PSJ device was then presented, followed by the discussion of its turn-on and turn-off characteristics at various gate resistance and temperature values extracted by DPT. Due to its unique $C_{gd}$ characteristics, the turn-on dV/dt of the PSJ transistor was slowed down as $V_{ds}$ decreased. During the turn-off transition, however, the load current was diverted away from the device under test (DUT) for charging the diode junction capacitances, which led to a drastic decrease in turn-off energy loss. This chapter was concluded with the comparison of on-state and switching characteristics of E-mode cascode PSJ device against their D-mode counterparts.

In fourth chapter, a brief overview of the fail-safe gate driver scheme for D-mode power devices proposed so far was presented initially. The D-mode devices inherently face critical safety concerns when the gate drive voltage supplies fail as both devices in a half-bridge circuit will be turned on and thus shoot-through event will occur. Also, shoot-through events may occur during normal operation due to controller faults and therefore must be mitigated. A new fail-safe gate driver circuit based on previous work is then presented and its operation principle and difference from the previous solution is clearly discussed in detail. The functionality of the

proposed circuit is verified via PSpice simulation and its prototype circuit layout was designed for hardware verification with the same components as for the simulation. Both the simulation and hardware test results demonstrate that the circuit presented in this chapter can ensure fail-safe operation of D-mode PSJ transistors, which can pave way for its application in power electronics.

In the fifth chapter, the fail-safe operation of bidirectional DC-DC converter using D-mode power devices with protection schemes was demonstrated by PSpice simulation. Then, the operating principle of the converter and its detailed design procedure including output LC filter design, heatsink selection, have been discussed in detail. Subsequently, by using the electrothermal model that incorporates Cauer thermal RC network to consider the effect of junction temperature, the power converter's efficiency was calculated to be above 98% for the output load range from 25% to its full rating. The conducted EMI issues that caused unwanted circuit behaviour at dc-link voltage levels above 300 V were identified and its possible remedies have been proposed.

## *6.2. Future Work*

The research presented in this thesis could be the foundation for performance evaluation of the latest PSJ devices and power converter designs with PSJ GaN devices and development of protection system for D-mode power devices. The following section summarises the key area of future work.

1. **Characterisation of multiple large-area PSJ devices:** As discussed in Section 5.7, the measured $C_{gs}$-$V_{gs}$ and $C_{gd}$-$V_{gs}$ characteristics of five PSJ transistor samples showed remarkable deviation from each other, which may lead to a

significant variation in their switching characteristics. Therefore, the same tests that were performed in this work shall be repeated for multiple number of PSJ device samples to observe how much variance exists between them.

2. **Paralleling of GaN devices and/or converters:**

The current rating of the large-area PSJ device used for this research was only up to 8 A, whilst the loads in aerospace and automotive applications will typically draw much higher level of current. Therefore, it is necessary to parallel multiple number of devices or converters if feasible.

However, paralleling of devices will pose significant challenges in terms of PCB layout as dynamic current sharing becomes the key to prevent heating up one device more than the others. Alternatively, the converters may be paralleled via interleaved configuration so that paralleling of devices and thus PCB layout challenges associated with it can be avoided. Nevertheless, a means of active current sharing must be implemented as they will be inherently imbalanced due to the variations between the components and duty cycles.

3. **Power converter design using cascode PSJ devices:**

The DC-DC converter can also be designed using E-mode cascode PSJ devices that will eliminate the need for GDSFP scheme and dc-link switches. However, their current ratings are smaller than their D-mode counterpart as their $V_{gs}$ is below 0 V and thus the device is not fully enhanced. This, in turn, will lead to a need for paralleling of devices and/or converters to achieve the same current rating as their standalone D-mode counterparts, which will pose challenges as aforementioned.

4. **Monolithic integration of the fail-safe gate drive scheme:**

Although the full functionality of GDSFP and DOCP schemes have been verified by simulation and experiment, their implementation led to a much larger PCB footprint and area required, which makes the solution less favorable compared to using standalone E-mode devices with no protection schemes. However, if the whole solution can be monolithically integrated into one chip, then the cost and area required for implementing them may be reduced significantly.

**5. Safe Operating Area (SOA) of PSJ devices:**

Although it was proven that the proposed DOCP scheme was capable of clearing out the shoot-through current within 1.5 µs of its occurrence at 700 V dc by experiment, the PSJ device went into irreversible breakdown when it was subject to a shoot-through current and a dc-link voltage of 800 V. This may indicate that it has exceeded its SOA, which needs further investigation in the future.

**6. Resonant converter topology with ZVS/ZCS operation:**

As clearly seen from the typical turn-on characteristics of the PSJ device in Section 3.1.3.5, the turn-on dV/dt was severely limited as $C_{gd}$ increased exponentially with the decrease in $V_{ds}$ when the device is in its 'on' state, which will severely degrade converters's efficiencies when they are switched at high frequencies i.e. > 100 kHz. Furthermore, a large EMI noise was coupled to the dc-link switch gate driver input at the turn-on events and thus disturbed steady-state operation of the converter as discussed in Section 5.6. To mitigate these issues, a shift to resonant converter topologies with zero-voltage switching (ZVS) or zero-current switching (ZCS) operation may be a viable option for PSJ

devices. However, this will require a more sophisticated PWM control strategy and additional LC components and thus weight and volume to create resonance.

**7. Passive component designs for high-frequency circuits:**

The lumped parasitic capacitance is present between the coil windings within the filter inductor, which is effectively placed in parallel to the inductor. This leads to the internal resonance where the inductor behaves as a capacitor if the frequency exceeds its 'self-resonant frequency' value [134]. At this range of frequency, converter operation may become unstable. A modification in the inductor winding design is required so that they are capable of dealing with high frequencies and thus the reliability of converter operation would be improved.

**8. Fault-tolerant control (FTC) design for power converters:**

Although efforts to prevent faults and hence improve system reliability are required, it is also important to ensure that the system can maintain its performance as close as possible to the desirable level when its component fails. According to [135], the flight control is one of the applications where minor component faults lead to catastrophic incidents and hence tolerating the system component's malfunction whilst maintaining its desirable performance and stability is the key requirement.

# 7 Appendix

## *7.1. Large-area PSJ-FET epilayer specifications*

The materials and thicknesses of epilayers of the POWDEC's large-area PSJ transistors provided for this research work are presented in Table 7-1.

| Layer | Thickness (nm) | Dopant | Concentration ($cm^{-3}$) |
|---|---|---|---|
| p-GaN | 3 | Mg | $2 \times 10^{20}$ |
| p-GaN | 60 | Mg | $5 \times 10^{19}$ |
| i-GaN | 65 | --- | --- |
| i-AlGaN | 40 | --- | --- |
| i-GaN | 800 | --- | --- |

*Table 7-1: Materials, thicknesses, dopants and doping concentrations of the epi-layers of the large-area PSJ-FETs ($L_{psj}$ = 40 µm, $W_g$ = 148 mm)*

## *7.2. Analysis of switching transients in double pulse test circuit*

This is a modified version of mathematical switching loss model proposed in [136] for diodes with reverse recovery charge. This model was adapted for Schottky diodes that has zero reverse recovery charge stored in their junction.

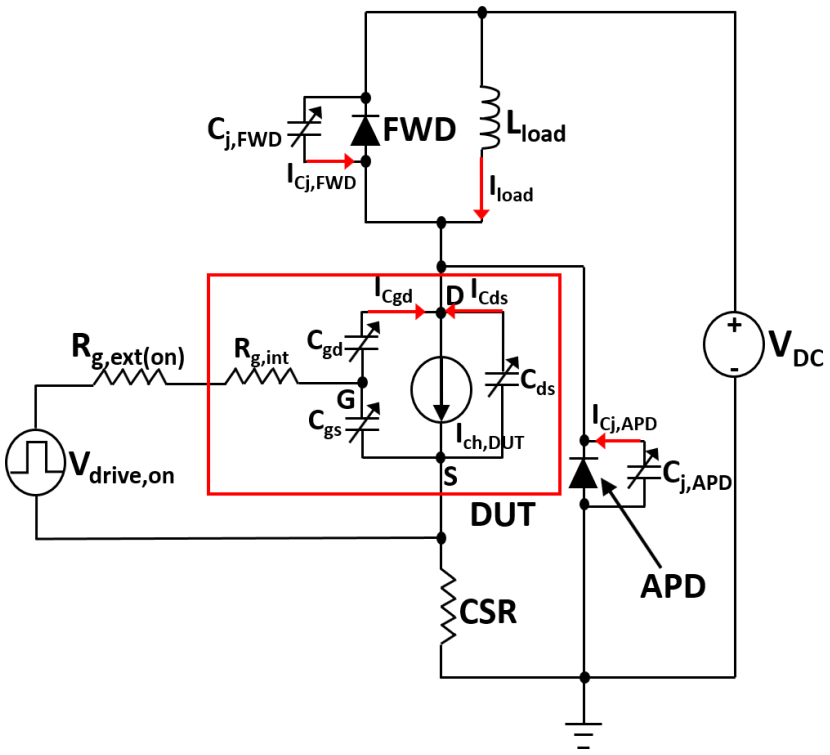



*Figure 7-1: Current flow direction in DPT circuit during DUT turn-on period*

**1. Turn-on delay interval:**

When the turn-on gate drive signal $V_{drv,on}$ is applied through $R_{g,ext(on)}$ and $R_{g,int}$ of the DUT, the DUT input capacitance ($C_{iss}$) is charged up. Unless the $V_{gs}$ of exceeds the turn-on threshold value $V_{th}$, the DUT will remain in its off state; thus, $I_{load}$ still flows through the freewheeling diode (FWD) and the effect of $L_S$ due to the change in $I_D$ can be ignored. The $V_{gs}$ (t) during this period is given by:

$$V_{gs}(t) = V_{drv,on} - \left(V_{drv,on} - V_{gs}(0)\right) \cdot e^{-\frac{t}{\tau_{iss}}} \quad \ldots(7\text{-}1)$$

Where $\tau_{iss} = R_{g,tot(on)} \cdot \left(C_{gd} + C_{gs}\right)$

**2. Drain current rise interval:**

From the point where $V_{gs}$ reaches $V_{gs,th}$, the DUT starts to turn on and its drain current ($I_d$) will start to rise. During this period, the gate current can be expressed as the sum of current through $C_{gs}$ and $C_{gd}$:

$$I_g(t) = C_{gs}\frac{dV_{gs}(t)}{dt} + C_{gd}\frac{dV_{gd}(t)}{dt} \quad \ldots(7\text{-}2)$$

The $I_g$ is also determined by the total turn-on gate loop resistance ($R_{g,tot(on)}$) presented, the turn-off drive voltage ($V_{drive,off}$), common source inductance ($L_S$) and the source current slew rate ($dI_D/dt$) and therefore the following equation is derived:

$$C_{gs}\cdot\frac{dV_{gs}(t)}{dt} + C_{gd}\cdot\frac{dV_{gd}(t)}{dt} = \frac{V_{drv,on} - V_{gs}(t) - L_S\cdot\frac{dI_S(t)}{dt}}{R_{g,tot(on)}} \quad \ldots(7\text{-}3)$$

During this period, the $V_{ds}$ decreases by the voltage drop induced by the rising $I_D$ across the parasitic inductances in the power loop:

$$V_{ds}(t) = V_{dc} - (L_D + L_S)\cdot\frac{dI_d(t)}{dt} \quad \ldots(7\text{-}4)$$

For simplicity, it is assumed that the current through capacitances $C_{gd}$ and $C_{ds}$ is much smaller than $I_D$. Therefore:

$$I_D(t) = g_m\cdot\left(V_{gs}(t) - V_{th}\right) \quad \ldots(7\text{-}5)$$

$$I_S(t) = I_D(t) + C_{gs}\cdot\frac{dV_{gs}(t)}{dt} \quad \ldots(7\text{-}6)$$

$$V_{gd}(t) = V_{gs}(t) - V_{ds}(t) \quad \ldots(7\text{-}7)$$

By substituting equations …(*7-4*)~(*7-7*) into …(*7-3*) and then applying Laplace transformation, the transfer function $V_{gs}(s)$ can be obtained as:

$$\therefore V_{gs}(s) = \frac{V_{drv,on}}{s} - (V_{drv,on} - V_{th})\cdot\frac{\tau_2 s + \tau_1}{\tau_2 s^2 + \tau_1 s + 1} \quad \ldots(7\text{-}8)$$

Where:

$$\tau_2 = (L_D + L_S)\cdot C_{gd}\cdot R_{g,tot}\cdot g_m + L_S\cdot C_{gs}$$

$$\tau_1 = R_{g,tot}\cdot\left(C_{gd} + C_{gs}\right) + g_m\cdot L_S$$

By applying inverse Laplace transformation to the $V_{gs}(s)$ above, the $V_{gs}(t)$ in time domain can be obtained accordingly. However, the resultant expression for $V_{gs}(t)$ will be different for overdamped $(\tau_1{}^2 - 4\tau_2 > 0)$ and underdamped conditions $(\tau_1{}^2 - 4\tau_2 < 0)$.

**Case I: Overdamped condition $(\tau_1{}^2 - 4\tau_2 > 0)$:**

$$\therefore V_{gs}(t) = V_{drv,on} - \left(V_{drv,on} - V_{th}\right) \cdot \left( e^{-\frac{\tau_1}{2\tau_2}t} \cosh\left(\frac{\sqrt{\tau_1{}^2 - 4\tau_2}}{2\tau_2}t\right) + \frac{\tau_1}{\sqrt{\tau_1{}^2 - 4\tau_2}} e^{-\frac{\tau_1}{2\tau_2}t} \sinh\left(\frac{\sqrt{\tau_1{}^2 - 4\tau_2}}{2\tau_2}t\right)\right) \quad \ldots(7\text{-}9)$$

$$\therefore I_d(t) = g_m\left(V_{drv,on} - V_{th}\right) - g_m \cdot \left(V_{drv,on} - V_{th}\right) \cdot \left( e^{-\frac{\tau_1}{2\tau_2}t} \cosh\left(\frac{\sqrt{\tau_1{}^2 - 4\tau_2}}{2\tau_2}t\right) + \frac{\tau_1}{\sqrt{\tau_1{}^2 - 4\tau_2}} e^{-\frac{\tau_1}{2\tau_2}t} \sinh\left(\frac{\sqrt{\tau_1{}^2 - 4\tau_2}}{2\tau_2}t\right)\right) \quad \ldots(7\text{-}10)$$

$$\therefore V_{ds}(t) = V_{DC} - \frac{2 \cdot g_m \cdot (L_D + L_S) \cdot \left(V_{drv,on} - V_{th}\right)}{\sqrt{\tau_1{}^2 - 4\tau_2}} e^{-\frac{\tau_1}{2\tau_2}t} \sinh\left(\frac{\sqrt{\tau_1{}^2 - 4\tau_2}}{2\tau_2}t\right) \quad \ldots(7\text{-}11)$$

**Case II: Underdamped condition $(\tau_1{}^2 - 4\tau_2 < 0)$:**

$$\therefore V_{gs}(t) = V_{drv,on} - \left(V_{drv,on} - V_{th}\right) \cdot \left( e^{-\frac{\tau_1}{2\tau_2}t} \cos\left(\frac{\sqrt{4\tau_2 - \tau_1{}^2}}{2\tau_2}t\right) + \frac{\tau_1}{\sqrt{\tau_1{}^2 - 4\tau_2}} e^{-\frac{\tau_1}{2\tau_2}t} \sin\left(\frac{\sqrt{4\tau_2 - \tau_1{}^2}}{2\tau_2}t\right)\right) \quad \ldots(7\text{-}12)$$

$$\therefore I_D(t) = g_m \cdot \left(V_{drv,on} - V_{th}\right) \cdot \left( 1 - e^{-\frac{\tau_1}{2\tau_2}t} \left( \cos\left(\frac{\sqrt{4\tau_2 - \tau_1{}^2}}{2\tau_2}t\right) + \frac{\tau_1}{\sqrt{\tau_1{}^2 - 4\tau_2}} \sin\left(\frac{\sqrt{4\tau_2 - \tau_1{}^2}}{2\tau_2}t\right)\right)\right) \quad \ldots(7\text{-}13)$$

$$\therefore V_{ds}(\mathrm{t}) = V_{DC} - \frac{2 \cdot (L_D + L_S) \cdot g_m \cdot \left(V_{drv,on} - V_{th}\right)}{\sqrt{4\tau_2 - {\tau_1}^2}} e^{-\frac{\tau_1}{2\tau_2}t} \sin\left(\frac{\sqrt{4\tau_2 - {\tau_1}^2}}{2\tau_2}t\right)$$

…(7-14)

### 3. Drain voltage fall time I:

As the $I_D$ has reached the full $I_{load}$, the polarity of the FWD current will be reversed so that its junction capacitance ($C_{j,FWD}$) is charged via DUT channel current ($I_{ch,DUT}$). The output capacitance ($C_{oss}$) of DUT and junction capacitance of the APDs ($C_{j,APD}$) will also be charged via $I_{ch,DUT}$, which yields the following set of equations:

$$g_m \cdot \left(V_{gs}(t) - V_{th}\right) = I_{load} - C_{node,tot} \cdot \frac{dV_{ds}(t)}{dt} \quad \text{…(7-15)}$$

$$\frac{V_{drv,on} - V_{gs}(t) - L_S \cdot \frac{dI_S(t)}{dt}}{R_{g,tot(on)}} = C_{gs} \cdot \frac{dV_{gs}(t)}{dt} + C_{gd} \cdot \left(\frac{dV_{gs}(t)}{dt} - \frac{dV_{ds}(t)}{dt}\right) \quad \text{…(7-16)}$$

$$I_S(t) = g_m \cdot \left(V_{gs}(t) - V_{th}\right) + C_{ds} \cdot \frac{dV_{ds}(t)}{dt} + C_{gs} \cdot \frac{dV_{gs}(t)}{dt} \quad \text{…(7-17)}$$

$$I_D(t) = I_S(t) - \left(C_{gd} + C_{gs}\right) \cdot \frac{dV_{gs}(t)}{dt} + C_{gd} \cdot \frac{dV_{ds}(t)}{dt} \quad \text{…(7-18)}$$

By substituting the expression for $\frac{dV_{ds}(t)}{dt}$ in (7-12) into (7-14) and then substituting $I_S$(t) to (7-13), the following equation can be derived:

$$I_S(t) = L_S \cdot C_{gs} \frac{d^2V_{gs}(t)}{dt^2} + \left(R_{g,tot(on)}\left(C_{gd} + C_{gs}\right) + L_S g_m \left(1 - \frac{C_{ds}}{C_{node,tot}}\right)\right) \cdot \frac{dV_{gs}(t)}{dt}$$

$$+ \left(\frac{R_g C_{gd} g_m}{C_{node,tot}} + 1\right) \cdot V_{gs}(t) = V_{drv,on} + \frac{R_{g,tot(on)} \cdot C_{gd} \cdot (g_m V_{th} + I_{load})}{C_{node,tot}}$$

…(7-19)

As a result, the transfer function $V_{gs}$(s) is derived as the following:

$$\therefore V_{gs}(s) = \frac{\tau_c}{\tau_0} \cdot \frac{1}{s} - \left(\frac{\tau_c}{\tau_0} - V_{gs,mil}\right) \cdot \frac{\tau_2 s + \tau_1}{\tau_2 s^2 + \tau_1 s + \tau_0} \quad \text{…(7-20)}$$

Where:

$$\tau_2 = L_S \cdot C_{gs}$$

$$\tau_1 = R_{g,tot(on)}\left(C_{gd} + C_{gs}\right) + L_S g_m \left(1 - \frac{C_{ds}}{C_{node,tot}}\right)$$

$$\tau_0 = \left(\frac{R_g C_{gd} g_m}{C_{node,tot}} + 1\right)$$

$$\tau_c = V_{drv,on} + \frac{R_{g,tot(on)} C_{gd} g_m V_{gs,mil}}{C_{node,tot}}$$

**Case 1: Overdamped condition ($\tau_1{}^2 - 4\tau_2 > 0$):**

$$\therefore V_{gs}(t) = \frac{\tau_c}{\tau_0}$$

$$- \left(\frac{\tau_c}{\tau_0} - V_{gs,mil}\right) \cdot \left( e^{-\frac{\tau_1}{2\tau_2} t} \cosh\left(\frac{\sqrt{\tau_1{}^2 - 4\tau_2\tau_0}}{2\tau_2} t\right) + \frac{\tau_1}{\sqrt{\tau_1{}^2 - 4\tau_2\tau_0}} e^{-\frac{\tau_1}{2\tau_2} t} \sinh\left(\frac{\sqrt{\tau_1{}^2 - 4\tau_2\tau_0}}{2\tau_2} t\right)\right)$$

…(7-21)

$$\therefore V_{ds}(t) = \frac{g_m \left(V_{gs,mil} - \frac{\tau_c}{\tau_0}\right)}{C_{node,tot}} \cdot t$$

$$+ \frac{g_m}{C_{node,tot}} \left(\frac{\tau_c}{\tau_0} - V_{gs,mil}\right) \cdot \left( e^{-\frac{\tau_1 - \sqrt{\tau_1{}^2 - 4\tau_2\tau_0}}{2\tau_2} t} \left(\frac{\tau_2\left(\tau_1 + \sqrt{\tau_1{}^2 - 4\tau_2\tau_0}\right)}{\tau_1{}^2 - 4\tau_2\tau_0 - \tau_1\sqrt{\tau_1{}^2 - 4\tau_2\tau_0}}\right) + e^{-\frac{\tau_1 + \sqrt{\tau_1{}^2 - 4\tau_2\tau_0}}{2\tau_2} t} \left(\frac{\tau_2\left(\tau_1 - \sqrt{\tau_1{}^2 - 4\tau_2\tau_0}\right)}{\tau_1{}^2 - 4\tau_2\tau_0 - \tau_1\sqrt{\tau_1{}^2 - 4\tau_2\tau_0}}\right)\right) + V_C$$

…(7-22)

$$\therefore I_D(t) = g_m \cdot \left(1 - \frac{C_{gd} + C_{ds}}{C_{node,tot}}\right) \cdot \left(\frac{\tau_c}{\tau_0} - \left(\frac{\tau_c}{\tau_0} - V_{gs,mil}\right)\right.$$

$$\left. \cdot \left(e^{-\frac{\tau_1}{2\tau_2}t}\left(\cosh\left(\frac{\sqrt{{\tau_1}^2 - 4\tau_2\tau_0}}{2\tau_2}t\right) + \frac{\tau_1}{\sqrt{{\tau_1}^2 - 4\tau_2\tau_0}}\sinh\left(\frac{\sqrt{{\tau_1}^2 - 4\tau_2\tau_0}}{2\tau_2}t\right)\right) - V_{th}\right)\right)$$

$$+ \frac{C_{gd} + C_{ds}}{C_{node,tot}} \cdot I_{load} + \frac{2C_{gd}\tau_0\left(\frac{\tau_c}{\tau_0} - V_{gs,mil}\right)}{\sqrt{{\tau_1}^2 - 4\tau_2\tau_0}} \cdot e^{-\frac{\tau_1}{2\tau_2}t} \cdot \sinh\left(\frac{\sqrt{{\tau_1}^2 - 4\tau_2\tau_0}}{2\tau_2}t\right)$$

…(7-23)

**Case II: Underdamped Condition ($\boldsymbol{{\tau_1}^2 - 4\tau_2 < 0}$):**

$$\therefore V_{gs}(t) = \frac{\tau_c}{\tau_0}$$

$$- \left(\frac{\tau_c}{\tau_0} - V_{gs,mil}\right) \cdot \left(e^{-\frac{\tau_1}{2\tau_2}t}\cos\left(\frac{\sqrt{4\tau_2\tau_0 - {\tau_1}^2}}{2\tau_2}t\right) + \frac{\tau_1}{\sqrt{4\tau_2\tau_0 - {\tau_1}^2}}e^{-\frac{\tau_1}{2\tau_2}t}\sin\left(\frac{\sqrt{4\tau_2\tau_0 - {\tau_1}^2}}{2\tau_2}t\right)\right)$$

…(7-24)

$$\therefore I_D(t) = g_m \cdot \left(1 - \frac{C_{gd} + C_{ds}}{C_{node,tot}}\right) \cdot \left(\frac{\tau_c}{\tau_0} - \left(\frac{\tau_c}{\tau_0} - V_{gs,mil}\right)\right.$$

$$\left. \cdot \left(e^{-\frac{\tau_1}{2\tau_2}t}\left(\cos\left(\frac{\sqrt{4\tau_2\tau_0 - {\tau_1}^2}}{2\tau_2}t\right) + \frac{\tau_1}{\sqrt{4\tau_2\tau_0 - {\tau_1}^2}}\sin\left(\frac{\sqrt{4\tau_2\tau_0 - {\tau_1}^2}}{2\tau_2}t\right)\right) - V_{th}\right)\right)$$

$$+ \frac{C_{gd} + C_{ds}}{C_{node,tot}} \cdot I_{load} + \frac{2C_{gd}\tau_0\left(\frac{\tau_c}{\tau_0} - V_{gs,mil}\right)}{\sqrt{4\tau_2\tau_0 - {\tau_1}^2}} \cdot e^{-\frac{\tau_1}{2\tau_2}t} \cdot \sin\left(\frac{\sqrt{4\tau_2\tau_0 - {\tau_1}^2}}{2\tau_2}t\right)$$

…(7-25)

$$\therefore V_{ds}(t) = \frac{g_m\left(V_{gs,mil} - \frac{\tau_c}{\tau_0}\right)}{C_{node,tot}} \cdot t - \frac{g_m\left(\frac{\tau_c}{\tau_0} - V_{gs,mil}\right)}{C_{node,tot}}$$

$$\cdot \left(\frac{\tau_1}{\tau_0}e^{-\frac{\tau_1}{2\tau_2}t}\cos\left(\frac{\sqrt{4\tau_2\tau_0 - {\tau_1}^2}}{2\tau_2}t\right) + \frac{4\tau_2\tau_0 - 2{\tau_1}^2}{2\tau_0\sqrt{4\tau_2\tau_0 - {\tau_1}^2}}e^{-\frac{\tau_1}{2\tau_2}t}\sin\left(\frac{\sqrt{4\tau_2\tau_0 - {\tau_1}^2}}{2\tau_2}t\right)\right)$$

…(7-26)

**4. Drain voltage fall time II:**

When $V_{ds}(t) = V_{ds,sat}$ the DUT starts to enter its ohmic I-V region. From this point, the $C_{iss}$ of the DUT is charged via gate current and thus $V_{gs}$ will rise towards $V_{drv,on}$ exponentially and $V_{ds}$ falls towards $V_{ds,on}$.

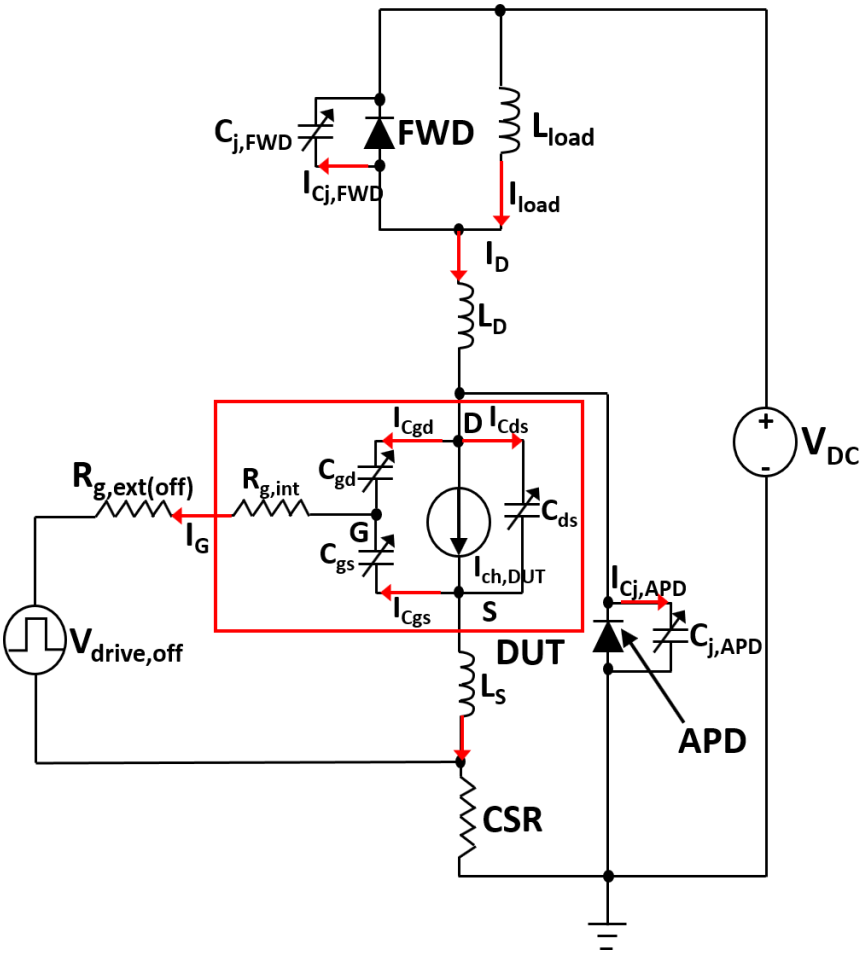



*Figure 7-2: Current flow direction in DPT circuit during DUT turn-off period*

The gate current ($I_G$) during this time interval is a combination of discharging currents through $C_{gd}$ and $C_{gs}$ and thus can be expressed as:

$$I_G(t) = -C_{gs}\frac{dV_{gs}(t)}{dt} - C_{gd}\frac{dV_{gd}(t)}{dt} \quad \ldots(7\text{-}27)$$

The $I_G$ is also determined by the total turn-off gate loop resistance ($R_{g,tot(off)}$) presented, the turn-off drive voltage ($V_{drive,off}$), common source inductance ($L_S$) and the source current slew rate ($dI_D/dt$) and therefore the following equation is derived:

$$-C_{gs}\frac{dV_{gs}(t)}{dt} - C_{gd}\frac{dV_{gd}(t)}{dt} = \frac{V_{gs}(t) - V_{drive,off} + L_S \cdot \frac{dI_S(t)}{dt}}{R_{g,tot(off)}} \quad \ldots(7\text{-}28)$$

Since $V_{gd}(t) = V_{gs}(t) - V_{ds}(t)$:

$$-\left(C_{gd} + C_{gs}\right) \cdot \frac{dV_{gs}(t)}{dt} + C_{gd} \cdot \frac{dV_{ds}(t)}{dt} = \frac{V_{gs}(t) - V_{drive,off} + L_S \cdot \frac{dI_S(t)}{dt}}{R_{g,tot(off)}} \quad \ldots(7\text{-}29)$$

During the drain voltage rise interval ($t_{Vds,rise}$), the $I_{load}$ is partially diverted away from $I_{ch,DUT}$ in order to charge the capacitances in DUT, APD and FWD. The current through $C_{ds}$ of DUT, $C_{j,APD}$ and $C_{j,FWD}$ is proportional to the ratio between each capacitance value and $C_{gd}$ and the sum of the charging currents through all capacitances is equivalent to the difference between $I_{load}$ and $I_{ch,DUT}$. This yields the following set of differential equations as following:

$$I_D(t) = g_m\left(V_{gs}(t) - V_{th}\right) - C_{gd}\frac{dV_{gs}(t)}{dt} + \left(C_{gd} + C_{ds}\right)\frac{dV_{ds}(t)}{dt} \quad \ldots(7\text{-}30)$$

$$I_S(t) = I_D(t) + C_{gd} \cdot \left(\frac{dV_{gs}(t)}{dt} - \frac{dV_{ds}(t)}{dt}\right) + C_{gs} \cdot \frac{dV_{gs}(t)}{dt} \quad \ldots(7\text{-}31)$$

$$g_m\left(V_{gs}(t) - V_{th}\right) + C_{node,tot}\frac{dV_{ds}(t)}{dt} - C_{gd}\frac{dV_{gs}(t)}{dt} = I_{load} \quad \ldots(7\text{-}32)$$

Where $C_{node,tot} = C_{gd} + C_{ds} + C_{j,FWD} + C_{j,APD}$.

Therefore, the relationship between $dV_{ds}/dt$ and $dV_{gs}/dt$ can be derived as:

$$\therefore \frac{dV_{ds}(t)}{dt} = \frac{I_{load} + C_{gd} \cdot \frac{dV_{gs}}{dt} - g_m \cdot \left(V_{gs}(t) - V_{th}\right)}{C_{node,tot}} \quad \ldots(7\text{-}33)$$

By substituting this to the equation, the following equation is obtained:

$$L_S\left(C_{gs}+\frac{C_{ds}\cdot C_{gd}}{C_{node,tot}}\right)\frac{d^2V_{gs}(t)}{dt^2}$$

$$+\left(R_{g,tot(off)}\left(C_{gd}+C_{gs}\right)-\frac{R_{g,tot(off)}\cdot {C_{gd}}^2}{C_{node}}+\frac{C_{gd}}{C_{node}}+L_S\cdot g_m\left(1-\frac{C_{ds}}{C_{node,tot}}\right)\right)\frac{dV_{gs}(t)}{dt}$$

$$+\left(1+\frac{C_{gd}\cdot g_m\cdot R_{g,tot(off)}}{C_{node,tot}}\right)V_{gs}(t)=\frac{C_{gd}\cdot R_{g,tot(off)}}{C_{node,tot}}(I_{load}+g_mV_{th})+V_{drive,off}$$

…(7-34)

This differential equation can be solved by applying Laplace transformation on both sides, from which the transfer function $V_{gs}$ (s) is derived as:

$$\therefore V_{gs}(s)=\frac{V_{gs}(0)\cdot(\tau_2 s+\tau_1)+\frac{\tau_c}{s}}{\tau_2 s^2+\tau_1 s+\tau_0}$$

…(7-35)

Where:

$$\tau_2=L_S\cdot\left(C_{gs}+\frac{C_{ds}\cdot C_{gd}}{C_{node,tot}}\right)$$

$$\tau_1=R_{g,tot(off)}\cdot\left(C_{gd}+C_{gs}\right)-\frac{R_{g,tot(off)}\cdot {C_{gd}}^2}{C_{node}}+\frac{C_{gd}}{C_{node}}+L_S\cdot g_m\left(1-\frac{C_{ds}}{C_{node,tot}}\right)$$

$$\tau_0=1+\frac{C_{gd}\cdot g_m\cdot R_{g,tot(off)}}{C_{node,tot}}$$

$$\tau_c=\frac{C_{gd}\cdot R_{g,tot(off)}}{C_{node,tot}}(I_{load}+g_mV_{th})+V_{drive,off}$$

$V_{gs}(0)$ = initial value of $V_{gs}$(t) at t=0.

In this case, the initial value $V_{gs}$(0) will be $V_{gs,mil}=\frac{I_{load}}{g_m}+V_{th}$ as the DUT enters its I-V saturation region. By taking the partial fraction in $V_{gs}$(s):

$$V_{gs}(s) = \frac{\tau_c}{\tau_0} \cdot \frac{1}{s}$$

$$- \left(\frac{\tau_c}{\tau_0} - V_{gs,mil}\right) \cdot \left( \frac{s + \frac{\tau_1}{2\tau_2}}{\left(s + \frac{\tau_1}{2\tau_2}\right)^2 - \frac{{\tau_1}^2 - 4\tau_2\tau_0}{4{\tau_2}^2}} - \frac{\tau_1}{\sqrt{{\tau_1}^2 - 4\tau_2\tau_0}} \cdot \frac{\frac{\sqrt{{\tau_1}^2 - 4\tau_2\tau_0}}{2\tau_2}}{\left(s + \frac{\tau_1}{2\tau_2}\right)^2 - \frac{{\tau_1}^2 - 4\tau_2\tau_0}{4{\tau_2}^2}} \right)$$

…(7-36)

By applying inverse Laplace transformation to the $V_{gs}(s)$ above, the $V_{gs}(t)$ can be obtained accordingly. However, the resultant expression for $V_{gs}(t)$ will be different for overdamped (${\tau_1}^2 - 4\tau_2\tau_0 > 0$) and underdamped conditions (${\tau_1}^2 - 4\tau_2\tau_0 < 0$). In the overdamped case, it is derived as the following:

$$\therefore V_{gs}(t) = \frac{\tau_c}{\tau_0} - \left(\frac{\tau_c}{\tau_0} - V_{gs,mil}\right) \cdot e^{-\frac{\tau_1}{2\tau_2}t}$$

$$\cdot \left( \cosh\left(\frac{\sqrt{{\tau_1}^2 - 4\tau_2\tau_0}}{2\tau_2}t\right) + \frac{\tau_1}{\sqrt{{\tau_1}^2 - 4\tau_2\tau_0}} \sinh\left(\frac{\sqrt{{\tau_1}^2 - 4\tau_2\tau_0}}{2\tau_2}t\right) \right)$$

…(7-37)

For the underdamped case:

$$\therefore V_{gs}(t) = \frac{\tau_c}{\tau_0} - \left(\frac{\tau_c}{\tau_0} - V_{gs,mil}\right) \cdot e^{-\frac{\tau_1}{2\tau_2}t}$$

$$\cdot \left( \cos\left(\frac{\sqrt{4\tau_2\tau_0 - {\tau_1}^2}}{2\tau_2}t\right) + \frac{\tau_1}{\sqrt{4\tau_2\tau_0 - {\tau_1}^2}} \sin\left(\frac{\sqrt{4\tau_2\tau_0 - {\tau_1}^2}}{2\tau_2}t\right) \right)$$

…(7-38)

The $V_{ds}(t)$ and $I_d(t)$ waveforms under overdamped condition can be obtained by substituting the expression for $V_{gs}(t)$ into equations (7-33) and (7-30), respectively:

$$\therefore V_{ds}(t) = \frac{\left(I_{load} - g_m\left(\frac{\tau_c}{\tau_0} - V_{th}\right)\right)\cdot t}{C_{node,tot}}$$

$$- \frac{\left(\frac{\tau_c}{\tau_0} - V_{gs,mil}\right)\cdot\left(C_{gd} + \frac{2\tau_2 g_m}{\tau_1 + \sqrt{{\tau_1}^2 - 4\tau_2\tau_0}}\right)\cdot e^{-\frac{\tau_1}{2\tau_2}t}\cosh\left(\frac{\sqrt{{\tau_1}^2 - 4\tau_2\tau_0}}{2\tau_2}t\right)}{C_{node,tot}}$$

$$- \frac{\left(\frac{\tau_c}{\tau_0} - V_{gs,mil}\right)\cdot\left(\frac{C_{gd}\tau_1}{\sqrt{{\tau_1}^2 - 4\tau_2\tau_0}} + \frac{2\tau_2\tau_1 g_m}{\tau_1\sqrt{{\tau_1}^2 - 4\tau_2\tau_0} - ({\tau_1}^2 - 4\tau_2\tau_0)}\right)\cdot e^{-\frac{\tau_1}{2\tau_2}t}\sinh\left(\frac{\sqrt{{\tau_1}^2 - 4\tau_2\tau_0}}{2\tau_2}t\right)}{C_{node,tot}}$$

$$- \frac{\frac{g_m}{2\tau_0}\cdot\left(\frac{\tau_c}{\tau_0} - V_{gs,mil}\right)\cdot\left(\tau_1\cdot e^{-\frac{\tau_1+\sqrt{{\tau_1}^2-4\tau_2\tau_0}}{2\tau_2}t} + \sqrt{{\tau_1}^2 - 4\tau_2\tau_0}\cdot e^{-\frac{\tau_1-\sqrt{{\tau_1}^2-4\tau_2\tau_0}}{2\tau_2}t}\right)}{C_{node,tot}}$$

…(7-39)

$$\therefore I_d(t) = -g_m\cdot\left(\frac{\tau_c}{\tau_0} - V_{gs,mil}\right)\cdot\left(1 + \frac{(C_{gd}+C_{ds})\tau_1\sqrt{{\tau_1}^2 - 4\tau_2\tau_0}}{2\tau_2\tau_0 C_{node,tot}}\right)\cdot e^{-\frac{\tau_1}{2\tau_2}t}\cosh\left(\frac{\sqrt{{\tau_1}^2 - 4\tau_2\tau_0}}{2\tau_2}t\right)$$
$$+ \left(\frac{\tau_c}{\tau_0} - V_{gs,mil}\right)\cdot\left(\left(\frac{C_{gd}+C_{ds}}{C_{node,tot}} - 1\right)\cdot\frac{2C_{gd}\tau_0}{\sqrt{{\tau_1}^2 - 4\tau_2\tau_0}\cdot 2\tau_2}\right.$$
$$+ g_m\cdot\left(\left(\frac{C_{gd}+C_{ds}}{C_{node,tot}}\right)\cdot\left(\frac{-\sqrt{{\tau_1}^2 - 4\tau_2\tau_0}}{\tau_1 + \sqrt{{\tau_1}^2 - 4\tau_2\tau_0}} + \frac{{\tau_1}^2}{\tau_1\sqrt{{\tau_1}^2 - 4\tau_2\tau_0} - ({\tau_1}^2 - 4\tau_2\tau_0)}\right) - \frac{\tau_1}{\sqrt{{\tau_1}^2 - 4\tau_2\tau_0}}\right)$$
$$\left. + \left(1 - \frac{C_{gd}+C_{ds}}{C_{node,tot}}\right)\cdot\frac{C_{gd}\sqrt{{\tau_1}^2 - 4\tau_2\tau_0}}{2\tau_2}\right)\cdot e^{-\frac{\tau_1}{2\tau_2}t}\sinh\left(\frac{\sqrt{{\tau_1}^2 - 4\tau_2\tau_0}}{2\tau_2}t\right)$$
$$- \frac{C_{gd}+C_{ds}}{C_{node,tot}}\cdot g_m\cdot\left(\frac{\tau_c}{\tau_0} - V_{gs,mil}\right)\cdot\left(-\frac{{\tau_1}^2 + \tau_1\sqrt{{\tau_1}^2 - 4\tau_2\tau_0}}{4\tau_2\tau_0}\cdot e^{-\frac{\tau_1+\sqrt{{\tau_1}^2-4\tau_2\tau_0}}{2\tau_2}t}\right.$$
$$\left. - \frac{\tau_1\sqrt{{\tau_1}^2 - 4\tau_2\tau_0} - {\tau_1}^2 + 4\tau_2\tau_0}{4\tau_2\tau_0}\cdot e^{-\frac{\tau_1-\sqrt{{\tau_1}^2-4\tau_2\tau_0}}{2\tau_2}t}\right) + g_m\cdot\left(\frac{\tau_c}{\tau_0} - V_{th}\right)\cdot\left(1 - \frac{C_{gd}+C_{ds}}{C_{node,tot}}\right) + \frac{C_{gd}+C_{ds}}{C_{node,tot}}$$
$$\cdot I_{load}$$

…(7-40)

The mathematical expressions for $V_{ds}(t)$ and $I_d(t)$ at underdamped condition (${\tau_1}^2 - 4\tau_2\tau_0 < 0$) can be derived using the same procedure.

## *7.3. FSM design for fail-safe converter control*

The schematic of the finite state machine (FSM) circuit that was designed and implemented on the Basys 2 FPGA board to achieve fail-safe operation of the GaN converter in this work is shown in Figure 7-3. The logic truth table and state diagram of the circuit diagram are presented in Table 7-2 and Figure 7-4, respectively. A slide switch on the FPGA board was assigned as the reset switch ($SW_{RST}$) that lets the user to manually toggle the switch so that the converter operation is resumed after the inverted EN signal from GDSFP, $\overline{EN_{GDSFP}}$, is recovered back to state '0' (i.e. after the gate drive supplies of the D-mode power devices are fully recovered). The SR latch was designed using two NOR gates so that the output PWM drive signal, $PWM_{out}$, and the EN signal for $S_{dc(HV)}$ and $S_{dc(LV)}$ devices in Figure 5-1, $EN_{Sdc}$, are disabled as state '0' (low) when $\overline{EN_{GDSFP}} = 1$ i.e. when gate drive supplies fail.

**Normal operation (R = 0, S = 1):** The $EN_{Sdc}$ signal remains at logic state '1' (high) and $PWM_{out}$ signal with constant duty cycle and switching frequency is transmitted on a continuous basis to the input side of the gate driver IC and hence to the power device in the converter. The half-bridge converter enters the normal operation only if the gate drive supplies for the both top and bottom devices are active and hence the logic state of the $\overline{EN_{GDSFP}}$ signal is '0'. The 16-digit binary output from counter 1 in Figure 7-3, $Q_1$ (15:0), was compared against the reference 16-digit binary values indicating the PWM frequency and duty cycles ($PWM_{freq}$ and $PWM_{duty}$) values so that the PWM signal with fixed frequency and duty cycle is continuously fed to the power devices in the converter during normal operation.

**Gate drive supply failure (R = 1, S = 0):** If one of the gate drive voltage supplies for the D-mode power devices is lost, then this failure would be detected by the GDSFP scheme in Figure 4-21 and thus $EN_{GDSFP} = 0$ i.e. $\overline{EN_{GDSFP}} = 1$. As a result, the next state of R and S (labelled as R' as S' in Figure 7-3) would be changed to '1' and '0', respectively, which yields the logic state of the output $EN_{Sdc}$ signal from the SR latch to be '0'. Consequently, the $S_{dc(HV)}$ and $S_{dc(LV)}$ devices are turned off so that the D-mode power devices within the converter circuit are fully isolated from both HV and LV supplies. Simultaneously, the $PWM_{out}$ signal becomes disabled so that no PWM signals are transmitted to the gate driver ICs.

**Gate drive supply recovery (R = 0, S = 0) and restoration of normal operation (R = 0, S = 1):** At the SR logic output of R = 1 and S = 0, the user may toggle the $SW_{RST}$ switch to be in state '0'; subsequently, the SR latch output would be transitioned to R = 0 and S = 0. When all of the gate drive supplies in the power converter are fully recovered (i.e. $\overline{EN_{GDSFP}} = 0$) and the $SW_{RST}$ is re-toggled by the user to be '1', the SR latch output is changed to R = 0 and S = 1 and hence $EN_{Sdc}$ = 1 (i.e. $S_{dc(HV)}$ and $S_{dc(LV)}$ devices are turned on) so that the converter is re-energised and the PWM signal is transmitted to the gate driver ICs after 1 sec. This time length was set by comparing the output of the counter 2 (in Figure 7-3), $Q_2$ (15:0), against the PWM time delay reference value, $PWM_{delay}$ (15:0); the PWM signal will be enabled when $Q_2 = PWM_{delay}$. Hence, the normal operation mode of the converter is restored.

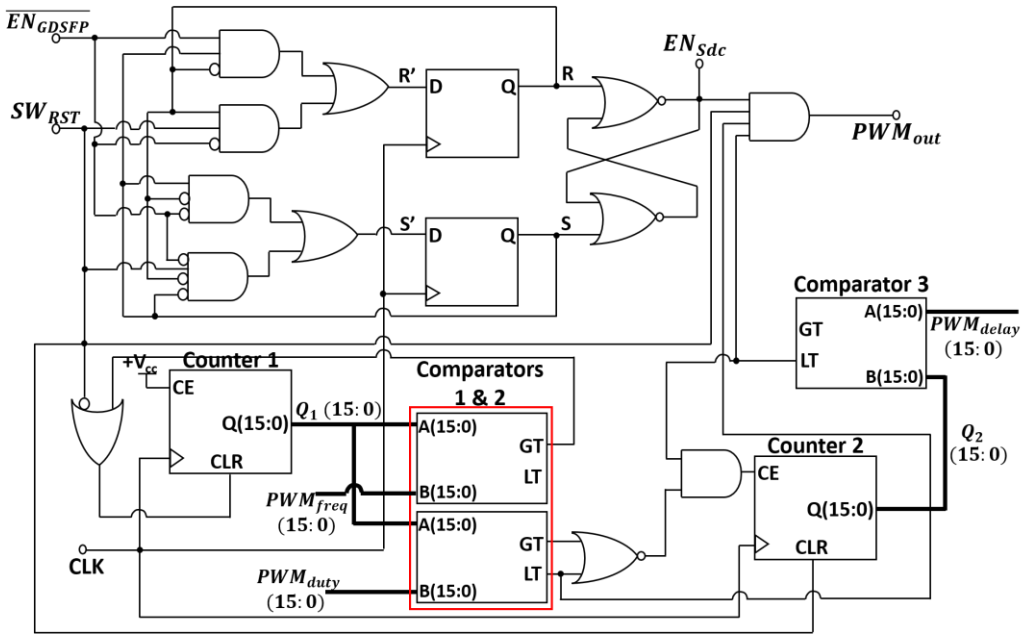



*Figure 7-3: Logic circuit diagram of FPGA configuration for fail-safe converter drive*

| Current state | | Input | | Next state | | Output |
|---|---|---|---|---|---|---|
| R | S | $\overline{EN_{GDSFP}}$ | $SW_{RST}$ | R' | S' | $EN_{Sdc}$ |
| 0 | 1 | 0 | X | 0 | 1 | 1 |
| 0 | 1 | 1 | X | 1 | 0 | 1 |
| 1 | 0 | X | 0 | 0 | 0 | 0 |
| 1 | 0 | X | 1 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| 0 | 0 | 1 | X | 0 | 0 | 0 |

*Table 7-2: Logic truth table of the FSM configuration implemented on FPGA board*

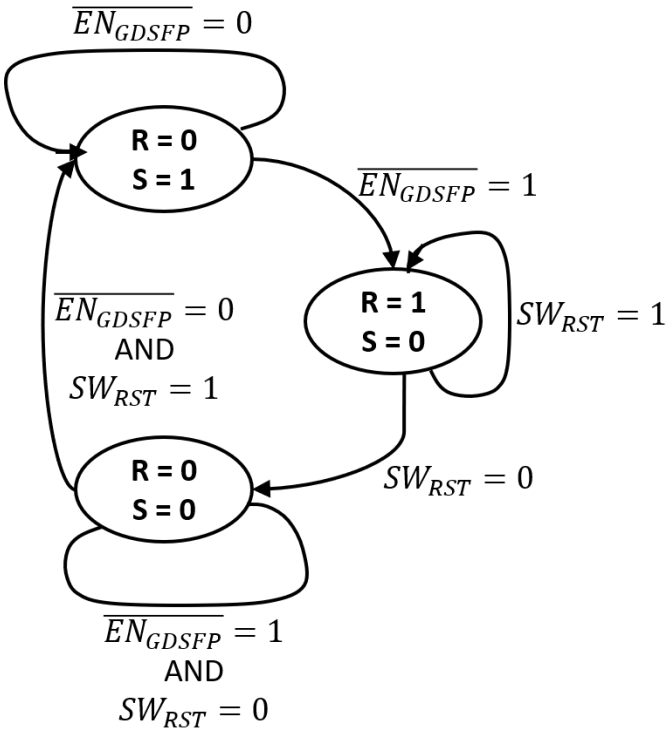



*Figure 7-4: Logic state diagram of the fail-safe converter control system implemented*

# 8 References


[1] K. A. Friedrich, K. Josef, J. Schirmer, and G. Schmitthals, "Fuel Cell Systems for Aircraft Application," *ECS Transactions*, vol. 25, no. 1, pp. 193-202, 2009.

[2] "Diesel fuel explained - Use of diesel." U.S. Energy Information Administration. https://www.eia.gov/energyexplained/diesel-fuel/use-of-diesel.php (accessed 26th Feb, 2020).

[3] "Road traffic statistics." The HM Government. https://roadtraffic.dft.gov.uk/summary (accessed 27th Feb, 2020).

[4] P. Busquin, J. Lumsten, M. Bischoff, D. Ranque, and P. Reutlinger, "European Aeronautics: A vision for 2020," Advisory Council for Aviation Research and innovation in Europe (ACARE), 2001.

[5] (2018). *The Road to Zero - Next step towards cleaner road transport and delivering our Industrial Strategy*.

[6] "How Do All-Electric Cars Work?" U.S. Department of Energy - Alternative Fuels Data Center. https://afdc.energy.gov/vehicles/how-do-all-electric-cars-work (accessed 2nd March, 2020).

[7] "How Do Gasoline Cars Work?" U.S. Department of Energy - Alternative Fuels Data Center. https://afdc.energy.gov/vehicles/how-do-gasoline-cars-work (accessed 2nd March, 2020).

[8] W. Spitz, B. Miller, and F. Morser, "Aviation Fuel Costs And Alternatives," ed: Transportation Research Board, 2012.

[9] "Alternative Aviation Fuels: Overview of Challenges, Opportunities, and Next Steps," ed: U.S. Department of Energy's Office of Energy Efficiency and Renewable Energy (EERE), 2017.

[10] (2007). *The Potential Use Of Alternative Fuels for Aviation*.

[11] S. R. Schill. "Blog: Biofuels and airplanes fly together." Ethanol Producer Magazine. http://ethanolproducer.com/articles/13307/ (accessed 25 May, 2018).

[12] S. Christopher. "Boeing 787 delivery flight to ANA marks first use of biofuels on the new Dreamliner and also first across the Pacific." GreenAir Communications. http://www.greenaironline.com/news.php?viewStory=1516 (accessed.

[13] N. Zhou. "Qantas uses mustard seeds in first ever biofuel flight between Australia and US " The Guardian. https://www.theguardian.com/environment/2018/jan/30/qantas-uses-mustard-seeds-in-first-ever-biofuel-flight-between-australia-and-us (accessed.

[14] J. Hernandez. "C-17 makes first flight on synthetic fuel blend." Air Mobility Command. http://www.amc.af.mil/News/Article-Display/Article/147816/c-17-makes-first-flight-on-synthetic-fuel-blend/ (accessed 30th May, 2018).

[15] J. Paur. (2010) Air Force Debuts Diofuel-guzzling Warthog. *WIRED*. Available: https://www.wired.com/2010/03/air-force-debuts-biofuel-guzzling-warthog/

[16] "Advances in more-electric aircraft technologies," *Aircraft Engineering and Aerospace Technology*, vol. 73, no. 3, 2001.

[17] P. Wheeler, "The more electric aircraft: Why aerospace needs power electronics?," presented at the Power Electronics and Applications, 2009. EPE '09. 13th European Conference on, Barcelona, Spain, 2009.

[18] C. R. Avery, S. G. Burrow, and P. H. Mellor, "Electrical generation and distribution for the more electric aircraft," presented at the Universities Power Engineering Conference (UPEC), 2007. 42nd International, Brighton, UK, 2007.

[19] A. C. Hoffman *et al.*, "Advanced secondary power system for transport aircraft," NASA, United States, 1985.

[20] J. A. Rosero, J. A. Ortega, E. Aldabas, and L. Romeral, "Moving Towards a More Electric Aircraft," *IEEE Aerospace and Electronic Systems Magazine*, vol. 22, no. 3, pp. 3-9, 2007.

[21] B. Zhang. "Boeing's most important plane could be headed for trouble." Business Insider. http://uk.businessinsider.com/boeing-787-dreamliner-sales-slow-2016-5 (accessed 31st May, 2018).

[22] G. Vogel, *Flying the Boeing 787*. Wiltshire, UK: The Crowood Press Ltd., 2013.

[23] R. T. Naayagi, "A Review of More Electric Aircraft Technology," presented at the Energy Efficient Technologies for Sustainability (ICEETS), 2013 International Conference on, Nagercoil, India, 2013.

[24] R. Todd, D. Wu, J. A. d. Santos Girio, M. Poucand, and A. J. Forsyth, "Supercapacitor-Based Energy Management for Future Aircraft Systems," presented at the Applied Power Electronics Conference and Exposition (APEC), 2010 Twenty-Fifth Annual IEEE, Palm Springs, CA, USA, 2010.

[25] S. C. Smith, P. K. Sen, and B. Kroposki, "Advancement of energy storage devices and applications in electrical power system," presented at the Power and Energy Society General Meeting - Conversion and Delivery of Electrical Energy in the 21st Century, 2008 IEEE, Pittsburgh, PA, USA, 2008.

[26] J. Garthwaite. "How ultracapacitors work (and why they fall short)." Gigaom. https://gigaom.com/2011/07/12/how-ultracapacitors-work-and-why-they-fall-short/ (accessed 31st May, 2018).

[27] A. Yu, V. Chabot, and Z. Jiujun, *Electrochemical Supercapacitors for Energy Storage and Delivery: Fundamentals and Applications*. NW, USA: CRC Press, 2013.

[28] C. Ilias, "Optimisation of High Voltage Electrical Systems for Aerospace Applications," PhD, School of Electrical and Electronic Engineering, The University of Manchester, Manchester, 2011.

[29] P. Wilson. "Electric aircraft—the future of aviation or wishful thinking?" Phys.org. https://phys.org/news/2015-08-electric-aircraftthe-future-aviation.html (accessed 31st May, 2018).

[30] B. Scrosati and J. Garche, "Lithium batteries: Status, prospects and future," *Journal of Power Sources,* vol. 195, no. 9, pp. 2419-2430, 2010.

[31] S. Sahoo, X. Zhao, and K. Kyprianidis, "A Review of Concepts, Benefits, and Challenges for Future Electrical Propulsion-Based Aircraft," *Aerospace,* vol. 7, no. 4, 2020.

[32] "Insight 07: Electrical power systems." Aerospace Technology Institute. https://www.ati.org.uk/strategy-insight/?pdf=7711 (accessed 15 Oct, 2015).

[33] J. Y. Tsao, S. Chowdhury, M. A. Hollis, D. Jena, and N. M. Johnson, "Ultrawide-Bandgap Semiconductors: Research Opportunities and Challenges " *Advanced Electronic Materials,* vol. 4, 2018.

[34] N. Kaminski and O. Hilt, "SiC and GaN devices – wide bandgap is not all the same," *IET Circuits, Devices & Systems,* vol. 8, no. 3, pp. 227-236, 2014.

[35] K. Nando, "State of the Art and the Future of Wide Band-Gap Devices," presented at the 13th European Conference on Power Electronics and Applications, 2009.

[36] "The Potential of Wide-Bandgap Semiconductors." Power Electronics News. https://www.powerelectronicsnews.com/the-potential-of-wide-bandgap-semiconductors/ (accessed 17 Oct, 2020).

[37] A. Lidow and J. Strydom, "Gallium Nitride (GaN) Technology Overview," *White paper: WP001,*

[38] S. Havanur and P. Zuk, "Power MOSFET Basics - Understanding Superjunction Technology," ed: Vishay Siliconix, 2015.

[39] T. Fujihira, "Theory of Semiconductor Superjunction Devices," *Japanese Journal of Applied Physics,* vol. 36, no. 10, pp. 6254-6262, 1997.

[40] J. Hancock, F. Stueckler, and E. Vecino, "Application Note AN 2013-04 - CoolMOS C7: Mastering the Art of Quickness," in *A technology Description and Design Guide*, ed. Austria: Infineon Technologies, 2013.

[41] W. Saito *et al.*, "High Breakdown Voltage (>1000 V) Semi-Superjunction MOSFETs Using 600-V Class Superjunction MOSFET Process " *IEEE Transactions on Electron Devices*, vol. 52, no. 10, pp. 2317-2322, 2005.

[42] S. M. Sze, *Modern Semiconductor Device Physics*. Canada: John Wiley & Sons, Inc., 1998.

[43] A. Sattar, "Insulated Gate Bipolar Transistor (IGBT) Basics," ed: IXYS Corporation.

[44] P. Zuk. "High-Voltage Silicon MOSFETs, GaN, and SiC: All have a place." EDN Network. https://www.edn.com/design/components-and-packaging/4375812/High-Voltage-Silicon-MOSFETs-still-hold-lead-over-SiC-and-GaN (accessed April 19, 2018).

[45] I. Rectifier, "Application Note AN-983 - IGBT Characteristics," ed, 2012.

[46] "IGBT Technologies and Applications Overview: How and When to Use an IGBT," ed: ON Semiconductor, 2018.

[47] H. Kawai, S. Yagi, S. Hirata, and F. Nakamura, "Low cost high voltage GaN polarization superjunction field effect transistors," *Physica Status Solidi A*, vol. 214, no. 8, 2017.

[48] T. Wonglakhon and D. Zahn, "Interaction potentials for modelling GaN precipitation and solid state polymorphism " *Journal of Physics: Condensed Matter*, vol. 32, 2020.

[49] O. Ambacher, J. Majewski, C. Miskys, A. Link, and M. Hermann, "Pyroelectric properties of Al(In)GaN/GaN hetero- and quantum well structures," *Journal of Physics: Condensed Matter*, vol. 14, no. 13, pp. 3399-3434, 2002.

[50] T. Nann and J. Schneider, "Origin of permanent electric dipole moments in wurtzite nanocrystals," *Chemical Physics Letters*, vol. 384, no. 1-3, pp. 150-152, 2004.

[51] O. Ambacher *et al.*, "Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face AlGaN/GaN heterostructures," *Journal of Applied Physics*, vol. 85, no. 6, pp. 3222-3233, 1999.

[52] O. Ambacher and V. Cimalla, *Polarisation Induced Effects in GaN-based Heterostructures and Novel Sensors* (Polarization Effects in Semiconductors: From Ab Initio Theory to Device Applications). New York: Springer, 2008.

[53] J. Piprek, *Nitride Semiconductor Devices: Principles and Simulation* (Spontaneous and Piezoelectric Polarisation: Basic Theory vs. Practical Recipes). Weinheim: Wiley, 2007.

[54] O. Ambacher *et al.,* "Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face AlGaN/GaN heterostructures," *Journal of Applied Physics,* vol. 85, no. 6, pp. 3222-3233, 1999.

[55] A. Nakajima, Y. Sumida, M. H. Dhyani, H. Kawai, and E. M. S. Narayanan, "High Density Two-Dimensional Hole Gas Induced by Negative Polarization at GaN/AlGaN Heterointerface," *Applied Physics Express,* vol. 3, no. 12, 2010.

[56] T. Mimura, S. Hiyamizu, T. Fujii, and K. Nanbu, "A New Field-Effect Transistor with Selectively Doped GaAs/n-AlxGa1-xAs Heterojunctions," *Japanese Journal of Applied Physics,* vol. 19, no. 5, pp. L225-L227, 1980.

[57] D. Delagebeaudeuf and N. T. Linh, "Metal-(n) AIGaAs-GaAs Two-Dimensional Electron Gas FET," *IEEE Transactions on Electron Devices,* vol. 29, no. 6, pp. 955-960, 1982.

[58] K. Lee, M. Shur, T. J. Drummond, and H. Morkoç, "Electron density of the two-dimensional electron gas in modulation doped layers," *Journal of Applied Physics,* vol. 54, no. 4, pp. 2093-2096, 1983.

[59] G. Liu, J. Wu, Y. Lu, Z. Li, and Y. Song, "Scattering due to spacer layer thickness fluctuation on two dimensional electron gas in AlGaAs/GaAs modulation-doped heterostructures " *Journal of Applied Physics,* vol. 110, no. 2, 2011.

[60] J. P. Ibbetson, P. T. Fini, K. D. Ness, S. P. DenBaars, J. S. Speck, and U. K. Mishrab, "Polarization effects, surface states, and the source of electrons in AlGaN/GaN heterostructure field effect transistors," *Applied Physics Letters,* vol. 77, no. 2, pp. 250-252, 2000.

[61] M. Miczek, C. Mizue, T. Hashizume, and B. Adamowicz, "Effects of interface states and temperature on the C-V behavior of metal/insulator/AlGaN/GaN heterostructure capacitors," *Journal of Applied Physics,* vol. 103, no. 10, 2008.

[62] A. Wang, L. Zeng, and W. Wang, "Surface donor states-dependent bare surface barrier height and 2DEG density of AlGaN/GaN heterostructure exerted uniaxial stress " *Materials Research Express,* vol. 5, no. 2, 2018.

[63] P. J. Parbrook, T. Wang, M. A. Whitehead, C. N. Harrison, R. J. Lynch, and R. T. Murray, "Crack formation and development in AlGaN/GaN structures," *Physica Status Solidi C,* vol. 0, no. 7, pp. 2055-2058, 2003.

[64] A. D. Bykhovski, B. L. Gelmont, and M. S. Shur, "Elastic strain relaxation and piezoeffect in GaN-AlN, GaN-AlGaN and GaN-InGaN superlattices," *Journal of Applied Physics,* vol. 81, no. 9, pp. 6332-6338, 1997.

[65] "MOSFETs." https://blog.mbedded.ninja/electronics/components/transistors/mosfets/ (accessed 18 Oct, 2020).

[66] N. Ikeda *et al.*, "GaN Power Transistors on Si Substrates for Switching Applications," *Proceedings of the IEEE,* vol. 98, no. 7, pp. 1151-1161, 2010.

[67] D. K. Kim and C. B. Park, "Growth of Crack-Free GaN Films on Si(111) Substrates with AlN Buffer Layers," *Journal of the Korean Physical Society,* vol. 49, no. 4, pp. 1497-1500, 2006.

[68] K. L. Enisherlova, T. F. Rusak, V. I. Korneev, and A. N. Zazulina, "Effect of SiC substrate properties on structural perfection and electrical parameters of AlGaN/GaN layer," *Modern Electronic Materials,* vol. 3, no. 1, pp. 50-56, 2017.

[69] T. Paskova, D. A. Hanser, and K. R. Evans, "GaN Substrates for III-Nitride Devices," *Proceedings of the IEEE,* vol. 98, no. 7, pp. 1324-1338, 2010.

[70] A. M. Wells, M. J. Uren, B. R.S., K. P. Hilton, T. Martin, and M. Missous, "Direct demonstration of the 'virtual gate' mechanism for current collapse in AlGaN/GaN HFETs," *Solid-state Electronics,* vol. 49, no. 2, pp. 279-282, 2005.

[71] R. Vetury, N. Q. Zhang, S. Keller, and U. K. Mishra, "The Impact of Surface States on the DC and RF Characteristics of AlGaN/GaN HFETs," *IEEE Transactions on Electron Devices,* vol. 48, no. 3, pp. 560-566, 2001.

[72] W. Saito, Y. Takada, M. Kuraguchi, K. Tsuda, I. Omura, and T. Ogura, "Design and Demonstration of High Breakdown Voltage GaN High Electron Mobility Transistor (HEMT) Using Field Plate Structure for Power Electronics Applications," *Japanese Journal of Applied Physics,* vol. 43, no. 4B, pp. 2239-2242, 2004.

[73] H.-C. Chiu, C.-W. Yang, H.-C. Wang, F.-H. Huang, H.-L. Kao, and F.-T. Chien, "Characteristics of AlGaN/GaN HEMTs With Various Field-Plate and Gate-to-Drain Extensions," *IEEE Transactions on Electron Devices,* vol. 60, no. 11, pp. 3877-3882, 2013.

[74] O. Hiraku, H. Hideyuki, and H. Kazushige, "Analysis of breakdown characteristics in source field-plate AlGaN/GaN HEMTs," *Physica Status Solidi,* vol. 13, no. 5-6, pp. 350-353, 2016.

[75] K. Sharma, A. Dasgupta, S. Ghosh, S. A. Ahsan, S. Khandelwal, and Y. S. Chauhan, "Effect of Access Region and Field Plate on Capacitance behavior of GaN HEMT," presented at the 2015 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC), Singapore, 2015.

[76] Y. Cai, Y. Zhou, K. J. Chen, and K. M. Lau, "High-Performance Enhancement-Mode AlGaN/GaN HEMTs Using Fluoride-Based Plasma Treatment," *IEEE Electron Device Letters,* vol. 26, no. 7, pp. 435-437, 2005.

[77] K. J. Chen *et al.*, "Physics of Fluorine Plasma Ion Implantation for GaN Normally-off HEMT Technology," presented at the 2011 International Electron Devices Meeting, Washington, DC, USA, 2011.

[78] H. Chen, M. Wang, and K. J. Chen, "Self-aligned enhancement-mode AlGaN/GaN HEMTs using 25 keV fluorine ion implantation," presented at the 68th Device Research Conference, South Bend, IN, USA, 2010.

[79] S. Quan, Y. Hao, X. Ma, Y. Xie, and J. Ma, "Enhancement-mode AlGaN/GaN HEMTs fabricated by fluorine plasma treatment," *Journal of Semiconductors,* vol. 30, no. 12, 2009.

[80] W. Saito, Y. Takada, M. Kuraguchi, K. Tsuda, and I. Omura, "Recessed-Gate Structure Approach Toward Normally Off High-Voltage AlGaN/GaN HEMT for Power Electronics Applications," *IEEE Transactions on electron devices,* vol. 53, no. 2, pp. 356-362, 2006.

[81] H.-S. Kim, S. Heo, and H.-Y. Cha, "Effective Channel Mobility of AlGaN/GaN-on-Si Recessed-MOS-HFETs," *Journal of Semiconductor Technology and Science,* vol. 16, no. 6, pp. 867-872, 2016.

[82] H.-S. Choi, "Mobility Degradation Effect to Hooge's Constant in Recessed-Gate Al2O3/AlGaN/GaN MIS Power Transistors," *IEEE Electron Device Letters,* vol. 35, no. 6, pp. 624-626, 2014.

[83] Z. Tang *et al.*, "600-V Normally Off SiNx /AlGaN/GaN MIS-HEMT With Large Gate Swing and Low Current Collapse," *IEEE Electron Device Letters,* vol. 34, no. 11, pp. 1373-1375, 2013.

[84] H. Kambayashi *et al.*, "Over 100 A operation normally-off AlGaN/GaN hybrid MOS-HFET on Si substrate with high-breakdown voltage," *Solid-State Electronics,* vol. 54, no. 6, pp. 660-664, 2010.

[85] Z. Yatabe, J. T. Asubar, and T. Hashizume, "Insulated gate and surface passivation structures for GaN-based power transistors," *Journal of Physics D: Applied Physics,* vol. 49, no. 39, 2016.

[86] P. Fiorenza, G. Greco, F. Iucolano, A. Patti, and R. Fabrizio, "Channel Mobility in GaN Hybrid MOS-HEMT Using SiO2 as Gate Insulator," *IEEE Transactions on Electron Devices,* vol. 64, no. 7, pp. 2893-2899, 2017.

[87] Y. Uemoto *et al.*, "Gate Injection Transistor (GIT)—A Normally-Off AlGaN/GaN Power Transistor Using Conductivity Modulation," *IEEE Transactions on Electron Devices*, vol. 54, no. 12, pp. 3393-3399, 2007.

[88] "GN001 Application Note: An Introduction to GaN Enhancement-mode HEMTs," ed: GaN Systems Inc, 2020.

[89] G. Grecoa, F. Iucolanob, and F. Roccafortea, "Review of technology for normally-off HEMTs with p-GaN gate," *Materials Science in Semiconductor Processing*, vol. 78, pp. 96-106, 2018.

[90] P. Kozodoy *et al.*, "Heavy doping effects in Mg-doped GaN," *Journal of Applied Physics*, vol. 87, no. 4, pp. 1832-1835, 1999.

[91] U. Kaufmann, P. Schlotter, H. Obloh, K. Ko¨hler, and M. Maier, "Hole conductivity and compensation in epitaxial GaN:Mg layers," *Physical Review B*, vol. 62, no. 16, 2000.

[92] D. Y. Jung, Y. Park, H. S. Lee, C. H. Jun, and H. G. Jang, "Design and Evaluation of Cascode GaN FET for Switching Power Conversion Systems," *ETRI Journal*, vol. 39, no. 1, pp. 62-68, 2017.

[93] W. Liu, H. Zhou, and E. Persson, "Switching Characteristics of Cascode GaN Switches," in *PCIM Europe 2015; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management; Proceedings of*, Nuremberg, Germany, 2015: IEEE, pp. 1002-1009.

[94] P. L. Brohlin, Y. K. Ramadass, and C. Kaya, "Direct-drive configuration for GaN devices,"

[95] A. Nakajima, M. H. Dhyani, E. M. S. Narayanan, Y. Sumida, and H. Kawai, "GaN Based Super HFETs over 700V Using the Polarization Junction Concept," presented at the 2011 IEEE 23rd International Symposium on Power Semiconductor Devices and ICs (ISPSD), San Diego, USA, 2011.

[96] A. Nakajima, K. Adachi, M. Shimizu , and H. Okumura "Improvement of unipolar power device performance using a polarization junction," *Applied Physics Letters*, vol. 89, no. 19, 2006.

[97] V. Unni, H. Y. Long, H. Yan, A. Nakajima, H. Kawai, and M. Ekkanath Sankara Narayanan, "Analysis of drain current saturation behaviour in GaN polarisation super junction HFETs," *IET Power Electronics*, vol. 11, no. 14, pp. 2198-2203, 2018.

[98] M. E. Coltrin, A. G. Baca, and R. J. Kaplar, "Analysis of 2D Transport and Performance Characteristics for Lateral Power Devices Based on AlGaN Alloys," *ECS Journal of Solid State Science and Technology,* vol. 6, no. 11, 2017.

[99] A. Lidow, J. Strydom, M. d. Rooij, and D. Reusch, *GaN Transistors for Efficient Power Conversion*, 2nd ed. John Wiley & Sons Ltd, 2015, p. 269.

[100] D. Reusch and J. Strydom, "Understanding the Effect of PCB Layout on Circuit Performance in a High Frequency Gallium Nitride Based Point of Load Converter," *IEEE Transactions on Power Electronics,* vol. 29, no. 4, pp. 2008-2015, 2014.

[101] A. Lidow and J. Strydom, "eGaN® FET Drivers and Layout Considerations," ed: Efficient Power Conversion (EPC), 2016.

[102] J. Watson, "High-Temperature Electronics Pose Design and Reliability Challenges," *Analog Dialogue*, no. 2, pp. 3-9

[103] P. D. Reigosaa *et al.*, "Comparison of Thermal Runaway Limits under Different Test Conditions Based on a 4.5 kV IGBT," *Microelectronics Reliability*, 2016.

[104] S. Kumar, S. B. Dolmanan, S. Tripathy, R. Muralidharan, and D. N. Nath, "Meandering gate edges for breakdown voltage enhancement in AlGaN/GaN HEMTs,"

[105] B. J. Baliga, "Power Semiconductors Device Figure of Merit for High-Frequency Applications," *IEEE Electron Device Letters*, vol. 10, no. 10, 1989.

[106] J. Hancock, F. Stueckler, and E. Vecino, "CoolMOS C7: Mastering the Art of Quickness," in *A technology Description and Design Guide*, ed. Austria: Infineon Technologies, 2013.

[107] "Wolfspeed: A Cree Company." https://www.wolfspeed.com/ (accessed May 8th, 2019).

[108] "GaN Systems." GaN Systems. https://gansystems.com/ (accessed April 17, 2019).

[109] K. S. A. Butcher, T. L. Tansley, and D. Alexiev, "An instrumental solution to the phenomenon of negative capacitances in semiconductors," *Solid-State Electronics,* vol. 39, no. 3, pp. 333-336, 1996.

[110] "Primer: ABCs of Probes," pp. 7-8

[111] J. B. Witcher, "Methodology for Switching Characterization of Power Devices and Modules," Master of Science, Virginia Polytechnic Institute and State University, 2002.

[112] C. M. Johnson and P. R. Palmer, "Current measurement using compensated coaxial shunts," *IEE Proceedings - Science, Measurement and Technology,* vol. 141, no. 6, pp. 471-480, 1994.

[113] Z. Zhang *et al.*, "Methodology for Switching Characterization Evaluation of Wide Band-gap Devices in a Phase-leg Configuration," presented at the 2014 IEEE Applied Power Electronics Conference and Exposition, Fort Worth, TX, USA, 2014.

[114] "PEARSON Current monitor 2877 Datasheet." Pearson Electronics, Inc. http://www.pearsonelectronics.com/pdf/2877.pdf (accessed.

[115] "Ingenieurbüro Billmann Coaxial Shunts." Ingenieurbüro Billmann. http://www.ib-billmann.de/koax_e.php (accessed.

[116] "GN003 Application Note - Measurement Techniques for High-Speed GaN E-HEMTs," ed: GaN Systems, 2018.

[117] "PEM CWT Ultra-mini Datasheet." Power Electronic Measurements Ltd. http://www.pemuk.com/Userfiles/CWTum%2030MHz/CWT%20Ultra-mini_0518(Web).pdf (accessed.

[118] P. Technology. https://www.picotech.com/ (accessed December 7th, 2019).

[119] "IPD040N03L G datasheet," 1.02 ed: Infineon Technologies, 2008.

[120] R. L. Kelley, M. S. Mazzola, W. A. Draper, and J. Casady, "Inherently Safe DC/DC Converter Using a Normally- On Sic JFET " *Twentieth Annual IEEE Applied Power Electronics Conference and Exposition*, pp. 1561-1565, 2005.

[121] D. Bergogne *et al.*, "Normally-On SiC JFETs in Power Converters: Gate Driver and Safe Operation," presented at the 2010 6th International Conference on Integrated Power Electronics Systems, Nuremberg, Germany, 2010.

[122] F. Dubois *et al.*, "Ultrafast Safety System to Turn-Off Normally On SiC JFETs," presented at the Proceedings of the 2011 14th European Conference on Power Electronics and Applications, Birmingham, UK, 2011.

[123] D. Peftitsis, J. Rabkowski, and H.-P. Nee, "Self-Powered Gate Driver for Normally ON Silicon Carbide Junction Field-Effect Transistors Without External Power Supply " *IEEE Transactions on Power Electronics*, vol. 28, no. 3, pp. 1488-1501, 2013.

[124] S. V. Giannoutsos, S. Kokosis, and S. N. Manias, "A Gate Drive Circuit for Normally-On SiC JFETs with Self-Protection Functions against Overcurrent and Shoot-Through Fault Conditions," presented at the IEEE 15th International Conference on Environment and Electrical Engineering (EEEIC), Rome, Italy, 2015.

[125] B. W. Williams, *Power Electronics: Devices, Drivers and Applications*. London: Macmillan Publishers Limited, 1987.

[126] C. W. T. Mclyman, M. O. Thurston, Ed. *Transformer and Inductor Design Handbook*, 3rd ed. USA: Marcel Dekker, Inc, 2004.

[127] J. Watson and G. Castro, "High-Temperature Electronics Pose Design and Reliability Challenges," *Analog Dialogue*, no. 2, pp. 3-9

[128] "Switching Regulator IC Series - Efficiency of Buck Converter," ed: Rohm Semiconductor Co. Ltd., 2016, pp. 1-15.

[129] W. Zhang, X. Huang, F. C. Lee, and Q. Li, "Gate Drive Design Considerations for High Voltage Cascode GaN HEMT," presented at the 2014 IEEE Applied Power Electronics Conference and Exposition (APEC), Fort Worth, TX, USA, 2014.

[130] "Frequency-Impedance Characteristics of Inductors and Determination of Inductor's Resonance Frequency." Rohm Semiconductor. https://techweb.rohm.com/knowledge/emc/s-emc/04-s-emc/8136 (accessed 12 Oct, 2020).

[131] Z. Wen, Y. Xu, C. Wang, X. Zhao, Z. Chen, and R. Xu, "A parameter extraction method for GaN HEMT empirical large signal model including self-heating and trapping effects," *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields,* vol. 30, no. 1, 2015.

[132] "5991-4656EN Application Note: Internal Gate Resistance Measurement Using the B1505A," ed. USA: Keysight Technologies, 2014.

[133] "Aluminum Electrolytic Capacitors (SMD) Datasheet," ed: Panasonic, 2019.

[134] "Frequency-Impedance Characteristics of Inductors and Determination of Inductor's Resonance Frequency." Rohm Semiconductor. https://techweb.rohm.com/knowledge/emc/s-emc/04-s-emc/8136 (accessed.

[135] P. Poure, P. Weber, D. Theilliol, and S. Saadate, "Fault-tolerant Power Electronic Converters: Reliability Analysis of Active Power Filter," presented at the IEEE International Symposium on Industrial Electronics, Vigo, Spain, 2007.

[136] J. Wang, H. S.-h. Chung, and R. T.-h. Li, "Characterization and Experimental Assessment of the Effects of Parasitic Elements on the MOSFET Switching Performance," *IEEE Transactions on Power Electronics*, vol. 28, no. 1, pp. 573-590, 2013.