The University Of Sheffield.

Advanced MOVPE Growth of Non-Polar GaN on Silicon and Others Based on Novel AlN buffer Technologies

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Abstract

Due to their wide band-gaps and excellent chemical & mechanical stability, III-nitride semiconductors play key roles in a wide range of applications, such as for general illumination, 5G mobile communications, visible light wireless communication (Li-Fi), high frequency and high temperature electronics, etc. Very recently there is an increasing demand for developing emitters and photodetectors with III-nitride materials for environmental protection, water purification, medical instrumentation, non-line-of-sight communications, etc. Moreover, the growth of III-nitride devices on industry-compatible silicon substrates exhibit many advantages in terms of wafer costs, scalability, silicon technology compatibility and silicon photonics where the integration of III-nitride emitters/photodetectors and electronics can serve as a platform for the fabrication of photonic and electronic integrated circuits.

Compared with the present III-nitride optoelectronics grown on c-plane substrates, non-polar GaN intrinsically exhibits many major advantages such as zero polarisation effects leading to a higher efficiency and a faster response speed. However, the crucial challenge is due to the crystal quality of non-polar GaN on industrial-compatible substrates which is far from satisfactory. In the last decade our research group at the University of Sheffield has developed a number of cost-effective overgrowth approaches for semi-polar and non-polar GaN on sapphire substrates by using high temperature (HT) AlN buffer technology on regularly arrayed micro-rod templates that lead to a step-change in crystal quality. Due to the advantages mentioned above these approaches are progressed further towards compatibility with silicon substrates. However, Ga melt-back etching and cracking are the main challenges due to a high temperature which GaN growth requires. Furthermore, it is almost impossible to grow non-polar GaN on planar silicon substrates.

In order to address these challenging issues, the project has developed and then has well-established a two-step approach to achieving high crystal quality non-polar $(11\bar{2}0)$ GaN on patterned (110) silicon substrates by means of a combination of a HT-AlN

buffer and selective MOVPE overgrowth techniques, where gallium melt-back etching has been eliminated and a step-change in crystal quality grown has been achieved. Detailed x-ray diffraction and PL measurements have been performed in order to characterise the non-polar GaN, confirming that both the dislocation density and the density of basal stacking faults (BSFs) have been significantly reduced, in particular, BSFs which have been reduced to an almost invisible level. The detailed optical properties have also been investigated.

On such high crystal quality $(11\bar{2}0)$ non-polar GaN with a micro-stripe configuration on the patterned (110) silicon, an InGaN/GaN multiple quantum wells (MQW) structure has been grown, leading to multiple emissions from different facets (polar and non-polar facets, where indium incorporation rates are different leading to a difference in indium content in InGaN). Advanced optical characterisation has been conducted by means of using confocal PL and cathodoluminescence (CL) measurements.

A non-polar GaN metal-semiconductor-metal (MSM) photo-detector (PD) with an ultra-high responsivity and an ultra-fast response speed in the ultraviolet spectral region, which was fabricated on such non-polar $(11\bar{2}0)$ GaN stripe arrays with a step-change in crystal quality. The non-polar GaN MSM PD exhibits a responsivity of ~7E2 A/W at 1 V bias and ~1.2E4 A/W at 5 V bias both under 360 nm ultraviolet illumination, which are more than 20 times higher and 4 orders of magnitude higher compared with the current state-of-the-art, respectively. The non-polar GaN MSM-PD displays a rise-time and a fall-time of 66 μs and 43 μs, respectively, which are three orders of magnitude faster compared with the current state-of-the-art.

We have also applied the HT-AlN buffer technique in the growth of GaN electronics on c-plane sapphire in order to explore a new approach toward the intrinsic limits of GaN electronics from the perspective of epitaxial growth. By using a novel two-dimensional growth mode benefiting from the HT-AlN buffer technology, which is different from the classic two-step growth approach, our high-electron-mobility transistors (HEMTs) demonstrate an extremely high breakdown field of 2.5 MV/cm

approaching the theoretical limit of GaN (3 MV/cm) and an extremely low off-state buffer leakage of 1 nA/mm at a bias of up to 1000 V. Furthermore, such HEMTs also exhibit an excellent figure-of-merit ($V_{br}^2/R_{on,sp}$) of 5.13×10^8 $V^2/\Omega \cdot cm^2$.

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Publications

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Acronyms

Al aluminium

AlGaN aluminium gallium nitride

AlN aluminium nitride

Al_2O_3 aluminium oxide (sapphire)

Au gold

BSF basal stacking fault

CCD charge-coupled device

CCS close-coupled showerhead

CHF_3 fluoroform

CL cathodoluminescence

CO_2 carbon dioxide

Cp_2MG bis(cyclopentadienyl) magnesium

Cu copper

DI water deionised water

DUV deep ultraviolet

ELOG epitaxial lateral overgrowth

FOMs figure of merits

FWHM full width at half maximum

Ga gallium

GaCl gallium monochloride

GaN gallium nitride

H_2 hydrogen

HCL hydrogen chloride

HEMT high electron mobility transistor

HF hydrofluoric

H_2O water

H_2O_2 hydrogen peroxide

HVPE hydride vapour phase epitaxy

H_2SO_4 sulfuric acid

In indium

InGaN indium gallium nitride

ITO indium tin oxide

IQE internal quantum efficiency

KOH potassium hydroxide

InN indium nitride

LD laser diode

LED light emitting diode

LEEBI low energy electron-beam irradiation

MBE molecular beam epitaxy

MFC mass flow controller

Mg magnesium

MIS metal-insulator-

	semiconductor
MOCVD	metal organic chemical vapour deposition
MOVPE	metal organic vapour phase epitaxy
MQW	multiple quantum well
MSM	metal-semiconductor-metal
N_2	nitrogen
NBE	near band emission
NH_3	ammonia
N_2O	nitrous oxide
O_2	oxygen
PCB	print circuit board
PD	photodetector
PECVD	plasma enhanced chemical vapour deposition
PL	photoluminescence
PSF	prismatic stacking fault
PSU	power supply unit
QCSE	quantum-confined Stark effect
QW	quantum well
RF	radio frequency
RIE	reactive-ion etching
SEM	scanning electron microscope
Si	silicon
SiC	silicon carbide
SiH_4	silane
Si_2H_6	disilane
SiN	silicon nitride
SiO_2	silicon dioxide
Ti	titanium
TIA	trans impedance amplifier
TMAl	trimethylaluminum
TMGa	trimethylgallium
TMIn	trimethylindium
UV	ultraviolet
XRD	x-ray diffraction
YBE	yellow-band emission
ZnO	zinc oxide

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Chapter 1

Introduction

This chapter starts with an introduction of developing energy for lighting, and a brief description about the history of the development III-nitride materials and devices for solid-state lighting is then presented. The challenges which the III-nitride research community is facing are subsequently introduced. A summary of the motivation and aim of this project is provided in this chapter. Finally, the thesis organisation is presented at the end of the chapter.

1.1 Energy and Lighting

Energy resources can be classified into two categories in terms of sustainability: non-renewable energy resources such as fossil fuels, traditional biomass and nuclear energy, and renewable energy resources like wind power, solar power, hydropower, etc. Currently, nearly 51% of all the energy resources are consumed for heating and cooling, while the rest 32% is used for transport and 17% for power supply or electricity generation. Among the energy resources used for power supply, only 26% is renewable energy [1].

In 2018 the demand for global energy was increased by 2.3%, which is the highest increase-rate over the past decade. From 2006 to 2016 the growth rate of the total energy consumption is 1.5% [2], among which fossil and nuclear energy contribute to a 1.4% increase. The estimated percentage of fossil fuels among the total energy consumption is 84.7% in 2018 [1]. Hence the world still has a huge dependence on fossil fuels. Fossil fuels release carbon dioxide during their transformation into energy. The carbon dioxide is one of the main reasons for global warming. The global emission of carbon dioxide was 33.1 gigatons (Gt) in 2018, significantly contributing to the appearance of the 5 consecutive warmest years from 2014 to 2018 in the last 100 years [3]–[5]. Due to the great concerns about global warming and climate change, the Paris

Agreement requires that the average rise in global temperature must be limited of 1.5 degrees Celsius (°C) per year. Compare to the global temperature on the pre-industrial levels it is estimated that only 10 years are left for human being in order to maintain the 1.5°C threshold which is the minimal requirement for eliminating a risk of irreversible climate change. This indicates that neither a reduction in consuming fossil fuels nor an increase in renewable energy is on a track. The targets for renewables, energy efficiency and energy access set out for 2030 by UN Sustainable Development Goal 7 (SDG7) will not be achieved unless a momentous expansion of the renewable energy industry occurs.

Energy consumption in human history was initially for cooking and then lighting in the ancient times. When early humans began to use fire as a lighting source from 125,000 BC, the evolution of lighting technology in human history has started. At about 70,000 BC, containers such as shells filled with animal fat were used to get fire. Oil lamps in 4500 BC and candles in 3000 BC represents the evolution of control of fire in the history of human beings [6], [7]. In the 18th century, different lamps were invented such as central draught fixed oil lamp and gas light. Starting from the 19th century the electric light significantly evolved [8]. A large number of electric lights was used in human society. Nowadays, lighting efficiency and energy consumption are the main issues of concern for lighting technology. One of the major electricity consumptions globally is lighting; 19% of the total electricity generated is consumed by lighting-related usage [9]. The low efficiency of traditional lighting methods uses a large amount of energy. To improve the efficiency of general lighting, solid state lighting based on III-nitride light-emitting diodes (LEDs) is expected to be one of the many promising solutions.

The first LEDs emitting low-intensity infrared light were reported in 1962 [10] and the first visible LED with exceptionally low intensity was introduced by Radio Corporation of America (RCA) in 1972 [11]. The brightness is so low that it could not be used for a conventional lighting system. In 1994 Shuji Nakamura who was then working for Nichia Corporation in Japan demonstrated the world's first blue LED with a brightness on the candela level [12], as a result of a joint effort with Isamu Akasaki and Hiroshi Amano

who invented a so-called two-step growth method on sapphire which exhibits a large lattice-mismatch with GaN and demonstrated another major technological breakthrough for achieving p-type GaN [13]. The first white LED, reported in 1995, was achieved by combining blue LEDs and yellow phosphor as a down conversion material [14]. After many years, now the LED lighting is quite common. With the development of LED technology, from the home roof lighting to road lights, LED lighting is almost everywhere in the world. But all these technical benefits are closely related to the rapid development of III-nitride research.

1.2 History of III-Nitrides Research

The first GaN semiconductor compound in a powder form was synthesised by Johnson in 1928 by flowing ammonia gas on gallium metal at high temperature [15]. GaN has a high melting point of over 2,500°C and a very high decompression pressure [16]. It is exceedingly difficult to manufacture a single crystal GaN ingot by the Czochralski process that is typical of industrial silicon production. The first single-crystalline GaN film was introduced by Maruska and Tietjen in 1969 [17]. The vapour-phase growth method was first applied in producing GaN films, where hydrogen chloride (HCl) gas was flowed over the surface of gallium metal (Ga) at a high temperature. The product of the reaction is gallium monochloride (GaCl). During the vapour-phase growth gallium monochloride as a gallium source reacts with ammonia (NH_3) as a nitrogen source. The compound finally generated on the sapphire substrate is gallium nitride. The GaN film grown by this method exhibited a high background electron concentration ($> 10^{19}\mathrm{cm}^{-3}$), and a high density of dislocations due to the large lattice mismatch between the GaN and sapphire. Molecular Beam Epitaxy (MBE) was first applied in the epitaxial growth of GaN on sapphire substrate using a two-step method in 1983 by Yoshida et al [18]. An aluminium nitride (AlN) buffer layer was prepared at a high temperature prior to any GaN growth, where the AlN buffer used aimed to reduce the lattice mismatch between GaN and sapphire, leading to a GaN film with an improved quality. Three years later in 1986, Amano et al. achieved GaN film on sapphire with both good morphology and good quality by using metal organic chemical vapour deposition (MOCVD) [19], where a key invention has

been used, which is a two-step growth procedure, but with an AlN buffer layer grown at a low temperature. In 1991, Nakamura further simplified the two-step method, and he used a low temperatures GaN buffer layer instead of the low temperatures AlN buffer by MOCVD [20]. Nowadays this method of growing high quality GaN films on sapphire substrates by MOCVD is widely used in manufacturing III-nitride devices on sapphire.

Another major step in progress of III-nitride semiconductor devices is due to the achievement of p-type GaN (p-GaN). In 1971 Pankove et al. of RCA produced the world's first GaN-based blue LEDs with an Zn doped metal-insulator-semiconductor (MIS) structure [21]. In 1973 Maruska et al. used magnesium (Mg) as a dopant and obtained a purple LED using an MIS structure [22]. Due to the poor quality of the GaN film and the unsolved p-GaN technology during that time the MIS structure GaN-based LED has an exceptionally low internal quantum efficiency. In 1989 Amano et al. demonstrated the first p-GaN with a low resistivity by applying low energy electron-beam irradiation (LEEBI) on MOCVD grown Mg-doped p-GaN [23]. However, such a p-type activation process was limited by the penetration depth of an e-beam. As a result, thin p-type GaN of the Mg-doped GaN could be obtained. In 1992 Nakamura et al. invented an annealing process under nitrogen ambient at a high temperature of 700°C [24], which can be applied in activating Mg-doped GaN with any size. The annealing process significantly reduced the resistivity of p-GaN from $1 \times 10^{6} \Omega \cdot \mathrm{cm}$ to $2 \Omega \cdot \mathrm{cm}$.

Based on the above achievements Nakamura et al. obtained high brightness blue LEDs with an indium gallium nitride (InGaN) / aluminium gallium nitride (AlGaN) double heterojunction structure in 1994 [12]. Next year in 1995, they demonstrated III-nitride LEDs from ultra-violet (UV) to green and yellow [25], [26].

III-nitride semiconductors across the entire composition all have direct bandgaps. The ternary alloys AlGaN and InGaN across the entire composition cover a wide spectral region from 6.2eV (AlN) through 3.43eV (GaN) to 0.7eV (InN), spanning a wide range from the deep UV through nearly the whole visible to the infrared in

theory. However, due to the low efficiency of high indium content InGaN, the low energy range may not be accessible in practise. Nevertheless, III-nitride semiconductors are still prospective materials for light emitters, solar cells, and detectors. After the first high brightness blue LED was reported [27], LEDs and LDs made by III-nitrides with different wavelengths were reported over the last two decades. The LEDs made by III-nitrides are playing a particularly important role nowadays. III-nitride visible LEDs have been widely used in general illumination, vehicle headlights, traffic lights, architecture lighting, road lighting, etc. III-nitride UV devices have important applications in biological detectors, equipment disinfection and water purification, etc. The blue LDs based on III-nitrides are applied for high-density storage optical disks, which is known as blue-ray technology [28].

III-nitride semiconductors have excellent thermal and chemical stability in addition to a high critical breakdown field as a result of their wide bandgaps. Due to intrinsic polarisation a high sheet carrier density of electrons can be generated at the interface between AlGaN and GaN in an AlGaN/GaN heterostructure without any modulation doping, which is different from AlGaAs/GaAs high electron mobility transistors (HEMTs). The inevitable defects obtained during doping process leads to alloy scattering effect and reduces the electron mobility. Without doping process, III-nitride becomes the best material for high-frequency, high temperature and high-power electronics. The first GaN metal-semiconductor field-effect transistor was demonstrated in 1993 [29].

The development of GaN electronic devices is in an intensive progress in particular in the field of radio frequency (RF) application, such as RF power amplifiers in 5G communication. However, the performance of current GaN electronic devices are far from what they should be in theory. This means that considerable effort will have to be devoted in order to achieve the best understanding of a number of fundamental issues.

1.3 III-Nitrides Challenges

Although the last two-decade effort has led to the successful commercialisation of blue LED technologies, these great achievements are still limited to III-nitride optoelectronics grown on c-plane substrates. This polar orientation also poses a number of great opportunities for further improving the performance of III-nitride optoelectronics, such as the “green/yellow” gap, efficiency droop, etc. The main challenges and fundamental issues in the development of III-nitrides will be discussed in detail in this section.

1.3.1 Quantum-Confined Stark Effect (QCSE)

Electrons and holes in excitons in bulk GaN are pulled apart or even ionised along the opposite directions under an external electric field. This becomes more complicated in a two-dimensional structure such as a quantum well structure consisting of quantum well and barrier, where potential barriers still confine electrons and holes as long as the external electric fields are below a threshold. For III-nitride visible or near UV emitters, InGaN is used as a quantum well with GaN as a barrier. Quantum wells confine the electrons and holes within a thin layer which increase the possibility of recombination and finally results in a higher quantum efficiency. For InGaN/GaN multi-quantum wells (MQW) grown on c-plane GaN, spontaneous and piezoelectric polarisation induced electric fields across the MQWs and the electric field is parallel to the c-direction. For piezoelectric of InGaN/GaN MQWs, the direction depends on the polarity of the crystal. The samples in this work are Ga-polarity, hence the polarisation constant is positive along the c-plane (0001) direction towards the surface which is opposite to the spontaneous polarisation. This generates the so-called quantum-confined Stark effect (QCSE).

Under the polarisation induced electric fields, the electrons and holes in InGaN quantum wells are displaced along opposite directions as schematically illustrated in Figure 1.1, which is also compared with its non-polar counterpart. As a result of QCSE, in the overlap of electron-hole wave functions are reduced and thus the internal

quantum efficiency (IQE) is decreased. Also, a red shift in the emitting wavelength is exhibited as a result of QCSE [30].

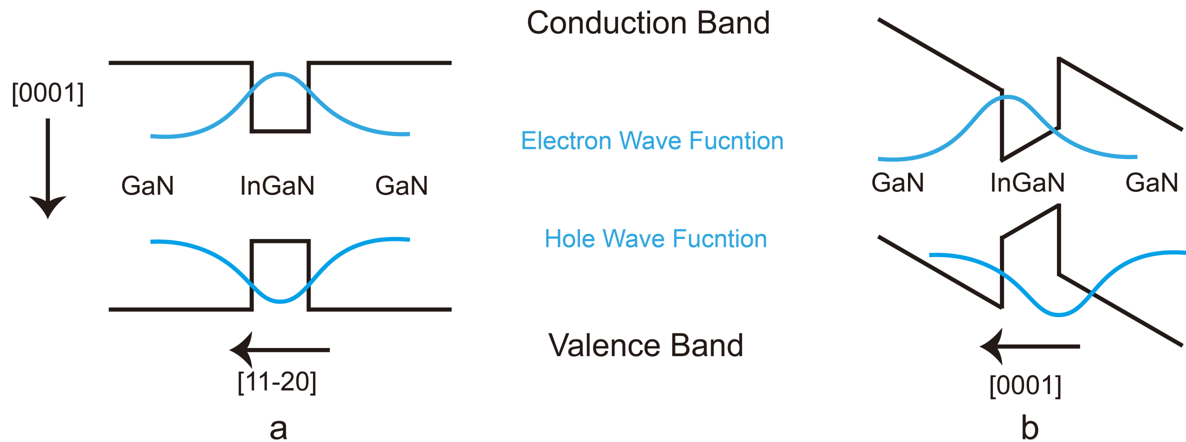

Figure 1.1: Band structure of InGaN/GaN MQWs grown on (a) (11$\bar{2}$0) non-polar GaN surface, where there is no polarisation induced electric fields and (b) (0001) c-plane, where the polarisation induced electrical fields are across the MQWs.

1.3.2 Efficiency Droop

It has been found that the efficiency of III-nitride LEDs initially increases with increasing injection current density at low current densities, normally less than 10 A/cm^2 [31], and then gradually reduces with further increasing injection current density at high current densities. This phenomenon is called efficiency droop. In order to explain the mechanism of efficiency droop, a number of models based on Auger recombination [32], electron overflow [33], defects [34], etc. have been put forward.

Auger recombination is one of non-radiative recombination processes, which involves a third carrier (either an extra electron or hole) which absorbs the energy released from the electron-hole recombination instead of emitting a photon. Electron overflow describes a process where the injected electrons from n-GaN overflow through InGaN MQWs as an active region and then directly arrive at p-GaN. Like any other models, these two models provide a reasonable explanation which are more likely to be the conclusion, but there is still no leading agreement of the cause.

1.3.3 Crystal Properties

GaN crystal exhibits high melting point and extremely high dissociation pressure [16], and thus it is extremely challenging to apply standard crystal production methods in manufacturing GaN substrate. Therefore, affordable GaN substrates are still not commercially available [35]. GaN has to be grown on foreign substrates such as sapphire or silicon. Of course, such hetero-epitaxial growth generates numerous problems such as a high dislocation density, which typically act as non-radiative recombination centres. For silicon substrates the situation becomes even more complicated, as the large difference of thermal expansion coefficient between GaN and silicon leads to severe cracking issues. Furthermore, there also exists so-called gallium melt back etching which will be discussed in the next chapter.

As stated above, InGaN/GaN LEDs grown on c-plane substrates suffer from electric field polarisation, leading to a reduction in quantum efficiency. This issue becomes more severe when InGaN/GaN LEDs move toward longer emission wavelength where high indium content in InGaN is required and results in an enhancement in piezoelectric polarisation. Therefore, the optical efficiency of InGaN/GaN based LEDs drops dramatically for longer wavelength emission such as green and yellow. From another end in the visible spectrum, it is well-known that longer wavelength devices such as AlInGaP LEDs exhibit a reduction in efficiency with decreasing wavelength from red to yellow, leading to the lowest efficiency in the yellow and even green spectral regions. Consequently, the lowest quantum efficiency in the green and yellow region is formed for all the existing III-V compound semiconductors. This is the so called "green/yellow gap" [36].

1.3.4 Epitaxial Substrates

As stated above, GaN is currently grown on foreign substrates, typically on sapphire, silicon, etc. SiC substrates are also sometimes used for the growth of GaN. The most widely used substrates at present in both industry and research is sapphire, which is a single aluminium oxide (Al_2O_3) crystal and thus is transparent. Sapphire has high

hardness and excellent stability at a high temperature, which is crucial for GaN growth as GaN growth requires a high temperature.

Sapphire exhibits a hexagonal crystal structure. In terms of crystal orientation there is c-plane (0001) for polar GaN growth, m-plane ($1\bar{1}00$) for semi-polar ($11\bar{2}2$) GaN growth and r-plane ($1\bar{1}02$) for non-polar ($11\bar{2}0$) GaN growth. (Major GaN crystal planes are illustrated in Figure 2.9) The lattice mismatch between sapphire and GaN is 16% [37]. Due to this large lattice mismatch, a high defect density is generated in GaN.

There is a growing interest of developing semiconductor devices with multiple functions, such as for the monolithic integration of electronic or photonic integrated circuits. Given that silicon technologies are mature, the integration of III-V compounds such as III-nitrides with silicon represents a future trend. However, silicon exhibits a cubic structure, which is different from wurtzite GaN. The lattice mismatch between (111) silicon and (0001) c-plane GaN is 17% [38]. The difference in coefficient of thermal expansion between GaN and silicon is as high as 155% [39]. Hence in addition to a high density of defects, cracking is easily generated during a cooling process after GaN growth at a high temperature. Furthermore, silicon easily reacts with gallium metal at a high temperature, which causes GaN epitaxial growth to collapse eventually leading to a stop in GaN growth. Therefore, GaN growth on silicon faces even greater challenges than that on sapphire.

Compared to either sapphire or silicon, silicon carbide (SiC) as a substrate exhibits the smallest lattice mismatch with GaN, which is only 3.5% [40]. Consequently, GaN grown on SiC substrate has much less dislocation density compared to sapphire or silicon substrate. However, the very expensive price of SiC limits the commercialisation of GaN on SiC. There are a number of other substrates such as zinc oxide (ZnO) [41], diamond [42], etc. but GaN on these substrates does not show competitive performance.

1.4 Motivation and Aim

Because of their wide band-gaps and excellent chemical and mechanical stability, III-nitride semiconductors have a great potential for a wide range of applications, such as general illumination, 5G mobile communications, visible light wireless communication (Li-Fi), high frequency, high power and high-temperature electronics, etc. Very recently there is an increasing demand for developing emitters and photodetectors with III-nitride materials for environmental protection, water purification, medical instrumentation, non-line-of-sight communications, etc. Moreover, the growth of GaN devices on industry-compatible silicon substrates exhibits advantages in terms of wafer costs, scalability, silicon technology compatibility and the integration of silicon photonics where the integration of III-nitride emitters/photodetectors and electronics can serve as a platform for the fabrication of photonic or electronic integrated circuits.

Due to an increasing demand such as scalability, cost reduction and integration with mature silicon technologies, the growth of III-nitride semiconductor on silicon substrates is one of the most promising options, in particular, in the area of manufacturing electronic devices [43]. A lot of industrial production lines are still silicon based. Presently, most of the commercialised III-nitride devices are based on sapphire substrates. Consequently, the development of III-nitride growth on silicon substrates has become a "hot topic" in the III-nitride semiconductor materials research. As stated above, the growth of III-nitrides on silicon substrates is facing a number of great challenges, in particular, the achievement of non-polar GaN devices on silicon.

C-plane III-nitrides on silicon have been widely developed worldwide, but have also demonstrated intrinsic challenges in further development [30], [31], while non-polar and semi-polar III-nitrides on silicon may be one of the promising solutions to address these challenges [44], [45], [46]. Researches on non-polar and semi-polar III-nitrides are mainly based on sapphire, while researches on non-polar and semi-polar III-nitride materials on silicon substrates are very limited due to great challenges from

the perspective of epitaxial growth of non-polar or semi-polar GaN. Even for epitaxy on sapphire, a high-density of defects has been observed. It is much more complicated when the substrate used is silicon, for which extra problems such as melt-back etching and cracking need to be overcome.

Our group has developed a novel HT-AlN buffer technology which leads to high crystal quality of c-plane, semi-polar and non-polar GaN on sapphire. The research carried out in this thesis is based on such a HT-AlN buffer technology. This work aims to develop high crystal quality $(11\bar{2}0)$ GaN stripes on patterned (110) silicon substrates by using our HT-AlN buffer. Two different kinds of device structures have been grown on such a high quality GaN stripes. A non-polar GaN metal-semiconductor-metal (MSM) photodetector (PD) with an ultra-high responsivity and an ultra-fast response speed in the ultraviolet spectral region have been achieved on the high quality non-polar $(11\bar{2}2)$ GaN stripe arrays. Furthermore, due to the stripe shape which forms two facets with different crystal orientations, an InGaN/GaN MQWs structure is grown on the GaN crystal to achieve multiple wavelength emissions. The optical properties of the GaN crystal and the InGaN/GaN MQWs structure are then investigated. Finally, our HT-AlN buffer technology with modification has been further applied in the growth of HEMTs with exceptional performance on c-plane sapphire, demonstrating the diverse functions of our HT-AlN buffer technologies.

1.5 Thesis Organisation

Chapter 1 briefly presents the history and development of III-nitrides with the main motivations and aims. Chapter 2 introduces the background of this research. Chapter 3 provides the details of the facilities required for carrying out this research. Starting from Chapter 4 the experiment details, the results and the result analysis are presented.

Chapter 4 provides the technical details about template fabrication for further overgrowth using the developed HT-AlN buffer technology on patterned (110) silicon substrates.

Chapter 5 presents the growth of non-polar $(11\bar{2}0)$ GaN stripes on the patterned (110) silicon substrates.

Chapter 6 demonstrates a non-polar GaN metal-semiconductor-metal (MSM) photodetector (PD) with an ultra-high responsivity and an ultra-fast response speed on patterned (110) silicon substrates

Chapter 7 demonstrates InGaN MQW structure with multi-wavelengths on non-polar GaN stripes on patterned (110) silicon substrates.

Chapter 8 demonstrates the universe of our HT-AlN buffer technology by employing the approach with modification in the growth of HEMTs with exceptional performance on c-plane sapphire.

Finally, conclusions and outlooks are provided in Chapter 9.

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Chapter 2

Background

This chapter presents the background of semiconductors (mainly III-nitride semiconductors) which is related to the research in this thesis in detail. This chapter is divided into three sections. General information about semiconductors is introduced in the first section. The second section specifically focuses on III-nitride semiconductors. Finally, the background for epitaxy of III-nitride semiconductors on silicon substrates is presented in the third section.

2.1 Semiconductors

Materials exist in different forms: gas, liquid, plasma and solid. Generally, solid materials can be categorised into three parts in terms of their electrical conductivity as conductors, insulators, and semiconductors, where the conductivity of a semiconductor can be tuned through a dopant method.

2.1.1 Band Structure

In a crystal which forms a periodic structure, there form a number of energy levels which allow electrons to stay which are called energy bands. At the temperature of absolute zero, the highest occupied energy band of a crystalline solid is full of electrons, and this energy band is called a valence band, while the lowest unoccupied energy band is called a conduction band. These two energy bands are separated by a bandgap as schematically illustrated in Figure 2.1, between which electrons from the valance band are forbidden to jump up to the conduction band [1]. Insulators and semiconductors have their Fermi levels inside their bandgaps. For insulator, the bandgap is so large that the electrons from the valence band cannot be energised and excited by thermal energy or external electric field to the conduction band. The Fermi level of the insulator are far away from any states that are able to carry current. The electrons cannot freely move and tightly bound in the state of a valence band.

Semiconductors has smaller bandgap compare to insulator. The Fermi level of the semiconductor is closer to the band edges. Fermi level of the semiconductor can usually be controlled by doping which cause the shift of the entire band structure (sometimes also cause the distortion of the band structure). The conductor has the Fermi level inside the delocalised band and a large number of states are readily to carry current.

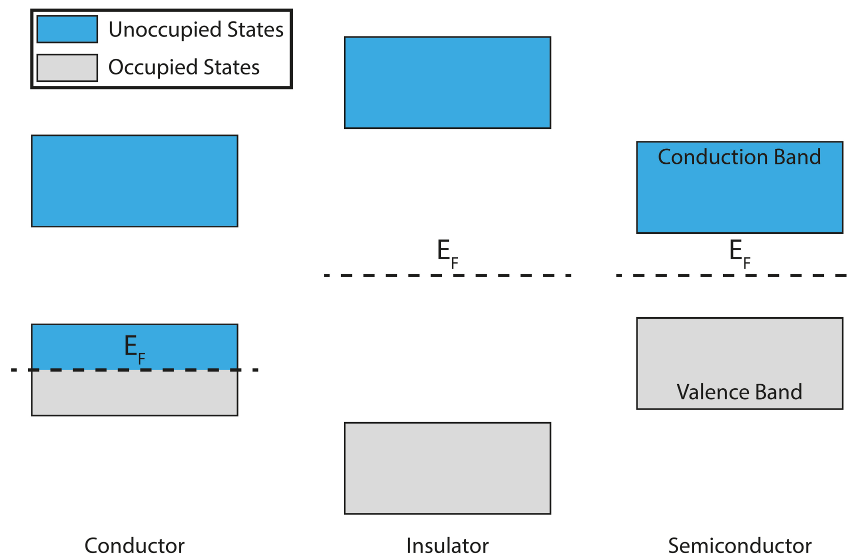

Figure 2.1: Schematic of the band structure of conductor, insulator, and semiconductor.

The band structure of a semiconductor can be categorised into two types: direct bandgap and indirect bandgap. This is defined based on an alignment between the valence band maximum and the conduction band minimum of a semiconductor in k-space (i.e., momentum space). A semiconductor with a direct band structure has the same k value for both the valence band maximum and conduction band minimum. In an indirect bandgap semiconductor, the k values of those are different. Therefore, a recombination process between electrons and holes are straightforward in direct bandgap semiconductors. In contrast, for an indirect bandgap semiconductor, a recombination process between electrons and holes has to involve a third party in order to maintain the momentum conservation [2]. With the excitation of light, the semiconductors can absorb it and then generate a pair of new carriers or an exciton. Besides the absorption, the light can stimulate a recombination event. The recombination can be separate into radiative recombination and non-radiative

recombination. The carriers in semiconductors can also be generated by the excitation of the external electric field.

Figure 2.2 illustrates a schematic of a recombination process between electrons and holes in a direct bandgap and an indirect bandgap semiconductor. For an indirect bandgap semiconductor, an extra phonon has to be involved in the recombination process in order to maintain the energy momentum (k) conservation, it can also be substitute by the involving of a crystallographic defect. Thus, the transitional probability between electrons and holes is reduced and leading to a significant reduction in optical efficiency. However, there is no such a restriction for a direct bandgap semiconductor. This makes direct bandgap semiconductors are much more favourable for the fabrication of emitters such as light-emitting diodes or laser diodes.

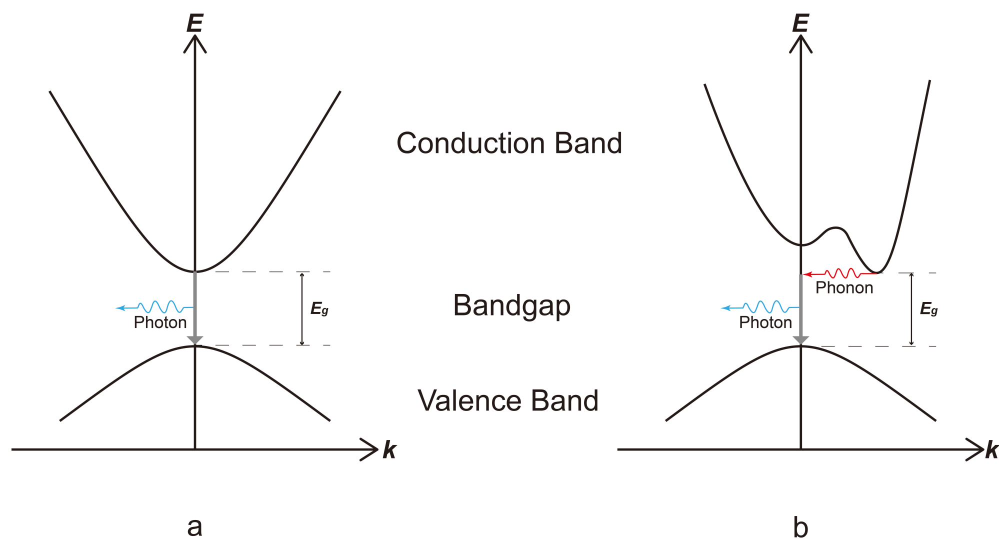

Figure 2.2: Schematic of a recombination process between electrons and holes in: (a) a direct bandgap; and (b) an indirect bandgap semiconductor.

2.1.2 Doping

Generally, doping is a process for deliberately introducing impurities into a semiconductor in order to tune the electrical properties of the material by generating extra free electrons or holes via thermal energy (K_BT, which is 26 meV at room temperature). In terms of the type of extra carriers generated by the dopant, there are p-type and n-type semiconductors. For the former, the dopants used for p-type are called acceptor while the dopants for n-type are called donor. For III-nitrides,

magnesium (Mg) is a typical p-type dopant source, and Mg atoms are introduced to substitute gallium (Ga) atoms, Mg-doped GaN then becomes free holes dominated semiconductor, while silicon (Si) is introduced to form n-type doping. Si atoms replace Ga atoms, providing extra electrons. For p-type GaN, there are several issues observed after the activation of implanted p-type dopant, such as a loss of nitrogen, surface damage and the creation of nitrogen vacancies [3].

2.1.3 Luminescence

When electrons in their excited state relax from a high energy level to a low energy level, for example, from a valence band to the conduction band, photons are emitted. This process is called luminescence. There are two types of luminescence involved in this thesis: photoluminescence and electroluminescence. The difference of the two types of luminescence is the excitation source where photoluminescence is excited by radiation and electroluminescence is excited by electric current or strong electric field.

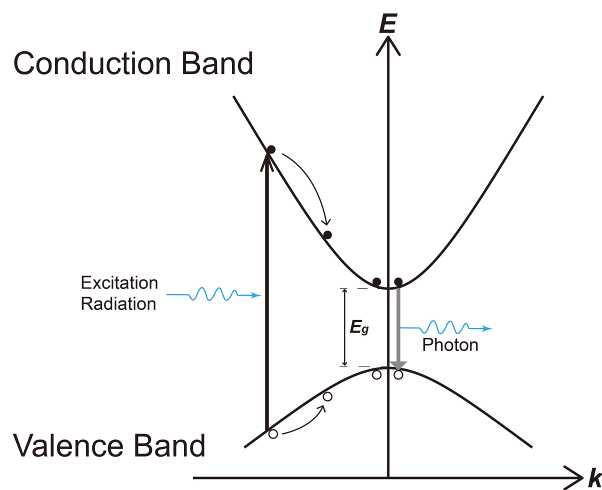

Figure 2.3: Schematic of a photoluminescence process.

Figure 2.3 is a schematic of photoluminescence process for a direct bandgap material, where an excitation source with photon energy is higher than the bandgap of the investigated material is used, typically, a laser. Under excitation conduction, electrons are initially excited from a valence band to a conduction band, leaving holes in the valence band, and then a recombination of electrons and holes takes place, emitting

photons. Electroluminescence is generated when an electrical current is injected across the material under forward bias.

2.1.4 Crystal Defects

For GaN epitaxial films grown on foreign substrates such as sapphire, GaN typically exhibits a high density of defects. There are generally four types of defects: point defects (zero dimensional), line defects (one dimensional), planar defects (two dimensional) and bulk defects (three dimensional).

Point Defects

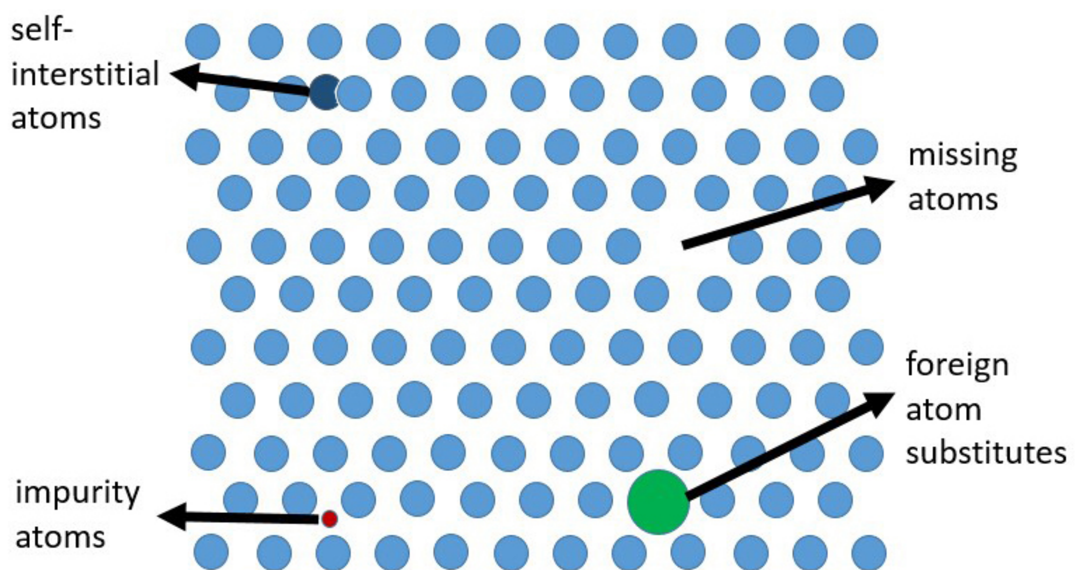

Figure 2.4: Schematic illustration of point defects.

Point defects are zero-dimensional defects. There are mainly four kinds of point defects and these can be separated into two categories; whether defects are intrinsic or extrinsic depends on the intervention of foreign atoms (Figure 2.4). A vacancy defect corresponds to the absence of an intrinsic atom. When an intrinsic atom is inserted into the space between the basic atoms, it is called self-interstitial atoms, these two defects are intrinsic. Extrinsic defects occur due to the introduction of foreign atoms, called impurities. There are two types of extrinsic defects. One is a foreign atom substitutes an intrinsic atom and the other is an impurity atom inserts into the basic atom spaces.

Line Defects

Line defects, or dislocations, are normally caused by the misalignment of an atom line. They are generally characterised by Burgers vector and dislocation lines. Burgers vector ***b*** defines the magnitude and direction of the disordered lattice and dislocation line describes the place where distortion happens. In general, dislocation line points out the direction of the dislocation and the Burgers vector give the magnitude and direction of the disordered lattice associated with the dislocation. The two main defined dislocations are the edge dislocations and the screw dislocations which differ by the directions between Burgers vector and dislocation lines.

Figure 2.5 illustrates the two types of dislocations in which the short arrow indicates the Burgers vector and the long arrow indicates the dislocation line: an edge dislocation if the two parameters are perpendicular to each other (90) and a screw dislocation if they are parallel (00). Sometimes, dislocations are featured with both screw and edge characters, meaning that the line direction and Burgers vector are neither perpendicular nor parallel.

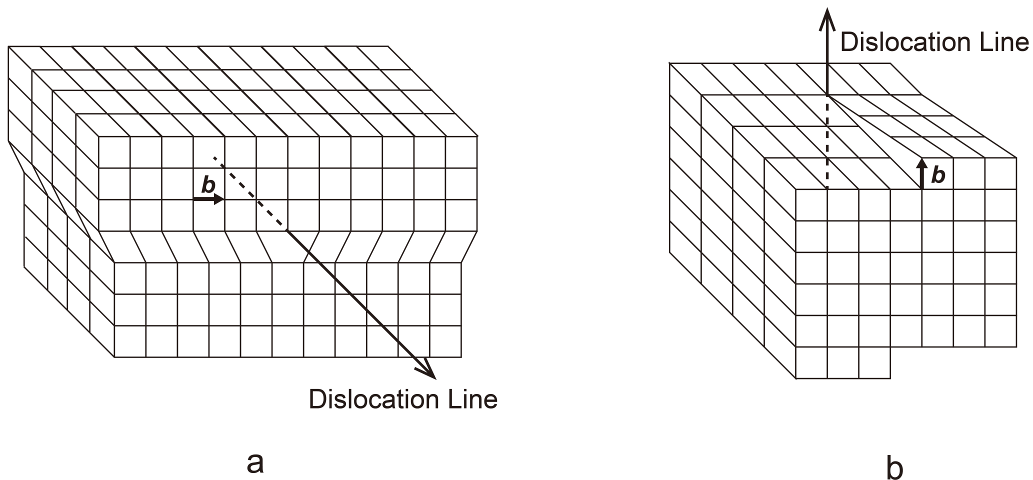

Figure 2.5: Schematics of (a) an edge dislocation; (b) a screw dislocation.

Planar Defects

Stacking faults are generated due to a wrong sequence of crystallographic planes. There are two main types of stacking faults: basal stacking fault (BSF) and prismatic

stacking fault (PSF). BSFs lie on the basal plane (0001) while PSFs lie on the prism plane ($1\bar{1}00$) [4]. During non-polar and semi-polar GaN epitaxy, as the c-plane is not parallel to the growth direction, the BSFs can extend to the top surface. This would significantly influence the optical properties of the non-polar and semi-polar devices as well as the surface morphology. BSFs can also cause electrical leakage which is detrimental to optoelectronic and electronic device operation [5].

Bulk Defects

Bulk defect happens on a relatively larger scale. Normally they are generated by the absence of a large number of atoms or caused by a cluster of impurity atoms. Cracks can be also considered as bulk defects. This is quite common when III-nitrides are grown on silicon substrates, due to the large thermal coefficient difference between the two materials. Bulk defects can damage a sample from the bottom to top surface.

2.2 III-Nitride Semiconductors

III-nitrides exhibit direct bandgap structures with a wide bandgap range from deep UV through the whole visible to infrared region. This section introduces the fundamental crystal structure and properties of III-nitrides, followed by the discussion on the tuneable bandgap across the entire alloy composition. Finally, a discussion on non-polar III-nitrides is presented.

2.2.1 Crystal Structure

For III-nitride semiconductors, there are three different crystal structures: wurtzite, zincblende [6] and the rock-salt structure. The rock-salt structure can generally only be achieved under extremely high pressure [7]. A zincblende or cubic structure can be obtained by growth on a cubic substrate, but it may easily transform into a wurtzite structure which exhibits much more thermodynamic stability. To keep GaN in zincblende structure, extra compressive stress needs to be obtained[8], [9]. A wurtzite structure is the most common structure of III-nitrides. This thesis only focuses on the research of III-nitride semiconductors with a wurtzite structure.

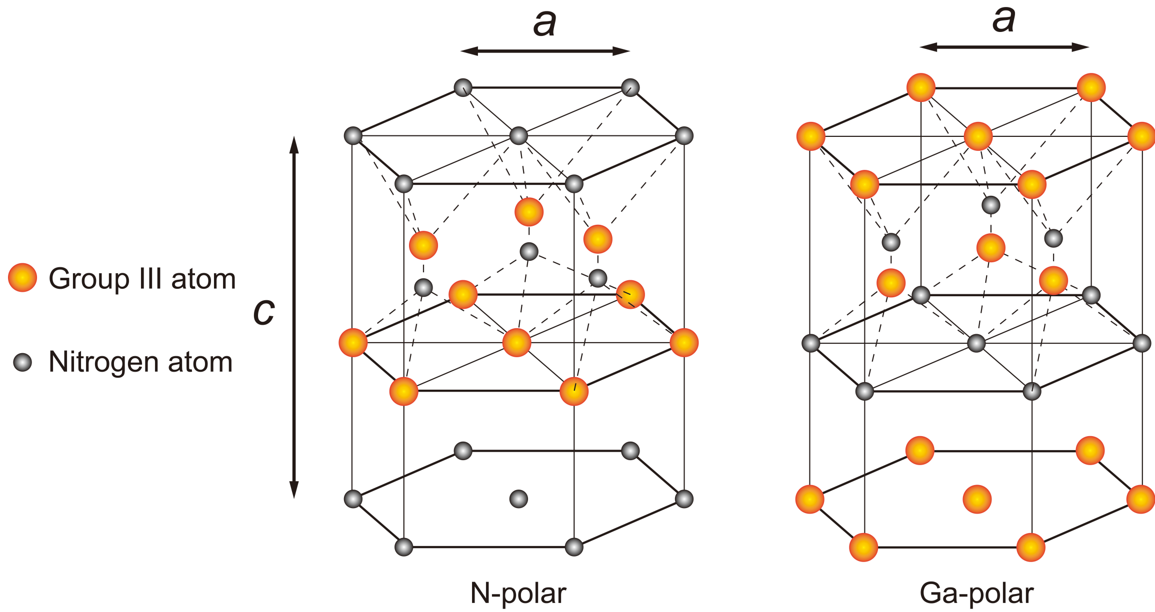

Figure 2.6: Schematics of III-nitride semiconductor with the wurtzite crystal structure.

Figure 2.6 shows a III-nitride semiconductor with a wurtzite crystal structure, where the grey spots represent nitrogen atoms and the gold ones are group III atoms such as gallium, aluminium, or indium. In this kind of crystal structure, every single nitrogen atom relates to four group III atoms. This makes the whole crystal form a hexagonal closed packed configuration. This hexagonal crystal unit cell can be defined by two parameters: the in-plane lattice constant a and an out-of-plane lattice constant c as schematically illustrated in Figure 2.6, labelled as two double arrow lines, respectively. The constant a indicates the distance between two adjacent atoms in the basal plane and constant c indicates the distance between two basal planes.

	AlN	GaN	InN
Lattice constant a (Å)	3.1112	3.18926	3.533
Lattice constant c (Å)	4.982	5.18523	5.693

Table 2.1: Lattice constants of wurtzite III-nitrides.

Table 2.1 above gives the lattice constants of III-nitrides: aluminium nitride (AlN), gallium nitride (GaN) and indium nitride (InN) [10].

Bravais Miller indices (h, k, i, l) are introduced to describe the plane and the direction of crystal lattice [11]. Figure 2.7 illustrates that the indices (h, k, l)

represents the intercept reciprocals along the three directions (a_1, a_2, a_3) inside a basal plane where l indicates the intercept reciprocals along c axis. In a wurtzite structure, $i = -(h + k)$, the Miller indices will normally be shown as (h, k, l).

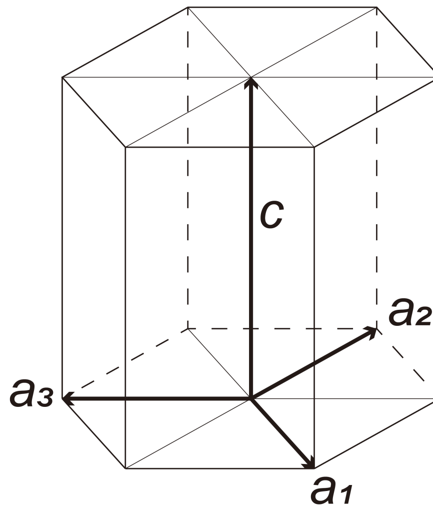

Figure 2.7: Bravais Miller indices in a wurtzite unit cell.

Figure 2.6 shows two types of GaN crystal structures with different atoms terminated on the top layers which are nitrogen atoms terminated and gallium atoms terminated. They are described as the N-polar and the Ga-polar, respectively. They can be indicated by Miller index system in which (0001) indicates the Ga-polar and (000-1) is the N-polar. The surface morphology of the two types of GaN layers is different. A smooth surface is normally observed for a Ga-polar GaN layer whilst the rough surface of N-polar GaN typically features hexagonal hillocks. The nitrogen atoms at N-face surface has much possibility to be combined in the extremely favourable reactions leading to the less stability of N-face GaN. Besides the influence on surface morphology, the polarity affects other properties of III-nitrides such as defects, chemical status, doping level, internal polarisation, etc., which in return determine electrical and optical performance. Intrinsic GaN with Ga-polar is inert and thus is hardly etched by either acids or alkaline solutions, while chemical etching processes can easily happen through surface defects or N-polar GaN.

2.2.2 Properties

The physical and chemical properties, such as melting point and thermal conductivity, as well as the electrical properties such as electron mobility and electrical breakdown field of GaN and other commonly used semiconductors are summarised in Table 2.2 [12]–[20].

Material	Thermal Conductivity ($W{\cdot}cm^{-1}K^{-1}$)	Melting Point (°C)	Electron Mobility ($cm^2V^{-1}s^{-1}$)	Breakdown Field ($kVcm^{-1}$)
GaN	2.3	2500	1245	5000
GaAs	0.55	1238	9400	400
Si	1.56	1414	1400	300
InP	0.68	1062	4000	500

Table 2.2: Semiconductor material properties at 300K.

Electron mobility is a parameter which is used to describe how quickly an electron can move within a material such as a semiconductor. One of the major mechanisms which determine electron mobility is due to scattering. Electron scattering may come from impurities, defects, phonons, etc. The highest electron mobility of a GaN thin film grown by MOCVD at room temperature reported so far is $1005\ cm^2V^{-1}s^{-1}$ while an electron mobility of $1245\ cm^2V^{-1}s^{-1}$ has been reported for HVPE epitaxy bulk GaN [19]. Compared to other semiconductors, GaN exhibits a higher breakdown voltage and a higher thermal conductivity.

2.2.3 Tuneable Bandgaps of III-Nitrides

Figure 2.8 summarises the major semiconductors in terms of energy bandgaps and lattice constants, which shows the bandgaps of III-nitrides can cover a wide range of spectrum including the whole visible spectrum. The lattice constant of III-nitride alloys as a function of composition can be illustrated by Vegard's law.

$$a_{A_xGa_{(1-x)}N} = (1-x)a_{AN} + xa_{GaN} \quad 2.3$$

where element A represents In or Al. $a_{A_xGa_{(1-x)}N}$ represents the lattice constant of the alloy. a_{AN} and a_{GaN} are the lattice constants of InN or AlN and GaN, respectively.

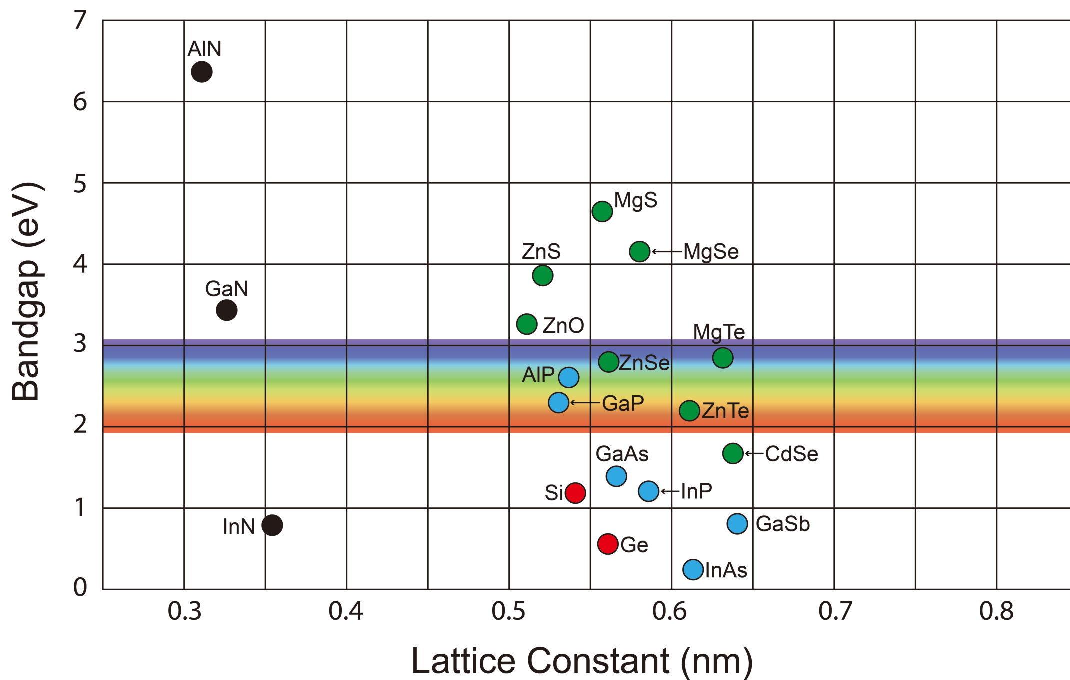

Figure 2.8: Bandgap vs lattice constant at 300K (Rebuild from [20]).

Material	Bandgap (eV)	Wavelength (nm)
AlN	6.2	200
GaN	3.42	363
InN	0.78	1590

Table 2.3: Bandgaps and luminescence wavelengths of III-nitrides.

Similarly, the bandgap of III-nitride alloys can be described by a linear relationship in a first-order approximation. Table 2.3 gives the bandgaps and their corresponding wavelength [14]. Thus, the wavelength of III-nitrides is alterable by forming ternary compounds with AlN, GaN and InN. In the UV spectral range, the wavelength can be tuned by adding aluminium composition into GaN. From the near UV to infrared, the indium composition in InGaN alloy determines the wavelength. In theory, InGaN covers the whole visible spectrum. The tuneable wavelength with a wide spectral range makes III-nitrides attractive for the fabrication of optoelectronic devices in both the UV and visible spectral regions. For now, low energy part of the spectrum

like red is not fully covered by III-nitride materials in practise, due to the low efficiency with high indium content. But green and blue range of the visible light spectrum is dominated by III-nitrides.

2.2.4 Non-polar and Semi-polar III-Nitrides

The most attractive property of non-polar and semi-polar III-nitrides is their reduced QCSE. This significantly increases the internal quantum efficiency (IQE) of III-nitrides emitters. Figure 2.9 illustrates six common planes of a wurtzite GaN with different orientations labelled by using Miller indices.

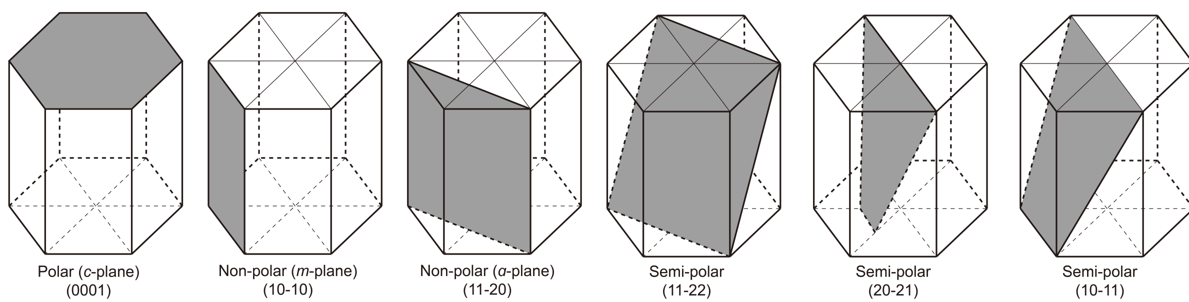

Figure 2.9: Crystal structures of six common hexagonal planes.

C-plane polar III-nitrides have been widely used and commercialised in the past decades. Non-polar planes are perpendicular to the c-plane. This thesis focuses on the research about non-polar $(11\bar{2}0)$ GaN. For semi-polar planes, they have an inclined angle in the range of 0° to 90° with respect to c-plane, the cosine of the inclined angle can be calculated by applying the Miller index and the lattice constants. For example, $(11\bar{2}2)$ plane has an inclined angle of 58.41° with respect to c-plane [21]. The inclined angle with respect to c-plane is the main reason for the reduction in the piezoelectric polarisation for semi-polar and non-polar III-nitrides. This results in a decrease in QCSE.

Using an InGaN as an example (AlGaN behaviour is also similar), Figure 2.10 illustrates the polarisation of InGaN with different indium compositions as a function of inclination angle with respect to c-plane. The total polarisation is the sum of spontaneous polarisation and piezoelectric polarisation which have the opposite directions. The directions of the two polarisations are fixed but the values vary

according to the orientation of the crystal. Starting from 0° inclination angle which is c-plane, the polarisation decreases with the increasing of the inclination angle and terminates at 0 at 55° inclination angle. The polarisation reverses [22] beyond that afterwards and finally is eliminated for non-polar InGaN with an inclined angle of 90°.

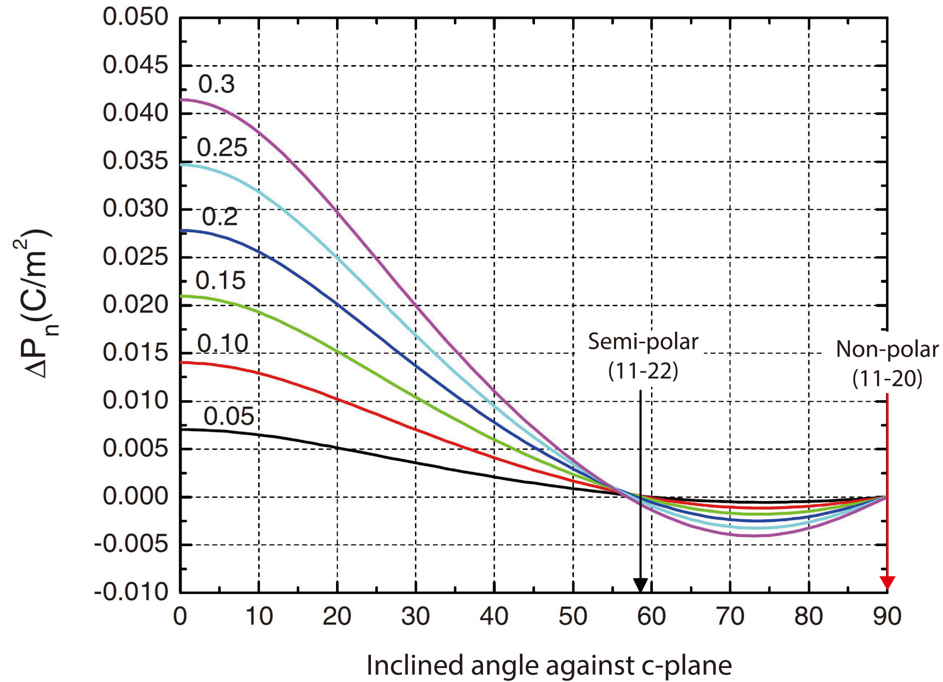

Figure 2.10: Polarisation as a function of inclined angle against c-plane of InGaN QWs with different indium compositions (Reproduced from [23]).

2.3 III-Nitrides Epitaxy on Silicon Substrates

Although there exist a number of advantages of using silicon substrates for GaN growth as stated in Chapter 1, the epitaxial growth of GaN on silicon substrates poses great challenges. This section starts with an introduction of the development of III-nitride epitaxial growth on silicon substrates, followed by presenting the major growth issues as a result of lattice mismatch, thermal expansion coefficient difference, and melt-back etching. Finally, the growth mechanism is briefly discussed.

2.3.1 Development of III-Nitrides Epitaxy on Silicon Substrates

By using a thin AlN buffer layer, the first GaN LEDs by MOCVD on Si were reported in

1999 [24]. Compared to the GaN-on-sapphire technologies which have been well established, GaN-on-Si suffers a wide range of issues from poor and cracking surface morphology to significantly low crystal quality, in particular, a high density of cracking which is often observed on GaN on silicon. In order to address these challenges, various methods have been proposed, such as selective growth on mask patterned templates [25], [26], selective growth on the etched templates [27], epitaxial lateral overgrowth (ELOG), etc.

Due to a number of challenges for non-polar or semi-polar GaN growth on Si substrate, there have been only a limited number of reports in literature so far. Due to the lack of epitaxial relationship between non-polar or semi polar GaN on any orientated Si substrate, in principle it is impossible to grow non-polar or semi-polar GaN on a planar silicon substrate. Therefore, it needs a patterned silicon as a substrate for the growth of semi-polar or non-polar GaN.

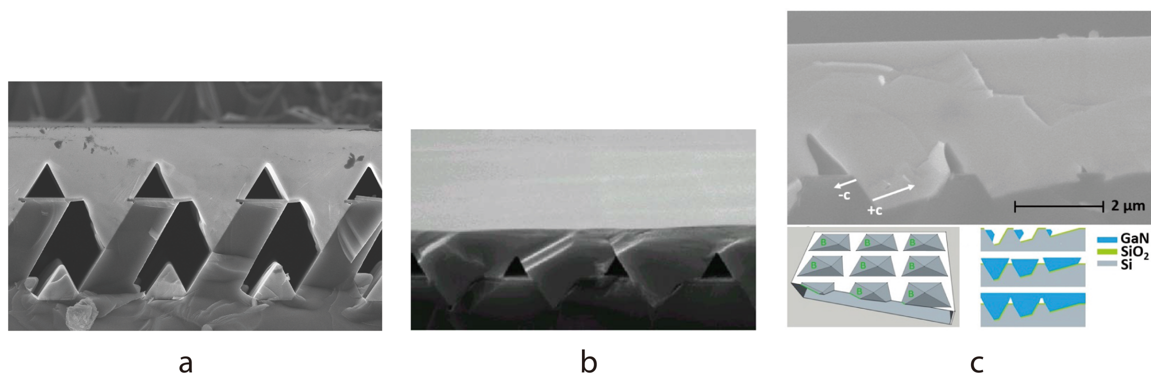

Figure 2.11: SEM images of $(11\bar{2}2)$ GaN on (a) trench, (b) groove and (c) hole patterned Si.

For example, for $(11\bar{2}2)$ semi-polar GaN grown on Si, Figure 2.11 shows a few examples of patterned silicon substrates: the first one is trench-like [28] as depicted in Figure 2.11a, the second one is groove-like as shown in Figure 2.11b [29], and the third one is based on arrayed micro-hole pattern (in Figure 2.11c) which was developed by our group [30], [31]. All these patterns are based on (113) silicon substrates which will be detailed in the next section. GaN on Si can achieve different orientations with various silicon orientations.

So far, the development of non-polar GaN on silicon lags behind its semi-polar

counterparts on silicon. Two kinds of non-polar GaN are interesting: $(11\bar{2}0)$ non-polar GaN on (110) silicon [32], and $(1\bar{1}00)$ non-polar GaN on (112) silicon [33]. As stated above, patterned silicon substrates are required in order to obtain non-polar GaN.

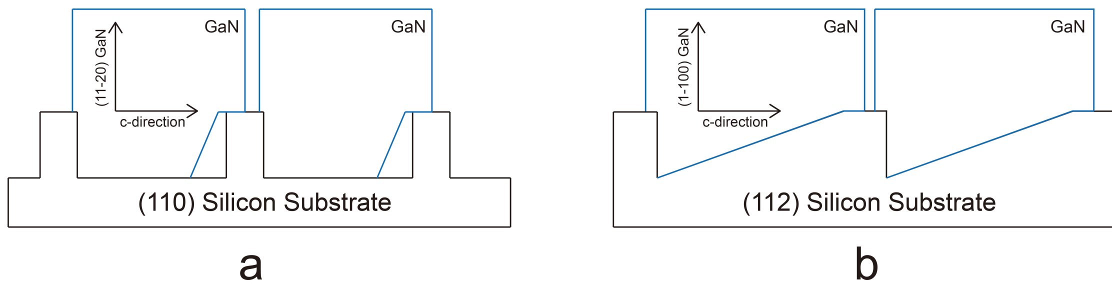

Figure 2.12: Cross-sectional schematic of non-polar GaN growth on silicon substrates. (a): $(11\bar{2}0)$ GaN on (110) Si; (b): $(1\bar{1}00)$ GaN on (112) Si.

Figure 2.12 illustrates schematic of non-polar GaN grown on these two patterned silicon substrates. For (110) silicon, a trench style pattern is required, while a groove pattern is required for (112) silicon substrates. Non-polar GaN grown on such patterned (110) silicon exhibits $(11\bar{2}0)$ orientation while $(1\bar{1}00)$ nonpolar GaN can be obtained on such patterned (112) silicon. The fabrication mechanism behind these two types of substrates is to form (111) facets on which selective growth of GaN is subsequently carried out. Such patterned silicon substrates can be obtained by using anisotropic chemical etching, which will be discussed in detail.

2.3.2 Lattice Mismatch

Normally, c-plane (001) GaN crystal forms a wurtzite structure with a six-fold surface symmetry, and (001) silicon crystal has a four-fold surface symmetry like GaAs. They do not match each other. To grow GaN on silicon substrates an orientation of silicon surface that fits the six-fold surface symmetry need to be introduced. However, (111) silicon has a surface with three-fold surface symmetry. Hence (111) silicon is the best choice for GaN growth on silicon substrates.

Although (111) silicon substrate is ideal for GaN growth, compared to silicon substrates with other orientations the lattice mismatch is still high. Figure 2.13 shows the planar structures of (111) silicon and (001) GaN.

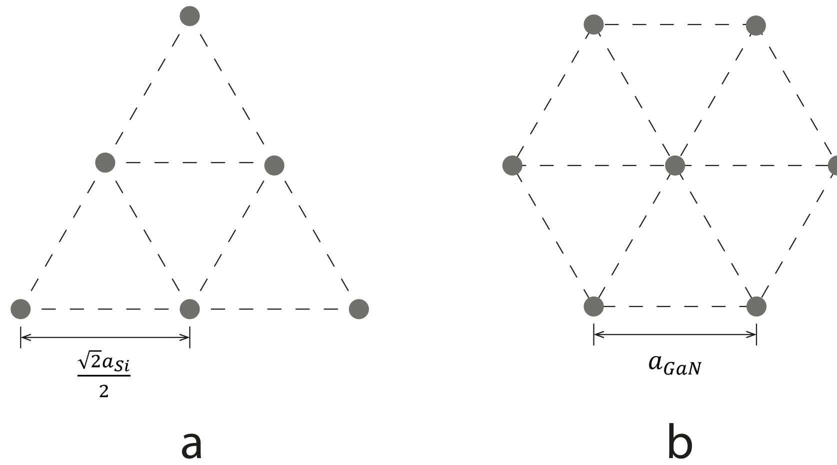

Figure 2.13: Planar schematics of (a): silicon atoms of (111) Si; (b): gallium atoms of (001) GaN.

The lattice mismatch between (001) GaN and (111) silicon is calculated by the formula below:

$$\frac{a_{GaN}-\frac{\sqrt{2}a_{Si}}{2}}{\frac{\sqrt{2}a_{Si}}{2}} = -17\% \qquad (2.4)$$

In this equation, $a_{Si} = 5.432\ \text{Å}$ is the in-plane lattice constant of cubic silicon and $a_{GaN} = 3.190\ \text{Å}$ is that of wurtzite GaN. This indicates that the GaN suffers tensile strain as a result of the lattice mismatch of 17% between GaN and silicon.

2.3.3 Epitaxy Mechanism

It is well-known that it is preferable to grow GaN on the (111) silicon facets due to the thermal dynamic stability at a high temperature. In order to obtain non-polar or semi-polar GaN on silicon, the idea is initially to achieve inclined (111) silicon facets with respective to the normal of silicon substrate. Semi-polar or non-polar GaN can be obtained by performing selective growth only on the inclined (111) facets. The inclined angle of (111) facets depends on different oriented silicon, leading to the finally formed GaN with either non-polar or semi-polar orientation. The formation of (111) facets is to use wet etching by potassium hydroxide (KOH) solution due to anisotropic etching mechanism. Due to the naturally anisotropic properties of silicon, chemical etching almost stops once the etching front meets (111) facets, as KOH solution can

etch any silicon facet except the (111) facet.

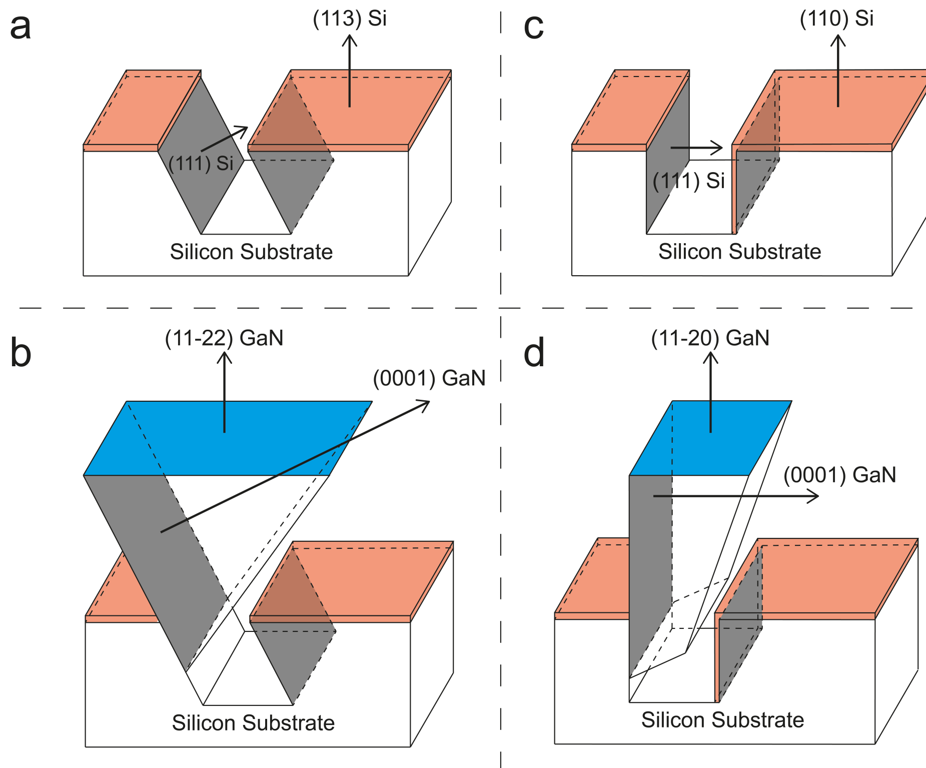

Figure 2.14: Schematics of (11$\bar{2}$2) and (11$\bar{2}$0) GaN on silicon substrates growth process. (a): Patterned (113) silicon substrate for the growth of (11$\bar{2}$2) GaN; (b): Growth of (11$\bar{2}$2) GaN on (113) silicon substrate; (c): Patterned (110) silicon substrate for the growth of (11$\bar{2}$0) GaN; (d): Growth of (11$\bar{2}$0) GaN on (110) silicon substrate.

Figure 2.14 illustrates two examples for the growth of semi-polar and non-polar GaN on patterned (113) and (110) silicon templates, respectively. After KOH etching under certain pattern, the silicon substrates form stripes with two parallel facets. For (113) silicon substrates, the two facets form an inclined angle with top surface. For (110) silicon substrates, the two facets are orthogonal to top surface. A top layer labelled as red indicates silicon dioxide masks as shown in Figure 2.14a and 2.14c. The grey coloured planes represent the (111) silicon facet formed after etching for subsequent selective growth. Figure 2.14b illustrates the growth of (11$\bar{2}$2) GaN on patterned (113) silicon substrate, where the formed surface labelled as blue is (11$\bar{2}$2) GaN when GaN is selectively grown on the (111) facet labelled as grey. The (11$\bar{2}$0) GaN growth on (110) silicon substrates has a similar situation. Figure 2.14c shows the formed (111) silicon facet labelled as grey for selective GaN growth, and Figure 2.14d shows the finally formed (11$\bar{2}$0) GaN surface labelled as blue as a result of selective overgrowth on a

patterned (110) silicon substrate.

2.3.4 Thermal Expansion Coefficient Mismatch

Direction of the lattice mismatch of GaN growth on silicon is parallel to lattice constant a. The thermal expansion coefficient of lattice constant a of silicon (2.6E-6K^{-1}) has much smaller value than GaN (5.59E-6K^{-1}). Between them the mismatch of thermal expansion coefficient is 115%. GaN obtained by MOCVD normally requires a high temperature, typically above 1000 °C. The large lattice mismatch generates tensile stress on GaN, leading to cracking and wafer bowing during cooling processes after growth [34]. This situation becomes increasingly serious with increasing GaN layer thickness above 1 μm.

2.3.5 Melt-back Etching

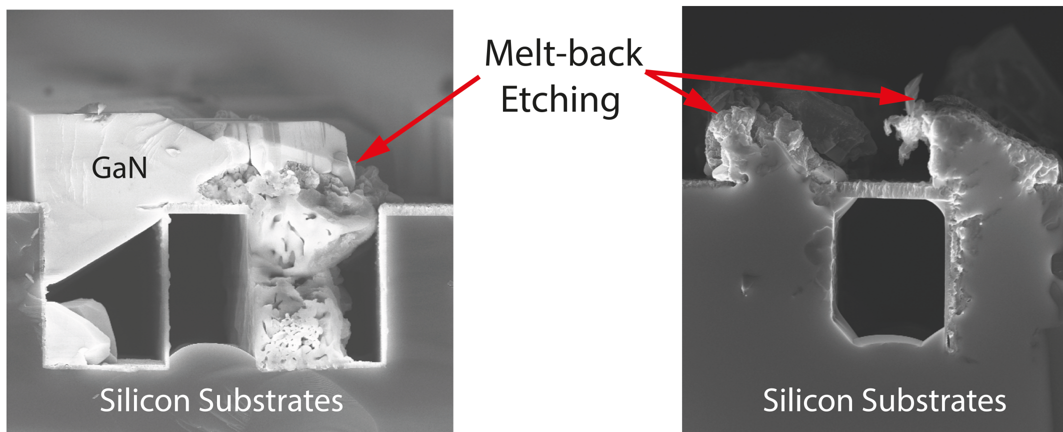

Figure 2.15: Cross-sectional SEM images of (11$\bar{2}$0) GaN growth on patterned (110) silicon with melt-back etching.

Melt-back etching has always been a serious issue for research of GaN growth on silicon over many years. It is an irreversible reaction between gallium and silicon at a high temperature. The result of the reaction is to form an eutectic Ga/Si alloy [35], [36]. As GaN growth needs to be performed at a high temperature over 1000 °C, this high temperature makes melt-back etching happen easily when gallium metal meets silicon. During GaN growth at such a high temperature, silicon from the substrate out-diffuses up to the epitaxially grown GaN which will then react with silicon. As a result

of melt-back etching, the GaN is heavily damaged as shown in Figure 2.15. Since this reaction is irreversible it is impossible to process such GaN with melt-back etching for further device fabrication or further growth.

To solve melt-back etching, it is important to initially deposit an extra layer in order to separate silicon and the subsequently grown GaN. Normally, an AlN layer is introduced. In this case, the quality and surface morphology of the AlN layer may highly affect melt-back etching [37], and also the crystal quality of the subsequently grown GaN. Another option is to reduce the growth temperature in order to eliminate melt-back etching, as melt-back etching can only take place at a high temperature [38]. GaN grown at a low temperature exhibits significantly low crystal quality. To achieve uniform GaN layer with high quality and smooth surface, melt-back etching must be eliminated.

2.4 Semiconductor Devices

This section presents two typical kinds of devices that can potentially be fabricated by using III-nitrides: photodetector (PD), high-electron-mobility transistors (HEMTs).

2.4.1 Photodetector (PD)

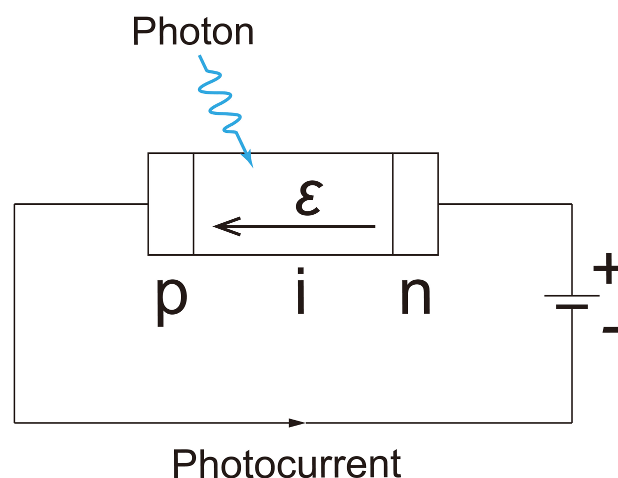

Figure 2.16: Schematic of a photodiode detector.

Figure 2.16 shows the schematic of a p-i-n photodetector operating under reverse-

bias. A thin intrinsic layer which is called an “i” region is sandwiched between p-type and n-type layers. Under reverse bias, only a leakage current is formed under dark conditions in a closed circuit as shown in Figure 2.16. Under illumination conditions, electron-hole pairs will be generated, leading to photon-induced current formed in the circuit under the bias. This current is called photocurrent.

A metal semiconductor metal photodetector (MSM-PD) is another kind of photodetector [39]. An MSM-PD was first proposed and developed by Sugeta et al. in 1979 [40], [41]. In 1981 it was also reported by Slayman and Figueroa [42], [43] and by Wei et al [44]. To enhance the performance of an MSM-PD by reducing dark current, the concept of an additional thin barrier-enhancement layer was introduced in 1988 [45]–[47]. Recently, the research of GaN-based MSM-PD has attracted a lot of interest due to different applications in the UV spectral region, such as photodetector, transistor for switching application and HEMT [48]–[51]. The major issues are due to a low responsivity and a slow response speed as a result of c-plane GaN which suffers from the polarisation issues.

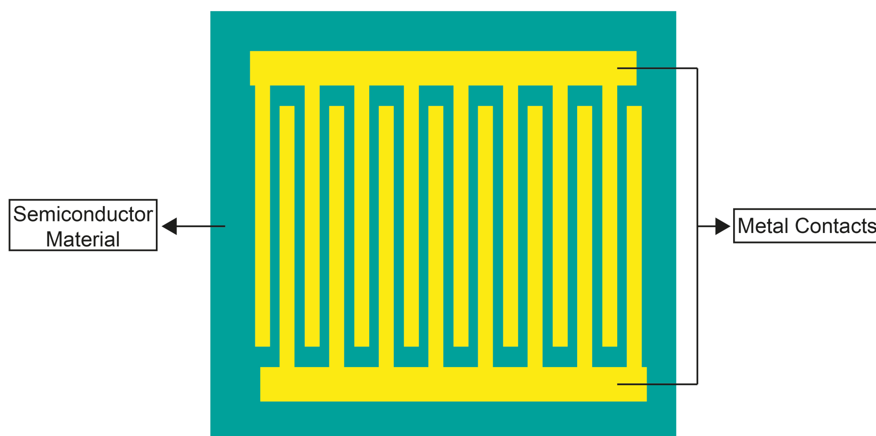

Figure 2.17: Schematic of an MSM-PD.

A typical MSM-PD can be fabricated by depositing a pair of metal interdigitated fingers on a semiconductor to generate two Schottky barriers that are connected back to back as shown in Figure 2.17. The areas between two metal contacts absorbs any incident signals. Compared to a standard Schottky-barrier PD, a MSM-PD can eliminate light absorption by metal contacts [52]. The main advantages of a MSM-PD are due to their high response speed and compatibility with FET technology [15].

The general characteristics of a photodiode are the quantum efficiency, response speed and device noise.

Equation 2.5 describes a quantum efficiency which is defined as the number of the electron-hole pairs generated per incident photon:

$$\eta = \frac{I_{ph}/q}{P_0/h\nu} \tag{2.5}$$

where I_{ph} is photocurrent generated by the PD and P_0 is the incident optical power. Responsivity is commonly used to characterize the performance of a PD which is defined as the ratio of the photocurrent to the optical power as expressed by Equation 2.6:

$$\Re = \frac{I_{ph}}{P_0} = \frac{\eta q}{h\nu} = \frac{\eta\lambda}{1.24}(A/W) \tag{2.6}$$

where η is the quantum efficiency. For an ideal photodiode, quantum efficiency η is 100% and the responsivity is $\lambda/1.24\,(A/W)$. Normally quantum efficiency is determined by optical absorption, surface reflectivity and internal quantum efficiency [15].

Response speed is commonly characterised by response time, which is mainly determined by a transit time between two contacts. The detail of this part will be introduced in Chapter 6, Section 6.3.2.

The main noise mechanisms for a photodiode are due to Johnson (thermal) noise and generation-recombination noise. Johnson noise is the result of the random motion of carriers, contributing to dark current. Generation-recombination noise is due to the fluctuation in the rates of generation and recombination of electron-hole pairs.

2.4.2 High-Electron-Mobility Transistor (HEMT)

GaN-based power devices have also been intensively studied over the past decades

[53]–[55]. GaN has a wide bandgap that the electrons from the valence band requires larger energy to jump into the conduction band. Under same temperature, the higher electric field leads to higher transition energy. Thus, compared to Si counterparts, GaN power devices exhibit much higher breakdown voltage due to its wide bandgap. In addition, unlike AlGaAs/GaAs, two-dimensional electron gases (2DEG) can be formed at the interface between AlGaN and GaN in an AlGaN/GaN heterostructure without using modulation doping. This is due to intrinsic polarisation, leading the 2DEG in an AlGaN/GaN device to achieve both a high sheet carrier density and a high electron mobility simultaneously [56]. These also brings a remarkable potential to achieve much lower on-state resistance and thus lower conduction loss than Si and SiC counterparts [56], [57]. Table 2.4 summaries the two commonly used figures of merit (FoM) for power applications, comparing between Si, SiC and GaN taking account of their relevant material properties, where E_c is the critical electric field strength, ν_{sat} is the saturation velocity, ε is dielectric constant and μ is electron mobility (electron mobility in 2DEG for GaN).

Figure of Merit	Si	4H-SiC	GaN
BFoM ($\varepsilon\mu E_c^3$)	1	130	650
JFoM ($E_c\nu_{sat}/2\pi$)	1	180	760

Table 2.4: Comparison of figures of merit for power application between Si, SiC and GaN. BFoM and JFoM are used to evaluate the low-frequency performance and high-frequency performance of power devices, respectively.

Baliga's figure of merit (BFoM) has been widely used to evaluate the low-frequency performance of power devices, considering the trade-off between the breakdown voltage and the on-state resistance [58]. The BFoM of GaN is much higher than that of SiC, meaning a much higher upper limit that GaN power devices can achieve due to its intrinsically high breakdown voltage and low conduction loss compared with SiC.

Johnson's figure of merit (JFoM) describes the high-frequency power switching performance of a device [59]. GaN exhibits a much higher JFoM than SiC as a result of its high saturation velocity which benefits from the polarisation induced 2DEG in

an AlGaN/GaN heterostructure, where the high sheet density of electrons that are confined within a triangular potential formed at the interface between AlGaN/GaN are well protected from ionised impurity scattering.

Figure 2.18 shows a basic structure for an AlGaN/GaN high electron mobility transistor (HEMT) grown on a foreign substrate (c-plane sapphire or (111) Si), which consists of a buffer layer and then an AlGaN/GaN heterostructure. A thick GaN layer (>1.5 μm) is normally used as the buffer layer, and needs to be semi-insulating or insulating to prevent buffer 'punch through' under the off-state of a transistor [60]. For (111) silicon substrates, it may require one or more transitional layers such as AlGaN between the GaN buffer and substrate, which is used to accommodate the large lattice mismatch and the large thermal expansion coefficient difference between GaN and silicon [60]. The 2DEG formed at the interface between AlGaN and GaN serves as the channel of the device.

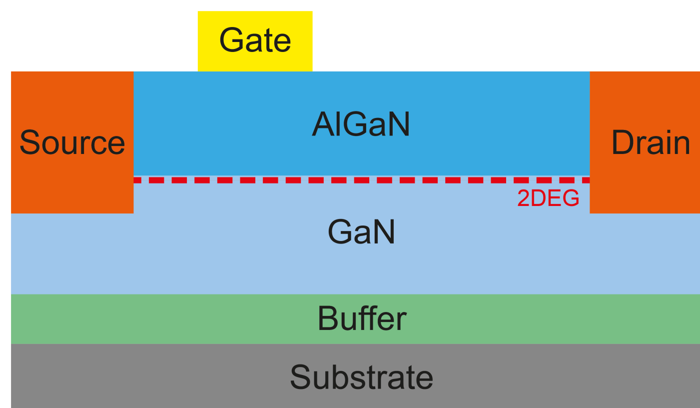

Figure 2.18: Basic device structure of an AlGaN/GaN HEMTs.

A HEMT requires three metal contacts as electrodes. Two ohmic contacts, which are used as a drain and a source, are formed to gain access to the 2DEG channel. Metal stacks of Ti/Al/Ni/Au are normally deposited and then annealed for the formation of TiN, leading to good ohmic contacts. A Schottky contact is used as a gate electrode and is typically formed by the metal stack of Ni/Au. Due to the presence of 2DEG formed as a result of intrinsic polarisation, such a HEMT device naturally exhibits a normally-on behaviour. Without any bias on the gate, current can flow along the 2DEG from drain to source, when a positive potential is applied between the drain and the

source. To pinch-off the channel, a negative bias is required at the gate in order to deplete the 2DEG underneath. The voltage which is applied to turn off the channel is defined as the threshold voltage (V_{th}) of the device. For normally on devices, the device is on-state without any bias on the gate. With the application of power device, the device may be failed for various reasons, such as gate signal failure, system failure, device quality, etc. In this case, the device keeps on-state which may leads to safety issues. Thus, it is also necessary to develop normally off devices.

The main performance indicators of HEMT are breakdown voltage, drain current and on-state resistance. The breakdown voltage (V_{br}) refers to the maximum off-state voltage that a transistor can withstand. It is one of the most important parameters for a power device, as it determines the voltage rating of a device. V_{br} can be defined when catastrophic breakdown occurs leading the device to be completely destroyed. The breakdown of AlGaN/GaN HEMTs can occur in two directions. A device may incur a lateral breakdown where leakage current is dominated through a gate electrode/a source electrode or a vertical breakdown where substrate/buffer leakage current dominates. To improve the lateral breakdown of a device, one can increase the gate-drain separation which results in an asymmetric geometry as shown in Figure 2.18. Alternatively, field plates can be implemented to modulate the electric field underneath gate-drain areas. In addition, it is critical to improve the resistivity of the buffer of a device, which can enhance both the lateral and vertical breakdown of a device.

The drain current (I_{DS}) is another important parameter which determines the current rating of a device, and is given by Equation 2.7:

$$I_{DS} = n_s \times q \times v_{eff} \tag{2.7}$$

where n_s is the sheet charge density, q is the electronic charge and v_{eff} is the effective velocity of electrons in the channel region. Initially, I_{DS} increase linearly with increasing bias (V_{DS}) applied between drain and source, and thus is determined by the sheet resistance and the potential between drain and source. With further

increasing V_{DS}, the gate-drain junction starts to pinch off and I_{DS} begins to saturate, where the transistor enters its saturation mode. To enhance I_{DS}, n_s can be increased by optimising a HEMT structure in order to maximise the polarisation effect. For AlGaN/GaN HEMTs, a remarkably high n_s, typically over 1E13 cm^{-3}, can be achieved in the 2DEG along with high v_{eff}, leading to a higher channel conductivity. I_{DS} is generally reported as normalised with respect to the gate width (W) of a transistor for comparisons between different devices.

The on-state resistance (Ron) determines the conduction loss of a device and thus is a critical factor that trades off the breakdown voltage, as suggested by the BFoM. For AlGaN/GaN HEMTs, Ron consists of both ohmic contact resistance and 2DEG channel sheet resistance. Therefore, it is necessary to optimise the fabrication of ohmic contacts in order to obtain the lowest contact resistance. However, for power devices, it is often the sheet resistance that dominates the total Ron. A reduction in gate-drain separation can significantly reduce Ron and thus conduction loss. However, a sacrifice is due to a reduction in voltage handling of a device. Ron can be extracted from the linear region of the I-V characteristics of a device and is often normalised to a device gate width for comparisons.

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Chapter 3

Equipment

This chapter introduces all the equipment which are used in order to carry out the project presented in this thesis. The project involves a wide range of research activities from epitaxial growth, template and device fabrication, material characterisation, and final device testing. In which the confocal PL measurement is carried out with the help of Mr. Peter Fletcher. The SEM-CL is performed by Dr. Jochen Bruckbauer in the University of Strathclyde. This chapter is divided into four sections: fabrication equipment, epitaxy equipment, characterisation equipment and photodetector (PD) measurement equipment.

3.1 Fabrication Equipment

3.1.1 Plasma Enhanced Chemical Vapour Deposition (PECVD)

PECVD is used to deposit thin films on a substrate. In this work, PECVD is used to deposit silicon dioxide (SiO_2) thin film on substrates. PECVD deposition exhibits uniformity and the quality of the deposited dielectric film is better than those by other deposition methods such as e-beam evaporator and sputter.

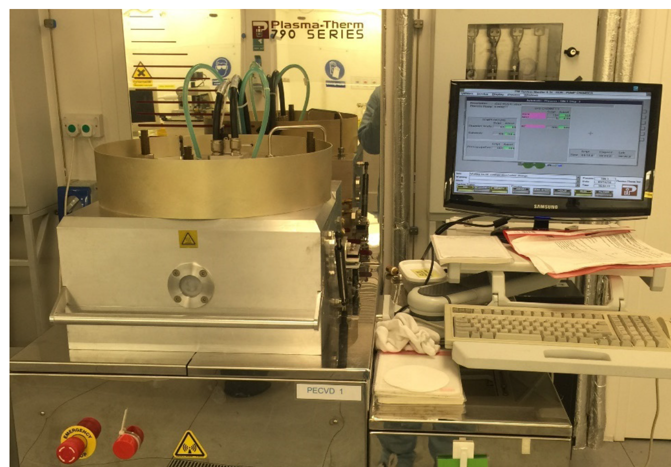


Figure 3.1: Plasma-Therm 790 series PECVD.

Figure 3.1 shows the photo image of the PECVD system used in this work, which is the Plasma-Therm 790 series, where the standard gases used for depositing SiO_2 are SiH_4, N_2O and N_2. The optimised deposition conditions: a typical deposition rate of SiO_2 under 25 W RF power at 300 ˚C. A typical SiO_2 film with a thickness of 120 nm is used as a mask for the work in the thesis.

3.1.2 Photolithography

A photolithography process is carried out in the yellow room of our device fabrication cleanroom. Spinner (Figure 3.2) is used for photoresist coating. In order to achieve a uniform coating of photoresist, our optimised conditions are a rotation speed of 4000 rev/min with a typical spinning time of 30 seconds. The photoresist used is BPRS-100. After spinning, a soft baking process is performed at 100 °C for one minute.

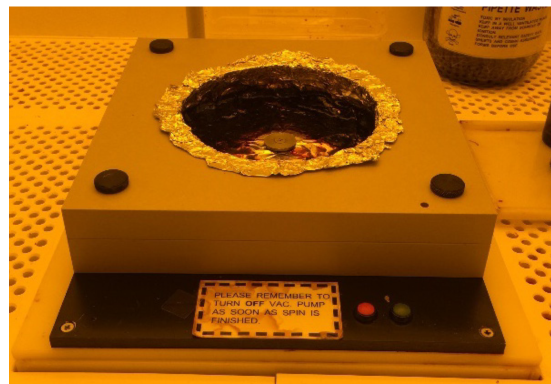


Figure 3.2: Spinner for photoresist deposition.

A mask aligner is used to transfer mask patterns from a mask to the photoresist deposited on a sample by exposing the sample to UV light. The mask aligner used in this work is Karl Suss MJB3 UV400 and UV300. The only difference between the two kinds of aligners is due to their UV lamp wavelength. The UV400 system is equipped with a UV light system with a wavelength of 350-450 nm, while the UV300 system has a 250-350nm UV light system. Figure 3.3 shows the image of our UV400 mask aligner system.

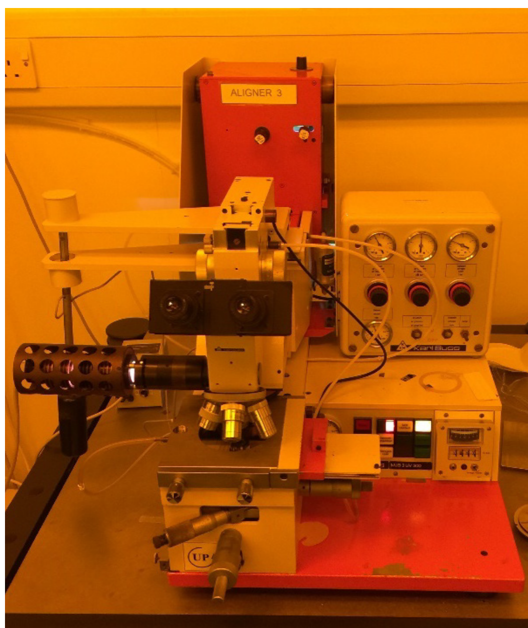


Figure 3.3: Karl Suss MJB3 UV400 mask aligner.

3.1.3 Reactive-Ion Etching (RIE)

RIE provides dry etching by using reactive plasma and specific gases. Figure 3.4 shows the photo image of the RIE system used for the project, a Plasma-Therm Shuttlelock Series RIE system. This system is mainly used to etch dielectrics such as SiN_x or SiO_2, where the typical mask for our RIE etching is photoresist.

Figure 3.4: Plasma-Therm Shuttlelock Series RIE.

Our optimised condition for RIE etching of SiO_2 or the project is that etching processes are carried out at a chamber pressure of 35 mTorr with an RF power of up to 150W at 13.56 MHz using CHF_3 with a flow rate of 35 sccm as an etchant gas.

3.1.4 E-Beam Deposition System

In order to perform selective growth as discussed in Section 2.3.3 a desired SiO_2 mask as shown in Section 2.3.3 is required, and such a mask pattern can be achieved by using e-beam deposition. The mechanism of e-beam deposition is to heat a source placed in a crucible by bombarding e-beam on the source. Figure 3.5 illustrates the mechanism of the e-beam deposition technique.

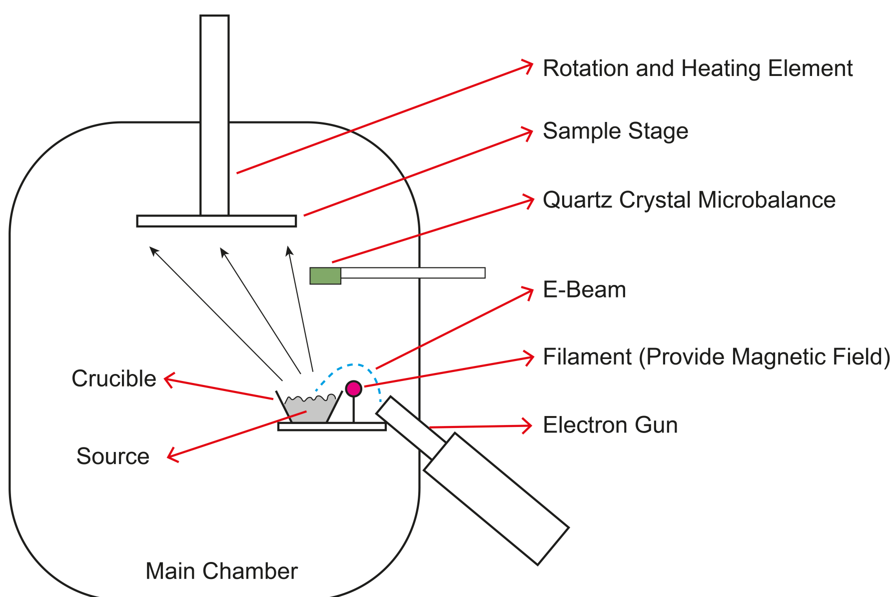


Figure 3.5: Schematics of e-beam deposition.

The e-beam deposition system used in this work is Mantis E-Beam System (Figure 3.6). To produce uniform deposition a sample needs to be rotated. However, in this work, the rotation cannot be used, as a selective deposition is required and thus a deposition with an e-beam along a specific direction allows for such a deposition. Our deposition is carried out at room temperature. The pressure of the deposition chamber is controlled by a turbopump system with a rotary pump as a pre-pump, which allows us to achieve a vacuum of $< 2E-7$ Torr (where the Turbopump works at 1000 Hz with a load of 24%). Our optimised conditions: a typical deposition rate of 0.5

nm/s at an electron gun current of 7 mA under bias of 7.5 kV.

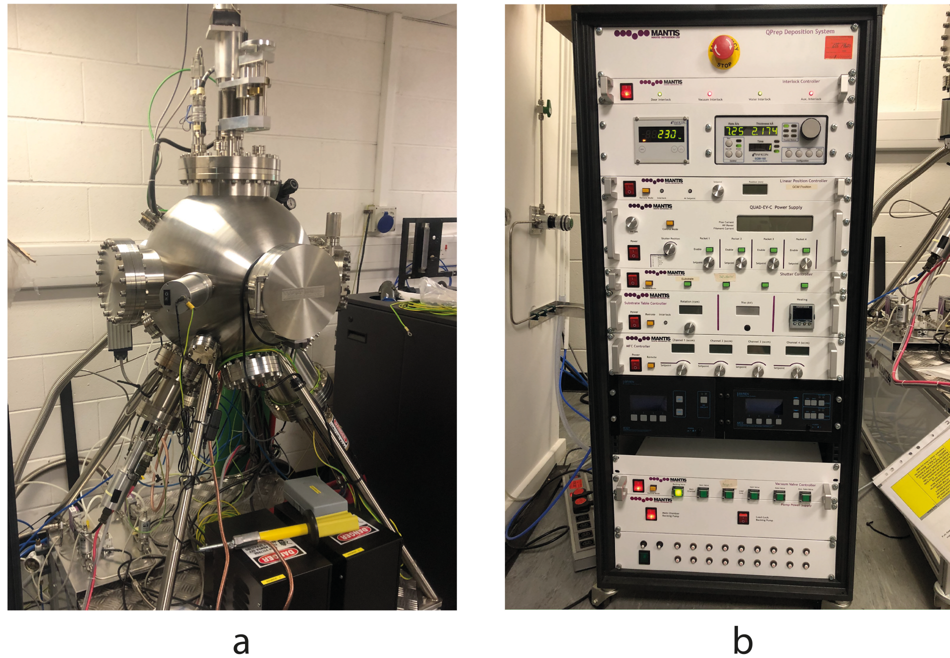


Figure 3.6: Mantis e-beam system (a): main chamber; (b): control panel.

3.2 Epitaxy Facilities

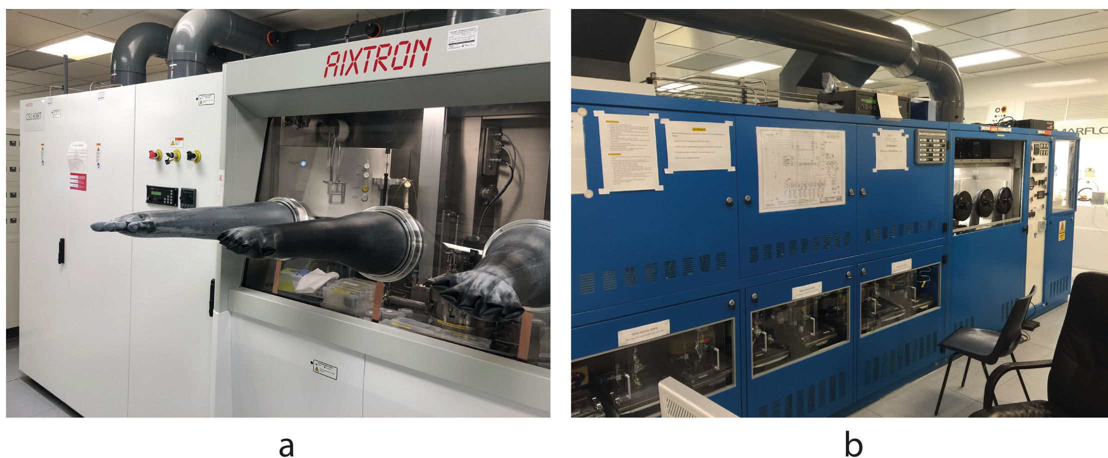


Figure 3.7: MOCVD (a): Aixtron 3×2" flip-top CCS reactor; (b): Thomas-Swan 3×2" vertical CCS reactor.

Metal-organic chemical vapour deposition (MOCVD) is used for the growth of III-nitride semiconductors for the project. Generally speaking, there are a number of different types of MOCVD system in terms of reactor configuration: a planetary rotation horizontal reactor, high-speed rotation vertical reactor [1] and close-coupled showerhead reactor (CCS). Two MOCVD systems have been used in this work, both

of which are the CCS systems. An Aixtron 3×2" flip-top CCS system is used for the growth of initial templates and then overgrowth on patterned templates. A Thomas-Swan 3×2" vertical CCS system is used for any device structures, such as InGaN/GaN MQWs and HEMTs. Figure 3.7a shows the Aixtron CCS system, while Figure 3.7b shows the Thomas-Swan CCS system.

3.2.1 MOCVD Growth Principle

MOCVD is a chemical deposition system with an accurately controlled gas flow which allows us to achieve any compound semiconductor deposition controlled on an atomic level. Metal organic sources as precursor are introduced into a reactor chamber, then undergo chemical reaction at a high temperature, and finally form compound semiconductor films on a proper substrate. All the flow rates of these precursors are controlled accurately by using pressure gauges and mass-flow controllers. The chamber pressure is controlled by a powerful pump with an accurate pressure controller. Figure 3.8 presents a standard process for MOCVD deposition. The substrate is placed on a susceptor and rotated with the susceptor during the whole growth process to ensure the uniformity.

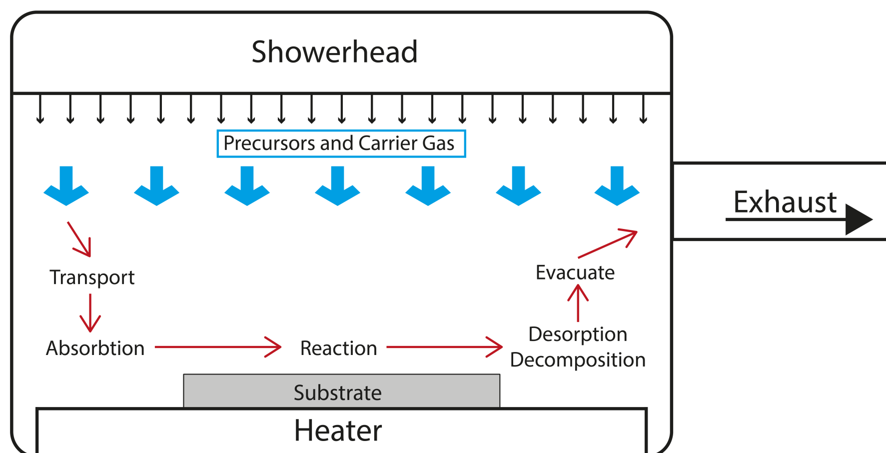
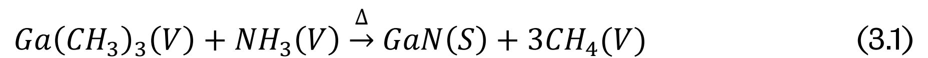


Figure 3.8: Schematics of the MOCVD deposition process.

For III-nitrides epitaxial growth, high purity ammonia gas (NH_3) is used to obtain nitrides as group V precursor; three different types of metal-organic sources are used as group III precursors, namely trimethylgallium (TMGa), trimethylaluminum (TMAl) and trimethylindium (TMIn). Two dopants are used for the doping of III-

nitrides: disilane (Si_2H_6) for n-type doping and bis(cyclopentadienyl)magnesium (Cp_2Mg) for p-type doping. Nitrogen (N_2) and hydrogen (H_2) are used as carrier gases. High purity hydrogen as a typical carrier gas can be achieved by using a high hydrogen purifier. For InGaN growth, hydrogen prevents the decomposition of ammonia and increases the ammonia coverage of the sample surface. With the increasing of the ammonia coverage, the indium adatoms becomes unstable and the incorporation efficiency reduced [2]. Thus, nitrogen is introduced as a carrier gas during InGaN growth. The main reaction of GaN growth is illustrated by the formula below [3]:



$$Ga(CH_3)_3(V) + NH_3(V) \xrightarrow{\Delta} GaN(S) + 3CH_4(V) \tag{3.1}$$

This reaction is between TMGa and ammonia under heating. In the formula, (V) indicates vapour state and (S) for solid state. The reaction is similar to AlN growth. All the sources including carrier gases that inject into the reactor must have high purity. The impurity of the gases leads to various issues such as low crystal quality, a high defect density and even chamber contamination.

3.2.2 MOCVD system

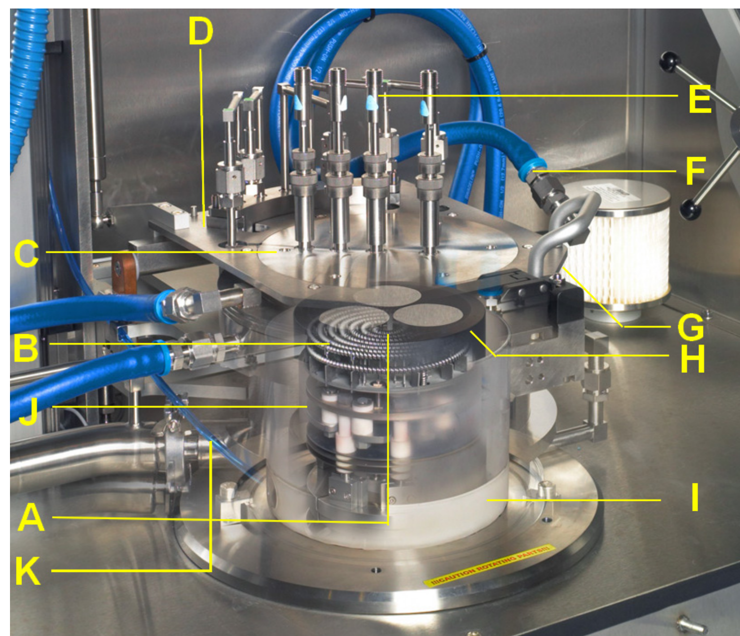


Figure 3.9: Image of elements in the reactor of MOCVD. A: thermocouple; B: tungsten heater; C: showerhead; D: reactor lid; E: optical probe; F: showerhead water cooling; G: double O-ring seal; H: susceptor; I: quartz liner; J: susceptor support; K: exhaust. (Taken from [4]).

The core component of a MOCVD system is so-called reactor chamber where the main process of crystal growth happens. A reactor chamber mainly consists of a showerhead system, a heater system, susceptor system and monitoring systems. Figure 3.9 is the photo image of a typical MOCVD reactor chamber. Wafers or substrates are placed in the pockets of a susceptor on above a heater but below a showerhead system. In order to achieve an ultra-high temperature, a double coil system with three zones is used for a heater element as shown in Figure 3.10, where each zone is controlled separately by an individual power supply unit.

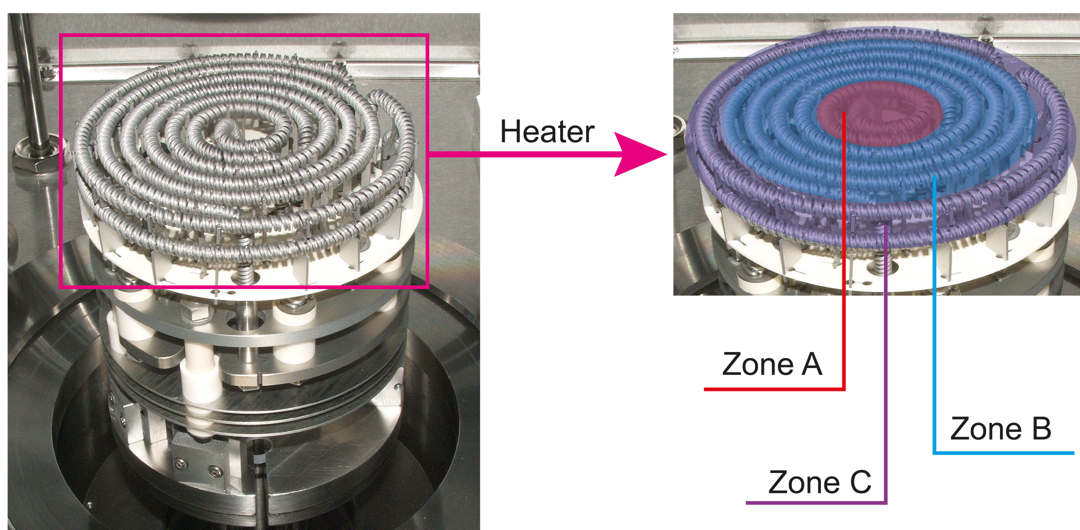


Figure 3.10: Image of the heater. (Modified from [4]).

All the gases and metal organic precursor are introduced into the reactor chamber through a stainless-steel showerhead as shown in Figure 3.11. The showerhead is designed to allow group V precursors and group III precursors to be injected into the reactor chamber separately in order to eliminate any pre-reaction, which is particularly important for the growth of AlN or AlGaN. Such a showerhead design also ensures an excellent uniformity. Furthermore, Figure 3.11 also shows four large holes, which are tubes for flowing hydrogen or nitrogen gas for an attached in-situ monitoring system. The three optical probes labelled as blue are for an Argus temperature monitoring system, while another one labelled as violet is for an in-situ laser monitoring system. The reactor chamber is fully sealed by a double O-ring system in order to eliminate any gas leakage when the chamber is closed.

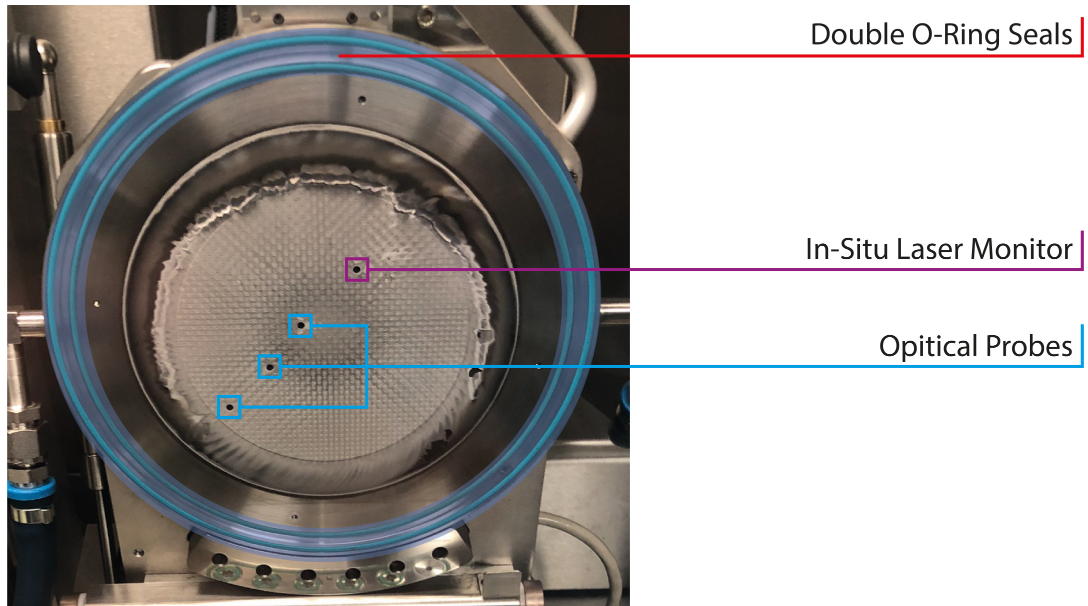


Figure 3.11: Image of the showerhead.

A susceptor is made from graphite coated with a thick SiC layer, which ensures an excellent temperature uniformity and an excellent resistance to any potential corrosion generated during high temperature epitaxial growth. Figure 3.12 shows the image of a susceptor where three 2” sapphire substrates are loaded into three pockets of the susceptor.

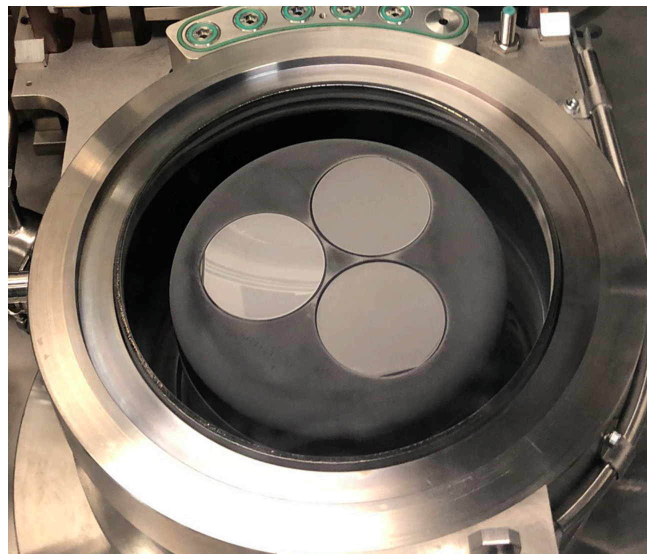


Figure 3.12: Image of the susceptor.

3.2.3 Gas System

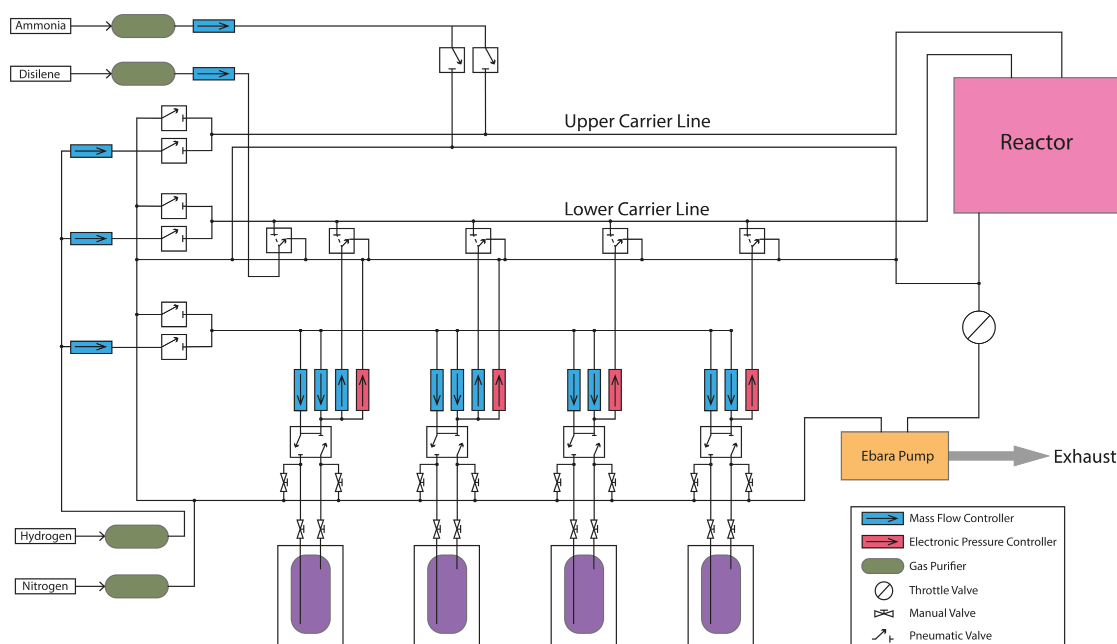


Figure 3.13: Schematics of the gas delivery system of MOCVD.

Gas delivery is controlled by various valves such as pneumatic valves, manual valves, and throttle valves. All the main gas lines of a MOCVD system are schematically illustrated in Figure 3.13, where hydride gas (ammonia) lines are fully separated from MO gas lines. This design is to prevent any potential pre-reactions between ammonia and MO sources. Along with the specially designed showerhead as explained above, the mixture of group V and III precursors and then their chemical reaction take place only above a susceptor in a reactor. All the gases that enter the MOCVD must be of high purity, and thus nitrogen/hydrogen needs to purify before entering into a reactor chamber. Therefore, both a nitrogen purifier and a hydrogen purifier are attached to a MOCVD system.

Palladium Membrane Purifier

Figure 3.14a shows the photo image of our hydrogen purifier, where the key component is a Pd membrane diffusion cell that typically operates at 300 ˚C - 400 ˚C. This acts as a kind of mesh filter, where the mesh dimension is small enough to only allow hydrogen molecule to pass through. Figure 3.14b shows a schematic illustration

of a Pd membrane diffusion cell.

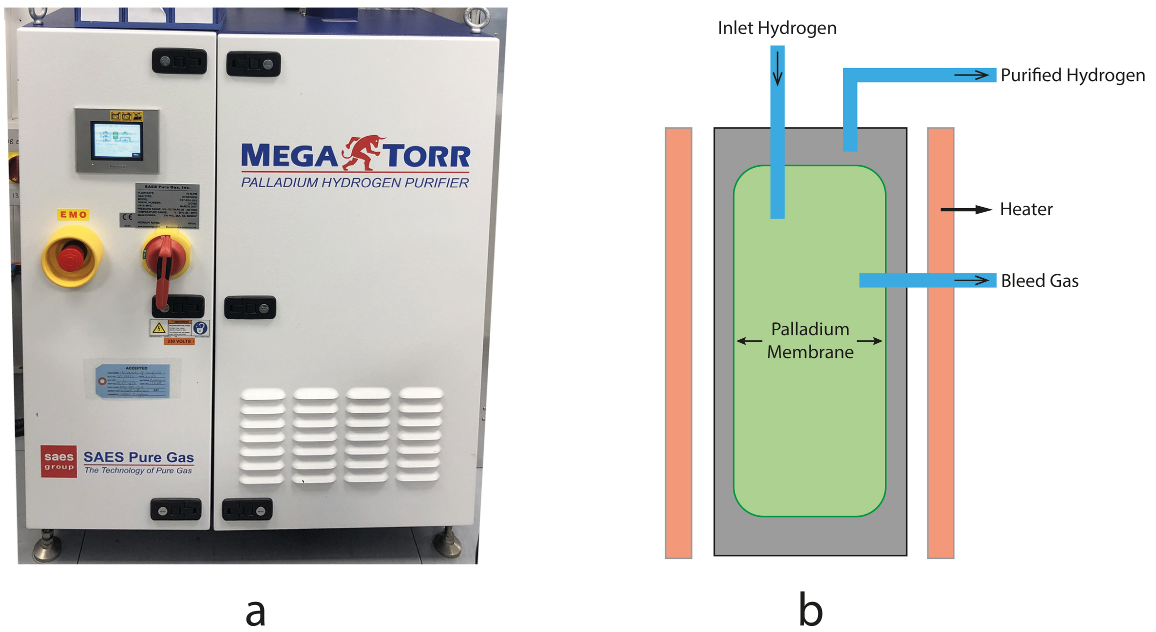


Figure 3.14: The (a): the image of hydrogen purifier, (b): schematics of hydrogen purifier cell.

Nano-Chem Purifier

Unlike a hydrogen purifier, this kind of purifier is widely used to purify nitrogen or ammonia. It removes a tiny amount of water (H_2O), oxygen (O_2) or carbon dioxide (CO_2) residual in nitrogen or ammonia through chemical reactions [5], [6]. The purification rate of this kind of purifier is lower than the palladium membrane purifier. Thus, hydrogen has a higher purity compared to nitrogen. Hence, normally, hydrogen acts as the carrier gas in most of the epitaxy. The ammonia utilised in this work has a purity of 99.99999% without applying the purification which is called white ammonia [7]. Another type of ammonia is called blue ammonia which has a purity of 99.99994%.

3.2.4 Metal-Organic Source Input System

A MO source input system controls the inlet of the MO source into the reactor chamber. A MO source input system consists of source storage unit, gas system and controller units including mass flow controllers and pressure gauge. The temperature of a MO source is controlled by being installed in a water bath. Figure 3.15 illustrates a typical MO source input system. There are two kinds of

configurations, as labelled by a blue dashed rectangular (Type A) and a red dashed rectangular (Type B).

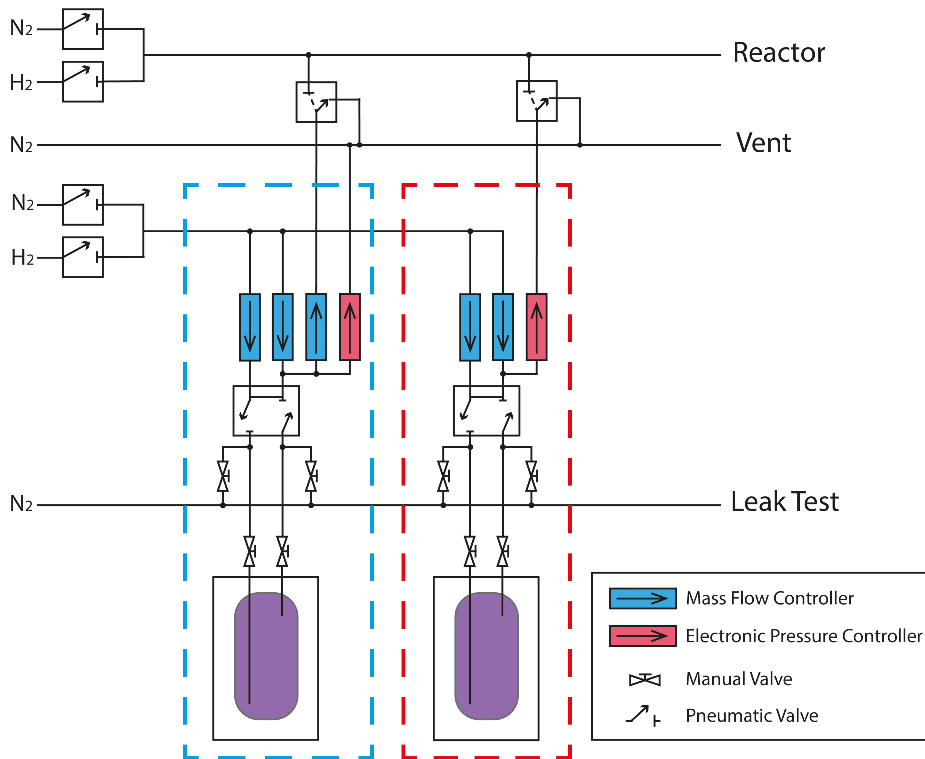


Figure 3.15: Schematics of a MO source input system of MOCVD.

MO sources are typically stored in a stainless-steel container called bubbler. An MO bubbler is installed in a water bath equipped with a refrigerator unit and a heater unit in order to maintain a constant temperature. Hydrogen or nitrogen as a carrier gas is injected into a MO bubbler in order to push the MO source out of the bubbler into the reactor chamber via pipe systems.

Type A is similar to type B but with an extra outlet mass flow controller (MFC). The two inlet MFCs (with arrow down) control source flowrate and pusher flowrate. Pusher line is applied for balancing the upper and lower main carrier lines during the epitaxy process. A pressure gauge controls the pressure in the bubbler.

If a MO source with a very low flowrate is required, an extra dilution line with an MFC has to be used in order to inject extra carrier gas into an output line. Hence the MO output is diluted in order to obtain a low flowrate. In the case, the actual MO source flowrate is calculated through Equation 3.2 below:

$$f(MO) = f_i \times \frac{f_s}{f_s + f_d} \quad (3.2)$$

where $f(MO)$ is the real MO source flowrate. f_i represents the flowrate of injecting line. f_s is the flowrate of the source line. f_d indicates the flowrate of the dilute line.An actual mole flow rate of a MO source depends on the pressure of a bubbler and the temperature of the bubbler. As mentioned above, the bubbler stays in a water bath with a constant temperature and the pressure of the bubbler is controlled by an electronic pressure gauge. Therefore, an actual mole flowrate MO is expressed by Equation 3.3:

$$n(MO) = \frac{f_c \times P_p}{V_m \times P_b} \quad (3.3)$$

where $n(MO)$ is the MO mass flux in a unit of mol/min; f_c is the flowrate of the carrier gas which is injected into the MO bubbler; P_p is the vapour partial pressure of the MO source, V_m is a constant with a value of 22414 cm^3/mol and P_b is the pressure of the bubbler. Vapour partial pressure of trimethyl source (TMGa, TMAl and TMIn) is calculated by:

$$Log(P_p) = B - \frac{A}{T} \quad (3.4)$$

Where A and B are constants, T is the temperature of bubbler in degrees Kelvin. The expression for the vapour partial pressure for a bis cyclopentadienyl source (Cp_2Mg) is given below:

$$Log(P_p) = B - \frac{A}{T} - 2.18 lnT \quad (3.5)$$

Source	Chemical Formula	A	B	Bubbler Temperature (K)	Melting Point (˚C)
TMGa	$Ga(CH_3)_3$	1703	8.07	273	-15.8
TMAl	$Al(CH_3)_3$	2134	8.22	291	15.4
TMIn	$In(CH_3)_3$	3204	11.00	303	88.4
Cp_2Mg	$Mg(C_2H_5)_2$	4198	25.14	303	176

Table 3.1: Parameters of MO bubblers.

Table 3.1 gives the main parameters of MO bubblers used in this work [8]–[11].

3.3 Characterisation Equipment

Both optical and electron microscopes are used to characterise the surface morphologies of samples. Besides, XRD and optical measurements are performed for the characterisation of the crystal lattice properties and optical performances. This section presents the two mainly used microscopes, XRD system, and three optical measurement systems.

3.3.1 Nomarski Interference Contrast Microscope

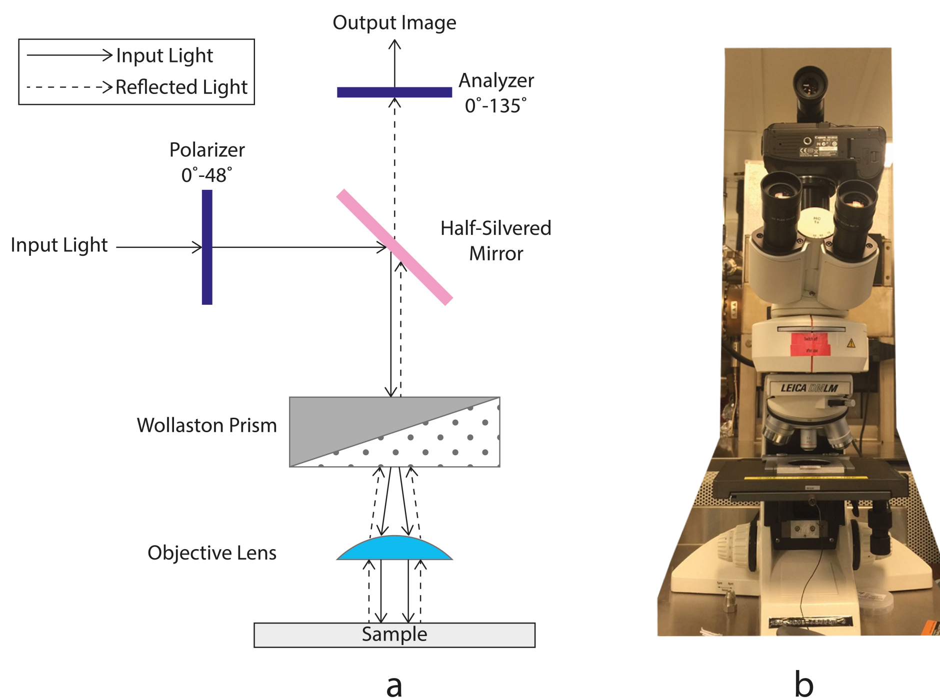


Figure 3.16: The (a): schematics of the light route, (b): an image of the Nomarski microscope.

Figure 3.16 shows the schematics of the configuration including all the main optical components of a Nomarski microscope system. This kind of optical microscope system enhances the contrast of an image especially for transparent materials by using optical interferometry effects. An input light splits into two identical parts through a Wollaston prism. The two beams are then projected on a sample surface. Finally, the two teams are reflected back to the prism. As a result of surface morphology and crystal properties, the optical paths of the two reflected beams are

different, generating interference due to the different phases of the two reflected beams. Therefore, an image finally formed as a result of interference effects significantly enhance the contrast of the image.

3.3.2 Scanning Electron Microscope (SEM)

Scanning electron microscope (SEM) is a very useful tool for characterising the surface morphology and cross-section of a sample. In an SEM system, an electron gun emits electrons, and are accelerated by a high voltage level up to 30kV. Then the electrons are collimated by a condenser lens and then pass through an aperture system. Finally, an electron beam is focused on a sample surface by deflection coils, generating back-scattered electrons and secondary electrons. These two kinds of electrons from the sample surface are collected and then detected by two detectors, forming images after being processed by computer. The schematics of a typical SEM system is presented in Figure 3.17a. Compared to an optical microscope system, a SEM system offers much higher resolution and magnification.

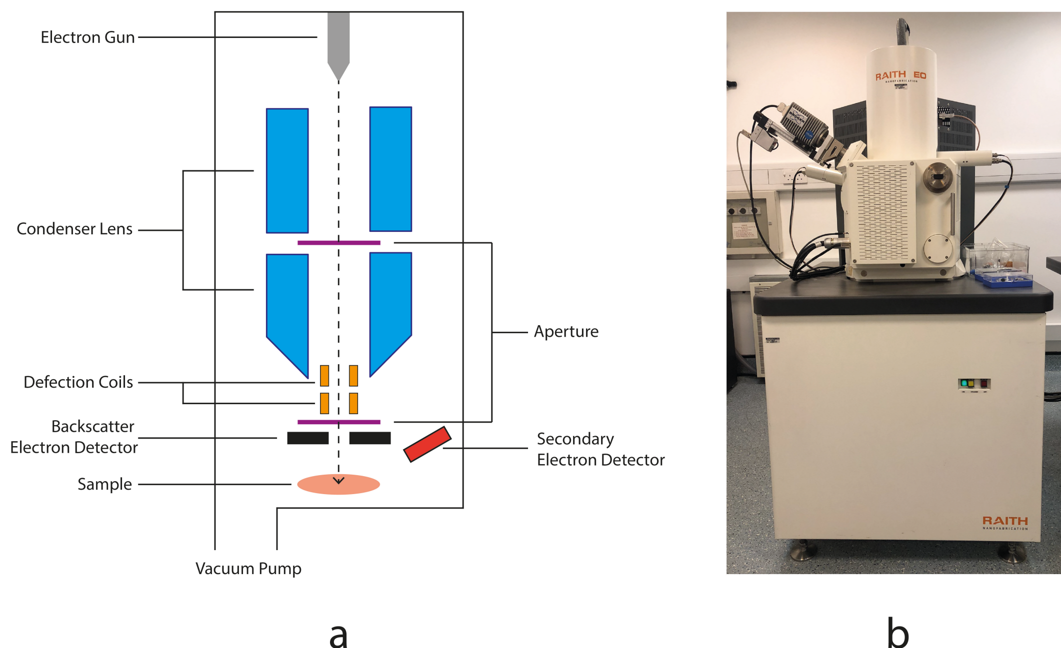


Figure 3.17: The (a): schematics, (b): an image of Raith SEM.

The main issue of the SEM measurement of insulator such as undoped GaN is surface charging. The silicon substrate of the GaN growth on silicon in this thesis is based on

n-type P doped silicon. Thus, the charging is significantly reduced. The SEM system used in this work is Raith EO Nanofabrication system with a resolution of down to 2 nm. This system is reconfigured from a Raith 150 electron-beam lithography (EBL) system. A photograph of this SEM system is shown in Figure 3.17b. The SEM operation needs to be performed under a high vacuum, normally 5×10^{-5} mBar in order to eliminate scattering. A sample has to be conductive in order to prevent electron charge on the sample surface leading to a degradation in image.

3.3.3 X-Ray Diffraction

An x-ray diffraction (XRD) system is one of the most powerful tools for non-destructively characterising the crystal properties of an epitaxy wafer. Basically, XRD measures a crystal lattice according to Bragg's law:

$$2d\sin\theta = n\lambda \tag{3.6}$$

Where d is the interplanar distance, θ is the incident angle, n is diffraction order and λ is the X-ray wavelength [12].

Figure 3.18 illustrates the schematics of the XRD measurement principle. X-ray is incident into a crystal along a particular angle which is determined by the crystal. As a crystal exhibits a periodic structure, it can be considered as a grating. Also, due to the short wavelength of X-ray (~1 Å), the X-rays are scattered by the crystal lattice planes finally forming constructive interference related to certain incident angles that obeys Bragg's law.

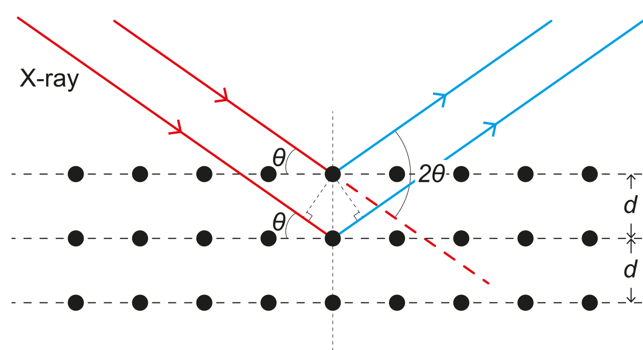


Figure 3.18: Schematics of Bragg's law applied in X-ray diffraction.

Figure 3.19a is the photograph of a Bruker D8 Discover HR-XRD system which is used for the research in this thesis. This is a high-resolution XRD system, consisting of X-ray tube, primary optics unit, sample stage, secondary optics unit and detector. By generating X-ray with a wavelength 1.5418 Å using a copper (Cu) anode, the X-ray is then introduced into a primary optics unit, where the X-ray is collimated by a Göbel mirror with a reduced beam divergence by a divergence filter, and then filtered with a monochromator and finally limited through a Soller slit. After the process of the primary optics, the X-ray is incident onto a sample. A secondary optics unit with the same function as the primary one receives the reflected X-ray from the sample and is then collected by a detector and converted into digital signals which are processed by a computer. The resolution of the XRD machine can be adjusted through tuning the slit width: one attached to the primary optics unit, and another installed in front of the detector controlled by the computer. The angular resolution of this XRD is down to 0.1°.

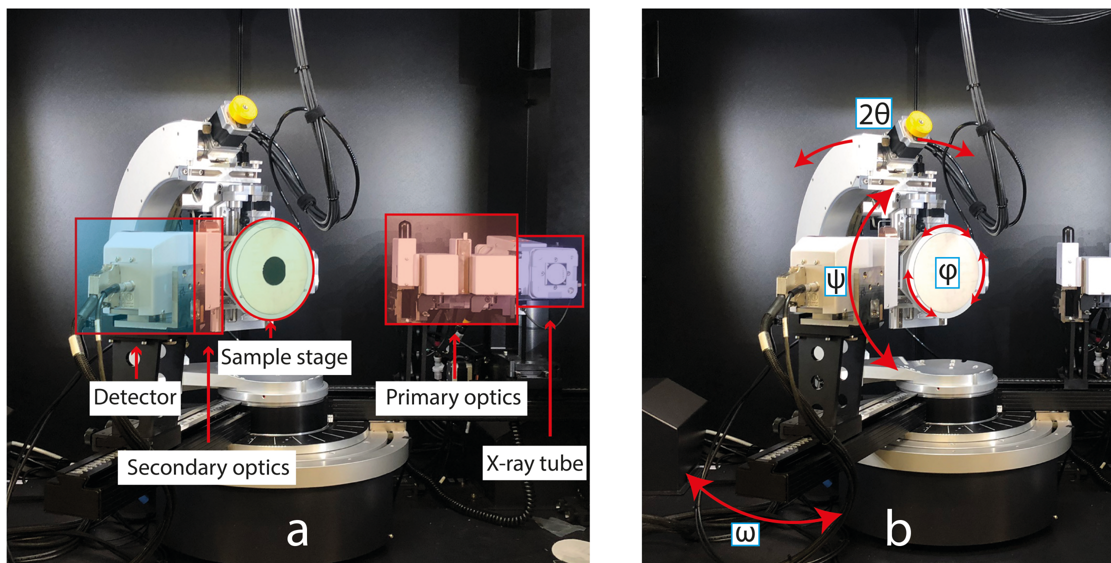


Figure 3.19: Bruker D8 XRD image with illustration of (a): components, (b): parameters.

Figure 3.19b illustrates the major components of the system. The sample stage can be moved along the traditional three-dimensional directions labelled as (x, y, z). Furthermore, the sample stage can be moved with two extra function, labelled as ψ and φ, respectively. The parameter ψ indicates an angle against the sea level of the sample stage and φ is the rotation angle of the sample stage. The incident angle of

the X-ray is ω. 2theta (2θ) represents the angle of the movement of the sample stage in the same direction as ω. Rocking curve and omega-2theta are the two main working modes for the measurement of this work. Rocking curve mode measures the intensity of the X-ray diffraction as a function of incident angle (ω). The measurement normally plots a single peak when measuring one material with a single orientation. The full width at half maximum (FWHM) of the peak indicates the crystal quality. Omega-2theta (ω-2θ) mode is a wide range scan with various incident angles. A multiple or single diffraction peaks can be measured, where the diffraction angles correspond to different materials or alloys with different composition [13]. The incident angle (ω) of certain material can be calculated by the computer through Bragg's law. Different materials with different orientations have different incident angles (ω), for example, is 14.2210°, the ω of (110) silicon is 11.5710° and the ω of (11$\bar{2}$0) GaN is 28.8870°.

3.3.4 Photoluminescence Spectroscopy

A photoluminescence (PL) spectroscopy system is the most common and widely used tool for evaluating optical properties. In Section 2.1.3, the principle of photoluminescence has been introduced. The bandgap of GaN is equivalent to an emitting wavelength of 363 nm. Therefore, a He-Cd laser with 325 nm wavelength is used for GaN PL measurements, while a 375 nm diode laser is normally used for InGaN/GaN MQW PL measurement, where only InGaN quantum wells can be excited.

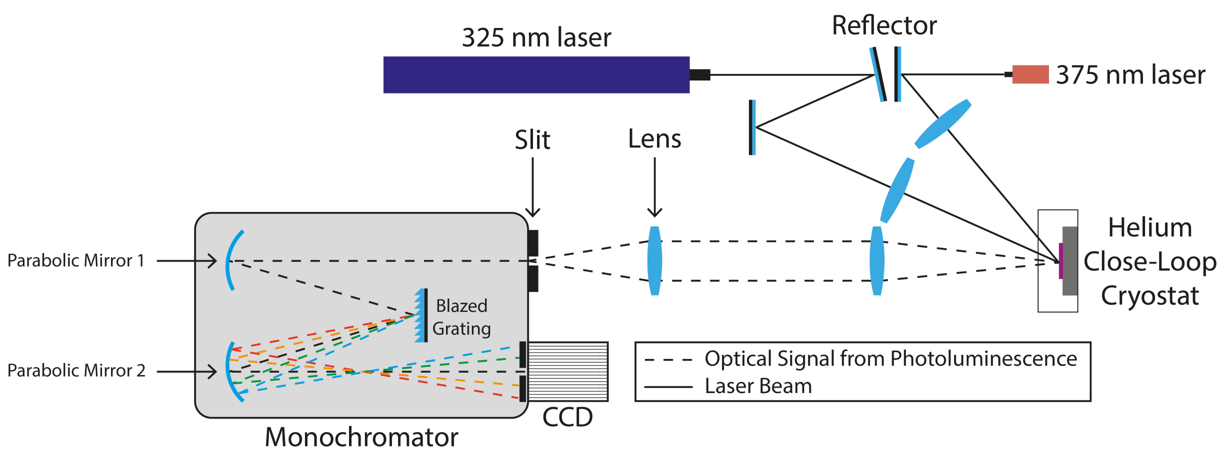


Figure 3.20: Schematics of the PL system.

Figure 3.20 illustrates the PL system used in this work, which is equipped with two lasers (a Kimmon 325 nm He-Cd laser and a Vortran Stradus 375 nm diode laser). A sample is placed on a sample stage inside a helium close-loop cryostat which allows the temperature of the sample to be varied from room temperature (300K) to 10K. Emission is then collected through by two lenses for collimation, and is dispersed by a monochromator (Horiba SPEX 500M spectrometer). Finally, emission is detected by a charge-coupled device (CCD). The slit before in front of the monochromator works as an aperture, it limits the light power to ensure it is under the maximum power that can be detected by the CCD. The CCD in this system is Horiba Syncerity thermoelectrically cooled CCD detector. This system can be used for standard PL measurements, low-temperature PL (LT-PL) measurements, temperature-dependent PL (TD-PL) measurements and excitation power-dependent PL measurements.

3.3.5 Confocal Microscope

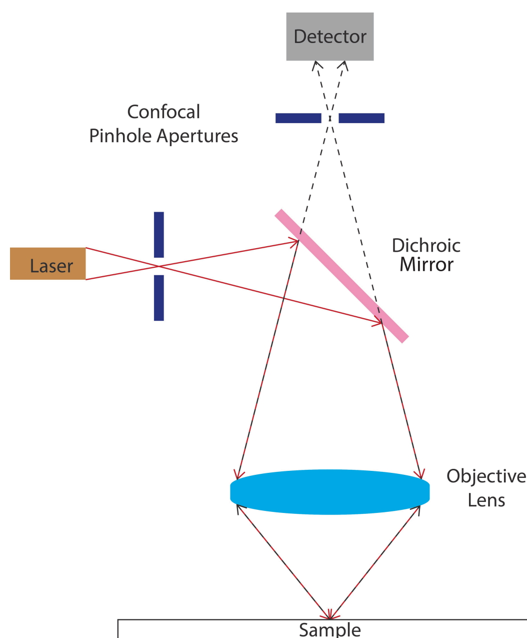


Figure 3.21: Schematics of a confocal microscope.

Figure 3.21 illustrates the schematic of a confocal microscope PL system. The major feature is due to two confocal pinhole apertures, limiting light or emission diffraction light for both illumination and detection. After a laser beam passes through the first

pinhole aperture a dichroic mirror is used to guide the laser beam to an objective lens with high magnification and high numerical aperture (NA), where the laser beam can be then focused into a tiny beam with a 100 nm scale on a sample. Emission is collected by the same objective lens and then passes through the dichroic mirror and finally the second pinhole aperture at the detector side. With the pinhole, any out-of-focus plane emission or scattering light can be removed at this stage. Finally, the emission is detected by a CCD detector. The confocal PL mapping can also be performed, as the sample stage is mounted on a piezo nano-positioner.

3.3.6 Scanning Electron Microscope - Cathodoluminescence (SEM-CL)

The principle of CL is similar to PL, but it uses an electron beam instead of a laser as an excitation source. However, the energy of primary electrons is far much larger than photons from any laser-based PL systems. As a result, the secondary electrons, Auger electrons and X-rays are scattered from the inelastic scattering of the primary electrons in the crystal. The scattered electrons and X-rays can also scatter. The cascade of scattering process may lead to 1000 secondary electrons from single incident electron [14]. The secondary electrons excite the sample and the electron from the valence band can jump into the conduction band if the kinetic energy is about three times of the bandgap [15]. Then the recombination of electrons and holes leads to the emission of photons. The main advantage of CL is the photoluminescence from a CL system is no longer limited by the energy of incident light. The CL system used to support this thesis is attached to a FEI Quanta 250 SEM system. The signal is detected by an Andor Newton electron multiplying charge-coupled device. Electron beam energies of up to 10 kV is used to measure the luminescence from up to 300 nm depth below the sample surface [16]. The special resolution of this system is approaching to 10 nm each pixel [17].

3.4 Photodetector (PD) Measurement Equipment

There are two main figure of merits (FoMs) for PD measurement, namely,

photoresponsivity and response time. Photoresponsivity is the gain, the ratio of the output to the input signal of the PD. Response time reflects the dynamic performance of PD. These two properties are measured through our custom built measurement system.

Photoresponsivity

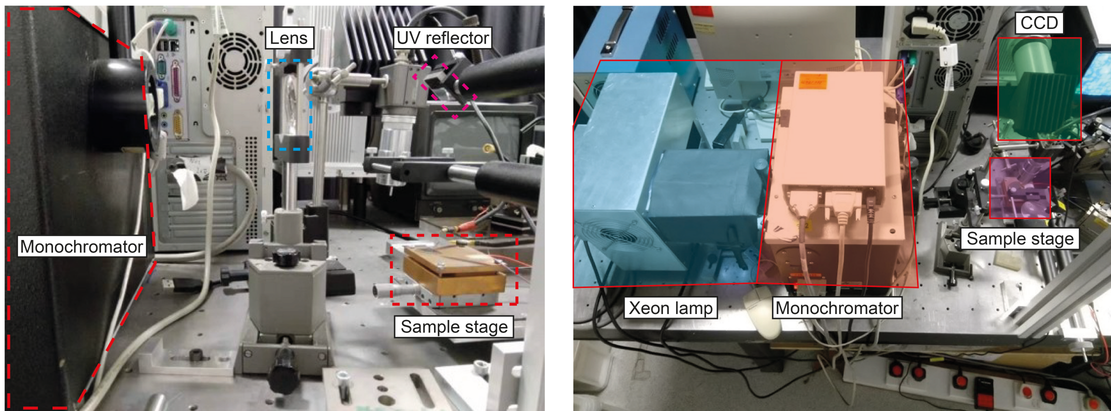


Figure 3.22: Images of custom build PD responsivity measurement system.

The basic idea of responsivity measurement is to measure the photocurrent generated by PD under varies voltage bias. The measurement system is shown in Figure 3.22. The light source is a Hamamatsu Xeon lamp with a power spectrum calibrated by a commercial PD having a known spectrum as provided by its datasheet.

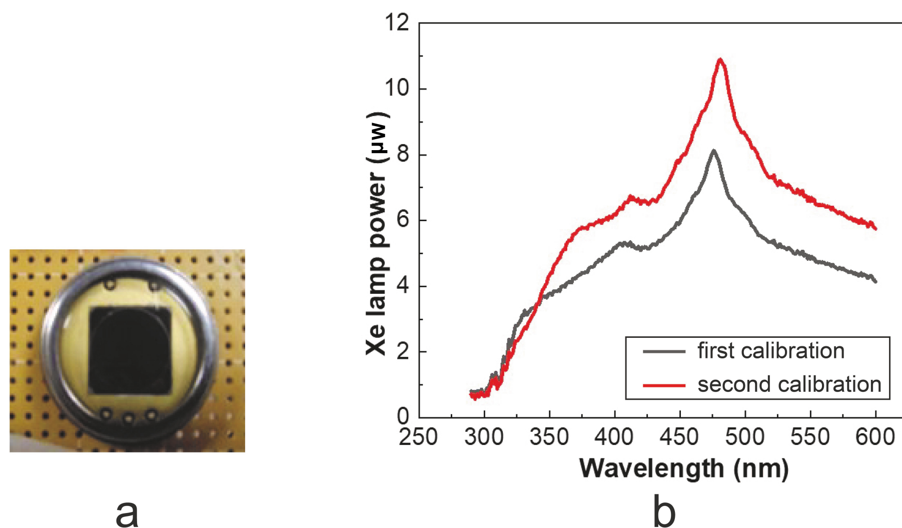


Figure 3.23: (a): Commercial PD for Xe lamp calibration, (b): Xe lamp calibration spectrum.

The commercial PD is shown in Figure 3.23a and the Xe lamp spectrum is calibrated

as Figure 3.23b. After passing through the monochromator and the reflecting by UV reflector, the power of incident light on the device surface is only in μW range. After passing through a SPEX 1681 monochromator a monochromatic light source with a selectable wavelength over 290-600 nm is available for GaN absorption. The output UV light is then focused by a lens and reflected onto the PD surface placed on the sample stage. The sample stage can be adjusted via axis x and y. A CCD is connected to a monitor for sample inspection purpose. The photocurrent generated by the PD is measured and recorded by a Keithley 2400 source meter.

Response Time

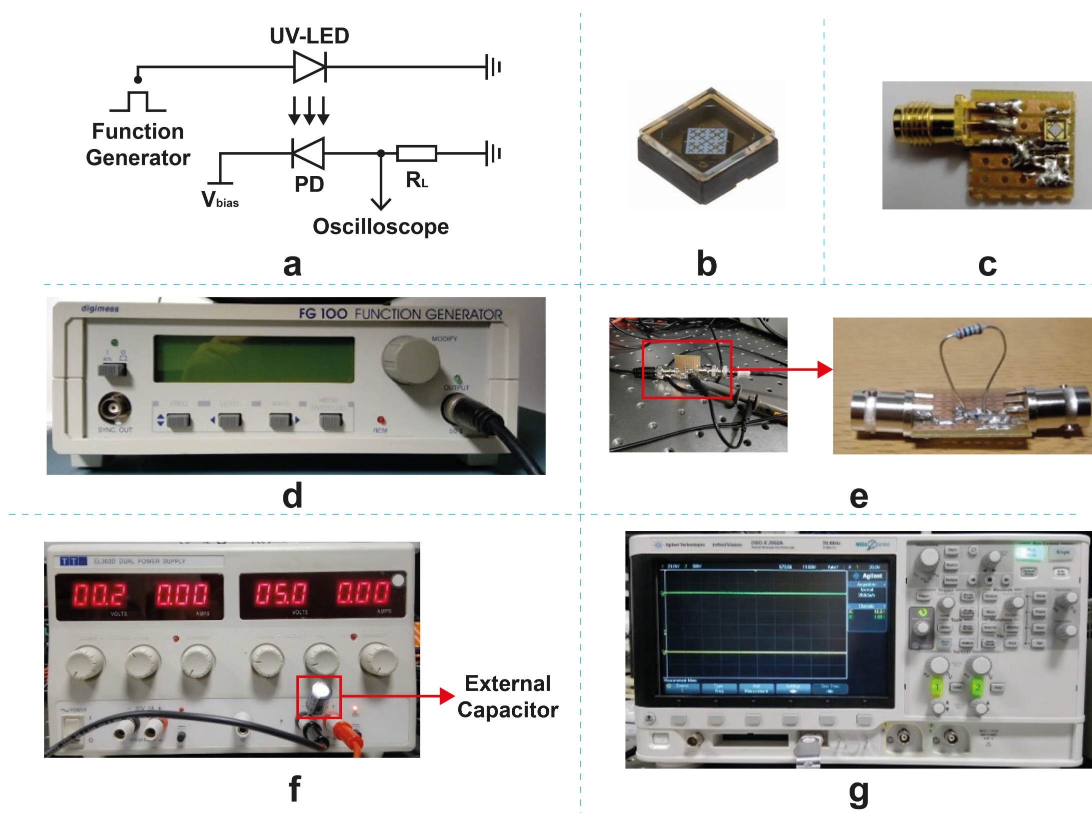


Figure 3.24: Schematics and images of PD response time custom build measurement system. (a): measurement circuit; (b): UV-LED as source light; (c): mounted UV-LED; (d): Digimess FG100 function generator; (e): External load resistor; (f): TTi EL302D dual power supply with an external capacitor; (g): Agilent X2002A oscilloscope.

Response time indicates the speed of the PD in collecting photo-generated carriers. For the measurement of response time, an external resistance is connected in the circuit for measuring the photovoltage waveforms, shown in Figure 3.24a. The light source is a Nichia NVSU233A-U365 UV-LED (Figure 3.24b) mounted on a small printed

circuit board (PCB) with an SMA connector for enabling wave modulation (Figure 3.24c). The modulation is achieved by Digimess FG100 function generator (Figure 3.24d); this generator has an amplitude of 3.2 V and an offset of 2 V at 1 kHz frequency. The PD is connected to an external load resistor (Figure 3.24e). The voltage bias (V_{bias}) is provided by TTi EL302D dual power supply with an external capacitor for noise reduction (Figure 3.24f). The final waveform on the loaded resistor is measured and displayed by Agilent X2002A oscilloscope which has a bandwidth of 79 MHz and a sampling rate of 2 GSa/s (Figure 3.24g).

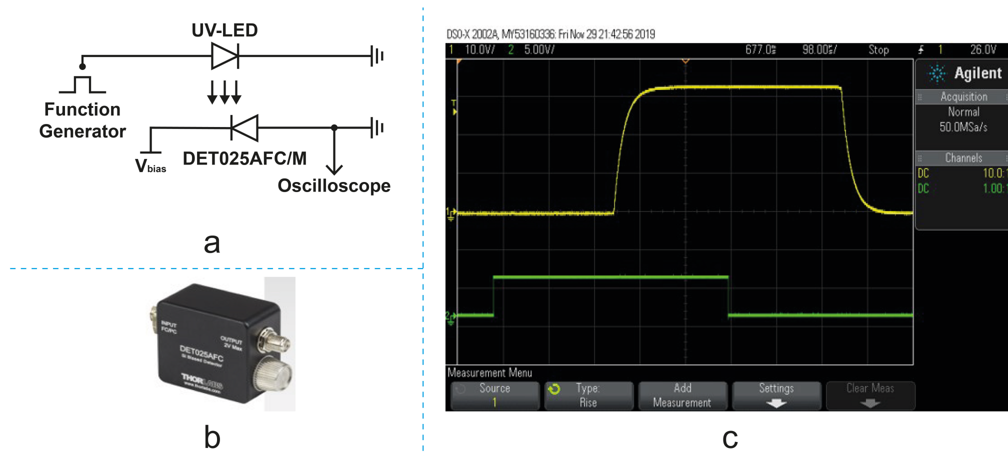


Figure 3.25: (a): Schematics of the circuit for reference commercial PD response time measurement, (b): commercial PD THORLAB DET025AFC/M, (c): response time result of reference commercial PD with 1 kHz UV-LED modulation.

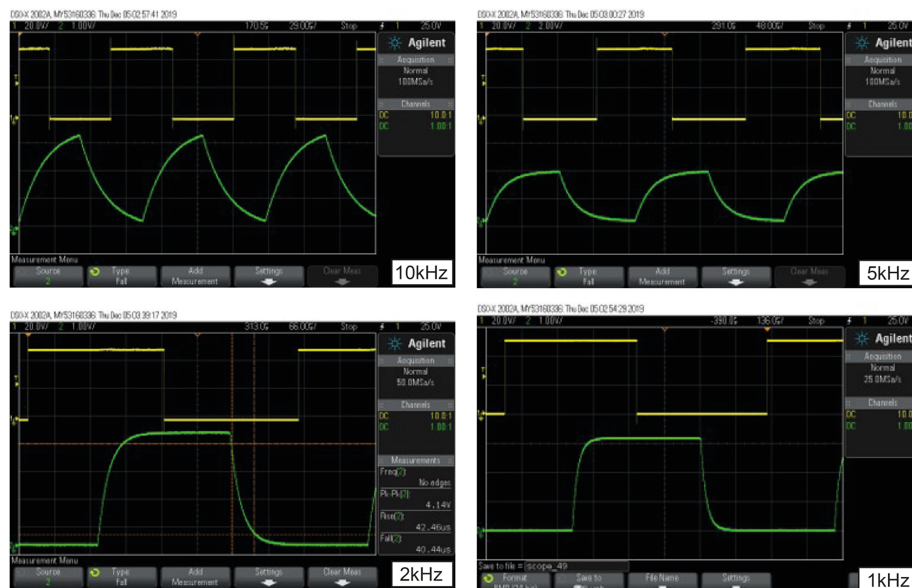


Figure 3.26: Response time results of reference commercial PD with 10 kHz, 5kHz, 2kHz and 1kHz UV-LED modulation.

To measure the response time of UV-LED itself, a commercial PD, THORLAB DET025AFC/M (Figure 3.25b) is connected into the system with the circuit shown in Figure 3.25a. The input signal of the UV-LED is modulated at 10 kHz, 5 kHz, 2 kHz, and 1 kHz. The results of response time measurement are shown in Figure 3.26, indicating a rise time of 40.60 μs and a fall time of 42.63 μs with the modulation speed of 2 kHz.

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Chapter 4

$(11\bar{2}0)$ Non-Polar GaN on Si Template with High-Temperature AlN Buffer Layer

The research of non-polar GaN on silicon starts with the fabrication of patterned silicon substrates and then the growth of high-temperature HT-AlN as a template. The template mentioned in this chapter needs both patterning fabrication and epitaxial growth. The basic idea of non-polar GaN on silicon substrates has been mentioned in Section 2.3.1. Normally (110) silicon or (112) silicon is used. However, GaN on silicon has a melt-back etching issue. To overcome this issue, the high-quality high-temperature AlN layer as an ideal buffer has to be initially prepared to separate the patterned silicon substrate and the subsequent GaN.

This work aims at growing high quality striped non-polar GaN with a flat top surface on patterned silicon substrates. On such a high quality non-polar GaN stripes, InGaN/GaN MQWs have been grown, where these MQWs have grown on different facets, namely, non-polar MQWs on the top surface, and others on the side facets which are perpendicular to the top surface. In this work, all the silicon substrates used are (110) silicon and thus all the GaN related epitaxy layers have an $(11\bar{2}0)$ orientation [1], [2].

In this chapter, the design and then fabrication of patterned templates on silicon for further overgrowth are presented in detail. A full procedure for the fabrication of the patterned templates has been established. The whole processes consist of substrate patterning, HT-AlN buffer layer epitaxy and a mask deposition for further selective overgrowth.

4.1 (110) Silicon Substrate Fabrication

Table 4.1 provides an orientation relationship between (111) silicon and other silicon such as (110) and (112) silicon substrates [1]–[3]. Generally speaking, it is preferred to

grow GaN on {111} silicon facets. In order to form non-polar GaN, we need to choose a particularly orientated silicon substrate, where {111} silicon facets need to be perpendicular to the substrate surface. In that case, the growth on such vertical facets can eventually lead to the formation of non-polar GaN. The equation for the angle between two cubic planes is shown in equation 4.1.

$$\boldsymbol{a} \cdot \boldsymbol{b} = |\boldsymbol{a}| \cdot |\boldsymbol{b}| \cdot \cos\theta \tag{4.1}$$

Table 4.1 demonstrates (112) Si which have two such facets can meet this requirement, while the (110) Si has four such facets. For the (112) Si, two facets are perpendicular to each other. To grow GaN stripes with flat sidewalls, two parallel facets are required. Both need to be perpendicular to the substrate surface. Thus, it is ideal to choose (110) Si to grow non-polar GaN. It has two pairs of parallel facets.

{111} Si index			Inclination angle against surface	
h	k	l	(110)	(112)
1	1	1	35.26°	19.47°
-1	1	1	90°	61.87°
1	-1	1	90°	61.87°
1	1	-1	35.26°	90°
-1	-1	1	144.74°	90°
-1	1	-1	90°	118.13°
1	-1	-1	90°	118.13°
-1	-1	-1	144.74°	160.53°

Table 4.1: Angular relationship between {111} silicon planes and the surface of (110) and (112) silicon substrates.

It is well-known than silicon can be effectively etched by potassium hydroxide (KOH) solution. However, the chemical etching rate is extremely low once the etching front meets any of {111} silicon facets. This is so-called anisotropic chemical etching, which provides us with an excellent opportunity to fabricate pattered silicon substrates for further selective overgrowth in order to obtain non-polar GaN.

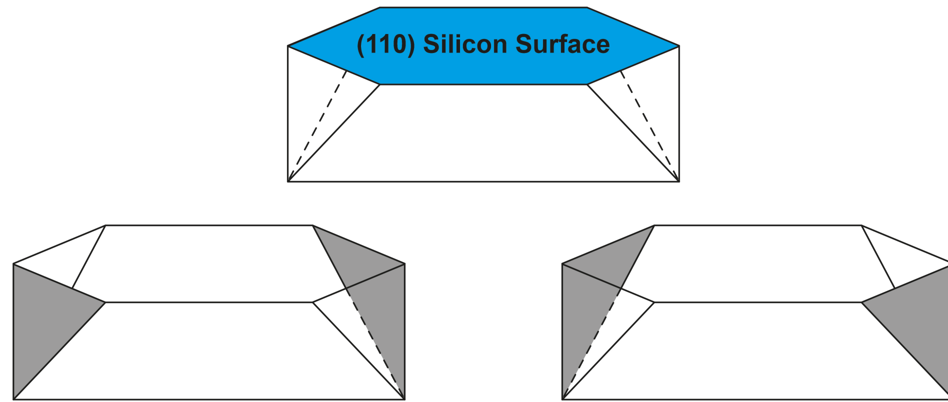


Figure 4.1: Six {111} facets after KOH etching of (110) Si. The blue top part is the surface of (110) Si, the two pairs of parallel {111} facets are painted in grey.

Figure 4.1 illustrates etched (110) silicon. By using one pair of the parallel {111} facets, the silicon stripes with two parallel sidewalls can be formed. Both side walls are perpendicular to the surface.

Fabrication Process

As usual, a (110) silicon substrate initially undergoes a standard cleaning process in order to remove any residuals by using solvents and then acids, where N-butyl acetate, acetone and isopropyl alcohol are used for removing organic contaminations. The mixture of sulphuric acid (H_2SO_4), hydrogen peroxide (H_2O_2) and deionised (DI) water are then used in order to remove any oxides [4], [5]. Subsequently, by using hydrogen peroxide, a very thin oxide will be formed on the surface via converting the surface into silicon dioxide (SiO_2). This very thin oxide will enhance the adhesion of SiO_2 mask prepared in the next step.

Figure 4.2 schematically illustrates a full procedure for the fabrication of a patterned (110) silicon substrate after surface treatment described above. A layer of SiO_2 is deposited by PECVD as a mask for subsequent wet etching. The thickness of the SiO_2 mask used in this work is 120nm. There may exist some particles remaining on the surface after the PECVD deposition step. Therefore, it is important to use solvent and DI water cleaning for further surface treatment after this step.

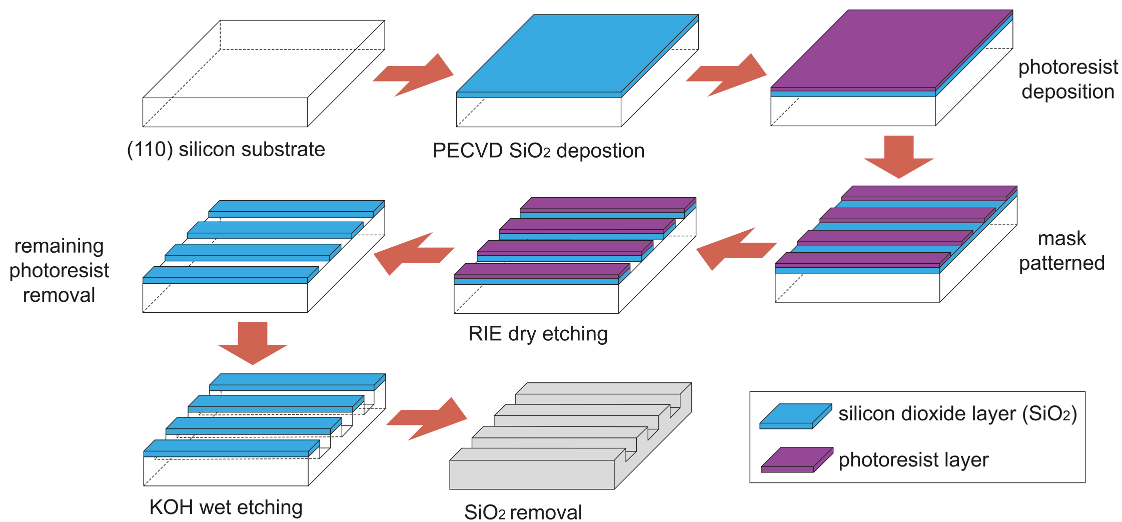


Figure 4.2: Schematics of (110) silicon substrate fabrication process.

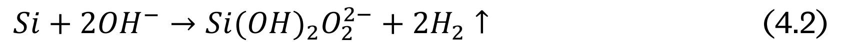
A layer of photoresist is then deposited on top of the substrate surface. The photoresist used is SPR-350. The rotation speed of spinning coater is set to 4000 RPM for 30 seconds. After photoresist coating, the sample is baked on a hot plate at 100 ˚C for 1 minute to harden the photoresist. The photoresist thickness used is typically ~1 μm measured after the baking step.

A mask aligner with a UV light source is used for transferring a strip pattern to the sample. The photomask pattern used in this work is 4 μm stripes with 4 μm opening windows. The photomask needs to be carefully aligned to be parallel with the direction of the cutting edge of (110) silicon substrate which is parallel to the (111) orientation. The optimised exposure time of this photoresist is 6 seconds to achieve a uniform pattern. MF-26A as a developer is used in order to remove exposed photoresist on the patterned substrate. The development time is generally 60 seconds. However, the scale of the pattern can be slightly adjusted by diluting the developer with additional DI water and tuning developing time.

Subsequently, the formed photo resist stripe as a mask to etch the SiO_2 layer underneath into SiO_2 stripes by RIE dry etching. Optimised RIE-etching conditions used for selective SiO_2 etching: CHF_3 with a flow rate of 35 sccm is used as etchant gases under an RF power of 90 W is used, leading to an etching rate of ~6 nm/min. The typical etching time is 20 minutes.

Wet Etching Process

After the formation of the patterned SiO_2 with 4 μm width SiO_2 stripes and 4 μm opening windows which act as a second mask for further chemical etching, the (110) silicon with such SiO_2 stripe masks on its top is immersed into an KOH solution with a concentration of 25% (wt.). The chemical etching of using KOH on Si can be described by Equation 4.2 given below [6].



$$Si + 2OH^{-} \rightarrow Si(OH)_2O_2^{2-} + 2H_2 \uparrow \quad (4.2)$$

The chemical etching initiates from the opening window areas between two neighbouring stripe SiO_2 masks, and then goes down further. As previously mentioned, the KOH almost does not etch {111} facets of silicon, where {111} facets are perpendicular to the surface. Eventually, two parallel sidewalls along the vertical direction are formed between two neighbouring stripe SiO_2 masks in each opening window.

Since the bottom of each trench formed between two neighbouring stripe SiO_2 masks in each opening window etched structure is still the (110) facet, the etching keeps going. Therefore, the etching depth can be controlled simply by etching time.

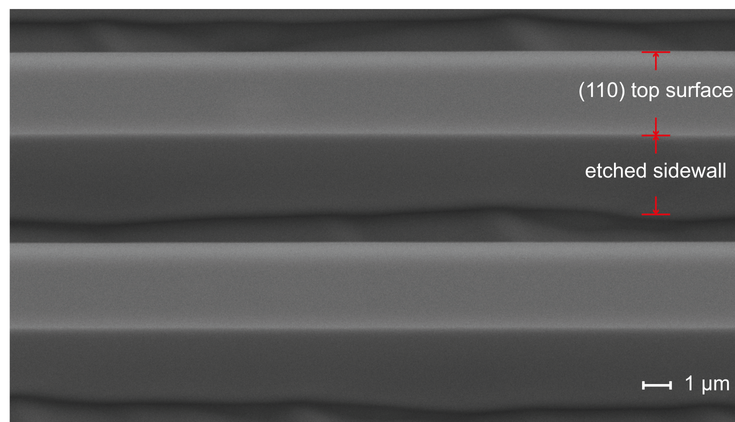


Figure 4.3: 30° tilted SEM image of the stripe patterned (110) silicon substrate.

After the desired etching depth is obtained, the chemical etching step is completed. The remained SiO_2 stripe masks are then removed simply by using hydrofluoric acid with a concentration of 10%. The process takes 10 minutes to thoroughly remove SiO_2.

Figure 4.3 shows the typical SEM image of a standard stripe patterned (110) silicon substrate, tilting it by 30°. The bottom of the trench in the figure is etched by KOH and shows an uneven morphology. Since the growth is happened at the sidewall, the bottom of the trench is better to be rough surface to reduce the unwanted growth from the bottom.

4.2 HT-AlN Buffer Layer Growth

Subsequently, a thick AlN buffer layer will be grown by using MOCVD, which is similar to any growth of GaN on (111) silicon substrates. This AlN buffer layer is required to cover all the facets formed in order to eliminate Ga etch-back issue during the followed GaN growth.

As the followed GaN growth is selectively performed on the vertical sidewall in each trench, not elsewhere, the growth of smooth AlN buffer layer becomes difficult. Furthermore, the sidewall is perpendicular to the top surface the thickness of the epitaxial layer may vary depending on the position on the sidewall; the closer to the bottom, the thinner the layer achieved. The thickness of the AlN need to be thick enough to cover all the facets of the silicon stripes including top surfaces, sidewalls, and the bottom of the trenches. Also, the thickness of the AlN should not be too thick which leads to rough surfaces and increasing of dislocations after growth. Thus, the thickness of the AlN buffer layer has been optimised to 200 nm on the sidewall near the top and 80 nm near the bottom.

Figure 4.4 schematically illustrates how the AlN buffer covers a stripe patterned (110) silicon substrate along with detailed cross-sectional SEM images taken at different positions along a vertical sidewall, showing the thickness of AlN buffer depends on positions along the vertical sidewall. The AlN buffer on the top surface is thickest, while the thickness of the AlN buffer on the sidewall gradually decreases.

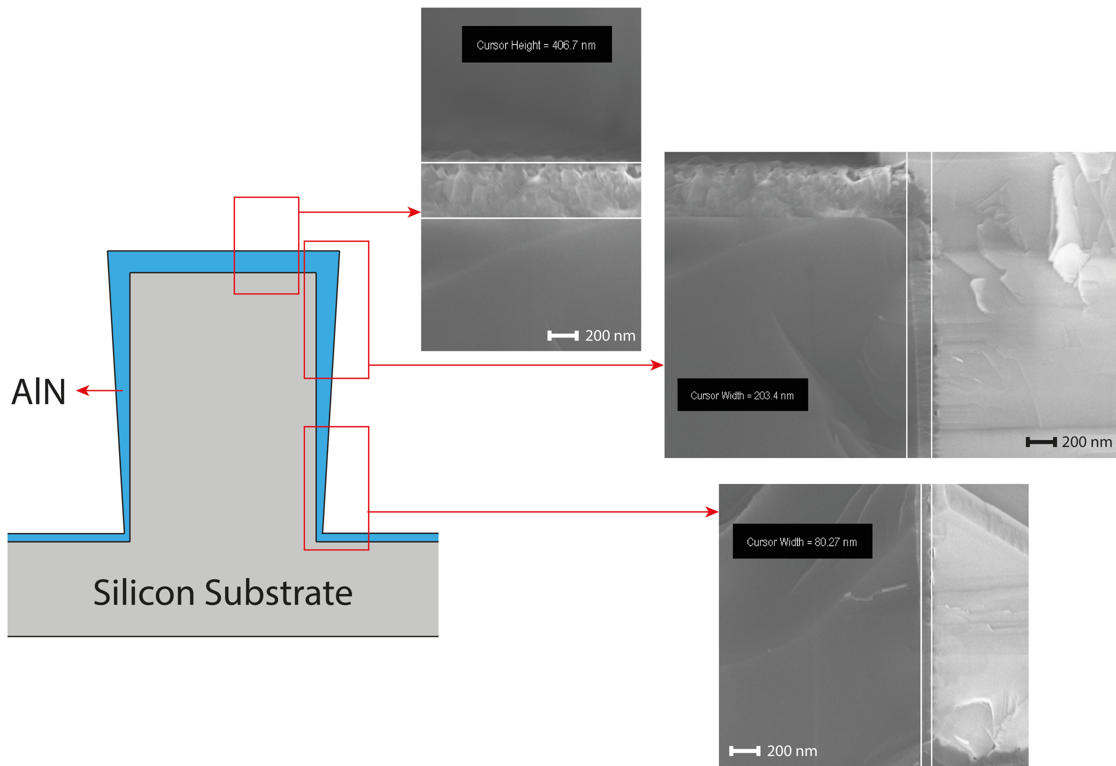


Figure 4.4: Cross-sectional schematics of AlN interlayer on the template with SEM measurement.

A standard procedure for the AlN buffer layer has been established. A high-temperature annealing process is initially applied to perform surface cleaning as usual which removes fabrication remaining particles and the thin oxidation layer on the growth surface . A TMAl pre-flow is then introduced with a small flow rate in order to form an Al nucleation layer, followed by AlN growth. A thin layer of low-temperature AlN (LT-AlN) is performed on the nucleation layer. Afterwards, a high-temperature AlN (HT-AlN) layer is grown on the LT-AlN layer. Finally, the template growth is finished with a very thin layer of low-temperature GaN (LT-GaN) layer to prevent the oxidisation of AlN for further processes.

The surface morphology of the AlN interlayer significantly affects the quality of further SiO_2 selective masks deposited, which will cover all the exposed facet except a (111) vertical facet on which GaN will be further grown. A rough surface may lead to peeling-off of the SiO_2 selective masks. The two different growth conditions for TMAl pre-flow steps are used. First condition uses TMAl pre-flow with a flowrate of 30 sccm for a pre-flow time of 20 seconds, while a TMAl flow with a flowrate of 20 sccm and a pre-flow time of 100 seconds are used for the second condition. The surface of the

sidewall is measured by using SEM with the 30° tilted sample stage, the measurement method is illustrated in Figure 4.5a. The surface morphologies of the AlN buffer layers grown under the two condition are presented in Figure 4.5b and 4.5c, showing their SEM images taken with a tilt angle of 30°, which confirms that the second condition (20 sccm for 100 sec) leads to better results than the first one (30 sccm for 20 sec) in terms of AlN morphology. TMAl pre-flow is the nucleation stage of the growth. From Figure 4.5b, the aluminium droplets from TMAl pre-flow has a poor coverage on the surface which leads to the ununiform growth and the worse surface morphology compare to Figure 4.5c.

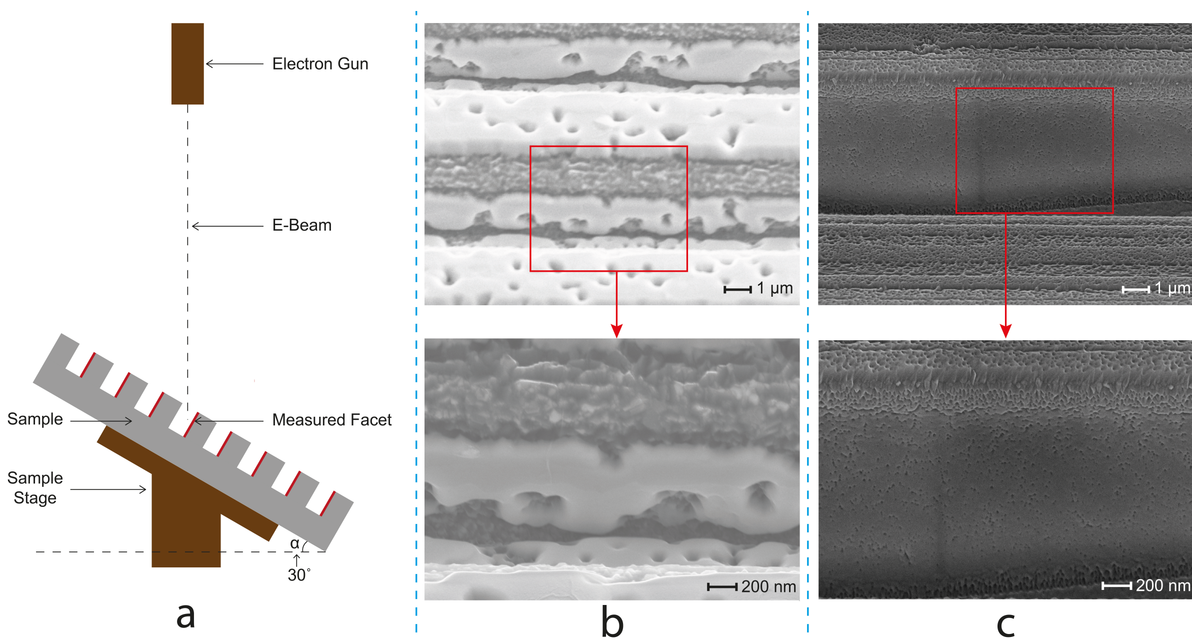


Figure 4.5: 30° tilted top-view SEM images of the grown template (a): schematic illustration of the measurement; (b): TMAl preflow of 30 sccm for 20 seconds and (c): TMAl preflow of 20 sccm for 100 seconds.

Both the TMAl pre-flow and subsequent AlN growth which are the two key parameters have been optimised in order to achieve a smooth surface of growth facet. Subsequent AlN growth consists of two steps, a thin AlN layer deposited initially at a low temperature (1085 °C, which we call LT-AlN) followed by AlN growth at a high temperature (1280 °C, which is labelled as HT-AlN). One of the critical parameters is due to the TMAl flowrate. The LT-AlN layer growth is conducted using an TMAl flowrate which is the same as that for the pre-flow step. For the HT-AlN growth step, the TMAl flow rate has been optimised in order to achieve a smooth surface.

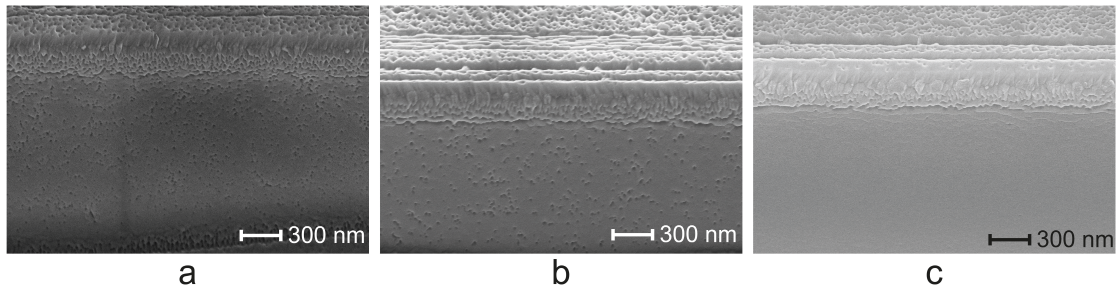


Figure 4.6: 30° tilted top view template SEM images of AlN buffer layer growth facet with different TMAl flowrate of (a): 120 sccm, (b): 30 sccm, (c): 20 sccm.

Figure 4.6 shows the plan-view SEM images of the AlN buffer layer grown using different TMAl flowrates for the HT-AlN but with identical pre-flow step and LT-AlN steps. Under a high TMAl flowrate of 120 sccm the surface of the AlN buffer exhibits a high density of pits as shown in Figure 4.6a. When the TMAl flowrate decreases to 30 sccm, a significant reduction in the density of pits is observed as displayed in Figure 4.6b. Further reducing the TMAl flowrate to 20 sccm (Figure 4.6c) leads to the smooth surface as shown in Figure 4.6c. Please note that the SEM images in Figure 4.6 are taken with a 30° tilt. The top surface morphology which will be selectively covered by subsequent SiO_2 deposition is quite different from the one (i.e., the vertical facets on which further GaN growth will be carried out).

4.3 Selective SiO_2 Mask Deposition

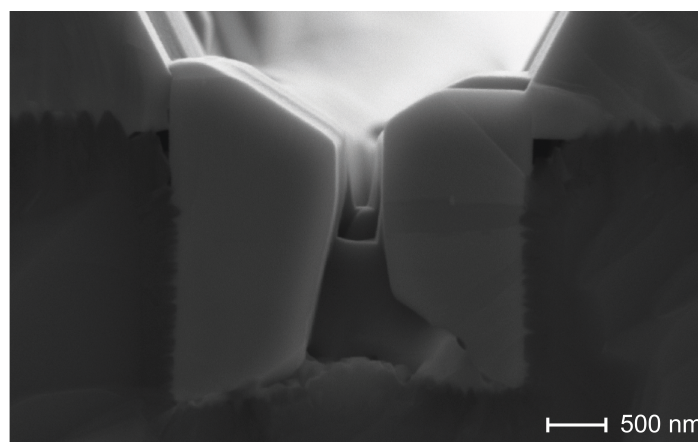


Figure 4.7: Cross-sectional SEM image of GaN growth without blocking layer.

As discussed in sections 4.1 and 4.2, two (111) silicon vertical sidewalls in each trench are formed by the anisotropic chemical etching method using KOH. After that, all the

formed facets are covered by an AlN buffer layer. In order to allow subsequent GaN growth to be conducted only on one of vertical (111) facets, further SiO_2 masks will have to selectively cover all the other facet except one of the vertical (111) facet. Otherwise, subsequent GaN will be grown on both of them. Figure 4.7 show a typical example, exhibiting GaN grown on both facets. From the figure, the growth is obtained on both of the sidewalls and the top of the stripes. The GaN growth in this work are normally Ga-polar (0001) GaN to achieve smooth surface. The two sidewalls have opposite growth directions but grow same (0001) Ga-polar GaN, hence the growth will stop after the trench is filled with the GaN crystal.

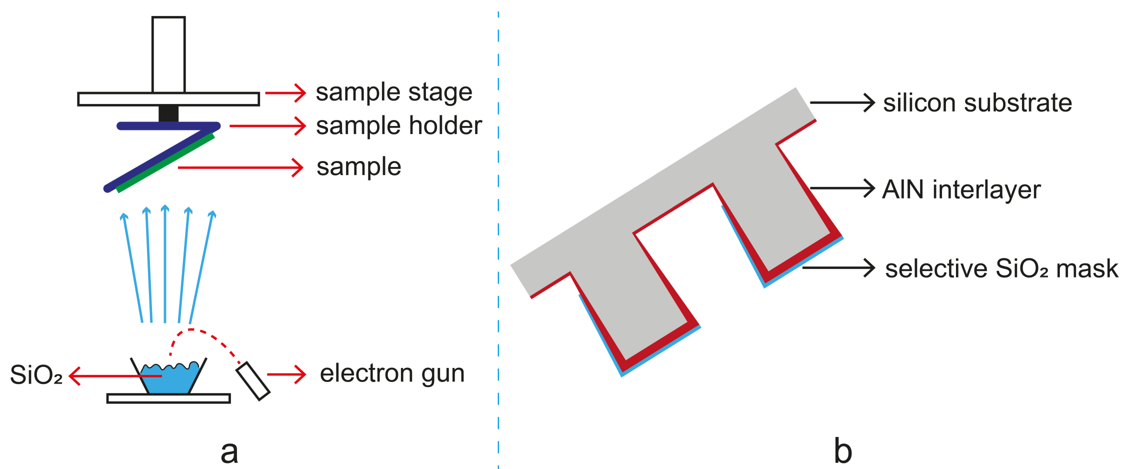


Figure 4.8: Schematics of (a): e-beam SiO_2 deposition with tilted sample holder; (b): template after SiO_2 deposition.

An e-beam evaporator is used to deposit SiO_2 for the purpose of selective growth. Figure 4.8a illustrates such a SiO_2 deposition through an e-beam evaporator with a tilted sample holder. An image of the template after SiO_2 deposition is presented in Figure 4.8b. The deposition of such SiO_2 is confirmed by a SEM image taken at a tilted angle from top. Figure 4.9a shows a line on one vertical facet covered with SiO_2 which is the boundary of the SiO_2, while Figure 4.9b shows another vertical facet without any SiO_2. This confirms that only one sidewall has been covered by SiO_2. Various thickness of the SiO_2 has been optimised. The optimised thickness for the SiO_2 deposition is ~30 nm.

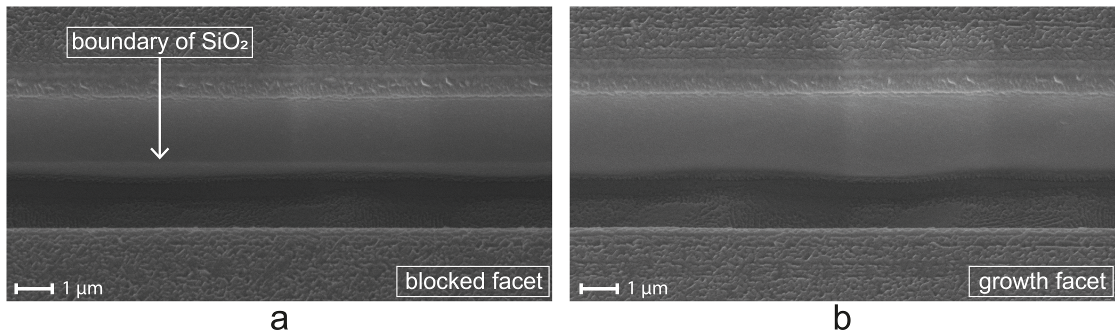


Figure 4.9: 30° tilted top view template SEM images of (a): blocked facet; (b): growth facet.

4.4 Final GaN Overgrowth

A standard treatment before further GaN overgrowth is used, namely, cleaning with acetone solvent for 3 minutes and then IPA for 3 minutes. Both steps are performed in an ultrasonic bath. After the cleaning treatment, HCl is used first, and then a dilute HF with a short time is further used for advanced cleaning. Finally, boiled aqua regia is utilised to enhance the cleanness level for 15 minutes in order to eliminate any potential contamination.

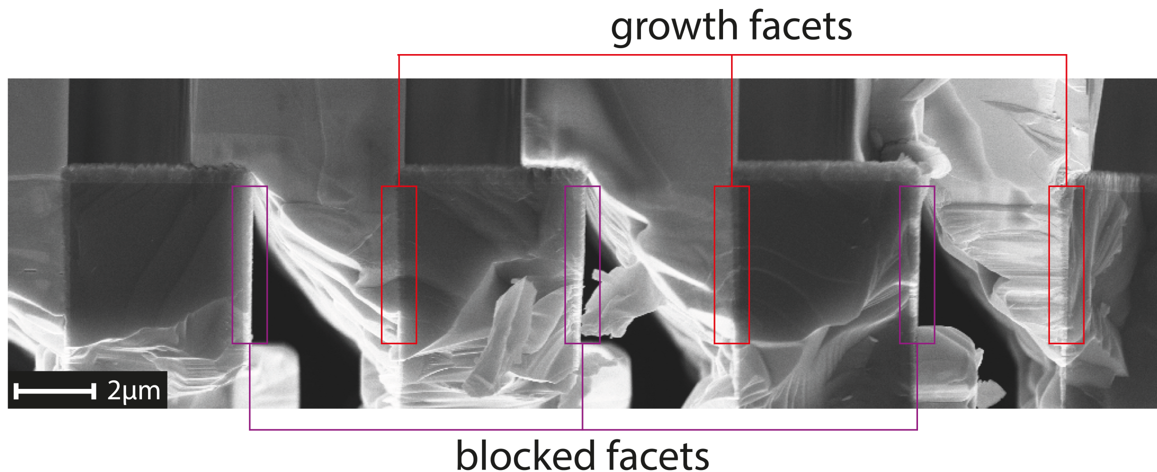


Figure 4.10: Cross-sectional SEM image of correct GaN growth.

After that, standard GaN growth conditions which we optimised for GaN on (111) silicon is used for further GaN selective growth on such a patterned (110) silicon substrate. Figure 4.10 shows a typical cross-sectional SEM image of our non-polar GaN stripes with vertical sidewalls on such a patterned (110) silicon substrate, demonstrating the GaN is indeed grown on the vertical facet without any SiO_2, while

GaN growth on any other facets is effectively suppressed.

4.5 Summary

The fabrication of a patterned template for final GaN overgrowth on patterned (110) silicon consists of silicon substrate patterning, AlN buffer growth, and selective SiO_2 mask deposition. TMAl pre-flow and HT-AlN buffer layer are two critical parameters in order to achieve a smooth AlN buffer layer deposited on vertical facets, on one of which the final GaN growth is conducted. The surface morphology of AlN layer highly rely on the TMAl flowrate. With a small TMAl flowrate (20 sccm) during TMAl preflow, the Al droplet for nucleation covers the growth surface with a high density and finally leads to a smooth surface morphology. The temperature of HT-AlN is optimised under previous work [7], [8]. A selective SiO_2 mask is obtained by an e-beam evaporator where the e-beam is injected at an optimised angle so that only one of the vertical (111) facets is allowed to be exposed while all the other facets are covered by the SiO_2 mask.

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Chapter 5

$(11\bar{2}0)$ Non-Polar GaN Stripes on Si Overgrowth

This chapter presents detailed growth and material characterisation of non-polar $(11\bar{2}0)$ GaN prepared on the patterned template described in Chapter 4, demonstrating non-polar $(11\bar{2}0)$ high crystal quality GaN stripes with a flat top surface and perpendicular sidewalls on (110) silicon template. The non-polar GaN presented in this work is obtained by means of using a selective overgrowth approach on the patterned template, where the GaN growth takes place only on one of the vertical (111) facets. This is achieved through this two-temperature growth method (LT-GaN and HT-GaN) on the patterned template as described in Chapter 4. This chapter presents a detailed overgrowth process in the first section. The second section focuses on the main issue during growth, namely melt-back etching. Section 5.3 and 5.4 provide the details on the optimisation of overgrowth conditions. The final section presents the material characterisation in order to evaluate of the crystal quality of our non-polar $(11\bar{2}0)$ GaN grown on the patterned templates. A brief conclusion is given at the end of this chapter.

5.1 Optimisation of Patterned Template Fabrication

Overgrowth Mechanism

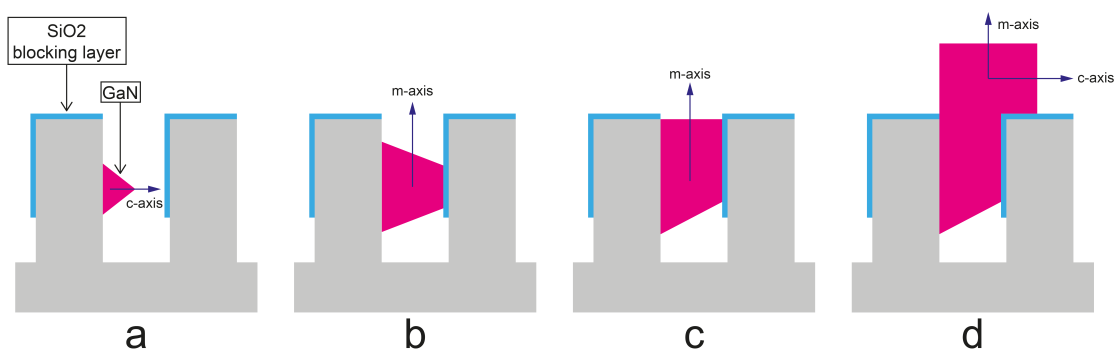

Figure 5.1: Schematics of $(11\bar{2}0)$ GaN overgrowth on (110) silicon mechanism.

Figure 5.1 schematically display a growth evolution process of $(11\bar{2}0)$ GaN overgrown on the patterned (110) silicon template described in Chapter 4. The overgrowth starts from a vertical (111) facet, the only facet which is not covered by SiO_2 masks. Initially, the overgrowth is carried out mainly along c-axis (Figure 5.1a) on the (111) facet, which is also the horizontal direction. After filling the gaps between two neighbouring stripes (Figure 5.1b) the overgrowth process continues along the vertical direction which is the non-polar direction (m-axis) (Figure 5.1c). Since trench between the two stripes are filled by grown GaN, the sources cannot contact the bottom facet after the gaps are filled and leads to the termination of the growth on the bottom facet. Once the overgrowth is above the top surface of the template, the overgrowth extends above the SiO_2 masks. Eventually, regularly arrayed GaN stripes with two parallel vertical sidewalls and a flat surface are formed.

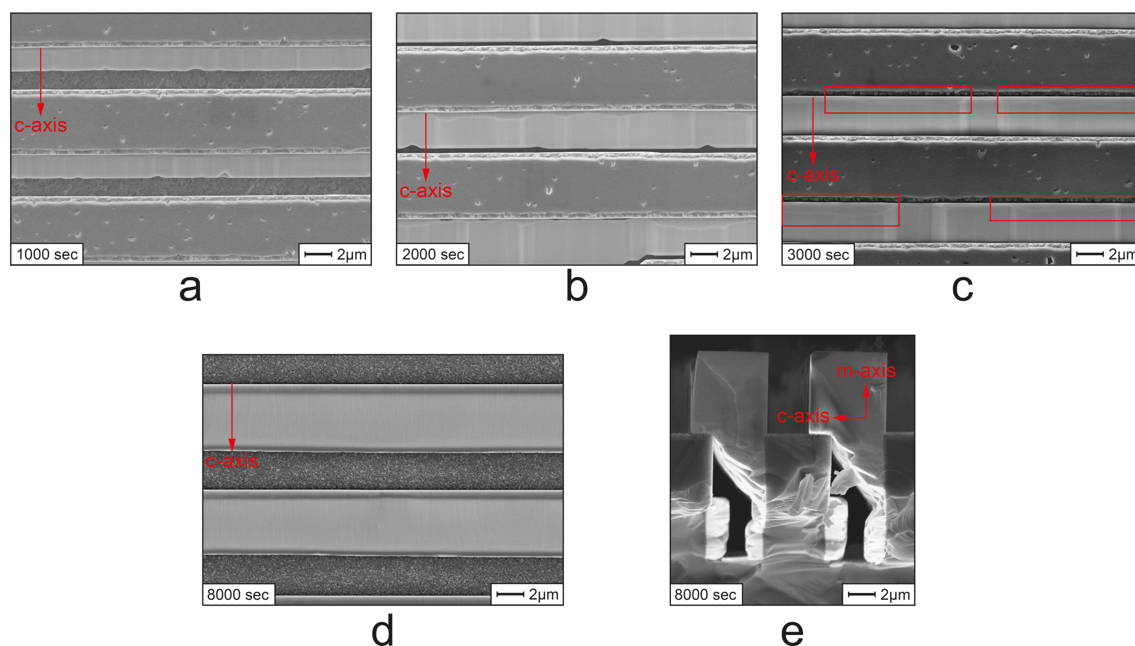

Figure 5.2: SEM images of $(11\bar{2}0)$ non-polar GaN overgrowth on (110) silicon with growth durations of (a): 1000sec top view; (b): 2000 sec top view; (c): 3000 seconds top view; (d): 8000 seconds top view; (e): 8000 seconds cross-section.

Figure 5.2a, 5.2b and 5.2c are the plan-view SEM images of the overgrown non-polar GaN as a function of growth time from 1000, 2000 to 3000 seconds. The gap is nearly filled in Figure 5.2b and the gap is fully filled in Figure 5.2c, there are clear boundaries in the red rectangles which indicates the process of achieving flat top surface. A further increased growth time allow us to further improve the crystal quality and

control the thickness. Figure 5.2d and 5.2e show the plan-view and cross-sectional SEM images of an overgrown non-polar GaN stripe with a growth time of 8000 seconds. According to Figure 5.2e, the sidewall is perpendicular to the sample surface and the top surface is parallel to the sample surface which indicates a perfect shape of the stripes. Figure 5.2e also confirms that growth occurs only on one sidewall of the silicon stripe and the other sidewall has been blocked.

Overgrowth Process

A clean surface for subsequent GaN overgrowth after SiO_2 mask deposition using the e-beam evaporator as described in Chapter 4 is important. During the previous ex-situ deposition of SiO_2, there is a potential to the generation of contamination. Therefore, we adopt an annealing process for an in-situ surface treatment prior to the non-polar GaN growth in our MOCVD chamber. The main parameters of the annealing process are due to annealing temperature and annealing time. The various annealing conditions used are as shown in Table 5.1.

Condition	Temperature (˚C)	Time (second)
A	1291	600
B	1291	900
C	1310	900

Table 5.1: Annealing conditions of $(11\bar{2}0)$ GaN overgrowth.

Figure 5.3 shows the plan-view SEM images of the overgrown GaN under three different annealing conditions listed in Table 5.1. Figure 5.3a show the sample with condition A, namely, the lowest annealing temperature and shortest annealing time. Clearly, it shows irregularities of the formed non-polar GaN stripes and also voids on the GaN stripes. With increasing annealing time to 900 seconds, which is condition B, the situation is better, and the number of voids are massively reduced, and the irregularity of stripes have also been improved. However, this improvement is still not good enough. Further increasing annealing temperature to 1310 ˚C with an annealing time of 900 second, which is condition C, regularly arrayed non-polar GaN stripes with a nice shape have been obtained. During the fabrication process of the template,

the sample surface may obtain contaminations. Longer annealing time with higher annealing temperature give a better treatment of the growth facet before GaN growth. The cleaner growth interface leads to uniform growth on the growth facet. In Figure 5.3a, it clearly shows large voids on the GaN stripes with the growth condition A. The large voids are eliminated under growth condition B which shown in Figure 5.3b. But the surface of the stripes is still uneven, and the shape of the stripes are ununiform. The stripes with smooth surface and uniform shape are achieved under growth condition C (Figure 5.3c). The target of this optimisation is to eliminate the voids and to achieve the smooth surface of the stripes.

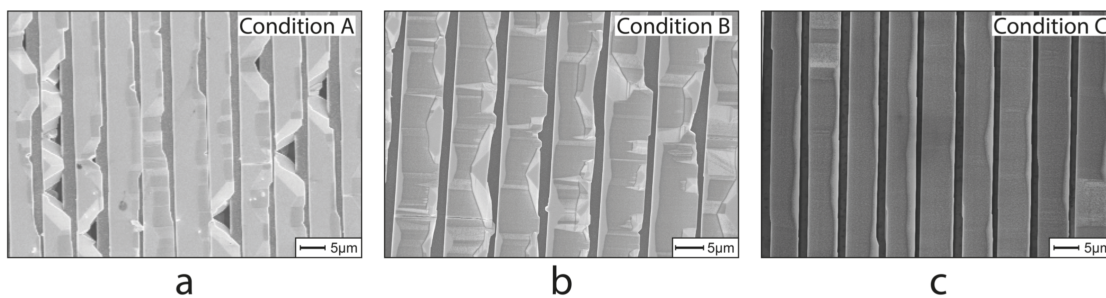

Figure 5.3: Top view SEM images of (11$\bar{2}$0) GaN overgrowth under annealing (a): condition A; (b): condition B; (c): condition C.

In order to eliminate any risk of potential Ga melt-back etching, the subsequent GaN growth after the in-situ surface treatment consists of the growth with two different temperatures. The first part is the growth under a high temperature (~1300°C) with a short growth time. This part enhances a lateral growth rate in order to make the trenches filled quickly. The second part is to conduct the GaN growth at an optimised temperature of ~1200°C, which is 100 °C lower than the temperature in the first step. A reduced temperature leads to a higher growth rate along the vertical direction and a reduction in lateral growth. Lateral growth is related to the diffusion length of Ga adatoms which increases with higher temperature. Thus, the longer diffusion length of Ga adatoms is achieved under a higher growth temperature which finally leads to a faster lateral growth rate. In contrast, lower temperature reduces the lateral growth rate and ensures a higher growth rate on top surface (m-direction) than sidewall (c-direction). This facilitates the shape of finally formed nonpolar GaN stripe with high and also vertical sidewalls. Furthermore, it also reduces the risk of Ga melt-back

etching as well. The typical growth time for the second step is around 7000 seconds, leading to the ultimate non-polar GaN stripes with a flat top surface and straight sidewalls.

5.2 Optimisation of Template Design and Growth Conditions for Eliminating Melt-Back Etching

Melt-back etching is one of the main issues for GaN growth on silicon substrates, which is particularly important for semi-polar and non-polar GaN on Si [1], although an AlN buffer layer is initially grown prior to any further GaN growth. In this work, a number of approaches have been attempted in order to eliminate melt-back etching.

A shallow trench leads to a high chance of GaN deposited on the bottom of the trench which is (110) facet in addition to the GaN grown on the desired vertical (111) facet. The competition of the growth on these two facets leads to a mixture of GaN with two different orientations, which eventually destroys non-polar GaN growth and also generate Ga melt-back.

<table>
<tr><th>Sample Number</th><th>Etching Depth (μm)</th><th>HT-GaN Temperature (°C)</th><th>LT-GaN Temperature (°C)</th><th>V/III Ratio</th><th>Growth Time (s)</th></tr>
<tr><td>N1</td><td>4</td><td rowspan="4">1300</td><td>1200</td><td>454</td><td>6000</td></tr>
<tr><td>N2</td><td>5</td><td>1200</td><td>454</td><td>6000</td></tr>
<tr><td>N3</td><td>7.5</td><td>1200</td><td>136</td><td>8000</td></tr>
<tr><td>N4</td><td>5</td><td>1300</td><td>454</td><td>6000</td></tr>
</table>

Table 5.2: Growth conditions of sample N1, N2 and N3.

The growth condition of sample N1, N2 and N3 are listed in Table 5.2. Figure 5.4 shows the cross-sectional SEM images of nonpolar GaN samples grown on a patterned template with a trench depth of ~4 μm, exhibiting severe melt back etching almost everywhere.

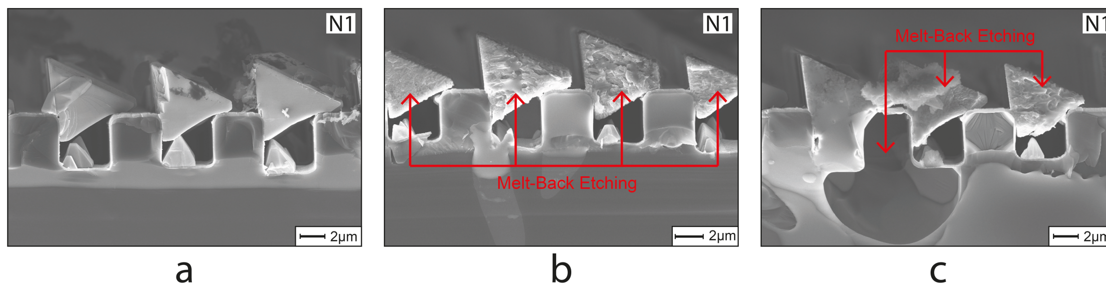

Figure 5.4: Cross-sectional SEM images of different spots on the sample with a trench depth of ~4µm (N1).

The bottom of the trench can keep etching in KOH solution so it is not a fixed (111) orientation that can stop the chemical etching. The defects of the GaN crystal grown on such surface have a high density and result in decomposition of the GaN, eventually generates melt-back etching. Figure 5.5 shows a cross-sectional SEM comparison of the nonpolar GaN samples grown on the patterned templates with different trench depths, which are ~4 µm, ~5 µm, and ~7.5 µm, respectively, given in Figure 5.5 a, b, and c, respectively. This comparison clearly demonstrates that a deep trench structure for a patterned template leads to a significant reduction in the bottom growth which generates melt-back etching.

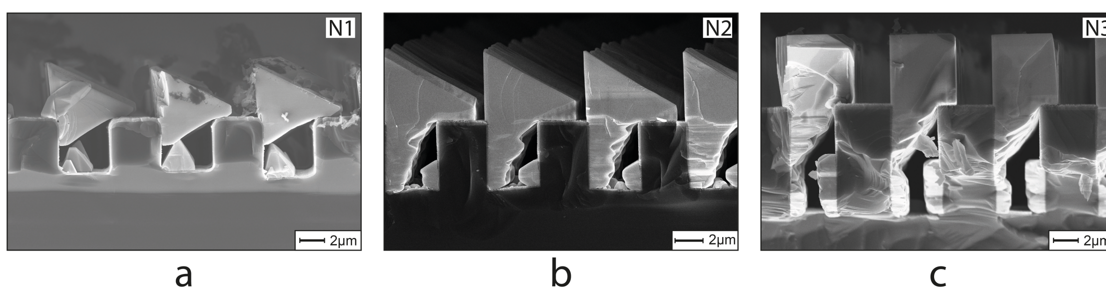

Figure 5.5: Cross-sectional SEM images of non-melt-back spots on the sample with a trench depth of (a): ~4 µm (N1), (b): ~5 µm (N2) and (c): ~7.5 µm (N3).

In order to further reduce a risk of Ga melt-back etching, the growth temperature for the second temperature GaN growth needs to be further reduced if a long growth time for GaN is required.

Figure 5.6 shows the cross-sectional SEM images of two samples grown on identical patterned templates (both with a trench depth of ~5µm) but at different growth temperatures. Figure 5.6a corresponds to the sample growth at 1200°C, while Figure

5.6b provides the SEM image of the sample grown at 1300 ˚C , showing clear melt-back etching.

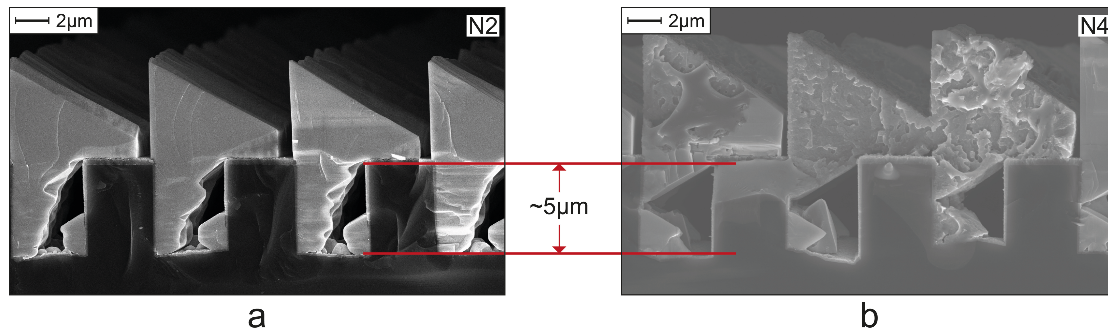

Figure 5.6: Cross-sectional SEM images of the samples with the same etched trench depth with a growth temperature of (a): 1200˚C (N2) and (b): 1300 ˚C (N4).

In conclusion, both trench depth and growth temperature affect the phenomenon of melt-back etching. Melt-back etching is irreversible. It damages the surface of the sample, substantially deteriorating the crystal quality. By decreasing the temperature and increasing the etching depth, melt-back etching can be substantially reduced. This is critical during the development of non-polar GaN devices.

5.3 Optimisation of Growth Temperature

Sample Number	Etching Depth (μm)	HT-GaN Temperature (˚C)	LT-GaN Temperature (˚C)	V/III Ratio	Growth Time (s)
N5	7.4	1230	1200	136	6000
N6	7.5	1266			7000
N7	7.3	1280			8000
N8	7.5	1300			6000
N9	7.2	1310			6000
N10	7.6	1325			6000

Table 5.3: Growth conditions of sample N5 to N10.

In order to further improve the crystal quality of non-polar GaN grown on patterned templates, a systematic investigation is carried out in terms of optimising growth temperature. As any further increase in the temperature for the second GaN growth step leads to a high risk of GaN melt-back etching, the optimisation work is carried out only for the first GaN growth. Table 5.3 shows the growth condition of sample N5

to N10.

XRD rocking curve is widely used to evaluate the crystal quality of GaN. Figure 5.7 presents the XRD rocking curve of the $(11\bar{2}0)$ GaN stripe sample labelled as N7, showing an XRD rocking curve FWHM of 324.36 arcsec (0.0901°) along the c-direction and a XRD rocking curve FWHM of 381.96 arcsec (0.1061°) along the m-direction.

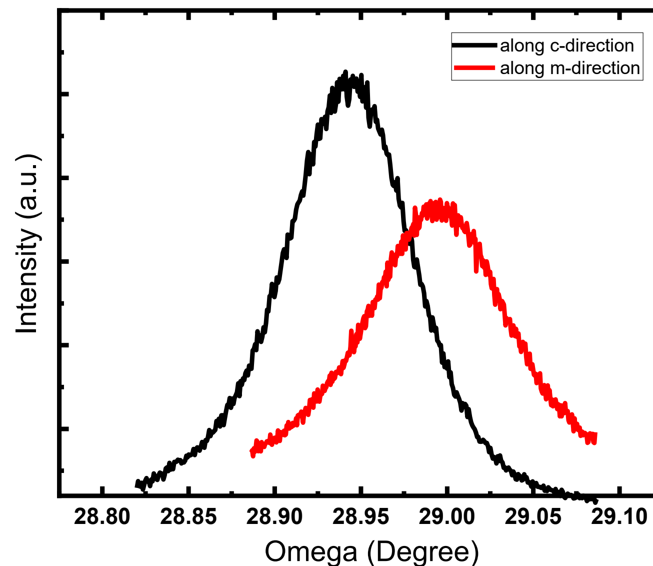

Figure 5.7: Sample N7 XRD rocking curves with two measurement directions.

Detailed evaluation for the crystal quality of non-polar GaN is to measure XRD rocking curve FWHMs as a function of azimuth angles from zero to 180°, where the azimuth angle is defined as zero when the projection of an incident X-ray beam is along c-direction of the epilayer. It means that the zero-azimuth angel corresponds to the c-direction, while the 90° azimuth angel represents the m-direction.

Figure 5.8 shows the XRD rocking curve FWHMs as a function of growth temperature (i.e., all the samples listed in Table. 5.3), exhibiting that the sample grown at 1230 °C the lowest temperature listed in Table 5.3 results in the worst crystal quality, where this sample shows a XRD rocking curve of 544.68 arcsec (0.1513°) along the [0001] direction (i.e., c-direction) and 874.8 arcsec (0.243°) along the $[1\bar{1}00]$ direction (.i.e., the m-direction). The best result is obtained on the sample grown at 1280 °C, which demonstrates an XRD rocking curve FWHMs of 338.04 arcsec (0.0939°) along [0001]

direction, 353.88 arcsec (0.0983°) along [1$\bar{1}$00] direction. A further increase in growth temperature leads to an increase in XRD rocking curve FWHM. For example, the sample grown at 1310^0 and 1325^0 C exhibit their XRD rocking curve FWHMs of 399.24 arcsec (0.1109°) and 400.68 arcsec (0.1113°) along the [0001] direction, respectively. The crystal quality is much better than standard (11$\bar{2}$0) GaN directly grown on sapphire without involving any overgrowth technique which typically exhibits a XRD rocking curve FWHM of 1180 arcsec along the [0001] direction and 1880 arcsec along the [1$\bar{1}$00] direction [2].

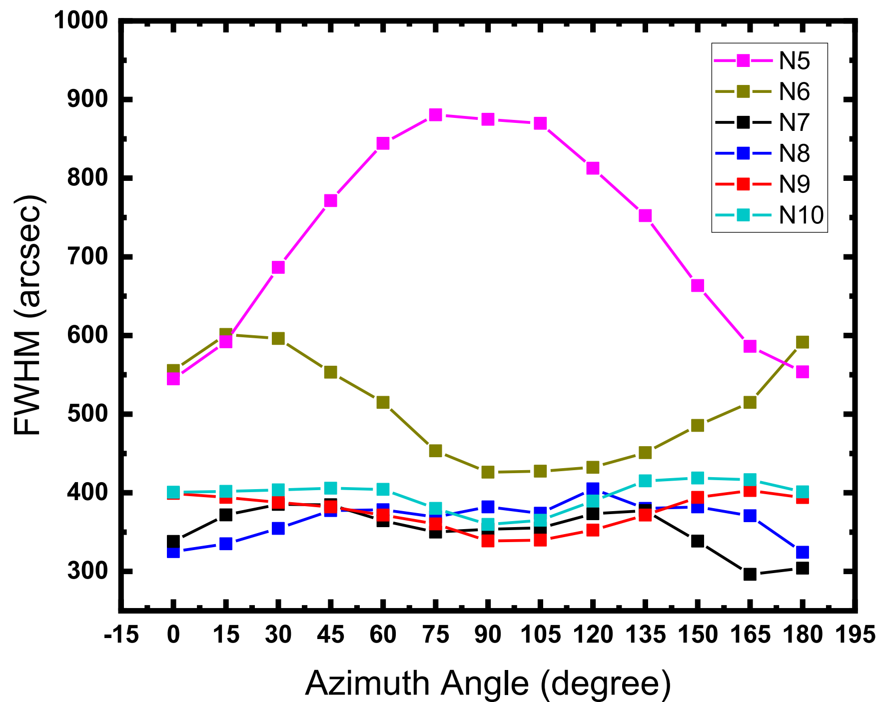

Figure 5.8: FWMHs of (11$\bar{2}$0) GaN rocking curves plotted with different azimuth angles for sample N5-N10.

The FWHM of the rocking curve measured from XRD is related to dislocation density. The dislocation density can be roughly estimated by Hirsch model shown in Equation 5.1.

$$\rho = \frac{\beta^2}{9\boldsymbol{b}^2} \tag{5.1}$$

Where ρ is dislocation density, β is XRD measured rocking curve physical broadening, $\boldsymbol{b}$ is the Burgers vector length in cm. There are three main types of

perfect dislocations in the wurtzite crystal lattice: **a**-type, **c**-type and **a**+**c**-type. For (11-20) non-polar GaN, the dislocation density strongly depend on the orientation during the measurement due to the anisotropy of non-polar GaN, which leads to the different dislocation densities under different azimuth angles [3]–[5].

5.4 Optimisation of V/III Ratio

Non-polar GaN with a smooth and flat top surface is essential for further growth of any device structures on top. An optimisation has been performed in terms V/III ratio which is a key factor. Generally speaking, a reduction in V/III ratio enhances a lateral growth rate [6], which helps obtain a flat surface. Table 5.4 shows the growth condition of sample N11 to N14, the V/III ratio is calculated in the MOCVD computer by applying the partial pressure of the certain bubbler.

Sample	N11	N12	N13	N14
Flowrate NH_3/TMGa (sccm)	1825/40	1000/40	600/40	300/40
V/III Ratio	828	454	272	136
Etching Depth (μm)	7.3	7.6	7.5	7.5
HT-GaN Temperature (°C)	1300			
LT-GaN Temperature (°C)	1200			
Growth Time (s)	7000	6000	7000	7000

Table 5.4: Growth conditions of sample N11 to N14.

Figure 5.9 displays the cross-sectional SEM images of the samples grown under different V/III ratio listed in Table 5.3 demonstrating that a reduction in V/III ratio significantly improve the top surface of the GaN stripe. Finally, with a V/III ratio with ~130 allows us to achieve a flat top surface. Lower V/III ratio leads to a 2D growth mode. Eventually, the lateral growth is limited and form high stripes with a flat top surface as well as a vertical sidewall.

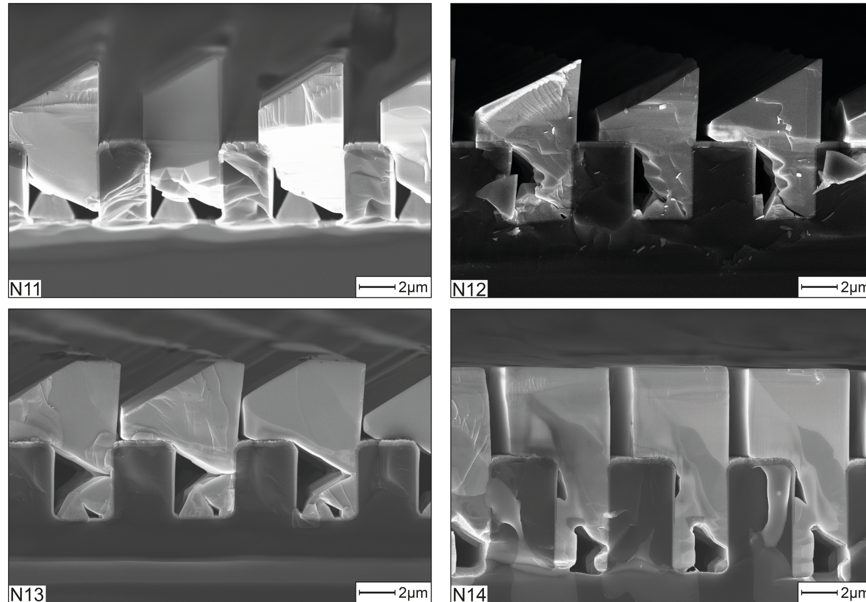

Figure 5.9: Cross-sectional SEM images of sample N11, N12, N13 and N14.

5.5 Optical Characterisation

Low-temperature PL measurements are very useful for the optical characterisation of nonpolar GaN, in particular the investigation of BSFs [7], one of the major defects an addition to dislocations in nonpolar GaN.

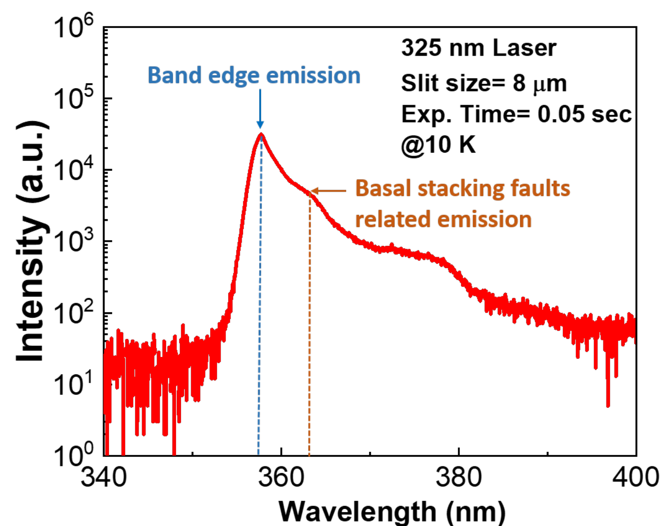

Figure 5.10: Photoluminescence spectrum of the non-polar (11$\bar{2}$0) GaN stripes grown on patterned (110) Silicon measured at 10K.

Figure 5.10 shows a PL spectrum of sample N7, measured at 10K using a 325 nm He-Cd laser as an excitation source. Figure 5.10 is plotted on a log scale in order to identify

any weak peaks. In addition to a very strong emission peak at 357.7 nm, which is due to the band-edge emission of the GaN, there is another weak peak at 363.6 nm, which is due to the BSFs-related emission [7]. The BSF has a structure of very thin zinc-blende layer embedded in the wurtzite matrix and a lower energy compare to pure GaN crystals, the large offset of the conduction band at the interface of zinc-blende layer and the wurtzite matrix, hence the BSFs can be considered as quantum-well like regions. The emission energy of the BSFs is lower and the wavelength is longer than band edge emission of GaN [8]. The ratio of the band edge emission intensity to the BSFs-related emission intensity is ~7.5, indicating an exceptionally low BSF density level.

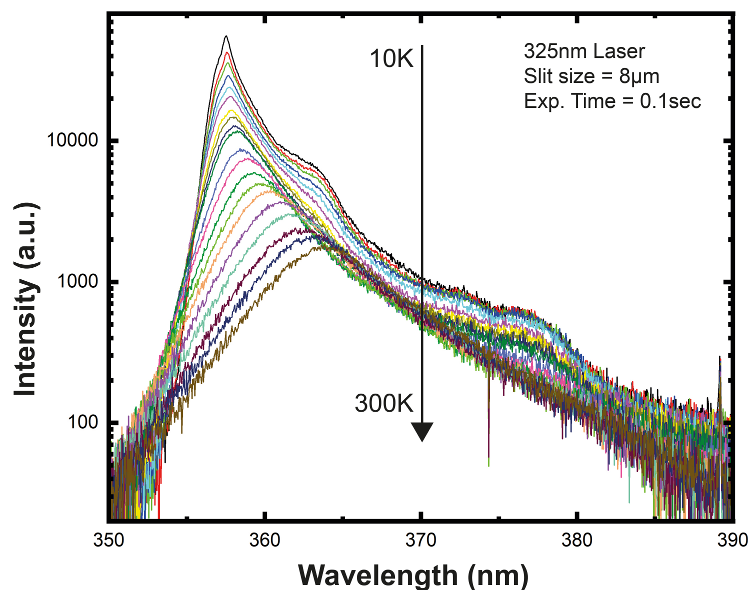

Figure 5.11: Temperature-dependent photoluminescence spectra of the non-polar (11$\bar{2}$0) GaN stripes grown on patterned (110) Silicon measured from 10K to 300K.

Figure 5.11 shows the temperature-dependent PL (TD-PL) spectra, exhibiting a redshift of the band-edge emission is observed with increasing temperature. To observe the redshift clearly, the peak energies have been plotted as a function of temperature in Figure 5.12. This redshift is caused by temperature-induced band-gap shrinkage [9]. The BSF-related emission is getting weaker with the increasing of the temperature and the band edge emission dominates among the temperature range. This further confirms the low BSF density level.

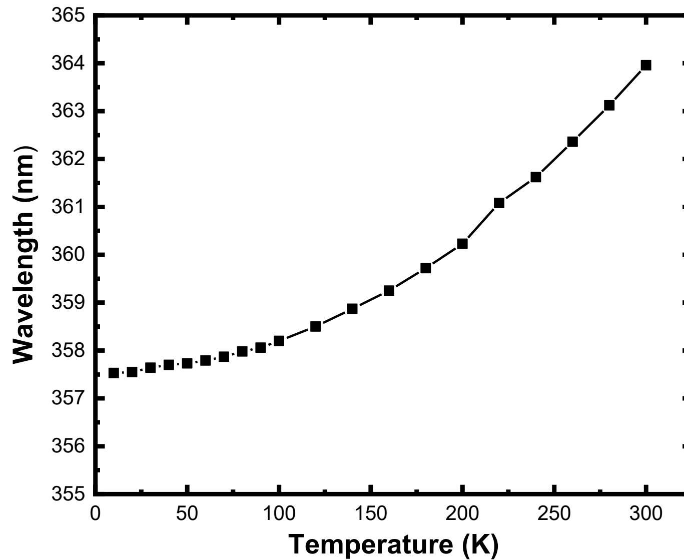

Figure 5.12: Temperature-dependent PL Peak wavelengths as a function of temperature.

5.6 Conclusion

This chapter established the detailed overgrowth of non-polar (11$\bar{2}$0) GaN stripes on patterned (110) silicon substrates. A two-temperature growth approach has been used in order to achieve selective growth on the patterned silicon substrates, allowing us to obtain non-polar GaN. A systematic optimisation has been performed in terms of the etching depth of the silicon substrate, growth temperature and V/III ratio. Eventually, Ga melt-back etching issues have been eliminated if the GaN growth is conducted at a high temperature. Furthermore, under these optimised conditions, high quality non-polar GaN with a flat top surface has been achieved. Detailed material characterisation including SEM cross-sectional measurements, XRD rocking curve measurements and low-temperature PL measurements have been conducted. XRD measurements have confirmed that our non-polar GaN exhibits a step-change in crystal quality. Low-temperature measurements show a significant reduction in BSF density. SEM measurements show that our approach can effectively eliminate Ga melt back and that a flat surface with vertical sidewalls have been successfully obtained.

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Chapter 6

$(11\bar{2}0)$ Non-Polar GaN Stripes Based Metal Semiconductor Metal Photodetector on Si

It is increasingly interesting to develop ultra-violet (UV) photodetectors (PD) which can find a wide range of applications in flame sensors, atmospheric ozone detection, space communications, bio-photonics [1]–[4], etc. Given the direct bandgap structure of GaN with its bandgap (3.4 eV) in the ultraviolet spectral range, it is expected that GaN based UV PDs exhibit superior performance to Si based PDs in the UV region (Si has an indirect band structure and a 1.1 eV bandgap) in the UV region. However, presently used GaN, dominated by c-plane GaN, exhibits inherent polarisation which is one of the fundamental limits for the fabrication of GaN based optoelectronics leading to a photodetector with reduced performance in terms of efficiency and response speed, while non-polar GaN intrinsically exhibits zero polarisation effects due to the perpendicular direction of the piezoelectric polarisation and the spontaneous polarisation. As a result, non-polar GaN based UV PDs are expected to have no effect of QCSE and demonstrate much higher efficiency and much faster response than their c-plane counterparts. For example, it has been reported that c-plane GaN based UV photodetectors exhibit a low responsivity of 0.00567 A/W because of their inherent spontaneous polarisation [5]. While nonpolar GaN (in spite of much lower crystal quality than its c-plane counterpart) has been reported to exhibit a responsivity of 0.155 – 25.32 A/W [5]–[10].

However, the x-ray rocking curve measurements of the nonpolar GaN show a large wide full width at half maximum of around 0.5-0.6° (the typical value of standard c-plane GaN is less than 0.1°), this means that a very high density of defects in the nonpolar GaN which causes the scattering of the electrons and leads to the slower response of nonpolar PD with the rise time of 0.046-17.5 sec and the fall time of 0.075-20.5 sec compared to the value of 10 ms or 30-59 ms reported for c-plane polar GaN

[11], [12]. Clearly, there is potentially a significant scope to make major improvements in GaN based UV photodetector if the crystal quality of nonpolar GaN can be improved.

Based on the previous approach of using non-polar $(11\bar{2}0)$ GaN on (110) silicon substrates mentioned in Chapter 5, photodiode devices are fabricated on such material samples. The first section of this chapter introduces the procedure to fabricate PD devices. The measurement methods have been presented in Section 3.4. The measurements are with the help of Dr. Yuefei Cai. The results are reported in the second section of this chapter. Finally, a summary is given at the end of this chapter.

6.1 Fabrication of PD

The fabrication process of $(11\bar{2}0)$ non-polar GaN PD is straightforward and the metal-semiconductor-metal photodetector (MSM-PD) fabricated on (0001) polar GaN with the same process is also fabricated for comparison. The growth structure of (0001) GaN is slightly different from $(11\bar{2}0)$ non-polar GaN. Due to the stripe structure of the non-polar GaN sample, the cracking is limited within certain regions. However, for (0001) polar GaN sample, cracking is usually a big issue. Thus, two step-graded AlGaN layers are applied prior to GaN growth to eliminate the cracking, which has been reported by our group in [13]. With $(11\bar{2}0)$ nonpolar and (0001) polar GaN sample, two types of PD are fabricated and then measured. The main principal of PD has introduced in Section 2.4.

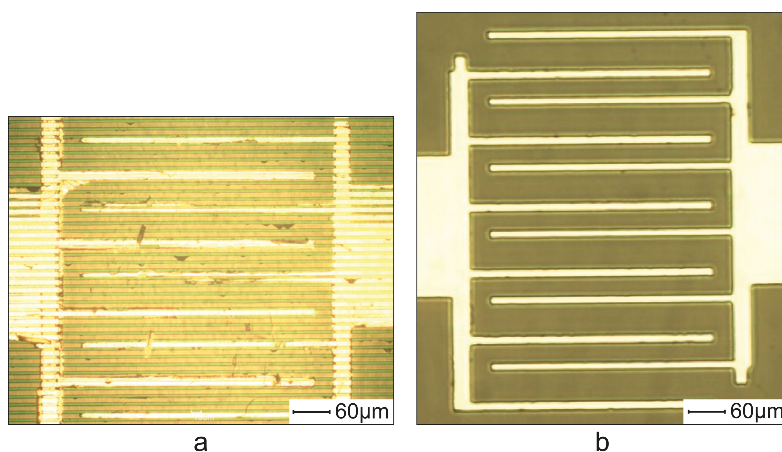

Figure 6.1: Nomarski microscope Images of (a): non-polar, (b): c-plane MSM-PD.

The fabrication methods for the two types of PDs are exactly the same, that is, forming interdigitated-finger MSM-PDs with an active area of 284×393 μm^2 on GaN surface. The interdigitated fingers have a 30 μm finger spacing and consist of titanium/aluminium/titanium/gold (Ti/Al/Ti/Au) Schottky metal stacks with thicknesses of 50/200/50/50 nm deposited by the thermal evaporator. Due to the anisotropy of mobility and carrier concentration inside the non-polar plane [7], the perpendicular design exhibits a very low photo/dark current ratio. Thus, for non-polar $(11\bar{2}0)$ GaN PD the fingers are designed parallel to the GaN stripes to achieve maximum photocurrent. The non-polar GaN in this work is unintentional doped GaN, and with this type of fabrication, the surface conduction and conduction across the trenches may both exist. Figure 6.1 shows the fabricated device of (a): non-polar $(11\bar{2}0)$ GaN MSM-PD and (b): c-plane (0001) GaN MSM-PD, respectively. The fingers shown in Figure 6.1a is fabricated on the top of the stripes. The height of stripes is around 4 μm which makes the fabrication process complicated and difficult. The sample used to fabricate photodetector is N7 mentioned in Chapter 5. The substrate of the GaN growth is n-type silicon which is conductive.

6.2 Results

The results in this section are separated into two parts: photoresponsivity results and response time results. For photoresponsivity, non-polar GaN on silicon PD is compared with a c-plane GaN on silicon PD. A benchmark is also given by comparisons with non-polar GaN on sapphire PDs from other groups. The response time of non-polar GaN on silicon PD is also compared with c-plane GaN on silicon PD as well as non-polar GaN on sapphire from other groups.

6.2.1 Photoresponsivity Results

Figure 6.2a shows the current-voltage (I-V) characteristic of our MSM-PD with an active area of 284×393 μm2 under dark and UV-illumination conditions. The inset of Figure 6.2a shows the image of our MSM-PD devices with an interdigitated finger configuration, where the finger Schottky metal contact consists of Ti/Al/Ti/Au

(50/200/50/50 nm) and the spacing between two neighbouring fingers is 30 μm. All the finger metal contacts are parallel to the stripe pattern direction. Photo-responsivity measurements have been carried out by a standard photo-response testing system. The dark current measurement results are shown in Figure 6.2a, the main reason of the dark current are silicon conduction and thermionic emission photocathode. Besides these, the dark current may also come from thermal excitation (generation) of carriers which are not necessarily directly from valence to conduction band, but possibly through defect states related to crystal defects or impurities.

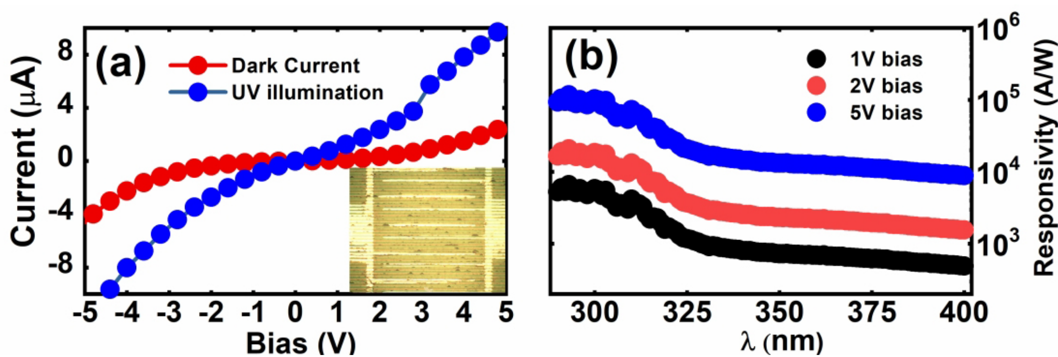

Figure 6.2: (a) Current-voltage (I-V) characteristic measured under dark and UV illumination conditions. Inset: microscope image of the non-polar GaN MSM-PD; (b) Responsivity of our non-polar GaN MSM-PD as a function of wavelength in the UV spectral region measured under different bias (1, 2 and 5 V).

Figure 6.2b shows the typical responsivity of our MSM-PDs as a function of wavelength measured under different bias (1 V, 2 V and 5 V). For details, Figure 6.2b shows that our MSM-PD exhibits a high responsivity of ~7E2 A/W under 360 nm UV illumination typically at 1V bias, which is more than 20 times higher than the current state-of-the-art. This value increases to ~2.2E3 A/W at 2 V bias and to ~1.2E4 A/W at 5 V bias, which is four orders of magnitude higher than the state-of-the-art [9]. Such a high responsivity can be attributed to the major improvement in the crystal quality of our non-polar GaN stripes, which significantly increases the mobility of the carriers and thus reduces the transit time of photogenerated carriers.

By having examined Figure 6.2b carefully, it can be found that the ratio of responsivity in the UV region to that in the blue region (below the GaN bandgap) is about 10. This

is due to the trenches between non-polar GaN stripes just covered by the AlN buffer layer directly on silicon, where the silicon within the trenches contributes to the absorption with a photon energy lower than the GaN bandgap. Especially for the void part on the stripe where the incident light directly excited on the exposed silicon substrate and AlN inside the trench. This also rules out the possibility of light absorption via point defects in the GaN layer or interface traps in the Ti/GaN Schottky junctions [14], further confirming the high quality of our non-polar GaN.

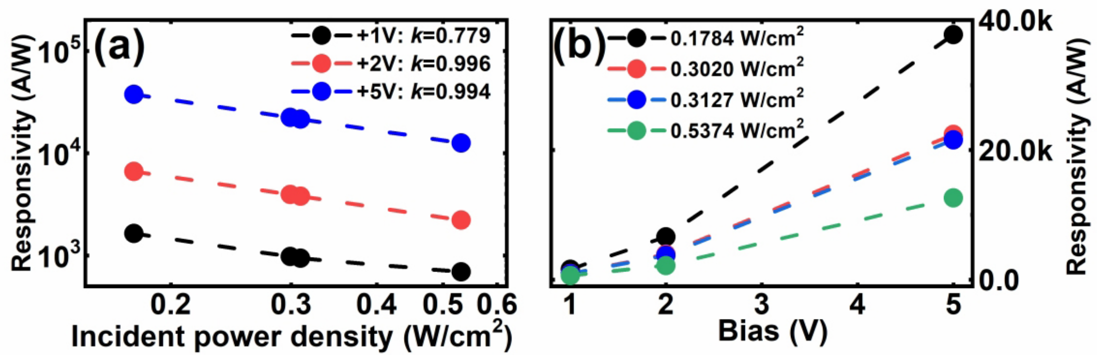

Figure 6.3: (a): Responsivity as a function of incident power density under 360 nm illumination at different bias; (b): Responsivity as a function of bias under 360 nm illumination.

Figure 6.3a presents the responsivity of our MSM-PDs as a function of incident power density under 360 nm illumination conditions measured under different bias, demonstrating that they follow the standard P^{-k} law where P is illumination irradiance, and k is an exponent in power-law which can be extracted by fitting. Here k has been obtained to be between 0.78~1, which is similar to other reports [15]. This indicates a photoconductive internal gain, explained as a modulation mechanism of the conductive volume of the layer. Photo-generated carriers are separated by potential barriers, induced as a result of dislocation-related band bending on either surface or within the bulk layer [15]. Moreover, the potential barriers also determine the carrier recombination and carrier capture, leading to an intrinsic non-exponential recovery process. Bias dependent responsivity measurements as shown in Figure 6.3b further confirm the photoconductive mechanism.

6.2.2 Response Time Results

In order to measure the response time of our MSM-PD, a commercial UV-LED serving as an UV illumination source at ~360 nm has been directly modulated by a square waveform generated by a signal generator (SG) at 1 kHz with an amplitude of 3.2 V and an offset of 2 V, while our MSM-PD has been used to detect the modulated UV light. The response time measurement system has been illustrated in Section 3.4, where our MSM-PD is biased at 5 V and a 2 kΩ load resistor (RL) is used.

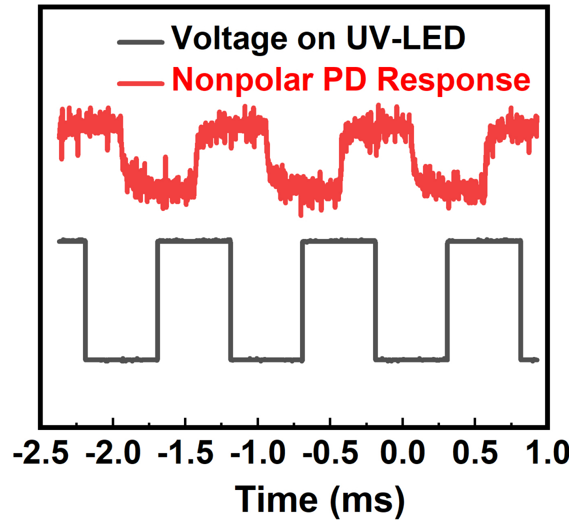

Figure 6.4: Response waveforms of non-polar PD in this work under modulated UV-LED illumination at 1 kHz.

Figure 6.4 displays both the input signal (i.e., the voltage waveform applied on UV-LED) and the response waveform of our MSM-PD. The rise and fall current can be expressed as the following equations [10]:

$$I(t) = I_{dark} + A[1 - \exp\left(-\frac{t-t_0}{t_{rise}}\right)] \quad (6.1)$$

$$I(t) = I_{dark} + A[1 - \exp\left(-\frac{t-t_0}{t_{fall}}\right)] \quad (6.2)$$

where I_{dark} is the dark current, A is scaling constant, t_0 is the time for switching on/off the UV light source. t_{rise} and t_{fall} is the rise and fall time, respectively and can be extracted by the fitting.

By fitting using a standard exponential function shown in Figure 6.5, the rise-time and the fall-time of our MSM-PDs are 66 μs and 43 μs, which are three orders of magnitude faster in comparison to the current state-of-the-art non-polar GaN PDs which are mostly in millisecond range [5]–[10]. The fast build-up and recovery time also indicates that a significant reduction in the number of shallow and deep traps in our nonpolar GaN, resulting in the shorter relaxation time [16]. This can be attributed to the step change crystal quality of our nonpolar GaN stripes. The result is close compare to the UV-LED response time which is 40.60 μs for the rise time and 42.63 μs for the fall time. The result of this work is the convolution of the LED electrical-optical modulation speed and the PD response speed, only represent the minimum performance of our PD device.

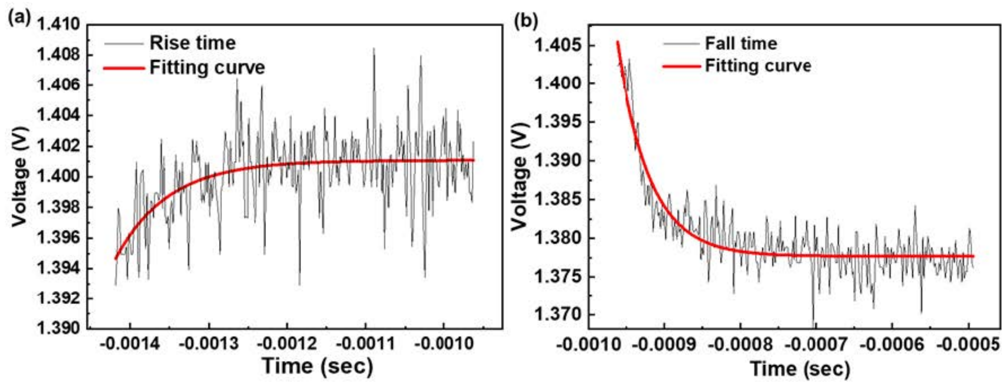

Figure 6.5: Fitting to extract (a) rise time and (b) fall time of nonpolar GaN PD in this work.

Table 6.1 shows our results benchmarked against the current state-of-the-art non-polar PDs in terms of performance, demonstrating that the crystal quality of non-polar GaN (evaluated by the FWHMs of XRD rocking curves) plays a vital role in obtaining high performance in terms of response time. For further comparison, we have also measured a typical c-plane GaN MSM-PD grown on (111) silicon, which was processed in the same batch as our non-polar GaN MSM-PD and was measured under identical conditions. The c-plane GaN MSM-PD exhibits a rise-time and a fall-time of 9 ms and 14.5 ms, respectively, which are much slower than our non-polar GaN MSM-PD and are similar to other c-plane MSM-PD results [10], [16]. This further confirms the major advantages of non-polar GaN.

Ref.	Year	Substrate	XRD Rocking Curve FWHM (arcsec)	Bias (V)	Responsivity (A/W)	Rise Time (sec)	Fall Time (sec)
This Work	2019	(110) Si	325 along [0002] 380 along $[1\bar{1}00]$	1	695.3	0.000066	0.000043
[6]	2019	r-sapphire	1908 2755 3309	1 1 1	25.243 25.32 4.42	0.257 0.222 0.163	1.99 2.1 1.2
[7]	2018	r-sapphire	2160 along [0002] 6480 along $[1\bar{1}00]$	1	1.8803	0.21	1.2
[9]	2018	$LaAlO_3$	756 along $[11\bar{2}0]$ 1476 along $[10\bar{1}1]$	5	1.35	0.046	0.075
[8]	2017	r-sapphire	1764 along $[11\bar{2}0]$	5	0.34	0.28	0.45
[5]	2015	r-sapphire	-	2	0.155	6	15
[10]	2014	m-sapphire	2336 along [0001] 3751 along $[12\bar{1}0]$	2	0.407	17.5	25

Table 6.1: Performance comparison of non-polar GaN MSM-PDs.

6.3 Summary

In conclusion, a non-polar GaN MSM-PD with superior performance has been reported, exhibiting an extremely high responsivity of ~7E2 A/W at 1 V bias and ~1.2E4 A/W at 5 V bias both under 360 nm UV illumination, which are more than 20 times higher and 4 orders of magnitude higher compared with the current state-of-the-art, respectively. The responsivity in UV region is ~10 times than that in the blue region (below the GaN bandgap). This is due to the trenches between non-polar GaN stripes just covered by the AlN buffer layer directly on silicon, where the silicon within the trenches and under the void defects on the stripes contribute to the absorption with a photon energy lower than the GaN bandgap. The rise-time and the fall-time of our MSM-PD are 66 μs and 43 μs, which are three orders of magnitude faster than those of the current state-of-the-art non-polar GaN PDs. The superior performance is attributed to previously introduced non-polar $(11\bar{2}2)$ GaN stripe arrays with a step-change in crystal quality grown on patterned (110) silicon substrates.

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Chapter 7

InGaN/GaN MQW Structure on $(11\bar{2}0)$ Non-Polar GaN Stripes on Si

Using the previous approach of high crystal quality $(11\bar{2}0)$ non-polar GaN stripes on silicon substrate described in Chapter 5, InGaN/GaN multi-quantum wells (MQWs) structure has been attempted to grow on the GaN stripes. The width of the GaN stripes is on a small scale of ~6μm in width and is tuneable by adjusting growth condition in particular the growth time. Due to the different growth rates of c-plane facet on the sidewall and non-polar facet on the top surface and with the different indium incorporation efficiencies of c-plane and non-polar InGaN, MQWs with multiple-wavelengths is obtained on a single GaN stripe. Detailed measurements by confocal photoluminescence (confocal PL) system and cathodoluminescence (CL) further confirm the multiple-wavelength emissions from the MQWs structure. This epitaxial structure has a potential application in producing multiple-colour light emitting diodes (LEDs) and micro-LED (μLED) arrays [1], etc.

The ultimate objective of multiple-wavelength MQWs on these non-polar GaN stripes is to achieve white LEDs. There are many publications on GaN based white LEDs. The latest approach is converting blue LEDs with yellow phosphor into white light sources. This approach is based on c-plane InGaN/GaN LEDs with the yellow emission provided by additional yttrium aluminium garnet phosphors which are pumped by the blue c-plane LEDs. This method is still associated with various issues, such as the heat generated from the instability of phosphors and the low efficiency due to self-absorption of phosphors [2]–[8]. With the combination of multi-wavelength features and μLED layout, our multi-wavelength LEDs on GaN stripes has a promising application in visible light communications, so called Li-Fi [9]. Many researches on phosphor free material has been reported. MQWs with different indium composition is normally applied as an active region to achieve multiple-wavelength emission [10], [11]. Several monolithic multi-colour emissions are reported [12]–[14] which are based

on the growth of three-dimensional GaN hexagonal annular structure. Another reported research done by our group is based on patterned non-polar GaN with a different structure formed on only semi-polar and non-polar facets for achieving multi-colour emissions [15]. These activities are all based on sapphire substrates. There are also limited reports of phosphor free multi-colour emissions on silicon which are based on InGaN nanowire or dot-in-a-wire [16], [17]. Compared to nanowire technology, our approach of non-polar GaN on silicon has advantages such as low cost and scalability.

This chapter first introduces the growth of the MQWs structure. This is then followed by the optical measurements, in particular, the confocal PL and cathodoluminescence (CL) measurements. The confocal PL measurement is with the help of Mr. Peter Fletcher and CL measurements are in collaboration with Dr. Jochen Bruckbauer in the University of Strathclyde. Finally, a summary is presented at the end of the chapter.

7.1 Growth of MQW Structure

The structure is epitaxial grown using the Thomas Swan MOCVD, which is mentioned in Section 3.2. The growth has four stages listed as following.

- n-GaN: this part can be grown either after the GaN overgrowth template growth or before the MQW structure epitaxy. The growth time of n-GaN layer doped with Si_2H_6 is 1300 seconds with an approximate thickness of 120nm.

- Thin GaN buffer layer: this layer is a thin GaN buffer (~10nm) with a growth time of 197 seconds. The operation condition is identical to that used for the GaN barrier of MQWs.

- InGaN/GaN MQWs: four InGaN/GaN QWs are grown on the GaN buffer. The QWs are very thin, for the top surface, the thickness is typically less than 2 nm and less than 10 nm for the barrier. The thickness on the sidewall is slightly thinner.

- p-GaN: this layer is doped with Mg with a thickness of ~150 nm.

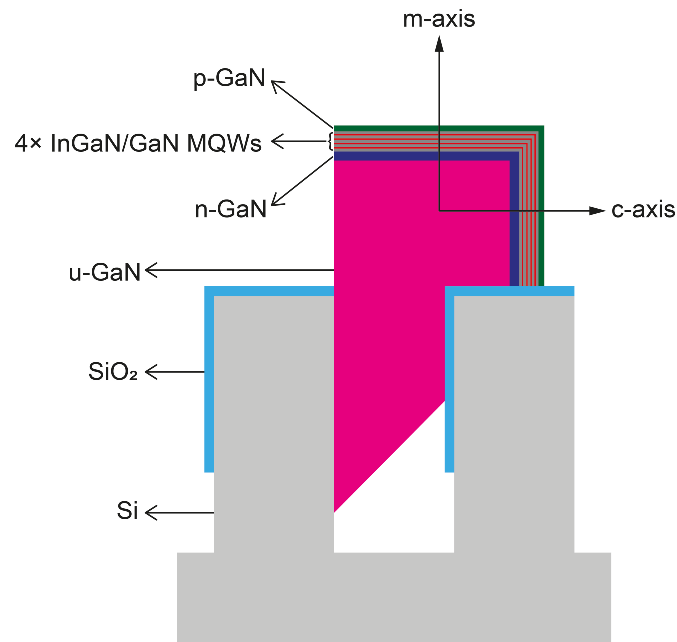

Figure 7.1: Cross-sectional schematics of InGaN/GaN MQW structure on (11$\bar{2}$0) GaN on Si.

Figure 7.1 illustrates the cross-section of InGaN/GaN the MQWs structure on (11$\bar{2}$0) GaN on silicon. The MQWs structure is established on both sidewall and the top surface of which the crystal orientations are c-plane and non-polar, respectively. The growth is confirmed by SEM cross-sectional image (Figure 7.2).

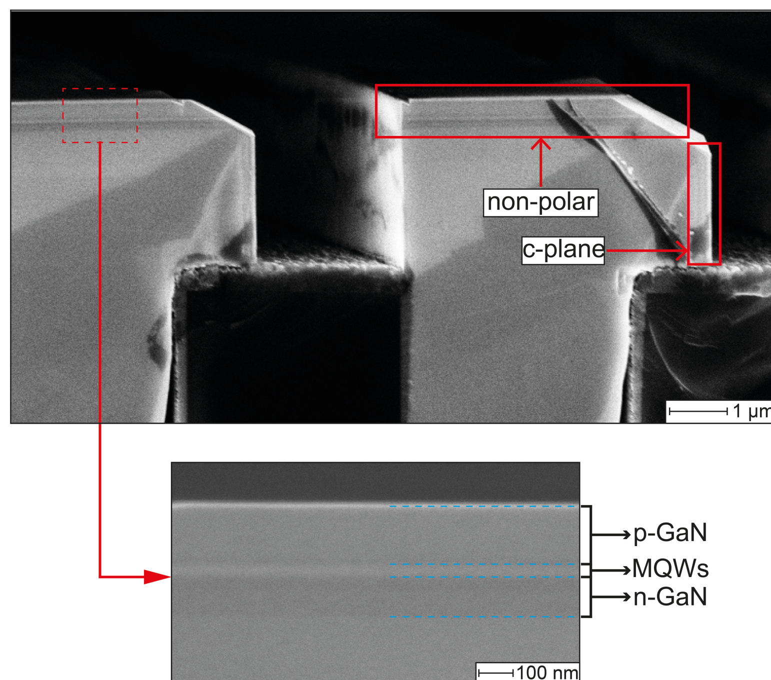

Figure 7.2: Cross-sectional SEM images of InGaN/GaN MQW structure on (11$\bar{2}$0) GaN on Si.

From the image, the MQWs are sandwiched between the n-GaN layer and the p-GaN layer. A bevelled edge at the corner of the stripe is also observed which is due to a relative high V/III ratio during the growth of the MQWs. The bevelled edge can be eliminated through reducing the V/III ratio of GaN growth condition as described in Section 5.4. The thickness of the top surface of the structure can also be evaluated through the SEM image. It is confirmed the n-GaN has a thickness of ~120 nm and p-GaN for ~150 nm. The full MQW structure has a thickness of ~50 nm, including five GaN buffers and four InGaN QWs. The structure on sidewall is slightly thinner than the top surface and difficult to measure from the SEM image.

7.2 Confocal PL Measurements

Confocal PL measurement is performed to investigate the luminescence wavelength of the different facets on the stripes due to its high resolution compared to standard PL system. The confocal PL system used in this work is WITec 300R confocal microscopy system with a Vortran Stradus 375 nm diode laser as the excitation source. The detector is a TE-cooled Andor Newton CCD. The typical measurement mode of the confocal system is mapping and integrating the intensity into an image and the corresponding emission spectrum is also provided by the system.

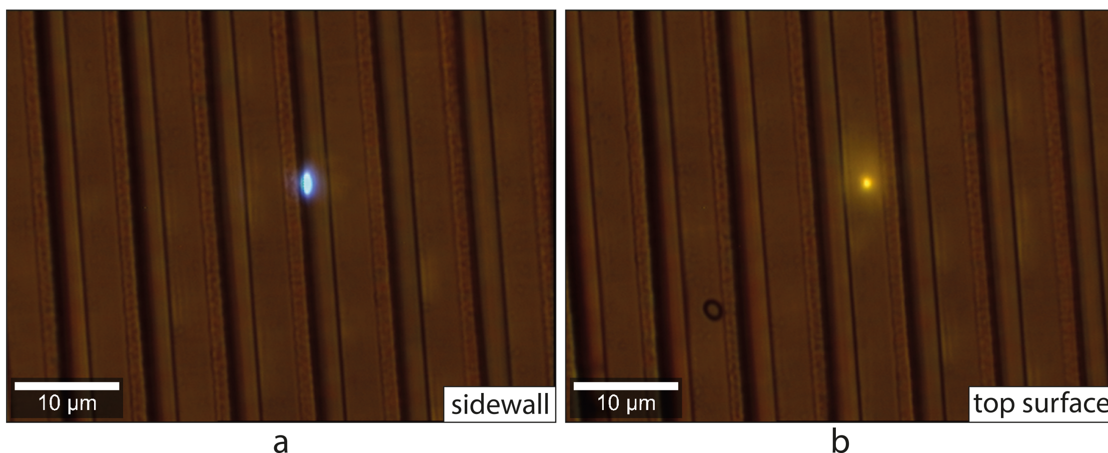

Figure 7.3: Confocal images of the emission from (a): sidewall; (b): the top surface of LED structure on $(11\bar{2}0)$ non-polar GaN stripes on Si.

The confocal PL measurement is performed under room temperature. The light spot is first illuminated on the sidewall (Figure 7.3a) and then on the top surface (Figure

7.3b). From the images, the sidewall shows a light blue colour and the top surface shows yellow due to the yellow-band emission (YBE) which comes from point defects and nitrogen vacancies. According to the figure the blue spot on the sidewall has a clear edge to the shape, which indicates that the luminescence comes from the MQWs on the surface of the sidewall; however, the yellow spot is identified with a blurred edge. The yellow-band luminescence comes from the GaN crystal. This indicates the MQWs on the top surface is not emitting or partly emitting. Hence confirms the different emitting wavelengths from the sidewall and the top surface. Wavelength mapping is then performed to determine the spectral profile.

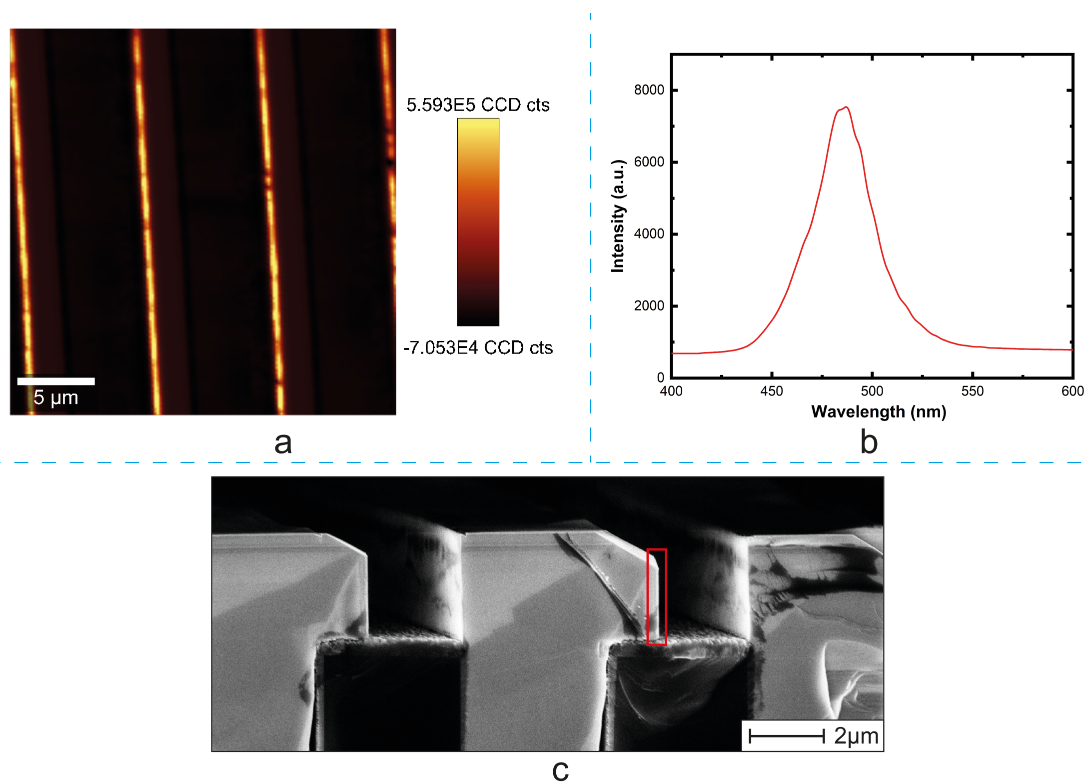

Figure 7.4: Confocal PL of non-polar GaN stripes on Si LED structure: (a) intensity mapping images with 485 nm emission; (b): emitting spectrum of sidewall; (c): cross-sectional SEM image with marked peak emission area.

The mapping is taken place with an area of 25μm×25μm. The intensity mapping with selected peak wavelength of 485 nm is presented in Figure 7.4a, the spectrum is plotted in Figure 7.4b. Figure 7.4c is the cross-sectional SEM image to point out the luminescence area marked in red. According to Figure 7.4a, the bright lines indicate that the emission comes only from the sidewall. But from the emission spectrum (Figure 7.4b), the spectral width is very wide, this is related to the nonuniform

thickness of sidewall MQWs.

The measurement is then performed on top surface and bevelled edge in order to investigate the luminescence from the two area. Figure 7.5a is the PL spectrum of the top surface and Figure 7.5b of the bevelled edge. Those regions are shown and marked as red rectangular in the cross-sectional SEM image (Figure 7.5c).

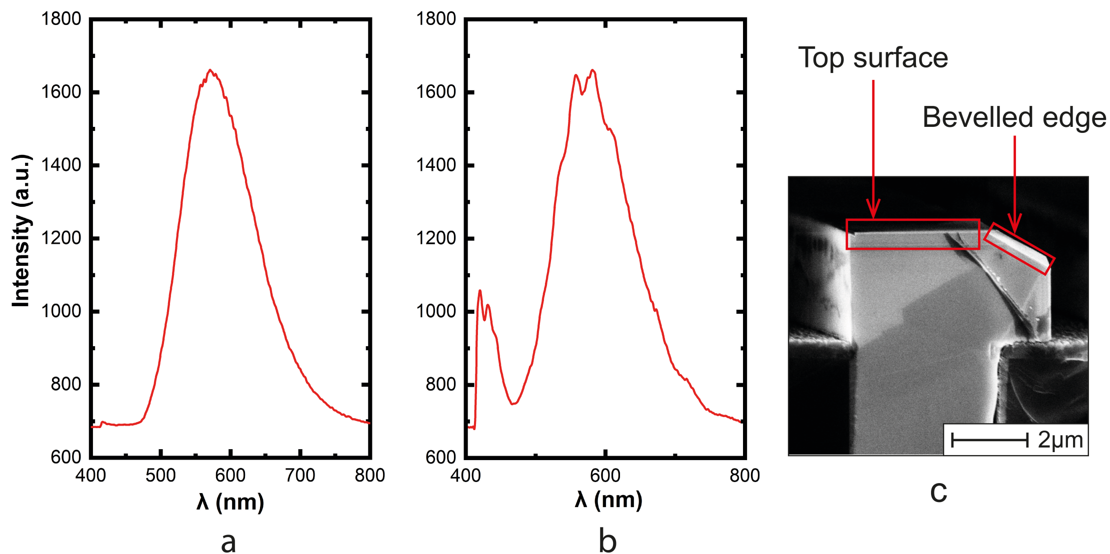

Figure 7.5: Confocal PL emitting spectra of non-polar GaN stripes on Si LED structure emitted from (a) top surface; (b): bevelled edge; (c): illustration of luminescence area on cross-sectional SEM image.

Figure 7.5a refers to only yellow-band emission on the top surface. There is no emission coming from MQWs on the top surface due to the low energy of 375 nm laser. For the bevelled edge emission spectrum in Figure 7.5b, a half-wave peak appears at the wavelength of ~410 to 450 nm. The bevelled edge does not belong to c-plane or non-polar but forms a semi-polar surface. The corresponding emission wavelength of MQWs in this region is shorter than 485 nm c-plane luminescence, and longer than top surface emission which has a wavelength of less than 400 nm. In order to further understand the wavelengths of our MQWs structure on different facets, CL measurements are performed through cross-sectional CL hyperspectral imaging [18].

7.3 CL Results

The CL hyperspectral image presents a full CL spectrum towards each pixel in an image [19]. To record the luminescence from the MQWs on different facets, cross-sectional CL hyperspectral image is performed.

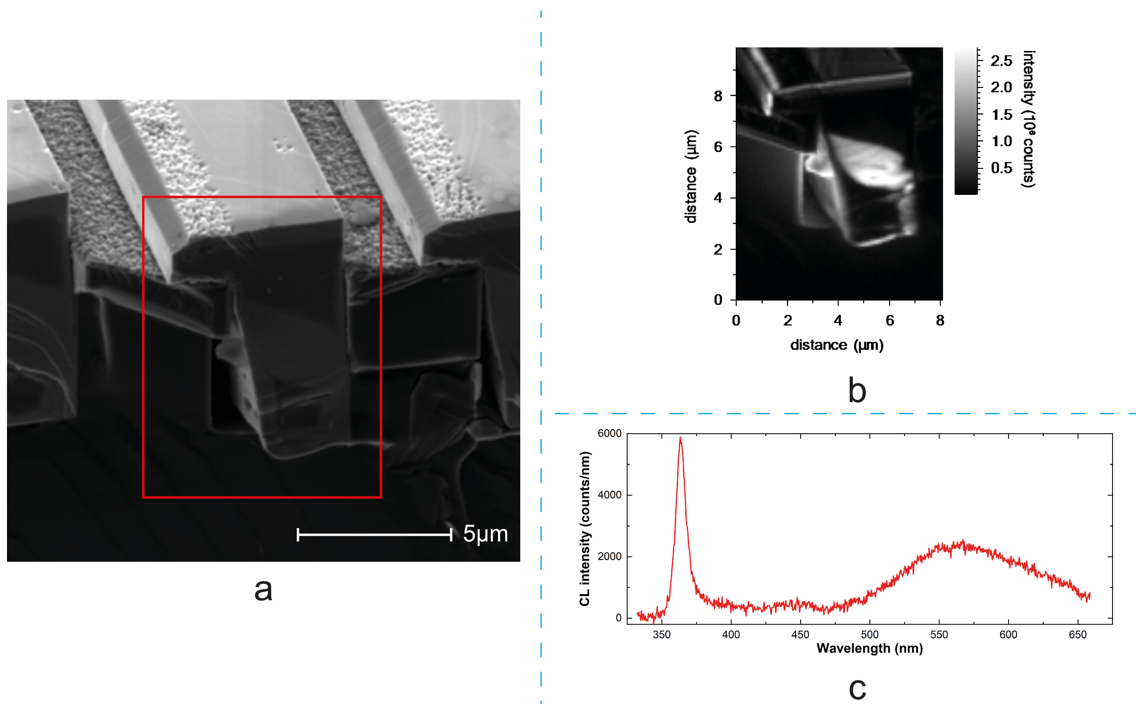

Figure 7.6: Non-polar (11$\bar{2}$0) GaN stripes on Si LED structure: (a): SEM images with marked CL measurement area; (b): panchromatic CL hyperspectral image; (c): CL mean spectrum.

Figure 7.6a is the SEM image of the measurement area; the CL measurement area is marked in red rectangular. The panchromatic CL hyperspectral image is presented in Figure 7.6b. The mean CL spectrum is provided in Figure 7.6c. From this result, it follows that the spectrum is dominated by GaN near band emission and yellow-band emission. Some unclear peaks are shown at the wavelength of 360 nm to 475 nm which contribute from sidewall MQWs, top MQWs and defects.

From the CL image is shown in Figure 7.7a and the spectrum plotted in Figure 7.7b. The luminescence from the MQWs on sidewall is established to be at with a wavelength of ~450nm. The pixels used for the spectrum are (13, 24) to (14, 25). The spectrum shows a clear peak around 450 nm. This refers to the c-plane MQWs on the sidewall. The yellow-band emission (YBE) is also observed but with a relatively lower

intensity. Thus, the sidewall MQWs is confirmed to be emitting at a wavelength of ~450 nm.

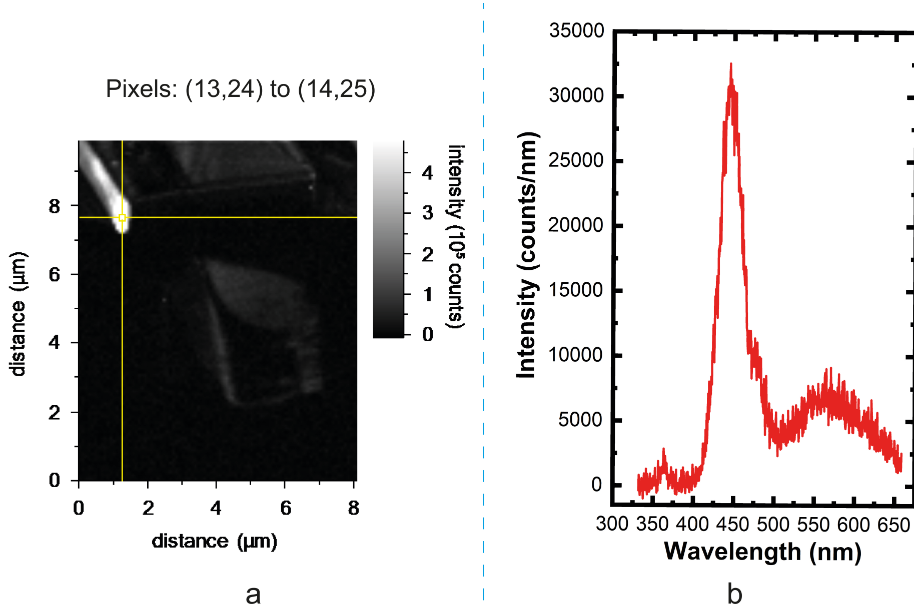

Figure 7.7: Integrated CL (a): hyperspectral images with wavelength of 420-480 nm; (b): spectrum of pixels: (13, 24) to (14, 25).

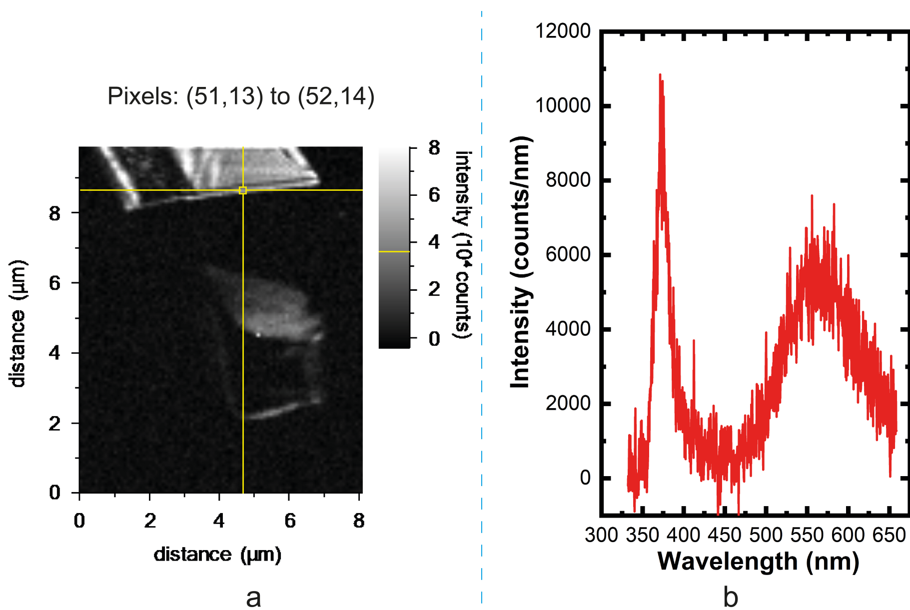

Figure 7.8: Integrated CL (a): hyperspectral images with wavelength of 380-390 nm; (b): spectrum of pixels: (51, 13) to (52, 14).

The integrated hyperspectral image is then taken place at the wavelength from 380 nm to 390 nm. The image is presented in Figure 7.8a. In this image, the area of the pixels performed with the spectrum recording is the from (51, 13) to (52, 14). The

spectrum is shown in Figure 7.8b which indicates the non-polar MQWs on the top surface has a wavelength of ~375 nm. This UV wavelength cannot be excited by 375 nm laser. The result matches the spectra from confocal PL measurement.

To further confirm the luminescence from the top surface, top view CL hyperspectral images are performed. Figure 7.9a is the SEM image of the scanning area. Figure 7.9b is the mapping of integrated wavelength from 370nm to 380nm. The bright region covers the whole top surface and indicates the luminescence of the MQW on top surface emitting at a wavelength of ~375 nm.

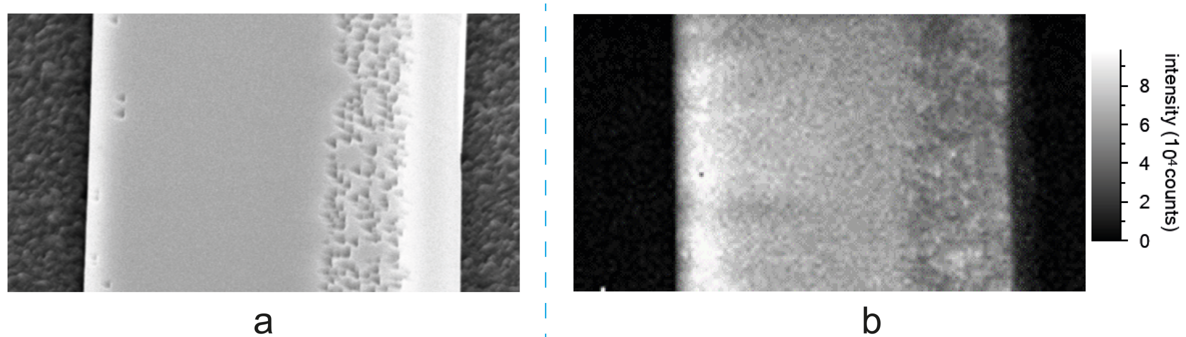

Figure 7.9: Top view (a): SEM image; (b): Integrated CL hyperspectral images with wavelength of 370-390 nm.

7.4 Summary

A MQW structure with multiple wavelengths is grown on the high crystal quality $(11\bar{2}0)$ non-polar GaN stripes on silicon substrate. The emission wavelength of the MQWs on the top surface is ~375 nm UV and ~450 nm for the sidewall. Thus, multi-wavelength emission is achieved in this MQWs structure. Judging from the SEM cross-sectional image, the thickness of the top surface is much larger compared to the sidewall. The emission wavelength of thicker MQWs should be longer than thinner one under same indium content [20]. Under same growth condition, c-plane InGaN/GaN MQWs has a longer wavelength than non-polar counterparts which indicates the lower indium incorporation coefficient of non-polar InGaN [21], [22]. In this work, it shows a much larger variation (75 nm) than that reported in reference [21], [22] (25 nm to 50 nm). This further confirms the non-polar InGaN has a much lower indium incorporation

efficiency than the c-plane InGaN under same growth condition. Lower indium incorporation efficiency leads to lower indium content and finally results in shorter emission wavelength. With the modification of the growth condition of MQWs, the tuneable wavelength of this structure is promisingly achievable.

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Chapter 8

Exploring an Approach toward the Intrinsic Limits of GaN Electronics

Previously, our group has researched on the AlN buffer layer [1]. With this technology, GaN crystal is grown on the AlN buffer and achieved high crystal quality GaN. Such high crystal quality GaN is an ideal material for electronic device. Based on this successfully grown high quality GaN, high-electron-mobility transistor with a record breakdown field is then fabricated. The measurement and fabrication of high-electron-mobility transistors (HEMT) are with the help of Dr. Sheng Jiang.

8.1 Introduction

Intrinsic GaN with inherent polarisation on c-plane substrates is supposed to exhibit superior electrical properties to almost all of the other existing semiconductors, such as high electron mobility and a very high sheet carrier density of two-dimensional electron gas (2DEG) formed in an AlGaN/GaN heterostructure but without using any modulation doping [2], [3] and high breakdown voltage (with the theoretical value of the critical electrical field of ~3MV/cm) [4], [5]. Due to its wide bandgap, intrinsic GaN is supposed to be at least semi-insulating. Despite significant progress obtained in the last two decades, the performance of GaN electronic devices is far from the limits of this material, which we believe is due to the challenges in material growth. Therefore, it is crucial to understand the fundamental issues from the perspective of epitaxial growth and then to explore a new approach toward these theoretical limits.

Currently, a standard growth approach for GaN grown on sapphire is based on the classic two-step method developed by three 2014 Nobel Prize Laureates Akasaki, Amano, and Nakamura by using metal-organic vapour-phase epitaxy (MOVPE) techniques; namely, a thin GaN or AlN nucleation layer is initially prepared at a low temperature (LT) followed by a thick GaN buffer layer grown at a high temperature prior to the growth of any further device structures. In terms of growth modes, this

approach is based on the initial formation of small islands on a nanometre scale evolved from the LT nucleation layer due to a subsequent annealing process followed by a gradual coalescence process to finally obtain a flat surface (i.e., initially a three-dimensional (3D) growth mode and then a 2D growth mode). This two-step growth approach has resulted in major improvement in the crystal quality of GaN in the last two decades, leading to unprecedented success in the field of III-nitride optoelectronics. However, this growth approach poses a great challenge in obtaining a semi-insulating GaN buffer layer, which is crucial for the growth of GaN electronics [6]–[8]. The GaN buffer grown by using the two-step method exhibits severe current leakage as a result of its low resistivity. In order to address this issue, a carbon-doped (C-doped) GaN buffer approach still based on the two-step method has been widely adopted for the growth of AlGaN/GaN-based high-electron-mobility transistors (HEMTs) as C-doped GaN, which can be obtained by growing nominally undoped GaN at a low temperature, has been proven to be efficient to suppress a buffer leakage based on a compensation mechanism [9], [10]. In detail, carbon, act as deep level acceptors, compensate structure defects such as nitrogen vacancies in the buffer region to increase the buffer resistivity. Despite the improvement in off-state buffer leakage, the best report on the critical electric field for a single C-doped buffer layer (not an HEMT structure) is limited to 2 MV/cm [9]. It is worth further highlighting that a C-doped buffer layer needs to be far from the 2DEG channel of an HEMT in order to prevent the high concentration of acceptors induced by C-doping from diffusing into the 2DEG channel (otherwise, this leads to a significant reduction in sheet carrier density) [10], [11]. As a result, an undoped GaN layer prepared at a high temperature (which can significantly reduce or eliminate C-doping) is generally required prior to the growth of the AlGaN barrier of an HEMT structure [10]. Of course, an increase in the undoped GaN layer thickness is more effective for stopping carbon diffusion while also enhancing the risk of a buffer leakage. Therefore, a compromise between buffer leakage and the thickness of the undoped GaN layer has to be made [10], [11]. Consequently, the critical electric field of a full HEMT structure using the C-doped buffer approach is limited to 1.5 MV/cm, which is far below the theoretical limit of GaN (3MV/cm) [12], [13].

Only a few reports, which have reported a higher breakdown field of GaN than 1.5 MV/cm, are limited to a p–n junction (in a vertical architecture) grown on extremely expensive bulk GaN substrates [13]–[18], which do not reflect the intrinsic properties of GaN due to the utilisation of a p–n junction. In addition, the breakdown field is calculated depending on the accuracy of the p-doping level used in a p–n junction, and furthermore, the major advantage of the 2DEG formed as a result of the inherent polarisation cannot be exploited for such a vertical architecture. Therefore, it is crucial to explore a new growth approach to fully exploit the upper limits of intrinsic GaN for widely used lateral devices where the 2DEG formed as a result of the inherent polarisation can be fully exploited.

In this study, we have explored an approach toward the limit of GaN materials by means of using our high-temperature AlN buffer, which was originally designed for the growth of novel III-nitride optoelectronics [19]–[23] instead of the classic two-step growth method, where a 2D growth mode is employed throughout the whole growth processes. A record breakdown field of 2.5 MV/cm has been demonstrated. Furthermore, high-voltage AlGaN/GaN HEMTs with an extremely low off-state buffer leakage current of down to 1 nA/mm at up to 1000 V have been obtained. The outcome is also applicable to non-polar HEMTs where no polarisation effect presents in the structure and 2DEG is induced through extrinsic doping normally in the AlGaN barrier.

8.2 Experimental Section

8.2.1 MOCVD Epitaxial Layer Growth on c-Plane Sapphire

Sample A was prepared using the classic two-step approach by a low pressure MOVPE system, namely, after an initially high temperature annealing process under ambient H_2, a 25-nm-thick GaN nucleation layer was grown at a low temperature of 550° C, followed by the growth of a 1.5 μm GaN buffer layer, and then a 1 nm AlN spacer and finally a 25 nm AlGaN barrier (20% Al composition) all grown at 1110 °C, respectively. Samples B to E were grown by using our high-temperature AlN buffer approach; namely, ammonia (NH_3) pre-flow was then conducted on sapphire for nitration after the substrate was initially subjected to a high-temperature annealing

process under ambient H_2. A 500 nm AlN buffer layer was subsequently grown at 1180 °C followed by the growth of a 1.5 µm GaN buffer layer, then a 1 nm AlN spacer, and finally a 25 nm AlGaN barrier (20% Al composition) all grown at 1110 °C, respectively. The details of the growth conditions are given in Table 8.1.

Sample	Buffer	Temperature (°C)	Pressure (Torr)	NH_3 (sccm)	TMGa (sccm)	TMAl (sccm)
B	GaN	1100	225	5840	65	-
	HT-AlN	1180	65	300	-	180
C	GaN	1110	225	5840	65	-
	HT-AlN	1180	65	300	-	180
D	GaN	1120	175	5840	65	-
	HT-AlN	1180	65	200	-	180
E	GaN	1130	175	5840	65	-
	HT-AlN	1180	65	150	-	180

Table 8.1: summary of growth parameters for Sample B – E up to GaN buffer layer.

Hall measurements were conducted on all the samples, showing a similar sheet carrier concentration of around 9×10^{12} cm^{-2} with an electron mobility around 1300 cm^2 V^{-1} s^{-1}, while single GaN cannot achieve such a high carrier concentration and such a high mobility.

8.2.2 Fabrication of AlGaN/GaN HEMTs

A mesa isolation was first performed using Cl_2-based inductively coupled plasma (ICP) dry etching with an etch depth of 350 nm. A Ti/Al/Ni/Au alloy (20/120/20/45 nm) was then deposited using a standard thermal evaporator followed by a rapid thermal annealing process at 775 °C for 1 min in order to form ohmic contacts for source and drain electrodes. A contact resistance of 1 Ω·mm was obtained by using a transmission line measurement. A Ni/Au alloy (20 nm/200 nm) was then deposited to form Schottky contact serving as a gate electrode. Finally, bond pad metal was deposited using Ni/Au (20 nm/200 nm) for electrical characterisation.

8.2.3 Breakdown Measurement

Two isolated ohmic pads with a gap spacing of 3 μm were used to test a breakdown. A 1000 V Keithley 2410 source measure unit (SMU) was used to supply a bias between the two ohmic pads and then monitor leakage current. The bias increased from 0 V with a 5 V step size until a catastrophic breakdown occurred in device under test (DUT). The breakdown voltage was recorded and was converted to an electric field over the 3 μm gap spacing. Four terminal breakdown measurements were performed to characterise an off-state leakage current for our HEMTs. A 1000 V Keithley 2410 SMU was connected to the drain electrode of the DUT to sweep the bias from 0 to 1000 V with a 5 V step size. The gate was pinched off at V_{GS} = −5 V using a 40 V Keithley 2602b SMU. Two Keithley 2410 and Keithley 2602b SMUs were used as ampere meters and were connected to the source and the substrate electrodes. The currents flowing through the drain, the source, the gate, and the substrate electrodes were monitored individually via the corresponding SMUs.

8.3 Results and Discussion

In order to maintain a 2D growth method and also to minimise auto carbon-doping in GaN (generally occurs at a low temperature [8]), high temperatures for both the growth of the thick AlN buffer (at 1180 °C) and the subsequent growth of a GaN buffer layer, then an AlN spacer, and finally an AlGaN barrier (all at 1110 °C) are utilised. Furthermore, a low V/III ratio needs to be carefully optimised in order to facilitate a 2D growth mode throughout the whole growth processes. AlGaN/GaN HEMTs with a depletion mode (D-mode) have been fabricated in order to characterise the electrical performance of the GaN buffer. Figure 8.1 shows the schematics of a standard HEMT structure, typically consisting of a 25 nm $Al_{0.20}Ga_{0.80}N$ barrier and a 1 nm AlN spacer in addition to the GaN buffer layer and the AlN buffer layer. The HEMT device was fabricated with a gate width of 100 μm, a gate length of 1.5 μm, a gate-drain separation (L_{GD}) of 9 μm, and a source-drain separation of 13 μm. The larger L_{GD} implemented than the source-drain separation is to withstand high drain voltages. In order to test the intrinsic properties of our GaN buffer, we did not use any passivation

or any field plates for the fabrication of the HEMTs.

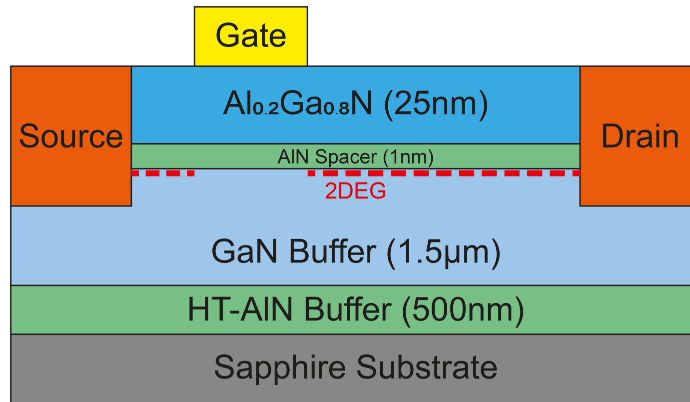

Figure 8.1: Schematics of our AlGaN/GaN HEMT structure.

In order to examine the maximal critical electric field of our samples, two isolated ohmic contacts with a 3 µm gap spacing have been fabricated where standard Ti/Al alloys are used for the ohmic contacts. The inset of Figure 8.2 schematically illustrates our setup for our buffer leakage measurements.

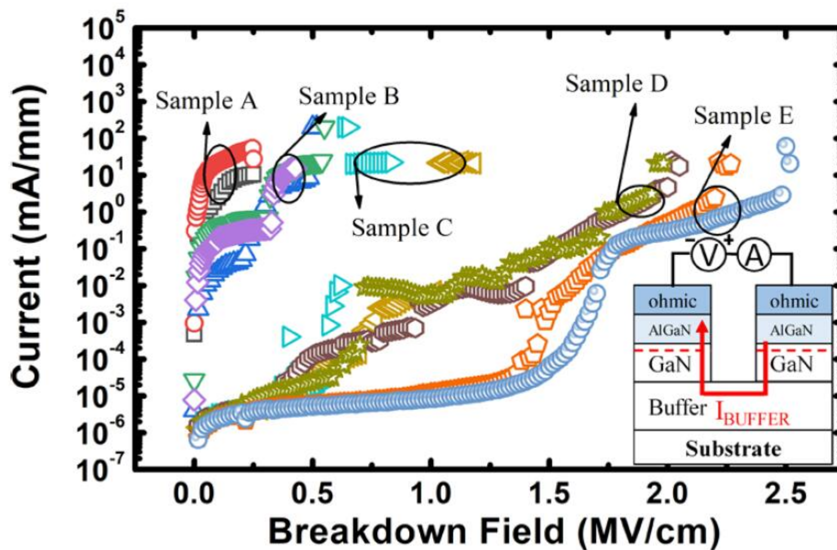

Figure 8.2: Data for the breakdown field measurements for all samples where sample E shows an extremely high breakdown field of 2.5 MV/cm. Inset: schematic of our test setup for buffer leakage measurements.

A bias, which is applied between the two ohmic contacts, increases until a breakdown takes place, where breakdown is defined as when the leakage current exceeds 20 mA/mm. Figure 8.2 shows the breakdown field results of all the samples. Two separate groups (samples A to C and samples D and E) have been identified. For

sample A and samples B and C, the breakdown takes place at a bias of <300 V, meaning low breakdown fields of 0.25, 0.5, and 1 MV/cm, respectively.

In remarkable contrast, samples D and E demonstrate a high breakdown field over 2 MV/cm, in particular sample E, which exhibits an extremely low buffer leakage of <1 μA/mm at up to 1.65 MV/cm and a breakdown voltage of 750 V that is equivalent to an extremely high breakdown field of 2.5 MV/cm. This value approaches the theoretical limit of GaN, which is more than 1.5 times the upper limit of any existing GaN buffers including C-doped GaN buffers.

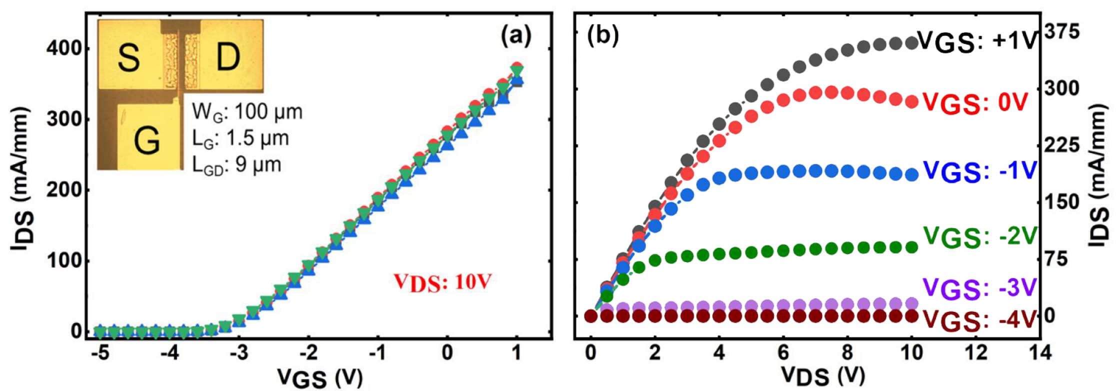

Figure 8.3: (a) Gate transfer characteristics (DC) of the devices fabricated on sample E; inset; optical image of the fabricated AlGaN/GaN HEMT; (b) I–V characteristics (DC) of the fabricated device.

Figure 8.3a shows the gate transfer characteristics of our AlGaN/GaN HEMTs fabricated on sample E as shown in the inset of Figure 8.3a. An output current of 370 mA/mm has been obtained at V_{GS} = 1 V with a threshold voltage of around −3.5 V. Figure 8.3b shows a typical I–V characteristic, exhibiting an on-state resistance (R_{on}) of 13 Ω·mm, which is equivalent to 1.95 mΩ·cm^2, considering the active region of a 1 μm transfer length from both source and drain electrodes. Four terminal breakdown measurements as illustrated in the inset of Figure 8.4a have been conducted to measure the buffer leakage of the devices. The gate is pinched off at V_{GS} = −5 V, while the drain is swept from 0 to 1000 V, the upper limit of the bias of our setup. The currents through the drain (I_{total}), source (I_{buffer}), gate (I_{gate}), and substrate (I_{sub}) electrodes have all been monitored, while only I_{total} and I_{buffer} have been shown for simplicity.

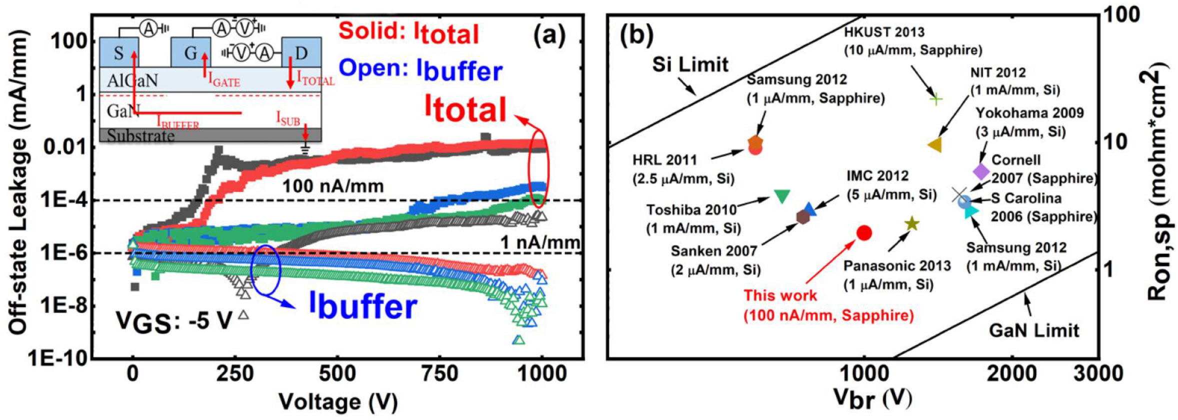

Figure 8.4: (a) four terminal breakdown results measured at V_{GS} = −5 V and V_{DS} of up to 1000 V with monitoring current through drain (I_{total}), source (I_{source}), gate (I_{gate}), and substrate (I_{sub}) (only I_{total} and I_{buffer} are shown); inset: schematic of our terminal breakdown measurement setup; (b) benchmarking our devices against the state-of-the-art by comparing their figures-of-merit (V_{br}^2/ $_{on,sp}$).

Figure 8.4a demonstrates that an extremely low off-state buffer leakage of <1 nA/mm at up to 1000 V has been achieved. The total leakage current is dominated by I_{gate} as a result of our highly resistive GaN buffer layer. Despite slight variation in I_{total}, an excellent off-state leakage current of 100 nA/mm has been achieved at 1000 V for the device with an L_{GD} of 9 µm without any field plates. Figure 8.4b shows that our device demonstrates an excellent figure-of-merit ($V_{br}^2/R_{on,sp}$) of 5.13 × 10^8 $V^2/\Omega\cdot cm^2$ compared to existing AlGaN/GaN HEMTs [25]–[36].

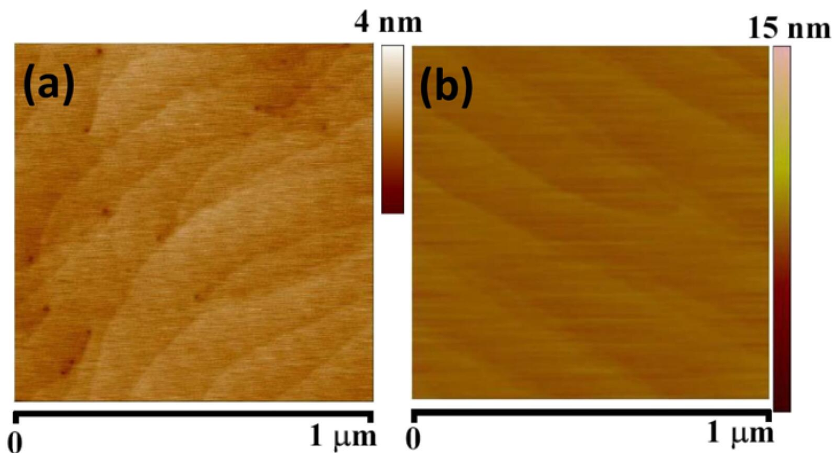

Figure 8.5: Typical AFM images of the GaN layer grown (a): using the classic two-step growth method and (b): on our HT-AlN buffer.

Further material characterisation has been conducted on samples D and E in order to explore the fundamental physics behind the extremely high breakdown voltage and

the extremely low leakage current. Figure 8.5a and 8.5b shows the atomic force microscopy (AFM) images of a standard GaN layer grown using the classic two-step growth method and the GaN layer grown on our high-temperature (HT) AlN buffer in a scanning area of 1 × 1 μm^2, respectively. Figure 8.5a shows that the standard GaN grown by using the classic two-step method typically exhibits a number of dark spots due to the termination of screw dislocations, which can be widely observed as a replica of GaN coalescence on GaN nano-islands formed from the thin LT nucleation layer due to the annealing processes mentioned above [36]. In remarkable contrast, Figure 8.5b shows the typical AFM image of the GaN grown on our HT-AlN that exhibits features with parallel and straight terraces without any dark spots, demonstrating a step-flow growth mode, that is, a typical 2D layer-by-layer growth mode, which is different from the classic two-step growth [20]–[23], [36].

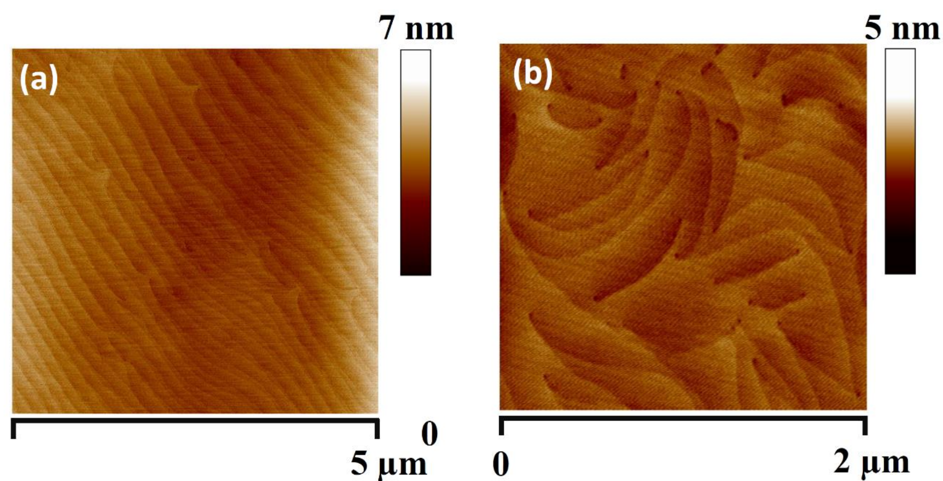

Figure 8.6: The AFM images of (a): the standard GaN and (b): the GaN on HT-AlN in a larger scanning area.

The AFM images with a larger scanning area are provided in Figure 8.6. Figure 8.6a exhibits features with parallel and straight terraces but without any dark spots, indicating a typical 2D layer-by-layer growth mode, while Figure 8.6b is a typical AFM image for standard GaN, showing spiral features with dark spots due to screw dislocations as a result of 3D growth. Detailed RMS data show an RMS value of 0.35 nm for the GaN on HT-AlN, and an RMS value of 0.47 nm for the standard GaN.

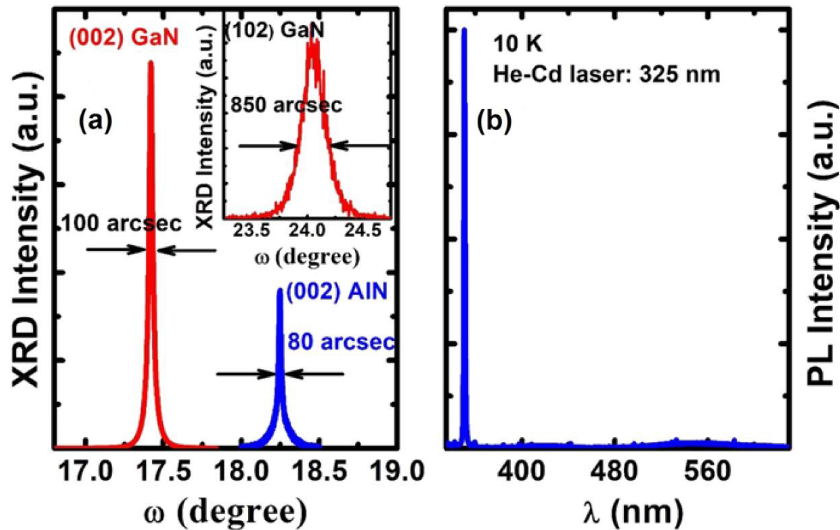

Figure 8.7: (a): XRD rocking curves of the GaN grown on our HT-AlN buffer and the HT-AlN buffer itself both along the (002) direction; inset: XRD rocking curve of the GaN grown on our HT-AlN buffer; (b): PL spectra of the GaN grown on our HT-AlN buffer, measured at 18 K using a 325 nm He-Cd laser as an excitation source.

These results are consistent with the X-ray diffraction (XRD) measurements performed along the (002) direction as shown in Figure 8.7a. The GaN on our HT-AlN buffer exhibits a narrow full width at half-maximum (FWHM) of the XRD rocking curve, ~100 arcsec, and the FWHM of the (0002) XRD rocking curve of our HT-AlN buffer itself is only 80 arcsec as we reported previously [20]–[23]. The much narrower FWHM indicates a very low screw dislocation density, which has also been confirmed by our transmission electron microscopy measurements [20]. Note that the typical FWHM of the (0002) XRD rocking curve of standard GaN grown by the two-step method is around 250−300 arcsec [36]. In order to maintain a 2D growth mode, it is necessary to grow an AlN buffer layer at a very high temperature and a very low V/III ratio under a low pressure [20]–[23]. The subsequent GaN buffer growth also needs to follow a similar trend with a high growth rate. An increased V/III ratio and a reduced growth temperature will lead to a deviation from a 2D growth mode, such as sample B and C.

Generally speaking, it has been predicted that the electrical properties of GaN are strongly affected by threading dislocations, namely, screw and edge dislocations[37], [38]. For example, screw dislocations generally generate current leakage paths. Therefore, it is crucial to significantly reduce the density of screw dislocations in

order to minimise leakage current in GaN [37], [38]. Edge dislocations are likely to accommodate any unintentional acceptor impurities. As a result, edge dislocations with a reasonably high density can effectively suppress leakage current [38]. The GaN grown on our HT-AlN in a 2D growth mode aligns with the two requirements. Although the FWHM of the XRD rocking curves of either the GaN or the AlN along the (002) direction is very narrow, meaning a very low screw dislocation density, the FWHM of the XRD rocking curve along the (102) direction is 850 arcsec for samples D and E as shown in the inset of Figure 8.7a, which is much broader than that of the standard GaN grown using the classic two-step growth method (typically ~300 arcsec). This means that our GaN exhibits a fairly high density of edge dislocations.

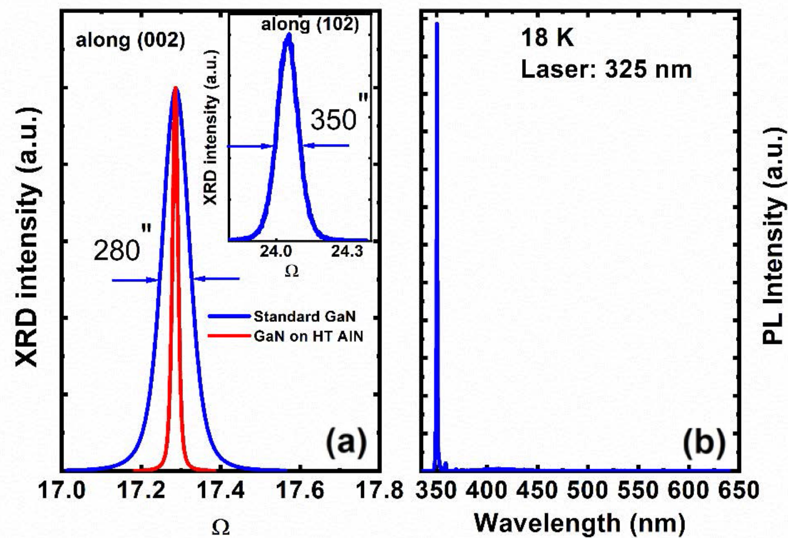

Figure 8.8: (a): Detailed XRD rocking curves of the standard GaN measured along the (002) and the (102) directions; (b): PL spectrum of the standard GaN measured at 18 K.

Figure 8.8a shows the XRD rocking curve of the standard GaN measured along the (002) direction, showing the full width half maximum (FWHM) is around 280 arcsec, which is often observed (the XRD rocking curve of the GaN on our HT-AlN buffer with a FWHM of 100 arc sec was also included as a reference). The Inset shows the XRD rocking curve of the standard GaN measured along the (102) direction, showing a FWHM of 350 arc sec, which is also often observed. Therefore, our results agree with the theoretical studies [7], [11], [37], [38], confirming the influence of threading dislocations on the electrical properties of GaN.

Further material characterisation includes low-temperature photoluminescence (PL) measurements performed at 18 K. C-doped GaN typically exhibits a much stronger yellow band emission centred at 550 nm due to carbon doping induced deep levels [7], [11]. In contrast, Figure 8.7b shows the PL spectrum of sample E, which exhibits a strong GaN band edge emission at 357 nm with a negligible yellow band emission at 550 nm. Figure 8.8b shows the photoluminescence (PL) spectra of the standard GaN measured at 18k using a 325 nm He-Cd laser, exhibiting a strong GaN band edge emission at 357 nm without any yellow band emission at 550 nm. This means that negligible auto carbon doping was generated during the epitaxial growth processes of our GaN at a high temperature. The conclusion agrees with the fact that a high growth temperature (>1100 °C) leads to a remarkable limit in carbon incorporation into GaN as a result of the increased availability of absorbed hydrogen [8]. The device structure we used in this study is based on the simplest D-mode AlGaN/GaN HEMT without any gate field plate or source field plate. As a result, the device is suitable for evaluating the buffer resistivity but is not optimised for its dynamic performance. Therefore, we did not conduct any dynamic or speed measurements of the device.

8.4 Conclusion

In conclusion, we have reported a record breakdown field of 2.5 MV/cm on our HEMTs grown using the undoped GaN buffer layer on our HT-AlN buffer technology on sapphire, which approaches the theoretical limit of GaN and is >1.5 times that of any existing GaN buffers including C-doped buffers. Our fabricated AlGaN/GaN HEMTs with an L_{GD} of 9 μm have demonstrated a negligible buffer leakage of 1 nA/mm at 1000 V and an excellent figure-of-merit ($V_{br}^2/R_{on,sp}$) of 5.13×10^8 $V^2/\Omega \cdot cm^2$. We believe that a 2D growth method, which benefits from our HT-AlN buffer technology, makes a major contribution to the extremely high breakdown field and the extremely low leakage current. The presented results also imply that it is possible to achieve the intrinsic limits of GaN electronics by further exploring epitaxial growth on large lattice-mismatched and industry compatible substrates.

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Chapter 9

Conclusion

This thesis represents the research of growth and characterisation of high crystal quality $(11\bar{2}0)$ non-polar GaN stripes on patterned (110) silicon substrates as required for relevant device structures.

In order to perform non-polar growth on silicon substrates, the patterning of (110) silicon substrates is necessary. The pattern is achieved by following the steps: SiO_2 mask deposition by PECVD; pattern formation through normal photolithography; window opening by RIE dry etching; silicon wet etching with KOH solution and, finally, SiO_2 mask removal by HF wet etching. With the achievement of high performance AlN buffer layer, a two-step growth approach is then performed to eliminate melt-back etching. Furthermore, the crystal quality is improved with significantly reduced dislocation density and basal stacking faults (BSFs) density. Between the two epitaxy steps, an angular e-beam deposition is applied to achieve selective growth on one of the facets of silicon pattern which finally forms $(11\bar{2}0)$ non-polar GaN. This method shows good performances on both uniformity and reproducibility.

An interdigitated finger MSM UV PD is then fabricated on our nonpolar GaN material and shows the superior performance of high responsivity and fast response speed. The results show a high responsivity of ~7E2 A/W at 1 V bias and ~1.2E4 A/W at 5 V bias both under 360 nm UV illumination and a fast response with a rise time of 66 μs and a fall time of 43 μs which are much better compared to other reported results. Thus, this non-polar GaN on silicon is serving as an excellent candidate for UV light detection application.

MQW structure is also grown on our non-polar GaN stripes to achieve multiple wavelengths light emission. The multi-wavelength with 375 nm UV on the top surface and 450 nm blue on sidewall has been confirmed by CL hyperspectral image mapping. With the SEM image, the thickness of the MQW on the top surface is confirmed to be

thicker than those at the sidewall, while the top surface emission has a much shorter wavelength than sidewall emission. The results indicate non-polar InGaN has a lower indium incorporation efficiency than c-plane InGaN.

The HT-AlN buffer technique is also applied in the growth of GaN electronics on c-plane sapphire in order to explore a new approach toward the intrinsic limits of GaN electronics from the perspective of epitaxial growth. The demonstration has an extremely high breakdown field of 2.5 MV/cm approaching the theoretical limit of GaN and an extremely low off-state buffer leakage of 1 nA/mm at a bias of up to 1000 V. Furthermore, our HEMTs also exhibit an excellent figure-of-merit ($V_{br}^2/R_{on,sp}$) of 5.13 × 10^8 $V^2/\Omega \cdot cm^2$. We believe that a 2D growth method, which benefits from our HT-AlN buffer technology, makes a major contribution to the extremely high breakdown field and the extremely low leakage current.

Future Work

The pattern geometry of silicon substrates can be further optimised in order to fabricate patterned templates with a large ratio of wing width to window opening width for further GaN growth, which allows us to achieve better understanding of such a selective growth mechanism. The wing width and the window opening width in this work are the same (4μm). For future fabrication, asymmetric stripes may be used to create wider or thinner stripes.

The height of non-polar GaN stripes could be tuned via various growth times for different applications. Correspondingly, both the AlN buffer growth and the thickness of SiO_2 masks can be further optimised in order to meet the requirements with maintaining crystal quality and shape. For SiO_2 deposition, different deposition angle may be used to achieve fully block of silicon stripe surface, unused sidewalls, and bottom of the trench. This will further reduce the possibility of melt-back etching.

Further optimisation in GaN growth may be conducted, including the design of new mask patterning with different shape, dimension, spacing, etc. The V/III ration may be further reduced to create higher stripes. Second overgrowth can be carried out to

further increase the crystal quality. This second overgrowth requires fabrication on the first overgrown GaN.

For device growth, there is further more work from the perspective of epitaxial growth, such as p-i-n photodiodes on such a high quality non-polar GaN, non-polar laser structures, non-polar LEDs, multiple-colour LEDs aiming at white LEDs for general illumination, μLED arrays, etc.

The multi-wavelength quantum well structure growth may be modified to create white luminescence. With the increasing of TMIn flowrate, and the reduction of temperature, the indium content may be raised and emit lower energy light. Thicker quantum wells may also be applied to achieve longer wavelength. The thickness variation of the sidewall and the top surface maybe reduced by decrease the lateral growth, since the InGaN is extremely sensitive to temperature, increasing the ammonia may be one of the solutions.

For MSM-PDs, better contact between metal and nonpolar GaN can be achieved through optimising fabrication process to decrease the dark current and noise level of PD devices. The load resistor can be replaced by a high bandwidth trans impedance amplifier (TIA) for a better signal-to-noise ratio. For further improving the signal-to-noise ratio, a higher power UV light source can be applied to shine more light onto the photodiode to ensure photocurrent far larger than the system noise level. The UV LED can be replaced by UV laser diode to achieve faster electrical-optical modulation speed to avoid the effect of the light source speed during measurement.

With the presented results in Chapter 8, it is possible to achieve the intrinsic limits of GaN electronics by further exploring epitaxial growth of HT-AlN layer and GaN layer on large lattice-mismatched and industry compatible substrates. For the HEMTs, different Al content and the thickness of AlGaN layer can be applied to optimise the performance. The GaN buffer thickness may also be optimised. The size of the HEMT can be enhanced to apply the HEMT in practical power switching application. A field plate may be applied in the HEMT structure to measure the dynamic performance of the device.