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Bidirectional Multilevel Converter for Grid-Tie Renewable Energy and Storage with Reduced Leakage Current

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Abstract

This thesis discusses a transformerless multilevel converter (MLC) applied to a domestic level renewable energy system consisting of PV panels and EV batteries in their 2nd life applications. MLCs enable the use of conventional switching devices due to reduced voltage stress. Being able to produce a multilevel output voltage waveform, MLCs require less filtering and therefore may produce better quality waveform when compared to a standard 2-level voltage source converter (VSC). In this study, various modulation techniques for MLCs are implemented and the performance of the converter analysed regarding regulations and standards.

The system is designed to have two-stage power conversion, including a DC-DC boost converter for adjusting each stage battery voltage, and maximum power point operation of the PV panels in each module. This provides a stable input voltage for the DC-AC converter stage. The cascaded H-bridge converter (CHB) is selected for the DC-AC conversion due to its isolated DC source requirement. This topology enables the separation of the total DC link voltage into different modules, increasing the accessibility of EV batteries in their 2nd life application. The base system is designed to be coupled without a transformer to the single-phase UK utility grid.

A systematic approach is adapted for examining the MLC system. The design procedure starts with system parameter definition and component selection. This is then validated using simulation analysis and hardware implementation to demonstrate the practicability of the system for the planned application. The control algorithm is implemented in a National Instruments (NI) CompactRIO FPGA that can transform graphical programming into VHDL code. To accelerate the implementation and optimisation process, a co-simulation environment is used between NI LabVIEW and NI Multisim software. This ensures the optimisation of control code before compilation and enables testing without having analogue circuitry.

Converters without galvanic isolation may exhibit ground leakage currents when coupled with grounded PV panels. This thesis analyses the common-mode and differential-mode voltages that CHB modules generate, and their effect on ground leakage current. The mathematical analysis suggests that leakage current may be supressed solely on changing the modulation method in a CHB converter. A novel leakage reduction pulse width

modulation (LRPWM) technique is proposed, which successfully diminishes the ground leakage current to within the limit allowed by VDE-0126-1-1 (withdrawn, accessed in 2018) or IEC 62109-2 standard. The experimental results show that LRPWM has superior performance when compared to conventional MLC modulation techniques.

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A thesis dedicated to my parents

Izgun

Contents

Nomenclature

AC	Alternating Current
ADC	Analog-to-Digital Converter
AF	Active Filter
ANPC	Active Neutral Point Clamped
APODPWM	Alternate Phase Opposition Disposition Pulse Width Modulation
BES	Battery Energy Storage
BEV	Battery Electric Vehicle
BSI	British Standards Institution
CHB	Cascaded H-bridge
DC	Direct Current
DG	Distributed Generation
DSP	Digital Signal Processor
DVR	Dynamic Voltage Restorer
EMI	Electromagnetic Interference
ESR	Equivalent Series Resistance
ESS	Energy Storage Systems
EV	Electric Vehicle
FACTS	Flexible Alternating Current Transmission System
FB	Full Bridge
FCC	Flying Capacitor Converter
FPGA	Field Programmable Gate Array
GaN	Gallium Nitride
GTO	Gate Turn-off Thyristor
HB	Half Bridge
HEV	Hybrid Electric Vehicle
HPWM	Hybrid Pulse Width Modulation
HVDC	High Voltage Direct Current
IC	Integrated Circuit
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronic Engineers
IGBT	Insulated Gate Bipolar Transistor
IPM	Intelligent Power Module
LRPWM	Leakage Reduction Pulse Width Modulation
LSPWM	Level Shifted Pulse Width Modulation
MCB	Miniature Circuit Breaker
MLC	Multilevel Converter

MMC	Modular Multilevel Converter
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracker
NI	National Instruments
NLC	Nearest Level Control
NPC	Neutral Point Clamped
PCB	Printed Circuit Board
PCV	Parasitic Capacitance Voltage
PDPWM	Phase Disposition Pulse Width Modulation
PHS	Pumped Hydro Storage
PI	Proportional Integral
PLL	Phase Locked Loop
PODPWM	Phase Opposition Pulse Width Modulation
PSPWM	Phase Shifted Pulse Width Modulation
PV	Photovoltaics
PWM	Pulse Width Modulation
RCD	Residual Current Device
RES	Renewable Energy Source
RMS	Root Mean Square
SC	Solidity Clamped
SHE	Selective Harmonic Elimination
SiC	Silicon Carbide
SOC	State of Charge
SOH	State of Health
SPCV	Sum of Parasitic Capacitance Voltage
SPWM	Sinusoidal Pulse Width Modulation
STATCOM	Static-synchronous Compensator
THD	Total Harmonic Distortion
UPFC	Unified Power Flow Controller
V2G	Vehicle to Grid
VHDL	VHSIC Hardware Description Language
VHSIC	Very High Speed Integrated Circuit
VSC	Voltage Source Converter
WBG	Wide Band Gap
ZSD	Zero State Decoupled
ZSMC	Zero State Mid-point Clamped

Symbol List

Δi_L	Inductor ripple current
ΔV_{dc}	DC link voltage ripple
ζ	Damping ratio
A, B, C	Output Terminals
C_1, C_2, …	Capacitors
C_b	Base capacitance
C_{DC}	DC link capacitor
C_{PV}	Total parasitic capacitance of the PV panel
C_{PV1}, C_{PV2}	Parasitic capacitances on each terminal of the PV panel
D	Duty cycle
D_1, D_2, …	Diodes
D_{boost}	Boost mode duty cycle of DC-DC converter
D_{buck}	Buck mode duty cycle of DC-DC converter
f_c	Corner frequency / resonant frequency
f_{fund}	Fundamental frequency
f_{sw}	Switching frequency
h	Order of harmonic to be compensated
I_d, I_d	d and q-axis current
I_g	Grid current
I_L	Inductor current
I_{lg}	Grid leakage current
I_{lm1}, I_{lm2}, …	Leakage current of modules
j	Module index
K_p, K_i	Proportional and integral gain
K_u	Ultimate gain
L_1, L_2, …	Inductors
L_c	Converter side inductance
L_g	Grid side inductance
m	Number of output voltage levels
m_a	Modulation index / Modulation amplitude
n	Number of modules
P, N	Positive and negative terminals
P, Q	Active and reactive power
$P_{conduction}$	Conduction losses

P_{loss}	Power loss
P_{PV}	Power generated by PV panel
P_{rr}	Reverse recovery losses
P_{sw}	Switching losses
Q	Quality factor
R_d	Damping resistance
R_{th}	Thermal resistance
s	Switch index
$S_1, S_2, \ldots$	Switches
$S_2', S_2', \ldots$	Switches operating in complementary manner
$SOC_{average}$	Average state of charge of batteries
T_A	Ambient temperature
T_{junc}	Junction temperature
$V_{c1}, V_{c2}, \ldots$	Triangular carrier waveforms
V_{CM}	Common-mode voltage
$V_{CM_{eq.}}$	Equivalent common-model voltage
V_{DC}	DC link voltage
V_{DM}	Differential-mode voltage
V_g	RMS voltage of the utility grid supply
$V_{grid\text{-}p(max)}$	Utility supply maximum peak voltage
$V_{m1}, V_{m2}, \ldots$	Module output voltages
V_{N_jO}	Parasitic capacitance voltage of j^{th} module
V_{N_TO}	Sum of parasitic capacitance voltages
V_{pv}	PV panel voltage
V_{pv_mpp}	PV panel maximum power point voltage
$V_{r1}, V_{r2}, \ldots$	Modified reference signals
V_{ref}	Utility supply reference waveform
V_{RMS}	Root-mean-square voltage
ω	Angular frequency in radians
X	Imaginary point
Z_b	Base impedance
Z_L	Impedance of filters
Z_{pvj}	Impedance of the PV panel

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Chapter 1
Introduction

1.1 The Utility Grid

Within the UK, the utility grid is divided into three areas, generation, transmission and distribution. Conventional methods of generating electricity mainly involves burning fossil fuels at a centralised power plant. The generated electricity is then transferred to a high voltage (HV) transmission network by step up transformers. The transmission network is a meshed network that delivers bulk power from the generators to medium voltage (MV) substations. The MV substations are interfaced with a low voltage (LV) distribution network where the voltage is lowered and the power is distributed to the end consumers. Figure 1.1 represents a conventional centralised utility grid.

In these conventional centralised systems, the utility grid allows unidirectional power flow from centralised power plants to end users only. The distribution network has a passive structure therefore self-healing is not possible, which makes the utility grid prone to failure [1]. Clearing a fault in a conventional system generally requires manual action therefore self-restoring capability is very limited and time consuming [2].

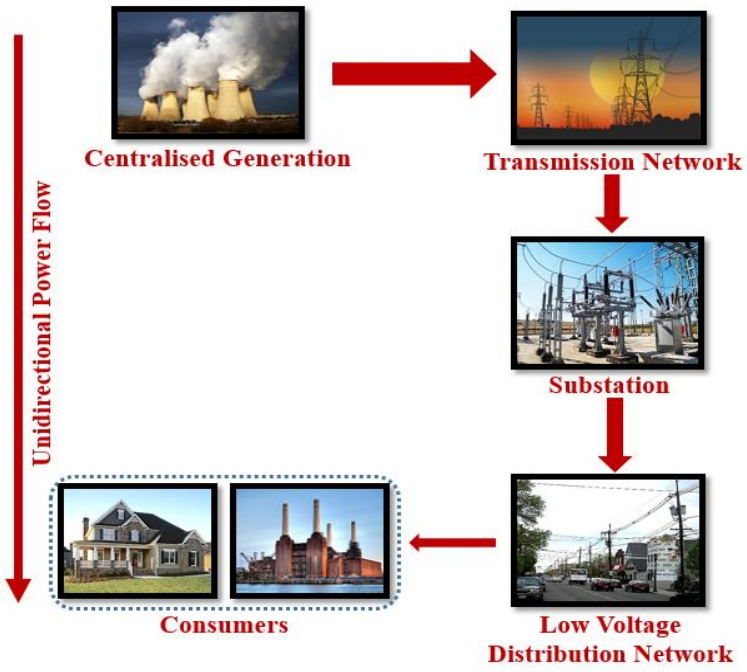

Figure 1.1: Conventional centralised utility grid

The utility grid is undergoing a significant change in recent years, mainly due to the attention given to renewable energy sources (RES), and the desire to satisfy societal concerns on environmental sustainability. This change is mainly driven by legislation and incentives by governments, alongside technological advancements such as communications, manufacturing, automation and power electronics. These advancements and incentives enable deployment of RES close to the point of energy consumption, or alternatively on the consumer side of the network; in other words they support distributed generation [3].

Distributed generation (DG) provide benefits not only to consumers but also to sites where there are deficiencies in the distribution network [4]. DG may increase utility network reliability, power quality and system efficiency if carefully planned [5]. DG has positive effects on the electricity price as its nature is flexible in many aspects such as: volume, operation and scalability [6]. Conversely, increased penetration of RES and DG in the energy generation mix may trigger problems in the conventional centralised grid infrastructure. Large scale diffusion of DG in generation share may lead to unstable voltage controls of low voltage distribution network due to the extent of power injection at the point of coupling [7]. DG consisting of RES also has an intermittent nature that may escalate the problems as there is also uncertainty in the generation profile.

In order to create a buffer between a traditionally centralised generation system being used in conjunction with DG and variable energy demand, energy storage systems (ESS) have already been integrated onto the utility grid. Globally installed utility-scale energy storage capacity is > 160 GW as of 2018, where the most deployed technology is pumped hydro storage (PHS). Furthermore, the battery energy storage (BES) share has increased to 3 GW by 2019, where leading counties such as Australia, China, Republic of Korea, United States and United Kingdom has accounted for 80% of this capacity [8]. 200 MW of BES was installed under the Enhanced Frequency Response procurement programme by National Grid in UK in 2018 [9]. It should be noted that ESS are not limited to PHS and BES. There are emerging technologies such as flywheel, compressed air storage, flow batteries, superconducting magnetic storage and thermal energy storage. These technologies have their own characteristics that may be suitable for short/long term storage or energy/power delivery.

Battery electric vehicle (BEV) and hybrid electric vehicle (HEV) registrations during 2019 also increased by 158% and 35% respectively compared to 2018 in UK [10]. EVs consist of

rechargeable batteries that are generally replaced by automotive manufacturers when their state of health (SOH) degrade to 70-80% compared to when the batteries are newly manufactured [11]. The replaced batteries may be unsuitable for EV applications, however they may be viable for other applications. The 'second life' application of these batteries for use in LV utility grid support is discussed in [11, 12]. Moreover, the integration of EVs into utility grid support is inevitable and already discussed in literature as vehicle-to-grid (V2G). V2G may bring value to EV batteries in their first life by providing ancillary services in grid support, boosting their asset value.

A 'smart grid' is an idea of innovating the existing utility grid by encouraging the use of state-of-art technologies such as computation, automation and sensors in order to deliver highly reliable, efficient, flexible and sustainable service that is based on establishing a two-way communication between the devices and the assets [13]. Figure 1.2 illustrates a representation of smart grid, including DG, RES, end users, and also communication and power electronic devices. Transitioning into a 'smart grid' brings many challenges for power electronic energy conversion and ESS as these systems not only need to be able to communicate with each other, but also need to deliver better power quality with low harmonic distortion [14].

As seen in Figure 1.2, most of the assets connected to the utility grid requires some form of electricity conditioning circuit in order to be coupled with the utility grid at correct voltage level. Power electronic converters provide reliable and efficient conversion due to advances in semiconductor devices, converter topologies and control. The emerging wide bandgap (WBG) semiconductor devices allows operation of converters at higher frequencies, resulting in better output voltage waveforms [15]. High power converters conventionally consist of high power switching devices that can withstand high voltage/current stress. Multilevel converters (MLC) brought the idea of dividing a DC bus voltage into smaller levels, therefore allowing the use of lower voltage semiconductor devices with high power converters. Increasing the number of voltage levels also provides a closer approximation to a sinusoid in a DC-AC converter, generating a better output voltage waveform with an inherently lower harmonic content, resulting in less filtering requirements. In the literature, various MLC topologies are studied, all having different characteristics and requirements that suit numerous applications. Various MLCs will be discussed in Chapter 2.

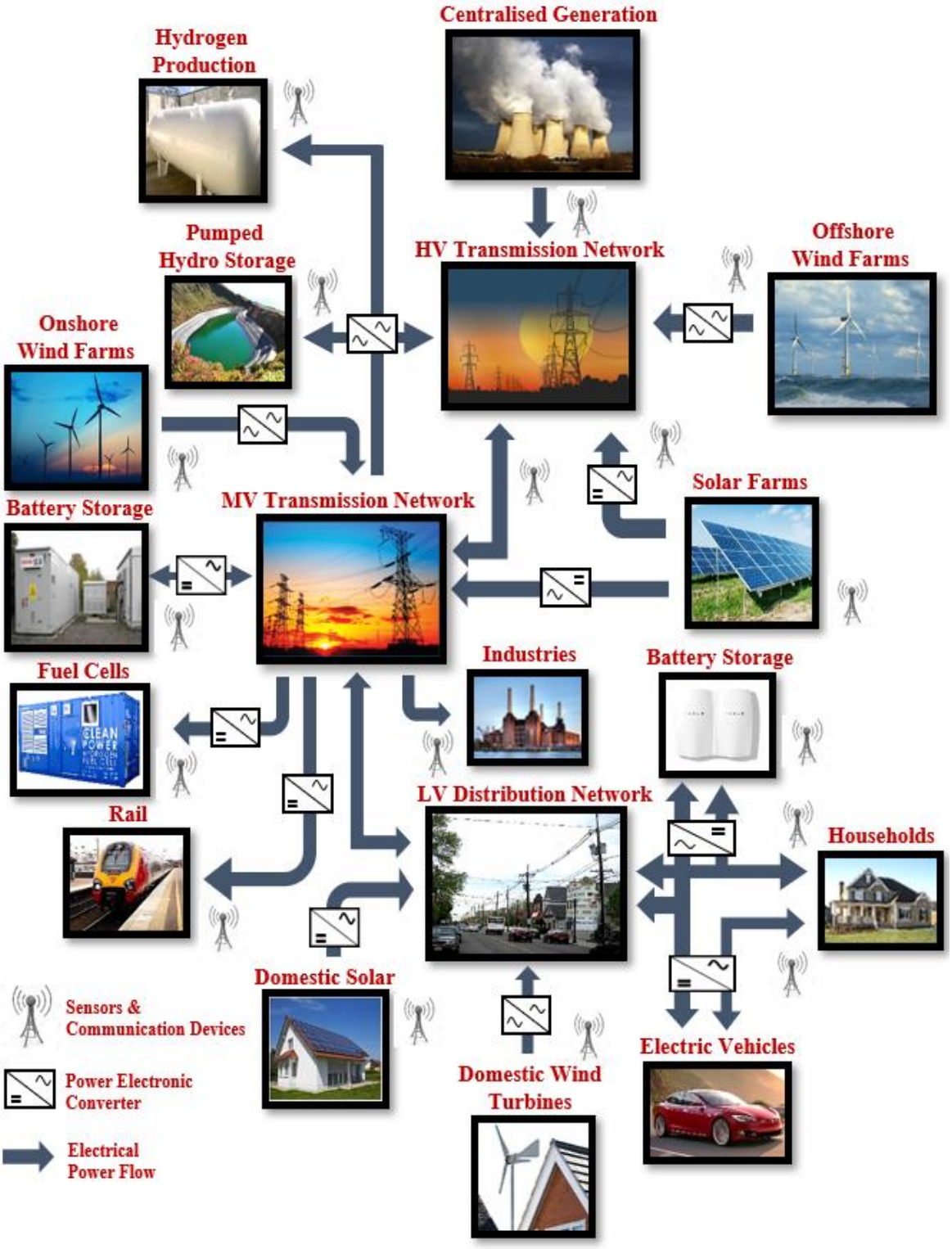

Figure 1.2: A representation of Smart Grid

1.2 Motivation and Application

This thesis embodies research undertaken on a 9-level multilevel converter utilising EV batteries in their 2nd life applications and PV panels. The converter is designed to be connected to UK single-phase grid at 230 V_{RMS} and 50 Hz, targeting a domestic scale application of 4 kVA. The converter aimed to have two-stage conversion, including a DC-DC converter for adjusting battery voltage, and also a cascaded DC-AC stage for grid-tie operation. The cascaded H-bridge (CHB) topology is chosen for the study as it provides high accessibility for EV batteries in their 2nd life application. The number of modules may be increased to achieve a more efficient maximum power point tracker for PV panels. Figure 1.3 represents a block diagram showing the main parts of the 9-level CHB converter.

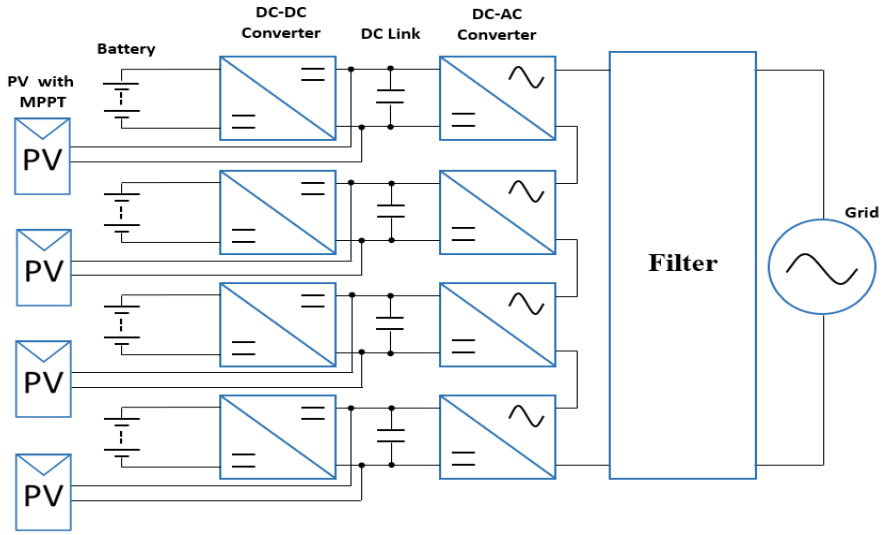

Figure 1.3: Block diagram for the 9-level CHB single-phase converter

Cascaded H-bridge converter is one of the most studied multilevel converter topologies as it requires isolated DC sources for correct operation. This makes this topology favourable when operated in conjunction with batteries and PV panels [16]. The cascaded structure enables reduction of the harmonics in output voltage/current waveforms, reducing the cost of coupled grid filter [17].

Transformerless H-bridge converters generate common-mode voltages causing ground leakage currents when coupled with grounded capacitive DC sources [18]. PV panels are grounded capacitive DC sources, as applications require them to be connected to ground for safety. Leakage current is a potential health hazard due to shock potentials caused by current flow, and it also degrades system efficiency and power quality due to current flow to the ground [19].

This research aims to study common-mode and differential-mode voltages to find a solution for reducing the ground leakage currents within a set of limits given by regulations and standards. Achieving this enables the use of EV batteries in their 2nd life applications with domestic rooftop PV systems by using same converter. Furthermore, this may increase the penetration of PV systems in low voltage distribution networks by using batteries as an energy storage buffer.

The proposed modulation technique allows the use of this topology without any adjustments to the hardware and allows the system to conform to the standards. This method increases the efficiency and power quality of the system. Furthermore, the lack of need for additional system components does not increase the system cost and volume due to reduced filtering requirement and lack of transformer. Additionally, two algorithms are discussed for conventional modulation schemes for balancing the state of charge of the batteries within modules during continuous operation. Lastly, the use of modern simulation software tools such as LabVIEW and Multisim in a co-simulation environment greatly reduced the implementation time of hardware controller.

1.3 Limitations

During this study, the main limitation was the lab space. A 4 kVA system interfacing batteries and PV panels would require more than 30 m^2 space, which was not available. This could be solved by using 4x PV emulators and 4x isolated power supplies. The funding going into this study was limited therefore author decided to emulate the PV behaviour by using transformers in conjunction with bridge rectifiers for achieving isolated DC supplies. Furthermore, standard film capacitors were used for replicating the capacitive behaviour of PV panel coupling to ground.

Another limitation was the point of grid coupling. The weak grid (high grid impedance) at the point of grid coupling made closed loop control tuning more difficult. Also, the university building where experimental kit is placed, houses many other experimental projects, including grid-tie machines and rectifiers that inject low order harmonics to the utility, distorting grid voltage.

Lastly, the grid safety transformer for initial tests was limited to 3.3 kVA discontinuous operation. As a result, some of the results were limited to this power rating, therefore calculated output current THD values may be higher than expected due to low power operation.

1.4 Scientific Contributions

This section presents the main scientific contributions according to the perspective of the author. These are listed below:

- A critical survey on multilevel converters.

Multilevel topologies such as Neutral Point Converter, Flying Capacitor Converter, Cascaded H-bridge Converter (CHB) and Modular Multilevel Converters are discussed. Their application, control and modulation techniques are discussed with the help of MATLAB/Simulink platform.

- A survey on suppressing leakage current in transformerless converters.

This contribution inspires future research on reducing leakage current in multilevel converters, detailing different converter topologies, filtering and modulation methods for suppressing ground leakage currents. As a result of this contribution, a generalised formula is proposed for calculating the sum of common-mode and differential-mode voltages in an *m*-level CHB converter. Furthermore, a modulation method for suppressing leakage current in a 9-level CHB is proposed.

- A case study on output filtering arrangement

The effects of converter output voltage levels and output filter arrangement on converter output waveforms are discussed. The study reveals that increased output voltage levels reduces filtering requirement. Moreover, leakage current cannot be suppressed solely on modulation based methods when output filter has an asymmetrical configuration.

- Use of modern simulation environments (Co-simulation)

Co-simulation environment reduces hardware implementation time by deploying control algorithm and virtual analogue circuitry in an environment where digital and analogue simulation engines may interact with each other.

- A two-stage grid-tie transformerless Cascaded H-bridge converter for renewable energy and battery energy storage

This modular system can utilise batteries and PVs within a two stage conversion system. Low voltage battery and PV systems are interfaced to the single-phase grid, allowing higher accessibility for 2nd life application batteries and modular maximum power point tracking for PVs. This may achieve a more efficient and reliable system.

1.5 Publications

[1] **I. Gunsal**, D. A. Stone, and M. P. Foster, "Suppressing Leakage Current for Cascaded H-bridge Converters in Grid-Tie Renewable Energy Systems," in *2019 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe)*, pp. P.1-P.8, 2019.

[2] **I. Gunsal**, D. Stone and M. Foster, "A transformerless single-phase multilevel converter for grid-tie renewable energy systems", *Energy Reports*, vol. 6, pp. 70-75, 2020.

[3] **I. Gunsal**, D. A. Stone, M. P. Foster, "A Unique Pulse Width Modulation to Reduce Leakage Current for Cascaded H-Bridge Inverters in PV and Battery Energy Storage Applications," in *Energy Procedia*, vol. 151, pp. 84-90, 2018.

[In Review]

I. Gunsal, D. A. Stone, M. P. Foster, "Suppressing Leakage Current for Cascaded H-Bridge Inverters in Renewable Energy and Storage Systems," in *IEEE Transactions on Industrial Electronics*, 2020.

1.6 Thesis Outline

In this section, the structure of the thesis and contents of all chapters are outlined.

CHAPTER 2 discusses a review of the state-of-the-art multilevel converters, detailing their operation with relevant simulations. This chapter includes a comparison for suitability of various topologies in different applications. Conventional multilevel converter modulation techniques are also discussed.

CHAPTER 3 investigates the effect of parasitic capacitance in a grid-tie PV converter. Common-mode analysis of single and three-phase systems are outlined and methods for suppressing ground leakage current are discussed. A novel modulation based method, Leakage Reduction Pulse Width Modulation (LRPWM), is proposed.

CHAPTER 4 details design of a 9 level Cascaded H-bridge (CHB) grid-tie converter including a two-stage conversion. The design is used as a base system for the hardware platform. MATLAB/Simulink system simulations are given and the control algorithm of the hardware platform is integrated in LabVIEW and Multisim co-simulation environment.

CHAPTER 5 presents prototype hardware that is used as the base system. The control platform and its implementation, sensors and signal conditioning, thermal management of power modules and hardware implementation of LRPWM are discussed. Experimental results for the algorithm discussed in Chapter 3 are presented.

CHAPTER 6 discusses grid connection and power quality for a grid-tie converter. Regulations and standards for this type of converters are investigated therefore grid-filter configurations and their effect on the converter performance is outlined. Various closed loop current control and phase locked loop algorithms are discussed and hardware implementation are shown.

CHAPTER 7 discusses conclusions and potential future work.

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Chapter 2
Multilevel Converters

2.1 Introduction

Transferring energy in forms of either alternating current (AC) or direct current (DC), provides advantages in different applications [1, 2]. Power electronic converters are used in transforming these different forms of energy into each other by using switching and/or passive devices (capacitors and inductors). Power converters have numerous application areas such as transportation, industry, renewable energy, defence and aerospace.

Semiconductor devices are main limiting factor when it comes to operating power electronic converters at MV and HV levels. The limited availability of HV semiconductors drove scientists to alternative solutions, such as using conventional 2-level converter topologies with switching devices that can withstand high voltage/current ratings or using emerging multilevel converter topologies with standard switching devices [3]. Multilevel topologies suffer less voltage/current stress on semiconductor devices, therefore it is possible to use highly reliable maturing technologies such as Insulated Gate Bipolar Transistors (IGBTs). Although wide-bandgap (WBG) devices like Silicon carbide (SiC) and Gallium Nitride (GaN) promise high switching frequencies and low switching loss, GaN devices still cannot compete with IGBT and SiC devices at high voltage range [4].

Multilevel converters (MLC) may be operated in unidirectional or bidirectional mode varying power flow direction for the purpose of the application. Bidirectional converters may reduce the system size when compared with using two unidirectional converters. MLCs can be constructed in many different ways depending on the topology, the number of output levels and application type [5-7]. Some of the research topics in MLCs include control algorithm enhancements [8], total harmonic distortion (THD) improvements [9] and DC link capacitor balancing [10].

This chapter provides an introduction to the MLCs, discussing the main topologies, presenting simulation studies for analysis, performing comparisons between topologies, application types and finally their modulation methods.

2.2 Multilevel Converters

MLCs are a sub category of power electronic converters that are able to generate three or more stepped output voltage levels with respect to the negative terminal of the DC link [11]. A multilevel waveform compared to a standard two-level waveform has smaller discrete voltage levels per switching transition. This allows MLCs to produce a closer approximation of sinusoidal reference wave. In addition, MLCs provide other advantages over standard 2-level converters such as; higher power quality output and reduced filtering requirements. In contrast, MLCs suffer from increased control complexity and reduced reliability due to the number of the switching devices and their negative effect on the DC link voltage [6, 12].

There has been an increased industrial and academic attention to the MLCs in recent years. Some of the most known and well-established topologies are as follows:

- Neutral-Point-Clamped Converter (NPC)
- Flying Capacitor Converter (FCC)
- Cascaded H-bridge Converter (CHB)
- Modular Multilevel Converter (MMC)

A patent [13] shows that MLC topologies have been around since 1975, where isolated DC sources are used in conjunction with full-bridge (FB) cells to create a multilevel output waveform. This idea can be related to the cascaded H-bridge converter (CHB) topology [7]. Other topologies, for example the neutral-point-clamped converter (NPC), which uses diodes to clamp the voltages from a single DC source, was introduced in 1980 [14]. Also the flying capacitor converter (FCC) was introduced in 1992 [15]. An FCC utilises capacitors to reduce the single DC source voltage into smaller levels to generate a multilevel output. However, the FCC topology suffers from capacitor voltage balancing issues. The modular multilevel converter (MMC) introduced in 2003 by A. Lesnicar and R. Marquardt provides high modularisation capability, which makes this topology very suitable for HV applications [16].

These MLCs are analysed in the following sub-sections, and circuit diagrams and their corresponding output voltage waveforms are illustrated. Here, the waveforms are generated by open loop simulations with a 10 kΩ load connected to the converter's output and 100V DC link at its input. Fundamental (f_{fund}) and switching frequencies (f_{sw}) are 50 Hz and 4 kHz respectively in order to better visualise switching events.

2.2.1 Cascaded H-bridge Converter

The cascaded H-bridge (CHB) converter requires of a number of series connected full-bridge converters (H-bridge). Each H-bridge needs an isolated DC source, therefore when increasing the output voltage levels, additional H-bridges and independent DC sources are required. A 3-level H-bridge topology is illustrated in Figure 2.1, where the circuitry has four active switching (S_1, S_2, S_3, and S_4) and no passive devices.

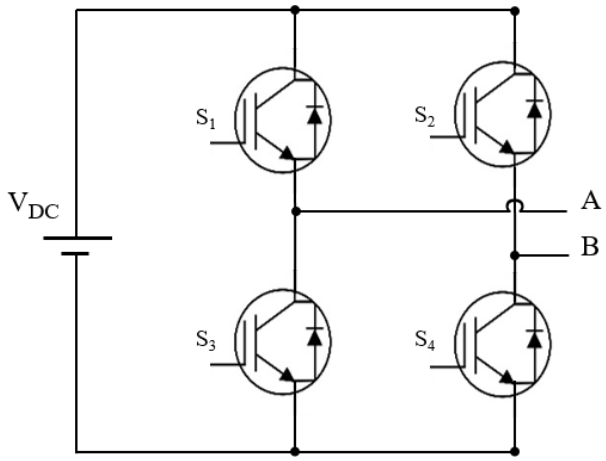

Figure 2.1: 3-level single-phase H-bridge converter

The H-bridge shown in Figure 2.1 has two switching devices in each leg that operate in complementary form (both switches at the same leg must not be 'ON' at the same time to avoid a short-circuit or shoot-through). The switching states of the H-bridge converter are presented in Table 2.1. Different switching combinations can generate three possible output voltage levels of $+V_{DC}$, 0V and $-V_{DC}$. S_1 and S_4 are 'ON' whereas S_2 and S_3 are 'OFF' in order to produce the positive DC output voltage. Conversely, S_1 and S_4 are 'OFF' whereas S_2 and S_3 are 'ON' to give an output voltage of $-V_{DC}$. There is more than one available configuration to give the 0V output state.

S_1	S_2	S_3	S_4	V_{out} (V_A-V_B)
1	0	0	1	V_{dc}
1	1	0	0	0
0	0	1	1	0
0	1	1	0	$-V_{dc}$

Table 2.1: Switching states of 3-level H-bridge converter

The output voltage measured between A and B terminals has three voltage levels and is shown in Figure 2.2.

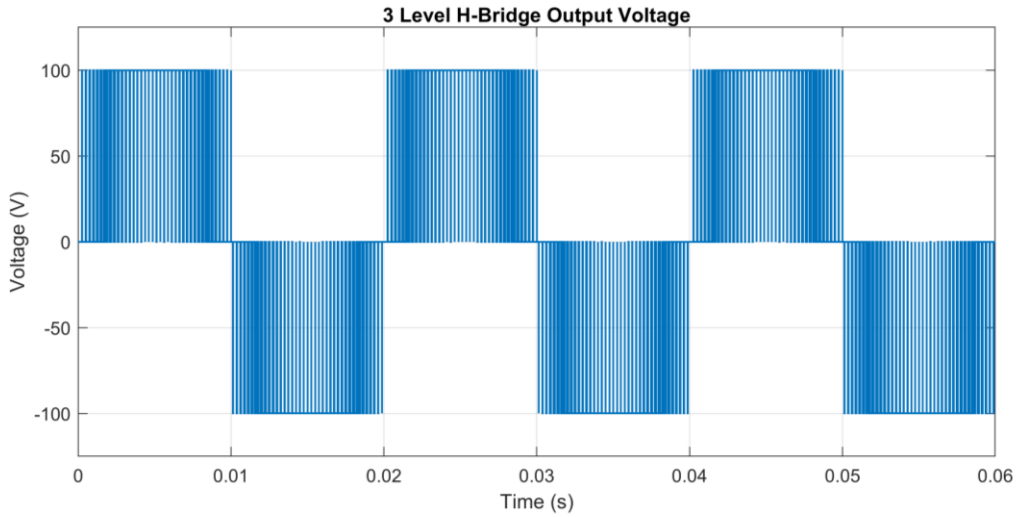

Figure 2.2: Output voltage waveform of 3-level H-bridge converter

The number of levels may be increased to form an *m*-level CHB converter. Two H-bridges are cascaded to form 5-level CHB converter, as shown in Figure 2.3. The output voltage measured between nodes A and B is the sum of the voltages across each H-bridge modules, and varies between $2V_{DC}$ and $-2V_{DC}$ respectively. When generating the remaining voltage levels ($+V_{DC}$, 0V and $-V_{DC}$), there are redundant switching states as these output voltage levels may be achieved with more than one switching pattern.

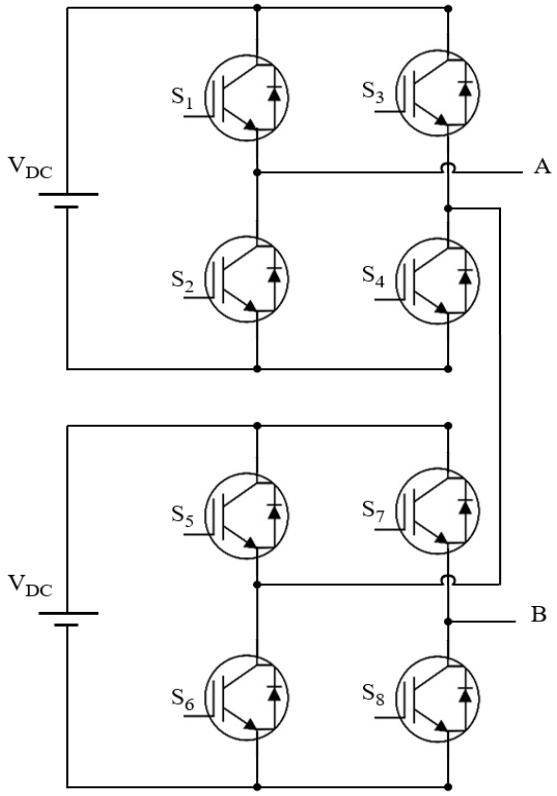

Figure 2.3: 5-level single-phase Cascaded H-bridge converter

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	V_{out}
1	0	0	1	1	0	0	1	$2V_{dc}$
1	0	0	1	1	0	1	0	V_{dc}
1	0	1	0	1	0	1	0	0
0	1	1	0	1	0	1	0	$-V_{dc}$
0	1	1	0	0	1	1	0	$-2V_{dc}$

Table 2.2: Switching states of 5-level cascaded H-bridge converter

Table 2.2 shows some of the possible switching states and Figure 2.4 illustrates the output voltage waveform of the 5-level CHB converter.

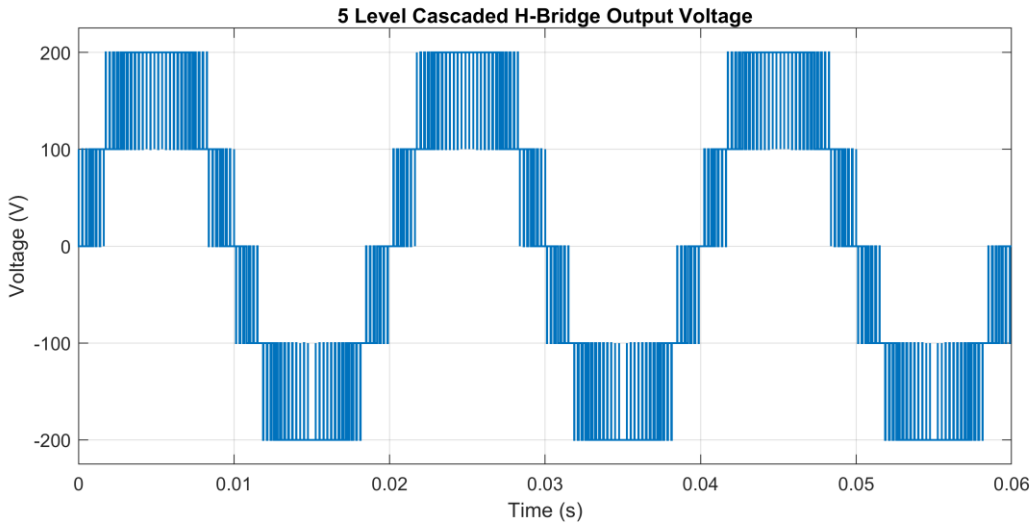

Figure 2.4: Output voltage waveform of 5-level Cascaded H-bridge converter

A CHB converter is capable of producing $m = 2n + 1$ output voltage levels, where n is the number of H-bridge modules in series. A 9-level CHB requires 4 cascaded H-bridge modules and can be seen in Figure 2.5. The voltage waveforms for a 9-level and a 15-level CHB are shown in Figure 2.6 and Figure 2.7 respectively. The number of semiconductor devices increases as the number of cascaded modules rises. As a result of this, the modulation complexity increases and also converter reliability reduces. However, the converter may become more fault tolerant by bypassing faulty modules [17].

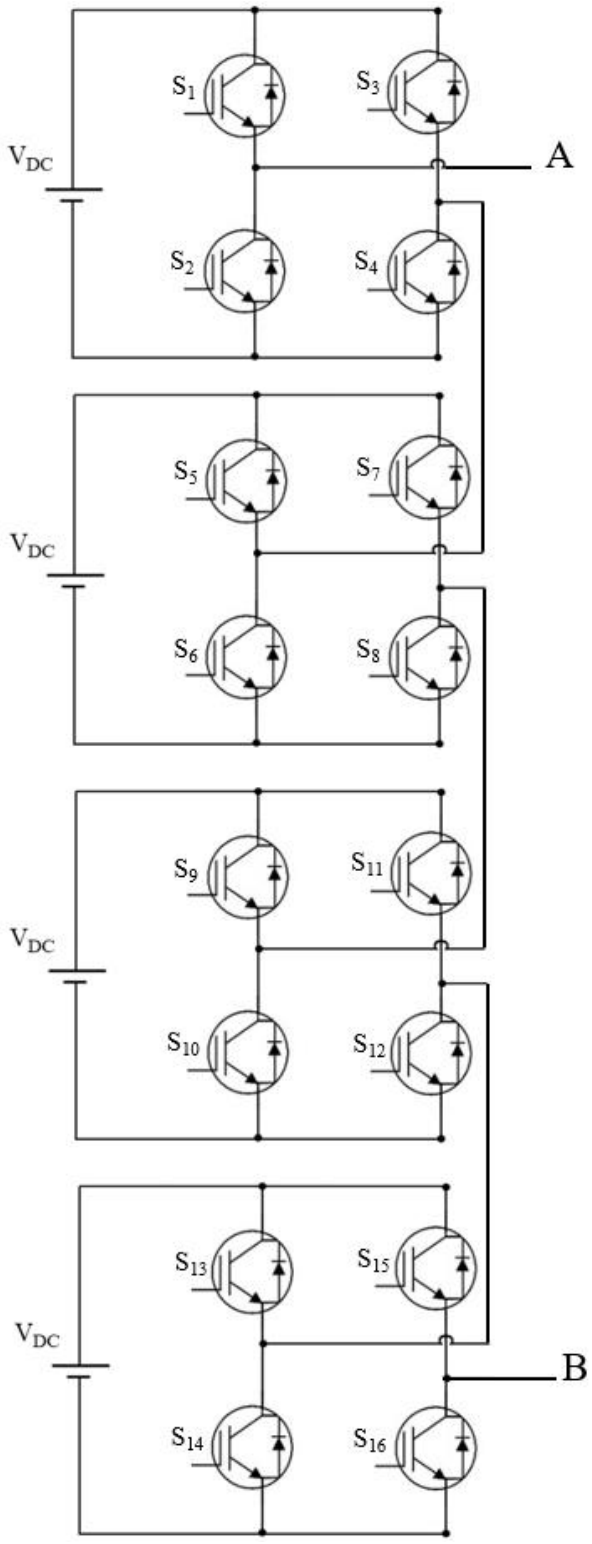

Figure 2.5: 9-level single-phase Cascaded H-bridge converter

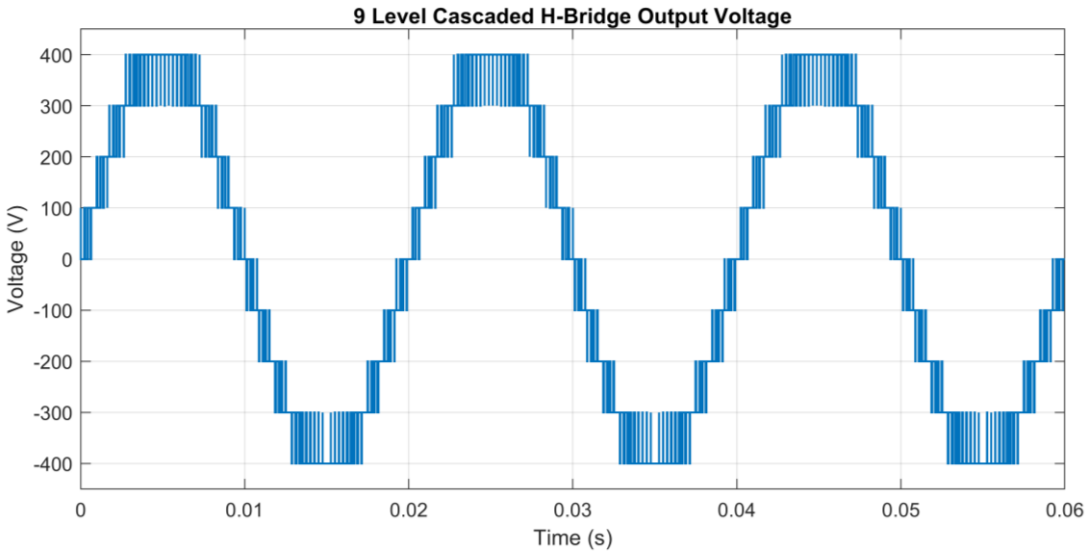

Figure 2.6: Output voltage waveform of 9-level Cascaded H-bridge converter

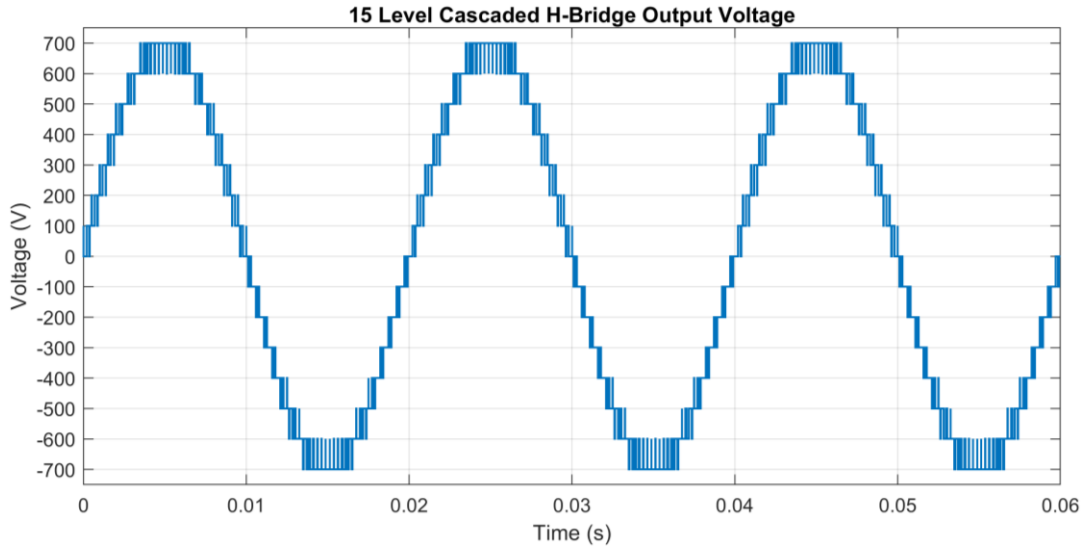

Figure 2.7: Output voltage waveform of 15-level Cascaded H-bridge converter

The CHB does not require either floating capacitors or clamping diodes compared to NPC and FCC, which makes this topology attractive in high power applications. In contrast, requiring an isolated supply can be a drawback depending on the type of application. Work previously presented in [18] reveals that the MMC is advantageous over both the CHB and NPC topologies for MV variable speed drives, when it comes to DC link energy and installed silicon area. In contrast, the study in [19] presents a comparison between CHB and MMC used with a 10 MVA battery storage system. This study concludes that the CHB is better suited for battery systems.

2.2.2 Neutral Point Clamped Converter

The neutral point clamped (NPC) converter (also known as diode clamped converter) requires a single DC source unlike CHB converters. The DC link is split into multiple voltage levels with capacitors, where diodes are used to clamp these voltage levels. A three-phase 3-level NPC is presented in [20] consisting of three converter legs. For single-phase operation, the NPC converter may have single or double leg configuration, each topology having individual strengths and weaknesses. For example, half-bridge (single leg) converters can only utilise half of the available DC link voltage, whereas full-bridge (double leg) converters suffer from common-mode voltage problems. A half-bridge 3-level NPC, Figure 2.8, consists of capacitors C_1 and C_2 in order to create voltage levels of $V_{dc}/2$ and $-V_{dc}/2$, and diodes D_1 and D_2 to clamp these voltages. The output voltage waveform for a half-bridge (HB) 3-level NPC is shown Figure 2.9. The output is connected between nodes A and B, where the point B is neutral point between the capacitors C_1 and C_2.

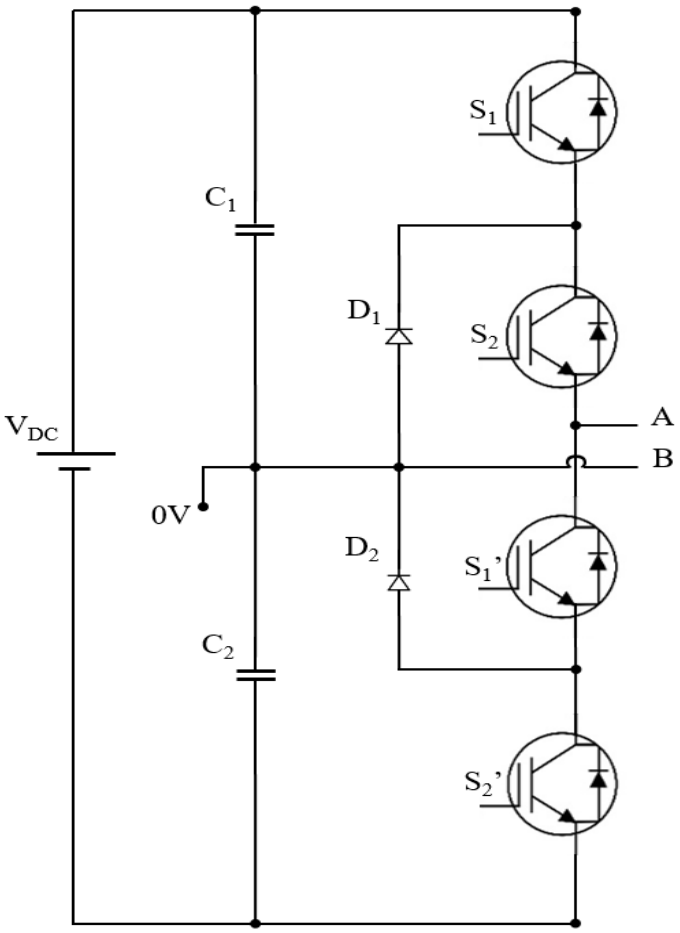

Figure 2.8: 3-level single-phase Neutral Point Converter

The switching states for a HB 3-level NPC are given in Table 2.3. The switches S_1 and S_1' are complementary switches (also S_2 and S_2') where '1' indicates the device is 'ON' and vice versa. It should be noted that the capacitor voltages need to be balanced during a complete switching pattern in order to maintain $V_{dc}/2$, 0 and $-V_{dc}/2$ between points A and B over a full switching cycle.

S_1	S_2	S_1'	S_2'	V_{out}
1	1	0	0	$V_{dc}/2$
0	1	1	0	0
0	0	1	1	$-V_{dc}/2$

Table 2.3: Switching states of 3-level Neutral Point Clamped converter

As the number of voltage levels in the converter increases, the harmonic content at its output reduces, leading to diminished filter requirements, thus reduced overall system size. The voltage stress on semiconductor devices also reduces with increasing levels however, the number of capacitors increases.

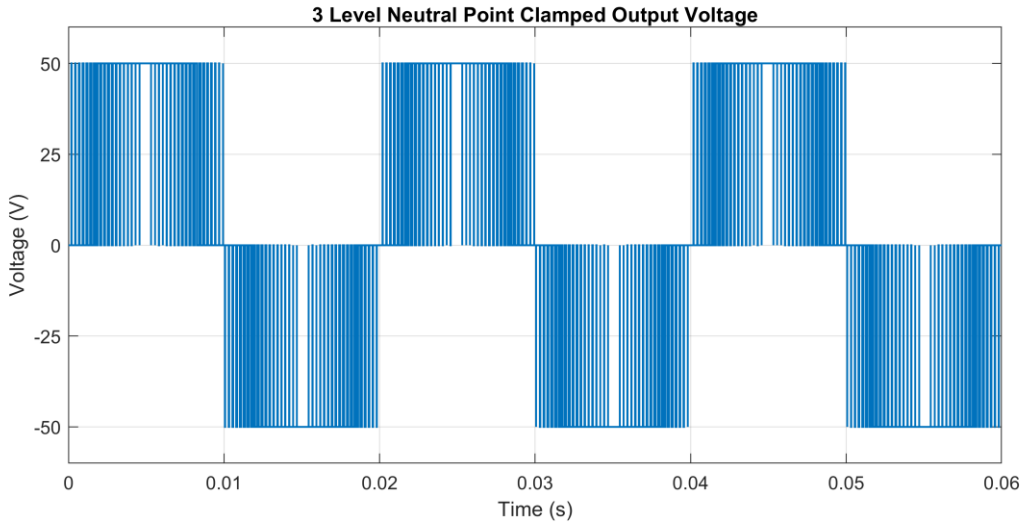

Figure 2.9: Output voltage waveform of half-bridge 3-level NPC converter

The NPC has different topology options when it comes to increasing the output voltage levels. For a 5-level NPC, one option is to add another leg to the standard HB 3-level NPC in order to end up with a full-bridge 5-level NPC. This converter is a full-bridge (FB)

topology therefore, the DC link voltage may be utilised fully. The output voltage levels are then: V_{dc}, $V_{dc}/2$, 0, $-V_{dc}/2$ and $-V_{dc}$. The FB 5-level NPC topology is shown in Figure 2.10. The switching states of FB 5-level NPC is detailed in Table 2.4. It should be noted that this table does not include all the redundant states that may be used for capacitor balancing.

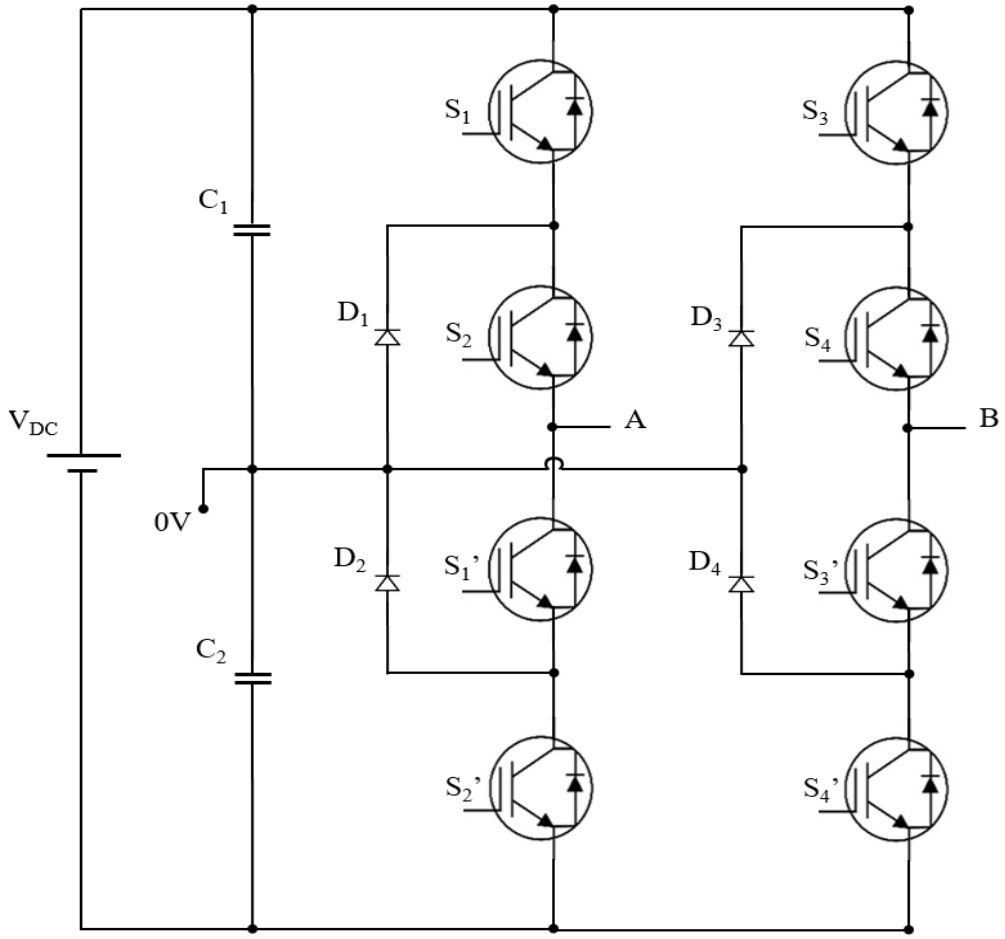

Figure 2.10: 5- level full-bridge single-phase Neutral Point Clamped converter

S_1	S_2	S_3	S_4	S_1'	S_2'	S_3'	S_4'	V_{out}
1	1	0	0	0	0	1	1	V_{dc}
0	1	0	0	1	0	1	1	$V_{dc}/2$
0	0	0	0	1	1	1	1	0
0	0	0	1	1	1	1	0	$-V_{dc}/2$
0	0	1	1	1	1	0	0	$-V_{dc}$

Table 2.4: Switching states of 5-level full-bridge Neutral Point Clamped converter

The output waveform for a FB 5-level NPC is shown in Figure 2.11. It can be seen that the 100V DC link is fully utilised.

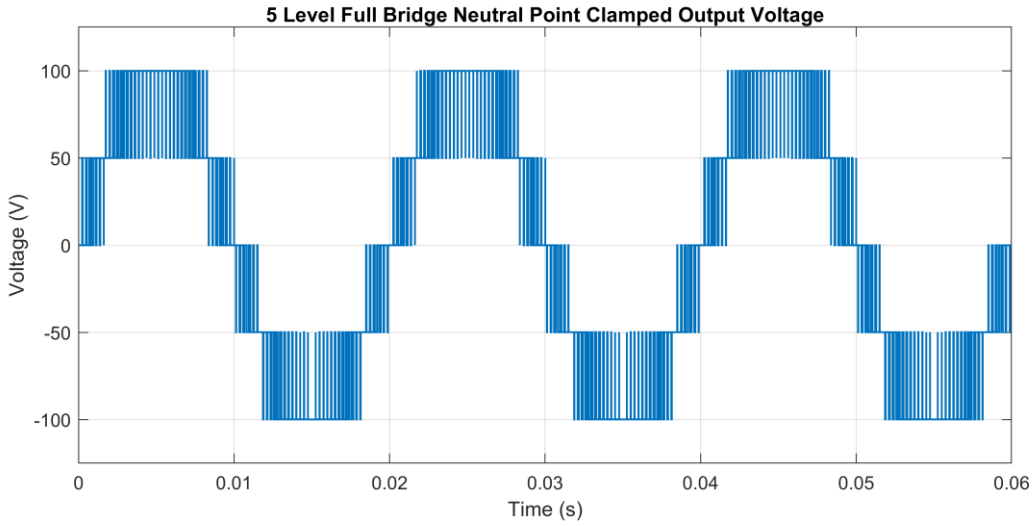

Figure 2.11: Output voltage waveform of 5-level full-bridge Neutral Point Clamped converter

The other approach to produce a 5-level NPC is to add extra capacitors and diodes to the half-bridge configuration. Half-bridge 5-level NPC topology can be seen in Figure 2.12. Although the HB 5-level NPC and FB 5-level NPC creates the same number of output voltage levels, the HB 5-level NPC has 2 more additional diodes and capacitors, summing to a total of 6 diodes and 4 capacitors. The output levels offered by HB 5-levels NPC is also different from FB version, which are $V_{dc}/2$, $V_{dc}/4$, 0, $-V_{dc}/4$ and $-V_{dc}/2$ (Figure 2.13). Despite having a lower utilisation of DC link in HB 5-levels NPC, this topology does not suffer from common-mode voltage problems as seen in a FB 5-level NPC [21].

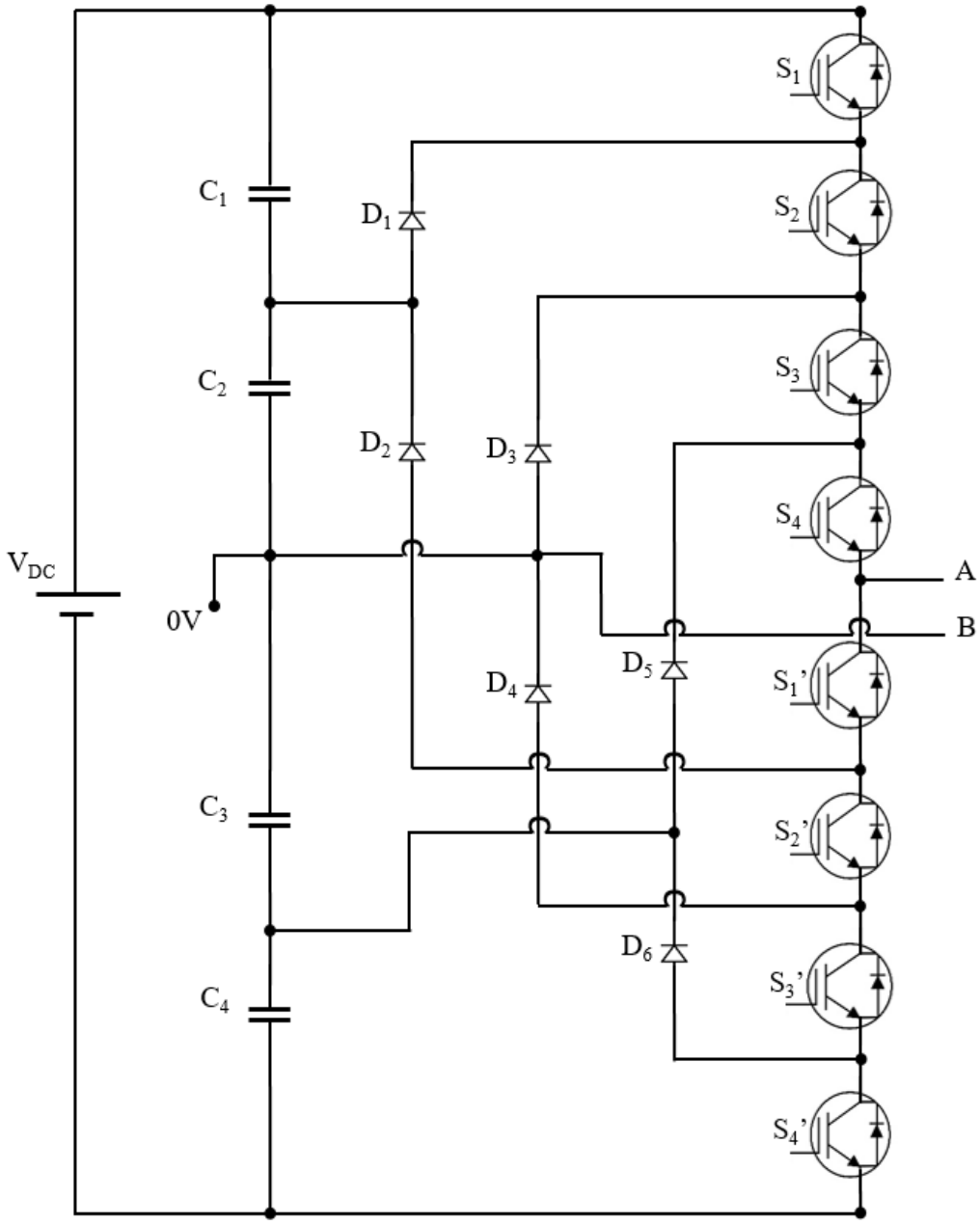

Figure 2.12: 5-level half-bridge single-phase Neutral Point Clamped converter

The switching states for the HB 5-level NPC is illustrated in Table 2.5, where all switches from S_1 to S_4' are represented. The switches S_1 - S_1', S_2 - S_2' and so on… are complementary pairs.

S_1	S_2	S_3	S_4	S_1'	S_2'	S_3'	S_4'	V_{out}
1	1	1	1	0	0	0	0	$V_{dc}/2$
0	1	1	1	1	0	0	0	$V_{dc}/4$
0	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	$-V_{dc}/4$
0	0	0	0	1	1	1	1	$-V_{dc}/2$

Table 2.5: Switching states of 5-level half-bridge Neutral Point Clamped converter

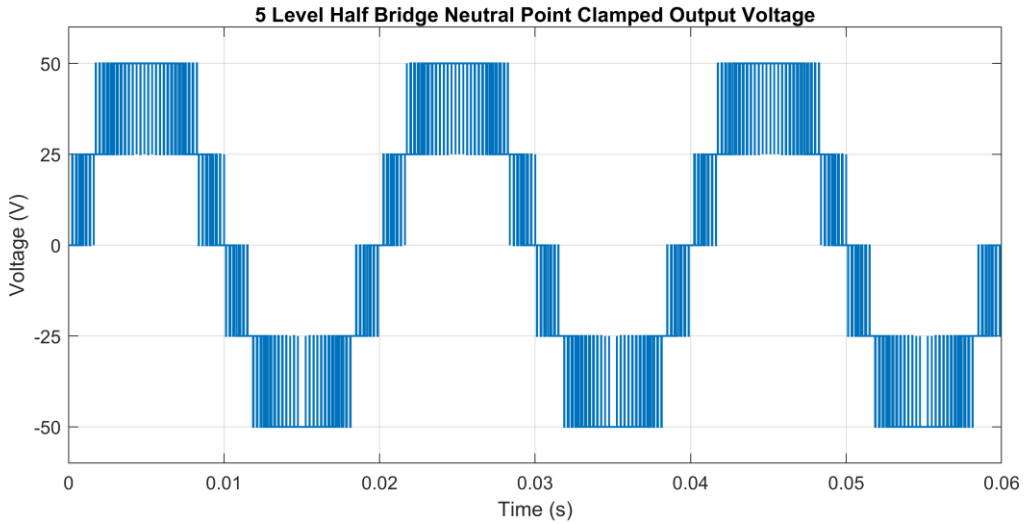

Figure 2.13: Output voltage waveform of 5-level half-bridge Neutral Point Clamped converter

A FB 9-level NPC can also be constructed by adding another leg to the HB 5-level NPC, where this topology has 16 switching devices, 12 clamping diodes and 4 DC link capacitors. Considering the number of devices as output voltage levels increases, the control of the converter becomes more complex. The circuit diagram of FB 9-level NPC and the resultant output voltage waveform are shown in Figure 2.14 and Figure 2.15 respectively.

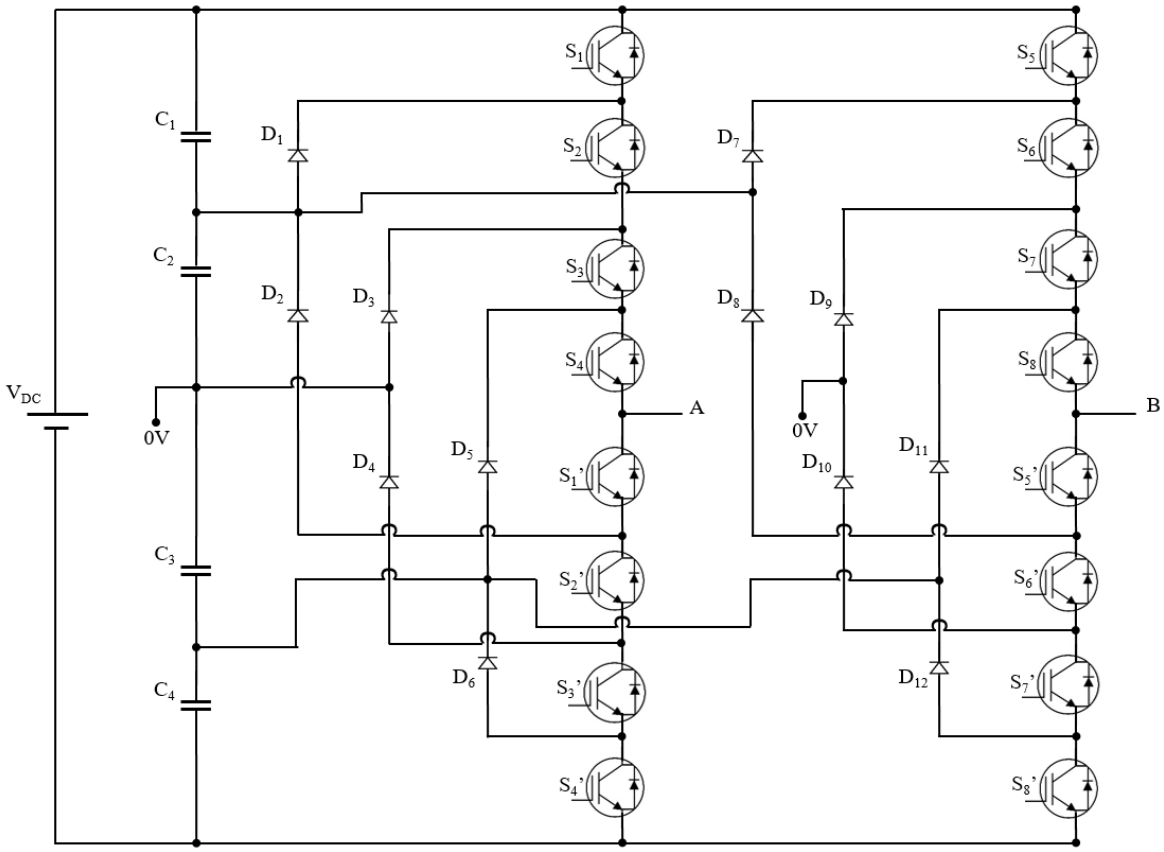

Figure 2.14: 9-level full-bridge single-phase Neutral Point Clamped converter

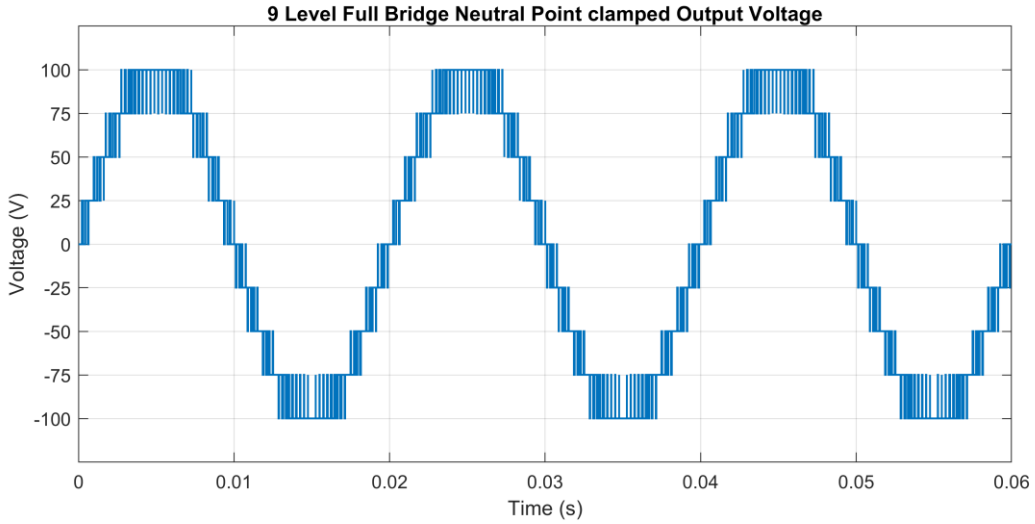

Figure 2.15: Output voltage waveform of 9-level full-bridge Neutral Point Clamped converter

HB and FB configurations are not the only way to construct an NPC converter. It is possible to hybridise multilevel converters as seen in [22], where a CHB and NPC topology are connected in series. It is also possible to operate multilevel converters in an asymmetrical way, where the DC voltage supplying each module varies. This may help to reduce the harmonic content of output without increasing the number of semiconductor devices. The work presented in [23] focuses on a hybrid 7-level Active-NPC and CHB topology, investigating the performance using a Selective Harmonic Elimination (SHE) modulation methodology. In [24], the harmonics performance of a HB 5 and 7-level NPC converter modulated with sinusoidal Pulse Width Modulation (PWM) is studied.

2.2.3 Flying Capacitor Converter

Similar to the NPC converter, the flying capacitor converter (FCC) does not require isolated DC supplies to operate. Capacitors C_1 and C_2 are used to create a split DC link voltage as with the NPC converter. The FCC uses flying capacitors instead of the clamping diodes to create additional output voltage levels. The FCC topology requires 4 switching devices S_1, S_2, S_1', and S_2' for 3-level HB operation. The topology of HB 3-level FCC is presented in Figure 2.16. Due to the increased number of capacitors and no clamping diodes, the capacitor charge balance can be difficult, and needs to be maintained for correct operation of the converter. The voltage across the capacitors needs to be maintained at $V_{DC}/2$ for HB 3-level FCC therefore the output voltage levels are balanced and the switching devices are all under similar voltage stress.

The switching states for a HB 3-level FCC are illustrated in Table 2.6. In order to create the 0V state, there are 2 combinations possible. These to combinations are used to charge or discharge C_3 so the output voltage levels $V_{DC}/2$, 0 and $-V_{DC}/2$ between terminals A and B are created. When the number of levels increases in an FCC topology, there are a higher number of redundant states for each output voltage level, giving the designer increased freedom when maintaining capacitor voltage levels. Although this seems like an advantage, higher output levels mean a higher number of capacitors need to be balanced. Having a higher number of capacitors also reduces the reliability, whilst increasing the cost and volume of this topology. Despite having these drawbacks, the FCC is used in traction applications [25].

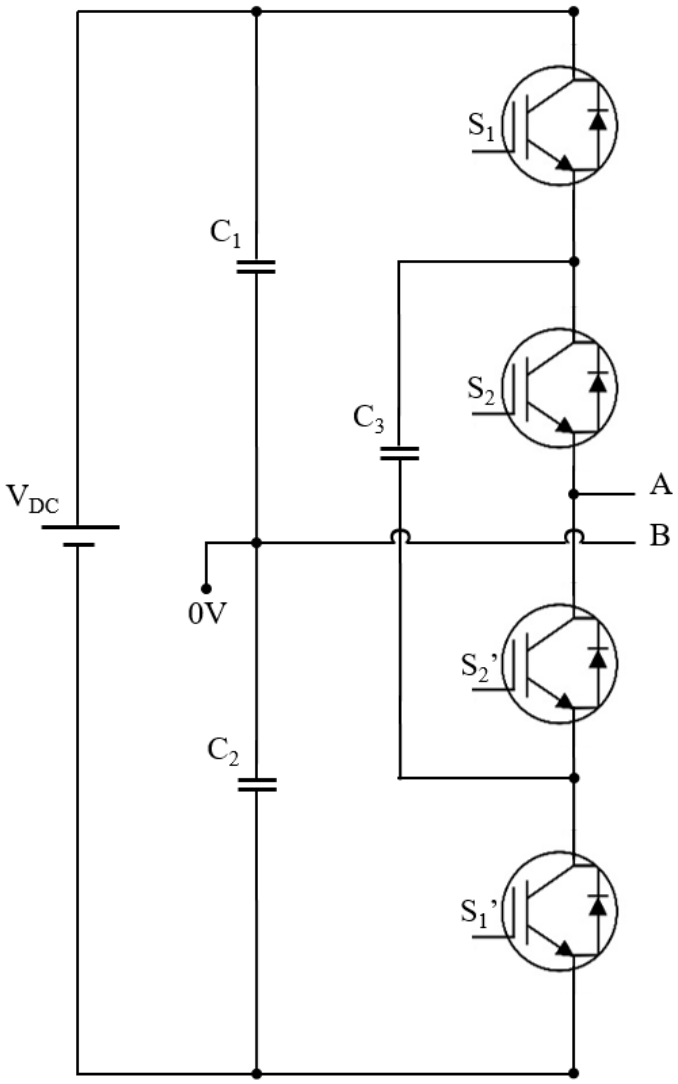

Figure 2.16: 3-level single-phase Flying Capacitor converter

S_1	S_2	S_2'	S_1'	V_{out}
1	1	0	0	$V_{DC}/2$
1	0	1	0	0
0	1	0	1	0
0	0	1	1	$-V_{DC}/2$

Table 2.6: Switching states of 3-level Flying Capacitor converter

The output voltage waveform of a HB 3-level FCC is shown in Figure 2.17. It can be seen that the 3-level output voltage is balanced and transitions between $V_{DC}/2$, 0 and $-V_{DC}/2$.

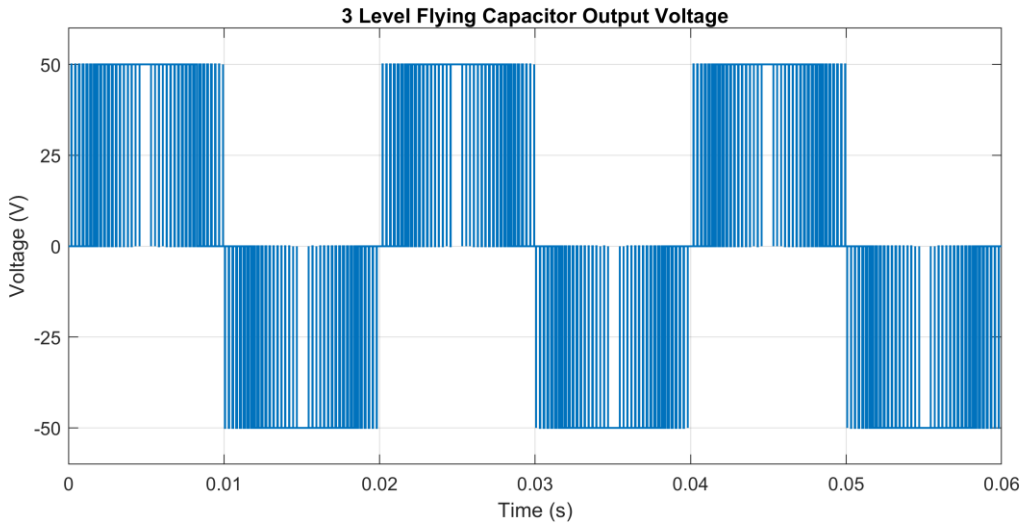

Figure 2.17: Output voltage waveform of 3-level FC converter

Alternatively, an additional leg can be added to the HB 3-level FCC topology to form the full-bridge 5-level FCC. FB 5-level FCC is illustrated in Figure 2.18 and it requires additional flying capacitors, C_3 and C_4.

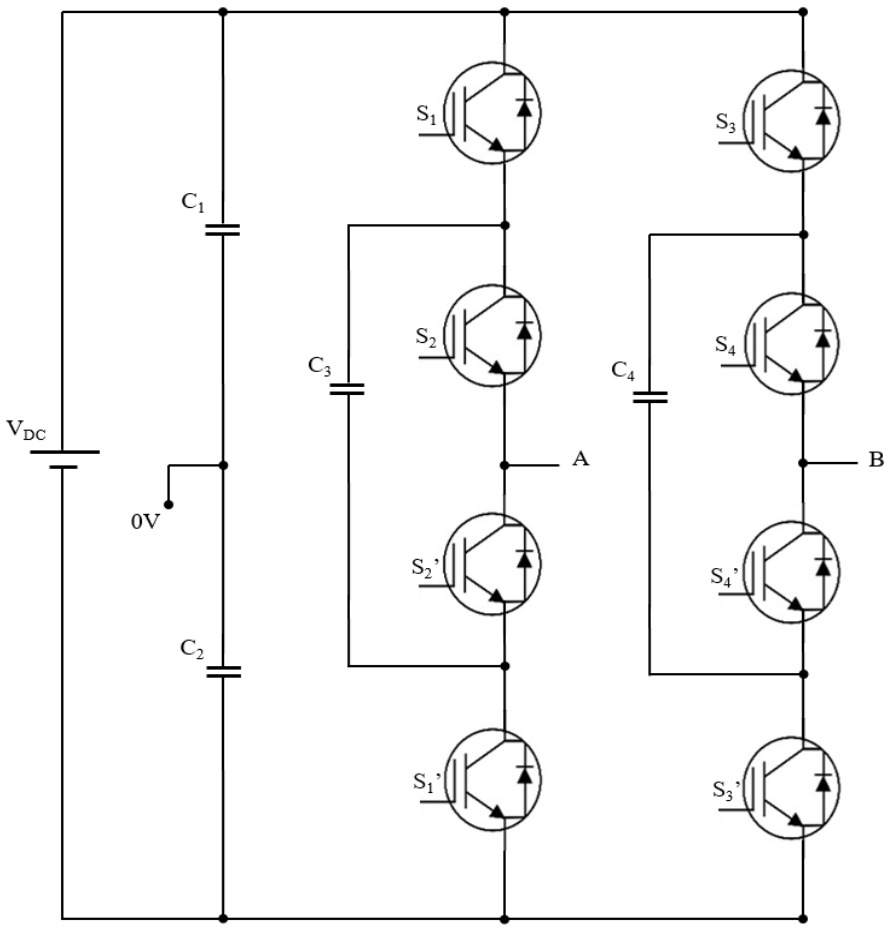

Figure 2.18: 5-level full-bridge single-phase Flying Capacitor converter

The switching states and the output voltage waveform for a FB 5-level FCC are shown in Table 2.7 and Figure 2.19 respectively. As it is a FB topology, the DC link is now fully utilised.

S_1	S_2	S_3	S_4	S_4'	S_3'	S_2'	S_1'	V_{out}
1	1	0	0	1	1	0	0	V_{DC}
1	0	0	0	1	1	1	0	$V_{DC}/2$
0	0	0	0	1	1	1	1	0
0	0	0	1	0	1	1	1	$-V_{DC}/2$
0	0	1	1	0	0	1	1	$-V_{DC}$

Table 2.7: Switching states of 5-level full-bridge Flying Capacitor converter

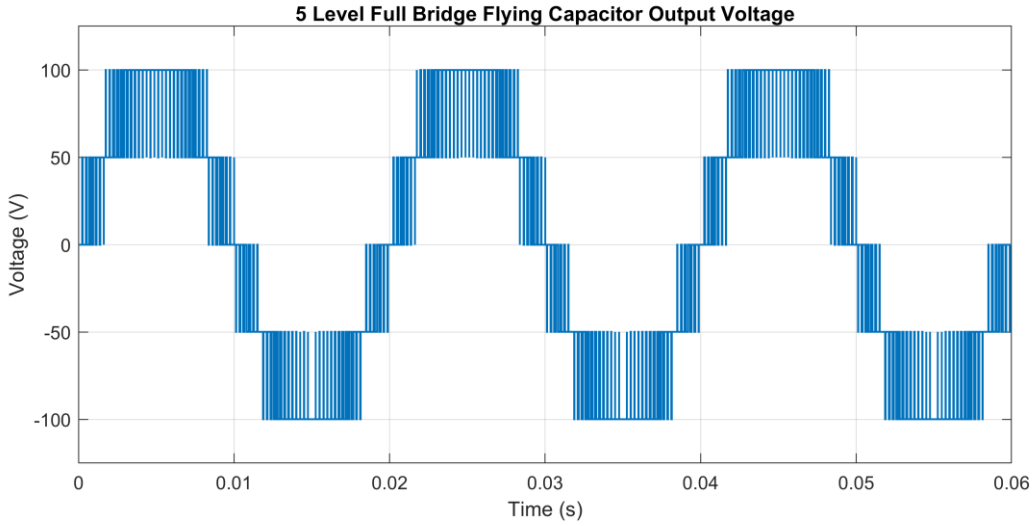

Figure 2.19: Output voltage waveform of 5-level full-bridge Flying Capacitor converter

As in the NPC topology, it is possible to form a HB version of 5-level FCC with additional flying capacitors. The total number of capacitors increases to 10 where 4 of them situated as DC link capacitors and remaining 6 as flying capacitors to create voltage levels $V_{dc}/2$, $V_{dc}/4$, 0, $-V_{dc}/4$ and $-V_{dc}/2$. A HB 5-level FCC topology, its switching states and output voltage waveform are shown in Figure 2.20, Table 2.8 and Figure 2.21 respectively.

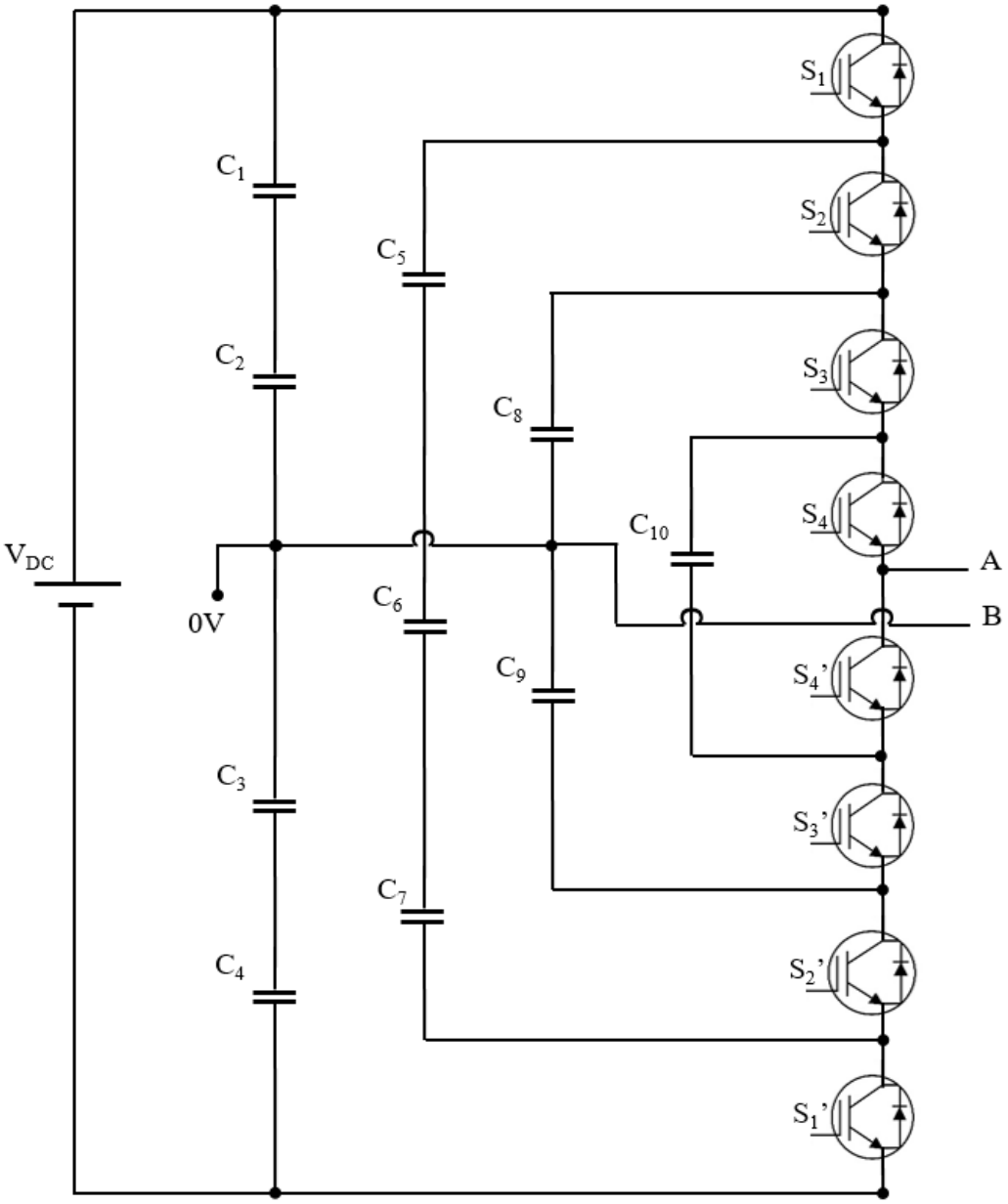

Figure 2.20: 5-level half-bridge single-phase Flying Capacitor converter

S_1	S_2	S_3	S_4	S_4'	S_3'	S_2'	S_1'	V_{out}
1	1	1	1	0	0	0	0	$V_{DC}/2$
1	1	1	0	1	0	0	0	$V_{DC}/4$
1	1	0	0	1	1	0	0	0
1	0	0	0	1	1	1	0	$-V_{DC}/4$
0	0	0	0	1	1	1	1	$-V_{DC}/2$

Table 2.8: Switching states of 5-level half-bridge Flying Capacitor converter

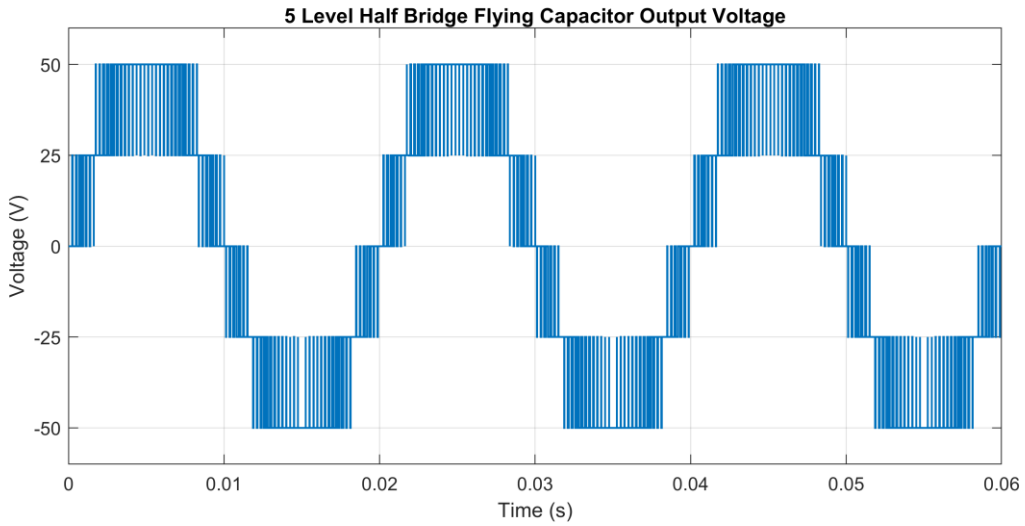

Figure 2.21: Output voltage waveform of 5-level half-bridge Flying Capacitor converter

A 9-level FB topology may be formed by connecting an additional HB 5-level FCC structure as a second leg. The circuitry for the FB 9-level FCC topology and the corresponding output waveform are shown in Figure 2.22 and Figure 2.23 respectively.

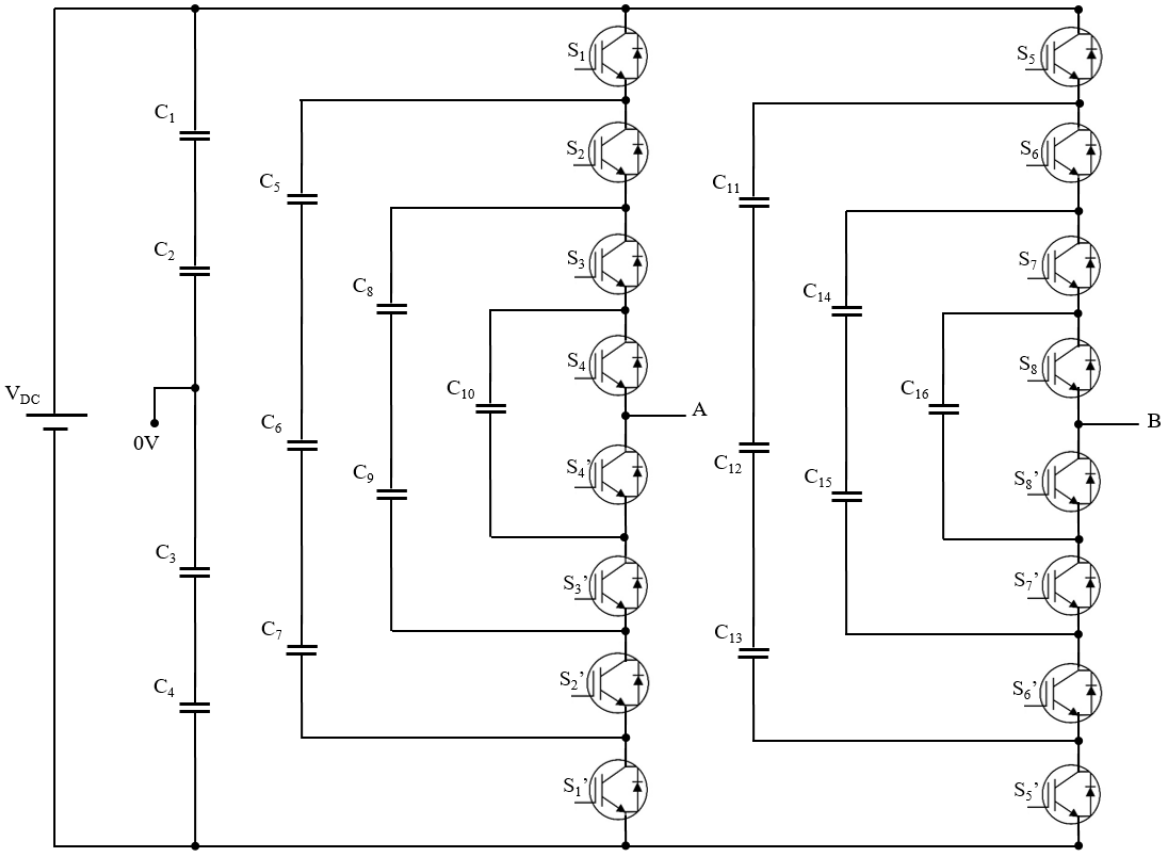

Figure 2.22: 9-level full-bridge single-phase Flying Capacitor converter

Here, 16 capacitors are required for this topology, making it difficult to control the voltage of each capacitor by considering redundant switching states. In Figure 2.23, the positive voltage levels between 0 to $V_{DC}/4$, $V_{DC}/4$ to $V_{DC}/2$, $V_{DC}/2$ to $3V_{DC}/4$ and $3V_{DC}/4$ to V_{DC} are unbalanced at the start of the simulation. Normally each voltage step should be 25V whereas they differ between 13V to 37V. Selecting appropriate switching states is important, as the converter has to balance these levels while providing the anticipated output voltage. It can be seen at the 4th fundamental cycle of the output voltage that the output voltage levels are balanced to 25V each.

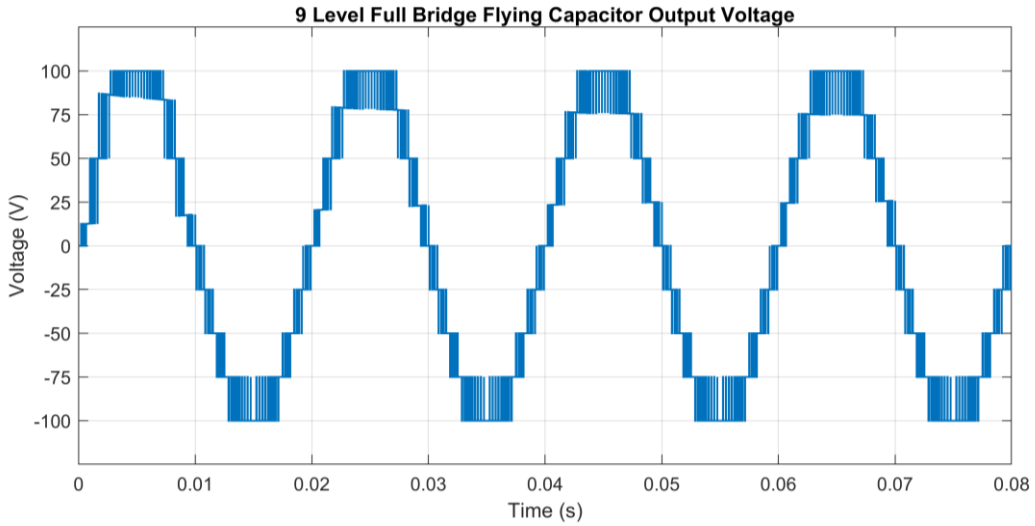

Figure 2.23: Output voltage waveform of 9-level full-bridge Flying Capacitor converter

Capacitor balancing is not possible at V_{DC} and - V_{DC} levels. The research on FCC is mostly focused on understanding the natural balancing of the capacitors during the whole modulation period. An example of this is seen in [26], which is a study on capacitor balancing of a three-phase FCC for an induction motor drive. FCC also requires an axillary pre-charge circuit for charging the capacitors. The literature in [27] presents a 7-level FCC prototype with a pre-charge circuit and power factor correction ability.

2.2.4 Modular Multilevel Converter

The modular multilevel converter (MMC) topology is suitable for high voltage applications due to its highly modular structure [16]. The operation of this converter is then extended for AC/AC and HVDC transmission applications given that unlimited number of modules may theoretically be achievable [28, 29]. The MMC topology consists of submodules having a floating capacitor usually connected to either a half-bridge or a full-bridge, unidirectional

cell, or even a NPC configuration. Considering the number of devices, the half-bridge submodule configuration is the most favourite due to the reduced number of devices leading to lower power loss. Having a floating capacitor at each submodule enables the use of a single DC source, but increases the control complexity. MMCs require an inductor in each arm of converter because circulating current is present during normal operation. These inductors also limit AC fault current between output terminals A and B. Fig. 2.24 illustrates a single-phase 3-level MMC consisting of half-bridges in submodules.

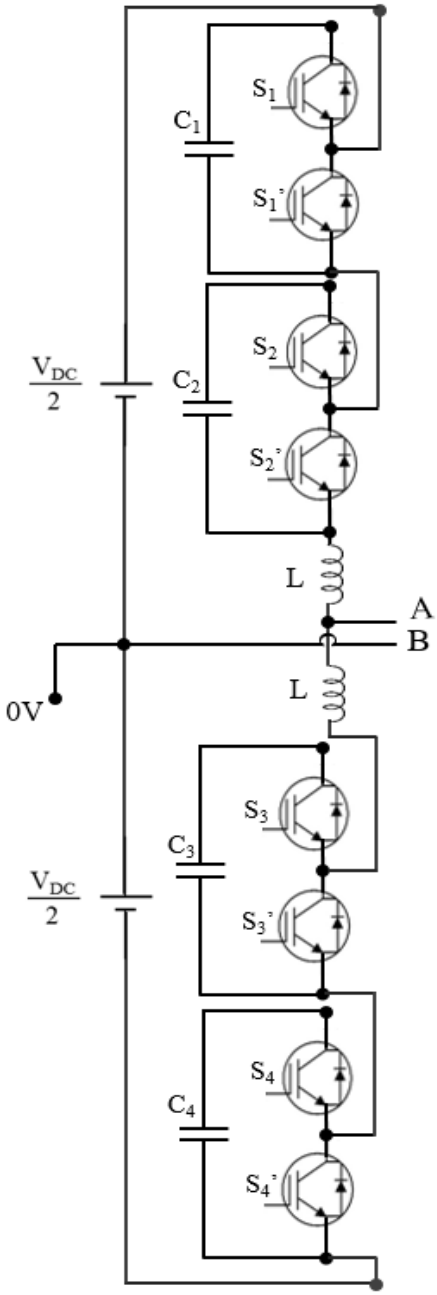

Figure 2.24: 3-level half-bridge single-phase Modular Multilevel converter

Switching top switch 'ON' in a half-bridge submodule leads to generation of positive floating capacitor voltage (i.e. S_1 'ON' & S_1' 'OFF'), the opposite combination results in 0V. The capacitor voltage for each level is determined by dividing DC link voltage to the number of submodules in a converter arm. Conversely, a full-bridge submodule is capable of generating positive, zero and negative output voltage, therefore the operating region of the converter is significantly widened. It is possible to select lower value of DC link voltage compared to the peak value of AC voltage with full-bridge submodules. Some of the switching states for half-bridge 3-level MMC and upper and lower arm voltages are presented in Table 2.9. The output voltage waveforms can be seen in Fig. 2.25.

S_1	S_1'	S_2	S_2'	S_3	S_3'	S_4	S_4'	V_{upper}	V_{lower}	V_{out}
0	1	0	1	1	0	1	0	0	V_{DC}	$V_{DC}/2$
1	0	0	1	0	1	1	0	$V_{DC}/2$	$V_{DC}/2$	0
1	0	1	0	0	1	0	1	V_{DC}	0V	$-V_{DC}/2$

Table 2.9: Switching states of 3-level half-bridge Modular Multilevel converter

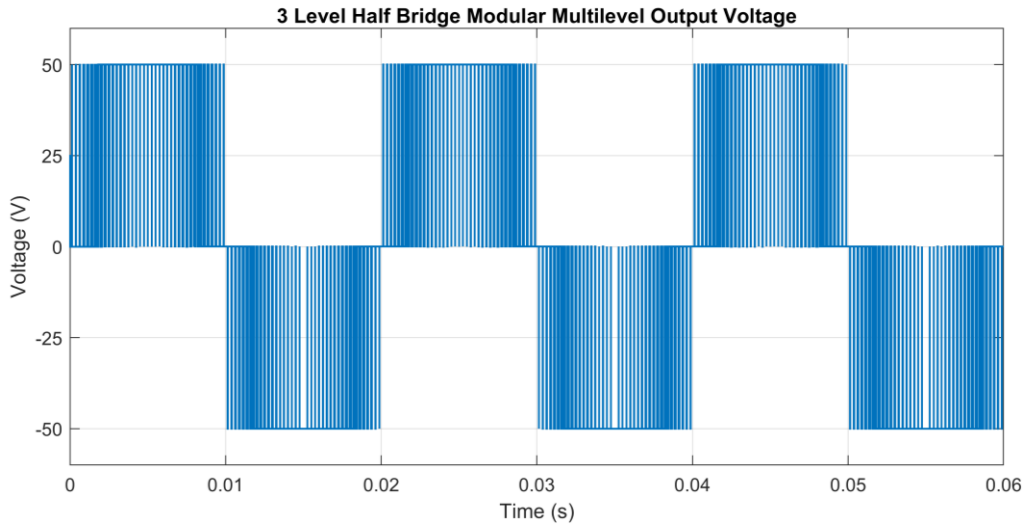

Figure 2.25: Output voltage waveform of 3-level half-bridge Modular Multilevel converter

As mentioned earlier, full-bridge combination of converter legs enables maximum utilisation of DC link voltage. A full-bridge 5-level MMC with half-bridge submodules is illustrated in Fig. 2.26.

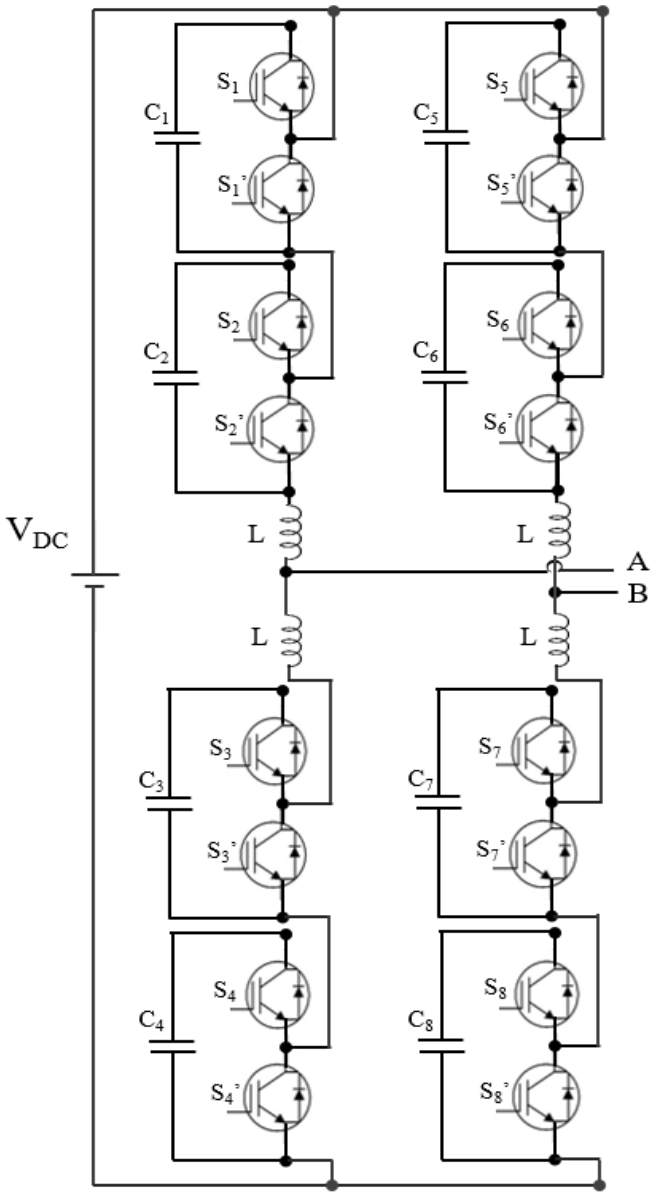

Figure 2.26: 5-level full-bridge single-phase Modular Multilevel converter

The FB 5-level MMC has two converter legs each formed from a 3-level MMC. This topology does not need a split DC link as each output node is connected to the midpoint of each converter leg. A FB 5-level MMC can produce V_{DC}, $V_{DC}/2$, 0, $-V_{DC}/2$ and $-V_{DC}$ output levels. There are many redundant switching states that are used to control the circulating converter leg currents for balancing the voltage of the floating submodule capacitor.

Some of the switching states for the FB 5-level MMC and the equivalent output voltage waveforms are illustrated in Table 2.10 and Fig. 2.27 respectively.

S_1	S_1'	S_2	S_2'	S_3	S_3'	S_4	S_4'	S_5	S_5'	S_6	S_6'	S_7	S_7'	S_8	S_8'	V_{out}
0	1	0	1	1	0	1	0	1	0	1	0	0	1	0	1	V_{DC}
0	1	0	1	1	0	1	0	1	0	0	1	1	0	0	1	$V_{DC}/2$
0	1	0	1	1	0	1	0	0	1	0	1	1	0	1	0	0
1	0	0	1	1	0	0	1	0	1	0	1	1	0	1	0	$-V_{DC}/2$
1	0	1	0	0	1	0	1	0	1	0	1	1	0	1	0	$-V_{DC}$

Table 2.10: Switching states of 5-level full-bridge Modular Multilevel converter

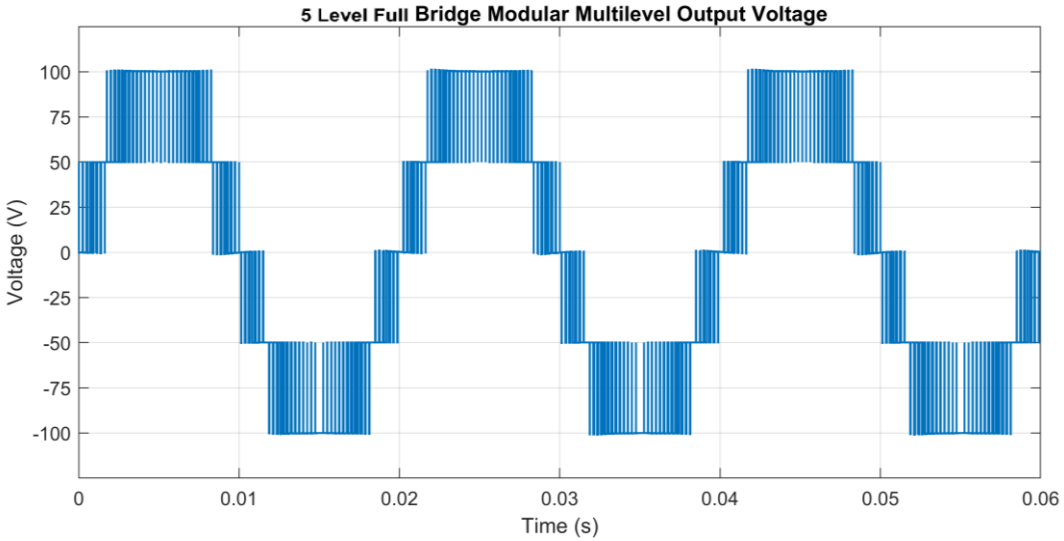

Figure 2.27: Output voltage waveform of 5-level full-bridge Modular Multilevel converter

A leg of an MMC is able to generate $m = (n + 1)$ output voltage levels, where n is the number of half-bridge submodules in a converter arm. A FB 5-level MMC has two converter legs compared to one in a HB 3-level MMC, but the number of submodules in each arm is equal. In contrast, a half-bridge 5-level MMC has one converter leg with double the amount of submodules in an arm. The circuit diagram for this topology can be seen in Figure 2.28. The switching states and output voltage waveform is omitted due to high number of redundant states.

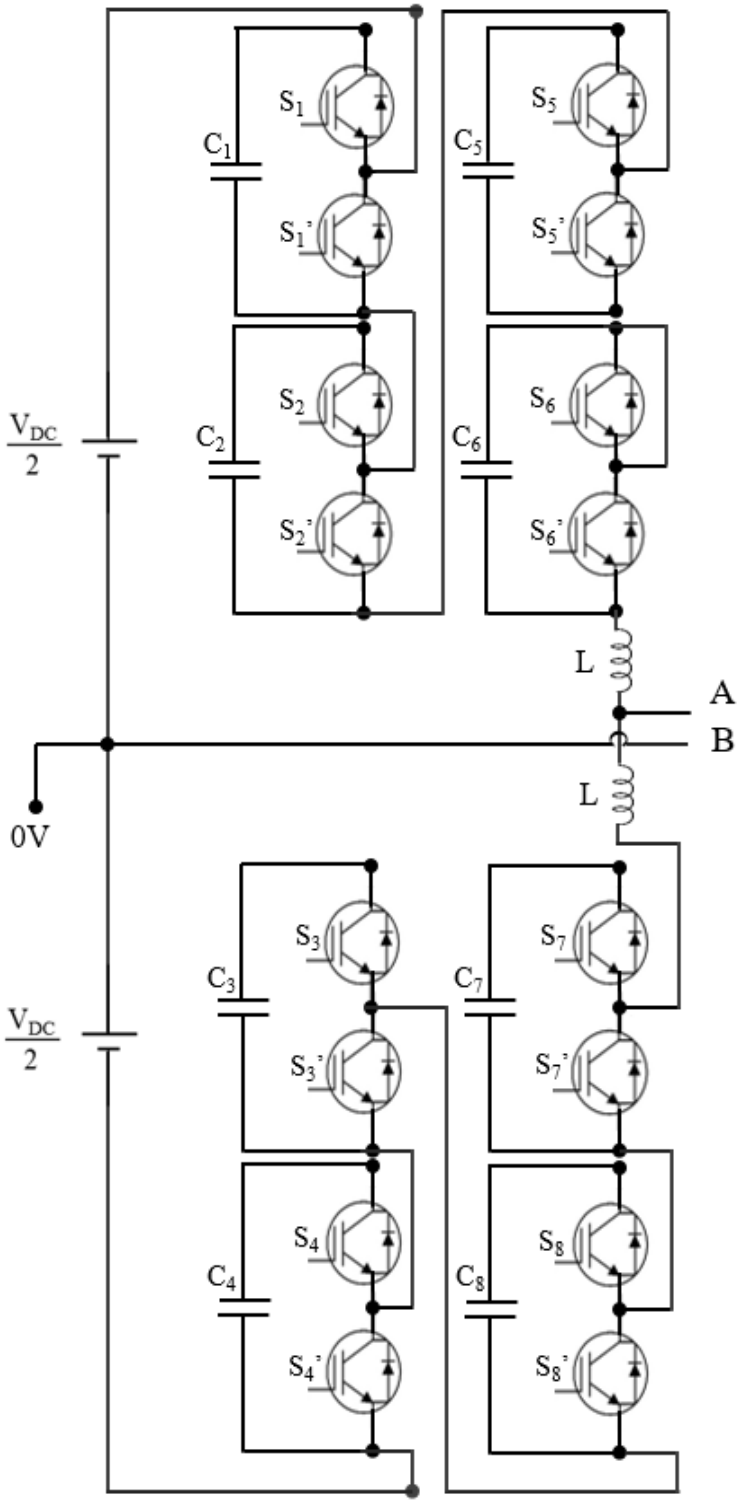

Figure 2.28: 5-level half-bridge single-phase Modular Multilevel converter

This MMC converter does respond well to extending the output voltage levels compared to FCC when it comes to floating capacitor voltage balancing. An example for good scalability may be a 17-level 2 MW early prototype of a MMC from 2004 [30]. With the progression of time, MMC is now generally used in HVDC applications, such as ULTRANET and

INELFE both being 2 GW interconnection in Europe [31, 32]. Although MMC is now widely used in industry, the number of devices compared to other topologies are higher, resulting in high converter volume. Moreover, controlling submodule floating capacitor voltages and requiring several energy management control for circulating current control increases the control complexity, therefore the computational burden.

2.3 Applications of MLCs

Multilevel converters are generally suited for medium to high power applications as switching devices are under low voltage stress. MLCs are commonly selected considering the type of application. Moreover, control algorithms and switching devices of these topologies are also selected considering the type of implementation. MLCs typically use Insulated-gate Bipolar Transistor (IGBT), or Silicon Carbide (SiC) and Gallium Nitride (GaN) switching devices for applications requiring switching frequencies from kHz to MHz range respectively. Some of the most important applications of MLCs are listed below:

I. Power Systems

As discussed in chapter 1, power distribution needs to be maintained and controlled continuously to ensure quality of operation. Conventionally, Flexible AC transmission systems (FACTS), active filters (AFs), static-synchronous compensators (STATCOMs), unified power flow controllers (UPFCs) and dynamic voltage restorers (DVRs) are used in order to provide services for stability, which is also obligated by relevant grid standards [33-36]. Considering harmonic and reactive power compensation applications, NPC, CHB and MMC topologies provide good characteristics, whereas FCC is typically undesirable for reactive power compensation [37]. CHB is often seen as the best topology due to ease of operation, as isolated DC sources do not require voltage balancing when compared to NPC and MMC topologies [12]. It should be noted that MMC may be better suited to high voltage applications as it allows coupling of load to the grid without a transformer.

II. Traction Drives and Marine Propulsion

Train traction applications are in medium voltage range and require high speed drives capable of four quadrant operation. MLCs suit this application as higher switching frequencies are easily achievable to allow faster dynamic response of high-speed drives. NPC and CHB topologies are already presented in literature for this operation [38, 39].

MMC is also used in traction applications to eliminate the 16.7 Hz transformer requirement when connecting European rail supplies with the distribution grid [40].

Marine propulsion is dominated by cycloconverter due to low cost and relatively compact size. It is reported, [41], that the NPC topology can potentially replace existing technologies in the 30 MW range due to improved power quality. There is also an increased interest in multiphase drives due to recent advances in multiphase machines. In [42], a NPC topology is considered as a 3-level five-phase motor drive for propulsion drives. In [43], the dimensioning of a 17-level MMC feeding a 3.9 MW machine is presented.

III. Renewable Generation and Conversion

Although the uptake of renewables in the UK and worldwide increased in the last decade, the suitability of MLCs for this application was being discussed in late 90s. Literature [44] discussed the application of MLCs in PV applications and indicated that NPC and CHB topologies are the most suitable topologies for this application. FCCs are also suitable for this application, but capacitor balancing complicates the control of this topology. The MMC is a less favourable topology as it needs bulky capacitance and complicated voltage and circulating current control mechanisms for correct operation [45]. In wind power applications, the MMC requires less silicon area and DC link energy compared to NPC and CHB [18]. However a MMC as a variable speed drive suffers from high submodule capacitor ripple voltage while operating at low frequencies [46]. MMCs are generally used for connecting offshore wind farms to mainland networks. In contrast, NPC is an accepted topology for wind power applications and a 6 MVA prototype is described in [47].

HVDC operation conventionally achieved by two-level converters consisting of gate turn-off thyristors (GTOs) or series connected IGBTs. The NPC and FCC topologies have issues with voltage balancing and are not suitable for HVDC applications, however a modified NPC topology can be an attractive solution for this type of application due to better power loss distribution in switching devices [48]. As mentioned in section 2.2.4, the MMC is proposed for HVDC applications due to its superior modularity. MMC is also a really good candidate for connecting utility networks with different operating frequencies.

The aforementioned application types of MLCs are widely accepted in industry, in addition they are also used in the automotive industry, regenerative conveyors, class D amplifiers

and energy storage applications. To date, the most important application areas of MLCs, and how likely each topology matches with the application type, is illustrated in Table 2.11.

Topology	STATCOM	Active Filters	FACTS	HVDC	Traction Applications	PV	Wind Power
Cascaded H-bridge	✓✓	✓✓	✓✓	✓	✓✓	✓✓	✓
Neutral Point Clamped	✓	✓	✓	✓	✓✓	✓✓	✓✓
Flying Capacitor	✗	✓	✗	✗	✓	✓	✗
Modular Multilevel	✓	✓	✓	✓✓	✓✓	✓	✓

Table 2.11: Application matching of MLCs

2.4 Comparison of Multilevel Converters

MLCs described in the previous sections are configured in half-bridge (HB) and full-bridge (FB) versions according to the number of converter legs present. A converter with a single leg indicates a HB, whereas 2 leg configuration is a FB topology. Table 2.12, illustrates the component list of the discussed topologies. It is possible to draw two important conclusions from Table 2.12: 1) the number of components is directly proportional with the number of levels, 2) FB leg configuration enables full utilisation of DC link voltage (V_{DC}) and the number of components is generally less for the same number of levels compared to the comparable HB leg configurations. FB configurations however suffers from common-mode voltage characteristics that will be analysed in Chapter 3. It should be noted that as the number of output voltage levels increases, the number of 'ON' state switching devices depends on modulation method, and may vary in each switching state. The voltage drop of these switching devices may unbalance each generated voltage step, causing problems at low voltage amplitude.

The FCC topology requires a lower component count when compared to NPC and MMC topologies in a FB 5-level configuration, however the volume of floating capacitors, reliability and type of application is limited. Conversely, the MMC requires the highest component count when compared to others, making it expensive and bulky for domestic scale applications. As a result, these topologies are not selected.

The CHB requires the least components compared to all other topologies, including no extra clamping diodes and floating capacitors. Considering total cost and volume of the converter, this forms an advantage compared to other topologies. It should be noted that the CHB requires isolated DC sources, which may be very suitable for battery and PV applications.

Topology	Output Voltage Levels	Converter Legs	DC Link Utilisation	DC-Link Capacitors	Number of Switches	Clamping Diodes	Floating Capacitors
Cascaded H-bridge	3	2	V_{DC}	1	4	0	0
	5			2	8		
	9			4	16		
	15			7	28		
Neutral Point Clamped	3	1	$\frac{V_{DC}}{2}$	2	4	2	0
	5	2	V_{DC}	2	8	4	
	5	1	$\frac{V_{DC}}{2}$	4	8	6	
	9	2	V_{DC}	4	16	12	
Flying Capacitor	3	1	$\frac{V_{DC}}{2}$	2	4	0	1
	5	2	V_{DC}	2	8		2
	5	1	$\frac{V_{DC}}{2}$	4	8		6
	9	2	V_{DC}	4	16		12
Modular Multilevel	3	1	$\frac{V_{DC}}{2}$	2	8	0	4
	5	2	V_{DC}	0	16		8
	5	1	$\frac{V_{DC}}{2}$	2	16		8
	9	2	V_{DC}	0	32		16

Table 2.12: Component comparison of MLCs

Table 2.13, shows a comparison of MLCs regarding the implementation factors such as modularity, fault tolerance and control properties [3]. The CHB being the only topology not having voltage balancing or start-up problems as it utilises isolated DC supplies. This makes the CHB easier to control compared to other topologies. Highly modularised converters tend to dynamically react better to a fault in a specific module by bypassing the faulty module from the current path.

Topology	Control Difficulty	Control Complexity	Fault Tolerance	Modularity
Cascaded H-bridge	Power sharing	Medium	High	High
Neutral Point Clamped	Voltage balancing	Medium	Low	Low
Flying Capacitor	Start-up Voltage	High	High	Low
Modular Multilevel	Voltage balancing	Very high	High	Very high

Table 2.13: Comparison of MLCs depending on implementation factors

2.5 Modulation Techniques for MLCs

The research into modulation methods of multilevel converter has always been a popular topic in literature [5, 6, 11, 49-51]. The main drivers for this are: 1) the desire to extend conventional two-level modulation techniques to the multilevel operation, 2) the number of high redundancy of switching states giving multi-degrees of freedom with the switching, 3) the complexity of floating capacitor balancing, and 4) the need to suppress negative effects of common-mode voltage. Traditionally, MLCs had lower output voltage levels due to the requirement of high number of integrated circuits that used as analogue modulator. The advancements in digital signal processors (DPS) and field programmable gate arrays (FPGA) made it easier to process more complex algorithms.

High switching state redundancy in MLCs enables modification of traditional modulation methods, creating unique techniques for specific applications. In order to analyse MLC modulation techniques, it is important to divide them into two main categories regarding their operation domain. From Figure 2.29, space vector based algorithms use the state space vector domain whereas voltage level based algorithms are based on generation of voltage levels within a time period, in other words time domain [3]. In some literature, MLC modulation methods are categorised depending on the switching frequency but in Figure 2.29, the colours represent this information. High switching frequencies generally provide higher quality output waveforms and are more suitable for applications requiring high dynamic response. In contrast, low switching frequency techniques are more suitable for high power MLCs due to reduced switching losses.

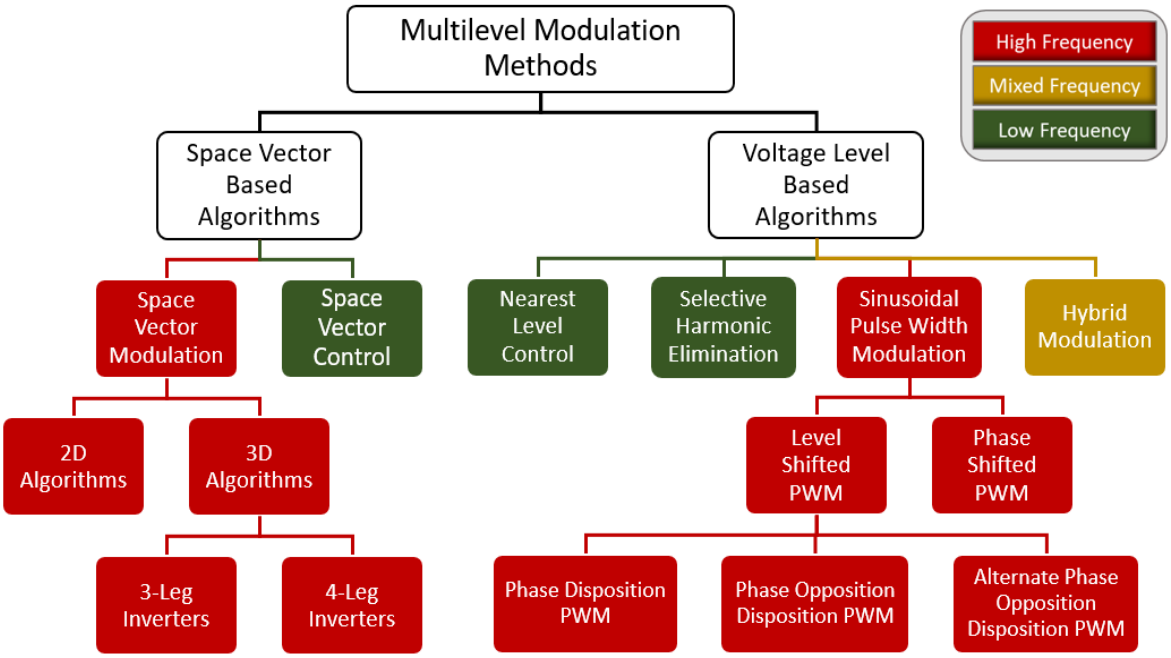

Figure 2.29: Multilevel converter modulation methods

Some of the most used modulation techniques for MLCs are discussed in the next sections. These are space vector modulation (SVM), selective harmonic elimination (SHE), nearest level control (NLC) and sinusoidal pulse width modulation (SPWM).

2.5.1 Space Vector Modulation

Space vector modulation (SVM) is conventionally applied to 3-phase 2-level converters as it is possible to use an AC reference voltage in the stationary reference frame ($\alpha\beta$ frame) in order to generate switching states. This regularly sampled technique directly determines the line voltages of a converter and can also be used in the over-modulation region. SVM design involves the definition of output vectors, separation and boundary identification of a space vector plane, and finally switching sequence definition. SVM techniques can reduce switching losses, however implementation to MLCs becomes more difficult as the number of voltage levels increases due to high number of redundant switching states. In a 3-phase m-level MLC modulated with SVM, m^3 switching states are present.

In [52], an algorithm is introduced for an m-level 3-phase converters that can efficiently computes the switching states, independent of the number of levels. SVM is closely related with level shifted pulse width modulation methods (LSPWM). In [50], this relation is shown for MLCs by injecting an optimised zero sequence component into the modulation pattern. It is also reported that this method better utilises the DC link, and produces a less

harmonically distorted output waveform. In contrast, the same modulation method introduces common-mode component, therefore alternatives such as [53] are proposed for the SVM technique that effectively supresses leakage current in a 3-phase MLC.

2.5.2 Selective Harmonic Elimination

Selective harmonic elimination (SHE) modulation is proposed for reducing the THD content of the output voltage waveform. Traditional methods involve finding an analytical solution for the commutation angle of switches by using Fourier series. Applying this, targeted reduction in specific harmonic content can be achieved. Finding an analytical solution of a system with nonlinear transcendental equations consisting of trigonometric terms is difficult, and requires approximation methods such as Newton Raphson. This can be achieved by analysing steady state equations in an offline environment. As a result, SHE algorithms are generally limited to open loop or low dynamic range applications. It should also be noted that the number of equations exponentially rises with increasing voltage levels in an MLC. In [51], SHE is applied to a 5-level CHB where a simulation study is also provided for an 11-level converter. Moreover, in [54] a generalised formula for MLCs is presented, where experimental results for single and three-phase systems up to 7-level operation are given. A real-time SHE algorithm is proposed and experimentally validated with a 150kVA 3-level NPC to obligate relevant grid codes in [55].

2.5.3 Nearest Level Control

Nearest Level Control is proposed for MLCs with high voltage levels due to easier implementation compared to other techniques. The given voltage reference is discretised before an upper and lower rounded value to the next integer voltage level is determined. Generally, a sawtooth signal is used to switch the output between the upper and lower rounded value in order to generate the correct output voltage level. MLCs that are used in high power applications with a high number of voltage levels tend to use this approach, as switching devices have fewer commutations in a fundamental period therefore reducing switching loses. This method can be sampled regularly or variably depending on the application. Literature [56] studied the impact of sampling frequency on harmonic distortion and found critical minimum and maximum values for uniform sampling. A simplified NLC voltage balancing method for MMC is proposed in [57], where the process of submodule selection made easy, therefore the method could lead to 60% memory and computational time reduction compared to the conventional algorithms. In an experimental study, a

modified NLC method is proposed where the number of AC output voltage levels has doubled compared to conventional NLC, leading to better harmonic spectrum with reduced switching frequency [58].

2.5.4 Sinusoidal Pulse Width Modulation

Sinusoidal pulse width modulation (SPWM) is conventionally applied by analogue oscillators and comparators. Gate signals for switching devices are achieved by comparing a sinusoidal voltage reference to a triangular or sawtooth carrier waveform. This method is extended to MLCs and widely accepted and studied due to its ease of implementation [59]. For an m level MLC, $(m-1)$ carrier waveforms are required. The amplitude of the reference value, and carriers, are generally normalised and the carrier frequency must be higher than the fundamental frequency. There are many SPWM methods available in literature and they are mainly divided into three categories depending how the carrier waveforms are arranged:

I. Level Shifted Pulse Width Modulation

In level shifted pulse width modulation (LSPWM) the carrier waveforms have a peak-to-peak amplitude of $2/(m-1)$, where all carriers must be at same frequency. All carriers are stacked on top of each other between the normalised maximum and minimum points (1 to -1) of the reference sinusoid waveform. LSPWM has different forms where carriers have different phase properties compared to each other:

- Phase Disposition Pulse Width Modulation (PDPWM). All of the carrier waves are in phase with each other. See Figure 2.30.
- Phase Opposition Disposition Pulse Width Modulation (PODPWM). Carriers in positive plane (1 to 0) are in phase whereas carriers in negative plane (0 to -1) are out of phase by 180^o compared to positive plane carriers. See Figure 2.32.
- Alternate Phase Opposition Disposition Pulse Width Modulation (APODPWM). Carrier next to each other are 180^o out of phase. See Figure 2.34.

Although LSPWM generate good harmonic content for the output voltage waveform, the power sharing in each module and the number of commutations per switch are not balanced when used with a CHB converter. In order to balance these out, it is possible to either rotate carriers within an allocated time or geometrically modify the reference sinusoid.

The following figures (Figures 2.31, 2.33, 2.35 and 2.37) illustrating harmonic spectrums are simulations of a 9-level CHB. Aforementioned conditions of 50 Hz fundamental frequency (f_{fund}) and 1 kHz switching frequency (f_{sw}) are used for these simulations. Modulation index is 1, and also there is no output filter for all simulations.

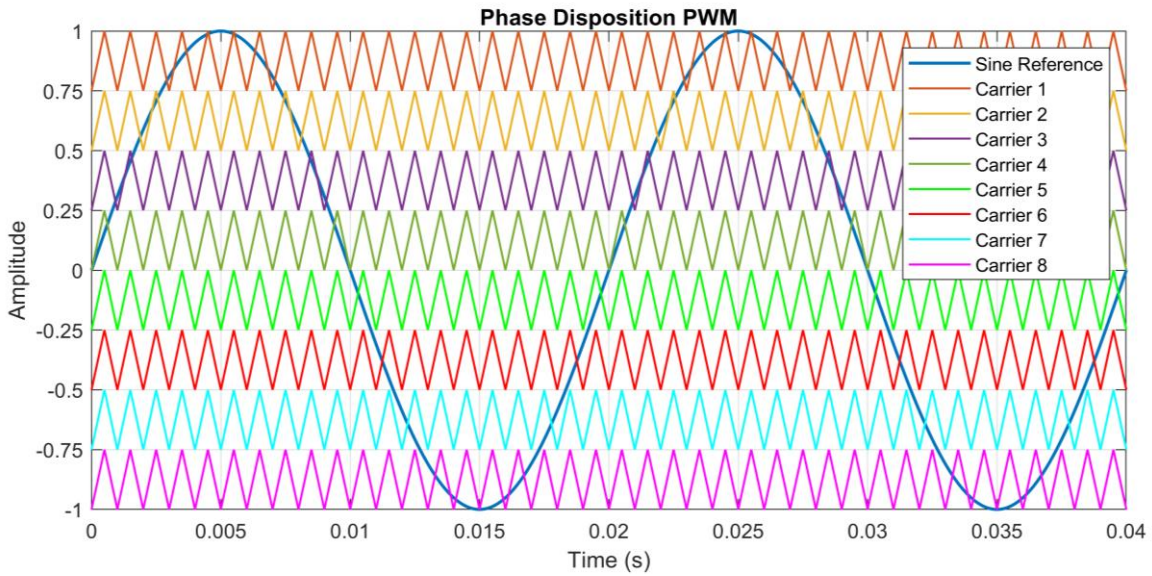

Figure 2.30: Phase disposition PWM carrier waveforms for 9-level MLCs.

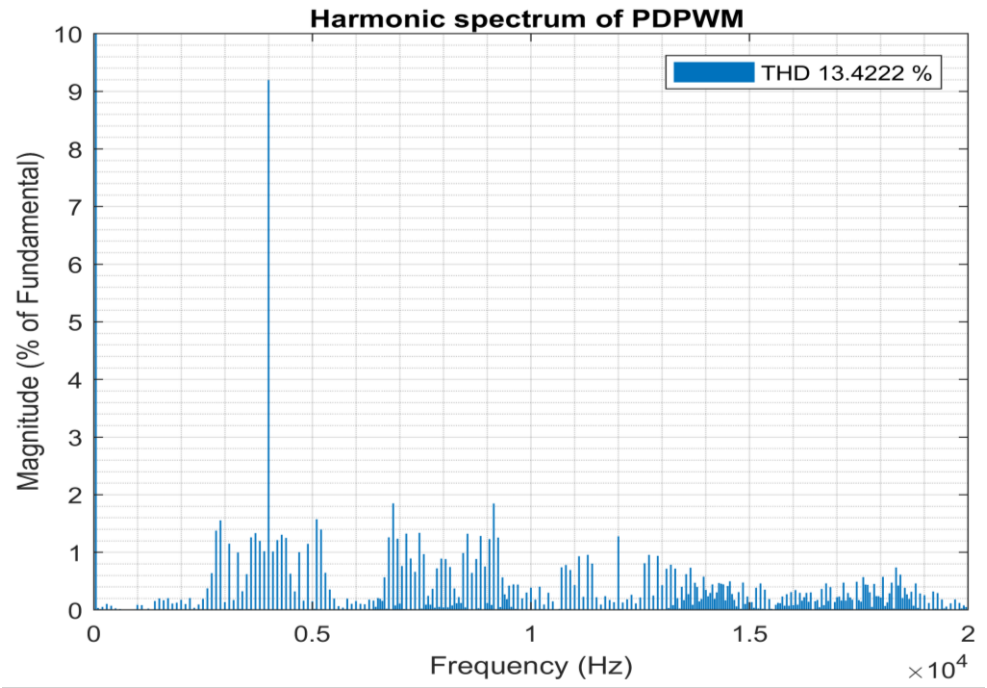

Figure 2.31: Harmonic spectrum of phase disposition PWM for 9-level CHB

It can be seen that switching frequency harmonic is dominant and the THD is 13.42%. Also, even sidebands of f_{sw} is supressed under 2% of the fundamental component.

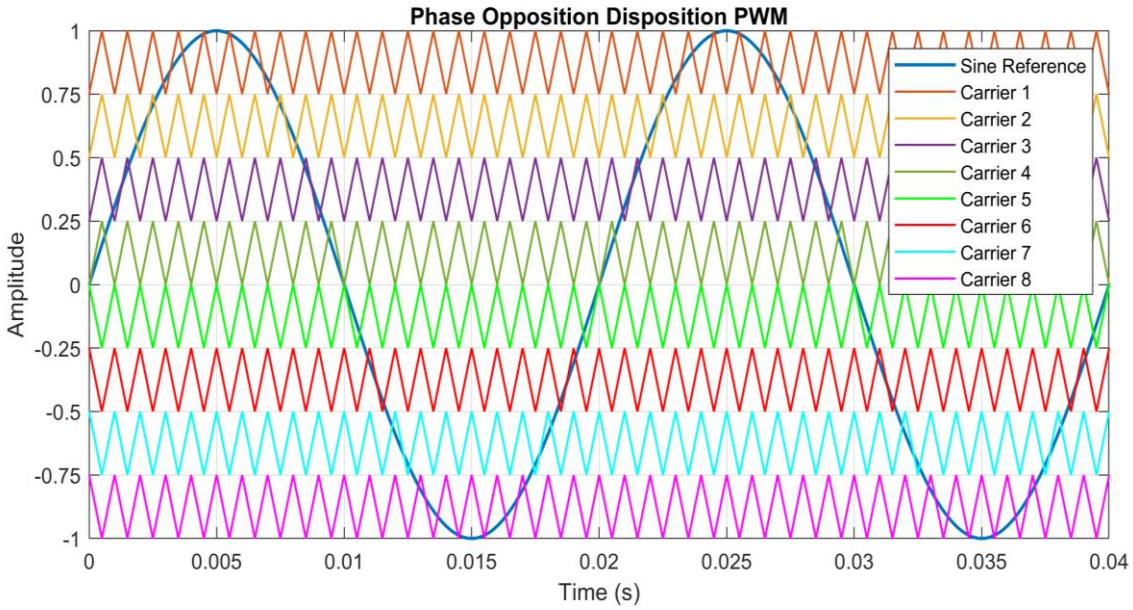

Figure 2.32: Phase opposition disposition PWM carrier waveforms for 9-level MLCs

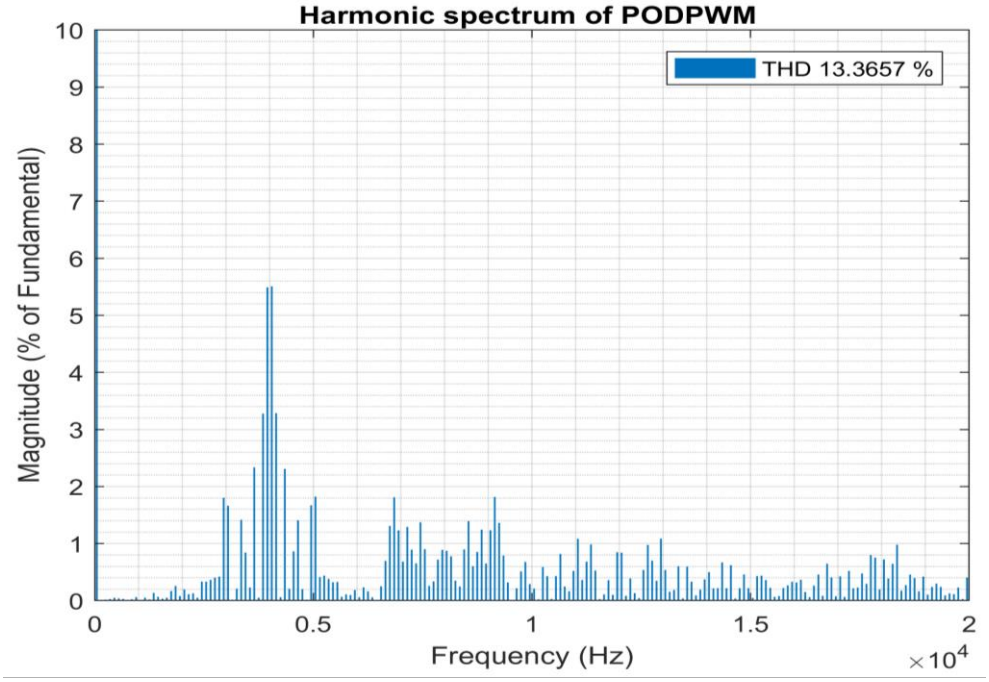

Figure 2.33: Harmonic spectrum of phase opposition disposition PWM for 9-level CHB

In PODPWM, switching frequency band and even sidebands are missing whereas the first odd sidebands have a magnitude of 5.5% of the fundamental component. THD is 13.37% which is slightly better than PDPWM.

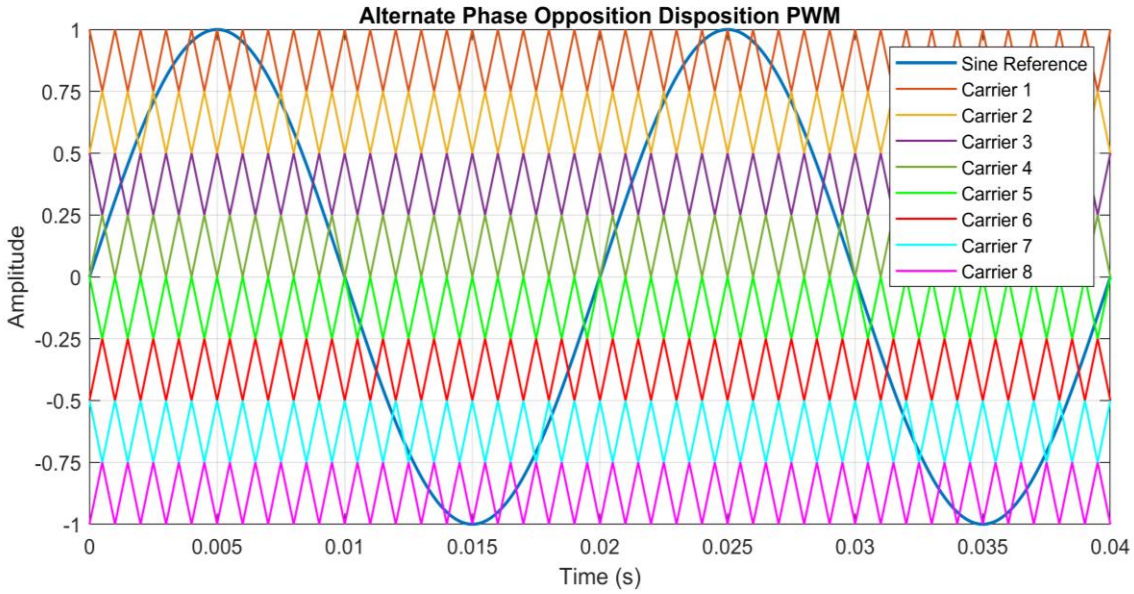

Figure 2.34: Alternate Phase Disposition PWM carrier waveforms for 9-level MLCs

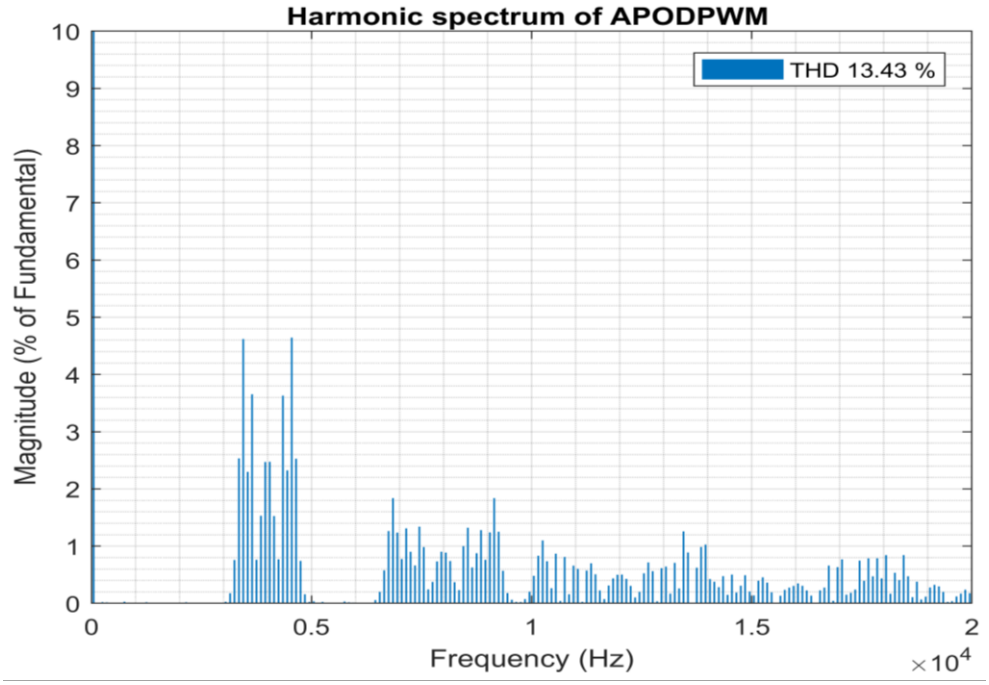

Figure 2.35: Harmonic spectrum of alternate phase opposition disposition PWM for 9-level CHB

In APODPWM, switching frequency component and even sidebands are missing. The dominant frequencies are odd sidebands that are situated further away from the switching frequency. 11^{th} sidebands of f_{sw} have the highest magnitude of 4.6% of the fundamental component. The THD is 13.43% which is very close to PDPWM.

II. Phase Shifted Pulse Width Modulation

Phase shifted pulse width modulation (PSPWM) works by phase shifting carriers for MLC operation. In contrast to LSPWM, all carriers have same magnitude. The required number of carriers are again $(m-1)$, where m is the number of output voltage levels. If n is the number of modules in a CHB, therefore each carrier needs to be shifted by $1/2nf_{sw}$ in time domain. The switching frequency is 125 Hz for better visualisation. Figure 2.36 illustrates carrier waveform for a 5-level CHB modulated with PSPWM.

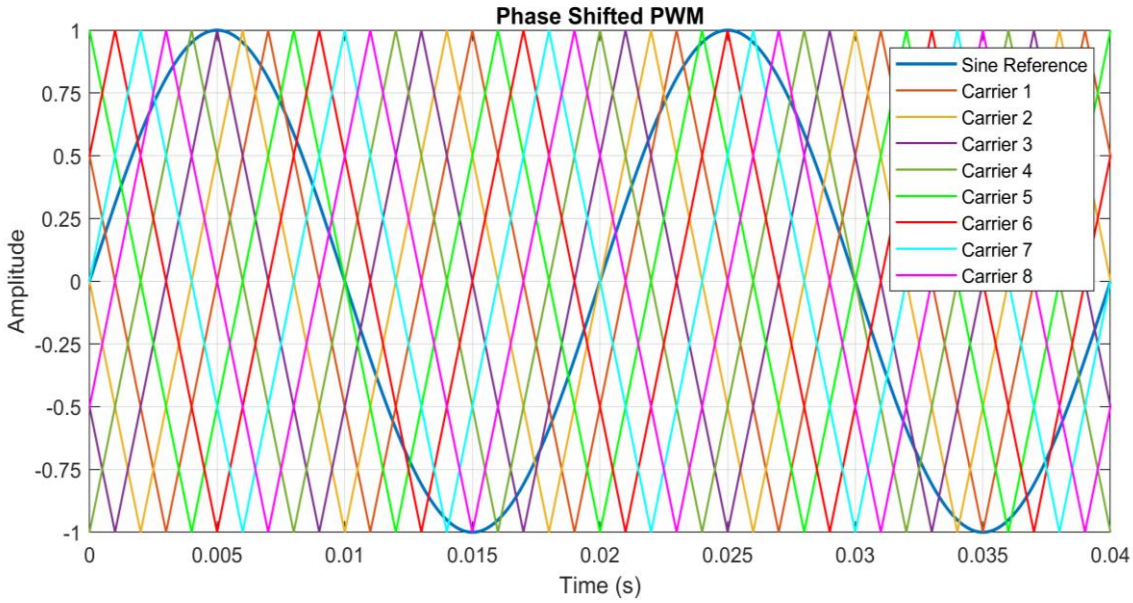

Figure 2.36: Phase Shifted PWM carrier waveforms for 9-level MLCs

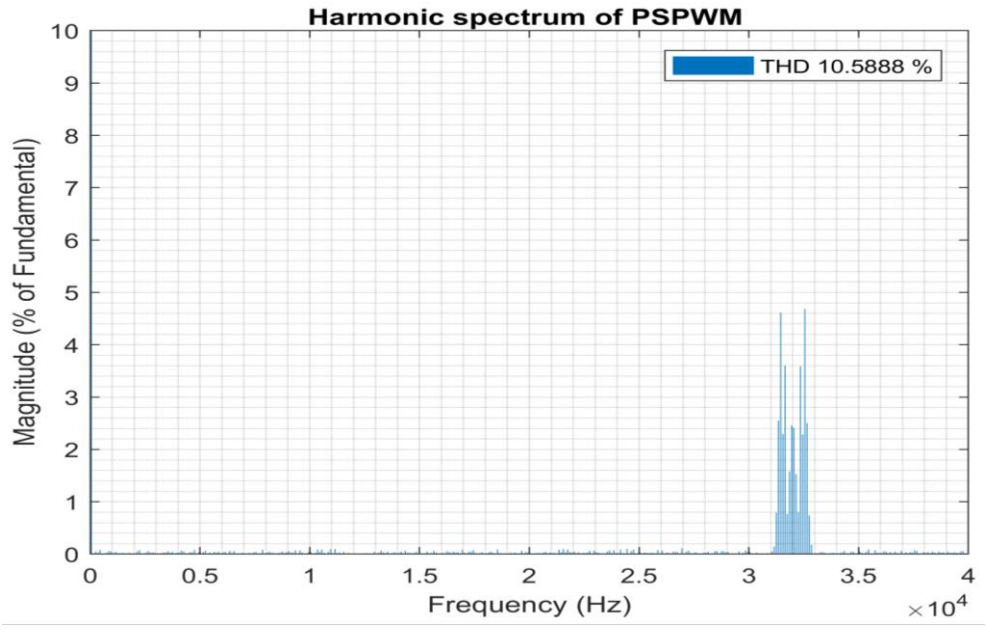

Figure 2.37: Harmonic spectrum of phase shifted PWM for 9-level CHB

PSPWM naturally balances the power drawn from each module. The number of commutations per switch in a fundamental cycle is similar therefore the chance of failure due to switching is equal. Figure 2.37 represents the harmonic spectrum of PSPWM with 4 kHz switching frequency. It can be seen that the dominant frequencies are at $2nf_{sw}$. The THD of this method is 10.59%, which is better than LSPWM. It should be noted that the effective switching frequency at the output waveform due to phase shifting is equal to nf_{sw}, resulting in lower THD.

III. Hybrid Pulse Width Modulation

Hybrid pulse width modulation HPWM is a mixture of level and phase shifting. This method is configurable to any MLC with 5 output voltage levels or more. Figure 2.38 illustrates a method for 9-level CHB where 4 different levels are present and each level contains 2 phase shifted carriers. Hybridisation of LSPWM and PSPWM allows benefiting from advantages of both techniques.

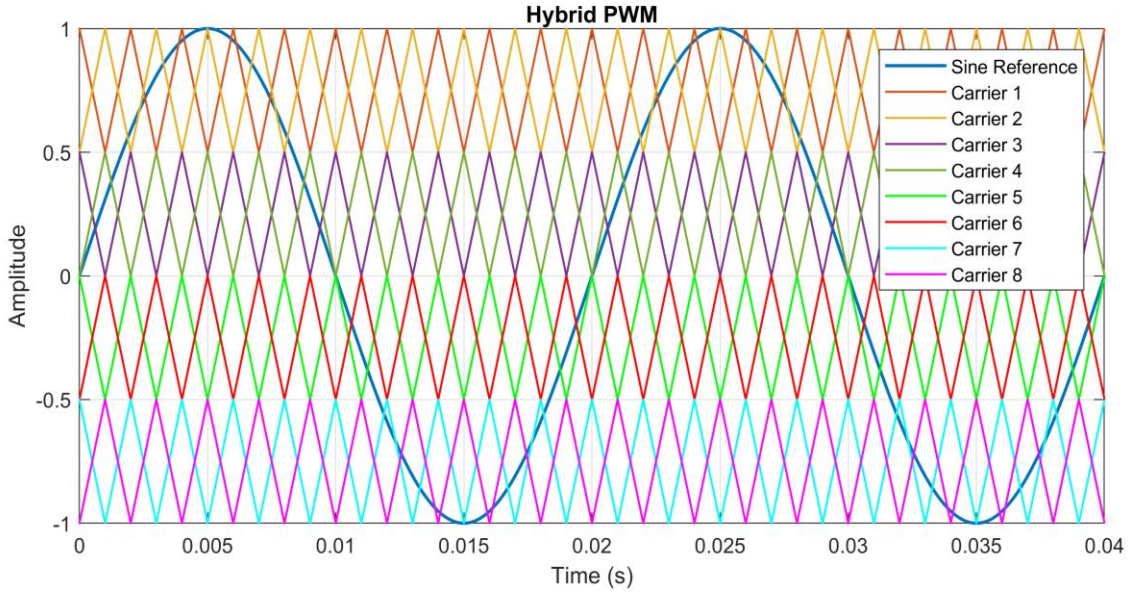

Figure 2.38: Hybrid PWM carrier waveforms for 9-level MLCs

Figure 2.39 shows the harmonic content of 9-level hybrid PWM technique for CHB converters. Phase shifting 2 carriers at same level pushed the dominant frequencies to $2f_{sw}$ and its multiples. The main switching frequency band is suppressed when compared to PDPWM and the THD values is 13.02%, which is expected when comparing LSPWM and PSPWM techniques.

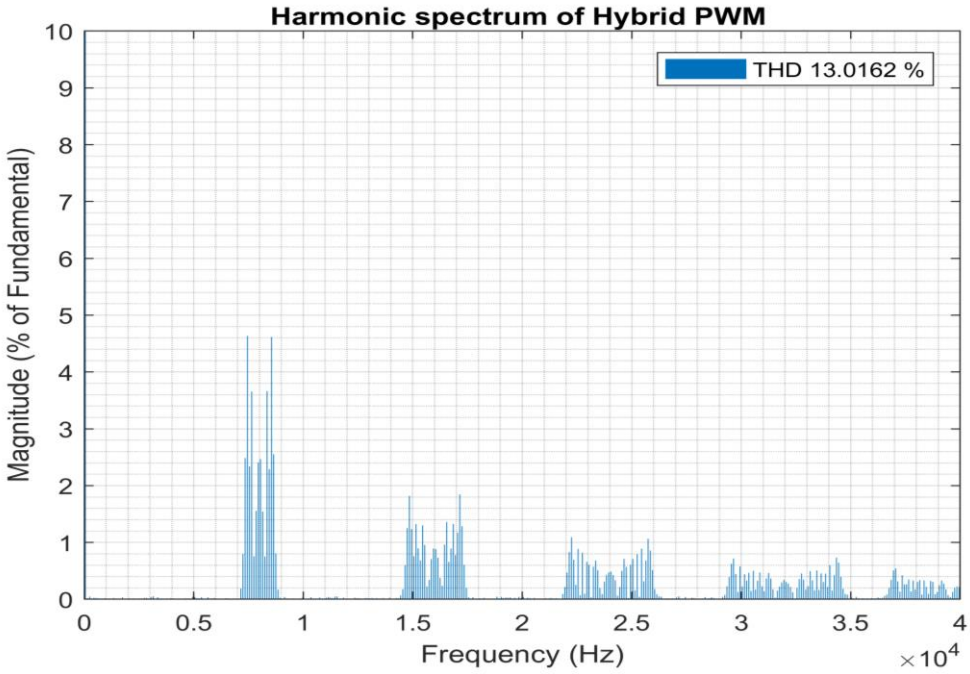

Figure 2.39: Harmonic spectrum of hybrid PWM for 9-level CHB

2.6 Chapter Summary

This chapter focused on multilevel converter topologies, their application and modulation strategies. Neutral point clamped, flying capacitor, cascaded H-bridge and modular multilevel converter topologies are discussed. The work embodied in this thesis is focused on grid-tie renewable energy and storage applications. Looking at applications and comparisons of MLCs, cascaded H-bridge topology provides the most viable and promising solution. CHB converter requires isolated DC sources, and fewer components are required compared to all other topologies. As this study is focused on grid-tie PV and battery applications, all the DC sources are isolated. Considering the other technologies, NPC is also a promising technology for domestic scale grid-tie applications but CHB provides higher accessibility to the batteries at their second life applications and has the added advantage of enabling implementation of modular maximum power point tracking (MPPT). Moreover, the FCC topology has limited applicability due to the requirement of huge number of capacitors. This makes this topology less reliable, costly and bulky compared to others. Finally, the MMC topology requires submodule capacitor balancing and suffers from circulating currents therefore the control is marginally more difficult than CHB topology and does not benefit the application at domestic scale.

The chapter shows that MLCs provide better output voltage waveforms by providing a better approximated sinusoid due to staircase operation. This leads to less filtering requirement, reduction of harmonics and reduced voltage stress on switching devices. Converter control and modulation techniques define the quality of output power and its stability. As a result of this, converter modulation techniques including space vector modulation, selective harmonic elimination, nearest level control and sinusoidal pulse width modulation methods are discussed. The effects of modulation methods and how it can be modified for common-mode voltage suppression will be detailed in Chapter 3.

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Chapter 3
Leakage Current in Transformerless Converters

3.1 Introduction

Grid-tie converters can be classified into two groups depending on the electrical isolation between the DC and the AC side of a converter: isolated or non-isolated. Usually, in isolated converters, a high frequency transformer appears at the DC side of the converter (Figure 3.1(a)), or a fundamental frequency transformer is used at the AC side of the converter, to provide the required galvanic isolation (Fig. 3.1(b)) [1]. A number of papers [2-5] discuss the efficiency of converters with galvanic isolation, showing this tend to be 1-2% lower when compared to the non-isolated converters. Moreover, high cost, size and weight of the transformers are the other aspects that encourage industry towards the implementation of transformerless topologies (Figure 3.1(c)). Transformers are conventionally used for preventing ground faults and reducing DC current injection to the AC utility in grid-tie systems, however technological advancements have made it is possible to address these issues within transformerless converters.

Countries have different regulations or standards for the grid-tie converters deployments. The sections relating to the use of transformers isolations generally specify and limit the DC current injection to the grid, and in some countries (United States) also obligate the use of galvanic isolation. Lack of galvanic isolation may create a common-mode circuit, which enables the leakage current to flow through parasitic capacitances to the ground [6-8]. The leakage current deteriorates system performance, reduces efficiency and causes electromagnetic interference (EMI) problems between components [9]. Additionally, high current flowing to ground is a safety concern that may cause electrocution, therefore needs to be addressed.

This chapter discusses transformerless converter topologies, showing how leakage current occurs due to common-mode voltages. Conventional leakage current suppression methods are described, their effectiveness is discussed, and a method for eliminating leakage current for a cascaded H-bridge (CHB) converter is presented.

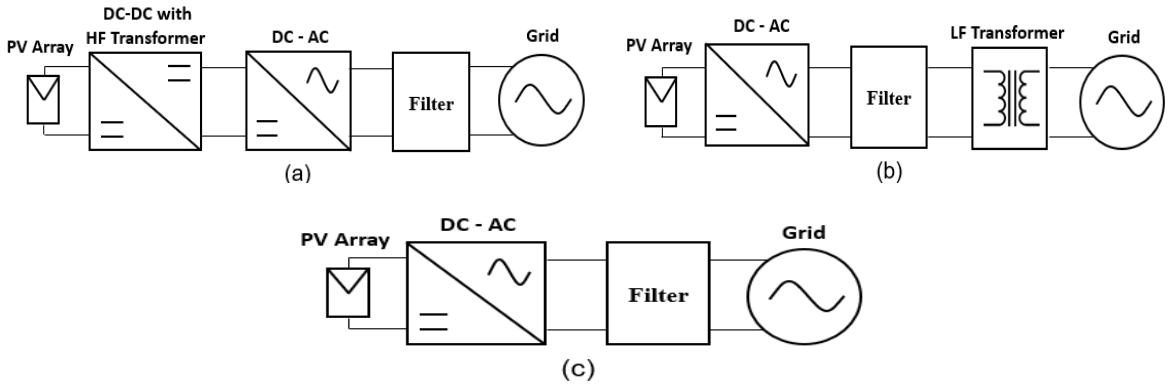

Figure 3.1: Grid-tie PV inverters (a) with high frequency galvanic isolation, (b) with low frequency galvanic isolation, (c) without galvanic isolation.

3.2 Stray Capacitance

In this study, a converter is analysed that utilises PV panels and batteries in a single-phase bidirectional grid-tie system. In this topology, the DC side stray capacitance is dominated by the PV panels. Although batteries and heatsinks may also have stray capacitance to ground, the magnitude of this capacitance is negligible when compared with PV panels [10]. PV panels have significant surface area, dielectric material between the surfaces, and also generally have a metallic frame forming a stray capacitance. In the UK, PV panels, like all other appliances need to be grounded for safety reasons. As the metallic frame of PV panels needs to be grounded, a stray capacitance (parasitic capacitance) is formed between the actual PV panel and the grounded frame. The magnitude of this capacitance relies on the following; surface area of the PV panel and its materials, PV panel frame size and its materials, the weather conditions and the dust that lies on the PV panel itself [11-13]. In [14], it is shown that measured stray capacitance was ~150pF when the panel is dry, whereas this value increased up to ~9nF when the panel's surface was wet. Furthermore, in [15] examples of calculated values are given, some of them were as high as 150nF/kW, concluding that an accurate way of calculating stray capacitance is difficult to achieve. The value of the leakage current in transformerless systems is directly related with the magnitude of this stray capacitance. It should be noted that the stray capacitance is present at both nodes of the PV panels as can be seen in Figure 3.2(a), which further complicates the effect. In literature, authors generally accept these two capacitances are identical and their sum may be approximated according to SMA Solar Technology by using $C \approx 50\ A/d$. Where C is capacitance in nF, A is electrically effective area of the PV panel in m² and d is distance between capacitor plates in mm. For the sake of simplicity, 100nF/kW capacitance per PV array is selected to be used in the simulation studies presented in this chapter.

3.3 Common-mode Voltage in Single-phase Systems

As mentioned previously, galvanic isolation helps to reduce the inherent issues in a grid-tie PV system, such as leakage currents to ground. If methods of removing the transformer are to be investigated, it is important to understand the circuitry in order to see how the leakage path is created without the transformer. Figure 3.2(a) shows a generic single-phase grid-tie PV converter with stray capacitances at each node of the PV. The stray capacitances on each terminal of the PV panel are C_{PV1} and C_{PV2}, it should be noted that $C_{PV} \cong C_{PV1} \parallel C_{PV2}$. The grid leakage current (I_{lg}), the DC link capacitor (C) and the filter inductors (L_1 and L_2) are also illustrated. Furthermore, the points '*P*' and '*N*' represent the positive and negative nodes of the DC link respectively; whereas the '*A*' and '*B*' terminals are connected to the filter inductors and then to the single-phase grid. Voltages V_{AN} and V_{BN} are the potential difference between output terminals A to the negative node of the DC link and vice versa. These voltages are imposed by the modulation scheme, therefore a model including them is shown in Figure 3.2(b).

The mathematical expressions of the common-mode voltage (V_{CM}) and the differential-mode voltage (V_{DM}) are defined as follows [7, 11, 16, 17]:

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} \tag{3.1}$$

$$V_{DM} = V_{AN} - V_{BN} \tag{3.2}$$

Rearranging equations (3.1) and (3.2), the inverter's output voltages can be expressed in terms of common-mode and differential mode voltages.

$$V_{AN} = V_{CM} + \frac{V_{DM}}{2} \tag{3.3}$$

$$V_{BN} = V_{CM} - \frac{V_{DM}}{2} \tag{3.4}$$

By using the equations, another model consisting common-mode and differential-mode voltages can be seen in Figure 3.2(c).

In [6], equations (3.3) and (3.4) are used to further simplify the circuit by considering the filter arrangement. As a result, the equivalent common-mode voltage $(V_{CM_{eq.}})$ can be defined.

$$V_{CM_{eq.}} = V_{CM} + \frac{V_{DM}}{2}\frac{L_2 - L_1}{L_1 + L_2} \tag{3.5}$$

A simple common-mode model can then be drawn using equation (3.5), in Figure 3.2(d).

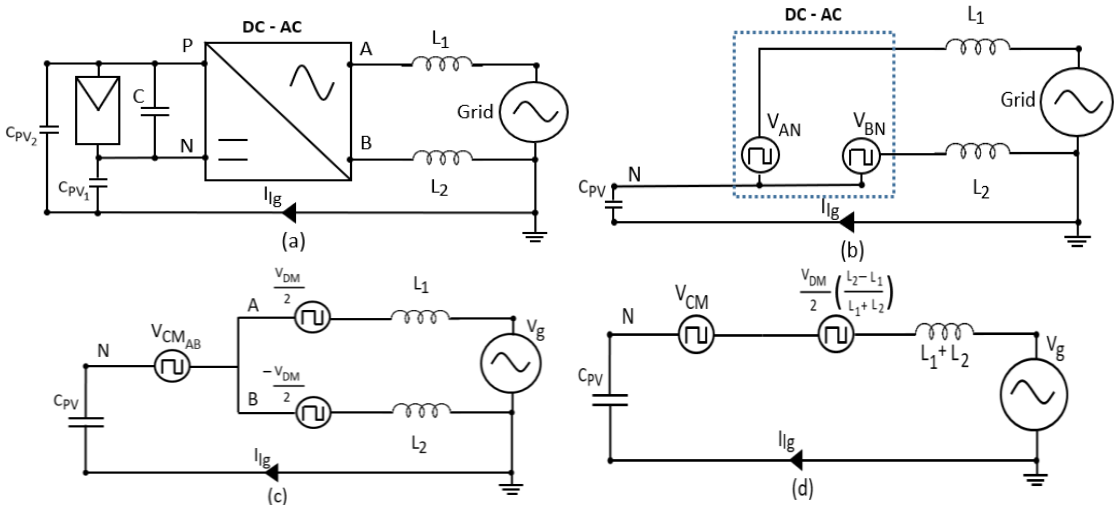

Figure 3.2: (a) Single-phase grid-tie PV converter, (b) model using voltage sources, (c) model showing common-mode and differential-mode voltages, (d) equivalent simple model

From equation (3.5), it is possible to say that leakage current in a single-phase grid-tie PV system does not only depend on the stray capacitance, but also the combination of common-mode and differential-mode voltages. Moreover, the output filter arrangement also has an effect on the leakage current. Dependent on the filter configuration, two different scenarios can be analysed:

In an asymmetrical design, where $(L_1 \neq 0,\ L_2 = 0\ or\ L_1 = 0,\ L_2 \neq 0)$, the $V_{CM_{eq.}}$ becomes:

$$V_{CM_{eq.}} = V_{CM} + \frac{V_{DM}}{2} = V_{AN} \qquad \text{when} \qquad (L_1 = 0\ ,\ L_2 \neq 0) \tag{3.6}$$

$$V_{CM_{eq.}} = V_{CM} - \frac{V_{DM}}{2} = V_{BN} \qquad \text{when} \qquad (L_2 = 0\ ,\ L_1 \neq 0) \tag{3.7}$$

In a symmetrical design of the filter inductors, where $(L_1 = L_2 \neq 0)$, the $V_{CM_{eq.}}$ becomes:

$$V_{CM_{eq.}} = V_{CM} = \frac{V_{AN} + V_{BN}}{2} \tag{3.8}$$

From equations (3.6) and (3.7), the equivalent common-mode voltage in a standard 2-level voltage source converter (VSC) with asymmetrical filter configuration is dependent on common-mode and also differential-mode voltages. In contrast, in a 2-level VSC with symmetrical filter configuration, equivalent common-mode voltages are affected by common-mode voltages only, which can be seen in equation (3.8).

In [18], frequency domain analysis is applied to the common-mode circuit of a full-bridge topology. It concludes that the generated leakage current is not always proportional to the stray capacitance value. The leakage current may increase at the resonant frequency of the formed resonant circuit that includes stray capacitances and output filter combination [18].

3.4 Common-mode Voltage in Three-phase Systems

In a three-phase system, galvanic isolation again mitigates the leakage currents. To mathematically analyse this, we can assume a three-phase PV system of 35A base current and 415 V line voltage, which is UK voltage standards. The base impedance for this system can be calculated as:

$$Z_b = \frac{V}{I} = \frac{415}{35} = 11.86\ \Omega \tag{3.9}$$

Using the calculated system base impedance, a base capacitance value can be calculated for a frequency limit of 50 kHz. This limit is set as leakage current frequencies above this value are mostly filtered by the EMI filter.

$$C_{b-50\ kHz} = \frac{1}{\omega_b Z_b} = \frac{1}{2\pi f_{fund}.Z_b} = 268\ nF \tag{3.10}$$

It is possible to neglect capacitances that are < 1% of the base capacitance, as these capacitances reactance >> base capacitive reactance and their influence is minimal below 50 kHz. The stray capacitance of a system with galvanic isolation is around 100 pF [19], which is mainly formed by the transformer stray capacitance. Therefore, galvanic isolation mitigates the effect of low frequency leakage current.

In a transformerless three-phase system with no neutral connection, the calculated maximum value of this stray capacitance is around 150nF/kW [15]. In order to analyse the system, common-mode and differential-mode voltages for phase A to B, B to C, and C to A need to be derived. As these processes are similar, only the derivation of common-mode and differential-mode derivation between phases A and B will be shown. A generic diagram for a conventional three-phase VSC is shown in Figure 3.3(a). The imposed voltages can be seen in Figure 3.3(b).

$$V_{CM_{AB}} = \frac{V_{AN} + V_{BN}}{2} \tag{3.11}$$

$$V_{DM_{AB}} = V_{AN} - V_{BN} = V_{AB} \tag{3.12}$$

Rearranging equations (3.11) and (3.12), the output voltages between converter output points ‘A’ and ‘B’, and the reference point ‘N’ can be expressed as:

$$V_{AN} = \frac{V_{DM_{AB}}}{2} + V_{CM_{AB}} \tag{3.13}$$

$$V_{BN} = -\frac{V_{DM_{AB}}}{2} + V_{CM_{AB}} \tag{3.14}$$

Models consisting of common-mode and differential-mode voltages, and the simplified equivalent circuit are shown in Figure 3.3(c) and Figure 3.3(d) respectively. Considering the heatsink to ground capacitance is equal for all phases, it is possible to derive equation (3.15).

$$V_{CM_{ABeq.}} = V_{CM_{AB}} + \frac{V_{DM_{AB}}}{2}\frac{L_B - L_A}{L_A + L_B} \tag{3.15}$$

If we repeat the same approach on other phases, the total common-mode voltage becomes:

$$V_{CM_{Total}} = V_{CM_{ABeq.}} + V_{CM_{BCeq.}} + V_{CM_{CAeq.}}$$

$$V_{CM_{Total}} = \frac{V_{AN} + V_{BN} + V_{CN}}{3} + \frac{V_{DM_{AB}}}{2}\frac{L_B - L_A}{L_A + L_B} + \frac{V_{DM_{BC}}}{2}\frac{L_C - L_B}{L_B + L_C} + \frac{V_{DM_{CA}}}{2}\frac{L_A - L_C}{L_C + L_A} \tag{3.16}$$

Using symmetrical output filter arrangement, equation (3.16) can be simplified into:

$$V_{CM_{Total}} = \frac{V_{AN} + V_{BN} + V_{CN}}{3} \tag{3.17}$$

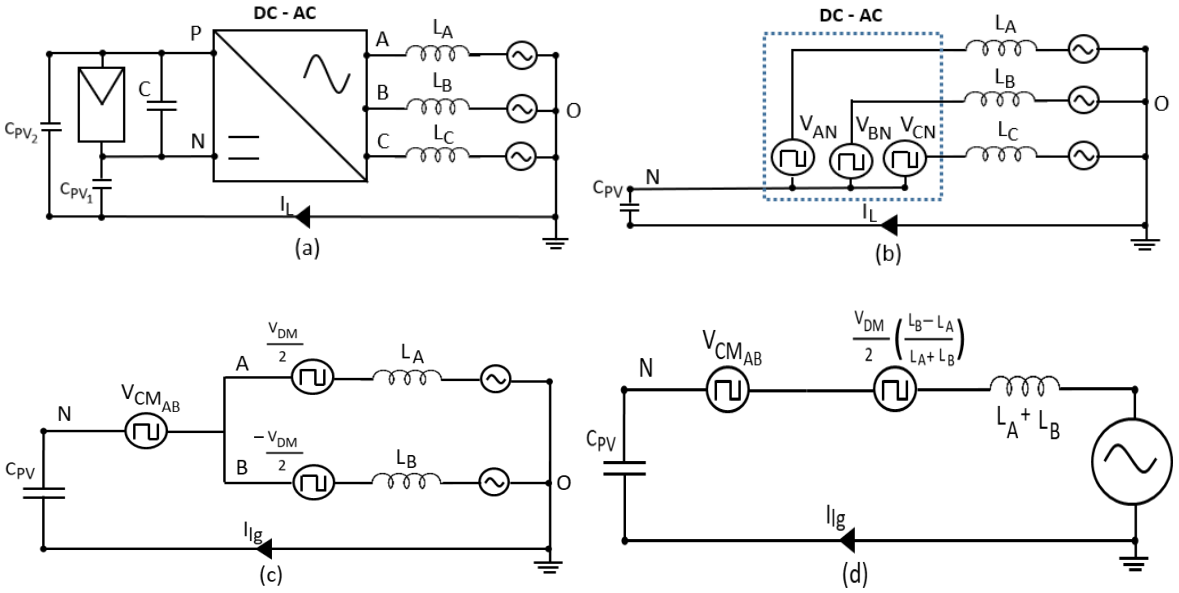

Figure 3.3: (a) Three-phase grid-tie PV converter, (b) model using voltage sources, (c) model showing common-mode and differential-mode voltages for 2 phases, (d) equivalent simple model for 2-phases

In [20], a three-phase PV system is tested and shows that connecting supply neutral to the mid-point of the DC link capacitors results in low leakage current. Moreover, high inductance in neutral line greatly increased the leakage current [19]. Another study tried using a four-phase hard switching converter to drive a three-phase machine in order to reduce common-mode voltages, and revealed that fourth leg may be used to inject zero-sequence current to reduce the leakage current [21].

3.5 Methods to Suppress Leakage Current

There are several methods available when it comes to suppressing the leakage current caused by common-mode circuit in a non-isolated converter. In literature, these methods can be categorised into three groups: 1) topology methods; where the topology of the converter is modified for eliminating the leakage current, 2) filtering methods; where common-mode filters or chokes are added to the leakage paths to provide attenuation, 3) modulation methods; where appropriate modulation is applied to switching devices to minimise common-mode voltages. Next sections will explain and analyse the effectiveness of these different methods for conventional and multilevel VSCs.

3.5.1 Converter Topologies

Modifying the converter topology is one of the approaches taken for supressing leakage current. Here, these methods are categorised into three subsections depending on the operation type of the converter. These are: 1) zero state decoupled topologies (ZSD), 2) zero state mid-point clamped topologies (ZSMC) and 3) solidly clamped topologies (SC). ZSD topologies operate by decoupling the DC and AC side of the converter during the zero voltage state, or in other words the freewheeling period. ZSMC topologies work by clamping the AC side of the converter to the mid-point of the DC link capacitors during the freewheeling period. Lastly, SC topologies have a solid connection between the AC side and the DC side of the converter. The next sections will provide circuit diagrams and analysis for the most common two topologies within these categories.

3.5.1.1 Zero State Decoupled Topologies

ZSD topologies enable decoupling of the PV panels from the AC side of the converter during the freewheeling period in order to block the ground leakage path. ZSD topologies generally include extra switching devices that block leakage paths during the zero voltage state. This addition usually reduces the conversion efficiency due to introduced extra switching losses, and also potentially increase the complexity of the modulation methodology. There are many examples of this approach that can be found in literature [22-26].

I. H5 Topology

H5 technology is one of the most popular topologies, which is patented by SMA Solar Technology [22]. This topology uses a hybrid modulation approach, and consists an additional switch 'S_5' for the decoupling of the stray capacitance during the freewheeling

period. Switches S_1 and S_3 are operated with the grid frequency, conducting continuously in positive and negative cycle of the reference wave respectively, whereas the remaining switches are commutated at the switching frequency. The positive voltage cycle is achieved by commutating switches S_1, S_4 and S_5 whereas in the negative voltage cycle, S_2, S_3 and S_5 are commutated. S_3, S_4 and S_5 are turned 'OFF' for the zero voltage output, therefore the freewheeling current travels through S_1 and the body diode of S_2, decoupling the stay capacitance from the AC side of the converter. The H5 topology is illustrated in Figure 3.4.

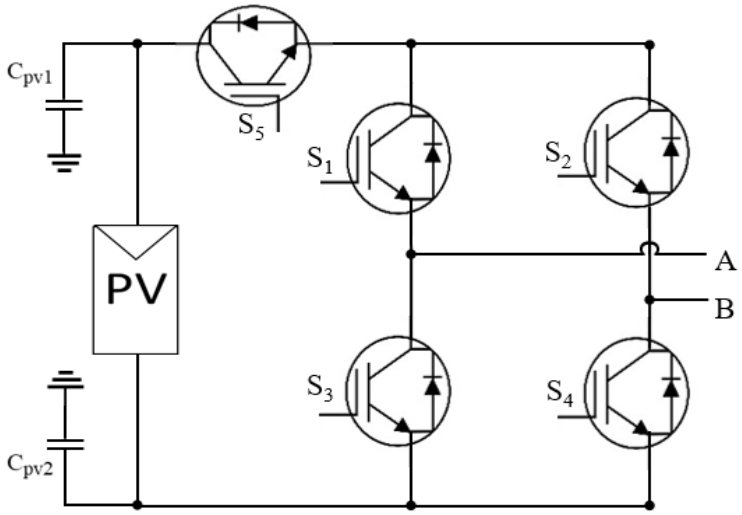

Figure 3.4: H5 topology from SMA Solar Technology

II. Highly Efficient and Reliable Inverter Concept (HERIC) Topology

Highly Efficient and Reliable Inverter Concept (HERIC) is introduced in [23] and patented by Sunways. This topology consists of two extra switches (S_5 and S_6) that are used for AC decoupling of the converter. The HERIC topology operates similarly to the unipolar modulated 3-level H-bridge topology but its common mode characteristics are similar to bipolar modulation [27], where leakage current to ground is mitigated. During the freewheeling period, either S_5 or S_6 is 'ON' dependent on the polarity of reference wave, whereas S_1, S_2, S_3 and S_4 are all 'OFF'. This topology has a higher efficiency when compared to H5, as the load current is short-circuited through either S_5 or S_6 during a zero voltage state of the H-bridge. The circuit diagram of HERIC topology is shown in Figure 3.5.

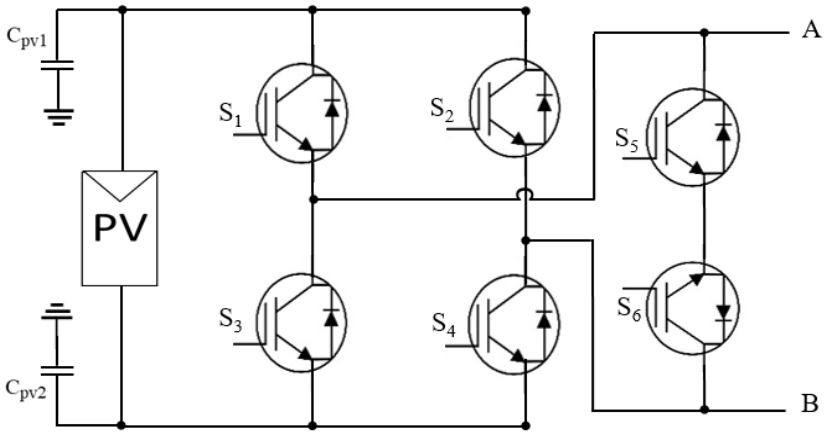

Figure 3.5: Highly efficient and reliable inverter concept (HERIC) topology

3.5.1.2 Zero State Mid-point Clamped Topologies

ZSMC topologies aim to clamp the common-mode voltage to half the input voltage during the freewheeling period of the H-bridge. Supressing high frequency common-mode voltages may help to reduce the leakage currents. These topologies generally have a split DC link, where its mid-point is used for clamping during the zero state with the help of an additional switch. Some of the examples for these topologies are presented in literature [1, 28-31].

I. oH5 Topology

The oH5 topology is a slightly modified version of H5 topology, which has additional switches and capacitors compared to a conventional H-bridge topology [28]. In Figure 3.6, either S_1 or S_2 is 'ON' during the freewheeling mode in the positive or negative half period of the grid current. In order to generate positive and negative DC link voltage switches S_1, S_4 and S_6 and S_2, S_3 and S_6 are 'ON' respectively.

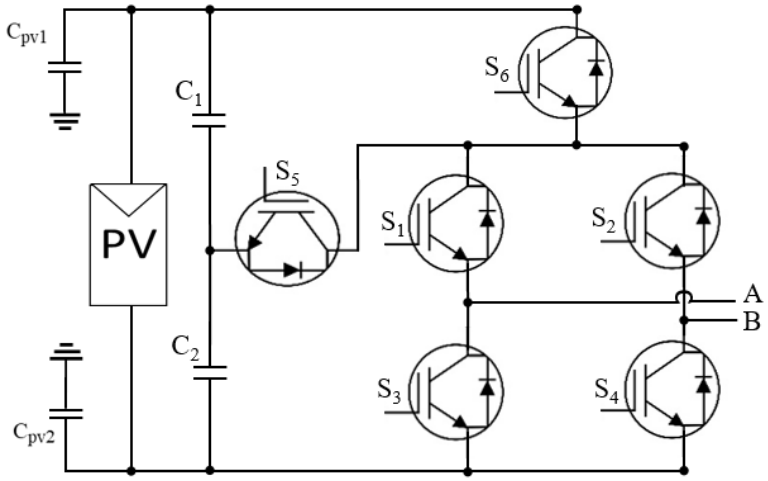

Figure 3.6: oH5 topology

II. H6 or Full-bridge with DC Bypass Topology

Figure 3.7 shows a H6 or full-bridge with DC bypass topology, which uses DC decoupling with additional switches (S_5 or S_6), diodes (D_1 or D_2) and capacitors (C_1 or C_2). This topology is used by Ingeteam [1, 29]. Similarly to oH5 topology, the common-mode voltage is clamped to the mid-point of the DC link with the help of clamping diodes. The turn-on speed of these clamping diodes are crucial as only one of these diodes conducts during the freewheeling period depending on the freewheeling path potential being higher or lower than the half of the DC link voltage. Switches S_1 - S_4 operates at grid frequency and all of them contribute to conduction losses during the positive and negative reference wave, increasing the conduction losses compared to other topologies.

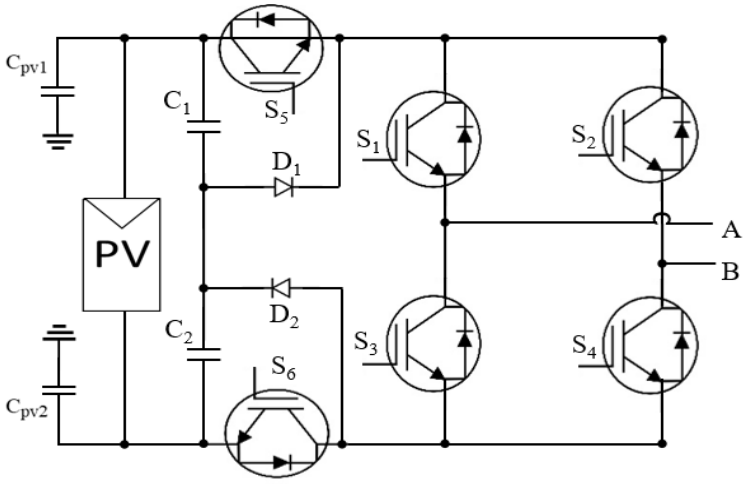

Figure 3.7: H6 or DC bypass topology from Ingeteam

3.5.1.3 Solidly Clamped Topologies

SC topologies have a solid connection between the AC side of the converter and the PV panel therefore the zero voltage state has a clamped voltage, resulting in non-varying common-mode voltages. SC topologies generally have more devices compared to a standard full-bridge topology, where clamping is achieved with the help of capacitors or diodes. Many examples of these topologies are present in literature [32-36]

I. Neutral Point Clamped Topology

The general multilevel neutral point clamped topology (NPC) was analysed in Chapter 2. The NPC topology and stray capacitances are illustrated in Figure 3.8. This topology achieves clamping of common-mode voltage during the freewheeling period with the help of diodes D_1 and D_2 [32]. During the positive voltage cycle, S_1 and S_2 are 'ON', and S_2 and

D_1 provide the freewheeling path. In contrast, S_1' and S_2' operate during the negative voltage cycle. The current passes through S_1' and D_2 at the negative freewheeling period. The voltage between the PV panel nodes and ground is constant as the mid-point of the DC link is grounded.

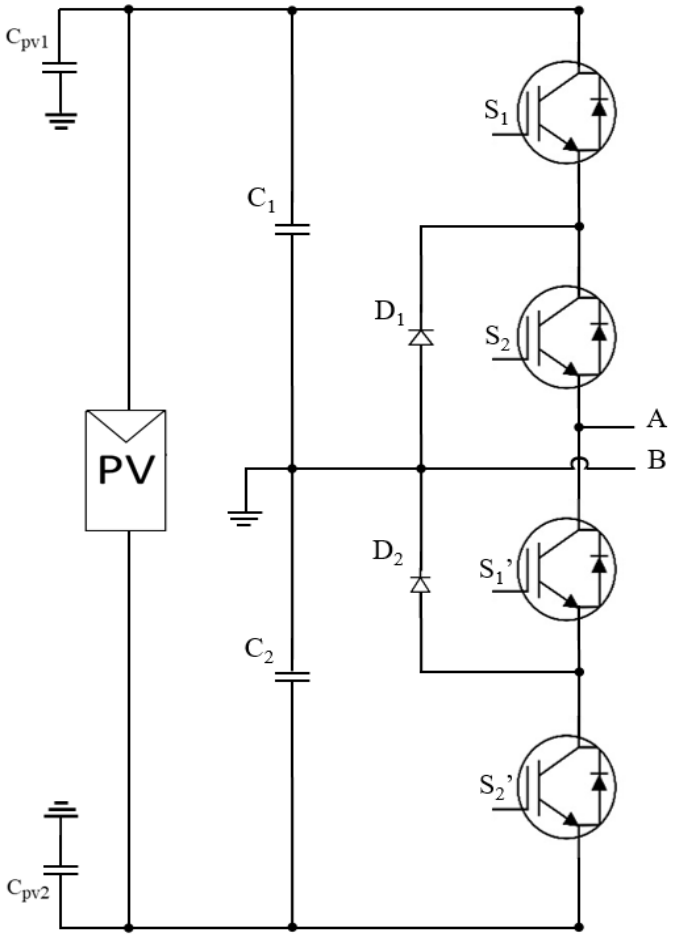

Figure 3.8: Neutral point clamped topology

II. Flying Capacitor Topology

The flying capacitor converter (FCC) is another topology described in Chapter 2. The FCC topology can theoretically provide an excellent solution to clamping common-mode voltage to the mid-point of the DC link as diodes are replaced with floating capacitors (Figure 3.9) [33]. In real-life applications, there are imbalances in floating capacitor voltages due to switching actions, which degrade the performance of the converter and potentially cause leakage current. The voltage ratio of C_1/C_3 and C_2/C_3 must be equal to 1, therefore average current flowing through the floating capacitor, C_3, is zero. Pre-charging capacitors is compulsory for this topology, and considering stray capacitances to ground, it is difficult to balance capacitor voltages [37].

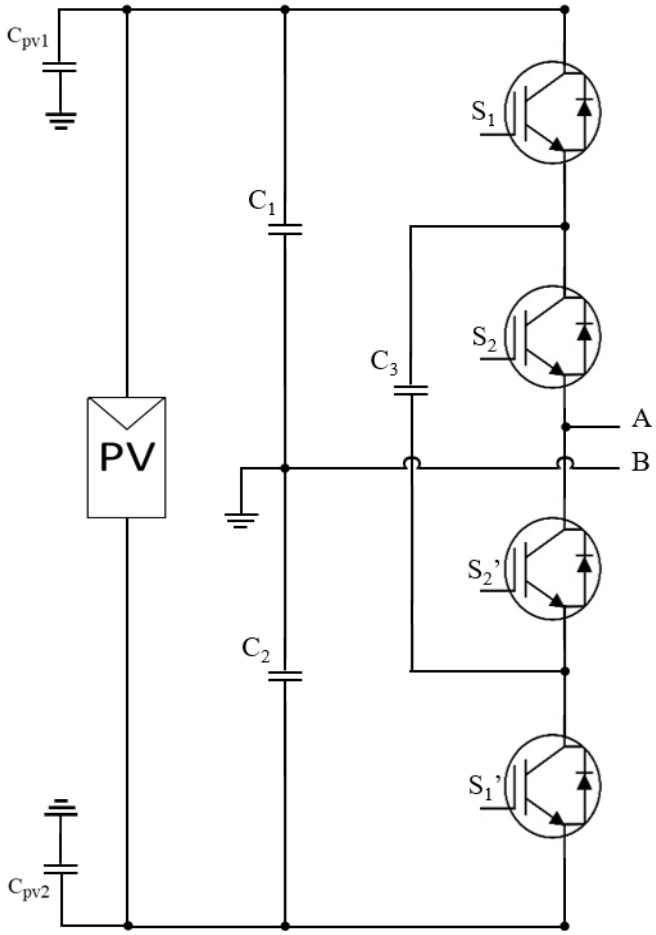

Figure 3.9: Flying capacitor topology

3.5.1.4 Cascaded H-bridge Topology

In a conventional H-bridge topology, aforementioned methods show that it is possible to eliminate or suppress the leakage current by changing the converter topology with additional devices. ZSD methods showed that decoupling the DC and/or AC side of the converter may reduce the leakage current. The ZSD topologies are generally cheaper and more reliable than the ZSMC and SC as ZSD topologies require least number of devices.

Figure 3.10 shows a generic *m*-level *n*-module CHB converter that utilises batteries and PV panels in its DC link via a buck-boost DC-DC converter to allow bi-directional energy transfer. The H-bridge modules are cascaded in series. Capacitances C_{j1} and C_{j2} (module index; j=1,2,…,n) are also included in Figure 3.10, illustrating the stray capacitance between the ground and PV terminals. The negative terminal of each H-bridge and PV "N_j" is accepted as reference point for j^{th} module, midpoints of each H-bridge leg are named "A_j" and "$\underline{B_j}$" forming the output terminals. Moreover, grid voltage, filter inductances, the ground point and grid leakage current are named as "V_g", "L_1" and "L_2", "O" and "i_{lg}" respectively.

Similarly to a 3-level H-bridge topology, CHB converters also have poor common-mode voltage characteristics with conventional modulation methods. In [38], it is stated that the amplitude of leakage current decreases with increasing CHB output voltage levels when input and output parameters are identical. Therefore, it is possible to say, with increasing CHB modules, the leakage current may decrease when operated with conventional modulation methods.

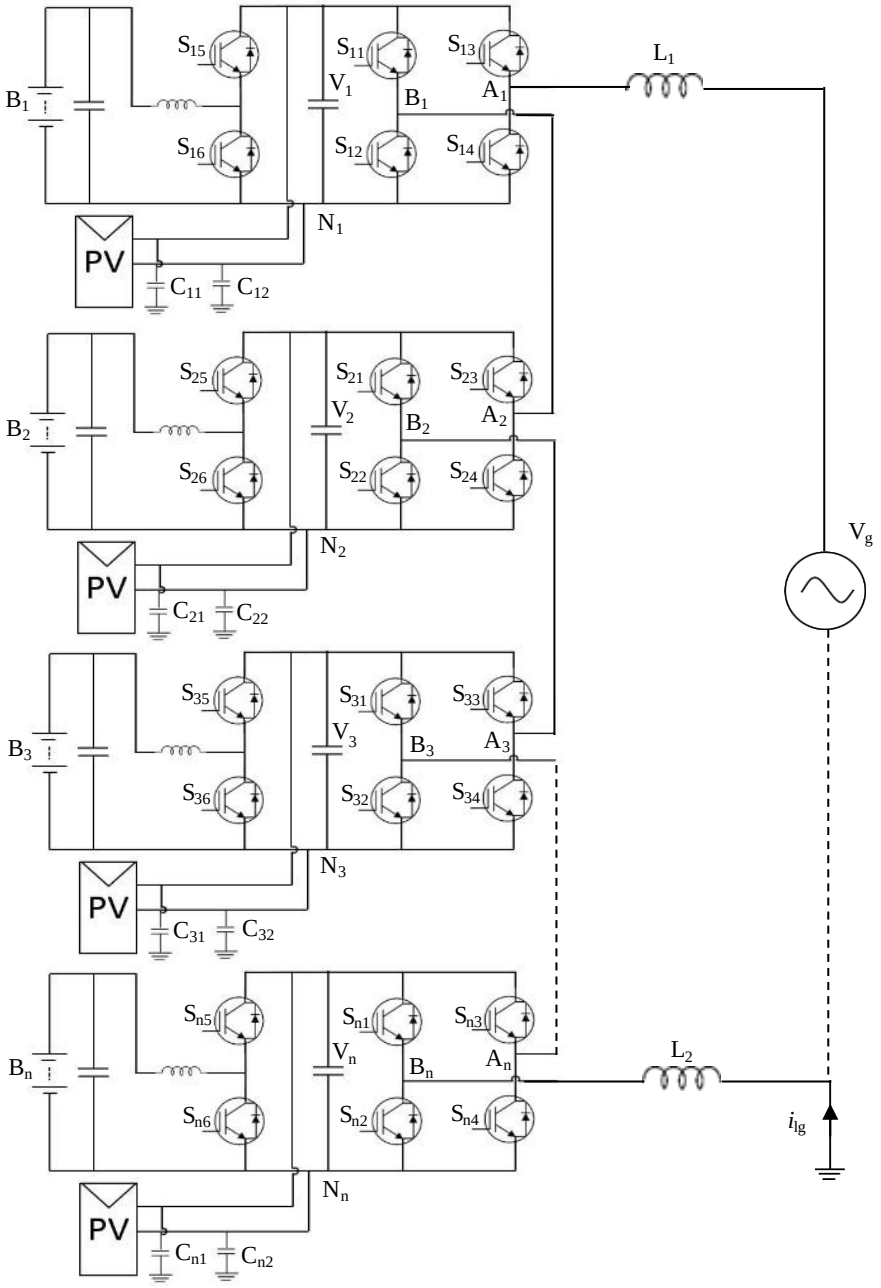

Figure 3.10: Single-phase m-level n-module cascaded H-bridge converter

In a series connected CHB converter, changing topology of modules may not suppress leakage current as there are inter-module leakage paths that are available between the PV

panels and the ground. It is possible to minimise the leakage current during the freewheeling period by adopting H5 modules, and modulating the CHB with phase disposition pulse width modulation (PDPWM). However, the total common-mode voltage consists of high frequency oscillations for most of the complete switching cycle, causing leakage currents to the ground. A five-level CHB consisting of H5 modules and a special filtering arrangement is proposed in [39]. Although this unique configuration helps to suppress leakage current, it compromises the output voltage quality and increases the complexity and cost of the converter.

3.5.2 Filtering Methods

Filtering is important when it comes to converters that generate common-mode voltages. As mentioned in section 3.3, the output filter of a converter has a significant impact on the leakage current in transformerless converters. Literature suggests that a filter solution, such as adding common-mode chokes, is also possible by creating a low impedance bypass loop for high frequency common-mode noise [39-42]. These studies mostly concentrate on symmetrical output filter condition as this eliminates the effect of differential-mode voltage on leakage current. In a cascaded condition, these studies recommend using symmetrical common-mode chokes at output terminals of each module. This helps to reduce leakage currents by providing attenuation but the output voltage waveform degrades. In [41], a simulation study is presented for a 5-level CHB converter, suggesting additional LC filters at the AC side of each module, having a 1:3 corner frequency to switching frequency ratio. In [42, 43], symmetrical common-mode chokes are placed at the terminals of the PV panels, aiming to provide an inductive path for the stray capacitance currents in the PV. This solution requires complex mathematical analysis when selecting filter values and the switching frequency needs to be predetermined. Filter solutions are generally costly and have a negative impact on converter volume and weight.

As the scope of this work is a single-phase CHB converter, it is important to generate a generalised equivalent circuit for an m-level n-module (where n=2,3,4,… and m=2n+1) CHB consisting of common-mode and differential-mode voltages for both asymmetrical and symmetrical output filter arrangements.

Capacitances C_{j1} and C_{j2} seen in Figure 3.10 are in parallel to the ground, therefore the equivalent parasitic capacitance of the j^{th} module is $C_{pvj} = C_{j1} \parallel C_{j2}$. If $C_{j1} = C_{j2}$, $C_{pvj} = 2C_{j1} = 2C_{j2}$. Using equations (3.3) and (3.4) and the circuit in Figure 3.10, the equivalent circuits representing common-mode and differential-mode voltages are illustrated in Figure 3.11. The node between common-mode and differential mode voltages "X_j" is an imaginary point that is used for ease of the circuit analysis, and does not exist in the real circuit. The output filter in Figure 3.11(a) represents an asymmetrical configuration where $L_1 \neq 0$, $L_2 = 0$ whereas in Figure 3.11(b) a symmetrical filter is shown where $L_1 = L_2 \neq 0$. These output filter configurations have distinct leakage current characteristics, thus should be examined separately.

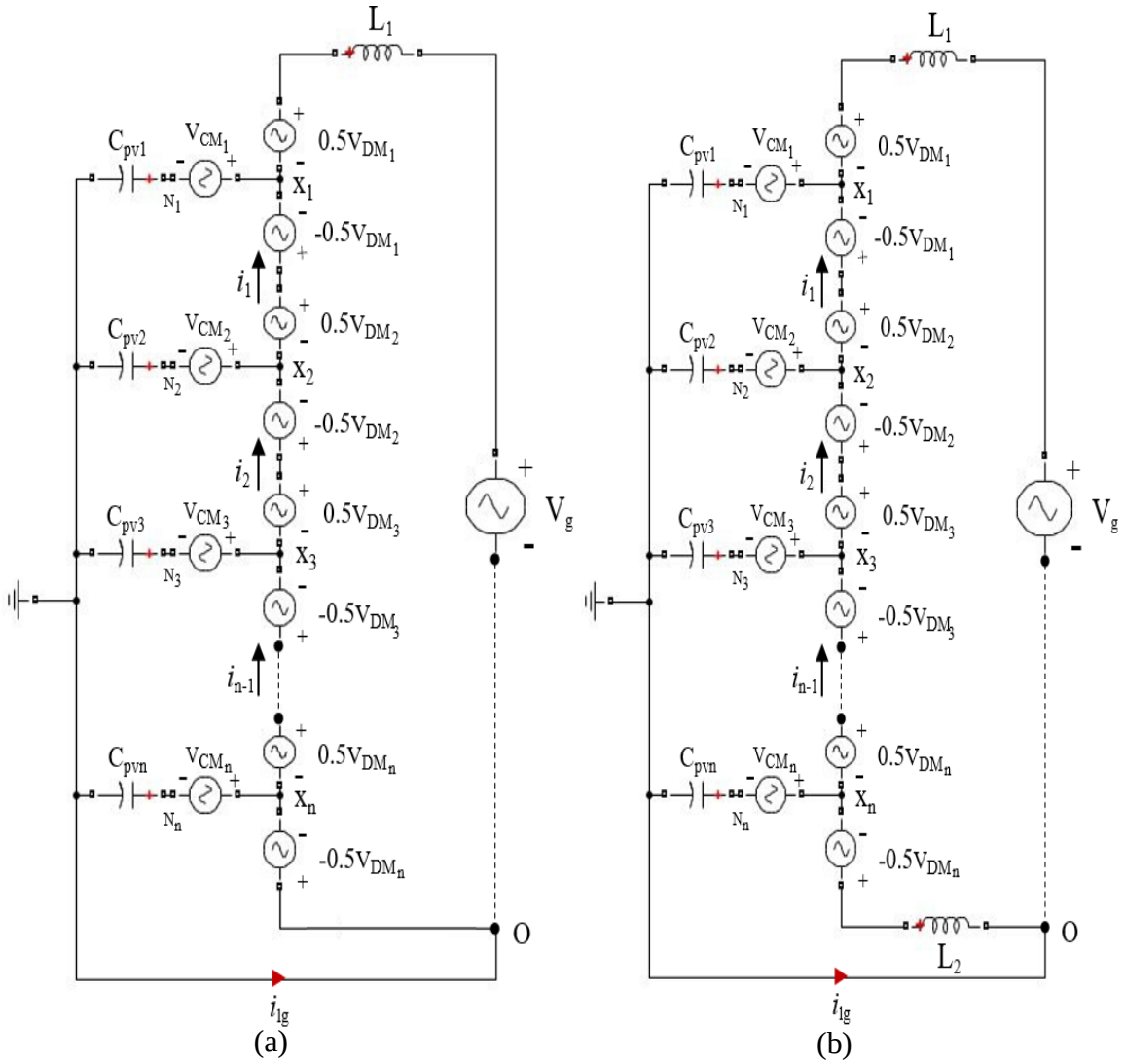

Figure 3.11: Equivalent circuit of an m-level n-module CHB (a) with asymmetrical filter, (b) with symmetrical filter

3.5.2.1 Asymmetrical Filtering

Assuming the above mentioned condition $L_1 \neq 0$, $L_2 = 0$, parasitic capacitance voltage (PCV) of j^{th} module can be obtained from Figure 3.11(a): (where j=1,2,…,n)

$$V_{N_jO} = 0.5V_{DM_j} - V_{CM_j} + \sum_{k=j+1}^{n} V_{DM_k} \tag{3.18}$$

If all terminal capacitances are equal, $C_{pv} = C_{pvj}$, then the grid leakage current i_{lg} (which is the sum of the module leakage currents) becomes:

$$i_{lg} = C_{pv}\frac{d}{dt}\sum_{j=1}^{n} V_{N_jO} = C_{pv}\frac{dV_{N_TO}}{dt} \tag{3.19}$$

where V_{N_TO} is the sum of parasitic capacitance voltages (SPCV), it can be derived as follows:

$$V_{N_TO} = -V_{CMT} + \sum_{j=1}^{n}(j - 0.5)\,V_{DM_j} \tag{3.20}$$

where $V_{CMT} = \sum_{j=1}^{n} V_{CM_j}$.

Grid leakage current in an asymmetrical circuit is given in (3.19). It can be seen that if V_{N_TO} varies over a period of time, leakage current will be present. Besides, the SPCV of an m-level converter is contributed by both differential-mode and common-mode voltages of the j^{th} module, as expressed in (3.20). Although the contribution of each module common-mode voltage is equal (unity coefficient), the differential-mode voltages have increasing coefficients, therefore distinguishing this outcome creates difficulties for modulation based leakage suppression methods.

3.5.2.2 Symmetrical Filtering

Adopting the aforesaid condition $L_1 = L_2 \neq 0$, Kirchhoff's law can be applied to nodes X_j in Figure 3.11(b) in order to obtain the following equation that applies to a n-module m-level CHB (where j=1,2,…,n and i=*1,2,…,n-1*).

$$\frac{V_{X_1O} - V_{CM_1}}{Z_{PV_1}} + \frac{V_{X_1O} + 0.5V_{DM_1} - V_g}{Z_{L_1}} - i_1 = 0 \tag{3.21}$$

$$\frac{V_{X_jO} - V_{CM_j}}{Z_{PV_j}} + i_{(j-1)} - i_j = 0 \ (\mathrm{j} \in \{2, \mathrm{n}-1\})$$

(3.22)

$$\frac{V_{X_nO} - V_{CM_n}}{Z_{PV_n}} + \frac{V_{X_nO} - 0.5V_{DM_n}}{Z_{L_2}} + i_{(n-1)} = 0$$

(3.23)

$$V_{X_iO} - V_{X_{(i+1)}O} = 0.5(V_{DM_i} + V_{DM_{(i+1)}})$$
$$V_{N_jO} = V_{X_jO} - V_{CM_j}$$
$$V_{N_TO} = \sum_{j=1}^{n} V_{N_jO}$$

(3.24)

The current between two adjacent modules are named as i_j, $i_{(j+1)}$,…,$i_{(n-1)}$. In a symmetrical filter configuration, it can be assumed that the impedance of filters are $Z_L = Z_{L_1} = Z_{L_2}$, where $Z_L = sL_1 = sL_2$. Additionally, we let the impedance of the parasitic capacitances be $Z_{pvj} = 1/sC_{pvj}$ to simplify the analysis. Substituting (3.21), (3.22), (3.23) and (3.24) the sum of parasitic capacitance voltage for an *n*-module CHB can be determined as:

$$V_{N_TO} = \frac{Z_{pv}\left(-2V_{CMT} + nV_g + \sum_{j=1}^{n}(2j - n - 1)\, V_{DM_j}\right)}{2Z_{pv} + nZ_L}$$

(3.25)

From [15] and section 3.2, the parasitic capacitance of a PV panel is calculated to be a maximum of ~150nF/kW. As a result, it can be said that $Z_{pv} \gg Z_L$ at low frequencies, i.e. grid-tie applications. The utility grid comprises low frequency harmonics only, therefore the magnitude of $Z_L \to 0$ and therefore may be neglected from analysis [44]. Considering this, equation (3.25) can be expresses as (see Appendix D):

$$V_{N_TO} \cong -V_{CMT} + \frac{n}{2}V_g + \sum_{j=1}^{n}\left(\frac{2j - n - 1}{2}\right)V_{DM_j}$$

(3.26)

Equation (3.26) reveals that when the number of cascaded H-bridges are odd (*n*=odd), the differential-mode voltage of the middle H-bridge does not contribute to SPCV, therefore it is impossible to keep SPCV constant in a complete switching cycle. Contrariwise, there may be a solution when the number of cascaded H-bridge modules are even (*n*=even). Using

equation (3.26), the SPCV of a four-module (n=4) CHB, the SPCV can be calculated using equation (3.27).

$$V_{N_T O} \cong -1.5V_{DM_1} - 0.5V_{DM_2} + 0.5V_{DM_3} + 1.5V_{DM_4} - V_{CMT} + 2V_g \tag{3.27}$$

Equation (3.27) approximates the SPCV for a nine-level four-module CHB, which is contributed by common-mode and differential-mode voltages. Notably the differential-mode voltages in modules 1 and 4 and modules 2 and 3 have opposite coefficients therefore a mechanism for reducing the leakage current with a combination of switching states may be possible over the complete switching cycle.

3.5.3 Modulation Techniques

The output voltages of each terminal V_{AN} and V_{BN} in a converter are created by switching actions. These voltages are directly related to the common-mode and differential-mode voltages of a converter that can be seen in equations from (3.1) to (3.4). In a conventional two-level VSC, the output voltages are limited to $+V_{DC}$ and $-V_{DC}$ therefore the ability to adjust the modulation strategy for constant SPCV is limited. Considering a single H-bridge module, three unique output voltages ($+V_{DC}$, 0 and $-V_{DC}$) can be generated with four possible switching states (see Table 2.1). Using equations from (3.1) to (3.4), common-mode and differential-mode voltages can be calculated for all four possible switching states, which can be seen in Table 3.1.

V_{AN}	V_{BN}	V_{CM}	V_{DM}	V_{out}
1	0	$V_{dc}/2$	V_{dc}	V_{dc}
1	1	V_{dc}	0	0
0	0	0	0	0
0	1	$V_{dc}/2$	$-V_{dc}$	$-V_{dc}$

Table 3.1: Common-mode and differential-mode voltages of H-bridge converter

In H-bridge converters, the effects of modulation strategy on the leakage current can be observed when bipolar modulation is applied. Bipolar modulation reduces the leakage current, however this modulation is not desirable as it only generates two output voltages and therefore requires strong output filtering [38]. Conversely, unipolar modulation (Table 3.1), cannot suppress leakage current although the number of output voltage levels are higher [45].

Modulation strategies for reducing leakage currents are presented for single-phase CHB converters [44-47]. In [45-47], sinusoidal pulse width modulation (SPWM) strategies are proposed for a five-level CHB, however leakage current spikes to ground are present while transitioning through the freewheeling period of the switching cycle. In [44], a modified phase disposition pulse width modulation method is proposed, which mitigates the leakage current in five-level CHB converters. In literature, modulation strategy methods are limited up to five-level CHB and there is no solution reported for a generalised *m*-level CHB. Modulation methods do not require extra devices such as transistors and/or inductors in order to suppress leakage currents and therefore provide the cheapest solution. Additionally, they do not increase the converter volume and weight. Here, a generalised circuit for an *m*-level *n*-module CHB is presented. Following that, a novel modulation strategy for a nine-level four-module CHB will presented, termed as leakage reduction pulse width modulation (LRPWM).

3.5.4 Leakage Reduction Pulse Width Modulation (LRPWM)

In order to provide a modulation strategy that reduces the leakage current, the switching function S_{jk} for a nine-level four-module CHB that imposes common-mode and differential-mode voltages needs to be determined using Figure 3.10:

$$S_{jk} = \begin{cases} 1, & S_{js} \quad ON \\ 0, & S_{js} \quad OFF \end{cases} \begin{pmatrix} \text{switch index,} \\ s = 1,2,3,4 \end{pmatrix} \tag{3.28}$$

If the DC link voltage is similar for all four of the modules, the imposed output voltages V_{AN_j} and V_{BN_j} for j^{th} module is given as:

$$V_{AN_j} = V_{dc} S_{j3} \tag{3.29}$$

$$V_{BN_j} = V_{dc} S_{j1} \tag{3.30}$$

A H-bridge has 4 valid switching states, therefore 256 valid unique switching states are present for a four module system (see Appendix A for 5, 7 and 9 level CHB switching states). Using equations (3.1), (3.2), (3.3), (3.4), (3.20), (3.27), (3.29) and (3.30) the sum of parasitic capacitance voltage (SPCV) '$V_{N_T O}$' can be calculated for each unique switching state for symmetrical and asymmetrical filter configuration.

Having a varying SPCV during a complete switching cycle causes leakage current in the system. Unfortunately, there is no combination of switching states that has non-varying SPCV throughout the whole switching cycle for an asymmetrical filter configuration, in an *m*-level CHB. From conditions in Table 3.2, +4V_{DC} and -4V_{DC} output stages can be achieved by only one unique switching state, and the SPCV of asymmetrical configuration for these levels are +6V_{DC} and -10V_{DC} respectively. This confirms that any modulation strategy will fail to suppress leakage current for a nine-level CHB with asymmetrical filter configuration.

Output Voltage	$S_{11}, S_{13}, S_{21}, S_{23}, S_{31}, S_{33}, S_{41}, S_{43}$	$V_{N_T O}$ **(Asym)**	$V_{N_T O}$ **(Sym)**
+4 V_{dc}	10101010	6V_{dc}	-2V_{dc}
+3 V_{dc}	10100010	4V_{dc}	-2V_{dc}
+2 V_{dc}	10110010	2V_{dc}	-2V_{dc}
+1 V_{dc}	11111000	0	-2V_{dc}
0	11110000	-2V_{dc}	-2V_{dc}
0	00001111	-2V_{dc}	-2V_{dc}
-1 V_{dc}	00011111	-4V_{dc}	-2V_{dc}
-2 V_{dc}	01001101	-6V_{dc}	-2V_{dc}
-3 V_{dc}	01000101	-8V_{dc}	-2V_{dc}
-4 V_{dc}	01010101	-10V_{dc}	-2V_{dc}

Table 3.2: Switching States of LRPWM

Conversely, it is possible to stabilise SPCV at -2V_{DC} while achieving a nine-level output voltage waveform in a symmetrical filter arrangement. If the converter is modulated by one of the combinations of switching states in Table 3.2, SPCV would be invariant and the leakage current would be minimised. From Appendix A, there is more than one unique switching states that generates -2V_{dc} SPCV for each of +3V_{DC}, +2V_{DC}, +1V_{DC}, 0V, -1V_{DC}, - 2V_{DC} and -3V_{DC} output voltage levels. When choosing leakage reduction pulse width modulation (LRPWM) switching states, the aim is to reduce the number of commutation events of switching devices in a complete switching cycle in order to reduce the switching losses and improve the efficiency of the modulation technique. The switching states of LRPWM is illustrated in Table 3.2.

Traditional PDPWM and PSPWM strategies may be implemented easily and do not require substantial computational power. Unfortunately, these modulation methods cannot produce a stable SPCV during complete switching cycle, therefore are unable to reduce leakage current. LRPWM requires only four carriers, unlike to PDPWM and PSPWM techniques, which requires eight carriers in order to generate gate signals for switches. The triangular carrier waveforms required by LRPWM, named as V_{c1}, V_{c2}, V_{c3}, and V_{c4}, must be in phase and have the same amplitude of 0.25, which are illustrated in Figure 3.12. These carriers are defined as $0 \le V_{c1} \le 0.25 \le V_{c2}$ $0.5 \le V_{c3}$ $0.75 \le V_{c4} \le 1$.

The utility reference waveform V_{ref} has to be modified, and compared with the distinct carriers to generate the switching functions S_{jk} for each transistor. The modified reference signals can be defined as:

$$\begin{cases} V_{r1} = V_{ref} \ during \ V_{ref} > 0\,, \quad V_{r1} = V_{ref} + 1 \ during \ V_{ref} < 0 \\ V_{r2} = V_{ref} \ during \ V_{ref} > 0\,, \quad V_{r2} = 1 \ during \ V_{ref} < 0 \\ V_{r3} = \left|V_{ref}\right| during -0.25 < V_{ref} < 0\,, \quad else \ V_{r3} = 0 \\ V_{r4} = 0 \ during \ V_{ref} > 0\,, \quad V_{r4} = \left|V_{ref}\right| \ during \ V_{ref} < 0 \\ V_{r5} = 1 \ during \ V_{ref} > 0\,, \quad V_{r5} = \left|V_{ref}\right| \ during \ V_{ref} < 0 \\ V_{r6} = V_{ref} \ during \ V_{ref} > 0\,, \quad V_{r6} = 0 \ during \ V_{ref} < 0 \\ V_{r7} = V_{ref} \ during \ 0 < V_{ref} < 0.25\,, \quad else \ V_{r7} = 0 \end{cases} \tag{3.31}$$

The switches in the same leg of the H-bridge have to turn 'ON' in complimentary manner (i.e. S_{j1} and S_{j2}). Gate pulses for each switch may be determined by comparing carrier waves with relevant reference waves in LRPWM strategy.

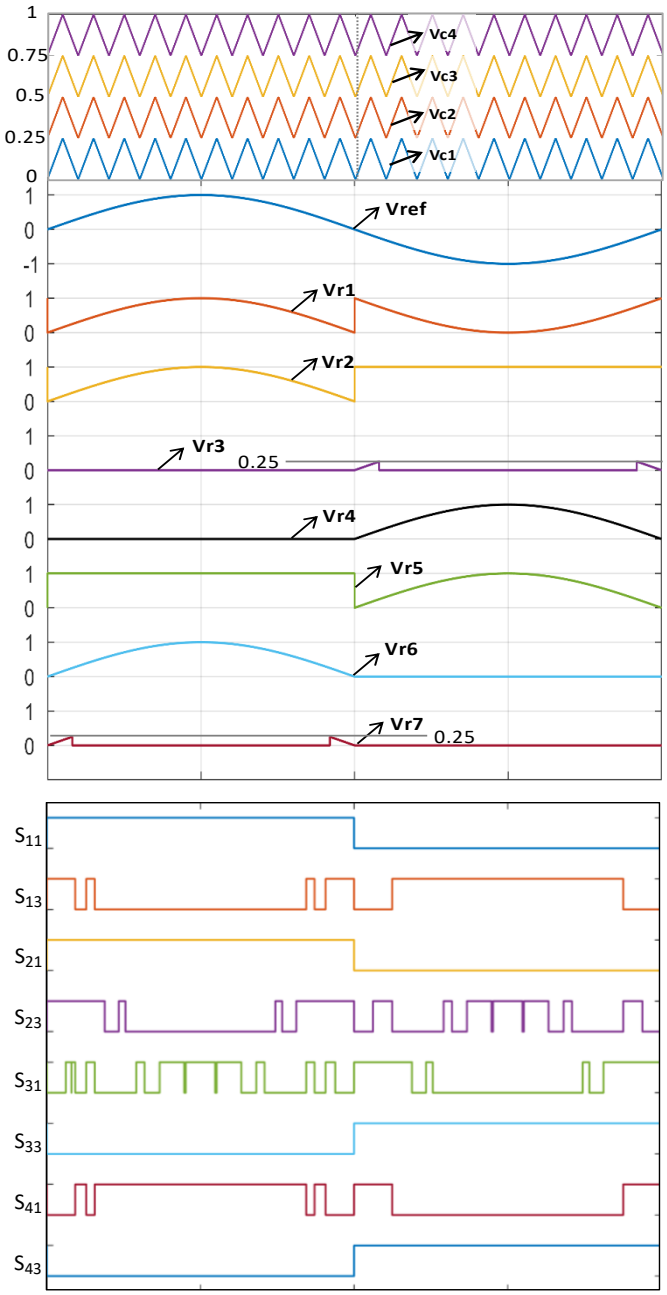

Figure 3.12: Switching pattern of LRPWM technique

If $V_{ref} > 0$, $S_{11}= S_{21}= S_{34}= S_{44}= 1$, $S_{12}= S_{22}= S_{33}= S_{43}= 0$; else $S_{11}= S_{21}= S_{34}= S_{44}= 0$, $S_{12}= S_{22}= S_{33}= S_{43}= 1$. If $V_{r1} < V_{c2}$ in the positive half cycle and $V_{r1} < V_{c3}$ in the negative half cycle $S_{13}= S_{42}= 1$, $S_{14}= S_{41}= 0$; otherwise $S_{13}= S_{42}= 0$, $S_{14}= S_{41}= 1$. In the positive half cycle if $V_{r2} < V_{c3}$, in the negative half cycle throughout $0 < V_{r4} < 0.25$ if $V_{r3} > V_{c1}$, and during $0.25 < |V_{ref}| < 0.75$ if $V_{r1} > V_{c3}$, and throughout $0.75 < V_{r4} < 1$ if $V_{r4} > V_{c4}$ $S_{23}= 1$, $S_{24}= 0$; otherwise $S_{23}= 0$, $S_{24}= 1$. In the positive half cycle during $0 < V_{r7} < 0.25$ if $V_{r7} > V_{c1}$, and during $0.25 < V_{ref} < 0.75$ if $V_{r1} < V_{c2}$ and during $0.75 < V_{ref} < 1$ if $V_{r6} > V_{c4}$, and during the negative half cycle if $V_{r5} < V_{c3}$ $S_{31}= 1$, $S_{32}= 0$; else $S_{31}= 0$, $S_{32}= 1$.

From Table 3.2, there are two different switching states for freewheeling period (0V output state). Throughout the zero crossing of reference wave, these states transition from one to the other subject to the polarity of the reference wave. There are ten unique switching states that achieve nine voltage levels for the correct operation of the CHB converter. Figure 3.12 represents the relevant gate pulses for each of the switching devices.

The proposed novel modulation strategy was implemented in MATLAB/Simulink to validate the success of LRPWM in suppressing the parasitic leakage current. In order to compare the results, conventional PSPWM and PDPWM techniques are also implemented. Simulation parameters include; DC link voltage of 115 V at each H-bridge module, grid voltage at 240 V_{RMS} and 50 Hz, 4 kHz switching frequency, a parasitic capacitance of 100 nF, a symmetrical grid filter of 3.51 mH and 9 µF in an LCL output filter arrangement.

Figure 3.13 shows individual module output voltages V_{m1}, V_{m2}, V_{m3} and V_{m4}, total output voltage V_{out} and lastly the grid current I_g of LRPWM strategy. Individual modules generate a three-level voltage waveform, achieving a nine-level output voltage waveform in total. After the grid filtering, the grid current waveform is high quality, and purely sinusoidal. The results show that the LRPWM approach can be applied to a nine-level CHB and produces a satisfactory output.

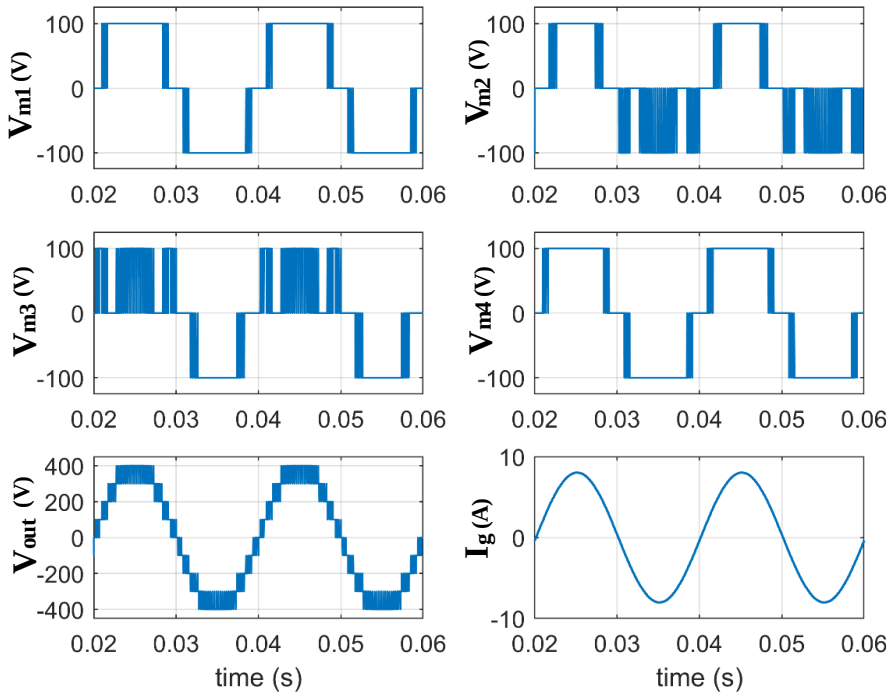

Figure 3.13: Simulation results of modules 1-4 output voltage waveforms, total output voltage and the grid current

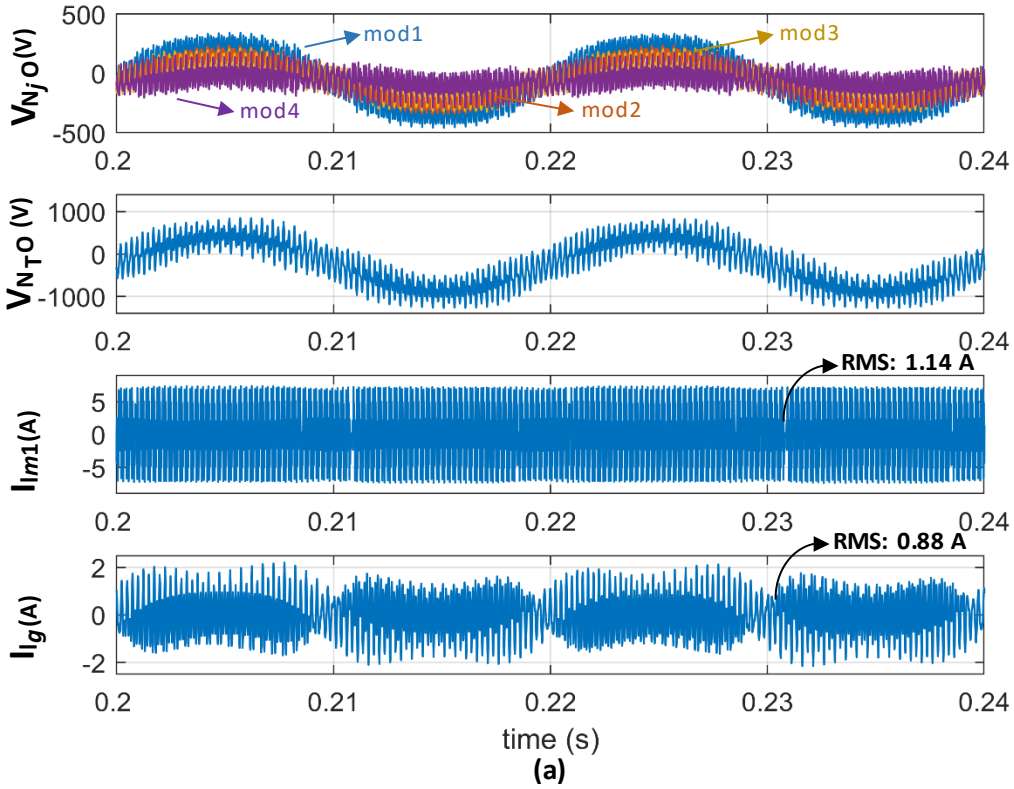

Figure 3.14: Simulation results of PCV of modules 1-4, SPCV leakage current of module 1and the grid leakage current of PSPWM strategy

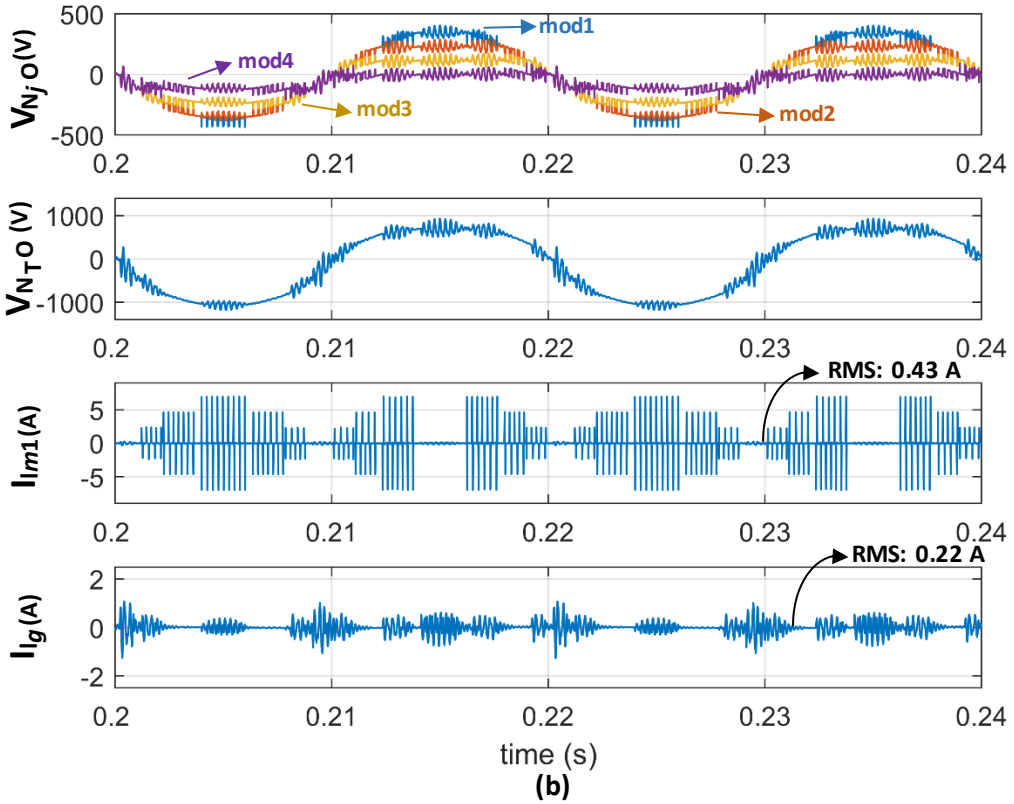

Figure 3.15: Simulation results of PCV of modules 1-4, SPCV leakage current of module 1and the grid leakage current of PDPWM strategy

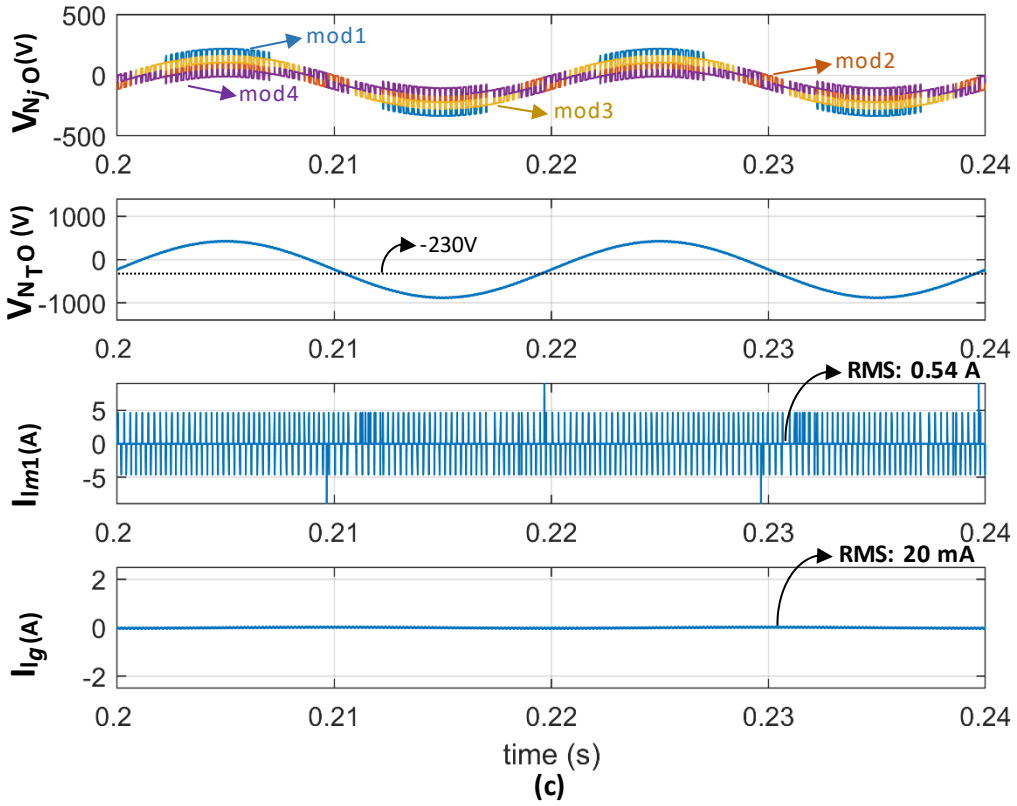

Figure 3.16: Simulation results of PCV of modules 1-4, SPCV leakage current of module 1and the grid leakage current of LRPWM strategy

PCV waveforms for individual modules of CHB, the SPCV, the leakage current of module 1 (I_{lm1}), and the parasitic grid leakage current is shown in Figures 3.14 to 3.16 for PSPWM, PDPWM and the proposed LRPWM respectively. The simulation results of conventional PSPWM and PDPWM strategies are given in Figures 3.14 and 3.15 respectively. The PCV at each module comprises pulsating voltages at switching frequency of the converter. These noisy voltage waveforms also effect the SPCV in both PSPWM and PDPWM, leading to leakage currents of 0.88 A_{rms} and 0.22 A_{rms} respectively.

LRPWM results are shown in Figure 3.16, and despite having a pulsating PCV waveform, the SPCV waveform has a RMS leakage current of 20mA. This is because the different PCV generated by different modules cancels with each other. The SPCV is sinusoidal and has a DC offset of -230 V, equal to $-2\,V_{DC}$. The simulation study is performed with highest possible grid distribution level voltage of 240V_{rms}, because higher grid voltages cause higher leakage current [44]. This can be confirmed by equation (3.27), where grid voltage component also contributes to the SPCV. Following this, the worst-case condition for leakage current is simulated.

3.6 Requirements for Leakage current

There are standards that regulate the leakage current in transformerless PV systems. VDE-0126-1-1 [48] is enforced in Germany (withdrawn as of 2020) which is an extension for IEC 62109-2 [49]. These standards obligate to monitor 3 different currents; 2 of which are ground fault currents and one system fault current. Lastly, this standard also obligates the measurement of the leakage currents, which is caused by potential variations through parasitic capacitive coupled elements, such as stray capacitance of PVs. It is recommended to monitor these currents with the help of a Residual Current Device (RCD). The standard VDE-0126-1-1 and IEC 62109-2 obligates to disconnect transformerless PV systems from the grid when peak value of the leakage current increases beyond 300 mA [48]. Moreover, disconnection times are recommended when the Root Mean Square (RMS) values of the leakage current instantaneously varies over a certain range. Table 3.3 details the values of these instantaneous changes and their corresponding disconnection times.

Instantaneous changes in leakage current (mA_{RMS})	Disconnection time (s)
30	0.3
60	0.15
150	0.04

Table 3.3: Instantaneous changes in leakage current and corresponding disconnection times according to VDE 0126-1-1.

The allowed instantaneous changes in leakage current is at maximum 30 mA, however PSPWM and PDPWM results in a root-mean-square (RMS) leakage current of 0.88 A_{rms} and 0.22 A_{rms} respectively, making them unacceptable for the case studied here with regards to the VDE-0126-1-1 standard. Conversely, LRPWM only produces 20 mA_{rms}, which conforms to the German standard.

3.7 Chapter Summary

Chapter 3 focused on common-mode voltages in transformerless grid-tie converters. Firstly, the effects of galvanic isolation and stray capacitances on grid-tie PV converters are discussed. Transformerless converters that utilise PVs, form a common-mode circuit that results in leakage currents when the voltage across these capacitances varies. Common-

mode voltage calculations for single-phase and three-phase applications are mathematically analysed and the effect of output filter arrangements on leakage current is discussed.

The study then focused on different ground leakage suppression methods, such as topologies, output filtering arrangements and modulation methods. The topology is chosen in Chapter 2 is a CHB converter. It is concluded that topology alterations of modules in a CHB cannot suppress leakage currents due to inter-module leakage paths. Furthermore, asymmetrical filter arrangement in a CHB converter also causes to leakage currents, which cannot be suppressed by any modulation method. Moreover, if the number of H-bridge modules are odd (n=odd), there is no solution as the SPCV cannot be kept constant at each output voltage level due to the middle H-bridge's differential-mode voltage not contributing to the SPCV. However, there may be a solution when the number of H-bridges are even (n=even).

Finally, a modulation method (LRPWM) is proposed for a four-module nine-level CHB that maintains the sum of parasitic capacitance voltages (SPCVs) constant during a complete switching cycle, which successfully suppresses the leakage currents and conforms to the German VDE-0126-1-1 standard.

The next chapter therefore focuses on a practical converter design, followed by the experimental evaluation of the proposed modulation methods in Chapter 5.

3.8 References

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Chapter 4
Converter Design and Simulations

4.1 Introduction

In previous chapters, multilevel converters (MLCs) were described, compared and problems related to common-mode voltages discussed. Cascaded H-bridge (CHB) converters require isolated DC supplies and therefore can be a suitable topology for a system utilising both PVs and battery energy storage. In particular, for a second life battery storage application, the CHB converter provides more flexibility and accessibility considering the age and origin of the battery, and enables implementation of modular maximum power point tracking in PV arrays.

This study aims to investigate a CHB based, grid-tie converter that can charge/discharge batteries following any given demand. The system is targeted to operate with a domestic rooftop PV systems, and utilise EV batteries in their second life, whilst being coupled to UK utility grid at 230 V_{AC} and 50 Hz. The battery is assumed to be sourced from some of the top selling EVs, for example the Nissan Leaf, Tesla Model S and Tesla Model 3 [1], however any other battery with matching or similar rating may be utilised.

Here, a 9-level CHB converter is designed to give a lower Total Harmonic Distortion (THD) waveform than a conventional 2-level Voltage Source Converter (VSC), or a MLC with lower output voltage levels [2]. The H-bridge is a full-bridge topology therefore it can utilise the DC source fully, unlike to a half-bridge topology that can only utilise half of the DC source voltage. Moreover, Chapter 2 detailed that CHB converter requires the least amount of total devices when compared with other MLCs that produce same output voltage levels.

Chapter 4 focuses on the specifications, analysis and design of the system, detailing a bidirectional DC-DC converter and a CHB converter to provide a two-stage conversion system. MATLAB/Simulink software is used to provide simulation results to verify the calculations and assumptions. Furthermore, the LabVIEW Co-simulation plugin with Multisim software is used to verify the FPGA based control algorithm's effectiveness in a virtual platform without the need of the actual converter circuit.

4.2 System Specifications and Control Platform

The system is designed to operate bi-directionally and be tied to the UK utility grid. The aim of the system is to produce a transformerless converter, and therefore there is no galvanic isolation between the DC and the AC side of the circuit. The UK utility grid has the same voltage and frequency properties as the rest of European utility network, 230 V_{rms} (+10% & -6%) at 50Hz (± 1%), and in a grid connected scenario, the converter needs to operate synchronously. A block diagram showing the most important components of the system is given in Figure 4.1.

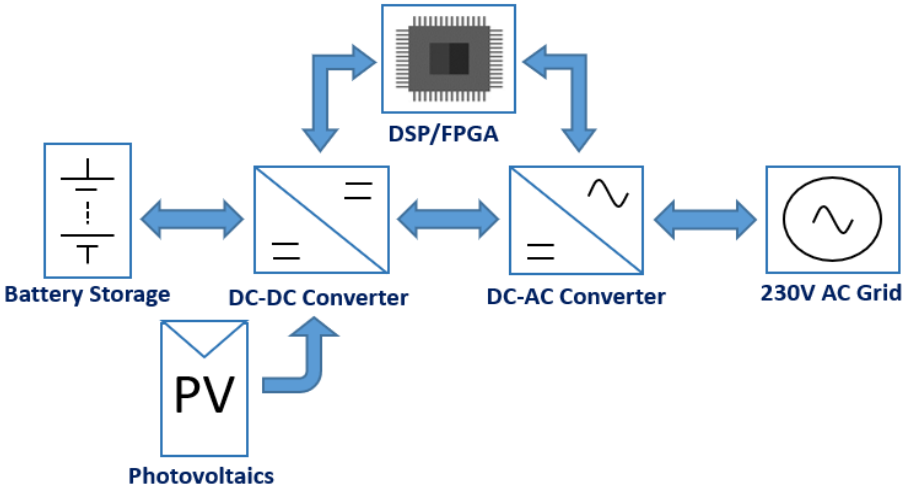

Figure 4.1: System block diagram

The most important specifications for the system are given below in Table 4.1.

Parameter	Symbol	Value
Output power	P_{out}	4 kVA
Output voltage	V_{grid}	230 $V_{AC\ rms}$
Input voltage / module	V_{in}	65.75 – 100 V_{DC}
DC link voltage / module	V_{dc_m}	100 $V_{DC\ nominal}$
PV panel MPP Voltage	V_{pv_mpp}	33.3 V_{DC}
PV panel maximum power	P_{pv}	325 W
Total DC link voltage	V_{dc}	400 V_{DC}
Maximum peak AC voltage	$V_{grid\text{-}p(max)}$	357.8 V_{AC}

Table 4.1: Specifications of the system

Figure 4.2 shows a circuit block diagram detailing the cascaded structure of the system, including 4 modules, each consisting a battery pack, PV array, a DC-DC converter and H-bridge converter. The system is able to transfer 4 kVA to the utility grid.

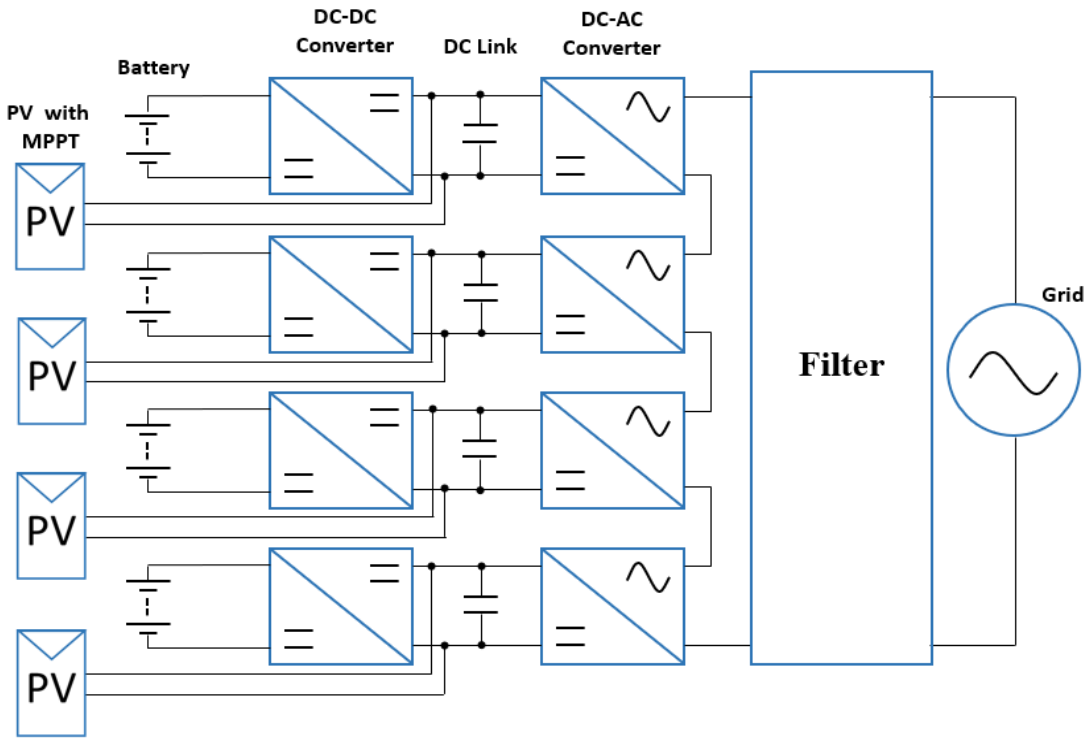

Figure 4.2: Circuit block diagram showing cascaded structure

The components that are present in Figure 4.1 such as battery, PV, DC-DC, AC-DC and the control platform are detailed individually in the next sections.

4.2.1 Battery

EV batteries tend to be replaced by automotive manufacturers when their State of Health diminishes to 70-80% percent of their original value [3]. Generally, this milestone is reached within 5-10 years of the car being placed on the market, depending on the use. Typically, the target battery for this system will have a capacity around 20-100 kWh depending on the EV model [4]. With the growth of EV market share, it is predicted that an increasing number of EV batteries will become available for a less demanding second life application, such as stationary energy storage application.

Although automotive manufacturers tend to not release their battery pack specifications, it is possible to find third party battery pack disassembly information. These sources reveal that Tesla uses Panasonic 18650 3.2 Ah cells whereas Nissan uses Automotive Energy Supply Corporation's 32.5 Ah pouch cells as of 2018 [5, 6]. From these sources, battery disassembly reveals that DC link voltage of these EVs are around 350 – 400 V, which is similar to the DC link voltage used in this study. It is important to know that any battery with similar specifications or any other comparable DC source may be used in this project.

4.2.2 Photovoltaics

Photovoltaic (PV) panel specifications may be selected according to the power rating required in a single module. In this study, each module should be able to provide around 1 kW. In a simulation study, 3x LG325N1C-A5 PV panels (each rated 325 W at MPP voltage) were connected in series to provide the specified voltage rating for each module [7]. The MPP voltage is panel dependant, but LG325N1C-A5 has 33.3 V_{pv_mpp} therefore, a DC link voltage of 100 V should allow the PVs to operate at their maximum power point (with suitable control). The total open circuit voltage of the PVs needs to be selected higher than the nominal DC link voltage. The DC link voltage may be pushed higher than the PV open circuit voltage to stop the power flow from PVs to the DC link. In this case, the power injected to the utility grid would be provided purely from the batteries.

4.2.3 Control Platform

The system is operated by a centralised master controller which will be detailed in Chapter 5. The control algorithm is implemented in cRIO-9063 which is a Digital Signal Processor (DSP) / Field Programmable Gate Array (FPGA) from National Instruments [8]. The system operates using LabVIEW software from National Instruments. This controller takes care of modulation algorithm to create gating signals for the switches, reads analog signals from sensors and therefore adjusts the output voltage and current of the multilevel converter. The cRIO-9063 is selected to provide high bandwidth for the control algorithm to ensure the system stays robust and reliable. It should be noted that this controller has 4 input module slots that can be configured. Properties of the hardware platform is detailed in Chapter 5.

Moreover, a Texas Instruments LAUNCHXL-F28379D real-time DSP is also used as a slave controller. This controller is a separate safety monitoring system that takes care of fault signals and shuts down the system by sending a signal to cRIO-9063 under a fault condition. The LAUNCHXL-F28379D has a MATLAB/Simulink plug-in where all the signals may be monitored in pseudo real-time.

4.2.4 DC-DC Converter Design

The system consists of a DC-DC converter in each module in order to operate the PVs at their MPP voltage, and also provide a relatively stable DC voltage to the CHB input. If the DC link left uncontrolled, the DC link voltage assumes the battery voltage, decreasing the efficiency of PV generation and also degrading the AC output current waveform as this is

uncontrolled. Figure 4.3, shows a bidirectional DC-DC converter utilising a battery pack. It has a conventional half-bridge design, consisting of two switches S_1 and S_2. These switches operate in a complimentary manner, where the duty cycle is compared with a sawtooth carrier to produce PWM gate pulses. Four quadrant operation is not required as the direction of current flow into the utility supply is determined by the grid side current controller and output bridge connected to nodes A and B.

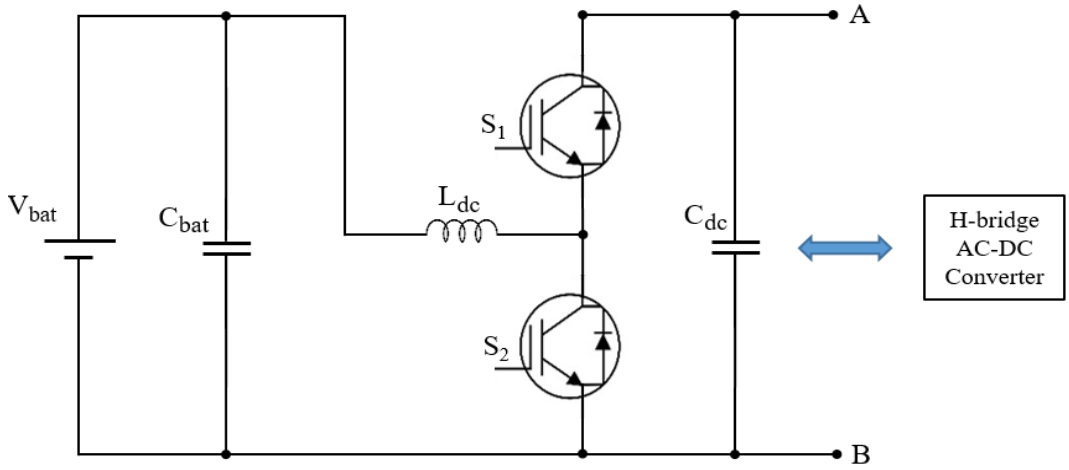

Figure 4.3: Bidirectional DC-DC converter

The electrical specifications for the bidirectional DC-DC converter are given in Table 4.2. Some of these values are taken from the battery and CHB converter to determine the operating range of the DC-DC converter in a single module. It is assumed that CHB converter draws equal power from individual series connected modules.

Parameter	Symbol	Value
Output power	P_{dc}	1 kW
Output voltage	V_{dc_m}	100 V_{DC}
Input voltage	V_{in}	65.25 – 100 V_{DC}
Switching frequency	f_{sw}	40 kHz
Inductor current ripple	Δi_L	< 10 % of output current

Table 4.2: Specifications of bidirectional DC-DC converter

Considering the boost operation of the DC-DC converter, the duty cycle of the converter is given in equation (4.1).

$$V_{out} = \left(\frac{V_{in}}{1-D_{boost}}\right) * \frac{1}{\eta} \tag{4.1}$$

The duty cycle for minimum and maximum input voltages can be calculated. Efficiency 'η' in a DC-DC converter is typically between 85-95%, however, for the simulation study we assume that the devices are lossless. Using the given values, the duty cycle varies between 0 and 0.3425, for the battery being fully charged and at its cut-off voltage respectively. The minimum practical inductance value can be calculated with equation (4.2). The minimum inductance value is determined by the input and output voltage, inductor current ripple and the switching frequency of the converter.

$$L_{min} > \frac{V_{in_{(\min)}} * (V_{out} - V_{in_{(\min)}})}{\Delta i_L * f_s * V_{out}} \tag{4.2}$$

The switching frequency of the DC-DC converter is selected to be 40 kHz, by considering the impact of frequency on device volume. Also, this frequency is inaudible to human ear. The inductor current ripple is assumed to be 10% of the output current (I_{out}), therefore the minimum inductor value can be calculated to be 563 μH. This value will be used for simulation studies.

Following this the RMS inductor current I_L, may be calculated using equation (4.3).

$$I_L = \frac{I_{out}}{1 - D_{boost}} \tag{4.3}$$

The inductor RMS current is therefore 15.21A_{rms}.

The output capacitance value may be then calculated using equation (4.4), given below.

$$C_{out} > \frac{I_{out_{(\max)}} * D_{max}}{f_s * \Delta V_{out}} \tag{4.4}$$

The DC-DC converter's output is coupled to the cascaded H-bridge's input, therefore they form a two-stage conversion system. The CHB DC link capacitance requirement is higher than the output capacitance of the DC-DC converter, therefore the DC link capacitance selection will be explained in section 4.2.5. Having higher capacitance at the output of the DC-DC converter may increase the settling time of the output voltage waveform, but also reduces the output voltage ripple 'ΔV_{out}'. In the DC-DC converter simulation, an output capacitance value of 270 μF is used, considering equation (4.4).

The bidirectional DC-DC converter is tested for buck and boost operation in MATLAB/Simulink based simulation. All aforementioned values are used for both simulation studies. As the buck mode duty cycle is lower than that of the boost mode, system component value requirements are lower, therefore the calculations are omitted here.

In order to simulate the boost mode, a 10 Ω resistor is connected as the load of the converter, in order to extract the correct power rating from battery (1 kW). Figure 4.4 shows the Simulink model of boost mode, bidirectional DC-DC converter.

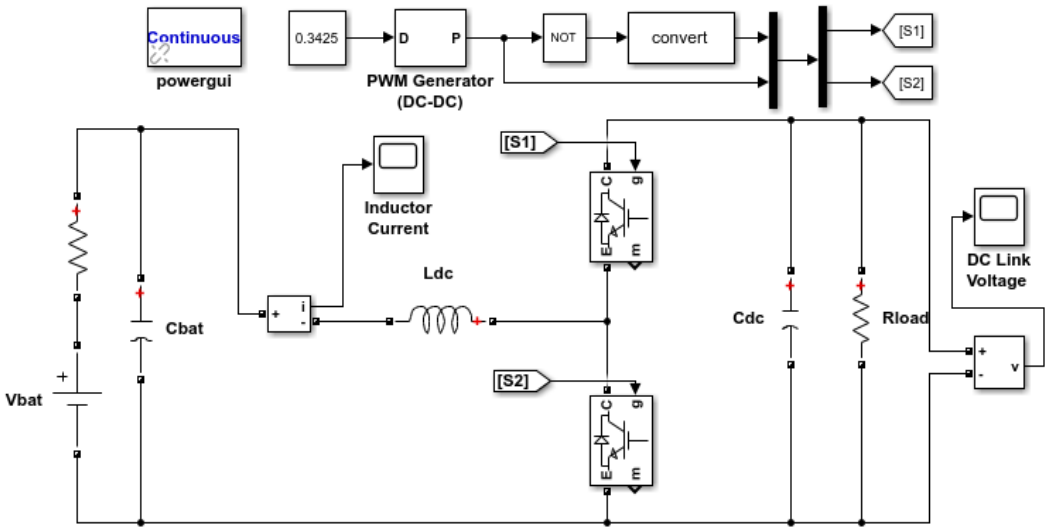

Figure 4.4: Bidirectional DC-DC converter boost mode MATLAB/Simulink Model

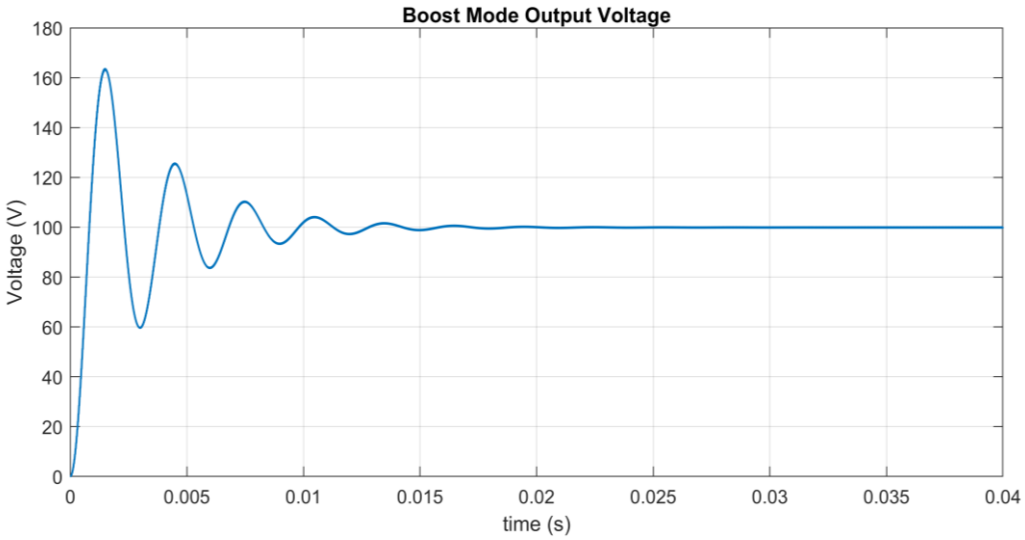

Figure 4.5: Bidirectional DC-DC converter boost mode output voltage waveform

Figure 4.5 illustrates the output voltage waveform of the boost mode operation of the bidirectional DC-DC converter. The simulation is performed as an open loop test on a fix duty cycle (D = 0.3475) and the input voltage is the minimum battery voltage. From Figure 4.5, the settling time of the converter is found to be around 22 ms.

In buck mode, the battery is replaced with a load. Moreover, the load becomes a DC source compared to boost mode, representing a voltage source for charging the battery. For buck operation, nominal battery charging voltage is assumed to be 90 V, therefore duty cycle is

reduced to 0.1. Figure 4.6 shows the Simulink model of buck mode bidirectional DC-DC converter.

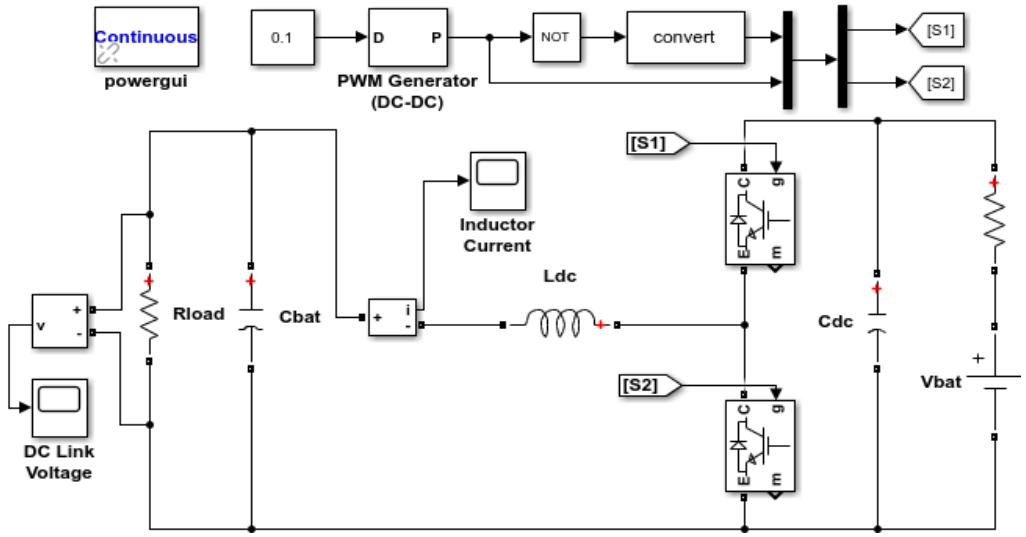

Figure 4.6: Bidirectional DC-DC converter buck mode MATLAB/Simulink Model

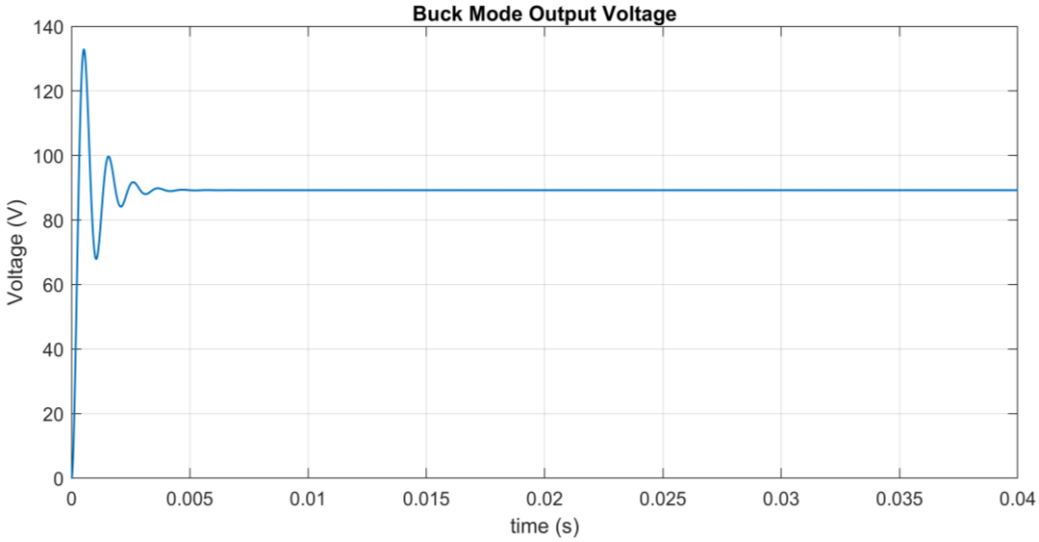

Figure 4.7: Bidirectional DC-DC converter buck mode output voltage waveform

Figure 4.7 illustrates the output voltage waveform of the buck mode operation of the bidirectional DC-DC converter. The simulation is again performed as open loop test with a fix duty cycle of (D = 0.1). Also, input voltage is the nominal battery charging voltage. The settling time of the converter is around 5 ms.

Looking at the results from abovementioned Figures 4.5 and 4.7, it can be said that the output voltage waveforms of open loop tests are at the desired range.

4.2.5 Cascaded H-bridge Converter Design

The cascaded H-bridge has 4 modules, connected in series to form the AC side of the converter, and is coupled to the utility grid via a symmetrical LCL filter. Conversely, each module is connected to a DC-DC converter which is coupled to a battery pack and PV array. This converter produces 9 output voltage stages. Therefore it is possible to generate output voltage levels $-4V_{dc}, -3V_{dc}, -2V_{dc}, -1V_{dc}, 0V,\ +1V_{dc}, +2V_{dc}, +3V_{dc}$ and $+4V_{dc}$. Figure 4.8 shows a 9-level cascaded H-bridge converter.

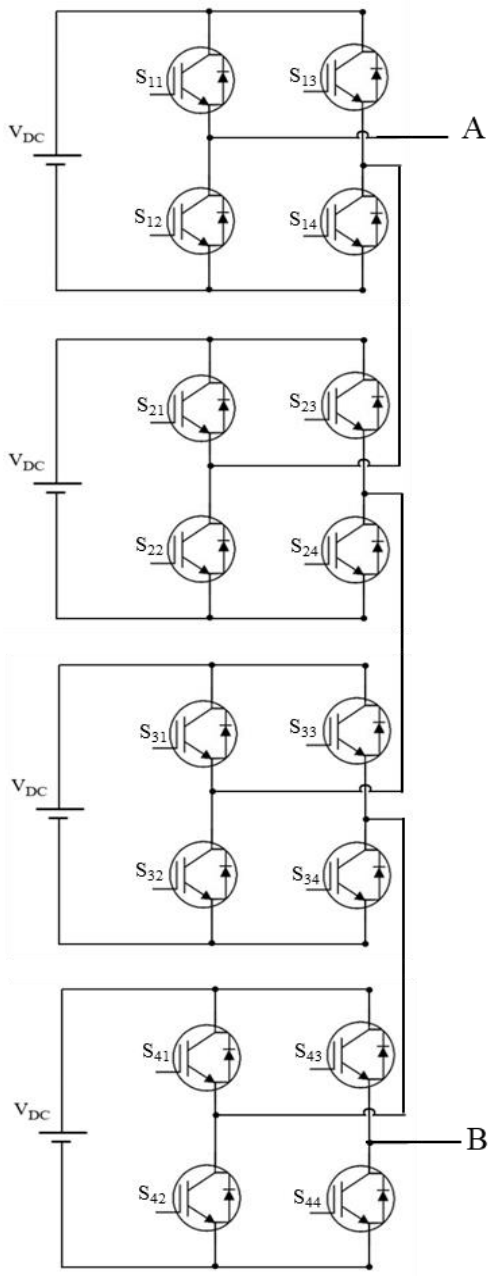

Figure 4.8: 9-level cascaded H-bridge converter topology

The DC link voltages need to be smoothed by DC link capacitors C_{dc}. Assuming the power is shared between all modules, it is possible to calculate the required value of DC link capacitance in equation (4.4) [9].

$$C_{dc} = \frac{\Delta V_{dc} * I_{ac}}{V_{dc} * f_{fund}} \tag{4.4}$$

where the peak-to-peak DC link voltage ripple is ΔV_{dc} and specified to be maximum 6%. A 4 kVA system at 230 V_{AC} is rated for 17.39 A_{RMS}. Using the equation, a total of 21 mF of capacitance is required for the converter. Considering 4 modules sharing the transferred power, 5.25 mF of capacitance is therefore required per H-bridge module. This should limit the switching ripple at isolated DC links to a maximum of 6%.

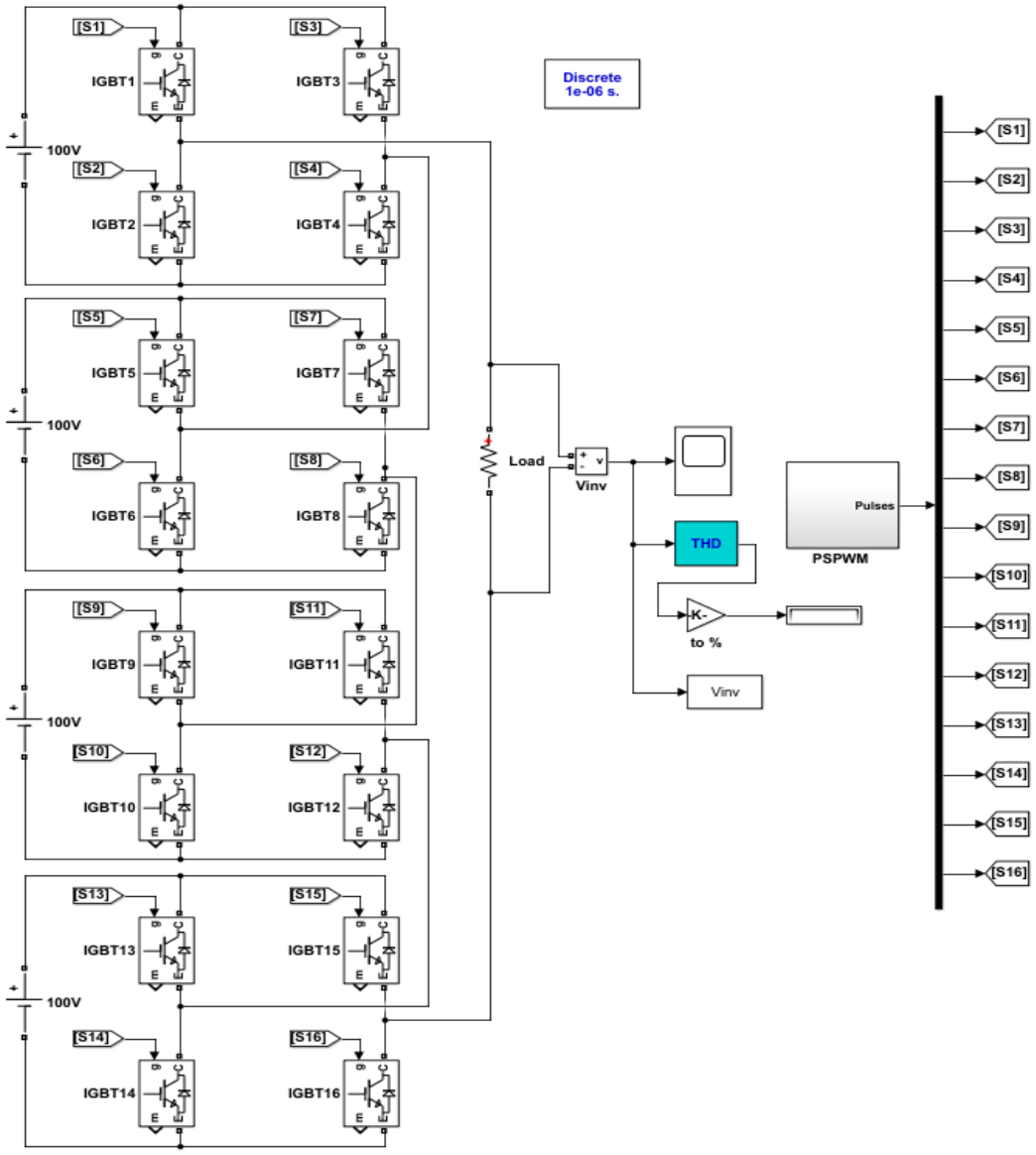

Figure 4.9: 9-level cascaded H-bridge converter MATLAB/Simulink Model

For the sake of simplicity in open loop simulation, the DC-DC converter is omitted and 100 V constant voltage sources used instead, and also an output load of 10 Ω is used for the load. The MATLAB/Simulink model and the corresponding output voltage waveform across the load resistor are given in Figure 4.9 and 4.10 respectively.

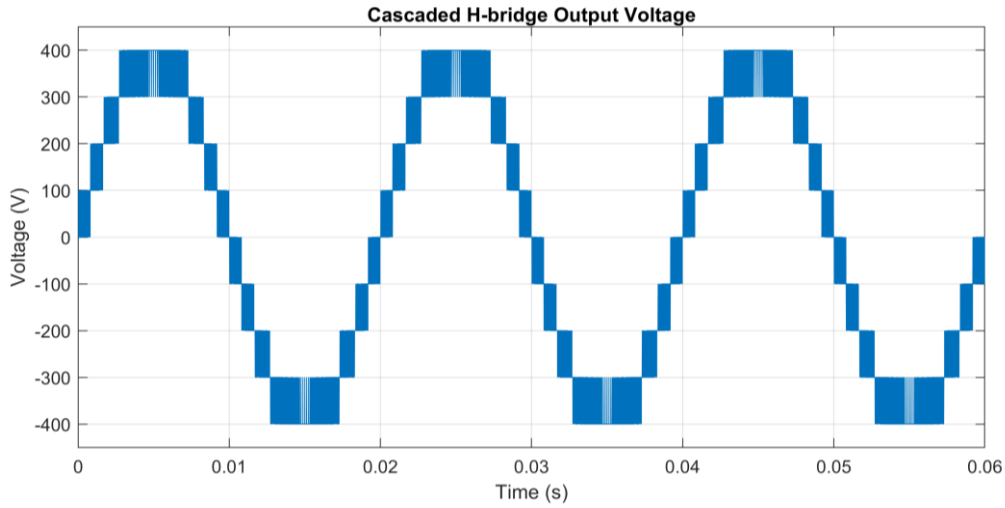

Figure 4.10: 9-level cascaded H-bridge output voltage waveform

The output voltage waveform harmonic spectrum for a 9-level CHB supplying a resistive load with PSPWM at 4 kHz is shown in Figure 4.11. The THD value of output voltage with a modulation index of 1 is found to be 13.73% at the Nyquist frequency (half of the sampling frequency of simulation).

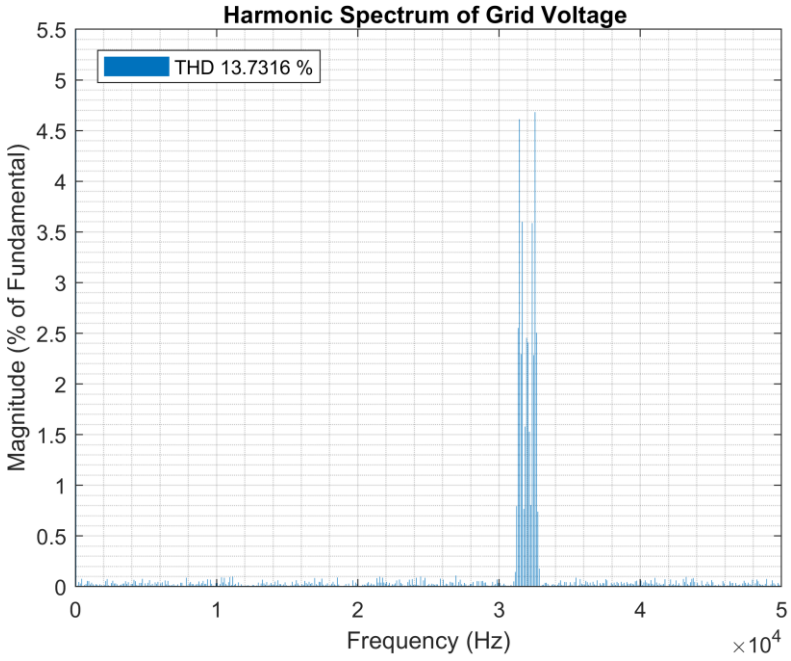

Figure 4.11: Harmonic spectrum of 9-level CHB output voltage with PSPWM

4.3 Full System Simulation

This section contains simulations of the full system including batteries, PV arrays, DC-DC converters and cascaded H-bridge coupled to the utility grid. In this system, closed loop controllers are present for controlling the DC link voltage and the grid voltage and current. The implemented algorithm for grid current control implemented in the synchronous rotating frame (DQ axis) in order to achieve independent active and reactive power control. This algorithm will be explained later in Chapter 6. A full circuit diagram is provided in Figure 4.12.

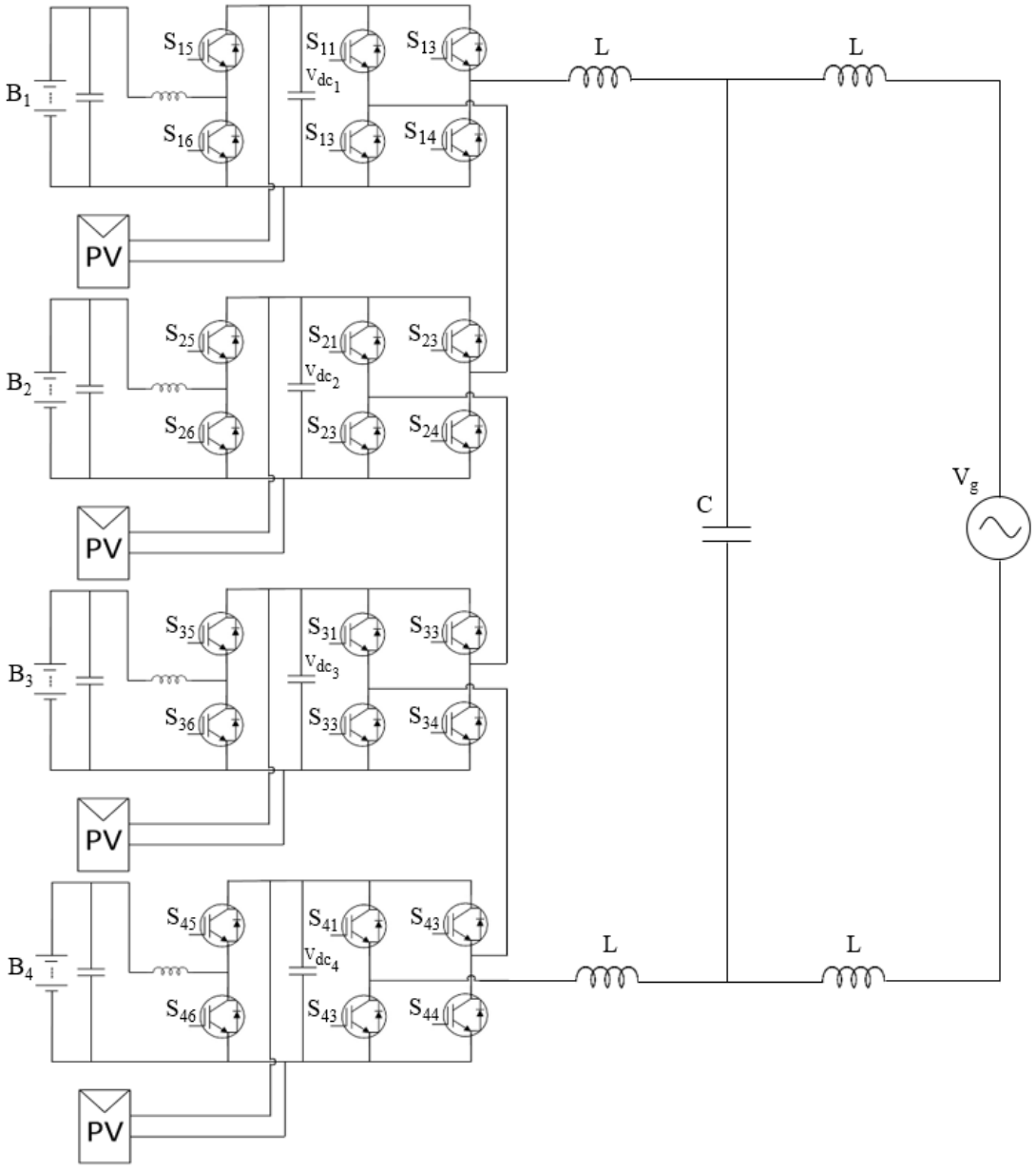

Figure 4.12: Full system circuit diagram

MATLAB/Simulink software is used for full system simulation. The battery voltage is maintained at 85 V, which is accepted as the nominal battery voltage. Here, batteries in each module have an identical State of Charge (SOC) of 50%. The standard built in Lithium-ion Simulink battery model is used with a capacity of 10 Ah. The nominal battery voltage is boosted up to the maximum power point voltage of the PVs (100 V_{DC}) in each module to maximise the power extracted. Maximum power point tracker (MPPT) works with a Perturb and Observe algorithm due to the ease of implementation. The Perturb and Observe algorithm is a standard approach to MPPT for PV arrays, based on monitoring the power output of the PV and changing the reference voltage fed to the DC-DC converter depending on the previously read power data [10].

The switching frequencies of DC-DC and AC-DC converters are 40 kHz and 4 kHz respectively, whereas the fundamental grid component is 50 Hz. The symmetrical LCL filter has 2x 2.34 mH inductors on the converter side and 2x 1.17 mH inductor on grid side, along with a capacitor of 9 µF. These values create a filter with resonant frequency of 1.34 kHz, which is below half of the AC-DC converter's switching frequency to prevent resonant operation and filter out the switching frequency components from the output waveforms.

It is important to examine the results from the power exchange perspective between the power sources in the system. Figure 4.13 shows the real power demand to be fed into the utility grid, the system real power exchange, battery power and PV power. In order to make the simulation more realistic, the change in irradiance is limited by a rate limiter block.

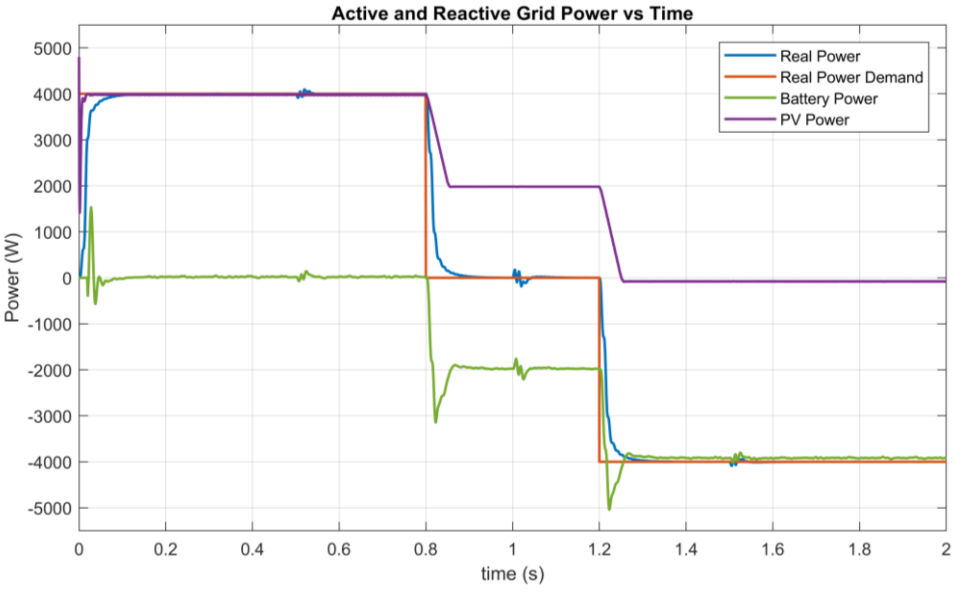

Figure 4.13: Power exchange between the power sources in the system

The requested grid demand by the operator is equal to the rated power at the start of the simulation. Until 0.8 second, 4 kW power is injected into the utility grid, which is generated by PVs therefore the batteries are idle. From 0.8 to 1.2 seconds, there isn't any power exchange from/to the grid, therefore the generated 2 kW from the PVs is absorbed by the batteries. From 1.2 seconds to the end of simulation, PV generation stops and batteries are charged by the utility grid at rated power. Examining the demand and real power curves, it is possible to say that the closed loop controller reaches its steady state value in around 100 ms without any overshoot. Figure 4.14 shows the active and reactive power demand and exchange with the utility grid.

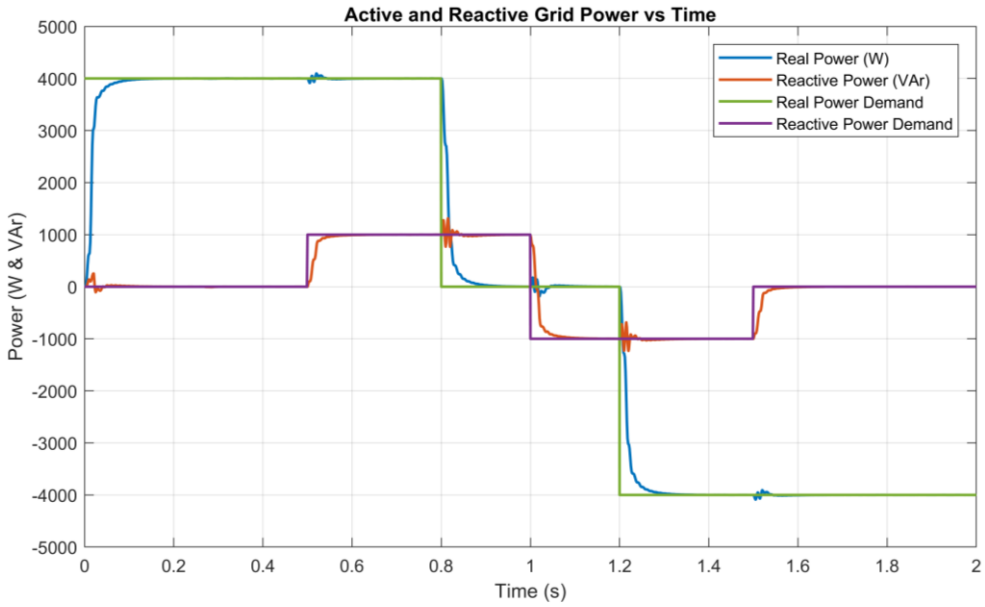

Figure 4.14: Active and reactive power exchange with the utility grid

Within the same simulation, the reactive power is also controlled independently. From 0.5 to 1 seconds of simulation, reactive power demand is set to 1 kVAr. Again, the same current controller reacts to this demand in 100 ms and reaches to steady state. Then the reactive power demand is set to -1 kVAr for 0.5 second and then reset to 0. The reactive power controller operates without any overshoot. There is a slight disruption in real or reactive power flow whenever the demand in real or reactive power changes, this is due to the current controller is trying to adjust the phase of the grid current to accommodate the demands.

The grid voltage, current and instantaneous power values are illustrated in Figure 4.15. The graph shows data from the same simulation study, illustrating the parts from 0.6 to 1.4 seconds in order to analyse the changes in grid current phase in detail.

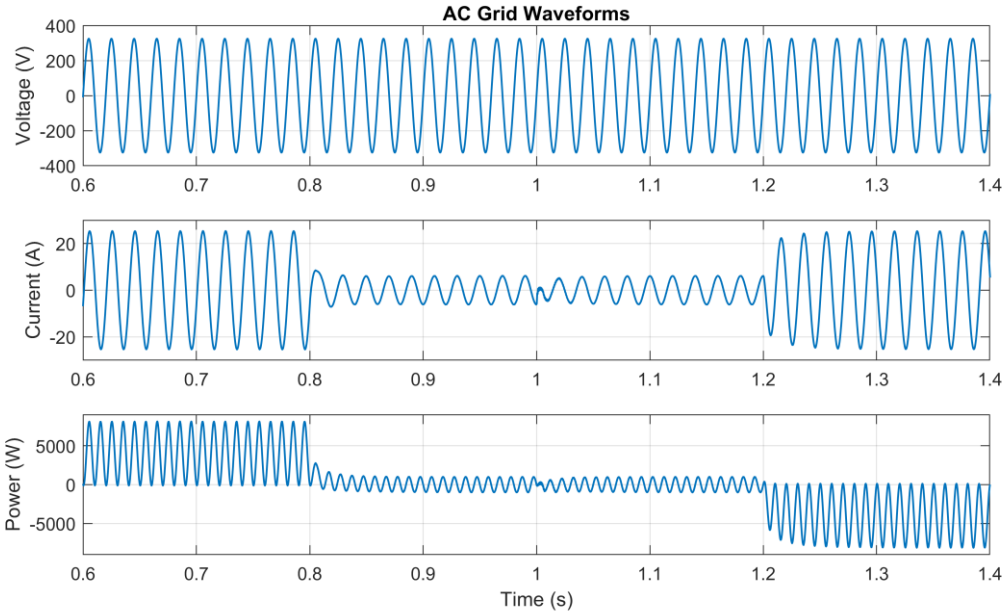

Figure 4.15: The utility grid voltage, current and instantaneous power

It can be seen that the phase of grid current changes with respect to the phase of the grid voltage, changing the direction of power transfer and/or reacting to a reactive power demand. The results seen in Figure 4.15 are filtered output waveforms. It can be seen that the waveforms are perfectly sinusoid and is of acceptable quality. In order to analyse the quality of grid current waveform, a harmonic spectrum analysis is provided in Figure 4.16.

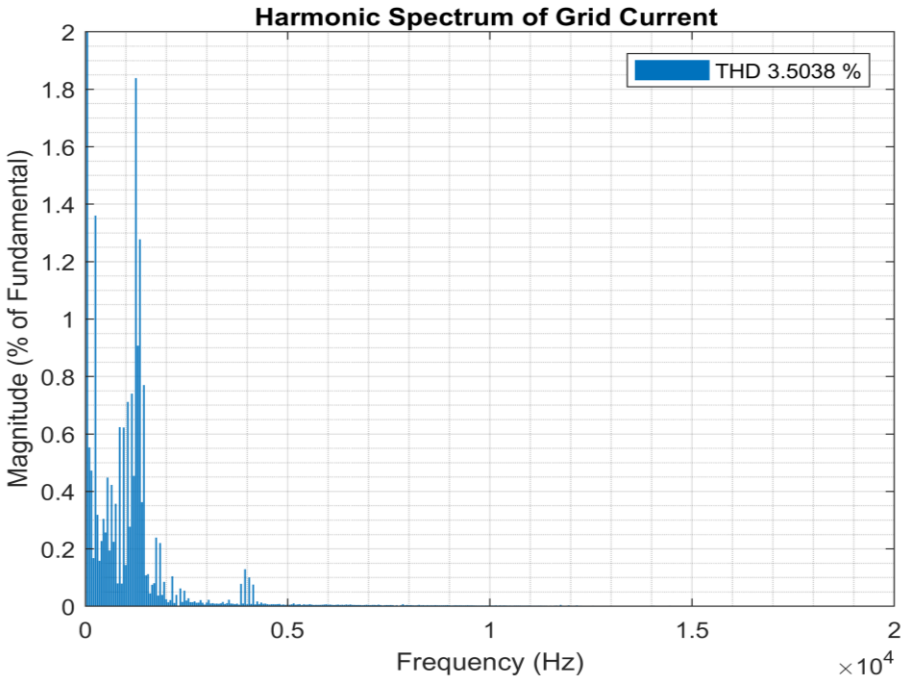

Figure 4.16: Harmonic spectrum of grid current in closed loop operation

In Figure 4.16, it is possible to see switching frequency components (4 kHz and sidebands) in grid current waveform. The Total Harmonic Distortion (THD) of the waveform is 3.5% which conforms to IEEE 519-2014 Recommended Practice and Requirements for Harmonic Control in Electric Power Systems [11].

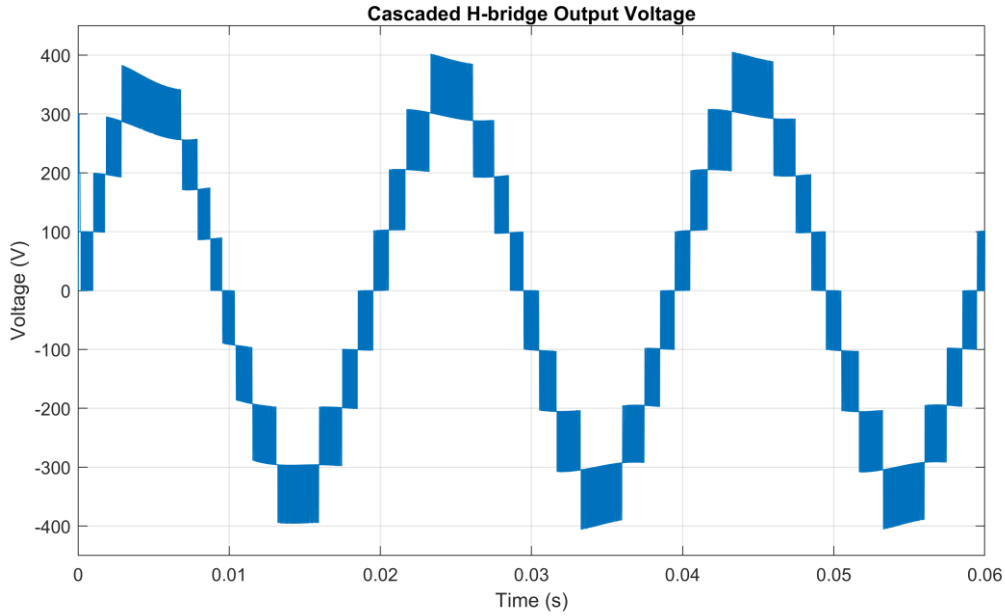

Figure 4.17: Unfiltered 9-level output voltage waveform of the cascaded H-bridge

Figure 4.17 shows the unfiltered 9-level output voltage waveform of the CHB taken from the same simulation study, where the modulation index is around 0.81.

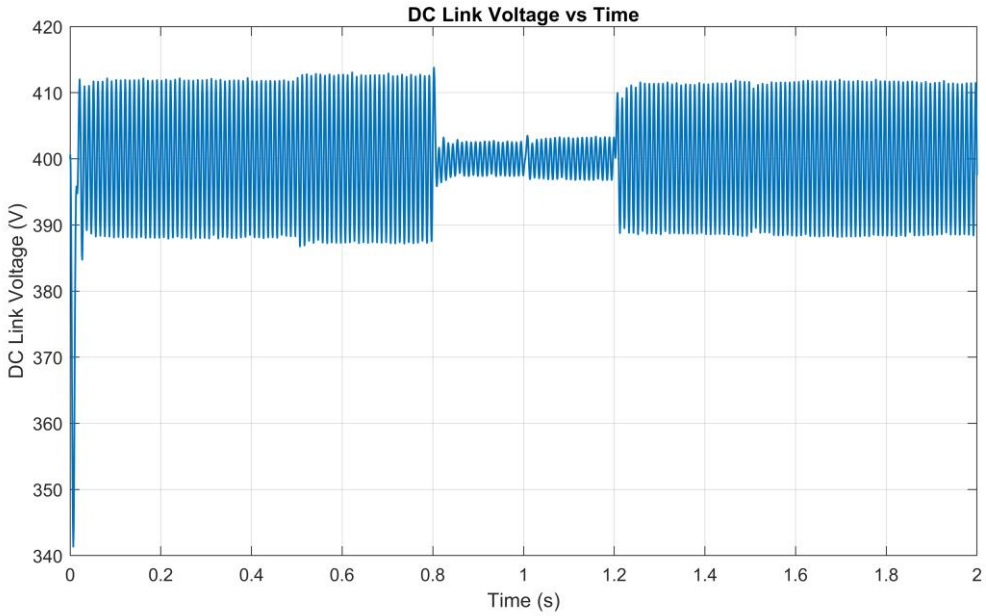

Figure 4.18: Total DC link voltage of the system

The DC link voltage reference in each module is set to 100 V_{DC} by the MPPT. Figure 4.18 shows the total DC link voltage which has a peak-to-peak voltage ripple of 24 V_{DC} at rated power. This is 6% of the total value which is in line with the calculated values.

4.4 State of Charge Balancing

The cascaded H-bridge converter consists of series connected, *n*-number H-bridges in order to achieve the desired output voltage waveform. In three-phase systems it is possible to inject zero-sequence voltage in order to achieve inter-phase battery balancing [12]. The scope of this work is single-phase CHB converters therefore this section focuses on the previously described 4 module 9-level CHB converter. In operation, it is important to manage the State of Charge (SOC) of each battery pack and ideally keep these values close to each other. In general, CHB converters allow the control of each battery/module power, and therefore a battery balancing method is achievable. It should be noted that in MLCs modulation techniques play an important role when it comes to the power transferred from/to each individual module.

In chapter 2, sinusoidal pulse width modulation methods for multilevel converters are categorised. Level shifted pulse width modulation (LSPWM) and phase shifted pulse width modulation (PSPWM) provide different characteristics when it comes to power transfer from/to individual modules. LSPWM does not provide balanced power operation as each carrier is compared with a specific part of the sinusoidal reference waveform. One way of solving this is to change the geometry of either the sinusoidal reference waveform, or the carrier waveform as seen in [13]. However, this method requires generating unique waveforms and therefore complicates the implementation of the modulation methodology. Another solution for balanced operation in LSPWM techniques is based on rotating the carrier waveforms that generate gate pulses between different modules within a specific period of time. Achieving this, balances the power transfer in each module in the long term.

LSPWM based methods require *m*-1 carriers, therefore a 9-level CHB requires 8 carrier waveforms, paired in twos for gate pulse generation in each module. Considering a balanced State of Charge scenario, a simulation study achieving balanced charging or discharging of batteries is analysed by implementing carrier rotating algorithm. This does not require complex geometric changes in the reference waveform, therefore it does not deform the output voltage and current waveforms. Figure 4.19 shows the power flow for the batteries while operating with carrier rotating algorithm in PDPWM technique.

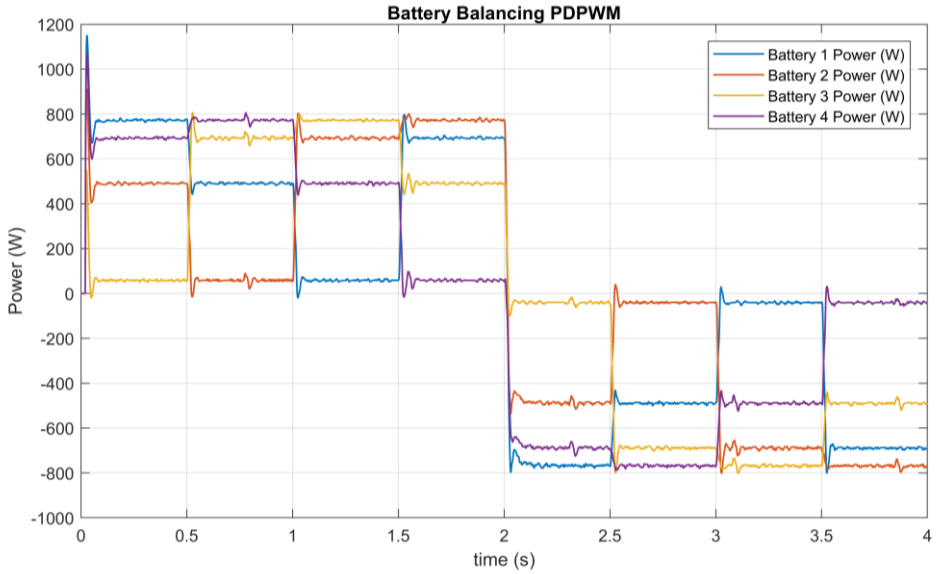

Figure 4.19: Battery power when carrier rotation algorithm is implemented in PDPWM

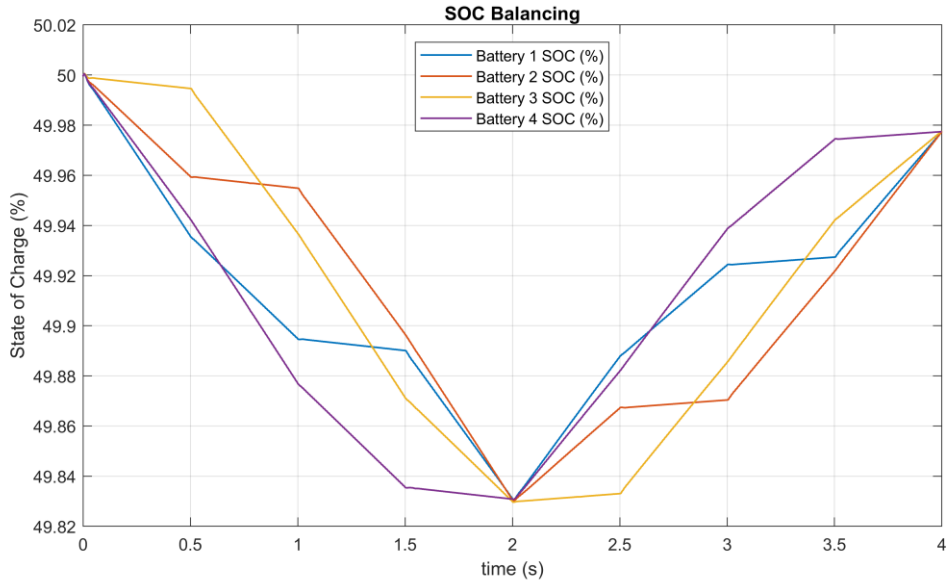

Figure 4.20: Battery state of charge when carrier rotation algorithm is implemented in PDPWM

Figure 4.20 represents the state of charge of the batteries with carrier rotation algorithm for balanced battery charge/discharging. It can be seen that carriers are rotated with periods of 0.5s. The start and end SOC of all batteries are same after each 2 second of operation.

Carrier rotation can also be applied to batteries with unbalanced SOCs. In order to achieve this, the average SOCs of all batteries needs to be calculated. Equations (4.5) can be used for finding the average SOC (where m is the number of modules and j=1,2,…,m).

$$SOC_{average} = \frac{\sum_j^m SOC_j}{m} \tag{4.5}$$

The error while discharging and charging batteries are given in equations (4.6) and (4.7) respectively.

$$SOC_{error_j} = SOC_j - SOC_{average} \tag{4.6}$$

$$SOC_{error_j} = SOC_{average} - SOC_j \tag{4.7}$$

Having two different equations for both discharging and charging modes results in opposite coefficients in the calculated error, therefore the same carrier waveforms can be selected for the same batteries in both modes. After finding the SOC error for each battery, a priority list can be made to select which module to be dis/charged with the most appropriate carrier.

In contrast, phase shifted pulse width modulation (PSPWM) naturally transfers balanced power from/to the modules, which makes it a popular modulation algorithm in CHB converters. In order to achieve battery balancing using this modulation method, the amplitude of the reference wave needs to be adjusted for each module. Again, SOC error in each module needs to be calculated considering equations (4.5), (4.6) and (4.7). The average of the modified reference wave amplitudes needs to be equal to the amplitude of original reference waveform in order not to disrupt the operation of the closed loop controller. In this study, a proportional controller is assigned to modify the sinusoidal reference waveform with respect to the error in SOC. It should be noted that the amplitude of the reference waveform must not allow it to enter the over-modulation region.

In order to prove the effectiveness of the algorithm, a simulation study with unbalanced battery SOCs is undertaken. Figure 4.21 shows the SOC of each battery in PSPWM.

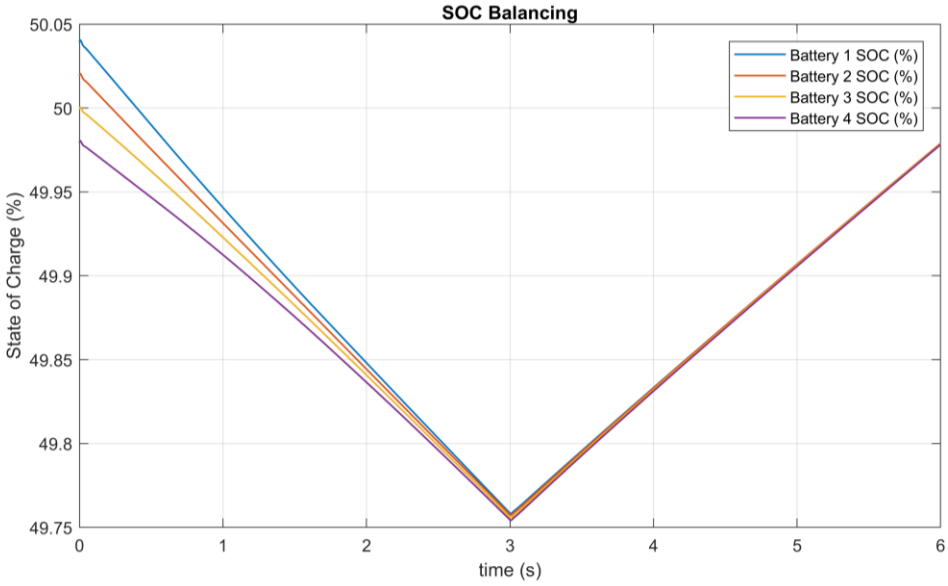

Figure 4.21: Battery state of charge when battery balancing algorithm applied in PSPWM

The initial SOC of each battery is selected to be 50.04%, 50.02%, 50% and 49.98% for batteries in module 1, 2, 3 and 4 respectively. Figure 4.21, shows that after 3 seconds of discharging and charging, the SOC of batteries in all modules are balanced.

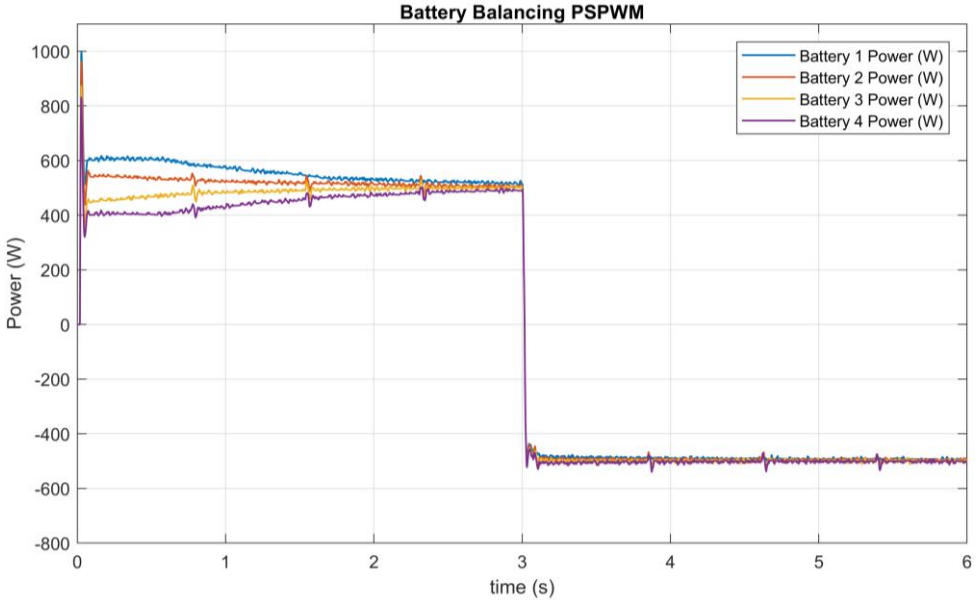

Figure 4.22: Battery power when battery balancing algorithm applied in PSPWM

Figure 4.22 shows the battery power in each module. It can be seen that the power levels extracted from the batteries are different at the start of simulation in order to balance the SOC. Towards the end of the simulation, the power injected into each battery becomes balanced as each SOC of each battery becomes balanced.

4.5 Co-simulation with LabVIEW and Multisim

The programming of the hardware platform is implemented in the National Instruments (NI) LabVIEW software suite. LabVIEW allows real-time communication with a hardware platform, and enables the user to create a graphical user interface for capturing and observing the data. Before building the converter, it is possible to use NI LabVIEW and NI Multisim software with the co-simulation plug-in to design a closed-loop point-by-point simulation of the controller FPGA code which will communicate with the CHB virtual circuit. Both programs allow the user to take advantage of two different simulation engines; such as the analogue simulation engine of Multisim, and digital simulation engine of LabVIEW. This allows verification of the effectiveness of the digital control logic, before constructing the actual CHB circuit. In this way, co-simulation enables insertion of Multisim models into external mode of LabVIEW software, therefore both programs can communicate whilst FPGA code controls the virtual circuit in Multisim.

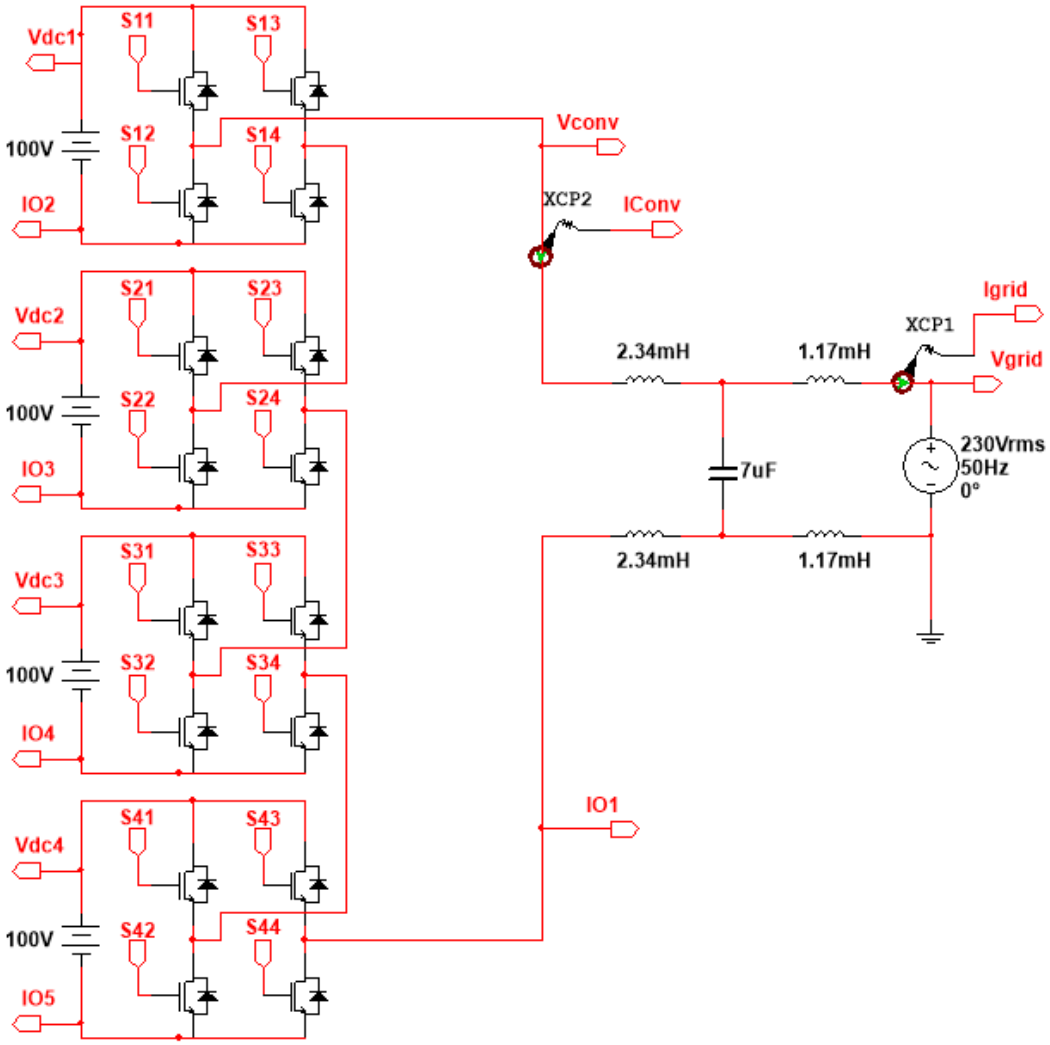

Figure 4.23: Multisim model of 9-level single-phase CHB converter

Figure 4.23 shows the Multisim model of the CHB with isolated DC sources, a symmetrical grid LCL filter and the utility grid. In order to achieve a closed loop system, DC link voltages of each module, grid current and grid voltage are measured and then exported to NI LabVIEW. The measured values are converted into the synchronous rotating frame in the FPGA, then the reference set-points of the grid current are followed by the implemented closed loop system for active and reactive power control.

Figure 4.24 shows the co-simulation model consisting of the FPGA code and Multisim interface in a control and simulation loop in LabVIEW. The real-time FPGA code is converted into the discrete time domain in order to allow synchronous communication with Multisim. Also the digital logic outputs of gate pulses from the FPGA code are converted into integers, which is the correct format for Multisim.

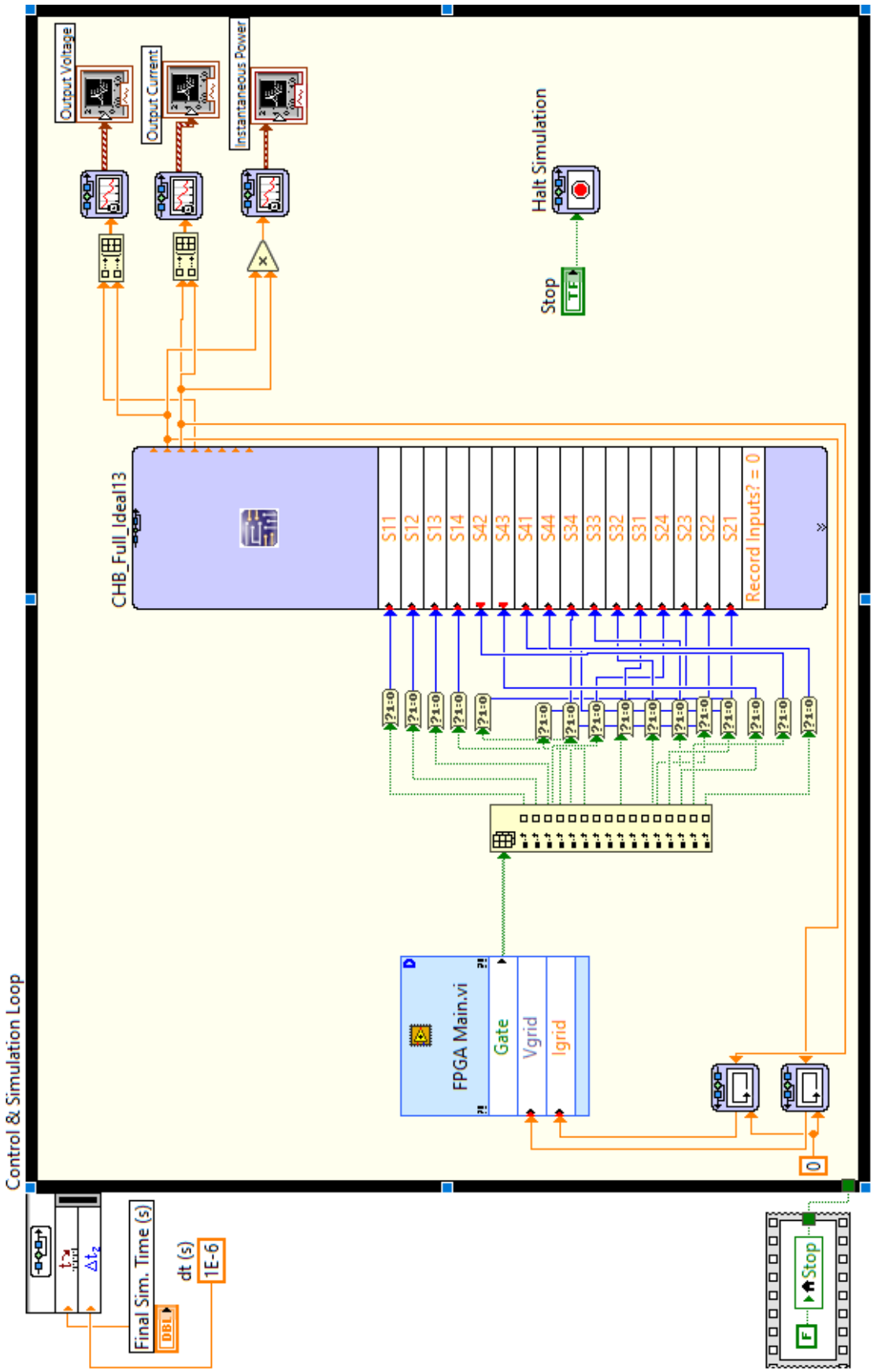

Figure 4.24: Co-simulation model in NI LabVIEW software

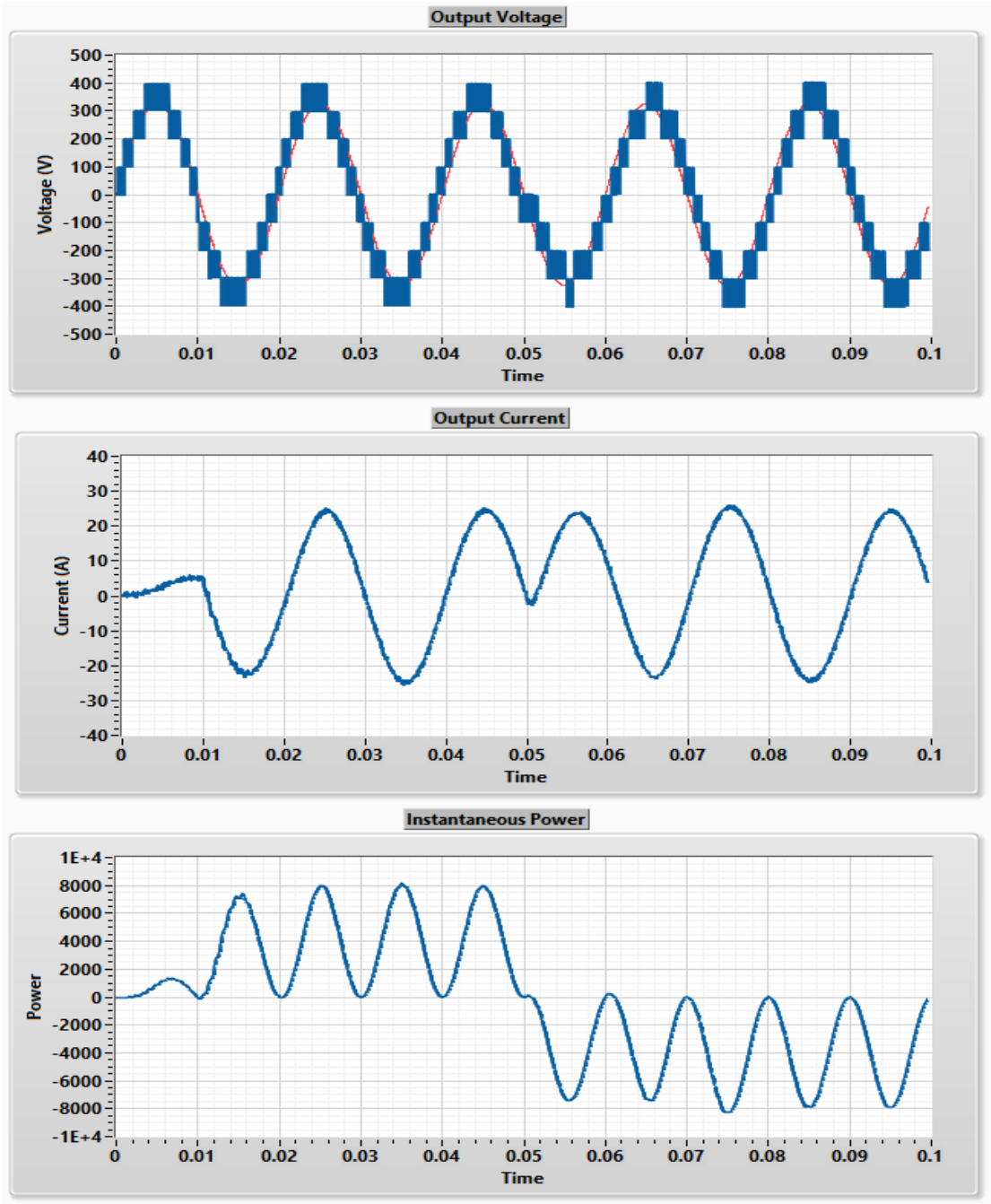

Figure 4.25: NI LabVIEW front panel showing converter voltage, gird current and power

Figure 4.25 shows the front panel of co-simulation in LabVIEW. The converter and grid voltage are represented in navy blue and red respectively, together with the grid current and grid instantaneous power. At 0.01 second into the simulation, the closed loop system algorithm is turned on and rated power is injected into the utility grid. At 0.05 second, rated power is extracted from the grid to the isolated DC sources. It can be seen that the closed loop controller reaches to its steady state in less than 2 fundamental cycles.

4.6 Chapter Summary

Chapter 4 focused on converter design and simulations of various system components. A system is defined that utilises batteries and PVs coupled to DC-DC converters, which control each DC link voltage of a 9-level cascaded H-bridge converter. The batteries represent a modern EV's battery pack reconfigured for a second life application in a stationary energy storage system that operates with PVs. A DC-DC converter is designed that is able to provide a relatively smooth DC input for a cascaded H-bridge converter. The full system is integrated into MATLAB/Simulink to validate the mathematical analysis and the behaviour of the analog circuitry. Then NI LabVIEW and Multisim software are used to validate the operation of control algorithm without the need of the actual converter circuitry.

The following chapter covers the experimental and hardware evaluations of H-bridge power modules, control algorithm and platform, and also auxiliary circuits for signal conditioning and measurement.

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Chapter 5
Hardware Evaluation

5.1 Introduction

In Chapter 4, design parameters were selected and relevant simulations made in order to assess the operation of the desired converter. The simulations were carried out on digital platforms such as MATLAB/Simulink and NI LabVIEW. This chapter describes the prototype converter that is used to verify the proposed modulation scheme; leakage reduction PWM (LRPWM).

In order to control a multilevel converter (MLC), a control hardware platform such as a microcontroller, field programmable gate array (FPGA) or digital signal processor (DSP) must be adopted. Each of these hardware platforms has its own benefits with regards to the end application. DSPs and microcontrollers are generally cheaper products, however they are limited when it comes to implementing complex modulation algorithms for MLCs. Conversely, FPGAs assign dedicated hardware in a programmable logic circuit, therefore multiple algorithms can be executed in parallel. This operation may achieve better performance when a fast dynamic response of the MLC is required.

The FPGAs are commonly programmed using the VHSIC hardware description language (VHDL). Conventionally, implementing MLC closed loop control is time consuming however, recent advancements in graphical programming languages have simplified and shortened this process. LabVIEW software can convert graphical input into VHDL code and also manage the FPGA memory for better utilisation of hardware resources.

As mentioned in chapter 4, LabVIEW and Multisim are utilised to accelerate the design process of the FPGA based system. The proposed LRPWM algorithm is first tested with a control and simulation loop in LabVIEW, converted into an FPGA compatible version and then flashed into the hardware platform. To this end, LabVIEW FPGA based systems are presented, such as the CHB converter wind energy conversion system in [1], and DC motor speed control in [2].

This chapter focuses on hardware a platform, detailing power modules, data acquisition and sensors, and also the control platform for closed loop operation. This system is used to

evaluate different modulation schemes, assess their performance when parasitic capacitance exists between terminals of isolated DC sources and ground.

5.2 Control Platform and Implementation

In this section, the hardware used as the control platform is discussed. The control system has a low-cost microcontroller as slave controller, and an FPGA/DSP master controller for closed loop control of the overall CHB converter.

5.2.1 DSP Slave Controller

Initially, a control platform for testing power modules was selected as the LAUNCHXL-F28379D from Texas Instruments. This microcontroller board contains a TMS320F28379D chip having a dual 32-bit 200 MHz processor. The development kit also has 1 MB on-chip flash memory, up to 24 channel 12-bit analog-to-digital converters (ADCs), two 10 MHz crystal oscillators and 4x 20-pin I/O headers [3]. The LAUNCHXL-F28379D is a low cost DSP which is suitable for initial testing and basic functional control. However, this controller does not allow complex mathematical manipulation of the oscillator waveforms, and therefore level shifted PWM (LSPWM) techniques cannot be implemented. Therefore, this board is used as a slave controller, taking care of safety and fault monitoring systems in the hardware implementation. Each H-bridge module has temperature and fault signal outputs, where these active 'HIGH' signals are fed into the slave controller.

The LAUNCHXL-F28379D can be programmed with either 'Code Composer Studio' or through the MATLAB/Simulink Embedded Coder plug-in. The support package converts Simulink block diagrams into C code, and allows downloading of embedded code onto the hardware platform. External mode operation allows graphical representation of pseudo real-time data in MATLAB/Simulink, allowing the user to visualise variables.

5.2.2 FPGA Master Controller

In order to implement the complex modulation algorithm mentioned in Chapter 3, a FPGA based controller is used. The FPGA allows reconfiguration of internal integrated circuitry post device manufacture. This is achieved through a matrix of logic blocks connected via definable, programmable interconnects. The programmable routing of these interconnects, flip-flops, look-up tables and I/O headers, enables the user to adapt internal circuitry to a specific objective, paralleling the execution of desired function by using available sources.

The FPGA is required as the carrier and sinusoidal reference waveforms require mathematical manipulations when physically implementing LRPWM. In order to achieve this, a National Instruments (NI) CompactRIO (cRIO) Controller is used. The NI cRIO-9063 is a configurable embedded controller that has a 667 MHz on board processor running NI Linux Real-Time, has 512 MB and 256 MB permanent and volatile (DRAM) memory, and a 1 Gbps Ethernet port [4]. The cRIO-9063 has a Xilinx Zynq 7000 series XC7Z020 FPGA and allows 4 'C series' modules to be connected on its chassis. 'C series' modules provide solutions for a variety of applications such as analog and digital I/O, image processing, motion control etc. Here, two NI 9401, one NI 9205 and one NI 9263 are used. The NI 9401 is an 8 channel bidirectional digital I/O module with minimum accuracy of 100 ns, which is used for generating gate pulses for switches [5]. The NI 9205 is an analog input module that has 16 bits ADCs, capable of measuring 16 differential or 32 single ended analog signals, at up to ± 10 V and a rate of 4 µS [6]. Finally, the NI 9263 is a 4 channel analog output module, which can generate ± 10 V 16 bit signals at a rate of 100kS/s per channel [7]. This module is used to visualise control variables in order to better tune the closed loop current controller. Figure 5.1 shows the practical controller setup.

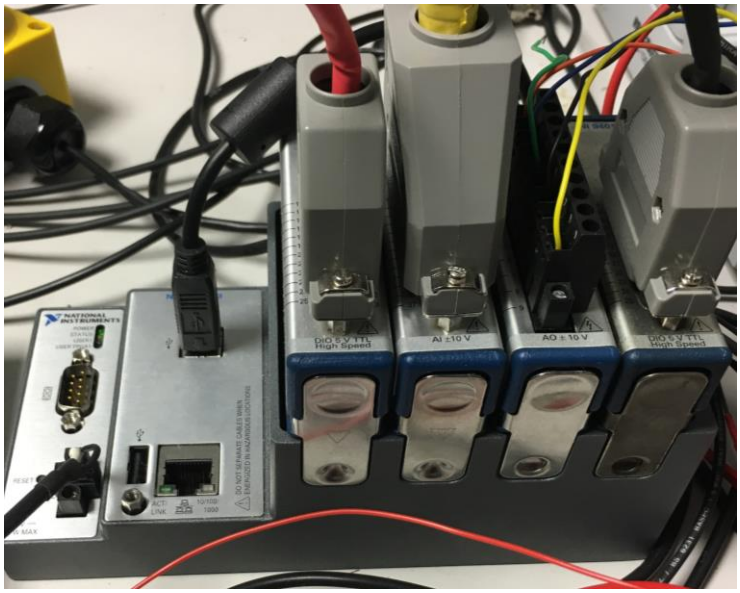

Figure 5.1: NI cRIO-9063 with 2x NI 9401, NI 9205 and NI 9263

This system can be programmed with the NI LabVIEW FPGA plugin. The LabVIEW FPGA has built-in function blocks such as PID control, DSP, I/O for interacting with 'C series' modules, waveform generators, and math functions. The algorithm is run in VI files, where these files can be transferred onto different hardware seamlessly as intermediate files are

optimised for target hardware during the compilation process. Moreover, a graphical user interface allows two-way communication between a host computer and a real-time target, such as cRIO-9063, to be established.

5.2.3 Master Controller Implementation

A master controller, cRIO-9063, is implemented by using the LabVIEW FPGA co-simulation plugin and Multisim software as mentioned in chapter 4. Initially, the modulation algorithm was implemented in MATLAB/Simulink before it is transferred into the LabVIEW code. The LRPWM is then tested with co-simulation to make sure there is congruity between simulation environments. Figure 5.2 shows 9 level CHB converter topology that is used in the experimental procedure.

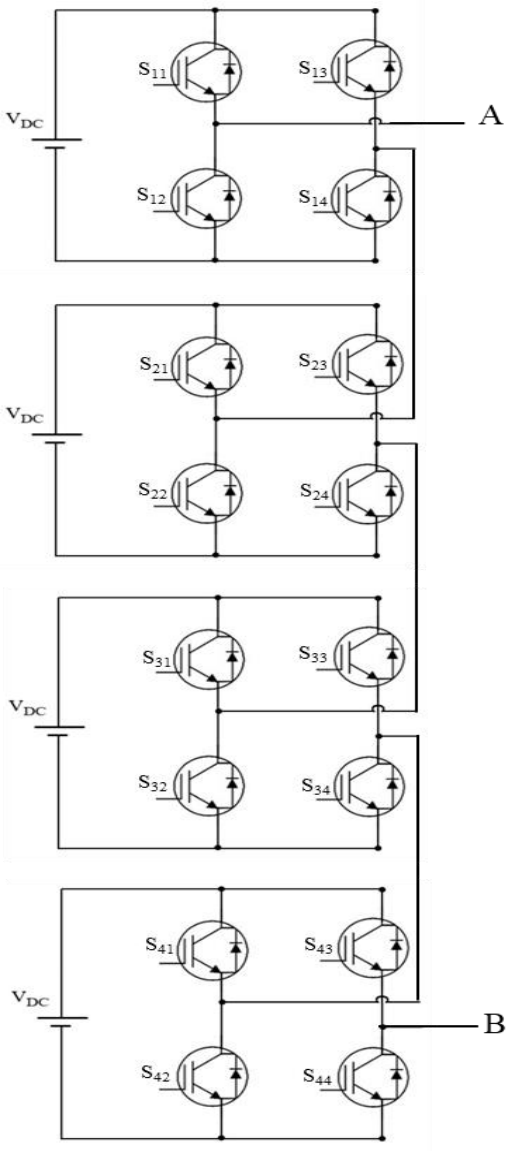

Figure 5.2: 9-level CHB converter topology

PWM gate pulse signals are generated for the circuitry in Figure 5.2. Co-simulation and experimental results of the PWM gate pulses for the 9 level CHB converter are shown in Figures 5.3, 5.4, 5.5 and 5.6.

Figures 5.3, 5.4, 5.5 and 5.6 illustrate gate signals for the LRPWM approach, when the switching frequency (f_{sw}) is 4 kHz and the modulation index (m_a) is 0.8. Figures 5.3 and 5.5 are taken from LabVIEW software whereas Figures 5.4 and 5.6 are experimental digital output waveforms of FPGA hardware.

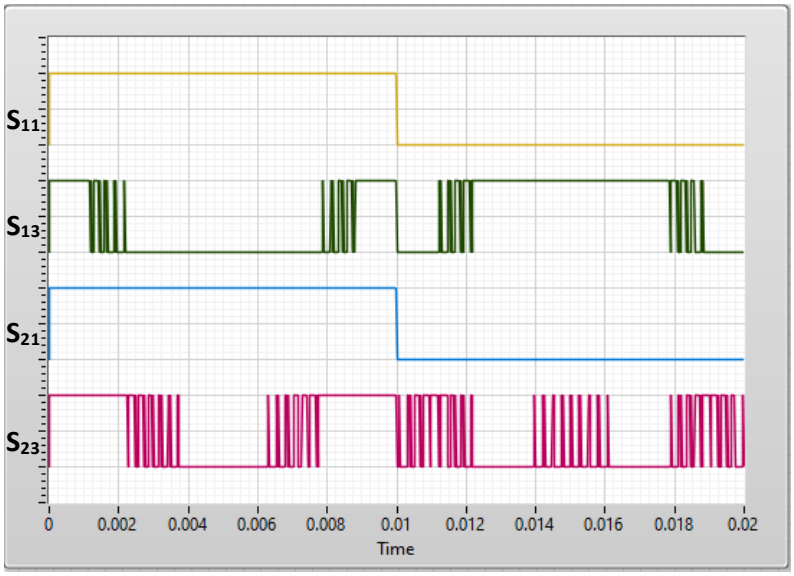

Figure 5.3: Switches S_{11}, S_{13}, S_{21} and S_{23} co-simulation output waveforms

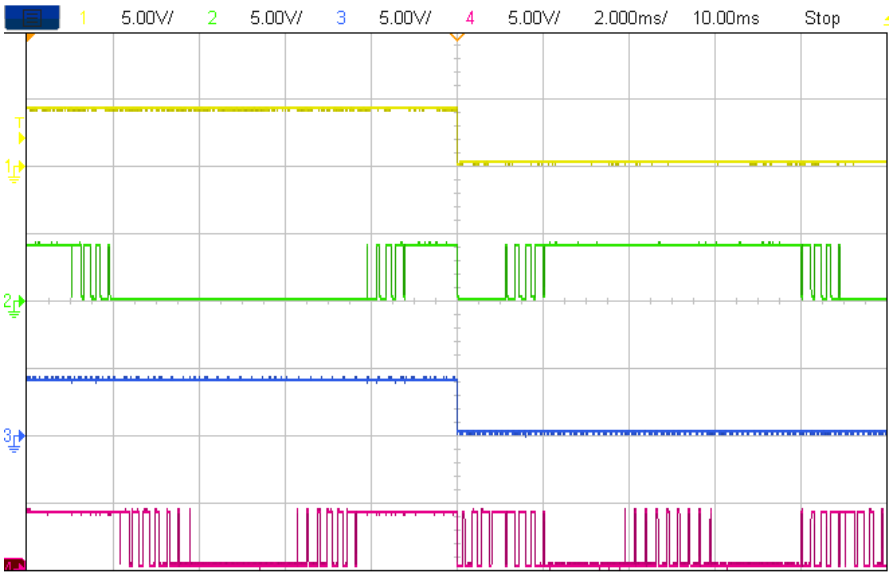

Figure 5.4: Switches S_{11}, S_{13}, S_{21} and S_{23} (Channel 1-4) experimental hardware output waveforms

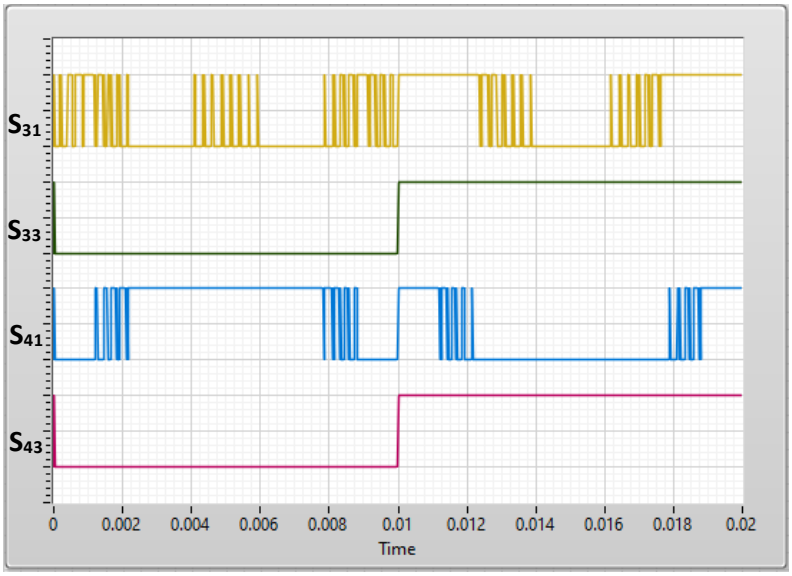

Figure 5.5: Switches S_{31}, S_{33}, S_{41} and S_{43} co-simulation output waveforms

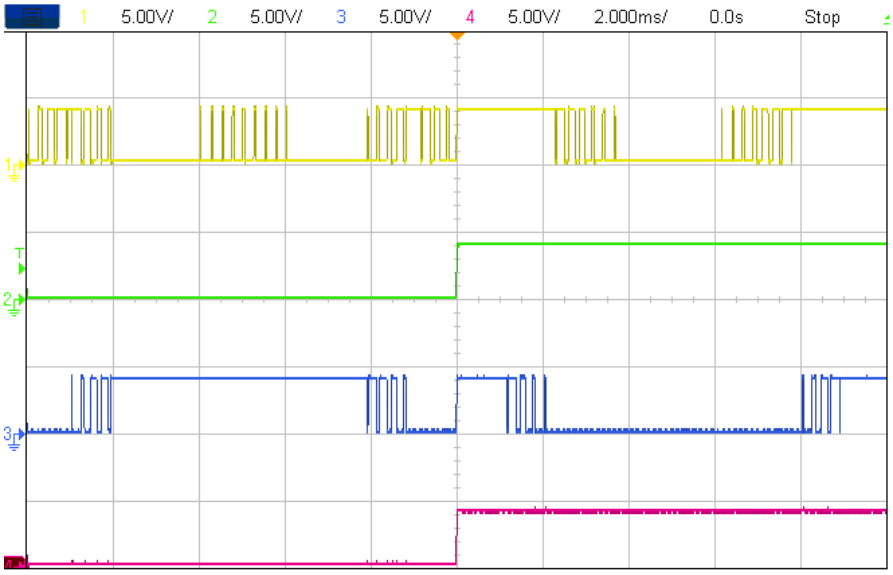

Figure 5.6: Switches S_{31}, S_{33}, S_{41} and S_{43} (Channel 1-4) experimental hardware output waveforms

Figures 5.3, 5.4, 5.5 and 5.6 demonstrate that the co-simulation environment and FPGA output waveforms are consistent. Generated FPGA outputs are between 0 and 5 V, which is the generic digital transistor-transistor logic (TTL) voltage level. The compliments of these waveforms are omitted, and the experimental result waveforms have 2 µs dead-time between switching actions in order to prevent shoot through occurring in a single H-bridge leg.

5.3 Data Acquisition and Sensors

The CHB converter is coupled to the utility grid, and therefore has to operate with closed loop control. To achieve this, isolated current and voltage measurements need to be taken from various parts of the converter. Waveforms of sensor outputs also need to be adjusted according to the input limits of the analogue input module. This section will detail current transducer, voltage sensor and signal conditioning circuits.

5.3.1 Isolated Current Transducer

LEM LA55-P and L55-P/SP1 current transducers are used for measuring currents in various parts of the converter, having transfer ratios of 1:1000 and 1:2000 respectively. These sensors are based on the Hall Effect, therefore provide galvanic isolation. The measuring range of LA55-P and LA55-P/SP1 are ± 50 A and ± 100 A respectively. It should be noted that there may be a ± 0.65 % uncertainty in the measurements, and the sensors have a maximum bandwidth of 200 kHz with a ± 15V supply. The circuit diagram for the use of the LA55-P/SP1 transducer is shown in Figure 5.7.

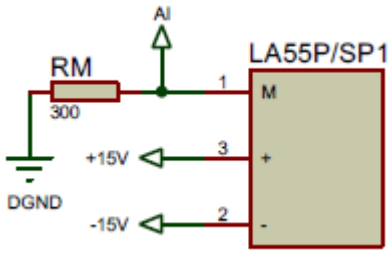

Figure 5.7: LEM LA55-P/SP1 current transducer circuit diagram

The value of R_M can be any value between 0 and 335 Ω for the LA55-P/SP1 and 0 and 135 Ω for the LA55-P, when the supply voltage is ± 15 V for maximum measurements of ± 50 A. The current consumption of the transducer is 35 mA.

In order to calibrate the sensor, a varying current source is used to provide values between 0 and 20 A in steps of 0.5 A, allowing a linear trend curve to be fitted to the response. The output values may then be calibrated in the digital platform. Figure 5.8 shows the characterisation curve of a LA55-P/SP1 current transducer.

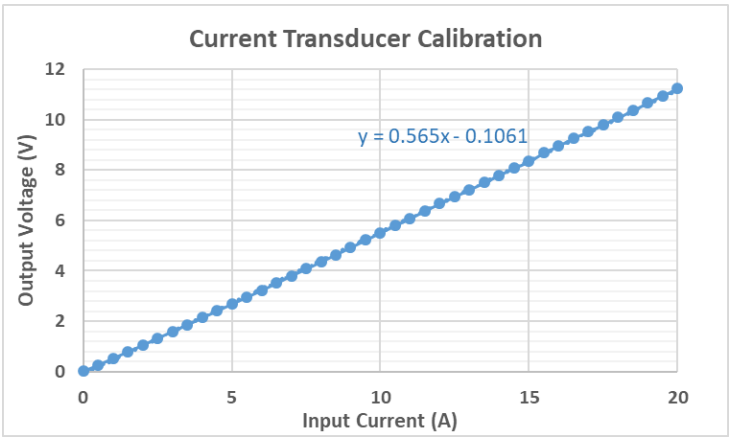

Figure 5.8: LA55-P/SP1 current transducer characterisation curve

5.3.2 Isolated Voltage Sensor

The LEM LV 25-P has a measuring range of 10 – 500 V, a transfer ratio of 2500:1000. The LV 25-P also uses the Hall Effect, similarly to the current transducer. The overall accuracy of the sensor is ± 0.8 % when the supply voltage is ± 15 V. The circuit diagram for the LV25-P is shown in Figure 5.9.

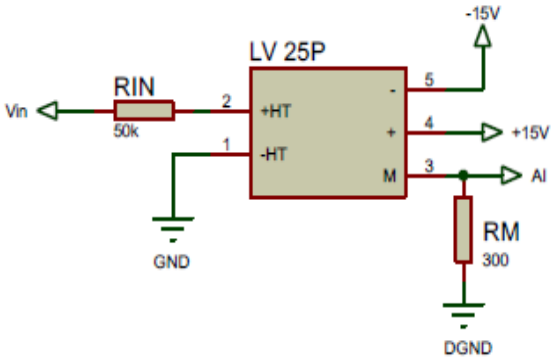

Figure 5.9:LV25-P voltage sensor circuit diagram

The maximum primary winding current in a LV25-P sensor should be 10 mA, therefore an input resistor R_{in} needs to be selected considering the maximum voltage to be measured. If the maximum voltage value to be measured is < 500 V.

$$R_{in} = \frac{V_{max}}{10\ mA} \tag{5.1}$$

$$R_{in} = 50\ k\Omega$$

$$V_{out} = (R_S + R_M) * I_S \tag{5.2}$$

$$V_{out} = (110 + 300) * 0.025$$

$$V_{out} = 10.25\ V$$

Where R_S and I_S are 110 Ω and 25 mA respectively. The value of R_M can vary between 100 and 350 Ω when the supply voltage is ± 15V.

In order to characterise the sensor, a variable voltage source is used, where the voltage values are changed between 0 – 500V in steps of 10V. A characterisation curve can then be fitted and therefore gain of this curve is used to calibrate the digital values in LabVIEW code. Figure 5.10 shows the characterisation curve of a LV25-P voltage sensor.

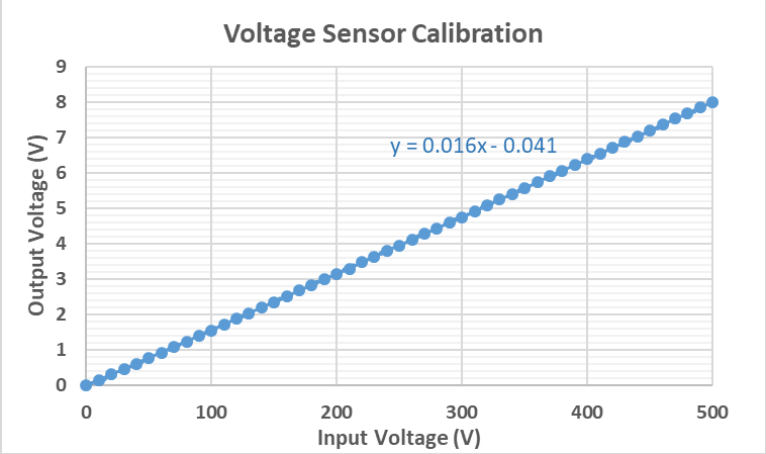

Figure 5.10: LV25-P voltage sensor characterisation curve

In order to take measurements from various parts of the experimental converter, a printed circuit board (PCB) is designed, which accommodates a voltage sensor and a current transducer, and can be seen in Figure 5.11.

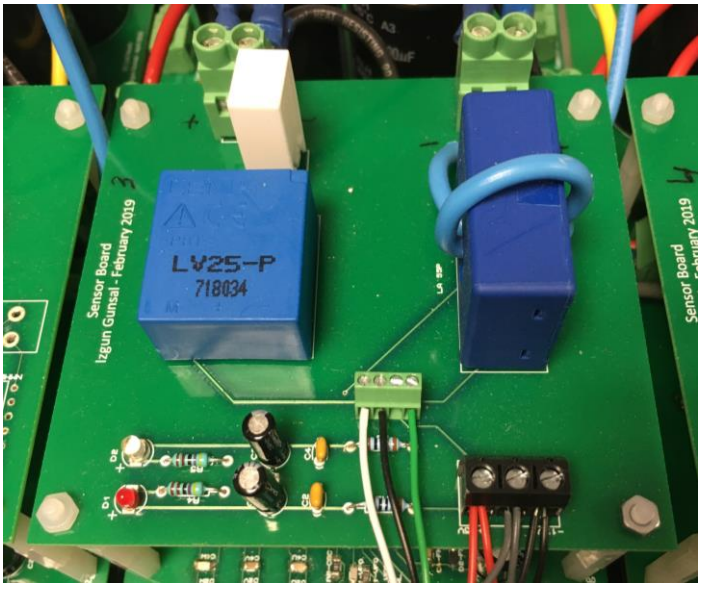

Figure 5.11: Sensor board showing LV25-P voltage sensor (left) and LA55-P/SP1 current transducer (right)

5.3.3 Signal Conditioning

For closed loop operation, 6 voltage and 6 current measurements are taken from a 9-level CHB converter. These are 4x DC link voltage measurements, 1x unfiltered converter output voltage, 1x grid voltage, 4x module leakage current, 1x grid leakage current and 1x grid current. The voltage and current sensors provide isolation and their output signals are variable voltage waveforms. The C series analogue input module NI 9205 can withstand up to ± 10 V, therefore a signal conditioning circuit is designed to limit the sensor output voltage to within this allowed limit. Figure 5.12 and 5.13 show a single channel of the signal conditioning circuit and prototype PCB respectively. The PCB consists of 12 channels, where each channel includes an inverting unity gain buffer circuit for improved noise immunity and a Schottky clamp (D3 and D4) for overvoltage protection. The voltage limit for Schottky clamp is selected as ± 10 V.

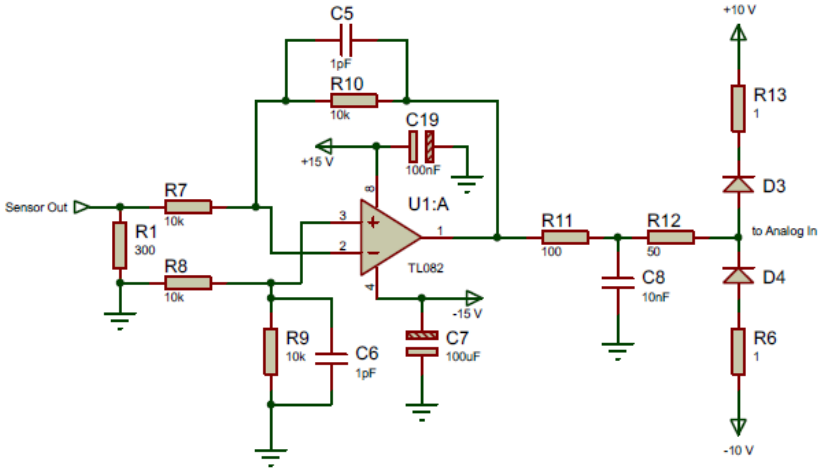

Figure 5.12: A single channel of signal conditioning circuit

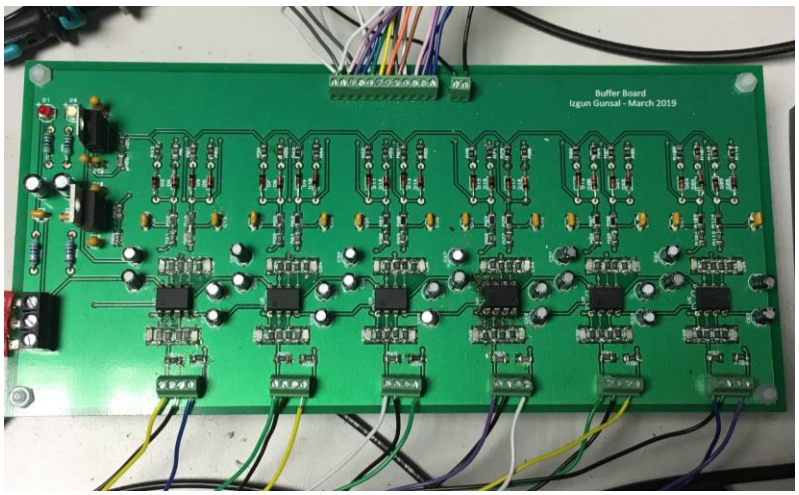

Figure 5.13: Signal conditioning board

5.4 Multilevel Converter Evaluation

This section details a 9-level CHB converter that was presented in previous chapters. Firstly, the evaluation is focused on a single H-bridge module (power module) as the CHB has a modular design, therefore all four modules are identical. Finally, the results for a 9-level CHB are analysed.

5.4.1 Power Module Evaluation

A power module consists of a single H-bridge circuit, bootstrap circuitry for driving high-side IGBTs and isolation circuitry for gate signals. Having a large number of switches in a 9-level CHB encourages the use of industry made intelligent power modules in order to increase reliability and reduce design time of the system. The intelligent power module, FNB34060T, is a three-phase bridge that can withstand 600 V at 40 A, where IGBTs are used as switches. The intelligent power module has internal gate drivers, however extra bootstrap circuitry is required for each high-side IGBT. Figure 5.14 shows the internal configuration of the FNB34060T. Each converter leg has separate open-emitter pins from low-side IGBTs that may be useful for individual leg current sensing. The FNB34060T also has built in temperature sensing, controlled under-voltage protection, and short circuit protection. In case of a violation to any of the protection circuitry, an active 'HIGH' fault signal is triggered. In order to use the FNB34060T as a H-bridge, a single leg is deactivated by sending a 'LOW' signal to the gate terminals of switches, such as S_1 and S_4 with respect to Figure 5.14.

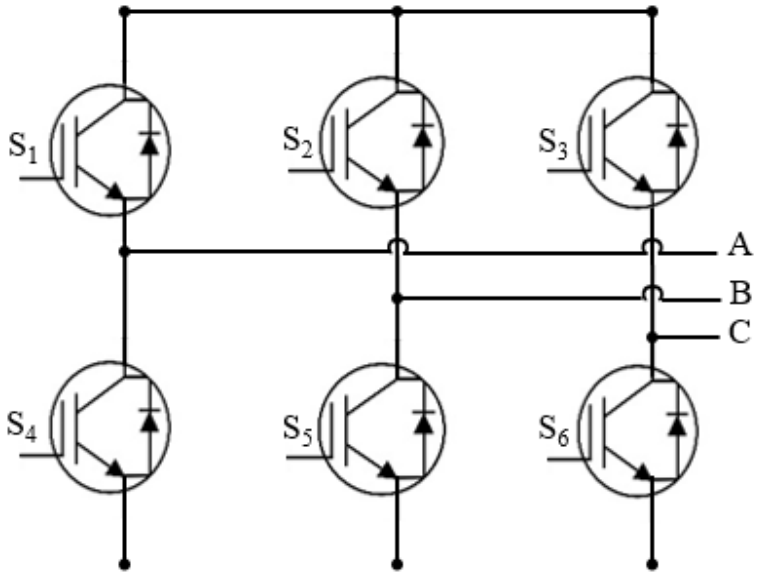

Figure 5.14: FNB34060T intelligent power module internal circuitry

A power module circuit consists of double channel optocouplers, HCPL-2630 from Avago Technologies, which can achieve a 10Mbit/s switching speed. Considering IGBTs are limited to 20 kHz maximum switching frequency, the propagation delay of optocoupler is well suited for this application.

Thermal management of the power module is important as the product datasheet specifies that a FNB34060T can operate at a maximum junction temperature of 150 ^{o}C [8]. Selection of a heatsink needs to be done after calculating power dissipation of the module. Equation (5.1) provide an approximate result for power dissipation in an intelligent power module.

$$P_{loss} = k \times (P_{sw.IGBT} + P_{conduction.IGBT} + P_{rr.diode} + P_{conduction.diode}) \quad (5.1)$$

Where *k* is the number of IGBT and diode pairs, $P_{sw.IGBT}$ and $P_{conduction.IGBT}$ are switching and conduction losses of an IGBT. Additionally, $P_{rr.diode}$ and $P_{conduction.diode}$ are losses during the reverse recovery and conduction periods of the diode. The FNB34060T datasheet provides information for energy loss of the diode and IGBT while driving an inductive load. The given test results are for 300 V_{nom} (collector-emitter voltage of datasheet test) which therefore needs to be normalised considering the application input.

$$P_{sw.IGBT} = \frac{(E_{ON}+E_{OFF})\times f_{sw} \times V_{dc}}{V_{nom}} \quad (5.2)$$

$$P_{sw.IGBT} = \frac{(1300e-6)\times 4000 \times 100}{300} = 1.73 \text{ Watts}$$

$$P_{rr.diode} = \frac{(E_{OFF})\times f_{sw} \times V_{dc}}{V_{nom}} \quad (5.3)$$

$$P_{rr.diode} = \frac{(170e-6)\times 4000 \times 100}{300} = 0.23 \text{ Watts}$$

The forward voltage drop for diode and the collector-emitter saturation voltage of the IGBTs are 1.75 V and 1.5 V respectively. The conduction times for these devices varies due to implemented active and reactive power control, therefore conduction losses are calculated as a total, considering the worst-case scenario.

$$P_{conduction.diode+IGBT} = V_f \times I_{rms} \quad (5.4)$$

$$P_{conduction.diode+IGBT} = 1.75 \times 17.4 = 30.45 \text{ Watts/each inverter leg}$$

By using equation (5.1), it is possible to calculate total losses in a module.

$$P_{loss} = 4 \times (1.73 + 0.23 + (30.45/2)) = 68.75 \text{ Watts/module}$$

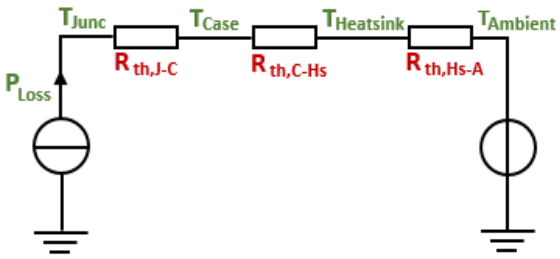

Figure 5.15: Thermal model for intelligent power module

Figure 5.15 shows thermal model of power module. Equation (5.5) can be used to calculate the thermal resistance of the required heatsink for safe operation of power module

$$T_{junc} = P_{loss} \times (R_{th,J-C} + R_{th,C-Hs} + R_{th,Hs-A}) + T_A \quad (5.5)$$

Where T_{junc} is the junction temperature of power module, P_{loss} is the power loss of the FNB34060T, $R_{th,J-C}$ is the thermal resistance from junction to power module case, $R_{th,C-Hs}$ is the thermal resistance from the case to heatsink (or thermal resistance of thermal paste), $R_{th,Hs-A}$ is the thermal resistance from the heatsink to its ambient and T_A is the ambient temperature.

$R_{th,C-Hs}$ is assumed to be 0.4 °C/W considering the area and thickness of the thermal paste used. $R_{th,J-C}$ is given as 0.2975 °C/W in the datasheet and T_A is assumed as 25 °C. As a result, the minimum thermal resistance of the heatsink, $R_{th,Hs-A}$ < 1.12 °C/W for keeping junction temperature at less than 150 °C. A heatsink with a thermal resistance of 0.83 °C/W is therefore used. Using this heatsink should keep the junction temperature < 130 °C, without considering forced air cooling by case fans. Figure 5.16 shows an intelligent power module PCB with heatsink.

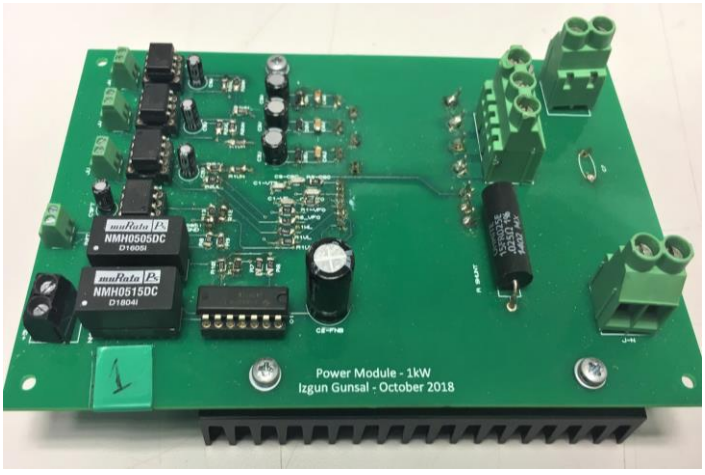

Figure 5.16: Heatsink and intelligent power module board

In order to test the power modules, an initial experiment is made by applying 100 V DC link voltage as the input. A 10 Ω resistive load is connected between two phases, A and B. Figure 5.17 shows output voltage waveform V_{AB} and two leg voltages for each phase V_A and V_B.

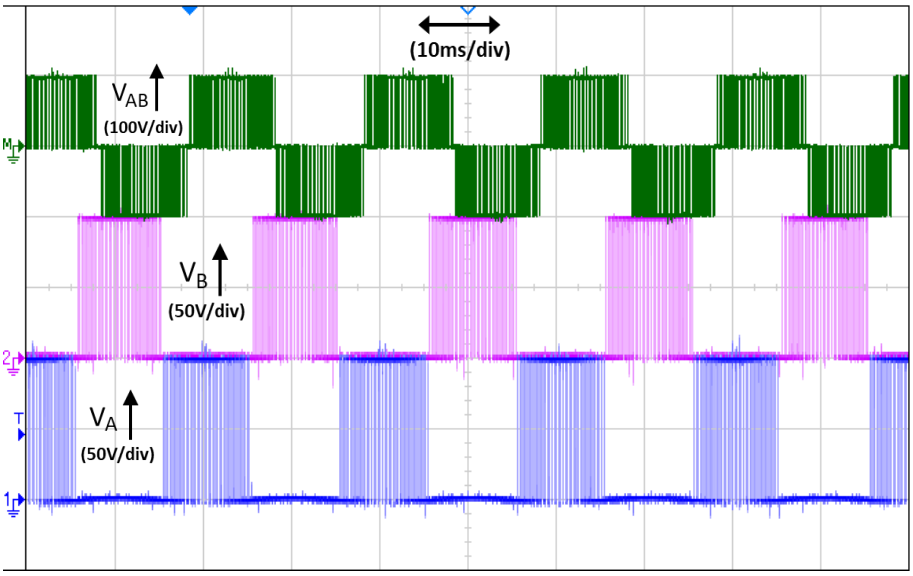

Figure 5.17: Output and leg voltages of an individual H-bridge module

It can be seen from Figure 5.17 that the power module prototype operates as expected, being able to produce a 3-level voltage output, $+V_{DC}$, 0 and $-V_{DC}$ (100V, 0V and 100V). A filter is needed to remove the high frequency components, such that a sinusoid output can be achieved. In order to check the quality of the output waveforms, a low-pass LC filter with a corner frequency tuned to half of the switching frequency is added at the output.

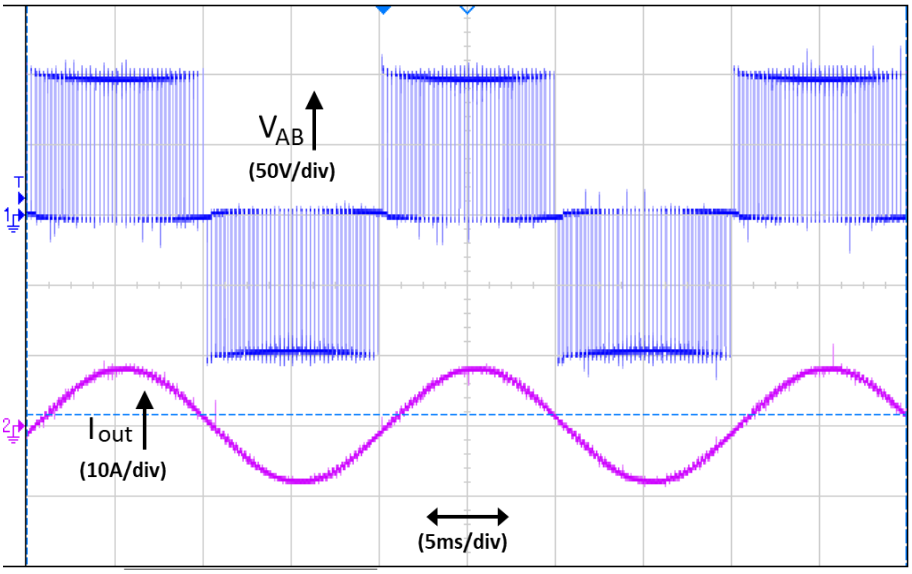

Figure 5.18: Unfiltered output voltage and filtered load current waveform

Figure 5.18 shows that the filtered output current is a good approximation to a sinusoid, when applied to a resistive load.

5.4.2 Cascaded H-bridge Evaluation

To test 9-level CHB converter, 4 isolated DC sources are required. Therefore, 4x RS-Pro toroidal step-down transformers are utilised to form the isolated supplies. These transformers have single primary (230 V_{RMS}) and dual open style secondary (2x 40 V_{RMS}) windings rated at 1 kVA each. The primary side of the transformers is connected to the three-phase utility supply, and the open style secondary windings are connected in series to achieve an 80 V_{RMS}. AC voltage, which is then converted to DC by using GBPC40 bridge rectifiers form Taiwan Semiconductor. Considering the UK grid voltage and diode forward voltage drop of the bridge rectifiers, an isolated DC voltage of ~112 V is achieved at rated power.

Four identical power module boards were designed and connected in series to achieve a 9-level CHB converter, shown in Figure 5.2, and also discussed in previous chapters. The experimental results from the 9-level CHB converter are detailed in the following sections. Figure 5.19 shows unfiltered output voltage (V_{out}) waveform at no load conditions when LRPWM is applied.

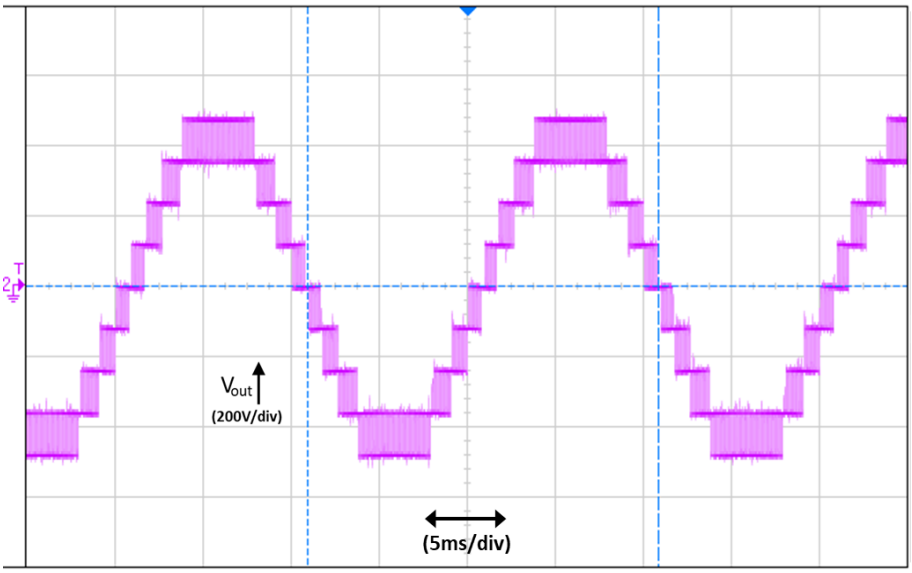

Figure 5.19: Unfiltered output voltage waveform of 9-level CHB at no load condition

It can be seen that the output waveform consists of 9 voltage levels which match with the simulation results. Although experimental results show some noise, this would be suppressed with the help of an output filter.

A symmetrical LCL output filter with a corner frequency of 1.34 kHz is adopted for filtering the switching frequency components from the output waveforms. Figure 5.20 shows the output voltage (pink), V_g, and current (blue), I_g, waveforms when a 50 Ω resistive load is connected across the phases A and B. LRPWM is also applied as the modulation scheme, and the modulation index is 0.77.

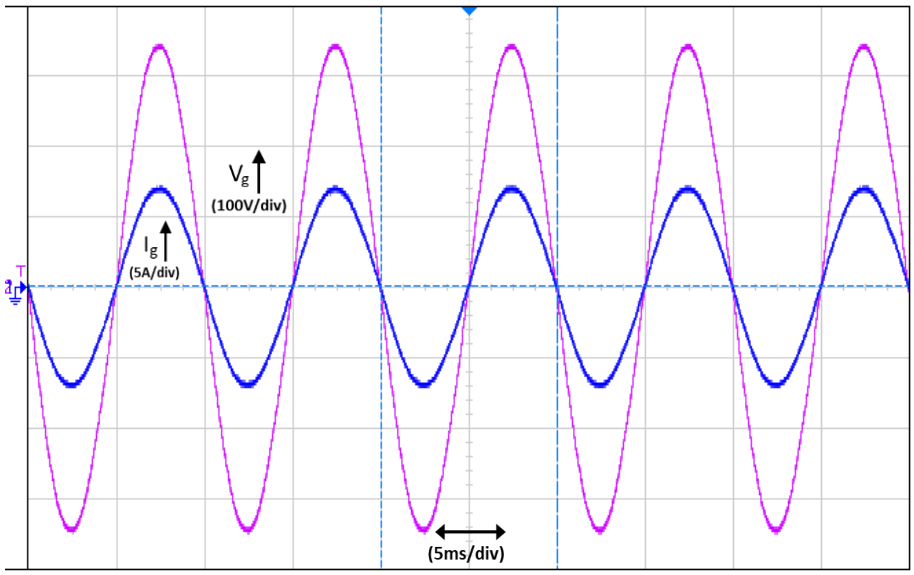

Figure 5.20: Output voltage and current waveform of 9-level CHB with LCL output filter

The voltage and current waveforms are sinusoidal are to be expected after low-pass filtering the output. The waveforms are in phase, corresponding to a purely resistive load condition.

In order to validate the bidirectional operation of 9-level CHB converter, the experimental hardware setup is modified, as the bridge rectifiers in the isolated supplies do not allow bidirectional operation. The output phases, A and B, become the system input connected to a single-phase supply. The DC (battery) side of the circuit now consists of resistors instead of an isolated transformer and bridge rectifier configuration. The new experimental setup is illustrated in Figure 2.21.

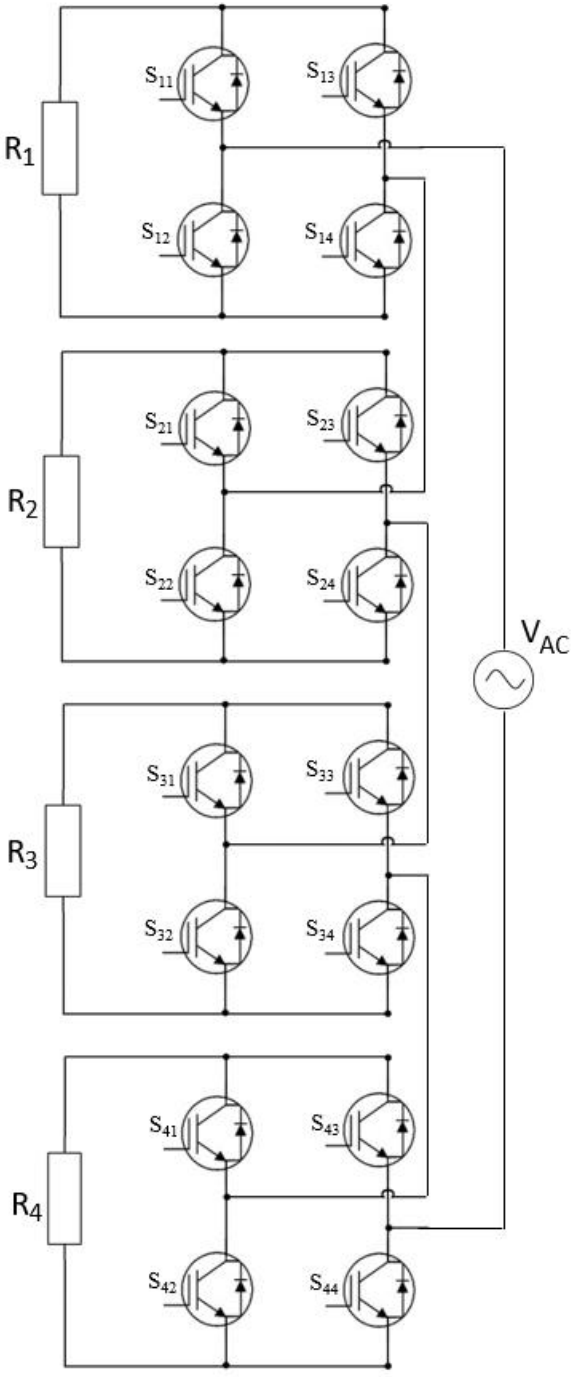

Figure 5.21: Experimental setup for AC to DC conversion of 9-level CHB converter

Resistors R_1, R_2, R_3, and R_4 in the different modules are all equal to 10 Ω. In order to achieve unity power factor, the current controller is set to extract -0.7 I_d, which corresponds to approximately -12.2 A_{rms} at the point of supply coupling. Figure 5.22 shows grid side voltage and current waveforms.

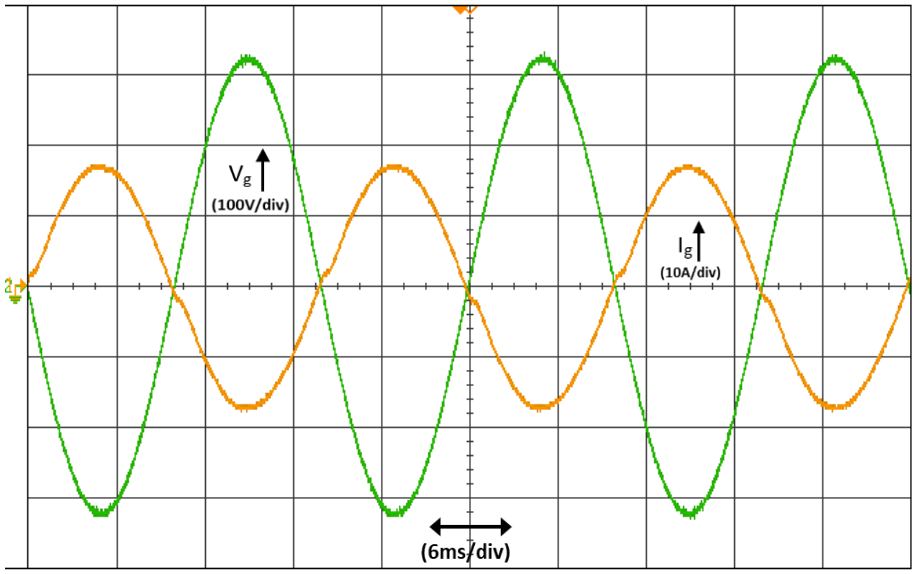

Figure 5.22: Grid side voltage and current waveform for AC to DC conversion

The grid voltage (Green), V_g, and grid current (Orange), I_g, waveforms are sinusoidal, and 180^o phase shifted from each other in Figure 5.22. This shows that the current is extracted from the grid supply and delivered to the resistors on the DC side of the circuit. Again, the current waveform is sinusoidal, out of phase with the voltage waveform, indicating a negative unity power factor at the grid side.

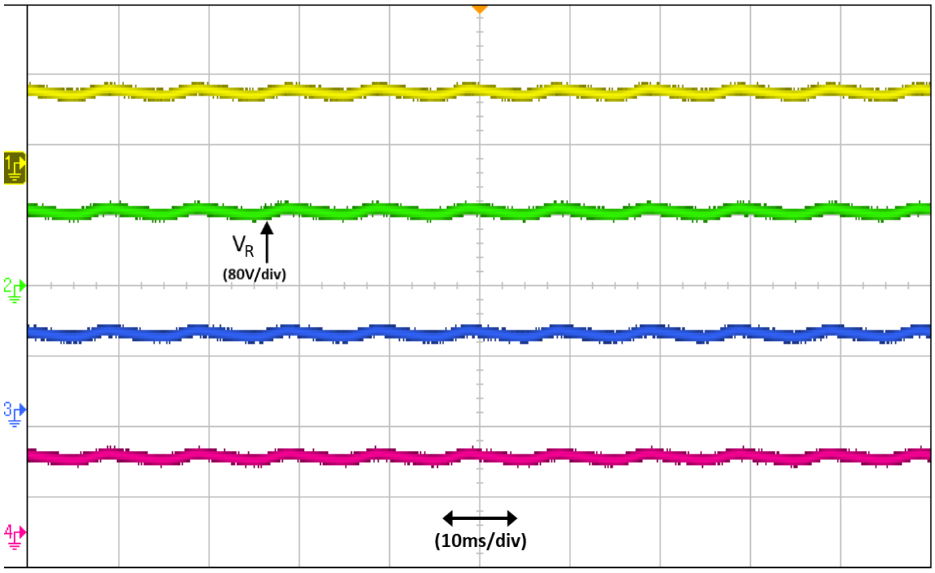

Figure 5.23: DC resistor voltages for AC to DC conversion

Figure 5.23 shows DC side resistor voltages. The DC waveform has double the line frequency ripple (100 Hz) which is an inherent feature for a single-phase AC-DC PWM converter [9].

5.5 Leakage Current Suppression Results

The previous sections covered the experimental assessment of the base system, which is constructed to validate the effectiveness of the LRPWM strategy in a PV connected scenario. For the sake of simplicity, capacitor boards are designed to be connected between a terminal of the DC link and ground within a power module in order to represent the stray (parasitic) capacitance between an actual PV panel and the grounded metallic frame. The stray capacitance is initially selected as 100 nF (thin film capacitors) in order to be consistent with simulations. The modulation index (m_a) remains at 0.8, and switching frequency is 4 kHz. Also, the same isolated DC source configuration is used as mentioned in 5.4.2. Additionally, a symmetrical LCL filter is added at the point of grid coupling, where the converter side inductances are 2x 2.34 mH, grid side inductances are 2x 1.17 mH, and the filter capacitance is 9 µF. This filter configuration has a corner frequency of 1.34 kHz.

Experimental results include comparisons between PSPWM, PDPWM and proposed LRPWM consisting of the unfiltered output voltage V_{out}, grid current I_g, grid voltage V_g, FFT analysis (THD) of grid current, leakage current of modules 1-4 I_{lm1}, I_{lm2}, I_{lm3}, and I_{lm4}, and the grid leakage current I_{lg}, which can be seen in Figures 5.24 - 5.32. Figure 5.24 shows unfiltered output voltage V_{out}, grid current I_g, and grid voltage V_g for the application of PSPWM.

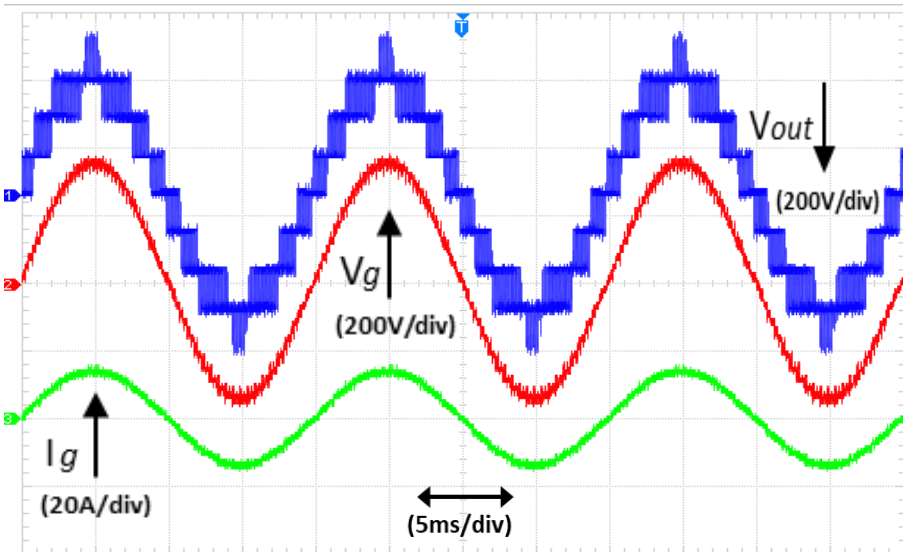

Figure 5.24: Unfiltered output voltage, grid voltage and the grid current with PSPWM

Due to parasitic capacitance at terminals of the isolated DC sources, the grid current I_g and grid voltage V_g have additional harmonics. The unfiltered output voltage V_{out}, has nine voltage levels, which is as expected.

Figure 5.25 and 5.26 show the FFT analysis (THD) of the grid current $I_{g,}$ and leakage current of modules 1-4 I_{lm1}, I_{lm2}, I_{lm3}, and I_{lm4}, and also the grid leakage current I_{lg} when PSPWM is used in the modulator.

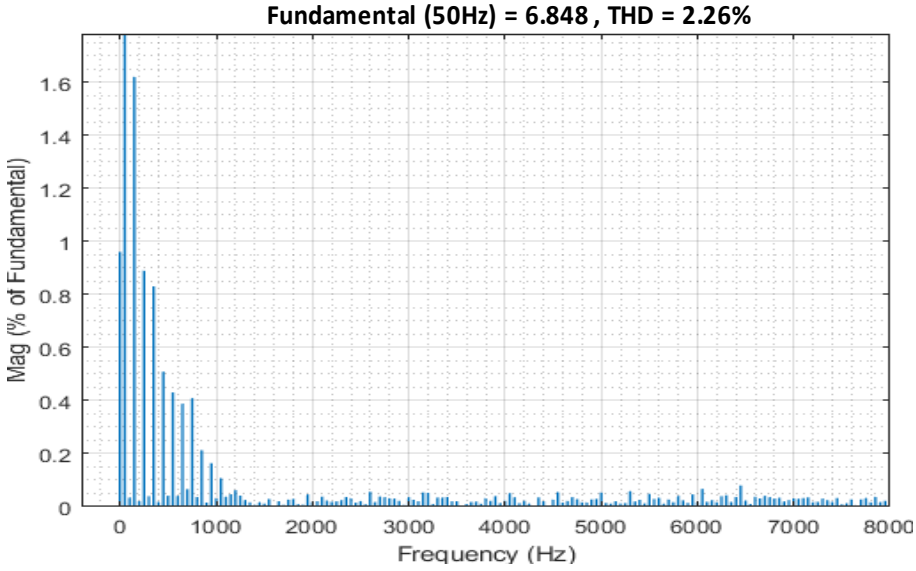

Figure 5.25: FFT of grid current with PSPWM

The THD of PSPWM is 2.26%, where the harmonic spectra contains low frequency harmonics, generally limited below 1 kHz.

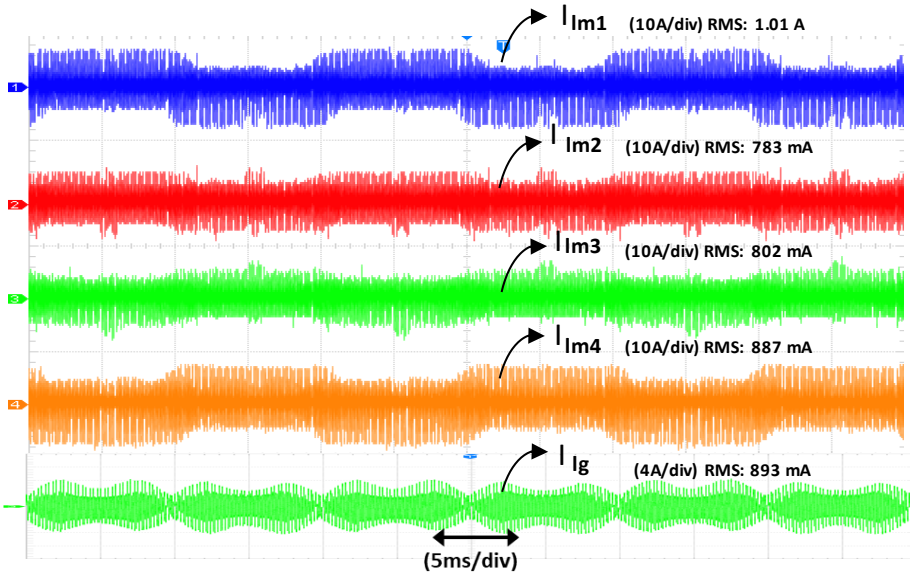

Figure 5.26: Leakage current of modules 1-4 and the grid leakage current with PSPWM

Figure 5.26 shows the leakage current of modules 1-4 and total grid leakage current. The envelope of the module leakage current and the respective RMS values varies considerably between each module. The grid leakage current is 893 mA.

Figure 5.27 shows unfiltered output voltage V_{out}, grid current I_g, grid voltage V_g for PDPWM.

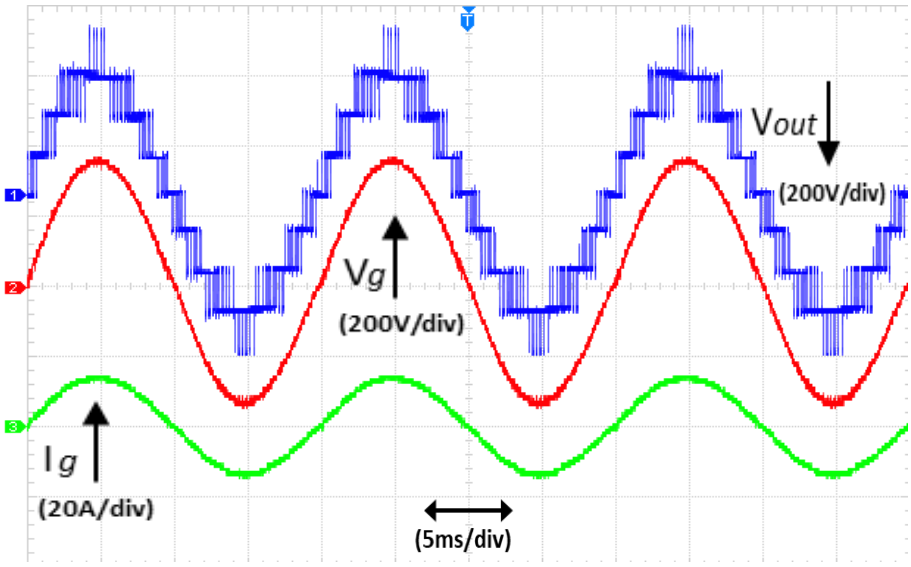

Figure 5.27: Unfiltered output voltage, grid voltage and the grid current with PDPWM

The waveforms show similar characteristics when compared with the PSPWM technique. Grid current I_g the grid voltage V_g are sinusoidal as expected. Figure 5.28 shows the THD of the grid current when PDPWM is used as the modulator.

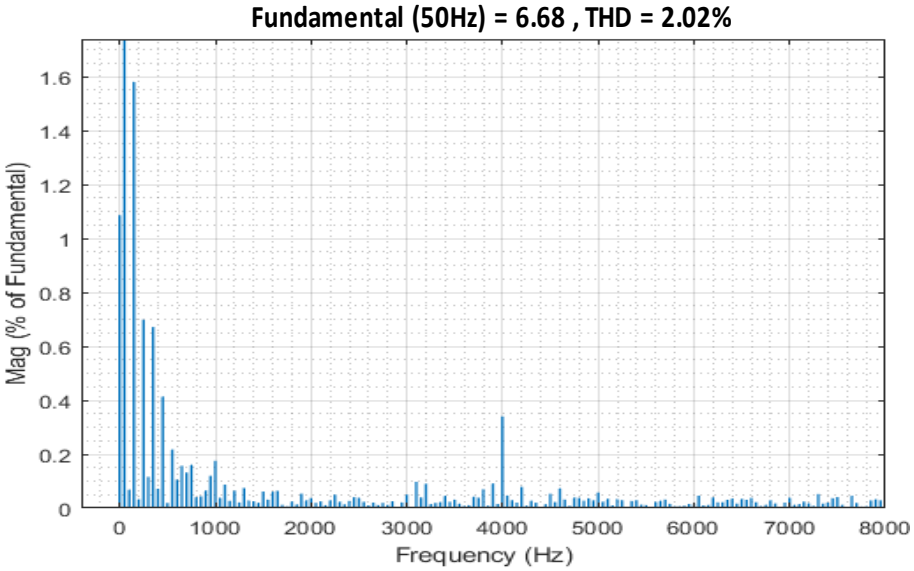

Figure 5.28: FFT of grid current with PDPWM

The THD of the PDPWM methodology is 2.02%, where the harmonic spectra not only contains low frequency harmonics, but also switching frequency harmonic that forms 0.38% of the fundamental component.

Figure 5.29 shows leakage current of modules 1-4 and the grid leakage current when PDPWM is used in the modulator.

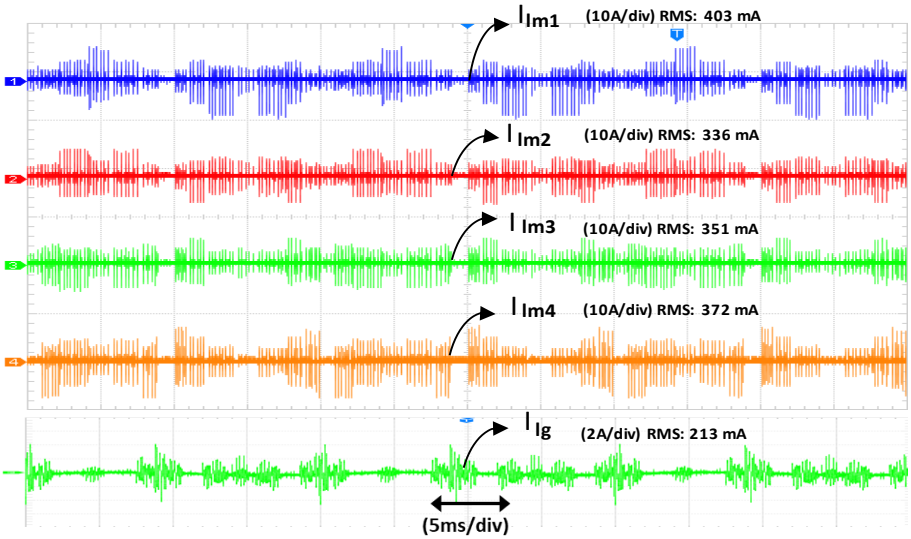

Figure 5.29: Leakage current of modules 1-4 and the grid leakage current with PDPWM

Applying PDPWM, the modules have more consistent RMS values but, again, the waveform envelopes vary as each module operates at different points of the reference sinusoid. All waveforms are consistent with the simulation study shown in chapter 3. The grid leakage current I_{lg} is 213 mA in this case, which is approximately 4 times lower than when PSPWM is applied.

Figure 5.30 shows unfiltered output voltage V_{out}, grid current I_g, grid voltage V_g for the proposed LRPWM methodology.

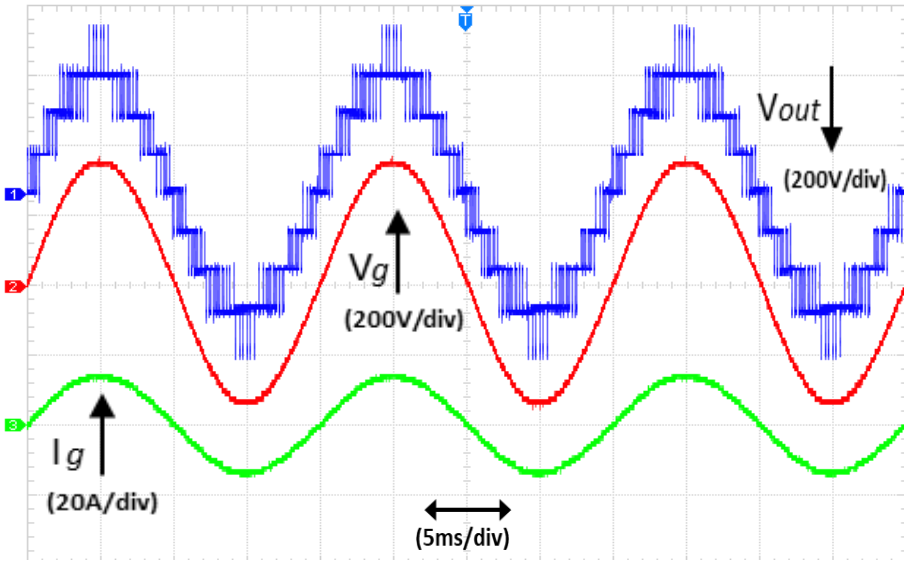

Figure 5.30: Unfiltered output voltage, grid voltage and the grid current with LRPWM

The waveforms show similar characteristics when compared with the PSPWM and PDPWM techniques. Grid current I_g and grid voltage V_g are sinusoidal, and unfiltered output voltage V_{out} has nine voltage levels. Figure 5.31 shows the harmonic analysis (THD) of the grid current when the proposed LRPWM is used in the modulator.

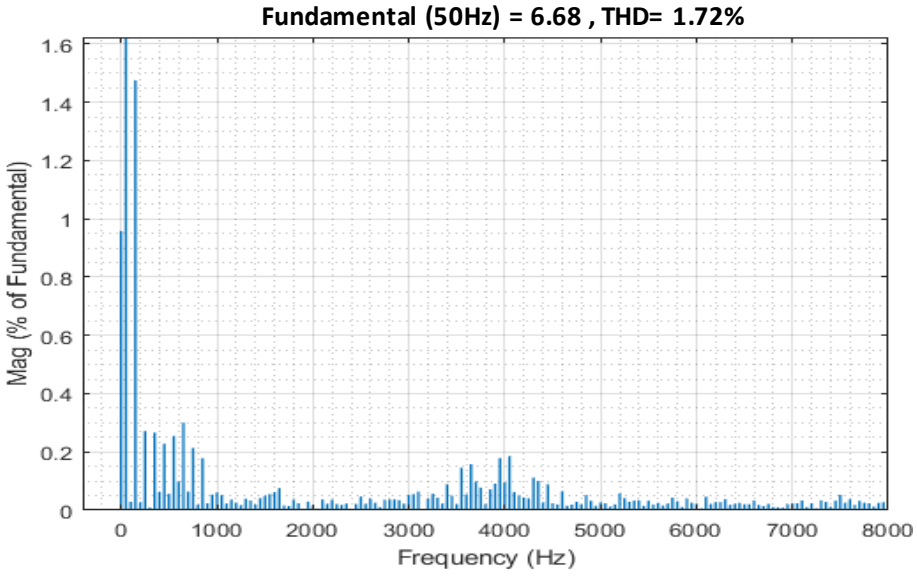

Figure 5.31: FFT of grid current with LRPWM

LRPWM has the lowest THD out of all tested modulation schemes. The harmonic spectrum has low frequency and switching frequency sideband harmonics, where the THD is 1.72%. It should be noted that all modulation methods create a grid current THD that conform to the IEEE 1547 standard. Figure 5.32 shows leakage current of modules 1-4, and the total grid leakage current of the proposed LRPWM.

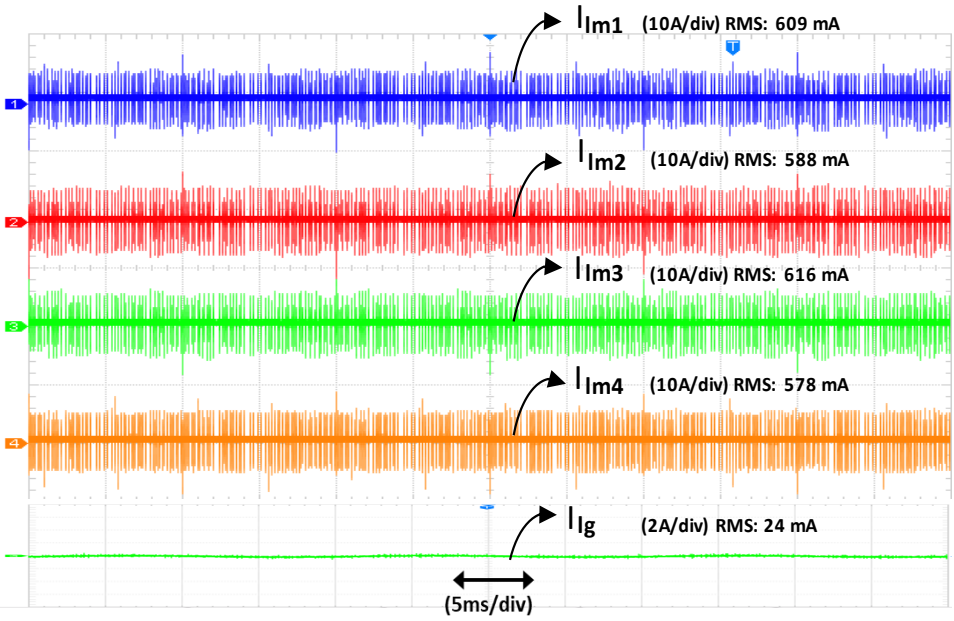

Figure 5.32: Leakage current of modules 1-4 and the grid leakage current with LRPWM

LRPWM provides very similar waveform envelopes, where the RMS module currents varies between 578 mA and 616 mA. Although the RMS module currents are higher than with PDPWM, their combination has a nulling effect and grid leakage current is only 24 mA.

From the above measurements, the measured values for grid leakage current in PSPWM, PDPWM and LRPWM are 893 mA, 213 mA and 24 mA respectively. It is verified that the proposed LRPWM method can reduce the leakage current flowing through the parasitic capacitances to the ground. As mentioned in chapter 3, German leakage standard VDE-0126-1-1 allows 30 mA maximum leakage current flow to the ground. In this case, LRPWM is the only modulation method that conforms to the VDE-0126-1-1 standard. It should be noted that LRPWM is a modulation scheme therefore, one can address the leakage current problem without adding to cost, weight, volume and size of the resultant converter.

The individual module leakage current values are higher than the total grid leakage current for PDPWM and LRPWM. In PSPWM, only module 1 has a higher module leakage current when compared with the total grid leakage current. Considering that all modulation schemes are tested at the same operating point, such as modulation index (m_a), switching frequency and parasitic capacitance value, LRPWM performs approximately 37 and 9 times better than PSPWM and PDPWM respectively, when it comes to grid leakage current. However, this performance gain may change when the operating point of converter changes.

5.5.1 Sensitivity Analysis of Leakage Current

In this section, the operating point of the converter is modified in order to understand the effect of switching frequency, modulation index and parasitic capacitance on the total grid leakage current. In chapter 2, PSPWM and PDPWM algorithms are discussed. Examining the nature of these carrier waveforms, variations in modulation index should affect PSPWM and PDPWM differently. In order to verify this, the parasitic capacitances are initially kept constant. The results are limited to the modulation indices > 0.75, because if modulation index falls below this value, one module becomes idle and does not contribute to power sharing in PDPWM. Experimental results for RMS grid leakage current with respect to switching frequency and modulation index (m_a) are illustrated in Figures 5.33 and 5.34 for PSPWM and PDPWM respectively. The stray capacitance is again 100 nF, as with previous sections.

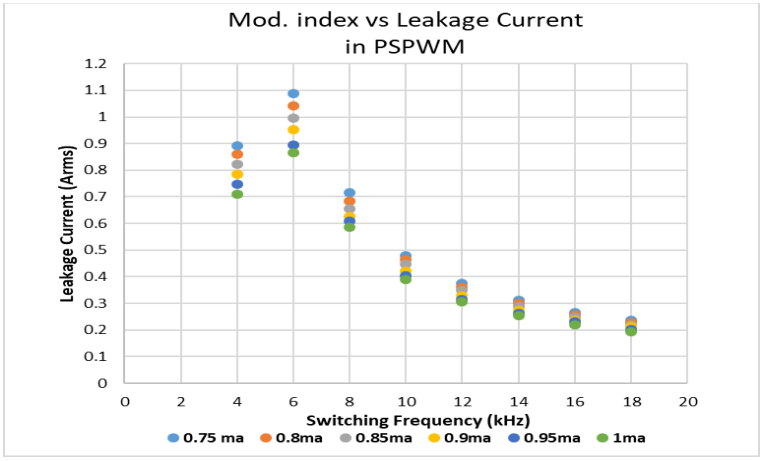

Figure 5.33: Grid leakage current with respect to different modulation indexes and switching frequencies in PSPWM with 100 nF stray capacitance

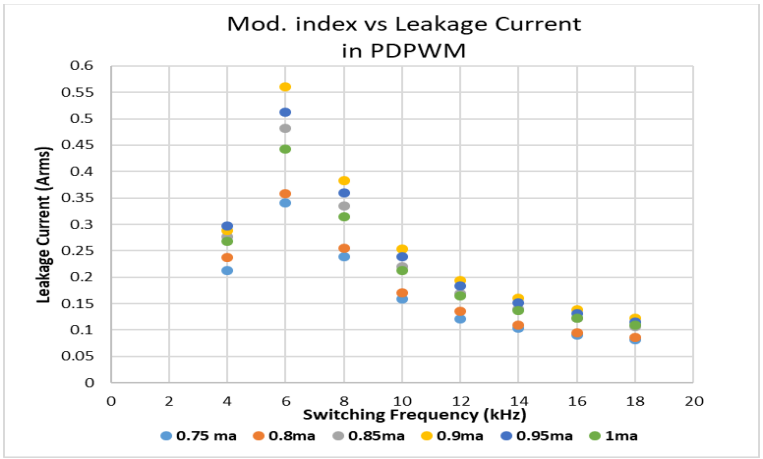

Figure 5.34: Grid leakage current with respect to different modulation indexes and switching frequencies in PDPWM with 100 nF stray capacitance

In Figures 5.33 and 5.34, it can be seen that both PSPWM and PDPWM tend to have higher grid leakage current with reduced switching frequency. It should be noted that the parasitic capacitances and inductances create a resonant circuit and this should be borne in mind when selecting the switching frequency. In Figure 5.33, it is obvious that PSPWM performs better when modulation index is closer to unity. In Figure 5.34, PDPWM has highest grid leakage values when operated at 0.9 modulation index. 0.75-0.8 modulation index range provides lower grid leakage current when using PDPWM, as the time at the maximum and minimum voltage levels ($+4V_{dc}$ and $-4V_{dc}$) during a fundamental switching cycle become shorter. Figure 5.35 and 5.36 shows experimental results for RMS grid leakage current with respect to switching frequency, and modulation index, when the stray capacitance values are reduced to 56 nF.

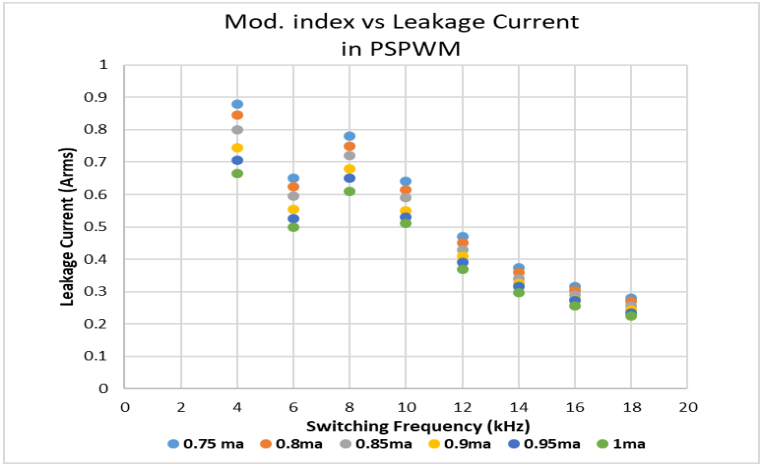

Figure 5.35: Grid leakage current with respect to different modulation indexes and switching frequencies in PSPWM with 56 nF stray capacitance

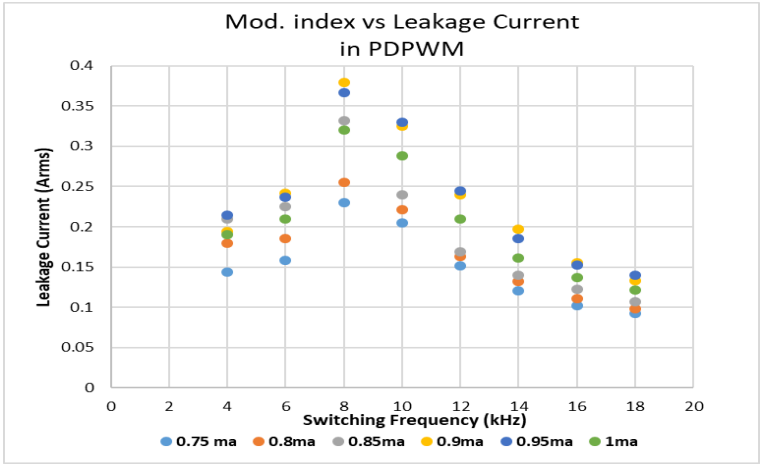

Figure 5.36: Grid leakage current with respect to different modulation indexes and switching frequencies in PDPWM with 56 nF stray capacitance

In Figures 5.33 and 5.34, it can be seen that both PSPWM and PDPWM tend to have higher grid leakage current with reduced switching frequency. It can also be seen that the resonant peak of the resonant circuit has shifted from 6 kHz to 8 kHz when the parasitic capacitance values are reduced to 56 nF. In Figure 5.35, PSPWM still performs better with unity modulation index, but has slightly higher grid leakage current with switching frequencies higher than 8 kHz. In Figure 5.36, PDPWM has highest grid leakage current when operated at 0.9-0.95 modulation index. Moreover, PDPWM performs better up to 10 kHz switching frequency when the stray capacitance is reduced to 56 nF.

To generalise, both PSPWM and PDPWM performs better with higher switching frequencies. The best modulation index for PSPWM is unity whereas this value for PDPWM is at 0.75-0.8 region. Reducing the value of parasitic capacitance increased the grid leakage current at high switching frequencies in both PSPWM and PDPWM respectively. Furthermore, LRPWM is not affected by switching frequency and/or modulation index variations for the tests considered, making it effective in suppressing grid leakage current over different operating points.

The experimental results are consistent with the simulation study and theory presented in chapter 3.

5.6 Chapter Summary

This chapter focuses on the experimental hardware platform for testing PSPWM, PDPWM and LRPWM for grid leakage current. The hardware is controlled with the master controller cRIO-9063 from National Instruments and the slave controller LAUNCHXL-F28379D from Texas Instruments. Firstly, gate signal generation and FPGA implementation are discussed. Then, isolated sensors and signal conditioning circuits are detailed. Following sections discussed power module evaluation and its thermal management.

Finally, a nine level CHB converter is evaluated and sensitivity analysis is performed on the grid leakage current when different modulators are used. It is shown that LRPWM performs better when parasitic capacitances are present at the isolated DC source terminals.

Next chapter will detail output filter, closed loop control and safe operation of a grid-tie CHB converter.

5.7 References

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Chapter 6
Grid Connection and Power Quality

6.1 Introduction

Previous chapters described the design and evaluation of a 9-level CHB converter for solar PV applications, featuring grid leakage current suppression. In this chapter, grid connection and the power quality of the converter will be discussed.

In order to couple the converter to the utility supply, measures such as grid synchronisation and closed loop control have to be deployed within the hardware. Moreover, the output voltage and current waveform harmonics need to be within an acceptable range, conforming to regulations and standards. Power converters driving a load or coupled with the utility, may introduce undesirable disturbances to the system they feed. These disturbances are generally a product of the PWM modulator and the closed loop control strategy. Additionally, the impedance of the appliances and loads driven also contribute to these disturbances. Particularly, inductive loads are notorious, due to the presence of active converter diodes during freewheeling period.

A conventional approach to measuring harmonics in a converter is based on calculating the total harmonic distortion (THD) of the waveform in question. THD measures conformity of the output waveform with respect to the ideal. In a DC-AC converter, the output voltage and current waveforms at the point of utility coupling are desired to be as close as possible to an ideal sinusoid. In [1], real-time calculation of switching angles for a MLC modulated with nearest level control is demonstrated, aiming to reducing the THD. Also in [2], it is discussed that the THD of an MLC is the combination of effects due to the switching frequency, modulation strategy, modulation index and the number of available output voltage levels.

The output filter plays a vital role when it comes to suppressing harmonics, which are caused by the switching devices. Commonly, passive filters are used in this application, minimising the THD. In [3], an LCL filter design process is detailed for a grid-tie high power wind turbine system. Alternatively, MLCs are often used as shunt active power filters for correcting disturbances caused by non-linear loads. An example of this is given in [4], where a 3-level NPC deployed in a three-phase, four wire system, is demonstrated.

An output filter is designed considering the limitations discussed in chapter 3 for minimising the THD in the base system. Regulations and standards for grid connected converters, closed loop control algorithms and converter safety and protection will be discussed later in this chapter.

6.2 Regulations and Standards

Power quality is critical in specific applications such as avionics and hospitals, where insufficient power quality may affect/damage the operation of other systems on the supply. In general, power quality may be affected by coupled loads and/or systems in a local network, and may manifest as being related to the voltage, frequency and harmonics of the supply. Converters are generally designed to produce little harmonic disturbances, however non-linear loads tend to inject unwanted harmonics, causing problems to other systems coupled to the same point in a local network. Considering this, converters should conform to specific regulations in order not to further degrade the local network.

As mentioned in chapter 2, use of high number of voltage levels in MLCs allows a reduction in output voltage harmonics, consequently leading to the need for smaller output filters. The total harmonic distortion (THD) is a parameter that is regulated by standards throughout the world [5], as is defined in equation (6.1).

$$THD = \frac{\sqrt{{I_{RMS}}^2 - {I_{fund}}^2}}{I_{fund}} \times 100 \tag{6.1}$$

where I_{fund} is the amplitude of fundamental component, I_{RMS} is the RMS output current. THD is therefore calculated as a percentage, and low values represent a closed approximation to the ideal waveform.

In order to regulate voltage, frequency and harmonics, standards and regulations are enforced for appliance and converter manufacturers to ensure utility supply quality. In the last decades, institutions such as the IEC (International Electrotechnical Commission), the IEEE (Institute of Electrical and Electronic Engineers) and the BSI (British Standards Institution) policed these regulations. An example of the BSI regulation can be seen as BS EN 61000, which regulates the EMC (electromagnetic compatibility) of an equipment in the electromagnetic medium [6]. BS EN 61000 states that THD should be < 5% at full power and < 8% within the full operating range. Other examples include IEC 61727 [7], which is dedicated to PV systems and their characteristics of the utility interface,

IEEE 1547 [5], which is a standard for interconnection and interoperability of distributed energy resources and power systems interfaces. Lastly, IEEE 519 [8], which is recommended practice for harmonic control in electrical power systems. Some of the key concerns considered as a part of these regulations are the range of injected DC currents, THD, individual harmonic current levels, nominal voltage and frequency range and detection of islanding operation. The summary of IEC 61727, IEEE 1547 and IEEE 519 regulations are shown in Table 6.1.

Standard	**IEC 61727**	**IEEE 1547**	**IEEE 519**
System Rating	< 10 kVA	< 30 kVA	< 69 kV
THD	5%	5%	5%
Maximum Harmonic Current Distortion of Odd harmonics Even Harmonics	(3 to 9) < 4% (11 to 15) < 2% (17 to 21) < 1.5% (23 to 33) < 0.6% (2 to 8) ≤ 1% (10 to 14) ≤ 0.5% (17 to 21) ≤ 0.5% (23 to 33) ≤ 0.5%	IEEE 519 limits apply	(3 to 9) ≤ 4% (11 to 15) ≤ 2% (17 to 21) ≤ 1.5% (23 to 33) ≤ 0.6% (>35) ≤ 0.3% 25 % of the listed odd harmonics
Power Factor at half rated power	0.9	0.9	-
DC current injection	< 1% of rated output current	< 0.5% of rated output current	-
Range of nominal voltage	85% - 110% (2s disconnection time)	45% - 120% (0.16s disconnection time)	-
Range of nominal frequency	50 ± 1 Hz (0.2s disconnection time)	60 ± 0.3 Hz (0.16s disconnection time)	-

Table 6.1: Summary of standards for grid-tied systems

It can be seen that different regulations have similar maximum harmonic current distortion for different system ratings (Table 6.1). The THD is generally limited to 5% for low power, whereas this level is lower for higher power interfaces. Moreover, ranges of nominal voltage and frequency and their relevant disconnection times are given. Considering the regulations and standards, a passive filter can be designed for the 9-level CHB converter, which is detailed in section 6.3.

6.3 Multilevel Converter Output Filter

In MLC, the high frequency content of the output waveform has to be filtered before coupling with a utility supply due to the previously mentioned standards and regulations. This output filter should ideally attenuate the unwanted harmonics without changing the fundamental frequency component. Typically, size and cost are the two main constraints when it comes to filter design. Filters tuned to lower frequencies tend to be more costly and larger in volume, as they generally require physically larger components to achieve the lower frequency operation. Filtering may be passive or active depending on devices and filter gain. Here, only passive filters are considered as active filters are not in scope for this work. In [9], 'L', 'LC' and 'LCL' filters are compared, with the study concluding that the 'LCL' filter topology has a better performance than others when similar values of inductance, capacitance are used. In [10], a custom 'LCL' filter is designed for a three-phase 2-level voltage source converter. Different passive filters are therefore studied in the following sections.

7.3.1 L Filter

The 'L' filter is simple to implement as it only requires a single inductor. Being simple to design makes it popular, however this filter only provides low attenuation (20dB/dec) and generally requires a high inductance value to achieve better attenuation, when compared with other filter types. The 'L' filter causes a voltage drop across the inductance, resulting in poor system dynamic response [11]. The implementation of the 'L' filter is illustrated in Figure 6.1.

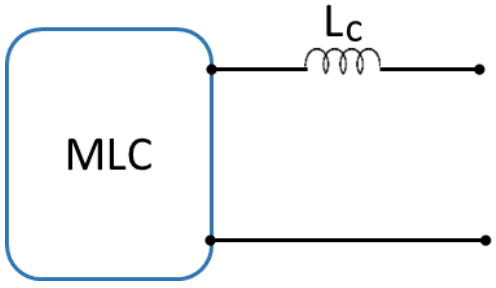

Figure 6.1: L Filter circuit diagram

The 'L' filter's corner frequency can be defined in equation (6.2).

$$f_c = \frac{1}{2\pi L} \tag{6.2}$$

7.3.2 LC Filter

The 'LC' filter is a second order low-pass filter, consisting of an inductor and a shunt capacitor. The value of the shunt capacitor plays a vital role, as increasing its value improves filtering capability at lower frequencies, however a high capacitance may cause higher inrush currents at start-up. The 'LC' filter provides a 40dB/dec attenuation, which is better than 'L' filter. The resonant (corner) frequency of the 'LC' filter is susceptible to a change in a grid-tie scenario, due to self-inductance of utility supply affecting the total inductance value in the filter circuit. The converter side inductances (L_c) may be configured a/symmetrically and a damping network may be added depending on the application. Figure 6.2 shows different 'LC' filter implementations.

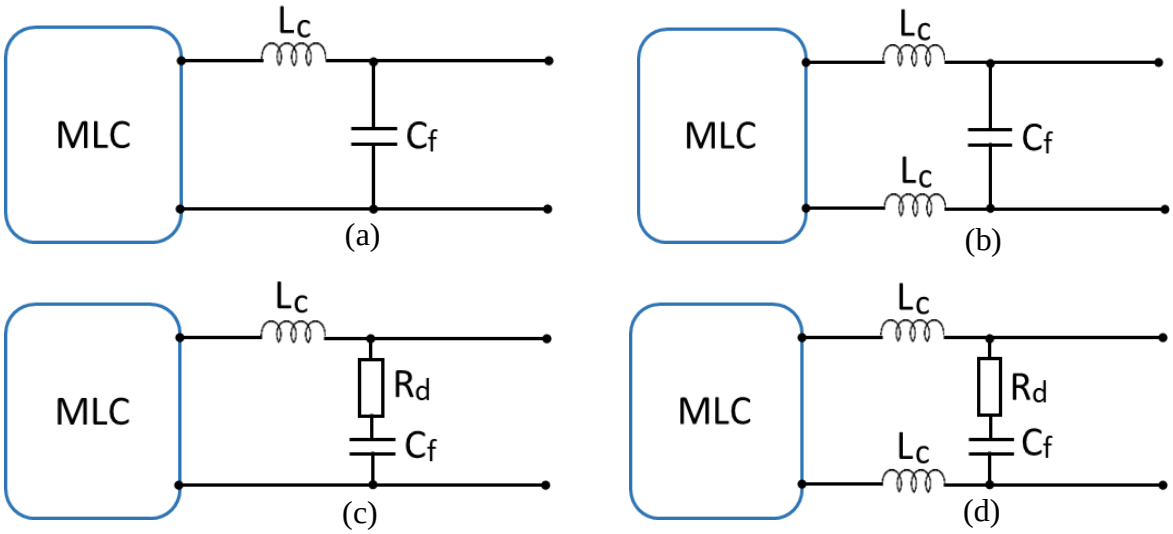

Figure 6.2: LC Filter combinations: (a) Asymmetrical LC, (b) Symmetrical LC, (c) Asymmetrical LC with R damping, (d) Symmetrical LC with R damping

The resonant frequency of the 'LC' filter is as follows:

$$f_c = \frac{1}{2\pi\sqrt{LC}} \tag{6.3}$$

The transfer function of a generic 'LC' filter is:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{(2\pi f_c)^2}{s^2 + 2\zeta(2\pi f_c)s + (2\pi f_c)^2} \tag{6.4}$$

where quality factor $Q = \frac{1}{2\zeta}$ and ζ is the damping ratio.

If L_c, C_f and R_d are 2x 2.34 mH, 9 µF, and 2 Ω respectively, bode plots for symmetrical and asymmetrical 'LC' filter, with and without damping can be seen in Figure 6.3.

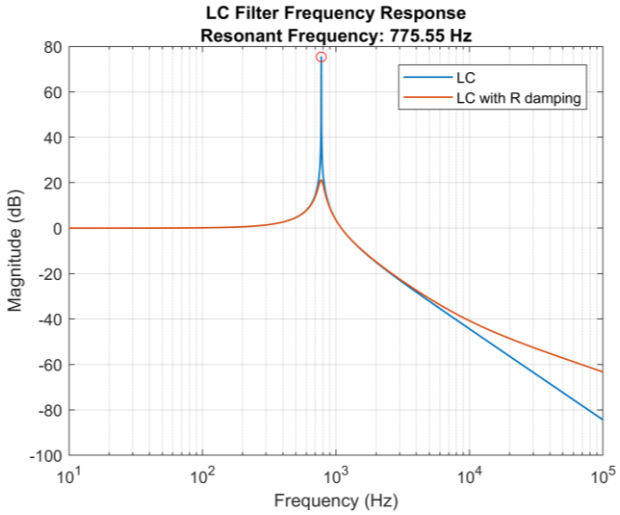

Figure 6.3: Bode plot for LC filter and LC filter with resistive damping

It can be seen that this 'LC' filter provides no attenuation below resonant frequency region. Resistive damping reduces the resonant peak from 77 dB to 20 dB. Conversely, high frequencies are more poorly attenuated with resistive damping. If these filters are connected to the base system (9-level CHB), the harmonic spectrum for the converter is given in Figure 6.4.

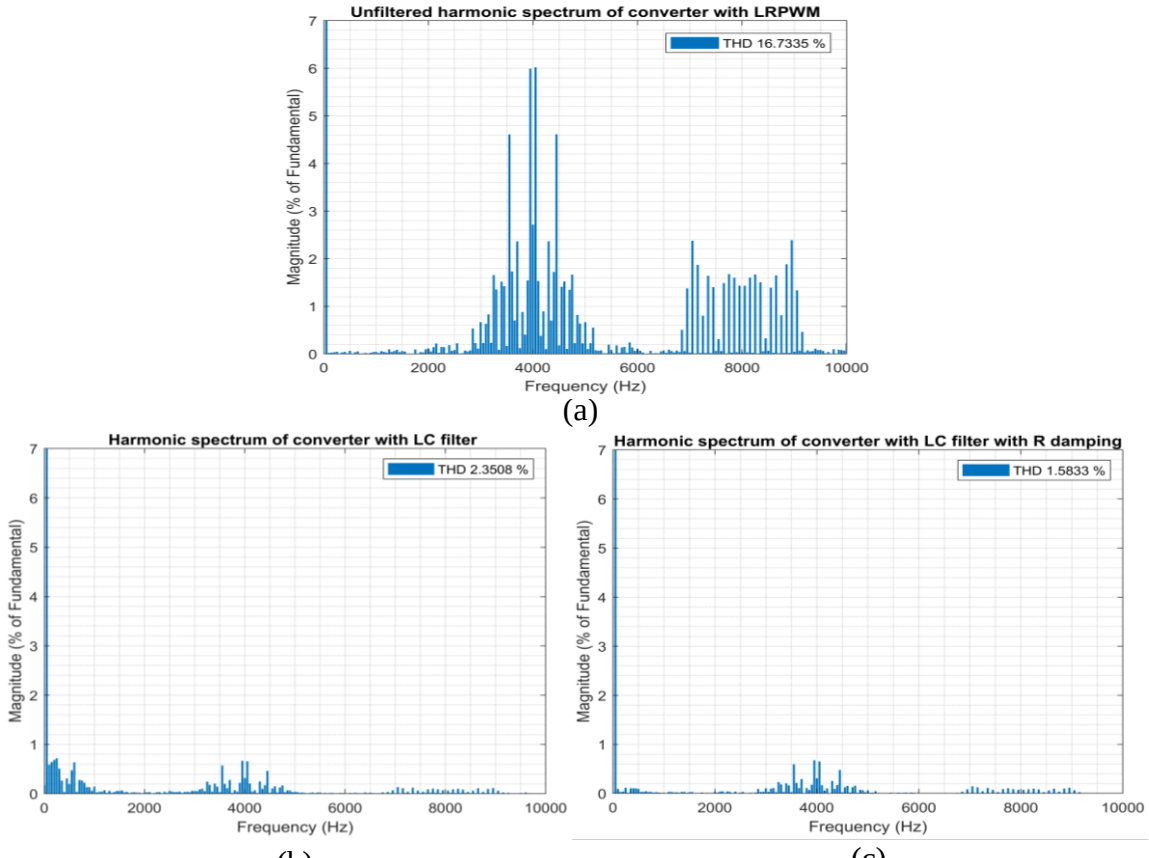

Figure 6.4: Harmonic spectrum of grid current without a filter and with different LC filters

The switching frequency components and their multiples in the 'LC' filter are greatly reduced when a filter is added at the point of grid coupling. This is reflected into the THD value, reducing it from 16.73% to 2.35% (Figure 6.4a and 6.4b) when an 'LC' filter is connected. Adding a series damping resistor greatly reduced the harmonics in the sub-switching frequency region. The use of resistive damping reduced the THD in output grid current from 2.35% to 1.58% (Figure 6.4b and 6.4c).

7.3.3 LCL Filter

The 'LCL' filter provides a 60dB/dec attenuation and so is superior, when compared with the 'L' and 'LC' filters. This filter consists of 2 inductors, L_c and L_g, which are the converter and grid side inductances respectively. As the 'LCL' filter has a grid side inductor, it is more resistant to changes in utility grid conditions, providing more predictable performance. Due to its better attenuation capabilities, the 'LCL' filter provides better performance around the corner frequency. Figure 6.5 shows different 'LCL' filter topologies.

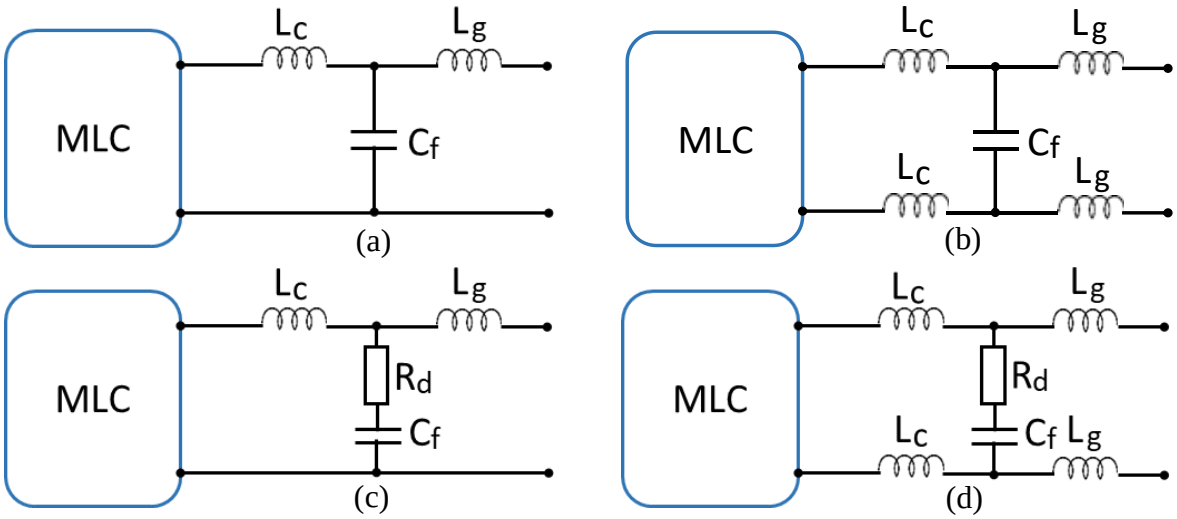

Figure 6.5: LCL Filter combinations: (a) Asymmetrical LCL, (b) Symmetrical LCL, (c) Asymmetrical LCL with R damping, (d) Symmetrical LCL with R damping

The resonant frequency of a 'LCL' filter is given by:

$$f_c = \frac{1}{2\pi}\sqrt{\frac{L_c+L_g}{L_cL_gC_f}} \tag{6.5}$$

The transfer function of a generic 'LCL' filter is:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{R_dC_f(s)+1}{L_cL_gC_fs^3+(L_c+L_g)R_dC_fs^2+(L_c+L_g)s} \tag{6.6}$$

In the literature, it is recommended to keep the total inductance value ≤ 10% of the base inductance and filter capacitance value ≤ 5% of base capacitance of the system in asymmetrical 'LCL' filters [10]. Moreover, the filter corner frequency should be tuned within a range of $10\, f_{fund} \leq f_c \leq 0.5\, f_{sw}$ in order to avoid resonant operation of the converter. System parameters for the prototype system are given in Table 6.2.

Parameter	Equation	Value
Fundamental Frequency	f_{fund}	50 Hz
Switching Frequency	f_{sw}	> 4 kHz
Base Power	P_b	4000 VA
Base Voltage	V_b	230 V_{RMS}
Base Current	$I_b = \frac{P_b}{V_b}$	17.39 A_{RMS}
Base Impedance	$Z_b = \frac{V_b}{I_b}$	13.225 Ω
Base Inductance	$L_b = \frac{Z_b}{\omega_{fund}}$	42.1 mH
Base Capacitance	$C_b = \frac{1}{Z_b \omega_{fund}}$	240.7 µF

Table 6.2: System Parameters for filter calculation

Similarly, if L_c, L_g, C_f and R_d are 2.34mH, 1.17mH, 9µF, and 2Ω respectively, bode plots for a symmetrical and asymmetrical 'LCL' filter, with and without resistive damping 'LCL' filter are shown in Figure 6.6.

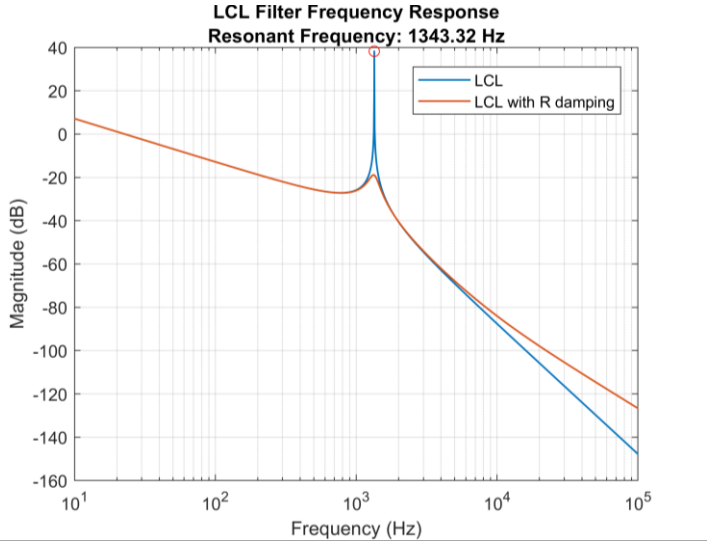

Figure 6.6: Bode plot for LCL filter and LCL filter with resistive damping

The resonant peak of the 'LCL' filter is 39 dB, reducing to -20 dB when a series damping resistor 'R' is added to the circuit. When a series damping resistor is added to 'LCL' filter, attenuation of signals over 5 kHz is reduced compared to without damping. It should be noted that due to equivalent series resistance (ESR) of the filter capacitor, the resonant peak should be lower in reality. The performance of these different 'LCL' filters when connected to the output of 9-level CHB converter can be seen in Figure 6.7.

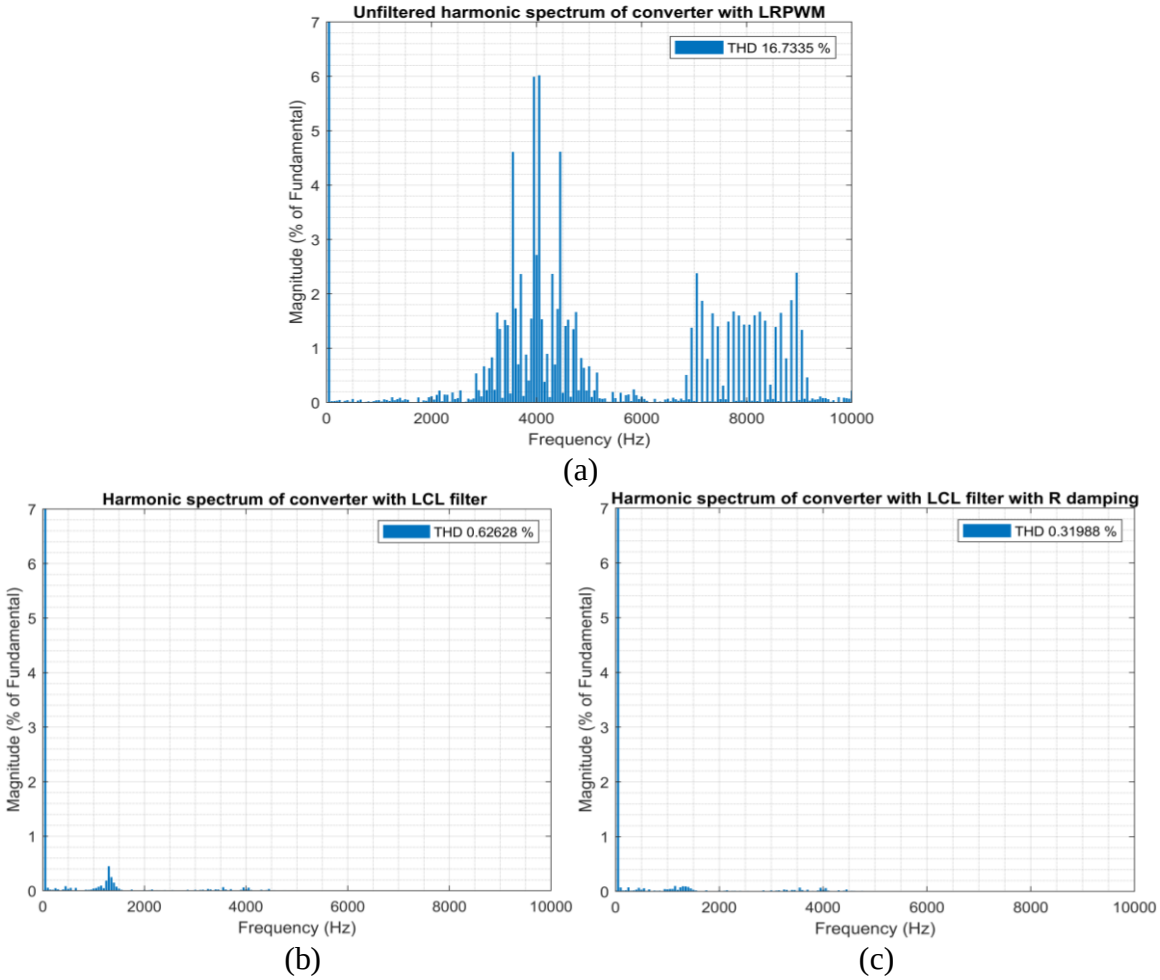

Figure 6.7: Harmonic Spectrum of grid current without a filter and with different LCL filters

The resonant frequency of the selected LCL filter is 1.34 kHz. Considering this, the switching frequency region harmonics are better attenuated. This also reflects into the THD value of the converter, reducing THD from 16.73% to 0.63% (Figure 6.7a and 6.7b). Again, the addition of series damping resistor further reduced the corner frequency region harmonics, therefore the converter THD changed from 0.63% to 0.32% (Figure 6.7b and 6.7c). Symmetrical configuration of filter inductances does not affect the attenuation provided by the filter. Furthermore, information in chapter 3 suggest the use of symmetrical filters, therefore a symmetrical 'LCL' filter is used in the base system.

6.4 Current Control of Multilevel Converters

Closed loop current control performance in a grid-tie converter is vital as this controller may affect the output current harmonic spectrum along with the overall dynamic response of the system [12]. As discussed previously, these aspects are regulated by standards and have to stay within certain limits. The role of the closed loop current controller is therefore to adjust the current flow through the 'LCL' filter, and hence the output, according to a given reference. There are 2 main approaches to current control that can be classified as: 1) linear current control and 2) non-linear current control. There are many examples in the literature for non-linear control structures, such as the hysteresis band controller, the predictive controller and the passivity based controller [13-15], however these are out of the scope of this thesis, therefore omitted from discussion. Conversely, linear current controllers such as the proportional-resonant (PR) and proportional-integral (PI) are discussed in following sections.

7.3.1 Neutral Frame (*abc* frame)

Neutral frame control is one of the first methods used for controlling the current at the point of common coupling in voltage source converters. In a three-phase system, the control of each phase current requires an individual controller per phase. In the neutral frame, the reference waveform is sinusoidal, therefore the controller has to track a varying amplitude, and be able to adapt to frequency changes accordingly. In [16], it is reported that *abc* frame current controllers tend to exhibit steady state error, but this can be minimised by using a PI controller, and a PWM transport delay [17]. Figure 6.8 shows a standard PR current controller in the neutral frame.

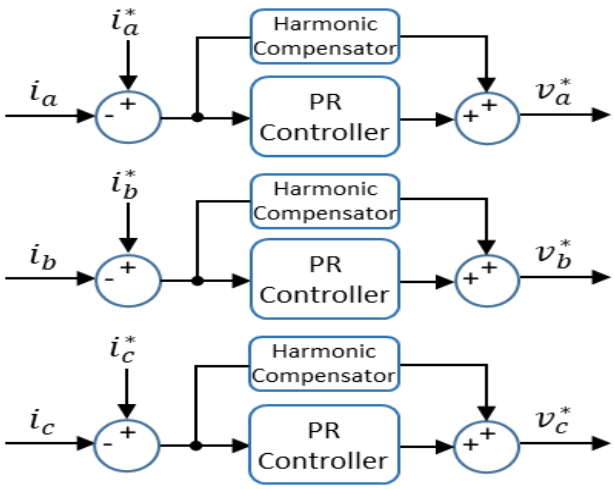

Figure 6.8: Neutral frame PR current control and harmonic compensator

where i_a^* is reference phase current, i_a phase current and v_a^* is reference phase voltage.

Proportional-Resonant (PR) current controller $G_c(s)$ may be defined by equation (6.7).

$$G_c(s) = K_p + K_i \frac{s}{s^2+{\omega_0}^2} \tag{6.7}$$

The harmonic compensator (HC) $G_h(s)$ may be defined by equation (6.8).

$$G_h(s) = K_{ih} \frac{s}{s^2+(\omega_0.h)^2} \tag{6.8}$$

where K_p is proportional gain K_i is integral controller gain, ω_0 is the fundamental frequency in radians, and h is the order of harmonic to be compensated.

Harmonic compensators are used to filter out specific low order harmonics. It is discussed that the PR controllers have better disturbance rejection and lower steady state error capability in neutral frame compared to a PI controller [18]. Also, the integral part in the PI controllers becomes ineffective at compensating higher order harmonics [19].

7.3.2 Stationary Reference Frame ($\alpha\beta0$ frame)

To use the stationary reference frame, neutral frame currents are transformed onto the stationary reference frame ($\alpha\beta0$ frame) using the Clarke transformation in three-phase systems. This reduces the number of controllable variables from three to two, however two controllers affect all three-phase currents [17]. In single-phase systems, the Clarke transformation (see Appendix B) cannot be applied directly due to the presence of only one phase [20]. In order to solve this, an imaginary orthogonal phase may be created with 90° (T/4) phase delay compared to the original. Using the $\alpha\beta0$ frame current control in single-phase systems, still two controllers are required; one for each α and β quadrature. Figure 6.9 shows the control structure of a stationary frame PR current controller with harmonic compensators in a three-phase system.

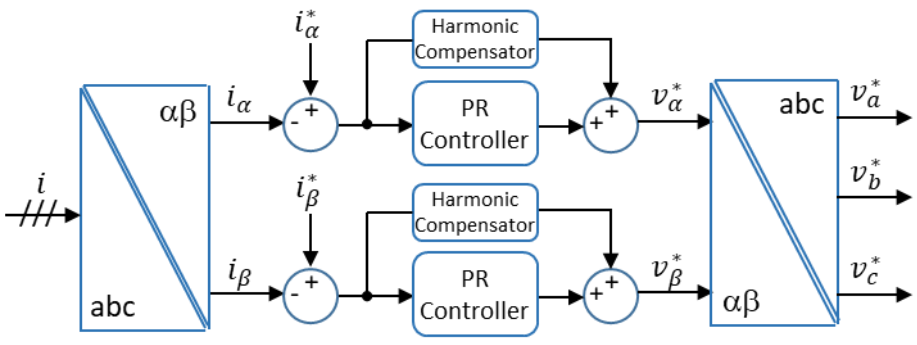

Figure 6.9: Stationary frame PR current controller and harmonic compensator

7.3.3 Synchronous Rotating Frame (*dq0* frame)

Synchronous rotating frame is popular and used commonly in control of not only grid-tie converters but also in electrical machines. The idea behind *dq0* frame control is to convert the sinusoidal nature of grid waveforms into DC values by transforming them into a rotating frame. This transformation is achieved by Clarke and Park transformation (see Appendix B). The synchronous rotating frame rotates with the fundamental angular frequency (ω). *dq0* frame can achieve zero steady state error due to infinite gain capability of an integrator at zero frequency [16, 21]. It should be noted that due to the rotating axis, the *d* and *q*-axis components are coupled in the converter model and therefore need to be decoupled. Decoupling (ωL) needs to be achieved by careful controller design as plant inductance values may have some uncertainty in practice [22]. Moreover, grid voltages in the *dq0* frame (v_d and v_q) should be feedforwarded to the system. Decoupling terms and feedforwarding reduces the effort of PI controllers, therefore a better steady state and dynamic performance are achieved. Harmonic compensation in the *dq0* frame may be achieved by implementation of resonant integrators as higher order harmonics are still AC quantities in the same synchronous frame [23]. The structure of a synchronous frame PI current controller with harmonic compensator is shown in Figure 6.9.

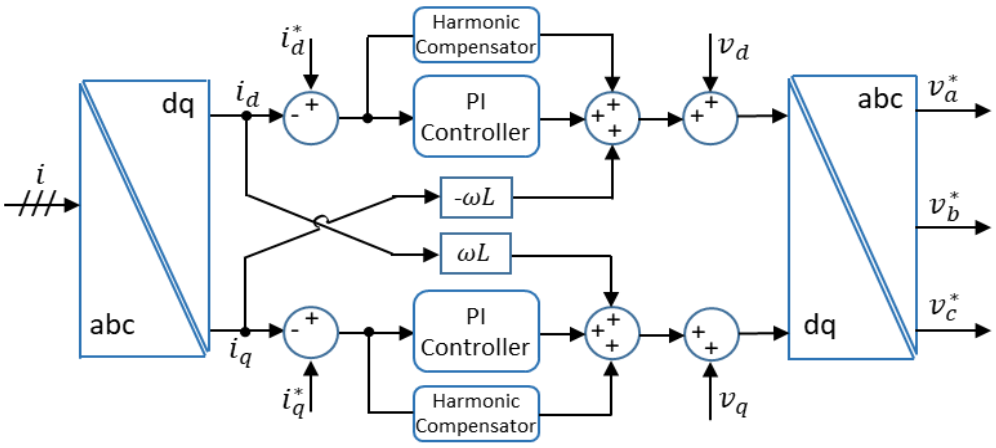

Figure 6.10: Synchronous frame PI current control and harmonic compensator

Proportional-Integral (PI) current controller $G_c(s)$ defined in equation (6.9).

$$G_c(s) = K_p + \frac{K_i}{s} \tag{6.9}$$

where K_p is proportional gain and K_i is integral controller gain.

Due to zero steady state error capability, the current controller used in this work is implemented in the synchronous rotating frame.

6.5 Grid Synchronisation and Phase Locked Loop

Grid-tie converters require synchronisation algorithms to extract useful information from the grid voltage, therefore the voltage output of the converter may be adjusted accordingly. It is vital to identify frequency and phase information of the utility grid, hence the phase and magnitude of the injected/extracted current can be determined. There are several ways to implement grid synchronisation algorithms such as with the use of filters and phase locked loops (PLLs) [24]. In [25], it is discussed that although filter algorithms are simpler to implement, they lack accuracy when the tracked signal has frequency variations under unbalanced grid conditions. Conversely, PLL based algorithms are harder to implement but they have better dynamic response.

A general structure of a PLL system can be seen in Figure 6.11, including a phase detector, loop filter and an oscillator.

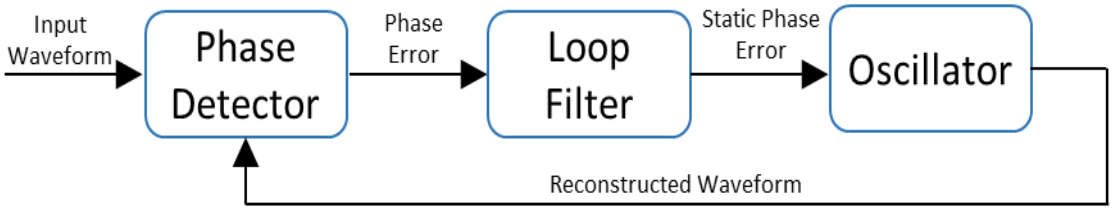

Figure 6.11: Structure of a Phase Locked Loop

A phase detector is used to find the phase error between the input waveform and the regenerated waveform. Generally, a loop filter is used to low pass filter the signal, which is then fed into an oscillator to reconstruct the generated signal continuously. In the early days, a PLL was constructed with analogue circuitry, but nowadays they are generally implemented in DSPs. PLLs can be implemented in either single-phase or multiple-phase systems, therefore the internal construction is slightly different for each application. In three-phase systems, the input signals can be converted into stationary reference or synchronous rotating frame with the help of Clarke and Park transformations. The output is then filtered and phase angle can be determined accordingly. This is one of the most popular and simplest algorithms in literature. In [26], a software based three-phase PLL is implemented and tested under distorted utility conditions.

In single-phase systems, grid synchronisation can be categorised depending on the system structure. In open loop systems, synchronisation can be done by using filters such as Kalman filters [27], adaptive notch filters [28] and artificial neural networks [29, 30].

In closed loop systems, various PLL based solutions are available in literature such as the adaptive PLL [31], orthogonal signal based PLL [32] and enchanted PLL [33]. Due to its simplicity and ease of compatibility with a synchronous reference frame based current controller, the orthogonal signal based PLL is used in the system in this work. Figure 6.12 represents block diagram of a single-phase PLL in the synchronous rotating frame.

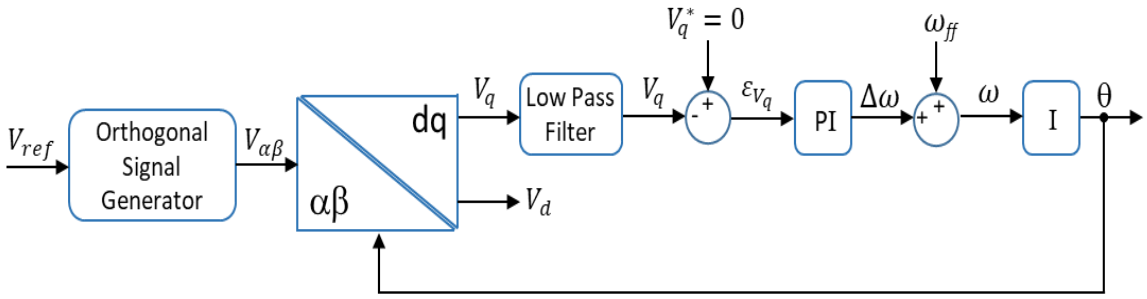

Figure 6.12: Single-phase Phase Locked Loop in synchronous rotating frame

There are various methods for generating the required orthogonal signal in a single-phase system, but here a T/4 transport delay is used to generate the β quadrature of the reference signal in the stationary reference frame, then the Park transform is applied to process the information into the synchronous rotating frame. The signal is then filtered, and passed through a PI controller, which can be used as a digital loop filter. The feedforward term of reference signal is added to the output of the loop filter and then integrated to calculate the phase information. The PLL is implemented in a NI cRIO 9063. Figure 6.13 shows the operation of the implemented PLL, gathering the frequency information (ω) of a 50 Hz normalised reference signal.

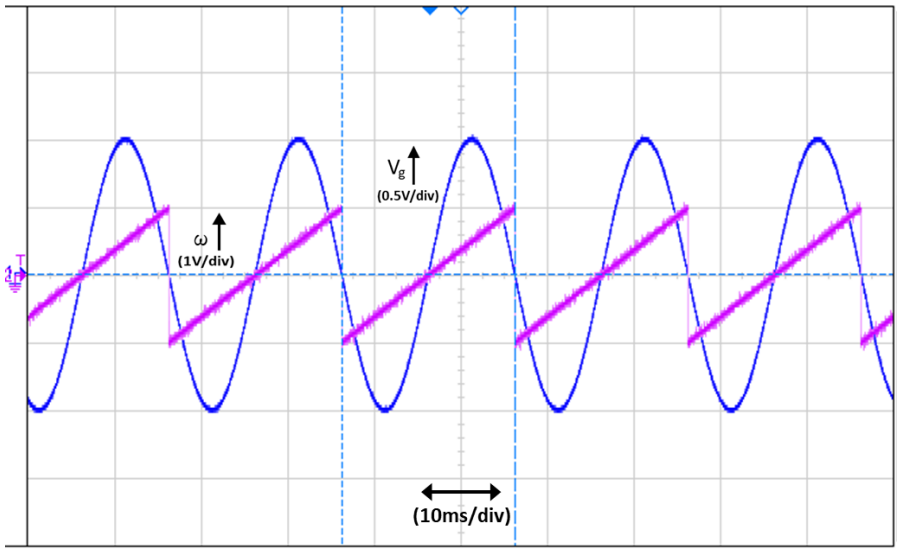

Figure 6.13: Normalised grid voltage and omega (ω) output of Phase Locked Loop

6.6 Synchronous Rotating Frame Current Controller Evaluation

As mentioned in previous sections, an orthogonal signal generator based PLL and a current controller in the synchronous rotating frame were implemented in a NI cRIO 9063 for closed loop control and synchronisation of the converter with the utility grid. The synchronous rotating frame current controller allows independent control of active and reactive current components, i_d and i_q respectively. As a result of this, it is possible to respond to active and/or reactive power commands given by the service provider independently.

In order to achieve independent active and reactive power control, a fast response inner current control loop is implemented for maintaining the required current magnitude and phase (see Figure 6.10). Moreover, a slower outer power loop is cascaded to the controller, which is responsible for controlling active and reactive power (P and Q) respectively. The equations for the slower power control loop (PQ control) are then given in equations (6.10) and (6.11).

$$P = v_d i_d + v_q i_q \tag{6.10}$$

$$Q = v_q i_d - v_d i_q \tag{6.11}$$

The PI controllers are tuned manually following the Ziegler-Nichols approach [34]. This method suggests setting an integral gain (K_i) to zero and increasing proportional gain (K_p) until ultimate gain (K_u) is reached. The ultimate gain is achieved when the output signal of the controller has stable and constant oscillations. The period of these oscillations (T_u) is then measured and the proportional and integral gains can be calculated according to a given table (see Appendix C). This method is selected for hardware tuning as the plant model may deviate from mathematical calculations. In order to achieve a higher bandwidth, the control system sampling frequency is selected to be double the switching frequency.

Figures 6.14 and 6.15 show the utility voltage (pink), and converter output current (navy blue), at the point of coupling when the current controllers have reached steady state. It should be noted that all given values of i_d and i_q, and their reference values i_d^* and i_q^* are in power units. The maximum power of the base system is 4 kVA.

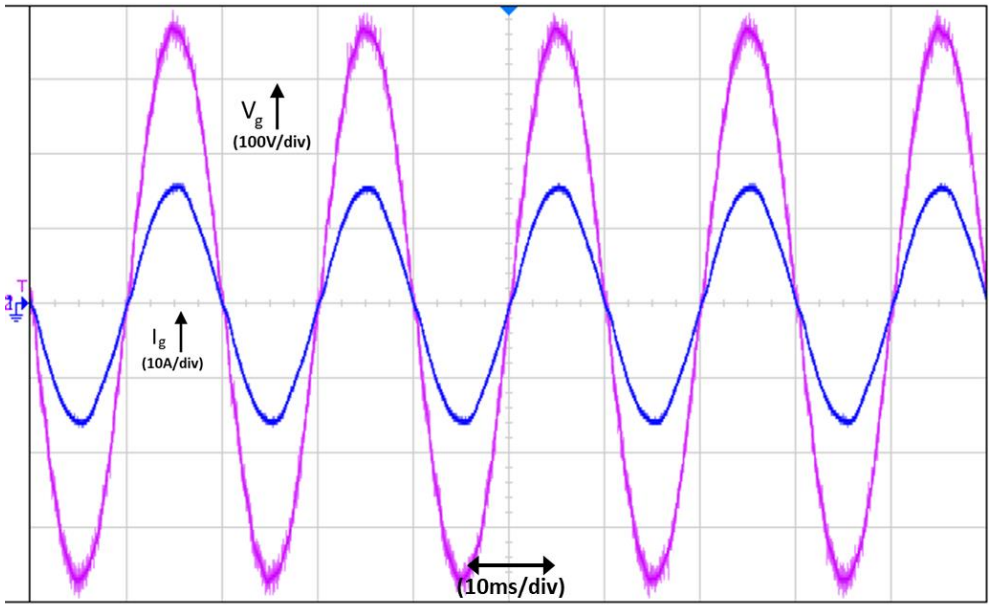

Figure 6.14: Utility voltage (pink) and output current (navy blue) when i_d^* = 0.7 and i_q^* = 0

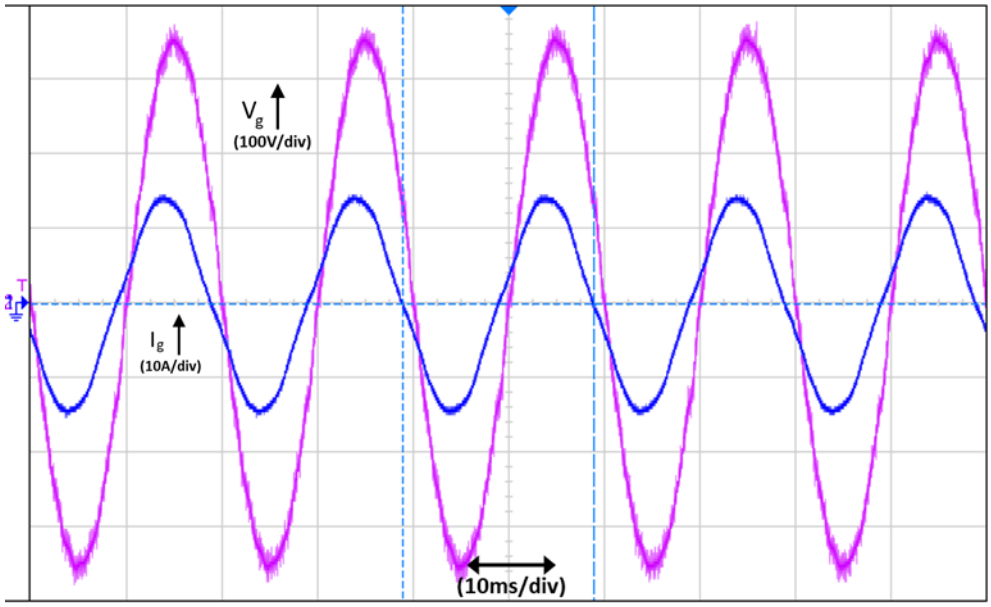

Figure 6.15: Utility voltage (pink) and output current (navy blue) i_d^* = 0.6 and i_q^* = 0.2

In Figure 6.14, the reference values of active and reactive current components are i_d^* = 0.7 and i_q^* = 0 respectively. By setting i_q^* = 0, purely active power flow can be achieved. The utility voltage and converter current are in phase, representing a power factor of 1. In Figure 6.15, the reference values of active and reactive current components are changed to i_d^* = 0.6 and i_q^* = 0.2 respectively. As seen from the Figure, the output current waveform leads the utility voltage, where P = 2.4 kW and Q = 800 VAr.

The transient response of the current controllers is illustrated in Figure 6.16, where a step change is applied to *d*-axis current reference, from i_d^* = 0 to i_d^* = 0.7. Meanwhile, *q*-axis current reference remains unchanged, i_q^* = 0.

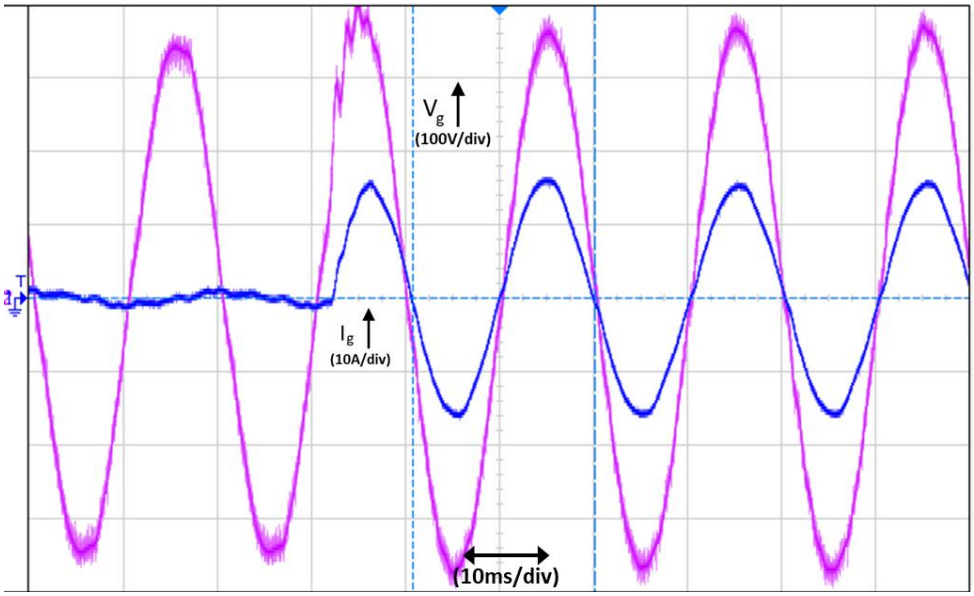

Figure 6.16: Utility voltage (pink) and output current (navy blue), step change of i_d^* = 0 to i_d^* = 0.7

In Figure 6.16, it can be seen that the output current is 0 before the step change in *d*-axis current reference. After the step change, the current controller reaches its steady state in less than 2 fundamental periods, < 40 ms. The harmonic content of the output current just after the transient period is given in Figure 6.17.

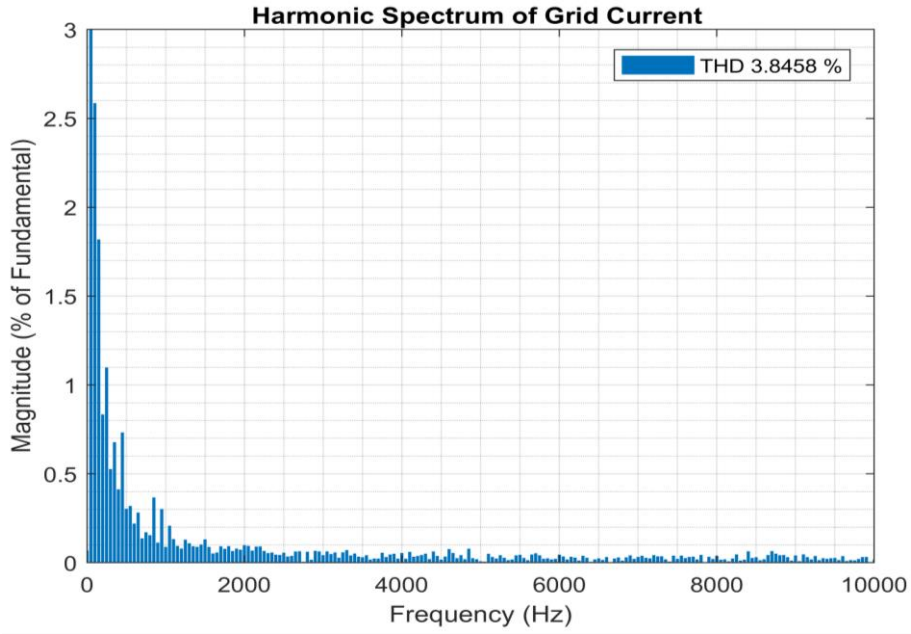

Figure 6.17: Harmonic spectrum of output current after 1 fundamental cycle of step change

The harmonic spectrum of output current waveform is measured after 1 fundamental cycle following the step change in *d*-axis current reference. Transient periods tend to have higher THD values, and here the THD value of output current is 3.84%, which complies with standards discussed in section 6.2. In Figure 6.16, during the step change response, the output current waveform does not overshoot, which is a good indication for system safety and correct controller tuning.

6.7 Safety and Protection

Safety measures need to be taken in order to conform to departmental health and safety regulations. Moreover, various parts of hardware should also be protected in case of a fault. Following sections detail safety and protection measures taken during experimental validation.

7.3.1 Safety Enclosure

The department health and safety regulations enforce all high voltage applications to be installed in a safety enclosure in order to reduce potential shock hazards. The enclosure should house the H-bridge modules, transformers, protection circuitry, LCL filter and point of grid coupling. The enclosure is fitted with an interlock for disconnecting the live circuitry when the enclosure lid is open. Furthermore, 6 fans are installed in push-pull configuration for thermal management. Figure 6.18 shows a picture of the full system and the workbench.

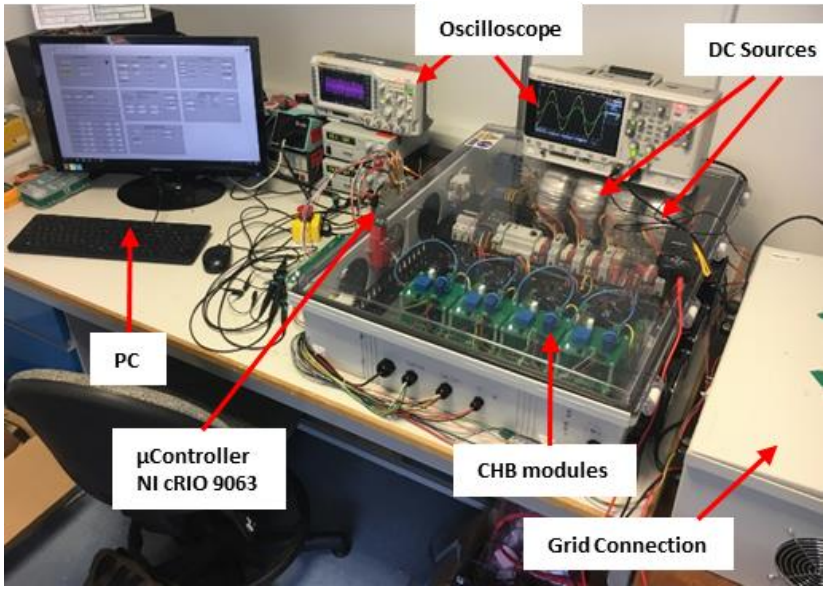

Figure 6.18: A picture of workbench and full system

7.3.2 Isolation and Circuit Breakers

Isolation and circuit breakers are required to minimize damage during a potential fault condition. VSCs generally consist of high and low voltage circuitry that need to be isolated from each other. Control hardware such as the DSPs and the FPGAs generally work at TTL level digital logic and cannot withstand voltage/current ratings that power modules operate. An isolation barrier is set between the FPGA and intelligent power modules (IPMs). In Figure 6.19, the isolation barrier between the FPGA and IPMs is shown.

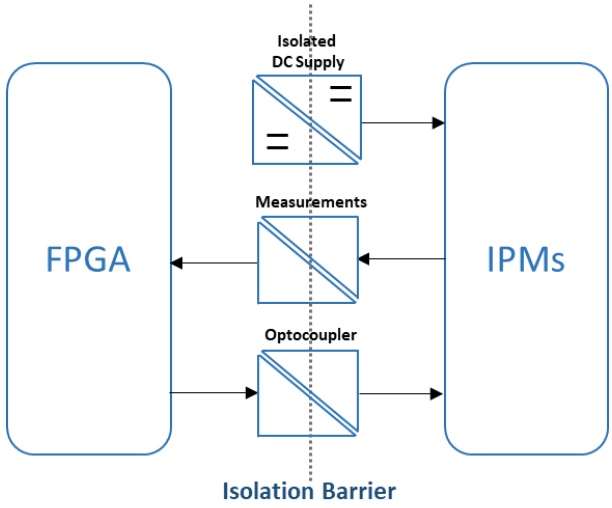

Figure 6.19: Isolation barrier between the FPGA and the intelligent power modules

DC power supplies feeding the auxiliary circuitry, current and voltage measurements taken from the IPMs and gating signals between the NI 9401 are isolated as mentioned in chapter 5. Regarding isolation, a 1:1 ratio isolating transformer is used to provide galvanic isolation at the point of grid coupling for initial testing. This transformer is rated for 3.3 kVA therefore a 13 A fuse added for additional safety. Moreover, the auxiliary circuitry is powered with a 10:1 transformer.

For protection, miniature circuit breakers (MCBs) are included in various parts of the circuitry for overcurrent protection. The first MCB is ABB System M Pro, three-phase type C and rated for 10 A, situated just after the three-phase coupling point in the safety enclosure. Then an ABB AF16-40-00-11 4-pole contactor, triggered by auxiliary circuitry, is used in series for dis/connecting the three-phase input. Finally, the primary side of each step-down transformers are also protected by a Schneider Electric 20A 1-pole type C MCBs. The circuit diagram and a photograph of hardware system consisting step down transformers, MCBs and contactors are shown in Figures 6.20 and 6.21 respectively.

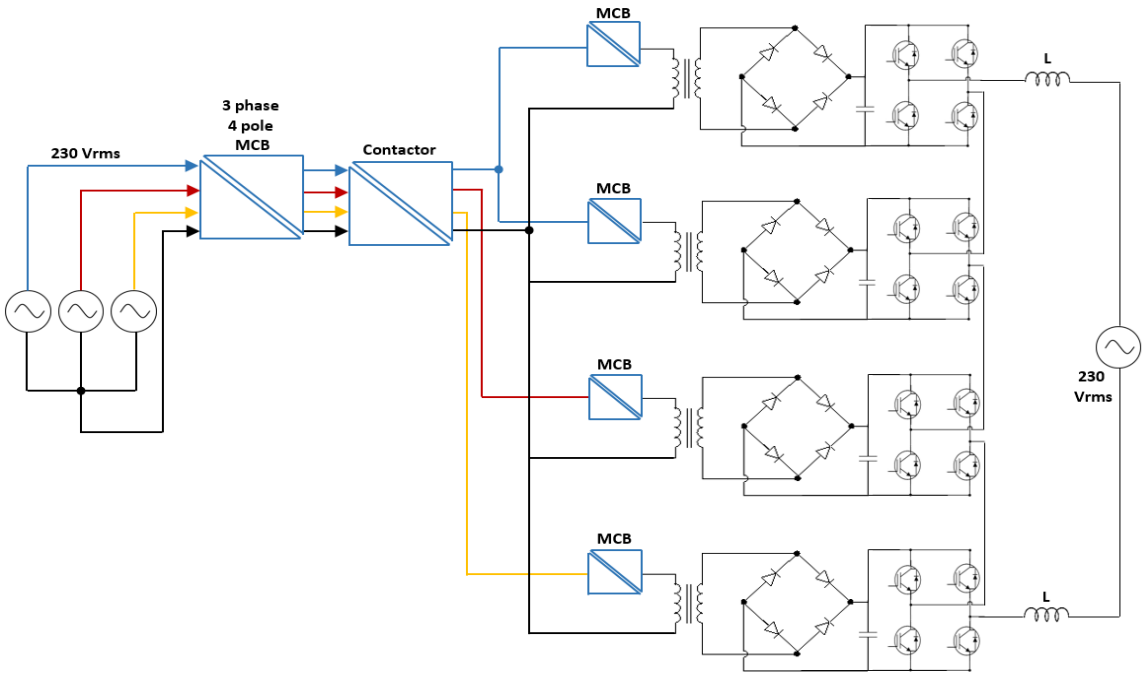

Figure 6.20: Block diagram of protection devices

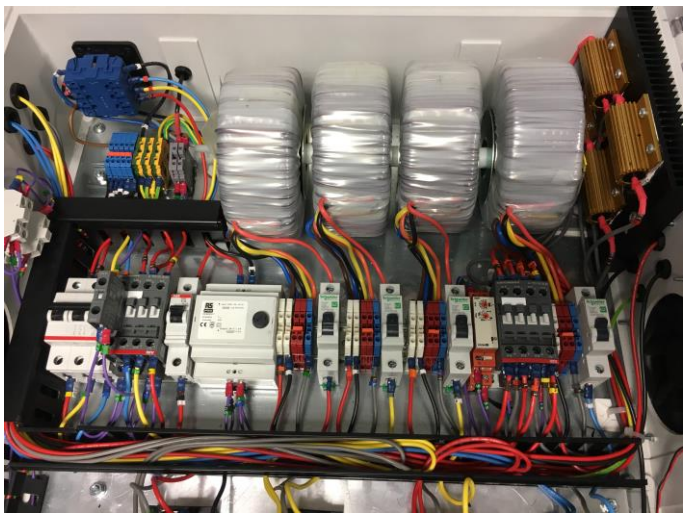

Figure 6.21: Transformers and protection circuitry

7.3.3 DC Link Management

The system has 4 toroidal step-down transformers for creating isolated DC supplies. Toroidal transformers are notorious for inrush currents therefore an inrush limiting circuit is designed for start-up in order not to trip the MCBs. The circuit consist of a 150 Ω 150 Watt resistor situated in the primary side of each transformers. This circuitry is disconnected with the help of a relay and contactor, triggered 7.5 seconds after initial start connection. Figure 6.22 shows DC link voltage waveforms for modules 1-4 during the start-up period.

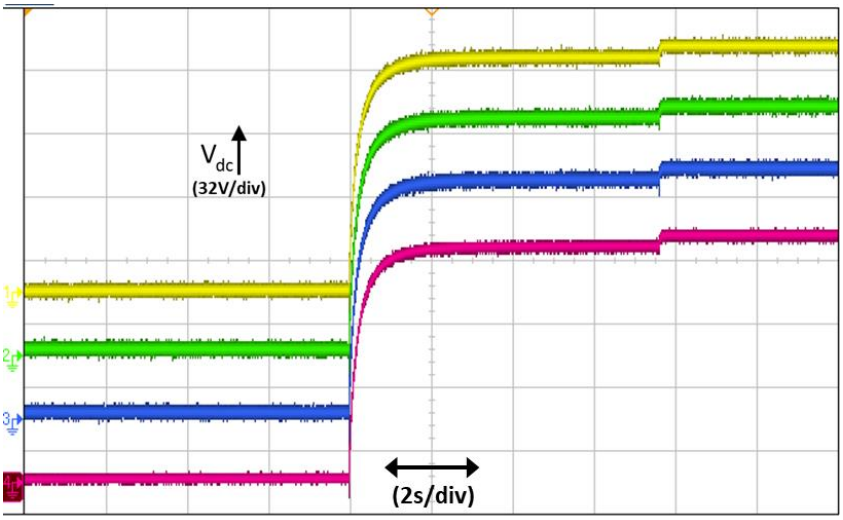

Figure 6.22: voltage waveforms for modules 1-4 during DC link pre-charge

Similarly, during shut-down period, the DC link capacitors must be discharged for safety reasons. In order to achieve this, bleeder resistors are paralleled with the DC link capacitors. Bleeder resistor are selected using equation (6.12).

$$V_c = V_0 . e^{\frac{-t}{RC}} \tag{6.12}$$

$$R = \frac{t}{\left(\ln\frac{V_c}{V_0}\right).C} = \frac{60}{\left(\ln\frac{112}{10}\right).6.6\times10^{-3}} = 3.76\ k\Omega$$

As a result, 3x 10 $k\Omega$ power resistors are used in parallel across the terminals of DC link capacitors. Although this causes extra losses during normal operation, the resistors ensure de-energisation of DC link capacitors in less than 60 seconds. Figure 6.23 shows the voltage waveforms for modules 1-4 during DC-link discharging.

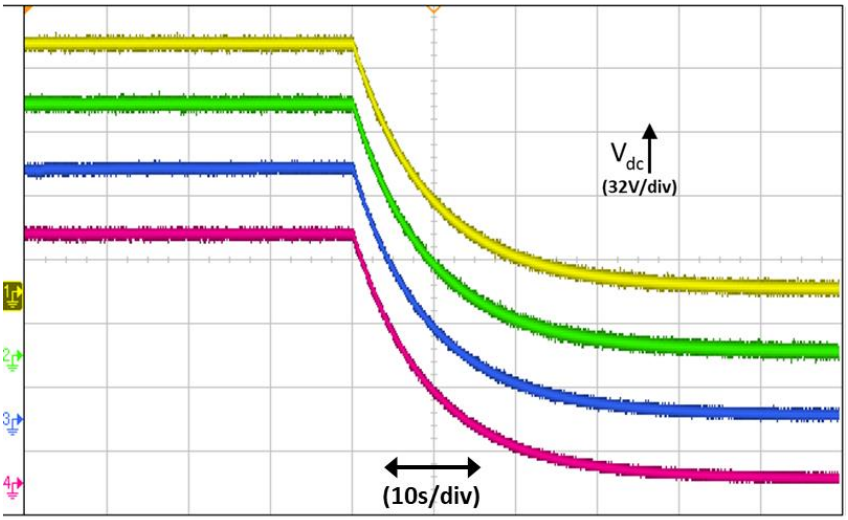

Figure 6.23: Voltage waveforms for modules 1-4 during DC link de-energise

6.8 Chapter Summary

This chapter firstly explored the regulations and standards enforced for grid-connected converters and appliances. Relating to this, possible output filter configurations are discussed for delivering high quality output voltage and current waveforms. The effect of these filter configurations on the output current waveform is also discussed.

Later, current control of MLCs in different frames and grid synchronisation methods are studied. For closed loop control operation, a phase locked loop and a current controller in the synchronous rotating frame are deployed. It has been shown that the closed loop current controller can respond to a given active and/or reactive power command in less than 2 fundamental cycles. The THD of the output current waveform found in compliance with the regulations and standards.

The final part of the chapter discusses the safety precautions taken during the experimental procedure to reduce potential risks at the work environment as well as experimental hardware.

Next chapter presents a conclusion for the work and also details potential future work.

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Chapter 7
Conclusions and Further Work

7.1 Introduction

This thesis has presented a 9-level multilevel cascaded H-bridge converter based system, developed for PV panels and EV batteries in their 2nd life application. The aim of the project was to use this converter in a domestic rooftop mounted system, in order to respond to any active/reactive power demands and use the storage system to help with the stabilisation of low the voltage distribution network. The negative effects of utilising grounded PV panels in a cascaded H-bridge converter have been analysed and the findings of the research has been presented in conferences such as EPE 2019.

Chapter 2 presented a literature review, detailing various multilevel converter topologies such as the neutral point converter (NPC), flying capacitor converter (FCC), modular multilevel converter (MMC) and cascaded H-bridge converter (CHB). The discussion includes topology comparison, operation and topology suitability into different application areas. Furthermore, various modulation methodologies for multilevel converters are discussed and their effect on output voltage waveform are presented. From this, the cascaded H-bridge converter was selected as the base system due to the lower requirement of total devices and importantly, its requirement for isolated DC sources. This would increase the accessibility for batteries in their 2nd life applications by dividing the total DC bus into smaller modules, and also reduce the total system cost.

Chapter 3 analysed leakage currents in transformerless converters. The analysis started by exploring the effect of galvanic isolation and stray capacitance of PV panels in grid-tie systems. A H-bridge produces both common-mode and differential mode voltages that create a varying voltage across the stray capacitances, causing leakage currents to ground. It is concluded that galvanic isolation helps by suppressing leakage current in a grounded PV coupled system, however the addition of a transformer generally adds to the cost of the system and may reduce conversion efficiency. Later in the chapter, methods for supressing leakage current in a transformerless converter are discussed. Topology solutions, common-mode filtering and modulation methods are also discussed. A mathematical analysis for

asymmetrical and symmetrical inductance filter configuration is represented. From the findings, a novel leakage reduction pulse width modulation (LRPWM) methodology was developed to maintain a constant voltage across the stray capacitances in order to supress leakage current in a 9-level CHB. It has also been discovered that if DC link voltages of each module are the same, then leakage current cannot be supressed solely by the modulation methods when an odd number of modules exist in the system. Conversely, leakage current reduction is possible when total number of modules are even. A generalised formula is proposed for the total voltage across the stray capacitances for an *m*-level CHB. Finally, a simulation study is presented comparing conventional modulation methods and the proposed LRPWM. It is shown that LRPWM can supress leakage current to 22 mA in a simulation study.

Chapter 4 started with detailing the specifications of the base system, then focusing on each part individually such as batteries, PV panels, DC-DC converter and AC-DC converter. Firstly, the specifications of EV batteries in their 2nd life application are detailed and their suitability for a domestic system is discussed. The design of a bidirectional buck-boost DC-DC converter is presented. A systematic approach is presented for the design of DC-DC converter, starting from mathematically defining converter parameters and then presenting a simulation study for both buck and boost operation. The same approach is then applied to a 9-level CHB converter, therefore the design of each conversion stage is detailed individually. Furthermore, the full base system including batteries, PV panels, DC-DC and AC-DC converters working in a closed loop system are simulated using MATLAB/Simulink software. Here, individual control of active/reactive power, grid synchronisation and battery state of charge balancing are shown.

Another contribution of Chapter 4 is to establish a co-simulation environment between LabVIEW and Multisim software by National Instruments. Co-simulation helped the author to achieve a closed-loop simulation of the FPGA code. It is important to mention that LabVIEW codes are automatically converted into VHDL which generally takes more than an hour to compile. In co-simulation, the digital LabVIEW code can be optimised while it interacts with analogue simulation engine of Multisim, which consists of the virtual analogue CHB circuitry, therefore the total compiling time can be greatly reduced. This also helped author to effectively design loop timings in control algorithm, which is technically more difficult in MATLAB/Simulink as additional toolboxes are required.

Chapter 5 focused on hardware implementation and evaluation of the base system. Firstly, the main control hardware and its slave controller are detailed. A step-by-step approach for generating gate pulses for LRPWM is presented. Then the design of a sensor board, which consists isolated voltage and current measurements, and also signal conditioning are presented. Later in the chapter, intelligent power module that consists of individual H-bridges and its thermal design procedure are discussed. Experimental results of the base system are given when stray capacitances are added to the system, and when different modulation techniques are applied as the modulator. The experimental results verify the simulation study results given in chapter 3, and are as expected. It can be said that LRPWM can supress the leakage current to 24 mA, which conforms to standard VDE-0126-1-1. Furthermore, the output current waveform has 1.72% THD that also complies with regulation and standards. It should be noted that DC-DC converters was not built due to time and research funding limitations.

Chapter 6 details regulation and standards relating to the power quality and allowed frequency and voltage ranges in a grid-tie converter. According to this, a literature review and simulation study for grid filters are presented. It is concluded that an 'LCL' filter with symmetrical filter inductance configuration can supress leakage current and conform to standards. Later in the chapter, phase locked loops and current control of multilevel converters in different frames are discussed. The author decided to use a PI current controller in synchronous rotating frame because of its superior steady state performance and infinite integral gain capability at zero frequency. The results of current controller for steady state and transient operation are shown and the performance of the current controller found to be satisfactory. Finally, safety and protection measures taken during experimental procedure are explained, detailing isolation barrier between low and high voltage circuitry and also control measures taken for correct operation of hardware during start-up and shut-down period.

7.2 Conclusions

This work provides a data driven practical analysis of a cascaded H-bridge multilevel converter, where a potential designer can initialise his/her research based on mathematical foundations. This thesis may be a guide on how to design the converter, select components, analytically understand the occurrence of ground leakage currents and take measures how to suppress it conforming to relevant standards. Furthermore, presented novel analytical

general formula for an *m*-level CHB converter urges the potential designer to use even number of H-bridge modules when leakage current suppression is essential.

This work also provides a co-simulation study where implementation of control system is achieved in a virtual environment, where no analogue circuitry is required. This, not only pre-ensures the control capability of the hardware, but also reduces the implementation time of an FPGA compilation process. The control system also allows dynamic change of control variables after the first compilation is complete. Following this, hours of compilation time may be diminished by a researcher.

Finally, this work presents a system that comprises of components that are widely available in market. It is shown that multilevel converters in an industrial or domestic application, may not badly suffer from predicted issues (ground leakage currents) if carefully designed. This may mitigate some concerns on multilevel converters; shifting them from being an academic interest to practical use, such as in domestic rooftop applications.

Utilising EV batteries (2^{nd} life application) with renewable generation, may be beneficial for low voltage distribution network stability. This work also adds value to EV batteries and enables them to be used longer before their end life, which is recycling. However, practical use of multilevel converters in domestic scale applications is still debateable due to cost, reliability and safety concerns in a grounded system. Presented novel work alleviates the safety concerns, improves not only the efficiency of the converter, but also power quality of conversion as ground leakage current is effectively supressed. It should be noted that this solution is independent of vital design parameters such as the switching frequency.

This work has shown that an MLC that utilises both renewable and storage elements may add value to EV batteries in their 2^{nd} life application, boosting their asset value. Moreover, it may also ease the problems caused by high share of renewables in generation mix.

7.3 Future Work

This research project exposed various future work opportunities that are suggested below.

7.3.1 Leakage Current Analysis and Modulation Techniques

The analysis done in this research project covered modulation-based solutions. As explained in chapter 3, it is possible to supress leakage current with topology changes and addition of common-mode chokes. The author suggests further investigation into combining these solutions together.

In literature, it is mentioned that battery and heatsink stray capacitance have accountable effect in ground leakage current therefore further investigation of these systems is advised. Furthermore, the effect of grid impedance, dead-time of switching devices and unbalanced operation of DC link voltage are also important to understand the problem, and therefore improve the solutions. Active grid filtering may be one of the potential solutions.

LRPWM is proposed with the aim of stabilising the total voltage across the stray capacitances, by taking into consideration of lowest possible switching events during a fundamental period for minimising power loss. This causes unbalanced power extraction from batteries, resulting in higher degrading of some batteries than others. Therefore, a battery management system plays a crucial role and needs to be further investigated.

Alternatively, the modulation algorithm may be further simplified and even converted into a generalised formula, which then extends the implementation of generating gate signals for an *m*-level CHB. This may further simplify the implementation of modulation algorithm.

7.3.2 High Frequency / High Power Application

The converter is built with industry made intelligent power modules, consisting IGBTs as switching devices. This has limited the switching frequency $\leq$ 20 kHz. The results in chapter 5 reveal that ground leakage current in conventional modulation schemes decreases when switching frequency increases. It may be motivating to increase switching frequency $\geq$ 100 kHz and analyse the results. Interestingly, phase disposition pulse width modulation (PDPWM) may have achieved VDE-0126-1-1 standard ground leakage current limit with increasing switching frequency. Furthermore, high frequency switching not only allows volume reduction of reactive components such as common-mode chokes and DC link capacitors, but also increases the output waveform quality.

The converter is limited to 4 kVA power rating and designed for domestic rooftop applications. It may be interesting to increase power rating to understand the challenges that need to be addressed. The author suggests looking into research areas such as switching device loss distribution, control optimisation for low switching frequency application and thermal management and packaging.

7.3.3 Energy Management Algorithm

The converter studied in this research can respond to independent active/reactive power demand requests. It is possible to create an algorithm benefitting the distribution network

operator therefore this converter may be used in voltage stabilisation. While doing this, a battery charge control algorithm should be designed to control battery state of charge taking into consideration of variables such as weather, time, planned maintenance and calendar of month.

7.3.4 Reliability and Number of Levels

Multilevel converters consist of higher number of components compared to industry standard 2-level converters, making them less reliable. Conversely, MLCs enhances power quality, adds fault tolerance and modularity to the system. It can be said that there is a trade-off between the reliability and the number of levels of an MLC within a specific application. Here, a question arises whether a configuration can be found to optimise the trade-off between the reliability and the number of present levels in an MLC. The analysis should detail the following performance related aspects; device power loss, thermal performance, reliability and cost optimisation of the system.

7.3.5 Redundancy and Fault Tolerance

Multilevel converters consist two or more modules that contribute to power conversion. Despite diminishing reliability of MLCs with higher number of modules, fault tolerant operation may be achievable. It may be possible to disable faulty modules and operate the converter while the fault is still present. Similarly, redundancy of modules may create freedom during designing process. Future work should cover modulation techniques, power sharing of modules and ground leakage current suppression.

Appendices

Appendix A – Switching States

5-level CHB switching states:

Sa1	Sa3	Sb1	Sb3	Output Voltage	Vcm1	Vcm2	Vdm1	Vdm2	VcmTotal	Vnto(SYM)	Vnto(ASYM)
1	0	1	0	2	0.5	0.5	1	1	1	-1	1
0	0	1	0	1	0	0.5	0	1	0.5	0	1
1	0	0	0	1	0.5	0	1	0	0.5	-1	0
1	0	1	1	1	0.5	1	1	0	1.5	-2	-1
1	1	1	0	1	1	0.5	0	1	1.5	-1	0
0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	1	0	0	1	-1	-1
1	0	0	1	0	0.5	0.5	1	-1	1	-2	-2
0	1	1	0	0	0.5	0.5	-1	1	1	0	0
1	1	0	0	0	1	0	0	0	1	-1	-1
1	1	1	1	0	1	1	0	0	2	-2	-2
0	0	0	1	-1	0	0.5	0	-1	0.5	-1	-2
0	1	0	0	-1	0.5	0	-1	0	0.5	0	-1
0	1	1	1	-1	0.5	1	-1	0	1.5	-1	-2
1	1	0	1	-1	1	0.5	0	-1	1.5	-2	-3
0	1	0	1	-2	0.5	0.5	-1	-1	1	-1	-3

7-level CHB switching states:

Sa1	Sa3	Sb1	Sb3	Sc1	Sc3	Output Voltage	Vcm1	Vcm2	Vcm3	Vdm1	Vdm2	Vdm3	VcmTotal	Vnto(SYM)	Vnto(ASYM)
1	0	1	0	1	0	3	0.5	0.5	0.5	1	1	1	1.5	-1.5	3
0	0	1	0	1	0	2	0	0.5	0.5	0	1	1	1	0	3
1	0	0	0	1	0	2	0.5	0	0.5	1	0	1	1	-1	2
1	0	1	0	0	0	2	0.5	0.5	0	1	1	0	1	-2	1
1	0	1	0	1	1	2	0.5	0.5	1	1	1	0	2	-3	0
1	0	1	1	1	0	2	0.5	1	0.5	1	0	1	2	-2	1
1	1	1	0	1	0	2	1	0.5	0.5	0	1	1	2	-1	2
0	0	0	0	1	0	1	0	0	0.5	0	0	1	0.5	0.5	2
0	0	1	0	0	0	1	0	0.5	0	0	1	0	0.5	-0.5	1
0	0	1	0	1	1	1	0	0.5	1	0	1	0	1.5	-1.5	0
0	0	1	1	1	0	1	0	1	0.5	0	0	1	1.5	-0.5	1
1	0	0	0	0	0	1	0.5	0	0	1	0	0	0.5	-1.5	0
1	0	0	0	1	1	1	0.5	0	1	1	0	0	1.5	-2.5	-1
1	0	1	0	0	1	1	0.5	0.5	0.5	1	1	-1	1.5	-3.5	-2
1	0	0	1	1	0	1	0.5	0.5	0.5	1	-1	1	1.5	-1.5	0
1	0	1	1	0	0	1	0.5	1	0	1	0	0	1.5	-2.5	-1
1	0	1	1	1	1	1	0.5	1	1	1	0	0	2.5	-3.5	-2
0	1	1	0	1	0	1	0.5	0.5	0.5	-1	1	1	1.5	0.5	2
1	1	0	0	1	0	1	1	0	0.5	0	0	1	1.5	-0.5	1
1	1	1	0	0	0	1	1	0.5	0	0	1	0	1.5	-1.5	0
1	1	1	0	1	1	1	1	0.5	1	0	1	0	2.5	-2.5	-1
1	1	1	1	1	0	1	1	1	0.5	0	0	1	2.5	-1.5	0

7-level CHB switching states continued:

Sa1	Sa3	Sb1	Sb3	Sc1	Sc3	Output Voltage	Vcm1	Vcm2	Vcm3	Vdm1	Vdm2	Vdm3	VcmTotal	Vnto(SYM)	Vnto(ASYM)
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	1	0	0	0	1	0	0	0	1	-1	-1
0	0	1	0	0	1	0	0	0.5	0.5	0	1	-1	1	-2	-2
0	0	0	1	1	0	0	0	0.5	0.5	0	-1	1	1	0	0
0	0	1	1	0	0	0	0	1	0	0	0	0	1	-1	-1
0	0	1	1	1	1	0	0	1	1	0	0	0	2	-2	-2
1	0	0	0	0	1	0	0.5	0	0.5	1	0	-1	1	-3	-3
1	0	0	1	0	0	0	0.5	0.5	0	1	-1	0	1	-2	-2
1	0	0	1	1	1	0	0.5	0.5	1	1	-1	0	2	-3	-3
1	0	1	1	0	1	0	0.5	1	0.5	1	0	-1	2	-4	-4
0	1	0	0	1	0	0	0.5	0	0.5	-1	0	1	1	1	1
0	1	1	0	0	0	0	0.5	0.5	0	-1	1	0	1	0	0
0	1	1	0	1	1	0	0.5	0.5	1	-1	1	0	2	-1	-1
0	1	1	1	1	0	0	0.5	1	0.5	-1	0	1	2	0	0
1	1	0	0	0	0	0	1	0	0	0	0	0	1	-1	-1
1	1	0	0	1	1	0	1	0	1	0	0	0	2	-2	-2
1	1	1	0	0	1	0	1	0.5	0.5	0	1	-1	2	-3	-3
1	1	0	1	1	0	0	1	0.5	0.5	0	-1	1	2	-1	-1
1	1	1	1	0	0	0	1	1	0	0	0	0	2	-2	-2
1	1	1	1	1	1	0	1	1	1	0	0	0	3	-3	-3
0	0	0	0	0	1	-1	0	0	0.5	0	0	-1	0.5	-1.5	-3
0	0	0	1	0	0	-1	0	0.5	0	0	-1	0	0.5	-0.5	-2
0	0	0	1	1	1	-1	0	0.5	1	0	-1	0	1.5	-1.5	-3
0	0	1	1	0	1	-1	0	1	0.5	0	0	-1	1.5	-2.5	-4
1	0	0	1	0	1	-1	0.5	0.5	0.5	1	-1	-1	1.5	-3.5	-5
0	1	0	0	0	0	-1	0.5	0	0	-1	0	0	0.5	0.5	-1
0	1	0	0	1	1	-1	0.5	0	1	-1	0	0	1.5	-0.5	-2
0	1	1	0	0	1	-1	0.5	0.5	0.5	-1	1	-1	1.5	-1.5	-3
0	1	0	1	1	0	-1	0.5	0.5	0.5	-1	-1	1	1.5	0.5	-1
0	1	1	1	0	0	-1	0.5	1	0	-1	0	0	1.5	-0.5	-2
0	1	1	1	1	1	-1	0.5	1	1	-1	0	0	2.5	-1.5	-3
1	1	0	0	0	1	-1	1	0	0.5	0	0	-1	1.5	-2.5	-4
1	1	0	1	0	0	-1	1	0.5	0	0	-1	0	1.5	-1.5	-3
1	1	0	1	1	1	-1	1	0.5	1	0	-1	0	2.5	-2.5	-4
1	1	1	1	0	1	-1	1	1	0.5	0	0	-1	2.5	-3.5	-5
0	0	0	1	0	1	-2	0	0.5	0.5	0	-1	-1	1	-2	-5
0	1	0	0	0	1	-2	0.5	0	0.5	-1	0	-1	1	-1	-4
0	1	0	1	0	0	-2	0.5	0.5	0	-1	-1	0	1	0	-3
0	1	0	1	1	1	-2	0.5	0.5	1	-1	-1	0	2	-1	-4
0	1	1	1	0	1	-2	0.5	1	0.5	-1	0	-1	2	-2	-5
1	1	0	1	0	1	-2	1	0.5	0.5	0	-1	-1	2	-3	-6
0	1	0	1	0	1	-3	0.5	0.5	0.5	-1	-1	-1	1.5	-1.5	-6

9-level CHB switching states:

Sa1	Sa3	Sb1	Sb3	Sc1	Sc3	Sd1	Sd3	Output Voltage	Vcm1	Vcm2	Vcm3	Vcm4	Vdm1	Vdm2	Vdm3	Vdm4	VcmTotal	Vnto(SYM)	Vnto(ASYM)
1	0	1	0	1	0	1	0	4	0.5	0.5	0.5	0.5	1	1	1	1	2	-2	6
0	0	1	0	1	0	1	0	3	0	0.5	0.5	0.5	0	1	1	1	1.5	0	6
1	0	0	0	1	0	1	0	3	0.5	0	0.5	0.5	1	0	1	1	1.5	-1	5
1	0	1	0	0	0	1	0	3	0.5	0.5	0	0.5	1	1	0	1	1.5	-2	4
1	0	1	0	1	0	0	0	3	0.5	0.5	0.5	0	1	1	1	0	1.5	-3	3
1	0	1	0	1	0	1	1	3	0.5	0.5	0.5	1	1	1	1	0	2.5	-4	2
1	0	1	0	1	1	1	0	3	0.5	0.5	1	0.5	1	1	0	1	2.5	-3	3
1	0	1	1	1	0	1	0	3	0.5	1	0.5	0.5	1	0	1	1	2.5	-2	4
1	1	1	0	1	0	1	0	3	1	0.5	0.5	0.5	0	1	1	1	2.5	-1	5
0	0	0	0	1	0	1	0	2	0	0	0.5	0.5	0	0	1	1	1	1	5
0	0	1	0	0	0	1	0	2	0	0.5	0	0.5	0	1	0	1	1	0	4
0	0	1	0	1	0	0	0	2	0	0.5	0.5	0	0	1	1	0	1	-1	3
0	0	1	0	1	0	1	1	2	0	0.5	0.5	1	0	1	1	0	2	-2	2
0	0	1	0	1	1	1	0	2	0	0.5	1	0.5	0	1	0	1	2	-1	3
0	0	1	1	1	0	1	0	2	0	1	0.5	0.5	0	0	1	1	2	0	4
1	0	0	0	0	0	1	0	2	0.5	0	0	0.5	1	0	0	1	1	-1	3
1	0	0	0	1	0	0	0	2	0.5	0	0.5	0	1	0	1	0	1	-2	2
1	0	0	0	1	0	1	1	2	0.5	0	0.5	1	1	0	1	0	2	-3	1
1	0	0	0	1	1	1	0	2	0.5	0	1	0.5	1	0	0	1	2	-2	2
1	0	1	0	0	0	0	0	2	0.5	0.5	0	0	1	1	0	0	1	-3	1
1	0	1	0	0	0	1	1	2	0.5	0.5	0	1	1	1	0	0	2	-4	0
1	0	1	0	1	0	0	1	2	0.5	0.5	0.5	0.5	1	1	1	-1	2	-5	-1
1	0	1	0	0	1	1	0	2	0.5	0.5	0.5	0.5	1	1	-1	1	2	-3	1
1	0	1	0	1	1	0	0	2	0.5	0.5	1	0	1	1	0	0	2	-4	0
1	0	1	0	1	1	1	1	2	0.5	0.5	1	1	1	1	0	0	3	-5	-1
1	0	0	1	1	0	1	0	2	0.5	0.5	0.5	0.5	1	-1	1	1	2	-1	3
1	0	1	1	0	0	1	0	2	0.5	1	0	0.5	1	0	0	1	2	-2	2
1	0	1	1	1	0	0	0	2	0.5	1	0.5	0	1	0	1	0	2	-3	1
1	0	1	1	1	0	1	1	2	0.5	1	0.5	1	1	0	1	0	3	-4	0
1	0	1	1	1	1	1	0	2	0.5	1	1	0.5	1	0	0	1	3	-3	1
0	1	1	0	1	0	1	0	2	0.5	0.5	0.5	0.5	-1	1	1	1	2	1	5
1	1	0	0	1	0	1	0	2	1	0	0.5	0.5	0	0	1	1	2	0	4
1	1	1	0	0	0	1	0	2	1	0.5	0	0.5	0	1	0	1	2	-1	3
1	1	1	0	1	0	0	0	2	1	0.5	0.5	0	0	1	1	0	2	-2	2
1	1	1	0	1	0	1	1	2	1	0.5	0.5	1	0	1	1	0	3	-3	1
1	1	1	0	1	1	1	0	2	1	0.5	1	0.5	0	1	0	1	3	-2	2
1	1	1	1	1	0	1	0	2	1	1	0.5	0.5	0	0	1	1	3	-1	3
0	0	0	0	0	0	1	0	1	0	0	0	0.5	0	0	0	1	0.5	1	3
0	0	0	0	1	0	0	0	1	0	0	0.5	0	0	0	1	0	0.5	0	2
0	0	0	0	1	0	1	1	1	0	0	0.5	1	0	0	1	0	1.5	-1	1
0	0	0	0	1	1	1	0	1	0	0	1	0.5	0	0	0	1	1.5	0	2
0	0	1	0	0	0	0	0	1	0	0.5	0	0	0	1	0	0	0.5	-1	1
0	0	1	0	0	0	1	1	1	0	0.5	0	1	0	1	0	0	1.5	-2	0
0	0	1	0	1	0	0	1	1	0	0.5	0.5	0.5	0	1	1	-1	1.5	-3	-1
0	0	1	0	0	1	1	0	1	0	0.5	0.5	0.5	0	1	-1	1	1.5	-1	1
0	0	1	0	1	1	0	0	1	0	0.5	1	0	0	1	0	0	1.5	-2	0
0	0	1	0	1	1	1	1	1	0	0.5	1	1	0	1	0	0	2.5	-3	-1
0	0	0	1	1	0	1	0	1	0	0.5	0.5	0.5	0	-1	1	1	1.5	1	3
0	0	1	1	0	0	1	0	1	0	1	0	0.5	0	0	0	1	1.5	0	2
0	0	1	1	1	0	0	0	1	0	1	0.5	0	0	0	1	0	1.5	-1	1
0	0	1	1	1	0	1	1	1	0	1	0.5	1	0	0	1	0	2.5	-2	0
0	0	1	1	1	1	1	0	1	0	1	1	0.5	0	0	0	1	2.5	-1	1
1	0	0	0	0	0	0	0	1	0.5	0	0	0	1	0	0	0	0.5	-2	0
1	0	0	0	0	0	1	1	1	0.5	0	0	1	1	0	0	0	1.5	-3	-1
1	0	0	0	1	0	0	1	1	0.5	0	0.5	0.5	1	0	1	-1	1.5	-4	-2
1	0	0	0	0	1	1	0	1	0.5	0	0.5	0.5	1	0	-1	1	1.5	-2	0
1	0	0	0	1	1	0	0	1	0.5	0	1	0	1	0	0	0	1.5	-3	-1
1	0	0	0	1	1	1	1	1	0.5	0	1	1	1	0	0	0	2.5	-4	-2
1	0	1	0	0	0	0	1	1	0.5	0.5	0	0.5	1	1	0	-1	1.5	-5	-3
1	0	1	0	0	1	0	0	1	0.5	0.5	0.5	0	1	1	-1	0	1.5	-4	-2
1	0	1	0	0	1	1	1	1	0.5	0.5	0.5	1	1	1	-1	0	2.5	-5	-3
1	0	1	0	1	1	0	1	1	0.5	0.5	1	0.5	1	1	0	-1	2.5	-6	-4
1	0	0	1	0	0	1	0	1	0.5	0.5	0	0.5	1	-1	0	1	1.5	-1	1
1	0	0	1	1	0	0	0	1	0.5	0.5	0.5	0	1	-1	1	0	1.5	-2	0
1	0	0	1	1	0	1	1	1	0.5	0.5	0.5	1	1	-1	1	0	2.5	-3	-1
1	0	0	1	1	1	1	0	1	0.5	0.5	1	0.5	1	-1	0	1	2.5	-2	0

9-level CHB switching states continued:

Sa1	Sa3	Sb1	Sb3	Sc1	Sc3	Sd1	Sd3	Output Voltage	Vcm1	Vcm2	Vcm3	Vcm4	Vdm1	Vdm2	Vdm3	Vdm4	VcmTotal	Vnto(SYM)	Vnto(ASYM)
1	0	0	1	1	1	1	0	1	0.5	0.5	1	0.5	1	-1	0	1	2.5	-2	0
1	0	1	1	0	0	0	0	1	0.5	1	0	0	1	0	0	0	1.5	-3	-1
1	0	1	1	0	0	1	1	1	0.5	1	0	1	1	0	0	0	2.5	-4	-2
1	0	1	1	1	0	0	1	1	0.5	1	0.5	0.5	1	0	1	-1	2.5	-5	-3
1	0	1	1	0	1	1	0	1	0.5	1	0.5	0.5	1	0	-1	1	2.5	-3	-1
1	0	1	1	1	1	0	0	1	0.5	1	1	0	1	0	0	0	2.5	-4	-2
1	0	1	1	1	1	1	1	1	0.5	1	1	1	1	0	0	0	3.5	-5	-3
0	1	0	0	1	0	1	0	1	0.5	0	0.5	0.5	-1	0	1	1	1.5	2	4
0	1	1	0	0	0	1	0	1	0.5	0.5	0	0.5	-1	1	0	1	1.5	1	3
0	1	1	0	1	0	0	0	1	0.5	0.5	0.5	0	-1	1	1	0	1.5	0	2
0	1	1	0	1	0	1	1	1	0.5	0.5	0.5	1	-1	1	1	0	2.5	-1	1
0	1	1	0	1	1	1	0	1	0.5	0.5	1	0.5	-1	1	0	1	2.5	0	2
0	1	1	1	1	0	1	0	1	0.5	1	0.5	0.5	-1	0	1	1	2.5	1	3
1	1	0	0	0	0	1	0	1	1	0	0	0.5	0	0	0	1	1.5	0	2
1	1	0	0	1	0	0	0	1	1	0	0.5	0	0	0	1	0	1.5	-1	1
1	1	0	0	1	0	1	1	1	1	0	0.5	1	0	0	1	0	2.5	-2	0
1	1	0	0	1	1	1	0	1	1	0	1	0.5	0	0	0	1	2.5	-1	1
1	1	1	0	0	0	0	0	1	1	0.5	0	0	0	1	0	0	1.5	-2	0
1	1	1	0	0	0	1	1	1	1	0.5	0	1	0	1	0	0	2.5	-3	-1
1	1	1	0	1	0	0	1	1	1	0.5	0.5	0.5	0	1	1	-1	2.5	-4	-2
1	1	1	0	0	1	1	0	1	1	0.5	0.5	0.5	0	1	-1	1	2.5	-2	0
1	1	1	0	1	1	0	0	1	1	0.5	1	0	0	1	0	0	2.5	-3	-1
1	1	1	0	1	1	1	1	1	1	0.5	1	1	0	1	0	0	3.5	-4	-2
1	1	0	1	1	0	1	0	1	1	0.5	0.5	0.5	0	-1	1	1	2.5	0	2
1	1	1	1	0	0	1	0	1	1	1	0	0.5	0	0	0	1	2.5	-1	1
1	1	1	1	1	0	0	0	1	1	1	0.5	0	0	0	1	0	2.5	-2	0
1	1	1	1	1	0	1	1	1	1	1	0.5	1	0	0	1	0	3.5	-3	-1
1	1	1	1	1	1	1	0	1	1	1	1	0.5	0	0	0	1	3.5	-2	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1	0	0	0	0	1	0	0	0	0	1	-1	-1
0	0	0	0	1	0	0	1	0	0	0	0.5	0.5	0	0	1	-1	1	-2	-2
0	0	0	0	0	1	1	0	0	0	0	0.5	0.5	0	0	-1	1	1	0	0
0	0	0	0	1	1	0	0	0	0	0	1	0	0	0	0	0	1	-1	-1
0	0	0	0	1	1	1	1	0	0	0	1	1	0	0	0	0	2	-2	-2
0	0	1	0	0	0	0	1	0	0	0.5	0	0.5	0	1	0	-1	1	-3	-3
0	0	1	0	0	1	0	0	0	0	0.5	0.5	0	0	1	-1	0	1	-2	-2
0	0	1	0	0	1	1	1	0	0	0.5	0.5	1	0	1	-1	0	2	-3	-3
0	0	1	0	1	1	0	1	0	0	0.5	1	0.5	0	1	0	-1	2	-4	-4
0	0	0	1	0	0	1	0	0	0	0.5	0	0.5	0	-1	0	1	1	1	1
0	0	0	1	1	0	0	0	0	0	0.5	0.5	0	0	-1	1	0	1	0	0
0	0	0	1	1	0	1	1	0	0	0.5	0.5	1	0	-1	1	0	2	-1	-1
0	0	0	1	1	1	1	0	0	0	0.5	1	0.5	0	-1	0	1	2	0	0
0	0	1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	1	-1	-1
0	0	1	1	0	0	1	1	0	0	1	0	1	0	0	0	0	2	-2	-2
0	0	1	1	1	0	0	1	0	0	1	0.5	0.5	0	0	1	-1	2	-3	-3
0	0	1	1	0	1	1	0	0	0	1	0.5	0.5	0	0	-1	1	2	-1	-1
0	0	1	1	1	1	0	0	0	0	1	1	0	0	0	0	0	2	-2	-2
0	0	1	1	1	1	1	1	0	0	1	1	1	0	0	0	0	3	-3	-3
1	0	0	0	0	0	0	1	0	0.5	0	0	0.5	1	0	0	-1	1	-4	-4
1	0	0	0	0	1	0	0	0	0.5	0	0.5	0	1	0	-1	0	1	-3	-3
1	0	0	0	0	1	1	1	0	0.5	0	0.5	1	1	0	-1	0	2	-4	-4
1	0	0	0	1	1	0	1	0	0.5	0	1	0.5	1	0	0	-1	2	-5	-5
1	0	1	0	0	1	0	1	0	0.5	0.5	0.5	0.5	1	1	-1	-1	2	-6	-6
1	0	0	1	0	0	0	0	0	0.5	0.5	0	0	1	-1	0	0	1	-2	-2
1	0	0	1	0	0	1	1	0	0.5	0.5	0	1	1	-1	0	0	2	-3	-3
1	0	0	1	1	0	0	1	0	0.5	0.5	0.5	0.5	1	-1	1	-1	2	-4	-4
1	0	0	1	0	1	1	0	0	0.5	0.5	0.5	0.5	1	-1	-1	1	2	-2	-2
1	0	0	1	1	1	0	0	0	0.5	0.5	1	0	1	-1	0	0	2	-3	-3
1	0	0	1	1	1	1	1	0	0.5	0.5	1	1	1	-1	0	0	3	-4	-4
1	0	1	1	0	0	0	1	0	0.5	1	0	0.5	1	0	0	-1	2	-5	-5
1	0	1	1	0	1	0	0	0	0.5	1	0.5	0	1	0	-1	0	2	-4	-4
1	0	1	1	0	1	1	1	0	0.5	1	0.5	1	1	0	-1	0	3	-5	-5
1	0	1	1	1	1	0	1	0	0.5	1	1	0.5	1	0	0	-1	3	-6	-6
0	1	0	0	0	0	1	0	0	0.5	0	0	0.5	-1	0	0	1	1	2	2
0	1	0	0	1	0	0	0	0	0.5	0	0.5	0	-1	0	1	0	1	1	1
0	1	0	0	1	0	1	1	0	0.5	0	0.5	1	-1	0	1	0	2	0	0
0	1	0	0	1	1	1	0	0	0.5	0	1	0.5	-1	0	0	1	2	1	1

9-level CHB switching states continued:

Sa1	Sa3	Sb1	Sb3	Sc1	Sc3	Sd1	Sd3	Output Voltage	Vcm1	Vcm2	Vcm3	Vcm4	Vdm1	Vdm2	Vdm3	Vdm4	VcmTotal	Vnto(SYM)	Vnto(ASYM)
0	1	1	0	0	0	0	0	0	0.5	0.5	0	0	-1	1	0	0	1	0	0
0	1	1	0	0	0	1	1	0	0.5	0.5	0	1	-1	1	0	0	2	-1	-1
0	1	1	0	1	0	0	1	0	0.5	0.5	0.5	0.5	-1	1	1	-1	2	-2	-2
0	1	1	0	0	1	1	0	0	0.5	0.5	0.5	0.5	-1	1	-1	1	2	0	0
0	1	1	0	1	1	0	0	0	0.5	0.5	1	0	-1	1	0	0	2	-1	-1
0	1	1	0	1	1	1	1	0	0.5	0.5	1	1	-1	1	0	0	3	-2	-2
0	1	0	1	1	0	1	0	0	0.5	0.5	0.5	0.5	-1	-1	1	1	2	2	2
0	1	1	1	0	0	1	0	0	0.5	1	0	0.5	-1	0	0	1	2	1	1
0	1	1	1	1	0	0	0	0	0.5	1	0.5	0	-1	0	1	0	2	0	0
0	1	1	1	1	0	1	1	0	0.5	1	0.5	1	-1	0	1	0	3	-1	-1
0	1	1	1	1	1	1	0	0	0.5	1	1	0.5	-1	0	0	1	3	0	0
1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	-1	-1
1	1	0	0	0	0	1	1	0	1	0	0	1	0	0	0	0	2	-2	-2
1	1	0	0	1	0	0	1	0	1	0	0.5	0.5	0	0	1	-1	2	-3	-3
1	1	0	0	0	1	1	0	0	1	0	0.5	0.5	0	0	-1	1	2	-1	-1
1	1	0	0	1	1	0	0	0	1	0	1	0	0	0	0	0	2	-2	-2
1	1	0	0	1	1	1	1	0	1	0	1	1	0	0	0	0	3	-3	-3
1	1	1	0	0	0	0	1	0	1	0.5	0	0.5	0	1	0	-1	2	-4	-4
1	1	1	0	0	1	0	0	0	1	0.5	0.5	0	0	1	-1	0	2	-3	-3
1	1	1	0	0	1	1	1	0	1	0.5	0.5	1	0	1	-1	0	3	-4	-4
1	1	1	0	1	1	0	1	0	1	0.5	1	0.5	0	1	0	-1	3	-5	-5
1	1	0	1	0	0	1	0	0	1	0.5	0	0.5	0	-1	0	1	2	0	0
1	1	0	1	1	0	0	0	0	1	0.5	0.5	0	0	-1	1	0	2	-1	-1
1	1	0	1	1	0	1	1	0	1	0.5	0.5	1	0	-1	1	0	3	-2	-2
1	1	0	1	1	1	1	0	0	1	0.5	1	0.5	0	-1	0	1	3	-1	-1
1	1	1	1	0	0	0	0	0	1	1	0	0	0	0	0	0	2	-2	-2
1	1	1	1	0	0	1	1	0	1	1	0	1	0	0	0	0	3	-3	-3
1	1	1	1	1	0	0	1	0	1	1	0.5	0.5	0	0	1	-1	3	-4	-4
1	1	1	1	0	1	1	0	0	1	1	0.5	0.5	0	0	-1	1	3	-2	-2
1	1	1	1	1	1	0	0	0	1	1	1	0	0	0	0	0	3	-3	-3
1	1	1	1	1	1	1	1	0	1	1	1	1	0	0	0	0	4	-4	-4
0	0	0	0	0	0	0	1	-1	0	0	0	0.5	0	0	0	-1	0.5	-2	-4
0	0	0	0	0	1	0	0	-1	0	0	0.5	0	0	0	-1	0	0.5	-1	-3
0	0	0	0	0	1	1	1	-1	0	0	0.5	1	0	0	-1	0	1.5	-2	-4
0	0	0	0	1	1	0	1	-1	0	0	1	0.5	0	0	0	-1	1.5	-3	-5
0	0	1	0	0	1	0	1	-1	0	0.5	0.5	0.5	0	1	-1	-1	1.5	-4	-6
0	0	0	1	0	0	0	0	-1	0	0.5	0	0	0	-1	0	0	0.5	0	-2
0	0	0	1	0	0	1	1	-1	0	0.5	0	1	0	-1	0	0	1.5	-1	-3
0	0	0	1	1	0	0	1	-1	0	0.5	0.5	0.5	0	-1	1	-1	1.5	-2	-4
0	0	0	1	0	1	1	0	-1	0	0.5	0.5	0.5	0	-1	-1	1	1.5	0	-2
0	0	0	1	1	1	0	0	-1	0	0.5	1	0	0	-1	0	0	1.5	-1	-3
0	0	0	1	1	1	1	1	-1	0	0.5	1	1	0	-1	0	0	2.5	-2	-4
0	0	1	1	0	0	0	1	-1	0	1	0	0.5	0	0	0	-1	1.5	-3	-5
0	0	1	1	0	1	0	0	-1	0	1	0.5	0	0	0	-1	0	1.5	-2	-4
0	0	1	1	0	1	1	1	-1	0	1	0.5	1	0	0	-1	0	2.5	-3	-5
0	0	1	1	1	1	0	1	-1	0	1	1	0.5	0	0	0	-1	2.5	-4	-6
1	0	0	0	0	1	0	1	-1	0.5	0	0.5	0.5	1	0	-1	-1	1.5	-5	-7
1	0	0	1	0	0	0	1	-1	0.5	0.5	0	0.5	1	-1	0	-1	1.5	-4	-6
1	0	0	1	0	1	0	0	-1	0.5	0.5	0.5	0	1	-1	-1	0	1.5	-3	-5
1	0	0	1	0	1	1	1	-1	0.5	0.5	0.5	1	1	-1	-1	0	2.5	-4	-6
1	0	0	1	1	1	0	1	-1	0.5	0.5	1	0.5	1	-1	0	-1	2.5	-5	-7
1	0	1	1	0	1	0	1	-1	0.5	1	0.5	0.5	1	0	-1	-1	2.5	-6	-8
0	1	0	0	0	0	0	0	-1	0.5	0	0	0	-1	0	0	0	0.5	1	-1
0	1	0	0	0	0	1	1	-1	0.5	0	0	1	-1	0	0	0	1.5	0	-2
0	1	0	0	1	0	0	1	-1	0.5	0	0.5	0.5	-1	0	1	-1	1.5	-1	-3
0	1	0	0	0	1	1	0	-1	0.5	0	0.5	0.5	-1	0	-1	1	1.5	1	-1
0	1	0	0	1	1	0	0	-1	0.5	0	1	0	-1	0	0	0	1.5	0	-2
0	1	0	0	1	1	1	1	-1	0.5	0	1	1	-1	0	0	0	2.5	-1	-3
0	1	1	0	0	0	0	1	-1	0.5	0.5	0	0.5	-1	1	0	-1	1.5	-2	-4
0	1	1	0	0	1	0	0	-1	0.5	0.5	0.5	0	-1	1	-1	0	1.5	-1	-3
0	1	1	0	0	1	1	1	-1	0.5	0.5	0.5	1	-1	1	-1	0	2.5	-2	-4
0	1	1	0	1	1	0	1	-1	0.5	0.5	1	0.5	-1	1	0	-1	2.5	-3	-5
0	1	0	1	0	0	1	0	-1	0.5	0.5	0	0.5	-1	-1	0	1	1.5	2	0
0	1	0	1	1	0	0	0	-1	0.5	0.5	0.5	0	-1	-1	1	0	1.5	1	-1
0	1	0	1	1	0	1	1	-1	0.5	0.5	0.5	1	-1	-1	1	0	2.5	0	-2
0	1	0	1	1	1	1	0	-1	0.5	0.5	1	0.5	-1	-1	0	1	2.5	1	-1
0	1	1	1	0	0	0	0	-1	0.5	1	0	0	-1	0	0	0	1.5	0	-2

9-level CHB switching states continued:

Sa1	Sa3	Sb1	Sb3	Sc1	Sc3	Sd1	Sd3	Output Voltage	Vcm1	Vcm2	Vcm3	Vcm4	Vdm1	Vdm2	Vdm3	Vdm4	VcmTotal	Vnto(SYM)	Vnto(ASYM)
0	1	1	1	0	0	1	1	-1	0.5	1	0	1	-1	0	0	0	2.5	-1	-3
0	1	1	1	1	0	0	1	-1	0.5	1	0.5	0.5	-1	0	1	-1	2.5	-2	-4
0	1	1	1	0	1	1	0	-1	0.5	1	0.5	0.5	-1	0	-1	1	2.5	0	-2
0	1	1	1	1	1	0	0	-1	0.5	1	1	0	-1	0	0	0	2.5	-1	-3
0	1	1	1	1	1	1	1	-1	0.5	1	1	1	-1	0	0	0	3.5	-2	-4
1	1	0	0	0	0	0	1	-1	1	0	0	0.5	0	0	0	-1	1.5	-3	-5
1	1	0	0	0	1	0	0	-1	1	0	0.5	0	0	0	-1	0	1.5	-2	-4
1	1	0	0	0	1	1	1	-1	1	0	0.5	1	0	0	-1	0	2.5	-3	-5
1	1	0	0	1	1	0	1	-1	1	0	1	0.5	0	0	0	-1	2.5	-4	-6
1	1	1	0	0	1	0	1	-1	1	0.5	0.5	0.5	0	1	-1	-1	2.5	-5	-7
1	1	0	1	0	0	0	0	-1	1	0.5	0	0	0	-1	0	0	1.5	-1	-3
1	1	0	1	0	0	1	1	-1	1	0.5	0	1	0	-1	0	0	2.5	-2	-4
1	1	0	1	1	0	0	1	-1	1	0.5	0.5	0.5	0	-1	1	-1	2.5	-3	-5
1	1	0	1	0	1	1	0	-1	1	0.5	0.5	0.5	0	-1	-1	1	2.5	-1	-3
1	1	0	1	1	1	0	0	-1	1	0.5	1	0	0	-1	0	0	2.5	-2	-4
1	1	0	1	1	1	1	1	-1	1	0.5	1	1	0	-1	0	0	3.5	-3	-5
1	1	1	1	0	0	0	1	-1	1	1	0	0.5	0	0	0	-1	2.5	-4	-6
1	1	1	1	0	1	0	0	-1	1	1	0.5	0	0	0	-1	0	2.5	-3	-5
1	1	1	1	0	1	1	1	-1	1	1	0.5	1	0	0	-1	0	3.5	-4	-6
1	1	1	1	1	1	0	1	-1	1	1	1	0.5	0	0	0	-1	3.5	-5	-7
0	0	0	0	0	1	0	1	-2	0	0	0.5	0.5	0	0	-1	-1	1	-3	-7
0	0	0	1	0	0	0	1	-2	0	0.5	0	0.5	0	-1	0	-1	1	-2	-6
0	0	0	1	0	1	0	0	-2	0	0.5	0.5	0	0	-1	-1	0	1	-1	-5
0	0	0	1	0	1	1	1	-2	0	0.5	0.5	1	0	-1	-1	0	2	-2	-6
0	0	0	1	1	1	0	1	-2	0	0.5	1	0.5	0	-1	0	-1	2	-3	-7
0	0	1	1	0	1	0	1	-2	0	1	0.5	0.5	0	0	-1	-1	2	-4	-8
1	0	0	1	0	1	0	1	-2	0.5	0.5	0.5	0.5	1	-1	-1	-1	2	-5	-9
0	1	0	0	0	0	0	1	-2	0.5	0	0	0.5	-1	0	0	-1	1	-1	-5
0	1	0	0	0	1	0	0	-2	0.5	0	0.5	0	-1	0	-1	0	1	0	-4
0	1	0	0	0	1	1	1	-2	0.5	0	0.5	1	-1	0	-1	0	2	-1	-5
0	1	0	0	1	1	0	1	-2	0.5	0	1	0.5	-1	0	0	-1	2	-2	-6
0	1	1	0	0	1	0	1	-2	0.5	0.5	0.5	0.5	-1	1	-1	-1	2	-3	-7
0	1	0	1	0	0	0	0	-2	0.5	0.5	0	0	-1	-1	0	0	1	1	-3
0	1	0	1	0	0	1	1	-2	0.5	0.5	0	1	-1	-1	0	0	2	0	-4
0	1	0	1	1	0	0	1	-2	0.5	0.5	0.5	0.5	-1	-1	1	-1	2	-1	-5
0	1	0	1	0	1	1	0	-2	0.5	0.5	0.5	0.5	-1	-1	-1	1	2	1	-3
0	1	0	1	1	1	0	0	-2	0.5	0.5	1	0	-1	-1	0	0	2	0	-4
0	1	0	1	1	1	1	1	-2	0.5	0.5	1	1	-1	-1	0	0	3	-1	-5
0	1	1	1	0	0	0	1	-2	0.5	1	0	0.5	-1	0	0	-1	2	-2	-6
0	1	1	1	0	1	0	0	-2	0.5	1	0.5	0	-1	0	-1	0	2	-1	-5
0	1	1	1	0	1	1	1	-2	0.5	1	0.5	1	-1	0	-1	0	3	-2	-6
0	1	1	1	1	1	0	1	-2	0.5	1	1	0.5	-1	0	0	-1	3	-3	-7
1	1	0	0	0	1	0	1	-2	1	0	0.5	0.5	0	0	-1	-1	2	-4	-8
1	1	0	1	0	0	0	1	-2	1	0.5	0	0.5	0	-1	0	-1	2	-3	-7
1	1	0	1	0	1	0	0	-2	1	0.5	0.5	0	0	-1	-1	0	2	-2	-6
1	1	0	1	0	1	1	1	-2	1	0.5	0.5	1	0	-1	-1	0	3	-3	-7
1	1	0	1	1	1	0	1	-2	1	0.5	1	0.5	0	-1	0	-1	3	-4	-8
1	1	1	1	0	1	0	1	-2	1	1	0.5	0.5	0	0	-1	-1	3	-5	-9
0	0	0	1	0	1	0	1	-3	0	0.5	0.5	0.5	0	-1	-1	-1	1.5	-3	-9
0	1	0	0	0	1	0	1	-3	0.5	0	0.5	0.5	-1	0	-1	-1	1.5	-2	-8
0	1	0	1	0	0	0	1	-3	0.5	0.5	0	0.5	-1	-1	0	-1	1.5	-1	-7
0	1	0	1	0	1	0	0	-3	0.5	0.5	0.5	0	-1	-1	-1	0	1.5	0	-6
0	1	0	1	0	1	1	1	-3	0.5	0.5	0.5	1	-1	-1	-1	0	2.5	-1	-7
0	1	0	1	1	1	0	1	-3	0.5	0.5	1	0.5	-1	-1	0	-1	2.5	-2	-8
0	1	1	1	0	1	0	1	-3	0.5	1	0.5	0.5	-1	0	-1	-1	2.5	-3	-9
1	1	0	1	0	1	0	1	-3	1	0.5	0.5	0.5	0	-1	-1	-1	2.5	-4	-10
0	1	0	1	0	1	0	1	-4	0.5	0.5	0.5	0.5	-1	-1	-1	-1	2	-2	-10

Appendix B – Clarke and Park Transformations

Clarke Transformation for single-phase application:

$$\begin{bmatrix} X_\alpha \\ X_\beta \end{bmatrix} = \begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} X_a \\ X_b \\ X_c \end{bmatrix}$$

Inverse Clarke Transformation for single-phase application:

$$\begin{bmatrix} X_a \\ X_b \\ X_c \end{bmatrix} = \begin{bmatrix} \frac{2}{3} & 0 \\ \frac{-1}{3} & \frac{\sqrt{3}}{3} \\ \frac{-1}{3} & \frac{-\sqrt{3}}{3} \end{bmatrix} \begin{bmatrix} X_\alpha \\ X_\beta \end{bmatrix}$$

Park Transformation for single-phase application:

$$\begin{bmatrix} X_d \\ X_q \end{bmatrix} = \begin{bmatrix} cos(\omega t) & sin(\omega t) \\ -sin(\omega t) & cos(\omega t) \end{bmatrix} \begin{bmatrix} X_\alpha \\ X_\beta \end{bmatrix}$$

Inverse Park Transformation for single-phase application:

$$\begin{bmatrix} X_\alpha \\ X_\beta \end{bmatrix} = \begin{bmatrix} cos(\omega t) & -sin(\omega t) \\ sin(\omega t) & cos(\omega t) \end{bmatrix} \begin{bmatrix} X_d \\ X_q \end{bmatrix}$$

Appendix C – Ziegler-Nichols Method

Controller Type	K_p	τ_i	τ_d
P	0.5 K_u	-	-
PI	0.45 K_u	0.85 T_u	-
PD	0.8 K_u	-	0.125 T_u
PID	0.6 K_u	0.5 T_u	0.125 T_u

Appendix D – Common Mode Voltage Derivations

5-level Symmetrical Inductance Circuit Derivation:

$$eq1 := \frac{Vxo_1 - Vcm_1}{Zpv} + \frac{Vxo_1 + 0.5\,Vdm_1 - V_g}{Z_L} - i_1 = 0$$

$$eq1 := \frac{Vxo_1 - Vcm_1}{Zpv} + \frac{Vxo_1 + 0.5\,Vdm_1 - V_g}{Z_L} - i_1 = 0 \quad (1)$$

$$eq2 := \frac{Vxo_2 - Vcm_2}{Zpv} + \frac{Vxo_2 - 0.5\,Vdm_2}{Z_L} + i_1 = 0$$

$$eq2 := \frac{Vxo_2 - Vcm_2}{Zpv} + \frac{Vxo_2 - 0.5\,Vdm_2}{Z_L} + i_1 = 0 \quad (2)$$

$$isolate(eq1,\ i_1);$$

$$i_1 = \frac{Vxo_1 - Vcm_1}{Zpv} + \frac{Vxo_1 + 0.5\,Vdm_1 - V_g}{Z_L} \quad (3)$$

$$isolate(eq2,\ i_1);$$

$$i_1 = -\frac{Vxo_2 - Vcm_2}{Zpv} - \frac{Vxo_2 - 0.5\,Vdm_2}{Z_L} \quad (4)$$

$$algsubs\left(i_1 = \frac{Vxo_1 - Vcm_1}{Zpv} + \frac{Vxo_1 + 0.5\,Vdm_1 - V_g}{Z_L},\ i_1 = -\frac{Vxo_2 - Vcm_2}{Zpv} - \frac{Vxo_2 - 0.5\,Vdm_2}{Z_L}\right)$$

$$-\frac{Z_L\,Vcm_1 - Z_L\,Vxo_1 - Zpv\,Vxo_1 - 0.5\,Zpv\,Vdm_1 + Zpv\,V_g}{Zpv\,Z_L} = -\frac{Vxo_2 - Vcm_2}{Zpv} - \frac{Vxo_2 - 0.5\,Vdm_2}{Z_L} \quad (5)$$

assign to a name →

$$eq3 \quad (6)$$

$$eq4 := Vxo_1 - Vxo_2 = 0.5\cdot(Vdm_1 + Vdm_2)$$

$$eq4 := Vxo_1 - Vxo_2 = 0.5\,Vdm_1 + 0.5\,Vdm_2 \quad (7)$$

$$isolate(eq4,\ Vxo_1);$$

$$Vxo_1 = 0.5\,Vdm_1 + 0.5\,Vdm_2 + Vxo_2 \quad (8)$$

$$isolate(eq4,\ Vxo_2);$$

$$Vxo_2 = -0.5\,Vdm_1 - 0.5\,Vdm_2 + Vxo_1 \quad (9)$$

$$subs(Vxo_1 = 0.5\,Vdm_1 + 0.5\,Vdm_2 + Vxo_2,\ eq3)$$

$$-\frac{1}{Zpv\,Z_L}\left(Z_L\,Vcm_1 - Z_L\left(0.5\,Vdm_1 + 0.5\,Vdm_2 + Vxo_2\right) - Zpv\left(0.5\,Vdm_1 + 0.5\,Vdm_2 + Vxo_2\right) - 0.5\,Zpv\,Vdm_1 + Zpv\,V_g\right) = -\frac{Vxo_2 - Vcm_2}{Zpv} - \frac{Vxo_2 - 0.5\,Vdm_2}{Z_L} \quad (10)$$

simplify symbolic →

$$\frac{\left(-1.\,Vcm_1 + 0.5\,Vdm_1 + 0.5\,Vdm_2 + Vxo_2\right)Z_L + \left(Vdm_1 + 0.5\,Vdm_2 + Vxo_2 - 1.\,V_g\right)Zpv}{Zpv\,Z_L} \quad (11)$$

$$= \frac{(Vcm_2 - 1.\ Vxo_2)\ Z_L + (-1.\ Vxo_2 + 0.5\ Vdm_2)\ Zpv}{Zpv\ Z_L}$$

assign to a name →

$$eq5 \tag{12}$$

$isolate(\ eq5,\ Vxo_2)$;

$$Vxo_2 = \frac{Z_L\ Vcm_1 - 0.5\ Z_L\ Vdm_1 - 0.5\ Z_L\ Vdm_2 - Zpv\ Vdm_1 + Zpv\ V_g + Z_L\ Vcm_2}{2.\ Z_L + 2.\ Zpv} \tag{13}$$

$subs(Vxo_2 = -0.5\ Vdm_1 - 0.5\ Vdm_2 + Vxo_1,\ eq5)$

$$\frac{(Vxo_1 - 1.\ Vcm_1)\ Z_L + (0.5\ Vdm_1 + Vxo_1 - 1.\ V_g)\ Zpv}{Zpv\ Z_L} = \frac{(Vcm_2 + 0.5\ Vdm_1 + 0.5\ Vdm_2 - 1.\ Vxo_1)\ Z_L + (0.5\ Vdm_1 + 1.0\ Vdm_2 - 1.\ Vxo_1)\ Zpv}{Zpv\ Z_L} \tag{14}$$

assign to a name →

$$eq6 \tag{15}$$

$isolate(\ eq6,\ Vxo_1)$;

$$Vxo_1 = \frac{Z_L\ Vcm_1 + Zpv\ V_g + Z_L\ Vcm_2 + 0.5\ Z_L\ Vdm_1 + 0.5\ Z_L\ Vdm_2 + Zpv\ Vdm_2}{2.\ Z_L + 2.\ Zpv} \tag{16}$$

$eq7 := Vxo_2 - Vcm_2 = Vno_2$

$$eq7 := Vxo_2 - Vcm_2 = Vno_2 \tag{17}$$

$isolate(\ eq7,\ Vno_2)$;

$$Vno_2 = Vxo_2 - Vcm_2 \tag{18}$$

$$subs\left(Vxo_2 = \frac{Z_L\ Vcm_1 - 0.5\ Z_L\ Vdm_1 - 0.5\ Z_L\ Vdm_2 - Zpv\ Vdm_1 + Zpv\ V_g + Z_L\ Vcm_2}{2.\ Z_L + 2.\ Zpv},\ eq7\right)$$

$$\frac{Z_L\ Vcm_1 - 0.5\ Z_L\ Vdm_1 - 0.5\ Z_L\ Vdm_2 - Zpv\ Vdm_1 + Zpv\ V_g + Z_L\ Vcm_2}{2.\ Z_L + 2.\ Zpv} - Vcm_2 = Vno_2 \tag{19}$$

assign to a name →

$$eq8 \tag{20}$$

$isolate(\ eq8,\ Vno_2)$;

$$Vno_2 = \frac{Z_L\ Vcm_1 - 0.5\ Z_L\ Vdm_1 - 0.5\ Z_L\ Vdm_2 - Zpv\ Vdm_1 + Zpv\ V_g + Z_L\ Vcm_2}{2.\ Z_L + 2.\ Zpv} - Vcm_2 \tag{21}$$

$eq9 := Vxo_1 - Vcm_1 = Vno_1$

$$eq9 := Vxo_1 - Vcm_1 = Vno_1 \tag{22}$$

$isolate(\ eq9,\ Vno_1)$;

$$Vno_1 = Vxo_1 - Vcm_1 \tag{23}$$

$$subs\left(Vxo_1 = \frac{Z_L\ Vcm_1 + Zpv\ V_g + Z_L\ Vcm_2 + 0.5\ Z_L\ Vdm_1 + 0.5\ Z_L\ Vdm_2 + Zpv\ Vdm_2}{2.\ Z_L + 2.\ Zpv},\ eq9\right)$$

$$\frac{Z_L\ Vcm_1 + Zpv\ V_g + Z_L\ Vcm_2 + 0.5\ Z_L\ Vdm_1 + 0.5\ Z_L\ Vdm_2 + Zpv\ Vdm_2}{2.\ Z_L + 2.\ Zpv} - Vcm_1 = Vno_1 \tag{24}$$

$\xrightarrow{\text{assign to a name}}$

$$eq10 \tag{25}$$

$isolate(\ eq10,\ Vno_1\ );$

$$Vno_1 = \frac{Z_L\ Vcm_1 + Zpv\ V_g + Z_L\ Vcm_2 + 0.5\ Z_L\ Vdm_1 + 0.5\ Z_L\ Vdm_2 + Zpv\ Vdm_2}{2.\ Z_L + 2.\ Zpv} - Vcm_1 \tag{26}$$

$$\frac{Z_L\ Vcm_1 + Zpv\ V_g + Z_L\ Vcm_2 + 0.5\ Z_L\ Vdm_1 + 0.5\ Z_L\ Vdm_2 + Zpv\ Vdm_2}{2.\ Z_L + 2.\ Zpv} - Vcm_1$$
$$+ \frac{Z_L\ Vcm_1 - 0.5\ Z_L\ Vdm_1 - 0.5\ Z_L\ Vdm_2 - Zpv\ Vdm_1 + Zpv\ V_g + Z_L\ Vcm_2}{2.\ Z_L + 2.\ Zpv} - Vcm_2$$

$$\frac{Z_L\ Vcm_1 + Zpv\ V_g + Z_L\ Vcm_2 + 0.5\ Z_L\ Vdm_1 + 0.5\ Z_L\ Vdm_2 + Zpv\ Vdm_2}{2.\ Z_L + 2.\ Zpv} - Vcm_1 \tag{27}$$
$$+ \frac{Z_L\ Vcm_1 - 0.5\ Z_L\ Vdm_1 - 0.5\ Z_L\ Vdm_2 - Zpv\ Vdm_1 + Zpv\ V_g + Z_L\ Vcm_2}{2.\ Z_L + 2.\ Zpv} - Vcm_2$$

$\overset{\text{simplify}}{=}$

$$\frac{(2.\ V_g + Vdm_2 - 2.\ Vcm_1 - Vdm_1 - 2.\ Vcm_2)\ Zpv}{2.\ Z_L + 2.\ Zpv} \tag{28}$$

$\xrightarrow{\text{limit}}$

$$V_g + 0.5000000000\ Vdm_2 - 1.\ Vcm_1 - 0.5000000000\ Vdm_1 - 1.\ Vcm_2 \tag{29}$$

7-level Symmetrical Inductance Circuit Derivation:

$$eq1 := \frac{Vxo_1 - Vcm_1}{Zpv} + \frac{Vxo_1 + 0.5\ Vdm_1 - V_g}{Z_L} - i_1 = 0$$

$$eq1 := \frac{Vxo_1 - Vcm_1}{Zpv} + \frac{Vxo_1 + 0.5\ Vdm_1 - V_g}{Z_L} - i_1 = 0 \quad \textbf{(1)}$$

$$eq2 := \frac{Vxo_2 - Vcm_2}{Zpv} + i_1 - i_2 = 0$$

$$eq2 := \frac{Vxo_2 - Vcm_2}{Zpv} + i_1 - i_2 = 0 \quad \textbf{(2)}$$

$$eq3 := \frac{Vxo_3 - Vcm_3}{Zpv} + i_2 + \frac{Vxo_3 - 0.5\ Vdm_3}{Z_L} = 0$$

$$eq3 := \frac{Vxo_3 - Vcm_3}{Zpv} + i_2 + \frac{Vxo_3 - 0.5\ Vdm_3}{Z_L} = 0 \quad \textbf{(3)}$$

$$isolate(eq1,\ i_1);$$

$$i_1 = \frac{Vxo_1 - Vcm_1}{Zpv} + \frac{Vxo_1 + 0.5\ Vdm_1 - V_g}{Z_L} \quad \textbf{(4)}$$

$$isolate(eq2,\ i_1);$$

$$i_1 = -\frac{Vxo_2 - Vcm_2}{Zpv} + i_2 \quad \textbf{(5)}$$

$$isolate(eq3,\ i_2);$$

$$i_2 = -\frac{Vxo_3 - Vcm_3}{Zpv} - \frac{Vxo_3 - 0.5\ Vdm_3}{Z_L} \quad \textbf{(6)}$$

$$algsubs\left(i_1 = \frac{Vxo_1 - Vcm_1}{Zpv} + \frac{Vxo_1 + 0.5\ Vdm_1 - V_g}{Z_L}, i_1 = -\frac{Vxo_2 - Vcm_2}{Zpv} + i_2\right)$$

$$-\frac{Z_L\ Vcm_1 - Z_L\ Vxo_1 - Zpv\ Vxo_1 - 0.5\ Zpv\ Vdm_1 + Zpv\ V_g}{Zpv\ Z_L} = -\frac{Vxo_2 - Vcm_2}{Zpv} + i_2 \quad \textbf{(7)}$$

assign to a name →

$$eq5 \quad \textbf{(8)}$$

$$isolate(eq5, i_2);$$

$$i_2 = -\frac{Z_L\ Vcm_1 - Z_L\ Vxo_1 - Zpv\ Vxo_1 - 0.5\ Zpv\ Vdm_1 + Zpv\ V_g}{Zpv\ Z_L} + \frac{Vxo_2 - Vcm_2}{Zpv} \quad \textbf{(9)}$$

$$algsubs\left(i_2 = -\frac{Z_L\ Vcm_1 - Z_L\ Vxo_1 - Zpv\ Vxo_1 - 0.5\ Zpv\ Vdm_1 + Zpv\ V_g}{Zpv\ Z_L} + \frac{Vxo_2 - Vcm_2}{Zpv}, i_2 = -\frac{Vxo_3 - Vcm_3}{Zpv} - \frac{Vxo_3 - 0.5\ Vdm_3}{Z_L}\right)$$

$$-\frac{Z_L\ Vcm_1 - Z_L\ Vxo_1 - Zpv\ Vxo_1 - 0.5\ Zpv\ Vdm_1 + Zpv\ V_g + Z_L\ Vcm_2 - Z_L\ Vxo_2}{Zpv\ Z_L} = \quad \textbf{(10)}$$

$$-\frac{Vxo_3 - Vcm_3}{Zpv} - \frac{Vxo_3 - 0.5\ Vdm_3}{Z_L}$$

assign to a name →

$$eq6 \tag{11}$$

$isolate(\ eq6, Vxo_1);$

$$Vxo_1 = \frac{1}{-Zpv - Z_L}\left(-\left(-\frac{Vxo_3 - Vcm_3}{Zpv} - \frac{Vxo_3 - 0.5\ Vdm_3}{Z_L}\right) Zpv\ Z_L - Z_L\ Vcm_1 \right. \tag{12}$$

$$\left. + 0.5\ Zpv\ Vdm_1 - Zpv\ V_g - Z_L\ Vcm_2 + Z_L\ Vxo_2\right)$$

$eq7 := Vxo_1 - Vxo_2 = 0.5 \cdot (Vdm_1 + Vdm_2)$

$$eq7 := Vxo_1 - Vxo_2 = 0.5\ Vdm_1 + 0.5\ Vdm_2 \tag{13}$$

$isolate(\ eq7, Vxo_1);$

$$Vxo_1 = 0.5\ Vdm_1 + 0.5\ Vdm_2 + Vxo_2 \tag{14}$$

$isolate(\ eq7, Vxo_2);$

$$Vxo_2 = -0.5\ Vdm_1 - 0.5\ Vdm_2 + Vxo_1 \tag{15}$$

$eq8 := Vxo_2 - Vxo_3 = 0.5 \cdot (Vdm_2 + Vdm_3)$

$$eq8 := Vxo_2 - Vxo_3 = 0.5\ Vdm_2 + 0.5\ Vdm_3 \tag{16}$$

$isolate(\ eq8, Vxo_2);$

$$Vxo_2 = 0.5\ Vdm_2 + 0.5\ Vdm_3 + Vxo_3 \tag{17}$$

$isolate(\ eq8, Vxo_3);$

$$Vxo_3 = -0.5\ Vdm_2 - 0.5\ Vdm_3 + Vxo_2 \tag{18}$$

$subs(Vxo_1 = 0.5\ Vdm_1 + 0.5\ Vdm_2 + Vxo_2,\ eq6)$

$$-\frac{1}{Zpv\ Z_L}\left(Z_L\ Vcm_1 - Z_L\left(0.5\ Vdm_1 + 0.5\ Vdm_2 + Vxo_2\right) - Zpv\left(0.5\ Vdm_1 + 0.5\ Vdm_2 + Vxo_2\right)\right. \tag{19}$$

$$\left. - 0.5\ Zpv\ Vdm_1 + Zpv\ V_g + Z_L\ Vcm_2 - Z_L\ Vxo_2\right) = -\frac{Vxo_3 - Vcm_3}{Zpv} - \frac{Vxo_3 - 0.5\ Vdm_3}{Z_L}$$

assign to a name →

$$eq9 \tag{20}$$

$isolate(\ eq9, Vxo_2);$

$$Vxo_2 = \frac{1}{-Zpv - 2\ Z_L}\left(-\left(-\frac{Vxo_3 - Vcm_3}{Zpv} - \frac{Vxo_3 - 0.5\ Vdm_3}{Z_L}\right) Zpv\ Z_L - Z_L\ Vcm_1 \right. \tag{21}$$

$$\left. + 1.0\ Zpv\ Vdm_1 - Zpv\ V_g - Z_L\ Vcm_2 + 0.5\ Z_L\ Vdm_1 + 0.5\ Z_L\ Vdm_2 + 0.5\ Zpv\ Vdm_2\right)$$

$subs(Vxo_2 = 0.5\ Vdm_2 + 0.5\ Vdm_3 + Vxo_3,\ eq9)$

$$-\frac{1}{Zpv\,Z_L}\left(Z_L\,Vcm_1-Z_L\left(0.5\,Vdm_1+1.0\,Vdm_2+0.5\,Vdm_3+Vxo_3\right)-Zpv\left(0.5\,Vdm_1+1.0\,Vdm_2+0.5\,Vdm_3+Vxo_3\right)-0.5\,Zpv\,Vdm_1+Zpv\,V_g+Z_L\,Vcm_2-Z_L\left(0.5\,Vdm_2+0.5\,Vdm_3+Vxo_3\right)\right)=-\frac{Vxo_3-Vcm_3}{Zpv}-\frac{Vxo_3-0.5\,Vdm_3}{Z_L} \tag{22}$$

assign to a name →

$$eq10 \tag{23}$$

$$isolate\left(eq10,\,Vxo_3\right); \tag{24}$$

$$Vxo_3=\frac{1}{2\,Zpv+3\,Z_L}\left(Z_L\,Vcm_1-0.5\,Z_L\,Vdm_1-1.5\,Z_L\,Vdm_2-Z_L\,Vdm_3-Zpv\,Vdm_1-Zpv\,Vdm_2+Zpv\,V_g+Z_L\,Vcm_2+Z_L\,Vcm_3\right)$$

$$subs\left(Vxo_3=-0.5\,Vdm_2-0.5\,Vdm_3+Vxo_2,\;eq10\right) \tag{25}$$

$$-\frac{1}{Zpv\,Z_L}\left(Z_L\,Vcm_1-Z_L\left(0.5\,Vdm_1+0.5\,Vdm_2+Vxo_2\right)-Zpv\left(0.5\,Vdm_1+0.5\,Vdm_2+Vxo_2\right)-0.5\,Zpv\,Vdm_1+Zpv\,V_g+Z_L\,Vcm_2-Z_L\,Vxo_2\right)=-\frac{-0.5\,Vdm_2-0.5\,Vdm_3+Vxo_2-Vcm_3}{Zpv}-\frac{-0.5\,Vdm_2-1.0\,Vdm_3+Vxo_2}{Z_L}$$

assign to a name →

$$eq12 \tag{26}$$

$$isolate\left(eq12,\,Vxo_2\right); \tag{27}$$

$$Vxo_2=\frac{1}{2\,Zpv+3\,Z_L}\left(Z_L\,Vcm_1-0.5\,Z_L\,Vdm_1-Zpv\,Vdm_1+Zpv\,V_g+Z_L\,Vcm_2+0.5\,Z_L\,Vdm_3+Z_L\,Vcm_3+Zpv\,Vdm_3\right)$$

$$subs\left(Vxo_2=-0.5\,Vdm_1-0.5\,Vdm_2+Vxo_1,\;eq12\right) \tag{28}$$

$$-\frac{1}{Zpv\,Z_L}\left(Z_L\,Vcm_1-Z_L\,Vxo_1-Zpv\,Vxo_1-0.5\,Zpv\,Vdm_1+Zpv\,V_g+Z_L\,Vcm_2-Z_L\left(-0.5\,Vdm_1-0.5\,Vdm_2+Vxo_1\right)\right)=-\frac{-1.0\,Vdm_2-0.5\,Vdm_3-0.5\,Vdm_1+Vxo_1-Vcm_3}{Zpv}-\frac{-1.0\,Vdm_2-1.0\,Vdm_3-0.5\,Vdm_1+Vxo_1}{Z_L}$$

assign to a name →

$$eq13 \tag{29}$$

$$isolate\left(eq13,\,Vxo_1\right); \tag{30}$$

$$Vxo_1=\frac{1}{2\,Zpv+3\,Z_L}\left(Zpv\,V_g+Z_L\,Vcm_1+Z_L\,Vcm_2+Z_L\,Vdm_1+1.5\,Z_L\,Vdm_2+0.5\,Z_L\,Vdm_3+Z_L\,Vcm_3+Zpv\,Vdm_2+Zpv\,Vdm_3\right)$$

$eq14 := Vxo_1 - Vcm_1 = Vno_1$

$$eq14 := Vxo_1 - Vcm_1 = Vno_1 \tag{31}$$

$isolate(eq14, Vno_1);$

$$Vno_1 = Vxo_1 - Vcm_1 \tag{32}$$

$eq15 := Vxo_2 - Vcm_2 = Vno_2$

$$eq15 := Vxo_2 - Vcm_2 = Vno_2 \tag{33}$$

$isolate(eq15, Vno_2);$

$$Vno_2 = Vxo_2 - Vcm_2 \tag{34}$$

$eq16 := Vxo_3 - Vcm_3 = Vno_3$

$$eq16 := Vxo_3 - Vcm_3 = Vno_3 \tag{35}$$

$isolate(eq16, Vno_3);$

$$Vno_3 = Vxo_3 - Vcm_3 \tag{36}$$

$$subs\left(Vxo_2 = \frac{Z_L\, Vcm_1 - 0.5\, Z_L\, Vdm_1 - Zpv\, Vdm_1 + Zpv\, V_g + Z_L\, Vcm_2 + 0.5\, Z_L\, Vdm_3 + Z_L\, Vcm_3 + Zpv\, Vdm_3}{2\, Zpv + 3\, Z_L},\ eq15\right)$$

$$\frac{Z_L\, Vcm_1 - 0.5\, Z_L\, Vdm_1 - Zpv\, Vdm_1 + Zpv\, V_g + Z_L\, Vcm_2 + 0.5\, Z_L\, Vdm_3 + Z_L\, Vcm_3 + Zpv\, Vdm_3}{2\, Zpv + 3\, Z_L} - Vcm_2 = Vno_2 \tag{37}$$

assign to a name →

$$eq17 \tag{38}$$

$isolate(eq17, Vno_2);$

$$Vno_2 = \frac{1}{2\, Zpv + 3\, Z_L}\left(Z_L\, Vcm_1 - 0.5\, Z_L\, Vdm_1 - Zpv\, Vdm_1 + Zpv\, V_g + Z_L\, Vcm_2 + 0.5\, Z_L\, Vdm_3 + Z_L\, Vcm_3 + Zpv\, Vdm_3\right) - Vcm_2 \tag{39}$$

$$subs\left(Vxo_1 = \frac{1}{2\, Zpv + 3\, Z_L}\left(Zpv\, V_g + Z_L\, Vcm_1 + Z_L\, Vcm_2 + Z_L\, Vdm_1 + 1.5\, Z_L\, Vdm_2 + 0.5\, Z_L\, Vdm_3 + Z_L\, Vcm_3 + Zpv\, Vdm_2 + Zpv\, Vdm_3\right),\ eq14\right)$$

$$\frac{1}{2\, Zpv + 3\, Z_L}\left(Zpv\, V_g + Z_L\, Vcm_1 + Z_L\, Vcm_2 + Z_L\, Vdm_1 + 1.5\, Z_L\, Vdm_2 + 0.5\, Z_L\, Vdm_3 + Z_L\, Vcm_3 + Zpv\, Vdm_2 + Zpv\, Vdm_3\right) - Vcm_1 = Vno_1 \tag{40}$$

assign to a name →

$$eq18 \tag{41}$$

$isolate(eq18, Vno_1);$

$$Vno_1 = \frac{1}{2\,Zpv + 3\,Z_L}\left(Zpv\,V_g + Z_L\,Vcm_1 + Z_L\,Vcm_2 + Z_L\,Vdm_1 + 1.5\,Z_L\,Vdm_2 + 0.5\,Z_L\,Vdm_3 + Z_L\,Vcm_3 + Zpv\,Vdm_2 + Zpv\,Vdm_3\right) - Vcm_1 \tag{42}$$

$$subs\left(Vxo_3 = \frac{1}{2\,Zpv + 3\,Z_L}\left(Z_L\,Vcm_1 - 0.5\,Z_L\,Vdm_1 - 1.5\,Z_L\,Vdm_2 - Z_L\,Vdm_3 - Zpv\,Vdm_1 - Zpv\,Vdm_2 + Zpv\,V_g + Z_L\,Vcm_2 + Z_L\,Vcm_3\right),\ eq16\right)$$

$$\frac{1}{2\,Zpv + 3\,Z_L}\left(Z_L\,Vcm_1 - 0.5\,Z_L\,Vdm_1 - 1.5\,Z_L\,Vdm_2 - Z_L\,Vdm_3 - Zpv\,Vdm_1 - Zpv\,Vdm_2 + Zpv\,V_g + Z_L\,Vcm_2 + Z_L\,Vcm_3\right) - Vcm_3 = Vno_3 \tag{43}$$

assign to a name →

$$eq19 \tag{44}$$

$simplify(isolate(eq18, Vno_1));$

$$Vno_1 = \frac{1}{2.\,Zpv + 3.\,Z_L}\left(\left(-2.\,Vcm_1 + Vcm_2 + Vdm_1 + 1.5\,Vdm_2 + 0.5\,Vdm_3 + Vcm_3\right)Z_L + \left(V_g + Vdm_2 + Vdm_3 - 2.\,Vcm_1\right)Zpv\right) \tag{45}$$

assign to a name →

$$eq20 \tag{46}$$

$simplify(isolate(eq17, Vno_2));$

$$Vno_2 = \frac{1}{2.\,Zpv + 3.\,Z_L}\left(\left(Vcm_1 - 0.5\,Vdm_1 - 2.\,Vcm_2 + 0.5\,Vdm_3 + Vcm_3\right)Z_L + \left(-1.\,Vdm_1 + V_g + Vdm_3 - 2.\,Vcm_2\right)Zpv\right) \tag{47}$$

assign to a name →

$$eq21 \tag{48}$$

$simplify(isolate(eq19, Vno_3));$

$$Vno_3 = \frac{1}{2.\,Zpv + 3.\,Z_L}\left(\left(Vcm_1 - 0.5\,Vdm_1 - 1.5\,Vdm_2 - 1.\,Vdm_3 + Vcm_2 - 2.\,Vcm_3\right)Z_L + \left(-1.\,Vdm_1 - 1.\,Vdm_2 + V_g - 2.\,Vcm_3\right)Zpv\right) \tag{49}$$

assign to a name →

$$eq22 \tag{50}$$

$eq23 := Vno_1 + Vno_2 + Vno_3$

$$eq23 := \frac{1}{2.\,Zpv + 3.\,Z_L}\left(\left(-2.\,Vcm_1 + Vcm_2 + Vdm_1 + 1.5\,Vdm_2 + 0.5\,Vdm_3 + Vcm_3\right)Z_L + \left(V_g + Vdm_2 + Vdm_3 - 2.\,Vcm_1\right)Zpv\right) + Vno_2 + Vno_3 \tag{51}$$

$$\frac{1}{2.\,Zpv+3.\,Z_L}\left(\left(-2.\,Vcm_1+Vcm_2+Vdm_1+1.5\,Vdm_2+0.5\,Vdm_3+Vcm_3\right)Z_L+\left(V_g+Vdm_2+Vdm_3-2.\,Vcm_1\right)Zpv\right)+\frac{1}{2.\,Zpv+3.\,Z_L}\left(\left(Vcm_1-0.5\,Vdm_1-2.\,Vcm_2+0.5\,Vdm_3+Vcm_3\right)Z_L+\left(-1.\,Vdm_1+V_g+Vdm_3-2.\,Vcm_2\right)Zpv\right)+\frac{1}{2.\,Zpv+3.\,Z_L}\left(\left(Vcm_1-0.5\,Vdm_1-1.5\,Vdm_2-1.\,Vdm_3+Vcm_2-2.\,Vcm_3\right)Z_L+\left(-1.\,Vdm_1-1.\,Vdm_2+V_g-2.\,Vcm_3\right)Zpv\right)$$

$$\frac{1}{2.\,Zpv+3.\,Z_L}\left(\left(-2.\,Vcm_1+Vcm_2+Vdm_1+1.5\,Vdm_2+0.5\,Vdm_3+Vcm_3\right)Z_L+\left(V_g+Vdm_2+Vdm_3-2.\,Vcm_1\right)Zpv\right)+\frac{1}{2.\,Zpv+3.\,Z_L}\left(\left(Vcm_1-0.5\,Vdm_1-2.\,Vcm_2+0.5\,Vdm_3+Vcm_3\right)Z_L+\left(-1.\,Vdm_1+V_g+Vdm_3-2.\,Vcm_2\right)Zpv\right)+\frac{1}{2.\,Zpv+3.\,Z_L}\left(\left(Vcm_1-0.5\,Vdm_1-1.5\,Vdm_2-1.\,Vdm_3+Vcm_2-2.\,Vcm_3\right)Z_L+\left(-1.\,Vdm_1-1.\,Vdm_2+V_g-2.\,Vcm_3\right)Zpv\right) \tag{52}$$

$$\xrightarrow{\text{simplify symbolic}}\quad\frac{\left(-2.\,Vcm_1+2.\,Vdm_3-2.\,Vdm_1+3.\,V_g-2.\,Vcm_2-2.\,Vcm_3\right)Zpv}{2.\,Zpv+3.\,Z_L} \tag{53}$$

$$\xrightarrow{\text{limit}}\quad-1.\,Vcm_1+Vdm_3-1.\,Vdm_1+1.500000000\,V_g-1.\,Vcm_2-1.\,Vcm_3 \tag{54}$$

9-level Symmetrical Inductance Circuit Derivation:

$$eq1 := \frac{Vxo_1 - Vcm_1}{Zpv} + \frac{Vxo_1 + 0.5\ Vdm_1 - V_g}{Z_L} - i_1 = 0$$

$$eq1 := \frac{Vxo_1 - Vcm_1}{Zpv} + \frac{Vxo_1 + 0.5\ Vdm_1 - V_g}{Z_L} - i_1 = 0 \quad (1)$$

$$eq2 := \frac{Vxo_2 - Vcm_2}{Zpv} + i_1 - i_2 = 0$$

$$eq2 := \frac{Vxo_2 - Vcm_2}{Zpv} + i_1 - i_2 = 0 \quad (2)$$

$$eq3 := \frac{Vxo_3 - Vcm_3}{Zpv} + i_2 - i_3 = 0$$

$$eq3 := \frac{Vxo_3 - Vcm_3}{Zpv} + i_2 - i_3 = 0 \quad (3)$$

$$eq4 := \frac{Vxo_4 - Vcm_4}{Zpv} + i_3 + \frac{Vxo_4 - 0.5\ Vdm_4}{Z_L} = 0$$

$$eq4 := \frac{Vxo_4 - Vcm_4}{Zpv} + i_3 + \frac{Vxo_4 - 0.5\ Vdm_4}{Z_L} = 0 \quad (4)$$

$isolate(eq1, i_1);$

$$i_1 = \frac{Vxo_1 - Vcm_1}{Zpv} + \frac{Vxo_1 + 0.5\ Vdm_1 - V_g}{Z_L} \quad (5)$$

$isolate(eq2, i_1);$

$$i_1 = -\frac{Vxo_2 - Vcm_2}{Zpv} + i_2 \quad (6)$$

$isolate(eq3, i_2);$

$$i_2 = -\frac{Vxo_3 - Vcm_3}{Zpv} + i_3 \quad (7)$$

$isolate(eq4, i_3);$

$$i_3 = -\frac{Vxo_4 - Vcm_4}{Zpv} - \frac{Vxo_4 - 0.5\ Vdm_4}{Z_L} \quad (8)$$

$$algsubs\left(i_1 = \frac{Vxo_1 - Vcm_1}{Zpv} + \frac{Vxo_1 + 0.5\ Vdm_1 - V_g}{Z_L}, i_1 = -\frac{Vxo_2 - Vcm_2}{Zpv} + i_2\right)$$

$$-\frac{Z_L\ Vcm_1 - Z_L\ Vxo_1 - Zpv\ Vxo_1 - 0.5\ Zpv\ Vdm_1 + Zpv\ V_g}{Zpv\ Z_L} = -\frac{Vxo_2 - Vcm_2}{Zpv} + i_2 \quad (9)$$

assign to a name →

$$eq5 \quad (10)$$

$isolate(eq5, i_2);$

$$i_2 = -\frac{Z_L\ Vcm_1 - Z_L\ Vxo_1 - Zpv\ Vxo_1 - 0.5\ Zpv\ Vdm_1 + Zpv\ V_g}{Zpv\ Z_L} + \frac{Vxo_2 - Vcm_2}{Zpv} \quad (11)$$

$$algsubs\left(i_2 = -\frac{Z_L\,Vcm_1 - Z_L\,Vxo_1 - Zpv\,Vxo_1 - 0.5\,Zpv\,Vdm_1 + Zpv\,V_g}{Zpv\,Z_L} + \frac{Vxo_2 - Vcm_2}{Zpv}, i_2 = -\frac{Vxo_3 - Vcm_3}{Zpv} + i_3\right)$$

$$-\frac{Z_L\,Vcm_1 - Z_L\,Vxo_1 - Zpv\,Vxo_1 - 0.5\,Zpv\,Vdm_1 + Zpv\,V_g + Z_L\,Vcm_2 - Z_L\,Vxo_2}{Zpv\,Z_L} = -\frac{Vxo_3 - Vcm_3}{Zpv} + i_3 \tag{12}$$

assign to a name

$$eq6 \tag{13}$$

$$isolate(eq6, i_3);$$

$$i_3 = -\frac{Z_L\,Vcm_1 - Z_L\,Vxo_1 - Zpv\,Vxo_1 - 0.5\,Zpv\,Vdm_1 + Zpv\,V_g + Z_L\,Vcm_2 - Z_L\,Vxo_2}{Zpv\,Z_L} + \frac{Vxo_3 - Vcm_3}{Zpv} \tag{14}$$

$$algsubs\left(i_3 = -\frac{Z_L\,Vcm_1 - Z_L\,Vxo_1 - Zpv\,Vxo_1 - 0.5\,Zpv\,Vdm_1 + Zpv\,V_g + Z_L\,Vcm_2 - Z_L\,Vxo_2}{Zpv\,Z_L} + \frac{Vxo_3 - Vcm_3}{Zpv}, i_3 = -\frac{Vxo_4 - Vcm_4}{Zpv} - \frac{Vxo_4 - 0.5\,Vdm_4}{Z_L}\right)$$

$$-\frac{1}{Zpv\,Z_L}\left(Z_L\,Vcm_1 - Z_L\,Vxo_1 - Zpv\,Vxo_1 - 0.5\,Zpv\,Vdm_1 + Zpv\,V_g + Z_L\,Vcm_2 - Z_L\,Vxo_2 + Z_L\,Vcm_3 - Z_L\,Vxo_3\right) = -\frac{Vxo_4 - Vcm_4}{Zpv} - \frac{Vxo_4 - 0.5\,Vdm_4}{Z_L} \tag{15}$$

assign to a name

$$eq7 \tag{16}$$

$$isolate(eq7, Vxo_1);$$

$$Vxo_1 = \frac{1}{-Zpv - Z_L}\left(-\left(-\frac{Vxo_4 - Vcm_4}{Zpv} - \frac{Vxo_4 - 0.5\,Vdm_4}{Z_L}\right)Zpv\,Z_L - Z_L\,Vcm_1 + 0.5\,Zpv\,Vdm_1 - Zpv\,V_g - Z_L\,Vcm_2 + Z_L\,Vxo_2 - Z_L\,Vcm_3 + Z_L\,Vxo_3\right) \tag{17}$$

$$eq8 := Vxo_1 - Vxo_2 = 0.5\cdot\left(Vdm_1 + Vdm_2\right)$$

$$eq8 := Vxo_1 - Vxo_2 = 0.5\,Vdm_1 + 0.5\,Vdm_2 \tag{18}$$

$$isolate(eq8, Vxo_1);$$

$$Vxo_1 = 0.5\,Vdm_1 + 0.5\,Vdm_2 + Vxo_2 \tag{19}$$

$$isolate(eq8, Vxo_2);$$

$$Vxo_2 = -0.5\,Vdm_1 - 0.5\,Vdm_2 + Vxo_1 \tag{20}$$

$eq9 := Vxo_2 - Vxo_3 = 0.5 \cdot (Vdm_2 + Vdm_3)$

$$eq9 := Vxo_2 - Vxo_3 = 0.5\ Vdm_2 + 0.5\ Vdm_3 \tag{21}$$

$isolate(eq9, Vxo_2);$

$$Vxo_2 = 0.5\ Vdm_2 + 0.5\ Vdm_3 + Vxo_3 \tag{22}$$

$isolate(eq9, Vxo_3);$

$$Vxo_3 = -0.5\ Vdm_2 - 0.5\ Vdm_3 + Vxo_2 \tag{23}$$

$eq10 := Vxo_3 - Vxo_4 = 0.5 \cdot (Vdm_3 + Vdm_4)$

$$eq10 := Vxo_3 - Vxo_4 = 0.5\ Vdm_3 + 0.5\ Vdm_4 \tag{24}$$

$isolate(eq10, Vxo_3);$

$$Vxo_3 = 0.5\ Vdm_3 + 0.5\ Vdm_4 + Vxo_4 \tag{25}$$

$isolate(eq10, Vxo_4);$

$$Vxo_4 = -0.5\ Vdm_3 - 0.5\ Vdm_4 + Vxo_3 \tag{26}$$

$subs(Vxo_1 = 0.5\ Vdm_1 + 0.5\ Vdm_2 + Vxo_2,\ eq7)$

$$-\frac{1}{Zpv\ Z_L}\left(Z_L\ Vcm_1 - Z_L\ (0.5\ Vdm_1 + 0.5\ Vdm_2 + Vxo_2) - Zpv\ (0.5\ Vdm_1 + 0.5\ Vdm_2 + Vxo_2)\right. \tag{27}$$

$$\left. - 0.5\ Zpv\ Vdm_1 + Zpv\ V_g + Z_L\ Vcm_2 - Z_L\ Vxo_2 + Z_L\ Vcm_3 - Z_L\ Vxo_3\right) = -\frac{Vxo_4 - Vcm_4}{Zpv}$$

$$- \frac{Vxo_4 - 0.5\ Vdm_4}{Z_L}$$

assign to a name →

$$eq11 \tag{28}$$

$isolate(eq11, Vxo_2);$

$$Vxo_2 = \frac{1}{-Zpv - 2\ Z_L}\left(-\left(-\frac{Vxo_4 - Vcm_4}{Zpv} - \frac{Vxo_4 - 0.5\ Vdm_4}{Z_L}\right) Zpv\ Z_L - Z_L\ Vcm_1\right. \tag{29}$$

$$+ 1.0\ Zpv\ Vdm_1 - Zpv\ V_g - Z_L\ Vcm_2 - Z_L\ Vcm_3 + Z_L\ Vxo_3 + 0.5\ Z_L\ Vdm_1 + 0.5\ Z_L\ Vdm_2$$

$$\left. + 0.5\ Zpv\ Vdm_2\right)$$

simplify =

$$Vxo_2 = \frac{1}{Zpv + 2.\ Z_L}\left(\left(Vcm_4 - 1.\ Vxo_4 + Vcm_1 + Vcm_2 + Vcm_3 - 1.\ Vxo_3 - 0.5\ Vdm_1\right.\right. \tag{30}$$

$$\left.\left. - 0.5\ Vdm_2\right) Z_L + \left(-1.\ Vxo_4 + 0.5\ Vdm_4 - 1.\ Vdm_1 + V_g - 0.5\ Vdm_2\right) Zpv\right)$$

$subs(Vxo_2 = 0.5\ Vdm_2 + 0.5\ Vdm_3 + Vxo_3,\ eq11)$

$$-\frac{1}{Zpv\ Z_L}\left(Z_L\ Vcm_1 - Z_L\ (0.5\ Vdm_1 + 1.0\ Vdm_2 + 0.5\ Vdm_3 + Vxo_3) - Zpv\ (0.5\ Vdm_1\right. \tag{31}$$

$$\left. + 1.0\ Vdm_2 + 0.5\ Vdm_3 + Vxo_3) - 0.5\ Zpv\ Vdm_1 + Zpv\ V_g + Z_L\ Vcm_2 - Z_L\ (0.5\ Vdm_2\right.$$

$$+ 0.5\ Vdm_3 + Vxo_3) + Z_L\ Vcm_3 - Z_L\ Vxo_3) = -\frac{Vxo_4 - Vcm_4}{Zpv} - \frac{Vxo_4 - 0.5\ Vdm_4}{Z_L}$$

assign to a name →

$$eq12 \tag{32}$$

$isolate(\ eq12, Vxo_3);$

$$Vxo_3 = \frac{1}{-Zpv - 3\ Z_L}\left(-\left(-\frac{Vxo_4 - Vcm_4}{Zpv} - \frac{Vxo_4 - 0.5\ Vdm_4}{Z_L}\right) Zpv\ Z_L - Z_L\ Vcm_1\right. \tag{33}$$

$$+ 1.0\ Zpv\ Vdm_1 - Zpv\ V_g - Z_L\ Vcm_2 - Z_L\ Vcm_3 + 0.5\ Z_L\ Vdm_1 + 1.5\ Z_L\ Vdm_2 + 1.0\ Z_L\ Vdm_3$$

$$\left. + 1.0\ Zpv\ Vdm_2 + 0.5\ Zpv\ Vdm_3\right)$$

simplify =

$$Vxo_3 = \frac{1}{Zpv + 3.\ Z_L}(\ (Vcm_4 - 1.\ Vxo_4 + Vcm_1 + Vcm_2 + Vcm_3 - 0.5\ Vdm_1 - 1.5\ Vdm_2 \tag{34}$$

$$- 1.\ Vdm_3)\ Z_L + (\ -1.\ Vxo_4 + 0.5\ Vdm_4 - 1.\ Vdm_1 + V_g - 1.\ Vdm_2 - 0.5\ Vdm_3)\ Zpv)$$

$subs(\ Vxo_3 = 0.5\ Vdm_3 + 0.5\ Vdm_4 + Vxo_4,\ eq12)$

$$-\frac{1}{Zpv\ Z_L}(Z_L\ Vcm_1 - Z_L\ (0.5\ Vdm_1 + 1.0\ Vdm_2 + 1.0\ Vdm_3 + 0.5\ Vdm_4 + Vxo_4) \tag{35}$$

$$- Zpv\ (0.5\ Vdm_1 + 1.0\ Vdm_2 + 1.0\ Vdm_3 + 0.5\ Vdm_4 + Vxo_4) - 0.5\ Zpv\ Vdm_1 + Zpv\ V_g$$

$$+ Z_L\ Vcm_2 - Z_L\ (0.5\ Vdm_2 + 1.0\ Vdm_3 + 0.5\ Vdm_4 + Vxo_4) + Z_L\ Vcm_3 - Z_L\ (0.5\ Vdm_3$$

$$+ 0.5\ Vdm_4 + Vxo_4)) = -\frac{Vxo_4 - Vcm_4}{Zpv} - \frac{Vxo_4 - 0.5\ Vdm_4}{Z_L}$$

assign to a name →

$$eq13 \tag{36}$$

$isolate(\ eq13, Vxo_4);$

$$Vxo_4 = \frac{1}{2\ Zpv + 4\ Z_L}(Z_L\ Vcm_1 - 0.5\ Z_L\ Vdm_1 - 1.5\ Z_L\ Vdm_2 - 2.5\ Z_L\ Vdm_3 - 1.5\ Z_L\ Vdm_4 \tag{37}$$

$$- Zpv\ Vdm_1 - Zpv\ Vdm_2 - Zpv\ Vdm_3 + Zpv\ V_g + Z_L\ Vcm_2 + Z_L\ Vcm_3 + Z_L\ Vcm_4)$$

simplify =

$$Vxo_4 = \frac{1}{2.\ Zpv + 4.\ Z_L}(\ (Vcm_1 - 0.5\ Vdm_1 - 1.5\ Vdm_2 - 2.5\ Vdm_3 - 1.5\ Vdm_4 + Vcm_2 + Vcm_3 \tag{38}$$

$$+ Vcm_4)\ Z_L + (\ -1.\ Vdm_1 - 1.\ Vdm_2 - 1.\ Vdm_3 + V_g)\ Zpv)$$

$subs(\ Vxo_4 = -0.5\ Vdm_3 - 0.5\ Vdm_4 + Vxo_3,\ eq13)$

$$-\frac{1}{Zpv\ Z_L}(Z_L\ Vcm_1 - Z_L\ (0.5\ Vdm_1 + 1.0\ Vdm_2 + 0.5\ Vdm_3 + Vxo_3) - Zpv\ (0.5\ Vdm_1 \tag{39}$$

$$+ 1.0\ Vdm_2 + 0.5\ Vdm_3 + Vxo_3) - 0.5\ Zpv\ Vdm_1 + Zpv\ V_g + Z_L\ Vcm_2 - Z_L\ (0.5\ Vdm_2$$

$$+ 0.5\ Vdm_3 + Vxo_3) + Z_L\ Vcm_3 - Z_L\ Vxo_3) = -\frac{-0.5\ Vdm_3 - 0.5\ Vdm_4 + Vxo_3 - Vcm_4}{Zpv} - \frac{-0.5\ Vdm_3 - 1.0\ Vdm_4 + Vxo_3}{Z_L}$$

assign to a name →

$$eq14 \tag{40}$$

$isolate(\ eq14, Vxo_3);$

$$Vxo_3 = \frac{1}{2\ Zpv + 4\ Z_L}(Z_L\ Vcm_1 - 0.5\ Z_L\ Vdm_1 - 1.5\ Z_L\ Vdm_2 - 0.5\ Z_L\ Vdm_3 - Zpv\ Vdm_1 - Zpv\ Vdm_2 + Zpv\ V_g + Z_L\ Vcm_2 + Z_L\ Vcm_3 + 0.5\ Z_L\ Vdm_4 + Z_L\ Vcm_4 + Zpv\ Vdm_4) \tag{41}$$

simplify =

$$Vxo_3 = \frac{1}{2.\ Zpv + 4.\ Z_L}((Vcm_1 - 0.5\ Vdm_1 - 1.5\ Vdm_2 - 0.5\ Vdm_3 + Vcm_2 + Vcm_3 + 0.5\ Vdm_4 + Vcm_4)\ Z_L + (-1.\ Vdm_1 - 1.\ Vdm_2 + V_g + Vdm_4)\ Zpv) \tag{42}$$

$subs(\ Vxo_3 = -0.5\ Vdm_2 - 0.5\ Vdm_3 + Vxo_2,\ eq14)$

$$-\frac{1}{Zpv\ Z_L}(Z_L\ Vcm_1 - Z_L\ (0.5\ Vdm_1 + 0.5\ Vdm_2 + Vxo_2) - Zpv\ (0.5\ Vdm_1 + 0.5\ Vdm_2 + Vxo_2) - 0.5\ Zpv\ Vdm_1 + Zpv\ V_g + Z_L\ Vcm_2 - Z_L\ Vxo_2 + Z_L\ Vcm_3 - Z_L\ (-0.5\ Vdm_2 - 0.5\ Vdm_3 + Vxo_2)) = -\frac{-1.0\ Vdm_3 - 0.5\ Vdm_4 - 0.5\ Vdm_2 + Vxo_2 - Vcm_4}{Zpv} - \frac{-1.0\ Vdm_3 - 1.0\ Vdm_4 - 0.5\ Vdm_2 + Vxo_2}{Z_L} \tag{43}$$

assign to a name →

$$eq15 \tag{44}$$

$isolate(\ eq15, Vxo_2);$

$$Vxo_2 = \frac{1}{2\ Zpv + 4\ Z_L}(Z_L\ Vcm_1 - 0.5\ Z_L\ Vdm_1 - Zpv\ Vdm_1 + Zpv\ V_g + Z_L\ Vcm_2 + Z_L\ Vcm_3 + 1.5\ Z_L\ Vdm_3 + 0.5\ Z_L\ Vdm_4 + 0.5\ Z_L\ Vdm_2 + Z_L\ Vcm_4 + Zpv\ Vdm_3 + Zpv\ Vdm_4) \tag{45}$$

simplify =

$$Vxo_2 = \frac{1}{2.\ Zpv + 4.\ Z_L}((Vcm_1 - 0.5\ Vdm_1 + Vcm_2 + Vcm_3 + 1.5\ Vdm_3 + 0.5\ Vdm_4 + 0.5\ Vdm_2 + Vcm_4)\ Z_L + (-1.\ Vdm_1 + V_g + Vdm_3 + Vdm_4)\ Zpv) \tag{46}$$

$subs(\ Vxo_2 = -0.5\ Vdm_1 - 0.5\ Vdm_2 + Vxo_1,\ eq15)$

$$-\frac{1}{Zpv\ Z_L}(Z_L\ Vcm_1 - Z_L\ Vxo_1 - Zpv\ Vxo_1 - 0.5\ Zpv\ Vdm_1 + Zpv\ V_g + Z_L\ Vcm_2 - Z_L\ (-0.5\ Vdm_1 - 0.5\ Vdm_2 + Vxo_1) + Z_L\ Vcm_3 - Z_L\ (-1.0\ Vdm_2 - 0.5\ Vdm_3 - 0.5\ Vdm_1 + Vxo_1)) = \tag{47}$$

$$-\frac{-1.0\,Vdm_3 - 0.5\,Vdm_4 - 1.0\,Vdm_2 - 0.5\,Vdm_1 + Vxo_1 - Vcm_4}{Zpv}$$

$$-\frac{-1.0\,Vdm_3 - 1.0\,Vdm_4 - 1.0\,Vdm_2 - 0.5\,Vdm_1 + Vxo_1}{Z_L}$$

assign to a name →

$$eq16 \tag{48}$$

$isolate(eq16, Vxo_1);$

$$Vxo_1 = \frac{1}{2\,Zpv + 4\,Z_L}\left(Zpv\,V_g + Z_L\,Vcm_1 + Z_L\,Vcm_2 + 1.5\,Z_L\,Vdm_1 + 2.5\,Z_L\,Vdm_2 + Z_L\,Vcm_3 + 1.5\,Z_L\,Vdm_3 + 0.5\,Z_L\,Vdm_4 + Z_L\,Vcm_4 + Zpv\,Vdm_3 + Zpv\,Vdm_4 + Zpv\,Vdm_2\right) \tag{49}$$

$simplify(isolate(eq16, Vxo_1));$

$$Vxo_1 = \frac{1}{2.\,Zpv + 4.\,Z_L}\left(\left(Vcm_1 + Vcm_2 + 1.5\,Vdm_1 + 2.5\,Vdm_2 + Vcm_3 + 1.5\,Vdm_3 + 0.5\,Vdm_4 + Vcm_4\right)Z_L + Zpv\left(V_g + Vdm_3 + Vdm_4 + Vdm_2\right)\right) \tag{50}$$

$eq17 := Vxo_1 - Vcm_1 = Vno_1$

$$eq17 := Vxo_1 - Vcm_1 = Vno_1 \tag{51}$$

$isolate(eq17, Vno_1);$

$$Vno_1 = Vxo_1 - Vcm_1 \tag{52}$$

$eq18 := Vxo_2 - Vcm_2 = Vno_2$

$$eq18 := Vxo_2 - Vcm_2 = Vno_2 \tag{53}$$

$isolate(eq18, Vno_2);$

$$Vno_2 = Vxo_2 - Vcm_2 \tag{54}$$

$eq19 := Vxo_3 - Vcm_3 = Vno_3$

$$eq19 := Vxo_3 - Vcm_3 = Vno_3 \tag{55}$$

$isolate(eq19, Vno_3);$

$$Vno_3 = Vxo_3 - Vcm_3 \tag{56}$$

$eq20 := Vxo_4 - Vcm_4 = Vno_4$

$$eq20 := Vxo_4 - Vcm_4 = Vno_4 \tag{57}$$

$isolate(eq20, Vno_4);$

$$Vno_4 = Vxo_4 - Vcm_4 \tag{58}$$

$$subs\left(Vxo_1 = \frac{1}{2.\,Zpv + 4.\,Z_L}\left(\left(Vcm_1 + Vcm_2 + 1.5\,Vdm_1 + 2.5\,Vdm_2 + Vcm_3 + 1.5\,Vdm_3 + 0.5\,Vdm_4 + Vcm_4\right)Z_L + Zpv\left(V_g + Vdm_3 + Vdm_4 + Vdm_2\right)\right),\ eq17\right)$$

$$\frac{1}{2.\,Zpv + 4.\,Z_L}\left(\left(Vcm_1 + Vcm_2 + 1.5\,Vdm_1 + 2.5\,Vdm_2 + Vcm_3 + 1.5\,Vdm_3 + 0.5\,Vdm_4 \right. \right. \tag{59}$$

$$+ Vcm_4)\ Z_L + Zpv\ (V_g + Vdm_3 + Vdm_4 + Vdm_2))\ - Vcm_1 = Vno_1$$

assign to a name →

$$eq21 \tag{60}$$

$$isolate(\ eq21,\ Vno_1);$$

$$Vno_1 = \frac{1}{2.\ Zpv + 4.\ Z_L}\ ((Vcm_1 + Vcm_2 + 1.5\ Vdm_1 + 2.5\ Vdm_2 + Vcm_3 + 1.5\ Vdm_3 + 0.5\ Vdm_4 \tag{61}$$
$$+ Vcm_4)\ Z_L + Zpv\ (V_g + Vdm_3 + Vdm_4 + Vdm_2))\ - Vcm_1$$

$$subs\left(Vxo_2 = \frac{1}{2.\ Zpv + 4.\ Z_L}\ ((Vcm_1 - 0.5\ Vdm_1 + Vcm_2 + Vcm_3 + 1.5\ Vdm_3 + 0.5\ Vdm_4 + 0.5\ Vdm_2\right.$$
$$\left. + Vcm_4)\ Z_L + (-1.\ Vdm_1 + V_g + Vdm_3 + Vdm_4)\ Zpv),\ eq18\right)$$

$$\frac{1}{2.\ Zpv + 4.\ Z_L}\ ((Vcm_1 - 0.5\ Vdm_1 + Vcm_2 + Vcm_3 + 1.5\ Vdm_3 + 0.5\ Vdm_4 + 0.5\ Vdm_2 \tag{62}$$
$$+ Vcm_4)\ Z_L + (-1.\ Vdm_1 + V_g + Vdm_3 + Vdm_4)\ Zpv) - Vcm_2 = Vno_2$$

assign to a name →

$$eq22 \tag{63}$$

$$isolate(\ eq22,\ Vno_2);$$

$$Vno_2 = \frac{1}{2.\ Zpv + 4.\ Z_L}\ ((Vcm_1 - 0.5\ Vdm_1 + Vcm_2 + Vcm_3 + 1.5\ Vdm_3 + 0.5\ Vdm_4 + 0.5\ Vdm_2 \tag{64}$$
$$+ Vcm_4)\ Z_L + (-1.\ Vdm_1 + V_g + Vdm_3 + Vdm_4)\ Zpv) - Vcm_2$$

$$subs\left(Vxo_3 = \frac{1}{2.\ Zpv + 4.\ Z_L}\ ((Vcm_1 - 0.5\ Vdm_1 - 1.5\ Vdm_2 - 0.5\ Vdm_3 + Vcm_2 + Vcm_3 + 0.5\ Vdm_4\right.$$
$$\left. + Vcm_4)\ Z_L + (-1.\ Vdm_1 - 1.\ Vdm_2 + V_g + Vdm_4)\ Zpv),\ eq19\right)$$

$$\frac{1}{2.\ Zpv + 4.\ Z_L}\ ((Vcm_1 - 0.5\ Vdm_1 - 1.5\ Vdm_2 - 0.5\ Vdm_3 + Vcm_2 + Vcm_3 + 0.5\ Vdm_4 \tag{65}$$
$$+ Vcm_4)\ Z_L + (-1.\ Vdm_1 - 1.\ Vdm_2 + V_g + Vdm_4)\ Zpv) - Vcm_3 = Vno_3$$

assign to a name →

$$eq23 \tag{66}$$

$$isolate(\ eq23,\ Vno_3);$$

$$Vno_3 = \frac{1}{2.\ Zpv + 4.\ Z_L}\ ((Vcm_1 - 0.5\ Vdm_1 - 1.5\ Vdm_2 - 0.5\ Vdm_3 + Vcm_2 + Vcm_3 + 0.5\ Vdm_4 \tag{67}$$
$$+ Vcm_4)\ Z_L + (-1.\ Vdm_1 - 1.\ Vdm_2 + V_g + Vdm_4)\ Zpv) - Vcm_3$$

$$subs\left(Vxo_4 = \frac{1}{2.\ Zpv + 4.\ Z_L}\ ((Vcm_1 - 0.5\ Vdm_1 - 1.5\ Vdm_2 - 2.5\ Vdm_3 - 1.5\ Vdm_4 + Vcm_2 + Vcm_3\right.$$
$$\left. + Vcm_4)\ Z_L + (-1.\ Vdm_1 - 1.\ Vdm_2 - 1.\ Vdm_3 + V_g)\ Zpv),\ eq20\right)$$

$$\frac{1}{2.\ Zpv + 4.\ Z_L}\ ((Vcm_1 - 0.5\ Vdm_1 - 1.5\ Vdm_2 - 2.5\ Vdm_3 - 1.5\ Vdm_4 + Vcm_2 + Vcm_3 \tag{68}$$

$$+ Vcm_4)\ Z_L + (-1.\ Vdm_1 - 1.\ Vdm_2 - 1.\ Vdm_3 + V_g)\ Zpv) - Vcm_4 = Vno_4$$

assign to a name →

$$eq24 \tag{69}$$

$$isolate(eq24,\ Vno_4);$$

$$Vno_4 = \frac{1}{2.\ Zpv + 4.\ Z_L}((Vcm_1 - 0.5\ Vdm_1 - 1.5\ Vdm_2 - 2.5\ Vdm_3 - 1.5\ Vdm_4 + Vcm_2 + Vcm_3 + Vcm_4)\ Z_L + (-1.\ Vdm_1 - 1.\ Vdm_2 - 1.\ Vdm_3 + V_g)\ Zpv) - Vcm_4 \tag{70}$$

$$simplify(isolate(eq21,\ Vno_1));$$

$$Vno_1 = \frac{1}{2.\ Zpv + 4.\ Z_L}((-3.\ Vcm_1 + Vcm_2 + 1.5\ Vdm_1 + 2.5\ Vdm_2 + Vcm_3 + 1.5\ Vdm_3 + 0.5\ Vdm_4 + Vcm_4)\ Z_L + (V_g + Vdm_2 + Vdm_3 + Vdm_4 - 2.\ Vcm_1)\ Zpv) \tag{71}$$

$$simplify(isolate(eq22,\ Vno_2));$$

$$Vno_2 = \frac{1}{2.\ Zpv + 4.\ Z_L}((Vcm_1 - 0.5\ Vdm_1 - 3.\ Vcm_2 + Vcm_3 + 1.5\ Vdm_3 + 0.5\ Vdm_4 + 0.5\ Vdm_2 + Vcm_4)\ Z_L + (-1.\ Vdm_1 + V_g + Vdm_3 + Vdm_4 - 2.\ Vcm_2)\ Zpv) \tag{72}$$

$$simplify(isolate(eq23,\ Vno_3));$$

$$Vno_3 = \frac{1}{2.\ Zpv + 4.\ Z_L}((Vcm_1 - 0.5\ Vdm_1 - 1.5\ Vdm_2 - 0.5\ Vdm_3 + Vcm_2 - 3.\ Vcm_3 + 0.5\ Vdm_4 + Vcm_4)\ Z_L + (-1.\ Vdm_1 - 1.\ Vdm_2 + V_g + Vdm_4 - 2.\ Vcm_3)\ Zpv) \tag{73}$$

$$simplify(isolate(eq24,\ Vno_4));$$

$$Vno_4 = \frac{1}{2.\ Zpv + 4.\ Z_L}((Vcm_1 - 0.5\ Vdm_1 - 1.5\ Vdm_2 - 2.5\ Vdm_3 - 1.5\ Vdm_4 + Vcm_2 + Vcm_3 - 3.\ Vcm_4)\ Z_L + (-1.\ Vdm_1 - 1.\ Vdm_2 - 1.\ Vdm_3 + V_g - 2.\ Vcm_4)\ Zpv) \tag{74}$$

$$eq25 := Vno_1 + Vno_2 + Vno_3 + Vno_4$$

$$eq25 := Vno_1 + Vno_2 + Vno_3 + Vno_4 \tag{75}$$

$$subs\left(Vno_4 = \frac{1}{2.\ Zpv + 4.\ Z_L}((Vcm_1 - 0.5\ Vdm_1 - 1.5\ Vdm_2 - 2.5\ Vdm_3 - 1.5\ Vdm_4 + Vcm_2 + Vcm_3 - 3.\ Vcm_4)\ Z_L + (-1.\ Vdm_1 - 1.\ Vdm_2 - 1.\ Vdm_3 + V_g - 2.\ Vcm_4)\ Zpv),\ eq25\right)$$

$$Vno_1 + Vno_2 + Vno_3 + \frac{1}{2.\ Zpv + 4.\ Z_L}((Vcm_1 - 0.5\ Vdm_1 - 1.5\ Vdm_2 - 2.5\ Vdm_3 - 1.5\ Vdm_4 + Vcm_2 + Vcm_3 - 3.\ Vcm_4)\ Z_L + (-1.\ Vdm_1 - 1.\ Vdm_2 - 1.\ Vdm_3 + V_g - 2.\ Vcm_4)\ Zpv) \tag{76}$$

assign to a name →

$$eq26 \tag{77}$$

$$subs\left(Vno_3 = \frac{1}{2.\ Zpv + 4.\ Z_L}((Vcm_1 - 0.5\ Vdm_1 - 1.5\ Vdm_2 - 0.5\ Vdm_3 + Vcm_2 - 3.\ Vcm_3 + 0.5\ Vdm_4$$

$$+ Vcm_4)\ Z_L + (-1.\ Vdm_1 - 1.\ Vdm_2 + V_g + Vdm_4 - 2.\ Vcm_3)\ Zpv),\ eq26\Big)$$

$$Vno_1 + Vno_2 + \frac{1}{2.\ Zpv + 4.\ Z_L}((Vcm_1 - 0.5\ Vdm_1 - 1.5\ Vdm_2 - 0.5\ Vdm_3 + Vcm_2 - 3.\ Vcm_3 \quad \textbf{(78)}$$
$$+ 0.5\ Vdm_4 + Vcm_4)\ Z_L + (-1.\ Vdm_1 - 1.\ Vdm_2 + V_g + Vdm_4 - 2.\ Vcm_3)\ Zpv)$$
$$+ \frac{1}{2.\ Zpv + 4.\ Z_L}((Vcm_1 - 0.5\ Vdm_1 - 1.5\ Vdm_2 - 2.5\ Vdm_3 - 1.5\ Vdm_4 + Vcm_2 + Vcm_3$$
$$- 3.\ Vcm_4)\ Z_L + (-1.\ Vdm_1 - 1.\ Vdm_2 - 1.\ Vdm_3 + V_g - 2.\ Vcm_4)\ Zpv)$$

assign to a name →

$$eq27 \quad \textbf{(79)}$$

$$subs\Big(Vno_2 = \frac{1}{2.\ Zpv + 4.\ Z_L}((Vcm_1 - 0.5\ Vdm_1 - 3.\ Vcm_2 + Vcm_3 + 1.5\ Vdm_3 + 0.5\ Vdm_4 + 0.5\ Vdm_2$$
$$+ Vcm_4)\ Z_L + (-1.\ Vdm_1 + V_g + Vdm_3 + Vdm_4 - 2.\ Vcm_2)\ Zpv),\ eq27\Big)$$

$$Vno_1 + \frac{1}{2.\ Zpv + 4.\ Z_L}((Vcm_1 - 0.5\ Vdm_1 - 3.\ Vcm_2 + Vcm_3 + 1.5\ Vdm_3 + 0.5\ Vdm_4 \quad \textbf{(80)}$$
$$+ 0.5\ Vdm_2 + Vcm_4)\ Z_L + (-1.\ Vdm_1 + V_g + Vdm_3 + Vdm_4 - 2.\ Vcm_2)\ Zpv)$$
$$+ \frac{1}{2.\ Zpv + 4.\ Z_L}((Vcm_1 - 0.5\ Vdm_1 - 1.5\ Vdm_2 - 0.5\ Vdm_3 + Vcm_2 - 3.\ Vcm_3$$
$$+ 0.5\ Vdm_4 + Vcm_4)\ Z_L + (-1.\ Vdm_1 - 1.\ Vdm_2 + V_g + Vdm_4 - 2.\ Vcm_3)\ Zpv)$$
$$+ \frac{1}{2.\ Zpv + 4.\ Z_L}((Vcm_1 - 0.5\ Vdm_1 - 1.5\ Vdm_2 - 2.5\ Vdm_3 - 1.5\ Vdm_4 + Vcm_2 + Vcm_3$$
$$- 3.\ Vcm_4)\ Z_L + (-1.\ Vdm_1 - 1.\ Vdm_2 - 1.\ Vdm_3 + V_g - 2.\ Vcm_4)\ Zpv)$$

assign to a name →

$$eq28 \quad \textbf{(81)}$$

$$subs\Big(Vno_1 = \frac{1}{2.\ Zpv + 4.\ Z_L}((-3.\ Vcm_1 + Vcm_2 + 1.5\ Vdm_1 + 2.5\ Vdm_2 + Vcm_3 + 1.5\ Vdm_3$$
$$+ 0.5\ Vdm_4 + Vcm_4)\ Z_L + (V_g + Vdm_2 + Vdm_3 + Vdm_4 - 2.\ Vcm_1)\ Zpv),\ eq28\Big)$$

$$\frac{1}{2.\ Zpv + 4.\ Z_L}((-3.\ Vcm_1 + Vcm_2 + 1.5\ Vdm_1 + 2.5\ Vdm_2 + Vcm_3 + 1.5\ Vdm_3 + 0.5\ Vdm_4 \quad \textbf{(82)}$$
$$+ Vcm_4)\ Z_L + (V_g + Vdm_3 + Vdm_4 + Vdm_2 - 2.\ Vcm_1)\ Zpv) + \frac{1}{2.\ Zpv + 4.\ Z_L}((Vcm_1$$
$$- 0.5\ Vdm_1 - 3.\ Vcm_2 + Vcm_3 + 1.5\ Vdm_3 + 0.5\ Vdm_4 + 0.5\ Vdm_2 + Vcm_4)\ Z_L + ($$
$$-1.\ Vdm_1 + V_g + Vdm_3 + Vdm_4 - 2.\ Vcm_2)\ Zpv) + \frac{1}{2.\ Zpv + 4.\ Z_L}((Vcm_1 - 0.5\ Vdm_1$$
$$- 1.5\ Vdm_2 - 0.5\ Vdm_3 + Vcm_2 - 3.\ Vcm_3 + 0.5\ Vdm_4 + Vcm_4)\ Z_L + (-1.\ Vdm_1 - 1.\ Vdm_2$$

$$+ V_g + Vdm_4 - 2.\ Vcm_3\big)\ Zpv\big) + \frac{1}{2.\ Zpv + 4.\ Z_L}\big(\big(Vcm_1 - 0.5\ Vdm_1 - 1.5\ Vdm_2 - 2.5\ Vdm_3 - 1.5\ Vdm_4 + Vcm_2 + Vcm_3 - 3.\ Vcm_4\big)\ Z_L + \big(-1.\ Vdm_1 - 1.\ Vdm_2 - 1.\ Vdm_3 + V_g - 2.\ Vcm_4\big)\ Zpv\big)$$

$$\xrightarrow{\text{simplify symbolic}} \frac{\big(-Vdm_2 - 2.\ Vcm_3 + Vdm_3 - 2.\ Vcm_1 - 2.\ Vcm_4 - 3.\ Vdm_1 + 4.\ V_g + 3.\ Vdm_4 - 2.\ Vcm_2\big)\ Zpv}{2.\ Zpv + 4.\ Z_L} \quad \textbf{(83)}$$

$$\xrightarrow{\text{limit}} -0.5\ Vdm_2 - 1.0\ Vcm_3 + 0.5\ Vdm_3 - 1.0\ Vcm_1 - 1.0\ Vcm_4 - 1.5\ Vdm_1 + 2.0\ V_g + 1.5\ Vdm_4 - 1.0\ Vcm_2 \quad \textbf{(84)}$$

11-level Symmetrical Inductance Circuit Derivation:

$$eq1 := \frac{Vxo_1 - Vcm_1}{Zpv} + \frac{Vxo_1 + 0.5\ Vdm_1 - V_g}{Z_L} - i_1 = 0$$

$$eq1 := \frac{Vxo_1 - Vcm_1}{Zpv} + \frac{Vxo_1 + 0.5\ Vdm_1 - V_g}{Z_L} - i_1 = 0 \quad \textbf{(1)}$$

$$eq2 := \frac{Vxo_2 - Vcm_2}{Zpv} + i_1 - i_2 = 0$$

$$eq2 := \frac{Vxo_2 - Vcm_2}{Zpv} + i_1 - i_2 = 0 \quad \textbf{(2)}$$

$$eq3 := \frac{Vxo_3 - Vcm_3}{Zpv} + i_2 - i_3 = 0$$

$$eq3 := \frac{Vxo_3 - Vcm_3}{Zpv} + i_2 - i_3 = 0 \quad \textbf{(3)}$$

$$eq4 := \frac{Vxo_4 - Vcm_4}{Zpv} + i_3 - i_4 = 0$$

$$eq4 := \frac{Vxo_4 - Vcm_4}{Zpv} + i_3 - i_4 = 0 \quad \textbf{(4)}$$

$$eq5 := \frac{Vxo_5 - Vcm_5}{Zpv} + i_4 + \frac{Vxo_5 - 0.5\ Vdm_5}{Z_L} = 0$$

$$eq5 := \frac{Vxo_5 - Vcm_5}{Zpv} + i_4 + \frac{Vxo_5 - 0.5\ Vdm_5}{Z_L} = 0 \quad \textbf{(5)}$$

$$isolate(eq1,\ i_1);$$

$$i_1 = \frac{Vxo_1 - Vcm_1}{Zpv} + \frac{Vxo_1 + 0.5\ Vdm_1 - V_g}{Z_L} \quad \textbf{(6)}$$

$$isolate(eq2,\ i_1);$$

$$i_1 = -\frac{Vxo_2 - Vcm_2}{Zpv} + i_2 \quad \textbf{(7)}$$

$$isolate(eq3,\ i_2);$$

$$i_2 = -\frac{Vxo_3 - Vcm_3}{Zpv} + i_3 \quad \textbf{(8)}$$

$$isolate(eq4,\ i_3);$$

$$i_3 = -\frac{Vxo_4 - Vcm_4}{Zpv} + i_4 \quad \textbf{(9)}$$

$$isolate(eq5,\ i_4);$$

$$i_4 = -\frac{Vxo_5 - Vcm_5}{Zpv} - \frac{Vxo_5 - 0.5\ Vdm_5}{Z_L} \quad \textbf{(10)}$$

$$algsubs\left(i_1 = \frac{Vxo_1 - Vcm_1}{Zpv} + \frac{Vxo_1 + 0.5\ Vdm_1 - V_g}{Z_L},\ i_1 = -\frac{Vxo_2 - Vcm_2}{Zpv} + i_2\right)$$

$$-\frac{Z_L\,Vcm_1 - Z_L\,Vxo_1 - Zpv\,Vxo_1 - 0.5\,Zpv\,Vdm_1 + Zpv\,V_g}{Zpv\,Z_L} = -\frac{Vxo_2 - Vcm_2}{Zpv} + i_2 \tag{11}$$

assign to a name →

$$eq6 \tag{12}$$

$isolate(\ eq6, i_2);$

$$i_2 = -\frac{Z_L\,Vcm_1 - Z_L\,Vxo_1 - Zpv\,Vxo_1 - 0.5\,Zpv\,Vdm_1 + Zpv\,V_g}{Zpv\,Z_L} + \frac{Vxo_2 - Vcm_2}{Zpv} \tag{13}$$

$$algsubs\left(i_2 = -\frac{Z_L\,Vcm_1 - Z_L\,Vxo_1 - Zpv\,Vxo_1 - 0.5\,Zpv\,Vdm_1 + Zpv\,V_g}{Zpv\,Z_L} + \frac{Vxo_2 - Vcm_2}{Zpv}, i_2 = -\frac{Vxo_3 - Vcm_3}{Zpv} + i_3\right)$$

$$-\frac{Z_L\,Vcm_1 - Z_L\,Vxo_1 - Zpv\,Vxo_1 - 0.5\,Zpv\,Vdm_1 + Zpv\,V_g + Z_L\,Vcm_2 - Z_L\,Vxo_2}{Zpv\,Z_L} = -\frac{Vxo_3 - Vcm_3}{Zpv} + i_3 \tag{14}$$

assign to a name →

$$eq7 \tag{15}$$

$isolate(\ eq7, i_3);$

$$i_3 = -\frac{Z_L\,Vcm_1 - Z_L\,Vxo_1 - Zpv\,Vxo_1 - 0.5\,Zpv\,Vdm_1 + Zpv\,V_g + Z_L\,Vcm_2 - Z_L\,Vxo_2}{Zpv\,Z_L} + \frac{Vxo_3 - Vcm_3}{Zpv} \tag{16}$$

$$algsubs\left(i_3 = -\frac{Z_L\,Vcm_1 - Z_L\,Vxo_1 - Zpv\,Vxo_1 - 0.5\,Zpv\,Vdm_1 + Zpv\,V_g + Z_L\,Vcm_2 - Z_L\,Vxo_2}{Zpv\,Z_L} + \frac{Vxo_3 - Vcm_3}{Zpv}, i_3 = -\frac{Vxo_4 - Vcm_4}{Zpv} + i_4\right)$$

$$-\frac{1}{Zpv\,Z_L}\left(Z_L\,Vcm_1 - Z_L\,Vxo_1 - Zpv\,Vxo_1 - 0.5\,Zpv\,Vdm_1 + Zpv\,V_g + Z_L\,Vcm_2 - Z_L\,Vxo_2 + Z_L\,Vcm_3 - Z_L\,Vxo_3\right) = -\frac{Vxo_4 - Vcm_4}{Zpv} + i_4 \tag{17}$$

assign to a name →

$$eq8 \tag{18}$$

$isolate(\ eq8, i_4);$

$$i_4 = -\frac{1}{Zpv\,Z_L}\left(Z_L\,Vcm_1 - Z_L\,Vxo_1 - Zpv\,Vxo_1 - 0.5\,Zpv\,Vdm_1 + Zpv\,V_g + Z_L\,Vcm_2 - Z_L\,Vxo_2 + Z_L\,Vcm_3 - Z_L\,Vxo_3\right) + \frac{Vxo_4 - Vcm_4}{Zpv} \tag{19}$$

$$algsubs\left(i_4 = -\frac{1}{Zpv\,Z_L}\left(Z_L\,Vcm_1 - Z_L\,Vxo_1 - Zpv\,Vxo_1 - 0.5\,Zpv\,Vdm_1 + Zpv\,V_g + Z_L\,Vcm_2 - Z_L\,Vxo_2 + Z_L\,Vcm_3 - Z_L\,Vxo_3\right) + \frac{Vxo_4 - Vcm_4}{Zpv},\ i_4 = -\frac{Vxo_5 - Vcm_5}{Zpv} - \frac{Vxo_5 - 0.5\,Vdm_5}{Z_L}\right)$$

$$-\frac{1}{Zpv\,Z_L}\left(Z_L\,Vcm_1 - Z_L\,Vxo_1 - Zpv\,Vxo_1 - 0.5\,Zpv\,Vdm_1 + Zpv\,V_g + Z_L\,Vcm_2 - Z_L\,Vxo_2 + Z_L\,Vcm_3 - Z_L\,Vxo_3 + Z_L\,Vcm_4 - Z_L\,Vxo_4\right) = -\frac{Vxo_5 - Vcm_5}{Zpv} - \frac{Vxo_5 - 0.5\,Vdm_5}{Z_L} \quad (20)$$

assign to a name →

$$eq9 \quad (21)$$

$$isolate(eq9, Vxo_1);$$

$$Vxo_1 = \frac{1}{-Zpv - Z_L}\left(-\left(-\frac{Vxo_5 - Vcm_5}{Zpv} - \frac{Vxo_5 - 0.5\,Vdm_5}{Z_L}\right)Zpv\,Z_L - Z_L\,Vcm_1 + 0.5\,Zpv\,Vdm_1 - Zpv\,V_g - Z_L\,Vcm_2 + Z_L\,Vxo_2 - Z_L\,Vcm_3 + Z_L\,Vxo_3 - Z_L\,Vcm_4 + Z_L\,Vxo_4\right) \quad (22)$$

simplify =

$$Vxo_1 = \frac{1}{Z_L + Zpv}\left(\left(Vcm_5 - 1.\,Vxo_5 + Vcm_1 + Vcm_2 - 1.\,Vxo_2 + Vcm_3 - 1.\,Vxo_3 + Vcm_4 - 1.\,Vxo_4\right)Z_L + \left(-1.\,Vxo_5 + 0.5\,Vdm_5 - 0.5\,Vdm_1 + V_g\right)Zpv\right) \quad (23)$$

$$eq10 := Vxo_1 - Vxo_2 = 0.5\cdot\left(Vdm_1 + Vdm_2\right)$$

$$eq10 := Vxo_1 - Vxo_2 = 0.5\,Vdm_1 + 0.5\,Vdm_2 \quad (24)$$

$$eq11 := Vxo_2 - Vxo_3 = 0.5\cdot\left(Vdm_2 + Vdm_3\right)$$

$$eq11 := Vxo_2 - Vxo_3 = 0.5\,Vdm_2 + 0.5\,Vdm_3 \quad (25)$$

$$eq12 := Vxo_3 - Vxo_4 = 0.5\cdot\left(Vdm_3 + Vdm_4\right)$$

$$eq12 := Vxo_3 - Vxo_4 = 0.5\,Vdm_3 + 0.5\,Vdm_4 \quad (26)$$

$$eq13 := Vxo_4 - Vxo_5 = 0.5\cdot\left(Vdm_4 + Vdm_5\right)$$

$$eq13 := Vxo_4 - Vxo_5 = 0.5\,Vdm_4 + 0.5\,Vdm_5 \quad (27)$$

$$isolate(eq10, Vxo_1);$$

$$Vxo_1 = 0.5\,Vdm_1 + 0.5\,Vdm_2 + Vxo_2 \quad (28)$$

$$isolate(eq11, Vxo_2);$$

$$Vxo_2 = 0.5\,Vdm_2 + 0.5\,Vdm_3 + Vxo_3 \quad (29)$$

$$isolate(eq12, Vxo_3);$$

$$Vxo_3 = 0.5\,Vdm_3 + 0.5\,Vdm_4 + Vxo_4 \quad (30)$$

$$isolate(eq13, Vxo_4);$$

$$Vxo_4 = 0.5\ Vdm_4 + 0.5\ Vdm_5 + Vxo_5 \tag{31}$$

$subs\left(Vxo_1 = 0.5\ Vdm_1 + 0.5\ Vdm_2 + Vxo_2,\ eq9\right)$

$$-\frac{1}{Zpv\ Z_L}\left(Z_L\ Vcm_1 - Z_L\left(0.5\ Vdm_1 + 0.5\ Vdm_2 + Vxo_2\right) - Zpv\left(0.5\ Vdm_1 + 0.5\ Vdm_2 + Vxo_2\right)\right. \tag{32}$$
$$\left. - 0.5\ Zpv\ Vdm_1 + Zpv\ V_g + Z_L\ Vcm_2 - Z_L\ Vxo_2 + Z_L\ Vcm_3 - Z_L\ Vxo_3 + Z_L\ Vcm_4 - Z_L\ Vxo_4\right)$$
$$= -\frac{Vxo_5 - Vcm_5}{Zpv} - \frac{Vxo_5 - 0.5\ Vdm_5}{Z_L}$$

assign to a name →

$$eq14 \tag{33}$$

$isolate\left(eq14,\ Vxo_2\right);$

$$Vxo_2 = \frac{1}{-Zpv - 2\ Z_L}\left(-\left(-\frac{Vxo_5 - Vcm_5}{Zpv} - \frac{Vxo_5 - 0.5\ Vdm_5}{Z_L}\right) Zpv\ Z_L - Z_L\ Vcm_1\right. \tag{34}$$
$$+ 1.0\ Zpv\ Vdm_1 - Zpv\ V_g - Z_L\ Vcm_2 - Z_L\ Vcm_3 + Z_L\ Vxo_3 - Z_L\ Vcm_4 + Z_L\ Vxo_4$$
$$\left. + 0.5\ Z_L\ Vdm_1 + 0.5\ Z_L\ Vdm_2 + 0.5\ Zpv\ Vdm_2\right)$$

simplify =

$$Vxo_2 = \frac{1}{Zpv + 2.\ Z_L}\left(\left(Vcm_5 - 1.\ Vxo_5 + Vcm_1 + Vcm_2 + Vcm_3 - 1.\ Vxo_3 + Vcm_4 - 1.\ Vxo_4\right.\right. \tag{35}$$
$$\left.\left. - 0.5\ Vdm_1 - 0.5\ Vdm_2\right) Z_L + \left(-1.\ Vxo_5 + 0.5\ Vdm_5 - 1.\ Vdm_1 + V_g - 0.5\ Vdm_2\right) Zpv\right)$$

$subs\left(Vxo_2 = 0.5\ Vdm_2 + 0.5\ Vdm_3 + Vxo_3,\ eq14\right)$

$$-\frac{1}{Zpv\ Z_L}\left(Z_L\ Vcm_1 - Z_L\left(0.5\ Vdm_1 + 1.0\ Vdm_2 + 0.5\ Vdm_3 + Vxo_3\right) - Zpv\left(0.5\ Vdm_1\right.\right. \tag{36}$$
$$\left. + 1.0\ Vdm_2 + 0.5\ Vdm_3 + Vxo_3\right) - 0.5\ Zpv\ Vdm_1 + Zpv\ V_g + Z_L\ Vcm_2 - Z_L\left(0.5\ Vdm_2\right.$$
$$\left. + 0.5\ Vdm_3 + Vxo_3\right) + Z_L\ Vcm_3 - Z_L\ Vxo_3 + Z_L\ Vcm_4 - Z_L\ Vxo_4\right) = -\frac{Vxo_5 - Vcm_5}{Zpv}$$
$$- \frac{Vxo_5 - 0.5\ Vdm_5}{Z_L}$$

assign to a name →

$$eq15 \tag{37}$$

$isolate\left(eq15,\ Vxo_3\right);$

$$Vxo_3 = \frac{1}{-Zpv - 3\ Z_L}\left(-\left(-\frac{Vxo_5 - Vcm_5}{Zpv} - \frac{Vxo_5 - 0.5\ Vdm_5}{Z_L}\right) Zpv\ Z_L - Z_L\ Vcm_1\right. \tag{38}$$
$$\left. + 1.0\ Zpv\ Vdm_1 - Zpv\ V_g - Z_L\ Vcm_2 - Z_L\ Vcm_3 - Z_L\ Vcm_4 + Z_L\ Vxo_4 + 0.5\ Z_L\ Vdm_1\right.$$

$$+ 1.5\ Z_L\ Vdm_2 + 1.0\ Z_L\ Vdm_3 + 1.0\ Zpv\ Vdm_2 + 0.5\ Zpv\ Vdm_3\Big)$$

simplify

$$Vxo_3 = \frac{1}{Zpv + 3.\ Z_L}\left(\left(Vcm_5 - 1.\ Vxo_5 + Vcm_1 + Vcm_2 + Vcm_3 + Vcm_4 - 1.\ Vxo_4 - 0.5\ Vdm_1 - 1.5\ Vdm_2 - 1.\ Vdm_3\right) Z_L + \left(-1.\ Vxo_5 + 0.5\ Vdm_5 - 1.\ Vdm_1 + V_g - 1.\ Vdm_2 - 0.5\ Vdm_3\right) Zpv\right) \tag{39}$$

$subs\left(Vxo_3 = 0.5\ Vdm_3 + 0.5\ Vdm_4 + Vxo_4,\ eq15\right)$

$$-\frac{1}{Zpv\ Z_L}\left(Z_L\ Vcm_1 - Z_L\left(0.5\ Vdm_1 + 1.0\ Vdm_2 + 1.0\ Vdm_3 + 0.5\ Vdm_4 + Vxo_4\right) - Zpv\left(0.5\ Vdm_1 + 1.0\ Vdm_2 + 1.0\ Vdm_3 + 0.5\ Vdm_4 + Vxo_4\right) - 0.5\ Zpv\ Vdm_1 + Zpv\ V_g + Z_L\ Vcm_2 - Z_L\left(0.5\ Vdm_2 + 1.0\ Vdm_3 + 0.5\ Vdm_4 + Vxo_4\right) + Z_L\ Vcm_3 - Z_L\left(0.5\ Vdm_3 + 0.5\ Vdm_4 + Vxo_4\right) + Z_L\ Vcm_4 - Z_L\ Vxo_4\right) = -\frac{Vxo_5 - Vcm_5}{Zpv} - \frac{Vxo_5 - 0.5\ Vdm_5}{Z_L} \tag{40}$$

assign to a name →

$$eq16 \tag{41}$$

$isolate\left(eq16,\ Vxo_4\right);$

$$Vxo_4 = \frac{1}{-Zpv - 4\ Z_L}\left(-\left(-\frac{Vxo_5 - Vcm_5}{Zpv} - \frac{Vxo_5 - 0.5\ Vdm_5}{Z_L}\right) Zpv\ Z_L - Z_L\ Vcm_1 + 1.0\ Zpv\ Vdm_1 - Zpv\ V_g - Z_L\ Vcm_2 - Z_L\ Vcm_3 - Z_L\ Vcm_4 + 0.5\ Z_L\ Vdm_1 + 1.5\ Z_L\ Vdm_2 + 2.5\ Z_L\ Vdm_3 + 1.5\ Z_L\ Vdm_4 + 1.0\ Zpv\ Vdm_2 + 1.0\ Zpv\ Vdm_3 + 0.5\ Zpv\ Vdm_4\right) \tag{42}$$

simplify

$$Vxo_4 = \frac{1}{Zpv + 4.\ Z_L}\left(\left(Vcm_5 - 1.\ Vxo_5 + Vcm_1 + Vcm_2 + Vcm_3 + Vcm_4 - 0.5\ Vdm_1 - 1.5\ Vdm_2 - 2.5\ Vdm_3 - 1.5\ Vdm_4\right) Z_L + \left(-1.\ Vxo_5 + 0.5\ Vdm_5 - 1.\ Vdm_1 + V_g - 1.\ Vdm_2 - 1.\ Vdm_3 - 0.5\ Vdm_4\right) Zpv\right) \tag{43}$$

$subs\left(Vxo_4 = 0.5\ Vdm_4 + 0.5\ Vdm_5 + Vxo_5,\ eq16\right)$

$$-\frac{1}{Zpv\ Z_L}\left(Z_L\ Vcm_1 - Z_L\left(0.5\ Vdm_1 + 1.0\ Vdm_2 + 1.0\ Vdm_3 + 1.0\ Vdm_4 + 0.5\ Vdm_5 + Vxo_5\right) - Zpv\left(0.5\ Vdm_1 + 1.0\ Vdm_2 + 1.0\ Vdm_3 + 1.0\ Vdm_4 + 0.5\ Vdm_5 + Vxo_5\right) - 0.5\ Zpv\ Vdm_1 + Zpv\ V_g + Z_L\ Vcm_2 - Z_L\left(0.5\ Vdm_2 + 1.0\ Vdm_3 + 1.0\ Vdm_4 + 0.5\ Vdm_5 + Vxo_5\right) + Z_L\ Vcm_3 - Z_L\left(0.5\ Vdm_3 + 1.0\ Vdm_4 + 0.5\ Vdm_5 + Vxo_5\right) + Z_L\ Vcm_4 - Z_L\left(0.5\ Vdm_4 + 0.5\ Vdm_5 + Vxo_5\right)\right) = -\frac{Vxo_5 - Vcm_5}{Zpv} - \frac{Vxo_5 - 0.5\ Vdm_5}{Z_L} \tag{44}$$

assign to a name →

$$eq17 \tag{45}$$

$isolate(\ eq17, Vxo_5);$

$$Vxo_5 = \frac{1}{2\ Zpv + 5\ Z_L}\left(-2.5\ Z_L\ Vdm_3 - Zpv\ Vdm_3 + Z_L\ Vcm_4 - 3.5\ Z_L\ Vdm_4 - Zpv\ Vdm_4 + Z_L\ Vcm_1 - Zpv\ Vdm_1 + Zpv\ V_g + Z_L\ Vcm_3 - 2.0\ Z_L\ Vdm_5 + Z_L\ Vcm_2 - 0.5\ Z_L\ Vdm_1 - 1.5\ Z_L\ Vdm_2 - Zpv\ Vdm_2 + Z_L\ Vcm_5\right) \tag{46}$$

simplify =

$$Vxo_5 = \frac{1}{2.\ Zpv + 5.\ Z_L}\left(\left(-2.5\ Vdm_3 + Vcm_4 - 3.5\ Vdm_4 + Vcm_1 + Vcm_3 - 2.\ Vdm_5 + Vcm_2 - 0.5\ Vdm_1 - 1.5\ Vdm_2 + Vcm_5\right) Z_L + \left(-1.\ Vdm_3 - 1.\ Vdm_4 - 1.\ Vdm_1 + V_g - 1.\ Vdm_2\right) Zpv\right) \tag{47}$$

$$subs\left(Vxo_4 = 0.5\ Vdm_4 + 0.5\ Vdm_5 + \left(\frac{1}{2.\ Zpv + 5.\ Z_L}\left(\left(-2.5\ Vdm_3 + Vcm_4 - 3.5\ Vdm_4 + Vcm_1 + Vcm_3 - 2.\ Vdm_5 + Vcm_2 - 0.5\ Vdm_1 - 1.5\ Vdm_2 + Vcm_5\right) Z_L + \left(-1.\ Vdm_3 - 1.\ Vdm_4 - 1.\ Vdm_1 + V_g - 1.\ Vdm_2\right) Zpv\right)\right)\right)$$

$$Vxo_4 = 0.5\ Vdm_4 + 0.5\ Vdm_5 + \frac{1}{2.\ Zpv + 5.\ Z_L}\left(\left(-2.5\ Vdm_3 + Vcm_4 - 3.5\ Vdm_4 + Vcm_1 + Vcm_3 - 2.\ Vdm_5 + Vcm_2 - 0.5\ Vdm_1 - 1.5\ Vdm_2 + Vcm_5\right) Z_L + \left(-1.\ Vdm_3 - 1.\ Vdm_4 - 1.\ Vdm_1 + V_g - 1.\ Vdm_2\right) Zpv\right) \tag{48}$$

assign to a name →

$$eq18 \tag{49}$$

$isolate(\ eq18, Vxo_4);$

$$Vxo_4 = 0.5\ Vdm_4 + 0.5\ Vdm_5 + \frac{1}{2.\ Zpv + 5.\ Z_L}\left(\left(-2.5\ Vdm_3 + Vcm_4 - 3.5\ Vdm_4 + Vcm_1 + Vcm_3 - 2.\ Vdm_5 + Vcm_2 - 0.5\ Vdm_1 - 1.5\ Vdm_2 + Vcm_5\right) Z_L + \left(-1.\ Vdm_3 - 1.\ Vdm_4 - 1.\ Vdm_1 + V_g - 1.\ Vdm_2\right) Zpv\right) \tag{50}$$

$$subs\left(Vxo_3 = 0.5\ Vdm_3 + 0.5\ Vdm_4 + \left(0.5\ Vdm_4 + 0.5\ Vdm_5 + \frac{1}{2.\ Zpv + 5.\ Z_L}\left(\left(-2.5\ Vdm_3 + Vcm_4 - 3.5\ Vdm_4 + Vcm_1 + Vcm_3 - 2.\ Vdm_5 + Vcm_2 - 0.5\ Vdm_1 - 1.5\ Vdm_2 + Vcm_5\right) Z_L + \left(-1.\ Vdm_3 - 1.\ Vdm_4 - 1.\ Vdm_1 + V_g - 1.\ Vdm_2\right) Zpv\right)\right)\right)$$

$$Vxo_3 = 0.5\ Vdm_3 + 1.0\ Vdm_4 + 0.5\ Vdm_5 + \frac{1}{2.\ Zpv + 5.\ Z_L}\left(\left(-2.5\ Vdm_3 + Vcm_4 - 3.5\ Vdm_4 + Vcm_1 + Vcm_3 - 2.\ Vdm_5 + Vcm_2 - 0.5\ Vdm_1 - 1.5\ Vdm_2 + Vcm_5\right) Z_L + \left(-1.\ Vdm_3 - 1.\ Vdm_4 - 1.\ Vdm_1 + V_g - 1.\ Vdm_2\right) Zpv\right) \tag{51}$$

assign to a name →

$$eq19 \tag{52}$$

$$isolate(\ eq19,\ Vxo_3);$$

$$Vxo_3 = 0.5\ Vdm_3 + 1.0\ Vdm_4 + 0.5\ Vdm_5 + \frac{1}{2.\ Zpv + 5.\ Z_L}\left(\left(-2.5\ Vdm_3 + Vcm_4 - 3.5\ Vdm_4 + Vcm_1 + Vcm_3 - 2.\ Vdm_5 + Vcm_2 - 0.5\ Vdm_1 - 1.5\ Vdm_2 + Vcm_5\right) Z_L + \left(-1.\ Vdm_3 - 1.\ Vdm_4 - 1.\ Vdm_1 + V_g - 1.\ Vdm_2\right) Zpv\right) \quad \textbf{(53)}$$

$$subs\left(Vxo_2 = 0.5\ Vdm_2 + 0.5\ Vdm_3 + \left(0.5\ Vdm_3 + 1.0\ Vdm_4 + 0.5\ Vdm_5 + \frac{1}{2.\ Zpv + 5.\ Z_L}\left(\left(-2.5\ Vdm_3 + Vcm_4 - 3.5\ Vdm_4 + Vcm_1 + Vcm_3 - 2.\ Vdm_5 + Vcm_2 - 0.5\ Vdm_1 - 1.5\ Vdm_2 + Vcm_5\right) Z_L + \left(-1.\ Vdm_3 - 1.\ Vdm_4 - 1.\ Vdm_1 + V_g - 1.\ Vdm_2\right) Zpv\right)\right)\right)$$

$$Vxo_2 = 0.5\ Vdm_2 + 1.0\ Vdm_3 + 1.0\ Vdm_4 + 0.5\ Vdm_5 + \frac{1}{2.\ Zpv + 5.\ Z_L}\left(\left(-2.5\ Vdm_3 + Vcm_4 - 3.5\ Vdm_4 + Vcm_1 + Vcm_3 - 2.\ Vdm_5 + Vcm_2 - 0.5\ Vdm_1 - 1.5\ Vdm_2 + Vcm_5\right) Z_L + \left(-1.\ Vdm_3 - 1.\ Vdm_4 - 1.\ Vdm_1 + V_g - 1.\ Vdm_2\right) Zpv\right) \quad \textbf{(54)}$$

assign to a name →

$$eq20 \quad \textbf{(55)}$$

$$isolate(\ eq20,\ Vxo_2);$$

$$Vxo_2 = 0.5\ Vdm_2 + 1.0\ Vdm_3 + 1.0\ Vdm_4 + 0.5\ Vdm_5 + \frac{1}{2.\ Zpv + 5.\ Z_L}\left(\left(-2.5\ Vdm_3 + Vcm_4 - 3.5\ Vdm_4 + Vcm_1 + Vcm_3 - 2.\ Vdm_5 + Vcm_2 - 0.5\ Vdm_1 - 1.5\ Vdm_2 + Vcm_5\right) Z_L + \left(-1.\ Vdm_3 - 1.\ Vdm_4 - 1.\ Vdm_1 + V_g - 1.\ Vdm_2\right) Zpv\right) \quad \textbf{(56)}$$

$$subs\left(Vxo_1 = 0.5\ Vdm_1 + 0.5\ Vdm_2 + \left(0.5\ Vdm_2 + 1.0\ Vdm_3 + 1.0\ Vdm_4 + 0.5\ Vdm_5 + \frac{1}{2.\ Zpv + 5.\ Z_L}\left(\left(-2.5\ Vdm_3 + Vcm_4 - 3.5\ Vdm_4 + Vcm_1 + Vcm_3 - 2.\ Vdm_5 + Vcm_2 - 0.5\ Vdm_1 - 1.5\ Vdm_2 + Vcm_5\right) Z_L + \left(-1.\ Vdm_3 - 1.\ Vdm_4 - 1.\ Vdm_1 + V_g - 1.\ Vdm_2\right) Zpv\right)\right)\right)$$

$$Vxo_1 = 0.5\ Vdm_1 + 1.0\ Vdm_2 + 1.0\ Vdm_3 + 1.0\ Vdm_4 + 0.5\ Vdm_5 + \frac{1}{2.\ Zpv + 5.\ Z_L}\left(\left(-2.5\ Vdm_3 + Vcm_4 - 3.5\ Vdm_4 + Vcm_1 + Vcm_3 - 2.\ Vdm_5 + Vcm_2 - 0.5\ Vdm_1 - 1.5\ Vdm_2 + Vcm_5\right) Z_L + \left(-1.\ Vdm_3 - 1.\ Vdm_4 - 1.\ Vdm_1 + V_g - 1.\ Vdm_2\right) Zpv\right) \quad \textbf{(57)}$$

assign to a name →

$$eq21 \quad \textbf{(58)}$$

$$isolate(\ eq21,\ Vxo_1);$$

$$Vxo_1 = 0.5\ Vdm_1 + 1.0\ Vdm_2 + 1.0\ Vdm_3 + 1.0\ Vdm_4 + 0.5\ Vdm_5 + \frac{1}{2.\ Zpv + 5.\ Z_L}\left(\left(-2.5\ Vdm_3 + Vcm_4 - 3.5\ Vdm_4 + Vcm_1 + Vcm_3 - 2.\ Vdm_5 + Vcm_2 - 0.5\ Vdm_1 - 1.5\ Vdm_2 + Vcm_5\right) Z_L + \left(-1.\ Vdm_3 - 1.\ Vdm_4 - 1.\ Vdm_1 + V_g - 1.\ Vdm_2\right) Zpv\right) \quad \textbf{(59)}$$

$$eq22 := Vxo_1 - Vcm_1 = Vno_1$$

$$eq22 := Vxo_1 - Vcm_1 = Vno_1 \tag{60}$$

$eq23 := Vxo_2 - Vcm_2 = Vno_2$

$$eq23 := Vxo_2 - Vcm_2 = Vno_2 \tag{61}$$

$eq24 := Vxo_3 - Vcm_3 = Vno_3$

$$eq24 := Vxo_3 - Vcm_3 = Vno_3 \tag{62}$$

$eq25 := Vxo_4 - Vcm_4 = Vno_4$

$$eq25 := Vxo_4 - Vcm_4 = Vno_4 \tag{63}$$

$eq26 := Vxo_5 - Vcm_5 = Vno_5$

$$eq26 := Vxo_5 - Vcm_5 = Vno_5 \tag{64}$$

$isolate(eq22, Vno_1);$

$$Vno_1 = Vxo_1 - Vcm_1 \tag{65}$$

$isolate(eq23, Vno_2);$

$$Vno_2 = Vxo_2 - Vcm_2 \tag{66}$$

$isolate(eq24, Vno_3);$

$$Vno_3 = Vxo_3 - Vcm_3 \tag{67}$$

$isolate(eq25, Vno_4);$

$$Vno_4 = Vxo_4 - Vcm_4 \tag{68}$$

$isolate(eq26, Vno_5);$

$$Vno_5 = Vxo_5 - Vcm_5 \tag{69}$$

$$eq27 := Vno_1 = 0.5\,Vdm_1 + 1.0\,Vdm_2 + 1.0\,Vdm_3 + 1.0\,Vdm_4 + 0.5\,Vdm_5 + \frac{1}{2.\,Zpv + 5.\,Z_L}\left(\left(-2.5\,Vdm_3 + Vcm_4 - 3.5\,Vdm_4 + Vcm_1 + Vcm_3 - 2.\,Vdm_5 + Vcm_2 - 0.5\,Vdm_1 - 1.5\,Vdm_2 + Vcm_5\right) Z_L + \left(-1.\,Vdm_3 - 1.\,Vdm_4 - 1.\,Vdm_1 + V_g - 1.\,Vdm_2\right) Zpv\right) - Vcm_1$$

$$eq27 := Vno_1 = 0.5\,Vdm_1 + 1.0\,Vdm_2 + 1.0\,Vdm_3 + 1.0\,Vdm_4 + 0.5\,Vdm_5 + \frac{1}{2.\,Zpv + 5.\,Z_L}\left(\left(-2.5\,Vdm_3 + Vcm_4 - 3.5\,Vdm_4 + Vcm_1 + Vcm_3 - 2.\,Vdm_5 + Vcm_2 - 0.5\,Vdm_1 - 1.5\,Vdm_2 + Vcm_5\right) Z_L + \left(-1.\,Vdm_3 - 1.\,Vdm_4 - 1.\,Vdm_1 + V_g - 1.\,Vdm_2\right) Zpv\right) - Vcm_1 \tag{70}$$

$isolate(eq27, Vno_1);$

$$Vno_1 = 0.5\,Vdm_1 + 1.0\,Vdm_2 + 1.0\,Vdm_3 + 1.0\,Vdm_4 + 0.5\,Vdm_5 + \frac{1}{2.\,Zpv + 5.\,Z_L}\left(\left(-2.5\,Vdm_3 + Vcm_4 - 3.5\,Vdm_4 + Vcm_1 + Vcm_3 - 2.\,Vdm_5 + Vcm_2 - 0.5\,Vdm_1 - 1.5\,Vdm_2 + Vcm_5\right) Z_L + \left(-1.\,Vdm_3 - 1.\,Vdm_4 - 1.\,Vdm_1 + V_g - 1.\,Vdm_2\right) Zpv\right) - Vcm_1 \tag{71}$$

$$eq28 := Vno_2 = 0.5\,Vdm_2 + 1.0\,Vdm_3 + 1.0\,Vdm_4 + 0.5\,Vdm_5 + \frac{1}{2.\,Zpv + 5.\,Z_L}\left(\left(-2.5\,Vdm_3 + Vcm_4 - 3.5\,Vdm_4 + Vcm_1 + Vcm_3 - 2.\,Vdm_5 + Vcm_2 - 0.5\,Vdm_1 - 1.5\,Vdm_2 + Vcm_5\right) Z_L + \left(-1.\,Vdm_3 - 1.\,Vdm_4 - 1.\,Vdm_1 + V_g - 1.\,Vdm_2\right) Zpv\right) - Vcm_2$$

$$eq28 := Vno_2 = 0.5\ Vdm_2 + 1.0\ Vdm_3 + 1.0\ Vdm_4 + 0.5\ Vdm_5 + \frac{1}{2.\ Zpv + 5.\ Z_L}\left(\left(-2.5\ Vdm_3 + Vcm_4 - 3.5\ Vdm_4 + Vcm_1 + Vcm_3 - 2.\ Vdm_5 + Vcm_2 - 0.5\ Vdm_1 - 1.5\ Vdm_2 + Vcm_5\right) Z_L + \left(-1.\ Vdm_3 - 1.\ Vdm_4 - 1.\ Vdm_1 + V_g - 1.\ Vdm_2\right) Zpv\right) - Vcm_2 \quad (72)$$

$$isolate(\ eq28,\ Vno_2);$$

$$Vno_2 = 0.5\ Vdm_2 + 1.0\ Vdm_3 + 1.0\ Vdm_4 + 0.5\ Vdm_5 + \frac{1}{2.\ Zpv + 5.\ Z_L}\left(\left(-2.5\ Vdm_3 + Vcm_4 - 3.5\ Vdm_4 + Vcm_1 + Vcm_3 - 2.\ Vdm_5 + Vcm_2 - 0.5\ Vdm_1 - 1.5\ Vdm_2 + Vcm_5\right) Z_L + \left(-1.\ Vdm_3 - 1.\ Vdm_4 - 1.\ Vdm_1 + V_g - 1.\ Vdm_2\right) Zpv\right) - Vcm_2 \quad (73)$$

$$eq29 := Vno_3 = 0.5\ Vdm_3 + 1.0\ Vdm_4 + 0.5\ Vdm_5 + \frac{1}{2.\ Zpv + 5.\ Z_L}\left(\left(-2.5\ Vdm_3 + Vcm_4 - 3.5\ Vdm_4 + Vcm_1 + Vcm_3 - 2.\ Vdm_5 + Vcm_2 - 0.5\ Vdm_1 - 1.5\ Vdm_2 + Vcm_5\right) Z_L + \left(-1.\ Vdm_3 - 1.\ Vdm_4 - 1.\ Vdm_1 + V_g - 1.\ Vdm_2\right) Zpv\right) - Vcm_3$$

$$eq29 := Vno_3 = 0.5\ Vdm_3 + 1.0\ Vdm_4 + 0.5\ Vdm_5 + \frac{1}{2.\ Zpv + 5.\ Z_L}\left(\left(-2.5\ Vdm_3 + Vcm_4 - 3.5\ Vdm_4 + Vcm_1 + Vcm_3 - 2.\ Vdm_5 + Vcm_2 - 0.5\ Vdm_1 - 1.5\ Vdm_2 + Vcm_5\right) Z_L + \left(-1.\ Vdm_3 - 1.\ Vdm_4 - 1.\ Vdm_1 + V_g - 1.\ Vdm_2\right) Zpv\right) - Vcm_3 \quad (74)$$

$$isolate(\ eq29,\ Vno_3);$$

$$Vno_3 = 0.5\ Vdm_3 + 1.0\ Vdm_4 + 0.5\ Vdm_5 + \frac{1}{2.\ Zpv + 5.\ Z_L}\left(\left(-2.5\ Vdm_3 + Vcm_4 - 3.5\ Vdm_4 + Vcm_1 + Vcm_3 - 2.\ Vdm_5 + Vcm_2 - 0.5\ Vdm_1 - 1.5\ Vdm_2 + Vcm_5\right) Z_L + \left(-1.\ Vdm_3 - 1.\ Vdm_4 - 1.\ Vdm_1 + V_g - 1.\ Vdm_2\right) Zpv\right) - Vcm_3 \quad (75)$$

$$eq30 := Vno_4 = 0.5\ Vdm_4 + 0.5\ Vdm_5 + \frac{1}{2.\ Zpv + 5.\ Z_L}\left(\left(-2.5\ Vdm_3 + Vcm_4 - 3.5\ Vdm_4 + Vcm_1 + Vcm_3 - 2.\ Vdm_5 + Vcm_2 - 0.5\ Vdm_1 - 1.5\ Vdm_2 + Vcm_5\right) Z_L + \left(-1.\ Vdm_3 - 1.\ Vdm_4 - 1.\ Vdm_1 + V_g - 1.\ Vdm_2\right) Zpv\right) - Vcm_4$$

$$eq30 := Vno_4 = 0.5\ Vdm_4 + 0.5\ Vdm_5 + \frac{1}{2.\ Zpv + 5.\ Z_L}\left(\left(-2.5\ Vdm_3 + Vcm_4 - 3.5\ Vdm_4 + Vcm_1 + Vcm_3 - 2.\ Vdm_5 + Vcm_2 - 0.5\ Vdm_1 - 1.5\ Vdm_2 + Vcm_5\right) Z_L + \left(-1.\ Vdm_3 - 1.\ Vdm_4 - 1.\ Vdm_1 + V_g - 1.\ Vdm_2\right) Zpv\right) - Vcm_4 \quad (76)$$

$$isolate(\ eq30,\ Vno_4);$$

$$Vno_4 = 0.5\ Vdm_4 + 0.5\ Vdm_5 + \frac{1}{2.\ Zpv + 5.\ Z_L}\left(\left(-2.5\ Vdm_3 + Vcm_4 - 3.5\ Vdm_4 + Vcm_1 + Vcm_3 - 2.\ Vdm_5 + Vcm_2 - 0.5\ Vdm_1 - 1.5\ Vdm_2 + Vcm_5\right) Z_L + \left(-1.\ Vdm_3 - 1.\ Vdm_4 - 1.\ Vdm_1 + V_g - 1.\ Vdm_2\right) Zpv\right) - Vcm_4 \quad (77)$$

$$eq31 := Vno_5 = \frac{1}{2.\ Zpv + 5.\ Z_L}\left(\left(-2.5\ Vdm_3 + Vcm_4 - 3.5\ Vdm_4 + Vcm_1 + Vcm_3 - 2.\ Vdm_5 + Vcm_2\right.\right.$$

$$-0.5\,Vdm_1 - 1.5\,Vdm_2 + Vcm_5\big)\,Z_L + \big(-1.\,Vdm_3 - 1.\,Vdm_4 - 1.\,Vdm_1 + V_g - 1.\,Vdm_2\big)\,Zpv\big) - Vcm_5$$

$$eq31 := Vno_5 = \frac{1}{2.\,Zpv + 5.\,Z_L}\big(\big(-2.5\,Vdm_3 + Vcm_4 - 3.5\,Vdm_4 + Vcm_1 + Vcm_3 - 2.\,Vdm_5 + Vcm_2 - 0.5\,Vdm_1 - 1.5\,Vdm_2 + Vcm_5\big)\,Z_L + \big(-1.\,Vdm_3 - 1.\,Vdm_4 - 1.\,Vdm_1 + V_g - 1.\,Vdm_2\big)\,Zpv\big) - Vcm_5 \quad (78)$$

$$isolate(eq31, Vno_5);$$

$$Vno_5 = \frac{1}{2.\,Zpv + 5.\,Z_L}\big(\big(-2.5\,Vdm_3 + Vcm_4 - 3.5\,Vdm_4 + Vcm_1 + Vcm_3 - 2.\,Vdm_5 + Vcm_2 - 0.5\,Vdm_1 - 1.5\,Vdm_2 + Vcm_5\big)\,Z_L + \big(-1.\,Vdm_3 - 1.\,Vdm_4 - 1.\,Vdm_1 + V_g - 1.\,Vdm_2\big)\,Zpv\big) - Vcm_5 \quad (79)$$

$$simplify(isolate(eq31, Vno_5));$$

$$Vno_5 = \frac{1}{2.\,Zpv + 5.\,Z_L}\big(\big(-2.5\,Vdm_3 + Vcm_4 - 3.5\,Vdm_4 + Vcm_1 + Vcm_3 - 2.\,Vdm_5 + Vcm_2 - 0.5\,Vdm_1 - 1.5\,Vdm_2 - 4.\,Vcm_5\big)\,Z_L + \big(-1.\,Vdm_3 - 1.\,Vdm_4 - 1.\,Vdm_1 + V_g - 1.\,Vdm_2 - 2.\,Vcm_5\big)\,Zpv\big) \quad (80)$$

$$simplify(isolate(eq30, Vno_4));$$

$$Vno_4 = \frac{1}{2.\,Zpv + 5.\,Z_L}\big(\big(-1.\,Vdm_4 + 0.5\,Vdm_5 - 2.5\,Vdm_3 - 4.\,Vcm_4 + Vcm_1 + Vcm_3 + Vcm_2 - 0.5\,Vdm_1 - 1.5\,Vdm_2 + Vcm_5\big)\,Z_L + \big(Vdm_5 - 1.\,Vdm_3 - 1.\,Vdm_1 + V_g - 1.\,Vdm_2 - 2.\,Vcm_4\big)\,Zpv\big) \quad (81)$$

$$simplify(isolate(eq29, Vno_3));$$

$$Vno_3 = \frac{1}{2.\,Zpv + 5.\,Z_L}\big(\big(1.5\,Vdm_4 + 0.5\,Vdm_5 + Vcm_4 + Vcm_1 - 4.\,Vcm_3 + Vcm_2 - 0.5\,Vdm_1 - 1.5\,Vdm_2 + Vcm_5\big)\,Z_L + \big(Vdm_4 + Vdm_5 - 1.\,Vdm_1 + V_g - 1.\,Vdm_2 - 2.\,Vcm_3\big)\,Zpv\big) \quad (82)$$

$$simplify(isolate(eq28, Vno_2));$$

$$Vno_2 = \frac{1}{2.\,Zpv + 5.\,Z_L}\big(\big(2.5\,Vdm_3 + Vcm_4 + 1.5\,Vdm_4 + Vcm_1 + Vcm_5 + Vcm_3 + 0.5\,Vdm_5 - 4.\,Vcm_2 - 0.5\,Vdm_1 + Vdm_2\big)\,Z_L + \big(Vdm_3 - 2.\,Vcm_2 + Vdm_4 - 1.\,Vdm_1 + V_g + Vdm_5\big)\,Zpv\big) \quad (83)$$

$$simplify(isolate(eq27, Vno_1));$$

$$Vno_1 = \frac{1}{2.\,Zpv + 5.\,Z_L}\big(\big(2.5\,Vdm_3 + Vcm_4 + 1.5\,Vdm_4 - 4.\,Vcm_1 + Vcm_5 + Vcm_3 + 0.5\,Vdm_5 + Vcm_2 + 2.\,Vdm_1 + 3.5\,Vdm_2\big)\,Z_L + \big(Vdm_3 + Vdm_4 + V_g + Vdm_5 + Vdm_2 - 2.\,Vcm_1\big)\,Zpv\big) \quad (84)$$

$$eq32 := Vno_1 + Vno_2 + Vno_3 + Vno_4 + Vno_5$$

$$eq32 := Vno_1 + Vno_2 + Vno_3 + Vno_4 + Vno_5 \quad (85)$$

$$subs\left(Vno_5 = \frac{1}{2.\,Zpv + 5.\,Z_L}\left(\left(-2.5\,Vdm_3 + Vcm_4 - 3.5\,Vdm_4 + Vcm_1 + Vcm_3 - 2.\,Vdm_5 + Vcm_2 - 0.5\,Vdm_1 - 1.5\,Vdm_2 - 4.\,Vcm_5\right)Z_L + \left(-1.\,Vdm_3 - 1.\,Vdm_4 - 1.\,Vdm_1 + V_g - 1.\,Vdm_2 - 2.\,Vcm_5\right)Zpv\right),\ eq32\right)$$

$$Vno_1 + Vno_2 + Vno_3 + Vno_4 + \frac{1}{2.\,Zpv + 5.\,Z_L}\left(\left(-2.5\,Vdm_3 + Vcm_4 - 3.5\,Vdm_4 + Vcm_1 + Vcm_3 - 2.\,Vdm_5 + Vcm_2 - 0.5\,Vdm_1 - 1.5\,Vdm_2 - 4.\,Vcm_5\right)Z_L + \left(-1.\,Vdm_3 - 1.\,Vdm_4 - 1.\,Vdm_1 + V_g - 1.\,Vdm_2 - 2.\,Vcm_5\right)Zpv\right) \quad \textbf{(86)}$$

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$$eq33 \quad \textbf{(87)}$$

$$subs\left(Vno_4 = \frac{1}{2.\,Zpv + 5.\,Z_L}\left(\left(-1.\,Vdm_4 + 0.5\,Vdm_5 - 2.5\,Vdm_3 - 4.\,Vcm_4 + Vcm_1 + Vcm_3 + Vcm_2 - 0.5\,Vdm_1 - 1.5\,Vdm_2 + Vcm_5\right)Z_L + \left(Vdm_5 - 1.\,Vdm_3 - 1.\,Vdm_1 + V_g - 1.\,Vdm_2 - 2.\,Vcm_4\right)Zpv\right),\ eq33\right)$$

$$Vno_1 + Vno_2 + Vno_3 + \frac{1}{2.\,Zpv + 5.\,Z_L}\left(\left(-1.\,Vdm_4 + 0.5\,Vdm_5 - 2.5\,Vdm_3 - 4.\,Vcm_4 + Vcm_1 + Vcm_3 + Vcm_2 - 0.5\,Vdm_1 - 1.5\,Vdm_2 + Vcm_5\right)Z_L + \left(Vdm_5 - 1.\,Vdm_3 - 1.\,Vdm_1 + V_g - 1.\,Vdm_2 - 2.\,Vcm_4\right)Zpv\right) + \frac{1}{2.\,Zpv + 5.\,Z_L}\left(\left(-2.5\,Vdm_3 + Vcm_4 - 3.5\,Vdm_4 + Vcm_1 + Vcm_3 - 2.\,Vdm_5 + Vcm_2 - 0.5\,Vdm_1 - 1.5\,Vdm_2 - 4.\,Vcm_5\right)Z_L + \left(-1.\,Vdm_3 - 1.\,Vdm_4 - 1.\,Vdm_1 + V_g - 1.\,Vdm_2 - 2.\,Vcm_5\right)Zpv\right) \quad \textbf{(88)}$$

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$$eq34 \quad \textbf{(89)}$$

$$subs\left(Vno_3 = \frac{1}{2.\,Zpv + 5.\,Z_L}\left(\left(1.5\,Vdm_4 + 0.5\,Vdm_5 + Vcm_4 + Vcm_1 - 4.\,Vcm_3 + Vcm_2 - 0.5\,Vdm_1 - 1.5\,Vdm_2 + Vcm_5\right)Z_L + \left(Vdm_4 + Vdm_5 - 1.\,Vdm_1 + V_g - 1.\,Vdm_2 - 2.\,Vcm_3\right)Zpv\right),\ eq34\right)$$

$$Vno_1 + Vno_2 + \frac{1}{2.\,Zpv + 5.\,Z_L}\left(\left(1.5\,Vdm_4 + 0.5\,Vdm_5 + Vcm_4 + Vcm_1 - 4.\,Vcm_3 + Vcm_2 - 0.5\,Vdm_1 - 1.5\,Vdm_2 + Vcm_5\right)Z_L + \left(Vdm_4 + Vdm_5 - 1.\,Vdm_1 + V_g - 1.\,Vdm_2 - 2.\,Vcm_3\right)Zpv\right) + \frac{1}{2.\,Zpv + 5.\,Z_L}\left(\left(-1.\,Vdm_4 + 0.5\,Vdm_5 - 2.5\,Vdm_3 - 4.\,Vcm_4 + Vcm_1 + Vcm_3 + Vcm_2 - 0.5\,Vdm_1 - 1.5\,Vdm_2 + Vcm_5\right)Z_L + \left(Vdm_5 - 1.\,Vdm_3 - 1.\,Vdm_1 + V_g - 1.\,Vdm_2 - 2.\,Vcm_4\right)Zpv\right) + \frac{1}{2.\,Zpv + 5.\,Z_L}\left(\left(-2.5\,Vdm_3 + Vcm_4 - 3.5\,Vdm_4 + Vcm_1 + Vcm_3 - 2.\,Vdm_5 + Vcm_2 - 0.5\,Vdm_1 - 1.5\,Vdm_2 - 4.\,Vcm_5\right)Z_L + \left(-1.\,Vdm_3 - 1.\,Vdm_4 - 1.\,Vdm_1 + V_g - 1.\,Vdm_2 - 2.\,Vcm_5\right)Zpv\right) \quad \textbf{(90)}$$

assign to a name →

$$eq35 \tag{91}$$

$$subs\left(Vno_2 = \frac{1}{2.\,Zpv + 5.\,Z_L}\left(\left(2.5\,Vdm_3 + Vcm_4 + 1.5\,Vdm_4 + Vcm_1 + Vcm_5 + Vcm_3 + 0.5\,Vdm_5 - 4.\,Vcm_2 - 0.5\,Vdm_1 + Vdm_2\right)Z_L + \left(Vdm_3 - 2.\,Vcm_2 + Vdm_4 - 1.\,Vdm_1 + V_g + Vdm_5\right)Zpv\right),\ eq35\right)$$

$$Vno_1 + \frac{1}{2.\,Zpv + 5.\,Z_L}\left(\left(2.5\,Vdm_3 + Vcm_4 + 1.5\,Vdm_4 + Vcm_1 + Vcm_5 + Vcm_3 + 0.5\,Vdm_5 - 4.\,Vcm_2 - 0.5\,Vdm_1 + Vdm_2\right)Z_L + \left(Vdm_3 - 2.\,Vcm_2 + Vdm_4 - 1.\,Vdm_1 + V_g + Vdm_5\right)Zpv\right) + \frac{1}{2.\,Zpv + 5.\,Z_L}\left(\left(1.5\,Vdm_4 + 0.5\,Vdm_5 + Vcm_4 + Vcm_1 - 4.\,Vcm_3 + Vcm_2 - 0.5\,Vdm_1 - 1.5\,Vdm_2 + Vcm_5\right)Z_L + \left(Vdm_4 + Vdm_5 - 1.\,Vdm_1 + V_g - 1.\,Vdm_2 - 2.\,Vcm_3\right)Zpv\right) + \frac{1}{2.\,Zpv + 5.\,Z_L}\left(\left(-1.\,Vdm_4 + 0.5\,Vdm_5 - 2.5\,Vdm_3 - 4.\,Vcm_4 + Vcm_1 + Vcm_3 + Vcm_2 - 0.5\,Vdm_1 - 1.5\,Vdm_2 + Vcm_5\right)Z_L + \left(Vdm_5 - 1.\,Vdm_3 - 1.\,Vdm_1 + V_g - 1.\,Vdm_2 - 2.\,Vcm_4\right)Zpv\right) + \frac{1}{2.\,Zpv + 5.\,Z_L}\left(\left(-2.5\,Vdm_3 + Vcm_4 - 3.5\,Vdm_4 + Vcm_1 + Vcm_3 - 2.\,Vdm_5 + Vcm_2 - 0.5\,Vdm_1 - 1.5\,Vdm_2 - 4.\,Vcm_5\right)Z_L + \left(-1.\,Vdm_3 - 1.\,Vdm_4 - 1.\,Vdm_1 + V_g - 1.\,Vdm_2 - 2.\,Vcm_5\right)Zpv\right) \tag{92}$$

assign to a name →

$$eq36 \tag{93}$$

$$subs\left(Vno_1 = \frac{1}{2.\,Zpv + 5.\,Z_L}\left(\left(2.5\,Vdm_3 + Vcm_4 + 1.5\,Vdm_4 - 4.\,Vcm_1 + Vcm_5 + Vcm_3 + 0.5\,Vdm_5 + Vcm_2 + 2.\,Vdm_1 + 3.5\,Vdm_2\right)Z_L + \left(Vdm_3 + Vdm_4 + V_g + Vdm_5 + Vdm_2 - 2.\,Vcm_1\right)Zpv\right),\ eq36\right)$$

$$\frac{1}{2.\,Zpv + 5.\,Z_L}\left(\left(2.5\,Vdm_3 + Vcm_4 + 1.5\,Vdm_4 - 4.\,Vcm_1 + Vcm_5 + Vcm_3 + 0.5\,Vdm_5 + Vcm_2 + 2.\,Vdm_1 + 3.5\,Vdm_2\right)Z_L + \left(Vdm_3 + Vdm_4 + V_g + Vdm_5 + Vdm_2 - 2.\,Vcm_1\right)Zpv\right) + \frac{1}{2.\,Zpv + 5.\,Z_L}\left(\left(2.5\,Vdm_3 + Vcm_4 + 1.5\,Vdm_4 + Vcm_1 + Vcm_5 + Vcm_3 + 0.5\,Vdm_5 - 4.\,Vcm_2 - 0.5\,Vdm_1 + Vdm_2\right)Z_L + \left(Vdm_3 - 2.\,Vcm_2 + Vdm_4 - 1.\,Vdm_1 + V_g + Vdm_5\right)Zpv\right) + \frac{1}{2.\,Zpv + 5.\,Z_L}\left(\left(1.5\,Vdm_4 + 0.5\,Vdm_5 + Vcm_4 + Vcm_1 - 4.\,Vcm_3 + Vcm_2 - 0.5\,Vdm_1 - 1.5\,Vdm_2 + Vcm_5\right)Z_L + \left(Vdm_4 + Vdm_5 - 1.\,Vdm_1 + V_g - 1.\,Vdm_2 - 2.\,Vcm_3\right)Zpv\right) + \frac{1}{2.\,Zpv + 5.\,Z_L}\left(\left(-1.\,Vdm_4 + 0.5\,Vdm_5 - 2.5\,Vdm_3 - 4.\,Vcm_4 \tag{94}$$

$$+ Vcm_1 + Vcm_3 + Vcm_2 - 0.5\ Vdm_1 - 1.5\ Vdm_2 + Vcm_5)\ Z_L + (Vdm_5 - 1.\ Vdm_3 - 1.\ Vdm_1 + V_g - 1.\ Vdm_2 - 2.\ Vcm_4)\ Zpv) + \frac{1}{2.\ Zpv + 5.\ Z_L}((-2.5\ Vdm_3 + Vcm_4 - 3.5\ Vdm_4 + Vcm_1 + Vcm_3 - 2.\ Vdm_5 + Vcm_2 - 0.5\ Vdm_1 - 1.5\ Vdm_2 - 4.\ Vcm_5)\ Z_L + (-1.\ Vdm_3 - 1.\ Vdm_4 - 1.\ Vdm_1 + V_g - 1.\ Vdm_2 - 2.\ Vcm_5)\ Zpv)$$

$$\xrightarrow{\text{simplify symbolic}}$$

$$\frac{1}{2.\ Zpv + 5.\ Z_L}((-2.\ Vcm_3 - 2.\ Vcm_2 + 2.\ Vdm_4 - 4.\ Vdm_1 + 5.\ V_g + 4.\ Vdm_5 - 2.\ Vdm_2 - 2.\ Vcm_1 - 2.\ Vcm_4 - 2.\ Vcm_5)\ Zpv) \quad \textbf{(95)}$$

$$\xrightarrow{\text{limit}}$$

$$-1.\ Vcm_3 - 1.\ Vcm_2 + Vdm_4 - 2.\ Vdm_1 + 2.500000000\ V_g + 2.\ Vdm_5 - 1.\ Vdm_2 - 1.\ Vcm_1 - 1.\ Vcm_4 - 1.\ Vcm_5 \quad \textbf{(96)}$$