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Contributing to Second Harmonic Manipulated Continuum Mode Power Amplifiers and On-Chip Flux Concentrators

By:

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A thesis submitted in partial fulfilment of the requirements for the degree of Doctor of Philosophy

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March 2019

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Abstract

The current cellular network consumes a staggering 100 TWh of energy every year. In the coming years, millions of devices will be added to the existing network to realize the Internet of Things (IoT), further increasing its power consumption. An RF power amplifier typically consumes a large proportion of the DC power in a wireless transceiver, improving its efficiency has the largest impact on the overall system. Additionally, amplifiers need to demonstrate high linearity and bandwidth to adhere to constraints imposed by wireless standards and to reduce the number of amplifiers required as an amplifier with a broader bandwidth can potentially replace several narrowband amplifiers. A typical approach to improve efficiency is to present an appropriate load at the harmonics generated by the transistor. Recently proposed continuous modes based on harmonic manipulation, such as class B/J continuum, continuous class F (CCF) and continuous class F^{-1} (CCF^{-1}), have shown the capability of achieving counteracting requirements viz., high efficiency, high linearity, and broad bandwidth (with a fractional bandwidth greater than 30%). In these classes of amplifiers, the second harmonic is manipulated by placing a reactive second harmonic load and the reactive component of the fundamental load is adjusted while keeping a fixed resistive component of the fundamental load.

The first contribution of this work is to investigate the reason for amplifiers designed in classes B/J continuum and CCF to achieve high efficiency at back-off and 1dB compression. In this thesis, we demonstrate that the variation of the phase of the current through the non-linear intrinsic capacitances due to the variation of the phase in the continuum of drain voltage waveforms in Class B/J/J* continuum leads to either a reduction or enhancement of intrinsic drain current. Consequently, a subset of voltage waveforms of the class B/J/J* continuum can be used to design amplifiers with higher P1dB, and efficiency at P1dB than in Class B. A simple choice of this subset is demonstrated with a 2.6GHz Class B/J/J* amplifier, achieving a P1dB of 38.1dBm and PAE at P1dB of 54.7%, the highest output power and efficiency at P1dB amongst narrowband linear amplifiers using the CGH40010 reported to date, at a comparable peak PAE of 72%.

Secondly, we propose a new formulation for high-efficiency modes of power amplifiers in which both the in-phase and out-of-phase components of the second harmonic of the current are varied, in addition to the second harmonic component of the voltage. A reduction of the in-phase component of the second harmonic of current allows reduction of the phase difference

between the voltage and current waveforms, thereby increasing the power factor and efficiency. Our proposed waveforms offer a continuous design space between class B/J continuum and continuous F^{-1} achieving an efficiency of up to 91% in theory, but over a wider set of load impedances than continuous class F^{-1}. These waveforms require a short at third and higher harmonic impedances, which are easier to achieve at a higher frequency. The load impedances at the second harmonic are reactive and can be of any value between $-j\infty$ and $j\infty$, easing the amplifier design. A trade-off between linearity and efficiency exists in the newly proposed broadband design space, but we demonstrate inherent broadband capability. The fabricated narrowband amplifier using a GaN HEMT CGH40010F demonstrates 75.9% PAE and 42.2 dBm output power at 2.6 GHz, demonstrating a comparable frequency weighted efficiency for this device to that reported in the literature.

IoT devices may be deployed in critical applications such as radar or 5G transceivers of an autonomous vehicle and hence need to operate free of failure. Monitoring the drain current of the RF GaN MMIC would allow to optimize the device performance and protect it from surges in its supply current. Galvanic current sensors rely on the magnetic field generated by the current as a non-invasive method of current sensing. In this thesis, our third major contribution is a planar on-chip magnetic flux concentrator, is enhance the magnetic field at the current sensor, thereby improving the current detection capability of a current sensor. Our layout utilizes a discontinuity in a magnetic via, resulting in penetration of the magnetic field into the substrate. The proposed concentrator has a magnetic gain x1.8 in comparison to air. The permeability of the magnetic core required is 500, much lower than that reported in off-chip concentrators, resulting in a significant easing of the specifications of the material properties of the core. Additionally, we explore a novel three-dimensional spiral-shaped magnetic flux concentrator. It is predicted via simulations that this geometry becomes a necessity to enhance the magnetic field for increased form factor as the magnetic field from a single planar concentrator deteriorates as its size increases.

Acknowledgements

It's been four years since I embarked on the doctoral research journey and this journey would not have been possible if it is not for the support of several individuals. A simple "thank you" might not be sufficient to express my gratitude towards them, nevertheless, I shall try.

First, I would like to thank my supervisor, Professor Maria Merlyne De Souza, for her financial support and technical direction without which I would not have started to work towards PhD. I also thank her for her helpful comments/corrections to the drafts, for bearing with my poor writing skills, for providing me with several opportunities to participate in public engagements and to attend conferences which improved my communication and presentation skills (still a lot more to learn), and for her support via skype even outside the working hours.

I would like to thank my second supervisor for his advice when I was struggling with the stability issue of one of the amplifiers and for being the third pair of eyes to verify the layouts before sending them out for fabrication.

I am grateful to workshop staff, Karl Rotchell and David Miller, for creating the metal bulk for the amplifiers and the plastic holders for the device, without which, I would have spent most of my time soldering and de-soldering the devices. Additionally, I thank them for creating a thermal platform which simplified the amplifier measurement. I thank EEE IT staff Fahmi Mohammad, Ian Wraith, and Thomas J Templeman for maintaining the license server of ADS and for their technical help to upgrade the RAM of my PC. I acknowledge the efforts of Dianne Webster in keeping the work environment safe and thank her for helping me whenever I am in need of advice. I would like to thank EEE administrative staff, especially Hilary Levesley and Frances Bright, for helping me with department formalities. I would like to thank EEE Finance staff and EEE Purchase staff for their effort to make the process of the expenses claim and the purchase of components/sundries simpler and faster.

A special thanks to my friend and colleague, Ashwani Kumar, for introducing me to my supervisor and being there to help me wherever required. I would like to thank my friend and colleague, Mirza Rasheduzzaman, for teaching me how to perform RF measurements and extraction process of RF Power transistors and for providing his data and programs for calibration against my own attempts. Thanks to my friend and colleague Xiaoyao Song and Peter Trend for their help in the cleanroom, especially during lab demonstrations. It is my pleasure to have met Dr Premlal Balakrishna Pillai, Asiel N Corpus Mendoza, Vineet Unni, Bhaskar Sen, and Zijiang Yang during my PhD with whom I shared wonderful moments. All

my friends, Sri Sai, Veerendra, Nitin, Joli, Pragya, Swaroop, and the list can go on with whom I shared wonderful moments.

Finally, no number of thanks are enough to express my gratitude for my mother, father, and brother for their unconditional love and support; The weekly call with them makes my life worthwhile.

List of Publications

Journals:

1. S. Faramehr, N. Poluri, P. Igic, N. Jankovic, and M. M. De Souza, "Development of GaN Transducer and On-Chip Concentrator for Galvanic Current Sensing," *IEEE Trans. Electron Devices*, pp. 1–6, 2019. (Authors N. Poluri and M. M. De Souza have worked on the simulation of on-chip flux concentrator and the authors S. Faramehr, P. Igic, and N. Jankovic have contributed to the simulation, fabrication and measurement of MagFETs)
2. N. Poluri and M. M. De Souza, "High-Efficiency Modes Contiguous With Class B/J and Continuous Class F^{-1} Amplifiers," *IEEE Microw. Wirel. Components Lett.*, vol. 29, no. 2, pp. 137–139, Feb. 2019.
3. N. Poluri and M. M. De Souza, "An Integrated On-Chip Flux Concentrator for Galvanic Current Sensing," *IEEE Electron Device Lett.*, vol. 39, no. 11, pp. 1752–1755, Nov. 2018.
4. N. Poluri and M. M. De Souza, "Investigation of the Effect of Weak Non-Linearities on P1dB and Efficiency of Class B/J/J* Amplifiers," *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 65, no. 9, pp. 1159–1163, Sep. 2018.

Conferences:

1. N. Poluri and M. M. De Souza, "A methodology to design broadband matching networks for continuum mode PAs," in Asia-Pacific Microwave Conference (APMC), 2019, pp. 1–3. (Oral Presentation)
2. N. Poluri and M. M. DeSouza, "SRFT based design of high efficiency broadband class BJF^{-1} power amplifiers," *The Future Power Challenge by Centre for Power Electronics*, 2019. [Online]. Available: http://www.powerelectronics.ac.uk/future-power-challenge/future-power-challenge.aspx. (Poster and Oral Presentations; Won 3rd position)
3. N. Poluri and M. M. De Souza, "CLASS BJF^{-1} : Simplifying the Design Methodology of RF Power Amplifiers," in *ARMMS*, 2019, no. April, pp. 1–7. (Oral Presentation)
4. N. Poluri and M. M. De Souza, "Class BJF^{-1} - A new class of amplifier for high efficiency and output power," in *Proceedings of 9th Wide Bandgap Semiconductors and Components Workshop, ESA, Harwell*, 2018, no. 1, pp. 141–148. (Oral Presentation)

5. S. Faramehr, N. Poluri, M. De Souza, P. B. Pillai, and P. Igic, “Integration of GaN Magnetic Sensors with Inductor for Galvanic Current Monitoring,” in *Centre for Power Electronics Annual Conference*, 2018. (Poster Presentation; Won 1st position)
6. M. Rasheduzzaman, N. Poluri, and M. M. De Souza, “Evaluation of Analytic Approach at Different Bias Points for Deep Class-AB Operation,” in *UK Semiconductors (UKS 2016) Sheffield, United Kingdom*, 2016. (Poster Presentation)

Glossary

Base-band data: A data generated form the UE which is yet to be modulated.

Basestation: A central hub to which all the UEs in the location are connected wirelessly.

Channel Access Schemes: This refers to the multiple access techniques which are required to coordinate the sharing of a communication channel by all the users.

Channel fading: Due to the reflection of the signal from various objects in the path and varying channel properties due to weather, the transmitted signal is never constant at a given location. This variation of signal with time is referred to as channel fading.

Class A power amplifier: The transistor for this class of amplifier is biased such that the quiescent drain current is half of the maximum drain current from the device. Both the current and voltage waveforms of this class are sinusoid.

Class AB power amplifier: The transistor in this class of amplifier is biased such that the quiescent drain current is lower than the half of the maximum drain current from the device. The voltage waveform of this class is sinusoidal.

Class B power amplifier: The transistor in this class of amplifier is biased such that the quiescent drain current is close to zero. The voltage waveform of this class is sinusoid and the current waveform is half sinusoidal.

Class B/J/J* continuum: Refers to the family of a continuum of voltage waveforms between the classes B, J* and J. The current waveform is half-sinusoidal.

Class C power amplifier: The transistor in this class of amplifier is biased such that the quiescent drain current is close to zero and the quiescent gate voltage is below the threshold voltage of the device. The voltage waveform of this class is sinusoid.

Class F power amplifier: In this class of amplifier mode, the current is half sinusoidal and the voltage is tuned to a square waveform obtained by presenting a short for even harmonics and open for odd harmonics.

Class F^{-1} power amplifier: In this class of amplifier mode, the current and voltage waveforms are shaped to a square wave and a half-sinusoid respectively by presenting a short to odd harmonics and an open to even harmonics.

Class J power amplifier mode: Class J mode is characterized by complex and capacitive impedances at the fundamental and second harmonic frequencies respectively. Both the current and voltage waveform are half sinusoidal and their fundamental components have a phase overlap of $\pi/4$ radian.

Class J* power amplifier mode: Class J* mode is characterized by complex and inductive impedances at the fundamental and second harmonic frequencies respectively. Both the current and voltage waveform are half sinusoidal and their fundamental components have a phase overlap of $\pi/4$ radian.

Cloud computing: Cloud computing refers to the situation where most of the data processing is performed with the network rather than the devices connected to the network. In this way, the devices need not be required to have very high computation power. Additionally, the data process can be performed only once and the consumption of power by the device reduces.

Continuous class F: In this class of amplifier, the current is half sinusoidal and a continuum to the voltage in class F which are obtained by a reactive load at the second harmonic frequency and complex load at the fundamental frequency.

Continuous class F^{-1}: In this class of amplifier, the voltage is half sinusoidal and a continuum of current waveform in class F^{-1} are obtained by a reactive load at the second harmonic frequency and complex load at the fundamental frequency.

Continuum modes: Classes of Amplifier which rely on the continua of voltage and/or current waveforms. Examples for continuum modes are CCF, CCF-1, and Class B/J/J* continuum.

DC IV of a transistor: Refers to the current from a transistor as a function of the gate and the drain voltages. Typically, for a power device, the current is obtained when the voltage at the gate and drain are pulsed ie., applied for a short duration.

De-embedding: the procedure to calculate the impedance at the intrinsic plane to corresponding to the impedances at the extrinsic plane of the device is referred to as de-embedding.

Doherty configuration: A Doherty architecture is designed with a combination of an amplifier, referred as the main or carrier amplifier with one or more auxiliary amplifier whose purpose to actively modulate the load impedance of main PA. The load impedances in the

Doherty configuration varies with the input power so that the main PA operates in saturation thereby achieving high efficiency for a range of power levels.

Embedding: Embedding is a process to calculate the impedances at the extrinsic plane corresponding to the impedances at the current generator plane.

Envelope tracking: The drain supply voltage of an amplifier is varied according to the input power to the amplifier such that the amplifier operates near saturation for the power level. This results in an improvement in the efficiency of the amplifier even at a low power level because of the reduced DC power consumption.

Extraction process: The process by which the approximate values of the parasitics used in this work are obtained.

GaAs: Gallium Arsenide; It is a compound semiconductor formed of Gallium and arsenic.

Galvanic current sensor: A sensor which converts the magnetic field into current or voltage. These devices use the deflection of the charges under the magnetic field.

GaN: Gallium Nitride; It is a compound semiconductor formed of Gallium and nitrogen.

Harmonically tuned amplifier: The harmonics from the device are considered for the design in this class of amplifier. The impedances that improve the amplifier are placed at harmonics.

HEMT: High electron mobility transistor or heterostructure FET; It is a field-effect transistor in which the conduction channel is formed at the interface of two materials with different bandgap.

Hybrid modes: The continuum of waveforms that exist between the two continuum modes are referred to as hybrid modes.

Insertion loss: Insertion loss quantifies the loss in the power of the signal as it propagates through a matching network.

Load line or Load cycle: The plot of the drain current with drain voltage is referred to as load cycle. If the load is resistive, the load cycle becomes a straight line passing through the bias point and is referred to as the load line of the amplifier.

Load-pull technique: In the load-pull technique, the load impedance presented to the device is swept through a range of values and the performance of the device (the output power, efficiency, etc.,) for each of the impedances is obtained.

Low noise amplifier: A low noise amplifier differs from a power amplifier is that it adds minimal noise to the signal.

Millimetre-wave technologies: The implementations which use the signal whose wavelength is in the range of millimetres ie., their operating frequency lie between 30 GHz and 300 GHz.

Multiple-input multiple-output: Signal is received by several antennas. The original signal is recovered processing the signal received by all the antennas.

Reflection coefficient: Reflection coefficient is defined as the ratio of reflected power to the incident power.

Series of continuous inverse modes (SCIM): A hybrid continuum contiguous with inverse class B/J continuum and CCF^{-1} is referred to as Series of continuous inverse modes.

Series of continuous modes (SCM): A hybrid continuum contiguous with class B/J continuum and CCF is referred to as a series of continuous modes.

TECR: Technology-related Empirical capacitance ratios (TECR)) is an algorithm to extract the extrinsic capacitances.

Transconductance: It is defined as the derivative of drain current with gate voltage. The term quantifies how effectively the gate voltage controls the drain current.

Up/down converter: This block changes the frequency of a carrier signal to a higher/ lower frequency.

A user equipment (UE): Any device that is capable of generating or receiving a signal. 3

Voltage Standing Wave Ratio (VSWR): When the waves travelling in forward and reverse direction superimpose over each other, a standing wave with crests and troughs appear. voltage standing wave ratio is referred to the ration of voltage at the crest to the voltage at the trough of a voltage standing wave.

Waveform engineering: In this approach, the impedances are chosen to obtain the voltage and current waveforms required for a class of amplifier.

Contents

Chapter 1: Introduction

1.1. Background

Mobile communications have developed tremendously from supporting voice calls in the first generation to support video streaming, video calls, and cloud computing in its fourth generation [1.1][1.2]. This development is due to improved modulation and channel access schemes, the improvement in the cellular network architecture, and the hardware capability of the network and mobile equipment. The first generation (1G) relied on frequency modulation with the user's voice signal separated in frequency (Frequency Division Multiple Access (FDMA)). The second generation utilized digital modulation schemes (such as Gaussian Minimum Shift Keying) and the user's data was separated in time (Time Division Multiple Access (TDMA)). The third (3G) and fourth (4G) generations use amplitude and phase modulation such as Quadrature Amplitude Modulation. In the former (3G), the users' data is modified based on an orthogonal code/s (a sequence of bits) assigned to them, such that several users utilize the same carrier frequency but their data can be separated based on the codes (referred to as Wideband Code Division Multiple Access). In the case of 4G, data from a user is divided into several streams and each stream is placed in orthogonal sub-carrier frequencies to mitigate channel fading (which occurs due to multi-path propagation of the wireless signal). Both the FDMA and TDMA schemes are employed in 4G. This evolution of the modulation and channel access schemes has improved frequency spectrum utilization and resulted in an improvement of data rates from 14.4 kbps in 2G to 200 Mbps or higher in 4G. The increase in data rate has resulted in several new applications, a few of them highlighted in Figure **1.1**.

The next-generation mobile communication system ie., 5G, is expected to deliver data rates higher than 4G with high-speed network connectivity in crowed locations with unlimited connected devices [1.3]. An example of this use case is a stadium or an open-air festival with a high density of mobile phones and wireless devices present for a limited time [1.3]. Sixth generation mobile communications (6G) represent even further evolution wherein flying base stations are proposed to tackle virtual reality, autonomous cars, aerial vehicles, and other applications that require high data rates with low latency of microseconds [1.4]. Additionally, while previous generations (1G - 4G) were intended to connect people, 5G will allow machine-to-machine communication [1.5][1.6].

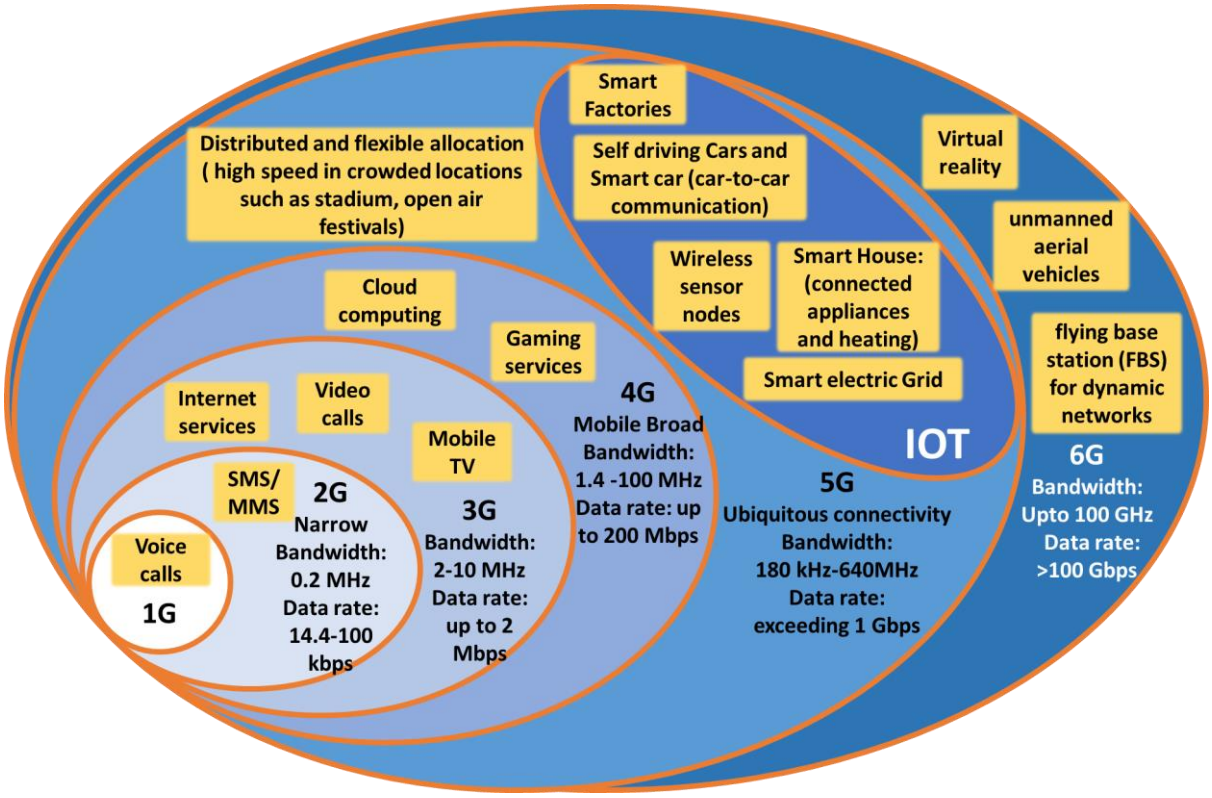

Figure 1.1: Infographics illustrating the applications enabled by the first to sixth generations of mobile network [1.2], [1.4]–[1.10]. The bandwidth in the figure includes carrier aggregation.

This new paradigm is often referred to as the "Internet of Things (IoT)" wherein a wide variety of devices (such as sensors, mobile phones, and actuators) communicate with each other to aggregate information for humans or Artificial intelligence (AI) to make informed decisions [1.11]. A few applications of the IoT are:

a) A smart home whose electrical appliances, fire alarm, and thermal management are connected to the network and can be remotely monitored and managed [1.12].
b) Smart factories in which equipment, machines, inventory, and people are connected. The aim is to enhance machine-machine collaboration for the creation of context-aware systems to minimize human error and human intervention in the production line. The second aim is to improve the human-machine collaboration by aggregating information from sensors, devices, machines, and people in real-time, to make informed and decentralized decisions [1.13]. This is often referred to as the industrial revolution 4.0 [1.13] and is envisioned to improve the productivity of factories [1.6].
c) In a smart grid, information regarding power generators (nuclear plants, coal plants, oil plants, wind turbines, and solar plants), electricity users (smart homes, industries, commercial users), and the power transmission network (transformers and transmission

lines) is collected from smart meters, sensors, and phase measurement units. This collected information is used to generate and deliver electric energy in an efficient, reliable, and sustainable manner [1.14].

d) A network of wireless sensor nodes can be deployed to detect forest fires and landslides to provide early warning or to monitor water pollution and air pollution. Each sensor node typically consists of one or more sensors, limited computation power, a transceiver, and/or an actuator. The network of sensor nodes works together to gather and compile measurement based on local decision processes and transmits the compiled information to the users via a mobile network [1.15][1.16].

e) Connected autonomous or self-driven cars, which make use of driver-assistive technologies such as cruise control, speed adaptation, and Vehicle-to-everything communication (vehicle-to-vehicle and vehicle-to-infrastructure) for collision avoidance, to improve road safety and fuel efficiency[1.17].

The data from and to the mobile phone or user equipment (UE) and IoT devices enter the cellular network via a basestation (BS). The block diagram of a BS is expanded in Figure **1.2** (a). For data transfer from the cellular network to the UE, a transmit path in Figure **1.2** (a) is used. In the transmit path, the base-band data/voice is upconverted to the RF signal and is then amplified by the power amplifier (PA). The amplified signal is radiated by an antenna or by multiple antennas (referred to as multiple-input multiple-output (MIMO)). MIMO minimizes the path loss between the base station and the UE. For the data received from the UE to the cellular network, the received RF signal from a UE by a BS is converted to the baseband signal via a receive path consisting of low noise amplifier (LNA) and power amplifier (PA), for amplifying the received signal, and a down converter to recover the baseband signal. The transmitter and receiver are referred together as a transceiver. The UE also consists of a similar transceiver but operates at lower power than the base station.

A robust cellular infrastructure is required to support high data rates. A simplified architecture of the backend 4G cellular network consisting of base-stations (BS), mobile switching networks, and data centers is shown in Figure **1.2** (b). The base-band data recovered from the UE is sent over to a mobile telephone exchange and routed via a core network (usually a network of fibers) as per the request of the mobile user. Each BS transmits and receives data/calls wirelessly from mobile phones (UE) located in a region, which is referred to as a "cell". Each cell assigned to a BS may further be divided into sub-regions referred to as sectors (typically 3 sectors) and the radio signal transmission and reception in each sector can be via

several antennas or antenna arrays. Depending on the number of sector and antennas, the base stations contain several transmitters and receivers.

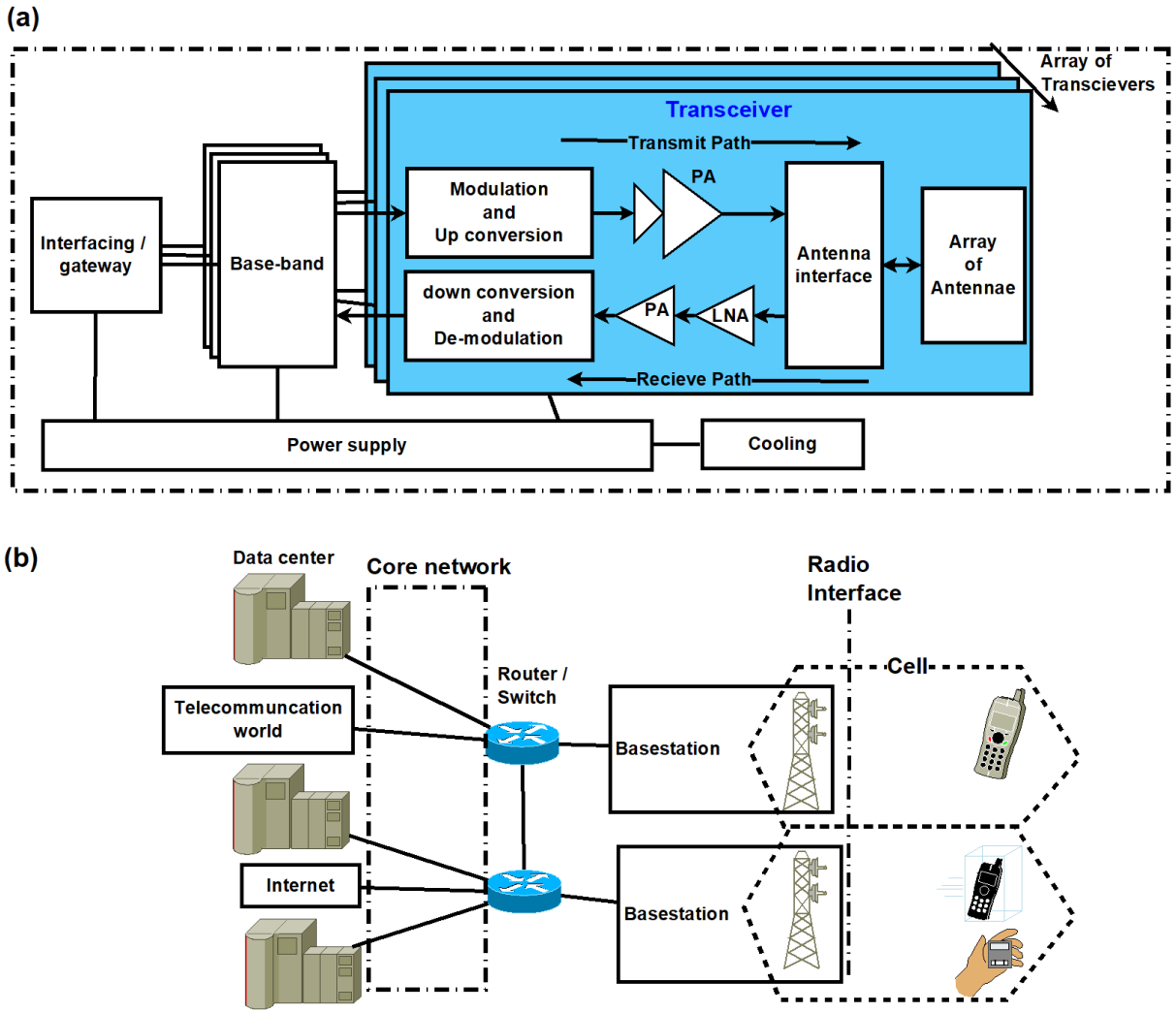

Figure 1.2: (a) The block diagram of a typical base station [1.18][1.19]. (b) A simplified architecture of a 4G network [1.20].

Base stations, based on their output power level, are categorized into wide-area BS (or Macro BS), medium-range BS (Micro BS), local area BS (Pico BS), and small BS (Femto BS) which are detailed in Table 1.1 [1.21]. Micro and Macro BS may be supported by several Pico and Femto BSs, each serving a small cell. The Pico and Femto BS are deployed in crowded areas to handle large data traffic.

By 2023, it is estimated that nearly an additional 5 billion wireless IoT devices will be connected to the 5G network [1.22][1.23]. Hence, each cell is expected to be connected to 50000+ devices [1.24]. To handle massive data coming from a large number of devices in the IoT and mobile phones, thousands of additional small cells (ie., Femto base stations) will be added to the existing cellular network rather than macrocells. Base-stations will employ

massive MIMO (greater than 128 antennae) to improve the spectral efficiency and millimetre-wave technologies to improve the bandwidth. This represents a shift in primary focus in the evolution of cellular networks; primary focus of evolution from 1G to 4G was the improvement of resource use (eg., spectrum via improving the modulation and channel access schemes) whereas 5G aims at improving both the cost and capacity of the resource deployment as well as resource use [1.25].

Table 1.1: Base Station rated carrier output power in 4G [1.21]

BS class	PA power range (Typical value)	Cell Type	Typical cell radius
Wide Area BS	20 W – 160 W (40 W)	Macro	>1 Km
Medium Range BS	2 W – 20 W (5 W)	Micro	250 m – 1 Km
Local Area BS	250 mW – 2W	Pico	100 m -300 m
Small BS	10 mW – 200 mW	Femto	10 m – 50 m

1.2. Motivation

The current cellular mobile network is estimated to consume 100 TWh of energy worldwide[1.26]. The percentage share of energy consumption of various components of the cellular network is shown in Figure **1.3** (a). Nearly 57% of the energy is consumed by base stations with the PA being the dominant consumer at 34 % to 67% of the base station power as highlighted in Figure **1.3** (b). Additional IoT devices and base-stations that will be added to the network to realize 5G will further increase the power consumption of the cellular network. The PA in a recently published state-of-the-art 5G transceiver consumes approximately 50% of the total transceiver's power [1.27]. Hence, minimizing the PA's energy consumption is critical for reducing the overall power consumption. Therefore, it must achieve the highest possible efficiency. This necessitates attention to methodologies to design highly efficient power amplifiers.

The continuous growth of cellular applications has led to the co-existence of multiple cellular standards such as 2G (GSM and EDGE), CDMA 2000, 3G, and 4G. Each of the wireless standards imposes a strict requirement on the linearity and output power of a transmitter over the operating bandwidth. The traditional one-radio-per-band architecture of the wireless transceivers, which uses a power amplifier (PA) for each band and wireless standard, is ineffective from the perspective of cost and form-factor. Another architecture, known as 'converged', employs PAs which cover multiple bands and support multiple standards thereby

increasing the interoperability and reducing the size and cost of transceivers [1.28]. This architecture requires amplifiers to meet the linearity and output power requirements over the desired broad range of frequencies. Broadband amplification will benefit not only future wireless communication systems such as WiMAX and 5G which use larger bandwidth to support increased data rates but also existing broadband systems such as radar and, environmental and climate monitoring (ECM).

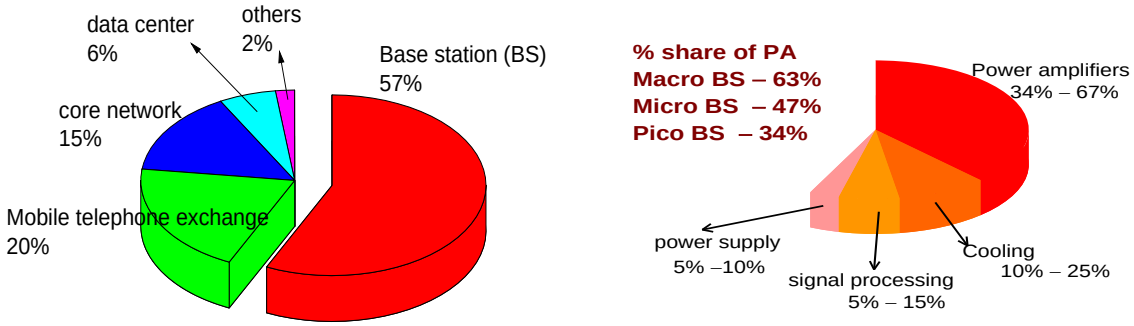

Figure 1.3: (a) Breakdown of energy consumption in cellular networks (excluding antennas) [1.29] (b) energy consumption of components in Base Station (excluding antennas) per antenna and sector [1.29][1.22].

Power amplifiers are categorized into classes that differ in operation and, hence, achieve different linearity, efficiency, bandwidth, and output power. Therefore, the choice of a particular class of operation is based on the requirement imposed by the application. The "conventional modes", viz. Class A, AB, B, C, F, and F^{-1}, require a specific load network, as shown in Table 1.2. On the other hand, continuous modes of amplifiers viz., class J, continuous class F, and continuous class F^{-1} can be designed for a range of impedances. The range of impedances available for the amplifier design has enabled the amplifier designed in these classes to demonstrate the potential to achieve efficient operation over a broad bandwidth, even spanning near or over octave frequencies [1.30][1.31]. In these classes of amplifiers, the second harmonic of the voltage or current is used to generate a set of efficient voltage and current waveforms. One of the focus of this research is "to design amplifiers with a high-efficiency using second harmonic manipulation".

In class J and continuous class F (CCF), the second harmonic of the voltage waveform is manipulated. Whereas, in continuous class F^{-1} (CCF^{-1}), the in-phase component of the current is completely removed and the quadrature component of the second harmonic component of the current waveform is manipulated. Continuum modes classes J and CCF^{-1} represent extremities with respect to the manipulation of the second harmonic component of the current;

in class J, the current remains unmanipulated whereas, in CCF^{-1}, the in-phase component is completely removed. Another drawback of class B/J continuum and CCF^{-1} is that they require a constant resistance or conductance component at the fundamental frequency which is difficult to achieve over a broad bandwidth. Hence it is desirable to explore the design space beyond these modes in amplifier design. Additionally, the amplifiers designed in classes B/J continuum and CCF have been reported to achieve high efficiency at back-off and 1dB compression and, to the best of our knowledge, the reason for this has remained unexplained.

TABLE 1.2: Load requirement of classes of amplifier

Class of operation	**Theoretical maximum efficiency**	**The requirement in load network**
Class A Class AB Class B Class C [1.40]	50% 50% - 78.5% 78.5% 78.5% - 100 %	Resistive load at f_0 and short at harmonic
Class F [1.28]	91 %	Resistive load at f_0, Short at $2f_0$, and open at $3f_0$
Class F^{-1}[1.28]	91 %	Resistive load at f_0, open at $2f_0$, and short at $3f_0$
Class J [1.40][1.41] Continuous class F [1.42]	78.5 % 91 %	any impedance from a wide range of complex loads with a constant resistive part at f_0, reactive loads at $2f_0$, and short at $3f_0$
Continuous class F^{-1} [1.43]	91 %	any impedance at f_0 from a set of a wide range of complex loads with constant conductance, reactive loads at $2f_0$, and open at $3f_0$

f_0 denotes the fundamental frequency

The performance of a power amplifier is sensitive to the fabrication process, applied drain voltage, and its operating temperature. In this context, monitoring the drain current of the power amplifier allow us to minimize the effect of these variations and optimize the performance of a power amplifier by adjusting the gate voltage to accommodate these variations [1.32]. Monitoring the drain current can allow to keep the power amplifier within its operating condition limits by controlling the gate and drain voltage. At the extreme, the power amplifier can be turned off; for instance, in the case of surges in the drain current that may damage the power amplifier. Additionally, monitoring the drain current will allow to ramp the drain voltage to counter for the effect of current collapse phenomenon typically demonstrated by GaN

HEMTs and the drain voltage can be modulated to improve the efficiency of the power amplifier (Figure 2.1 (a) in [1.33]); this technique is referred as envelope tracking.

In general, monitoring the current flowing through the critical sub-systems of an IoT device is desirable. This is because IoT systems are deployed in smart houses, connected autonomous vehicles (CAV), smart grid, and WSN have critical functionality and their failure may result in catastrophic consequences. For example, autonomous cruise control, early warning system, and autonomous emergency braking functionality of a connected autonomous vehicle depends upon the radar and 5G transceiver of the Vehicle-to-everything communication system [1.17] [1.34]. A failure of an FM radio or a GPS in a manually driven car does not lead to the loss of control whereas the hazard severity of the failure of autonomous cruise control is rated high [1.35]. Hence, these IoT systems need to be fault-tolerant. Condition monitoring, fault detection, and annunciation are required for the system to be fault-tolerant [1.36]; a way to accomplish this is by monitoring the current flowing through the critical connection in an IoT device.

Galvanic current sensors, such as the MagFET [1.37] and hall-effect sensors [1.38], detect the magnetic field generated by the current, without any direct electrical connection with the sensor. Such a non-invasive method can be employed for current monitoring in a wide range of applications [1.38]. Sensors could be placed close to a conductor carrying a current to be sensed, the current can be estimated based on the magnetic field from conductor line [1.39]. A focus of this work is to improve the magnetic field at the magFET for a given current flowing through the copper line.

1.3. Objectives

The objectives of this thesis are:

1) to explore the amplifier modes in which the in-phase component of the second harmonic frequency is partially removed.
2) to investigate the reason, for high efficiencies at P1dB and back-off power, and to utilize such knowledge to design an amplifier that demonstrates high efficiency and output power at 1dB compression.
3) to propose a structure to increase the magnetic field strength in a galvanic current sensor.

1.4. Organisation

This thesis is organised into seven chapters.

The basic concepts of power amplifiers are presented in Chapter 2. This chapter introduces the benefits of tuning harmonics. The theoretical background of the various continuum modes, which rely on the second harmonic manipulation, proposed in the literature is presented in this chapter.

Chapter 3 presents an extraction procedure to obtain the parasitic elements of a small signal equivalent circuit of a GaN HEMT. The parasitic components of the CGH40010 are extracted from the vendor model. This chapter reviews the basics of EM simulations and compares the ensuing result with the measurement of the amplifier. The extracted parasitics and EM concepts are utilized for the design of amplifiers in subsequent chapters of this thesis.

In Chapter 4, we present a formulation for new hybrid continuum modes which are contiguous with class B/J continuum and continuous class F. The output power and efficiency of these modes are analysed both in theory and in simulation using the Vendor model. A simple methodology to design an amplifier in this mode is presented. Two amplifiers are designed in the proposed mode and their measurement results are presented.

In Chapter 5, we have investigated the effect of weak non-linearities on the class B/J continuum. The analysis reveals that due to the combined effect of non-linear capacitances and the extrinsic parasitic elements at the drain terminal, a subset of class B/J continuum simultaneously achieves both high efficiency and linearity ie., P1dB (output power at 1dB compression). A design of an amplifier based on a waveform from this subset and its measurement results are presented.

In Chapter 6, a novel integrated on-chip flux concentrator for enhancing the magnetic field at a current sensor is presented. The dependence of the enhancement in the magnetic field from the two variants of a proposed flux concentrator viz., single and double loop on their length is analysed via simulations.

Finally, conclusions are drawn in Chapter 7. Possible extensions of this work are briefly discussed.

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Chapter 2: . Basics of RFPAs and the Review of Continuum Modes

2.1. Introduction

Classes A, AB, B, and C modes of amplification consider only the fundamental frequency in the design process. As explained in the previous chapter, the efficiency and bandwidth of an amplifier can be improved if the harmonics generated by the transistor are considered. The class J mode is an extended version of class B that relies on the second harmonic manipulation to achieve high efficiency over a larger bandwidth. A further improvement in efficiency in the continuous class F and F^{-1} amplifiers is achieved by considering up to the third harmonic in the design. This chapter contains a revision of the basic amplifier design concepts and a literature review on class J, continuous class F, and continuous class F^{-1} amplifiers. Before reviewing the class of amplifier, an active device i.e., a transistor, which is required to perform amplification is examined.

2.2. Overview of a Transistor

Because of mathematical simplicity, the analysis of an amplifier can be initiated with an ideal model of the transistor [2.1] whose DC drain current (I_d) vs. drain voltage (V_{ds}) (I-V) characteristics are shown in Figure 2.1 (a). In the figure, I_m denotes the maximum saturation current. The DC IV of the transistor can be divided into two regions: linear region below the knee voltage and saturation region above the knee voltage. The transistor needs to be operated within the physical limits imposed on the current and the voltage defined by the maximum saturation current (I_{max}) and breakdown voltage respectively. The quiescent voltage of a transistor (V_{dsq}) is typically 2-3 times smaller than the breakdown voltage. Within the saturation region, the transistor acts as a gate voltage (V_{gs}) dependent current source between the threshold (V_{th}) and saturation ($V_{gs(sat)}$) voltages shown in Figure 2.1 (b). The drain current I_d in this region is dependent on the gate voltage only as:

$$I_d = \begin{cases} 0 & V_{gs} < V_{th} \\ g_m(V_{gs} - V_{th}) & V_{th} \le V_{gs} < V_{gs(sat)} \\ g_m(V_{gs(sat)} - V_{th}) & V_{gs} \ge V_{gs(sat)} \end{cases} \quad (2.1)$$

Where, g_m is known as the transconductance defined as

$$g_m = \frac{dI_d}{dV_{gs}} \quad (2.2)$$

This relationship between the I_d and V_{gs} is known as transfer characteristics. It is shown in Figure 2.1 (c).

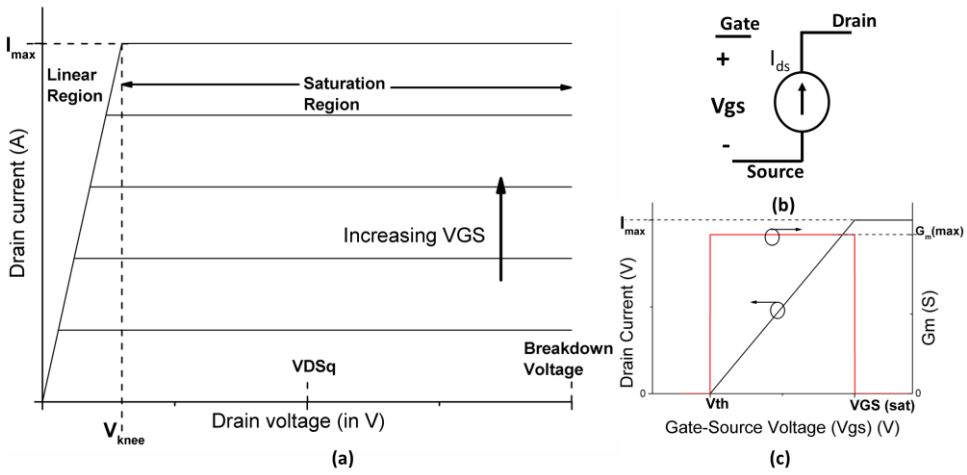

Figure 2.1: (a) IV of an ideal device (b) Equivalent of transistor operation in saturation region (c) Transfer characteristics of an ideal device.

The IV of a device can be represented as a product of the device transfer characteristics and the knee profile ($k(V_{ds})$) which represents a variation of the drain current with drain voltage as

$$I_d = \begin{cases} 0 & V_{gs} < V_{th} \\ k(V_{ds}) * g_m(V_{gs} - V_{th}) & V_{th} \leq V_{gs} < V_{gs(sat)} \\ k(V_{ds}) * g_m(V_{gs(sat)} - V_{th}) & V_{gs} \geq V_{gs(sat)} \end{cases} \quad (2.3)$$

The knee profile of an ideal device, which is often considered in amplifier analysis is given by

$$k(V_{ds}) = \begin{cases} 0 & V_{ds} < 0 \\ \dfrac{V_{ds}}{V_k} & 0 \leq V_{ds} < V_k \\ 1 & V_{ds} > V_k \end{cases} \quad (2.4)$$

Where, V_k denotes the knee voltage of the transistor.

On the application of a sinusoidal signal v_{gs} at the gate terminal of the transistor, the transistor generates an AC drain current (i_d), given by

$$i_d = g_m * v_{gs} \quad (2.5)$$

Because of this relationship, the applied input signal to the transistor is replicated at the drain of the transistor but with the amplitude magnified by the gain g_m.

However, a real transistor exhibits a non-linear relationship between the gate voltage and drain current due to nonlinear transconductance, nonlinear parasitic components, and clipping of current [2.1]. These effects result in harmonic generation leading the distortion of the current in an RF power amplifier.

1. **Nonlinear transconductance**: The gate voltages and drain currents in the saturation region are not linearly related, an example is illustrated in Figure 2.2 (a), and hence the

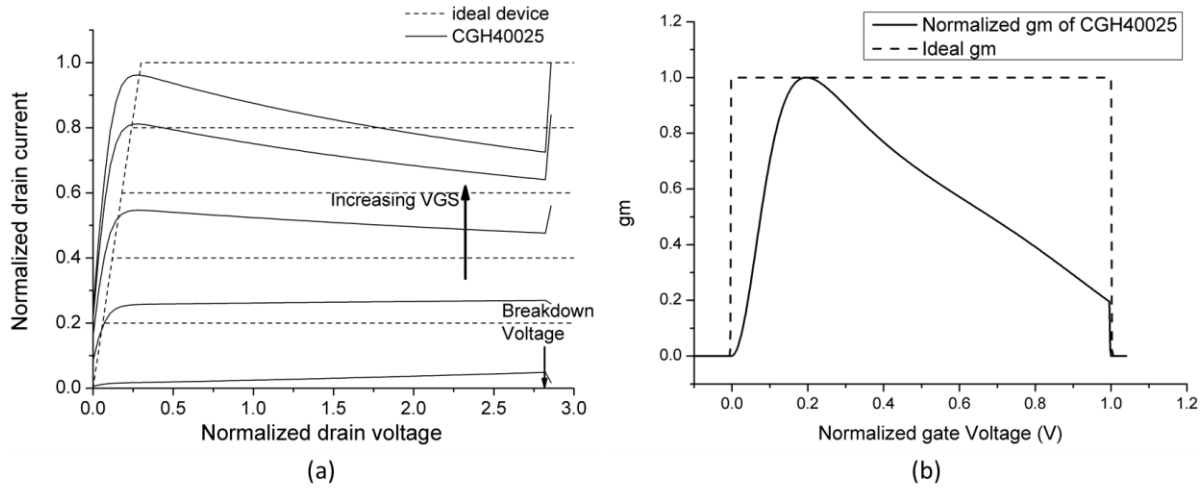

Figure 2.2: Comparison of (a) Normalized (to peak value) drain current vs normalized (to V_{DSq}) and (b) g_m (transconductance) normalized to peak value, of an ideal and a real device (CGH40025)

corresponding transconductance exhibits a non-linear relation with gate voltage as shown in Figure 2.2 (b). The nonlinear transconductance of the transistor can be modelled using the Volterra series as

$$I_d = \begin{cases} g_m V_{gs} + g_{m2} V_{gs}^2 + g_{m3} V_{gs}^3 + \cdots + g_{mn} V_{gs}^n + \cdots & V_{th} < V_{gs} < V_{gs}(sat) \\ 0 & otherwise \end{cases} \quad (2.6)$$

Where, g_{mn} denotes the Volterra coefficient of order n. The values of Volterra coefficients depend on the transistor and the bias conditions of the transistor. Because of this non-linear relationship between current and controlling gate voltage, the generated current also consists of multiple harmonics.

2. **Clipping of the current:** The current waveform clips when the input voltage goes below the threshold voltage or when the drain voltage goes below the knee voltage. In the former case, the efficiency of the amplifier improves due to a reduction in DC current component (quiescent current) flowing through the device, whereas in the latter case, the output power and linearity of the amplifier decrease due to a dip in the peak

of the current. A simulation using an ideal device is performed to illustrate the clipping of the current. From the current waveform in Figure 2.3, a large dip in the drain current can be observed even when the drain voltage goes marginally below the knee voltage of the transistor.

The knee profile of GaN and GaAs HEMTs can be approximated modelled in the polynomial form as [2.2]

$$k(V_{ds}) = \begin{cases} 0 & V_{ds} < 0 \\ \left(\frac{V_{ds}}{V_{dsq}}\right)^{N} & 0 \leq \frac{V_{ds}}{V_{dsq}} < 1 \\ 1 & \frac{V_{ds}}{V_{dsq}} > 1 \end{cases} \tag{2.7}$$

A major benefit of the N-model is that a closed-form expression for drain current in the knee region and the output power and efficiency at saturation can be derived. The approximate knee profile of the GaN device is obtained for $4 \leq N \leq 8$ whereas for GaAs $N \geq 24$ [2.2].

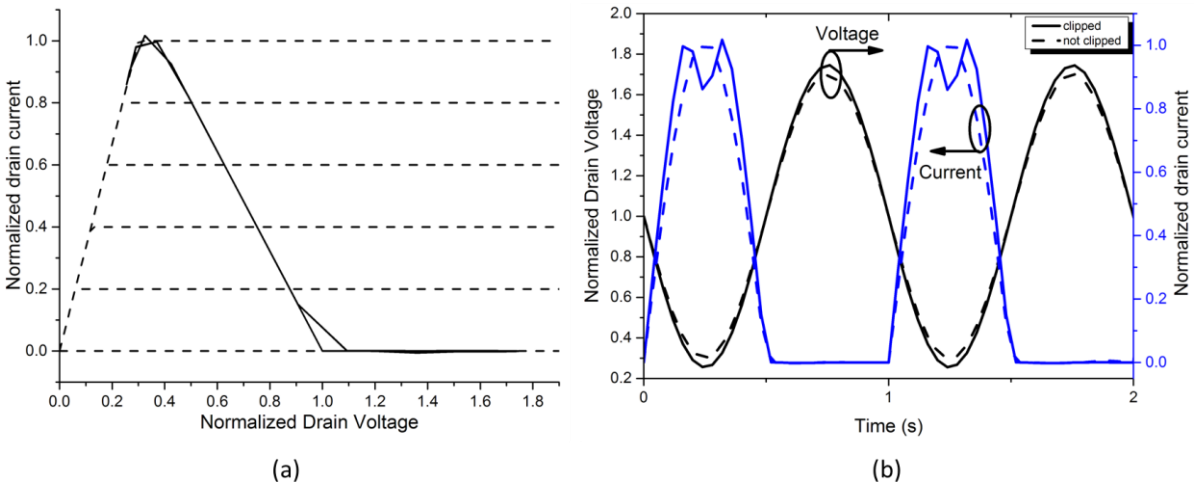

Figure 2.3: (a) Clipped drain current versus drain voltage (b) Voltage, and clipped and unclipped current waveforms.

This model of device IV is referred to as the N-model. IV for N=6 and N=24, which represents approximate IV of GaN and GaAs devices using N-model, are plotted in Figure **2.4**. It can be seen that GaN devices have a fairly deep knee region, as a result, the drain current will clip for a lower voltage swing in GaN than GaAs for a fixed quiescent drain voltage. General high-efficiency amplifier implementations keep quiescent current close to zero to achieve high efficiency and maintain the drain voltage above the knee voltage to achieve linearity.

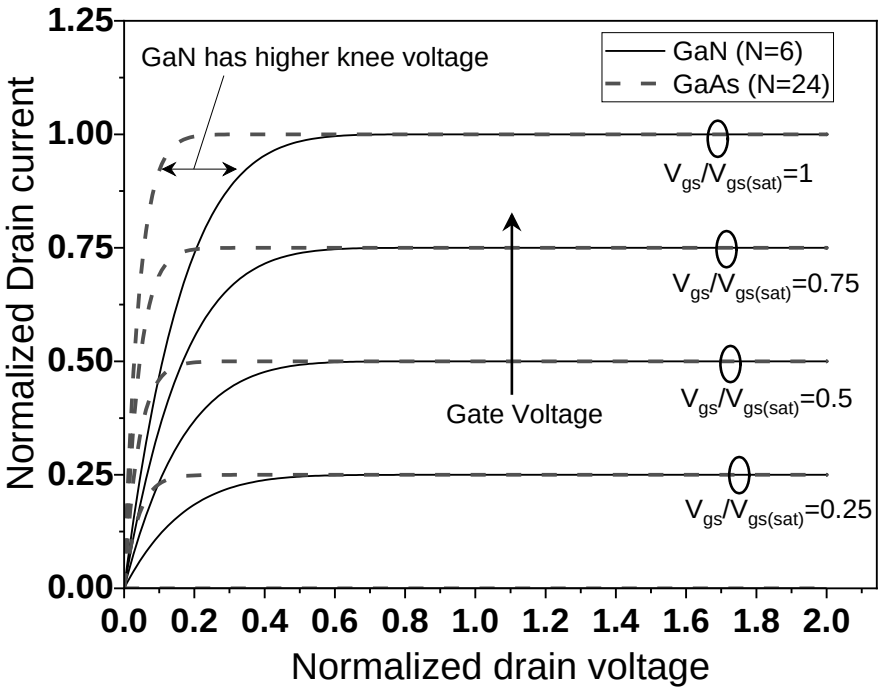

Figure 2.4: (a) Clipped drain current versus drain voltage (b) Voltage, and clipped and unclipped current waveforms.

3. **Nonlinear parasitic elements:** The parasitic effect arises due to the structure of the device. The equivalent circuit of the transistor[2.3]–[2.6] considering the parasitic effects is shown in Figure 2.5. Of these the drain-pad capacitance (C_{pd}), gate-pad

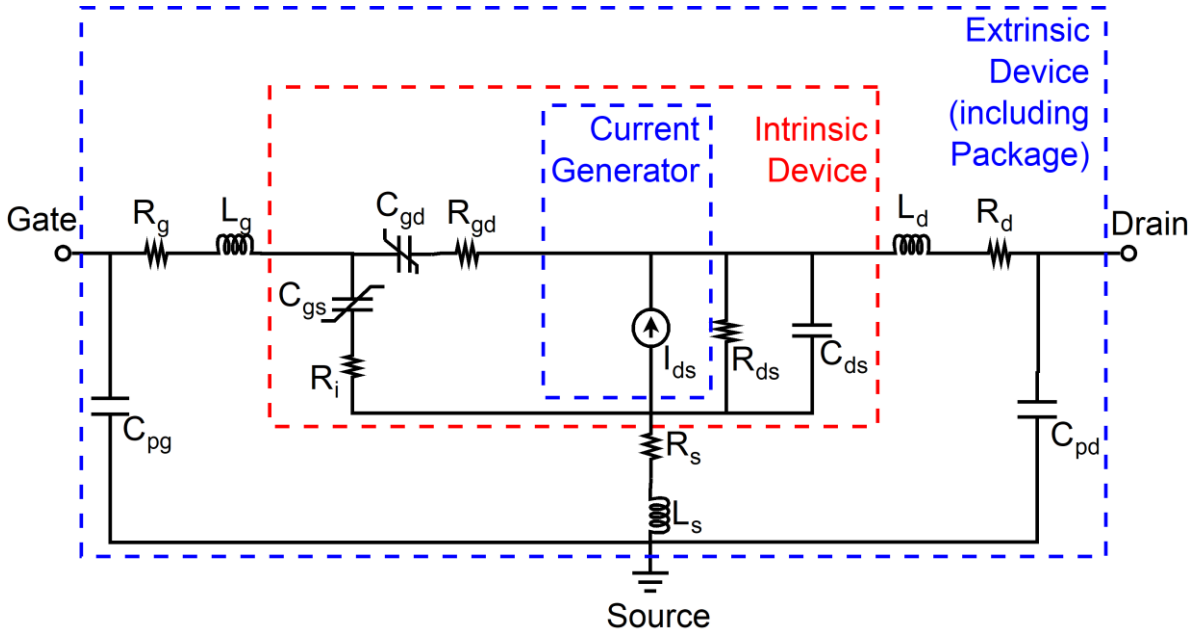

Figure 2.5: The equivalent circuit of the transistor

capacitance (C_{pg}), resistances (source (R_s), drain (R_d), and gate (R_g) resistances) and inductances (source (L_s), gate (L_g), and drain (L_d) inductances) are bias independent whereas the intrinsic capacitance (drain-source capacitance (C_{ds}), gate-source (C_{gs}), and gate-drain capacitance(C_{gd})), output conductance (g_{ds}), R_i, and R_{gd} are bias dependent. The value of intrinsic capacitances depends upon the instantaneous voltage across them leading to the generation of harmonics.

The device model of the transistor in Figure 2.5 is shown to be accurate only up to 6 GHz [2.7]. The accuracy of the model can be increased by additional elements to accurately model the parasitic effects in the device. 20-element [2.7] or 22-element [2.8] models of the transistor were shown to be accurate up to 20 GHz. Alternatively, the accuracy of the model can be increased by modelling the extrinsic parasitic effects originating from the metal lines at the gate, drain and source terminals and the package by transmission lines to account for their length rather than lumped components. The transmission line will model the phase variation along the fingers of a transistor, which are marked in Figure **2.6** (a). Hence, these models can accurately model transistor at frequencies higher than 100 GHz. An example of a distributed model is shown in Figure **2.6** (b). In this model, the transistor is modelled as an interconnect of n slices (cross-section) of a transistor. Each finger in a slice is modelled by the intrinsic model of the transistor with parasitic elements, similar to intrinsic device marked in Figure **2.5**. These intrinsic models are connected by 6 transmission lines; 2 transmission lines at gate, source, and drain terminals of the intrinsic device. The length and width of these transmission lines are dependent on the number of slices and the widths of gate, source and drain terminals of the transistor respectively. These transmission lines can be modelled by passive elements as well [2.9]. The gate and drain terminals of the device

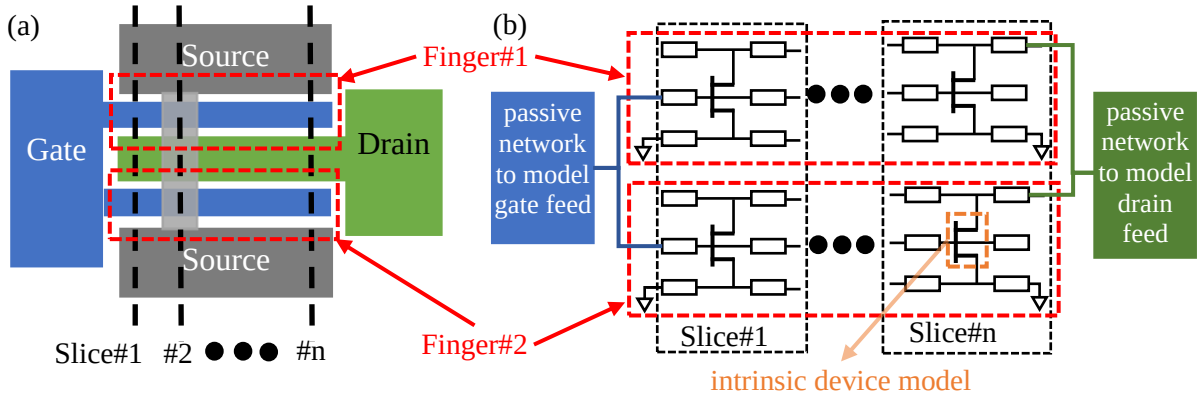

Figure 2.6: (a) Top view of a simplified layout of a GaN HEMT transistor (b) High frequency distributed model of the transistor [2.9]

to which the fingers connect are modelled by passive networks. This model was able to characterize the device up to 150 GHz [2.9] by using 8 slices. Similarly, the transistor is modelled in [2.10] as the interconnect of 3 sections; one section is the cross-section with air bridge (slice#2 in Figure **2.6** (a)) and the other two sections are on either side of the air bridge. This model was able to model a GaN HEMT up to 300 GHz.

2.3. Basics of an amplifier design

A typical design of an RF power amplifier is shown in Figure 2.7. The transistor is biased with the DC power supply at a pre-selected quiescent point of the transistor characteristic. The RF signal is superimposed on the quiescent bias of the transistor. The transistor requires appropriate impedances to be presented at its input and output, to obtain the required performance.

The input and output matching networks enable the maximum power transfer from the preceding (represented by a source in Figure 2.7) and succeeding (represented by a load in Figure 2.7) components respectively. The input matching network is designed such that it presents the required impedance (which maximizes output power/efficiency/gain) at the gate terminal of the transistor and minimizes the mismatch between the source and the amplifier ie., the reflection coefficient of the source (Γ_{SS}) and the input reflection of the amplifier (Γ_{in}) are conjugates of each other (ie., $\Gamma_{SS} = \Gamma_{in}^{*}$). Similarly, the output matching network presents optimal impedance at the drain terminal of the device and $\Gamma_{LL} = \Gamma_{out}^{*}$, where Γ_{LL} and Γ_{out} denote the reflection coefficient of the source and the output reflection of the amplifier respectively.

Apart from achieving the required matching, it is desirable for the matching network to achieve minimal insertion loss and the required quality factor (Q). The insertion loss (IL) quantifies the loss in the power of the signal as it propagates through a matching network and is defined as

$$IL = \frac{P_{Mout}}{P_{Min}}, \tag{2.8}$$

where, P_{Mout} and P_{Min} are the input and output power of a matching network.

The quality factor of a matching network is defined as

$$Q = \frac{f_0}{BW}, \tag{2.9}$$

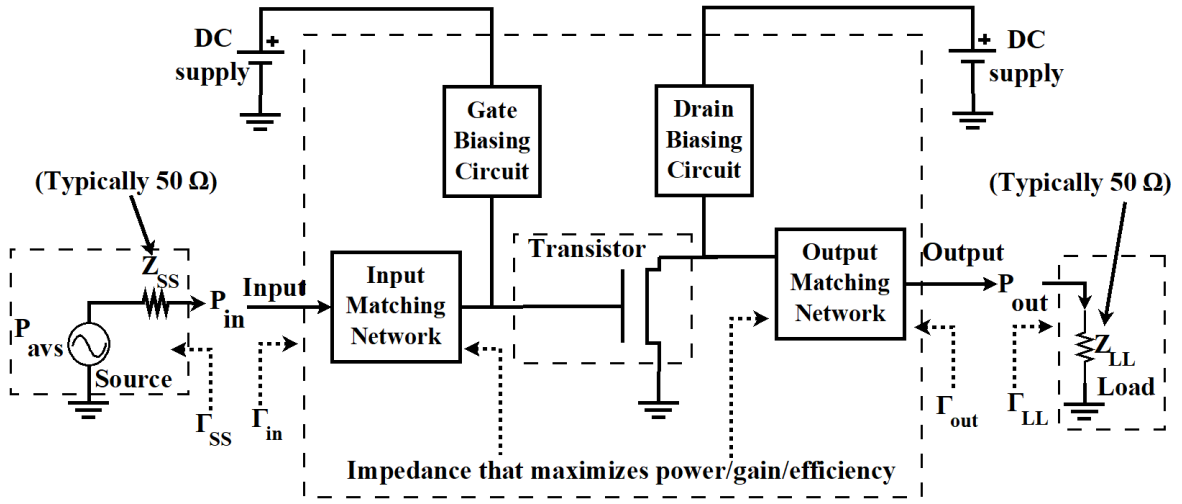

Figure 2.7: A block diagram of a typical single-stage RF power amplifier

where, f_0 and BW denote the centre frequency and bandwidth of the matching network respectively. A low Q matching network is desirable as it will demonstrate a larger bandwidth. In addition, a low Q will result in a low voltage standing wave ratio (VSWR) leading to lower heat dissipation within the matching network. To decrease Q, the number of components used in a matching network needs to be increased. On the other hand, as the number of components increases, the insertion loss of a matching network increases. Hence, the choices matching network topology and the number of components is dictated by the inherent trade-off between IL and BW.

If $\Gamma_{SS} \neq \Gamma_{in}^*$, the power delivered to the amplifier at the input from the source (P_{in}) is only a portion of the available power from the source (P_{avs}). Similarly, in case $\Gamma_{LL} \neq \Gamma_{out}^*$, only a portion of the power generated from the amplifier will be delivered to the load (the delivered power to load is denoted by P_{out} in Figure 2.7). Transducer power gain which takes into account the mismatch from the source and load is typically used for characterizing the amplifier and defined as[2.11]

$$G_T = \frac{P_{out}}{P_{avs}} \tag{2.10}$$

How efficiently the overall amplifier circuit performs power amplification can be defined by

$$Drain\ efficiency(\eta) = \frac{P_{out}}{P_{dc}} \tag{2.11}$$

$$Power\ Added\ efficiency\ (PAE) = \frac{P_{out}}{P_{dc}}\frac{(G_T - 1)}{G_T} \tag{2.12}$$

Where, P_{dc} denotes the DC power consumed by the amplifier. PAE takes into account the input power to the transistor and hence is a more accurate measure of efficiency than drain efficiency. The efficiency of the amplifier depends on the impedances presented to the transistor and losses in the matching networks.

The nonlinear transconductance and nonlinear parasitic components of the transistors generate relatively small harmonic components than current clipping, hence these are regarded as weak nonlinear effects compared to the clipping of current [2.1][2.12]. Under the cumulative effect of the nonlinearities of the transistor, applying a single tone sinusoid at the gate of the transistor leads to harmonics in the current waveform as

$$I(\theta) = I_{DC} + \sum_{n=1}^{\infty} \left(I_{ni} \cos(\mathrm{n}\theta) + I_{nq} \sin(n\theta) \right) \tag{2.13}$$

Because of the spreading of the power in the harmonics, the gain of an amplifier decreases. The output power levels at which the gain is 1dB (P1dB) and 3dB (P3dB) less than its value at a small signal are called 1dB compression point and 3dB compression point respectively. P1dB is generally chosen as the metric of linearity of an amplifier because of the large harmonic content in the output voltage and current waveform beyond this power level. P3dB is the metric of the output power of the amplifier at saturation.

Another important criterion for an amplifier is unconditional stability which indicates that the amplifier will not demonstrate an unconstrained increase in its output power even when input power is fixed or when no input is applied. The reason for the amplifier instability can be understood by representing the amplifier in terms of scattering parameters of the transistor and matching networks as shown in Figure 2.8. For example, the output power from the device (P_o) will get reflected from the load matching network, denoted by R in Figure 2.8. R will be fed back at the input of the transistor if $S_{T12} \neq 0$ and this power will be reflected by the input matching network and amplified by the device by a factor S_{T21} , contributing to P_o. If this contribution from R increases P_o, this increase will lead to an increase in R which in turn leads to further increase in P_o. This amplification of reflections due to mismatches at the gate and drain terminals of the device due to forward (S_{T21}) and reverse (S_{T12}) gain of the device will eventually lead to an uncontrolled increase in P_o and destruct the transistor.

The conditions of the unconditional stability that must be satisfied are:

1) The magnitude of the reflection coefficient at the input plane of the device with output matching network connected, denoted by S'_{T11} in Figure 2.8, should be less than 1 ie., $|S'_{T11}| < 1$. S'_{T11} is given by

$$S'_{T11} = S_{T11} + \frac{S_{T21}S_{T12}\Gamma_o}{1 - S_{T22}\Gamma_o} \tag{2.14}$$

2) The magnitude of the reflection coefficient at the output plane of the device with input matching network connected, denoted by S'_{T22} in Figure 2.8, should be less than 1 ie., $|S'_{T22}| < 1$. S'_{T22} is given by

$$S'_{T22} = S_{T22} + \frac{S_{T21}S_{T12}\Gamma_I}{1 - S_{T11}\Gamma_I} \tag{2.15}$$

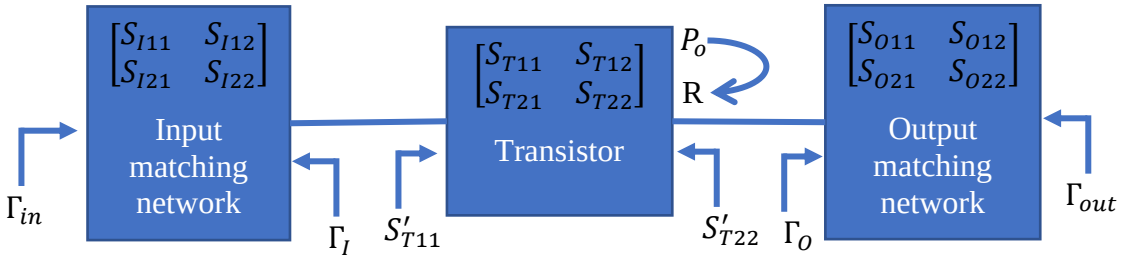

Figure 2.8: An S-parameter representation of a single-stage RF power amplifier

Γ_o and Γ_I which satisfy the conditions in (2.14) and (2.15) respectively needs to be selected for the design of the amplifier. A closed-form solution for Γ_o and Γ_I exist and are referred as "stability circles" [2.11]. The stability condition needs to be satisfied at all frequencies not just at the design frequency. Much of the design process of the amplifier revolves around finding optimal impedances to achieve the required performance while achieving stability.

2.4. Amplifier classes A, AB, B, and C

The amplifiers can be categorized into classes A, B, AB, and C based on their Quiescent operating point and these classes are introduced in the following subsections. These classes form the basis for the other amplifier classes, introduced later in the thesis, which differ in the way the harmonics are considered in amplifier design.

2.4.1. Class A

Biasing the gate halfway between the V_{th} and $V_{gs(Sat)}$ maximizes the linear output power of the amplifier by avoiding the clipping of current. Quiescent drain current flowing through the transistor is $I_{max}/2$ at this gate bias. Since the main aim of designing a power amplifier is to

maximize the output power at the load at the fundamental frequency only, it would seem obvious that all the harmonics should be shorted. The load at the fundamental frequency should be resistive because it has the highest power factor. Such a bias and load condition is referred to as Class A mode.

The maximum current waveform flowing through the device can then be written as

$$I_d = \frac{I_{max}}{2} + \frac{I_{max}}{2}\cos(\theta) \tag{2.16}$$

The maximum swing allowed by the drain voltage is

$$V_{ds} = V_{dsq} - \left(V_{dsq} - V_k\right)\cos(\theta) \tag{2.17}$$

The optimal load resistance that will have the voltage swing given in equation (2.17) when the current given in equation (2.16) flowing through it is [2.1]

$$R_{opt} = \frac{2\left(V_{dsq} - V_k\right)}{I_{max}} \tag{2.18}$$

The efficiency of this amplifier can be calculated as

$$\eta_A = \frac{V_{dsq} - V_k}{2V_{dsq}} \tag{2.19}$$

This class of amplifier can at the most achieve 50% efficiency, which is achieved when $V_k = 0$.

2.4.2. Reduced conduction angle modes: Classes AB, B, and C amplifiers

The efficiency of the amplifier can be increased either by reducing the DC power consumption at a constant output power or by increasing the output power while keeping the DC power constant. A general approach to increase efficiency is by reducing the DC power consumed by the transistor, without affecting output power. One method is to reduce the DC bias of the transistor, as in the case of the reduced conduction angle modes viz., class AB, class B and class C [2.1][2.13].

The transistor is assumed to be biased at the quiescent drain to source and gate to source voltages of V_{DSq} and V_{GSq}, respectively with a drain current of I_{DSq}. The idea is to reduce the DC power consumption by reducing the quiescent drain current flowing through the device. Based on the gate voltage (V_{GSq}) of the transistor, amplifiers are classified into classes AB, B,

Table 2.1: classical reduced conduction angle modes

Class of amplifier	V_{GSq}	I_{DSq}
Class AB	$V_{th}<V_{GSq}<V_{GSsat}/2$	$0<I_{DSq}<I_{max}/2$
Class B	V_{th}	0
Class C	$V_{GSq}<V_{th}$	0

and C [2.1][2.14] as shown in Table 2.1. Since the gate bias of classes AB, B, and C is close to the threshold voltage, the device conducts only for a portion of a complete input cycle (2π) which is denoted by the conduction angle (α). α can be calculated as

$$\alpha = 2\cos^{-1}\left(\frac{I_{dsq}}{I_{max}}\right) \tag{2.20}$$

The optimum resistive load should maximize both the voltage and current swing, thereby the output power. The maximum current is limited to I_{max} and minimum voltage to V_k. The current waveform can be computed as

$$\begin{aligned} I_{ds}(\theta) &= \begin{cases} I_{dsq} + I_{max}\cos(\theta), & -\frac{\alpha}{2} < \theta < \frac{\alpha}{2} \\ 0, \ otherwise \end{cases} \\ &= I_{dc} + I_1\cos(\theta) + \cdots + I_n\cos(n\theta) + \cdots \end{aligned} \tag{2.21}$$

Where,

$$I_{dc} = \frac{I_m}{2\pi}\frac{2\sin\left(\frac{\alpha}{2}\right) - \alpha\cos\left(\frac{\alpha}{2}\right)}{1-\cos\left(\frac{\alpha}{2}\right)} \tag{2.22}$$

$$I_1 = \frac{I_m}{2\pi}\frac{\alpha - \sin(\alpha)}{1-\cos\left(\frac{\alpha}{2}\right)} \tag{2.23}$$

$$I_n = \frac{I_m}{\pi\left(1-\cos\left(\frac{\alpha}{2}\right)\right)}\int_{-\frac{\alpha}{2}}^{\frac{\alpha}{2}}\left(\cos(\theta)-\cos\left(\frac{\alpha}{2}\right)\right)\cos(n\theta)\,d\theta \tag{2.24}$$

The voltage waveform will be sinusoidal because the harmonics are shorted.

$$V_{ds}(\theta) = V_{dc} - (V_{dc} - V_k)\cos(\theta) \tag{2.25}$$

The voltage and current waveforms of these classes are plotted in Figure **2.9** (a). Since the load is purely resistive, the current and voltage are in phase and the plot of the drain current with drain voltage is a straight line, passing through the bias point. This line is known as the load line of the amplifier. The load lines of these classes of amplifier are shown in Figure 2.9 (b).

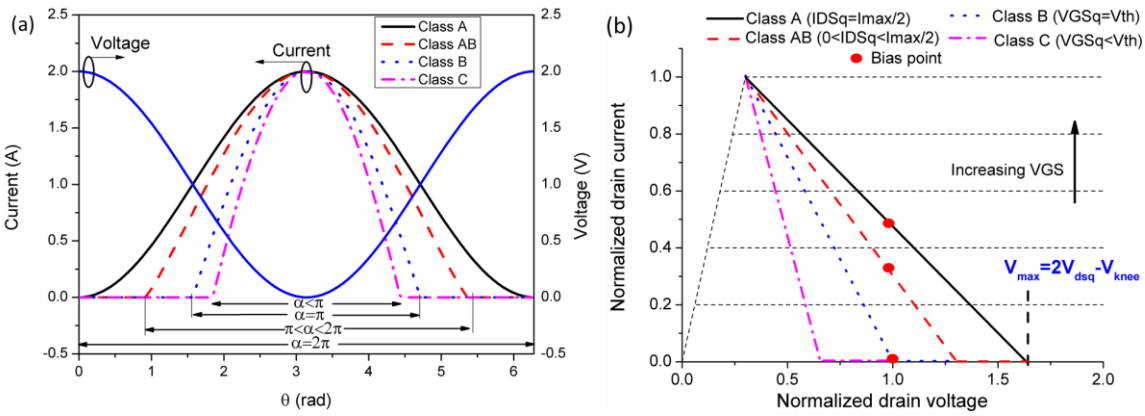

Figure 2.9: (a) The Current and Voltage waveforms in reduced conduction angle modes (b) Load line of the class A, AB, B, and C amplifiers superimposed on the IV of the transistors

The efficiency and output power can be obtained as [2.1]

$$P_{out} = \frac{(V_{dc} - V_k)I_1}{2} \tag{2.26}$$

$$\eta_B = \frac{P_{out}}{P_{dc}} = \frac{\pi(V_{dc} - V_k)I_1}{2V_{dc}I_{dc}} \tag{2.27}$$

The output power and efficiency of Class A, AB, B, and C are shown in Figure 2.10. Class A demonstrates the highest linearity because of the sinusoidal current waveform but has the least efficiency. At the other extreme, class C has the highest efficiency but, has the output power and linearity less than that of class A [2.1]. Classes AB and Class B have efficiencies in between those of classes A and C at the same output power as class A. Hence, the "deep" class AB (V_{GSq} near to V_{th}) and class B are preferred as they represent the trade-off between output power and efficiency, but if linearity is taken into account, class AB prevails. The maximum efficiency that can be achieved by class B mode is $\frac{\pi}{4}$ (≈78.5%) which is achieved if $V_k = 0$[2.1].

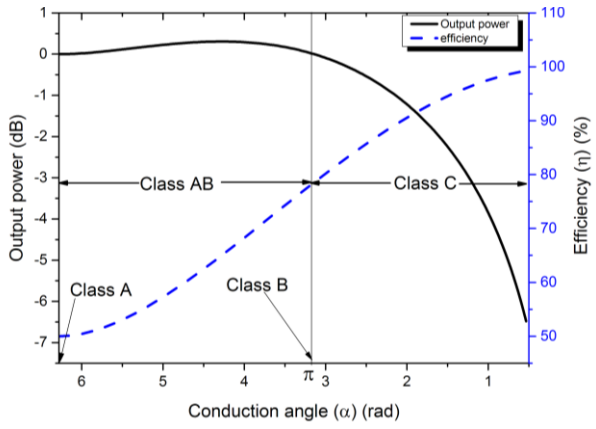

Figure 2.10: Output power and Efficiency under a reduced conduction angle (α) [2.1]

2.5. Tuning of harmonics

The clipping of the current cannot be avoided because, with an increase of input power, the drain voltage swing increases and output voltage goes below the knee voltage. However, the input power at which this happens in the reduced conduction angle mode can be increased by placing appropriate impedances at the harmonics of the current given in equation (2.13), thereby improving the linear output power of an amplifier [2.1]. This also leads to an efficient set of non-overlapping voltage and current waveforms to reduce DC power consumption.

The complexity of the matching network grows with an increase in the required number of harmonic terminations. Moreover, the drain-source capacitance (C_{ds}) presents a low impedance to higher harmonics making them difficult to tune. Hence, generally, up to the third harmonic is considered to be practically feasible [2.15], [2.16]. Even though, tuning harmonics improves the efficiency, because of the large combination of fundamental, second and third harmonics, obtaining the impedances required for an amplifier requires time-consuming load-pull/source pull simulations or measurements [2.17]. Such an approach lacks any generalized procedure to look into the trade-off between efficiency, linearity, and bandwidth.

The most general approach is to formulate an efficient set of voltage and current waveforms, based on which impedances can be calculated. In the following section, we illustrate a formulation for the manipulation of the second harmonic of the voltage.

2.6. Manipulation of the second harmonic of voltage

The main purpose of the second harmonic component is to increase the magnitude of the fundamental component. The minima and maxima of the voltage can be increased by adding the second harmonic in phase with the fundamental component as shown in Figure 2.11 (a). The minima can be restored to the edge of saturation by increasing the fundamental component, as shown in Figure 2.11 (b), via an increase in the magnitude of the load impedance.

The second harmonic will also effectively flatten the voltage in half the cycle and will increase the peak in the remaining half of the cycle. Flattening the lower half of the cycle can reduce the knee interaction whereas the peaking in the second half of the cycle has minimal effect on the performance, as long as the peak is below the breakdown voltage of the transistor.

The second harmonic manipulated voltage can be written as [2.18]

$$V_{ds}(\theta) = V_{dc} - \delta(k_2)(V_{dc} - V_k)\cos(\theta) - \mathrm{k}_2\delta(k_2)(V_{dc} - V_k)\cos(2\theta) \tag{2.28}$$

Where, $\delta(k_2)$ is the gain in voltage over a un-manipulated waveform, given in equation 2.25, and k_2 controls the magnitude of the second harmonic voltage. The output power ($P_{out|m}$) and efficiency (η_m) of the second harmonic manipulated voltage can be given as

$$P_{out|m} = \delta(k_2) P_{out|B} \tag{2.29}$$

$$\eta_m = \delta(k_2) \eta_B \tag{2.30}$$

The output power and efficiency will be higher than in class B as long as $\delta(k_2) > 1$ which can be achieved if $k_2 \in \left(-\frac{2+\sqrt{2}}{4}, 0\right)$ [2.18]. The maximum value of $\delta(k_2)$ is $\sqrt{2}$ which is obtained at $k_2 = -\frac{\sqrt{2}}{4}$.

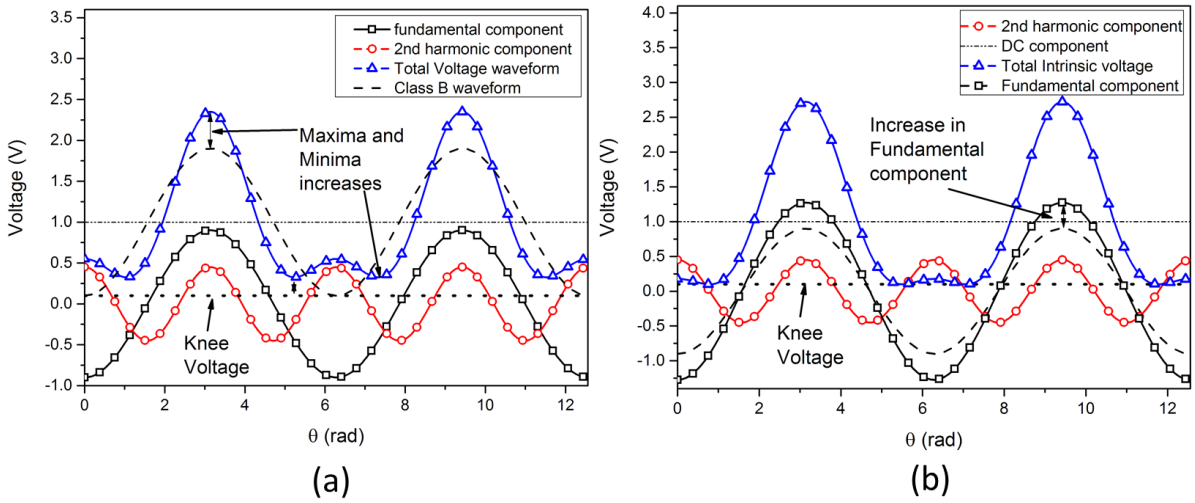

Figure 2.11: (a) The effect of addition of second harmonic on class B voltage waveform (b) The increase in the fundamental component due to second harmonic.

However, to generate the voltage waveform as given by equation 2.28, with the current waveform in equation 2.21, requires a purely resistive load at the second-harmonic. The termination to second and higher harmonics needs to be reactive so that no power is delivered at these harmonics. Possible ways to achieve this manipulation are:

1) The second harmonic of the drain current can be phased with respect to that of the drain voltage using the harmonic generation property of the nonlinear input capacitance [2.18].
2) It can be observed that equation 2.28 is restricted to the in-phase second harmonic component. A relevant phase shift in the fundamental component of the voltage can be introduced based on the magnitude of the second harmonic component. Such a mode of the power amplifier is called as class J [2.1].

The first solution is less versatile than the second, as it depends on an uncontrollable harmonic generation of input capacitance. Whereas the second method can be easily implemented by proper termination at the output. This approach is discussed in the following section.

2.7. Class J and class B/J/J* continuum

The starting point of a class J PA is to bias the device either in deep class AB or in class B. Class J mode is characterized by complex and reactive impedances at the fundamental and second harmonic frequencies respectively. This contrasts with conventional classes where the load is purely resistive at the fundamental frequency.

The current is half-sinusoidal as in the case of class B. Since the second harmonic is terminated by a reactive load, the phase difference between the second harmonic component of voltage and current needs to be $\pm\frac{\pi}{2}$. The complex impedance at the fundamental frequency introduces a quadrature component to the voltage waveform. The voltage across the drain and source can be defined as

$$V_{ds} = V_{DC} + V_{1q}\sin(\theta) + V_{1i}\cos(\theta) + V_{2q}\sin(2\theta) \tag{2.31}$$

Where, V_{1q} and V_{2q} are the quadrature components of voltage at fundamental and second harmonic frequencies respectively, and V_{1i} is the in-phase component of voltage at the fundamental frequency. It can be observed that the magnitude of the quadrature-phase of the fundamental voltage component (V_{1q}) adds another degree of freedom to the voltage waveform given in equation (2.28), which is controlled by the complex load at the fundamental frequency.

The V_{ds} in equation (2.22) should satisfy the following conditions:

a) For the linear operation of the amplifier, V_{ds} should remain above the knee voltage to avoid clipping of the current waveform. The clipping of current leads to a drastic reduction of output power and efficiency.
b) The in-phase component (V_{1i}) of the voltage should be maximized to increase the output power and efficiency of the amplifier.

The analysis presented in [2.1],[2.19], [2.20] reveals that the efficiency of class B can be achieved if the phase of the fundamental component is properly adjusted based on the magnitude of the second harmonic. The closed-form expression for the voltage obtained in [2.21] is

$$V_{ds} = V_{DC} - (V_{DC} - V_k) * (\cos(\theta) + \alpha \sin(\theta)) + \frac{\alpha}{2}(V_{DC} - V_k)\sin(2\theta) \tag{2.32}$$

Where, $\alpha \in [-1,1]$.

The current and voltage waveforms of Class B/J/J* continuum (or Class J[1]) are plotted in Figure 2.12. It can be observed that α=0 corresponds to class B. The voltage swing in class J ($\alpha = 1$) is much higher than in class B because of the considerable second harmonic component in the voltage waveform.

Since the in-phase component is independent of α, the output power and efficiency are the same for the family of voltage waveforms, which can be calculated as

$$P_{out|J} = \frac{(V_{dc} - V_k)I_m}{4} = P_{out|B} \tag{2.33}$$

$$\eta_J = \frac{P_{out|J}}{P_{dc}} = \eta_B \tag{2.34}$$

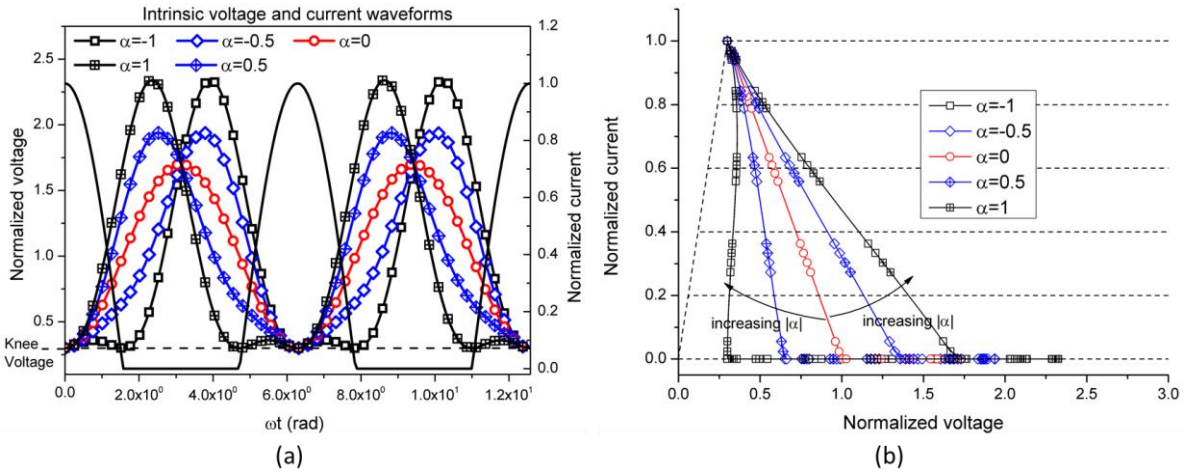

Figure 2.12: (a) Class B/J/J* continuum voltage and current waveforms for α=1,0.5,0,-0.5, and -1. The waveforms for α=0 correspond to class B. The peak of the voltage increases with an increase in the magnitude of α, and asymptotically tends to a half sinusoid for $\alpha = \pm 1$. (b) Loadlines of class J amplifier for α=1,0.5,0,-0.5, and -1. A spreading of the loadline of class J amplifier can be observed.

Each of these waveforms, given in equation (2.32), requires a specific set of fundamental and second harmonic impedances. The impedance required to maintain the voltage and current waveforms given in equations (2.32) and (2.21) can be calculated as

$$Z_{fund} = \frac{(V_{DC} - V_{knee})}{\frac{I_m}{2}}(1 + j\alpha) = R_{opt} + j\alpha R_{opt} \tag{2.35}$$

[1] Even though the initial definition of class J corresponds to α=1, following research papers refer to this family of waveforms as class J

$$Z_{sec} = -j\frac{\frac{\alpha}{2}(V_{DC} - V_{knee})}{\frac{2I_m}{3\pi}} = -j\frac{3\pi\alpha}{8}R_{opt} \tag{2.36}$$

Where, $R_{opt} = \frac{2(V_{DC}-V_{knee})}{I_m}$ is the optimal load line resistance of class B for maximum linearity [2.1]. The set of fundamental and second harmonic impedances in equations (2.35) and (2.36) are plotted in Figure **2.13**. The substantial second harmonic component, due to the reactive component at the load is balanced by the reactive component at the fundamental load and the reactive components of fundamental and second harmonic load are related as

$$\frac{\Im m\{Z_{sec}\}}{\Im m\{Z_{fund}\}} = \frac{3\pi}{8} \tag{2.37}$$

It should be noted that the impedances shown in Figure **2.13** are at the current generator plane (shown in Figure 2.5) and are independent of transistor/ device technology. The influence of the device output package parasitics and the intrinsic drain capacitances (which are shown in Figure 2.5) need to be accounted for to obtain a representation of the impedances presented to the internal current generator[2.22]. Very few vendor models allow such access with only one major vendor Wolfspeed, an exception (since 2014).

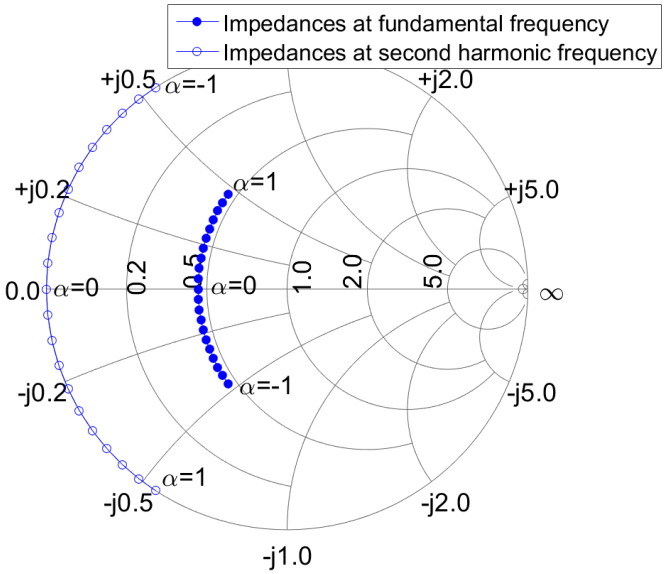

Figure 2.13: Fundamental and second harmonic impedance of class B/J continuum amplifier at current generator plane

The general expressions for class B/J impedances as a function of conduction angle are derived in [2.23]. Since class J is biased as in class B or deep class AB [2.20], these expressions have little application in the practical design of the class B/J amplifier than those derived in (2.35)

and (2.36) which are based on the class B bias condition. Extending the Class B/J continuum to higher harmonics is more useful, which is discussed in the following section.

2.7.1. Extended class J modes

The formulation in equation (2.38) assumes that the third and higher harmonics are terminated with a short. A generic voltage formulation for the class B continuum was presented in [2.21].

$$V_{ds}(\theta) = V_{dc}(1 - \cos(\theta))(1 - \alpha_n \sin(n\theta)); n \geq 1 \; and \; \alpha_n \in [-1,1] \tag{2.38}$$

Where, α_n is a design parameter which controls the magnitude of the quadrature component of the fundamental and second harmonic components, simultaneously. All of these voltage waveforms have the same efficiency and output power. Maintaining the drain voltage for n requires a matching network to the $(n+1)^{th}$ harmonic.

In particular, n=2 provides another practically feasible solution as it requires matching up to the 3rd harmonic only. However, it was observed in [2.24] that this implementation requires a significant reactive component at the 2nd and 3rd harmonics, which is difficult to realize due to low impedance presented by the drain-source capacitance (C_{ds}) at a higher frequency. As a solution, the current was allowed to collapse (clip) by allowing the drain voltage to go below the knee voltage of the transistor to generate the required harmonics. The harmonics generated due to current collapse extend the design space of class J. The voltage under these conditions can be written as

$$V_{ds}(\theta) = V_{dc} - V_{dc}\cos(\theta) + \frac{\gamma}{2}V_{dc}sin(2\theta) - \frac{\gamma}{3}V_{dc}\sin(3\theta); \;\; \gamma \in [-1.1,1.1] \tag{2.39}$$

Since this design method depends on current collapse, this leads to a deterioration in the linearity of the amplifier [2.19].

The class B/J/J* continuum has been extended in [2.25] by adding an arbitrary harmonic element to the voltage formulation in equation (2.32) as

$$V_{ds}(\theta) = V_{dc}(1 - \cos(\theta))(1 - \alpha\sin(n\theta))(1 + \gamma\cos(m\theta)); \\ -1 \leq \alpha, \gamma \leq 1; n, m \in N + \tag{2.40}$$

The added empirical parameter (γ) contributes to in-phase and quadrature-phase components at higher harmonics causing a decrement in the efficiency. Even though the added arbitrary harmonic element leads to a much larger design space but only a few modes can be used to

design the amplifier because of the increase in difficulty in designing a matching network to avail of the improvement which requires 3rd and higher terminations.

2.7.2. Effect of lossy second harmonic termination on the efficiency of class J

In the theory of class J, the load to the second harmonic termination is assumed to be purely reactive. However, in practice, presenting a purely reactive termination at the second harmonic is difficult to achieve not only over a large bandwidth but also at a narrow bandwidth, due to losses in the matching network. The discrepancy with theory leads to deterioration of efficiency and output power. For the practical case, the drain voltage in class J can be expressed as[2.26]

$$V(\theta) = V_k + (V_{DC} - V_k)\{1 - \cos(\theta + \delta)\}\{1 + \alpha \sin(\theta + \gamma)\} \tag{2.41}$$

where, $0 \leq \delta, \gamma < 2\pi$ and $-1 \leq \alpha \leq 1$

Choosing $\delta = \tan^{-1}(\alpha)$ and $\gamma = 0$ will result in the class J voltage waveforms given in (2.32). Sweeping γ corresponds to a varying resistive component at the second harmonic impedance. This equation represents all possible waveforms that are achievable by the real lossy broadband matching network, albeit in analytical fashion [2.26].

This analytical expression is used for a rigorous investigation into the effect of straying off of the second harmonic load impedance from ideal for a given fundamental load given in (2.35) using the concept of second harmonic "clipping contours" [2.26] [2.27]. The second harmonic clipping contour represents the second harmonic load impedances at which the voltage waveform grazes the knee voltage for a given fundamental load ie., $V(\theta) \geq V_k$ in (2.41). The second harmonic clipping contour divides a Smith chart into two regions: a clipping region and a linear region. Impedances in the clipping region cause the drain voltage to go below the knee voltage of the transistor whereas impedances in the linear region maintain the drain voltage above the knee voltage but with a reduction in efficiency. The linear operation of class J was achieved over a broad bandwidth by avoiding the clipping region while taking into account the practical difficulty in achieving reactive termination at the second harmonic load in [2.27]. However, this analysis is computationally intensive as they require at least 10^{15} calculations per contour that can be reduced to 10^4 if numerical root-finding methods are used [2.27].

Conventionally, clipping contours are used to only distinguish the load conditions for which voltage grazes or remain above the knee region ie., $(V(\theta) \geq V_k)$ and those that do not. The effect of the clipping of drain current as the drain voltage goes below V_k on the output power and the efficiency of a class J were studied in [2.28][2.29]. The study [2.28] reveals that the

continuum of impedances exists even when the current clips and its dependence upon the knee profile is obtained via simulations.

2.7.3. Effect of non-linear elements on the performance of class J

In theory, the maximum efficiency and the output power of class B/J continuum are the same as in class B for all values of α. However, real devices show an increase in efficiency and output power above class B, for a range of α values, and deterioration in performance for other values of α. The range of values of α for which the performance of a PA improves over class B is dependent on the device; inductive loading at the fundamental frequency (ie., for $\alpha > 0$) [2.30][2.31][2.32] whereas capacitive loading at the fundamental frequency (ie., for $\alpha < 0$) [2.33] can be observed to enhance the PAE and output power. The harmonics generated from C_{ds} have been reported as the reason for the increase of peak PAE and peak output power in [2.30][2.31][2.33] and we have shown that non-linear C_{gs} plays a role in the improvement of PAE and output power at back-off power levels [2.32].

The harmonics generated from the non-linear C_{ds} were incorporated in the design process in [2.34] to reduce the phase difference to increase the efficiency. It is illustrated for a GaN HEMT that the harmonics from the output capacitance (a combination of C_{ds} and C_{gd}) are significant at high output power levels only because the C_{ds} is strongly nonlinear only in the knee region [2.34]. The harmonics generated from C_{ds} at high power levels have been utilized to achieve class J operation using purely resistive and reactive loads at the fundamental and second harmonic frequencies respectively. A resistive load at fundamental frequency reduces the phase mismatch between the voltage and current in a class J amplifier, leading to improvement in the efficiency. This load condition referred to as saturated PA, has been claimed as a further optimized version of class J. Since harmonics generated from C_{ds} are used, the tolerance of harmonic load increases, thereby adding additional flexibility to the matching network design. It can be observed from Table 2.2 that this amplifier has the highest reported efficiency so far in narrowband class J amplifiers. However, the analysis of the effect of the nonlinearity over the bandwidth and the broadband capability of class J mode is absent.

The non-linear C_{gs} results in an additional second and higher harmonic components at the gate node apart from the applied input signal [2.18]. A study of the influence of a second-harmonic voltage component at the gate node of the device on the optimum load impedance, output power, and drain efficiency [2.35][2.36] reveals that the drain efficiency and the output power can be improved by proper second harmonic terminations. Additionally, source impedances at

Table 2.2: Efficiency of the class J amplifier reported in literature

Reference / Year	Mode	Device type	PAE (%)	Center Frequency (in GHz) / Bandwidth (in MHz)	Output power at saturation (in dBm)
[2.34] / 2010	classJ	GaN HEMT	77.3	2.14 (-)	40.6
[2.83] / 2010	classJ	Si-LDMOS	77	1 (230)	41.14
[2.23] / 2011	Class J	GaN HEMT	64.5	2.13 (140)	39.75
[2.84] / 2013	class J	LDMOS	62.8	0.505 (-)	57
[2.85] / 2015	class J	GaAs HBT	57.5 -62	0.824 (90)	34
[2.13] / 2015	Class J (cascade)	GaAs HBT (InGaP Emitter)	62	0.814 (100)	34
[2.86] / 2016	class-J	InGaP/GaAs HBT	40.5-55.8	1.71 (340)	28*
[2.87] / 2014	class J	GaAs HBT	51.6	2.4 (-)	29.5

*P1dB

the second harmonic frequency could result in the second harmonic voltage to be out-of-phase with the fundamental voltage, leading to a reduction of the conduction angle of the drain current and a loss of efficiency [2.34][2.36]. However, the second harmonic source impedances that deteriorate the efficiency are observed to be confined to a small region on the Smith chart [2.34][2.36]. The design methodology adopted in [2.34] is simply to avoid the second harmonic impedance of the matching network to fall within this region. Rather than relying on the harmonics generated by C_{gs} to shape the gate voltage for high efficiency, a two-stage cascaded PA is proposed wherein the harmonics generated from the PA in the first stage are utilized to shape the voltage at the gate of the second PA [2.37]. In the case of [2.37], both the devices in the two-stage cascaded mode operate in class J.

In addition to non-linear capacitances, harmonics are also generated from the non-linear drain-source resistance (R_{ds}) [2.38]. This study of the effect of non-linear drain resistance on the load impedance, output power, efficiency and bandwidth of class J in [2.38] has revealed that non-linear R_{ds} limits the maximum bandwidth over which higher efficiency and output power can be obtained.

2.7.4. Active second harmonic tuning

In this approach of designing a class J PA[2.39], not only the second harmonic generated by the device of the class J amplifier (primary amplifier) is utilised but also a second harmonic is injected into the load by another amplifier (secondary amplifier), typically operating in class C. The harmonic injection has been shown to improve the efficiency and output power of the amplifier [2.40]. For the case of an amplifier designed in [2.40], the theoretical improvement in efficiency and output power are estimated as 5% and 1.5 dB respectively, whereas the realized amplifier shows an improvement of 2.4% and 0.8 dB in PAE and output power respectively. Additionally, if only the harmonics generated by the device are considered, the bandwidth of the class J amplifier cannot exceed octave frequencies because the second harmonic impedances, which are reactive, at the lower end of the bandwidth becomes the fundamental load at the higher end. The second harmonic injected by the secondary amplifier varies the second harmonic impedance. Because of the active tuning of the second harmonic load, this amplifier architecture [2.39] can achieve bandwidth above octave frequencies. However, this configuration underutilizes the secondary amplifier as it is used only for the amplification of second harmonic frequency.

2.8. Benefits of class J mode

A wider range of impedances facilitates broadband design, as the movement of the impedance of the output matching network with frequency can be easily incorporated into the design [2.20] [2.19]. It has been shown that an output matching network with just two elements (a microstrip line and a radial stub) can result in efficiency above 55% over a broad bandwidth (1 GHz – 3 GHz) [2.41]. Additionally, the requirement of a reactive load rather than a short allows reducing the Q of the matching network and the complexity of the matching network [2.42][2.43]. This is convenient from the perspective of a matching network design as the second harmonic termination can be realised by the drain capacitance itself [2.23]. Also, the bandwidth of the classical classes of operation is limited by the device and package parasitics. The drain capacitance and parasitic elements of the package can be absorbed into the output matching network in a fruitful manner to ease the class J amplifier design [2.44][2.45] [2.22][2.46] thereby simplifying the design of matching network for the broadband amplifier. Such an approach has allowed to achieve efficiency over 60% across the frequencies ranging from 1.4GHz to 2.6GHz class J PA with simple single stub matching network [2.19]. Alternatively, load-pull simulations can be performed at the intrinsic device by de-embedding

the parasitic element to obtain efficiency contours over the normalized fundamental and 2nd harmonic reactive plane [2.47].

A generalized method was proposed in [2.45] to match impedances at fundamental and second harmonics over broadband. A large pool of matching networks of the same topology was analytically synthesized and evaluated. A matching network which fits the requirement was selected. This procedure was demonstrated for double stub and stepped impedance matching network. However, it requires the prior selection of matching network topology and the analytical expression for the fundamental and second harmonic impedances for the selected topology.

It was noted in [2.48] that selecting a higher resistance value, in equation (2.35), reduces the power dissipation in parasitic elements and the dimensions of the transistor were optimized to meet the requirement. The higher quiescent drain voltage achieved in the process moved the optimal impedances close to the centre of the Smith chart providing an opportunity to minimize the losses in the matching network through the realization of low Q matching network. Such an integrated approach allowed to optimize the transistor and matching network simultaneously to realize a high-efficiency class J amplifier.

Class J has demonstrated its capability of high efficiency over a broad bandwidth, as can be observed in Table 2.3 It has demonstrated bandwidth exceeding octave frequencies; in one implementation [2.39] with efficiency above 69% using second harmonic injection, though, in another implementation [2.49] which uses passive load network, the efficiency is heavily compromised to 12 %. Efficiencies above 63% and 50% over the frequency range spanning X-band were reported in [2.50] and [2.24] respectively. Class J operation has also been demonstrated at 25-27 GHz [2.51]. It was shown in [2.52][2.53][2.54] that the efficiency of class J can be maintained even at the back-off power level of 10 dB by varying the reactance of load in accordance to the input power, which can be accomplished by a varactor diode. This leads to a much less complex circuitry eliminating the requirement for extra active components as in the case of envelope tracking and Doherty configuration [2.16].

A typical class J amplifier employs second harmonic to extend its bandwidth. Recent high-efficiency implementations [2.55]–[2.57] have employed class F/F^{-1}, in which frequencies up to third harmonic are considered in the design, in conjunction with second harmonic manipulation to achieve high efficiency.

Table 2.3: Bandwidth and efficiency of the reported broadband class J amplifier in literature

Reference / year	Mode	Device type	Frequency Range (in GHz)/ Bandwidth (in %)	PAE (%)	Psat(in dBm)
[2.19] / 2009	classJ	GaN HEMT	1.4 - 2.6 / 60	60-70*	40
[2.20] / 2009	classJ	GaN HEMT	1.35-2.25 /50	60-70*	40
[2.39] / 2011	dual band (classes J &B)	GaN HEMT	0.6 - 2.4 /120	69-75*	40.3
[2.50] / 2011	Class J	10x75µm GaAs pHEMT	7.0 –12 /52	63-65*	26-28
[2.47] / 2011	class J	GaN HEMT	2.30-2.70 /16	58-65	40-40.79
[2.88] / 2012	Class J	BiCMOS with TWV@	0.5 - 0.9 /57	62-68.9*	30-30.9
[2.45] / 2012	class J hybrid	GaN HEMT	1.60-2.20 /31	55-68*	40-41
[2.45] / 2012	class J hybrid	GaN HEMT	0.5 - 1.8 /113	50-69*	39-40.8
[2.44] / 2012	Class J	GaN HEMT	0.9 - 2.3 / 87	53-63	47.8-48.4
[2.89] / 2013	class J	GaN HEMT	1.65- 2.7 /48	55-72*	40.5
[2.48] / 2013	Class J	GaN	2.25-3.08 /31	>50*	26.8
[2.24] / 2014	Class J	GaN HEMT++	9.20-10.80 /16	>50%	37.8
[2.49] / 2014	Class J	GaN HFET	1.0 - 4.0 /120	>12	20.3+
[2.90] / 2014	class J	GaN HEMT	1.6 - 2.5 /44	55-70	40
[2.51] / 2014	class J-cascode	120-nm SiGe BiCMOS	27-29 /7.14	33.8-35.3	18-18.9
[2.91] / 2014	class J (Bias independent)	AlGaN/GaN	1.8 - 2.7 /40	>60	32.2 at 10V 44.3 at 40V
[2.38] / 2016	Class J	AlGaAs–InGaAs pHEMT	3.5 - 7.0 / 67	>50	26.2-27.8
[2.25] / 2016	extended class B/J continuum	GaN HEMT	2.85-4.25 /39	54.5%–74%	40.68–41.99

Psat: Output power at saturation *Drain Efficiency ++Bare Die @ Through wafer vias +P1dB

2.9. The second harmonic manipulated Class F/F^{-1}

In the ideal class F amplifier, the voltage is tuned to a square waveform, as shown in Figure 2.14, obtained by presenting a short for even harmonics and open for odd harmonics [2.58].

This configuration has non-overlapping current and voltage waveforms, and zero dissipation at harmonics, leading to 100% efficiency. However, from the practical perspective, achieving precise terminations at an infinite harmonic is difficult if not impractical. Hence, up to the third harmonic is typically considered in the design process. However, an amplifier design process using up to the 4th harmonic has been demonstrated in [2.59]. Raab [2.15] has shown that efficiency can be maintained above 90% by considering up to the third harmonic frequency. The voltage of class F truncated up to 3rd harmonic frequency can be written as

$$V_F(\theta) = 1 - \frac{2}{\sqrt{3}}\cos(\theta) + \frac{1}{3\sqrt{3}}\cos(3\theta) \tag{2.42}$$

The third harmonic of the voltage flattens the voltage to generate symmetric near square waveform in Class F as can be seen from the truncated current and voltage waveforms of class F amplifier shown in Figure 2.14 (a). As in the case of second harmonic manipulation illustrated in section 2.6, this enables an increase in fundamental component and a reduction in the overlap between the voltage and current leading to an increase in the efficiency.

On the other hand, in the class F^{-1} amplifier, the current and voltage waveforms are shaped to a square wave and a half-sinusoid respectively by presenting a short to odd harmonics and an open to even harmonics. The ideal and truncated current and voltage waveforms of a class F inverse amplifier are shown in Figure 2.14 (b).

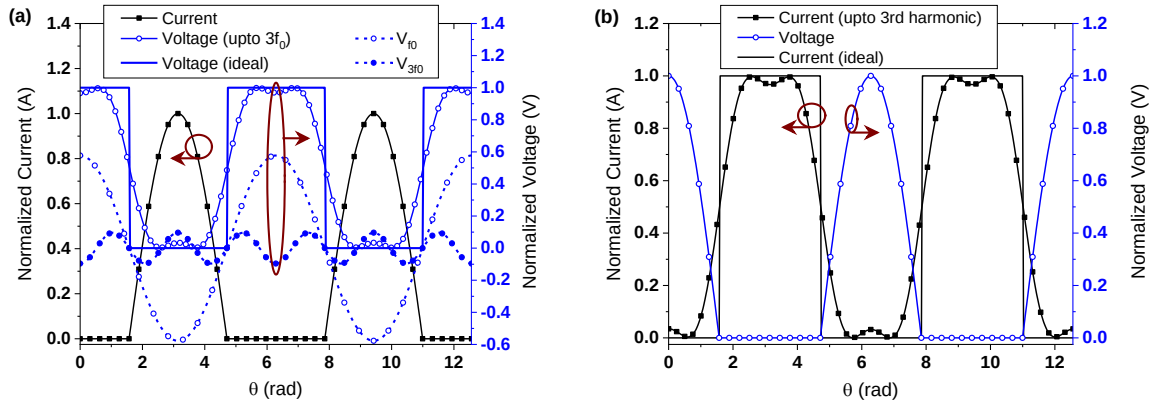

Figure 2.14: The ideal and truncated (up to 3rd harmonic) current and voltage waveforms of (a) class F and (b) inverse class F amplifiers.

However, the requirement of the precise harmonic terminations such as short at second harmonic and open at third harmonic require high resonant and high-quality factor structures [2.59][2.60]. Even though these structures enable the realization of the higher efficiency amplifiers, this comes at a cost of limited bandwidth. This limitation makes these classes of

operation less appealing for broadband applications. Similar to class B/J continuum, the proposed continuum of voltage [2.55] and current [2.56][2.57] waveforms to class F and class F^{-1}, respectively, allow reactive terminations at the second harmonic frequency, resulting in an increase in the bandwidth of the amplifier with the same advantages during the amplifier design process as discussed in section 2.8. These continuum of waveforms to class F and class F^{-1} are referred to as continuous class F (CCF) and continuous class F^{-1} (CCF^{-1}). The reactive termination phases the second harmonic component of voltage waveform in the continuous Class F, similar to class J, whereas it phases the second harmonic component of the current waveform in the continuum modes of class F^{-1}.

2.9.1. Continuous class F mode

The current is half sinusoidal as in class J mode and voltage in the continuous class F is given by [2.61][2.62]

$$V_{ds}(\theta) = 1 - \frac{2}{\sqrt{3}}\cos(\theta) - \gamma\sin(\theta) + \frac{7\gamma}{6\sqrt{3}}\sin(2\theta) + \frac{1}{3\sqrt{3}}\cos(3\theta) - \frac{\gamma}{6\sqrt{3}}\sin(4\theta)$$
$$= \left(1 - \frac{2}{\sqrt{3}}\cos(\theta)\right)^2\left(1 + \frac{1}{\sqrt{3}}\cos(\theta)\right)(1 - \gamma\sin(\theta)) \quad (2.43)$$

Where, $|\gamma| < 1$

The formulation in equation 2.43 has an additional reactive component in the second harmonic frequency over the traditional class F given in equation 2.42. This reactive second harmonic component flowing through the device is compensated by a suitably phased fundamental frequency component. Various values of the design parameter γ lead to different waveforms each of which can be obtained by a set of load impedances given by

$$Z_{L1} = R_{opt}\sqrt{\left(\frac{4}{3} + \gamma^2\right)}\angle\tan^{-1}\left(\frac{\sqrt{3}\gamma}{2}\right)$$
$$Z_{L2} = -j\frac{7\sqrt{3}\pi}{24}\gamma R_{opt} \quad (2.44)$$
$$Z_{L3} = \infty$$

These impedances are plotted in Figure 2.15. All of these impedances have the same efficiency of class F over a large set of impedances. Therefore, this significantly wide design space eliminates the requirement of short to obtain the optimum efficiency; this not only reduces complexity but also results in a simplified methodology to design broadband continuous class F [2.61].

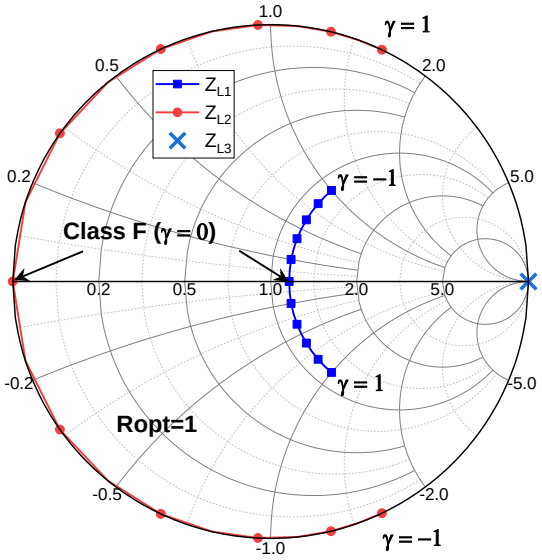

Figure 2.15: The theoretical impedances of continuous class F for R_{opt}=1

2.9.2. Second harmonic manipulation of the current: Continuous class F^{-1}

Continuous class F^{-1} is obtained by shaping the current waveform of class F^{-1} whilst maintaining the constant voltage waveform [2.57][2.56] by placing a reactive load impedance (Z_{L2}) at the second harmonic.

$$Z_{L2} = \frac{1}{G_{L2}} = jy_2 \tag{2.45}$$

In [2.57], the quadrature component of the second harmonic was added to the class F^{-1} current waveform by multiplying an extra operator

$$i(\theta) = \underbrace{(i_{dc} - i_1\cos(\theta) + i_2\cos(2\theta) + i_3\cos(3\theta))}_{Class\ F^{-1}}\underbrace{(1 - \zeta\sin(\theta))}_{Additional\ term} \tag{2.46}$$

Where, $i_{dc} = 0.37$, $i_1 = 0.43$, $i_2 = 0$, $i_3 = 0.06$, $-1 < \zeta < 1$

Alternatively, the second harmonic component of current in the case of the class B mode, given in equation 2.21, can be eliminated to obtain the current waveform in continuous class F inverse [2.56] as

$$= I_{DC} + \sum_{n=1}^{3} a_{in}\cos(\theta) + b_{in}\sin(\theta) \tag{2.47}$$

Where,

$$I_{DC} = \frac{I_{max}}{\pi} \tag{2.48}$$

$$a_{i1} = I_m\left(\frac{1}{2} - \frac{8}{9\pi^2}\right) \quad ; \quad b_{i1} = \frac{4(V_{dc} - V_{knee})}{3\pi * y_2} \tag{2.49}$$

$$a_{i2} = 0 \quad ; \quad b_{i2} = \frac{(V_{DC} - V_{knee})}{2 * y_2} \tag{2.50}$$

$$a_{i3} = \frac{-8I_{max}}{5\pi^2} \quad ; \quad b_{i3} = \frac{4(V_{DC} - V_{knee})}{5\pi * y_2} \tag{2.51}$$

The voltage waveform of class F^{-1}, given in the equation below (in (2.52)), is the second harmonic manipulated voltage in equation (2.28) at $k_2 = -0.35$. This value of k_2 corresponds to the maximum voltage gain ($\delta(k_2)$), as shown in Figure 2.17 (a).

$$V_d(\theta) = V_{dc} - \sqrt{2}(V_{dc} - V_k)\cos(\theta) - \frac{V_{dc} - V_k}{2}\cos(2\theta) \tag{2.52}$$

It can be seen that only the quadrature components of the current (b_{i1}, b_{i2}, b_{i3} ...) vary with the reactive impedance at the second harmonic (y_2) and the fundamental impedance needs to be adjusted according to y_2 as

$$Z_{L1} = \frac{\sqrt{2}(V_{dc} - V_k)}{I_m\left(\frac{1}{2} - \frac{8}{9\pi^2}\right) + j\frac{4}{3\pi}\frac{(V_{dc} - V_k)}{y_2}} \tag{2.53}$$

The ideal voltage and current waveforms of continuous class F^{-1} and the corresponding required impedances at fundamental and second harmonic frequencies are plotted in Figure **2.16** (a) and (b) respectively. The current is seen to be peaking to the right or to the left depending upon whether the second harmonic impedance is inductive ($y_2 > 0$ ie., $b_{i2} > 0$) or capacitive ($y_2 < 0$ ie., $b_{i2} < 0$). All these waveforms achieve the same efficiency as class F^{-1}. Importantly, this mode does not require an open at the second harmonic frequency and the designer can choose from a range of impedances illustrating the flexibility in the design process. The range of impedances (y_2) of CCF^{-1} is limited to waveforms such that $b_{i2} \leq \pm 0.3a_{i1}$ [2.56] because any further increase in the impedance results in the peak of the drain current to exceed the maximum device current (I_m), as can be seen from the Figure **2.16** (a) which shows the limiting case $b_{i2} = \pm 0.3a_{i1}$.

The set of impedances in class CCF^{-1} design space can be traced with frequency in a clockwise direction at fundamental and second harmonic frequencies whereas class J or CCF will require counter-clockwise rotation on the Smith chart. Since the passive networks have clockwise impedance traces with frequency as formulated by the Foster reactance theorem [2.11], CCF^{-1} is easier to realise than class J.

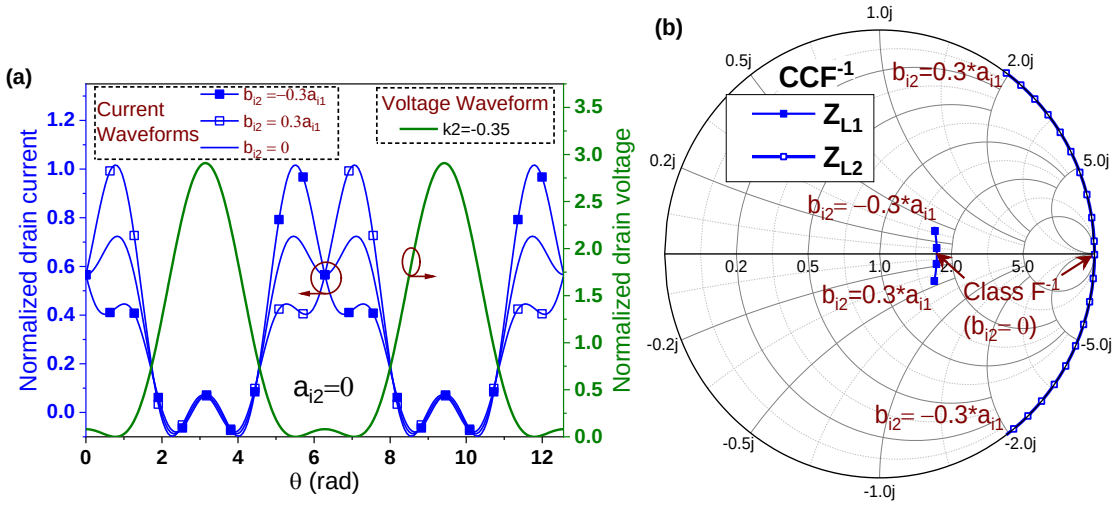

Figure 2.16: (a) The theoretical current and voltage waveforms of continuous class F^{-1} (CCF^{-1}) (b) The theoretical impedances of CCF^{-1}

2.10. Extended Continuum Modes

Even though the continuum modes (class B/J continuum, CCF, and CCF^{-1}) have a range of impedances to choose from, their fundamental impedances lie on a constant resistance in the case of class B/J continuum and CCF whereas the fundamental impedances of CCF^{-1} lie on a constant conductance circle, as seen from Figures **2.13**, **2.15**, and **2.16**. However, designing a matching network to match a constant resistance or conductance is difficult if not impractical over a broad range of frequencies [2.55].

2.10.1. Extended CCF^{-1}

A series of continuous class F^{-1} modes [2.63][2.64] were obtained by using the generic voltage waveform, given in equation (2.28), by varying k_2 between -0.18 and -0.35. The values of k_2 less than -0.35 are avoided, even though $\delta(k_2) \geq 1$ as can be seen in Figure 2.17 (a), because the overshooting of the voltage for these values leads to reliability issues. These extended series of CCF^{-1} have efficiencies less than class F^{-1} because of the decrease in the fundamental component of voltage. However, it still maintains a higher efficiency than class B. The family of the voltage and the current waveforms in extended continuous class F^{-1} are plotted in Figure 2.17 (b). An alternative form of a voltage formulation for the extended continuum is proposed in [2.64] as

$$V_{ds}(\theta) = 1 + \alpha\cos(\theta) + \beta\cos(2\theta)$$

Where, $\alpha - \beta = 1$ for $1 \leq \alpha \leq \frac{4}{3}$

$$\frac{\alpha^2}{8\beta} + \beta = 1 \text{ for } \sqrt{2} \geq \alpha > \frac{4}{3} \qquad (2.54)$$

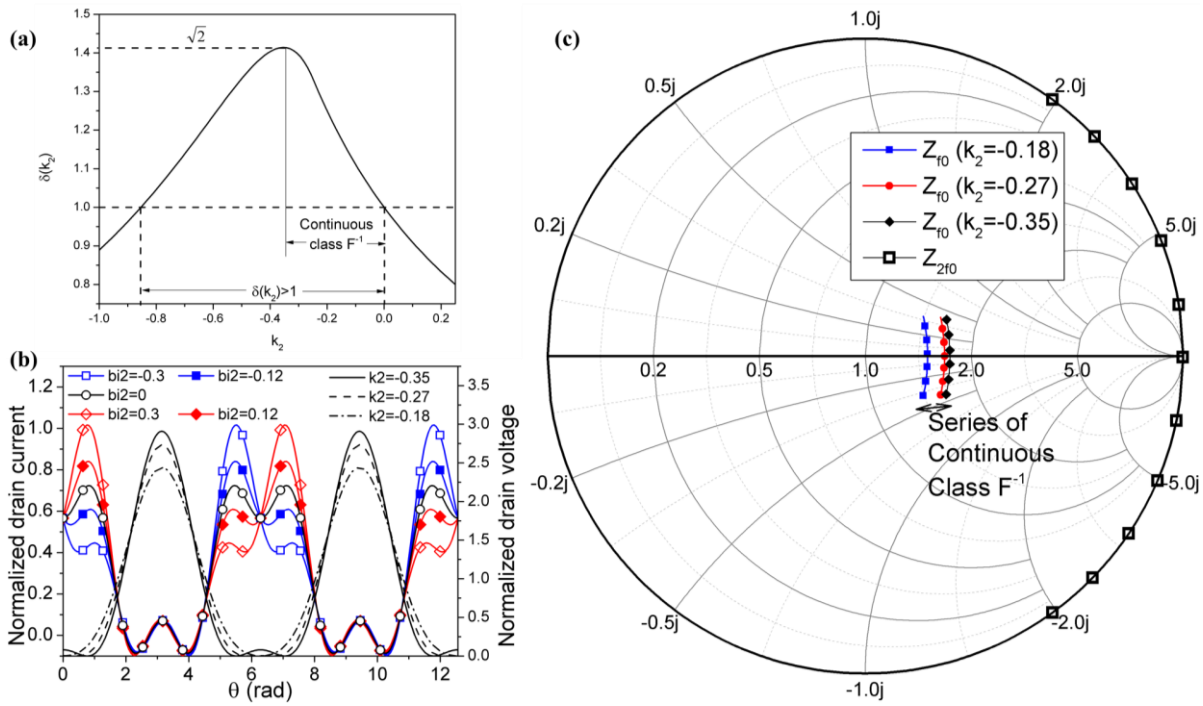

Figure 2.17: (a) Magnitude of the fundamental component of voltage with k_2 (b) The family of voltage and current waveforms of continuous class F^{-1} series (c)The fundamental (Z_{f0}) and second harmonic impedances (Z_{2f0}) of continuous class F^{-1}

From the voltage, given in equation (2.28), and current waveforms, given equations (2.48)-(2.51), the conductance at a fundamental frequency can be calculated as

$$G_{L1} = \frac{I_m\left(\frac{1}{2} - \frac{8}{9\pi^2}\right) + j\frac{4}{3\pi}\frac{(V_{dc} - V_k)}{y_2}}{\delta(k_2)(V_{dc} - V_k)} \tag{2.55}$$

The impedances required at the fundamental and second harmonic frequencies are plotted in Figure 2.17 (c). From the ratio of the reactive components of second and fundamental admittances, given in equation 2.56, it can be observed that class F^{-1}/J mode requires a much higher reactive component in conductance. In other words, a less reactive component in impedance at a fundamental frequency is required by this mode than in class J.

$$\frac{\Im m\{G_{L1}\}}{\Im m\{G_{L2}\}} = \frac{3\pi}{2\sqrt{2}} \tag{2.56}$$

A smaller ratio leads to a much smaller range of fundamental impedances than the class J continuum, as can be observed in Figure 2.17 (c).

The output power and efficiency for extended continuous class F^{-1} are [2.63]

$$P_{out} = \frac{\delta(k_2)(V_{dc} - V_{knee})}{2} I_{max}\left(\frac{1}{2} - \frac{8}{9\pi^2}\right) \tag{2.57}$$

$$\eta = \frac{P_{out}}{P_{dc}} = \frac{\pi\delta(k_2)}{2}\left(1 - \frac{V_{knee}}{V_{dc}}\right)\left(\frac{1}{2} - \frac{8}{9\pi^2}\right) \tag{2.58}$$

The efficiency of continuous class F^{-1} is 91% when V_k=0. Even though extended continuous class F^{-1} achieves efficiencies less than this, it can achieve high-efficiency operation over a broad range of frequencies as observed from Table 2.4.

Table 2.4: Performance of continuous class F and class F^{-1} reported in literature

Reference / year	Mode	Device type	Frequency Range (in GHz) / Bandwidth (in %)	DE (%)	Psat (in dBm)
[2.56] / 2011	Continuous class F^{-1}	GaN HEMT	3.5/ -	65	47
[2.92]/ 2011	Continuous F	GaN HEMT	0.55 - 1.10 / 66.7	65-80	39.3-41.2
[2.61] / 2012	Continuous F	GaN HEMT	1.45 - 2.45 / 51.3	70-81	40.41-42.25
[2.80] / 2012	Continuous F/F^{-1}	GaN HEMT	1.30 - 3.30 / 86.9	60-83	40-41.76
[2.75]/ 2013	Continuous F	GaN HEMT	0.53 - 1.33 / 86.0	70-80	39-41.4
[2.64] / 2016	extended Continuous F^{-1}	GaN HEMT	2.40 - 3.90 / 47.6	62-75	39.63-41.4
[2.63] / 2016	extended Continuous F^{-1}	GaN HEMT	0.50 - 0.90/ 57.1	75-84	40-41.05

Psat= Output power at saturation

2.10.2. Hybrid modes

The continua of waveforms that exist between the two continuum modes are referred to as hybrid modes. These waveforms result in a design space which has a varying real part of the impedances at the fundamental frequency. An example of such a mode is class BJF which uses the design space that lies between the class B/J continuum and continuous class F [2.65]. For this mode, the drain current is the same as class B, given in (2.21) while the drain voltage is formulated as

$$V_{DS} = (1 - \alpha\cos(\theta) + \beta\cos(3\theta)) * (1 - \gamma\sin(\theta))$$
$$\text{Where, } \alpha - \beta = 1 \text{ for } 1 \leq \alpha \leq \frac{9}{8} \tag{2.59}$$
$$\alpha\left[\left(\frac{2}{3} + \frac{2\beta}{\alpha}\right)\sqrt{\frac{1}{4} + \frac{\alpha}{12\beta}}\right] = 1 \text{ for } \alpha > \frac{9}{8}$$

The voltage waveform of class B/J continuum and CCF are obtained for $\alpha = 1, \beta = 0$ and $\alpha = \frac{2}{\sqrt{3}}, \beta = \frac{1}{3\sqrt{3}}$ respectively. The values of α lie between 1 and $\frac{2}{\sqrt{3}}$ and choosing a value of β which satisfies (2.59) results in a voltage waveforms contiguous with class B/J continuum and CCF. The corresponding real part of the fundamental impedance varies from Ropt (optimal load line

resistance of class B) to 1.154*Ropt (optimal load impedance of class F). These waveforms are referred to as a series of continuous modes (SCM)

Series of continuous inverse modes (SCIM) was proposed in [2.66] where the drain voltage is half sinusoidal (whereas the current waveform in SCM is half sinusoidal) and the continuum of current waveforms (and the voltage waveforms in SCM) as

$$I_{DS} = (1 - \alpha\cos(\theta) + \beta\cos(3\theta)) * (1 - \gamma\sin(\theta)); \quad -1 \leq \gamma \leq 1 \tag{2.60}$$

$$V_{DS} = 1 + \frac{2}{\sqrt{2}}\cos(\theta) + \frac{1}{2}\cos(2\theta) \tag{2.61}$$

α and β are free parameters and the constraints on them are same as in (2.59). The design space lies between the CCF-1 and the not much utilised "inverse class B/J continuum". These could achieve high efficiency over fractional bandwidth as high as 120 %, as observed in Table 2.5.

Table 2.5: Performance of SCM and SCIM based amplifiers reported in the literature

Reference / year	Mode	Device type	Frequency Range (in GHz) / Bandwidth (in %)	DE (%)	Psat (in W)
[2.65]/ 2014	SCM	GaN HEMT	1.4-2.7/ 63.4	70.4-78.3	10.7-16.6
[2.68]/ 2015	SCM	GaN HEMT	1.6-2.8/ 54.5	70.3-81.9	10.2-17.8
[2.66]/2016	SCIM	GaN HEMT	3.2-3.7/14	70-83	10.5-16
[2.69]/2018	SCM	GaN HEMT	0.8-3.2/120	57-74	9.3-19.5
[2.70]/2019	SCM	GaN HEMT (MMIC)	4.2-7.0/ 50	44-52	2.6-4.4
[2.70]/2019	SCM	GaN HEMT (MMIC)	4.6-6/ 26.4	45-54	2.95-4.17

Psat= Output power at saturation

2.10.3. Resistive-resistive extension of continuum modes

The continuum modes (Class B/J continuum, CCF, CCF^{-1}, SCM, and SCIM) require a reactive component at the second harmonic frequency, which cannot be satisfied over a broad range of frequencies. This constraint can be overcome by extending the mode by including a resistive component at the second harmonic frequency that theoretically lies on the Γ=1 circle on the Smith chart [2.67] to sacrifice the efficiency.

2.10.3.1. ***Resistive-Resistive Class J***

An analysis into the effect of lossy second harmonic impedance on the performance of class J was presented in [2.71] through a formulation which is validated by experiments on a GaN HEMT device. The formulation of voltage is given by

$$V_J = \underbrace{(1-\cos(\theta))}_{Class\ B}\ \underbrace{(1-\alpha\sin(\theta))}_{reactive\ Class\ J\ term}\ \underbrace{(1+\beta\cos(\theta))}_{resistive\ Class\ J\ term} \tag{2.62}$$

The impedance required to generate this waveform is given by

$$Z_{fund} = \left((1-\beta) - j\alpha\left(1-\frac{\beta}{4}\right)\right)R_{opt} \tag{2.63}$$

$$Z_s = \left(\beta + j\alpha(1-\beta)\right)\frac{3\pi}{8}R_{opt} \tag{2.64}$$

These impedances are plotted in Figure 2.18(a). It can be observed that the resistance at the fundamental frequency needs to be reduced due to the increase in losses at the second harmonic frequency. This is to maintain an appropriate phase between the fundamental and second harmonic frequencies. The output power and efficiency can be calculated from equations (2.62) and (2.21) as

$$P_{rf} = \frac{\pi}{4}(1-\beta)V_{DC}I_{DC} \tag{2.65}$$

$$\eta_D = \frac{\pi(1-\beta)}{2(2-\beta)} \tag{2.66}$$

It can be noted that an efficiency greater than 70% can be maintained as long as $\beta < 0.2$ from the plot of efficiency with β shown in Figure 2.18(b). This efficiency can be achieved even with a resistance as high as ~11Ω at the second harmonic frequency. Even though the resistive extension degrades the efficiency, the resistive extension has enabled the authors to design a multi-octave amplifier operative over a frequency range of 0.4 GHz - 2.7 GHz [2.72].

2.10.3.2. ***Resistive-Resistive CCF***

An extension to the CCF mode to widen the design space and the effect of the lossy second harmonic termination is studied in [2.55]. The formulation of this extended mode is given by

$$V_{CCF} = (1-\alpha\cos(\theta))^2(1+\beta\sin(\theta))(1-\gamma\sin(\theta))$$

$$\text{Where, } 0.75 \le \alpha \le 1.5, \frac{\alpha}{2} \le \beta \le \frac{\alpha}{1.4}, \text{ and } -1 \le \gamma \le 1 \tag{2.67}$$

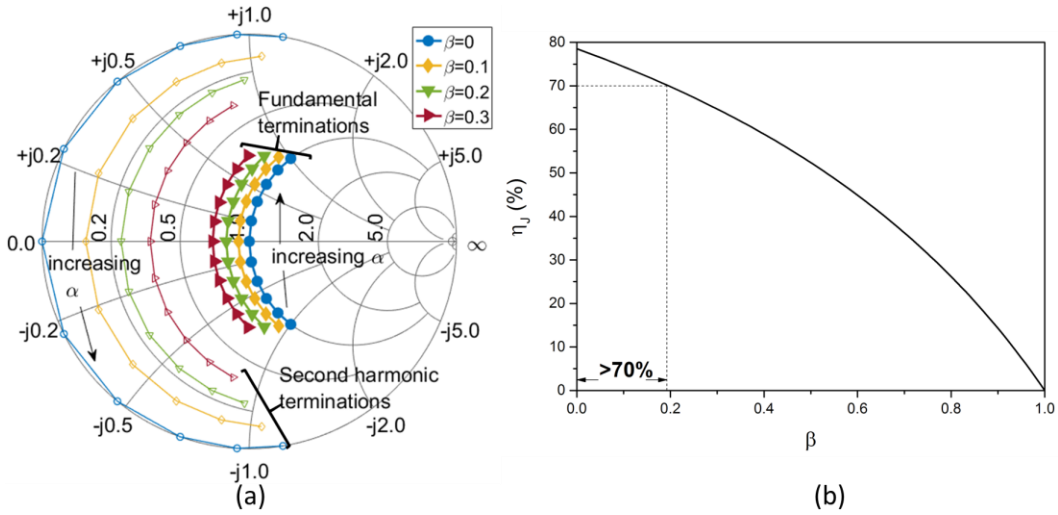

Figure 2.18: (a) The fundamental impedances of class J with resistive loading at second harmonic frequency (b) Deterioration of efficiency due to losses in second harmonic.

Comparing (2.67) with the voltage of CCF given in (2.43), it is seen that α and β are the new free parameters and $\alpha = \frac{2}{\sqrt{3}}$ and $\beta = \frac{1}{\sqrt{3}}$ results in CCF. Increasing α and β increases the real part of the impedances at the fundamental and second harmonic frequencies respectively, resulting in a larger design space for amplifier design. However, as the value of α and β depart from those of CCF, both efficiency and output power decreases. The efficiency remains above 78.5% (ie., above class B) if α and β lie in the range given in (2.67) [2.55]. Alternatively, the resistive second harmonic for CCF can also be formulated similar to the resistive extension of class B/J continuum in (2.62) as [2.73]

$$V_{CCF} = \underbrace{\left(1 - \frac{2}{\sqrt{3}}\cos(\theta)\right)^2 \left(1 + \frac{1}{\sqrt{3}}\cos(\theta)\right)(1 - \gamma\sin(\theta)) * (1 + \delta\cos(\theta))}_{Voltage\ formulation\ of\ CCF} \tag{2.68}$$

Where, $0 \leq \delta \leq 1$, and $-1 \leq \gamma \leq 1$

As δ increases from 0 to 1, the resistive component of the fundamental load impedance decreases and the resistive component of the second harmonic impedance increases, resulting in an increase in the design space. The resulting impedances at the fundamental and second harmonic frequencies and the corresponding efficiency as δ is varied is shown in Figure **2.19**.

However, the efficiency decreases as δ increases and it remains above that of class B (78.5%) for $\delta > 0.36$ [2.73]. The major benefit of this formulation is that the second harmonic and fundamental impedances have the same resistive part for $\delta = 0.54$ which allows the design of multi-octave amplifiers [2.74] [2.75].

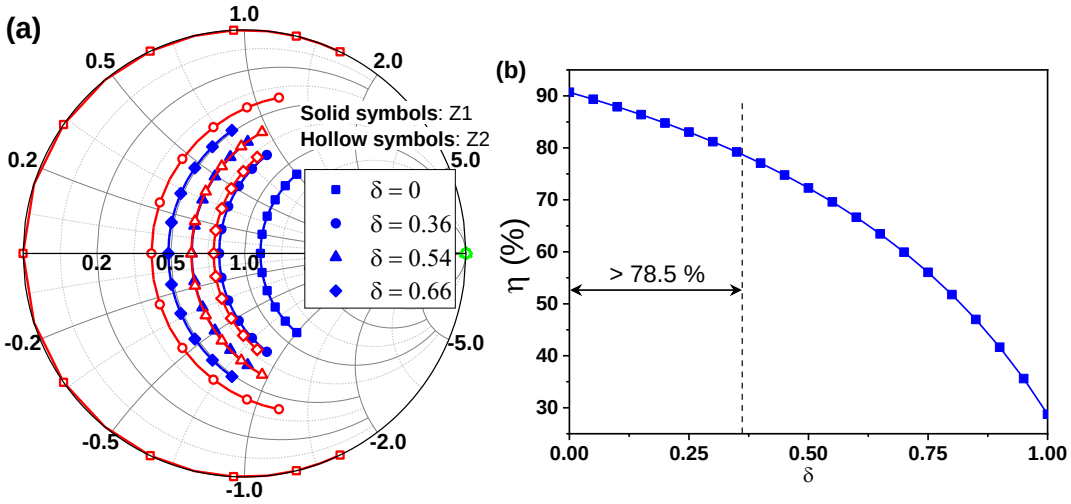

Figure 2.19: (a) The fundamental impedances of CCF with resistive loading at second harmonic frequency (b) Deterioration of efficiency due to losses at second harmonic.

2.10.3.3. *Resistive-resistive SCM and SCIM*

More advanced modes such as the resistive-reactive extension of the Series of Continuous Modes (SCM) [2.65] and Series of Inverse Continuous Modes (SICM) [2.64] represent further evolutions of this approach that is gaining increasing popularity [2.75]–[2.78]. These design spaces are easily defined by phase-shifted waveforms in hybrid continuous modes of voltage shifted waveforms that enable the second harmonic terminations to have both real and imaginary parts [2.79]. The design space corresponding to the modes discussed is plotted in Figure **2.20**.

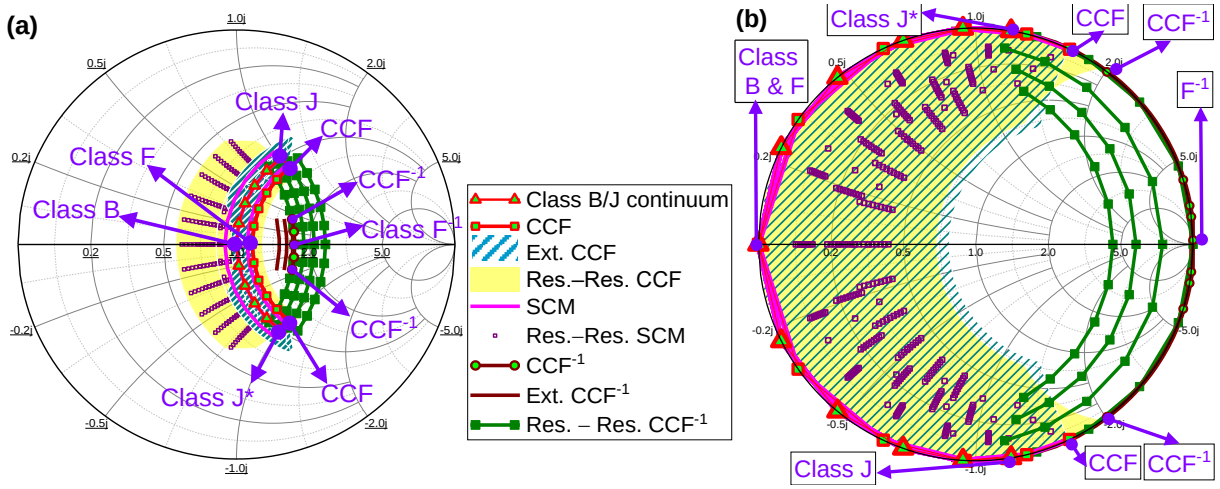

Figure 2.20: Design space of class B/J continuum, CCF, CCF^{-1}, Class BJF (SCM), Resistive-resistive SCM/CCF, and Resistive-resistive SCIM/CCF^{-1} (a) Load impedances at fundamental frequencies (b) Load impedances at second harmonic frequencies.

2.10.4. Mode transferring:

Some amplifier designs exploit mode transfer ie., design the amplifier in one class for a certain range of frequencies and a different class for the remaining range of frequencies. An example of this is an amplifier designed to operate in CCF^{-1} for frequencies between 1.3-2.3 GHz and in CCF for a higher band of frequencies 2.3-3.3 GHz by setting an appropriate drain bias voltage [2.80]. This mode transfer concept between CCF and CCF^{-1} has been used for the design of 23.5-41 GHz power amplifier intended for the use of 5G application [2.81]. At an extreme, an amplifier is designed to transfer the mode to classes F, F^{-1}, J, J* and B at selected frequencies, which corresponds to LTE and 3G bands in the frequency range of 1.9 GHz to 2.7 GHz [2.82].

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Chapter 3: Tools to design an RF power amplifier: Device characterization and EM simulations

3.1. Introduction

A typical amplifier design flow consists of two steps: calculation of optimum source and load impedances and design of the matching network. The optimum impedance can be obtained using a load-pull/source-pull measurement of the device. In the load-pull/source-pull technique, the impedance presented to the device is swept through a range of values and the performance of the device (the output power, efficiency, etc.,) for each of the impedances is obtained. The impedances which meet the design specification are selected and the matching network is designed to match these impedances. Although the load-pull measurements provide accurate optimum impedances[3.1], the application of this approach is limited to fundamental frequency as a large combination of harmonic impedances leads to exorbitant to large sweep times [3.2].

Another approach that is of interest is waveform engineering, in which the impedances are chosen to obtain the voltage and current waveforms required for a particular mode. The waveforms provide additional insight into the operation of the amplifier. Apart from that, the major advantage of this approach over the load-pull technique is that the optimal impedances at fundamental and harmonic frequencies are predicted simultaneously, as we have seen in chapter 2. However, the theoretical formulation of the waveforms does not consider the influence of parasitics and the non-linearities of a transistor (mainly non-linear capacitors and device IV). Therefore analytical expressions were derived by our group [3.3]–[3.6] for class B and class AB which takes into account the influence of parasitics and device IV. However, deriving such expressions for non-linear capacitances is cumbersome, even considering one non-linear capacitance (non-linear input capacitance)[3.7]. Alternatively, non-linear capacitors can be simulated in a non-linear simulator while the influence of device IV can be obtained from measurement [3.8] or from the simulation of the current generator[3.9]. The former has only been demonstrated for fundamental frequency whereas the latter requires extraction of device model consisting of at least 80 parameters from the measurement.

To simplify the design process, waveform engineering is often coupled with load-pull and this design approach consists of the following four steps:

1) Obtain the theoretical impedances corresponding to the voltage and current waveform of the chosen mode from the formulation at the intrinsic plane.

2) Calculate the impedances at the extrinsic plane corresponding to the impedances in step 1. This process is called “embedding”. An approximate parasitic model of the device consisting of the parasitics at the drain terminal is embedded.
3) Perform load-pull simulation/measurement around the impedance values obtained in step 2.
4) Design the matching network for impedances in step 3 and optimize further via EM simulations.

This approach can be considered as an extension of the load-pull technique wherein step 1 minimizes the number of impedances at the fundamental and harmonic frequencies that need to be swept in step 3. Such an approach using expensive load-pull equipment used in conjunction with waveform measurement setup has been demonstrated in the design of broadband and high-efficiency amplifiers [3.2][3.10][3.11][3.12]. This approach has also been demonstrated using a transistor model. However, in this case, the accuracy of the design approach depends on the accuracy of the model.

In this work, we utilize the transistor model from the vendor for the design process. Simulation of the non-linear models of the device in a CAD environment allows multiple design iterations to be performed without having to fabricate an actual amplifier. Additionally, the vendor model of the transistor (CGH40010F) used in this work provides the intrinsic current and voltage waveforms which are necessary to confirm the class of the power amplifier; simplifying the design process. However, calculating the extrinsic impedances corresponding to the required intrinsic waveforms ie.., “embedding” in step 2, requires approximate values of the parasitic elements of the equivalent circuit of the transistor. In this chapter, we present the extraction process by which the approximate values of the parasitics used in this work are obtained. We then explain the embedding process and discuss its accuracy. The extraction presented in this chapter is based on the work done by our group in [3.5], [3.13], [3.14].

Another critical step in amplifier design is performing EM simulations of its layout viz., step 4. The device models can be simulated along with the electromagnetic (EM) simulations of the layout allowing to fine-tune the amplifier performance before fabrication. Because of the ease of integration with transistors, microstrip technology is used for the realization of the layout. Electromagnetic simulations can accurately predict the performance of microstrip lines and hence is indispensable in the design of the amplifier. This chapter also presents the simulation

results of a matching network [3.10], a class AB amplifier designed by our group, and a class J amplifier [3.15] to demonstrate the process.

3.2. Extraction of parasitic elements of a GaN device

A 16-element small-signal equivalent circuit of a GaN device at a bias point is shown in figure 3.1. This approximate model is obtained by replacing the non-linear parasitics (intrinsic capacitances (C_{gs}, C_{gd}, and C_{ds}) and G_{ds} by linear capacitance and G_{ds} with values corresponding to those at the bias point. Additionally, the non-linear current generator is replaced by a voltage controlled current source with a transconductance at the bias point. This approximates the device model in figure 2.4 in chapter 2 and is applicable for low input power levels.

The small-signal equivalent model of a transistor may be extracted from its S-parameters at the bias point by optimizing the component values until the s-parameters of the model matches with s-parameters [3.16]. The optimal values of the component obtained by this approach will

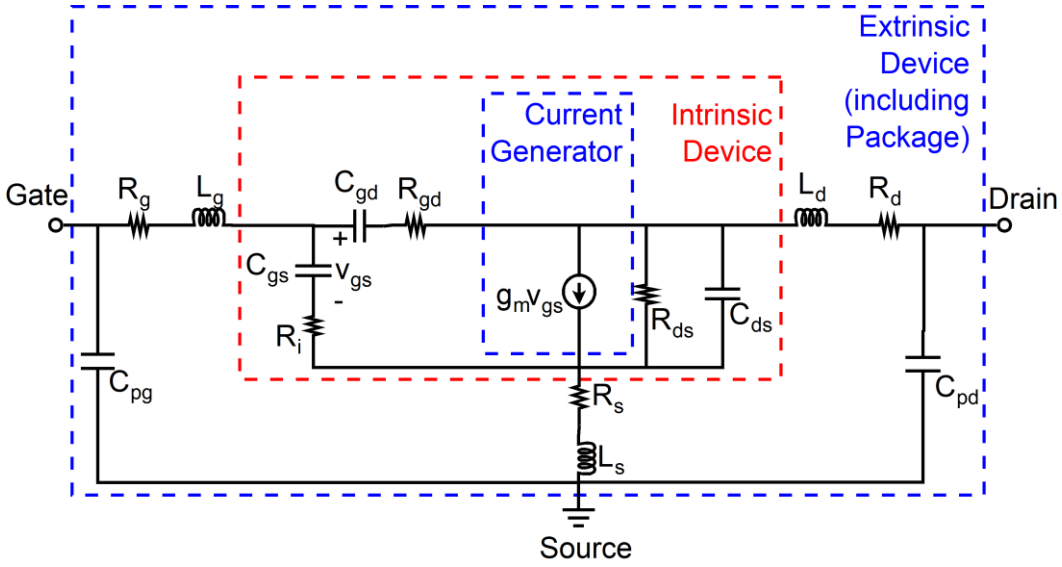


Figure 3.1: The equivalent circuit of the transistor below pinch off.

depend on the optimization method, error function and the starting values [3.17].

On the other hand, we utilize a GaN HEMT extraction process which consists of the Dambrine extraction procedure and minor tweaking of some elements of the model which consists of the following two steps [3.17]:

1) Extraction of the extrinsic parasitic element from the s-parameters of the device at cold condition (V_{ds}=0). The extrinsic pad capacitances are extracted from *cold pinch-off condition* ($V_{gs} < V_{th}$ and $V_{ds} = 0$). At this condition, the equivalent circuit of a device is simplified as the intrinsic device can be represented with a π network of three capacitors (C_{gs}, $C_{gd,}$ and C_{ds}) [3.17][3.18], as shown in figure **3.2**. Whereas the extrinsic resistances and inductors are extracted from *cold forward condition* ($V_{gs}>V_{th}$ and V_{ds}=0).
2) The extraction of the intrinsic parameters from the s-parameters of the device biased at the quiescent point ($V_{ds} = V_{dsq}$ and $V_{gs} = V_{gsq}$).

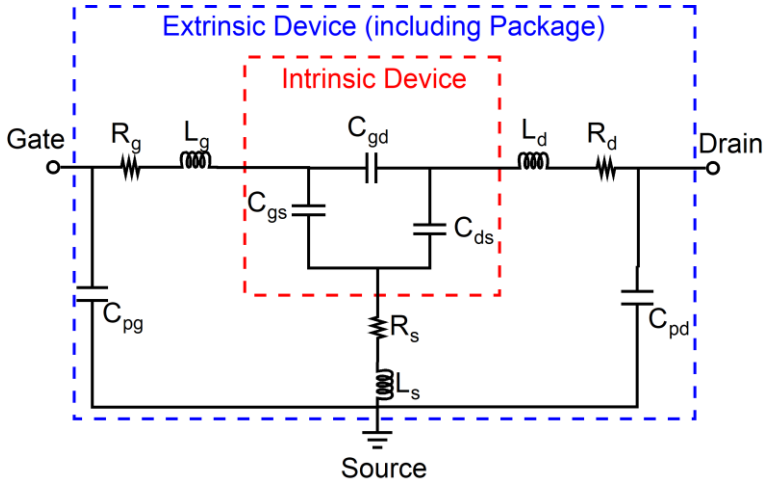


Figure 3.2: The equivalent circuit of the transistor below pinch off.

3.2.1. Extraction of extrinsic pad capacitances (which including package parasitics)

For low frequencies (below 1 GHz), the effect of inductors and resistors can be neglected [3.18][3.19]. The equivalent circuit of the device at cold pinch-off condition is as shown in figure 3.3.

Imaginary parts of the Y parameters of the device are related to capacitances as

$$Im(Y_{11}) = j\omega(C_{pg} + C_{gs} + C_{gd}) = j\omega(C_{gs0} + C_{gd}) \quad (3.1)$$

$$Im(Y_{12}) = -j\omega C_{gd} \quad (3.2)$$

$$Im(Y_{22}) = j\omega(C_{pd} + C_{ds} + C_{gd}) = j\omega(C_{ds0} + C_{gd}) \quad (3.3)$$

Where the total capacitance between the gate-source terminals and drain-source terminals are denoted by C_{gs0} and C_{ds0}, given by:

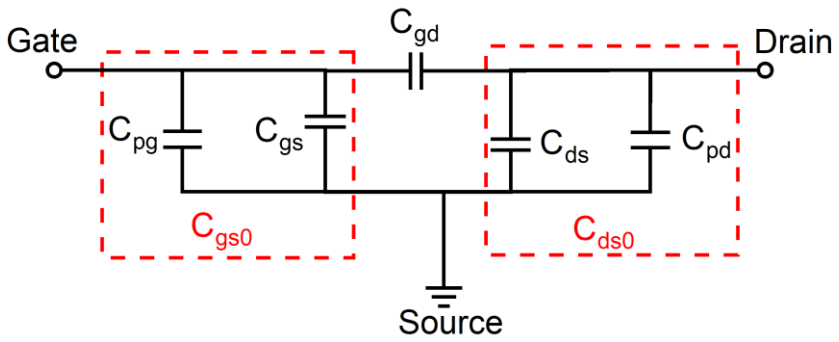


Figure 3.3: Equivalent circuit at cold forward condition

$$C_{gs0} = C_{gs} + C_{pg} \tag{3.4}$$

$$C_{ds0} = C_{ds} + C_{pd} \tag{3.5}$$

The capacitances C_{gd}, C_{gs0} and C_{ds0} can be extracted from the slope of the Y parameters of the device with frequency, ω. The extraction of these capacitances for the vendor model of CGH40010 device is shown in figure **3.4**. However, the 4 unknown capacitances cannot be evaluated using the two relations given in equations (3.4) and (3.5). C_{pd} is assumed to be equal to C_{pg} owing to the symmetrical gate and drain pads in GaN HEMTs [3.18][3.20][3.19] and this assumption is assumed in the extraction of CGH40010 [3.5]. The additional relationships between the capacitances such as the ratio of capacitances can be used [3.20]. However, these ratios between capacitances are related to the structure of the device and are not universal and

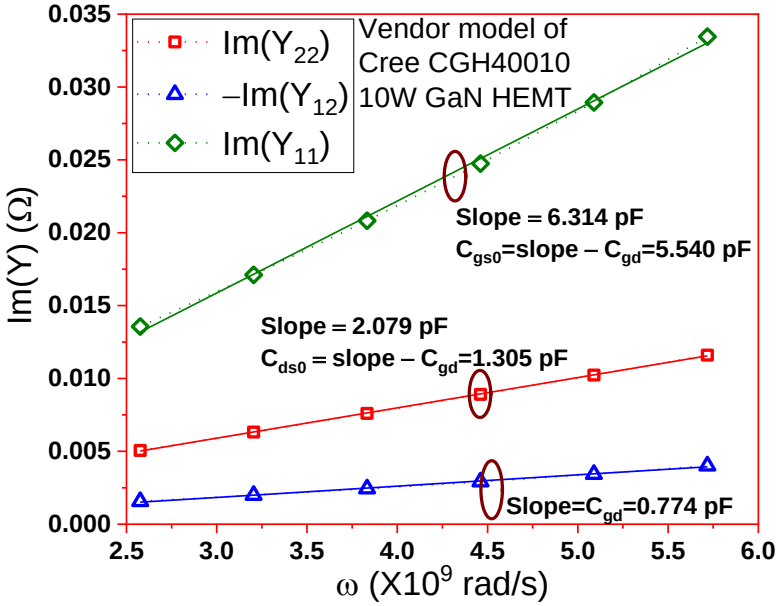


Figure 3.4: Extraction of the branch capacitors (C_{ds0}, C_{gs0}, and C_{gd}) from the simulated Y-parameters of the device at cold pinch-off condition ($V_{gs} < V_{th}$ and $V_{ds} = 0\ V$)

hence cannot be applied to different devices [3.19]. To extract the extrinsic capacitances, instead, we use a simplified version of the TECR (Technology-related Empirical capacitance ratios) algorithm [3.18][3.20] shown in figure **3.5**.

In this algorithm, the pad capacitances (C_{pd} and C_{pg}) are swept and the error (ϵ_S) between the S-parameter of the equivalent circuit (S^M) in figure **3.2** and the S-parameter of the vendor model under *cold pinch-off condition* (S^V) is calculated. The pad capacitances that result in the minimum error (ϵ_S) is selected as the value of the capacitance. The error (ϵ_S) is defined as [3.20]

$$\epsilon_S = \frac{1}{N}\sum_{n=1}^{N}\left|\left|\epsilon^*(f_n)\right|\right|_1 \tag{3.6}$$

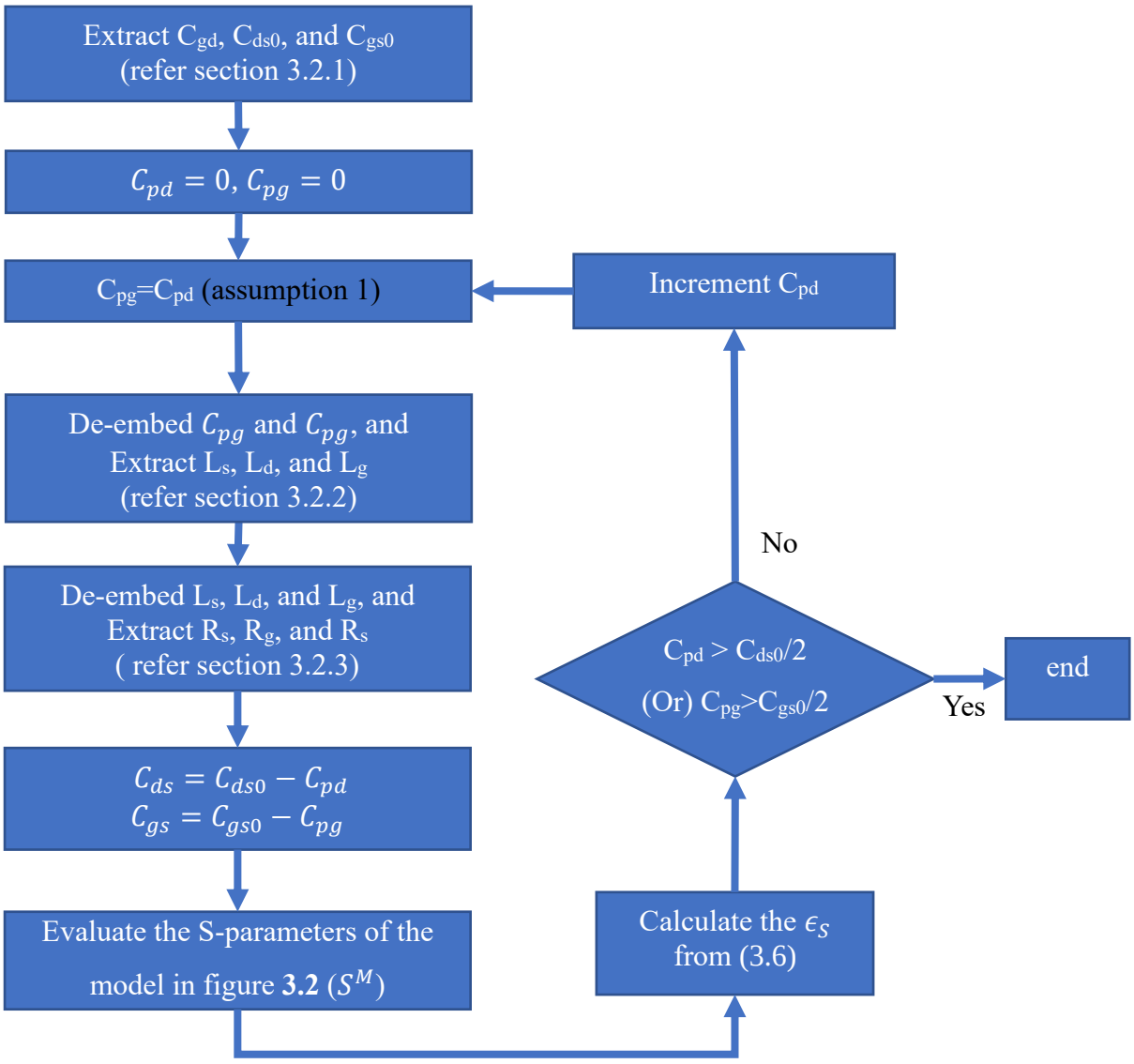


Figure 3.5: The flow chart of the algorithm used for extraction of the pad capacitances.

Where N denotes the total number of data points, f_n denotes the frequency of the nth data point and the error between S-parameters S^V and S^M at the frequency f_n is defined as

$$\epsilon^*(f_n) = \begin{bmatrix} \frac{\Delta S_{11}(f_n)}{1+|S_{11}^V(f_n)|} & \frac{\Delta S_{12}(f_n)}{\max\left(S_{21}^V(f_n), S_{12}^V(f_n)\right)} \\ \frac{\Delta S_{21}(f_n)}{\max\left(S_{21}^V(f_n), S_{12}^V(f_n)\right)} & \frac{\Delta S_{22}(f_n)}{1+|S_{22}^V(f_n)|} \end{bmatrix} \tag{3.7}$$

Where,

$$\Delta S_{ij} = |Re(S_{ij}^V(f_n) - S_{ij}^M(f_n))| + |Im(S_{ij}^V(f_n) - S_{ij}^M(f_n))| \tag{3.8}$$

The output of the TECR algorithm ie., ϵ_S as pad capacitance is varied from 0 to 600 fF is plotted in figure **3.6**. Based on this plot, the values of C_{pg} and C_{pd} are chosen as 0.460 pF. Only the extraction of the pad capacitance is different from the extraction procedure utilised by our group in [3.5] whereas the extraction of the extrinsic inductances and resistance is the same reported in [3.5].

3.2.2. Extraction of extrinsic inductance

The extrinsic inductances are extracted from the S-parameters under cold forward (V_{ds}=0 and V_{gs}>$V_{pinchoff}$) condition [3.19]. The equivalent circuit of the device under this condition after de-embedding the pad capacitances is shown in figure 3.7. The Pi configuration of the intrinsic capacitances is converted into a T configuration to ease the extraction process. R_{ch} in the figure denotes the channel resistance.

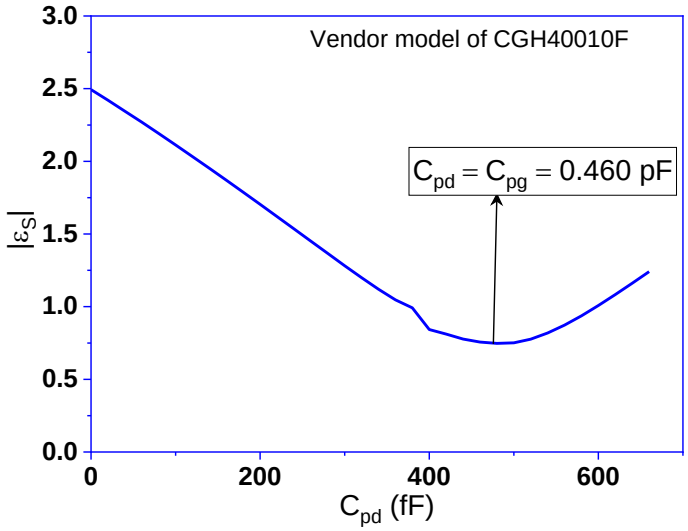


Figure 3.6: Error (ϵ_S) as the pad capacitance varied from 0 pF to 660 fF (=C_{ds0}/2). The S-parameters of the device at cold pinch-off condition ($V_{gs} < V_{th}$ and $V_{ds} = 0\ V$)

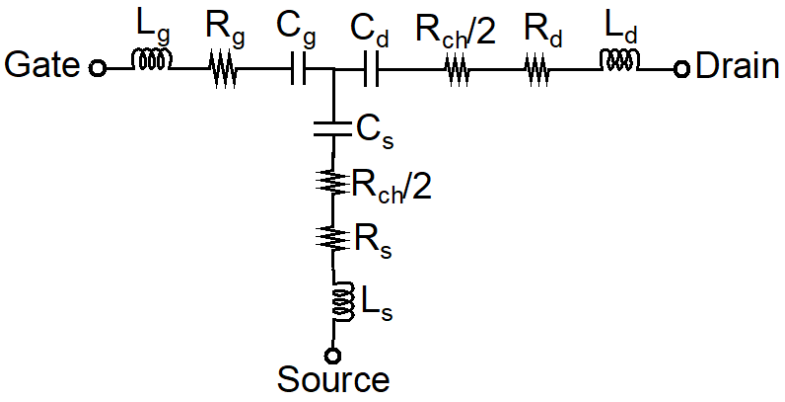


Figure 3.7: Equivalent circuit at cold forward condition

The Z-parameters of this equivalent circuit can be expressed as

$$Z_{11} = R_s + R_g + \frac{R_{ch}}{2} + j\left[\omega(L_s + L_g) - \frac{1}{\omega C_g} - \frac{1}{\omega C_s}\right] \tag{3.9}$$

$$Z_{12} = Z_{21} = R_s + \frac{R_{ch}}{2} + j\left[\omega L_s - \frac{1}{\omega C_s}\right] \tag{3.10}$$

$$Z_{22} = R_d + R_s + R_{ch} + j\left[\omega(L_s + L_d) - \frac{1}{\omega C_s} - \frac{1}{\omega C_d}\right] \tag{3.11}$$

Extrinsic inductances L_s, $L_g$and L_d can be determined from the slope of $\omega Im(Z_{ij})$ plotted against ω^2 as shown in figure **3.8**.

3.2.3. Extraction of resistances

There are four unknown resistances in equations (3.7)-(3.9), but only three relationships can be obtained by equating real parts of these equations. This has been overcome in the formulation proposed in [3.18]. First, extrinsic capacitances and inductances are de-embedded from the measured s-parameters to obtain the Z parameter Z^{Rcold}. The Z^{Rcold} can be related to extrinsic resistances as [3.18]

$$\frac{Re(Z_{22}^{Rcold})}{Im(Z_{22}^{Rcold})}\omega \approx -\frac{1}{C_{ch}R_{ch}} + \frac{\omega}{Im(Z_{22}^{Rcold})}(R_d + R_s) \tag{3.12}$$

$$\frac{Re(Z_{12}^{Rcold})}{Im(Z_{22}^{Rcold})}\omega \approx -\frac{\beta}{C_{ch}R_{ch}} + \frac{\omega}{Im(Z_{22}^{Rcold})}Rs \tag{3.13}$$

$$\frac{Re(Z_{11}^{Rcold})}{Im(Z_{22}^{Rcold})}\omega \approx -\frac{\alpha}{C_{ch}R_{ch}} + \frac{\omega}{Im(Z_{22}^{Rcold})}(R_g + R_s) \tag{3.14}$$

R_s can be obtained from the slope of $\frac{Re(Z_{12}^{Rcold})}{Im(Z_{22}^{Rcold})}\omega$ plotted against $\frac{\omega}{Im(Z_{22}^{Rcold})}$. Similarly, R_d and R_g can be obtained from the slopes of $\frac{Re(Z_{22}^{Rcold})}{Im(Z_{22}^{Rcold})}\omega$ and $\frac{Re(Z_{11}^{Rcold})}{Im(Z_{22}^{Rcold})}\omega$ respectively. The extraction of the resistances is shown in figure **3.9**.

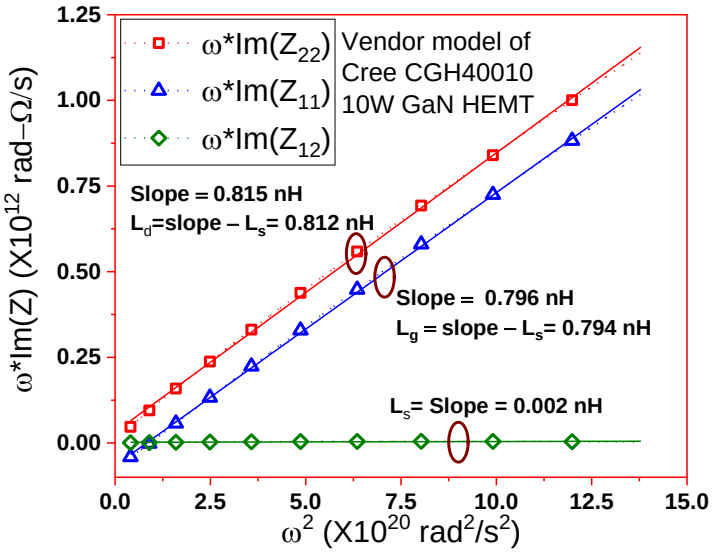


Figure 3.8: Extraction of the inductances (L_d, L_g, and L_s) from the simulated Z-parameters of the device at cold forward condition ($V_{gs} > V_{th}$ and $V_{ds} = 0\,V$). For this figure, C_{pd}=C_{pg}=460 pF is used.

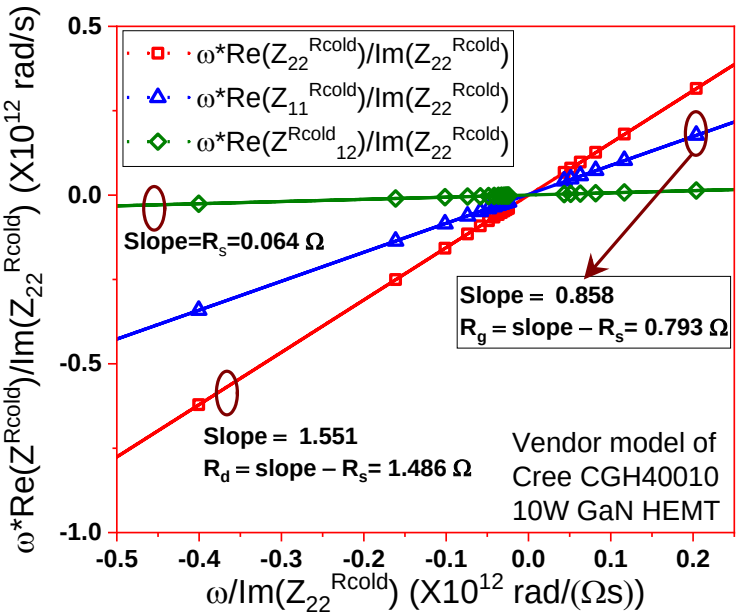


Figure 3.9: Extraction of the resistance from the simulated Z-parameters of the device at the cold forward condition ($V_{gs} > V_{th}$ and $V_{ds} = 0\,V$). The pad capacitances and extrinsic inductances obtained in figures **3.6** and **3.8** respectively are de-embedded.

3.2.4. Extraction of intrinsic parameters

The calculated extrinsic elements are de-embedded from the S-parameters of the device at the bias point to obtain the Y parameters of the intrinsic device. The equivalent circuit of the intrinsic device is shown in figure 3.10.

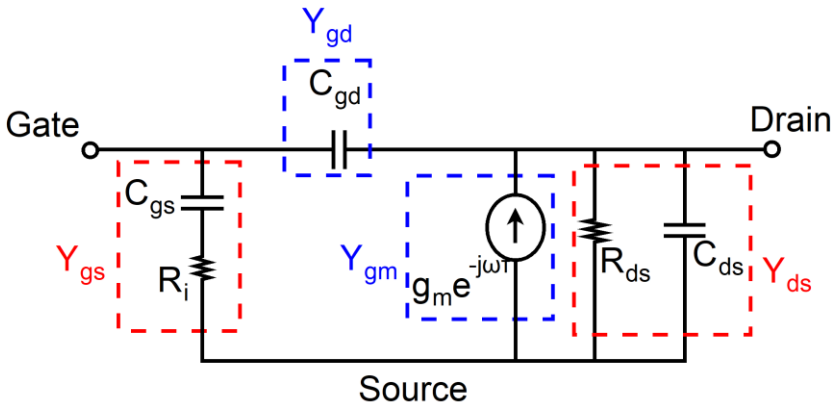


Figure 3.10: The equivalent circuit of the intrinsic device

The Y parameters of the intrinsic device (Y^i) can be expressed as [3.17]

$$Y_{11}^i = \frac{R_i C_{gs}^2 \omega^2}{D} + j\omega\left(\frac{C_{gs}}{D} + C_{gd}\right) \qquad Y_{12}^i = -j\omega C_{gd} \tag{3.15}$$

$$Y_{21}^i = \frac{g_m \exp(-j\omega\tau)}{1 + jR_i C_{gs}\omega} - j\omega C_{gd} \qquad Y_{22}^i = g_{ds} + j\omega\left(C_{ds} + C_{gd}\right) \tag{3.16}$$

Where $D = 1 + \omega^2 C_{gs}^2 R_i^2$.

Since $\omega^2 C_{gs}^2 R_i^2 \approx 0$ for low frequencies [3.18][3.17], the admittance (Y_{gs}, Y_{gd}, Y_{gm}, and Y_{ds}) of the branches of the equivalent circuit can be approximated as

$$Y_{gs} = Y_{11}^i + Y_{12}^i \approx R_i C_{gs}^2 \omega^2 + j\omega C_{gs} \tag{3.17}$$

$$Y_{gd} = -Y_{12}^i = j\omega C_{gd} \tag{3.18}$$

$$Y_{gm} = Y_{21}^i - Y_{12}^i = \frac{g_m \exp(-j\omega\tau)}{1 + jR_i C_{gs}\omega} \tag{3.19}$$

$$Y_{ds} = Y_{22}^i + Y_{12}^i = g_{ds} + j\omega C_{ds} \tag{3.20}$$

The individual elements from equations were separated as [3.18][3.19]

$$\omega C_{gs} \approx \frac{\left|Y_{gs}\right|^2}{Im\left(Y_{gs}\right)} = \left(Im(Y_{11}) + Im(Y_{12})\right)\left(1 + \frac{\left(Re(Y_{11}) + Re(Y_{12})\right)^2}{\left(Im(Y_{11}) + Im(Y_{12})\right)^2}\right) \tag{3.21}$$

$$\omega C_{gd} = Im\left(Y_{gd}\right) = -Im\left(Y_{12}^{i}\right) \tag{3.22}$$

$$\omega C_{ds} = Im(Y_{ds}) = Im(Y_{22}) + Im(Y_{12}) \tag{3.23}$$

$$g_{ds} = Re(Y_{ds}) = Re(Y_{22}) + Re(Y_{12}) \tag{3.24}$$

$$\omega R_i = \frac{1}{C_{gs}}\left(\frac{Re\left(Y_{gs}\right)}{Im(Y_{gs})}\right) = \frac{Re(Y_{11}) + Re(Y_{12})}{C_{gs}\left(Im(Y_{11}) + Im(Y_{12})\right)} \tag{3.25}$$

Using the approximation that $\omega^2 C_{gs}^2 R_i^2 \approx 0$ for low frequencies, following [3.18], g_m and τ can be obtained from the relationships:

$$\left(\frac{1}{g_m}\right)^2 \omega^2 = \frac{1}{C_{gs}^2}\left|\frac{Y_{gs}}{Y_{gm}}\right|^2 \tag{3.26}$$

$$\omega\tau = -phase\left(j\omega C_{gs}\left(\frac{Y_{gm}}{Y_{gs}}\right)\right) \tag{3.27}$$

The extraction process of C_{gs}, C_{ds}, C_{gd}, g_{ds}, R_i, g_m, and τ of vendor model of CGH40010 at V_{ds}=28 V and I_{DSq}= 150mA is illustrated in figure **3.11**. The parasitic elements C_{pd}, C_{pg}, L_s, L_d, L_g, R_s, R_d, and R_g, obtained in figures **3.6**, **3.8**, and **3.9**, were de-embedded from the S-parameters of the vendor model.

The extracted elements values need to be optimized to achieve a better match between the S-parameters of the equivalent model and vendor model [3.5][3.18]. Rather than optimizing all the components in a single optimization step, we optimize elements in an eight-step procedure shown in Table **3.1** [3.16]. This partitioning of the optimization problem into steps is based on the relative sensitivity of the S-parameter to the variation of elements. For example, the output reflection coefficient of the device (S_{22}) is the most sensitive to a change in R_{ds} and C_{ds} [3.21] and hence, when these two elements are varied or optimized, the target is to minimize the error in S_{22}. In each step, a selected combination of components, shown in Table **3.1**, is varied to find a least-squares fit of an S-parameter of the equivalent model with the S-parameter of the vendor model. These steps are performed in sequential order and repeated until the average

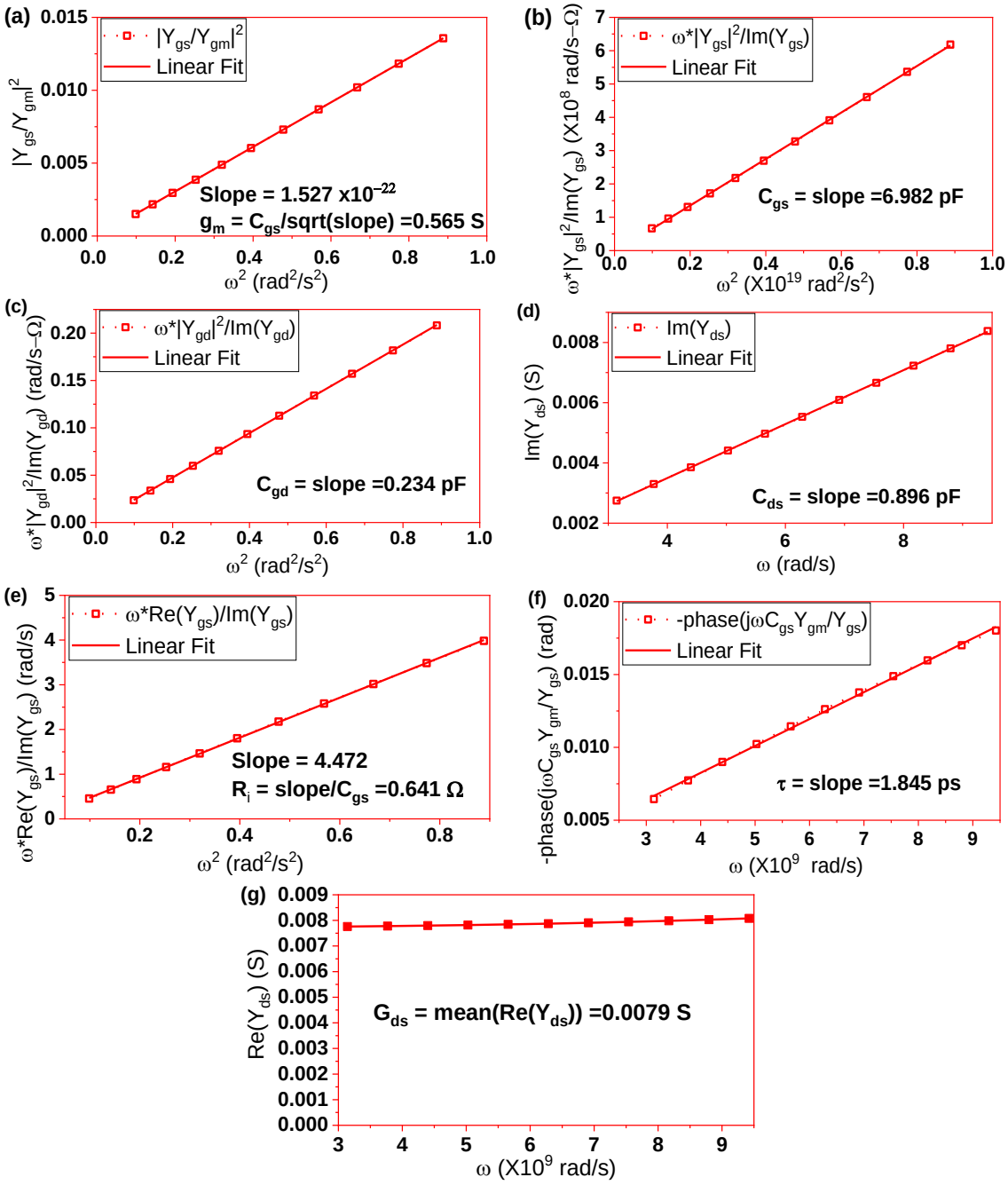


Figure 3.11: The extraction of intrinsic component value from the S-parameter at the bias V_{DSq}=28 V, I_{DSq}=150 mA (a) g_m (b) C_{gs}(c) C_{gd}(d) C_{ds}(e) R_i (f) τ (g) G_{ds}

relative percentage error between the S-parameters of the vendor model and equivalent model (E_{rel}) is minimized. E_{rel} is calculated as

$$E_{rel} = \frac{1}{4N}\sum_{i=1}^{2}\sum_{j=1}^{2}\sum_{n=1}^{N}\frac{\left|S_{ij}^{V}(f_n) - S_{ij}^{M}(f_n)\right|}{\left|S_{ij}^{V}(f_n)\right|} \tag{3.28}$$

Where, f_n denotes the nth sampling frequency.

TABLE 3.1: EIGHT STEPS IN THE ITERATIVE ROUTINE USED FROM OPTIMIZING THE COMPONENT VALUES

Step	Elements optimized	S-parameter fitted	Frequency range
1	R_{ds}, C_{ds}	S_{22}	All
2	C_{gs}	S_{11}	all
3	C_{gd}, R_s	S_{12}	all
4	g_m	S_{21}	all
5	R_d, L_d, C_{pd}	S_{22}	upper half
6	R_g, L_g, C_{pg}, R_i	S_{11}	upper half
7	L_s	S_{12}	upper half
8	τ	S_{21}	upper half

The extracted parasitic elements before and after optimization are summarized in Table 3.2. The percentage change of R_s and L_s is the highest because of the shortfall of the extraction process [3.5]. The large percentage change in τ and R_i can be attributed to error propagation as their accuracy depends on the accuracy of C_{gs}. E_{rel} before and after optimization are 8% and 5.9% respectively over the frequency range 0.5 GHz to 6 GHz. The S-parameters of the extracted equivalent model after optimization and the vendor model over the frequency range 0.5 GHz to 6 GHz are plotted in figure **3.12**. It is seen that they are in close agreement.

3.2.5. Extraction of intrinsic elements at gate and drain voltages other than the bias point

Non-linear capacitances are extracted from the vendor model of CGH40010 as they were required for a qualitative study in chapter 5. S-parameters of the device are generated for the gate and drain voltages in the range of -4 to -1 V and 0 V and 28 V. The extrinsic elements in Table **3.1** are de-embedded to obtain Y-parameters (Y^m) of the intrinsic device. Rather than extracting the intrinsic component by data-fitting followed by optimization, we have used analytical expressions for the intrinsic component value that minimizes the l_2 norm of the error between the equivalent model and vendor model [3.22][3.23]. This is because the extraction method based on analytical expressions provides values in a single step and is easier to program in Matlab. The analytical expressions were given as[3.22][3.23]:

$$R_i = \frac{\sum_k Re\left(Y^m_{gs,k}\right)}{\sum_k \left|Y^m_{gs,k}\right|^2} \; ; \; C_{gs} = \frac{\frac{1}{2\pi}\sum_k \left(\left|Y^m_{gs,k}\right|/f_k\right)^2}{\sum_k Im\left(Y^m_{gs,k}\right)/f_k} \tag{3.29}$$

$$G_{ds} = \frac{\sum_k Re\left(Y^m_{ds,k}\right)/f_k}{\sum_k 1/f_k} \; ; C_{ds} = \frac{1}{2\pi}\frac{\sum_k Im\left(Y^m_{ds,k}\right)}{\sum_k f_k} \tag{3.30}$$

$$C_{gd} = \frac{1}{2\pi}\frac{\sum_k \left(\left|Y^m_{gd,k}\right|/f_k\right)^2}{\sum_k Im\left(Y^m_{gd,k}\right)/f_k} \; ; G_m = \frac{\sum_k \left|Y^m_{gm,k}\left(1 + j2\pi f_k C_{gs} R_i\right)\right|/f_k}{\sum_k 1/f_k} \tag{3.31}$$

TABLE 3.2: The extracted parasitic components of the equivalent model from the vendor model of CGH40010 at Idsq=150 mA and Vdsq=28 V

	C_{pg} (in pF)	C_{pd} (in pF)	L_s (in nH)	L_d (in nH)	L_g (in nH)
Before Optimization	0.460	0.460	0.0020	0.812	0.794
After Optimization	0.404	0.404	0.0040	0.790	0.798
% Change	-12.2	-12.2	100.0	-2.7	0.5
	R_s (in Ω)	R_d (in Ω)	R_g (in Ω)	C_{gs} (in pF)	C_{ds} (in pF)
Before Optimization	0.060	1.486	0.793	6.982	0.896
After Optimization	0.040	1.280	0.616	7.332	1.100
% Change	-33.3	-13.9	-22.3	5.0	22.8
	C_{gd} (in pF)	R_{ds} (in Ω)	Gm (in S)	Ri (in Ω)	Tau (in ps)
Before Optimization	0.234	126.582	0.565	0.640	1.845
After Optimization	0.215	113.730	0.581	0.370	2.003
% Change	-8.1	-10.2	2.9	-42.2	8.6

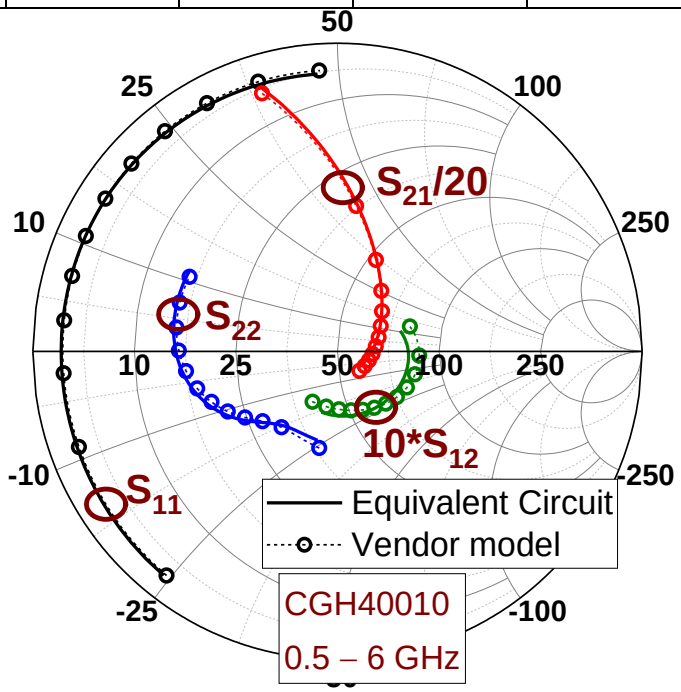


Figure 3.12: The S-parameters of the equivalent model after optimization and the S-parameters of vendor model at V_{dsq}=28 V and I_{dsq}=150 mA

However, these expressions are derived for a transistor operating as a voltage-controlled current source. Hence for the extraction of bias point for which device is off ($V_{gs}<V_{th}$), data fitting as in section 3.2.4 is used. The extracted C_{gs}, C_{gd}, and C_{ds} are plotted in figure **3.13**.

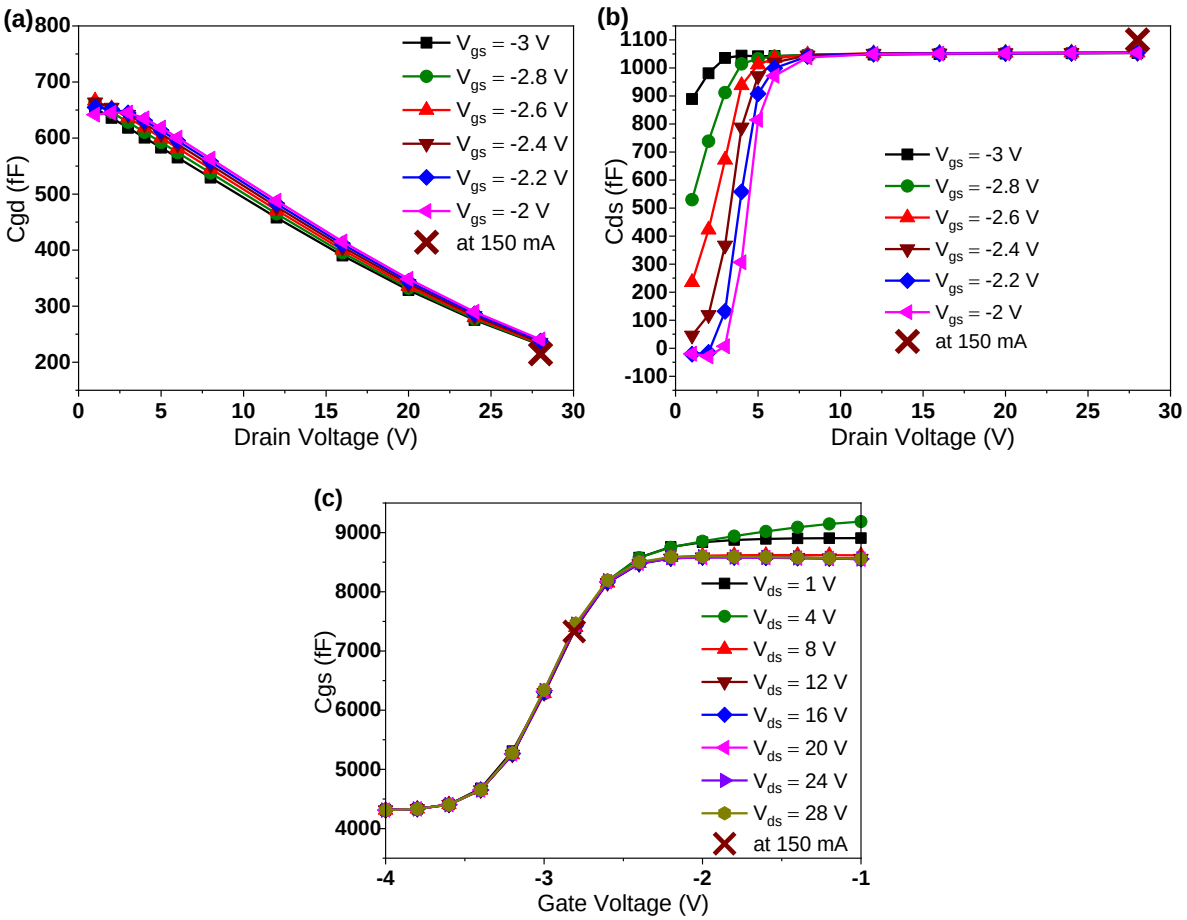


Figure 3.13: Extracted values of (a) C_{gd} (b) C_{ds} (c) C_{gs} from the vendor model for V_{gs} between -2 V and -3 V and V_{ds} between 0 V and 28 V.

Since these non-linear capacitances are required only for qualitative analysis, we have not performed the optimization as in section 3.2.4 to improve the accuracy of the extracted component values. For all the amplifier simulation during design in this thesis, we have used the existing vendor model.

3.3. Embedding and De-embedding procedure

The simulation using the vendor models are performed at the device plane whereas theoretically calculated impedances are at the current generator plane of the device. Hence the obtained impedances need to be translated to the current generator plane to obtain the corresponding impedances at the extrinsic plane. This is referred to as “embedding”. In a similar fashion, the impedance at the extrinsic plane of the device needs to be translated to the intrinsic plane to confirm the class of amplifier, which is referred to as “de-embedding”.

The approximated parasitic model consisting of C_{ds}, R_d, L_d, and C_{pd}, shown in figure **3.14**, at the drain of the device is used [3.10][3.24][3.25] to gain access to the current generator plane.

This is valid because C_{gd} is one order of magnitude less than C_{ds} and, L_s and R_s are negligibly small, as can be seen from Table 3.2. However, this parasitic model consists of only 4 elements resulting in an error from the actual value. However, it is favoured because of its simplicity and has been extensively used in the design of continuum-based amplifiers. Additionally, the aim is to estimate approximately the impedances at which load-pull needs to be performed.

For the de-embedding process, the approximate parasitic network is simulated by placing the load $Z_{extrinsic}$ at the package plane to obtain the corresponding impedance at the intrinsic plane. Vendor models (from Cree) provide the current and voltage waveforms at the intrinsic current generator plane, upon simulating the model with $Z_{extrinsic}$. In this case, accurate $Z_{intrinsic}$ can be obtained directly from the model itself. Nevertheless, the estimation of $Z_{intrinsic}$ is required for a real device or in the simulation if the model does not provide access to the internal waveforms.

The embedding can be performed in a CAD design environment by using the negated version of the parasitic model ie., using the negative value for the parasitics, as shown in figure **3.14** [3.10]. The $Z_{extrinsic}$ can be calculated from the simulation of this negated version of the network

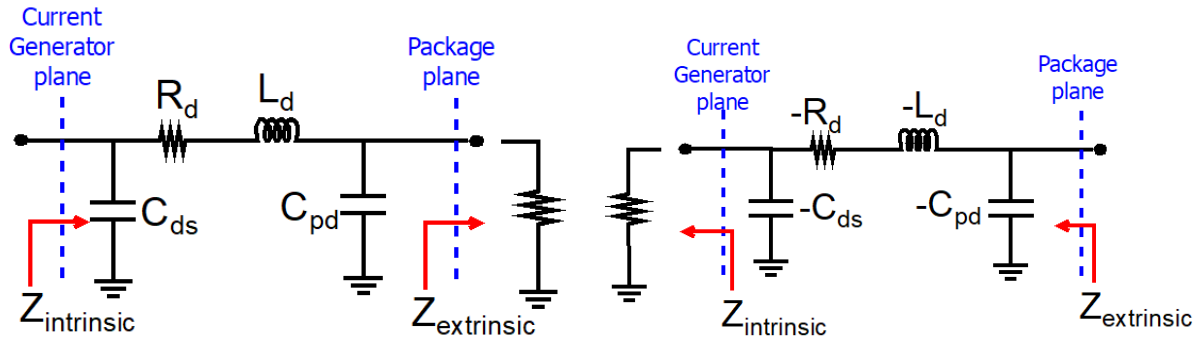


Figure 3.14: (a) Approximated parasitic model at the drain of a GaN HEMT (b) Negated version of the parasitic model. $Z_{intrinsic}$ and $Z_{extrinsic}$ denote the impedances at current generator plane and device plane respectively.

with $Z_{intrinsic}$ at the current generator plane. This process of embedding is required even with the cree models, as they do not allow to place the impedance at the intrinsic plane.

An example of the embedding and de-embedding process is illustrated using the CGH40010 for the fundamental impedances of classes B, J, F^{-1}, and CCF^{-1} in figure **3.15** (a) and (b). The theoretical optimal load line resistances for CGH40010 are reported between 32 Ω and 38.1 Ω and hence the theoretical impedances are calculated for these values. The calculated impedances are plotted in figure **3.15** (a). After applying the embedding process illustrated in

figure **3.14**, the corresponding impedances at the extrinsic plane at frequency 2.6 GHz are plotted in figure **3.15** (b).

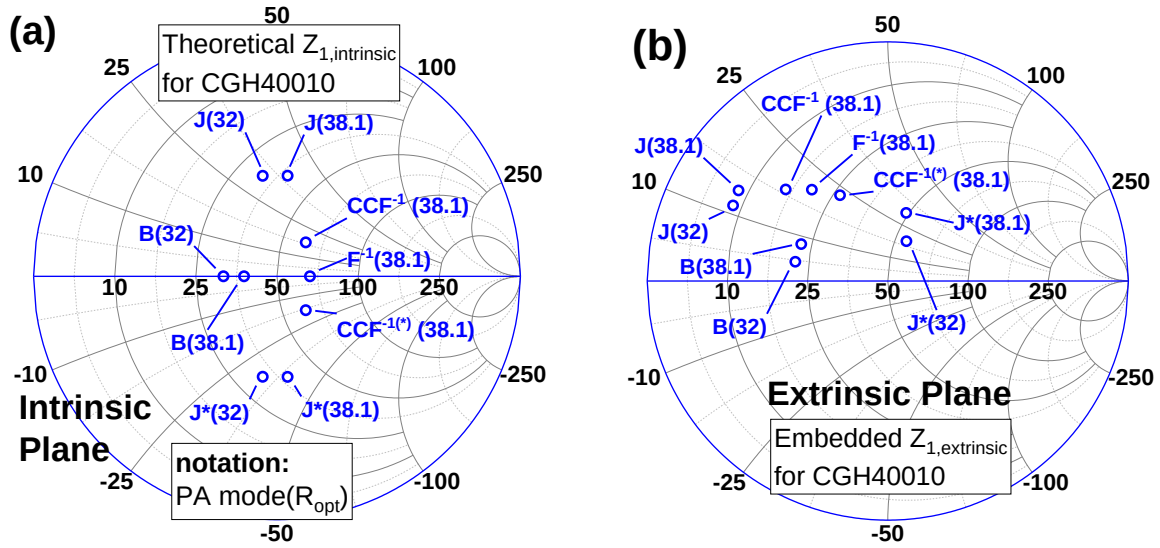


Figure 3.15: The theoretical impedances at the intrinsic plane of classes B, J, J* and CCF^{-1} at the fundamental ($Z_{1,intrinsic}$) frequency are in (a). The corresponding impedances at extrinsic plane after embedding at fundamental ($Z_{1,extrinsic}$) are in (b).

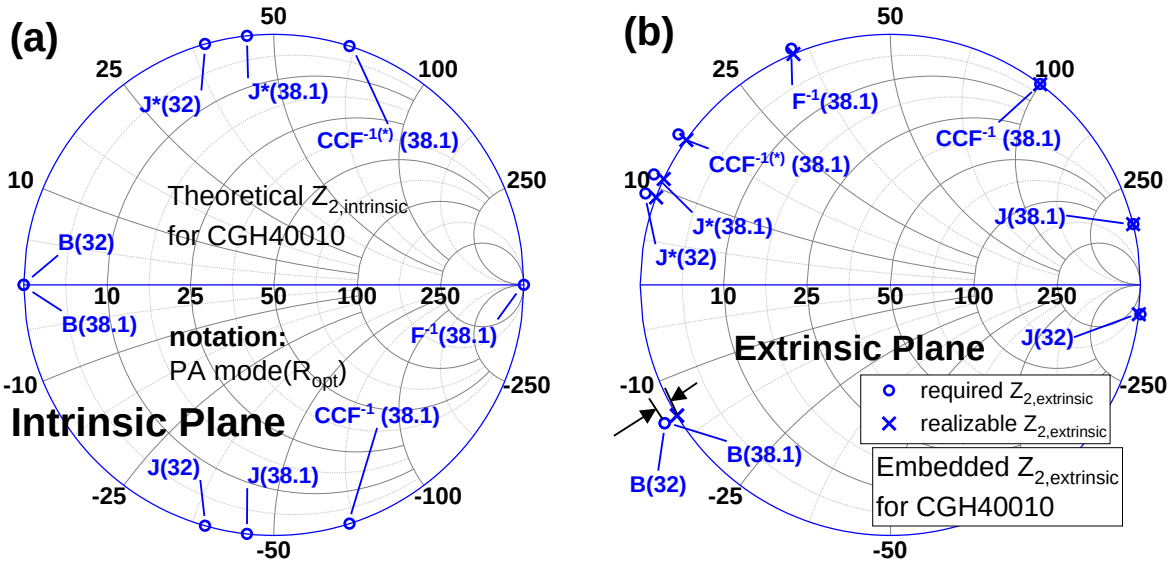


Figure 3.16: The theoretical impedances at the intrinsic plane of classes B, J, J* and CCF^{-1} at the second harmonic ($Z_{2,intrinsic}$) frequency are in (a). The corresponding impedances at extrinsic plane after embedding at second harmonic frequency ($Z_{2,extrinsic}$) are in (b).

In the similar way, we have performed the embedding process for the second harmonic impedances, the theoretical calculated impedances are plotted in figure **3.16** (a) and the corresponding impedances at the extrinsic plane at frequency 5.2 GHz are plotted in figure **3.16** (b). It can be observed in figure **3.16** (b) that some second harmonic impedances have negative

real part indicating that an active load (which supplies the second harmonic to the device) is required for these impedances. This additional second harmonic is required to compensate for the attenuation due to R_d. Hence, for it to be realizable with a passive matching network, we replace the negative part of these impedances with zero resulting in a corresponding approximated second harmonic impedance, which is (denoted by X) plotted in figure **3.16** (b).

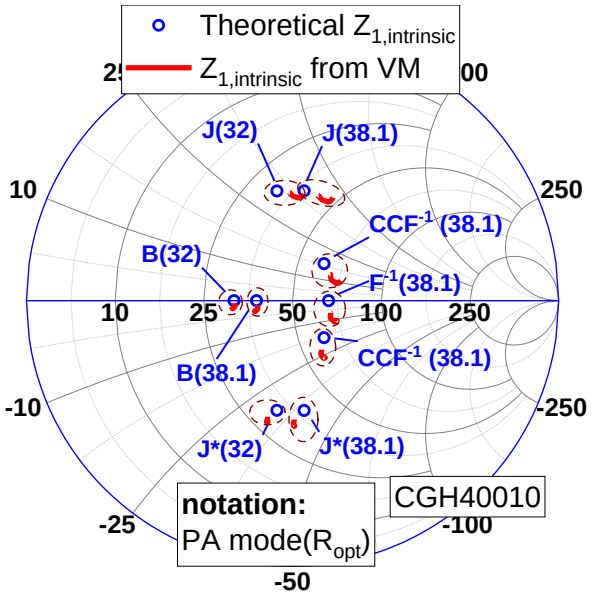


Figure 3.17: The impedances at the intrinsic place of the vendor model in simulation compared with the theoretical (target in figure **3.15** (a) and **3.16** (a)) values. The impedances at the fundamental frequency ($Z_{1,intrinsic}$) are compared with theoretical values.

We simulate the vendor model with the fundamental and the corresponding second harmonic impedance in figure **3.15** (b) and **3.16** (b) respectively. We sweep the input power to the device in the harmonic balance simulation and the intrinsic impedances are calculated as the ratio of the intrinsic voltage and current waveforms generated by the vendor model. The intrinsic impedances calculated from the vendor model are compared with the theoretical impedances (in figure **3.15** (a)) at fundamental frequency in figure **3.17**. The fundamental impedances from the vendor model can be seen to be very close to the theoretical values, however, they depend slightly on the input power level.

The comparison of the intrinsic impedances calculated from the vendor model are compared with the theoretical impedances (in figure **3.16** (a)) at the second harmonic frequency ($Z_{2,intrinsic}$) is plotted in figures **3.18** (a), (b), and (c). The simulated $Z_{2,intrinsic}$ change quite considerable with input power in the case of the second harmonic frequency. In the case of class B in figures **3.18** (a) and (b), and CCF^{-1} in **3.18** (c), the real part of $Z_{2,intrinsic}$ becomes negative. This indicates

that the device may become unstable for these power levels. $Z_{1,intrinsic}$ and $Z_{2,intrinsic}$ change with input power because of the harmonic non-linear capacitances (C_{gd} and C_{gs}) at low power level [3.26] and the knee region at a high power level. The simplified parasitic network fails to predict the second harmonic impedances. The discrepancy between $Z_{2intrinsic}$ from the Vendor model and the simple parasitic network is much larger when $Z_{2intrinsic}$ is greater than zero ie., $Z_{2intrinsic}$ is inductive. This larger discrepancy for inductive $Z_{2intrinsic}$ can in part be attributed to the larger discrepancy between the required and realized impedance for the inductive than the capacitive $Z_{2intrinsic}$ in figure **3.16** (b). Hence, in this work, we slightly adjust the impedances at fundamental frequency whereas we use load-pull simulation at the second harmonic frequency to choose the second harmonic impedances which results in higher efficiency.

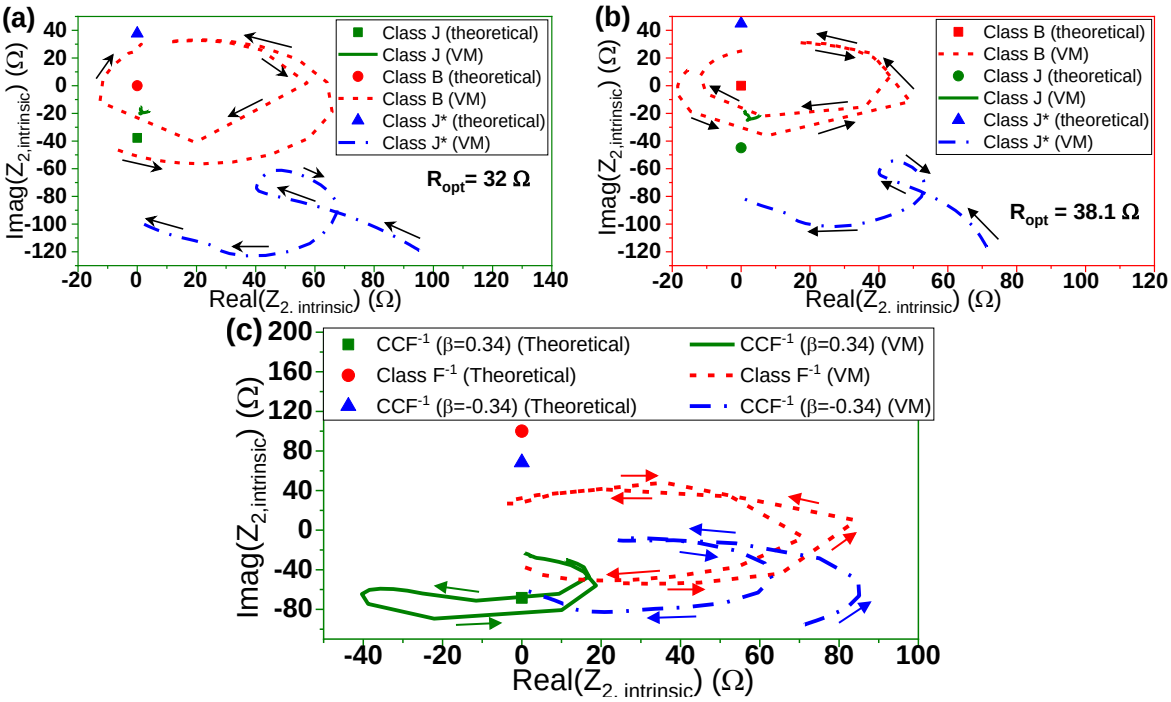


Figure 3.18: The impedances at the intrinsic place of the vendor model in simulation compared with the theoretical (target in figure **3.15** (a) and **3.16** (a)) values. The impedances at the second harmonic frequency ($Z_{2,intrinsic}$) for classes B, J, and J* for R_{opt}=32 Ω and R_{opt}=38.1 Ω are compared in (a) and (b) respectively whereas the comparison for CCF^{-1} is in (c). The arrows in the (a), (b), and (c) denote the direction of change in impedances as power increases.

3.4. EM simulation methods in ADS[2]

ADS has three EM simulation modes viz., momentum RF, momentum microwave and FEM (Finite element method). Momentum is based on a division of the layout into 2D cells (square or trapezoid) using a 2D mesh and the method of moments to calculate the currents flowing

[2] ADS stands for Advanced Design System

through the layout. On the other hand, FEM is based on division of the layout into tetrahedral cells using a 3D mesh to calculate the electric and magnetic fields for each cell using Maxwell's equations. The meshes used in FEM and Momentum are shown in figure 3.19. The mesh should be fine enough to discretize the smallest structure in the layout [3.27] to obtain accurate results. However, the time of simulation increases with a decrease in cell size. Hence, starting with a coarse mesh, simulations should be performed by decreasing the size of the mesh until the results of interest, in this case, S-parameters, do not change.

Momentum can provide accurate predictions for planar structures. FEM can provide accurate results for 3D structures as well. However, it is computationally intensive and requires considerable simulation time than momentum microwave. EDA software such as EMPro and CST can perform FDTD (finite difference time domain) simulation which is as accurate than FEM [3.27]. However, FEM is found to be accurate enough in predicting the performance of microstrip lines.

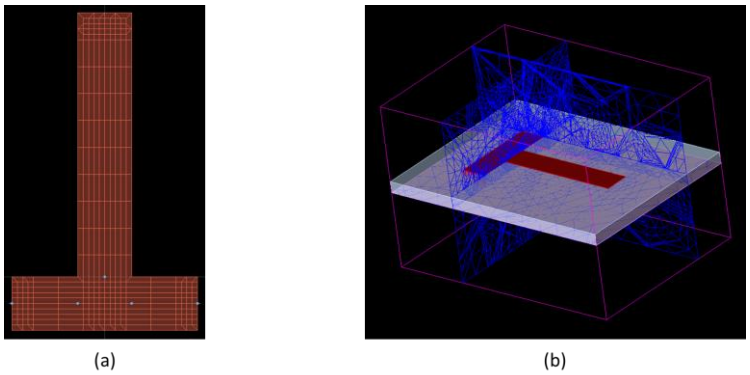


Figure 3.19: Mesh used in (a) Momentum and (b) FEM

Signals in microstrip lines are evaluated as electromagnetic waves in EM simulations. Whereas, signals through lumped elements and transistors are evaluated as voltages and currents. This requires the conversion of voltages and currents into EM waves and vice-versa at some point in the circuit. ADS handles this conversion by extracting the S-parameters of the laid out microstrip lines. The evaluated S-parameters are used in the simulation of the entire circuit with lumped elements.

The S-parameters of the layout are calculated by ADS by exciting the layout with fictitious current sources, connected to the layout at points where the lumped elements are connected in the schematic. The excitation to be supplied by the current sources depends on the corresponding component. For example, since the input and output of the amplifier are connected to an RF power source and meter respectively, a fictitious current generator

connected to the input and output needs to be specified as the RF source. On the other hand, a fictitious current generator connected in the place of biasing voltage source needs to be defined as DC current generator. Ports and pins are used in ADS to define the excitation generated by the fictitious current generator.

3.4.1. Pins and ports

Pins are placed at the location where components are connected in the layout. The terminal fictitious current generator is connected to the pin. The pin can be a single point or can have finite length. In the case of point pins, shown in figure **3.20** (a), the excitation is applied over the entire width of the edge of the microstrip line. This is not an accurate physical representation of the actual circuit if there is an appreciable difference between the widths of the package leads of the component and microstrip lines. Even with this inaccurate representation, the performance of the RF PA can be predicted accurately [3.28]. The effect of this difference is more pronounced in the case of active devices [3.29]. Edge pin is a way to define the width of the package leads in ADS. Edge pins, shown in figure **3.20** (b), in ADS are simulated with a constant voltage throughout the pin. The EM simulations [3.30] performed on the package of the transistor reveals that voltage varies across the width of the lead. Hence approximating the contact between the transistor and microstrip line as edge pin leads to inaccuracy in the result. In the absence of knowledge of the package and connections of the transistor, the simulation can be performed with the edge pin with an understanding that the accuracy of the results is limited.

Ports consist of two or more pins. If only one pin is assigned to the port, the other pin is assumed to be the ground pin, which lies on the bottom layer of the microstrip line, as shown in Figures **3.20** (a) and **3.20** (b). For the components connected to the top layer of the microstrip, both the pins are on the top layer as shown in figure **3.20** (c). This configuration is called a differential port.

3.4.2. Port Calibration

EDA software allows a range of settings to accurately model the coupling effects arising from the connected lumped components. This is handled in ADS by calibrating the ports. Before performing the simulation, each port is calibrated to remove or consider the parasitic effects. The calibration techniques should be chosen according to the available model of the lumped element. The different calibration techniques supported by ADS are:

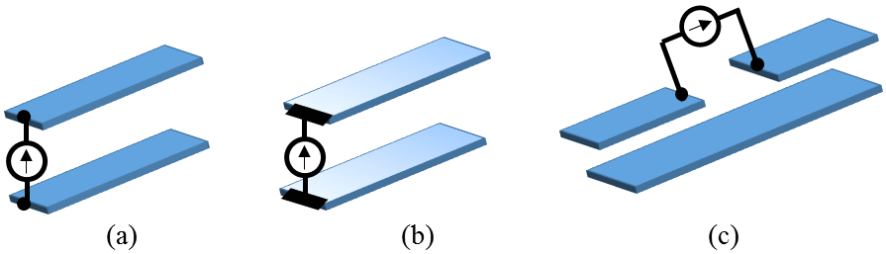


Figure 3.20: (a) Port with point pins (b) Port with edge pins (c) Differential port

1) TML (TransMission Line): A transmission line of the same impedance whose length is calculated based on the frequency of interest is connected to the port as shown in figure **3.21** (a). The EM effects of the inserted calibration transmission line are removed by de-embedding its s-parameters. This calibration should be used when a transmission line is connected to the port. The transmission line of zero length, i.e., a current source directly connected to the port, can be used if the transmission line extension used in TML calibration intersects with metal in the same layer.

2) Delta gap and SMD calibration: When an SMD (surface mount device) component is placed in the layout, mutual coupling arises between the pads and the neighbouring components. A delta gap should be used for the SMD components if the parasitic effects arising due to their packages are not known. Whereas, SMD calibration is used if those effects are known. For example, this calibration can be used if S-parameters of the component are obtained from the vendor which includes the effect of packages and pads.

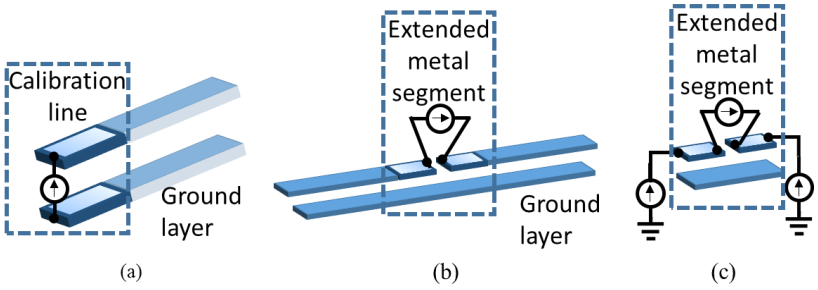


Figure 3.21: (a) TML calibrations setup (b) SMD calibration setup (c) Delta gap calibration setup

Delta gap calibration is performed by extending the metal inward into the gap between the ports as shown in figure **3.21** (b). This extended metal crudely models the parasitic effects arising due to the pads of the surface mount devices. Whereas in SMD calibration, the calibration standard (extended metal) is simulated separately, as shown in figure **3.21** (c), and de-embedded. As de-embedding the calibration standard only removes the self-impedance

arising due to the extended metal, only the coupling between the extended metal and other components is taken into account.

3) **None:** This refers to an uncalibrated port. This can be used when none of the above calibrations is suited for the component. The layout is excited by simply connecting the lumped current source to the port. However, this will provide accurate results only if the length of the port is less than one-tenth of the wavelength at maximum simulation frequency. It has been observed that "none" calibration can give more accurate results than SMD calibration [3.31]. In [3.32], it has been suggested to use SMD calibration if the number of surface mount components is large.

Table 3.3 summarizes which calibration is suitable for which component.

Table 3.3:Calibration type and its applicability

Port calibration	Component connected to the port
TML	Transmission line/Coaxial cable
TML (length zero)	Transmission line/Coaxial cable
Delta gap	Surface mount devices (when the package parasitic are not known)
SMD	Surface mount devices (when the package parasitic are known)*.
Direct (or None)	All components.
Auto	Software will select calibration automatically.

* None calibration can give more accurate results than SMD calibration

3.5. EM simulations results

EM simulations of an output matching network [3.10], a class AB amplifier designed by our group[3.5], and a class J amplifier[3.15] were performed to illustrate the process. The layout of an output matching network reported in [3.10] is shown in figure **3.22** (a). The close agreement of the simulated reflection coefficient and insertion loss with those reported in [3.10] can be observed.

The layouts of the class AB amplifier and the class J amplifier are shown in figures **3.23** and **3.24**(a) respectively. The edge pins are used for a transistor, and the width of the edge pins is set equal to the width of the lead of transistor (1.28mm) [3.33]. "None" calibration is applied to the ports corresponding to the transistor and DC supply. The point pins instead of edge pins are assigned to capacitors and resistors even though they have finite width because the use of edge pins is found inaccurate for SMD components [3.31]. Figures **3.24**(b) and **3.25**(b) reveal a close match between simulated and measured gain and output power. The predicted and

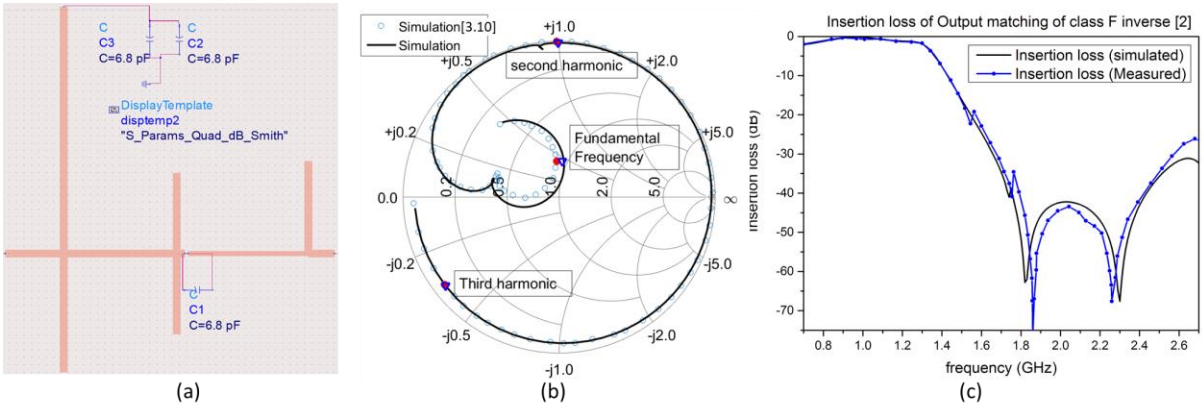


Figure 3.22: (a) Layout of an output matching network [3.10] (b) Comparison of simulated reflection coefficient reported in [3.10] with the simulation in this work (c) Comparison of the measured[3.10] and simulated insertion loss

measured S-parameters of the class AB amplifier are in close agreement as shown in figure **3.25**(a).

PAE is accurately predicted for the class J amplifier, as observed in figure **3.24** (b), whereas large discrepancy between measured and simulated PAE of the class AB can be observed in **3.25** (b) using FEM and momentum. The discrepancy in PAE can be attributed to the model of the device, considering the similarity between the layouts of these two amplifiers and the accuracy of the EM simulations of microstrip lines.

3.6. Summary

We have extracted the small-signal equivalent circuit of the device consisting of 16 elements from the S-parameters of the vendor model of 10W GaN HEMT (CGH40010F). We embed and de-embed the parasitic elements at the drain viz., C_{ds}, R_d, C_{pd}, and L_d to simplify the design process. Embedding and De-embedding process in the CAD environment using this approximate parasitic network is illustrated. It is observed that an approximate parasitic network fails to predict the second harmonic impedances at the intrinsic plane. Hence, the load-pull simulation at second harmonic frequency is used to select the optimal second harmonic impedance in future chapters. The basic insights are provided into how EDA software performs EM co-simulation viz., simulating EM fields in layout and voltage and current of lumped components together. The configuration used at pin and port of the layout depending on the connected lumped component to them is established. EM simulations of amplifiers indicate that device models may be incapable of predicting its performance, especially PAE.

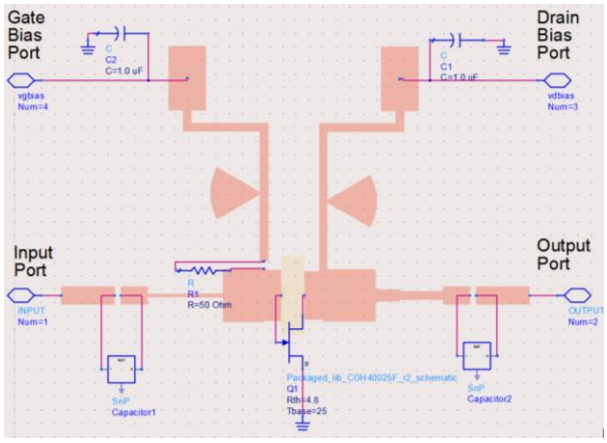
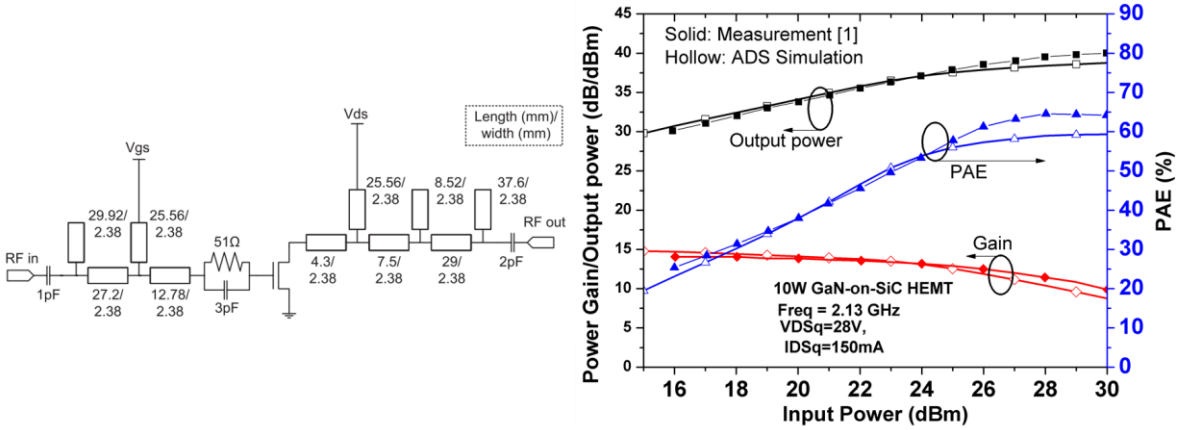
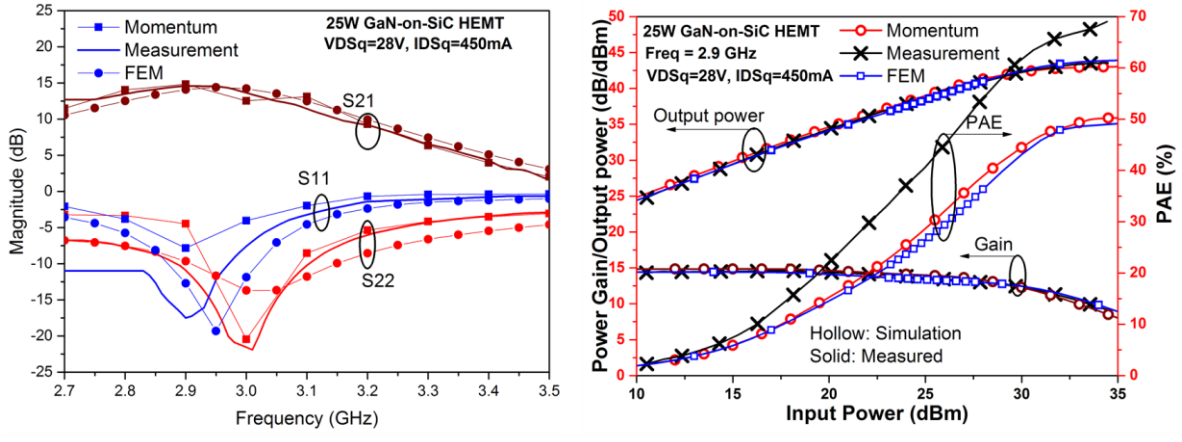


Figure 3.23: Schematic of the amplifier designed using CGH40025[3.33] by our group (VDSq=28V,IDSq=450mA). Amplifier was fabricated on the RO4350B substrate[3.34]. The measured S-parameter of capacitor obtained from vendor are used in simulation.



(a) (b)

Figure 3.24: (a) the schematic of the class J amplifier design in [3.15] (Vds=28V,IDSq=100mA). CGH40010 was as the transistor (b) Measured [3.15] and simulated (Momentum) Gain, Output power and efficiency of the amplifier



(a) (b)

Figure 3.25: Measured and simulated (a) S-parameter and (b) Gain, Output power and efficiency of the amplifier

3.7. References

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Chapter 4: The continuum between classes B/J and Continuous class F^{-1}

4.1. Introduction

The class B/J continuum for amplifier design, proposed by Cripps [4.1], utilizes the second harmonic of voltage to increase the fundamental component through the device. However, such an approach does not benefit the efficiency nor the output power of the amplifier because of the corresponding increase in the mismatch between the phase of the fundamental components of voltage and current [4.2]. This can be illustrated by re-writing the class J continuum voltage waveform [4.1], given in (2.32), in the form of equation (2.28) as

$$V_j = V_{DC} - \delta_v\,(V_{DC} - V_k)\cos\left(\theta + \Psi_{\mathrm{pf(J)}}\right) - \delta_v k_2 (V_{DC} - V_k)\cos(2\theta + \Psi_2) \tag{4.1}$$

Where,

δ_v denotes the voltage gain over the class B or un-manipulated condition

$\Psi_{\mathrm{pf(J)}}$ and Ψ_2 denote the phase difference of the fundamental and second harmonic components of the voltage with the current in class B (given in (4.1)) respectively

k_2 is defined as the ratio of the magnitude of the second harmonic to the fundamental component.

Comparing equations (2.32) with (4.1), the values can be evaluated as

$$\delta_v = \sqrt{1+\alpha^2};\ \Psi_{pf(J)} = \tan^{-1}(\alpha) \tag{4.2}$$

$$k_2 = -\frac{\alpha}{2\sqrt{1+\alpha^2}};\ \Psi_2 = \frac{\pi}{2} \tag{4.3}$$

$$\eta_J = \eta_B \delta_J \cos\left(\Psi_{pf(J)}\right) \tag{4.4}$$

Where, η_J and η_B denote the efficiency of class J and class B respectively.

An increase in the magnitude of this second harmonic by a factor of α/2, where α∈[-1,1], increases the fundamental component of the voltage by $\delta_v\left(=\sqrt{1+\alpha^2}\right)$ but also increases the phase difference between the voltage and current by $\left|\Psi_{pf(J)}\right|$. Voltage gain ($\delta_v$), the magnitude of the phase difference between the voltage and current ($\left|\Psi_{pf(J)}\right|$), power factor ($\cos\left(\Psi_{pf(J)}\right)$), and the ratio of efficiency of class B/J continuum over class B (η_J/η_B) are plotted in Figure **4.1** as α is increased from -1 to 1. It can be seen from the figure, that an increase in $\left|\Psi_{pf(J)}\right|$ with $|\alpha|$ reduces the power factor ($\cos\left(\Psi_{pf(J)}\right)$), and this reduction in power factor compensates the increase in δ_v with $|\alpha|$ resulting in the same efficiency as class B. This shows that even though the manipulation of the second harmonic in class J increases the fundamental

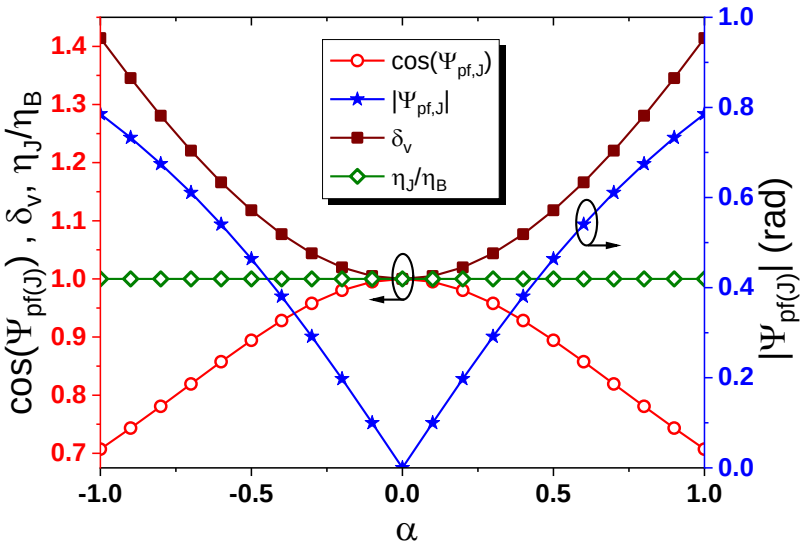

Figure 4.1: Voltage gain (δ_v), the phase difference between the voltage and current ($|\Psi_{pf(J)}|$), power factor ($\cos(\Psi_{pf(J)})$), and the ratio of efficiency of class B/J continuum over class B (η_J/η_B) versus α

component of the voltage flowing through the device, it does not benefit the efficiency. The only benefit of class B/J continuum is its flexibility of design space, as shown in Figure **4.2** (a).

On the other hand, continuous class F^{-1}, proposed by Kim [4.3] relies on the elimination of the in-phase component of the second harmonic and manipulation of the quadrature component of the second harmonic of the current in class J. The voltage waveform of continuous class F^{-1} is the same as that in class J for $|\alpha|=1$ but with fundamental and second harmonic components phase-shifted by $\pi/4$ and $\pi/2$ respectively. This shift in voltage waveform is shown in Figures **4.2** (b) and (c). This shift reduces the phase mismatch from $\pi/4$ in class J to 0 in class F^{-1}, thereby increasing the power factor. As a result, the drain efficiency of class F^{-1} is 91% as opposed to 78.5% in class J with a short at third and higher harmonics.

These classes represent two extremities, of manipulating the second harmonic of the current with an intermediate set of current waveforms shown to exist in [4.2]. We propose a new contiguous set of current waveforms between these classes whereby the in-phase component of the second harmonic of the current in class J is partially removed to achieve higher efficiency.

4.2. Formulation of the proposed continuum

A simplified model of a transistor i.e. a transistor acting as a voltage-controlled current source with unit gain, is assumed in deriving the formulation. The knee voltage and peak current of the transistor are V_k and I_m respectively. The second harmonic manipulated current waveform

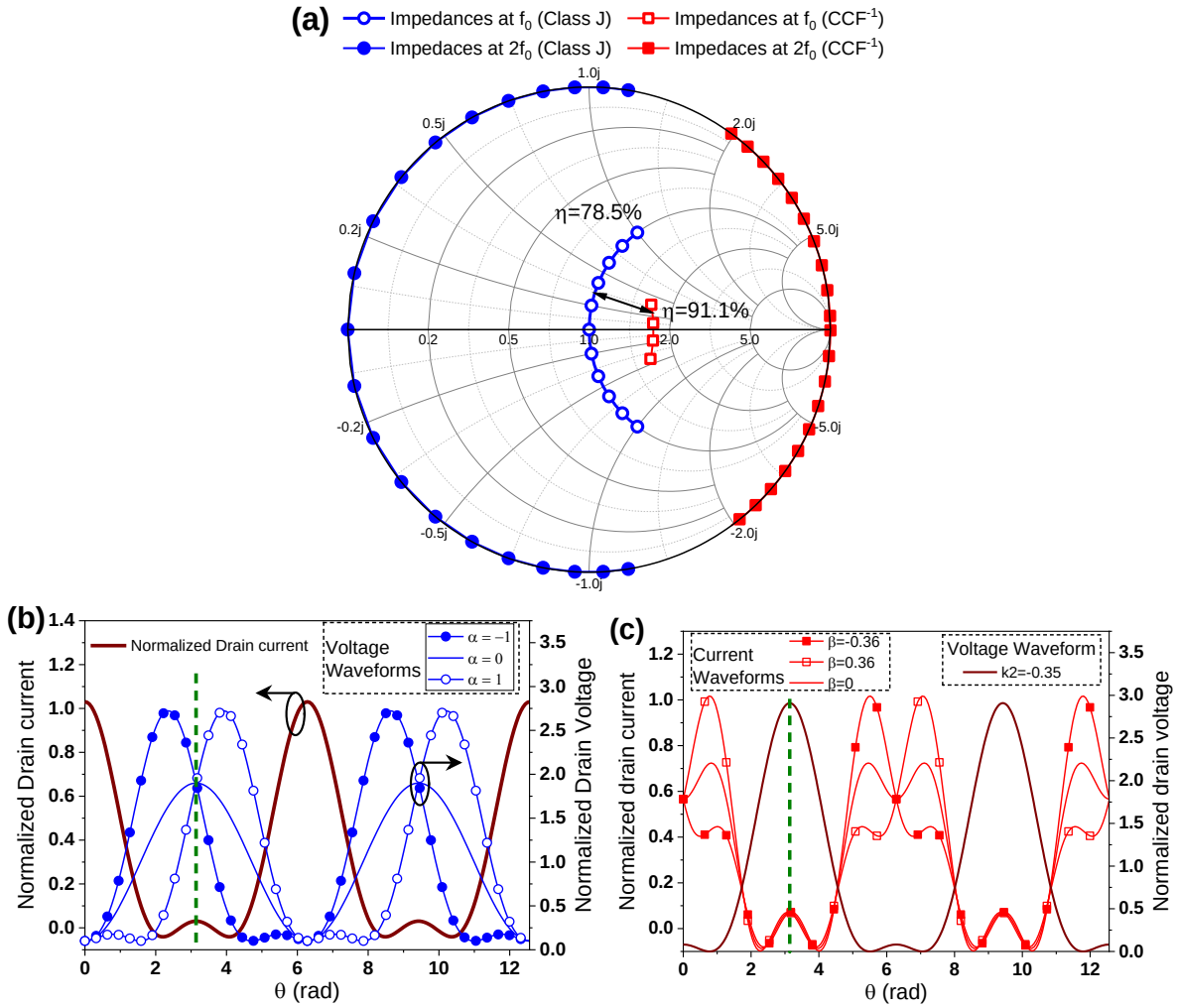

Figure 4.2: (a) Fundamental and second harmonic frequencies of class J and continuous class F^{-1}(CCF^{-1}) at the current generator plane. (b) Voltage and current waveforms of class J (c) Voltage and current waveform of continuous class F^{-1}(CF^{-1})

is derived from conventional class B, consisting of a resistive load at the fundamental frequency, with harmonics shorted.

4.2.1. Current waveforms

The drain current in a class B/J continuum is [4.1]

$$I_{DS(J)}(\theta) = \frac{I_m}{\pi} + \left\{\frac{I_m}{2}\right\}\cos(\theta) + \left\{\frac{2I_m}{3\pi}\right\}\cos(2\theta) + \cdots \tag{4.5}$$

Where, I_m is the maximum current of the device. The fundamental and second harmonic load impedances result in the removal of the second harmonic component ($i_2(\theta)$) from $I_{DS(J)}(\theta)$ [4.3]. The resulting drain current of the device ($I_{ds}(\theta)$), is given as

$$I_{DS}(\theta) = \begin{cases} I_{DS(J)}(\theta) - i_2(\theta) & \left(2p - \frac{1}{2}\right)\pi < \theta < \left(2p + \frac{1}{2}\right)\pi \\ 0 & otherwise \end{cases} \tag{4.6}$$

Where p is an integer. We express $i_2(\theta)$ as in (4.7), wherein, the in-phase component of the second harmonic of the current in class J is partially removed by a factor (k).

$$i_2(\theta) = k\left\{\frac{2I_m}{3\pi}\right\}\{2\cos(2\theta)\} - 2C_Q \sin(2\theta)\,;\ 0 \le k \le 1 \tag{4.7}$$

Where C_Q is an arbitrary real number. The minimum of $|C_Q|$ is zero and the maximum it can attain is such that the peak current of $I_{DS}(\theta)$ is I_m. k = $C_Q = 0$, in class B/J continuum [4.1] whereas k=1 in continuous class F^{-1} [4.3]–[4.5].

we get $I'_{DS}(\theta)$ as

$$I'_{DS}(\theta) = I_{DC} + A_{i1}\cos(\theta) + B_{i1}\sin(\theta) + A_{i2}\cos(2\theta) + B_{i2}\sin(2\theta) + \sum_{n=3}^{\infty}(A_{in}\cos(n\theta) + B_{in}\sin(n\theta)) \tag{4.8}$$

Where,

$$I_{DC} = \frac{I_m}{\pi} \tag{4.9}$$

$$A_{i1} = I_m\left[\frac{1}{2} - \frac{8k}{9\pi^2}\right];\ B_{i1} = \frac{8C_Q}{3\pi} \tag{4.10}$$

$$A_{i2} = \frac{2I_m}{3\pi}(1-k);\ B_{i2} = C_Q \tag{4.11}$$

$$A_{in} = \frac{I_m}{\pi}\left(\frac{\sin\left((n+1)\frac{\pi}{2}\right)}{n+1} + \frac{\sin\left((n-1)\frac{\pi}{2}\right)}{n-1}\right) - \frac{4kI_m}{3\pi^2}\left(\frac{\sin\left((n+2)\frac{\pi}{2}\right)}{n+2} + \frac{\sin\left((n-2)\frac{\pi}{2}\right)}{n-2}\right)(n>2) \tag{4.12}$$

$$B_{in} = \frac{2C_Q}{\pi}\left(\frac{\sin\left((n-2)\frac{\pi}{2}\right)}{n-2} - \frac{\sin\left((n+2)\frac{\pi}{2}\right)}{n+2}\right)(n>2) \tag{4.13}$$

The dependence of quadrature components (B_{in}), in (9) on C_Q demonstrates flexibility in the choice of the reactive component of the fundamental and second harmonic loads. We define β as $\frac{B_{i2}}{A_{i1}}$ to express the quadrature components of the current relative to its in-phase component. β is independent of the device maximum current I_m.

The magnitude of A_{i1} and A_{i2} as k is increased from 0 to 1 is plotted in Figure **4.3** (a). The value of k cannot be less than zero as negative values would cause the peak of the $I'_{DS}(\theta)$ to

exceed the maximum current (I_m). Furthermore, to realize values of k >1 would require negative resistance or a harmonic injection at the second harmonic frequency. The A_{i1} and A_{i2} reduce as k increases from 0 to 1, as can be inferred from (4.10) and (4.11). We define this reduction of the in-phase fundamental component of the current from class B/J as current loss, denoted by δ_{Ii}, given by:

$$\delta_{Ii} = \frac{A_{i1}}{A_{i1|B}} = \frac{A_{i1}}{I_m/2} = 1 - \frac{16k}{9\pi^2} \tag{4.14}$$

The current loss allows the flow of quadrature components through the device. However, the magnitude of the quadrature components (which are proportional to β) cannot result in a total current higher than I_m (device maximum current). The allowed range of the variation of β with k plotted in Figure **4.3** (b), is obtained by simulating the current in (4.8) for each value of k until the peak of the current $I_{DS}(\theta)$ is equal to I_m. The allowed range of β increases as k increases, because of in-phase components (A_{i1} and A_{i2}) flowing through the device decreases.

Typically, an RF power amplifier is matched at most up to 3 harmonics. The approximation of $I'_{DS}(\theta)$ up to 3 harmonics in class BJF^{-1}, are compared with those of Classes J and CCF^{-1} in Figure **4.4**. Figure **4.4** (a) shows the unmanipulated Class J/B current waveform whereas the Class CCF^{-1} waveform in Figure **4.4** (c) may either peak to the right or the left depending upon whether β >0 or β<0. Class BJF^{-1} in the centre (Figure **4.4** (b)) retains the basic characteristics of CCF^{-1}, but the waveforms are, under our ideal conditions, more smoothly peaked on either side depending upon the magnitude and sign of β.

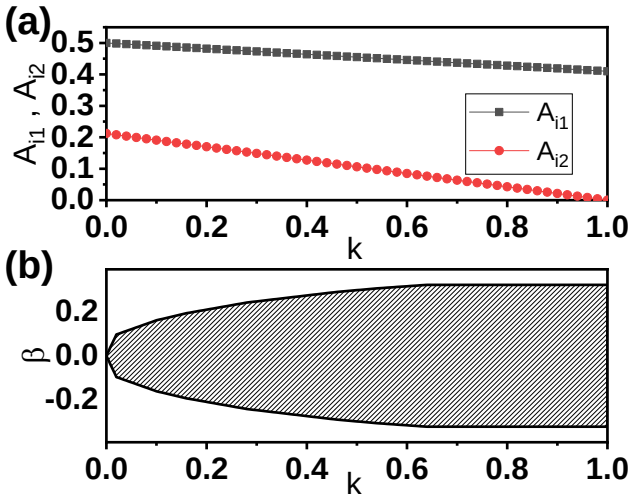

Figure 4.3: (a) The in-phase fundamental (A_{i1}) and second harmonic (A_{i2}) components of the current waveforms versus k (b) The allowed values of β (which indicate the magnitude of quadrature component) versus k

However, this manipulation changes the phase of the fundamental and second harmonic frequencies. The phases of the fundamental (θ_1) and second harmonic (θ_2) components of the current are

$$\theta_1 = \tan^{-1}\left(\frac{8\beta}{3\pi}\right) \tag{4.15}$$

$$\theta_2 = \tan^{-1}\left(\frac{\beta\left\{\frac{3\pi}{4} - \frac{4k}{3\pi}\right\}}{(1-k)}\right) = \tan^{-1}\left(\frac{\beta\delta_{Ii}}{\frac{4}{3\pi} - \frac{3\pi}{4}(1-\delta_{Ii})}\right) \tag{4.16}$$

θ_1 varies between -16^0 to 16^0 whereas, θ_2 varies from 0 in class B/J to 90^0 in class F^{-1}.

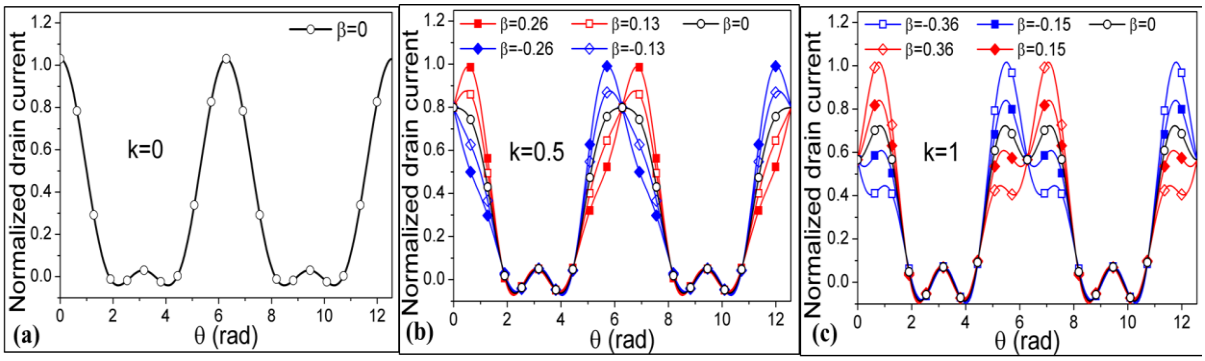

Figure 4.4: The current waveforms in the proposed continuum in comparison with Classes J and CCF^{-1}. (a) Class B/J continuum (k=0) (b) Proposed mode at k=0.5 (c) CCF^{-1} (k=1)

4.2.2. Voltage waveforms

We propose drain voltage waveforms with a phase of ±π/2 at the second harmonic frequency so that the load at the second harmonic is purely reactive for all values of k in the following equation (4.17) as:

$$V_{DS} = \mathrm{V_k} + (V_{dc} - \mathrm{V_k})\left\{1 - \cos\left(\theta - \frac{\theta_2}{2}\right) - \alpha\sin\left(\theta - \frac{\theta_2}{2}\right) + \frac{\alpha\sin(2\theta - \theta_2)}{2}\right\} \tag{4.17}$$

$$= V_{dc} - (V_{dc} - V_k)\delta_v\cos\left(\theta - \frac{\theta_2}{2} - \Psi_{pf(J)}\right) + \frac{\alpha}{2}(V_{dc} - V_k)\sin(2\theta - \theta_2)$$

Where, $\alpha \in [-1,1]$ is proportional to the magnitude of the second harmonic of the voltage, $\delta_v = \sqrt{1+\alpha^2}$ is the voltage gain and $\Psi_{\mathrm{pf(J)}} = \tan^{-1}(\alpha)$ is the phase difference between the current and voltage waveforms in Class J retaining its usual meaning [4.1].

This voltage waveform is obtained by shifting the fundamental and second harmonic components of the voltage waveform of class B/J continuum by $\theta_2/2$ and θ_2 respectively,

giving an overall phase difference between the fundamental components of the current and voltage waveforms Ψ_{pf} as:

$$\Psi_{\text{pf}} = \Psi_{pf(J)} - \theta_1 + \frac{\theta_2}{2} = \underbrace{\tan^{-1}(\alpha)}_{\Psi_{pf(J)}} + \frac{1}{2}\underbrace{\tan^{-1}\left(\frac{\beta}{(1-k)}\left\{\frac{3\pi}{4} - \frac{4k}{3\pi}\right\}\right)}_{\theta_2} - \theta_1 \qquad (4.18)$$

As k is increased from 0 to 1, from (4.16), θ_2 increases from 0 to $\pi/2$ if β is positive and decreases from 0 to $-\pi/2$ if β is negative. Hence by choosing α and β with opposite signs, from (4.18), it can be observed that θ_2 negates the effect of α in $\Psi_{pf(J)}$. On the other hand, choosing α and β with opposite signs results in an increase in the phase difference due to an increase in θ_1. Since the variation of θ_1, which is between -16^0 and 16^0, is considerably smaller than θ_2, which can attain phases between -90^0 and 90^0, Ψ_{pf} can be lower than $\Psi_{pf(J)}$ benefitting the efficiency and output power . The voltage and current waveforms in class J and our proposed class are plotted in Figure **4.5** for k=0.52, to demonstrate the reduction in phase difference. Ψ_{PF} is lower than Ψ_{J} as δ_{Ii} decreases (ie., k increases) provided α and β have opposite signs [4.6].

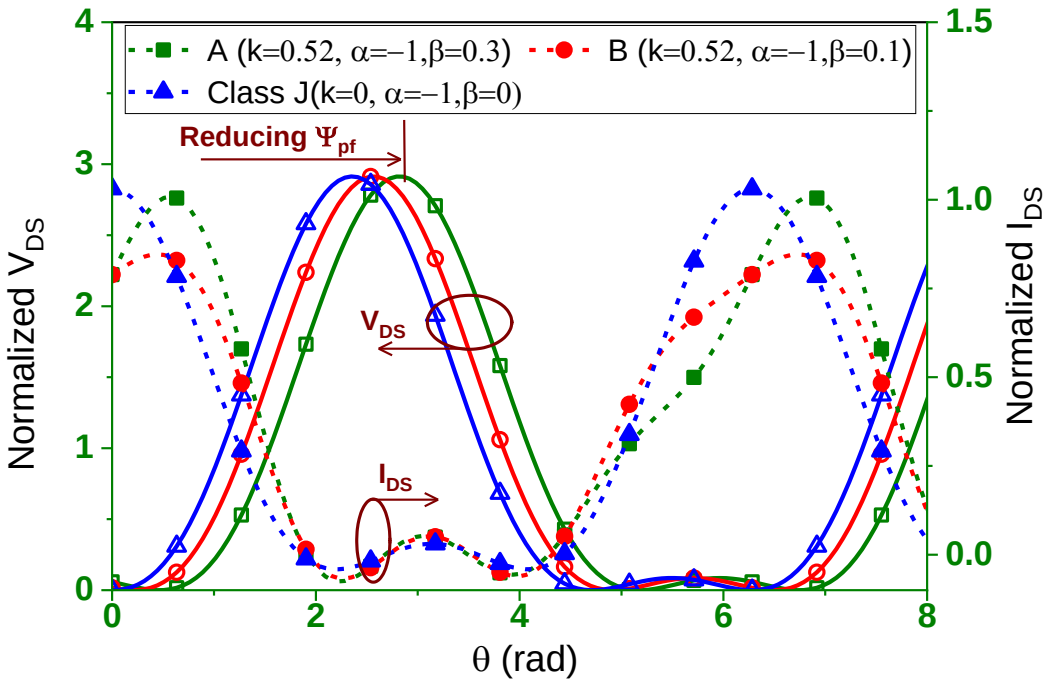

Figure 4.5: Normalized voltage and current waveforms for k=0.5. Voltage and current waveforms obtained by setting V_{DC}=1, I_m=1, and V_k=0.

4.2.3. Output power and efficiency

The output power (P_{out}) and efficiency (η_{out}) are expressed in terms of the output power ($P_{out|B}$) and efficiency ($\eta_{out|B}$) of class B respectively as:

$$P_{out} = P_{out|B}\delta_v\delta_{Ii}\sqrt{1+\frac{64\beta^2}{9\pi^2}}\cos(\Psi_{pf}) = P_{out|B}G_{VI}\cos(\Psi_{pf}) \quad (4.19)$$

$$\eta_{out} = \eta_{out|B}\delta_v\delta_{Ii}\sqrt{1+\frac{64\beta^2}{9\pi^2}}\cos(\Psi_{pf}) = \eta_{out|B}G_{VI}\cos(\Psi_{pf}) \quad (4.20)$$

Where, G_{VI} is defined as the gain in the product of the current and voltage over class B, calculated as

$$G_{VI} = \left(1-\frac{16k}{9\pi^2}\right)\sqrt{\{1+\alpha^2\}\left\{1+\frac{64\beta^2}{9\pi^2}\right\}} = \delta_v\delta_{Ii}\sqrt{1+64\beta^2/9\pi^2} \quad (4.21)$$

The power factor ($\cos(\Psi_{pf})$), G_{VI} and the efficiency with k are plotted in Figure **4.6**. The power factor increases due to a reduction of Ψ_{pf} as k increases, whereas, G_{VI} reduces with k due to the reduction of A_{i1} with k. The increase in power factor compensates for the reduction in G_{VI} resulting in an efficiency and output power higher than in class B/J; waveforms 'A' and 'B' marked in Figure **4.5** achieve 2% and 9% higher efficiency than class J. Not only the efficiency but also the output power of the proposed mode is higher than class J, in proportion to the efficiency as revealed by (4.19). On the other hand, adjustment of the loadline to increase efficiency results in a trade-off with output power, which is not the case in this work. In the extreme case of k=1 and $|\alpha|$=1, $|\theta_2|$ is $\pi/2$ which corresponds to continuous class F^{-1} (CCF^{-1}), $|\theta_2|$ is $\pi/2$, causing the minimum phase difference between the fundamental components of the

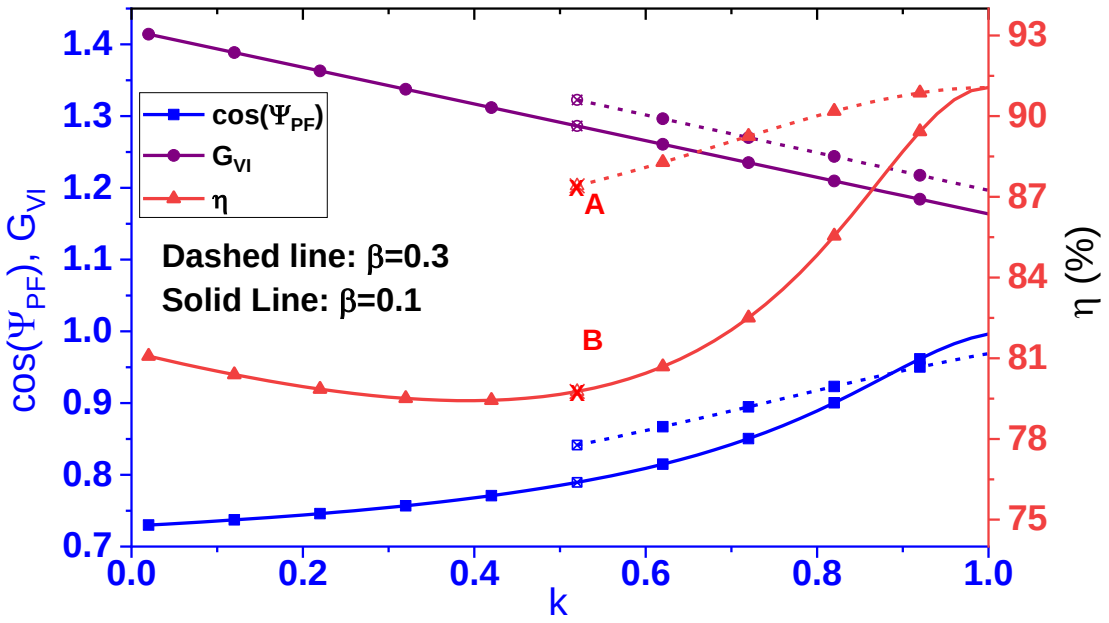

Figure 4.6: (b) Power factor (cos (Ψ_{pf})), Current-Voltage gain (G_{VI}), and efficiency as k increased from 0 to 1 for α=-1, and β=0.3 and 0.1,

voltage and current, resulting in an efficiency of 91% [3]. θ_1, θ_2 and G_{VI} increase with an increase in β as seen from (4.15), (4.16), and (4.21) respectively, resulting in higher efficiencies in Figure **4.6**. The increase in θ_1 results in a lower power factor for β=0.3 than β=0.1 as k approaches 1.

The maximum allowable value of β (β_{max}) for a given k and the contours of efficiency (η) with α and k when β= β_{max} are plotted in Figure **4.7**. As k increases from 0 to 1, the in-phase components (A_{i1} and A_{i2}) decrease and hence β_{max} increases. Reducing |α| while maintaining constant k and β, reduces efficiency and output power because the magnitude of the fundamental component of the voltage decreases. Hence, the minimum |α| required to achieve η>78% decreases with increase in k via a reduction of the fundamental component of current ie., Not all values of α (ie., δ_v) in (4.17) but only a subset of δ_v will result in an improvement of efficiency depending on the δ_{Ii}; decreasing δ_{Ii} (ie., increasing k) requires higher values of δ_v to compensate for the current loss. The efficiency can be maintained within 2% over a range of waveforms defined by k, α, and β. The waveforms for k>0, except for CCF^{-1}, have not been previously described. Because these waveforms are contiguous with class J and CCF^{-1} with both these classes at extremities, the linearity of these modes lies in between these two classes.

In (4.19) and (4.20), $\sqrt{1+64\beta^2/9\pi^2} \approx 1$ even for the maximum value of β and therefore neither benefits the efficiency nor the output power. On the other hand, $\delta_v\delta_{Ii}\cos(\Psi_{pf})$ can be greater than 1, resulting in higher output power and efficiency than class B/J [4.6], as can be seen in Figures **4.6** and **4.7**. This presents an interesting possibility; sacrificing the fundamental

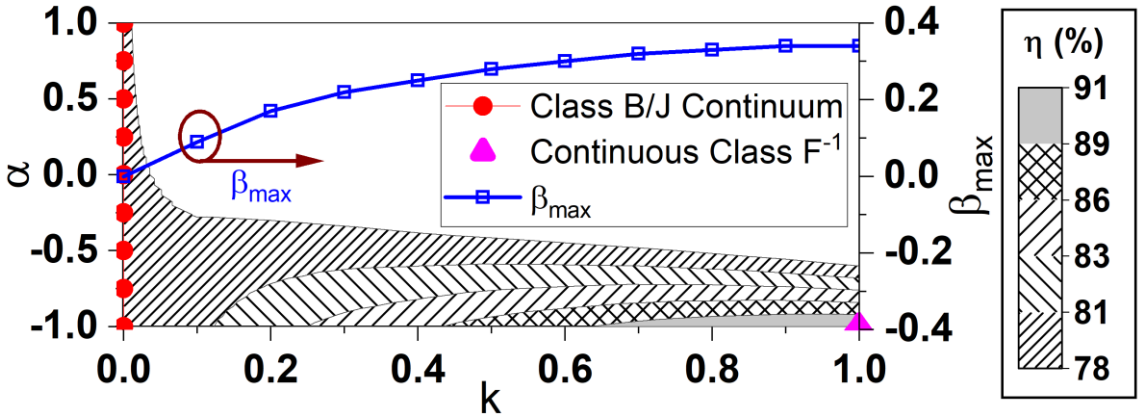

Figure 4.7: The maximum allowable value of β vs k. The contours of efficiency with α and k for β= β_{max} calculated from (4.20). V_{DC}=1V, I_m=1A, and V_k=0V were used for this simulation. Shaded regions demonstrate design flexibility in comparison to continuous class F^{-1} and class B/J.

component of the current ($\delta_{Ii} < 1$) for a lower phase shift ($\Psi_{pf} < \Psi_J$) and reaping the benefit from voltage gain ($\delta_v > 1$) due to second harmonic manipulation of the voltage.

The impedances at fundamental ($Z_{1,int}$) and second harmonic ($Z_{2,int}$) frequencies, required to maintain the waveforms are calculated from (4.17) and (4.8), are

$$Z_{1,int} = R_{opt}\left(\frac{\delta_v}{\delta_{Ii}\sqrt{1+64\beta^2/9\pi^2}}\right)e^{-\mathrm{j}\Psi_{PF}}$$
$$= R_{opt}\left(\delta_v e^{-\mathrm{j}\Psi_J}\right)\left(\frac{e^{j\theta_1}}{\sqrt{1+64\beta^2/9\pi^2}}\right)\left(\frac{e^{j\left(\frac{-\theta_2}{2}\right)}}{\delta_{Ii}}\right) \quad (4.22)$$

$$Z_{2,int} = \frac{i\alpha R_{opt}}{\sqrt{\left\{\frac{8(1-k)}{3\pi}\right\}^2 + \{2\beta - (32\beta k)/(9\pi^2)\}^2}}$$
$$= \frac{j\alpha R_{opt}}{2\sqrt{4\left(\frac{2}{3\pi} - \frac{3\pi}{8}(1-\delta_{Ii})\right)^2 + \delta_{Ii}^2\beta^2}} \quad (4.23)$$

These calculated impedances are plotted in Figure **4.8** for k=0, 0.5, and 1 using (4.22) and (4.23). For each value of k, the values of α and β are varied so that the impedances achieve higher efficiency than in a un-manipulated second harmonic class B. Increasing δ_v (ie., the

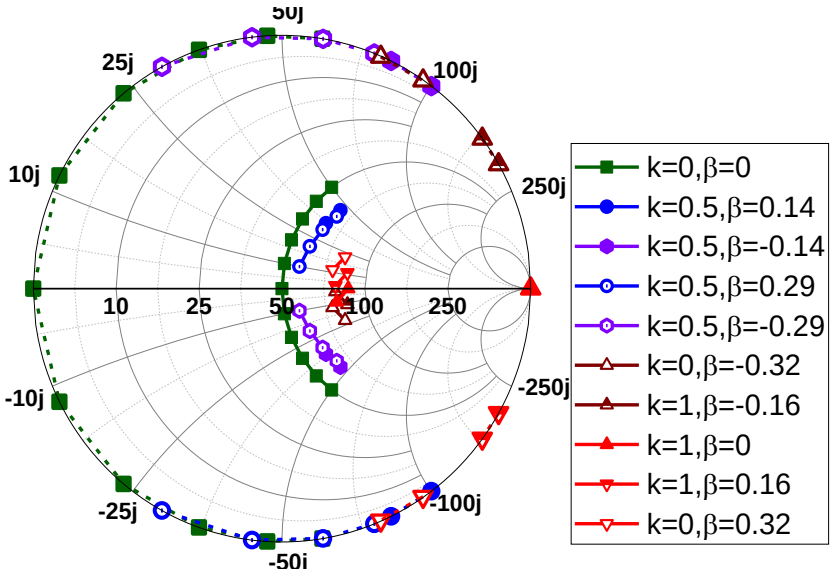

Figure 4.8: Theoretical fundamental (Z1) and second harmonic impedances (Z2) for k=0, k=0.5, and k=1 and varying α and β. All these impedances achieve efficiencies between 91% and 78.5%

magnitude of α) not only increases the magnitude of $Z_{1,int}$ but also its phase, leading to an increase in the reactive component of $Z_{1,int}$. Increasing the magnitude of β results in very small variation in the magnitude of $Z_{1,int}$, as $\sqrt{1+64\beta^2/9\pi^2}$ is 1.04 even for the maximum value of β but it increases the reactive component of $Z_{1,int}$. It is seen that reducing |α| and increasing |β| moves the second harmonic impedance towards a short circuit. The variation of the impedances with α and β is similar to class B/J continuum [4.1] and CCF^{-1} [4.3][4.5] respectively, from where they are derived.

Decreasing δ_{Ii} results in an increase in the magnitude of the $Z_{1,int}$, as can be inferred from (4.22), and in the reduction of Ψ_{pf}, as can be inferred from (4.18). As a result, the design space shows the shape of an increasing resistive component and decreasing reactive component of $Z_{1,int}$. This increment of the resistive component implies an implicit tradeoff between maximum efficiency, and linearity if no other considerations are taken into account in the choice of DC bias of the amplifier. Because the range of values of α for which efficiency is greater than in class B decrease with increase in k (decrease in δ_{ii}), a purely resistive impedance at the fundamental frequency cannot be attained for k=0.5 in Figure **4.8**. This shows that the proposed formulation differs from the effects of a simple increment in the load line resistance. Similarly, decreasing δ_{Ii} reduces the denominator of $Z_{2,int}$ resulting in an increase in its magnitude. The higher value of $Z_{2,int}$ leads to a reduction of the flow of the second harmonic current. Moreover, for a given impedance at the fundamental frequency, there exist two different impedances at the second harmonic; each achieving different efficiency, revealing an aspect (amongst several) of flexibility in the design.

The continuum of waveforms for k=1 as α reduces, results in a design space that is contiguous with CCF^{-1}, same as the extended CCF-1[4.7]. However, the proposed design space differs from the formulation of extended CCF^{-1} in that the increase in design space is achieved whilst reducing the required reactive component at the fundamental frequency. This can be observed from the calculated fundamental and second harmonic impedances at k=1 plotted in Figure **4.8**. Interestingly, a combination of resistive load ($\sqrt{2}$ times the impedance at class B) at the fundamental frequency with larger inductive or capacitive second harmonic load is also achieved for k=1, |β|=0.16 and α=0.8. This load setting is referred to as "saturated PA" that has demonstrated a class J amplifier with the peak efficiency beyond 78% [4.8].

The theoretical maximum efficiency contours for a given fundamental impedance are plotted in Figure **4.9**. Efficiencies for all possible values of k, α, and β are first calculated and the

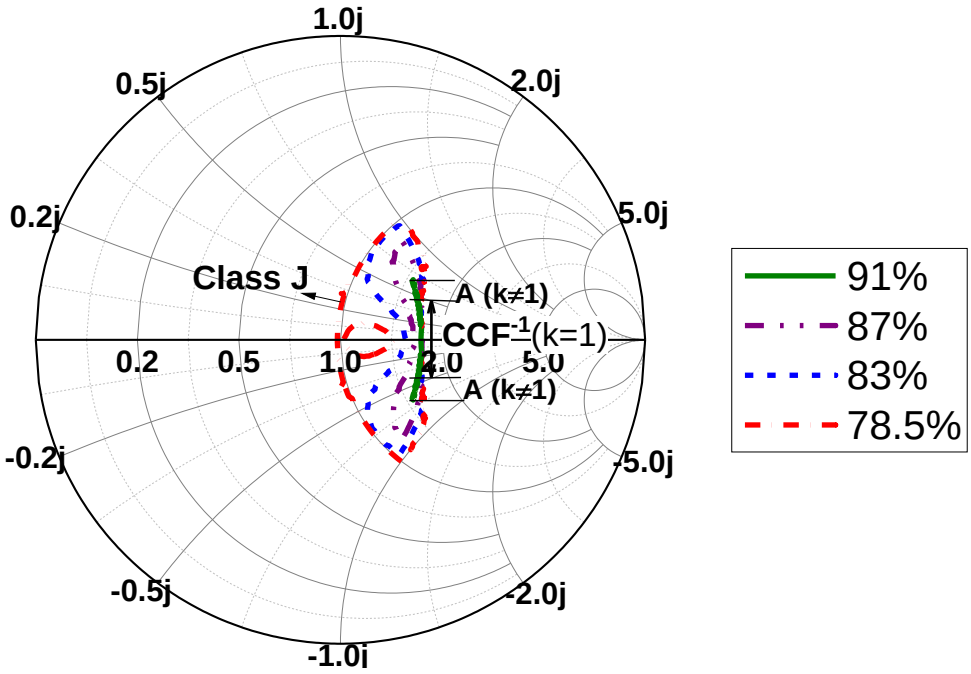

Figure 4.9: Contour plot of the maximum efficiency for k, α and β in (a)

resultant used to generate the contours. The extended 91% contour (marked by A) reveals that the efficiency of class F^{-1} can also be achieved through a combination of k ($\neq 1$), α, and β, and not just for k=1, as in class CCF^{-1}, further providing an additional aspect of flexibility of design.

4.3. On the realizability of the proposed waveforms

The current waveforms proposed for this mode require the partial removal of the in-phase component of the second harmonic component, as can be seen from (4.7) and (4.6), whereas the complete elimination of the second harmonic frequency is the starting point for class F^{-1} [4.3]. Some ways of achieving this are [4.2]:

1) by injecting harmonics by external circuitry (such as by the use of a varactor diode) and/or
2) utilizing the harmonics arising due to the non-linearity of intrinsic capacitances or using the knee region of the transistor ie., the voltage to venture into the knee region.

The second way is readily available, especially as GaN transistors have a fairly deep knee voltage. The drain current of a GaN device, considering the N-model of the knee profile given equation (2.12), is related to the drain voltage as [4.9]

$$i_{ds}(\theta) = A(\theta)\left(1 - \left(1 - \frac{V_{DS}(\theta)}{V_{dc}}\right)^{N}\right) \tag{4.24}$$

Where, $A(\theta)$ denotes the baseline current the device would generate without the knee [4.9] ie., $A(\theta)$ is equal to $I_{DS(J)}(\theta)$ in equation (4.6) where the knee region is not considered. Equation (4.6) can be rewritten as

$$i_{ds}(\theta) = A(\theta)\left(1 - \frac{i_2(\theta)}{A(\theta)}\right) \tag{4.25}$$

Where, $\left(2p - \frac{1}{2}\right)\pi < \theta < \left(2p + \frac{1}{2}\right)\pi \ \forall \ p \in Z$. From (4.25), it is evident that the proposed current waveforms can be realizable if $\left(1 - \frac{V_{DS}(\theta)}{V_{dc}}\right)^N = \frac{i_2(\theta)}{A(\theta)}$. This condition is certainly not valid for $\frac{V_{DS}(\theta)}{V_{dc}} \ll 1$ ie., for small input signal at the gate, in which case, $i_{ds}(\theta) \approx I_{ds(J)}(\theta)$. This approximation is universal for all continuum modes which rely on current manipulation including CCF[-1]. However, as the input power increase, the $V_{DS}(\theta)$ ventures into the knee region resulting in a generation of harmonics due to the factor $\left(1 - \frac{V_{DS}(\theta)}{V_{dc}}\right)^N$. Additionally, non-linear capacitances also generate harmonics as the input power increases. These two contribute to the factor $\frac{i_2(\theta)}{A(\theta)}$.

To illustrate the role of knee region and non-linear capacitances in realizing the current and voltage waveforms, we have simulated the following two models for two conditions ($k = 0.7$, $\beta = -0.3$, $\alpha = 0.6$) and ($k = 0.7$, $\beta = 0.3$, $\alpha = -0.6$), and compared them with the formulation which represents our target waveform, irrespective of the device characteristics:

1) **A current generator model of CGH40010 (CG model):** We have pulsed the gate and drain of a vendor model and obtained the intrinsic drain current. The vendor model outputs the intrinsic drain current; thus eliminating the need for de-embedding the extrinsic resistance which is otherwise required [4.10]. The obtained pulsed IV are plotted in Figure **4.10** and a table-based model in ADS is created to read this IV to emulate the current generator of CGH40010. The non-linear g_m and the knee characteristics of a specific device (CGH40010) are captured by this model.
2) **The vendor model of CGH40010**: This model includes the effects of the knee voltage and non-linear capacitances.

We have biased the device model in near class B condition (V_{DSQ} = 28 V and I_{DSQ} = 6 mA) for these simulations. This bias condition is selected for illustration. The waveforms for the actual bias of an amplifier (V_{DSQ} = 28 V and I_{DSQ} = 150 mA) is shown later in this chapter. The intrinsic impedances at fundamental and second harmonic frequencies corresponding to (k =

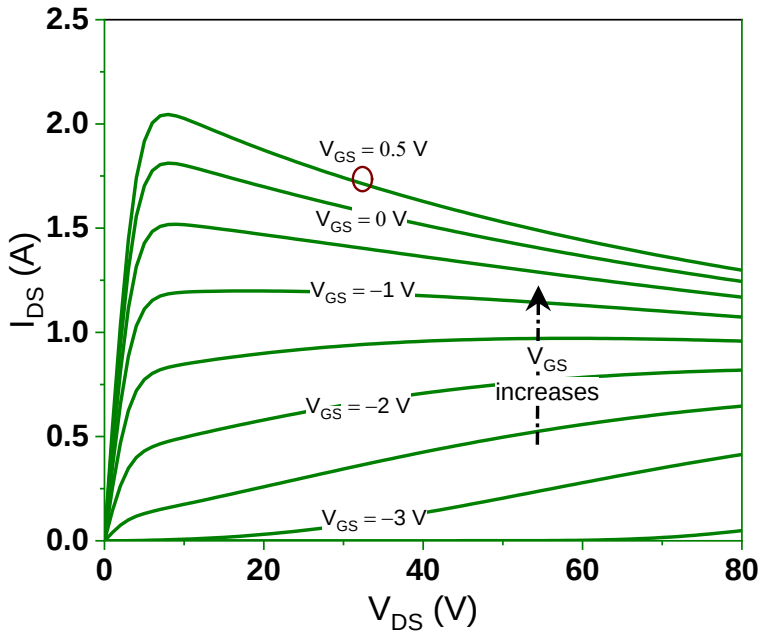

Figure 4.10: The pulsed IV obtained from the vendor model. Pulsed IV is obtained for the pulse width 1.2 μs and pulse period 50 μs with the device biased at V_{DSQ} = 28 V and V_{GSQ} = -3.8 V

0.7, $\beta = -0.3$, $\alpha = 0.6$) and (k = 0.7, $\beta = 0.3$, $\alpha = -0.6$) are calculated from (4.22) and (4.23) and these lie between the design space of class B/J and CCF^{-1}. Using the vendor model, the calculated impedances are embedded to the extrinsic plane by the method explained in section 3.3. The third and higher harmonics are shorted in both cases; in the CG model case, this simply implies placing a short at the intrinsic plane whereas, with the vendor model, an open circuit is presented at the extrinsic plane. This results in the shorting of the higher harmonics at the intrinsic plane because of C_{ds}.

The obtained load cycles of both the models are plotted in Figure **4.11**. The power levels are chosen such that the ratio of the minimum of the intrinsic drain voltage and V_{DC} ie., $\frac{V_{min}}{V_{DC}}$ is same for all the devices. $\frac{V_{min}}{V_{DC}}$ is indicative of the knee incursion in the device.

The current waveforms from both the models are compared with formulation for $\frac{V_{min}}{V_{DC}} = 0.05$ are plotted in Figure **4.12** respectively. The ideal theoretical waveform corresponding to this case is predicted from equations (4.8), (4.17) and (4.8). The current waveforms from the CG model show a sharp transition when compared with the vendor model. This can be due to a difference in the gate-source voltage; in the CG model it is sinusoidal whereas the non-linear C_{gs} in the vendor model introduces harmonics, causing a deviation from the sinusoid [4.11][4.12]. Additionally, the C_{ds} and the extrinsic parasitic elements at the drain terminal act

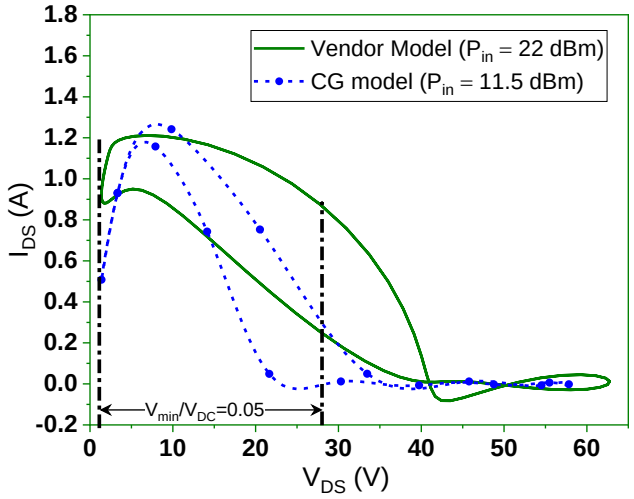

Figure 4.11: Load cycles of vendor model and CG model for the power level is adjusted such that they are similar knee incursion ($\frac{V_{min}}{V_{DC}} = 0.05$).

as a low pass filter. The waveforms from the vendor model are much closer than to theoretical waveforms indicating that the realization of the waveforms requires not just the harmonic from the knee region but also the non-linear capacitances.

Figure **4.13** shows a comparison of the current and voltage waveforms (up to the third harmonic) from the theoretical and vendor model. The results of the simulation show a peaking of the current to the left and right as expected from theory. A good qualitative agreement is seen between the current waveforms and the voltage shows a good match for β=0.3 whereas a slight reduction in the voltage is observed for $\beta = -0.3$.

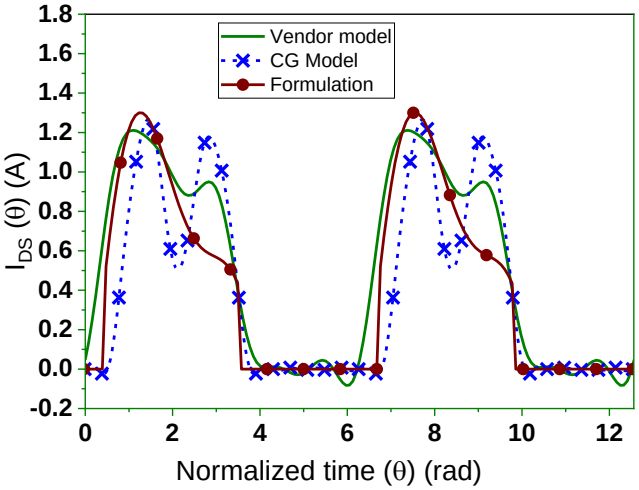

Figure 4.12: A comparison of the current waveforms from the formulation, vendor model and CG model for k = 0.7, $\beta = -0.3$, $\alpha = 0.6$ for $\frac{V_{min}}{V_{DC}} = 0.05$.

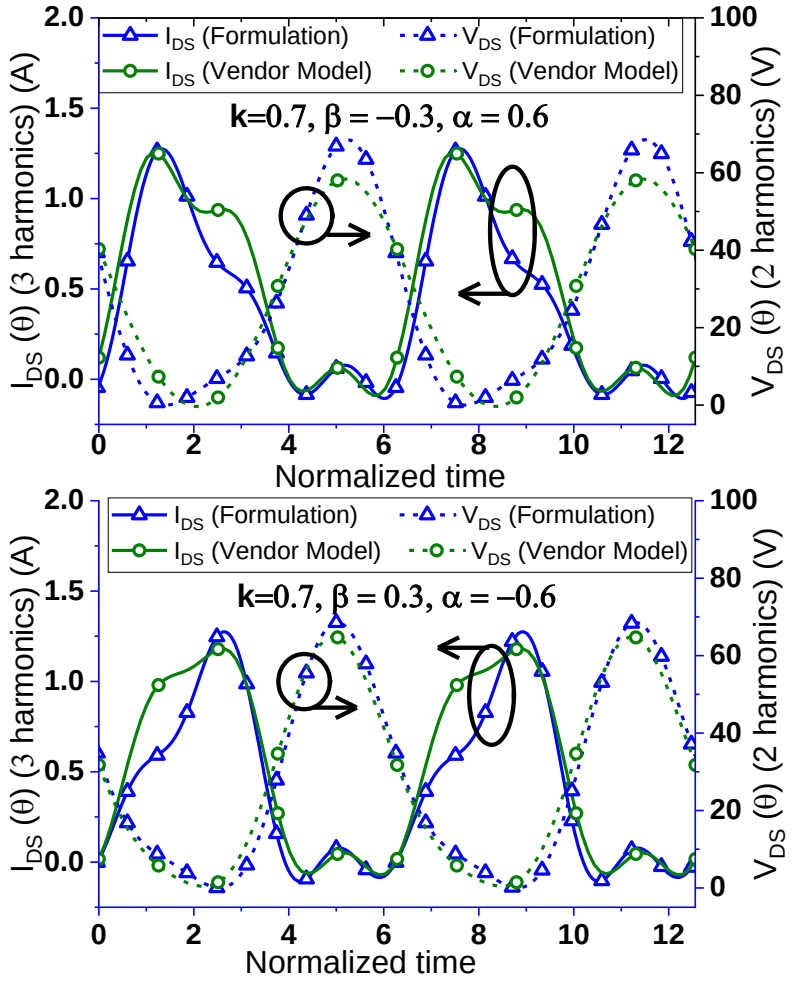

Figure 4.13: A comparison of the voltage and current waveforms (upto third harmonic) from the formulation and the vendor model for (a) k = 0.7, $\beta = -0.3$, $\alpha = 0.6$ and (b) k = 0.7, $\beta = 0.3$, $\alpha = -0.6$.

However, the magnitude and phase of the second harmonic component of the current vary with input power, as illustrated in Figure **3.16**. Hence, using the harmonics generated from the non-linear capacitances and the knee region, an approximation of the current and voltage waveforms in (4.8) and (4.17) can only be realized in a narrow range of input power levels; in the case of the vendor model, this is around power level that corresponds to $\frac{V_{min}}{V_{DC}} \approx 0.05$. The approximate shape of our current characteristics can be derived by extending the analysis of knee characteristic presented for class B in [4.9][4.13] and by considering the effect of non-linear capacitances as in [4.14] [4.15]. Alternatively, we rely on the vendor model to explore the impedance region that lies between class B/J continuum and CCF^{-1} for the amplifier design. We simulate the vendor model for all the impedances in the new design space and select the impedances which benefit the efficiency and output power.

4.4. Implementation and Results

A 10 W GaN HEMT from Cree, CGH40010F, is chosen for this study. The device is biased in deep class AB mode (V_{dsq}=28 V, I_{dsq}=150 mA) for this implementation. The optimal loadline resistance (R_{opt}) is found to be 38.1 Ω.

4.4.1. Choosing the design impedances

The impedances which result in improvement in efficiency and output power as revealed by equations (4.20) and (4.19) are obtained by presenting impedances from the design space to the vendor model. The theoretical intrinsic impedances are calculated from (4.22) and (4.23) for all values of (α, β, k). The corresponding extrinsic impedances are calculated using the approximated drain parasitic network of the power device, as discussed in section 3.3. The device is simulated for all these extrinsic impedances and the source impedance is set to 2.3-j*4 (an optimal impedance found from the source pull simulation for class B condition). The contours of the obtained simulated peak PAE and the maximum output power are plotted over the intrinsic impedances in Figure **4.14**.

The contours reveal a region of impedances of highest efficiency and output power. These impedances do not correspond to either of the established classes, class J and CCF^{-1}. Since this

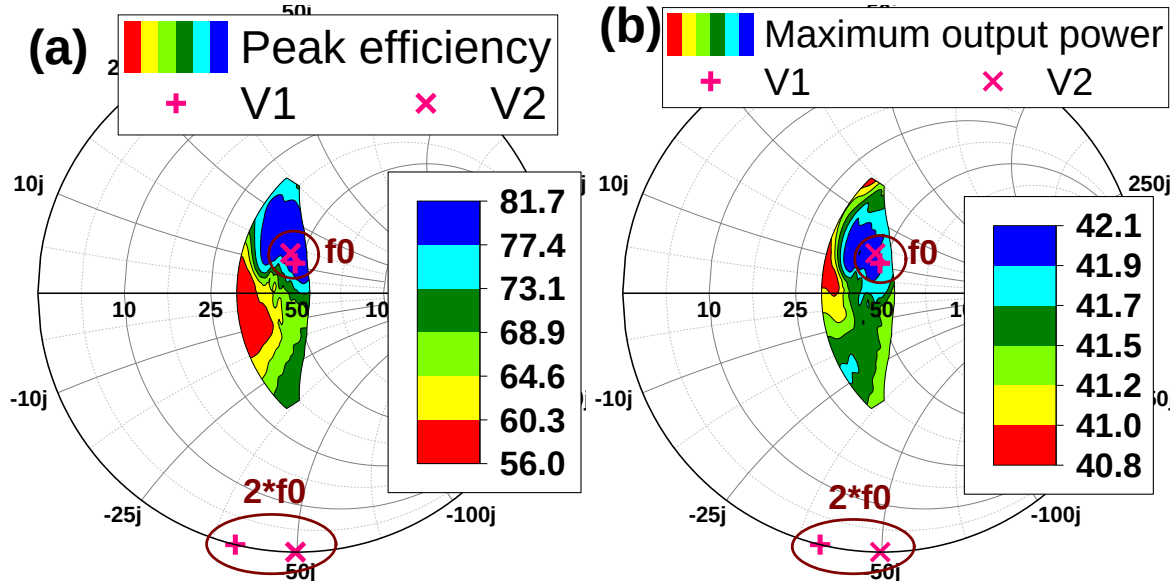

Figure 4.14: Simulated PAE and output power over the proposed design space. (a) The contours of PAE overlaid on the intrinsic design space (b) The contours of output power overlaid on the intrinsic design space. The source impedance is set to 2.3-j*4 obtained from the source pull simulation of the vendor model. The selected impedances for the amplifier design which corresponds to (α,β,k)= (-0.6, 0.3, 0.7) and (-0.5,0.1,0.6) are marked in both figure as V1and V2 respectively.

region lies in between these two classes, the linearity also lies between these two classes. Additionally, placing inductive loads at the fundamental frequency results in higher efficiency than capacitive loads. This is because of the non-linear feedback capacitance, as we have shown for the class BJ continuum in [4.16]. The drain voltage across the feedback capacitance due to inductive loading results in the current from the feedback capacitor to be added to the intrinsic drain current from the intrinsic current generator, leading to additional output power and efficiency over capacitive loading. From the higher efficiency and output power region, waveform parameters corresponding to the (α,β,k)=(-0.6, 0.3, 0.7)[4.6] and (-0.5,0.1,0.6), referred to as V1 and V2 respectively in Figures **4.14** (a) and (b), are chosen for implementation.

4.4.2. Matching network design

An output matching network is designed at the centre frequency (f0) of 2.6 GHz in three segments shown in Figure **4.15**.

(1) The second harmonic frequency (Ss),

(2) fundamental frequency (Sf), and

(3) an impedance transformer (IT).

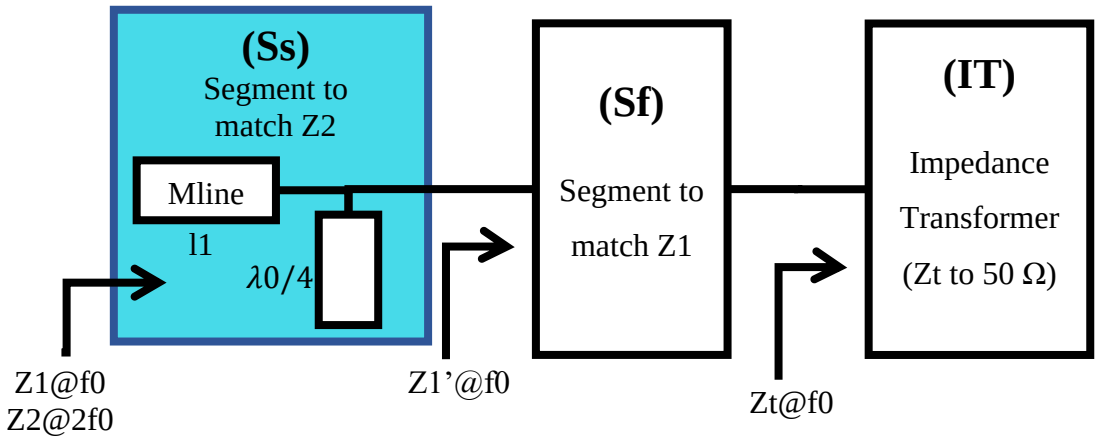

Figure 4.15: The block diagram of the matching network consisting of a segment to match the impedance at the second harmonic frequency (Ss), a segment to match the impedance at the fundamental frequency (Sf), and an impedance transformer (IT).

The segment Ss has an open stub of a quarter wavelength, presenting a short at the second harmonic. As a result, succeeding segments, Sf and IT, do not affect the impedance at the second harmonic frequency. The length of the microstrip line (l1) in this segment is chosen to match Z2 at 2*f0. The section Sf matches the impedance Z1' to Zt. Z1' is such that the overall

matching network presents Z1 at the frequency f0 to the transistor. Zt is chosen to be closer to $\sqrt{50 * real(Z1)}$ resulting in a lower change in impedance with frequency than when matched directly to 50 ohms. Additionally, Zt can be varied between $real(Z1)$ and 50 ohms, so that the width of the matching lines (Wline and Wstub) of this segment lie within the specifications of the foundry. An impedance transformer is used to match Zt to 50 ohms [4.17].

To account for the non-linear nature of the intrinsic capacitances, the second harmonic impedance is obtained from load-pull simulations at the second harmonic frequency using the vendor model of the device, while placing the calculated fundamental impedance, shown in Figure **4.14**, at the load [4.6].

The obtained load impedances at fundamental and second harmonic frequencies corresponding to version 1 (V1(k=0.7, α=-0.6 and β=0.3) [4.6]) are plotted in Figure **4.16** (a). The photograph of the designed amplifier V1 is shown in Figure **4.16** (b). Sf is realized using an architecture with two open stubs. IT is realized using 3 order Chebyshev bandpass filter. The width and length of the microstrip lines of this filter are obtained directly from the design tool in ADS. It matches 50 ohms at a load of 35 ohms over the frequency range 2 GHz – 3 GHz. The input matching networks use a stepped impedance topology. The source impedance at the fundamental frequency from source pull simulation is obtained as 4.9-j*1.8. The input and output matching networks are realized on a 0.762 mm thick R4350B substrate. The realized impedances of the designed output matching network V1 are characterized using a VNA(ZVA-

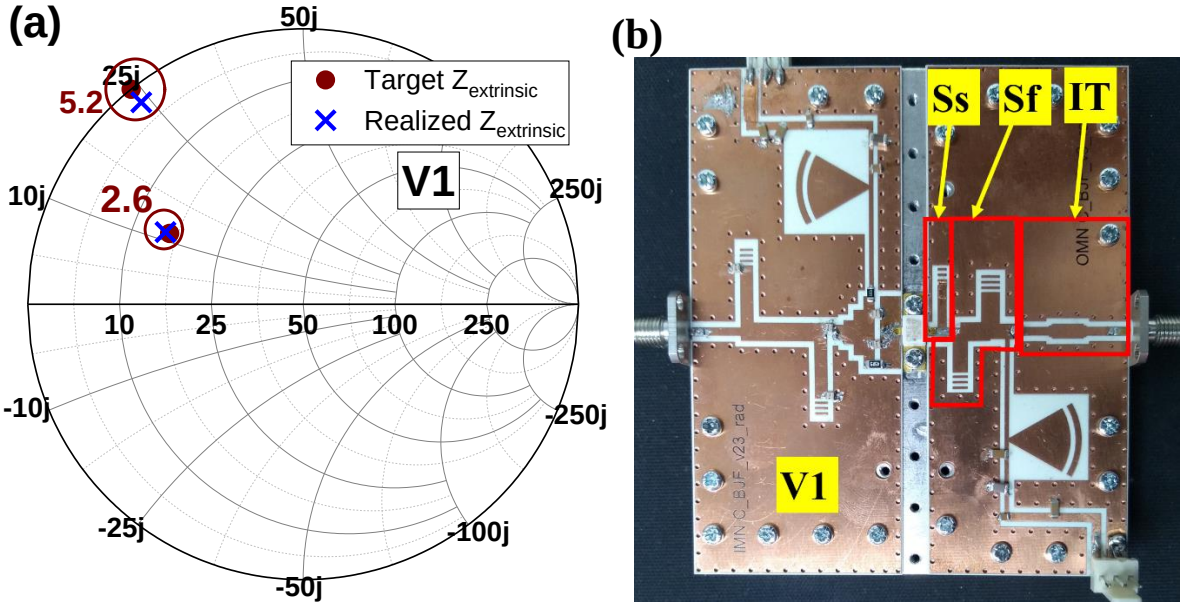

Figure 4.16: (a) Theoretical and the realized fundamental (Z1) and second harmonic impedances (Z2) for version 1 (k=0.7, α=-0.6 and β=0.3). (b) Photograph of the designed amplifier V1

24). The measured impedances at 2.6 GHz and 5.2 GHz are compared with the target impedances in Figure **4.16** (a) which reveal a close agreement; the difference between the target and realized impedances at fundamental and second harmonic impedances is 3.6 % and 7.9 % respectively.

The measured impedances over the frequency range 2.3 GHz-2.8 GHz and the corresponding second harmonic frequency 4.6 GHz-5.6 GHz are translated to the intrinsic plane and are plotted in Figure **4.17**. Even though the matching network is designed at a point frequency f0, a large range of available impedances over broad frequencies are found to lie in the high-efficiency region of Class BJF^{-1}, resulting in bandwidths of 600 MHz, despite being designed narrowband. This further attests to the ease of design of this class of amplifier.

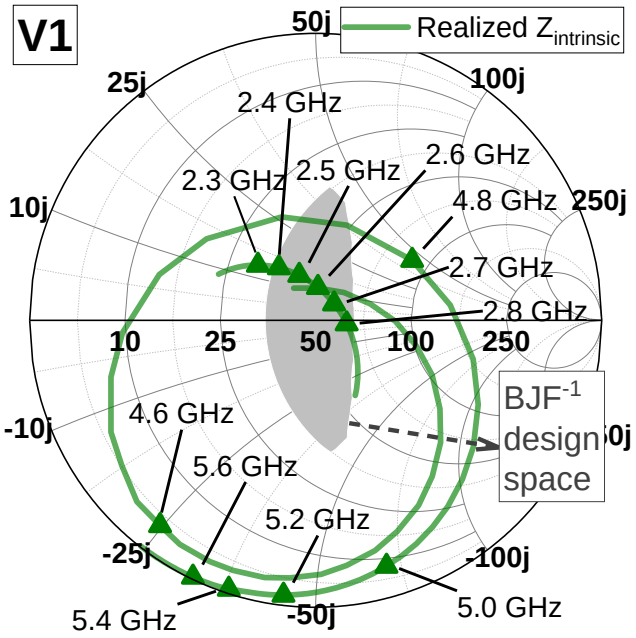

Figure 4.17: The impedance achieved by the matching network at the intrinsic plane. The impedances that overlap with the Class BJF^{-1} design space are highlighted.

The intrinsic voltage and current waveforms obtained from harmonic balance simulation and from the theoretical calculation are plotted in Figure **4.18**. The peaking of current to the right and the increase of the maximum of normalized voltage $V_{DS,}$ in excess of a factor of 2, reveal the manipulation of the second harmonic of both the voltage and current waveforms, conforming with theory.

The target impedances for V2 (k=0.6, α=-0.5 and β=0.1) are plotted in Figure **4.19** (a). The fabricated amplifier is shown in Figure **4.19** (b). Sf is realized using two stubs (one open stub

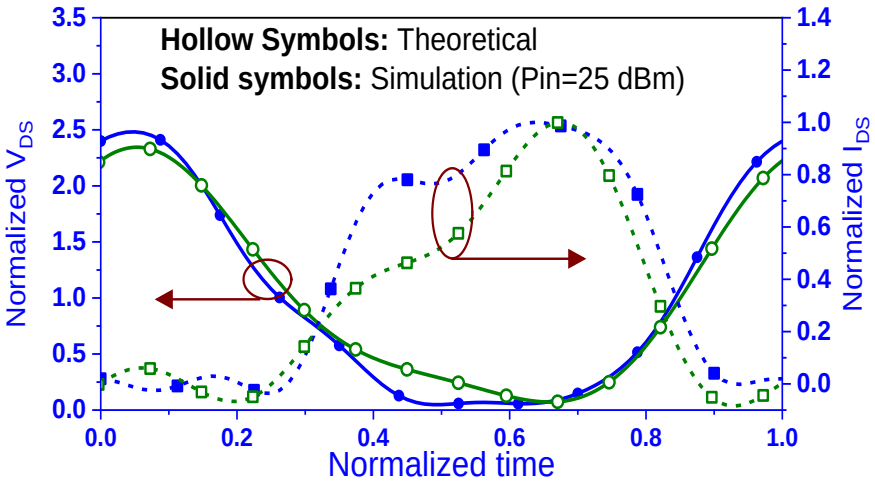

Figure 4.18: The intrinsic voltage and current waveforms from simulation and the theoretical waveforms. The voltage and current are normalized to V_{DC} and I_m respectively. V_{DC}=28 V, V_k=2 V, and R_{opt}=38.1 Ω are used in the calculation of I_{DS}, and V_{DS}.

and one short stub) architecture. In this case, the short stub is used for biasing. The IT is the same as the one used for V1.

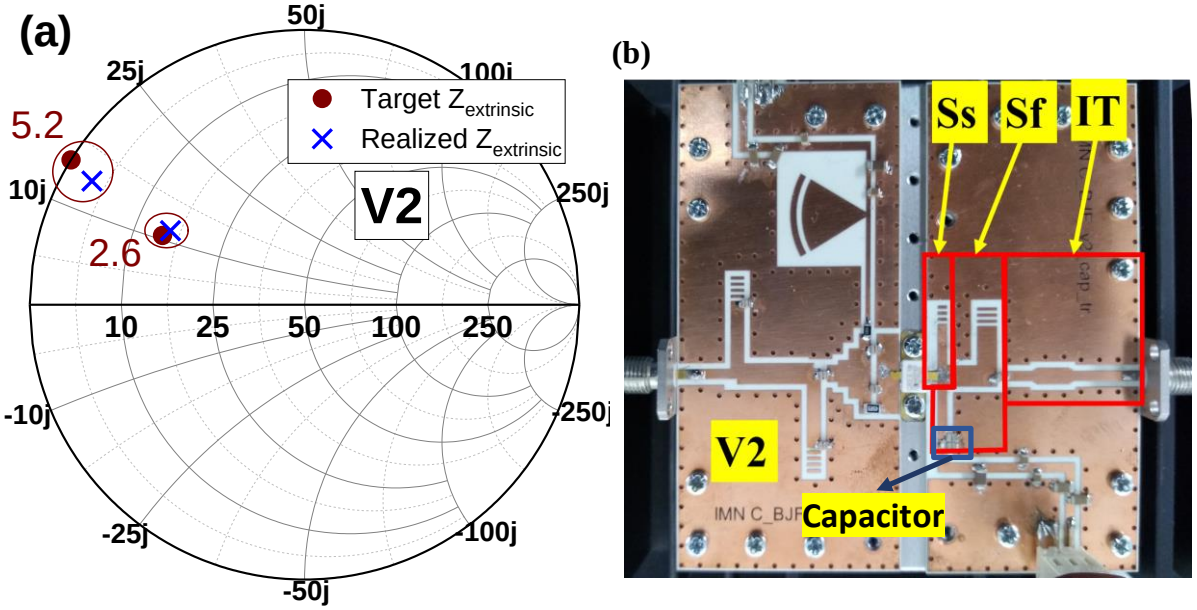

Figure 4.19: (a) Theoretical and the realized fundamental (Z1) and second harmonic impedances (Z2) for version 2 (k=0.6, α=-0.5 and β=0.1). (b) Photograph of the designed V2

The measured impedances at 2.6 GHz and 5.2 GHz of the output matching network V2 are compared with the target impedances in Figure **4.19** (a). A close agreement between these target and measurement impedances can be seen, however, the difference between them is larger than in amplifier V1; the difference between the target and realized impedances at fundamental and second harmonic impedances is 8.2 % and 21.5 % respectively. A possible reason for this discrepancy is that the capacitor (highlighted in Figure **4.19** (b).) has a finite

width (1.5 mm) whereas it has been assumed to make contact at a single point in simulation which is an approximate representation of the actual capacitor contact. This capacitor is an integral part of the matching network and may have led to this discrepancy.

The measured impedances with the frequency of the output matching network is plotted in Figure **4.20**. In this case, impedances over the frequency range of 900 MHz are found to lie in the high-efficiency region of Class BJF^{-1}, which is 300 MHz higher than V1.

In both cases, there is a good match between the target and realized impedances at f0. The ratios $\left|\frac{\Im m(Z_{1,int})}{\Im m(Z_{2,int})}\right|$ and $\left|\frac{\Im m\left(\frac{1}{Z_{1,int}}\right)}{\Im m\left(\frac{1}{Z_{2,int}}\right)}\right|$ are 1.15π and 2π, neither equal to 3π/8 as in class B/J continuum and continuous class F^{-1}; showing a paradigm shift from the conventional continuum. A strong resistive component is observed in the trajectory of the second harmonic impedance as it drops from the ideal reactance, but this can be addressed via resistive second harmonic impedances [4.4].

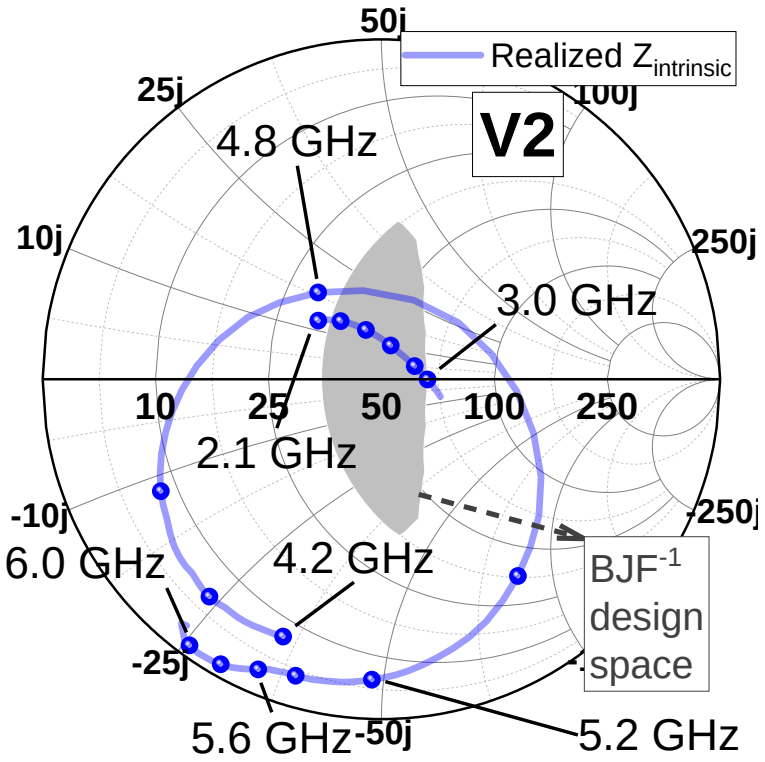

Figure 4.20: The impedance achieved by the matching network (V2) at the intrinsic plane. The impedances that overlap with the Class BJF^{-1} design space are highlighted.

Even though the same source matching network design circuit is used, the measured source matching network of V1 and V2 have demonstrated impedances 5.3-j*1.9 and 6.6-j*2.6 respectively. This difference between the impedances can be due to the tolerances of the

lumped component used in the matching network. The amplifier is simulated using the measured S-parameters of the input and output matching network and the obtained power gain and the PAE are plotted in Figure **4.21**. The gain of Amplifier V1 (using source match V1 and load match V1) is ~1.4 dB higher than the gain of Amplifier V2 (using source match V2 and load match V2). To understand the reason for a lower gain of amplifier V2, we have replaced the S-parameters of source matching of V2 with S-parameters of V1 in simulation and the obtained gain is the same as V1. This clearly indicates the slight difference between the realized source impedances of V1 and V2 result in the lower gain of amplifier V2. On the other hand, the peak PAE of V2 is lower by ~3% than the peak PAE of V1. This lower PAE is achieved by V2 even if the source matching network of V1 is used, indicating that the PAE is dependent on the load matching network and not on the source matching network.

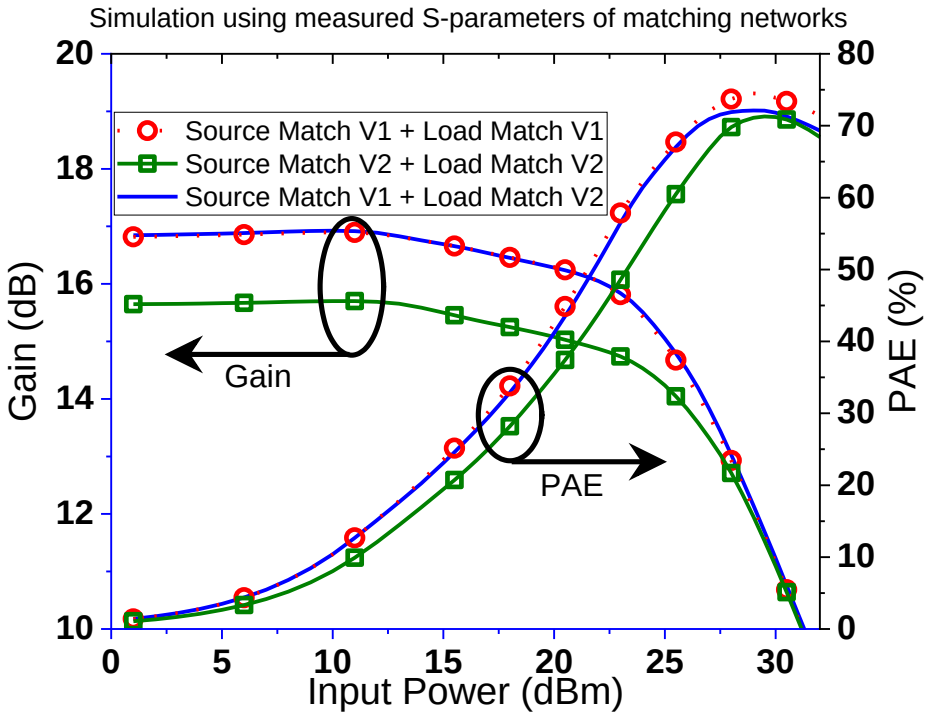

Figure 4.21: The simulated Gain and PAE of amplifiers at 2.6 GHz using the measured S-parameters of matching networks.

4.5. Measured results of the amplifier.

The measured S-parameters of the amplifier V1 and V2 are plotted in Figure **4.22**. The small-signal gain of amplifier V1 between the frequencies 2.2 GHz -2.8 GHz is above 16.3 dB with the maximum gain of 20.2 dB. On the other hand, the small-signal gain of the amplifier V2 over the frequency range 2.1 GHz to 3 GHz is between 15.4 dB and 19.4 dB, slightly lower

than amplifier V1. The directivity (the difference between forward and reverse gain) of both the amplifiers is greater than 42 dB.

The measured transducer power gain, output power and efficiency of both amplifiers at 2.6 GHz and their variation with frequency are plotted in Figure **4.23** (a) and (b) respectively. Amplifier V1 demonstrates a peak PAE of 75.9% and 42.2 dBm output power at 2.6GHz. The response of the amplifier with frequency is plotted in Figure **4.23** (b), revealing a near flat output power, and DE remains above 65% over a 600 MHz 24% fractional bandwidth, despite being designed narrowband at 2.6 GHz. The average DE over the bandwidth (from 2.2 GHz to 2.8 GHz) is 73.4 %. Amplifier V2 demonstrates a peak PAE of 72.4% and 42.2dBm output power at 2.6GHz whereas an average DE over the bandwidth (from 2.1 GHz to 3 GHz) of 72.6 % as shown in Figure **4.23** (b).

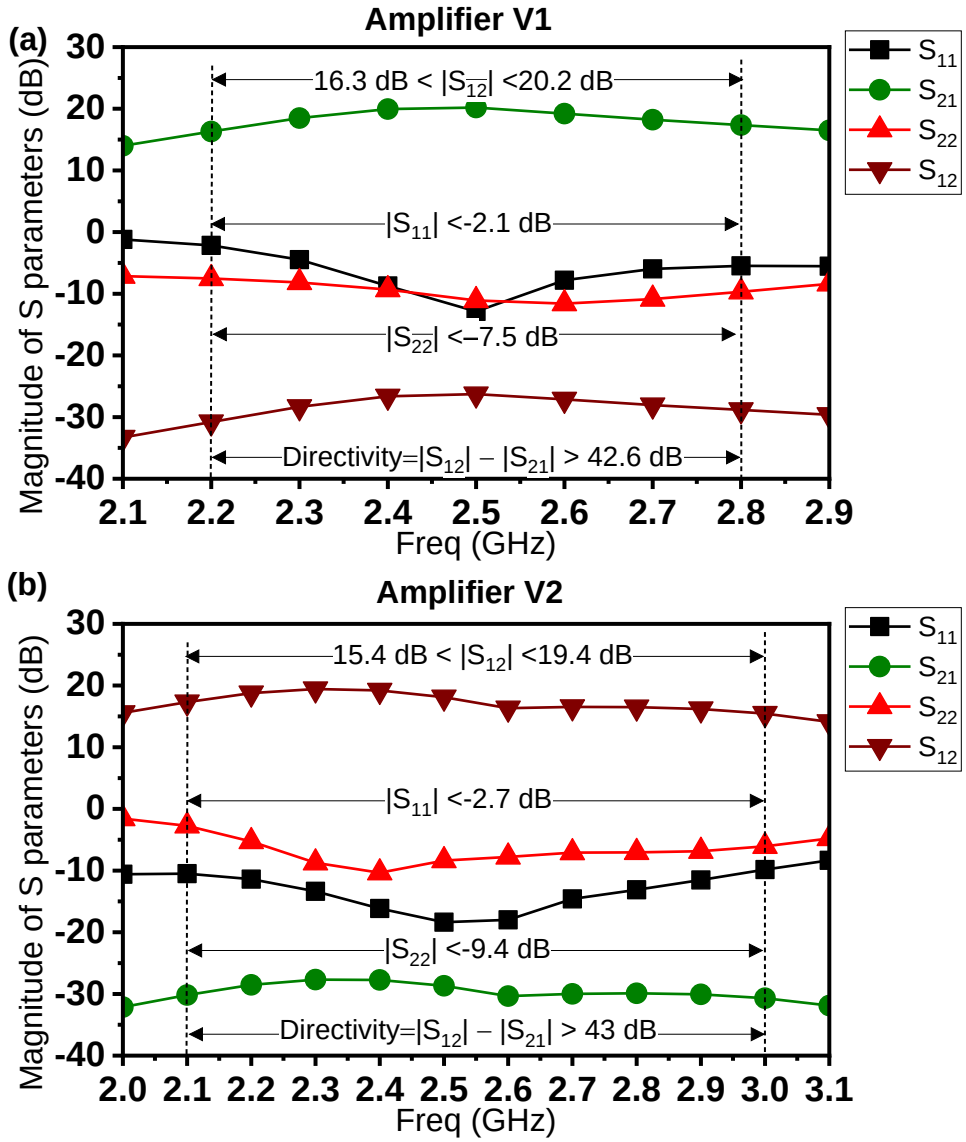

Figure 4.22: The measured S-parameters of the amplifiers (a) V1 and (b) V2

These measured efficiencies of the two amplifiers at 2.6 GHz are within 1% to the simulated results in Figure **4.21**. However, at 2.6 GHz, the gain of amplifier V2 is around ~3.5 dB lower than the gain of V1, whereas the simulation in Figure **4.21** reveals that only ~1.5 dB reduction in the gain can be attributed to the difference between the impedances of source matching network of V1 and V2. A further investigation using load-pull measurements rather than relying on the model is required to understand this gain difference between these two versions. It is to be noted that these amplifiers were designed taking the output power and efficiency into consideration whereas less attention has been paid to the gain. Since the gain is dependent on the source matching network, as revealed in Figure **4.21**, the design of source matching network

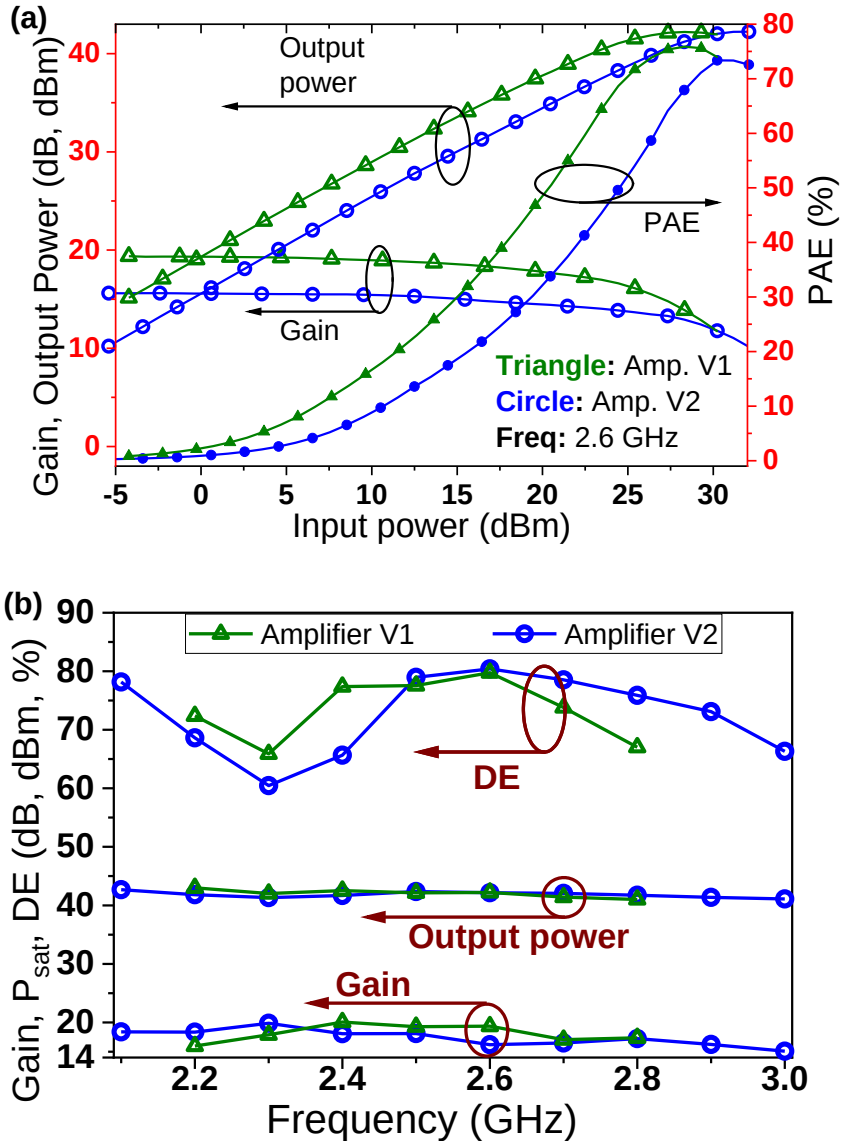

Figure 4.23: The measured Gain, output power, and PAE of the amplifiers at 2.6 GHz. (b) The gain, output power, and DE versus frequency of the designed amplifiers.

needs to be improved to minimize its sensitivity to the tolerances of the lumped components and the gain of the amplifiers needs to be considered early on in the design process.

Both amplifiers show remarkable flat output powers above 41 dBm respectively whereas the gain of V1 and V2 remain above 16 dB and 15 dB respectively over their respective bandwidths. Both amplifiers have lower DE near 2.3 GHz because the intrinsic second harmonic impedance around this frequency has a large real part as opposed to the requirement of class BJF^{-1}. The peak DE of the amplifiers V1 and V2 is 80.4% and 79.7% respectively.

TABLE 4.1: Comparison of performance of the designed amplifiers with the narrowband amplifiers using the same device CGH40010F

Ref.	Class of operation	Frequency (in GHz)	Pout (in dBm)	PAE (in %)	FE (%$\sqrt[4]{GHz}$)
[4.24]	Class J	2.13	39.7	64.5	77.9
[4.16]	Class J	2.6	41.72	72.3	91.8
[4.19]	Class F	3.1	40	82	108.8
[4.25]	class F/F3	2.15	40	73.1	88.5
[4.26]	SHT	2.18	40.02	60.7	73.8
[4.21]	SHT	2	40.4	80.4	95.6
[4.22]	class-F-1	2.655	41	73.9	94.3
[4.27]	class-F-1	2.55	41.4	73	92.2
[4.28]	class-F-1	3.53	40.25	65.5	89.9
[4.29]	class E	3.5	40.2	69.7	95.3
[4.30]	class E	2.5	38.3	74	93.1
[4.18]	THP class EF	2.22	39.5	80	97.7
[4.8]	Saturated PA	2.14	40.6	77.3	93.5
Amp. V1 [4.6]	**BJF-1**	**2.6**	**42.2**	**75.9**	**96.4**
Amp. V2	**BJF-1**	**2.6**	**42.2**	**72.4**	**91.9**

FE=PAE*$\sqrt[4]{Freq.(in\ GHz)}$; SHT = Second harmonic tuned; THP = Third harmonic peaking

The designed amplifiers are compared with other high-efficiency narrowband amplifiers using the same device reported in the literature in Table 4.1. A third harmonic peaking class EF amplifier [4.18] and a class F amplifier [4.19] using the same device have higher FE than our amplifier V1 but achieve output power 2.7 dB and 2.2 dB lower than this work respectively.

TABLE 4.2: Comparison of the designed amplifier with the state-of-the-art amplifiers with comparable bandwidth using CGH40010F reported in the literature.

Ref.	Mode	Bandwidth (GHz, %)	Output power (dBm)	DE (AE) %,(%)	FE
[4.31]	J	2.3-2.7, 16	40-40.8	60-69(63)	78.3
[4.23]	SCM	1.6-2.8, 54.6	40-42.5	67.5-81.9 (76.4)	92.5
[4.32]	SCIM	2.4-3.9, 47.6	39.63-41.4	62-75 (68.1)	90.7
[4.33]	CCF	1.45-2.45, 51.3	40.4-42.3	70-81 (75.9)	89.7
[4.34]	HT	1.8-2.7, 37.6	40.6-41.7	68-77 (73.3)	90
[4.35]	E	1.7-2.4, 34.1	38.9-41	71-87 (76.4)	91.3
Amp. V1 [4.6]	BJF^{-1}	2.2-2.8, 24.0	41-43	65.9-79.7 (73.4)	92.4
Amp. V2	BJF^{-1}	2.1-3, 35.3	41-43	60-80 (72.6)	91.7

AE = Average Efficiency, FE=AE*$\sqrt[4]{Center\ Freq.\ (in\ GHz)}$, HT = harmonic tuned, SCM = series of continuous modes, SCIM=Series of inverse continuous modes

The comparison of our work with the best class J [4.20], class F [4.19], second harmonic tuned [4.21], class F^{-1} [4.22] and saturated PA [4.8] reveal that our work represents a design methodology yielding high output power and efficiency with comparable FE for this device.

For a fair comparison, as FE does not favour broadband amplifiers, we have compared our amplifier with others of comparable bandwidth in Table 4.2. FE of our amplifier is comparable to others even though we have matched at a single frequency. Additionally, the design methodology presented here requires tuning of second harmonic only whereas other works in Table 4.2 require impedances up to the 3rd harmonic, whilst designing the matching network. Amplifier [4.23] designed based on a series of continuous modes which relies on the inclusion of the resistive component has demonstrated higher bandwidth with similar FE indicating that our formulation will benefit from a similar extension to theory.

4.6. Conclusion

A new theoretical formulation for the current and voltage waveforms achieving efficiency ranging from that of class B to class F^{-1} is proposed in this work. Assisted by second harmonic manipulation, the mismatch in the phases of the fundamental components of voltage and current of these waveforms is lower than class J. An amplifier designed based on the proposed waveforms achieves 79.7% DE and 42.2 dBm output power at 2.6 GHz. A major implication of the proposed continuum is a wide design space available to designers with simultaneous high efficiency and output power in comparison to continuous class F^{-1} or class BJ, thus easing amplifier design.

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Chapter 5: Investigation of the effect of weak non-linearities on P1dB and efficiency of class B/J/J* amplifier

5.1. Introduction

Wireless communication systems require power amplifiers with high efficiency and linearity to reduce battery consumption and interference respectively. As a solution, Cripps proposed a continuum of voltage waveforms from class J*/B/J, which differ in phase, but achieve constant output power and peak efficiency [5.1]. These high-efficiency, yet linear, waveforms require inductive, short, and capacitive loads for classes J*, B and J, respectively, at the second harmonic, whilst the reactive component of the fundamental load is adjusted according to the load impedance at the second harmonic. The principle of class B/J/J* continuum has been applied to class F[5.2], class F^{-1}[5.3] and class E[5.4] modes to alleviate the need for precise load terminations with the resulting modes referred to as continuous classes F[5.5], F^{-1}[5.6] and E [5.7] respectively. The continuum modes demonstrate efficiency above 60% over a wide bandwidth [5.5][5.6][5.8][5.9][5.10] and allow the drain capacitance to be absorbed into the output matching network thus easing amplifier design [5.10].

Interestingly, the class B/J/J* continuum and the continuous class F demonstrate state-of-the-art high efficiencies at P1dB and at the back-off power levels, as summarized in Table 5.1. At one extreme, a low power (27.4 dBm) GaAs amplifier demonstrated 62% PAE at P1dB [5.11] whereas the continuous class F yielded a drain efficiency (DE) of 42% at 6.5dB back-off power level in [5.12] with a performance similar to that of a Doherty PA. It appears that the improvement of efficiency at back-off in Class B/J/J* can be attributed to the current generated from intrinsic capacitances. For the case of class J, the improvement over class B is due to the harmonics of current generated from the non-linear output capacitance C_{out} (a combination of the feedback capacitance (C_{gd}) and drain-source capacitance (C_{ds})) [5.13], corroborated in [5.14] and [5.15] by measured peak efficiencies 9.2% and 7% higher than class B respectively. The harmonics from non-linear C_{out} have been shown to improve peak PAE in continuous class F [5.12].

However, no work, to the best of our knowledge, describes the conditions to obtain high efficiencies at P1dB and back-off power nor has analysed the influence of the weak non-

TABLE 5.1: Reported high efficiencies at P1dB and back-off power

Ref.	Mode	Device Technology	Psat(dBm)	Merit	Freq. (in GHz)
[5.27]	Class B/J/J*	BiCMOS	18	31.5% PAE at P1dB	24
[5.11]	Class B/J/J*	GaAs pHEMT	27.4	62% PAE at P1dB	5.25
[5.25]	Class B/J/J*	GaN HEMT	39.7	50% DE at 5dB backoff	2.13
[5.22]	Class B/J/J*	GaN HEMT	41.2	50% DE at 5.5dB backoff	2.5
[5.18]	Class B/J/J*	GaN HFET	26.8	44% PAE at10dB backoff	2.5
[5.28]	CCF	GaN HEMT	40	50% DE at 5dB backoff	1.8
[5.12]	CCF	GaN HEMT	42.2	42% DE at 6.5dB backoff	2.14

DE and PAE denote Drain Efficiency and Power Added Efficiency respectively. CCF denotes Continuous class F. Freq. denotes Frequency.

linearities (non-linear gm and non-linear capacitances) on the performance of a class B/J/J* amplifier, as addressed in this work. A simple method that relies on an analysis of the influence of weak non-linearities on the intrinsic drain current is illustrated for the selection of high-efficiency voltage waveforms in the continuum.

5.2. Effect of weak non-linearities

The device selected for this study is a 10W GaN HEMT, CGH40010F. The device is biased in deep class AB mode (V_{dsq}=28 V, I_{dsq}=150 mA) and the optimal loadline resistance (R_L) found to be 38.1Ω. The equivalent circuit of the transistor used for the analysis is shown in Figure **5.1**. C_{ds} is assumed to be linear and C_{gd} and C_{gs} are assumed to be dependent on the gate-drain voltage (V_{gd}) and gate-source voltage (V_{gs}) respectively. The values of the extrinsic parasitic elements of the device in Table 3.2 which are extracted from the vendor model from the CGH40010 were used. The non-linear capacitors in Figure **3.12** are used in this chapter. The non-linear current generator I_{gen} is implemented via a table look-up as a function of the intrinsic gate (V_{gsi}) and drain (V_{dsi}) voltages.

5.2.1. Influence of intrinsic parasitic elements on intrinsic drain current

The influence of the currents flowing through the intrinsic capacitances on the drain current is analyzed by dividing the intrinsic device into resistive and capacitive cores [5.16] as shown in Figure **5.1**.

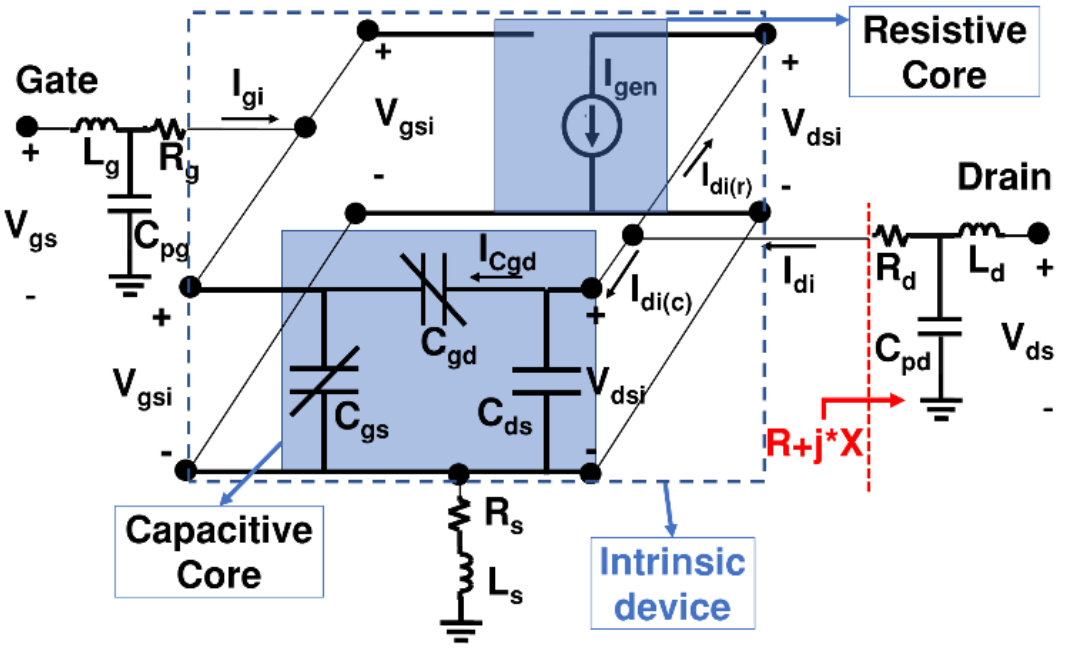

Figure 5.1: Equivalent model of a transistor with capacitive and resistive cores; R+j*X denotes the impedance at the fundamental frequency in parallel to C_{ds}.

The currents in the intrinsic device are calculated in the following way:

1) The current from the resistive core ($I_{di(r)}$) and the magnitude of the drain voltage in class B (v_s) upon application of a gate voltage (v_{gsi,f_0}) with frequency f_0 is obtained by imposing the loadline on the resistive core[5.17].

2) The continuum of voltages, V_{dsi}, from Class J* to B to J [5.18] is calculated using **5.1**

$$V_{dsi} = V_{dsq} - \delta_J v_s\{\cos(2\pi f_0 t + \Psi_1) + k_2 \cos(4\pi f_0 t + \Psi_2)\} \quad (5.1)$$

Where,

$$\delta_J = \sqrt{1+\alpha^2};\ \Psi_1 = \tan^{-1}(\alpha) \quad (5.2)$$

$$k_2 = \frac{\alpha}{2\sqrt{1+\alpha^2}};\ \Psi_2 = -\frac{\pi}{2} \quad (5.3)$$

Where, $\alpha \in [-1,1]$, δ_J denotes the voltage gain over a class B, Ψ_1 and Ψ_2 denote the phase of the fundamental and second harmonic components respectively, and k_2 is defined as the ratio of the magnitude of the second harmonic to the fundamental component. The values of V_{dsi} obtained from 5.1 for v_{gsi,f_0}=2V are plotted in Figure **5.2** (a).

3) V_{dsi} and V_{gsi} are applied to the capacitive core to obtain currents through the parasitic components of the intrinsic device. The overall current flowing through the device is obtained by superimposing the currents through the resistive and capacitive cores [5.17] [5.16].

Equation 5.1 reveals that the magnitude and phase of the fundamental frequency increases as we move from class B to J (α=1) and class B to J* (α=-1), as can be seen from Figure **5.2** (a), with classes J/J* having the highest magnitude of the fundamental voltage (δ_J) and phase mismatch (Ψ_1) given by $\sqrt{2}$ and |π/4| respectively. The effect of the magnitude and phase of V_{dsi} on the intrinsic drain current I_{dsi}(=$I_{di(r)}$+I_{Cgd}) where I_{cgd} denotes the intrinsic capacitive feedback current, is as follows:

(a) Its effect on $I_{di(r)}$ can be ignored if the device is in saturation i.e., the minimum of V_{dsi} remains above the knee voltage of the transistor (min(V_{dsi})>V_k). The simulated $I_{di(r)}$ is plotted in Figure **5.2** (b).

(b) An increase in the magnitude of V_{dsi} with |α| causes the magnitude of I_{Cgd} to increase with |α|, as seen from the plot of simulated I_{Cgd} in Figure **5.2** (b).

(c) The phase difference between $I_{di(r)}$ and V_{dsi} decreases as α increases (Figure **5.2** (a) and (b)). This leads to a reduction of the phase difference between $I_{di(r)}$ and I_{Cgd}, as seen in Figure **5.2** (b), thereby increasing the fundamental component of I_{dsi} ($I_{dsi,f0}$) flowing through the device with α, as shown in Figure **5.2** (c). For α=-1, the I_{Cgd} is out of phase with $I_{ds(r)}$, resulting in the lowest drain current flowing through the device.

(a), (b) and (c) are valid if min(V_{dsi})>V_k otherwise, strong non-linear effects (clipping of drain current) contribute to the intrinsic drain current. This condition is met only up to a certain amplitude of v_{gsi,f_0} depending on the device and R_L. For the current device and R_L, an amplitude of v_{gsi,f_0}<2.3V satisfies this condition. It can be inferred that as the frequency is varied, the magnitude of I_{Cgd} varies whilst the phase difference between I_{Cgd} and $I_{di(r)}$ remains the same. Hence the difference between the fundamental components of the drain current between α=-1 and α=1 increase with frequency.

5.2.2. Influence of intrinsic parasitic on output power, PAE and IMD3

The output power and PAE are obtained by a procedure, widely used in the literature: The intrinsic impedances at the fundamental ($Z_{L1,int}$) and second harmonic ($Z_{L2,int}$) frequencies of the continuum [5.18], given by (5.4), are translated to the extrinsic plane as in [5.8].

$$Z_{L1,int} = R_L + j\alpha R_L \tag{5.4}$$

$$Z_{L2,int} = -j\frac{3\pi}{8}\alpha R_L \tag{5.5}$$

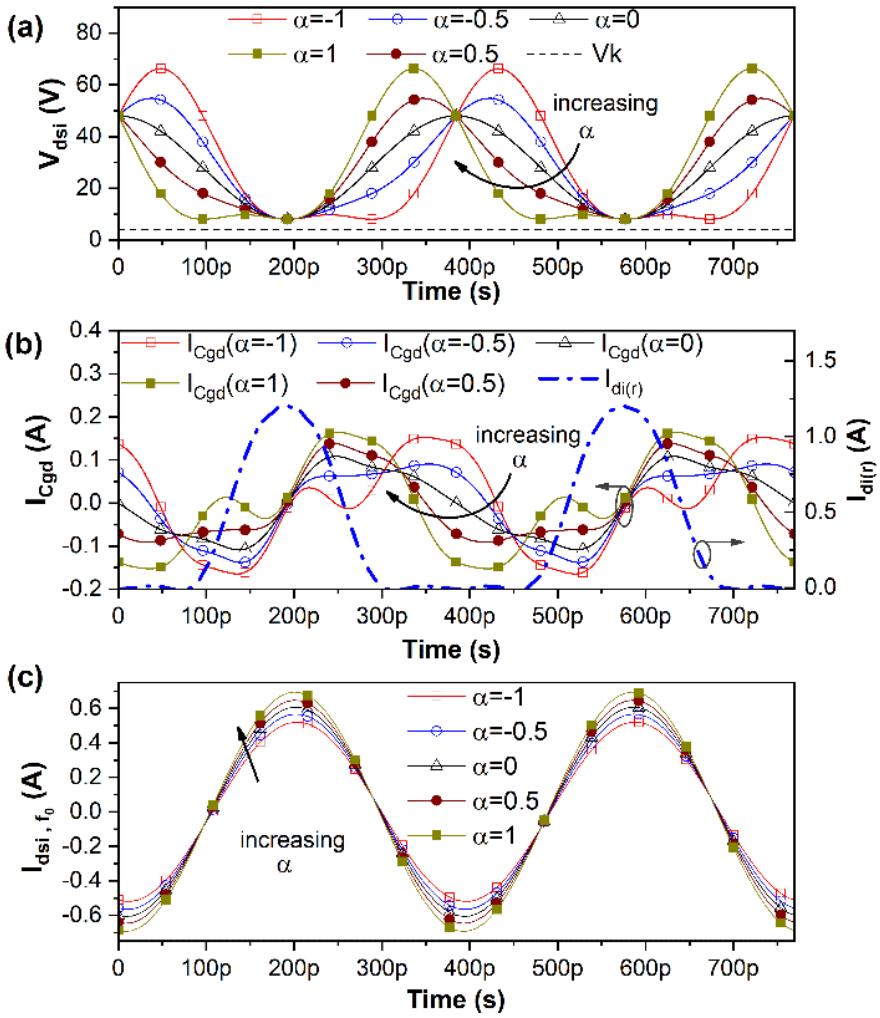

Figure 5.2: (a) Intrinsic drain voltage versus time (b) Intrinsic drain current from the resistive core and the feedback capacitor versus time (c) Fundamental component of the intrinsic drain ($I_{dsi,f0}$) current, at Vs=20V and v_{gsi,f_0}=2V as α is varied from -1 to 1 at a frequency (f_0) of 2.6 GHz and R_L=38.1Ω.

The optimal source impedance at α=-1 is used for all values of α so that a change in performance of the amplifier (gain, P1dB, and PAE) is a direct consequence of a change in the drain voltage with α. Matching networks are designed using ideal transmission lines.

Due to an increase in drain current with α, the gain of the amplifier and, thereby its efficiency, increase with α as seen from a plot of output power and PAE in Figure **5.3** (a). The increase in the gain from α=-1 to 1 is nearly 4 dB. Additionally, P1dB of class J is higher than class B whereas the efficiency and P1dB of class J* is less than that of class B. The increase in P1dB is because the 1dB compression is determined by harmonics from the non-linear Cgs and hence achieved at nearly the same input powers for all values of α. Since the gain increases with α, the output power corresponding to 1dB compression (P1dB) increases with α. The increment in P1dB from α=-1 to α=1 is 4dB whereas the increment in PAE corresponding to P1dB (PAE

at P1dB) is as high as 20%. These provide significant margins of improvement to amplifier designers.

The additional contribution of I_{Cgd} to drain current for α=1 leads to a higher change in output power for a given change of input power than for α=0 because of which the AM-AM distortion of class J is lower than for class B, as shown in Figure **5.3** (b). Since the flow of I_{Cgd} is out of phase with respect to I_{dsi} (refer Figures **5.2** (b) and (c)) for α=-1, it reduces the change of phase with input and hence AM-PM distortion for class J* will be lower than for Class B, as shown in Figure **5.3** (b). The contour of PAE with α and output power plotted in Figure **5.4** reveal that PAE at back-off output power increases with α, due to an increase in gain with α. The difference in PAE at 5dB back-off output power between -1 and 1 is approximately 6%. The plot of P1dB, P2dB, and P3dB in Figure **5.4** reveals that the variation in P1dB with α is greater than that of P2dB which is greater than P3dB. This is because, at higher compression, non-linear effects due to clipping dominate the performance rather than weak non-linearities. It has been shown that clipping of the drain current causes the output power and PAE of the amplifier to remain constant with α under the assumption that C_{ds} is linear [5.8]. Recent work has shown that non-

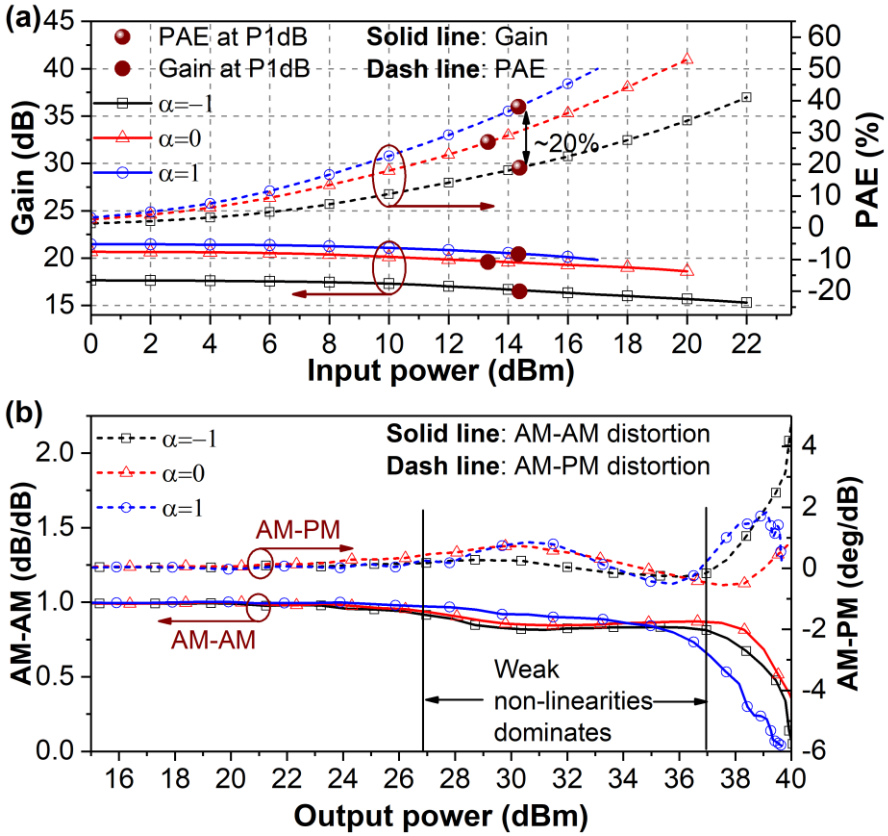

Figure 5.3: (a) Simulated Gain and PAE at 2.6 GHz for α=-1, 0 and 1 corresponding to class J*, class B and class J respectively. The input power is swept until the minimum of the drain voltage grazes the knee voltage. (b) Simulated AM/AM and AM/PM distortion for α=-1, 0 and 1 at 2.6 GHz.

linear nature of the C_{ds} results in an increase of output power and PAE at saturation for a range of α values, as observed in Figure **5.4** [5.19][5.20][5.21]. Nevertheless, the PAE corresponding to P1dB shows a greater variation than the PAE corresponding to P2dB and P3dB. This observation is in line with the literature, whereby, constant efficiencies over broadband were reported at P2dB [5.8] or higher compression levels [5.9], rather than P1dB, while [5.22] is an exception. In [5.22], the impedances, which were selected based on extensive load-pull simulations for efficiency near P1dB, in fact, correspond to α>0 (Figure 4 in [5.22]) which corroborates the results of this work.

A plot of gain and P1dB with α in Figure **5.4** reveals that the output power decreases for α>0.5 even though the power generated by the intrinsic device increases due to increase in drain current with α. This is because a reduction of R and |R/X| (to less than 1), given in equations 5.6 and 5.7, causes the power delivered to the load to reduce as α increases, where R and X (shown in Figure **5.1**) denote the resistance and reactance respectively in parallel with C_{ds} at the fundamental frequency.

$$R = \frac{R_L}{B^2 + (1 + \alpha B)^2} \tag{5.6}$$

$$\frac{R}{X} = \frac{1}{B(1 + \alpha^2) + \alpha} \tag{5.7}$$

where $B = 2\pi f_0 C_{ds} R_L$.

For B<1, |R/X| becomes less than 1 for $\alpha > \alpha_c$, where,

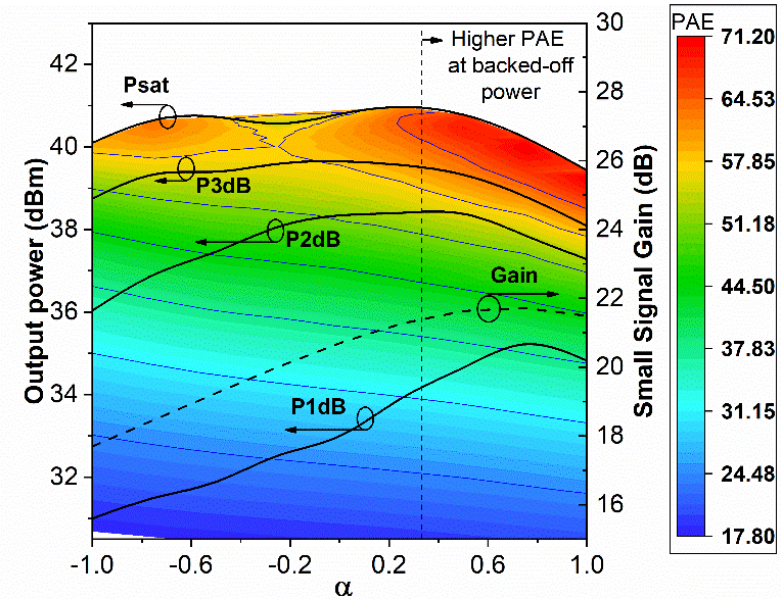

Figure 5.4: Simulated PAE contours as a function of output power and α. P1dB, P2dB, P3dB, Psat (the output power at saturation), and gain for α between -1 and 1 at 2.6 GHz.

$$\alpha_c = -\frac{0.5}{B} + \sqrt{\frac{1-4B}{4B^2} - 1} \quad (B < 1) \tag{5.8}$$

In Figure **5.4**, B=0.68 and α_c=0.26, and R/X gradually decrease from 1 at α=0.3 to 0.5 at α =1, as seen in Figure **5.5**, counteracting the increase in power generated at the intrinsic plane due to the feedback capacitor and voltage gain (δ_J). Hence, the maximum output power and gain are achieved at a balance point between α_c and 1, in this case, α≈0.65. On the other hand, |R/X|<1 leads to suppression of harmonics of the voltage delivered to the load for $\alpha > \alpha_c$ [5.23]. As we reduce the design frequency (B), α_c increases whereas the effect of parasitics decreases. For low frequencies ($B \ll 1$), leading to $R \approx R_L$ and $|R/X| = |1/\alpha| > 1$, which implies that the power generated at the intrinsic plane is transferred to the load, independent of α. This implies that at high frequencies, where B is close to 1, a subset of the continuum defined by α>α_c has a constant P1dB and a flat gain response.

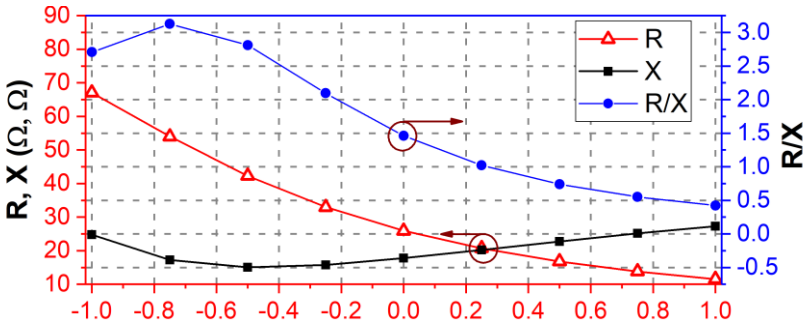

Figure 5.5: Simulated R, X, and R/X with α, where R and X denote the effective resistance and reactance respectively in parallel with C_{ds} at f_0.

Simulated third-order intermodulation distortion (IMD3) shows small improvement for α>0.5 for P_{out} between 26dBm and 36 dBm, as shown in Figure **5.7** (a), because of the lower AM-AM distortion as seen in Figure **5.3** in this power range, that results in a slight improvement in ACPR (Adjacent Channel Power Ratio) of 16-QAM signal in simulation for average power between 22dBm and 30dBm in Figure **5.7** (b). On the other hand, because of the lower AM-PM distortion for α<0, seen in Figure **5.3**, the EVM (Error Vector Magnitude`) improves over class B (Figure **5.7** (b)).

The higher gain for α> 0 coupled with a slight improvement in IMD3 for P_{out} between 26dBm and 36 dBm, causes PAE corresponding to a given IMD3 (between -30dBc and -20dBc) to improve by 10% and 5% for α=1 and α=0.5 respectively as shown in Figure **5.6**. For lower IMD3 (<-30 dBc), P_{out} <26 dBm, PAE is weakly dependent on α because the drain current is comparable to the bias current and I_{Cgd} is negligible. Importantly, Figures **5.4**, **5.7**, and **5.6**

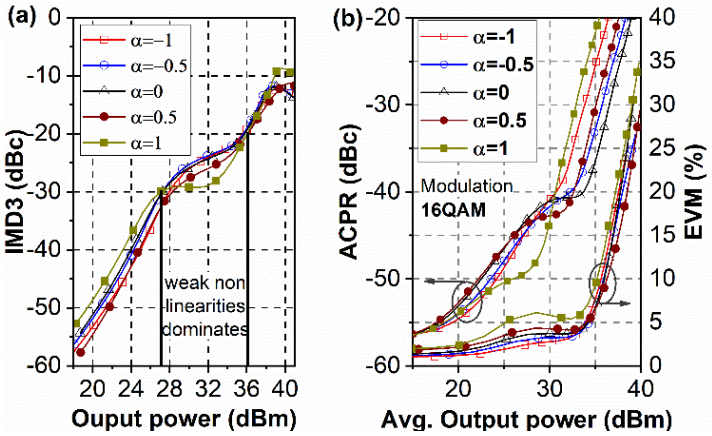

Figure 5.7: (a) Simulated IMD3 versus output power (using vendor model) for α between -1 and 1(b) Simulated ACPR and EVM for a 16-QAM signal. Data rate (3.84Mbps) and channel bandwidth (5MHz) of the input signal are same as in WCMDA. The peak to average ratio of the input signal is 2dB

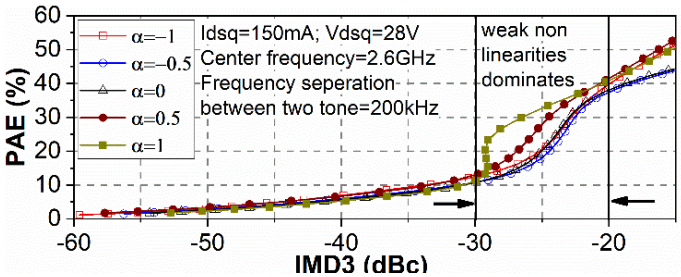

Figure 5.6: Simulated PAE versus IMD3 as α varied from -1 to 1 using vendor model. The frequency separation between the tones is 200kHz.

reveal that for a set of waveforms in the class B/J continuum, higher P1dB, and higher efficiency at P1dB and at back-off power levels is achievable than class B, without sacrificing IMD3. For the current device, operating at frequency 2.6GHz, this set is defined as $\alpha \in [0.4,1]$. The conclusions of this investigation can be extended to continuous class-F since continuous F mode has a similar variation of the phase of voltage [5.5].

5.3. Implementation and experimental results

5.3.1. Amplifier design

Based on Figure **5.4** an α≈0.55 is selected as the optimum value for a high P1dB and efficiency at P1dB without sacrificing the maximum output power. The extrinsic fundamental (Z_{L1}) and second harmonic (Z_{L2}) impedances for α≈0.55 are calculated using the method in section 5.2. The optimal source impedance (Z_{s1}) which maximizes P1dB without sacrificing gain, is obtained from source pull simulations of the vendor model. The input and output matching networks are realized using stepped impedance and double stub configurations respectively, as

shown in Figure **5.8** (a), on a RO4350B substrate of thickness 0.762mm. The output matching network consists of one segment to match Z_{L1} and another segment to match Z_{L2}. The segment matching the second harmonic impedance is placed close to the device to minimize matching network losses [5.24] and the stub in it shorts the second harmonic. Hence, the segment matching Z_{L1} does not influence Z_{L2}; allowing independent control of the fundamental and second harmonic impedances in the matching network, easing its design and optimization.

It is observed that the matching networks of this amplifier do not satisfy the stability criterion

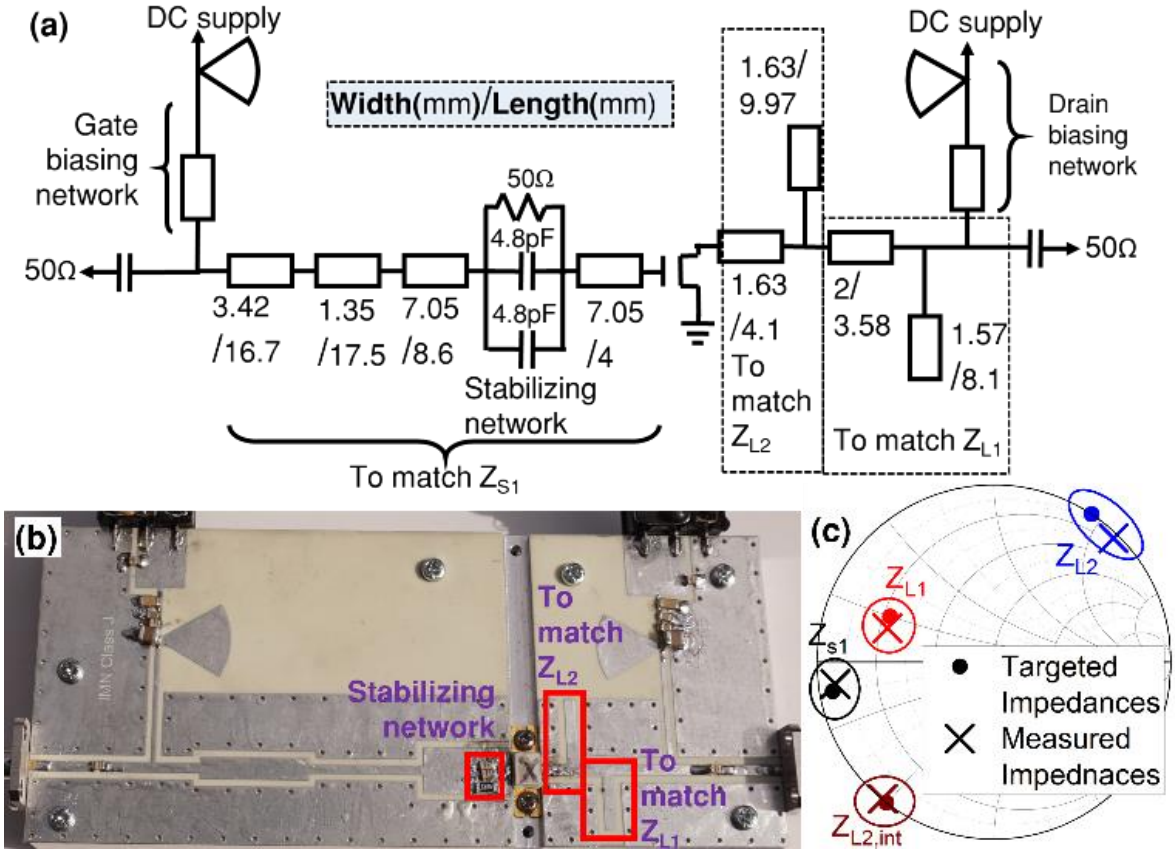

Figure 5.8: (a) Schematic of the designed amplifier (b) Photograph of the designed amplifier (c) Measured and targeted source impedance at fundamental frequency (Z_{s1}), extrinsic load impedances at fundamental (Z_{L1}) and second harmonic frequencies (Z_{L2}), and intrinsic load impedances at second harmonic frequency ($Z_{L2,int}$)

discussed in chapter 2 at low frequency. This is because this GaN HEMT device has very high gain at very low frequencies and hence is prone to instability. To make the amplifier stable, we have placed a high pass filter close to the gate terminal of the device which will compensate for the GaN HEMTs high gain at low frequencies. This high pass filter is realized by a parallel RC network in the input matching network and the values of resistor and capacitor are chosen

to ensure unconditional stability while having a minimal effect at the design frequency[5.25]. The designed amplifier is shown in Figure **5.8** (b).

5.3.2. Measurement Results

The fabricated matching networks are measured individually and are compared with the targeted values in Figure **5.8** (c), which shows that Z_{s1} and Z_{L1} are in close agreement. The difference between the target and measured Z_{L2} does not affect the performance of the amplifier as the discrepancy in the corresponding intrinsic impedances ($Z_{L2,int}$), in turn, in α, is small as can be seen from Figure **5.8** (c).

The measured and simulated output power, gain and efficiency of the fabricated class J are plotted in Figure **5.9** (a). The peak efficiency achieved by this amplifier is 72.3% and the output power at saturation is 41.72dBm. The output power and efficiency at 1dB compression are 38.13dBm and 54.7%. Measured IMD3 and PAE with a two-tone signal shown in Figure **5.9** (b) reveal that IMD3 remains below -30dBc and -20dBc till 35dBm and 38.7dBm output power respectively and attains PAE of 39% and 58.6% respectively.

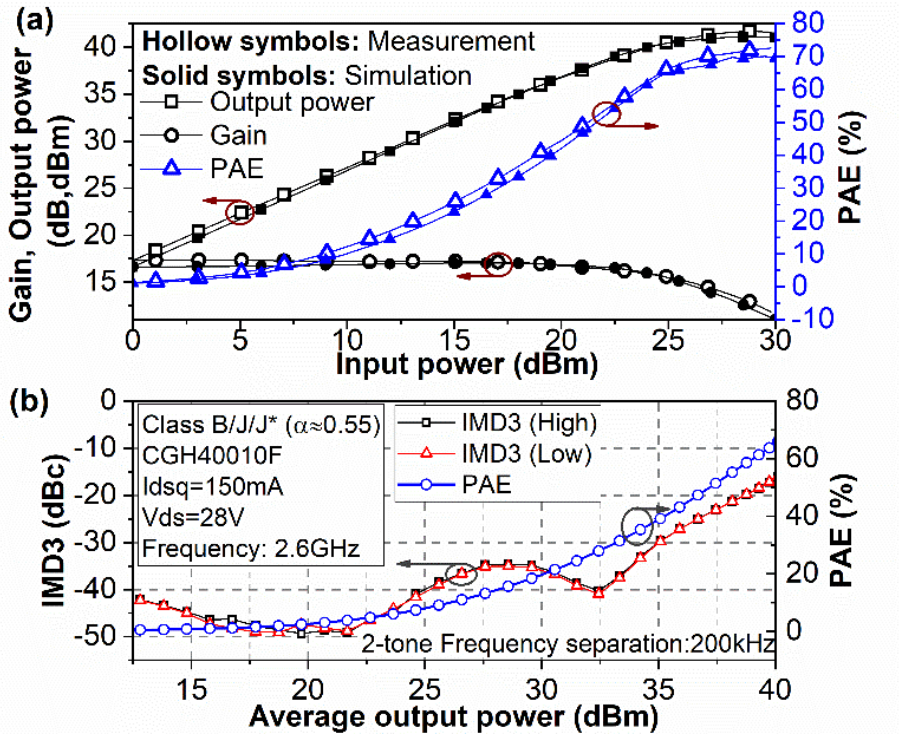

Figure 5.9: (a) Measured and simulated (using vendor model) gain, output power and PAE of the designed amplifier. (b) Measured IMD3 products and PAE of the designed amplifier under two-tone excitation centred at 2.6GHz with frequency separation of 200kHz

The designed amplifier is compared with the state of the art high-efficiency narrowband linear amplifiers using the same device in Table 5.3. Our design shows a higher figure of merit than those reported in terms of output power and PAE at 1dB compression. The PAE at 5dB back-off is nearly 45%, which is comparable to reported high efficiency at back-off power for the amplifiers with P_{sat} close to 40dBm given in Table 5.1. As can be seen from Figure **5.4**, even higher efficiency can be achieved by choosing a higher value of α but at the expense of output power and P1dB. A comparison of the fabricated PA with saturated PA, optimized for peak efficiency from [5.13], in Table 5.2 reveals that the designed amplifier achieves PAE lower by 3% at -35dBc ACLR whereas 13% higher PAE is achieved at ACLR of -22.3 dBc than the saturated PA. The designed amplifier achieves 14% higher PAE than class AB at the IMD3 level from [5.26]. This shows that higher efficiencies than class AB and saturated PA can be achieved for a given distortion level in the region dominated by the effect of non-linear capacitances as shown in Figure **5.7**, for this device between -30dBc and -20dBc.

TABLE 5.3: State of the art high efficiency linear narrowband amplifiers reported in literature using GaN HEMT (CGH40010)

Ref.	Mode	Freq. (in GHz)	Peak PAE (%)	Figure of Merit	PAE at P1dB (%)	P1dB (dBm)	Psat (dBm)
[5.13]	Saturated PA	2.14	77.3	113	42.55*	35.06*	40.6*
[5.25]	Class J	2.13	64.5	94	47.57*	35.73*	39.7
[5.23]^	Class J	1.5	87#	106#	55.2#	35.6	39.5*
[5.26]	Class AB	2.25	45	67.5	32	39	40
This work	Class B/J/J*	2.6	72.3	116	54.7	38.13	41.7

Figure of Merit=Peak PAE*(**Freq.** in GHz)$^{1/2}$ where **Freq.** is Frequency *These values are extracted from the figures in the papers; ^ design procedure adopted in [24] does not sacrifice efficiency at the reported frequency whilst achieving broad bandwidth; # Drain efficiency

TABLE 5.2: Comparison of ACLR/IMD3 and average PAE with Narrowband Power amplifier designed using CGH40010 reported in literature

Reference	Mode	Freq. (GHz)	ACLR/IMD3 (dBc)	Avg. Output power (dBm)	Avg. PAE (%)
[5.13]	Saturated PA	2.14	-22.3#	34.2	42.3
This work	Class B/J/J*	2.6	-22.3*#	38.25	55.8
[5.13]	Saturated PA	2.14	-35#	28	20
This work	Class B/J/J*	2.6	-35*#	28	17
[5.26]	Class AB	2.25	-21	40	41
This work	Class B/J/J*	2.6	-21	38.3	56

Bandwidth of input signal is 10MHz. ACLR in [5.13] is measured at offset 7.5MHz. * ACLR estimated from measured IMD3 [5.29] in 5.9.

5.4. Conclusions

The study of the influence of the non-linear feedback capacitance, on the performance of a class B/J/J* continuum amplifier, shows that the gain, P1dB, and efficiency at back-off power increase from class J* to class B to class J due to a variation of the phase of the voltage waveforms across its non-linear Cgd. Based on this knowledge, a trade-off involved with the choice of α is analyzed in this chapter. It is shown that a subset of the continuum results in higher PAE at P1dB than Class B (or deep class AB) and these modes can be replaced by the class B/J/J*, at a higher frequency, without sacrificing linearity using the methodology presented here. This work utilizes this additional benefit of the continuum, not previously discussed, which is a remarkable 20% increase in efficiency at P1dB from class J* to J, to prototype a high efficiency (72% PAE) power amplifier displaying 38 dBm P1dB and 55% PAE at P1dB.

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Chapter 6: An Integrated on-chip flux concentrator for galvanic current sensing

6.1. Introduction

On-chip current sensors are desirable components to provide inbuilt protection of power devices against current overshoot and to enhance the short circuit capability of smart power ICs and RF power amplifier MMIC. Galvanic sensors, such as the MagFET [6.1] and hall-effect sensors, which detect the strength of the magnetic field can be used for current monitoring [6.2]. MagFET and hall effect sensor utilize the change in the current and the Hall voltage due to the deflection in the moving charges induced by the external magnetic field respectively. The change in the current and voltage is proportional to the external magnetic field. The magnetic fields generated by the electric current flowing through a metal strip either power load current or the SenseFET current can be measured using these galvanic sensors and the current from the conductor line can be estimated based on the measured magnetic field[6.3][6.4]. Such a non-invasive method of current monitoring is highly attractive in a wide range of applications because of easier integration and low circuit cost [6.2].

The sensitivity of a galvanic current sensor to the magnetic field depends on the carrier mobility, hall factor and its geometry[6.5][6.6]. In this context, inherent polarization in GaN gives rise to a high-density 2DEG even without the application of an external bias. Despite bulk mobility lower than that of silicon, electrons in this 2DEG have the mobility of up to 2000 cm^2/Vs, approximately 50% higher than that in silicon [6.7]. This lends itself to extremely sensitive MAGFETs[6.8] and Hall devices [6.9] in GaN that are attractive on account of their compatibility with integrated CMOS drivers for power management ICs in GaN [6.10].

The resolution and sensitivity of a galvanic current sensor to current can be increased further by an arrangement consisting of two [6.5][6.11] or more magFETs [6.12][6.13] at the cost, however, of increasing the chip area. Alternatively, the induced current deflection or induced voltage of a galvanic sensor can be increased by increasing the magnetic field at the sensor. Increasing the magnetic field induced by the current to be sensed is more favourable and achievable than an increasing number of sensors. This can be achieved by routing the metal line around the hall device [6.14][6.15]. Alternatively, the galvanic current sensor could be accompanied by its magnetic flux concentrator [6.4][6.16] which acts as a passive amplifier of the magnetic field. By applying the concentrator, the magnetic field is enhanced while the

current to be sensed remains the same, thereby reducing the current demand for the same flux and reducing the conduction loss in the power module.

In this work, we propose a structure to amplify the magnetic field strength in a galvanic current sensor, such as a MagFET or a Hall sensor, which relies on a combination of both the above approaches: routing a copper line around a sensor as well as a magnetic concentrator.

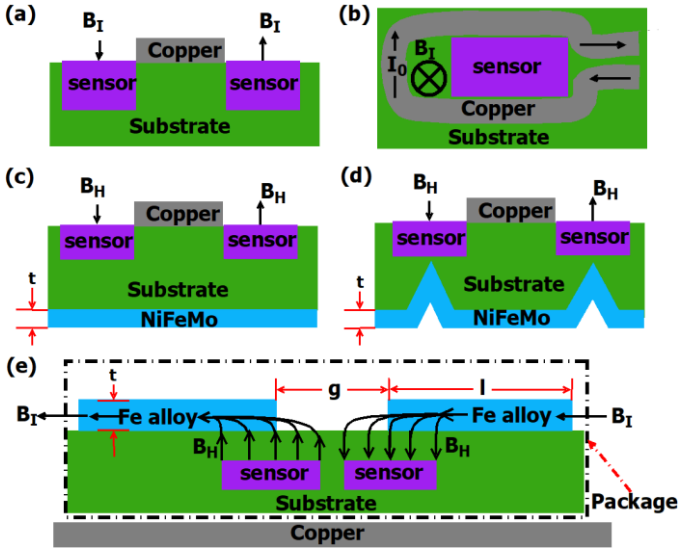

Figure 6.1: Arrangement of Galvanic current sensors in on-chip implementations (a) On-chip integrated current sensor [6.5][6.12] (b) Conductor loop [6.15] (c) Sheet magnetic concentrator [6.4] (d) Tip magnetic concentrator [6.4]. (e) Integrated magnetic concentrator (IMC) at the top [6.16].

Moreover, this structure is much easier to fabricate than a conventional inductor [6.17].

6.2. Background and Methodology

Figure **6.1** describes implementations of conventional sensors for on-chip current sensing. In Figure **6.1** (a), sensors surrounding a conductor carrying a current (I_0) to be sensed, rely on its magnetic field, (B_I), in a direction normal to the surface as [6.5]

$$B_I = F_I I_0 \tag{6.1}$$

Where, F_I the conversion factor of the structure depends on the relative position of the sensor with respect to the conductor. In Figure **6.1** (b) the current circles around the sensor increasing the magnetic field, resulting in higher F_I than in Figure **6.1** (a). F_I can be further improved by increasing the number of loops of the copper line around the sensor in Figure **6.1** (b) [6.15][6.18]. Alternatively, a magnetic material is used to increase the field strength by concentrating the magnetic flux at the sensor in Figures **6.1** (c), (d), and (e). These magnetic material structures, referred to as flux concentrator, act as magnetic amplifiers with magnetic

gain G_M. The G_M depends on the shape and the magnetic properties of the flux concentrator. The magnetic thin film shown in Figure **6.1** (c) increases the component of the magnetic field along the normal direction, whereas its tip implemented via a groove increases the flux density in Figure **6.1** (d) even further. These require fabrication steps at the back of the substrate, including substrate thinning. In contrast, integrated magnetic concentrators (referred to as IMCs) are integrated on the same side as the sensor [6.16]. Integrated magnetic concentrators (IMC)[6.16], shown in Figure **6.1** (e), utilize the fringing magnetic field at the edge to convert the applied uniform magnetic field parallel to the surface into the vertical direction. The magnetic field at the surface of the sensor in the normal direction can be related to the current through it as:

$$B_H = F_I G_M I_0 \tag{6.2}$$

where F_I is the conversion factor in the absence of the flux concentrator and I_0 is the current passing through the metal strip.

The effective conversion factor (F_c) in these cases can be expressed as

$$F_c = \left(\frac{B_H}{I_0}\right) = \left(\frac{B_H}{B_I}\right)\left(\frac{B_I}{I_0}\right) = F_I G_M \tag{6.3}$$

Where, $G_M = B_H/B_I$, and B_H and B_I denote the minimum normal component of the magnetic field at the sensor with and without field concentrators.

In comparison to the above, we propose a novel structure in Figure **6.2** (a) with an underlying sensor, in this case, a GaN substrate, which improves both F_I and G_m. Figure **6.2** (b) depicts how a conventional loop inductor, with a copper line surrounded by a laminate of magnetic material or an air core, might typically be integrated with the sensor [6.19]. Figure **6.2** (c) shows the cross-sectional view of our novel structure in which the magnetic core does not extend beneath the copper line (A-B). Φ_{Top}, Φ_{right}, Φ_{left} and Φ_{bottom} in Figures **6.2** (b) and (c) denote magnetic fluxes in the directions identified as the top, right, left, and bottom, respectively, at the junction where the magnetic via meets the magnetic layer at the surface "A" identified in the figures. The magnetic field in both structures is normal to the sensor as required because of the structural symmetry around the X-Z plane.

Typically a small proportion of the total current (I_{total}) to be sensed is diverted into the conductor using a busbar with a notch [6.20] or a SenseFET [6.21] shown in Figures **6.2** (d) and **6.2** (e) respectively. In the former, a proportion of the current flowing through the loop

inductor is determined by the ratio of the width of the copper in the inductor and the bus bar i.e., the ratio of the series resistance of the inductor and bus bar. In the latter case, the ratio of the widths of the SenseFET and the power device determines the proportion of current flowing through the loop inductor. In both cases, since the proportion is fixed and known, the overall current can be estimated from the measured I_0. Based on a current-carrying capability of Cu/Au of ~10^6 A/cm^2, I_0 up to 50 mA can safely flow through a metal line of width 5 µm and thickness 1 µm.

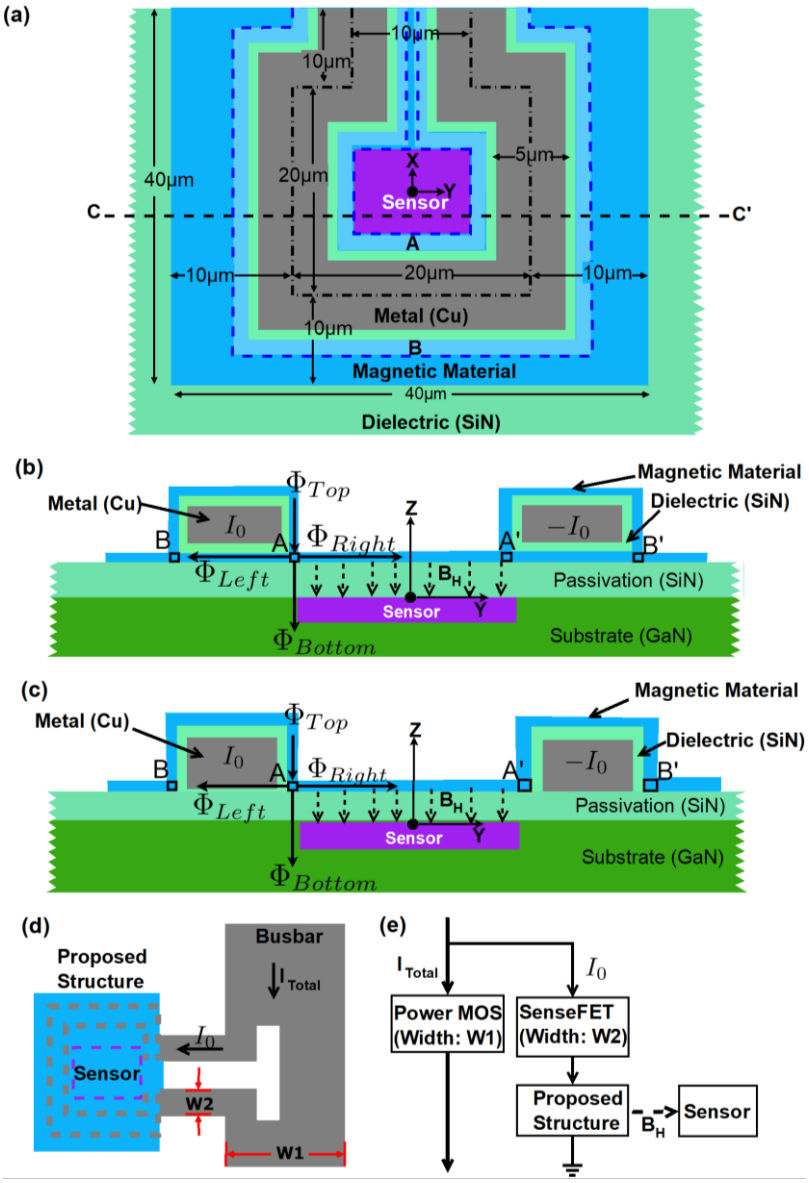

Figure 6.2: (a) Top view of a loop inductor integrated with a galvanic current sensor i.e. (a MagFET or a hall-effect sensor). (b) Cross-sectional view across C-C' assuming a conventional loop inductor with magnetic film below the Cu wire (c) Cross-sectional view across C-C' of the proposed structure without magnetic film below the Cu wire. (d) A schematic of a busbar with a notch to divert a portion of the total current (I_{Total}) into the proposed structure. (e) A schematic using senseFET to divert a portion of the total current (I_{Total}) into the proposed structure.

Two geometries of the loop inductor are compared using magnetostatic simulations in ANSYS EM suite (Maxwell) on a GaN substrate of thickness 80µm with relative permittivity and resistivity set to 9.5 and 6 Ω-cm respectively [6.22]. We find that the resistivity of the substrate does not affect the results within a range of 0.1-100 Ω-cm. The passivation consists of 300 nm of SiN of relative permittivity 7 [6.23]. The width and thickness of the copper line of the inductor are 5 and l µm respectively. The thickness of the magnetic film is 200 nm. Soft magnetic alloys, CoZrO, CoTaZr, and CoTaZrB, which are widely considered for on-chip inductors in CMOS, have reported permeability in the range 67-83 [6.24], 1000 [6.19], and 665-1080 [6.23]. Their corresponding resistivity is 600Ω-cm [6.24], 99 Ω-cm [6.19], and 115 Ω-cm [6.23] respectively. Therefore, the permeability of the magnetic material is varied from 10 to 1080 in simulations, whereas resistivity is set to a nominal value of 100 µΩ-cm, representing the worst-case scenario for eddy current losses. The current through the inductor (I_0) is set to 20mA.

6.3. Results and Discussion

A change in the field distribution due to removal of the magnetic material below the Cu wire between A and B is illustrated by a ratio of fluxes from the left, right and bottom, with respect to the flux at the top viz., Φ_{Left}/Φ_{Top}, Φ_{Right}/Φ_{Top}, and Φ_{Bottom}/Φ_{Top} respectively, plotted in Figure **6.3**.

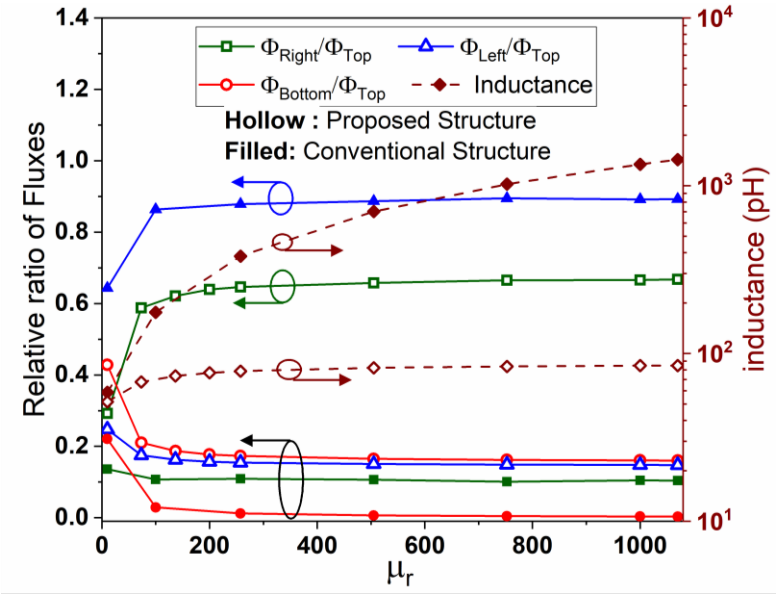

Figure 6.3: The ratio of fluxes (Φ_{right}/Φ_{Top}, Φ_{left}/Φ_{Top}, and Φ_{bottom}/Φ_{Top}) and inductance of the proposed and conventional structures versus μ_r.

In the conventional structure, as μ_r is increased, Φ_{Left} increases at the expense of Φ_{Bottom}, and saturates beyond μ_r =200. For μ_r>200, most of the flux induced by the current I_0 is concentrated

within the magnetic material with nearly 90% looping around the copper winding, resulting in an increase of inductance with μ_r while only 10% leaks into the magnetic film between the

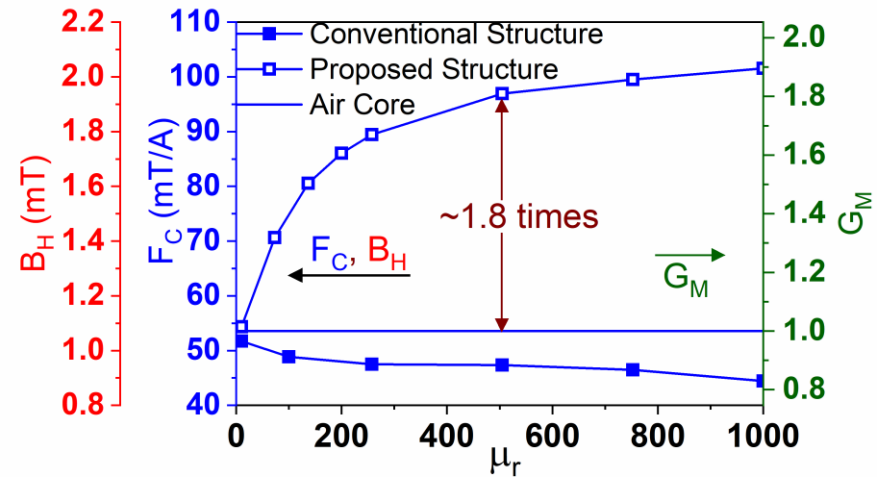

Figure 6.4: Conversion factor (F_C), magnetic field at the sensor (B_H), and magnetic gain (G_M) of the conventional, air core, and proposed structures versus permeability.

conductors. This is because the magnetic material around the metal layer offers a low reluctance path to the field lines through the copper with very little available to the underlying sensor. On the other hand, in the proposed structure, due to the presence of the magnetic material on the right coupled with an absence of magnetic material between A-B causes the field distribution to shift towards the right and bottom as evident from Figure **6.3**; Φ_{Bottom} and Φ_{Right} are 80% of Φ_{Top} showing an opposing distribution of the field. Φ_{Bottom} is still a considerable percent (at least 18%) of the overall flux induced in the magnetic via (Φ_{Top}) for all values of μ_r. Hence, the magnetic field in the substrate is enhanced by the current flowing through the copper as well as field penetration at the discontinuity A-B for all values of μ_r.

Conversion factors (F_c) of the conventional, proposed and air-core structures with the permeability of the magnetic material are plotted in Figure **6.4**, indicating an increase of G_m, and thereby F_c, of the proposed structure by the factor of 1.8. On the other hand, F_c of the conventional structure reduces from 52mT/A to 45 mT/A.

Recent work [6.25] has shown that the optimal length of the MagFET is 65 um which is longer than the initial generation of GaN sensors proposed in [6.19], the single loop flux concentrator in Figure **6.5** is modified accordingly and the corresponding dimensions are shown in table 6.1.

The relative permeability of the magnetic film μ_r=1000 (similar to CoTaZr) [6.17] is used for simulation. The magnetic field induced by the flux concentrator (B_{eff}) is at an angle, Φ with respect to the underlying sensor as shown in Figure **6.6** (a), with its *z*-component labelled (B_z).

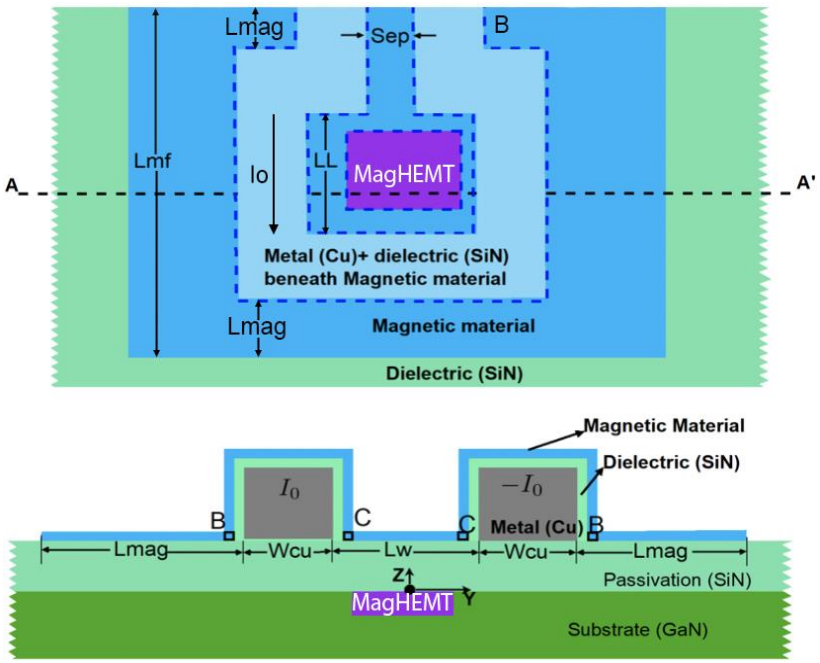

Figure 6.5: (a) The top view of the planar flux concentrator of cross section and (b) the cross-sectional view at A-A'.

TABLE 6.1: The dimension of the single loop integrated flux concentrator chosen for the new generation of Sensors				
L_{mag}	**L_w**	**Sep**	**W_{cu}**	**LL**
7.5 µm	22 µm	5 µm	5 µm	65 µm

The contours of Φ and B_z in the single loop configuration of the flux concentrator (shown in Figure **6.5**) are plotted in Figures **6.6** (b) and (c) respectively. The Φ remains less than 1^0 for nearly 90% of the sensor surface and less than 5^0 throughout the sensor surface. Such a small deviation cannot be obtained from concentrators which rely on fringing magnetic fields, such as tip concentrators and IMCs unless their size is several orders larger than the sensor. The magnitude of the field increases by 3-4 times as we move towards the edge from the centre as shown in Figure **6.6** (b). Additionally, the conversion factor defined by (6.3) as the ratio of the magnetic field to the current flowing through the loop is higher at the edge than the centre. However, the conversion factor reduces from 96 mT/A for L×W=15 × 15 μm^2 in Figure **6.4** to 58 mT/A as the length increases and the magnetic field reduces due to an increase in separation of the current paths.

Table 6.2 shows an improvement in the conversion factor of our structure in comparison to reported structures also evaluated via simulation alone, by a factor of 12. The major drawback of the tip and sheet concentrator is the fabrication required at the bottom surface of the substrate

including substrate thinning. The IMC requires a large chip space (in the range of mm) and thicker magnetic material, typically in the range of 20um, ideally equal to gap marked as "g" in Figure **6.1** (e), in the magnetic material near the sensor. The permeability of the magnetic material should be greater than 1500 and a minimum length is 250um to achieve G_m of 1.5 [6.26].

On the other hand, the proposed structure achieves a gain of 1.8 at a fraction ($\sim\frac{1}{60}$) of chip space and much lower permeability. Another major drawback of the IMC is a requirement of a constant B field to be applied throughout requiring the width of the conductor to be of a similar order as that of the IMC.

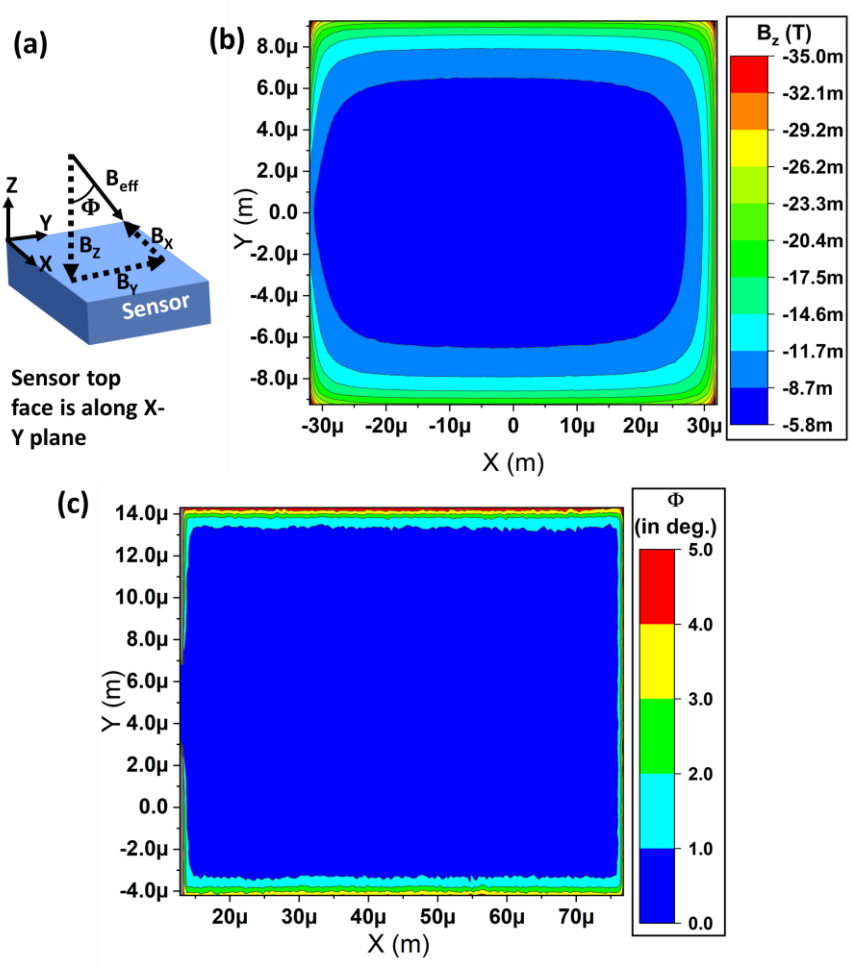

Figure 6.6: (a) The schematic of magnetic field components on top of sensor, (b) contours of strength of magnetic field along z-direction above the sensor, and (c) contours of angle between the Bz and effective magnetic field. These contours reveal the proposed flux concentrator generates magnetic field along the normal to the sensor as required with the angular deviation less than 5 degrees.

TABLE 6.2: A Comparison of the conversion factor from this work with reported literature

structure	Ref.	FI (mT/A)	GM	Fc (mT/A)	μr	t (um)
Magnetic sheet	[6.4]	0.05-0.1	1.5	0.075-0.15	~$2x10^4$	1.5
Tip concentrator	[6.4]	0.05-0.1	3*	0.15-0.3	~$2x10^4$	1.5
On-chip Metal line	[6.12]	4.95	--	4.95	--	--
	[6.5]	8	--	8	--	--
Integrated Magnetic concentrator	[6.16](a)	--	5*	--	~10^4	20
	[6.27](b)	--	21	--	10^5	22
	[6.26](c)	0.02-0.5[6.28]*	8*	0.16-4	>1500	20
Proposed Structure	**This work(d)**	**53.7**	**1.8**	**96.6**	**>500**	**0.2**
	This work(e)	**32.2**	**1.8**	**58**	**>500**	**0.2**

*experimental

(a) Tanga shape; Length:1.1mm; width:0.5mm

(b) Tanga shape; Length:2mm; Width:1mm

(c) Two Circular IMCs; diameter: 1mm.

(d) Square shape; Length:40um; Width:40um

(e) Square shape; Length:85um; Width:47um

Even though IMCs achieve higher G_m than other structures, they suffer from low F_I because they are designed to measure the current in off-chip conductors. The proposed structure and on-chip metal line perform better because the current conductor is separated from the B sensor by passivation alone. It is to be emphasized that the proposed structure is intended only for on-chip current detection, whereas the IMC is also versatile in angular sensing, e-compass, position sensing.

6.4. Study of Induced Field and Conversion Factor of the on-chip spiral flux concentrators

To increase the conversion factor back to its original value, a second copper loop in the spiral structure is required, shown in Figures **6.7** (a) and (b). The effective conversion factor of the single loop structure as its length (indicated by LL in Figure **6.7** (a)) increased from 20 μm to 65 μm is plotted in Figure **6.8**. The result of this alteration on the predicted conversion factor is shown in Figure **6.8** (red line). Two loops in a planar geometry do not improve the

performance (and are not indicated here). The inductance of the single loop and spiral structures are plotted in Figure **6.8**. Inductance increases as the length increases, however, the value of inductance is lower than 1 nH for the cases, which has a minimal impact on the rise time.

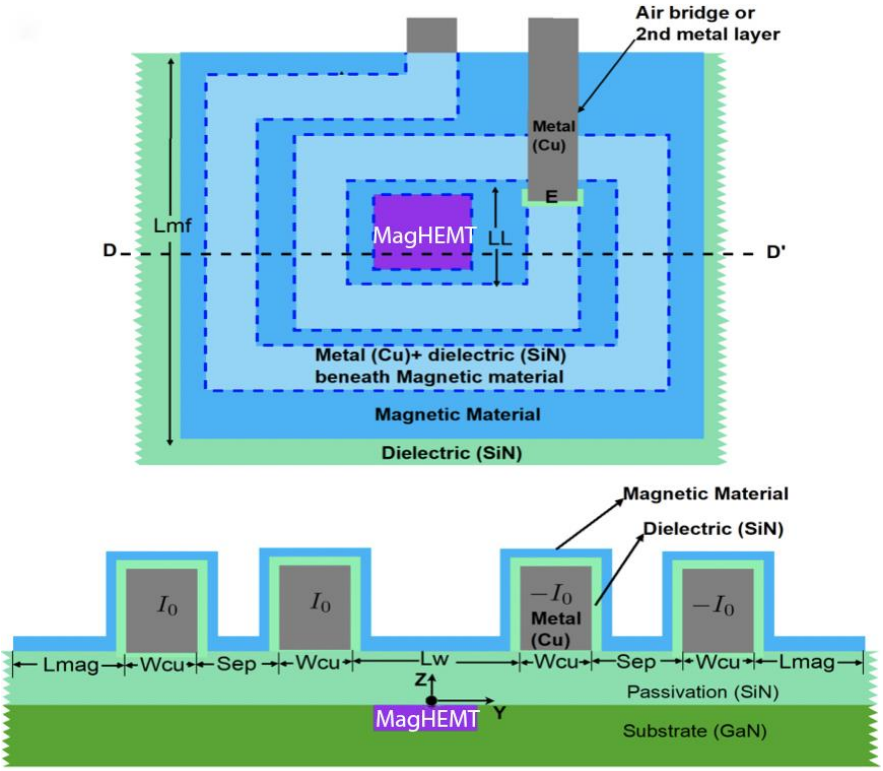

Figure 6.7: (a) The top view of the planar flux concentrator of cross section 15x15 microns and (b) the cross-sectional view at A-A'. (c) Top view of the flux concentrator with the copper spiral for dimensions > 15×15 microns. (d) The cross-sectional view of the structure at D-D'.

Unlike a single loop, whose length (LL) can be chosen the same as the sensor, the spiral flux concentrator needs to be longer than the sensor. This is because, at the air bridge (marked E in Figure **6.7** (c)), the flow of current lies along the *z*-direction and the fringing fields from the discontinuity of the magnetic film at E contribute to the magnetic fields along X and Y direction, i.e. tangential to the surface of the sensor. This is illustrated by the contours of Φ at the surface of the sensor in Figure **6.8**. The direction of the fringing field is no longer in the *z*-direction near point E, but remains as high as 60^o, in comparison to 6^o in the centre. As a result, the double or multiloop structure needs to be longer than the sensor, by at least 15 μm in the present case.

The proximity of the current loop to the sensor is limited by the quality of the SiN passivation and can be increased as necessary to the micrometre range. The conversion factor

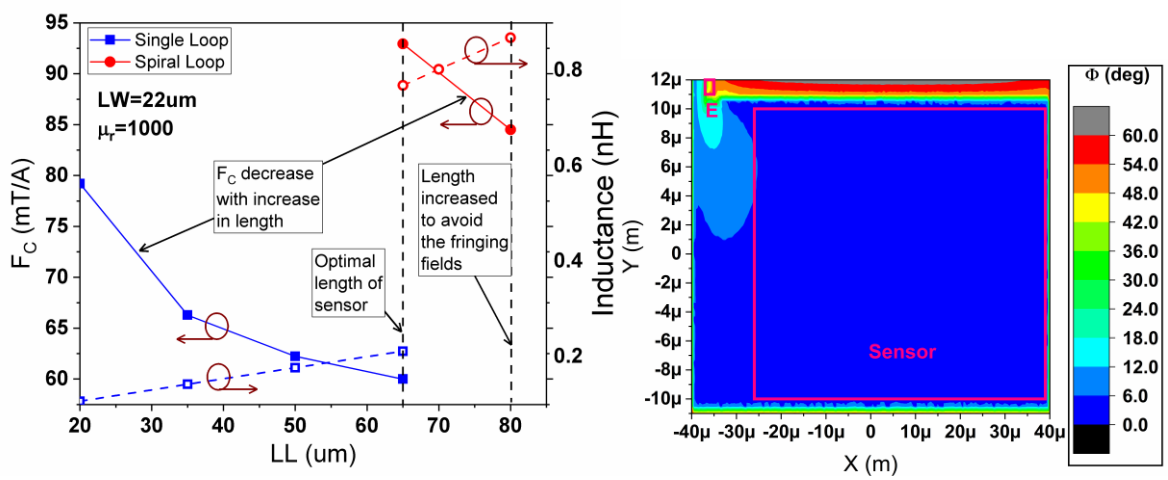

Figure 6.8: (a) The conversion factor of the single and spiral loop flux concentrators as the length is increased from 20 μm to 80 μm. (b)The contours of the angle between the B_Z and effective magnetic field above the sensor from the spiral flux concentrator. These contours reveal the proposed spiral flux concentrator generates magnetic field along the normal to the sensor as required with the angular deviation less than 6 degrees in the highlighted region.

is plotted as the distance between the spiral flux concentrator and the MagHEMT is increased up to 5 um in Figure **6.9**. The thickness of the SiN can be increased up to 2 um without degrading the F_C. Additionally, F_C remains above ~79.5 mT/A (~94% of the maximum value) even when the separation is 4um.

A comparison between the effective conversion factor, F_C, and sensitivity, S, of this work with reported literature is presented in Table 6.3. The F_C and S given in this paper show significant improvement compared to values previously reported [6.5][6.12]. The product of the conversion factor of our spiral structure (85 mT/A) with the sensitivity of the GaN MagHEMT (17.21 %/T) predicts that the presented structure can detect the currents almost 3 times smaller than the CMOS metal line structure.

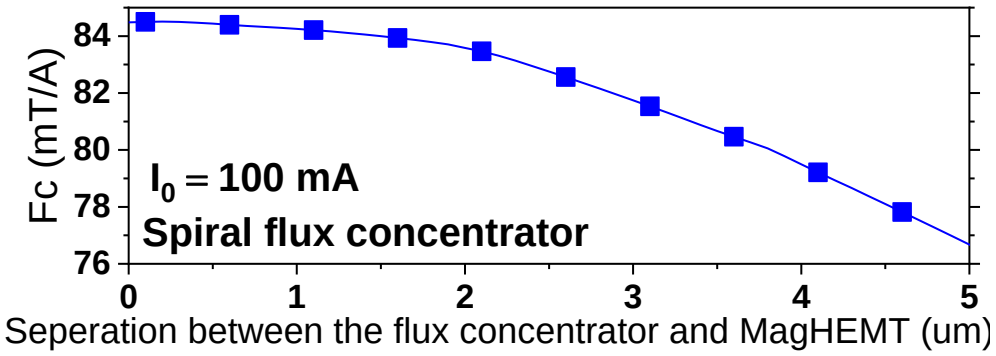

Figure 6.9: The conversion factor as the function of distance between the flux concentrator and the MagHEMT

TABLE 6.3: A compastion of the Fc, Sr and FC*Sr from this work with literature

Ref.	Technology	Structure	Predicted FC (mT/A)	Measured S (%/T)	Predicted Fc*S (%/A)
[6.12]	Si-CMOS	On-chip Metal line	4.95	--	0.5
[6.5]	Si-CMOS	On-chip Metal line	8	5.2	0.042
This work	GaN	Single Loop	58	17.21	0.998
This work	GaN	Spiral	85	17.21	1.46

6.5. Conclusion

This work demonstrates a method to improve the detection limit of a current sensor and its sensitivity in a form factor that is compact and can be easily integrated on-chip. The magnetic gain 1.8 is achieved with the permeability as low as 500 via simulations, much lower than other flux concentrators reported by simulation, requiring less stringent specifications on the magnetic material. This is mainly due to the way by which a portion of the field induced in the magnetic material is diverted into the substrate via a combination of the current conductor and the magnetic film. This combination is unsuitable for high inductance structures but works well for sensors by diverting the field into the substrate to improve the sensitivity.

6.6. References

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Chapter 7: Conclusions and Future Work

Classes J and CCF^{-1} have already illustrated their capability in achieving high-efficiency operation. Our new formulation ($B/J/F^{-1}$ continuum) developed in chapter 4 demonstrates the potential for a contiguous set of impedances between class J and continuous class F^{-1} which enables the amplifier to achieve efficiencies greater than class J. This work unlocks this design space to develop a methodology to design high-efficiency broadband amplifiers. Two amplifiers were designed using a GaN HEMT CGH40010 at the same frequency 2.6 GHz as demonstrators. It is observed that due to the feedback current flowing in the gate-drain capacitance, a set of waveforms in the class B/J continuum can achieve higher efficiency at P1dB. A simple method to calculate this waveform is presented and proved by an amplifier also. As a step towards realising a fault-tolerant PA and MMIC, we have proposed a novel on-chip flux concentration for improving the on-chip current detection capability.

7.1. Main achievements:

The major results of this thesis are summarized are:

- A new formulation which relies on the manipulation of the second harmonic of both current and voltage is developed. The second harmonic manipulation reduces the mismatch in the phases of fundamental components of voltage and current lower than in class J. A wide set of voltage and current waveforms with efficiency greater than that of class J is obtained. It is shown that the class J continuum and CCF^{-1} are special cases of the new formulation at either extreme. A major implication of the proposed continuum is a wide design space with simultaneous high efficiency and output power in comparison to CCF^{-1} or class B/J, thus easing amplifier design.
- We report the benefits of Class BJF^{-1} amplifiers, i.e., high efficiency over an intrinsically large bandwidth, and ease of design due to a wider choice of impedances available in the design space of class BJF^{-1}. The matching is performed at a single frequency to target high power and efficiency. By dividing the matching network into segments, the matching at fundamental and second harmonic frequencies is performed independently simplifying the design process. Two amplifiers designed by this method demonstrated 600MHz and 900MHz bandwidth and achieve high efficiency in excess of 72% at 2.6 GHz.
- It is observed that the linearity of a GaN HEMT decreases as the impedance at second harmonic is varied from capacitive to inductive. A study of the non-linear feedback

capacitance shows that the gain, P1dB, and efficiency at back-off power increases from class J* to class B to class J due to a variation of the phase of the voltage waveforms across its non-linear Cgd. A major implication of this is a higher PAE at P1dB than Class B (or deep class AB) without sacrificing linearity using the methodology presented here.

- This work demonstrates a method to improve the detection limit of a current sensor and its sensitivity in a form factor that is compact and can be easily integrated. The magnetic gain 1.8 is achieved with the permeability as low as 500 via simulations, much lower than reported flux concentrators in literature, requiring less stringent specifications on the magnetic material. The concept is demonstrated for loop and spiral flux concentrators.

7.2. Future work

- In Chapter 4, we have shown that the approximated voltage and current waveforms of class B/J/F^{-1} continuum can be realized in simulation for a certain power level. These waveforms need to be measured and compared with theoretical waveforms. Additionally, the realization of these waveforms required utilizing both the knee region and the non-linear capacitances of the device. The extent of the contribution of each of these effects needs to be investigated. This would eliminate the need for load-pull simulations used in this work. Also, this would provide additional insights into linearity.
- The next step is to improve the bandwidth of the amplifier by exploiting class B/J/F^{-1} continuum. The major challenge is to choose an appropriate set of impedances with frequency from class B/J/F^{-1} continuum and to design the matching network. A stepwise methodology to design a broadband matching network needs to be developed.
- Doherty configuration can be used to enhance the efficiency of the class B/J/F^{-1} amplifier at back-off power levels. The main aim is to combine the broadband potential of the continuum mode with the efficiency enhancement of the Doherty approach. The already realized class J Doherty amplifiers have demonstrated broad bandwidths. Since these implementations have utilized the class B/J continuum, the efficiencies cannot exceed 78.5%. The combination of Doherty with newly proposed class B/J/F^{-1} continuum is expected to achieve an efficiency of class F^{-1} (90 %) with third harmonic over a broad bandwidth.

- The impedance of a matching network can be made to adjust according to the applied power level via a varactor diode. This adaptive matching network can be employed along with the proposed continuum to improve the efficiency at the back-off power level. This method results in a much lower bill of materials than the Doherty architecture.
- The amplifiers designed in this work operate at frequencies less than 3 GHz. On the other hand, 5G has frequency bands at frequencies between 26 – 28 GHz. A prototype of an amplifier operating at these frequencies needs to be designed to prove the applicability of second harmonic manipulation at such high frequencies.
- The flux concentrator is analysed via simulation only in this work. It needs to be fabricated and to demonstrate its benefits in practice.