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Modelling and Control of a Grid-Connected Full Bridge Modular Multilevel Converter for Integration of Wind Energy Conversion Systems

By

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Abstract

The research work of this PhD thesis presents a performance analysis of the grid connected full bridge modular multilevel converter FB-MMC operating in the buck and boost modes, considered different levels of the dc link voltage with respect to constant grid voltage. The main objective of this research work is to analyse the influence of the ratio between the converter input and output voltages on behaviour of voltage and current harmonic components in the FB-MMC, with giving emphasis of this analysis on the 2^{nd} order circulating current, capacitor voltage ripples and THD of the phase output voltage.

The contributions of this research works involve development of the phase-shifted carriers PSC- PWM strategy through defining ac and dc modulation indexes, which allow to investigate the operation of the FB-MMC in the boost mode over a wide range the dc link voltage and to explore those of the optimal operating points. The steady-state analytical model is also developed to fully understand how the dc link voltage level influences low order harmonic components of the FB-MMC voltages and currents. The 2^{nd} harmonic circulating current and resonant inductance equations are calculated in the boost mode using this analytical model. The results of this analysis expose an optimal operating point when the FB-MMC operates in the boost mode at 60% of the nominal dc link voltage, in which the 2^{nd} order circulating current is minimized without using the circulating current suppression control, and consequently, of a decrease in the capacitor voltage ripples. As design consideration, this research work may suggest that this optimal operating point can be exploited to reduce the FB-submodule capacitor size, as the capacitor voltage ripple is considerably lowered.

A further analytical model is proposed in this research work. In particular, it is to identify high order harmonic contents of PWM voltage waveforms of the FB-MMC. Thus analytical expressions of this model are derived to describe an interaction of high order frequency harmonics and different dc link voltage levels.

Based on this analytical model, performance harmonic is evaluated using THD of the output voltage. In the boost mode, the obtained results expose a nonlinear behaviour of THD regarding different operating points of the dc link voltage. These results also reveal that the optimal dc link levels that used to achieve better THD value are highly depended on a number of FB-submodules of each arm, capacitor voltage regulation approaches and displacement angle.

Under two different capacitor voltage regulation approaches, the results obtained from both analytical models are validated to those of simulated switching models of the FB-MMC, that built in MATLAB/Simulink environment.

In addition, the main findings of this performance analysis are studied and compared using both the real-time simulation and experimentation. In which a down-scaled prototype for the single-phase FB-MMC inverter is built, and its obtained results are verified to those of a simulated switching model, that designed using a digital simulator of OPAL-RT OP4500.

Publication

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Chapter 1: Introduction

1.1 Background and motivation

In recent years, most electrical power generated depends on non-renewable resources that use fossil fuels. Thus implementing these types of fuels, by burning them to produce electricity, are predominately responsible for increasing dioxide carbon CO_2 emissions, which reaches up to 40% worldwide [1]. Consequently, many concerns can be posed significant challenges of whether climate change because of air pollution, or even concerning with an efficiency of power generation and transmission. Hence, researchers' attention in this field has been paid more for adopting renewable energy as reliable and efficient solutions used to mitigate a progression of these issues, then to reduce a negative impact of the climate change problem [2]. Presently, electrical power production is widely employed the renewable energy resources, which are also known as a clean power like wind, solar, hydro-power, etc., which yielding decrease in a fossil fuel consumption and carbon emissions reduction eventually [3]. A wind turbine system WTS is becoming more utilization among the renewable energies which intended for reducing the CO_2 emissions. The tendency towards an increase in installation of the WTS with large capacity plants in a range of MW 2. Nowadays, UK considers wind energy conversion system WECS as a viable source for producing electricity [2].

1.2 Wind energy conversion system WECS

Essentially, an amount of wind energy conversion system relies on the weather and geographic conditions, which are variable of time. Typically, wind energy conversion system WECS is a structure that used to convert the wind power into electrical power via a mechanical power system. The WECS should be designed to achieve a maximum power extraction from wind turbine generator at different operating conditions, is that to satisfy requirements of a grid integration [4], [5]. As

illustrated in Fig 1.1, a typical structure of the wind energy conversion system can mainly comprise of a wind turbine rotor, gearbox, electrical generator and power electronic converter as an interface, and then transformer for the electrical power grid integration [3], [4], [6].

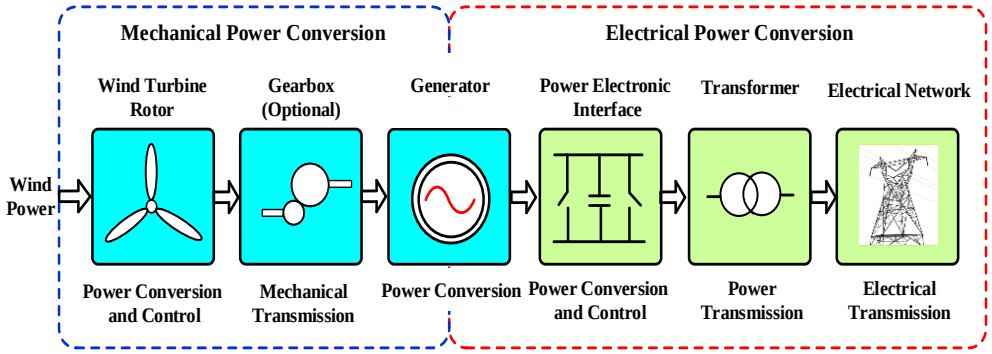


Fig 1.1 Typical structure of the wind energy conversion system

Where designed blades of the wind turbine can aerodynamically capture the wind energy, therefore, it converts into rotating mechanical power, and then into electrical power by generator unit. An operation of speed between the wind turbine and the electrical generator rotors can be matched by using the gearbox. Electrical generator rotors can be matched by using the gearbox. A power electronic converter plays a significant role in the wind conversion system. It can be used as an interface between the wind turbine system and the electrical power grid. Where, the power converter can be able to enhance efficiency and reliability for WECS regarding a variety of the wind speed [4], [5],[7], [8].

1.3 Modular multilevel converter MMC for WECS

Various multilevel converter topologies can be implemented to facilitate wind energy integration. As compared to the traditional two-level converters, they are used because of low voltage across the power electronic devices, improving output voltage quality and low switching frequency [9]. For medium voltage (MV) and the

high power converter applications such as WECS, a technical solution using multilevel converters can be classified into indirect conversion (AC/DC/AC) and direct conversion (AC/AC). Among multilevel converters, some researchers have paid more attention to use a modular multilevel converter MMC as a promising topology in the WECS. Regarding the technical solution of indirect conversion (AC/DC/AC), the MMC topologies can be used as a back-to-back BTB configuration, which provided with a common dc link. For a full bridge modular multilevel converter FB-MMC topology, it is configured using single-phase bridge submodules. Thus the FB-MMC can provide buck and boost operating modes that regards a variation in the dc-link voltage. Therefore, the FB-MMC is more suitable for WECS over others in terms of a tolerating broad range of the variations in the dc-link voltage. Here, the ac voltage can be generated independently of the dc link voltage [10].

1.4 Main objectives of the thesis

The major objectives of the research work in this thesis are to analyse a performance of the FB-MMC while operating in the buck and boost modes under varying dc link voltage. This analysis could be beneficial in making a design consideration when the FB-MMC operates in some applications such as WECS. The analysis of this research work will consider an implementation of the FB-MMC for integrating a direct drive variable-speed WECS with the power grid, whereas a time-varying of the dc link voltage is a main technical issue that impacts on WECS integration requirements. The main project goals of this thesis will be given as the following

- A review on the state of the art of existing power converters used for the PMSG based WECS will first be discussed by considering their benefits and drawbacks. And then the review will highlight why the MMC could be a competitive topology in this application as opposed to other power converters.

- Some analytical model which established to describe an operation of the MMC under dynamic and steady states will be introduced in the literature review. Furthermore, some comprehensive analyses published to identify high order harmonic contents of the PWM voltage waveforms will be reviewed and discussed.

- Basic structure and principle operation of the MMC based on full bridge submodules will be studied.

- Design of the single-phase FB-MMC model built in the MATLAB/Simulink environment will be considered. Based on a phase-shifted carrier PWM strategy, this simulated switching model of the FB-MMC will be used to define modulation indexes, which allow to specify the buck and boost modes. This model will also be used to explore a range of these modulation indexes when the FB-MMC operates over a full range of the dc-link voltage.

- This simulated switching models of the FB-MMC will be utilised to fully understand how different dc-link voltage levels in the boost mode influences 2^{nd} order harmonic-circulating current, capacitor voltage ripples and THD of the phase output voltage. The analysis will be carried out under two different capacitor voltage regulation approaches

- As further preparation for performance analysis, the simulated switching model above will be developed to the grid connected FB-MMC based on the three-phase system. In this research work, a design of two closed-loop control circuits for the grid connected FB-MMC will be optimized that considers a synchronous sampling technique. The first control circuit is to achieve active and reactive powers, while the second control circuit is to regulate the dc capacitor voltages of each FB-SM and to minimize the 2^{nd} order circulating current. An impact of the second control circuit on the 2^{nd} order circulating current and the capacitor voltage ripples will be investigated when FB-MMC works at the boost mode.

- In this research work, the steady-state analytical model of the FB-MMC will be developed regarding the operation in the buck and boost modes. This analytical model is necessary to fully understand the behaviour of low order harmonic components in voltages and currents, in which the dc link operates at different voltage levels. For this purpose, analytical expressions describing the 2^{nd} harmonic circulating current and capacitor voltage ripples can be derived and validated though the single-phase simulated model in the open-loop mode.

- A comprehensive analysis to identify high order harmonic contents for PWM voltages of the FB-MMC will be developed in this research work. This analysis undertaken is to realise how different levels of the dc link voltage mainly influences the behaviour of high order harmonic contents in the buck and boost operating modes. By using the harmonic spectrum form, harmonic content amplitudes resulted from this comprehensive analysis will be verified with FFT results of a simplified simulated model of the FB-MMC.

- Modelling of the FB-MMC using a real-time simulation will also be presented in this research work. Based on the single-phase system, this simulated switching model as an inverter will be executed in the real-time to verify main concepts of the FB-MMC at the buck and boost modes of operation. This simulated switching model will be designed in MATLAB/Simulink interfaced with the RT-LAB software. While the implementation of this simulated switching model of FB-MMC will be carried out using OPAL OP4500 simulator. A down-scaled prototype for the single-phase FB-MMC inverter will also be built in this research work. The results obtained from both the real-time simulation and experimentation will be studied and compared under these operating conditions.

1.5 Limitations of the research work

The main limitations of this project can be given as the following:

- The experimental prototype of the FB-MMC based on the single-phase system is only configured with four submodules, that related to the cost and complexity.
- The capacitor voltage balancing control of FB-MMC is not implemented whether off-line simulation, real-time simulation or experimentation circuit.
- A dynamic state condition of FBM-MC is not analyzed
- No-fault or unbalance conditions are undertaken in this study

1.6 Organization of the thesis

The research work of this thesis is organized as follows:

- Chapter 2 first presents a literature review on feasible configurations of WECS implementing power converters. The review emphasises on some existing power converter topologies including MMC and then discusses their benefits and drawbacks when using in a variable speed WESC based on a full-scale power BTB converters. The literature review in this chapter introduces some analytical modelling for the MMC, which were established to describe the behaviour of voltage and current components of the MMC in the dynamic and steady-state conditions. Furthermore, some comprehensive analyses published to identify the harmonic contents of the PWM voltage waveforms are reviewed and discussed.

- Chapter 3 describes a PWM modulation strategy based on the phase-shifted carriers PSC-PWM and defines modulation parameters, which can be used to specify the operation of the FB-MMC in the buck and boost modes under varying dc link voltage. As preparation for the FB-MMC analysis, a simulated switching model of the single-phase FB-MMC is first provided that to explore the influence of the dc link voltage on the 2^{nd} harmonic circulating current, capacitor voltage ripple and THD of the output voltage. The FB-MMC simulated switching model is then extended to three-phase system. Control circuits that required for the grid connected FB-MMC based on the three-phase system are analysed.

- In Chapter 4, a steady-state analytical modelling for the FB-MMC is developed. By setting different levels of the dc link voltage of the FB-MMC, the analytical expressions are derived to describe the impact of the operation in the buck and boost modes on in low-frequency ripple components which are: arm current, submodule capacitor current, submodule capacitor voltage, submodule output voltage, arm voltage, and phase output voltage of FB-MMC. Furthermore, the amplitude and phase angle are calculated for the second harmonic circulating current. The simulation results are validated for switching and analytical models of the FB-MMC.
- Chapter 5 proposes a comprehensive analytical modelling to identify the harmonic contents of PWM voltage waveforms on the FB-MMC. As the converter operates in the buck and boost modes, this analysis is first established to fully understand the interaction of high order frequency harmonics that regards different dc link voltage levels. The comprehensive analytical modelling of the FB-MMC is then evaluated by comparison with the FFT analysis of the switching model simulation results.
- In Chapter 6, real-time simulation of the single-phase FB-MMC model is built and executed, that is to verify the main findings of the converter proposed in Chapter 4 and 5. In this chapter, designing FB-MMC model considers a methodology technique of the electrical hardware solver eHS. The CPU and FPGA platforms of the real-time simulator of OPAL OP4500 are first used to configure the real-time simulation model. A down-scaled prototype for the single-phase FB-MMC is then built, and OP4500 simulator is exploited to generate PWM signals of IGBT devices of the FB-MMC. By considering open-loop testing, results obtained from experiments are verified to those of the real-time simulation at the same operating points.
- In Chapter 7, it gives summaries and conclusions on the presented research work of this thesis. Also, future works are suggested.

Chapter 2: Literature Review on Using Power Converters for Wind Energy Conversion system

2.1 Introduction

A literature review in this chapter presents on the topics of this research work. The first section in 2.2 introduces the main configurations of wind energy conversion systems WECS. It focusses on variable speed WECS with a full-scale power converter. In section 2.3, the review provides insight into most common power converter topologies which implemented into a direct drive of multi-poles permanent magnet synchronous generator PMSG based WECS. In this section, benefits and shortcomings of reviewed power converters, particularly MMC, are also discussed, as they are configured with back to back BTB converters. For maximum power point tracking MPPT algorithms published, they are given in according to the direct drive of PMSG based WECS. Basic operation principles of the FB-submodule based MMC is detailed in section 2.4. In section 2.5, it presents a literate review on some analytical model for MMC in the time and frequency domains. The reviewed modelling of MMC deal with dynamic and steady states to describe voltage and current components in low frequency for different applications, such as WECS, HVDC, and machine drives. Lastly, section 2.6 presents a further literature review on the analytical model of MMC, which established to identify the harmonic contents of the PWM voltage waveforms. Comprehensive analyses in this literature review mainly emphasis on identification of high-frequency harmonic contents existed in voltages of MMC. This review also discusses two pulse width modulation strategies adopted in these comprehensive analyses, namely level-shifted carries LSC-PWM and phase-shifted carries PSC-PWM, that is to evaluate voltage level generated and total harmonic distortion of MMC output voltage.

2.2 Feasible Configurations of Wind Energy Conversion Systems

This section presents a literature review on feasible technical solutions which using a power converter for wind energy conversion systems WECS. Whereas they are employed to improve integration between the wind turbine generator and grid system under different operating conditions [11]. These technical solutions, which have to satisfy both generator and grid side requirements, can be categorised into fixed speed wind energy system and variable speed wind energy system [11], [3], [12]. The fixed speed wind energy system was proposed in the 1980s [13]. A configuration system consists of an asynchronous squirrel cage induction generator SCIG with a soft starter using thyristors, as shown in Fig 2.1. Here, the wind turbine generators are directly connected to the power grid via step-up transformers. Thus they can be operated with a rotor speed variation of < 1 %. A bank of shunt capacitors is required to provide the reactive power compensation, that is to achieve a unity power factor. By using SCIGs, attractive solutions can be provided, such as simple construction, low cost. A smooth grid integration achieves by connecting the soft starter without synchronisation equipment. Otherwise, the main drawbacks are: it does not have a speed control system. Thus, it needs a stiff grid for stable operation and reliability, and the high mechanical stress caused by wind torque pulsation.

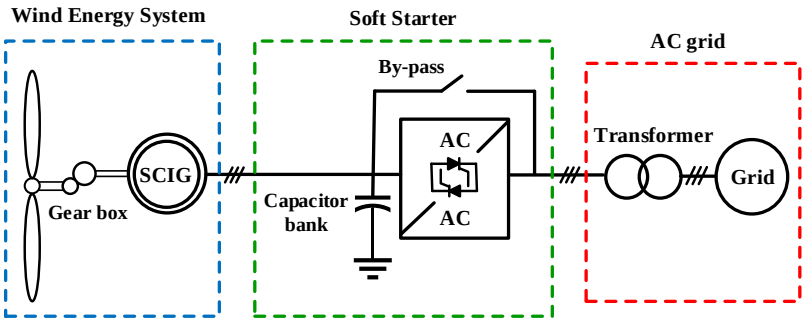


Fig 2.1 Fixed speed wind energy system using the soft starter converter

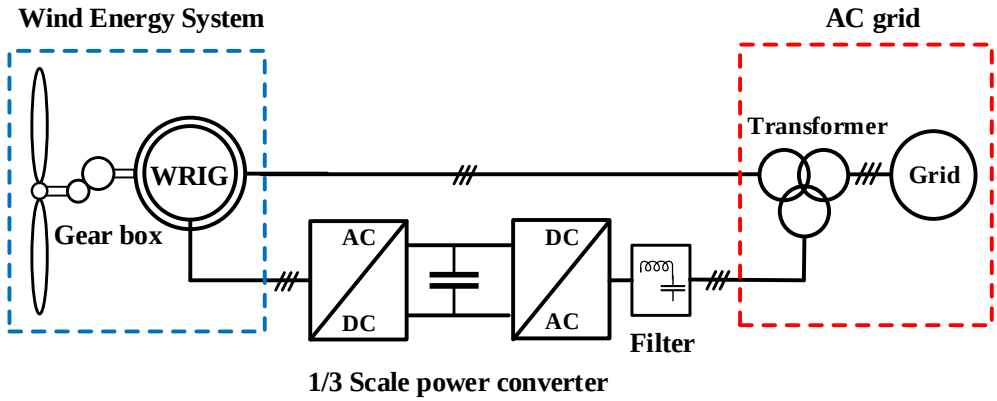


Fig 2.2 Variable speed wind energy system based on the partial scale power converter

However, the variable speed wind energy system has many features as compared to the fixed speed wind energy system, which is lower in mechanical component stress, such as a gearbox and a shaft due to the variability of the wind speed and torque. Furthermore, producing maximum power output with less fluctuated power may be injected into the network [12]. This literature review presents two main configurations of the variable speed wind energy system, a partial scale and full-scale power converters. In modern WECSs, these variable speed configurations are implemented to maximise power energy captured from the wind. They can also achieve control of the active and reactive power under all operating conditions. The partial scale power (frequency) converter, which is also called a Doubly Fed Induction Generator DFIG, has been presented in [3], [12], [14], [15]. It can give a partial variable speed with a wound rotor induction generator (WRIG). In this configuration, the power grid is connected to the generator stator directly. While the rotor is integrated into the grid by ac/dc/ac power electronic converters via slip rings, as shown in Fig 2.2 [11]. The rotor speed (slip) can be varied by the partial scale power converter (frequency converter) control. Using a back to back BTB converter, the generator rotor can transfer an output power of 1/3 to the grid as compared to its stator. The BTB converter is also used to compensate the reactive power, and to perform the soft grid interconnection. The main feature here is that the generator can feed energy to the gird at sub-synchronous and super synchronous.

Besides a presence of slip rings, another main drawback of this configuration is limited controllability with a protection system during a fault in power grid, as the stator is directly connected to the grid [11],[3],[12]. However, another configuration of variable speed WECS based on the full-scale power converter can be employed, as shown in Fig 2.3. The generators employed can be the squirrel cage induction generator SCIG, wound rotor synchronous generator WRSG and permanent magnet synchronous generator PMSG. They are smoothly connected to the grid through full-scale power BTB converters and transformers [11], [3]. The generator side is interfaced to the ac-dc converter, which allows handle generator output power under a wide range of speed and to perform at unity power factor, while the dc-ac converter interfaced with the grid side can be used to provide active and reactive power conversion and to maintain the capacitor of the dc link voltage constant.

For a variable speed WECS which using a multi-pole permanent magnet synchronous generator PMSG, the wind turbine here can be directly coupled to the BTB power converter without using a gear-box, or gearbox size required can be reduced. The variable-speed WECS based on direct drive PMSG has better features over other types. For instance, operating at low speed with gearless can increase in the reliability of the WECS. Furthermore, a self-excitation ability of the PMSG can improve the efficiency of the operation at high power factor [4], [16], [17].

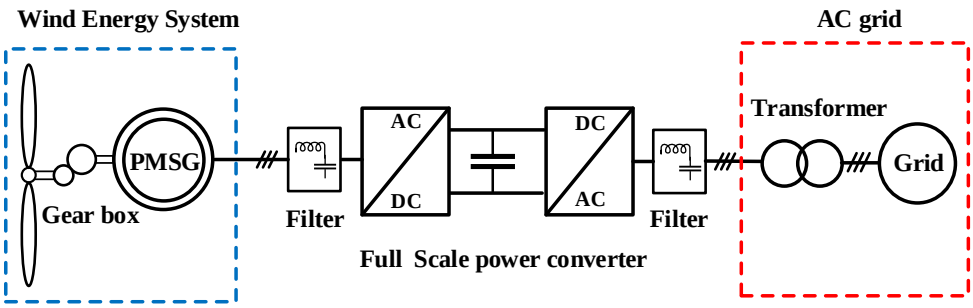


Fig 2.3 Variable speed wind energy system based on the full-scale power converter

2.3 Review on the state of the art of power converters used for the PMSG based WECS

Many topologies of the power converters can be utilised to interface the wind turbine equipped with PMSG to the grid system. The main objective of these topologies is to achieve both the wind generator and power grid side requirements in terms of high efficiency, less cost-effective and more reliable with a simple maintenance solution [18]. In addition, they should be able to control active power and to compensate the reactive power, that is to fulfil the grid codes regardless of the wind speed variation [1], [19]. In the generator side, the power converter should be able to capture maximum power from the wind generator under variable output voltage and frequency values [18],[1]. However, output voltage and frequency of the power converter in the grid side should be synchronised to the grid. A topology used in the BTB configuration can be included two or multi-level converters either in the back end (generator side) or front end (grid side). Therefore, some of the power converter topologies used are reviewed and discussed in the following sections.

2.3.1 Implementing two-level converter into PMSG based WECS

The most common topology employed to interface direct drive of PMSG based WECS with the gird is the back to back two-level voltage sourced converter as illustrated in Fig 2.4. In the generator side, maximum wind energy can be captured by voltage sourced rectifier VSR. The voltage sourced inverter VSI can control the active and reactive power and maintain the dc link voltage constant. Even though this converter has a simple structure with six switches topology for both sides, it may suffer from a high voltage stress dv/dt in high power medium voltage applications. Moreover, large size filters can be needed to comply with gird system requirements in terms of better total harmonic distortion [3], [20], [21].

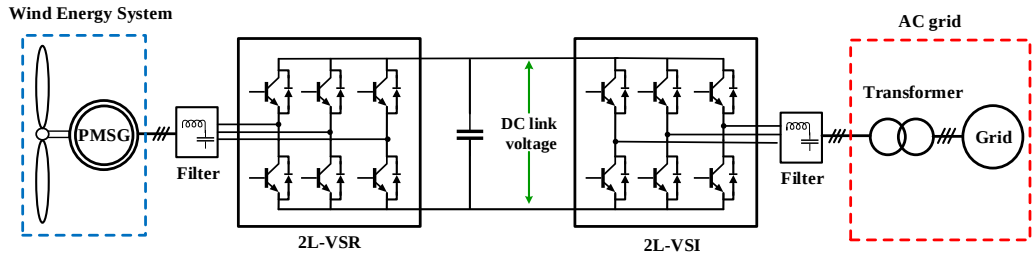


Fig 2.4 Configuration of direct drive PMSG for WECS using two-level BTB converter

In a semi-controlled with the BTB converter are shown in Fig 2.5. Compared to the former converter topology, a low cost-effective solution and well reliability can be obtained that by replacing a three-phase six diodes instead of a two-level VSR. This topology is composed of diodes rectifier, dc-dc booster converter and two-level voltage source inverter. Where it can rectify the wind generator output by an uncontrolled diode rectifier, hence the dc link voltage will vary as the wind speed changes due to the weather conditions. In this case, the dc-dc boost converter is used to regulate the dc link capacitor voltage steadily and to achieve a maximum power point tracking MPPT [22]. Because the reactive power is not required in such a PMSG, this converter topology transfers uni-directionally the active power to the power grid system based on the voltage sourced inverter VSI, [4], [8], [16], [10], [23].

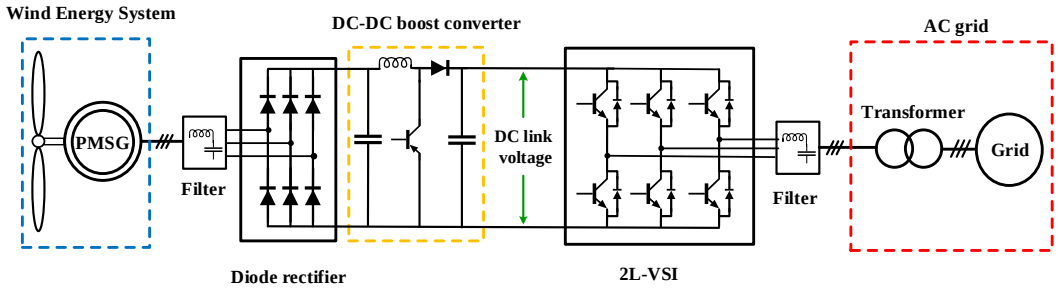


Fig 2.5 Configuration of direct drive PMSG for WECS using diodes rectifier, dc-dc booster converter and two-level voltage source inverter

2.3.2 Implementing multi-level converter into PMSG based WECS

In comparison with the conventional two-level converters, the multilevel converter topologies can achieve a high number of the output voltage levels. Therefore, smaller filter size is needed as the output voltage waveform quality is enhanced. Also, voltage stress across power electronic devices of the converter is reduced. The multilevel converters can be used as a technical solution in high voltage systems. Fig 2.6 shows a neutral point diode clamped NPC multilevel converter utilizing for direct-drive PMSG based WECS, as presented in [11], [4], [16], [18], [24], [25]. This topology is constructed from the BTB converter to meet the requirements of the gird integration. The advantage of 3L-NPC is that one more level can be implemented as compared to 2L-VSC [4], [11]. In this case, zero voltage level can be obtained by connecting a midpoint of the IGBT switches to the converter neutral point through clamping diodes. Nevertheless, the main drawback of this topology is that dc link capacitors suffer a voltage fluctuation due to asymmetrical loss distribution among switching devices. Therefore, a control circuit is required to balance the dc link capacitor voltage of this topology.

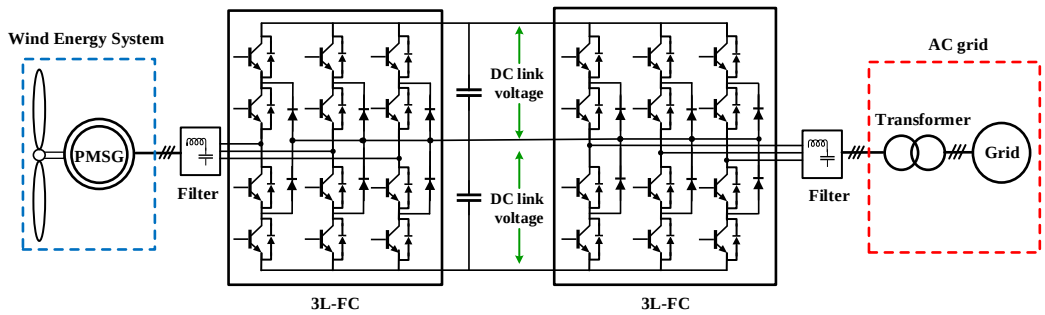


Fig 2.6 Configuration of direct drive PMSG for WECS using back to back neutral point diode clamped multilevel converter

However, the topology of the flying capacitor FC multilevel BTB converter can also be incorporated with the direct drive of PMSG for WECS. Fig 2.7 presents three

levels FC converter. Similar to the NPC, the capacitors in the FC converter are used to synthesise the output voltage levels regarding switching states. The FC converter level can easily be extended if compared to NPC. The main shortcomings of this topology have bulky capacitors, and implementation of capacitor voltage balancing control is much more complicated. Moreover, these capacitors require for pre-charging to get the same voltage level [4], [16], [25].

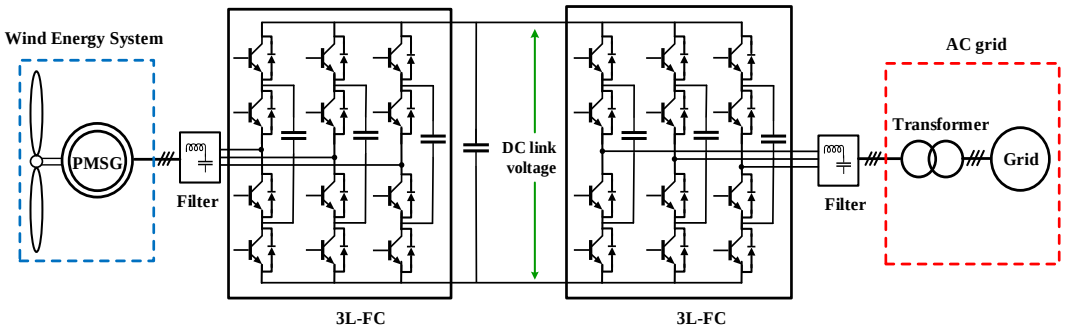


Fig 2.7 Configuration of direct drive PMSG for WECS using back to back flying capacitor multi-level converter

2.3.3 Implementing modular multilevel converter MMC into direct drive PMSG based WECS

The modular multilevel converter MMC is first proposed by Marquardt and Lesnicar in 2004 [26]. The state of art of the MMC topologies is considered in [27], [28]. The MMC can be an attractive solution for the high power medium voltage applications such as WECS, and HVDC-grid system. This section highlights why the MMC is possible to be a competitive topology in WECS, as opposed to the standard two-level voltage source converter. In general, the configuration of back-to-back BTB voltage source converters is widely employed in the WECS. The two-level BTB voltage source converters based WECS is shown in Fig 2.4. In order to increase the operating voltage of the two-level voltage source converter, a series connection of IGBT devices can be utilised to realize one device [29], [30]. If this technical solution is adopted, the two-level voltage source converter can be able to

block any level of the dc link voltage converter. The main limitation of this approach is a capability of withstanding voltage steps at a high switching frequency up to 2 kHz [31]. Besides, the use of IGBT devices connected in series may result in more complexity to the system. That could impose some static and dynamic problems within the operation of the two-level voltage source converter. However, as the modular multilevel converter MMC can offer a more attractive technical solution, it has become a most competitive candidate in WECS and HVDC applications. The MMC has composed of a series connected submodules. That can allow a device switching frequency in the MMC to be reduced, in comparison with the two-level voltage source converter. Consequently, of a low voltage stress dv/dt across IGBT device, and a decrease in THD of the output voltage under the same switching frequency. In addition, an increase in efficiency of the MMC due to the reduction in the device switching frequency [29], [32]. Other MMC features can also be summarised as the following:

- Usage of submodules connected in series can bring more benefits such as modularity designed and simplicity of voltage scaling, which allow the MMC to meet any voltage level requirement.
- More reliability can be obtained, as the redundancy operation is realized.
- A decrease in harmonic contents of the output voltage makes the AC filtering stage requirement less, thus cost installation can be reduced.
- In medium voltage high power conversion, the MMC can directly be connected to the grid without using a transformer.
- Short circuit current in the dc link of the MMC can be limited by the upper and lower arm inductors.

Nevertheless, the main limitations are that high numbers of the power electronic devices and capacitors are required to design the MMC submodules. Also de-rated converter power because of the circulating current which generated in the dc side of

the converter. Additionally, the control circuits of the MMC can increase complexity, that because an individual capacitor voltage balancing control is required [9], [20], [32], [33].

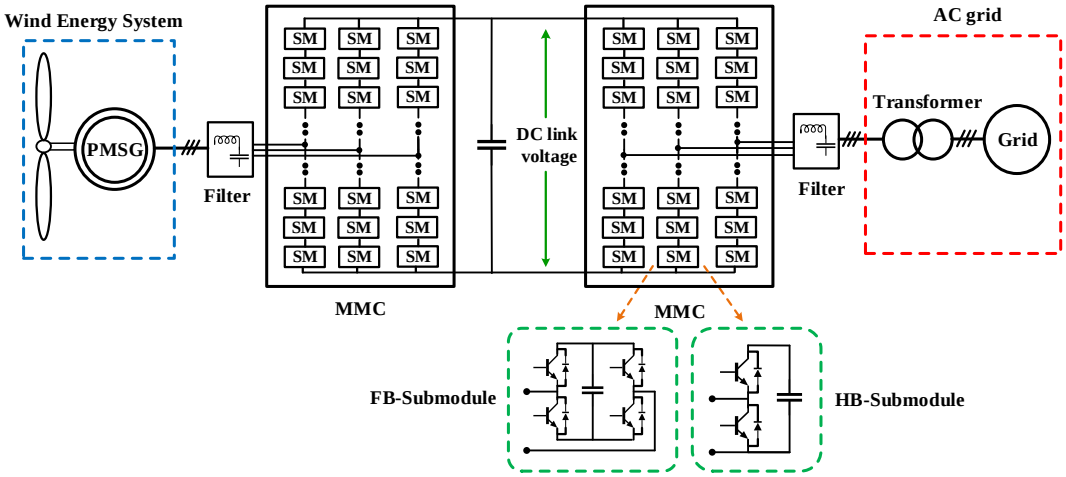


Fig 2.8 Configuration of direct drive PMSG for WECS using back to back modular multi-level converter

The MMC can be constructed with a high number of half bridge or full bridge submodules, as illustrated in Fig 2.8 [28]. As compared to the FB-MMC, an implementation of the HB-MMC can offer lower cost-effectiveness and less expensive in the HVDC-grid systems. However, the FB-MMC can operate in both buck and boost modes, as reported by Akagi in [10]. These attractive features would be exploited to interface direct-drive PMSG for WECS, in which the dc link voltage may vary by the wind speed. As the generator is equipped with multipole PMSG, higher power factor and more efficiency can be obtained from this WECS while operating in low speed, and the generator frequency here is typically in the range of (5-20) Hz [4], [7], [34], [10]. Hence, the reactive power exchange is not required. In the case, it gives the possibility of replacing the MMC in the generator side by a six-pulse diode rectifier as shown Fig 2.10, which can lead to reduce in the cost and increase WECS efficiency and reliability [10]. For maximum power point tracking MPPT algorithms, three methods are proposed to be in use for the direct-driven

PMSG based WECS, including power signal feedback PSF control [35], [36], hill-climb search HCS [37] and tip speed ratio TSP control [38].

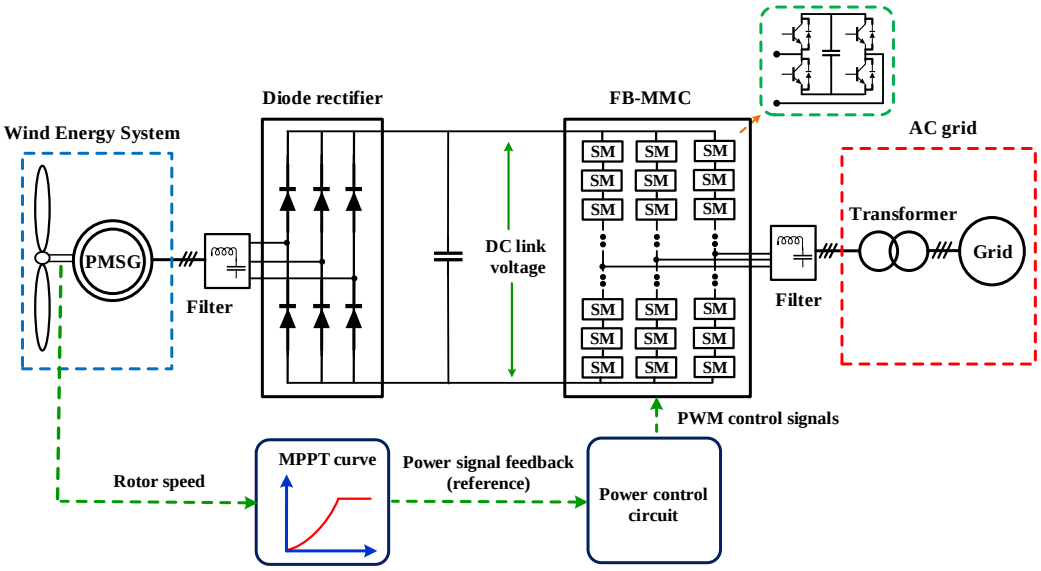


Fig 2.9 Direct drive PMSG based WECS using diode rectifier and full bridge modular multilevel converter

However, this study in chapter 3 shows that the possibility of implementing the MPPT algorithm using the PSF. In this control method, a power reference signal can be given using the MPPT curve, in which a rotor speed (or wind speed) is set as the input [6], [39], [40]. Note that the MPPT curve can be obtained from an equation of the optimum output power versus the wind speed. The study is brought to demonstrate the behaviour of the grid connected FB-MMC, that when applied to the configuration of the direct drive of PMSG based WECS as explained Fig 2.10.

2.4 Structure and operation of FB-submodule based MMC

The basic structure of each FB-submodule FB-SM is composed of four IGBT switches with anti-parallel diodes. They are in parallel connection with a submodule capacitor C_{SM}. The main switches of FB-SM are T_1 and T_3, which operate with auxiliary switches T_1 and T_3 in a complementary manner. The freewheeling diodes for these switches are D_1, D_3, D_2 and D_4, respectively, as illustrated in Fig 2.10. Regarding the switching combinations, the FB-submodule can be inserted either at

positive or negative voltage states and bypassed at zero voltage state in any arm current direction [41], [42]. As given in Table 2.1, it is assumed that On and Off switching states of the IGBT switches are represented '1' and '0', respectively. For a case of the IGBT switches T_1 and T_4 are On-state and T_2 and T_3 are Off-state. The output voltage V_{SM} of the FB-SM is inserted at a positive voltage state. Here, the submodule capacitor is charged when the arm current flows in th positive direction $i_{arm} > 0$. While the capacitor is discharge if this current direction is $i_{arm} < 0$. However, when the IGBT switches T_2 and T_3 are On-state and T_1 and T_4 are Off-state. In this case, the positive arm current direction $i_{arm} > 0$ discharges the submodule capacitor.

Table 2.1: Possible switching combinations related to the output voltage, current path direction and capacitor state of the FB-submodule

Switching state					Output voltage V_{SM}	Arm current		Submodule Capacitor state
	T_1	T_2	T_3	T_4		direction	path	
(a)	1	0	0	1	$+V_C$	$i_{arm} > 0$	D_1, D_4	charging
(b)	1	0	0	1	$+V_C$	$i_{arm} < 0$	T_1, T_4	discharging
(c)	0	0	1	1	0	$i_{arm} > 0$	T_3, D_4	uncharge
(d)	0	0	1	1	0	$i_{arm} < 0$	D_3, T_4	uncharge
(e)	1	1	0	0	0	$i_{arm} > 0$	D_1, T_2	uncharge
(f)	1	1	0	0	0	$i_{arm} < 0$	T_1, D_2	uncharge
(g)	0	1	1	0	$-V_C$	$i_{arm} > 0$	T_2, T_3	discharging
(h)	0	1	1	0	$-V_C$	$i_{arm} < 0$	D_2, D_3	charging

Otherwise, this capacitor is charged for the negative arm current direction $i_{arm} < 0$. Moreover, there are four possible switching combinations where the FB-SM is bypassed at zero voltage state. Of note that the submodule capacitors need to be pre-charged at a rated voltage, which allows to produce the desired voltage at the MMC output [43],[44], [45]. Thus a pre-charge control is an important process to realize the safe operation for the MMC with smoothly starting up, particularly in HVDC applications. Otherwise, improper charging capacitors may damage to submodule components, as a result of unbalanced capacitor voltages [45].

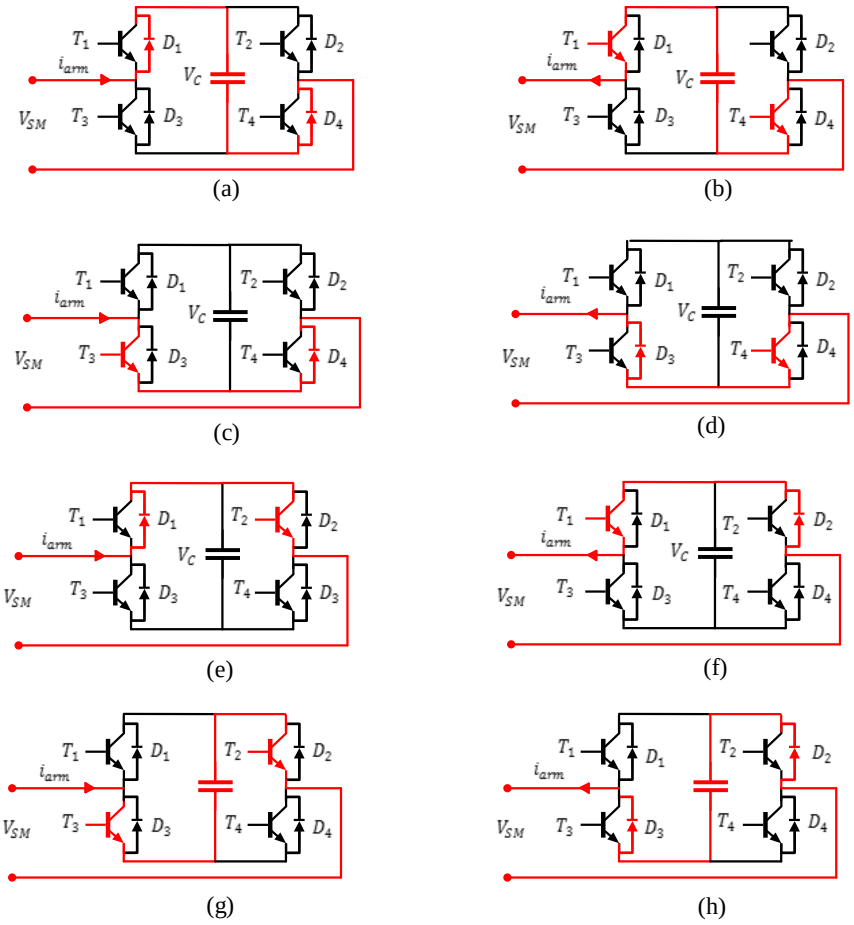


Fig 2.10 Current path direction in the FB-submodule while operating at different switching combinations

The conventional pre-charge control can be classified into two stages: uncontrolled pre-charging and controlled pre-charging. In the first stage, all submodule capacitors are charged equally through the free-wheeling diodes of the submodules, that by using the dc voltage source; however, capacitor voltage levels are insufficient to operate of the MMC at the desired output voltage. In the second stage, the controlled pre-charge is used to charge submodule capacitors further to their rated voltage. It can be achieved by controlling the rest energy, which flows from the AC side of the MMC [46], [47], [48].

2.5 Steady-state analysis modelling for MMC

This section presents a literature review on some of the analytical models which proposed to describe a behaviour of electrical quantities for MMC regarding

different operational conditions. Many efforts were introduced various analytical modelling for MMC in the dynamic and steady states, that would be valuable to optimise the converter parameters in terms of the submodule capacitors and arm inductors sizing. Also, the analytical modelling can be used to show an impact of second harmonic circulating current and to develop controller circuits for MMC. For the dynamic- state, the first models for MMC have been revealed in [26], [49]. Based on HB-MMC topology, these models were configured simply without arm inductors. Thus, influence a circulating current, which flows through upper and lower converter arms, was not made explicit in these model, as shown in Fig 2.11 (a). In reference [50], this model has been modified by inserting an inductor in each arm, that is used to regulate and shape the circulating current, as shown in Fig 2.11 (b). It noted that an assumption in these models was not accounting for submodules interaction in both MMC arms. Thus, all the submodules in each converter arm are represented as a controlled voltage source associated with only line frequency.

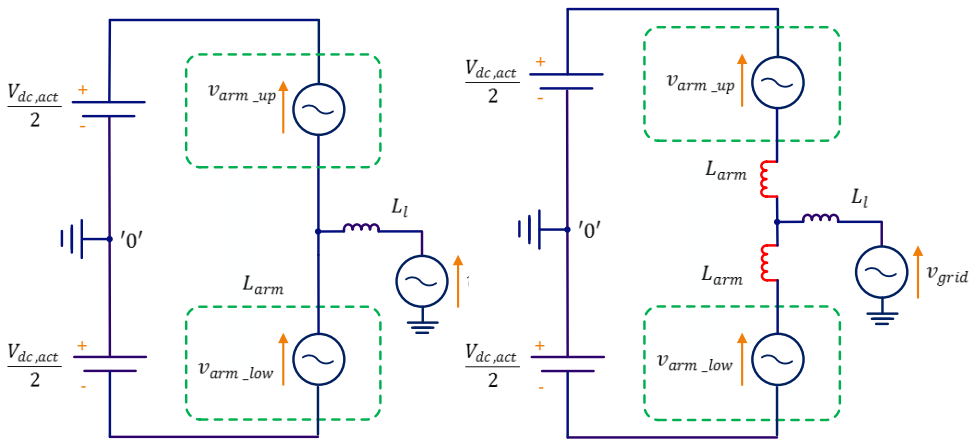


Fig 2.11 Modelling of MMC based on the single-phase system, (a) when arm inductors not introduced, (b) when arm inductors introduced

Based on this modelling, an instantaneous power analysis in the MMC arms was introduced in [51], [52]. It pointed out that asynchronous fluctuations of the submodule capacitors may cause the circulating current as a negative sequence

component. For a large number of the submodule, another MMC modelling using an analysis of the energy stored has been developed in [53], [54], [55], that model allows to reduce control circuits complexity. The difference is that a variable (nonlinear) capacitance is used to represent each converter arm, as illustrated in Fig 2.12. This model is useful to determine a voltage of each HB-MMC arm by estimating the total stored energies in MMC leg. A balance controller in this approach is proposed to mitigate the circulating current and to balance the capacitor voltage of submodules, whereas this controller depends on the difference between the energies in the upper and lower converter arms.

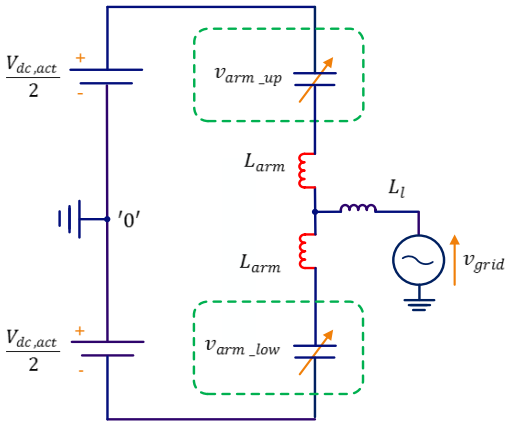


Fig 2.12 Modelling of MMC based on the single-phase system when converter arm introducing as variable capacitors

A detailed modular multilevel converter in high voltage levels was also modelled in [56], [57], that to describe a dynamic response behaviour. This nonlinear model was based on an average value to replicate a response for the switching devices and control circuits of this converter topology. This approach is only valid to simulate MMC transient behaviour in the time domain. Due to the difficulty of evaluation of the harmonic propagation in the time domain, HB-MMC analytical model was employed in the frequency domain in [58]. That is to fully understand the behaviour of harmonic contents in the arm currents and submodule capacitance voltages. This model would be convenient for HB-MMC operating in the

rectification and inversion modes. For HVDC system applications, a proposed decoupled α-β model for the modular multilevel converter has been presented in [59]. In this modelling, a state plane analysis based on the power flow is used to identify the circulating energy associated with the load, source, and capacitor ripples in the arm of the converter. This approach can be used to reduce voltage ripples across submodule capacitors for both HB-MMC and FB-MMC topologies. In order to satisfy the parameters design and power flow analysis, a new MMC phasor model was established in [60]. This model with high order was firstly derived in a *d*-*q* reference frame accounting for the circulating current. Also, this study has modelled the circulating current suppression control of the second-order harmonic. An additional phasor model has been reported in [61], that achieves an analysis of small-signal stability. A linear state-space model associated with multivariable approach was firstly discussed in [62], that is to deal with complexity caused by increasing in the voltage levels (with the high number of IGBT switches). A harmonic linearization modelling approach was reported in [63], [64], that captures internal dynamic features due to harmonics of the circulating current and ripple capacitor voltage. Because these quantities can affect on the stability of the HB-MMC, analytical impedance model in the ac side of HB-MMC is utilised to improve small signal stability for the wind energy integration system, in whether to apply for the time domain or the frequency domain [65]. Energy stored in legs of MMC was also derived in [66] for an optimal parameter design, that by taking into account the arm inductors and the submodule capacitors. Thus mathematical formula has been derived that to identify a relationship of the arm inductance value related to a magnitude of the circulating current.

Based on a steady-state analysis; however, other analytical approaches to evaluate the properly harmonic performance of HB-MMC have been introduced in [67], [68], [69]. In these analytical studies, the impact of a controller uses to suppress the circulating current was not considered. The expressions published in [67] are useful to describe interactions among voltage and current harmonic components in

the HB-MMC. The derived equations indicated that the circulating current, which exists in the upper and lower converter arms, may contain harmonics of odd and even orders. The [67] also introduced that the second harmonic of the circulating current is still dominant. By considering different resonant frequencies, a new criterion is identified to select optimal values for the arm inductance and submodule capacitance as well. A steady-state analytical model for HB-MMC has been established in [68] that considers an average model schematic, as shown in Fig 2.13. The analytical model obtained is proven by simulation and experimental results. Based on a circular interaction, the analytical model equations were derived that is to understand the relationship among voltages, currents and their harmonics. Thus, explicit equations for the magnitude and phase angle of the circulating current (2nd order harmonic) were also deduced. These analytical expressions would be sufficient for HB-MMC connected to the grid application, in which arm inductance value is set to be a few times more than resonance inductance of a double line frequency.

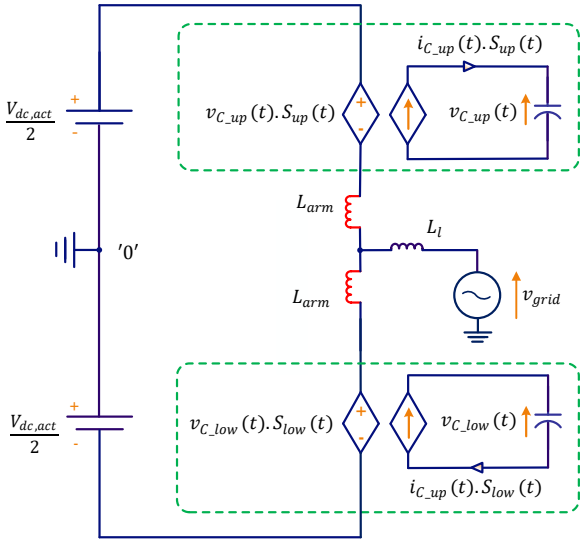


Fig 2.13 Average model representation of the single-phase MMC

The steady-state analytical model established in [68] has been extended depending on the reference model [69], that develops HB-MMC model to be suitable for the machine drive applications. In this case, derived equations included an impact

on the circulating current with both 2nd and 4th order harmonics to HB-MMC performance. Optimal values of the circulating current harmonics were obtained using the particle swarm optimisation algorithm, and then they were injected into converter arms to minimise voltage ripples across submodule capacitors. The steady-state analytical model of HB-MMC in [68] was developed in [70], [71] that considers the influence of 2nd order circulating current control. The analytical equations obtained from these models propose an optimal 2nd harmonic voltage reference that injected into the control circuit. That leads to reduce a voltage ripple across submodule capacitors. In HVDC applications, another proposed steady-state model was recently published in [72], which is achieved to improve a calculation of harmonic component amplitudes for voltages and currents in arms and submodules of HB-MMC. An iteration algorithm was adopted in this new model to calculate these amplitudes. This enhanced model was also compared to other previous models in terms of achieving more accurate sizing for the submodule capacitors. A generalised dynamic model of MMC was published in [73], that is to simplify a converter controller design and simulation results, whereas the proposed schematic is valid for single or three-phase MMC analysis. A switch model terminal behaviour for MMC was deduced in [74], [75] based on the former modelling. By using a schematic of the average model, three-phase controlled voltage sources are represented in the *abc* coordination. While controllable current sources are performed to charge the capacitor in each submodule, that represents a fluctuation of each capacitor voltages when reflected on the controllable voltage source.

For the FB-MMC model, a steady-state analysis was proposed in [128], [76] that considers at the fixed level of the dc link voltage. These study utilized both positive and negative voltage states generaed by FB-SMs, that is to reduce both fundamental and second-order voltage ripples across the FB-SM capacitor. The optimized design in this model was utilised for HVDC transmission system. By considering an analysis method published in [77], the reduction in capacitor voltage ripples of the FB-MMC was also achieved using positive and negative voltage states

of FB-SMs combined with the 2nd order-circulating current injection. Hence, an ac voltage boosting under the nominal value of the dc link voltage requires to increase the modulation index up to 1.414. Another steady-state analysis of the FB-MMC was introduced in [78]. Under various operating conditions, it revealed that the reduction in the voltage ripples that utilises both positive and negative voltage states are strongly related to angle of power factor. A reduction in energy storage requirement are analysed in accordance with variations in the number of FB-SMs.

By considering the aforementioned literature review, the steady-state analysis methods, particularly the FB-MMC topology, were established to operate the converter under the nominal value of the dc link voltage. Hence, the analytical expressions derived in these analyses would not be adequate to describe a behaviour of voltage and current harmonic components, in which the FB-MMC works at the buck and boost modes. Thus this study proposes and develops a steady-state analysis of the FB-MMC considering the influence of the variations in the dc link voltage, which operates at equal and lower than its nominal value. Analytical expressions of voltage and current harmonic components on the FB-MMC are derived that considers the operation in the buck and boost modes. Besides, an amplitude and phase angle of the second harmonic circulating current is calculated using this analysis. Under these operating conditions, two FB-submodule capacitor voltage regulation strategies are implemented and discussed in this research work, that is to fully understand the behaviour of low order harmonic components of voltages and currents on the FB-MMC in the boost mode.

2.6 Analytical harmonic contents identification for MMC

This section considers a further literature review on a comprehensive analysis that uses to evaluate THD by identifying PWM harmonic contents of MMC voltages. In the analysis, a methodology of double Fourier series has been first utilised to identify a general formula for harmonic contents of the PWM wave for

two-level voltage source inverter 2L-VSI published in [79], and then was developed by [80], [81], [82] and [83]. This methodology using multi-carrier PWM strategies is extended to the MMC topologies for this purpose. Whereas, these multi-carrier PWM can primarily be classified into level-shifted carrier LSC-PWM and phase shift carrier PSC-PWM, as introduced in [84]. Based on these modulation strategies,

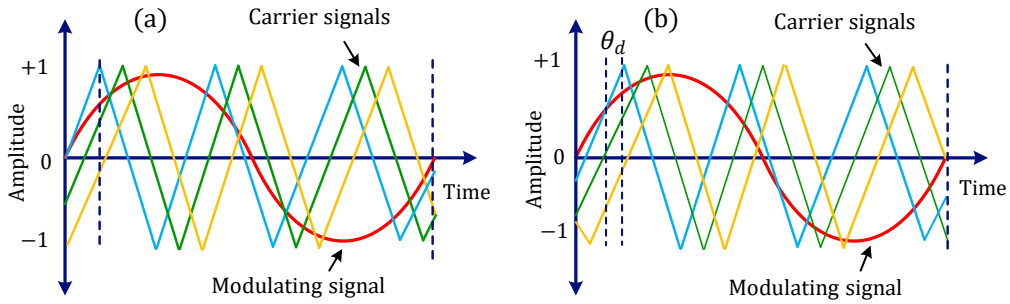


Fig 2.14 Modulation strategy of MMC based PSC-PWM: (a) without using the displacement angle, (b) with using the displacement angle

PWM gate signals for each submodule switches are easily generated; as the corresponding triangular carrier of the submodule is compared to modulating (reference) signal. For the HB-MMC topology, detailed PWM harmonic contents based on the PSC-PWM is analysed that to give features in lower THD within high effective switching frequency, as presented in [85]. It reported that two different phase output voltage levels with N+1 and 2N+1 can be generated, whereas N (odd or even) is the number of submodules per arm. By using the same modulation strategy, a general prescriptive of harmonic contents in the output voltage of the HB-MMC has been discussed in [86] and compared to cascaded H-bridge converters CHB. That is to obtain better harmonic cancellation. An impact of the dead time on the harmonic components is also considered. For both HB-MMC and FB-MMC, The PWM mathematical modelling was found and verified experimentally in [2]. Regarding odd and even number of submodule/arm, two different output voltage levels are produced because of harmonic cancellation with and without using displacement angle θ_d, as shown in Fig 2.14. This angle is conducted at an optimal

value between the upper and lower carrier waveforms. It concluded that the modulation strategy of PSC-PWM could offer attractive features in the terms of lower THD within high effective switching frequency. Besides, the energy stored in each submodule is distributed evenly. However, a harmonic performance of the output voltage levels and the circulating current can be functioned by a displacement angle. In order to operate the HB-MMC in low switching frequency in the range of 50-100 Hz, the PSC-PWM has been modified to be phase-shifted rotating carrier PSRC-PWM as recently discussed on a theoretical modelling in [87].

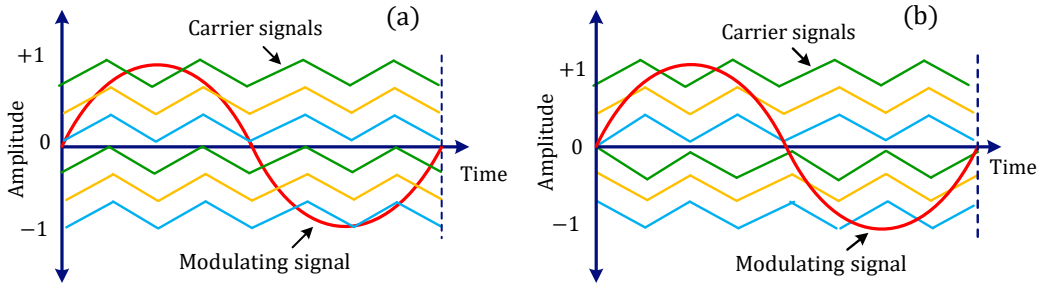


Fig 2.15 Modulation strategy of MMC based LSC-PWM: (a) using Phase Disposition PD-PWM, (b) using Alternate Phase Opposition Disposition APOD-PWM

On the contrary, the modulation strategy of LSC-PWM using a Phase Disposition PD-PWM and Alternate Phase Opposition Disposition APOD-PWM have also been carried out and compared in [84], [88], as illustrated in Fig 2.15. They have reported that the modulation scheme can generate different output voltage levels. In PD-PWM scheme can generate $2N+1$ phase output voltage levels. Thus it can be observed that the THD performance in the ac side of MMC is better than APOD-DPWM because of odd carrier groups cancellation. For the case of APOD-DPWM, the phase output voltage levels produced is $N+1$, harmonic distortion of the circulation current in the dc side is minimized, and hence the size of arm inductor can be less. The authors [84] in have reported that the PD-PWM would give harmonics performance better than that of PSC-PWM, but it may suffer from uneven loss distribution, as well as, the high effective switching frequency of PSC-PWM

can reduce THD with the high number of submodules [2]. It observed that LS-PWM strategy might cause an unequal energy distribution among the submodules. However, a mixture of the half-bridge and full-bridge cells can also be employed to form a hybrid MMC, for this case, the PWM schemes utilised for this structures have been developed in [89] to improve the harmonic minimisation of the output voltage.

From the previous literature review, there is no analytical model for PWM harmonic contents has been introduced to evaluate high order harmonics of the FB-MMC, whereas the dc link voltage varies. Hence analytical expressions are proposed in chapter 5 to identify the behaviour of these harmonic contents that existed in PWM output voltages. Thus analytical harmonic solution based on PSC-PWM scheme is proposed and developed using the double Fourier series expansion. The developed comprehensive analysis is mainly used to identify high order harmonic contents of the phase output voltage on the FB-MMC in the boost mode.

2.7 Chapter summary

This chapter presented a literature review on feasible configurations of the variable speed based wind energy conversion system WECS. The features and drawbacks of the traditional and multilevel converter topologies were discussed in terms of the generator side, the dc link voltage and grid side requirements. Among these converters, the emphasis of this chapter has been set on employing the FB-MMC in the direct drive of PMSG based WECS. A maximum power point tracking MPPT algorithm which suitable for this type of the WECS has been studied. Moreover, some steady-state analyses, which published to understand the behaviour of voltage and current components of the HB-MMC and FB-MMC, have been reviewed in this chapter. For high order harmonic contents identification, further analytical modelling of the MMC voltages were discussed and compared in terms of employing level-shifted carriers LSC-PWM and phase-shifted carriers PSC-PWM strategies.

Chapter 3: Design Consideration of the Full Bridge Modular Multilevel Converter Connected to the Grid under Variable DC Link Voltage

3.1 Introduction

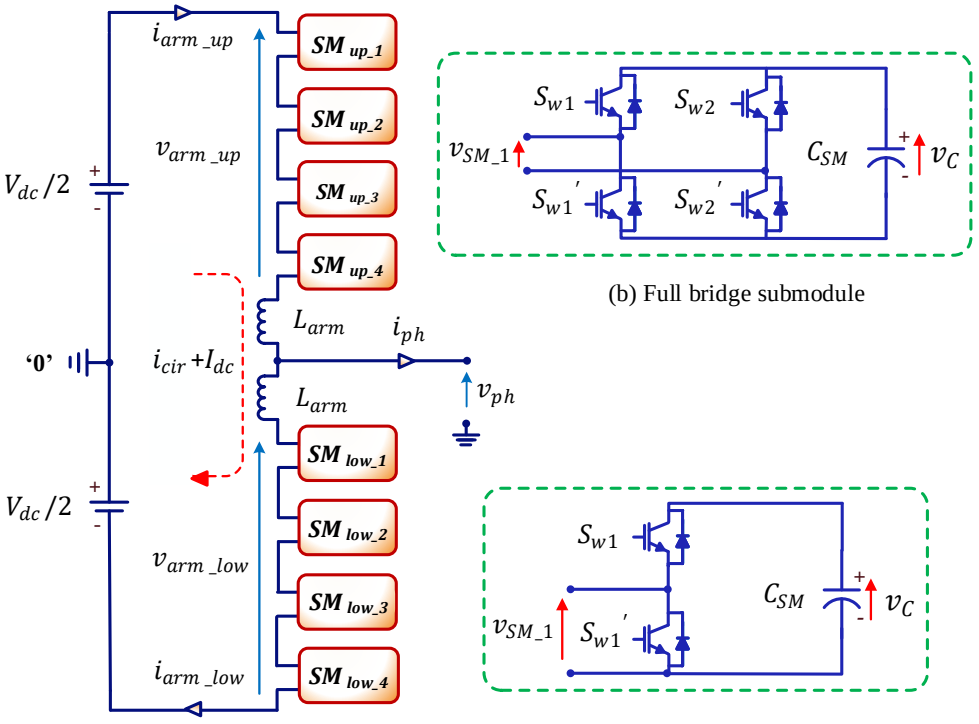
This chapter presents the full bridge modular multilevel converter FB-MMC. This converter can work in the buck and boost modes that regard the dc link voltage level. It is thus suitable for the grid-connected applications in which the dc link voltage varies over a wide range, such as in wind energy generation system. Based on the phase-shifted carriers PSC, this work develops the PWM modulation strategy by defining the dc and ac modulation indexes, that enable the FB-MMC to operate in the boost mode under varying dc link voltage. To explore a range of these modulation indexes in the boost mode over full range of the dc-link voltage, the developed modulation strategy is first applied to the single-phase FB-MMC switching model using in open-loop mode. However, in order to show the validity of the proposed modulation strategy in closed-loop control, this switching model of FB-MMC is then extended to the three-phase system, while connected to the grid. Two closed-loop control systems are employed in the grid connected FB-MMC. These control systems are used to achieve the active and reactive powers (by using the grid side current controller) and to minimize the 2^{nd} harmonic circulating with regulating the dc capacitor voltage of FB-submodules. Under these operating conditions, the work discusses two different regulation approaches for the FB-submodule capacitor voltages. The first approach regulates the dc capacitor voltage at the nominal value defined by the grid voltage, while in the second approach, the dc capacitor voltage varies according to the variations in the dc link voltage. This study reveals that the circulating current, capacitor voltage ripple and output voltage THD are highly dependent on the level of the dc link voltage. It identifies that the specific level of the dc link voltage can play a significant role in minimising the

circulating current and capacitor voltage ripple. In this work, the switching models of the FB-MMC are developed in Matlab\ Simulink environment and used to validate the proposed modulation strategy, and to analyse dependences of capacitor voltage ripples, circulating current and THD on the level of dc link voltage. These dependencies are revealed in this chapter and further analysed and analytical modelling in Chapter 4.

3.2 Operating principles of the modular multilevel converter MMC

3.2.1 Circuit configuration based on the single-phase system:

The typical circuit configuration of the MMC is illustrated in Fig 3.1. Based on the single-phase system, the MMC is constructed using the upper and lower arms, whereas each arm is formed by *N* number of identical full bridge submodules FB-SMs or half bridge submodules HB-SMs in the cascaded connection.



(a) Single phase MMC inverter

(b) Full bridge submodule

(c) Half bridge submodule

Fig 3.1 Circuit configuration of modular multilevel converter MMC: (a) phase leg of MMC, (b) Full bridge submodule, (c) Half bridge submodule

For a case of N is four, the submodules in the upper and lower arms are indicated by SM_{up_1} to SM_{up_4}, and SM_{low_1} to SM_{low_4}, respectively. In the FB-submodule, the main switches for both legs are denoted by Sw_1 and Sw_2, and their complementary are $Sw_1'$and Sw_2'. While the main switch with its complementary in the leg of HB-submodule are represented by Sw_1 and Sw_1' respectively.

As shown in Fig 3.1, the voltage and current quantities of the single-phase MMC inverter are illustrated in which v_{ph} and i_{ph} are phase output voltage and current in the ac side of the MMC. The dc link voltage is represented by $+V_{dc}/2$ and $-V_{dc}/2$, which is relative to the supply midpoint '0'. Moreover, v_C is the voltage across the submodule capacitor C_{SM}, and v_{SM} is corresponding to the output voltage of the submodule. Voltages of the upper arm v_{arm_up} and lower arm v_{arm_low} can be obtained by summing the output voltages of their submodules. A current in the upper arm is i_{arm_up}, while in the lower arm, it is i_{arm_low}. It can also be seen from Fig 3.1 that inductors of inductance L_{arm} are inserted in each arm, as they are needed to compensate for voltage interactions between the upper and lower arms. In this research work. The main parameters for the FB-MMC simulated switching model are chosen similarly to an industrial FB-MMC. These main system parameters used for this analysis are listed in Table 3.1.

Table 3.1: List of main parameters used in the simulation of the analytical and switching model for the single-phase FB-MMC

Parameter	Value [Unit]
Nominal active power P_n	1/3 M [W]
Nominal phase voltage V_{ph} r.m.s	3.535k [V]
Nominal phase current I_{ph} r.m.s	105 [A]
Nominal Frequency f_o	50 [Hz]
Nominal dc link voltage V_{dc_nom}	10k [V]
Submodule capacitance C_{SM}	2m [F]
Upper / lower arm Inductances L_{arm}	3m [H]
Submodule number N	4
Nominal voltage across submodule capacitor V_C	2.5k [V]
Switching frequency for each FB-submodule f_{sw}	1k [Hz]

Note that a circulating current i_{cir}, which is characterised by the dominant 2nd order harmonic component, is largely defined by the arm inductance and submodule capacitance. A trade-off between the value of submodule capacitance C_{SM} and the maximum capacitor voltage ripple has to be identified to achieve optimal system performance and improved efficiency [90]. A proper value of the arm inductance has to be carefully chosen to reduce the circulating current, in particular, to avoid the resonance at twice the fundamental frequency [67] (see Appendix A).

3.2.2 Full bridge versus Half bridge submodules:

In the modular multilevel converter based on half bridge submodule HB-MMC, as shown in Fig 3.1, each HB-submodule can only produce two voltage levels, which are positive voltage with $+v_C$ and the zero voltage. The upper arm voltage v_{arm_up} and the lower arm voltage v_{arm_low} falls within the following range [10]:

$$0 \leq v_{arm\_up} = \frac{V_{dc}}{2} - v_{ph} \leq +Nv_C \tag{3.1}$$

$$0 \leq v_{arm\_low} = \frac{V_{dc}}{2} + v_{ph} \leq +Nv_C \tag{3.2}$$

From (3.1) and (3.2), it can be observed that v_{arm_up} and v_{arm_up} are unidirectional voltages ranging from 0 to Nv_C. Thus, the amplitude of the output voltage is limited by the dc link voltage as $\hat{v_{ph}} \leq V_{dc}/2$ [10]. In the grid-connected mode, the output voltage of the HB-MMC has to be kept close to the grid voltage, and the dc capacitor voltage is regulated to the nominal value of $V_C = V_{dc}/N$. If the dc link voltage V_{dc} is less than $2\hat{v_{ph}}$, the grid connection cannot be achieved even if the dc capacitor voltage is increased to more than V_{dc}/N [10].

On the contrary, the full bridge submodules can generate negative, positive and zero voltages, and the voltage ranges of the upper and lower arm voltages of the FB-MMC can be extended using the following equations [10]:

$$-Nv_C \leq v_{arm\_up} = \frac{V_{dc}}{2} - v_{ph} \leq +Nv_C \tag{3.3}$$

$$-Nv_C \leq v_{arm\_low} = \frac{V_{dc}}{2} + v_{ph} \leq +Nv_C \tag{3.4}$$

From (3.3) and (3.4), it can be noted that v_{arm_up} and v_{arm_low} are bidirectional voltages covering the range from $-NV_C$ to $+NV_C$. For this case, the amplitude of the output voltage is not restricted by the dc link voltage. The FB-submodules will also generate the negative voltage $-V_C$ when the converter operates in the boost mode (when $V_{dc} < 2\hat{v_{ph}}$), While in the buck mode (when $V_{dc} = 2\hat{v_{ph}}$), only positive voltage $+V_C$ and the zero voltage are generated. Of note that the number of FB-submodules, which are inserted at the negative voltage state, is directly related to the level of the dc link voltage. As a result, the output voltage of the FB-MMC can be regulated independently of the dc link voltage.

Unlike the HB-MMC, this attractive solution of the FB-MMC, which allows operation in the buck and boost modes, can be utilised to address a technical challenge of the dc link voltage variation. Therefore, FB-MMC is suitable for the grid interface renewable sources such as the wind energy system [10], whereas the dc link voltage varies over a wide range.

3.3 Developed Pulse Width Modulation Strategy for FB-MMC

3.3.1 PSC-PWM for FB-MMC operating in buck mode

In this section, A modulation strategy introduced in [2] for the FB-MMC is discussed in details. The introduced modulation strategy considers using PSC-PWM. Two modulating signals have been assigned to operate each FB-submodule; the first modulating signal for the left leg, while other for the right leg of the FB-

submodule. Regarding the submodule in the lower arm as an example, these modulating signals can be given as follows [2] :

$$m_{low\_LL}(t) = \left\{\frac{3}{4} + \frac{M_{ac}}{4}\sin(\omega_0 t)\right\} \tag{3.5}$$

$$m_{low\_RL}(t) = \left\{\frac{3}{4} - \frac{M_{ac}}{4}\sin(\omega_0 t)\right\} \tag{3.6}$$

From (3.5) and (3.6), M_{ac} refers to the ac modulation index, and ω_0 is a fundamental angular frequency. It is also noted that the dc offset of the modulating signals is set as fixed values, which regards the nominal dc link voltage level. When the FB-MMC works in this mode, modulation parameter M_{ac} is only used in this modulation strategy to specify the operation mode of the FB-MMC. For this case, the FB-MMC can only operate in the buck mode. And the output voltage of each submodule of the FB-MMC is either inserted at a positive level of $+V_C$ or bypassed with zero voltage. The dc capacitor voltage of the FB submodule is regulated to the nominal value of $V_C = V_{dc\_nom}/N$, whereas V_{dc_nom} is the nominal value of the dc link voltage. By using modulating signals defined by (3.5) and (3.6), an averaged value of the output voltage for each submodule in the lower arm can be given as the follows:

$$\begin{aligned} v_{SM\_low}(t) &= V_C\left(m_{low\_LL}(t) - m_{low\_RL}(t)\right) \\ &= V_C\left(\frac{1}{2} + \frac{M_{ac}}{2}\sin(\omega_0 t)\right) \\ &= \frac{V_{dc\_nom}}{2N} + \frac{M_{ac}V_{dc\_nom}}{2N}\sin(\omega_0 t) \end{aligned} \tag{3.7}$$

Where $v_{SM_{low}}(t)$ considers an averaged value of the FB submodule output voltage, which can be obtained by ignoring voltage ripples resulted from the switching frequency. From (3.7), it can be observed that both the dc-component and

fundamental voltages generated by the FB-submodule is directly associated to the dc link voltage V_{dc_nom}. Therefore, the limitation of the modulation strategy in [2] is that the amplitude of the FB-MMC output voltage is restricted to the nominal value of dc link voltage as the same operation of the HB-MMC. Moreover, the dc link voltage has to be two times the peak grid voltage as $V_{dc\_nom} = 2\hat{v_{ph}}$ [10]. That is to operate the FB-MMC considering grid connection requirements. Hence, the modulation strategy in [2] can be used to operate the FB-MMC only under constant dc link voltage. Here, M_{ac} should only be adjusted around one.

3.3.2 Extended PSC PWM for FB-MMC operating in both buck and boost modes

This research work develops the modulation strategy based on PSC-PWM. The developed modulation strategy is utilised from the method for the FB-MMC operating in buck mode [2] and is extended to the grid-connected FB-MMC under variable dc link voltage. In this developed modulation strategy, two modulation parameters are defined as the dc modulation index M_{dc} and ac modulation index M_{ac}, which allow for specifying the FB-MMC operation in the buck and boost modes. The output voltage is regulated by the modulation index M_{ac}, while M_{dc} is used to adjust the dc-offset of the output voltage of each FB-submodule according to the variations in the dc link voltage. To satisfy the grid-connected requirement under these operational conditions. This research work proposes the modulation signals for each FB-submodule in the upper and lower arm. For the lower arm as defined by (3.5) and (3.6), the two modulating signals are developed for this PSC-PWM strategy as follows:

$$m_{low\_LL}(t) = \left\{\frac{1}{2} + \frac{M_{dc}}{4} + \frac{M_{ac}}{4}\sin(\omega_0 t)\right\} \tag{3.8}$$

$$m_{low\_RL}(t) = \left\{\frac{1}{2} - \frac{M_{dc}}{4} - \frac{M_{ac}}{4}\sin(\omega_0 t)\right\} \tag{3.9}$$

Similarly, the two modulating signals are also required for each FB-submodule in the upper arm. For this case, the modulating signals for the left and right legs can be given as follows:

$$m_{up\_LL}(t) = \left\{\frac{1}{2} + \frac{M_{dc}}{4} - \frac{M_{ac}}{4}\sin(\omega_0 t)\right\} \tag{3.10}$$

$$m_{up\_RL}(t) = \left\{\frac{1}{2} - \frac{M_{dc}}{4} + \frac{M_{ac}}{4}\sin(\omega_0 t)\right\} \tag{3.11}$$

Using the developed modulation strategy, it gives the FB-MMC an ability to produce the amplitude of the output voltage independently of the dc link voltage level. Thus, all FB-submodules will generate same the dc offset voltages with $V_{dc\_act}/2N$ that to meet the variation in the dc link voltage, while the amplitude of the fundamental voltages of the submodules are maintained constant with $\hat{v_{ph}}/2N$. Where V_{dc_act} refers to an actual value of the dc link voltage, the fundamental voltages in the lower arm submodules are generated in the opposite direction to those of the submodules in the upper arm. Using the developed modulating signals proposed by (3.8) and (3.9), the output voltage of each FB submodule in the lower arm as an example can be expressed as follows:

$$\begin{aligned} v_{Sm\_low}(t) &= V_C\left(m_{low\_LL}(t) - m_{low\_RL}(t)\right) \\ &= V_C\left(\frac{M_{dc}}{2} + \frac{M_{ac}}{2}\sin(\omega_0 t)\right) \\ &= \frac{V_{dc\_act}}{2N} + \frac{\hat{v_{ph}}}{N}\sin(\omega_0 t) \end{aligned} \tag{3.12}$$

where $\hat{v_{ph}} = \dfrac{V_{dc\_nom}}{2}$

Here, V_{dc_act} refers to an actual value of the dc link voltage. Form (3.12), the modulation parameters used in the developed modulation strategy can be discussed

in this section. Therefore, the ac modulation M_{ac} can be defined as the ratio between the fundamental component of the FB-submodule output voltage and the half of the dc capacitor voltage $V_C/2$ as the following expression:

$$M_{ac} = \frac{\hat{v_{ph}}/N}{V_C/2} = \frac{V_{dc\_nom}/(2N)}{V_C/2} \tag{3.13}$$

While a ratio of the dc component generated in the FB-submodule output voltage to the half of the dc capacitor voltage $V_C/2$ is defined by the dc modulation index M_{dc} as follows:

$$M_{dc} = \frac{V_{dc\_act}/2N}{V_C/2} \tag{3.14}$$

Based on $v_{Sm\_low}(t)$ operates at the buck and boost modes is also shown in Fig 3.2. It can be noted that the operating in the buck mode is achieved when the actual voltage of the dc link voltage V_{dc_act} is equal to its nominal value V_{dc_nom}. As aforementioned, each FB submodule voltage in this mode is generated with the positive state at $+V_C$, and is bypassed with zero voltage state.

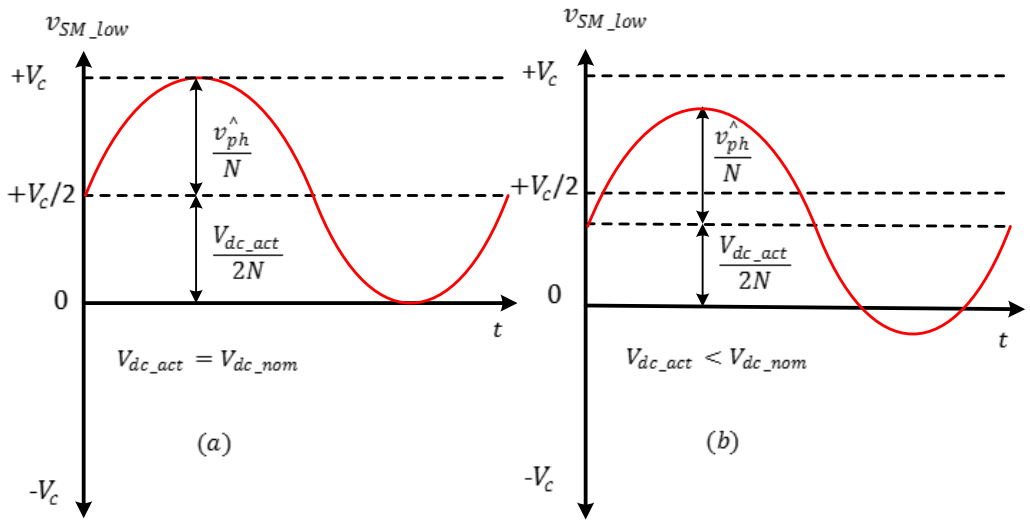


Fig 3.2 The output voltage of FB-submodule in the lower arm (a) when FB-MMC operates in the buck mode (b) when FB-MMC operates in the boost mode

Otherwise, it works in the boost mode when the value V_{dc_act} goes below V_{dc_nom}. Note that in the boost mode each FB submodule voltage is generated at the positive and negative states, namely at +V_C and -V_C, while it is bypassed with zero voltage state.

3.3.3 FB-submodule capacitor voltage regulation approaches under varying dc link voltage

For the grid-connected FB-MMC in the boost mode, the dc link voltage can operate in a range of (0 to V_{dc_nom}), as the FB-submodule capacitor voltages are decoupled in the boost mode from the actual dc link voltage level [91]. Hence, two different regulation approaches can be employed for the dc capacitor voltage V_C of each FB-submodule. In the first strategy, the dc capacitor voltage V_C is regulated to the nominal value, which is determined by the buck mode minimum dc link voltage requirement. While in the second approach, the dc capacitor voltage V_C varies according to the variations in the dc link voltage [10]. The second regulation is desirable because it can be used to reduce the voltage stress across the switching devices of the FB-submodules. From Fig 3.2, it can be observed that the value of the dc capacitor voltage for both regulation approaches should satisfy the following expression:

$$V_C \geq \frac{V_{dc\_act}}{2N} + \frac{\hat{v_{ph}}}{N} \tag{3.15}$$

Otherwise, the FB-MMC will operate in an overmodulation region. In the first regulation approach, the dc capacitor voltage of each FB-submodule is regulated to the fixed value whereas the dc link voltage V_{dc_act} varies within the range of [0, V_{dc_nom}] as illustrated in blue in Fig 3.3. The fixed value of V_C is considered at a nominal voltage of the FB-submodule capacitor, which can be determined at buck

mode when $V_{dc\_act} = V_{dc\_nom}$. According to $\hat{v_{ph}} = V_{dc\_nom}/2$ (for a case of the grid connected mode), the nominal value of V_C can be obtained from (3.15) as follows:

$$V_{C\_nom} = \frac{V_{dc\_nom}}{N} \tag{3.16}$$

In this case, the dc modulation index M_{dc} only varies, that covers the range of [0, 1] obtained from (3.14), while the ac modulation index M_{ac} is adjusted to be one as obtained from (3.13). Fig 3.4 illustrates in blue the range of the modulation indexes for this regulation approach. Compared to the previous method, the reduced value of V_C can be also regulated in accordance with the dc link voltage levels [10]. The minimum value of V_C can be reduced in the boost mode is determined by using (3.15) as follows:

$$V_C = \frac{V_{dc\_act} + V_{dc\_nom}}{2N} \tag{3.17}$$

In this case, the dc capacitor voltage V_C can be regulated from V_{dc_nom}/N to $V_{dc\_nom}/2N$, which allows covering the dc link voltage V_{dc_act} in range of [0,V_{dc_nom}], as illustrated in red in Fig 3.3. Here, M_{dc} varies in the range of [0, 1] which obtained from (3.14). While the M_{ac} varies regarding (3.13), that covering the range of [2, 1] as illustrated in red in Fig 3.4. As a result, both modulation indexes M_{dc} and M_{ac} can instantaneously vary in accordance with the level of the dc link voltage. It can be noted that the sum of ($M_{ac} + M_{dc}$) should not exceed the maximum of two to assume the FB-MMC works in a linear region . Otherwise, the FB-MMC may operate in the overmodulation region. In this case, some intersection points between the modulating signal and the carrier are missed. The overmodulation region allows to increase the phase output voltage if compared to the linear modulation region. However, it leads to increase THD of the phase output voltage, and consequently, of a decrease in the current and power quality. Whereas overmodulation leads to generate low-order harmonics, which are higher than the fundamental frequency of the phase output voltage [92], [93].

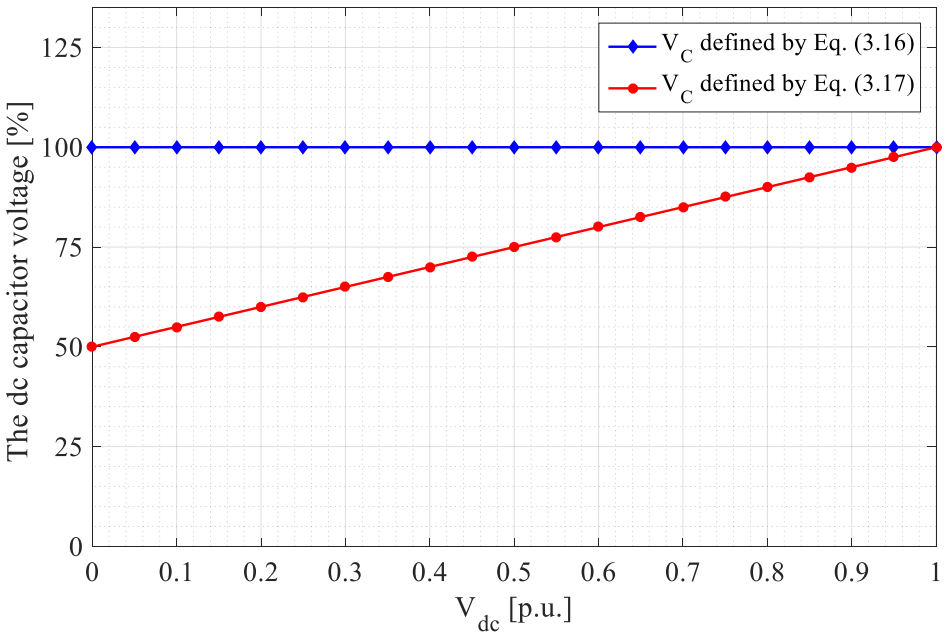


Fig 3.3 The ranges of the dc capacitor voltage V_C when the FB-MMC operates in the boost mode

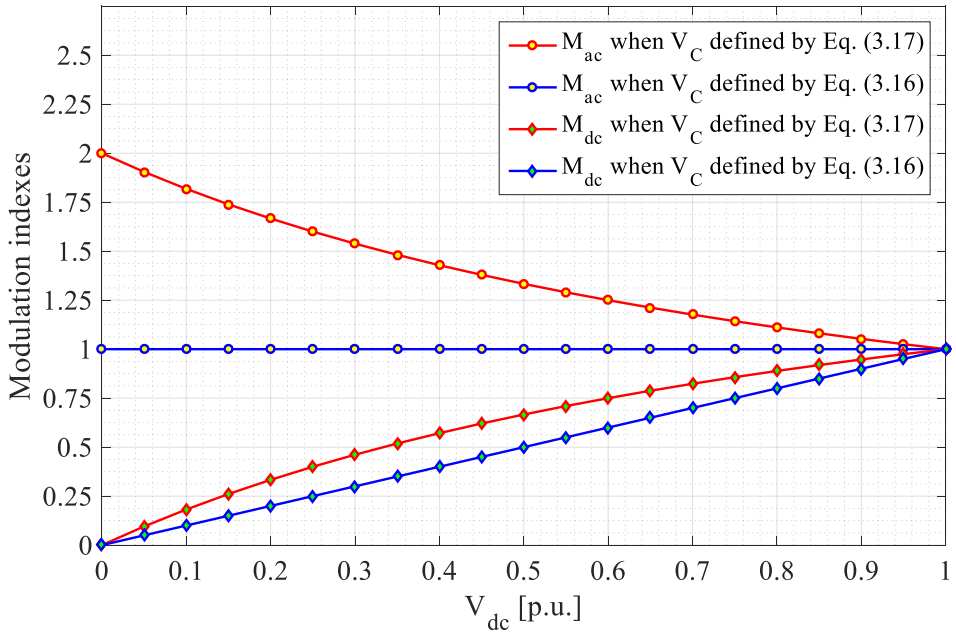


Fig 3.4 The ranges of the modulation indexes M_{ac} and M_{dc} when FB-MMC operates in the boost mode

3.3.4 PSC PWM scheme for the switching model of FB-MMC

The phase-shifted carriers based PWM scheme is implemented using the developed modulating signals into the switching models of the FB-MMC. For this modulation strategy, each submodule of the FB-MMC has a specific carrier based on the triangular waveform $c_{r\_SM}(t)$. As the carrier waveforms are normalized with respect to the nominal value of the dc capacitor voltage V_{C_nom}, an amplitude of each carrier waveform is determined with a maximum value of $+1$ and a minimum value of zero. In this work, the FB-MMC considers four submodules per arm. Hence, a phase angle is used of π/4 between the carriers of two adjacent FB-submodules in the same arm [2], [85]. For the upper and lower arms, the triangular carriers are shifted as 0, π/4, π/2, 3π/4. A displacement angle of (π /2N= π/8 can be added to the phase angle of the carriers in the upper or lower arms [2]. In order to modulate the main switch in each submodule leg, the PWM gate signal is provided by a comparison of the leg modulating signal and the submodule carrier. Fig 3.5 shows the developed PSC-PWM modulation scheme.

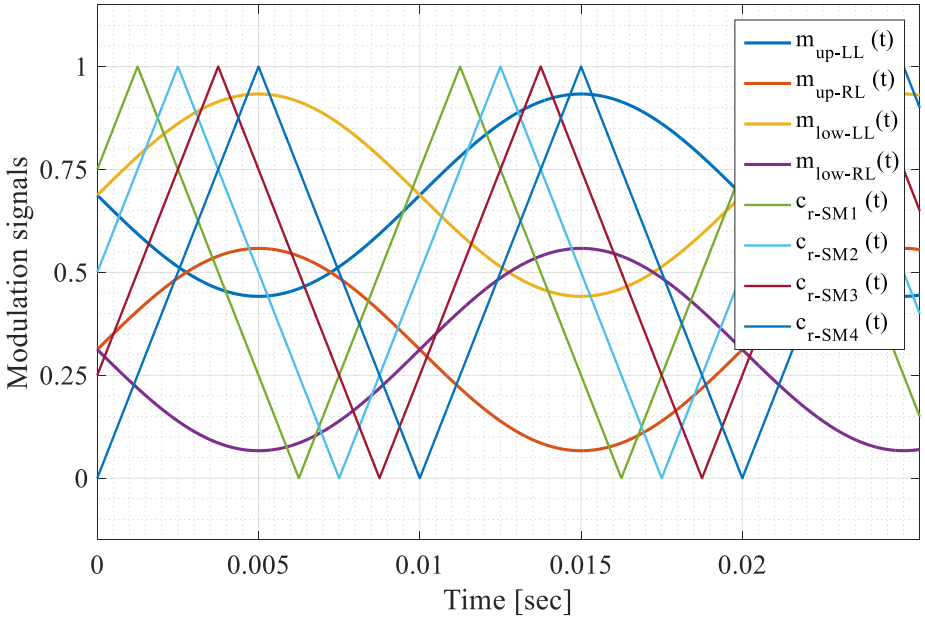


Fig 3.5 PSC-PWM scheme for the FB-MMC with N= 4

which is applied for the FB-MMC with *N*=4. Here, both modulation indexes M_{ac} and M_{dc} are set at one, and the carrier frequency is chosen to be 100 Hz for illustration, while the fundamental frequency is 50 Hz.

3.4 The grid connected FB-MMC under varying dc link voltage

3.4.1 Circuit configuration of the three-phase system:

A circuit configuration of three-phase FB-MMC while connecting to the grid is demonstrated in Fig 3.6 The FB-MMC structure contains six identical arms, and each arm has one inductor and four FB-submodules in series connection. Each phase leg of the FB-MMC is previously detailed in section 3.2.1. The FB-MMC which operates as the inverter is connected to the ac grid through line inductors.

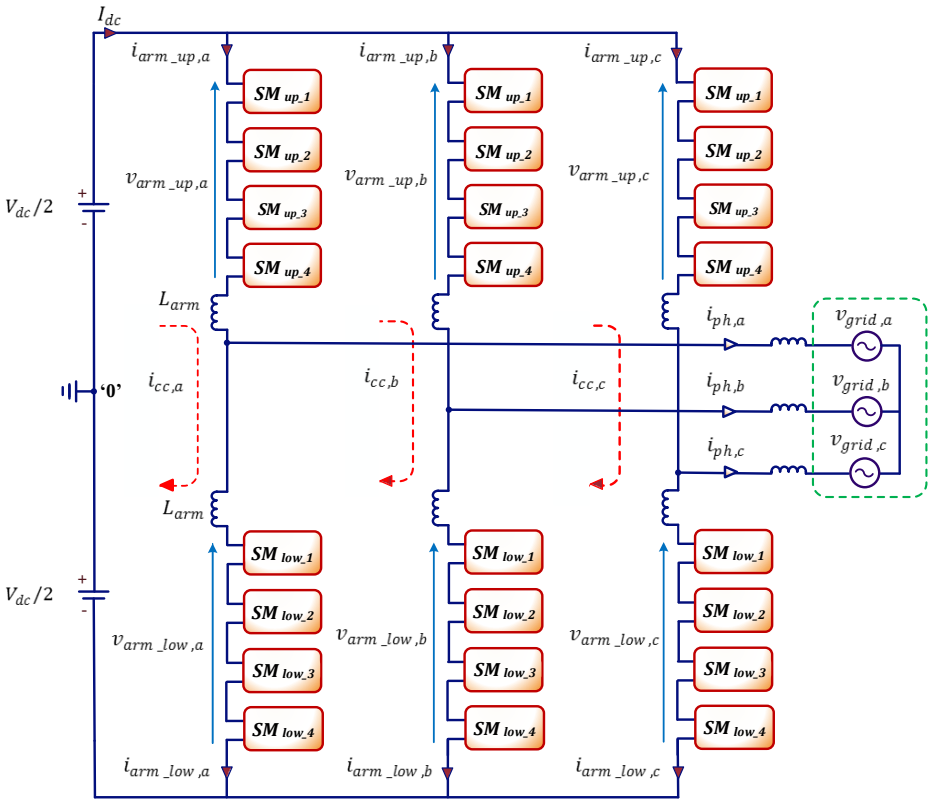
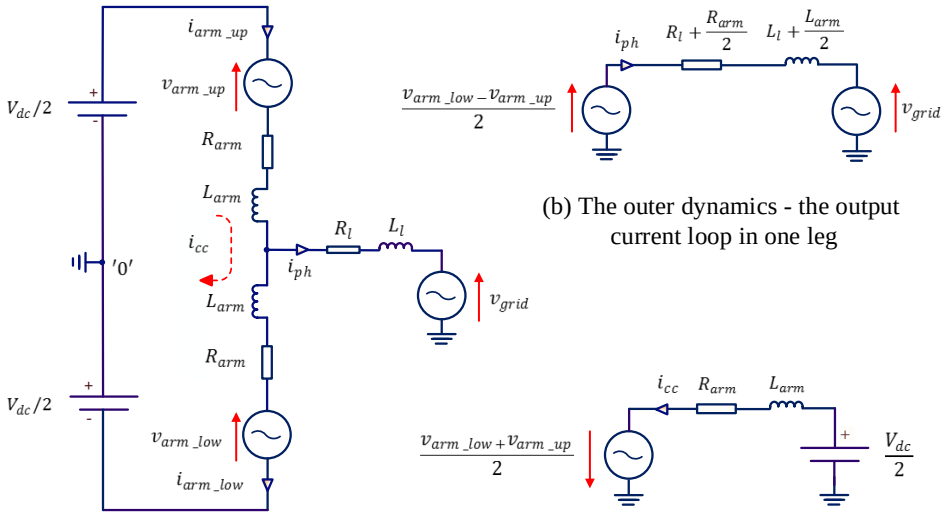


Fig 3.6 Circuit configuration of three-phase grid connected FB-MMC

In this work, the switching model of this circuit configuration is built in the MATLAB\Simulink environment, that is to validate the design of control loops using the proposed PSC PWM modulation strategy.

3.4.2 Dynamic modelling of the grid connected FB-MMC

The dynamic modelling of the grid connected FB-MMC is considered in this research work to optimise parameters of a control circuit used. For any number of submodules per arm, this modelling can be used for evaluating the behaviour of the FB-MMC in the dynamic and steady-state conditions. First, it is required to design the control systems, which deals with the active and reactive control and the dc capacitor voltage regulation of the FB-submodules with the circulating current control. Each controller loop is adjusted according to its system plant, that can be obtained from the dynamic modelling analysis.



(a) Equivalent circuit of the FB-MMC

(b) The outer dynamics - the output current loop in one leg

(c) The inner dynamics-the circulating current loop in one leg

Fig 3.7 Dynamic modelling of the grid connected FB-MMC based on the single-phase schematic

According to [55] and [94], the dynamic modelling can be expressed by algebraic and differential expressions, and described in the single-phase schematic

as illustrated in Fig 3.7 (a). By applying Kirchhoff' voltage law, the dynamic equation in each phase leg can be obtained as follows [55],[94]:

$$v_{grid} = \frac{V_{dc}}{2} - v_{arm\_up} - R_{arm}\, i_{arm\_up} - L_{arm}\frac{di_{arm\_up}}{dt} - R_l\, i_{ph} - L_l\frac{di_{ph}}{dt} \tag{3.18}$$

$$v_{grid} = -\frac{V_{dc}}{2} + v_{arm\_low} + R_{arm}\, i_{arm\_low} + L_{arm}\frac{di_{arm\_low}}{dt} - R_l\, i_{ph} - L_l\frac{di_{ph}}{dt} \tag{3.19}$$

Where R_{arm} and R_l refer to the arm and line resistances. The line inductor is denoted by L_l. Also, the v_{grid} refers to the grid voltage. In this modelling, a single voltage source in each arm is considered to be equivalent to all FB-submodule voltages. By subtracting (3.19) from (3.18), the outer dynamic equation of the FB-MMC, as shown in Fig 3.7 (b) is determined as the following expression:

$$v_{grid} = v_{ph} + \left(R_l + \frac{R_{arm}}{2}\right) i_{ph} + \left(L_l + \frac{L_{arm}}{2}\right)\frac{di_{ph}}{dt} \tag{3.20}$$

The output voltage v_{ph} which is the voltage of converter output terminal to reference midpoint of the dc link. Thus it can be deduced as follows [94]:

$$v_{ph} = \frac{v_{arm\_low} - v_{arm\_up}}{2} \tag{3.21}$$

It can be seen that v_{ph} is controlled using the upper and lower arm voltages. As a result, the difference between the output voltage v_{ph} and the grid voltage is utilized to drive the output current i_{ph}. Using Kirchhoff's current law, the output current for each phase can be given as follows [55],[94]:

$$i_{ph} = i_{arm\_low} - i_{arm\_up} \tag{3.22}$$

When considering that the upper and lower arms have symmetrical structure, the output current is evenly divided into the two arms of the converter. The upper and lower arm currents can be defined as a function of the output and circulating currents as in the following expressions [55],[95]:

$$i_{arm\_up} = \frac{i_{ph}}{2} + i_{cc} \tag{3.23}$$

$$i_{arm\_low} = -\frac{i_{ph}}{2} + i_{cc} \tag{3.24}$$

Where i_{cc} represents the circulating current that flows within the dc link of the FB-MMC. Because of the difficulty in the measuring of the circulating current directly, it can be estimated depending on i_{arm_up} and i_{arm_low} as follows [55],[95]:

$$i_{cc} = \frac{i_{arm\_up} + i_{arm\_low}}{2} \tag{3.25}$$

Note that the circulating current i_{cc} in each phase leg (the dc inner loop) is composed of the ac component current at second-order harmonic i_{cir}, and superimposed on to one-third dc component current I_{dc} as follows [55], [95]:

$$i_{cc} = \frac{I_{dc}}{3} + i_{cir} \tag{3.26}$$

Both I_{dc} and i_{cir} only circulate in the dc link of the FB-MMC. Thus these currents don't appear in the grid side. The dc current I_{dc} can provide the active power transfer from the dc link of the FB-MMC to the ac grid side. While the high circulating current i_{cir} can negatively affect the converter performance [55]. The inner dynamic behaviour of the FB-MMC, as shown in Fig 3.7 (c) is given by adding (3.18) to (3.19) as follows [54], [96], [97]:

$$R_{arm}\, i_{cir} + L_{arm} \frac{di_{cir}}{dt} = \frac{V_{dc}}{2} - \frac{v_{arm\_low} + v_{arm\_up}}{2} \tag{3.27}$$

Consequently, the voltage v_{cir}, which excites the circulating current i_{cir}, can be found by as follows [54], [96], [97]:

$$v_{cir} = \frac{V_{dc}}{2} - \frac{v_{arm\_low} + v_{arm\_up}}{2} \tag{3.28}$$

It can be seen that the circulating current is generated by the difference between the dc link voltage of the FB-MMC and the sum of the upper and lower arm voltages. Based on [90] and [95], the dynamic performance of the FB submodule capacitor voltages for each arm can be expressed as follows:

$$\frac{C_{SM}}{N}\frac{dv_{C\_up}^{\Sigma}}{dt} = (m_{up\_LL} - m_{up\_RL})i_{arm\_up} \tag{3.29}$$

$$\frac{C_{SM}}{N}\frac{dv_{C\_low}^{\Sigma}}{dt} = (m_{low\_LL} - m_{low\_RL})i_{arm\_low} \tag{3.30}$$

Where $v_{C\_up}^{\Sigma}$ and $dv_{C\_low}^{\Sigma}$ represent a summation of all FB-submodule capacitor voltages of the upper and lower arms, respectively. Hence, the total sum capacitor voltage is determined as [95]:

$$v_{C}^{\Sigma} = \frac{v_{C\_up}^{\Sigma} + v_{C\_low}^{\Sigma}}{2N} \tag{3.31}$$

Where v_{C}^{Σ} represents an average capacitor voltage. By considering the modulating signals defined by (3.8), (3.9), (3.10) and (3.11) yields:

$$\frac{C_{SM}}{N}\frac{dv_{C\_up}^{\Sigma}}{dt} = \left(\frac{M_{dc}}{2} - \frac{M_{ac}}{2}\sin(\omega_0 t)\right)i_{arm\_up} \tag{3.32}$$

$$\frac{C_{SM}}{N}\frac{dv_{C\_low}^{\Sigma}}{dt} = \left(\frac{M_{dc}}{2} + \frac{M_{ac}}{2}\sin(\omega_0 t)\right)i_{arm\_low} \tag{3.33}$$

from (3.30), (3.31) and (3.32), it can be obtained as follows:

$$\frac{dv_C^{\Sigma}}{dt} = \frac{M_{dc} i_{cc}}{2C_{SM}} + \frac{M_{ac} i_{ph}}{2C_{SM}} \tag{3.34}$$

From the analysis presented in [95], the relation of the circulating current i_{cc} and average capacitor voltage v_C^{Σ} can be obtained from the above expression.

3.5 Control system of the grid connected FB-MMC

This work considers a design of control system, which are applied for the FB-MMC connected to the grid while the dc link voltage is varying. The control systems are designed using the dynamic modelling presented in the previous section. Two control circuits are given to ensure the FB-MMC works appropriately in the buck and boost modes. Based on the three-phase system as shown in Fig 3.8, the first control circuit is used to deal with the active and reactive power, while the other is used to regulate the dc capacitor voltages and to reduce the 2nd harmonic circulating current.

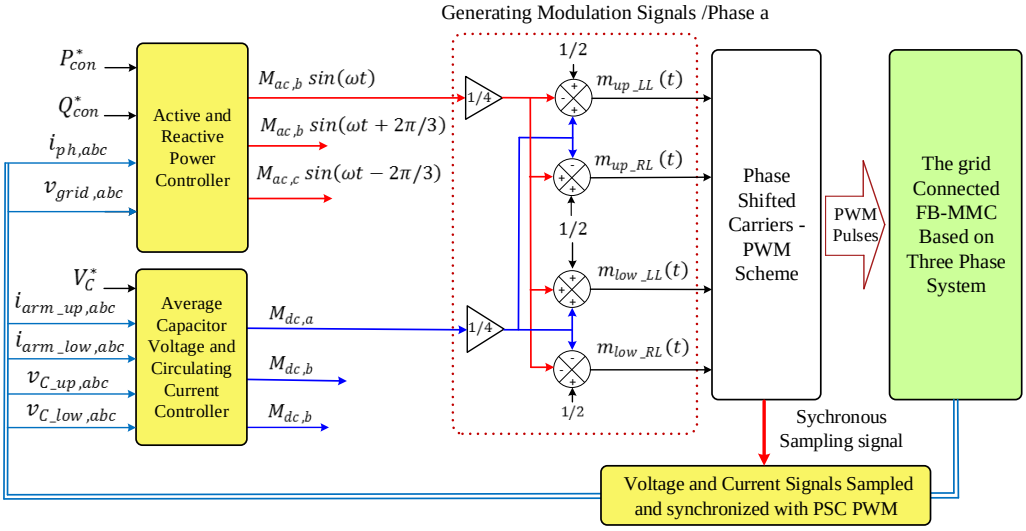


Fig 3.8 Control system employing for three-phase grid connected FB-MMC

3.5.1 Synchronous sampling based on the proposed PSC-PWM

A control circuit based on synchronous sampling technique was introduced in [98] and [99] for a single-phase full bridge converter, that allows removing these switching ripples from feedback measured current signals. These ripples which superimposed on a converter current are resultant from switching states of IGBT devices. In this work, the synchronous sampling technique is developed using the proposed PSC-PWM scheme, that to be used in the control circuits of the FB-MMC. Therefore, a design of the control circuits regards that all current input signals are sampled and synchronized with PSC-PWM scheme. Of note that a maximum amplitude of the switching ripple, which is existed in the upper and lower arm currents of the FB-MMC, can be estimated as follows [30] and [95] :

$$\Delta i = \frac{V_C}{2L_{arm}\, f_{sw,eff}} = \frac{V_C}{2L_{arm}\, 2Nf_{sw}} \tag{3.35}$$

Where $f_{sw,eff}$ refers to an equivalent switching frequency. For this case, the $f_{sw,eff}$ is determined by $2N$ times of the triangular carrier frequency f_{sw} [89]. Fig 3.9 shows that feedback measured current waveform $i(t)$ is resampled at every upper and lower peaks of the all triangle carriers in the PSC-PWM scheme. As a result, the sampled current $i_{samp}(t)$ is achieved eight values in one carrier interval $T_{sw} = 1/f_{sw}$. Thus, the sampling period T_{samp} can be obtained as follows:

$$T_{samp} = T_{sw,eff} = \frac{1}{f_{sw,eff}} = \frac{1}{2Nf_{sw}} \tag{3.36}$$

Here, a frequency of the sampling signal is $1/T_{samp}$. According to [81] and [98], the sampling technique in this research work can also be introduced as an asymmetrical double-edge regular sampled PWM. However, twice frequency of the sampling signal is possible to be obtained using PSC-PWM scheme if the crossing points of two adjacent carriers are considered as additional sampling reference (see Appendix C).

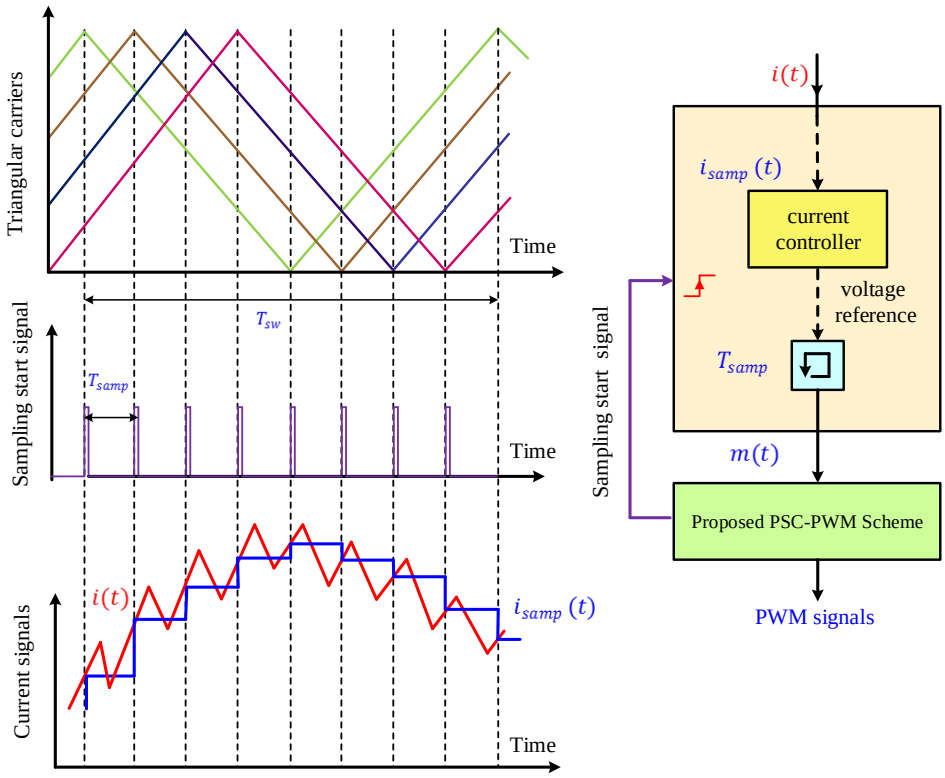


Fig 3.9 Synchronous sampling for the current waveform using the proposed PSC-PWM strategy, (a) The sampled current related to the carrier waveforms (b)Block diagram of the synchronous sampling method

3.5.2 Active and reactive power control:

A power control system for the grid connected FB-MMC is described in this section, that referring to the first control circuit displayed in the main section 3.5. The power control structure introduced in [100] for the HB-MMC is employed in this work to regulate the output current of the FB-MMC, as illustrated in Fig 3.10. In inversion mode, this control circuit is used to transfer the active powers from the dc to the ac side while the dc link varies. Two PI controllers in this circuit are implemented by translating the output converter currents from the *abc* into the *dq*-reference frames. The phase-locked loop PLL is also used to synchronise FB-MMC voltages with the grid voltage, that is achieved by estimating $\omega_0 t$ (the angular frequency of the grid).

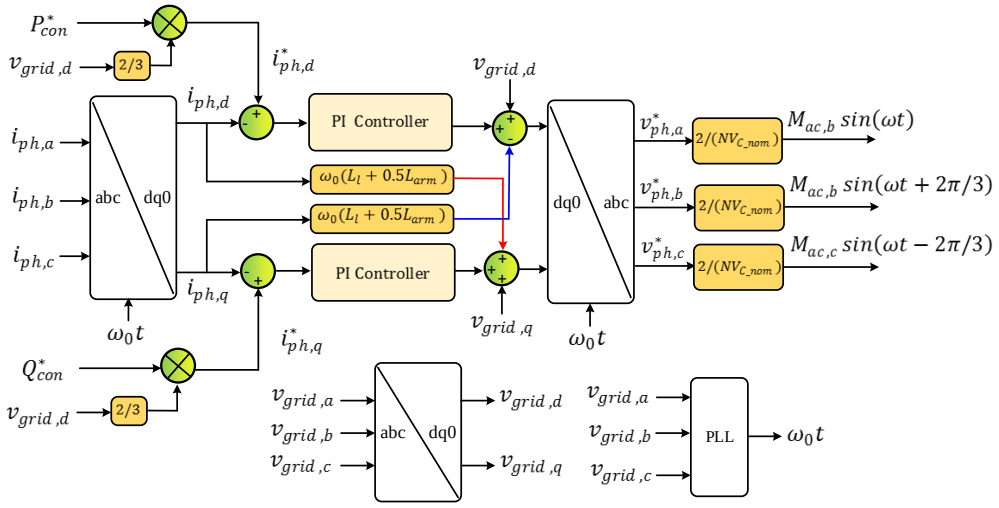


Fig 3.10 Active and reactive power control structures

The dynamics of the active power P_{con} and reactive power Q_{con} can be obtained from the following equations [101]:

$$P_{con} = \frac{3}{2}\left(v_{grid\_d}\ i_{ph\_d} + v_{grid\_q}\ i_{ph\_q}\right)$$
$$Q_{con} = \frac{3}{2}\left(v_{grid\_q}\ i_{ph\_d} - v_{grid\_d}\ i_{ph\_q}\right) \quad (3.37)$$

Where i_{ph_d} and i_{ph_q} refer to the output current in dq-axis coordinate system. It is assumed that the converter is connected to the stiff grid. Thus the d-axis is aligned to the grid voltage vector. For this case, the grid voltage in the q-axis v_{grid_q} is equal to zero. Hence, the current commands in the dq-frame, which are used to control P_{con} and Q_{con} independently, can be expressed as follows:

$$i^*_{ph\_d} = \frac{2}{3}\frac{P^*_{con}}{v_{grid\_d}}$$
$$i^*_{ph\_q} = \frac{2}{3}\frac{Q^*_{con}}{v_{grid\_d}} \quad (3.38)$$

Where $i^*_{ph\_d}$ and $i^*_{ph\_q}$ represent the current commands represented in the d and q-axis, respectively. These values are directly calculated from the desired active

power P_{con}^{*} and reactive power Q_{con}^{*} and then are set to track the instantaneous active and reactive powers. The current de-coupling terms defined by $\omega_o(L_l + 0.5L_{arm})$ and the voltage feed-forward voltages v_{grid_d} and v_{grid_q} are also employed in the control structure, to enhance the dynamics response for both PI-controllers. The output voltage commands in the *abc* reference frame are provided by the current controllers, which are:

$$\begin{aligned} v_{ph,a}^{*} &= M_{ac,a}\, sin(\omega t) \\ v_{ph,b}^{*} &= M_{ac,b}\, sin(\omega t + 2\pi/3) \\ v_{ph,c}^{*} &= M_{ac,c}\, sin(\omega t - 2\pi/3) \end{aligned} \tag{3.39}$$

Note that the output voltage commands are normalized with $2/(NV_{C\_nom})$, that to be matched with the minimum and maximum amplitudes of the proposed PSC-PWM scheme. In order to design the current controller, the dynamics of the grid connected FB-MMC defined by (3.20) are arranged in the *dq* coordinates as [101] and [102]:

$$\begin{aligned} v_{grid\_d} = v_{ph\_d} + \left(R_l + \frac{R_{arm}}{2}\right) i_{ph\_d} + \left(L_l + \frac{L_{arm}}{2}\right) \frac{di_{ph\_d}}{dt} \\ - j\omega_o \left(L_l + \frac{L_{arm}}{2}\right) i_{ph\_q} \\ v_{grid\_q} = v_{ph\_q} + \left(R_l + \frac{R_{arm}}{2}\right) i_{ph\_q} + \left(L_l + \frac{L_{arm}}{2}\right) \frac{di_{ph\_q}}{dt} \\ - j\omega_o \left(L_l + \frac{L_{arm}}{2}\right) i_{ph\_d} \end{aligned} \tag{3.40}$$

When the current decoupling terms are not taken into account, the equations defined by (3.40) can be given by transforming into the Laplace domain as follows:

$$\frac{i_{ph\_dq}}{v_{grid\_dq} - v_{ph\_dq}} = \frac{1}{s\left(L_l + \frac{L_{arm}}{2}\right) + \left(R_l + \frac{R_{arm}}{2}\right)} \tag{3.41}$$

That can also be simplified to:

$$\frac{i_{ph\_dq}}{v_{ph\_dq} - v_{grid\_dq}} = \frac{1/R_{con}}{sT_{RL\_con} + 1} \tag{3.42}$$

where

$L_{con} = \left(L_l + \frac{L_{arm}}{2}\right), R_{con} = \left(R_l + \frac{R_{arm}}{2}\right)$ and $T_{RL\_con} = L_{con}/R_{con}$

Note that T_{RL_con} refers to a time constant of the plant model, which is the FB-MMC output current. In order to parametrise PI controller gains (k_{p_i} and k_{i_i}), the output current control loop including the sampling time delay T_{samp} and PWM delay T_{pwm} are considered in this control design, as shown in Fig 3.11.

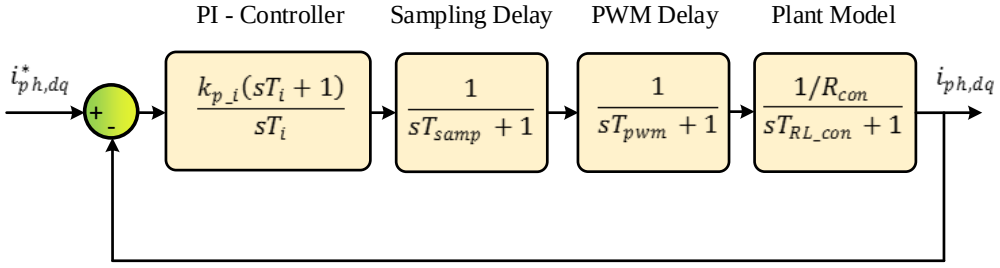


Fig 3.11 Block diagram of the output current control loop

Where T_i refers to the integral time constant of the PI controller, which is $T_i = k_{p\_i}/k_{i\_i}$. It can be seen that current sampling and PWM delays are represented by a first-order system [103] [104]. For a case of the FB-MMC, the T_{pwm} representing in an average time delay is equal to half of the effective switching cycle $T_{sw,eff}$ as follows:

$$T_{pwm} = \frac{T_{sw,eff}}{2} = \frac{1}{4Nf_{sw}} \tag{3.43}$$

While T_{samp} is defined by (3.36). Therefore, the transfer function of the output current control circuit can be expressed as:

$$G_{i\_ol}(s) = \frac{k_{p\_i}\left(\frac{sT_i + 1}{sT_i}\right)/R_{con}}{\left(sT_{samp} + 1\right)\left(sT_{pwm} + 1\right)\left(sT_{RL\_con} + 1\right)} \tag{3.44}$$

According to [104], both T_{pwm} and T_{samp} are small time constants with respect to the time constant of the plant model T_{RL_con}, i.e. ($T_{pwm} \ll T_{RL\_con}$, and $T_{samp} \ll T_{RL\_con}$). Hence, the open loop transfer function can be simplified as in the following expression:

$$G_{i\_ol}(s) = \frac{(k_{p\_i}/R_{con})(sT_i + 1)}{sT_i(sT_d + 1)\left(sT_{RL\_con} + 1\right)} \tag{3.45}$$

Where T_d is the total time delay of $T_{pwm} + T_{samp}$. By using the pole-zero cancellation method, the slow system pole can be cancelled by controller zero when considering that $T_i = T_{RL\_con}$. As a result, the open-loop transfer function can be represented as:

$$G_{i\_ol}(s) = \frac{(k_{p\_i}/R_{con})}{sT_{RL\_con}(sT_d + 1)} \tag{3.46}$$

Based on (3.46), the closed-loop transfer function will become a second-order system as follows:

$$G_{i\_cl}(s) = \frac{G_{i\_ol}(s)}{1 + G_{i\_ol}(s)}$$

$$G_{i\_cl}(s) = \frac{\frac{k_{p\_i}}{R_{con}T_{RL\_con}T_d}}{s^2 + \frac{1}{T_d}s + \frac{k_{p\_i}}{R_{con}T_{RL\_con}T_d}} \tag{3.47}$$

For tuning of the closed-loop control, an optimum modulus method is taken into consideration [55] and [105]. Therefore, the proportional gain of the PI controller k_{p_i} is calculated from the condition as follows:

$$\left|\frac{G_{i\_ol}(s)}{1+G_{i\_ol}(s)}\right| = \left|\frac{k_{p\_i}}{R_{con}T_{RL\_con}T_d\,(j\omega)^2 + R_{con}T_{RL\_con}(j\omega)+1}\right| = 1 \quad (3.48)$$

By evaluating (3.48) as introduced in [55] and [105], the proportional gain k_{p_i} can be given as follows:

$$k_{p\_i} = \frac{R_{con}T_{RL\_con}}{2T_d} \quad (3.49)$$

According to that, the controller parameters k_{p_i} and T_i are calculated. For a case of the equivalent switching frequency of 8 kHz, the sampling time delay T_{samp} is 1/8000 ms and the PWM delay T_{pwm} is 1/16000 ms. By considering system parameter values as $L_{arm} = 3\ mH,\ L_l = 5mH, R_{arm} = 0.05\Omega$ and $R_l = 0.05\Omega$, the controller parameters are found to be the proportional gain k_{p_i} = 17.33 and the integral time constant T_i = 0.08667 s.

3.5.3 The dc capacitor voltage and circulating current control:

The second control system applied for the grid connected FB-MMC is utilised to regulate the dc capacitor voltages of the FB-SMs and to minimise the 2nd order circulating current. This closed-loop control system is also known as an average capacitor voltage control [10],[100] ,[106] and [107]. In this work, another control circuit to regulate the dc capacitor voltages of FB-SMs is configured that considers the open-loop testing. Both closed and open loops are achieved that to comprehend an influence of the boost mode on the 2nd order circulating current, as the FB-MMC operates at different levels of dc link voltage. Both closed and open loops of the dc

capacitor voltage control are exploited to generate the dc modulation index M_{dc}, which gives the FB-MMC an ability to perform at the buck and boost modes.

3.5.3.1 When the closed-loop control used

For a case of the closed-loop control, the cascaded control structure for each phase includes current inner and voltage outer loops as illustrated in Fig 3.12 [107].

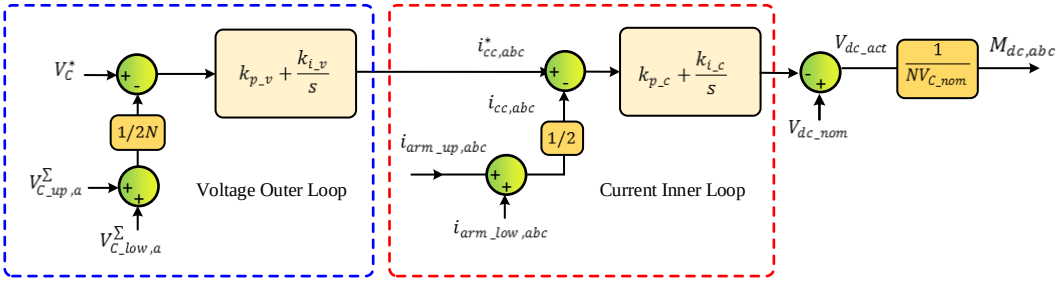


Fig 3.12 Control structure of the average capacitor control (closed-loop mode)

Under the operating condition of the grid connected mode, the current inner loop is employed to minimise in the 2nd order circulating current of the converter arms. That can be achieved by controlling the currents in both the upper and lower arms. Therefore, the plant model of the inner loop can be deduced from the inner dynamic performance of the FB-MMC [95], which are defined by (3.27) and (3.28). Hence, the inner dynamics from v_{cir} to i_{cir} can be evaluated in the Laplace domain as follows:

$$\frac{i_{cc}}{v_{cir}} = \frac{1/R_{arm}}{sT_{RL\_cc} + 1} \tag{3.50}$$

Where $T_{RL\_cc} = L_{arm}/R_{arm}$ represents a time constant of the plant model, which is the circulating current loop. The circulating current command i_{cc}^* is generated by the voltage outer loop, while the actual circulating current i_{cc} can be obtained from measuring arm currents. The difference between i_{cc}^* and i_{cc} is fed into the PI

controller in the current control inner loop to generate v_{cir}, which can be utilised to reduce the circulating current and to regulate the dc capacitor voltages of the FB-SMs.

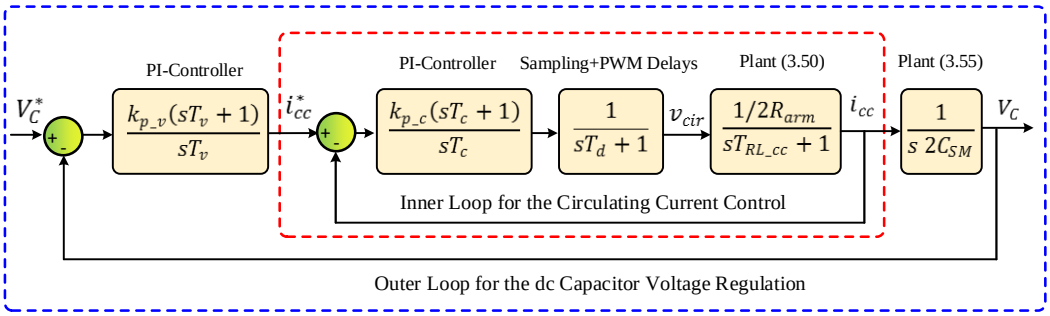


Fig 3.13 Block diagram for the closed-loop control of the dc capacitor voltage and circulating current for each converter phase

The inner loop for the circulating current control which including a total time delay T_d of this control loop, i.e. $(T_{samp} + T_{pwm})$ is illustrated in Fig 3.13. Thus the open-loop transfer function can be obtained as follows:

$$G_{cc\_ol}(s) = \frac{(k_{p\_c}/R_{arm})(sT_c+1)}{sT_c(sT_d+1)(sT_{RL\_cc}+1)} \tag{3.51}$$

Where T_c is the proportional time constant of the PI controller, which is used for the current inner loop. Based on the Pole-Zero cancellation method, the T_c is chosen to be equal T_{RL_cc}. The open-loop transfer function can be simplified to:

$$G_{cc\_ol}(s) = \frac{(k_{p\_c}/R_{arm})}{sT_{RL\_cc}(sT_d+1)} \tag{3.52}$$

The optimum design for the controller gains is evaluated according to the optimum modulus method [55], [105]. Therefore, the closed-loop transfer function is given as the following equation:

$$G_{c\_cl}(s) = \frac{G_{c\_ol}(s)}{1 + G_{c\_ol}(s)} = \frac{\frac{k_{p\_c}}{R_{arm} T_{RL\_cc} T_d}}{s^2 + \frac{1}{T_d} s + \frac{k_{p\_c}}{R_{arm} T_{RL\_cc} T_d}} \tag{3.53}$$

Based on (3.53), the proportional gain k_{p_c} is found regarding the condition as:

$$\left| \frac{G_{c\_ol}(s)}{1 + G_{c\_ol}(s)} \right| = 1$$

Therefore,

$$k_{p\_c} = \frac{R_{arm} T_{RL\_cc}}{2T_d} \tag{3.54}$$

With parameter values of $L_{arm} = 3mH, R_{arm} = 0.05\Omega$ and the total time delay $T_d = T_{samp} + T_{pwm}$=3/16000, the proportional gain k_{p_c} = 8 and the integral time constant T_c = 0.06 s. It noted that the current control inner loop should be faster than the voltage outer loop. The bandwidth of $G_{c\_cl}(s)$ is 1.3302 kHz. That is obtained from the bode diagram, as shown in Fig 3.14.

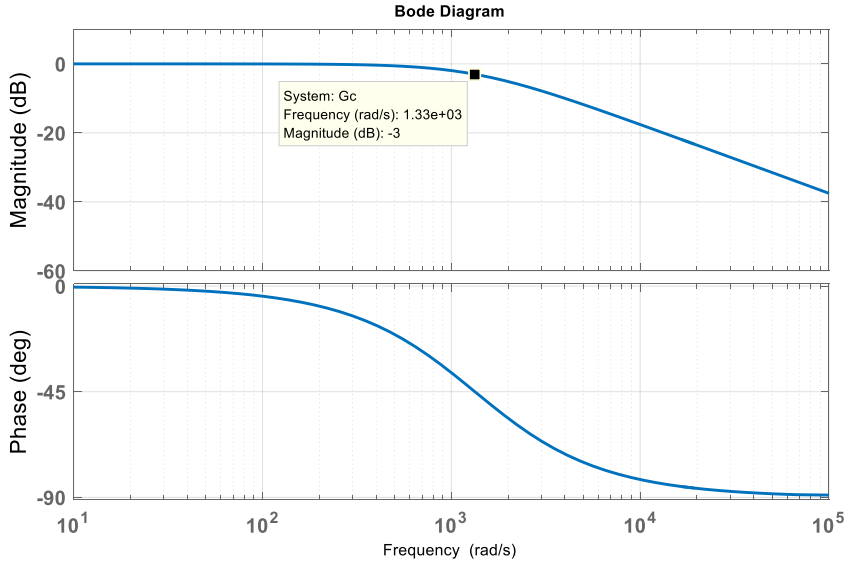


Fig 3.14 Bode diagram of the closed inner loop the dc capacitor voltage and circulating current control

For the voltage outer loop, it is used to ensure the dc capacitor voltage of each FB-submodule is regulated to the reference value. For each phase leg, the actual value of the dc capacitor voltage is firstly determined by the summation of all FB-submodule capacitor voltages within the lower and upper arms. According to obtain the actual average value, the summation of the capacitor voltages is divided by *2N*, which is the number of FB-submodules per leg. Thus, the actual average value is also defined by (3.31), while the reference value of the dc capacitor voltage is adjusted according to the regulation approaches as explained previously in (3.3.3). The circulating current reference i_{cc}^{*} is produced by the PI controller in the voltage outer loop, which depends on the difference between the reference value V_C^{*} and actual value v_C^{Σ}. According to [95], the variables v_C^{Σ} and i_{cc} which need to be regulated in the voltage outer control loop can be obtained from (3.34). Thus, the relation between v_C^{Σ} and i_{cc} (model plant) in the Laplace domain is given as follows:

$$\frac{v_C^{\Sigma}}{i_{cc}} = \frac{1}{s}\frac{1}{2C_{SM}} \tag{3.55}$$

The open-loop transfer function for the voltage outer loop can be expressed as:

$$G_{v\_ol}(s) = G_{c\_cl}(s)\frac{k_{p\_v}(1+sT_v)}{sT_v}\frac{1}{2C_{SM}s} \tag{3.56}$$

Because the current inner loop is faster than the voltage outer loop, the $G_{c_{cl}}(s)$ is set to one. Therefore, the closed-loop transfer function is:

$$G_{v\_cl}(s) = \left(\frac{1}{2C_{SM}}\right)\frac{k_{p\_v} + sk_{i\_v}}{s^2 + \frac{sk_{p\_v}}{2C_{SM}} + \frac{k_{i\_v}}{2C_{SM}}} \tag{3.57}$$

Where k_{p_v} and k_{i_v} refer to the proportional and integral gains of the PI controller for the voltage outer loop. It can be seen from (3.57) that the closed-loop

$G_{v\_cl}(s)$ is expressed in the second order system. To evaluate the controller gains k_{p_v} and k_{i_v}, the poles of $G_{v\_cl}(s)$ are compared with those of the reference system characteristic which can be given as follow [101]:

$$s^2 + 2\xi\omega_n s + {\omega_n}^2$$

Resulting in

$$k_{p\_v} = 2C_{SM}\, 2\xi\omega_n \qquad (3.58)$$

$$k_{i\_v} = 2C_{SM}\, {\omega_n}^2$$

Where ξ and ω_n are the damping ratio and the natural frequency of the $G_{v\_cl}(s)$. For good dynamic performance, the damping factor ξ is taken as 0.7. When the bandwidth of $G_{v\_cl}(s)$ is set to be slower than the grid frequency, the ω_n is chosen as 50π rad/s [95] and [101]. With the capacitance value C_{SM}= 2 mF, the controller gains are calculated as k_{p_v} = 0.8884 and k_{i_v}= 98.7. The bandwidth of $G_{c\_cl}(s)$, which is 322 Hz, are resulted from the bode diagram, as shown in ,Fig 3.15.

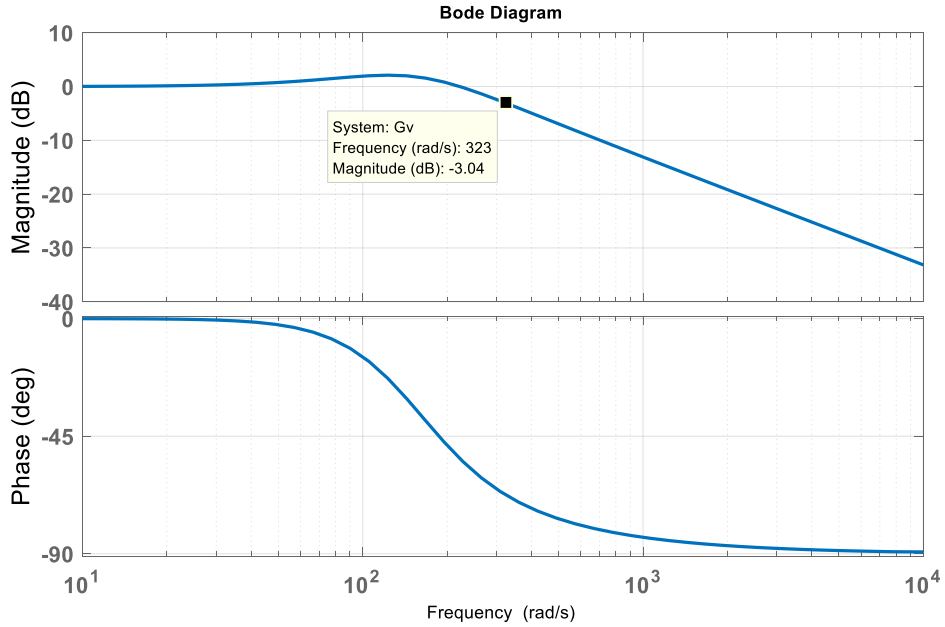


Fig 3.15 Bode diagram of the closed outer loop for the dc capacitor voltage and circulating current control

3.5.3.2 When the open-loop mode used

A second control approach to control the dc capacitor voltage is employed in this research work using the open-loop. It is applied for three-phase grid connected FB-MMC. The aim of this analysis is to analyse the influence of the operation in the boost mode on the 2nd harmonic circulating current. It is essential to notice that this open-loop control does not allow to suppress the 2nd harmonic circulating current. For the lower and upper arms in each phase, Fig 3.16 demonstrates how to regulate the dc capacitor voltages of the FB-submodules by using the open control loop. According to (3.14), the dc modulation index $M_{dc,abc}$ are generated in open loop mode to adjust V_C with respect to (3.16) as follows:

$$M_{dc,abc} = \frac{V_{dc\_act}/(2N)}{V_C/2} = \frac{V_{dc\_act}}{V_{dc\_nom}} \tag{3.59}$$

While to adjust V_C regarding the actual value of the dc link voltage level based on (3.17), the dc modulation index of this approach is obtained as follows:

$$M_{dc,abc} = \frac{V_{dc\_act}/(2N)}{V_C/2} = \frac{2V_{dc\_act}}{V_{dc\_nom} + V_{dc\_act}} \tag{3.60}$$

For both regulation approaches of the average capacitor control in the open-loop mode, it can be considered that the dc modulation index $M_{dc,abc}$ is generated in accordance with the actual and nominal values of the dc link voltage. Of note that each capacitor voltage for both the open and closed control loops may need to be balanced by using an individual voltage control as in [10] and [108] or sort and select method [97], [107], [109]. Capacitor voltage balancing is not considered in this study

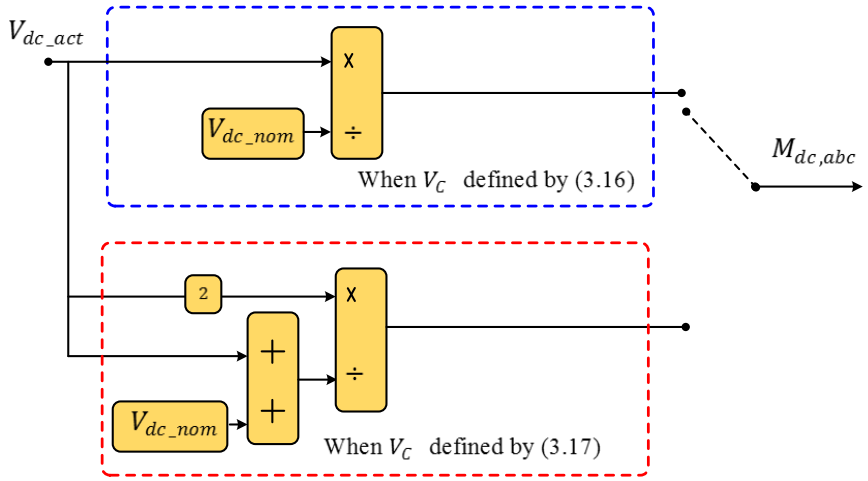


Fig 3.16 Block diagram of the average capacitor control in the open-loop mode

3.6 Simulation Results and Discussions:

3.6.1 Operation of the FB-MMC based on the single-phase system:

In order to study performance characteristics of the FB-MMC while being connected to the grid under variation in the dc link voltage, the switching model of the single-phase system illustrated in Fig 3.1 is built-in MATAB\Simulink environment (see Appendix A). The output of the FB-MMC is connected to the passive RL load. For all values of the dc link voltage V_{dc}, the FB-MMC output voltage is maintained at the constant value, while the power is first kept at the constant nominal value, and the case when power varies in accordance with the variation in the dc link voltage. Hence, this analysis is valid for grid mode. The simulation model matches well the performance of the single-phase FB-MMC connected to the grid with the phase-locked loop PLL, the output current controllers, and submodule capacitor voltage regulators and without the 2nd order circulating current control. For this case, the simulation model operates in the open-loop mode in which the modulation indexes M_{dc} and M_{ac} are adjusted manually.

3.6.1.1 Operating modes of the FB-MMC:

The FB-MMC is modulated using the developed PSC-PWM scheme with the switching frequency f_{sw} of 1 kHz, which is a frequency for each the triangular carriers. Fig 3.17 shows this modulation scheme when the FB-MMC operates in buck mode. It can be seen from Fig 3.18 that the FB-submodule voltage v_{SM} is generated with only two levels of voltages: the positive voltage $+v_C$ when the submodule is inserted, and the zero voltage when the submodule is bypassed. Fig 3.19 presents the developed PSC-PWM scheme when the FB-MMC works in the boost mode. As shown in Fig 3.20, the FB-submodule here is inserted at the negative voltage $-v_C$ or at the positive voltage $+v_C$. And at zero level voltage when the submodule is bypassed. For one fundamental period in the boost mode, it should be noted that the number of switching cycles of v_{SM} which inserted at $-v_C$ increases as V_{dc} decreases. The simulation results in the rest of the work are firstly obtained for the case when the dc capacitor voltage is regulated at the nominal value defined by the buck mode and given by (3.16). The simulation results are then compared with the case when the dc capacitor voltage is regulated in accordance with the dc link voltage given by (3.17). The behaviour of the grid-connected FB-MMC based on the abovementioned two regulation approaches is discussed in terms of the output voltage THD, the circulating current and capacitor voltage ripple. The complex interactions capacitor voltage ripple and their modulation references under the variable dc link voltage will lead to nonlinear behaviour of their electrical quantities on the dc and ac sides. That will be demonstrated further in the research work. The electrical characteristics are critical to system performance. Thus, it is necessary to realise their behaviour in order to be able to take them into account in the design phase for optimal system operation.

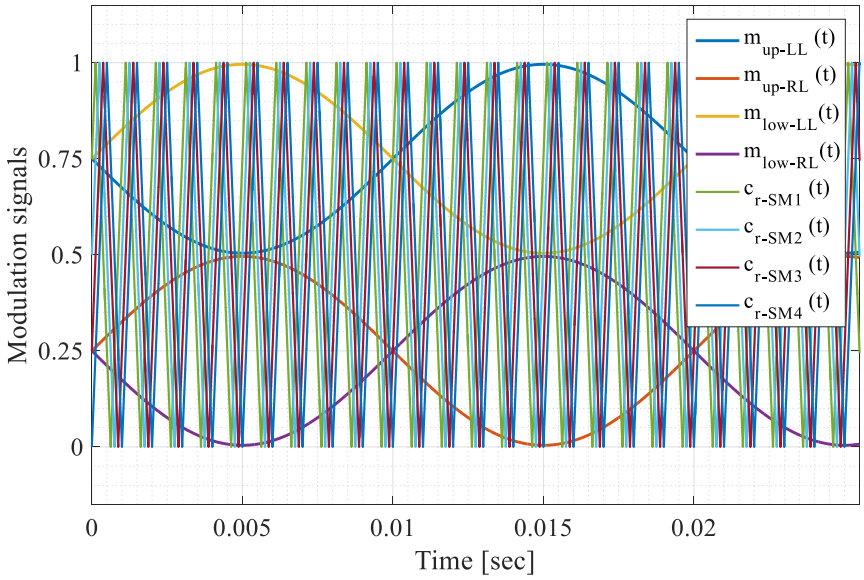


Fig 3.17 PSC-PWM scheme when FB-MMC operating in buck mode V_{dc_act} =V_{dc_nom}, M_{dc} =1 and M_{ac} = 1 and V_C defined by (3.16)

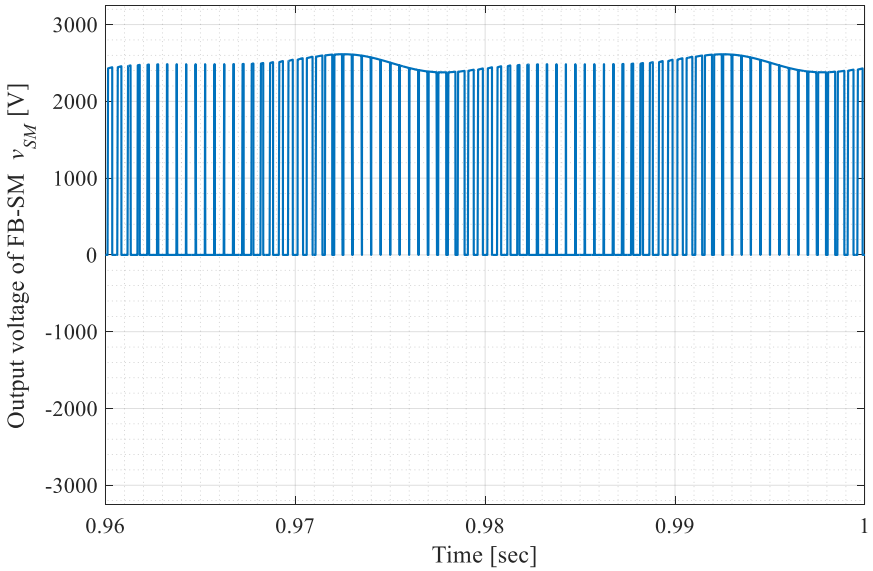


Fig 3.18 Output voltage of FB submodule when operating in buck mode V_{dc_act} = 100%of V_{dc_nom}, M_{dc} =1 and M_{ac} = 1 and V_C defined by (3.16)

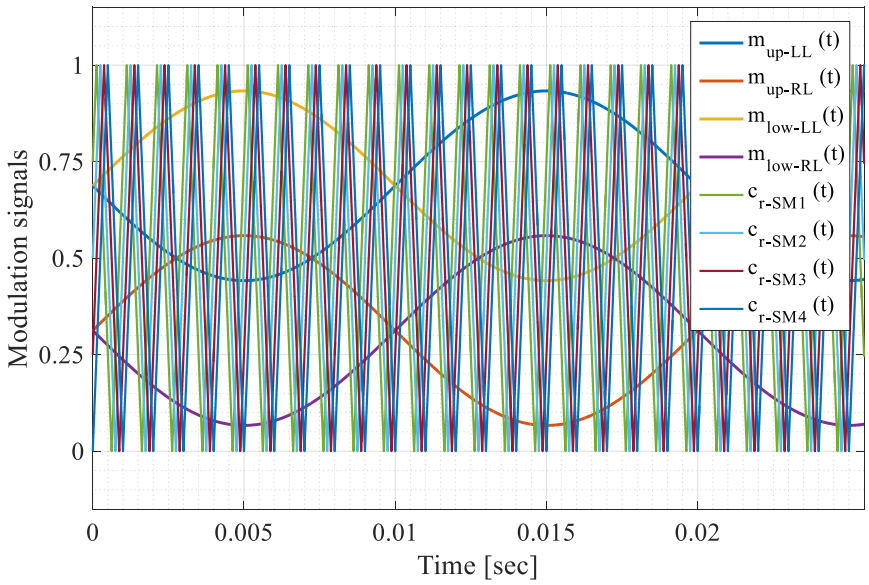


Fig 3.19 PSC-PWM scheme when FB-MMC operating in the buck mode V_{dc_act} = 75% of V_{dc_nom} , M_{dc} =0.75, M_{ac} = 1 and V_C defined by (3.16)

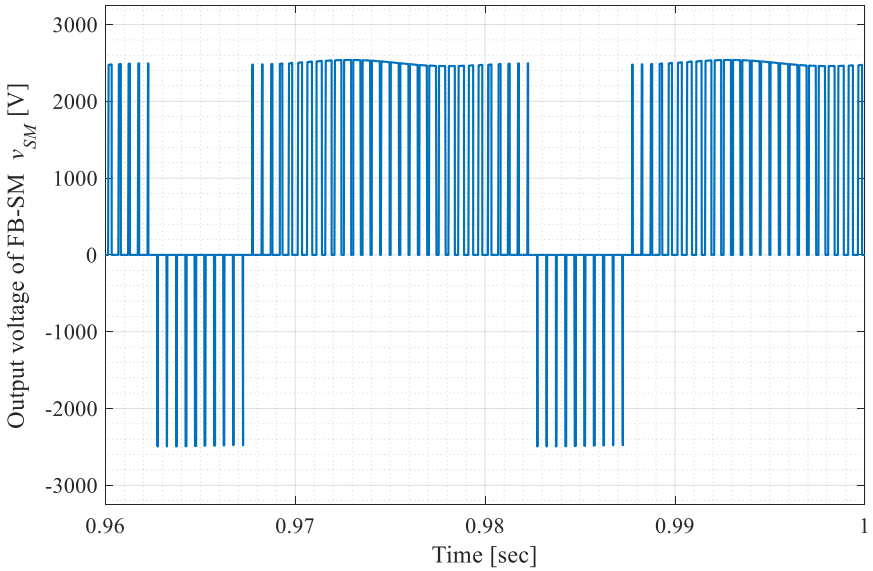


Fig 3.20 Output voltage of FB submodule when operating in buck mode V_{dc_act} = 75% of V_{dc_nom}, M_{dc} =0.75, M_{ac} =1 and V_C defined by (3.17)

3.6.1.2 Harmonic performance of the FB-MMC:

Since the FB-MMC submodules are inserted in the boost mode at the positive and negative voltages, namely at $+v_C$ and $-v_C$, interleaving of the upper and lower arm voltage levels occurs. The impact of the interleaving on the THD of the output voltage is exposed in this section. In this analysis, the output current is maintained constant at its nominal value defined in Table 3.1 while the dc link voltage varies from around zero to V_{dc_nom}. The simulation results in Fig 3.21 show that the THD values of the output voltage for the different levels of the voltage V_{dc_act}. It can be seen that the THD can vary as the dc link voltage varies. The simulation results shown in blue are obtained for the case when the zero displacement angle is used. For this case, the output voltage THD is at its minimum of around 15% when the dc link voltage is in the range of (70%-80%) and the range covering (20%-30%). The results illustrated in red are obtained for the case when an optimal displacement angle of π/8 is implemented, and it can be observed that the THD values are approximately shifted concerning the zero displacement angle case. Therefore, in order to remain the THD at the minimum value of around (13%-18%) over a wide dc link range, the displacement angle has to be adjusted in accordance with the dc link voltage. Note that a formula used to calculate THD can be given as follows [81]:

$$\text{THD} = \left\{ \sqrt{\sum_{n=2,3,\dots}^{\infty} \left(\frac{v_{ph,rms}^{(n)}}{v_{ph,rms}^{(1)}} \right)^2} \right\} 100\% \tag{3.61}$$

Where $v_{ph,rms}^{(1)}$ refers to the fundamental component value of $v_{ph}(t)$ in RMS, and harmonic components of order *n* are denoted by $v_{ph,rms}^{(n)}$. In order to realise the interleaving effect, the simulation results of the output voltage of the FB-MMC for the three values of the dc link voltage and the zero displacement angle are presented in Fig 3.22-Fig 3.25. The results in Fig 3.22 are given for the nominal dc link voltage of V_{dc_nom} and the dc capacitor voltage defined by (3.16), as defined in Table 3.1.

In this case, the FB-MMC works in the buck mode in which each submodule generates only $+v_C$ and the zero and the total number of output voltage levels is five as obtained for *N*+1, as can be observed in Fig 3.22. The modulation indexes for this case are: M_{dc} = 1 and M_{ac} =1. Fig 3.23 displays the simulation results of the output voltage of the FB-MMC for a dc link voltage of 75% of V_{dc_nom} and the dc capacitor voltage defined by (3.16). For this case, the FB-MMC operates in the boost mode, where each submodule can also generate the negative voltage $-v_C$, in addition to the positive voltage $+v_C$ and the zero voltage. The number of output voltage levels is increased to nine, which is given by *2N*+1. It can also be observed from Fig 3.21 that the minimum THD at this operating point is obtained. The modulation indexes for this case are: M_{dc} =0.75 and M_{ac} =1. For a dc link voltage of 60% of V_{dc_nom}, the THD of the output voltage increases, because the interleaving of the arm voltages is not optimal at this operating point, as can be seen in 3.21 and Fig 3.24. The modulation indexes for this case are: M_{dc} = 0.6 and M_{ac} = 1. On the contrary, when the dc capacitor voltage are defined by (3.17), more voltage levels of eleven are achieved at this operating point with the lower THD, as shown in Fig 3.25. The modulation indexes for this case are: M_{dc} =0.75 and M_{ac} =1.25.

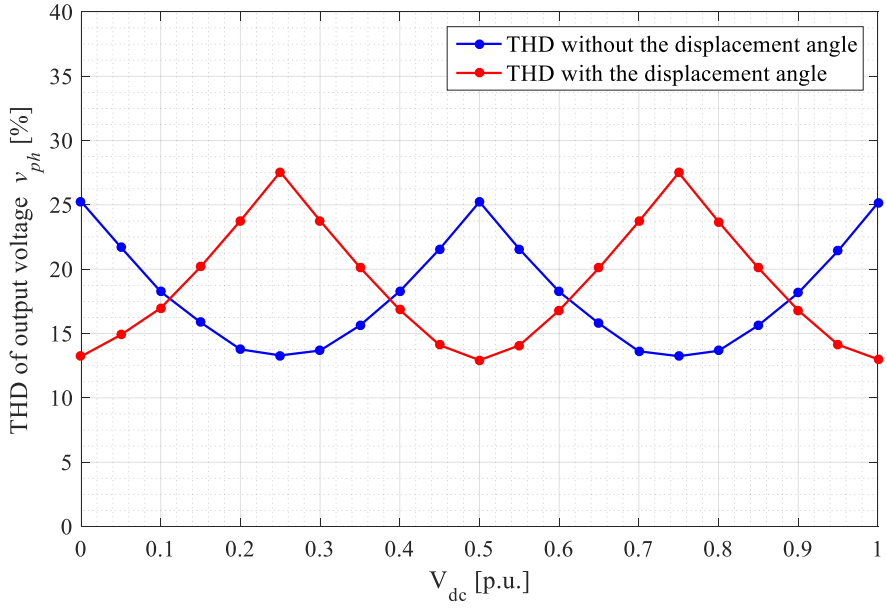


Fig 3.21 THD of the output voltage of FB-MMC when V_C defined by (3.16), M_{ac} =1 and M_{dc} = [0-1]

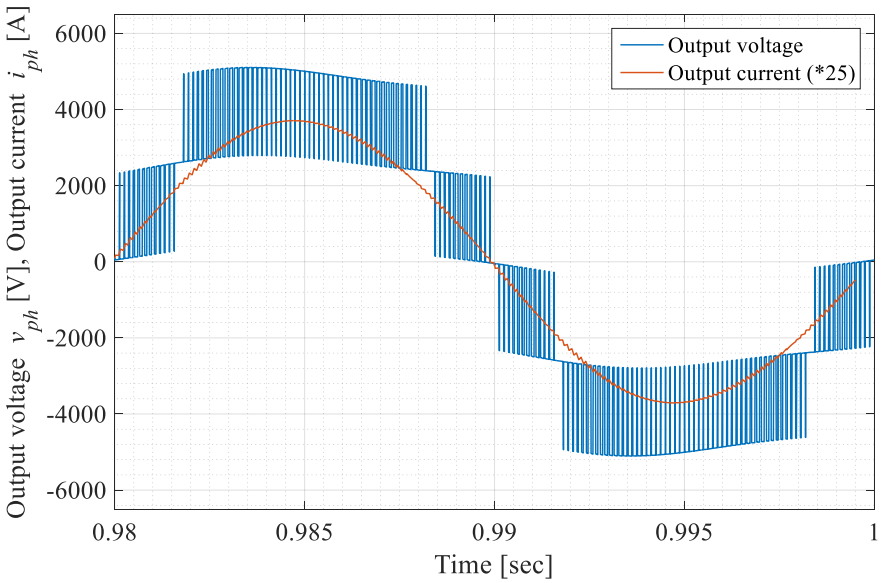


Fig 3.22 Output voltage and current of FB-MMC operates in buck mode V_{dc_act} = V_{dc_nom}, , M_{dc} =1 and M_{ac} =1 when V_C defined by (3.16)

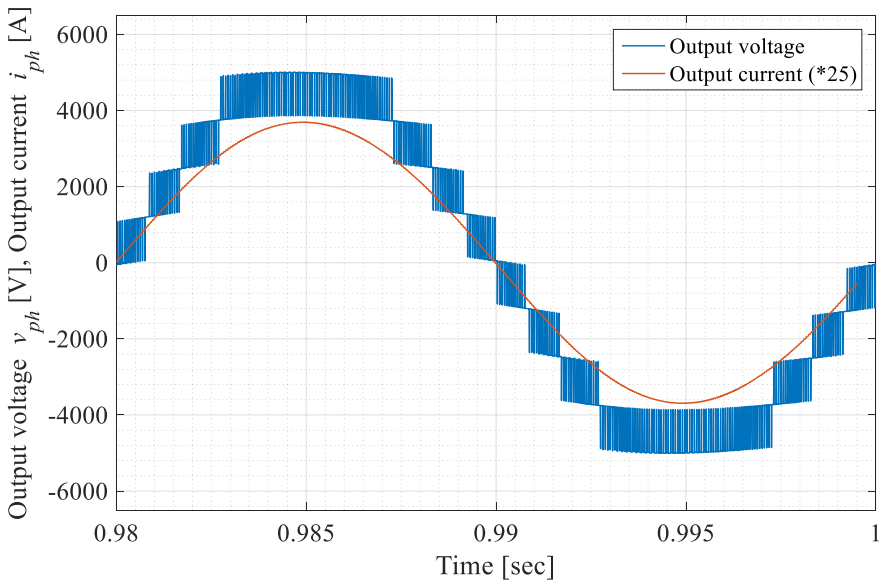


Fig 3.23 Output voltage and current of FB-MMC operates in the boost mode V_{dc_act} = 75% of V_{dc_nom}, , M_{dc} =0.75 and M_{ac} =1 and V_C defined by (3.16)

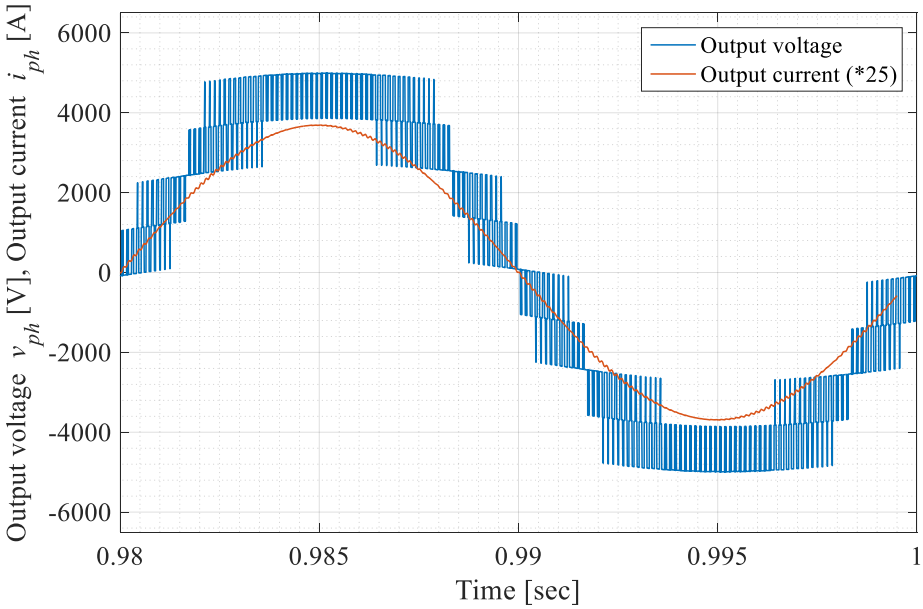


Fig 3.24 Output voltage and current of FB-MMC operates in the boost mode V_{dc_act} = 60 % of V_{dc_nom}, M_{dc} =0.6, M_{ac} =1 and V_C defined by (3.16)

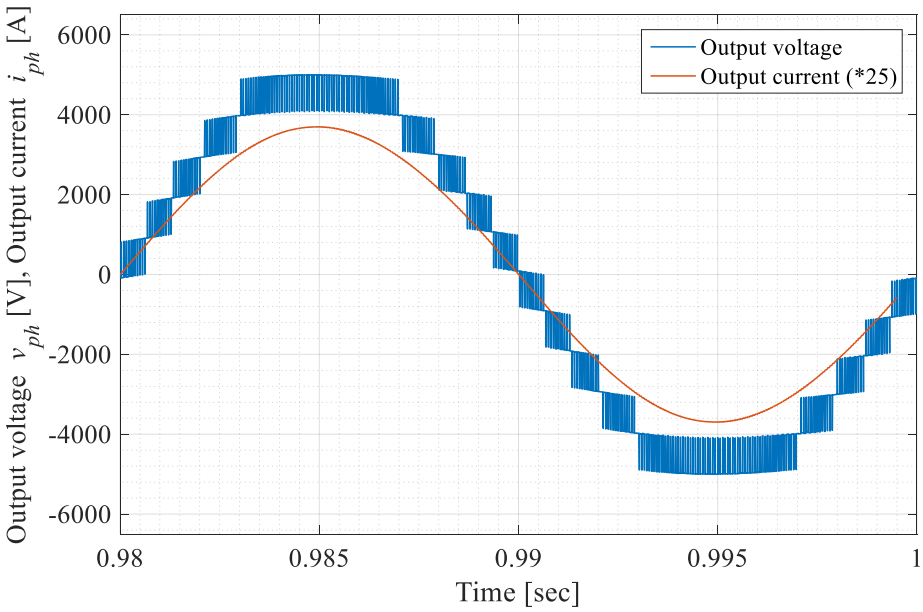


Fig 3.25 Output voltage and current of FB-MMC operates in the boost mode V_{dc_act} = 60% of V_{dc_nom}, M_{dc} =0.75, M_{ac} =1.25 and V_C defined by (3.17)

3.6.1.3 Circulating current and capacitor voltage ripple:

As for results in the previous section, the output current is also kept constant at its nominal value defined in Table 3.1 while the dc link voltage varies from around zero to V_{dc_nom}. The capacitor voltage is set to its nominal value given by (3.16). The simulation results are obtained for different values of the power factor in the range of [1,0], that by adjusting the RL load parameters at the output of the FB-MMC. They are obtained for the case when the submodule capacitor voltages are defined by (3.16). The simulation results presenting the circulating current and capacitor voltage ripple are shown respectively in Fig 3.26 and Fig 3.27. Of note that a percentage of the voltage ripple ε is calculated as the following expression:

$$\varepsilon = \frac{max(v_C(t)) - min(v_C(t))}{V_C}.100\% \qquad (3.62)$$

It can be seen that the circulating current is significantly affected by the variations in the dc link voltage, in particular when the dc link voltage goes below 15% of V_{dc_nom}. In the lower range of the dc link voltage, the circulating current can be reduced by operating at a low power factor. This point would be taken into consideration under fault ride-through requirements, as FB-MMC should work at the lower power factor to produce high reactive power [55]. Thus, it would be achieved without exceeding capacitor voltage ripple limits, as the circulating current is reduced. The reduced the circulating current will then affect the capacitor voltage ripple. For the system analysed in this work the minimum capacitor voltage ripple at the unity power factor can be achieved when the dc link voltage is set at 60% of V_{dc_nom} and the unity power factor. The results of this analysis reveal that the boost operating mode may be the optimal operating mode of the grid-connected FB-MMC.

3.6.1.4 Resonant operating point:

A series resonant circuit of the modular multilevel converter is formed of the arm capacitor with the equivalent capacitance of C_{SM}/N and the arm inductor of inductance L_{arm}. In order to avoid the higher circulating current with its second harmonic component occurring at the resonant point, a value of inductance L_{arm} for different resonant frequencies has to be identified. Fig 3.28 shows the RMS value of the second harmonic of the circulating current for different values of the arm inductance L_{arm} in the range of [0.5mH, 4mH]. The results are obtained for the different levels of the dc link voltage, i.e. for the nominal voltage V_{dc_nom} with the converter operating in buck mode, and for 60% of V_{dc_nom} and 35% of V_{dc_nom} with the converter operating in the boost mode. It can be seen that the resonant inductance is also affected by the level of the dc link voltage and that the minimum circulating current at the resonant point is obtained for a dc link voltage of 60% of V_{dc_nom} which was also the optimal operating point with respect to the minimum circulating current and capacitor voltage ripple with L_{arm} set as in Table 3.1.

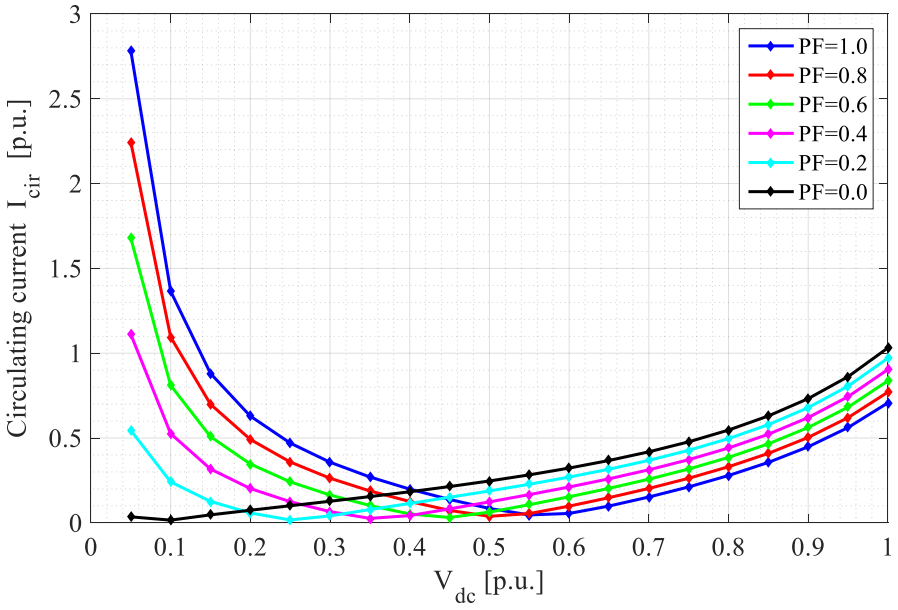


Fig 3.26 Circulating current versus dc link voltage when M_{dc} =[0-1], M_{ac} =1 and V_C defined by (3.16)

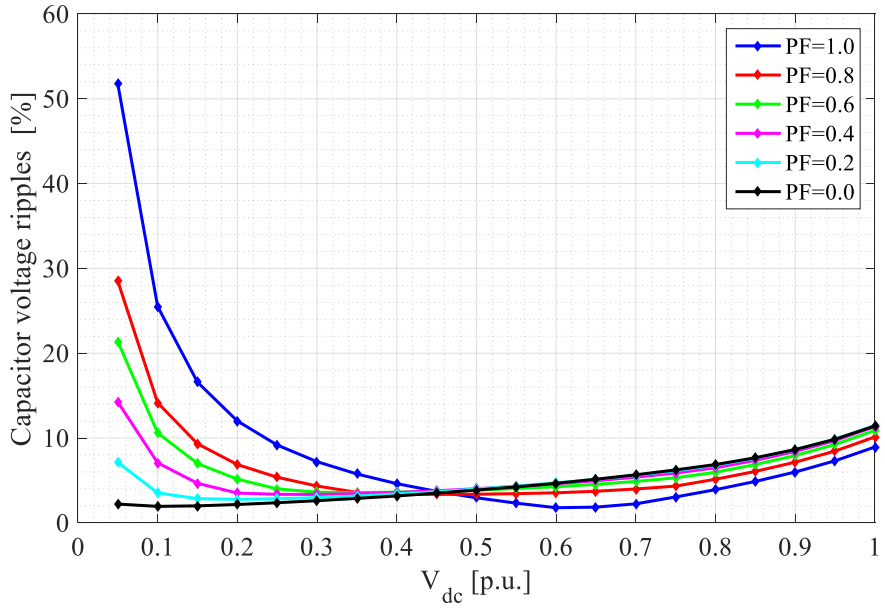


Fig 3.27 Capacitor voltage ripple versus dc link voltage when M_{dc} =[0-1], M_{ac} =1 and V_C defined by (3.16)

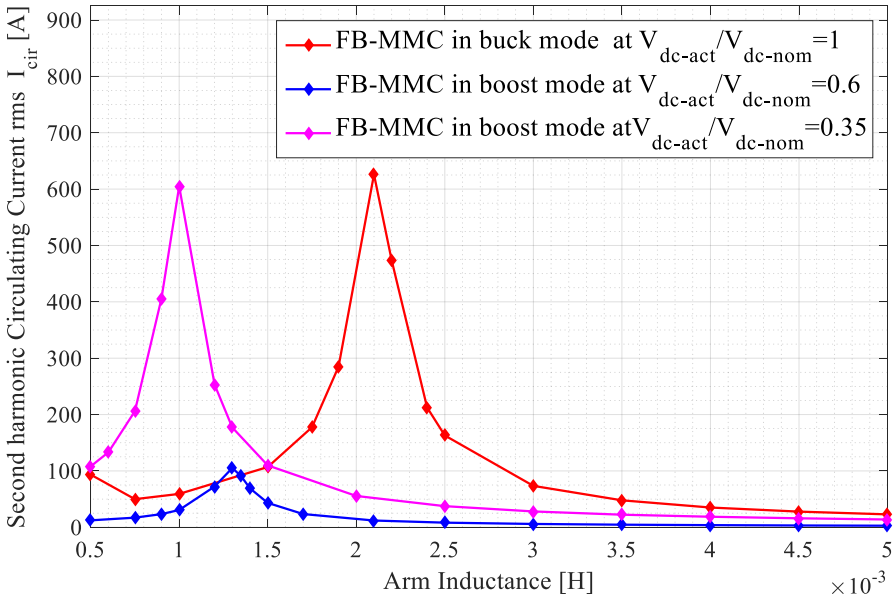


Fig 3.28 Circulating current versus different arm inductances when V_C defined by (3.16)

3.6.1.5 Comparison of the dc capacitor voltage regulation method:

This analysis is undertaken by employing the second capacitor voltage regulation approach, in which voltage V_C is set in accordance with the variations in the dc link voltage and (3.17), and then results obtained are compared to those of the first regulation approach. Of note that the ac modulation index M_{ac} is greater than one when the second regulation approach is used. The simulation results for the circulating current, capacitor voltage ripple and the output voltage THD are shown respectively in Fig 3.29, Fig 3.30 and Fig 3.31. It can be seen that both the circulating current and capacitor voltage ripple increase when the second regulation approach is employed, in particular for the dc link voltages goes below 40% of V_{dc_nom}. On the contrary, the THD of the output voltage is improved for the dc link voltages goes below 70% of V_{dc_nom} and the minimum THD is obtained for 60% of V_{dc_nom}. The time domain results of the output voltage for this operating point are shown in Fig 3.25 and it can be observed that the output voltage has 11 levels. However if $+v_C$ is sets by (3.16) the minimum THD of the output voltage is obtained for a dc link

voltage of 75% of V_{dc_nom} with only 9 voltage levels as shown in Fig 3.23.Of note is that in this analysis, the output power of the FB-MMC is kept at the nominal value, defined by Table 3.1.

Further analysis of the FB-MMC to understand the behaviour of the circulating current at the different levels of the output power is undertaken. Moreover, it is assumed that the output power varies in accordance with the variations in the dc link voltage. The simulation results are shown in Fig 3.32. For this case, the dc link current is fixed at a constant value of 37A, which is determined by the buck mode minimum dc link voltage requirement. The results are obtained for the first regulation approach when V_C is defined by (3.16) and for the second regulation approach when V_C is given by (3.17). The circulating current increases when the second regulation approach is implemented. This current can reach the extreme values, in particular for dc link voltages below 30% of V_{dc_nom}. As a result, the nonlinear behaviour in the circulating current will then affect the capacitor voltage ripple.

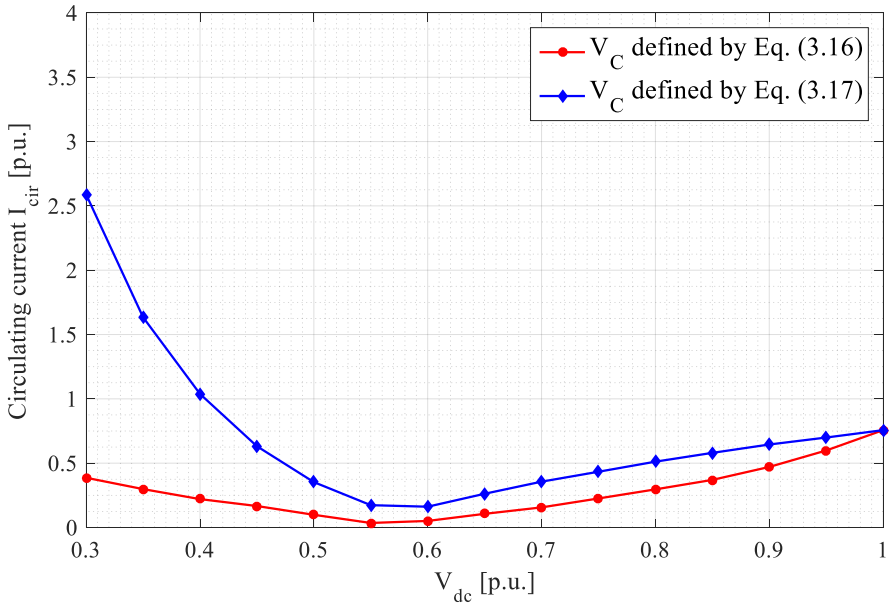


Fig 3.29 Circulating current when the output power is fixed at the nominal value while variation in of the dc link voltage

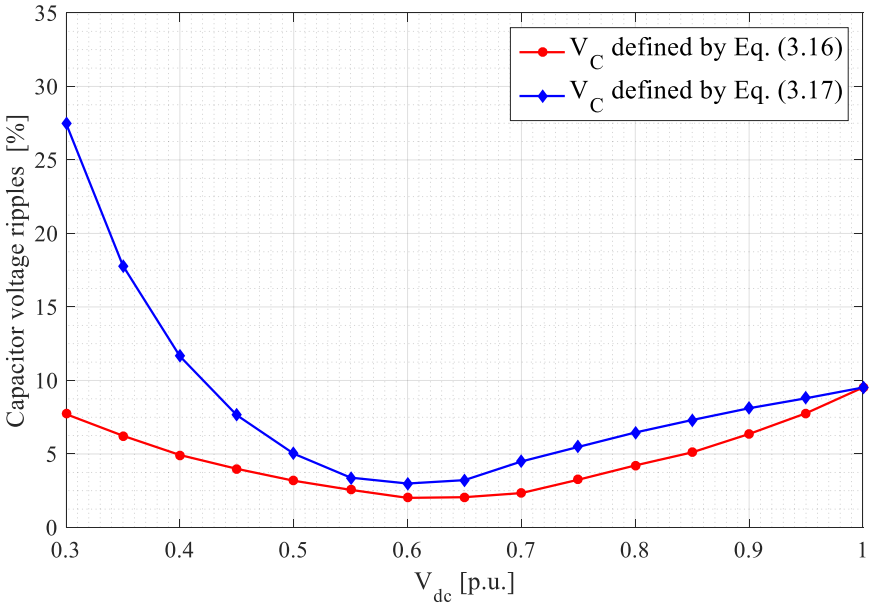


Fig 3.30 Capacitor voltage ripple when the output power is fixed at the nominal value while variation in of the dc link voltage

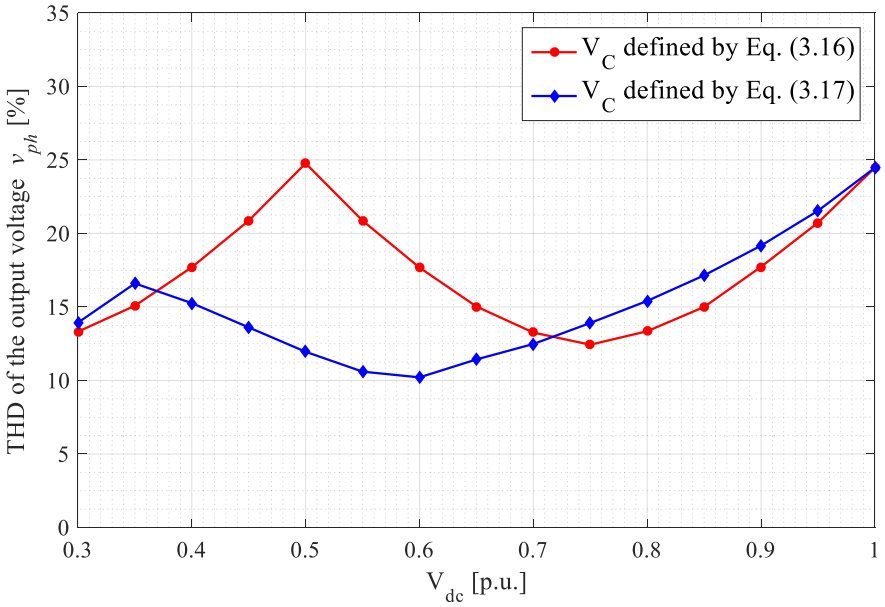


Fig 3.31 THD of the output voltage when the output power is fixed at the nominal value while variation in of the dc link voltage

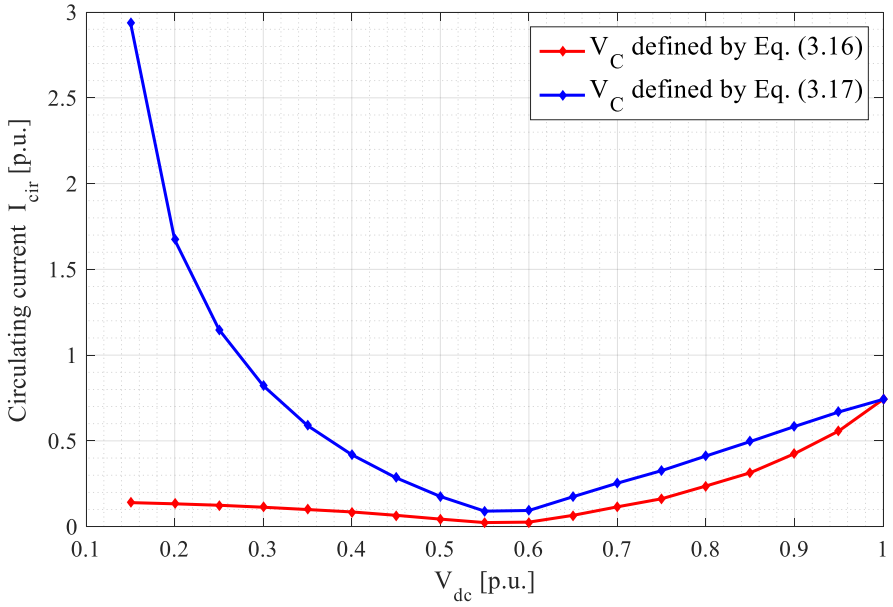


Fig 3.32 Circulating current versus the variation in the dc link voltage when the output power varies

3.6.2 Operation of the grid connected FB-MMC based on the three-phase system:

In order to evaluate performance characteristics of the grid connected FB-MMC when working in the buck and boost modes under different dc link voltage levels, the switching model of the three-phase system based on Fig 3.6 is built-in the MATALB\Simulink environment (see Appendix C). This switching model is modulated with the developed PSC-PWM scheme, and the developed synchronous sampling technique which presented in 3.5.1 is implemented into the control circuits of the FB-MMC. Both closed-loop control as shown in Fig 3.12 and the open-loop mode as shown Fig 3.16 are exploited to generate M_{dc} of each phase, which allows to regulate the capacitor voltage. While generating M_{ac} for each phase is based on the active and reactive power control, which uses the phase locked loop PLL to synchronize the FB-MMC with the grid voltage. Under these operating conditions, the simulation results are presented in terms of the influence of the 2nd harmonic circulating current (without and with its control loop) on the voltage and current quantities of the FB-MMC.

3.6.2.1 The grid connected FB-MMC operating in buck mode when the dc link voltage is fixed at the nominal value.

For this case, the actual value of the dc link voltage is kept constant at its nominal value ($V_{dc\_act} = V_{dc\_nom} = 10$ kV). The FB-MMC is connected to the grid with a line voltage of 6 kV. The phase output current and active power are provided with around 100 A RMS and 1 MW, respectively. In this case, the sampling frequency used for the control circuits is $1/T_{samp} = 8$ kHz which is equal to the effective switching frequency $f_{sw,eff}$ of the FB-MMC. Fig 3.33 shows the 2nd harmonic circulating current waveform while the FB-MMC is connected to the grid in the buck mode. For phase 'a' as an example, it can be observed that the circulating current control minimises the circulating current from 72.5 A to 4.4 A (in RMS

values), that if compared with using the open-loop circuit. It means that i_{cir} is reduced by 93.39 %. For these results, the circulating circuit controller is enabled at the simulation time equal to 0.75 s. Fig 3.34 shows three-phase output voltages and currents of the FB-MMC under the same operating conditions as in Fig 3.33. The output voltages are generated with 5 levels, and THD of the phase output voltages is slightly reduced from 25.7% to 25.2% when the circulating current circuit employed. While a reduction in THD of the phase output current is more significant, which is decreased from 10.8% to 3.1%. The reduced 2nd order circulating current cause capacitor voltage ripple to decrease. With the dc current of 34.36 A, the influence of the i_{cir} minimization can be seen in the upper and lower arm currents of phase 'a' as shown in Fig 3.35. For the voltage ripple of the FB-submodule capacitors, Fig 3.36 shows that the voltage ripple across FB-SM capacitor in the upper and lower arms is reduced from 8.8% to 3.28% after the circulating current control enabled. Regarding these results of the gird connected FB-MMC, it can be concluded that circulating current control is necessary at the buck operating point.

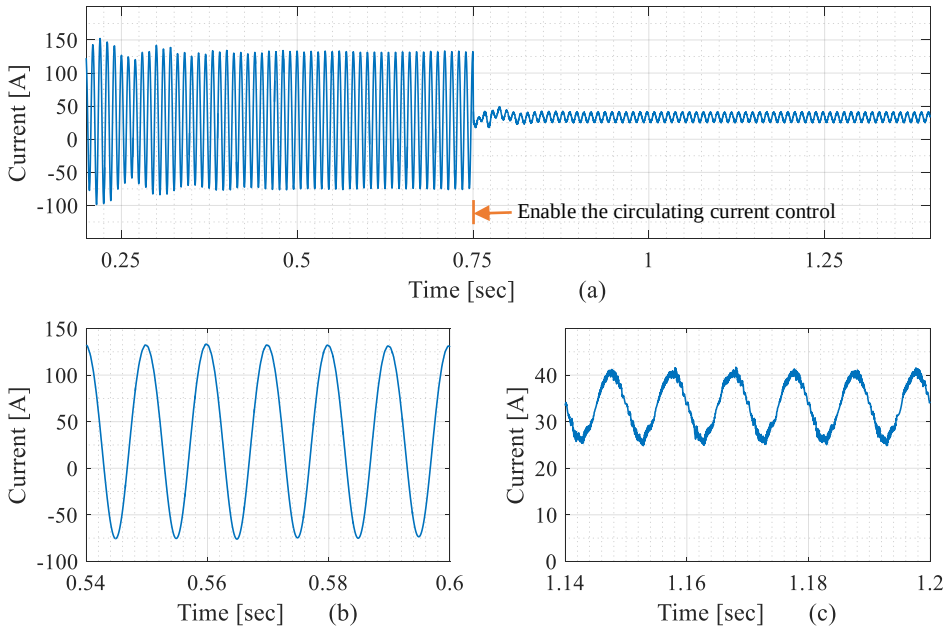


Fig 3.33 (a) The 2nd order circulating current waveform while FB-MMC operating in the buck mode at $V_{dc\_act} = V_{dc\_nom}$, (b) Zoomed portion of (a) when the average control is set as open-loop, (c) Zoomed portion of (a) when the average control is set as closed-loop

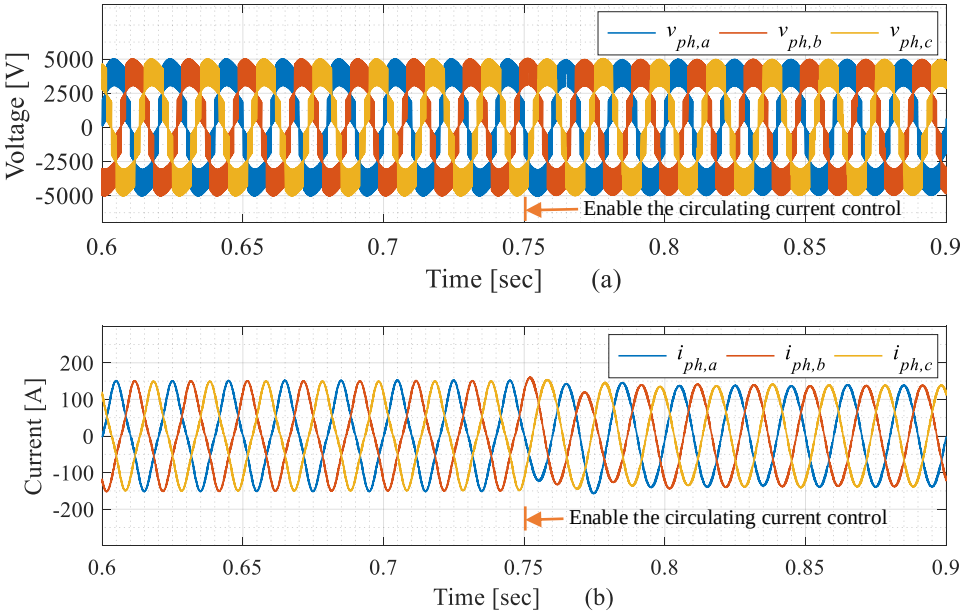


Fig 3.34 Output voltage and current waveforms of the FB-MMC works in buck mode when $V_{dc\_act} = V_{dc\_nom}$, (a) Three phase output voltages, (b) Three phase output currents

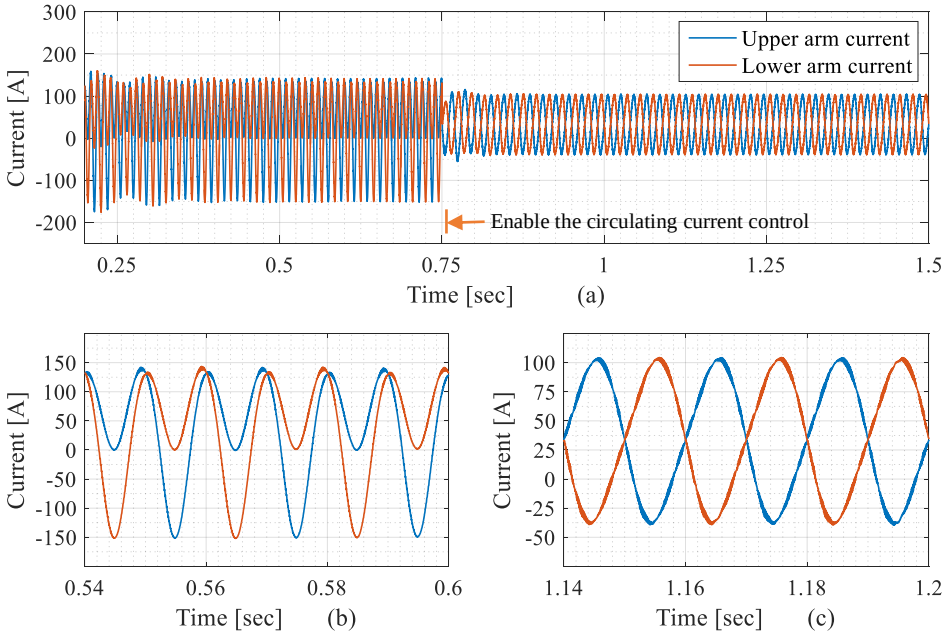


Fig 3.35 (a) The upper and lower arm currents while FB-MMC operates in buck mode at $V_{dc\_act} = V_{dc\_nom}$, (b) Zoomed portion of (a) when the average control is set as open loop, (c) Zoomed portion of (a) when the average control is set as closed-loop

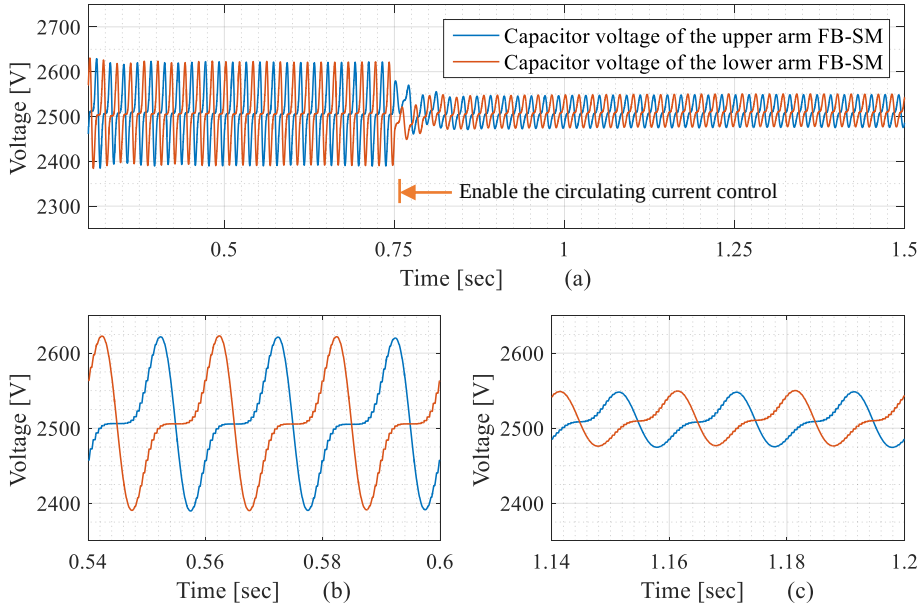


Fig 3.36 (a) The capacitor voltages for FB-SMs in upper and lower arms when operating in buck mode, at $V_{dc\_act} = V_{dc\_nom}$ (b) Zoomed portion of (a) when the average control is set as open loop, (c) Zoomed portion of (a) when the average control is set as closed-loop

3.6.2.2 The grid connected FB-MMC operating in the boost mode when the dc link voltage is fixed at 60% of its nominal value

For this case, both the two regulation approaches for FB-submodule capacitor voltages are examined for the case when the actual level of the dc link voltage operates at 60% of its nominal value V_{dc_act} = 0.6 V_{dc_nom}, and $1/T_{samp} = 8$ kHz s. According to the results in Fig 3.26. This level of the dc link voltage can be considered as an optimal operating point, as regarding the circulating current value. In this study, the output current is kept around 100 A in RMS the aim of this study is that to show an impact of the boost operating mode on the 2nd order circulating current compared to the buck operating mode. In the first regulation approach, the capacitor voltages for all FB-submodules are adjusted to around 2.5 kV based on (3.16). According to Fig 3.37, it can be seen that the 2nd order harmonic circulating current is reduced to 4.9 A (RMS) when no circulating current control employed. The decrease in the circulating current is about to 93.25% compared to the buck

operating mode. Moreover, it can be seen that when circulating current control is enabled, i_{cir} is only slightly further reduced. It means that the designed circulating current control has less impact at this dc link voltage level. For both control loops, Fig 3.38 shows three-phase output voltages and currents of the FB-MMC under the same condition in Fig 3.37. Note that the output voltages are generated with 9 levels and THD of around 15.6%. It can be observed that the interleaving at this operating point is not at an optimum of the circulating current control. For THD of the output currents, they are around 2.75%. The impact of the circulating current control on the arm currents for phase 'a' is shown in Fig 3.39. Note that the dc current increases from 34.36 to 54.8, that when the dc link voltage is at 60% of nominal value and the output power is kept at the fixed value. From Fig 3.40, voltage ripple across the FB-submodule capacitor in the upper and lower arms is around 1.5%, and it reduces 1.28% when FB-MMC operating in the open-loop mode. It can be concluded from these simulation results that the 2nd order harmonic circulating current is minimised at this operating point without employing the circulating current control.

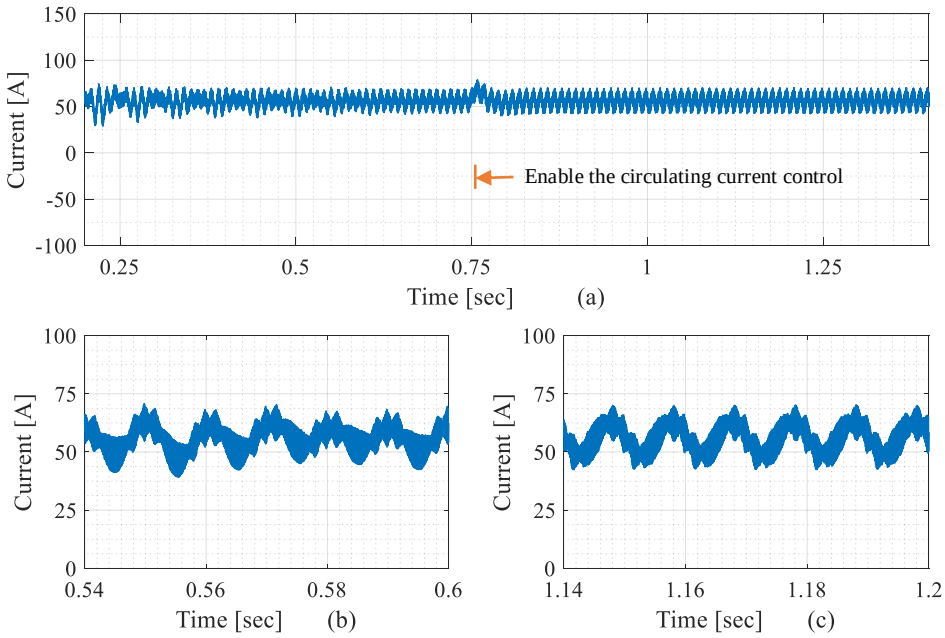


Fig 3.37 (a) The 2nd order circulating current while FB-MMC operating in the boost mode at $V_{dc\_act} = 60\%$ of V_{dc_nom} and V_C defined by (3.16), Zoomed portion of (a) when the average control is set as open loop, (c) Zoomed portion of (a) when the average control is set as closed-loop

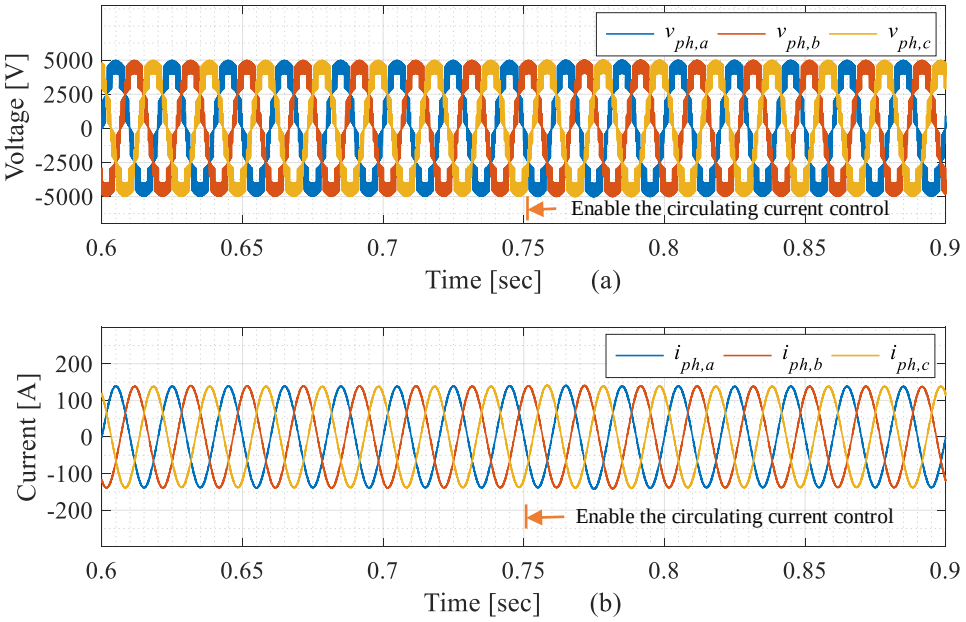


Fig 3.38 Output voltages and current waveforms of the FB-MMC works in the boost mode at $V_{dc\_act} = 60\%$ of V_{dc_nom} and V_C defined by (3.16), (a) Three phase output voltages, (b) Three-phase output currents

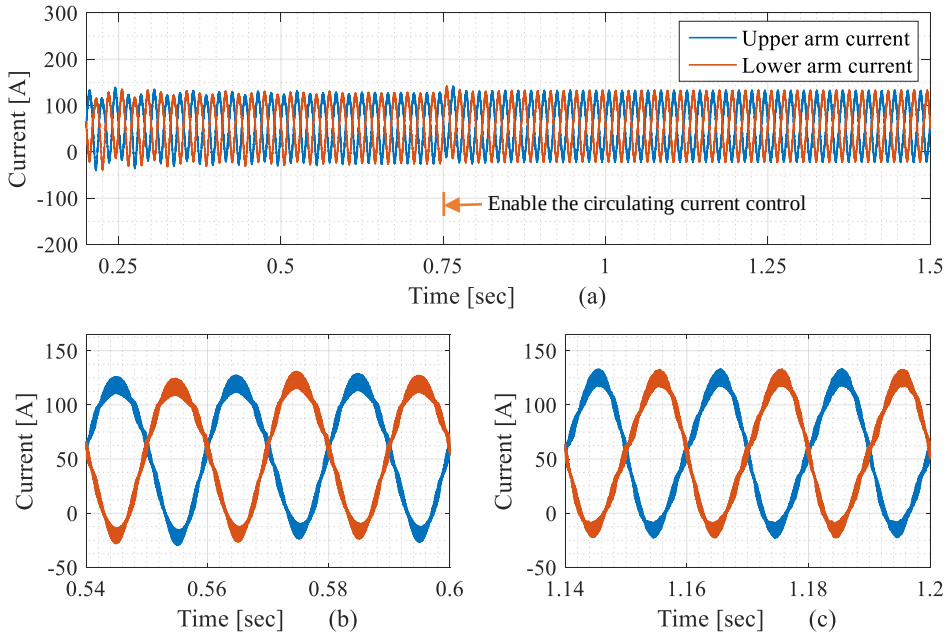


Fig 3.39 (a) Upper and lower arm currents while FB-MMC operating in the boost mode at $V_{dc\_act} = 60\%$ of V_{dc_nom} and V_C defined by (3.16), (b) Zoomed portion of (a) when the 2nd circulating current control is disabled, (c) Zoomed portion of (a) when the 2nd circulating current control is enabled

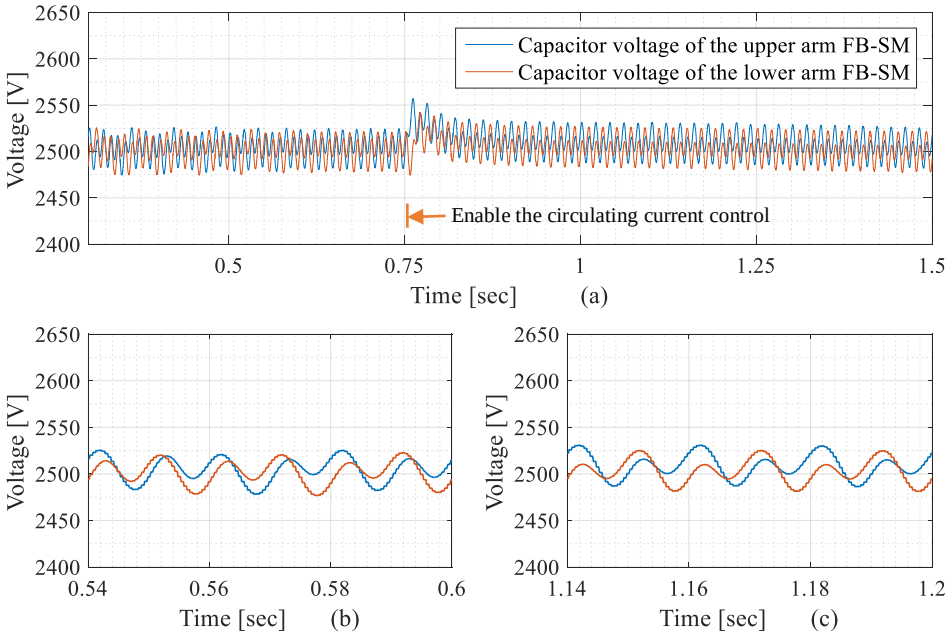


Fig 3.40 Capacitor voltages for FB-SMs in upper and lower arms when operating in the boost mode at $V_{dc\_act} = 60\%$ of V_{dc_nom} and V_C defined by (3.16), (b) Zoomed portion of (a) when the average control is set as open loop, (c) Zoomed portion of (a) when the average control is set as closed-loop

However, for the second regulation approach defined by (3.17), the capacitor voltages for all FB-submodules is reduced from 2.5 kV to around 2 kV. For this study, the actual dc link voltage and output currents are kept at the same values as for the tests shown in Fig 3.37-Fig 3.40. In the open-loop mode, Fig 3.41 shows that the 2nd order circulating current is decreased to 11.3 A (RMS). As compared to the buck operating mode, the reduction in the circulating current is about to 84.5.4%. Otherwise, this reduction is reached to 90.8% when the circulating current control employed. Fig 3.42 shows both three-phase output voltages and currents of the FB-MMC. As the interleaving at this operating point occurs the optimal point compared to the first regulation approach, the output voltages are obtained with 11 level and THD of around 9.1%. However, THD of the output currents is decreased from 3.9% to 2.9% when the circulating current control is enabled. The influence of i_{cir} minimization on the upper and lower arm currents is shown in Fig 3.43.it can be seen that dc current increases to 55.4. The capacitor voltage of FB-submodule of

upper and lower arms show the ripple factor of 3.25% in the open-loop. When enabling the closed-loop circuit is enabled, the ripple factor is reduced to 2.15% as illustrated in Fig 3.44. It can be observed that the switching ripples are superimposed to circulating and both arm currents, that because of the interleaving between the output voltages of the FB-submodules in the upper arm and those of the lower arm.

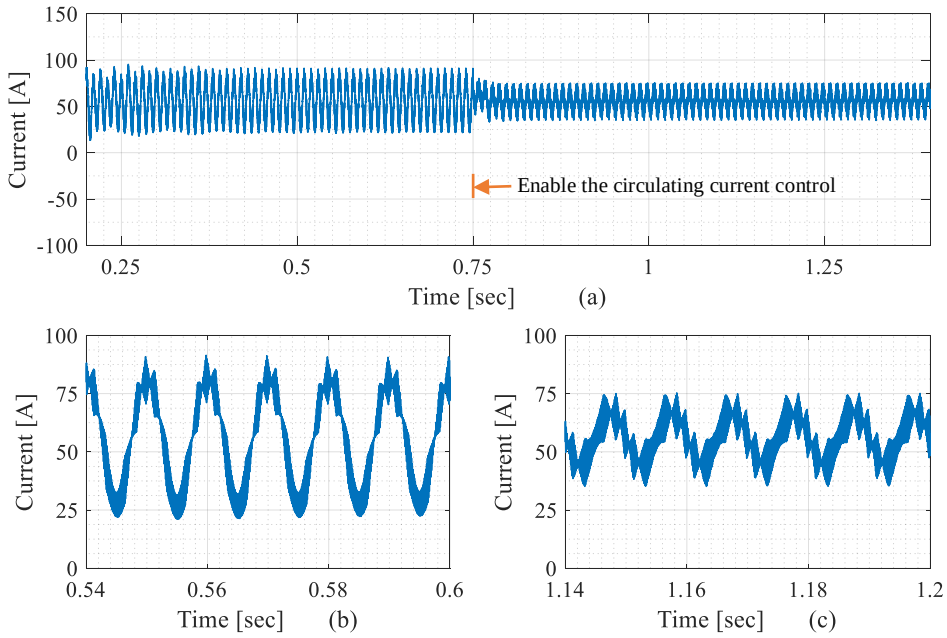


Fig 3.41 (a) The 2nd order circulating current while FB-MMC operating in the boost mode at $V_{dc\_act} = 60\%$ of V_{dc_nom} and V_C defined by (3.17), Zoomed portion of (a) when the average control is set as open loop, (c) Zoomed portion of (a) when the average control is set as closed-loop

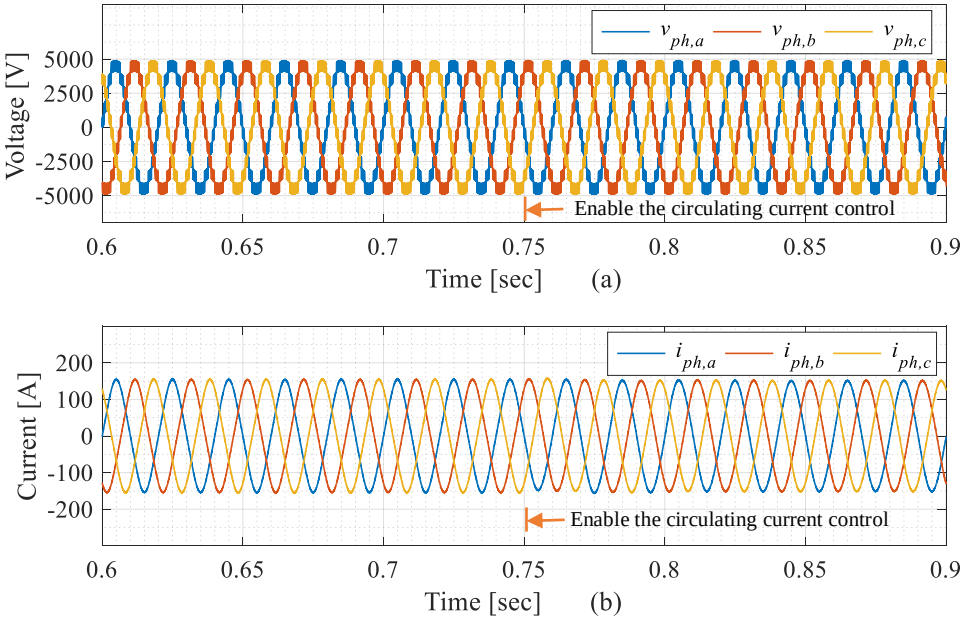


Fig 3.42 Output voltages and current waveforms of the FB-MMC works in the boost mode when $V_{dc\_act} = 60\%$ of V_{dc_nom} and V_C defined by (3.17), (a) Three phase output voltages, (b) Three-phase output currents

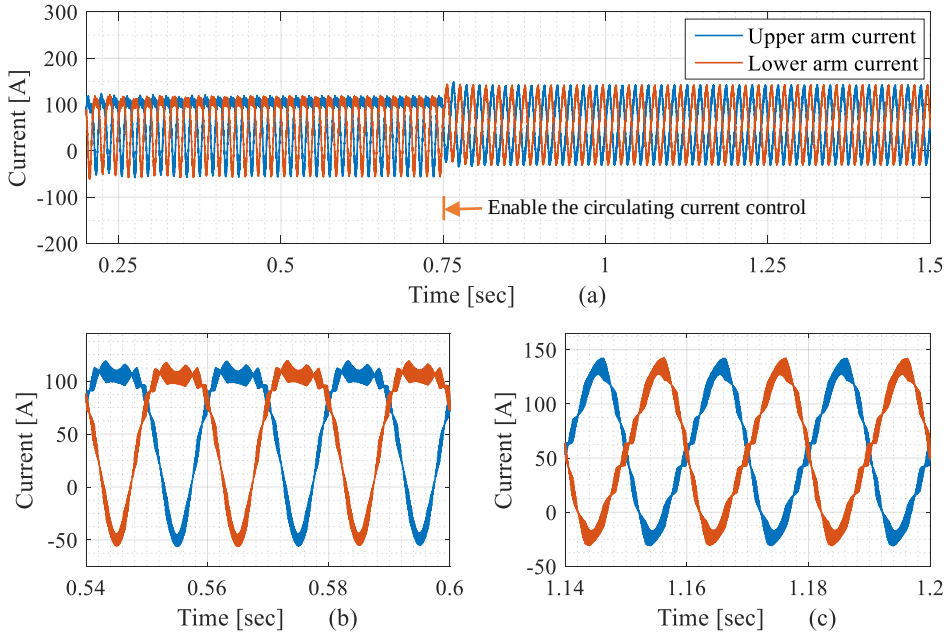


Fig 3.43 (a) (a) Upper and lower arm currents while the FB-MMC operating in the boost mode at $V_{dc\_act} = 60\%$ of V_{dc_nom} and V_C defined by (3.17), (b) Zoomed portion of (a) when the average control is set as open loop, (c) Zoomed portion of (a) when the average control is set as closed-loop

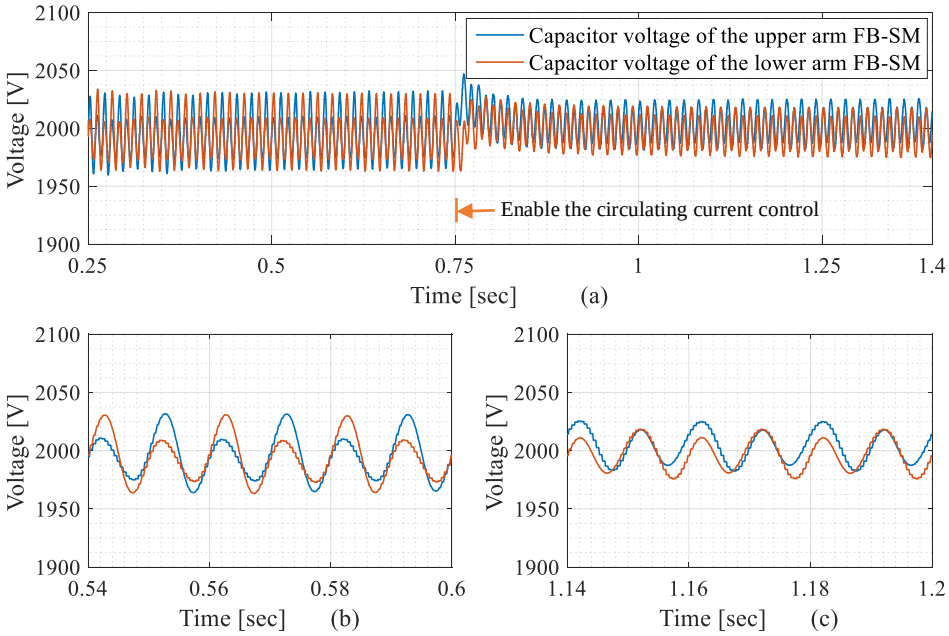


Fig 3.44 Capacitor voltages for FB-SMs in upper and lower arms when operating in the boost mode at $V_{dc\_act} = 60\%$ of V_{dc_nom} and V_C defined by (3.16) 3.17), (b) Zoomed portion of (a) when the average control is set as open loop, (c) Zoomed portion of (a) when the average control is set as closed-loop

3.6.2.3 The grid connected FB-MMC operating in the boost mode while the dc link voltage is varying

The FB-MMC, which is discussed before, can be utilised to interface the grid with the variable speed direct driven wind generation system, as shown in Fig 3.45 [10], [36]. Due to the absence of the gearbox, the type of this generation system can significantly be improved by employing the multi-pole permanent magnet synchronous generator PMSG. Thus, it can operate at high efficiency with low speed of operation. Also, when a diode rectifier is employed, the generator side can operate with close to unity power factor operation [10],[8],[12]. As the PMSG is directly coupled with the wind turbine, the dc link voltage of this wind generation system varies according to time-varying generator speed.

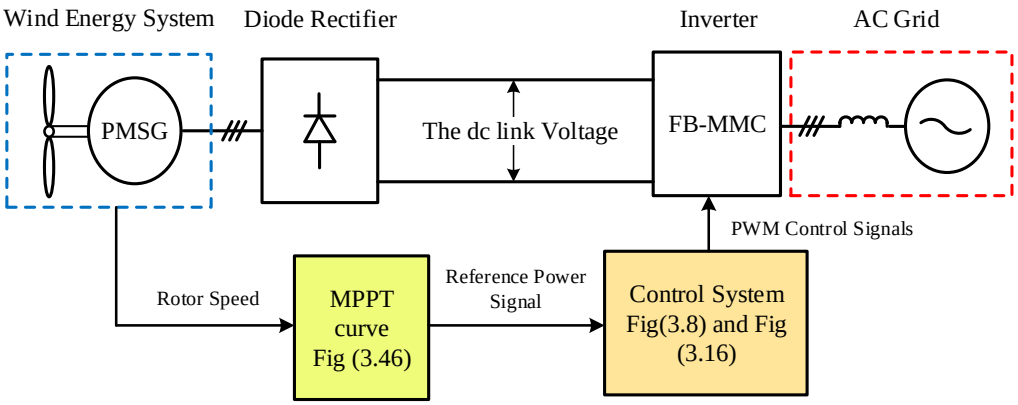


Fig 3.45 Feasible circuit conversation for variable speed direct drive of WECS

The MPPT curve used in the PSF method represents a maximum output active power which obtained at the corresponding rotor speed of the PMSG. The data points of the MPPT curve can first be acquired from simulation or off-line experiment results, and then recorded in a lookup table [35], [36]. Here, the output active power is sent as a reference signal to the control system of the grid connected FB-MMC. Actual value of the output active power of the FB-MMC is controlled by adjusting M_{dc} through the PI controllers [6], [39], [40]. Note that the output reactive power of the FB-MMC is adjusted to be zero. As demonstrated in Fig 3.46. The behaviour of the wind turbine can be classified into three modes of operation. The first region is a parking mode that when wind turbine speed is less than the cut-in speed. As the generated power is too small in this mode, it can be considered as zero. In the second region, the wind turbine speed mode covers the range from higher than the cut-in speed to the rated speed. For this mode, the maximum power generated is obtained from the MPPT curve under the rated speed of operation. The third region describes the wind turbine speed mode in which the speed ranges from the rated speed to the cut-out speed. For this mode, the power generated is restricted to the rated value, even if the wind speed goes higher than the rated value. That can be achieved by adjusting a pitch angle of the wind turbine. Note that the cut-in and cut-out speeds, respectively, denote to a minimum and maximum speeds provided by the wind energy systems.

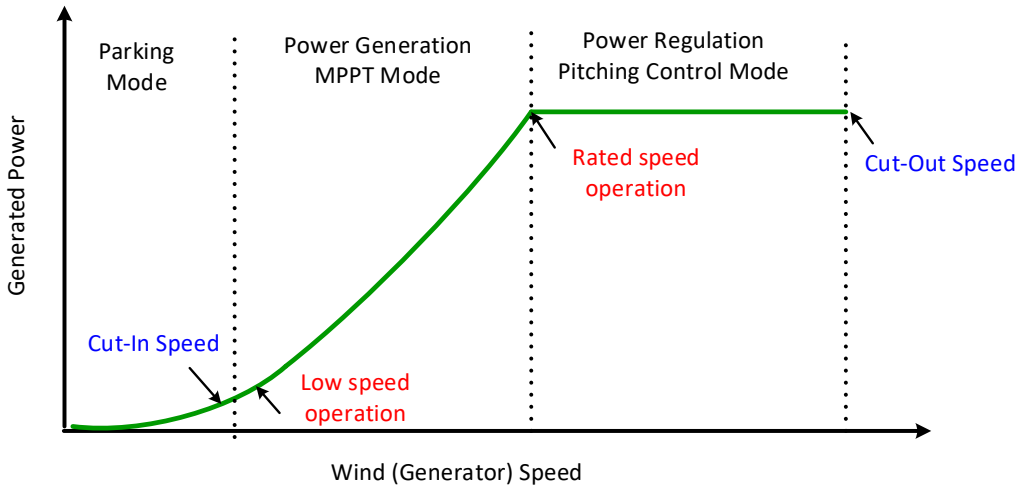


Fig 3.46 Typical behaviour of wind turbine speed

3.6.2.3.1 Operating under constant dc capacitor voltage

In order to emulate the time-vary wind turbine speed (power generated) in this study, the dc link voltage is adjusted to cover the range of (10kV-100V). For simplicity, it is assumed that the dc link voltage with the nominal value of 10 kV refers to the PMSG when operates at the rated speed of operation, while the dc link voltage value of 100 V is set as the PMSG operates at low speed of operation. Note that fluctuation in the dc link voltage due to the diode rectifier is neglected in this work, as shown in Fig 3.47 (a). For this case, the FB-MMC starts to operate from the buck mode to the boost mode, that when V_{dc_act} goes down from 10 kV at time = 0.5 sec. Fig 3.47 (b) shows three-phase output voltages while the FB-MMC is connected to the grid with the line to line voltage equal to 6 kV. The maximum output voltage level of nine is obtained, while the minimum level is five. Fig 3.48 (a) shows the capacitor voltages of all FB-submodules regulated to the nominal value of 2.5 kV according to (3.16). As shown in Fig 3.48 (b), the FB-submodule is inserted at the positive voltage of +2.5 kV and the zero when buck mode before 0.5 sec. Besides, the insertion at the negative voltage of -2.5 kV is achieved after time 0.5 sec. It can be observed that the time interval of negative voltage state increases

as the V_{dc_act} decreases. Because the output currents (generated power) are associated with the time-vary wind turbine speed, these currents decrease the dc link voltage decreases, as shown in Fig 3.49 (a). In the reference and actual values, the active and reactive powers are presented in Fig 3.49 (b). Under the variation of the dc link voltage defined in Fig 3.37, it can be seen that the actual value of each the active and reactive powers is exactly able to track to its reference value, in which the sampling frequency ($1/T_{samp} = 8$ kHz) is implemented. In this case, that active power P_{con} is reduced from 1 MW to around 9.6 kW, while the reference reactive power Q_{con} is kept around zero.

3.6.2.3.2 Operating under varying dc capacitor voltage

Further, the second approach employed in this work to regulate the capacitor voltage based on (3.17). It is used to study the characteristic of the grid connected FB-MMC. Under the same operating conditions, as shown in Fig 3.47-Fig 3.49. Fig 3.50 shows the three-phase output voltages are generated with more levels which are 9,11,13,15, which are related to the actual value of V_{dc_act}. Based on (3.17), the capacitor voltage in Fig 3.51 (a) varies from 2.5 kV to 1.3 kV with respect to V_{dc_act}, as compared with results in Fig 3.47. Each FB-submodule in the boost mode is inserted either at the negative or positive voltage levels of the reduced dc capacitor voltage, and at zero voltage when FB-SM is bypassed as shown in Fig 3.51 (b). The decrease in three output currents is achieved from about l00 A to 0.25 A RMS as displayed in Fig 3.52 (a). The sampling frequency of this case is ($1/T_{samp} =$ 16 kHz s) which is taken as twice effective switching frequency. That to consider a fast dynamics of the reference value V_C^* when changes with respect to the dc link voltage. Even if all the dc capacitor voltages vary at the same time as the dc link voltage variation, it can be seen that the tracking of the active power P_{con} to its reference value P_{con}^* is acceptable, as shown in Fig 3.52 (b). The reactive power Q_{con} of this system is also kept around zero during the variable dc link voltage.

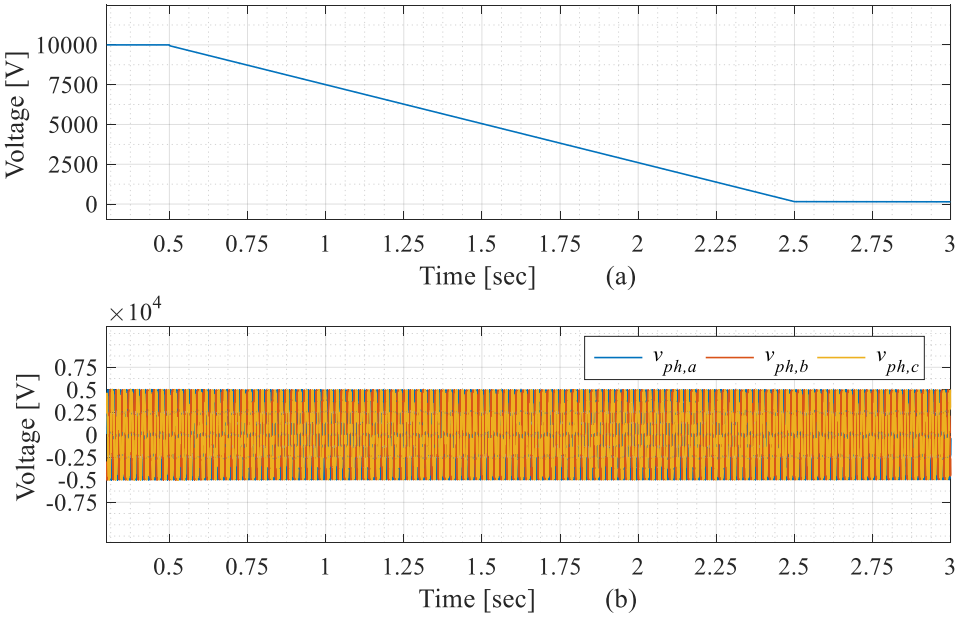


Fig 3.47 Variation in the dc link voltage when V_C is defined by (3.16): (a) V_{dc_act} varies from 10 kV to 100 V, (b) Three phase output voltges at the same operational conditions

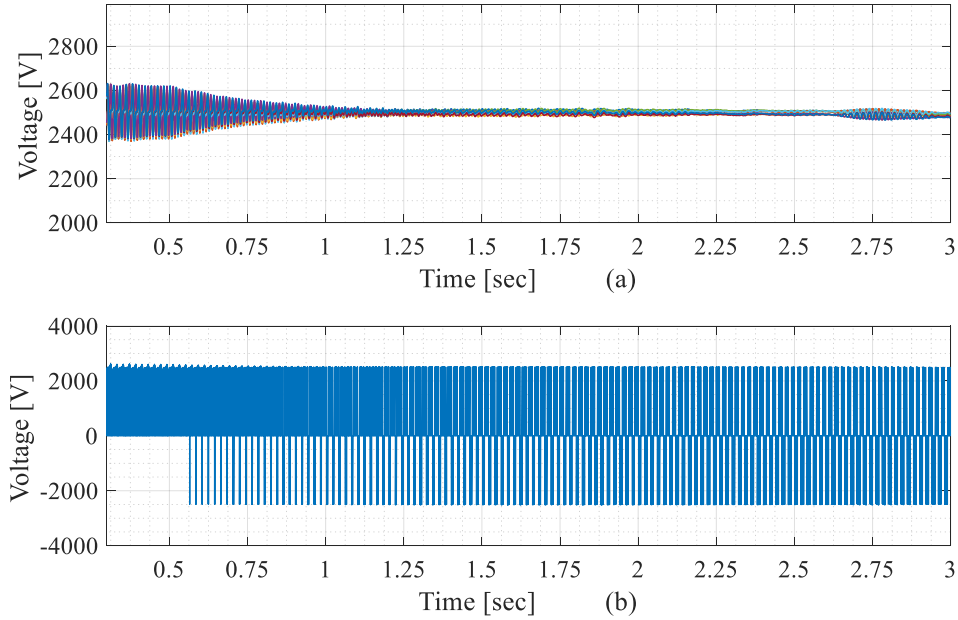


Fig 3.48 (a) Capacitor voltages of all FB-submodules regulated by (3.16) under varying dc link voltage, (b) Output voltage of one FB-submodule in the upper arm under the same operational conditions

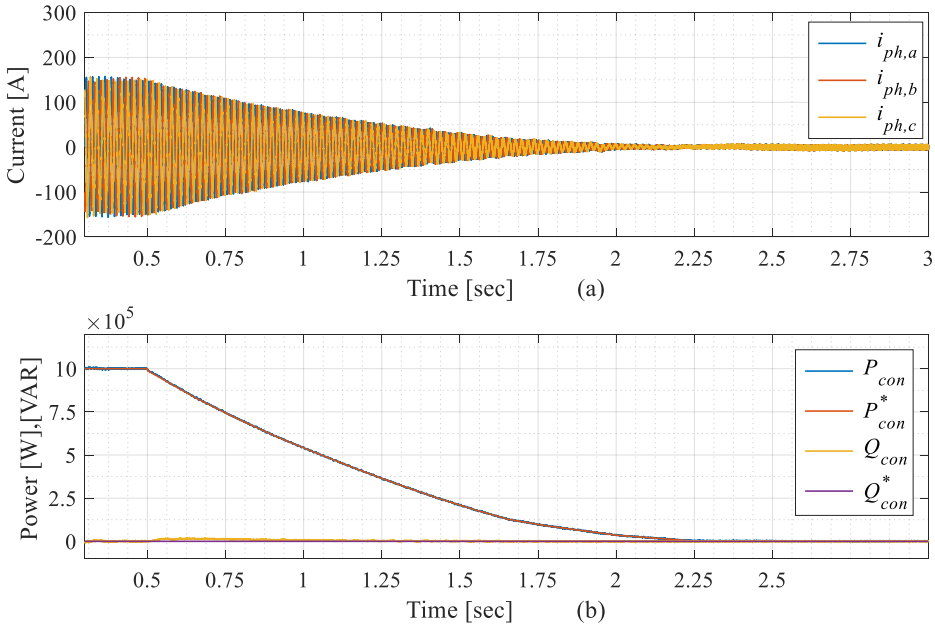


Fig 3.49 (a) Three-phase output current when under varying dc link voltage when V_C is defined by (3.16), (b) Active and reative powers exchange under the same operational conditions

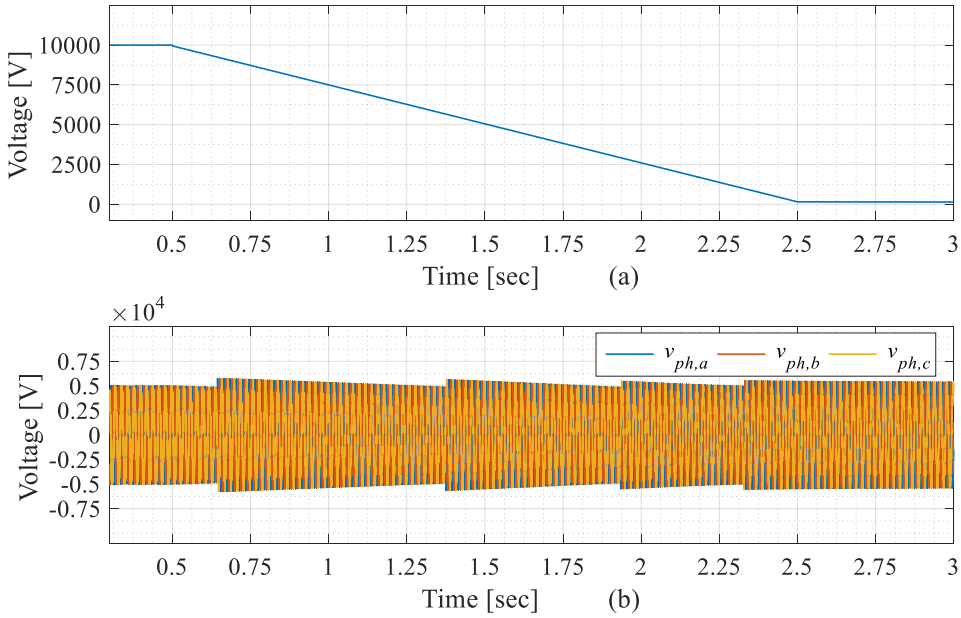


Fig 3.50 Variation in the dc link voltage when V_C is defined by (3.17): (a) V_{dc_act} varies from 10 kV to 100 V, (b) Three-phase output voltages at the same operational conditions

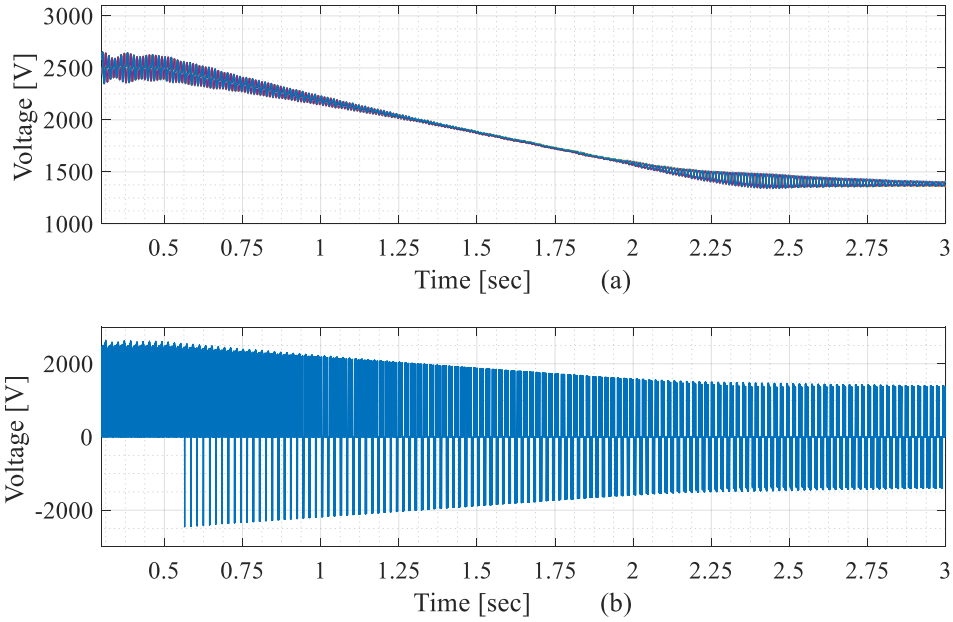


Fig 3.51 (a) Capacitor voltages of all FB-submodules regulated by (3.17), under varying dc link voltage, (b) Output voltage of one FB-submodule in the upper arm under the same operational conditions

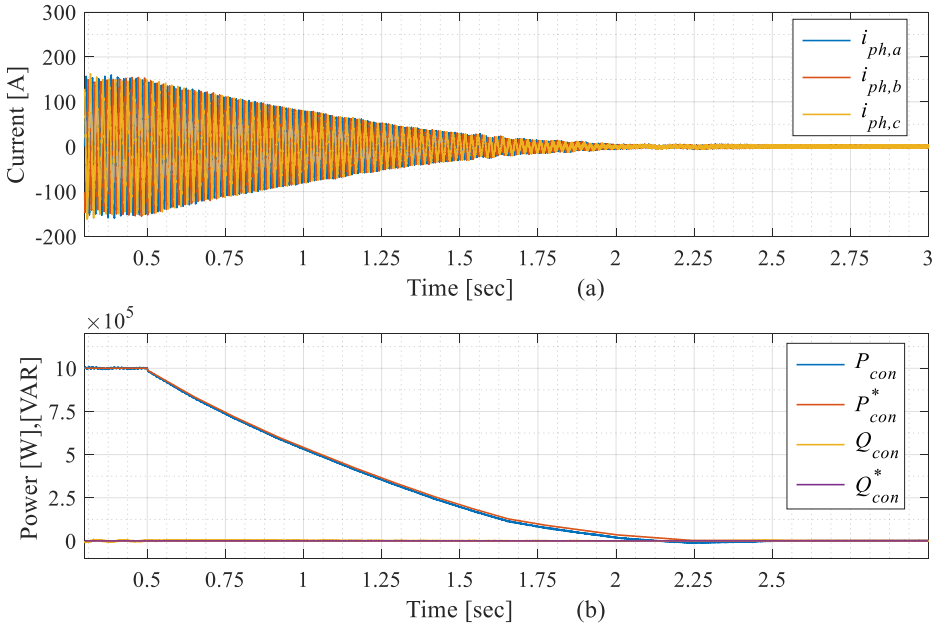


Fig 3.52 (a) Three-phase output current when under varying dc link voltage when V_C is defined by (3.17), (b) Active and reative powers exchange under same operational conditions

3.7 Chapter summary

In this chapter, the FB-MMC has been presented and analysed as a possible technical solution to the grid connected converter for the integration of WECS. The main feature of the FB-MMC when it is operated either in buck mode or boost mode is studied and discussed, in order to address an issue that is related to the variation in the dc link voltage. The main objective of this chapter was to analyse the influence of the dc link level on the circulating current, capacitor voltage ripples and THD of the phase output voltage and to investigate the optimal operation of the FB-MMC in the boost mode. The PSC- PWM strategy was developed in this work by determining of modulation parameters. Whereas the ac and dc modulation indexes are used to specify the operation of the FB-MMC in the buck and boost modes, in which the dc link voltage varies in the range of [0-V_{dc_nom}]. The single-phase FB-MMC switching model was first implemented using open-loop mode, that is to validate the effectiveness of the developed PSC-PWM. Under these operating conditions, two different regulation approaches for the FB-submodule capacitor voltages were analysed and compared. Of note that the dc capacitor voltage in the first approach was regulated at the nominal value defined by the grid voltage. While the second approach regulates the dc capacitor voltage according to the variations in the dc link voltage. The main contribution is that the 2nd order circulating current was minimized without using the circulating current suppression control, in which the FB-MMC operates in the boost mode at 60% of the nominal dc link voltage. As a result, the capacitor voltage ripples were reduced. Therefore, it gives a possibility to considerably decrease the capacitor size at this optimal operating point in the boost mode. In addition, obtained shows that the lower range of the dc link voltage, the circulating current and capacitor voltage ripple can also be decreased by operating the system at a low power factor. For design considerations, results exposed that different resonant inductances can also be obtained. It also showed that THD of the output voltage is highly dependent on the level of the dc link voltage when the FB-

MMC operates in the boost mode due to the interleaving effect. While connected to the grid, this switching model of the FB-MMC has been extended to the three-phase system. Where closed-loop control systems employed were first optimised depending on the synchronous sampling technique. control systems were then used to validate the proposed modulation strategy. Then one of these control systems was employed to control the output active and reactive powers while the second control system was used to minimise the 2^{nd} harmonic circulating current and to regulate dc capacitor voltage of FB-submodules. The performance analysis of the FB-MMC in the buck and boost operating modes was verified through results obtained from the simulated models.

Chapter 4: Steady-State Analysis of the Full Bridge Modular Multilevel Converter Operating in Buck and Boost Modes

4.1 Introduction

This chapter develops the steady-state analytical mode for the full bridge modular multilevel converter FB-MMC, the modelling is analysed in details based on the single-phase system. That can also be extended to the three-phase system. The developed steady-state analytical model is valid for the FB-MMC operating in both buck and boost modes. The boost mode is achieved in this analysis by setting different levels of the dc link voltage, while FB-MMC is connected to the stiff grid. Under these operating condition, the developed analytical modelling allows describing low order harmonics in the arm currents, submodule capacitor currents, submodule capacitor voltages, submodule output voltages, arm voltages, and output voltage of FB-MMC. In addition, this developed analytical model provides an amplitude and phase angle of the circulating current. The developed analytical model is general and can be used for the two different dc capacitor voltage regulation strategies, which employed in this research work and discussed in Chapter 3. The first strategy regulates the dc capacitor voltage to the nominal value set by the dc voltage requirement of the grid connected FB-MMC in the buck mode. While in the second strategy, the dc capacitor voltage varies according to the different levels of the dc link voltage. In the boost mode, the results of this analysis show that the circulating current and voltage ripples across the FB-SM capacitors can be minimised without circulating current control when FB-MMC works at specific levels of the dc link voltage. The FB-MMC switching model based on the single-phase system is built-in MATLAB/Simulink, that is to validate the developed analytical model. The obtained results of the FB-MMC switching model are compared to those of the steady-state analytical model.

4.2 Average model representation of the FB-MMC

An average model representation of the FB-MMC can be useful in terms of the investigation into the steady-state analysis of the FB-MMC. It allows describing harmonic behaviour under different operation conditions. In the case of the average model, the submodules are generally modelled without modelling switching power devices. Instead of, each arm consists of the controlled voltage sources, that to represent the equivalent sum of the output voltages of all submodule in the cascaded connection. Hence, the controlled sources determine a relation among voltages and currents of the submodules depending on the average switching function of each arm [30],[69]. In this work, the average model of the FB-MMC is exploited to understand complex system harmonics behaviour in the buck and boost modes of operation. Based on the single-phase FB-MMC circuit configuration shown in Fig 3.1, the schematic of the FB-MMC average model is shown in Fig 4.1.

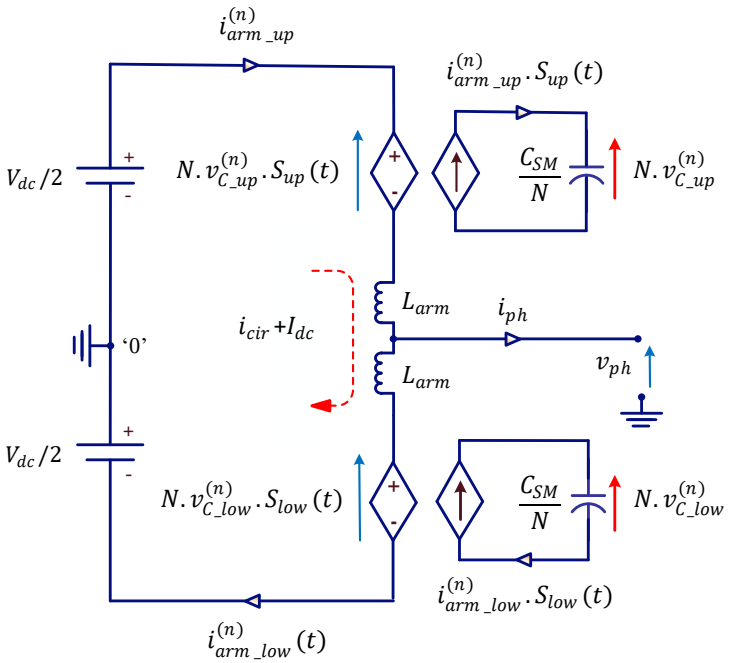


Fig 4.1 Schematic of the single-phase FB-MMC based on the average model representation

4.3 Steady-state analysis of the FB-MMC

This research work develops a steady-state analytical model of the FB-MMC, which effectively reveals how the operation in both buck and boost modes influences harmonic behaviours of the FB-MMC, in particular, the 2nd harmonic circulating current. This current is considered as an inherent issue related to efficiency, circuit parameter design and control performance of the FB-MMC. Therefore, the developed steady-state analytical model can be beneficial for power loss calculation [110], [97] and submodule capacitor and arm inductor sizing [66], [111]. Also, this study can be utilised to enhance control strategies for reducing submodule capacitor ripple by minimising or injecting of the 2nd order circulating current [69], [112]. In reference [68], the steady-state analysis is introduced based on a circular interaction among various electrical quantities in MMC. It can explicitly express the relation among harmonic components of the submodule capacitor and arm voltages and currents in the HB-MMC. In [68], expressions for amplitude and phase angle of the 2nd harmonic circulating current are also provided.

In this work, however, the steady-state analysis is developed for the grid connected FB-MMC. Based on the above mentioned circular interaction, the steady-state analytical model is developed by employing the modulating signals developed and presented in section in 3.3. In this analysis, expressions for amplitude and phase angle for the FB-MMC operating in the buck and boost modes are provided.

Some assumptions in this work are made to simplify the steady-state analysis of the FB-MMC, which are as follows:

- The FB-MMC operates in this work in inverter mode. Thus the power is transferred from the dc side to the ac side of the converter, and power losses are neglected. However, this analysis is also valid for bidirectional power flow.

- The steady-state analysis is established by considering the open-loop control. Thus, this steady-state analysis does not include the impact of the circulating current suppression control.

- It is assumed that all FB-submodules are identical. Thus the output voltages of the FB-submodules are equally generated with relating to the amplitude and phase angle.
- Voltages across the FB-submodule capacitors are the same and self -balanced.
- Moreover, the PWM waveforms of the output voltage of FB- submodules and the capacitor currents are represented with the averaged values (i.e. harmonics with high frequency are ignored).

Considering the above assumptions, the developed steady-state model of the FB-MMC can provide in the time-domain expressions for low order harmonic components of FB-MMC arm currents and voltages, FB-submodule capacitor voltages, and output phase voltages. The analysis also includes the calculation of the 2nd harmonic circulating current amplitude and phase angle. This analysis is presented in the following sections.

4.3.1 Calculation of the arm currents in the FB-MMC

On the basis of the circular interaction, as firstly presented in [68], the steady-state modelling should be established first from the arm currents. For the grid connected FB-MMC, it can be assumed that both upper and lower arm currents are essentially composed of three components which are: the dc component current, load (fundamental) current and the circulating current with the dominant 2nd order harmonic [68]. As the steady-state analysis is established using the single-phase system, the upper and lower arm currents can be given in according to [68] as follows:

$$\begin{aligned} i_{arm\_up}^{(n)}(t) &= i_{arm\_up}^{(0)}(t) + i_{arm\_up}^{(1)}(t) + i_{arm\_up}^{(2)}(t) \\ &= I_{dc} + \frac{I_m}{2}\sin(\omega_0 t + \theta) + I_{cir}\sin(2\omega_0 t + \varphi_{cir}) \end{aligned} \tag{4.1}$$

$$
\begin{aligned}
i_{arm\_low}^{(n)}(t) &= i_{arm\_low}^{(0)}(t) + i_{arm\_low}^{(1)}(t) + i_{arm\_low}^{(2)}(t) \\
&= I_{dc} - \frac{I_m}{2}\sin(\omega_0 t + \theta) + I_{cir}\sin(2\omega_0 t + \varphi_{cir})
\end{aligned} \tag{4.2}
$$

In this research work, n refers to the harmonic order. The dc component in the arm currents (at $n = 0$) is represented by I_{dc}. The I_m denotes the peak value of the load current(at $n = 1$), and the load (power factor) angle is denoted by θ. While the amplitude and phase angle of the circulating current (at $n = 2$) is expressed by I_{cir} and φ_{cir} respectively. It is observed that half of the load current in the ac side flows within each arm but in the opposite direction [68], [113]. In order to calculate the dc component current I_{dc} at different levels of the dc link voltage V_{dc_act}, it can be considered that the power in the dc side P_{dc} and that in the ac side P_{ac} are balanced in this analysis. For this case of the FB-MMC in the buck and boost modes, the calculation for I_{dc} can be obtained by ignoring the power losses as follows:

$$
\begin{aligned}
& P_{dc} = P_{ac} \\
& V_{dc\_act}\, I_{dc} = V_{ph,rms}\, I_{ph,rms}\cos(\theta) \\
\because\ & V_{ph,rms} = \frac{V_{dc\_nom}}{2\sqrt{2}} \\
& I_{ph,rms} = \frac{I_m}{\sqrt{2}} \\
\therefore\ & V_{dc\_act}\, I_{dc} = \frac{V_{dc\_nom}}{2\sqrt{2}}\frac{I_m}{\sqrt{2}}\cos(\theta) \\
& I_{dc} = \frac{I_m}{4\left(V_{dc\_act}/V_{dc\_nom}\right)}\cos(\theta)
\end{aligned} \tag{4.3}
$$

Where $V_{ph,rms}$ and $I_{ph,rms}$ refer to the fundamental output voltage and current in RMS values. Of note that the reduction in the dc link voltage may lead to a rise in the dc current when the output current is kept at a constant value.

4.3.2 Calculation of the FB-submodule capacitor voltages

In this analysis, capacitor current harmonics FB-submodule capacitors can be calculated from the arm currents and the average switching functions of the FB-submodule. For the case of an FB-submodule in the upper arm, the average switching function can be deduced from the modulation signals defined by (3.10) and (3.11) as follows:

$$\begin{aligned} S_{up}(t) =\ & m_{up\_LL}(t) - m_{up\_RL}(t) \\ =\ & \frac{1}{2} + \frac{M_{dc}}{4} - \frac{M_{ac}}{4}\sin(\omega_0 t)\ - \frac{1}{2} + \frac{M_{dc}}{4} - \frac{M_{ac}}{4}\sin(\omega_0 t) \\ =\ & \frac{M_{dc}}{2} - \frac{M_{ac}}{2}\sin(\omega_0 t) \end{aligned} \tag{4.4}$$

Consequently, harmonic components in the capacitor current are expressed here as a product of the upper arm current defined by (4.1) and the average switching function defined by (4.4) as follows:

$$\begin{aligned} i_{C\_up}^{(n)}(t) &= S_{up}(t) * i_{arm\_up}^{(n)}(t) \\ &= i_{C\_up}^{(1)}(t) + i_{C\_up}^{(2)}(t) + i_{C\_up}^{(3)}(t) \end{aligned}$$

$$\begin{aligned} i_{C\_up}^{(1)}(t) =\ & \frac{M_{dc} I_m}{4}\sin(\omega_0 t + \theta) - \frac{M_{ac} I_{dc}}{2}\sin(\omega_0 t) \\ & - \frac{M_{ac} I_{cir}}{4}\cos(\omega_0 t + \varphi_{cir}) \end{aligned} \tag{4.5}$$

$$i_{C\_up}^{(2)}(t) = \frac{M_{ac} I_m}{8}\cos(2\omega_0 t + \theta) + \frac{M_{dc} I_{cir}}{2}\sin(2\omega_0 t + \varphi_{cir})$$

$$i_{C\_up}^{(3)}(t) = \frac{M_{ac} I_{cir}}{4}\cos(3\omega_0 t + \varphi_{cir})$$

Where $i_{C\_up}^{(n)}(t)$ refers to the capacitor n-order current harmonics of the upper arm FB-submodule. For the lower arm FB submodule, the average switching

function is obtained using the modulation signals defined by (3.8) and (3.9) as follows:

$$\begin{aligned} S_{low}(t) &= m_{low\_LL}(t) - m_{low\_RL}(t) \\ &= \frac{1}{2} + \frac{M_{dc}}{4} + \frac{M_{ac}}{4}\sin(\omega_0 t) - \frac{1}{2} + \frac{M_{dc}}{4} + \frac{M_{ac}}{4}\sin(\omega_0 t) \\ &= \frac{M_{dc}}{2} + \frac{M_{ac}}{2}\sin(\omega_0 t) \end{aligned} \quad (4.6)$$

Then, harmonic components in the capacitor ripple current are expressed as a product of the lower arm current defended by (4.2) and the average switching function defended by (4.6) as the following equations:

$$\begin{aligned} i_{C\_low}^{(n)}(t) &= S_{low}(t) * i_{arm\_low}^{(n)}(t) \\ &= i_{C\_low}^{(1)}(t) + i_{C\_low}^{(2)}(t) + i_{C\_low}^{(3)}(t) \\ &= -i_{C_{up}}^{(1)}(t) + i_{C_{up}}^{(2)}(t) - i_{C\_up}^{(3)}(t) \end{aligned} \quad (4.7)$$

The capacitor current n-order harmonics of the lower arm FB-submodules are denoted by $i_{C\_low}^{(n)}(t)$. From (4.5) and (4.7), it can be concluded that the FB-submodule capacitor current comprises the 1st, 2nd and 3rd harmonic components. Each harmonic in capacitor voltage of FB-submodule is directly excited by the corresponding harmonic in capacitor current. Accordingly, the analytical expression describing harmonic components in the capacitor voltage of the upper arm FB-submodule are obtained by integrating the capacitor current that defined in (4.5) as follows:

$$\begin{aligned} v_{C\_up}^{(n)}(t) &= \int i_{C\_up}^{(n)}(t)\, dt \\ &= v_{C\_up}^{(0)}(t) + v_{C\_up}^{(1)}(t) + v_{C\_up}^{(2)}(t) + v_{C\_up}^{(3)}(t) \end{aligned} \quad (4.8)$$

$$v_{C\_up}^{(0)}(t) = V_C$$

$$v_{C\_up}^{(1)}(t) = \frac{M_{ac}I_{dc}}{2C_{SM}\omega_0}\cos(\omega_0 t) - \frac{M_{dc}I_m}{4C_{SM}\omega_0}\cos(\omega_0 t + \theta) - \frac{M_{ac}I_{cir}}{4C_{SM}\omega_0}\sin(\omega_0 t + \varphi_{cir})$$

$$v_{C\_up}^{(2)}(t) = \frac{M_{ac}I_m}{16C_{SM}\omega_0}\sin(2\omega_0 t + \theta) - \frac{M_{dc}I_{cir}}{4C_{SM}\omega_0}\cos(2\omega_0 t + \varphi_{cir})$$

$$v_{C\_up}^{(3)}(t) = \frac{M_{ac}I_{cir}}{12C_{SM}\omega_0}\sin(3\omega_0 t + \varphi_{cir})$$

Where the capacitor voltage n-order with *n*th harmonic components are represented here by $v_{C\_up}^{(n)}(t)$. Thus, the dc component term is represented by $V_{C\_up}^{(0)}(t)$. While other terms are expressed by $V_{C\_up}^{(1)}(t), V_{C\_up}^{(2)}(t)$ and $V_{C\_up}^{(3)}(t)$, which refer to the ac components of the 1st, 2nd and 3rd harmonic-order respectively. Similarly, the capacitor current defined by (4.7) is integrated to find the analytical expression for the capacitor voltage harmonic components across the lower arm FB-submodule, which is represented by $V_{C\_low}^{(n)}(t)$ as follows:

$$\begin{aligned} v_{C\_low}^{(n)}(t) &= \int i_{C\_low}^{(n)}(t)\, dt \\ &= v_{C\_low}^{(0)}(t) + v_{C\_low}^{(1)}(t) + v_{C\_low}^{(2)}(t) + v_{C\_low}^{(3)}(t) \\ &= v_{C\_up}^{(0)}(t) - v_{C\_up}^{(1)}(t) + v_{C\_up}^{(2)}(t) - v_{C\_up}^{(3)}(t) \end{aligned} \quad (4.9)$$

In which $v_{C\_low}^{(0)}(t)$ is the dc component term of the capacitor voltage expressions, while the ac harmonic components are defined by $v_{C\_low}^{(1)}(t), v_{C\_low}^{(2)}(t)$ and $v_{C\_low}^{(3)}(t)$. For both analytical expressions in (4.8) and (4.9), the dc component terms represent the dc capacitor voltage V_C of the FB-submodule, which can be adjusted in accordance with the two different capacitor voltage regulation strategies as aforementioned in the section 3.3.3. For the ac harmonic components terms, it

can be observed that the even harmonic components are equal in amplitude and phase for both (4.8) and (4.9). On the contrary, their odd harmonic components have the same amplitude and but are in the opposite direction. Of note, an energy variation in the FB-submodule capacitor can be related to the ac harmonic components, while energy stored in the FB-submodule capacitor is related to the dc capacitor voltage of V_C. In terms of the FB-MMC operating in the buck and boost modes, it can be seen from the developed analytical expressions that the capacitor voltage ripple of the FB-submodule is influenced by both dc and ac modulation indexes M_{dc} and M_{ac}. Because $M_{dc} < 1$ specifies the operation of the FB-MMC in the boost mode, an amplitude of each ac component term that is related to M_{dc} can be decreased as the dc link voltage decreases. Note that, the capacitor voltage ripple components expressed as a function of I_{cir} can be significantly reduced when the FB-MMC operates in the boost mode at the specific dc link voltage levels as demonstrated in Chapter 3 that I_{cir} is almost zero for same dc link voltage levels, or in the buck and boost modes when the 2nd harmonic circulating current suppressing control is employed. However other capacitor voltage ripple components still exist as they are not influenced by minimising I_{cir}.

4.3.3 Calculation of the FB-submodule output voltage

For this case, harmonic components of the FB-submodule output voltage are mainly produced through an interaction of the FB-submodule capacitor voltage and the FB-submodule switching function. As a product of the capacitor voltage components in (4.8) and corresponding average switching function in (4.4), the expression for the output voltage of the upper arm FB-submodule can be calculated as follows:

$$
\begin{aligned}
v_{SM\_up}^{(n)}(t) &= S_{up}(t) * v_{C\_up}^{(n)}(t) \\
&= v_{SM\_up}^{(0)}(t) + v_{SM\_up}^{(1)}(t) + v_{SM\_up}^{(2)}(t) \\
&+ v_{SM\_up}^{(3)}(t) + v_{SM\_up}^{(4)}(t)
\end{aligned} \tag{4.10}
$$

Where $v_{SM\_up}^{(n)}(t)$ refers to the n-order harmonic components of the output voltage of FB-submodule in the upper arm. Accordingly, it can be noted that the output voltage of the upper arm submodule is expressed in terms of dc and ac components. As the circulating current is dominated by the 2nd harmonic component, the analysis shows that the output voltage of the FB-submodule includes dc and fundamental components and the 2nd, 3rd, and 4th order harmonics.

In this developed steady-state analysis, an accurate expression of the output voltage in FB submodule is derived and can be used to optimise the operation of FB-MMC in the boost mode. For the dc components generated in the FB submodule output voltage, it can be written as:

$$
\begin{aligned}
v_{SM\_up}^{(0)}(t) = V_C &+ \frac{M_{ac}^2 I_{dc}}{8C_{SM}\omega_0} - \frac{M_{dc}M_{dc}I_m}{16C_{SM}\omega_0}\sin(\theta) \\
&+ \frac{M_{ac}^2 I_{cir}}{16C_{SM}\omega_0}\cos(\varphi_{cir})
\end{aligned} \tag{4.11}
$$

Where V_C is the dc voltage capacitor, and $v_{SM\_up}^{(0)}(t)$ refers to the dc voltage produced in each upper arm submodule. For the balanced system, it can be defined by (3.16) or (3.17). The dc component is mainly generated by the dc capacitor voltage V_C, and additional dc components are generated due to the influence of the capacitor voltage ripple, which they are typically very small and can be neglected.

In the case of fundamental component, the output voltage of the FB-submodule in the upper arm is expressed as follows:

$$
\begin{aligned}
v_{SM\_up}^{(1)}(t) = & -\frac{M_{ac}V_c}{2}\sin(\omega_0 t) + \frac{M_{dc}M_{ac}I_{dc}}{4C_{SM}\omega_0}\cos(\omega_0 t) \\
& + \left(\frac{M_{dc}^2 I_m}{8C_{SM}\omega_0} - \frac{M_{ac}^2 I_m}{64C_{SM}\omega_0}\right)\cos(\omega_0 t + \theta) \\
& - \frac{3M_{dc}M_{dc}I_{cir}}{16C_{SM}\omega_0}\cos(\omega_0 t + \varphi_{cir})
\end{aligned}
\tag{4.12}
$$

Where the sum of the 1st order harmonic components are characterized by $v_{SM\_up}^{(1)}(t)$. It can be noted that the first term of expression (4.12) refers to the desired component of the output voltage can be regulated directly by changing M_{ac} under constant V_C. Other components in (4.12) are generated due to submodule capacitor voltage ripple and show complex dependences on $\theta, M_{dc}, M_{ac}, I_{dc}, I_m$ and I_{cir}. under certain operating conditions in the boost mode, the components in (4.12) which are functions of M_{dc}can be reduced as was demonstrated in Chapter 3. The last term in is a function of $I_{cir}$and will be around zero under the circulating current control.

Furthermore, other undesired harmonic components, which presented in the output voltage of the FB-submodule, are caused by the effect of interaction between the capacitor voltage ripple and the corresponding switching function. These undesired components are generated as the 2nd, 3rd and 4th order harmonics, and detailed expressions for these voltage components can be obtained as follows, respectively:

$$
\begin{aligned}
v_{SM\_up}^{(2)}(t) = & -\frac{M_{ac}^2 I_{dc}}{8C_{SM}\omega_0}\sin(2\omega_0 t) \\
& + \frac{3M_{dc}M_{ac}I_m}{32C_{SM}\omega_0}\sin(2\omega_0 t + \theta) \\
& + \left(\frac{M_{ac}^2 I_{cir}}{12C_{SM}\omega_0} - \frac{M_{dc}^2 I_{cir}}{8C_{SM}\omega_0}\right)\cos(2\omega_0 t + \varphi_{cir})
\end{aligned}
\tag{4.13}
$$

Then,

$$v_{SM\_up}^{(3)}(t) = \frac{M_{ac}^2 I_m}{64 C_{SM} \omega_0} \cos(3\omega_0 t + \theta) - \frac{5 M_{ac} M_{dc} I_{cir}}{48 C_{SM} \omega_0} \sin(3\omega_0 t + \varphi_{cir}) \tag{4.14}$$

And also,

$$v_{SM\_up}^{(4)}(t) = \frac{M_{ac}^2 \, I_{cir}}{48 C_{SM} \omega_0} \cos(4\omega_0 t + \varphi_{cir}) \tag{4.15}$$

Where $v_{SM\_up}^{(2)}(t)$, $v_{SM\_up}^{(3)}(t)$ and $v_{SM\_up}^{(4)}(t)$ denote to voltage components at the 2nd, 3rd and 4th harmonics generated in the upper arm FB-submodule. Since I_{cir} can be minimised in the boost mode at $M_{dc} = 0.6$, as was demonstrated in Chapter 3, a decrease in the output voltage undesired harmonics can be noted from the analytical expressions in (3.13), (3.14) and (3.15), as the some of the terms are influenced by both M_{dc} and I_{cir}. Hence, the fourth harmonic components can be properly minimised as it has only one term which is correlated to I_{cir}. Similary, a detailed analytical expression for the output voltage of lower arm FB-submodule can be deduced from multiplying the capacitor voltage ripple in (4.9) with the average switching function in (4.5). Thus, the expression can be written as follows:

$$\begin{aligned} v_{SM\_low}^{(n)}(t) &= S_{low}(t) * v_{C\_low}^{(n)}(t) \\ &= v_{SM\_low}^{(0)}(t) + v_{SM\_low}^{(1)}(t) + v_{SM\_low}^{(2)}(t) \\ &\quad + v_{SM\_low}^{(3)}(t) + v_{SM\_low}^{(4)}(t) \\ &= v_{SM\_up}^{(0)}(t) - v_{SM\_up}^{(1)}(t) + v_{SM\_up}^{(2)}(t) \\ &\quad - v_{SM\_up}^{(3)}(t) + v_{SM\_up}^{(4)}(t) \end{aligned} \tag{4.16}$$

Where $v_{SM\_low}^{(n)}(t)$ represents *n*-order harmonic components of the output voltage of the lower arm FB-submodule. Under the buck and boost operating modes, the analysis shows that the 1st, 2nd, 3rd and 4th order harmonics in $v_{SM\_up}^{(n)}(t)$ are the same as those of $v_{SM\_low}^{(n)}(t)$ in both the amplitude and phase. While their 2nd and 4th order harmonics are of opposite phase regarding the 2nd and 4th order harmonics in $v_{SM\_low}^{(n)}(t)$. Besides, the voltage components of $v_{SM\_low}^{(0)}(t)$, $v_{SM\_low}^{(1)}(t)$, $v_{SM\_low}^{(2)}(t)$, $v_{SM\_low}^{(3)}(t)$ and $v_{SM\_low}^{(4)}(t)$ have same as performance characterises as of $v_{SM\_up}^{(0)}(t)$, $v_{SM\_up}^{(1)}(t)$, $v_{SM\_up}^{(2)}(t)$, $v_{SM\_up}^{(3)}(t)$ and $v_{SM\_up}^{(4)}(t)$, respectively, and are also influenced by both M_{dc} and I_{cir}.

4.3.4 Calculation of the arms and output phase voltages of the FB-MMC

Analytical expressions for the upper and lower arm voltages can be calculated based on the expressions of the output voltage of the FB-submodules. As each arm is formed by the cascaded connection of *N* identical FB-submodules, the expression for the upper arm voltage can be given as follows:

$$\begin{aligned} v_{arm\_up}^{(n)}(t) &= N.S_{up}(t) * v_{C\_up}^{(n)}(t) \\ &= N.\begin{Bmatrix} v_{SM\_up}^{(0)}(t) + v_{SM\_up}^{(1)}(t) + v_{SM\_up}^{(2)}(t) \\ + v_{SM\_up}^{(3)}(t) + v_{SM\_up}^{(4)}(t) \end{Bmatrix} \end{aligned} \tag{4.17}$$

Where $v_{arm\_up}^{(n)}(t)$ is the upper arm voltage which contains the dc and ac components of the n^{th} order. However, the expression for the lower arm voltage is also calculated as follows:

$$
\begin{aligned}
v_{arm\_low}^{(n)}(t) &= N.S_{low}(t) * v_{C\_low}^{(n)}(t) \\
&= N.\begin{Bmatrix} v_{SM\_low}^{(0)}(t) + v_{SM\_low}^{(1)}(t) + v_{SM\_low}^{(2)}(t) \\ +v_{SM\_low}^{(3)}(t) + v_{SM\_low}^{(4)}(t) \end{Bmatrix} \\
&= N.\begin{Bmatrix} v_{SM\_up}^{(0)}(t) - v_{SM\_up}^{(1)}(t) + v_{SM\_up}^{(2)}(t) \\ -v_{SM\_up}^{(3)}(t) + v_{SM\_up}^{(4)}(t) \end{Bmatrix}
\end{aligned} \tag{4.18}
$$

Where the lower arm voltage with the dc and ac components up to the n^{th} order is defined by $v_{arm\_low}^{(n)}(t)$. As voltage drop across the arm resistor is not taken into account in this analysis, the expression for output phase voltage of the FB-MMC can be obtained from the difference between the upper and lower arm voltage components as follows:

$$
\begin{aligned}
v_{ph}^{(n)}(t) &= \left(v_{arm_{low}}^{(n)}(t) - v_{arm_{up}}^{(n)}(t) \right)/2 \\
&= \frac{1}{2} N.\begin{Bmatrix} v_{SM\_up}^{(1)}(t) + v_{SM\_low}^{(1)}(t) \\ +v_{SM\_up}^{(3)}(t) + v_{SM\_low}^{(3)}(t) \end{Bmatrix} \\
&= N.\begin{Bmatrix} v_{SM\_up}^{(1)}(t) + v_{SM\_up}^{(3)}(t) \end{Bmatrix}
\end{aligned} \tag{4.19}
$$

It can be noted that output phase voltage of the FB-MMC, in addition to the desired components at the fundamental frequency, also comprises the 3rd order harmonic. However, a common-mode voltage which is only generated in the dc side [68] can be calculated by summing up the upper and lower arm voltages as follows:

$$
\begin{aligned}
v_{com}^{(n)}(t) &= v_{arm\_low}^{(n)}(t) + v_{arm\_up}^{(n)}(t) \\
&= N.\begin{Bmatrix} v_{SM\_up}^{(0)}(t) + v_{SM\_low}^{(0)}(t) + v_{SM\_up}^{(2)}(t) \\ +v_{SM\_low}^{(2)}(t) + v_{SM\_up}^{(4)}(t) + v_{SM\_low}^{(4)}(t) \end{Bmatrix}
\end{aligned} \tag{4.20}
$$

Besides the dc link voltage, it can be observed from this analysis that the ac voltage components of the 2nd and 4th harmonics still exist in the common-mode

voltage $v_{com}^{(n)}(t)$. For the case for the grid connected FB-MMC, only the 2nd order harmonic while the 4th harmonic has a minor impact and can be neglected.

4.3.5 Calculation of the circulating current in the FB-MMC:

Based on the above analysis, it can be calculated the ac voltage ripple of the 2nd harmonic component predominantly exists in the common-mode voltage. As a result, the 2nd harmonic circulating current can be generated in the FB-MMC arms. For this study, the analytical expression of the circulating current is calculated, that enables to represent its relationship with the average switching function under the buck and boost modes of the dc link voltage. As an impedance path for each arm is mainly inductance, the analytical expression for the 2nd harmonic circulating current can be obtained from an integration of $v_{SM\_up}^{(2)}(t) + v_{SM\_low}^{(2)}(t)$ multiplying by the number of FB-submodule for each arm as follows:

$$\begin{aligned} I_{cir}\sin(2\omega_0 t + \varphi_{cir}) &= -\frac{N}{2L_{arm}}\int\left\{v_{SM\_up}^{(2)}(t) + v_{SM\_low}^{(2)}(t)\right\}dt \\ &= \frac{NM_{ac}^2 I_{dc}}{16{\omega_0}^2 C_{SM} L_{arm}}\cos(2\omega_0 t) \\ &-\frac{3NM_{dc}M_{ac}I_m}{64{\omega_0}^2 C_{SM} L_{arm}}\cos(2\omega_0 t + \theta) \\ &+\left(\frac{NM_{ac}^2 I_{cir}}{24{\omega_0}^2 C_{SM} L_{arm}} - \frac{NM_{dc}^2 I_{cir}}{16{\omega_0}^2 C_{SM} L_{arm}}\right)\sin(2\omega_0 t + \varphi_{cir}) \end{aligned} \tag{4.21}$$

Based on the left side of the expression (4.21), it can be seen that two variables of amplitude I_{cir} and phase angle φ_{cir} are presented to define the assumed 2nd harmonic circulating current in the time domain. As terms of the expression in (4.21) are composed of trigonometric functions, they can be solved to describe explicit expressions for the amplitude and phase of the 2nd harmonic circulating current. The amplitude I_{cir} can be expressed as follows:

$$I_{cir} = \frac{\sqrt{(A\cos(\theta) - B)^2 + (A\sin(\theta))^2}}{1 - \frac{NM_{dc}^2}{16{\omega_0}^2 C_{SM} L_{arm}} - \frac{NM_{ac}^2}{24{\omega_0}^2 C_{SM} L_{arm}}} \tag{4.22}$$

Where: $A = \frac{3NM_{ac}M_{dc}I_m}{64{\omega_0}^2 C_{SM} L_{arm}}, B = \frac{NM_{ac}^2 I_{dc}}{16{\omega_0}^2 C_{SM} L_{arm}}$

While the calculation for the phase angle φ_{cir} can be given as follows:

$$\varphi_{cir} = arctan(A\cos(\theta) - B, -A\sin(\theta)) \tag{4.23}$$

If compared to other expressions which introduced in [66], [67], [68] and [69], the analytical expression for the 2nd harmonic circulating current developed in this analysis is a function of both M_{dc} and M_{ac} and is valid for both buck and boost modes. The developed expression, which describes the behaviour of the 2nd order circulating current analytically, can be used for modelling and designed of the grid connected FB-MMC.

4.3.6 Development of criteria for resonant inductance in the FB-MMC:

For the MMC, the criteria of parameters design take into consideration a resonance phenomenon that exists between the capacitors of submodules and the arm inductors. Accordingly, a resonance characteristic in the 2nd harmonic circulating current is considered to avoid an increase in the circulating current that occurs at the resonant point. In the grid connected FB-MMC, the arm inductance value L_{arm} has to be chosen a few times higher than a resonant inductance value L_r. The resonant inductance L_r is defined in [67] as follows:

$$L_r = \frac{5NM_{ac}^2}{48{\omega_0}^2 C_{SM}} \tag{4.24}$$

The formula defined by (4.24) is proposed for the resonant inductance, which is considered for the parameter design of the submodule capacitor and arm inductor in the HB-MMC. However, this formula can only provide a resonant point for when the FB-MMC operating in the buck mode. Thus the operation of the FB-MMC at different levels of the dc link voltage is not taken into account by (4.24). This work develops the formula for L_r in the boost mode. As the resonant point can be found from the analytical expression of the 2nd harmonic circulating current amplitude [67], [69], the expression defined by (4.22) is used for developing the formula for the resonant inductance in the boost mode as follows:

$$L_r = \frac{2NM_{ac}^2 + 3NM_{dc}^2}{48{\omega_0}^2 C_{SM}} \tag{4.25}$$

It can be observed that the developed formula in the above can expose the influence of the dc modulation index M_{dc}. Therefore, the value of the resonant inductance in the boost mode can also be related to a specific level of the dc link voltage. The behaviour of the resonant inductance can be exploited in the parameter design while the FB-MMC works at a specific value of the dc link voltage. Based on the switching model results in Fig 3.28, it shows that better resonant behaviour in the boost mode is obtained when the dc link voltage at 60% of the nominal value. For this case, a maximum of I_{cir} which occurs at its resonant point (inductance) is still much less than those of other resonant points. The circulating current control here can reduce I_{cir} with less effort. Therefore, this operating point can provide a degree of freedom to choose the value of the arm inductance.

4.4 Simulation results and discussion for FB-MMC model

To validate the developed steady-state analytical model of FB-MMC, the simulations in this research work are undertaken in the same operating points as the switching model. Therefore, the simulation results of the analytical model are compared to those of the switching model, which is built-in the MATLAB/Simulink in Chapter 3 (see Appendix A and B). As this analysis considers the grid connected FB-MMC, the comparison results are provided when the FB-MMC operates in the buck and the boost modes by setting different levels of the dc link voltage. For this case, operational characteristics of voltage and current components of the FB-MMC are presented in both time and frequency domains, that to show the validity of the analytical model accuracy. Also, the simulation results of harmonic spectrums based on FFT analysis are presented with normalised amplitude for voltage and current. Where the rated values of the output voltage and current are used to normalise amplitude for voltage and current components in the FB-MMC, respectively. Of note that the simulation parameters used for both the developed steady-state analytical and switching models are mainly listed in Table 3.1.

4.4.1 Operating FB-MMC in the buck mode

In order to achieve both the analytical and switching models of the FB-MMC at buck operating mode, the actual value of the dc link voltage V_{dc_act} is kept at its nominal value ($i.e\ V_{dc\_act} = V_{dc\_nom} =$ 10 kV). Besides, the modulation indexes M_{ac} and M_{dc} are manually adjusted at 1. Note that the switching model employing the PSC-PWM strategy considers the carrier frequency of 1 kHz. By considering that the FB-MMC operates at unity power factor, a comparison of the upper and lower arm current waveforms in both analytical and switching models are presented in Fig 4.2 (a) and (b). These simulation results are also confirmed by including FFT analysis as shown in Fig 4.2 (c), that to quantify amplitudes of the arm current

components in both models. Each of the arm currents in the analytical model is calculated from (4.1) and (4.2). Of note that the arm current components are here normalised by I_m, which is the peak value of the load current. Along with the dc component current I_{dc}, Fig 4.3 shows the 2nd harmonic circulating currents I_{cir} for both analytical and switching model. The I_{cir} is calculated depending on (4.21), (4.22) and (4.23), while I_{dc} is obtained from (4.3) in the analytical model. For upper and lower arm FB-submodules, the average capacitor currents based on (4.5) and (4.7) in the analytical model are compared to this of the switching model, as shown in Fig 4.4. It is worth mentioning that each capacitor current of FB-submodule is resultant from arm current that modulated by corresponding switching function. The capacitor voltages of the FB-submodule in the upper and lower arms are shown in Fig 4.5. The simulation results show a match with the analytical expression derived by (4.8) and (4.9) and the switching model (in the open-loop control). For all FB-submodules, the dc capacitor voltages V_C are regulated around the nominal value which is 2.5 kV. That is achieved by adjusting both M_{ac} and M_{dc} to be one. Here, the V_C represents the minimum requirement of the operating in the buck mode. Due to the ripple components, it can be observed that the voltage across capacitors are fluctuated with a maximum of 9.4 % above the nominal value. As shown in Fig 4.5 (c), the FFT analysis is used to quantify the 1st, 2nd and 3rd harmonic components for each capacitor voltage. Noted that these components are normalised by $V_{dc\_nom}/2$. For the switching model, results show a slight voltage amplitude of the 4th harmonic component. That is not considered in the analytical model of the FB-MMC, as the circulating current with the 2nd harmonic component is only assumed to exist in this developed analytical model. Fig 4.6 presents the output voltage of the FB-submodule in the upper and lower arms. These voltages are analytically calculated from (4.9) and (4.10). However, in the switching model, the results show these voltages, when FB-submodules are inserted with positive voltage $+V_C$ and zero voltage as the submodules are bypassed. Note that each output voltage of the FB-submodule is obtained from the capacitor voltage that modulated by corresponding

switching function. The simulation results in Fig 4.7 (a) and (b) show the arm voltage waveforms of the analytical and switching models. These voltages are calculated from the sum of the output voltages of all FB-submodules in each arm. They are analytically represented by (4.18) and (4.19). Regarding the FB-MMC with N=4, the arm voltage waveforms in the switching model are produced at five levels as the FB-submodules are only inserted with the positive voltage of V_C. Using FFT analysis, harmonic spectrums for the arm voltages of both models are presented in Fig 4.7 (c). For analytical model, amplitudes of the ripple components in the arm voltages are obtained by using the expressions defined by (4.11), (4.12), (4.13), (4.14) and (4.15). Fig 4.8 (a) shows that the output phase voltage $v_{ph}(t)$ of the switching model is generated with five levels. This voltage is also matched to the analytical model derived in (4.19). Harmonic spectrums presented in Fig 4.8 (b) is indicated that $v_{ph}(t)$ is included voltage ripple of the 3rd order which caused by the influence of the circulating current. For the switching model, switching frequency of the FB-submodule, arm and output voltage waveform are twice those of the HB-MMC. Apart from this, the operational characteristics of voltage and current ripples for both FB-MMC and HB-MMC are similar that only when FB- MMC works at the buck mode.

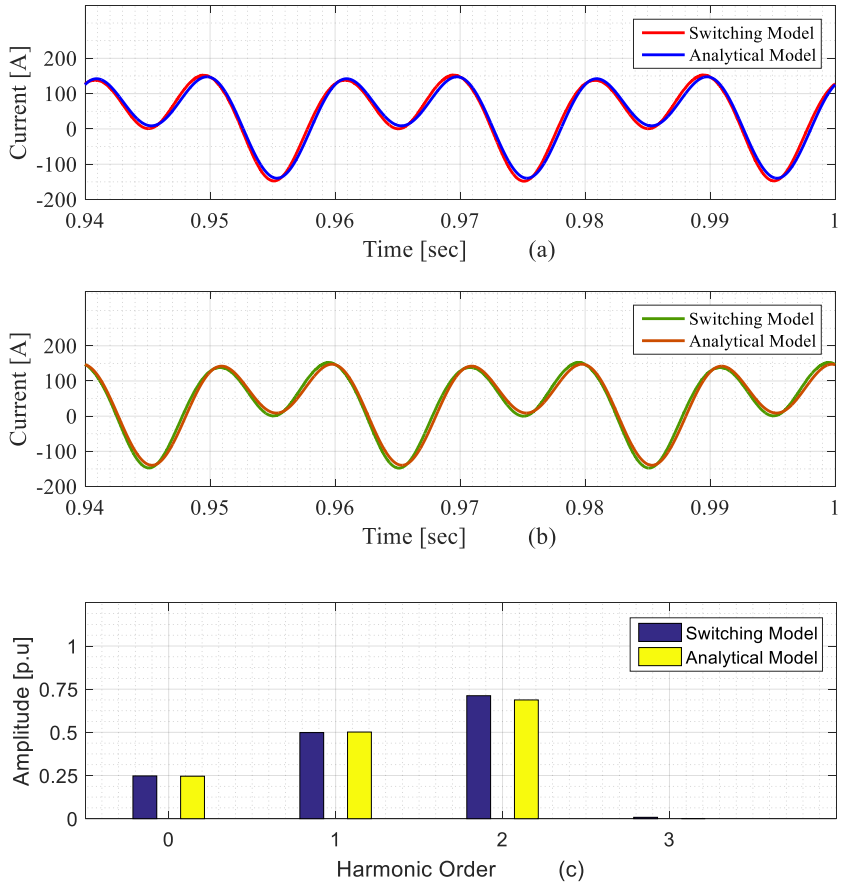


Fig 4.2 Comparison of the switching and analytical model arm currents when the FB-MMC operates at buck mode at M_{dc}= 1, M_{ac}= 1, PF = 1 and V_C defined by (3.16) (a)- Upper arm current (b)- Lower arm current (c)- Harmonic spectrum of arm current components normalized by I_m

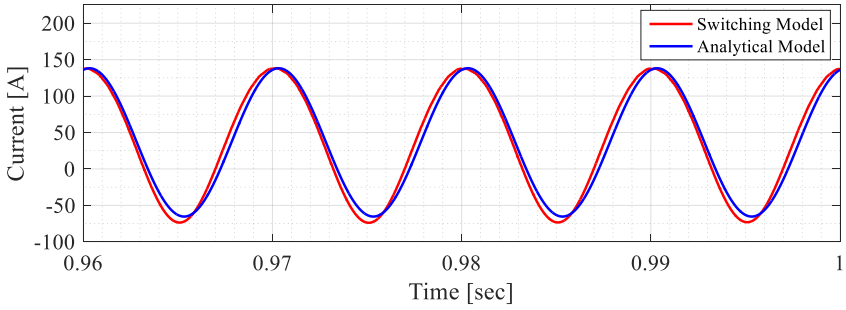


Fig 4.3 Comparison of the switching and analytical model the 2nd harmonic circulating currents when the FB-MMC operates at buck mode M_{dc}= 1, M_{ac}= 1,, PF = 1 and V_C defined by (3.16)

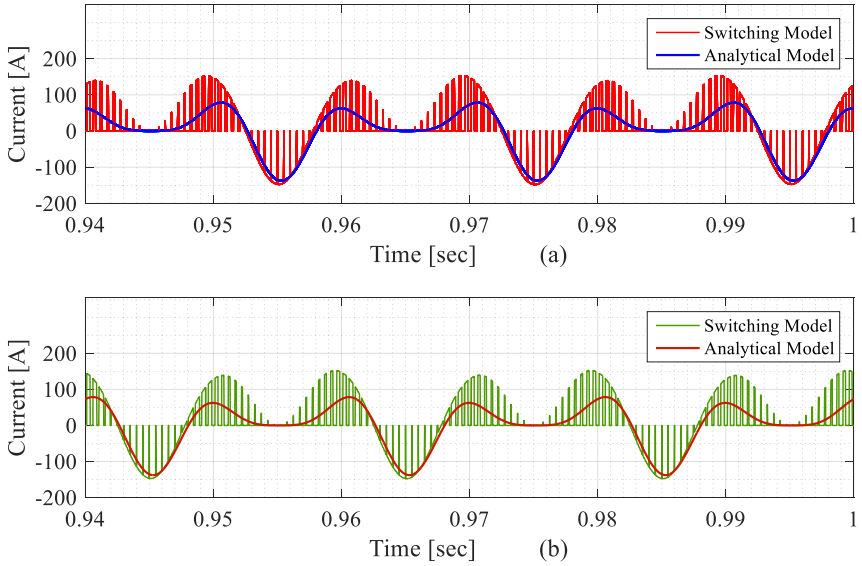


Fig 4.4 Comparison of the switching and analytical model capacitor currents when the FB-MMC operates at buck mode at M_{dc}= 1, M_{ac}= 1, PF = 1 and V_C defined by (3.16) (a)- Upper arm capacitor current (b)- Lower arm capacitor current

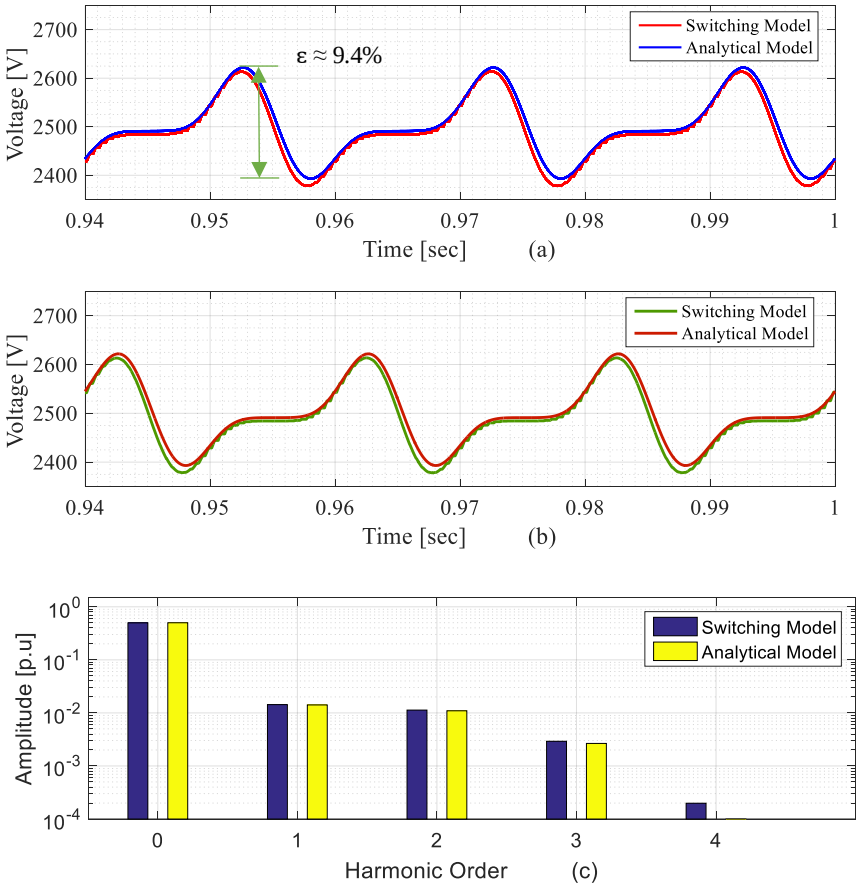


Fig 4.5 Comparison of the switching and analytical model capacitor voltages when the FB-MMC operates the buck mode at M_{dc}= 1, M_{ac}= 1, PF = 1 and V_C defined by (3.16) (a)- Upper arm capacitor voltages (b)- Lower arm capacitor voltages (c)- Harmonic spectrum of capacitor voltage components normalised by $V_{dc\_nom}/2$

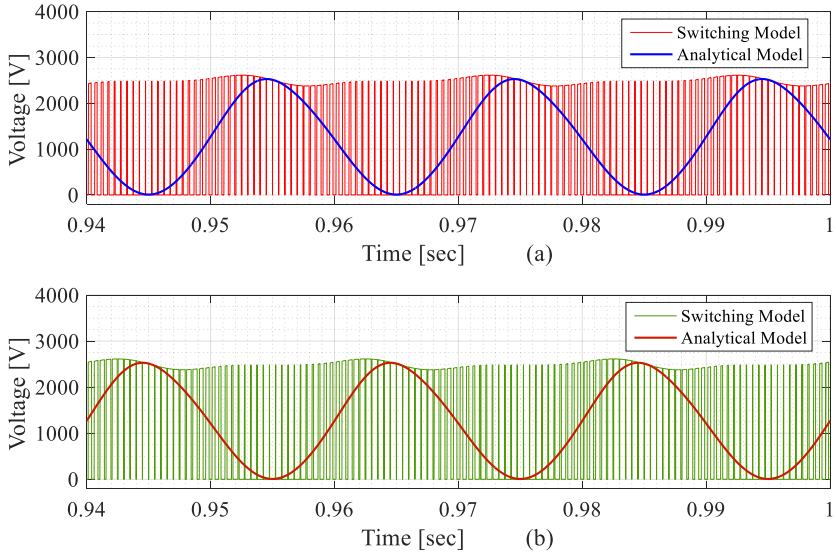


Fig 4.6 Comparison of the switching and analytical model submodule voltages when the FB-MMC operates at buck mode at M_{dc}= 1, M_{ac}= 1,, PF = 1 and V_C defined by (3.16), (a)- Upper arm submodule voltages (b)- Lower arm submodule voltages

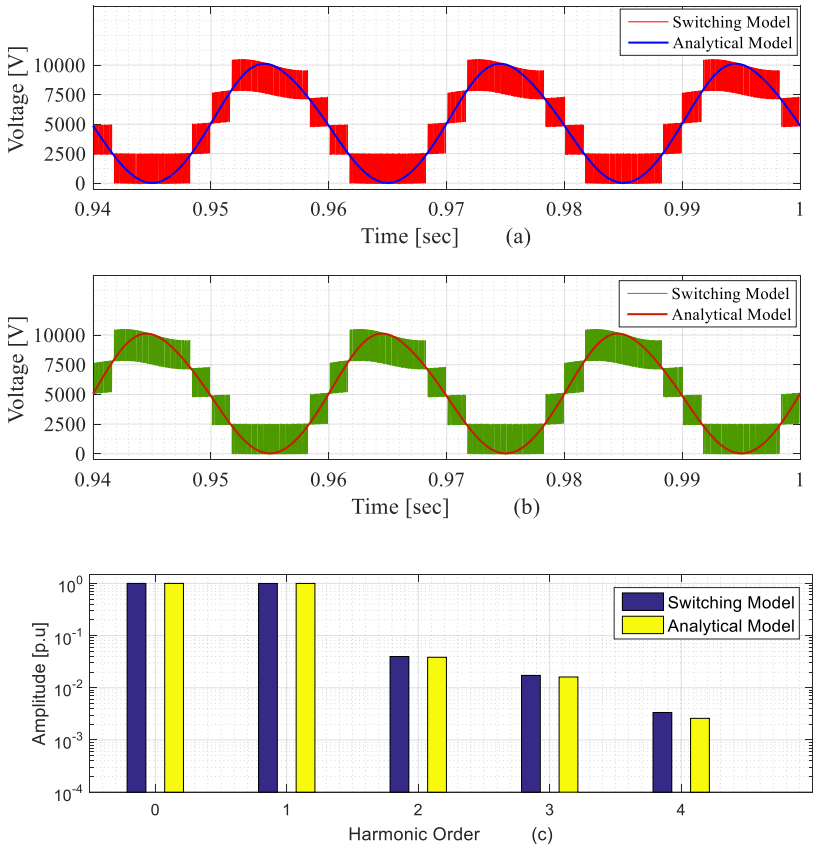


Fig 4.7 Comparison of the switching and analytical model arm voltages when the FB-MMC operates in the buck mode at M_{ac} = 1, M_{dc}= 1, PF = 1 and V_C defined by (3.16),(a)- Upper arm voltages (b)- Lower arm voltages (c)- Harmonic spectrum of arm voltage components normalised by $V_{dc\_nom}/2$

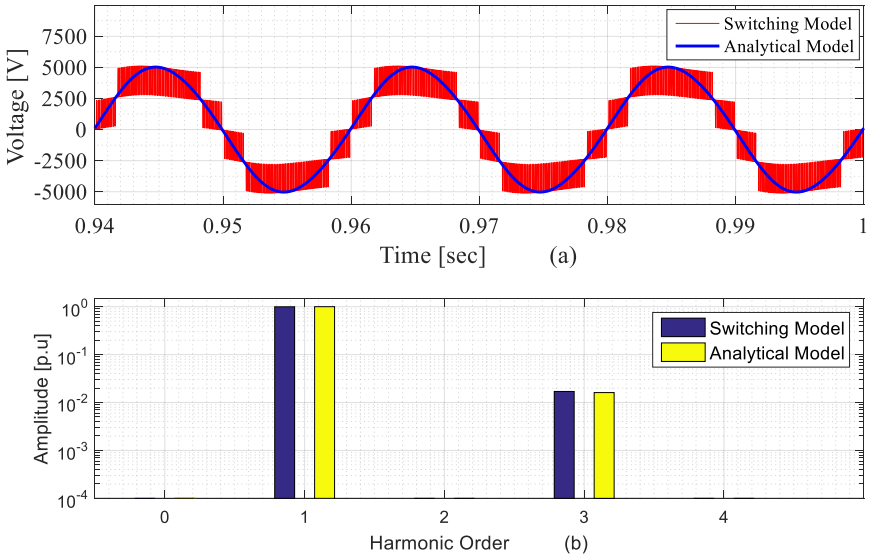


Fig 4.8 Comparison of the switching and analytical model output phase voltage when FB-MMC operates at the buck mode at M_{dc}= 1, M_{ac}= 1, PF = 1 and V_C defined by (3.16), (a)- the output phase voltage (b)- Harmonic spectrum of the output phase voltage components normalized by $V_{dc\_nom}/2$

4.4.2 Operating FB-MMC in the boost mode:

In this mode, the results of the FB-MMC models are simulated at the optimal operating point, in which the actual dc link value V_{dc_act} is performed at 60 % of its nominal value. For this case, the two FB-submodule capacitor voltage regulation approaches, which discussed in Chapter 3, are employed to demonstrate the validity of the developed steady-state analytical model under these operating conditions.

4.4.2.1 When FB-submodule capacitor voltage is regulated to its nominal value

For the case of the first regulation approach of the capacitor voltage which defined by (3.16), the ac and dc modulation indexes are adjusted as M_{ac}= 1 and M_{dc} = 0.6. For the arm currents, analytical equations defined by (4.1) and (4.2) are matched with the switching model results, as shown in Fig 4.9 (a) and (b). Although, it shows that the arm currents have superimposed on the switching frequency ripple.

That is because the interleaving occurs between the arm voltages at the boost mode and switching harmonic not completely cancelled. Harmonic spectrums to identify the amplitudes of the arm currents components of both models are presented in Fig 4.9 (c) that to show how the boost mode at this operating point influences the 2nd harmonic currents. If compared to the buck mode, it can be observed that circulating currents are reduced to 92.33 %. As the FB-MMC works at constant load current mode, the dc current component increases to around 40 %. Fig 4.10 shows that the 2nd harmonic circulating current of the switching model is superimposed on the switching ripples. The capacitor currents of both models are shown in Fig 4.11. Unlike the buck mode, a direction of each FB-submodule capacitor current in the boost mode is not always matched to corresponding arm current. For the case of the switching model, it can be seen that the direction of each capacitor current is reversed because its FB-submodule is inserted in negative polarity. This point would be more beneficial in making a consideration about capacitor voltage balancing control for the FB-MMC. The simulation results, which are shown in Fig 4.12 (a) and (b), confirm closely match of the capacitor voltages, which obtained from the analytical model and the switching model. Based on the values of the modulation indexes, each of the submodule dc capacitor voltages is regulated to 2.5 kV. In this case, capacitor voltages fluctuation is reduced to 1.48 %. The harmonic spectrums presented in Fig 4.12 (c) show the amplitudes of the 1st, 2nd and 3rd order components of the capacitor voltage are significantly decreased, as they are influenced by the reduction of I_{cir}. In comparison with FB-submodule output voltages for both models as shown Fig 4.13. It can be noted from the analytical model that a negative part of the average output voltage is generated, that because the dc-offset is directly related to the level of the actual dc link voltage. However, in the switching model, it shows the negative part of this voltage is generated when the FB-submodule is inserted negative voltage $-V_C$. As illustrated in Fig 4.14 (a) and (b), one more level in the boost mode is produced in each arm voltages of the switching model. Analytically, however, the dc offset of each arm voltage is always generated at $V_{dc\_act}/2$. As it is

assumed that the grid connected FB-MMC, the amplitude of the fundamental in arm voltages of both models are maintained constant with $\hat{v_{ph}}/2N$. Besides, Fig 4.14 (c) of the harmonic spectrums shows a decrease in amplitudes of the ripple components in the arm voltages of both models which influenced by I_{cir}. In Fig 4.15 (a), the output phase voltages $v_{ph}(t)$ in the average and switching waveforms is presented. From this, it can be seen that $v_{ph}(t)$ in the switching model of the FB-MMC is generated with nine levels. Although this operation of the dc link voltage at 60 % of its nominal value is considered as the optimal operating point to minimise the 2nd harmonic circulation current, the switching model result shows that the interleaving is not optimally achieved. In the boost mode, the amplitude of the 3rd ripple component in $v_{ph}(t)$ becomes 80.2 % less if compared to the buck mode as Fig 4.15 (b).

4.4.2.2 Comparison results when FB-MMC working in both buck and boost modes

In this section, the comparison results based on the validated analytical model is made between the operation of FB-MMC in the buck and boost modes, that to show a difference in the characteristic of the 2nd harmonic circulating currents, arm currents and the ac ripple across FB-submodule capacitor voltage. For the boost mode regards the optimal operating point, it can be observed that the RMS value of the circulating current is minimised from 74.45 to 5.71 A as compared to the buck mode as shown in Fig 4.16 (a). Regardless of the dc component current, this minimisation due to the boost mode positively influences the arm current waveforms. The upper arm current as an example is shown in Fig 4.16 (b). Accordingly, the fluctuation of the capacitor voltage is decreased from 9.4 % to 1.48 %. As illustrated in Fig 4.16 (c). The results of the normalised capacitor voltage in the upper arm only are considered the ac ripple components.

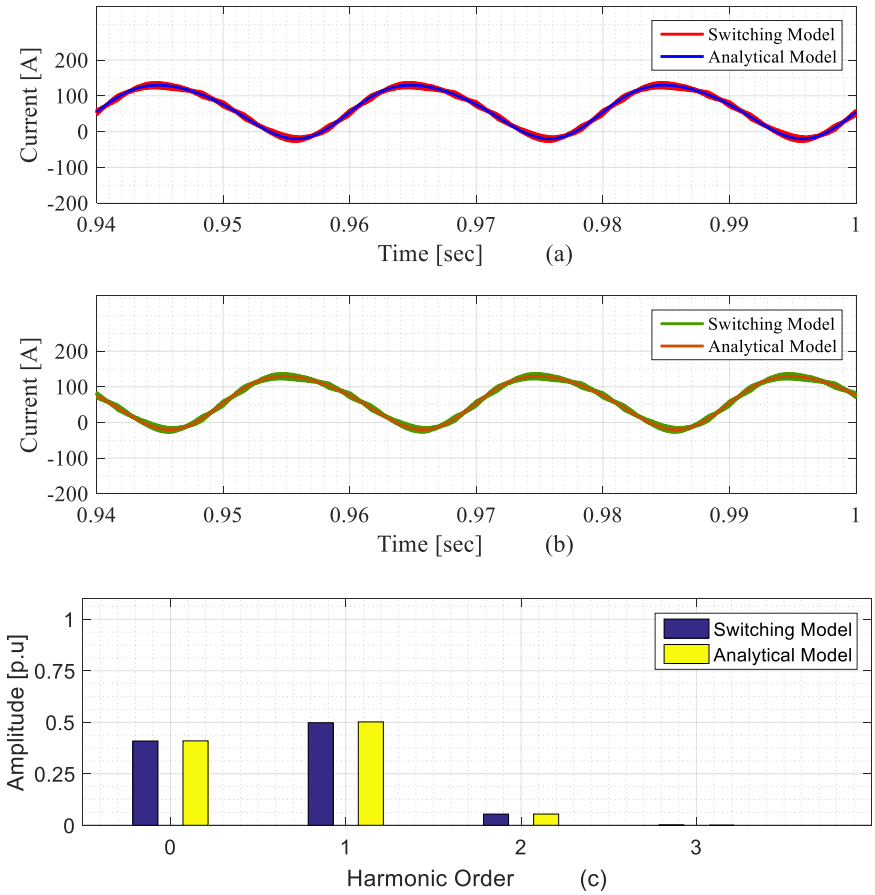


Fig 4.9 Comparison of the switching and analytical model arm currents when FB-MMC operates in the boost mode at V_{dc_act}= 60 % of V_{dc_nom}, M_{dc}= 0.6, M_{ac}= 1, PF = 1 and V_C defined by (3.16), (a)- Upper arm current (b)- Lower arm current (c)- Harmonic spectrum of the arm current components normalised by I_m

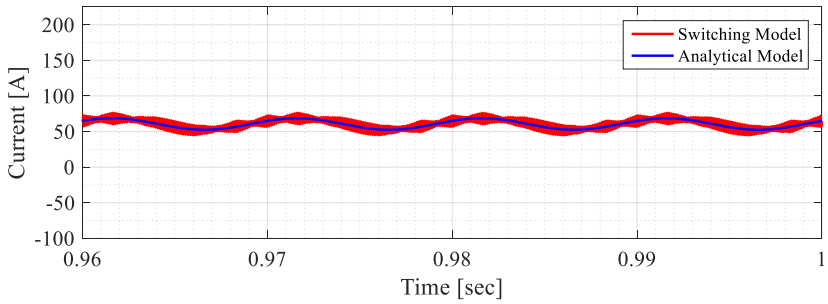


Fig 4.10 Comparison of the switching and analytical model the 2nd harmonic circulating currents when the FB-MMC operates in the boost mode at V_{dc_act}= 60 % of V_{dc_nom}, M_{dc}= 0.6, M_{ac}= 1, PF = 1 and V_C defined (3.16)

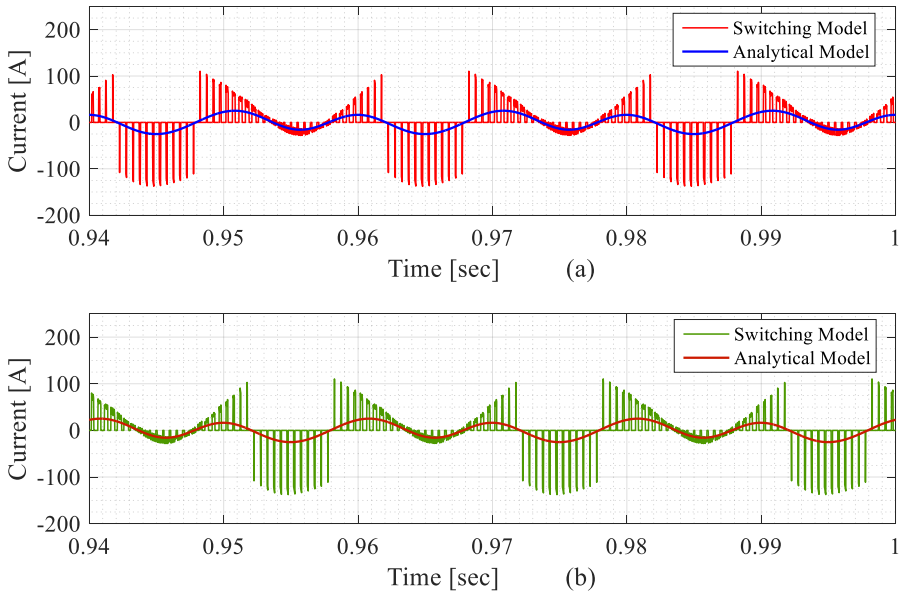


Fig 4.11 Comparison of the switching and analytical model capacitor currents when FB-MMC operates in boost mode, V_{dc_act}= 60 % of V_{dc_nom}, M_{dc}= 0.6, M_{ac}= 1, PF = 1 and V_C defined by (3.16),(a) Upper arm capacitor currents (b) Lower arm capacitor currents

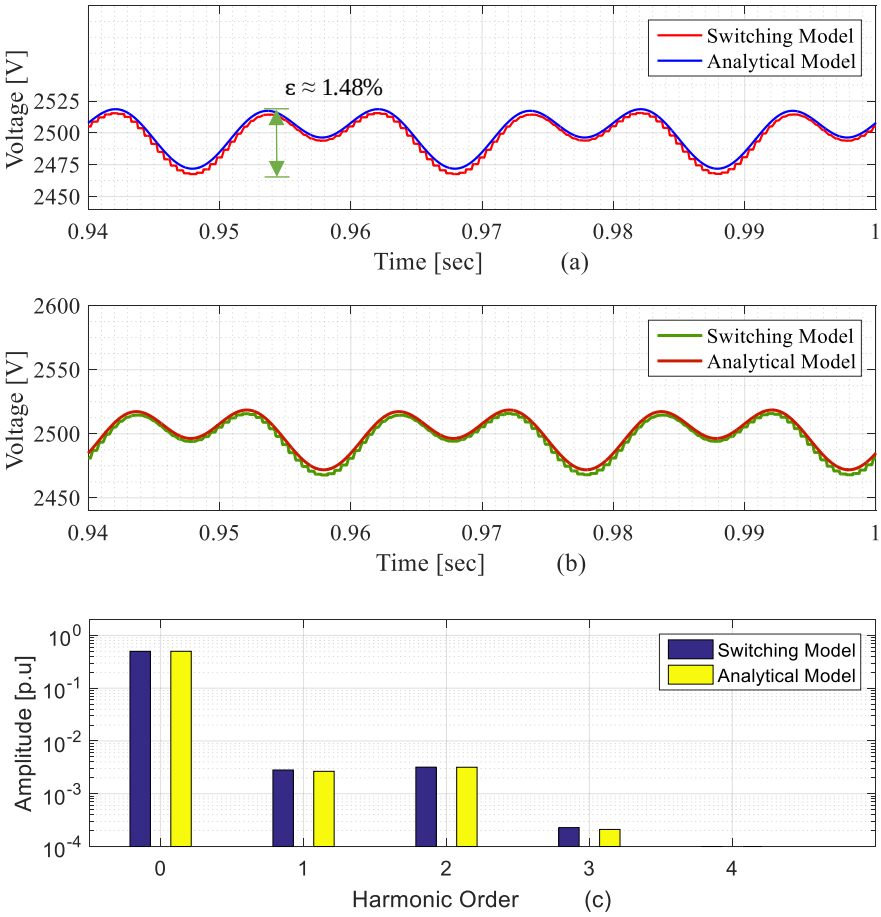


Fig 4.12 Comparison of the switching and analytical model capacitor voltages when the FB-MMC operates in the boost mode at V_{dc_act}= 60 % of V_{dc_nom}, M_{dc}= 0.6, M_{ac}= 1, PF = 1 and V_C defined by (3.16): (a)- Upper arm capacitor voltages (b)- Lower arm capacitor voltages (c)- Harmonic spectrum of the capacitor voltage components normalised by $V_{dc\_nom}/2$

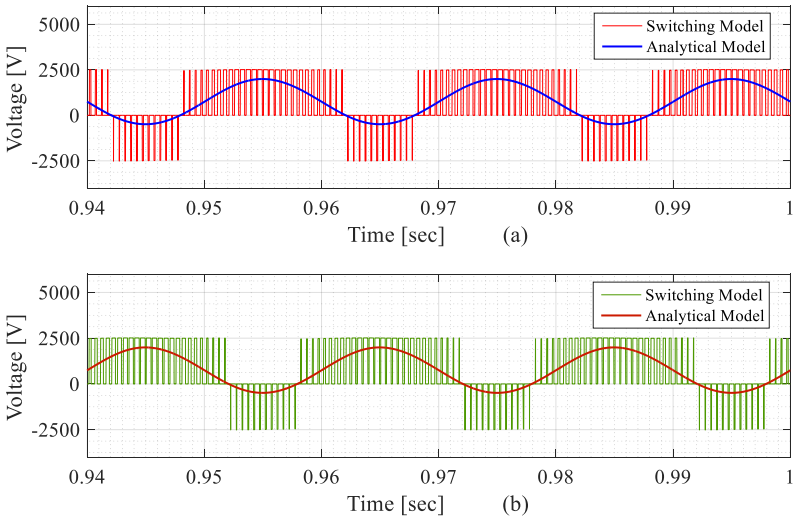


Fig 4.13 Comparison of the switching and analytical model submodule voltages when the FB-MMC operates in the boost mode at V_{dc_act}= 60 % of V_{dc_nom}, M_{dc}= 0.6, M_{ac}= 1, PF = 1 and V_C defined by (3.16), (a)- Upper arm submodule voltages (b)- Lower arm submodule voltages

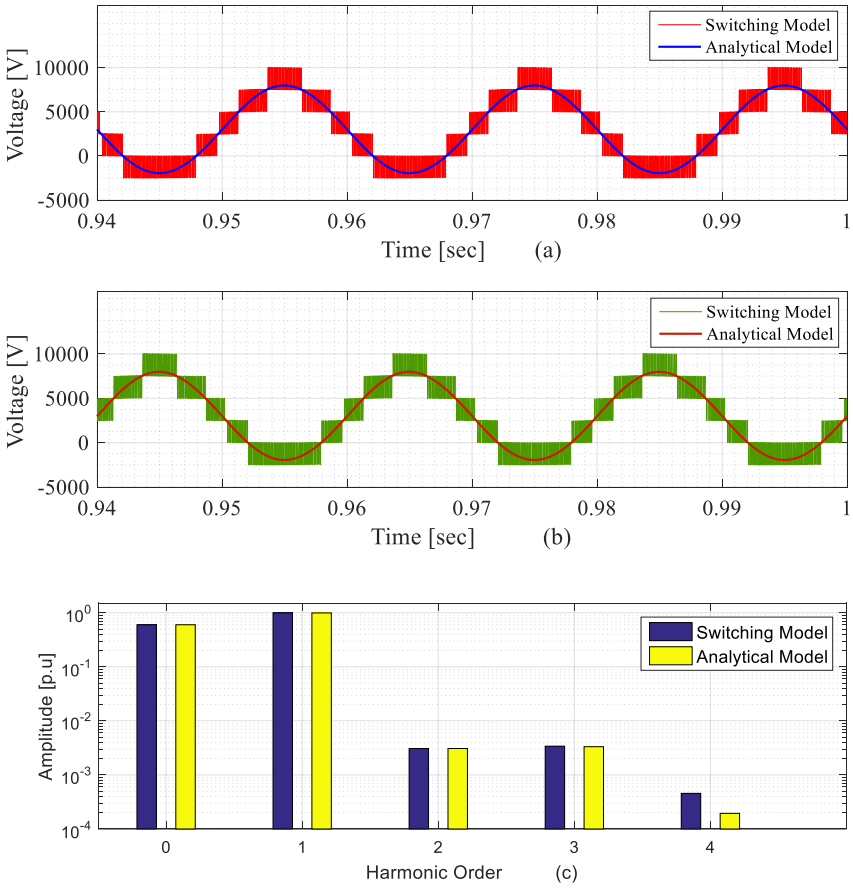


Fig 4.14 Comparison of the switching and analytical model arm voltages when the FB-MMC operates in the boost mode at V_{dc_act}= 60 % of V_{dc_nom}, M_{dc}= 0.6, M_{ac}= 1, PF = 1 and V_C defined by (3.16), (a)- Upper arm voltages (b)- Lower arm voltages (c)- Harmonic spectrum of the arm voltage components normalised by $V_{dc\_nom}/2$

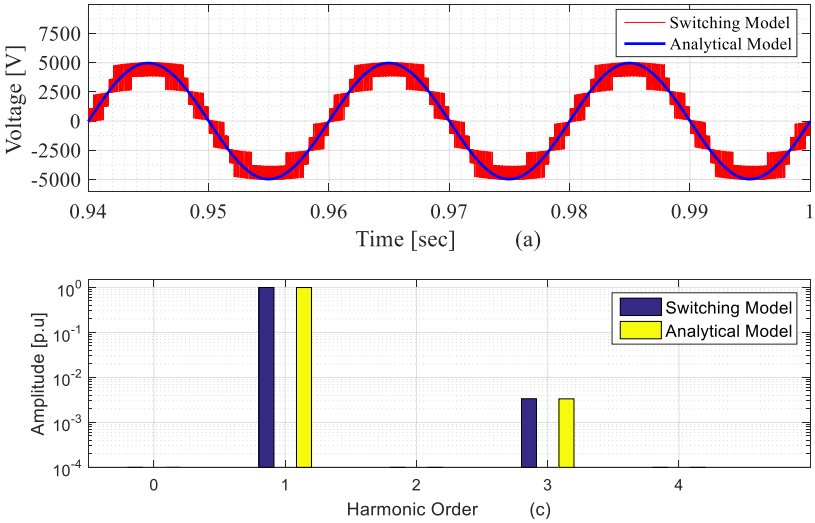


Fig 4.15 Comparison of the switching and analytical model output voltage when FB-MMC operates in the boost mode, V_{dc_act}= 60 % of V_{dc_nom}, M_{dc}= 0.6, M_{ac}= 1, PF = 1 and V_C defined by (3.16),(a)- the output phase voltage (b)- Harmonic spectrum of the output phase voltage components normalised by $V_{dc\_nom}/2$

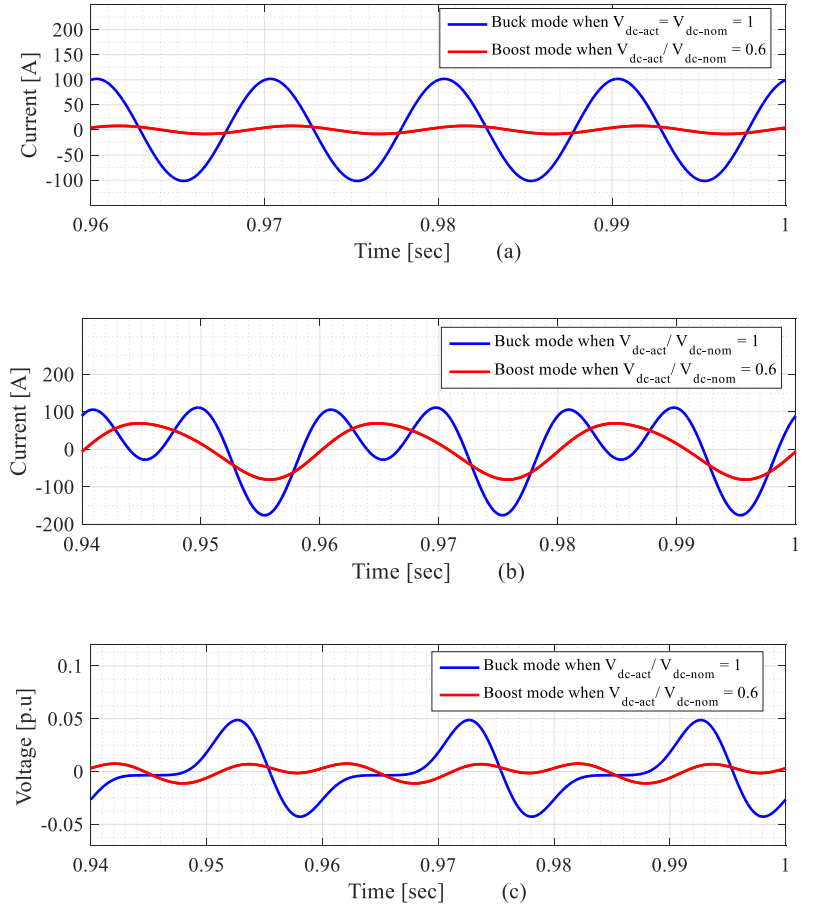


Fig 4.16 Comparison results of the analytical model of the FB-MMC while operating in the buck and boost modes under different dc link levels, (a) the 2nd harmonic circulating currents, (b) the upper arm currents, (c) capacitor voltages of the upper arm FB-submodules normalised by V_C

4.4.2.3 When FB-submodule capacitor voltage is reduced according to the dc link voltage level

Based on the second approach of the capacitor voltage regulation defined by (3.17), the simulation results of the developed steady-state analytical model are also validated with the switching model results on the FB-MMC. In this case, the FB-MMC is achieved at the optimal operating point (i. e. $V_{dc\_act} = 60$ % of V_{dc_nom}) so that from (3.13) and (3.14) the ac and dc modulation indexes are calculated as M_{ac} = 1.25, M_{dc}= 0.75. In the simulation results, the upper and lower arm currents of both FB-MMC models are matched, as shown in Fig 4.17 (a) and (b). It can be indicated that these arm currents have more a fluctuation if compared to the first capacitor voltage regulation, That because the decrease in the 2nd harmonic circulating current is not adequate as shown Fig 4.17 (c) and Fig 4.18. Note that, in the switching model, the switching ripple currents still exist in each of the arm currents and circulating current. Based on the validation of both FB-MMC models, as presented in Fig 4.20 (a) and (b), the capacitor voltage ripples are maximum of 2.32 %. In this case of using (3.17), each dc capacitor voltage is reduced from 2.5 kV to 2 kV, which means that reduction reaches to 20 % as compared to the first regulation approach defined by (3.16). Note that Fig 4.20 (c) shows the effect of the reduction in I_{cir} on the amplitudes of the voltage ripple components. Furthermore, Fig 4.21 illustrates the output voltages of FB-submodules in the analytical and switched models. Note that each FB-submodule in the switching model is inserted with the reduced value of V_C in the positive and negative polarities. While in the analytical model, the dc offset of the average output voltage is related to V_{dc_act}. The upper and lower arm voltages are validated for both the analytical and switching models as Fig 4.22 (a) and (b). For this case, the dc offset of each arm voltage is generated at $V_{dc\_act}/2$. while the amplitude of the fundamental in arm voltages of both models are remained around $\hat{v_{ph}}/2N$ that to meet the requirements of the grid-connected FB-MMC. It can also be seen from switching mode, that arm voltages are

produced more level in the boost mode. In the harmonic spectrum, Fig 4.22 (c) illustrates the decrease in amplitudes of the ripple components in the arm voltages of both models as I_{cir} is minimised due to the boost operating mode. Fig 4.23 (a) shows a validation of the output phase voltages $v_{ph}(t)$ in the average and switching waveforms. Based on this operating point, it can be observed that the output phase voltages $v_{ph}(t)$ levels of the switching model are increased from nine to eleven that when the second approach of capacitor regulation is implemented. From Fig 4.23 (b), it shows a reduction in the amplitude of the 3rd ripple component in $v_{ph}(t)$ becomes 59.5% instead of 80.2 % that when the first capacitor voltage regulation is employed.

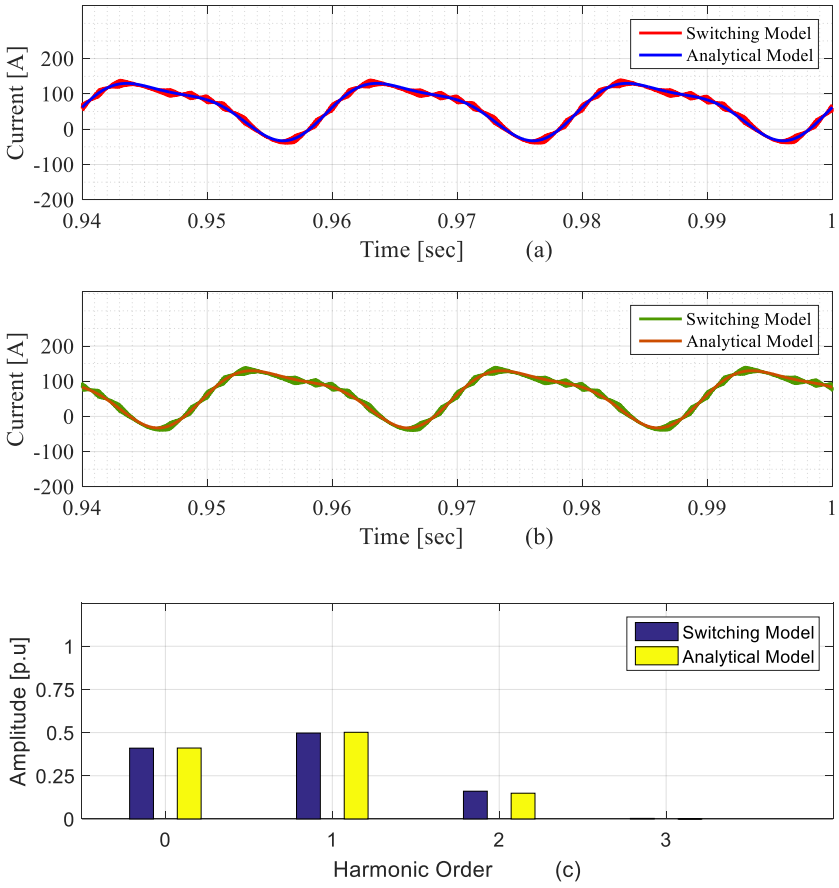


Fig 4.17 Comparison of the switching and analytical model arm currents when FB-MMC operates in the boost mode at V_{dc_act}= 60 % of V_{dc_nom}, M_{dc}= 0.75, M_{ac}= 1.25, PF = 1 and V_C defined by (3.17), (a)- Upper arm current (b)- Lower arm current (c)- Harmonic spectrum of the arm current components normalised by I_m

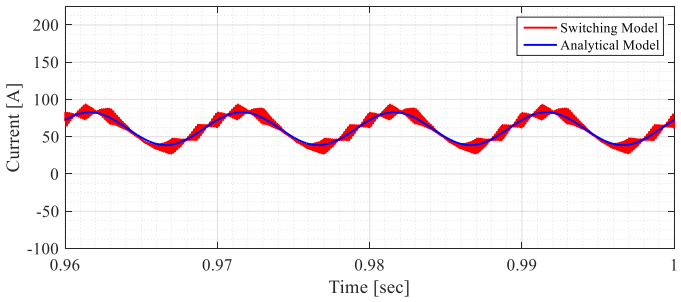


Fig 4.18 Comparison of the switching and analytical model the 2nd harmonic circulating currents when the FB-MMC operates in the boost mode at V_{dc_act}= 60 % of V_{dc_nom}, M_{dc}= 0.75, M_{ac}= 1.25, PF = 1 and V_C defined by (3.17)

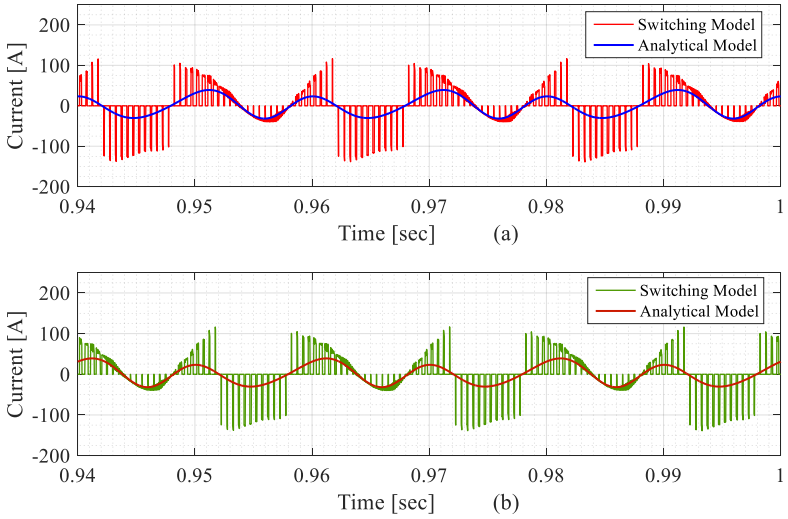


Fig 4.19 Comparison of the switching and analytical model capacitor currents when the FB-MMC operates in the boost mode at V_{dc_act}= 60 % of V_{dc_nom}, M_{dc}= 0.75, M_{ac}= 1.25,, PF = 1 and V_C defined by (3.17), (a)- Upper arm capacitor current (b)- Lower arm capacitor current

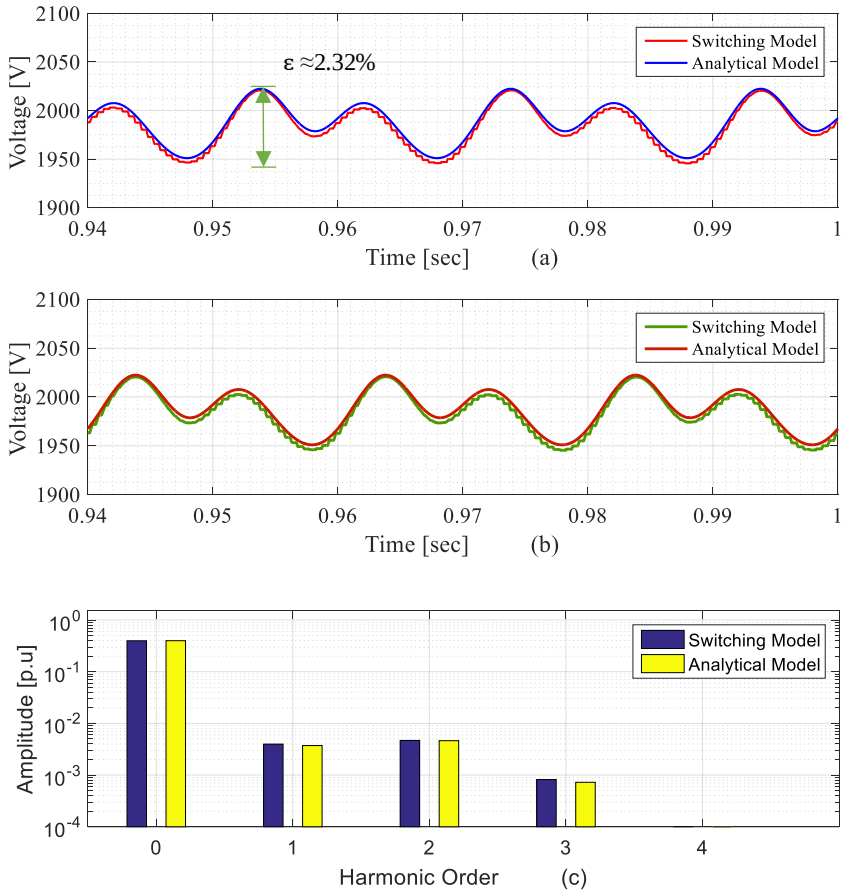


Fig 4.20 Comparison of the switching and analytical model arm voltages when FB-MMC operates in the boost mode at V_{dc_act}= 60 % of V_{dc_nom}, M_{dc}= 0.75, M_{ac}= 1.25, PF = 1 and V_C defined by (3.17),(a) Upper arm capacitor voltages (b) Lower arm capacitor voltages (c)- Harmonic spectrum of the capacitor voltage components normalised by $V_{dc\_nom}/2$

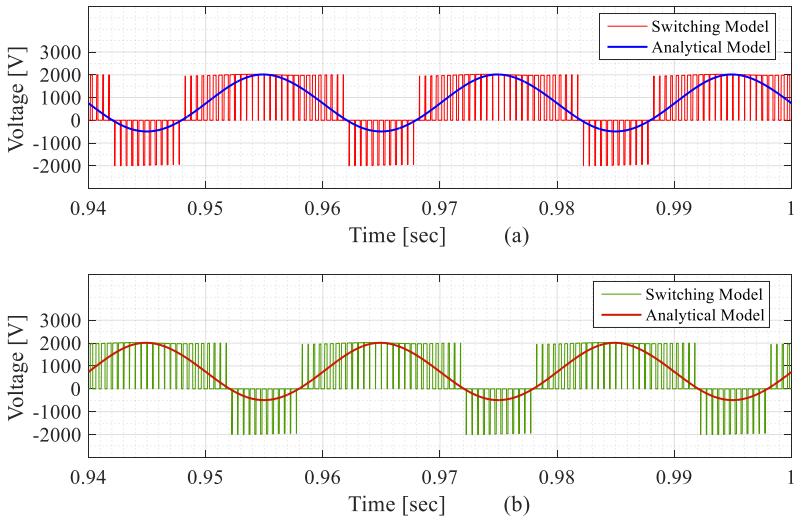


Fig 4.21 Comparison of the switching and analytical model submodule voltages when FB-MMC operates in the boost mode at V_{dc_act} = 60 % of V_{dc_nom}, M_{dc}= 0.75, M_{ac}= 1.25, PF = 1 and V_C defined by (3.17), (a) Upper arm submodule voltages (b) Lower arm submodule voltages

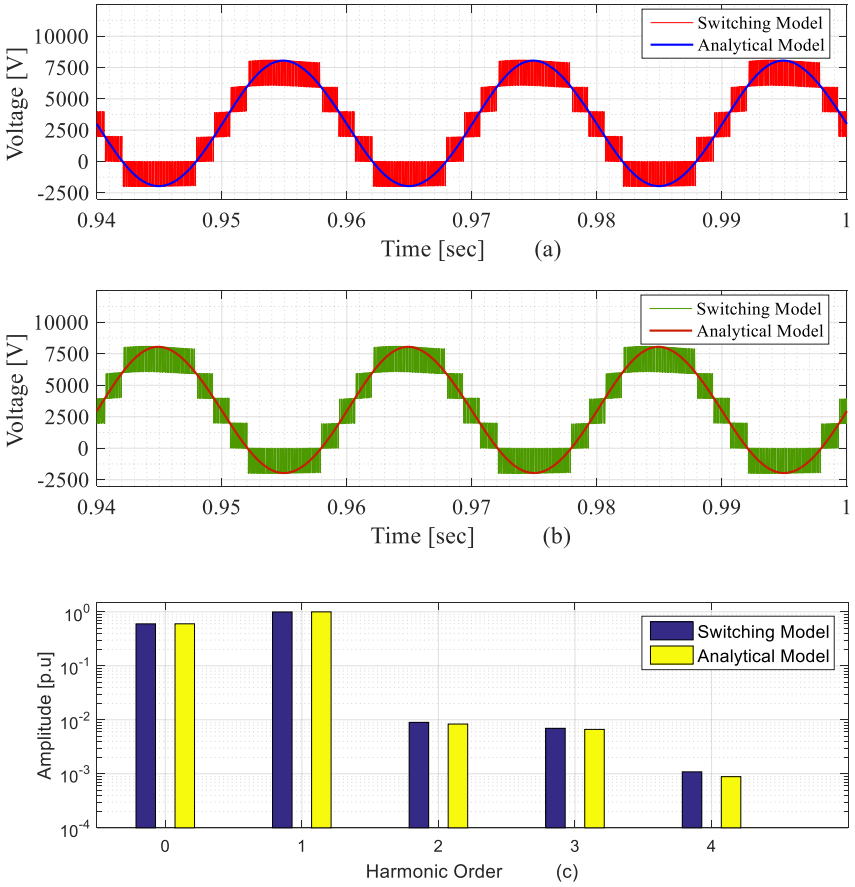


Fig 4.22 Comparison of the switching and analytical model arm voltages when the FB-MMC operates in the boost mode at V_{dc_act}= 60 % of V_{dc_nom}, M_{dc}= 0.75, M_{ac}= 1.25, PF = 1 and V_C defined by (3.17), (a)- Upper arm voltages (b)- Lower arm voltages (c)- Harmonic spectrum of arm voltages normalised by $V_{dc\_nom}/2$

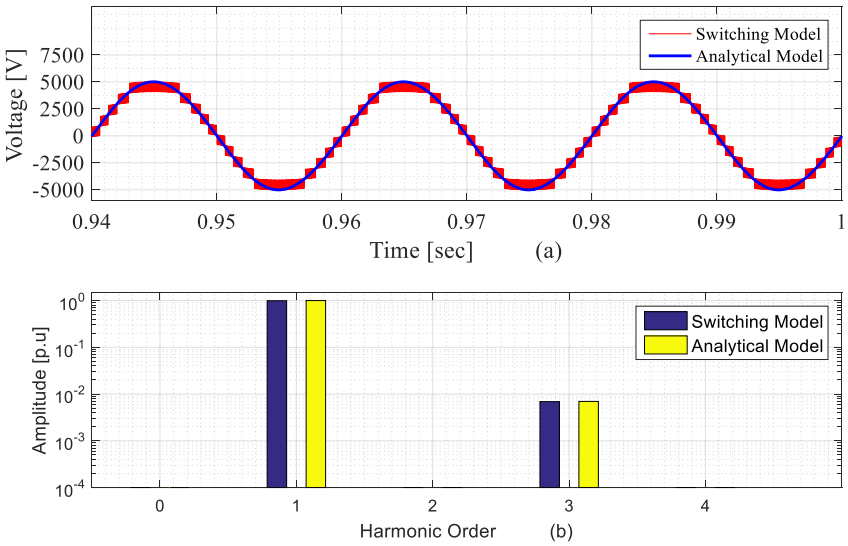


Fig 4.23 Comparison of the switching and analytical model output phase voltage when the FB-MMC operates in the boost mode at V_{dc_act}= 60 % of V_{dc_nom}, M_{dc}= 0.75, M_{ac} = 1.25, PF = 1 and V_C defined by (3.17), (a)- the output phase voltage (b)- Harmonic spectrum of the output phase voltage components normalised by $V_{dc\_nom}/2$

4.4.2.4 Comparison results of the FB-submodule capacitor voltage regulation approach in the boost mode

In this section, the comparison results using the validated analytical model are made to show a difference in the two capacitor voltage regulation approaches. In which the FB-MMC operates in the boost mode. Note that the boost mode regards the optimal operating point. For the second regulation approach defined by (3.17), it can be observed from Fig 4.24 that the RMS value of the circulating current I_{cir} is increased from 5.71 to 16.7 A, as compared with (3.16). That may lead to the power losses of the converter to be increased. For the upper arm as an example, Fig 4.24 shows the arm currents waveform which influenced by the value of I_{cir}. Although, the capacitor voltage ripple increases from 1.48 % to 2.32 % regarding the approach in (3.17), this voltage ripple is acceptable, as an acceptable capacitor voltage fluctuation can be reached up to 10 % [100], [114].

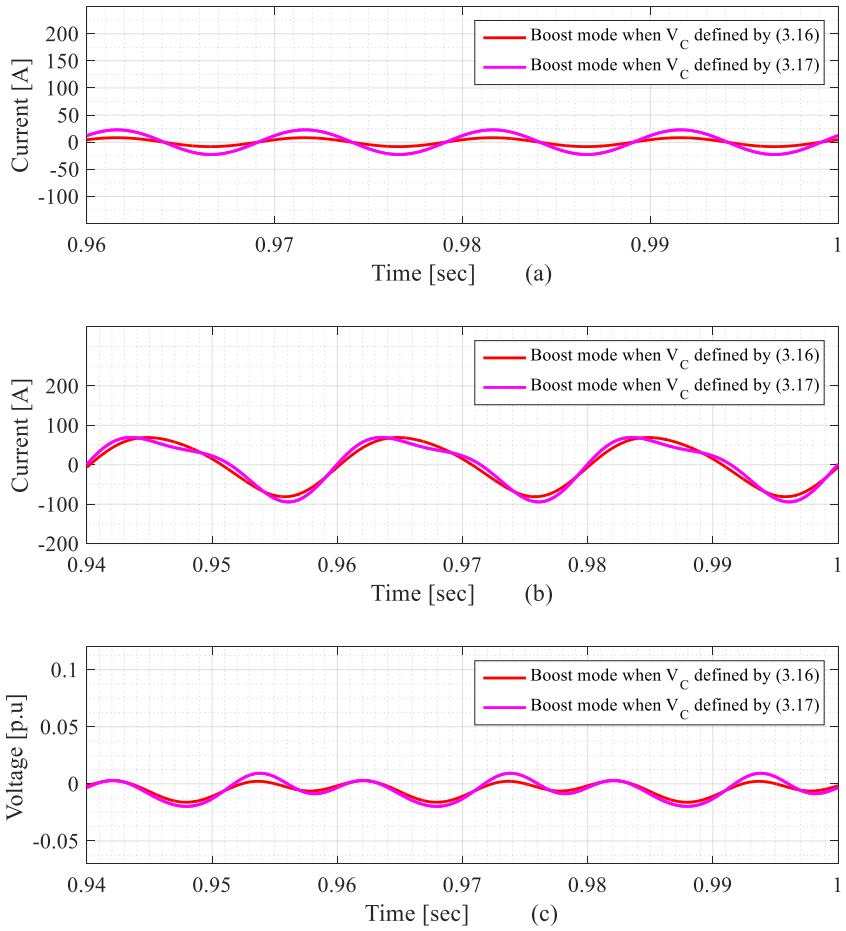


Fig 4.24 Comparison results of the FB-MMC analytical model while operating in the boost mode under two capacitor voltage regulation approaches at $V_{dc\_act} =$ 60 % of V_{dc_nom}, (a) the 2nd harmonic circulating currents, (b) the upper arm currents, (c) capacitor voltages of the upper arm FB-submodules normalized by V_C

4.5 Chapter summary

In this chapter, The steady-state analytical model was developed to be valid for the grid connected FB-MMC. Based on the circular interaction, analytical expressions have been established to describe low order harmonic components in the arm currents, submodule capacitor currents, submodule capacitor voltages, submodule output voltages, arm voltages, and output voltage of FB-MMC. The main contributions in Chapter 4 are that dependencies of capacitor voltage ripples and the

2nd harmonic circulating current are first revealed the influence of the dc link voltage while the FB-MMC working in the boost mode. Whereas these dependencies are represented using both dc and ac modulation indexes, which their values are used to specify the mode of the FB-MMC operation. Furthermore, analytical expressions for amplitude and phase angle of the 2nd order harmonic circulating current were developed to be valid the FB-MMC operates in the buck and boost modes. By setting different levels of the dc link voltage. The results revealed that the resonant inductance is also affected by the level of the dc link voltage and that the minimum circulating current at the resonant point is obtained for a dc link voltage of 60% of V_{dc_nom} which was also the optimal operating point with respect to the minimum circulating current and capacitor voltage ripples. The FB-MMC switching model based on the single-phase system was built using the MATLAB/Simulink that is to validate the developed analytical model. The obtained results of the switching model are matched and compared to those of the steady-state analytical model.

Chapter 5: Analytical harmonic solution for switched voltage waveforms of the full bridge - modular multilevel converter operating in the buck and boost modes

5.1 Introduction

This chapter presents a comprehensive analytical harmonic solution, which can allow identifying a harmonic behaviour of PWM switched output voltage waveforms of the FB-MMC. The analysis undertaken is to understand how the modulating signals, which defined by M_{ac} and M_{dc}, interact with the phase-shifted carriers to generate the high order frequency in the FB-MMC voltage waveforms. It shows an interaction of high order frequency harmonics, which caused by the arm voltages interleaving, as the FB-MMC operates in the buck and boost modes. For operating over entire the dc link voltage range, this analysis is utilised to calculate the THD value of switched output voltage. The influence of the two capacitor voltage regulation strategy, as discussed in Chapter 3, with/without including the displacement angle on the THD value are also considered. The analytical approach to identify a general formula for harmonic contents of PWM voltages is achieved based on a double Fourier series expansion in two time variables, and double edge naturally sampled PWM is adopted. For this case, the analytical expressions are derived for the submodule leg voltages, FB submodule output voltage, arm voltages and output phase voltage. The analytical results show that the THD behaviour of the output voltage might be exposed to nonlinearity regarding different operating points of the dc link voltage in boost mode. The proposed analytical solution to identify harmonic contents is evaluated by comparison with FFT analysis of simulated PWM output voltage waveforms, which results from the FB-MMC switching model.

5.2 General analytical harmonic solution for PWM voltage waveform

A generalized analysis employed to identify the harmonic contents of PWM voltages for two-level voltage source inverter 2L-VSI was first introduced in [79]. For different assumptions and operation conditions, some researchers have developed this analysis in [80], [81], [82] and [83]. Although the FFT analysis is commonly used to compute baseband and sideband harmonic contents of simulated PWM waveforms, the accuracy of FFT analysis can be very sensitive to a simulation time step (sample period), length and periodicity of the simulated PWM waveform. Alternatively, this generalized analysis in [79] can be more beneficial to determine these harmonic contains. The generalized analysis considers the phase-shifted carrier based PWM strategy. Thus, three different modulation strategies can be used, which are termed as naturally sampled PWM, asymmetrical regular sampled PWM and symmetrical regular sampled PWM [81]. For the case of the naturally sampled PWM approach, the modulating signals are naturally sampled as a conventional analogue technique [115]. Switched pulses resulted from an intersection of the modulating signal and carrier are modulated for both sides as the carrier is triangular waveform based. Hence, a type of modulation process is named a double-edge naturally sampled PWM. According to [81], an analytical solution for harmonic behaviour of one phase leg of two-level voltage source inverter VSI is obtained, that to determine baseband and sideband harmonic contents of PWM output voltage which is considered as a unit cell. The analytical solution here is achieved depending on a double Fourier series expansion in two time variables. The analytical solution variables of $x(t) = \omega_c t + \theta_c$ and $y(t) = \omega_0 t + \theta_0$ are assumed to describe time varying on the carrier waveform in the high-order frequency over the modulating signal at low-order frequency. These two variables are also considered to be an independently periodic cycle. The angular frequency of the triangular carriers and modulating signals are represented by ω_c and ω_0 , respectively. While the phase shift angles of the carrier waveforms and fundamental are denoted by θ_c and θ_0,

respectively. A solution trajectory line defines a relationship of $x(t)$ and $y(t)$ in the *x-y* plane as shown in the graphical representation of PWM implementation in Fig 5.1 (a) [81].

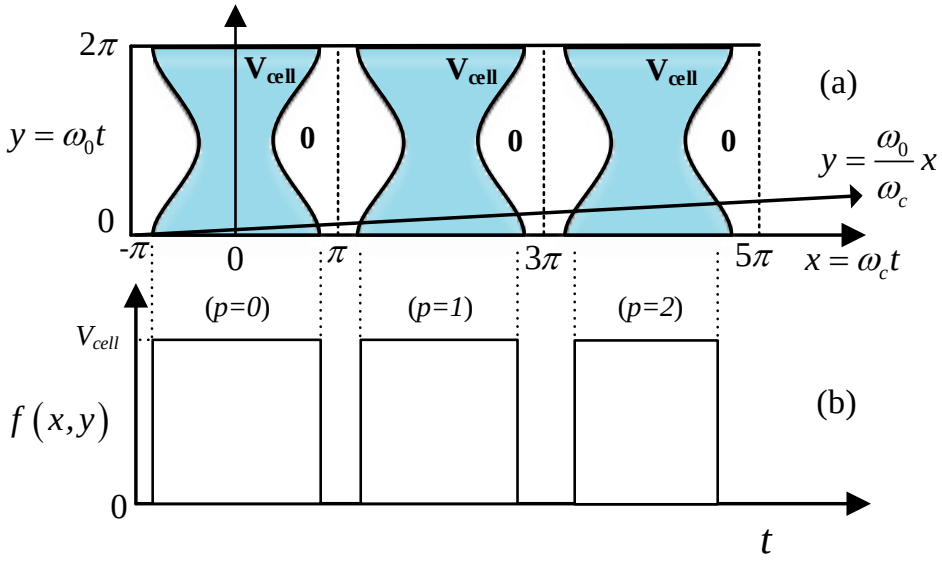


Fig 5.1 Graphical representation of the double edge naturally sampled PWM process for the cell voltage of the converter

It can be seen that time interval in the x-axis which corresponding to the carrier frequency is scaled in the range of ($-\pi < \omega_c < \pi$), while the y-axis is scaled in radians from 0 to 2π which corresponding fundamental frequency. Moreover, for the case of the angles θ_c and θ_0 are assumed to be zero, the switching instants for the double-edge naturally sampled PWM can be determined by the intersecting point between the trajectory line and boundary of two switching voltage levels as the follows:

$$y = \frac{\omega_0}{\omega_c} x \tag{5.1}$$

However, the boundary (the parts marked blue) describes an area of the constant values for the function $f(t) = f(x(t), y(t))$ in terms of the carrier waves and modulating signals are periodically varying. For this case, resulting PWM wave of the output voltage regards to the value of the function $f(t)$ as depicted in Fig

5.1(b) [81]. Of note that two switching voltage levels are from 0 to the terminal voltage across the dc side of the unit cell, that defined by V_{cell}. Any time varying function $f(t)$ is assumed as periodic in both x and y. Based on the double Fourier series, the general expression for harmonic contents can be given in the complex form C_{mn} as follows [81]:

$$C_{mn} = A_{mn} + jB_{mn} = \frac{1}{2\pi^2} \int_{-\pi}^{\pi} \int_{-\pi}^{\pi} f(x,y) e^{j(mx+ny)}\, dxdy \tag{5.2}$$

Where coefficients A_{mn} and B_{mn} can be obtained as the following expressions:

$$A_{mn} = \frac{1}{2\pi^2} \int_{-\pi}^{\pi} \int_{-\pi}^{\pi} f(x,y) \cos(mx + ny)\, dxdy \tag{5.3}$$

$$B_{mn} = \frac{1}{2\pi^2} \int_{-\pi}^{\pi} \int_{-\pi}^{\pi} f(x,y) \sin(mx + ny)\, dxdy \tag{5.4}$$

As introduced in [81], the general analytical solution to evaluate harmonics contents in based PSC-PWM method can be given by solving the double Fourier integral analysis above as follows:

$$\begin{aligned} f(x,y) = \frac{A_{00}}{2} &+ \sum_{n=1}^{\infty} \left[A_{0n} \cos\left(n(\omega_0 t + \theta_0)\right) + B_{0n} \sin\left(n(\omega_0 t + \theta_0)\right)\right] \\ &+ \sum_{m=1}^{\infty} \left[A_{m0} \cos\left(m(\omega_c t + \theta_c)\right) + B_{m0} \sin\left(m(\omega_c t + \theta_c)\right)\right] \\ &+ \sum_{m=1}^{\infty} \sum_{\substack{n=-\infty \\ n\neq 0}}^{\infty} \left[A_{mn} \cos\left(n(\omega_0 t + \theta_0) + m(\omega_c t + \theta_c)\right)\right. \\ &\left. + B_{mn} \sin\left(n(\omega_0 t + \theta_0) + m(\omega_c t + \theta_c)\right)\right] \end{aligned} \tag{5.5}$$

Where Fourier expansion of $f(x, y)$ is expressed at any time-varying as a sum of sinusoidal harmonic contents. It can be noted that values of the harmonic contents are defined using Fourier expansion coefficients A_{mn} and B_{mn}. Of note that the angular frequency of each harmonic can be defined using the carrier index variable *m* and baseband index variable *n*. The harmonic order of the carrier multiplies can be represent by *m* in the range of ($m = 1, \ldots, \infty$), while *n* defines harmonic order for the baseband and sideband contents in the range of ($n = -\infty, \ldots, -1, 0, 1, \ldots, \infty$). As the general formula of (5.5) can be utilised to express a harmonic spectrum of PWM switched output voltage of the converter. The first term refers to half of the dc component of PWM voltage waveform in which the index variables ($m = 0$, $n = 0$). Moreover, the first summation term donates to the baseband harmonics with low order frequency around the fundamental component at ($m = 0$, $n \neq 0$). In the second summation, it indicates to the carrier wave harmonics with high order frequency at the index variables at ($m \neq 0$, $n = 0$). While the term of the double summation refers to the sideband harmonics in high order frequency which centred around the carrier multiples when the baseband and carrier index variables with ($m \neq 0$, $n \neq 0$), respectively.

5.3 Proposed analytical modelling for indenting harmonic contents of PWM voltage waveforms in the FB-MMC

Based on the analytical harmonic solution presented in the previous section, this work develops an analytical modelling to express harmonic contents for PWM voltage waveforms of the FB-MMC. The analysis is undertaken to expose how different levels of the dc link voltage can influence a behaviour of harmonic contents in high order frequencies, as the FB-MMC works at buck and boost modes. In order to achieve this, the analytical harmonic solution given in which the developed modulating signals defined by M_{ac} and M_{dc} are modulated with the phased shifted carriers. This modulation approach here is considered as the double-edge naturally

sampled PWM. In terms of the harmonic performance evaluation in the FB-MMC, analytical expressions are calculated for the FB-submodule left and right leg voltages, lower and upper FB submodule voltages, and lower and upper arm voltages and output phase voltage.

5.3.1 Analytical harmonic solution for FB-submodule output voltage

In order to evaluate the performance of harmonic contents of switched FB-submodule voltage, it is necessary to establish an analytical modelling of PWM waves for each submodule voltage leg. For the case of the switching model, the main and complementary switches of each leg are modulated by a comparison of the modulating and triangular carrier waveforms. Whereas a comparison result switches the FB-submodule leg to the dc capacitor voltage of V_C, in which the modulating signal is higher than the carrier waveform. Otherwise, the FB-submodule leg is switched to zero voltage. According to the modulation process, a resultant switched voltage in each FB-submodule leg produces a stream of voltage pulses with the value of V_C and zero. This resultant switched voltage waveform is composed of carrier/sideband harmonics in the high order frequencies besides the dc component and fundamental. Of note that any baseband harmonic is not considered as this analytical solution uses the double edge modulation with the naturally sampled PWM [81].

Based on the developed PSC-PWM scheme, which illustrated in Chapter 3, an analytical solution to identify harmonic contents of the switched voltage leg can be correlated to the dc and ac modulation indexes. As values of M_{dc} and M_{ac} specify the operation of the FB-MMC in the buck and boost modes, the analytical solution in this work can provide an influence of the dc link voltage on amplitudes of these harmonic contents for each switched voltage wave of FB submodule leg.

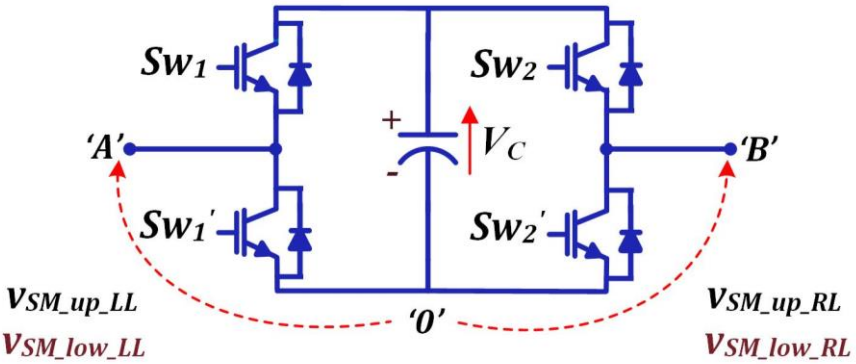


Fig 5.2 Circuit configuration of FB submodule illustrating output voltage for both left and right legs in the upper or lower arm

In Fig 5.2, it presents a circuit structure of FB submodule in upper or lower arms, which illustrates the switched voltage waveform generated across terminals in each leg of the FB-submodule. For the upper arm FB submodule, the switched voltage of the left leg which denoted by $v_{SM\_up\_LL}(t)$ appears on the submodule terminal 'A' that related to '0'. While the switched voltage waveform of the right leg $v_{SM\_up\_RL}(t)$ can be found from submodule terminal 'B' and '0'.

In this research work, the analytical modelling of the switched voltage wave of each leg determines the harmonic contents based on the analysis of the unit cell introduced in [81]. Accordingly, the analytical harmonic solution regarding the double-edge naturally sampled PWM as illustrated in Fig 5.1 is used for this purpose. Hence, a position of the switched pulses of one leg (rising and falling edges) is obtained from the intersections of the trajectory solution line and the boundary for two switching voltage levels (areas coloured blue). From the modulating signal/carrier comparison, the rising edge x_r and falling edges x_f can also be determined from the switching instants as indicated in Fig 5.3.

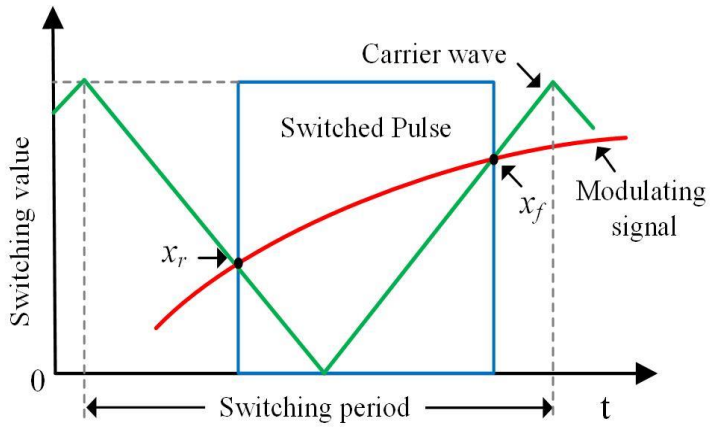


Fig 5.3 Switched pulse process based on the double edge naturally sampling PWM

For the main switch in the left leg of the FB-submodule, the modulating signal $m_{up\_LL}(t)$ defined by (3.10) is rearranged to fulfil the approach of the analytical harmonic solution. As a result, the switching instants to represent the rising edge x_r can be expressed in which the $f(t)$ changes from 0 to $+V_C$ as follows:

$$x_r = 2\pi p - \pi\left(\frac{1}{2} + \frac{M_{dc}}{4} - \frac{M_{ac}}{4}\cos(y)\right) \tag{5.6}$$

While the falling edge x_f of the switching instants when the $f(t)$ changes from $+V_C$ to 0 can be expressed as:

$$x_f = 2\pi p + \pi\left(\frac{1}{2} + \frac{M_{dc}}{4} - \frac{M_{ac}}{4}\cos(y)\right) \tag{5.7}$$

Where the sample period index is defined by (p=1, 2, 3 …). The expressions (5.6) and (5.7) represent the inner integral limits of this type of the modulating process. Based on the double integration analytical solution, the inner and outer integral limits can be specified using (5.2), (5.6) and (5.7) as the following:

$$A_{mn} + jB_{mn} = \frac{1}{2\pi^2} \int_{-\pi}^{\pi} \int_{-\pi\left(\frac{1}{2}+\frac{M_{dc}}{4}-\frac{M_{ac}}{4}\cos(y)\right)}^{\pi\left(\frac{1}{2}+\frac{M_{dc}}{4}-\frac{M_{ac}}{4}\cos(y)\right)} V_C \, e^{j(mx+ny)} \, dxdy \tag{5.8}$$

The analytical solution in this research work assumes that the FB-submodule capacitor voltage V_C is correspondent to the dc link voltage $2V_{dc}$ of the 2L-VSC [81]. In this analytical solution, it is also considered that the FB- submodule capacitor voltage is fixed at the dc component value, (i.e. the voltage ripples across the FB-submodule capacitor are neglected). According to (5.8), the particular values of the carrier index variable *m* and baseband index *n* are employed to evaluate various magnitudes of the low and high order harmonic components, which generated by the switched voltage of FB-submodule leg. Therefore, Fourier expansion coefficients as the dc-component can be evaluated when $m = n = 0$ as follows:

$$A_{00} + jB_{00} = \frac{V_C}{2\pi^2} \int_{-\pi}^{\pi} \int_{-\pi\left(\frac{1}{2}+\frac{M_{dc}}{4}-\frac{M_{ac}}{4}\cos(y)\right)}^{\pi\left(\frac{1}{2}+\frac{M_{dc}}{4}-\frac{M_{ac}}{4}\cos(y)\right)} dxdy \tag{5.9}$$

By solving both inner and outer integrals, respectively, the evaluation of these coefficients yields to:

$$\begin{aligned} A_{00} + jB_{00} &= \frac{V_C}{2\pi^2} \int_{-\pi}^{\pi} 2\pi \left(\frac{1}{2} + \frac{M_{dc}}{4} - \frac{M_{ac}}{4}\cos(y)\right) dy \\ &= V_C \left(1 + \frac{M_{dc}}{2}\right) \end{aligned} \tag{5.10}$$

Note that the dc component (offset) of this analytical solution is $A_{00}/2$. To determine the coefficients in the fundamental, they can be obtained when $m = 1, n = 0$, as follows:

$$A_{0n} + jB_{0n} = \frac{V_C}{2\pi^2} \int_{-\pi}^{\pi} \int_{-\pi\left(\frac{1}{2}+\frac{M_{dc}}{4}-\frac{M_{ac}}{4}\cos(y)\right)}^{\pi\left(\frac{1}{2}+\frac{M_{dc}}{4}-\frac{M_{ac}}{4}\cos(y)\right)} e^{jny} \, dxdy \tag{5.11}$$

The analytical solution of the inner integral is given as:

$$A_{0n} + jB_{0n} = \frac{V_C}{2\pi^2} \int_{-\pi}^{\pi} 2\pi \left(\frac{1}{2} + \frac{M_{dc}}{4} - \frac{M_{ac}}{4}\cos(y)\right) e^{jny} dy \qquad (5.12)$$

Considering Euler's formula of the cosine function which is:

$$cos(a) = \frac{\left[e^{ja} - e^{-ja}\right]}{2} \qquad (5.13)$$

That simplifies to:

$$A_{0n} + jB_{0n} = \frac{V_C}{\pi} \int_{-\pi}^{\pi} \left[\left(\frac{1}{2} + \frac{M_{dc}}{4}\right) e^{jny} - \frac{M_{ac}}{8} e^{j(n+1)y} + \frac{M_{ac}}{8} e^{j(n-1)y}\right] dy \qquad (5.14)$$

According to the outer integral, both first and second terms of the above expression (5.14) can be solved as follows:

$$\int_{-\pi}^{\pi} \left(\frac{1}{2} + \frac{M_{dc}}{4}\right) e^{jny} dy = \left(\frac{1}{2} + \frac{M_{dc}}{4}\right) \frac{e^{jn\pi} - e^{-jn\pi}}{jn} = \left(\frac{1}{2} + \frac{M_{dc}}{4}\right) \frac{e^{j\pi} - e^{-j\pi}}{jn} = 0 \qquad (5.15)$$

Then it becomes as:

$$\int_{-\pi}^{\pi} -\frac{M_{ac}}{8} e^{j(n+1)y} dy = -\frac{M_{ac}}{8} \left\{\frac{e^{j(n+1)\pi} - e^{-j(n+1)\pi}}{jn}\right\} = -\frac{M_{ac}}{8} \left\{\frac{e^{j2\pi} - e^{-j2\pi}}{j2}\right\} = 0 \qquad (5.16)$$

It can be seen that the solution of these terms results in zero for $n \geq 1$. However, the third term of (5.14) is integrated to be as

$$\int_{-\pi}^{\pi} \frac{M_{ac}}{8} e^{j(n-1)y} dy = \int_{-\pi}^{\pi} \frac{M_{ac}}{8} dy = \pi \frac{M_{ac}}{4} \tag{5.17}$$

Consequently, the evaluating coefficients for this case can be given as the following:

$$A_{0n} + jB_{0n} = \frac{M_{ac}}{4} V_C \tag{5.18}$$

On the contrary, the coefficients for the carrier harmonics when *m>0*, *n=0* can be given as follows:

$$\begin{aligned} A_{m0} + jB_{m0} &= \frac{V_C}{2\pi^2} \int_{-\pi}^{\pi} \int_{-\pi\left(\frac{1}{2}+\frac{M_{dc}}{4}-\frac{M_{ac}}{4}\cos(y)\right)}^{\pi\left(\frac{1}{2}+\frac{M_{dc}}{4}-\frac{M_{ac}}{4}\cos(y)\right)} e^{jmx} dx dy \\ &= \frac{V_C}{2jm\pi^2} \int_{-\pi}^{\pi} \begin{Bmatrix} e^{jm\pi\left(\frac{1}{2}+\frac{M_{dc}}{4}\right)} e^{jm\pi\left(-\frac{M_{ac}}{4}\cos(y)\right)} \\ -e^{-jm\pi\left(\frac{1}{2}+\frac{M_{dc}}{4}\right)} e^{jm\pi\left(\frac{M_{ac}}{4}\cos(y)\right)} \end{Bmatrix} dy \end{aligned} \tag{5.19}$$

According to Jacobi-Anger expansions which are:

$$\int_{-\pi}^{\pi} e^{j\xi\cos(z)} e^{jnz} dz = 2\pi j^n J_n(\xi)$$

In the case of *n=0*, (5.20)

$$\int_{-\pi}^{\pi} e^{j\xi\cos(z)} dz = 2\pi J_0(\xi) = 2\pi J_0(-\xi)$$

Whereas $J_n(z)$ denotes to the first kind - Bessel functions of order *n* and value of the argument z [81]. This analytical solution can be simplified as:

$$A_{m0} + jB_{m0} = \frac{V_C}{jm\pi} J_0(-m\frac{\pi}{4}M_{ac}).\left\{e^{jm\pi\left(\frac{1}{2}+\frac{M_{dc}}{4}\right)} - e^{-jm\pi\left(\frac{1}{2}+\frac{M_{dc}}{4}\right)}\right\}$$
$$= \frac{2V_C}{m\pi} J_0(m\frac{\pi}{4}M_{ac}).\sin(m(2+M_{dc})\frac{\pi}{4}) \quad (5.21)$$

Of note that Euler's formula of the sine function used to simplify the above expression is:

$$sin(a) = \frac{\left[e^{ja} - e^{-ja}\right]}{2j} \quad (5.22)$$

In a case when index variables $m>0$ and $n \neq 0$, the coefficients of the baseband harmonics are defined as follows:

$$A_{mn} + jB_{mn} = \frac{V_C}{2\pi^2} \int_{-\pi}^{\pi} \int_{-\pi\left(\frac{1}{2}+\frac{M_{dc}}{4}-\frac{M_{ac}}{4}\cos(y)\right)}^{\pi\left(\frac{1}{2}+\frac{M_{dc}}{4}-\frac{M_{ac}}{4}\cos(y)\right)} e^{j(mx+ny)} dxdy$$
$$= \frac{V_C}{2jm\pi^2} \int_{-\pi}^{\pi} \begin{Bmatrix} e^{jm\pi\left(\frac{1}{2}+\frac{M_{dc}}{4}\right)} e^{jm\pi\left(-\frac{M_{ac}}{4}\cos(y)\right)} e^{jny} \\ -e^{-jm\pi\left(\frac{1}{2}+\frac{M_{dc}}{4}\right)} e^{jm\pi\left(\frac{M_{ac}}{4}\cos(y)\right)} e^{jny} \end{Bmatrix} dy \quad (5.23)$$

Following Jacobi-Anger expansions [81], the above expression can be rewritten as follows:

$$A_{mn} + jB_{mn} = \frac{V_C}{jm\pi} \cdot \begin{Bmatrix} j^{-n} J_n(-m\frac{\pi}{4}M_{ac})\ e^{jm\pi\left(\frac{1}{2}+\frac{M_{dc}}{4}\right)} \\ -j^n J_n(m\frac{\pi}{4}M_{ac})\ e^{-jm\pi\left(\frac{1}{2}+\frac{M_{dc}}{4}\right)} \end{Bmatrix} \quad (5.24)$$

By considering Euler's formula of the sine function [81], the analytical solution of the coefficients can be simplified to:

$$A_{mn} + jB_{mn} = \frac{2V_C}{m\pi}\ (-1)^n J_n(m\frac{\pi}{4}M_{ac})\sin((m(2+M_{dc})+2n)\frac{\pi}{4}) \qquad (5.25)$$

The coefficients derived in (5.10), (5.18), and (5.25) are substituted into (5.5), that to express the harmonic contents of any time-varying switched voltage waveform of each FB-submodule left leg in the upper arm as follows:

$$\begin{aligned} v_{SM\_up\_LL}(t) &= \frac{V_C}{2} + \frac{M_{dc}V_C}{4} - \frac{M_{ac}V_C}{4}\cos(\omega_0 t) \\ &+ \frac{2V_C}{\pi m}\sum_{m=1}^{\infty}\left\{J_0(m\frac{\pi}{4}M_{ac})\ sin\left((2+M_{dc})m\frac{\pi}{4}\right)\right\}.\cos(m\omega_c t) \\ &+ \frac{2V_C}{\pi m}\sum_{m=1}^{\infty}\sum_{\substack{n=-\infty \\ n\neq 0}}^{\infty}\left\{(-1)^n J_n(m\frac{\pi}{4}M_{ac})\ sin\left([(2+M_{dc})m+2n]\frac{\pi}{4}\right)\right\}. \\ &\qquad\qquad \cos(m\omega_c t + n\omega_0 t) \end{aligned} \qquad (5.26)$$

Similarly, for switched voltage wave of each right leg in the same FB submodule, the modulating signal $m_{up\_RL}(t)$ defined in (3.11) can be used to derive an expression for harmonic contents. In this case, the analytical harmonic solution can be given as follows:

$$\begin{aligned} v_{SM\_up\_RL}(t) &= \frac{V_C}{2} - \frac{M_{dc}V_C}{4} + \frac{M_{ac}V_C}{4}\cos(\omega_0 t) \\ &+ \frac{2V_C}{\pi m}\sum_{m=1}^{\infty}\left\{J_0(m\frac{\pi}{4}M_{ac})\ sin\left((2-M_{dc})m\frac{\pi}{4}\right)\right\}.\cos(m\omega_c t) \\ &+ \frac{2V_C}{\pi m}\sum_{m=1}^{\infty}\sum_{\substack{n=-\infty \\ n\neq 0}}^{\infty}\left\{J_n(m\frac{\pi}{4}M_{ac})\ sin\left([(2-M_{dc})m+2n]\frac{\pi}{4}\right)\right\}. \\ &\qquad\qquad \cos(m\omega_c t + n\omega_0 t) \end{aligned} \qquad (5.27)$$

The analytical harmonic solution derived in (5.26) and (5.27) can provide a relation of the modulation indexes and amplitudes of the odd and even carrier\sideband harmonic contents. As the first carrier group achieves at m_f (which represents a frequency ratio f_{sw}/f_0), an existence or cancellation of these harmonic groups in high order frequencies are significantly affected by operating points of

FB-MMC in the buck and boost modes. It can also be noted that two of the dc components are generated across each voltage leg. The first dc component is constant at $V_C/2$, while the second one $M_{dc}V_C/4$ varies in accordance with the dc link voltage levels. The fundamental generated by each FB- submodule leg is related to $M_{ac}V_C/4$. Also, the analysis can show an impact of the capacitor voltage regulation approaches on the amplitude of all harmonic contents under different operating conditions. To validate the analytical expressions derived in (5.26) or (5.27) against those of the half bridge submodule, they can be revised by setting M_{dc} with zero and replacing $M_{ac}$with $2M_{ac}$ [85], [86]. The harmonic contents of time varying switched output voltages for any FB submodule in the upper arm $v_{SM\_up}(t)$ can be evaluated from those of the left and right voltage legs. According to (5.26) and (5.27), the harmonic contents of the $v_{SM\_up}(t)$ can be calculated from a subtraction of $\{v_{SM\_up\_LL}(t) - v_{SM\_up\_RL}(t)\}$. In this case, a resultant switching frequency of the FB-submodule output voltage is twice of the device switching frequency, and the first carrier harmonic group achieves at $2m_f$. Consequently, amplitudes and orders of carrier\sideband harmonic contents of $v_{SM\_up}(t)$ are identified in this work by replacing the carrier index variable m with $2m$, as compared to the expressions in (5.26) and (5.27). Hence, it can be given as follows:

$$
\begin{aligned}
v_{SM\_up}(t) &= v_{SM\_up\_LL}(t) - v_{SM\_up\_RL}(t) \\
&= \frac{M_{dc}V_C}{2} - \frac{M_{ac}V_C}{2}\cos(\omega_0 t) \\
&+ \frac{V_C}{\pi m}\sum_{m=1}^{\infty} J_0\left(m\frac{\pi}{2}M_{ac}\right)\begin{Bmatrix} sin\left((2+M_{dc})m\frac{\pi}{2}\right) \\ -sin\left((2-M_{dc})m\frac{\pi}{2}\right)\end{Bmatrix}.\cos(m\omega_c t) \\
&+ \frac{V_C}{\pi m}\sum_{m=1}^{\infty}\sum_{\substack{n=-\infty \\ n\neq 0}}^{\infty} J_n\left(m\frac{\pi}{2}M_{ac}\right)\begin{Bmatrix} (-1)^n\ sin\left([(2+M_{dc})m+n]\frac{\pi}{2}\right) \\ -sin\left([(2-M_{dc})m+n]\frac{\pi}{2}\right)\end{Bmatrix}. \\
&\qquad \cos(m\omega_c t + n\omega_0 t)
\end{aligned}
\tag{5.28}
$$

Similarly, the analytical harmonic solution based on the developed modulating signals based on (3.8) and (3.9) can be used, that to identify harmonic contents of time-varying switched output voltages for any FB submodule in the lower arm can be given as follows:

$$v_{SM\_low}(t) = v_{SM\_low\_LL}(t) - v_{SM\_low\_RL}(t)$$

$$= \frac{M_{dc}V_C}{2} + \frac{M_{ac}V_C}{2}\cos(\omega_0 t)$$

$$+ \frac{V_C}{\pi m}\sum_{m=1}^{\infty} J_0\left(m\frac{\pi}{2}M_{ac}\right)\begin{Bmatrix} sin\left((2-M_{dc})m\frac{\pi}{2}\right) \\ -sin\left((2+M_{dc})m\frac{\pi}{2}\right)\end{Bmatrix}.\cos(m\omega_c t) \qquad (5.29)$$

$$+ \frac{V_C}{\pi m}\sum_{m=1}^{\infty}\sum_{\substack{n=-\infty \\ n\neq 0}}^{\infty} J_n\left(m\frac{\pi}{2}M_{ac}\right)\begin{Bmatrix} sin\left([(2-M_{dc})m+2n]\frac{\pi}{2}\right) \\ -\ (-1)^n\ sin\left([(2+M_{dc})m+2n]\frac{\pi}{2}\right)\end{Bmatrix}. \cos(m\omega_c t + n\omega_0 t)$$

Under different dc link voltage levels, the carrier\sideband of these harmonic groups (amplitude and order) will be studied and compared, as they are influenced by both ac and dc modulation indexes while FB-MMC in the buck and boost operating modes.

5.3.2 Analytical harmonic solution for switched output phase voltage of FB-MMC

Because each FB-MMC arm is configured with the cascaded connection of the N^{th} number of FB-submodules, harmonic contents of switched arm voltage can be determined from the analytical harmonic solution of the FB-submodule output voltage. In this case, harmonic cancellation can be optimally achieved as the phase angle for triangular carriers of each FB-submodule is shifted by π/N. Therefore, only sideband harmonics centred around N^{th} multiples of the carrier harmonic

group can exist in the harmonic spectrum [2], [85], [116]. Accordingly, the harmonic contents for time-varying switched voltage on the upper arm can be evaluated as follows:

$$v_{arm\_up}(t) = N.v_{SM\_up}(t) = \frac{NM_{dc}V_C}{2} - \frac{NM_{ac}V_C}{2}\cos(\omega_0 t)$$

$$+\frac{V_C}{\pi m}\sum_{m=1}^{\infty} J_0(mN\frac{\pi}{4}M_{ac}) \begin{Bmatrix} sin\left((2+M_{dc})mN\frac{\pi}{2}\right) \\ -sin\left((2-M_{dc})mN\frac{\pi}{2}\right) \end{Bmatrix}.\cos(m\omega_c t) \quad (5.30)$$

$$+\frac{V_C}{\pi m}\sum_{m=1}^{\infty}\sum_{\substack{n=-\infty \\ n\neq 0}}^{\infty} J_n(mN\frac{\pi}{2}M_{ac}) \begin{Bmatrix} (-1)^n\ sin\left([(2+M_{dc})mN+n]\frac{\pi}{2}\right) \\ -sin\left([(2-M_{dc})mN+n]\frac{\pi}{2}\right) \end{Bmatrix}. \cos(m\omega_c t + n\omega_0 t)$$

It can be observed that the analytical expression of $v_{SM\_up}(t)$ which defined by (5.28) is revised the high-frequency harmonics by replacing m with mN, that allows to identify amplitudes of carrier\sideband harmonic contents of $v_{arm\_up}(t)$. Similarly, an expression to identify harmonic contents of the lower arm voltage $v_{arm\_low}(t)$ can be written depending on (5.29) as follows:

$$v_{arm\_low}(t) = N.v_{SM\_up}(t) = \frac{NM_{dc}V_C}{2} + \frac{NM_{ac}V_C}{2}\cos(\omega_0 t)$$

$$+\frac{V_C}{\pi m}\sum_{m=1}^{\infty} J_0(mN\frac{\pi}{2}M_{ac}) \begin{Bmatrix} sin\left((2-M_{dc})mN\frac{\pi}{2}\right) \\ -sin\left((2+M_{dc})mN\frac{\pi}{2}\right) \end{Bmatrix}.\cos(m\omega_c t) \quad (5.31)$$

$$+\frac{V_C}{\pi m}\sum_{m=1}^{\infty}\sum_{\substack{n=-\infty \\ n\neq 0}}^{\infty} J_n(mN\frac{\pi}{2}M_{ac}) \begin{Bmatrix} sin\left([(2-M_{dc})mN+n]\frac{\pi}{2}\right) \\ -\ (-1)^n sin\left([(2+M_{dc})mN+n]\frac{\pi}{2}\right) \end{Bmatrix}. \cos(m\omega_c t + n\omega_0 t)$$

Of note that the resultant switching frequency for each arm output voltage is $2N$ of the device switching frequency. If the number of the FB-submodule is even, further harmonic cancellation can be achieved by using the phase displacement angle θ_d [2], [85]. In this case, the carrier and sideband harmonic contents of the lower arm voltage $v_{arm\_low}(t)$ are needed to multiply a term $\{\cos(mN(\theta_d - \pi)/2\}$. Where this term for using the phase displacement angle is assessed and examined in this study. Harmonic contents for the output phase voltage of the FB-MMC is identified due to an interaction between harmonic contents of both the upper and lower arm voltages. Consequently, time-varying switched output phase voltage $v_{ph}(t)$ can be given by an expression of harmonic contents as follows:

$$v_{ph}(t) = \frac{v_{arm\_low}(t) - v_{arm\_up}(t)}{2} = \frac{M_{ac}NV_C}{2}\cos(\omega_0 t)$$
$$+\frac{V_C}{2\pi m}\sum_{m=1}^{\infty}\sum_{\substack{n=-\infty \\ n\neq 0}}^{\infty}\left(\begin{array}{l} J_n(mN\frac{\pi}{2}M_{ac})\left\{\begin{array}{c}(-1)^n\ sin\left([(2+M_{dc})mN+n]\frac{\pi}{2}\right) \\ -sin\left([(2-M_{dc})mN+n]\frac{\pi}{2}\right)\end{array}\right\} \\ J_n(mN\frac{\pi}{2}M_{ac})\left\{\begin{array}{c}sin\left([(2-M_{dc})mN+n]\frac{\pi}{2}\right) \\ -\ (-1)^n sin\left([(2+M_{dc})mN+n]\frac{\pi}{2}\right)\end{array}\right\} \end{array}\right) \quad (5.32)$$
$$.\cos(m\omega_c t + n\omega_0 t)$$

According to (3.32), the analytical harmonic solution can show that amplitudes of all even carrier\sideband harmonics are entirely eliminated in the $v_{ph}(t)$, as they have the same direction in both of the arm voltages. While those of odd carrier\ sideband harmonics still exist in the frequency spectrum. Therefore, the values of M_{dc} and M_{ac} which based on the buck and boost operating modes of the FB-MMC only influence amplitudes of the odd harmonics whether at high or low order frequencies. From (3.26)-(3.32), it can be seen that the M_{ac} only affects amplitudes of the harmonics, while the M_{dc} affects the frequency of the harmonics (harmonic order) besides their amplitudes.

5.4 Simulation results and discussion of the analytical harmonic solution for switched voltage waveform of FB-MMC

The analytical harmonic solution which proposed in this research work is evaluated over different operating conditions, that to identify amplitudes of harmonic contents which existed\cancelled in the switched voltage waveforms of the FB-MMC. Simulation results include amplitudes of harmonic contents for switched voltages for any FB-submodule, each arm and output phase of the FB-MMC. These results are used for a calculation of THD value of the output phase voltage $v_{ph}(t)$ while the operation of the FB-MMC covering a full range of dc link voltage. In this case, the analytical harmonic solution is implemented and simulated using MATLAB\M-files environment (see Appendix E). As a result, the analytical harmonics are validated by comparison with FFT results of those in a simplified switching model of the FB-MMC. Of note that this switching model is built to simulate these switched voltage waveforms regardless of a drop voltage of the arm inductors (see Appendix D). As for the analytical harmonic solution, the influence of the voltage ripples across FB-submodule capacitor is not taken into account in the simplified switching model. The simulation parameters for both analytical and switching models are defined by the FB-MMC details listed in Table 3.1.

5.4.1 Evaluation of THD for the output voltage based on the switching model of FB-MMC

Simulation results in this section are presented to show interleaving of the voltage arms in terms of THD performance and generated levels of the output phase voltage. Using the simplified switching model of the FB-MMC, Fig 5.4 shows the obtained values of THD when the dc link voltage that covers the range from 0 to V_{dc_nom}. Of note that simulation results here are achieved with no load condition, and an impact of the displacement angle is also not employed.

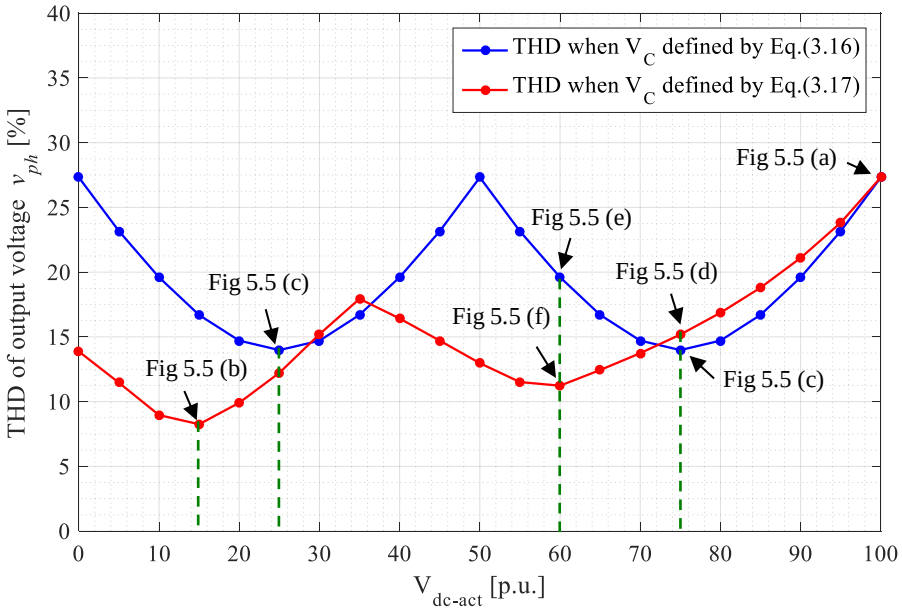


Fig 5.4 Comparison results of THD performance for the output voltage of FB-MMC under two different approaches of V_C regulation in the boost mode

Based on the THD curves shown in Fig 5.4, some operating points of the dc link voltage are selected in this analysis, to give a comparison of the two different approaches of V_C regulation. That considers better THD and the number of the voltage levels generated at $v_{ph}(t)$. For both regulation approaches of V_C, the results show that maximum THD value of 27.32 % is obtained at the buck mode as $V_{dc\_act} =$ 100 % of V_{dc_nom}. In this case, the output phase voltage $v_{ph}(t)$ is generated with five levels, and each voltage level is scaled to V_C which is equal to 2.5 kV, as shown in Fig 5.5 (a). In the boost mode, however, the THD can be achieved at a minimum value of 8.3 % in which the dc link voltage V_{dc_act} operates at 15 % of V_{dc_nom}, and V_C is regulated using the second approach in (3.17). In this case, the voltage levels of $v_{ph}(t)$ become fifteen and each voltage level is scaled to $V_C/2$ which is 719 V as shown in Fig 5.5 (b). While regulating V_C based on the first approach in (3.16) can achieves minimum THD value of 13.98 %, as V_{dc_act} operates at 25 % or 75% of V_{dc_nom}. For the latter operating point, Fig 5.5 (c) shows the output voltage has nine levels, each voltage level is scaled to $V_C/2$ of 1.25 kV.

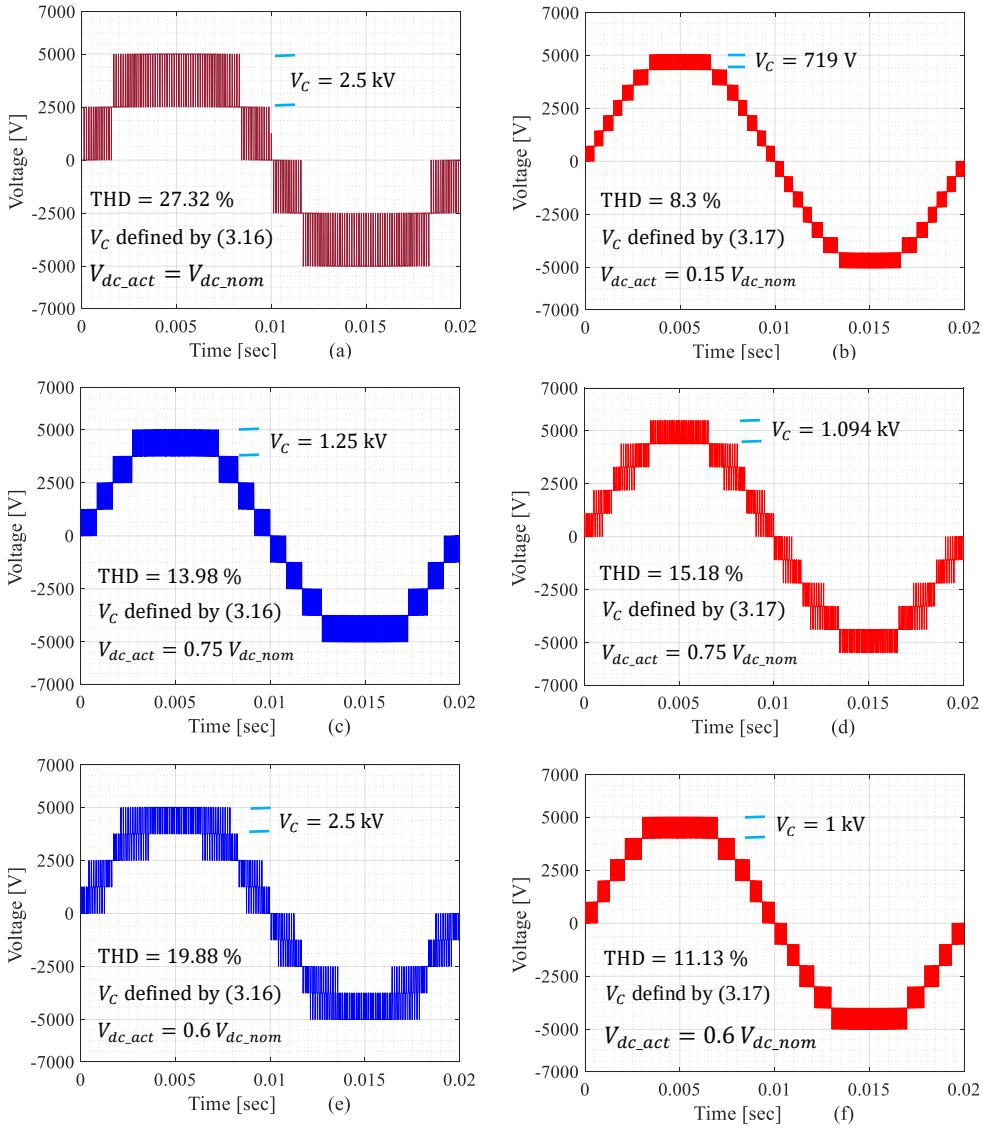


Fig 5.5 Comparison results of voltage levels generated in the output voltage waveform of FB-MMC when different dc link voltages achieved under two regulation approaches of V_C in buck and boost modes

At the same operating point, however, the THD value increases to 15.18% when the second regulation approach in (3.17) is applied. Although $v_{ph}(t)$ is generated at eleven levels (each level has $V_C/2$ at 1.094 kV), Fig 5.5 (d) reveals that is not the case of the optimal interleaving occurred between the voltage arms. In Fig 5.5 (f) shows that the same number of the voltage levels of $v_{ph}(t)$ can be done at the optimal interleaving as V_{dc_act} operates at 60 %. In this case, the THD value decreases to 11.23 %, and each voltage level of $v_{ph}(t)$ is scaled to $V_C/2$ which equals

to 1 kV. For operatting point at the same dc link voltage (i.e. V_{dc_act} = 60 % of V_{dc_nom}), the increase in THD value reaches up to 19.88 % as V_C is achieved regarding the approach of (3.16). Even if $v_{ph}(t)$ is generated at nine levels in which each voltage level is $V_C/2$ of 1.25 kV. Fig 5.5 (e) shows that the case of interleaving is not optimum under this operating condition. As different output voltage levels can be generated under these operating conditions, the behaviour of the harmonic of this output phase voltage $v_{ph}(t)$ will be discussed in more details in terms of harmonic existence\cancellation, and interleaving occurrence. In the next section, resultant harmonic contents of the proposed analytical harmonic solutions (as the analytical model) are verified with those of the simplified switching model under some specified operating points, which illustrated before in Fig 5.5 (a), (c), (d) and (f).

5.4.2 Harmonic identification of switched voltage waveforms on FB-MMC under different dc link voltage levels

The analytical harmonic solution proposed in this chapter is evaluated under different operating conditions, that to identify amplitudes of harmonic contents existed\cancelled in the switched voltage waveforms of the FB-MMC. This harmonic solution considers the amplitudes of harmonic contents for the output voltages of the FB-submodule, arm and phase of the FB-MMC. Hence, this solution can allow a calculation of the THD value of the output phase voltage $v_{ph}(t)$ in which the operation of the FB-MMC covering the full range of dc link voltage. In order to achieve that, expressions of the analytical harmonic solution are implemented and simulated using MATLAB\M-files environment. In order to execute these analytical expressions in the M-files, the simulation parameters are defined by the details of the FB-MMC model listed in Table 3.1. As the switching frequency for the FB-submodule device is set to be 1 kHz. Here, the frequency (carrier) ratio $\{m_f = f_{sw}/f_0\}$ is equal to 20. This ratio with its multiples will represent a presence of the harmonic (carrier) groups in the harmonic spectrum that calculated from the

analytical model. A range of sideband harmonics centred around the carrier is also presented for each harmonic group. Of note that resultant amplitudes of the harmonic contents of each voltage waveform are normalised to $V_{dc\_nom}/2$, as they are shown in the harmonic spectrum form.

5.4.2.1 Harmonic analysis when FB-MMC operating in the buck mode

As the derived expressions for the analytical harmonic solutions are implemented using the simulation in the M-file based model, the analytical model here is executed with the simulated parameters of (V_{dc_act} = 10 kV, V_C = 2.5 kV, M_{dc} and M_{ac} = 1), that to emulate the operation of the FB-MMC at the buck mode. Based on (5.28) or (5.29), amplitudes of the harmonic contents for each FB-submodule output voltage waveform is evaluated under these operating conditions, as shown in Fig 5.6. It can be observed that the harmonic spectrum of each FB submodule output voltage contains only even sideband harmonics around the odd carrier and odd sideband harmonics around the even carrier. For each FB-submodule in the upper arm as an example, $v_{SM\_up}(t)$ comes as the results of $\{v_{SM\_up\_LL}(t) - v_{SM\_up\_RL}(t)\}$; therefore, the first carrier group achieves at $2m_f$ =40 which represents twice switching frequency f_{sw}. For each arm voltage based on (5.30) or (5.31), the harmonic contents only exist in the carrier groups of $\{2Nm_f\}^{th}$ multiples, that because the harmonic cancellation here is based on N (the number of series connected FB-submodules of each arm. For the case of $N = 4$, the harmonic contents of the arm voltage using the analytical model are identified as shown in Fig 5.7. These results are also validated with those of the switching model, as illustrated in Fig 5.9. It can be seen that only odd sidebands are centred around $2Nm_f$, $4Nm_f$, $8Nm_f$ carrier groups. Because the odd sideband harmonics existing in the upper and lower voltages have opposite directions, these harmonics appear without any cancellation in $v_{ph}(t)$ as presented in Fig 5.5 (a). In the buck mode, Fig 5.9 also

shows that these harmonics of $v_{ph}(t)$ defined by (5.32) are centred around sathe me carrier groups as those of the arm voltages.

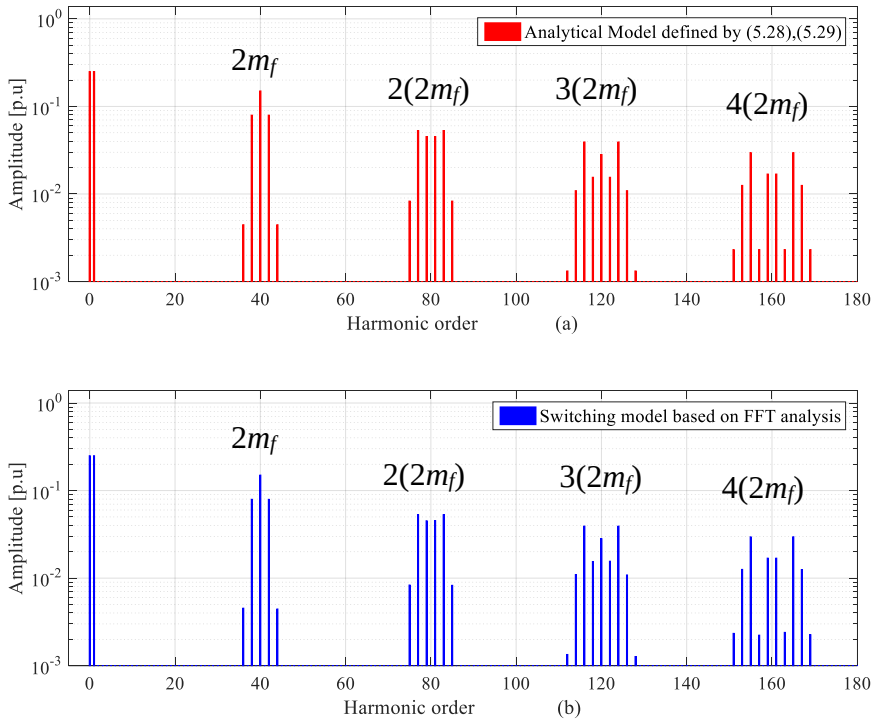


Fig 5.6 Harmonic spectrums for each FB-submodule operates in the buck mode at V_{dc_act}= V_{dc_nom}, M_{dc}= 1, M_{ac}= 1, and V_C defined by (3.16): (a) The analytical model results, (b) FFT of the switching model results

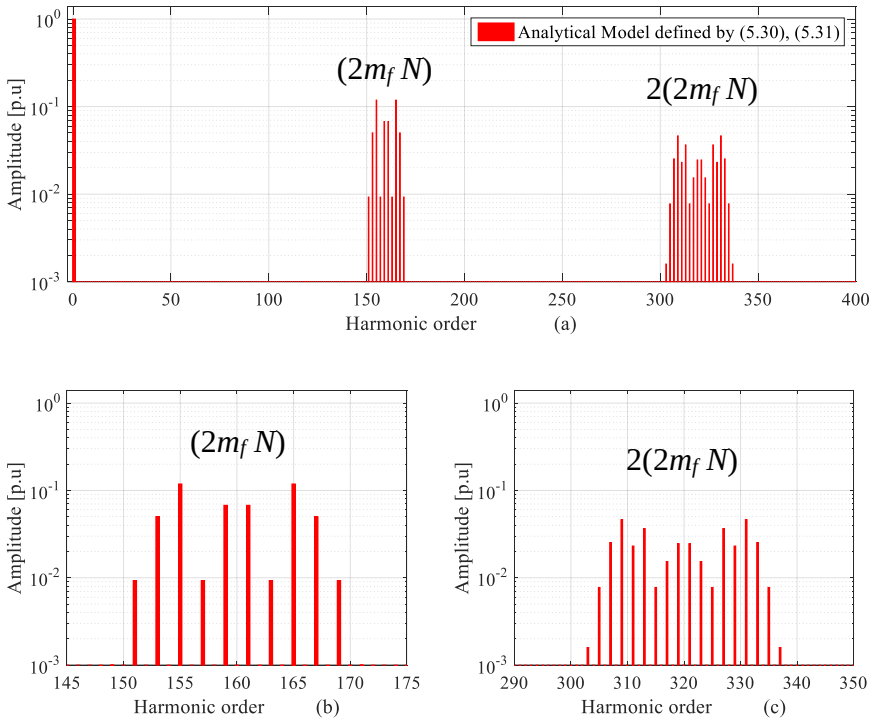


Fig 5.7 Harmonic spectrums of the arm voltage when the FB-MMC operates in the buck mode with V_{dc_act}= V_{dc_nom}, M_{dc} = 1 , M_{ac} = 1 and V_C defined (3.16): (a) The analytical model results, (b) Frequency range of the 1st carrier group of (a), (c) Frequency range of the 2nd carrier group of (a).

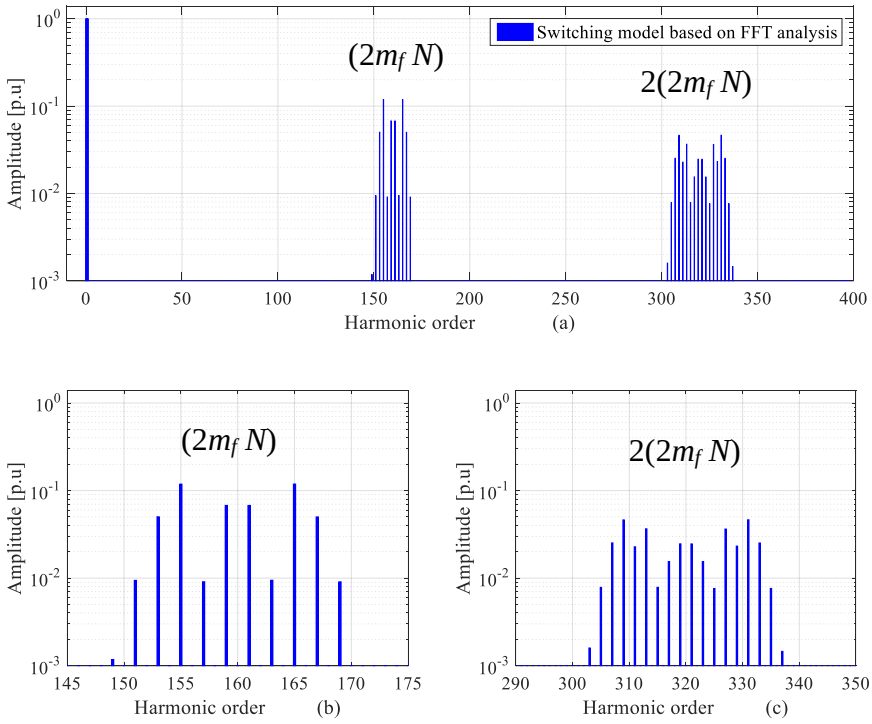


Fig 5.8 Harmonic spectrums of the arm voltage when the FB-MMC operates in the buck mode with V_{dc_act}= V_{dc_nom}, M_{dc} = 1, M_{ac} = 1 and V_C defined by (3.16): (a) FFT of the switching model, (b) Frequency range of the 1st carrier group of (a), (c) Frequency range of the 2nd carrier group of (a).

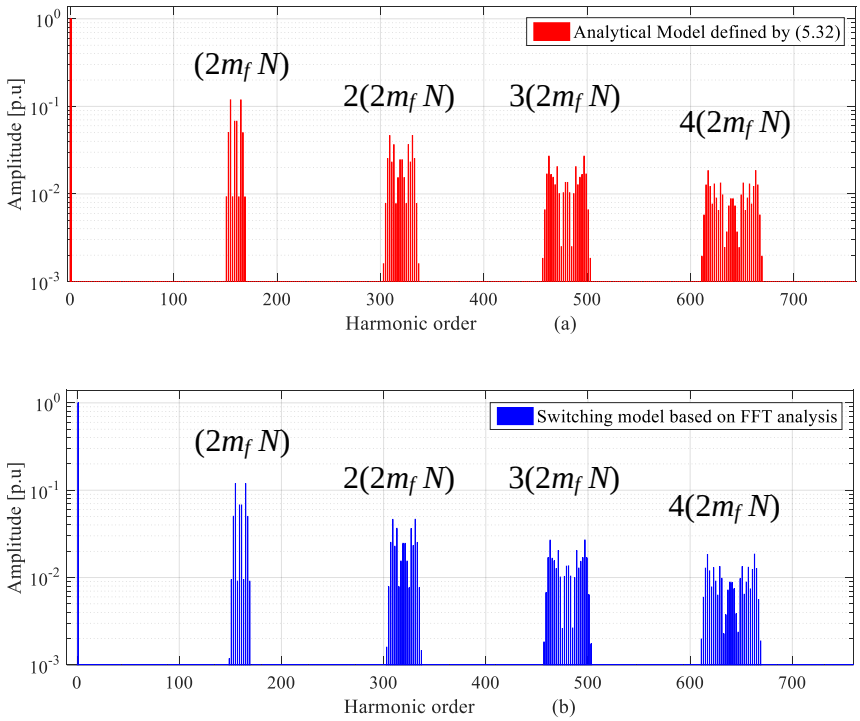


Fig 5.9 Harmonic spectrums for the output voltage of FB-MMC when operates in the buck mode at V_{dc_act}= V_{dc_nom}, M_{dc} = 1, M_{ac} = 1 and V_C defined by (3.16): (a) The analytical model results, (b) FFT of the switching model results

5.4.2.2 Harmonic analysis when the FB-MMC operating in the boost and V_C is regulated at V_{dc_nom}/N

In terms of better THD in the boost mode, the operating point is chosen to analyse harmonic contents of the output voltage $v_{ph}(t)$ for both the analytical and switching models. For the case of V_C determined by (3.16), the simulated parameters of (V_{dc_act} = 7.5 kV, V_C = 2.5 kV, M_{dc} = 0.75 and M_{ac} = 1) are implemented, that to emulate the operation of the FB-MMC at boost mode. Under this operation condition, amplitudes of the harmonic contents for each FB-submodule output voltage waveform is evaluated using (5.28) or (5.29) as shown in Fig 5.10. It can be observed from this the harmonic spectrum that carrier groups of $2(2m_f)$ contains only even sideband harmonics, while other carrier groups consists of the even and odd sideband harmonics. The harmonic contents for the arm voltage are calculated using (5.30) and (5.31) and presented in Fig 5.11, and the obtained results are also verified with those of the switching model as shown in Fig 5.12. It can be noted that sideband harmonics with even order are only centred around the odd carrier groups, while for the even carrier groups, the odd sideband harmonics only exist. As the even sideband harmonics are the same for both voltage arms, which result in their cancellation in the output phase voltage $v_{ph}(t)$. In this case, the harmonic spectrum exists in the carrier group of $2(2m_f)$ as shown in Fig 5.13. Note that the number of the output voltage levels is increased to nine at this operating point, as displayed in Fig 5.5 (c). For the case of the interleaving under these operating conditions is considered as an optimum.

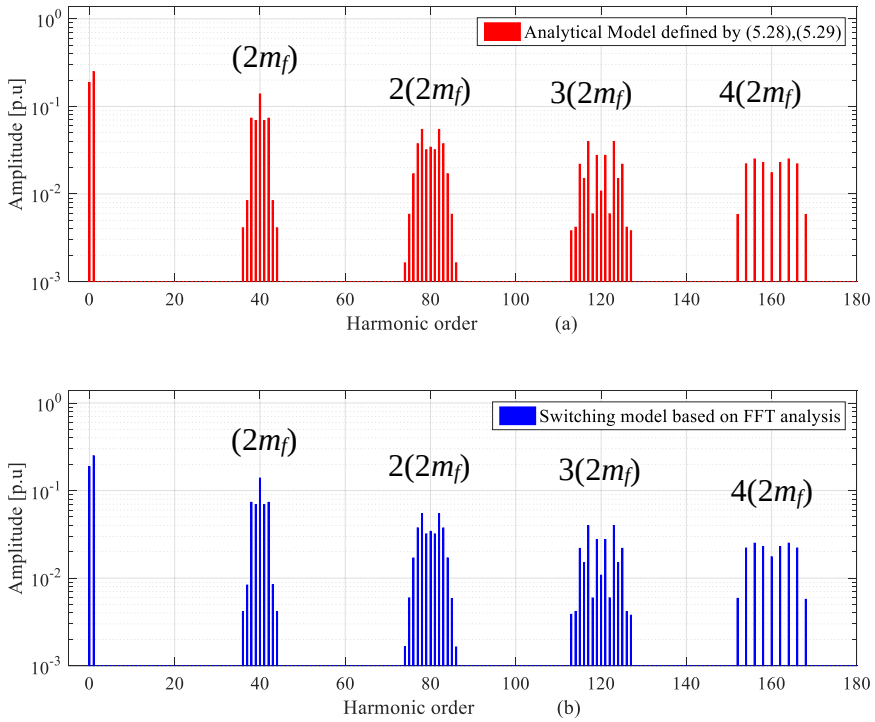


Fig 5.10 Harmonic spectrums for each FB-submodule operates in the boost mode at V_{dc_act}= 75 % of V_{dc_nom}, M_{dc}= 0.75, M_{ac}= 1, and V_C defined by (3.16): (a) The analytical model results, (b) FFT of the switching model results

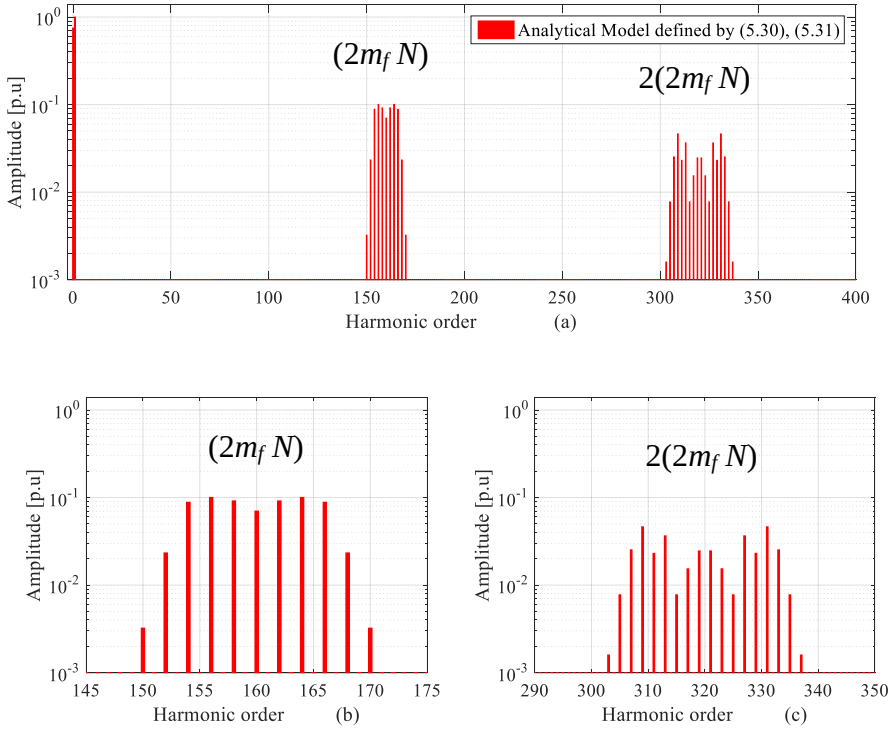


Fig 5.11 Harmonic spectrums of the arm voltage when the FB-MMC operates in the boost mode with V_{dc_act}= 75 % of V_{dc_nom}, M_{dc} = 0.75, M_{ac} = 1 and V_C defined (3.16): (a) The analytical model results, (b) Frequency range of the 1st carrier group of (a), (c) Frequency range of the 2nd carrier group of (a).

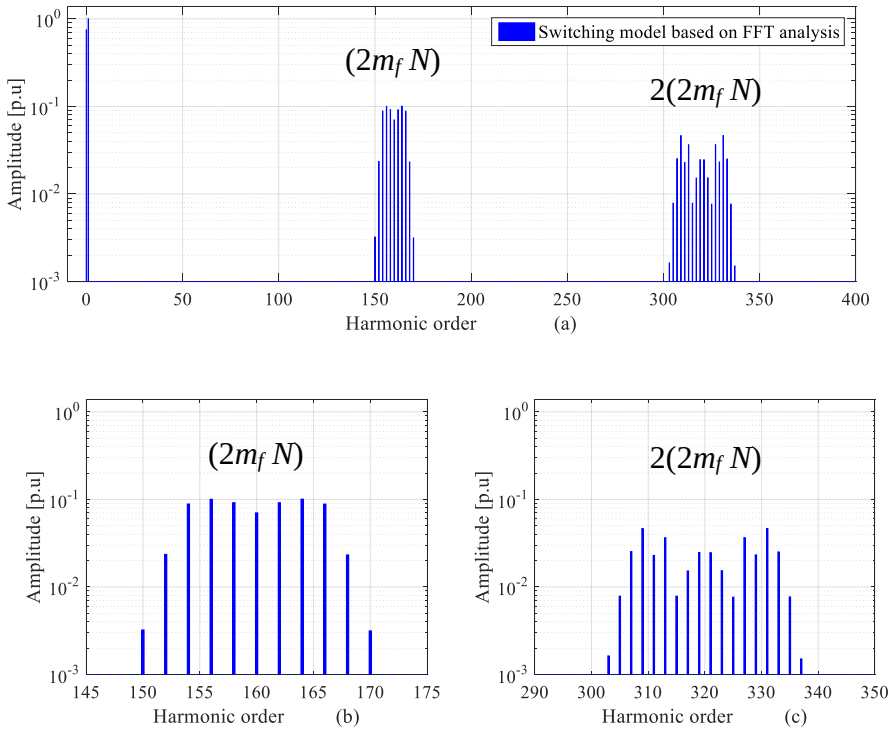


Fig 5.12 Harmonic spectrums of the arm voltage when the FB-MMC operates in the boost mode with V_{dc_act}= 75 % of V_{dc_nom}, M_{dc} = 0.75, M_{ac} = 1 and V_C defined by (3.16): (a) FFT of the switching model, (b) Frequency range of the 1st carrier group of (a), (c) Frequency range of the 2nd carrier group of (a).

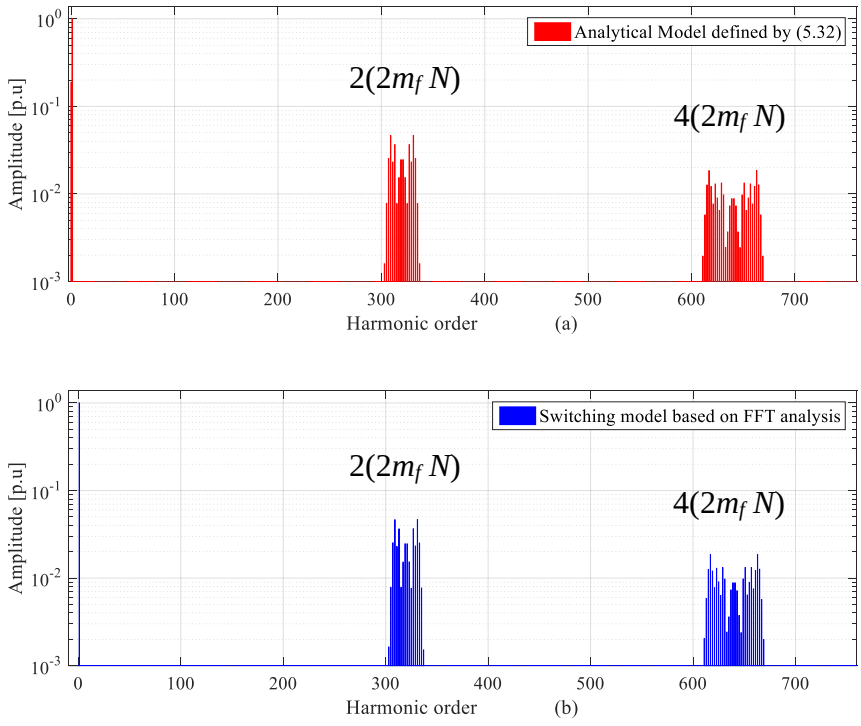


Fig 5.13 Harmonic spectrums for the output voltage of FB-MMC when it operates in the boost mode at V_{dc_act}=75 % of V_{dc_nom}, M_{dc} = 0.75, M_{ac} = 1 and V_C defined by (3.16): (a) The analytical model results, (b) FFT of the switching model results

5.4.2.3 Harmonic analysis when FB-MMC operating in the boost mode and V_C regulated according to the dc link voltage level at $(V_{dc\_nom} + V_{dc\_act})/(2N)$

Based on the same dc link voltage level in the previous section, harmonic contents of the output voltage $v_{ph}(t)$ is also analysed using both of the analytical and switching models. For the case of V_C determined by (3.17), the simulated parameters of (V_{dc_act} = 7.5 kV, V_C = 2.187 kV, M_{dc} = 0.86 and M_{ac} = 1.14) are used for the FB-MMC model at the boost operating mode. In the simulation results, amplitudes of the harmonic contents for each FB-submodule output voltage waveform defined in (5.28) or (5.29) are evaluated, as shown in Fig 5.14. It can be seen that both of even and odd sideband harmonics are centred around all carrier groups of $\{2m_f\}^{th}$ multiples. Therefore, the carrier group of $\{2Nm_f\}^{th}$ multiples of the arm voltage defined by (5.30) or (5.31) contain both even and odd sidebands as illustrated in the harmonic spectrum in Fig 5.15 and Fig 5.16. Accordingly, the harmonic contents of $v_{ph}(t)$ are presented in Fig 5.17. Compared to Fig 5.13, it can be observed that although even sidebands are cancelled in $\{2Nm_f\}^{th}$ multiples, the odd sideband harmonics still exist in the odd carrier groups as they can be generated in odd and even carries of arms voltages, which result in not complete harmonics cancellation of the odd carrier groups in the output phase voltage at this operating conditions. Here, the interleaving is not at the optimum case as illustrated in Fig 5.5 (d), Fig 5.15, Fig 5.16 and Fig 5.17. In this case of the capacitor voltage regulation, however, the optimum interleaving can be achieved as illustrated in Fig 5.5 (f), that when the FB-MMC works at V_{dc_act} = 60% of V_{dc_nom}. The simulated parameters of (V_{dc_act} = 6 kV, V_C = 2 kV, M_{dc} = 0.75 and M_{ac} = 1.25) are implemented into both of the analytical and switching models, that to analyse the harmonic contents for this case. Fig 5.18 shows the amplitudes of the harmonic contents for each FB-submodule output voltage waveform. It can be noted that even or odd sidebands exist in the carrier groups of $\{2Nm_f\}^{th}$ multiples contain even or odd sidebands, while both of even and odd sidebands are centred around other carrier groups. For

the harmonic contents of both models are evaluated in Fig 5.19 and Fig 5.20. It can be seen that even sidebands are centred around odd carriers, while odd sidebands are centred around even carriers. These results in harmonic cancellation of the output voltage $v_{ph}(t)$, that because the even sideband harmonics of each voltage arm have the same direction. In this case, the harmonic spectrum exists in the carrier group of $\{4Nm_f\}^{th}$ multiples as illustrated in Fig 5.21. In this operating point, the number of output voltage levels is increased to eleven. Regardless of the amplitudes of harmonic contents, the behaviour of the harmonic is similar to the case of section 5.4.2.2. It can be concluded from the harmonic spectrum of the FB-submodule output voltage that if the carrier groups of $\{2Nm_f\}^{th}$ multiples contain odd or even sideband harmonics that will lead to the proper interleaving. Otherwise, if both odd and even sidebands existed together in the carrier groups of $\{2Nm_f\}^{th}$ can result in not proper interleaving. For the harmonic cancellation in the output voltage, it can be obtained when only even sideband harmonics are centred around carrier of $\{2Nm_f\}^{th}$ multiples in each FB-submodule output voltage.

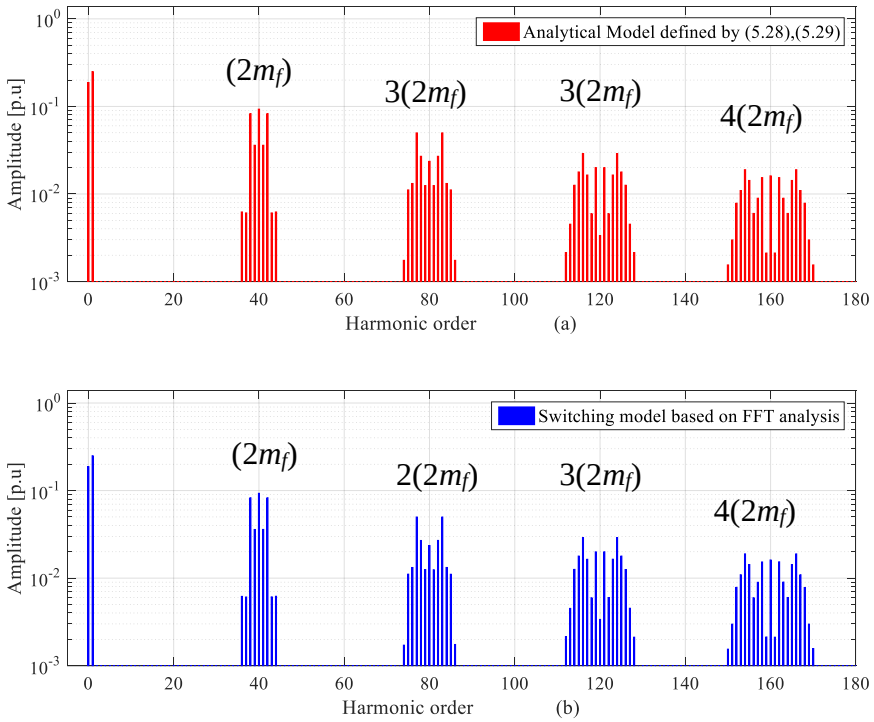


Fig 5.14 Harmonic spectrums for each FB-submodule operates in boost mode at V_{dc_act}= 75 % V_{dc_nom}, M_{dc} = 0.86, M_{ac}= 1.14 and V_C defined by (3.17): (a) The analytical model results, (b) FFT of the switching model results

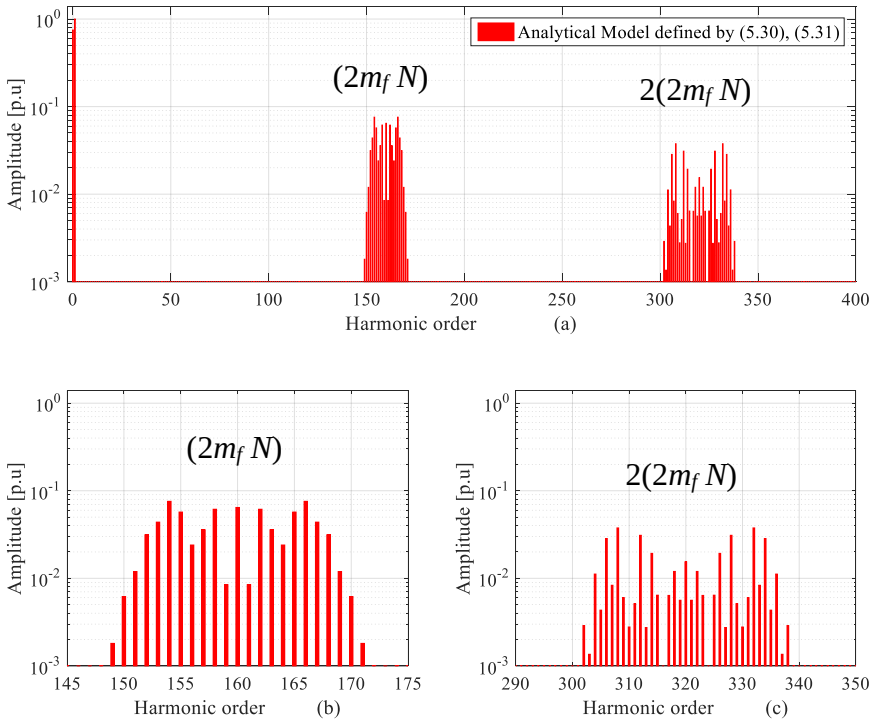


Fig 5.15 Harmonic spectrums for voltage of FB-MMC arm operates in boost mode with V_{dc_act}=75 % of V_{dc_nom}, M_{dc} = 0.86, M_{ac} = 1.14 and V_C defined (3.17): (a) The analytical model results, (b) Frequency range of the 1st carrier group of (a), (c) Frequency range of the 2nd carrier group of (a).

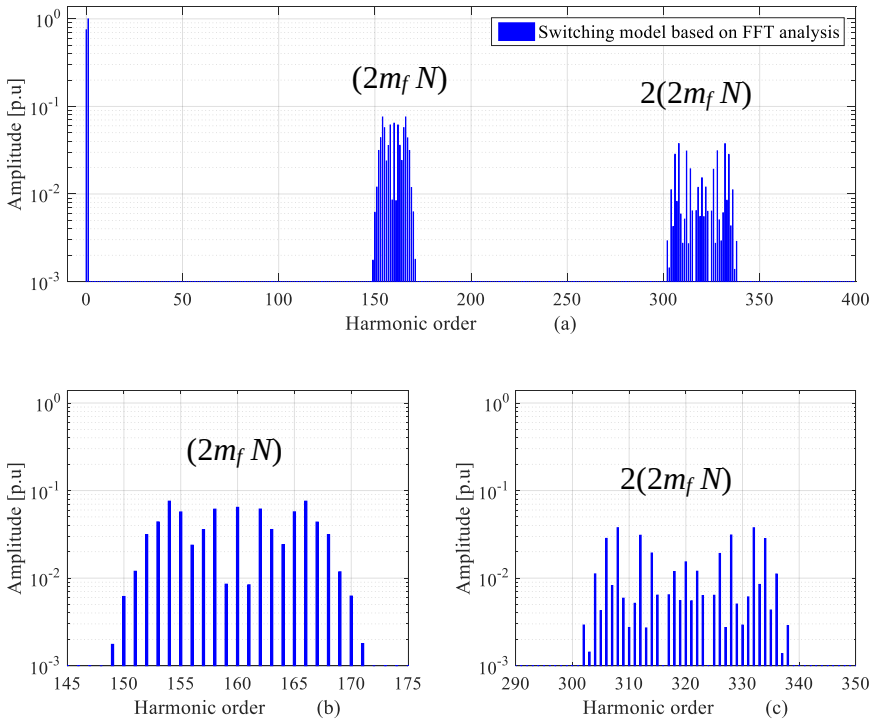


Fig 5.16 Harmonic spectrums for voltage of FB-MMC arm operates in boost mode with V_{dc_act}=75 % of V_{dc_nom}, M_{dc} = 0.86 and M_{ac} = 1.14 and V_C defined by (3.17): (a) FFT of the switching model, (b) Frequency range of the 1st carrier group of (a), (c) Frequency range of the 2nd carrier group of (a).

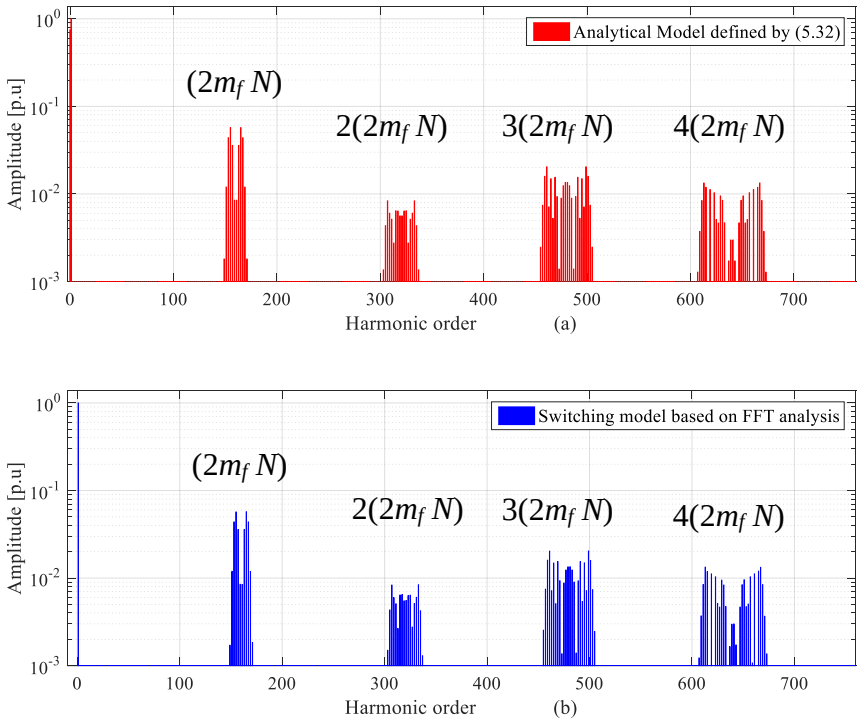


Fig 5.17 Harmonic spectrums for the output voltage of FB-MMC when operates in boost mode at V_{dc_act}= 75 % of V_{dc_nom}, M_{dc} = 0.86 and M_{ac} = 1.14 and V_C defined by (3.17): (a) The analytical model results (b) FFT of the switching model results

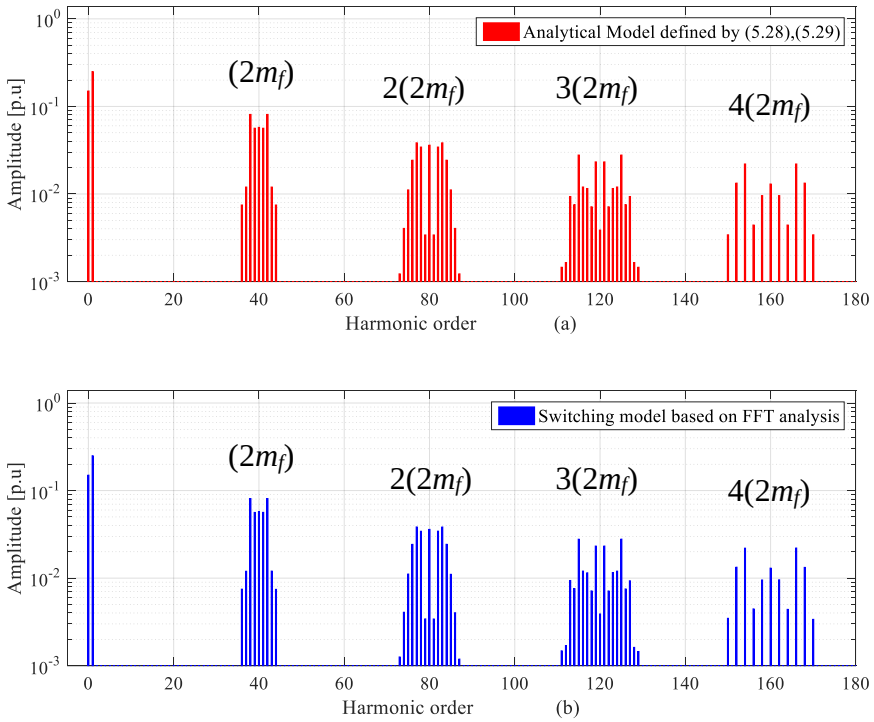


Fig 5.18 Harmonic spectrums for each FB-submodule operates in the boost mode at V_{dc_act}= 60 % V_{dc_nom}, M_{dc} = 0.75, M_{ac}= 1.25 and V_C defined by (3.17): (a) The analytical model results, (b) FFT of the switching model results

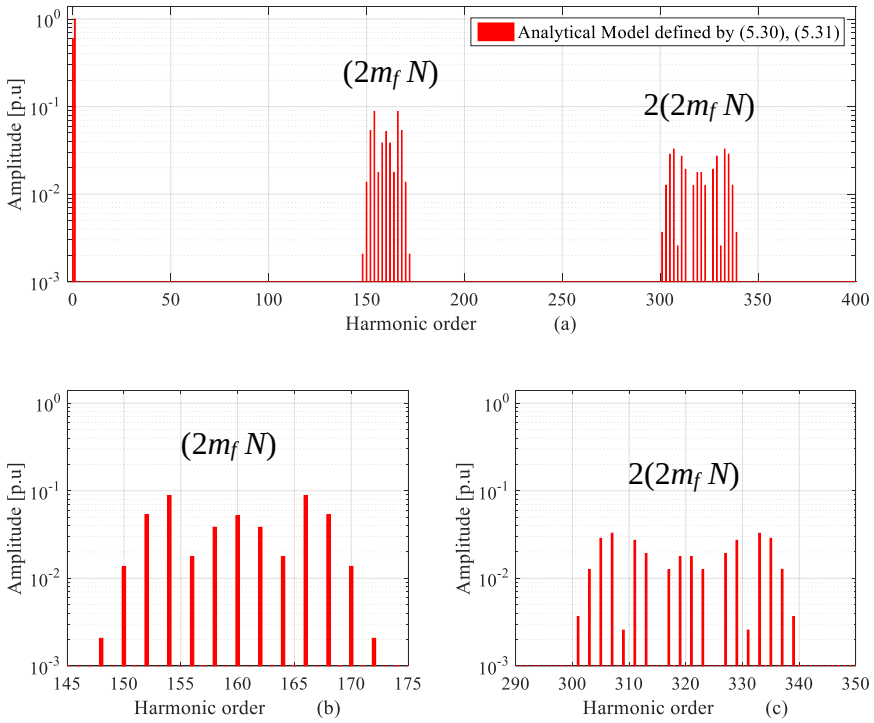


Fig 5.19 Harmonic spectrums of the arm voltage when the FB-MMC operates in the boost mode with V_{dc_act}=60 % of V_{dc_nom}, M_{dc} = 0.75, M_{ac} = 1.25 and V_C defined (3.17): (a) The analytical model results, (b) Frequency range of the 1st carrier group of (a), (c) Frequency range of the 2nd carrier group of (a).

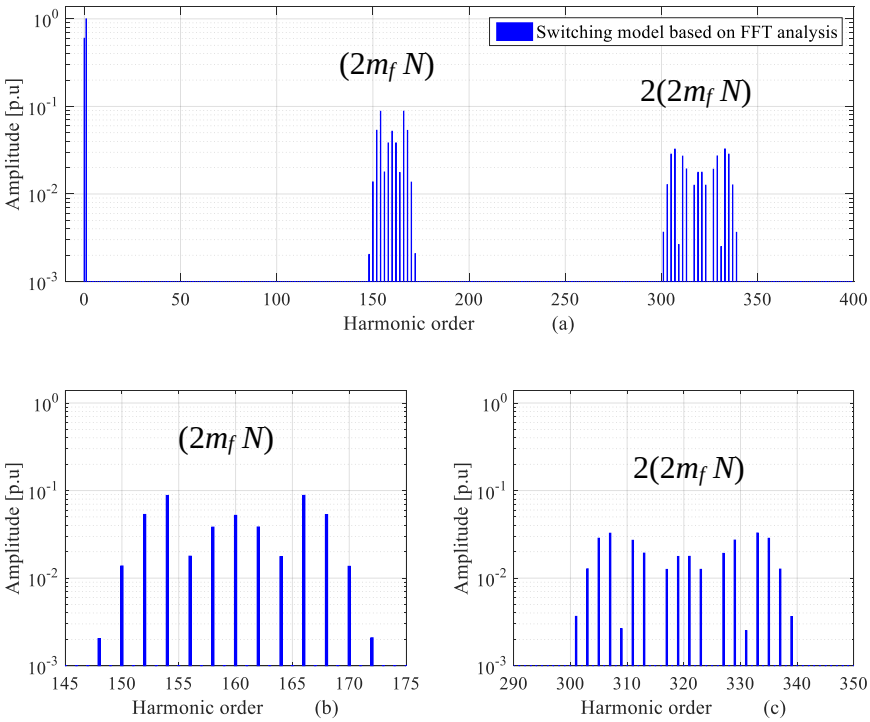


Fig 5.20 Harmonic spectrums of the arm voltage when the FB-MMC operates in the boost mode with V_{dc_act} = 60 % of V_{dc_nom}, M_{dc} = 0.75 and M_{ac} = 1.25 and V_C defined by (3.17): (a) FFT of the switching model, (b) Frequency range of the 1st carrier group of (a), (c) Frequency range of the 2nd carrier group of (a).

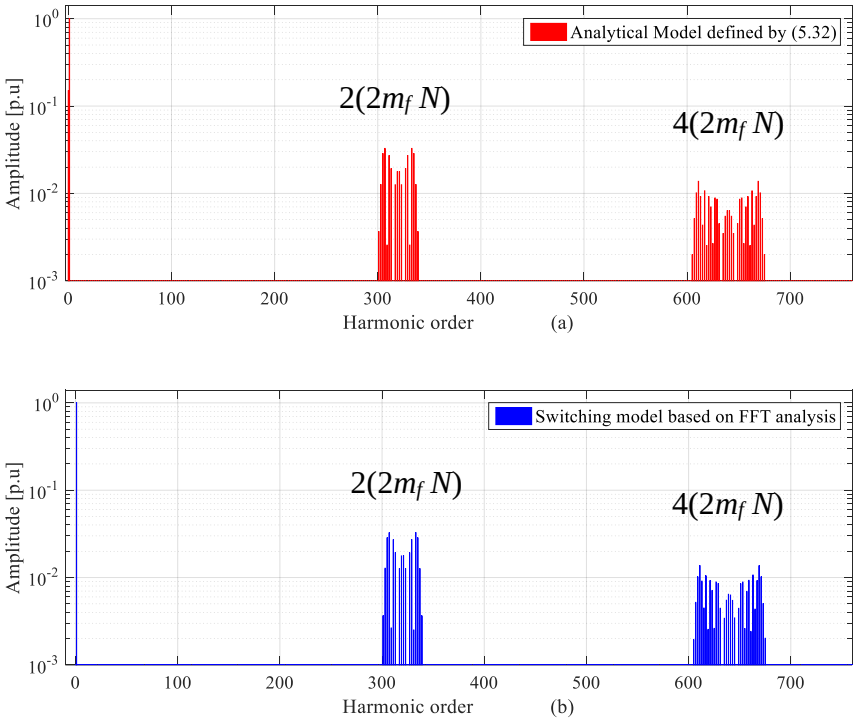


Fig 5.21 Harmonic spectrums for the output voltage of FB-MMC when operates in boost mode at V_{dc_act}= 60 % of V_{dc_nom}, M_{dc} = 0.75 and M_{ac} = 1.25 and V_C defined by (3.17): (a) The analytical model results (b) FFT of the switching model results

5.4.3 Evaluation of THD for the output voltage based on the proposed harmonic solution (analytical model) of FB-MMC

As the accuracy of the proposed analytical harmonic solution is validated, the THD performance for the output voltage is calculated using (5.32) and (3.61). For the case of the variation for the dc link voltage, the calculation of THD values in buck and boost modes is undertaken regarding some operational conditions which are the number of the FB-submodule in each arm (odd and even numbers), the voltage regulation approaches for the FB-submodule capacitor (defined by (3.16) and (3.17)), and the impact of the optimal displacement angle of $(\pi/2N)$. In this section, a different number of the FB-submodules per each arm is studied. which includes: two, three, four and five FB-submodules. Using the analytical harmonic expression defined by (5.32), a maximum of 20 harmonic groups is simulated in the M-file based model to calculate THD of the output phase $v_{ph}(t)$. In the range of the dc link voltage covering [0, V_{dc-nom}], the simulation results expose that different THD values can be achived according to these operation conditions as illustrated in Fig 5.22, Fig 5.23, Fig 5.24 and Fig 5.25. It can be seen from these figures that the number of the FB-submodules, capacitor voltage regulation approaches and employing the displacement angle significantly influence the THD value as compared to the same of the dc link voltage levels. Whereas, it can also be noted that the THD curves are approximately shifted as compared to the zero displacement angle case. In addition, these curves employing the reduced V_C approach move downward according to the reduction in the dc link voltage level. To satisfy the minimum value of THD in a wider dc link voltage range, the displacement angle has to be adjusted regarding these operational conditions. Note that the THD results obtained from both of the analytical and switching models are closely matched, as illustrated in Fig 5.24 and Fig 5.4.

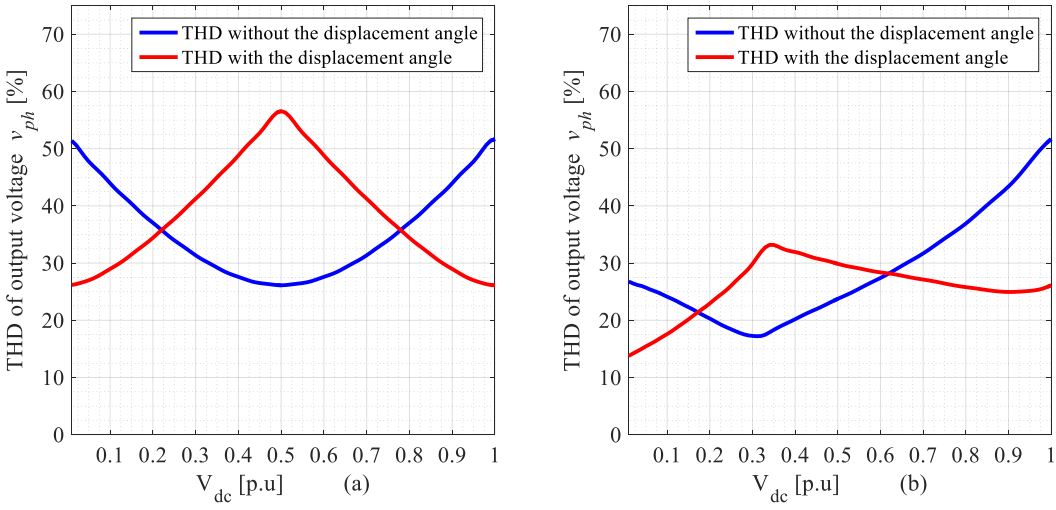


Fig 5.22 Simulation results of the output voltage THD based on the proposed harmonic solution when $N = 2$ and V_C regulation approach: (a) defined by (3.16), (b) defined by (3.17).

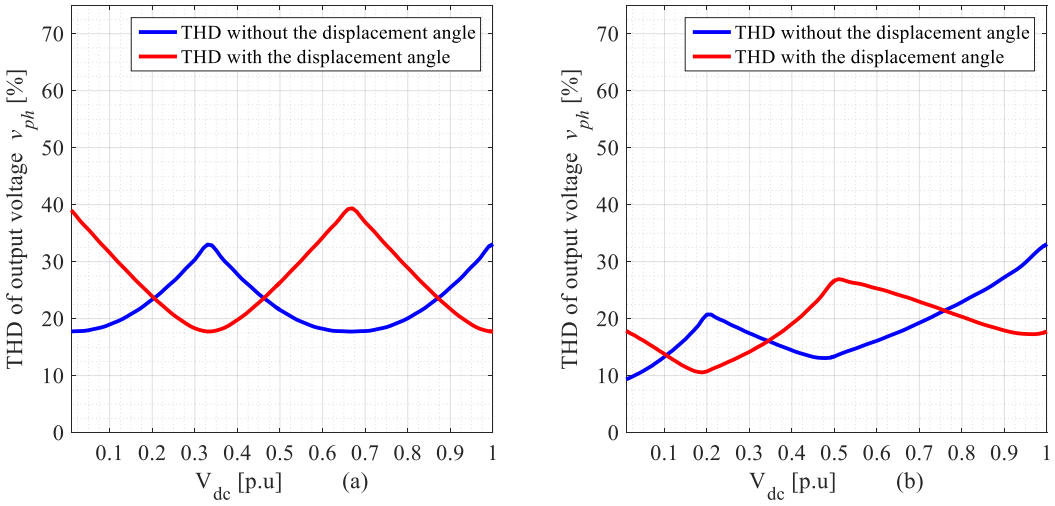


Fig 5.23 Simulation results of the output voltage THD based on the proposed harmonic solution when $N = 3$ and V_C regulation approach: (a) defined by (3.16), (b) defined by (3.17).

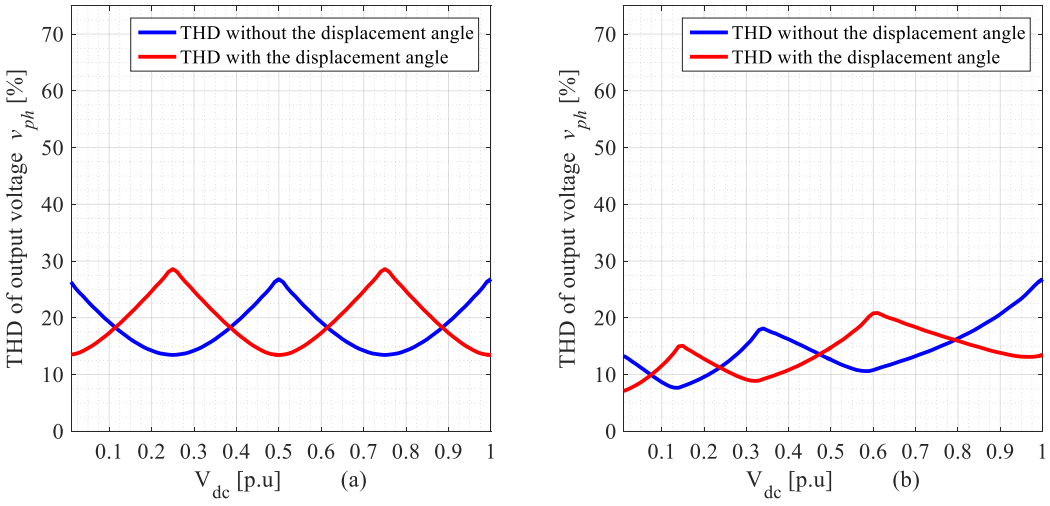


Fig 5.24 Simulation results of the output voltage THD based on the proposed harmonic solution when $N = 4$ and V_C regulation approach: (a) defined by (3.16), (b) defined by (3.17).

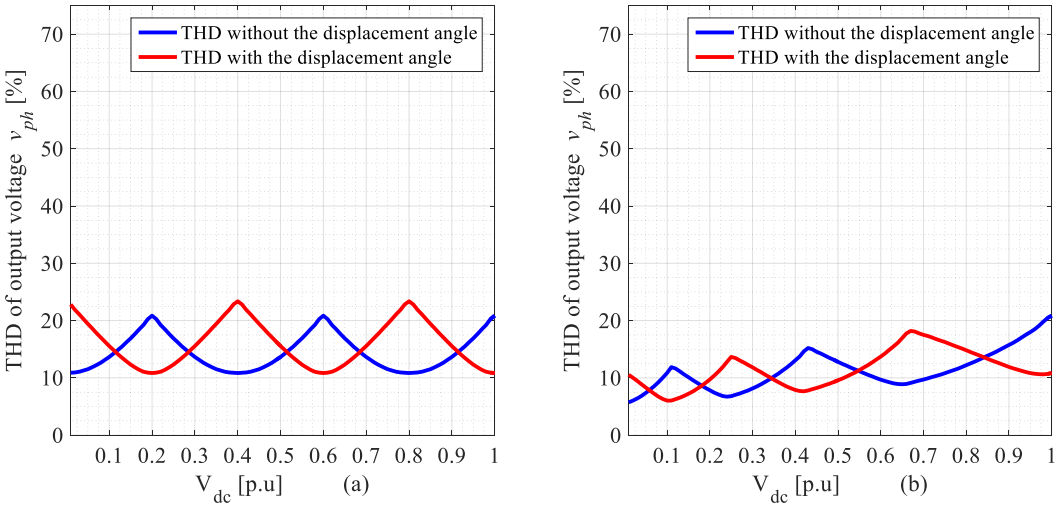


Fig 5.25 Simulation results of the output voltage THD based on the proposed harmonic solution when $N = 5$ and V_C regulation approach: (a) defined by (3.16), (b) defined by (3.17).

By considering the analysis undertaken in this chapter, a comparison to evaluate the performance of the FB-MMC over the HB-MMC is given in terms of switching losses and filter size demands. In the FB-MMC, the number of IGBT switching devices is double if compared to the HB-MMC. Assuming that the same device switching frequency is used in both the HB-MMC and FB-MMC, consequently, the switching losses of the FB-MMC is totally twice that of the HB-MMC [89]. However, these additional IGBT devices can be utilised by taking into consideration the fact that the FB-MMC can operate at different levels of the dc link voltage. While HB-MMC can only operate when the dc link voltage level is fixed at the nominal value V_{dc_nom}, as the dc link voltage here has to be two times the peak grid voltage as $V_{dc\_nom} = 2\hat{v_{ph}}$.

Whether the HB-MMC or FB-MMC, they are connected to the grid through an ac filter such as LCL filter. The ac filter size can significantly be reduced through an increase in the effective switching frequency, whereas the first carrier group of the high order harmonics in the output voltage is relevant to the effective switching frequency value. For the grid connected FB-MMC, the first carrier group is eliminated while operating in the boost mode at the optimal points of the dc link voltage. Thus the effective switching frequency is increased to two times without affecting more switching losses, as the device switching frequency remains at the same value. To reduce the ac filter size, these optimal operating points in the boost mode may be taken into account for the ac filter design consideration.

5.5 Chapter summary

In this chapter, comprehensive analytical modelling was established to identify the harmonic contents of PWM voltage waveforms on the FB-MMC. This analysis undertaken was based on a double Fourier series expansion in two variables that considers developed PSC-PWM scheme. In this work, the double edge naturally sampled PWM has been used. The analytical expressions to identify harmonic

contents were derived for the submodule leg voltages, FB submodule output voltage, arm voltages and output phase voltage. The analytical results revealed an influence of the dc and ac modulation indexes, dc voltage capacitor regulation approaches and employing displacement angle on the amplitude and order of harmonic contents. They also showed that THD behaviour of the output voltage was exposed to nonlinearity regarding different operating points of the dc link voltage in the buck and boost mode. The analytical results were verified by a comparison with FFT analysis of those resulting from the simplified switching model of the FB-MMC.

Chapter 6: Real-Time Digital Simulation and Experimental Implementation of the FB-MMC Operating in the Buck and Boost Modes

6.1 Introduction

This chapter presents the real-time simulation of the single-phase FB-MMC inverter. This work is brought to verify the operation of the FB-MMC in the buck and boost modes under different levels of the dc-link voltage. The FB-MMC and control scheme circuits are simulated using CPU and FPGA cores of the OPAL-RT OP4500. The simulated models are built-in MATLAB/Simulink interfacing the RT-LAB software. Building models consider a methodology technique of the eHS solver. In this case, the CPU model is created to generate PWM gating signals for switching devices using the developed PSC-PWM strategy proposed in Chapter 3. However, a virtual FB-MMC circuit is built and executed in real-time using FPGA model. In this work, the validity of FB-MMC under these operating conditions is also confirmed using experimentation. Here, a down-scaled prototype is configured as the single-phase FB-MMC inverter. The OP4500 simulator in the open-loop testing is used to generate PWM gating signals, which are used to modulate IGBT switching devices. The same the CPU model used in the real-time simulation is exploited in the experimental FB-MMC. Based on the steady-state analysis, the validation for the main findings of the FB-MMC is firstly shown and compared by using both the real-time simulation and experimentation results. In addition, the analytical model of the harmonic contents of PWM waveform voltages, which presented in Chapter 5, is verified using the experimental results of the FB-MMC prototype. Experimentally, the obtained results showed that some differences are mainly caused by the non-ideal switching function of IGBT devices, voltage drop and magnetic characteristic of the arm inductors, the capacitor voltage regulation of the FB-SMs is not implemented.

6.2 Real-Time Simulation

Real-time simulation is considered as an important technology. That can be used to validate the performance of electrical power systems. There are many advantages of implementation in the real-time simulation. This technology can be used to improve and test control strategies in various applications such as power converters, motor drives etc. The real-time simulation can perform a speed which is the same as that of a physical plant model [117]. It can efficiently conduct more test in the lab with lower cost, as this technology is mainly based on the computer simulation. Typically, a control application of the real-time simulators can be classified into three different techniques as [118], [119]:

- Rapid Control Prototyping (RCP)
- Hardware in the Loop (HIL)
- Software in the Loop SIL

In the RCP application, a controller model is built using the real-time simulator and then interfaced to the physical plant model via I/O analogue and digital boards of the simulator. However, the HIL simulation is used to test a physical controller by connecting to the real-time simulator via I/O analogue and digital boards. The real-time simulator executes a virtual plant model instead of implementing the physical plant model. In the SIL application, both controller and virtual plant models are both built and simulated using the same real-time simulator. Many advantages are brought using the SIL if compared to the RCP and HIL. Here the simulated models are less cost and better stable than real models. Besides, physical input and output feedbacks would be not required to interface the controller model with the plant model. The SIL can allow easily to repeat the results under different test conditions. The SIL is also called Fully Digital Simulation [118].

6.3 Opal-RT Simulator

An Opal-RT simulator is a computer device with higher performance, that can be used to simulate electrical power systems in real-time [120]. Any simulated models for these power systems are required to be designed using an RT-LAB environment. In this study, a complete real-time simulation working is executed on an Opal-RT OP4500 simulator that implementing RT-LAB software v11.0.8.13. Each product of the Opal-RT digital simulator is composed of two main parts: the first part contains CPU (multi-core processor computer), and the second part consists of the analogue and digital I/O signal modules via FPGA board. For a case of the Opal -RT OP4500 simulator, the CPU has four Intel Xeon 3.3 GHz processing cores with operating system Linux Redhat. The CPU can send and receive digital and analogue signals based on KINTEX 7 XILINX FPGA I/O board. Each OP4500 simulator can be configured up to 96 fast I/O channels with signal conditioning [117], [120]. Fig 6.1 displays chassis front and rear views of the Opal RT OP4500 simulator which implemented into this investigation.

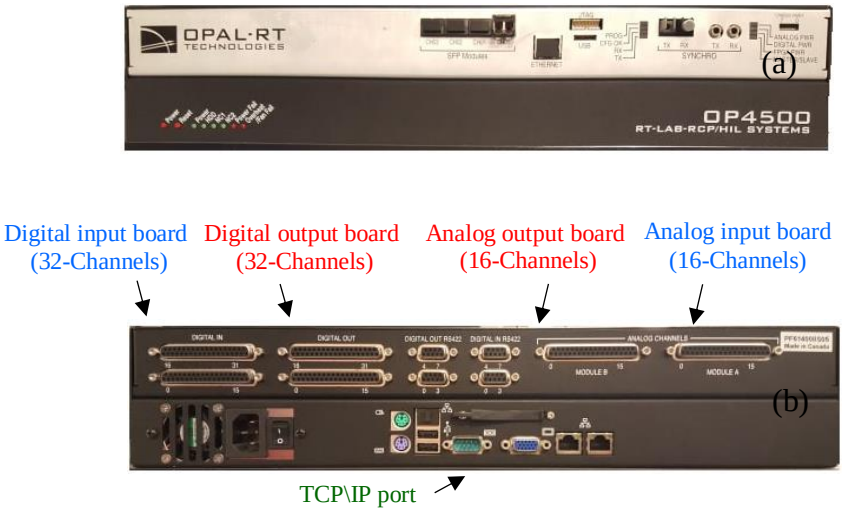


Fig 6.1 Opal-RT OP4500 simulator: (a) Chassis front view, (b) Chassis rear view

6.4 RT-LAB Model

An RT-LAB software is interfaced with the MATLAB/Simulink environment, that allows creating system models using on SimPowerSystem Blockset. The RT-LAB software is used to connect a host PC with a target machine (Opal-RT simulator). Whereas, the host PC works as a command station for users. The RT-LAB software calls to edit and modify the simulated model, and to convert this model to C code, and then to compile and load C code into the target machine [120], [121], [122]. In this study, the converted model to C code is downloaded to a specified target machine via an Ethernet cable connection which defining a certain IP address. The real-time system configuration is illustrated in Fig 6.2

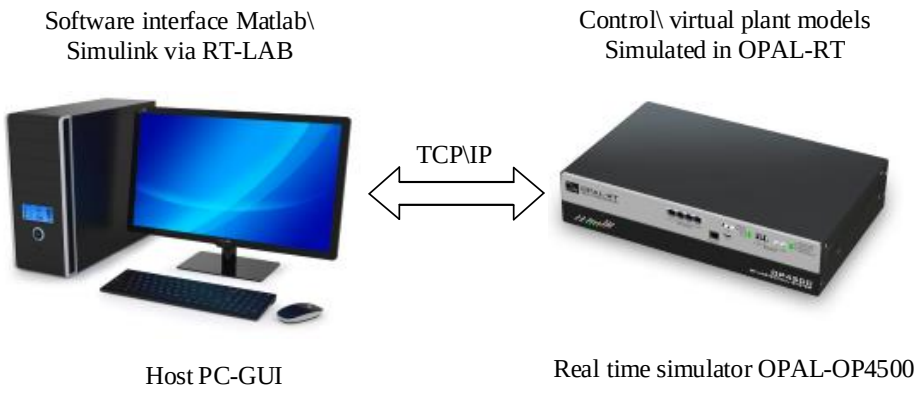


Fig 6.2 Diagram of the real-time simulator OP4500 interfaced host PC

To build any circuit model which based on the RT-LAB environment, two or more subsystems are required to be in the MATLAB/Simulink. That can allow executing the circuit model on the OPAL-RT simulator in real-time. These subsystems are classified to console subsystem SC, master subsystem SM and additional slave subsystems SS [117], [122], [123]. The console subsystem is used as a graphical user interface GUI, which allows variables and commands to be changed during the RT simulation. For displaying status data and measurements of the simulated model, the console subsystem can also contain some Simulink blocks

such as switches and scopes. Both SM and SS subsystems in the RT simulation are used for computation. They consist mainly of mathematical models, control systems and the I/O board blocks. Besides, computation subsystems do not require any change during the RT simulation. Each computation subsystem is executed on one target of the CPU core. Any simulated model only needs one SM subsystem.

6.5 Electric Hardware Solver eHS

An Electric Hardware Solver eHS is developed in the OPAL real-time simulation system [121]. This method allows users to facilitate the real-time simulation of electric circuit models based on FPGA core, and to perform it with a sampling time of sub-microsecond [124],[125]. The eHS solver is a powerful floating-point solver which uses a modified nodal analysis of Pejovic's method [121]. It can solve a conductance matrix to find the current in each branch and the voltage at each node of the electrical circuit model. Using MATLAB/Simulink through RT-LAB, difficulties associated with building electric circuit models based on FPGA can be avoided [125]. As these circuit models can automatically be generated in the eHS solver without using HDL code of FPGA devices. In this case, the real-time simulation based on FPGA can only support specific power electrical element models in MATLAB/Simulink libraries. While most blocks in these libraries are supported to be executed on the CPU core [121].

6.6 Modelling of the FB-MMC based on the eHS Solver

The real-time simulation, which based on the methodology technique of the eHS solver, is utilised in some power converter application. In [124], it is used for the simulation of the MMC connected to the HVDC grid. For a photovoltaic grid connected three-phase inverter, it is used as the HIL simulation based on eHS as presented in [126]. Moreover, this simulation method is validated in [125] for some power converter circuits such as three-phase matrix converter, NPC converter and

DC to DC boost converter. All these power converter circuits are simulated using OPAL-RT OP7000 with multi FPGA platform. In this work, a virtual FB-MMC model is built and executed in the real-time using the OPAL-RT OP4500 simulator. Based on the eHS solver, the FB-MMC model is designed with MATLAB/Simulink interfacing the RT-LAB software. In this case, an implementation of CPU and FPGA models are required to simulate the FB-MMC model. Here, the simulated models of the FB-MMC are built using blocks from eFPGAsim and SimPowerSystems libraries. Note that the control application for the simulated FB-MMC considers the simulation-in-loop SIL.

6.6.1 The CPU model of the FB-MMC based eHS solver

For a case of the CPU model, it is grouped into only two subsystems: console and master subsystems [121]. In this real-time simulation work, the console subsystem of the CPU model is identified by SC_Console, while the master subsystem is donated by SM_PSCPWM_eHS_IOs, as shown in Fig 6.3.

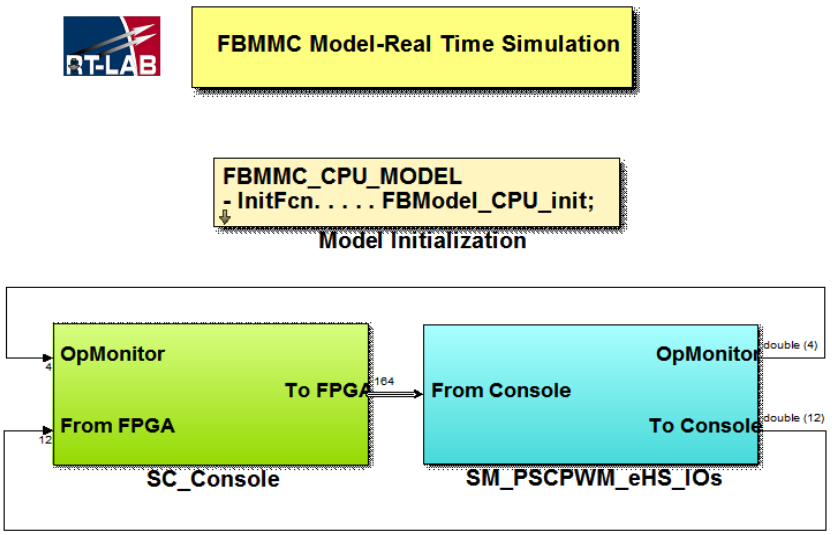


Fig 6.3 Main CPU model of the FB-MMC using SIL

Fig 6.4 shows the console subsystem that is executed on the host PC to monitor the FB-MMC model during the real-time simulation. As the console subsystem is created to be a user interface, it allows specifying operating of the FB-MMC model in the buck and boost modes. These modes are achieved by adjusting both the dc and ac modulation indexes. In the console subsystem, eHS solver outputs are mapped to hardware analogue outputs. Whereas their gain, offset, and range can also be selected for each analogue output channel [121].

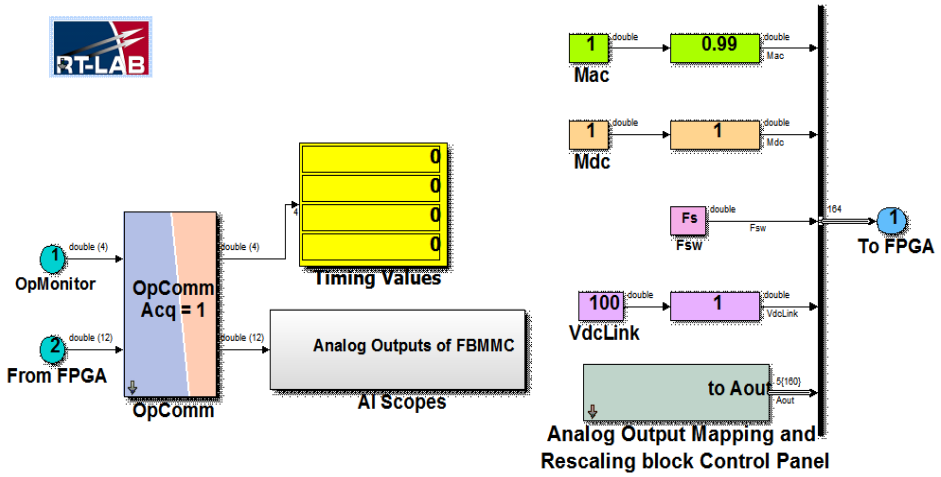


Fig 6.4 Console subsystem in the CPU model of the FB-MMC

In this case, the eHS solver outputs represent voltage\current measurement blocks, which placed inside the FPGA model of the FB-MMC. The scopes in the console subsystem can also be used to display the voltage\current measurements, while the model of FB-MMC is executed in the real-time simulation. However, a set of specific blocks is placed inside the master subsystem. As shown in Fig 6.5, this subsystem is implemented to configure the eHS solver and run the FB-MMC model on the FPGA core.

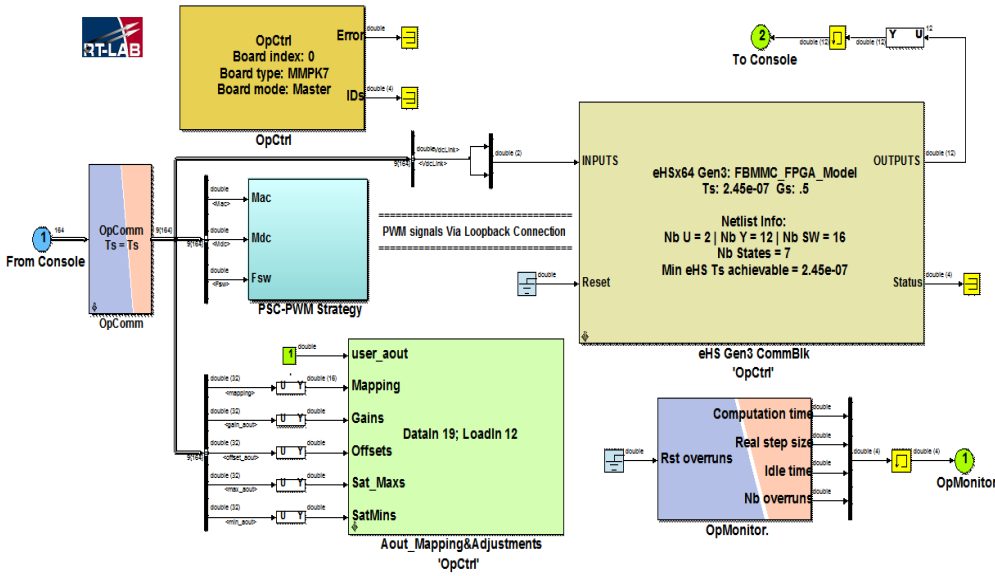


Fig 6.5 Master subsystem in the CPU model of the FB-MMC

The main block in the SM subsystem of the CPU model is “eHS Gen3 CommBlk” [121]. This block is used to interface between the CPU and FPGA models. Therefore, it gives an ability to communicate with the FPGA board and to initialise the eHS core and run at a higher sampling rate. In this simulated model, this block provides eHS input, which used to set a value of the actual dc link voltage v_{dc_act} of the FB-MMC. While, this block also reads the eHS outputs, which represent voltage and current measurement blocks that placed inside the FPGA model. The voltage and current signals can be displayed via the console system. These signals are physically sent to the analogue output board using “Aout_Mapping and Adjustments” block [121]. Therefore, the “Aout_Mapping and Adjustments block in the master subsystem has to be connected to “Analog Output Mapping and Rescaling” block in the console subsystem. To achieve communication between the console and master subsystems blocks, “OpComm” blocks are inserted in these subsystems to receive singles from each other [121],[123]. All input scalar or vector signals of both subsystems must go through the OpComm block before being connected. In order to flash up the FPGA board, an OpCtrl block is placed inside the master subsystem of the CPU model [121],[123]. The OpCtrl block is used to control

and initialise the settings of the FPGA card in the OP4500 simulator. In this case, bitstream files are set in the OpCtrl block. Thus the I\O configuration is programmed on the FPGA board before the CPU model is loaded. For monitoring overruns, an OpMonitor block can also be added to the master subsystem [121]. This block is used to retrieve timing information about the CPU model. Where outputs of this block can give various timing information, which includes computation time, real step size, idle time and a number of overruns [119]. The PWM out block is utilized to produce PWM signals on the digital output channels of an OP525x carrier which linked to FPGA card [121]. A maximum of an 8 channel digital output subsection is implemented in each PWM out block as Pulse Width modulated signal. To generated PWM signal, two parameters are needed to be set as inputs for the PWM out block: duty cycle and carrier frequency. For each channel of the digital output subsection, the duty cycle falls into the range of [0,1]. While a value of the carrier frequency is provided in Hz. In this work, the FB-MMC is built in the FPGA model with two FB-submodule per arm. Here, two of the PWM out blocks are implemented as the total switching devices of 16 is required. Each PWM out block produces four PWM signals and four complementary PWM signals. Thus, a dead time (rise time delay) to the complementary PWM signals are introduced in 1µ sec inside both the PWM out blocks. In the experimental implementation, the dead time value is beneficial to prevent the dc link voltage shoot through.The developed PSC-PWM strategy proposed in 3.3.2 is utilized in the CPU model to generate PWM signals for the FB-MMC, as illustrated in Fig 6.6. In terms of the buck and boost operating modes, a value of the duty cycle of each FB leg is based on the ac and dc modulation indexes. Regarding the actual dc link voltage and the capacitor voltage regulation, the M_{ac} + M_{dc} together should not exceed a maximum of two in which the modulation scheme of the FB-MMC is always performed in a linear mode. Otherwise, the duty cycle becomes saturated when the M_{ac} + M_{dc} is out of the range. The PWM generation mode inside the PWM out block is selected as asymmetric, that to set carrier as the triangular waveform. Initial phase shift between each triangular carrier is also set

inside this block. All these values are sent from the CPU model in the RT-LAB software to FPGA bitstream through PCI bus of the target machine.

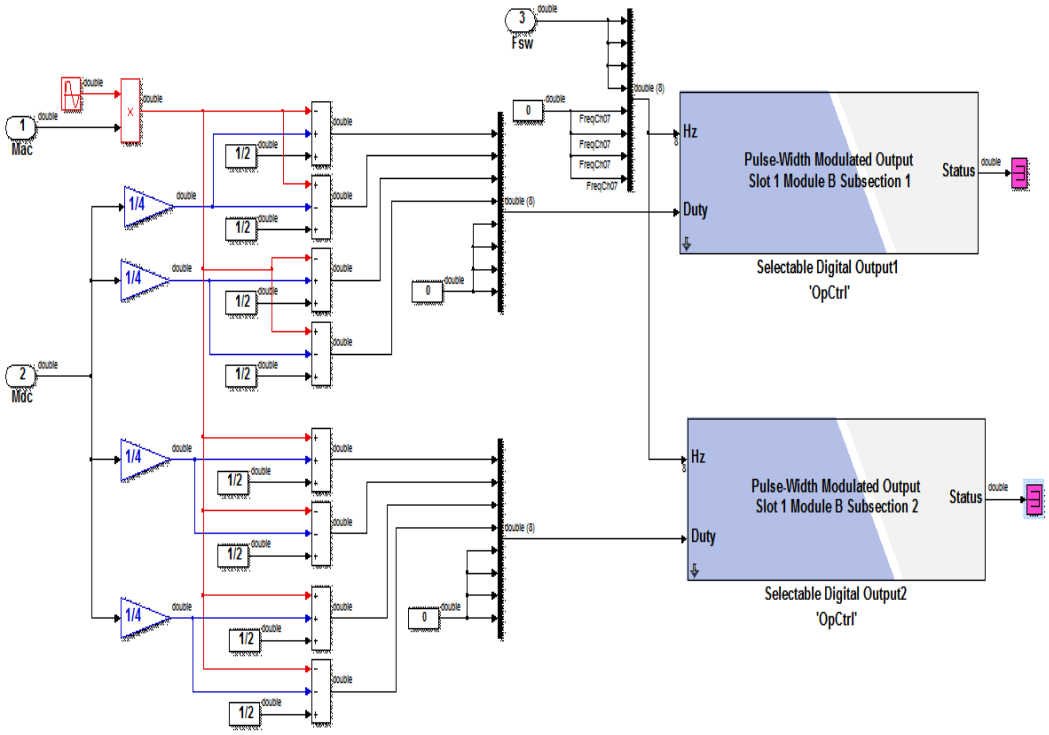


Fig 6.6 Generating PWM signals based on the developed PSC-PWM strategy using the CPU model

6.6.2 The FPGA model of the FB-MMC based on eHS solver

To build the circuit of the FB-MMC model, which using MATLAB\Simulink via RT-LAB software, a specific rule of design has to be taken to implement into the FPGA. Where this rule allows to run the FB-MMC on the FPGA board utilising the eHS solver. Thus a computation of voltages and currents for the FB-MMC circuit are achieved in the real-time simulation. For this case, blocks of switching devices, voltage sources and voltage and current measurement blocks are named with a specific prefix followed by a two-digit index card [121]. Fig 6.7 illustrates an implementation of the FPGA model for the FB-MMC based on eHS solver. As the FB-MMC circuit based on the single-phase system is configured with two FB-submodule per arm, the switching devices in the upper arm are named starting from

SW01 to SW08. While those of the lower arm are set from SW09 to SW16. The dc link voltage sources are named as U01 and U02. Note that the value of each voltage source is equal to $V_{dc\_act}/2$. For measurement blocks, the name of the FB-submodule capacitor voltage measurements is set be Y01 to Y04. The Y05 and Y06 are named for the output voltage of the FB-submodule in the upper and lower arm, respectively. The upper and lower current measurements are identified by Y07 and Y08. Besides, a naming of the output phase current and voltage are Y09 and Y10, respectively. Specific blocks from SimPowerSystem library are only used to configure the FB-MMC circuit. Note that powergui block is added to the FPGA model. The M-files is created to initialise the FPGA and CPU model parameters. In order to execute the real-time simulation properly, the sample time of one microsecond here is selected for FPGA model. While the CPU model is 50 µ sec.

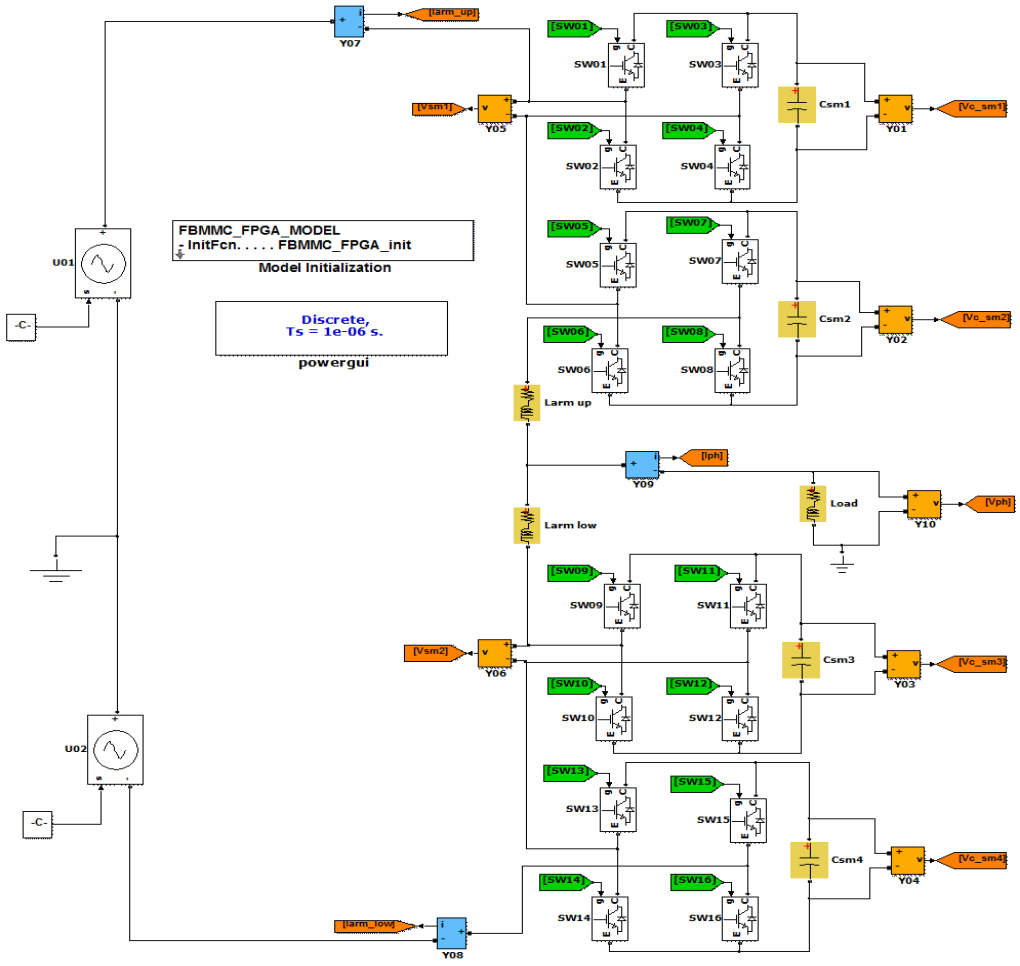


Fig 6.7 Implementation of the FPGA model for the single-phase FB-MMC using SIL

In the FPGA model of this work, the PWM gating signals for the switching devices for the FB-MMC circuit are physically received from the digital input board. This is achieved using a Loopback adapter. This adapter is employed for connecting the digital output board to digital input board. Thus, PWM signals generated in the FPGA card are acquired by the FPGA model in the same RT simulator. In this case, loopback adapter along with a 40-pin flat ribbon cable is used to connect input and output channels between two DB-37 connectors [120]. These connectors are located on the rear of the OP4500 simulator, as shown in Fig 6.8.

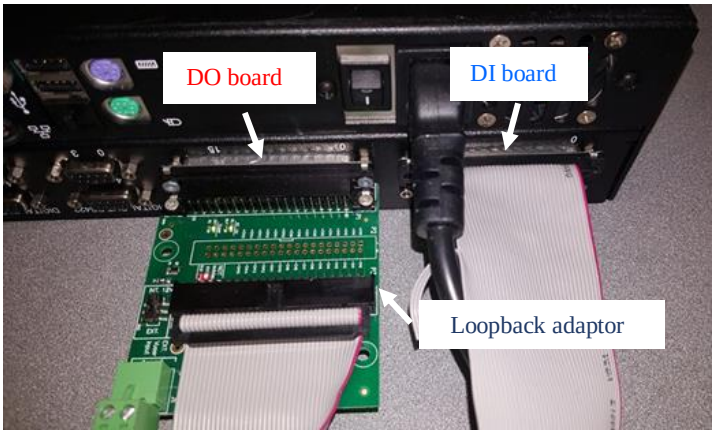


Fig 6.8 Loopback adapter in connecting the digital output board to digital input board

6.7 Experimental FB-MMC Prototype

In this work, a down-scaled prototype for the single-phase FB-MMC is configured, that to verify experimentally the operation principle of the grid connected FB-MMC in the buck and boost modes. Under these operating conditions, this experimental prototype is provided to support the main findings of the steady-state analysis of the FB-MMC. Moreover, it is set to validate the analytical model of the harmonic contents existed in the PWM voltage waveforms of the FB-MMC. Of note that the main circuit parameters of the FB-MMC implemented for both the prototype hardware and the real-time simulation model are listed in Table 6.1.

Table 6.1: List of main parameters used in the prototype hardware and real simulation of the FB-MMC based on the single-phase system

Parameter	Value [Unit]
Nominal active power	70 [W]
Nominal phase voltage V_{ph} r.m.s	35 [V]
Nominal phase current I_{ph} r.m.s	2 [A]
Nominal frequency f_o	50 [Hz]
Nominal dc link voltage V_{dc_nom}	100 [V]
Submodule capacitance C_{SM}	2.5 m [F]
Upper / lower arm Inductances L_{arm}	2m [H]
Load Resistance R_{load}	17 [Ω]
Load inductance L_{load}	5m [H]
Submodule number per arm N	2
Aluminium electrolyte capacitors	4.7 m [F]
Nominal voltage across submodule capacitor V_C	50 [V]
Switching frequency for FB-submodule leg f_{sw}	2k [Hz]
Sampling frequency (1/sample time)	20k [Hz]

As shown in Fig 6.9, the main components used in this experimental implementations are introduced as follows:

(1) - Host PC as user interface

(2) - OP4500 simulator to generate PWM signals in the open-loop testing

(3) - Digital interface board to connect the OP4500 and FB-MMC prototype

(4) - Fiber Optic cables

(5) - FB-submodules enclosure (The metal box)

(6) - Upper and lower arm inductors

(7) - The Load inductor

(8) - The Load resistor

(9) - Main dc voltage supply which is used for the dc link voltage.

(10) - Two Aluminium electrolyte capacitors that are used to create a neutral point.

(11) And (12) - Two dc voltage supplies are used to serve Digital output interfaced board and FB-submodule main-boards, respectively.

(13) - Digital voltage meters to monitor capacitor voltages of each FB-submodule.

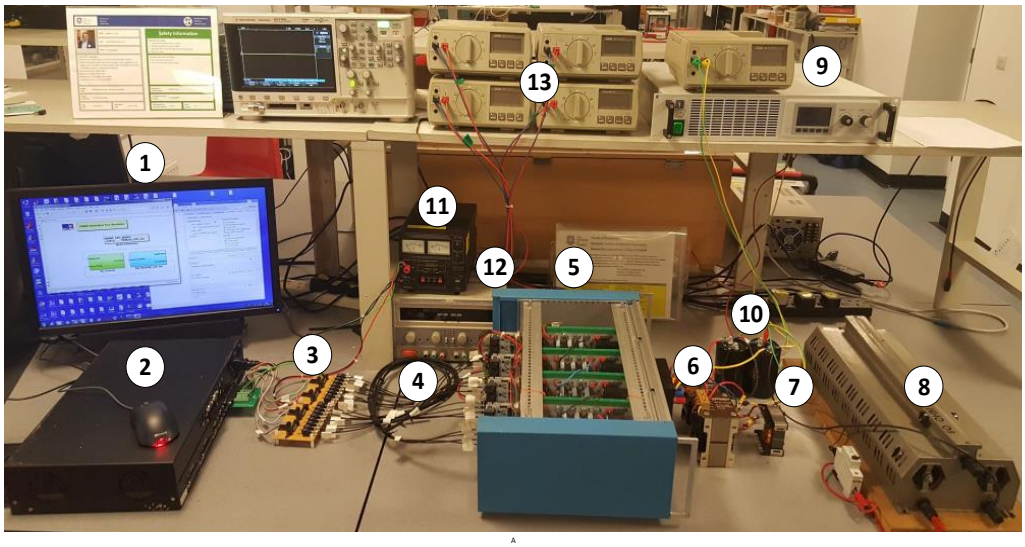


Fig 6.9 Photograph of an experimental implementation for the single-phase FB-MMC connected RL passive load

6.7.1 Control platform using the O4500 simulator

In this work, the O4500 simulator is implemented as a control platform to conduct experiments in the laboratory. PWM signals for IGBT devices of the FB-MMC are experimentally generated using the O4500 simulator, that to verify developed PSC-PWM strategy proposed in chapter 3. In the open-loop testing, a control scheme is required to operate a physical FB-MMC prototype. To achieve that, the CPU model which built for the virtual FB-MMC circuit is similarly used to operate the physical FB-MMC prototype.

6.7.2 Description of the FB-submodule main-board

In this work, a down-scaled prototype for the single-phase FB-MMC is configured with four FB-submodule. These FB-submodules are designed by Imperix Company for implementation of multilevel converters [126]. They are suited to configure low-voltage laboratory prototype of the FB-MMC. For the configuration, all FB-submodules are placed within a metal enclosure. Each FB-submodule board can easily be connected to any control platform as the gate drive circuits which built

inside each board are designed with Optical Fiber inputs as displayed in Fig 6.10. That allows to drive PWM gating signals generated in the control platform to IGBTs of the FB-submodule. The dc capacitor voltage of this FB-submodule is regulated around (50-33) V. Moreover, the main-board of each submodule is provided with voltage and current transducers, but they are not used in this work.

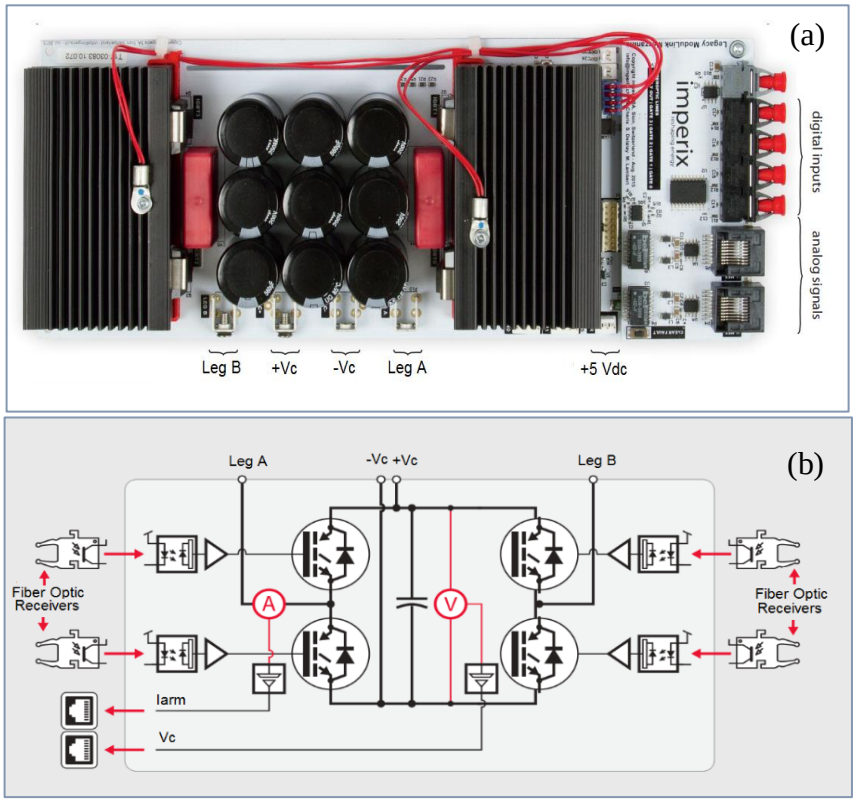


Fig 6.10 (a) Top view of the FB-submodule main-board designed by Imperix, (b) Simplified schematic of the FB-submodule provided with Optical Fiber inputs, embedded logic circuits and I/O connectors

6.7.3 Digital interface board

Design of a digital interface board is required in this research work, which allows connecting the digital output board of the OP4500 simulator to command inputs of the FB-submodule. For the FB-MMC prototype having four power submodules, the digital interface board is built on 16 independent channels as illustrated in Fig 6.11. Each digital channel is composed of a Fiber Optic transmitter

integrated with a drive circuit. The main FB-submodule board are provided with Optic Fiber receivers which used as gate drive circuit inputs of IGBTs. PWM signals generated in DO channels of the OP4500 are received using the digital interface board as an electrical form, and then converted into modulated light steams by the Fiber Optic transmitters. Modulated light steams are transmitted across Fibre Optic cables which easily used for connection between Fiber Optic receivers and transmitters. In the main-board of the FB-submodules, the modulated light steams are received and converted to electrical form as PWM gating signals for IGBTs. TC44678 MOSFET drivers are built-in the digital interface board works as buffers. They provide electrical isolation between the OP4500 simulator and FB-submodules. These circuits are used to drive much more currents required for the Fiber Optic transmitters. That because the driving current in the DO board of the OP4500 is limited. To power up DO boards from the external voltage supply of +5V, DB37 breakout board needs to be connected. Moreover, this breakout board is used to connect wiring of the OP4500 simulator and designed interface board.

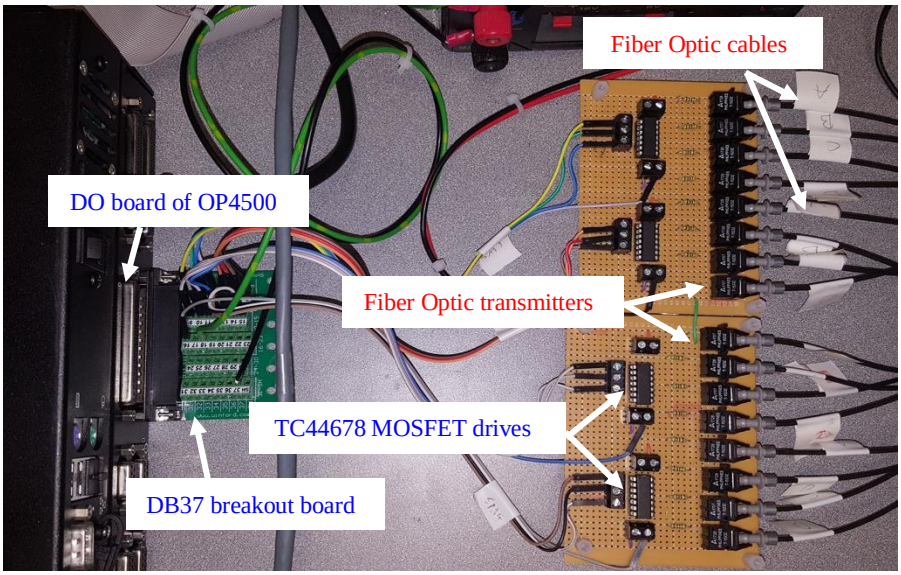


Fig 6.11 Digital interface board that designed to connect between the OP4500 simulator and main board of the FB-submodules

6.8 Real-Time Simulation and Experimental Results

For a case of the steady-state analysis, a validation for the main findings of the FB-MMC is firstly confirmed using both the real-time simulation and experimentation results. In addition, the analytical model to the harmonic contents of PWM waveform voltages is verified using the experimental results of the FB-MMC prototype. The real-time simulation results are obtained from the simulated models using CPU and FPGA cores of the OP4500. As aforementioned, the CPU model is built to generate PWM gating signals for switching devices of the single-phase FB-MMC circuit implemented in the FPGA model. Here, generating gating signals is built using the developed PSC-PWM strategy, and the control scheme is based on the open-loop mode. Experimentally, however, results are achieved using the down-scale prototype of the single-phase FB-MMC. As for the controller, the OP4500 real-time simulation is used in the open-loop testing to generate PWM gating signals of this prototype. In this case, the same the CPU model used in the real-time simulation is exploited in the experimental FB-MMC. Under the buck and boost operating modes, the results are conducted for both real-time simulation and experimental prototype of the FB-MMC. Of note, the main circuit parameters listed in Table 2 are the same for the real-time simulation and experimentation.

6.8.1 Steady-state analysis and validation of the FB-MMC results

In this work, the real-time simulation of the single-phase FB-MMC is undertaken in the buck and boost modes with the same operating conditions as the experimental prototype. Thus, the real-time simulation results for the upper and lower arm currents, output phase current, second harmonic-circulating current, capacitor voltage ripple of upper and lower arm submodules, and output phase voltage of the FB-MMC are shown and compared to the experimental waveforms under steady-state condition. Although the FB-MMC is connected to the passive

load, these obtained results are valid for the grid-connected FB-MMC, as the amplitude of the output phase voltage $\hat{v_{ph}}$ is maintained around $V_{dc\_nom}/2$ while varying the dc link voltage.

6.8.1.1 When the FB-MMC operating at buck mode

For the case of the FB-MMC operates at buck mode, the actual dc link voltage is set to 100 V. Thus this value of the dc link voltage is considered at this operating point as the nominal value V_{dc_nom}. In this case, the modulation indexes M_{ac} and M_{dc} are adjusted around 1 regarding the actual dc link voltage, that to maintain $\hat{v_{ph}}$ around $V_{dc\_nom}/2 = 50$ V. When the power factor is approximately unity, Fig 6.12 shows the real-time - simulation results of the upper and lower arm currents and resultant output phase current which is $\left(i_{arm\_low}(t) - i_{arm\_up}(t)\right)/2$. Under the same operating conditions, Fig 6.13 shows experimental results of these current waveforms. In the real-time simulation, the resultant second harmonic circulating current is obtained from $\left(i_{arm\_low}(t) + i_{arm\_up}(t)\right)$ as shown in Fig 6.14. While Fig 6.15 exhibits the resultant second harmonic circulating current experimentally. To compare the real-time simulation and experimental results, amplitudes of the arm current components associated FFT spectrum are shown in Fig 6.16. Of note that some differences in the results obtained are caused by many reasons in the experiments. Mainly, they are non-ideal switching function of IGBTs, voltage drop and magnetic characteristic of the arm inductors, and the capacitor voltage regulation for FB-SMs is not implemented into this work. Regarding the values of the modulation indexes M_{ac} and M_{dc}, the capacitor voltage V_C of each FB-submodule is regulated in this buck mode around 50 V. For both simulation and experimental results, the capacitor voltage ripples of the upper and lower FB-submodules are displayed in Fig 6.17 and Fig 6.18. It can be observed that the voltage across capacitors fluctuates around 4 %. As the FB-MMC is configured with *N*=2, the output phase voltage here is produced with two levels. The real-time

simulation result of the output phase voltage is presented in Fig 6.19, and is experimentally compared in Fig 6.20.

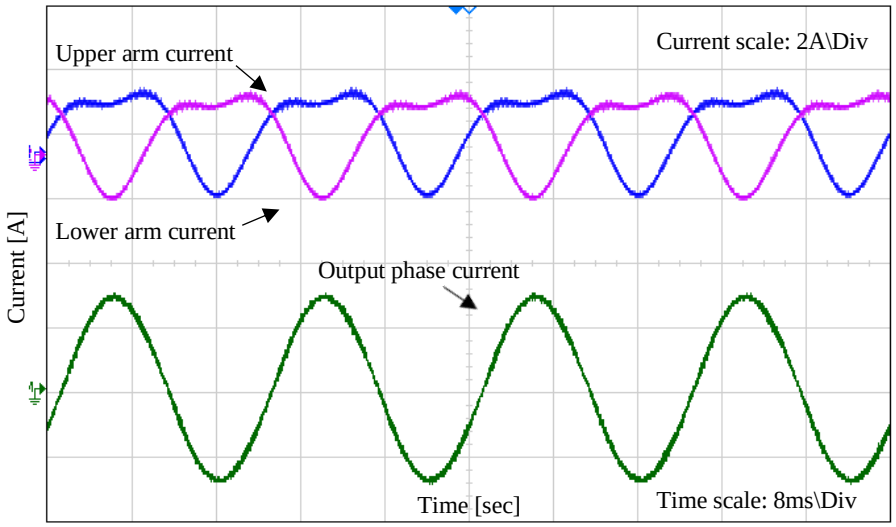


Fig 6.12 Real-time - simulation results of the upper and lower arm currents and resultant output phase current when the FB-MMC operates in buck mode at V_{dc_act} =100 V (100 % of V_{dc_nom}), and $V_C = 50$ V which defined by (3.16)

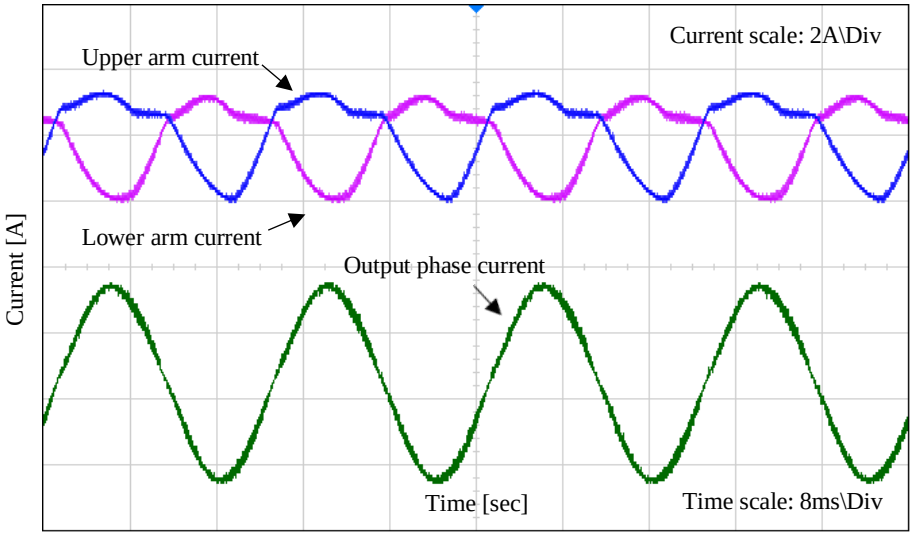


Fig 6.13 Experimental results of the upper and lower arm currents and resultant output phase current when the FB-MMC operates in the buck mode at V_{dc_act}=100 V (100 % of V_{dc_nom}), and $V_C = 50$ V which defined by (3.16)

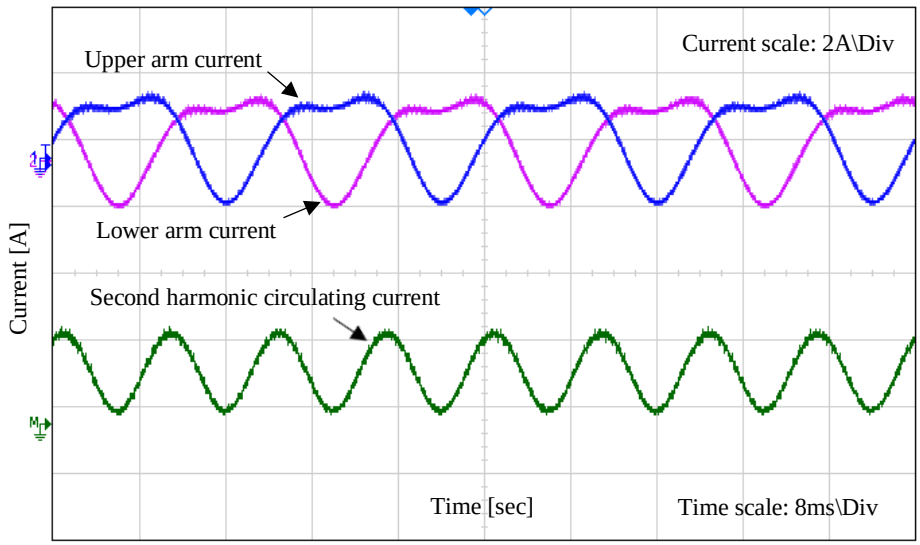


Fig 6.14 Real-time - simulation results of the upper and lower arm currents and resultant second harmonic-circulating current when the FB-MMC operates in buck mode at V_{dc_act}=100 V (100 % of V_{dc_nom}), and V_C = 50 V which defined by (3.16)

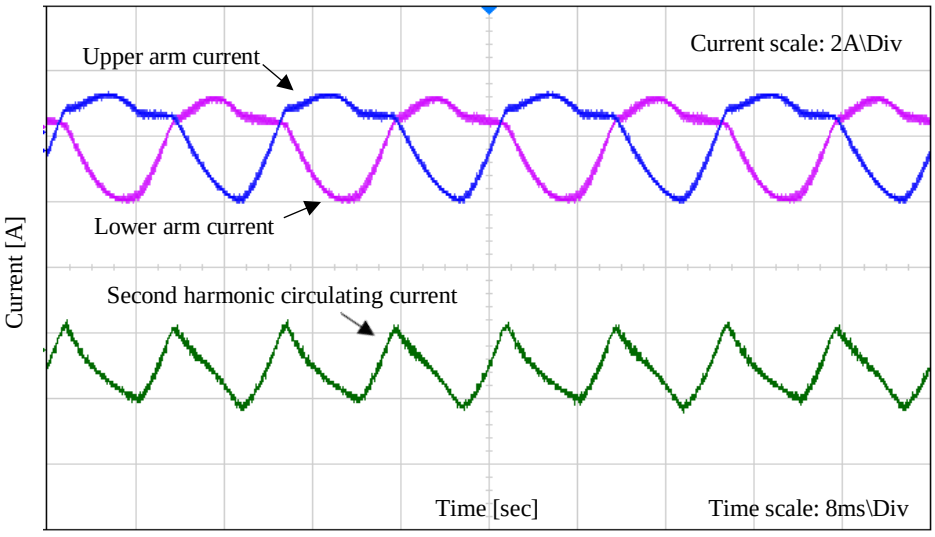


Fig 6.15 Experimental results of the upper and lower arm currents and resultant second harmonic-circulating current when the FB-MMC operates in buck mode at V_{dc_act}=100 V (100 % of V_{dc_nom}), and V_C = 50 V which defined by (3.16)

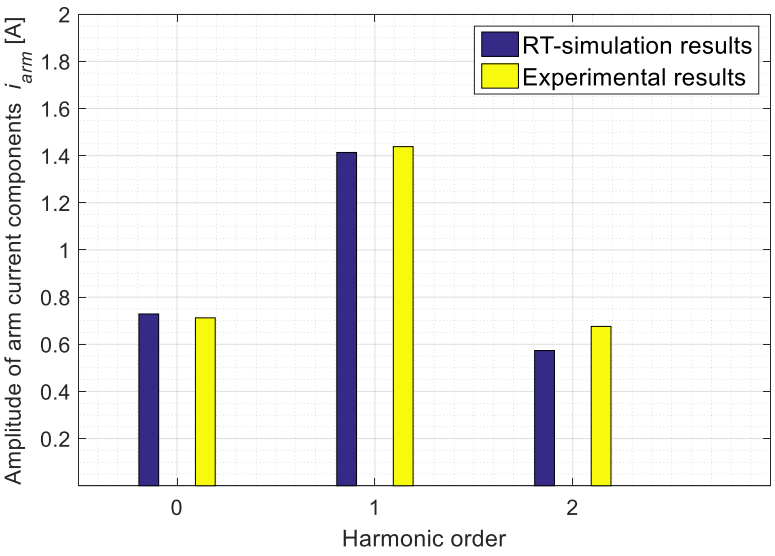


Fig 6.16 FFT harmonic spectrum of the arm current (in amplitudes) when the FB-MMC operates in buck mode at V_{dc_act}=100 V (100 % of V_{dc_nom}), and $V_C = 50$ V which defined by (3.16)

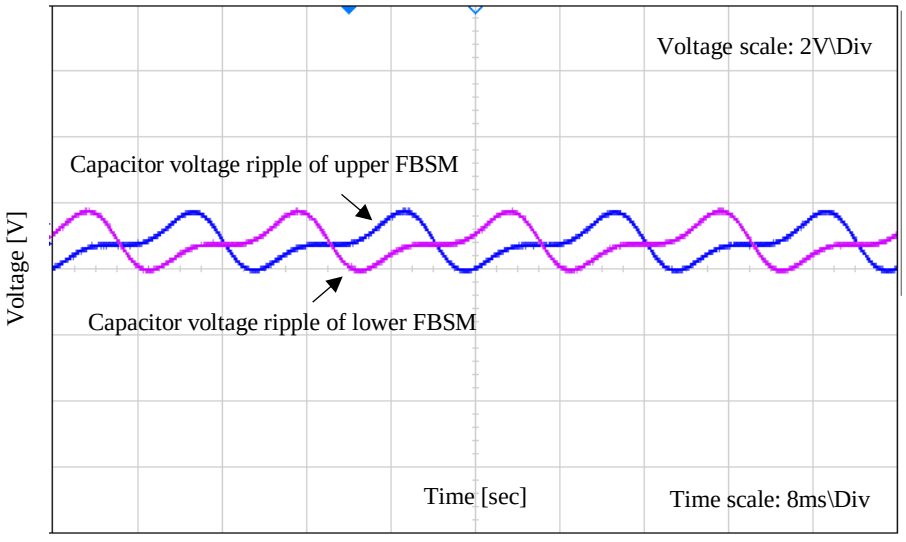


Fig 6.17 Real-time - simulation results of the upper and lower capacitor voltage ripples when the FB-MMC operates in buck mode at V_{dc_act}=100 V (100% of V_{dc_nom}), and $V_C = 50$ V which defined by (3.16)

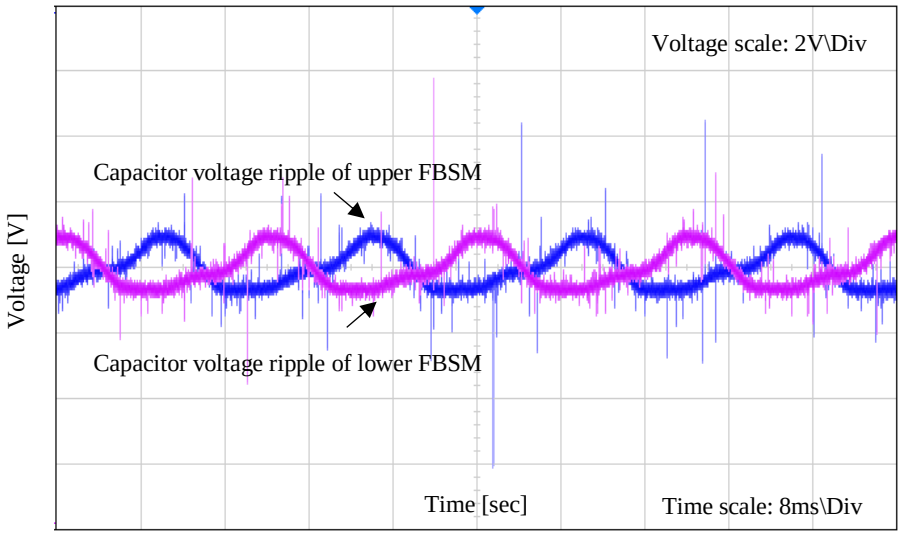


Fig 6.18 Experimental results of the upper and lower capacitor voltage ripples when the FB-MMC operates in buck mode at V_{dc_act}=100 V (100% of V_{dc_nom}), and $V_C = 50$ V which defined by (3.16)

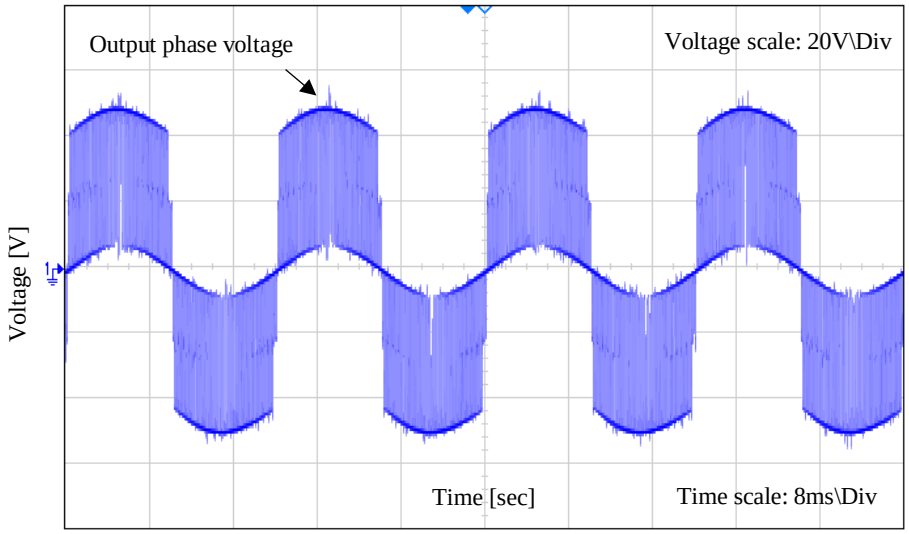


Fig 6.19 Real-time - simulation results of the output phase voltage when the FB-MMC operates in buck mode at V_{dc_act}=100 V (100 % of V_{dc_nom}), and $V_C = 50$ V which defined by (3.16)

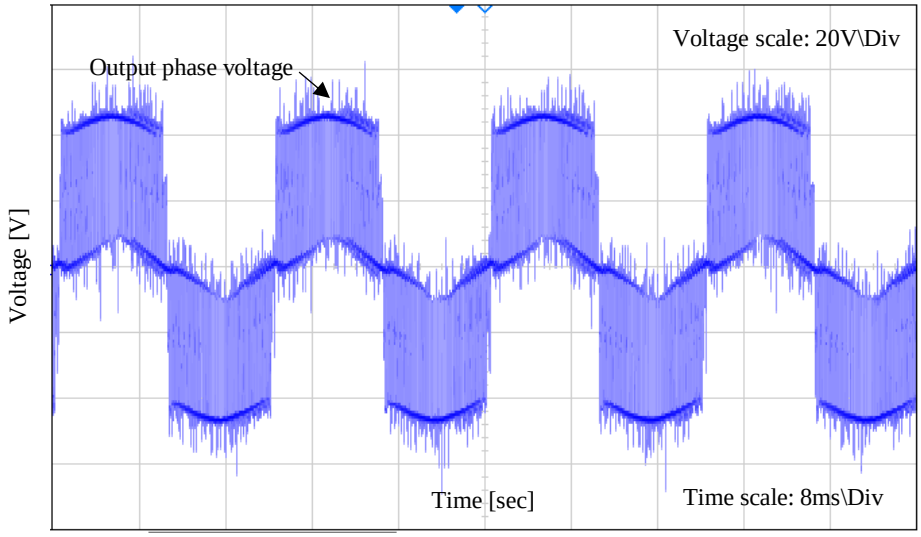


Fig 6.20 Experimental results of the output phase voltage when the FB-MMC operates in buck mode at V_{dc_act}=100 V (100% of V_{dc_nom}), and $V_C = 50$ V which defined by (3.16)

6.8.1.2 When the FB-MMC operating at the boost mode

In the boost mode, the FB-MMC implemented into the real-time simulation and experiments are carried out while V_{dc_act} is performed at 60 % of V_{dc_nom}. Two regulation voltage approaches for the FB-submodule capacitors are also tested in this work. In the first regulation approach as defined by (3.16), the values of the modulation indexes are adjusted in the real-time simulation to be ($M_{dc} = 0.6$ and $M_{ac} = 1$) , that allows to maintain the amplitude of the output phase voltage $\hat{v_{ph}}$ around ($V_{dc\_nom}/2$=50 V). In this case, the upper and lower arm currents and resultant output phase current are verified for both the real-time simulation and experimentally, as shown in Fig 6.21 and Fig 6.22. The resultant second harmonic circulating currents are also obtained as displayed in Fig 6.23 and Fig 6.24. It can be observed that circulating currents and arm currents are superimposed on the switching ripples, that because the interleaving between the upper and lower arm voltages occurs in the boost mode. Fig 6.25 shows amplitudes of the upper and lower arm currents associated FFT spectrum. It can be seen that the reduction in the second

harmonic circulating currents is achieved at this operating point of the boost mode. As the FB-MMC works at constant load current mode, the dc current components increased, and half of the load currents remain constant if compared to the buck mode. Experimentally, it requires to be set at M_{dc} = 0.56 instead of 0.6, that to overcome a voltage drop across arm inductors during the boost mode condition, while M_{ac} is kept at the same value. The capacitor voltage ripples of the upper and lower FB-submodules are displayed and compared in both Fig 6.26 and Fig 6.27. It can be observed that the fluctuation of the capacitor voltages is decreased to 2%. Of note that all capacitor voltages are regulated around 50 V regarding (3.16). If compared to buck mode, more voltage levels are achieved at this operating point of the boost mode. From both Fig 6.28 and Fig 6.29, it can be seen that the output phase voltages are generated with five voltage levels. Where each voltage level is scaled by $V_C/2$. In experimental results, it can be seen that the scale of the voltage output level is significantly affected by M_{dc} and capacitor voltages which are not regulated evenly.

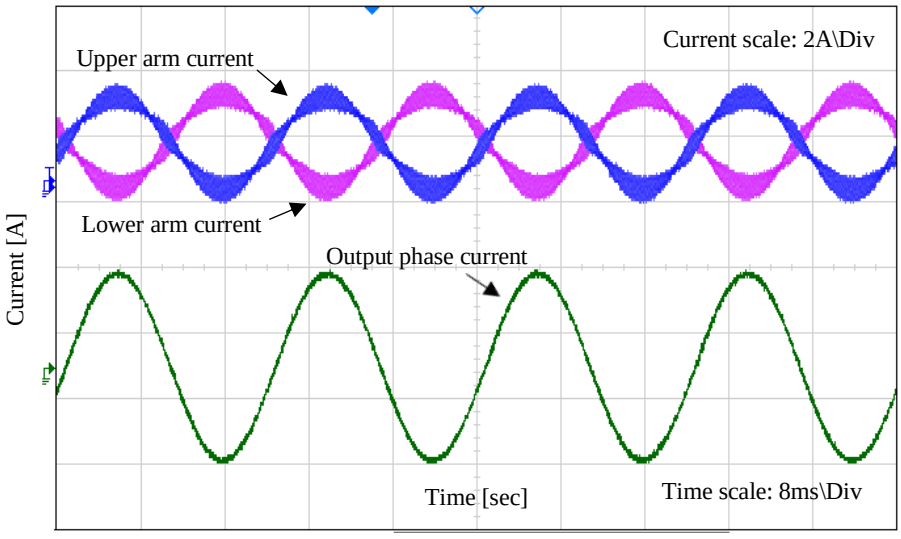


Fig 6.21 Real-time simulation results of the upper and lower arm currents and resultant output phase current when the FB-MMC operates in the boost mode at V_{dc_act}=60 V (60 % of V_{dc_nom}), and V_C = 50 V which defined by (3.16)

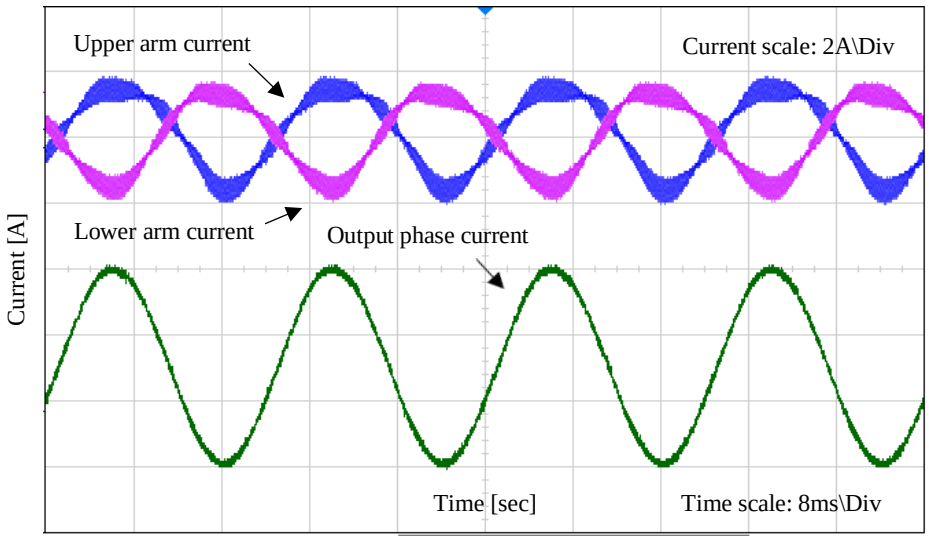


Fig 6.22 Experimental results of the upper and lower arm currents and resultant output phase current when the FB-MMC operates in boost mode at V_{dc_act}=60 V (60 % of V_{dc_nom}), and $V_C = 50$ V which defined by (3.16)

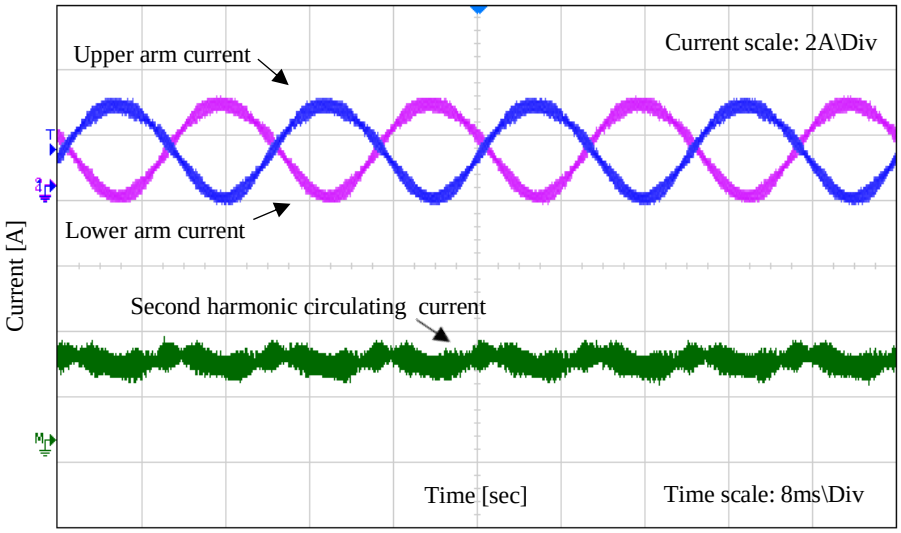


Fig 6.23 Real-time simulation results of the upper and lower arm currents and resultant second harmonic-circulating current when the FB-MMC operates in the boost mode at V_{dc_act}=60 V (60 % of V_{dc_nom}), and $V_C = 50$ V which defined by (3.16)

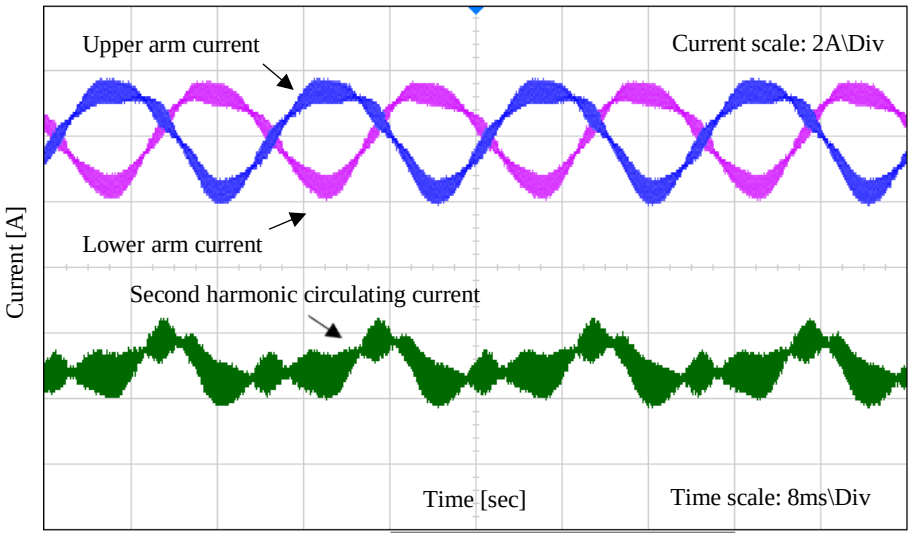


Fig 6.24 Experimental results of the upper and lower arm currents and resultant second harmonic-circulating current when the FB-MMC operates in the boost mode at V_{dc_act}=60 V (60 % of V_{dc_nom}), and V_C = 50 V which defined by (3.16)

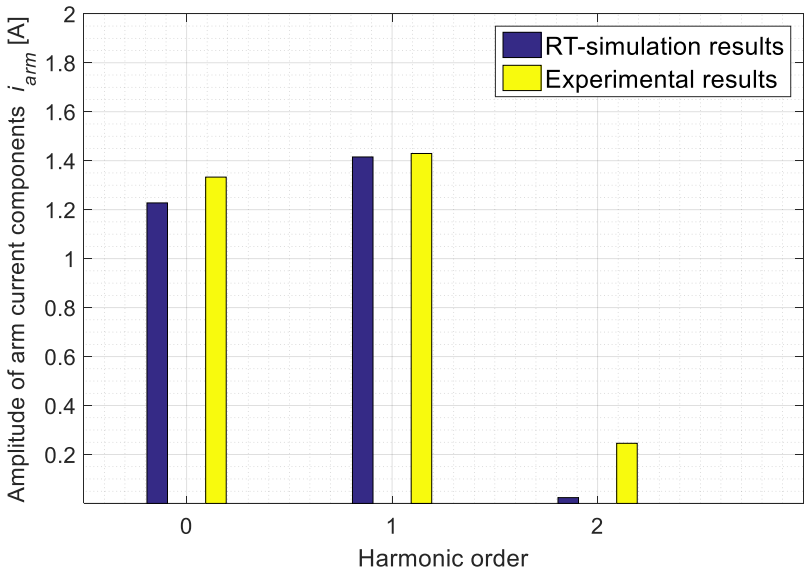


Fig 6.25 FFT harmonic spectrum of the arm current (in amplitudes) when the FB-MMC operates in boost mode at V_{dc_act}=60 V (60 % of V_{dc_nom}), and V_C = 50 V which defined by (3.16)

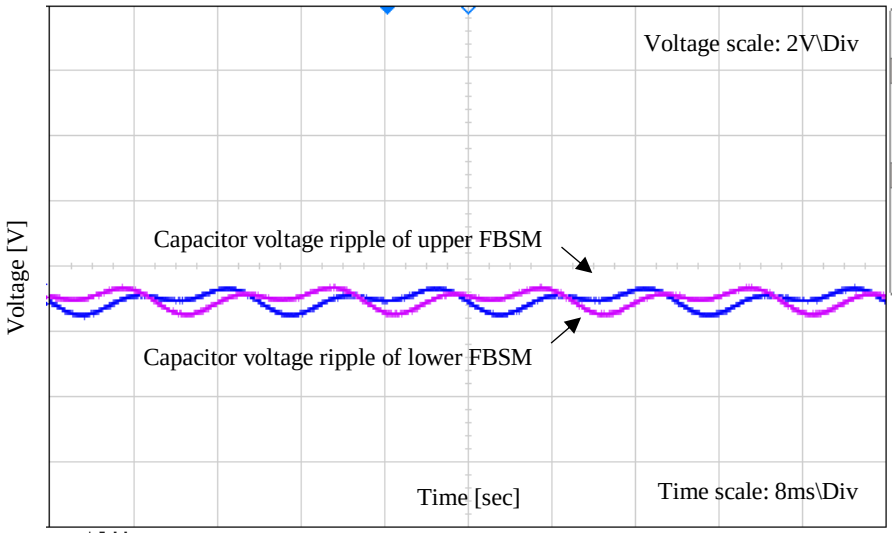


Fig 6.26 Real-time simulation results of the upper and lower capacitor voltage ripples when the FB-MMC operates in the boost mode at V_{dc_act}=60 V (60 % of V_{dc_nom}), and $V_C = 50$ V which defined by (3.16)

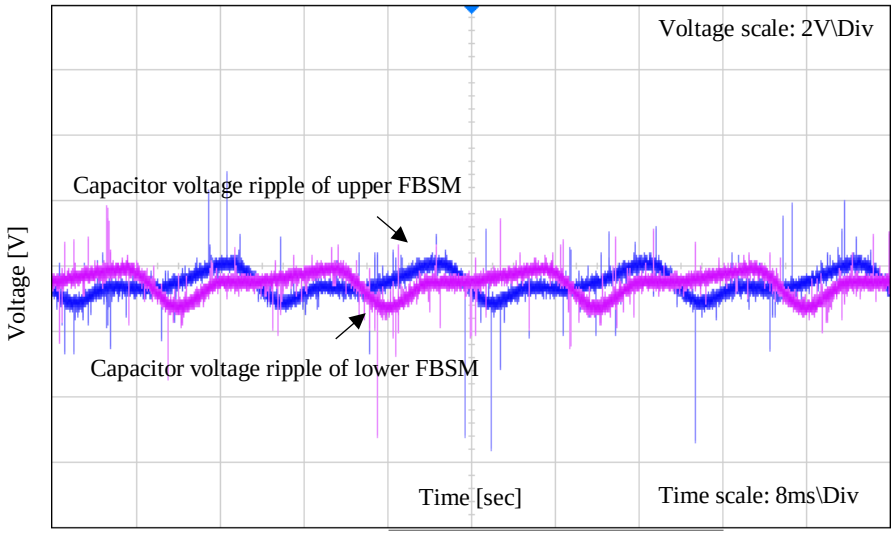


Fig 6.27 Experimental results of the upper and lower capacitor voltage ripples when the FB-MMC operates in the boost mode at V_{dc_act}=60 V (60 % of V_{dc_nom}), and $V_C = 50$ V which defined by (3.16)

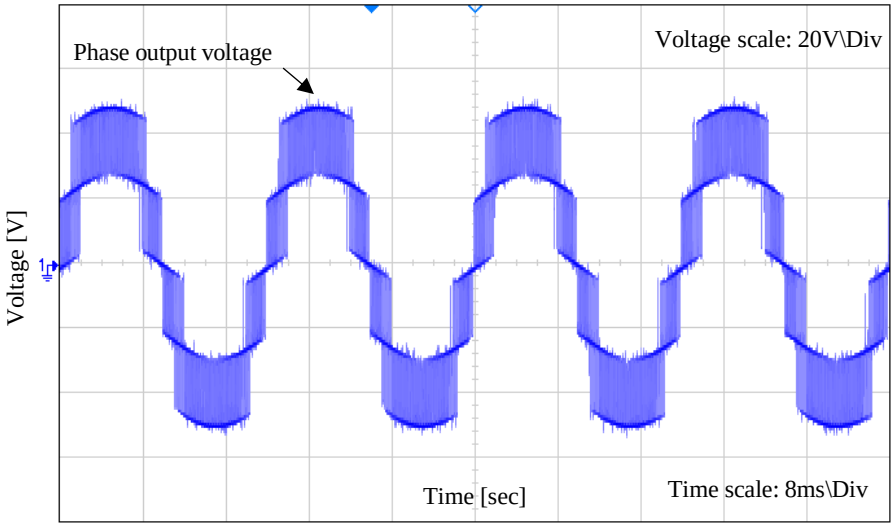


Fig 6.28 Real-time simulation results of the output phase voltage when the FB-MMC operates in the boost mode at V_{dc_act}=60 V (60 % of V_{dc_nom}), and $V_C = 50$ V which defined by (3.16)

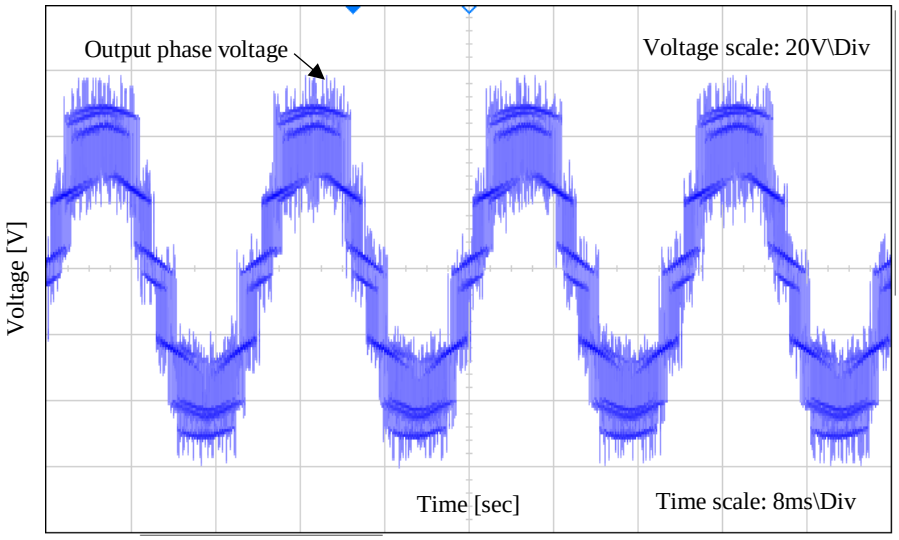


Fig 6.29 Experimental results of the output phase voltage when the FB-MMC operates in the boost mode at V_{dc_act}=60 V (60 % of V_{dc_nom}), and $V_C = 50$ V which defined by (3.16)

However, the second approach of the capacitor voltage regulation is made according to V_{dc_act}. In this case, the values of the modulation indexes are set in the

simulation to be $M_{ac} = 1.75$ and $M_{dc} = 0.75$. Under this operating point, the upper and lower arm currents and output phase current are verified in the real-time simulation and experiment, as illustrated in Fig 6.30 and Fig 6.31. For the second harmonic circulating currents, the results are also presented in Fig 6.32 and Fig 6.33. It can be noted that arm currents and circulating currents are superimposed on the switching ripples due to the interleaving in the boost mode. FFT results of the arm currents are compared and shown in Fig 6.34. For both simulation and experimental results, the capacitor voltage ripples of both arm FB-submodules are fluctuated around 2%, as shown in Fig 6.35 and Fig 6.36. Considering (3.17), the capacitor voltage V_C of each FB-submodule here is regulated around 40 V. Experimentally, it requires to be set at M_{dc} = 0.73, that to regulate $\hat{v_{ph}}$ at 50 V. Both simulation and experimental results of the output phase voltage are displayed in Fig 6.37 and Fig 6.38. As voltage level is scaled by $V_C/2$. $\hat{v_{ph}}$ is generated with seven levels. Experimentally, the voltage level is affected by uneven capacitor voltage regulation.

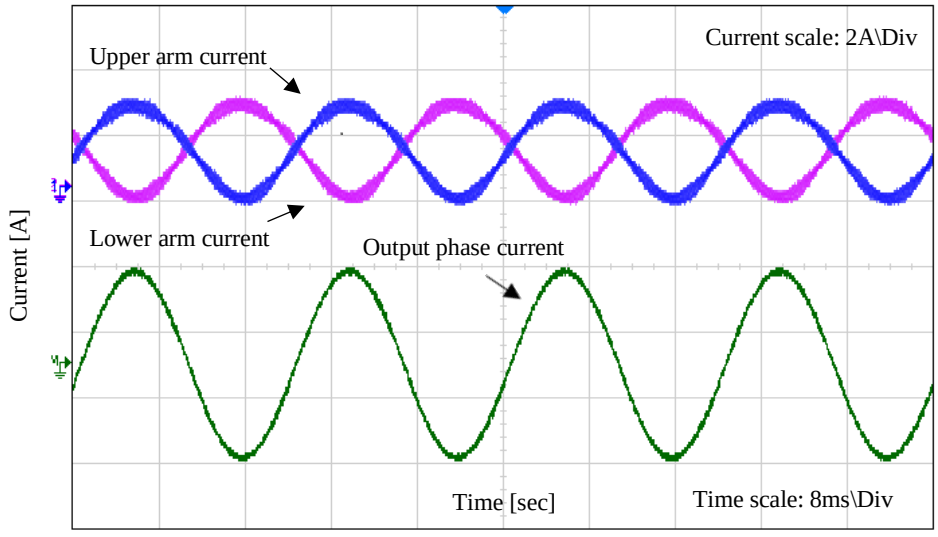


Fig 6.30 Real-time simulation results of the upper and lower arm currents and resultant output phase current when FB-MMC operates in boost mode at V_{dc_act}=60 V (60 % of V_{dc_nom}), and V_C = 40 V which defined by (3.17)

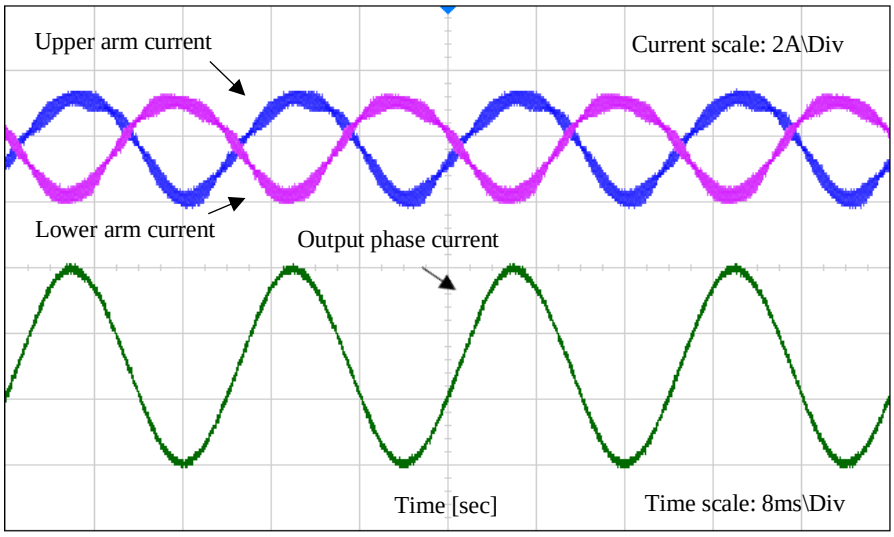


Fig 6.31 Experimental results of the upper and lower arm currents and resultant output phase current when the FB-MMC operates in boost mode at V_{dc_act}=60 V (60 % of V_{dc_nom}), and V_C = 40 V which defined by (3.17)

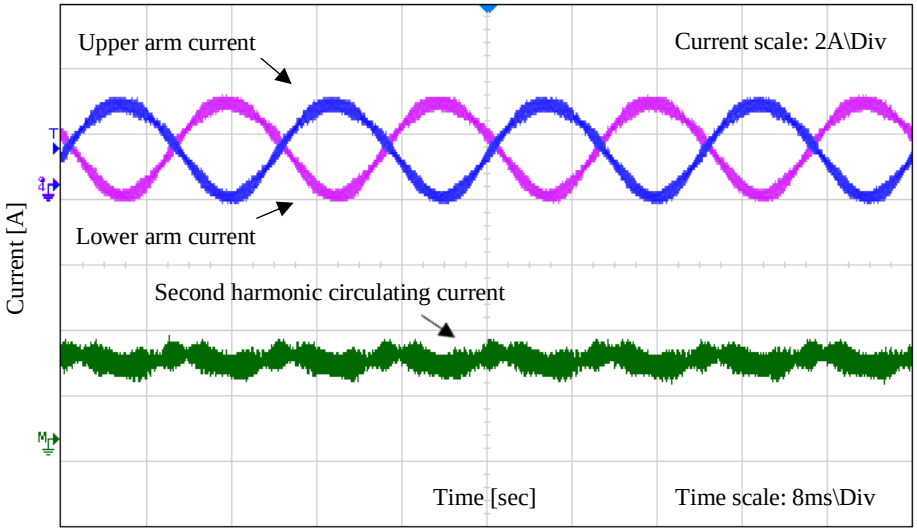


Fig 6.32 Real-time simulation results of the upper and lower arm currents and resultant second harmonic-circulating current when the FB-MMC operates in the boost mode at V_{dc_act}=60 V (60 % of V_{dc_nom}), and V_C = 40 V which defined by (3.17)

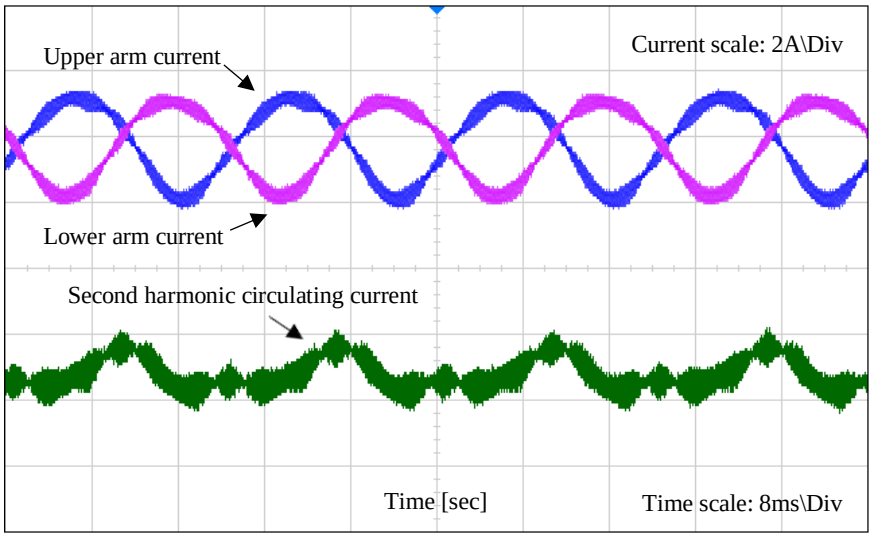


Fig 6.33 Experimental results of the upper and lower arm currents and resultant second harmonic-circulating current when the FB-MMC operates in the boost mode at V_{dc_act}=60 V (60 % of V_{dc_nom}), and V_C = 40 V which defined by (3.17)

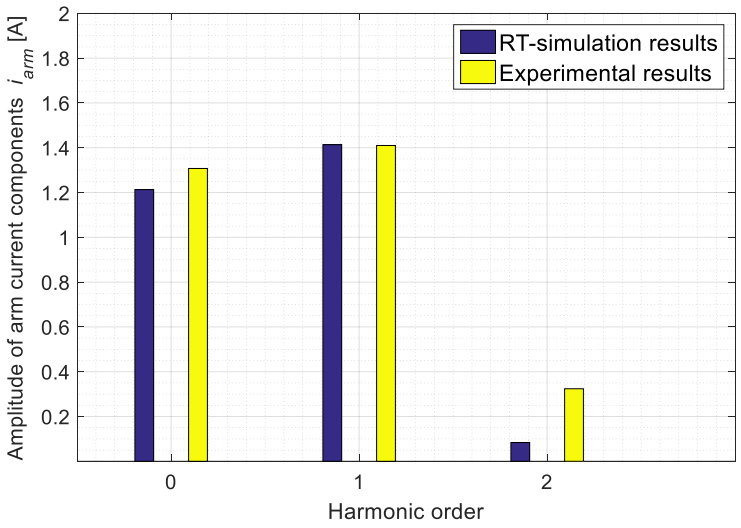


Fig 6.34 FFT harmonic spectrum of the arm current (in amplitude)when the FB-MMC operates in the boost mode at V_{dc_act}=60 V (60 % of V_{dc_nom}), and V_C = 40 V which defined by (3.17)

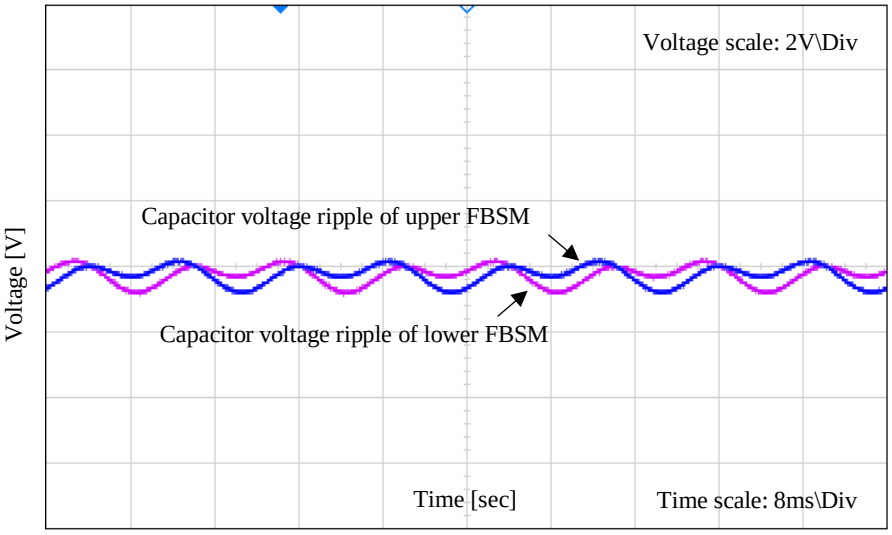


Fig 6.35 Real-time simulation results of the upper and lower capacitor voltage ripples when the FB-MMC operates in the boost mode at V_{dc_act}=60 V (60 % of V_{dc_nom}), and $V_C = 40$ V which defined by (3.17)

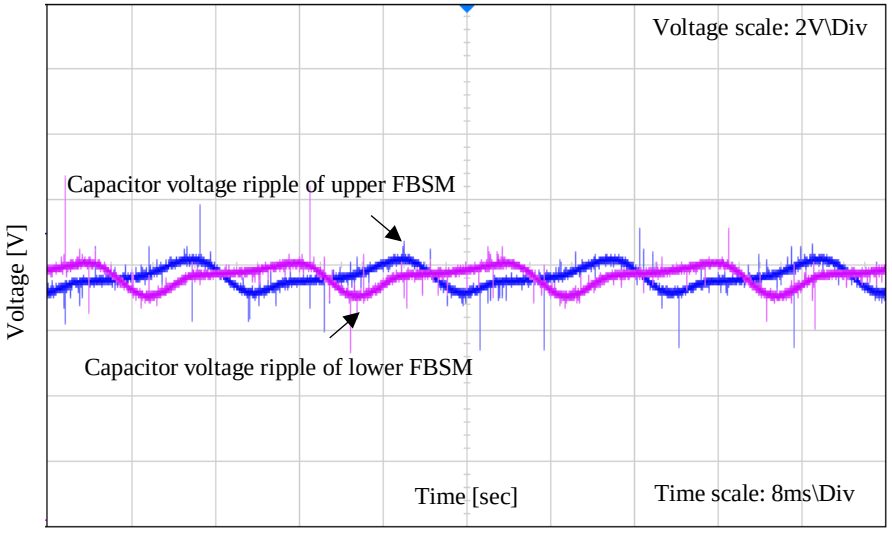


Fig 6.36 Experimental results of the upper and lower capacitor voltage ripples when the FB-MMC operates in the boost mode at V_{dc_act} = 60 V (60 % of V_{dc_nom}), and $V_C = 40$ V which defined by (3.17)

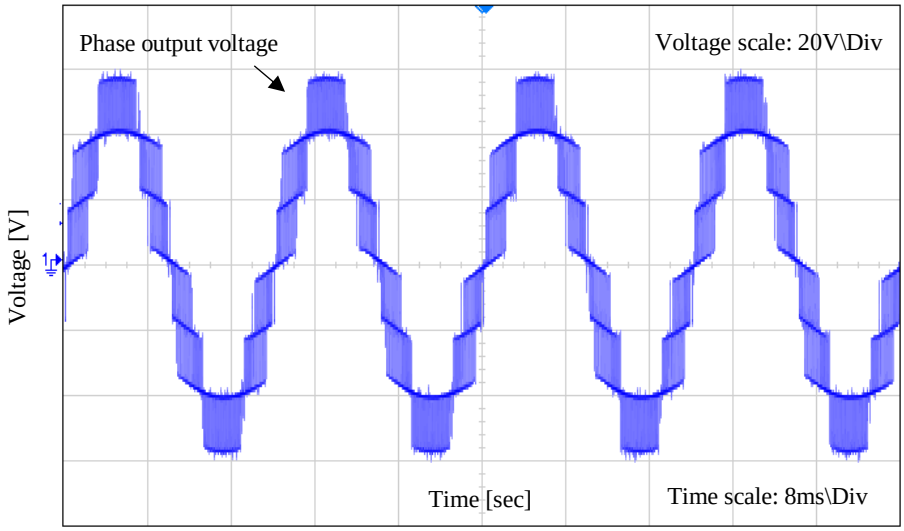


Fig 6.37 Real-time simulation results of the output phase voltage when the FB-MMC operates in the boost mode at V_{dc_act}=60 V (60 % of V_{dc_nom}), and $V_C = 40$ V which defined by (3.17)

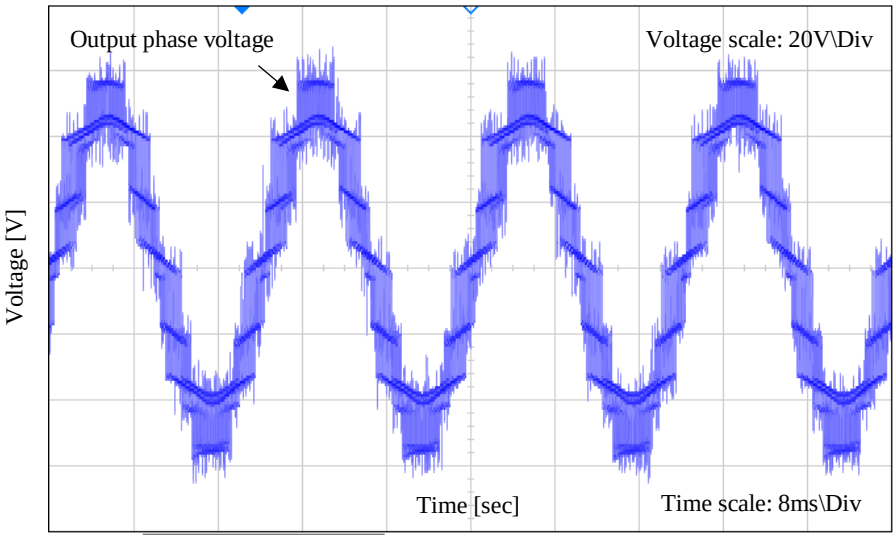


Fig 6.38 Experimental simulation results of the output phase voltage when the FB-MMC operates in the boost mode at V_{dc_act}=60 V (60 % of V_{dc_nom}), and $V_C = 40$ V which defined by (3.17)

6.8.2 The analytical model of harmonic contents and experimental validation for PWM voltage waveforms of the FB-MMC

Experiments on the single-phase FB-MMC prototype is conducted in this section under the buck and boost modes. The FB-MMC prototype is modulated using the developed PSC-PWM strategy, and the switching frequency f_{sw} of the IGBT device is equal to 2 kHz. Thus the frequency ratio is determined as $m_f = f_{sw}/f_o = 40$. Experimental results obtained are shown for the output voltage of the upper and lower FB-submodules, the upper and lower arm voltages, and output phase voltage. The harmonic spectrum associated with FFT of these experimental results is analysed and validated to expressions of the analytical harmonic contents model of PWM voltage waveforms. This analytical model, which derived in chapter 5, is implemented using the simulation in the M-file based model. Of note that some differences are caused by the modulation strategy used that considers different sampling time. Whereas the analytical harmonic content expressions are derived regarding the double-edge naturally sampled PWM. However, in experiments, the double-edge asymmetrical sampled PWM is implemented into OP4500 simulator. Referring to obtained results of the output voltage THD which illustrated in blue in Fig 5.22 (a) and (b), some operating points of the FB-MMC are specified at a different level of the dc link voltage.

6.8.2.1 Harmonic contents validation when FB-MMC operating in buck mode

In this case, the FB-MMC prototype is tested under buck mode in which V_{dc_act} = 100 V. Both dc and ac modulation indexes are adjusted around 1. That is to regulate V_C around 50V as defined by (3.16). Fig 6.39 shows the experimental output voltage waveforms of upper and lower FB-submodules. Here, FB-submodules are produced only two levels of voltages: the positive voltage $+50$ V when the submodule is inserted, and the zero voltage when the submodule is bypassed. As shown in Fig 6.40, the harmonic spectrum of these experimental results is analysed using FFT and then compared to that of the analytical expression of the harmonic contents defined by (5.28). Each FB-submodule output voltage is

produced as a result of a subtraction between the right and left leg voltages. Consequently, the first carrier group achieves at $2m_f$ =80 which represents twice switching frequency f_{sw}. It can also be seen that the harmonic spectrum of each FB submodule output voltage contains only even sideband harmonics around the odd carrier groups> While the odd sideband harmonics around the even carrier. The upper and lower arm voltage waveforms are experimentally displayed in Fig 6.41. Of note that all amplitudes of harmonic contents in this study are normalised by $V_{dc\_nom}/2$. Because the FB-MMC is configured with two FB-submodules per arm, the harmonic cancellation here is achieved by phase shifting each FB-submodule carrier of π/2. Fig 6.42 shows the analytical expression of the harmonic contents defined by (5.30) and experimental validation. It shows that harmonic carrier groups of each arm voltage achieve at $\{4m_f, 8m_f, ..\text{etc}\}$ which can be expressed by $\{2Nm_f\}^{th}$ multiples. It can be noted that sideband harmonic contents in each carrier group are existed in the odd order harmonics. The output phase voltage waveform of three levels is presented in Fig 6.43. As the odd sideband harmonics in the upper arm voltage are in opposite directions to those of over the lower arm voltages, these sideband harmonic contents appear without any cancellation in the output phase voltage as illustrated in Fig 6.44. The results here are achieved based on the analytical expression of the harmonic contents defined by (5.32) and then matched with experimental validation.

6.8.2.2 Harmonic contents validation when FB-MMC operating in the boost mode

In this case, the FB-MMC prototype is tested at two operating points under the boost mode. These operating points are chosen in terms of achieving an optimal THD of the output phase voltage. Based on the first capacitor voltage regulation as illustrated in blue in Fig 5.22 (a), the optimal operating point is obtained when the FB-MMC prototype works at V_{dc_act} = 50 V (50 % of V_{dc_non}).

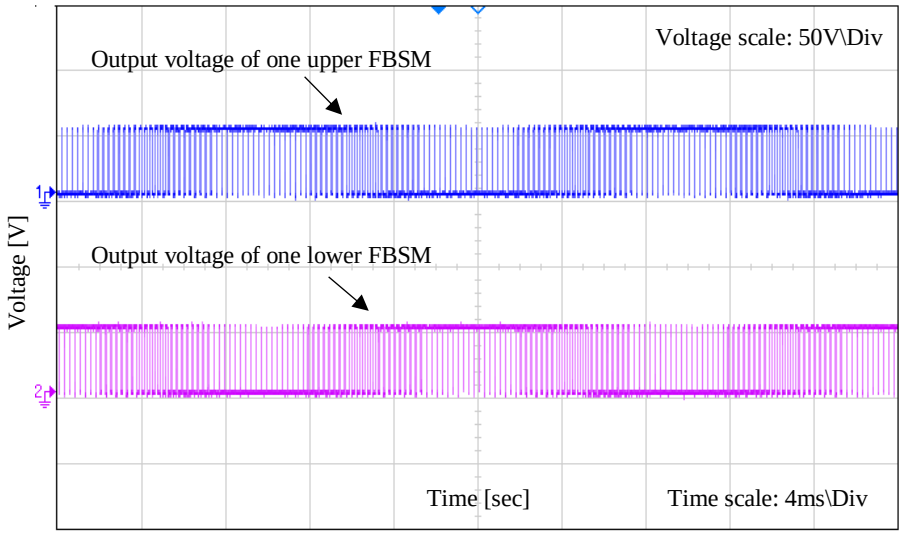


Fig 6.39 Experimental output voltage waveforms of the upper and lower FB-submodules when FB-MMC with (N=2) operates in buck mode at V_{dc_act}= 100 V (100 of V_{dc_nom}), and $V_C = 50\ V$ which defined by (3.16)

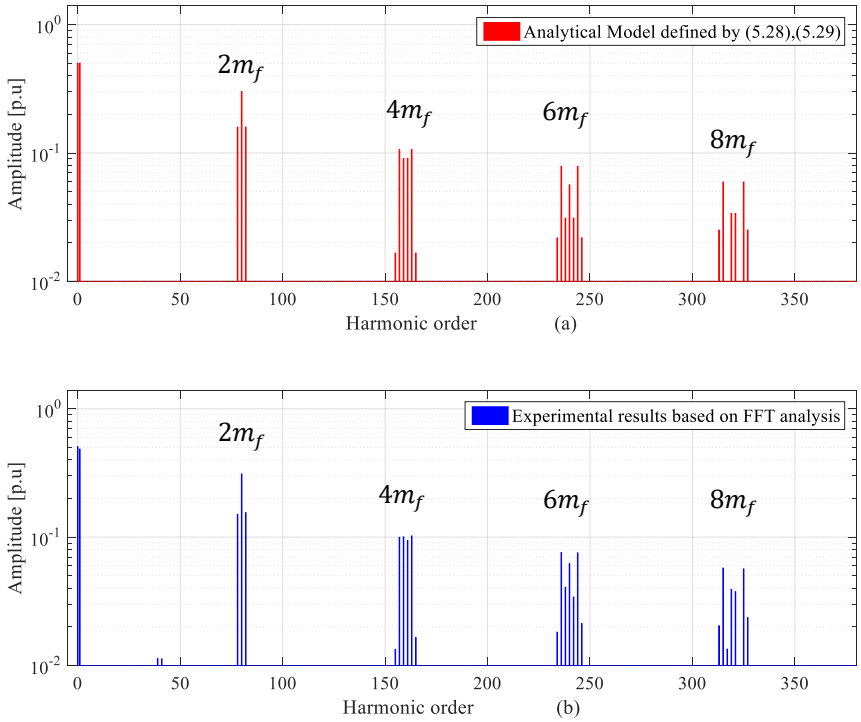


Fig 6.40 Harmonic spectrums for any FB-submodule voltage operates in buck mode at V_{dc_act} = 100 V (100 of V_{dc_nom}), and $V_C = 50\ V$ which defined by (3.16): (a) The analytical model results, (b) FFT of the experimental results

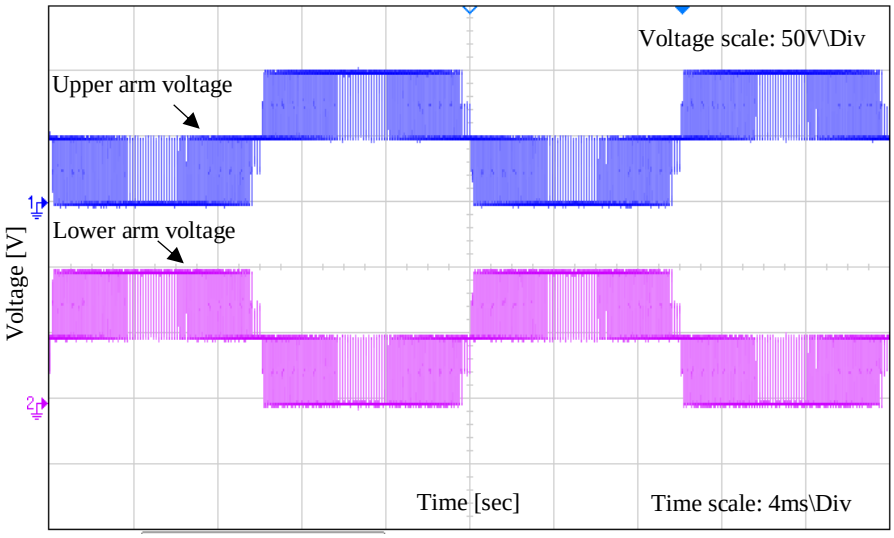


Fig 6.41 Experimental the upper and lower arm voltage waveforms of the FB-MMC with (N=2) when operates in buck mode at V_{dc_act}= 100 V (100 of V_{dc_nom}), and $V_C = 50\ V$ which defined by (3.16)

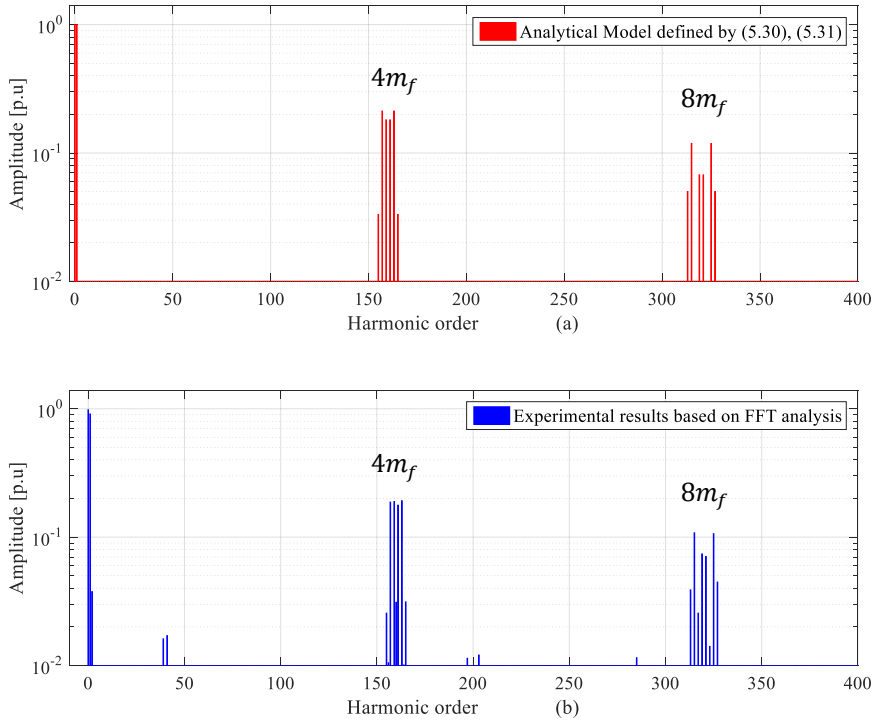


Fig 6.42 Harmonic spectrums for any arm voltage when FB-MMC operates in buck mode at V_{dc_act}= 100 V (100 of V_{dc_nom}), and $V_C = 50\ V$ which defined by (3.16): (a) The analytical model results, (b) FFT of the experimental results

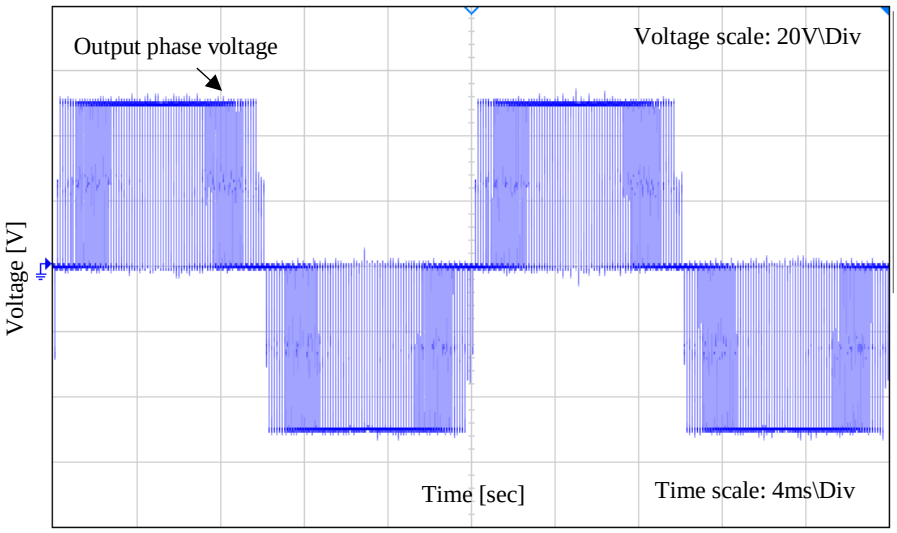


Fig 6.43 Experimental output phase voltage waveform of the FB-MMC with (N=2) when operates in buck mode at V_{dc_act}= 100 V (100 of V_{dc_nom}), and $V_C = 50\ V$ which defined by (3.16)

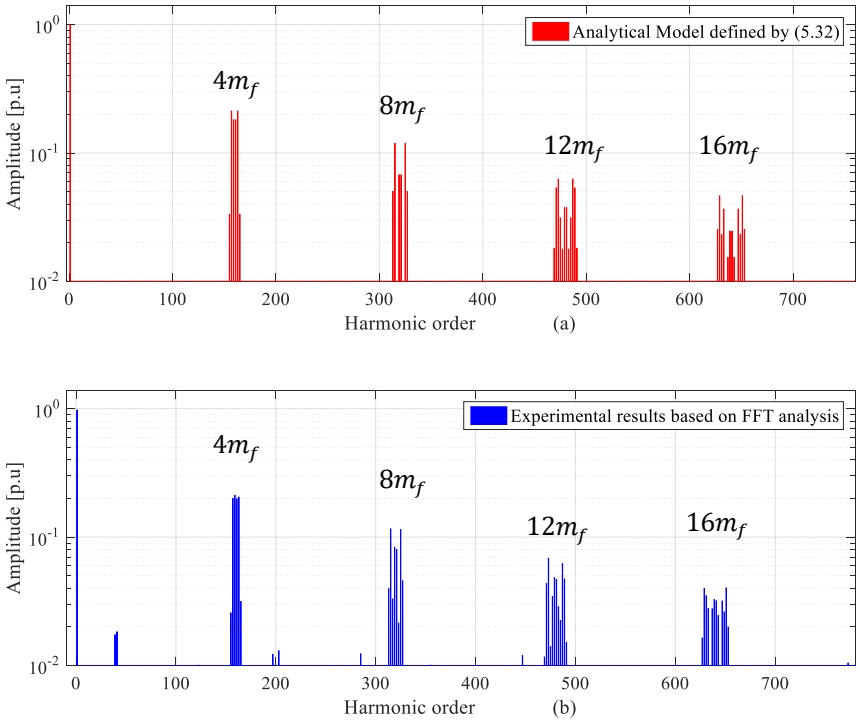


Fig 6.44 Harmonic spectrums for output phase voltage when FB-MMC operates in buck mode at V_{dc_act}= 100 V (100 of V_{dc_nom}), and $V_C = 50\ V$ which defined by (3.16): (a) The analytical model results, (b) FFT of the experimental results

Here, the values of the modulation indexes are adjusted to be ($M_{dc} = 0.5$ and $M_{ac} = 1$) that allows regulate V_C around 50 V as defined by (3.16), and to maintain the amplitude of the output phase voltage $\hat{v_{ph}}$ around ($V_{dc\_nom}/2$=50 V). Under this operating condition, Fig 6.45 shows the experimental output voltage waveforms of upper and lower FB-submodules. In this case, each FB-submodule is inserted either at the negative voltage -50 V or at the positive voltage $+50$ V, and the zero voltage when the submodule is bypassed. Fig 6.46 shows the analytical expression of the harmonic contents defined by (5.30). They are compared to experimental results that analysed using FFT. It can be indicated that the harmonic spectrum of each FB submodule output voltage contains odd and even sideband harmonics around the odd carrier groups of $\{2m_f, 6m_f, .. \text{etc}\}$. For a case of the even carrier groups of $\{4m_f, 12m_f, .. \text{etc}\}$, they consist of the even sideband harmonics, while odd sideband harmonics are centred around even carrier groups of $\{8m_f, 16m_f, .. \text{etc}\}$. The experimental voltage waveforms of both arms are displayed in Fig 6.47. These arm voltages are generated at three levels. Based on the expression defined by (5.30), results of the analytical harmonic contents are obtained and verified to the experimental results, as shown in Fig 6.48. It can be observed that that harmonic carrier groups of each arm voltage achieve at $\{4m_f, 8m_f, .. \text{etc}\}$ expressed by $\{2Nm_f\}^{th}$ multiples. At this operating point, results show that the even sideband harmonic contents are existed in each odd carrier groups. On the contrary, the odd sideband harmonic contents occur in each even carrier groups. Since these even sideband harmonics in the upper arm voltage are in same directions to those of the lower arm voltages, these sideband harmonic contents are cancelled in the output phase voltage. Consequently, the output phase voltage is generated with five levels, as shown in Fig 6.49. In comparison with the analytical expression defined by (5.32) and experimental contents, the harmonic carrier groups achieve at $\{8m_f, 16m_f, .. \text{etc}\}$, as illustrated in Fig 6.50.

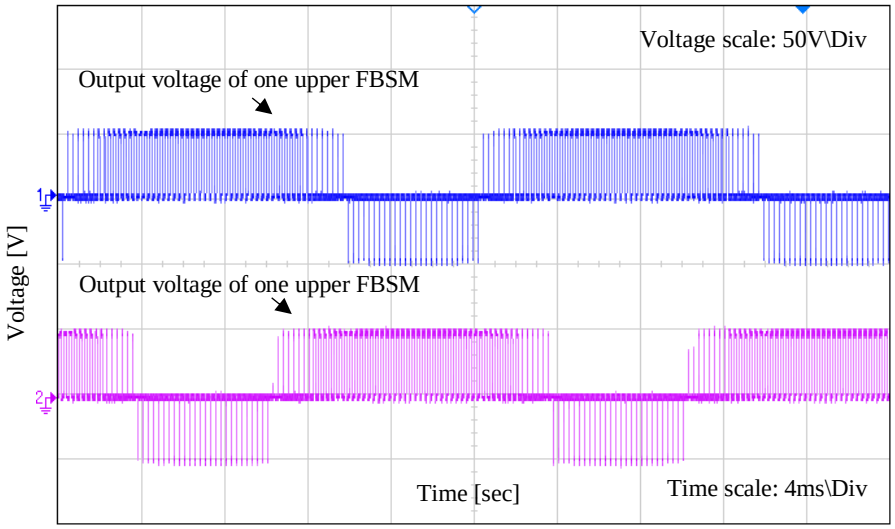


Fig 6.45 Experimental output voltage waveforms of the upper and lower FB-submodules when FB-MMC with (N=2) operates in boost mode at V_{dc_act}= 50 V (50 of V_{dc_nom}), and $V_C = 50$ V which defined by (3.16)

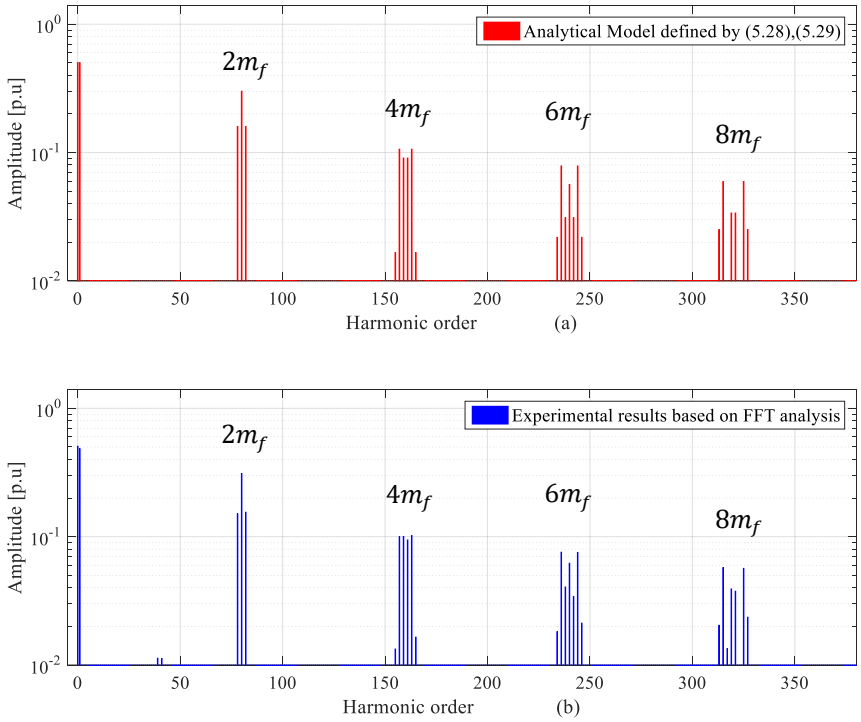


Fig 6.46 Harmonic spectrums for any FB-submodule voltage operates in the boost mode at V_{dc_act} = 50 V (50 of V_{dc_nom}), and $V_C = 50$ V which defined by (3.16): (a) the analytical model results, (b) FFT of the experimental results

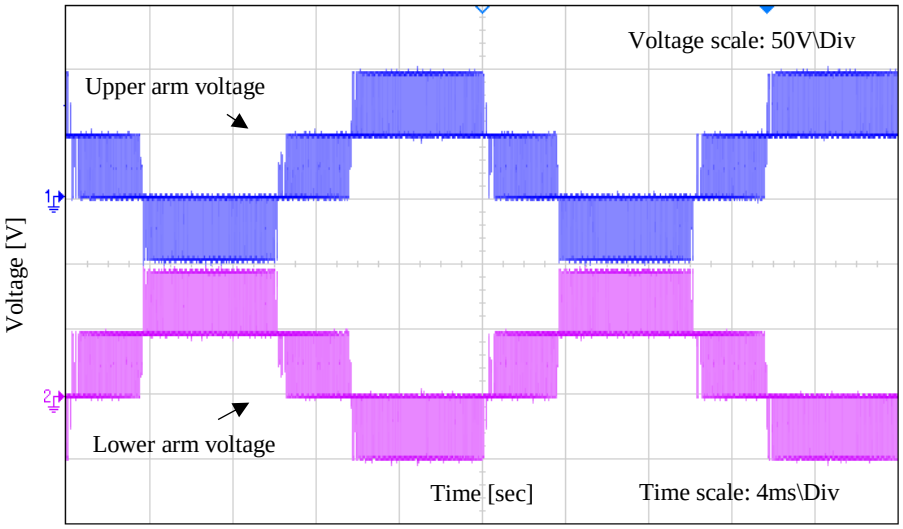


Fig 6.47 Experimental the upper and lower arm voltage waveforms of the FB-MMC with (N=2) when operates in the boost mode at V_{dc_act}= 50 V (50 of V_{dc_nom}), and $V_C = 50$ V which defined by (3.16)

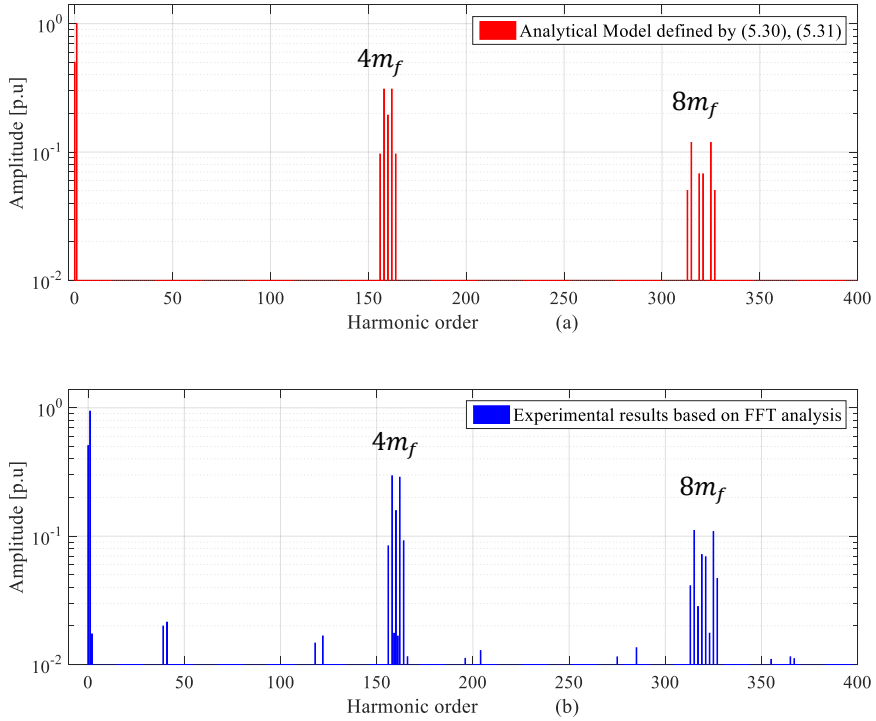


Fig 6.48 Harmonic spectrums for any arm voltage when FB-MMC operates in the boost mode at V_{dc_act}= 50V (50 of V_{dc_nom}), and $V_C = 50$ V which defined by (3.16): (a) The analytical model results, (b) FFT of the experimental results

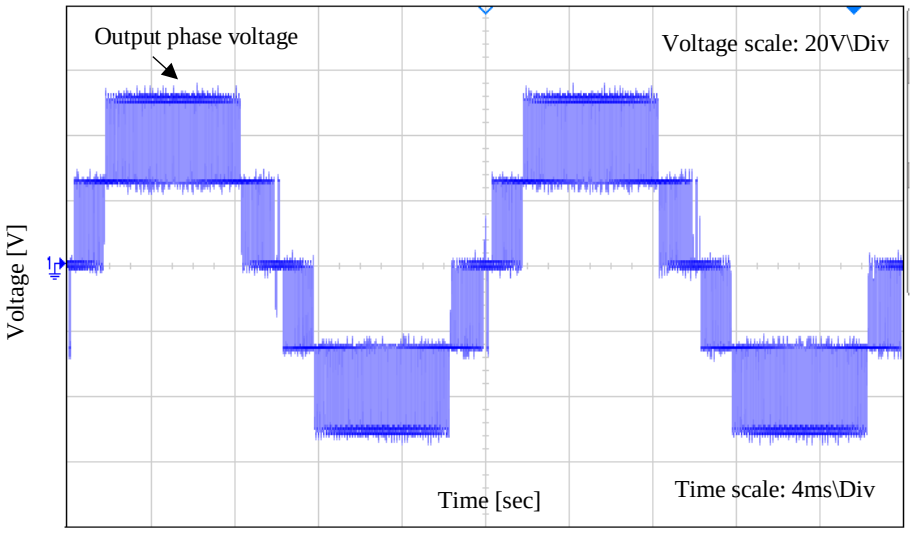


Fig 6.49 Experimental output phase voltage waveform of the FB-MMC with (N=2) when operates in the boost mode at V_{dc_act}= 50 V (50 of V_{dc_nom}), and $V_C = 50$ V which defined by (3.16)

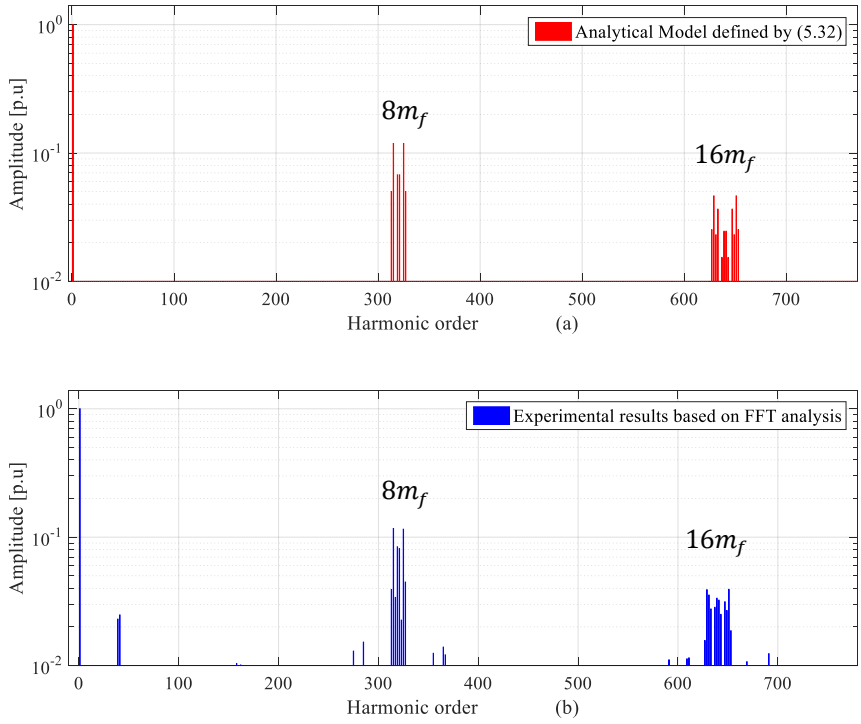


Fig 6.50 Harmonic spectrums for output phase voltage when FB-MMC operates in the boost mode at V_{dc_act}= 50 V (50 of V_{dc_nom}), and $V_C = 50\ V$ which defined by (3.16): (a) The analytical model results, (b) FFT of the experimental results

Based on the second capacitor voltage regulation as illustrated in blue in Fig 5.22 (b), it shows that better THD of the output phase voltage is obtained while the FB-MMC operating at V_{dc_act} around 33 V (33 % of V_{dc_non}). Here, the values of the modulation indexes are set to be ($M_{dc} = 0.5$ and $M_{ac} = 1.5$), that allows adjust V_C around 33 V as defined by (3.17), and to keep the amplitude of the output phase voltage $\hat{v_{ph}}$ around ($V_{dc\_nom}/2$=50 V). Considering this operating condition, the experimental output voltage waveforms of the upper and lower FB-submodules are shown in Fig 6.51. Each FB-submodule is inserted either at the positive voltage $+33$ V or the negative voltage -33 V, and the zero voltage when the submodule is bypassed. Fig 6.46 presents the analytical expression of the harmonic contents defined by (5.30). They are shown and matched to experimental results associated with FFT analysis. It can be observed that the harmonic spectrum of each FB submodule output voltage contains odd and even sideband harmonics centred around the odd carrier groups of $\{2m_f, 6m_f, .. \text{etc}\}$. For a case of the even carrier groups of $\{4m_f, 12m_f, .. \text{etc}\}$ contain of the even sideband harmonics. Otherwise, the odd sideband harmonics are centred around even carrier groups of $\{8m_f, 16m_f, .. \text{etc}\}$. Regardless of the sideband harmonic amplitudes, it can be seen that an existence of these sideband harmonic orders in the operating point defined by (3.17) is similar to those of the first operating point defined by (3.16). The experimental arm voltage waveforms are exhibited in Fig 6.52. These arm voltages are produced at three levels, as presented in Fig 6.53. Using the analytical expression defined by (5.30), results of the harmonic contents are found and verified to the experimental results as Fig 6.54. It can be observed that that harmonic carrier groups of each arm voltage achieve at $\{4m_f, 8m_f, .. \text{etc}\}$ expressed by $\{2Nm_f\}^{th}$ multiples. Similar to the first operating point, results of this operating point show that the even sideband harmonic contents exist in each odd carrier groups. While the odd sideband harmonic contents occur in each even carrier groups. Because these even sideband harmonics in the upper arm voltage have same directions to those of the lower arm voltages, these

sideband harmonic contents are eliminated in the output phase voltage. However, the output phase voltage is generated with seven voltage levels, as shown in Fig 6.55. Besides operating the FB-MMC in the boost mode, it can be revealed that output phase voltage is synthesised to more voltage levels regarding the dc capacitor voltage of the FB-submodule. Both of the analytical expression defined by (5.32) and experimental harmonic contents are compared, as shown in Fig 6.56. The harmonic carrier groups still achieve at $\{8m_f, 16m_f, ..\text{etc}\}$ if compared to those of the harmonic spectrum in Fig 6.50. It can be noted that the harmonic content amplitudes are significantly decreased because the dc capacitor voltages are regulated at the reduced value; therefore, a value of THD for the output phase voltage is reduced at this operating point.

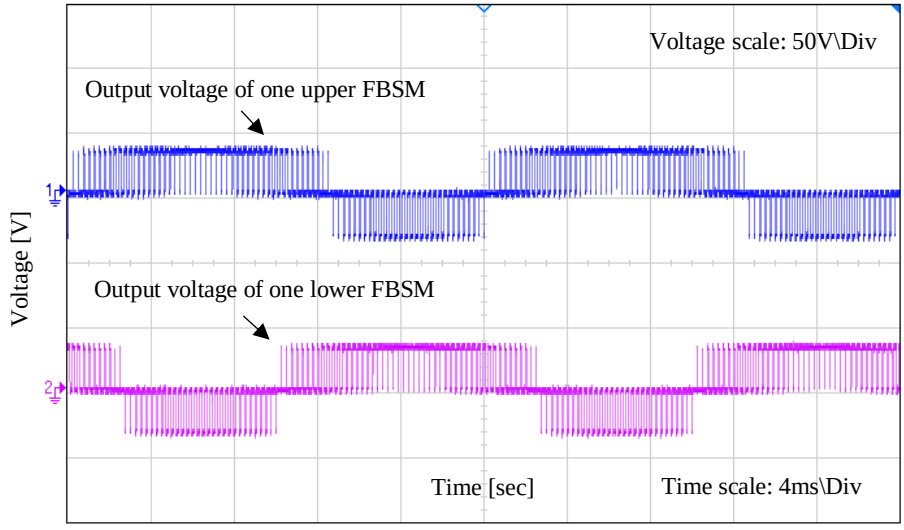


Fig 6.51 Experimental output voltage waveforms of the upper and lower FB-submodules when FB-MMC with (N=2) operates in the boost mode at V_{dc_act}= 33 V (50 of V_{dc_nom}), and $V_C = 34$ V which defined by (3.17)

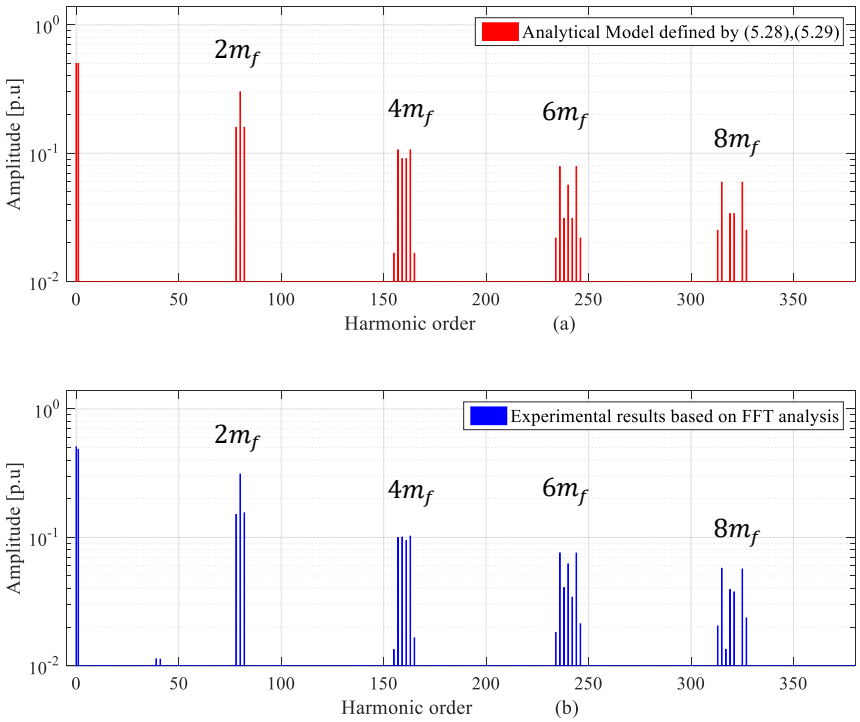


Fig 6.52 Harmonic spectrums for any FB-submodule voltage operates in the boost mode at V_{dc_act} = 33 V (50 of V_{dc_nom}), and V_C = 34 V which defined by (3.17): (a) the analytical model results, (b) FFT of the experimental results

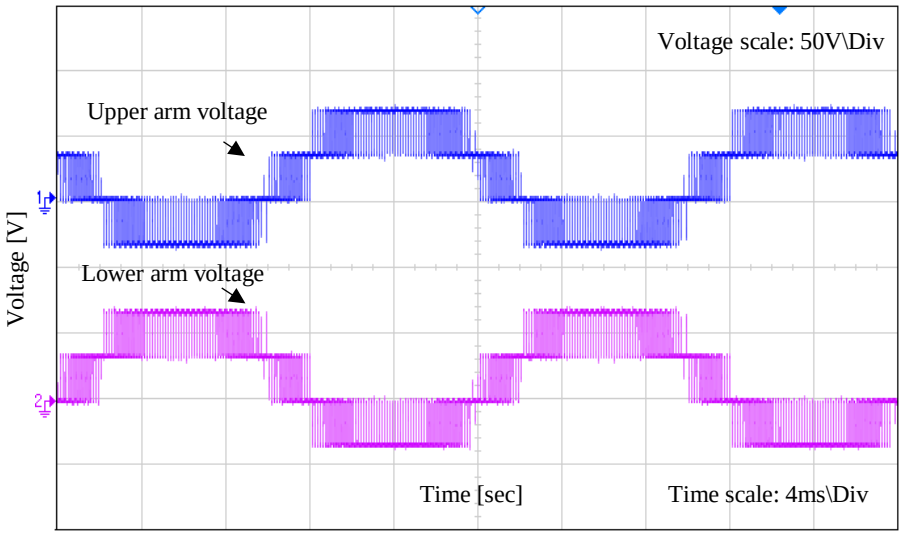


Fig 6.53 Experimental the upper and lower arm voltage waveforms of the FB-MMC with (N=2) when operates in the boost mode at V_{dc_act}= 33 V (33 of V_{dc_nom}), and V_C = 34 V which defined by (3.17)

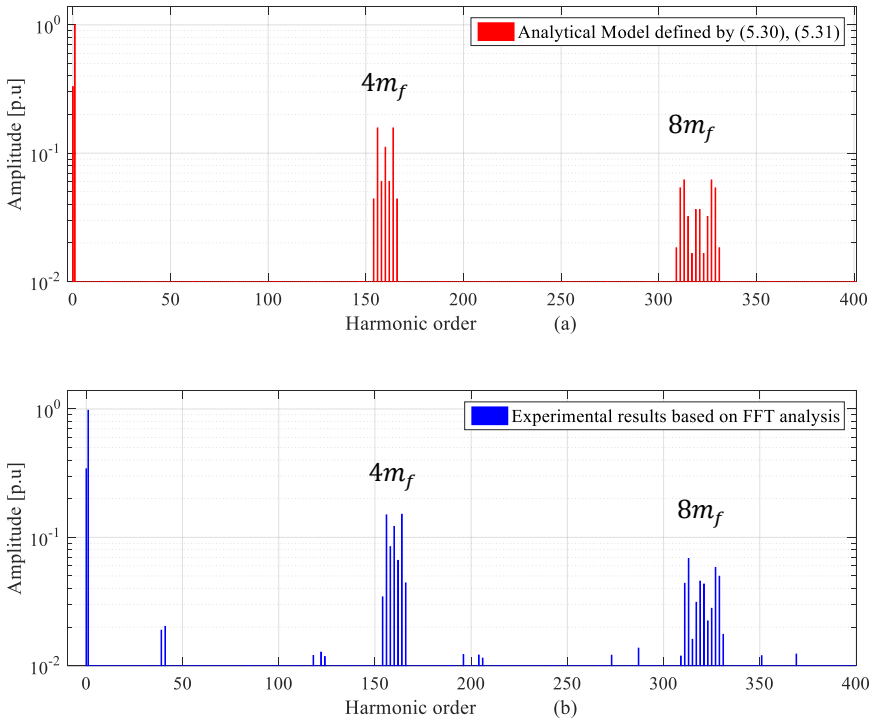


Fig 6.54 Harmonic spectrums for any arm voltage when FB-MMC operates in the boost mode at V_{dc_act}= 33 V (33 of V_{dc_nom}), and V_C = 34 V which defined by (3.17): (a) The analytical model results, (b) FFT of the experimental results

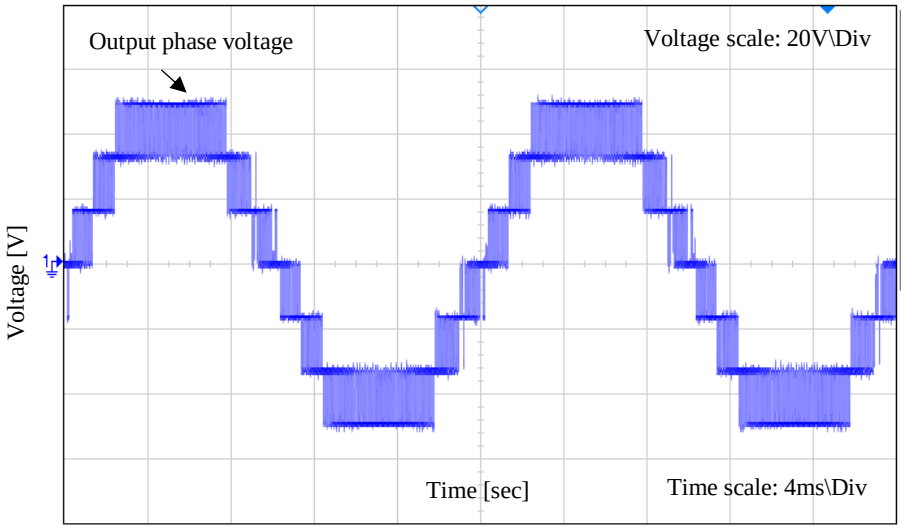


Fig 6.55 Experimental output phase voltage waveform of the FB-MMC with (N=2) when operates in the boost mode at V_{dc_act}= 33 V (33 of V_{dc_nom}), and V_C = 34 V which defined by (3.17)

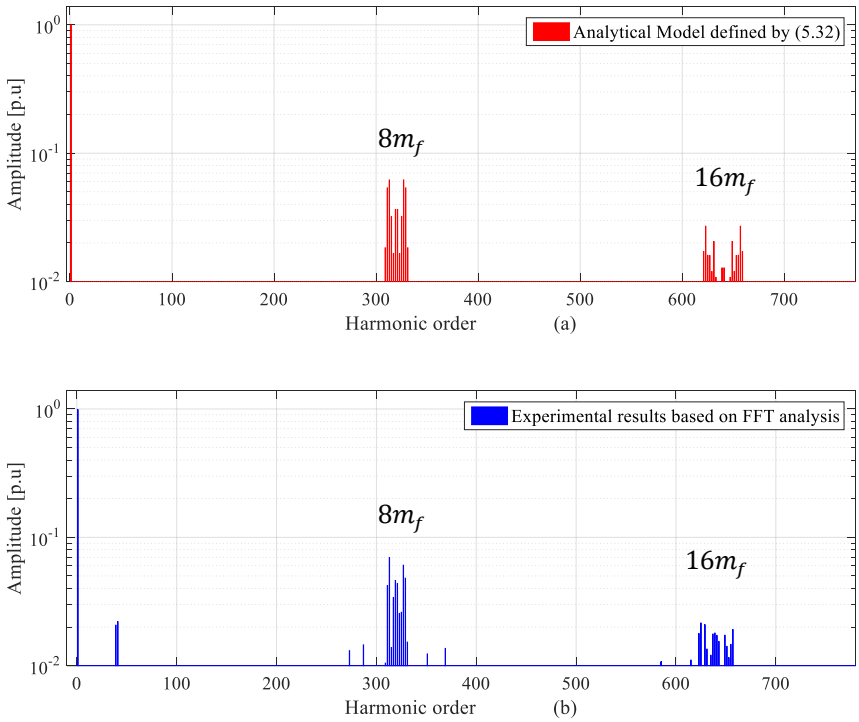


Fig 6.56 Harmonic spectrums for output phase voltage when FB-MMC operates in the boost mode at V_{dc_act}= 33 V (33 of V_{dc_nom}), and V_C = 34 V which defined by (3.17): (a) The analytical model results, (b) FFT of the experimental results

6.9 Chapter summary

The main objectives of this chapter were to prove the main findings analysed in Chapter 4 and 5. The single-phase FB-MMC inverter model was built and executed on in the real-time simulation using OPAL-RT OP4500. Using a methodology technique of the eHS solver, both FPGA and CPU cores of the real-time simulator OP4500 were employed to simulate FB-MMC and control circuit. Where the developed PSC-PWM strategy presented in Chapter 3 has been implemented using the CPU model. That is to generate PWM gating signals required. Otherwise, a virtual FB-MMC circuit was executed in the real-time using FPGA model. The CPU and FPGA models have developed in MATLAB/Simulink interfacing the RT-LAB environment. In addition, a down-scaled prototype for the single-phase FB-MMC inverter was built in this research work. The same CPU model of the OP4500

simulator was also used to obtain PWM gate signals for the prototype of the FB-MMC. By considering the steady-state analysis developed in Chapter 4, results obtained were firstly shown and compared using both the real-time simulation and experimentation, that when the FB-MMC works at buck and boost modes. To validate analytical expressions established in Chapter 5, obtained results of high order harmonic contents for the output voltage of FB-submodule, arm and output phase voltages have been proven by the experimental results of the FB-MMC prototype.

Chapter 7: Conclusions and Future Works

7.1 Conclusions

The research work of this thesis is brought to analyse a performance of the FB-MMC while operating in the buck and boost modes under variable dc link voltage. the analysis undertaken considers using the FB-MMC to interface a direct drive variable-speed WECS with the power grid, whereas a time-varying of the dc link voltage is a main technical issue that impacts on WECS integration requirements. This section summaries the literature review, the main objectives and contributions of this research work.

Chapter 1 has highlighted motivation and main objectives of the research work in this thesis that considers the implementation of the modular multilevel converter for the wind energy conversion system. The limitations of this project were also given in this chapter.

Chapter 2 has provided insight into the state of the art power converter that implemented into the direct-drive PMSG based WECS application. The emphasis was placed on considering the MMC as competitive topology in this application over other power converters. For the HB-MMC and FB-MMC modelling, Chapter 2 has also reviewed some steady-state analysis models that introduced to fully understand a characteristic of low order harmonic components in voltages and currents. Based on the different modulation strategies, the literature review in Chapter 2 has also focused on some comprehensive analyses that established to describe a behaviour of high order harmonic contents of PWM.

In Chapter 3, the main objectives were to analyse the operation of the FB-MMC in the buck and boost modes. The emphasis in this chapter was given to study an influence of the dc link level on the circulating current, capacitor voltage ripples and THD of the phase output voltage, in which the dc link voltage varies in the range of [0-V_{dc_nom}]. In order to achieve this, the single-phase FB-MMC switching simulated

model was first implemented using open-loop mode to validate the effectiveness of PSC-PWM strategy under these operating conditions. Then this simulated model has been extended to the three-phase system while connected to the grid. Two closed-loop control circuits have also been designed for the grid connected FB-MMC. The first control circuit is used to achieve the output active and reactive powers while the second is to minimise the 2^{nd} harmonic circulating current and to regulate dc capacitor voltage of the FB-submodules. Of note that two different regulation approaches for the FB-submodule capacitor voltages were analysed and compared. The first approach is regulated at the nominal value defined by the grid voltage. Otherwise, the second approach regulates the dc capacitor voltage according to the variations in the dc link voltage

The main contributions achieved in Chapter 3 are summarised as follows: the PSC- PWM strategy is first developed through determining of the ac and dc modulation indexes that are used to specify operating in the buck and boost modes. Besides, the two closed-loop control circuits are optimised depending on the synchronous sampling technique.

The obtained results revealed that the 2^{nd} order circulating current is minimized without using the circulating current suppression control, in which the FB-MMC operates in the boost mode at 60% of the nominal dc link voltage, and consequently, of a decrease in the capacitor voltage ripples. For design consideration, the research work regards the operation at this dc link voltage level as an optimal operating point in terms of the minimum the circulating current and capacitor ripples, that obtained from the performance analysis of the FB-MMC in the boost mode. Hence, it gives a possibility to considerably reduce the capacitor size if the dc link voltage level is maintained at this optimal operating point. In addition, the operating in the boost mode exposed that different resonant inductances are obtained in accordance with the dc voltage levels.

Moreover, the obtained results showed that in the lower range of the dc link voltage, the circulating current and capacitor voltage ripples are decreased by

operating the system at a low power factor. It also showed that THD of the output voltage is highly dependent on the level of the dc link voltage when the FB-MMC operates in the boost mode due to the interleaving effect.

The performance analysis of the FB-MMC in the buck and boost operating modes was verified through results obtained from both single-phase and three-phase switching simulated models.

The main contribution in Chapter 4 is that the steady-state analytical model is developed to be valid for the grid connected FB-MMC in the boost mode. Based on the classical circular interaction, analytical expressions are established to describe how the dc link voltage level influences low order harmonic components in the arm currents, submodule capacitor currents, submodule capacitor voltages, submodule output voltages, arm voltages, and output voltage of FB-MMC. Dependencies of capacitor voltage ripples and the 2nd harmonic circulating current are revealed while the FB-MMC works in the boost mode, as they are represented in both dc and ac modulation indexes which influenced of the dc link voltage level. In addition, analytical expressions for amplitude and phase angle of the 2nd order harmonic circulating current are developed to be valid within these operating conditions.Thus, the resonant inductance formula is developed for the boost operating mode.

By setting different levels of the dc link voltage, the obtained results of the developed steady-state analytical model are validated to those of the single-phase switching simulated model.

The main contribution in Chapter 5 of this research work is the development of comprehensive analytical modelling to identify high order harmonic contents of PWM voltage waveforms on the FB-MMC, which operates in the boost under varying dc link voltage that covering the range of [0-V_{dc_nom}]. Based on the PSC-PWM strategy developed in this research work, PWM voltage waveforms are modulated by the double edge naturally sampled PWM. This analysis undertaken is established using a methodology of the double Fourier series expansion in two time variables. The results obtained by developed analytical expressions for the

submodule leg voltages, FB submodule output voltage, arm voltages and output phase voltage revealed that high order harmonic contents in the boost mode are influenced by the dc link voltage level, whereas these analytical expressions to identify harmonic contents are derived regarding the dc and ac modulation indexes.

By considering the two dc voltage capacitor regulation approaches and the impact of the displacement angle. The obtained results showed that the behaviour of THD of the output voltage is exposed to nonlinearity regarding different operating points of the dc link voltage in the buck and boost modes. This research work proposes optimal operating points of the dc link voltage level in terms of better THD of the output voltage can be obtained. This research work revealed that these optimal operating points are relevant to the number of FB-submodules of each arm, capacitor voltage regulation approaches and the impact of the displacement angle.

The results obtained from developing the comprehensive analytical modelling in the boost mode are verified by a comparison with FFT analysis of those resulting from the simplified simulated switching model of the FB-MMC.

In Chapter 6, the major objective was set to prove the main findings analysed in Chapter 4 and 5. The single-phase FB-MMC inverter model was first built and executed on in the real-time simulation using OPAL-RT OP4500. Using a methodology technique of the eHS solver, both FPGA and CPU cores of the real-time simulator OP4500 were employed to simulate FB-MMC and control circuit. The PSC-PWM strategy developed in Chapter 3 has been implemented using the CPU model. That is to generate PWM gating signals required. Otherwise, a virtual FB-MMC circuit was executed in the real-time using FPGA model. The CPU and FPGA models have developed in MATLAB/Simulink interfacing the RT-LAB environment.

Moreover, a down-scaled prototype for the single-phase FB-MMC inverter was built in this research work. The same CPU model of the OP4500 simulator was also used to obtain PWM gate signals for the prototype of the FB-MMC.

The main contribution in Chapter 6 is that results obtained from for the buck and boost operating modes of the FB-MMC are studied and compared using both the real-time simulation and experimentation. These results of low harmonic ripples of the FB-MMC are analysed that considers the steady-state analysis developed in Chapter 4. In addition, the results obtained from the analytical expressions established in Chapter 5 to identify high order harmonic contents are validated with the FFT analysis of the experimental results of the FB-MMC prototype. This validation is achieved on the harmonic contents for the output voltage of FB-submodule, arm and output phase voltages.

7.2 Future works

Future works consider further investigations that can be made to analyze the operation of the grid connected FB-MMC for WECS. Some suggestions and ideas can be given as follows

- By taking into account the main contributions of this research work, the FB-MMC parameters can be designed with lower cost-effective when the dc link voltage level is fixed in the boost mode at the proposed optimal operating point, which is 60% of its nominal value. In this case, the performance analysis shows minimization in the capacitor voltage ripples due to the decrease in the 2^{nd} order harmonic circulating current. Thus the analysis of the research work can be exploited to reduce the FB-submodule capacitor size, as the capacitor voltage ripple is lowered. Therefore, this research work would suggest that the switching model of the FB-MMC that used in Chapter can be designed using the FB-submodule capacitor value of 0.5 mF and 0.25 mF, instead of 2 mF. Further improvement can be obtained at this optimal operating point that when the capacitor voltage regulation approach defined by (3.17) is applied. As shown the output voltage is produced in eleven levels, that regards 2N+3, with achieving

better THD. Also, the voltage across each submodule capacitor is reduced to 80 % of its nominal value, as compared to this defined by (3.16).

- For the three-phase grid connected FB-MMC under variable dc link voltage, a capacitor voltage balancing control that considers a sort and select algorithm can be implemented into a further investigation. In this case, each output voltage of the FB-submodule in the boost mode is generated in the positive and negative states. This point can be more beneficial to improve the sort and select algorithm, as these states can be exploited to reverse the capacitor current independently of the arm current direction. Therefore overcharge and discharge voltages of the FB-submodule capacitor can be avoided in a fast rate process. An impact of the sampling frequency, which are used for measuring signals of all capacitor voltages and the upper and lower arm currents, on the capacitor voltage balancing control can also be studied.

- In order to improve the developed steady-state analysis presented in Chapter 4, it can be extended by considering the effect of the 2^{nd} harmonic circulating current control. Based on the closed-loop analysis, a reference voltage of the 2^{nd} harmonic component can be calculated at different operating points of the FB-MMC in the buck and boost modes and then employed for an injection of the 2^{nd} harmonic circulating current.

- As the comprehensive analysis proposed in Chapter 5 is analysed depending on the double edge naturally sampled PWM, the harmonic contents can be identified by using double edge symmetrical and asymmetrical regular sampled PWM. A comparative study of three regular sampled PWM techniques can be investigated to evaluate the THD of output phase voltage. In addition, a dead-time error voltage can be taken into consideration of this PWM harmonic analysis.

Appendices

The appendices of this research work are brought to show more details of the simulated circuits of the FB-MMC that built-in MATLAB\Simulink environments. They present a switching model layout that includes the M-files to initialize their parameters. For the implementation of the proposed analytical expressions, the M-file based model codes are also listed in these appendices.

Appendix A Implementing the switching model of the FB-MMC

The switching model of the FB-MMC illustrated in Fig 3.1 is built-in MATAB\Simulink environment, as shown in Fig A.1. Where the circuit configuration of the switching model is based on the single-phase system. This simulation model operates in open-loop mode in which the modulation indexes M_{dc} and M_{ac} are adjusted through M-file that used to initialize model parameters. The M-file code is listed as follows:

```
clc; close all;
Ts=1e-6;                % Simulation step time
Fs=1000;                % Switching frequency
f=50;                   % Nominal frequency
w=2*pi*f;               % Angular frequency
N=4;                    % No. of FB-SM
PF=0.99                 % Power factor - Desired value
Vdc_nom=10000;          % Nominal value of the dc link voltage
Vm =Vdc_nom/2;          % Max.amplitude of the output phase voltage
D=0.6                   % The decrease in the dc link voltage
Vdc_act=D*Vdc_nom;      % Actual value of the dc link voltage

Vc_ref=Vdc_nom/N;       % The 1st capacitor voltage regulation defined by (3.16)
% or% Vc_ref=(Vph_nom+Vdc_act/2)/N; % The 2nd capacitor voltage regulation defined
by (3.17)

% Modulation Indexed
Mdc=Vdc_act/(N*Vc_ref);
Mac=(Vdc_nom/2/N)/(Vc_ref/2);

C=2e-3;                         % FB-SM capacitance value
Larm=3e-3;                      % Arm inductance value
Rarm=0.05;                      % Arm resistance value
Q1=0;Q2=45;Q3=90;Q4=135;        % Phase shifted carriers
Qd=0;                           % Displacement angle
% When the FB-MMC connected to Load %
```

```
Vph= Vm/sqrt(2);                % the output phase voltage in R.M.S
Iph=105;                        % Desired output current in RMS
Im=sqrt(2)*Iph;
Q=acos(PF);                     % Output current angle
% Calculate the load value to obtain desired Iph and PF
Pload=Vph*Iph*(cos(Q));         % The active power
Rload=Pload/(Iph^2);
Zload=Vph /Iph;
Xload=sqrt(Zload^2-Rload^2);
Lload=Xload/(100*pi);
Vc0=Vdc_nom/N;                  % Initial value of the capacitor voltage
% Snubber circuit parameters
Ron=1e-4;Rs=1e5;Cs=inf;
```

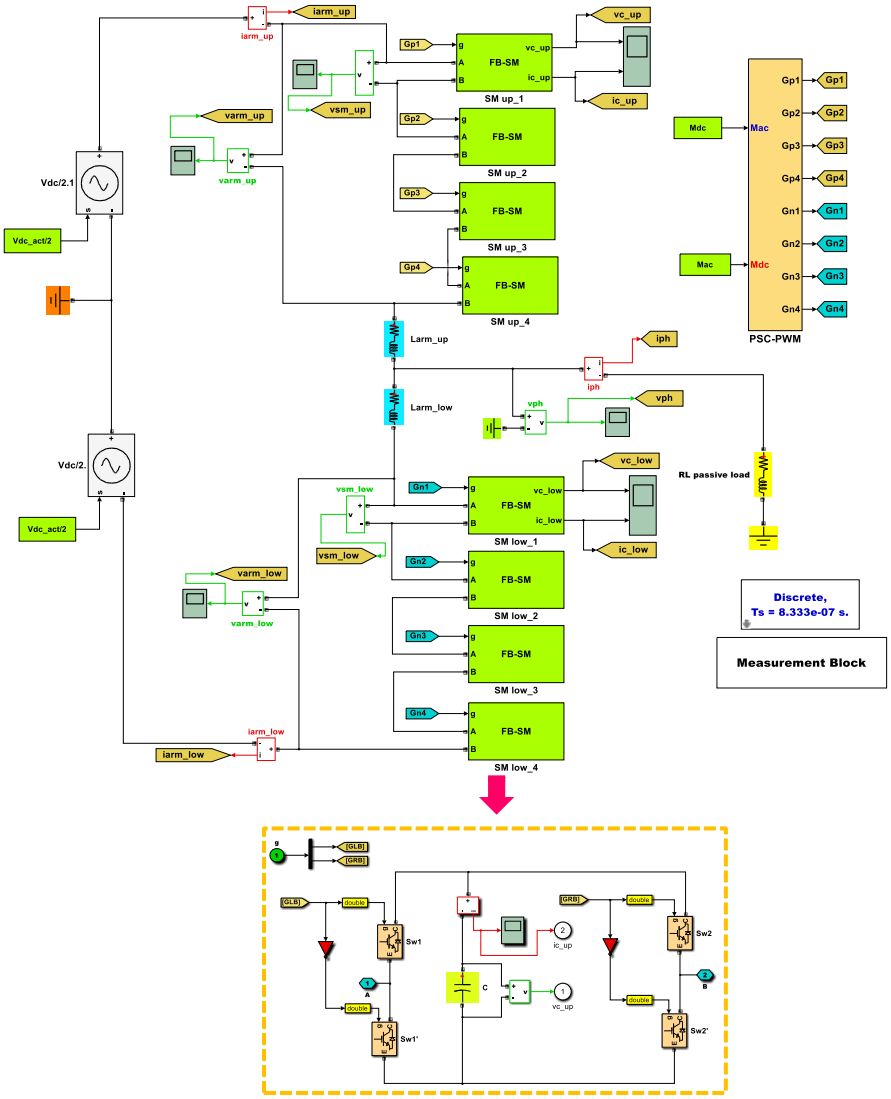


Fig A.1 Model configuration of the single phase FB-MMC in MATLAB\Simulink

Moreover, the layout circuit to generate PWM gate signals of the FB-MMC switching model is illustrated in Fig A.2. This circuit considers the developed PSC-PWM strategy presented in section 3.3.2.

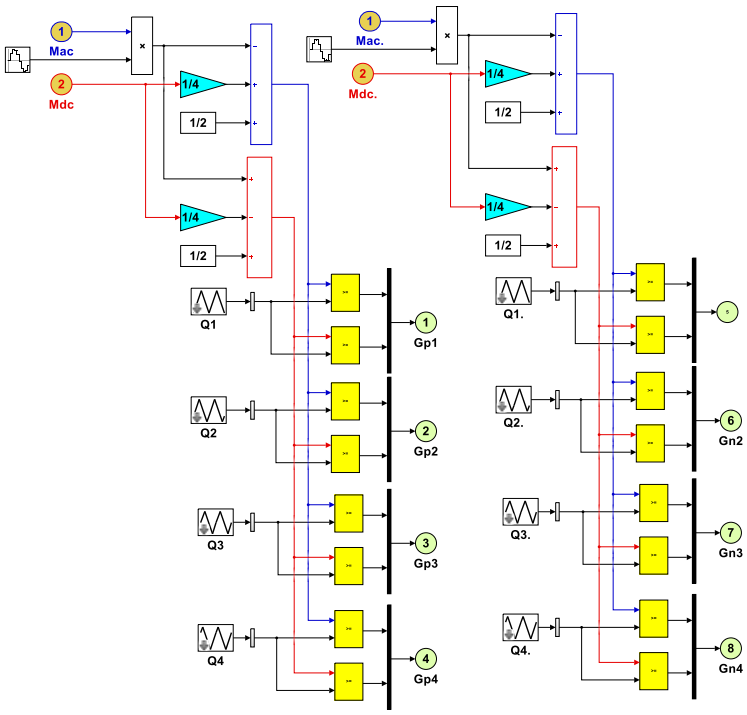


Fig A.2 Layout circuit of the PSC-PWM circuit in MATLAB\Simulink

Appendix A.1 Selection of the submodule capacitor and arm inductor

To improve the dynamic performance and efficiency of the modular multilevel converter, a parameter design of the submodule capacitor C_{SM} and the arm inductor L_{arm} are required. The submodule capacitor is determined by compromising between the voltage requirement and size of the submodule capacitor. In terms of an energy-power ratio EP, the submodule capacitor value can be obtained from the following equations [90]:

$$C_{SM} = \frac{EP\ N\ S_n}{3\left(\frac{V_C}{N}\right)^2} \tag{A.1}$$

Where the energy-power ratio EP represents maximum total energy stored in submodule capacitors regarding apparent power S_n. In this work, the EP is chosen as 140 Joul/KVA [108]. By using other parameter values of $N = 4, V_C = 2.5$ kV, S_n=1MVA, the submodule capacitor value is calculated as $C_{SM} = 2\ m$F. For the grid connected FB-MMC, the arm inductance value L_{arm} has to be chosen a few times higher than the resonant inductance value L_r [68]. The resonant inductance L_r defined by (4.24) [67] is about 2.1 mH. The simulation results of the FB-MMC switching model shows that the circulating current in RMS value increases as the arm inductance L_{arm} nears to a resonant inductance L_r as shown in Fig A.3

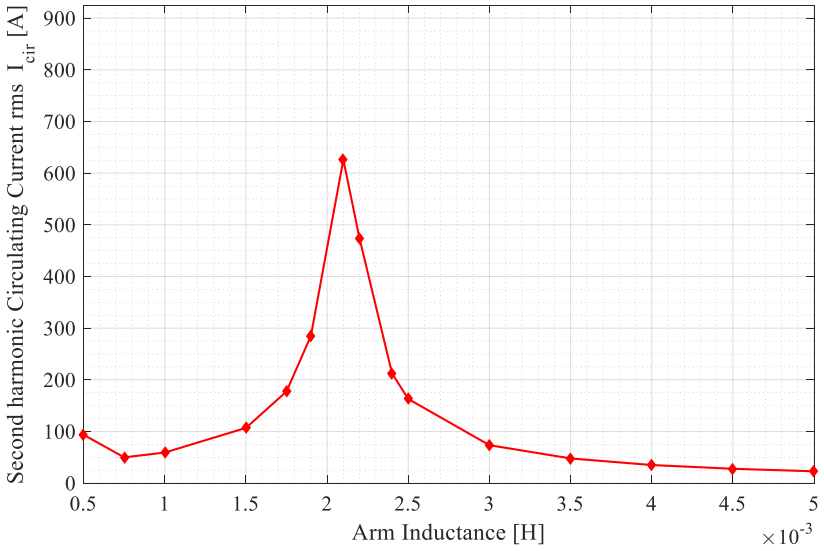


Fig A.3 Circulating current versus different arm inductances C_{sm} is 2 mF

In this work, the arm inductance value L_{arm} is selected to be 3 mH.

Appendix B Implementing the steady-state analytical model of FB-MMC

In the steady-state analysis presented in Chapter 4, the analytical expressions derived for voltage and current quantities of the FB-MMC are implemented and simulated using MATLAB\M-files environment. The obtained results are validated by a comparison with those of the switching model presented in Appendix A The MATLAB\M-files code is given as follows

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%        The Analytical Model of the FB-MMC        %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%


clc;close all;
TT=1;                            %Simulation time
Ts=1e-6;                         %Simulation time step
w=100*pi;C=2e-3;L=3e-3;N=4;  %Simulation parameters
dc_nom=10000;               %Nominal value of the dc link voltage
D=0.6                       %The decrease in the dc link voltage
Vdc_act=D*Vdc_nom;          %Actual value of the dc link voltage

%The 1st capacitor voltage regulation defined by (3.16)
Vc_ref=Vdc_nom/N;
%The 2nd capacitor voltage regulation defined by (3.17)
Vc_ref=(Vdc_nom+Vdc_act)/(2*N)-10;

% Modulation indexes
Mdc=Vdc_act/(N*Vc_ref);
Mac=(Vdc_nom/2/N)/(Vc_ref/2);

%%%%%%%%%%%%%%%%%%%%%%%
% Circulating Current %
%%%%%%%%%%%%%%%%%%%%%%%

% Calculation of the amplitude of output phase current
Iph=105;
PF=0.999;
Im= Iph *sqrt(2);
Q=acos(PF);
t=0:Ts:TT;
t=t';
iph_a=Im*sin(w*t+Q);

% Calculation of the dc component current
Idc=Mac*PF*Im/4/Mdc;

% Calculation of the 2nd circulating current
A=3*Mac*Mdc*N*Im/(64*w^2*C*L);
B=-Mac^2*N*Idc/(16*w^2*C*L);
D=Mdc^2*N/(16*w^2*C*L);
E=Mac^2*N/(24*w^2*C*L);
Icir=sqrt((A*cos(Q)+B)^2+(A*sin(Q))^2)/(1-D-E)
y=A*cos(Q)+B;
x=-A*sin(Q);
Qcir=180/pi*atan2(y,x);

if Qcir>=0;
   Qcir=180-180/pi*atan2(y,x);
   Qcir=pi/180*Qcir;
else
   Qcir=-(180+Qcir);
   Qcir=pi/180*Qcir;
end
```

```
icc_a=Icir*sin(2*w*t+Qcir)+Idc;

figure(1);
plot(Time,icc,'-r','LineWidth',1.75);hold on;
plot(Time,icc_a,'-b','LineWidth',1.75);hold off;
xlabel('Time [sec]','fontsize',22,'fontweight','normal');
ylabel('Current [A]','fontsize',22,'fontweight','normal');
leg = legend('Switching Model','Analytical Model');
set(leg,'FontSize',13);
set(gca,'FontSize',16,'FontName','Times New
Roman','fontweight','normal');
set(gca,'xLim',[0.96 1]);
set(gca,'yLim',[-100 225]);
set(gca,'xTick',[0.96 0.97 0.98 0.99 1])
set(gca,'yTick',[-100 -50 0 50 100 150 200])
grid on;grid minor;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Upper and Lower arm currents %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

figure(2);
subplot(2,1,1)
iarm_up_a=iph_a/2+icir_a;
iarm_low_a=-iph_a/2+icir_a;

plot(Time,iarm_up,'color',[1 0 0],'LineWidth',2);hold on;
plot(Time,iarm_up_a,'color',[0 0 1],'LineWidth',2);hold off;

xlabel('Time [sec] (a)','fontsize',22,'fontweight','normal');
ylabel('Current [A]','fontsize',22,'fontweight','bold');
leg = legend('Switching Model','Analytical Model');
set(leg,'FontSize',13);
set(gca,'FontSize',16,'FontName','Times New
Roman','fontweight','normal');
set(gca,'xLim',[0.94 1]);
set(gca,'yLim',[-200 350]);
set(gca,'xTick',[0.94 0.95 0.96 0.97 0.98 0.99 1]);
set(gca,'yTick',[-200 -100 0 100 200]);
grid on;grid minor;

subplot(2,1,2)
plot(Time,iarm_up,'color',[0.3 0.6 0],'LineWidth',2);hold on;
plot(Time,iarm_low_a,'color',[0.8 0.3 0],'LineWidth',2);hold
off;

xlabel('Time [sec] (b)','fontsize',22,'fontweight','normal');
ylabel('Current [A]','fontsize',22,'fontweight','bold');
leg = legend('Switching Model','Analytical Model');
set(leg,'FontSize',13);
set(gca,'FontSize',16,'FontName','Times New
Roman','fontweight','normal');
set(gca,'xLim',[0.94 1]);
set(gca,'yLim',[-200 355]);
set(gca,'xTick',[0.94 0.95 0.96 0.97 0.98 0.99 1]);
set(gca,'yTick',[-200 -100 0 100 200]);
```

```
grid on;grid minor;


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Capacitor current in the upper and lower arm FB-SM %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

figure(3);

ic_up_a1=-Mac*Idc/2*sin(w*t)+Mdc*Im/4*sin(w*t-Q)....
-Mac*Icc/4*cos(w*t+Qcir);
ic_up_a2=Mac*Im/8*cos(2*w*t-Q)+Mdc*Icir/2*sin(2*w*t+Qcir);
ic_up_a3=Mac*Icir/4*cos(3*w*t+Qcir);

ic_up_a=ic_up_a1+ic_up_a2+ic_up_a3;
ic_low_a=-ic_up_a1+ic_up_a2-ic_up_a3;

subplot(2,1,1);

plot(Time,ic_up,'color',[1 0 0],'LineWidth',1);hold on;
plot(Time,ic_up_a,'color',[0 0 1],'LineWidth',1.5);hold off;

xlabel('Time [sec] (a)','fontsize',22,'fontweight','normal');
ylabel('Current [A]','fontsize',22,'fontweight','bold');
leg = legend('Switching Model','Analytical Model');
set(leg,'FontSize',13);
set(gca,'FontSize',16,'FontName','Times New
Roman','fontweight','normal');
set(gca,'xLim',[0.94 1]);
set(gca,'yLim',[-200 350]);
set(gca,'xTick',[0.94 0.95 0.96 0.97 0.98 0.99 1]);
set(gca,'yTick',[-200 -100 0 100 200]);
grid on;grid minor;

subplot(2,1,2)

plot(Time,ic_low,'color',[0.3 0.6 0],'LineWidth',1);hold on;
plot(Time,ic_low_a,'color',[0.8 0.1 0],'LineWidth',1.5);hold
off;
xlabel('Time [sec] (b)','fontsize',22,'fontweight','normal');
ylabel('Current [A]','fontsize',22,'fontweight','bold');
leg = legend('Switching Model','Analytical Model');
set(leg,'FontSize',13);
set(gca,'FontSize',16,'FontName','Times New
Roman','fontweight','normal');
set(gca,'xLim',[0.94 1]);
set(gca,'yLim',[-200 355]);
set(gca,'xTick',[0.94 0.95 0.96 0.97 0.98 0.99 1]);
set(gca,'yTick',[-200 -100 0 100 200]);
grid on;grid minor;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Capacitor voltage in the upper and lower arm FB-SM  %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

figure(4);
```

```
vc_up_a1=1/(w*C)*(Mac*Idc/2*cos(w*t)-Mdc*Im/4*cos(w*t-Q) ...
         -Mac*Icir/4*sin(w*t+Qcir));

vc_up_a2=1/(w*C)*(Mac*Im/16*sin(2*w*t-Q) ...
         -Mdc*Icir/4*cos(2*w*t+Qcir));

vc_up_a3=1/(w*C)*(Mac*Icir/12*sin(3*w*t+Qcir));

vc_up_a= (Vc_ref+vc_up_a1+vc_up_a2+vc_up_a3);
vc_low_a= (Vc_ref-vc_up_a1+vc_up_a2-vc_up_a3);

subplot(2,1,1);

plot(Time,vc_up,'color',[1 0 0],'LineWidth',1.5);hold on;
plot(Time,vc_low_a,'color',[0 0 1],'LineWidth',1.5);hold off;

xlabel('Time [sec] (a)','fontsize',22,'fontweight','normal');
ylabel('Voltage [V]','fontsize',22,'fontweight','normal');
leg =legend('Switching Model','Analytical Model');
set(leg,'FontSize',13);
set(gca,'FontSize',16,'FontName','Times New
Roman','fontweight','normal');
set(gca,'xLim',[0.94 1]);
set(gca,'yLim',[2350 2750]);
set(gca,'xTick',[0.94 0.95 0.96 0.97 0.98 0.99 1]);
grid on;grid minor;

subplot(2,1,2);
plot(Time,Vc_low,'color',[0.3 0.6 0],'LineWidth',2);hold on;
plot(Time,Vc_low_a,'color',[0.8 0.1 0],'LineWidth',2);hold
off;

xlabel('Time [sec](b)','fontsize',22,'fontweight','normal');
ylabel('Voltage [V]','fontsize',22,'fontweight','normal');
leg =legend('Switching Model','Analytical Model');
set(leg,'FontSize',13);
set(gca,'FontSize',16,'FontName','Times New
Roman','fontweight','normal');
set(gca,'xLim',[0.94 1]);
set(gca,'yLim',[2350 2750]);
set(gca,'xTick',[0.94 0.95 0.96 0.97 0.98 0.99 1]);
grid on;grid minor;


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%  The output voltage of FB-SM in upper and lower arm %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%


figure(5);

vsm_up_a0=Mdc/2*Vc_ref...
          +Mac^2*Idc/(8*w*C)*sin(-Q)...
          -Mac*Mdc*Im/(16*w*C)*sin(-Q)...
          +Mac^2*Icir/(16*w*C)*cos(Qcir);
```

```
vsm_up_a1=-Mac/2*Vc_ref*sin(w*t)....
          +Mdc*Mac*Idc/(4*w*C)*cos(w*t)...
          -Mdc^2*Im/(8*w*C)*cos(w*t-Q)...
          -Mac^2*Im/(64*w*C)*cos(w*t-Q)...
          -3*Mdc*Mac*Icir/(16*w*C)*sin(w*t+Qcir);

vsm_up_a2=-Mac^2*Idc/(8*w*C)*sin(2*w*t)...
          +Mdc*Mac*Im/(16*w*C)*sin(2*w*t-Q)...
          +Mac^2*Icir/(16*w*C)*cos(2*w*t+Qcir)...
          +Mdc*Mac*Im/(32*w*C)*sin(2*w*t-Q)...
          -Mdc^2*Icc/(8*w*C)*cos(2*w*t+Qcir)...
          -Mac^2*Icc/(48*w*C)*cos(2*w*t+Qcir);

vsm_up_a3=Mac^2*Im/(64*w*C)*cos(3*w*t-Q)...
          +5*Mac*Mdc*Icir/(48*w*C)*sin(3*w*t+Qcir);

vsm_up_a4=Mac^2*Icir/(48*w*C)*cos(4*w*t+Qcir);

vsm_up_a=(vsm_up_a0+vsm_up_a1+vsm_up_a2+vsm_up_a3+vsm_up_a4);
vsm_low_a=(vsm_up_a0-vsm_up_a1+vsm_up_a2-vsm_up_a3 ...
           +vsm_up_a4);

subplot(2,1,1);

plot(Time,vsm_up,'color',[1 0 0],'LineWidth',0.5);hold on;
plot(Time,vsm_up_a,'color',[0 0 1],'LineWidth',1.5);hold off;

xlabel('Time [sec] (a)','fontsize',22,'fontweight','normal');
ylabel('Voltage [V]','fontsize',22,'fontweight','normal');
leg =legend('Switching Model','Analytical Model');
set(leg,'FontSize',13);
set(gca,'FontSize',16,'FontName','Times New
Roman','fontweight','normal');
set(gca,'xLim',[0.94 1]);
set(gca,'yLim',[-200 4000]);
set(gca,'xTick',[0.94 0.95 0.96 0.97 0.98 0.99 1]);
set(gca,'yTick',[0 1000 2000 3000 4000]);
grid on;grid minor;

subplot(2,1,2);

plot(Time,vsm_low,'color',[0.3 0.6 0],'LineWidth',0.5);hold
on;
plot(Time,vsm_low_a,'color',[0.8 0.1 0],'LineWidth',1.5);hold
off;
xlabel('Time [sec] (b)','fontsize',22,'fontweight','normal');
ylabel('Voltage [V]','fontsize',22,'fontweight','normal');
leg =legend('Switching Model','Analytical Model');
set(leg,'FontSize',13);
set(gca,'FontSize',16,'FontName','Times New
Roman','fontweight','normal');
set(gca,'xLim',[0.94 1]);
set(gca,'yLim',[-200 4000]);
set(gca,'xTick',[0.94 0.95 0.96 0.97 0.98 0.99 1]);
set(gca,'yTick',[0 1000 2000 3000 4000]);
```

```
grid on;grid minor;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% The upper and lower arm voltage %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

figure(6);
varm_up_a=N*(vsm_up_a0+vsm_up_a1+vsm_up_a2+vsm_up_a3 ...
          +vsm_up_a4);
varm_low_a=N*(vsm_up_a0-vsm_up_a1+vsm_up_a2-vsm_up_a3 ...
           +vsm_up_a4);

subplot(2,1,1);

plot(Time,Vpa,'color',[1 0 0],'LineWidth',0.25);hold on;
plot(Time,Vp,'color',[0 0 1],'LineWidth',1.5);hold off;

xlabel('Time [sec]
(a)','fontsize',22,'fontweight','normal');
ylabel('Voltage [V]','fontsize',22,'fontweight','normal');
leg = legend('Switching Model','Analytical Model');
set(leg,'FontSize',13);
set(gca,'FontSize',16,'FontName','Times New
Roman','fontweight','normal');
set(gca,'xLim',[0.94 1]);
set(gca,'yLim',[-500 15000]);
set(gca,'xTick',[0.94 0.95 0.96 0.97 0.98 0.99 1]);
set(gca,'yTick',[0 2500 5000 7500 10000]);
grid on;grid minor;

subplot(2,1,2);

plot(Time,Vna,'color',[0.3 0.6 0],'LineWidth',0.25);hold on;
plot(Time,Vn,'color',[0.8 0.1 0],'LineWidth',1.5);hold
off;grid on;

xlabel('Time [sec]
(b)','fontsize',22,'fontweight','normal');
ylabel('Voltage [V]','fontsize',22,'fontweight','normal');
leg = legend('Switching Model','Analytical Model');
set(leg,'FontSize',13);
set(gca,'FontSize',16,'FontName','Times New
Roman','fontweight','normal');
set(gca,'xLim',[0.94 1]);
set(gca,'yLim',[-500 15000]);
set(gca,'xTick',[0.94 0.95 0.96 0.97 0.98 0.99 1]);
set(gca,'yTick',[0 2500 5000 7500 10000]);
grid on;grid minor;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% The output phase voltage %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

figure(7);
```

```
vph_a=(varm_up_a-varm_up_a)/2;

plot(Time,vph,'color',[1 0 0],'LineWidth',0.25);hold on;
plot(Time,vph_a,'color',[0 0 1],'LineWidth',2);hold off;

xlabel('Time [sec]','fontsize',22,'fontweight','normal');
ylabel('Voltage [V]','fontsize',22,'fontweight','normal');
leg = legend('Switching Model','Analytical Model');
set(leg,'FontSize',13);
set(gca,'FontSize',16,'FontName','Times New
Roman','fontweight','normal');
set(gca,'xLim',[0.94 1]);
set(gca,'yLim',[-6000 10000]);
set(gca,'xTick',[0.94 0.95 0.96 0.97 0.98 0.99 1]);
set(gca,'yTick',[-7500 -5000 -2500 0 2500 5000 7500]);

 grid on;grid minor;
```

Appendix C Implementing of the switching model of the grid connected FB-MMC

The switching model of the grid connected FB-MMC presented in Fig 3.6 is built-in MATAB\Simulink environment as illustrated Fig A.4 Based on three-phase system, this switching model is designed to operate under fixed and variable dc link voltage. Design of the control circuits of the FB-MMC switching model is built according to the synchronous sampling technique presented in section 3.5.1. This technique is used to synchronize the control circuits with the PSC-PWM interrupt (sampling start signals). As illustrated in Fig A.5 and Fig A.6, the PWM interrupt is generated at every upper and lower peak of all triangle carriers. In this case, the sampling frequency is $1/T_{samp} = 1/8$ kHz. However, if the crossing points of two adjacent carriers are taken as additional PWM interrupt, the sampling frequency is $1/T_{samp} = 1/16$ kHz. This synchronous sampling technique allows removing these switching ripples from feedback measured output current signals as shown in Fig A.7 and Fig A.8.

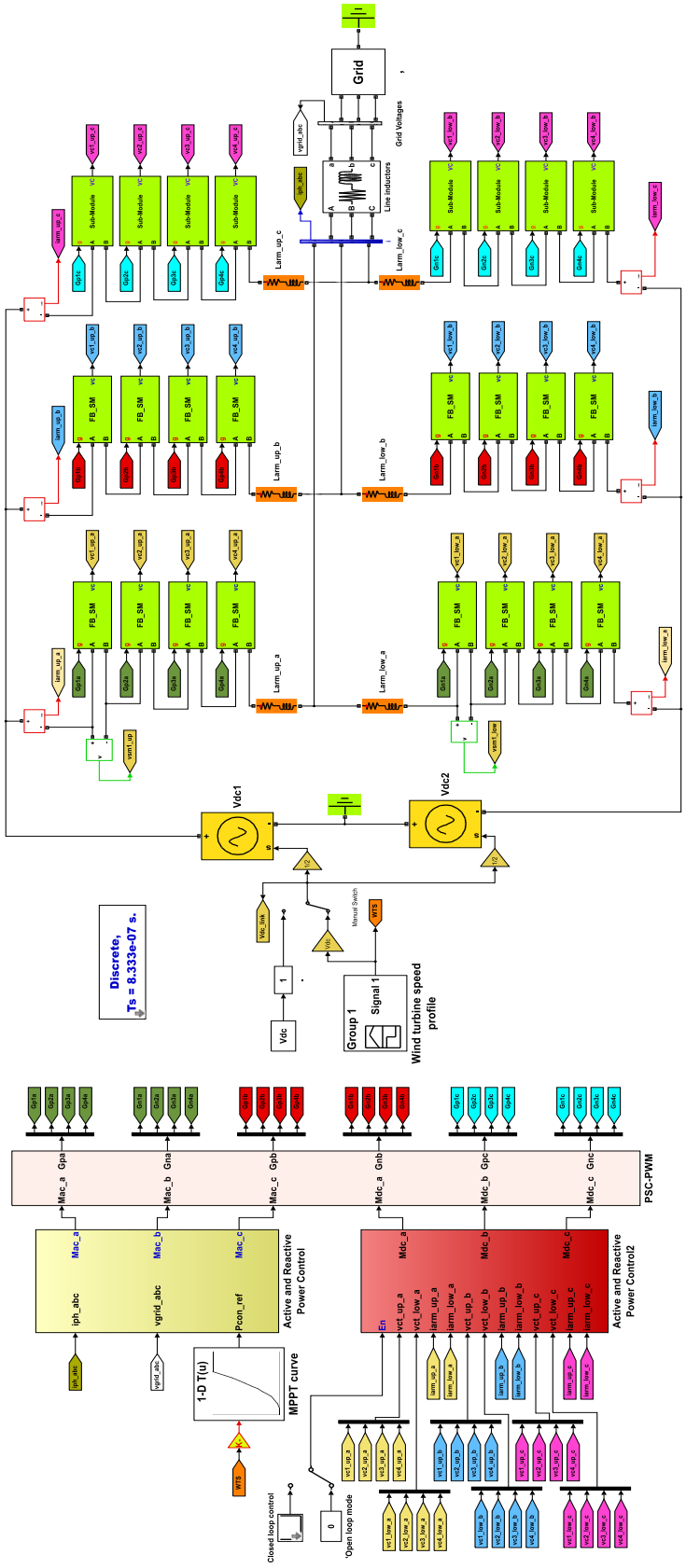


Fig A.4 Layout configuration of three-phase grid connected FB-MMC in MATLAB\Simulink

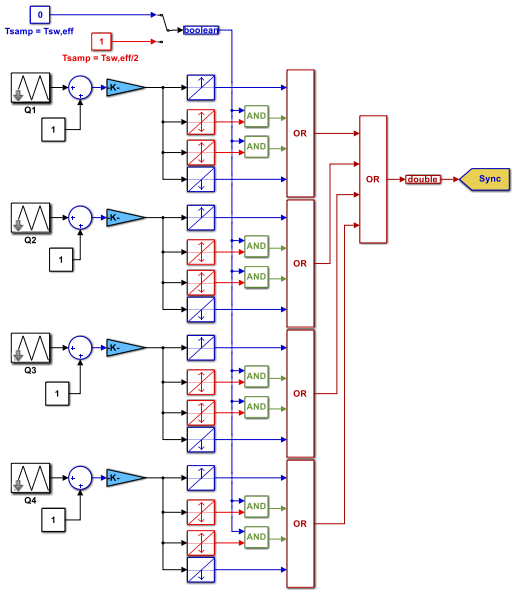


Fig A.5 Detailed circuit using the synchronous sampling technique implemented in MATLAB\Simulink

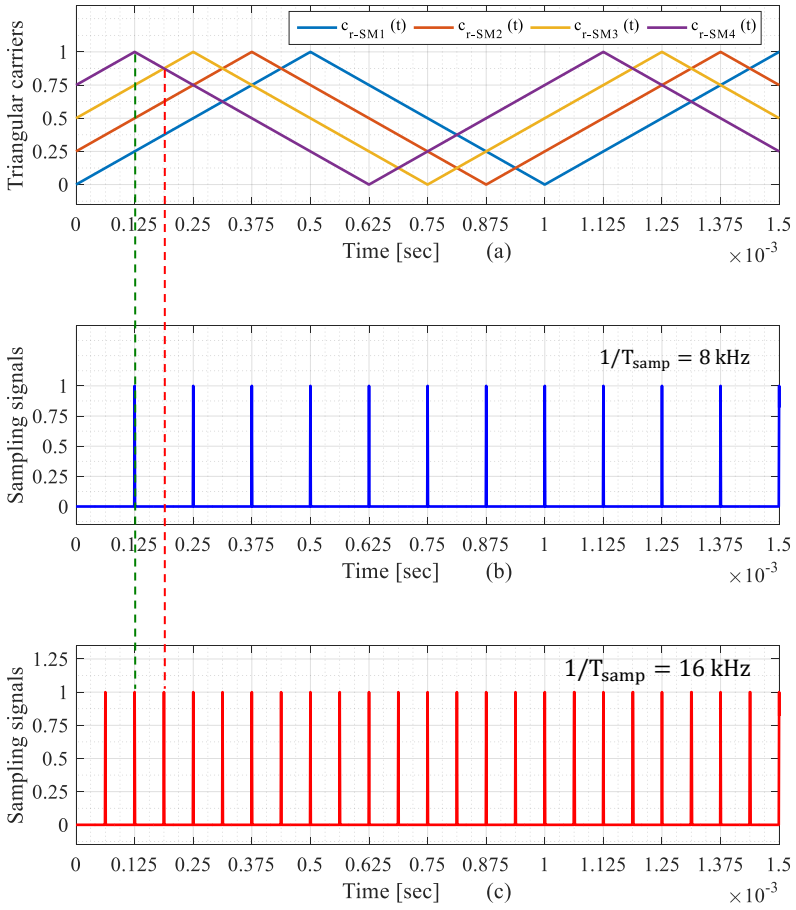


Fig A.6 Synchronous sampling for the current waveform using the proposed PSC-PWM strategy, (a) PSC-PWM scheme for the FB-MMC (b) Sampling start signals when $1/T_{samp} = 8$ kHz (c) Sampling start signals when $1/T_{samp} = 16$ kHz

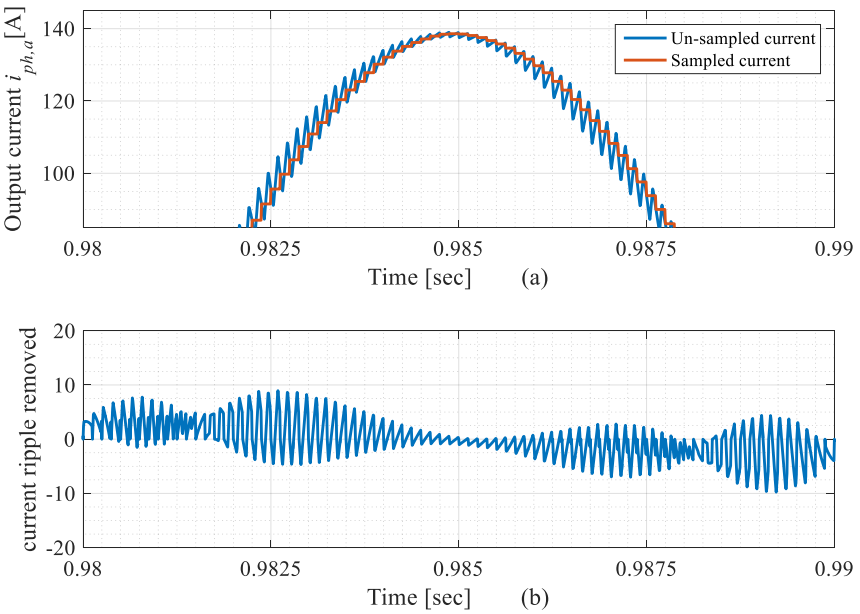


Fig A.7 (a) Zoomed portion of un-sampled and sampled measured output current when synchronous sampling achieved at $1/T_{samp} = 1/8\,\text{kHz}$, (b) current ripple removed after the output current sampling

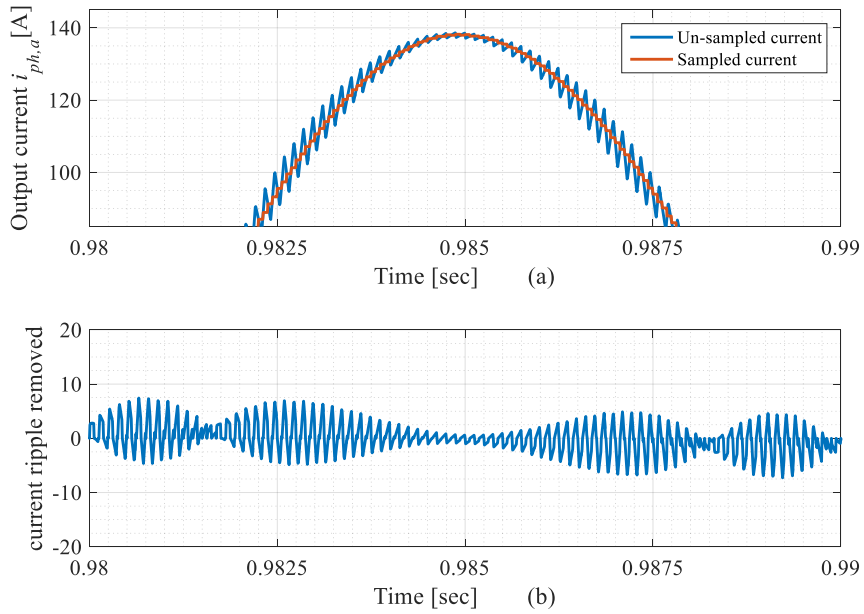


Fig A.8 (a) Zoomed portion of un-sampled and sampled measured output current when synchronous sampling achieved at $1/T_{samp} = 1/16\,\text{kHz}$, (b) current ripple removed after the output current sampling

Two different control circuits for the FB-MMC are implemented into the simulation. The first control circuit presented in section 3.5.2 is designed to regulate the active and reactive power. That considers PLL to synchronize the FB-MMC with the grid voltage as shown in Fig A.9

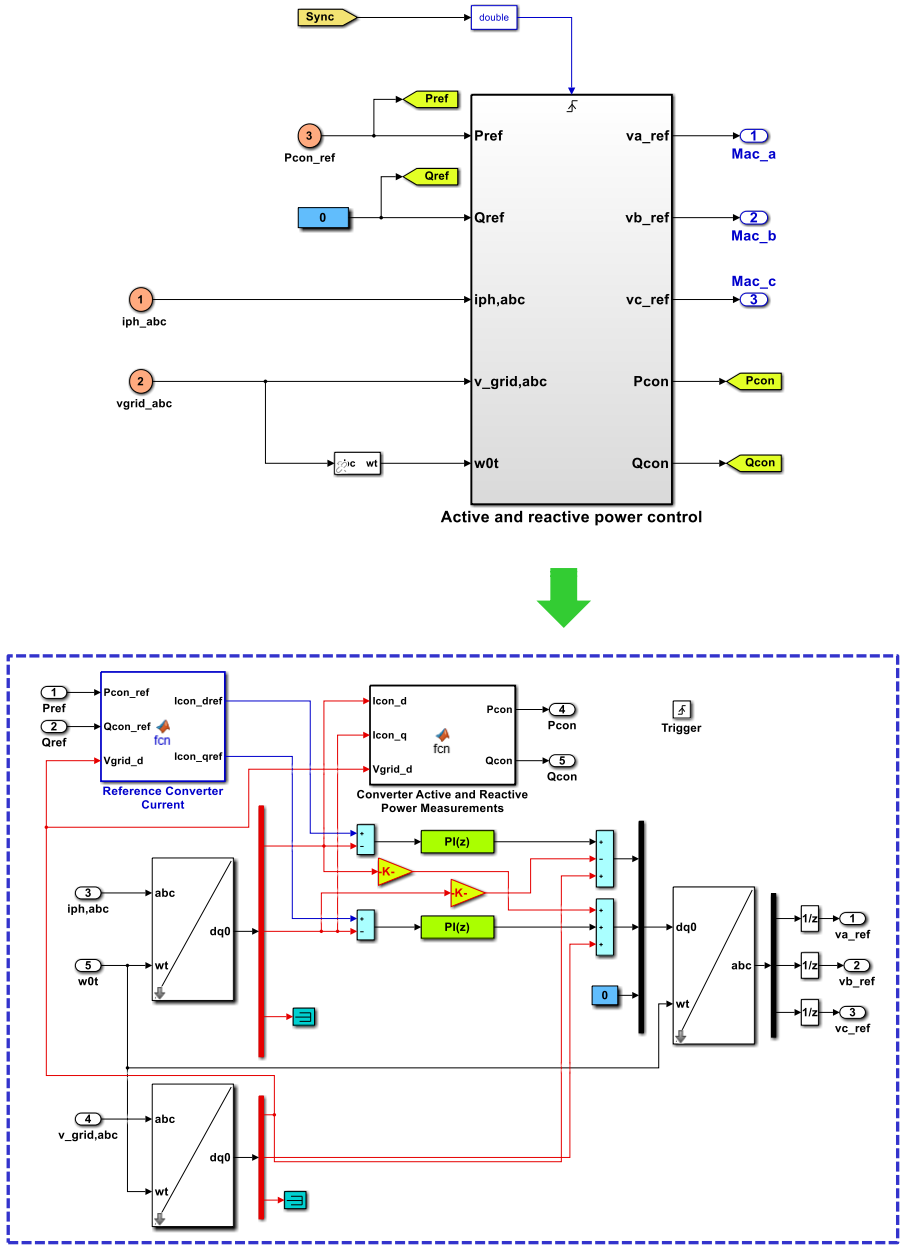


Fig A.9 Detailed model of the active and reactive power controller of three-phase grid connected FB-MMC in MATLAB\Simulink

The reactive and active power control consists of transformation blocks. They are used to compute the FB-MMC converter currents in the dq0-rotating reference frame for three-phase sinusoidal signals in the abc stationary frame. The abc to dq0 transformation blocks of the output currents can be given as follows:

$$\begin{bmatrix} i_{ph.d} \\ i_{ph.d} \\ i_{ph,0} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} sin(\omega_0 t) & sin(\omega_0 t - \frac{2\pi}{3}) & sin(\omega_0 t + \frac{2\pi}{3}) \\ cos(\omega_0 t) & cos(\omega_0 t - \frac{2\pi}{3}) & cos(\omega_0 t + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} i_{ph.a} \\ i_{ph.b} \\ i_{ph,c} \end{bmatrix} \quad (7.2)$$

The ω_0 refers to a rotation speed (rad/s) of the rotating reference frame. However, these signals are back transformed to *abc* stationary frame reference as the modulating signals (voltages). The *dq0* to *abc* transformation block can be obtained as follows:

$$\begin{bmatrix} v_{ph.a} \\ v_{ph.b} \\ v_{ph,c} \end{bmatrix} = \begin{bmatrix} sin(\omega_0 t) & cos(\omega_0 t) & 1 \\ sin(\omega_0 t - \frac{2\pi}{3}) & cos(\omega_0 t - \frac{2\pi}{3}) & 1 \\ sin(\omega_0 t + \frac{2\pi}{3}) & cos(\omega_0 t + \frac{2\pi}{3}) & 1 \end{bmatrix} \begin{bmatrix} v_{ph.d} \\ v_{ph.d} \\ v_{ph,0} \end{bmatrix} \quad (7.3)$$

However, the second control circuit is the average capacitor voltage and circulating current control, which is mainly built to regulate the dc capacitor voltage of all FB-submodules and to minimize the 2nd harmonic circulating current as illustrated in Fig A.10.

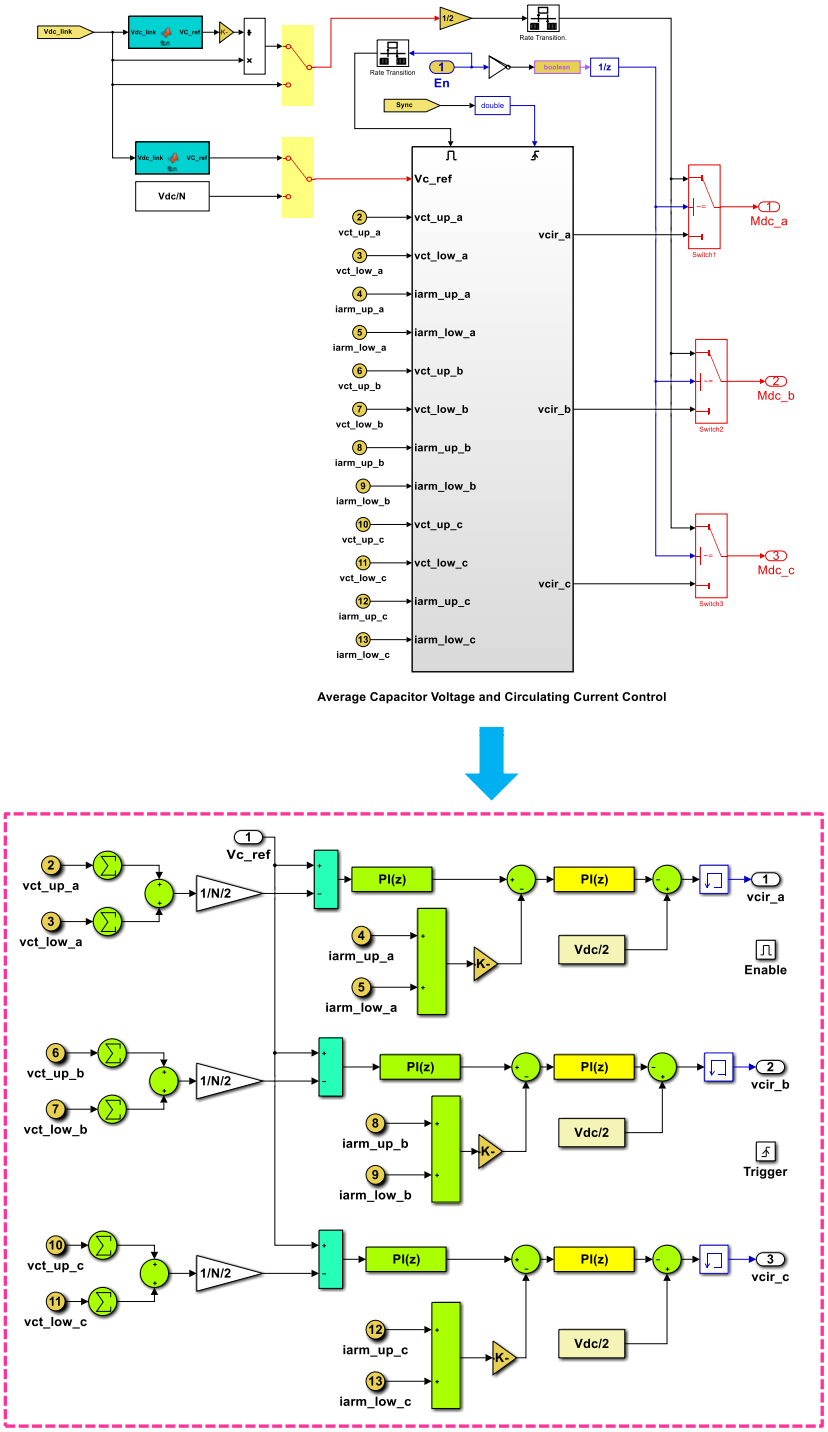


Fig A.10 Detailed model of the dc capacitor voltage and circulating current controller of three-phase grid connected FB-MMC in MATLAB\Simulink

Appendix D Implementing the simplified switching model of the FB-MMC used for harmonic contents identification

The simplified model of the FB-MMC is implemented in MATLAB\Simulink that to validate results obtained from the analytical modelling derived in Chapter 5. As shown in Fig A.11, this model is built in the four FB-submodules per arm. Instead of using a capacitor, each FB-submodule uses a dc voltage source, as voltage ripples across the FB-submodule capacitor are not considered in this analysis. In addition, the simplified switching model is not composed of the arm inductors. This simulation model operates in the open-loop mode in which the modulation indexes, capacitor voltage and simulation time step are adjusted via M-file that used to initialize model parameters. The M-file code is listed as follows:

```
clc; close all;
Vdc_nom=10000;                  %  Nominal value of the dc link voltage
D=0.6                           % The decrease in the dc link voltage
Vdc_act=D*Vdc_nom;              % Actual value of the dc link voltage
N=4                             % No. of FBSM

% The 1st capacitor voltage regulation defined by (3.16)
Vc_ref=Vdc_nom/N;
% The 2nd capacitor voltage regulation defined by (3.17)
% OR%Vc_ref=(Vdc_nom+Vdc_act)/(2*N)-10;

% Modulation indexes
Mdc=Vdc_act/(N*Vc_ref);
Mac=(Vdc_nom/2/N)/(Vc_ref/2);

f=50;                           % Fundamental frequency
Fsw=2000;                       % Switching frequency
mf=Fsw/f;                       % Frequency ratio

Fc=mf*f;
Tc=1/Fc;

period_fund=1/f;                % fundamental period
period_sample=(Tc/2/4000);      % sample period % 1.25e-7
Ts=period_sample;               % simulation time step

% Shifted angles carrier waves
Q1=0;Q2=45;Q3=90;Q4=135;
```

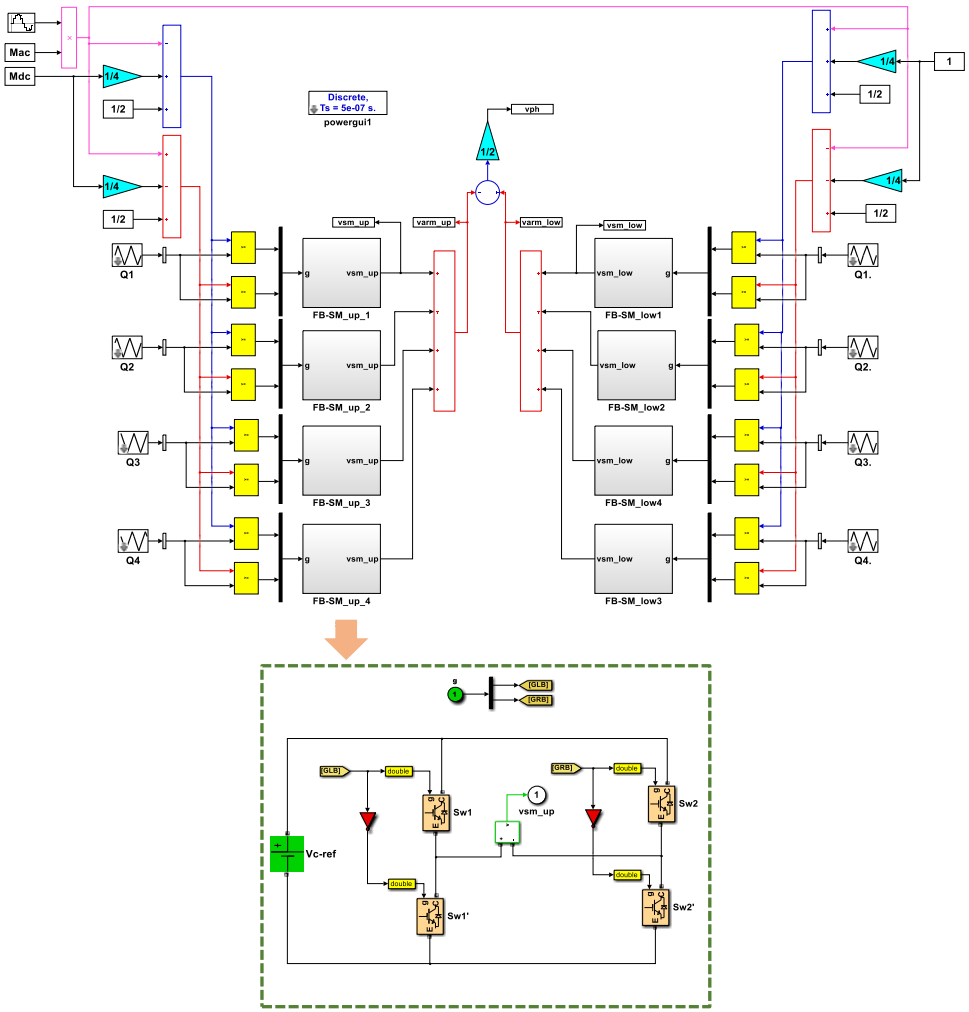


Fig A.11 Simplified switching model of the single-phase FB-MMC implemented in MATLAB\Simulink

Appendix E Implementing analytical modelling for PWM harmonic contents of the FB-MMC voltages

The analytical expressions derived in Chapter 5 are implemented and simulated using MATLAB\M-files environment. The obtained results of the M-file simulation are verified to those of the simplified switching model of the FB-MMC. Of note that the harmonic spectrum range of Har_max is calculated in this M-file simulation from as the following expressions [83]:

$$Har\_max = m\_max.m_f - n\_max$$
$$n\_max = abs\ (n\_min) \tag{7.4}$$
$$n\_min = 1 - m\_max.m_f$$

Where n_max and n_min refer to maximum and minimum baseband indexes, respectively. They are used to determine the range of the sideband harmonics centred around the carriers. Thus, M-files code of this analytical modelling to identify the harmonic contents of the FB-MMC is given as follows:

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Analytical Modelling of Harmonic Contents Identification %
% for PWM voltage of submodule of the FB_MMC                %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

clc; close all;

Vdc_nom=10000;        % Nominal value of the dc link voltage
D=0.6;                % The decrease in the dc link voltage
Vdc_act=D*Vdc_nom;    % Actual value of the dc link voltage
N=4;                  % No. of FB-SM

%The 1st capacitor voltage regulation defined by (3.16)

Vc_ref=Vdc_nom/N;

%The 2nd capacitor voltage regulation defined by (3.17)
%Or
Vc_ref=(Vdc_nom+Vdc_act)/(2*N);

% Modulation indexes

Mdc=Vdc_act/(N*Vc_ref);
Mac=(Vdc_nom/2/N)/(Vc_ref/2);


f=50;                 % Fundamental frequency
fsw=1000;             % Switching frequency of IGBTs
mf=fsw/f;             % Frequency ratio mf= 20

% Harmonic Number and Range

m_max=4; % Harmonic group number
h_min=1;
n_min(m_max)=(h_min-m_max*mf);       % Minimum baseband index
n_max(m_max)=abs(n_min(m_max));      % Maximum baseband index
h_max(m_max)=m_max*mf+n_max(m_max); % Harmonic spectrum range

%%%
```

```
for Har_0=1:1 %% Left Leg %%

%%%%% The dc component %%%%%

vsm_up_H0=(Mdc/2)*Vc_ref;

%%%%% Fundamental component %%%%%%

k=1;
for i=1:k
for h=1
    vsm_up_H1(i,h)=-(Mac/2)*Vc_ref;
end

%%%%% Baseband Harmonics %%%%%%

for h=2:h_max(m_max)
    vsm_up_H1(i,h)=0;
end
end

%%%%% Carrier Harmonics %%%%%

for i=1:k
for m=1:m_max
    n=0;
    q=0;
    h=m*mf+n;

CH=sin(m*(2+Mdc)*pi/4)-sin(m*(2-Mdc)*pi/4);
vsm_up_Hm(i,h)=(2*Vc_ref)/(pi*m)*besselj(q,m*pi*Mac/4)*CH;

    g1=m*mf-mf+1;
    g2=m*mf-1;
for y=g1:g2
    vsm_up_Hm(i,y)=0;
end
for y=(m_max*mf+1):m_max*mf+n_max(m_max)
    vsm_up_Hm(i,y)=0;
end
end
end


%%%%% Baseband Harmonics %%%%%

for i=1:k
for h=1:h_max(m_max)
    vsm_up_Hn(i,h)=0;
end
end
for i=1:k
for m=1:m_max
    n_min(m)=(h_min-m*mf);
    n_max(m)=h_max(m_max)-abs(n_min(m));
```

```
for n=n_min(m):n_max(m)
    q=n;
    h=m*mf+n;
    h_max(m)=m*mf+abs(n_min(m));

if n~=0


BH=(-1)^n*sin(((2+Mdc)*m+2*n)*pi/4) ...
          sin(((2-dc)*m+2*n)*pi/4);

vsm_up_Hn1(i,h)=(2*Vc_ref)/(pi*m)*besselj(q,m*pi*Mac/4)*BH;

else
   vsm_up_Hn1(i,h)=0;
end
for z=1:h_max(m)
if z==h
vsm_up_Hn(i,z)=vsm_up_Hn(i,z)+ vsm_up_Hn1(i,z);
end
end
end
end
end

%%%%% Sum  H0 %%
 for i=1:k
 for z=1:(h_max(m_max))

vsm_up_H(i,z)=vsm_up_H1(i,z)+vsm_up_Hm(i,z)+vsm_up_Hn(i,z);
   end
end
end;

%% Normalization of the harmonic amplitudes with Vdc_nom/2 %%

xmax=h_max(m_max);
x=0:1:xmax;
vsm_up_H_norm(1,x(2:end))=vsm_up_H(1,x(2:end))*2/(Vdc_nom);
vsm_up_H_norm_amp(1,x(2:end))=abs(vsm_up_H_norm(1,x(2:end)));

%%%% Plotting harmonic spectrums of the Analytical model %%%%

figure(1);

vsm_up_H0_norm=vsm_up_H0/Vdc_nom*2
bar(x,[vsm_up_H0_norm,vsm_up_H_norm_amp],'r','BarWidth',0.3);
xlabel('Harmonic order
(a)','fontsize',30,'fontweight','normal');
ylabel('Amplitude
[p.u]','fontsize',30,'fontweight','normal');
set(gca,'FontSize',16,'FontName','Times New
Roman','fontweight','normal');
axis([-5 180 1e-2 1.4]);
set(gca, 'YScale', 'log')
```

```
leg =legend('Analytical Model defined by (5.28),(5.29)');
set(leg, 'FontSize', 16);
grid on;

%%%% Plotting harmonic spectrums of the switching model %%%%

figure(2);

signal=vsm_up;
signal=signal(end-1/(f*Ts):end);
L=length(signal);
m=2*fft(signal)/L;
Amp=abs(m);
fs=1/Ts;
ff=0:fs/L:(H-1)*(fs/H);
Amp(1)=Amp(1)/2;
ff=ff/ff(2);

bar(ff(1:H),Amp(1:H),'FaceColor',[0 0 1],'EdgeColor',[0 0
1],'BarWidth',0.25);
xlabel('Harmonic order
(b)','fontsize',30,'fontweight','normal');
ylabel('Amplitude
[p.u]','fontsize',30,'fontweight','normal');
set(gca,'FontSize',16,'FontName','Times New
Roman','fontweight','normal');
axis([-5 180 1e-2 1.4]);
leg =legend('Switching model based on FFT analysis');
set(leg, 'FontSize', 16);
set(gca, 'YScale', 'log');
grid on;


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Analytical Modelling of Harmonic Contents Identification %
% for PWM arm voltage of the FB_MMC                        %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

clc; close all;

Vdc_nom=10000;        % Nominal value of the dc link voltage
D=0.6;                % The decrease in the dc link voltage
Vdc_act=D*Vdc_nom;    % Actual value of the dc link voltage
N=4;                  % No. of FB-SM

%The 1st capacitor voltage regulation defined by (3.16)

Vc_ref=Vdc_nom/N;

%The 2nd capacitor voltage regulation defined by (3.17)
%Or
Vc_ref=(Vdc_nom+Vdc_act)/(2*N);

% Modulation indexes

Mdc=Vdc_act/(N*Vc_ref);
```

```
Mac=(Vdc_nom/2/N)/(Vc_ref/2);


f=50;                  % Fundamental frequency
fsw=1000;              % Switching frequency of IGBTs
mf=2*fsw/f*N;              % Frequency ratio 2*mf*N= 160

% Harmonic Number and Range

m_max=4; % Harmonic group number
h_min=1;
n_min(m_max)=(h_min-m_max*mf);       % Minimum baseband index
n_max(m_max)=abs(n_min(m_max));      % Maximum baseband index
h_max(m_max)=m_max*mf+n_max(m_max); % Harmonic spectrum range

%%%

for Har_0=1:1 %% Left Leg %%

%%%%% The dc component %%%%%

varm_up_H0=(Mdc/2)*Vc_ref;

%%%%% Fundamental component %%%%%%

k=1;
for i=1:k
for h=1
    varm_up_H1(i,h)=-(Mac/2)*Vc_ref;
end

%%%%% Baseband Harmonics %%%%%%

for h=2:h_max(m_max)
    varm_up_H1(i,h)=0;
end
end

%%%%% Carrier Harmonics %%%%%

for i=1:k
for m=1:m_max
    n=0;
    q=0;
    h=m*mf+n;

CH=sin(m*N*(2+Mdc)*pi/2)-sin(m*N*(2-Mdc)*pi/2);
varm_up_Hm(i,h)=(Vc_ref)/(pi*m)*besselj(q,m*N*pi*Mac/2)*CH;

    g1=m*mf-mf+1;
    g2=m*mf-1;
for y=g1:g2
    varm_up_Hm(i,y)=0;
end
for y=(m_max*mf+1):m_max*mf+n_max(m_max)
    varm_up_Hm(i,y)=0;
```

```
end
end
end


%%%%% Baseband Harmonics %%%%%

for i=1:k
for h=1:h_max(m_max)
    varm_up_Hn(i,h)=0;
end
end
for i=1:k
for m=1:m_max
    n_min(m)=(h_min-m*mf);
    n_max(m)=h_max(m_max)-abs(n_min(m));

for n=n_min(m):n_max(m)
    q=n;
    h=m*mf+n;
    h_max(m)=m*mf+abs(n_min(m));

if n~=0


BH=(-1)^n*sin(((2+Mdc)*m*N+n)*pi/2)- ...
          sin(((2-Mdc)*m*N+n)*pi/2);

varm_up_Hn1(i,h)=(Vc_ref)/(pi*m)*besselj(q,m*N*pi*Mac/2)*BH;

else
   varm_up_Hn1(i,h)=0;
end
for z=1:h_max(m)
if z==h
varm_up_Hn(i,z)=varm_up_Hn(i,z)+ varm_up_Hn1(i,z);
end
end
end
end
end

%%%%% Sum  H0 %%
 for i=1:k
 for z=1:(h_max(m_max))
     varm_up_H(i,z)=varm_up_H1(i,z)+varm_up_Hm(i,z) ...
                   +varm_up_Hn(i,z);
   end
end
end;

%% Normalization of the harmonic amplitudes with Vdc_nom/2 %%

xmax=h_max(m_max);
x=0:1:xmax;
varm_up_H_norm(1,x(2:end))=varm_up_H(1,x(2:end))*2/(Vdc_nom);
```

```
varm_up_H_norm_amp(1,x(2:end))=abs(varm_up_H_norm(1,x(2:end))
) ... ;

%%%% Plotting harmonic spectrums of the Analytical model %%%%

figure(1);

varm_up_H0_norm=varm_up_H0/Vdc_nom*2
bar(x,[varm_up_H0_norm,varm_up_H_norm_amp],'r','BarWidth',0.3
);
xlabel('Harmonic order
(a)','fontsize',30,'fontweight','normal');
ylabel('Amplitude
[p.u]','fontsize',30,'fontweight','normal');
set(gca,'FontSize',16,'FontName','Times New
Roman','fontweight','normal');
axis([-5 180 1e-2 1.4]);
set(gca, 'YScale', 'log')
leg =legend('Analytical Model defined by (5.28),(5.29)');
set(leg, 'FontSize', 16);
grid on;

%%%% Plotting harmonic spectrums of the switching model %%%%

figure(2);

signal=varm_up;
signal=signal(end-1/(f*Ts):end);
L=length(signal);
m=2*fft(signal)/L;
Amp=abs(m);
fs=1/Ts;
ff=0:fs/L:(H-1)*(fs/H);
Amp(1)=Amp(1)/2;
ff=ff/ff(2);

bar(ff(1:H),Amp(1:H),'FaceColor',[0 0 1],'EdgeColor',[0 0
1],'BarWidth',0.25);
xlabel('Harmonic order
(b)','fontsize',30,'fontweight','normal');
ylabel('Amplitude
[p.u]','fontsize',30,'fontweight','normal');
set(gca,'FontSize',16,'FontName','Times New
Roman','fontweight','normal');
axis([-5 180 1e-2 1.4]);
leg =legend('Switching model based on FFT analysis');
set(leg, 'FontSize', 16);
set(gca, 'YScale', 'log');
grid on;
```

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