Synthesised Local Oscillator Design Considerations for Satellite Data Communications Systems

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Abstract

This thesis presents a new coherent approach to the problems of phase noise in satellite communications systems. An original aspect of this approach is the consideration of the effect of synthesised local oscillators, rather than local oscillators in general, as sources of phase noise. Performance of local oscillators in such systems is critical, particularly with respect to low data rates.

The study of synthesiser performance includes a detailed investigation of suitable synthesiser architectures for satellite communications usage. Resulting from this are recommendations for a unique hybrid of those synthesiser techniques which is most suited to the particular demands of satellite communications work. Guidelines for synthesiser component design required to implement these techniques are presented here with the aim of avoiding the problems frequently observed within synthesisers. The expertise gained from such a study of synthesisers is used to predict the effect of using synthesised local oscillators on a satellite data link, a topic not often covered in literature on satellite data systems.

A particular problem exists with flicker noise from tuneable oscillators which are required to enable capture of received signals. Direct digital synthesis (DDS) provides a ready solution to this problem but may introduce unwanted spurious signal products. A novel patented method of reducing these products to a generally satisfactory level is described here which ensures the viability of a proposed new integrated transmitter synthesiser approach. In order to provide a synthesised local oscillator from DDS at microwave frequencies some additional techniques must be used. One such approach using step recovery diodes (SRDs) is described here. An in depth study is presented here that shows that although they are capable low phase noise performance, care must be taken to avoid chaotic effects.

Finally a novel approach to link budget analysis is suggested. Results are presented here of software analysis written in the course of this research work to calculate the impact of local oscillator phase noise upon link sensitivity. This demonstrates the possible advantages of the above synthesiser techniques for local oscillators in satellite data communications systems.

CONTENTS

1 Introduction

1.1 Overview and objectives

In recent years, there has been increasing use of satellite data systems, particularly with respect to very small aperture terminals (VSATs). However unlike the television receive-only market (TVRO), the market volume is insufficient for large economies of scale to be made. The market volume for TVRO equipment enables such units to sell at a few hundred pounds per unit. Satellite data terminals, on the other hand, have been restricted to a much smaller market base and the cost per unit is much higher, being thousands of pounds per unit. In order to broaden the market base for satellite data terminals, costs of the terminals must fall.

One of the problems restricting such a fall in costs is lack of standardisation of system format throughout the industry. The other problem lies in providing suitable low cost local oscillators for the satellite terminal downconversion and upconversion stages. Low cost downconverters have been developed for TVRO applications, and these must be synthesised to allow selection of different channels. However, these present a number of problems when used for satellite data systems. This thesis examines such problems, particularly with respect to phase noise, and recommends guidelines for the design of synthesised converters suitable for data systems. It is shown that the close to carrier phase noise is more important in the case of satellite data terminals than in the TVRO case where wideband noise is of greatest concern.

Satellite data terminals must also be synthesised to allow versatile re-allocation of channels. In the majority of cases the satellite channel user does not want to have any concern about the link RF frequency so it is desirable that this function would be governed by the hub controller, and any channel re-allocation be undertaken automatically without

any user intervention. For this function to be provided, the local oscillators should consist of a synthesiser programmable from a logic controller such as a microprocessor.

Until recently, synthesiser technology has been geared towards either the radio and TVRO markets, or the radar and military markets. In the radio and TV markets, the emphasis is on low far from carrier phase noise. Private mobile radio (PMR) synthesisers must have low phase noise in the adjacent channel, or the radio receiver sensitivity suffers by reciprocal mixing of phase noise onto a strong adjacent channel signal. TV signals occupy a broad frequency band and therefore it is essential to maintain low average phase noise over this broad bandwidth. These requirements may be met by means of a moderately high Q fundamental oscillator operating at the local oscillator frequency [Linnecar, 1974].

With PMR, the range of frequency tuning may not be very large, but the individual channels are closely spaced. Achieving the phase noise specification by means of the synthesiser processing circuitry would be difficult within the budget allowed for in the radio set price. Therefore, the usual approach is to phase lock a low noise VCO, designing the VCO to fit the phase noise specification of the set. The synthesiser control circuitry then ensures that the long term stability of the crystal oscillator is transferred to the output. As the synthesiser processing circuitry phase noise is now not critical, a cheap single IC synthesiser can be used for phase locking. An important difference between PMR radio and satellite data system requirements is that with the latter the phase noise has a degrading effect upon the modulation itself, in contrast to merely adjacent channel considerations with the former. As a result of potential modulation degradation, close to carrier phase noise performance becomes critical. Another vital difference is that the local oscillator must operate at microwave frequencies so the phase noise becomes worse as a result of multiplication from the reference frequency.

Radar synthesisers make similar demands in terms of phase noise as satellite data systems in that they must operate at microwave frequencies, and display very low phase noise at close to carrier frequencies, in order to resolve slow moving targets from background clutter [Roulston, 1984]. A typical requirement for phase noise in this case is -130 dBc/Hz at 3 kHz from carrier at 10 GHz. However, the step size in this case is usually large, of the order of 20 MHz. The cost of this type of synthesiser is usually no object and they are ruggedised for airborne use.

With the advent of small terminal satellite communications, the Ku bands are rapidly becoming crowded. As demand increases, there is mounting pressure on spectral allocation and bandwidth. In order to keep the same information rate, and reduce

bandwidth, higher order modulation systems must be used. Unfortunately, such schemes place more pressure on system phase noise levels.

Among the problems encountered with the application of PMR type synthesisers to satellite data communications systems are the following:-

1) A wide tuning range of hundreds of MHz are required;

2) The close to carrier phase noise of microwave tuneable free running oscillators is excessive;

3) Susceptibility to vibration becomes a problem due to narrow bandwidth phase locked loops;

4) Accurate modulation is difficult.

It is the object of this thesis to investigate methods of providing a cost effective solution to the design of synthesisers for satellite data terminals.

An additional problem is that carrier frequencies are rising and Ka band (30GHz) systems are beginning to enter service. As the frequency of such links increases, more will be demanded from local oscillators in terms of phase noise and spurious levels.

With present day synthesiser technology, the cost tends to follow a series of vertical steps [Payne, 1984] rather than rising smoothly with increasing specification demands. This results from a given configuration failing to deliver the increased performance, and therefore necessitating a more complicated design.

In order to arrive at a cost effective solution, it is vital to transform the system requirements into a suitable specification for a synthesiser, to avoid expensive over-engineering. The synthesiser design should meet any future upgradability requirements, for instance a more bandwidth efficient modulation scheme may be used in the future.

A problem that exists to date from a system designer's point of view is that information on phase noise has been piecemeal. This is particularly true with regard to the effect of phase noise on system performance. System designers are often left with little understanding of how phase noise is generated within local oscillators and synthesisers. Synthesiser component designers on the other hand, often have limited understanding at the system level. Demarcation exists therefore between the system designer and the synthesiser component designer. A result of this is that synthesisers may be designed towards a

certain phase noise goal without regard to future upgradability, or other factors that may be important to system performance.

This thesis aims therefore aims to bring together the phase noise information relevant to system designers. Armed with a such an understanding of phase noise, a bridge is attempted between the system level design and the component design. Only through the forming of such a bridge will a true cost effective compromise be reached that ensures a long working life for a data system. It is the intention of the author to provide overall guidance to both system and component designers on the design and selection of synthesised local oscillators.

1.2 Outline of Thesis

Phase noise is first investigated in chapter 2 by studying how it originates and what effect it has on a RF signal. From this, phase noise effects within oscillators are considered so that an understanding of the oscillator spectral shape can be achieved.

In the course of the classical analysis of oscillator noise presented in chapter 2, a problem is identified which comes under scrutiny in chapter 3: most treatments of oscillator noise ignore the 1/f or flicker noise, particularly the resonator contribution. Chapter 3 attempts to provide some insight into the curious phenomenon of flicker noise or 1/f noise. Although predominantly a low frequency effect, various modulation modes can result in flicker noise appearing on a RF signal. Chapter 3 shows why 1/f noise is of particular importance in designing synthesisers for low data rate satellite communications equipment. In addition to general 1/f effects, the high Q resonator in an oscillator, such as a crystal, can contribute its own 1/f noise. In chapter 3 we show that the resonator noise is the principal component of microwave oscillator close to carrier phase noise and therefore a dominant factor in designing for satellite data communications systems.

In order to assess synthesiser phase noise, the synthesiser architecture must be determined. A survey of possible synthesiser designs is undertaken in chapter 4 and their merits and problems compared. Using an assessment of the architectures, methods of combining the different techniques to form a hybrid microwave synthesiser are developed. During the course of this investigation, other problems such as vibration and phase "hits " are shown to be of importance.

On completion of the survey of possible synthesiser architectures carried out in chapter 4, chapter 5 investigates the phase noise and spurious contributions of each subsection in a synthesiser. One problem to be given particular attention is the minimisation of "excess noise" of a frequency multiplier in addition to the theoretical frequency multiplication factor. Phase locked loop and non phase locked loop methods of frequency multiplication are investigated. Computer simulation techniques are devised for both a phase locked loop multiplier and a step recovery diode (SRD) comb generator multiplier. In the case of phase locked loop synthesis the computer model is used to investigate injection locking and how it can affect system design. Chapter 5 describes a method of combining the locking properties of a phase locked loop multiplier with the low phase noise performance of the SRD. After assessment of the resultant static phase noise levels, methods of reducing the effects of vibration are discussed.

Chapter 6 goes on to assess the likely impact on system performance of the phase noise levels introduced by the synthesiser architectures. Phase noise degradation calculations are performed for coherent receivers used with a variety of different modulation schemes. The phase noise analysis given in chapter 6 includes not only random phase noise, but also discrete spurious sidebands. The case is argued for a phase noise link budget to be performed iteratively alongside the normal communication link budget. It is shown that the phase locked loop type multiplier synthesiser contributes excessive close to carrier phase noise to the phase noise link budget for higher order modulation schemes.

This prompts an investigation, documented in chapter 7, into the use of a step recovery diode (SRD) as a means of reducing phase noise. From work done by the author previously on SRD multipliers it was apparent that very low levels of excess phase noise can be achieved in this way. However, under certain circumstances, the phase noise levels can be severely degraded. To facilitate investigation, computer programs were written to simulate the SRD as a comb generator and results of these simulations are shown in chapter 7. A salient feature of the simulation results shown in chapter 7 is the demonstration of the tendency of the SRD circuits to show chaotic behaviour. It is shown that such chaotic behaviour can drastically degrade the phase noise performance of the SRD multiplier comb generator. A series of design guidelines are developed and presented in chapter 7 to enable the lowest possible phase noise levels from a synthesiser using SRD circuits to be achieved.

In particular, methods are described where the SRD is combined with a direct digital synthesiser (DDS) to provide a fine stepping synthesiser.

Direct digital synthesis provides low phase noise and immunity to vibration, but at present the spurious performance often leaves something to be desired. Chapter 8 presents a thorough investigation of this problem, leading to a possible solution for which a patent has been applied. A method is described where, by the addition of some extra digital components, the spurious signal levels using real 8 bit DACs can be reduced below - 70 dBc. Computer simulations are described that illustrate the maximum spurious signal levels. A test DDS synthesiser was constructed to verify the results of our simulations. The results of this test synthesiser are displayed showing the improvements in spurious signal levels. Most of the spurious signal reduction takes place in the digital domain which enables a high level of integration.

Use of DDS is particularly interesting as it enables the synthesiser to be modulated directly from the output of digital signal processing devices. By making the synthesiser perform upconversion and modulation, an opportunity is therefore given to move the synthesiser from the periphery to the centre of the system, making it more justifiable economically to improve its performance. A method of accomplishing this is given in chapter 9.

Finally, predicted phase noise levels for various synthesiser configurations are inserted into a phase noise analysis program written by the author. This program predicts the BER performance of a satellite data communications system for any given synthesiser performance and system configuration. Results of such an analysis are compared with measurements taken on an actual modem in chapter 9. It is shown that by use of techniques outlined in this thesis, the dominant phase noise contribution to the satellite link comes from the satellite transponder itself. There is thus an argument for tightening of the transponder phase noise specification to enable the use of higher order modulation schemes in the satellite link.

1.3 Background and origin of research

This thesis originated through the Pandata program for commercial data links by satellite [Garrett, 1988] originally undertaken by Ferranti Computer Systems Ltd, (formerly CSR Ltd) of Ilkley. The system was originally intended as a direct sequence spread spectrum CDMA (code division multiple access) terminal using BPSK with forward error correction. One of the chief obstacles to be overcome to make the Pandata system viable was the provision of low cost local oscillator technology. Initially an attempt was made using a TVRO type low noise block front end and synthesised down converter. Catastrophic degradations in system sensitivity resulted, which were overcome only by

the use of professional microwave synthesised signal generators. Research into methods of providing low cost, low phase noise microwave synthesis was clearly necessary.

In the first stages of this research, CSR developed an offset QPSK ground station modem terminal for the Skyphone program [Brown, 1989], which is an in flight telephone system for commercial airlines. A VHF phase locked loop synthesiser was designed for this using the 3 loop technique as described in §4.2.4, with a fixed phase locked oscillator for the microwave 1st LO. The implementation loss of the modem above the theoretical sensitivity level was only 0.2dB. However the tuning range was only 24MHz, too narrow for many applications. It was necessary to continue the research to enable the above performance to be achieved using a wide tuning range microwave synthesiser.

This work was carried out at the University of York under the guidance of Mr T. C. Tozer, and Dr A. G. Burr. The work was made possible by the kind support of Ferranti Computer Systems Ltd of Ilkley (formerly CSR Ltd) and Ferranti Computer Systems Ltd Microwave and Satellite Communications division at Poynton. The author would wish to particularly thank: Dr R. Gough and Mr K. Hodson of CSR Ltd for helping to initialise this work along with assistance during its progress; Mr. Tozer, and Dr Burr for their helpful supervision; along with Mr M. Evanson, Dr D. Lynes and Mr G. Parkinson of Poynton for their kind assistance. The author would wish to thank other people from the University of York and Ferranti for their support and encouragement.

1.4 References

Brown, S. 1988 Design of a C channel Skyphone modem for the Inmarsat Aeronautical Satellite Service. *4th International Conference on Satellite Systems for Mobile Communications and Navigation,* IEE, London. October 1988.

Garrett, P., Firman, D. & Hodson, K. 1988 Data distribution by satellite. *Journal of the IERE.* Vol. 58, No. 3, pp. 109-116.

Heron, R., Marston, P. & Garrett, P. 1989 The development of a coded 8 PSK modem using digital signal processors. *International Journal of Satellite Communications,* Vol. 7, pp. 67-77.

Linnecar, T. 1974. Maximum tolerable local oscillator noise in a 12GHz FM satellite television receiver. *The Radio and Electronic Engineer,* Vol. 44, No 2, pp. 77-84.

Payne, J. June 1984 Synthesisers - An equation for cost effectiveness. *Microwaves and RF* Vol 23, No 6, p. 89.

Roulston, J. 1984. Multimode airborne radar - a review. *Conference Proceedings, Military Microwaves MM84,* pp137-147, London.

2 *Phase Noise, origins & Fundamental Design Considerations*

2.1. Introduction

This Chapter describes the fundamental properties of phase noise, as generally understood, and its relationship to thermal noise. Noise is a fundamental problem in all communication systems, the effect being to obscure the transmitted information in some way. In satellite data communication systems noise results in an increase in Bit Error Rate (BER) or a penalty in terms of link power budgets. Phase noise, although less widely appreciated than thermal noise, is none the less just as important in terms of link budget considerations. Investigation of phase noise effects begins with a study of the degrading effects in general terms, and this is followed by a study of the origins of phase noise. Individual blocks of a communication system are investigated and the phase noise contribution of each block is assessed. Finally, the significance of synthesiser "excess noise" is stressed. "Excess noise" is noise over and above the reference oscillator contribution whereas most treatments of phase noise often simply consider the local oscillator to have standard oscillator noise sidebands such as $1/f^3$ noise.

2.2. Noise in communication systems

2.2.1. Degradations and noise

The function of a communication system is to provide a faithful replica at the output of the information present at the input. All communication systems will however degrade in

some way the information at the output as compared with that at the input. The principal examples are:-

1) Noise -The addition of unwanted signals not related to the original signal;

2) Distortion -The modification of the signal by a function related to the original signal (including inter-symbol interference).

These degradations are well known in connection with analogue signals, and they have direct equivalents in digital systems. Here noise is present along with inter-symbol interference (ISI), the digital equivalent of distortion: the end result is an increase in the errors present at the output. The resulting error performance is commonly measured as the BER which is defined as the ratio of error bits to the total number of bits sent.

In order to overcome these degradations of performance in satellite systems, a number of measures may need to employed: improvement in link budget parameters (eg an increase in transmitter power); use of error correction coding; and techniques such as maximum likelihood estimation at the receiver. Techniques may also be called for to compensate for some ISI (eg adaptive threshold decoding). However, the effects of noise cannot be entirely eliminated, and it will be shown in chapter 6 that phase noise can lead to virtually irreducible error rates in certain circumstances.

The noise present in a satellite communication system can take three forms:

1) Interference from another carrier or signal;

2) Thermal or additive noise;

3) Phase noise, largely from local oscillators.

The first two sources are well documented [Feher, 1981], [Betts, 1983], but the third source is not so well understood and is covered in chapters 3 and 6.

2.2.2. Effects of noise

The effect of noise upon a digital modulation scheme (QPSK) is illustrated in fig2.1.

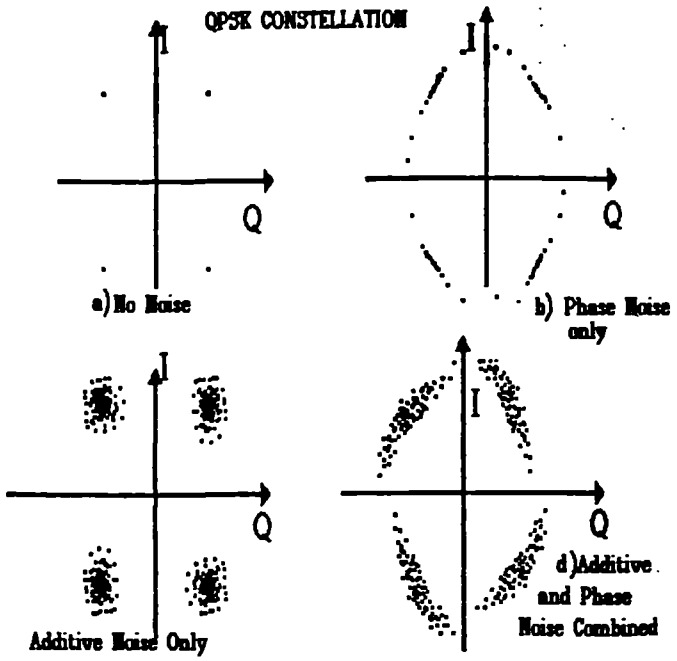


Fig 2.1 Effect of noise on signal constellations

The shaded areas illustrate the uncertainties mapped out due to noise; when the noise crosses a phase boundary, an error results. For a given noise level, the error rate is determined by the probability density function (PDF) of the noise. Additive noise gives a circular spread on the diagram, and this leads to "E_b/n_o degradation", where E_b/n_o is the energy per bit to noise density ratio. Fig 2.2 shows further how E_b/n_o degradation occurs: the ratio of dots that cross the decision threshold to the total number of dots represent the probability of a wrong decision.

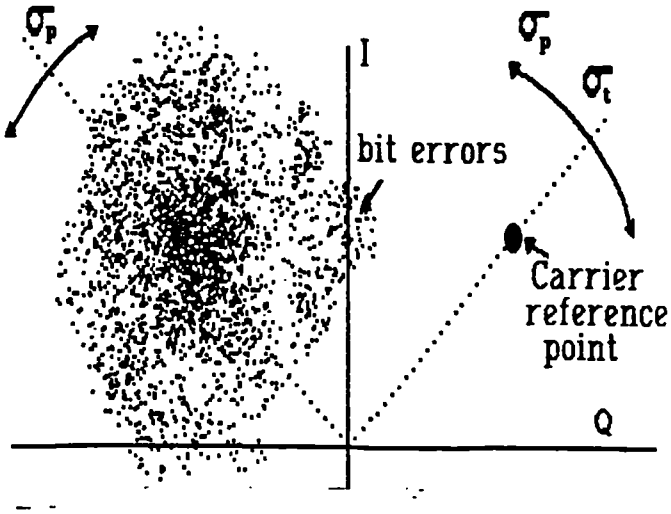


Fig 2.2 BER degradations caused at low SNR as a result of thermal noise

In addition to this is degradation due to timing errors at the demodulator. Whichever demodulation system is used, the timing of the data transitions has to be derived from the received data signal, and the effect of noise is to create uncertainties in the recovered timing. In fig2.1 the effect of timing jitter is a random circular displacement of the axis. Fig 2.1d displays the effect of using the recovered timing (including jitter) as the frame of reference and observing the resultant data signal. The circular additive noise uncertainty area becomes elliptical, increasing the probability of a wrong decision. The first degradation is a function of thermal noise, but the second is a function of both thermal and phase noise.

2.2.3. Random phase noise

Phase noise is due to random shifts in the phase of a signal that occur in passing through a system. The result is variation in the timing of the output signal referred to the input signal. Phase noise is essentially a multiplicative effect, as opposed to an additive effect such as thermal noise; the signal is effectively multiplied by $e^{j\theta}$ where θ is a random variable. The ratio of phase noise to carrier power is independent of the signal level once the phase noise has been introduced. When a signal is downconverted to a lower frequency, the angle of phase noise is unchanged from the initial source. Such frequency conversions add additional phase uncertainties, with each local oscillator contributing additional phase noise to the downconverted signal. Much care has to be taken in the design of microwave oscillators, since, for synthesised and phase locked oscillators, the effect of phase noise increases by $20\log N$ for a constant time jitter, where N = output frequency/reference frequency = $(f_{out})/(f_{ref})$.

The problem can be much more acute in synthesised local oscillators because of the increase in the complexity of signal processing circuits controlling the synthesiser. In order to design suitable local oscillators, therefore, there is a requirement to evaluate the effect of phase noise on the demodulation of the signal. Coupled with this is a requirement to evaluate cost effective techniques for minimising the phase noise contribution of synthesised local oscillators.

2.2.4. Periodic phase noise

Periodic phase noise takes the following forms:-

1) Close to carrier spurious;

2) Far from carrier spurious receive;

3) Far from carrier spurious transmit.

1) Close to carrier spurious (within the the bandwidth of the receive signal) power adds to the random phase noise as a root sum of squares, to produce the E_b/n_o degradation as mentioned above.

2) For the case of a receiver, any spurious signals outside the bandwidth of the wanted signal may, if of sufficient level, result in false locking of the receiver carrier recovery circuits if coherent detection is used. Also there may be breakthrough of the synthesiser spurious signals through the receiver downconverter, and consequently a signal present at the output for no signal input.

3) In transmit, spurious output signals outside the bandwidth of the wanted signal may cause embarrassment to other uses by appearing in their channels. This is most undesirable, therefore the spurious output specification of the transmitters is of utmost importance.

2.3. Origins of phase noise

2.3.1. Johnson, or thermal, noise

Johnson, or Thermal, noise is a fundamental form of noise caused by thermal motion in matter. It is a property of all electrical systems and has many sources. Phase noise originates from interaction between such noise and a signal carrier.

The noise power N created from any source is given by:

$$N = kTB \tag{2.1}$$

where k is Boltzmann's constant, and has value $1.38\text{x}10^{-23}$J/K, T is the ambient temperature in degrees Kelvin, and B is the bandwidth. At ambient temperature (300K) noise power is -174 dBm/Hz. This noise is proportional to bandwidth and independent of frequency, and therefore is described as white noise. The noise power rolls off at very high frequency due to the quantum behaviour of electrons, and therefore has the response [Van der Ziel, 1986a]:-

$$n_0(f) = n_0(0)\frac{hf}{kt\left(e^{hf/kt} - 1\right)} \tag{2.2}$$

where h = Planck's constant, $n_0(f)$ is the noise density per Hz at frequency f, and $n_0(0)$ is the noise density at low frequencies. This roll off commences at 10^{14} Hz, and hence noise can be considered as white for all practical communications frequencies.

2.3.2. Shot noise

Shot noise is the due to the fact that current flows in discrete quanta of charge rather than as a continuous flow. It therefore arises in the form of pulses having amplitudes equal to an integral number of the basic unit of electronic charge q. Shot noise is a fundamental source of noise occurring in all electronic devices that have a direct current flowing through them. Shot noise current I_n is determined by [Van der Ziel, 1986b]:-

$$I_n(\text{rms}) = \sqrt{(2qI_{dc}B)} \tag{2.3}$$

where $q = 1.6 \times 10^{-19}$ Coulombs, and I_{dc} is the DC current. The spectral distribution of shot noise is the same as for thermal noise (ie. white over the communication bands).

2.3.3. Flicker noise

This is a generic term applied to all noise which has the relationship with frequency (f) such that:-

$$n_0(f) \propto f^{-\gamma} \tag{2.4}$$

where $n_0(f)$ is the noise power spectral density, and $\gamma \approx 1$.

This noise has many sources, for example: resistors (where it is known as excess noise); surface states in semiconductors; traps and recombination centres in semiconductors; and conductivity modulation in semiconductors.

Flicker noise is a characteristic of all active devices, and having many sources it is more pronounced in some devices than in others. Because of the reciprocal frequency relationship, flicker noise is fundamentally a low frequency phenomenon, being masked by white noise at higher frequencies. Flicker noise is usually specified by either of two methods: by extrapolating down to 1 Hz (e.g. -120 dBm/Hz at 1 Hz); or by the noise power in a decade bandwidth (flicker noise has equal power per decade bandwidth). Fig 2.3 displays a typical $1/f$ spectrum.

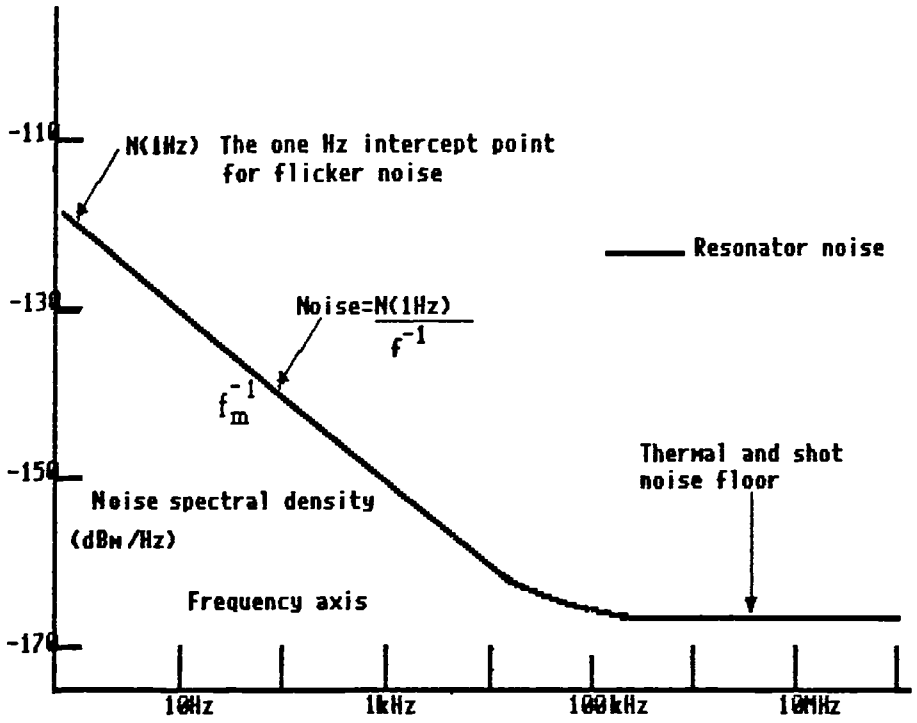


Fig 2.3 Flicker noise in the frequency domain

2.4. Analysis of noise in communication systems

2.4.1. Additive noise

Consideration is now given to the effect of additive noise on communications systems. Additive noise is defined as that produced when a signal is passed through a system and the noise of the system is added with no interaction between signal and noise. Fig2.4 shows noise and a signal carrier.in the frequency domain. Because additive noise power is dependent upon bandwidth, it is convenient to analyse in terms of normalised noise power. This is frequently achieved by normalising it to the power obtained by passing it through a hypothetical filter of equivalent noise bandwidth of 1Hz. At RF, in spectrum analysers for example, practical filters have a bandwidth much larger than 1Hz so the noise may be normalised as:-

$$n_0(1\text{Hz}) = \frac{N_p}{B} \qquad (2.5)$$

where n_o is the noise power in a 1Hz bandwidth, B is the noise bandwidth of the filter and N_p is the total noise power.

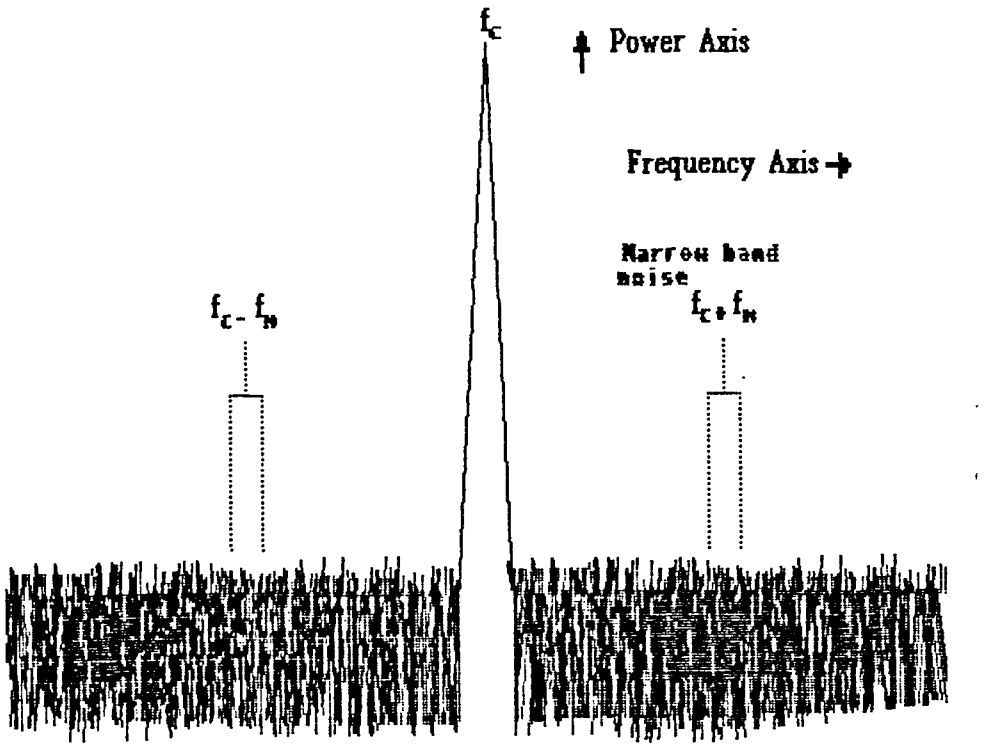


Fig 2.4 Frequency domain representation of a carrier plus additive noise

2.4.2. Modelling additive noise

The effect on the carrier of the noise sidebands can now be studied by considering the nature of the noise passed by a 1 Hz filter. If the filter is placed at a frequency $f_o + f_m$, then for a time interval of much less than 1 second, the noise will behave as a sine wave:-

$$V_n(t) = V_n(0)\sin((f_o + f_m)2\pi t + \phi) \tag{2.6}$$

where $V_n(0)$ is the instantaneous amplitude, and the phase ϕ is uniformly distributed over a long time interval. Therefore, although for times much less than the reciprocal of filter bandwidth there would be little change in ϕ, over a period of time much greater than reciprocal filter bandwidth ϕ will appear to be uniformly distributed. The amplitude V_n will be almost constant over time intervals much less than 1 second and a slow variation in this level will occur for greater periods. The amplitude variation probability density function ($P(V_n)$) follows the Rayleigh distribution curve [Halan, 1974a]:-

$$p(V_n) = \frac{V_n}{\sigma^2}\exp\frac{-V_n^2}{2\sigma^2} \tag{2.7}$$

where V_n is the instantaneous envelope level and σ is the RMS value of the noise. The mean value of the function is $V_n = \sqrt{(\pi/2)}\sigma$. Fig 2.5 displays the Rayleigh distribution curve.

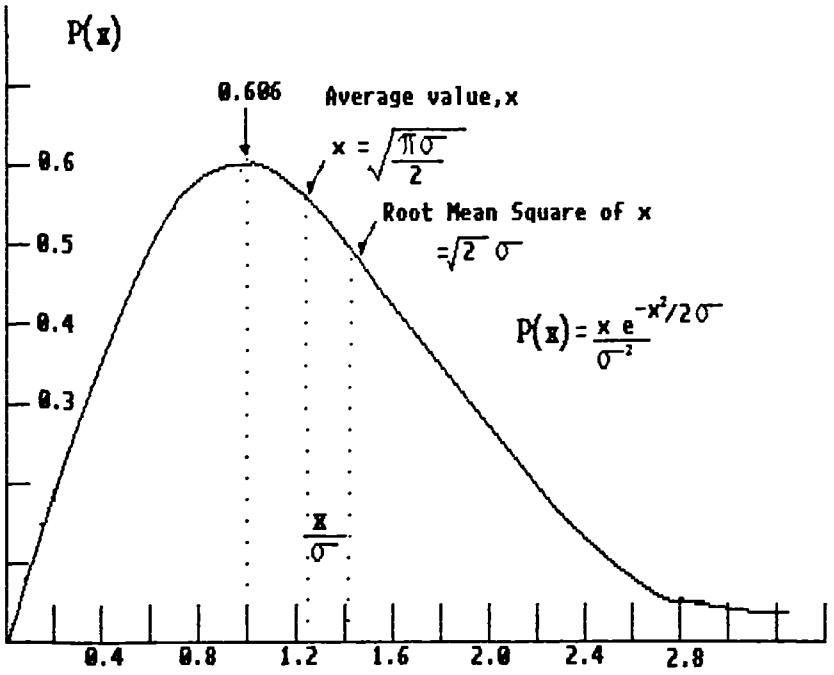


Fig 2.5 The Rayleigh distribution curve

2.4.3. The Ricean Distribution

The Rayleigh distribution is for narrow-band Gaussian noise alone, but if narrow band noise and a carrier are present, the amplitude distribution is described by the Ricean family of curves. If the instantaneous noise and signal amplitude is z and σ is the RMS noise level [Halan, 1974b], then:-

$$p(z) = \frac{z}{\sigma^2}\exp\left(\frac{-1}{\sigma^2}\left(z^2 + A^2\right)I_o\left(\frac{Az}{\sigma^2}\right)\right) \qquad (2.8)$$

where $I_o(x) = \sum_{n=0}^{\infty} \frac{x^{2n}}{2^{2n}(n!)^2}$ (modified Bessel function of zero order),

and A is the amplitude of the carrier wave, $A \sin(2\pi f_o t)$.

Fig 2.6 displays the probability function against amplitude level for the Ricean functions of carrier plus noise. When the carrier amplitude tends towards zero the Ricean distribution tends towards the Rayleigh distribution. Although always greater than the carrier amplitude, the combined mean amplitude approaches the carrier amplitude at high carrier to noise (*C/N*) ratios.

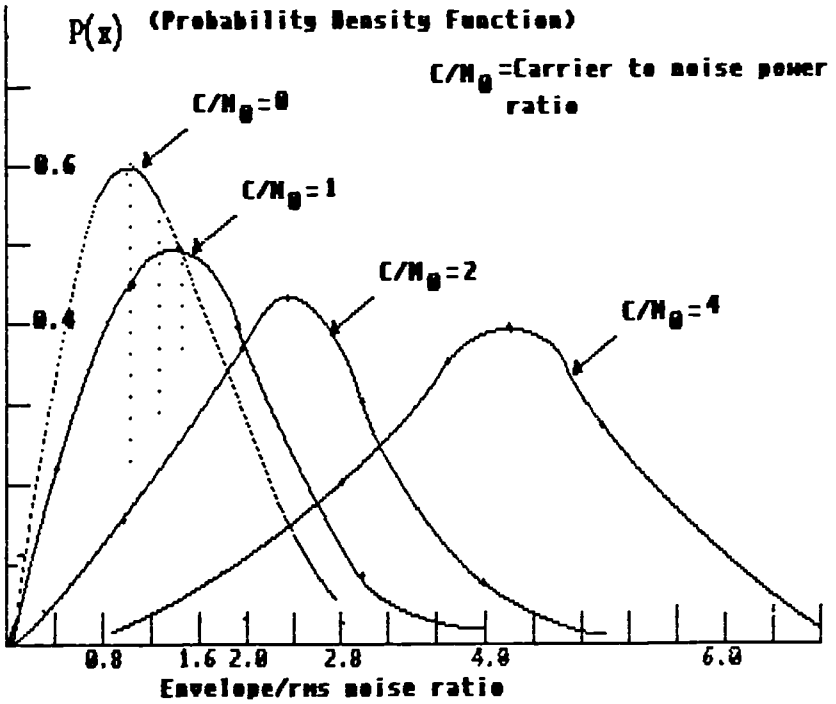


Fig 2.6 The Ricean distribution family of curves for different carrier to noise ratios

Also, at high *C/N* ratios the distribution curve approaches a symmetrical Gaussian distribution centred upon the carrier amplitude. Fig2.7 shows the mean of the amplitude function against carrier to noise and fig2.8 the standard deviation.

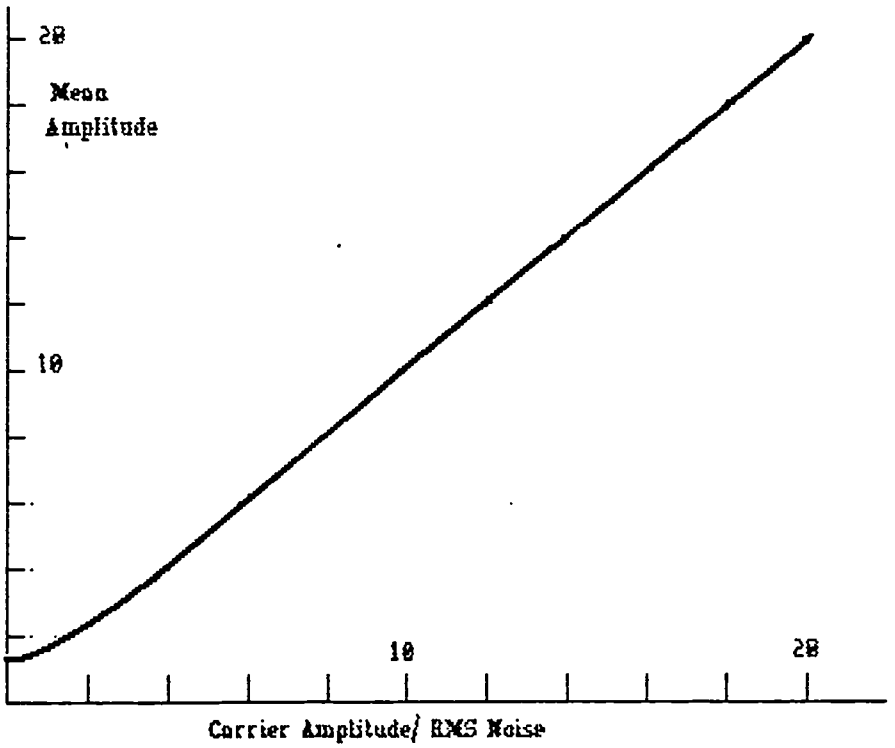


Fig 2.7 Plot of the mean amplitude of carrier plus noise

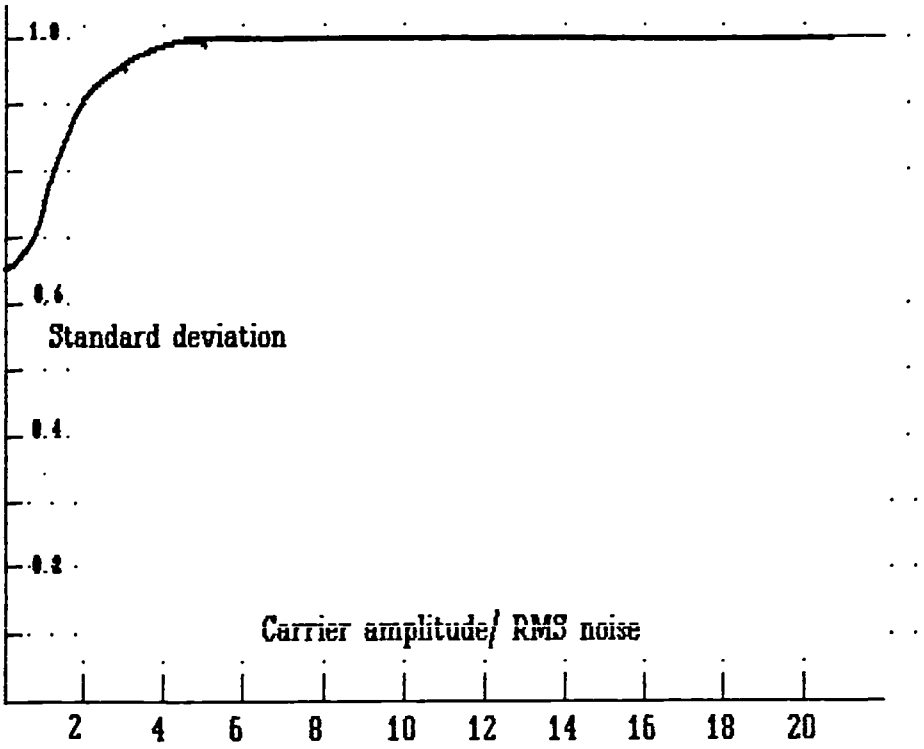


Fig 2.8 Plot of the standard deviation of the envelope against the carrier to noise ratio

The distribution of phase of a carrier plus additive noise is a complicated relationship [Halan, 1974c]. Briefly, the uniformly distributed noise phase function becomes increasingly biased towards the carrier phase as the *C/N* increases. As the carrier becomes much greater than the noise, the phase distribution approximates to a Gaussian distribution around the carrier phase (fig2.9). This suggests that the analysis may be simplified if the sum of the total noise power is much less than the carrier power. In this case the noise can be treated as a continuum of sinusoids placed at small frequency intervals apart. These sinusoids may be considered as separate signals or as modulation sidebands on the main carrier, providing the total power is much less than the carrier power and the law of superposition applies.

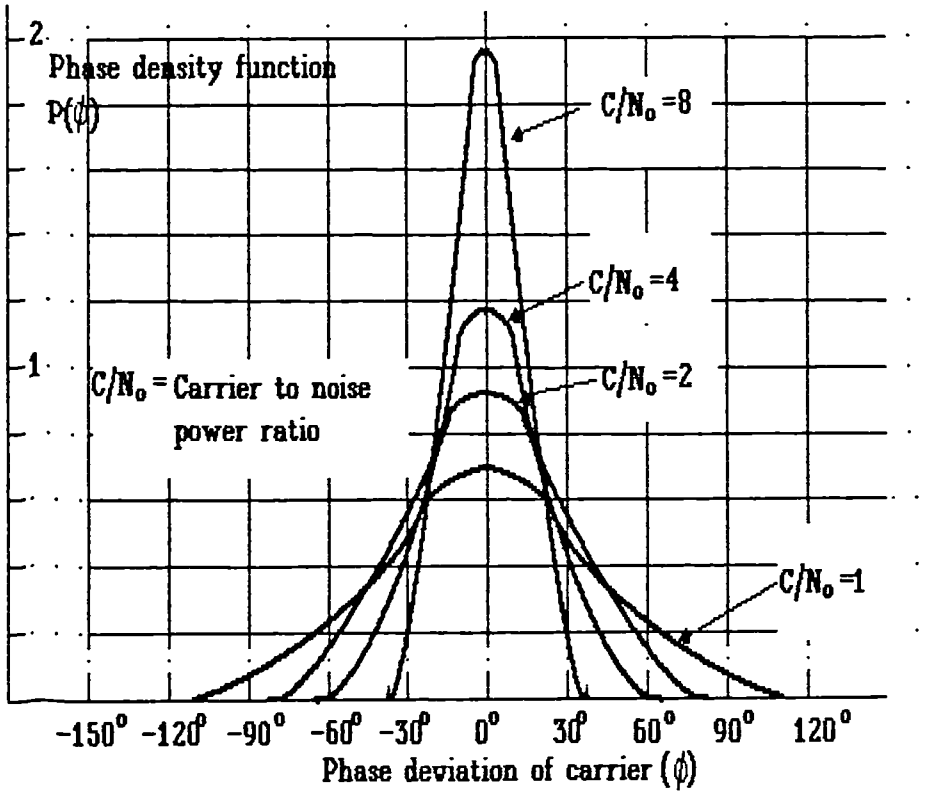


Fig 2.9 Density function of phase for a carrier plus noise

If one of these sinusoids of frequency $f_c + f_m$ is added to a carrier f_c, the result can easily be visualised in vector form as in fig2.10. If the f_c carrier vector is imagined de-rotated (so the whole diagram rotates with angular velocity $2\pi f_o$ rads/s), then the noise vector will rotate around the carrier vector at $2\pi f_m$, or ω_m. It can be seen that there will be simultaneous amplitude and phase modulation of the carrier wave. The amplitude will move between V_c+V_n, and V_c-V_n, where V_c is the carrier amplitude and V_n is the noise amplitude. The phase deviation will vary between $+V_n/V_c$ and $-V_n/V_c$ radians (if $V_n<<V_c$). This is the contribution if a single sideband is considered, but with additive noise, there will also be a sideband at $f_m - f_c$. It was shown earlier that narrowband noise has a Rayleigh amplitude distribution and uniform phase distribution. Therefore for random noise there will be no amplitude correlation between the sidebands. Also the phase relationship will be completely random. This means that the upper and lower sidebands will be completely independent of each other and their only common feature is long term average power, which is equal.

The sidebands of a carrier and additive noise are therefore said to be *non-conformable* [Robins, 1982]. It is this property which distinguishes additive noise from pure amplitude or phase noise.

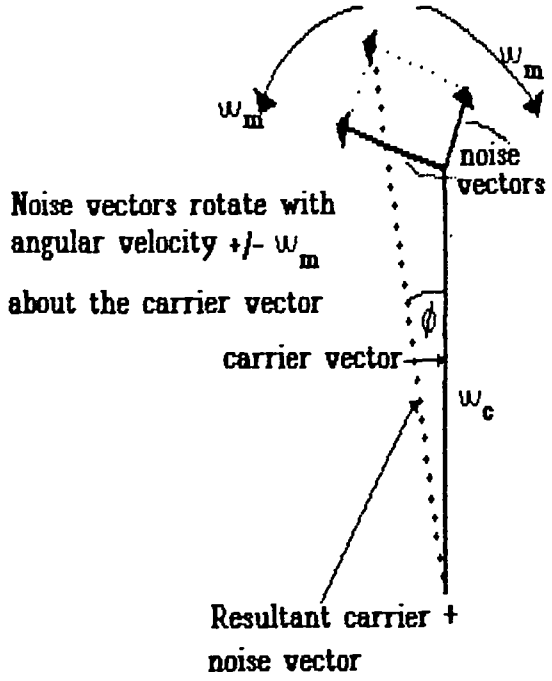


Fig 2.10 Additive noise vectors with the carrier vector de-rotated

2.4.4. Limiters

The creation of phase noise is best studied by considering the action of a pure limiter on a carrier with additive noise. A limiter is represented by the following conditions:-

Input > 0 volts, Output = + volts

Input < 0 volts, Output = - volts

A perfect limiter will therefore remove any amplitude variations in the signal while passing the phase variations unaffected, providing the noise is small in comparison with the carrier.

The general analysis of a narrow band limiter has been derived by Davenport [Davenport, 1953]. At low signal to noise ratios, the noise sidebands interact with each other as well as with the carrier. The approximation that all sidebands can be considered independently is therefore no longer valid. However if the carrier to total noise ratio is moderate, then each 1 Hz sideband can be considered independently as the interaction between them becomes a negligible second order effect. This analysis can be much simplified by considering the noise as a single sideband vector along with the carrier and observing the resultant vector as maintained constant in amplitude, but with the phase variations remaining.

Fig 2.11 illustrates the result in vector form of a carrier and noise sideband. The noise vector will have a uniform distribution of phase with respect to the carrier. As a result of this both amplitude and phase variations will be present in the combined signal. The limiter will remove the amplitude variations. This necessitates the creation of two sidebands in order to cancel out the amplitude variations in the combined signal.

Fig 2.11 shows the effect of additive noise on the carrier, and fig2.12 the resultant vectors after a limiter. This therefore results in two vectors of half the original noise amplitude, rotating at equal angular frequency with respect to the carrier but in opposite directions (so that amplitude variations cancel out).

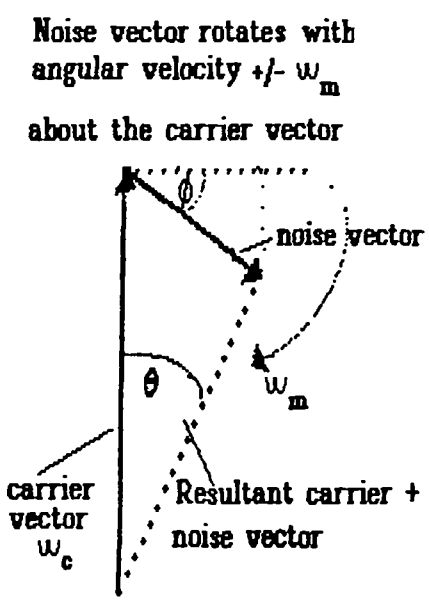


Fig 2.11 Single noise vector with the carrier vector de-rotated

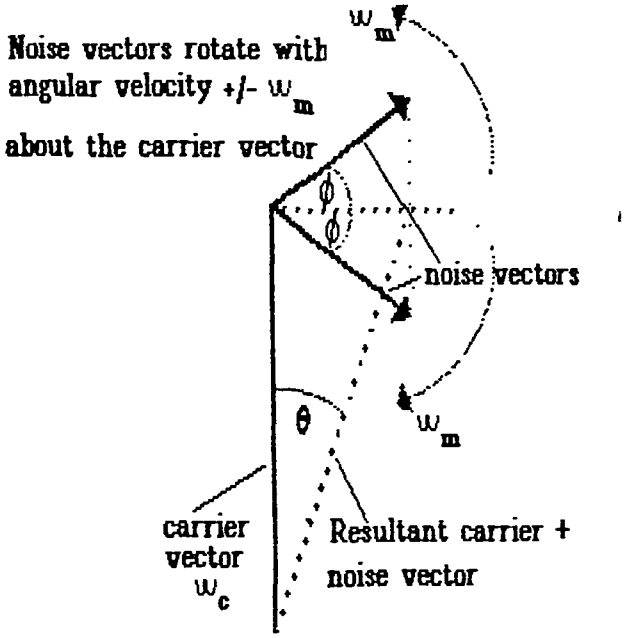


Fig 2.12 Phase noise vectors with the carrier vector de-rotated

The rotating sideband vectors for phase modulation are seen in fig2.12. The amplitude of the phase noise sidebands is half that of the single additive noise sideband before limiting; hence the single sideband of additive noise before a limiter becomes two sidebands of frequency $f_c \pm f_m$ about the carrier, the power of each being 6dB less than the additive noise. If additive noise is present at frequencies f_m about the carrier, the resulting phase noise sidebands will be a power sum of the contributions from the upper and lower additive noise sidebands, resulting in a 3dB reduction in noise sideband power after the limiter.

The resultant noise sidebands will always be equal in amplitude even when considered over small increments in time. The phase relationship of the sidebands will be such that the vectors have equal and opposite angles about the carrier vector. Phase noise sidebands are therefore said to be *conformable*. The above approximation is valid for total signal to noise ratios of down to 10dB. Less than this and the cross products between the noise sidebands result in more noise power density than the 3dB predicted above. Fig2.13 displays limiter noise suppression against carrier to noise ratio.

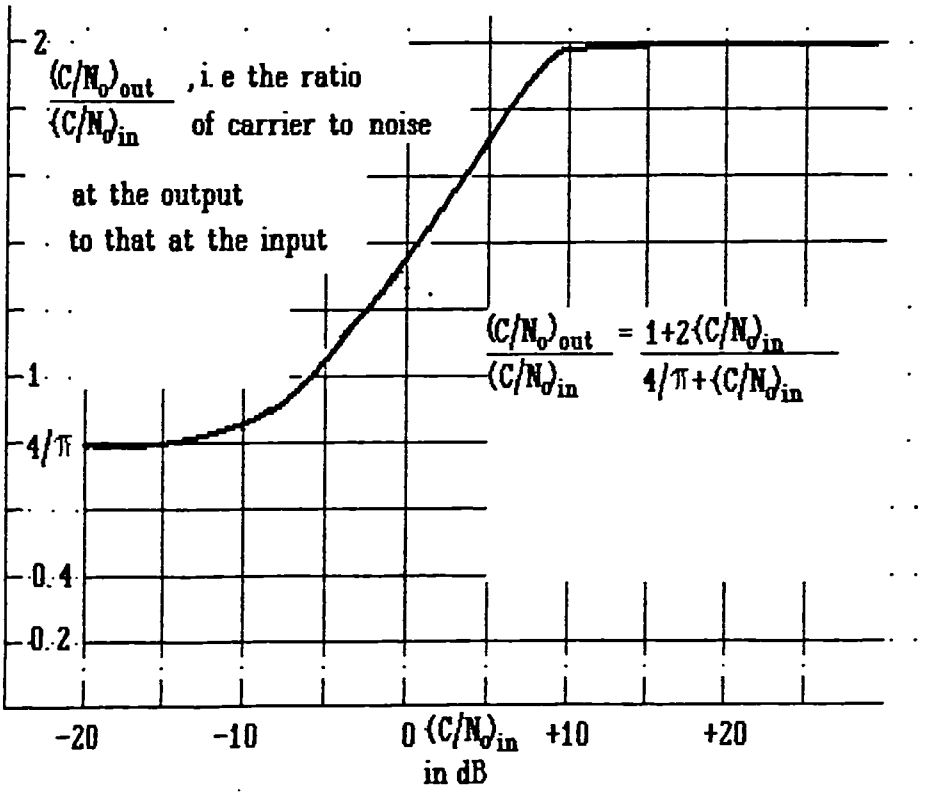


Fig 2.13 The suppression of noise on passing through an ideal limiter

2.5. Phase noise sources within communication systems

2.5.1. Introduction

Phase noise can arise from any of the circuit blocks that make up a typical transmit-receive system. The phase noise generated within a system can have either additive or multiplicative generating mechanisms. Fig2.14 displays the circuit blocks that comprise a

transmitter, and fig2.15 displays the receiver. Principal sources of phase noise are highlighted in bold.

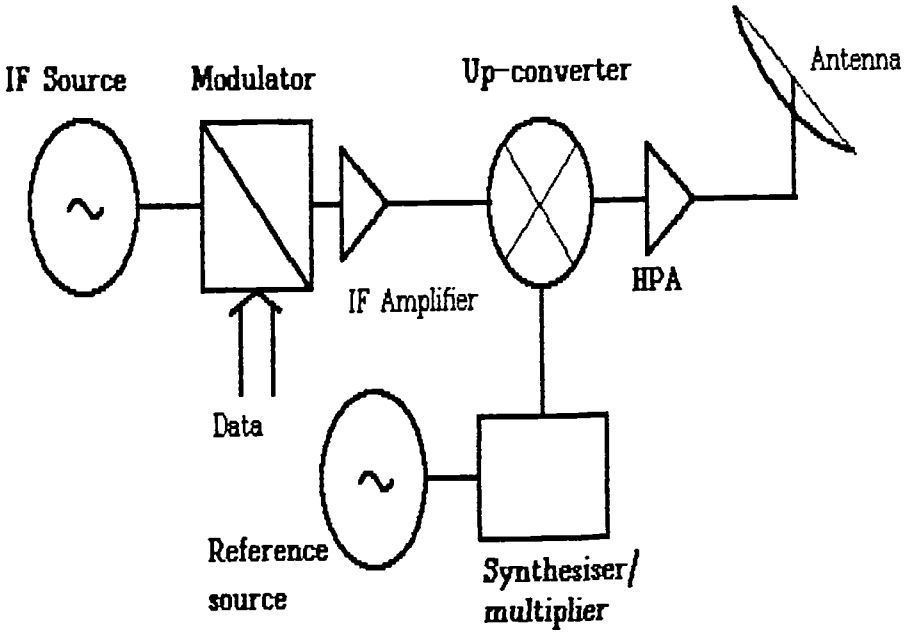


Fig 2.14 Block diagram of simplified transmitter showing principal phase noise sources in bold

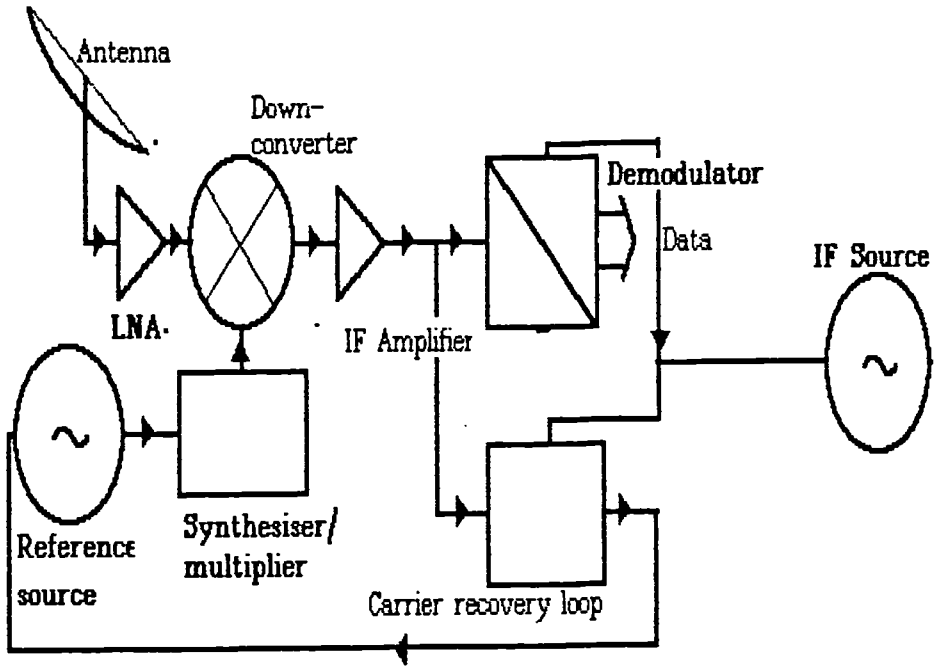


Fig 2.15 Block diagram of simplified receiver showing principal phase noise sources in bold

2.5.2. Phase noise from additive noise

This is generated from broadband noise that is near the carrier frequencies; it is added by simple summation with the carrier, and subsequent limiting removes the AM component (if the signal to noise ratio is good enough). Carrier to phase noise power ratio is proportional to carrier power at point of addition.

2.5.3. Multiplicative sources of phase noise

This occurs when noise that is generated far away from the carrier is allowed to modulate the carrier. Flicker noise (originating at baseband) is an example of the multiplicative effect. Another common multiplicative effect occurs when broadband noise is applied to a non-linear device such as a limiter. A characteristic of multiplicative noise is that the carrier to phase noise ratio is not proportional to carrier power.

2.5.4. Main link phase noise contributors

The main sources of phase noise in a transmit-receive system such as that for satellite communications are:

1) Receiver low noise amplifier;

2) Transmitting power amplifier;

3) Transmitting oscillators;

4) Local oscillator in receiver (particularly the first LO);

5) Transmitting multiplication/synthesis scheme.

Each of these sources adds phase noise and causes degradation of the bit error rate. Such degradation is quantified in chapter 6.

2.5.5. Receiver contribution

The low noise amplifier (LNA) at a receiver input adds thermal noise by an additive process, as already discussed. A common noise figure (NF) at the input is ≈ 2dB for an inexpensive LNA. Any reduction in NF is likely to result in a disproportionate rise in system cost. An increase in signal level at the input to the receiver will improve the carrier to noise power, but this involves an increase in either receive dish aperture, or satellite EIRP. However there is a multiplicative effect taking place that it is not normally considered in system specifications. At Ku band, gallium arsenide MESFETS (GaAs FETS) are typically used, and the nature of these devices is that they contribute considerable $1/f$ noise to the RF input [Motchenbacker & Fitchen, 1973]. This appears as

$1/f$ phase modulation of the input. Such phase noise must therefore be measured as part of the phase noise analysis of the overall system. Satellite transponders similarly tend to employ GaAs FETs and these will also contribute to phase noise. Most published work on GaAs devices concentrate on either the broadband thermal noise of the device as an amplifier, or the flicker noise of the device as an oscillator, but no treatment has been found of the RF flicker noise performance as an amplifier. Such properties of the device are recommended for investigation therefore.

2.5.6. Tx power amplifier effects

Power amplifiers in the satellite are generally travelling wave tubes (TWTs); some earth stations may also employ TWTs for transmission. These add flicker noise by multiplicative conversion effects. The power level in transmitters is too high for additive effects to be important.

2.5.7. Oscillators

A satellite communication system will employ a number of oscillators in signal sources, frequency converters etc. These will all contribute phase noise. Later sections of this thesis examine in detail this contribution, for both crystal oscillators and frequency synthesisers.

2.6. Oscillator performance

2.6.1. Oscillator phase noise as a function of resonator group delay

The block diagram of an oscillator loop is shown in fig2.16. The conditions for maintaining oscillation are:

$$\left| G_{osc} \right| = 1, \qquad \angle G_{osc} = 2n\pi \tag{2.9}$$

where G_{osc} is the oscillator open loop gain.

The phase noise introduced into the oscillator loop can be represented by a phase modulator placed at point A. According to modulation theory the result of a phase perturbation at a modulation frequency ω_m is the appearance of sidebands at $\omega_c \pm \omega_m$. The resonator has associated with it a group delay τ, where:-

$$\tau = \frac{d\theta}{d\omega} \tag{2.10}$$

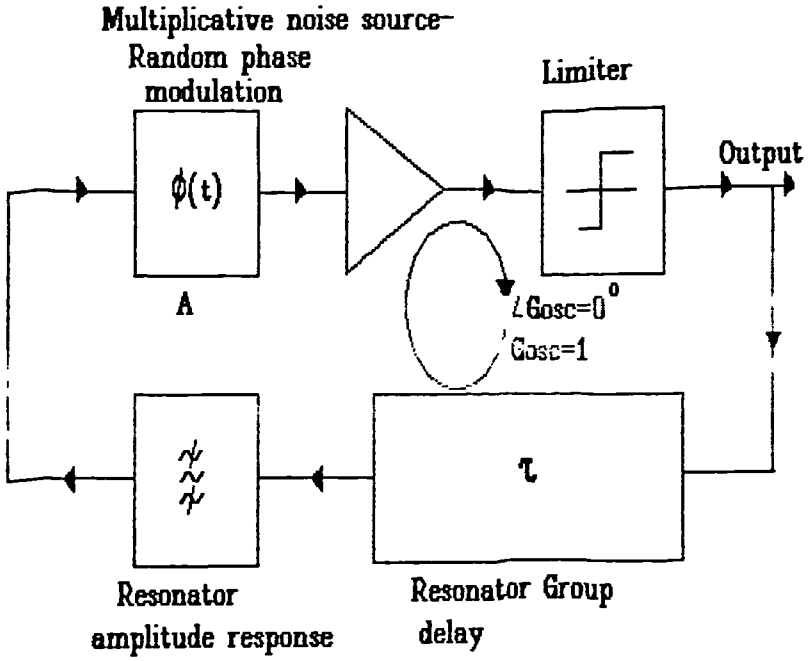


Fig 2.16 Block diagram of an oscillator displaying phase noise multiplication effect

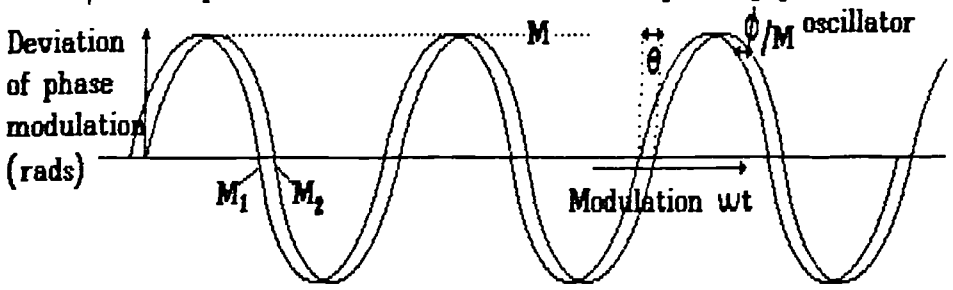
Representations of the phase modulations within the oscillator are displayed in fig2.17. The modulation would therefore create an extra phase shift ϕ at a modulation frequency ω_c. The oscillator must at all times have zero phase shift around the loop. Any phase shift due to the phase noise modulations described above must be cancelled therefore in another part of the loop; the only possible means of achieving this is by means of the group delay of the resonator. Therefore large changes in oscillator closed loop phase occur so that the resonator group delay can provide compensating open loop phase shifts. Inside the resonator bandwidth the attenuation of the fed back signal can be considered to be negligible. It is then possible to calculate the phase modulation at the output of the oscillator providing the following assumptions can be made:-

1) That there is no relative resonator attenuation, ie the offset frequency is within the resonator passband;

2) The resonator group delay results in a small phase shift to the phase modulation, so that small angle approximations can be applied.

θ is a fixed phase shift caused by the resonator group delay to the modulation

ϕ is the phase modulation deviation due to open loop phase noise of the oscillator



A is the peak deviation of the open loop oscillator phase due to noise,

M_1 is the closed loop deviation before the resonator,

and M_2 is the closed loop deviation after the resonator

Closed loop vector diagram for oscillator modulation

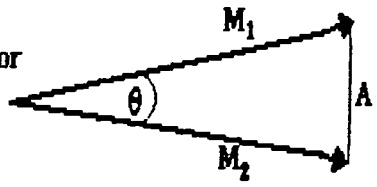


Fig 2.17 Time domain and vector diagrams for oscillator modulation by phase noise

This phase shift is constant, and arises as a result of the time delay through the resonator. The noise modulation is considered to be of such a narrow bandwidth that it can be approximated as sinusoidal in nature. The condition ∠Gosc= n2π must apply to the loop including the noise modulation.

Therefore the phase shift ϕ must be equal to the difference between that appearing at the output of the oscillator and that appearing at the opposite side of the resonator. The resulting magnitude of the phase deviations can be represented by a vector diagram as shown also in fig2.17. *A* is the peak modulation amplitude due to noise and *M* is the magnitude of the oscillator output phase deviation. Therefore the modulation ϕ is given by:-

$$\phi = A \sin \omega_c t = M \sin \omega_c t - M \sin(\omega_c t + \theta) \qquad (2.11)$$

The RHS of (2.11) refers to the difference between the phase modulation at the output of the resonator and that of the input. Expanding (2.11) and applying the following small angle approximations we have:-

$$\begin{aligned} \text{Cos } \theta &\approx 1 \\ \text{Sin } \theta &\approx \theta \\ A \sin \omega_c t &\approx M(\sin \omega_c t - \sin \omega_c t - \{\cos \omega_c t\}\theta) \end{aligned} \tag{2.12}$$

Therefore the relationship between peak deviations is:-

$$A \approx M\theta \tag{2.13}$$

This is the phase shift of the modulation and is due to the time delay (group delay) through the resonator, τ, which is given by $\tau = \frac{d\theta}{d\omega_c}$.

Assuming constant group delay, then:-

$$\tau = \frac{\theta}{\omega_c} \tag{2.14}$$

The group delay of the resonator is determined by its loaded Q, Q_L, and:-

$$\tau = \frac{Q_L}{\pi f_o} \tag{2.15}$$

where f_o is the frequency of oscillation. Equation (2.15) is important as it uniquely defines Q_L.

Substituting (2.14) into (2.15) gives:-

$$\frac{Q_L}{\pi f_o} = \frac{\theta}{\omega_c} \tag{2.16}$$

Far from the carrier, the phase shift at the modulation frequency through the resonator is sufficiently decorrelated so that there is little modification of the phase noise modulation at the output of the oscillator. Consequently, phase noise is now frequency independent and at a level frequently referred to as the 'oscillator noise floor'. This is given by:-

$$A^2 = \frac{kT_n}{2} \tag{2.17}$$

where T_n is the noise temperature of the amplifier input, k is Boltzmann's constant, and A represents the amplitude of the noise modulation. The relationship between the output noise of the oscillator and the input is found from equations (2.13) and (2.16) where M is the closed loop phase deviation of the oscillator:-

$$M = \frac{Af_0}{2f_c Q_L} \tag{2.18}$$

The peak deviations can be converted to noise power densities by squaring. In terms of phase noise power density to carrier ratio $\mathcal{L}$ (f), the oscillator noise can be expressed as (2.19), assuming thermal noise only is present:-

$$\mathcal{L}(f) = \frac{kT_n}{2} \cdot \left(\frac{f_0}{2f_cQ_L}\right)^2 \qquad (2.19)$$

giving the relationship quoted by Leeson [1966].

Therefore for $f_c < f_o/2Q_L$ the noise side band power is raised by a factor $\left(\frac{f_0}{2f_cQ_L}\right)^2$ [Leeson, 1966] giving:-

$$\mathcal{L}(f) = \mathcal{L}(\infty)\left(\frac{f_0}{2f_cQ_L}\right)^2 \qquad (2.20)$$

where $\mathcal{L}(\infty)$ is the broadband phase noise floor within the loop.

2.6.2. Spectral shape of oscillator sidebands

The spectral shape of the oscillator sidebands can be determined from equation (2.19). The amplifier spectrum, as discussed elsewhere is multiplied by the factor $\left(\frac{f_0}{2f_cQ_L}\right)^2$. For offset frequencies less than $f_o/2Q_L$, this factor has a reciprocal square relationship with frequency. This means that when the phase noise is plotted on a logarithmic offset frequency axis, the slope of the graph is changed by a factor -2. The spectral shape is modified depending on whether the $1/f$ corner frequency f_c is less than or greater than the resonator half bandwidth frequency. This explains the commonly observed f^{-2} or f^{-3} curves. These curves are shown in §3.3.4.

In addition, crystal and SAW oscillators can show an f_c^{-4} slope very close to the carrier known as the "random walk" effect [Parker, 1986]. The f_c^{-4} slope can also occur further out from the carrier if any of the following occur:-

1) coincident spurious modes;

2) burst noise (in drastic cases).

2.7. Frequency synthesis

2.7.1. Introduction

Frequency synthesis is considered to be necessary for the receiver local oscillator to enable versatile re-allocation of channels. There are two fundamental methods of frequency synthesis, the incoherent and coherent methods [Mannassewitch, 1976a]. The incoherent method depends upon heterodyning a bank of reference oscillators whereas the coherent method derives the frequency from a single reference source. The requirement for a multiplicity of highly stable and therefore expensive reference oscillators for the incoherent approach favours the second approach for data systems, although the first approach may give phase noise benefits (see §5.7.5). The coherent approach can be further sub-divided into the following four categories:

1) Direct synthesis;

2) Indirect synthesis;

3) Numerically controlled oscillator (or Direct Digital synthesis);

4) Hybrid synthesis.

Each of these approaches has its particular drawbacks and advantages which depend upon the application. Therefore a complete survey of these is necessary and synthesiser design is discussed in more detail in chapter 4.

2.7.2. Penalties resulting from use of a synthesiser

In addition to the $20\log N$ degradation of the reference oscillator, excess noise may also be added by signal processing circuitry within a synthesiser. The properties of the reference oscillator would be degraded by the synthesiser processing circuitry. The two particular problems likely to be created are:-

1) Phase noise;

2) In-band unwanted discrete carrier signals (spurious signals).

The first of these is random in nature, whereas the second is deterministic.

Phase noise arises from noise sources in the synthesiser processing circuitry, and from any subsidiary oscillators used. This has been described as "excess" or "residual" noise, as it is additional to any noise generated by the reference source [Mannassewitch, 1976b]. In many inexpensive frequency synthesisers where the design is not specified for data communications, this noise would be far in excess of that for reliable data reception [Wilson, & Tozer, 1989].

In band spurious signals can take the following forms:-

1) Mains related spurious signals;

2) Unwanted harmonics of the synthesiser reference frequency;

3) Spurious mixing products.

Close to carrier spurious sidebands have the same effect as phase noise in that carrier jitter is the result at the demodulator. Far from carrier spurious sidebands have the effect of reducing the dynamic range of the system. If the spurious signal is at a high enough level, then false locking onto the spurious signal is possible, as is the reception of interfering signals at unwanted frequencies. In the case of transmitters, the spurious signals could result in interference to other links on other frequencies. Chapter 4 of this thesis deals with synthesiser design considerations in some detail.

2.8. Summary

The mechanism by which phase noise originates from additive noise has been shown. A distinction has been made between phase noise originating from additive noise and multiplicative noise effects. The problem of flicker noise has been raised. It has been shown how these effects contribute to the overall shape of typical local oscillator sidebands.

2.9. Further work

There is a requirement for an investigation of the flicker noise characteristics of travelling wave tube amplifiers and GaAs FET amplifiers.

2.10. References

Betts, J.A. 1983 *Signal processing, modulation and noise* , chap. 8, p188. Unibooks.

Davenport, W.B. Jr. June 1953 Signal to Noise ratios in bandpass limiters. *J. Applied Physics.* **24**, 720-727.

Feher, K. 1981, *Digital Communications*, chap.1, p. 40. NJ:.Prentice Hall.

Halan, W. 1974a *Detection of Signals in Noise.* p. 102 Academic Press, New York.

Halan, W. 1974b *ibid* p. 105

Halan, W. 1974c *ibid* p. 107

Leeson, D.B. 1966 A simple model of Feedback Oscillator noise spectrum. *Proceedings of the IEEE.* pp. 329-330

Mannassewitch V. 1976a *Frequency synthesis theory and design*, chap1 p. 7. Wiley.

Mannassewitch V. 1976b *ibid.* p. 108

Motchenbacker, C.D. & Fitchen, F.C. 1973 *Low noise electronic design,* p. 67. Wiley.

Parker T.E. 1986, Random Walk frequency fluctuations in SAW oscillators *40th Annual Frequency Control Symposium.* p. 241.

Robins, W. 1982 *Phase noise in signal sources*, Peter Peregrinus chap1 p. 14.

Van der Ziel, A. (b) *ibid* chap 6 p. 111.

Van der Ziel, A. 1986a *Noise in Solid State Devices and Circuits*, chap5 p. 64. Wiley NY

Wilson, M.P. & Tozer, T.C. 1989 Synthesisers for low data rate satellite receivers. *IEE Second Frequency Control and Synthesis Symposium.* Conference Paper Number 303.

3 *Flicker, Phase, and Frequency Noise in RF Systems*

3.1 Introduction

This section further examines the origins of phase noise and related phenomena. Some aspects are discussed which, though not normally considered, may result in increased levels of phase noise.

A fundamental source of phase noise is flicker noise. Although flicker noise is a low frequency phenomenon, there are mechanisms which result in its appearance at RF, around the carrier frequency. The mechanism by which it appears is not as simple as that for additive white Gaussian noise (AWGN) and is the subject of much contention. The fact, however, that the noise power is concentrated close to the carrier frequency has implications for low data rate systems. There is a case, therefore, for further investigation into this subject. The noise can originate in both reference and synthesiser oscillators. The $1/f^3$ reference oscillator noise sidebands originate mainly in the resonator; for the synthesiser, the shape is $1/f^3$ and is determined by the active components. There is relatively little information available on this topic, and attempts are made to develop it in this thesis.

In the case of crystal oscillators it has often been assumed that the responsibility for reducing the effect of flicker noise rested with the oscillator circuit designer; however, it has more recently become appreciated that flicker noise within the resonator itself may dominate the output spectrum [Moulton, 1986].

3.2 Phase noise generation in amplifiers

3.2.1 Transistor amplifier noise sources

Initially, it is instructive to consider a transistor amplifier. The overall noise generated within a transistor amplifier has many origins. In a typical transistor amplifier, there are several noise sources; Johnson and shot noise are both white noise sources and give the device its noise figure throughout the RF regions. The principal source of Johnson noise is in the base spreading resistance of the transistor ($r_{bb'}$), while shot noise is due to DC current flow in the device.

An equivalent circuit of a bipolar transistor displaying these noise sources is shown in fig 3.1. The symbols pertaining here are [Motchenbacker & Fitchen, 1973]:-

γ	=	constant exponent in the flicker noise model
α	=	frequency exponent in the flicker noise model (approximately unity)
B_o	=	transistor current gain
q	=	electronic charge
$r_{bb'}$	=	base spreading resistance
r_b	=	1/f component of base spreading resistance
$r_{b'e}$	=	equivalent base-emitter resistance
I_c	=	collector current
I_b	=	base current
T	=	temperature in Kelvin
k	=	Boltzmann's constant
R_s	=	source resistance

The equivalent noise input to the device is [*ibid*]:-

$$E_{ni}^2 = 4kT(r_{bb'}+R_s) + 2qI_b(r_{bb'}+R_s)^2 + 2qI_c\left(\frac{r_{bb'}+R_s+r_{b'e}}{\beta_o}\right)^2$$

Johnson Noise *Base Shot Noise* *Collector Shot Noise*

$$+ \left(\frac{2qf_cI_b^{\gamma}(R_s+R_b)^2}{f^{\gamma}}\right) + 2qI_c(r_{bb'}+R_s)^2\left(\frac{f}{f_T}\right)^2 \qquad (3.1)$$

Flicker Noise *Collector Shot Noise HF Roll-off*

Some of these components are discussed below.

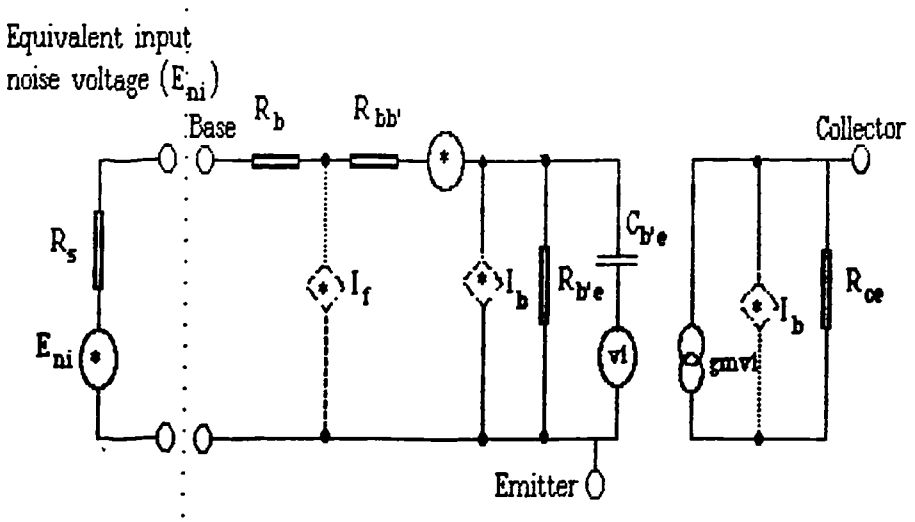


Fig 3.1 Equivalent circuit of bipolar transistor showing noise sources

3.2.2 Flicker or 1/f noise

Flicker noise is the least understood aspect of the noise sources, with its effects not as well defined and documented as the white noise sources. Some of the effects may be determined by fundamental laws of physics (as in Johnson noise), while others vary between different devices and manufacturing processes. A typical flicker phase noise plot for an amplifier is displayed in fig3.2. Flicker noise may be normalised to a 1Hz intercept point n_o (1Hz).

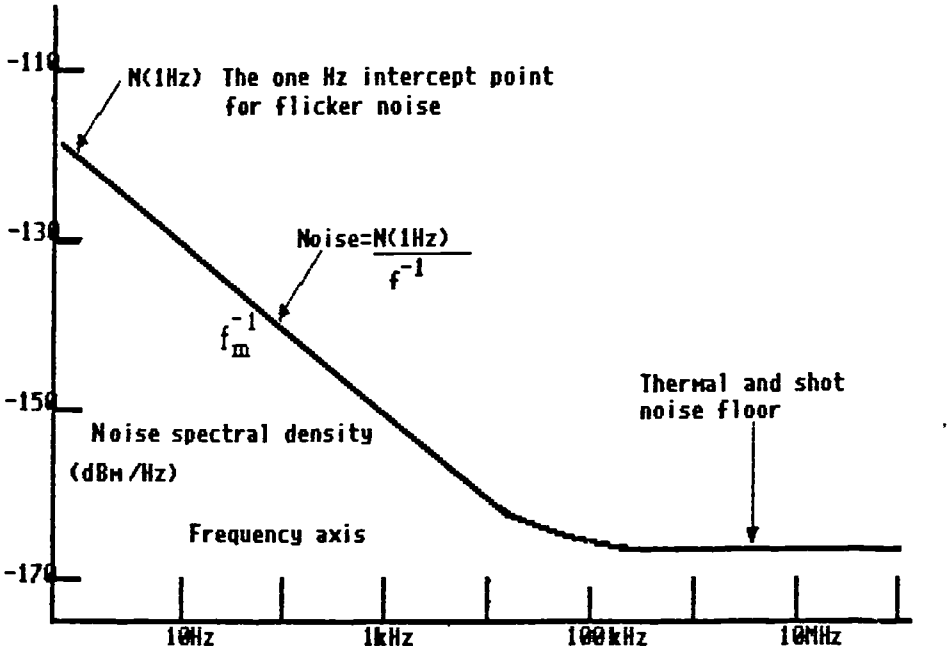


Fig 3.2 Flicker noise in the frequency domain

Flicker noise has been ascribed to surface effects within devices because [Buckingham, 1983a]:-

a) Junction field effect transistors, which are predominantly bulk effect devices, show a reduced level of flicker noise;

b) Bipolar devices having their base emitter junction operating in reverse zener breakdown mode show an increased 1/f noise level.

Voltage breakdown of a bipolar device emitter-base junction releases "hot" (high energy) electrons into the oxide layer of the device, resulting in increased surface layer currents in the device, and increased flicker effects. However junction FETs are not immune to this effect, indicating that there may be a bulk effect also. Another theory relates 1/f noise to stresses within the device crystal lattice [Buckingham, 1983b]. These stresses create traps which hold and release charge carriers with a time delay that is 1/f in spectral response. This effect is very pronounced in Gallium Arsenide, which, due to the nature of the atoms which make up the compound and the doping, has a highly stressed lattice [Pucel, 1986].

3.2.3 Flicker noise at RF

The output of an RF amplifier has a phase noise spectrum consisting of additive white noise and multiplicative $1/f$ noise. Fig 3.3 shows a display of the phase noise spectrum of a carrier after passing through an undegenerated transistor amplifier, as would be seen on an ideal spectrum analyser with infinite dynamic range and 1 Hz resolution bandwidth. If germanium or silicon devices are used in the RF amplifier, then it has been found that the level of $1/f$ phase noise at RF is not dependent upon the device used (as opposed to at baseband [Halford, 1967]).

There are two principal multiplicative mechanisms by which flicker noise could be introduced to the RF spectrum:-

i) Non linear upconversion by intermodulation effects (analogue multiplication mixing effects);

ii) Phase modulation by non-static device parameters.

If non-linear upconversion by analogue multiplication is the dominant mechanism, then the flicker phase noise would be drive level dependent. This is because a variable level carrier is used in the mixing process. However experimental evidence reveals a constant level of flicker noise when the signal level is varied over a range of 30 to 40dB [Moulton, 1985] and would tend to indicate that phase modulation effects are responsible.

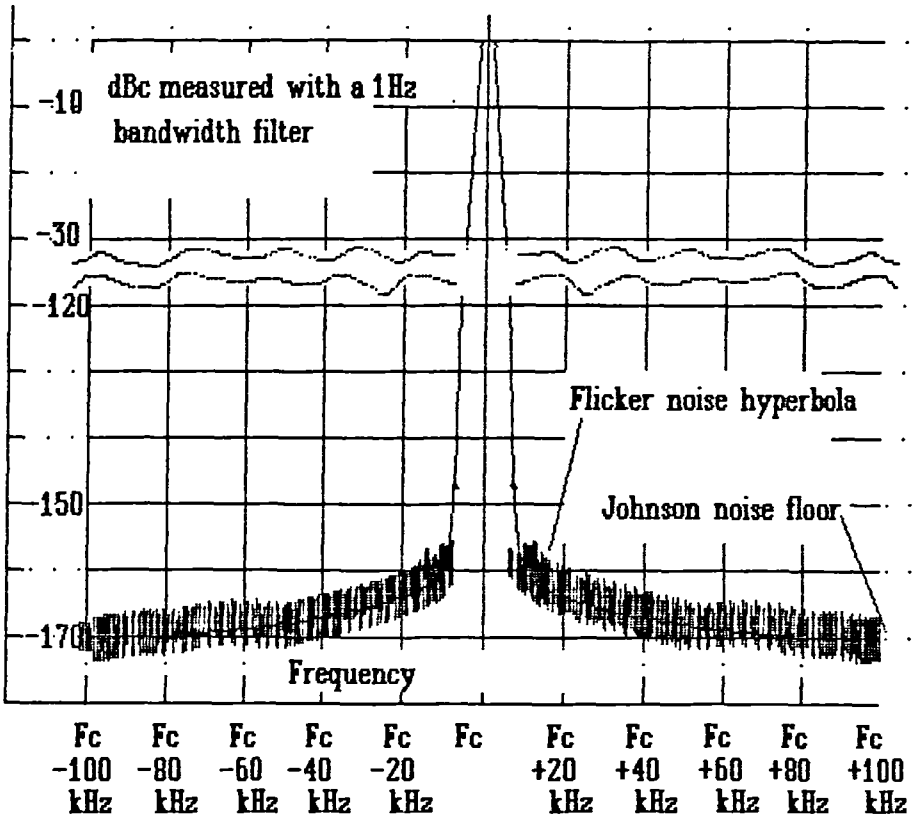


Fig 3.3 A plot of flicker phase noise in the frequency domain after amplification by an undegenerated transistor amplifier

Fig 3.4 shows a plot of phase noise introduced by a single transistor amplifier with and without emitter degeneration.

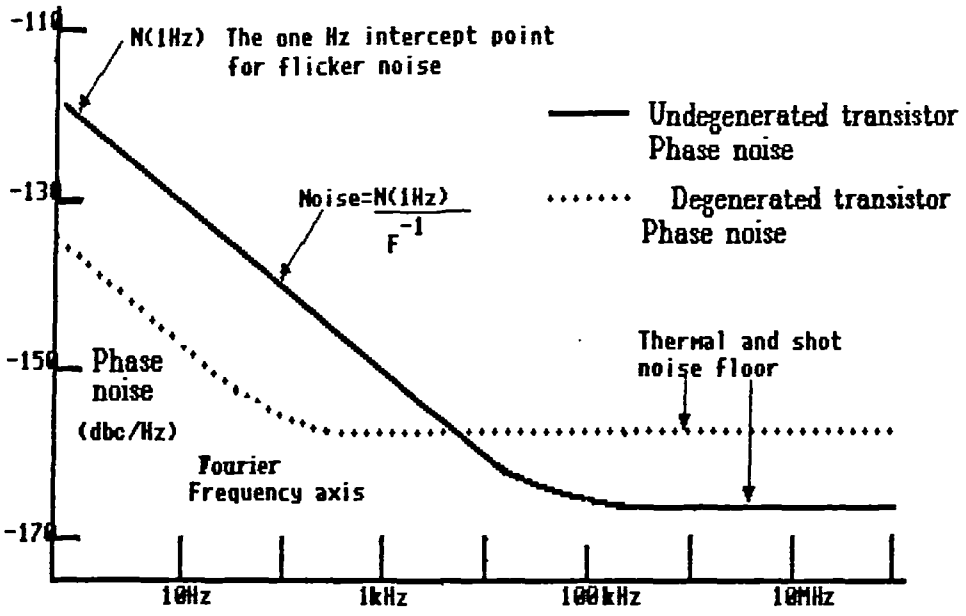


Fig 3.4 Plot of transistor amplifier phase noise levels (silicon bipolar)

Fig 3.5 shows simplified circuit diagrams of the amplifier.

Fig 3.5a Simplified transistor amplifier with no emitter degeneration

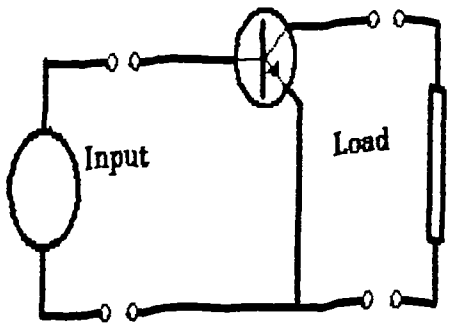
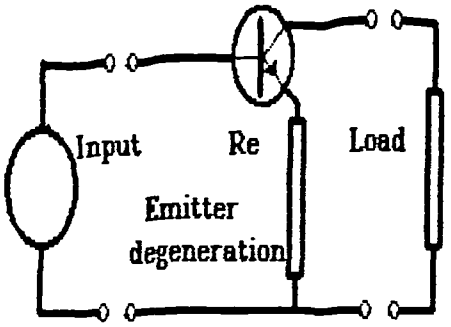


Fig 3.5b Simplified transistor amplifier with emitter degeneration



Emitter degeneration is a very effective form of RF feedback, frequently used to reduce performance dependence upon transistor parameter variations. Fig 3.6 indicates the parameters that could be involved in producing the phase modulation effect. The transistor parameters R_b(base resistance), g_m(mutual conductance), C_{be} and C_{cb} (emitter-base and collector-base junction capacitances) tend to fluctuate about their average values, thus causing phase modulation of the carrier. In small signal amplifiers the effect is 20-30 dB higher than upconverted $1/f$ noise [Muat, 1986a]. The $1/f$ intercept point has been measured to be approximately -120 dBc/Hz at 1 Hz offset. This has been observed [Muat, 1986b] to be constant over the RF region from HF to mid UHF (700 MHz). The effect of R_b and g_m could explain the constant phase modulation effect. The effect of junction capacitance C_{cb} and C_{be} would result in increased flicker noise at higher frequencies. The effect of adding the emitter resistor results in g_m being determined by the resistor, providing its conductance is much less than the g_m of the transistor. Thus it would be expected that flicker noise variations in g_m would be much reduced in the degenerated case. In fact, due to the application of emitter degeneration, up to 40dB reduction in flicker noise in the VHF region can be achieved [Kroupa, 1973]. This is as a result of circuit dependence upon the external emitter resistance rather than g_m. However, the resistor increases the Johnson noise floor as can be seen in fig 3.4.

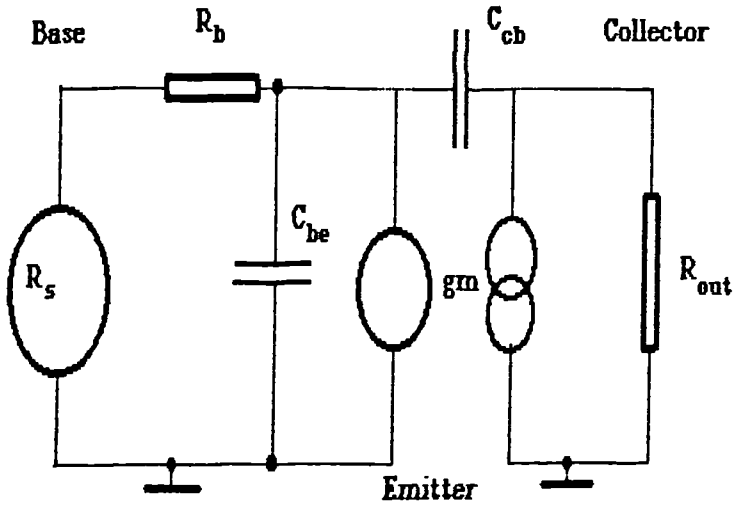


Fig 3.6 Equivalent circuit of transistor showing parameters subject to flicker noise

3.3 Phase noise generation in oscillators

3.3.1 Resonators

The thermal noise and flicker noise effects present in amplifiers also occur in oscillators. However in addition to this, there is also a flicker noise contribution from the resonator.

To appreciate the need for a resonator element, we need to consider the Barkhausen criterion for maintaining oscillation, which is:

$$|G_{osc}| = 1$$
$$\angle G_{osc} = n2\pi \qquad (3.2)$$

where G_{osc} is the gain of the oscillator loop and $\angle G_{osc}$ indicates the loop phase shift. In addition to this, for maximum oscillator stability:-

$$\frac{\delta}{\delta\omega}(\angle G_{osc}) = \text{max possible} \qquad (3.3)$$

In addition to the loop gain requirements for oscillation, there must also be some frequency selection within the loop. If this is not the case then unstable oscillations will result as in fig3.7 [Boyles, 1986]; this can typically occur if two phase-frequency characteristics oppose each other within the oscillator loop.

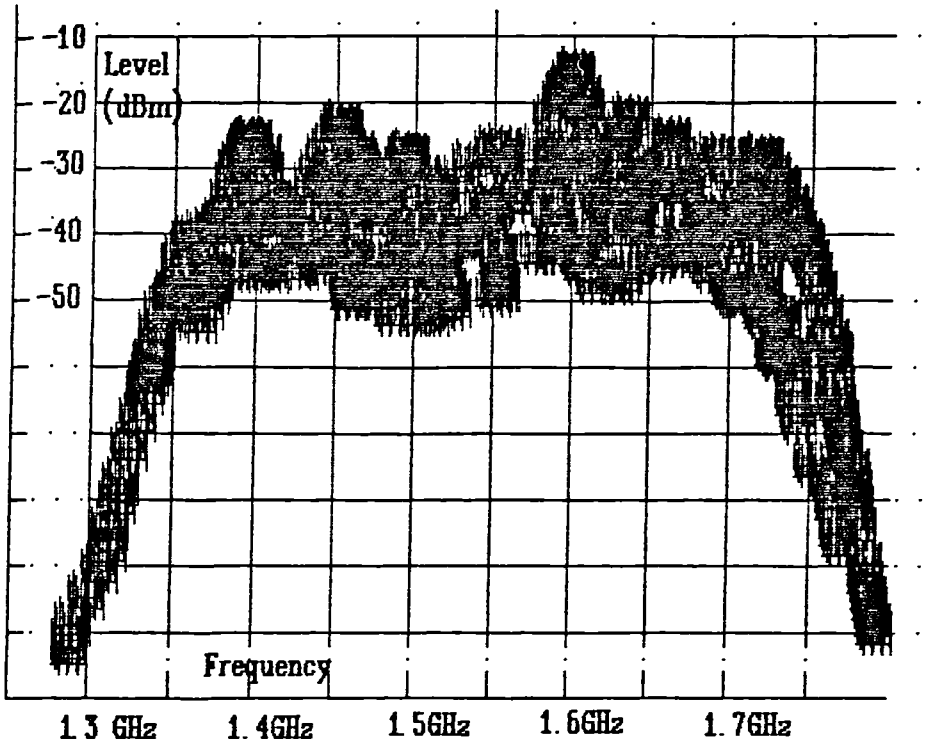


Fig 3.7 A typical oscillator spectrum if no frequency selectivity exits within the oscillator loop

Oscillator frequency selection is usually provided by means of a resonator with group delay, Γ. Fig 3.8 shows a block diagram of an oscillator loop, displaying the sources of noise within the loop. These sources could be either additive thermal noise or multiplicative $1/f$ noise. Although the oscillator does respond differently in each case, it is convenient to consider the noise as random phase modulation within the loop. The oscillator noise spectrum is derived by considering the resonator to have a group delay Γ which is related to its loaded Q (Q_L) by the expression:-

$$\Gamma = Q_L/\pi f_o \qquad (3.4)$$

This gives a result that is accurate for offset from carrier frequencies << the resonator half bandwidth frequency $f_o/2Q_L$. Consequently the noise is raised by a factor:

$$\mathcal{L}_{cl}(f) = \mathcal{L}_{ol}(f)\frac{f_o^2}{(f_m Q_L)^2} \qquad (3.5)$$

where $\mathcal{L}_{ol}(f)$ is the oscillator open loop phase noise, and $\mathcal{L}_{cl}(f)$ is the closed loop noise.

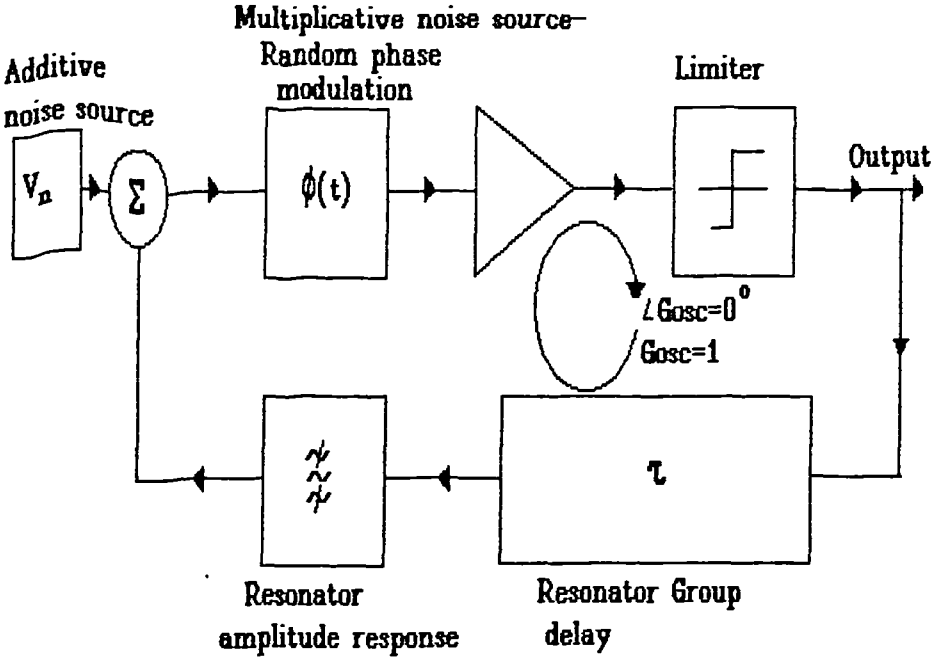


Fig 3.8 Block diagram of an oscillator displaying phase noise sources

3.3.2 Additive noise

If a limiter is present in the circuit, then the amplitude variations due to additive noise (Johnson or Shot) will be removed, provided that there is no AM to PM conversion within the limiter. The effective phase noise contribution of the thermal noise is reduced by 3dB compared with that resulting if all the thermal noise power consisted of phase noise. The phase noise sideband power level $\mathcal{L}(f)$ is dependent upon the carrier to additive noise power ratio at the effective noise summing point.

The formula for additive oscillator phase noise is:-

$$\mathcal{L}(f_m) = \frac{kT_n f_o^2}{8Cf_m^2 Q_L^2} \qquad (3.6)$$

3.3.3 Multiplicative noise

The effect of multiplicative noise is as if random phase shifts were introduced into the oscillator loop equal in value to the noise level. Such noise generally has a $1/f$ relationship with offset from carrier frequency, close to carrier, and is independent of carrier power level within the oscillator. Since this noise is effectively phase noise, no 3dB reduction occurs as with additive noise.

The phase noise contribution from multiplicative noise is therefore:-

$$\mathcal{L}(f_m) = \frac{f_o^2}{4Q_L^2 f_m^2}\frac{\mathcal{L}(f_o)}{f_m} = \frac{f_o^2}{4Q_L^2}\frac{\mathcal{L}(f_o)}{f_m^3} \qquad (3.7)$$

where $\mathcal{L}(f_o)$ is the phase noise at 1 Hz offset from carrier of the oscillator circuit measured as an open loop two port device. It can be noticed that the phase noise sideband power possesses an inverse cubic relationship with offset frequency.

The phase noise sideband power is independent of where the signal is removed from the oscillator if $f_m << f_o/2Q_L$. However, if the noise sidebands at f_m are greater than the half power bandwidth, then the sideband power depends upon which point is used to extract the signal.

3.3.4 Spectral Shape

The typical spectral shape of an oscillator with $1/f^3$ phase noise sidebands is displayed in fig 3.9 as would be shown on a spectrum analyser screen. In addition to the steeply rising sidebands it can be noticed that the tip of the display is diffuse. This is due to the fact that the actual frequency of oscillation is non stationary, an important characteristic of this phenomenon.

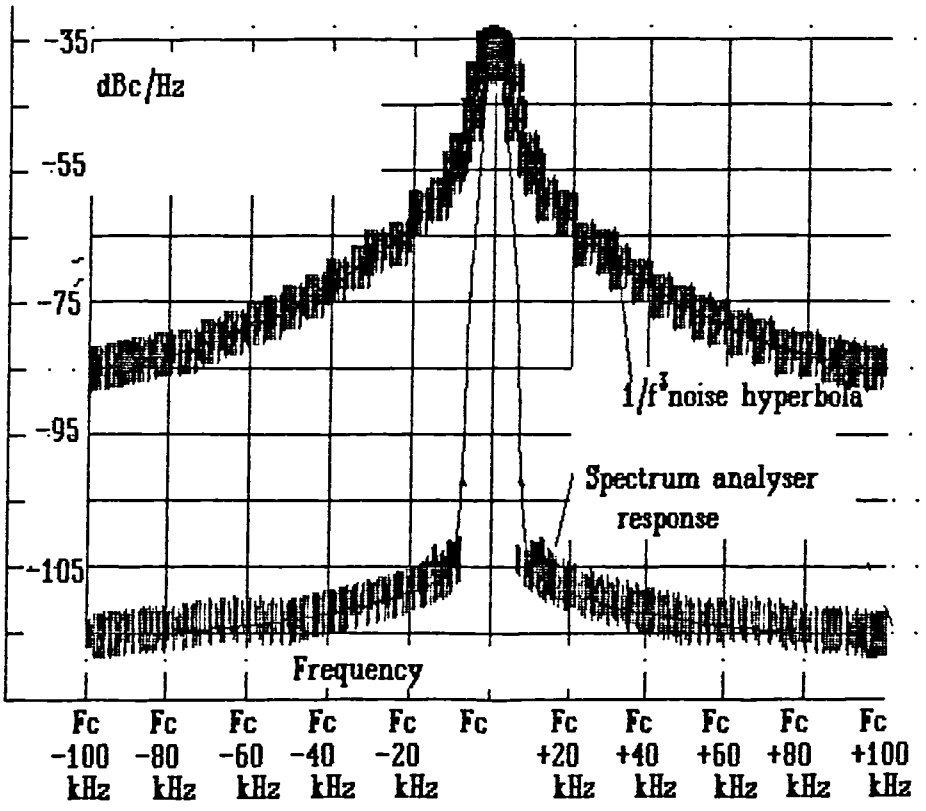


Fig 3.9 Flicker noise effects within an oscillator

If the phase noise sidebands are plotted on logarithmic scales, then the gradient is increased by a factor -2 over the open loop gradient, for offset frequencies $< f_o/2Q_L$ due to the factor:

$$\mathcal{L}_{cl}(f) = \mathcal{L}_{ol}(f) \frac{f_o^2}{(f_m 2Q_L)^2} \tag{3.8}$$

where $\mathcal{L}_{ol}(f)$ is the oscillator open loop phase noise and $\mathcal{L}_{cl}(f)$ is a closed loop phase noise as mentioned earlier. Consequently, close to carrier phase noise follows a $1/f_m^3$ spectrum as commonly observed in oscillators. This theory is developed further in §5.6.2.2 in order to deal with the case of an injection locked oscillator.

Figs 3.10 & 3.11 display two commonly observed oscillator sideband spectra.

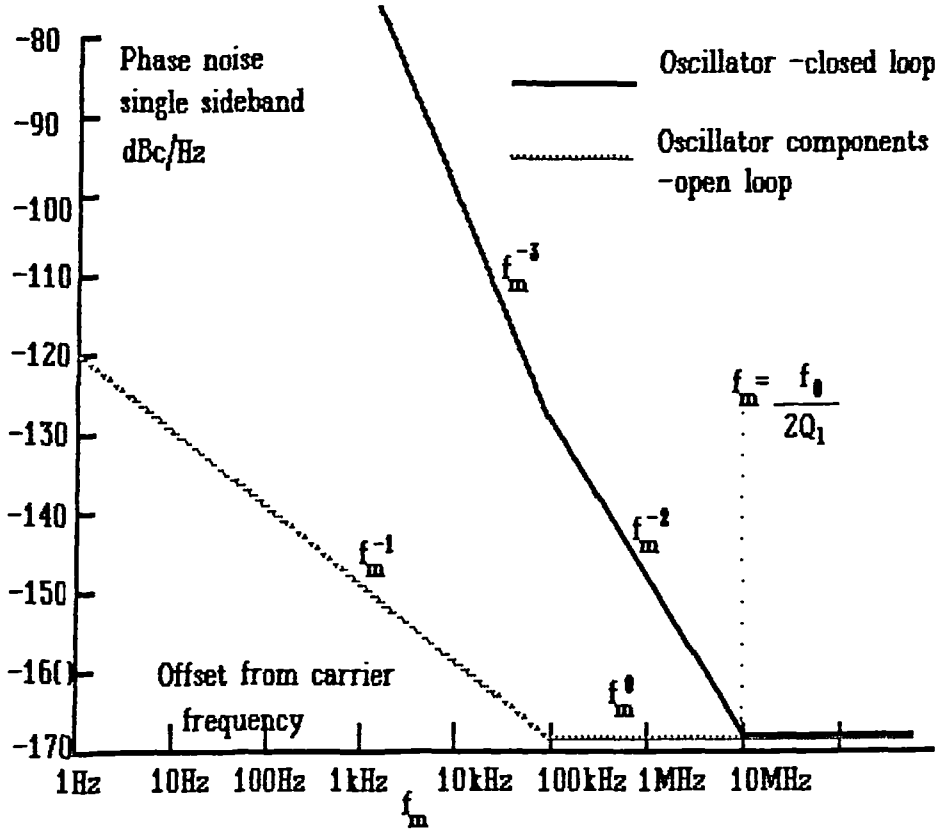


Fig 3.10 Logarithmic phase noise sideband characteristic - low Q case

The first instance is for a low Q resonator oscillator, such as a Voltage Controlled Oscillator (VCO). In this case the frequency where the $1/f$ noise spectrum becomes less than the white noise spectrum, f_α, is less than the resonator half power bandwidth $f_o/2Q_L$. Consequently, the spectrum has the following asymptotes:-

$$f_m^{-3} \quad (f_m < f_\alpha)$$

$$f_m^{-2} \quad (f_\alpha < f_m < f_o/2Q_L) \qquad (3.9)$$

$$f_m^{0} \quad (f_m > f_o/2Q)$$

For the case of a high Q resonator such as a crystal oscillator, the f_α point is greater than the resonator half bandwidth point, and the noise contribution from the amplifier displays the following asymptotes:-

$$f_m^{-3} \quad f_m < f_o/2Q_L$$

$$f_m^{-1} \quad f_o/2Q_L < f_m < f_\alpha \qquad (3.10)$$

$$f_m^{0} \quad f_m > f_\alpha$$

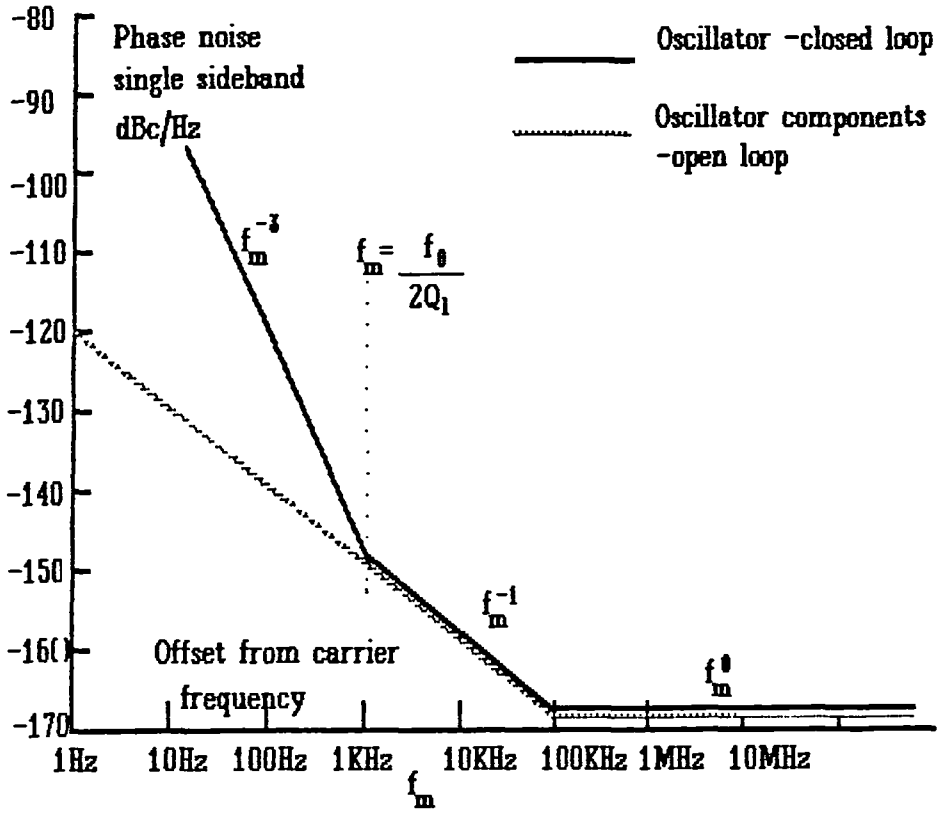


Fig 3.11 Logarithmic phase noise sideband characteristic - high Q case

In general, low Q resonators result in high close to carrier phase noise, but allow a wide tuning range. Conversely high Q resonators result in low close-to-carrier noise and a more stable oscillator, but have a very restricted tuning range.

This fundamental oscillator theory results in over optimistic results for oscillator phase noise. There are additional mechanisms for phase noise generation in oscillators:-

a) AM to PM conversion;

b) Large signal effects in the limiter;

c) Resonator noise;

d) Dynamic phase noise due to vibration;

e) Phase "hits" or discontinuities in phase [Ondria & Singleton, 1988].

The effects of the above are very significant in data communications because they are predominant in the close-to-carrier region. Until requirements arose for low cost low data rate VSAT communications, the far-from-carrier phase noise was considered more important. The close-to-carrier region has not been as thoroughly investigated therefore as the far-from-carrier region.

3.3.5 Crystal oscillator noise

3.3.5.1 Introduction

In frequency synthesis, some kind of reference oscillator is required, and the noise spectrum of this will dominate the output at close-to-carrier modulation frequencies. This reference is normally provided by a crystal oscillator. The phase noise of the crystal oscillator can originate in the maintaining amplifier or in the resonator.

3.3.5.2 The Maintaining Amplifier

The effect of phase noise in the maintaining amplifier has already been studied [Everard, 1986]. This is under the control of the circuit designer, who must ensure that the phase noise contribution of this is at least 10dB below that of the crystal resonator [Driscoll, 1985].

3.3.5.3 The Crystal Resonator

Flicker phase noise contributions of resonators has been studied by many authors eg. [Driscoll, 1985a], [Jungerman, 1985], [Driscoll, 1985b]. There are two types of resonator noise effects possible [Parker, 1985]:-

Type (i) Variations in the phase relationship between the resonator terminal and the acoustical vibrations inside the resonator;

Type (ii) Disturbances to the acoustical vibrations themselves by physical effects within and around the resonator.

In the resonator curve displayed in fig 3.12, effect (i) results in vertical displacement of the resonator phase curve. On the other hand, effect (ii) results in a random horizontal shift in the curve. Effect (ii) is equivalent to random shifts in the resonator frequency.

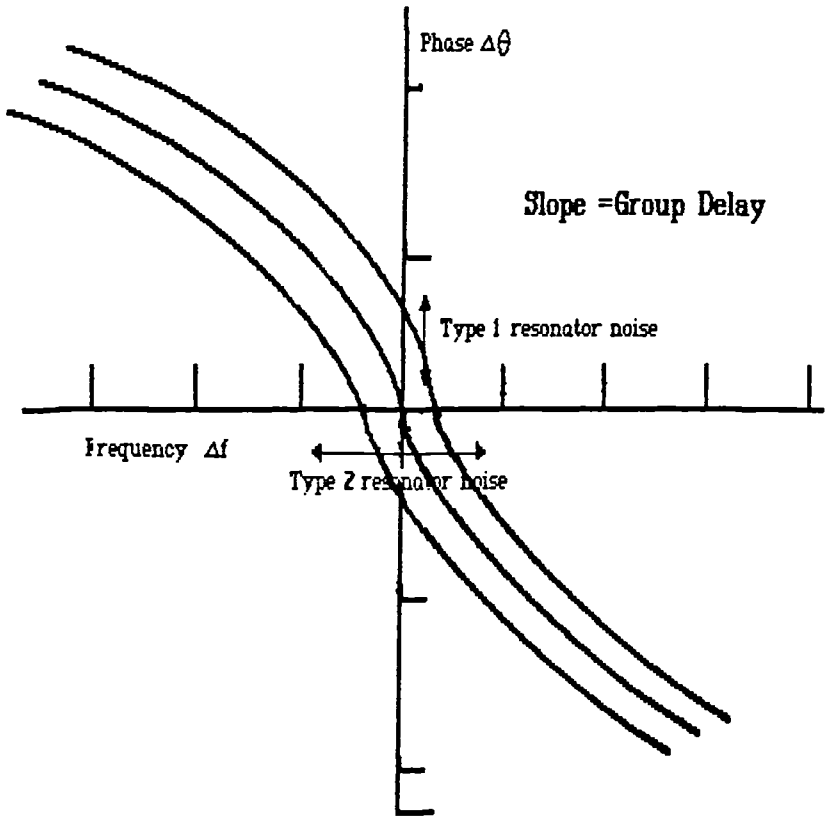


Fig 3.12 Resonator phase frequency curve with noise effects

3.3.5.4 Measurements and Results

Fig 3.13 displays a block diagram showing the two port method of resonator phase noise measurement. The loaded Q of the resonator (slope of the resonator curve) can be varied by altering the matching network. The amplifiers are proprietary silicon MMIC modules which possess low $1/f$ noise. Loaded Q's of the two resonators should be identical to avoid decorrelation of source noise. The resulting noise is the sum of the noise contributions of each resonator, and the resulting spectrum depends whether a type (i) or (ii) noise generation process is involved.

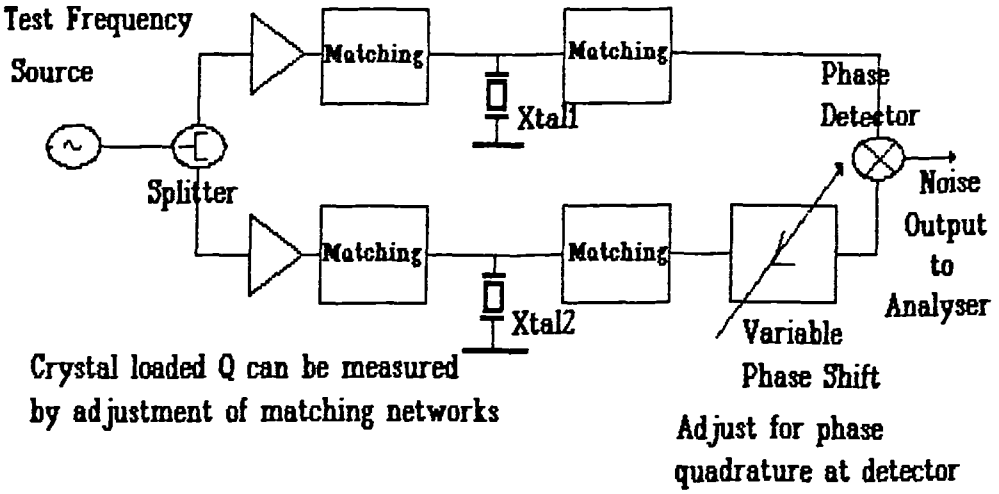


Fig 3.13 Crystal resonator phase noise measurement

The spectrum of noise generation is displayed in fig3.14 for a type (i) effect. Phase noise is independent of loaded Q in the region for $f_m < f_o/2Q_L$. For $f_m > f_o/2Q_L$ the noise is modified by the 6dB/octave roll-off imposed by the resonator. This response is also apparent from the resonator phase frequency curve. Since the noise displaces the curve vertically, the resultant phase noise is independent of the slope of the curve. The $f_o/2Q_L$ factor is the half bandwidth of the resonator.

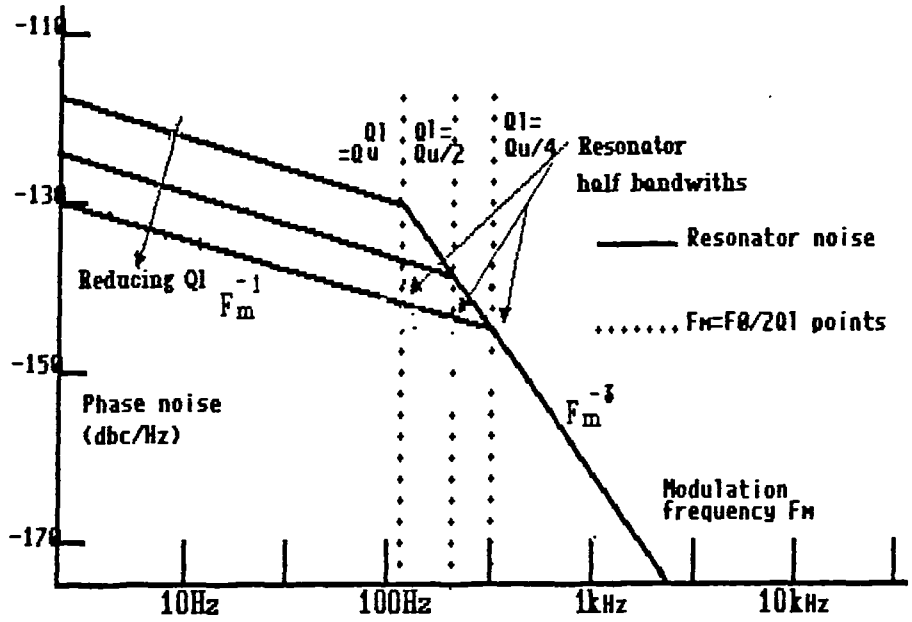


Fig 3.14 Type one resonator noise spectrum

Fig 3.15 illustrates the spectrum obtained for the type (ii) mechanism; as can be seen, the effect is the reverse of the type (i) effect.

For $f_m < f_o/2Q_L$, movement of the resonator characteristic due to noise of δf results in phase disturbances:-

$$\delta\theta = \frac{2Q_L\delta f}{f_o} \tag{3.11}$$

Therefore halving Q_L halves the phase deviation, $\delta\theta$, resulting in a 6dB reduction in phase noise. For $f_m < f_o/2Q_L$, the resonator response displays a single pole (6 dB/octave) roll off. Therefore the phase noise rolls off at 9dB/octave above the resonator half bandwidth. Since lowering the Q_L by half lowers the in-bandwidth phase noise by 6dB, and raises the half bandwidth by twice, the net effect is that the phase noise above the half bandwidth is independent of Q_L.

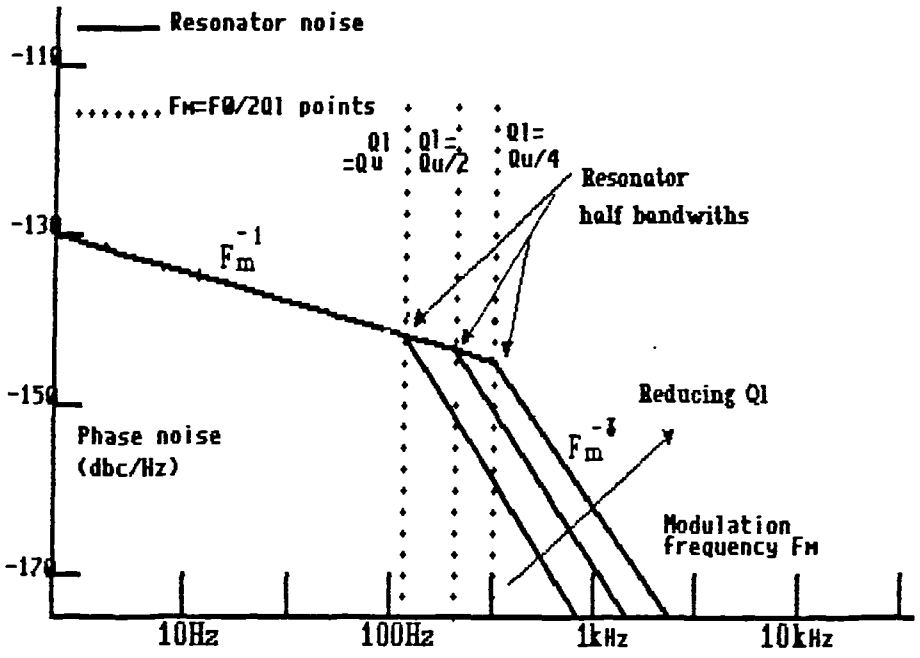


Fig 3.15 Type two resonator noise spectrum

The type (i) phase noise is most likely to be a function of the coupling to the resonator of the terminals, and type (ii) is a function of the physical properties of the resonator itself.

In quartz crystals, the bulk of the resonator structure comprises the quartz, and so the type (ii) effect is likely to be dominant. Experimental evidence [Parker, 1985] appears to verify this.

3.3.5.5 Closing the loop

Closing the loop around the amplifier resonator combination to make an oscillator results in a reversal of the open loop effects. As discussed in §2.6, the closed loop phase noise increases at 6dB/octave above the open loop as f_m decreases below $f_o/2Q_L$. Therefore instead of the break in the slope from 9dB/octave to 3dB/octave occurring at the half bandwidth point as in the open loop case, the noise continues to rise at 9dB/octave. This gives rise to the important effect whereby for type (ii) noise the $1/f^3$ noise is independent of the loaded Q of the resonator (as shown by fig3.15).

If type (i) noise dominates, then the $1/f^3$ noise is dependent upon Q_L. Fig3.16 shows how the effect of closing of the loop of a 100MHz crystal oscillator can be observed for different loaded Q's.

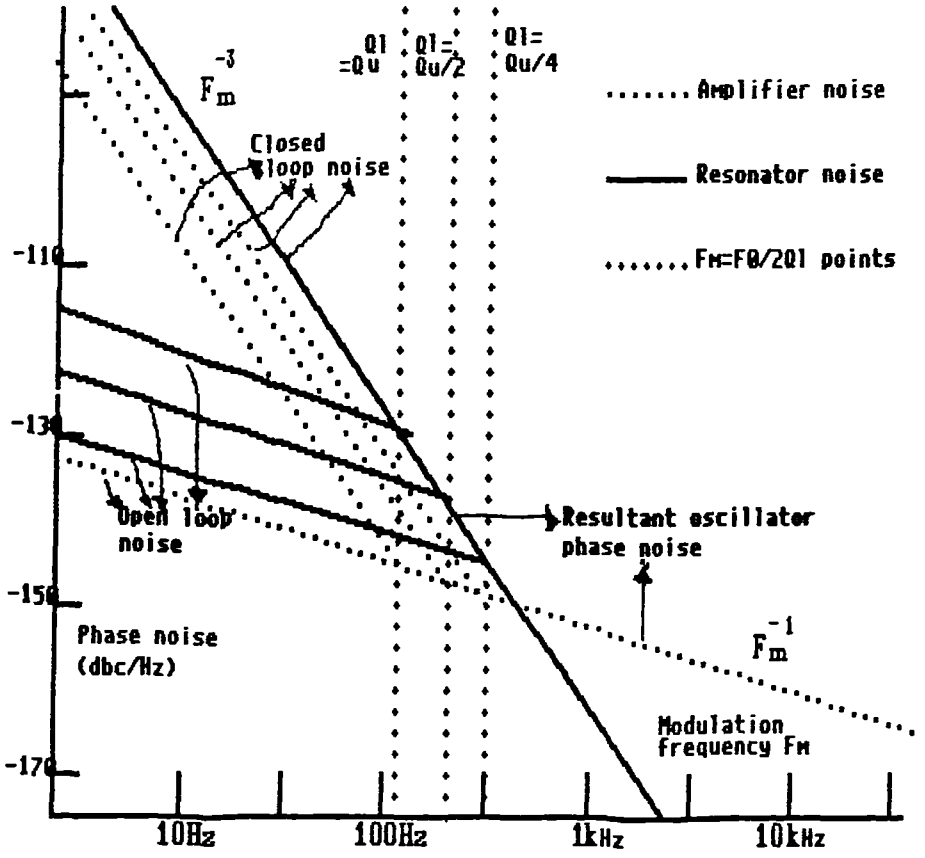


Fig 3.16 Phase noise generation within a 100MHz crystal oscillator

3.3.5.6 Other Phase noise effects in crystals

Burst Noise

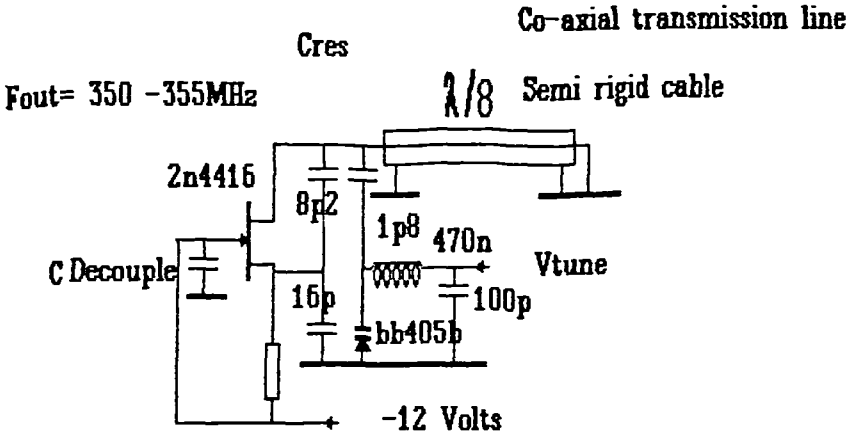
Burst noise consists of discrete disturbances in phase [Moulton, 1986]. Burst noise is more easily revealed in the time domain than in the frequency domain, as the sharp transient energy is likely to be spread in frequency, and may be obscured by flicker noise. This form of noise may be more troublesome than flicker noise in a data system as the sharp transients may be indistinguishable from data. The significance of this is therefore that a crystal oscillator could appear better on a spectrum analyser, yet give inferior performance in a system.

Crossing Modes

Crossing modes are spurious modes that occur alongside crystal oscillator main modes in such a manner as to create a point of inflection in the phase frequency characteristic of the resonator [Muat, 1986c]. This results in a very low effective loaded Q, and consequently, a noisy oscillator.

3.3.6 Other flicker noise sources

The varactor is also possibly a source of flicker noise. Rohde [1983] displays curves showing a slope of 20dB/octave as a result of varactor diode degradations. Slopes of approximately 30dB/octave have however been observed by the author as indicated below. This has been confirmed by Martin [1981] who measured a 135MHz JFET oscillator. The circuit displayed in fig3.17 was used to provide the results shown in fig3.18.



All resonant circuit capacitors are ATC 175 series High Q Chip caps.

Fig 3.17 Circuit diagram of VCO used for phase noise tests

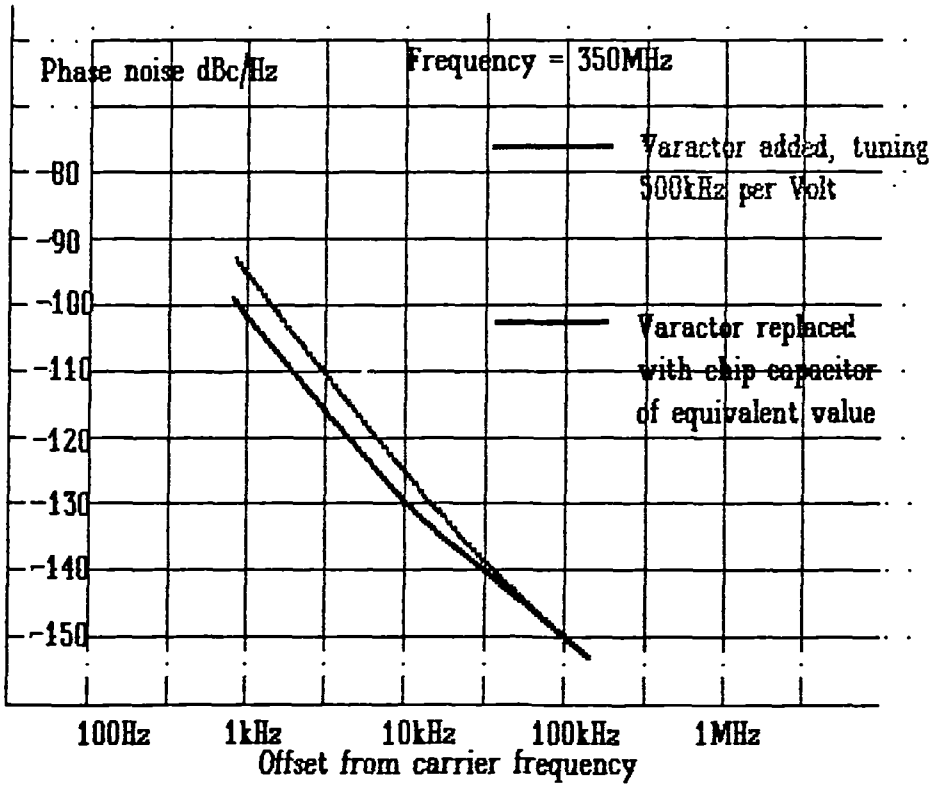


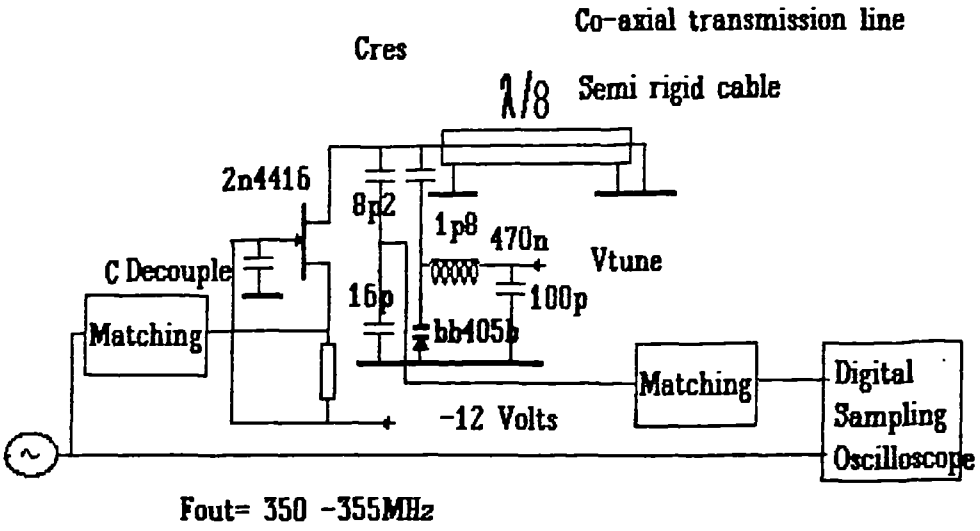
Fig 3.18 Measured results for a 350MHz JFET VCO

The loaded Q was also obtained by means of a digital sampling oscilloscope with the test setup of fig 3.19. The circuit was connected in open loop format, and driven at a level equivalent to that when oscillating in closed loop configuration. A time domain reflectometry measurement is taken at the input to determine the input impedance at the FET source at the level which will exist in the oscillator. A transforming network is placed at the output to load the resonant network with an impedance equal to that of the FET source, and a plot of phase shift against frequency is then taken. The resulting loaded Q's are found to be:-

Q_L with varactor = 240

Q_L no varactor = 286

If the phase noise increase was due to the change in loaded Q, then a noise degradation of 1.5 dB would be expected. The degradation measured is far more than this, and also is not constant with offset from carrier frequency. This leads to the conclusion that other mechanisms must be responsible for the extra noise besides Q degradation.



The oscillator loaded Q can be measured from the large signal group delay

Fig 3.19 Open loop loaded Q measurements on an oscillator

3.4 Conclusions

This section has shown that the phase noise of a practical oscillator circuit can be far in excess of the theoretical calculations based on additive noise. In particular, close to carrier phase noise is more likely to be affected.

Flicker phase noise brings additional degradation, and has been shown to occur both in the resonator and in the oscillator loop. If the flicker noise originates in the oscillator loop, increasing resonator loaded Q will reduce the phase noise, but this is in general ineffective against resonator noise. There is much scope for further work in relation to the sources of flicker noise. In particular it is not known which sources are fundamental and which are determined by the manufacturing process. This leads to some confusion as to whether flicker noise is device dependent or not.

It has been shown that with high Q resonators the resonator noise dominates over circuit noise in the close to carrier region. Responsibility for low close to carrier phase noise reference sources ultimately rests with the supplier of the crystals rather than with the circuit designer. With bulk acoustic materials such as crystals, varying resonator loaded Q

has little effect on the phase noise. Some crystals also display other disturbing effects such as burst noise and crossing modes.

A further problem with flicker noise has been shown to exist as a result of introducing varactors to enable electronic tuning of oscillators. The author has shown that adding the varactor increases the level of noise over and above that predicted from a reduction of the loaded Q. This means that other mechanisms are responsible for the noise increase apart from Q degradation.

Flicker noise also arises in other circuits such as multipliers, amplifiers, and dividers, all commonly used in synthesiser circuits.

3.5 Further work

There are further investigations required into flicker noise effects in synthesiser circuits, particularly with respect to frequency multipliers and dividers. A comparative evaluation of different oscillator circuits and varactor types for flicker noise performance is also required, but is beyond the scope of this thesis.

A contradiction exists between previous work on the subject of RF flicker noise for different classes of device [Jungerman, 1985], [Pucel, 1986]. This needs investigation to determine whether this is truly device independent. If there is a dependency then an investigation is required to determine whether it is dependent upon semiconductor type (silicon or gallium arsenide) or structure (MOSFET, or JFET).

3.6 References

Boyles, J.W, June 1986 The oscillator as a reflection amplifier - an intuitive approach to oscillator design. *Microwave Journal.*

Buckingham, M.J. 1983a *Noise in electronic devices and systems.* chap5 p. 135. Wiley

Buckingham, M.J. 1983b *Ibid.* chap6 p. 145

Driscoll, M.M. 1985a Spectral degradation in VHF crystal controlled oscillators due to short-term instability in quartz resonators. *40th Annual Frequency symposium.*IEEE

Driscoll, M.M. 1985b Low Noise Crystal Oscillators using 50Ω modular amplifier sustaining stages. *40th Annual Frequency Symposium*, IEEE

Everard, J.K.A. August 1986 Low Noise Power Efficient Oscillators: Theory and Design. *IEE proceedings*. vol.133. Part G, No.4, pp 172-180.

Halford, D, Wainwright, A.E, % Barnes, J.A, 1968 1/f noise in RF amplifiers and frequency multipliers, characterisation causes and cures. *22nd Annual Frequency Control Symposium, Fort Monmouth, NY.*IEEE

Jungerman, R.L. *et. al.* 1985 Delay Dependence Of Phase noise in SAW filters. *40th Annual Frequency Symposium.NY.*IEEE

Kroupa, V.F. 1973 *Frequency synthesis theory design and applications.* p. 54 Griffin.

Martin, M. 1981 Low noise VHF-Oscillator with diode tuning, digital frequency control,and frequency indicator. *VHF Communications.* UKW-Berichte, BAIERSDORF, Germany Vol 2.

Motchenbacker, C.D. & Fitchen, F.C. 1973a Low noise electronic design, chap 8 p143.

Moulton, G. 1985 Analysis and prediction of phase noise in resonators and oscillators and resonators. *Hewlett Packard RF and Microwave Symposium,* NY

Moulton, G. April 1986 Dig for the roots of oscillator noise. *Microwaves and RF* pp. 65-69.

Muat, R. & Upham, A. 1986a Low noise oscillator design *Hewlett Packard RF and Microwave Measurement Symposium and Exhibition,* London p. 24

Muat, R. & Upham, A. 1986b *Ibid.* p. 17.

Muat, R. & Upham, A. 1986c *Ibid.* p. 28

Muat, R., 1984 Designing Oscillators for Spectral Purity. *Microwave and R.F News.* Three parts: Vol 23, No 7 p 133-142,160, July 1984; Vol.23, No 8, Aug. 1984, pp166-170; Vol.23 No 9, Sep. 1984 pp211-217.

Ondria, J. & Singleton, J. A 9th May 1988 Highly Temperature Stabilised K Band (18 - 26.5 GHz) Gunn VCO for High Capacity Radio Systems. *IEE Colloquium on Microwave Components in Telecommunications, London.*

Parker, T.E. 1985 1/f Frequency Fluctuations in acoustic and other stable oscillators. *39th Annual Frequency Symposium.* p. 97. IEEE

Pucel,A. 1986 The GaAs FET oscillator - its signal and noise performance, *40th Annual Frequency Symposium* p385-391.

Rohde, U. 1983 Digital PLL Frequency Synthesisers, Theory and Design. chap 2, p. 82.

Scherer, D. April 1979. Today's lesson - Learn about low noise electronic design part 1. *Microwaves.*

4 A Survey of Synthesiser Techniques

4.1 Introduction

Synthesisers are critical elements in a satellite communication system, and can serve as oscillators in the transmitter, the satellite transponder, and the receiver chain. As such, they contribute to phase noise at all stages.

The term synthesiser implies an oscillator whose output frequency can be controlled, preferably with programmable logic. Modern communication systems call for readily selectable frequencies in order to allow channel selection, and this is taken to extremes in the case of frequency hopping spread spectrum systems.

Among the characteristics of concern to the system designer are: settling time; resolution; temperature stability, and cost. Phase noise is however also a critical parameter and this section examines some of the implications in terms of various design options.

There are two principal classes of synthesiser: incoherent and coherent. Incoherent synthesis is the manipulation of a bank of reference frequencies to produce a desired output frequency. This has been largely superseded due to demands on frequency stability and accuracy which would be costly to implement if a multitude of sources were used. Coherent synthesis is the derivation of the output frequency from one master reference source.

In coherent synthesis there are three principal operations that can be applied to a reference frequency to synthesise the output frequency. These are:-

1) Multiplication

2) Fractionalisation

3) Combination.

In the first method, also called the harmonic method, the output is an integer multiple of a reference frequency. This has the advantage of simplicity and the fixed reference frequency being easily filtered out. The disadvantage is that the output frequency selection is too coarse for many applications.

The second method has phase noise advantages since the reference frequency is greater than the output frequency. The disadvantage is that the output frequency is generally low. The third method combines methods 1 and 2 in such a manner to provide the greatest flexibility in output.

There are four principal hardware implementations of synthesis:

		Operation
a)	Direct analogue	*1 & 3*
b)	Direct digital	*2*
c)	Phase locked loop	*1*
d)	Hybrid techniques	*3*

As to selecting the method of synthesis applicable for a particular application, there needs to be an assessment of criteria which can be applied to aid the selection of an optimal local oscillator arrangement. This chapter will assess different synthesiser architectures with a view to possible selection for a satellite communication system. Chapters 6 and 9 define the requirements for a synthesiser for such systems; the essential requirements may succinctly be expressed as:-

i) Low cost

ii) Simple compact units

iii) Low close to carrier phase noise

iv) Low spurious signals at the output

v) Good immunity to vibration

In addition, chapter 9 suggests that the following could simplify the design of integrated satellite data terminals:-

vi) Rapid low transient selection of channels

vii) Very close channel spacing of less than 1 Hz

viii) Modulation capability.

Many synthesiser manufacturers often have a vested interest in some form of synthesis scheme based on historical familiarity with a certain technology, eg. a filter company that produces direct analogue synthesisers, or a phase lock loop IC manufacturer. One of the aims of this chapter therefore is the study of synthesiser architecture without any bias towards a particular scheme.

4.2 Phase locked synthesis

4.2.1 Introduction to PLL synthesis

In recent times, phase locked loops (PLLs) have dominated many aspects of frequency synthesis. This is due mainly to the availability of complete phase locked loops on integrated circuits. Phase locked loop synthesisers are extremely well documented [Rohde, 1983a], [Manassewitsch, 1985a], [Egan, 1981a]. The basic loop is known as the N divisional loop and is displayed in fig4.1.

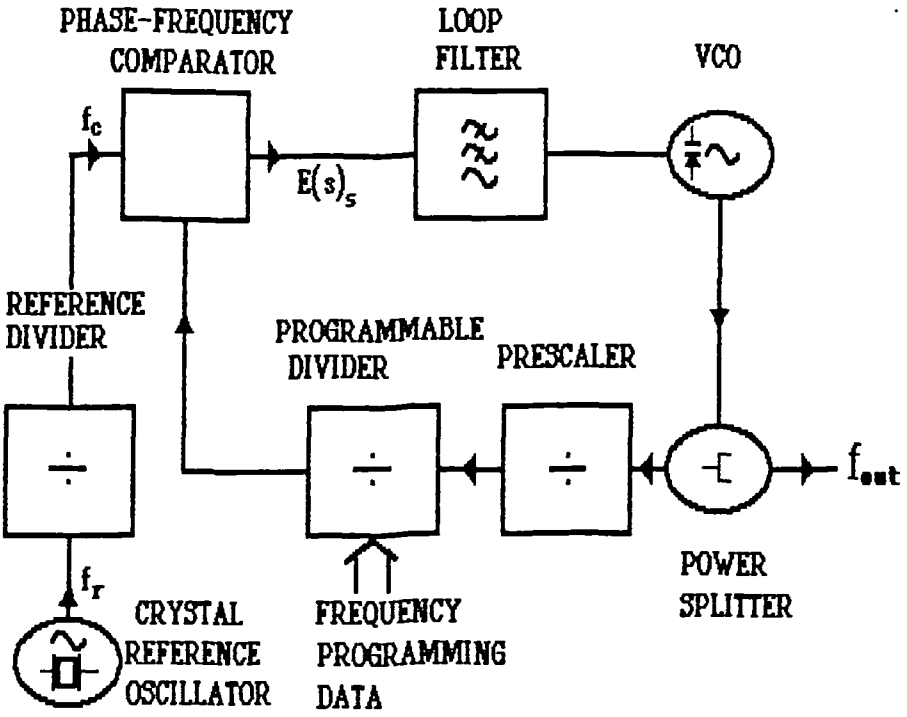


Fig 4.1 ÷N Phase locked loop synthesiser

The concept is that the output frequency is locked by feedback to the reference frequency and therefore becomes an integer multiple thereof. Ideally the phase detector should be a digital type as indicated in fig4.2, as analogue phase detector types can introduce false locking problems.

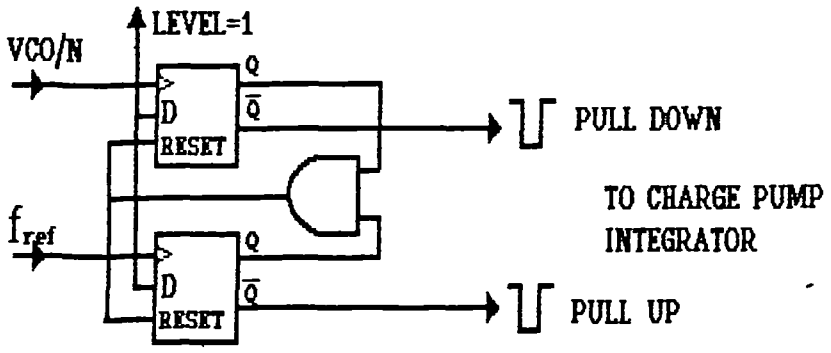


Fig 4.2 Edge triggered digital phase detector

The advantages of PLL synthesisers are:-

i) Simple implementation as single IC synthesisers are readily available;

ii) Low costs;

iii) Simple alignment procedure;

iv) Compact;

v) Economical power consumption.

The disadvantages are:-

i) Phase noise is relatively high;

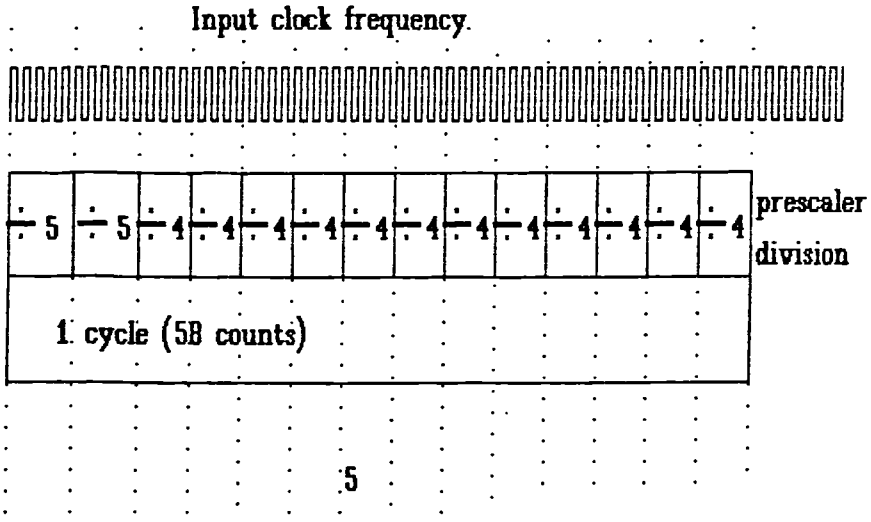
ii) Susceptible to microphony due to restricted loop bandwidth;

iii) Susceptible to induced hum due to sensitivity of post phase detector circuitry;

iv) Non-linear phase detectors introduce special design problems;

v) Restricted choice of reference frequencies.

The TVRO market has ensured the proliferation of cheap single IC synthesisers, but these pose special problems for data communications [Wilson, 1988]. The maximum frequency of operation of synchronous dividers is ≈ 100MHz, necessitating the use of some form of prescaler. A fixed modulus prescaler increases the output frequency, but the step size is increased to pf_{ref} where p is the prescaler division ratio. This problem is usually overcome by the use of a variable modulus prescaler (VMP) [Rohde, U, 1983b] as in fig 4.3.



Units counter counts from the preset value to zero, and prescaler set to N+1, prescaler remains at N for the remainder of the reference cycle

Fig 4.3 Operation of dual modulus prescaler

The division ratio of the VMP varies over one reference cycle as shown. If the prescaler is set to divide by $p + 1$ for l output cycles and p for n-l cycles, the divider total division is set by $n_t = (p + 1)\, l + p\, (n - l)$, giving:-

$$n_t = p\, n + 1 \qquad (4.1)$$

The problem with this scheme is that:-

i) The minimum division ratio is $n^2 - n$;

ii) VMPs are not available with input frequencies above 1 GHz [Rohde, 1983b].

The VMPs are usually designed to minimise power consumption rather than phase noise. It is possible to cascade VMPs to reduce the $n^2 - n$ value as in fig 4.4. The function of a cascaded prescaler is shown in fig 4.5.

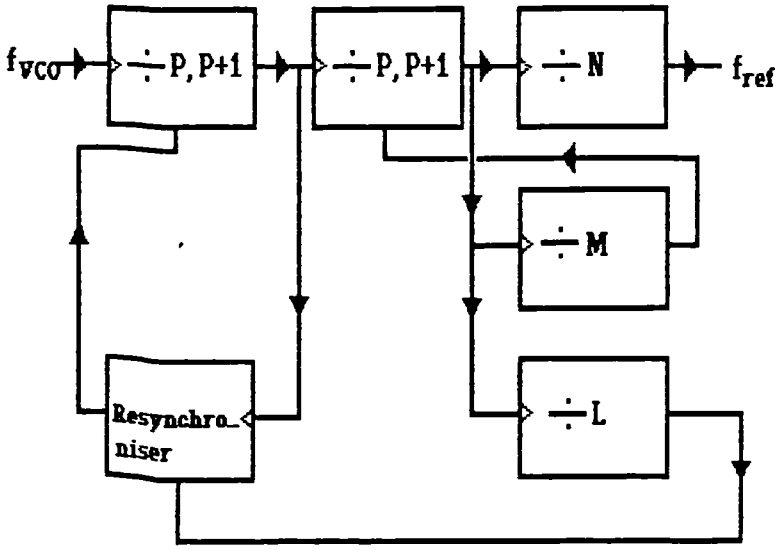


Fig 4.4 Multistage dual modulus counters

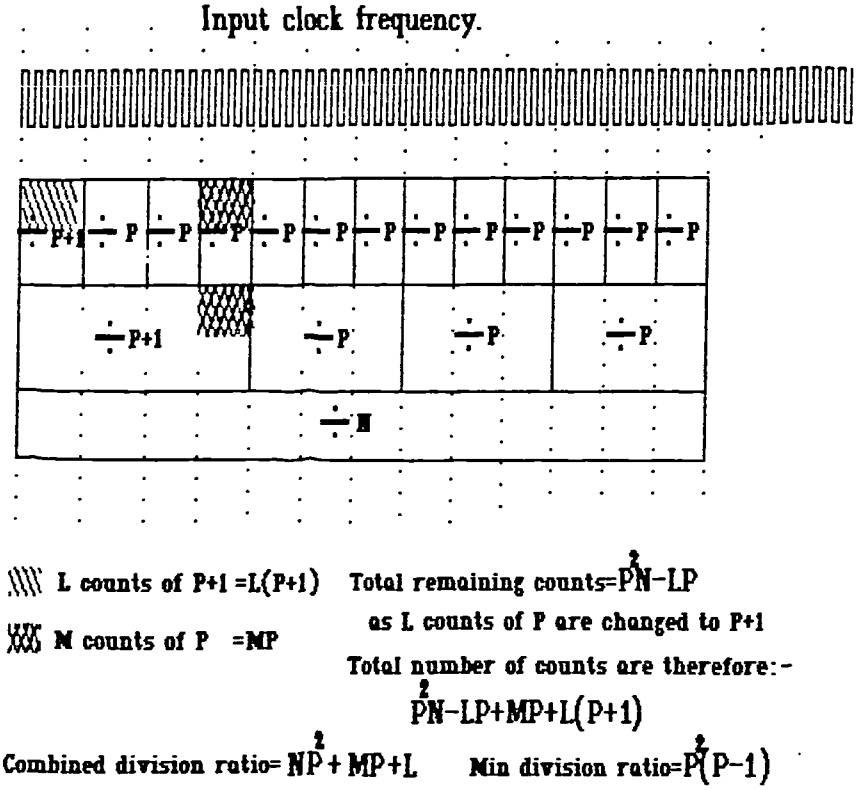


Fig 4.5 Operation of cascaded dual modulus prescalers

To implement this scheme above 1 GHz then a fixed modulus prescaler would be required, extending operation to ≈ 4.5 GHz using inexpensive commercially available dividers [Avantek, 1990]. In this case, the frequency stepping will be equal to the reference frequency times the single modulus divider ratio. The maximum reference frequency is set by the minimum division ratio, that is $(n^2 - n)$, and by the propagation delays of the devices employed. This is about 2 MHz for economical configurations. The use of frequencies much less than this will result in excess static phase noise, dynamic phase noise, and oscillator phase "hits" [Znojkiewicz & Vassilakis, 1987]. The latter two are particularly troublesome for digital communications. A consequence is that the N divisional loop is inflexible in the choice of operating frequencies. A modification to the N divisional loop that overcomes many of the problems and enables a step size of f_{ref} at frequencies up to 4.5 GHz is discussed later and in the author's paper [Wilson, 1988].

4.2.2 Increasing Resolution

Many techniques have been introduced to increase the resolution of the basic N phase locked loop. They fall into two categories:-

1) Multiple loops;

2) Fractional N.

The multiple loop approach basically involves utilising cascaded N loops that are progressively scaled and mixed together [Stirling, 1987a], [Rohde, 1983c], [Egan, 1981b], [Brewerton, & Urbaneta, 1984], substituting phase locked loops for RF filters. The fractional N schemes all use a non constant division ratio to change the average output frequency together with some techniques for cancellation of spurious products.

4.2.3 Multiple Loops

The multiple loop is strictly classified as a hybrid between the direct and the phase locked loop configurations. The output from one loop is fractionalised by division and summed in by means of a mixer, as with the direct analogue synthesis. If the synthesiser is to be used as part of a down-conversion or upconversion scheme, a multiple loop configuration synthesiser can either be built within one synthesiser, or be distributed throughout the down-conversion stages as a succession of single loop stages as in fig4.6.

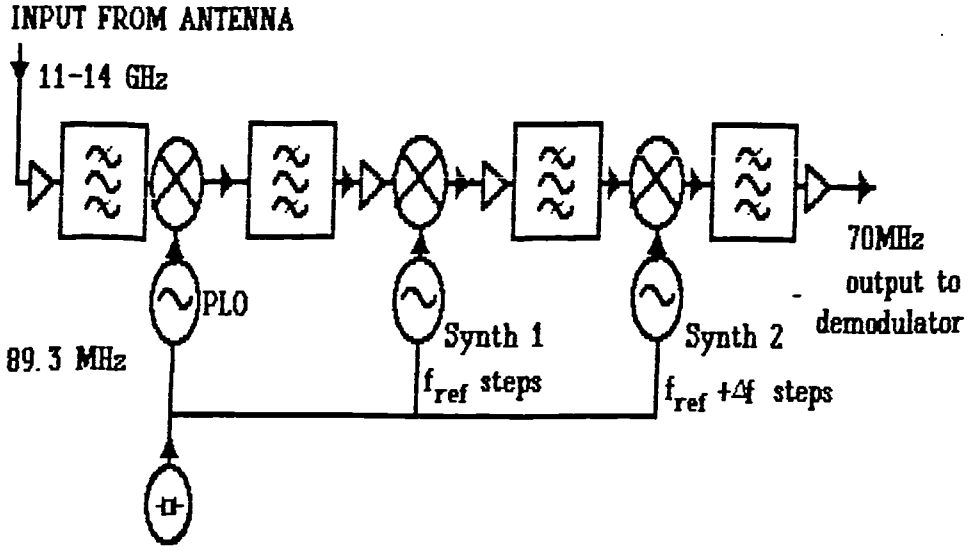


Fig 4.6 Increasing resolution by means of a succession of single loop synthesiser stages

The advantages of the multiple loop synthesiser over distributed synthesis are:-

a) The synthesiser becomes a self contained block that can be exchanged for different band coverage and eases testing and servicing.

b) Although there is more demand on the synthesiser filtering, the synthesiser filters have only to handle carrier wave (cw) RF rather than signals. It is desirable that the signals through the receiver/transmitter IF chain can be at a fixed frequency. This can ease filter requirements, since in many cases there are stringent demands upon group delay and amplitude variations over the

pass band frequencies of these filters. If these filters were designed for fixed frequency IF, then the performance could be achieved at lower cost.

4.2.4 Three loop synthesiser

A block diagram of the three loop synthesiser is displayed in fig4.7. If the reference frequency generator is made to be a bank of crystals, then excellent phase noise performance can be achieved since the offset frequency is added in with no frequency multiplication to degrade performance.

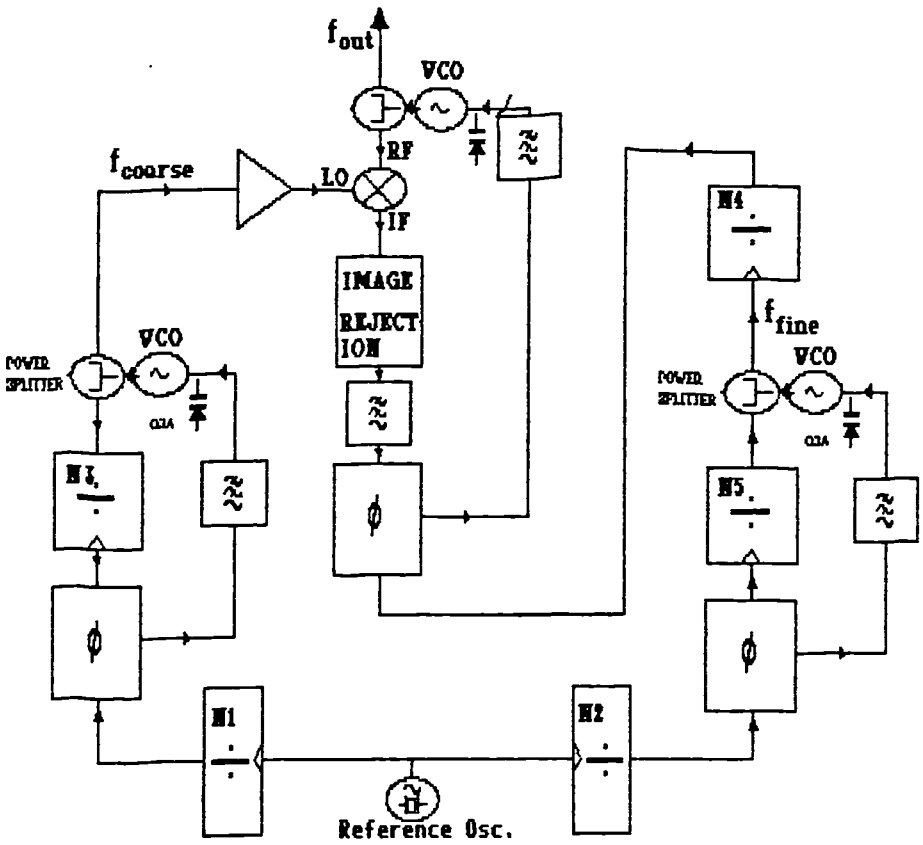


Fig 4.7 3 loop summing or vernier synthesiser

The problems with three loop synthesiser technique are:-

1) Careful screening is required in order to isolate the separate RF sections;

2) The frequency resolution is limited by the division ratio of scaling divider S which would imply high frequencies for VCO_1 in the fine loop;

3) There is a problem of breakthrough of the IF frequency into the output, particularly when synthesising at microwave frequencies. This is compounded by the wide frequency range of the synthesiser IF and the sensitivity of some IF channels.

In order to overcome the basic problem of frequency resolution, more synthesisers can be cascaded as with direct frequency synthesis. One of the cascaded sections can be observed in fig4.8. The synthesis stages can be repeated as necessary to provide the required resolution [Egan, 1981b]. The use of a phase locked loop enables the saving of one reference frequency and one mixer per stage as compared with the direct synthesiser of fig4.14. This is as a result of the band pass to low pass transformation within the phase locked loop.

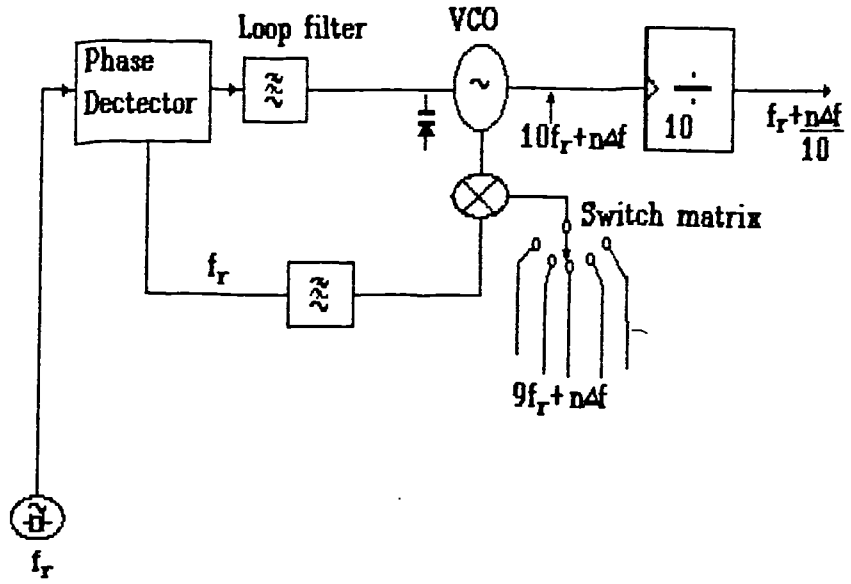


Fig 4.8 Phase locked loop equivalent of double mix divide synthesis

Although the repetition of the basic synthesiser units reduces the parts cost, extensive screening is required between the synthesiser loops [Brown, 1989]. This demands a large number of screened enclosures for each synthesiser. The phase noise of an iterative multiple loop synthesiser is amongst the lowest recorded for any synthesiser, achieving better than -130 dBc/Hz at a few kHz from a 10GHz Carrier [Brewerton & Urbaneta, 1984]. The advantages of the multiple loop approach are therefore:-

i) Low phase noise;

ii) Capable of low spurious output;

iii) Repeated stages reduce cost of components and testing;

iv) Fast switching times of less than 1 μs [Brown, 1989].

The disadvantages include:-

1) Complex RF circuitry, especially around RF switches;

2) Thorough screening of each section required;

3) Limited scope for size reduction by LSI circuitry;

4) Relatively high labour costs involved in manufacture, therefore will not achieve price reduction in volume;

5) Not so readily modified if finer resolution is required.

4.2.5 Fractional N PLL Synthesiser

There are three basic fractional N techniques:-

1) Digiphase

2) Modified Digiphase, or "Kingphase"

3) Fractional N phase interpolation.

Historically the first fractional N technique was the Digiphase [Gillete, 1969]. A block schematic of this technique is displayed in fig4.9. There are two parts to this concept: the phase accumulator; and the phase error correction employing a DAC [Hassun, 1984].

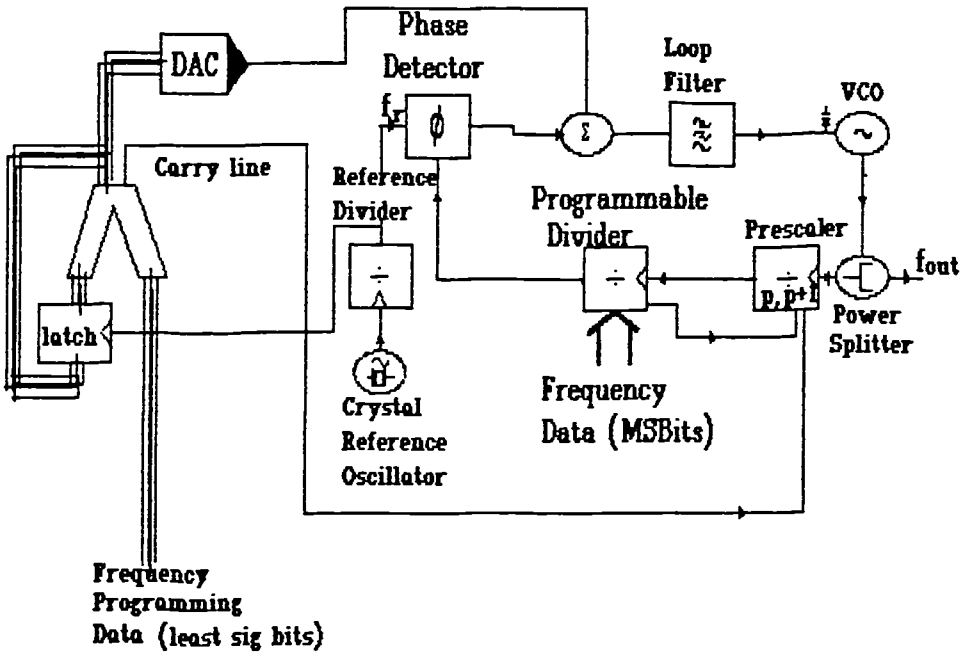


Fig 4.9 Digiphase synthesiser

If zero is summed into the phase accumulator, then this represents zero phase error and the synthesiser becomes a straight N divide. However, if a phase difference is repeatedly summed into the accumulator, this phase advance represents a frequency less than the reference frequency, a "fractional" frequency. When this phase advance becomes greater than or equal to 2π radians, then the value of N division is switched to N + 1 for the

duration of one reference cycle. Although the synthesiser output frequency would average at a fractional multiple of the reference frequency, non-stationary phase errors would occur at sub-multiples of the reference frequency that would be extremely difficult to remove. The DAC therefore takes the phase increments from the accumulator and converts them to a compensatory voltage to be summed in at the loop filter. This becomes, in effect, a direct digital synthesiser operating within a phase locked loop [Bjerede & Fisher, 1976].

The advantages of this system are:-

i) Arbitrary fine frequency resolution, depending upon size of phase accumulator;

ii) The use of excessively low reference frequencies is avoided;

iii) Readily implemented in LSI;

iv) Reduction in the complexity of RF circuitry;

v) Phase and frequency modulation capability.

Disadvantages include:-

i) Good screening essential between input and output frequencies;

ii) Spurious performance limited by DAC non-linearities;

iii) Temperature dependent spurious performance related to incomplete cancellation of phase error products due to timing errors and amplitude errors;

iv) The maximum reference frequency f_{ref}, ie. the phase comparison frequency, is limited by critical timing paths within the system, preventing the use of low values of N;

v) Poor phase and frequency modulation capability;

vi) Difficult to align.

The DAC timing and non-linearities introduce severe restrictions on the spurious performance. Although a 12 bit DAC could in theory give -78 dBc spurious performance, when timing and non-linearity errors are taken into account the figure is more likely to be -40 dBc [Underhill, 1986]. The contribution of the DAC in terms of phase noise degradation is likely to be significant due to the fact that it acts at the loop filter and will be succeeded by a large multiplication ratio in the loop transfer function. This is as a result of a low phase detection frequency.

4.2.6 Kingphase Synthesiser

In order to overcome the problems of DAC inaccuracies, an innovative method was developed by King (hence "Kingphase") that applies two levels of phase interpolation [King, 1978], [Duck & King, 1983], see fig4.10.

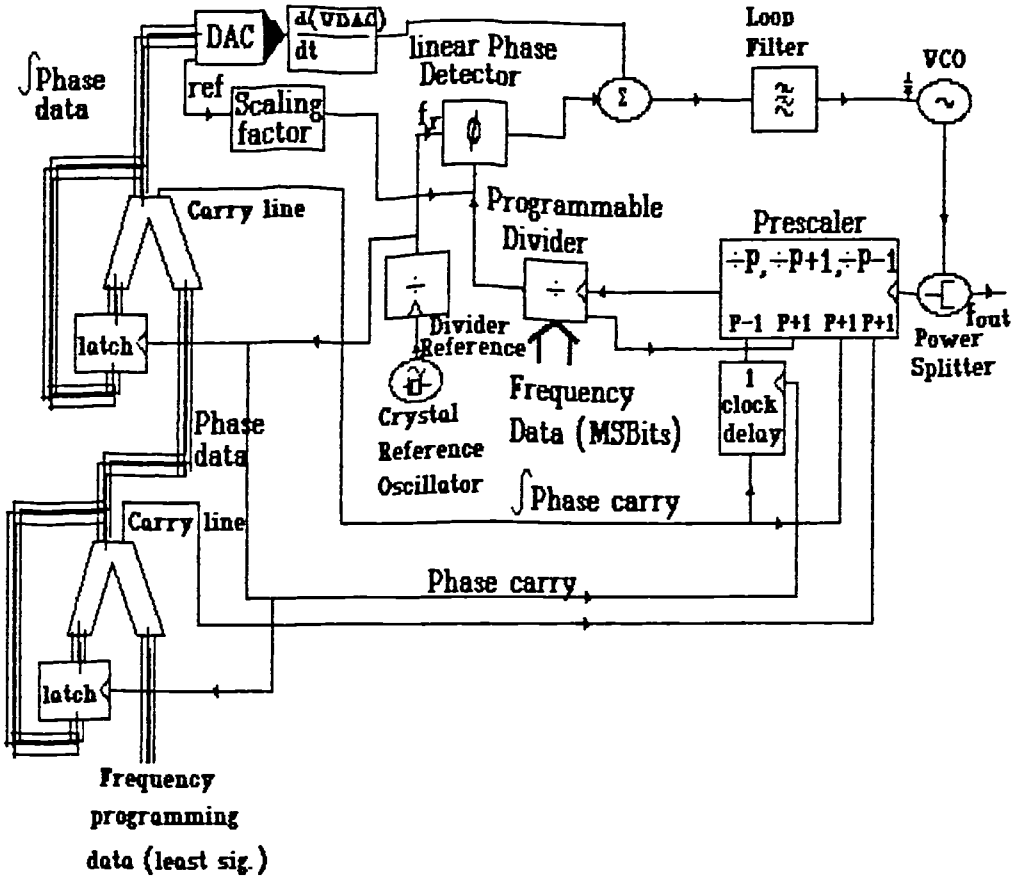


Fig 4.10 Kingphase synthesiser

The Kingphase, or linear phase modulation, synthesiser represents the first attempt to spread the spurious generating error components away from the carrier frequency, enabling them to be effectively filtered by the phase locked loop transfer function. The first accumulator stores phase information as in the Digiphase system and the overflow carry outputs from this accumulator change the N divider to N + 1 as before. However the phase outputs from this accumulator are added into a second accumulator, which stores the integral of phase; this integral of phase performs compensation by two means:-

i) The carry output is differentiated and applied to the dividers. This is accomplished by applying the overflow to increase the division ratio by one. In the next reference cycle the division ratio is decreased by one. The result is

a much closer fit to the desired output phase plane before analogue interpolation.

ii) The integral of phase accumulator value is applied to the DAC for analogue interpolation. Since this correction voltage is to be differentiated before application to the summing point, it is much less sensitive to DAC errors than the digiphase system. However it is just as demanding upon phase detector linearity.

Fig 4.11 displays the Kingphase scheme with a 4 bit phase accumulator and a value of 1 input as the fractional value. The integral of phase accumulator is applied to the DAC for analogue interpolation.

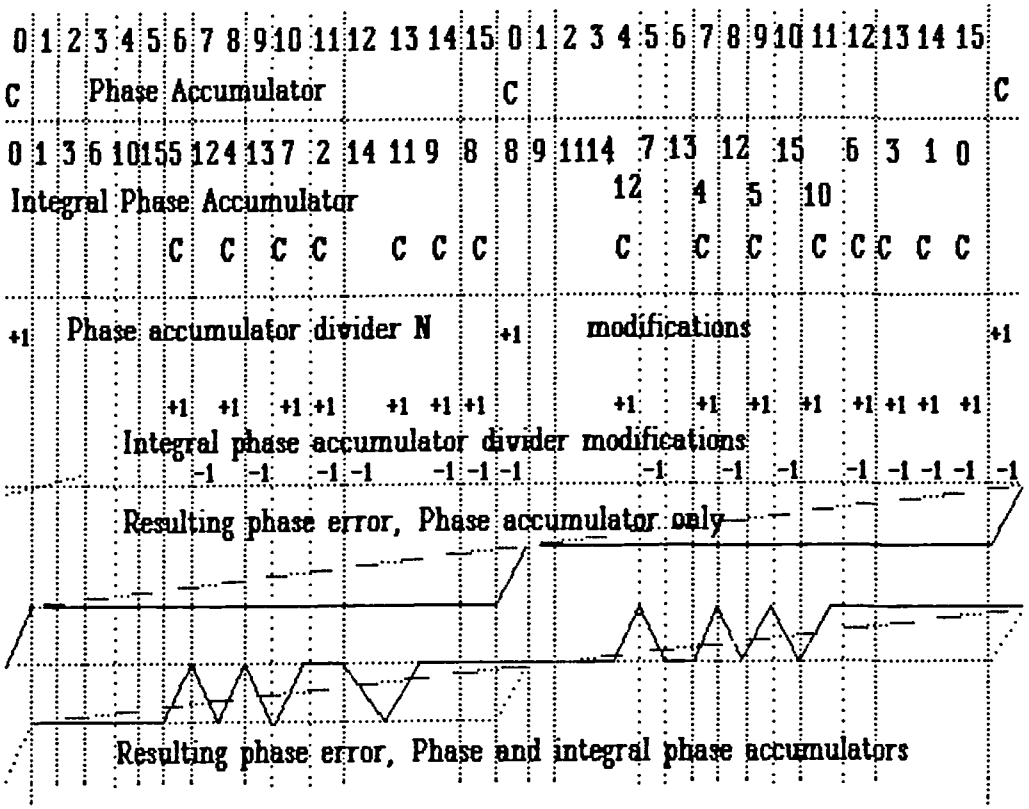


Fig 4.11 Operation of the Kingphase synthesiser with fractional offset

Overflows from the integral of phase accumulator are input to the divider control shift register. On overflow, the N divider is increased by one, this being immediately followed by a decrease of one. The resulting phase error is displayed as the second trace of fig 4.11. Although there are still errors from the ideal phase interpolation, the level of the low frequency components are very much reduced. This is as a result of the differentiation of the divide by N frequency control. Differentiation in the time domain corresponds to a frequency domain response proportional to f^2. The error components due to this process rise at 6dB per octave, and are therefore very low close to carrier.

The fundamental goal of the Kingphase scheme, however, was to enable the DAC to perform integral phase interpolation rather than phase interpolation as with the digiphase scheme. Since this correction voltage is to be differentiated before application to the summing point, it is much less sensitive to DAC errors at low offset from carrier frequencies than the digiphase system. However it is just as demanding upon phase detector linearity. The DAC noise should contribute less to the output phase noise because the output is differentiated.

The advantages of this system are:-

Advantages as listed for the digiphase system above, plus the following:-

i) Spurious levels are much reduced and not as sensitive to temperature variations;

ii) Phase noise is reduced close to carrier due to the differentiating circuit;

iii) Most of the processing components are digital, therefore enabling a high level of integration.

The disadvantages include:-

i) The PLL loop bandwidth is restricted therefore only very low data rate modulation can be used;

ii) Restricted reference frequency upper limit;

iii) Good screening is essential between input and output;

iv) DAC Non-linearity.

There are still serious limitations for data communications with the Kingphase system. The Kingphase system has been used for data communications, but it has been suggested [Britten &Martin, 1989] that vibration may have been a problem.

Two timing paths exist through the synthesiser, the divider path and the phase correction path. These limit the maximum reference frequency that can be used. The level of spurious generation for a given DAC accuracy and cancellation adjustment rises at 6dB per octave towards the reference frequency [Racal, 1983]. A plot of spurious responses against offset from carrier frequency is displayed in fig4.12 for the Kingphase synthesiser (obtained from [*ibid*, 1983]). This means that the loop bandwidth must be a small fraction of of the reference frequency (typically < 0.1%). If a wide bandwidth PLL is required, the phase detection frequency must be so high that a linear phase detector

would be expensive and difficult to implement. Use of a low PLL bandwidth increases susceptibility to dynamic phase noise and "phase hits".

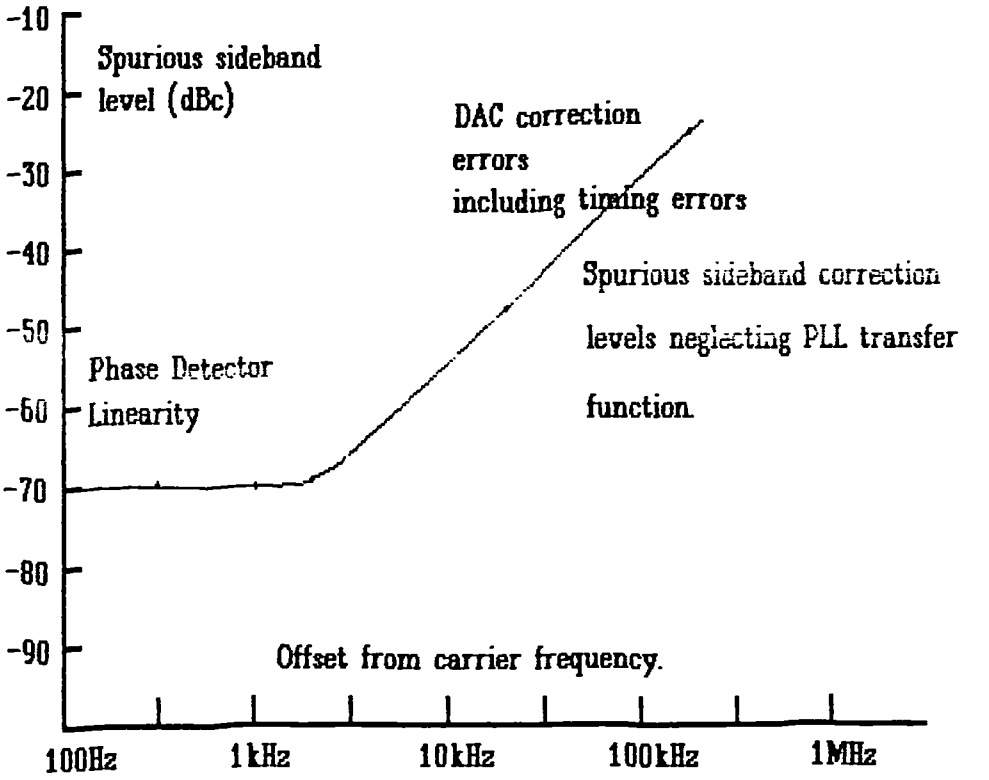


Fig 4.12 Discrete sideband performance of the Kingphase technique with 1 MHz phase comparison frequency and 2% DAC linearity

The requirement of good screening between input and output is true of any fractional synthesis technique, and is not specific to the Kingphase technique.

4.2.7 Fractional N "Analogue Phase Interpolation" Method

This system is similar to the Digiphase systems but it presents another method of overcoming the DAC linearity problem. It is achieved by means of a switched charge pump in the phase detector. The charge pump current is switched on for a length of time proportional to the contents of the phase accumulator [Hewlett-Packard, 1978]. A block diagram of the system is displayed in fig4.13. This results in a correctly summed phase interpolation at the phase detector. Timing is still a problem, but the phase error spectrum is uniform with frequency and so it can tolerate a wider loop bandwidth. A disadvantage with this approach is that fairly complicated analogue circuitry is required for the switching making integration more difficult. In common with other fractional N phase locked loop schemes, unless it can be implemented in VLSI, a very complicated system results.

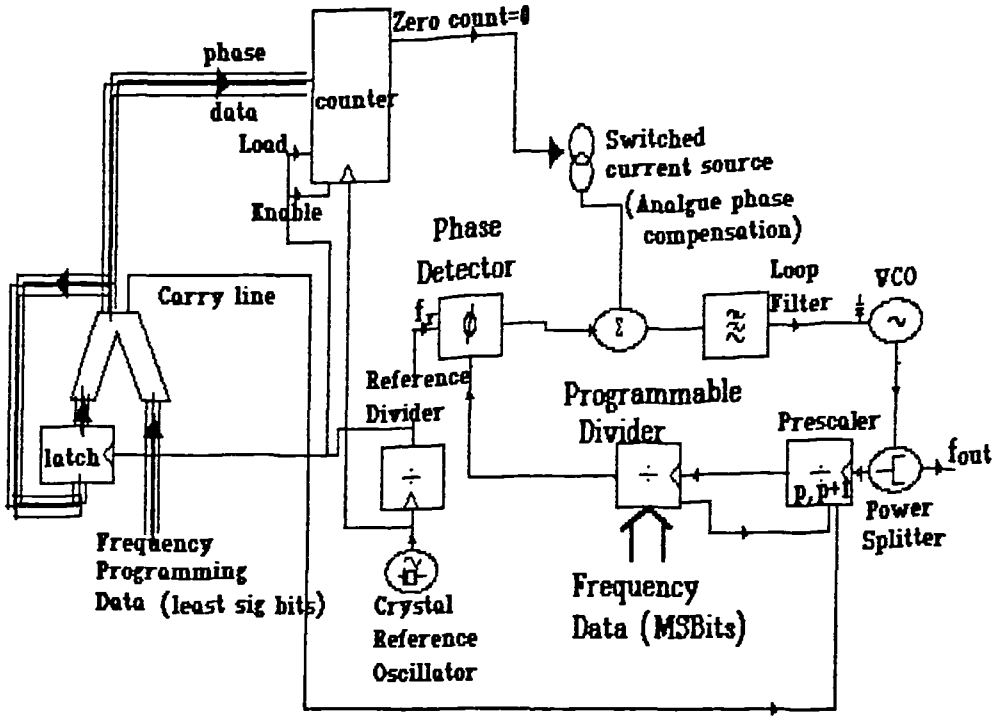


Fig 4.13 Fractional N synthesiser

4.2.8 Harmonic Sampling Loop

Fig 4.14 displays a schematic of the harmonic sampling phase locked loop which is a very simple phase locked loop that involves applying an impulse to a Schottky diode phase detector. This is a multiplicative synthesiser technique only. A detailed description of the sampling loop is given in §5 4.3.1. The detector is gated for the duration of the impulse. Sampling of the RF signal occurs at a rate determined by the reference frequency, and any difference between the RF signal and an integer harmonic of the reference frequency is aliased down to the difference frequency. If the RF frequency is equal to a harmonic of the reference frequency, then a DC signal is output from the phase detector which can be used to lock the loop. When the diode is not gated, the sampled signal is stored at the hold capacitor. An efficient method of generating the impulse is by means of a step recovery diode (SRD) [Josefsberg, 1991] and design criteria for this type of circuit are further covered in chapter 7. If a fast step recovery diode and Schottky detector diodes are used, then operation can be obtained at frequencies of up to 20GHz [Grove, 1966].

The harmonic sampling loop can offer the following advantages over the use of a ÷N loop:-

i) Avoiding long chains of dividers improve phase noise;

ii) Oscillators can be locked at frequencies at which low phase noise dividers are not available, eg Phase-locked dielectric resonator oscillator (DRO).

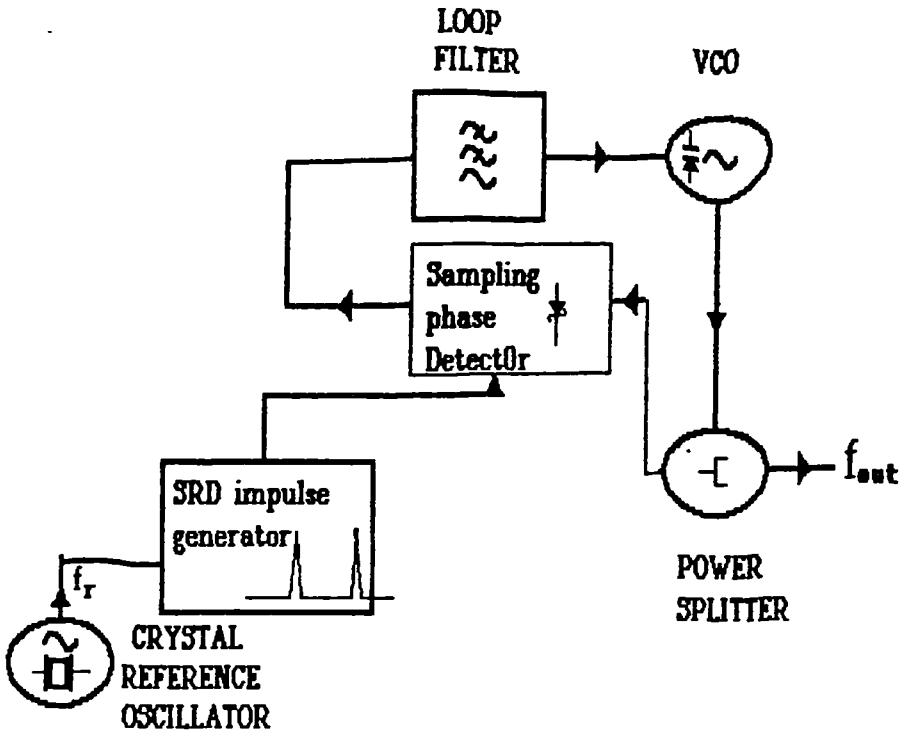


Fig 4.14 Harmonic sampling phase locked loop synthesiser

4.2.9 M/N Loop

A block diagram of a M/N synthesiser is given in Fig4.15 [Thrower, 1977]. This is so called because the output of the main synthesiser loop is divided by a factor M, as well as the N division in the feedback loop. Although there are now a greater number of channels possible, the output frequency channel step size is no longer constant. This problem may be overcome by the addition of another loop at the output of the synthesiser which frequency multiplies by *M*. An alternative name to this synthesiser is the tandem synthesiser since two division ratios are changed in tandem [ibid]. Although the M/N synthesiser is similar in architecture to the 3 loop synthesiser followed by a multiplier, the design is eased by the restricted range of the IF frequency. This synthesiser is covered in more detail in § 4.7 below. Advantages of the M/N synthesiser are:-

1) Reduced tuning range of the main oscillator required, therefore a lower noise oscillator performance could be achieved;

2) Reduced loop count to achieve the same level of performance as with the multiple loop synthesiser;

3) Simplified microwave circuitry required.

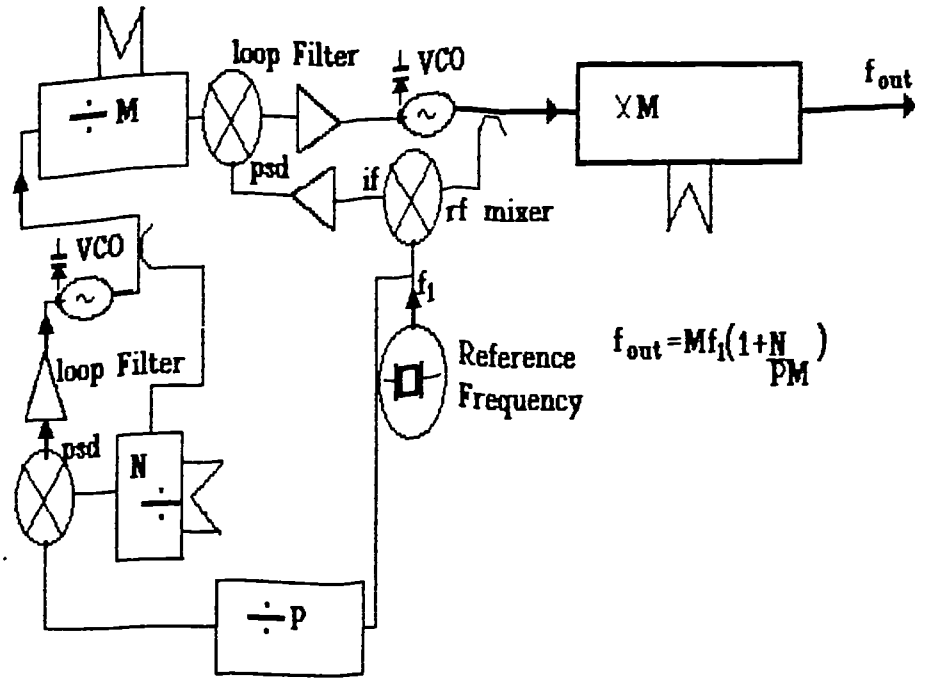


Fig 4.15 N/M Synthesiser block diagram

The main disadvantage of the N/M technique is that the multiplication ratio in the output must be changeable in integer steps, not always possible in microwave multiplier and phase locked oscillator circuits.

4.3 Direct analogue synthesis

4.3.1 Introduction

Direct analogue synthesis employs the use of mixers, filters, dividers and switches to perform mathematical operations on the reference frequency to obtain the output frequency. In order that the units are cost effective to build and test, it is vital that repetitive sections are employed [Manassewitsch, 1985b]. One such scheme is known as iterative direct synthesis. A bank of reference frequencies is used throughout this system, spaced apart a nominal frequency Δf. This bank of frequencies is coherently derived by multiplication or division from some master reference frequency and the same reference frequencies are used throughout the system. At the frequency selection matrix, these reference frequencies are input to the switch. The switch selects the appropriate frequency for that section to give the wanted frequency at the output. As a result, parallels can be drawn between multiple loop indirect synthesis blocks and direct synthesis blocks. This would provide an effective comparison between the PLL technique and the direct

synthesis technique. A commonly employed direct synthesis technique is the decadic double mix divide as seen in fig4.16.

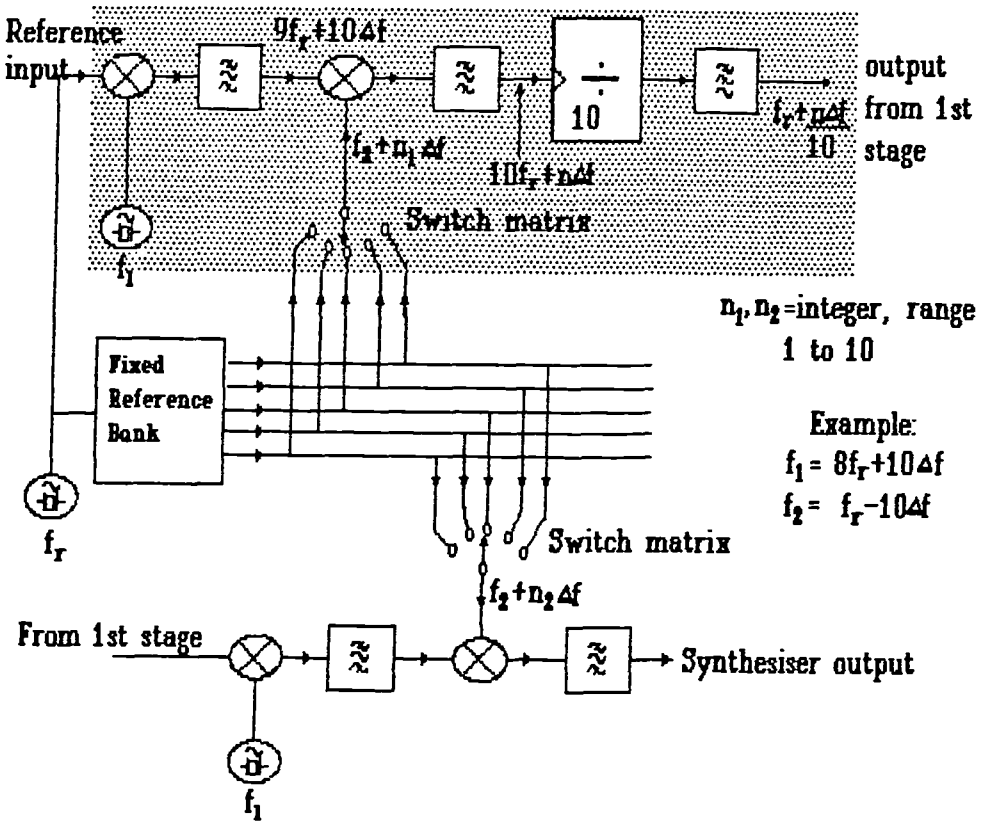


Fig 4.16 Example of double mix divide iterative direct synthesis

An example of specific frequencies that can be used are given in this figure. Also shown in fig4.8 is the equivalent PLL technique. In addition to the bank of reference frequencies, two master frequencies f_1 and f_2 need to be generated for the double mixing process. These must be related to the master reference frequency f_{ref} by the relationship:-

$$f_{in} = \left(\frac{f_1 + f_2}{9}\right) \qquad (4.2)$$

Output frequency selection is by means of switch matrices consisting of electronically gated RF switches. These are readily available with high reverse isolation and fast switching times. The shaded block shows the area which can be repeated for as many stages as necessary to give the desired resolution by feeding the output of the shaded block into the reference input of the succeeding stage. Finally, an iterative stage is provided at the output, but with the divider omitted. For the direct synthesis technique, with one iterative stage and one output stage, as shown in fig4.16, the synthesis equations are:-

$$f_{out} = \left(\frac{f_{ref} + f_1 + f_2 + n_1\Delta f}{10}\right) + f_1 + f_2 + n_2\Delta f = 10\, f_{ref} + \frac{n_1\Delta f}{10} + n_2\Delta f \quad (4.3)$$

Fixed frequencies f_1 and f_2 are determined by equation 5.2 and a mixing combination that gives the lowest levels of in-band spurious. These frequencies are used throughout all the iterative blocks. In equation (4.3) it can be observed that the factor n_1 is divided by a factor of 10 at the output and n_2 has unity weighting. Usage of a double mix system enables the elimination of tracking filters and the use of realistic filter values to enable the elimination of unwanted mixing products. A triple mix divide technique (fig4.17) can be used to space out the frequencies to ease filtering, and to reduce the generation of spurious products in the mixers.

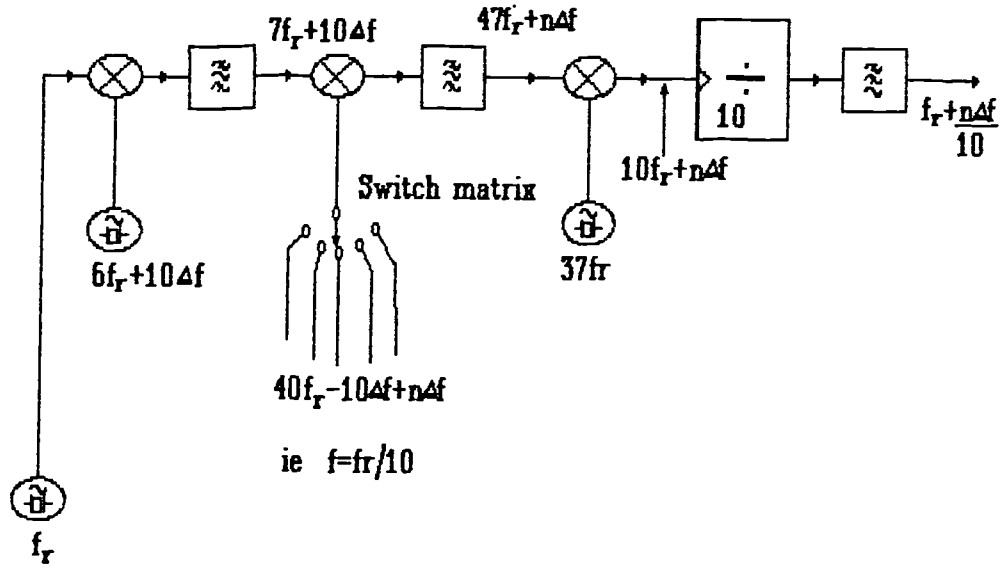


Fig 4.17 Triple mix divide synthesis eases filter requirements

The design of such circuitry is a non-trivial exercise owing to the presence of large numbers of potential spurious mixing products [Meyer, 1970].

4.3.2 Comparison of Direct Analogue synthesis with PLL technique

It has been quoted in published literature [Feinberg, 1986] that the advantage of the direct analogue synthesis technique is that it is much faster owing to the lack of loops. However such analyses often neglect the group delay associated with the spurious rejection filters required with such synthesisers [Stirling, 1987b]. Further work that could therefore be undertaken would be to compare the speed performance of a double mix divide synthesiser with an equivalent Z-transform speed optimised phase locked loop for similar configurations and for an identical spurious specification. The PLL technique allows considerable simplification in that one fewer reference frequency is required to be

distributed, and in addition one mixer and three bandpass filters are eliminated. The consequent reduction in the number of stages and frequencies generated eases screening requirements which will impact on costs per section. Another advantage is the fact that the mixer input frequencies are closer together so that in-band spurious frequencies are of a higher order and therefore lower in levels. This PLL approach is a classic case of a hybrid technique retaining the fast RF switching of the direct synthesiser.

4.3.3 Switching time considerations

The ultimate switching time of a direct analogue synthesiser is limited by the maximum clock rate of the divider (presently 14GHz). This would theoretically allow a switching time of around 10nS making it one of the fastest techniques known. The PLL approach may be limited by the slewing speed of the VCO, in this case, to something slower than this [Harris, 1989]. Research is presently being undertaken into harnessing the parametric oscillation phenomenon in varactors to enable division in millimetric synthesisers up to 100GHz [Harrison, 1977], [Harrison, 1983]. One distinct property of this type of synthesis is that a large frequency change will be faster than a small change as the small change has to ripple through a larger number of sections. A conclusion can therefore be drawn that although the switching speeds of phase locking and direct analogue synthesisers may be comparable, the limited slew rate of the VCO may provide the ultimate limitation to the switching speed of the fastest PLL synthesisers.

4.3.4 Output faults

One distinct advantage of the direct approach is that if a fault occurs then the result is likely to be no output rather than a free running VCO output.

4.3.5 Advantages of direct analogue synthesis

These are:-

i) Capable of the fastest switching time of any synthesis technique

ii) Very low phase noise close to carrier

iii) Failure likely to result in lack of output rather than an output at the incorrect frequency

iv) Capable of implementation in a small size at millimetre wave frequencies

v) Could accommodate high data rate modulation.

4.3.6 Disadvantages of Direct Analogue Synthesis

These are:-

i) Complex RF circuitry required

ii) Potential for spurious generation as a result of the number of mixers and frequencies present, therefore extreme care is required in the design and construction

iii) Labour intensive to build, therefore not cheap to manufacture in volume

iv) Far from carrier phase noise relatively high compared with PLL techniques

v) Difficult to commit to LSI circuitry, therefore limited miniaturisation possible

vi) Not so readily modified if finer resolution is required.

4.4 Direct digital synthesis (DDS)

4.4.1 Introduction

Direct digital synthesis (DDS) is a generic term for synthesisers which generate the output frequency by digital manipulation of the reference frequency. DDS is a purely fractional operation on the reference frequency, as opposed to phase locked loop synthesis which includes multiplicative operation on the reference frequency.

Types of direct digital synthesis include [Reinhardt , 1986]:-

i) Pulse output DDS

ii) Pulse swallowing DDS

iii) Triangle output DDS

iv) Sine output DDS

v) Phase interpolation DDS

vi) Jitter injection DDS.

The first three types, although simple in architecture, suffer from aliasing of the harmonic series, resulting in excessive spurious products. The method (v) applies a compensating phase correction to methods (i) and (ii) to reduce the phase error at the pulse transitions that result in spurious responses. Method (vi) [Wheatley & Phillips, 1981], [Wheatley, 1983] involves the use of a random dithering technique to spread the spectral errors throughout the DDS spectrum up to the clocking frequency. Method (iv), the sine output DDS, is the most common implementation of DDS, and involves the generation of a sinewave in an attempt to reduce the harmonic content that can be aliased back. Because of the high spurious signal content, the other types will not be considered further. Here the sine output DDS is to be examined further.

4.4.2 Sine Output DDS

A schematic diagram of a sine output direct digital synthesiser (hereafter to be referred to as DDS) is shown in fig4.18. It comprises a look up table which stores the phase voltage coefficients of a sinewave. The amount of phase advance per clock cycle is given by the value added in to the phase accumulation register at each clock cycle. This therefore controls the output frequency. The output of the look up table is applied to a digital to analogue converter (DAC) in order to construct the analogue output frequency. Unwanted higher frequency aliasing products are removed by the anti-aliasing products.

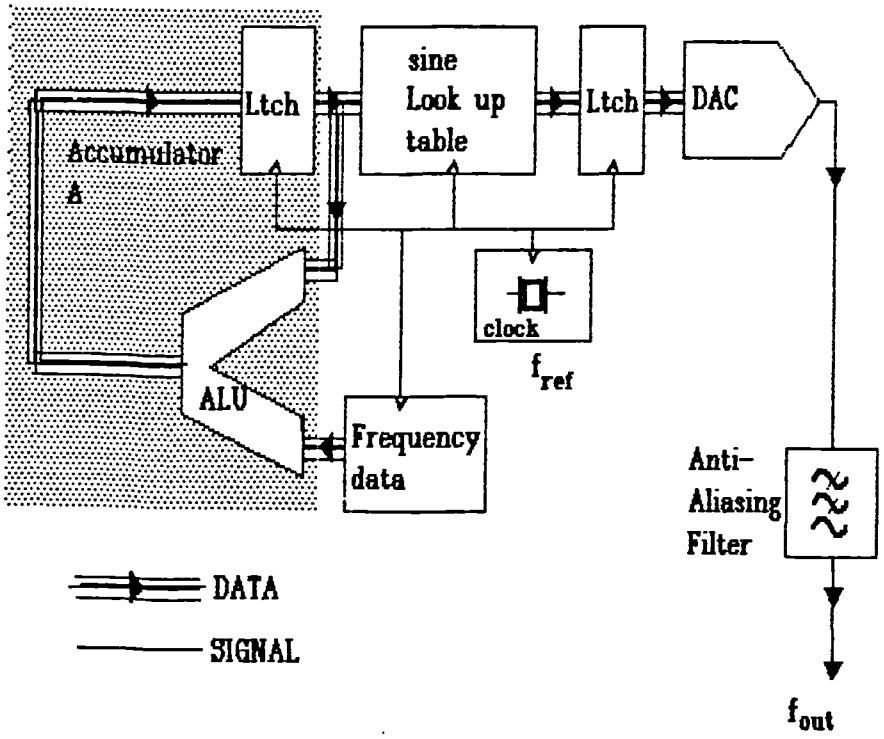


Fig 4.18 Direct digital synthesiser (DDS) block diagram

4.4.3 Operation of DDS

A fixed time interval is generated for the operation by means of a clock pulse, and the value added into the accumulator ALU advances the phase value entered to the look up table every clock cycle. Phase is therefore represented by the accumulator contents. The accumulator is effectively integrating the data value fed into it, therefore the input data represents frequency, since angular frequency $\omega = \frac{d\phi}{dt}$, where ϕ is the phase content of the accumulator.

If the content of accumulator A represents a complete cycle of phase, and is of dimension m bits, and the input is value p, then the phase advanced in one clock period will be:-

$$\phi = 2\pi p\ 2^{-m} \qquad \text{radians} \tag{4.4}$$

If the clock frequency is f_{ref} then the output frequency will be:-

$$f_{out} = \frac{\phi f_{ref}}{2\pi} \tag{4.5}$$

Therefore:-

$$f_{out} = p\ 2^{-m} f_{ref} \tag{4.6}$$

The minimum step size can be found be found by setting $p = 1$ and this gives the criterion for the size of the accumulator:-

$$m = \texttt{ceil}\left(\log_2\left(\frac{f_{ref}}{2\delta f}\right)\right) \tag{4.7}$$

where `ceil` is the nearest integer number greater than the result of the operation in brackets.

The generation of the output primary spectrum is shown in fig4.19. The actual synthesis process is a reversal of the sampling of a sinewave. Fig4.19a displays the effect of impulse sampling a sinewave. The frequency domain displays the output frequency at f_{out} and the two aliasing components at $f_{ref} \pm f_{out}$. These components are π radians out of phase with the f_{out} component, hence they appear below the frequency axis in fig4.19a.

In a practical synthesiser the output will be held at a constant level between clock transitions, so the effect of the hold function must be accounted for. In the time domain, the effect is convolution of the sampled sinewave with the hold function as shown in fig4.19(c). This is equivalent to frequency domain multiplication of the sampled sinewave with the hold function. An equation representing the hold function is given

below, with T_s equal to the clock period, and T_s,T_p equal to the peak DAC output amplitude:-

$$G(s) = \frac{T_s}{T_p} \exp\left(\frac{-j\omega T_s}{2}\right) \text{sinc}\left(\frac{\omega T_s}{2}\right) \qquad (4.8)$$

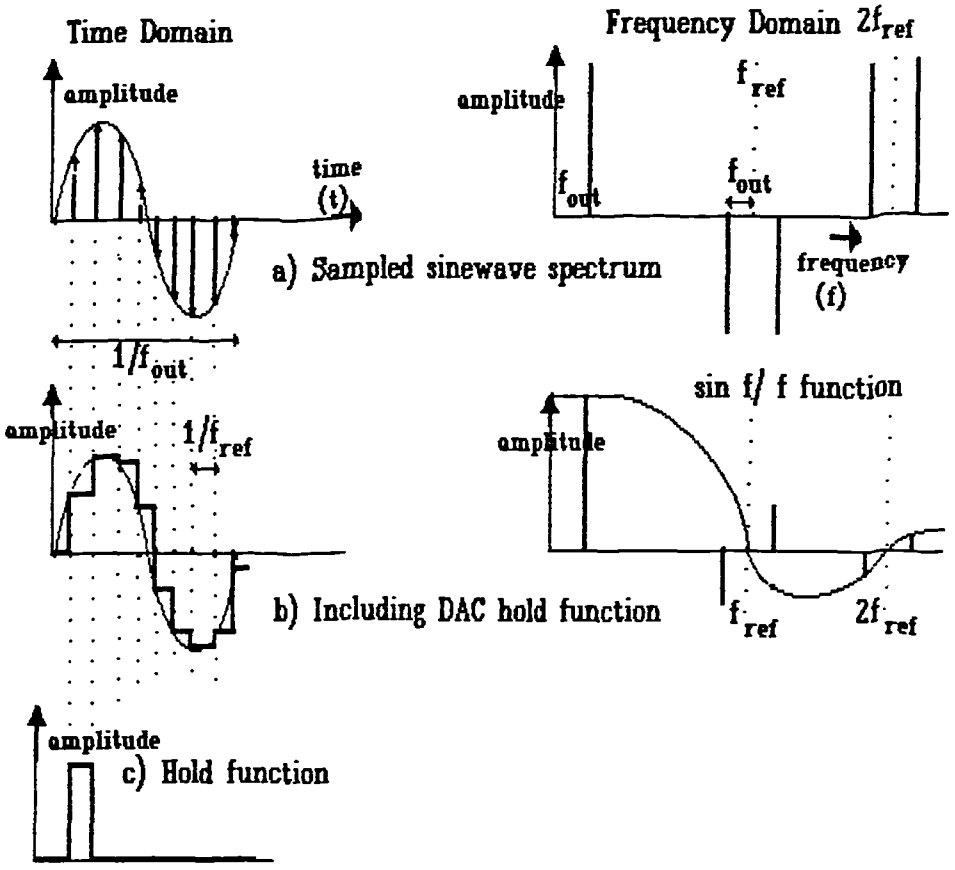


Fig 4.19 Operation of the direct digital synthesiser

The result of this is the spectrum displayed in fig4.19b. Nulls are present at the clock frequency and its harmonics. The aliasing component, if $f_{out} << f_{ref}$, is very much reduced by the sinc function. If f_{out} is close to $f_{ref}/2$, the aliasing component will be close in amplitude (3dB down on the low frequency level) and frequency and thus difficult to filter from the wanted signal. An anti-aliasing filter will therefore be required to remove the unwanted signal.

Being able to produce a realistic filter is the factor determining the ultimate limitation of the maximum output frequency. At $f_{ref}/2$, the output frequency and aliased component may cancel each other out. This technique, as with all sampling techniques, is subject to the Nyquist criterion. The aliasing component can be filtered out by the anti aliasing filter (shown in fig4.18). The ability of this filter to reject the aliasing component sets the maximum fraction of the clock frequency that can be output to typically $\approx 0.4f_{ref}$.

The phase word is a truncation of the accumulator value applied to the address input of sine wave table ROM. The width of this word is determined by the size of the ROM.

The advantages of the DDS technique are:-

i) It is suitable for very large scale integration (VLSI) implementation, therefore reducing chip count;

ii) Random phase noise is very low;

iii) There are no microphony sensitive VCOs or bandpass filters;

iv) Frequency step size can be arbitrarily fine, being only constrained by the size of the phase accumulation register;

v) Channel selection is extremely fast as it is not constrained by loop settling times or bandpass filter group delays.

The disadvantages are:-

i) Discrete spurious products tend to be relatively high;

ii) The output frequency is restricted at present to a few hundred MHz;

iii) For the higher speed versions the cost per unit tends to be rather high.

4.4.4 Phase noise in DDS

Since the reference clock frequency is higher than the output frequency, this tends to reduce the phase noise at the output of this type of synthesiser. Fig4.20 [Browne, 1988] displays published results for a typical direct digital synthesiser. The phase noise is generated at the input latch to the DAC and the DAC itself, so therefore these parts should be selected for low phase noise. Logic gate jitter in the latch and DAC controllers, combined with noise generated in the analogue circuits of the DAC contribute mainly towards the phase noise.

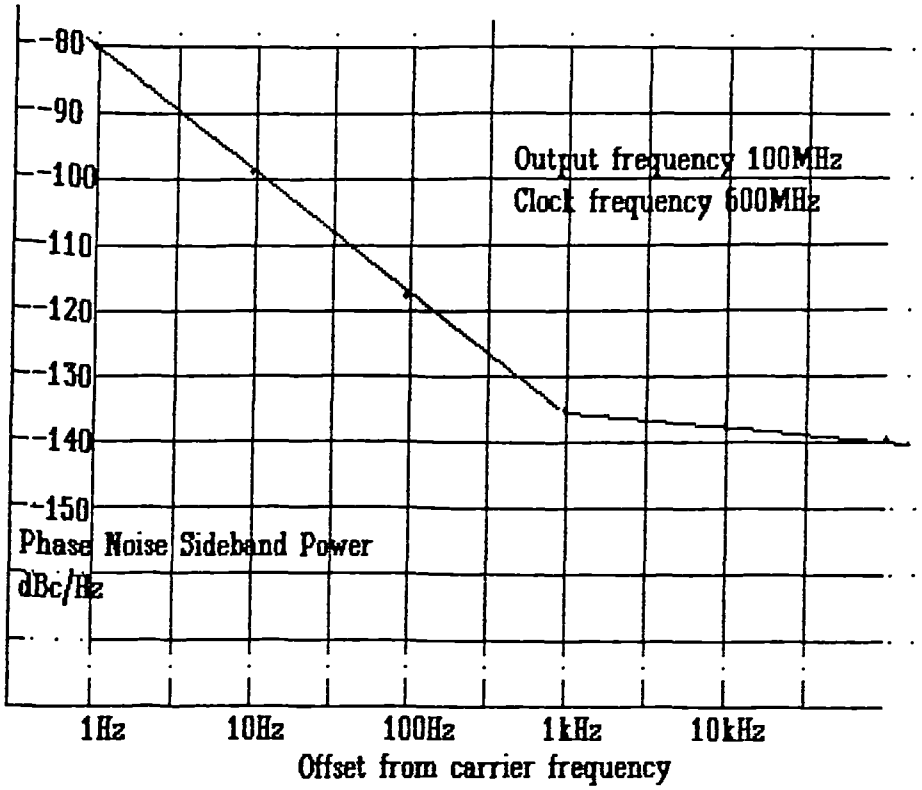


Fig 4.20 Published results [Browne, 1988] for a direct digital synthesiser

4.4.5 Frequency resolution

The minimum frequency step is set by the size of the accumulator. The number of bits, L, is given by:-

$$L = \texttt{ceil}\left(\log_2\left(\frac{f_{ref}}{2\delta f}\right)\right) \tag{4.9}$$

where `ceil` = integer larger than function, and δf = frequency step. If a very large scale integration VLSI synthesiser chip is purchased, then the size of the accumulator is fixed at chip manufacture and this is not alterable by the user. It is essential to acquire a chip that is capable of providing the finest frequency resolution that is likely to be required in a system; some accumulators allow for cascading to increase the resolution.

4.4.6 Switching time

This is determined by:-

1) The time required for a new phase step to be propagated through the system. For a pipelined adder this will be several clock cycles [Williams, 1987].

2) The time response of the anti aliasing filter.

There is a trade-off here in that if the maximum output frequency is only a small fraction of the reference frequency, then a simple filter will be required. The group delay will then be small; eg for a maximum of $f_{ref}/10$, a third order Chebychev filter of 1dB ripple would give a delay of $4/f_{ref}$. If the output frequency is allowed to be up to $0.4f_{ref}$, then a multistage elliptical filter would be required to reject the aliasing product at f_{ref}. In this case the filter delay could be as high as $200/f_{ref}$ for a 100MHz reference frequency system, and maximum output frequency of 10MHz [Zverev, 1967]. The propagation delay time would be approximately 80ns but with a maximum output frequency of 40 MHz this could rise to 2μs.

4.4.7 Discrete spurious

The major problem with the DDS technique is the generation of discrete spurious signals. There is a theoretical limit due to the quantization errors determined by the resolution of the DAC [Matteson & Coyle, 1988]. The total distortion products generated by quantization are represented by [Benn & Jones, 1989]:-

$$S/N = 2^n \sqrt{6} \tag{4.10}$$

This refers to the total power present in all spurious and harmonics (apart from an aliasing product at $f_{ref} - f_{out}$). However the close to carrier spurious is usually more relevant. This can be calculated by considering the DDS as a sampled data system acting on a quantized sine wave. The harmonics of the sampled signal become aliased back by the reference frequency as in fig4.21. If the output frequency is an integer sub-multiple of the reference frequency, then all the higher order products alias back to the output frequency and no close to carrier spurious signals are generated. Predicting where the spurious signals are likely to occur is a straightforward task, but predicting the magnitude of the spurious is extremely complicated. The frequency distance of the closest spurious to the carrier can be found from consideration of the sampling and aliasing process [Nicholas & Samuli, 1987]. Each output frequency will have harmonics associated with it due to the non-linearities in the DDS process.

If f_0 and f_{ref} are the output and reference frequencies, then harmonics will exist at mf_0 and nf_{ref} where m and n are integers. When a harmonic at mf_0 is near to the output frequency f_0 away from a harmonic of the clock sampling frequency nf_{ref}, then that harmonic is aliased back to near the output frequency.

Spurious signals are therefore generated at:-

$$m f_0 \pm n f_{ref} = f_{ref} \pm f_s \tag{4.11}$$

therefore:-

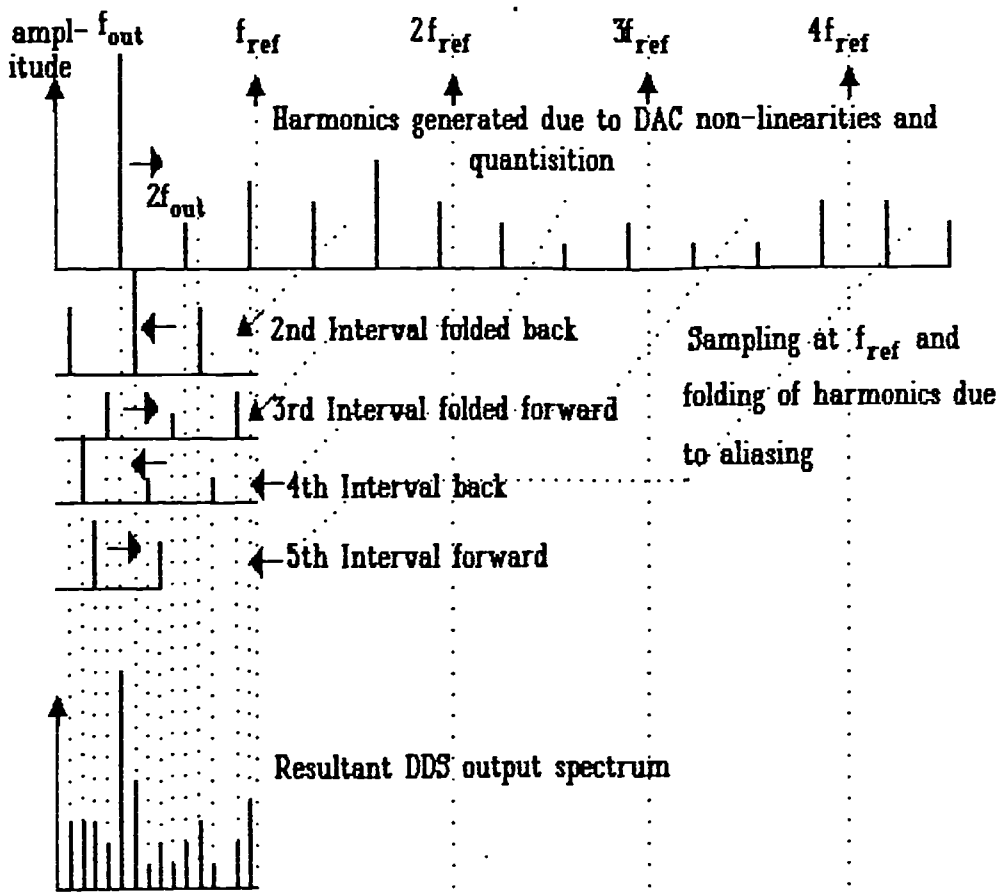


Fig 4.22 Aliasing back of harmonic distortion products to give spurious signals

$$f_s = m\, f_o \pm (n-1)\, f_{ref} \tag{4.12}$$

where f_s represents the spurious sideband frequency offset from carrier. Representing the highest common factor of f_o and f_r as:-

$$f_{out} = x\, f_1 \tag{4.13}$$

and:-

$$f_{ref} = y\, f_1 \tag{4.14}$$

where x and y are integer values, then:-

$$f_s = (mx \pm (n-1)y) f_1 \tag{4.15}$$

if f_1 is the highest common factor of f_r and f_o, then for any m and n, the lowest non zero value of $(mx \pm (n-1)y)$ is 1. Therefore, the closest spurious frequencies will be at f_1. In a direct digital synthesiser there will always be a lowest common factor to f_r and f_o,

which is determined by the accumulator word length L. This relationship between the minimum step size and the reference frequency is:-

$$\delta f = \frac{f_{ref}}{2^L} \tag{4.16}$$

If a frequency select word p is input to the synthesiser, then the output frequency is:-

$$f_o = p\ \delta f \tag{4.17}$$

substituting (4.16) and (4.17) into (4.19) and (4.20) then:-

$$x\ f_1 = p\ \delta f \tag{4.18}$$

and:-

$$y\ f_1 = 2^L\ \delta f \tag{4.19}$$

therefore:-

$$y\ p = x\ 2^L \tag{4.20}$$

If the highest common factor of p and 2^L is C, then the minimum spurious frequency from carrier is:-

$$f_s = C\ \delta f \tag{4.21}$$

However if an offset from this frequency of f is introduced, then spurious frequencies will be generated at:-

$$\text{Lower sidebands} = f_{out} - ((nm + 1) - 1)\delta f \tag{4.22}$$

$$\text{Upper sidebands} = f_{out} + ((nm - 1) + 1)\delta f \tag{4.23}$$

where n is an integer and m is the nearest integer submultiple of f_{out}. The consequence of this is that the level of close to carrier spurious decreases as m increases, as the power present in higher harmonic products diminishes, but often this rate of decrease is slow. More work is required to establish the exact harmonic levels.

The principal sources of spurious signals in direct digital synthesis are due to [Williams, 1987], [Burr Brown, 1988], [McCune, 1988]:-

i) DAC non-linearities;

ii) Non-linearities in the switching transients of the DAC;

iii) Data skew at the input to the DAC;

iv) Phase and amplitude word truncations.

In a practical DDS, the first three sources are likely to dominate the fourth. The DAC suffers from two types of non-linearity [Analogue Devices, 1984] and both enhance the production of harmonics. However the integral non-linearity produces low harmonics (up to the 5th) while differential linearity produces high order harmonics (>5th). Integral non-linearity is only a problem at frequencies close to the maximum output frequencies ($> 0.25f_{ref}$). The spurious products fall rapidly with reducing frequency. Differential linearity on the other hand produces large numbers of high order spurious even at low output frequencies ($< 0.1f_{ref}$). Therefore it is essential to employ a DAC which has been designed for very good differential linearity, such as is required for video applications. Switching transients can be reduced by employing a fast sample and hold at the output of the DAC as in fig4.22. The sample and hold is switched to track after the DAC settling time. It is vital however that both hold feedthrough and intermodulation effects of the transient are minimised [Williams, 1987].

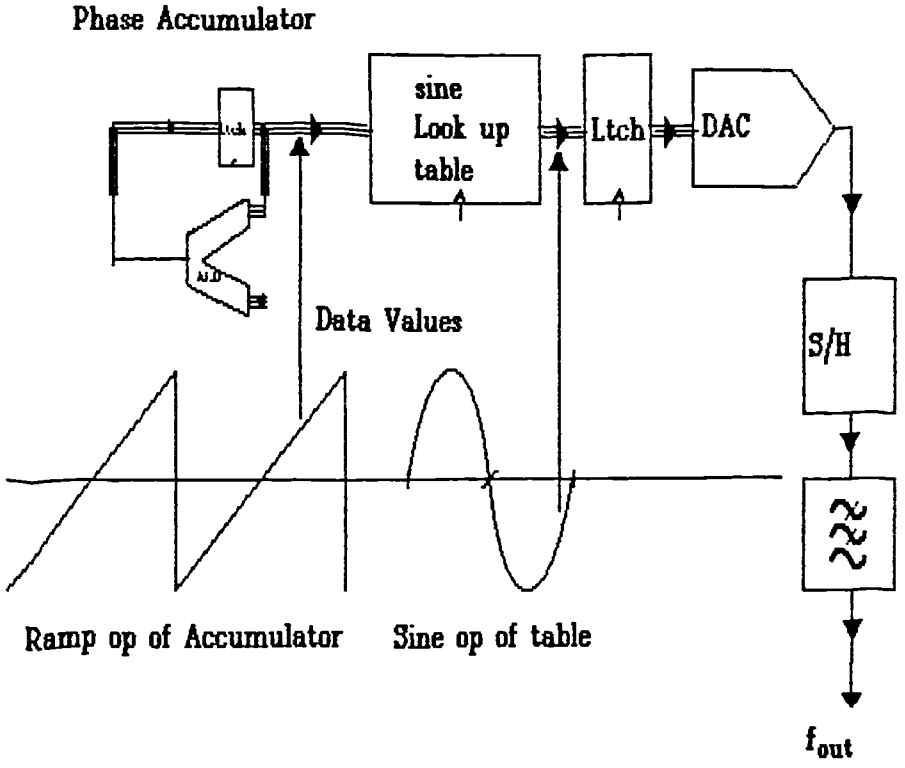


Fig 4.22 Direct digital synthesiser with sample/hold to reduce glitches

Data skew is caused by different input bit lines to the DAC changing at different intervals in time. This results in unwanted output transitions at the output of the DAC with catastrophic effects on the spectral purity. Fig4.23 displays the basic synthesiser performance of an experimental DDS clocked at 7.6MHz and with an output frequency of 799kHz.

4.4.8 Numerical Example

The above spurious analysis can be illustrated by a numerical example. Measurements were taken for a DDS clocked at 4MHz. This has a 16 bit accumulator and it is programmed with the value 13088. The output frequency is determined by equation (4.9) to be:-

$$f_{out} = 4 \times 10^6 \times 2^{-16} \times 13088 \qquad (4.24)$$

$$f_{out} = 798.82813\,kHz \qquad (4.25)$$

The resulting output is displayed in fig4.23.
In order to determine the spurious spacing of the sideband spectrum, the highest common factor must be found for f_{out} and f_{ref}. The highest common factor of 13088 and 2^{16} is 32, since 13088/32= 409, which is a prime number. From the relationship (4.21), the spectral lines are spaced at 32 step size intervals apart in frequency, in this case 1.953125kHz. Therefore, a spurious signal will be present at this interval across the entire output spectrum, but the levels will vary greatly between different spurious products. This can be observed from the spectrum analyser plot of the synthesiser output, fig4.23. The closest spurious signals are at 32 × channel spacing away from carrier, and can be only just observed as they merge into the spectrum analyser IF filter skirts.

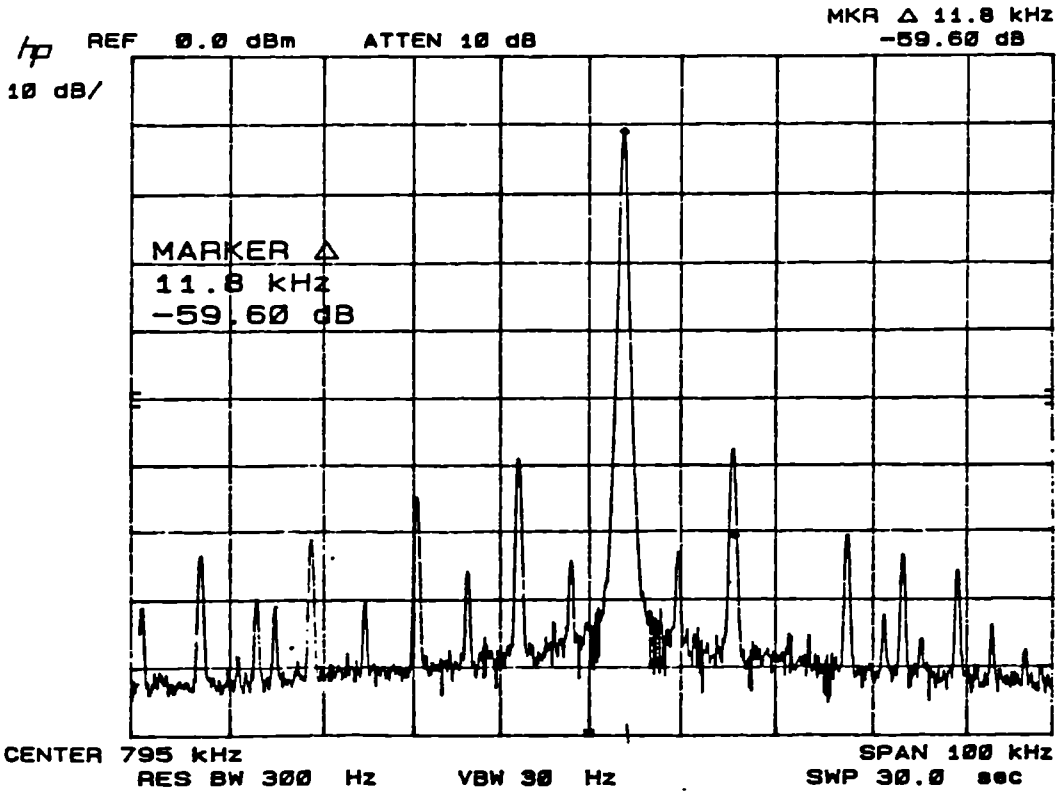


Fig 4.23 Output spectrum of direct digital synthesiser clocked at 4 MHz

4.4.9 Cost of direct digital synthesis

At present the cost increases rapidly with reference frequency (f_{ref}). This is due to the fact that:-

i) Specialised high frequency processes are required to manufacture the transistors in the integrated circuits;

ii) Special design techniques are required to optimise the speed of the operations within the system [Williams, 1987];

iii) Fast DDS is very demanding on DAC technology.

If a 2 GHz reference frequency is to be used the transistors must have a transition frequency (f_T) of greater than 20 GHz [Saul & Taylor, 1989a], [Saul & Taylor, 1989b]. However if the reference frequency is 20 MHz then cheap custom ULAs (uncommitted logic arrays) can be employed.

The DAC could be one of the many standard video devices which are already in volume production, and are therefore economic. The cost of a synthesiser in this case could be < £50. Comparing published results for the direct digital synthesiser and for a digiphase synthesiser [Underhill, 1986], [Browne, J 1988] would indicate that the performance of such a unit would be comparable, in terms of discrete spurious, with the basic digiphase phase locked loop technique. Phase noise performance however would be much improved on account of the higher reference frequency. The performance would be inadequate for use at microwave frequencies and so additional techniques are required in order to synthesise at GHz frequencies. This suggests a requirement for the use of hybrid synthesis techniques.

4.5 Downconversion/upconversion schemes

4.5.1 Application

With the aid of the synthesiser architecture survey reported in the first part of this chapter, a study is now undertaken of possible combinations of such architectures most suitable for satellite communications use. A satellite system is likely to employ several downconversion and upconversion stages. These arise in:-

i) The transmitter (typically to 70MHz, and again to 700MHz prior to final carrier frequency);

ii) The satellite (generally a single downconversion stage, albeit of fixed translation frequency);

iii) The receiver (typically from RF to 70MHz, perhaps via an intermediate 700 MHz, and again to lower IFs within the modem).

Each stage of conversion relies upon an oscillator or synthesiser of some kind. One of the criteria that is most instrumental in determine the structure of a synthesiser is its position in the satellite link.

4.5.2 Position of synthesisers in a satellite link

The ideal position for a synthesiser in an upconversion or downconversion system (eg. a commercial satellite system) is the first local oscillator on account of the smaller percentage tuning range required at that point. This simplifies the frequency conversion problems since mixer intermodulation products will be of a higher order. If the antenna is to be

close to the receiver, for example with portable satellite equipments, then the first stage can be synthesised. However, this can create problems if the antenna is to be remotely located. In such a case, the synthesiser will have to be remote programmed across the link from the antenna to the main unit. It would be considerably simpler, therefore, if a fixed local oscillator could be used for the first LO as shown in fig4.24. This could therefore be a self contained unit, requiring only the IF connections (with power). A further advantage of this is that the synthesiser could be located close to the modem where it could aid signal acquisition. Chapter 9 covers this form of downconverter arrangement by discussing a split synthesis technique. In such an arrangement, each local oscillator stage is synthesised. The problems with this approach is that front end bandwidth will be limited, extra complication is involved due to three stages of conversion, and spurious signal problems are more likely due to the wide tuning range at L-band. In addition, chapter 9 shows that the phase noise induced BER degradation of the spilt synthesis technique is worse than using a single low phase noise synthesiser because the phase noise produced from each synthesised LO is additive.

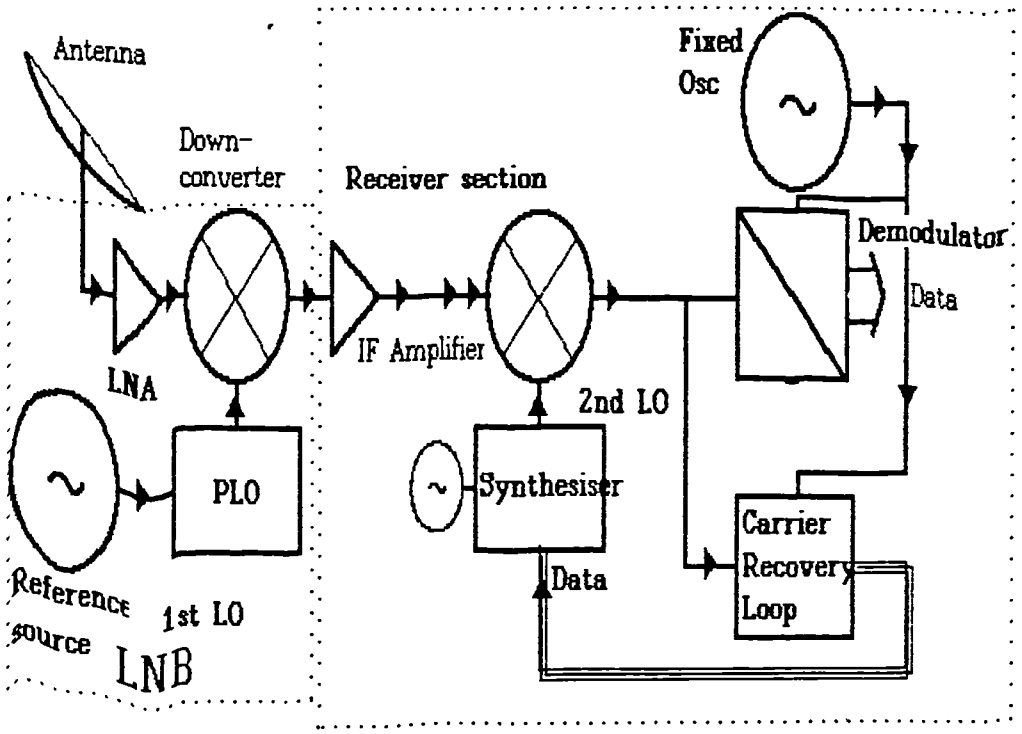


Fig 4.24 Fixed front end approach to downconverter/demodulator design

With the simplified schemes discussed in chapter 9, it may be possible to mount all the RF sections at the antenna, and transmit the baseband signals down the cable. If this was possible, considerable savings in cost could result as the long downlead cable could be inexpensive low frequency cable rather than expensive low loss RF cable.

For the remainder of this chapter, both fixed frequency and synthesised first local oscillators will be investigated.

4.6 Fixed first local oscillator

We concern ourselves here with the choice of the first local oscillator (LO), as this exemplifies the design consideration. The following choices are likely to be available for the first LO in a receiving system:-

i) Free running dielectric resonator oscillator (DRO);

ii) Phase locked oscillator (PLO) with L-band cavity oscillator and multiplier;

iii) Phase locked DRO;

iv) Phase locked voltage controlled oscillator;

v) Microwave oscillator (direct).

4.6.1 Free running DROs

4.6.1.1 Characteristics

Free running DROs have conventionally being used for commercial television receive only (TVRO) applications. The DRO is housed within the low noise block converter (LNB). For data communications this type of oscillator poses three problems:-

i) Excessive phase noise;

ii) Phase "hits" due to mechanical construction;

iii) Frequency stability.

The phase noise of a free running DRO compared with a multiplied crystal oscillator is observed is fig4.25. The free running oscillator plot was obtained by measurement from a typical TVRO LNB. The performance of the system can be quantified and it will be

shown in chapter 9 that a considerable loss in sensitivity (ie. link budget penalty) will be the result.

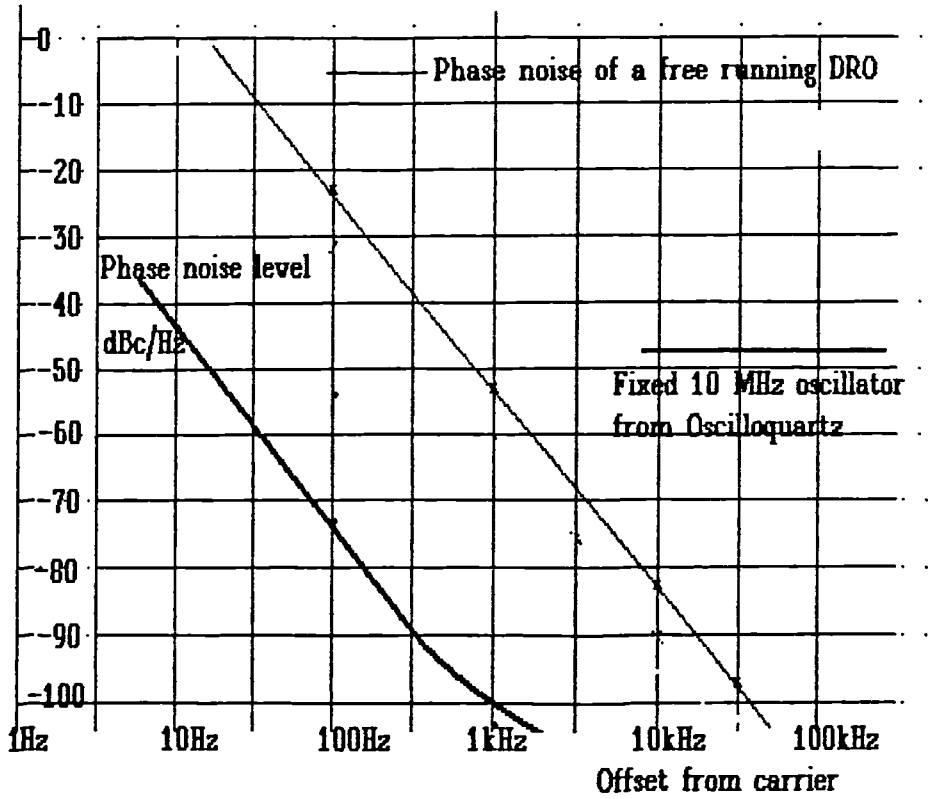


Fig 4.25 Comparison of multiplied crystal oscillator and free running DRO phase noise

4.6.1.2 Phase "hits" with DROs

Phase "hits" are also an important consideration in data systems beside phase noise and are further discussed in §6.5 Higher data rate systems may be more seriously degraded since more data is likely to be lost during a "hit". With a free running DRO, the mechanical construction of the oscillator and oscillator housing would have to be carefully designed to avoid phase "hits". These are due to sudden movements of the mechanical dimensions of the frequency determining elements as the environmental parameters change. The resulting sudden discontinuities in phase give errors in the data modulation.

4.6.1.3 Frequency stability

The frequency stability performance of a DRO over the operating temperature range may mean that a search over a frequency range of many MHz is required in order that the receiver can acquire the signal. Such search and acquisition can take considerable time and is therefore undesirable.

4.6.2 Phase locked oscillators

4.6.2.1 The need for phase locking

Chapter 9 illustrates that excessive BER degradation is likely over a data link if free running DROs or cavity oscillators are used. To take advantage of the improved phase noise performance of a multiplied crystal oscillator, some form of phase locking of the microwave oscillator is desirable; in order to produce a phase locked oscillator (PLO), some form of electronic tuning is required. Microwave oscillators that can be tuned are cavity oscillators, DROs,VCOs, and YIG tuned oscillators (YTO). YTOs are most likely to be used in tuneable local oscillators so discussion of these will be reserved for §4.7 of this chapter.

4.6.2.2 L-band cavity PLO

This is a mature technology consisting of a cavity oscillator operated at high power levels driving a multiplier filter arrangement which selects the required output harmonic. The disadvantage of this is that the cavity oscillator tends to be bulky. The mechanical construction is critical in order to avoid phase "hits" and this results in cavity oscillators being expensive. Another problem is that around one watt of power is generated at L-Band, and this may cause problems if sensitive receiving circuits are present in the same chassis.

4.6.2.3 Ceramic resonator oscillator

The ceramic resonator oscillator is a variation on the cavity oscillator PLO above whereby the mechanically tuned cavity oscillator is replaced with a ceramic cavity oscillator. The high dielectric constant of the ceramic cavity makes possible considerable miniaturisation.

The advantages of the ceramic resonator are:-

i) Compact construction;

ii) Freedom from phase "hits" due to the fact that the frequency determining element is a totally enclosed single unit;

iii) The frequency stability is excellent.

The disadvantage of this is that multiplication is still required up to the final output frequency together with high power at L-band.

4.6.3 Phase Locked DRO

Dielectric resonator oscillators, on account of the high Q of the resonator, are capable of good far-from-carrier phase noise. The close-to-carrier phase noise is generally poor however, due to the higher $1/f$ noise of microwave active devices and some method of phase locking to a low close-to-carrier crystal oscillator would therefore be desirable. In order to achieve this a harmonic sampling loop can be used to phase lock a DRO. The advantage is that the fundamental frequency oscillator means the output is at local oscillator frequency. The lack of requirement for a multiplier and filter results in very compact construction.

The disadvantages are:-

i) The lack of frequency stability and the lack of harmonic power with the crystal oscillator at around 10MHz means that a VHF crystal oscillator is required as a reference oscillator;

ii) It is more susceptible to phase hits as the resonant frequency is to some extent dependent upon the oscillator enclosure;

iii) The DRO has a very limited tuning range, therefore is suitable for fixed frequency oscillators only.

4.6.4 Voltage controlled oscillators

The advantage of voltage controlled oscillators (VCOs) is that fundamental output frequency operation can be achieved. However, the following disadvantages result with VCOs:-

i) The low Q of these results in poor far-from-carrier phase noise performance;

ii) The poor frequency stability demands that a high reference frequency be used in order to avoid the output being at the wrong harmonic of the reference frequency.

4.6.5 Microwave oscillators

At present, the only microwave oscillator that can compete with the crystal oscillator is the High Overtone Bulk Acoustic Resonator or HBAR. Currently, these are expensive, although this may change in future.

4.6.6 Choice of crystal oscillator frequency

The above synthesisers generally rely upon some kind of crystal reference, and here there are many design considerations to be taken into account. For close-to-carrier phase noise, the main contribution is noise from the crystal resonator. A 10MHz crystal can be made with lower resonator phase noise than a 100MHz crystal when the noise is normalised at a particular output frequency, and it is more desirable to use a 10MHz crystal oscillator as a reference in order to obtain low close to carrier phase noise. This poses the following:-

i) More demand is placed upon the phase locking technique;

ii) A frequency stable oscillator must be used at microwave frequencies.

For the phase locking technique, a harmonic locking phase detector is more desirable because of simplicity and lower phase noise than the divider type phase locking.

Chapter 7 discusses the problems associated with multiplying from a frequency as low as 10 MHz. Although harmonic locking phase detectors using SRDs are capable of low phase noise, increased flicker noise will result at 10MHz rather than VHF. For the lowest close to carrier phase noise therefore, an optimum scheme is a VHF crystal phase locked to a low phase noise 10MHz crystal.

4.7 Tuneable first local oscillators and synthesisers

4.7.1 Introduction

§4.5.2 of this chapter indicates that considerable simplification can be achieved if the first local oscillator can be made tuneable. For this to be viable, especially with remote mounted front ends, cost effective rugged compact synthesiser units must be capable of being realised. Obstacles that must be overcome are the high frequency of the output and the temperature range over which an antenna mounted unit must operate. The aim of the remainder of this chapter is to determine the most viable approach to a synthesised first local oscillator. This is accomplished by a study of the architectures and performance of three microwave synthesiser implementations. These 3 types are:-

i) VHF synthesiser and PLO

ii) L band Cavity Synthesizer

iii) M/N synthesiser.

4.7.2 VHF synthesiser and PLO

One possible approach to the problem of providing a synthesised microwave local oscillator is a VHF synthesiser followed by a phase locked oscillator (PLO). The architecture of a VHF synthesiser suitable for satellite communication applications is shown in fig4.26. Although the output frequency of the synthesiser is at VHF, a microwave phase locked oscillator (PLO) must be used in order to obtain a synthesised signal at microwave frequencies.

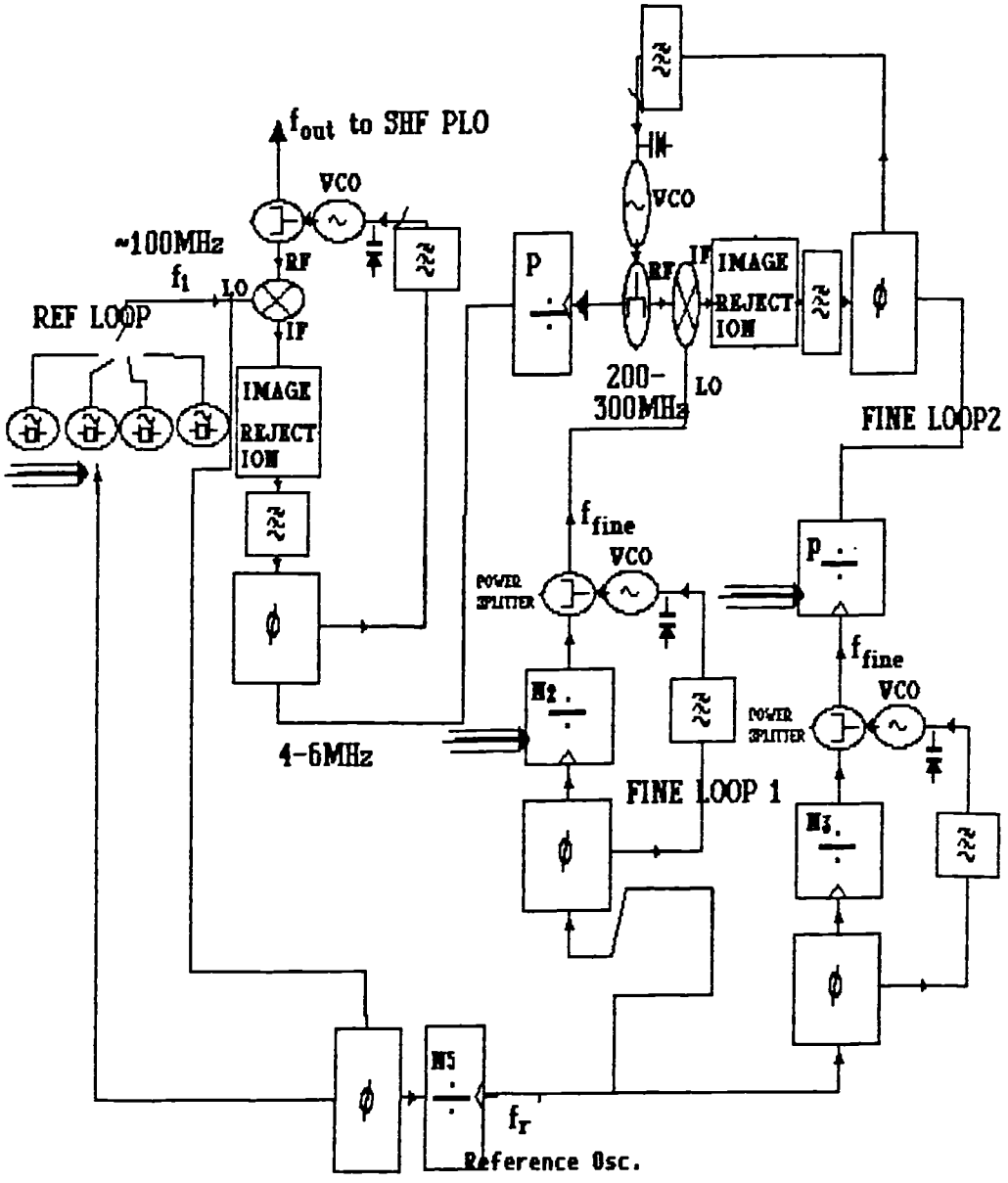


Fig 4.26 Multiple PLL VHF synthesiser

Usually this PLO would consist of an L-band cavity oscillator followed by a multiplier. The L-band oscillator is phase locked to a harmonic of a comb generator. Since a two stage frequency multiplication process is involved the overall multiplication factor *M* must be factored into two integer multiples m_c and m_m where m_c is the multiplication of the input reference frequency to L-Band and m_m is the output multiplication ratio. Therefore the total multiplication ratio m is given by:-

$$M = m_c\, m_m \tag{4.26}$$

Restrictions are therefore placed on the value of m such that m_c and m_m are themselves integers. As a result of this, the M/N architecture described in §4 2.9 of this chapter cannot easily be implemented. The VHF synthesiser must therefore be of the multiple loop type described in §4 2.3 of this chapter. Since the output frequency is multiplied by *M*, strict demands are placed on the spurious signals and phase noise outputs of the VHF synthesiser. The majority of fractional techniques would have excessive spurious outputs to be used directly as the reference frequency input to a PLO. To obtain a 60dB spurious level at 20GHz, a spurious level of better than -106 dBc is required at 100MHz. Since a multiplication of *M* times occurs in the PLO, the tuning range at the output of the VHF synthesiser is F_{tune}/M. In order to guarantee a small value of the synthesiser intermediate frequency (IF), the reference frequency f_1 must be made tuneable. Therefore a bank of switched crystals must be used for this reference, phase locked to a master reference. f_1 is an integer multiple of the synthesiser reference frequency f_r. Therefore, the output frequency of the crystal oscillator loop f_1 is given by:-

$$f_1 = f_r N_1 \tag{4.27}$$

A small IF frequency is necessary to avoid mixer related spurious being introduced into the loop. A recommended implementation of a VHF synthesiser is given in fig4.26. The synthesis equation for this loop is:-

$$f_{out} = \frac{f_{ref}}{2}\left(\frac{N_3}{P^2} + \frac{N_2}{P}\right) + f_1 \tag{4.28}$$

Two cascaded fine loops are used, each succeeded by a scaling divider of ratio P. It is this scaling divider that enables fine frequency stepping at the output. Ratio N_2 is that of the programmable divider in the first fine loop and N_3 is that of the second fine loop. Ratios N are therefore programmable and P is fixed. A single synthesiser IC can be used for each loop such as the Qualcomm CA 3036 IC which includes the dividers and the phase detector [Qualcomm, 1990].

With the 3 loop synthesiser of fig 4.7 a problem exists in that meeting the requirements of the phase noise specifications at the output requires too coarse phase steps in the fine loop.

In order to overcome this problem, a further fine loop is required to be mixed in. Therefore an extra mixing loop is also required to combine these loops. A total of 6 phase locked loops are required, including the PLO at the output. The architecture is ultimately limited by the step size of the fine loop satisfying the phase noise and microphony requirements of the synthesiser. If finer step size is required, then more loops must be cascaded. In order to keep the phase noise and spurious signals within the specification bounds, a large number of crystals may be required, approximately one per 100MHz at 10 GHz. The synthesiser must be split into 8 screened sections (not including PLO). Tuning range at the local oscillator is restricted by the tuning range of the cavity oscillator multiplier to approximately 8% of the output frequency.

4.7.3 Synthesis at microwave frequencies

It is possible to implement a multiple loop synthesiser at microwave frequencies [Stirling, 1987d]. This would have a speed advantage since there is nothing placed at the output of the synthesiser. The disadvantage of this however, is that care would have to be taken to ensure that synthesiser IF products do not swamp a sensitive receiver. This would require a proliferation of active devices at microwave frequencies, and would therefore have a severe impact on cost. In addition, the microwave components must be adapted to the output frequencies required, making it difficult to economise by scale in production.

4.7.4 L Band synthesiser with cavity

The L-band cavity synthesiser is an extension of the VHF synthesiser. Because of the increased VCO frequency, the reference frequency of the coarse loop can be increased. This allows for increased rejection of spurious signals and phase noise. A reduction in the number of reference crystals to two is now possible. A recommended implementation of such a synthesiser is given in fig4.27. The synthesis equation is as below:-

$$f_{out} = \left(\frac{f_{ref}}{2}\left(\frac{N_2}{P}\right) + f_{ref}N_1\right)M \qquad (4.29)$$

Factor N_1 is the programmable frequency multiplication ratio of the coarse loop, N_2 is the programmable divider in the fine loop and P is the scaling divider at the output of the fine loop. Since the synthesiser IF band is mixed in at L-band the post oscillator multiplication is lower than with the VHF band. As a result of the lower multiplication ratio, noise degradation from the IF is reduced by approximately 23dB. This allows the use of only one IF loop for a step size of down to 125kHz at 10GHz.

The problem with this type of synthesiser is that as higher values of the final output frequencies are required, 20logN degradation of the IF phase noise would result. This would require a major restructuring of the synthesiser as frequencies are increased or the

step size is reduced. Two L-band oscillators are required alongside the appropriate mixing and phasing circuitry at L-band. In order to provide a low phase noise coarse loop, this loop has to employ a secondary comb generator. Fig 429 shows the coarse loop in the shaded area. The use of two comb generators implies a more complicated coarse loop which must be partitioned internally, so the total number of screened compartments must be not less than 6, not including the cavity oscillator-multiplier. Unfortunately the comb generators are not easily adapted to a high level of integration.

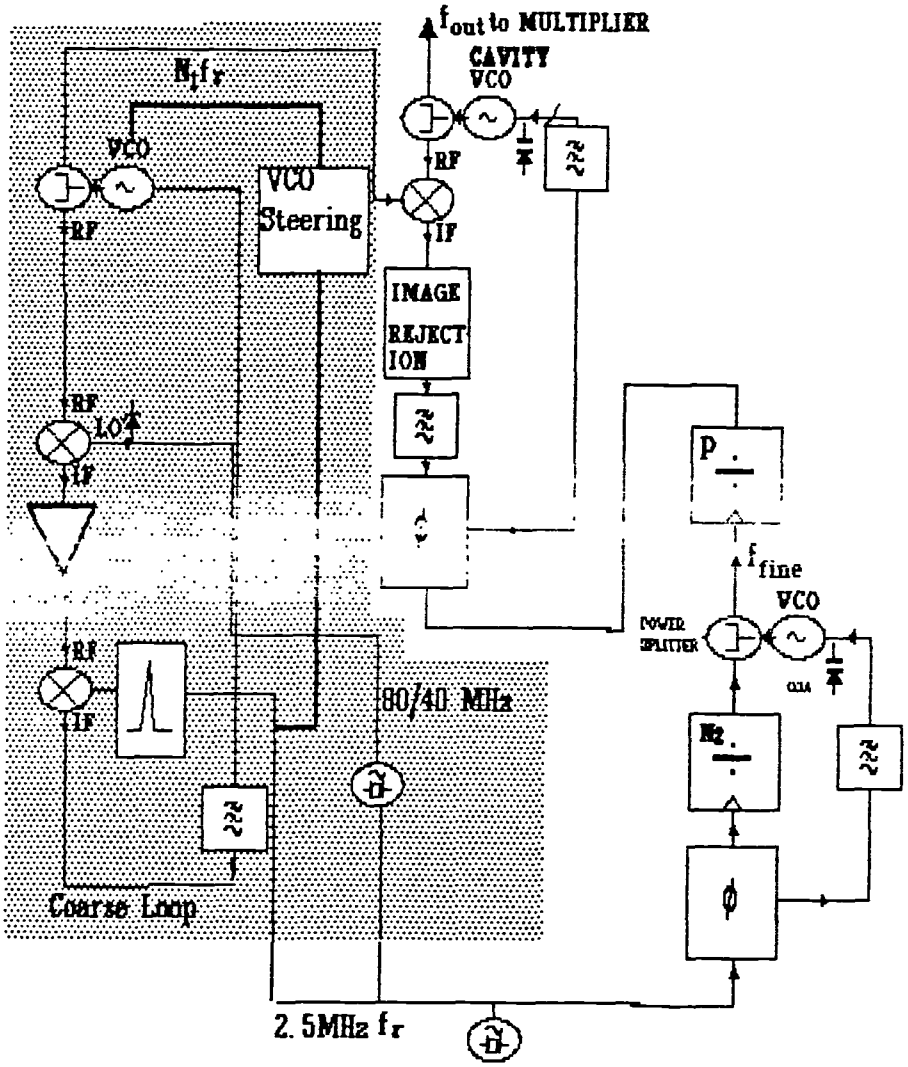


Fig 4.27 Block diagram of L-Band cavity synthesiser

4.7.5 YIG oscillators

Another approach is to discard the cavity multiplier approach and use a tuneable microwave oscillator. One type of tuneable oscillator that is suitable for the high frequencies required is the Yttrium Iron Garnet (YIG) oscillator. Such oscillators have been used in military and electronic warfare applications for some time, although only recently have they been cheap and compact enough for civil satellite communication

applications. A YIG oscillator consists of a Yttrium iron garnet in the shape of a sphere that has a resonant frequency which is dependent upon the applied magnetic field. There are many references in the literature eg.[Osbrink & Grande, 1989] to this type of oscillator so only a brief description is required. Tuning the YIG resonator is equivalent to tuning both the inductance and the capacitance simultaneously of a conventional oscillator. Therefore a very wide tuning range is possible. The loaded Q of the resonator is typically between 200 and 300 [Grande, 1990], a value between that of the cavity oscillator or DRO and that of a varactor controlled oscillator. Since the resonant element of the oscillator is compact, YIG oscillators have proved themselves resistant to phase "hits" [Vella, 1991], and are therefore highly suitable for data communications applications. YIG oscillators have too wide a tuning range for most satellite communication applications, so therefore it is possible to compromise tuning range for power consumption and size by means of permanent magnet bias. The phase noise compared with other oscillators is shown in fig 4.28 obtained by measurement at Ferranti [internal communication, G. Parkinson, 1991].

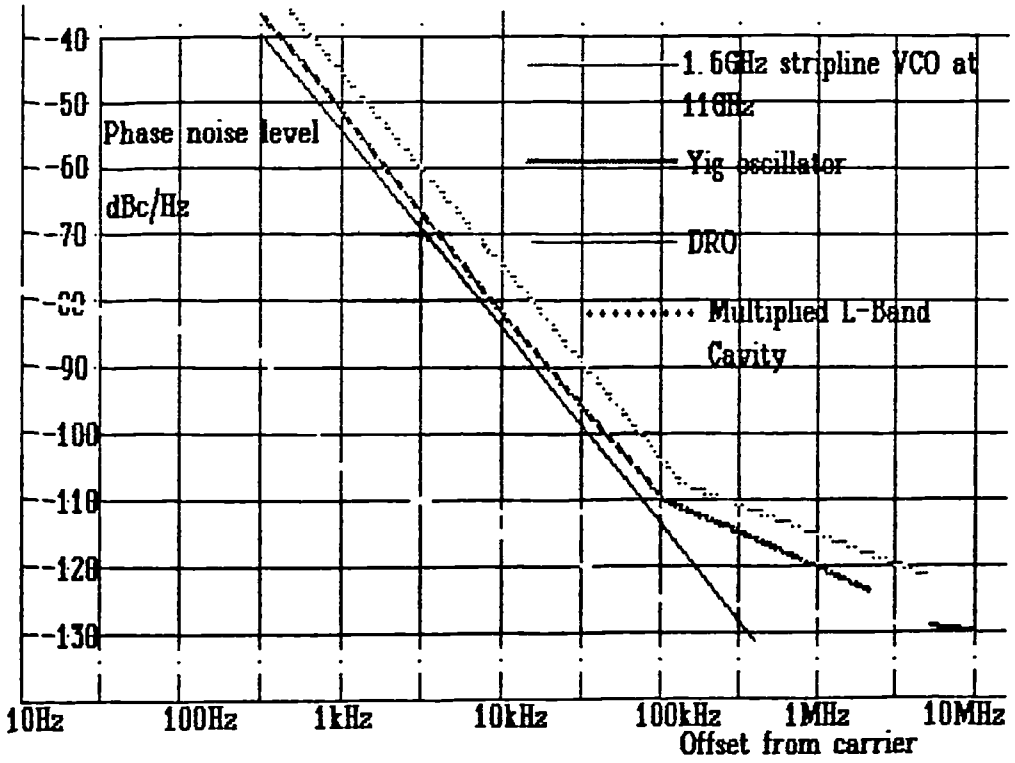


Fig 4.28 Phase noise of free running microwave oscillators

4.7.6 YIG phase locked oscillators

By the use of a microwave step recovery diode sampling detector, it is possible to phase lock a YIG oscillator to a VHF reference source. The advantage of such an arrangement is that the multiplication ratio can be any integer value. Therefore it is possible to use this arrangement to form a synthesiser. However, the step size in this case would be 50MHz minimum; if smaller step sizes were required then the phase locked oscillator must be combined with other synthesiser methods. A block diagram of a YIG phase locked oscillator is given in fig4.29. A programming voltage is applied to the main tuning coil port; this is a large tuning coil which provides the main magnetic field for the tuning.

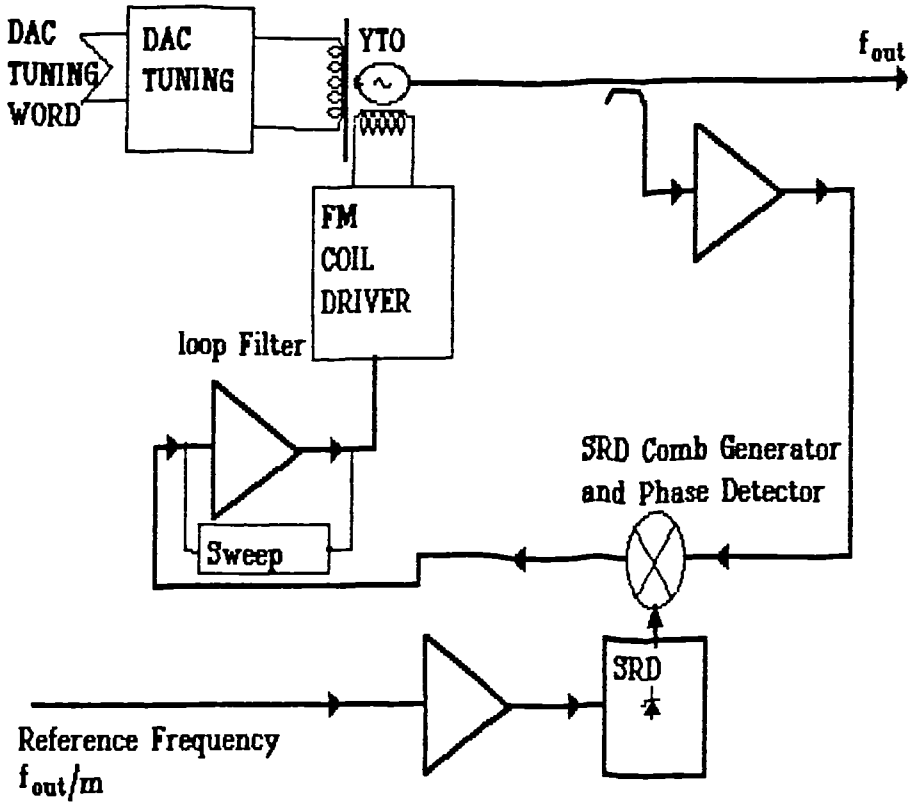


Fig 4.29 Block schematic of YIG PLO

This large coil is capable of tuning the frequencies over many GHz. However the coil must have a large inductance and therefore is relatively slow to tune. The 3dB bandwidth of such a tuning is likely to be a few kHz [Law, 1985] and is insufficient for phase locking purposes. Therefore a separate FM coil is provided for this purpose. Only a limited tuning range of approximately 70MHz is possible from the FM coil. The inductance of the coil is very much lower. As a result of reduced inductance, bandwidth

is increased. A typical 3dB point of an FM tuning coil is 1MHz. This increased frequency is much more suitable for systems that must incorporate some form of phase locking. If the reference frequency is made equal to a frequency above that of the tuning range of the FM coil then the YIG oscillator is capable of a wide phase locking range.

Unlike the cavity phase locked oscillator, no output multiplier is required, therefore there is complete freedom over the selection of multiplication value *M*. The value *M* refers to the harmonic of the reference frequency that the output oscillator locks to. *M* is the ratio of output frequency to the reference frequency; the frequency multiplication factor of the YIG phase locked oscillator (YIG PLO) is restricted only by the tuning range of the main tuning coil. The composition of the phase locked loop is identical to a conventional phase locked source apart from the change of oscillator. The main coil is pre-tuned to approximately the correct frequency by means of the pre-tune DAC. When the loop is not locked, the loop filter is arranged to sweep the FM coil tuning, until the YIG frequency is an exact harmonic of the reference frequency. In this case, phase locking will occur.

4.7.7 The YIG N/M synthesiser

The fact that a YIG oscillator has complete freedom over the selection of ratio *M* enables the use of a modified synthesiser architecture. Since there is no multiplication at the output of the YIG PLO, the factor m_m in equation (4.26a) is unity and therefore the multiplication ratio *M* can take on any integer value. This extra flexibility can be fully exploited in an additional synthesiser architecture shown in fig4.30. Such an architecture is known as the N/M synthesiser, since it is based upon the use of two division ratios that can be changed. Being allowed this extra degree of freedom enables some of the complexity of the above described architectures to be avoided. The frequency synthesis equation is:-

$$f_{out} = f_{ref}\left(\frac{N_1}{2M} + \frac{N_2}{8M}\right)M \qquad (4.30)$$

All division ratios *M* and N are programmable. N_1 is the division ratio of the divider in the feedback of the coarse loop and N_2 is the division ratio of the divider in the fine loop. At the output frequency, the values of *M* cancel, but at VHF, the variable value of *M* enables a reduced tuning range of f_{ref}/M rather than f_{tune}/M with concomitant reduction in the level of spurious signals generated by the mixer in the transfer loop (see §5.4.6). Furthermore, this enables the effective multiplication of the fine loop to the output frequency to be *independent* of the final output frequency. There is therefore no need for architectural changes as the output frequency is increased. There is only one reference frequency required which means that this could be a high quality reference source.

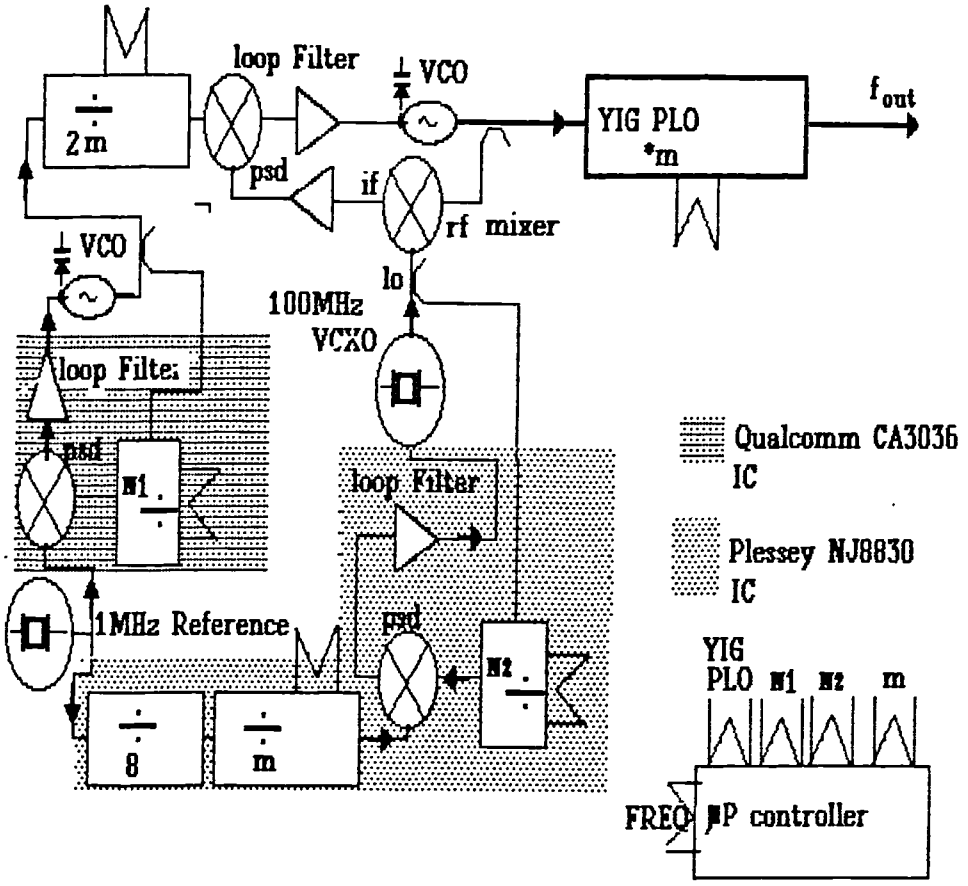


Fig 4.30 Block schematic of YIG N/M synthesiser

With this type of synthesiser there is unfortunately a limit to the minimum resolution of the fine loop. This is determined by the phase noise and microphony of the coarse loop. However the frequency increment at the mixer per fine step is very small. As only one reference frequency is required, it is possible to employ a VCXO for this frequency and form this into a synthesiser with a large division ratio. In this case output microphony and phase noise will be determined by the VCXO and a narrow loop bandwidth of approximately 1 Hz must be used. Providing the loops are sufficiently isolated from one another, the spurious generating mechanism of this loop is virtually non existent enabling - 80 dBc to be achieved at the output at 10GHz. This does not include spurious modes introduced by the crystal.

§4.2.1 shows that the problem with single chip PLL synthesisers is that loop bandwidth and phase noise performance must be compromised over that possible with entirely discrete components. However the extra flexibility allowed by the M/N architecture enables a synthesizer frequency plan such that this reduced performance can be tolerated.

Unlike the previously discussed synthesisers, the demands on the various loops are such that a high level of integration is therefore possible. Single chip synthesisers can be used for the fine and coarse loops. Demands of the coarse loop is still quite severe for the majority of synthesiser chips, but the latest generation of synthesiser chips, such as the Qualcomm CA 3036 has sufficient flexibility to meet the demands of the coarse loop. Since the reference loop is a narrow band loop the step size can be reduced to low values (100 Hz is a realistic minimum). If a narrow loop bandwidth is used in the fine loop, the phase noise becomes determined by the crystal oscillator, and the demands on the synthesiser chip are removed. Therefore a PMR synthesiser chip, such as the Plessey NJ8830, can be used. Although the Plessey device has poorer phase noise performance and is inflexible in its choice of reference frequency, it is a fraction of the price of the Qualcomm chip, consumes less current, and has a much smaller surface area. Thus, integration of the two loops give this architecture the highest integration level of all the viable alternatives.

A further advantage of the YIG M/N synthesiser is that the YIG harmonic locking section is a stand alone product itself, a YIG PLO. This gives a further advantage in terms of product rationalisation. The microwave section is simplified and can be made output frequency independent. Microwave component costs are therefore reduced drastically.

One problem with this type of synthesiser is that fine frequency selection is through a narrow band loop that will have a very long settling time. The settling time could be of the order of seconds, even if adaptive loop filtering is used. However, for the vast majority of satellite communication work which does not require regular channel changes this will not be a difficulty. If rapid frequency selection is required, then a DDS variant of the synthesiser must be provided.

The multiplication ratio M is large and therefore care must be taken to ensure that the frequency multiplying components do not degrade performance. This effect is further investigated in chapter 7.

4.7.8 N/M loop with DDS

In order to provide a truly dynamic synthesiser a modification is required. Fig4.31 indicates that the narrow loop bandwidth synthesiser disappears and the coarse loop is replaced with a DDS (direct digital synthesiser). Settling time will now be of the order of microseconds. This form of synthesiser is especially suitable for tracking applications. A DDS has capability of arbitrarily fine frequency resolution enabling the step size to be set by the controlling microprocessor, rather than the configuration of the loops. The division is necessary to ensure that the DDS stays within the phase noise and spurious signals

specifications. The analogue circuitry is very much simplified compared with the other synthesiser methods. Spurious products generated in an unmodified DDS are in general too great for this implementation. Chapter 8 outlines methods that can be used to reduce the spurious levels of the DDS to levels compatible with this method.

Some synthesiser implementations follow the DDS with a narrow bandwidth phase locked loop to remove some of the spurious products [Vella, 1991]. In applying this, they have rejected the single most important asset of a DDS: its ability to rapidly change frequency. A loop bandwidth of 1 kHz means that a frequency change will take 10's of milli-seconds, whereas a DDS is capable of doing this in nanoseconds. The implementation which is proposed here follows the DDS with a wide bandwidth loop, thus reducing frequency change times.

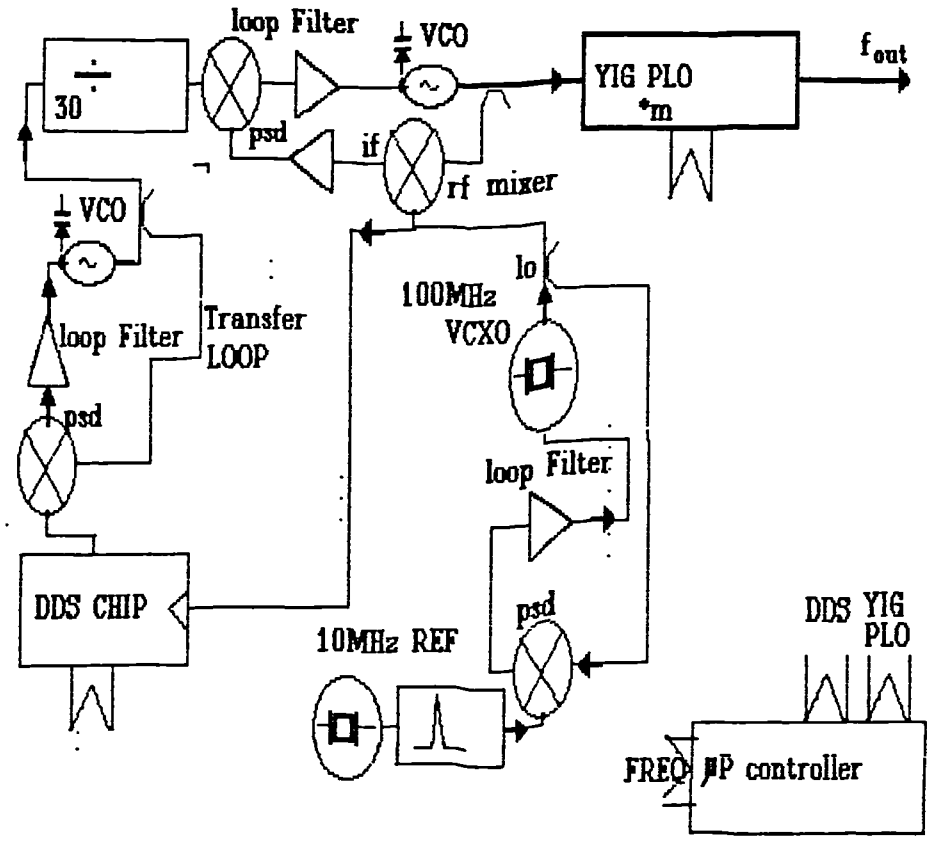


Fig 4.31 Block schematic of YIG synthesiser with DDS

Such an arrangement is possible because of the spurious reduction techniques outlined in chapter 8. The DDS replaces the coarse loop in the M/N synthesiser. Since the DDS has such fine resolution that no interpolation is required, the 100MHz reference is fixed frequency, and the divider in the output of the DDS can be a fixed divider. This allows considerable simplification by removing a high frequency variable divider. The transfer loop at the DDS output is used to reject the broadband noise output from the DDS which would otherwise add in a root sum of squares manner at the divider input. The loop bandwidth must be approximately equal to the minimum frequency at the output of the divider.

4.8 Expected phase noise performance of microwave LO

4.8.1 Estimation of phase noise

A prediction of phase noise levels of the synthesiser types given in the previous section is given here. Phase noise data is taken from the various oscillators and synthesiser processing circuitry measurements performed by the author and detailed elsewhere in this thesis.

4.8.2 VHF synthesiser

For the VHF synthesiser of fig 4.26, the principal phase noise contributors are:-

i) The single chip synthesiser phase detector and dividers;

ii) The synthesiser transfer loop;

iii) The 100MHz processing components and the step recovery diode harmonic generator;

iv) The Cavity oscillator;

v) The VCXO.

4.8.2.1 Using a single IC synthesiser

An example of an integrated circuit PLL ÷N synthesiser is the Qualcomm 3036 IC. The phase detectors and dividers in the Qualcomm IC all contribute phase noise to the output signal within the loop bandwidth. This phase noise has been measured by Qualcomm engineers [Qualcomm 1991] to be -150dBc at 1 MHz reference frequency. Other measurements on ECL type dividers indicate similar figures (see § 5.7.2.4). By

multiplying this signal by the effective transfer function to the output frequency of the synthesiser, f_{out}, the final output phase noise can be determined. 1 MHz is chosen as a comparison frequency according to the criteria given in §4.2.1 of this chapter.

4.8.2.2 Synthesiser transfer loop

The synthesiser transfer loop covers from 4 to 6 MHz in this synthesiser implementation. Using a FAST TTL phase detector, the phase noise contributed can be estimated according to equation (5.46) of chapter 5 to be a maximum of -148 dBc/Hz.

4.8.2.3 Step recovery diode phase noise

Step recovery phase noise data is taken from published measurements displayed in §5 7.5 for a 100 MHz input.

4.8.2.4 VCXO phase noise

The VCXO phase noise dominates the close to carrier spectrum. Standard low phase noise crystals are used since 5 of these are required for each synthesiser unit. The phase noise plots are taken from measurements by the author. These measurements agree with those obtained by Driscoll [1985].

4.8.2.5 VHF synthesiser and PLO phase noise at microwave frequencies

Fig 4.32a and fig 4.33 series of plots show the expected phase noise of the VHF synthesiser at 10 GHz and 20 GHz respectively. The VHF synthesiser is as the configuration shown in fig 4.26. Coarse loop phase noise performance is dictated principally by the VCXO phase noise. Fine loop contribution to the overall phase noise is determined by the Qualcomm synthesiser chip. This is multiplied up by $20\log N$ to the synthesiser output frequency output so the fine loop phase noise contribution is frequency dependent. Phase noise performance of such a configuration comes close to the Eutelsat specification at 20 GHz [Eutelsat 1989]. It must be stressed that this is an overall system specification and therefore refers to the sum of all contributions.

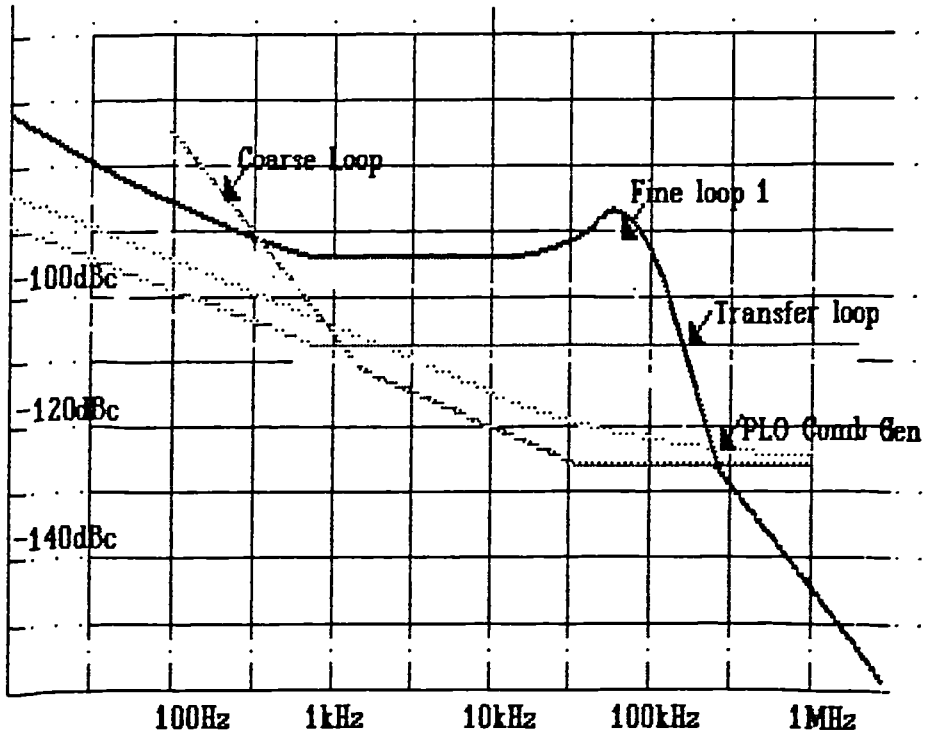


Fig 4.32 Phase noise contributions, VHF synthesiser at 10GHz

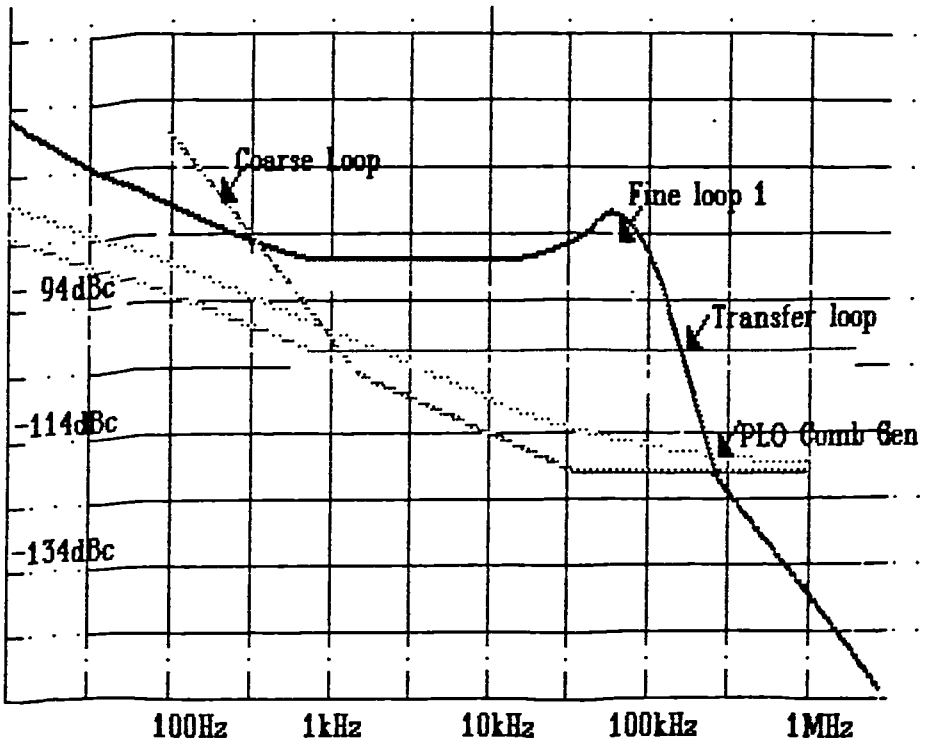


Fig 4.33 Phase noise contributions, VHF synthesiser at 20GHz

4.8.3 L-Band synthesiser

4.8.3.1 Coarse loop phase noise

With the L-Band synthesiser, the coarse synthesiser will be the dominant source of phase noise. Multiplication of the phase noise from the single IC loop is less than with the VHF synthesiser. Once again, the dominant source of phase noise is frequency dependent. In order to realise the phase noise specification, considerable complication of the coarse loop is required including the use of a secondary phase detector.

The phase noise is determined by the secondary sampling phase detector, SRD phase noise and crystal oscillators. Measurements obtained from a working circuit are plotted in fig 4.34. The sampling of SRD noise by the secondary phase detector represents the largest phase noise component, except at very low offset from carrier frequencies.

4.8.3.2 Fine loop phase contribution

The phase noise arises principally from the Q3036 chip and the VCO. Since the loop mixing is at L-Band, rather than VHF, the translation multiplication factor to the output is reduced by 23dB.

4.8.3.3 Transfer loop

As with the fine loop, since the multiplication factor is reduced, a 23dB reduction in transfer loop contributions as compared against the VHF synthesiser occurs.

4.8.3.4 L-Band synthesiser phase noise at microwave frequencies

Fig 4.34 and fig 4.35 show the expected phase noise of the L-band synthesiser. Such a synthesiser has phase noise which is dominated by the secondary sampling phase detector in the coarse loop. Contributions from the Qualcomm synthesiser IC and transfer loop are very much reduced on account of the lower multiplication factor to the synthesiser output frequency. The phase noise is reduced over that of the VHF synthesiser. It can be deduced from the simulation of chapter 7 that the multiplier after the cavity oscillator should contribute negligible phase noise on account of the high drive frequency.

The L-Band cavity oscillator synthesiser could be modified to replace the fine loop with a DDS synthesiser. In this case the output from the DDS will be connected directly to the transfer loop, and the secondary sampling detector omitted from the course loop. Such a combination would give a similar phase noise performance to the DDS/YIG combination outlined in §4.8.5 below in this chapter, and would enable high data rate modulation of the synthesiser. However, the presence of the multiplier at the output limits the flexibility of the synthesiser arrangement.

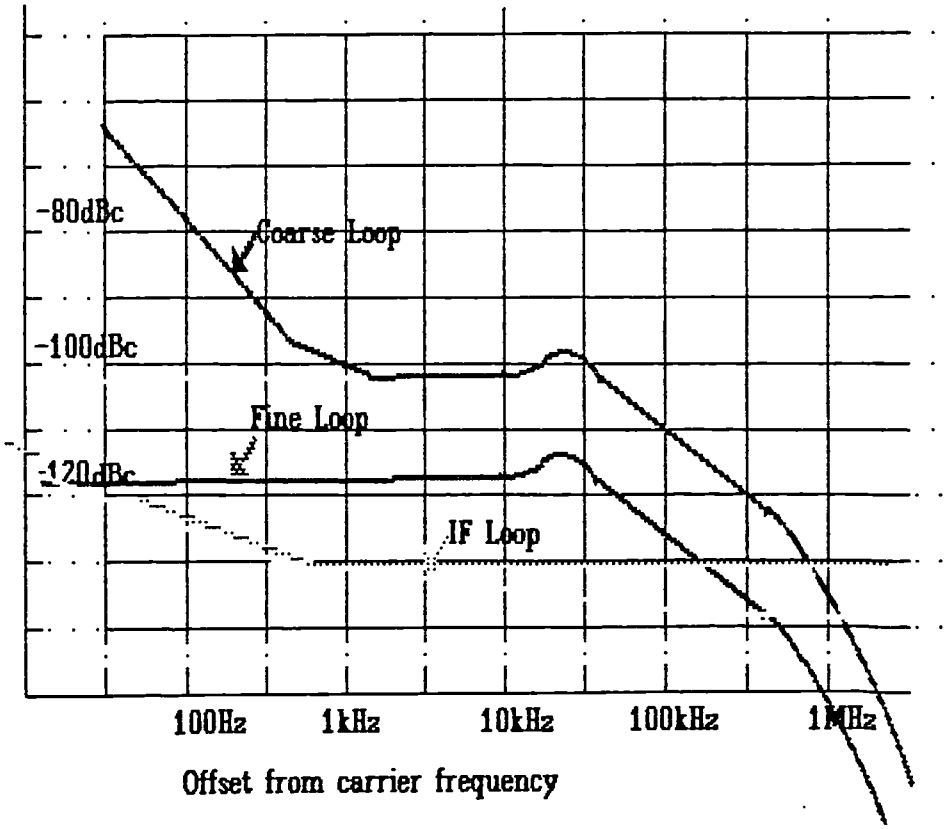


Fig 4.34 Phase noise contributions, L-band cavity synthesiser at 10GHz

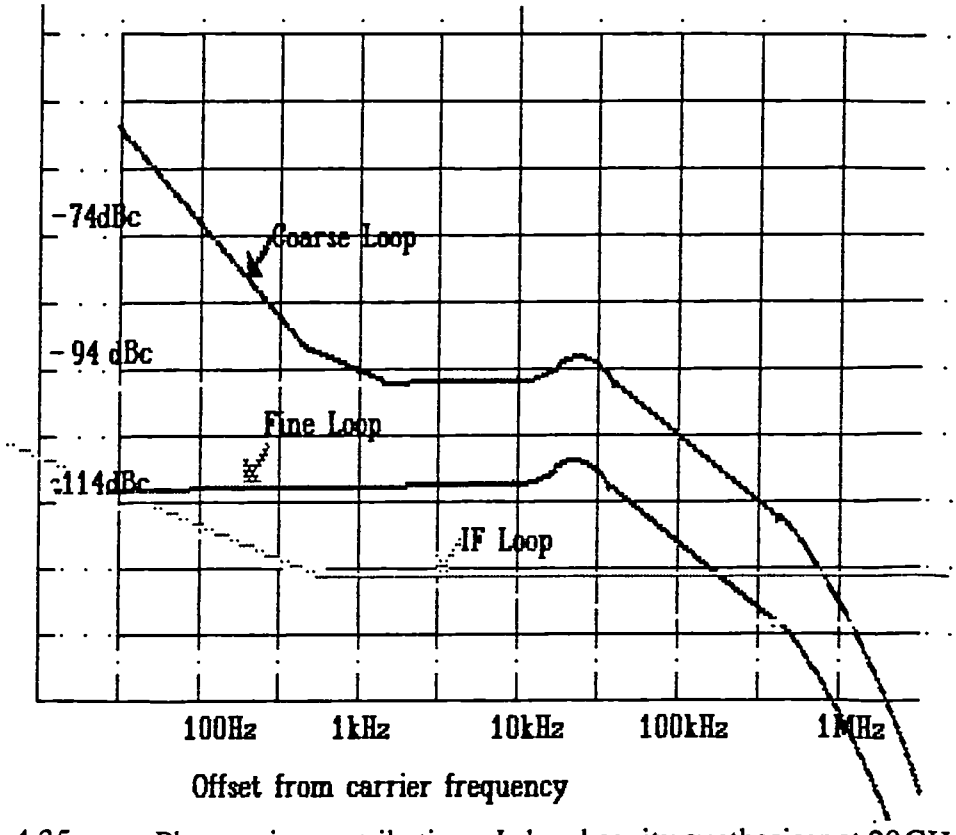


Fig 4.35 Phase noise contributions, L-band cavity synthesiser at 20GHz

4.8.4 YIG M/N synthesiser

4.8.4.1 Coarse loop phase noise

Using the M/N architecture enables the division ratio after the coarse loop to be higher; a reduction in phase noise transferred to the output will therefore follow. Increasing the output frequency increases the division ratio following the coarse loop by a proportional amount, therefore phase noise contributions from the coarse loop will be independent of output frequency.

4.8.4.2 Transfer loop

The required tuning range of the transfer loop is in inverse proportion to the output frequency as mentioned in §4.7.7 of this chapter. From equation (5.46) of chapter 5 it can be seen that the phase noise power at the output is inversely proportional to the phase detector frequency. Therefore, this source of phase noise should increase by 3dB for every doubling of output frequency.

4.8.4.3 VCXO

The VCXO phase noise increases at 6dB for every doubling of output frequency.

4.8.4.4 SRD comb generator phase noise

Phase noise contributions from the comb generator in the N/M synthesiser will be identical to that of the VHF synthesiser case and will increase by 6dB for every doubling of output frequency.

4.8.4.5 YIG N/M microwave synthesiser phase noise

The projected phase noise levels from the YIG synthesiser configuration is given in fig4.36 for a 10GHz synthesiser configuration and fig4.37 for a 20GHz synthesiser. The YIG synthesiser configuration is capable of the best phase noise performance at the higher output frequencies. All this is achieved without even considering the superior phase noise performance of a YIG oscillator. When YIG oscillator performance is considered, the phase noise advantage becomes even greater. This advantage comes about because the tuning range of the VHF transfer loop is reduced over that of the VHF synthesiser PLO arrangement. Transfer loop tuning range reduces further as the output frequency is increased. Such a reduced tuning range means that a higher division ratio is possible after the coarse loop. The advantage of the intended implementation suggested here compared with other possible implementations is that translation from this chip to the final output frequency is output frequency independent. Most other configurations degrade the phase noise by $20\log N$. Therefore the phase noise is independent of output frequency. This is especially convenient for satellite communications work where phase

noise specifications are in general carrier frequency independent. Degradation by 20log$N$ still applies to the 100MHz signal, however. An interesting development of this is to replace the coarse loop with a DDS.

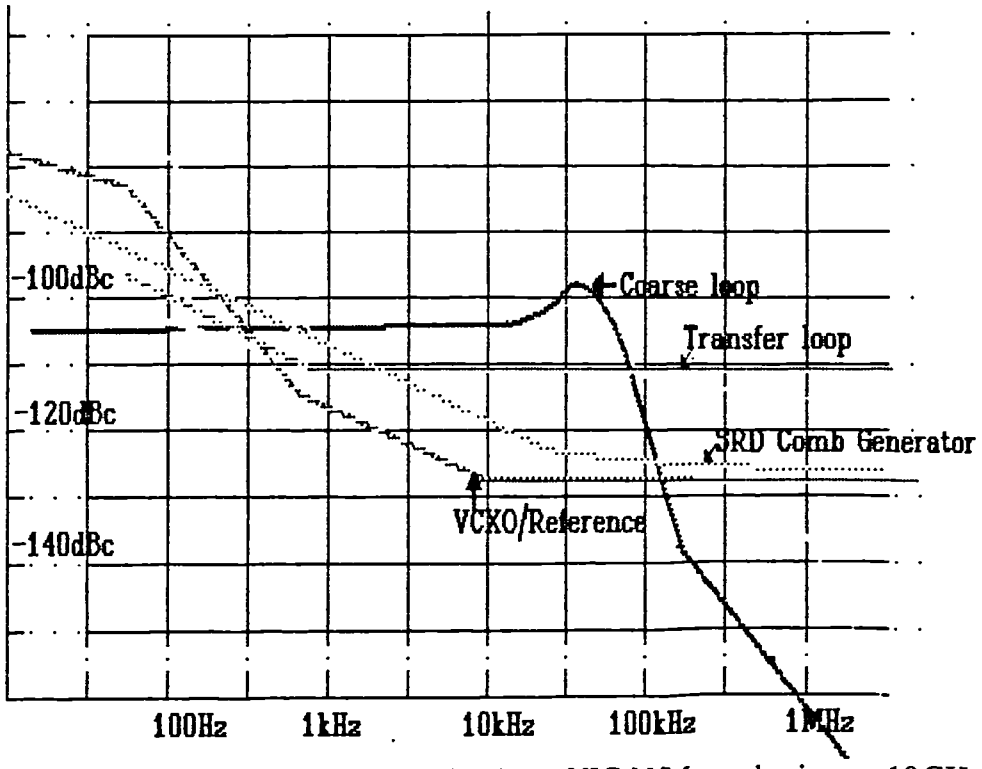


Fig 4.36 Phase noise contributions, YIG N/M synthesiser at 10GHz

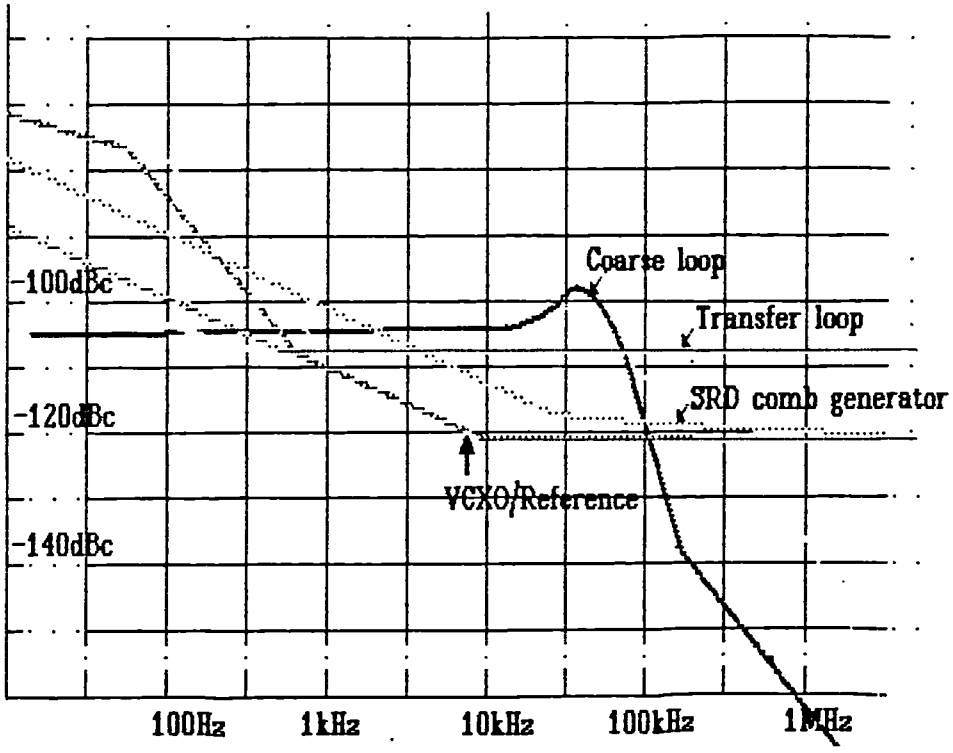


Fig 4.37 Phase noise contributions, YIG N/M synthesiser at 20GHz

4.8.5 YIG M/N synthesiser with DDS

4.8.5.1 DDS

Replacing the coarse loop with a DDS enables the low phase noise of a DDS to be exploited. If the spurious reduction technique of chapter 8 is implemented, a phase noise of -120 dBc/Hz could be expected from a DDS synthesiser with a 300 MHz clock rate. This translates to a phase noise of -114 dBc/Hz at the final output frequency at microwave. The phase noise of the other components apart from the VCXO will be identical to that of the synthesiser discussed in the previous section.

4.8.5.2 VCXO

Using the DDS enables the use of one fixed frequency VHF reference crystal. Therefore a very low phase noise SC cut crystal could be employed to give excellent close to carrier phase noise levels. SC crystals are more expensive, but the phase noise has been measured [personal communication, Cains,T, 1991] at -130 dBc/Hz at a 100 Hz offset on a 100 MHz carrier frequency for an oscillator circuit.

4.8.5.3 YIG N/M synthesiser with DDS, phase noise overall

Lowest phase noise figures of all the projected synthesiser arrangements surveyed are available from the N/M synthesiser with DDS. Fig 4.38 displays the phase noise contributions to the output of a 10 GHz N/M and DDS hybrid synthesiser and fig 4.39 a 20 GHz synthesiser.

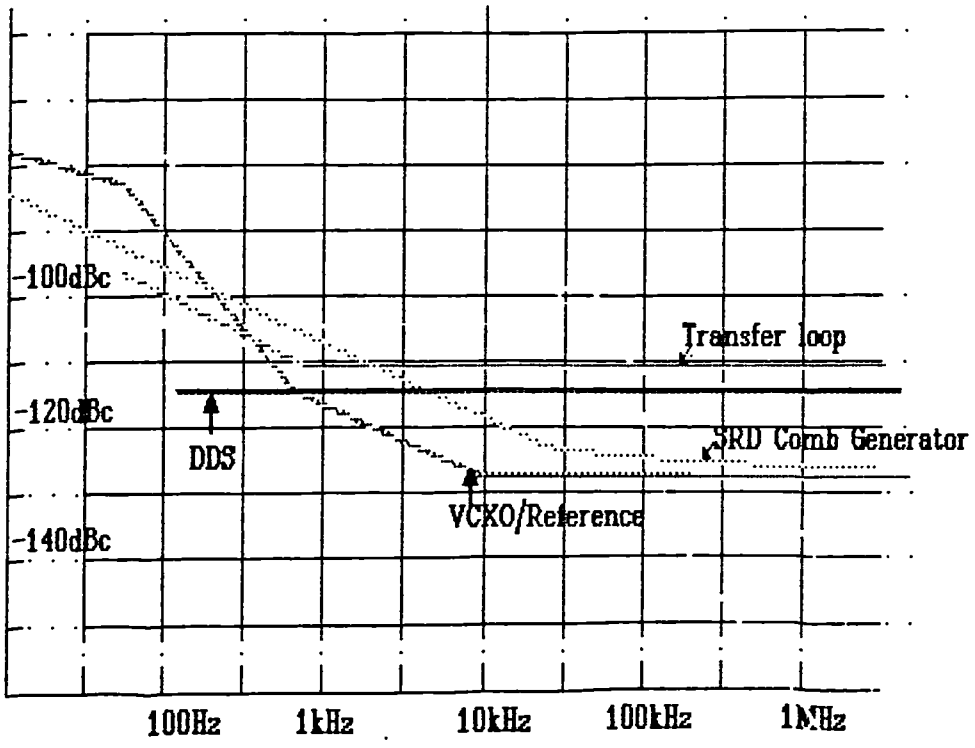


Fig 4.38 Phase noise contributions, YIG N/M synthesiser with DDS at 10 GHz

A phase noise contribution of less than 110dBc/Hz is given from the DDS section, and therefore with an improved transfer loop, this figure could be obtainable at the synthesiser output for offset frequencies of greater than 3kHz. This synthesiser would be capable of being modulated at relatively low modulation rates of a few kBits/sec. For higher modulation rates of 100s of kBits/sec, a microwave VCO would be required at the synthesiser output, but the far from carrier phase noise would suffer.

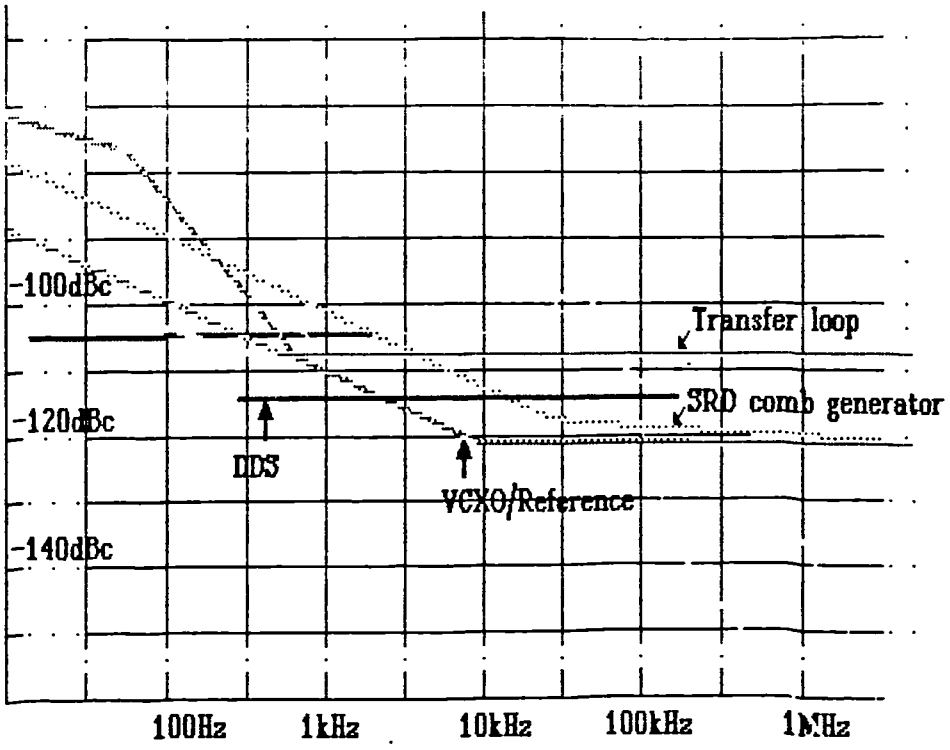


Fig 4.39 Phase noise contributions, YIG N/M synthesiser with DDS at 20GHz

4.9 Conclusions

In chapter 4 a synthesiser survey has been undertaken, initially looking at synthesis methods and finally discussing microwave synthesiser implementations.

Multiplicative synthesis schemes such as the N divide phase locked loop have the fundamental drawback of a high multiplication ratio, resulting in high phase noise and a limit to the minimum step size capability. Although this can be overcome by a multistage downconverter, designing for a small step size places critical demands on the downconverter filtering.

More care has to be taken with the design of fractional and combinational synthesisers because of the potential for spurious outputs that can occur as close to the wanted carrier as a single channel spacing. This unwanted output would be too close to carrier to be removed by filtering such as with a phase locked loop.

Multiple section iterative direct analogue and phase locked loop combinational schemes, although capable of excellent performance, have complicated RF circuitry, and have stringent multiple section screening requirements. For this reason the iterative techniques were rejected in the later parts of the chapter which deal with possible implementations of microwave synthesisers.

The fractional synthesis schemes of direct digital synthesis and fractional 'N' have simplified architectures, less demands upon screening, and arbitrarily fine frequency resolution. They are, however, susceptible to internal processing errors which can result in the generation of spurious frequencies. Some fractional 'N' techniques rely on a narrow phase locked loop bandwidth to remove the spurious responses from the output. This is undesirable in a digital data system as there would be vibration induced VCO phase noise present at the output. The fractional techniques have the advantage of having the capability of being directly phase and frequency modulated.

A table giving comparison between the techniques is difficult because of the many different aspects of synthesiser design, such as step size, phase noise, spurious requirements, switching speed and output frequency.

The performance and implementation of four possible architectures have been considered with a view to synthesising a microwave local oscillator. It now possible to conclude which combinations offer the greatest flexibility and yield the most efficient synthesiser in terms of phase noise against level of complexity.

The VHF synthesiser is the most complicated requiring 6 loops, a multitude of low phase noise reference crystals and a PLO at the output. If a cavity PLO is used, large amounts of power will be generated at L-band frequencies so there is a potential interference problem. Due to the phase noise demands on each loop, it is not possible for much integration of the loops. The only possible advantage of a VHF synthesiser is when the synthesiser must be remote mounted from the microwave local oscillators, as it is much easier to cable 100MHz than 10GHz. This advantage could however be gained from the other architectures by dividing the outputs down in frequency.

The L-Band synthesiser suffers from the disadvantage of requiring two microwave oscillators. In addition, the demands on the coarse loop in terms of phase noise performance is quite severe, and a multiple stage phase detection is required. Such an arrangement is complicated and does not allow much scope for integration. However only one fine loop is now required. This arrangement could, however be modified to include a DDS capable of being modulated at high data rates.

As a result of the synthesiser survey, it can be concluded that the YIG M/N synthesiser architecture, or its DDS variant is suitable for most satellite communication applications. With the M/N architecture, the VHF input to the YIG PLO has a very much reduced tuning range. This enables the coarse loop of the previously discussed architectures to be replaced with a single high quality crystal reference source. Therefore, this loop removes much of the complication of the previously discussed architectures. By allowing this high quality reference to tune over a small frequency range, it is possible to interpolate between the steps of the fine loop, and therefore have a much smaller step size than the previous architectures. The main disadvantage of this approach is the tuning speed: once a frequency step is made, it would take several seconds before the full specifications of the synthesiser would again be reached. In many applications where the frequencies are changed infrequently this may not be important. If this is important, then the alternative implementation involving the DDS must be used.

With the DDS approach, tuning speed would be microseconds providing the tuning range is within the FM coil tuning range of the YIG oscillator, otherwise the tuning speeds of the main coil must be taken into account, and the tuning speed would then be milliseconds. This is an unavoidable restriction imposed by the YIG oscillator. This effect would not be important if the DDS is used for low data rate modulation or tracking purposes. Careful design procedures must be followed if the DDS approach is used to avoid problems with spurious signals. The two key areas are the DDS generated spurious, and the *M* loop multiplier response, both of which will be covered in later sections.

The DDS would result in about 10dB reduction of phase noise to about -115 dBc/Hz. The spurious performance would be equal. With a DDS the tuning would be virtually continuous with a step size of less than 1 Hz at the output frequency.

4.10 References

Analogue Devices 1984 Integral non-linearity and differential non linearity. *Integrated circuits data book.* Vol 1 pp. 9-23.

Avantek 1990 data sheet for IFD50010.

Benn, H.P & Jones, W.J 1989 A fast hopping frequency synthesiser, *IEE conference on Frequency Control and Synthesis, Leicester.* p. 70.

Bjerede, B. & Fisher, G. May 1976 A new phase accumulator approach to Frequency Synthesis. *Proc IEEE NAECON.76.* p. 928.

Brewerton, D. & Urbaneta, N. June 1984 Synthesiser primer, defining the elements of good design. *Microwaves and RF.* p. 79.

Britten, P.D. & Martin, J.B. 1989 Frequency synthesisers for the Prodat Aeronautical Terminal. *IEE conference on Frequency Control and Synthesis, Leicester.*

Brown, D.A. 1989 New technique provides agile high spectral purity frequency synthesiser for future communications systems. *IEE conference on Frequency Control and Synthesis, Leicester.*

Browne, J. July 1988 All GaAs line-up fuels high speed Digital Synthesiser. *Microwaves and RF.*

Burr-Brown February 1988 Fulfilling the promise, a new high performance direct digital synthesiser design. *Data release.*

Driscoll, M.M. 1985 Low noise crystal oscillators using 50Ω modular amplifier sustaining stages. *40th Annual Frequency Symposium.* IEEE

Duck, D.R. & King, N.March 1983 Development of digital frequency synthesisers for H.F. Communications Receivers. *Proceedings IEE Conf on Land Mobile Radio, Leeds.*

Egan, W. 1981a *Frequency Synthesis by Phase Lock,* chap. 3, p. 29. Wiley.

Egan, W. 1981b *Frequency Synthesis by Phase Lock,* chap. 7, p. 168. Wiley.

Eutelsat 1989 Eutelsat II specification for Satellite data link equipment, *Document no Eut.PS.ASCA 0054/E110* Issue 5 p 35.

Feinberg, P. June 1986 Multiple synthesis techniques optimise instruments performance. *RF Design.*

Gillete, G.C. August 1969 Digiphase Principle. *Frequency Technology.*

Grande, V. September 1990 Use Permanant-Magnet Resonators to tune YIG oscillators. *Microwaves & RF.* pp. 162-173.

Grove, W.M 1966 A DC to 12.4GHz feedthrough sampler for oscilloscopes and other RF systems. *Hewlett Packard News.* p. 12.

Harris, M.V. 1989 An investigation into the frequency settling time and post tuning drift of broadband microwave varactor tuned oscillators. *IEE conference on frequency control and synthesis publication 303 Leicester.* p. 97.

Harrison, R.G. 1977 A broadband frequency divider using varactors. *IEEE Trans MTT25.* No 12. pp. 1055-1058.

Harrison, R.G. 1983 Theory of the varactor frequency halver. *IEEE Trans MTTs digest.* pp. 203-205.

Hassun, R. June 1984 The common denominators of Fractional N. *Microwaves and RF* p. 107.

Hewlett Packard 1978 Synthesiser NO 3335A, Instruction Manual. pp. 816-836.

Josefsberg, K. May 1991 Efficient comb generator sampler locks DRO to 100MHz input. *Microwave Journal.* p. 304.

King, N. 1978 UK Patent gb2026268 Frequency Synthesis.

Law, W.R. 1985 Towards a YIG tuned phase locked source. *Ferranti Computer Systems Technical Memorandum.* no 86-05/02.

Manassewitsch, V. 1985a *Frequency synthesisers, theory and design.* chap. 4, p. 226. Wiley.

Manassewitsch, V. 1985b *Frequency synthesisers, theory and design.* chap. 1, p. 16. Wiley.

Matteson, E. & Coyle, L. 1988 Phase Noise in Direct Digital Synthesisers. *42 Annual Frequency Control Symposium.* p 352.

McCune, E.W. Jr 1988 Control of Spurious Signals in Direct Digital Synthesis. *R.F Expo proceedings.* p. 523.

Meyer, D.G. 1970 An ultra low noise direct frequency synthesiser. *Proceedings of the 24th annual frequency control symposium.* p. 223.

Nicholas, H.T & Samuli, H 1987 An analysis of the output spectrum of Direct Digital Frequency Synthesis in the presence of Phase Accumulator Truncation. *Proceedings of the 41st Annual Frequency control Symporium. pp.* 495-502.

Osbrink, N.K. & Grande, V Sept 1989 Yig sources target 8GHz commercial use. *Microwaves & RF.* pp. 141-148.

Qualcomm 1991 Preliminary application note: Q3036 phase locked loop PLL frequency synthesiser phase noise measurements. p 2 Qualcomm San Diego.

Racal 1983 Synthesisers for communications receivers. *Racal Communications Ltd Bracknell, Internal report.*

Reinhardt, V.*et al.* 1986 A short survey of frequency synthesiser techniques. *40th Annual Frequency Control Symposium.* p. 355.IEEE

Rodhe, U 1983b ibid. chap. 4, p. 276.

Rohde, U. 1983a *Digital PLL Frequency Synthesisers, Theory and Design,* chap. 1, p.1 Prentice Hall.

Rohde, U. 1983b *Digital PLL Frequency Synthesisers, Theory and Design,* chap. 4, p. 276. Prentice Hall.

Rohde, U. 1983c *Digital PLL Frequency Synthesisers, Theory and Design,* chap. 5, p. 314. Prentice Hall.

Saul, P.H & Taylor, D.G. 1989b A 2GHz Clock Direct Frequency Synthesiser. *IEE conference on Frequency Control and Synthesis Leicester.*

Saul, P.H. & Taylor, D.G. 1989a A High Speed Direct Frequency Synthesiser. *Plessey Research Review.* p. 63.

Stirling, R. 1987a *Microwave Frequency Synthesizers,* chap. 9, p. 88. Prentice-Hall.

Stirling, R. 1987d ibid. chap. 16, p. 150.

Stirling, R.C. 1987b *Microwave Frequency Synthesizers.* chap. 2, p. 15.

Thrower, K. 7th April 1977 Techniques for frequency synthesis. *IERE International conference on frequency control and synthesis. University of Surrey, Guildford.*

Underhill, Prof. M.J. 1986 Frequency synthesers and standards. In *Radio Receivers.* (ed. Gosling), Chap. 4. p. 123. Peter Peregrinus.

Vella, P. May 1991. Novel synthesiser cuts size, weight, and noise levels. *Microwaves and RF.* pp. 231-236.

Wheatley, C.E. & Phillips, D.E. May 1981 Spurious Suppression in Direct Digital Synthesisers. *Proceedings of the IEEE35th annual Frequency control symposium, Philadelphia.*

Wheatley, C.E. 18 October 1983 Digital frequency synthesiser with random jittering for reduced discreet spectral spurs. *United States patent 4,410,954.*

Williams, F. May 1987 Direct numerical synthesis of sine waves. *RF design.* p. 30.

Wilson, M.P. 9th May 1988 Low cost synthesised sources for VSAT frequency converter applications. *IEE Colloquium on Microwave components in telecommunications, London.*

Znojkiewicz, M.E. & Vassilakis, B. 1987 Phase transients in Digital Radio Local Oscillators. *IEE MTT-S Digest.* p. 475.

Zverev, 1967 *A Handbook of filter synthesis.* p. 323 Wiley NY.

5 Synthesiser component design considerations

5.1 Introduction

This section describes research undertaken by the author into the effect of the components of a synthesiser upon the output excess phase noise and spurious signals, that is the noise present at the output over and above the theoretical $20\log N$ [Grebenkemper, 1982] multiple of the reference phase noise. Details of specific phase noise performance of synthesiser circuitry in obtainable literature are sparse and there is ample scope for investigative work here.

The components to be discussed in this section are frequency dividers, multipliers, and limiters. The other major synthesiser components, oscillators, have already been covered in chapters 1 to 3 and appear frequently in published literature. However it is difficult to predict the performance of a synthesiser simply from oscillator specifications alone. By investigating the performance of dividers, multipliers and limiters all the major components within a synthesiser can be quantified, and the most economical synthesiser configuration may be derived.

An important aspect of synthesiser design is electromagnetic interference (EMI). Signals generated in one part of a synthesiser may couple into another area and give unwanted spurious signals by interference effects. An interference emitter is a source of interference to surrounding circuitry, and a susceptor is a circuit sensitive to EMI. One of the major problems of synthesiser design lies in separating the above two. Two of the most problematic circuits in synthesiser design as regards EMI are multipliers and dividers. It is suggested that multipliers can be broadband emitters and dividers, broadband susceptors. An area not often considered, but investigated in this section is the effect of limiters on broadband noise and as an interference susceptor. This is followed by a

consideration of the effect of broadband noise and signals on phase noise in logic circuits. Another EMI problem not always appreciated is the susceptibility of low Q oscillators to external signals close to their free running frequency.

Frequency multiplication of some form is necessary to transfer the low close to carrier phase noise performance of a crystal oscillator to microwave frequencies. There is a phase noise degradation of at least $20\log N$ for a frequency multiplication factor N. A substantial proportion of this chapter will therefore be devoted to a study of frequency multipliers for which many configurations are possible. The effect of various multiplier circuits upon output phase noise is to be considered with the aim of producing guidelines for correct selection.

One possible implementation of a frequency multiplier is the divide by N phase locked loop (PLL). Although the divide by N phase locked loop is simple to implement and align, it brings certain drawbacks. Many phase detectors used with this kind of loop sufferer from severe non-linearity, and this effect is studied along with possible remedial action. Another problem is the phase noise introduced by digital devices. Different phase detector configurations are compared for phase noise, linearity and reference spurious feedthrough. Phase noise introduced by a phase locked loop configured as a multiplier using a variety of phase detectors is compared with the phase noise of non PLL multipliers. The comb generator sampling loop is discussed as a possible compromise between the simplicity of alignment of the phase locked loop multiplier and the phase noise level performance of the non phase locked loop multiplier. During the investigation of phase detectors a new type of phase detector was invented, the image rejection phase detector. This type of phase detector is described together with its use in a transfer loop in multiple loop synthesisers.

Many authors apply the $20\log N$ rule to dividers, in reverse to that applied to multipliers; however, a subtle flaw lies with this approach in that it does not take full account of broadband effects. Here broadband effects will be analysed by a method based on consideration of the switching action in a perfect limiter. This switching action can fold up the spectrum over a broad range to around the carrier; such a switching action can occur at the input stages of digital circuitry within a divider, and this can result in higher than expected phase noise and spurious signals at the output of the dividers. Limiter theory is then developed to attempt a prediction of divider and phase detector phase noise when used within a PLL synthesiser.

PLL design is further investigated by means of a computer simulation written by the author. This simulation is applied to problems related to injection locking and vibration in

phase locked loop synthesisers. Modifications to PLL designs which would improve rejection of vibration are examined.

Finally, a method of overcoming the $20\log N$ rule is suggested that uses non-coherent frequency multiplication is discussed.

5.2 Noise sources within synthesisers

5.2.1 Introduction

Synthesised sources generate both discrete spurious and random noise modulation. The latter is traditionally referred to as phase noise. The noise can be both inherent in the synthesiser circuits and induced by external vibrations (microphony). Both processes can degrade the BER performance of a data link as shown in chapter 6. From BER measurements taken on a satellite data receiver subject to shock such as is discussed in chapter 9 it can also be concluded that vibration is a particular problem. This topic is covered in §5.8.

5.2.2 Discrete spurious

Sources of discreet spurious signals are:-

1. Mains related products;
2. External signals, ie EMI susceptibility;
3. Reference feedthrough;
4. Unwanted spurious mixing components.

Mains hum and EMI susceptibility (1 & 2) refer to sources external to the synthesiser unit. The first step towards reduction of these is to investigate the means of coupling of the interference. Power supplies are a particular problem. Switched mode power supplies generate very large amplitude signals with a large harmonic content. Furthermore the frequency changes with loading and as the power supply oscillator is allowed to free-run, the frequency becomes a function of the regulation mechanism. If a switched mode power supply is to be used in the system then particular attention must be paid to filtering and RF coupling. With linear power supplies the dominant means of coupling are magnetic and acoustic. Since the spectrum is concentrated at low frequencies this form of power supply is usually less troublesome than the switched mode which produces a broad spectrum of

interference. Due to the switching action of the latter, harmonics of the switching frequency can be present up to hundreds of MHz. Therefore broadband filtering must be present for several modes of propagation, for example, electromagnetic radiation, transmission along power supply lines, mutual coupling through the ground circuitry, and coupling into signal cables whenever switch mode power supplies are used.

Numbers 3 and 4 of the above listed discrete spurious sources are inherent in the synthesiser processing circuitry. Sources of spurious products are well documented in the literature for direct and indirect analogue synthesisers [Manassewitsch, 1985a],[,Rohde, 1983a]. The important difference between reference related spurious and mixing products is that the former can normally be removed by filtering, whereas the latter can move across the output signal spectrum and be as close to the output as one output channel spacing. Reference related spurious signals are normally associated with multiplier synthesis, where all output frequencies are a product of the reference frequency only.

In fractional synthesis unwanted mixing products are present alongside reference spurious signals due to the necessity of including some form of frequency conversion within the loop. This effect can be demonstrated by consideration of the spurious generation equations for a mixer [Bain, 1989]. Applying a similar analysis as in §4.4.7 results in the presence of spurious products at offset frequencies of c channels away where c is the highest common factor of the inputs to the mixer.

5.2.3 Reference spurious

Reference spurious signals arise due to feedthrough of the reference frequency to the RF spectrum around the carrier, so that sidebands appear at the reference frequency and at its harmonics.

In the frequency multiplier, the reference frequency feedthrough is determined by the out of band rejection of the output filter. Consequently the problems associated with unwanted sideband rejection increase with increasing multiplication ratio. This is because the nearest reference sideband becomes a smaller fraction of the output frequency and therefore filters of a smaller percentage bandwidth must be used. However multipliers can provide excellent adjacent channel suppression at low multiplication ratios due to high filter element Q's that are possible at microwave frequencies [Wong, 1988].

5.2.4 Phase locked loop reference rejection

Phase locked loops can be used to provide improved rejection of adjacent reference sidebands [Stirling, 1987]. The phase locked loop performs a low pass to bandpass

transform to phase modulation, so that the low pass characteristic of the phase locked loop H(s) is transformed to the bandpass characteristic by the low pass to bandpass transformation [Kuo, 1966]:-

$$H(s)_{bp} = \frac{\omega_o}{2\omega_c}\left(\frac{s}{\omega_o} + \frac{\omega_o}{s}\right) \qquad (5.1)$$

where ω_o is the carrier frequency and ω_c is the phase locked loop cut off frequency. The advantage of this is that the filtering can be done at baseband where it is generally more economical and where more effective filters can be realised. Consequently, in theory very large multiplication ratios can be accommodated, though in practice this is not recommended for the reasons described in §5.7.2.4 of this chapter.

In a phase locked loop, there is a natural rejection of spurious feedthrough above the loop bandwidth, of 20dB per octave ie. a single pole rejection. This can be increased by adding additional filtering on the VCO control line. A third order type two loop displays an increased reference frequency attenuation as against the second order type two loop [Jones, 1986]. The third order loop is formed by the use of a single pole VCO control line filter. However, there is a limit to the amount of filtering that can be applied within the loop, otherwise the transfer characteristic of the phase locked loop will have poles in the right half plane on the s diagram and the loop be unstable. Calculation of a phase budget at the unity loop gain frequency is the simplest way of avoiding this problem. This method is extensively covered in the literature eg. [Rohde, 1983b]. There is therefore a potential problem with reference feedthrough if the loop bandwidth is not small relative to the reference frequency.

One type of phase detector in common use is the analogue phase detector. The analogue phase detector of fig5.1 will typically have 30dB of reference frequency suppression [Watkins and Johnson, 1989] and no suppression of twice the reference frequency.

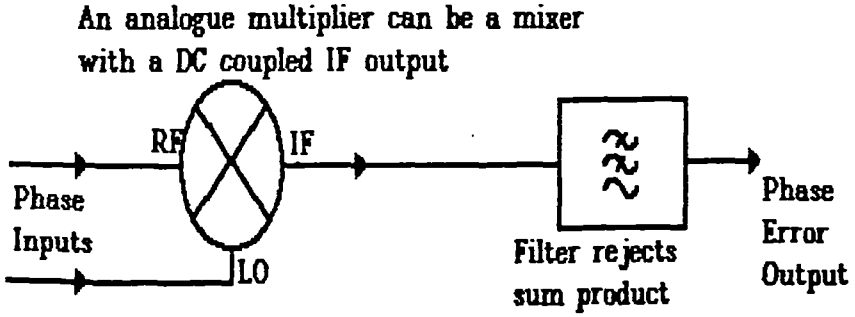


Fig 5.1 Using a mixer as an analogue phase detector

Some of the contributions to the overall noise performance from individual components within the synthesiser will now be discussed.

5.3 Effect of limiters and dividers in synthesisers

5.3.1 Significance of limiters in synthesisers

Limiters are critical elements in frequency synthesisers as they may contribute to the overall spurious and noise performance. Limiters are commonly used in frequency synthesisers to convert the analogue outputs from (for example) mixers, VCOs and filters to suitable inputs for driving digital dividers. Digital dividers as with limiters involve switching through an approximately linear transition region between the static levels. Effects akin to those occurring in limiters can therefore be shown to occur within digital devices themselves.

5.3.2 Noise considerations for limiters in synthesisers

Within most synthesisers there will be methods of conversion of sinewaves into squarewaves. This process may be considered to be perfect limiting. Most analyses of limiters' effects on the presence of sign for the presence of signals and noise relate to the main transmit-receive signal path and are therefore concerned with a bandlimited environment [Aein, 1973] [Davenport, 1953]. On the other hand, synthesiser work demands a noise analysis over a broad bandwidth. To this end attention must be focused on the noise generated by the active devices within the limiter alongside that present additive to the input signal. Since broadband noise will be indigenously present within the limiter, the process of phase noise generation within limiters must be treated as limiting a signal plus broadband noise, since there is no narrow band process within the limiter.

5.3.3 Measurement of noise effects within limiters

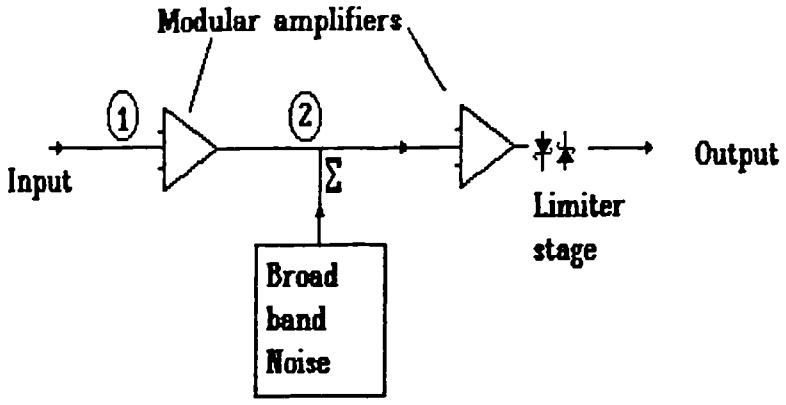


Fig 5.2 Block diagram of experimental limiter

An experiment was undertaken to investigate noise effects within limiters. A signal and broadband additive noise was applied to the 1st stage of a limiting amplifier (fig5.2) and an amplifier with a gain in the linear region of 45dB was used together with a Schottky diode limiter at the output. The amplitude of the signal was varied and the output signal was measured on a spectrum analyser. Care was taken to ensure that limiting occurred only at the output stage. The output signal to noise ratio was measured and plotted against the input drive power giving the plot shown in fig5.3.

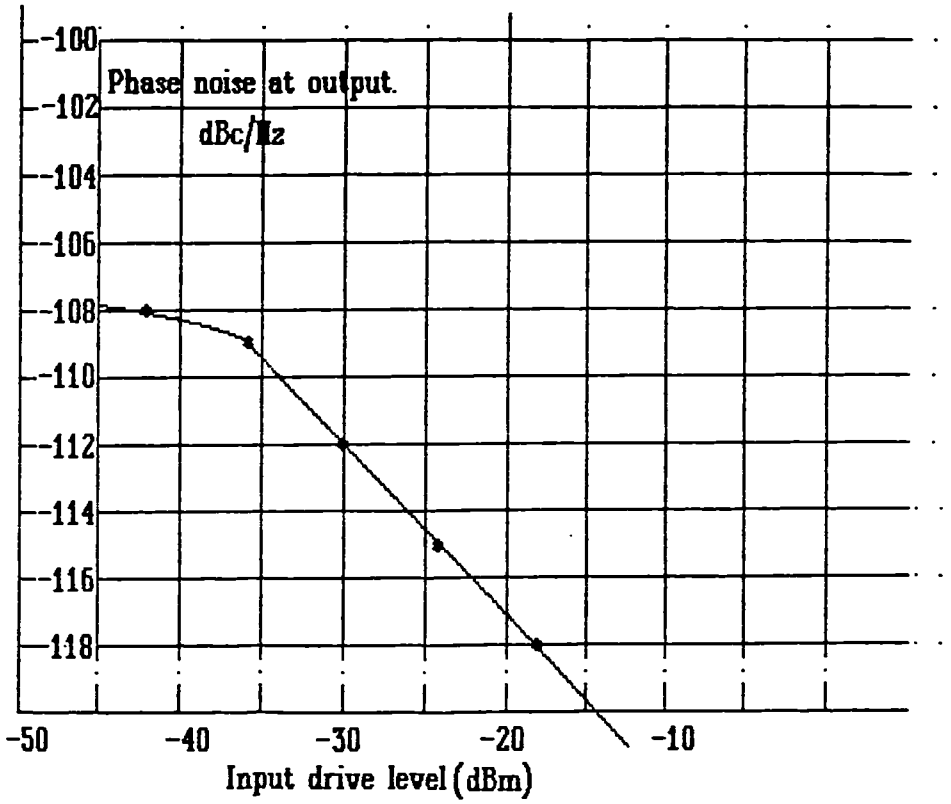


Fig 5.3 Measured phase noise of ideal limiter

It can be observed that for drive levels above a certain threshold, there is a 3dB improvement in output signal to noise ratio for every 6dB increase in drive level.
This indicates that the output signal to noise ratio varies in relation to the square root of the input drive level. The following section provides some explanation for this behaviour.

5.3.4 Conversion of additive noise to multiplicative noise in a limiter

By treating the limiter as a clipping amplifier a noise analysis can be performed. In an ideal limiter, there will be no AM to PM conversion of noise. Consequently, the response of the limiter to AM noise is not considered in this analysis.

Fig 5.4 shows a limiter in the time domain. The shaded line indicates the output of the amplifier if no limiting mechanism was present, and the large signal gain equalled the small signal gain. Amplifier gain will be represented by G in the linear region; limiting occurs at output voltage level $\pm V_L$; the input level is V_i and the angle at which the amplifier is in its linear region is β where (if $\beta \ll 1$ radian):-

$$\beta = \frac{2V_L}{G\,V_i} \tag{5.2}$$

The time t for which this transition occurs is:-

$$\tau = \frac{t_c V_L}{\pi G V_i} \tag{5.3}$$

The limiter is considered to have a signal at the input plus broadband additive noise. This noise is assumed to remain additive as it passes through the amplifier. At the output of the limiter, during the clipping part of the cycle, the noise is assumed not to contribute to the output; only during the active region is the noise assumed to be amplified. Therefore, the effective output noise at a frequency around the output fundamental frequency can be found from a convolution of the broadband noise function with a window function which is of value 1 during the transition period and 0 at other times. The window function can be represented as a sinc function in the frequency domain:-

$$W(\omega) \approx \sum_{n=-\infty}^{n=\infty} \frac{\tau\omega_c}{2\pi} \mathrm{sinc} \frac{m\tau\omega_c}{2} \tag{5.4}$$

where ω_c is the reference frequency, and m represents harmonics of the reference frequency. A result of this convolution operation would be carrier phase jitter in the form of random phase modulation, or phase noise.

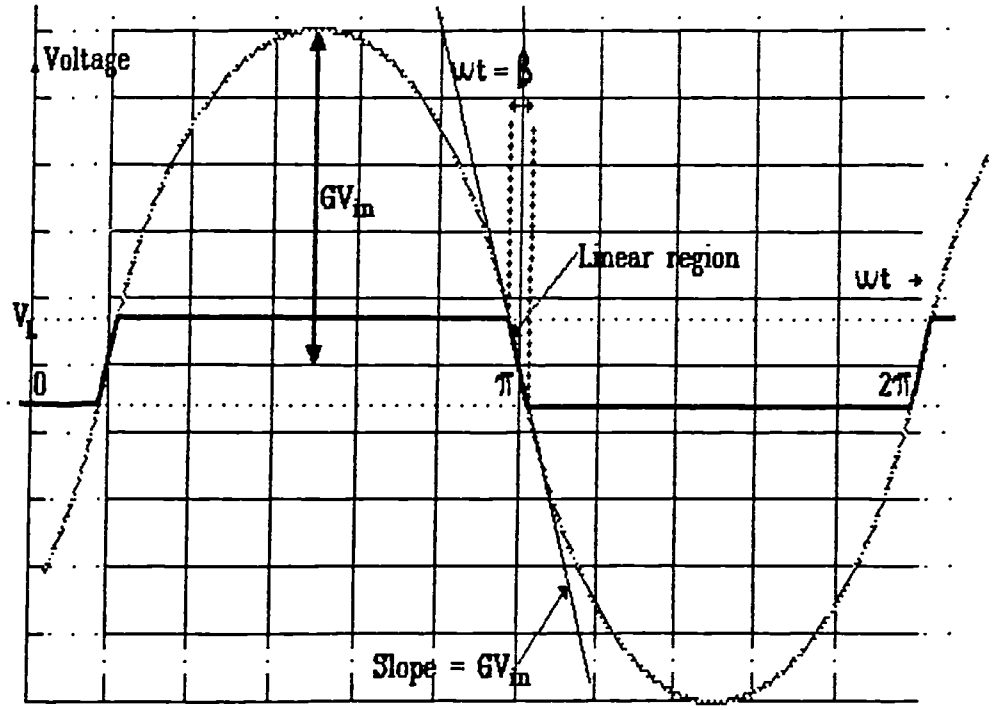


Fig 5.4 Time domain waveforms of a limiter

Owing to the narrow active window of the limiter phase noise can be introduced from noise at a very broad band of frequencies, extending up to frequencies of many multiples of the carrier rate. Performing convolution, as described above, results in the sampling and aliasing of the broadband noise to phase noise modulation on the carrier. This effect applies to offset from carrier frequencies of up to half the carrier frequency. Any periodic signals within the previously described broadband would be affected in a similar manner to phase noise. The convolution must therefore be applied to any periodic signals at the input to the limiter. Fig5.5 shows the effect of considering the transitions as a window function. At the output of the limiter, the noise output is represented by $N_o(f)$.
The result of considering amplification of the noise during the window period only is [Wilson & Tozer, 1989]:-

$$N_o(f) \approx \frac{N_o \tau \omega_c}{\pi} \qquad (5.5)$$

at the fundamental frequency ω_c. Limiter noise output, $N_o(f)$ is therefore a function of the additive noise level before the limiter (at point 2 in fig5.2), the limiter transition time, and the fundamental output frequency ω_c. This is as would be expected from a calculation of

the ratio of the noise power being transmitted to the output (window function = 1) to that being suppressed (window function = 0).

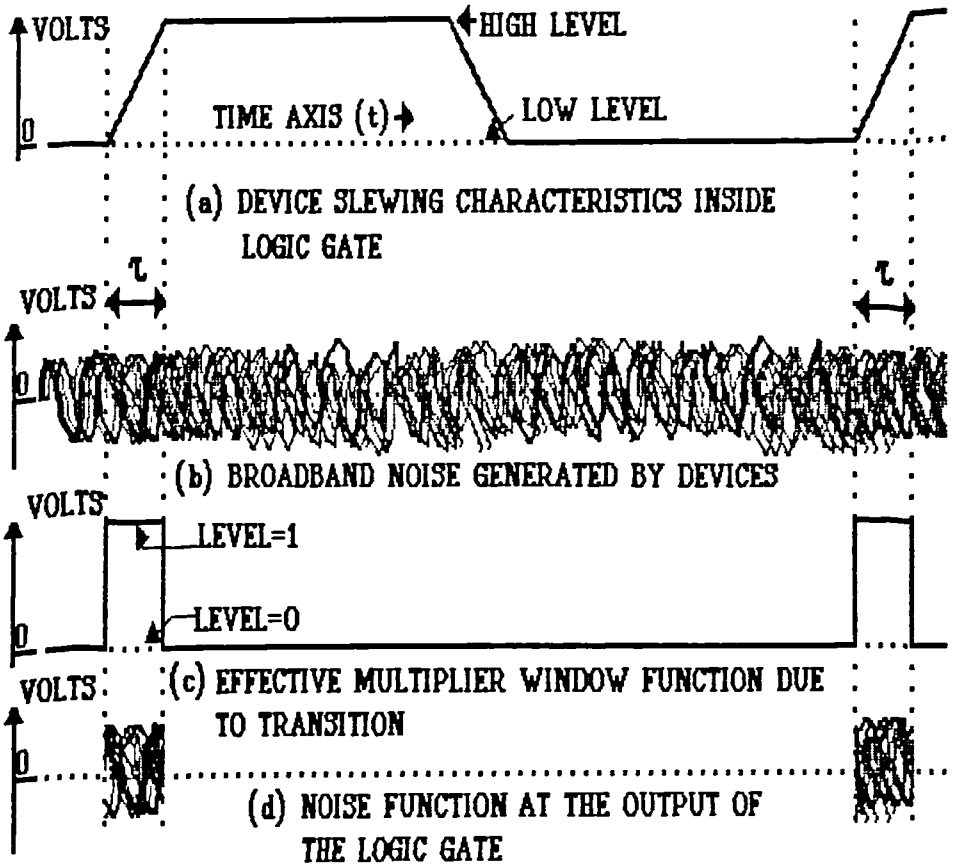


Fig 5.5 Contribution of device noise to limiters and logic device phase noise

Although a simple analysis based on the ratio of the transition time to the off time has been given [Wilson & Tozer, 1989], the convolutional approach would show that noise present at high frequencies (large value of N) appears at the carrier output frequencies. It follows that aliasing down from high frequencies has serious implications for synthesiser design in that noise peaks and spurious signals would be folded down around the carrier from far frequencies. The circuit would be sensitive to noise over a very broad band of frequencies and this must be taken into account in the design of the synthesiser.

For synthesiser design, it can be deduced from this section that the use of high gain, high speed low noise devices is essential for low phase noise at the limiter. Coupled with this, however it is essential that the stage is adequately screened and decoupled over a frequency range corresponding to the f_t of the devices. Using emitter degeneration would have serious implications for broadband white phase noise as effective device gain will be reduced, the devices will switch slower, and another noise sources is introduced into the circuit. Such degeneration may have an effect upon the $1/f$ noise of such a stage, but

futher study of this is beyond the scope of this thesis and can be recommended as an item of further work.

5.3.5 Frequency dividers

Frequency dividers are now available for use in synthesis at frequencies up to greater than 20 GHz. Three commonly used forms of dividers are digital devises, dynamic charge storage devices, and parametric devices. Digital devices are almost universally used at the lower frequencies (up to 5 GHz) and devices are presently being manufactured that can achieve 14 GHz. They are based on the flip flop and can therefore be considered as static in operation, that is as long as the pulse rise time is kept short, there is no lower frequency limit to the operation.

Dynamic devices are based upon a similar principle as dynamic RAM, that is charge storage in a MOSFET junction. Such devices use fewer transistors than the static variety and are capable of operating at frequencies of greater than 20 GHz. A major disadvantage of these devices is however, that, as they depend upon charge storage for their operation, there will be a minimum toggle frequency for correct operation.

Parametric devices rely upon a parametric amplifier made to oscillate at a subharmonic of the the input pump frequencies. Of all the divider types, these devices are capable of the highest frequency of operation, but they are the most difficult to align and manufacture.

This chapter will concentrate on digital dividers. These devices will therefore have two states at their input to the devices with a transition through those states as the digital elements change states. The resulting phase noise of the output will be a summation of all the contributions from the digital elements in the critical path between input and output.

5.3.6 Application of the limiter theory to digital dividers

The limiter theory described in the previous section (§5.3.4) can now be applied to digital dividers. A window area is created at the input of a divider whereby noise generated by the input devices during the transition is sampled. This leads to speculation that the phase noise power density at the output of the divider is proportional to the toggle frequency.

It is possible to consider the divider problem from another angle. If the noise addition at the divider transitions are considered to be events independent of other transitions, the total RMS time jitter in seconds must be independent of the divider toggling frequency. This means that the total RMS phase jitter is proportional to the toggle frequency. Total RMS phase jitter can be found from the phase noise density by integration in the

frequency domain. Phase noise originates mainly from the edge transitions in the case of clocked digital devices, and such transitions only occur in the same direction once per cycle. Since the phase noise is only active at discrete points in time, the problem resembles that of a sampled data system. Therefore the power spectrum will take the form:-

$$\mathcal{L}(\omega) = \mathcal{L}(0)\mathrm{sinc}^2\left(\omega T_p/2\right) \tag{5.6}$$

where T_p is the period of one reference cycle, $\mathcal{L}(0)$ is the phase noise asymptote at low frequencies, and $\mathcal{L}(\omega)$ is the frequency dependent phase noise power density.

By performing a power integration, the equivalent rectangular bandwidth of the phase noise can be shown to be $1/2T_p$. As described in §5.3.4 above, this noise may consist of noise aliased down from higher frequencies by sampling during the transitions. Therefore the total phase noise power will exist over a bandwidth of $1/T_p$, that is a range equivalent to the toggle frequency, at the output of a digital device.

Because the total RMS time jitter is constant the total RMS phase jitter power is increased by a squared relationship with frequency, but the integration area increases proportionally to frequency. Therefore, phase noise power density increases in a proportional relationship to frequency.

In practice, the divider problem is more complex than this, particularly since there is a tendency for oscillations to occur at high frequencies when the input stage is in its linear region [Apte & Cummings, 1990]. This means that oscillations will begin to build up if the transitions through the linear region are not rapid. Effects on noise performance would then be unpredictable. It is vital that the dividers are fed with transitions that are approximately equal to or faster than a reciprocal of the maximum toggle frequency of the divider. From the suggestions raised in §5.3.4 concerning the selection of limiters, the same criterion can be applied to dividers. ECL, although generally reckoned to be fast, consists of emitter coupled amplifiers switching between current limited states. Therefore the transition through the linear regions is relatively slow and the limiting amplitude is at a low level (typically 0.7 volts). With voltage limiting logic such as TTL and CMOS the logic is generally slower, but this is principally due to increased propagation delay during the limiting state rather than a slow transition region. This, coupled with the higher thresholds of voltage limiting logic indicates that ECL may not give the best phase noise performance. From the above criteria, indications are that FAST TTL should give the lowest phase noise. More on this subject will be given in §5.7 dealing with the phase noise of *+N* PLL synthesisers. However, the absence of saturated states may give ECL the edge in terms of phase detector linearity. This is further discussed in §5.7.2.3.

With dividers, the sampling and aliasing effects described earlier in this section have important EMI implications. Since signals can be aliased down from a broad range of frequencies, the device can act as a broadband susceptor. Aliased spectral components from frequencies close to a multiple of the divider output frequency can appear as close-to-carrier sidebands at the output frequency.

Dividers and limiters are often an integral part of a phase locked loop which is commonly used in synthesisers. Therefore PLLs will be considered next.

5.4 Phase Locked Loops

5.4.1 Introduction

Phase locked loops find extensive usage in frequency synthesis. A brief survey of the properties of various PLL implementations will now follow. The phase locked loop synthesiser can use the following phase detectors:-

a) Dual flip-flop phase frequency detector

b) Harmonic sampler

c) Analogue multiplier (mixer)

d) Ramp sampler (linear phase)

e) Image rejection phase detector

f) Single flip flop.

5.4.2 Phase Frequency Detector

5.4.2.1 Introduction

The phase frequency detector is the most common type of phase detector, and therefore is very well referenced [eg. Egan & Clark, 1978], [Connell, 1987]. A circuit diagram of a phase frequency detector is given in fig5.6. The phase output is not a level proportional to signal, but is in fact a pulse width modulated signal. One distinctive feature of this detector is that it is frequency sensitive. This is due to the fact that this detector is a state machine with the present state being dependent on previous states of the detector.

Assuming the detector starts with both outputs at zero, whichever output (pull up or pull down) goes high depends upon whichever input goes high first. Once an output goes high, it requires a transition on the opposite input to the phase detector to cancel this high level. Whichever input has the greater number of transitions will always be the one which can set the corresponding output. Such an output will be reset by the input with the lesser number of transitions. Such sensitivity to the relative number of transitions of each input gives the phase detector the property of frequency sensitivity.

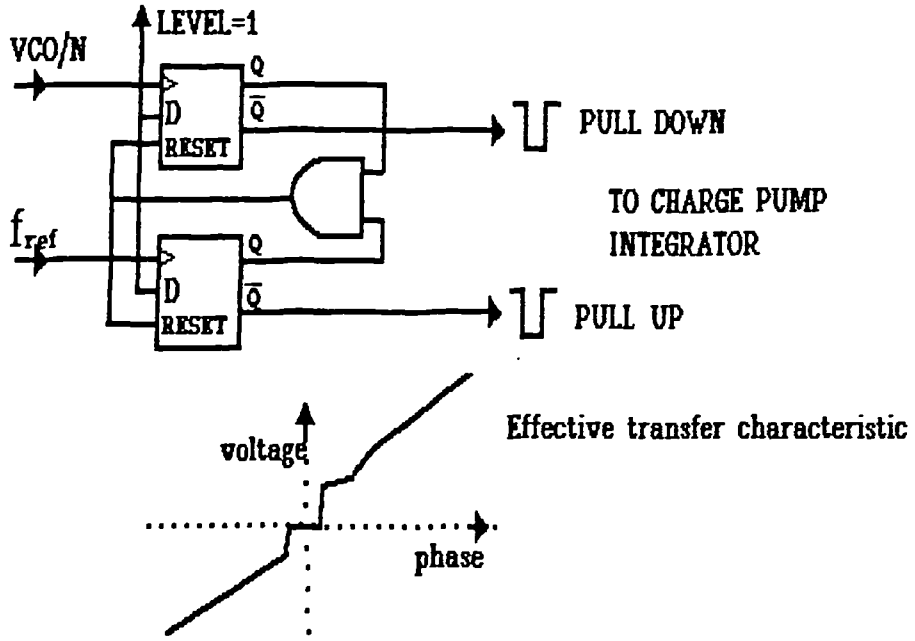


Fig 5.6 Phase Frequency Detector

5.4.2.2 Performance of the Phase Frequency Detector

There is much literature concerning the lack of linearity of this kind of phase detector [eg. Egan & Clark, 1978]. Although Fast TTL offers lower noise than other digital phase detectors, the non-linearity effects can be much worse [Connell, 1987]. One of the methods of overcoming this problem is to apply a fixed bias to the input of the integrator. The output of the phase detector must therefore be offset in order to cancel this bias. Phase detector operation is then biased away from the zero phase error region where most of the non-linearity exists. The disadvantages of applying bias are:-

1) The reference feedthrough from the phase detector is increased;

2) There is a possibility of introducing noise on the bias line.

Connell [*ibid*] discusses a method of measurement of non-linearity effects. The author was concerned because the quoted 1° phase resolution for the technique did not offer fine enough phase resolution to expose all the phase-gain variations. The 1kHz signal employed effectively averages out any phase-gain deviations within the range of this

sweep. An alternative scheme is therefore proposed here for measurement of non-linearity effects as shown in fig5.7.

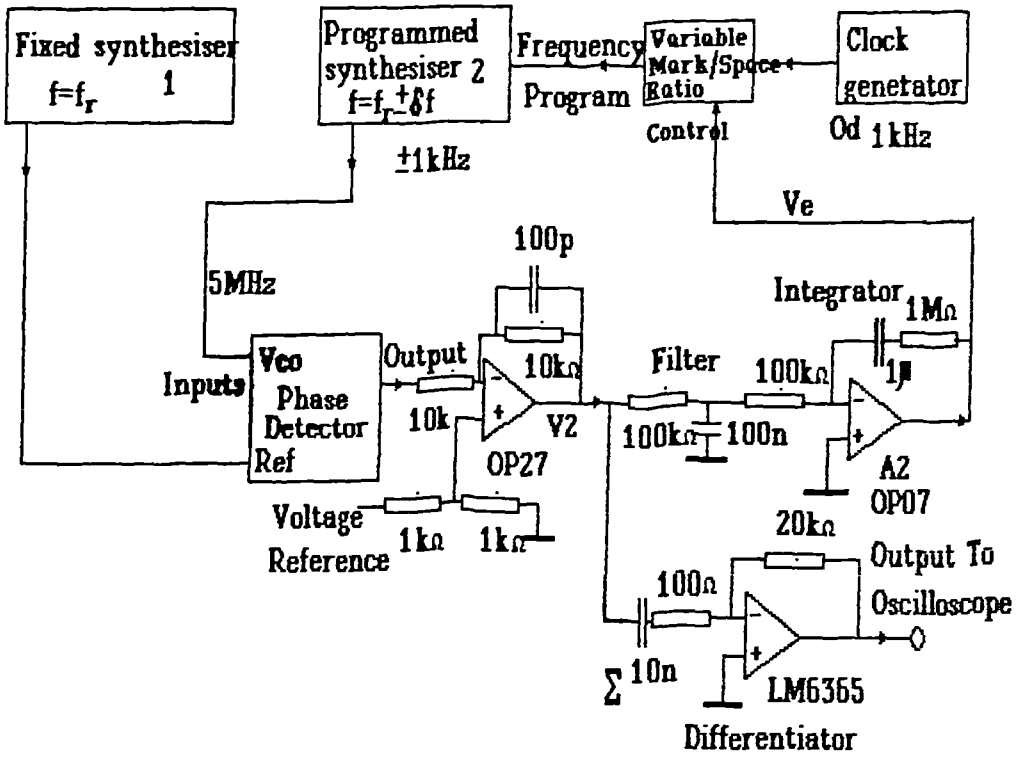


Fig 5.7 Linearity measurement of phase detector

The phase detector is connected to two synthesisers, both maintained at the same frequency. The phase of synthesiser 2 is swept relative to synthesiser 1 resulting in the presence of a swept voltage at the output of the phase detector. Dividing this voltage (after removal of any static offset) by the phase difference at the input to the phase detector gives the gain of the phase detector in volts per radian. The output of the phase detector feeds two circuits each performing a separate functions: phase locking and measurement. Phase locking is necessary to ensure that the phase detector is always swept about its central region. Any DC offset in the phase detector characteristic must be removed from the gain calculation, and this is achieved by obtaining the change in output over the change in input rather than measuring static values. A frequency step is equivalent to a phase ramp, so therefore synthesiser 2 has its frequency switched $\pm f_d$ about the nominal frequency to provide a phase ramp input to the phase detector and enable its transfer characteristics to be swept. In order to obtain zero mean phase error, the filtered phase error voltage V_e is fed to the mark-space ratio control of oscillator O_d. This is in effect a phase locked loop whereby the voltage V_e controls the mean frequency of synthesiser 2 by means of the mark-space ratio of O_d. Amplifier A2 forms the loop filter. The phase deviation ϕ_d is given by:-

$$\phi_d = \frac{\pi \delta f_r}{2 f_{ck}} \tag{5.7}$$

where ϕ_d is the maximum phase deviation at the detector, δf_r is the frequency offset at the synthesiser, and f_{ck} is the clock generator frequency. The resultant voltage V_2 is a ramp that traces out the phase characteristic of the phase detector. Changes in slope gradient are not as easily observed as changes in level, therefore it is preferable to have a plot of phase detector gain rather than the transfer characteristic (fig5.8). The ramp is converted to a gain value by the differentiator. Phase detector gain value, K_p, is determined by the slope of the phase plot:-

$$K_p = \frac{d\phi}{dt} \tag{5.8}$$

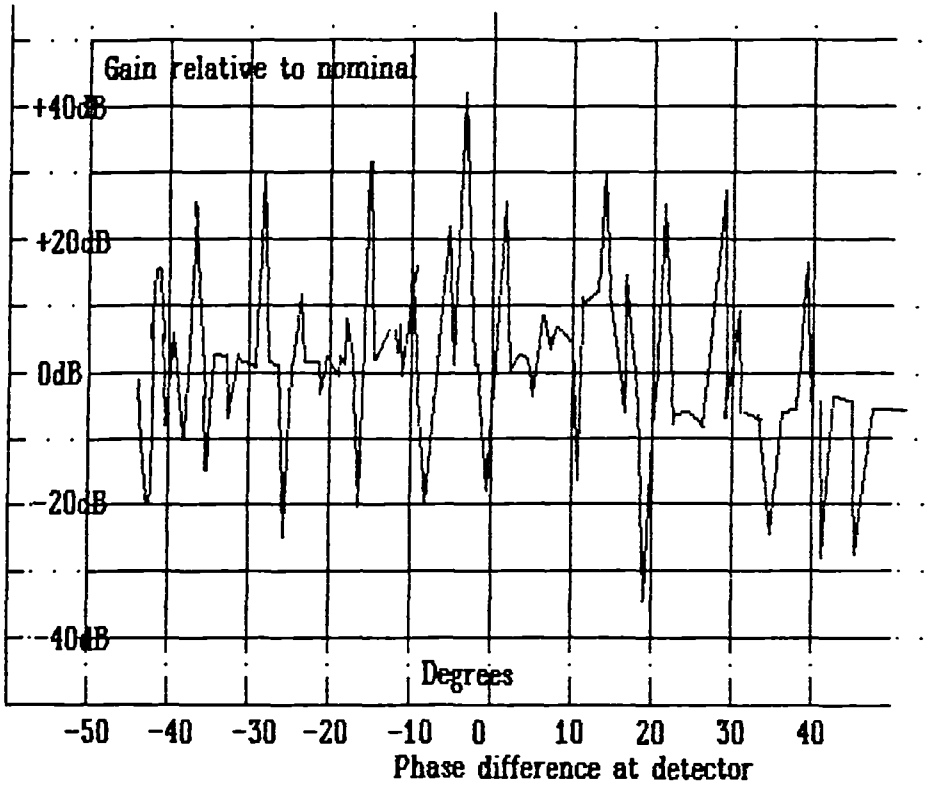


Fig 5.8 Gain of Fast TTL phase detector, unmodified version

The advantage of this measurement technique over that suggested by Utsi [1983] is that a fixed locked synthesiser can be employed rather than using the frequency modulation input which tends to lack stability by comparison. In order to examine the results published by Connell & Egan, the gain of the phase detector in fig5.9 with its output configured as in fig5.10 was measured at 5MHz; the resulting gain plot, (see fig 5.8) was then similar to that noted by Connell [1987], but the gain peaks were even higher (40 dB). Initially a charge pump type circuit was tested, but similar results were obtained

with the operational amplifier arrangement of fig5.10. This contradicts findings by Hatchett [1978] which suggest that the charge pump is the cause of the non-linearity problem.

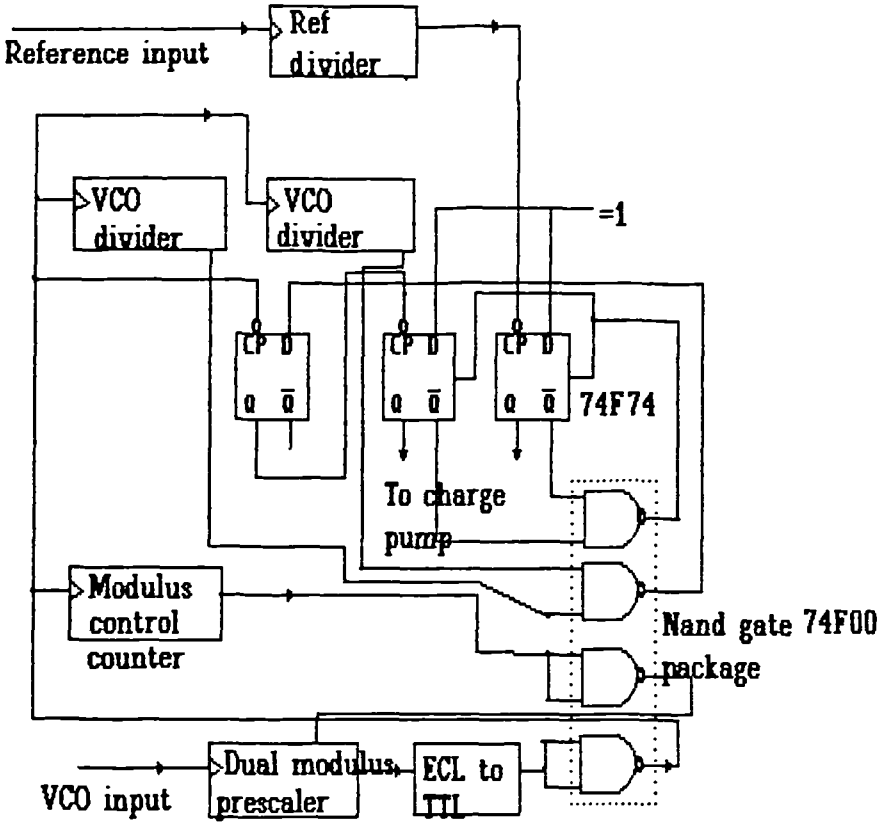


Fig 5.9 Arrangement of phase detector and dividers which gave poor linearity

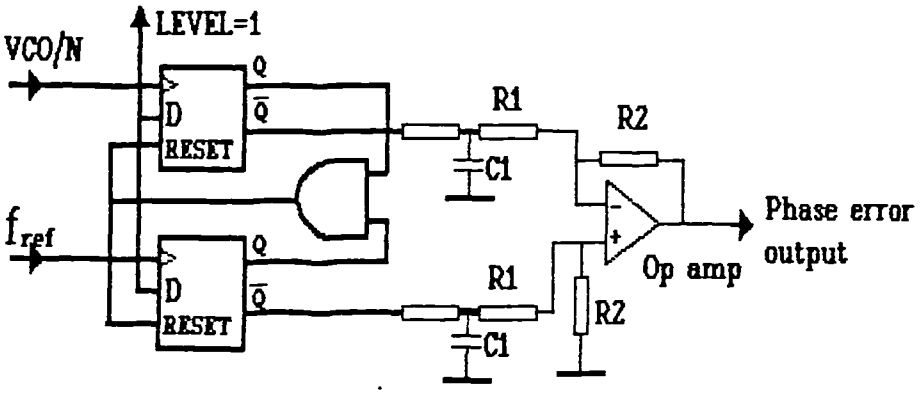


Fig 5.10 Phase Frequency Detector using linear amplifier

This suggests that the non-linearity problem may be internal to the device. Underhill [personal communication, 1989] suggests a "ratchet effect" internal to the device whereby ringing and other transient phenomena result in a variation of propagation delay according to various switching effects internal to the devices. The measured gain plot in fig5.8 described above would be unusable as the switching glitches would be spread throughout the phase detector characteristic and applying bias would therefore be ineffectual. It was

noticed that in fig 5.9, the Nand gate shares several functions including a high frequency clock buffer. The circuit was redesigned to only use one of the gates for switching applications, that is the feedback for the two flip-flops. Also, improvements to the layout resulted in direct connections between the flip flops and the Nand gates without crossing other signal lines. A gain plot resulting from the modification described above, measured by the author, is shown in fig 5.11. This is an improvement in the gain plot shown in fig 5.8 in that the large positive gain peaks have been eliminated leaving a single "deadband". A bias current applied to the phase detector enabled the production of reliable synthesiser designs.

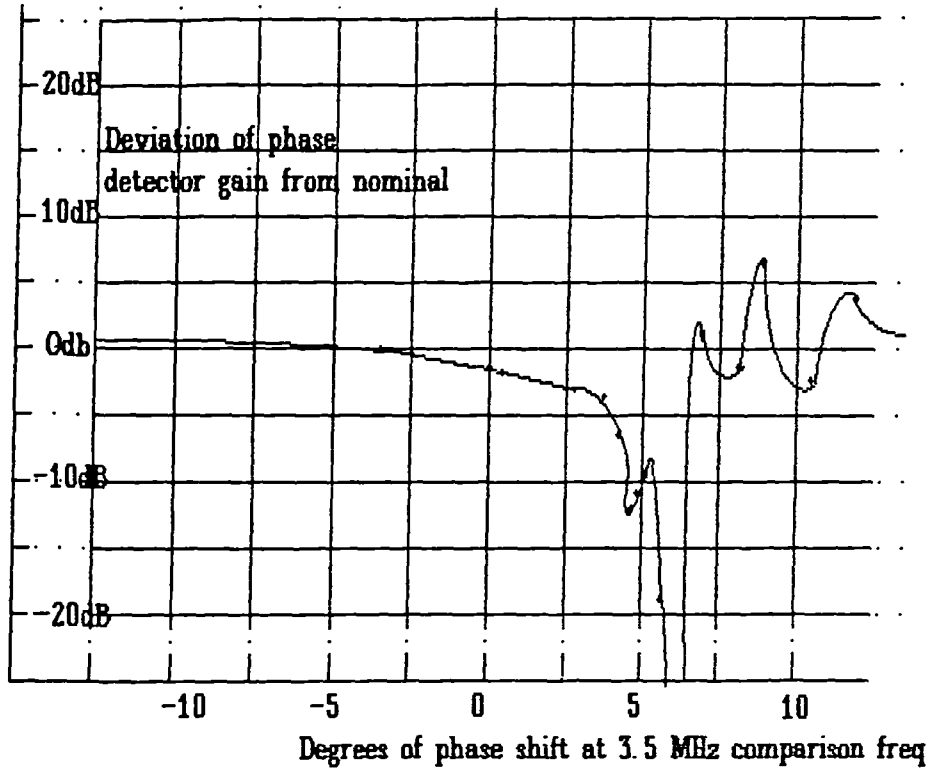


Fig 5.11 Gain characteristic of a modified Fast TTL Phase Detector

However, the use of a fixed bias introduced reference feedthrough that required heavy filtering on the VCO line to reduce the spurious signal. Excess phase shift in the VCO filter places a restriction on the maximum loop bandwidth value which is undesirable for fast settling loops. A possible solution to this problem [Rohde, 1983c] is the injection of the bias in the form of a pulse rather than a constant current. The pulse should ideally be placed so as to minimise interaction between the bias pulse and the phase detector operation. This method is displayed in fig 5.12. A suitable pulse is available in the form of an overflow output from the divide by *N* counters. Since both transients are confined to a small part of the phase detector duty cycle, the resulting phase modulation spectrum would be concentrated at higher frequencies and hence be easier to filter out. Unfortunately, however, such a pulse would also contribute jitter and therefore would degrade the phase noise floor of the detector. The use of a specially designed linear phase

detector may improve matters, however, but the phase noise of the device is still not defined.

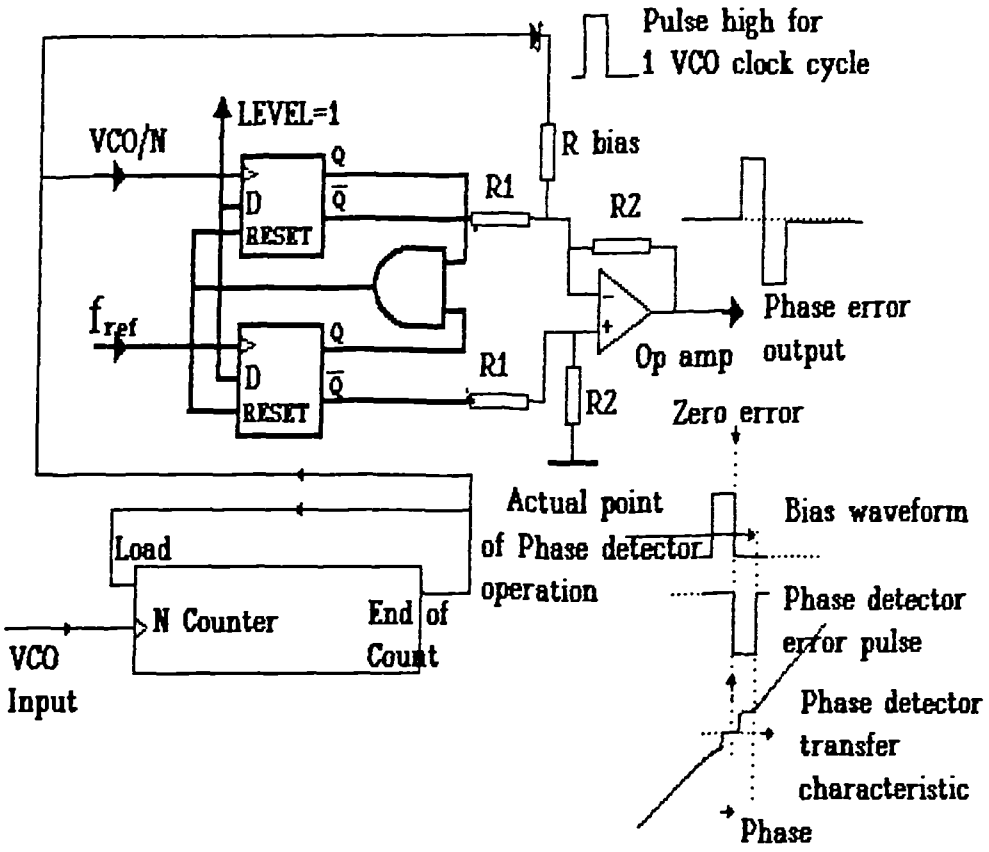


Fig 5.12 Applying pulse biased offset to linearise a Phase Frequency Detector

5.4.3 Harmonic sampling phase detector

5.4.3.1 Sampling loop

Fortunately there is a ready solution to the problem of reference feedthrough. A zero order data hold sampling at the reference frequency has infinite theoretical reference suppression at the reference frequency and its harmonics. The zero order data hold response is:-

$$K_p = \exp\left(\frac{-j\omega\tau}{2}\right)\mathrm{sinc}\left(\frac{\omega\tau}{2}\right) \tag{5.9}$$

This response has a zero at an ω value of $2/T$. The phase lag introduced by this filtering effect compares favourably with other loop filters. In addition, the effect of the sample and hold can be incorporated into a Z transform analysis of a phase locked loop to optimise settling times [Baker, 1989]. Usually the sample and hold function is incorporated into the phase detector itself. The most commonly used phase detector of this type is the 3 state dual flip flop phase frequency comparator of fig5.6. This is so called because of its ability to provide frequency acquisition as well as phase locking.

5.4.3.2 Microwave Sampling Phase Detector

The drawbacks of the phase frequency detector in terms of phase noise, reference feedthrough, bandwidth restriction and linearity prompted an investigation into other phase detection circuitry. Microwave sampling phase detectors are usually driven by a Step Recovery Diode (SRD) comb generator which when correctly designed may have the following advantages:-

1) Lower phase noise;

2) Complete freedom of choice of reference harmonic and multiplication ratio;

3) Operation at frequencies over 20GHz.

Step recovery diodes are further discussed in chapter 7. Microwave sampling phase detectors make use of the narrow impulse delivered by SRDs to turn on diodes arranged as a sampling gate. SRDs are also commonly used in frequency multipliers as in fig5.13.

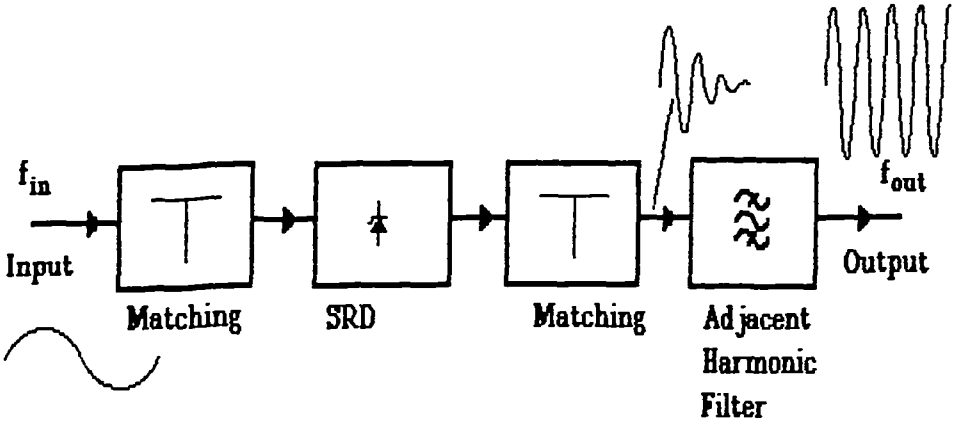


Fig 5.13 Fixed frequency step recovery diode multiplier

A problem with the frequency multiplier arrangement of fig5.13 is the rejection of adjacent reference sidebands with larger multiplication ratios, say >10. If, instead of using the SRD as a frequency multiplier, it is used to drive a sampling gate in a phase locked loop (PLL), the inherent rejection at the sampling frequency of the sample and hold can be used to reject reference sidebands. Additional rejection of reference sidebands is given by the PLL transfer function.

Another possible method of frequency multiplication is given in fig5.14. The PLL affords additional rejection of sidebands if the loop bandwidth is made narrower than the reference sideband frequency.

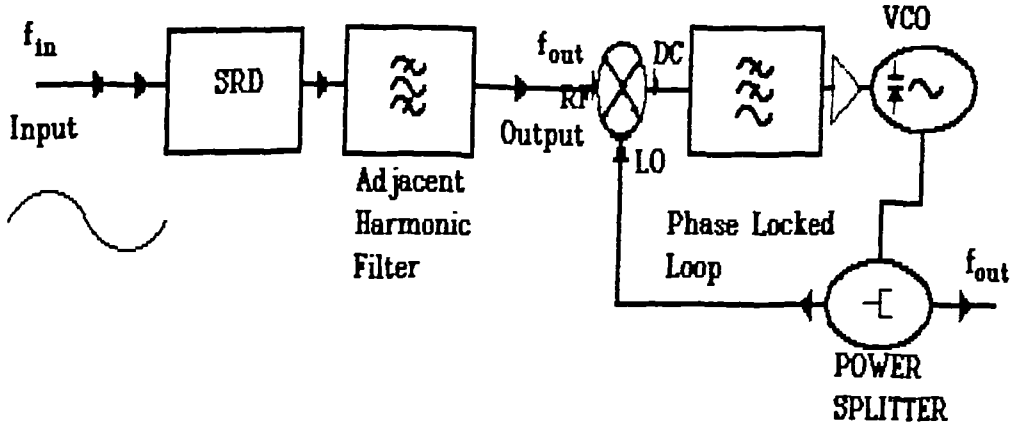


Fig 5.14 Fixed Frequency SRD Multiplier with PLL as sideband filter

An analogue mixer is used as a phase detector in this case. The problem with the multiplier PLL scheme is that flexibility is lost because the multiplier must be fixed tuned. Therefore one cannot change the multiplication ratio by an electrical means. One method of overcoming this problem would be to replace the multiplier with a YIG filter and comb generator as shown in fig 514. Additional amplification is required because of the low output of the comb generator at any single frequency; this combined with the bulkiness, expense and power consumption of the multistage YIG filter makes fig 514 a less attractive option for satellite communications work. If the filter is omitted and the comb generator fed directly into a mixer, the high peak amplitude of the comb generator output would overdrive the mixer.

The high speed sample and hold detector is the most desirable option for frequency multiplication in satellite communications applications. A block diagram of a sampling phase locked oscillator is displayed in fig 5.15. If the oscillator is a YIG tuned oscillator or a voltage controlled oscillator (VCO) then complete flexibility in the choice of multiplication ratio *M* is achieved. This facility can be used to simplify a microwave synthesiser as described in §4.8.4. The operation can be represented in signal processing terms as a mixer followed by a hold device; mixing results in the comb signal being multiplied with the VCO signal.

If the baseband component of the signal after analogue multiplication (mixing) were used to form the error to control the phase locking, its level would be too low to be effective. Therefore, a hold function is applied to the output of the multiplier. Applying a hold function enables a value of baseband signal to be held until the next reference pulse arrives.

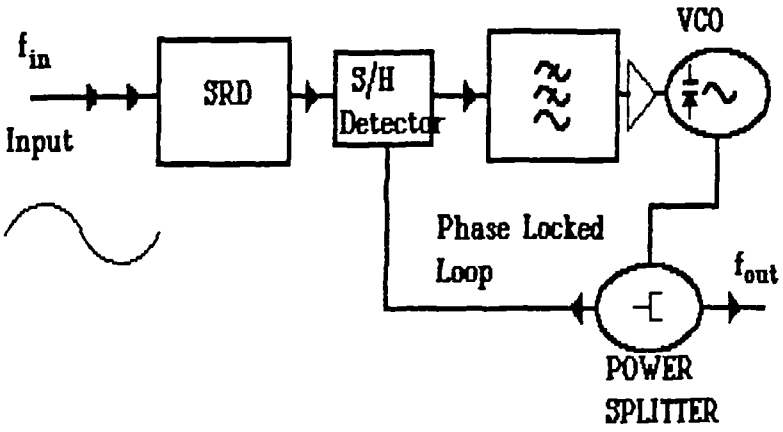


Fig 5.15 Broadband SRD sampling Phase Locked Oscillator

Fig 5.16 displays the function of the sample and hold detector in the time and frequency domains.

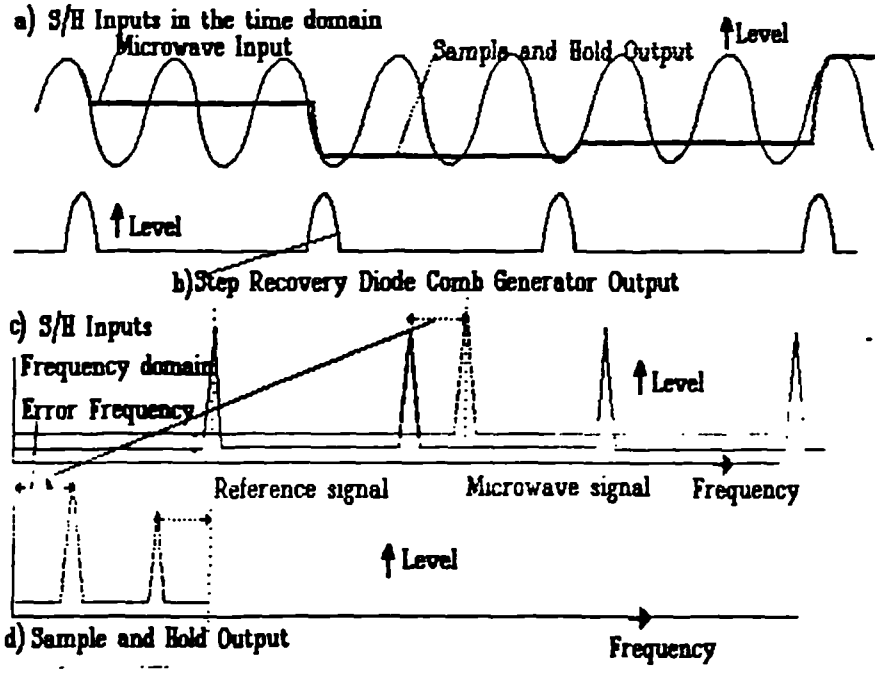


Fig 5.16 Operation of the Harmonic Sampling Detector in the time (a&b) and frequency (c&d) domains

The Laplace transform of the hold function in this detector is given [Egan, 1980] by:-

$$G(s) = \frac{1}{T_p s}\left(1-\exp\left(T_s s\right)\right) \tag{5.10}$$

where T_p is the duration of the on pulse and T_s is the sample period. Substituting $s = j\omega$ gives:-

$$G(s) = \frac{T_s}{T_p}\exp\left(\frac{-j\omega T_s}{2}\right)\mathrm{sinc}\left(\frac{\omega T_s}{2}\right) \tag{5.11}$$

This is the definitive equation for a hold device. The Fourier transform of an impulse is a comb of lines of amplitude T_p/T_s. Therefore the result of the above described multiplication is a reduction of amplitude by T_p/T_s. Following this by the hold function restores the overall gain back to unity.

The reference frequencies fall at the null points of the hold transfer function hence the theoretical attenuation of the reference is infinite. At the front of the equation the exponential factor corresponds to a phase shift of $\omega T_s/2$ in the detector of the transfer function. This phase shift must be taken account of in PLL dynamics calculations.

5.4.3.3 Increasing phase detector bandwidth

An extra pole must be added to the theoretical transfer function above due to the finite time taken to charge the hold capacitor during the sample period t_p, due in turn to finite response times of the sampling diodes and inductance in the sampling circuit. The circuit of the phase detector as used in many phase locked oscillators is displayed in fig5.17a. The circuit is self biasing in that it derives its own bias voltage through rectification in diode pair D2 and D3. A pulse is generated during the impulse period of the SRD and is coupled through by capacitors C1 and C2. These capacitors differentiate the waveform and provide sharp conduction pulses to D2 and D3. When the diodes conduct, D2 and D3 end of capacitors C1 and C2 are connected to the microwave input signal. When the diodes reverse, the voltage stored on C1 and C2 is increased by an amount equal to the voltage stored at the junction of D2 and D3.

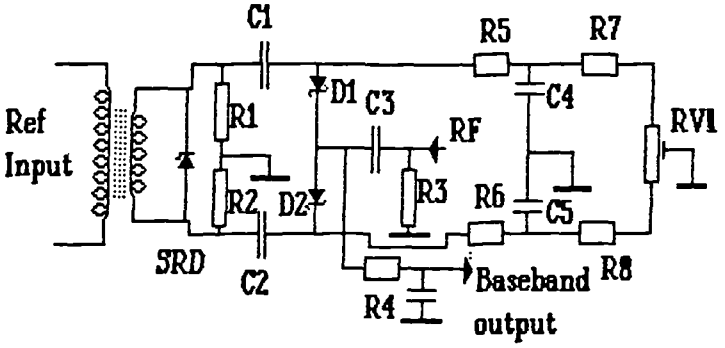


Fig 5.17a Commonly used sampling phase detector

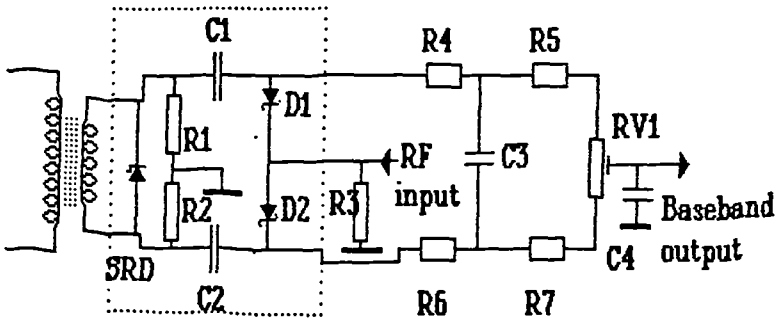


Fig 5.17b Improved phase detector for greater bandwidth

A problem exists in that the stored voltage is decoupled to ground through C4 and C5. This provides a pole at a low frequency forcing a reduction in loop bandwidth, which would be unsatisfactory if there were a possibility of injection locking, or if it were to be used in a high vibration environment, or in a frequency hopping synthesiser where the locking time must be small. The author has investigated the problem of the phase detector pole. A synthesiser was built whereby a 1GHz signal was phase locked to a 2.5MHz comb generator. A plot of the response of the phase detector in terms of peak amplitude at the output against error frequency was obtained. The response obtained was approximately single pole, first order and the point at which the output was 3dB down on the DC level taken as the phase detector pole frequency. There must be an allowance for the sinc ωt sampling function in this calculation. Calculations based on these measurements reveal a phase detector pole at 180kHz, which would restrict the natural frequency ω_n of the loop to approximately 50kHz. This means that problems could be encountered since the VCO was a low Q very wide bandwidth device. There is a danger of problems due to injection locking of the VCO (see §5.6.3).

A modification to the circuit therefore was devised. Fig5.17b displays the modified circuit. Separation of the bias circuits from the signal circuits has been achieved. The bias is developed across C3. Baseband signals are developed across C1, C2, and C4. Resistors R3, R4, and RV1 provide the second half of the bridge. DC Balance is provided by RV1. Measurements on the improved circuit revealed a pole at 800kHz. Increasing the reference frequency to 10MHz increases the pole to 1.675MHz.

5.4.3.4 Upper frequency of operation of sampling phase detector

The maximum frequency of operation of the above described circuit will be set by the amplitude of the comb and the effect of stray components in the circuit. The maximum frequency of operation was measured to be 1.6GHz. In order to increase this it is possible to either:-

(1) add reflectors to speed up the switch off of the diodes; or

(2) use an integrated comb generator phase detector.

Method 1 is based on the sampling detector arrangement designed by Grove [1967]. This phase detector operates by allowing the reflected wave from a short circuit to turn off the detector diodes after they have been turned on by the SRD pulse wave. The reflected wave will be 180° out of phase with the applied wave, and will cancel the effect of the applied waveform. Fig5.18 gives a circuit of a microstrip equivalent of the Grove method.

By using the arrangement of fig 5.18 the maximum frequency of operation was doubled to 3.2 GHz. The circuit is similar to fig 5.16a apart from the addition of microstrip lines X1 and X2. These lines reflect the pulse back to the diodes, turning them off after a time interval equal to twice the propagation length of the microstrip line. However, since the SRD used has a risetime of 50 ns, it is evident that the maximum frequency of operation is restricted by the inductance arising from interconnections between the components. There is commercially available a complete phase detector package measuring 1mm x 1mm which can operate up to 20 GHz [Metellics, 1989], the circuit equivalent of which is shown in the dotted area of fig 5.18. The increased speed is obtained due to the small size of the device.

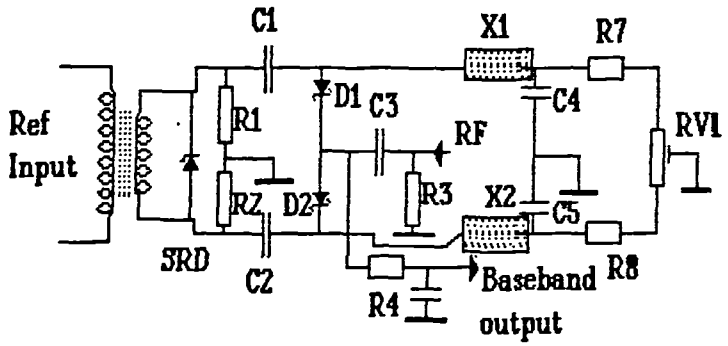


Fig 5.18 Speeding up sampling phase detector by means of reflection strips X1 and X2.

5.4.3.5 Two Phase detector approach

In order to overcome the problems of linearity and reference feedthrough, a two phase detector approach has been recommended [Underhill, 1977]. The phase frequency detector is used for acquisition, and a ramp and hold type detector is used to maintain lock. Utsi [1983] also recommends the ramp and hold phase detector to solve the linearity problem. Underhill [1986a] suggests that a harmonic sampling phase detector could be used in conjunction with a rate multiplier type frequency locking loop to combine the low noise performance of the former with the broadband frequency locking capability of the latter. An alternative method to this was developed by the author [Wilson, 1988] where the frequency locking capability of the phase frequency detector is combined with the high frequency phase locking of the sample and hold phase detector as shown in figure 5.19.

The advantage of using the phase frequency detector in such a manner is that single IC synthesisers are available with a phase frequency detector built in, and the phase frequency detector can rapidly achieve lock.

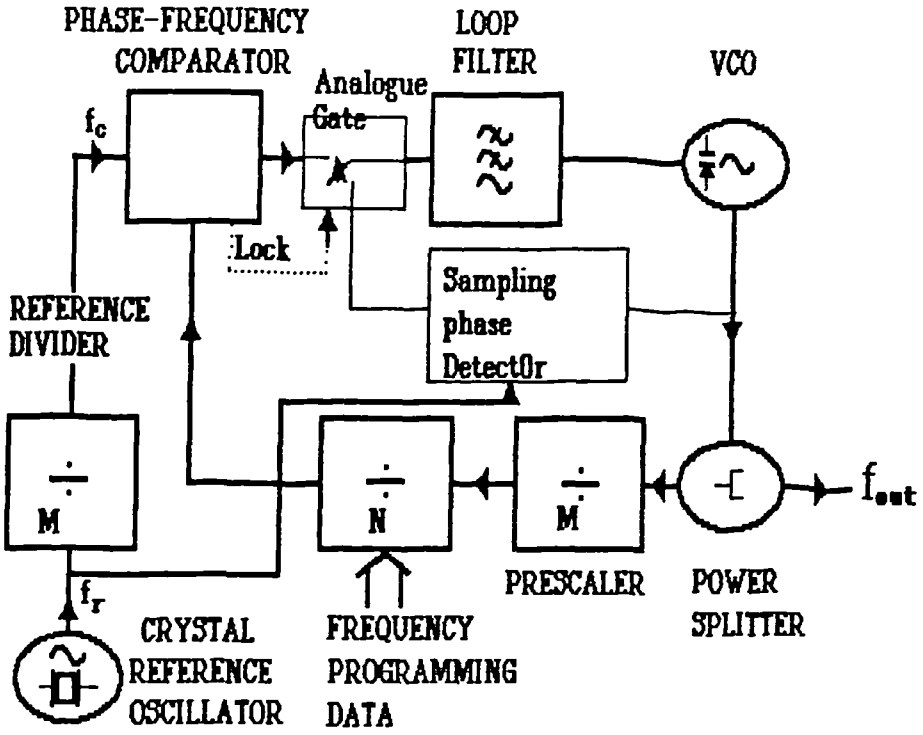


Fig 5.19 Two phase detector method of reducing phase noise

The harmonic sampling detector is phase sensitive and therefore does not have the frequency locking capability of the frequency detector. Therefore, the initial locking is achieved using the phase frequency detector and, when the phase error is reduced to a low value, the sampling phase detector assumes control. The phase frequency detector must then be removed from the loop, otherwise contention will occur between the two controllers. There is still a requirement for the phase frequency detector to monitor the locking condition of the loop. It is not necessary to operate the two detectors at the same reference frequency, the only required condition being that the detectors give a DC output at the same frequency. The phase detector will lock to any harmonic of the reference frequency:-

$$f_{out} = f_{ref}N \tag{5.12}$$

where the factor N is an integer. For the divider arrangement of fig5.19, the relationship for locking is:-

$$f_{out} = f_{ref}N\frac{M}{R} \tag{5.13}$$

In order for both arrangements to lock at the same output frequency f_{out} then we require $R = M$. Therefore the problem of the phase comparison frequency having to be reduced

if a fixed prescaler *M* is used, is overcome. This is of great benefit as fixed prescalers are available at frequencies of up to 5GHz and variable modulus prescalers manage 1.3GHz at present. This method also gives greater flexibility over the choice of prescaler. If locking time is not critical, then the prescaler could be replaced with a fixed divider. The advantage of the two phase detector approach is therefore:-

(1) The problems of reference feedthrough of the phase frequency detector are reduced;

(2) The phase noise is much lower and more easily predicted;

(3) Higher phase comparison frequencies can be used;

(4) The elimination of the variable modulus prescaler results in reduction in complexity and current consumption and easier sourcing of devices;

(5) Loop gain parameters are independent of changes in *N* value;

(6) Higher phase detector gain reduces sensitivity to hum and amplifier noise.

One of the problems that need to be overcome is a method of fast reliable switching between the phase detectors. When transfer occurs, the phase detector must be switched into the loop and the phase frequency detector must be removed. This must be achieved without introducing transients into the loop that may cause the loop to lock at the wrong harmonic of the reference frequency. One method of overcoming this problem is with a Schottky diode gate.

5.4.3.6 Measurement of performance of 2 phase detector loop

A single loop synthesiser including a Fast TTL phase detector was built with the minimum of gates in the signal path. The performance was measured against a unit containing a dual phase detector.

A synthesiser built by the author to include the two phase detector method had output spectra as displayed in fig 5.20. This measurement was obtained on a HP 8566B spectrum analysers. One of the traces is that of the output when the phase frequency detector is maintaining lock. The second trace is that of the harmonic phase detector controlling the VCO. Table 5.1 displays a comparison between two identical step size synthesisers. Apart from a 20dB reduction in static phase noise, there is a vast improvement in discrete spurious and the increase in loop bandwidth enables an increase of 29 dB of loop suppression of dynamic phase noise originating in the VCO.

Table 5.1 Comparison of measured synthesiser performance for an output frequency of 2GHz and a channel step of 2.5MHz		
	Fast TTL detector	*Dual detector*
Phase Noise at 2.5 kHz offset	-83 dBc/Hz	-103 dBc/Hz
Reference sidebands	-35 dBc (625 kHz)	-70 dBc (2.5 MHz)
Loop natural frequency (f_n)	15 kHz	80 kHz

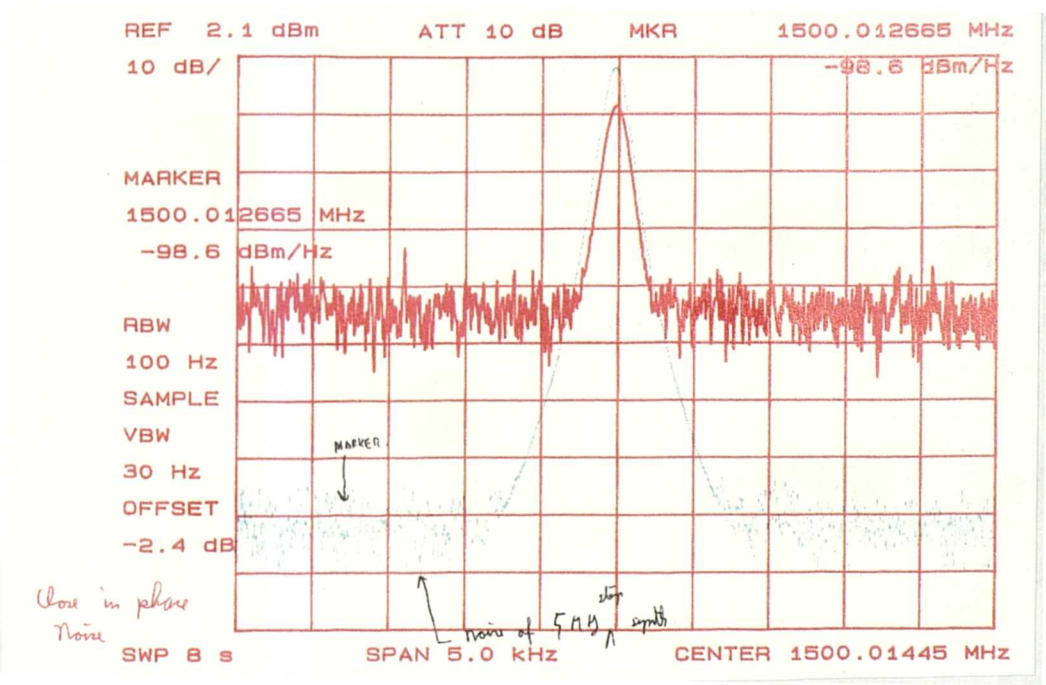


Fig 5.20 Spectrum analyser plot of the two phase detector synthesiser at 1.5 GHz output

5.4.4 Analogue multiplier

The analogue multiplier, together with the digital equivalent, the exclusive-or gate, is also ubiquitous in frequency synthesisers. The input signals are multiplied together, to yield the following:-

$$\mathrm{Sin}(\omega t + \alpha)\mathrm{Sin}(\omega t + \beta) = \frac{1}{2}\left(\cos(\alpha - \beta) - \cos(2\omega t + \alpha + \beta)\right) \qquad (5.14)$$

Equation (5.14) suggests that upon achieving phase lock there will be an unwanted component at twice the input frequency, and the baseband output will be zero, with $\alpha - \beta = \pi/2$, ie the input is in quadrature. This type of phase detector is well covered in the literature [eg. Robins, 1982 (2)]. It is phase sensitive only, therefore an acquisition aid will be required [eg. Cheah, 1991]. If the inputs are not sinusoidal, there is a potential for self locking onto a harmonic of the input signal. Of particular hazard is a frequency divider with a third harmonic which is only 10dB down on the fundamental. To avoid false lock, therefore, an exclusive or gate should be used with digital signals. A squarewave digital signal at the gate is equivalent to a sinewave at the analogue multiplier, therefore if the harmonics of one signal lie at the same frequency as the fundamental of the other, then there is no resulting DC output. However two signals of equal fundamental frequency will give rise to a DC output.

5.4.5 Linear ramp phase detector

The linear ramp phase detector, also known as the dual sampling detector or ramp sampling detector, is also well covered in the literature [eg. Underhill, 1980]. Its greatest virtue is its linearity and excellent reference sideband rejection. The essential feature is a ramp which converts time intervals into a voltage levels. If the time interval is started on the reference pulse edge and finishes on the divided output of the VCO edge, then this time interval is proportional to the phase difference between the waveforms.

Fig 5.21 gives a simplified circuit diagram and fig 5.22 displays the operation of the ramp sampling detector. The S-R flip flop on the LHS of fig 5.21 provides a pulse for the duration of the phase difference between the input waveforms. Capacitor C1 is charged by switched current source I1 resulting in a voltage ramp across C1. When a transition occurs at the VCO input, the ramp is stopped. The resultant phase error value is temporarily stored in C1. During this hold period, C2 is connected to the output of C1. In fig 21 a monostable is used to determine the time duration that C2 is connected to C1. This is intended for illustrative purposes only, and in practice the C2 sampling pulse would be derived from the VCO divider chain. Before the end of the reference cycle, C2 is disconnected from C1, and the charge in C1 is dumped to ground. Due to this secondary sampling effect, the reference feedthrough rejection is very good, and extra filtering, apart from the loop filtering may not be necessary for most applications. The phase noise, however, is measured to be the highest of any of the phase detectors. At 25 kHz comparison frequency, the phase noise of this type of phase detector (Plessey NJ88C25) was measured to be - 134 dBc/Hz, as against - 156 dBc/Hz for a CMOS phase frequency detector both referred back to 25kHz. The increased noise could be due to the increased complexity of this type of circuit and the possibility of extra noise introduced in the capacitor charging and discharging circuits.

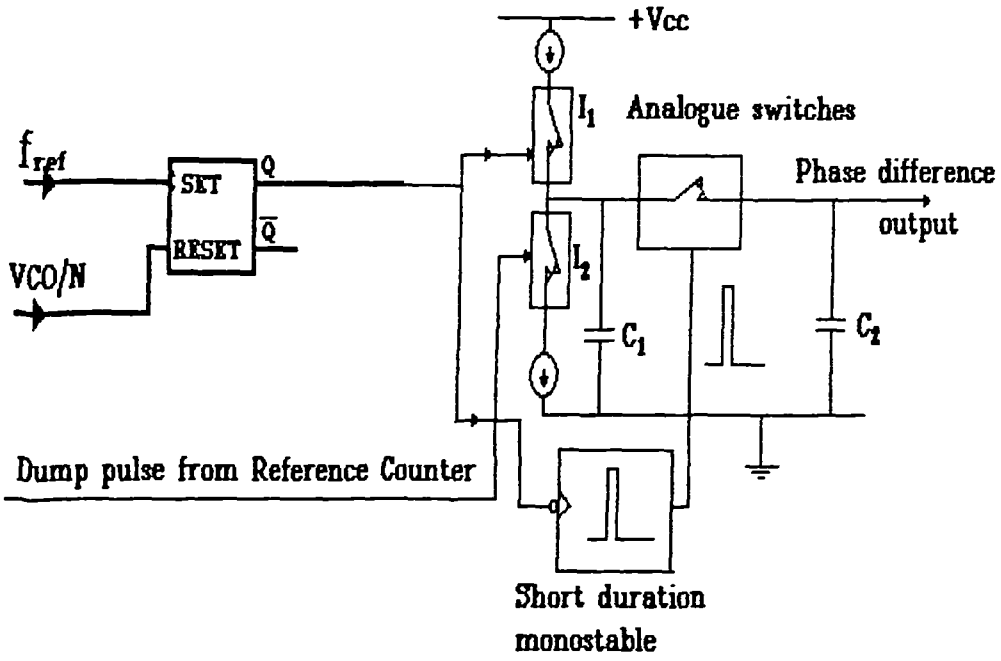


Fig 5.21 Dual sampling phase detector, circuit diagram

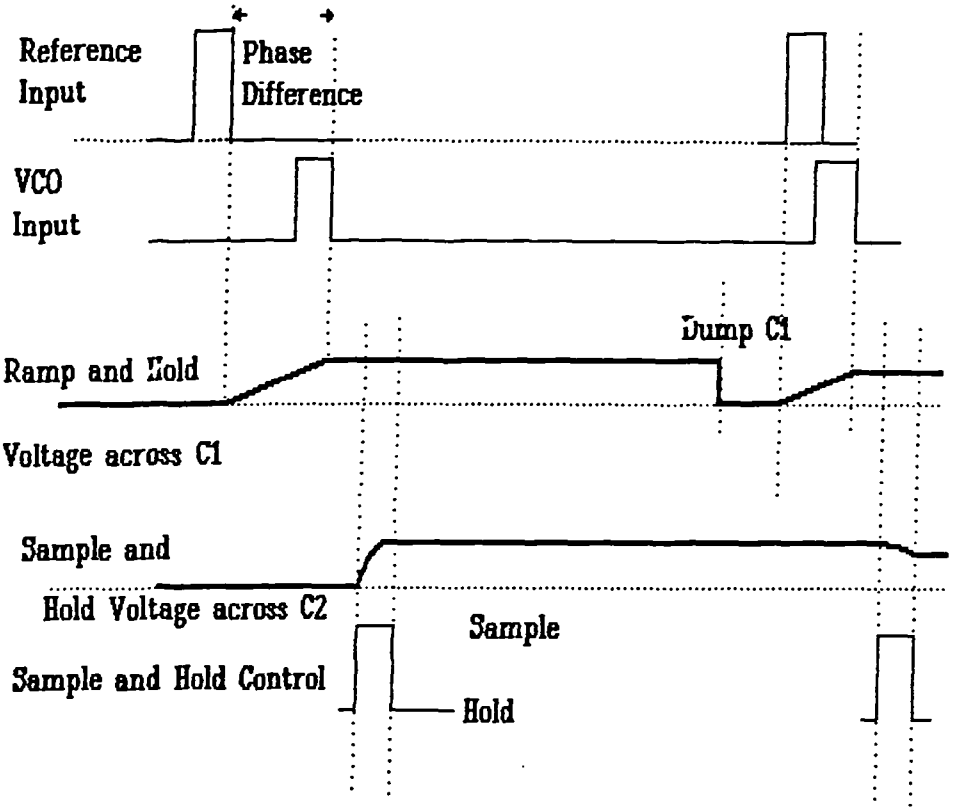


Fig 5.22 Dual sampling phase detector operation

5.4.6 Image rejection phase detector

A problem exists when using a phase detector for the transfer section of a multiple loop synthesiser, such as fig 5.23.

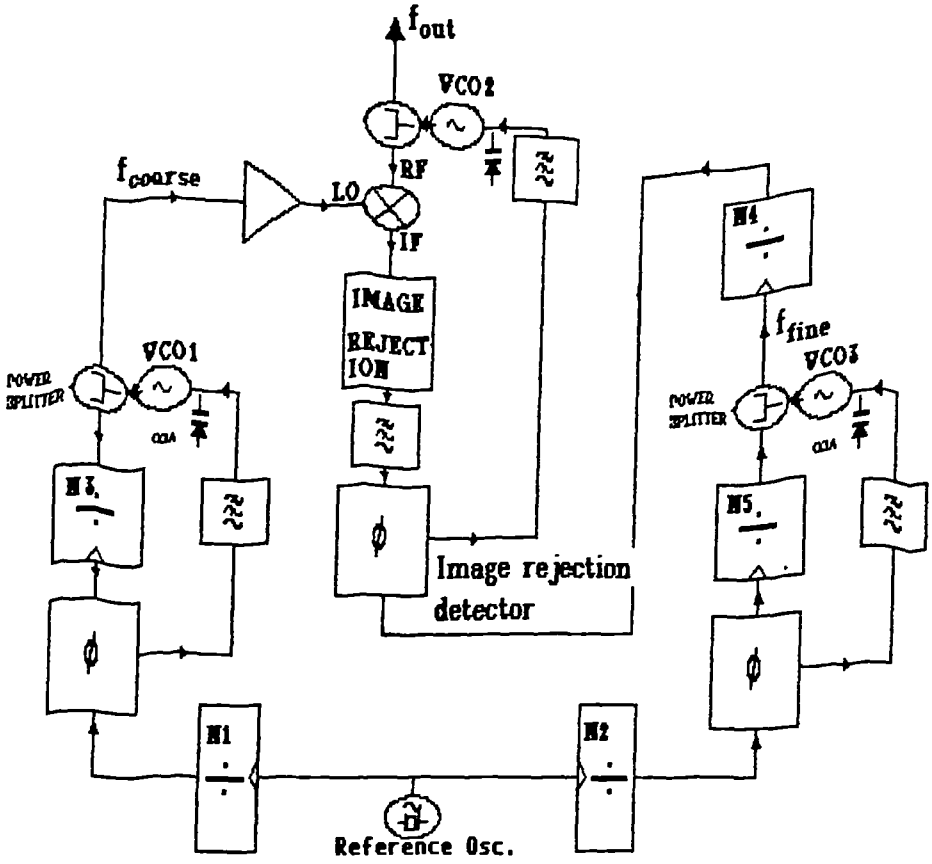


Fig 5.23 3 loop summing, or vernier synthesiser

Chapter 4 established that for good spurious response rejection, VCO1 and VCO2 should be as close together in frequency as possible. However, if very accurate tracking of the VCOs is not achieved, then there is a possibility of the frequency of VCO2 to be on the wrong side of that of VCO1 (eg. at the difference frequency rather than at the sum). In this case, there will be a difference frequency in the translation loop, but an ambiguity exists as this frequency could be equal to the same difference frequency if VCO2 is greater than or less than in frequency to VCO1. In order to resolve this ambiguity, an image rejection phase detector was designed that contributed towards a patent application [Hardstone, Lees &Wilson, 1991]. Fig 5.24 displays the functional diagram of the image rejection phase detector.

In the image rejection phase detector, the output of VCO2 is split into an in-phase and quadrature component. These components are mixed with the output from VCO1 and the following results occur:-

Case 1 If $\omega 2 < \omega 1$

In phase mixer:

$$\sin(\omega_1 t)\sin(\omega_2 t) = 1/2(\cos(\omega_1 - \omega_2)t - \cos(\omega_1 + \omega_2)t) \qquad (5.15)$$

Quadrature mixer:

$$\sin(\omega_1 t)\cos(\omega_2 t) = 1/2(\sin(\omega_1 - \omega_2)t + \sin((\omega_1 + \omega_2)t) \quad (5.16)$$

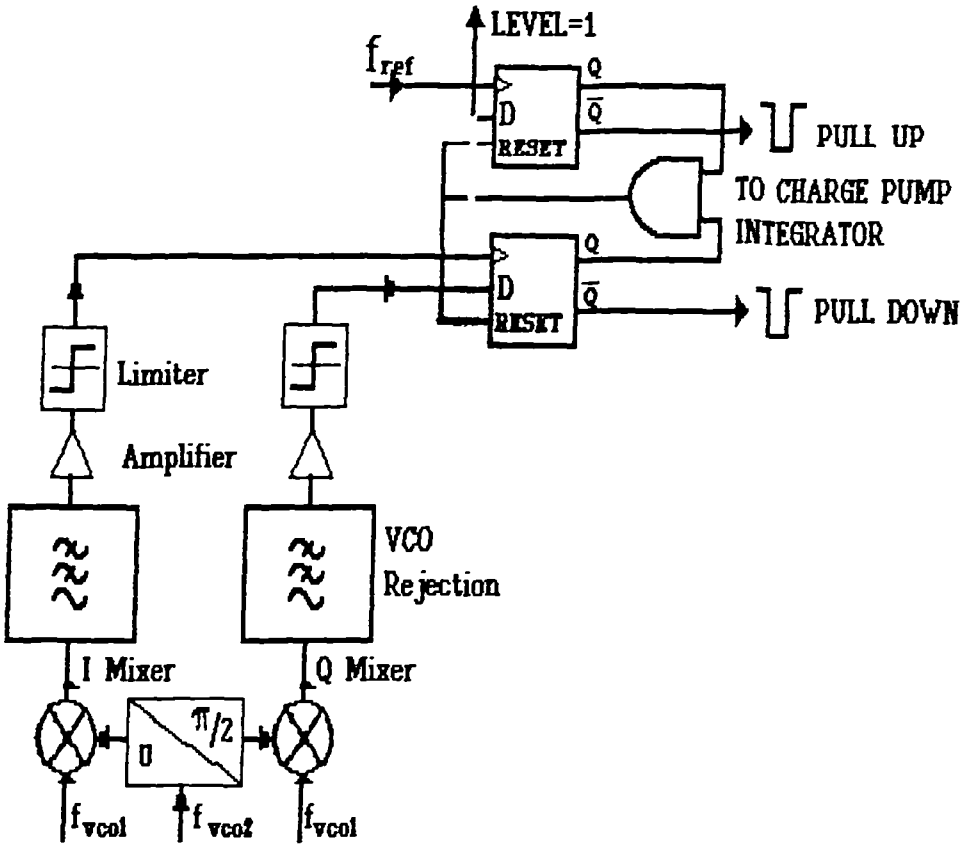


Fig 5.24 Image rejection phase detector

Case 2 If ω2 > ω1

In phase mixer:

$$\sin(\omega_1 t)\sin(\omega_2 t) = 1/2(\cos(\omega_2 - \omega_1)t - \cos(\omega_1 + \omega_2)t) \quad (5.17)$$

Quadrature mixer:

$$\sin(\omega_1 t)\cos(\omega_2 t) = 1/2(-\sin(\omega_2 - \omega_1)t + \sin((\omega_1 + \omega_2)t) \quad (5.18)$$

For all the above cases, the difference term that is required for phase locking is the first term on the right and the unwanted sum signal is the second term. In the first case, when VCO2 is lower in frequency than VCO1, the I mixer phase detector error will lead the Q mixer phase detector error phase error by $\pi/2$. In the second case, the Q mixer output will change phase by π in relation to the first case, and therefore the I mixer output will now lag the Q mixer output by $\pi/2$.

At the phase detector, the in-phase signal input clocks the signal flip flop and the quadrature component becomes the D input. When the VCO2 is tuned to the incorrect side of VCO1, the signal flip flop becomes permanently reset and the reference permanently set, resulting in a rapid return to the correct side of VCO1.

The advantage of the image rejection phase detector detector in a multiple phase locked loop synthesiser is that VCO1 and VCO2 can operate much closer together in frequency, therefore any harmonic intermodulation products at the mixer would be of higher order and thus at a very low level. This results from the fact that higher terms in the mixer analogue multiplier intermodulation characteristic have lower values of coefficients.

5.4.7 Summary of phase detector survey

Phase frequency detectors possess the useful property of being able to perform frequency and phase acquisition simultaneously. On locking, however, noise performance is inferior to that obtained using other types of phase detector. Good noise performance is possible by the use of a microwave sampling phase detector. Combining the two detectors into a PLL synthesiser and automatically switching between them enables a rapid acquisition loop with good noise performance to be built.

The image rejection phase detector enables achievement of rapid acquisition in a summing loop where the output frequencies and reference frequencies are close.

5.5 Simulation of a PLL Synthesiser

5.5.1 Introduction

It has been described in chapter 4 why direct digital synthesis (DDS) is the ideal method of synthesis for a frequency hopping or fast frequency agile source, although this may have to be combined with other synthesis methods such as PLL synthesis in order to achieve the desired range [Harris, 1991]. Wide bandwidth phase locked loops are necessarily to ensure fast switching speed, and the normal PLL design procedures are complicated by the discrete time nature of the digital sections of the PLL. For this reason, in order to investigate settling times of phase locked loop synthesis after frequency hops, software simulation of the PLL was written which is further discussed in appendix A3.

Frequency agility requirements fall into four distinct cases for data communications systems:-

1) Fixed frequency communications

This refers to a case when the frequency is selected by the user and then remains on that channel until a further instruction to change channels is received from the user. The settling time requirements for such a system are not critical, as a channel change transient is not anticipated during normal communications.

2) Signal tracking synthesiser

In this case, the synthesiser is used to track the signal, allowing for temperature drifts and Doppler shifts. Here, the following are required for the synthesiser:-

a) Fine enough resolution in frequency in order to avoid BER degradation or loss of carrier lock during tracking;

b) The frequency change transient should be of short enough duration to avoid degradation or loss of lock.

The frequency changes are typically of small frequency steps.

3) Slow frequency hopping

The frequency channel is changed at periods of many data clock cycles. One common implementation is to aid in the provision of secure communications for civil systems. In this case it may be possible that coherent detection can still be used. The requirements are similar to the tracking synthesiser, but frequency change is more random, and can result in large shifts in frequency. Slow frequency hopping can also be used in conjunction with other communication techniques such as direct sequence spread spectrum [Dixon, 1985].

4) Fast frequency hopping

The frequency channel is changed at the data rate, or at greater rates than the data rate. In this case coherent communication is impossible due to non-coherent combining at the receiver and non-coherent combining loss occurs. The principal requirement for synthesiser design in this case is fast switching and low settling time.

In all the above cases, apart from case 1, the frequency change response time is of critical importance.

5.5.2 Using a hybrid synthesis scheme to obtain low settling time frequency agility

With a hybrid synthesis scheme it is vital that the various tradeoffs are examined so that the subsections that make up the hybrid can be configured correctly. As discussed in §4.8.3.4, a PLL can be used to ensure full bandwidth coverage, and a time domain simulation can be used to aid correct selection of reference frequency and other loop parameters.

5.5.3 Phase locked loop synthesis

In the past phase locked loop digital $\div N$ synthesis was associated with slow frequency stepping [Gorski - Popiel, 1979]. A block diagram of such a synthesiser is displayed in fig 5.32 of §5 7.2 of this chapter. This association arose out of a misunderstanding about the effect of digital devices within a phase locked loop; this will be elucidated in the paragraph below. Before the problem was seriously addressed, PLL loop bandwidth would typically have been reduced to a maximum of 1/40 of the reference frequency, at which the loop would have been indistinguishable from that of the analogue loop, and therefore could be analysed by the usual equations. A slow response and poor resistance to microphony are a consequence of the use of too narrow a loop bandwidth.

Initial investigations by workers in the field revealed discrepancies between the observed behaviour of a PLL and the usual analogue equations as the loop bandwidth approached the reference frequency [eg. Przedpelski, 1983]. The discrepancies suggested some dead time or delay effect. This delay effect was initially ascribed to "divider delay" in which the finite delay between signal input to the dividers and the output was held responsible [Goldman, 1984]. Work by Egan [1984] and Crawford [1985] suggested that the sampled time nature of the digital phase detector was responsible, and could be allowed for by a time delay of $\exp(-sT_s)$ into the open loop transfer function. This is equivalent to multiplying the magnitude by a factor of unity and adding an open loop phase shift of $\omega T_s/2$. The stability is determined from Bode plots in the usual way, and gives a pessimistic result for the stability of the loop. Crawford suggested that a more accurate result would be obtained from a Z transform analysis of the PLL response. Blake [1988] applied the sampling model of a PLL and predicted frequency and phase lock in approximately 8 sample periods for the optimum step response loop. The optimum loop natural frequency would be 23% of the reference frequency and a natural frequency of 32% is the maximum limit for stability.

Baker [1989] suggested that for a phase frequency detector there is no sampling delay, but that the sampling delay should be added if a sample and hold device be used in the loop. He then went on to apply the Z-transform to a third order type 2 loop with a sample and hold phase detector. Egan [1991] arrived at the conclusion that the sampling delay must be applied if the phase frequency detector is used with a second order type 2 loop; but not if used with a third order type 2 loop having the additional pole much less than the reference frequency. This is because a second order loop does not have any loop filtering at the reference frequency and all the higher order sampling terms are allowed through. The higher order terms contribute to the sampling delay. If a filter is applied as with a third order loop, the higher order terms are negligible compared with the fundamental, and consequently cannot increase the phase delay. This suggests that a third order type 2 loop is more desirable for use with a phase frequency detector since better reference rejection is obtained for little degradation in loop stability. With a speed optimised phase locked loop, there is little filtering of the reference components, leading to problems with reference sidebands. We overcame these problems with the aid of a second analogue phase detector as mentioned in §5 4.3.5 above.

5.5.4 Computer aided design of phase locked loops

If more filter stages are included after the loop filter, the Z transform analysis becomes complicated and a simulation program would be desirable. This is particularly the case with a practical high speed loop where the response of the VCO must be taken into account [Harris, 1989]. Conventional phase locked loop analysis programs perform a frequency domain analysis on the loop. The phase detector and VCO are given an approximate characteristic, and the Laplace transform of the loop filter stage is taken. Any post loop filtering is then added in the form of a Hurwitz polynomial [McGillen & Cooper, 1986]. The combined open and closed loop transfer functions are then evaluated. Initially, a commercially available software package that followed this approach was evaluated by the author. This is a dedicated synthesiser design package by Rohde [1983d], the "PLL Design" kit, available from Compact Corp. Unfortunately the program calculated (wrongly) stable results for a phase locked loop with a natural frequency greater than the reference frequency. Such a result is not possible for a loop that includes digital phase detectors or dividers. Therefore a program is designed that gives more accurate results for loop bandwidths close to the reference frequency, and this program is described below.

5.5.5 Phase locked loop simulation program

5.5.5.1 Method of simulation

The author proceeded to write a dedicated phase locked loop simulation program. Simple documentation on this design is given in appendix A2 and a listing of this program is given in appendix 2. A time domain simulation method is used which solves the loop differential equations over discrete intervals in time. Fig5.25 is a block diagram representing the simulation model. Output and reference frequencies are indicated by f_v and f_{ref} respectively. An improvement on Badger's [1988] method is used in that the implicit Trapezoidal integration rule is applied rather than the Backward Euler method to the simultaneous differential equations, resulting in greater accuracy as discussed later in Chapter 7. The phase detector is the conventional phase frequency type, although this could be replaced by other types if necessary, and is described by its logical function. A charge pump type loop filter is assumed, although this could be replaced by an op-amp type. The time increment is represented by Δt.

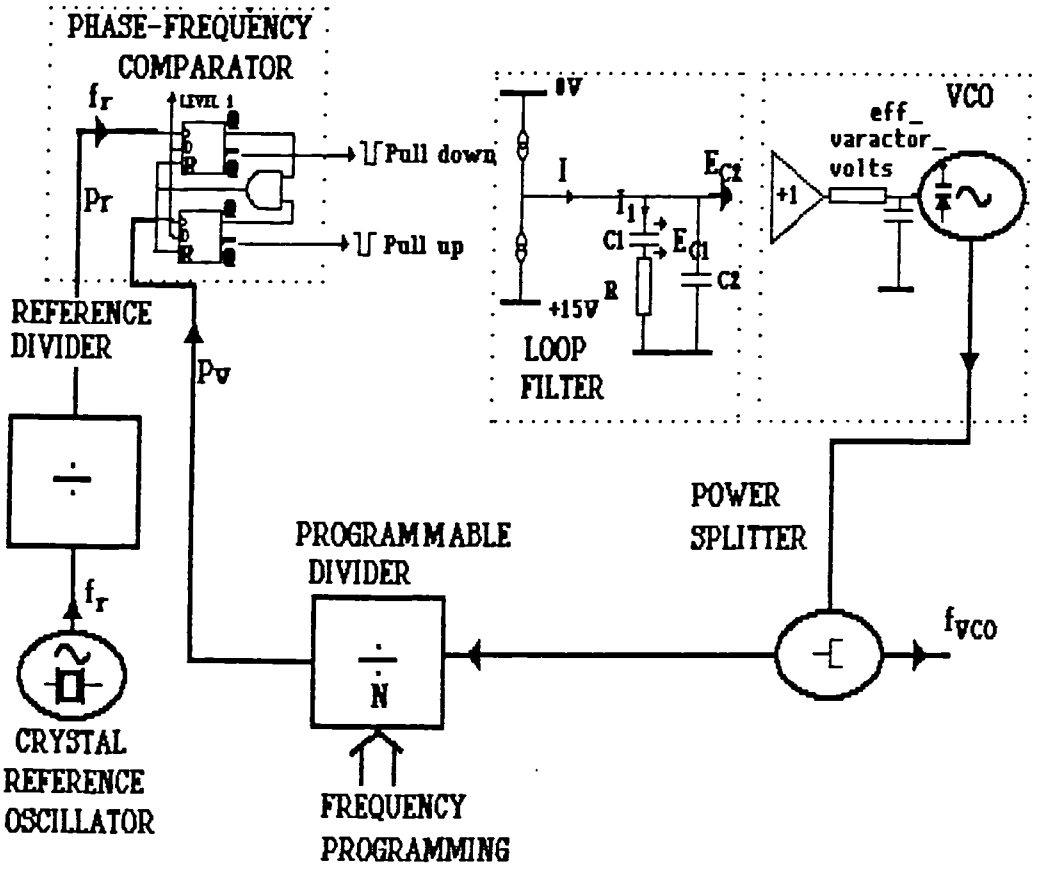


Fig 5.25 PLL simulation, models and variables

5.5.5.2 Loop filter in simulation

As with the step recovery diode simulator in chapter 7, a trapezoidal integration is carried out for the capacitors in the loop filter capacitor. For a capacitance *C*:-

$$E_c = \int_{n-1}^{n} \frac{I(t)}{C}\,dt \tag{5.19}$$

Applying the integration rule to this:-

$$E_{c(n)} = E_{c(n-1)} + \frac{I_{(n-1)}dt}{2C} + \frac{I_{(n)}dt}{2C} \tag{5.20}$$

where $E_{c(n)}$ is the present step voltage across capacitor *C*, and $E_{c(n-1)}$ is the previous step voltage across *C*, $I_{(n)}$ and $I_{(n-1)}$ represent the corresponding current values through the capacitor.

By applying Kirchhoffs' laws and the integration approximation of equation 5.20 to the loop filter network the following equations are produced:-

$$E_{c1(n)} = E_{c1(n-1)} + \frac{I_{1(n-1)}dt}{2C_1} + \frac{I_{1(n)}dt}{2C_1} \tag{5.21}$$

$$E_{c2(n)} = E_{c2(n-1)} + \frac{(I_{(n-1)}-I_{1(n-1)})dt}{2C_2} + \frac{(I_{(n)}-I_{1(n)})dt}{2C_2} \tag{5.22}$$

$$E_{c2(n)} = E_{c1(n)} + I_1R \tag{5.23}$$

A problem lies in applying the above equations directly in that the unknown current I_1 is implicit. This can be overcome by rearranging the equations in the form:-

$$I_{1(n)} = \frac{2C_1C_2\left(E_{c2(n-1)} - E_{c1(n-1)}\right) - I_{1(n-1)}\,C_2\,dt + C_1dt(I_{(n)} + I_{(n-1)} - I_{1(n-1)})}{C_1\,dt + C_2dt + 2C_1C_2R} \tag{5.24}$$

$$E_{c1(n)} = E_{c1(n-1)} + \frac{(I_{(n-1)} - I_{1(n-1)})dt}{2C_2} + \frac{(I_{(n)} - I_{1(n)})dt}{2C_2} \tag{5.25}$$

$$E_{c2(n)} = E_{c1(n)} + I_1R \tag{5.26}$$

I_1 can be first solved, enabling $E_{c1(n)}$ to be obtained, followed by $E_{c2(n)}$. These values are then stored for use as the n-1 values in the next time increment.

More complicated loop filters, such as elliptical filters can be included by either forming the network equations into a matrix as in chapter 7, or by applying the bilinear transform to the poles and zeros of a loop filter [Hatcher, 1989].

5.5.5.3 Results of optimum settling time simulation

Fig 5.26 displays the results of a simulation of a PLL synthesiser with the values of phase locked loop components given in table 5.2. The loop filter, consisting of C1, *R* and C2, is a lead lag type followed by a reference filter capacitor, giving the loop a third order type 2 characteristic.

Table 5.2

Simulation element		Circuit value	Units
Reference frequency	f_r	1	MHz
Division ratio	*N*	200	
VCO tuning at 0 Volts		150	MHz
VCO Tuning at 2 Volts		250	MHz
Phase detector; dual flip flop PFD			
VCO settling time constant		10	ns
Charge pump current	*I*	1	mA
Loop filter capacitor	C_1	200	pF
Damping resistor	*R*	6	kΩ
Post loop filter capacitor	C_2	40	pF

In Fig 5.26, varactor tuning voltage (fine trace) and phase error (bold trace) are plotted against the time axis. The centre of the plot represents zero phase error.

The loop settles in approximately 6 reference cycles, that is 6μs. However this settling time is very sensitive to changes in loop parameters. For example a rise in loop gain of 3 dB from the optimum settling point results in an unstable loop giving oscillations at half reference frequency. This simulation is extended later in this chapter to enable study of locking phenomena and loops of different order.

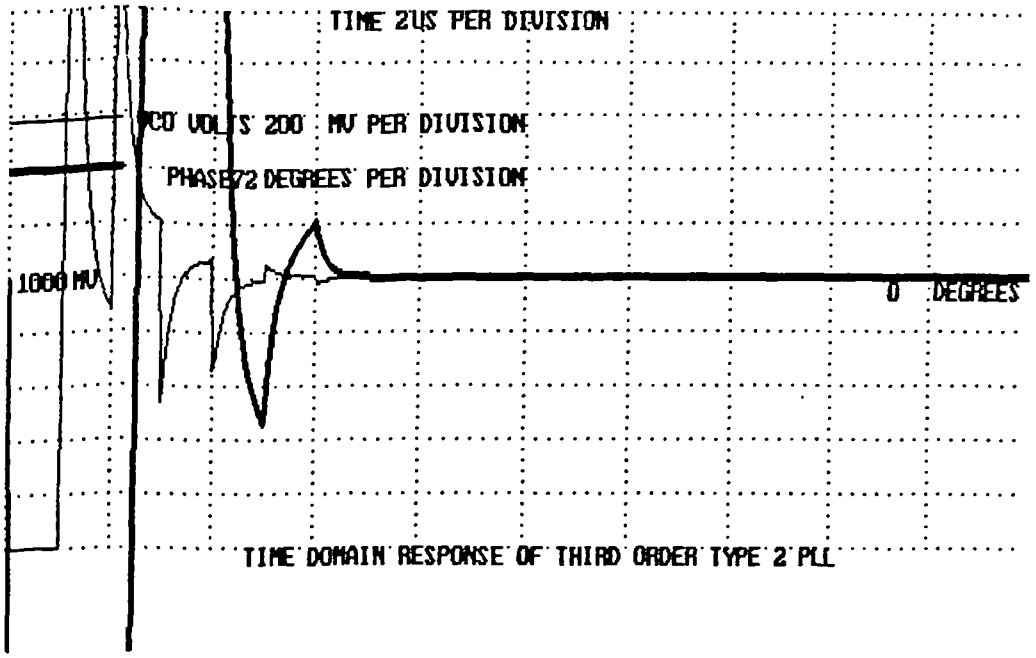


Fig 5.26 PLL simulation, result for an optimum settling time loop

5.5.5.4 Summary of time domain simulation of PLL

Consideration of the switching and settling time of a synthesiser has led to the development by the author of a time domain simulation program for phase locked loop synthesisers. Commercially available software for PLL synthesis does not consider the sampling effects of dividers and phase detectors, hence giving inaccurate results as the natural frequency approaches the reference frequency. Armed with a suitable model of a phase locked loop it is now possible to examine further problems that may occur within synthesisers such as injection locking.

5.6 Spurious signal injection into local oscillators

5.6.1 Introduction

Spurious signals incident upon a free running oscillator can have various effects depending upon the frequency difference between the spurious frequency and the

oscillator frequency. Sources of induced spurious signals can include radiated signals, power supplies, mixers connected to the oscillator output, and varactor tuning circuits. Although these susceptibilities are displayed by any free running oscillators, this section will dwell on voltage controlled oscillators.

5.6.2 Effect of spurious signal injection on a free running oscillator

At RF, there are three effects of injection of spurious signals into an oscillator, depending upon the offset from carrier region:-

1) Broadband ($f_m > f_o/2QL$), offset from carrier (region 1);

2) Resonator bandwidth enhancement ($f_m < f_o/2QL$), offset from carrier (region 2);

3) Injection locking ($f_m << f_o/2QL$), offset from carrier (region 3).

Analysis of the effect of a spurious signal on an oscillator can be performed in a similar manner to the effect of noise in chapter 3. Bandlimited noise was considered to aid the analysis and here the same treatment is given a discrete spurious incident signal. In the broadband region 1, the output depends upon the position of the resonator. The spurious signal is additive to the VCO signal and subsequently modified by any limiting function and resonator function within the oscillator. The limiter results in the creation of two sidebands and a 6dB reduction of power in each sideband. This can be seen from equation 3.5 in chapter 3, but since only one sideband was incident upon the circuit, the power will be halved. The resonator will also attenuate the signal if there is a stopband for offset frequencies above the $f_o/2Q_L$ frequency. Since the resonator is the most likely susceptor for the interference [Manassewitsch, 1985b] a good position for the resonator is after the amplifier but before the limiter; a circuit with this configuration is least susceptible to external signals, providing care is taken with broadband interference if a hard limiter is used. In the broadband region, therefore, the spurious sidebands at the output can never be greater than the ratio of spurious signal to oscillator signal at the susceptor.

In region 2, there is effectively little attenuation of the spurious RF signal by the resonator. If the spurious signal is substituted for the phase noise in equation (3.7) in chapter 3, then assuming an ideal limiter the following relationship results:-

$$(N/C)_{out} = \frac{(N/C)_{in}}{4}\left(1 + \frac{f_0^2}{4Q_L^2 f_m^2}\right) \qquad (5.27)$$

Equation (5.27) suggests that there is a 20dB enhancement of the spurious signal for each decade reduction of f_m, as in the case of phase noise. Therefore the spurious sidebands can appear much larger than the incident spurious signal level which will be further

discussed in §5.6.2.1. This can be a major problem for the design of frequency synthesisers [Underhill, 1986b].

In region 3, an even more troublesome phenomenon can occur. In chapter 2, fig2.17, repeated as fig5.27, graphically displays the effect of phase noise on the oscillator by considering the resonator delay between vectors A and B of the modulation.

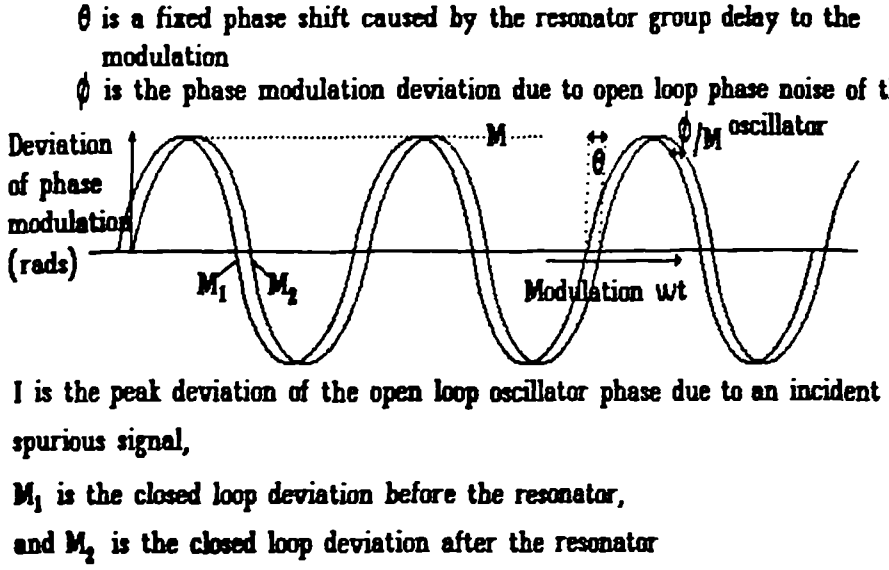


Fig 5.27 Time domain and vector diagrams for oscillator modulation by phase noise

For the case of an injected spurious signal, a similar analysis can be applied. Assume that a small signal **I** is incident upon the oscillator and is added to oscillator vector **A** at the input to the resonator r. **I** rotates around **A** at f_m. The resultant vector **B** now displays a phase shift of θ where:-

$$\theta = \text{Arcsin}\left(\frac{I}{A}\right)\sin(\omega_s t) \qquad (5.28)$$

This extra phase shift occurring in region 2 or 3 would violate the Barkhausen criterion for an oscillator, so the oscillator must react to enable a loop phase shift of zero. This can be accomplished in two ways: enhanced phase modulation for offset from carrier region 2, or injection locking for offset from carrier region 3.

5.6.2.1 Enhanced phase modulation

Here, as can be seen from the vector diagrams illustrating enhanced phase modulation given in fig 5.28, the incident spurious vector **I** rotates around oscillator vector **A**. The phase shift as given in equation (5.28) above occurs. The Barkhausen criterion for oscillation must still be satisfied, however. This can only be achieved by changing the phase shift through the resonator.

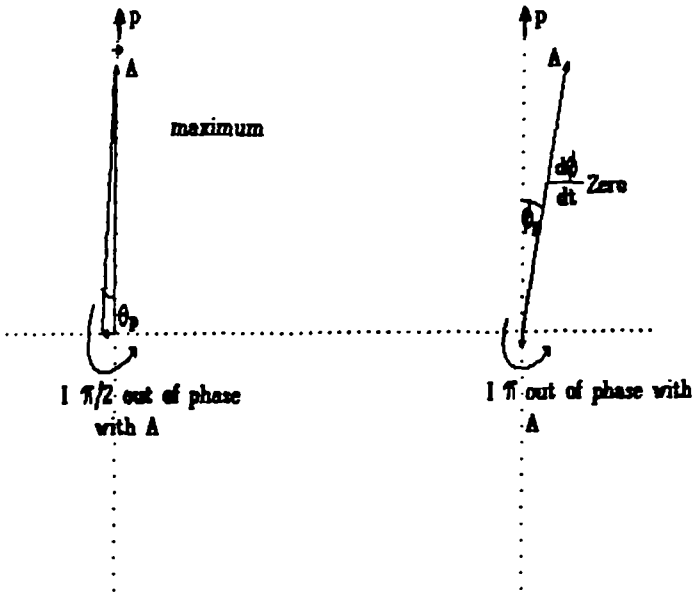


Fig 5.28 Local oscillator enhancement of incident spurious signal

Because of the resonator group delay Γ, additional phase shift through the resonator σ is related to oscillator output phase change from nominal where:-

$$\sigma = \Gamma\frac{d\phi}{dt} \tag{5.29}$$

Assuming the oscillator has phase modulation ϕ at a rate ω_m then the phase error ϕ will be:-

$$\phi = \phi_p \sin(\omega_m t) \tag{5.30}$$

where ϕ_p is the peak phase error.

Differentiating the above and looking for the maximum rate of change at the peak value of ϕ, that is ϕ_p, then:-

$$\sigma = \left(\frac{d\phi}{dt}\right)_{max} = \omega_m\phi_p \tag{5.31}$$

and:-

$$\theta_p = \sigma_p = \Gamma\omega_m\phi_p \tag{5.32}$$

In chapter 3, the relationship between oscillator loaded Q and group delay was shown to be:-

$$\Gamma = \frac{Q_L}{\pi f_0} \tag{5.33}$$

Substituting this into equation (5.29) gives:-

$$\frac{\phi_p}{\theta_p} = \frac{f_0}{Q_L 2f_m} \tag{5.34}$$

Assuming an ideal limiter, the conversion from incident power to phase shift is:-

$$\frac{N_0/C_{out}}{N_0/C_{inc}} = \frac{\phi_p^2}{\theta_p^2} = \frac{f_0^2}{Q_L^2 4f_m^2} \tag{5.35}$$

since the output spurious power is proportional to the angular deviation squared. If an ideal limiter is used, an incident spurious signal power n_0/C_{inc} is converted to spurious phase modulated sideband power by the relationship (see §2 6.1):-

$$n_0/C_{inc} = \frac{N_0/C_{spur}}{4} \tag{5.36}$$

Substituting this into equation (5.35) gives the oscillator output spurious for an incident spur power n_0/C_{spur}:-

$$(n_0/C)_{out} = \frac{(n_0/C)_{spur}}{4}\left(1 + \frac{f_0^2}{4Q_L^2 f_m^2}\right) \tag{5.37}$$

Fig 5.28 displays the effect of the spurious signals in a phase diagram. The line P refers to the average phase of the oscillator. Spurious signal I rotates at the spurious offset frequency. The rate of change of oscillator modulation angle ϕ produces phase shift through the resonator which is cancelled by **I**. When **I** lies on the vertical axis, then **I** is almost in phase with **A** and **A** will be at the stationary point at the peak of the deviation. Since $d\phi/dt$ will be at its lowest, σ will be zero. In fig 5.29 **I** is rotating at a slower rate and as a result ϕ is achieving large angular swings such that the small angle theory no longer applies. In this case **I** becomes perpendicular to **A** for a large portion of the cycle in the upper half of the diagram. The value of **I** that corresponds to the stationary points of ϕ moves to the left as shown.

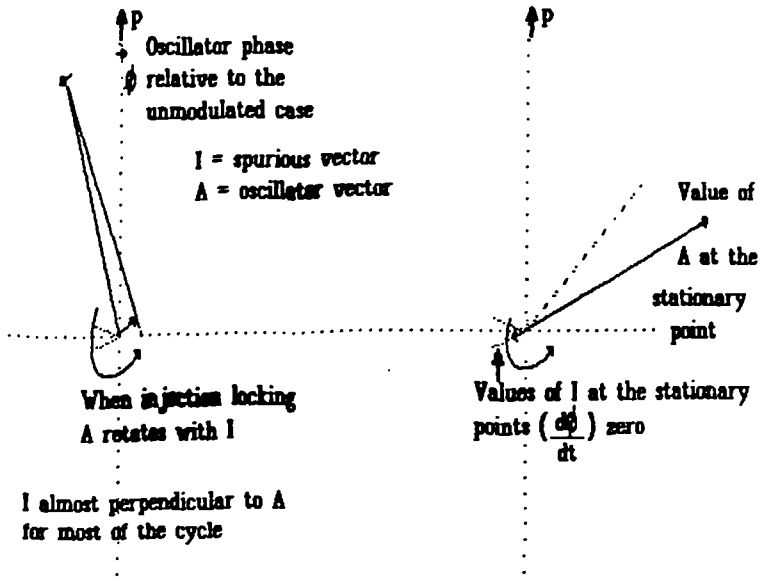


Fig 5.29 Effect of incident spurious signal under large signal conditions

5.6.2.2 Injection locking

Referring again to fig 5.29, the next logical step is for **I** to remain perpendicular to **A** for a full half cycle of **I**. For this to occur,

$$\left(\frac{d\phi}{dt}\right) = \frac{\omega_m}{2} \tag{5.38}$$

Rather than vector **A** swinging back and forth as above, the vector will continue to rotate in the same direction. From equation (5.33):-

$$\sigma = \frac{\tau\omega_m}{2} \tag{5.39}$$

The rotation of *m* provides a phase shift which is exactly compensated by **I**. In this case **A** rotates continuously with **I**. This results in the third condition listed at the beginning of §5.6.2 which is known as injection locking [Kurokawa, 1969]. In this case, the oscillator becomes monotonic at a frequency $f_o - f_m$ and the output at f_o suddenly disappears.

Using equation (5.33) it is possible to examine this effect further. Substituting for Γ results in:-

$$\sigma = Q_L \frac{f_m}{f_0}. \tag{5.40}$$

The incident power needs to provide this angle. Since the two vectors are at the same frequency, voltage addition will take place. Addition of **I** occurs in a peak to peak manner to increase the phase of **A**. The following value of σ results,

$$\sigma = \frac{I}{A} \tag{5.41}$$

Combining this with equation (5.40) results in the following condition for injection locking:-

$$\frac{P_i^2}{P_0^2} = Q_L \frac{f_m}{f_0} \tag{5.42}$$

The factor f_m in this case defines the "locking bandwidth" whereby the oscillator will injection lock over twice f_m around f_o. The actual process involved is far more complex than this simplified analysis suggests since the differing effects of the limiter on the monotonic and non-monotonic signals has not been taken into account, neither has the effect of the oscillator loop gain. The capture effect of the limiter results in the suppression of the non dominant signals by 6dB [Underhill, 1989]. The result of this is that there is 6dB more gain for the signal at f_m when the oscillator becomes monotonic. This, together with the excess gain normally provided to maintain oscillation can result in considerable hysteresis whereby the oscillator, once locked can remain locked over a region greater than the locking bandwidth. In addition, various chaotic states are possible due to the heavily non-linear injection process.

It has been suggested [Farr, 1986], [Lucus, 1989] that this method be used to provide low close to carrier phase noise LO's at microwave frequencies. However it can only be successfully employed in conjunction with oscillators that are stable in resonator frequency and possess a low Q_L (<100). If a dielectric resonator is used with a loaded Q of 2000 in a 20GHz oscillator, then the locking bandwidth for a - 60 dBc signal would be 10kHz. This would therefore impose stringent temperature requirements on the oscillator. If the injected signal is an impulse, such as from a Step Recovery Diode (SRD), then any increase in injected power will result in unwanted sidebands on the oscillator at the SRD drive frequency due to limited stopband attenuation of the resonator.

Injection locking must still be considered, however, to be an undesirable phenomenon when phase locked VCO's are employed [Underhill, 1986b]. VCOs are usually low Q circuits, and are therefore more susceptible to injection locking. The "brute force" approach would be to exclude any signals from the oscillator which are capable of injection locking the VCO. This may prove costly to implement and a more satisfactory solution would be to model the effect of contention between the injection locking and phase locking systems. An extension has been added to the Pascal PLL simulation described in §5.5.5 to enable modelling of the injection locking effect.

5.6.3 Model of injection locking of oscillator

A simplified model of the injection locked oscillator is used for the study of the behaviour within a phase locked loop. By reference to fig 5.29, the injected signal provides the extra phase shift through the resonator that occurs due to rotation of the oscillator phase vector. The angle of the injected signal to the oscillator signal is therefore given by θ where:-

$$\theta = \arcsin\left(\frac{f_m}{f_L}\right) \tag{5.43}$$

where f_m is the offset from the nominal oscillator frequency, and f_L is the injection locking bandwidth [Kurokawa, 1976], [Hines, 1968].

Within the injection locking bandwidth, the phase noise power of the free running local oscillator is multiplied [Farr, 1986] by a factor:-

$$\phi_{lo(locked)} = \phi_{lo(free)}\left(\frac{1}{1+\left(\frac{f_m}{f_L}\right)^2}\right) \tag{5.44}$$

where f_L is the injection locking bandwidth and f_m is the offset from carrier frequency. The local oscillator power is reduced by 6dB per octave reduction (power of 2) in frequency below the locking bandwidth as in the case for a first order loop. Since most oscillator phase noise increases at 9dB/octave reduction in offset frequency close to carrier, then there should be an increase of 3dB per octave reduction in frequency. This agrees with measurements taken by Farr [1986].

This first order characteristic was included in the simulation program. The behaviour of the VCO on locking is different from PLLs due to the non-monotonicity of the oscillator signals. However this effect is not taken into account in the simulation. A block diagram of the simulated system is displayed in fig 5.30. A third order type two phase locked loop designed for minimum locking time is used in the simulation. Adding the injection locking produces some interesting results. The worst case occurs when the injection angle is 180° out of phase with the phase locking angle. Simulation shows that if the injection locking bandwidth exceeded the phase locking bandwidth, a contention oscillation results in phase transitions that could resemble data; such transitions would result in a high BER in an operating data receiving system. If sufficiently irregular, these transitions may not be observable on a spectrum analyser, making tracing of the problem difficult. In less severe cases of injection locking, the loop parameters of the synthesiser are modified.

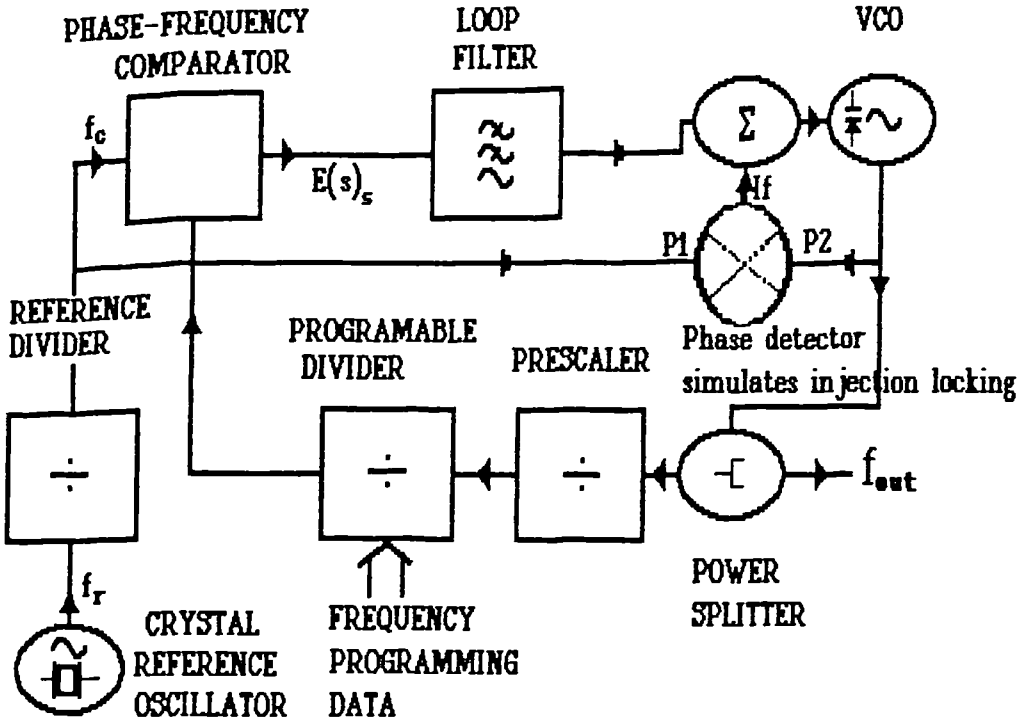


Fig 5.30 Block diagram of simulated phase lock loop with injection lock

Results of the author's simulation are given in fig5.31 showing the effect of changing phase locked loop gain with an injection locked PLL and with no injection locking. As the value of loop gain moves away from the ideal in the simulation, the settling time degrades more rapidly with injection locking than it would without injection locking.
The loop becomes unstable with lower values of loop gain, in comparison with the non injection locked case which is unconditionally stable for low gain values. Margins of stability are therefore reduced. This problem could occur whenever a phase locked loop is used within a synthesiser, particularly when phase locking to a comb generator. A minimum value of isolation is required after the VCO to provide sufficient attenuation of any potentially injection locking signals that may be present at the output, for example due to EMI induced spurious signals, or harmonics of a comb generator or divider chain.

The phase locked loop is one of a number of methods of frequency multiplication. Having discussed phase locked loops a comparison with these other methods will now follow.

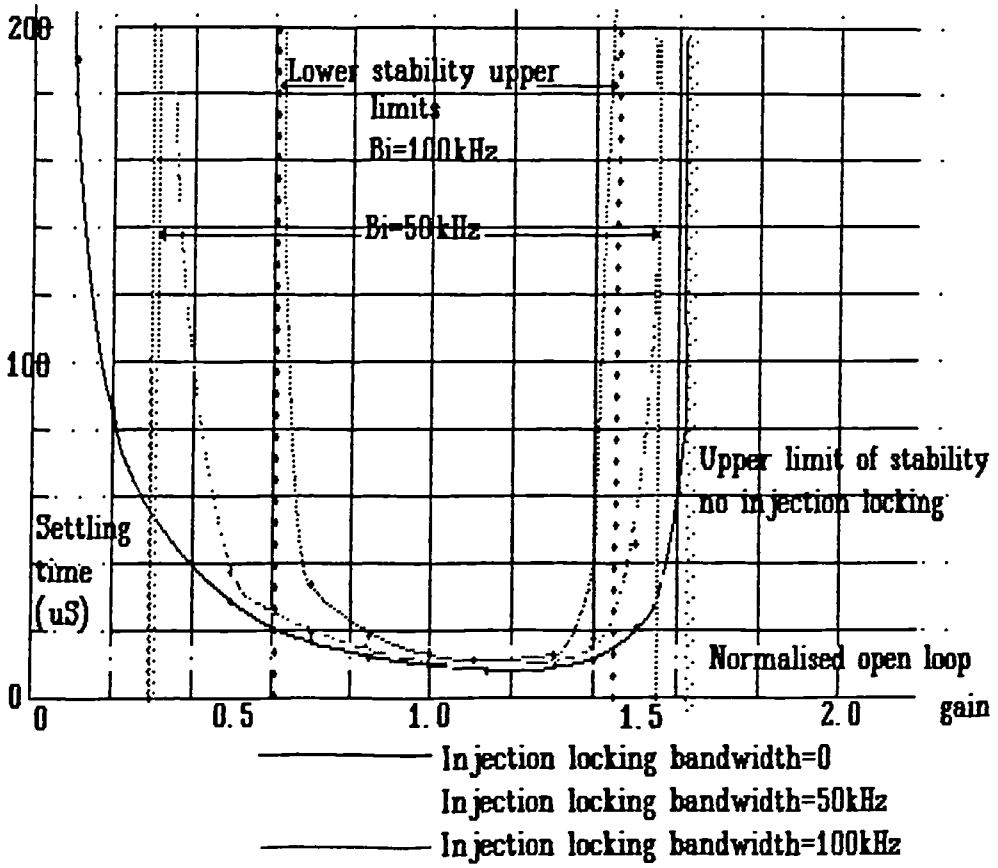


Fig 5.31 Influence of VCO injection locking upon PLL settling time

5.7 Phase noise in Frequency multipliers

5.7.1 Introduction

In order to operate at high frequencies eg.around 30GHz, then some form of frequency multiplication must be employed. There are many methods of frequency multiplication, with different levels of implementation difficulties and phase noise levels. One such example, the SRD multiplier, is further dealt with in chapter 7.

5.7.2 Phase noise of dividers and phase detectors

5.7.2.1 Divide by N loop

In order to compare the phase noise of various multiplication schemes it is necessary to evaluate the phase noise of the phase locked loop multiplier. Phase noise contributions of digital dividers and detectors were discussed in § 5.3.5. Such predictions must now be compared with measurements taken on actual loops.

5.7.2.2 Measurement of N loop synthesiser phase noise

Measurements were taken on a synthesiser based on the block diagram of fig 5.32 as part of a programme leading to the development of a Ku-band local oscillator. The VCO was a stripline L-Band oscillator, the output of which was to be fed to a frequency multiplier.

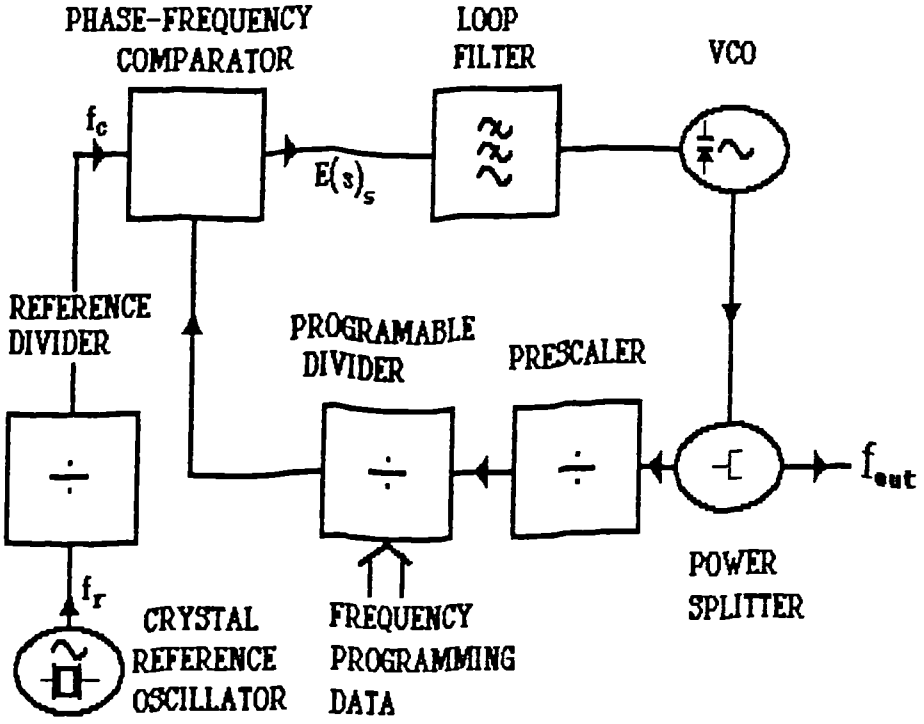


Fig 5.32 A ÷N PLL Synthesiser

Phase noise sidebands were measured on a spectrum analyser type HP8566B. Measurements on a spectrum analyser are acceptable if the source is stable and has noise sidebands significantly higher than the analyser local oscillator. Therefore this technique is acceptable since the synthesiser has a crystal oscillator as reference. Two types of loop filters were used, the charge pump type loop filter and a balanced linear op-amp filter. In addition phase noise measurements were performed on both the phase frequency detector and divider section of a CMOS MC145151 synthesiser IC and on a 74LS74 D type with a 74LS00 Nand gate in a minimum active gate synthesiser configuration. A Vectron type 217-6050 crystal oscillator is used as a reference source for these measurements; the phase noise contribution of this oscillator is at least 20dB below any of the authors' measurements on the synthesiser. Reference phase comparison frequencies were set by the programmable reference divider, and the output frequency changed by means of the programmable VCO dividers. For comparison purposes, an ECL divide by 2 was used to drive an SRD at 50MHz and phase noise measurements obtained.

5.7.2.3 Results

Fig 5.33 displays the results of the phase noise measurements. All measurements were obtained at an offset from carrier frequency of 1 kHz and with a loop natural frequency of 10 kHz.

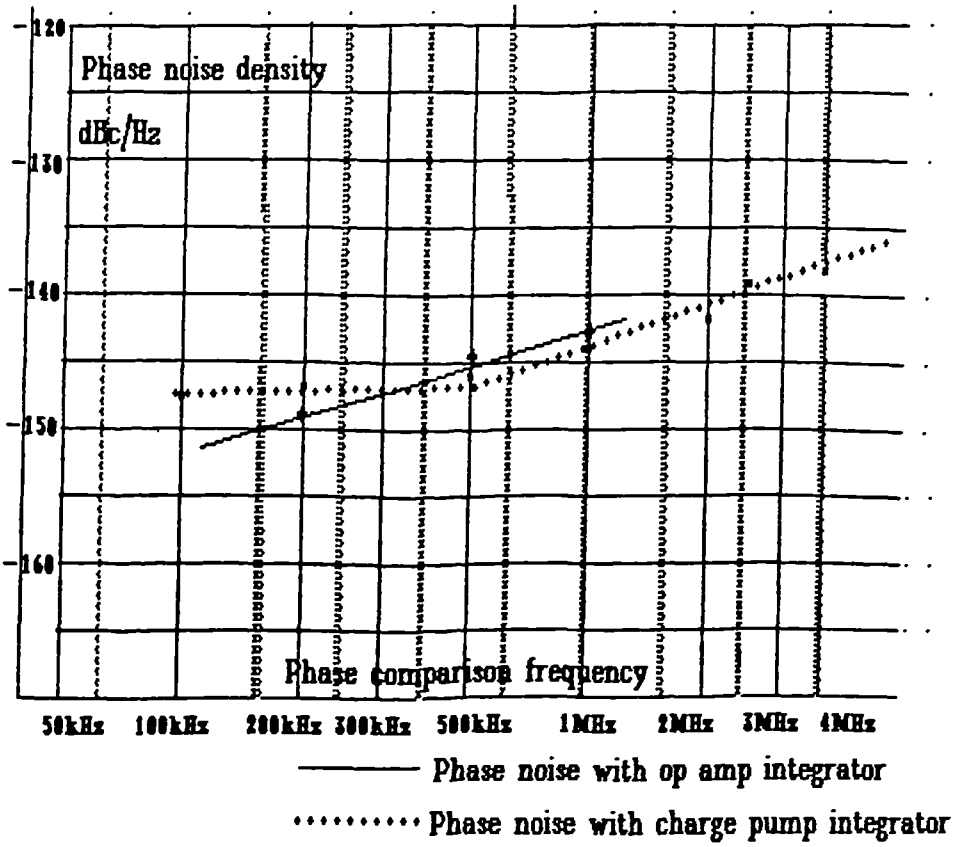


Fig 5.33 Phase noise of a ÷N PLL Synthesiser referred to the reference frequency

The dashed line indicates measurements taken with the CMOS MC145151 and a linear balanced filter using a low noise op amp type OP27GN. The dotted measurements were taken with LS TTL and a charge pump filter. The solid line indicates the LS synthesiser with the low noise op amp fitted. These measurements approximately conform to equation (5.45), apart from when the charge pump loop filter was used at low frequencies. With the latter loop filter, a high impedance is presented to the tuning varactor and this may increase phase noise levels.

5.7.2.4 Discussion of results

The divide by *N* loop synthesiser used in these measurements was shown in the block diagram of fig 5.32. Although this form of frequency multiplication is simple, we have measured significantly more phase noise at the output than with other methods. Using a 50 MHz step size harmonic sampling loop synthesiser controlling a 2GHz VCO, which in turn drives a SRD multiplier, the phase noise is plotted in fig 5.34. This includes noise from the SRD and ECL divider. Phase noise results for the LS TTL detector are excessive

for most communications work, and far in excess of that from the ECL divider/SRD combination.

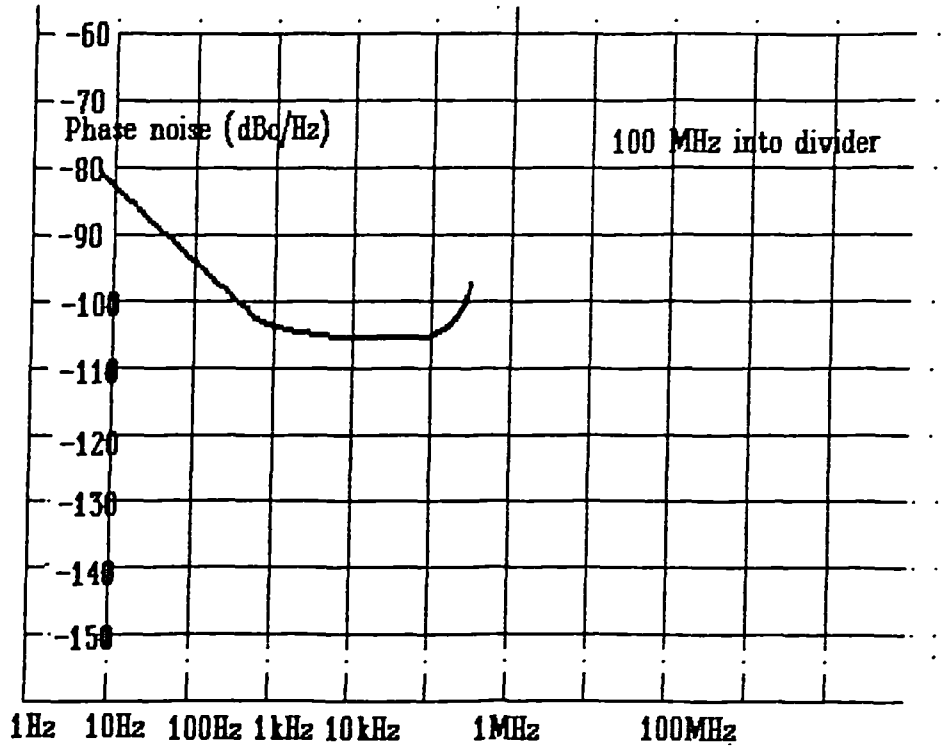


Fig 5.34 Phase noise of UPB581c ÷2 divider and SDI 101575-30 SRD.

However, at elevated temperatures (60°C) the divider/SRD combination phase deteriorated by 40dB and this problem is investigated further in chapter 7. The mechanism for phase noise generation is extremely complex in the case of the phase frequency divider and difficult to determine. There are many variables, and manufacturers of digital dividers, apart from certain producers of high speed devices, do not provide data on the phase jitter of their devices. Empirical rules can be applied to predict the level of noise floor obtained from a divide by *N* synthesiser using a dual flip-flop phase frequency detector in a minimum gate configuration. The phase detector noise floor measured by the author and normalised to 1Hz is as follows:-

Table 5.3

logic family	*Extrapolated phase noise 1 Hz intercept*
HCMOS	-200 dBc/Hz
LSTTL	-205 dBc/Hz
10K series ECL	-203 dBc/Hz
FAST TTL	-210 to -215 dBc/Hz

The phase noise can be estimated at the output of the synthesiser by means of the following formula [Wilson, 1988]:-

$$\mathcal{L}(f_{out}) = \mathcal{L}(f_{1Hz}) + 20 \log f_{out} - 10 \log f_{ref} \quad (5.45)$$

where $\mathcal{L}(f_{out})$ is the phase noise in dB at the output frequency, $\mathcal{L}(f_{1Hz})$ is the phase noise normalised to a reference frequency of 1 Hz, and f_{ref} is the reference frequency. This requires closer investigation and more work is required to study the effect of phase noise in this type of synthesiser. The phase noise performance of the latest high speed submicron HCMOS devices (eg. ACT) devices has not been evaluated. It is beyond the scope of this work to investigate this, but it could be recommended for further investigation. At frequencies close to carrier, flicker phase noise results in an increase in phase noise levels to above the figures predicted in equation (5.45). This equation indicates that the phase noise at the output of the synthesiser increases as the phase comparison frequency is decreased, therefore a problem of high phase noise is presented if a large multiplication ratio *N* is implemented.

5.7.3 Non reactive Multipliers

5.7.3.1 Schottky diode multipliers

A non-reactive multiplier is a multiplier which relies on the variation of the real part only of the device impedance with drive voltage; as opposed to a reactive multiplier which produces variations in the real and imaginary parts of that impedance. Examples of non-reactive multipliers are those using Schottky diodes or transistors.

Non reactive multipliers employ a fast switching device to provide the harmonic generation. Such a device can be either a diode or transistor. Transistors can also be used with the added advantage that gain can also be incorporated into the system [Faller, 1973]. Schottky diodes, however, have the reported ability [Scherer, 1981] to generate the lowest level of close to carrier phase noise, but have the disadvantage of generating only low order harmonics. Fig 5.35a displays a schematic of a doubler using Schottky diodes. The Fourier series expression for the voltage output of the doubler is:-

$$V = V_{pk}(2 - 4(\cos 2\omega_{ref}t + \cos 4\omega_{ref}t + \ldots..)) \quad (5.46)$$

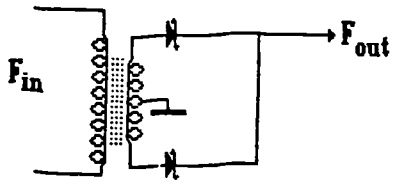


Fig 5.35a Schottky diode frequency doubler

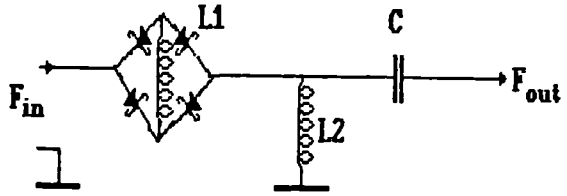


Fig 5.35b Schottky diode frequency tripler

One implementation of a Schottky diode tripler is a squarewave generator as in fig5.35b. Square waves possess a series of odd harmonics decreasing at a rate of $1/n$ (6dB/octave) against frequency. A plot of harmonic power against frequency is given for various frequency multipliers in fig5.36c. The tripler appears to give greater harmonic power than the SRD comb generator, but this is because the SRD comb generator power is spread over a larger number of harmonics. The tripler is also feasible as a harmonic generator, unlike the doubler where harmonic level falls approximately 12dB per octave.

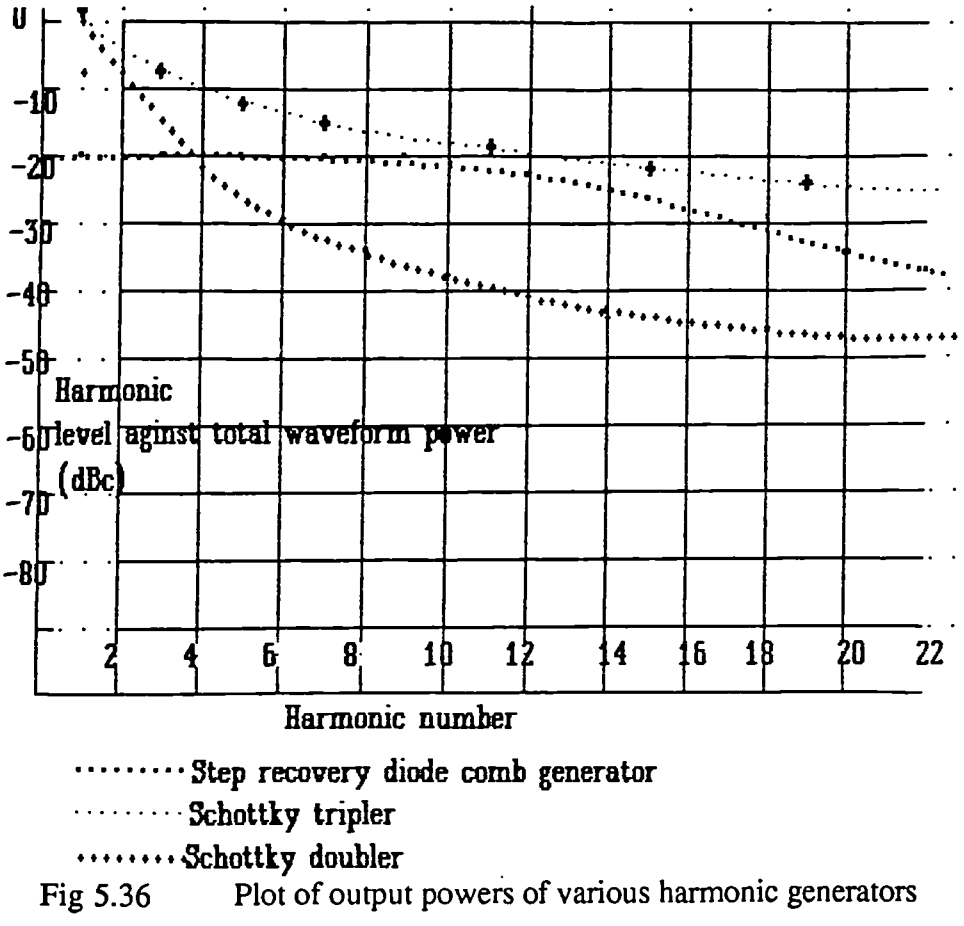


Fig 5.36 Plot of output powers of various harmonic generators

The advantage of Schottky diodes, is that the associated minority carrier recombination effects are negligible. Also the output phase is dependent upon the input phase rather than on a combination of input phase and amplitude as with reactive multipliers. Therefore AM to PM conversion is much lower with this type of multiplier. With Schottky diodes, $1/f$ noise generation is reported to be the lowest of any multiplication method [Wenzel, 1987].

In addition to this, special Schottky diodes can be purchased which possess a very low level of flicker noise. Since the real part of the impedance only is switched, parametric upconversion and oscillation effects are less troublesome. On the other hand, efficient simple high order multipliers may be best realised with SRDs, by virtue of their impulsive nature.

Fig 5.37 illustrates a phase noise plot obtained for Schottky diode multipliers by Wenzel.

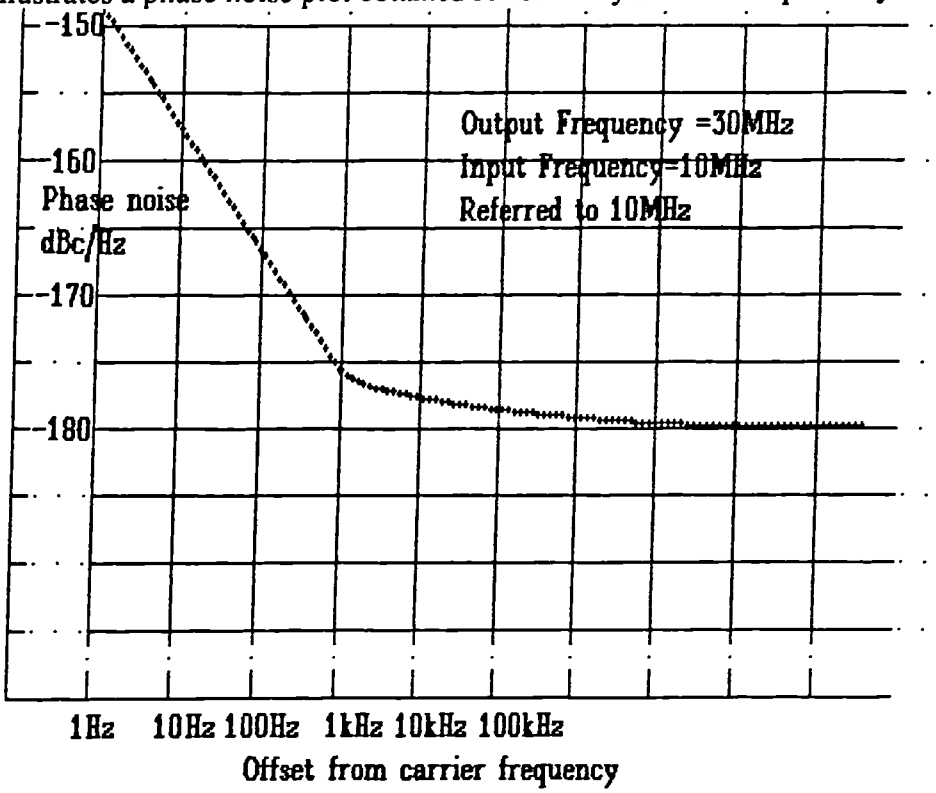


Fig 5.37 Measured phase noise plot of shottky diode multiplier at 10MHz from [Wenzel, 1987]

Care has to be taken, however with harmonic generators because of their EMI implications. When fast switching devices are used, such as Schottky diodes and SRDs, a broad spectrum of frequencies are generated, therefore these devices act as broadband EMI emitters, and such radiation must be contained. Particular hazards are: use with dividers which are broadband susceptors of EMI, and injection locking of oscillators. Use of comb generators is best therefore restricted to a section of circuitry where low phase noise is particularly critical, and the circuitry can be well isolated. An example of such an approach is given in §4.8.4.

5.7.3.2 Subharmonic mixers

There is a very important development of the non-reactive multiplier which can enable low phase noise synthesis to extend into the hundreds of GHz region. This is the subharmonic mixer. A Schottky diode multiplier is actually incorporated into a mixer

circuit, so the RF signal is mixed with a harmonic of the local oscillator signal (LO) [Carson, Schneider & McMaster, 1978]. The mixer diodes are arranged in anti parallel in order that the complete mixer characteristic is traced out twice per cycle. Mixing is therefore achieved at twice the harmonic drive frequency. Developments of this technique are allowing the use of frequencies of four times and greater of the local oscillator frequency. The same criteria apply to this form of mixer as to the Schottky multiplier in terms of excess phase noise.

5.7.4 Varactor multipliers

Varactor multipliers utilise the non-linear capacitance voltage relationship of the varactor diode. This results in waveform distortion and the subsequent generation of harmonics. The main non-linear generation is a second order process which means that harmonics other than the second are produced at a very low level. Therefore idler circuits are necessary to re-circulate the lower order harmonics and allow higher harmonic generation by mixing due to the device non-linearity. For example the third harmonic is created by multiplication of the second harmonic with the drive waveform. An idler resonance is necessary consisting of a series resonance at the second harmonic, in order to allow second harmonic current to flow through the diode. This idler can create additional problems due to parametric upconversion and oscillation. Also the idlers increase the number of adjustments and complicate the alignment procedure. For this reason, use of varactor multipliers tends to be restricted to doublers or when high power output multipliers are required. Work by McDade [1966] suggests that varactor multipliers may introduce lower phase noise than SRD multipliers due to the absence of recombination current.

5.7.5 Non-coherent frequency multiplication

All previous discussions are related to coherent multiplication, ie one reference source. However if more than one source is combined then interesting results follow.

§5.1 mentions that on multiplying up to microwave frequencies, the crystal oscillator phase noise is degraded by:-

$$20 \log \left(\frac{f_{out}}{f_{in}} \right) \quad \text{dB} \tag{5.47}$$

where f_{in} is the input frequency and f_{out} is the output frequency. The sinewave crystal reference source is raised to a power equivalent to the frequency multiplication ratio in order to produce the output frequency. This can be demonstrated by considering frequency doubling by squaring a signal (analogue multiplication by itself).

Input frequencies to the analogue multiplier can be represented as:-

$$V_1 = A\sin(\omega t + \alpha) \qquad V_2 = A\sin(\omega t + \beta) \tag{5.48}$$

where α and β are phase noise errors introduced by phase noise. Applying each source to an analogue multiplier results in:-

$$A\sin(\omega t + \alpha)\, A\sin(\omega t + \beta) = \frac{A^2}{2}\left(\cos(\alpha - \beta) - \cos(2\omega t + \alpha + \beta)\right) \tag{5.49}$$

If both inputs are from the same source (coherent multiplication) then $\beta = \alpha$ and therefore equation (5.49) becomes:-

$$A\sin^2(\omega t+\alpha) = \frac{1}{2}\left(1 - \cos(2\omega t + 2\alpha)\right) \tag{5.50}$$

Equation (5.50) suggests that the output frequency would be twice the input frequency and have twice the phase error superimposed on it. This accounts for the 6dB rise in phase noise in this case. If, however, the frequency multiplication is achieved from two uncorrelated sources, then the two inputs will be independent, therefore the phase error terms α and β in equation (5.49) would be uncorrelated. The combined effect of two uncorrelated phase errors would be their root sum of squares:-

$$\overline{\alpha + \beta} = \sqrt{\alpha^2 + \beta^2} \tag{5.51}$$

Phase errors will now be increased by 3dB rather than the 6dB increase for the single source case. Fig5.38 illustrates a method of frequency multiplication based upon this principle. A single source is fed to a 16 times frequency multiplier to obtain an output at 1.6 GHz in fig5.38a. In fig 5.38b, however, 16 sources are combined to provide the output frequency.

The sources are all phase locked together to a common reference with loops that have a narrow loop bandwidth compared to the offset from the carrier frequencies likely to be of importance in the application. This eliminates frequency errors from the system (apart from the master reference). The phase degradation of the 16 source method will be 12dB ($10\log\frac{f_{out}}{f_{in}}$) rather than 24dB with conventional multiplication. Therefore an improvement of 12dB can be made in the output phase noise performance. A problem with this method is that the complication of 16 reference oscillators forbids this technique for production equipment, but this may not be a problem for a reference local oscillator to test the production equipment. If the test equipment oscillator is 12dB lower in phase noise than the production equipment, then the error introduced will be approximately

0.3 dB rather than the 3dB expected from the conventional two source method. The figure of 0.3dB is a far more acceptable error margin for measurements.

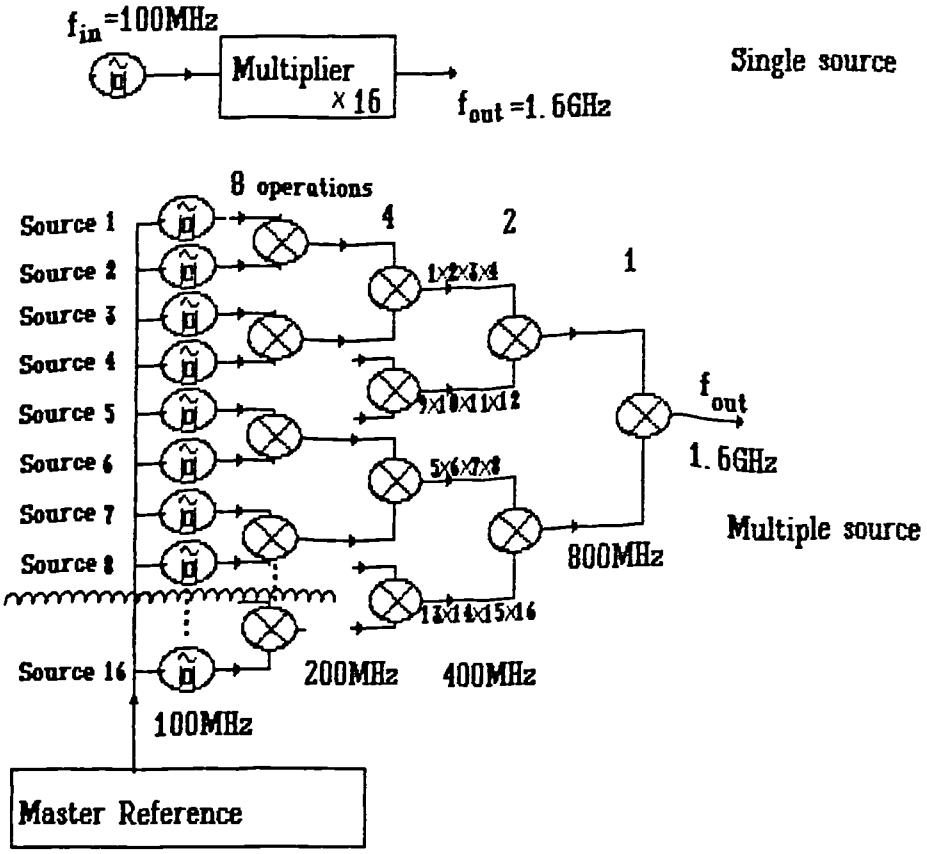


Fig 5.38 Coherent and incoherent forms of frequency multiplication

5.7.6 Summary of multiplier phase noise

Fig 5.39 gives plots of phase noise measured from different multiplier schemes given by various publications. The noise plots are normalised to 10GHz for comparison.

By far the worst contribution is from the Gallium arsenide phase frequency detector. The plot is taken from results published by Gavin & Hickling [1988] measured at a phase comparison frequency of 10MHz. Substantially better results are obtained from a 74F series phase comparator measured by the author. The phase comparison frequency was 5 MHz. This is clearly surpassed by phase locked oscillators based on SRD harmonic generators. Divide by *N* phase locked loops in general give poor phase noise performance in comparison with other methods. The SRD multiplier gives low phase noise if driven from a high frequency. Schottky diodes appear to deliver the lowest phase noise figures when driven from low frequency sources. Using non-coherent frequency multiplication results in still further reduction of phase noise, but at a cost of vastly increased complexity. Therefore this method is best reserved for phase noise measurement equipment.

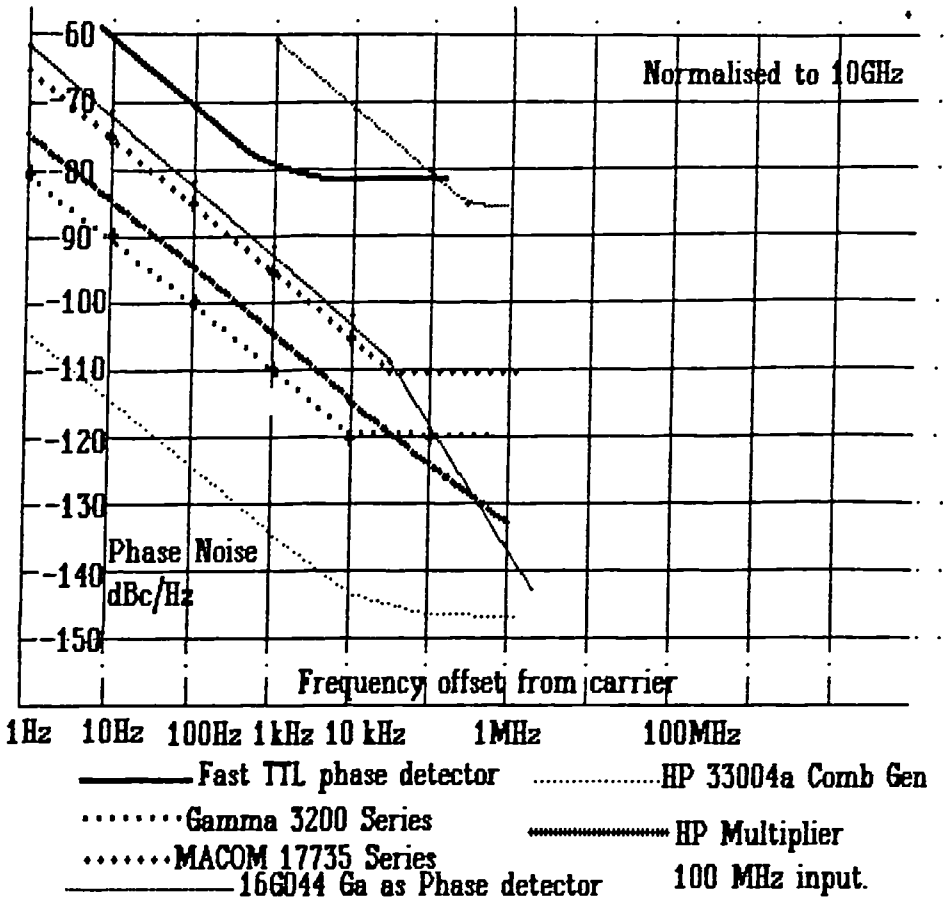


Fig 5.39 Phase noise of some comb gens, multipliers and phase locked oscillators

The preceding discussions refer to static phase noise, ie that generated within the local oscillator in perfectly still conditions. As much equipment will have to perform in high vibration environments, it is necessary to consider phase noise effects under dynamic conditions.

5.8. Dynamic phase noise (Vibration)

5.8.1 Methods of reducing the effects of vibration

Besides the consideration of static phase noise, the effect of vibration must be carefully considered as many applications for data transmission equipment operate in high vibration environments. Vibration tends to affect the phase noise of the synthesiser by changing the physical parameters of resonators used in oscillators and filters. Therefore, in indirect synthesisers, these effects are present in the reference oscillator and VCO's, and in direct synthesisers in the reference oscillators and filters.

Vibration in crystal oscillators is a vast subject in itself and as such is outside the scope of this work.

The effects of vibration are considered in the author's 3rd paper [Wilson & Tozer 1989]. The crystal oscillator reference should ideally be mounted in a vibration proof environment. The VCOs must be phase locked to the reference so that the loop gain is high enough to suppress vibration for all disturbance frequencies likely to be encountered. A second order or third order type 2 loop is normally used for phase locking in synthesisers. Possible approaches to the problem of vibration include:-

1) Use of a wide bandwidth loop;

2) Use of a third order type three loop [Tausworthy & Crow, 1972].

In a second order or third order type 2 loop with 2 poles at the open loop origin, the loop gain increases at 40dB per decade reduction in modulation frequency. If an extra pole can be added near the origin, to form a third order type 3 loop, this will increase to 60dB per decade. The result of this is a large increase in loop gain at low frequencies for an equivalent loop bandwidth. For static phase noise, little advantage would be gained for the extra complexity since the phase noise - frequency slope is rarely greater than f^{-4} (40dB per decade). However if high level vibrations are present at low offset from carrier frequencies, for example on a ship's deck, then the extra loop gain could be of benefit.

5.8.2 Loop gain compensation with third order type three PLL

In order to investigate this effect further, a computer simulation of a third order Tausworth-Crow Loop was carried out to assess the feasibility of using the loop in the presence of imperfect integrators (finite DC gains of op amps). The simulation described in §5.5.5 was modified to include an extra integrator in the loop filter.

A block diagram of the phase locked loop simulated is shown in fig5.40. The extra op amp is simulated by the second current source and loop filter components C3, C4 and R2. R3 and R4 are included to represent the finite loop gains of op amps.

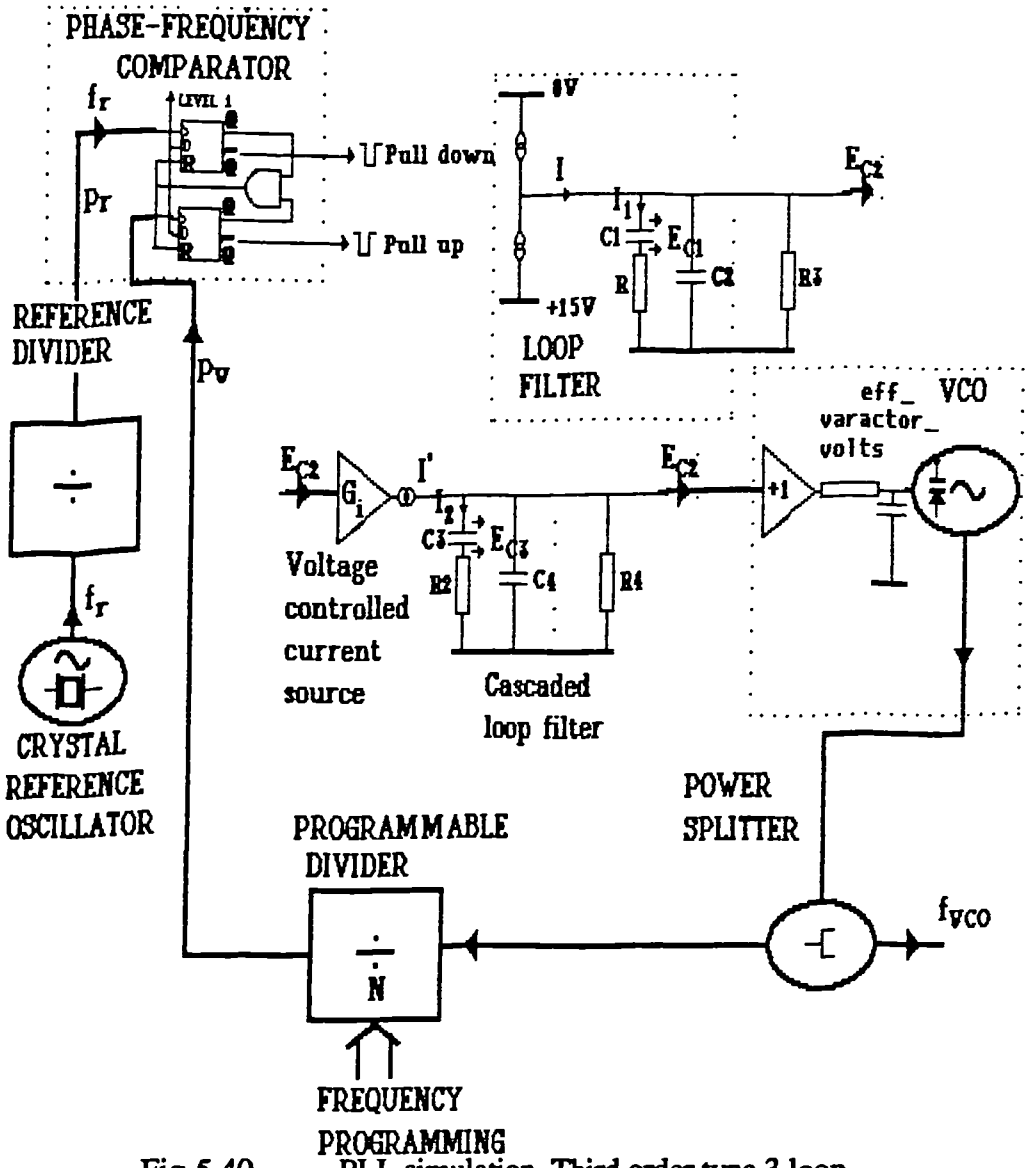


Fig 5.40 PLL simulation, Third order type 3 loop

Fig 5.41 displays the results of the computer simulation of a third order type two loop and fig 5.42 a third order type three loop written in order to predict the effects of vibration. To simulate oscillator microphonics, a 100Hz signal is used to modulate the oscillator frequency. In figs 5.41 and 5.42 the fine trace represents the oscillator resonator frequency deviation due to vibration, and the thick trace represents the phase deviation of the oscillator when locked.

In order to obtain the third order type three loop plot of fig 5.42, a modification to the above program is carried out to simulate the effect of adding an extra integrator stage to form the third order type three loop. Extra loop gain at the lower frequencies results in a lower level of spurious signals. Both loops had a phase detector reference frequency of 25 kHz.

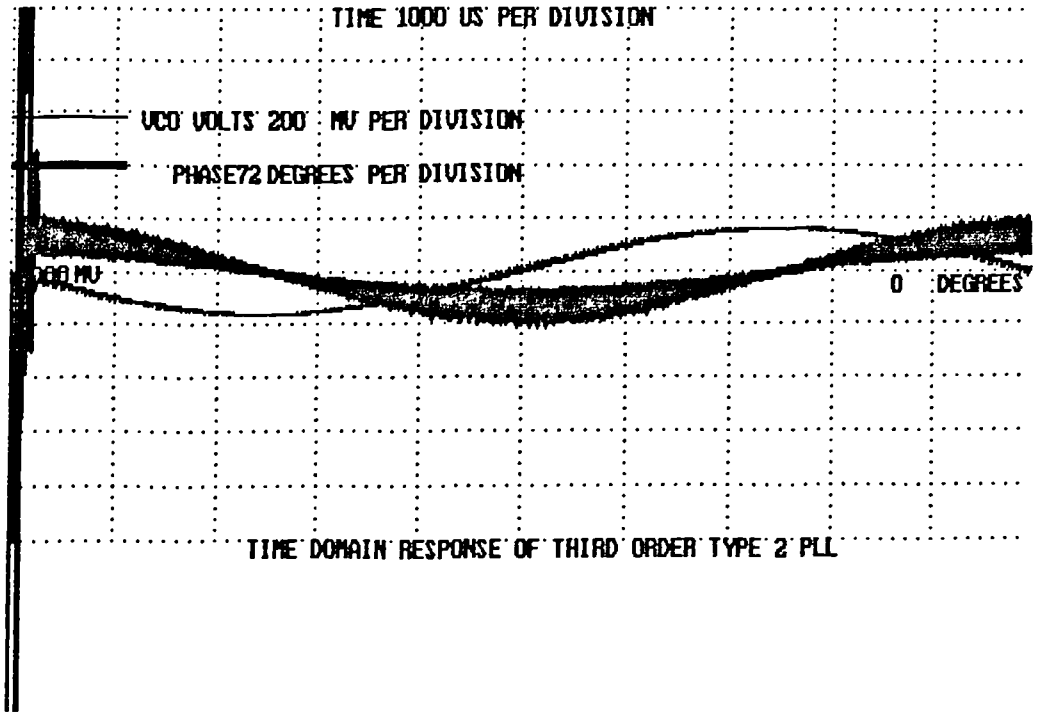


Fig 5.41 Simulated effect of vibration on a Third order type 2 loop

The output frequencies were 5 MHz and the uncorrected deviation of the oscillator was 200 kHz peak. An open loop Bode plot of such a loop indicates there is a point at low frequencies where the forward loop gain phase shift becomes greater than 180°. This means that the loop gain has a lower limit for stability besides the upper limit. Loop gain must be carefully controlled therefore. Limited benefit would be gained, however, if the synthesiser channel spacing were close, since this limits loop bandwidth. Its possible main application is in retro-fitting to synthesisers that have vibration problems since few additional components are required (1 op amp stage).

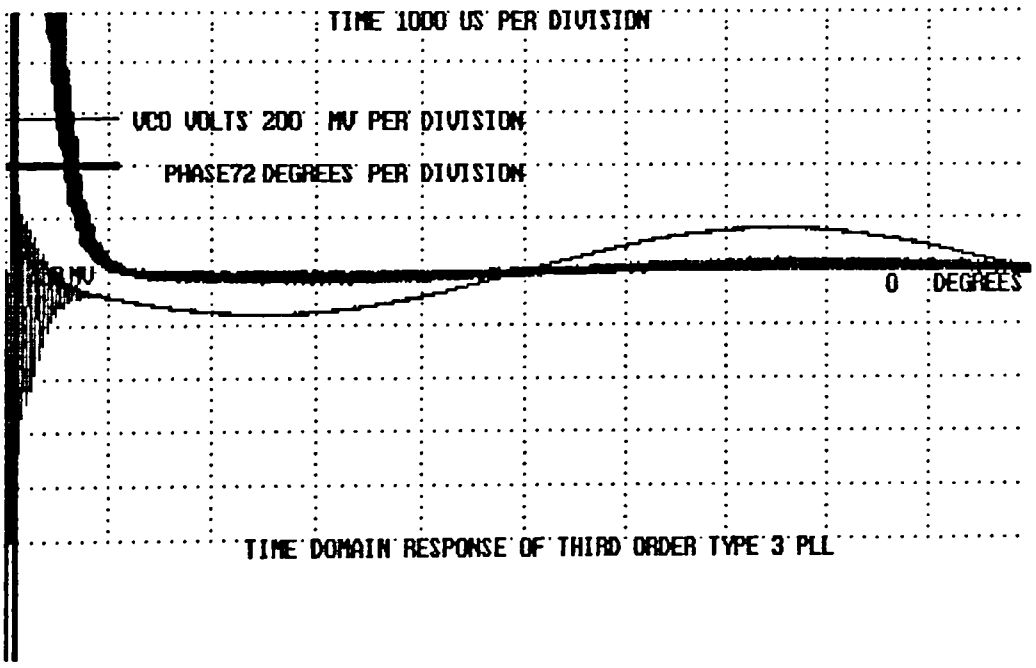


Fig 5.42 Simulated effect of vibration on a Third order type 3 loop

If close channel spacings are required, then it is inevitable that the required loop bandwidth will be greater than the channel spacing, and this involves the following options:-

1) Multiple loop synthesiser

2) Direct digital synthesiser

3) Fractional phase locked loop.

5.9 Conclusions

This chapter has addressed a number of key issues concerning the sources of noise within synthesisers.

Spurious signal problems have to be treated differently according to whether the synthesiser is a simple multiplier, or whether it is a fractional or combinational synthesiser. With a fractional or combinational synthesis scheme, spurious signals, once introduced are too close to the carrier to be easily removed.

It was suggested that the addition of limiters and digital dividers may act as broadband interference susceptors where broadband noise and spurious signals are folded down to around the carrier. Extra care needs to be taken whenever these devices are used to ensure they are not exposed to such broadband signals. Here we also show that phase noise power density introduced by digital devices is proportional to the toggling frequency.

There are many types of phase detectors which can be used in frequency synthesisers. The phase frequency detector is commonly used in PLLs because of its self acquisition properties. Linearity is a problem with this type of detector, and methods of overcoming this problem were discussed including layout and IC utilisation.

High phase noise is a problem with the phase frequency detector, but it has been shown that this can be reduced by adopting the two phase detector approach. In addition, the use of a microwave sampling detector enabled the linearity problem to be overcome, and is capable of operating at a higher microwave frequency than a variable modulus prescaler. A modification to the commonly used phase frequency detector has been suggested that would increase switching speeds and allow the use of higher loop bandwidths.

In the PLL transfer loop, as commonly used in multiple loop synthesisers, an ambiguity can occur if the oscillators to be locked together are close together in frequency. An image rejecting phase detector has been developed which rapidly rejects the ambiguous frequency locking condition. This configuration has been used to enable rapid locking in multiple loop synthesiser configurations.

Although phase locked loop synthesisers had a reputation of being slow, methods of speeding the locking and raising the loop bandwidth have been presented. There is a minimum settling time which can be obtained by selection of optimal loop filter component values. However, care must be taken as there is only a 3dB loop gain stability margin at the minimum settling time point. Commercial phase locked loop simulation programs for PLL synthesisers demonstrated shortcomings, therefore a phase locked loop simulation program was written by the author to enable study of locking times and the problem of injection locking. Simulation showed that phase and frequency locking can generally be achieved in a few reference periods with a phase frequency detector.

Simulation of PLLs was extended to include injection locking. The model of injection locking used was a simplified one but it demonstrated the effect of injection locking upon stability. Injection locking introduced a minimum loop gain for stability and reduced the maximum loop gain for stability. Reduced stability margins are a direct consequence of injection locking therefore. The spurious sensitivity of free running VCO's increases by 6 dB for each octave reduction in offset frequency below the loaded resonator half bandwidth. Extreme care must therefore be taken in the screening of low Q oscillators.

The issue of phase noise in frequency multipliers and dividers has been addressed and it emerged that a scarcity of available literature existed on the subject. It was discovered that analogue type multipliers could offer a much lower phase noise alternative to PLLs which use dividers. GaAs phase frequency comparators gave very poor phase noise especially close to carrier. Measurements were undertaken of phase noise in divide by N PLLs that use digital dividers.

The third order type three phase detector was shown to be advantageous in some cases for the suppression of dynamic phase noise arising from vibration. It was shown that it may be possible to retro-fit an existing synthesiser with an extra amplifier to give a third order type 3 response. Care must be taken to ensure that loop gain is kept within bounds for this type of loop. Benefits from such a modification are limited if the phase comparison frequency is low, and in this case an alternative synthesiser design must be considered.

Frequency multiplication is a critical part of microwave frequency synthesis. This chapter outlines various component design considerations necessary for good phase noise performance.

5.10 Further work

An investigation would be required of currently available synthesiser and phase detector integrated circuits that claim to have overcome the linearity problem. They should be evaluated for phase noise levels and reference spurious breakthrough. Samples of the latest generation of submicron CMOS logic need to be evaluated alongside other types of logic for phase noise levels. The subject of phase noise generated by digital logic in general requires more work, to determine whether present divider and phase detector technology could be improved. One suggestion would be the provision of special resynchronisation circuits driven from the device clock input that are optimised for low phase noise. This chapter covered the problem of frequency independent phase noise in

divider and phase detector circuits. However benefits could be gained from investigating the effects of 1/f noise in dividers and limiters.

Many different configurations of analogue mixer are possible. Measurements would be required to ascertain their high order spurious performance. In particular, the spurious performance of passive mixers could be compared with that of active mixers.

The two phase detector approach requires more refinement to obtain a fast switch over between the phase detectors.

Injection modeling involved extensive simplifications and consequently the results obtained were only valid when the PLL was within its linear region. Improvements are therefore required to the injection locking model to include non linear effects in the simulation.

5.11 References

Aein, J.M. December 1973 Multiple access to a hard limiting satellite repeater. *IEE Transactions on Space electronics and telemetry.* p. 159.

Apte, D.R & Cummings, T.J. March 1990 Designing with high frequency prescalers. *R F Design.* p. 47-52.

Badger, D. 1988 Improved Accuracy for Transient Analysis. *RF Expo, Proceedings.* pp. 147-156.

Bain, R. May 1989 A Mixer Spurious Plotting Program. *RF Design* p. 32.

Baker, D. A July 1989 Reference cancelling Phase frequency Detector. *RF Design.* p. 35.

Blake, J. May 1988 Design of wideband frequency synthesisers. *RF Design.* p. 26

Carson, E.R, Schneider, M.V. & McMaster, T.F 1978 Subharmonically pumped millimeter wave mixers. *IEEE Trans, MTT.* Vol MTT-26. No 10. pp706-715

Cheah, J.Y.C., April 1991 Parasitic Positive Frequency Aquisition in a PLL. *RF Design.* p. 69-76.

Connell, P.P.R. 1987 Phase detectors in wideband phase locked loops. *1st international conference on frequency control and synthesis. Universiy of Surrey*

Crawford, J. Feb 1985 The Phase/ frequency Detector. *RF Design.* pp. 46-57.

Davenport, W.B. Jr. June 1953 Signal to noise ratios in Bandpass limiters. *Journal of Applied Physics.* p. 720

Dixon, R.C. 1976 Spread spectrum systems. chap. 2, p. 31. NY: Wiley.

Egan, W. & Clark, E. June 7 1978 Test Your charge pump phase detectors. *Electronic Design.* vol. 26, p. 134.

Egan, W. Feb 1991 Sampling Delay, Is it real? *RF Design.* p. 114.

Egan,W. March/April 1984 Letter to the editor. *RF Design* pp. 9A, 12A

Faller, H December 1973 Try a transistor in your next frequency multiplier. *Microwaves* p. 48.

Farr, A.N. January 1986 Injection locking for ultra low noise UHF and Microwave sources. *IEE Colloquium digest Low noise Oscillators and Synthesisers.* p. 1/1.

Farr, A.N. January 1986 Injection locking for ultra low noise UHF and Microwave sources. *IEE Colloquium digest Low noise Oscillators and Synthesisers.* p. 1/5.

Gavin, D.T & Hickling, R.M. July 1988. PLL Synthesiser phase locks with GaAs Comparator. *Microwaves & R.F.*

Goldman, S. March,April, 1984 Divider delay, the missing PLL analysis ingredient. *RF Design* pp. 58a-66a.

Gorski-Popiel,J 1979 *Frequency Synthesis Techniques,* chap. 2. p. 37. Wiley.

Grebenkemper, C.J. 1982 Tutorial on phase noise. In *Application Notes* (ed. Watkins & Johnson), p. 5.

Grove, W.M. 1967 A DC to 12.4 GHz Feedthrough Sampler for Oscilloscopes and other RF Systems. *Hewlett Packard Technical Review.* p. 12

Harris, M.V. 19 November 1991 A J-Band spread spectrum synthesiser using a combination of DDS and phaselock techniques. *IEE colloquium digest, Direct digital synthesis.*

Harris, M.V. 1989 An investigation into the frequency settling time and post tuning drift of broadband microwave varactor tuned oscillators. *IEE conference on frequency control and synthesis publication 303 Leicester* p. 97.

Hatcher, S. October 1989 Modelling PLL Tracking of Noisy Signals. *RF Design* p. 113.

Hatchett, J. Oct 25, 1978 A few more points. *(letters) Electronic Design.*

Hines, M.E, Collinett, J-C.R & Ondria, J.G. Sept 1968 FM noise suppression of an injection phase locked oscillator. *IEEE Trans MTT.* Vol. MTT-16, No. 9, pp. 738-742.

Jones, J. 1986 *Modern Communications Circuits,* chap. 9, p. 353. McGraw-Hill.

Kuo, F. *Network analysis and synthesis.* chap.13, p. 407. Wiley

Kurokawa, K. 1976 Microwave solid state oscillator circuits. In *Microwave Devices,* (ed. M.J. Howes & D.V. Morgan) - chap. 5, p. 225.Wiley NY

Kurokawa, K. July-August 1969 Some basic characteristics of broadband negative resistance oscillator circuits. *The Bell System Technical Journal.* p. 1941.

Lee, B.S., Hardstone, J. & Wilson, M P. 1991 Phase locked loop oscillator control circuit. *GB patent application no 9113682.0.*

Lucas, J.P. et al. 1989 A 20GHz Injection Locked Dielectric Resonator Oscillator. *IEE Conference publication 303 Frequency control and synthesis.* p. 62

Manassewitsch, V 1985a *Frequency synthesis, theory and design.* chap. 2 p. 58

Manassewitsch, V 1985b, ibid chap. 3, p. 164.

McDade, J.C. Feb 1966 Measurement of Additive Phase Noise Contributed by the Step Recovery Diode in a Frequency Multiplier. *Proceedings of the IEEE.* p. 292 294.

McGillen, C. & Cooper, G.R. 1986 *Continuous and discrete signal and systems and system analysis,* chap. 5 p. 244. CBS International Edition.

Metellics 1989 *Metellics phase detector type* (DATA SHEET) MSDP1020-E50

Przedpelski, A.B. July/August 1983 PLL Primer, Part 3. *R.F. Design.* pp. 48-58

Robins, W. 1982a *Phase noise in signal sources.* chap. 7. p. 100. Peter Perigrinus

Robins, W. 1982b *ibid.* chap. 7, p. 123.

Rohde, U. 1983a *Digital PLL Frequency Synthesisers, Theory and Design.* chap. 4, p. 204. Prentice Hall, NJ.

Rohde, U. 1983d ibid. chap. A2, p. 408.

Rohde, U. 1985b, ibid. chap A-1. p. 381.

Rohde, U. 1985c, ibid. chap 4. p. 277.

Scherer, D. 1981 Generation of low phase noise microwave signals. *Hewlett Packard RF and Microwave simposium and exibition notes*. p. 20.

Stirling, R. 1987 *Microwave frequency synthesizers,* chap. 8, p. 77. Prentice Hall

Tausworthe, R.C & Crow, R.B 1972 Improvements in deep space tracking by the use of Third order loops. *ITC72 Conference record* pp577-583

Underhill, M. June 1980 Wide range frequncy synthesisers with improved dynamic performance. *The radio and electronic engineer.* Vol. 50, No. 6, pp. 291-296.

Underhill, Prof. M.J. 1986a Frequency synthesers and standards. In *Radio Receivers.* (ed. Gosling), Chap. 4. p. 80 W. Peter Peregrinus

Underhill, Prof. M.J. 1986b ibid. p. 100.

Underhill, Prof. M.J. 1989 Fundamental limitations of oscillator performance. *IEE Conference publication 303 Frequency control and synthesis*. p. 21.

Utsi, P.A.V. March 1983 Phase noise in digital plls due to detectors and dividers. *Proceedings "IEE Conf on Land Mobile Radio" Leeds.*

Watkins and Johnson 1989 *Mixer catalogue,* Catalogue. p. 37

Wenzel, C. July 1987 New topology multiplier generates odd harmonics. *RF Design.* p. 32

Wilson, M.P & Tozer, T.C. October 1989 The effect of Local Oscillator Phase Noise in Low Data-Rate Satellite Receivers. *IEE Colloquium Digest no 1989/114, Modems and Codecs for Satellite Communications", London.* p. 4/1

Wilson, M.P. & Tozer, T.C. October 1989 The effect of local oscillator phase noise in low data rate satellite receivers. *IEE Colloquium digest* 1989/114. *Modems and Codecs for Satellite Communications, London.*

Wilson, M.P. 9th May 1988 Low cost synthesised sources for VSAT frequency converter applications. *IEE colloquium on Microwave components in telecommunications, London.*

Wong, J.S 1988 A Computer aided frequency multiplier design. *Proceedings RF Expo*

6 *Effect of phase noise upon system performance*

6.1 Introduction

This chapter examines the effect of synthesised local oscillator phase noise upon practical systems. Satellite data communications systems are analysed in terms of phase noise, data rate and modulation schemes, culminating in the development of the concept of a link budget for phase noise. Chapter 9 continues this by calculating the phase noise link budget for various local oscillator and system configurations. The emphasis here is upon coherent modulation schemes, in particular BPSK and QPSK.

Local oscillator performance is a vital factor in digital communications systems especially as frequencies of over 30GHz are increasingly being used. Any loss in sensitivity of the receiver, even of fractions of a dB, must be made up by increasing the power of the satellite transponder, or the size of antennas, both of which are expensive measures. Although modulation and coding schemes result in coding gains which reduce receiver demands on link budgets, such gains could be compromised if due consideration is not given to local oscillator design. This applies not only to the receiver, but throughout the link. Therefore it is necessary to assess the likely effect of the parameters of synthesised local oscillator upon bit error rate (BER) performance. The local oscillators that must be considered are all the local oscillators in the system, and this is undertaken by analysis of the effect on the demodulator of oscillator phase noise.

As an example, although the local oscillators used in domestic TVRO downconverters are very inexpensive owing to mass production, their use in some data links may have such an adverse effect upon the link budget that the system is unworkable. Even if the link performance is viable, the margins to other forms of interference may be impaired. TVRO downconverters however tend to employ a free running dielectric resonator oscillator

(DRO), possessing poor close to carrier phase noise that will excessively degrade demodulator performance. A plot of the phase noise sidebands of a typical DRO in comparison with multiplied crystal oscillators is displayed in fig6.1. It will be shown later that such hardware can be quite unsuitable for use in data communications at low bit rates, and with correspondingly low C/N_o.

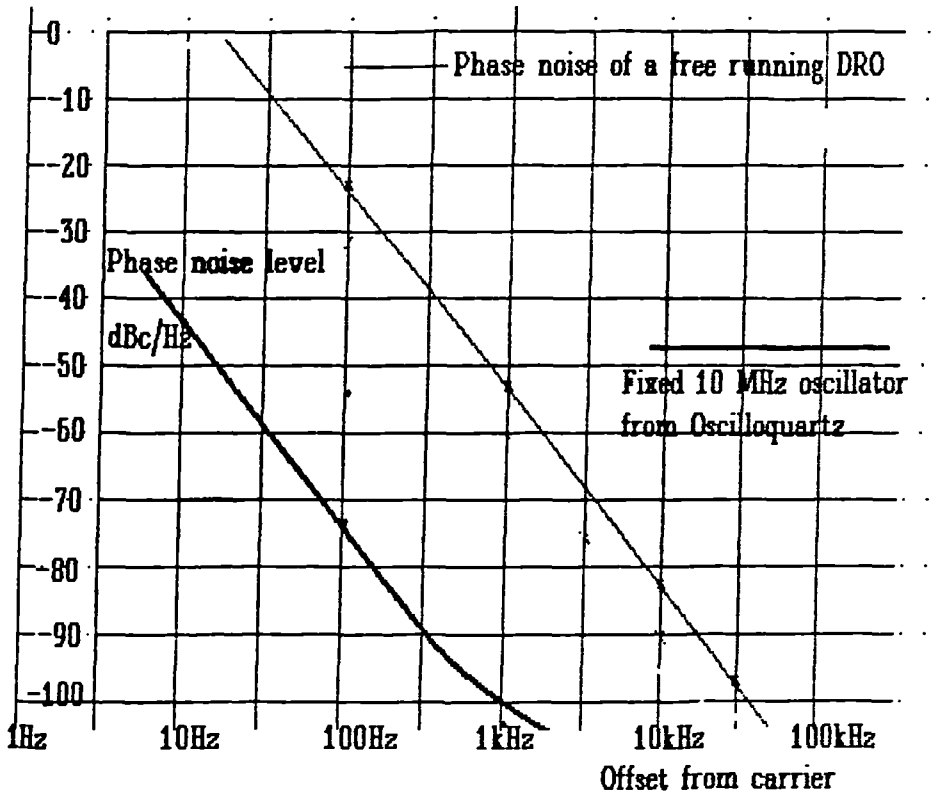


Fig 6.1 Comparison of multiplied crystal oscillator phase noise, and free running DRO phase noise

Analysis is undertaken for a variety of synthesised local oscillator configurations in order to determine the optimum combination for a particular application. In addition to the analysis, the performance of a trial modem and satellite link built for link budget analysis will be considered.

6.2 Analysis of Coherent Phase Shift Keying

6.2.1 In the presence of a perfect recovered carrier

Analysis of the performance of a data demodulator in the presence of thermal and phase noise can be very involved, especially when coding techniques are employed. Therefore, the case of straightforward binary phase shift keying (BPSK) will be initially considered.

A perfect recovered carrier is assumed in the first instance, and this situation is well covered in the literature [Betts, 1983]. Calculations are performed in terms of the energy per bit to noise-density ratio, E_b/N_o. E_b is the signal power divided by the bit rate and has units of watts/Hz. (In coded systems it is important to distinguish between the information energy per bit E_i and system link energy per bit E_s: the former is derived using the bit rate at system I/O (input output) whereas the latter is derived from the bit rate over the link. The ratio of the two depends upon the symbol or coding rate). As described in chapter 3 of this thesis, a bit error occurs when the noise perturbation causes the decision threshold to be crossed to give an output error. Fig6.2 shows the effect of noise causing the decision thresholds to be crossed for a quadrature phase shift keyed (QPSK) signal.

In the presence of additive thermal noise, the noise spreads the actual constellation points around the ideal constellation points (Fig6.2 a) in a circular fashion. The probability of crossing the threshold gives the error rate P_{eo}, assuming matched filtering, as [Bhargava, 1981a]:-

$$P_{eo} = \frac{1}{2}\left(\text{erfc}\sqrt{\left(\frac{E_b}{N_o}\right)}\right) \qquad (6.1)$$

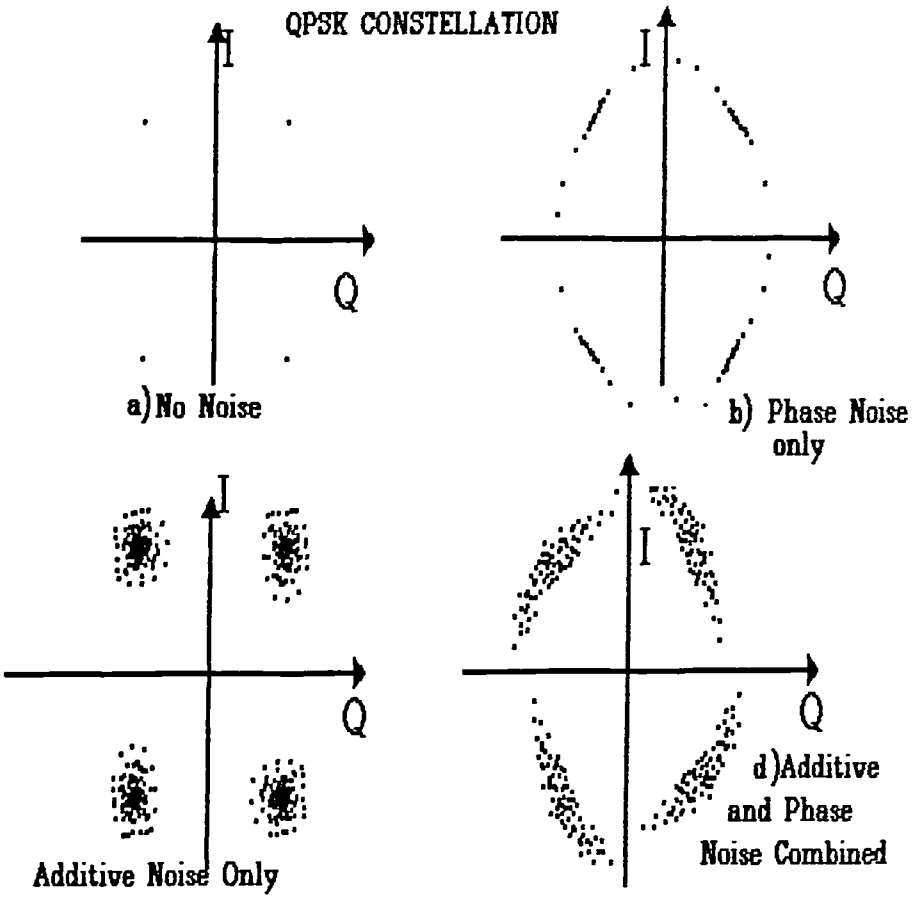


Fig 6.2 Effect of noise on signal constellations

The curve displayed in the extreme left of fig 6.3 shows the case with no carrier jitter, and assumes that perfect carrier recovery takes place. However, in a practical demodulator, the following will occur:-

1) Static phase error, ϕ_o, due to phase shifts in filters, amplifiers and offsets in phase detectors;

2) Residual thermal noise on the recovered carrier, ϕ_t;

3) Local oscillator phase noise on recovered carrier, ϕ_p.

As can be seen for the curves displayed in figs 6.3 and 6.4, any coding gain is rapidly lost if carrier recovery loop (CRL) phase errors are present. It is therefore necessary to look at the performance of a CRL in some detail.

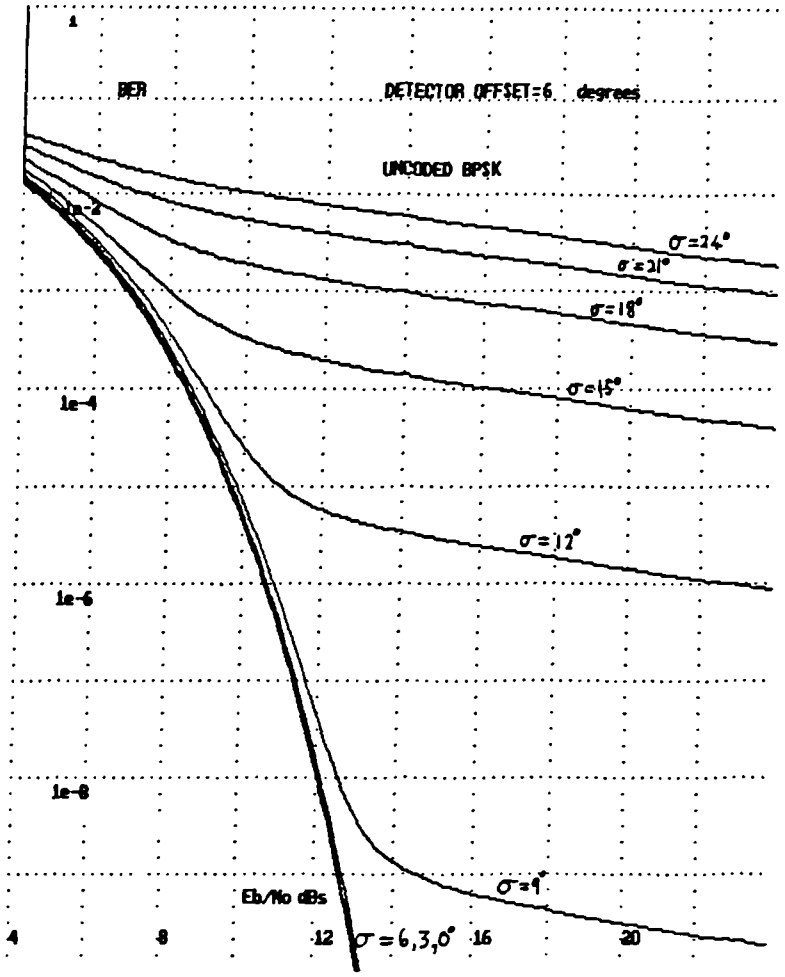


Fig 6.3 BER-E_b/N_o plot for uncoded BPSK in the presence of an imperfect recovered carrier

These curves are produced from a computer program written by the author, which performs calculations of equation 6.7 in §6.2.3. This program is incorporated into the phase noise analysis program discussed in chapter 9.

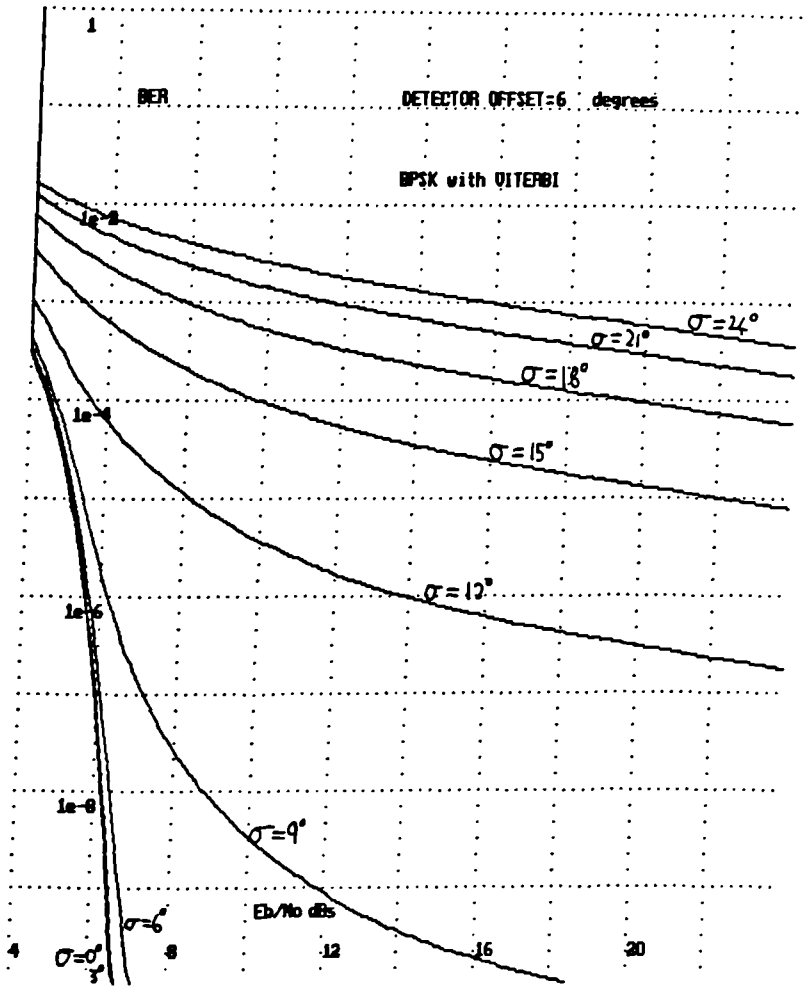


Fig 6.4 BER-E_b/N_o plot for Viterbi BPSK in the presence of an imperfect recovered carrier

6.2.2 Effect of a fixed carrier phase offset

The effect of a fixed carrier offset is an effective reduction in the E_b/N_o at the demodulator. The carrier offset at the demodulator is represented by θ. The demodulated waveform is:-

$$\sqrt{P}\sin\theta\, d(t) \tag{6.2}$$

where d(t) is the modulation that can have values of ± 1. In the case of a fixed recovered carrier offset, θ_o the recovered signal effective $\frac{E_b}{N_{oeff}}$ becomes:-

$$\frac{E_b}{N_{oeff}} = \frac{E_b}{N_o} \sin^2\theta \qquad (6.3)$$

It is desirable, therefore, to minimise the offset in order to maximise E_b/N_{oeff}. A major source of the static phase offset is the phase shift through the pre-squarer filter.

6.2.3 The effect of a time variant carrier phase offset

In the analysis performed by Holmes [1982a] the phase noise is considered to be a time variant offset. This results in a mean offset of θ_o with a phase noise offset of $\phi(t)$ added, so that:-

$$\varepsilon(t) = \theta_o + \phi(t) \qquad (6.4)$$

where $\varepsilon(t)$ is the instantaneous phase offset.

In order to calculate the bit error rate of the system with phase noise, it is necessary to evaluate the following over all possible values of phase error:-

$$P_e = \frac{1}{2}\text{erfc}\sqrt{\frac{E_b}{N_o}\cos^2\varepsilon} \qquad (6.5)$$

Or alternatively:-

$$P_e = Q\sqrt{\frac{2E_b}{n_o}\cos^2\varepsilon} \qquad (6.6)$$

The average bit error rate can be found from the integral:-

$$BER = \int_{-\pi}^{\pi} P_e(\phi)\, P(\phi).d\phi \qquad (6.7)$$

where $P(\phi)$ is the probability density function of the phase error [Bhargava, 1981b]. From the above this integral becomes:-

$$BER = \int_{-\pi}^{\pi} \frac{1}{2}\text{erfc}\sqrt{\frac{E_b}{n_o}\cos^2(\theta_o + \phi(t))}\, P(\phi).d\phi \qquad (6.8)$$

There is a possible source of error here in that for finite θ_o there is a small probability of $\theta_o + \phi(t)$ exceeding $\pm\pi$, whereupon the BER will erroneously appear to fall again. However this effect should not contribute to erroneous results for usable values of phase noise. The analysis presented here assumes that the phase noise is close to carrier [Holmes, J.K.1982b] and does not significantly change over one data bit period.

However some synthesisers can have significant phase noise at the data rate. In this case the noise offset should be averaged over one cycle so that the expression (6.8) becomes:-

$$Pe = \frac{1}{2}\,\mathrm{erfc}\sqrt{\frac{E_b}{N_o}\,\overline{\cos^2\varepsilon}} \tag{6.9}$$

where $\overline{\cos^2\varepsilon}$ is the mean value of $\cos^2\varepsilon$ over one symbol period.

6.2.4 Probability density function of phase offset due to phase noise

In order to evaluate the above integral (equation 6.7), it is necessary to provide results for $P(\phi)$, the probability density of there being a phase offset of ϕ due to phase noise. Viterbi [1963] analyses the tracking performance of a second order carrier recovery loop in the presence of phase noise by application of Fokker Planck techniques. These techniques are devised to allow prediction of system behaviour when the input is randomly variable. They are therefore suitable for phase locked loop analysis when the signal to noise ratio is too small for linear analysis. By application of the Fokker plank techniques the probability density function can be shown to be:-

$$P(\phi) = \frac{\exp(\alpha' \cos\phi)}{2\pi I_o(\alpha')} \tag{6.10}$$

where α is the signal to noise ratio in the loop bandwidth given by:-

$$\alpha = \frac{A^2}{n_o B_L} \tag{6.11}$$

and A/n_o is the signal to noise density ratio and BL is the loop bandwidth. Equation (6.10) is the Tikhonov probability distribution and is the Gaussian distribution modified for angular systems. For a second order loop [Gardner, 1979a]:-

$$\int_0^\infty |H(s)|^2.df = \omega_n\left(\zeta + \frac{1}{4\zeta}\right) \tag{6.12}$$

For a reasonably large α (say >5) then α can be approximated as:-

$$\alpha = \frac{1}{\sigma_\phi^2} \tag{6.13}$$

Where σ_ϕ^2 is the phase error variance.

One problem is that the Fokker plank techniques were devised to produce results for a system whereby the noise process driving the system is large compared to system bandwidth, such as with additive thermal noise. However in the case of local oscillator phase noise, the noise process occurs within the loop (Fig6.5). The above analyses may therefore not be strictly applicable [Prabhu, 1976], but this approach will be adopted here as a reasonable approximation. The above distribution is approximately Gaussian for large α (for α say > 20). For most cases of usable phase noise, the Gaussian distribution can be applied for both thermal and phase noise.

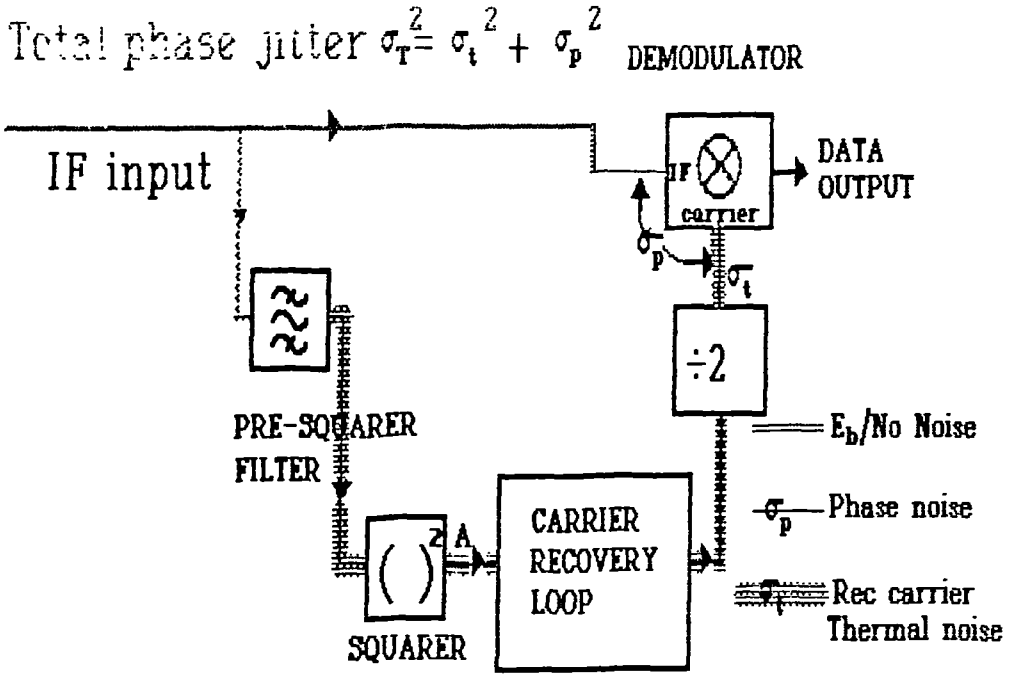


Fig 6.5 BPSK Coherent demodulator displaying components of noise

The complete integral to be applied becomes:-

$$BER = \int_{-\pi}^{\pi} \frac{1}{2}\text{erfc}\sqrt{\frac{E_b}{n_o}\cos^2(\theta_o+\phi(t))}\,\frac{\exp(\sigma^{-2}\cos\phi)}{2\pi I_o(\sigma^{-2})}.d\phi \qquad (6.14)$$

6.3. Carrier Recovery

6.3.1 Origin of Phase Errors

There are three factors to be considered giving rise to phase errors. These are as discussed below.

6.3.1.1 Static Phase Errors

It is the nature of CRLs that some form of static phase error is difficult to avoid. Fig6.6 displays a schematic of a typical CRL. The principal source of static phase errors is uncertain differential phase shifts in the paths between data recovery and carrier regeneration usually due to filtering. The use of digital techniques could assist in reducing this by the implementation of more stable filters. The use of second order loops would remove the offset frequency dependence of the phase error at the phase detector, leaving a residual constant phase shift.

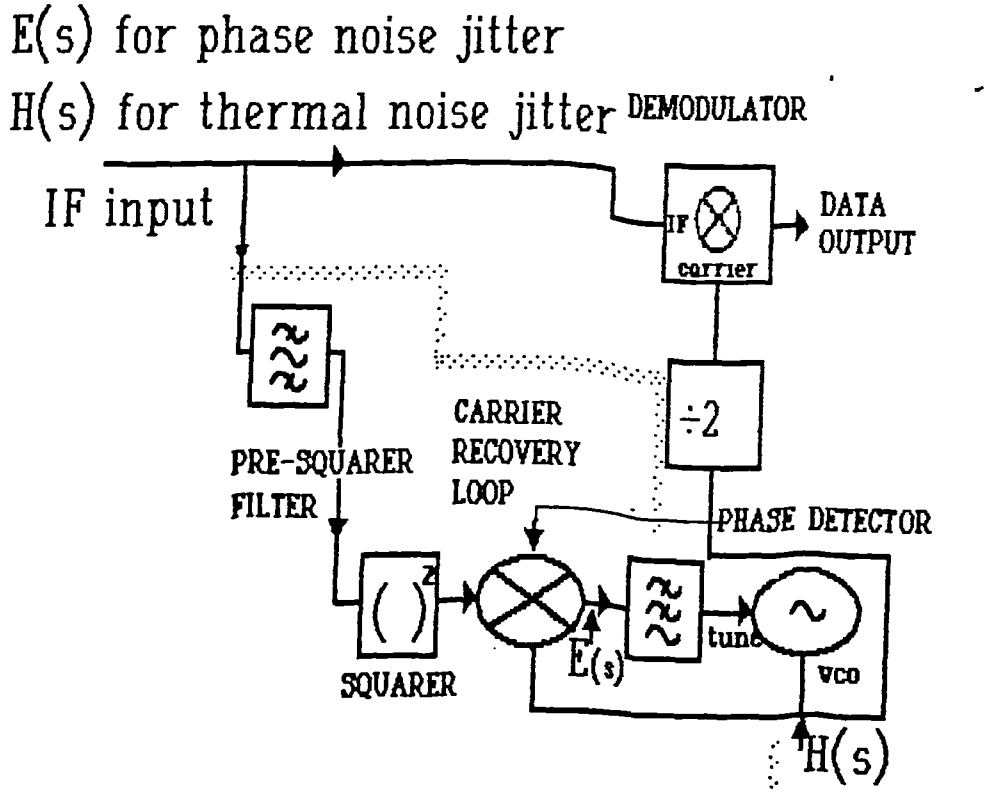


Fig 6.6 Block diagram of carrier recovery loop

6.3.1.2 Dynamic Phase Errors

As stated earlier in this report, the phase jitter at the demodulator results from thermal noise and local oscillator phase noise. The total local oscillator phase noise to be considered is the root sum of squares contribution of each local oscillator in the link, including both transmitter, satellite transponder and receiver downconverters (and, to a lesser extent, the local carrier recovery oscillator). A computer generated plot of the BER against E_b/n_o using equation (6.14) is given in fig 6.3 of §6.2.1 with the carrier recovery phase jitter as a parameter.

6.3.1.3 Thermal Noise

In coherent demodulation, the carrier component is normally absent from the signal and has to be regenerated by a non-linear operation. In a power CRL, the signal is raised to a power equal to the number of phase states in the data signal, and the phase shifts in the signal are multiplied by the power to which the signal is raised. The signal at point A in fig 6.6 consists of a carrier and broadband noise; since the carrier occupies a very narrow spectral width, a very narrow filter must be used to isolate the carrier from the noise. The CRL provides a filtering function by means of a narrow band phase locked loop (PLL). An alternative implementation is the Costas Loop, whose performance is essentially equivalent to the power CRL [Holmes, 1982c].

6.3.2 Thermal noise and the CRL multiplier

A rigourous analysis of the effect of the multiplier in a CRL is extremely complicated owing to the presence of noise, modulation and carrier in the calculation. The usual method of analysis is the convolution of the signal and noise with itself. Oberst and Schilling [1971] obtain their results using an unmodulated carrier as the input. They make no mention of the frequency distribution of the noise around the recovered carrier, but they do consider the effect of different pre-squarer filters. Davenport and Root [1987] use the same method but obtain the spectral distribution at the output for the case of a rectangular input frequency distribution. Holmes [1982d] and Gardner [1979b] also use a rectangular input frequency distribution but take account of modulation in their analysis. A plot of calculated output signal to noise ratios against input signal to noise ratios is given in fig 6.7 [Oberst & Schilling, 1971] for different carrier recovery powers.

One fact that emerges in all the analyses is that in high signal to noise ratios there is a degradation of $20\log(\mathbf{n})$ dB in signal to noise ratio (SNR) at the output of the multiplier, where **n** is the power to which the signal is raised. At low SNRs, there is an additional loss known as the squaring loss. In many communications systems, such as those using

coding, or direct sequence spread spectrum, the SNR at the squaring loop can be negative, so consideration of the squaring loss becomes vital.

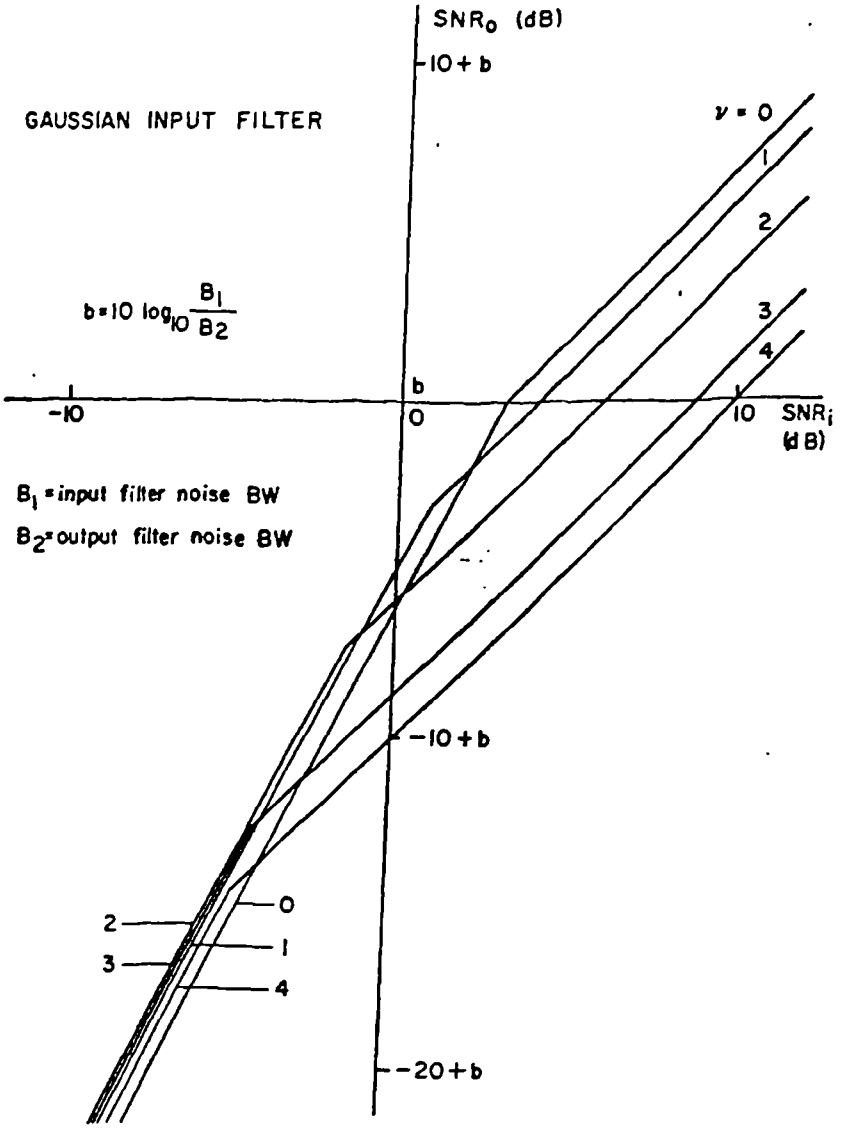


Fig 6.7 Signal to noise ratio after raising signal to a power N [Oberst & Schilling, 1971]

Using the Oberst and Schilling method, the relationship between the SNR at the output of the squarer (snr_o) and that at the input to the squarer (snr_i) is given by:-

$$snr_o = \frac{\frac{1}{2}\left(\frac{B_p}{B_L}\right)(snr_i)^2}{F(2) + 2(snr_i)} \tag{6.15}$$

where B_p is the bandwidth of the presquarer filter and B_L is the equivalent noise bandwidth of the CRL. F(n) is a factor derived from the convolution of the input spectrum with itself n times (2 for a squaring loop). In order to work with noise density ratios, the following substitutions are made:-

$$snr_o = C/N_oB_L, \quad snr_i = S/N_oB_p \tag{6.16}$$

where C is the recovered carrier power and S is the signal power at the input. At low signal to noise ratio, the squaring loss portion of the input-output noise curve can be extended to the output signal to noise axis to give a 0dB intercept point. This intercept point is therefore a useful figure of merit in order to determine the efficiency of the squarer.

Substituting 6.21 into 6.20 gives:-

$$\frac{C}{N_o} = \frac{1}{2}B_P \frac{\left(\frac{S}{N_oB_P}\right)^2}{F(2)+2\frac{S}{N_oB_P}} \tag{6.17}$$

Inverting this to obtain the noise density to carrier power gives:-

$$\frac{N_o}{C} = 4\left(\frac{1}{2}F(2)\frac{N_oB_P}{S} + 1\right)\frac{N_o}{S} \tag{6.18}$$

If $\frac{1}{2}F(2)\frac{N_oB_P}{S} \ll 1$, the result is independent of the Presquarer filter and the output signal to noise ratio is 4 times that at the input, equivalent to a 6dB rise in noise. The factor $\frac{1}{2}F(2)\frac{N_oB_P}{S}$ is known as the "squaring loss". When it becomes greater than unity, the output noise increases by 12dB for every 6dB increase in input noise. This is displayed in fig6.7 which is Oberst and Schilling's plot for a Gaussian presquarer filter. The factor F(2) is dependent upon presquarer filter response and is:-

$F(2) = \sqrt{2}$ for a Gaussian response

and $F(2) = 2$ for a single pole filter.

For the case of a Gaussian filter the noise sidebands are:-

$$\frac{N_o}{C} = 4\left(\frac{1}{\sqrt{2}}\frac{N_oB_P}{S} + 1\right)\frac{N_o}{S} \tag{6.19}$$

It appears that the output noise spectral shape depends upon the shape of the presquarer filter. According to Davenport the use of a rectangular presquarer filter results in a triangular distribution due to squaring loss. Figs6.8 and 6.9 illustrate squarer performance as depicted by Davenport. Fig6.8 shows the effect of the squarer on a Gaussian noise input only. The spectral distribution forms a triangular shape at twice the input frequency, the apex of the triangle being at the center of the input noise band and the base stretches over twice the input band.

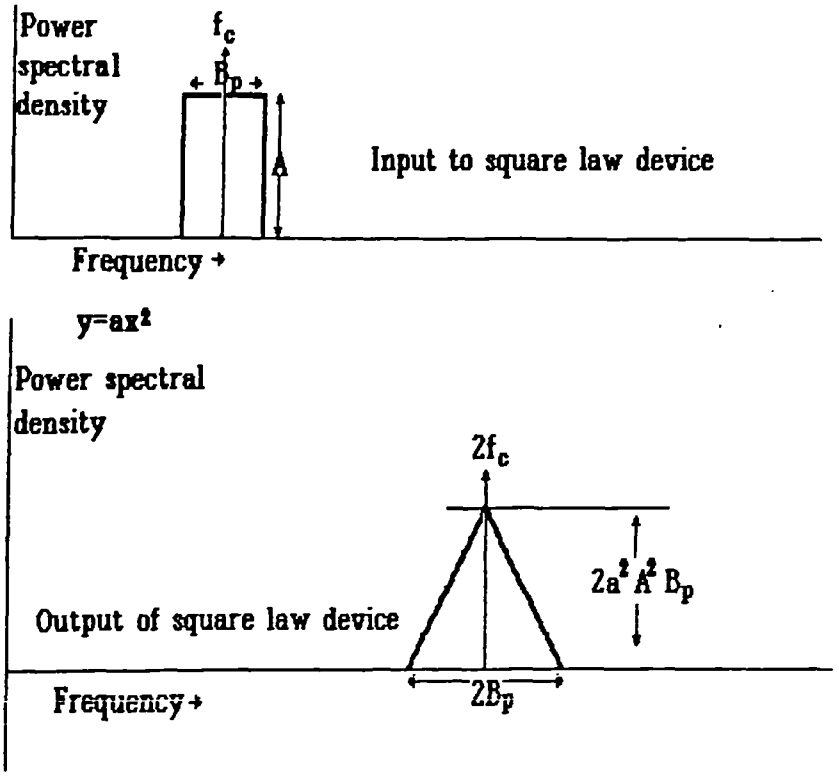


Fig 6.8 Gaussian noise only input to squarer

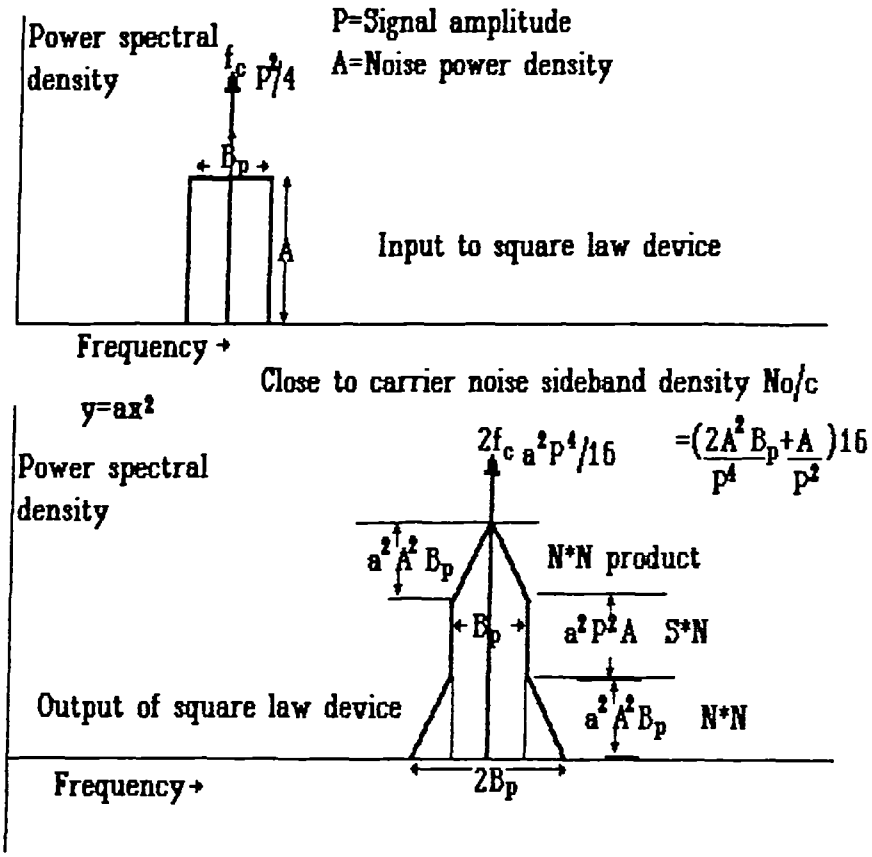


Fig 6.9 Signal and noise input to squarer

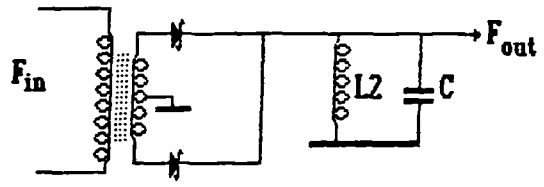
The peak of this apex is at a power density proportional to the square of input power and input power bandwidth. On application of input signal, the signal x noise products and noise x noise products are additive, so in addition to the triangle distribution as in fig 6.8 there is a rectangular distribution of width equal to the input bandpass filter.
The rectangular distribution is due to signal x noise products. The corresponding equation of noise sideband density for a rectangular pre-squarer filter is:-

$$\frac{N_o}{C} = 4\left(\frac{1 n_o B_P}{2\ S} + 1\right)\frac{N_o}{S} \qquad (6.20)$$

Note that the point at which the slope of the signal/noise curve changes from (1 dB to 1 dB) to (2 dB to 1 dB) is 4.5dB higher for a rectangular filter than for a Gaussian, so it is expected that superior performance should be obtainable from a Gaussian input filter.

6.3.3 Measured Results from a Carrier recovery loop squarer

As part of prototyping programme of a 20.48 kbaud BPSK modem, the performance measurements of which will be covered in §9.10, a squarer was built and its performance evaluated against the theory. The squarer function is provided by a Schottky diode full wave rectifier which has approximately square law characteristics [Stroud, 1984]. A surface acoustic wave filter with Gaussian characteristics and a noise bandwidth of 300 kHz was used as a presquarer filter. Such devices are inexpensive and readily available commercially for use as FM stereo IF filters in broadcast receivers. Fig 6.10 shows a circuit diagram of the squarer implementation for the BPSK modem.



Schottky Diode Frequency Doubler

As used to recover carrier in the experimental BPSK system

L2 and C form a resonant circuit at the output frequency

Fig 6.10 Schottky diode frequency multiplier

An intercept point of +40 dBm was required of the input amplifier in order to avoid degradation of the input signal with negative signal to noise ratios. By using a specially calibrated spectrum analyser against a known filter response, the input signal to noise ratio was measured. Recovered carrier sideband noise to carrier power ratio is shown against input noise to signal power in fig 6.11.

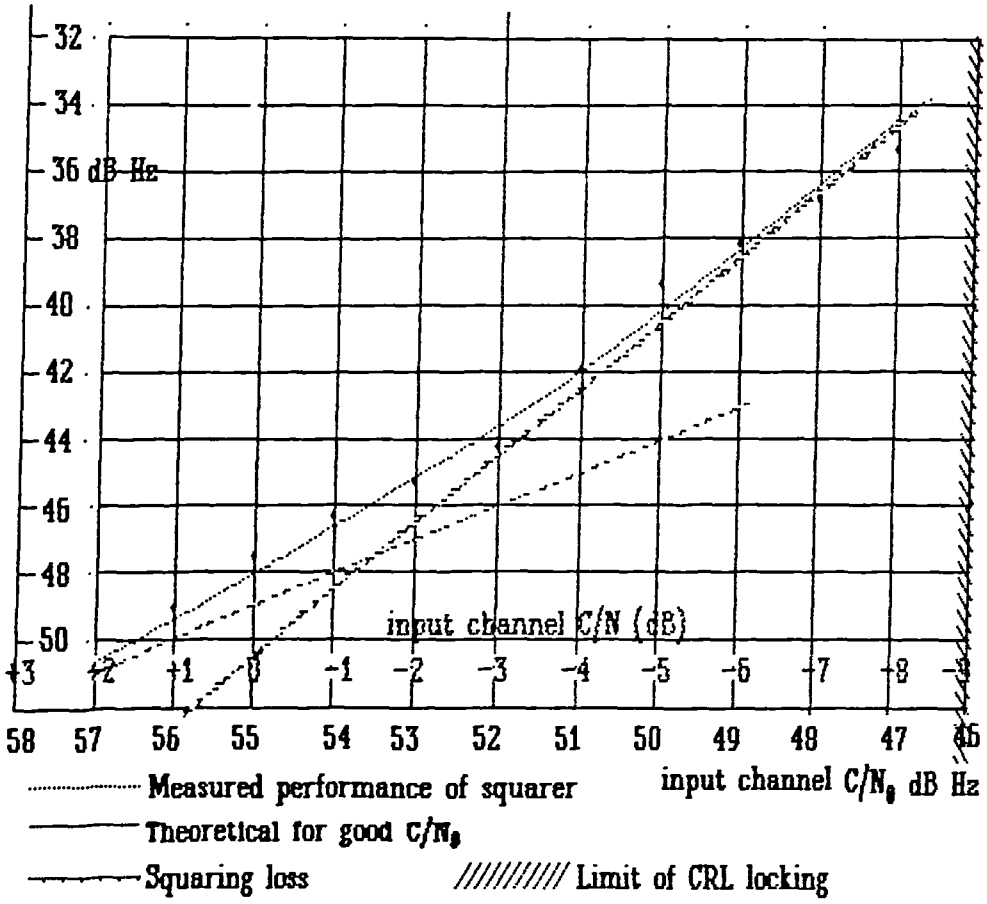


Fig 6.11 Measured performance of squarer and Gaussian filter

On this curve is shown the zero squaring loss line and a straight line fit is placed against the curve in the squaring loss region. A plot of the recovered carrier and its noise sidebands is shown in fig6.12. A plot is obtained for each of the two different input signal to noise ratios; the upper plot represents the spectrum for a -49dBc/Hz noise density to signal ratio which would incur considerable squaring loss. It can be noticed that the spectral density profile is approximately flat around the carrier which contradicts Davenport's expectation of a triangular noise profile. However, there is spectral broadening at the edges of the presquarer bandpass filter response which is in agreement with Davenport's theory. This curved profile around the carrier could explain the superior performance of the Gaussian filter against the rectangular filter as used by Davenport which results in the recovered carrier being at the apex of the triangular noise profile. The intersection of the above plotted squaring loss line in fig6.11 with the zero loss line gives a measure of squarer performance. Such an intersection is represented by a squaring loss factor of unity in equations (6.22) and (6.23). The intersection point is at an input signal to noise ratio of -2.0dB and can be compared with -1.5dB as predicted by Schilling's analysis. Davenport's analysis gives an intercept point of +3dB which would result in higher recovered carrier jitter. This intercept point is therefore a useful figure of merit in order to determine the efficiency of the squarer.

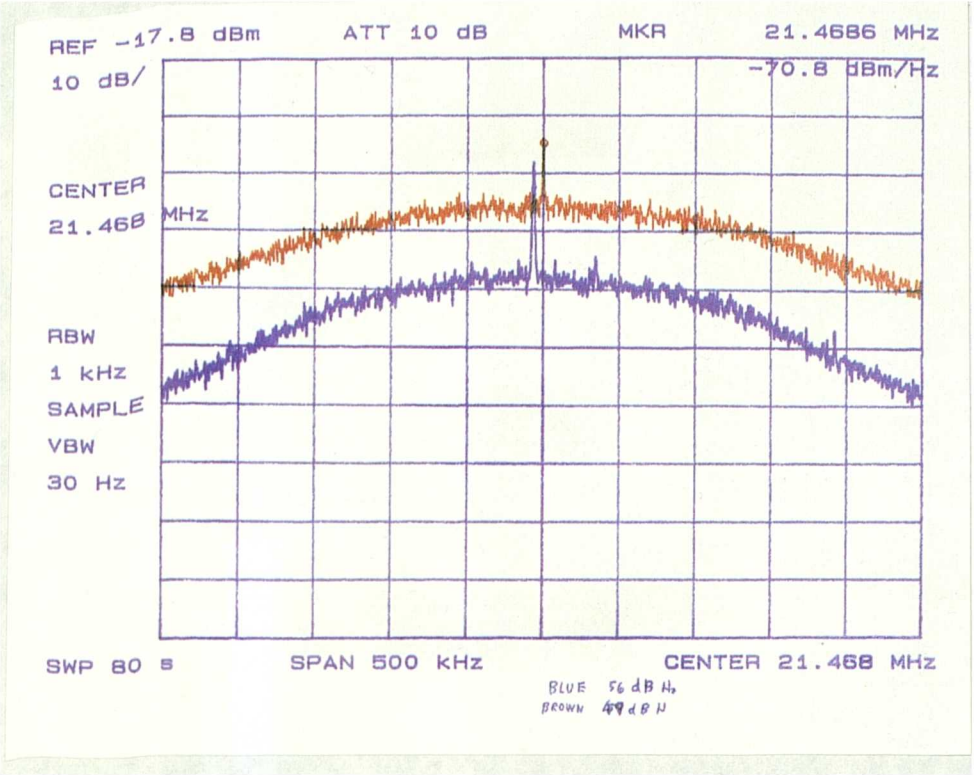


Fig 6.12 Spectrum analyser plots of the recovered carrier at the squarer output

6.3.4 Calculation of Recovered Carrier Jitter

It is necessary to determine the jitter on the recovered carrier due to the additive thermal noise, as well as that on the signal itself. Both of these are applied to the multiplier forming the signal demodulator, and the degree of decorrelation of the two must be determined. As described by Prabhu [1976], the CRL is usually a second order loop and performs the following functions:-

1) Re_inserts the carrier into the signal, in order that it can be demodulated;

2) Reduces the effect of broadband additive noise on the recovered carrier by means of the out of band rejection of the unwanted noise.

The thermal noise will appear as phase noise sidebands around the recovered carrier. This is due to the reduced sensitivity of the CRL phase detector to the amplitude component of the noise [Viterbi, 1966a] when the signal to noise ratio in the PLL bandwidth is good. Inside the loop bandwidth of the PLL, the value of the phase noise sidebands on the recovered carrier will be $\mathcal{L}_{crl}(0)$, where:-

$$\mathcal{L}_{crl}(0) = \frac{N_0}{8C} \tag{6.21}$$

and hence:-

$$\mathcal{L}_{crl}(0) = \frac{1}{2}\left(\frac{1}{\sqrt{2}}\frac{N_0 B_p}{S} + 1\right)\frac{N_0}{S} \tag{6.22}$$

The recovered carrier is at twice signal frequency, therefore the phase deviation must be divided by two to normalise it with respect to the carrier. The noise power must therefore be divided by four. A further factor of two can be included to account for the fact that the additive noise on the recovered carrier is converted to phase noise. (This is only valid for good PLL SNRs.) This brings the total division ratio to 8. The sideband level is modified by the closed loop transfer function of the CRL ($H(s)_{crl}$). From modulation theory [Robins, 1982a] the jitter can be determined as σ_t where:-

$$\sigma_t = \frac{1}{2}\left(\frac{1}{\sqrt{2}}\frac{N_0 B_p}{S} + 1\right)\frac{N_0}{S}\int_0^\infty 2|H(s)|^2.df \tag{6.23}$$

The result of the integral operation is determined by the CRL characteristics, viz: the loop natural frequency ω_n and loop damping factor ζ. The most commonly used value of damping factor is 1.3 [Blanchard, A., 1976a], [Robins, 1982b], as this gives the optimum resistance to CRL cycle slipping.

For a CRL damping factor of 1.3 it can be shown that:-

$$\int_0^\infty 2|H(s)|^2.df = \frac{3\omega_n}{2} \tag{6.24}$$

Assuming a second order PLL, the integral in equation (6.24) is equal to the equivalent noise bandwidth of the phase locked loop bandwidth, B_L, which is also given by:-

$$B_L = \frac{\omega_n}{2}\left(\zeta + \frac{1}{4\zeta}\right) \tag{6.25}$$

where ζ is the loop damping factor.

For the particular case of ζ which is usually chosen of 1.3:-

$$B_L = \frac{3\omega_n}{4} \qquad \text{Hz} \tag{6.26}$$

and inserting this in equations (6.23) and (6.25) gives:-

$$\sigma_t^2 = \frac{3\omega_n}{4}\left(\frac{1}{\sqrt{2}}\frac{N_o B_p}{S} + 1\right)\frac{N_o}{S} \qquad (6.27)$$

The natural loop frequency of the CRL is therefore a function of the additive sourced phase jitter.

6.3.5 Other Coherent PSK Schemes

A QPSK signal can be considered as two orthogonal BPSK signals on the same channel. The same error rate analysis that is applied to BPSK signals can also be applied to QPSK, but account must be taken of interference between the two signals for a non zero phase reference. It can be shown that the error rate for QPSK is given by:-

$$P_e = \frac{1}{2}\left(Q\sqrt{\frac{2E_b(\cos E + \sin E)^2}{N_o}} + Q\sqrt{\frac{2E_b(\cos E - \sin E)^2}{N_o}}\right) \qquad (6.28)$$

where Q(x) is the Marcum Q function.

There is a 50% probability of the quadrature signal having the same level as the in phase signal. In this case the resultant E_b/N_o is the sum of the component E_b/N_o values from the in phase and quadrature signals. The first part of equation (6.28) relates therefore to I and Q data being equal. On the other hand if the data values are in opposition, the quadrature component must be subtracted, thus giving the second part to equation (6.28).

This must be substituted into the expression (6.7) above to obtain a BER result. The value of the Q function is exactly defined as:-

$$P(\phi) = \frac{1}{\sqrt{2\pi}}\int_x^\infty \exp\frac{-u^2}{2}\,du \qquad (6.29)$$

However, in order to aid numerical evaluation, a form of Mills expansion is used as published by Zelen & Severo [Abramowitz & Stegun, 1964], which gives a residual error:-

$$\delta < 7.5\times10^{-8}.$$

The Mills expansion is as follows:-

$$Q(x) = \frac{\exp\frac{-x}{2}}{\sqrt{2\pi}}(b_1 t + b_2 t^2 + b_3 t^3 + b_4 t^4 + b_5 t^5) + \delta \qquad (6.30)$$

where:-

$$t = \frac{1}{(1+px)} \tag{6.31}$$

and:-

$p = .2316419$

$b_1 = .3193811530$

$b_2 = -.356563782$

$b_3 = .1.781477937$

$b_4 = -1.821255978$

$b_5 = 1.330274429$

For offset QPSK, as can be seen in fig 6.13, a data transition point in one signal occurs at the midpoint of the other signal. If a data change occurs at the transition the interference component from the first half of the second signal is cancelled by the component from the second half. In this case the BER is identical to that of BPSK. If no transition occurs then the error rate is identical to that of QPSK. The probability of either of these cases occurring is one half.

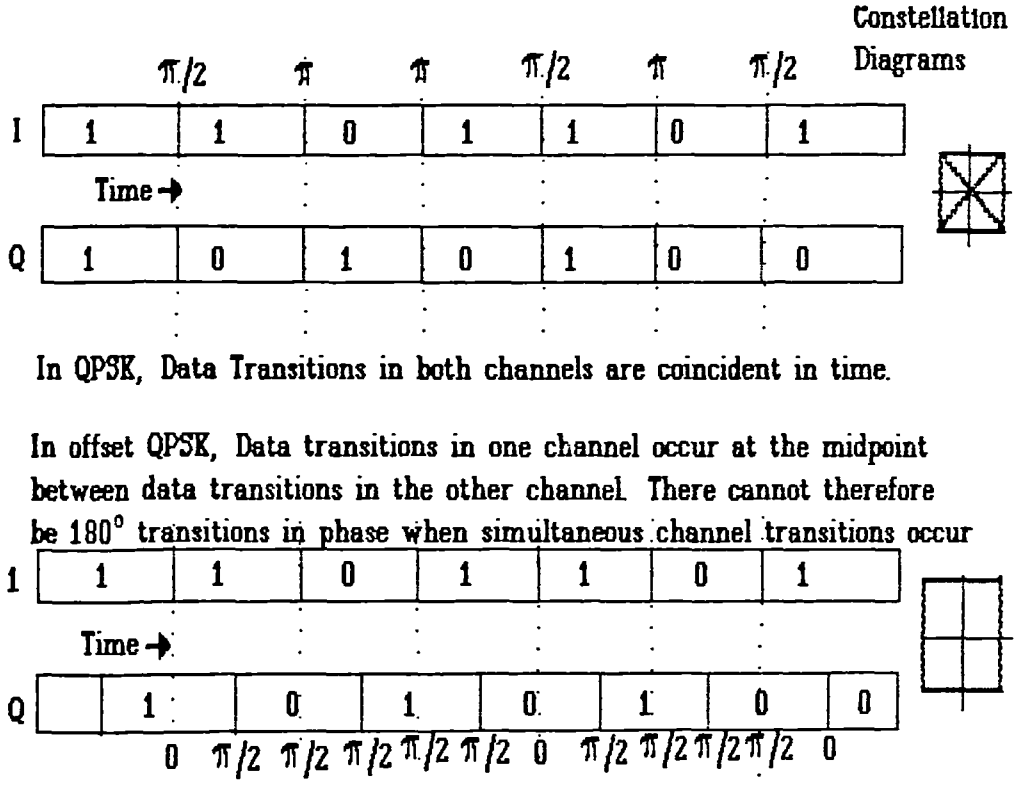


Fig 6.13 Offset QPSK modulation

Therefore the BER for an offset QPSK signal is:-

$$P_{OQPSK} = \frac{1}{2}P_{QPSK} + \frac{1}{2}P_{BPSK} \tag{6.32}$$

Computer plots have been produced during work for this thesis to show the degradation of BER for various modulation and coding schemes. The results can be compared with published work [Holmes, 1982e],[Heller & Jacobs, 1971]. Fig 6.14. displays these without coding for offset QPSK. The value of jitter used is the RSS (root sum of squares) jitter in degrees, allowing for the response of the CRL.

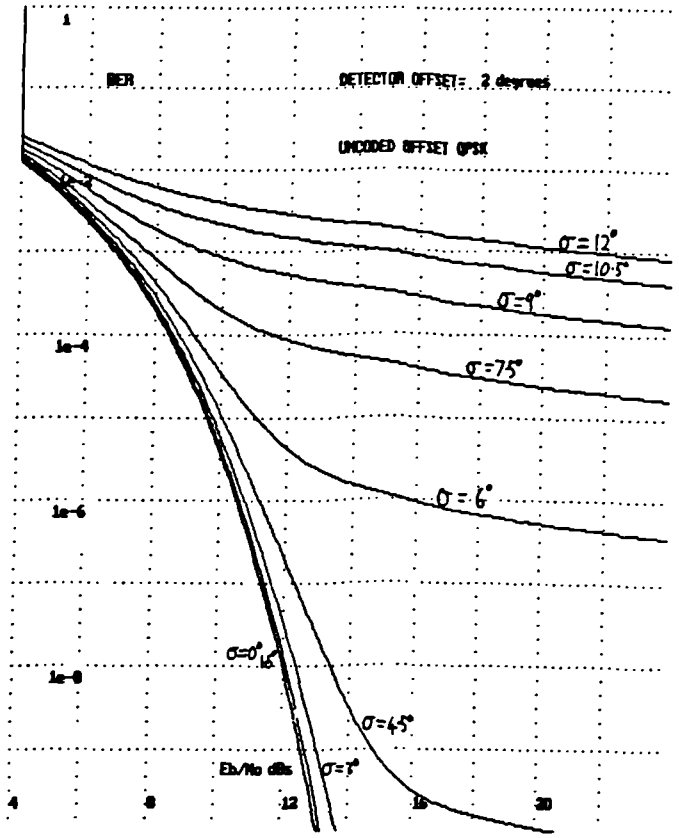


Fig 6.14 Plots of BER against E_b/N_o for different values of recovered carrier jitter, uncoded QPSK

In a QPSK system a frequency quadrupler must be used to recover the carrier and the corresponding jitter value for a quadrupler can be shown to be approximately:-

$$\sigma_t^2 = \frac{3\omega_n}{4}\left(\frac{1N_oB_p}{4\ S} + 1\right)\frac{N_o}{S} \tag{6.33}$$

Throughout this thesis, half-rate Viterbi convolutional encoding, constraint length 7, with Viterbi decoding, will be considered. (Hereinafter referred to simply as 'Viterbi'.)

6.3.6 Bit Error Rates for Coded Data

In order to operate at lower signal to noise ratios, some form of Forward Error Correction coding (FEC) is often used. For satellite channels in the presence of Gaussian noise, convolutional encoding with Viterbi decoding is often chosen. The bit error rates for coded channels cannot be accurately analytically defined, so they have to be found by simulation results and a polynomial fit found to the BER vs E_b/N_o curve [Heller & Jacobs, 1971]. This polynomial must be used to replace the standard error rate expression (or its equivalent for QPSK), viz:-

$$P_e = P_{eo}\{E_b/N_o \cos^2(\theta_o + \phi(t)\} \tag{6.34}$$

where θ_o is the static phase offset and $\phi(t)$ is the offset due to phase noise. The result of this operation has been published in the literature [Heller & Jacobs, 1971]. In order to generate the above polynomial, the author applied a polynomial fit to published performance data on a commercially available Viterbi device [Sorep, 1989]. Computer generated curves have been produced, and shown to agree with the published literature. Fig 6.15 displays BER curves with offset QPSK as above, using convolutional coding and Viterbi half-rate, constraint length seven, with soft decision 4 level decoding.

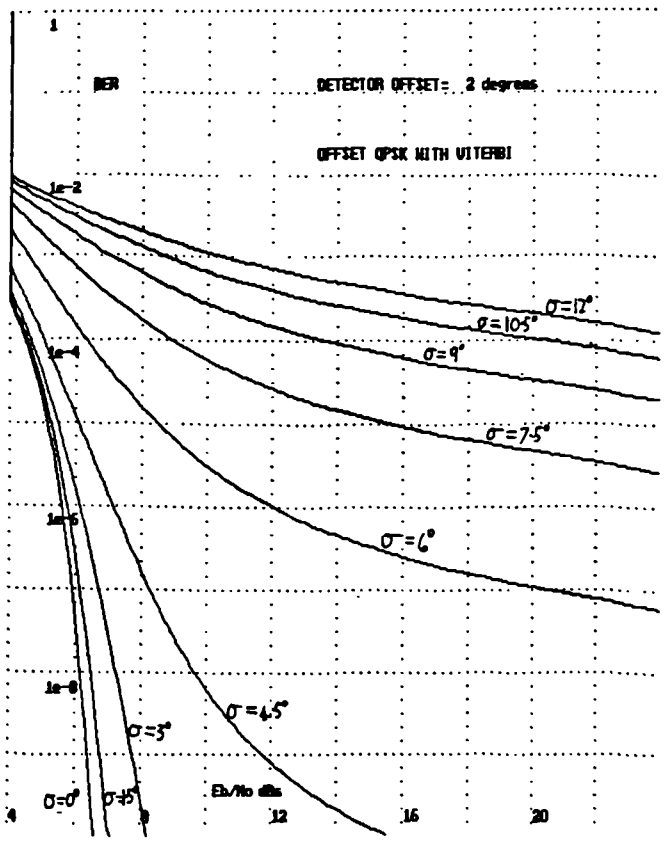


Fig 6.15 Plots of BER against E_b/N_o for different values of recovered carrier jitter, coded QPSK

One striking feature of these curves is the steepness of the BER curve when Viterbi decoding is employed with half-rate seven segment convolutional encoding.

When coding is used, the data rate over the link, b_L, is related to the information rate b_i by:- $b_L = b_i/m$, where m is the coding rate ($m < 1$). For phase noise calculations b_L is used for the data-rate, whereas the information rate b_i may be plotted as the independent variable in phase noise degradation plots. Fig 6.15 gives the BER curves for a coded QPSK signal.

6.3.7 Discrete spurious signals

In practice, a synthesiser system will not only contain random phase noise sidebands, but also discrete sidebands. These sidebands, commonly referred to as spurious signals will have different effects on the BER calculation to Gaussian distributed random noise. At the CRL, the resultant effective spurious contribution would be the root sum of squares (RSS) of all individual spurious signals modified by the error function of the carrier recovery loop:-

$$\sigma_{ps}^2 = 2 \sum_{f=0}^{f_d} P_s(f)|E(s)|^2 \qquad (6.34a)$$

where σ_{ps}^2 is the phase jitter variance due to discrete spurious signals, and $P_s(f)$ is the power of each individual spurious signal at an offset from carrier frequency f. The distribution of σ_{ps}^2 can be assumed to be uniform rather than Gaussian. Therefore this variance can be added to the static phase offset in equation 6.8 to give:-

$$BER = \int_{-\pi}^{\pi} \frac{1}{2} \operatorname{erfc} \sqrt{\frac{E_b}{N_o} \cos^2(\theta_o + \sigma_{ps} + \phi(t))\, P(\phi)}.d\phi \qquad (6.34b)$$

Therefore when attempting a BER analysis of a system, the phase error contribution of the spurious signals must be calculated before the random phase noise effects are calculated.

6.3.8 Acquisition time

If the above system was adapted to a spread spectrum application and the local oscillator was required to tune over 2 MHz in order to acquire the signal, then the expected acquisition time could be of interest.

The maximum sweep rate is determined by [Viterbi, 1963b]:-

$$\dot{\omega} = \omega_n$$

Assuming a loop bandwidth of 18.63Hz the maximum sweep rate would be 2.18kHz per second. In order to guarentee reliable locking, it would be necessary to sweep less than this, say 1.3kHz per second, whereupon a sweep time of 26 minutes would be required. This would be totally unacceptable for most applications. A method of speeding acquisition would therefore be required. One possible approach would be the use of an FFT based search algorithm together with a direct digital synthesiser implemented as in chapter 8 used to provide a search oscillator.

6.4 Phase Noise Jitter

6.4.1 Introduction

So far only the additive thermal noise contributions to the carrier recovery jitter have been considered. However, the phase noise of every local oscillator in the link also contributes to this jitter figure.

6.4.2 Phase Noise Link Budget

The system designer has traditionally calculated a thermal noise link budget in order to arrive at the most economical means of providing a given BER [Feher, K, 1981]. This involves considering propagation loss, dish size, satellite EIRP, and front-end noise figure in order to arrive at a suitable E_b/N_0. Another link budget calculation may thus be required which considers the cumulative effect of all the local oscillators in the link.

This process could well be iterative with the first process based solely upon additive thermal noise, leading eventually to a final value of E_b/N_0. The BER degradation may be determined by the above equation (6.7) (or plots such as fig7.4) for a given total phase jitter variance σ_T^2. This jitter variance is the sum of all the jitter variances in the system, ie:-

$$\sigma_T^2 = \sigma_t^2 + \sigma_p^2 \quad \text{and} \quad \sigma_p^2 = \sum_{i=1}^{n} \sigma_i^2 \tag{6.35}$$

The total phase jitter at the demodulator σ_T^2 is the sum of contributions from additive thermal noise σ_t^2 and the total local oscillator phase noise σ_p^2. The total local oscillator phase noise is in turn the root sum of the squares of contributions of each local oscillator in the link, where n is the total number of local oscillators.

6.4.3 Phase Noise to Jitter Conversion

Equation (6.7) requires the phase noise to be expressed as a variance in radians squared, but oscillator phase noise is conventionally expressed as a phase noise power density ratio as a function of offset from carrier frequency. If synthesised local oscillators are used then the phase noise distribution can vary according to the synthesiser architecture, and is not necessarily the f^{-3} relationship quoted in many authors' analyses of the problem [Surinder,K 1988]. In order to convert the phase noise sidebands to carrier recovery jitter, the response of the CRL to the noise sidebands must be considered. The CRL responds to local oscillator phase noise as if the noise originates within the loop, rather than external to it as with the additive noise. The reason for this is because, as shown in in fig 6.6, the same phase noise is present in both the data and carrier recovery arms of the demodulator. The CRL can respond to the phase noise and closes the loop around it by means of the local oscillator that it controls. Any phase noise which appears at the demodulator does so as a result of the error function of the CRL, where:-

$$H(s)_{crl} = 1 - E(s)_{crl} \tag{6.36}$$

The phase jitter contribution of each local oscillator can be found by integrating the phase jitter components of the sidebands over all offset frequencies up to the data rate:-

$$\sigma_{px}^2 = 2\int_0^{f_d} \mathcal{L}(f_m) 2|E(s)|^2 . df_m \tag{6.37}$$

The integration from zero offset from carrier is defined in this case because the f^{-3} relationship close to carrier of the oscillator is balanced by the f^4 relationship of the PLL error function. The magnitude of the error function for a second order loop is [Blanchard, 1976b]:-

$$|E(s)|^2 = \frac{\frac{\omega^4}{\omega_n^4}}{1 + \frac{(4\zeta^2 - 2)\omega^2}{\omega_n^2} + \frac{\omega^4}{\omega_n^4}} \tag{6.38}$$

where ω_n is the loop natural frequency in radians/sec, and ζ is the synthesiser damping factor.

In order to evaluate the RMS jitter it is necessary to integrate the phase noise over a frequency range up to the data rate. There are two possible approaches to this:-

1) Integrate for measured and plotted values of phase noise for the local oscillator;

2) Perform a phase noise analysis of the synthesiser and then integrate the E(s) curve.

Procedure 1 is normally taken if either of the following are used:-

a) An oscillator of known power law for the phase noise sidebands; or,

b) A local oscillator where the internal structure is either not known, or not of interest and only measurements are required.

An example of Procedure 1 is when dealing with a satellite transponder, or when determining specification levels. Procedure 2 is used when dealing with the design of data terminal synthesisers whereby the influence of the synthesiser architecture upon terminal performance can be evaluated. A computer program has been written for each case, as part of the work for this thesis, to perform the above calculations, and will be further described in chapter 9.

6.4.4 Phase Jitter to BER Conversion

The bit error rate can be determined as:-

$$BER = \int_{-\pi}^{\pi} P_e(\phi)\, P(\phi).d\phi \tag{6.39}$$

where $P_e(\phi)$ is the probability of an error conditioned on ϕ, and $P(\phi)$ is the probability of finding a given phase offset ϕ, where, for a second order carrier recovery loop:-

$$P(\phi) = \frac{\exp(\sigma^{-2} \cos \phi)}{2\pi I_o(\sigma^{-2})} \tag{6.40}$$

(I_o is the modified Bessel function of zero order).

6.5 Phase "Hits"

Phase "hits" are a sudden discontinuity in the phase of the output of a local oscillator. The causes include:-

1) Temperature effects in local oscillator resonators [Ondria, &Singleton, 1988].

2) Bifurcation points in frequency multipliers and PLOs [Wilson, M.P. & Tozer, T.C, 1991]. Multiplier bifurcation points are investigated in detail in chapter 7.

3) Resonator "burst noise". Evidence of resonator burst noise has been discussed in §3.3.5.6.

Phase "hits" are a problem because the "hit" becomes misrepresented as data. Due to the high speed nature of this transient, this becomes more of a problem with high speed data and more data is lost in this case. Phase "hits" can be measured in a similar manner to the 2-port phase noise test circuit of §3.3.5.4. The output is differentiated and then fed to a threshold detector. Transitions above a certain threshold are subsequently counted. Hwan & Brown [1988] suggested another method suitable for PLOs. The tuning voltage fed to the oscillator varactor is monitored for sudden changes. A window comparator then enable s any such "hits" to be logged by a computer.

In oscillators, rather than a continuous change in mechanical dimension, sometimes the change occurs in a ratchet manner as stored mechanical energy is suddenly released. This sudden change in mechanical dimension results in a sudden phase change in the output, or phase "hit". If the oscillator is phase locked, unless a very wide loop bandwidth is used, the PLL will temporarily lose lock, and therefore be ineffectual as regards phase hit performance. Attention therefore must be paid to the detailed mechanical design of the oscillator. Some oscillators are more susceptible to phase "hits " than other types. The implications for microwave oscillator design is further discussed in §4.6.1.2. It is beyond the scope of this thesis to thoroughly investigate phase hits and therefore such an investigation is recommended for further work.

6.6 Influence of Reference Phase Noise upon System Performance

6.6.1 Introduction

The residual phase noise may be obtained by adding the $20\log N$ factor in dB to the fundamental reference phase noise in the receiver CRL. Although the degradation thus caused is generally small compared to the synthesiser excess noise, it may not be the case for low error rates. This is because the reference phase noise typically displays an offset frequency dependence of f^{-3} up to an offset frequency of 1 kHz.

Another problem is that there must be some means of providing a continuously variable VCXO so the CRL may lock onto the incoming signal. This oscillator must be able to cope with all the frequency uncertainties in the system, including ageing and temperature

effects. VCXOs that have a larger pulling range must use a resonator with a lower unloaded Q, resulting in greater f^{-3} noise [Parker, T.E, 1985]. One way of overcoming this problem is to use a synthesiser with narrow step size to track the signal. A possible solution to this problem is discussed in chapter 8.

6.6.2 Differentially Encoded PSK (DPSK)

It has been suggested that non-coherent demodulation techniques may provide an alternative method of demodulation for low data rates [Robins, 1982c]. A block diagram of a DPSK demodulator is displayed in fig6.16. This is in effect a frequency demodulator. The probability of error P_e with a differential demodulator is:-

$$P_e = \frac{1}{2}\exp\text{-}(E_b/N_o) \tag{6.40}$$

where $N_o/2$ is the (double sided) amplitude of the power spectrum of the additive white Gaussian noise (AWGN).

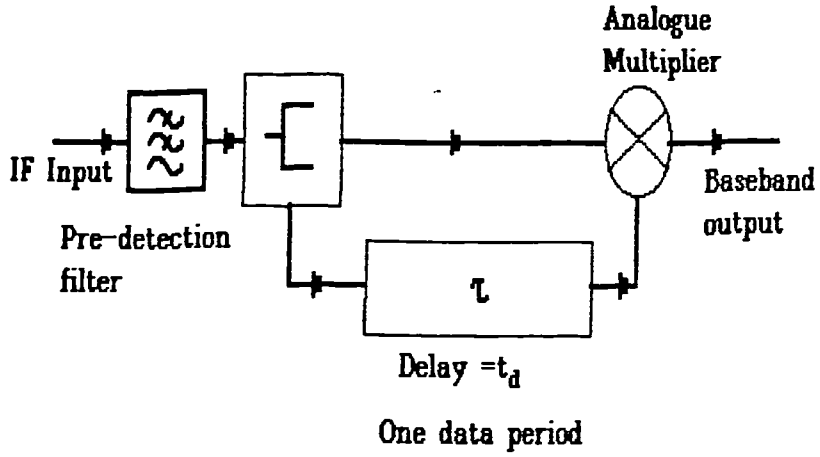


Fig 6.16 Non-coherent DPSK demodulator

This represents a theoretical required increase in E_b/N_0 of ≈0.8dB over that for coherent BPSK for most practical error rates. The main problems with this technique are [Park,J.H, 1978],[Winters, J.H, 1984]:-

1) The frequency uncertainty of the downconverted signal must be kept small;

2) The filtering must be carefully matched to avoid excessive losses due to intersymbol interference (ISI);

3) The delay must be accurately toleranced;

4) The clock recovery circuits become more critical.

All this implies a requirement for the use of digital signal processing techniques in the demodulator.

The effect of 2) alone increases the losses by typically at least another 1.2dB; normally this additional loss is highly undesirable, but it is possible that use of this technique can be made for conditions where coherent demodulation is difficult, or impossible. Such conditions include low data rates and high carrier frequencies (eg >30GHz), or the resultant non-coherent combining from frequency hopped spread spectrum systems. For the high frequency case there must be a point where the implementation loss for a coherent demodulator will exceed that of the non coherent demodulator; this could be a subject for further investigation.

The problem with the coherent case is that it is subject to the close to carrier $1/f^3$ noise of the reference resonator. The relative sensitivity to phase noise of the non-coherent demodulator is not constant with frequency. The sensitivity profile is displayed in fig 6.17, which is a plot of the sensitivity against offset from carrier frequency as given by Robins [Robins,W.P, 1982c].

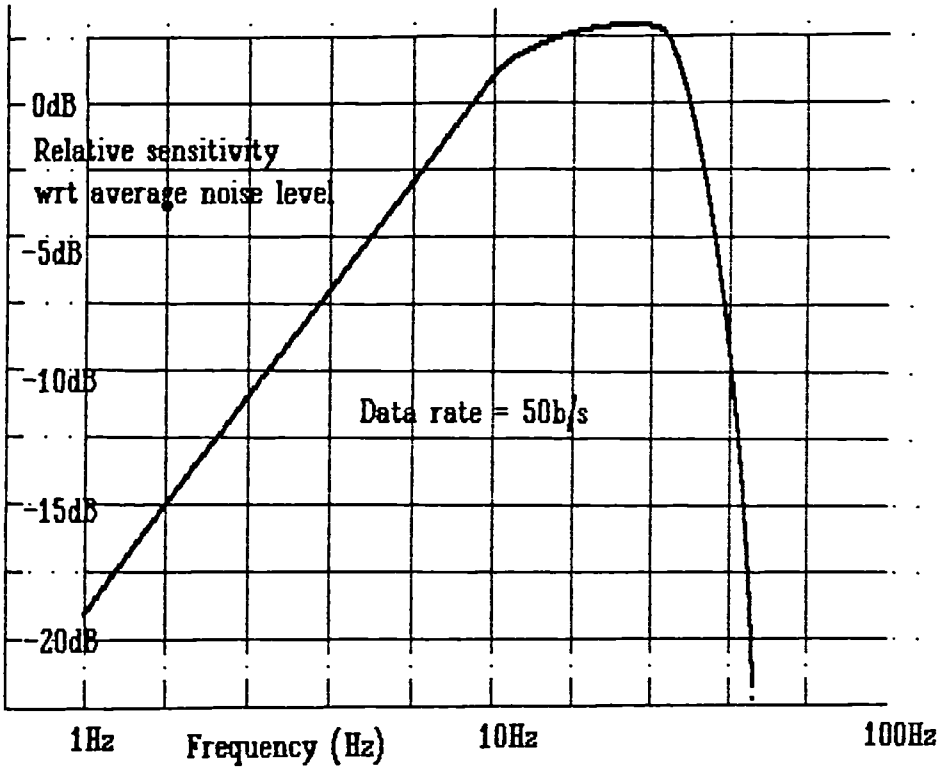


Fig 6.17 Relative sensitivity of non-coherent demodulator to phase noise

At low offset frequencies relative to the data rate the sensitivity increases at 6dB per octave increase in offset frequency. However, the sensitivity of this technique peaks at

the half data rate, and so therefore this technique may be more subject to the effects of synthesiser excess phase noise. Although the sensitivity to very close to carrier phase noise is reduced with this technique, the sensitivity to noise at half the symbol rate is increased relative to coherent BPSK demodulation. This would result in an increased sensitivity to synthesiser phase noise, vibration, and spurious sidebands.

Vibration and discrete spurious may pose a particular problem because of the localised spectral properties of discrete components. This has particular relevance to direct digital synthesis that may be used in frequency hopping applications. Therefore more care may be needed in the synthesiser design, but it may be more resilient to reference resonator noise. The advantage of this is that the synthesiser design is under the control of the terminal manufacturer, but the quality of crystals is less of a known quantity, and crystal manufacturers may demand a premium payment for low phase noise crystals.

The calculation of the degradation due to phase noise would proceed in a similar manner to that of coherent methods, but the weighting function for the differential demodulator must be added. Furthermore, phase noise will be passed onto the clock recovery circuits, the response of which must also be taken into account.

6.7 Conclusion

Chapter 6 has analysed possible effects on system performance of phase noise. The effect of imperfect carrier recovery was analysed with respect to a BPSK system. This was extended to include QPSK and the effect of coding. Computer programs were written to produce curves of sensitivity degradations against recovered carrier jitter. Such curves indicated that uncoded BPSK was relatively insensitive to phase noise, but QPSK and in particular coded BPSK and QPSK had steep BER curves and were therefore very sensitive to phase noise. These degradations result in adverse effects on the system link budget that may require expensive modifications to system components such as power amplifiers or low noise amplifiers.

The additional degradations brought about by the effects of phase noise imply that a phase noise link budget is required in addition to the usual system power link budget for each local oscillator in the system. Many local oscillators have phase noise sidebands which display both discrete and random components. These components must be given separate treatment in any link budget analysis.

Carrier recovery by the use of a frequency multiplier has been discussed and analysed. It has been shown that a square law input to output noise relationship is reached as the signal to noise ratio becomes negative. Carrier recovery multiplier performance is therefore critical especially when coded schemes are used that have a low signal to thermal noise ratio. The intersection of the square law section to the linear section of the output noise curve gives a useful figure of merit for a carrier recovery circuit.

There is a contradiction in requirements for the carrier recovery loop for coherent demodulation schemes. A narrow carrier recovery loop bandwidth is required to effectively remove thermal noise, and a wide loop bandwidth is required to remove phase noise.

The use of differential demodulation techniques may be advantageous when very low data rates are employed. In this case the dominant effect would be the $1/f^3$ noise of the crystal resonator source which could impose insuperable problems for a coherent system. Differential demodulation is more sensitive to noise components further away from carrier and therefore may not be advantageous when the phase noise is not falling steeply as the offset frequency is increased.

Phase noise requirements for synthesised local oscillators have been considered in chapter 6 in terms of possible impact on system performance.

6.8 Further work

The analysis applied in chapter 6 for coherent systems assumes that most of the phase noise power is close to the carrier and therefore within the carrier recovery loop bandwidth. However if most of the power is outside the CRL bandwidth, the CRL will have little effect and therefore a modification to the above analysis may be required. It is beyond the scope of the thesis to investigate this, but could be recommended as a topic of further investigation.

The fact that other degradations in system response are likely to be present simultaneously with the phase noise effects implies that simulation will be required to obtain accurate results. Such a simulation is beyond the scope of this thesis but important factors have been raised that must be taken into consideration. For the modulation schemes discussed in chapter 6, the tails of the various noise distributions discussed (Gaussian, Tikhonov)

were far more significant in determining the BER than the main body of the distribution. This implies that the Gaussian model used must be tested to ensure an accurate tail, rather than using without question the Gaussian models provided by the simulation package used. Many standard models are derived from the central limit theorem and may produce poor tails unless large numbers of samples are used.

6.9 References

Abramowitz, M & Stegun, I. 1964 Handbook of Mathematical Functions, chap. 26, p. 993, National Bureau of Standards.

Betts, J.A. 1983 *Signal processing, modulation and noise*, chap. 8, p. 188. Unibooks,

Bhargava, V.K. 1981a *Digital Communications by Satellite*, chap 4, p. 103. NY: Wiley

Bhargava, V.K. 1981b ibid. chap. 5, p. 126.

Blanchard, A. 1976a *Phase locked loops and their application to coherent receiver design*, chap. 12, p. 323. NY: Wiley.

Blanchard, A. 1976b ibid. chap. 6, p. 105.

Davenport, W. & Root W. 1987 *An introduction to the theory of random signals and noise*, chap. 12, p. 257. NY: IEEE Press.

Feher, K. 1981, *Digital Communications*, chap.1, p. 40. NJ:.Prentice Hall.

Gardner, F. 1979a *Phaselock techniques*, 2nd ed., chap 3, p. 20. NY: Wiley.

Gardner, F. 1979b ibid. chap. 11, p. 227

Heller, J.A. & Jacobs, I.M. Oct 1971 Viterbi Decoding for Satellite and Space Communication. *IEEE Trans Comm Tech.* Vol. 19, No. 5, p. 845

Holmes, J.K. 1982a *Coherent Spread Spectrum Systems*, chap. 6, p. 269. NY: Wiley.

Holmes, J.K. 1982b ibid. chap. 6, p. 273.

Holmes, J.K. 1982c ibid. chap. 5, p. 129.

Holmes, J.K. 1982d ibid. chap. 5, p. 121.

Holmes, J.K. 1982e ibid. chap. 6, p. 269.

Hwan, E. & Brown, R. January 1988 Microwave sources for digital radio. *Microwave Journal.*

Oberst, J.F. & Schilling, D.L. Feb 1971 The SNR of a frequency doubler. *IEEE Trans Com.Tech.* pp. 97-99.

Ondria, J. & Singleton, J A. 9th May 1988 Highly Temperature Stabilised K Band [18 - 26.5 GHz] Gunn VCO for High Capacity Radio Systems. *IEE Colloquium on Microwave Components in Telecommunications., London.*

Park, J.H. Jr. April 1978 Correspondance on Binary DPSK detection *IEEE Transactions on Communications.* Vol. Com-26, No. 4. p. 484.

Parker, T.E. 1985 1/f Frequency Fluctuations in acoustic and other stable oscillators. *39th Annual Frequency Symposium.* p. 97.

Prabhu, V.K., March 1976 PSK performance with imperfect carrier phase recovery. *IEEE Trans AES.* Vol. 12, No.2, pp. 275-285.

Robins, W. 1982a *Phase noise in signal sources,* chap3, p. 38. Peter Peregrinus

Robins, W. 1982b ibid, chap10, p. 251.

Robins, W. 1982c ibid, chap10, p. 251.

Robins, W.P. *Phase noise in signal sources,* chap.10, p. 262. Peter Peregrinus.

Sorep, 1989 SOR5053 Viterbi Decoder Integrated Circuit, In Data Communications data sheet, Sorep, France vol1 p63

Stroud, K.A. 1984 *Fourier series and harmonic analysis,* chap. 7, p. 107. Stanley Thornes

Surinder, K. July 1988 Local Oscillator Selection for Digital Satellite Communications. *Microwave Journal.* No 7, p. 129.

Viterbi, A.J. 1963 Phase locked loop Dynamics in the presence of Noise by Fokker-Planck techniques. *Proceedings of the IEEE convention.* Vol 51, no 12 p1737

Viterbi, A.J. 1966a *Phase locked loop coherent receiver design,* chap. 4, p. 112. McGraw-Hill.

Viterbi, A.J. 1966b, ibid, chap. 2, p. 33.

Wilson, M.P. & Tozer, T.C. Feb 1991 Computer simulation of SR diode comb generators. *RF Expo. WestProceedings, Santa Clara.*

Winters, J.H. January 1984 Differential Detection with Intersymbol Interference and Frequency Uncertainty. *IEEE Transactions on communications.* Vol Com32, No 1 p. 25.

7 Phase Noise and Spurious Considerations for SRD Circuits

7.1 Introduction

In order to predict the phase noise and spurious performance of a synthesised local oscillator, it is necessary to determine the response of any multipliers or phase locked oscillators used within. Chapter 5 discussed design guidelines in general for frequency multipliers and mentions the fact that step recovery diodes (SRDs) potentially offer low phase noise performance. This chapter expands the subject further by exposing various caveats that must be observed to obtain reliable performance with SRDs. Computer simulations are described here which enable predictions of SRD circuit performance; these demonstrate the fact, that under certain conditions, such circuits are capable of chaotic behaviour.

Classically, for frequency multiplication, the $20\log(f_{out}/f_{in})$ rule is applied to the phase noise and the amplitude noise component is assumed to be eliminated by the multiplication process. However this rule will not account for:-

1) Any excess noise added by the multiplier;

2) AM to PM conversion;

3) Subsequent phase locked loop response;

4) Parametric enhancement, or subharmonic phenomena.

These effects depend upon the actual multiplier configuration and cannot be readily determined by simple "rule of thumb". Two additional noise phenomena need to be considered:-

i) The effect of the multiplier on noise sidebands present on the reference signals;

ii) Indigenous noise sources to the multiplier circuit.

Both effects are important. The first case is particularly relevant to far-from-carrier noise and spurious signal specifications, and the second case to close-to-carrier noise specifications.

Although the SRD is capable of low phase noise frequency multiplication, performance can be impaired by apparently unpredictable effects if care is not exercised during the design process. In this chapter, the computer simulations and models used are described and, following this, stability problems are demonstrated by means of a time domain simulation. A fast Fourier transform (FFT) is then taken of the time domain simulation to illustrate the effects of stability problems on phase noise in the frequency domain. It will be shown here that SRDs are capable of showing chaotic behaviour. This leads to a discussion of how the observed chaotic behaviour relates to recursion theory and ultimately to an extension of the SRD simulation program which can rapidly evaluate comb generator stability.

Further extensions of the program are described which enable investigation of the effect of carrier lifetime fluctuations and self bias levels upon SRD phase noise. Finally an SRD comb generator circuit is described; this comb generator was constructed so that the effects discussed in this section could be measured.

7.2 Effects of frequency multipliers on phase noise

In all cases of frequency multiplication involving one source (coherent) the phase noise at the input is increased by a theoretical minimum of $20\log(f_{out}/f_{in})$ at the output [Grebenkemper, 1982]. The offset from carrier frequency will be unchanged and, unless the noise sidebands become so great that the small angle criterion is violated, the spectral profile will remain unchanged. The $20\log(f_{out}/f_{in})$ ratio represents the best that can be achieved with a noise free multiplier and, in addition to this, in practice there will be noise internally generated from the multiplier known as "excess noise" [Manassewitsch, 1985a].

Whereas there is an absolute minimum level of phase noise degradation, which is a fundamental property of frequency multiplication, the response to AM noise depends upon the configuration of the multiplier [Kroupa, 1973a]. A circuit with a small signal

polynomial response will raise the AM noise also by 20log (f_{out}/f_{in}). If there is a limiter associated with the multiplier then the increase will be very much less than this. However some multipliers convert the amplitude noise to phase noise by AM to PM conversion. This can result in unexpectedly large amounts of phase noise being produced. Chapter 5 mentions the fact that reactive multipliers are worse in this respect. In addition, reactive multipliers tend to be more prone to subharmonic and chaotic phenomena. However, a particular reactive multiplier using a SRD can be both simple and efficient; therefore this merits particular attention.

7.3 Step Recovery Diode (SRD)

7.3.1 Characteristics of SRD's

SRDs are chiefly used as impulse generators or as frequency multipliers. Their ability to switch rapidly is almost universally exploited in their application. An impulse generator outputs narrow pulses, and is often referred to as a comb generator because of the frequency domain representation of such an impulse as a comb of steadily decreasing harmonics. Frequency multiplication refers to a circuit with a resonance at the output thus enabling concentration of the output energy at a single output frequency rather than at a broadband comb of frequencies. The circuit that will be discussed here will be the comb or impulse generator.

The SRD is well covered in the literature [eg Hewlett-Packard, 1969], and particularly with reference to frequency multipliers [Pontius, 1967] [Lean, 1978] [Hamilton & Hall, 1967a], although literature on the use of SRDs in phase locked loops is scarce, and little is written about the phase noise performance.

Briefly the step recovery diode has a doping profile as displayed in fig7.1. and a capacitance voltage characteristic as displayed in fig7.2. Step recovery diodes consist of a PIN junction with a doping profile such that charge carriers can accumulate in the intrinsic layer during conduction. Unlike normal diode rectification, the charge stored during conduction must be depleted during reverse bias before conduction can cease. In the forward conduction mode charge carriers are injected into the depletion region and the diode displays very low resistance. When the drive voltage reverses, the carriers are swept out of the intrinsic region. When charge carriers accumulate in the intrinsic region after conduction, there will be a finite time before all carriers are removed.

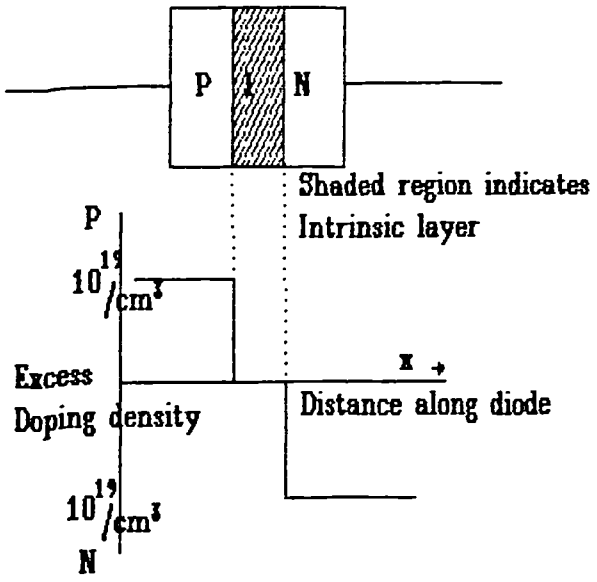


Fig 7.1 Doping profile of step recovery diode

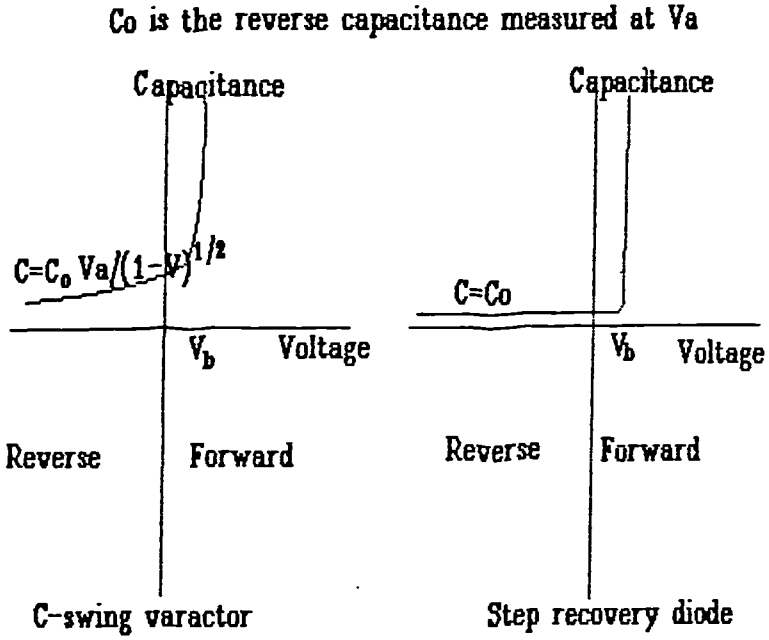


Fig 7.2 Capacitance voltage characteristic of a varactor and a SRD

When these carriers are removed from the intrinsic region, the mechanism for current flow in the diode is removed, and the diode characteristics resemble a reverse biased diode. Essentially, the diode shows two distinct modes of operation, the conduction mode and

the impulse, or reverse bias, mode. On conduction the diode displays a low impedance resembling that of a large capacitor. In the reverse biased mode, diode capacitance is very low, and shows little capacitance variation with applied current or voltage.

The step recovery effect was originally discovered by Boff and Moll in 1960 [Boff, 1960]. Since then, a great deal of design effort has been invested to optimise the speed of transfer between reverse recovery high current flow and reverse bias low current flow [Watson, 1969]. In order to control reverse bias capacitance changes the intrinsic region is in fact very lightly doped [Siemens, 1987].

7.3.2 Applications of SRD

SRDs find applications in frequency multipliers, impulse generators, microwave sampling devices for Phase locked oscillators (PLOs) and time domain devices. Their applications in PLOs are widespread, such frequency sources being the backbone of most communications systems. In addition the property of generating large numbers of harmonics enable them to find use in frequency synthesis.

All these applications exploit the devices' ability to switch rapidly between the high current reverse recovery phase and the low current reverse bias phase. This rapid transition enables the device to produce pulses with rapid transitions which can be measured in 10's of picoseconds. Large multiplication ratios are capable of being realised in a single step by virtue of the step recovery diode's property of rapid transition, which represents the single most important property of the SRD.

7.3.3 The SRD as a means of frequency multiplication

Fig 7 3 gives a typical circuit diagram of an SRD impulse generator, and fig7.4 displays the resulting waveforms.

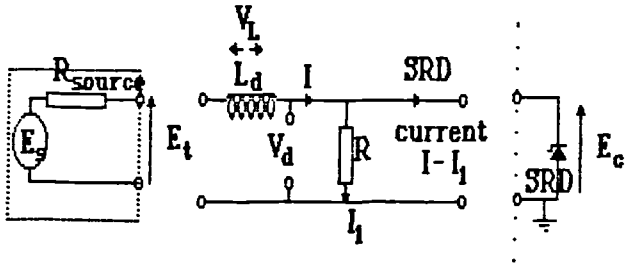


Fig 7.3 Circuit diagram of SRD impulse generator

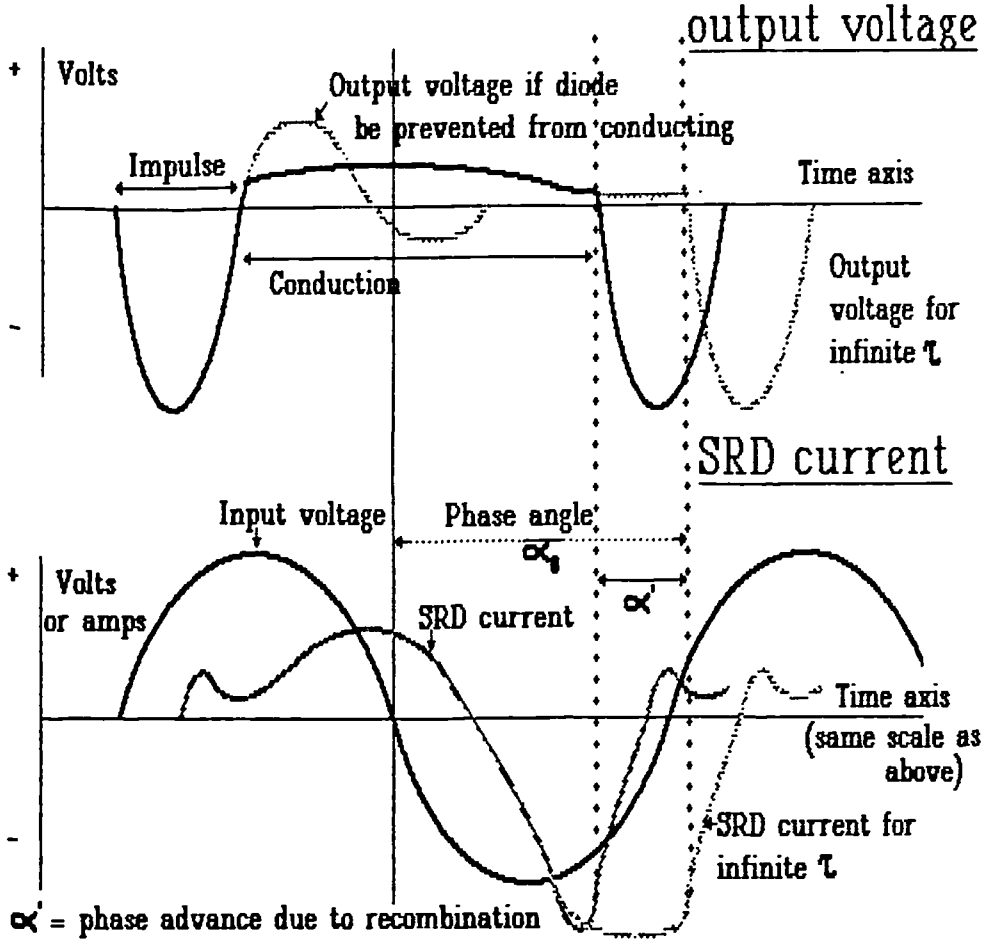


Fig 7.4 Current and voltage plots for a SRD comb generator

Fig 7.3 is the simplest circuit possible to generate a comb of harmonics. It consists of a small inductance, the impulse inductance L_d and a load resistance R_x. An equivalent circuit is shown in dotted lines consisting of the diode bulk resistance R_d and diode junction capacitance C_d. As outlined in §7.3.1, there are two parts to the cycle, the conduction mode and the impulse mode. During the conduction mode, the effective value of C_d is virtually infinite, therefore giving the diode a low impedance at its terminals. When the transition to the impulse mode occurs, C_d suddenly drops to its low reverse value, therefore the diode terminal impedance suddenly rises. This sudden abrupt change in current flow can be as high as 10^9 amps per second. Any inductance present, such as the drive inductance L_d results in large voltage spikes as in fig7.4. The resulting sharp spike results in spectral energy being present at frequencies of >100 GHz. A damped resonant circuit is formed from a combination of drive inductance, diode capacitance, and load resistance, and the output voltage begins to ring as shown in the top half of fig7.4. If reversion to the conduction mode could be prevented, then the output voltage would continue to ring as shown by the dotted line. When the forward barrier voltage of the diode is exceeded, however, the diode begins to conduct. Damping of the waveform is altered due to the very low on resistance of the diode. The ringing waveform becomes

severely overdamped, resulting in a relatively long decay time of the SRD voltage after this point.

A critical factor in determining the phase noise characteristics of the comb generator is the conduction angle α. This is the angle between the reversal of the input drive voltage and the start of the impulse region and is therefore determined by the time interval required in order to remove accumulated carriers in the intrinsic layer. There are two mechanisms for removal of this accumulated charge: diffusion and recombination. With diffusion, as many charge carriers flow out of the layer as was introduced, so the mean current flow is zero, therefore there is no rectification. With recombination, the accumulated charge recombines at a rate determined by the carrier lifetime τ. Any carriers that are lost due to recombination must be made up by current flow from the supply, hence a small DC current flows; carrier recombination therefore results in rectification.

In the normal operating mode of the SRD, carrier lifetime τ is long compared with an input cycle period therefore the DC current flow due to rectification will be only a small fraction of the AC current.

The differential equation for the impulse period can be shown to be of the form:-

$$x(t) = L_d C_d \frac{d^2 V_c}{dt^2} + R_x C_d \frac{dV_c}{dt} + V \tag{7.1}$$

where x(t) is the driving waveform and V_c is the voltage across the capacitor. The free response of the circuit can be shown to be:-

$$V_c(t) = \frac{I_p}{2C_d\beta}\left(e^{-(A-\beta)t} - e^{-(A+\beta)t}\right) \tag{7.2}$$

where A and β are given by:-

$$A = \frac{1}{2R_x C_d} \qquad \beta = \frac{1}{2}\sqrt{\left(\frac{1}{R_x C_d}\right)^2 - \frac{4}{L_d C_d}} \tag{7.3}$$

If β is imaginary then equation (7.2) becomes:-

$$V_c(t) = \frac{I_p}{C_d\beta} e^{-At} \sin(\beta t) \tag{7.4}$$

or if β is zero then equation (7.2) becomes:-

$$V_c(t) = \frac{I_p t}{C_d}\left(\exp\left(\frac{-t}{2R_x C_d}\right)\right) \tag{7.5}$$

These equations explain the steep rise during the impulse period. As the value of β increases, the pulse becomes wider.

The implementation of the step recovery diode in a phase locked loop or as a multiplier has been described in chapter 4. In the present chapter, spurious and noise generation properties will be examined. During the course of several months of work with SRD comb generators it became apparent that although the device is capable of low phase noise harmonic generation, under certain circumstances the phase noise can be severely degraded. In addition it became apparent that subharmonic phenomena can suddenly appear. A manual on the subject of harmonic generators [Hewlett-Packard, 1969] suggested that the bias circuits may be responsible for the subharmonic generation. However, we confirmed by measurement that even if all resonances are removed and the device is operated at zero bias, subharmonic phenomena can still appear.

The remainder of this chapter will analyse this effect and the variation in phase noise levels. Many parameters have potential to affect the level of phase noise, we therefore investigated these effects using computer simulation techniques. In particular, an attempt is made to establish whether the subharmonic phenomena can degrade phase noise.

7.4 Step recovery diode phase noise

7.4.1 Phase noise mechanisms

Extensive literature searches failed to reveal an analysis of the phase noise of the SRD multiplier, therefore one was investigated by the author.

Upconversion of noise from the input frequencies to the output frequencies is governed by the Manley-Rowe relationships [Manley& Rowe, 1956]:-

$$v(t) = \sum_{m=-\infty}^{+\infty} \sum_{n=-\infty}^{+\infty} V_{(m,n)} \exp\left(j\{m\omega_i + n\omega_{ref}\}\right) \tag{7.6}$$

$$i(t) = \sum_{m=-\infty}^{+\infty} \sum_{n=-\infty}^{+\infty} I_{(m,n)} \exp\left(j\{m\omega_i + n\omega_{ref}\}\right) \tag{7.7}$$

where ω_{ref} is the input carrier frequency and v(t) and i(t) represent the voltage and currents through a non-linear reactance. These define a Fourier series that consists of a series of harmonics with sidebands at frequency $\pm\omega_i$ offset from carrier. Idler frequency is the term that commonly refers to the ω_i frequency. The Manley-Rowe relationships predict that an extra input signal of either at frequency offset ω_i from carrier, or at a baseband frequency of ω_i, will result in sidebands at offset from carrier frequency $\pm\omega_i$ at the harmonics of the frequency ω_{ref}. This upconversion effect will also apply if the sidebands are replaced by noise.

The sources of noise are [Watanabe & Fakatsu, 1967]:-

1)	Additive thermal noise	white
2)	Avalanche noise	white
3)	Microplasma noise	$1/f^2$
4)	Recombination noise	$1/f$
5)	AM to PM noise	$1/f$ and white.

The signal levels at the input to the multiplier are generally large (eg, +20dBm) so that the additive thermal noise is small compared with the signal (eg, -160 dBc/Hz at 5GHz output frequency). Noise performance is, however, critically dependent upon signal level [Scherer, 1981a].

Avalanche breakdown results in high levels of white noise [Watanabe & Fakatsu 1967] if the firing voltage peaks are excessive due to high drive levels. Microplasma noise can result in an f^{-2} relationship with offset frequency; this in turn causes excessive close to carrier phase noise. If the drive level is optimised for maximum output power, the phase noise may be increased due to breakdown effects. It has been reported for example [Scherer, 1981a] that a 500MHz multiplier specified for +27dBm drive level was found to give optimum noise performance at +24dBm.

Recombination noise occurs as a result of statistical variations in carrier lifetime. Watanabe [*ibid*] suggested that a higher level of noise was generated in a varactor when forward conduction occurs. McDade [1966] confirmed that higher noise levels were generated when significant rectification occurred. This prompted an investigation here as to the possible influence of carrier recombination effects on the noise level. Statistical fluctuations in carrier recombination result in variation in the effective carrier lifetime, τ.

In the intrinsic (I) layer, some of the carriers recombine rather than become swept out of the layer; as a result, more carriers are swept into the intrinsic layer during the forward conduction than are swept out during reverse recovery. Some rectification takes place, and a small DC current, I_{dc}, flows. The percentage of carriers that recombine in a cycle of input can be calculated [Hewlett-Packard, 1969], giving the average storage time as: $t_a = 1/2f_{ref}$, where f_{ref} is the input drive frequency. DC current flow is determined by $I_{dc} = I_{pac}/\omega_{ref}\tau$, where I_{pac} is the peak AC current.

This recombination results in a reduction in the charge that must be removed from the I layer. A premature termination of the recovery period therefore results. The ratio of charge lost in the recovery period q_0 to the total charge q_t is:-

$$\frac{q_0}{q_t} = \frac{2\pi}{\tau\omega_{ref}} \tag{7.8}$$

Assuming that the recovery current is approximately constant around the impulse time, then the ratio of charge lost to total charge is equal to the ratio of phase advance α' to the firing angle α_o. Charge loss indicates the fraction of a cycle that the impulse point has moved, therefore α_o is a constant representing the value of α corresponding to infinite lifetime:-

$$\alpha = \alpha_o\left(1+\frac{1}{f_{ref}\tau}\right) \tag{7.9}$$

In predicting phase noise, statistical variations in carrier lifetime are assumed to occur. To simplify the analysis, sinewave variations in τ will be considered. The instantaneous value of τ, $\tau(t)$, will be:-

$$\tau(t) = \bar{\tau} + \sqrt{2}\upsilon\tau \sin \omega_m t \tag{7.10}$$

where ω_m is the effective frequency of the noise, υ is the fraction of the RMS statistical variations in τ to τ and $\bar{\tau}$ is the mean value of τ. By differentiating 7.9, the conversion factor can be found from τ variations to α variations:-

$$\frac{d\alpha}{d\tau} = -\left(\frac{\alpha_o}{f\tau^2}\right) \tag{7.11}$$

The RMS fluctuations in α, $\Delta\alpha$ can be found from substituting the RMS fluctuations in τ from equation (7.10) into equation (7.11), giving:-

$$\Delta\alpha = -\left(\frac{\alpha_o\upsilon}{f\tau}\right) \tag{7.12}$$

These RMS fluctuations in α represent the value of phase noise introduced by carrier lifetime fluctuations and therefore the phase noise introduced by a step recovery diode due to recombination, provided $f_{ref} >> 1/\tau$.

7.4.2 Effect of biasing

Fig 7.5 displays a method of self biasing the SRD. If self bias were used to enhance the

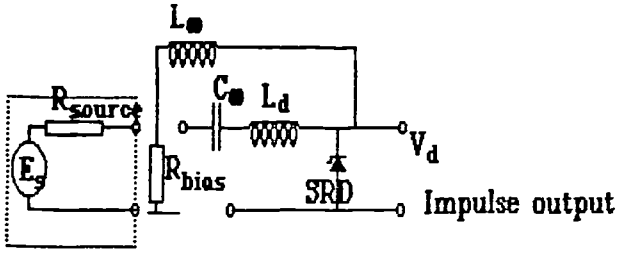


Fig 7.5 Circuit of SRD impulse generator showing biasing

output power of the multiplier, the value of the bias voltage would vary due to changes in the recombination current I_{dc}. This current is determined by τ, the carrier lifetime. τ fluctuates as a predominantly *1/f* process [Buckingham, 1983], therefore the value of self-bias voltage will also fluctuate. Firing angle variation occurs as a result of its dependence upon the lifetime, and flicker phase noise is therefore generated. The relationship between bias voltage and firing angle is [Hamilton & Hall, 1967b]:-

$$E_c + \phi = E \sin\left(\alpha_o - \pi\omega\sqrt{\frac{4R_d^2 L_d C_d^2}{4R_d^2 C_d - L_d}}\right) \qquad (7.13)$$

where E_c is the bias voltage, ϕ is the diode junction barrier potential, E is the applied signal voltage, C is the reverse capacitance of the diode, L_d is the driving inductance, and R_d is the load resistance.

7.4.3 AM to PM conversion

This is another principal mechanism for phase noise generation in SRD multipliers. A variation in amplitude of the drive signal results in some variation in the firing angle [Hamilton & Hall 1967b] and might arise from mutual conductance variation due to *1/f* effects in the driver transistor. A computer simulation as described later in this chapter could aid the selection of an optimum amplitude and wave shape of the drive waveform for minimum AM to PM conversion.

7.4.4 Subharmonic phenomena: parametric oscillation or chaos?

The negative real admittance component of a device that displays non-linear capacitance voltage effects is [Manassewitsch, 1985b]:-

$$G = \frac{-\pi f_o n C_v}{n+1} \tag{7.14}$$

where n is determined by the junction properties of the diode used ($n = \frac{1}{2}$ for abrupt junction diodes).

The voltage capacitance for a junction diode can be described as:-

$$C(v) = K_s\left(\frac{\phi - V_s}{\phi - V}\right)^n \tag{7.15}$$

where C_d is the capacitance measured at some DC voltage V_d and ϕ is the diode contact potential (approximately 0.7 V). With a step recovery diode, the capacitance voltage curve is extremely steep, resulting in a large n value. Therefore if $n \rightarrow \infty$, then:-

$$\left(\frac{n}{n+1}\right) \rightarrow 1 \tag{7.16}$$

and equation (7.14) becomes:-

$$G = -\pi f_o C_V \tag{7.17}$$

The presence of this negative conductance indicates that the device is susceptible to oscillation. These oscillations are often called parametric oscillations by analogy with reactance swing varactors [Prabhu, 1967]. There are problems however in using this equation to determine stability: negative resistance is essentially a small signal parameter, and cannot be easily fitted to the heavily non-linear operation of the SRD multiplier/comb generator.

It has been suggested [Hewlett-Packard, 1969] that the presence of resonances in the band at which the negative resistance exists is the cause of parametric instabilities. These resonances are called idler resonances. Apart from the instability problem, any gain in the system must be investigated as this implies the possibility of raising the level of noise in the system. Any such noise level increase may have adverse effects upon phase noise level. SRD comb generators do exhibit parametric gain [Hewlett-Packard, 1969], and this can increase the noise level already present. Kwitkowski, addressing the problem of stability of power amplifiers [Kwitkowski, 1988], suggested the addition of a low level carrier from a sweep generator. An alternative is to use additive broadband noise and this

was employed during the measurements described in §7.11. Such noise peaking effects are also simulated in software with random noise values added to the driving waveform as described in §7.7.

It has been observed, however, from practical work with SRDs that it is possible to obtain parametric instabilities even when there were no idler circuit elements intentionally designed into the circuit. The assumption that idler elements are necessary may be as a result of an over simplistic consideration of negative resistance effects only. Parametric effects may be analysed in terms of non-linear differential equations. However these non-linear differential equations are capable of showing chaotic behaviour. Such unstable chaotic behaviour is described in §7.8 below. M I Sobhy *et al* [1990] suggested that any driven second order nonlinear system is capable of chaotic behaviour. Even the basic SRD impulse circuit of fig7.3 is of this form. It could however be argued that parametric oscillations are a specific manifestation of a more general effect known as chaos. This suggests that the subharmonic phenomena may be associated with the operation of the device as an impulse generator, rather than due to any externally applied circuitry such as bias circuits or other resonant circuits. Various authors [Vidkjaer, 1976], [Bernard & Neau 1990] have found that subharmonic phenomena most frequently occur at either close to carrier or at half carrier frequency.

Because of the complicated behaviour of the SRD comb generator circuit it was considered necessary to produce a computer simulation in order to guarantee correct functioning. Models had to therefore be developed to enable simulation. In this manner, several iterations of component values could be assessed in terms of stability. The following section will describe the methods used.

7.5 Computer simulation of SRD circuit

7.5.1 Modelling

The models to be used in this simulation are based on the networks displayed in fig7.6, and fig7.7. The circuit elements were taken from papers by Krakauer [1962] and Friis [1967]. Friis illustrates the actual models used for the diode. In the dotted areas are circuit elements used to simulate the diode. Modelling is accomplished by splitting the reference cycle into two parts: the impulse part, and the conduction part. Fig7.6 displays the equivalent circuit of the simplest SRD comb generator, ie. with no means of impedance matching at the input. Circuit **a** is the actual circuit simulated, and C_∞ and L_∞

are effectively infinite value components used for self bias purposes. L_d is the impulse inductance, and V_d is the output impulse voltage. In the conduction mode, circuit **b** displays the equivalent circuit with the SRD represented by a voltage source V_{bar}, and a forward resistance R_f.

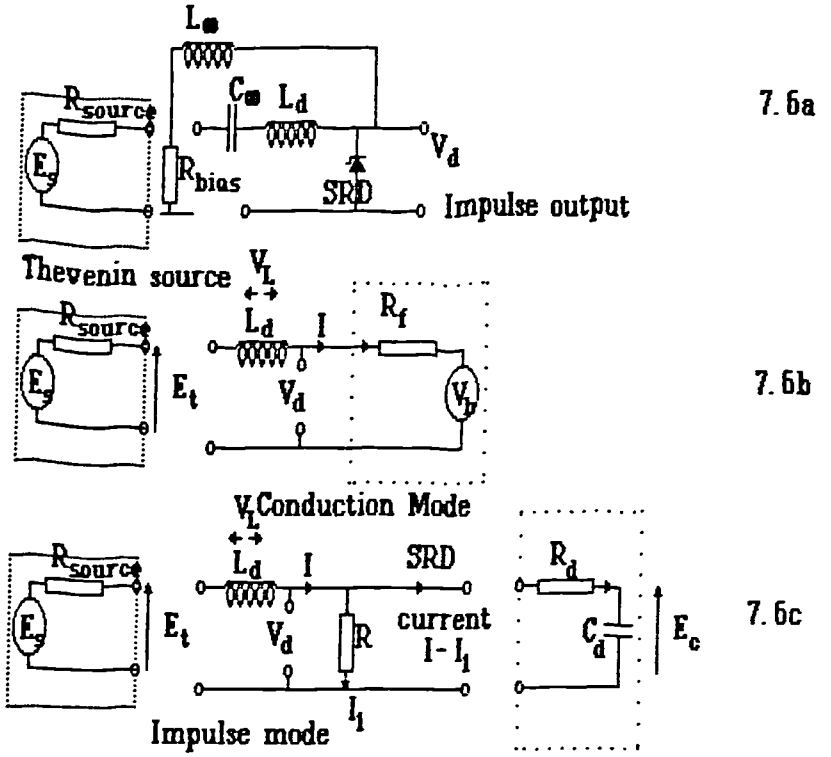


Fig 7.6 Step recovery diode equivalent circuits used in simulation, network 1

In the reverse mode, circuit **c**, the forward voltage source, V_{bar} is replaced with the the reverse junction capacitance, C_d. The drive voltage is assumed to have a source resistance, R_{source}.

A problem with this simple comb generator circuit is that the input impedance R_{source} must be small or the damping effect on the drive inductance would be such that the impulse output voltage would be limited. To overcome this problem the matching transformer and reflection capacitor circuit of fig7.7 is introduced. The problem of the source impedance damping the impulse inductance is solved by introducing the reflection capacitance C_2, and the impedance matching transformer secondary inductance L_2.

Although the model for the conduction part is different from that of the reverse part, the conduction model can be built with the same nodal elements as used in the reverse model. This can be achieved by setting the diffusion capacitance to infinity, and the stored voltage constant at the barrier voltage. Therefore an identical network is built for both cases. In

order to solve the network behaviour, differential equations are built from the current and voltage relationships for each of the elements [Kuo, 1966].

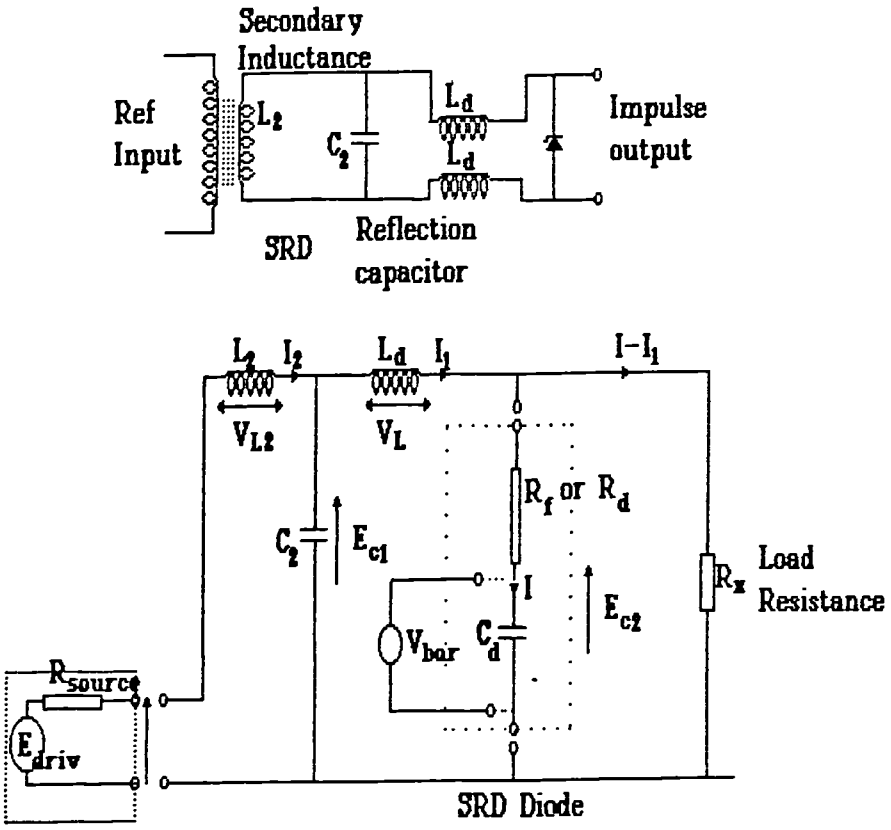


Fig 7.7 Step Recovery Impulse Generator and Matching Transformer, network 2

The relationships for the resistive elements is Kirchhoff's law, and the voltage V_L across the inductor L is given by:-

$$V_L = -L\frac{dI}{dt} \tag{7.18}$$

Inductor current I due to applied voltage V_L is given by:-

$$I = L\int_{t(n-1)}^{t(n)} V_L.dt \tag{7.19}$$

For the case of a capacitive element C, the current through the capacitor as a function of applied voltage V is given by:-

$$V_L = C\frac{dV}{dt} \tag{7.20}$$

Expressing current I in terms of applied voltage V is:-

$$V = \int_{t(n-1)}^{t(n)} \frac{I}{C} dt \qquad (7.21)$$

The drive waveform can be any repetitive waveform, but a sinewave is most frequently specified:-

$$E_{driv} = E_{pk} \sin(2\pi f_r t) \qquad (7.22)$$

where E_{driv} is the source voltage at any instant t., R_s is the source equivalent output resistance (in fig7.7), L2 is the driver transformer output inductance, C_1 is the impulse reflection capacitor and L_d is the impulse inductance. The conduction angle α is represented by the phase of the reference cycle at the termination of the conduction part of the simulation.

Another factor that must be included is the breakdown voltage of the SRD junction. When the voltage across the diode exceeds the avalanche voltage in the impulse part of the cycle, the diode impedance drops to a low value. In the simulation this is represented by limiting the voltage across the diode to the avalanche voltage.

Conduction analysis commences when the SRD is forward biased, and finishes when all the charge carriers are swept out of the intrinsic layer. Fig7.6b shows the model used for the conduction phase. The diode equivalent circuit consists of a resistor representing the junction bulk resistance in series with a battery representing the barrier potential of the SRD junction.

In the impulse part of the cycle, the SRD model is represented as in fig7.6c. This consists of the junction capacitance C_d, the reverse bias diode loss, R_d and the load R_x. Termination of the impulse phase is made to occur when the voltage across the equivalent junction capacitance exceeds the barrier voltage V_{bar}.

So far, in the model, the lifetime of carriers in the forward part of the cycle was assumed to be infinite. Allowance therefore must be made for a finite lifetime. The charge carriers injected into the diode during forward conduction are assumed to decay with a time constant τ. Total charge will decay according to [Grove 1967]:-

$$q = q_o \exp\frac{-t}{\tau} \qquad (7.23)$$

7.5.2 Choice of simulation method

There are many techniques used for simulation of electronic circuitry. The most commonly used are [Obregon, 1990]:-

i) Linear frequency domain

Solution of linear impedance networks;

ii) Harmonic balance technique

Uses method 1 with the non-linear elements lumped together and solved in the time domain;

iii) Volterra series

Expresses the non-linear transfer function of the system as a sum of a polynomial series;

iv) Describing function

Essentially 1 modified to use the large signal admittance coefficients in the networks;

v) Time domain analysis

Step by step solution of integro-differential equations.

i) Linear analysis is the process of forming and solving the admittance matrix for the system in the frequency domain. The analysis can give rapid results, but is not suitable when it is necessary to analyse non linear effects.

ii) A hybrid of the linear and non linear methods has been devised, known as the harmonic balance technique. As a steady state solution only is produced, this method is not suitable if the transient response is required. The linear components of the network are abstracted and analysed in the frequency domain. This leaves the non linear elements which must be analysed in the time domain. Equations are formed for each of the harmonics in the Fourier series for the time domain network. Applications are for mainly determining the operating points of amplifiers and oscillators so that factors such as compression points or harmonic output can be determined. This is not suitable for strongly non linear systems such as SRD multipliers where the frequency domain network cannot be determined.

iii) Analysis by Volterra series involves the representation of the network initially as its linear transfer function. In parallel with the linear network is a series of networks

having transfer functions of ascending order up to an order n to represent the non linearity of the system. This is equivalent to a Fourier series representing a signal as a series of up to order *n*. If the network is strongly non linear, such as with the SRD circuit, the value of n required before transfer function h(*n*) becomes insignificant is large. As a result of a large number of transfer functions being required, insuperable computational problems arise.

iv) The describing function method defines a large signal admittance matrix alongside the small signal. Circuits such as transmitter output stages, where the large signal characteristics can be measured at several different operating points, are most suitable for analysis by the describing function method. Extrapolation can then be used to find the correct large signal characteristics. This method is not suitable for broadband cases where large series of harmonics are generated as its accuracy depends upon the filtering of the harmonics.

v) In time domain simulation, the integro-differential equations are formed for the system and solved on a step by step basis. A classic example of this is the transient analysis mode of the Spice simulation system. The frequency domain can be obtained from the time domain by means of a fast Fourier transform (FFT) after the initial transient condition has elapsed. Although time domain analysis can be very demanding in terms of computational effort, it has many advantages when the steady state mode of operation cannot be assumed, or the non-linearities dominate the transfer function of the circuit. It is for this reason that time domain analysis was selected for study of the SRD circuit.

7.5.3 Time domain simulation

A time domain simulation involves solution of the system differential equation over discrete time intervals. Such a simulation could be either non-linear or piecewise linear. Time domain simulations have one great drawback, however; recursion. A recursive formula is used to derive the present time step results from the previous. Recursive formulae can show the kind of chaotic instability that we are attempting to demonstrate in this chapter with SRD's. It was vital, therefore, that the algorithms were investigated for stability before use in the simulation. One test that can be applied to gain confidence in the simulation results is to vary the time step.

With a non-linear simulation, at each step, non-linear relationships are assumed and the problem is solved by iteration [Calahan, 1971]. The Spice transient simulation uses this method [Nagel, 1975]. A problem with this method is that stability of solution cannot be guaranteed [Meares, & Hymowitz, 1988], especially in the presence of noise. By assuming that the system is linear over each time step it is possible to arrive at a method

that is less accurate but more reliable in terms of stability [Gear, 1971]. Such a method is known as a piecewise linear method.

The simplest method of piecewise linear differential equation solving is the Euler method [Stroud 1990]. With this method, the differential equation:-

$$\frac{dy}{dt} = f(t,y)) \tag{7.24}$$

is written as a difference equation:-

$$y_n = y_{n-1}+\Delta t\ f(t_{n-1},y_{n-1})) \tag{7.25}$$

This is now recursive, as y_n will become y_{n-1} for the next time step.

A problem with the forward Euler technique is that stability is conditional on the time step, and this is precisely the condition that must be avoided. However, Badger [1988] has applied the more stable backward Euler technique to a transient analysis of the Phase Locked Loop (see chapter 5):-

$$y_n = y_{n-1}+\Delta t\ f(t_n,y_n)) \tag{7.26}$$

In this manner, equation (7.21) describing the voltage stored in capacitance C can be converted to:-

$$y_n = y_{n-1}+\Delta t \frac{I_{n-1}}{C} \tag{7.27}$$

By using this method of approximation, the resultant integration of the current through capacitance C is as displayed in fig7.8. The value of I_n is assumed constant from timestep t_{n-1} to t_n.

Therefore, if a steep gradient is encountered for di/dt, a large error will result. Errors introduced by the Euler method can be shown to be of the form [Dalquist & Bjorck, 1974a]:-

$$y(x,\Delta t) = y(x) + \Delta t\, c_1\,(x) + \Delta t^2 c_2(x) + \Delta t^3\, c_3(x)+..... \tag{7.28}$$

where the expressions containing Δt constitute the error of one step and c_1, c_2 ....etc. are constants.

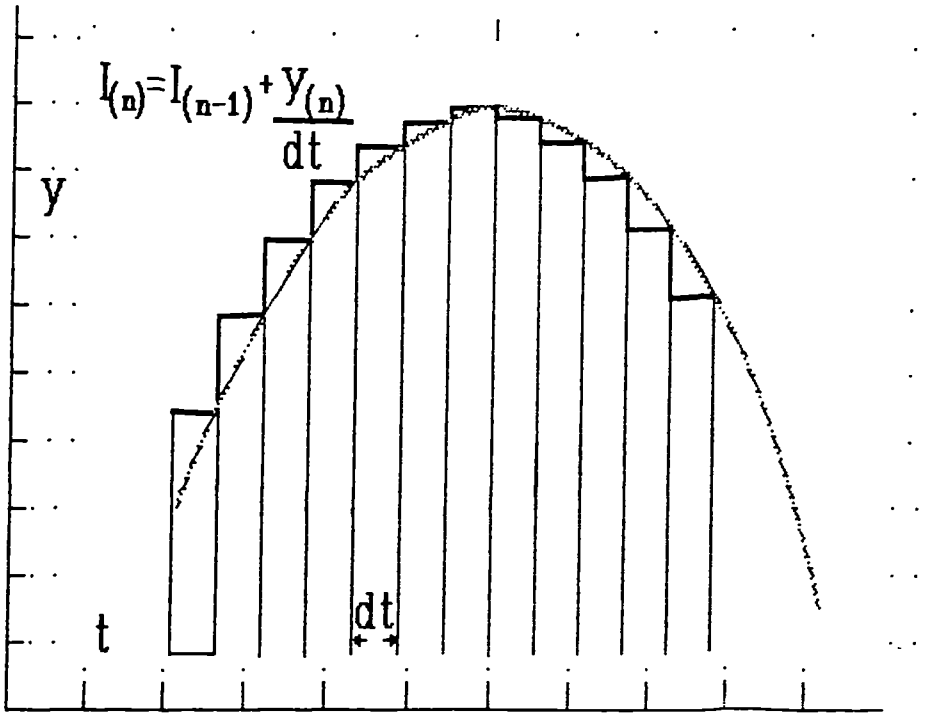


Fig 7.8 Piecewise linear time domain simulation with first order polynomial approximation to the integration

If instead, however, the value of I_n is not assumed constant, but a trapezoidal approximation is carried out to equations (7.19) and (7.21), then a considerable improvement in accuracy is possible. This can be observed from fig7.9 showing a much closer fit to the curve in this case.

The formula for trapezoidal integration is:-

$$y_n = y_{n-1} + \frac{\Delta t}{2} f(t_{n-1}, y_{n-1}) + \frac{\Delta t}{2} f(t_n, y_n) \tag{7.29}$$

giving for equation (7.21):-

$$V_n = V_{n-1} + \frac{\Delta t}{2}\frac{I_{n-1}}{C} + \frac{\Delta t}{2}\frac{I_n}{C} \tag{7.30}$$

The error for the integration approximation can be shown to be:-

$$y(x,\Delta t) = y(x) + \Delta t^2 c_1(x) + \Delta t^3 c_3(x) + \Delta t^4 c_4(x) \ldots\ldots \tag{7.31}$$

By eliminating the Δt term present in equation (7.28), considerable improvement in accuracy can be gained. Implicit integration methods are used since in general they give more reliable results than explicit methods such as the Runge Kutta method [Nagel, 1975]. The method is called implicit integration because the integration appears on the right hand side of the equation.

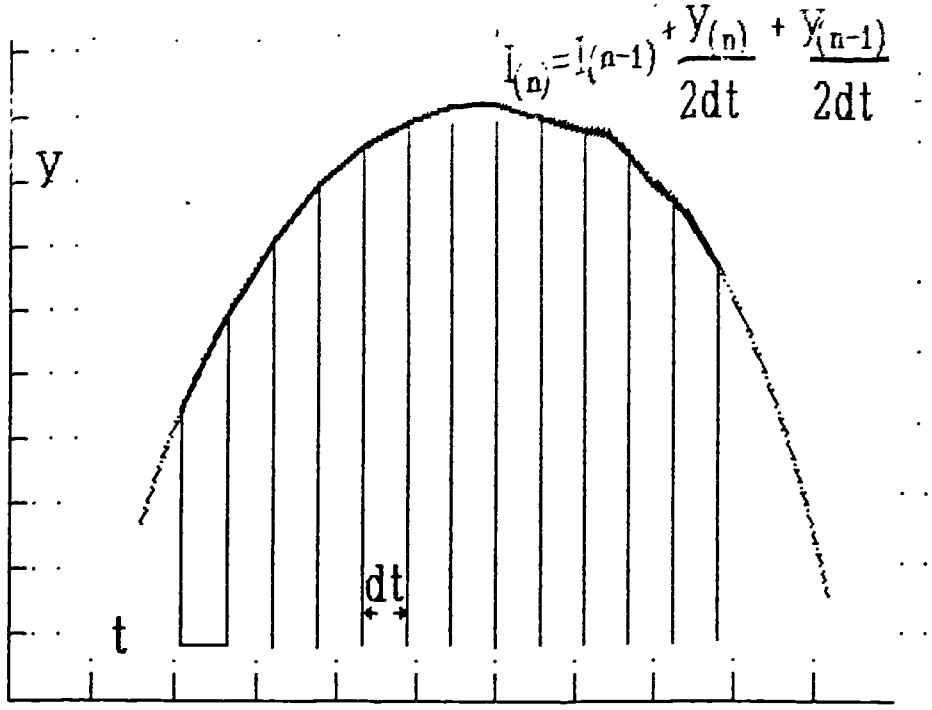


Fig 7.9 Second order polynomial integration approximation (Trapezoidal) improves accuracy

Trapezoidal integration is a polynomial integration of order 2. This is the maximum order for an A-stable integration that is easy to implement. A-stability describes an algorithm that is stable if the solution is stable [Dalquist & Bjorck, 1974]. It is possible to reduce the truncation error by the use of a higher order integration approximation. A method of improving the truncation error by performing 3 trapezoidal integrations of different time steps and extrapolating to a zero time step was devised by the author. This was effectively a fourth order method, and would normally provide an increased accuracy of several orders of magnitude. However, this method is conditionally stable and would require careful control of the time step. It was considered that this trade-off of reliability against accuracy was not acceptable and therefore discarded in favour of the simple trapezoidal method.

There can be difficulties with single step trapezoidal integration if the eigenvalues of the approximation equations are near the imaginary axis. Such an occurrence is likely if a resonant circuit has a natural frequency around the inverse of the time step and a small

damping factor. In this case, the integration is operating near the limits of stability, and the solutions at each time-step oscillate around the correct value. An example where this may result is in allowing for diode package inductance, giving rise to what is known as a "stiff" set of differential equations. The cure may lie in the use of Gears [1971b] multi-step methods which are stable for such stiff problems. Device package parasitics were not included in the simulation described here, but are recommended for further research work into comb generator simulation.

A diagram of the SRD embedded in a comb generator circuit is shown in fig7.7. The network current and voltage variables are also shown. There are 5 elements in this network, requiring 5 equations for the network. Applying the trapezoidal integration rule to the reactive elements yields the following four equations:-

$$I_2 = I'_2 + \frac{\Delta t}{2}\frac{V'_{L2}}{L_2} + \frac{\Delta t}{2}\frac{V_{L2}}{L_2} \tag{7.32}$$

$$I_1 = I'_1 + \frac{\Delta t}{2}\frac{V'_{L1}}{L_1} + \frac{\Delta t}{2}\frac{V_{L1}}{L_1} \tag{7.33}$$

$$E_{C1} = E'_{C2} + \frac{\Delta t}{2}\frac{(I'_2 - I'_1)}{C_1} + \frac{\Delta t}{2}\frac{(I_2 - I_1)}{C_1} \tag{7.34}$$

$$E_{C2} = E'_{C2} + \frac{\Delta t}{2}\frac{I'}{Cd} + \frac{\Delta t}{2}\frac{I}{Cd} \tag{7.35}$$

It is necessary to define a link between sections of the network, so that a non-singular system of simultaneous equations can be formed. Applying Kirchhoff's laws to the network gives the following equations for V_{L1} and V_{L2} which can be substituted into equations (7.32) and (7.33):-

$$V_{L2} = E_{driv} - I_2 R_s - E_{c1} \tag{7.36}$$

$$V_{L1} = E_{C1} - V_d \tag{7.37}$$

The resulting five simultaneous linear equations can be formed into the linear system:-

$$\mathbf{B} = \mathbf{A}\,\mathbf{x} \tag{7.38}$$

and thus solved for x. The components of equation (7.38) are:-

$$\mathbf{x} = \begin{bmatrix} I_2 \\ E_{C1} \\ I_1 \\ V_d \\ I \end{bmatrix} \tag{7.39}$$

$$A = \begin{bmatrix} 2L_2+R_S\Delta t & \Delta t & 0 & 0 & 0 \\ -\Delta t & 2C_1 & \Delta t & 0 & 0 \\ 0 & -\Delta t & 2L & \Delta t & 0 \\ 0 & 0 & R_L & -1 & -R_L \\ 0 & 0 & 0 & 2C_d & -(2CR_F+\Delta t) \end{bmatrix} \quad (7.40)$$

$$B = \begin{bmatrix} 2L_2I'_2 + (V'_L + E_{driv})\Delta t \\ 2CE'_{C1} + (I'_2 - I'_1)\Delta t \\ 2LI'_1 + (E'_{C1} - V'_d)\Delta t \\ 0 \\ 2C_dE'_{C2} + I'\Delta t \end{bmatrix} \quad (7.41)$$

This could be solved by using upper and lower decomposition followed by Gaussian elimination. The problem with Gaussian elimination is for *N* equations the number of computations is of the order of N^3 [Berry, 1971]. Since a sparse matrix is formed for this type of network, a reduction of the number of computations can be achieved [Hachtel et al, 1971]. The matrix **A** is a tri-diagonal matrix, and the total number of computations to solve the system is 3(N-1) [Dalquist, & Bjorck, 1974c]. Since the values of the variables in the matrix cannot be defined on construction of the algorithms, partial pivoting must be carried out to avoid divide by zeros or a loss in accuracy. For a tri-diagonal matrix with partial pivoting, 5(N-1) operations are required. With the SRD simulation, the linear solving program was originally taken from the Linpac series of linear solving programs [Strang, 1980]. The program was converted to Pascal during the course of this research and modified to enable fast solutions of a tri-diagonal system with partial pivoting. A listing of this is given in appendix A2.

To undertake a time domain simulation, the linear system is solved between t for the known nodal values, and $t + \Delta t$ for the unknown nodal values. The recursion is provided by equating the solved nodal values to the known nodal values on the succeeding step.

During the process of a simulation, a decision must be taken to change between the reverse and forward modes of the simulation. For phase noise estimation, any changes in firing angle must be accurately determined. In general, the time steps are too coarse to satisfy this requirement, and so a method of interpolation between time steps is required. One of the problems in using Spice for frequency multiplier simulation is that the discrete timesteps of the computations can lead to troublesome limit cycle oscillations which obscure any phase noise effects. A standard method of interpolating against external

boundary conditions is Newton-Raphson's interpolation [Dalquist & Bjorck, 1974d], [Calahan, 1972]:-

$$t_{n+1} = t_n - \frac{f'(t)}{f(t)} \tag{7.42}$$

where f(t) is the dependent variable under consideration. f'(t), the time derivative is found from the gradient of the previous points calculated. Therefore the solution to the limit cycle problem adopted here is to perform Newton-Raphson iterations against a boundary condition to interpolate between calculation steps. The iteration is carried out to an end point t_{window} given by:-

$$t_{window} > |t_n - t_{n+1}| \tag{7.43}$$

If t_{window} is set too small then convergence will fail due to round off errors. Therefore it is desirable that t is set to a minimum level commensurate with negligible contribution to calculation errors. The algorithm implementation is illustrated in appendix A2.

7.5.4 Carrier lifetime effects

In the conduction part of the simulation it is important to consider the carrier lifetime. Charge carriers accumulate in the junction during forward conduction. Summation of the charge flowing through the junction at each step of the calculation simulates charge storage.

The total charge *q* that has accumulated in the diode can now be calculated, but this charge decays according to [Grove, 1967] from an initial value q_o:-

$$q = q_o \exp\left(\frac{-t}{\tau}\right) \tag{7.44}$$

Modelling of the effect of the carrier lifetime τ is achieved by the convolution of the carrier decay function with the applied current *I*. A modified value of the carrier concentration at the end of each step results. We have derived the following expression by performing a convolution of the decay function with the forward current:-

$$q = \left(\frac{I + I_o}{2}\right)\tau\left(1 - \exp\left(\frac{-t}{\tau}\right)\right) + q_o \exp\left(\frac{-t}{\tau}\right) \tag{7.45}$$

When the accumulated charge is found to become negative the Newton-Raphson's interpolation routine is initiated to find the exact point at which the charge becomes zero. At the exact point at which the accumulated carrier concentration charge reaches zero, the program switches to the impulse mode.

7.5.5 Self bias

In addition it is necessary to simulate the effect of self bias. A self bias circuit has been shown in fig7.5, consisting of bias resistance R_{bias} and inductance L_{∞}. As discussed in §7.3.3 a small DC current flows due to recombination. This current is found by averaging the current flow through the diode over one cycle. The averaging operation is:-

$$I_{dc} = f_{ref} \int_{(t - 1/f_{ref})}^{t} i\,dt \tag{7.46}$$

This DC current is converted to the bias voltage by multiplying the value with the bias resistor:-

$$E_{dc} = I_{dc} r_{bias} \tag{7.47}$$

7.5.6 Using simulation to calculate phase noise

Having established a stable configuration, the phase noise can be predicted. A most suitable method of estimating phase noise levels is to examine changes in the firing angle α measured against the phase of the reference drive waveform.

One of the objects of the program to be described in appendix A2 therefore is to calculate the firing angle α. In order to improve the accuracy, Newton-Raphson's interpolation is performed in between discrete time steps at the termination of the conduction cycle. Any change in value of the following will change the firing angle:-

1) Carrier lifetime;

2) Drive level;

3) Diode model value fluctuations (resistance and capacitance).

Considering the observations of Watanebe [Watanabe & Fakatsu, 1967] and McDade [1966], the contribution of carrier lifetime functions to phase noise was investigated. A conversion factor is determined for carrier lifetime fluctuations to phase noise by applying a step change to the carrier lifetime and observing the change in α. Determination of the lifetime change $\Delta\tau$ would be necessary by means of either measurement or noise theory. For ease of comparison a constant phase noise level of -115 dBc/Hz was assumed at 1Hz from carrier as reported by Muat [1986]. Fig7.42, §7.10.5, displays a plot of reciprocal carrier lifetime against phase noise, other parameters remaining constant, with and without self bias. A constant bias level of 1volt is maintained by changing the bias resistor to compensate for the effect of changing carrier lifetimes. The results for the phase noise are

normalised to 1 Hz from carrier so that a $1/f$ relationship can be applied to the phase noise levels at other offsets from carrier frequencies. These figures can be applied to other offset frequencies by applying a factor $-10\log_{10}(f)$.

If no bias is used, the phase noise angle varies approximately according to the reciprocal of lifetime, as predicted from equation (7.12) above. If bias is used, the program indicates a higher level of phase noise, less dependent upon lifetime.

7.5.7 Simulation program functional description

7.5.7.1 Program overview

The complete SRD simulation was written in Turbo Pascal Version 5.5 run on a PC using a 33 MHz 80386 and 80387 co-processor. Program listings together with a description can be found in appendix A2.

At the core of the program is the time domain simulation which runs continuously in a closed loop, the loop being completed for each computed time-step of the simulation. These time-steps will be for either the reverse or forward modes, transition between the two modes being determined by the following boundary conditions:-

Forward to reverse mode	Stored charge $q < 0$
Reverse to forward mode	Voltage across junction capacitance > barrier voltage *and* diode current > 0

At the periphery of the main program lie the other sub program packages which act upon the simulation and modify the input data. The following functions are provided by these packages:-

a) Time domain simulation

b) Frequency domain plot with added noise

c) Feigenbaum diagram

d) Phase noise- carrier lifetime plot

e) Firing angle recurrence relation plot

7.5.7.2 Time domain plot

The basic function of the simulator is to provide a time domain file of the circuit over user defined time limits. This can be either plotted to a screen or printed as a hardcopy.

7.5.7.3 FFT plot

For the FFT plot, the simulation is carried out with 4 types of noise sources either added to or modulating the carrier input as will be described in §7.7.2:-

a) Additive noise

i) baseband

ii) RF (at carrier frequency)

iii) Broadband

b) AM noise

c) PM noise.

Any of these can be optionally selected by the user. They are all filtered by a first order filter function to limit adverse high frequency effects with the simulation. Upon requesting an FFT, the results of the time domain simulation are stored in a large array in extended memory of size determined by the user. The FFT time increments are equally spaced and independent of the simulation time steps. Linear interpolation is carried out between the nearest data points to the FFT time increment. On completion of the time domain simulation, an in place FFT is taken so the time domain data is replaced by frequency domain data. The user will then need to specify the frequency range of which an FFT is taken. An option exists in the display package for the FFT to provide a moving average of the display to reduce noise variations and enable a value to be estimated for noise levels. The moving average is taken retrospectively as the frequency point is incremented.

7.5.7.4 Feigenbaum diagram

The remaining functions require the calculation of the firing angle α. This is calculated for each cycle when the first reverse mode step is encountered. A Feigenbaum diagram is formed from a plot of firing angle against load resistance and is discussed in §7.8.1 in connection with SRD instability and subharmonic phenomena. The load resistance is incremented by a small amount as a new conduction cycle is initiated. Load resistance is represented by the horizontal axis of the diagram. A value of firing angle is given each time the reverse region is initiated from a calculation of the time interval between the present reverse region and the previous one. Firing angle plots are obtained on an axis from $\pi/2$ to $3\pi/2$ radians. Any firing angle values above that represent a lost impulse and are overlaid by having the nearest integer value of 2π subtracted. Any value of firing angle below $\pi/2$ represents double pulsing and is represented by a white spot. The number of cycles subtracted is represented by a colour of the diagram as displayed on the computer screen as follows and such a display is illustrated in plates 1 to 3 of §7.8.1.:-

0	white
1	red
2	light blue
3	yellow
4	light green

The display is updated at the start of the reverse region, as a new value of α is calculated; also a value is written to a file in a RAM disk for permanent storage after the program halts. Such a data file enables rapid recreation of the display by storing the graph co-ordinates.

The program halts after a user specified maximum value of R is exceeded.

7.5.7.5 Phase noise plot

As described in §7.4.1, a small change is applied to the carrier lifetime in order to estimate the resulting value of contribution to output phase noise. Ten cycles of input are then allowed before the resulting phase change is measured. This is to enable transient effects to decay away. After a measurement is taken, the carrier lifetime is incremented to the next value to be plotted in the graph.

The adjustments to carrier lifetime, τ, and subsequent measurements are carried out at the start of the reverse region. The number of cycles are counted, and upon reaching the 10th, either of the following may occur:-

a) A value of firing angle α is stored, and the lifetime is incremented by a small factor; or

b) A new value of α is obtained and from it, the previously stored value of α is subtracted.

This resultant change of α is used to represent the phase noise value. A new value of carrier lifetime in then applied ready for the next plotting point. Steps a) and b) are carried out in turn after 10 successive cycles have elapsed.

Inverse lifetime is sent to the plotting package as the horizontal axis, as described in §7.10.5, and phase noise is sent to the vertical axis. Since the inverse lifetime factor is used, the graticule routine was re-written for a reciprocal factor on the horizontal axis. Results from this option are presented and discussed in §7.10.5.

7.5.7.6 Recurrence relationships

The theory behind the use of recurrence relationships to ascertain the likelihood of stability problems is given in §7.9.3. To obtain a recurrence relationship, the starting point on the

time axis is varied, and the value of successive cycles firing angle are plotted against the previous cycle firing angle. On starting, the value of time is normally set corresponding to the point on the input drive equal to the diode barrier voltage. For the recurrence relationship plot, this time is offset by a factor that is incremented in a loop around the time domain simulation. As the simulation proceeds for each time increment, the value of α obtained for each successive input cycle is stored in an array. On completion of the simulation, the nth value of α, stored chronologically in the α array are plotted against the (n - 1)th value of α, for values of $n = 3$ to the final value of α stored. Following this, the loop increments the simulation starting time offset and another simulation is carried out until the offset range covered approximately equals one cycle. This method was chosen in preference to adding displacements to α when the simulation is running, because difficulties would be encountered when α becomes a strange attractor, that is when non-convergence to a singular value occurs (see §7.8).

7.6 Time domain simulation results and implications

7.6.1 Time domain simulation results

The results of simulations for two comb generator circuits are presented below. The first to be considered is the basic impulse generator of fig7.6. of §7.5.1. Secondly, a practical comb generator that contains the inductance of the matching transformer, and a reflection capacitor that restricts the fast rising impulse to the output stage was considered. By setting the values of L1 and C1 to zero, the second circuit can be modified to give the first circuit, enabling the same simulation to be used for both cases. The resulting time domain plots given by the simulator for the basic impulse generator is displayed in figs7.10 and 7.12 below. Table 7.1 below illustrates the values of components used in the simulations.

A time domain plot of a normally operating SRD comb generator is displayed in fig7.10. The voltage level across the diode is plotted as the fine upper trace. Diode current is plotted as the lower, more dense trace. The impulse in diode voltage corresponds to a sharp step in negative diode current. When the charge is removed from the intrinsic layer, the impulse occurs as the diode impedance rapidly rises. Initially, the diode conducts and the carrier concentration in the junction increases. Maximum stored charge is achieved when the diode current falls to zero, and begins to decline as the current flow is reversed. Although the current flow is now negative, the diode junction is equivalent to a very large capacitance, and the diode terminal voltage will remain positive, although the output

voltage will fall due to the voltage across diode bulk resistance R_d. As the stored charge falls to zero, the virtually infinite junction capacitance falls rapidly to the reverse junction capacitance.

Table 7.1

Simulation element		Network 1	Network 2	Units
Reverse capacitance	C_d	2.2	2.2	pF
Reverse resistance	R_d	3	3	Ω
Minority carrier lifetime	τ	100	100	ns
Impulse drive inductance	L_d	80	80	nH
Load Resistance	R_x	50	100	Ω
Source resistance	R_{source}	10	10	Ω
Peak drive voltage	E_{pk}	4	6	V
Drive frequency	f_r	100	100	MHz
Transformer inductance	L_1	0	470	nH
Reflection capacitor	C_2	0	25	pF
Time step	dt	10^{-10}	10^{-10}	s

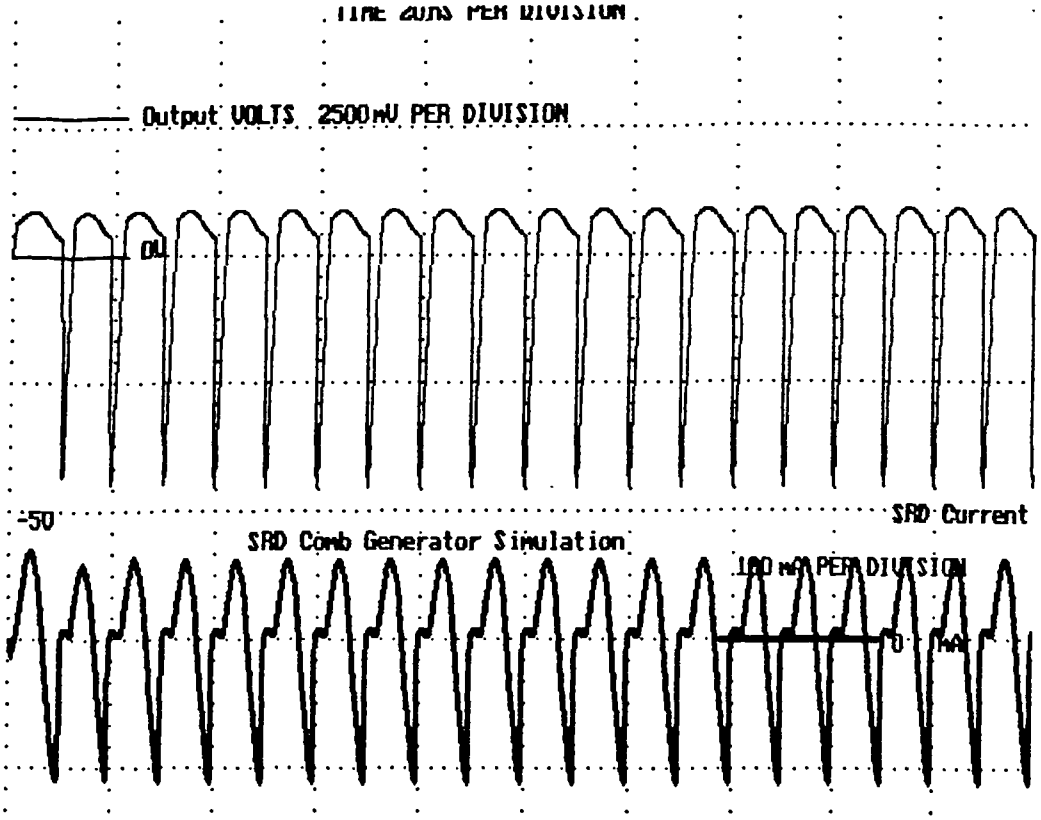


Fig 7.10 Time domain simulation with 50Ω load, network 1

Consequently, a sharp peak in reverse (negative) voltage occurs and a damped oscillation begins in the diode reverse voltage due to the effect of drive inductance and reverse capacitance. When the oscillation results in the diode junction barrier voltage being exceeded, forward conduction begins. This effect has been illustrated earlier in fig7.4. The forward conduction is being driven by stored energy in inductance L_d. A small amount of residual reference feedthrough is present due to the finite bulk resistance of the diode, but this is small in comparison with the large reverse peak in output voltage that occurs as the diode impedance increases.

The frequency domain representation of the time domain files can be obtained by a fast Fourier transform. Fig7.11 displays the frequency domain plot of the time domain file of fig7.10. A series of harmonics of steadily decreasing intensity is obtained. Between harmonics, there is noise present as a result of the noise source introduced to the simulation.

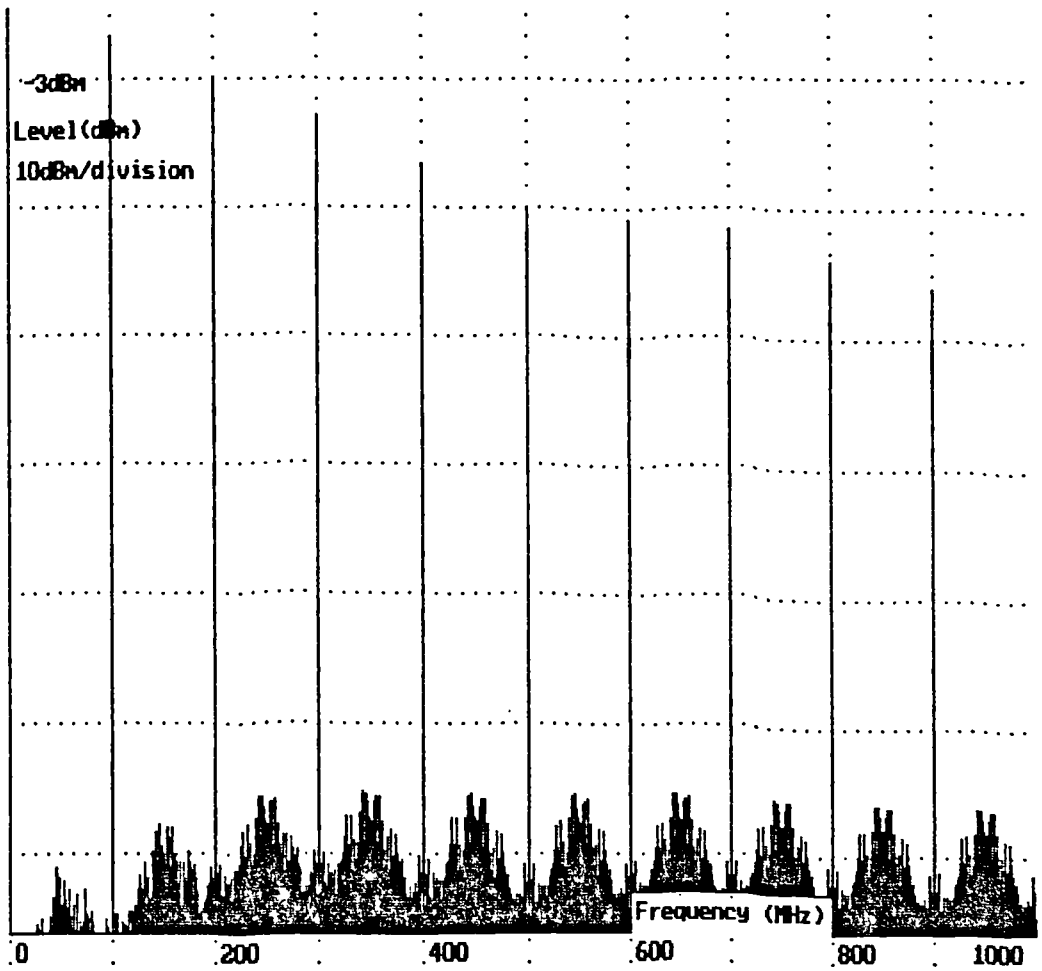


Fig 7.11 FFT of comb generator with 50Ω load and broadband additive noise, network 1

7.6.2 Demonstration of the stability problem

The time domain simulation can now be used to investigate the various subharmonic phenomena that may occur.

Ryan [Ryan & Williams, 1964] suggested that carrier storage effects can result in frequency division. The effect of carrier storage division is that oscillation can occur at sub-multiples of the driver frequency f_{ref}. Although it is possible to harness this property to undertake frequency division as well as multiplication [Pritchard, 1985], in general these spurious modes are undesirable. Such modes could be induced in the simulation, and in a real circuit (see §7.11) by simply changing the load resistance Rx. Fig7.12 displays a time domain simulation of a SRD comb generator showing the effect of raising the load resistance to 400Ω, giving carrier storage division. Every alternate impulse is lost when more carriers are injected into the intrinsic region than can be removed during

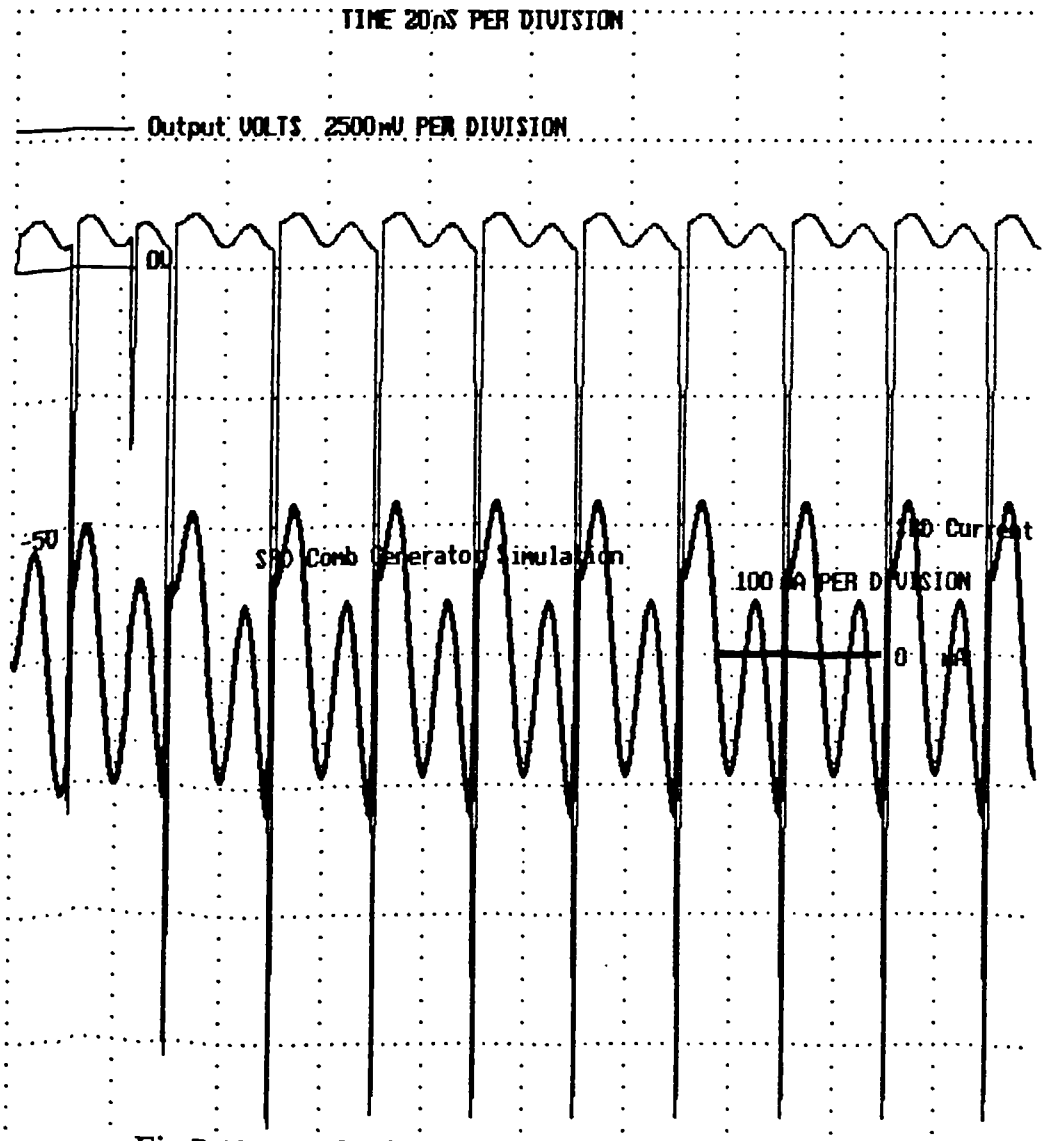


Fig 7.12 Carrier storage division, network 1, R_x=400Ω

Note the complete obliteration of every alternate pulse due to charge storage effects. This provides proof that parametric oscillation can be achieved without idlers.

In fact the above described mode of operation more closely resembles a digital divider rather than a negative resistance parametric oscillator [Goto, 1959]. An FFT of the time domain file indicates that frequency halving is taking place. If this effect could be stable and reliably maintained, then use could be made in the design of synthesisers. A plot of a time domain measurement with a digital storage scope is shown in fig7.13 and displays this effect. In the frequency domain this effect is displayed in fig7.25 in §7.8.1 that shows the frequency domain results.

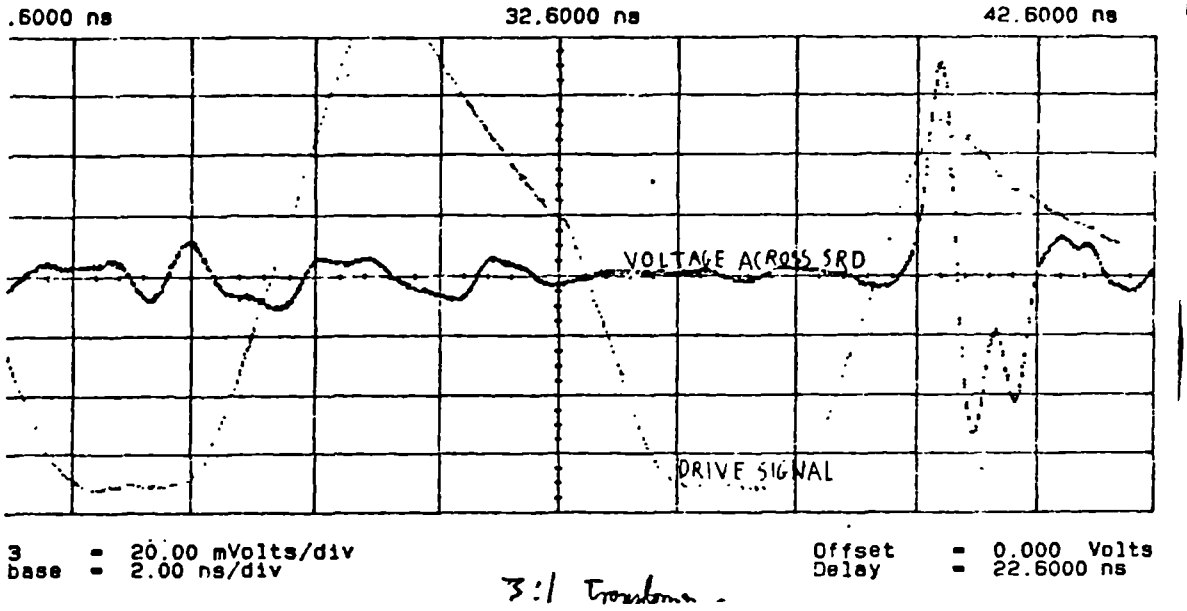


Fig 7.13 Digital storage oscilloscope trace showing carrier storage division

Fig 7.14 displays the fact that still other modes of operation are possible. This plot was obtained by including the matching transformer and a load resistance of 1400Ω. Random variations in the period of the waveform appears to occur. An FFT of this time domain file gives a plot resembling broadband noise similar to fig7.27 of §7.8.1. This phenomenon is commonly referred to by RF engineers as "spectral breakup".

Thus the mode of operation of the same circuit configuration can be varied; altering one of the circuit parameters slightly results in drastic changes in behaviour, and such changes are termed *bifurcations* [Lauwerier 1986a];

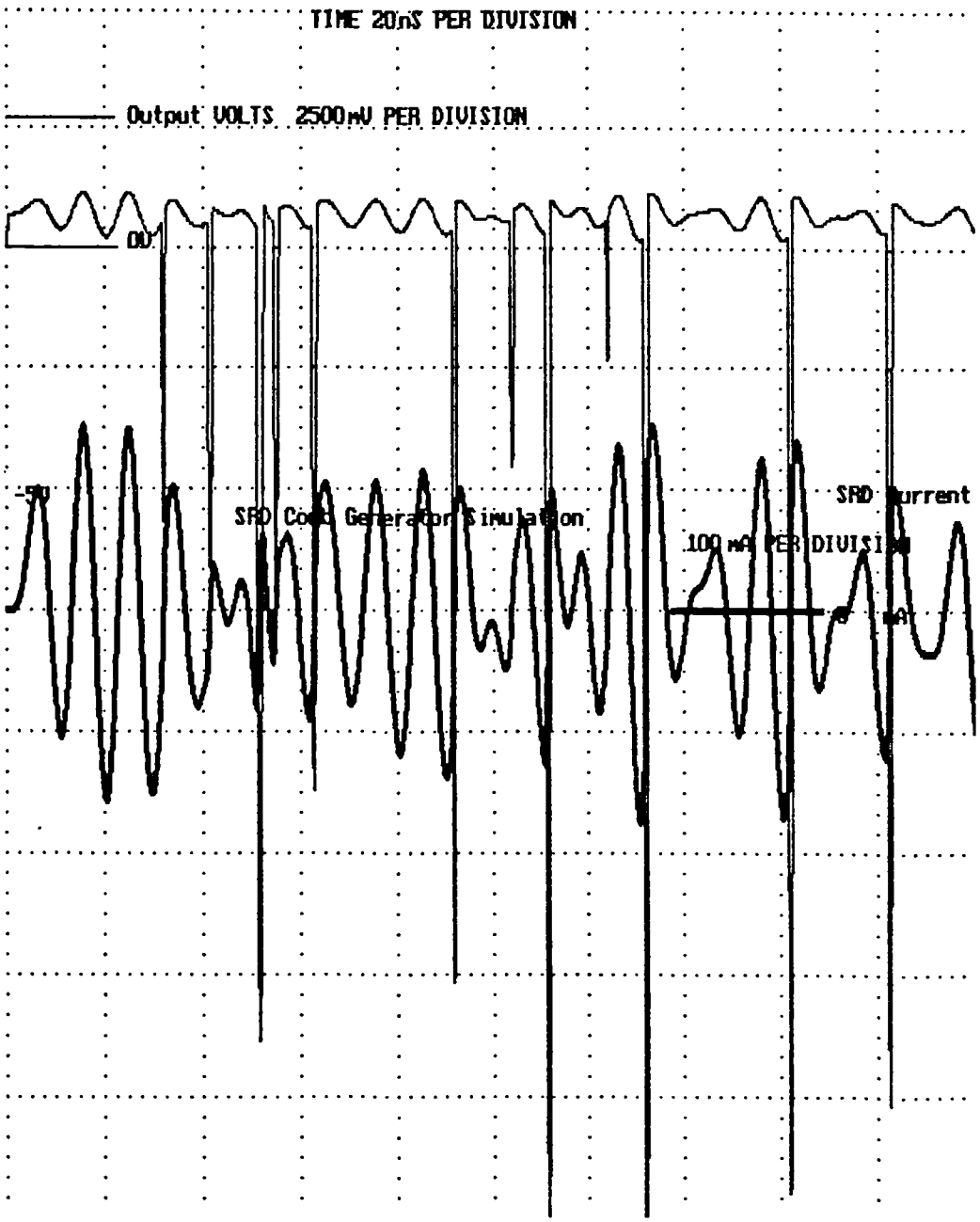


Fig 7.14 Time domain plot, network 2
showing chaotic behaviour with R_X=1300Ω

A time domain simulation is capable of indicating the mode of operation, but used alone cannot indicate whether or not the circuit is operating near a bifurcation point, nor is it able to enable evaluation of phase noise. One method of overcoming these difficulties is to transform the time domain results into the frequency domain by means of an FFT, and this will be discussed in the next section.

7.7 Using simulation to investigate stability and phase noise effects

7.7.1 Simulation method

Phase noise is investigated by the introduction of noise sources into the SRD model. Since the investigation concentrates on the mean power level of the noise rather than its power distribution, uniform rather than Gaussian distributed random numbers are used. (Accurate Gaussian random numbers use considerably more computation time to generate than uniform random numbers.) Uniform numbers are acceptable if the output mean power only of the noise is of interest, but if the simulation is to be part of a larger system simulation that is sensitive to the noise distribution (eg bit error rates) then Gaussian distributed random numbers must be used.

Initially, the degradation effects of the comb generator upon a signal with noise modulations are considered. Distribution of the noise in the frequency domain is plotted with the aid of an FFT, and this enables a further check on stability. Then, noise sources internal to the SRD are simulated and the results discussed in §7.10. Particular attention is given to carrier recombination noise as this appears to the principle noise source in the SRD. Changes to the self-bias and SRD lifetime are made during simulation and the resulting noise output is recorded.

7.7.2 Input signal models

For the case of noise modulations on the input signal, the following noise excitations were used:-

1) Additive noise;

2) Amplitude Modulation (A.M) noise;

3) Phase noise.

To study the spectral distribution of the noise and signals at the output of the comb generator, the appropriate noise modulation is selected, and a time domain file is created. Subsequently, an FFT is taken of the time domain file to convert it to a frequency domain file.

The input carrier to noise density is first established by obtaining an FFT of the modulated input waveform. From a moving averaged display obtained as described in §7.5.7.3 the carrier to noise density ratio is measured by inspection against the graticule. For each noise type, the measured signal to noise ratio in dB is given with the captions of fig7.15 to 7.19. The same procedure is repeated for the FFT of the 10th harmonic of the output of the simulated comb generator; the difference in these levels in dB gives the actual noise increase due to frequency multiplication, which can be compared with the theoretical value of 20dB.

The RF input signals to be used in the simulations are shown in figs7.15 to 7.19. Fig7.15 displays the signal with random phase modulation. Fig7.16 displays amplitude modulation, fig7.17 is bandlimited RF noise, fig7.18 broadband additive noise and fig7.19 is baseband additive noise.

With the additive noise, it is important to bandlimit the noise applied to the simulation to ensure accurate results by avoiding aliasing problems. The noise is bandlimited by applying the function:-

$$V_{ni} = V_{npk}\,(2 \times \text{rand} - 1) \tag{7.48}$$

$$V_{noi(n)} = V_{noi(n-1)} + \left(V_{ni} - V_{noi(n-1)}\left(1 - \exp\left(\frac{-t}{\Gamma}\right)\right)\right) \tag{7.49}$$

where rand is a random number generated by PASCAL and V_{npk} is the peak noise voltage. Γ is a filter time constant of 1/fr, V_{ni} is the random noise voltage source, $V_{noi(n-1)}$ is the previous noise output of the bandlimiting filter and V_{noi} is the present output. If the random number is updated at every time step in the simulation and the additive noise formula is used:-

$$E_{driv} := E_{peak}\left(\sin(2\pi ft) + V_{noi}\right) \tag{7.50}$$

A spectral display obtained by computation of the FFT of the broadband additive noise and input reference frequency is given in fig7.15.

As can be seen from the Manley-Rowe series equations (7.6 & 7.7), additive noise can introduce phase noise in a non linear circuit by two principal mechanisms: direct at the carrier frequency and by upconversion from low frequencies. Both effects are possible in the step recovery frequency multiplier and so it is necessary to discriminate between these effects. Low frequency noise on the input signal can be filtered out by means of a transformer, but effects within the diode such as forward barrier voltage fluctuations cannot be removed in this manner.

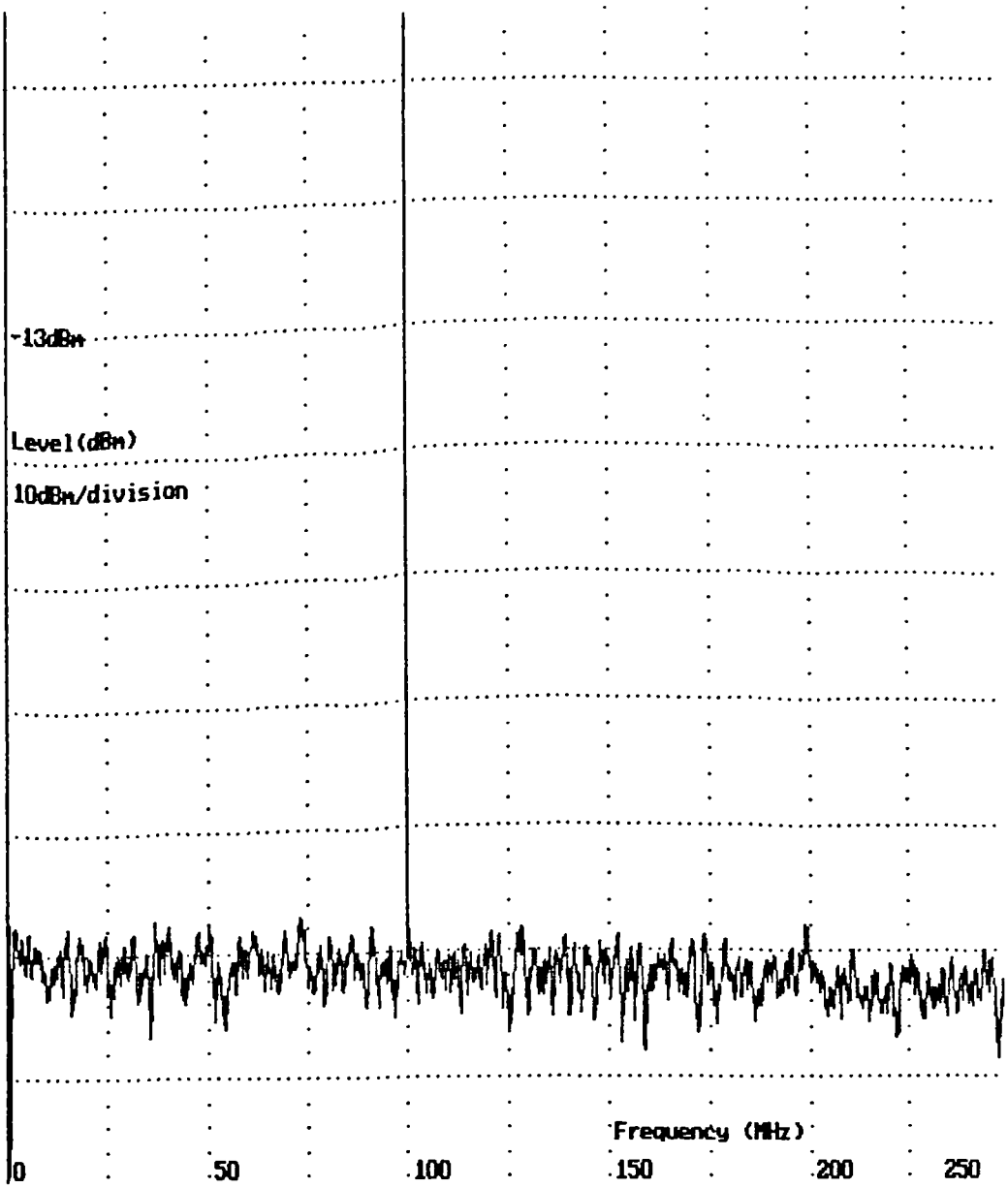


Fig 7.15 Input signal +broadband additive noise; signal to noise density = -68 dB

If instead of adding a new random number every time step of the time domain simulation, a new random number is added every input cycle, baseband additive noise is created. Equation (7.49) can be also used in this case. Baseband additive noise can be used to investigate upconversion effects from low frequencies. In the frequency domain, a spectrum that is approximately flat at DC, but with notches at the reference frequency is obtained as can be seen from fig7.16.

A.M noise is assumed to be unchanged by the multiplier according to many authors [Kroupa, 1973]. Other authors assume that the multiplier is to be preceded by a limiter [Manassewitsch, 1985c]. However this does not consider the fact that residual AM noise can be introduced by the limiting process and by the multiplier itself. There are publications [Fairley, 1968] that assume a multiplier raises the AM noise by $20\log N$, where N is the multiplication ratio. Egan [1981] states that in many cases AM noise is

suppressed by the multiplier, but carries on to say that the degree of suppression of the multiplier depends upon the configuration. Manassewitstch [*ibid*] suggests that the actual multiplier response to AM noise is given by $20\log(m\,N)$ where m is a configuration dependent coefficient which can vary from 0 (total suppression) to 1 ($20\log N$ rule).

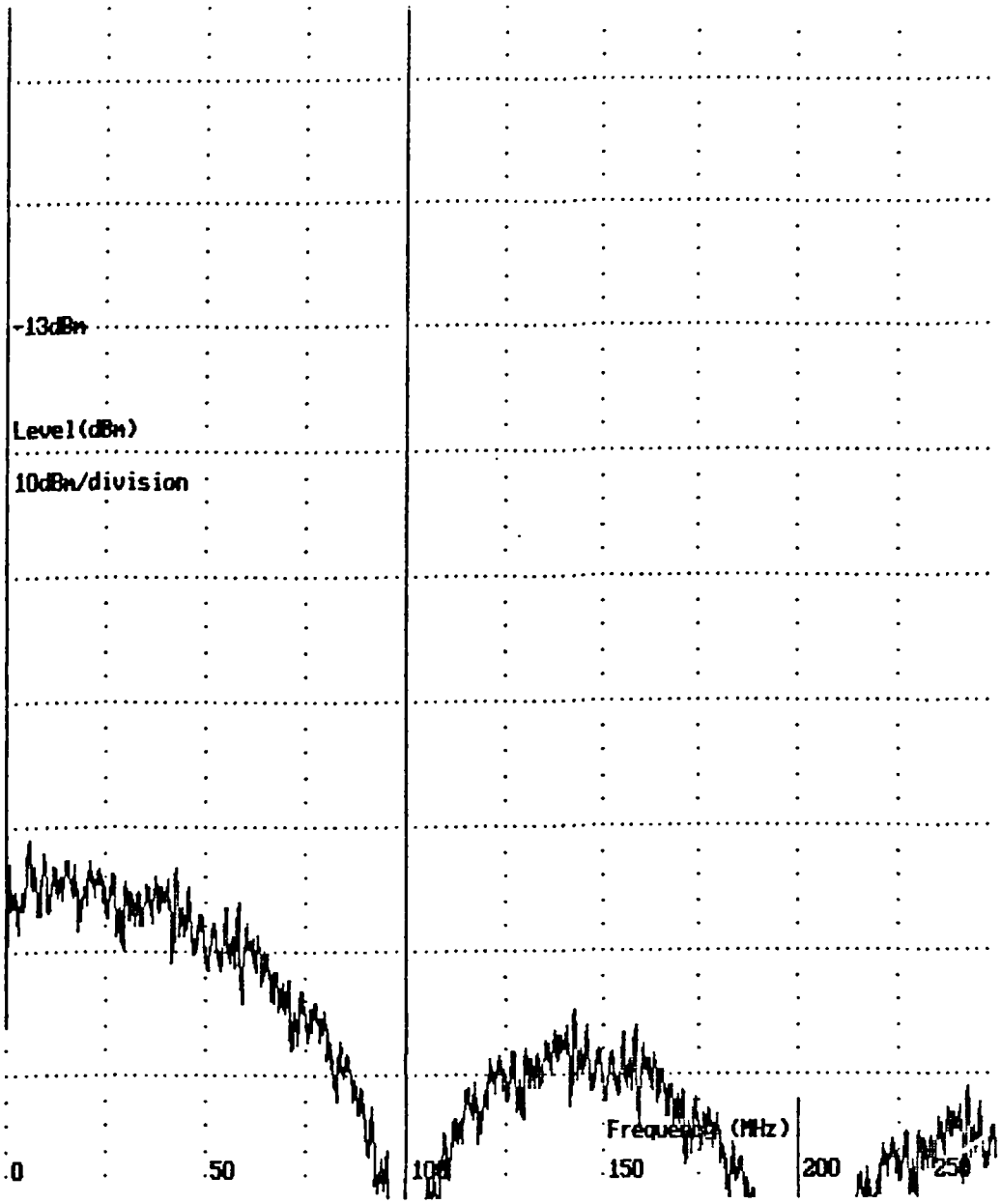


Fig 7.16 Input signal +baseband additive noise signal to noise density = 71 dB

For the specific case of the SRD multiplier, the sensitivity to AM noise can be determined by the simulation program described here. AM noise modulation on the input carrier is introduced by the following equation:-

$$E_{driv} := E_{peak}(1 + V_{noi})\sin(2\pi ft) \qquad (7.51)$$

Once again a filtering function such as (7.50) must be applied to avoid aliasing problems. Fig 7.17 shows the input signal with AM noise applied.

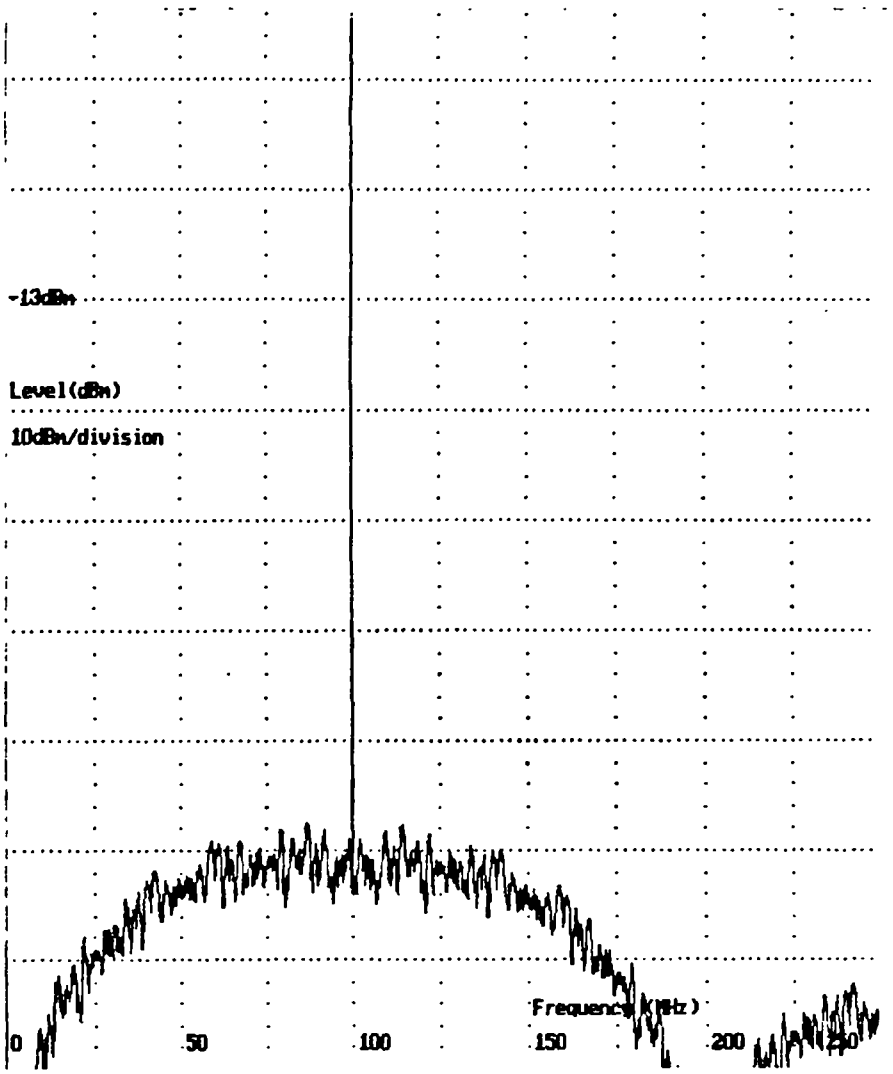


Fig 7.17 Input signal + AM noise; signal to noise density = -75dB

Phase noise is introduced by phase modulation of the applied waveform:-

$$E_{driv} := E_{peak}\sin(2\pi ft + V_{noi}) \tag{7.52}$$

Fig 7.18 displays the effect of phase noise upon the input signal.

The RF additive noise is obtained by simultaneously applying AM and phase noise. Separate random numbers V_{ni1} and V_{ni2} are used for the AM and phase noise.

$$V_{ni1} = V_{npk}(2 \times \text{rand} - 1) \tag{7.53}$$

$$V_{noi1(n)} = V_{noi1(n-1)} + \left(V_{ni1} - V_{noi1(n-1)}\right)\left(1 - \exp\left(\frac{-t}{\Gamma}\right)\right) \tag{7.54}$$

$$V_{ni2} = V_{npk}(2 \times \text{rand} - 1) \tag{7.55}$$

$$V_{noi2(n)} = V_{noi2(n-1)} + \left(V_{ni2} - V_{noi2(n-1)}\right)\left(1 - \exp\left(\frac{-t}{\Gamma}\right)\right) \qquad (7.56)$$

This is an approximation that is only valid for the good signal to noise conditions that are likely to occur with synthesisers. A frequency domain representation of the bandlimited additive noise is a spectrum that is approximately flat around the carrier, but has notches at baseband and twice carrier frequency.

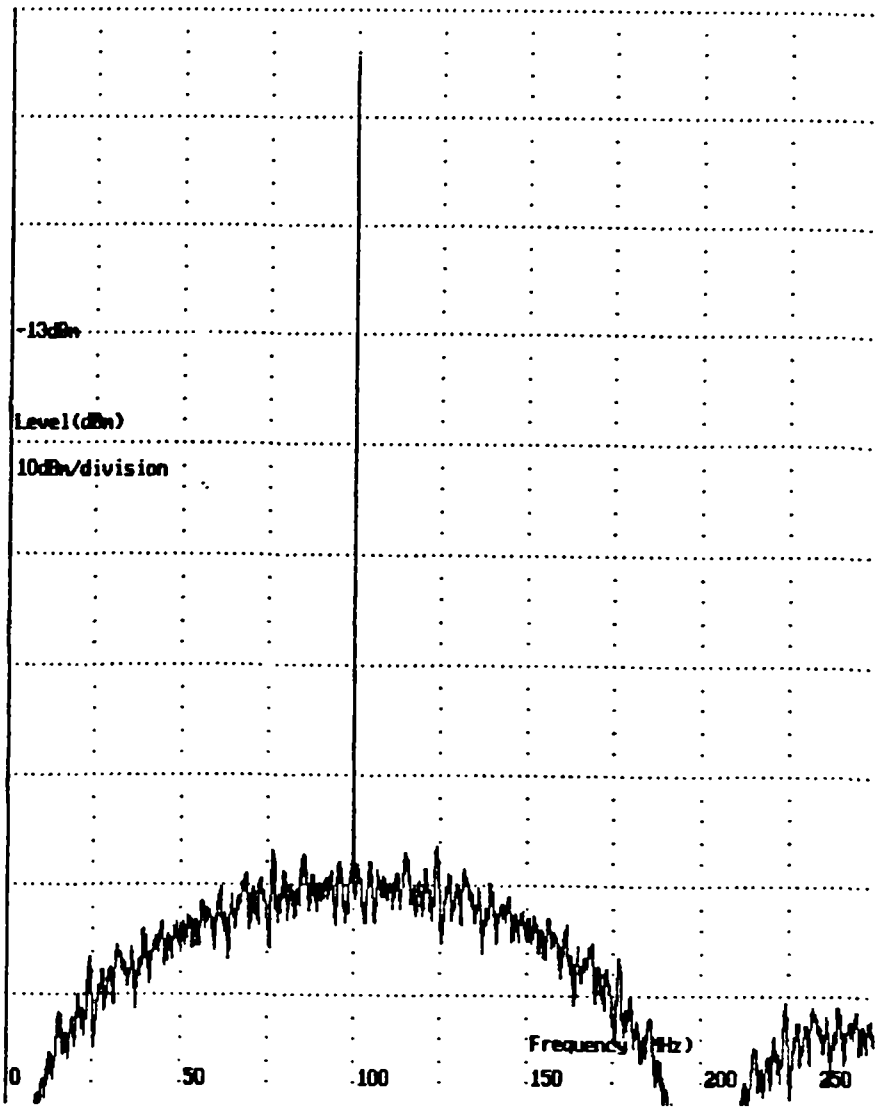


Fig 7.18 Input signal +phase noise; signal to noise density = -75dB

Fig 7.19 displays the spectrum with bandlimited additive noise added. A single time constant filter is used for simplicity. The filtering function is not as ideal in terms of frequency response as if more complex filtering is used such as finite impulse response or window filters, but is less demanding on computation. If more accurate results are desired such filters will be required.

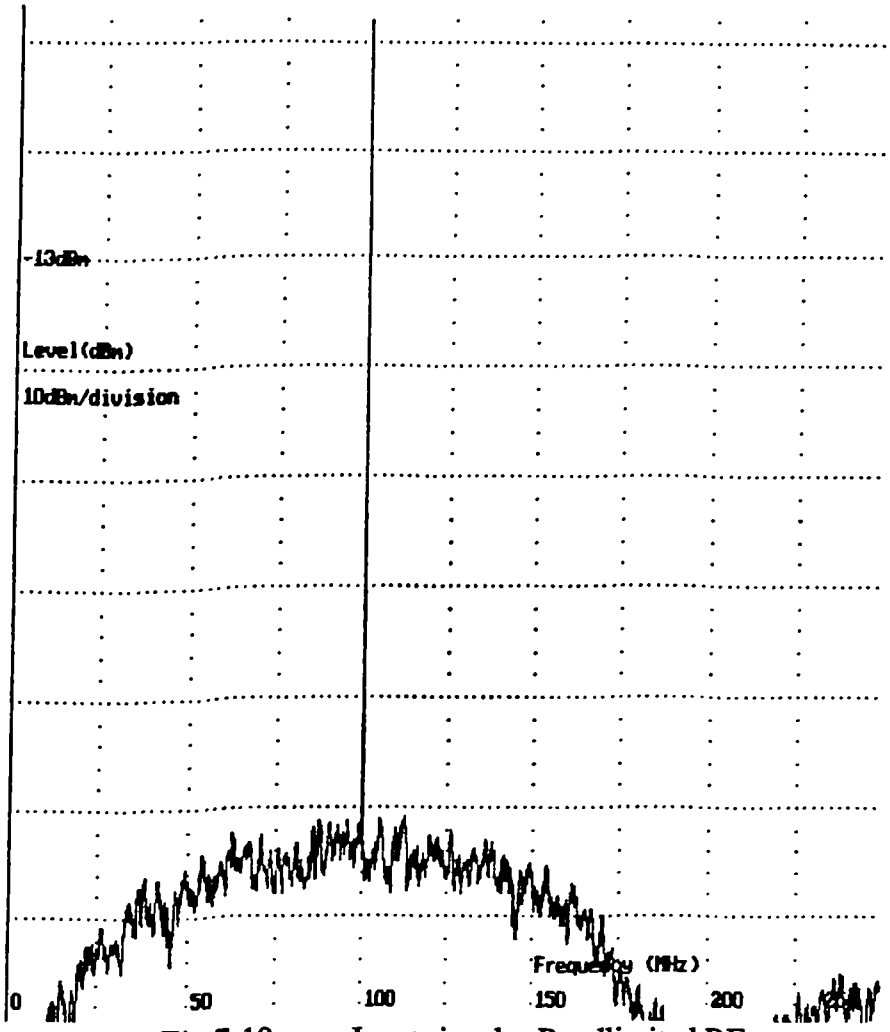


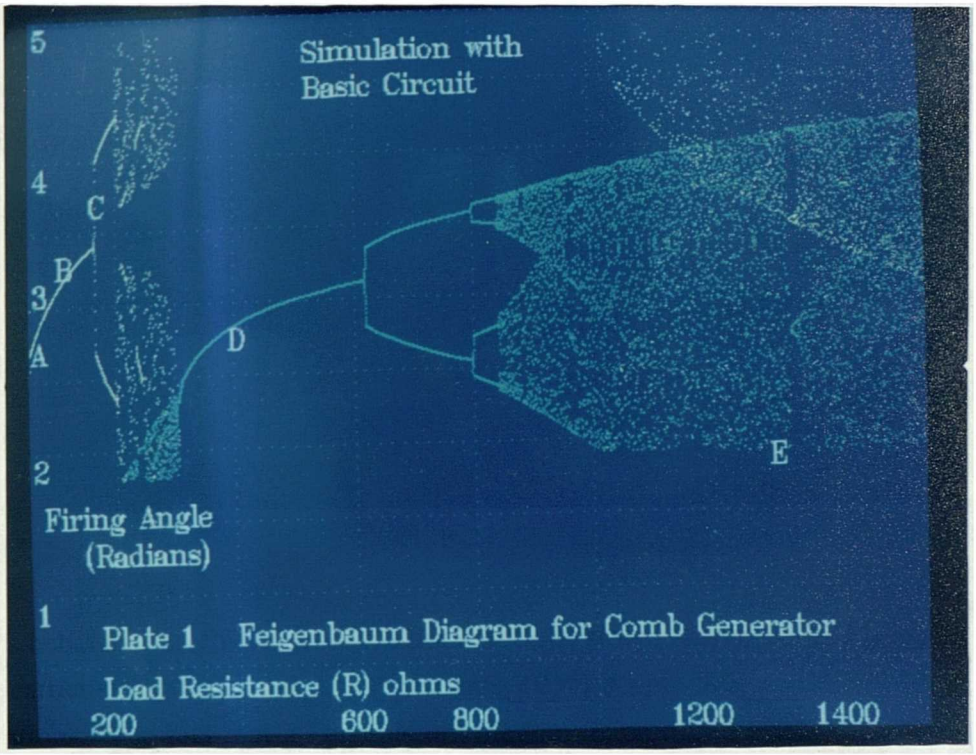
Fig 7.19 Input signal + Bandlimited RF
Additive noise; signal to noise density = -75dB

7.8 Bifurcations: implications for phase noise and spectral purity

7.8.1 Relationship between the Feigenbaum diagram and the frequency domain spectrum

An option exists in the SRD simulation program as discussed in §7.5.7.4 to plot the firing angle α against load resistance R. For a certain mode of operation of the comb generator circuit, certain values of firing angles will be reached after initial transients have decayed, the value of α is therefore the attractor. The attractor - load resistance R plot was introduced to map out all possible modes of operation of the comb generator circuit. For a particular value of load resistance, either a single value of α exists (sink attractor), multiple values of α are produced in cyclic rotation (limit cycle attractor shown as multiple

points on the graph), or very large number of α points may exist (strange attractor). The last condition is known as chaos, and the transitions between the conditions are the bifurcation points. Such a plot of α values, displayed as plate 1, is of particular interest as it resembles a class of solutions displaying chaotic behaviour known as Feigenbaum structures [Becker &Dorfler 1990]. A Feigenbaum diagram is a particular form of the bifurcation diagram [ibid] that is commonly encountered in chaos theory.



This behaviour originates from the population of stored charge carriers in the device, and the carrier storage effect [Ryan & Williams, 1964] is a physical manifestation of the above solutions. The fact that a Feigenbaum diagram is produced implies that some form of recursion or feedback mechanism must be present together with a non-linear function. The value of α determines the number of charge carriers generated in the conduction phase, these in turn determine the value of α in the next cycle, and so on. Non-linearities are introduced mainly by the discontinuity between the conduction and impulse regions. Period doubling at the onset of the chaotic behaviour is a characteristic of this particular phenomenon, hence the subharmonic generation.

It would seem that the Feigenbaum Diagram enables a more global approach to the problem of phase noise analysis since it can include carrier storage division, not easily accounted for by parametric (negative resistance) analysis.

Even if oscillations cannot occur, the parametric gain will result in enhancement of either the SRD noise or driver circuit noise (see fig7.11) as discussed in §7.4.4. At frequencies close to the desired signal the negative resistance is reduced due to finite carrier lifetime. We observed, however, that this "parametric gain" is closely linked to the distance from splits or bifurcations in the Feigenbaum Diagram. Referring to Plate 1 the single line at the left represents stable harmonic generation. For low noise frequency multiplication it is vital that the bifurcation points be avoided.

In order to demonstrate the significance of the Feigenbaum diagram, points on such a diagram are related here to their corresponding frequency domain plots by selecting RF additive noise on the input and obtaining an FFT of the time domain file. Subsequent to obtaining the FFT, the noise sidebands at the 10th harmonic are displayed. Both circuit configurations given in §7.5.1 are subject to this simulation. Initially, dependence of phase noise on the effect of bifurcation points is investigated with RF additive noise applied at the input, an FFT taken of the time domain file and fig7.20 displays the spectrum with a 50Ω load to the simplest comb generator circuit as given in table7.1. Fig 7.21 shows the effect of increasing the load to 100Ω.

In fig7.10, §7.6.1. a time domain simulation of a correctly functioning comb generator with one impulse per cycle of input has been displayed. An impulse occurs when the charge is removed from the intrinsic layer, and the diode impedance rapidly rises. Point **A** on the Feigenbaum diagram (plate 1) represents a stable comb generator with a single value of α. An FFT of the above simulation is displayed in fig7.20 showing noise sidebands at the 10th harmonic. There is significant peaking at the half carrier frequency, but the noise is increased by approximately 20dB in comparison with the sidebands on the RF input signal. This is as expected from the 20Log (N) formula.

Increasing the value of load resistance nearer the bifurcation point at point **B** gives an FFT plot of fig7.21. At an offset frequency of half the input frequency, the peaking increases to 14dB, but at the close to carrier frequencies, no additional degradation is apparent.

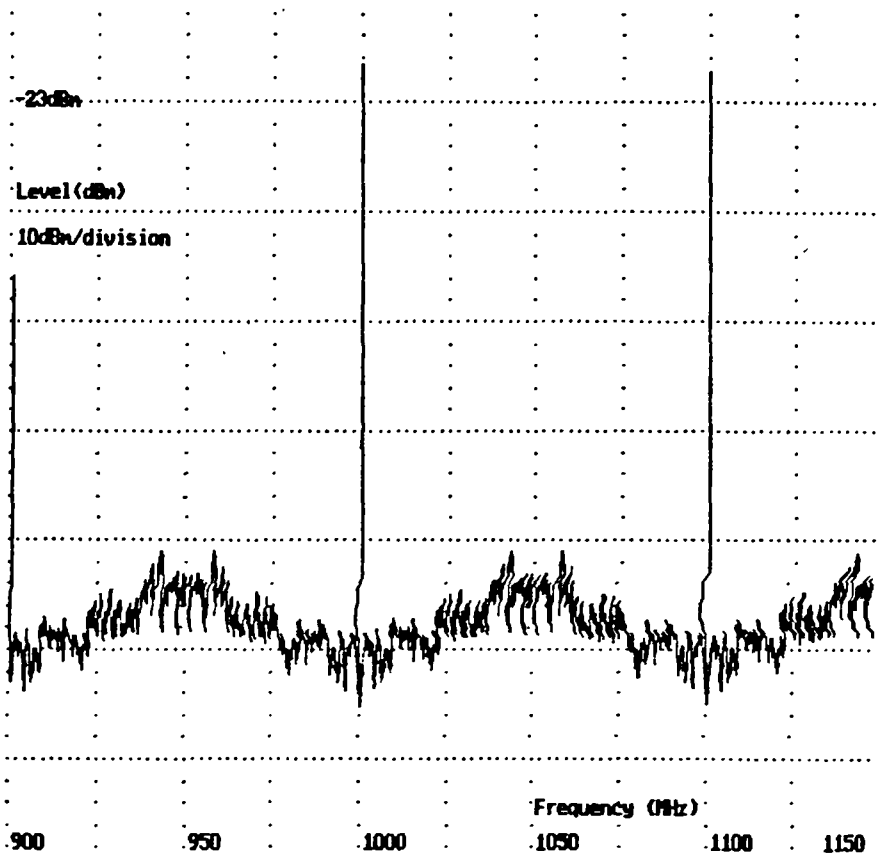


Fig 7.20 Rf additive noise added, network 1, 50Ω load.

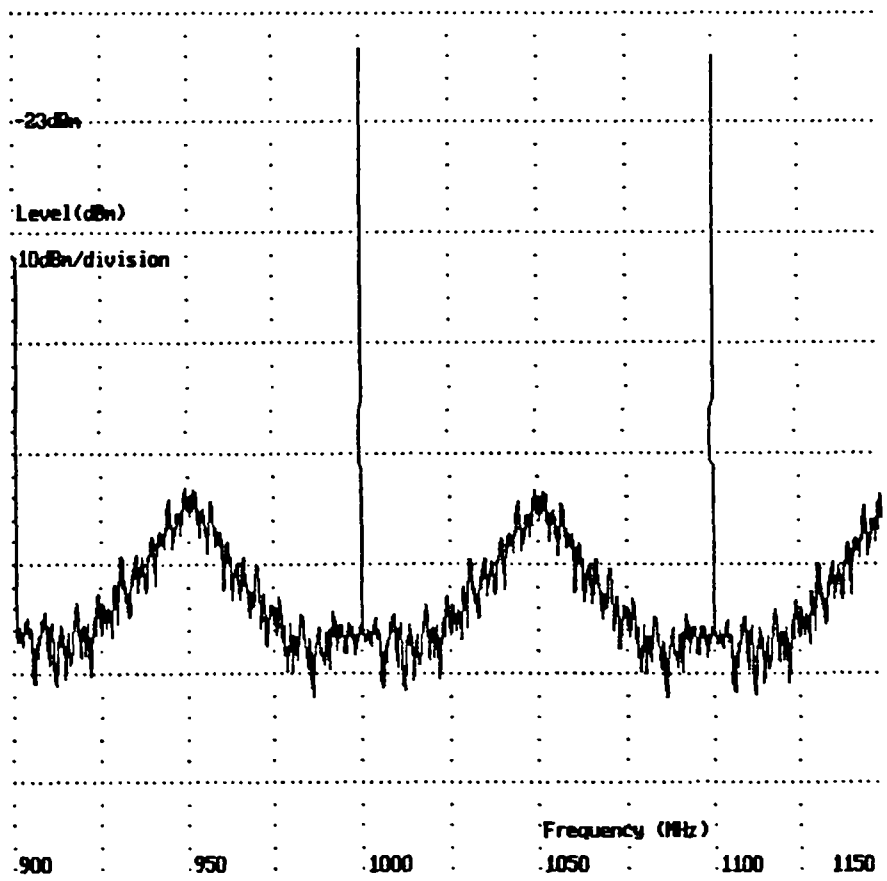


Fig 7.21 Rf additive noise added, network 1, 100Ω load.

The peaking in the noise floor is much more pronounced between the comb lines. If a large peak occurs at any frequency, in some systems, the noise will appear at baseband due to non linear intermodulation effects, and phase noise degradation could result as in the case with fig7.22 which was obtained by increasing the load resistance to 140Ω. Noise peaking at the half carrier frequency increases to 27dB and the close to carrier noise is increased an extra 17dB above the theoretical level.

As a check to ensure that the bifurcations were a result of SRD behaviour and not due to the algorithm, simulations were carried out at varying values of time step. Only slight differences in results were obtained, on account of the different values of integration approximation error.

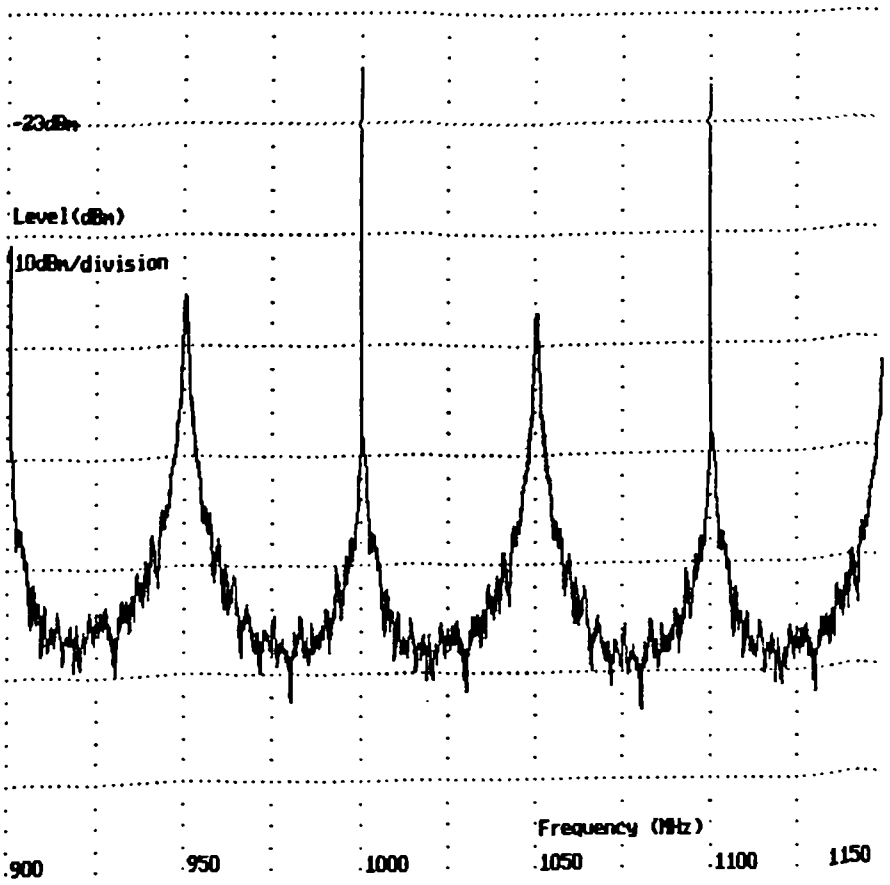


Fig 7.22 Rf additive noise added, network 1, 140Ω load.

At the bifurcation point on plate 1, as indicated by point C, it can be noticed that the phase plot is vertical on the α axis. A vertical line indicates that a range of phase values can exist simultaneously. This has disastrous implications for the phase noise and "phase hit" performance. An FFT of the time domain file, fig7.23, displays the resulting high phase noise, obtained by increasing the load resistance to 164Ω. As the bifurcation point is approached at 164Ω the noise at the 10th harmonic becomes greater in power than the signal.

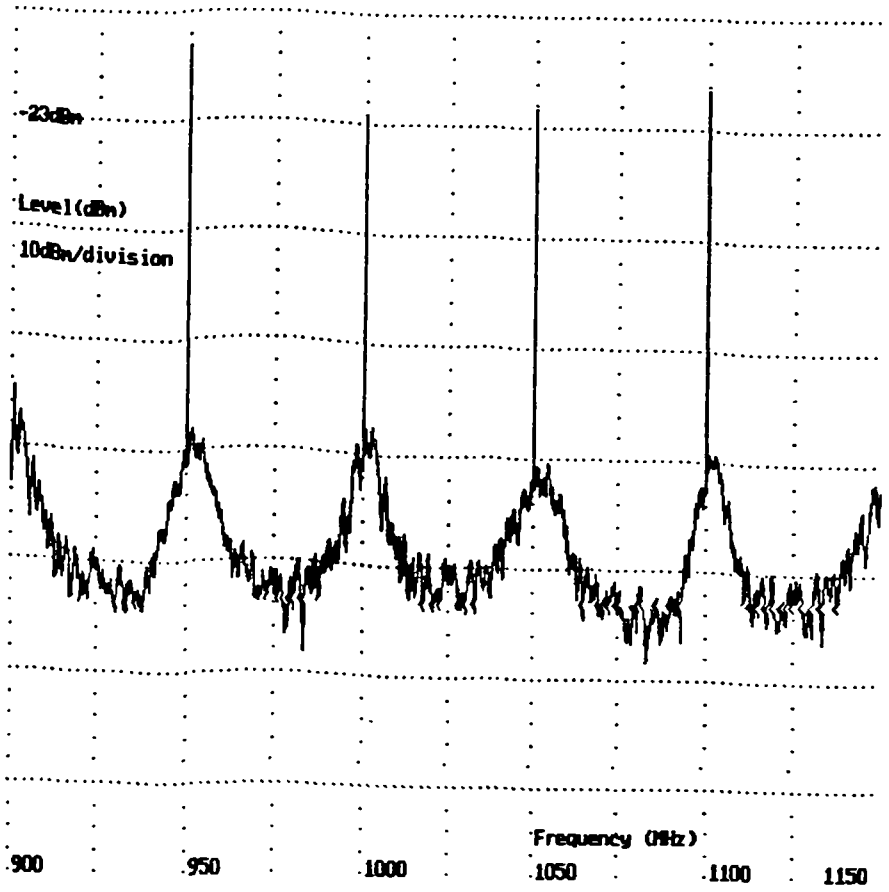


Fig 7.23 Rf additive noise added, network 1, plot of 10th harmonic with 164Ω load.

A spectrum analyser plot of a comb generator built to a circuit as described in §7.11 and measured by the author is displayed in fig7.48 below.

As the bifurcation point is approached, a plot of the close-to-carrier excess phase noise above the multiplication factor is displayed in fig7.24. It can be observed that the noise stays close to the multiplication factor, until R_X is increased above 110Ω. The phase noise begins to increase and rises rapidly towards the asymptote at the bifurcation point. This effect could have catastrophic consequences for any system if such a circuit is used as a local oscillator.

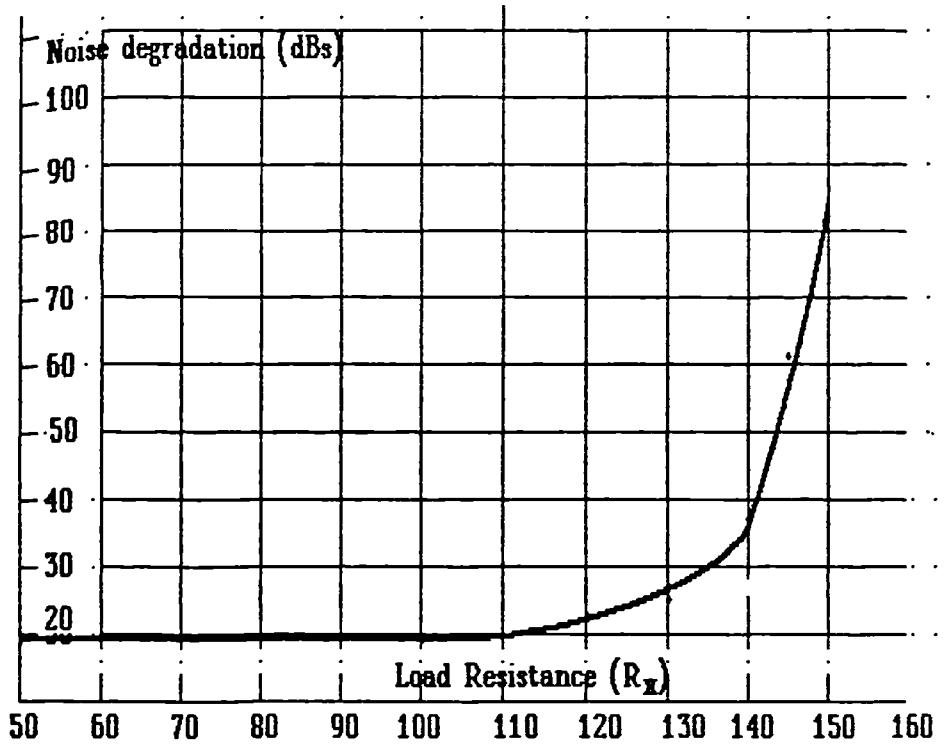


Fig 7.24 Plot of excess noise close to carrier for network 1 against load resistance as bifurcation point is approached

At the bifurcation point, two attractor points appear, but the impulse repetition rate is equal to the input frequency. However, the firing angle takes on of two possible values for each alternate input cycle. After this bifurcation point a region of chaotic behaviour is encountered. In this region, the repetition rate is equal to the input frequency, but the strange attractor α will take on many values, but at a rate of one per cycle. When the load resistance becomes greater than 300Ω, cycles begin to be lost at the output, and on increasing values of R_x still further, a stable carrier storage division region is obtained. Frequency halving is indicated by a colour change to blue on the Feigenbaum diagram, plate 1. Fig 7.25 shows the 10th harmonic of the input frequency with a load resistance of 400Ω. The noise sidebands appear to show a degradation of 8 dB in addition to the multiplication factor, but stable frequency halving is demonstrated.

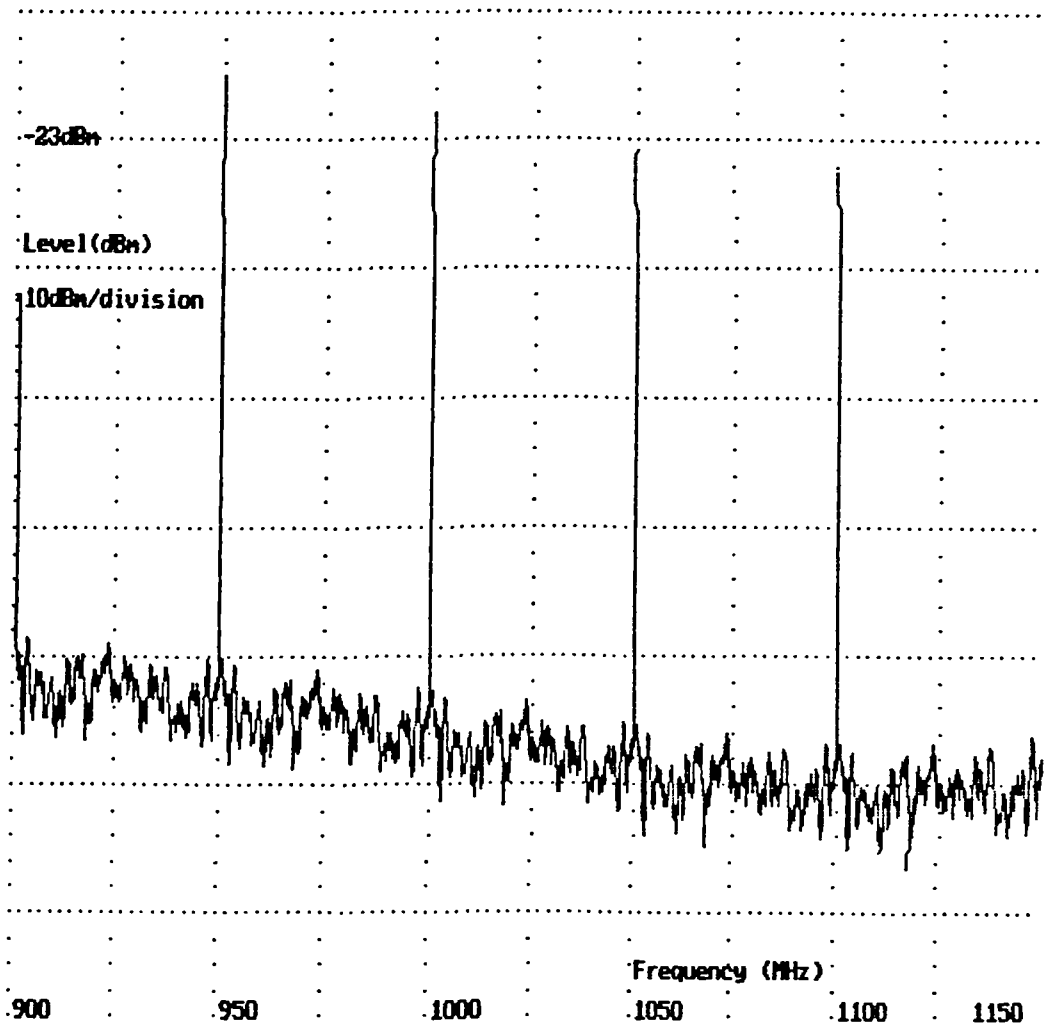


Fig 7.25 Rf additive noise added, network 1, plot of 10th harmonic with 400Ω load

On further increases of load resistance to 500, fig 7.26 is given showing peaking effects between the comb lines as a further bifurcation point is approached. Noise peaks are visible at a quarter carrier frequency indicating the emergence of another bifurcation point, as can be seen from fig7.26. Excess noise degradation above the multiplication factor is now 4dB.

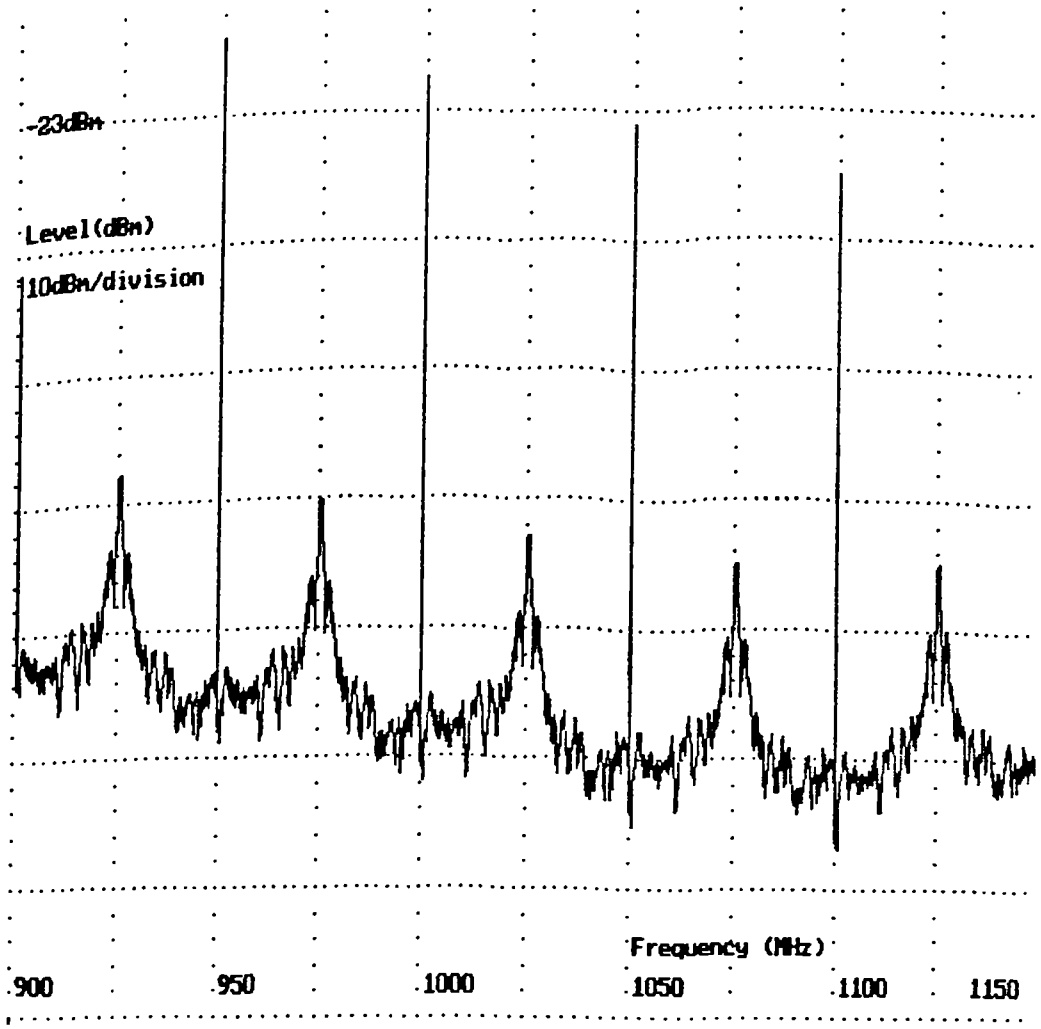


Fig 7.26 Rf additive noise added, network 1, plot of 10th harmonic with 500Ω load

At very high values of load resistance, such as 1300Ω, a further region of chaotic behaviour as displayed as can be seen at point **E** in the Feigenbaum diagram, plate 1. A frequency domain plot, fig 7.27, indicates a continuous spectrum resembling noise. The noise source is turned off to demonstrate that the noisy spectrum resulting is due to the circuit behaviour rather than any noise source. This provides evidence that the noise like structure of the spectrum originates from the chaotic behaviour of the comb generator circuit and exists even there is no noise source present in the circuit. The spectrum is due to chaotic behaviour rather than noise. Another characteristic behaviour of such a chaotic circuit operation is a drastic change in overall shape of the spectrum for only slight changes in load resistance, and there are windows in the chaotic region where a discrete line spectrum can suddenly appear.

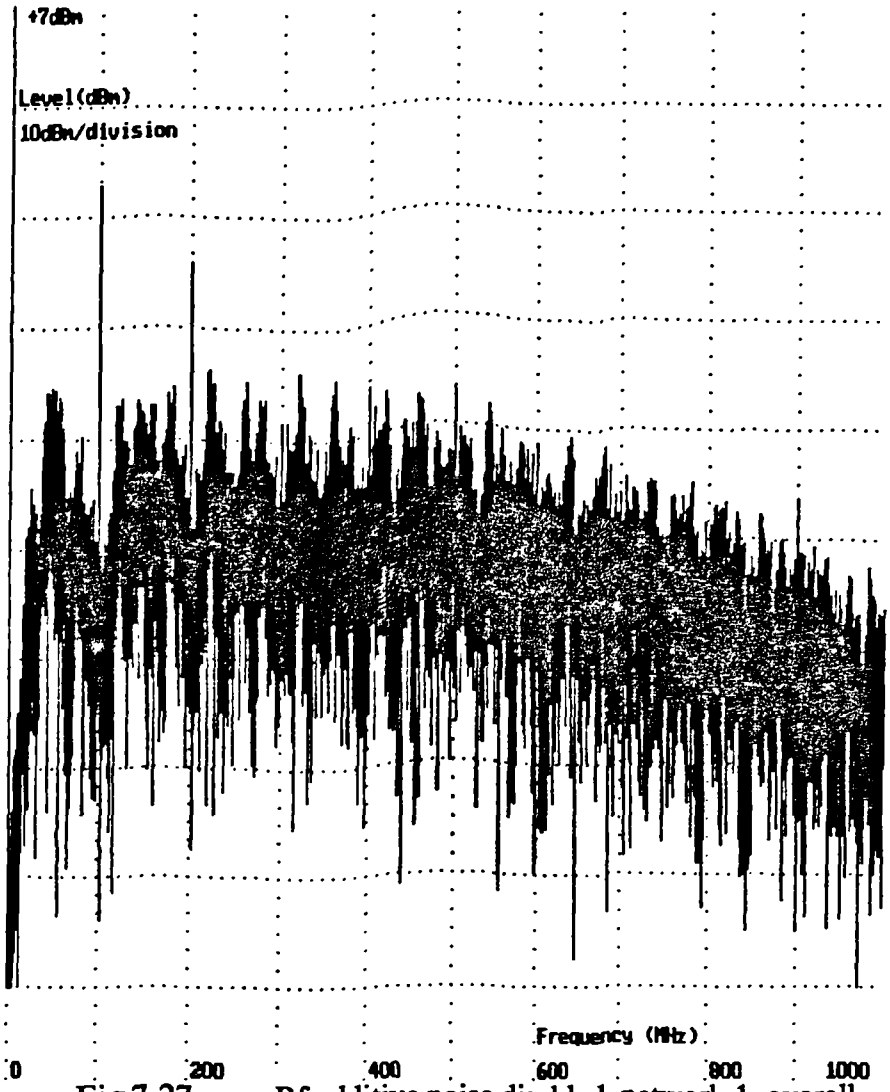


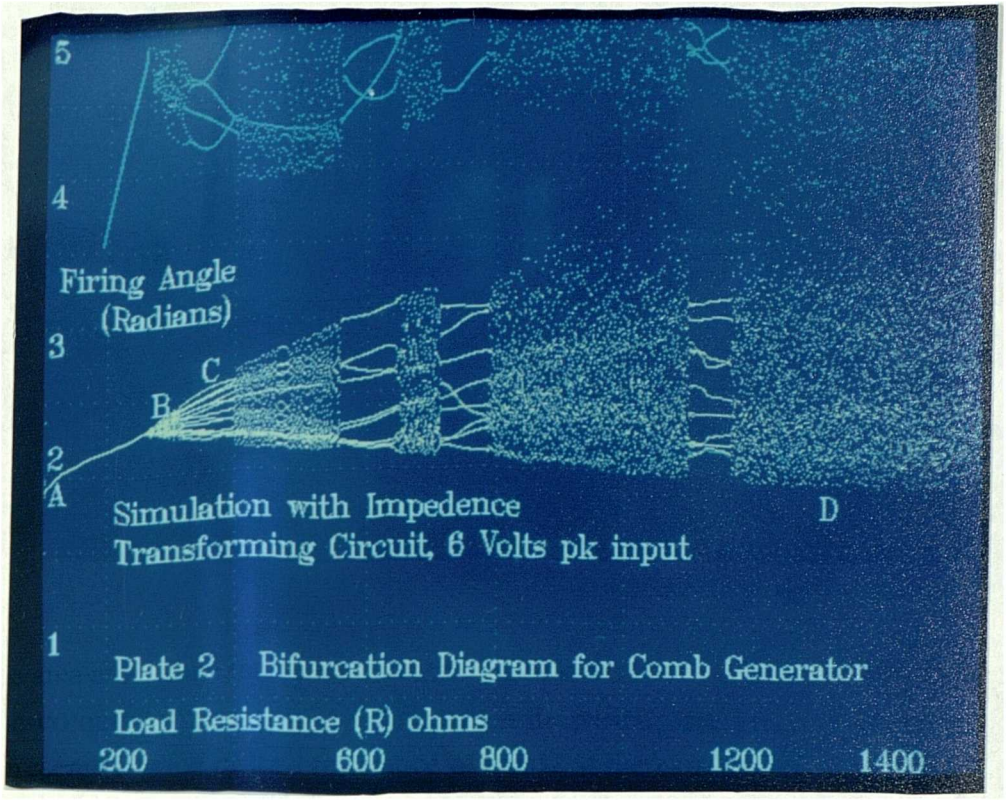
Fig 7.27 Rf additive noise disabled, network 1, overall spectrum showing chaotic behaviour with a 1300Ω load

The Feigenbaum diagram indicates that the phenomenon is not noise, since noise would result in a random spread of points on the display. The display is not random, but forms a pattern characteristic of chaotic systems.

7.8.2 Multiple bifurcations

A particular form of bifurcation diagram that relates to period doubling chaos is given by a Feigenbaum diagram. Such a form of chaos describes effects resulting in the formation of half carrier subharmonics. As mentioned in §7.6.2 other forms of chaos are possible. If the comb generator is driven by the high inductance matching transformer circuit of network 2, fig7.7, §7.5.1, then another form of chaos common in RF non-linear circuitry is possible. This results in the chaos developing close to the RF carrier frequency rather than half carrier frequency. The bifurcation diagram corresponding to values given in table7.1 is given in plate2. A scale of colours are used to represent the different periods between the firing of the SRD. The white dots appearing higher up the

graph represent double pulsing, that is more than one pulse is being produced per input cycle.



The area around the multiple bifurcation point is expanded to give the plot of fig7.28. The colours representing the different time periods are given in §7.5.7.4. Point A represents a value of load resistance of 100Ω at the extreme left of plate2. At such a value of resistance, the comb generator is displaying normal harmonic generator operation and fig7.29 illustrates the output spectrum. This spectrum is formed from RF additive noise at the input and by a load resistance of R_X=100Ω; showing the effect of "parametric gain" increasing the level of noise above the theoretically expected level. Noise sidebands are increased at a frequency of approximately 20MHz away from the carrier by 10dB above the theoretical 20Log$N$. The increase is sustained for offset frequencies greater than 20MHz offset frequencies. However, the noise floor is free from any peaking under these conditions. Any spurious signals on the input carrier signal at an offset from carrier frequency of 20MHz would also be raised by a factor of 10dB in addition to the multiplication factor. If the transfer function of a phase locked oscillator including a SRD as a comb generator fails to include this additional factor in the synthesiser spurious signal calculations, the synthesiser will perform worse than expected and may well fail to meet any specifications for spurious signals.

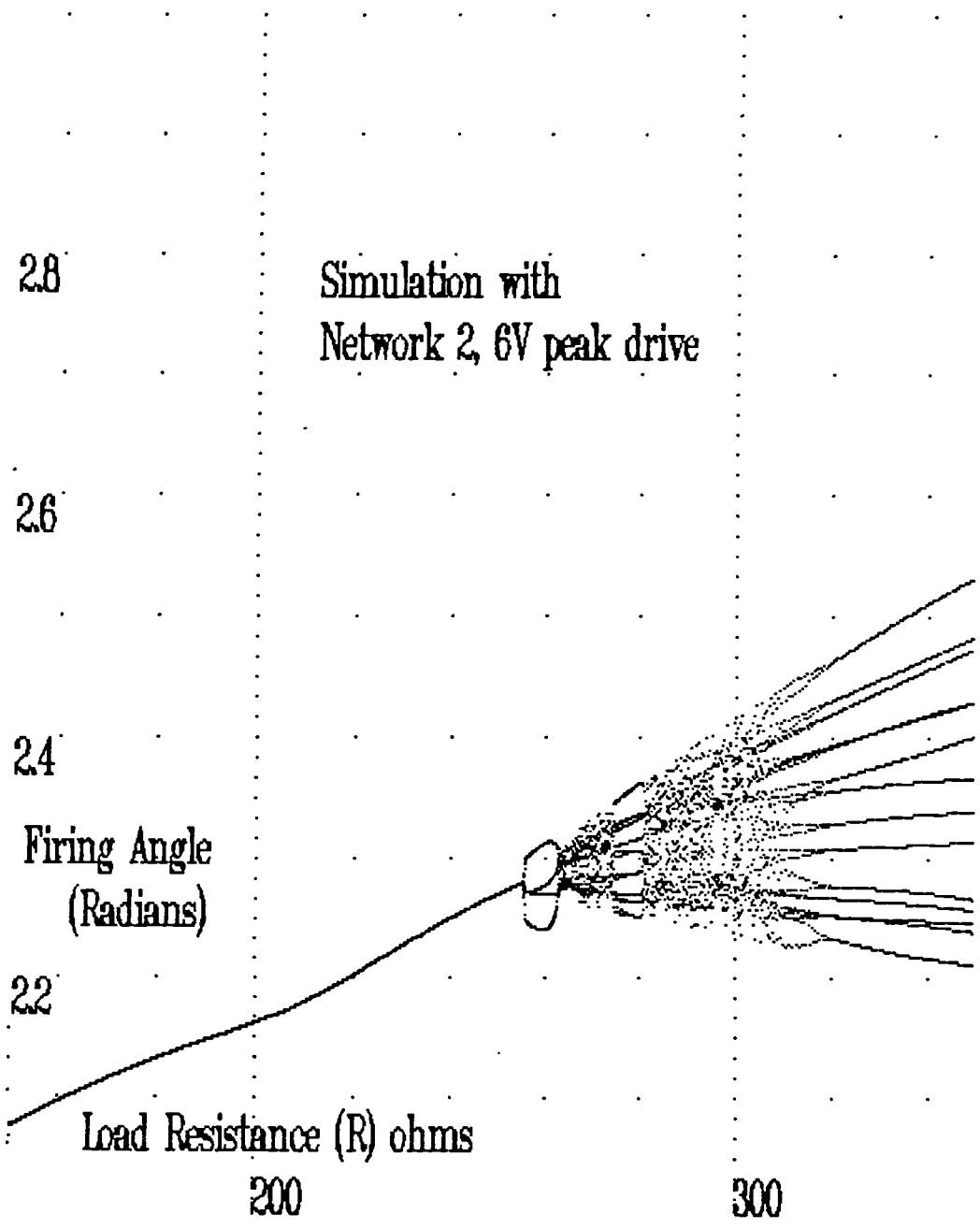


Fig 7.28 Plot of enlarged area of multiple bifurcation point, plate2

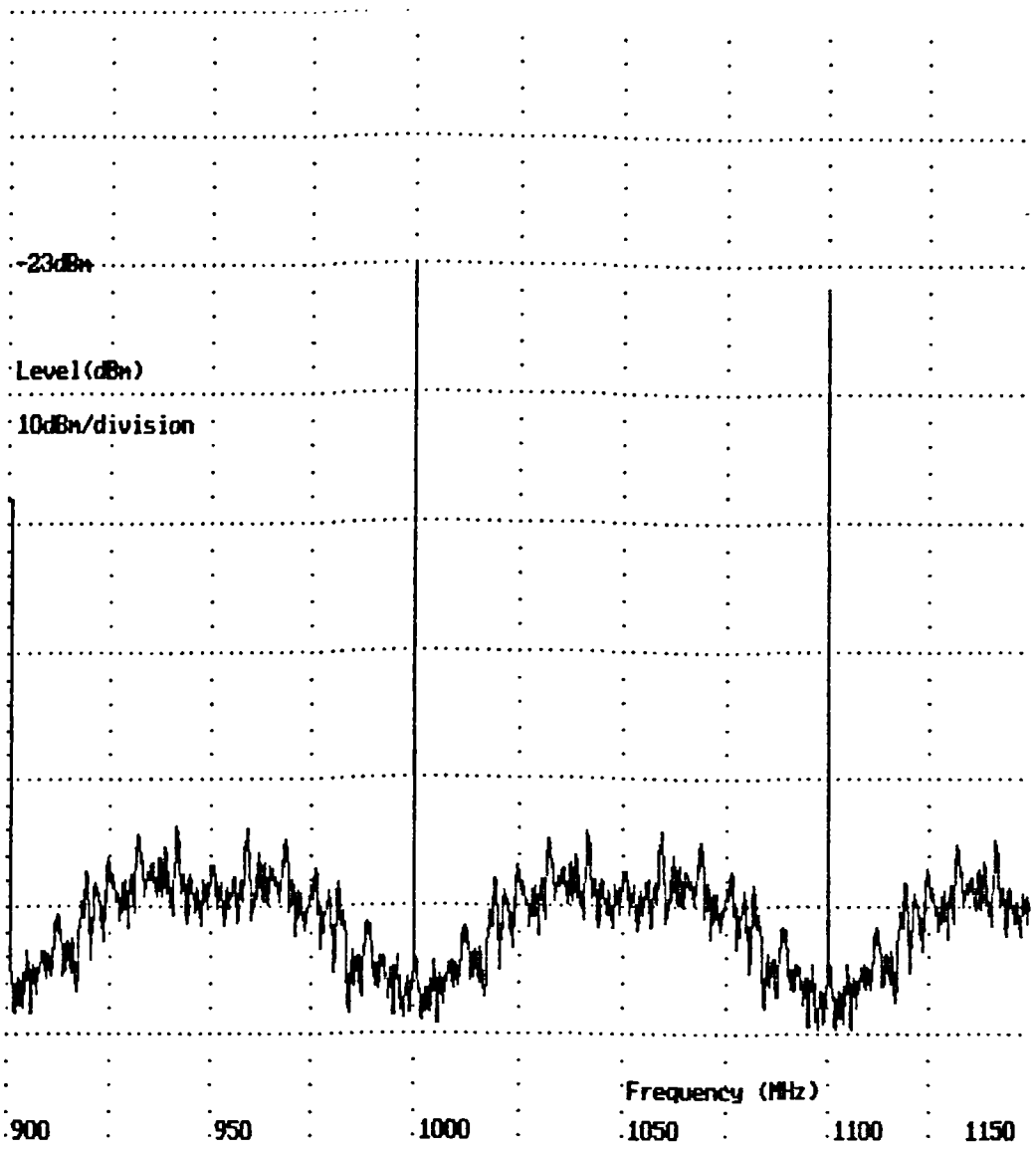


Fig 7.29 Plot of comb generator with 100Ω load, network 2.

Increasing R_X to 270Ω at point B just before the multiple bifurcation point on plate 2 results in the appearance of noise peaks around the carrier frequency as shown in fig 7.30. Peaking of the noise floor in SRD circuits has also been demonstrated by measurement [Scherer, 1981]. Again as the bifurcation point is approached, the phase noise is increased. With network 2, there exists a multiple bifurcation point, that is the attractor α branches into many points; this effect is further discussed in §7.9.5.

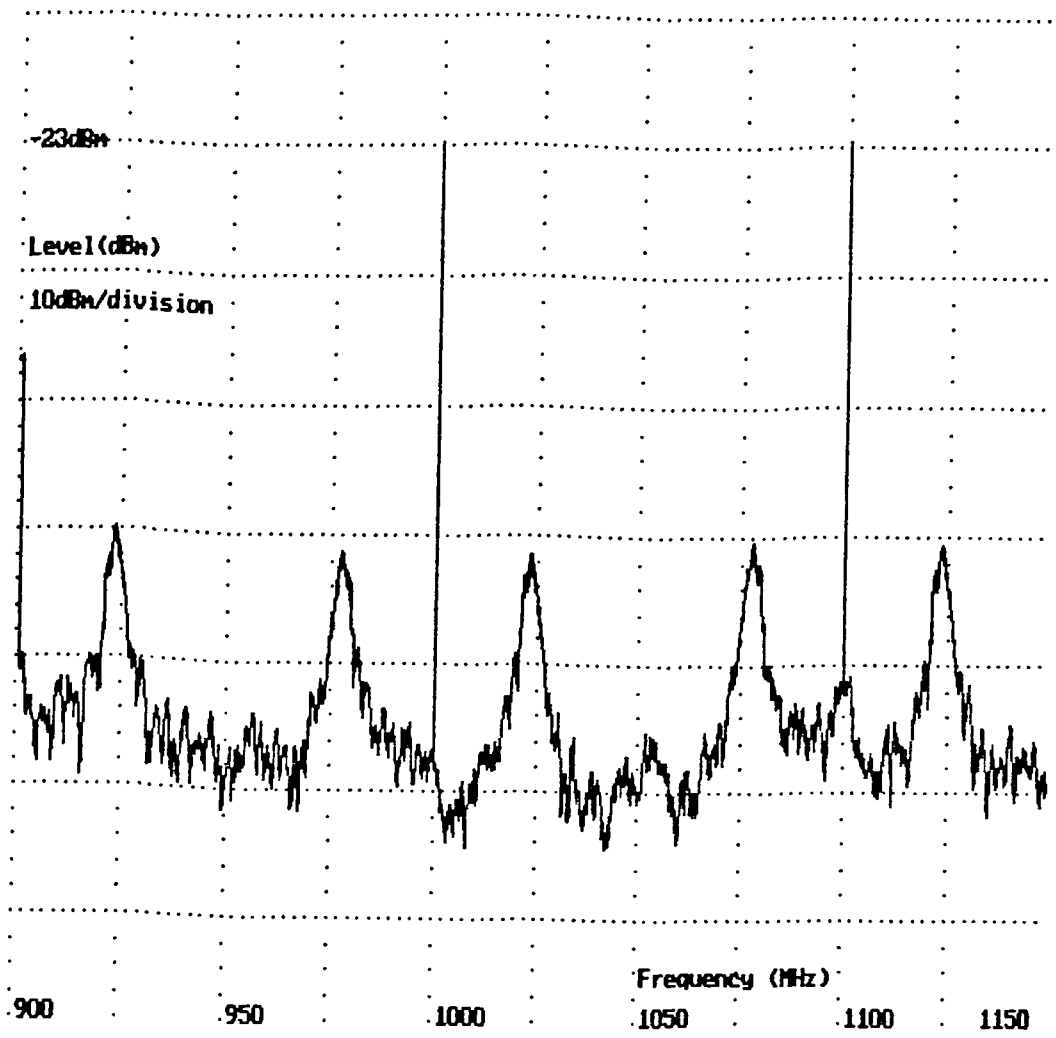


Fig 7.30 Plot of comb generator with 270Ω load, network 2.

At point C, an FFT of the spectrum, fig 7.31, displays the degeneration of the circuit performance into chaos for a load resistance of 350Ω. Close to carrier noise is raised by 20 dB above the multiplication factor theoretical level and spurious signals are appearing at large numbers of offset frequencies. This spectrum is typical in cases where the close to carrier form of chaotic behaviour occurs.

Such form of chaos can also be observed in class C RF power amplifiers [Luettgenau, 1973] where the effects are potentially destructive.

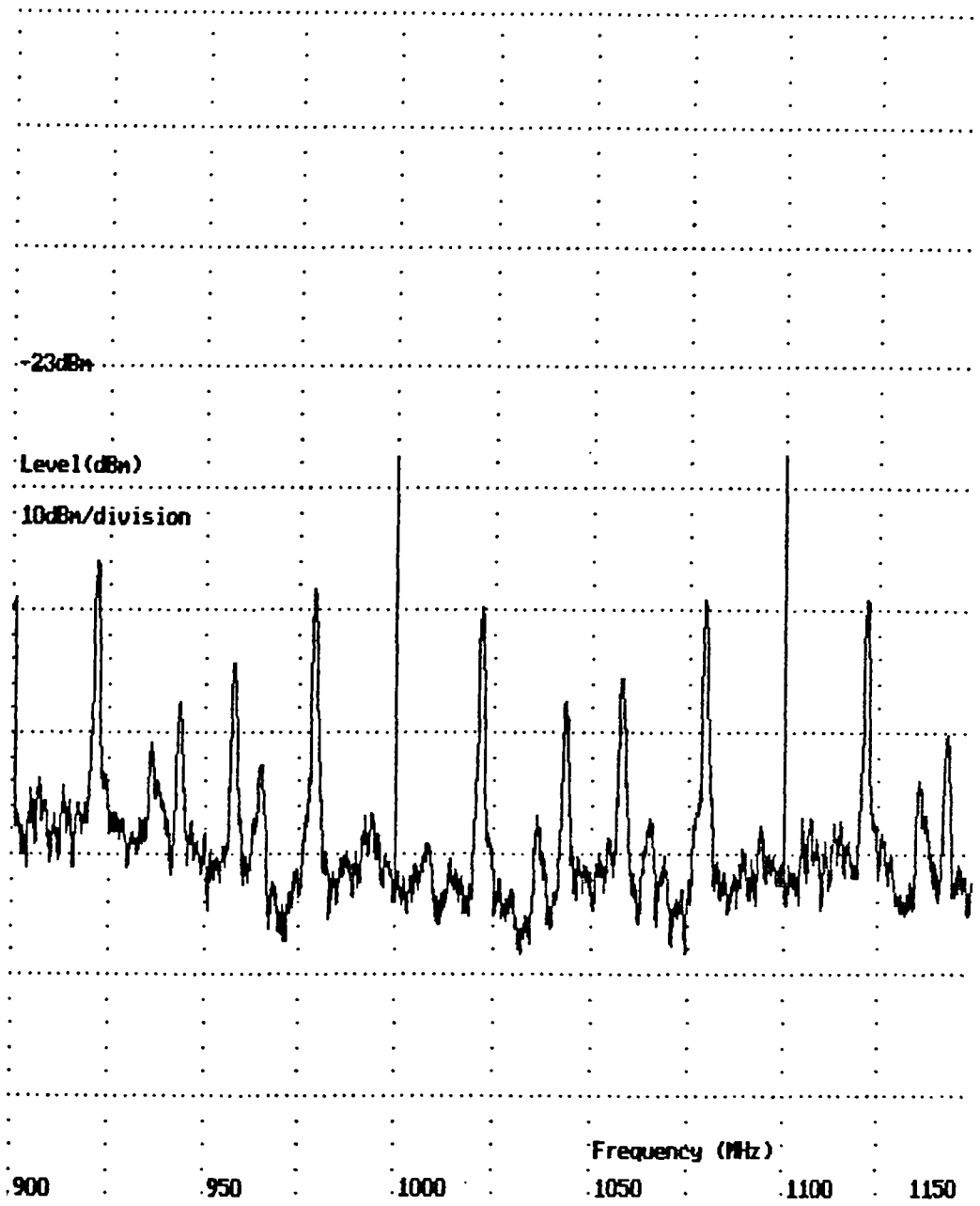


Fig 7.31 Plot of comb generator with 350Ω load, network 2.

Raising the drive level to 12 volts peak with network 2 gives another bifurcation diagram, plate 3. In this case there is variation in the number of successive missed cycles as revealed by the numbers of colours in the diagram. The time domain plot, fig 7.11 reveals that this is the case.

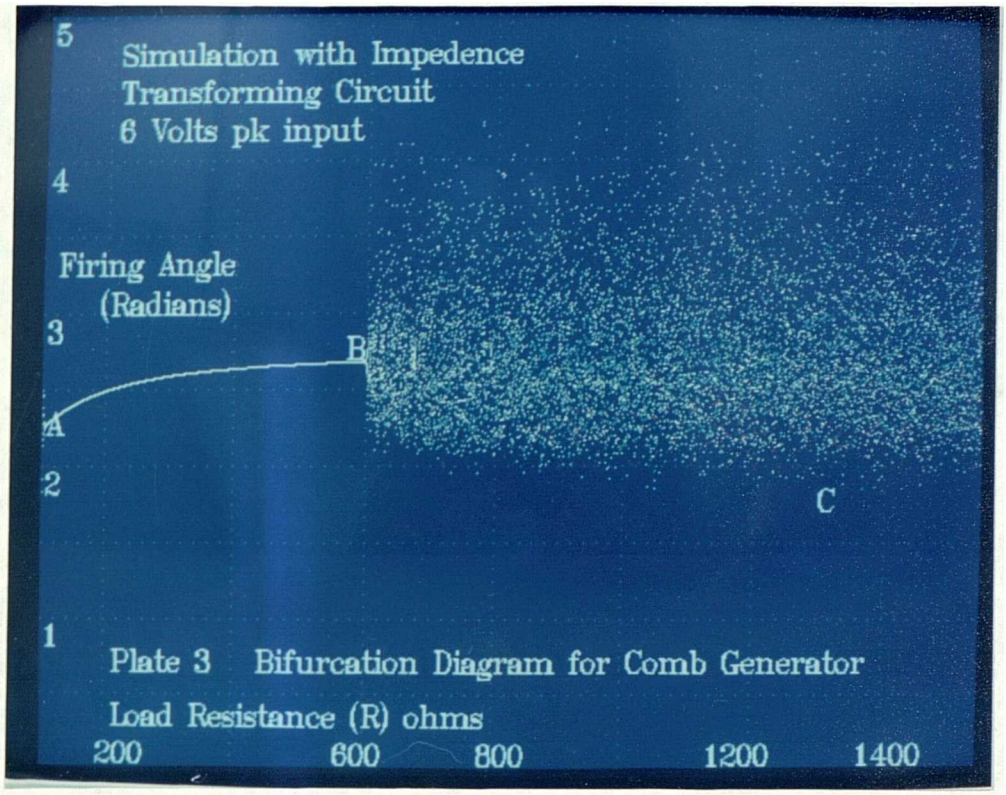


Plate 3 Bifurcation Diagram for Comb Generator

7.9 Recurrence relationships and bifurcations

7.9.1 Introduction to recurrence relationships in SRD circuits

Having demonstrated that bifurcations have important implications for the phase noise performance of a SRD comb generator in the previous section, the origin of the bifurcation effect in such circuits will be discussed here.

Feigenbaum published a paper [Feigenbaum, 1978] demonstrating the universality of the bifurcation effect. This universality applies to systems that contain some form of recurrence relationship ie:-

$$x_n = f(x_{n-1}) \tag{7.57}$$

For dynamical systems a steady state solution exists when:-

$$x_n = x_{n-1} \tag{7.58}$$

For this reason, x_n is called the attractor.

Carrier storage effects could contribute to the recurrence relationship since the quantity of charge stored affects the firing angle α; in turn affecting the the charge stored in the next period. In studying chaotic behaviour of the comb generator it is convenient to make the firing angle α be the attractor.

7.9.2 Contribution to the recurrence by the SRD impulse

One mechanism by which the stored charge in one cycle affects the stored charge in the successive cycle will be discussed here. A change in the level of stored charge as a result of firing angle changes alters the current flowing in the diode at the onset of the impulse I_p. A relationship between the current I_p and the reverse impulse can be obtained from equation 7.2:-

$$V_d = \frac{I_p}{2C_d\beta}\left(\exp-(A - \beta)t - \exp-(A + \beta)t\right) \tag{7.59}$$

where A and β are as defined in §7.3.3. When the forward cycle commences, the energy remaining from the impulse response contributes to the recurrence effect. This contribution depends upon the value of β. A plot of the residual energy after the impulse interval against the value of load resistance R_x is given in fig7.32. Point A corresponds to a damping factor ζ of unity, where ζ is given by:-

$$\zeta = \sqrt{1+\left(\frac{\beta}{\omega_o}\right)^2} \qquad \omega_o = \sqrt{\frac{1}{LC}} \tag{7.60}$$

A value of unity for ζ occurs at a load resistance R_x in ohms of:-

$$R_x = \sqrt{\frac{L}{4C}} \tag{7.61}$$

With the values used for network 1, this corresponds to a value of 95.3 Ω for R_x.

As can be seen from fig7.32, on decreasing ζ below 1, the energy contribution to the next cycle increases substantially.

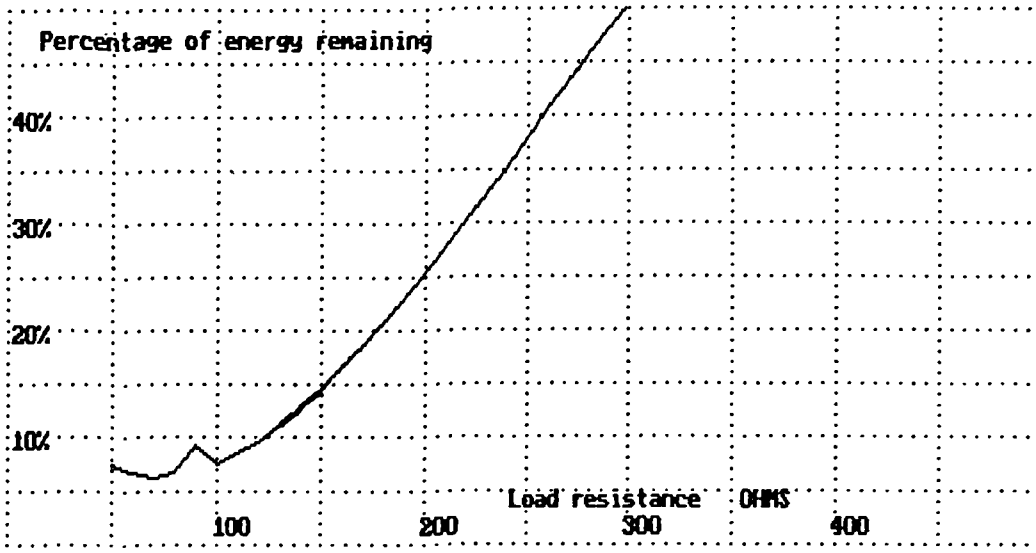


Fig 7.32 Plot of residual impulse energy against damping factor at termination of impulse period

7.9.3 Determining stability from recurrence relation plots

A plot of the recurrence relationship for α was obtained from the time domain simulation. The initial conditions of the simulation were varied and a plot made of the resulting values of α.

Plots of α_n against α_{n-1} are illustrated in figs7.35 to 7.38. These plots are obtained by monitoring the firing angle in the first period and storing this as α_{n-1}. In the succeeding period, the firing angle is stored as α_n. A complete plot can be built up from as little as 20 cycles making this a rapid method of evaluating stability. A straight line is plotted on the graph representing $\alpha_{n-1} = \alpha_n$.

Figs7.33 and 7.34 illustrate possible relationships between α_n and α_{n-1}. The shaded curve is the recurrence relationship, and the solid line a possible locus of the value of α to the attractor.

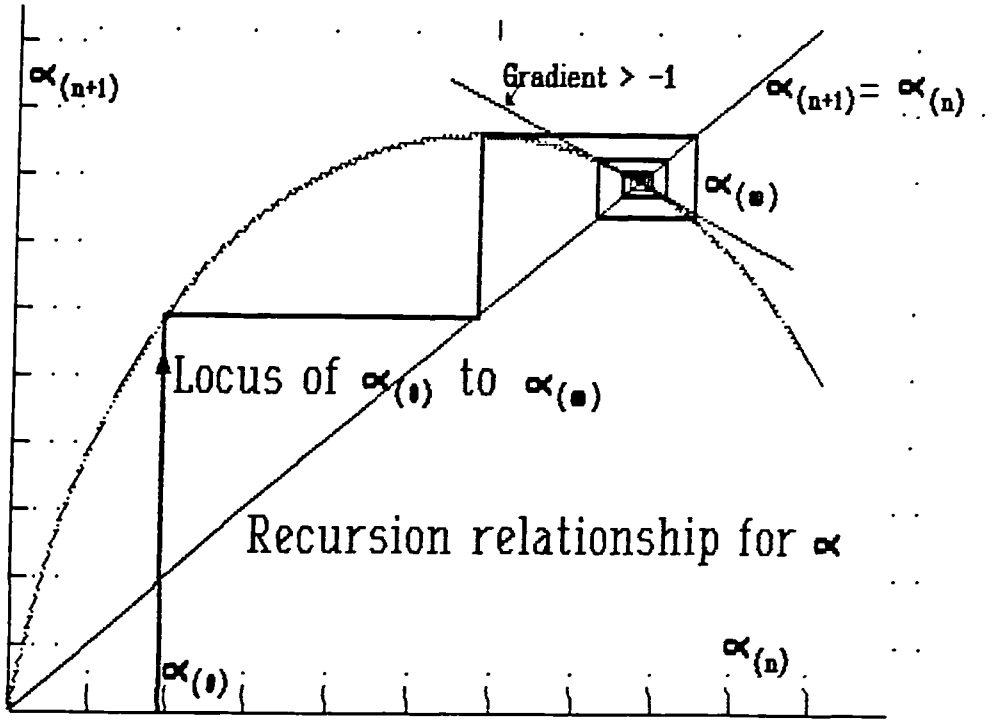


Fig 7.33 Recurrence relation: damped oscillatory locus to the attractor α_∞

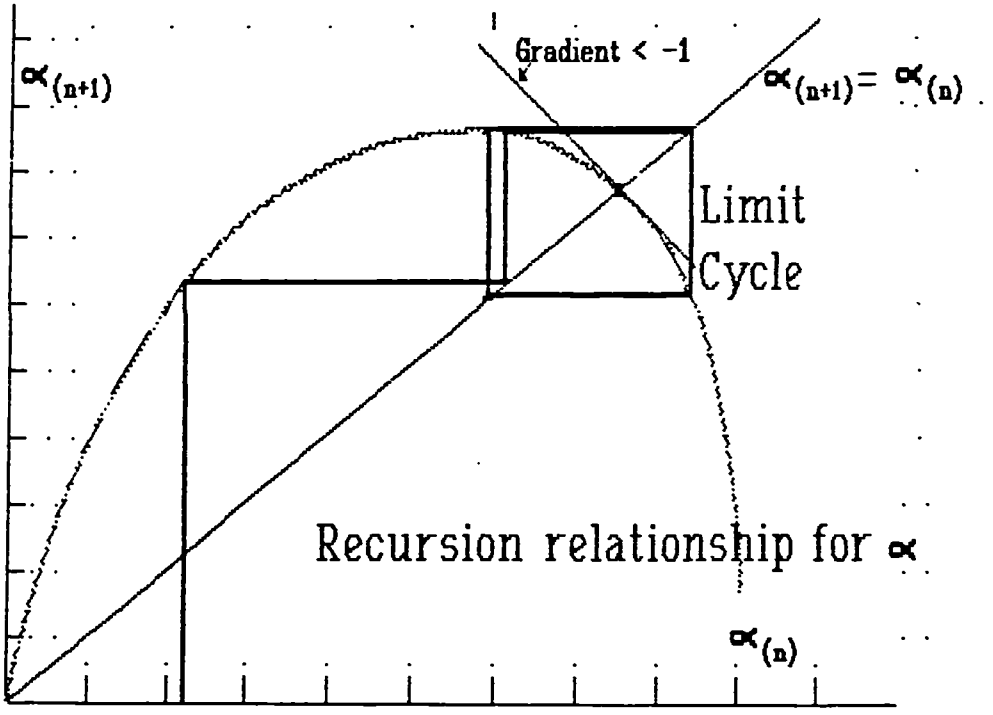


Fig 7.34 Recurrence relation: limit cycle attractor

Feigenbaum [1978] suggests that the gradient of the recurrence relationship determines what form the convergence of α_n takes to the attractor α_∞: a positive slope suggests monotonic convergence, a fractional negative slope gives a damped oscillatory convergence for example in fig7.35, and a slope of -1 gives the limit for convergence to a singular attractor α_∞. If the absolute value of the slope is greater than -1, for example in fig7.36, then the recurrence trajectory will diverge away from α_∞ in an expanding locus until the geometric mean of the slopes at α_2 and α_1 is unity. At this point, a stable recurrence occurs between α_2 and α_1. This trajectory is known as a "limit cycle oscillation" and occurs in many cases such as digital filters [Rabiner & Gold, 1975]. The transition point between singular α_∞ and limit cycle oscillation gives a bifurcation point. The bifurcation point is therefore defined as the point where the gradient is:-

$$\frac{d\alpha_n}{d\alpha_{n-1}} = -1 \tag{7.62}$$

It is possible for the limit cycle oscillation to be unstable, such as in fig7.36, where successive cycles result in the geometric mean being alternately greater than or less than unity. In this case a further bifurcation is possible. This situation occurs in the bifurcation diagram at point D'.

The recurrence plot ceases at a particular value of α_{n-1}. If α_{n-1} exceeds this, the charge in the next forward mode will not decrease to zero, therefore the impulse will not occur in that time period. Therefore if the limit cycle oscillation extends beyond the maximum point of the recurrence relationship, a cycle is omitted, and an impulse occurs at every alternate cycle.

In the case of the plot, fig7.35, for $R_x = 50\Omega$ the slope is of value -0.25 indicating a non monotonic convergence with limited oscillation.

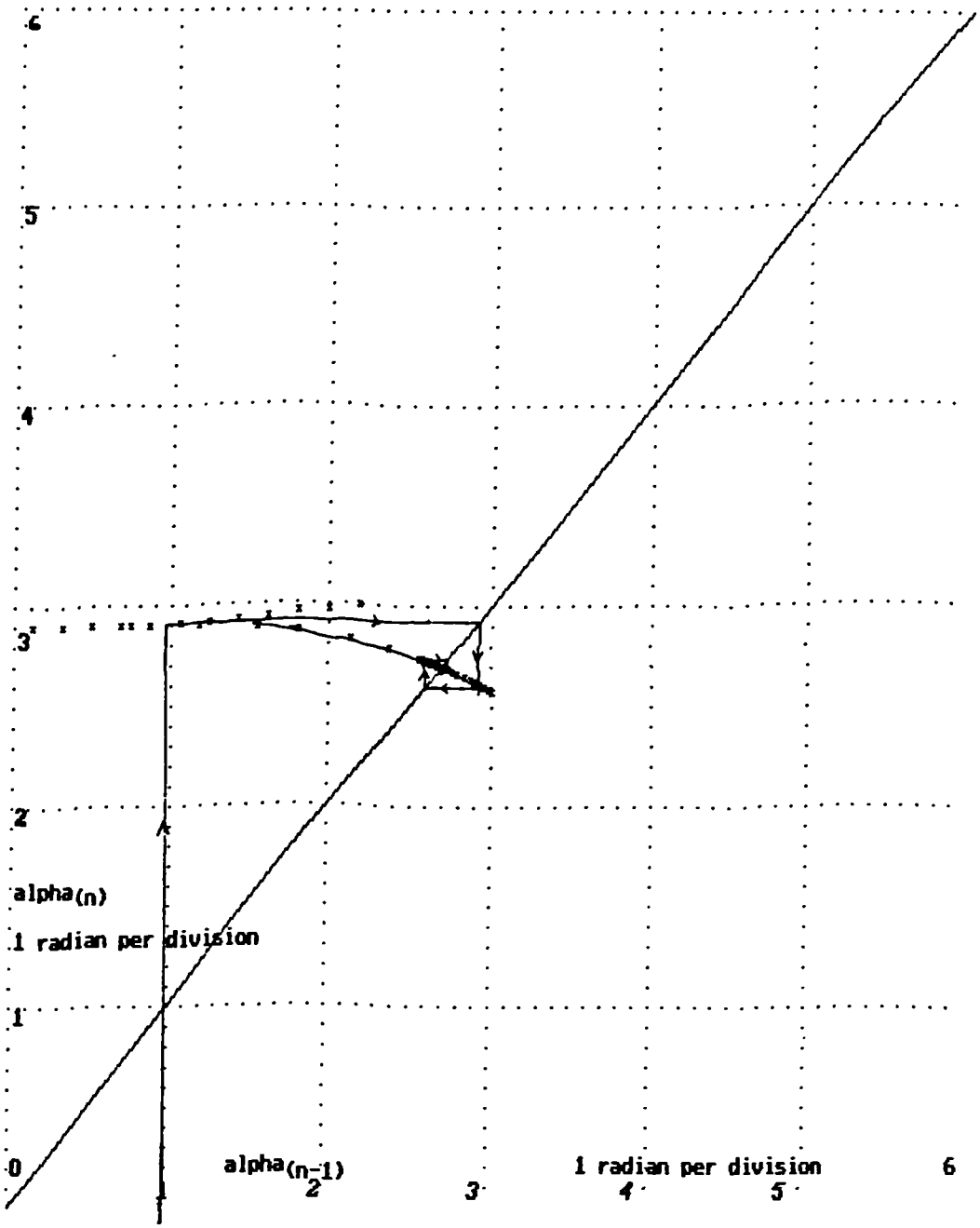


Fig 7.35 Plot of recurrence relationship with 50Ω load resistance

For R_X = 100Ω the slope is now -0.75. Onto fig7.36 is traced the trajectory of the recurrence to a value of α_∞ for the case of R_X = 100Ω. Fig 7.36 indicates that the convergence *is non-monotonic* with many *oscillation* cycles before α_∞ is finally reached. In the case of R_X = 100, although a convergence occurs to a singular value α_∞ there is considerable oscillation before the final value is reached. This oscillation in the time domain results in peaking in the frequency domain. This can be clearly seen in fig7.21, §7.8.1, which is a FFT plot of the time domain *simulation* of network 1 with a 100Ω load. The noise peaks up by 14dB in this case, and could be a potential embarrassment to the performance of a system that includes such a circuit in its local oscillator.

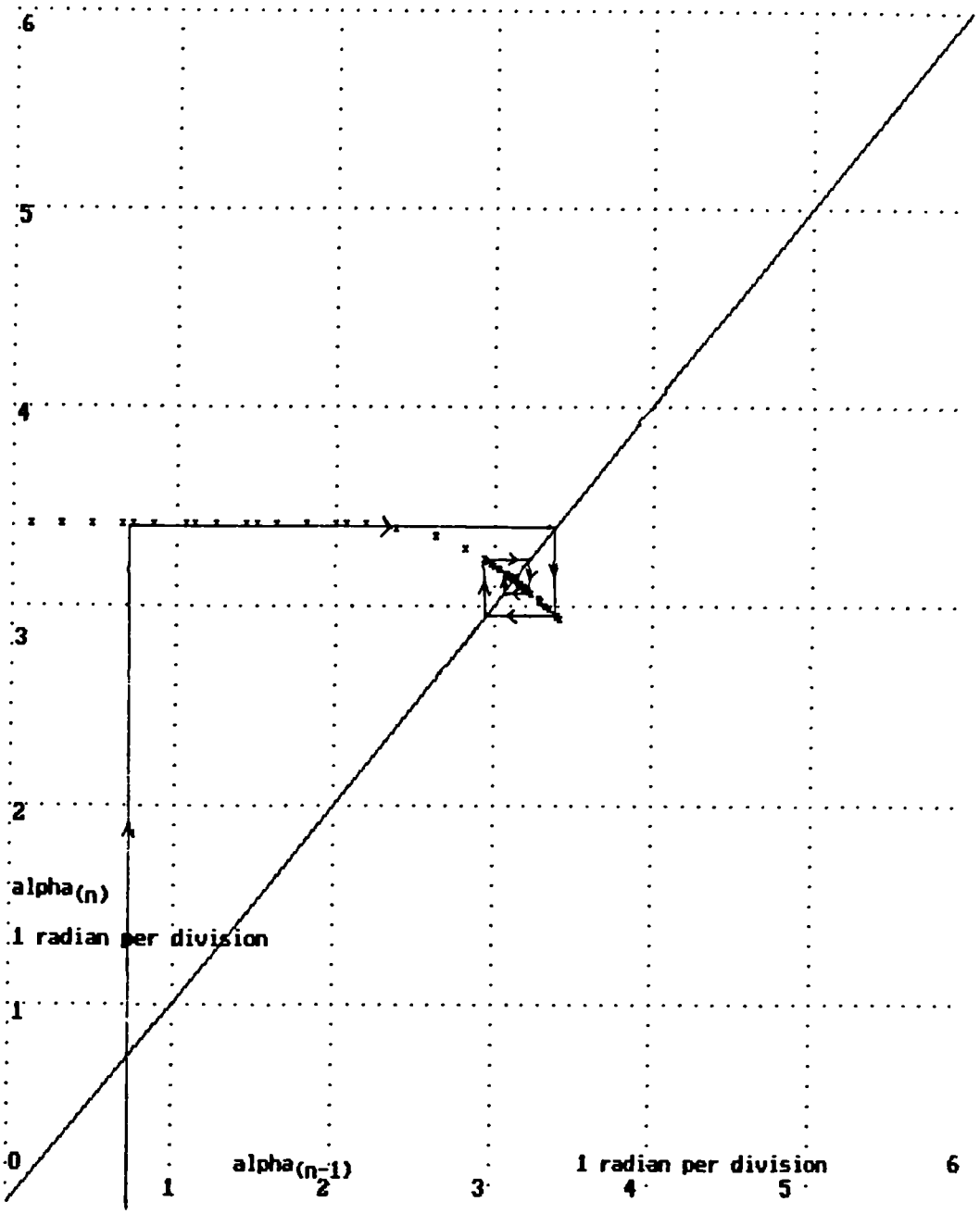


Fig 7.36 Plot of recurrence relationship with 100Ω load resistance

For R_x = 161 Ω at point C, the slope is -1, corresponding to the bifurcation point. This can be seen in the plot 7.37. Stable limit cycle oscillations occur when the geometric mean of the gradients at the intersection of the oscillations with the recurrence curve of α equals -1.

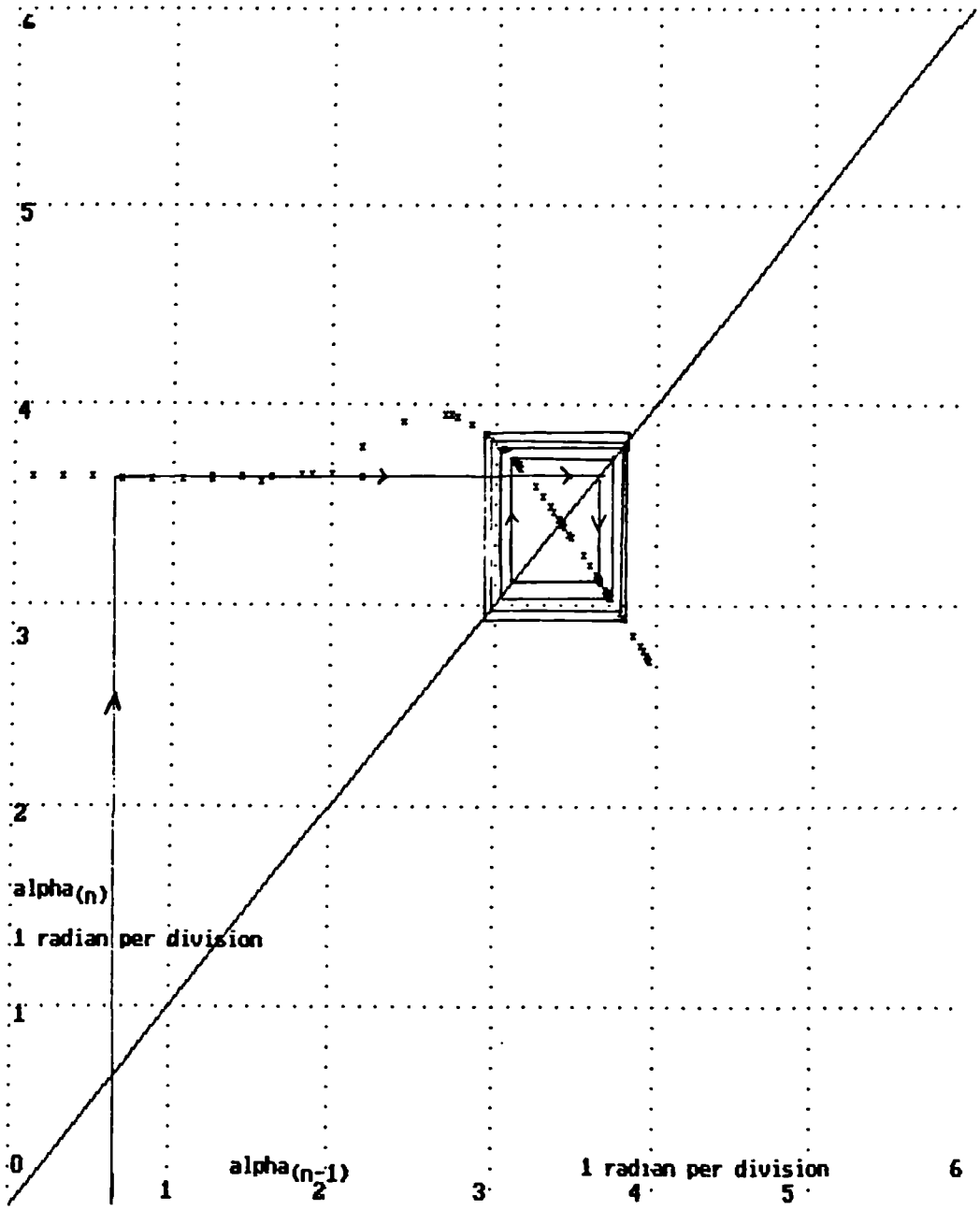


Fig 7.37 Plot of recurrence relationship with 161 Ω load resistance

Increasing the value of R_x beyond this in fig 7.38 results in the limit cycle oscillation developing as indicated by the rectangle at the intercept between y = x and the recurrence curve. In this case the limit cycle oscillations are unstable, leading to further bifurcations.

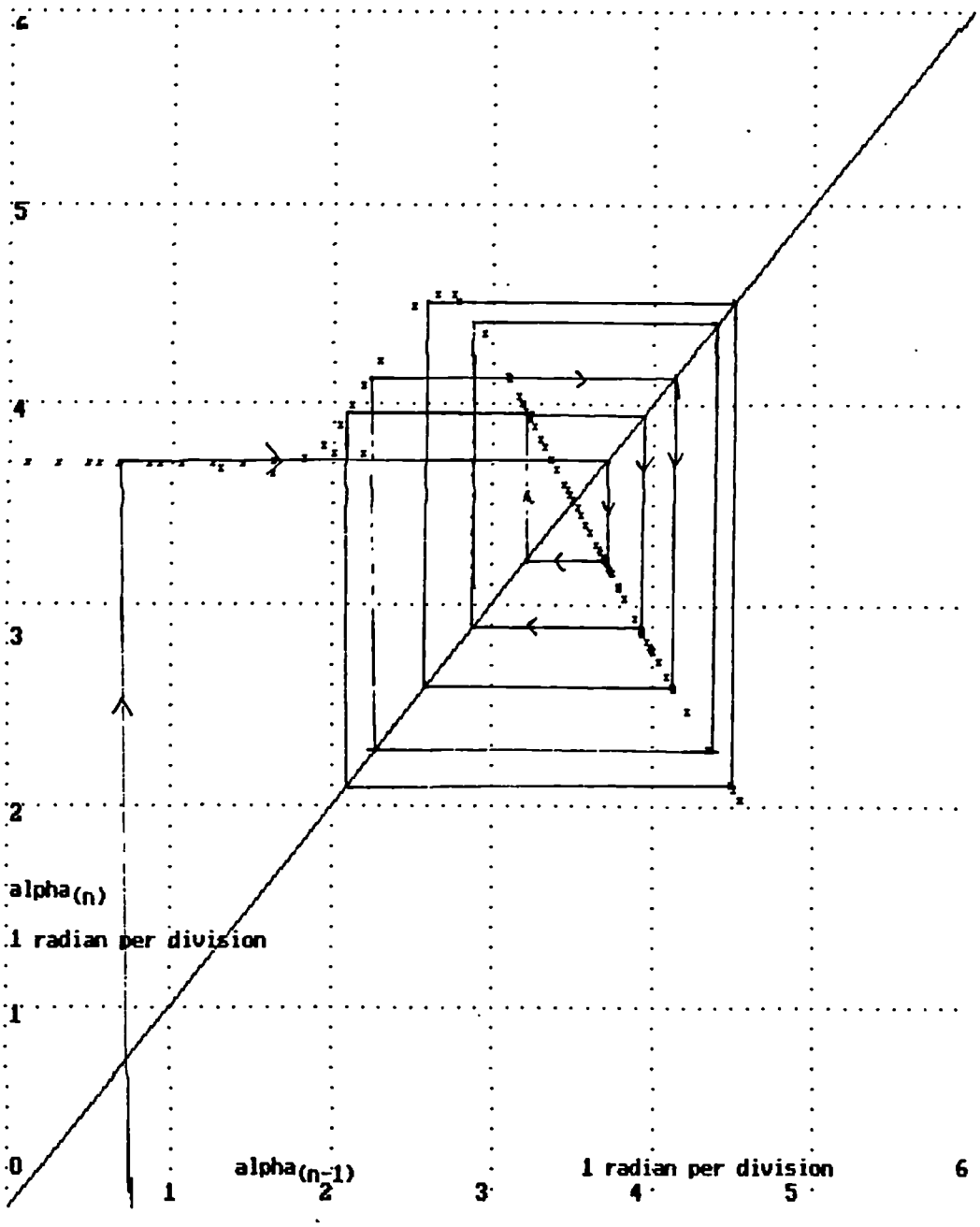


Fig 7.38 Plot of recurrence relationship with 200Ω load resistance showing unstable limit cycle oscillation

7.9.4 Other contributions to the reccurrence relation

The oscillatory convergence cannot be totally explained by energy remaining after the reverse impulse, however. According to fig7.32, there is little energy transferred from the previous cycle through the reverse impulse region for load impedances of less than 100 Ω. Therefore, the quantity of stored charge in one cycle can have little direct effect on the stored charge in the next cycle; although the frequency domain plots of fig7.21 suggest considerable peaking. Another means by which the stored carrier level in one region may influence the charge level in the next region must be found and investigations with the simulation program reveal that it is the phase of the conduction and reverse impulse regions relative to the drive waveform that result in the peaking effect. Increasing the duration of the conduction mode past the equilibrium value results in an increase in the phase angle of the impulse region. Such an increase in phase angle results in an increased drive voltage being applied to the impulse coil towards the end of the impulse period, thus shortening the impulse period. This increased drive results in the onset of the next forward region being delayed further towards the end of the positive going half of the input drive waveform. Consequently, the maximum charge level in the intrinsic region of the SRD will be lower, thus a shorter charge removal time will be required. Since both forward and reverse regions are shorter in time duration, an increase in firing angle for one cycle results in a decrease in the firing angle for the next forward cycle.

As can be observed from fig7.32, an increase in the slope of the recurrence relationship corresponds to an increase of the energy fed forward from the previous cycle. It is implied therefore that a high value of damping factor would be necessary to ensure stability. Unfortunately, however, a high damping factor would result in poor output at high harmonic frequencies. To ensure that sufficiently large amounts of energy are available at higher harmonics it is necessary to operate the comb generator at a low damping factor. This is particularly the case with a frequency multiplier which must operate at maximum efficiency. This poses a problem with respect to stability. A plot of the recurrence relationship would considerably ease the risks associated with the design of comb generators and multipliers. Multipliers must frequently operate in conditions of extreme temperatures such as at antenna mountings. When a low damping factor is used, the recurrence curve gradient changes rapidly. Although a multiplier may exhibit monotonic convergence at room temperature, this may not be the case at other temperatures. In fact the operating point may pass right through the region of oscillatory convergence and through a bifurcation point. Disastrous effects on system performance will therefore ensue. Fig7.39 displays a 10GHz multiplier that displayed such an instability over temperature.

As a result of the stability problem, the extra complexity of a comb generator driven PLO over a multiplier can be justified when the local oscillator must operate over a wide temperature range.

This section has shown that there are three effects that determine the stability of the SRD comb generator:-

1) Carrier storage effects resulting in failure to switch to the impulse mode during some cycles. This is characterised by a discontinuity in the recurrence curve.

2) Energy stored in the SRD reverse capacitance and impulse inductance remaining after the termination of the impulse mode, revealed by sharp curves in the recurrence graphs for alpha.

3) Phase relationships of the regions with respect to the input waveform result in a gentle curve in the recurrence plots. A connection between this stability effect and the shape of the driving waveform is therefore indicated.

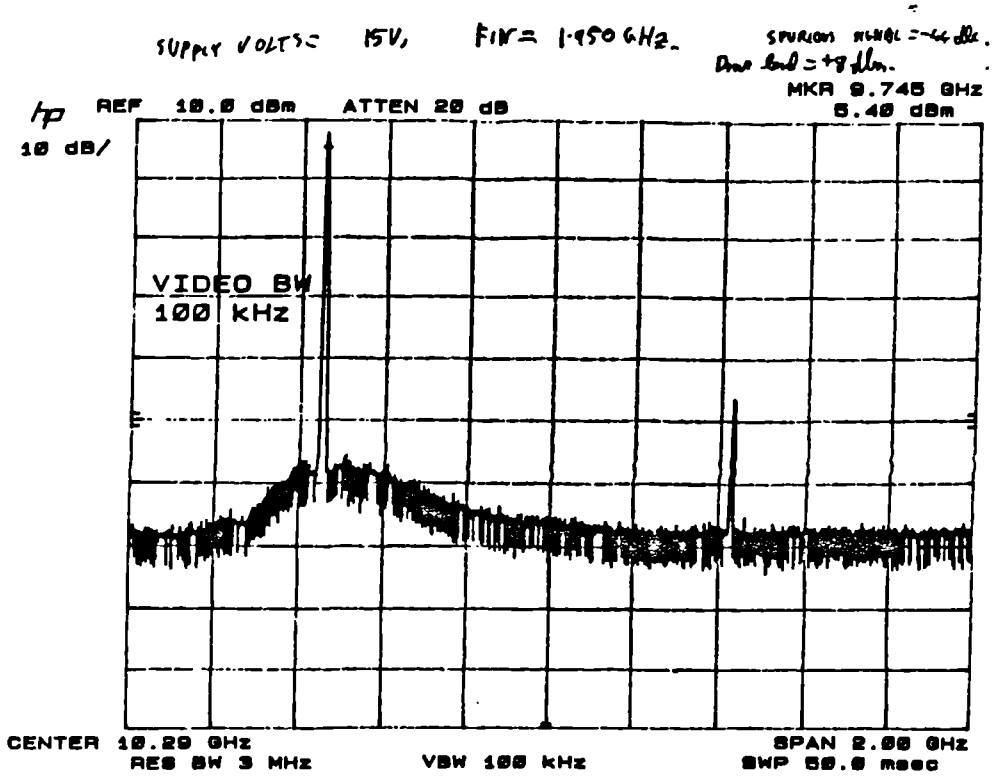


Fig 7.39 Spectrum analyser plot of a 10 GHz multiplier displaying period doubling

Further work, not covered by this thesis, would be required to assess the effect on stability of the shape of the driving waveform.

7.9.5 Recurrence relation and multiple bifurcation points

The recurrence relationships so far discussed are for a single dimensional recurrence map which result in period doubling bifurcations. More complex behaviour results if a multi-dimensional recurrence map exists for a particular configuration [Lauwerier 1986b]. Such is the case for network 2 using the matching transformer, where the phase of the voltage across the reflection capacitor and the SRD firing angle enter into the recurrence relation. With the one dimensional recurrence relation, the limit cycle attractor can only move out from the sink in two directions on a single line, therefore each bifurcation results in successive period doubling. With a multidimensional recurrence, the limit cycle attractor can move out from the sink in many directions, resulting in the limit cycle looping round many points. Therefore the bifurcation point becomes a multiple bifurcation point as shown in plates2 and 3. The fact that the attractor can break into a long limit cycle enables the chaotic phenomena to develop at close to carrier frequencies rather than at half carrier for period doubling chaotic behaviour. It is beyond the scope of this thesis to examine multi-dimensional recurrence relationships in more detail, but is recommended as a topic for further research.

7.10 Results of simulation: other noise effects

7.10.1 Flicker noise from the driver stage

The simulation work discussed so far used additive noise modulation on the input. Other noise modulations are considered here and are of interest primarily as possible means of introducing $1/f$ noise.

7.10.2 Frequency domain plotting of the simulations with phase noise on the input

Plots were obtained for both networks using phase noise on the input carrier and load resistances of 100Ω. The plots closely resembled the additive noise plots and are therefore not presented here. Approximately $20\log N$ of degradation in the noise floor is revealed.

7.10.3 Effect of AM noise

AM noise is of interest because a mechanism exists for introduction of $1/f$ noise as a result of low frequency amplitude variations from the preceding amplifier/ limiter stage. On applying AM noise to network 1 with a 100Ω load resistor, a similar plot to the additive noise plot of fig7.21 is obtained. The noise is raised by 19dB against the noise at the input frequency, that is 1dB less than the multiplication factor. A plot of the output obtained from applying AM noise to network 2 with a 100Ω resistor is displayed in fig7.40. The AM noise is raised 17dB from that at the carrier frequency. There is an increase in upconverted noise away from the carrier as with additive noise. In both these cases, AM results in noise multiplication alongside PM noise. One may therefore conclude that the AM rejection of the SRD circuit is poor.

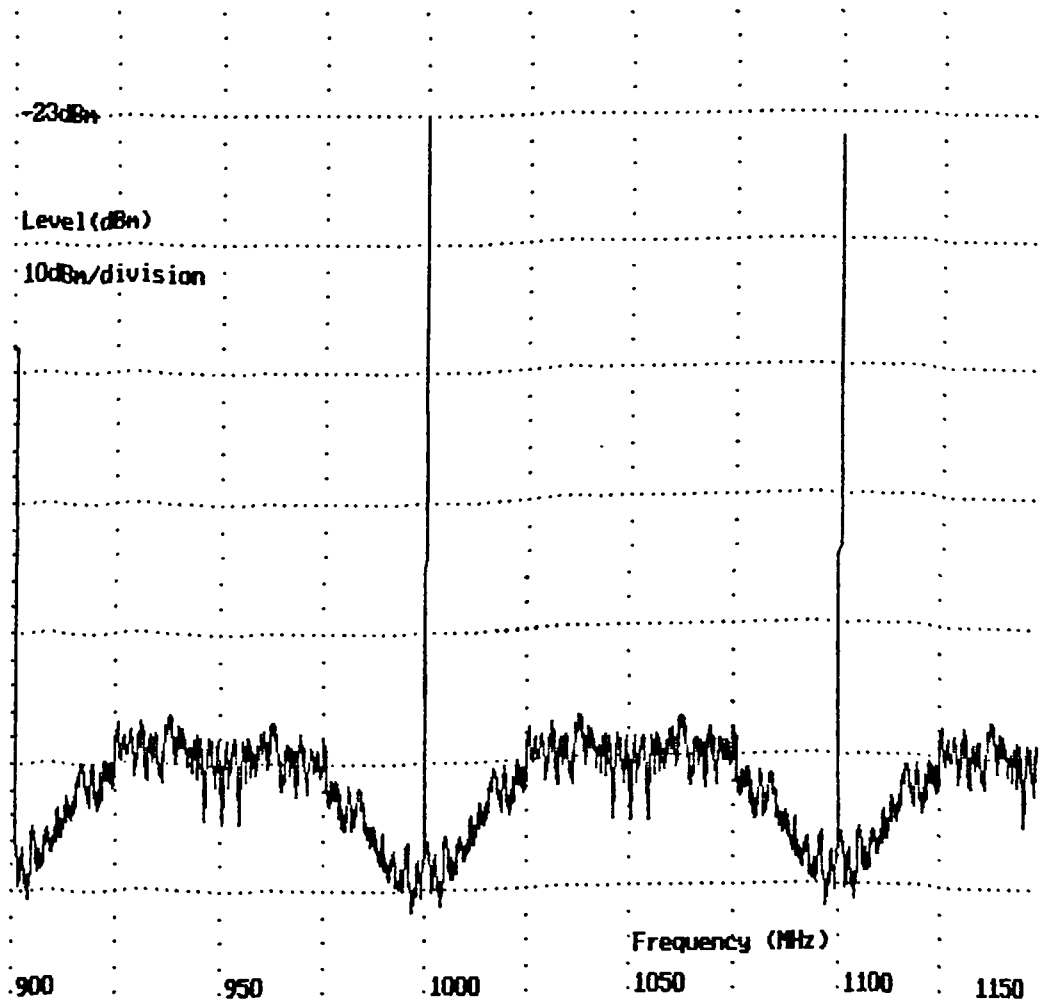


Fig 7.40 FFT Plot of comb generator output with 100Ω load, network 2, AM input noise.

7.10.4 Broadband additive noise

Broadband additive noise was input to the simulation of network 1 with a 100Ω load on the output. Noise degradation is now 30dB, that is 10dB above the multiplication factor. Included in this figure is the upconversion factor from low frequencies. Therefore the SRD is more sensitive to upconverted low frequency noise, than to noise at the input carrier frequency.

7.10.5 Effect of bias

The simulations so far studied deal with externally introduced noise to the SRD. Attention is now turned to the indigenous sources of phase noise. Baseband additive noise is used to simulate the effect of barrier voltage fluctuations. Degradation is measured by comparing the signal to noise at the output harmonic to that of the ratio of input signal to low frequency noise. Low frequency noise sensitivity is of particular interest as there is potential for $1/f$ noise to be introduced here as well as with the AM noise. Fig7.41 shows a plot of baseband upconversion against bias resistance for the simulation. As the bias voltage is increased, the circuit becomes less sensitive to baseband noise. This could suggest that adding bias could make the circuit less sensitive to barrier voltage variations.

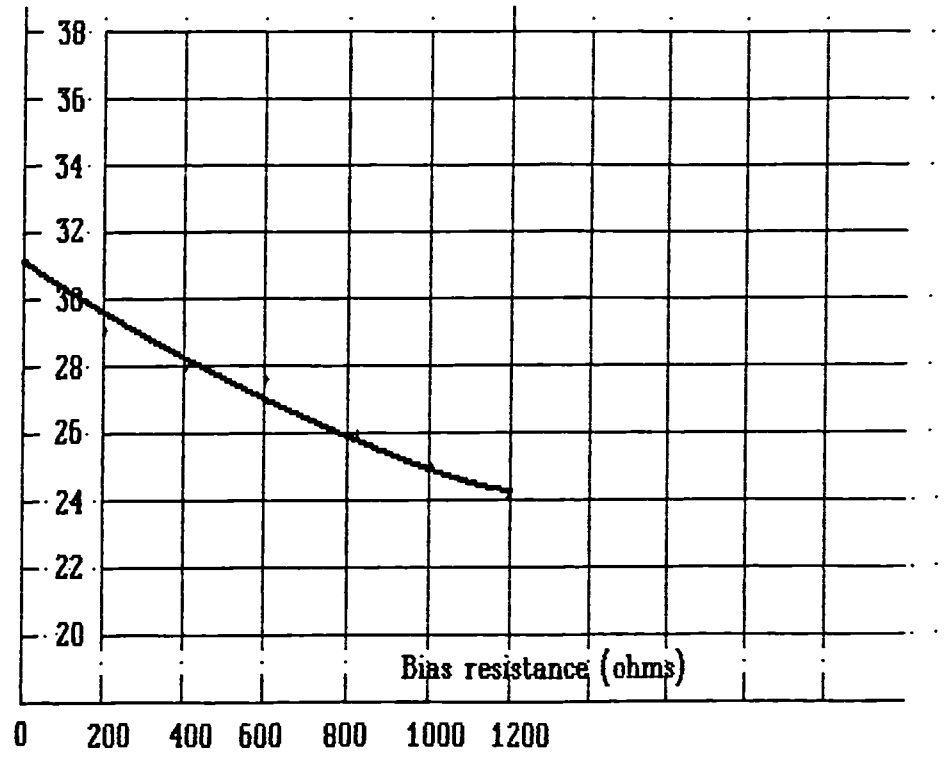


Fig 7.41 Relationship between bias resistance and upconverted baseband additive noise, simulated SRD comb generator

7.10.6 Effect of carrier lifetime fluctuations

Another indigenous mechanism for $1/f$ noise is carrier lifetime fluctuations. By varying the lifetime of the carrier and observing the change in firing angle, the effect of carrier lifetime upon phase noise can be estimated. A conversion factor is determined for carrier lifetime fluctuations to phase noise by applying a step change to the carrier lifetime and observing the change in α as described in §7.4.1. The lifetime change would need to be determined from either measurement or noise theory. For ease of comparison a constant phase noise level of -115 dBc/Hz was assumed at 1 Hz from carrier [Muat, 1986]. Fig 7.42 displays a plot of reciprocal carrier lifetime against phase noise, other parameters remaining constant, with and without self bias. As the lifetime is varied, the DC current used for self bias varies. Therefore the value of bias resistor is changed to keep a constant bias level of 1 volt. The results are intended to apply at 1 Hz from carrier. These figures can be applied to other offset frequencies by applying a factor $-10\log_{10}(f)$.

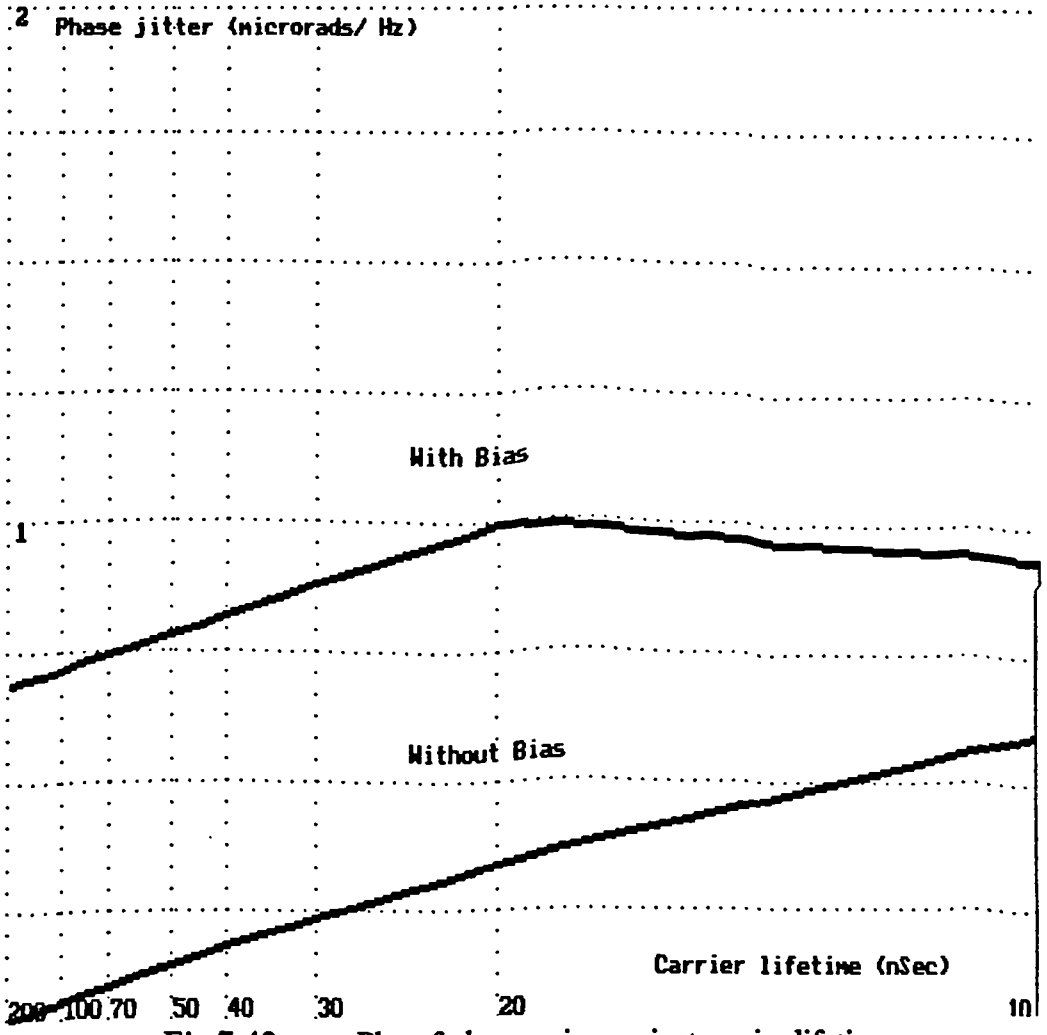


Fig 7.42 Plot of phase noise against carrier lifetime calculated for SRD comb generator drive frequency of 100 MHz

If no bias is used, the phase noise angle varies approximately according to the reciprocal of lifetime, as predicted from equation (7.12) above. If bias is used, the program indicates a higher level of phase noise, less dependent upon lifetime.

The effect of carrier lifetime variations agrees with that suggested by McDade [1966] in that phase noise increases with increased forward current. For best phase noise performance therefore, the reference frequency should be well above the reciprocal of the lifetime.

According to the computer simulation, when self bias is used, the fluctuations in carrier lifetime result in fluctuations in bias voltage which exacerbate the phase noise degradation. Long carrier lifetime devices, which would otherwise result in low phase noise if no bias was used, show a particularly marked increase in phase noise. This is in contradiction with the sensitivity to forward bias voltage variations. More information is required to determine the optimum operation point by consideration of the trade off between the relative levels of carrier recombination noise and noise due to forward barrier fluctuations. $1/f$ noise noise levels could in particular be determined by the above discussed effects. McDade [*ibid*] and others observed more noise when significant rectification current was flowing. The implication from this is that the dominant mechanism for noise introduction is carrier recombination, rather than baseband forward voltage fluctuations of the junction barrier voltage which would occur independently of rectification.

In order to optimise the noise performance it would be necessary to minimise the effect of recombination noise, barrier fluctuation effects, AM to PM conversion, and then take an FFT of the spectrum in order to evaluate subharmonic effects.

7.11 Measured results

7.11.1 Published results for SRD multiplier phase noise

It is instructive to compare some available results for phase noise performance of comb generators, multipliers and phase locked oscillators. These are shown in fig7.43. Manufactured phase locked oscillators have much higher phase noise than the comb generator optimised for low phase noise. The $1/f$ intercept point of the 500MHz comb generator at f_{in} is -131 dBc/Hz [Scherer, 1981]. If a value can be assigned to the lifetime variations, then it should be possible to predict the phase noise for any SRD comb generator.

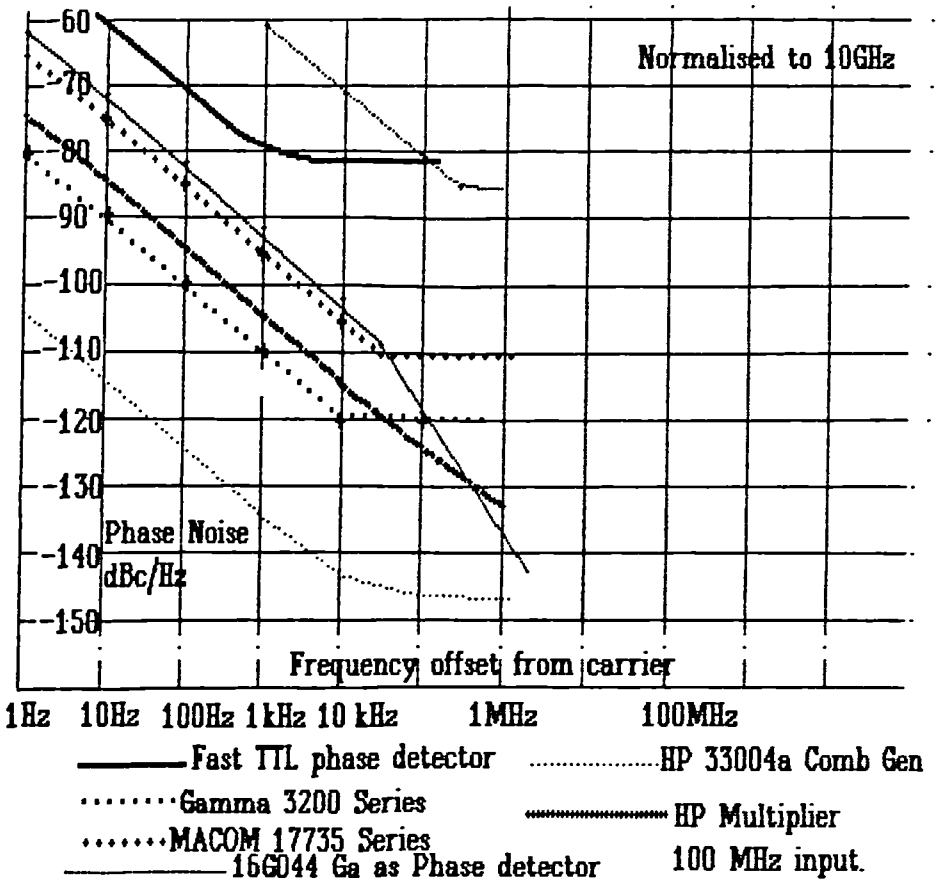


Fig 7.43 Published phase noise figures of comb generators,multipliers, and phase locked oscillators

7.11.2 Stability of SRD comb generator, measurements

In order to verify the simulated results, comb generators were built and measured. In the time domain, measurements were taken with a Digitizing Sampling Oscilloscope (DSO). type HP54121T (Hewlett-Packard). Fig 7.44 displays the circuit used for the measurement of SRD performance in the simplest configuration which was driven by a Marconi 2022 signal generator followed by a ENI 603L 3 W amplifier and output filter to reduce the harmonic content to below 50 dB. 3 dB pads are used to reduce the effect of undefined impedances. Drive inductance is formed from the secondary of the matching transformer. A small capacitor is used as a potential divider at the output to couple signals to the HP 8566B spectrum analyser. Diodes D1 and D2 are for the sampling phase detector. The RF input is unused in this measurement. The digital sampling oscilloscope (DSO) is connected directly across one side of the SRD.

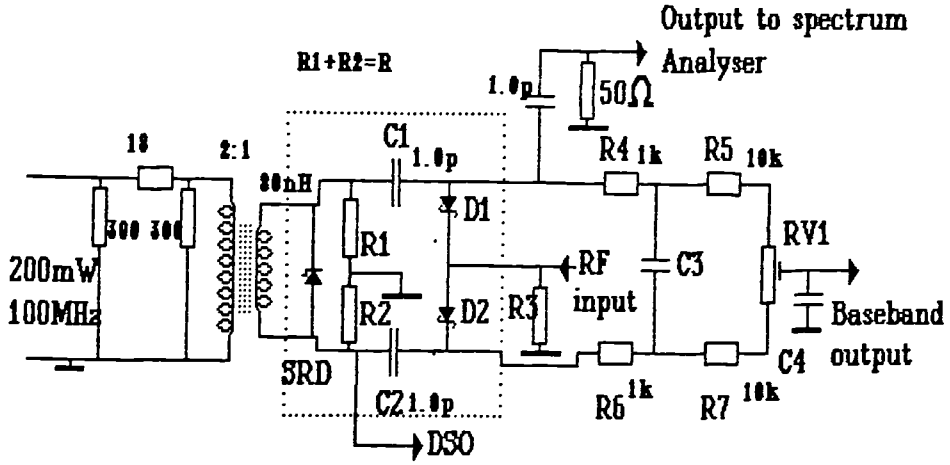


Fig 7.44 Simplest SRD comb generator circuit built for measurements

Measurements for a circuit corresponding to network 2, §7.5.1 were obtained from the specially built sampling phase detector circuit of fig7.45. Fig7.46 displays a method of adding broadband noise. In addition to the matching transformer, there are two impulse inductors L_d and the reflection capacitor added. The advantage of this circuit is that it allows a broader bandwidth on the input but stills maintains narrow pulse widths at the output.

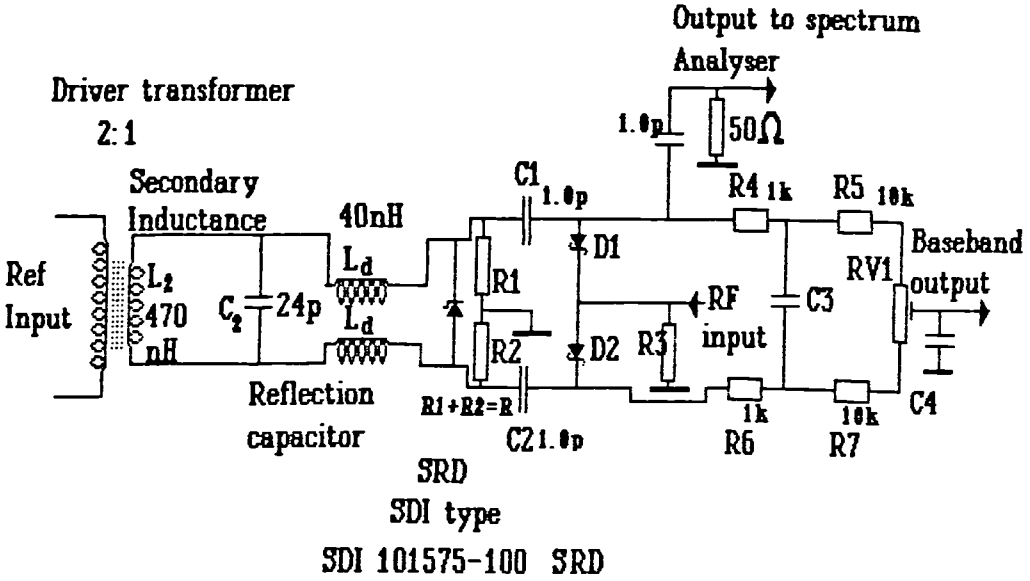


Fig 7.45 Circuit with matching transformer and reflection capacitor built for measurements

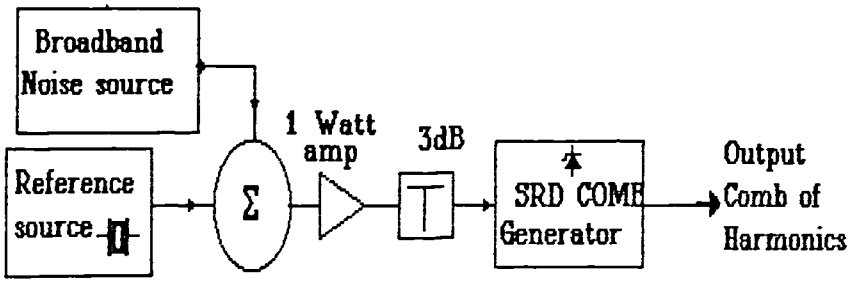


Fig 7.46 Adding broadband noise to investigate peaking effects

Fig 7.47 and 7.48 displays the results of DSO plots for values of load resistance of 100Ω and 500Ω respectively. The 500Ω plot shows clearly the effect of carrier storage period doubling.

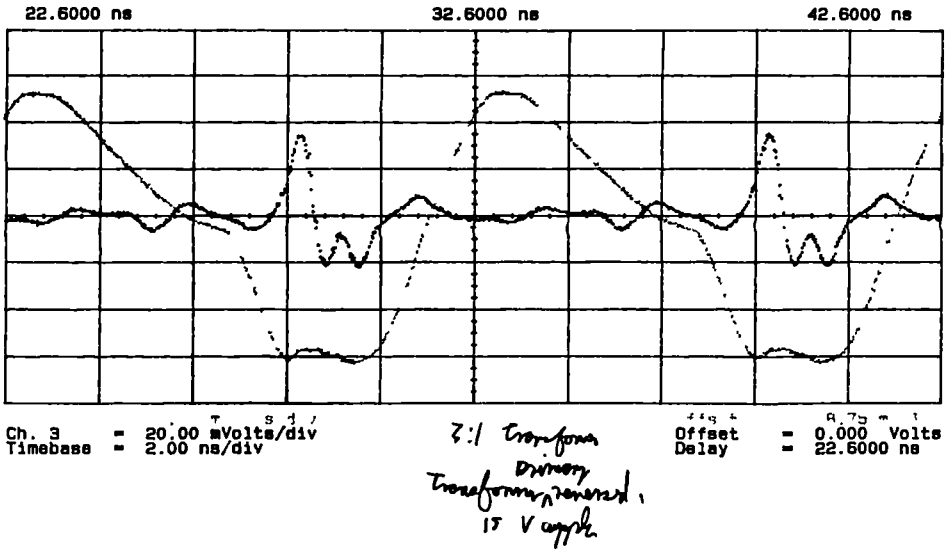


Fig 7.47 Digital storage oscilloscope (DSO) plot of SRD comb generator with 100Ω load

Frequency domain plots were made with a Hewlett-Packard HP8566B spectrum analyser.

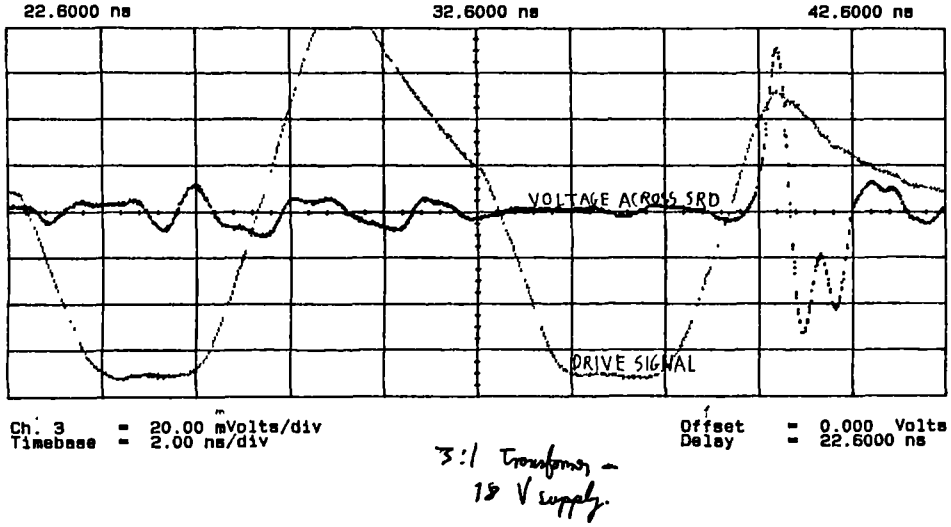


Fig 7.48 Digital storage oscilloscope (DSO) plot of SRD comb generator with 500Ω load

The drive frequency is in this case 88 MHz, but similar effects were obtained to that at 100 MHz. Fig 7.49 displays the frequency domain plot with a 130Ω load.

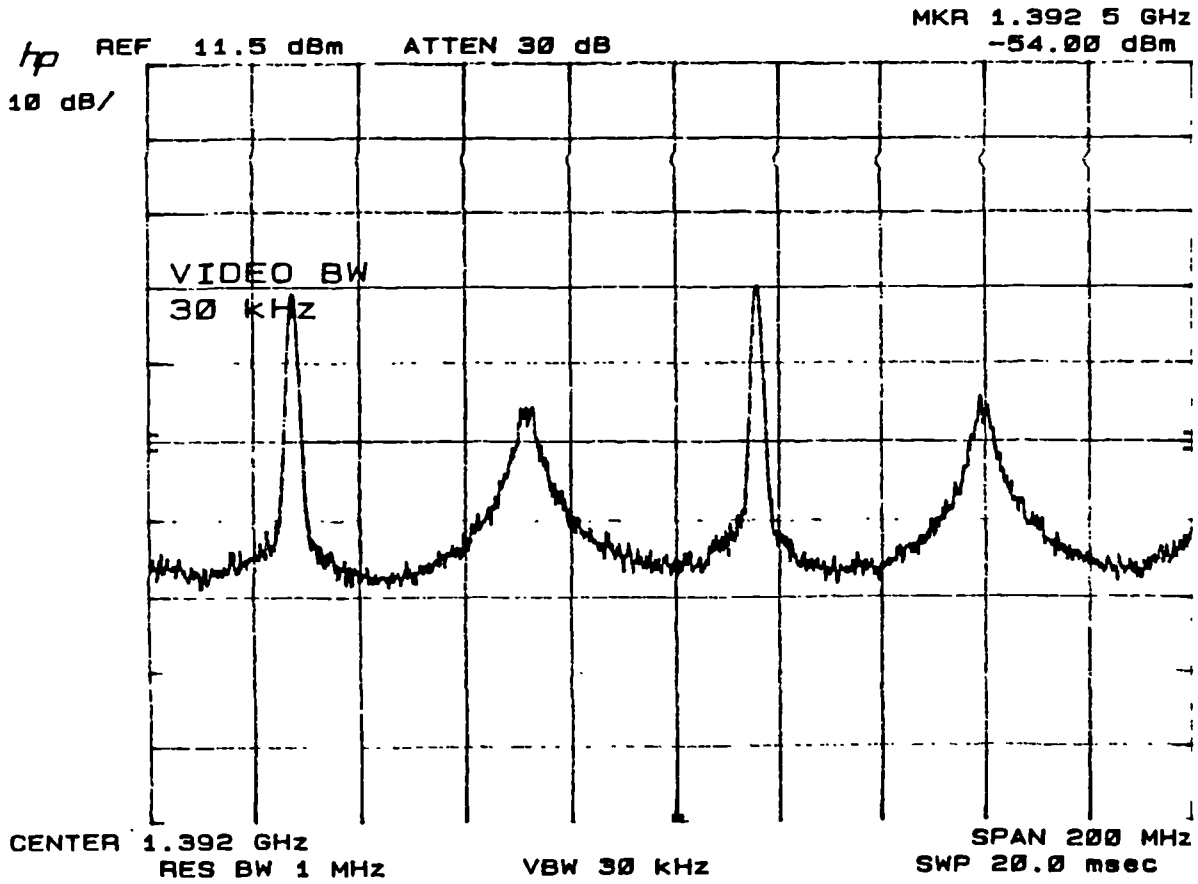


Fig 7.49 Spectrum analyser plot of SRD comb generator showing half carrier noise peaks

Noise peaks at half carrier offset frequencies can be noticed. An increase in noise level is also displayed around the carrier harmonics. Increasing the load resistance to 150Ω results in the drastic degradation of signal to noise ratio as can be observed from fig7.50. The effect of the bifurcation point on the phase noise can be clearly observed.

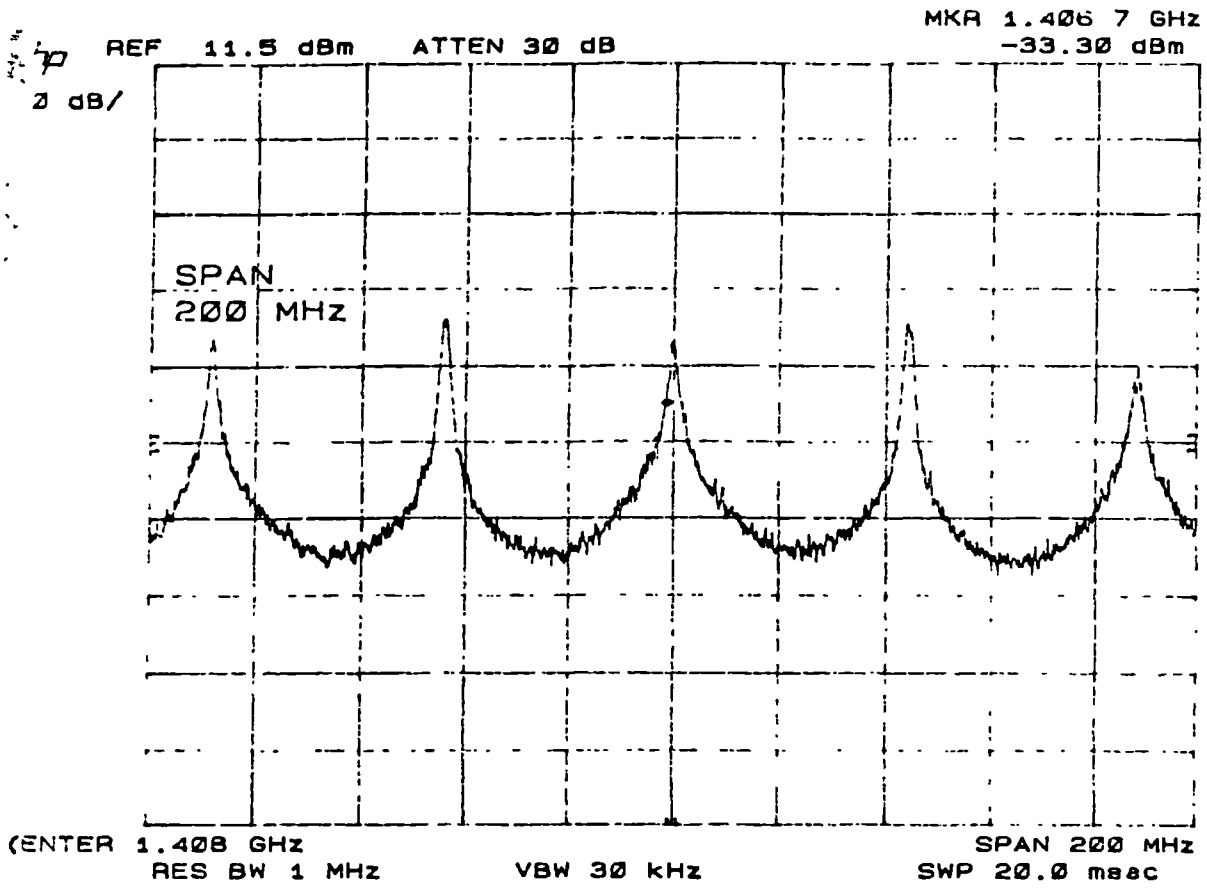


Fig 7.50 Spectrum analyser plot of SRD comb generator showing bifurcation point

Increasing the value of the load resistance to 400Ω gives stable frequency halving. Fig 7.51 shows this frequency halving effect. It can be observed that the noise sidebands have increased.

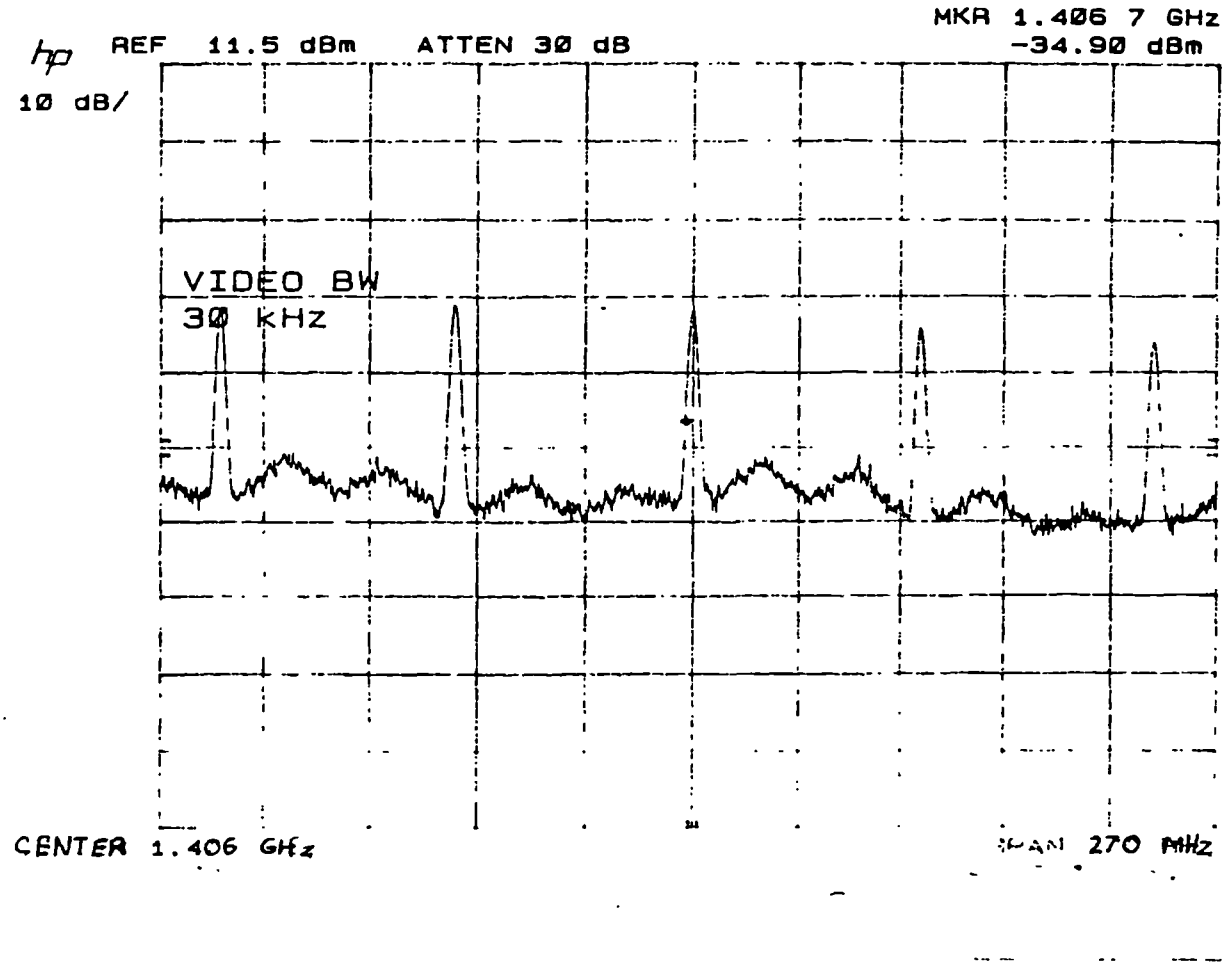


Fig 7.51 Spectrum analyser plot of SRD comb generator with 400 Ω load showing carrier storage division.

A broadband plot displaying carrier storage division by having a load resistance value of 400 Ω can be observed in fig7.52.

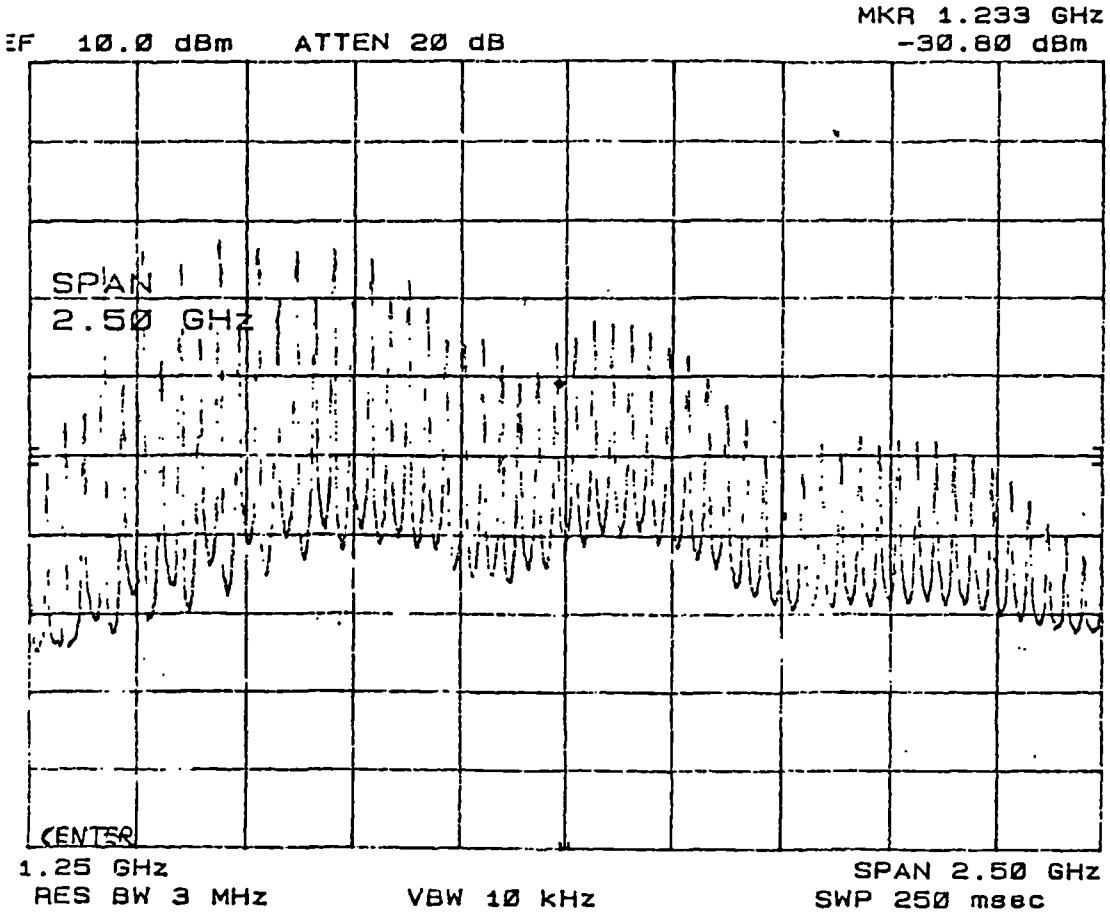


Fig 7.52 Spectrum analyser plot of SRD comb generator showing broadband output of network 1 with frequency halving.

A broadband plot of the SRD generator built with network 2 and a 100Ω load resistor is given in fig7.53. Stable comb generation at the input frequency can be observed. A reduced frequency range span can be seen in fig7.54. Increasing levels of noise sidebands as the offset from carrier frequency increases can be observed as predicted with the simulation result of fig7.29.

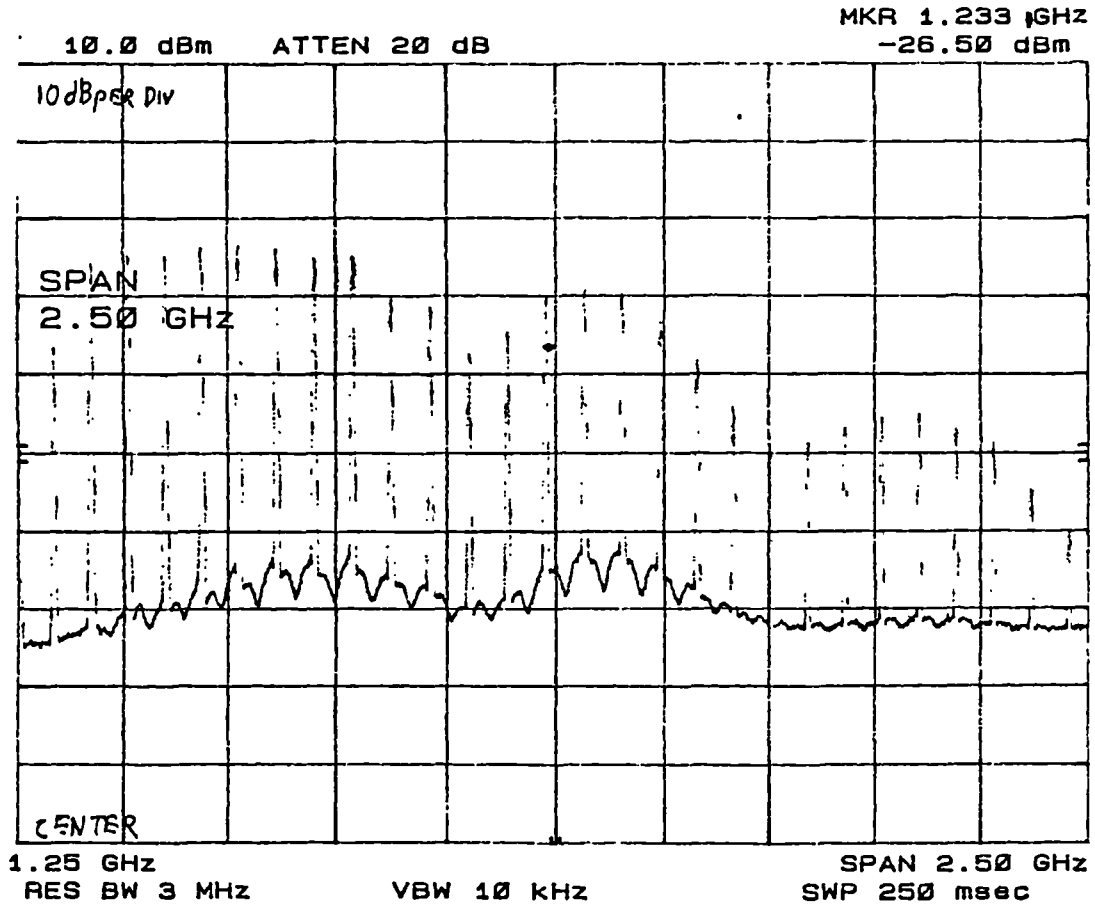


Fig 7.53 Spectrum analyser plot of SRD comb generator showing broadband output of network 2 with 100Ω load

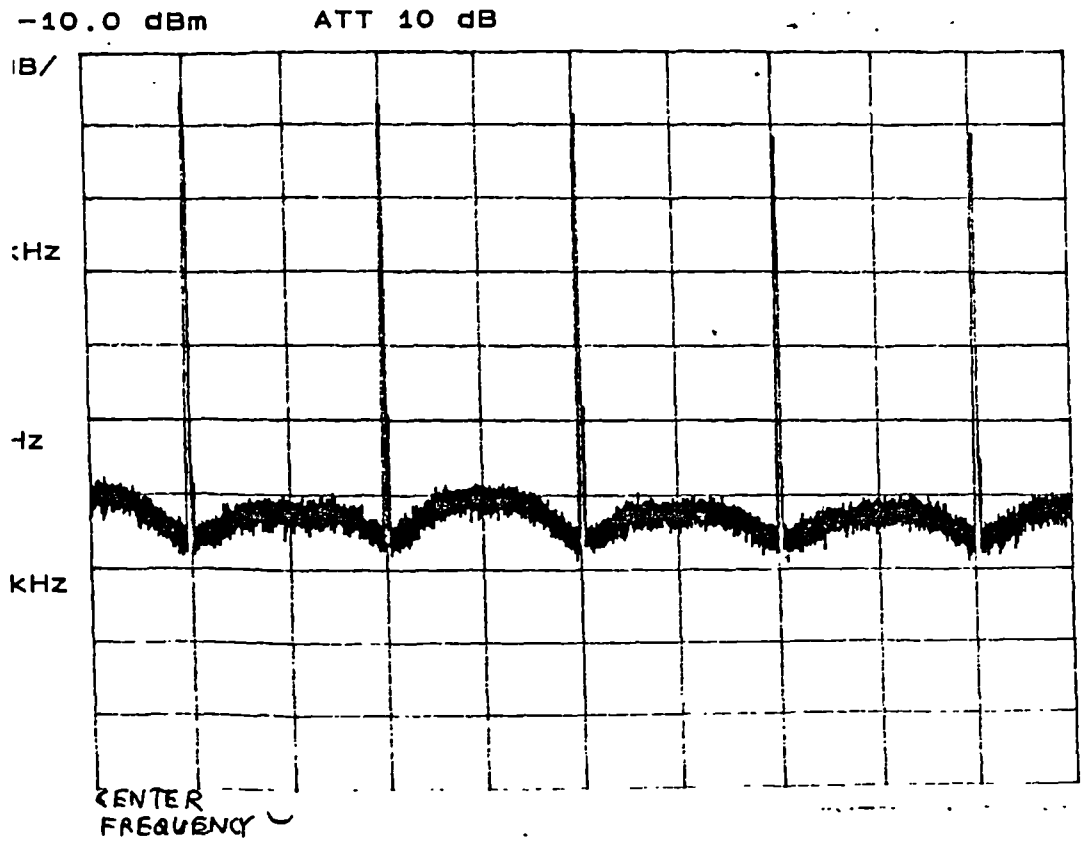


Fig 7.54 Spectrum analyser plot of broadband output of network 2 with 100Ω load, reduced frequency span

7.11.3 Measurements of phase noise of SRD comb generators

The author has measured the phase noise performance of a comb generator driven from a crystal oscillator. Two crystal oscillator circuits are measured, both derivatives of the Colpitts circuit. Collector output is used for the circuit of fig7.55 and also another output is taken directly from the resonator circuit as suggested by Rohde [1983c]. Fig7.56 displays the measurement circuit. An output from a 3GHz cavity oscillator is connected to the microwave input of a sampling phase detector driven from a comb generator. Downconverted output from the phase detector is fed through a gain compensated amplifier to ensure gain flatness across the band. It is important that the level fed into the phase detector is maintained at such a level that the phase detector is not driven out of its linear operating region. Confirmation of linearity is obtained by plotting output voltage against input. Drive level is maintained 10dB below the 1dB compression point. The noise spectrum is plotted on a low frequency spectrum analyser.

The resulting plot is displayed in fig7.57 for the two sources. By taking the output from the collector of the Colpitts oscillator transistor, a higher output noise level results. Peaking in the noise floor occurs as predicted by the simulation. It can be observed that

the different methods of driving the comb generator give noise peaking at different offset from carrier frequencies. However, this may be explained by the different drive levels and drive waveforms in each case. Using the sampling phase detector for downconversion is prone to errors introduced by simultaneous downconversion from the image frequency. For this reason noise measurements were taken at a frequency of 30 MHz, giving an error of 3dB at the lowest noise point measured.

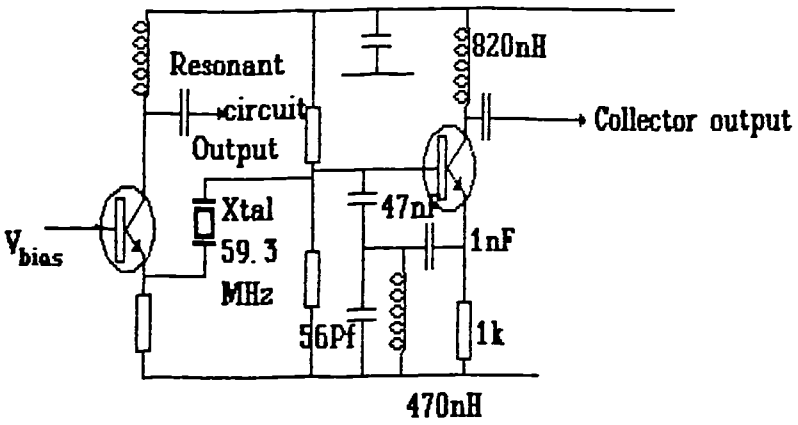


Fig 7.55 Crystal Oscillator circuit used for Step Recovery Comb Generator Measurements

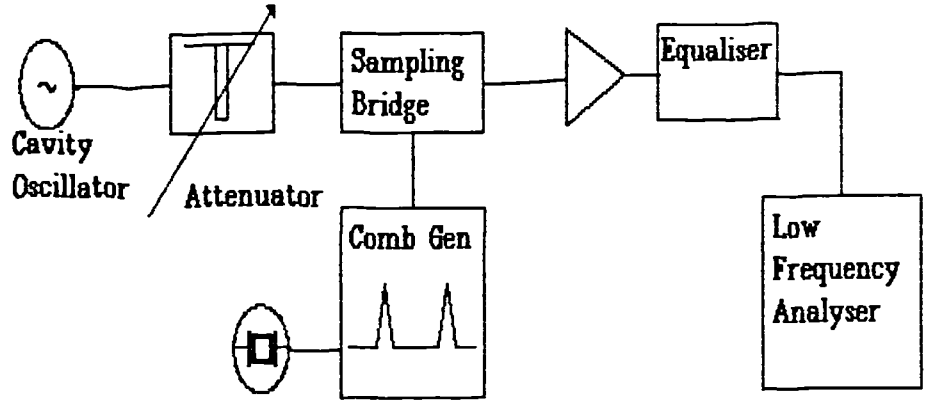


Fig 7.56 Equipment used to measure phase noise of Xtal oscillator, comb generator combination

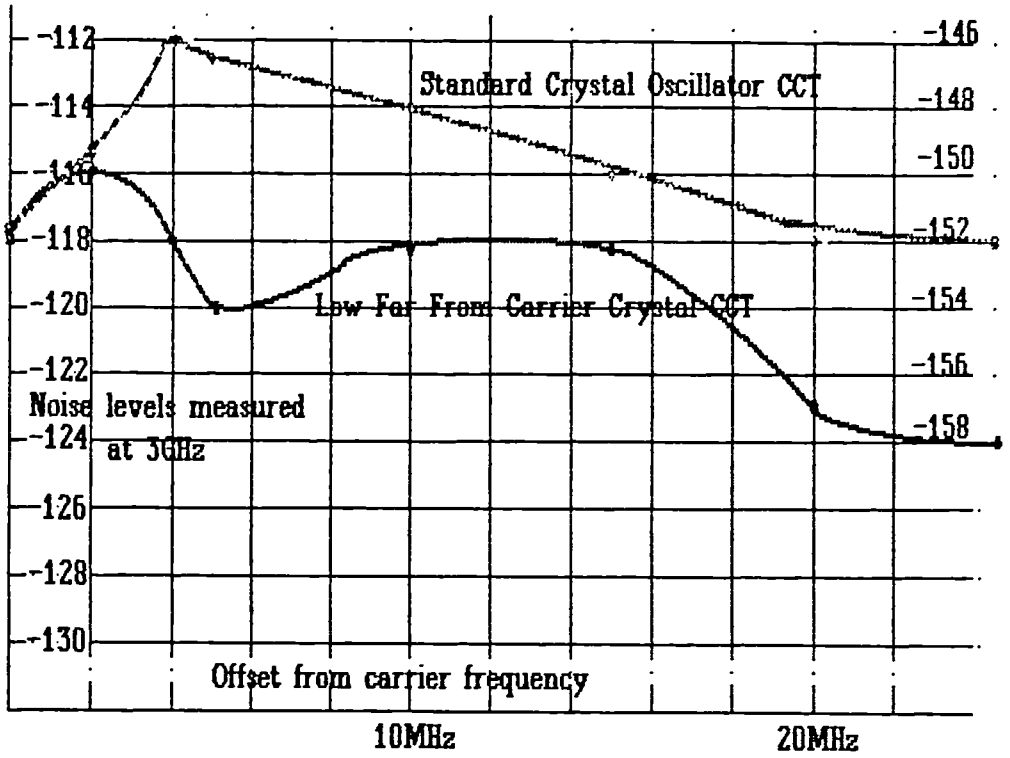


Fig 7.57 Measured phase noise values for the step recovery diode comb generator/ sampler for a 3GHz Rf signal and a 59MHz reference source

7.12 Summary and conclusions

Chapter 7 described a SRD comb generator simulator that could be used to guarantee low phase noise performance when SRDs are used for frequency multiplication.

Chapter 7 has investigated a number of key factors that must be considered in the design of SRD based comb generators. A simulation program for SRDs has been written that demonstrated important effects that can occur in the actual circuits. Time domain simulation was initially carried out, followed by a conversion to the frequency domain by FFT. This simulation has enabled the study of subharmonic phenomena and phase noise performance of such circuits. Both these topics are not very well covered in published works. The subharmonic effects were compared with the work of Feigenbaum which suggest similarities with classic period doubling chaotic effects. Modifications to the simulation program enabled the production of both a recursion diagram and a bifurcation diagram. A recursion diagram demonstrated the fact that it is possible for a comb generator, which may appear to be stable, to suddenly degenerate into period doubling chaos. The bifurcation diagram demonstrates the possible operating modes that the circuit is capable of. Both diagrams demonstrated how the phase noise can be severely degraded

by such effects. Also shown was the fact that two forms of chaotic behaviour can be supported by the SRD circuit: period doubling chaos, and a close to carrier form of chaos. The simulation showed that the use of higher Q circuits in the SRD impulse generator increased the likelihood of chaotic behaviour, and that more problems were likely to be experienced with multipliers than comb generators.

The simulation was used to study excess noise effects that increase the multiplier phase noise degradation effects above the theoretical $20\log N$. In some cases, especially as a result of subharmonic effects, the excess noise can be severe and could seriously degrade the far from carrier spurious and phase noise performance of local oscillators. In general, it was shown that the phase noise sidebands of the multiplied SRD signal increase as the offset from carrier frequency increases. This could result in increased phase noise if the comb generator is used as a harmonic mixer. If the downconverted signal is phase locked at the lower frequency, the signal to noise ratio will reduce as a result of the subharmonic effects between the harmonics. For optimum noise performance it is preferable for the phase locking to occur at zero offset frequency at the SRD phase detector.

For the optimum phase noise performance, simulation and theory indicate that a long lifetime diode and zero bias are desirable. As the reference input frequency decreased, $1/f$ and white recombination noise becomes greater in level. For this reason, SRD comb generators give better performance with a reference frequency much greater than the reciprocal of the lifetime. This corresponds to coarse frequency steps in a synthesiser. Indications are that the phase noise levels will be high if the SRD is used in a fine stepping synthesiser with a low reference frequency. If a fine stepping synthesiser is required, the SRD loop would have to be combined with a DDS as described in the next section. In chapter 4 a synthesiser configuration that enables fine stepping while driving the SRD at a high reference frequency is described.

The investigation into AM noise suggests that this is increased by the $20\log N$ factor by AM to PM conversion, and the AM rejection of such a comb generator is poor. Therefore as much AM noise as possible should be removed before the SRD harmonic generator circuit.

7.13 Further work on SRD comb generators

The SRD simulation program could be developed further by the addition of a user friendly interface with the aim of providing a useful design tool for engineers.

To enable accurate phase noise levels to be predicted in SRD comb generators, a value must be determined for the statistical fluctuations of the carrier lifetime. This may either be measured, or calculated from semiconductor theory.

The effect on stability margins of different drive waveforms could be investigated other than the sinewave input used in chapter 7. §7.9.4 raised the possibility of controlling the shape of the recurrence relationship by means of the waveshape; there may be an optimum waveshape which may be provided by the driver circuit. Another effect worth investigating would be the effect of drive amplitude upon AM to PM conversion to minimise the introduction of phase noise from this source.

In the simulation described in this chapter, no account was taken of device parasitics such as lead inductance. Although the simulation equations could be easily altered to achieve this, Gear integration methods may be desirable for accurate results. A recommendation for further work would be to implement such modifications.

In this chapter, it was demonstrated how a recurrence relationship could be plotted for a single resonant circuit. If more than one resonant circuit exists, as for example in network 2 of §7.5.1 then more work will be required to produce a multidimensional recurrence plot.

7.14 References

Badger, D 1988 Improved Accuracy for Transient Analysis *Rf expo. proceedings.* pp. 147-156.

Becker, K. & Dorfler, M. 1990 *Dynamical systems and Fractals,* chap. 2, p. 40. Cambridge University Press.

Bernard, M.Y. & Neau, J.C. 1990 A Surprising Phenomenon: the Chaos. *European Microwave conference.*

Berry, R.D. January 1971 An optimal ordering of electronic circuit equations for a sparse matrix solution. *IEEE transansactions on Circuit Theory.* Vol CT-18, No. 1, p. 40-50.

Boff, A.F., Moll, J. & Shen, R. 1960 A new high speed effect in solid state diodes. *International Solid State Circuit Conference Digest of technical papers.*

Buckingham, M.J. 1983 *Noise in Electronic Devices and Systems,* chap. 5, p. 128. NY: Wiley.

Calahan, D January 1971 Numerical considerations for implementaion of a nonlinear transient circuit analysis program. *IEEE transansactions on Circuit Theory.* Vol CT-18, No. 1, p. 66.

Calahan, D.A. 1972 *Computer Aided Network Design,* NewYork : McGraw-Hill.

Dalquist ,G. & Bjorck,A. 1974b ibid. chap. 8, p. 378.

Dalquist ,G. & Bjorck,A. 1974c ibid. chap. 5, p. 165.

Dalquist, G. & Bjorck, A. 1974a *Numerical Methods,* chap. 8, p. 339. Englewood Cliffs, N.J.: Prentice-Hall.

Dalquist, G. & Bjorck, A. 1974d ibid. chap. 6, p. 222.

Egan, W. 1981 *Frequency Synthesis by Phase Lock,* chap. 4, p. 72. Wiley

Fairley, D.O. 1968 Noise considerations for solid state microwave sources in high capacity FM radio systems. Telecommunications, April 1968 pp11-16

Feigenbaum, M.J. 1978 Quantitive universality for a class of nonlinear transformations. *Journal of Statistical Physics.* Vol. 19, No. 1., pp. 25-52.

Friis, H.T. July 1967 Analysis of harmonic generator circuits for step recovery diodes. *Proceedings of the IEEE.* Vol. 15, no. 7, p1192.

Gear, C.W. January 1971a Simultaneous numerical solution of differential-algebraic equations. *IEEE transansactions on Circuit Theory.* Vol. CT-18, No. 1, p. 90-95.

Gear, C.W. 1971b *Numerical initial value problems in ordinary differential equations.* Englewood Cliffs, chap 11 p216 N.J.: Prentice-Hall.

Goto, E. August 1959 The Parametron, A digital computing element which utilises parametric oscillations. *Proceedings of IRE.* Vol. 47, No 8, p. 1304-1316.

Grebenkemper, J. 1982 Tutorial on phase noise. *Watkins Johnson application note.* p. 5.

Grove, A.S. 1967 *Physics and Technology of Semiconductor Devices,* chap. 5, p. 121. NY: Wiley.

Hachtel, G.D., Brayton, R.K. & Gustavson, F.G. Jan 1971 The sparse tableau approach to network analysis and design. *IEEE Trans Circuit Theory.* Vol CT-18, pp. 101-112.

Hamilton, S. & Hall, R. 1967a Shunt mode generation using step recovery diodes. *Hewlett Packard technical note.* p. 65.

Hamilton, S. & Hall, R. 1967b Shunt mode Harmonic generation using Step Recovery Diodes. *Hewlett Packard technical note .* p. 70.

Hewlett Packard 1967 *Hewlett Packard application note AN416*, Palo Alto.

Hewlett-Packard 1969 Harmonic generation using step recovery diodes. *Hewlett Packard application note* 920. Various authors

Krakauer, M. July 1962 Harmonic generation, rectification, and lifetime evaluation with the step recovery diode. *Proceedings of the IRE .* p. 1666.

Kroupa, V. 1973a *Frequency synthesis, theory design and applications.* chap. 2, p. 52. NY: Wiley.

Kuo, F. 1966 *Network Analysis and Synthesis.* chap. 5, p. 120. Wiley.

Kwitkowski, P.A. 1989 RF power amplifier instability - causes and cures. *RF Expo Proceedings.* pp. 1-12.

Lauwerier, H. 1986a One dimensional iterative maps. In *Chaos.* (ed. Holden), Chap. 3. p. 41 W. Manchester University Press.

Lauwerier, H. 1986b Two dimensional iterative maps. In *Chaos.* (ed. Holden), Chap. 4. p. 75 W. Manchester University Press.

Lean, G.D. Sept 1978 Versatile microwave source. *Wireless world,* p. 56.

Luettgenau, G.G 1973 Some notes on broadband solid state power amplifiers. *Communications products application bulletin, MCP Electronics* P21

Manassewitsch, V. 1985a. *Frequency synthesisers, theory and design,* chap. 2, p. 119. NY: Wiley.

Manassewitsch, V. 1985b *Frequency synthesisers, theory and design,* chap. 6, p. 369. NY: Wiley.

Manassewitsch, V. 1985c *Frequency synthesisers, theory and design,* chap. 2, p. 122. NY: Wiley.

Manley, J.M. & Rowe, H.E. July, 1956 Some general properties of non linear elements Part 1 general energy relationships. *Proceedings of IRE.* Vol. 44, pp. 904-613.

McDade, J.C. Feb 1966 Measurement of Additive Phase Noise Contributed by the Step Recovery Diode in a Frequency Multiplier. *Proceedings of the IEEE.* p. 292-294.

Meares, L.G & .Hymowitz, C.E. 1988 *Simulating with Spice,* chap. 3, p. 3-5. Intusoft Publications.

Muat, R. & Upham, A. 1986 Low noise oscillator design *Hewlett Packard RF and Microwave Measurement Symposium and Exibition,* London p. 24

Nagel, L. May 1975 Spice2: A computer program to simulate semiconductor circuits. *Electronics Research Laboratory Report. No. ERL-M520,* University of California, Berkeley.

Obregon, J. 1990 Non Linear Analysis and Design of Microwave Circuits. *European microwave Conference 1990, proceedings.* p. 1089-1094.

Pontius, B. 1967 "One step high order Frequency Multipliers," Hewlett Packard Application Note AN416

Prabhu, V.K. 1967 Stability considerations in lossless varactor frequency multipliers. *The Bell System Technical Journal,* Nov 1967 pp 2035-2059

Pritchard, R. 1985 *Microwave dividers.* Leeds University, PhD Thesis, UK. p. 64.

Rabiner, L. & Gold, B. 1975. Theory and application of digital signal processing, chap 5, p. 350 NJ: Prentice Hall.

Rohde, U. 1983 *Digital PLL frequency synthesisers ,* chap. 4, p. 204. N.J: Prentice Hall.

Ryan, W.D. & Williams, H. Sept. 1964 The carrier storage frequency divider, a steady state analysis. *IEE Transactions on Circuit Theory.* pp. 396-403.

Scherer, D. 1981a Generation of low phase noise microwave signals. *Hewlett Packard RF and Microwave symposium and exhibition notes.* p. 21.

Siemens AG 1987 *Microwave Diode Data.* Varactor section, p. 3. Munchen: Siemens AG.

Sobhy, M.I. *et al.* 1990 Chaotic Behavior of Microwave Circuits. *European Microwave Conference.* pp. 363-368.

Strang, G. 1980 *Linear Algebra and its Applications,* Appendix C, pp. 371-375. 2nd ed., London: Acedemic Press.

Stroud, K. 1990 *Further engineering mathematics,* chap. 6, p. 262. London: Macmillan.

Vidkjaer, J. October 1976 Instabilities in RF Power Amplifiers Caused by a Self Oscillation in the transistor bias network. *IEEE Journal of Solid State Circuits.* Vol SC11, No. 5. p. 703.

Watanabe, T. & Fakatsu, Y .Nov.-Dec. 1967 Characteristics of semiconductor noise generated in varactor frequency multipliers. *Review of the Electrical Communication Laboratory.* Vol. 15, Nos. 11-12, p. 760.

Watson, H.A. 1969 *Microwave Semiconductor Devices and Their Circuit Applications,* chap. 7, p. 189. NY: McGraw-Hill.

8 New Design Techniques for DDS

8.1 Introduction

The major problem with fine step size synthesisers is achieving low phase noise together with immunity to vibration and low levels of spurious signals. Direct digital synthesis (DDS) will provide low phase noise and immunity to vibration, but the spurious signal performance at present often leaves something to be desired. In this chapter a thorough investigation of the problem is undertaken. This leads to a possible solution for which a patent has been applied for. Most of the processing takes place in the digital domain which enables a high level of integration. Many spurious problems arise from the use of an imperfect digital to analogue converter (DAC), therefore this chapter will begin with a discussion of the use of DACs in DDS.

8.2 A Survey of DAC performance

8.2.1 DAC Architectures

There are several types of DAC in common usage [Merisse, 1988]. The principal types are the current weighted DAC, the segmented DAC, and the R-2R ladder DAC.

The current weighted DAC consists of a bank of switched current sources (See fig8.1.). This raises problems of glitches due to mismatches in the switching characteristics.

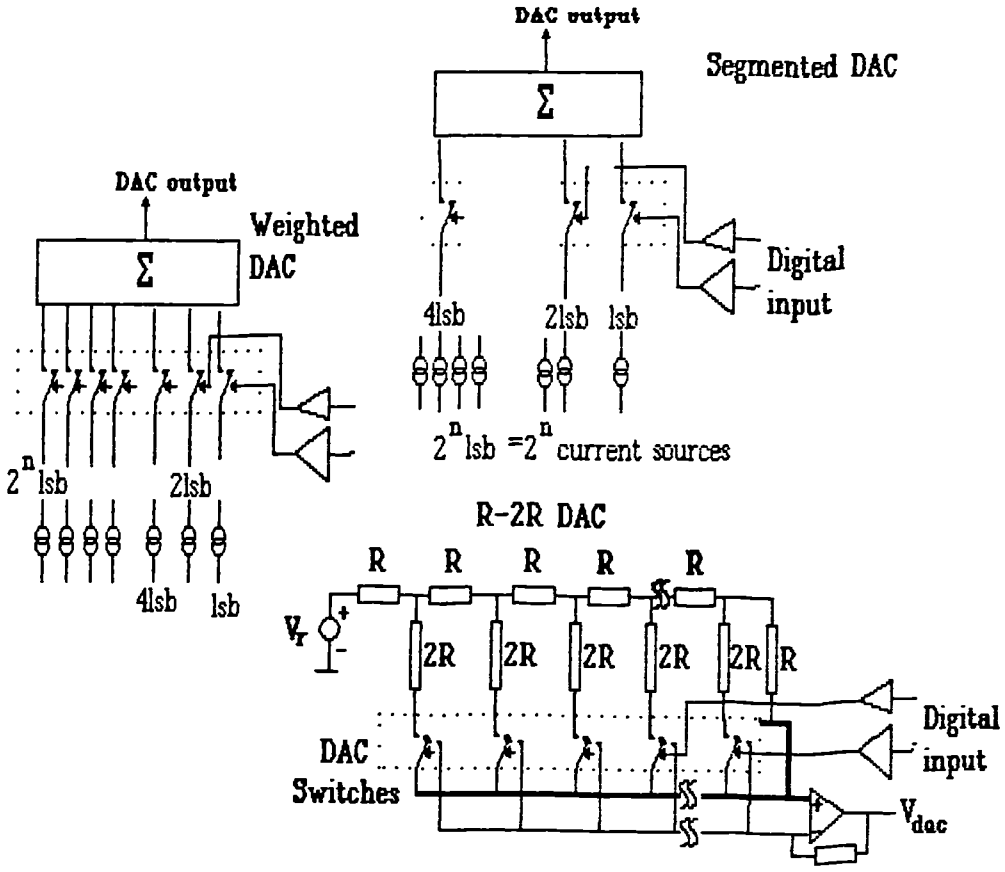


Fig 8.1 DAC Architectures

The current weighted DAC is potentially the fastest DAC.

The R-2R DAC is shown in fig 8.1c. The R-2R network effectively forms an attenuation ladder, whereby the current is halved at each stage. This network, although not as prone to glitches relies on expensive laser trimming of the resistors for accuracy.

A segmented DAC consists of a bank of matched equal current sources. The scaling is then formed by paralleling up current sources for increasing significance on the input bit, ie. the nth significant bit will have 2^n current sources connected to this. Clearly such a DAC can only have limited resolution due to the number of current sources required.

The latest generation of DACs have a Hybrid architecture [Jordan, 1991]. A Hybrid architecture consists of a segmented architecture for the most significant bits and a R-2R network for the least significant bits. Glitch performance is superior for the Hybrid types of DACs.

Each of the above mentioned types of DACs can be of either multiplying or non multiplying configuration. A multiplying DAC is a DAC which has a facility for

programming the input reference current. Since the current is used as a reference for the current sources, the output is effectively scaled by the input reference current. A non multiplying DAC will not have this current brought out to the external pins. By keeping the reference current internal, a reduction in complication of the circuitry and therefore distributive capacitance results in higher speed performance [Analog Devices, 1988].

8.2.2 Use of a DAC in Direct Digital Synthesis

The hub of a sinewave output direct digital synthesiser is the DAC. There are many different DAC architectures and it is necessary to evaluate specific parameters that are most relevant to direct digital synthesis. The most obvious factor is the DAC resolution, but other factors are just as important. These factors are:-

1) Update rate;

2) Glitch level;

3) Differential linearity;

4) Integral linearity;

5) Digital feedthrough;

6) Clock feedthrough;

7) Cost.

8.2.3 Update rate

This is determined by the settling time of the switches in the DAC. The settling time is usually quoted as the time required for the output to settle to within a stated range around the final steady state value (usually ±1/2 LSB). For synthesiser usage, the output is continuously updated, and so therefore this settling transient is a source of error at the output. This maximum update rate will put a ceiling on the clock frequency of the synthesiser. 8 bit non-multiplying DACs possess the maximum update rates [Weiss, 1989] while high precision 16 bit DACs have a slow update rate [Saul, 1991]. For synthesiser usage, the form of the settling transient is more important than its duration. A settling transient that is linear in relation to the steady state change is equivalent to low pass filtering the output. A non-linear transient, in addition to this, will generate unwanted spurious frequencies.

8.2.4 Glitch level

A glitch is a transient that is a result of skew in the switching of currents that compose the analogue output of the DAC [Jordan, 1991]. Since there is no linear relationship between this and the magnitude of the DAC transition, then intermodulation product problems will result. There is a difference between this and a linear transient which is the equivalent of the effect of a low pass filter on a perfect transition. The latter process will not introduce intermodulation products. The glitch problem is aggravated by any timing skew on the digital signals at the input to the DAC. A desirable feature is therefore the use of a clocked register on the same chip as the DAC. The use of high resolution DACs does not necessarily imply improved glitch performance as the effect appears to be related to the speed of the current switches.

8.2.5 Differential non-linearity (DNL)

Differential non-linearity is an additional source of high order products in a DDS. It is the deviation of a LSB step from $2^n/(n-1)$. This therefore introduces a limit on the resolution of the DAC. For this reason larger bit DACs have lower levels of differential non-linearity. Unlike the previous effects DNL is a static DAC parameter, therefore the primary harmonic spectrum (ie that before aliasing) will be independent of output frequency.

8.2.6 Integral Non-linearity (INL)

Integral non-linearity (INL) is the overall deviation of the DAC transfer characteristic from a straight line. Since this effect encompasses the full DAC transfer curve, low order intermodulation distortion products occur at the output of the DAC. INL determines the overall accuracy of the DAC [Daura, 1985]. Instrumentation DACs will therefore be optimised for lower integral non-linearity.

8.2.7 Clock feedthrough

In a practical DAC, with a clocked latch, there will always be feedthrough of the clocking frequency to the output [Kamoto, Akazawa & Shinagawa, 1988]. This, in itself, will not constitute a problem, as the clock frequency can be filtered out. However, if the level of feedthrough varies according to the state of the DAC switches, then an average error value could exist which is not linearly related to the output signal. Consequently, spurious products would be generated. Intermodulation effects with the clock frequency is a major problem with high speed devices [personal communication, Jordan 1991].

8.2.8 Digital feedthrough

One of the major problems with high speed DDS is the feedthrough of the digital signals at the DAC input. The digital signals have a similar effect on the output as data skew, introducing non linear effects, and therefore intermodulation products. Avoiding digital feedthrough is difficult in a practical system because of the effect of lead inductances and stray capacitances [Colotti, 1990]. The problem can be alleviated to some extent by the use of a clocked DAC. A similar effect to this occurs internally in the DAC when the flip-flops in the clocked latch at the digital input changes state. A spike is generated that can be transferred to the analogue side of the current switch circuitry [Kamoto et al, 1988].

8.2.9 Cost

The cost of a DAC depends on the technology employed and the application. The use of a DAC that will be employed in other popular applications such video graphics will incur lower costs than a dedicated DAC. Prices of high speed DACS could be reduced as demand for high speed DDS increases.

8.2.10 Comparison of available DACS

A survey was carried out into six DAC manufacturers' products in order to ascertain suitability for use in a DDS and the results are displayed in table 8.1.

Table 8.1 DACS suitable for DDS

	Resolution	non-linearity Diff	non-linearity Integral	glitch V.sec	Settling time	to level	Clocked register	Max Clock	Technology	approx cost $
Triquint TQ6112-m	8 BIT	0.2%		<25pV s	1ns	1%	Yes	1GHz	Ga As	250
Triquint TQ6111-m	8 BIT	0.2%			1ns		Yes	600MHz	Ga As	150
Plessey SP98608	8 BIT	0.2%	0.2%	20pV s	2.5ns	0.2%	Yes	450MHz	ECL	59
Plessey SP9770	10 BIT	0.05%	0.05%	90pV s	12ns	0.1%	no	50MHz	ECL	
Plessey MV95408	8 BIT	0.2%	0.2%	<100pV s	20ns	0.2%	yes	50MHz	CMOS	7
TRW TDC 1018-1	8 BIT	0.2%	0.2%	< 46pV s	10ns	0.2%	yes	200MHz	ECL	19
TRW TDC 1112	12 BIT	0.025%	0.025%	25pv s	30ns	0.025%	yes	50MHz	ECL	
ADL AD9703	8BIT	0.2%	0.2%	70pv s	4ns	0.1%	yes	300MHz	ECL	
ADL AD9768	8BIT	0.2%	0.2%	200pV s	5ns	0.2%	no	100MHz	ECL	28
ADL AD568	12BIT	0.05%	0.0375%	350pV s	35ns	0.025%	no		BIPOLOR	
Burr Brown DAC63	12BIT	0.012%	0.012%	61pV s	70ns	0.012%	no	30MHz	ECL	
Harris DAC16b	16BIT	0.003%	0.003%	ns	1000ns	0.0015%	no		TTL	

Non-linearity levels decrease with increasing resolution as would be expected. Technology and internal configuration determine glitch levels rather than resolution. Superior glitch performance can be obtained with low level logic such as ECL and GaAs and by using an internal clocked latch to eliminate data skew at the input terminals. This

implies that increasing the resolution of the DAC does not necessarily mean improved DDS performance at high clock speeds. Work is required to ascertain the effect of the different non-linearities upon the spectral purity of a DDS at different clock rates. Published figures generally show that as the Nyquist limit is approached when the DAC is clocked at its maximum rate, the spurious performance deteriorates.

Another factor that must be considered is the increased close to carrier phase noise of any GaAs switches used in the DAC due to the high $1/f$ phase noise of GaAs devices (see §3.2.2). Unfortunately there is no data available for the phase noise of a GaAs DAC.

The cost of DACs increases drastically above 500MHz at present.

8.2.11 Dynamic properties of DACs in DDS

Since a DDS is likely to be clocked at the maximum clocking frequency of the DAC, the DAC dynamic performance is the most important parameter to consider. The static parameters such as INL and DNL will remain constant with clocking frequencies, but the dynamic effects, particularly the glitch performance will degrade markedly. In adopting a strategy for improving DDS performance, the glitch problem must be of the foremost importance.

8.3 Improving The Performance of Direct Digital Synthesis

8.3.1 The problem of spurious signals with high speed DACs

Although the DDS technique has many desirable properties, the spurious content of the output is excessive for most satellite communications applications. To enable operation at high clock frequencies, it would be desirable to employ a 8 bit fixed reference DAC. Such DACs have achieved clock rates of over 2GHz [Saul, & Taylor, 1989]. From measurement and from published results, the maximum spurious level up to 1/3 clock frequency of a 8 bit DDS, with the DAC clocked at its maximum frequency appears to be around -45dB [Browne 1988], [Stanford Telecom, 1987]. To date there have been several attempts to improve the spurious performance of this technique.

8.3.2 Existing spurious reduction techniques

8.3.2.1 Use of a Zero Order Sample and Hold

A zero order sample and hold can be placed after the DAC to remove DAC non linear glitches as in fig8.2 [Burr Brown, 1988]. The sample hold device samples after the DAC has settled, thus removing the DAC transient energy.

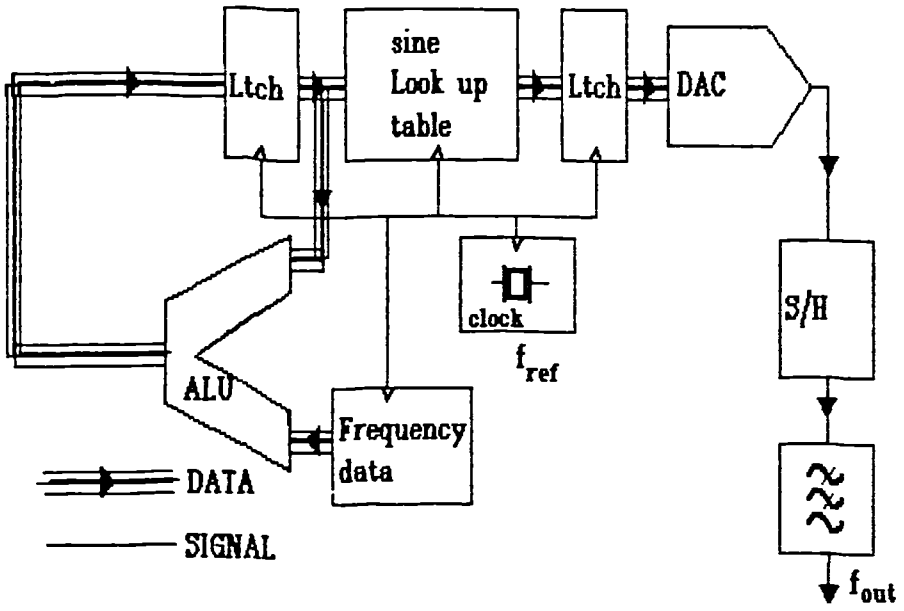


Fig 8.2 Direct Digital Synthesiser Block Diagram

8.3.2.2 Use of Dither to convert spurious signals to broadband noise

Wheatley [Wheatley & Phillips, 1981] suggested the removal of the DAC and the generation of square waves rather than sine waves. Dither is then applied to the phase accumulator to randomise the resulting square wave Fourier series and convert this to broadband noise. Thus the output spectrum consists of carrier plus noise rather than carrier plus square wave products.

8.3.2.3 Random switching between 2 DACs

A method has been developed [Fish, 1982] to reduce spurious products in the direct digital synthesiser by random switching between DACs. A direct digital synthesiser is modified as shown in fig8.3 by switching in a pseudo-random fashion between 2 DACS or between two function generators (with similar control of the DAC reference voltage), or between two function generator DAC pairs, or by randomly or pseudo-randomly varying the scaling voltage applied to a multiplying DAC.

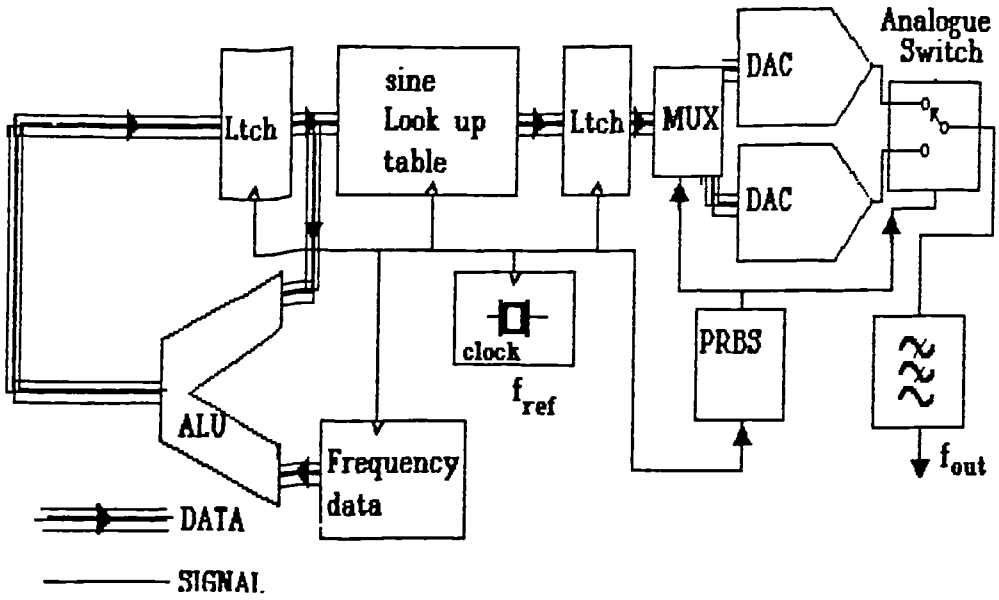


Fig 8.3 The Fish Synthesiser

8.3.2.4 Selection of output frequencies that avoid close to carrier Spurious

This involves the use of frequency outputs from the direct digital synthesis that have the spurious signals far removed from the carrier (see chapter 4) [Jones & Gardiner, 1987]. The far from carrier spurious signals can then be removed by means of bandpass filters or a phase locked loop. In order to ensure that the spurious signals do not appear close to the wanted carrier it is necessary to restrict the output frequencies to values that have a high common factor between output and reference frequencies.

8.3.3 Disadvantages of existing techniques

8.3.3.1 Post DAC Sample and Hold

The disadvantage of the use of the sample and hold deglitcher is as follows:-

1) The cost of a suitable high speed sample and hold that will not degrade performance due to intermodulation products is prohibitive;

2) The deglitcher can only reduce the spurious products associated with DAC switching. The remaining spurious products will be unaffected.

8.3.3.2 Squarewave synthesiser and dither

The elimination of the DAC in such a synthesiser, results in a low overall signal to noise ratio. The resulting phase noise sidebands of this system calculate to be approximately -72 dBc/Hz (-37 dBc in a 3 kHz bandwidth) [Wheatley & Phillips, 1981]. This figure is far in excess of that required by satellite data links [Eutelsat, 1989].

8.3.3.3 DAC Switching

Fish [1982] also suggests the use of a pseudo random sequence to randomise periodic errors in the direct digital synthesis process, but the method of application of the pseudo random sequence is in such a manner that there is little decorrelation of the DAC transfer characteristic. An averaging of the DAC transfer characteristics results. If the DACs are identical (ie if they are from the same batch), then little improvement would occur with this method.

A further development of the above approach [*ibid*] is the use of random scaling before the DAC and its subsequent removal by means of varying the reference voltage at the input to a multiplying DAC. One problem with this is that multiplying DACs, on account of their construction, are slower than fixed reference DACs [Analog Devices, 1988]. Another problem is that of scaling and rescaling the portion of the output cycle which is at a low level relative to the quantization. This means that either the randomisation at that point is limited, leading to repeating errors (and hence spurious output signals), or a large amount of noise being introduced.

8.3.3.4 Restriction of output frequencies

The problem with this technique is that the output frequency is restricted to values that give no close to carrier spurious frequencies, the nearest spurious signal frequency is arranged to be so that it is capable of being rejected by a phase locked loop at the output. The highest common factors in the fraction of the output frequency to the clock frequency ratio must be kept high so the phase accumulator output repeats itself over a short duration. While this is acceptable for radar applications where the number of channels is limited, in satellite systems where carrier tracking is required or in frequency hopped spread spectrum applications, channel spacing can be less than 1 Hz. This would require a PLL bandwidth of millihertz which would be totally unacceptable.

8.4. A novel Technique for the reduction of DDS spurious

8.4.1 Introduction

The following section describes a novel technique invented by the author which is producing encouraging results [Wilson, 1990]. The technique is based on the application of the pseudo-random numbers to achieve the following:-

1) Decorrelation of the DAC transfer characteristic;

2) Dither of the digital trigonometric word to reduce quantization effects.

8.4.2 The objective of DAC decorrelation

A typical DAC transfer function is displayed in fig 8.4

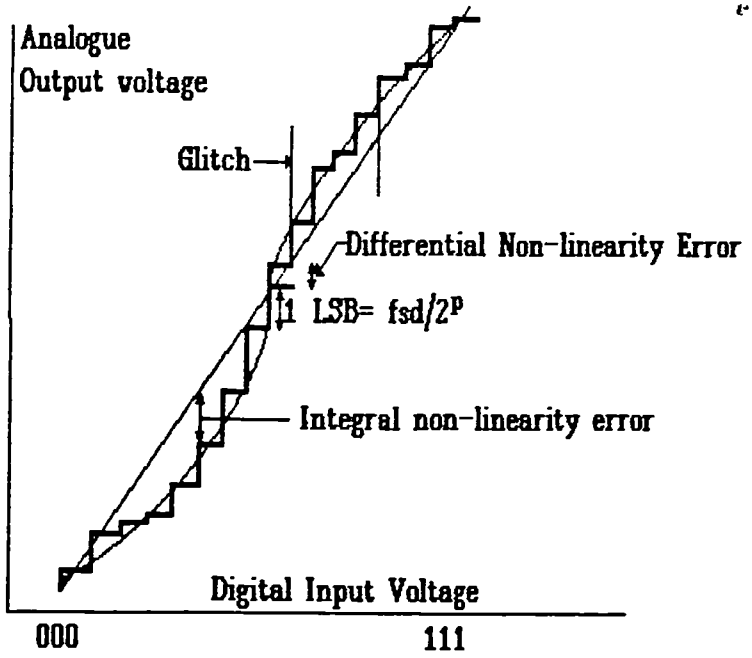


Fig 8.4 DAC Non-linearity errors

As described in chapter 4, apart from quantization, the main sources of errors are DAC polynomial linearity errors and switching transients.

8.4.2.1 Polynomial errors

The output of a practical DAC will consist of the following:-

$$V_{out}=V_{ref}((Q/(2T-1))Ep(Q) \qquad (8.1)$$

where V_{ref} is the DAC reference voltage, Q the digital input word, T the full scale digital world, and Ep(Q) a polynomial which represents non-linearity errors of the DAC. When a sinewave is acted upon by a polynomial function, each term in the polynomial raises the sinewave to the corresponding power of that term. It can be shown that each ($\sin^n x$) term produces a series of (sin mx) terms up to $m = n$ [Bromich, 1908] where m and n are integers. Therefore, polynomial errors result in the sampled waveform consisting of a sinewave plus harmonics of order m. These harmonics are aliased by the sampling frequency f_{ref} to produce spurious signals [Wheatley, & Phillips, 1981]. This polynomial is independent of f_{ref} and represents the integral non-linearity (INL), and differential non-linearity (DNL). The effect of these errors is displayed in fig 8.4.

8.4.2.2 Switching errors

Owing to the fact that not all the DAC current sources switch simultaneously, transients are introduced which are unrelated to the analogue level transitions [Harris, 1982]. This has the effect of introducing an additional error polynomial Sp(Q) which can be expressed in terms of the averaged value of the transients over one f_{ref} period. The actual values in the polynomial are dependent upon the level transitions and reference frequency f_{ref} involved. Sp(Q) represents dynamic non-linearity effects of the DAC and is distinguishable from DNL and INL in that the base spectrum before aliasing changes with output frequency. The DAC decorrelation technique aims to randomise the error polynomials so that there is no correlation of errors from one cycle of the DAC characteristic to the next.

8.4.2.3 The Principle of Decorrelation

In the time domain, decorrelation produces the effect shown in fig 8.5.

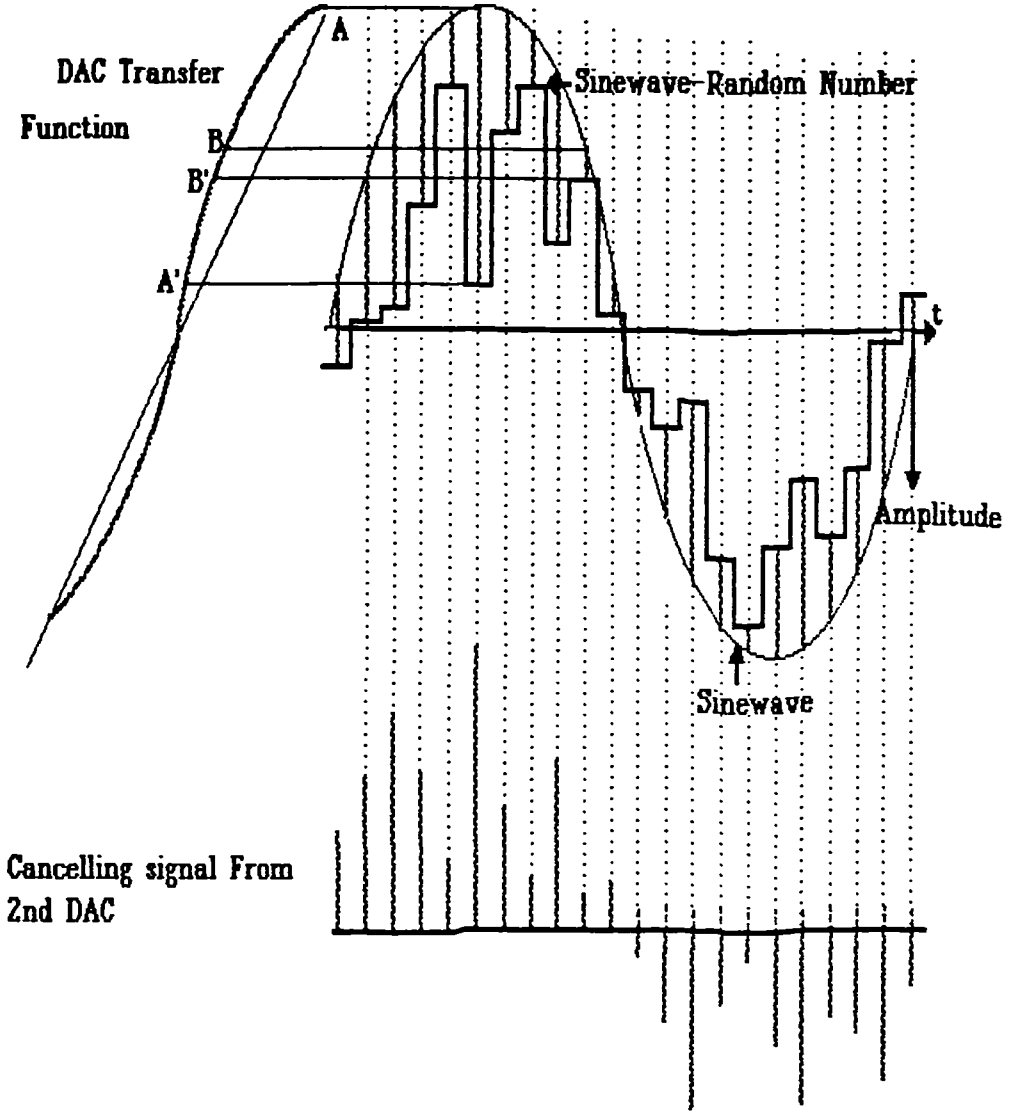


Fig 8.5 DAC decorrelation over one DDS cycle

A pseudo-random number is added or subtracted to the look up table output by means of an ALU placed at the digital port of the DAC. By reference to fig8.5 the decorrelation process acting upon a typical DAC transfer function can be observed. A DAC output level at point **A** becomes **A'** and that at point **B**, **B'**. By the analogue subtraction of a compensating signal from a second DAC, the signal is restored to the correct level. On a subsequent cycle of signal, for the same intended output point, the random number offset will be different, leading to a different values of **A'** and **B'**. Errors will therefore not correlate between adjacent cycles.

The effective output of the analogue circuitry is the average of all levels over which the decorrelation is applied. The memory mapped sinewave modified by the decorrelated DACS will have a spectrum as displayed in fig8.6. After sampling at the clock frequency, the noise, rather than the harmonics are folded back over the signal output range. Instead of a carrier plus aliased harmonics being present at the output, carrier plus noise result. Effectively, the reconstructed sampled data signal becomes a sinewave plus noise rather than sinewave plus harmonics: in order to completely randomise the polynomials, every level of the DAC should be used at random to generate each level of desired output signal. Therefore the added decorrelation factor must be uniform across all DAC levels, and be cancelled in the post DAC analogue section by means of another DAC.

In practice complete decorrelation of the DAC is difficult to achieve as the average value of all the DAC levels would be zero. Therefore a compromise must be reached where some weighting of the DAC decorrelation distribution is allowed. This weighting should be designed to be effective on the lowest order term possible in the error polynomials ie integral non-linearity [Zavrel, 1987]. Two methods of implementation of the decorrelation technique have been investigated by the author. These will be described below.

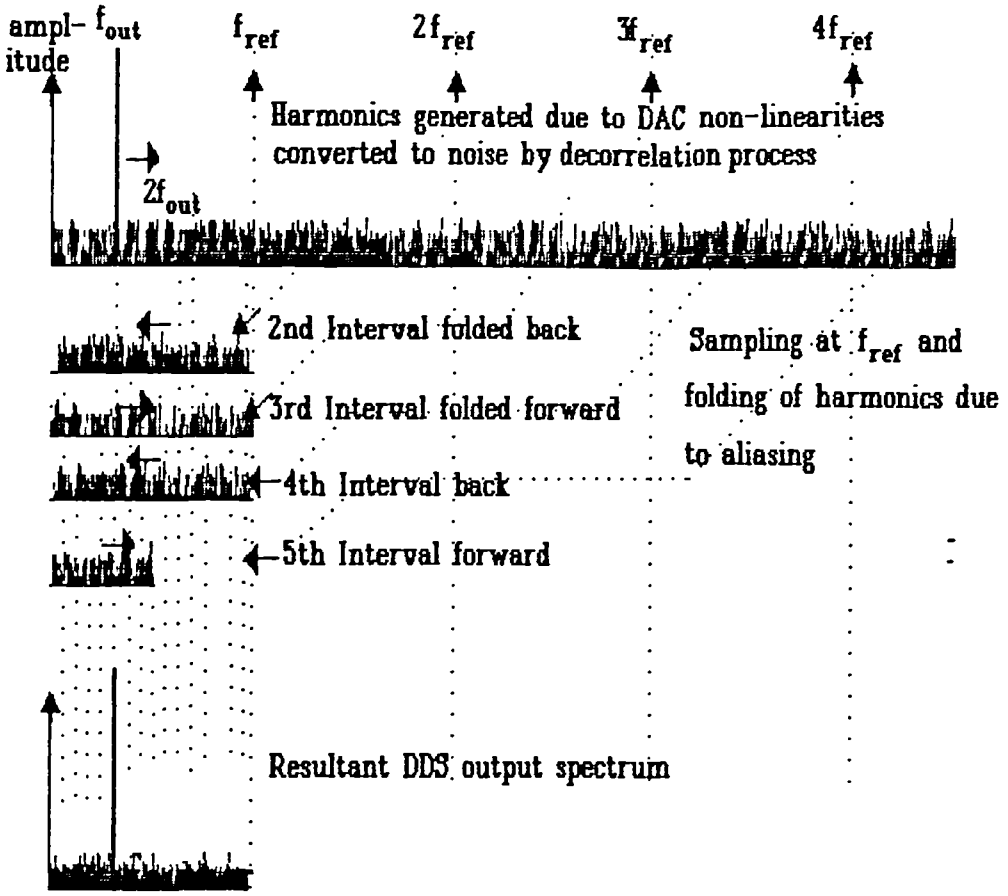


Fig 8.6 Conversion of spurious products to noise by the DAC decorrelation process

8.4.3 First Implementation Method 1: No Overflows

In this method a P-1 bit random number is subtracted (if the trigonometric word is positive) or added (if the trigonometric word is negative) to the main DAC input. In this manner overflows are prevented. The random number is also fed to the second DAC, and the output of the DACs are summed in such a manner that the desired output signal is recreated. It is seen that the random number component number is effectively removed. A residual error signal remains, but the error pattern becomes non-repetitive. Fig 8.7 demonstrates the technique.

Uppermost on fig 8.8 can be observed the output from the post look-up table DAC. The sinewave is regenerated by adding in the output of DAC2. With this technique, only the upper or lower half of the DAC is being decorrelated and there is a possibility of a repetitive discontinuity at the zero voltage level. Due to these factors, the improvement in spurious levels was expected to be limited. It was confirmed by measurement that there is a limit to spurious improvement of approximately 10dB (see fig 8.51 for results).

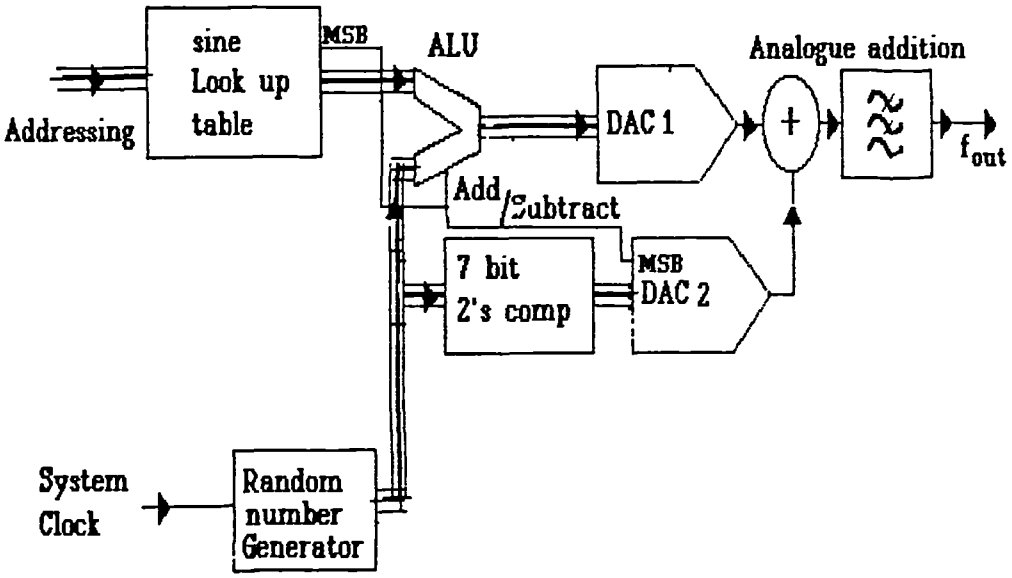


Fig 8.7 Decorrelation embodiment no 1

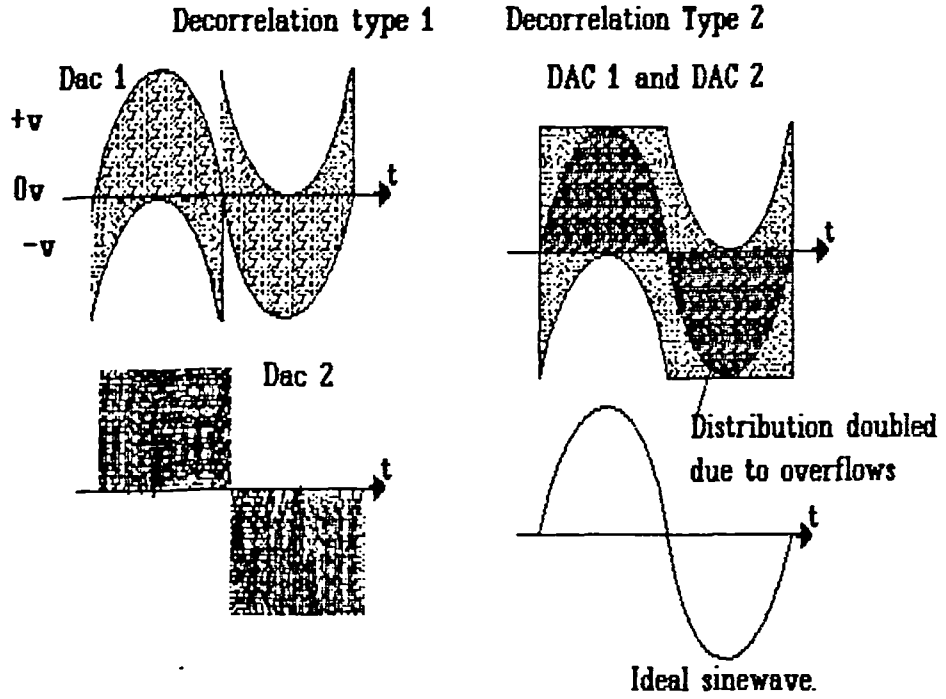


Fig 8.8a Probability distribution of DAC values, no overflows

Fig 8.8b Probability distribution with overflows

8.4.4 Second Implementation Method Allowing overflows

A modified decorrelation method was implemented to enable the use of accumulator overflows as displayed in fig 8.9.

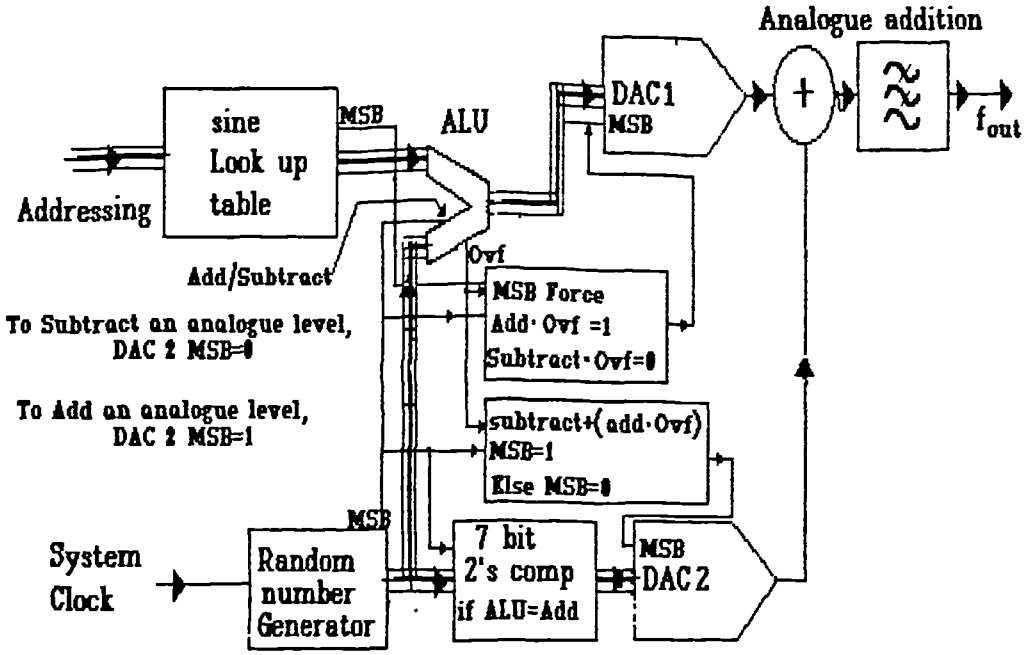


Fig 8.9 Decorrelation embodiment no2

In this method, the post look up table DAC output level is determined by the n-1 least significant bits of the n bit pseudo random number. Digital addition or subtraction of the random number to the output voltage word is achieved by an accumulator following the PROM table and ALU function is controlled according to the MSB of the random number. In this way, the ALU adds or subtracts randomly. The system would have to be able to accommodate ALU overflows: a problem exists in that when such an overflow occurs, the ALU would output a result corresponding to the opposite half of the sinewave to that of the desired output. This is unacceptable as the second DAC output can only compensate for up to half the output range.

A solution to the overflow problem found during the course of study for this chapter will now be described. If the sum of all the components added to, or subtracted from, the look up table output word a (and the resulting carry is ignored) all add up to (2^p) for a p bit word, then a value of a is again produced. These components can be added or subtracted by a mixture of digital and analogue means. Therefore on occurrence of an overflow, a half range ($2^p/2$) value is added or subtracted from the input to the DAC, by digital means, to bring it in range of the compensating DAC. This is most conveniently achieved by forcing the MSB of the DAC input. The compensating DAC adds the remainder to return the output to the correct level.

The following table summarise the operations for the four scenarios; where a is the amplitude word and y the p-1 bit pseudo-random number.

Table 8.2

Addition, no overflow		
DAC word	$a + y = a'$	
Compensation DAC	$-y$	
Result	$a' - y = a$	

Addition, with overflow		
DAC word	$a + y = a' - 2p$+carry	$(a'>2p)$
MSB adjustment DAC	$a' - 2^p + 2^{p-1} = a' - 2^{p-1}$	applied to signal
Compensation DAC	$+(2^{p-1} - y)$	
result	$a'-2^{p-1}+(2^{p-1}-y) = a$	

Subtraction no overflow		
DAC word	$a - y = a'$	
Compensation DAC	$+y$	
result	$a' + y = a$	

Subtraction with overflow		
DAC word	$a - y = a' + 2^p$ + borrow	$a<0$
MSB adjustment	$a' + 2^p - 2^{p-1} = a' + 2^{p-1}$	
Compensation DAC	$-(2^{p-1} - y)$	
output	$a' + 2^{p-1} - (2^{p-1}-y) = a$	

The function $2^{p-1}-y$ is readily provided by 2's complementing the $p-1$ bits of the random number y. Fig 8.8 in §8.4.3 of this chapter displays the distribution of DAC levels as a result of allowing overflows. Although the waveform structure of each DAC output appears identical, instantaneously the actual outputs are different. With this method, the decorrelation covers the total range of the DAC at the centre level of the waveform. At the waveform peaks, only half the DAC characteristic is used. A residual signal level is therefore still present in the DAC outputs giving rise to an intermodulation generation capability. It will be shown that there is still a second order harmonic and intermodulation generation capability; however any residual signal is less than the noise power, resulting in noise cross products being generated alongside signal cross products. This may suggest a reduction in signal related cross products. The effect of this method on integral non linearity may be limited therefore. On the other hand, differential non-linearity effects are completely decorrelated by method 2. With method 1, differential effects around the

centre of the DAC characteristic will not be decorrelated, and there would be a crossover distortion effect.

The method of combining the DAC outputs is important. Most high speed DACS have a current and an inverse current output (I and $\bar{I}$). It is important to use both the outputs in a balanced mode in order to reduce low even order effects [McCune, 1988]. A suggested method is given in fig8.10. This involves the use of all of the DAC output currents from both DACS in a summation circuit at the outputs.

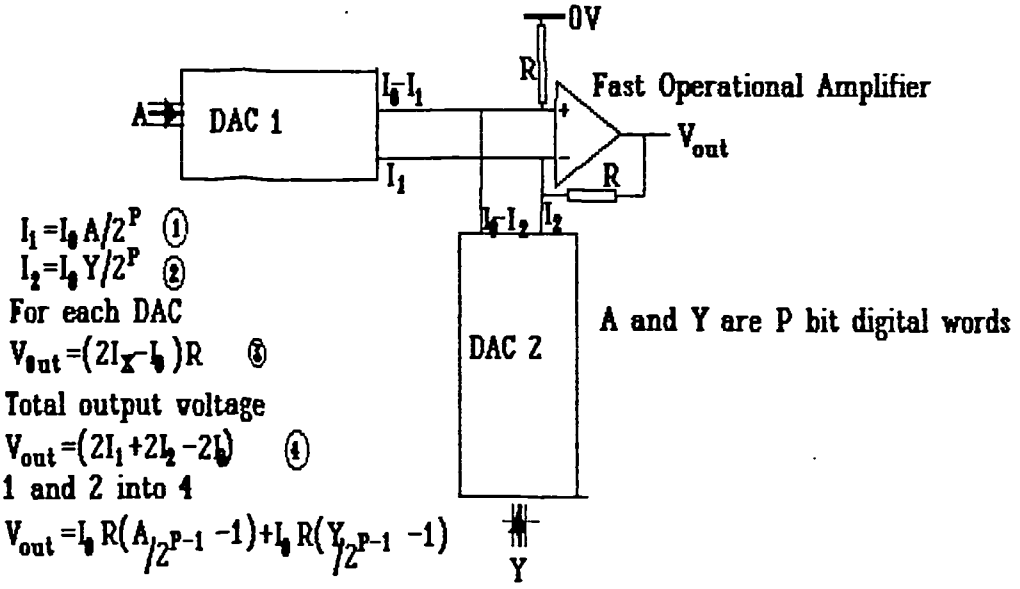


Fig 8.10 Analogue summation of decorrelated DACS

8.4.5 Reducing truncation spurious signals by Dither

All direct digital synthesisers will introduce some truncation of the digital phase and amplitude words. Both these truncation effects will each introduce spurious signals in the analogue domain. Truncation of the phase and amplitude digital words (quantization effects) result in a sawtooth error function as displayed in fig8.11. Wheatley and Phillips, [1981] proposed the use of phase accumulator dither to overcome the problem of DDS spurious. In their method the DAC was removed resulting in a squarewave rather than a sinewave synthesiser.

The process of dithering of the errors then becomes a one rather than a two dimensional (phase and amplitude) problem as with the sinewave synthesiser. Phase accumulator dither can be applied after the phase accumulator output. The output transition normally occurs too late by an amount t_e seconds, as there has to be an accumulator overflow in order to obtain an edge transition. The clock period will be represented as t_c.

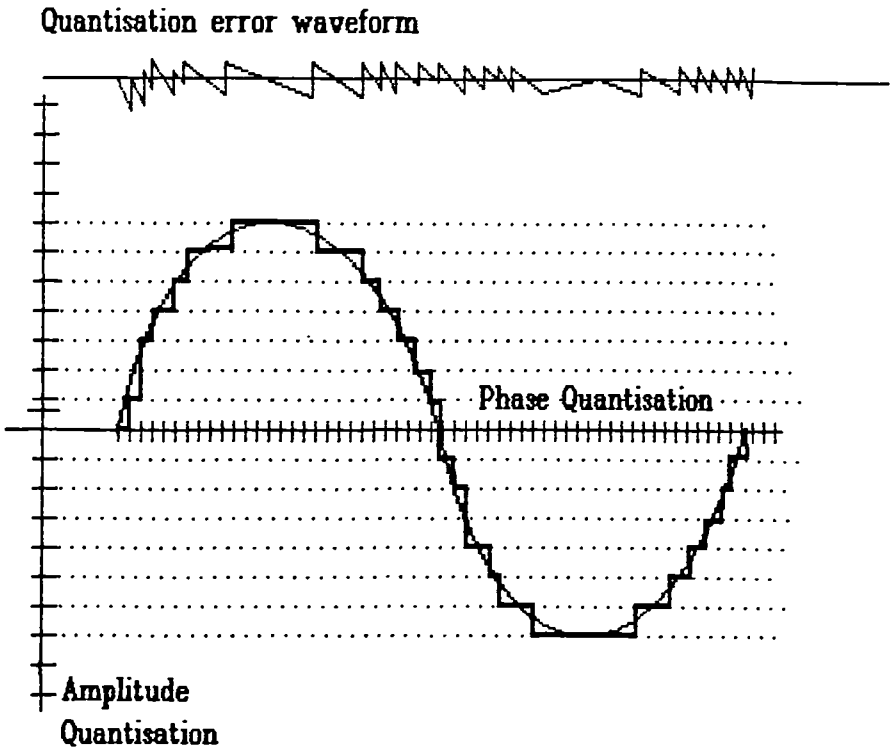


Fig 8.11 Error waveform due to DAC quantization

Therefore, although the average transition is correct, the repetitive edge jitter of up to one clock cycle too late gives rise to spurious products. Referring to fig8.12, when a random number of $e = 0$ to $e = k - 1$, where k is the frequency word, is added, the probability of late overflows is given by:-

$$p(t_e) = \frac{e}{k} \tag{8.2}$$

and the probability of early overflows by:-

$$p(t_e\text{-}t_c) = \frac{(1\text{-}e)}{k} \tag{8.3}$$

The resulting periodic average value $\langle t \rangle$ is:-

$$\langle t \rangle = t_e\, p(t_e) + (t_e\text{-}t_c)p(t_e\text{-}t_c) \tag{8.4}$$

Substituting equation 8.3 into 8.4 gives:-

$$\langle t \rangle = t_e\, \frac{e}{k} + (t_e\text{-}t_c)(1\text{-}\frac{e}{k}) \tag{8.5}$$

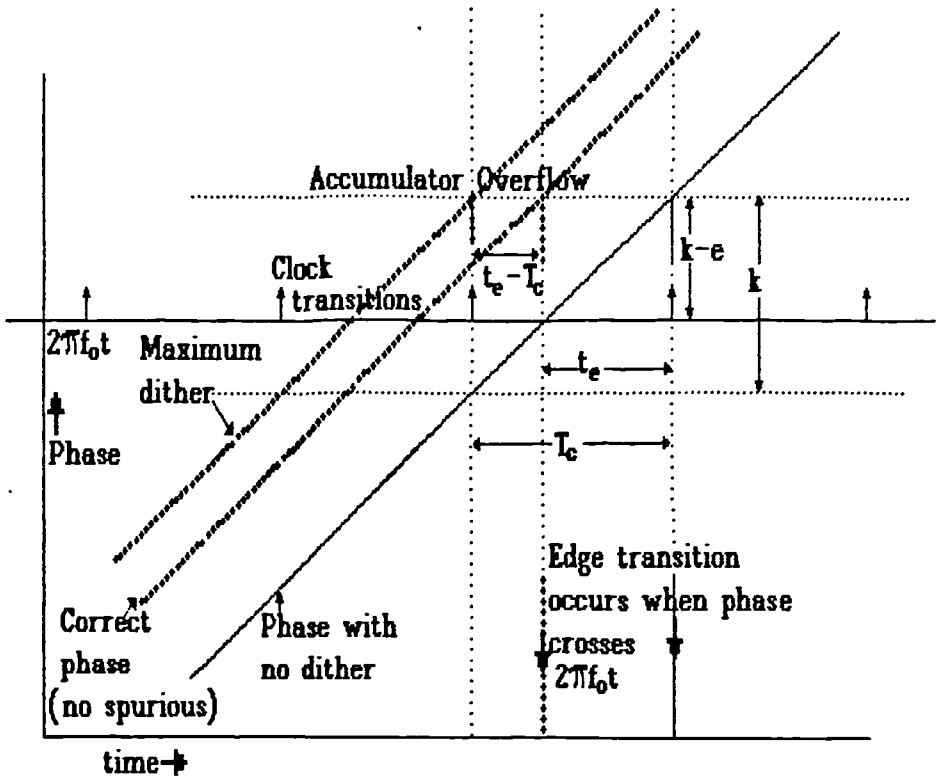


Fig 8.12 The Wheatley spurious reduction technique

Now from fig 8.12:-

$$\frac{k-e}{k} = \frac{t_e}{t_c} \tag{8.6}$$

Inserting this into equation 8.5 gives $\langle t \rangle = 0$. Although the average value of t=0, the actual value is randomly displaced from this, giving rise to phase noise. The error displacements using this method are large, resulting in high levels of phase noise (see fig 8.13).

The author has investigated the application of dither to a sinewave synthesiser. It was found [Wilson, 1990] that dither could be applied to provide interpolation (interpolative dither) between truncation points on the DAC and hence reduce spurious signals due to truncation. Phase noise can be much reduced if it is applied to a sinewave rather than a squarewave synthesiser. However, the situation is more complicated with the sinewave type of synthesiser. With a sinewave synthesiser, the error waveform is as displayed in fig 8.11. The cycle period of the sawtooth error waveform varies according to the part of the cycle of the synthesised wave.

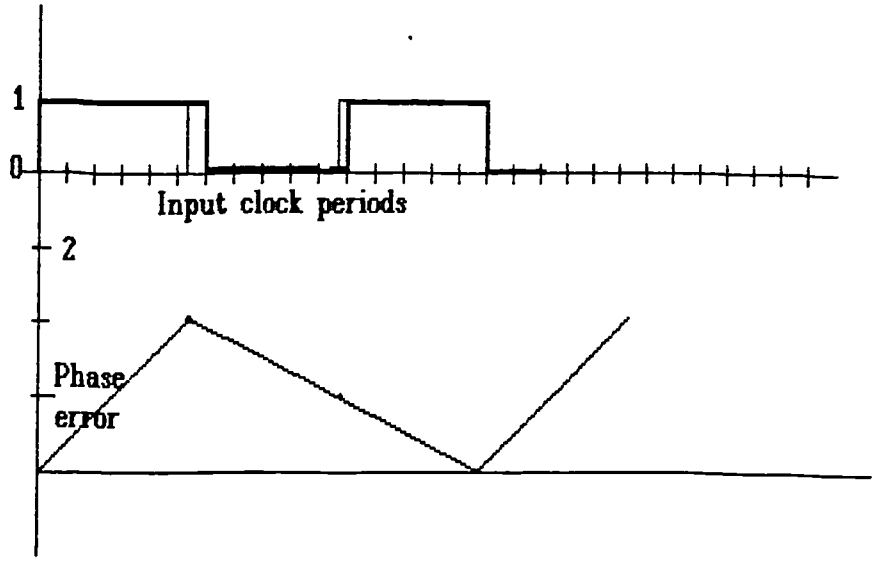


Fig 8.13 Phase error for the square wave DDS

If an 8 bit output look up table is driven from a 12 bit phase address, then the number of input steps per output step varies from 5 at zero level to 163 at the waveform peaks. There is obviously a trade off between dither and added phase noise. Unlike that of a squarewave synthesiser, the length between steps in phase is independent of frequency word, so the dither random number level can be fixed. The reason why dither has not previously been applied to a sinewave synthesiser is that the effect of DAC non-linearities dwarfs the contribution due to DAC quantization errors [Williams, 1987]. This would render the dither effect ineffectual if the DAC non-linearities are allowed to remain. However the effects of DAC decorrelation are such that the possibility of benefits from dither can be considered. Fig 8.14 displays the method used by the author to add phase and amplitude dither.

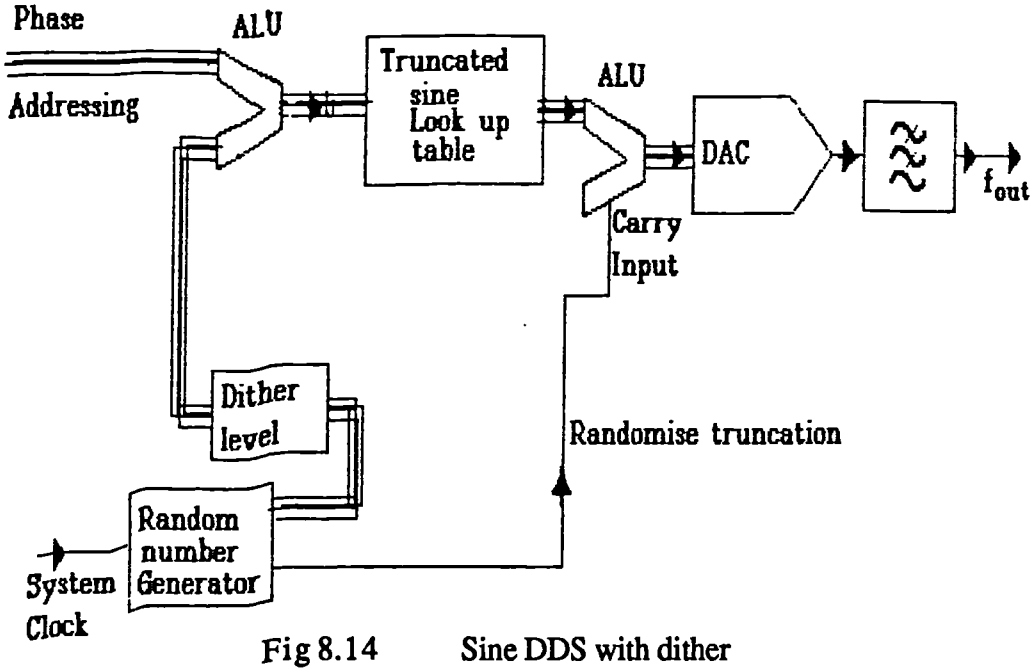


Fig 8.14 Sine DDS with dither

8.5 Phase noise penalty incurred by the new interpolative dither technique

8.5.1 Mechanism for phase noise effects

Although the new interpolative dither technique is effective in combating the DDS truncation problem, there is a disadvantage in that the use of pseudo random numbers introduces some broadband phase noise into the output of the DDS. The noise has a flat frequency distribution, therefore should be less of a problem for low data rate satellite communication system systems than other forms of phase noise. Since the clocking frequency of a DDS is generally high, the phase noise will be spread over a broad range of frequencies, resulting in a low value of phase noise density. It is important, however, to quantify these phase noise levels to compare the new technique presented here to that already suggested by Wheatley [*ibid*].

The phase noise mechanisms for a DDS using the new technique will be due to:-

1) Incomplete cancellation of the PRN at the DAC outputs;

2) The baseband component of the randomised glitch energy;

3) Noise due to interpolative dither on the truncation.

Incomplete cancellation of the PRN will result in noise at the output of the DDS. The feed through of the total noise energy is likely to be more of a problem at high clocking frequencies, but it may be possible to introduce some form of dynamically adjusting cancellation technique. Such a technique would adjust the timing and magnitude of the combining signals for the optimum broadband noise levels. This is beyond the scope of this thesis, but can be recommended as an item of further work.

The DAC glitches cannot be cancelled as the randomisation of this normally periodic effect is an inherent part of the technique.

The phase noise introduced by dither also cannot be cancelled as it is an inherent part of the technique, therefore it is vital that the minimum amount of dither commensurate with adequate spurious signal cancellation be used.

The last two effects, namely dither and DAC glitches will now be calculated for a typical DDS implementation.

8.5.2 Calculation of phase noise introduced by phase word dither

8.5.2.1 Noise power

In the consideration of noise effects, the following terms will be used:-

$N_{(\phi)}$ Total phase noise power to carrier ratio,

$S_{(\phi)}$ total phase noise equivalent power in radians,

n_o noise power total, *N* noise power density,

$S_{o(\phi)}$ total radian equivalent noise density,

$\mathcal{L}$ phase noise power density to carrier ratio

L the number of phase steps in one output cycle.

Since dither is applied before the look up table it can be considered as phase modulation. If the dither word is considered as width D, the equivalent RMS phase modulation power for a uniformly distributed dither signal is:-

$$D_{rms\phi} = \frac{D}{2\sqrt{2}} \tag{8.7}$$

Total noise power to radian ratio, S_ϕ is:-

$$S_\phi = 4\pi^2 D_{rms\phi}{}^2/L^2 \qquad \text{rads}^2 \tag{8.7b}$$

8.5.2.2 Frequency distribution

In order to obtain the noise density it is necessary to obtain the the frequency distribution of the noise. This noise is assumed to be constant between reference cycles. Therefore, from the sampling theorem, the noise distribution is:-

$$n_0(f) = n_0(0)\ \text{sinc}^2\left(\frac{\pi f}{f_{ref}}\right) \tag{8.8}$$

where $n_0(0)$is the effective noise density at DC. For the lower frequency of operation of the direct digital synthesiser,

$$n_0(f) \approx n_{(0)}(0)$$

The relationship between the noise density and total noise power is therefore:-

$$N = \int_0^{\infty} n_0(0)\ \mathrm{sinc}^2\left(\frac{\pi f}{f_{ref}}\right) df \tag{8.9}$$

Evaluating this integral [Dwight, 1961a] gives a relationship between noise density and total noise power for a sampled data system.:-

$$N = n_{0(0)}(f_{ref})/2 \tag{8.10}$$

Applying this to the noise power radian ratio of equation (8.7b) gives the radian noise density ratio $S_{0\phi}$ in terms of radian noise power ratio S_ϕ for small values of S_ϕ:-

$$S_{0\phi}(0) = 2S_\phi/(f_{ref}) \tag{8.11}$$

Therefore:-

$$S_{0\phi}(0) = \frac{8\pi^2 D_{rms\phi}{}^2}{f_{ref} L^2} \tag{8.12}$$

From modulation theory (see §2.4.4) the phase noise power density is 3dB less in value than the noise density in radians. Therefore, the phase noise power density ratio $\mathcal{L}_{(0)} = S_0/2$. Hence:-

$$\mathcal{L}_{(0)} = \frac{4\pi^2 D_{rms\phi}{}^2}{f_{ref} L^2} \tag{8.13}$$

Converting to a relationship involving the dither word D from equation (8.7) gives:-

$$\mathcal{L}_{(0)} = \frac{\pi^2 D^2}{2 f_{ref} L^2} \tag{8.14a}$$

It may be more convenient to express this in dB form:-

$$\mathcal{L}_{(0)} = 20(\log10(\pi)+\log10(D)-\log10(L)) - 10(\log10(f_{ref}))-3 \tag{8.14b}$$

The largest step on the phase axis occurs at the sinewave peak where $dv/d\Phi$ is a minimum. Calculations suggest that $L/32$ phase steps would be required to produce one LSB amplitude step at this point. This would give -83 dBc/Hz for 1 MHz clock rate and -113 dBc/Hz for 1 GHz clock rate. For comparison, the Wheatley technique gives the following result [Wheatley & Phillips, 1981]:-

$$\mathcal{L}_{(0)} = \frac{3 f_{ref}{}^2}{\pi^2 f_{out}} \tag{8.15a}$$

For $f_{out}/5$ this would result in -62 dBc/Hz for 1 MHz and -92 dBc/Hz for 1 GHz, an improvement of 21 dB using a DAC.

If the value of the dither word is reduced, then the phase noise introduced will reduce but the spurious signals will rise. It is therefore possible to arrive at a suitable compromise for the system requirements. A good compromise would be one step width at the zero crossing point where the effect of truncation errors would be a maximum upon the phase jitter. In this case, the value of L would be 1024. Corresponding phase noise figures are then 101 dBc/Hz at 1 MHz and -131 dBc/Hz at 1 GHz. Using a 10 bit DAC would improve these figures to -113 dBc/Hz at 1 MHz and -143 dBc/Hz at 1 GHz.

One problem with the dither technique using DACs is that the width of the DAC step varies throughout the cycle. Ideally, therefore the dither dimension D would have to vary, which would be considerably difficult to implement in hardware. Therefore the effect on spurious reduction of a non ideal dither must be considered.

8.5.3 Non ideal phase word dither

Phase dither performs a time averaging function on the waveform. The dither can be considered therefore as a window which is time shifted by the system clock. This is demonstrated in fig 8.15.

Truncation gives a sawtooth shaped waveform as displayed in fig 8.11. The effect of dither on the truncation errors may be demonstrated by approximating the sawtooth waveform to a sinewave. Therefore, the frequency domain representation will be a single spurious signal corresponding to this sinewave.

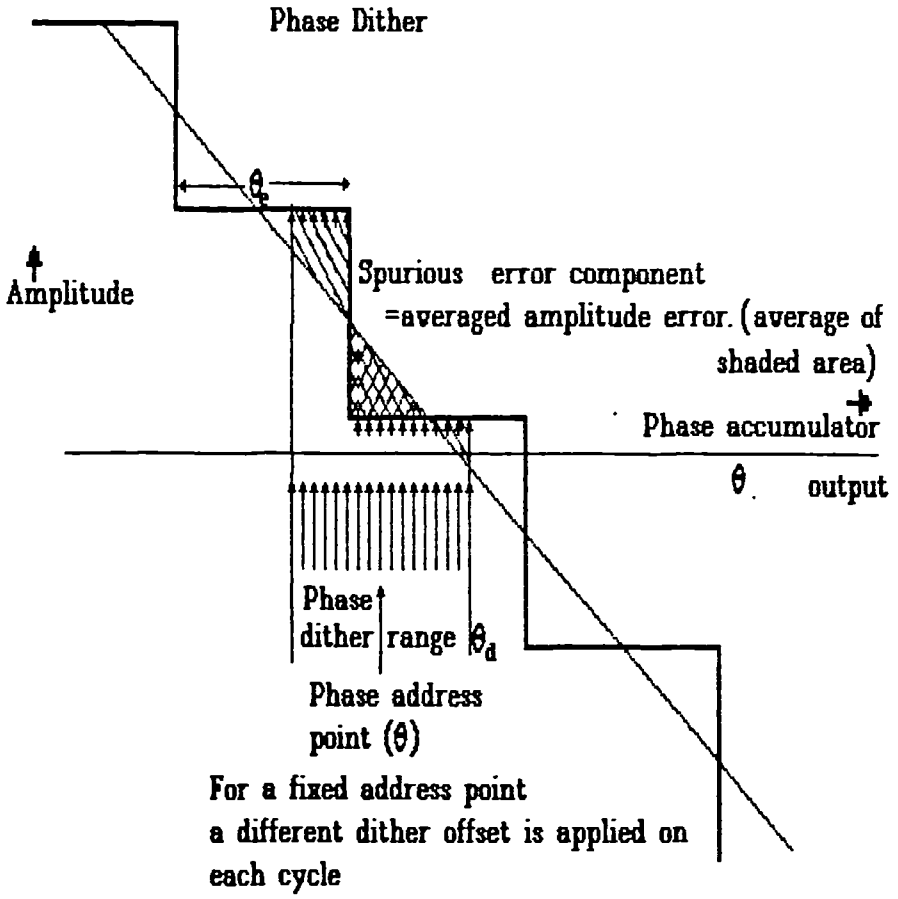


Fig 8.15 Phase Dither

If dither is applied, the effect displayed in fig 8.16 occurs for a error waveform E_t given by:-

$$E_t = E_{tpk} \cos(\omega t) \tag{8.15b}$$

where E_{tpk} is the peak amplitude.

The point in the ωt axis that a sample is taken is uniformly distributed throughout the dither width, therefore the average periodic residual of the waveform can be represented as:-

$$\langle E_t \rangle = \frac{E_{tpk} \int_0^{\omega t_1} \cos(\omega t) dt}{(\omega t_1)} \tag{8.15c}$$

giving:-

$$\langle E_t \rangle = E_{tpk} \text{sinc}(\omega t_1) \tag{8.15d}$$

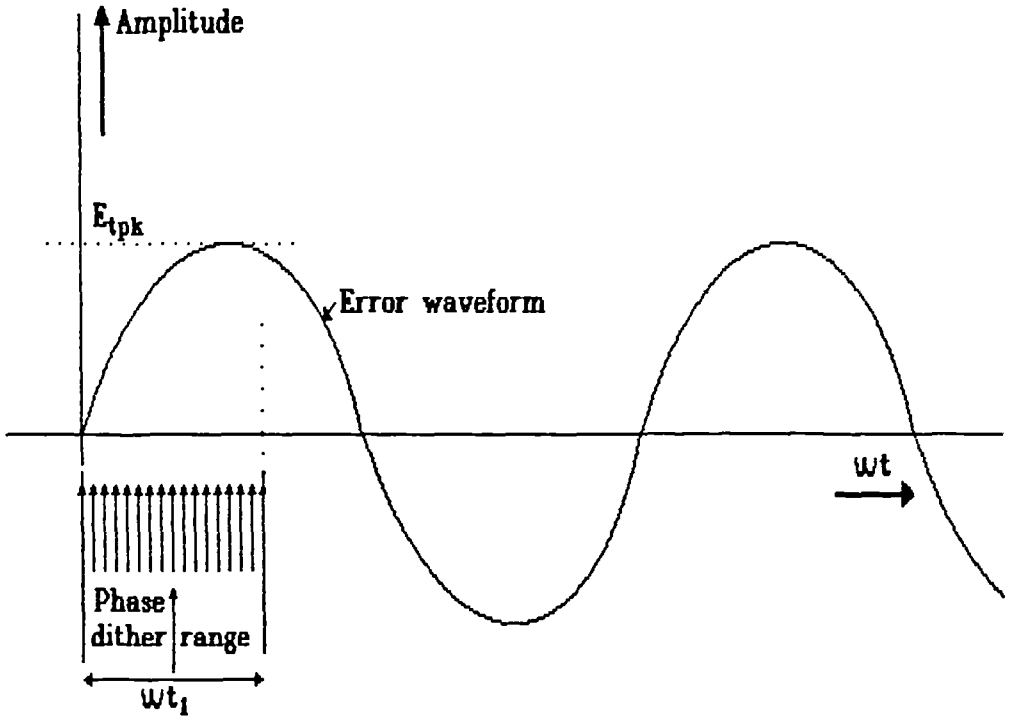


Fig 8.16 Effect of non-ideal phase dither on a sinusoidal error component

A sketch of these function is given as fig8.17.

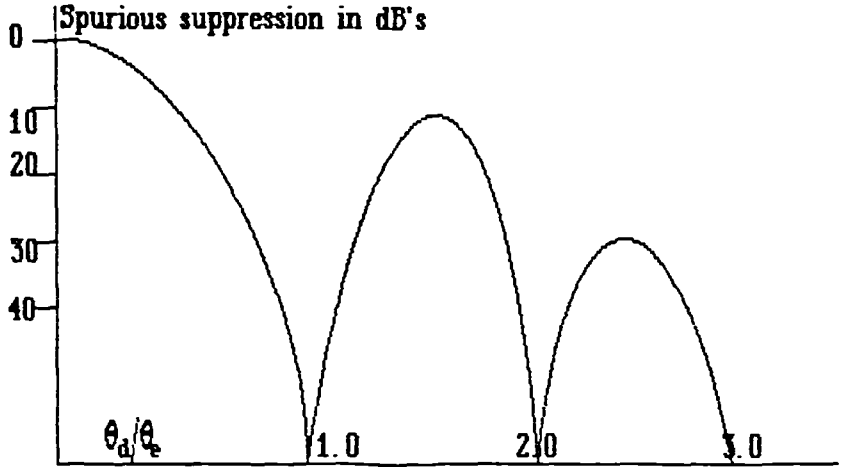


Fig 8.17 Dither width / error waveform width in phase space

The amplitude of the resulting spurious signal after dither will be non-zero apart from exact multiples of the DAC step. Therefore apart from this special case, a repetitive residual will remain, although the amplitude of the correlated repetitive error signal will reduce. So if a restriction must be placed on the dither width D, then it could be worth considering another dither function other than uniform. One possible function that could be readily implemented is the Gaussian function. This suggests that a computer

simulation would be required to determine the effect of both uniform and Gaussian functions on the error residual is required. Such a simulation is beyond the scope of this thesis, but can be recommended as an item of further work.

8.5.4 Amplitude Dither

The effect of amplitude dither is to randomise the round up of the least significant bit at the DAC input. Fig 8.18 displays the effect of a finite truncated word on the synthesised sinewave. The sinewave becomes a series of quantized steps. This has been attributed [Reinhardt, 1986] as the major contributor to source of spurious signals in DDS, but it is maintained that this is incorrect and the predominant source is from DAC dynamic effects.

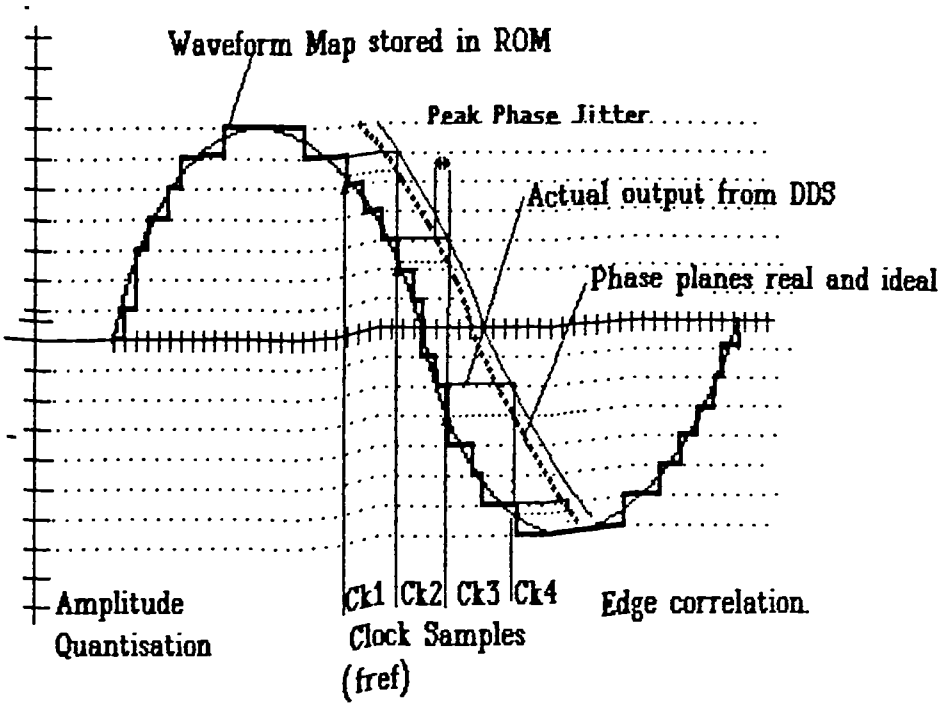


Fig 8.18 Error waveform through DAC quantization in a DDS

Each quantized step produces its own set of Fourier components. By using Parsivals' theorem it can be shown that the sum of all the individual quantized steps (ie the composite synthesised waveform) is equal to the sum of the Fourier components of each step. Some of the Fourier components will be coincidental at certain output frequencies. As the Fourier components will be additive and subtractive, widely different levels of these Fourier components will be present across the output spectrum. An analysis of the spectrum of DDS phase and amplitude truncation has been presented [Nicholas and Samueli, 1987] which demonstrates that spurious products can indeed be additive and produce high levels at some output frequencies. The maximum spurious signal for a 8 bit DAC and 12 bit phase quantization is -47.5 dBc; this can be compared with the general formula for DDS truncation noise [Hosking, 1973], e_r:-

$$e_r = 2^n\sqrt{6} \qquad (8.16)$$

which gives a value of signal to noise of 56dB. In order to satisfy Parsivals' theorem, the amplitude of the wanted signal must reduce, which implies correlation of the quantization edges.

8.5.5 Quantization edge correlation

Fig 8.18 also displays the effect on a sampled quantized waveform of correlated edges. Clock samples are denoted by ck1, ck2 etc. At ck8 the sequence is repeating but advanced by few bits. On successive samples of the complete waveform, the sampling points advance to the quantization edge and there is a simultaneous shift in all the sampling points, resulting in a maximum amount of phase jitter. This increase of close to carrier phase jitter will be shown in the truncation simulation of §8.10.2 of this chapter. The phase modulation can be approximately shown to be -52dBc. This quantization edge effect can be reduced by means of amplitude dither of one least significant bit, giving an effect as displayed in fig8.19. The sine look up table is truncated rather than rounded, and a least significant bit is added at random, to enable the table output to be either rounded up or down at random.

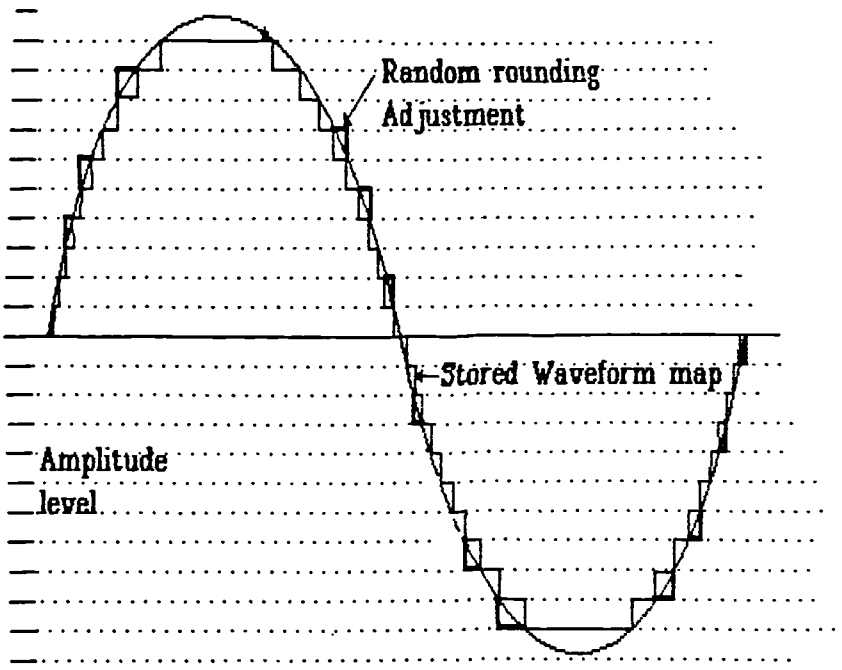


Fig 8.19 Destruction of edge correlation by means of amplitude dither

Effectively, the contribution of each quantization edge is randomised, reducing the effect of spurious product addition. There is still periodicity in the averaged error waveform however, resulting in discrete spurious signal products, but they are more evenly distributed. This periodicity is displayed in fig8.19. Phase dither can be applied to

reduce this periodicity by means of an adder on the output of the phase accumulator as in fig 8.14, in §8.4.5 of this chapter. If amplitude dither is applied together with phase dither, then any remaining repetitive errors will be evenly distributed across the spectrum. A DDS built by the author using uniform phase dither and amplitude dither was found to have (see fig 8.51) discrete spurious products of approaching 80dB using 8 bit DACs at frequencies up to $f_{ref}/8$. This is unprecedented for a direct digital synthesiser using 8 bit DACs.

8.5.6 Phase Noise as a result of DAC Decorrelation

It has already been noted that the process of DAC decorrelation implemented while undertaking work associated with this chapter, (see §8.4.2) converts spurious signals to broadband additive noise. It is important to calculate the level of phase noise produced. Presented here is an analysis produced by the author of the expected phase noise due to decorrelation of glitches. The principal contribution to the spurious signals of an unmodified DDS is the DAC switching glitches, therefore it is expected that the principal contributor to decorrelated DAC noise will be glitches.

The waveshape of a typical DAC glitch is displayed in fig 8.20.

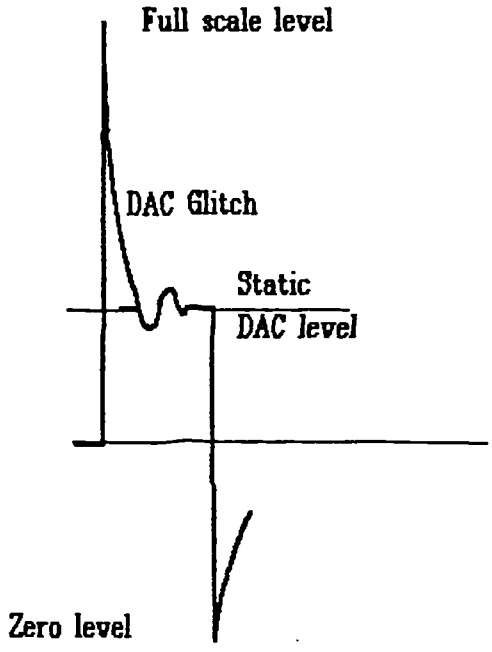


Fig 8.20 Typical DAC transition with glitches

It has already been previously stated in §8.2.10 that the glitches that occur as the DAC changes state are likely to be the major source of noise. Rather than sampled pseudo random noise, the noise takes the form of a series of Dirac Delta functions (see fig 8.21)

[Stroud, 1985] of pseudo random area. This can be formed by differentiating the sampled random function.

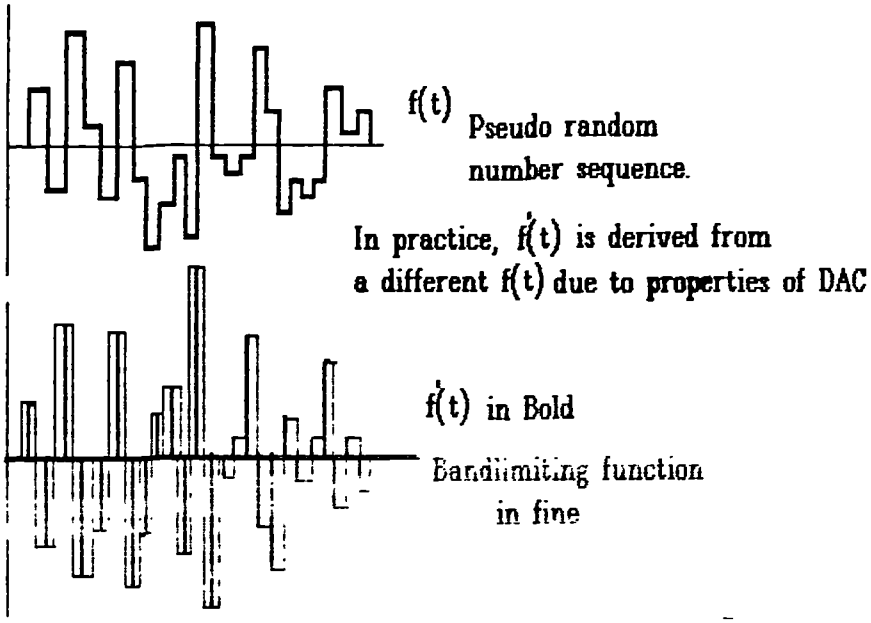


Fig 8.21 Noise contributions of DAC glitches

The differentiated glitch pseudo random function is unrelated to the actual pseudo random sequence that is used to decorrelate the DACs as the glitch amplitude is unrelated to the DAC level transition, but the distribution of glitch levels is assumed here to be uniform. By differentiation of the pulse spectrum, the shape of the glitch spectrum can be derived. The Laplace Transform of the differentiation operation in the time domain is equivalent to multiplication by s in the frequency domain. In the frequency domain, a pseudo random signal $V_n(f)$ can be represented as:-

$$V_n(f) = \sqrt{n_0(0)}\,\mathrm{sinc}\left(\frac{\pi f}{f_{ref}}\right) \tag{8.17}$$

Differentiating this in the frequency domain is equivalent to multiplying this by $2\pi f/f_{ref}$, therefore:-

$$\dot{V}_n(f) = \sqrt{4n_0(0)}\,\sin\left(\frac{\pi f}{f_{ref}}\right) \tag{8.18}$$

In order to calculate the noise power for a particular output frequency, equation (8.18) is integrated over all frequencies. As in the case of evaluating phase noise due to dither, the integral of this equation is made equal to the power as calculated from the time domain representation of the waveform.

Hence, the frequency domain power calculation is:-

$$N_{(\phi)}{}^2 = \int_0^{\infty} 4n_0(0)\,\sin^2\left(\frac{\pi f}{f_{ref}}\right)df \tag{8.19}$$

The result of this evaluation of this integration is infinity as the sin x function is not contained. This agrees with the time domain representation which will also be infinity on account of the infinite height of the Delta Dirac function. Unfortunately, the evaluation of the spectral density function n_o at a particular output frequency from direct integration of equation (8.19) is therefore prevented. One way to overcome this problem is to consider the power which is likely to appear in band only. The power can be band limited by considering the glitch to be averaged over one clock cycle as in fig8.21 above. Bandlimiting the power in this way can be achieved by multiplying by the hold function.

If the peak glitch energy is represented by the voltage averaged over one second, as Q Volts seconds, and assuming a uniform distribution of glitches, the average glitch power may be expressed as:-

$$N_{(g)} = \frac{Q\, f_{ref}{}^2}{2} \tag{8.20}$$

Assuming the glitch energy remains constant over one clock cycle, the glitch can be multiplied by the hold function,

$$H_{(f)} = \mathrm{sinc}\left(\frac{\pi f}{f_{ref}}\right) \tag{8.21}$$

This gives a function representing the approximate in band noise power distribution:-

$$V_n(f) = \sqrt{4n_0(0)}\sin\left(\frac{\pi f}{f_{ref}}\right).\ \mathrm{sinc}\left(\frac{\pi f}{f_{ref}}\right) \tag{8.22}$$

Squaring 8.22 to obtain the noise power density gives:-

$$n_0 = 4n_0(0)\frac{\sin^4\left(\frac{\pi f}{f_{ref}}\right)}{\left(\frac{\pi f}{f_{ref}}\right)^2}df \tag{8.23}$$

This function is now contained and the power in the frequency domain spectrum can be evaluated [Dwight, 1961b].

$$N = \int_0^{\infty} 4n_0(0) \frac{\sin^4\left(\frac{\pi f}{f_{ref}}\right)}{\left(\frac{\pi f}{f_{ref}}\right)^2} df \qquad = n_0 f_{ref} \tag{8.24}$$

The quantity $4n_0(0)$ represents the maximum noise density point on the output spectrum and will be referred to N_{omax}.

In the time domain, the power level must now be evaluated. If the output range is represented by V volts, then the signal output RMS power will be $V/2\sqrt{2}$. Assuming a uniform distribution of glitches in the time domain, the noise to signal ratio (N/C) at the output of the DAC is therefore given by:-

$$N/C = 8\left(\frac{Q\, f_{ref}}{V_{DAC}}\right)^2 \tag{8.25}$$

From Parsivals' theorem, the total power in the time domain can be equated to the total power in the frequency domain:-

$$N = \frac{n_{omax} f_{ref}}{4} \tag{8.26}$$

From equations (8.25) and (8.26),

$$n_{omax}/C = 32 f_{ref}\left(\frac{Q}{V_{DAC}}\right)^2 \tag{8.27}$$

Substituting this into the differentiated noise spectral density function (equation (8.18)) results in an equation for the additive noise density ratio n_o/C:-

$$n_o/C = 32 f_{ref}\left(\frac{Q}{V_{DAC}}\right)^2 \sin^2\left(\frac{\pi f}{f_{ref}}\right) \tag{8.28a}$$

For random additive noise, the phase noise sideband components are half of the total additive noise, therefore the phase noise $\mathcal{L}_{(\phi)}$ is:-

$$\mathcal{L}_{(\phi)} = 16 f_{ref}\left(\frac{Q}{V_{DAC}}\right)^2 \sin^2\left(\frac{\pi f}{f_{ref}}\right) \tag{8.28b}$$

This is the final result for the prediction of phase noise due to glitches after DAC decorrelation. The spectral shape of the resulting signal plus noise is as shown in fig 8.22.

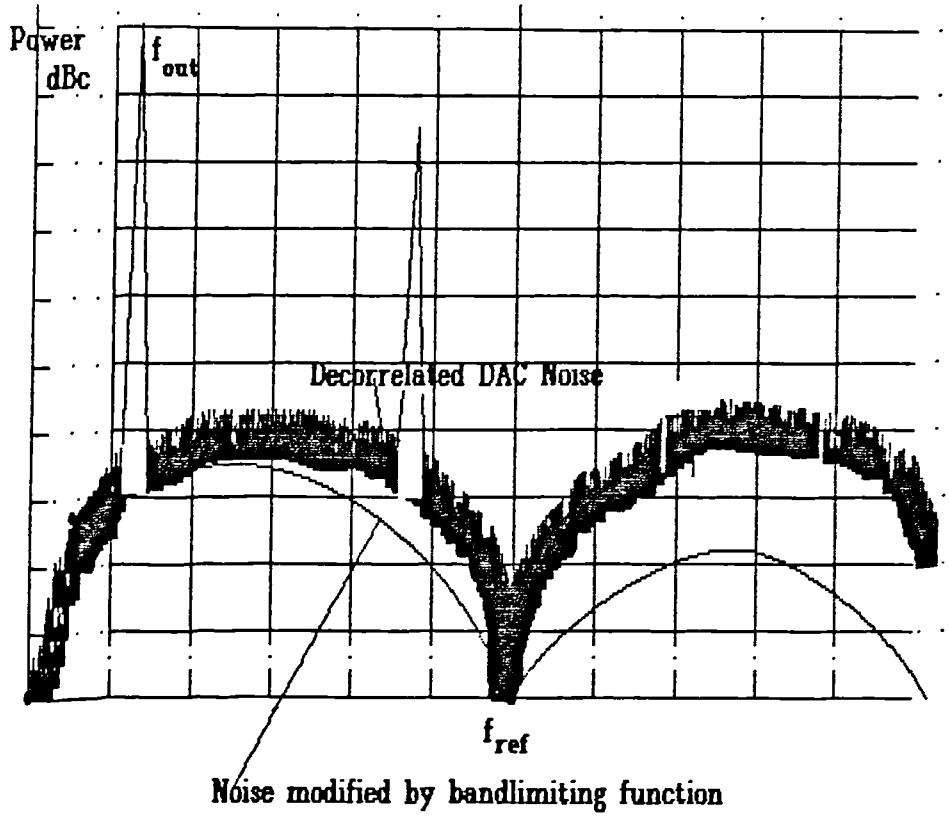


Fig 8.22 Signal and noise spectrum of DDS with DAC decorrelation

Equation 8.28b implies that the glitch spectrum will have a distinctive shape rather than the flat spectral shape predicted for the other error spectrums. Fig8.51 in §8.11.6 show results measured from a DDS incorporating DAC decorrelation built by the author. It can be observed that the spectra are indeed not flat and in fact the phase noise declines at 6dB per octave for reducing output frequency as can be expected by equation 8.28b for $f_{out}<<f_{ref}$. If this equation is applied to some commercially available DACs then interesting results follow, as below.

Considering 2 DACs, the noise power will be purely additive, however and will increase by 3 dB. The net result will be a degradation of 3dB in signal to noise ratio over that predicted above.

Table 8.3 presents the dynamic characteristics of some of the latest generation of high speed DACs. The commercial DACS under consideration are: the Triquint TQ6111B [TRW, 1988], TRW TDC1018 [F.g.Weiss, A, 1986] and the latest development from Analogue Devices, the low glitch AD9720.

Table 8.3

	TQ6111B	TDC1018	AD9720
Resolution	8 bit	8 bit	10 bit
Max clock frequency	1 GHz	200 MHz	350 MHz
Glitch energy	25 pVsec	30 pVsec	4 pVsec
Full scale range	1 V	1.071	1.0 V

If the TDC1018 is clocked at 200MHz and an output frequency of 50MHz is selected, the close to carrier additive noise can be calculated to be be -116dBc/Hz, corresponding to -119dBc/Hz of phase noise. With the Triquint clocked at 1GHz, and an output frequency of 250MHz chosen, -113dBc/Hz of Phase noise can be expected, while selection of 50MHz, will result in -126dBc/Hz of phase noise.

With the low glitch DAC type ADC 9720 the phase noise at 50MHz would be an impressively low -139dBc/Hz. This performance is 35dB better than the Wheatley technique. The above phase noise figures could be improved if a sample and hold is placed after the DACS to reduce some of the glitch energy. This would incur a cost penalty and may degrade spurious performance.

8.6 Calculation of spurious reduction as a result of DAC decorrelation

8.6.1 Spurious signal generation due to DAC errors in DDS

After calculating the predicted phase noise levels an attempt will be made to analyse the spurious signal levels in order to assess the advantage of the new technique. Spurious product calculation is an extremely complex issue. However, a comparison can be gained by the introduction of a DAC error and a subsequent calculation of the spurious products. In this treatment of the problem, the spurious products are considered to originate from a 'base spectrum', which is the Fourier series representation of the primary waveform before sampling and aliasing effects take place. Points on this primary waveform are addressed by the phase output of the accumulator, therefore the usual horizontal time axis for waveforms is replaced with a phase space axis.

The base spectrum consists of a sinewave and harmonics. We model the DDS process as a sampled waveform system where the sampled waveform is the stored sinewave plus errors, called the primary waveform. This stored waveform consists of a sinewave and

distortion products (harmonics) giving rise to the primary or base spectrum mentioned in §4.4.3. The actual output of the DDS is equivalent to sampling the primary waveform at a clock frequency f_{ref}. §4.4.3 discusses how these harmonics are aliased by the sampling frequency (clock). Fig 8.23 displays a time domain representation of the DDS base spectrum with an error added to the DAC to initiate calculation of the spurious products.

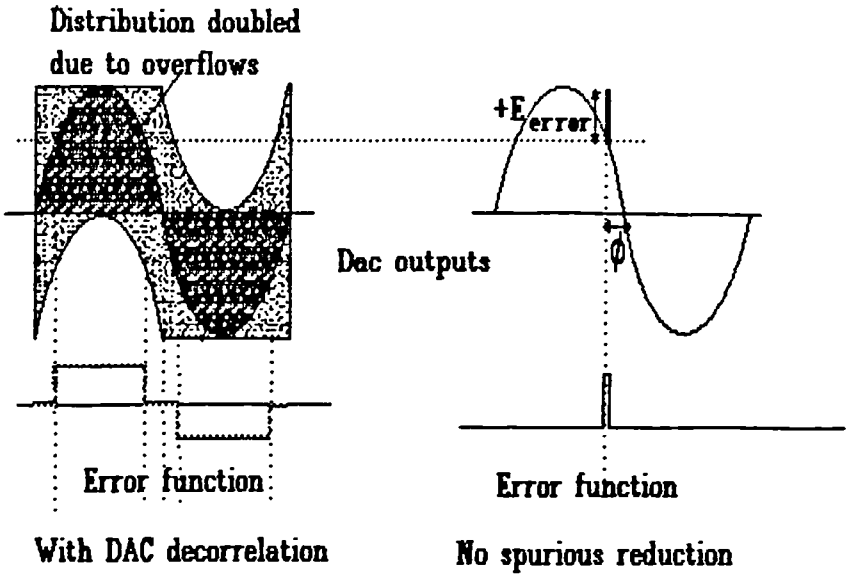


Fig 8.23 Probability distribution of DAC values

Fig 8.24 displays the resulting error function rescaled in preparation for conversion to its corresponding Fourier series. The error pulse is one DAC step wide and occurs once per accumulator cycle. The mark - space ratio of this pulse in the primary waveform is $2\pi m$ where:-

$$m = 2^{p-1} \tag{8.29}$$

and p is the resolution of the DAC in bits. The maximum width of this pulse in primary waveform phase space T is:-

$$\Delta\phi_{max} = \cos^{-1}\left(1 - \frac{1}{m}\right) \tag{8.30}$$

If $\Delta\phi$ is less than $\Delta\phi_{max}$ then:-

$$\Delta\phi = \frac{1}{m}\,\mathrm{Sec}(\phi) \tag{8.31}$$

From fig 8.24, the Fourier series coefficients are:-

$$A_n = \frac{2}{\pi}\int_0^{\Delta\phi/2} E_{error}\cos(nx)dx \tag{8.32}$$

This gives a series:-

$$E_{Series} = \frac{E_{error}}{\pi} \sum_{n=0}^{n=\infty} \frac{1}{n} \text{Sin } n \frac{1}{m} \text{Sec}(\phi) \cos nT \tag{8.33}$$

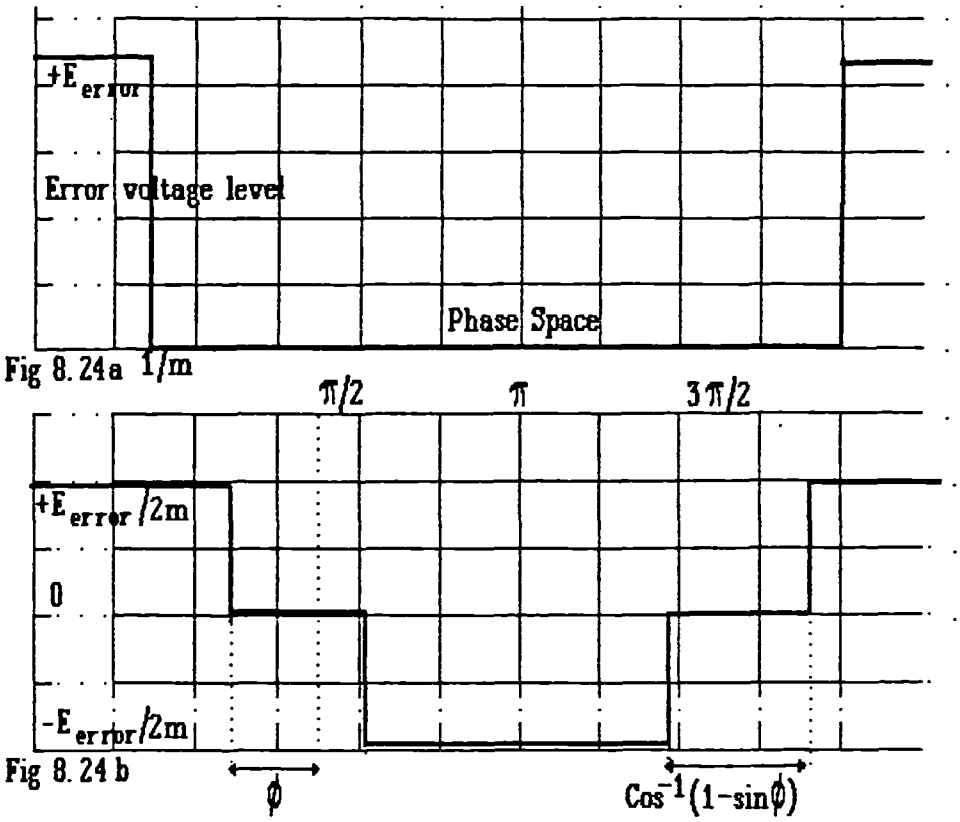


Fig 8.24 Error responses for DDS without (upper) and with (lower) DAC decorrelation

For comparative purposes, let the error occur at an angle of 30°. Also assuming that n is $<< m$, that is the harmonics considered are less than the reciprocal error pulse width, then the above series approximates to a flat comb of harmonics of the form:-

$$E_{Series} = \frac{E_{error}}{m\pi}\left(\frac{2}{\sqrt{3}} + \frac{2}{\sqrt{3}} \cos(T) + \frac{2}{\sqrt{3}} \cos 2(T) + \ldots\ldots\right) \tag{8.34}$$

This is an important result as it goes some way to explaining why spurious signals abound in many DDS implementations. A large series of slowly declining spurious signals result. These will be aliased back to around the carrier frequency as discussed in chapter 4.

8.6.2 Effect of DAC decorrelation on static errors

Initially, the spurious signals generated by static errors will be considered. These are represented as before by an error E_{error} as before. There are three levels of probability of the error influencing the output.

1) Probability 0

2) Probability 1/2m

3) Probability 1/m

Probability of zero occurs when the output is more than the MSB in equivalent voltage level away from the point at which the error occurs. A probability of $1/2m$ occurs when there are no overflows (thinly shaded region of fig8.23). A probability of $1/m$ occurs when overflows result in the folding over of the DAC outputs. The effective error output voltage is shown in fig8.24.

The Fourier series of this waveform will now be found to enable the base spectrum to be calculated. By multiplying this probability by the error voltage, one can find the contribution of the error to the output. Inserting this into the formulae for the Fourier coefficients gives:-

$$A_n = \frac{1}{\pi}\left(\int_0^{\pi/2-\phi} \frac{E_{error}}{m}\cos(nx)dx\right) + \frac{1}{\pi}\left(\int_{\pi-\cos^{-1}(\sin\phi)}^{\pi} \frac{E_{error}}{m}\cos(nx)dx\right) \tag{8.35}$$

Calculating the Fourier coefficients results in:-

$$A_n = \frac{1}{\pi}\frac{E_{error}}{m}\frac{1}{n}\left(\sin n\left(\pi/2-\phi\right)+\sin n\left(\pi-\cos^{-1}(\sin\phi)\right)\right) \tag{8.36}$$

For comparison with the undecorrelated case, the coefficients are calculated for the case of the error appearing at an angle of 30 degrees, therefore substituting $\phi = \pi/6$ into equation (8.36) gives:-

$$E_{Series} = \frac{E_{error}}{n\pi m}\left(\sqrt{3}\right)\cos 5(T)+\sqrt{3})\cos\ 7(T)+..... \tag{8.37}$$

Fig 8.25 compares the spurious levels contributed by equation 8.34 with the spurious levels from equation 8.37. For values of ϕ other than $\pi/6$, even products will begin to appear, but at reduced levels. The important difference is the appearance of the factor $\frac{1}{n}$ in the coefficients, thus resulting in much lower levels of high order spurious signals. All

spurious signals are reduced relative to the undecorrelated case, but in particular the reduction of higher spurious products gives a much cleaner spectrum.

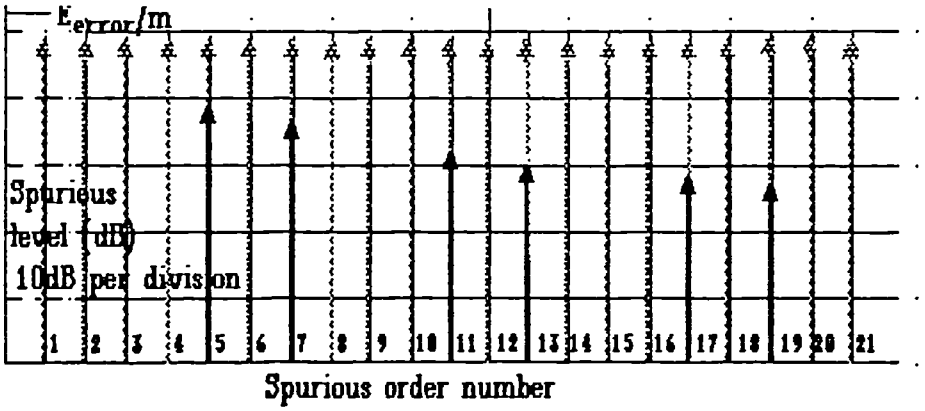


Fig 8.25 Comparison of spurious levels for static errors, with and without DAC decorrelation

8.6.3 Dynamic errors

8.6.3.1 definition

At high clocking speeds, dynamic errors are the major cause of spurious products, rather than static errors, and the spurious reduction scheme was designed particularly to cope with dynamic errors. Such errors relate to the clock frequency and display a distinction from static errors in that their contribution to the primary spectrum depends upon the clocking frequency. In our analysis presented here the assumption is made that switching glitches are the main contributor to dynamic errors: the highest glitch levels occur for changes in the second most significant bit (MSB/2) and the most significant bit (MSB) of the DAC word, which are the major transition points and therefore give the highest level of dynamic errors.

8.6.3.2 MSB/2 glitches

The probability of a second most significant bit transition (for example from 00111111 to 01000000 for an 8 bit DAC) is analysed here. In fig 8.26 the distribution of transitions can be seen. At the most negative point (level 0), point A on fig 8.26, the probability of a MSB/2 transition is 0.25. As the output level rises, transitions of MSB/2 to zero in the lower quarter will be replaced by identical transitions to the third quarter.

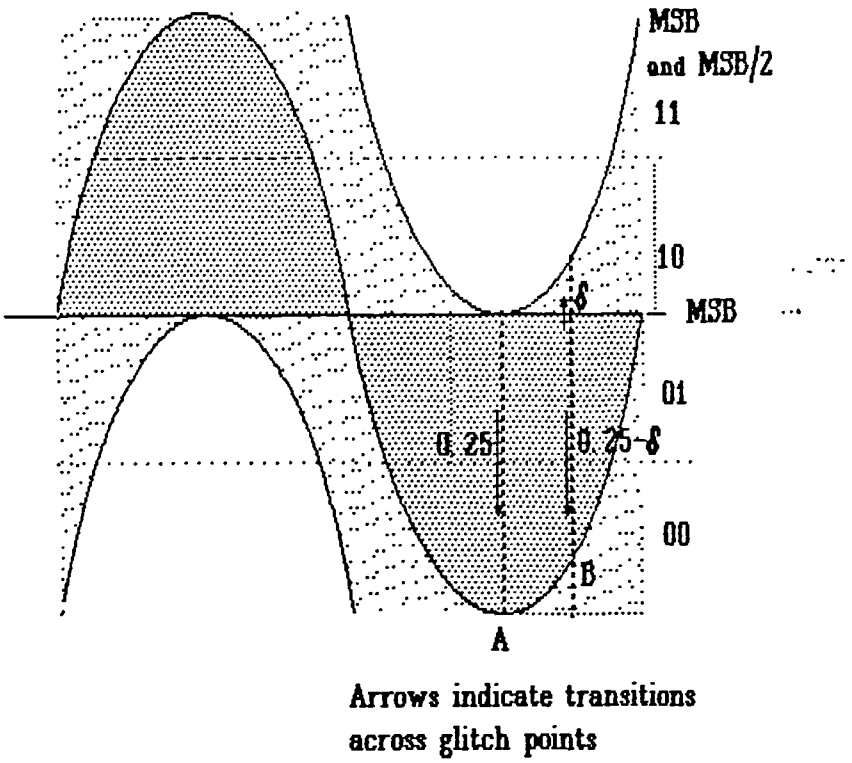


Fig 8.26 Probability of MSB/2 transitions with DAC decorrelation

In fig 8.26 this corresponds to a new point **B**. Transitions from MSB/2=1 in the upper quarter to MSB/2 = 0 in the lower quarter are reduced by δ, where δ is the ratio of the distance below the sine curve at **B** to half the DAC range. This will be offset by the number of transitions from the second quarter, MSB/2 = 0 to the third quarter MSB/2 = 1 which will be δ. The probability of a MSB/2 transition will therefore remain constant. When the DDS output moves above the lower MSB/2 point, the loss in lower MSB/2 transitions are replaced by upper MSB/2 transitions. Effectively, MSB/2 transition probability remains unchanged at 0.25 throughout the cycle resulting in a base spectrum containing a DC component only. The same criteria apply to lesser transitions.

8.6.3.3 MSB glitches

In many DAC implementations, the major transition is at MSB. The analysis commenced for the undecorrelated case will now be extended to include dynamic glitches. Although a similar analysis can be performed as for the static case, the width of the error pulse must be modified. In the static case a particular error E_{error} occurs for a particular DAC output level. In the dynamic case, however, the error occurs on a transition across the MSB boundary. Rather than be determined from the static DAC level width, the error is therefore determined by the clock period. Effectively, the error pulse window, as shown in fig 8.24a above becomes such that:-

$$m' = \frac{f_{out}}{2\pi f_{clock}} \quad \text{.....radians} \tag{8.38}$$

Pulse width modification becomes necessary because the base spectrum appears as if there are many error pulses rather than a single error pulse as represented by equation (8.29). The DAC levels over a window m' show an identical error due to the transition glitch. This pulse must therefore be represented as being the width of one clock cycle rather than one quantisation bit as with the static case. Inserting the modified pulse width m' into the series for the DAC error primary spectrum in phase space T (equation 8.33):-

$$E_{series} = \frac{E_{dynerror}}{\pi} \sum_{n=0}^{\infty} \frac{1}{n} \text{Sin } n\frac{1}{m'} \cos(nT) \tag{8.42}$$

where $E_{dynerror}$ represents the dynamic errors introduced due to the glitch. The error spectrum is a slowly declining series. As with the static case, spurious signals will abound. In addition the lower order spurious signal levels will be at much higher levels than with the static case due to a reduced effective value of m.

MSB glitch contributions will now be determined on the assumption that DAC decorrelation is invoked. The probability of an MSB transition is calculated from fig 8.27. The probability is zero at the peak and trough of the output waveform, but rises as a function of the upper bound of the probability distribution.

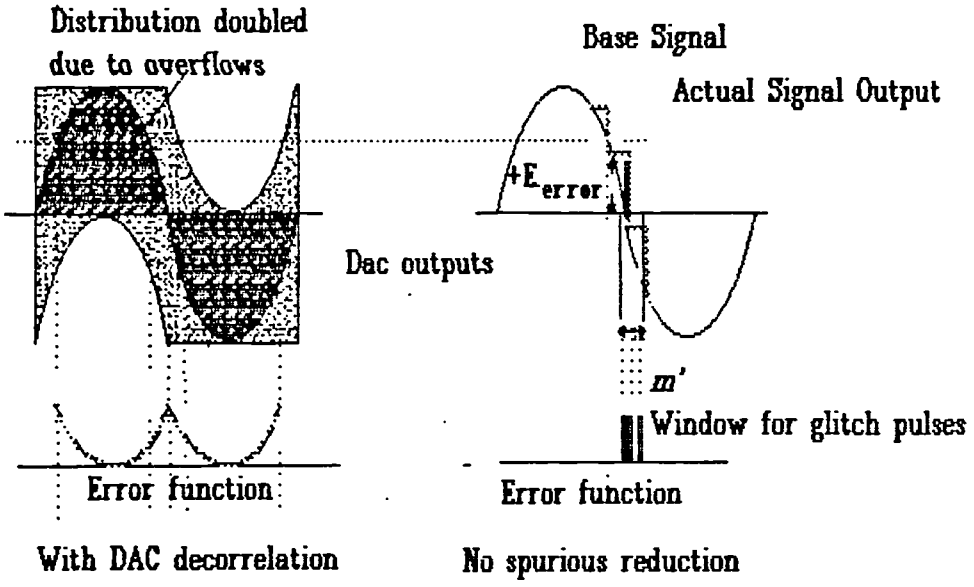


Fig 8.27 Probability distribution of DAC values due to MSB glitches

The upper bound takes the form:-

$$E_{pulse} = 1\text{-}\sin T \tag{8.43}$$

The distribution of transitions across the MSB boundary becomes therefore:-

$$B_y = \frac{1}{4}(1\text{-}\sin^2 T) \tag{8.44}$$

In order to find the level of the error component due to glitches, the amplitude of the glitch must be found besides the distribution. There are two possible relationships between the DAC destination level (determined by the amplitude of the transition across the MSB boundary) and the glitch amplitude: constant and proportional to the transition. The former case is assumed to apply for cases of clock feedthrough, switching spike feedthrough, and digital signal feedthrough; the latter case is assumed to apply for a glitch contribution from current source mismatch.

8.6.3.4 Constant glitch level

If the glitch level is assumed constant, the glitch error E'_{error} can be determined from equation 8.44 to be:-

$$E'_{error} = E_{glitch} f_{ref} \left(\frac{1}{4} + \frac{\mathrm{Sin}^2 T}{4}\right) \tag{8.44a}$$

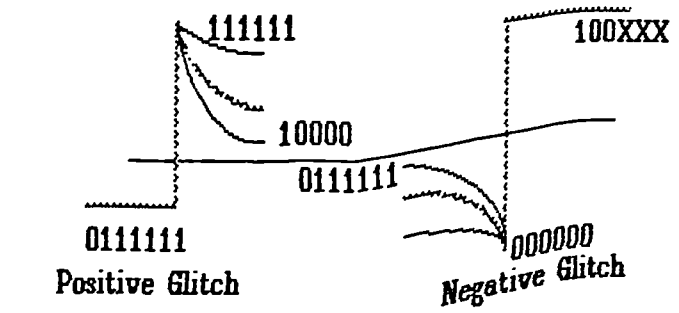
Where E_{glitch} is the glitch energy in volts seconds. By the use of trigonometric identities, the above can be rearranged to give:-

$$E'_{error} = E_{glitch} f_{ref} \frac{1}{8} (1 + \mathrm{Cos}(2T)) \tag{8.44b}$$

The most striking feature of this is that the error function consists of a DC level and the second harmonic only. If DAC decorrelation is not used, the error function consists of a series of harmonic terms.

8.6.3.5 Switching mismatch glitch errors

Fig 8.28 shows the effect of DAC decorrelation on glitch errors due to mismatches in the current source switching. The contribution of a glitch to the output depends upon the particular transition. Assuming that the non-linear component of the glitch is an impulse equal to an MSB in height, the actual contribution of the glitch to the error function can be calculated. In this case a linear relationship between the destination DAC level and the glitch height would be upheld. According to fig 8.28 it is possible for either the MSB switch to occur before the LSBs turn off, or vice versa. In the former case a positive glitch would occur, or in the latter case a negative glitch. With a negative glitch, the lower the starting point, the lower the glitch level.



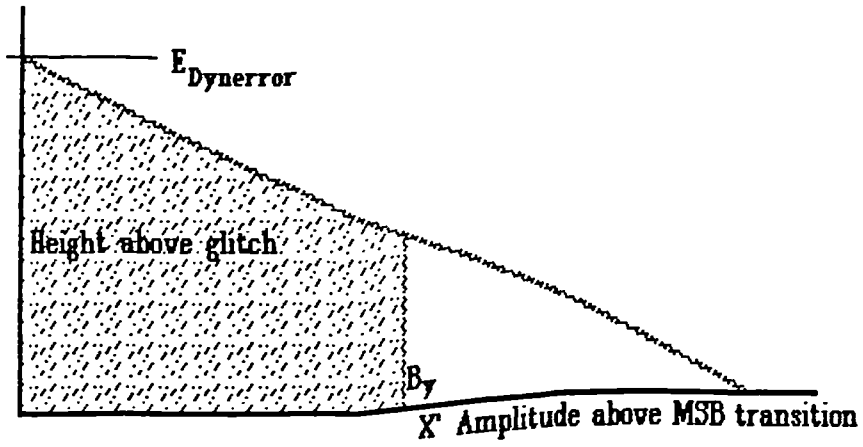


Fig 8.28 Effect of DAC output transitions on the glitch level

On the other hand, a positive glitch is reduced on increased level of DAC destination address. If the contribution of the glitch to errors is $E_{dynerror}$ then the actual error introduced as a function of DAC destination level is:-

$$E'_{error} = 1\text{-}x' \tag{8.45}$$

The total contributions of glitches to the spurious error function as a function of boundary B_y is the area under this curve as shown hashed in fig 8.28:-

$$E'_{error} = E_{dynerror}\int_0^{B_y} 1\text{-}x'dx' \tag{8.46}$$

This results in:-

$$E'_{error} = E_{dynerror}\left(B_y\text{-}\frac{B_y^2}{2}\right) \tag{8.47}$$

Substituting equation (8.44) above into this gives:-

$$E'_{error} = E_{glitch}f_{ref}\left(\frac{1}{4}(1 - \mathrm{Sin}^2T) - \frac{1}{32}(1 - \mathrm{Sin}^2T)^2\right) \tag{8.48}$$

By the use of trigonometric identities, the above can be rearranged to give:-

$$E'_{error} = E_{glitch} f_{ref} \left(\frac{7}{64} + \frac{7}{64} \text{Cos}(2T) - \frac{1}{256} \cos(4T) \right) \qquad (8.49)$$

In this case there is a much smaller fourth order term present.

8.6.4 Comparison of calculated spurious levels

It is instructive to compare the level of spurious signals for the cases of output of one third clock frequency, $f_{Clock}/3$ and one fifth clock frequency $f_{Clock}/5$. With no decorrelation applied, the error waveform can be shown from equation 8.42 to be:-

$$E_{series} = \frac{E_{glitch} f_{ref}}{\pi} \sum_{n=0}^{\infty} \frac{1}{n} \text{Sin } n\frac{1}{m} \cos(nT) \qquad (8.49a)$$

In the following examples, a typical high speed DAC is assumed with a glitch energy of 100psV. and 100MHz clock frequency.

Output of one third clock frequency

In this case, the second harmonic product is calculated from equations (8.42) and (8.49). The spurious level would be:-

Error spur =	-57dBc	DDS
Error spur =	-58dBc	DAC decorrelation technique, Clock or dig feedthrough
Error spur =	-59.2dBc	DAC decorrelation technique, switching mismatch

Total spurious suppression 1dB.

Output of one fifth clock frequency

For the case of 1/5 of the clock frequency, the following spurious levels would be calculated:-

Error spur =	-62.4dBc	DDS

Error spur =	-∞dBc	DAC decorrelation technique, Clock or dig feedthrough
Error spur =	-88dBc	DAC decorrelation technique, switching mismatch

Total spurious either 25 dB or absolute depending upon the source of the errors.

With the second order product, the above calculations show little change to the level of spurious signals, but in practice with the unmodified DDS there will be additional contributions to the second order product from other major transitions; such contributions will be absent when the spurious reduction techniques are used. For higher order products the above equations predict large reductions in spurious signal levels from glitches as a result of the use of such techniques.

8.7 Summary of spurious reduction techniques

In summary, a fundamental principle behind the DAC decorrelation technique is the broadening of the errors in the sampled time domain by a random signal. These lead to a corresponding contraction of spurious signals in the frequency domain. This means that the spurious signals are concentrated in the fundamental (wanted) signal and lower harmonics, thus giving a drastic reduction in the levels of higher harmonics. Two methods of DAC decorrelation have been studied and are the subject of a patent application (Wilson, 1990). These techniques involve the use of two DACs, each DAC providing a randomly varying contribution to the analogue output. The second technique allowing overflows provides a much improved spurious reduction capacity.

In addition to the decorrelation of the DACs to improve DAC related errors, the question of improving truncation spurious errors by means of interpolative dither was investigated. A disadvantage of these techniques is the increase in broadband noise level, but the levels are sufficiently low for satellite data communications usage. As clock frequencies are increased, a reduction in noise density should occur as the noise energy is spread over a broader frequency range. For this technique to be economically viable, however the extra logic required must be integrated in the form of a custom IC or a Logic Array. Having demonstrated that the spurious reduction techniques are theoretically viable, computer simulations are presented in §8.9, followed by details of the construction of an experimental synthesiser and measured results in §8.11.

8.8 Other applications

There are possibilities for extending the basic principle of this invention outside the field of frequency synthesis. The reduction of harmonic and other spurious products could be applied to many systems that employ DACS and ADCs. One particular application could be in pulse doppler radar digitizers where correlation of spurious products close to the wanted signal could obscure small targets close to a reflection from a large target. In audio work, the human ear finds a preponderance of high order spurious products much more disturbing than broadband noise. Therefore a potential exists to reduce impairments in the quality of sound processed by ADCs and DACs in digital audio equipment. Other examples where this technique could be useful include instrumentation and video applications.

8.9 Simulation work for DDS

8.9.1 The requirement for simulation

Since there are many distortion generating processes involved in Direct Digital Synthesis, a simulation would be a most suitable means of predicting expected performance. The situation is complicated by the fact that there are many possible output frequencies, each with a unique spectrum. In order to gain confidence in a proposed implementation it is necessary to investigate each channel over the band of interest. A simulation would be required to search through each channel and record the worst case performance obtained.

8.9.2 Fast Fourier Transform

8.9.2.1 Using FFT to obtain the DDS spectrum

A principal part of a simulation for a DDS consists of a time domain simulation of the waveform construction followed by a conversion to the frequency domain to observe the resultant frequency spectrum. Since the synthesis process is equivalent to a reconstruction of a sampled sinewave, a Fast Fourier Transform (FFT) is a most effective means of analysis. From chapter 4, it was indicated that the longest cycle of repetition is 2^p clock cycles. The synthesiser is therefore clocked through 2^p clock cycles, where p is the accumulator width. From the repetition rate, the lowest spurious frequency will be

$F_{clock}/2^P$. Therefore, in order to resolve individual spurious products, the FFT size should be 2^P.

If 2^P are taken, one for each clock cycle, FFT processing gives an output point corresponding to each possible output channel frequency of the synthesiser. From consideration of the data that must be accurately resolved, that is discrete spurious frequencies, it is desirable that synthesiser operations repeat exactly at a rate equal to the reciprocal of FFT width. In this case no FFT overlapping, or windowing would be required. Fig 8.29 displays the situation with no overlapping. The bars represent the possible outputs from the DDS, and the curve the response of the FFT process. Each DDS output corresponds to a peak in the FFT channel response, but is at the nulls of each of its neighbours. It follows that a single FFT sample can then be taken of a complete DDS cycle, and the results will accurately represent the DDS output spectrum. The disadvantage of this method is that large FFTs are required (64kpoints for 16 bit DDS, and $4*10^9$ for 32 bit DDS). For the 16 bit case, the size is manageable, but presents an insuperable problem for the 32 case. However, the 16 bit case can be treated as a subset of the 32 bit case, and the 16 bit case will be used in the study.

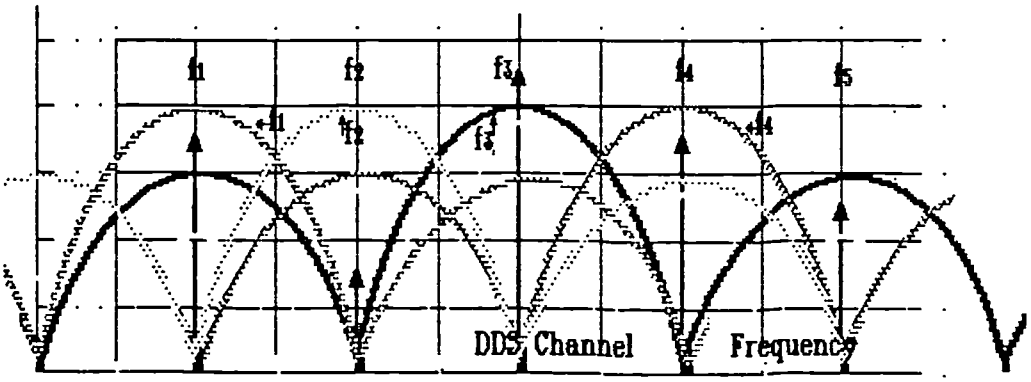


Fig 8.29 Response of non-overlapped FFT to DDS spurious signals

8.9.2.2 FFT Algorithm

The FFT is a discrete Fourier Transform (DFT) with the redundant steps removed. There is an abundance of literature on the treatment of FFTs, therefore only a brief description will be given here. The DFT can be represented by [Rabiner-Gold, 1975a]:-

$$X(k) = \sum_{n=0}^{n=N-1} x(n)W^{nk} \qquad (8.50)$$

where X(k) is the output in the frequency domain and x(n) is the nth input sample in the time domain, where:-

$$W^{nk} = e^{-j\left(\frac{2\pi}{N}\right)nk} \tag{8.51}$$

The FFT removes the repeating terms in W^{nk}. A full DFT can be split into two smaller DFTs, one operating on the even terms on the input and one on the odd terms:-

$$X(k) = \sum_{n=0}^{n=N/2-1} x(2n)W^{2nk} + \sum_{n=0}^{n=N/2-1} x(2n+1)W^{(2n+1)k} \tag{8.52}$$

This involves a 50% reduction in computations over a full DFT. Each of these DFTs can in turn be reduced into smaller DFTs. Putting W_N^2 equal to $W_{N/2}$ equation 8.52 can be written as:-

$$X(k) = \sum_{n=0}^{n=N/2-1} x_1(n)W_{N/2}^{n\,k} + W_N^k \sum_{n=0}^{n=N/2-1} x_2 W_{N/2}^{n\,k} \tag{8.53}$$

The DFT output X(k) can be written therefore in terms of two smaller DFTs X(1) and X(2):-

$$X(k) = X_1(k) + W_N^k \;\; X_2(k) \qquad 0 \le k \le \frac{N}{2} - 1 \tag{8.54}$$

or:-

$$X(k) = X_1(k-\tfrac{N}{2}) + W_N^k \;\; X_2(k-\tfrac{N}{2}) \qquad \frac{N}{2} \le k \le N - 1 \tag{8.55}$$

This process can be iterated until it arrives at a starting point of N/2 2-input DFTs.

8.9.2.3 FFT program design

With the 16 bit case, a large data memory must be managed, therefore special program techniques must be used for optimum performance. The design is based on that used by Cooley and Welch [Cooley, Lewis, Welch, 1969].

The machine to be used was based on an IBM PS2 using a 33MHz 80386 microprocessor, and Pascal used as the top level design language. The following facts had to be taken into account in the design of the program:-

1) The machine can only perform high speed memory access from a limited cache memory storage (32kbyte);

2) The core of the FFT process (the butterfly) is performed more efficiently by ensuring parallelism between the 80386 and its 80387 numeric co-processor unit.

The program is designed to allow restricted access to the memory at any one instant.

To enable effective parallelism, the butterfly is written in 80386 and 80387 assembly code, and subsequently inserted as a subroutine into the main Pascal code. Using this approach, an FFT program was produced by the author that performed a 256kpoint FFT in 61 seconds. Fig8.30 displays a data flow diagram of the FFT process.

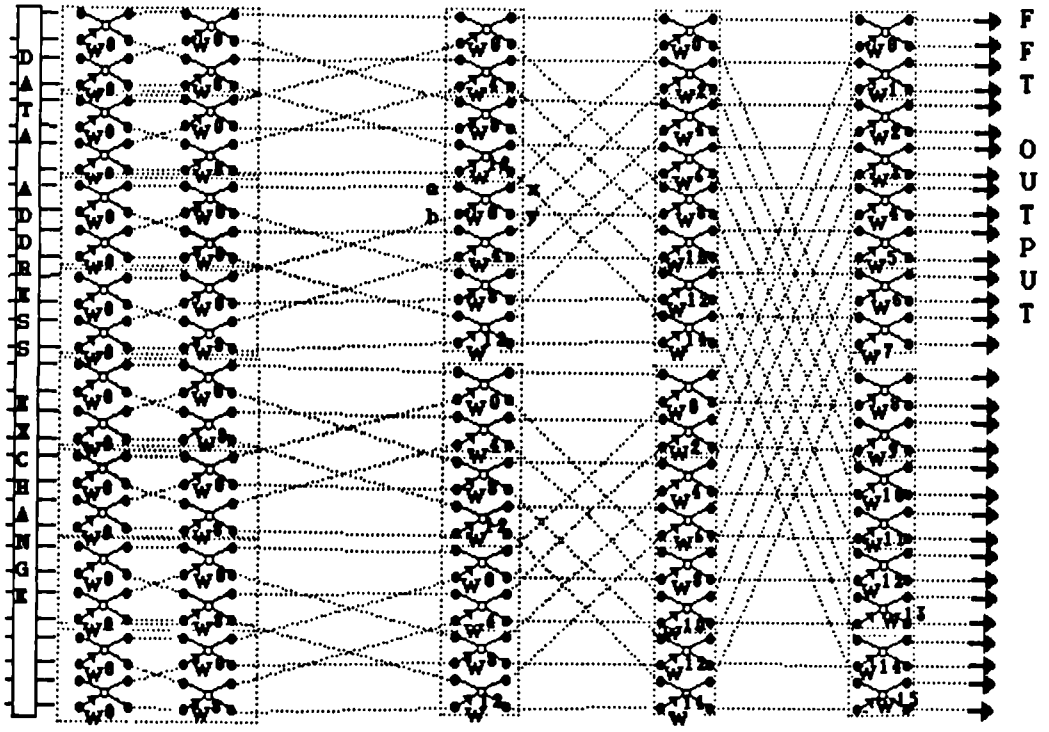


Fig8.30 Data flow diagram for the particular implementation of a FFT used here, the dotted borders indicate memory cacheing

The first operation, at the top of the diagram is the bit shuffling operation that arranges the data in correct order for the decimation in time algorithm. Bit shuffling is the name given to the process where an address of an time domain point is bit reversed, and the data is moved to a location pointed to by the bit reversed address. A procedure was written by the author that performed bit-wise operations on the memory address. The bit reversing is implemented in assembler code by testing each bit and re-writing the bit in reverse order. A method developed by Radar [1968] is considerably more efficient, but was not implemented as the overall time saving would be minimal (less than 1 second out of 61 for a 250k FFT). Bit shuffling of addresses is necessary to ensure that the frequency domain data appears in the correct order. The data is initially arranged in blocks of 2048 point FFTs, as can be observed from fig 8.30 (shown here as 4 point FFTs for clarity). This means that the processor has instantaneous access to only 16kbyte of data if single precision numbers are used in the data. When the decimation block becomes greater than 2 kbyte, then the block is split as can be observed from the RHS of fig 8.30. Storage of

coefficients W_n after use in the butterfly must be achieved so they can be reused in subsequent blocks.

A critical path analysis of the FFT process reveals that the butterfly is by far the slowest step in the process. This in effect contains most of the numeric processing. A flow diagram of the butterfly is given in fig8.31.

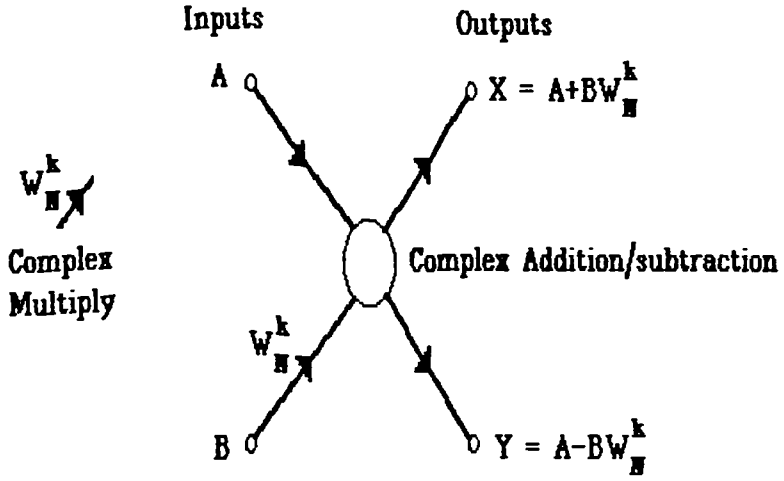


Fig 8.31 Data flow diagram for the FFT butterfly

The only other non-trivial numeric processing is the principal root of unity W_N^1 . As this is evaluated only $\log_2(N)$ times, for moderate to large N, W_N^1 is well outside the critical path. The 80387 processor is arranged to be continuously engaged in numeric processing, while the 80386 simultaneously manages memory and program flow. Fig 8.32 displays the data flow diagram of the 80387 processing of the butterfly.

Efficient butterfly processing could be achieved by using the 80387 stack as a scratchpad for intermediate results. 8 stack registers are present within the 80387 which can be accessed more rapidly than the memory. Numbers are given on the data flow diagram which indicate stack usage. Fig8.32 is the flow diagram that was produced prior to the assembly code to minimise the number of operations required in the butterfly process.

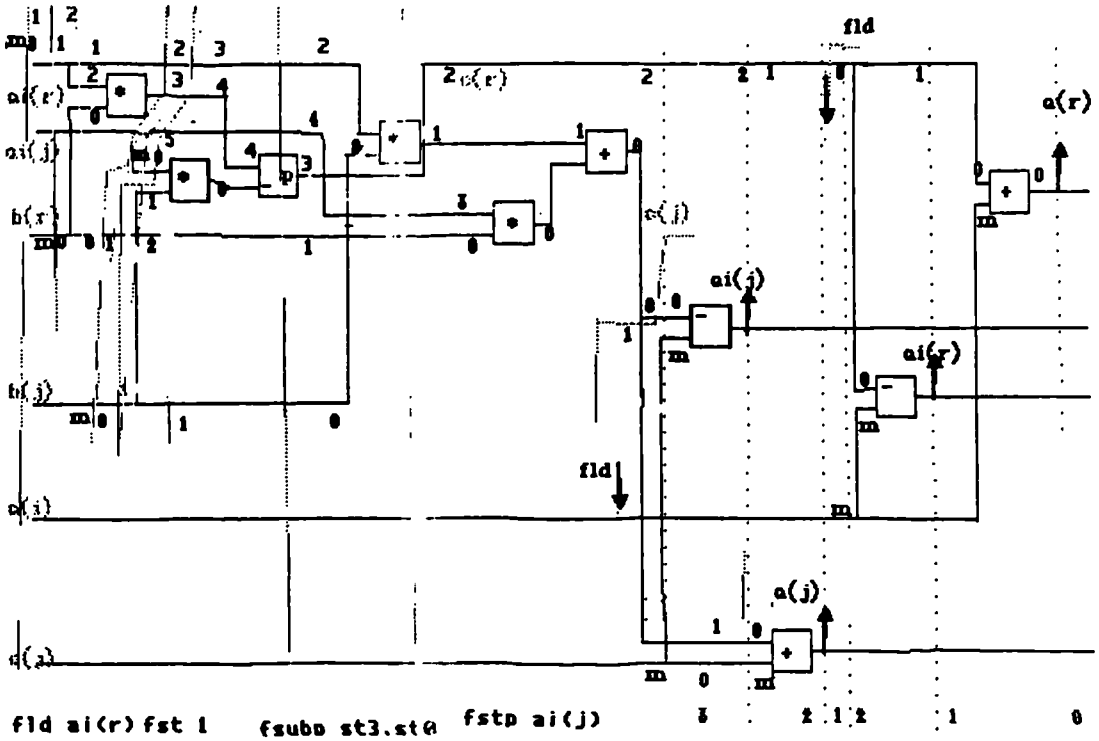


Fig 8.32 Data flow and stack utilisation diagram for the FFT butterfly using the 80387 numerics coprocessor IC.

8.9.2.4 Accuracy

There is a trade off between processing speed, memory usage and accuracy. The formula for accuracy is (Rabiner-Gold, 1975b):-

$$\text{error}/C = \sqrt{N}2^{-b}(0.3)\sqrt{8} \tag{8.56}$$

where b is the number of bits resolution. Error/C is the ratio of RMS error to RMS full scale signal. A single precision IEEE number has 24 bits precision for the mantissa. For a FFT size of 256k an effective signal to noise ratio of -104dB results, ignoring any round off effects in the W_N^k multiplier coefficients. If there is a round effect here due to single precision then there will be negligible additional degradation because this factor is only used once per butterfly. However, if the principal root W_N^1 is made single precision, this will be effectively multiplied many times, the build up in roundoff errors would be catastrophic. Therefore double precision numbers are used for this as there is negligible penalty in storage or speed for this factor.

8.9.3 FFT Response to Noise

In order to establish the noise density present at the output of the simulated synthesiser the response of the FFT to noise must be known. Each output channel of the FFT is often

referred to as a "bucket". As mentioned in §8.9.2.1 non overlapping FFTs will be performed. Fig 8.29 of this chapter, §8.9.2.1, displays the response of the FFT "buckets" to noise. The output of the FFT to noise is represented by a power integration to infinity under this curve. Since with noise it is not important that some of the output may have originated from other output buckets, the aliasing is not considered a problem. The form of the rectangular window response is given by:-

$$E_{pulse} = \frac{\sin(\pi f)}{\pi f} \tag{8.57}$$

The power integration is given by:-

$$E_{pulse} = \int_0^{\infty} \frac{\sin^2(\pi f)}{\pi^2 f^2} df = \frac{1}{2} \tag{8.58}$$

This represents only one half of the response, therefore the bandwidth conversion factor for a rectangular window in this case is unity.

8.9.4 Simulation of DDS, truncation effects only

The program details for the DDS simulation is given in appendix 3. Simulation of the DDS is straightforward if truncation effects only are studied. As with a real look up table DDS the look up table is calculated upon starting the program. Addressing of the look up table is achieved by an integer having a maximum value 2^q, where q is the phase word. Phase truncation is therefore represented by the value of q. The output of the look up table is restricted to values of 2^m where m is the resolution of the DAC (amplitude truncation). The look up table is represented by the following:-

$$V_{out} = 0.5+(2^p-2)\left(0.5+0.5\cos\left(\frac{2\pi T}{2^q}\right)\right) \tag{8.59}$$

where V_{out} represents the synthesiser output voltage and T the phase input word value to the table. Voltage levels for each time sample are stored in memory in a file. After the simulation processing, an FFT is performed on the file, and the results displayed in a spectrum analyser type logarithmic display. The vertical axis used in the display is given by:-

$$V_{out} = 10\log_{10}(x^2+y^2) \tag{8.60}$$

where $V_{FFT} = x + jy$.

The output is approximately valid up to the Nyquist frequency, but as the upper half of the spectrum is exactly the mirror image of the lower half, this region is never plotted.

8.9.5 Truncation plus dither

To the simulation program above, a dither word D is added to the phase input word. In addition, rounding is controlled by a random number. The source of the random numbers is the pseudo random number generator used in the Pascal program. Dither application is equivalent to phase modulation with a random signal. This phase word is of maximum value $2d$ where d is the number of bits of the word. The phase and amplitude dither are provided from separate random numbers.

Amplitude dither is provided by random rounding of the output of the look-up table according to a pseudo-random binary sequence. The look-up table is rounded down if the sequence is zero, or up if the sequence is one.

Phase dither is injected by summation of the dither value to the output of the phase accumulator. An idealised DAC is assumed as in §8.9.4.

8.9.6 DAC simulation

Although simulation of the DDS is simple, the same cannot be said for simulation of DACs. Intermodulation effects within DACs are complicated and have many sources [Personal communication, Basler, 1991]. Therefore, rather than attempting to simulate a particular DAC, a model was built of a perfect DAC and by introducing to this the effects discussed in §8.2, a prediction can be made of possible degradations. The DAC to be simulated was a switched current source [Weiss, 1986]. In the simulation, a weighted current source is switched in for each bit of the DAC input word. The program description and code for the DAC simulation is given in appendix 3. The simulation was split into two parts; static effects and dynamic effects.

8.9.6.1 Static Effects

Static effects are errors introduced by mismatches within current sources. In the simulation, this is represented by a random error component added (or subtracted) to the ideal current for each control bit. In this way, a Monte Carlo simulation of DAC models can be undertaken. Such errors are responsible for INL and DNL in a real DAC. A plot of DAC errors is given in fig 8.33 for this type of error. The standard deviation of the DAC errors was assumed to be LSB/2. A Monte Carlo program generates a simulated production run of DACs. Each DAC is a file consisting of current sources and associated error values.

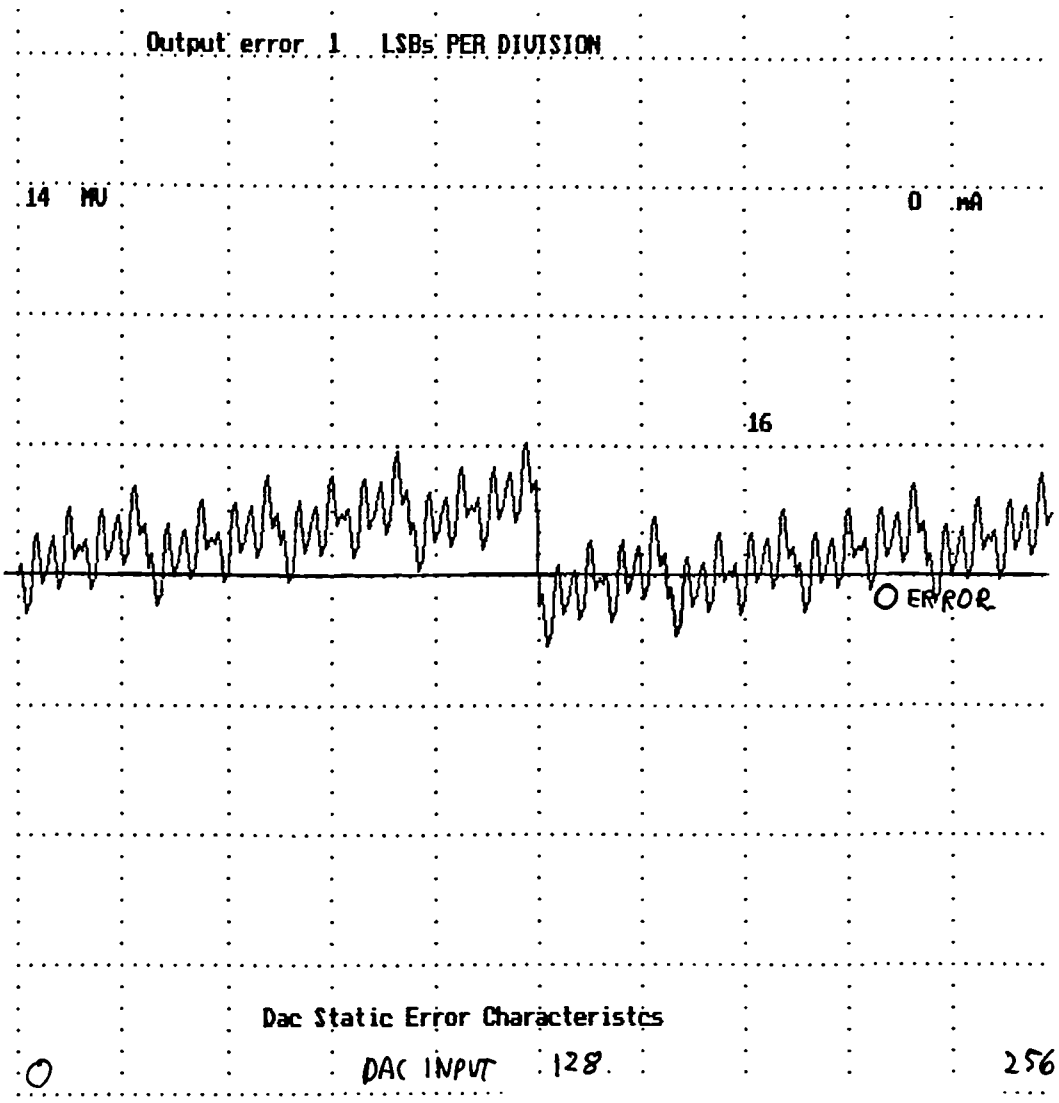


Fig 8.33 DAC static error characteristics

8.9.6.2 Dynamic errors

The situation becomes even more complicated when dynamic factors are considered as is required for a fast DDS simulation. With switching effects, the DAC output is dependent not only upon the present output level, but also upon previous DAC levels. Since the clock period is usually greater than the the DAC settling time, a useful approximation is to consider the present (x(n)) and previous DAC state (x(n-1)), but states previous to this are ignored. Modelling of the switching transient needs to be undertaken. Two aspects to this switching are considered:-

1) Variations in propagation delay;

2) Variations in the switching transient.

For a clocked DAC, the effect of propagation delay will be minimalised, and so the dominant effect considered is the switching transient.

For the simulation, an exponential first order transient is assumed, although in practice the transient is more likely to be second order due to the effect of metalization inductance and diffusion capacitance. The transient for a first order system takes the form:-

$$I_{trans} = (I_0 - I_F)e^{-j\left(\frac{t}{\tau_t}\right)} + I_F \tag{8.61}$$

where τ_t is the time constant of the transient, I_0 is the switched current source initial current, I_F the final current and I_{trans} the current during the transient. These factors are entered into the Monte Carlo analysis to take account of the spread of diffusion characteristics across the chip. A calculated value is required of the average error over one clock period t_p. This error, $\Delta I_{switching}$ will have contributions from the propagation delay t_p and the settling transient:-

$$\Delta I_{switching} = \frac{\int_0^{\infty} (I_0 - I_F)e^{-j\left(\frac{t}{\tau_t}\right)} df + I_0 t_p}{t_{ck}} \tag{8.62}$$

Evaluating this integral gives:-

$$\Delta I_{switching} = \frac{(I_0 - I_F)(t_p + \tau_t)}{t_{ck}} \tag{8.63}$$

A sketch illustrating the nature of this transient is illustrated in fig 8.34. When the DAC is clocked during the simulation, an error current (I_{err}) is added to the static current depending upon the previous value of the current. If the switch was turned off, the output current consists of the error voltage only. If the current source is turned on, the error current is added to the static current. If there is no change in the current then no error component is added. Feedthrough from the other current sources or clock intermodulation is not taken into account in order to simplify the analysis.

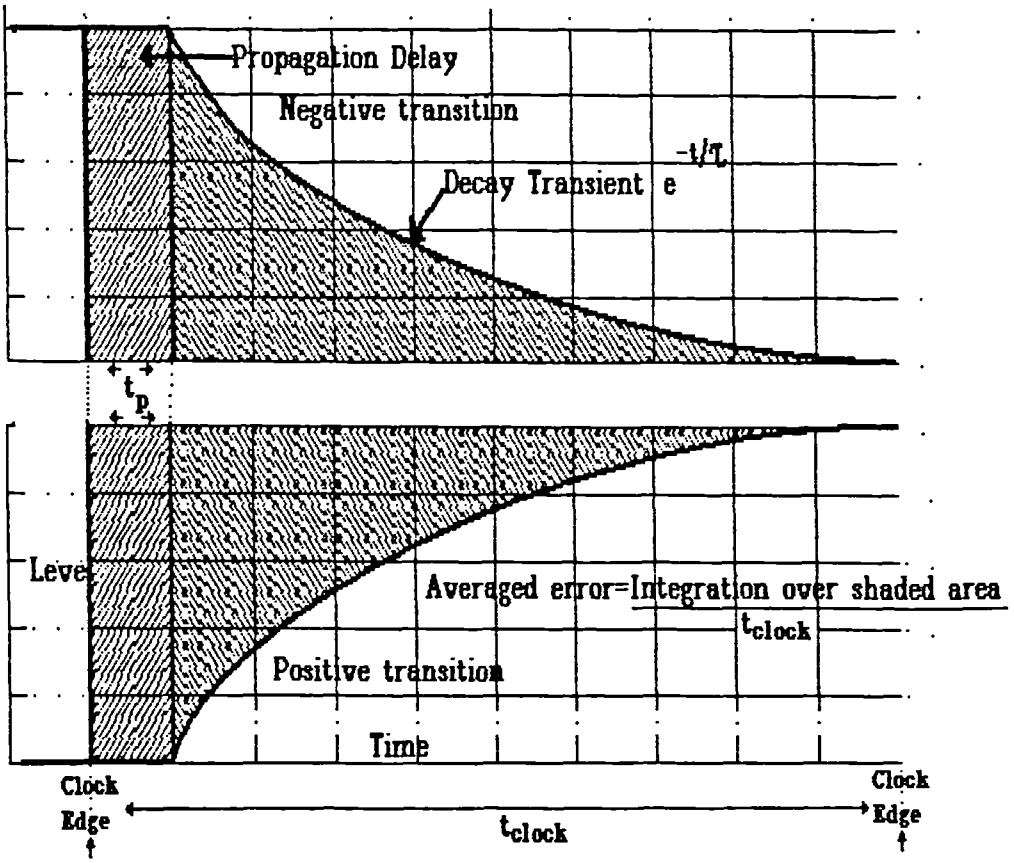


Fig 8.34 Simulated DAC current switch transient

The next component that was considered was digital signal feedthrough. This is modelled by capacitive edge coupling from the digital signals to the current sources. When a digital transition takes place, a component of this is assumed to couple through to each current source, resulting in an error value. This is a very simplified model of the actual problem which can include inter-metalisation coupling in the IC, and cross coupling through the ground and external circuit. The composite DAC current is modelled as:-

$$I_{analogue} = \frac{I_{ref}}{2^P}\left(LSB2^0 + LSB_{+1}2^1 ..... + MSB2^{P-1}\right) \qquad (8.64)$$

which is the idealised model for a DAC.

There will be an error contribution to each bit, as determined by:-

$$I_{per\ bit} = I_{source} + \Delta I_{static} + \Delta I_{switching} + \frac{C_{HL} V_{s+/-}}{t_p} \qquad (8.65)$$

where I_{source} is the switched current source current for the bit, ΔI_{static} is a random value selected from the Monte Carlo process, ΔI\S\DO6(switching) is as defined by equation 8.63 and C_{HL} is the capacitive coupling between the control bits and the analogue coupling for

a high to low control logic swing on the particular DAC input bit. V_s (+/-)is the effective logic voltage swing, and if a low to high logic swing occurs, a different value of coupling capacitance C_{LH} is used in place of C_{HL} in equation 8.65. Different values of $C_{coupling}$ are used depending upon whether a positive or negative logic swing occurs at the input to the DAC. This facility is used to model the effects of spikes from the control logic coupling to the DAC current source switch. The particular values of coupling capacitance used for the two DACs in the DDS simulations of §8.9.9 and §8.10.3 are displayed in table 8.4.

Table 8.4
Digital switching feedthrough capacitances

Capacitance	DAC1	DAC2
C_{LH}	0.13 pF	0.093 pF
C_{HL}	0.2 pF	0.16 pF

The aim of this model was to be representative, rather than accurately model a particular DAC. However, benefits could be gained from modelling clock intermodulation effects in addition, but this is beyond the scope of the thesis. A specification giving DAC characteristics and limits is shown in table 8.5 and this is used as an input to a computer program which provides a Monte Carlo simulated production run of 20 DACs with a Gaussian spread on the various error contributions. Two samples were selected with approximately the standard deviation on all error characteristics. These yielded the worse dynamic linearity characteristics, (fig 8.35) and are used for the spectral plots of the new DDS techniques in this chapter. The time constant and propagation delay have spreads on them that have standard deviations given by the corresponding spreading values in table 8.5

Table 8.5 Simulated DAC specification

DAC Characteristic	Value
Max clock frequency	100 MHz
DAC current mismatch (each bit)	± 0.5 LSB
Digital edge feedthrough capacitance	0.2 pF max
DAC settling time constant	1.1 ns
Settling time constant spread between bits	100 ps
Switch propagation delay spread	600 ps
Glitch energy	156 pVs

8.9.7 Simulation of DAC Decorrelation

In order to simulate of DAC decorrelation effects two DACS are selected from the Monte Carlo production run. These DAC files are then inserted into the DDS with decorrelation simulation program as outlined in appendix 3. The algorithm used in the Decorrelation simulation is exactly as described in §8.4.4. Pseudo random numbers are provided by means of the Pascal pseudo random number generator.

8.9.8 High speed DDS, without spurious reduction

For the simulations described in the remainder of this chapter, a DDS will be studied using the following parameters:-

	Values	Units
Clock frequency	100	MHz
Accumulator size	16	bits
Frequency Word	9356 or	16374
Output Frequency	14.276	MHz

Before carrying out the DDS simulation, the characteristics of the simulated DAC selected from the Monte Carlo process is plotted by a software routine that increments through the DAC characteristic. By incrementing through the digital word at the DAC input, and dividing the DAC output by the ideal value of DAC output corresponding to the input digital word, a DAC linearity curve can be obtained. If the DAC switching effects are ignored, then a plot of INL and DNL is obtained, giving the plot of fig8.33 in §8.9.6.1.

If the DAC is incremented at full clocking speed and switching errors are included, a plot can be obtained of the DAC dynamic characteristic, such a plot is displayed as fig8.35. It can be observed that the linearity is poorer, and that glitches occur as the most significant bits change

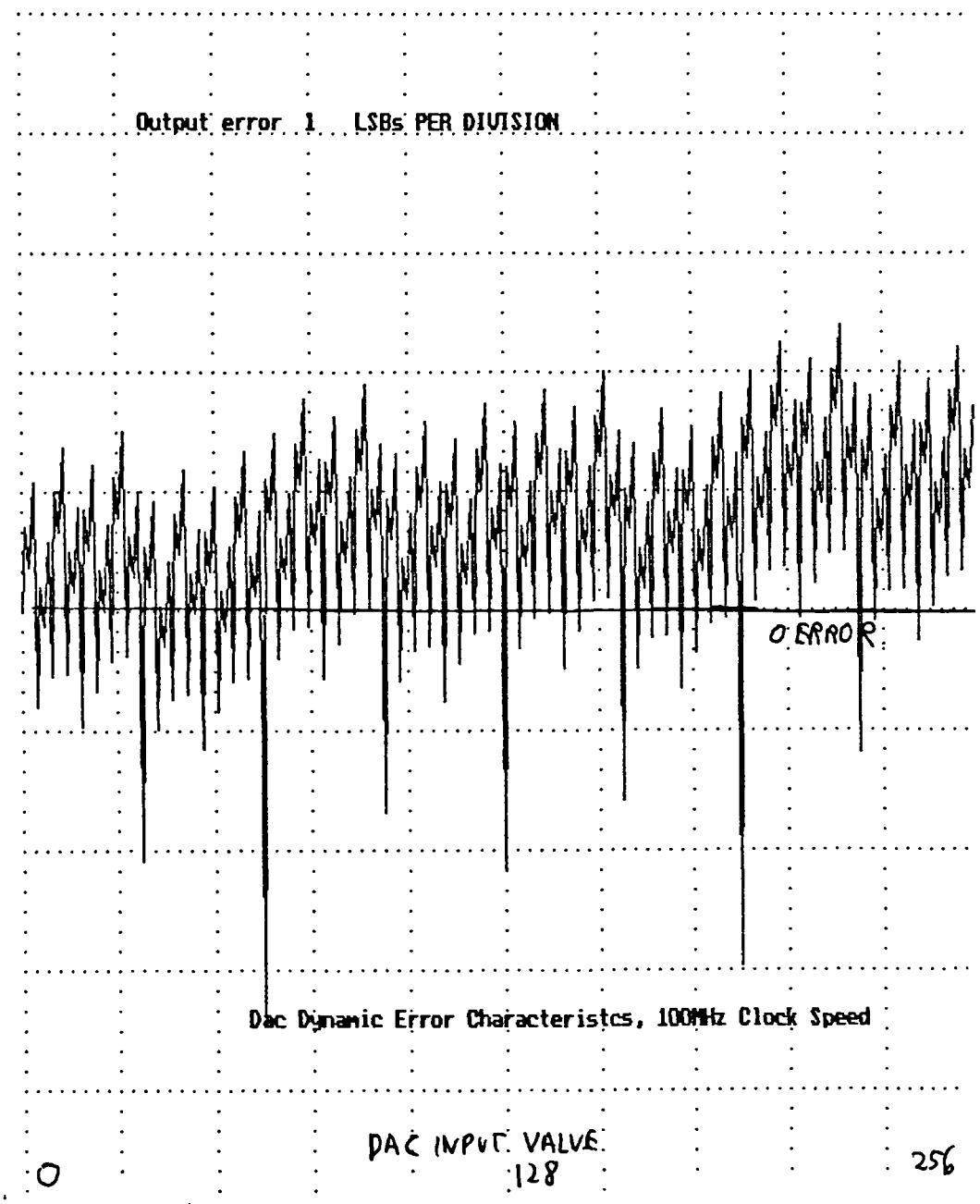


Fig 8.35 DAC dynamic error characteristics at 100MHz

A simulation of a 100MHz synthesiser was performed with no spurious reduction techniques enabled. A FFT of the resulting DAC output can be observed in fig8.36.

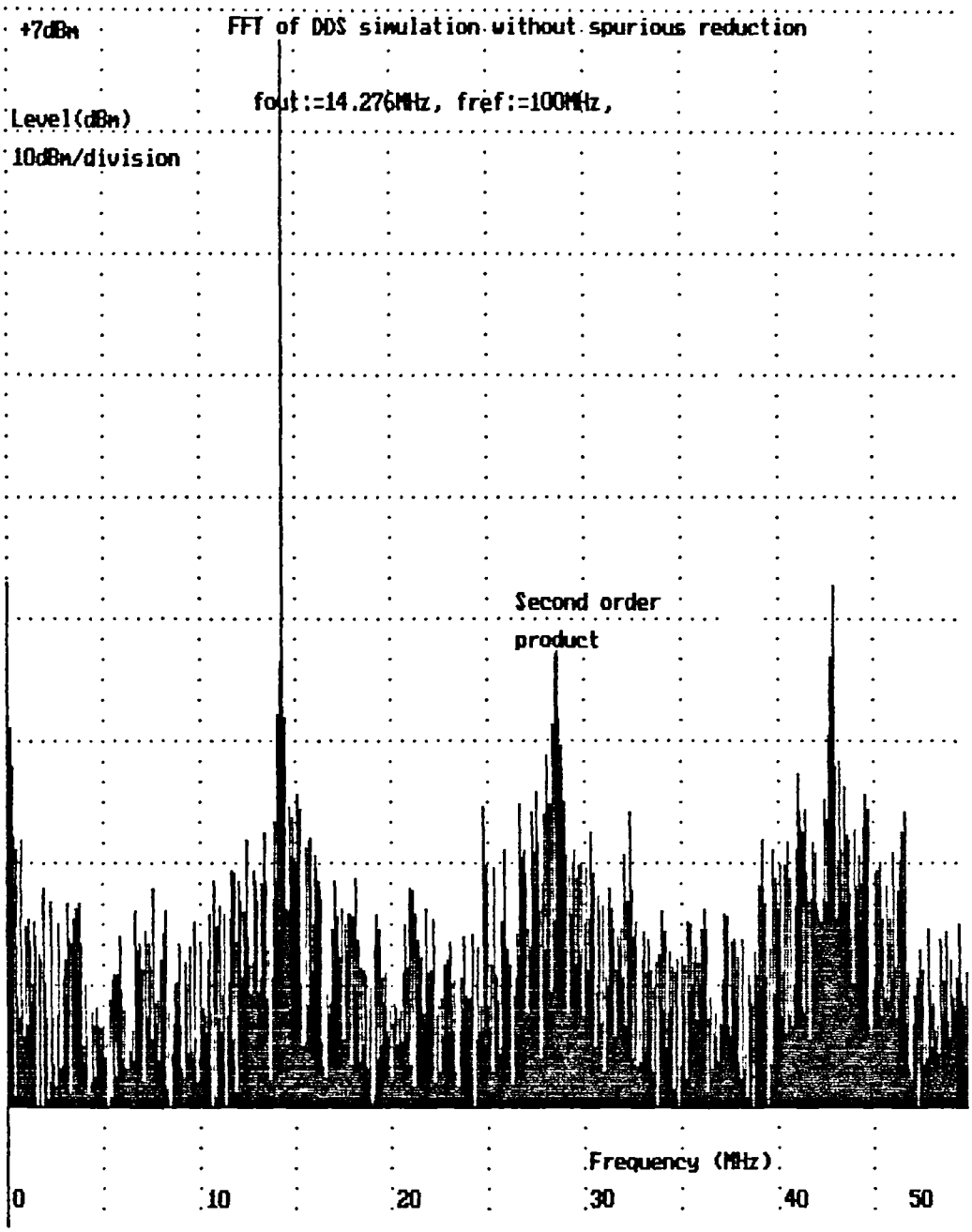


Fig 8.36 Broadband FFT of DDS giving 14.276MHz output

If a perfect DAC is used, and the simulation is repeated, an FFT plot, fig8.37 is obtained, showing the effect of errors due to truncation. The real DAC spectrum of fig8.36 is more typical of high speed synthesisers than the idealised case of fig8.37.

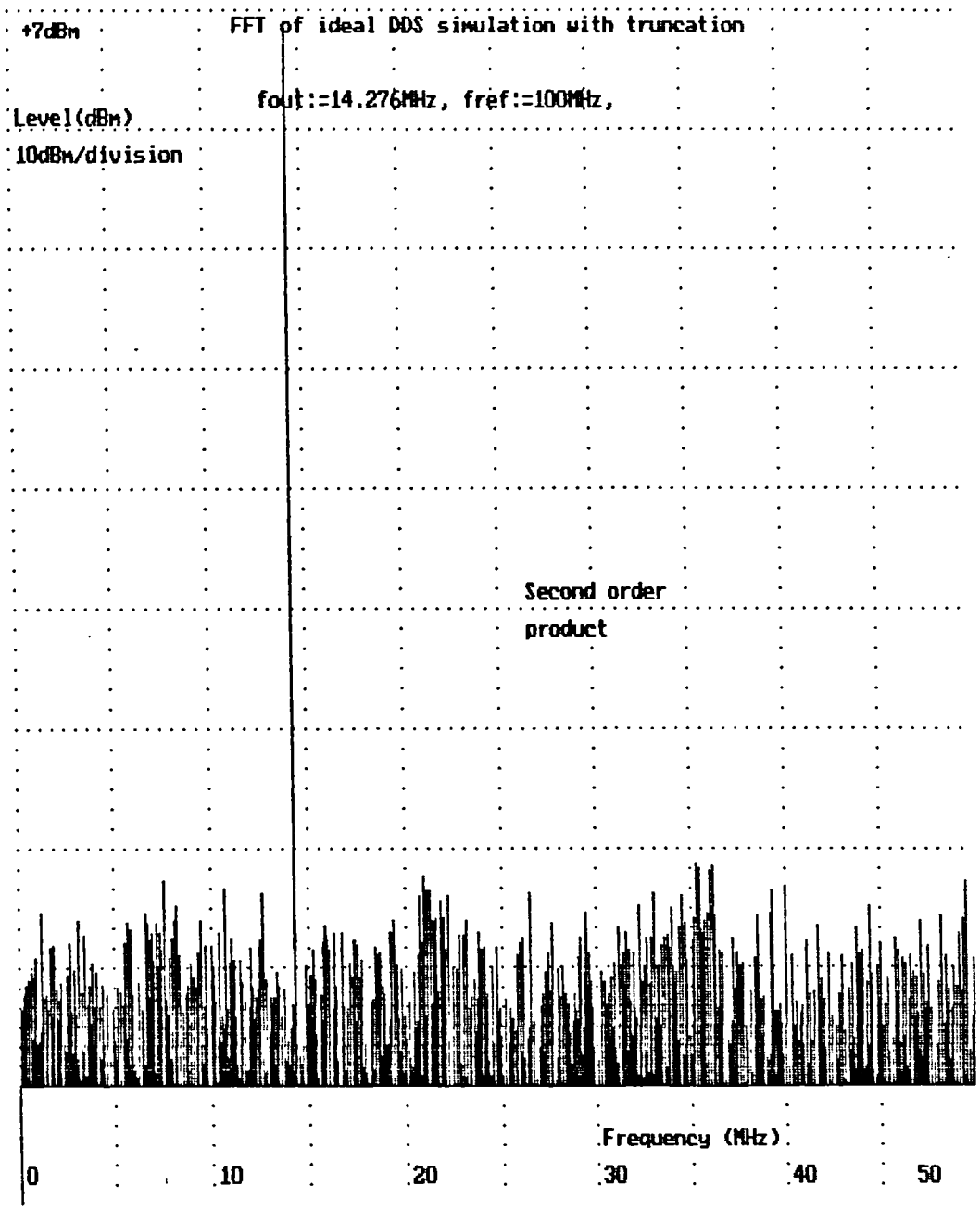


Fig 8.37 Broadband plot, Ideal DDS with truncation

Fig 38 gives a close to carrier plot of the sidebands, and it can be observed that the highest spurious level is -50dBc. Large numbers of high order spurious signals are visible in the broadband plot of fig8.36 up to the Nyquist frequency. Second and third harmonics are also clearly visible.

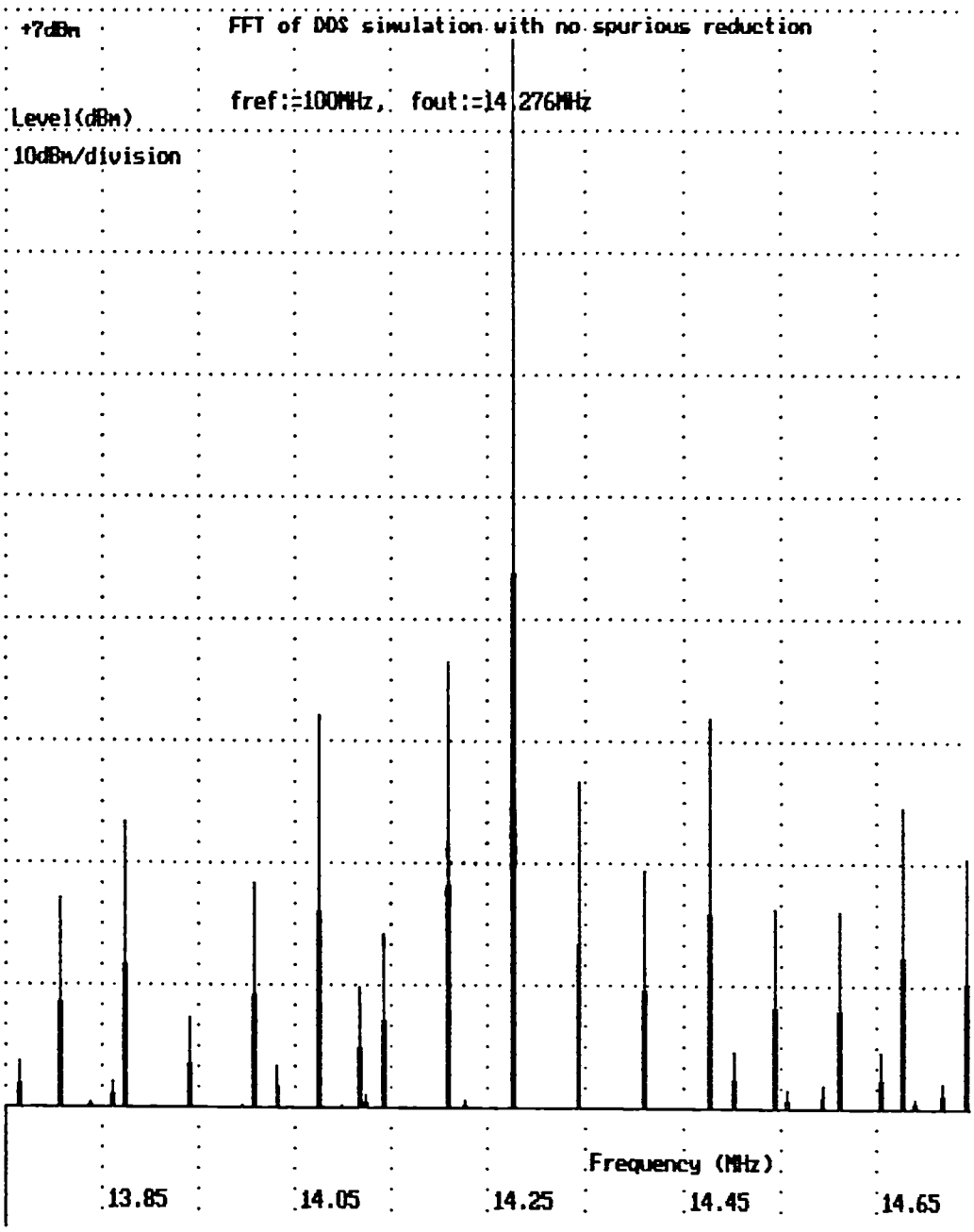


Fig 8.38 Fig 8.36 expanded showing close to carrier region

8.9.9 High speed DDS, including spurious reduction methods

Firstly, a simulation was obtained with the decorrelation but no truncation dither applied. The FFT output is displayed in fig8 39. Spurious level reduction can be clearly observed, but some products are still clearly visible above the noise floor.

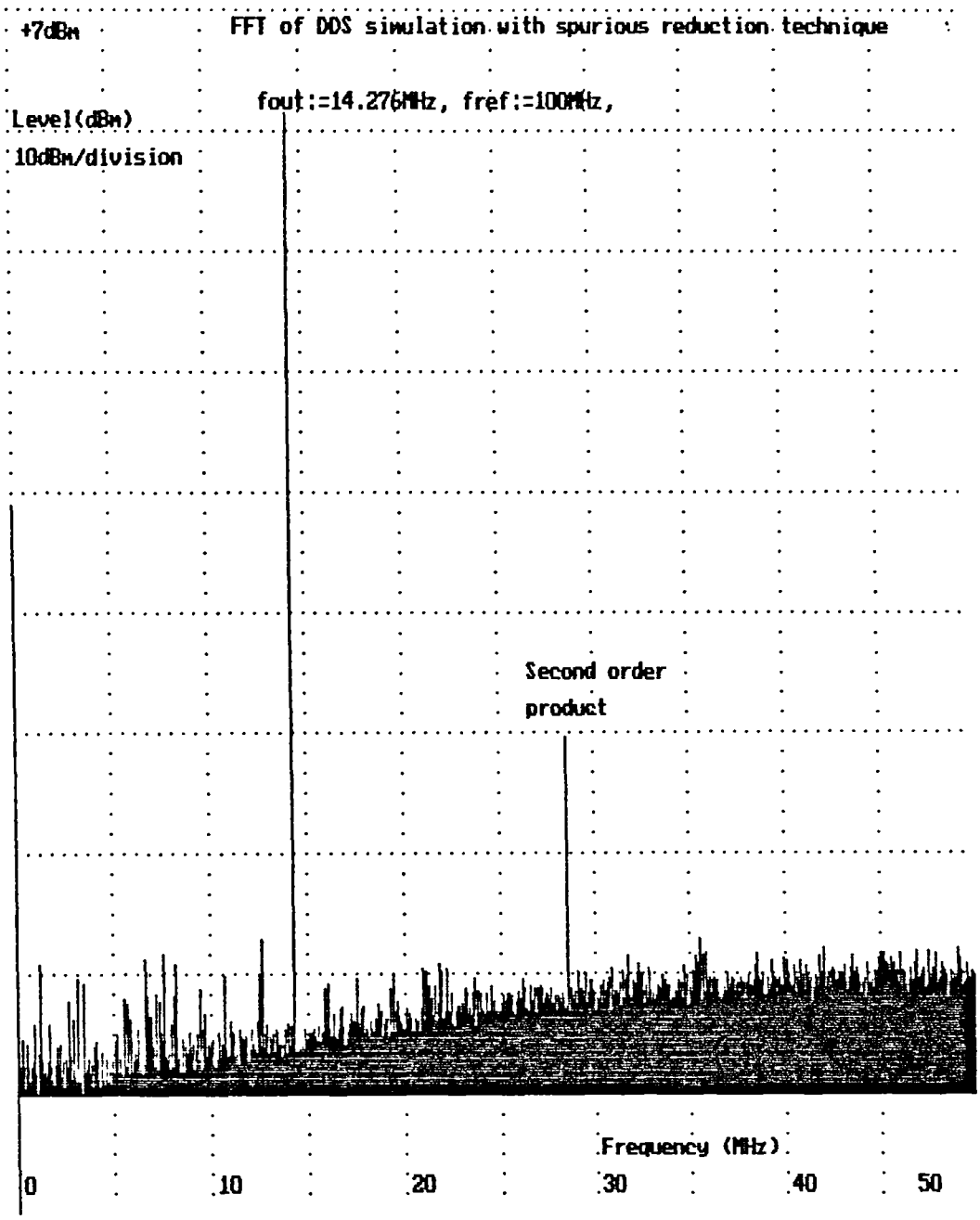


Fig 8.39 Broadband DDS with decorrelation, but no dither

By applying truncation interpolative dither in addition to decorrelation, the spectrum display of fig 8.40 can be obtained. Spurious products can no longer be observed clearly above the noise floor, apart from the second order product.

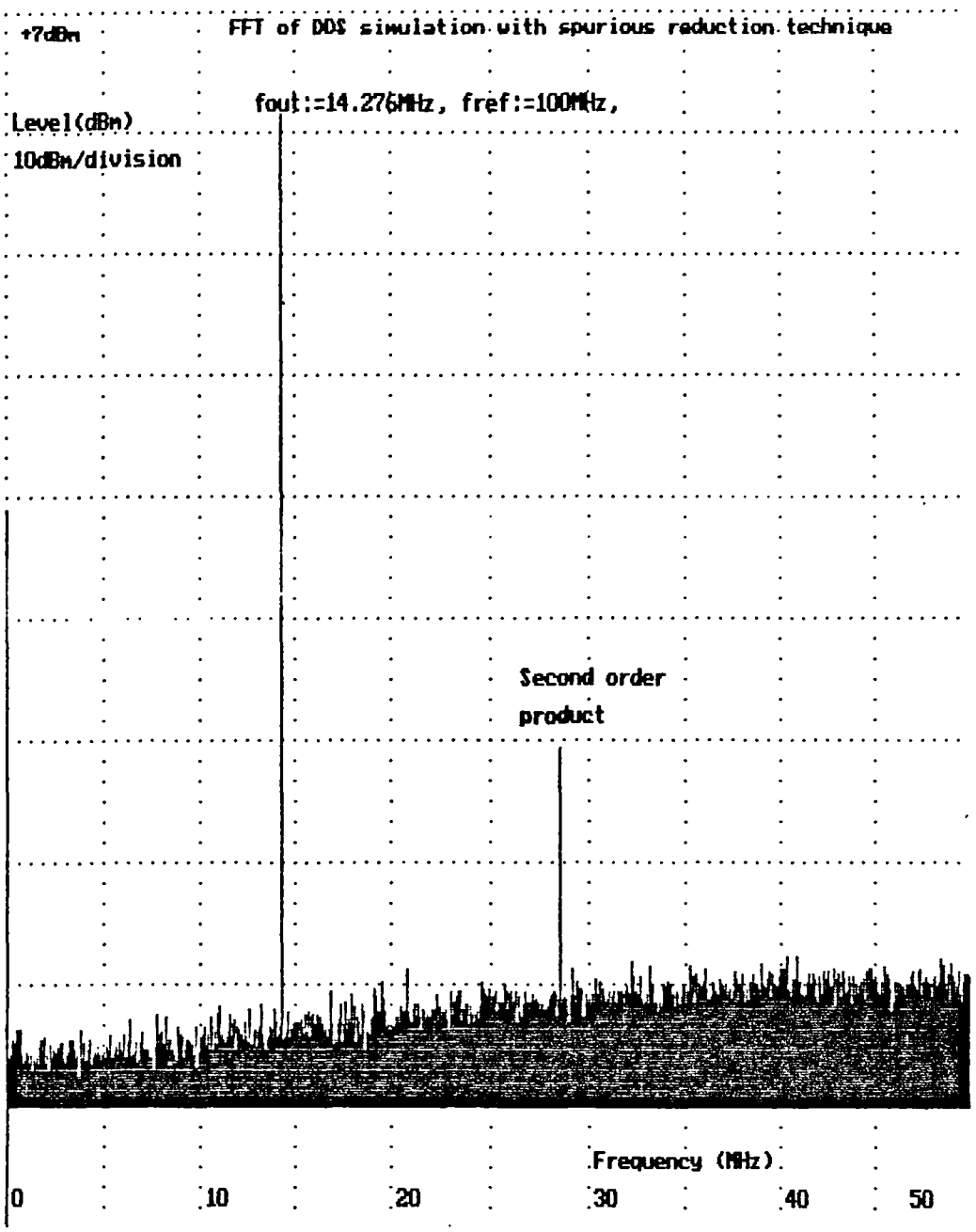


Fig 8.40 Broadband DDS with decorrelation, and interpolative dither

By expanding a region around the carrier of the broadband plot of fig 8.40, the plot of fig 8.41 is obtained. The spurious sideband signals are reduced to a level indistinguishable from the noise floor.

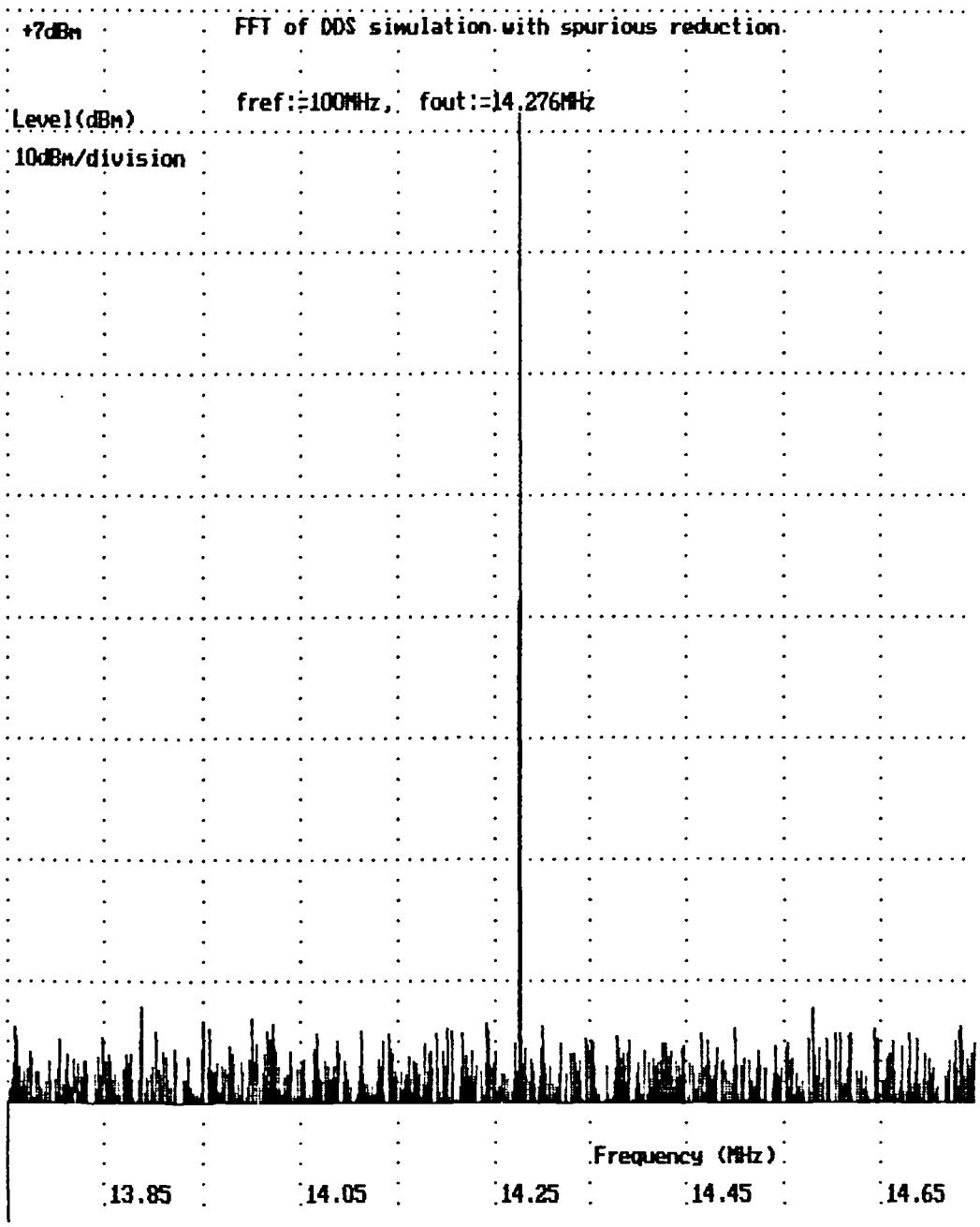


Fig 8.41 Fig 8.40 expanded showing close to carrier region

In many DDS implementations, the 3rd harmonic aliased product is usually high. This occurs at $f_{ref}/4$, therefore a simulation was performed at this output frequency. Fig8.42 illustrates the output spectrum with no spurious reduction techniques enabled, clearly illustrating the third order product at $f_{out} = f_{clock}/4$. Applying decorrelation results in the spectrum of fig8.43 for an identical range of frequencies. The third order product is reduced by at least 20dB.

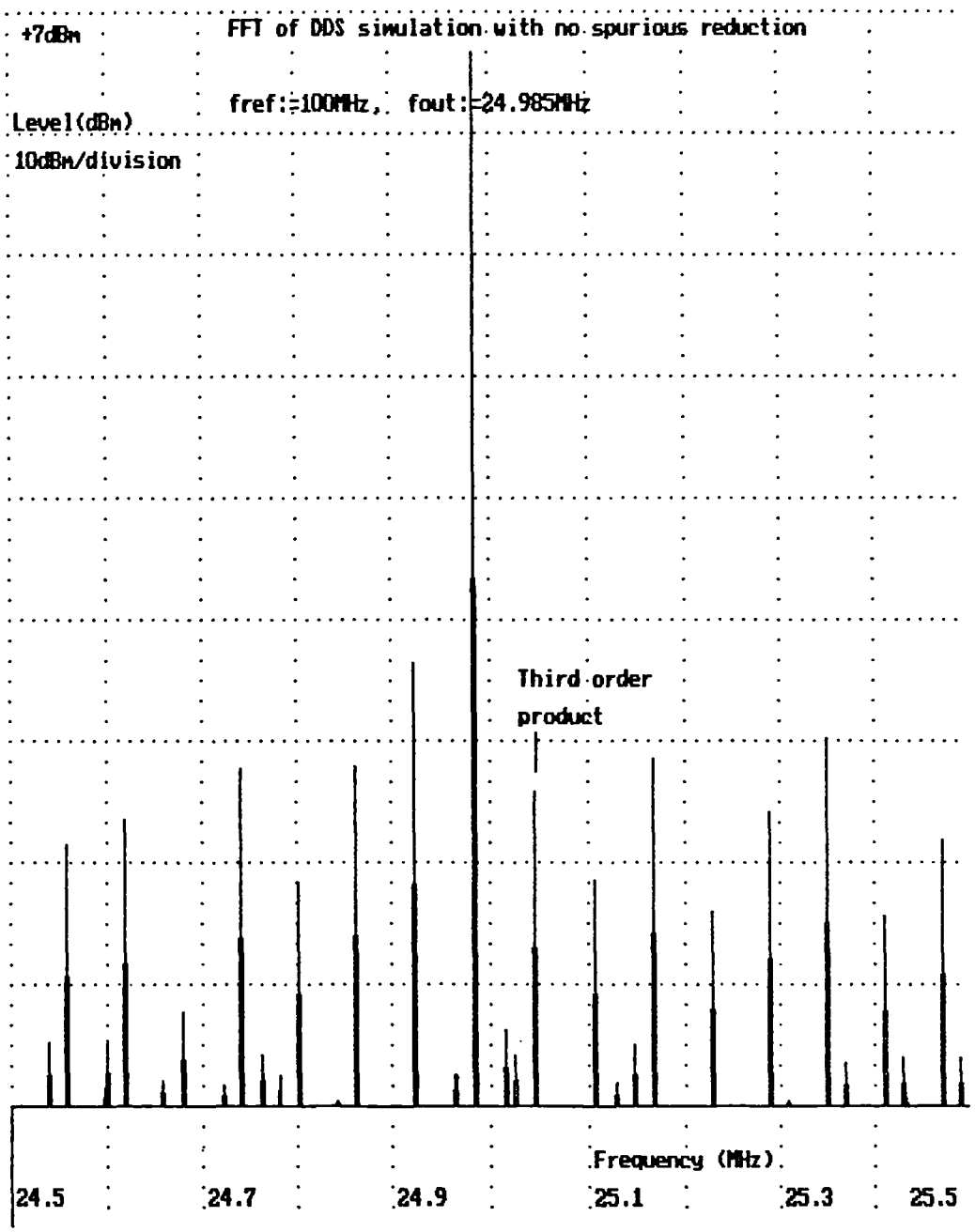


Fig 8.42 DDS simulation with real DAC, showing third order product.

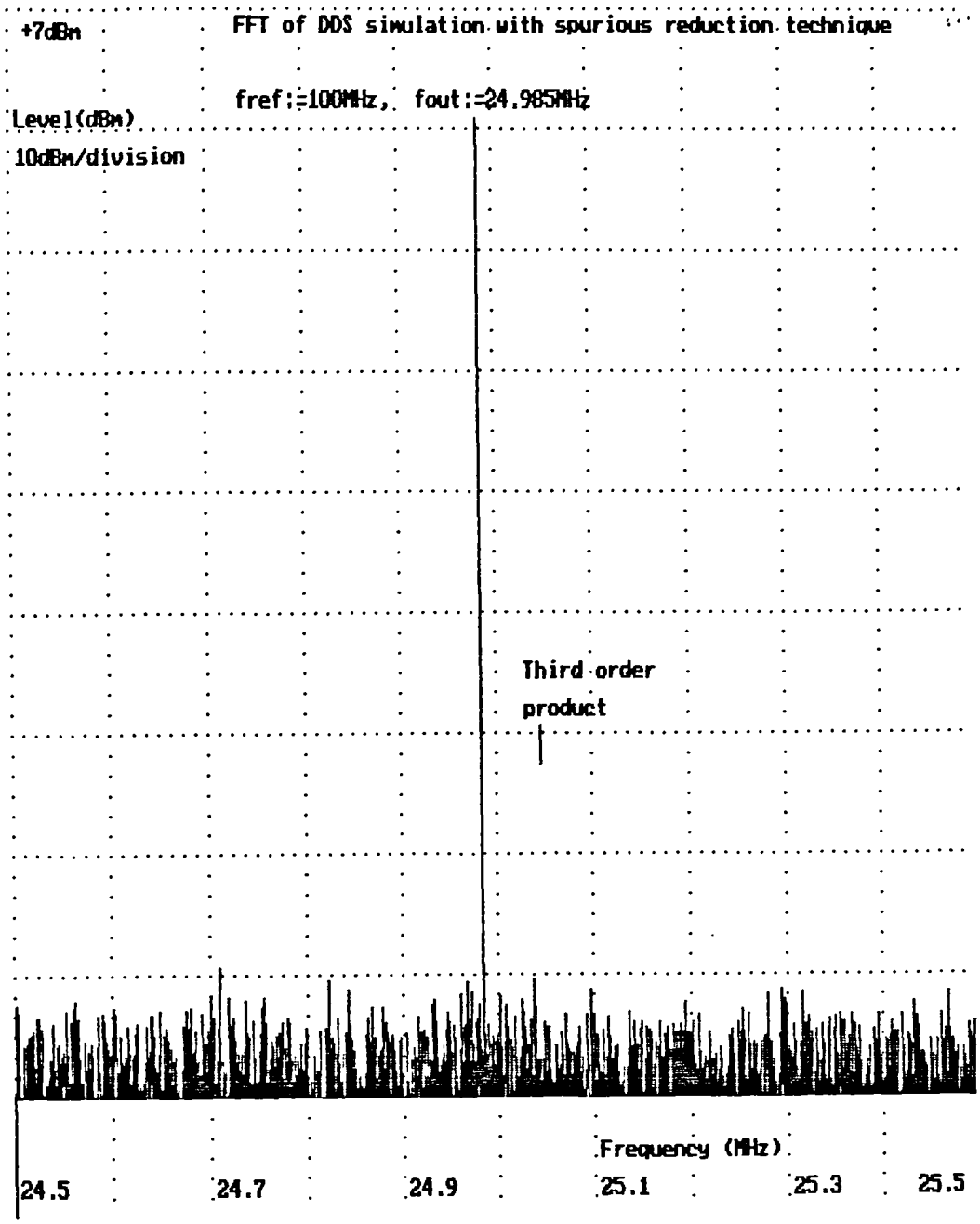


Fig 8.43 DDS simulation with real DAC and decorrelation, showing third order product.

8.10 Frequency Search of Simulated Synthesiser

With direct digital synthesisers, the error spurious spectrum can change drastically as different output frequency channels are selected. For this reason it is necessary to undertake a frequency search. The synthesiser is incremented through a range of possible output frequencies and the maximum level of spurious signal produced by the FFT is noted. The close to carrier spurious signals are primarily of interest, therefore searching is

restricted to a limited region around the carrier. Modifications were therefore carried out to include each synthesiser simulation in a loop that repeats the simulation for every frequency increment. Appendix A4 illustrates the program simulates the DDS and stores the data. Maximum levels of spurious signals are monitored over a small range of 200 channels. A histogram is then used to display the maximum spurious signal level for each band.

8.10.1 Ideal Synthesiser, no dither

Fig 8.44 displays the plot of the frequency search for the ideal 8 bit synthesiser over a search range of ±1 MHz. It can be observed that there is considerable variability in the levels of spurious signals between the bands. Another observation is that no trend is visible as the output frequency is increased. The maximum spurious level obtained with 8 bit amplitude and 12 bit phase resolution is -58 dBc at an output frequency of 12.109 MHz. This result is a theoretical one therefore the results for a practical unmodified DDS implementation will be greater than -58dBc.

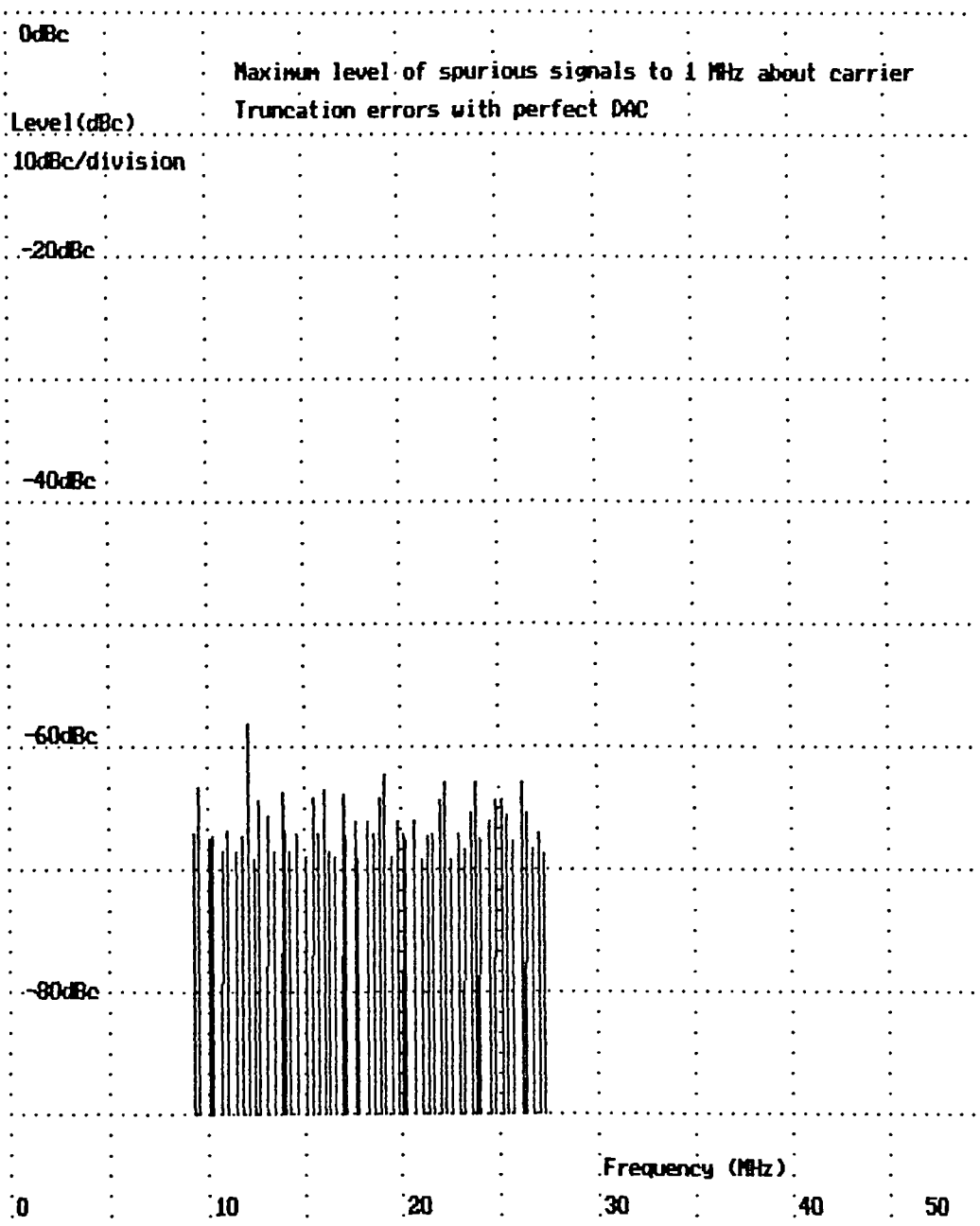


Fig 8.44 Maximum levels of spurious signals obtained from frequency search of 9.155 to 27.47 MHz

8.10.2 Ideal Synthesiser, with dither

Phase and amplitude dither are then introduced to the simulation of the ideal synthesiser. The phase dither is 8 bits wide giving a total dither value of 1/256 of a cycle. With dither applied, the FFT size was increased to 250k points to allow increased resolution of spurious signals in the noise. A frequency scan is begun of the synthesiser resulting in a maximum spurious level plot as shown in fig 8.45. The maximum level obtained in the plot is -75 dBc which can be contrasted with -58 dBc with no dither.

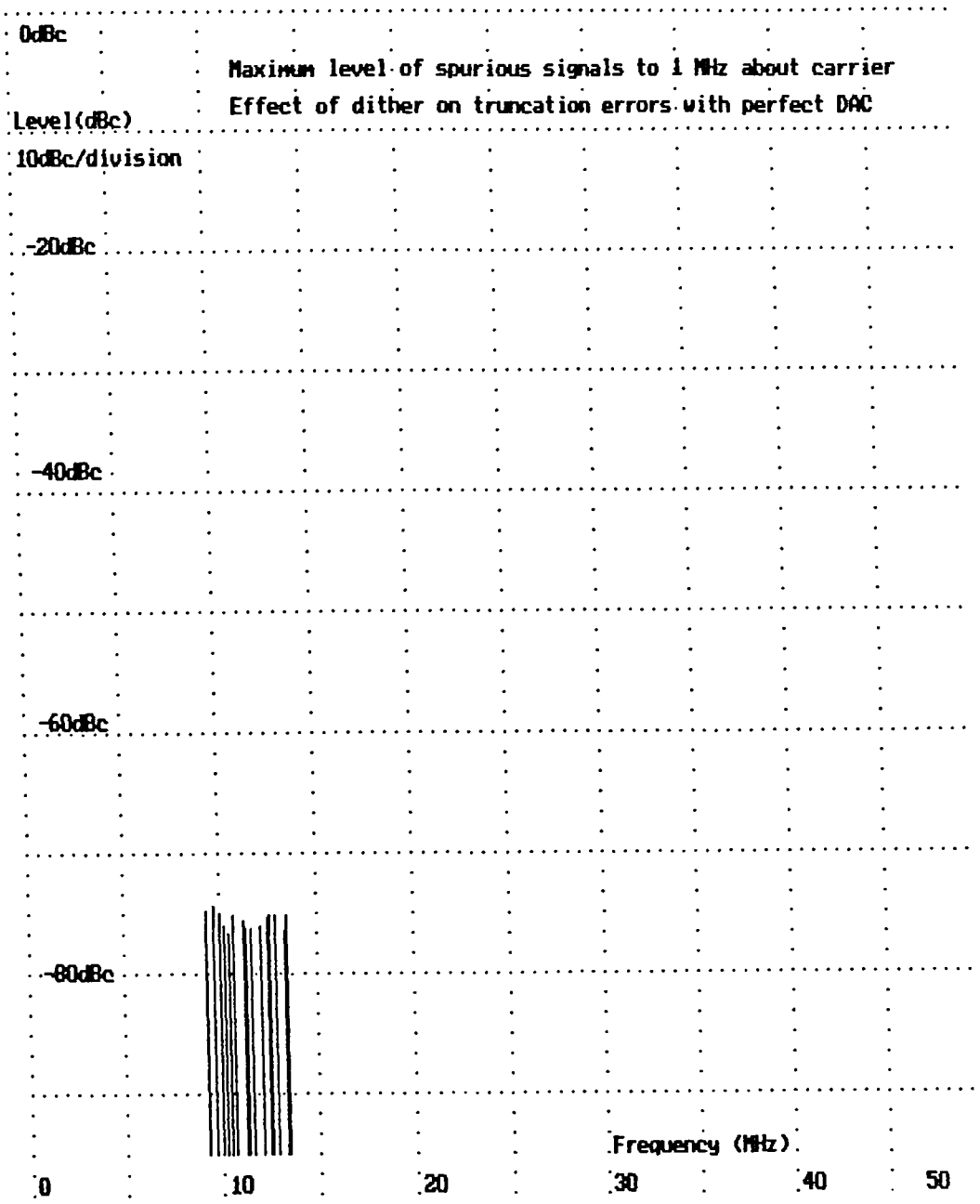


Fig 8.45 Spurious signal levels, ideal DAC and dither, frequency range 9.155 to 13.732 MHz

8.10.3 Synthesiser with simulated real DAC, DAC decorrelation and dither

A frequency scan of the complete synthesiser with simulated real decorrelated DACs and interpolative dither is displayed in fig 8.46. As with §8.9.9, a 256k FFT is used. The maximum spurious signal levels recorded range from -72 dBc for a frequency value of 9 MHz to -68 dBc at 27.5 MHz. This may not be the actual level of spurious signals, but the peak levels of the residual pseudo-random noise at the output. Nevertheless, the level

of spurious signals is below that given by truncation errors from a DDS with an idealised DAC as plotted in fig 8.44 above.

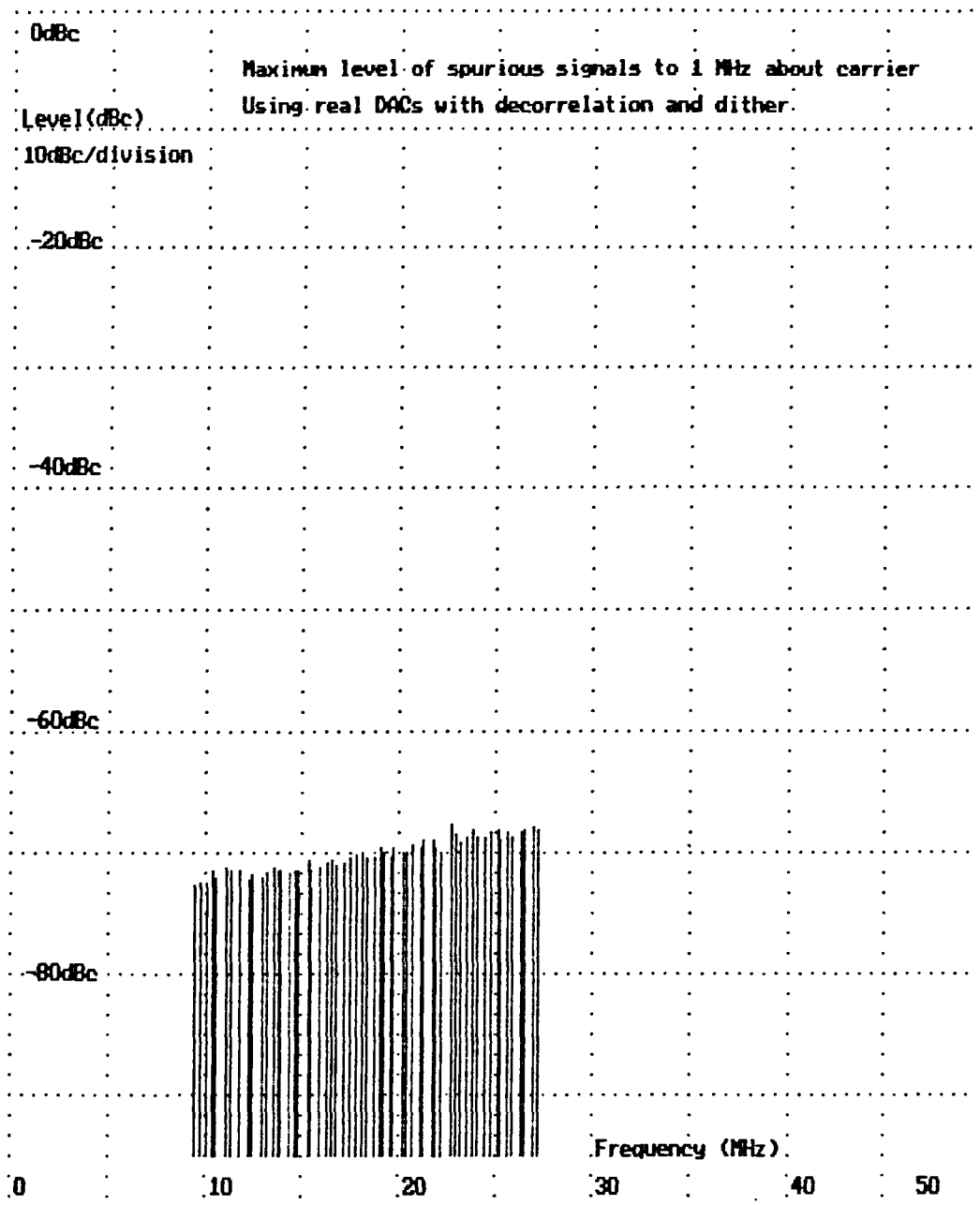


Fig 8.46 Spurious levels, real DAC, decorrelation and dither, frequency range 9.155 to 27.47 MHz

8.11 Measurements on a DDS built to incorporate spurious reduction techniques

8.11.1 Look-up Table

After computer simulations indicated favourable results with the spurious reduction techniques described in §8.4, construction of an experimental synthesiser commenced. The synthesis equation used was:-

$$V_{out} = 0.5+(2^P-2)\left(0.5+0.5\cos\left(\frac{2\pi T}{2^A}\right)\right) \qquad (8.66)$$

This equation was blown into a 4kbit EPROM which allowed the use of 12 bit address lines and 8 bit data lines.

8.11.2 Pseudo-random number generator (PRN)

Fig 8.47 displays the circuit diagram of the random number generator used in the experimental synthesiser [Rabiner &Gold, 1980c]. An advantage of such an implementation is speed, as one random number per clock cycle is generated. The random number generator must be seeded, and this is achieved by allowing the bank of flip-flops A to be set to a high impedance output state. The pull up and pull down resistors R1 - 3 set the value of the seed. Other flip-flop output will be indeterminate, but this gives no adverse consequence as the actual seed value is unimportant so long as all bits are neither all ones or all zeros. When the flip flop outputs are changed from the high impedance state to the enabled state, the pseudo-random number generation process begins.

8.11.3 First decorrelation circuit

Fig 8.48 displays a schematic diagram of the circuitry that implements the first decorrelation method. IC51 is a 16 bit ALU configured as an accumulator by enabling the internal feedback path between the output register and the B input register. Immediately following this is the look-up table IC52 which is a 64kbit EPROM that stores a complete cycle of a sinewave. After the EPROM is placed a re-synchronising latch IC53 which cuts down the propagation delay between the output of the EPROM and 4 bit ALUs IC54 and IC56. These ALUs add the pseudo-random sequence if the EPROM MSB output is low, or subtract if the MSB bit is high. Outputs from the ALUs are fed to clocked latch IC55, which reduces data skew at the input to the DAC. IC59, IC60, IC61, IC62 enable

cancellation of the pseudo-random number by addition if IC 54 and IC56 subtract, and form the 2's complement for subtraction if IC54 and 56 add. Complementation of the pseudo random signal is achieved be means of the XOR gates of IC59 and IC60.

Latch IC58 can be enabled and disabled to allow the decorrelation to be inserted or removed. Such a facility enables the performance to be compared with or without the use of the spurious reduction technique.

Fig 8.49 shows the summation of the DACs. The DACS used were DAC 0800, which gave a particularly poor spectrum in the normal DDS circuit. Both DACS have re-synchronising latches at the input as discussed above. The analogue outputs of the DACS are summed at the op amp IC82 as described in §8.4.4.

8.11.4 Second decorrelation circuit

Fig 8.50 is a schematic of the second decorrelation circuit. In essence, the circuit is similar to fig 8.48 but includes extra circuitry to allow the ALU to overflow. Overflows are managed by means of the gates in IC8 to 11. The output, pin 8 of IC 8 forces the signal DAC, IC80 of fig 8.49 MSB when overflows occur. Overflows or underflows are signalled by means of the carry output from the the post EPROM ALU comprising IC5 and IC7. The output of IC9 pin 8 controls the MSB of the cancellation DAC, IC81 of fig 8.49 via IC16. Decorrelation is enabled by means of S1. At the RHS of fig 8.50, the digital signals are fed to the analogue conversion circuit of fig 8.49. IC13 to 16 performed 2's complementation as do IC59 to 62 of fig 8.48. The analogue conversion circuit is identical for whichever decorrelation circuit is used. No cancellation or balancing adjustments are provided. A spectrum analyser can be connected to the analogue output to enable the spurious signal and noise sidebands to be measured. In both DDS circuits the clock frequency is provided by crystal X1.

8.11.5 Interpolation dither circuit

Fig 8.50 also includes the phase dither circuit. This is implemented by means of an adder IC2 which adds the pseudo random number to the output of the phase accumulator. The magnitude of the distribution limits (width) to the pseudo-random number (PRN) can be set by a DIP switch DIP1 in ascending powers of 2 to a maximum of 2^8. In the interests of economy, the PRN is selected from lower tappings on the output of the PRN generator of fig 8.47. In doing so, only one PRN generator is required for the synthesiser. Such a practice will not guarantee freedom from correlation with the PRN used for DAC decorrelation, but measurements indicated that dither still produced significant gain. A computer simulation is recommended for further study to ensure that the spurious signals

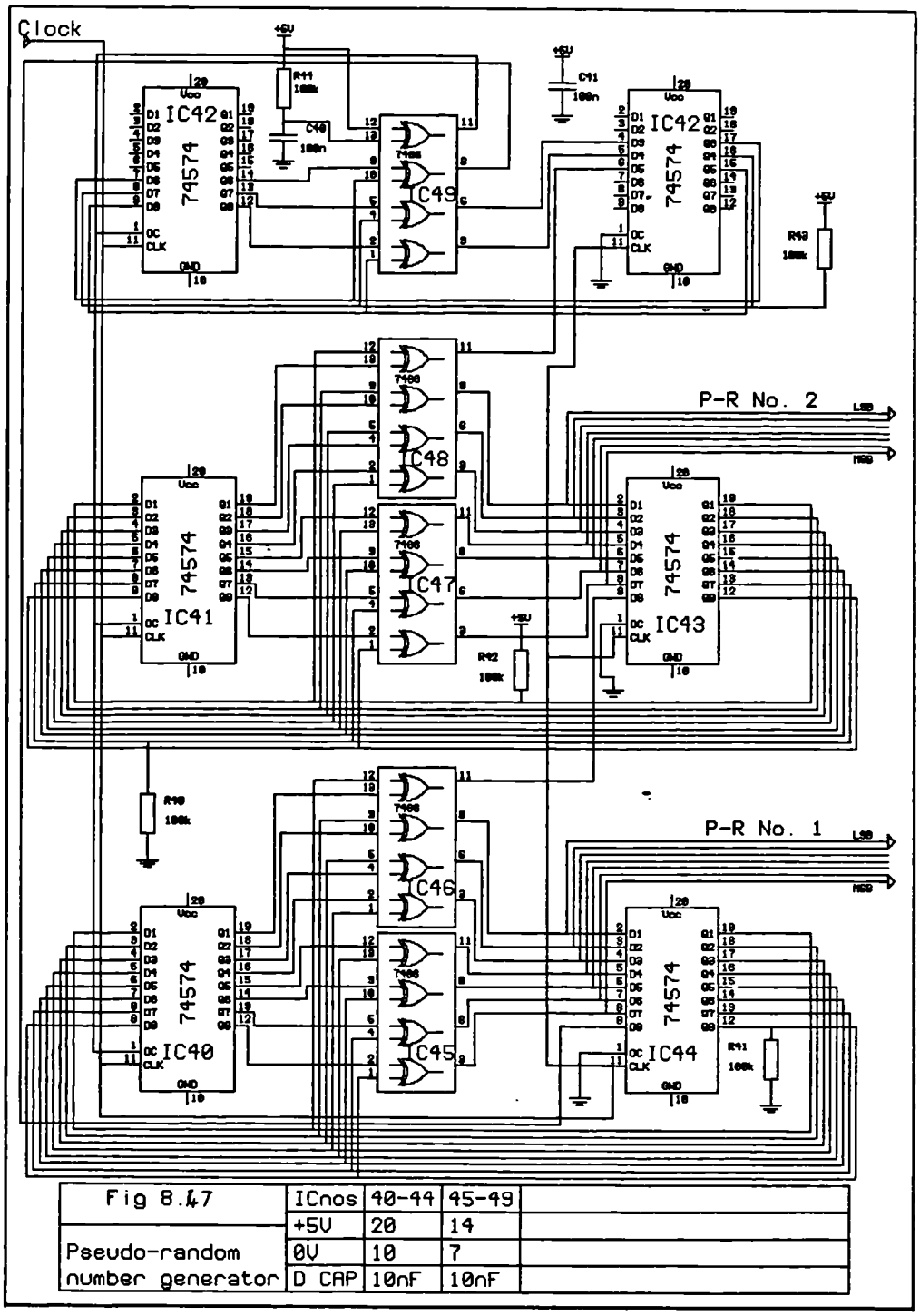


Fig 8.47	ICnos	40-44	45-49	
	+5V	20	14	
Pseudo-random number generator	0V	10	7	
	D CAP	10nF	10nF	

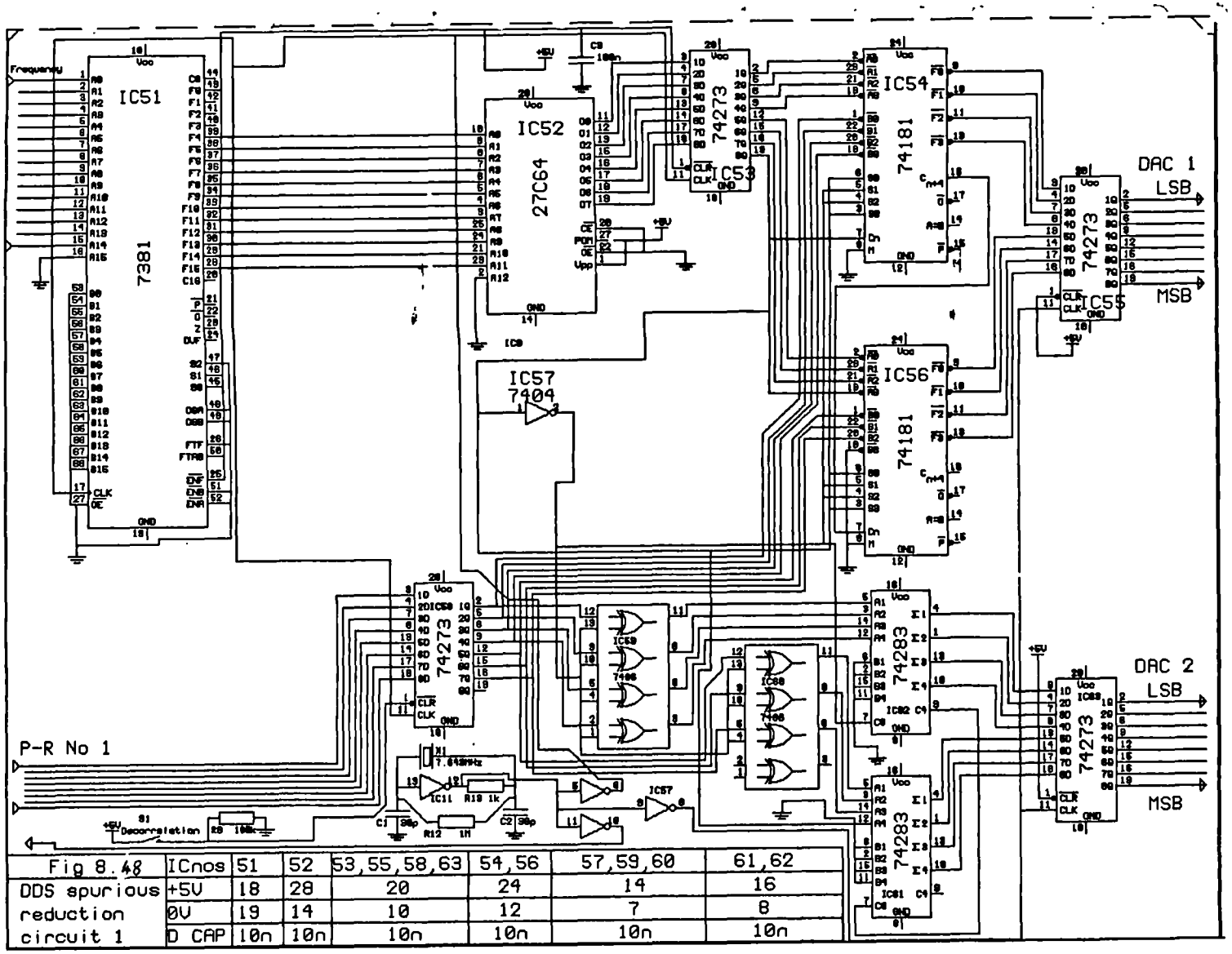


Fig 8.48	ICnos	51	52	53,55,58,63	54,56	57,59,60	61,62
DDS spurious	+5V	18	28	20	24	14	16
reduction	0V	19	14	10	12	7	8
circuit 1	D CAP	10n	10n	10n	10n	10n	10n

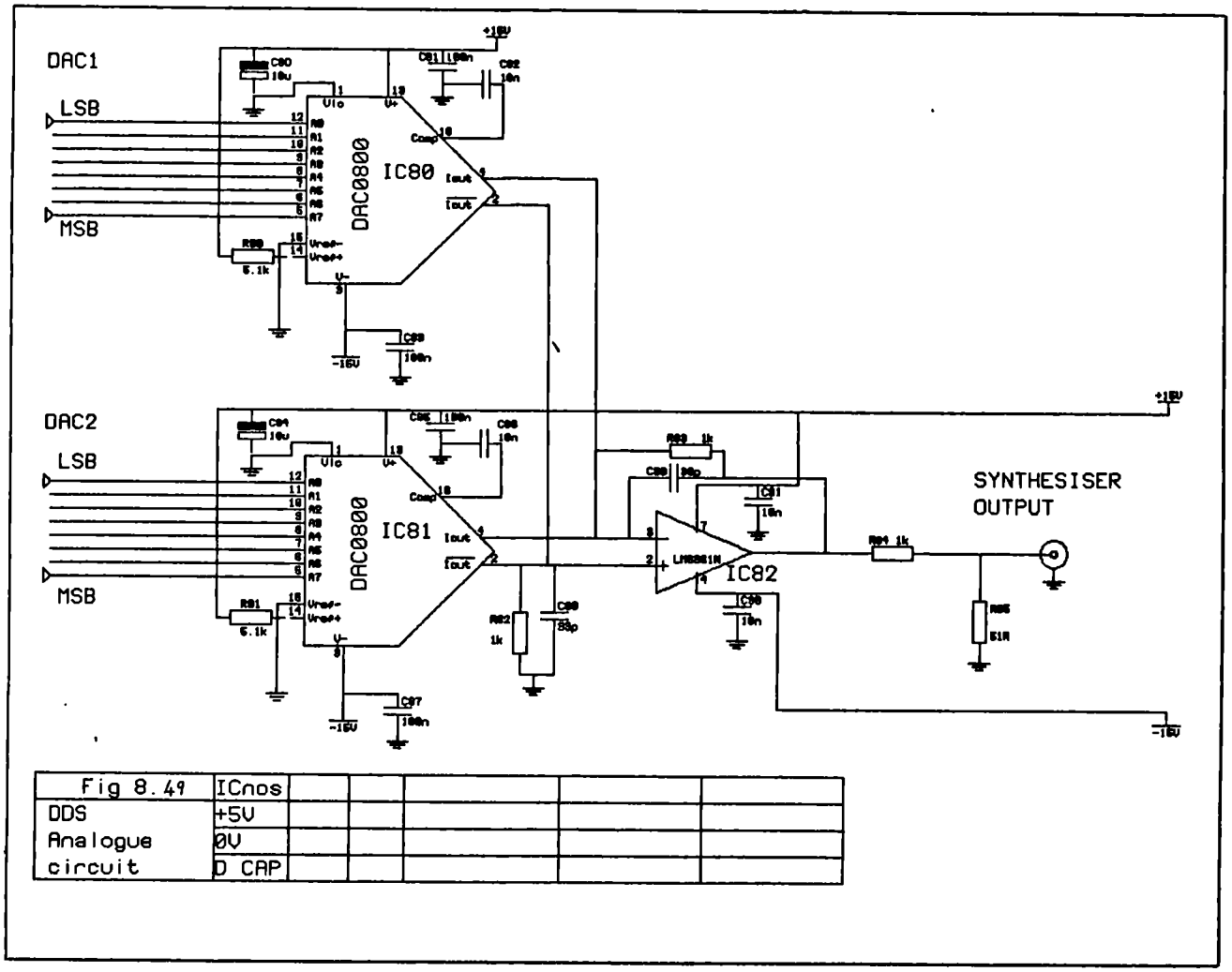


Fig 8.49	ICnos					
DDS	+5V					
Analogue	0V					
circuit	D CAP					

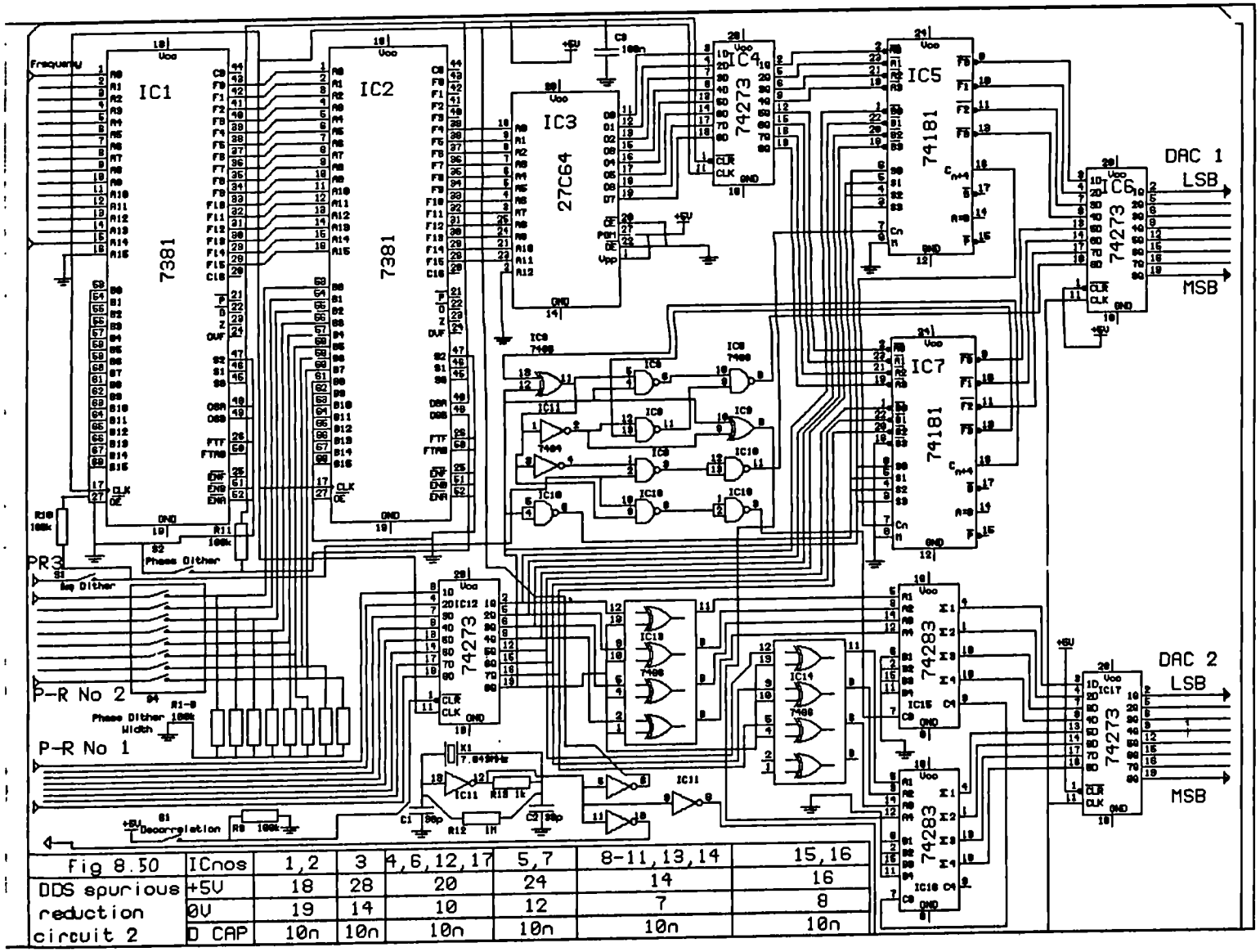


Fig 8.50	ICnos	1,2	3	4,6,12,17	5,7	8-11,13,14	15,16
DDS spurious	+5V	18	28	20	24	14	16
reduction	0V	19	14	10	12	7	8
circuit 2	D CAP	10n	10n	10n	10n	10n	10n

remained low for all frequency outputs and accumulator phase states. Phase truncation dither is selected by S2, and two state amplitude truncation dither by means of S3.

8.11.6 Verification of performance

A DDS has been built to implement the above techniques discussed in §8.4.3 and §8.4.4. 7.6 MHz was used as the clock rate f_{ref}. The resulting performance is displayed in fig 8.51.

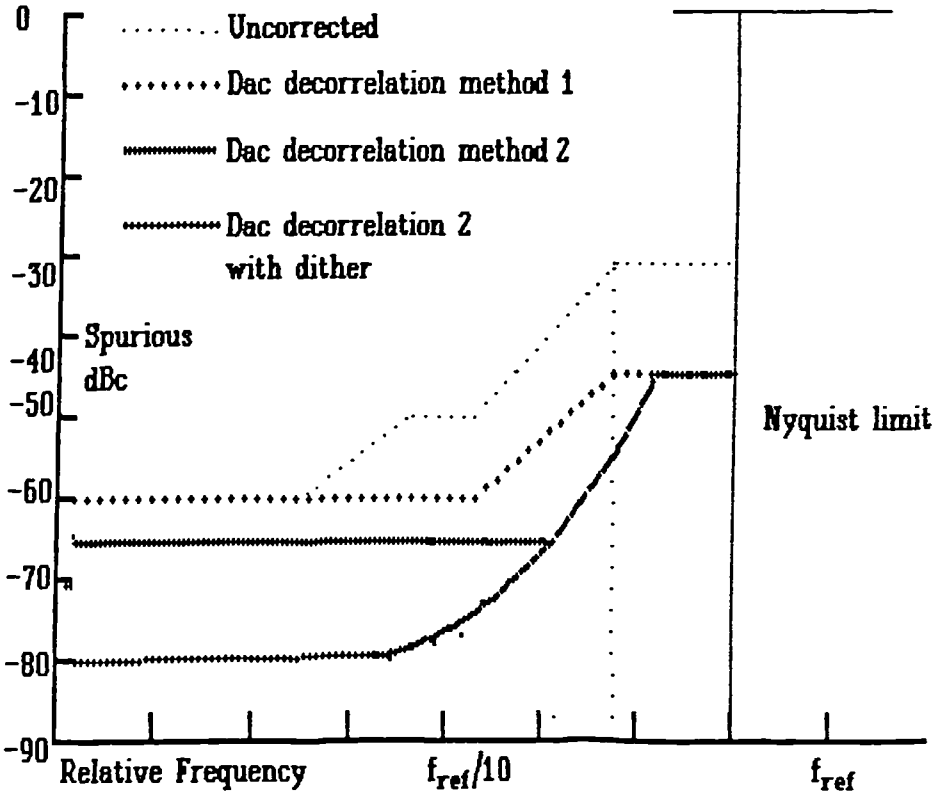


Fig 8.51 Measured performance of various DDS embodiments f_{ref}=7.643 MHz

Decorrelation method 2 gives far superior results to that of method 1. Although the spurious products were reduced with method 2, they were reduced still further by the simultaneous application of dither, and the number of products were also reduced (fig 8.52). Also it can be noted that the spurious reduction was not as effective for output frequencies above $f_{ref}/4$. It was not clear from the measurements whether these spurious signals arise within the DACS or within the operational amplifiers following the DACs. Table 8.6 shows that the harmonics of f_{out} are also reduced by this technique.

Fig 8.52 illustrates a spectrum analyser plot of the close to carrier spectrum of the measured DDS output at 1.529 MHz.

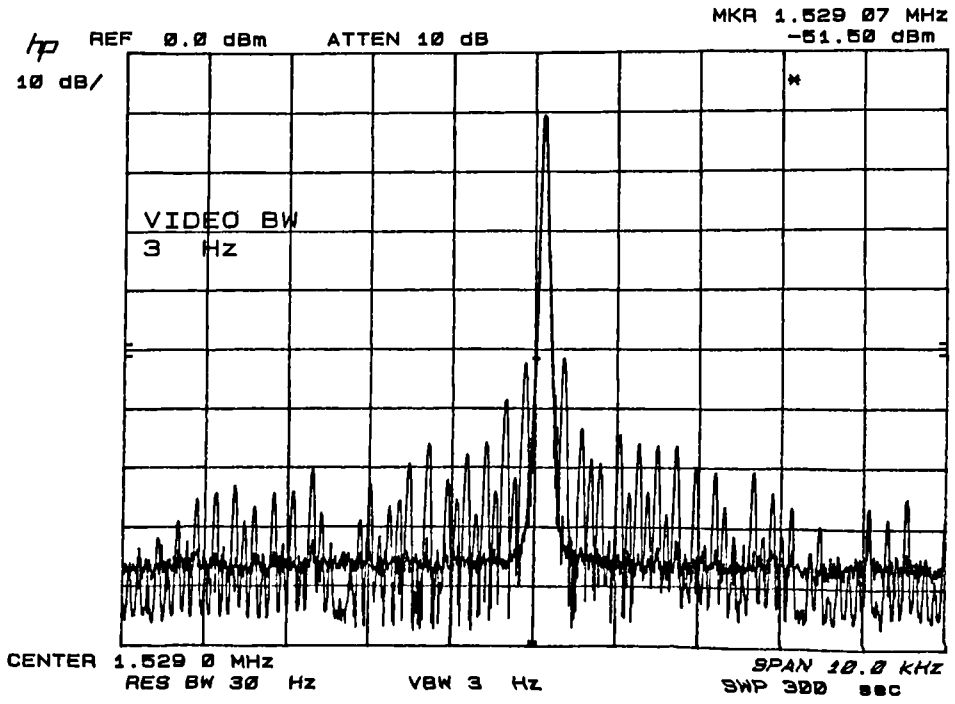


Fig 8.52 Measured Spurious signals of the prototype DDS, f_{out} = 1.5291 MHz

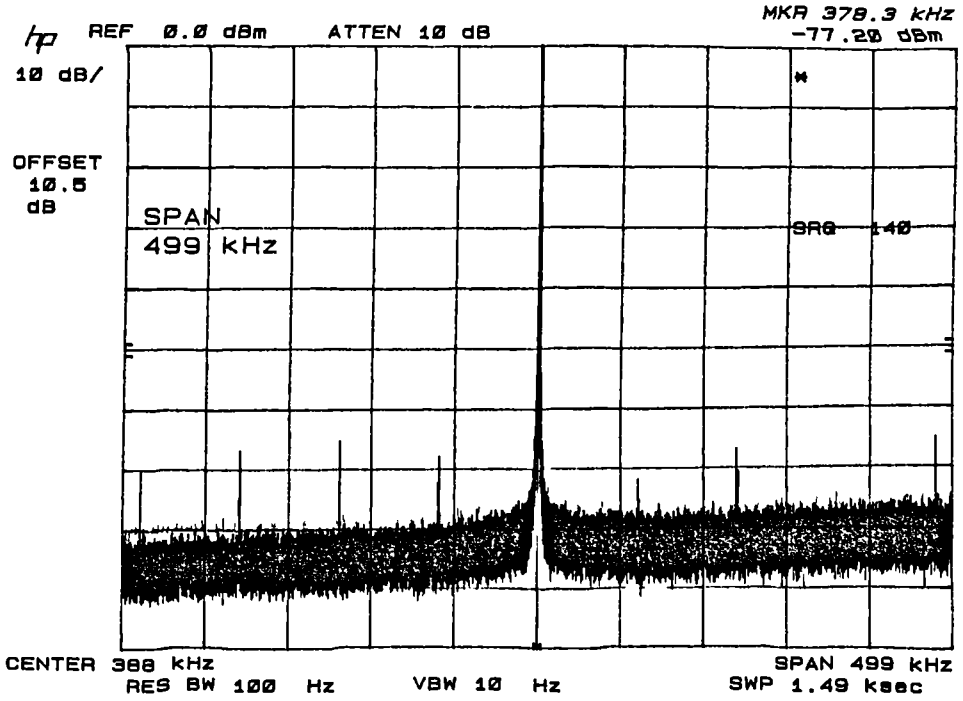


Fig 8.53 Effect of DAC decorrelation and dither, prototype DDS, f_{out} = 388 kHz

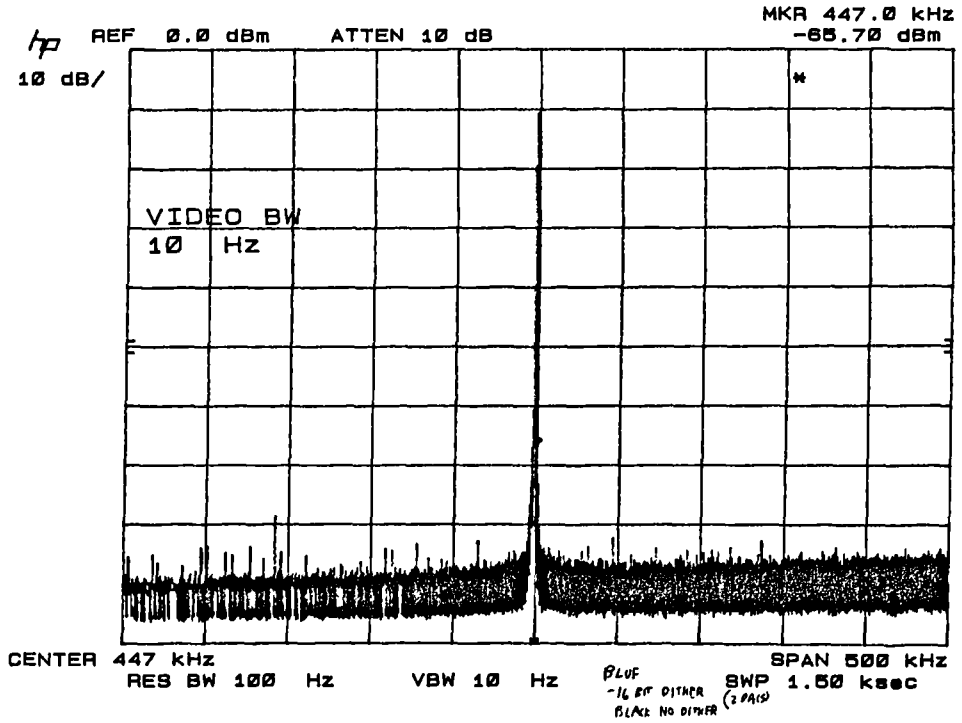


Fig 8.54 Effect of DAC decorrelation and dither, prototype DDS, f_{out} = 388kHz

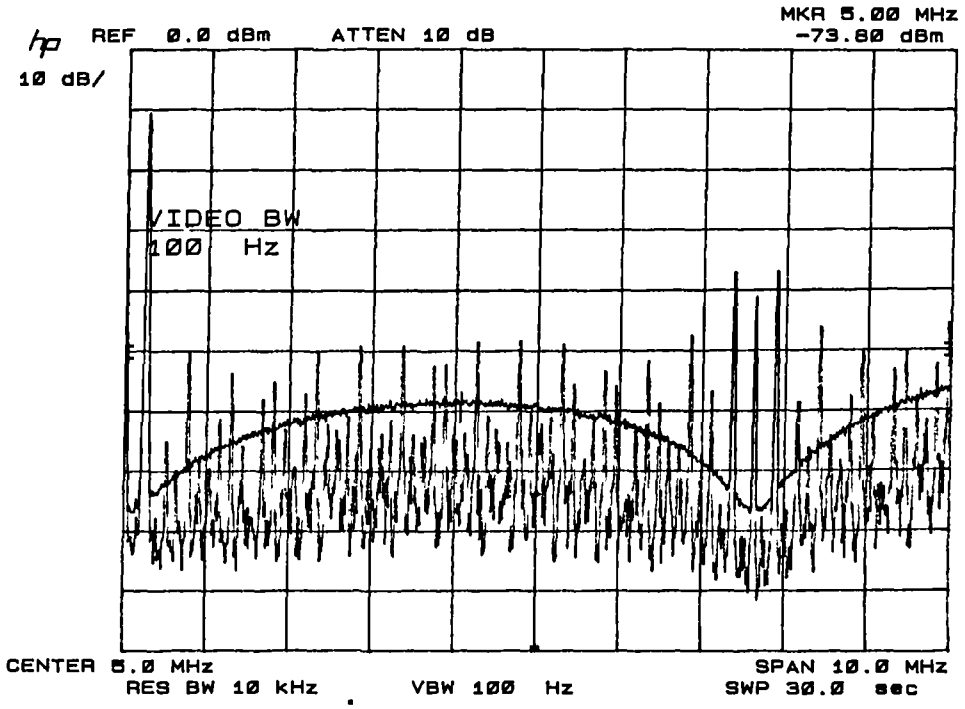


Fig 8.55 Broadband plot of prototype DDS, f_{out} = 274kHz

A blue trace is used to represent the output with no spurious reduction, and the black trace represents the synthesiser with decorrelation applied and phase truncation dither switched off. To demonstrate the effect of dither, figs 8.53, and 8.54 show the output spectrum of the synthesiser at 388 kHz and 447 kHz respectively. In the former spectrum, the brown plot represents the application of decorrelation and amplitude dither only, and the green trace shows the reduction in spurious signal levels by the simultaneous application of phase truncation dither and decorrelation. The latter plots, fig 8.54 show the effect of a frequency change, removing the dither gives the black trace, and applying the dither gives the blue trace. Broadband plots are given by fig 8.55, for a 274 kHz output, displaying the effect of decorrelation on the harmonics. The spectral shape of the noise due to the glitches can be clearly seen here, predicted by equation 8.28b to be distributed in the form of a sine curve.

The output noise of the prototype synthesiser was measured with the aid of a Hewlett-Packard spectrum analyser type HP8566B. Noise density figures obtained from such a measurement will include the AM component of the noise, and this must therefore be allowed for in the calculation of the phase noise levels. The noise sideband measurement results obtained from the prototype DDS are given in fig 8.56. These results were obtained 10 kHz from the carrier.

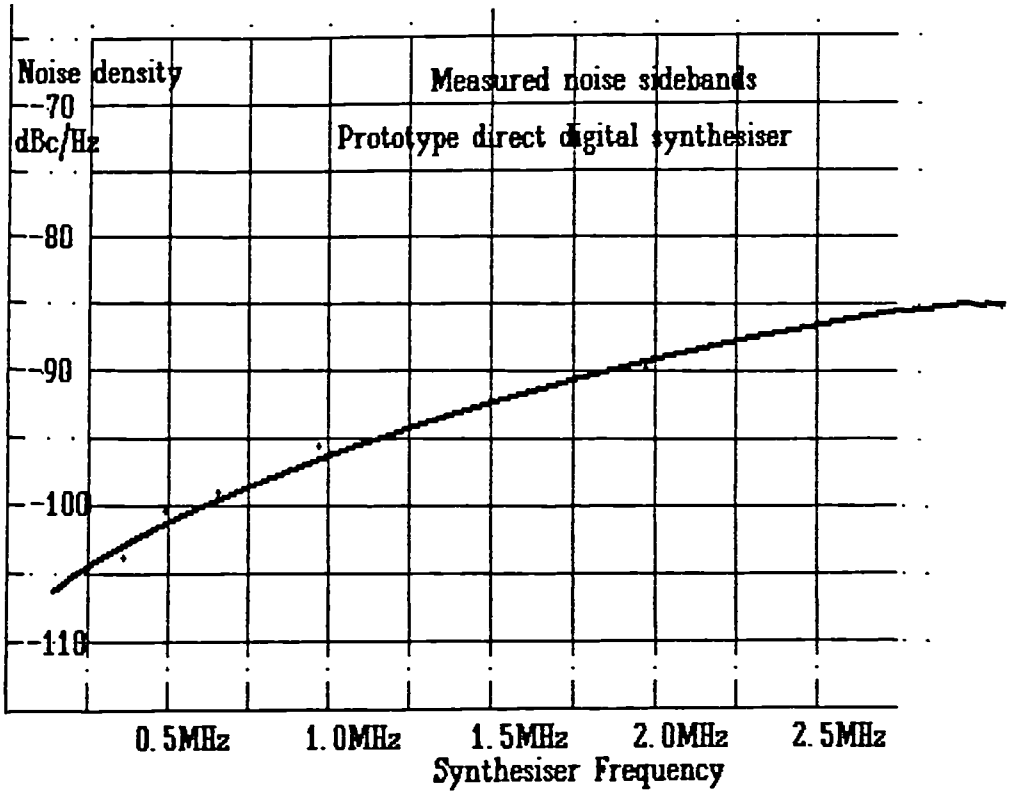


Fig 8.56 Measured phase noise of the prototype DDS, $f_{ref} = 7.643$ MHz

Having demonstrated the effect at low frequencies it is now necessary to implement this at RF frequencies. Computer simulations need to be undertaken to ascertain the effect of the different DAC non-linearities. The effect of different forms of dither must also be considered on the spurious performance of the synthesiser. In addition, degradation of the phase noise performance of a synthesiser by a sample and hold must also be considered. The implementation of this form of synthesiser in conjunction with other techniques in order to realise a fast hopping/ high purity microwave synthesiser is recommended for consideration.

Table 8.6 DDS measured harmonic output

Clock Frequency 7.64314 MHz		Harmonic			
Frequency	Decorrelation	2nd	3rd	4th	5th
60 kHz	Off	-52 dBc	-55 dBc	-62 dBc	-55 dBc
	On	-70 dBc	-65 dBc	<-75 dBc	-66 dBc
250 kHz	Off	-55 dBc	-38 dBc	-60 dBc	-44 dBc
	On	<-70 dBc	-60 dBc	<-70 dBc	<-70 dBc
450 kHz	Off		-32 dBc		
	On		-60 dBc		
1.9 MHz	Off	-40 dBc	-27 dBc		
	On	-44 dBc	-48 dBc		

8.12 Conclusions

Chapter 8 has showed that significant reduction of spurious signal levels can be achieved for DDS without compromising phase noise levels excessively for satellite communications work.

In chapter 6 a requirement for a fine stepping synthesiser with low spurious sidebands, low phase noise and low susceptibility to microphony is suggested. Direct digital synthesis can provide low microphony and phase noise, but the reduction of the spurious sideband levels are the subject of this chapter. In direct digital synthesis, the majority of the spurious signals arise from non-linearities in the DAC. A discussion of these non-linearities was given. It was concluded that glitches from switching errors was a major contribution to the spurious signal spectrum at high clocking speeds. Existing methods of overcoming spurious problems were described. All these methods displayed some drawback which hindered their usefulness.

In this chapter two new techniques are introduced that reduce the spurious signal levels. These techniques involve the use of locally generated pseudo-random signals to remove repetition of the error patterns in the DACs. The only analogue components required are an extra DAC and a summing means; most of the processing can be accomplished using digital circuitry. Both methods involve the addition of the pseudo-random number to the digital output from the synthesiser, which is subsequently removed after conversion to an analogue signal by the second DAC. The methods differ, however, in that overflows in the digital summation are allowed and catered for in the second scheme. Allowing overflows demonstrated much reduction in residual spurious signals by comparison with the first method. Therefore the remainder of the chapter concentrated on the application of the second method. These methods were termed DAC decorrelation owing to their removal of time domain correlation of the DAC errors that result in high spurious signal levels. Suppression of dynamic DAC errors enabled the use of an interpolative dither to reduce truncation errors.

Having established a suitable method of spurious reduction, the chapter followed this with a phase noise analysis of the decorrelation end dither methods. The analysis indicated that the phase noise is a function of DAC glitch level, output frequency and clock frequency. Predicted levels of phase noise was lowest from a segmented DAC clocked at 300MHz which gave a noise floor of better than -125dBc/Hz. Phase noise levels should improve as the clock frequency is increased.

Following the phase noise study, an analysis of discrete spurious levels was undertaken. In the general case this proved an extremely complex issue, therefore a simplification was allowed by considering the errors as an impulse. The aim was therefore to compare spurious levels resulting from implementation of the different methods, rather than predict the absolute levels. For static errors a reduction in levels occurred that increased with the order of the spurious product. When dynamic errors (glitch errors) was considered, all products higher than the second vanished. This satisfied the aim of DAC decorrelation in reducing the effect of DAC switching phenomena.

Computer simulation programs were written for the following cases:-

a) DDS with an ideal DAC showing the effect of truncation errors

b) Application of interpolative dither to an ideal DDS

c) DDS using a real DAC

d) DDS using a real DAC along with DAC decorrelation and dither.

The computer simulations were undertaken by creating a time domain file of the synthesiser output and converting by means of an FFT to the frequency techniques. Special computation techniques had to be devised to to enable rapid processing of the large FFT files. Simulation **d)** confirmed that spurious signals of an order greater than 2 were drastically reduced by the decorrelation process. To provide confirmation of spurious reduction a spurious search was undertaken over a range of frequencies most likely to be used in practice. Since the close to carrier frequencies are most of interest, the spurious search was restricted to ±1 MHz from carrier.

A plot of maximum spurious levels obtained by simulation **d)** over the frequency range, not only confirms spurious signal reduction from the unmodified DDS case but also shows reduction below the ideal DAC case.

Finally, to confirm the results obtained from this chapter, a DDS was built such that the decorrelation and dither techniques could be implemented. A switch was included so that the DDS performance could be measured with and without spurious reduction techniques. With the first decorrelation method, the spurious products were reduced by at most 10 dB. With the second method applied together with interpolative dither spurious signals were progressively reduced on increasing order to a level of -75 dBc below carrier. In some cases the reduction was greater than 30 dB.

8.13 Further work

The work presented in chapter 8 could be continued by investigating alternative dither techniques. One such technique is the generation of Gaussian distributed random numbers for the dither process.

Simulation could be improved by the use of a more accurate DAC model gained from the manufacturer of the DAC. Also a DDS could be built using the decorrelation technique and including one of the latest generation of segmented DACs.

Although effective modifications have been described, they would be difficult to justify economically unless integrated into a single chip. A program would therefore be required to produce a custom logic device for the digital circuitry. Low cost erasable programmable high density logic devices are available, but the maximum clock speed is at present limited to less than 100 MHz. Faster programmable logic devices are available than this but they will be subject to high development costs. Such a path could be justified

only if economies of scale can be made. An essential part of a further development would therefore be marketing research to see if such economies of scale could be made.

One further modification to the synthesiser could be the use of an active phase noise cancellation circuit. In this case, the noise level is monitored at an unused part of the band, for instance at very low frequencies, and adjustment made to amplitude and timing of one of the DACs to find the lowest phase noise point. By the use of control theory techniques, the noise could be dynamically maintained at the lowest point. Such a technique could enable the realisation of a very low phase noise synthesiser.

References

Analog Devices 1988 AD9768. *Data Conversion Products Databook,* chap. 2, p. 304.

Bromich, T.J. 1908 *Introduction to the theory of infinite series,* p. 177. London: Macmillan.

Browne, J. July 1988 All GaAs line-up fuels high speed Digital Synthesiser. *Microwaves and RF.*

Burr Brown 1988 *Fulfilling the promise: A New High Performance Direct Digital Synthesis Design.* Burr Brown Product Developments. Vol. XIII, No.3.

Colotti, J. 1990 Dynamic evaluation of high speed, high resolution D/A converters. *R.F Design* November 1990, pp. 51-64.

Cooley, J.W., Lewis, P. & Welch, P.D 1969 The finite Fourier transform. *IEEE Transactions on Audio and Electroacoustics.* Vol. 17, No. 2, pp. 77-86.

Daura, F. 1985 The specification of A/D and D/A convertors. *Revista Espanola De Electronica.* Aug-Sept 1985, pp. 70-73.

Dwight, H.B. 1961a *Tables of integrals and other mathematical data,* Integral No. 858.652, p. 221, 4th Ed., McMillan.

Dwight, H.B. 1961b *Tables of integrals and other mathematical data,* Integral No. 858.654, p. 221, 4th Ed., McMillan.

Eutelsat 1989 Eutelsat II specification for Satellite data link equipment, Document no Eut.PS.ASCA 0054/E110 Issue 5 P35

Fish, P.J. June 1982 Direct Digital Synthesiser. *UK Patant No GB 2121627A 2.*

Harris Inc. 1982 Definition of DAC Specifications. *Harris Linear and Data Conversion Handbook* . p. 5-20.

Hosking, R.H. 1973 Direct digital frequency synthesis. *IEEE, Intercon Technical Papers, Paper 34/1.* pp 77 82

Jones, W.J. & Gardiner, J.G. April 1987 Microwave synthesis using mixed analogue and digital techniques. *International conference on Frequency Control and Synthesis, the University of Surrey.*

Jordan, P 1990. A ten bit 350MHz synthesiser for direct digital synthesis. *Proceedings of RF Expo East,* Orlando, Florida. Nov 15th, 1990. p73

McCune, E.W. Control of spurious signals in direct digital synthesizers. *Proceedings of RF Technology Expo 88, Anaheim, California, February 10-12, 1988.* pp. 523 - 537.

Merisse, J.P 1988. A/D and D/A converters, principles and definitions. *Mesures(France)* Vol 53. No 9 pp55-8

Nicholas, H.T. & Samueli, H. 1987 An Analysis of the output spectrum of direct digital synthesis in the presence of phase accumulator truncation. *Proceedings of the 41st Annual Frequency Control Symposium.* p. 495-502.

Rabiner, L. & Gold, B. 1975a. Theory and application of digital signal processing, chap 6, p. 359 NJ: Prentice Hall.

Rabiner, L. & Gold, B. 1975b. *ibid,* chap 10, p. 591

Rabiner, L. & Gold, B. 1975c. *ibid,* chap 9, p. 568

Radar, C.M. 1968, Discrete Fourier Transforms when the number of data samples is prime, *Proc IEEE*,56, No.6, 1107-1108.

Reinhardt, V., Gould, K., McNab, K., Bustamante, M. 1986. A short survey of synthesiser design techniques. *40th Annual Frequency Control Symposium.* pp. 355-365.

Saul, P 1991 Technological limitations in direct digital synthesis. *Colloquium on Direct Digital Synthesis, Digest*. No 1991/172, Bradford

Saul, P.H. & Taylor, D.G. 1989 A 2GHz clock direct digital synthesiser. *Symposium on VLSI Circuits,* Kyoto, Japan. May 25-27 1989.

Stanford Telecom 1987 STEL 9272 130MHz Direct Digital Synthesiser, In *Stanford Telecom Short Form Catalogue,* p. 8.

Stroud, K.A. 1985 Laplace Transforms, chap. 7, p. 195. Stanley Thornes.

TRW 1988 Data converters and DSP products data book Section B, p. 28.

Weiss, F.G. 1986 A 1Gs/s 8-Bit GaAs DAC with on-chip current sources. *Proceedings of the IEEE Gallium Arsenide Integrated Circuit Symposium, Grenelefe, Florida, October 1986.* p. 217-220.

Wheatley, C.E. & Phillips, D.E. 1981 Spurious suppression in direct digital synthesisers. *USA Eradcom May 1981 FT. Monmouth NJ0770.*

Williams, F. 1987 Direct numerical synthesis of sine waves. *RF Design.* May 1987, pp. 30 - 33.

Wilson, M.P. 1990 Signal generation using digital to analogue conversion. *European patent.application no 91302926.0*

Zavrel, R. March 1988 Digital modulation using the numerically controlled modulated oscillator. *RF Design* March 1988, p. 27-31.

9 Application of synthesis to satellite communications systems

9.1 Introduction

This chapter examines the application of synthesiser technology discussed earlier in this thesis to satellite data communications systems.

The advent of digital signal processor (DSP) technology is creating new opportunities for satellite modem modulation techniques [Davarian & Sumida, 1989]. Unfortunately there has not been a similar leap forward in local oscillator technology and many producers are adhering to mobile radio/TVRO synthesiser practice, often with disastrous implications for the BER performance [Payne, 1984]. One effect of such use of noisy synthesisers is that BPSK tends to be still favoured for practical modulation schemes over more advanced coding/modulation schemes such as QPSK and 8PSK. Although the latter can offer greater bandwidth efficiency and coding gain, BPSK is more robust in terms of phase noise degradation [Heron, 1989].

Some of the synthesisers studied are capable of being directly modulated. This has implications for possible simplification of communications systems. This chapter therefore examines how synthesisers, when combined with digital signal processors (DSP), could provide a complete interface between the data and the RF signals. For a transmitter, an architecture is described whereby a synthesiser, DSP and power amplifier are all that is required for a complete transmitter section of a modem. However, not only is it possible to simplify the system design, but lower phase noise levels enable the use of more efficient high level modulation schemes. The effect of such simplifications are demonstrated in this chapter.

Specific satellite communications systems are examined in terms of phase noise performance, applying figures gained from synthesiser configurations studied earlier in this thesis. A goal of such a study is to compare the capabilities of the synthesiser configurations with performance requirements of various modulation schemes. The work centres around a computer program developed to plot performance in terms of equations outlined previously. Initially modem performance is analysed, and this is followed by calculation of effects on overall system link budgets.

Results measured from a modem with a data analyser are then obtained using two different local oscillator configurations. The BER curves are then plotted to compare the effect of the synthesiser configuration.

9.2 Key areas of concern for local oscillator design

So far the following issues have arisen in the use of synthesiser technology for local oscillators in satellite communications systems:-

1) Crystal oscillator technology:

2) In many synthesiser designs the close to carrier phase noise is determined by digital divider and phase detector phase noise, as discussed in §5.7.2.3, which are only in exceptional circumstances specified by the device manufacturer [Avantek, 1989].

3) The inadequate vibration performance of many synthesiser designs.

4) The complexity of present transmitter and receiver design practice is likely to result in pressure to economise on synthesiser performance.

5) The high cost of local oscillators for frequency hopping spread spectrum systems may preclude this technique for competitively priced secure communications systems.

9.2.1 Crystal oscillator technology

In chapter 3 the problem of crystal oscillator phase noise was discussed and in chapter 6 the effect of this on the performance of communications systems was reviewed. As exposed in §6.3.5, problems were most significant for communications systems using high order modulation schemes.

One of the principal problems in the design of receivers arises as a result of having to provide an AFC system to track out oscillator ageing and satellite doppler effects. The coherent demodulators must include a VCO in order to close the carrier recovery loop and track the received signal. There are two usual approaches to this as in fig9.1 and 9.2: the short loop and the long loop methods.

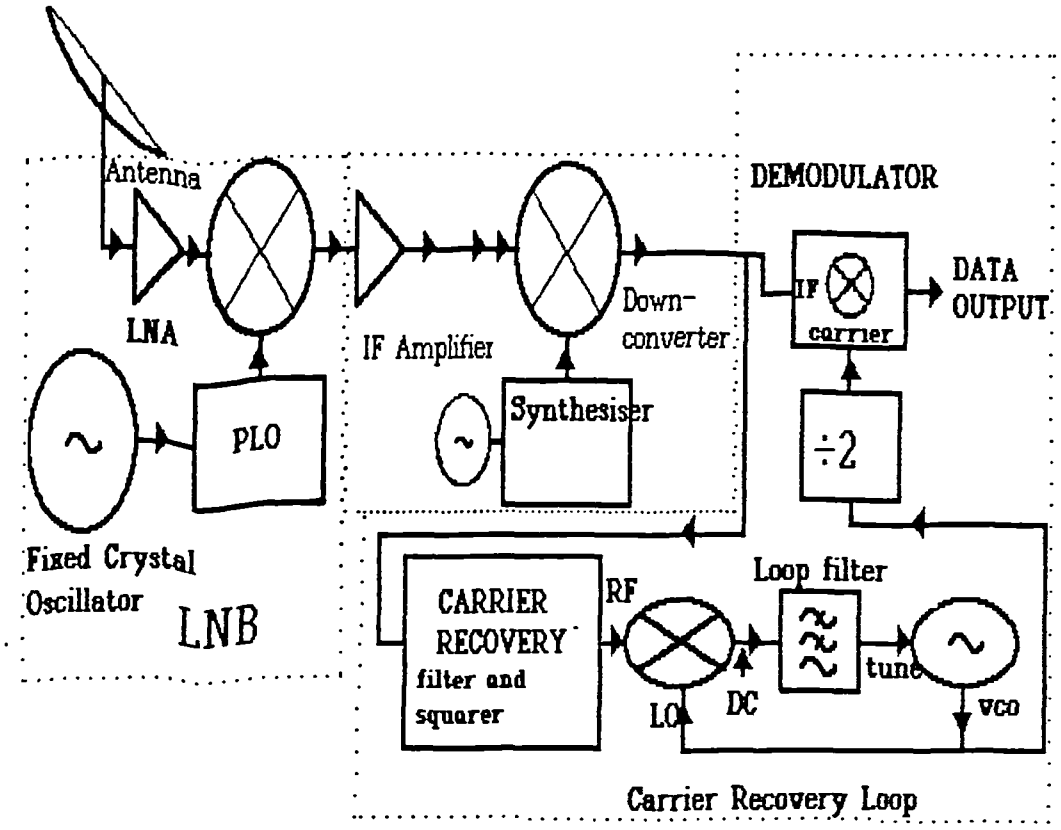


Fig 9.1 Receiver system employing a "short loop" Carrier recovery loop

Short loop

An example of a short loop is displayed in fig9.1. The VCO is placed directly in the demodulator and is tuned to provide the recovered carrier. A minimum tuning range of 2% would typically be required to provide adequate carrier tracking. This is beyond the pulling range of crystal oscillators and would therefore imply a requirement to use a voltage controlled oscillator (VCO). However VCOs produce more phase noise, are sensitive to shock and vibration, and are susceptible to mains related spurious.

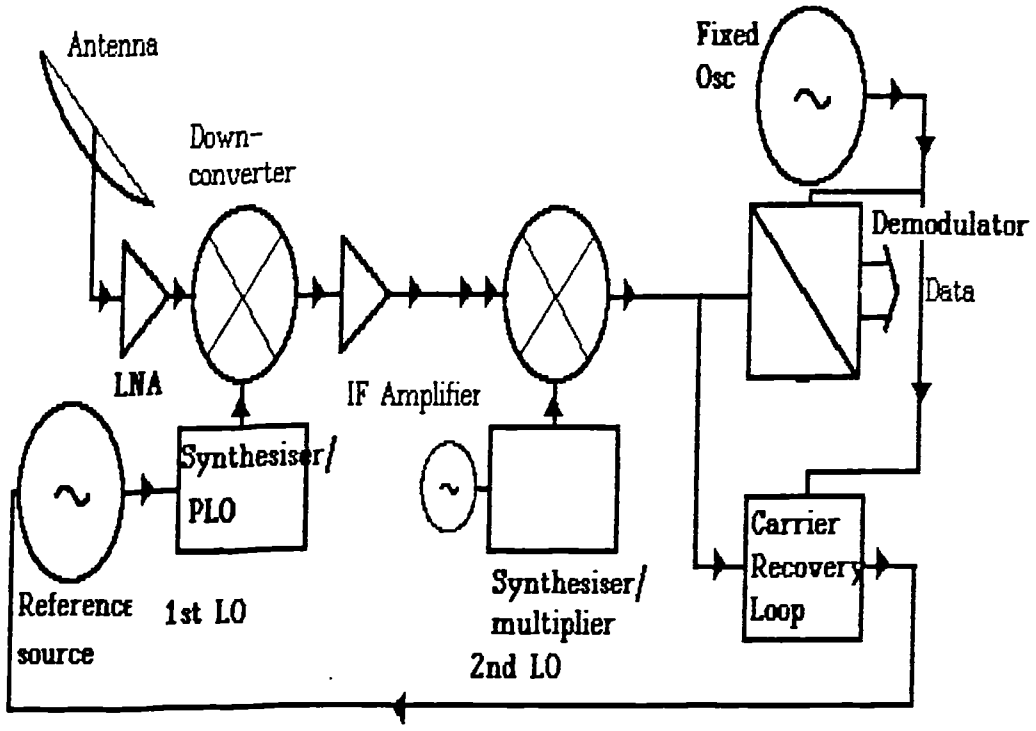


Fig 9.2 "Long loop" approach to downconverter /demodulator design

Long loop

An example of a long loop is displayed in fig 9.2. The VCO in the demodulator is replaced with a fixed oscillator, and the crystal oscillator which provides the reference for the 1st local oscillator is varied. Tuning requirements for the VCO to ensure carrier tracking are now reduced to typically 100ppm and can be provided by a voltage controlled crystal oscillator (VCXO). The problems with this technique are that:-

a) Vcxos tend to be more expensive to produce than fixed crystal oscillators and tend to have inferior phase noise and long term stability performance compared with fixed frequency oscillators.

b) In many systems the first conversion stage is often a self contained unit of reference oscillator, phase locked oscillator (PLO), and low noise amplifier (LNA). If a VCXO is used then it would be necessary to provide a tuning voltage or reference frequency up to the front end which adds to system complexity.

There are now available on the market inexpensive fixed frequency crystal oscillators that have proven vibration and static phase noise performance [Zeigler, 1988]. There would clearly be an advantage if a fixed frequency oscillator could be employed as a reference

source for the microwave local oscillators. Fig9.3 displays typical phase noise curves for a fixed crystal oscillator and VCXO with appreciable tuning range.

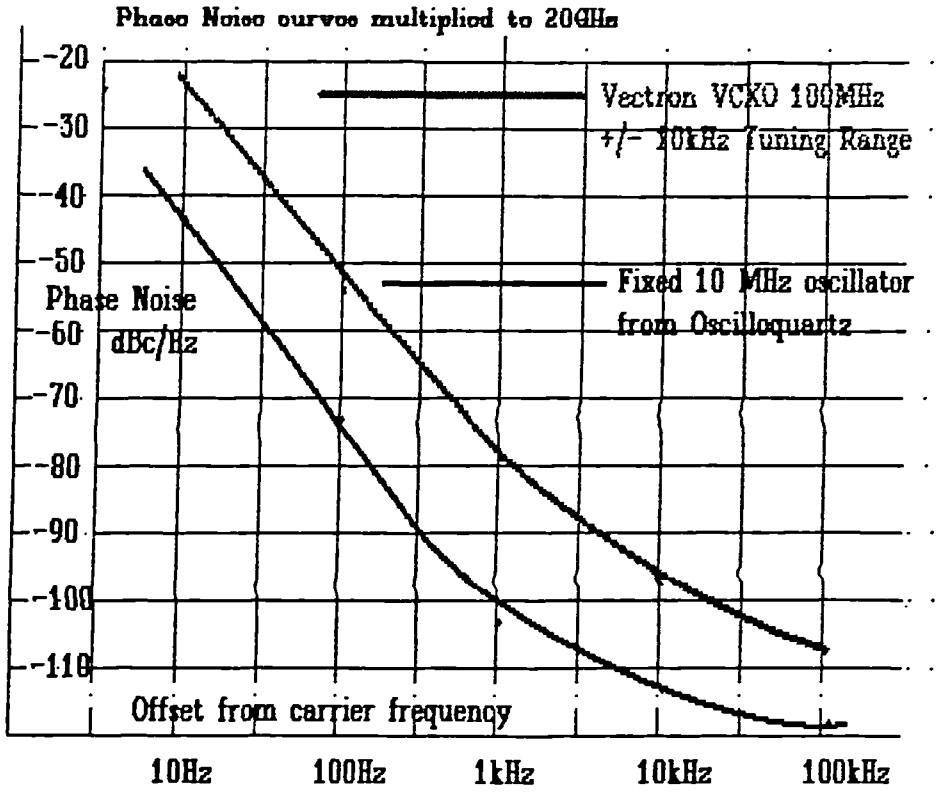


Fig 9.3 Comparison of a commercial VCXO and fixed frequency oscillator phase noise

9.2.2 Synthesiser logic devices

Many current synthesiser designs rely on the phase noise performance of digital dividers to determine the close to carrier phase noise [Rodhe, 1983]. A method has been described by the author in chapter 5 that avoids the problem of digital divider phase noise. However this method is only likely to yield advantages for synthesiser step sizes of 1MHz or higher. To implement the modulation techniques outlined in this chapter, finer step sizes are required. Methods of reducing the step size have been outlined in chapter 4.

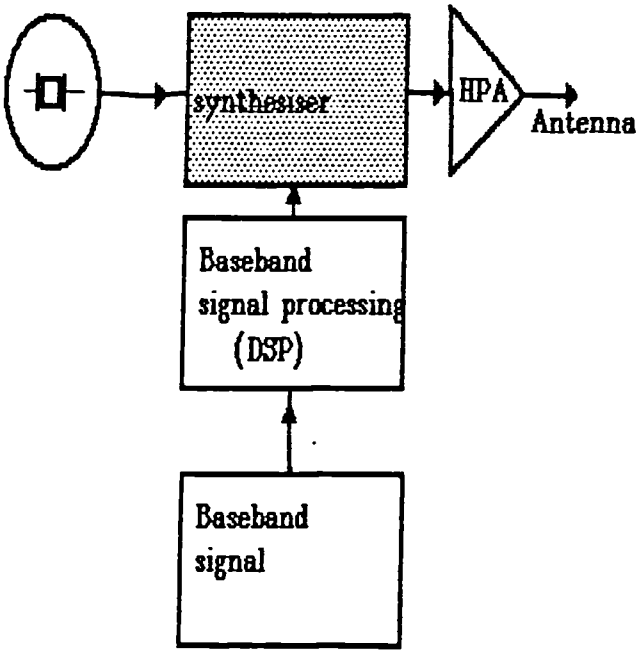
9.2.3 Synthesiser vibration performance

As stated in chapter 6 satellite modems will frequently have to operate in high vibration environments. Besides this they must not lose lock or give bursts of high BER when subject to moderate shock. Frequently the effects on performance are greater than static phase noise [Wilson & Tozer, 1989]. Unlike static phase noise there appears to be little quantitive data available on this subject. A computer simulation in chapter 5 predicts that a considerable reduction in vibration induced phase noise could be achieved by the use of

third order type three phase locked loops in the synthesisers. It is preferable however, to design the architecture so that wide loop bandwidths are possible in the PLLs.

9.2.4 System configuration performance tradeoffs

The multistage up- and down-conversion techniques typically used are complex, require critical alignment procedures, and are demanding upon screening requirements. A block diagram of a typical satellite communication transmitter is shown in fig9.4.



PROPOSED TRANSMITTER

Fig 9.4 Typical plan of a transmitter

A block diagram of a typical satellite communication transmitter multi-stage upconverter is given in fig9.5 which is followed by the high power amplifier stage (HPA). After each frequency conversion, notch filters and band pass filters are required to prevent spurious responses. In addition, each stage must be separately screened, and the synthesised local oscillators must in turn have separate screening.

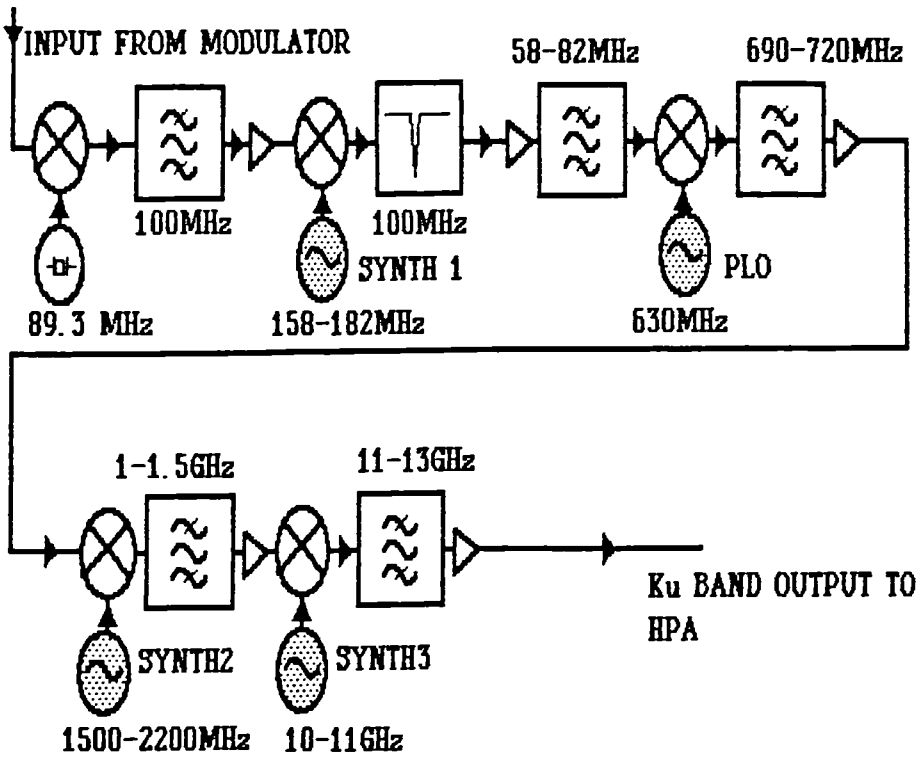


Fig 9.5 Block diagram of a typical satellite communication upconverter

One method of overcoming these difficulties is to combine the process of modulation, frequency generation, and up-conversion into one unit, the *synthesiser* in order to form an integrated transmitter as shown in fig9.6.

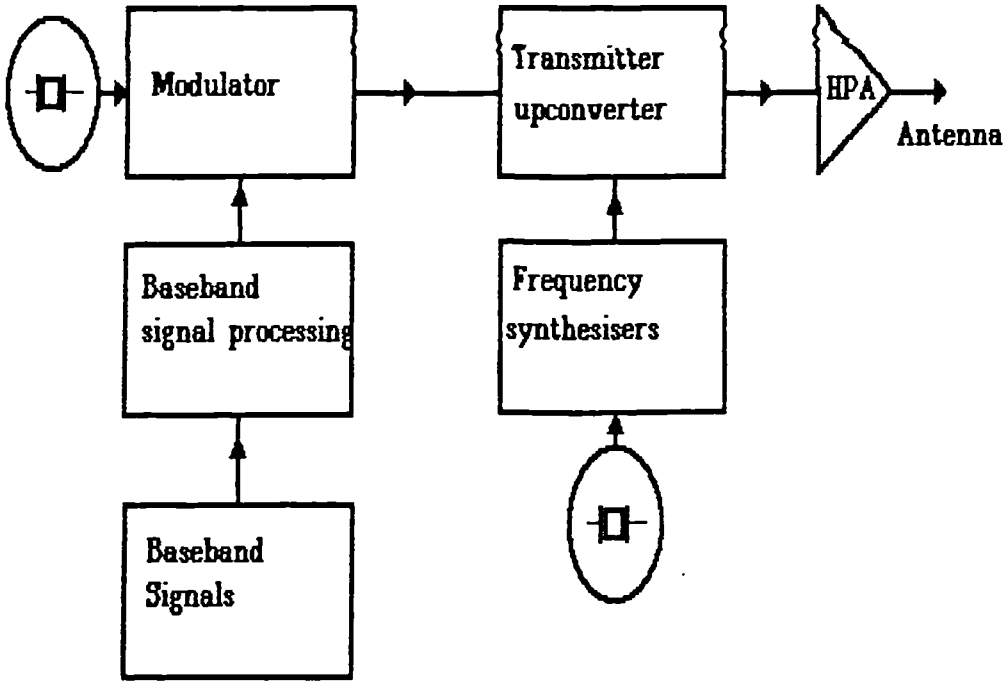


Fig 9.6 Block diagram of the proposed transmitter

The synthesiser itself therefore becomes the link between the digital baseband signal processing domain and the analogue radio frequency domain. This has several advantages:-

1) The synthesiser is moved from the periphery of the system, as shown in the shaded area of fig9.5 to the centre as in the shaded area of fig9.6, making it more justifiable economically to improve its performance.

2) If the final output frequency can be generated at the synthesiser then multi stage up conversion will not be required.

3) Accurate control of the modulation process can be achieved by connection of a digital signal processor (DSP) to the digital modulation input of the synthesiser.

4) The total number of local oscillators are reduced, therefore reducing the total number of phase noise sources (see §9.8.4.3).

With consideration of these points, a possible scheme for a simplified transmitter system will now be described.

9.3 An integrated approach to transmitter design

A block diagram of a typical satellite communication upconverter and transmitter has been displayed in fig9.5. This consists of many stages which must be screened from each other, therefore making it a relatively expensive item to produce, especially as demands on transmitter spurious levels are increasing [GCEL, 1990]. The possibility of employing the synthesiser to form the link between the analogue and digital sections of the transmitter has been made realisable by the application of digital circuits to synthesisers. One possible solution is the use of a PLL synthesiser in the form of the fractional *N* /digiphase technique. A major problem could occur due to the limited loop bandwidth used in these techniques. In FM radio speech channels a commonly used technique is two point modulation [Scott & Underhill, 1980]; in this technique, modulation is simultaneously applied to the VCO and the phase detector. When correctly adjusted, the PLL response is unaffected by the modulation. The following problems may arise in applying this technique to data systems:-

a) The data rate in many systems may approach that of the loop bandwidth of the PLL, therefore care would be required to maintain effective cancellation of the signal at the PLL.

b) It would be difficult to provide the accurate phase control required for high order digital modulation schemes such as QPSK and higher.

In chapter 8, direct digital synthesisers have been demonstrated that can attain low spurious signal levels. Use of the direct digital synthesiser (DDS) can now therefore be considered a realistic option. With a direct digital synthesiser, phase modulation may simply be provided by means of an adder at the output from the phase accumulator [McCune, 1987]. Response time is therefore no longer a problem, and accurate phase control can be achieved.

Use of this technique entails problems due to the limited output frequencies of direct digital synthesisers. It is not possible, as yet, to obtain an output directly at microwave frequencies from a DDS. However, work is at present being undertaken [Saul & Taylor, 1989] to increase the speed of the devices with a microwave DDS as the ultimate goal. The direct modulation suggested by McCune [*ibid*] would still require a conventional analogue upconverter to reach microwave frequencies. Jones *et al* [1989] suggested the use of the transfer phase locked loop to raise the DDS to microwave frequencies. Since the PLL phase detection frequency can be high, a wide loop bandwidth can be used, alleviating the requirement for two point modulation within the PLL. Unfortunately, by its very nature, only phase information can be transferred through the loop. Therefore only constant amplitude modulation schemes such as MSK (minimum shift keying) and FSK (frequency shift keying) can be employed directly with this technique as these modulation systems can be provided by phase variations only. Gaussian minimum shift keying (GMSK) is particularly suitable and has low sidelobe levels. Phase shift keyed modulation (PSK) schemes must normally be subjected to bandlimiting to avoid adjacent channel interference during transmission. Concomitantly, signal envelope variations occur. To enable bandlimited PSK modulation some means of providing the necessary amplitude variation at the output must be provided; this will be discussed in the following section.

9.4 A novel technique aiding integrated transmitter design

For an integrated approach to modulator, and transmitter design, some means of providing simultaneous phase and amplitude modulation of the signal is required [Davarian & Sumida, 1989]. Direct digital synthesis has the facility to enable accurate phase modulation of the signal as discussed in §4.4. This property enables DDS to be an ideal choice for the new integrated approach to transmitter design. Central to such an approach is the resolution of the modulation into PM and AM components. With DDS, an arithmetic multiplier can be placed after the PROM stored waveform map to provide AM by varying the level of the signal according to the baseband modulation Zavrel [1988]. There are however, the following disadvantages with this technique:-

1) Reduction of spurious free dynamic range due to rescaling of the DAC average AC level;

2) A linear upconverter is still required to transfer the amplitude modulation to the antenna output.

The first problem arises because the DAC range must now correspond to the peak signal level and not to the average signal level as when no AM is provided. This would correspond to loss in DAC dynamic range.

Illustrated in fig9.7 is a block diagram of a novel approach to these problems proposed by the author. The PM can be input direct to the synthesiser, and the AM components are input into an amplitude modulator placed after the synthesiser. Essentially the novel part of the improved modulation scheme proposed here transfers the amplitude modulation circuit to the microwave output of the modulator before the high power amplifier stage (HPA). PIN diodes can be used to provide the amplitude modulation, since the reactive component of the diode impedance is relatively constant with modulation.

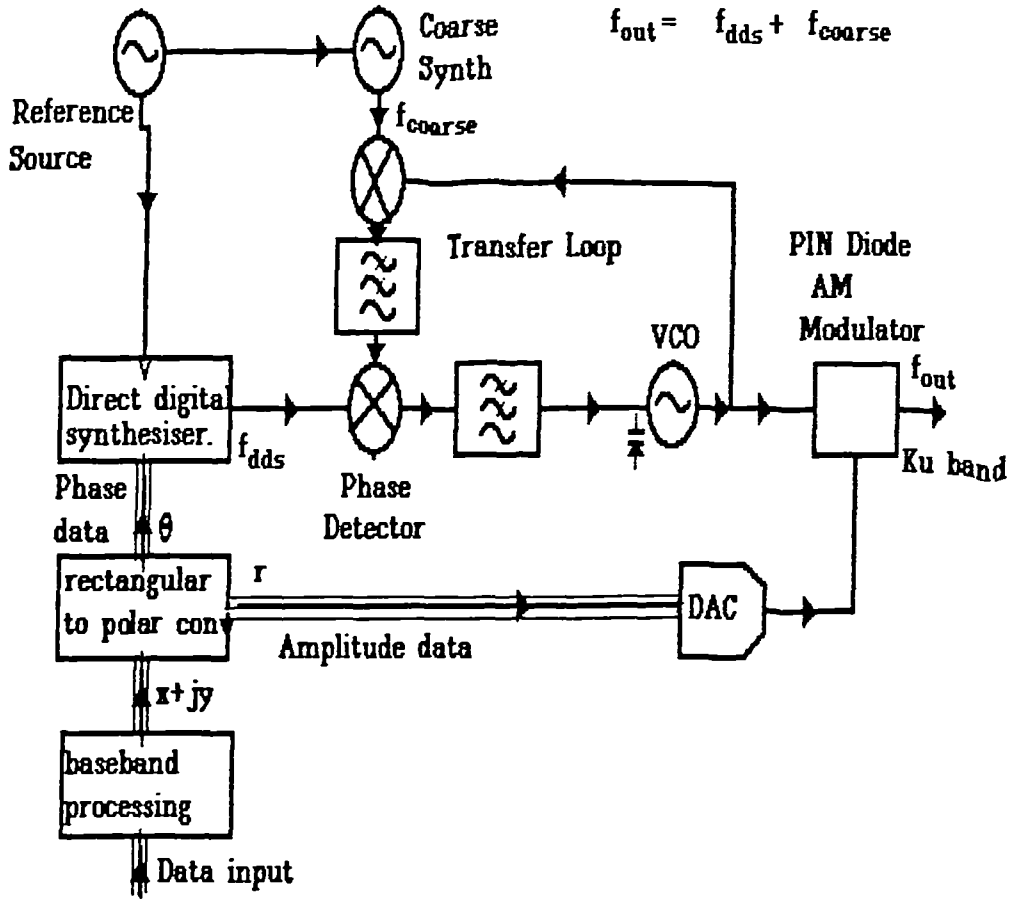


Fig 9.7 Combined modulator /synthesiser

The variation in phase shift through a PIN diode amplitude modulator is less than 5° for a 3 dB amplitude modulation at 18GHz [General Microwave, 1988]. This could be compensated for by providing a phase adjustment to the phase modulator. Baseband modulating signals must first be filtered and then input to a cartesian to polar converter in order to resolve the signal into phase and amplitude components. Such an operation could form part of the pre-modulator baseband signal processing normally undertaken by a DSP. A problem still exists however, in that the amplitude modulation introduces some undesirable phase modulations. Therfore with bandlimited PSK, a modulation scheme should be chosen such that amplitude variations are kept to a minimum. For example, Signal Processing Worksystem (SPW) simulations are given here for bandlimited QPSK and bandlimited offset QPSK so that their amplitude variations can be compared. A block diagram of an SPW simulation of a bandlimited offset QPSK modulator is given in fig9.8.

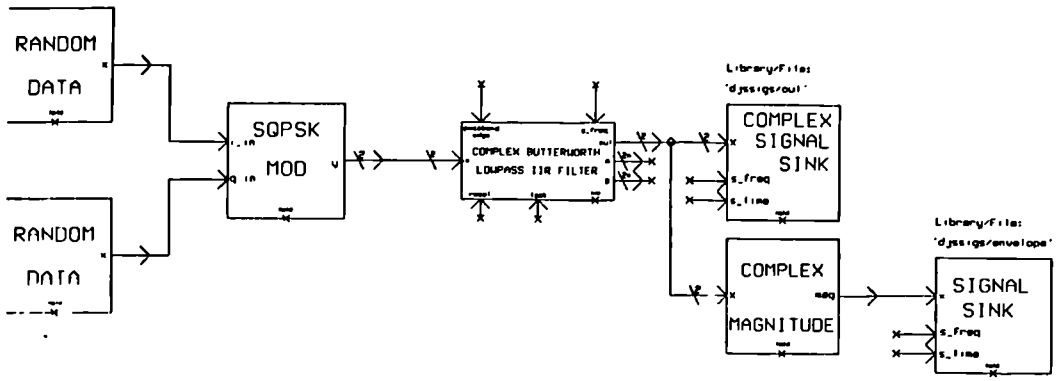


Fig 9.8 Block diagram of bandlimited offset QPSK SPW simulation

The filter provides a lowpass bandwidth of 1.5 times the data rate. A constellation diagram of such a simulation is given in fig9.9, and the envelope variation given in fig 9.10; the latter diagram indicates that envelope levels never fall to zero.

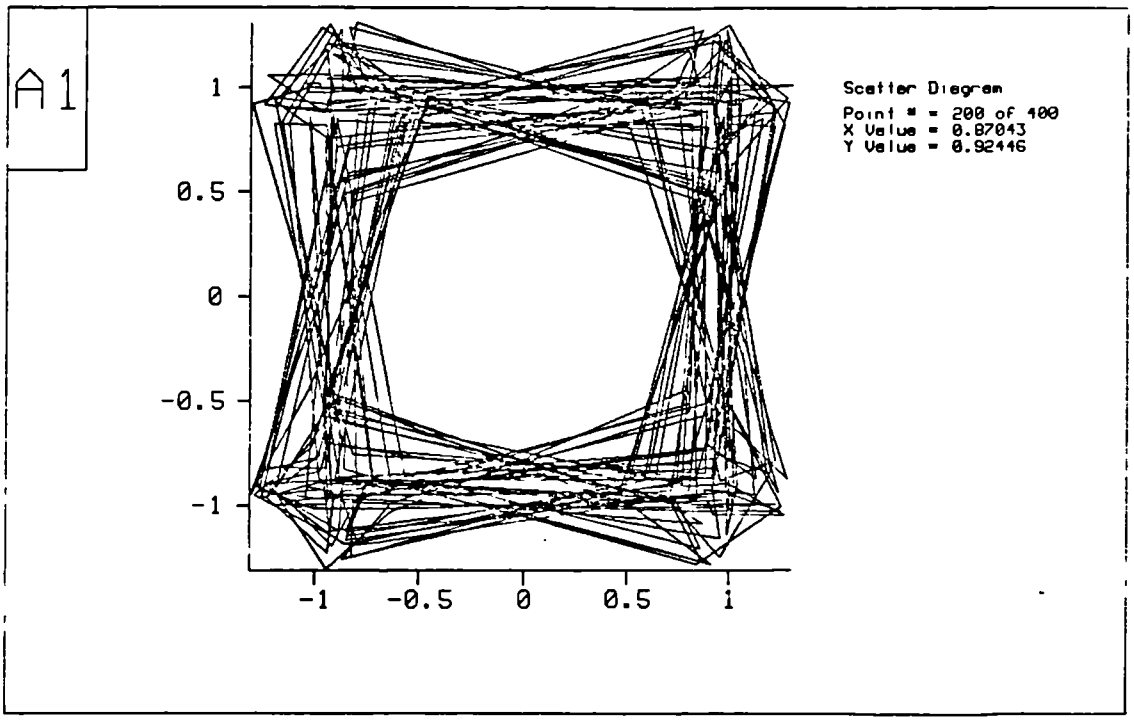


Fig 9.9 Constellation diagram given by bandlimited offset QPSK SPW simulation

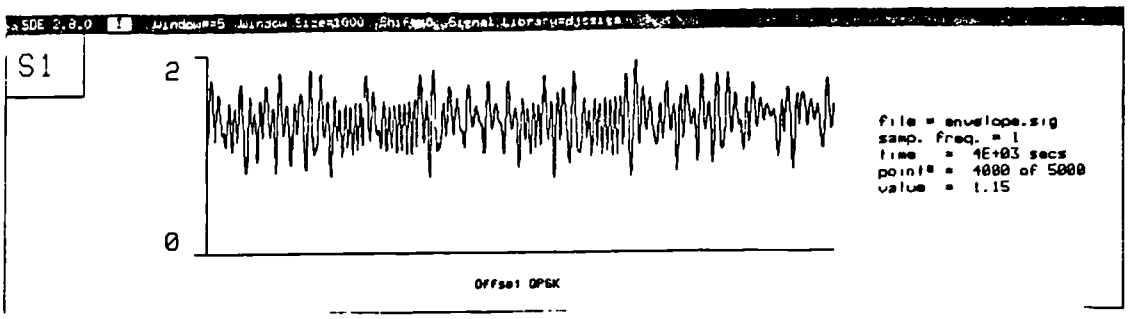


Fig 9.10 Envelope variation at the output of bandlimited offset QPSK SPW simulation

An idealised form of the constellation diagram is given in fig9.11.

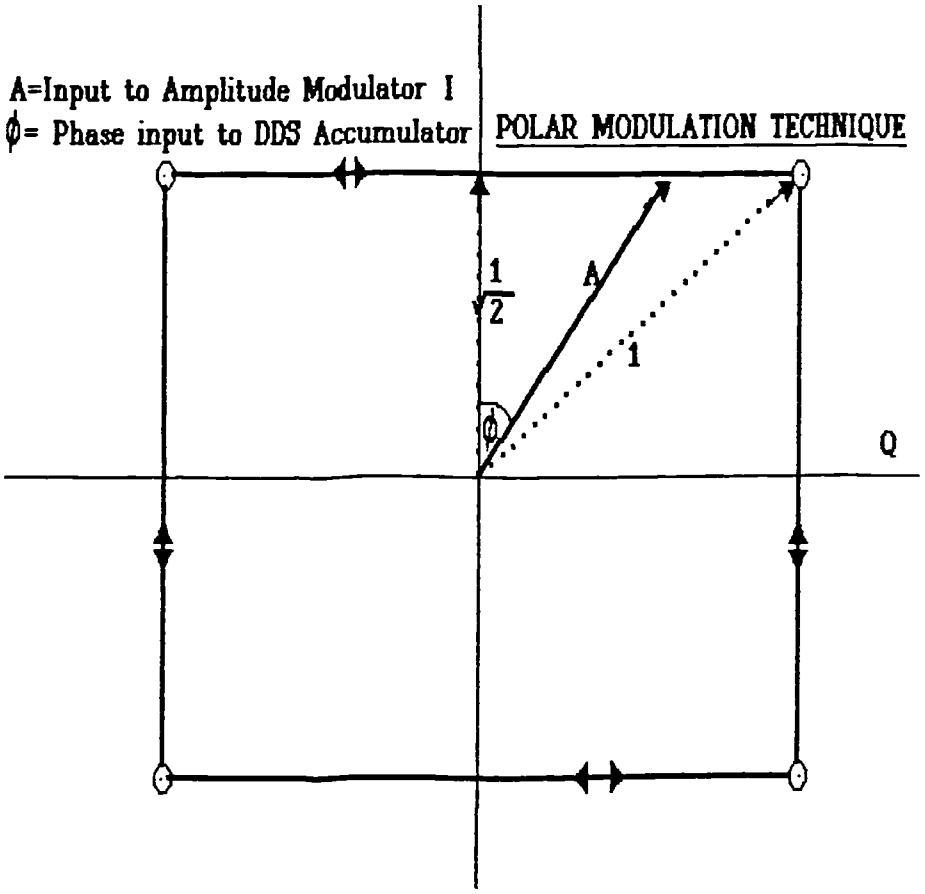


Fig 9.11 Idealised offset QPSK constellation diagram

The actual trajectory of the signal is displayed by means of the thick solid lines. Overall signal variation can be easily shown by inspection to be $\sqrt{2}$. This means that the total amplitude variation for offset QPSK is 3dB. Also it can be noticed that in fig9.9 and fig 9.11 there are no crossings through the centre of the constellation. For comparison, a similar simulation was run of straight QPSK. Such a simulation results in the constellation plot of fig9.12.

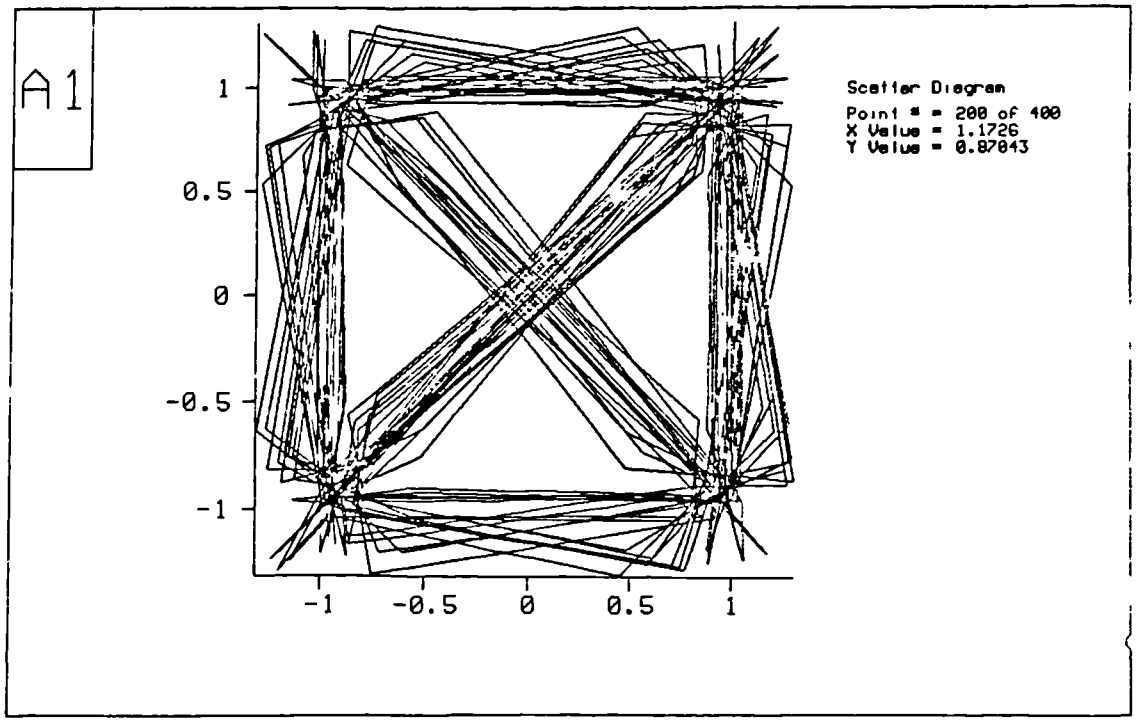


Fig 9.12 Constellation diagram given by bandlimited straight QPSK SPW simulation

It can be noticed that zero crossings are now present. For straight QPSK, the corresponding variation will be infinity as there are transitions through the centre of the constellation diagram. The envelope plot of fig9.13 shows that indeed this is the case.

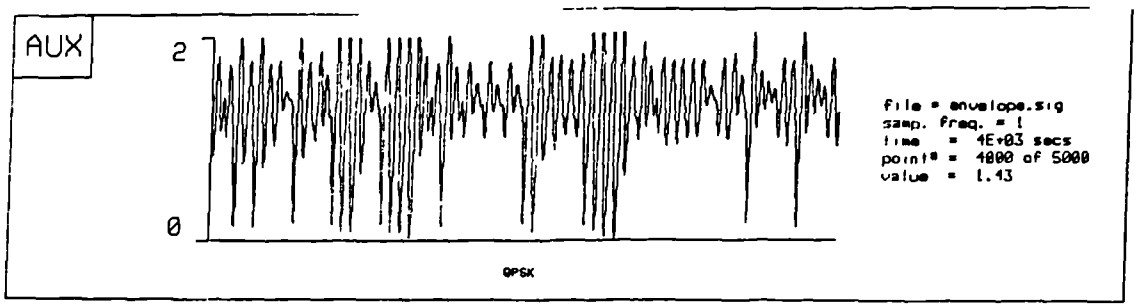


Fig 9.13 Envelope variation at the output of bandlimited straight QPSK SPW simulation

Infinite amplitude variations increase phase variations to approximately 50° as found from typical PIN diode attenuator data sheets [General Microwave, *ibid*]. Therefore the method is better suited to modulation schemes with restricted amplitude variation, such as offset QPSK. Although this appears to be very restrictive in terms of modulation schemes, such schemes also enable more efficient usage of power amplifiers.

9.5 Alternative Approaches to Receiver design

Having considered a method of simplifying transmitter design, alternatives to receiver design must be considered. Unfortunately, the design of a receiver will not be as straightforward as the transmitter case for the simple reason that the gain is much higher. A typical receiver gain from antenna to demodulator is 90dB, as opposed to 50dB with a transmitter. Overcoming this gain problem requires some intermediate frequency conversion, and hence image problems arise.

The receiver section of a data system can however, be very much simplified by the use of DSP techniques. There are several options available for DSP demodulators.

a) Baseband sampling

The received signal is downconverted to baseband at the IF mixer as shown in fig9.14.

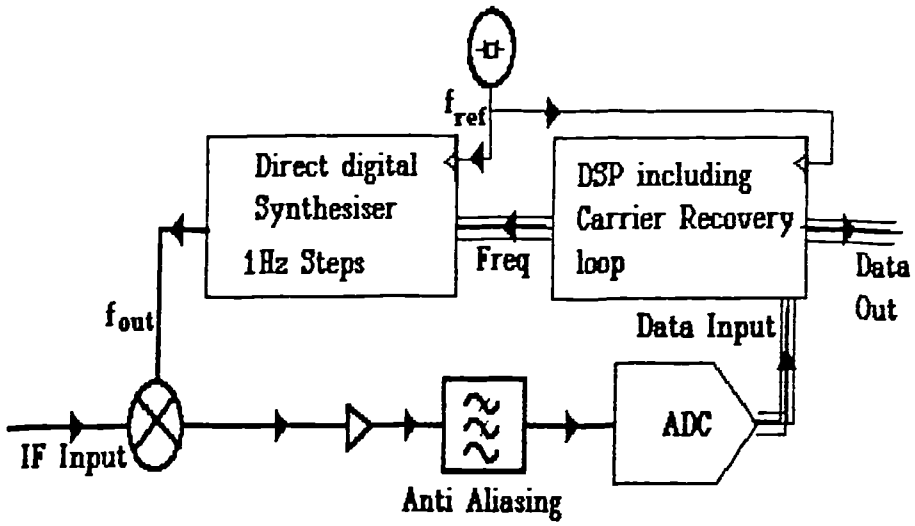


Fig 9.14 Direct digital synthesiser and DSP in a data receiver

Carrier recovery then can be achieved by means of a Costas loop [Britten & Martin, 1989]. Although Costas loops can be implemented in a DSP, a VCXO will be required to provide interpolation between the synthesiser frequency steps and this must be external to the system. A fine stepping frequency synthesiser can then be used as a local oscillator. The anti- aliasing filter must have a low pass function. Unfortunately with this approach, DC offsets can degrade performance [*ibid*] and an analogue VCXO would be required. Implementing a Costas loop also requires that a quadrature mixer is used for the downconversion [Holmes, 1982], the advantage of which is that image rejection is no longer a problem.

b) Quasi baseband sampling

Quasi baseband sampling principally aims to remove the problem of DC offsets. A block diagram of a quasi baseband sampling system is similar to the baseband system displayed in fig9.14.

The difference is that the signal is downconverted to nearly baseband, ie. much less than the data rate [Heron, *ibid*]. A carrier gyration loop [Marston, 1987], which is a mathematical form of a carrier recovery loop, is used within the DSP to track and demodulate the signal. Any frequency synthesiser used for tracking must have fine enough step size to avoid introducing significant phase transients into the gyration process. The gyration can only operate on a complex baseband signal so a quadrature downconverter must be used even for a BPSK signal. A major advantage of this approach is that the VCXO is no longer required. Image rejection is still not a problem as the signal is near baseband. AC coupling can be used thereby eliminating problems of DC offsets. The disadvantage is that a more complex mixer arrangement is required to provide the complex signals.

c) IF or bandpass sampling

With bandpass sampling, the IF signal is converted to baseband by a pre-DAC sample and hold which samples at a subharmonic of the IF frequency [Vaughan, 1991]. If a complex modulation scheme such as QPSK is used, then quadrature sampling would be necessary to obtain the I and Q samples. With quadrature sampling, the Q sample is taken at a time delay corresponding to a quadrature phase shift at the IF frequency after the I sample. The pre-conversion bandpass filter becomes the anti-aliasing filter for the sampling rather than the more usual lowpass anti-aliasing filter. This anti aliasing filter is critical to preserving the signal to noise ratio of the down converter as adjacent signals and noise at multiples of the sampling frequency are aliased by the sampling process into the wanted channel. A particular problem can arise if strong adjacent channel signals are present. The baseband signal at the output of the sample and hold can be input directly to the DACs and the remainder of the processing accomplished digitally. FFT algorithms could be used to assist carrier recovery [Inmos, 1989], in order to speed up acquisition. There is much scope for further investigation on this subject. A fine stepping synthesiser could be accomplished with digital circuitry within the DSP [Plessey, 1988]. This would take the form of a DDS with no DAC present at the output. Analogue local oscillators used in such a system would thus be coarse stepping resulting in much simplification. The advantage of such a system would be the increased flexibility, but the disadvantage at present is the prohibitive cost of the high speed signal processing components and the possibly stiff requirements for an anti-aliasing filter. All this may change however, in the future and these areas require further investigation.

9.6 Summary of integrated receiver and transmitter design techniques

Concern was raised by the author in §9.2.4 about the complexity of typical transmitter upconversion equipment. The author has suggested a method of taking advantage of the latest synthesiser developments to simplify the transmitter. In addition to the use of new synthesiser technology suggested in chapter, the author proposed the use of a novel 2 point modulation technique to eliminate upconversion and make feasible a fully integrated transmitter design.

The receiver was not so readily simplified. A brief study of receiver techniques was undertaken to investigate the feasibility of some simplification. The principal obstacle to simplification is the necessity to preserve the real and imaginary components of the signal. A firm favourite at the present appears to be the quasi baseband sampling receiver, a

critical element of this approach is a synthesiser of very fine step size. However, direct digital synthesis could be used to advantage to provide a tracking synthesiser to replace the VCO in the demodulator.

One advantage of an integrated approach to receiver and transmitter design is the reduction of the total number of local oscillators contributing phase noise to a complete satellite link. In order to assess any advantage of the integrated techniques, comparison must be made with conventional transmitter receiver techniques by means of a phase noise link budget analysis as described in §6.4.2. Such an analysis is carried out in the remainder of this chapter.

9.7 Link Budget Analysis for Phase Noise

9.7.1 Introduction to link budget analysis

All the synthesiser techniques discussed in chapters 4, 8 and 9 must be evaluated in terms of system requirements. In particular, it would be of interest to demonstrate if any possible gain in system performance can accrue from the use of the integrated design techniques discussed earlier in this chapter. Chapter 6 exposed that a requirement exists for a phase noise link budget to be concomitant with the usual communications link budget. Before carrying out a complete link budget analysis however, further considerations and improvements to synthesiser design were reported in chapters 7 to 9 so enabling the availability of a full range of synthesiser phase noise profiles.

Link budgets are analysed for a selection of satellite system configurations, coherent modulation techniques and synthesiser phase noise levels. One salient feature of this section is a demonstration of the effect of phase noise on FEC (forward error correction), commonly used in satellite data links. Convolutional coding and Viterbi soft decision decoding is the FEC scheme studied in this section, hereafter referred to as "Viterbi decoding". The analysis is performed by a Pascal program written by the author that incorporates a unique feature necessary for accurate phase noise link budget analysis. In addition to providing a demonstration of benefits gained to satellite system performance by applying the synthesiser design techniques in this thesis, the link budget analysis program could be useful in itself as a tool for system design. The program had to be sufficiently flexible to enable a variety of local oscillator and synthesiser architectures to be incorporated into the analysis.

9.7.2 Methodology

9.7.2.1 Program functional description

The function of the analysis program packages is to calculate the degradation in sensitivity for a bit error rate (BER) specified by the user. Before commencement of the analysis, phase noise and offset from carrier frequency data points are input into an preliminary database for each local oscillator in the system. This database is accessed by a database management program that is not discussed here. On completion of the analysis, a plot of degradation in sensitivity is obtained against data rate, with the ratio of carrier recovery loop bandwidth to data rate as a parameter. Data rate is plotted logarithmically on the horizontal axis. Degradation is plotted in dB on the vertical axis.

A value of phase jitter σ_{px} must be obtained from the integration programs for each local oscillator in the link. The resultant phase jitter at the demodulator is then the RSS of all phase *jitter contributions* as described above. A modified BER curve can then be plotted which accounts for this phase jitter. For a constant BER, the E_b/N_0 can be compared with the ideal BER curve and an estimate of the BER degradation obtained for the phase errors. The analysis program automates this process and plots the expected degradation over a wide range of data rates.

9.7.2.2 Structure chart (Tree Diagram)

The program will be described in this section by means of the structure chart of fig9.15. This diagram illustrates how the various Pascal units are called by each other and by the main program. Detailed listings of code and documentation will be given in appendix 4. Central to the structure chart is the main analysis program. This runs in a loop which repeatedly increments the data rate in a logarithmic fashion and analyses the link for each value of data rate. This main program calls various units in turn. The input unit controls the updating of the database each time the program is initiated. Output, controlled by the appropriate unit, is sent to the screen and optionally gives a hardcopy from a printer. Each local oscillator phase noise sideband is converted into a recovered carrier phase jitter contribution by means of an appropriate integration unit and its phase noise database. The degradation is calculated within the BERCALC unit. An additional unit is called from within the BERCALC unit, the thermal noise unit, which calculates the thermal noise jitter contribution.

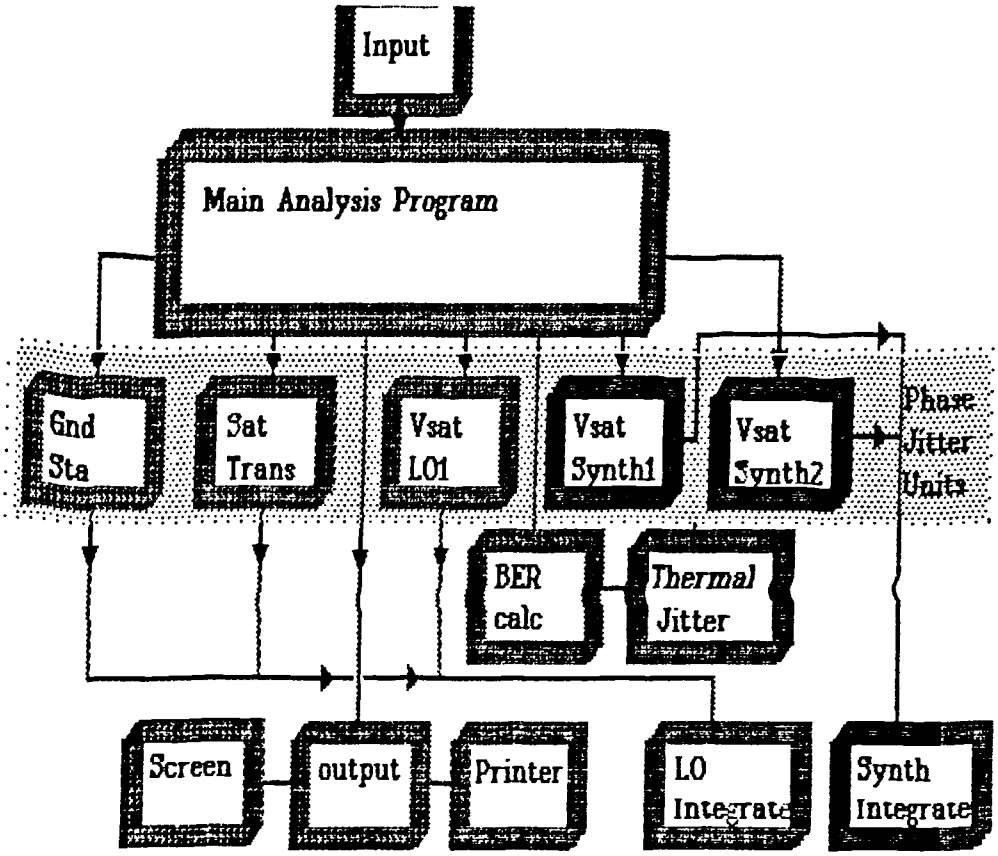


Fig 9.15 Structure chart for phase noise link budget program

9.7.2.3 Bit Error Rate estimation unit

As discussed in §6.4.2, a value of phase jitter σ_{px} must be obtained from the integration programs for each local oscillator in the link. The resultant phase jitter at the demodulator is then the RSS of all phase jitter contributions as described above. A modified BER curve can then be plotted which accounts for this phase jitter. In chapter 6, a program was discussed that produced a graph of estimated bit error rate against calculated phase jitter. This program forms a unit which can be incorporated into the main analysis program. A modification had to be carried out to enable calculation of the loss in sensitivity from the BER phase jitter curves. Fig 9.16 shows an example curve selected from those of fig 6.3 to illustrate this process. For a constant BER, a horizontal line is drawn across the graph. An intersection of this line with the ideal BER curve occurs at point **A** and with the modified BER for finite phase jitter at point **B**. Sensitivity degradation is represented by the distance from **A** to **B** on the horizontal axis.

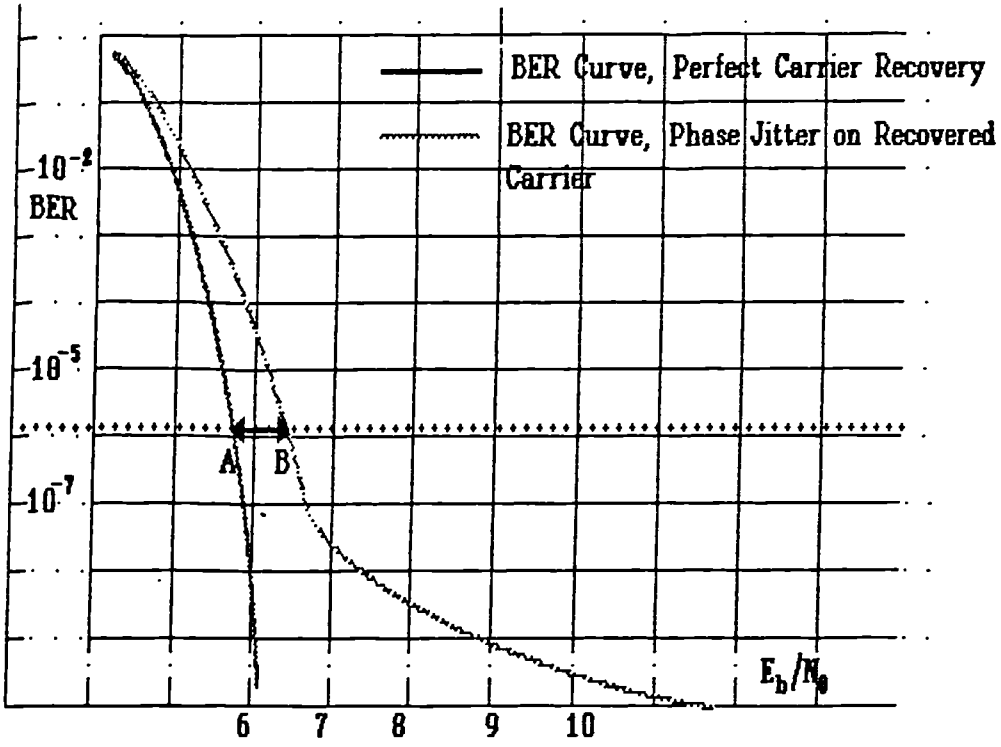


Fig 9.16 · Example BER curve showing calculation of phase noise degradation of link budget

9.7.2.4 Thermal noise jitter unit

Another unit calculates a figure for the thermal noise jitter variance in radians as a function of carrier loop bandwidth, input filter bandwidth and E_b/N_0. This unit uses the thermal noise calculations referred to in §6.3.1.3 and is called by the BER calculation unit for the reasons which will be elaborated in §9.7.2 below.

9.7.2.5 Phase noise jitter units

A phase noise jitter unit, called from the main program, will exist for each local oscillator in the system. Its function is to call up the appropriate local oscillator data base and integrate the phase noise sidebands to give a value for the phase noise jitter. As each value of phase jitter is returned to the main program, a test is carried out to establish wether the cumulative phase jitter is likely to result in a degradation value off the scale of the output plot. If this is the case, integrations are discontinued to avoid wasting CPU time calculating values of degradation that are excessive to be of use. Each phase jitter unit calls either of two phase noise integration units depending whether the synthesiser architecture is known or just the phase noise curve.

9.7.2.6 Phase noise integration

As discussed in chapter 6, an integration must be formed of the phase noise sidebands modified by the $|E(s)|^2$ response of the carrier recovery loop. This integration is performed numerically by Simpson's rule in the analysis program. If Simpson's rule is applied without modification under the phase noise curves, a large number of steps would be required. For example, if the CRL loop bandwidth is 1/1000 of the Data Rate then 10000 steps would be required for an accurate integration. A more efficient method is to apply the summation rule and integrate over each decade:-

$$\int_{f_1}^{f_2} |E(s)|^2 df = \int_{f_1}^{10f_1} |E(s)|^2 df + \int_{10f_1}^{10^2 f_1} |E(s)|^2 df + \ldots\ldots \int_{10^n f_1}^{f_2} |E(s)|^2 df \qquad (9.1)$$

In this case the number of steps can be reduced to 80 with little degradation in accuracy. This method makes use of the fact that the phase noise is generally higher close to carrier.

In each phase jitter analysis unit, there are a choice of two integration units to cover the two cases of phase noise data input that could arise as described in §6.4.3:-

9.7.2.7 Integration unit 1: Measured phase noise

A logarithmic interpolation is taken between the phase noise points and an integration performed. Logarithmic interpolation is used because phase noise specifications are frequently presented in logarithmic form. *In this case, data is entered into the program in* logarithmic amplitude form. For local oscillators, §3.3.5 demonstrated that phase noise can be represented as a reciprocal polynomial series. A straight line is then taken between two data points as can be seen from fig 9.17. An area representing the phase noise integration is shown by the shading under the phase noise curve.

Between the data points, the 1 Hz intercept point c and the slope of the graph m are related to the extrapolated logarithmic power by:-

$$\log_{10}(\mathcal{L}(f)) = m \log_{10} f + c \qquad (9.2)$$

In order to perform the integration, the logarithmic phase noise sideband power, $\log_{10}(\mathcal{L}(f))$ must be converted to actual sideband power, $\mathcal{L}(f)$. Thus by taking antilogarithms of equation (9.2) we obtain the equation used in the noise integration process:-

$$\mathcal{L}(f) = mf + 10^c \qquad (9.3)$$

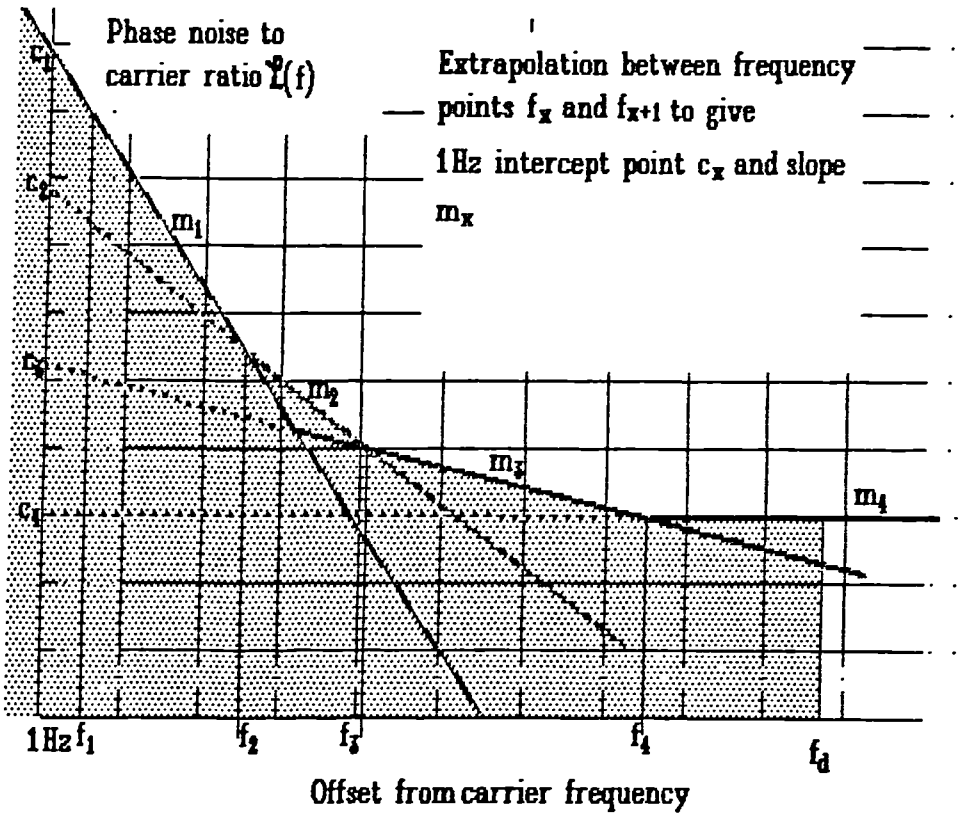


Fig 9.17 Integration of local oscillator sidebands.

When performing the integration, the program begins at the left of fig 9.17 and progresses to the reciprocal of the data rate, the data frequency, f_d. Extrapolation is calculated between the two database points (f_1 to f_5) which lie immediately either side of the current calculation point on the frequency axis. Calculation of the 1 Hz intercept point c_x and the slope m_x is undertaken between frequency points f_x and f_{x+1}. The slope and intercept factors are used to obtain the extrapolated power at the current integration calculation point. The integration is complete when the current calculated point equals the data rate.

9.7.2.8 Integration unit 2: Synthesiser architecture

An integration unit was written for cases where the synthesiser architecture is known for the local oscillator. It was assumed to be a single loop PLL synthesiser such as shown in fig 5.32 or that one PLL predominated, although the program could be readily modified for other forms of synthesis. For the divider and phase detector noise, a third order type 2 transfer function is assumed [Wilson & Tozer, 1989]:-

$$H_{syn}(s) = \frac{\omega_n^2 + 2\zeta\omega_n s}{\Gamma s^3 + s^2 + 2\omega_n\zeta s + \omega_n s} \qquad (9.4)$$

where ω_n is the loop damping factor, s is the complex frequency variable, ζ is the damping factor, and Γ is the post loop filter time constant.

VCO phase noise is multiplied by the synthesiser PLL error function, $E_{syn}(s)$. In the design study undertaken in this chapter, the third order response is approximated by the second order type 2 error response. This error function is given by:-

$$|E(s)|^2 = \frac{\frac{\omega^4}{\omega_n^4}}{1 + \frac{(4\zeta\omega^2 - 2)\,\omega^2}{\omega_n^2} + \frac{\omega^4}{\omega_n^4}} \tag{9.5}$$

A diagram illustrating the contributions to single loop synthesiser phase noise and the effect of integrating the sidebands is given in fig9.18. The solid line indicates the composite phase noise of the synthesiser.

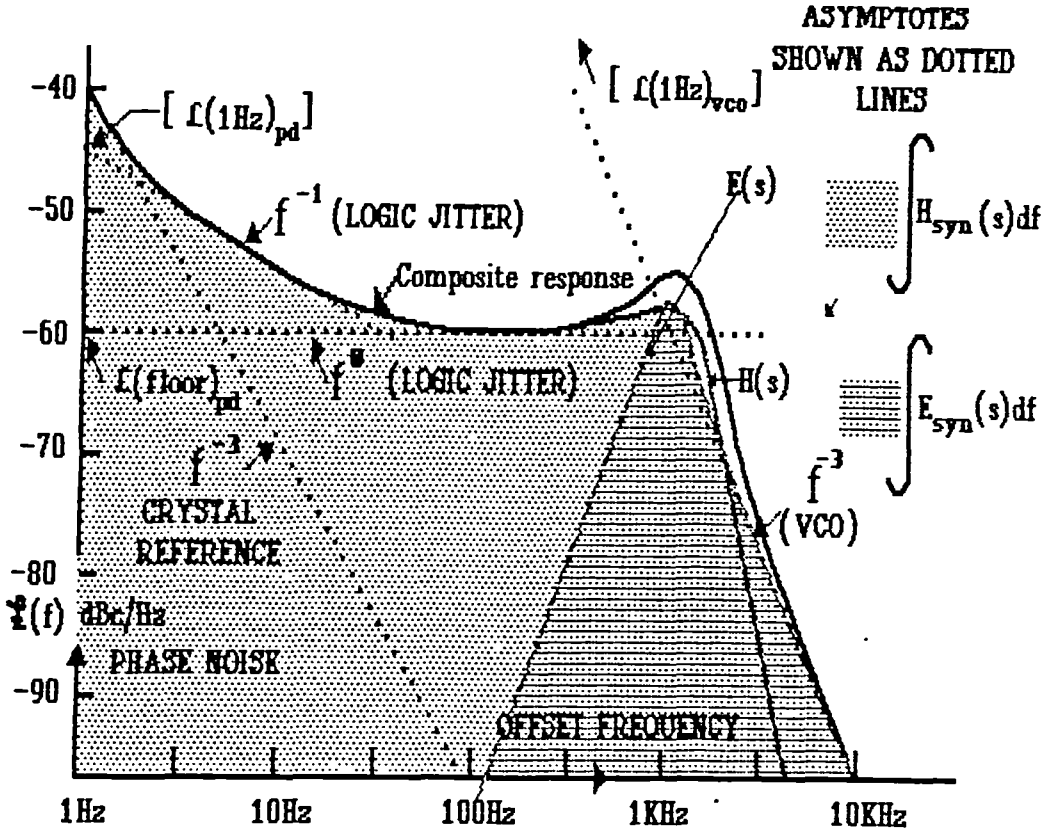


Fig 9.18 Phase noise integration of PLL synthesiser sidebands

At lower offset from carrier frequencies, this composite phase noise is approximately equal to the reference noise transferred through the loop. §5.7.2.4 described the sources of phase noise from components in this type of synthesiser. The components of the synthesiser loop that contribute phase noise multiplied by $H_{syn}(s)$ are shown in the shaded section of fig9.18. Components in the unshaded section are multiplied by $E_{syn}(s)$. Phase dividers and phase detector noise will have contributions from $1/f$ noise and a

wideband frequency independent noise floor. The wideband noise is given by equation (5.45) in §5.7.2.4. The composite noise from a single loop PLL can be shown to be [Wilson & Tozer, *ibid*]:-

$$\mathcal{L}(f_m)_{tot} = H_{syn}(s)B\left(\frac{\mathcal{L}(1\text{ Hz})_{pd}}{f_m} + \mathcal{L}(\text{floor})_{pd}\right) + E_{syn}(s)\frac{\mathcal{L}(1\text{ Hz})_{vco}}{f_m{}^3} \qquad (9.6)$$

Equation (9.6) is formed from the various phase noise power relationships for the different components within the synthesiser loop. Digital dividers and phase detectors have $1/f$ and frequency independent contributions to the noise densities. Voltage controlled oscillators as discussed in §3.3.6 have predominantly $1/f^3$ phase noise profiles close to the carrier. $1/f$ contributions of PLL digital devices in the synthesisers are accounted for in the first term. Such noise of dividers and phase detectors is a subject lacking exposure in published literature. *Measurement of these levels are therefore* required for a particular synthesiser configuration. The term $\mathcal{L}(1\text{ Hz})_{pd}$ refers to the 1 Hz intercept point ($1/f$ noise extrapolated down to 1 Hz). Also multiplied by $H_{syn}(s)$ is the second term of the equation giving the wideband noise floor of the digital devices $\mathcal{L}(\text{floor})_{pd}$. VCO noise appears in the third term and is represented by $\mathcal{L}(1\text{ Hz})_{vco}$, again referring to noise extrapolated back to 1 Hz. VCO phase noise, unlike divider and detector noise is reduced by the feedback loop gain of the PLL. Therefore, the VCO phase noise is multiplied by the loop error function $E_{syn}(s)$, which is related to the loop transfer function by:-

$$E_{syn}(s) = 1 - H_{syn}(s) \qquad (9.7)$$

In fig 9.18, the effect of the third term is the boundary of the dark shaded area. It can be noticed that the ultimate rate of attenuation for a third order type 2 loop $H_{syn}(s)$ is 40 dB/octave, whereas the E(s) roll off is determined by the phase noise of the VCO, that is 30 dB/octave at the most. The phase noise integration takes the area under the combined response curve.

Integration of $\mathcal{L}(f_m)_{tot}$ up to the data rate results in a value of phase jitter, σ_{px} for that particular local oscillator.

9.7.3 Parameters and Program steps

Steps taken by the analysis program will now be described. Plots of sensitivity degradation are obtained over a range of data rates using the carrier recovery loop bandwidth as a parameter. In this way, the optimum carrier recovery loop bandwidth can be given for a particular configuration. Program steps taken during the analysis are as follows:-

1) Calculation of the phase jitter contribution at the demodulator due to each local oscillator in the system as a function of data rate and CRL bandwidth;

2) Calculation of the perfect recovered carrier E_b/N_0 for the specified BER;

3) Calculation of the additive thermal noise contribution to the demodulator jitter for the above level of E_b/N_0;

4) Find the increase in E_b/N_0 necessary to attain the desired BER with the combined RSS of all the above calculated jitters;

5) Re-calculate the additive jitter contribution (step 3) with the new value of E_b/N_0;

6) Iteration is performed on steps 4 and 5 until the desired level of accuracy is attained;

7) Subtract the modified value of E_b/N_0 in dB from the phase noise free channel E_b/N_0 to obtain the degradation in sensitivity.

A unique feature of this link budget analysis program incorporated by the author is the ability to include the additive jitter contribution calculation in an iteration loop that calculates the degradation in sensitivity in the presence of phase jitter for a user defined BER. This is necessary because a reduction in sensitivity forces an increase in input signal to noise ratio, thus giving a reduced value of thermal jitter σ_t. Subsequently, this modified value must be used in the calculation of the total phase jitter σ_T for the next iteration.

As the BER curves are very steep, especially when Viterbi decoding is used, care has to be taken with the iteration algorithm. The standard iteration algorithms, such as Newton-Raphson's [Dalquist & Bjorck, 1974], implemented elsewhere in this thesis, may fail if used alone. Even the bisection method may give catastrophic failure when implemented here. A not very optimal, but very reliable method used here is to increase the E_b/N_0 in 1 dB steps until the specified BER is exceeded. After overstepping the desired BER, the next lower 1 dB step is selected and E_b/N_0 is increased in 0.1 dB steps until the specified BER is again reached. The Newton-Raphson algorithm could be applied after the 1 dB stepping stage, to greatly improve accuracy. However, since since such a level of accuracy is out of proportion with the remainder of the link budget, it is difficult to justify the increased complexity in the program.

Because of the inclusion of the thermal noise jitter calculation in the above described iteration, the thermal noise jitter unit is called from within the BER unit, rather than from the main program as with the local oscillator jitter units. The latter units give phase jitters that are independent of signal levels therefore it is not necessary to include them in the iteration loop.

9.7.4 System Configuration

9.7.4.1 Architecture

A block diagram of a typical one way satellite communication data link system is shown in fig9.19.

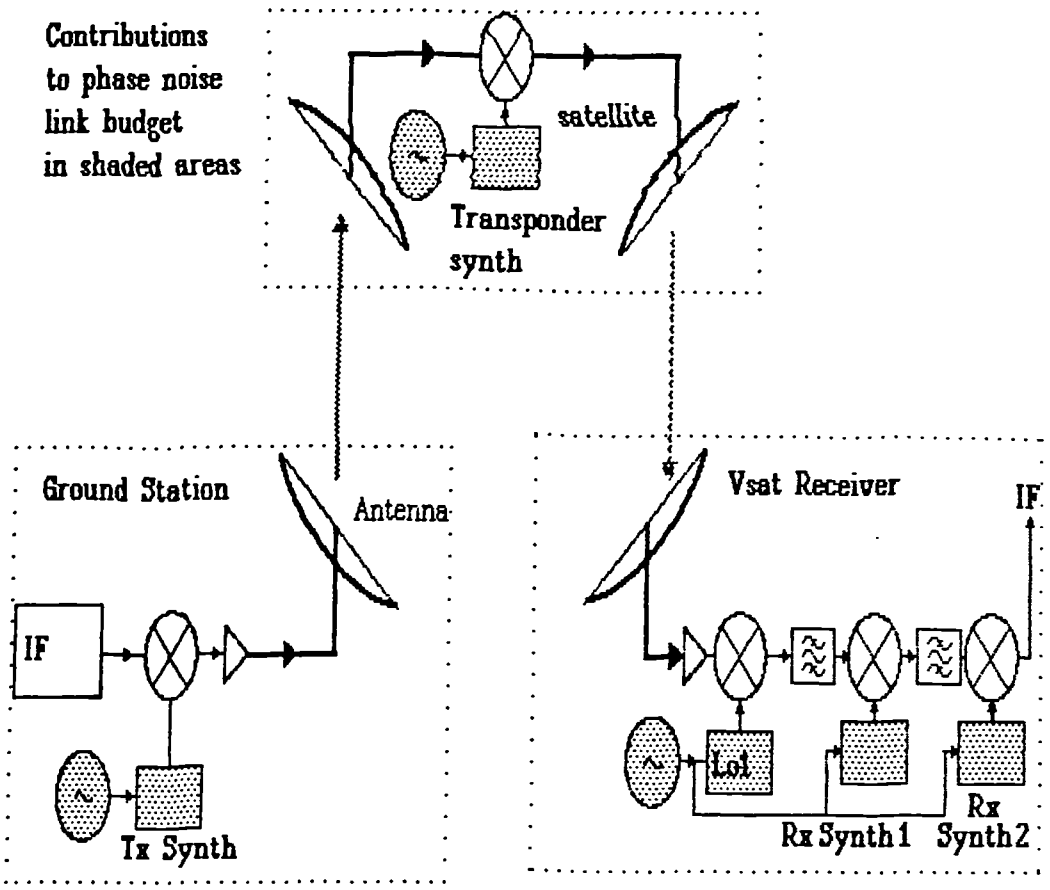


Fig 9.19 Block diagram of typical SATCOM 1-way link

Major phase noise contributors that are analysed by the phase noise link budget program described in chapter 9.7 are shown shaded. Fig9.19 relates to a receiver with split synthesis local oscillators. Each local oscillator will have its phase noise contributions entered separately. For the ground station and satellite transponders, the phase noise of the station or transponder are usually considered as a whole, rather than considering each separate local oscillator. Therefore the complete phase noise specification for the grand station and transponder are entered.

The link configurations analysed were as follows:-

1) Hub station to VSAT;

2) VSAT to Hub station;

3) VSAT to VSAT.

In the case of VSAT to VSAT, to a large extent the arrangement of oscillators is symmetrical, in the transmitter from IF interface up to carrier frequency and *vice versa* in the receiver. It may help to initially describe these in terms of the receiver configuration. Two broad classes of receiver configurations will be considered either with a single synthesiser feeding the first local oscillator, or synthesis split between the local oscillators.

9.7.4.2 Receiver local oscillators - Split synthesis

An example of a split synthesis receiver is shown in fig4.6 of §4.2.3. The receiver downconverter system was analysed by means of the programs described in §9.7. The first local oscillator achieves down-conversion from the carrier frequency to a suitable wide-range IF, perhaps 70 or 700MHz. It is assumed to be a fixed tuned oscillator as discused earlier in this thesis, and will be either a free running DRO as used in TVRO low noise blocks (LNBs), or some form of phase-locked oscillator locked to a crystal oscillator. Examples of the phase noise of these two oscillators at Ka band are shown in fig9.20 for a free running DRO and later in fig9.23 for a phase locked oscillator locked to a crystal oscillator.

The second and third local oscillators are synthesised in order to provide the frequency selection: the first local oscillator provides coarse frequency selection, whereas the second stage provides the individual channel selection.

The synthesiser blocks consist of single phase locked loops (PLLs). Each PLL employs a VCO, which may contribute significant phase noise sideband power as illustrated in fig9.20. This shows the results of the author's measurements on a DRO and a wide tuning range TVRO type VCO. Close to carrier phase noise sideband levels are largely determined by the PLL reference signal which is provided by a crystal oscillator.

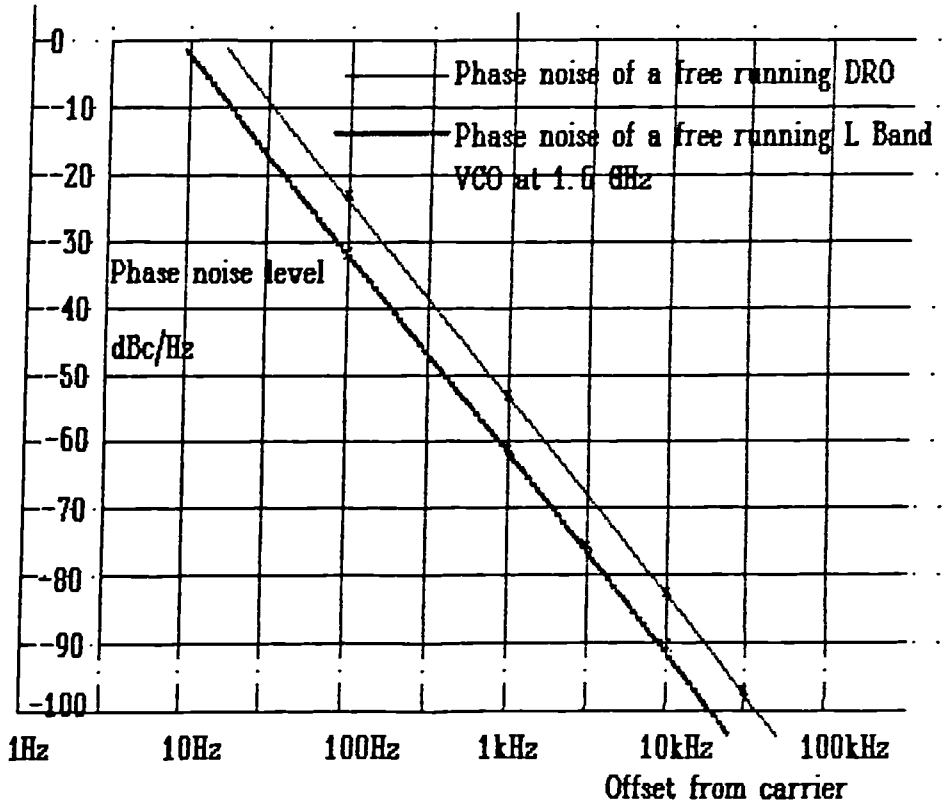


Fig 9.20 Phase noise of free running microwave oscillators

The detailed design of the PLL synthesiser blocks determine the phase noise characteristics, and ultimately the BER degradations; different PLL techniques are considered in these calculations, viz:-

1) Single chip CMOS divider phase detector with a variable modulus prescaler added to provide division from UHF;

2) Use of a specially designed low noise synthesiser.

The parameters of the above synthesiser configurations are summarised below:-

Table 9.1

Parameter	CMOS		LOW NOISE		
	fine	coarse	fine	coarse	
Phase detector noise floor	-50	-67	-90	-103	dBc/Hz
Phase detector 1Hz Intercept	-35	-50	-70	-73	dBc/Hz
VCO 1Hz Intercept point	+15	50	+15	50	dBc/Hz
Synthesiser Loop Natural Freq.	100	7k	2.5k	80k	Hz
Synthesiser loop Damping Factor	0.7	0.7	0.7	0.7	
Post loop filter break frequency	500	15k	20k	250k	Hz

9.7.4.3 Receiver local oscillators - synthesised 1st LO

In some applications, such as in portable satellite communication equipment, it may be desirable to have the first stage synthesised to simplify the downconverter. In this case, the YIG based synthesiser together with a DDS will be considered as described in chapter 4. When analysing this synthesiser, the phase noise curve of fig4.34 (chapter 4) is entered into the phase noise integration program. A point worth considering here is that the DDS scheme discussed in chapter 8 has phase noise that is not purely Gaussian; the phase noise is in fact band limited uniformly distributed noise. When bandlimiting such noise, the group delay of the filter results in a series of uniformly distributed events combining together over the duration of this group delay. Such summing together can be shown by the use of the central limit theorem to give an approximately Gaussian response [Papoulis, 1965]. Since the noise can never be greater than the total uniformly distributed noise power, the tail of the distribution is at a finite level rather than at infinity with a purely Gaussian distribution. A reduced level of this tail means the effective contribution to the overall BER would be reduced. However, making an exception like this to the one oscillator would considerably complicate system analysis. A good conservative estimate is therefore to assume the noise from the low spurious DDS is purely Gaussian distributed as is all the other random phase noise in the system.

The other local oscillator in the system is not considered as it would be a fixed oscillator at a much reduced frequency.

9.7.5 Link Specifications

9.7.5.1 Detailed specification of each section of the link

After broadly considering the configuration of the links to be analysed by the phase noise link budget program, detailed specifications of each link component will follow.

9.7.5.2 Satellite transponder

The satellite transponder phase noise is derived from the Eutelsat II phase noise specification [Eutelsat, 1989]. As the exact composition of the local oscillators is unknown, the phase jitter contribution must be determined by integration of the oscillator sideband specification. This phase noise performance is represented in fig9.21.

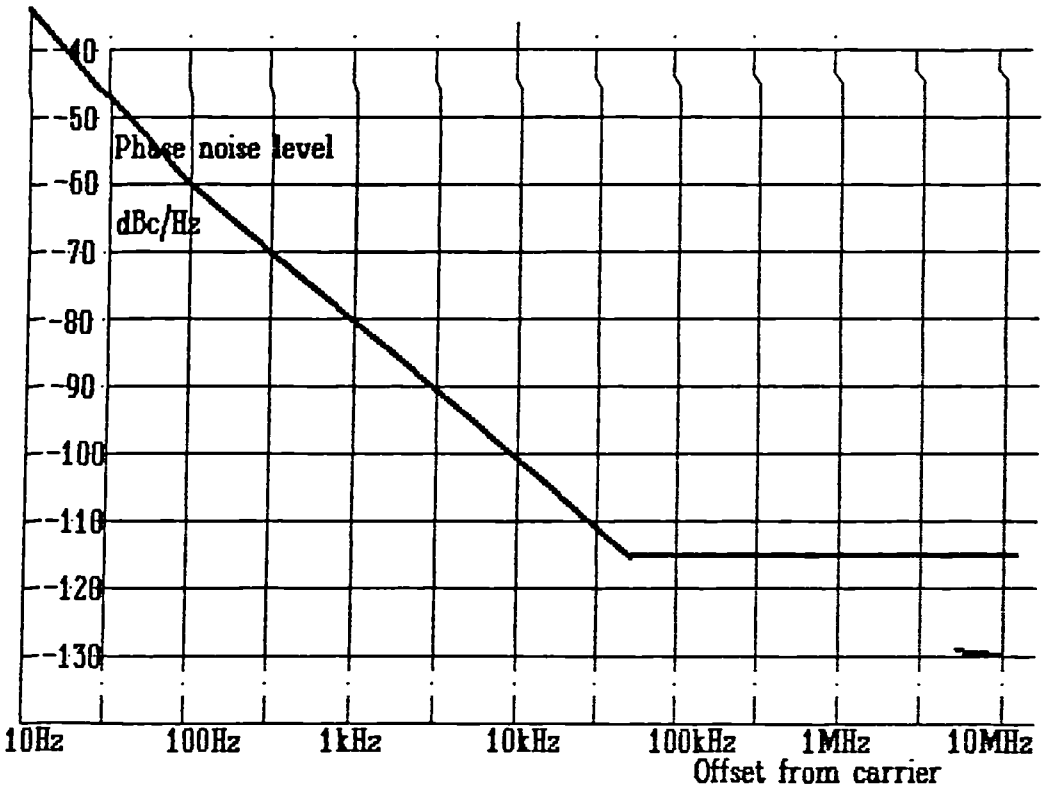


Fig 9.21 Phase noise of Eutelsat satellite transponder

9.7.5.3 Hub Station to VSAT

In this analysis, the Eutelsat SMS specification [Eutelsat 1987] for the data service ground station local oscillators may be used for the hub station transmitter. Again, as the exact composition of the local oscillators are unknown, the phase jitter contributions are determined by integration of the oscillator sideband specifications. The phase noise performance is represented in fig9.22.

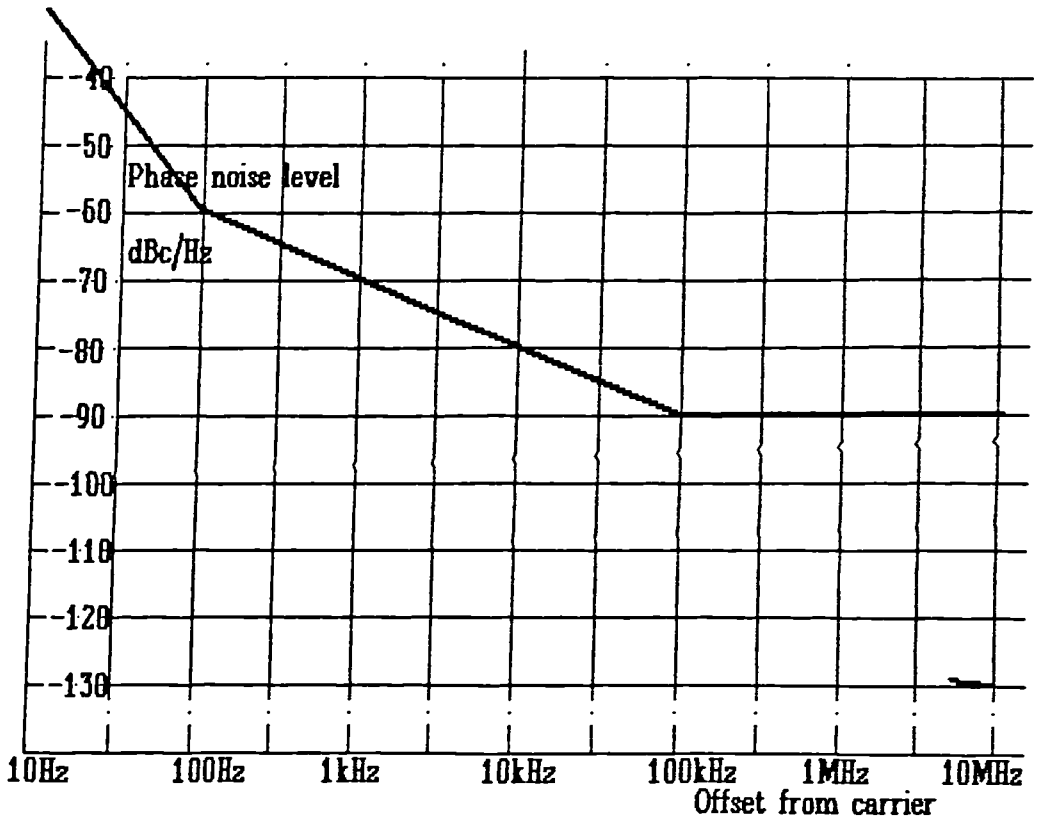


Fig 9.22 Phase noise specification for the Eutelsat ground station transmitter

For the hub station receiver, the local oscillator configuration is defined, therefore synthesiser transfer functions are used rather than a phase noise specification.

The following local oscillator options are analysed:

1st Local oscillator (Converting Carrier to 1.5 GHz, or v.v)

1) Single frequency free running DRO, phase noise as fig9.20;

2) Phase locked Voltage Controlled Oscillator, phase noise as in fig 9.23;

3) Phase locked DRO, phase noise as in fig9.23;

4) Direct modulation synthesiser, very low phase noise incorporating DDS and the very low phase noise BVA [Besson & Peier, 1980] crystal resonator reference source, phase noise as in fig9.24.

2nd Local oscillator (Converting 1.5 GHz. to 700 MHz or v.v)

1) Single IC synthesiser;

2) Low phase noise synthesiser;

3rd Local oscillator (Converting 700 MHz to 70 MHz or v.v)

1) Single IC synthesiser;

2) Low phase noise synthesiser;

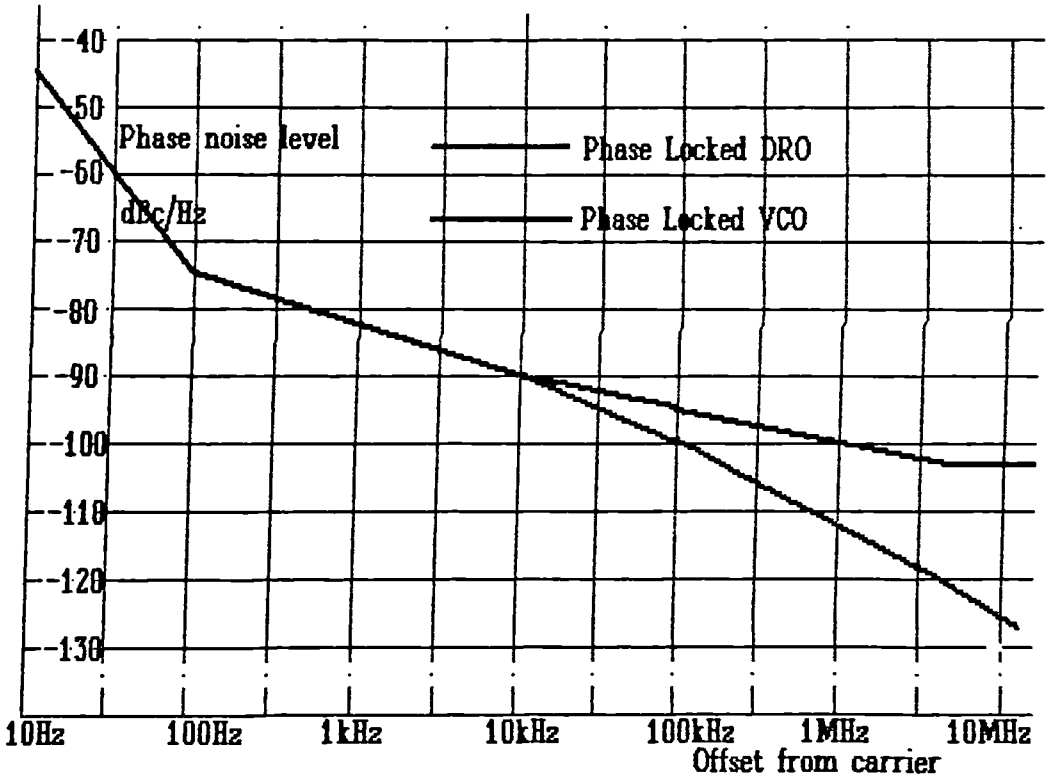


Fig 9.23 First local oscillator phase noise performance using PLOs

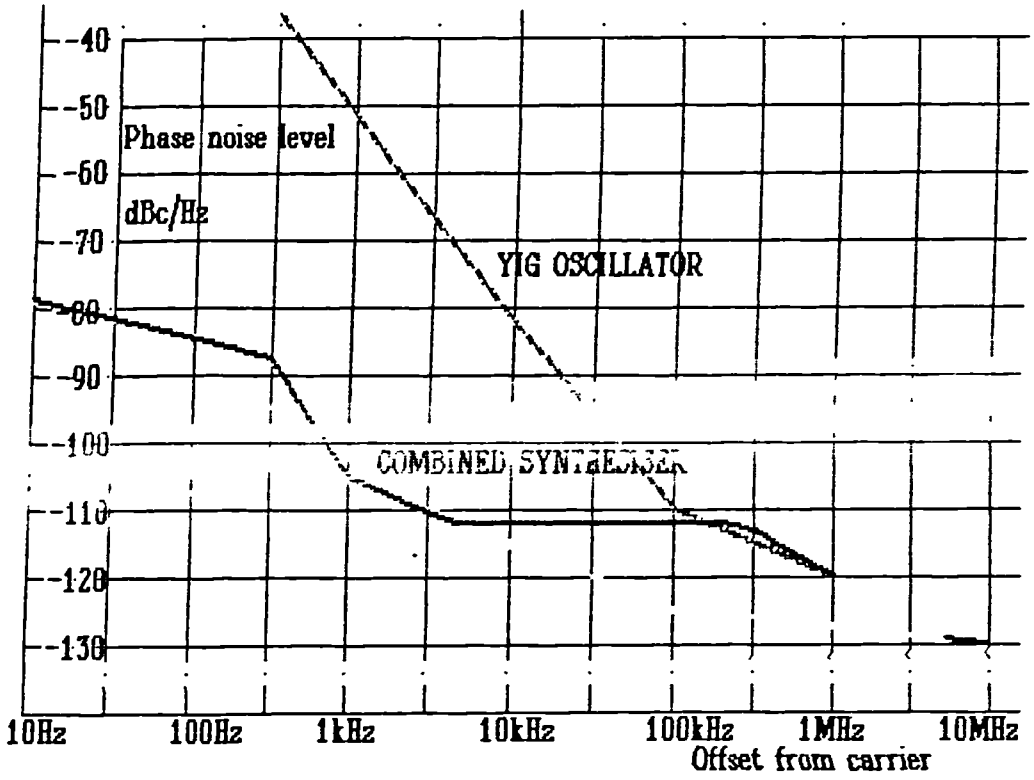


Fig 9.24 Very low phase noise synthesised first LO

9.7.5.4 VSAT to hub station

The phase noise level is assumed the same as the Hub station to VSAT case.

9.7.5.5 2-way VSAT link

In this case the transmit and receive local oscillators are assumed identical.

9.7.5.6 2-way VSATs with Direct Modulation

A direct modulation transmitter consists of a direct digital synthesiser modulated with data. The configuration outlined in fig4.31 is used in this study. A direct digital frequency synthesiser clocked at 300MHz is used as the modulator. This drives a wideband PLL transfer loop of loop bandwidth 10MHz. The reference loop is a YIG synthesiser. Here a single local oscillator is assumed, using a special low phase noise crystal resonator. For the receive section, only a single synthesised local oscillator is used, consisting of a YIG M/N synthesiser as described in chapter 4.

9.7.5.7 Choice of crystal resonator

The following crystal oscillator reference sources (which drive all the synthesisers) are assumed:

1) An inexpensive VHF crystal resonator of standard phase noise performance;

2) A specially designed low phase noise crystal reference source at 10MHz output frequency, eg the BVA resonator [Oscilloquartz, 1990].

9.7.5.8 Modulation

The following modulation schemes are considered in this analysis:

a) Uncoded BPSK;

b) BPSK with 7 segment half rate convolutional coding and Viterbi 16 level quantized soft decision decoding;

c) Uncoded Offset QPSK;

d) Offset QPSK with Forward Error Correction as b).

9.8 Results of several configurations selected from above

9.8.1 Overview

The results of the computer analyses are plotted in figs9.25 to 9.39, (Plots1 to 14). These show the degradation of performance (ie sensitivity) in dB due to phase noise, as a function of the data rate, f_d, and the carrier recovery loop bandwidth (eg $f_d/10$, etc). A BER of 10^{-7} is taken throughout. There are 14 plots altogether, which are according to the table following. The prefix 'C' before the modulation indicates the use of FEC.

All plots display an increase in degradation at low data rates above that possible with perfect carrier recovery, this is due to the steeply rising close to carrier phase noise. Such phase noise can be tracked out with the carrier recovery loop for higher data rates.

Table 9.2

	Hub-VSAT & vice-versa	2-way	2-way Direct mod
Free running DRO Low cost Synthesiser	*BPSK* *Plot 1* *CBPSK* *Plot 2*		
1st LO Phase locked Low cost Synthesiser	*BPSK* *Plot 3* *CBPSK* *Plot 4* *OQPSK* *Plot 5* *COQPSK* *Plot 6*	*CBPSK* *Plot 10*	
1st LO Phase locked Low noise Synthesiser	*CBPSK* *Plot 7* *COQPSK* *Plot 8*	*CBPSK* *Plot 11*	
Phase locked DRO Low noise Synthesiser	*COQPSK* *Plot 9*		
Phase locked DRO Very Low noise Synthesiser BVA reference			*CBPSK* *Plot 12* *OQPSK* *Plot 13* *COQPSK* *Plot 14*

9.8.2 Use of TVRO systems

Initially, degradations were calculated for phase noise performances as would be encountered if a TVRO type system be used; with a free running DRO used as the first local oscillator. For uncoded BPSK systems, as can be observed from plot 1 (fig 9.25), degradation begins to occur for data rates of less than 100 kbit/s. For the coded system, plot 2 (fig 9.26) shows degradation occurring for data rates below 1 Mbits/s. Coding gain still results over that of an uncoded system, but the coding gain is reduced. The reduction is due to the fact that a higher carrier loop bandwidth can be used for an uncoded system due to the lower levels of thermal noise jitter contributions. By contrast, below 20 kbits/s, the coding gain becomes higher than for a system with no phase noise.

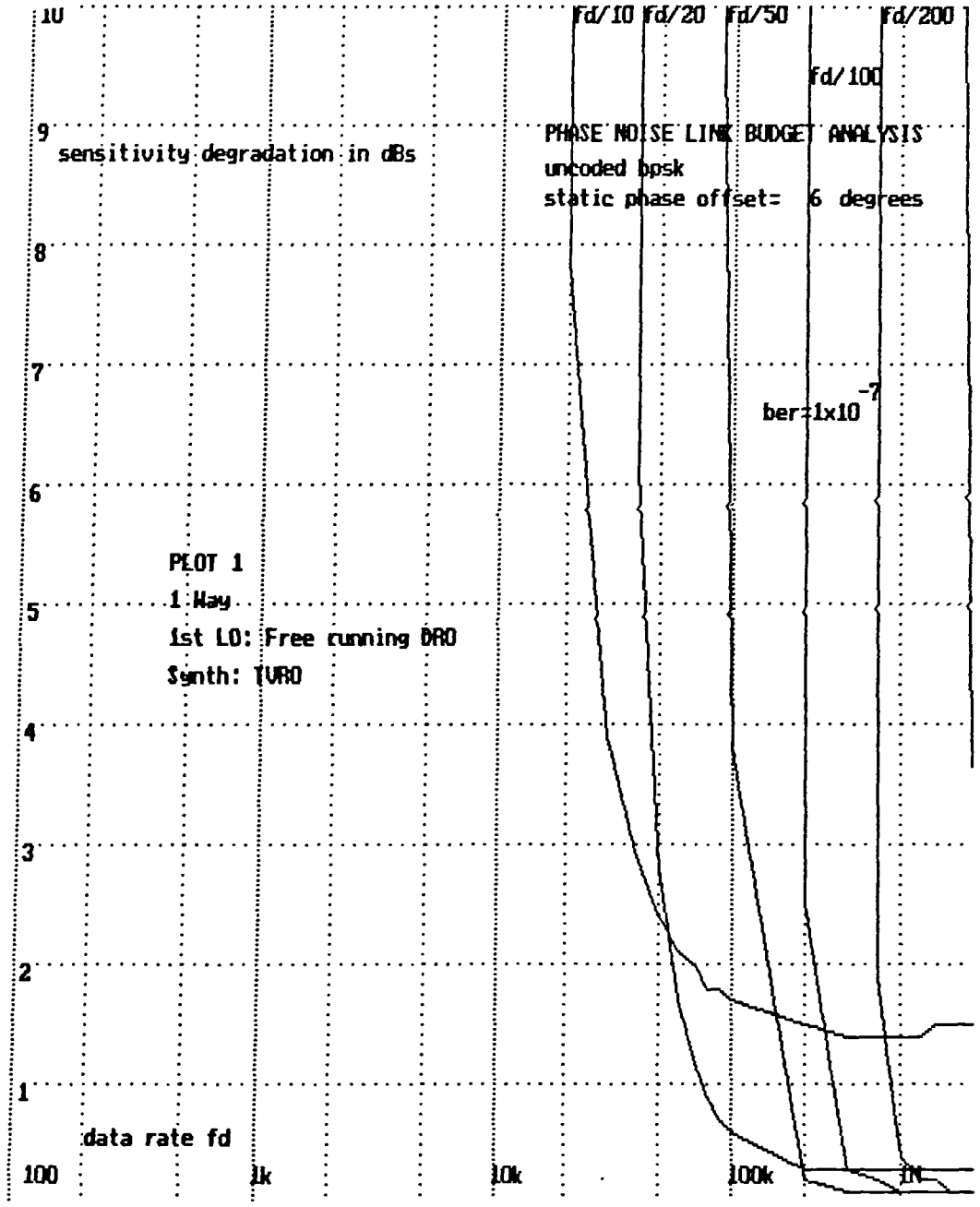


Fig 9.25 Plot 1 Phase noise degradation: Uncoded BPSK, free running DRO

When coding is used, the link data rate is increased, resulting in an increase of thermal noise; this increase of thermal noise is allowed for in the calculations of Viterbi coding gains. If the dominant phase noise mechanism is $1/f^3$ noise, there will be little increase in effective phase noise levels for the increased link rate. Therefore an increase in the effective coding gain should be observed. However, for uncoded systems it is possible to reduce the effect of phase jitter by the use of a wider CRL bandwidth, due to the lower thermal noise level.

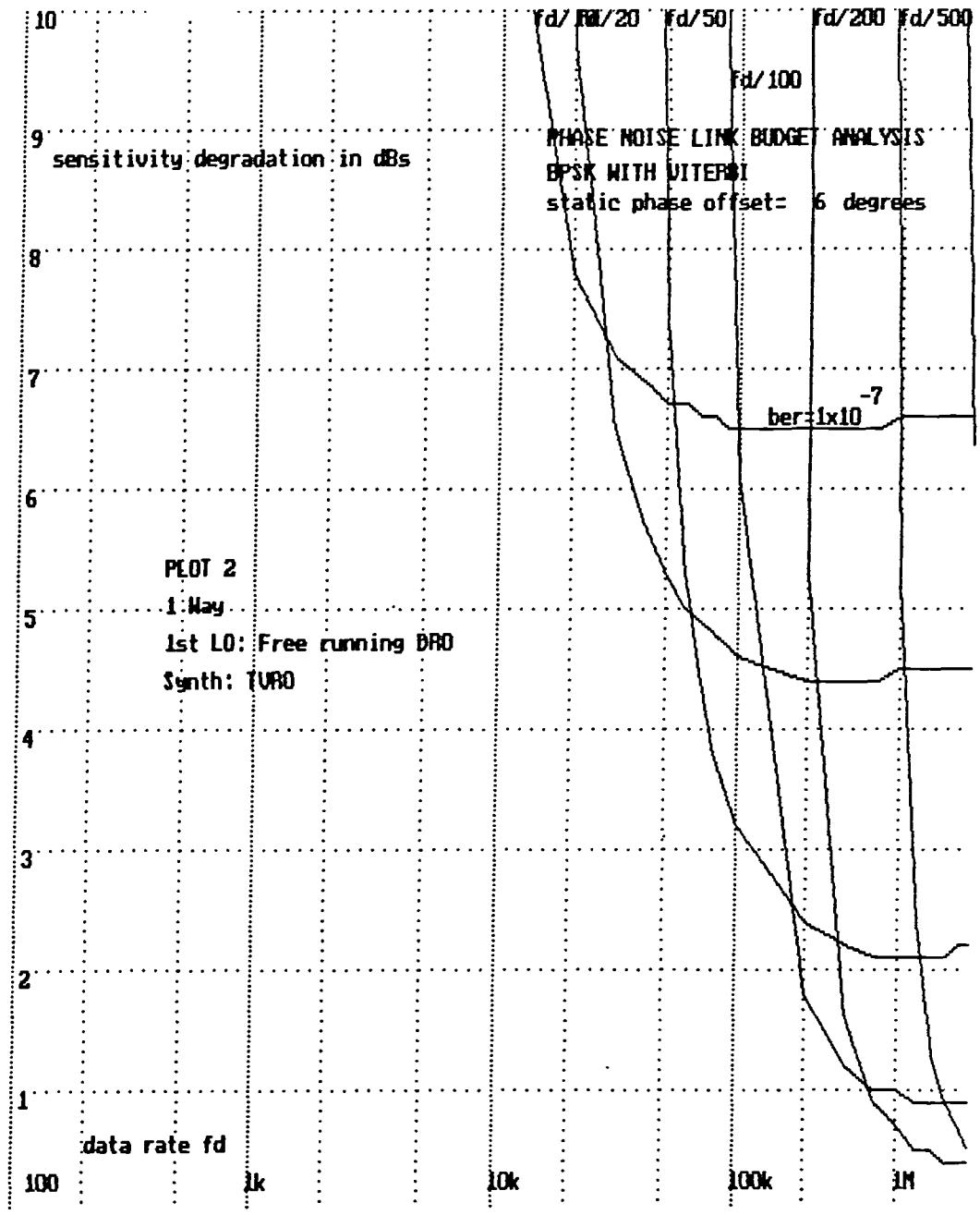


Fig 9.26 Plot 2 Phase noise degradation: Viterbi BPSK, free running DRO

This effect of $1/f^3$ noise should become visible for data rates below 20kbits/s because it is not practicable to increase the carrier recovery loop bandwidth above a tenth of the data rate for the uncoded case. Any increase of loop bandwidth may result in data feedthrough of the carrier recovery loop.

9.8.3 One way systems with phase locked local oscillators

9.8.3.1 BPSK uncoded

As expected from the theory, uncoded BPSK is the most robust modulation scheme in the presence of phase noise. As can be observed from plot 3 (fig 9.27), if a phase locked 1st local oscillator is used the performance is insensitive to synthesiser type for data rates of 1 kbits/s or greater.

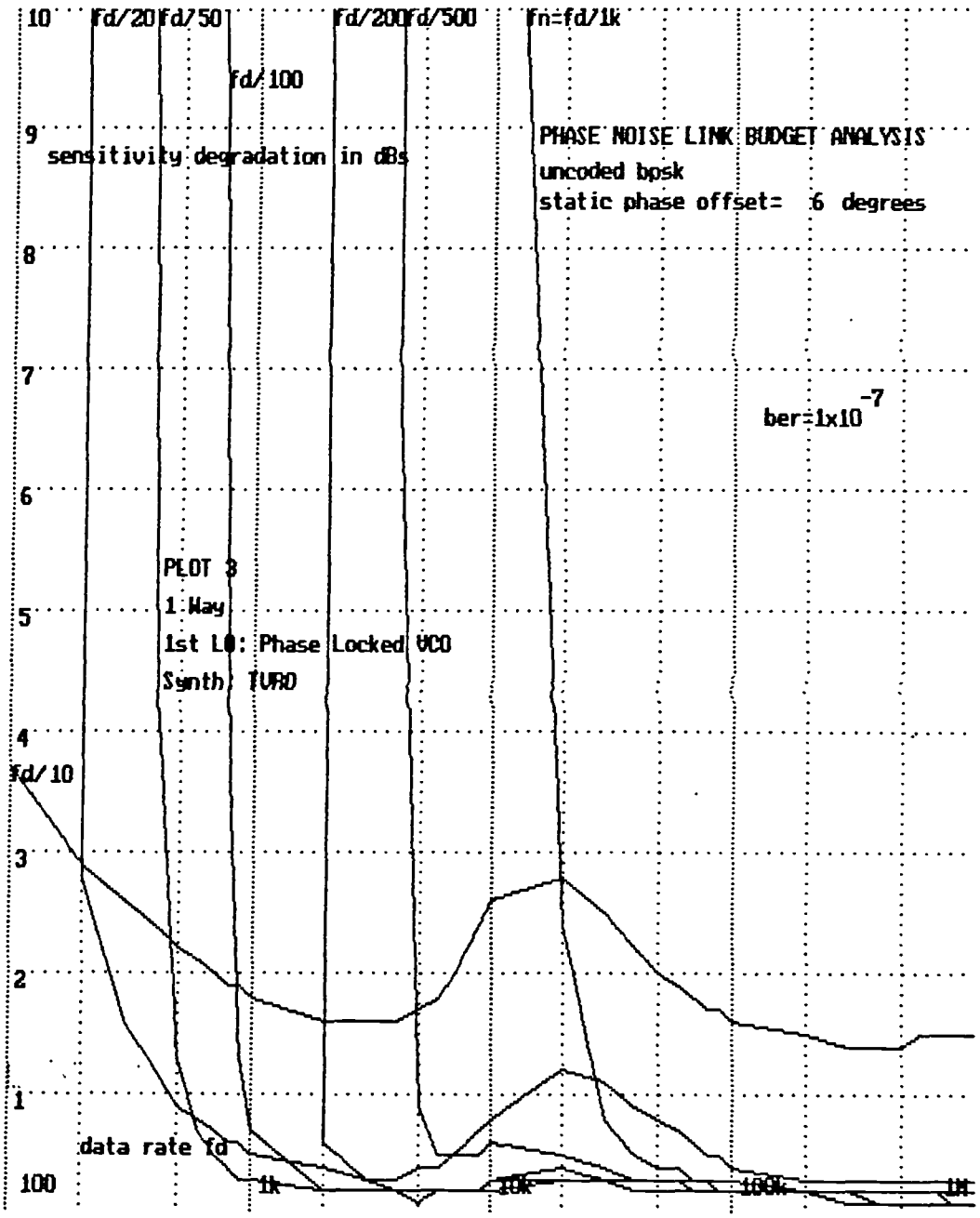


Fig 9.27 Plot 3 Phase noise degradation: Uncoded BPSK, Phase Locked VCO First LO, TVRO synthesiser

At low data rates, degradation occurs due to close to carrier phase noise of the crystal oscillators. With low phase noise oscillators in the transmitter and receiver, degradation still occurs for data rates of less than 200bits/s. The dominant contribution to the phase noise is the transponder crystal oscillator, determined by the satellite specification. This is irreducible and therefore the minimum limit for uncoded BPSK can be taken to be 200 bits/s with these parameters.

9.8.3.2 Coded BPSK

The use of forward error correction coding has a marked effect upon the phase noise sensitivity of systems. Coding gain is the gain in sensitivity over that obtained if coding is not used for identical conditions.

From plot7 (fig9.31, later) it can be observed that the lowest data rate that can be used before significant degradation occurs is 2kbits/s, but coding gain will result for data rates of greater than 100bits/s. The use of a low cost synthesiser (plot4, fig9.28) results in some degradation for most error rates.

For a Viterbi system, the increased bit rate over the channel should result in negligible increase in phase noise power for $1/f^3$ noise; this can be contrasted with a 3dB increase for thermal noise. However, the level of thermal noise is much higher with Viterbi due to squaring loss in the carrier recovery loop. As a result, there is less margin available for phase noise; consequently, the Viterbi system is more sensitive to both synthesiser noise and reference noise. An experimental modem was tested and is described later in §9.10. This operated at 20.48kbits/s which is marked as a vertical bar on fig9.28 for ease of reference.

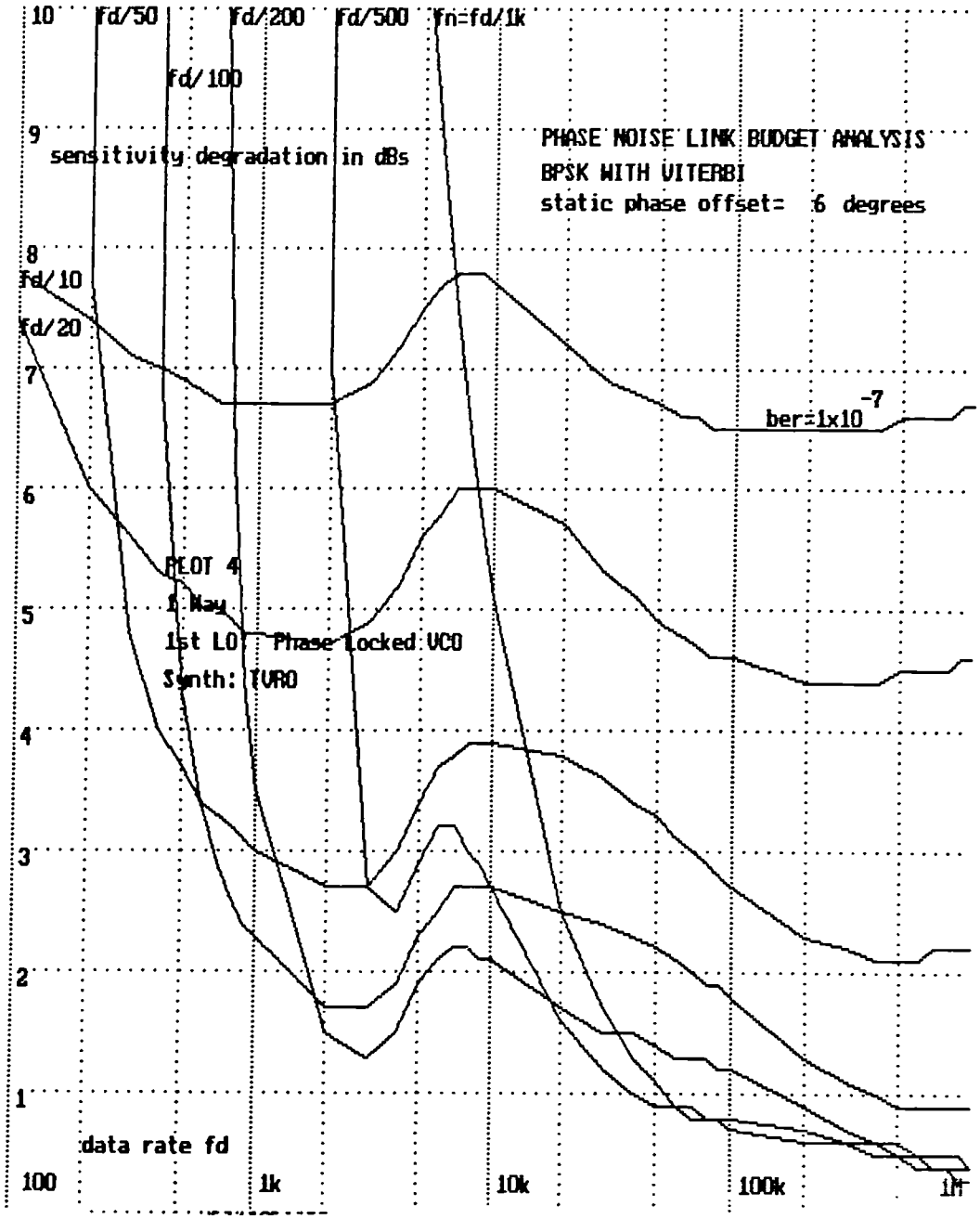


Fig 9.28 Plot 4 Phase noise degradation: Viterbi BPSK, Phase Locked VCO First LO, TVRO synthesiser

9.8.3.3 Uncoded offset QPSK

For QPSK systems, the degradations were excessive for all data rates studied. The static phase offset had to be reduced to 2 degrees in order to obtain useful results, which implies the use of digital techniques to reduce this offset for QPSK.

The degradation results for a system using uncoded QPSK and single chip synthesisers is shown in plot 5 (fig 9.29). With QPSK systems, phase noise has a much more drastic effect.

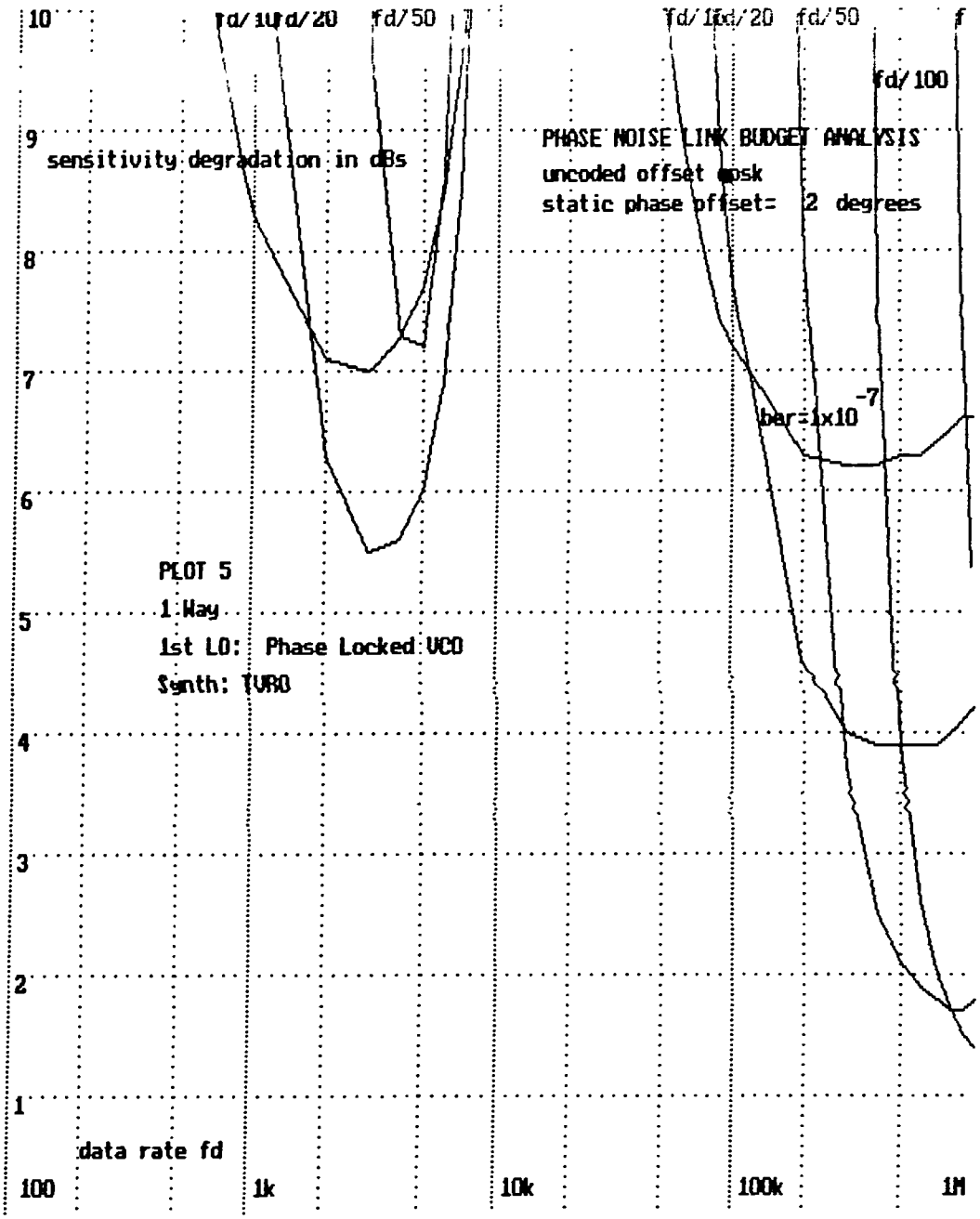


Fig 9.29 Plot 5 Phase noise degradation: Uncoded QPSK, Phase Locked VCO First LO, TVRO synthesiser

When a low cost synthesiser is used, degradation rapidly increases for data rates below 1 Mbits/s. At data rates of 10kbits/s, the degradation is greater than 10dB. If a low noise synthesiser is used, then little degradation occurs until the data rate becomes less than 10kbits/s. At high data rates, in a similar manner to plot 8 (fig 9.32) for coded QPSK, the degradation begins to increase again, and is due to the high far-from-carrier noise of the VCO used as local oscillator.

9.8.3.4 Offset QPSK with Viterbi

This is the most demanding of all the situations surveyed as regards phase noise. If cheap synthesisers are used, as shown in plot 6 (fig 9.30), the degradation is totally unacceptable.

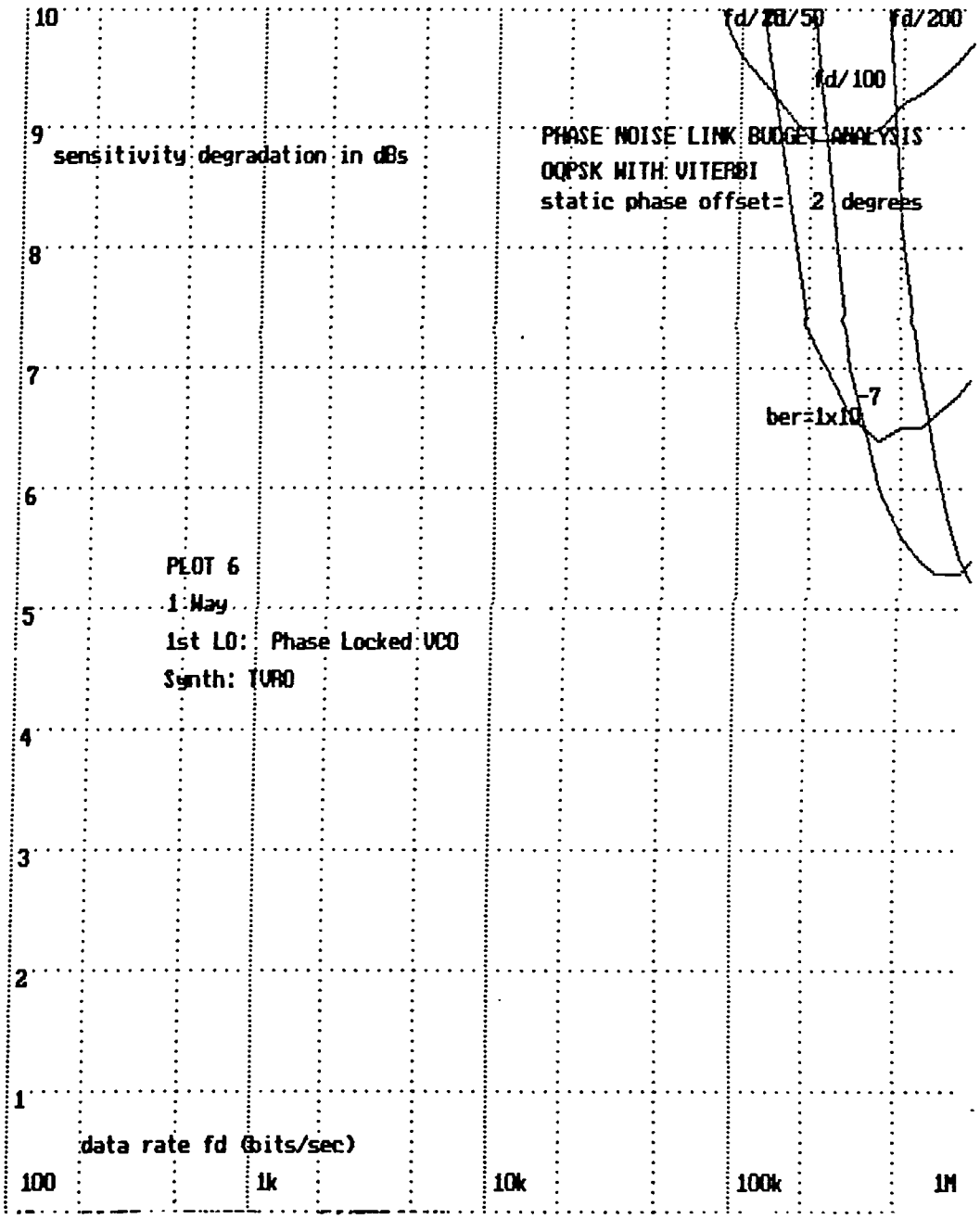


Fig 9.30 Plot 6 Phase noise degradation: Viterbi QPSK, Phase Locked VCO First LO, TVRO synthesiser

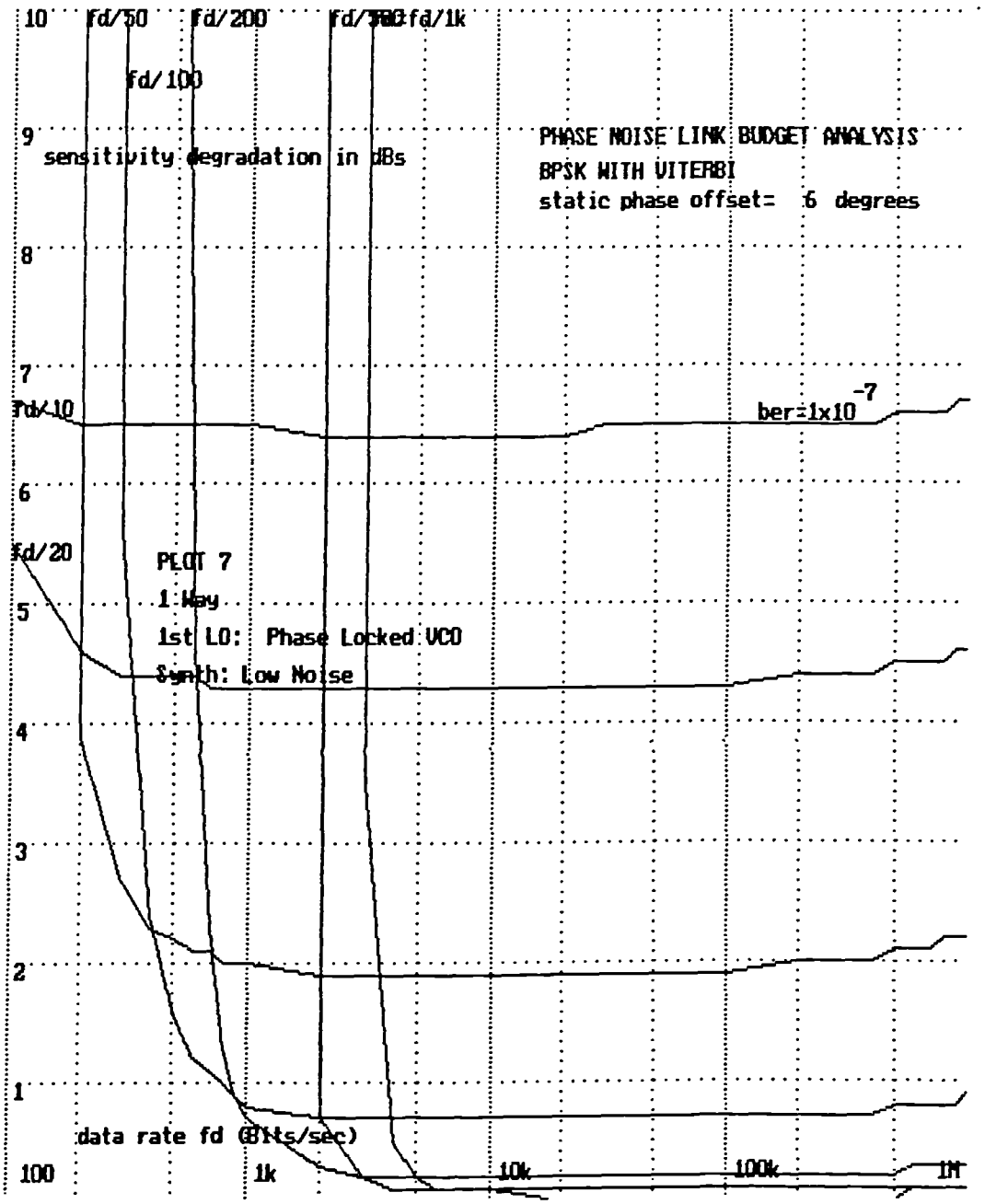


Fig 9.31 Plot 7 Phase noise degradation: Viterbi BPSK, Phase Locked VCO First LO, low noise synthesiser

Therefore low noise synthesisers are mandatory with this modulation format. With the low noise synthesiser, as can be observed from plot 8 (fig 9.22), the degradation never falls below 1 dB and increases rapidly below 10 kbits/s. Increased sensitivity to VCO phase noise is also observed by the increase of phase noise at data rates of above 500 kbits/s. Plot 9 (fig 9.33) displays the effect of replacing the phase locked VCO with a phase locked DRO; the improved far-from-carrier noise results in reduced degradation at high data rates, hence the rise in degradation evident in plot 8 does not occur.

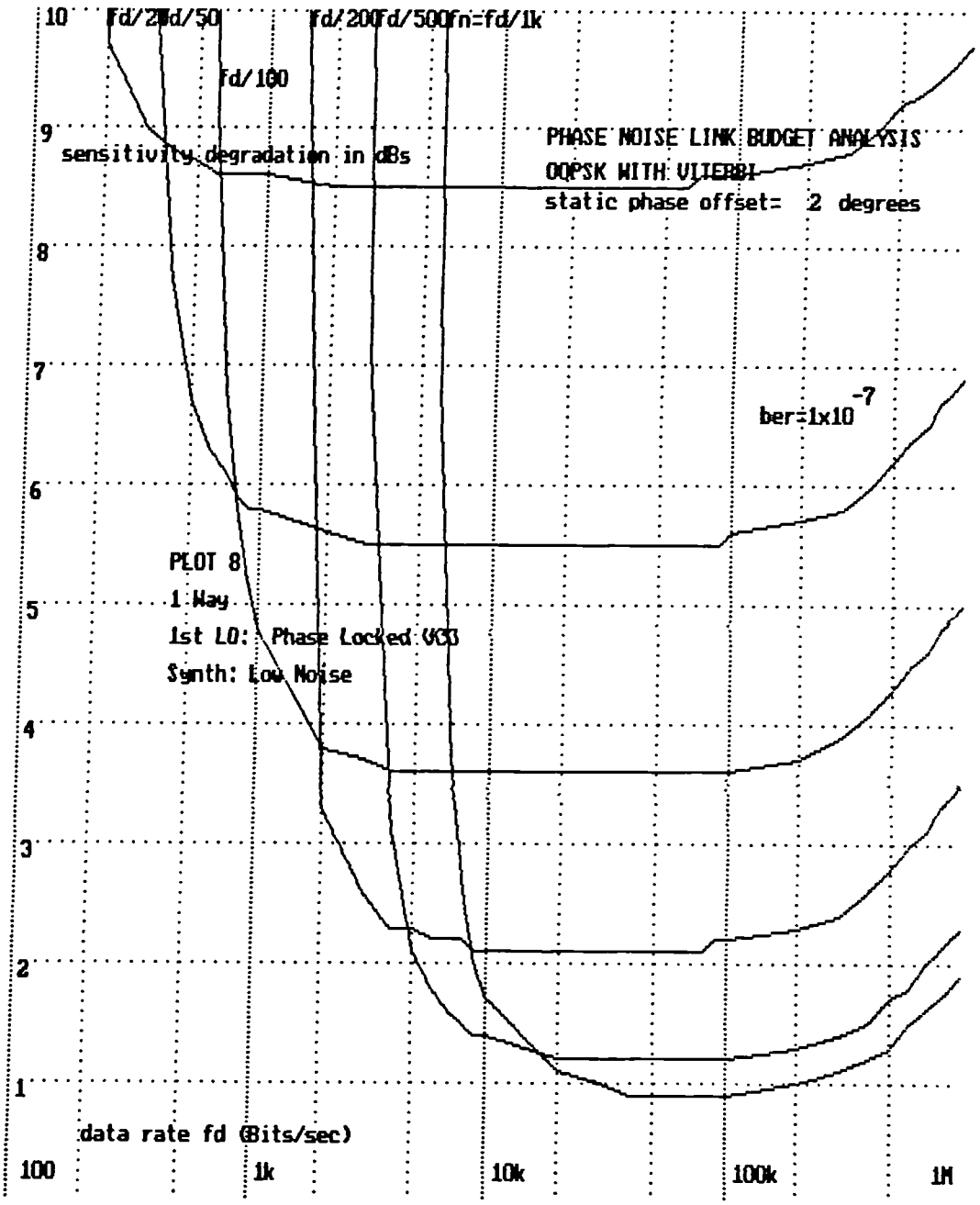


Fig 9.32 Plot 8 Phase noise degradation: Viterbi QPSK, Phase Locked VCO First LO, low noise synthesiser

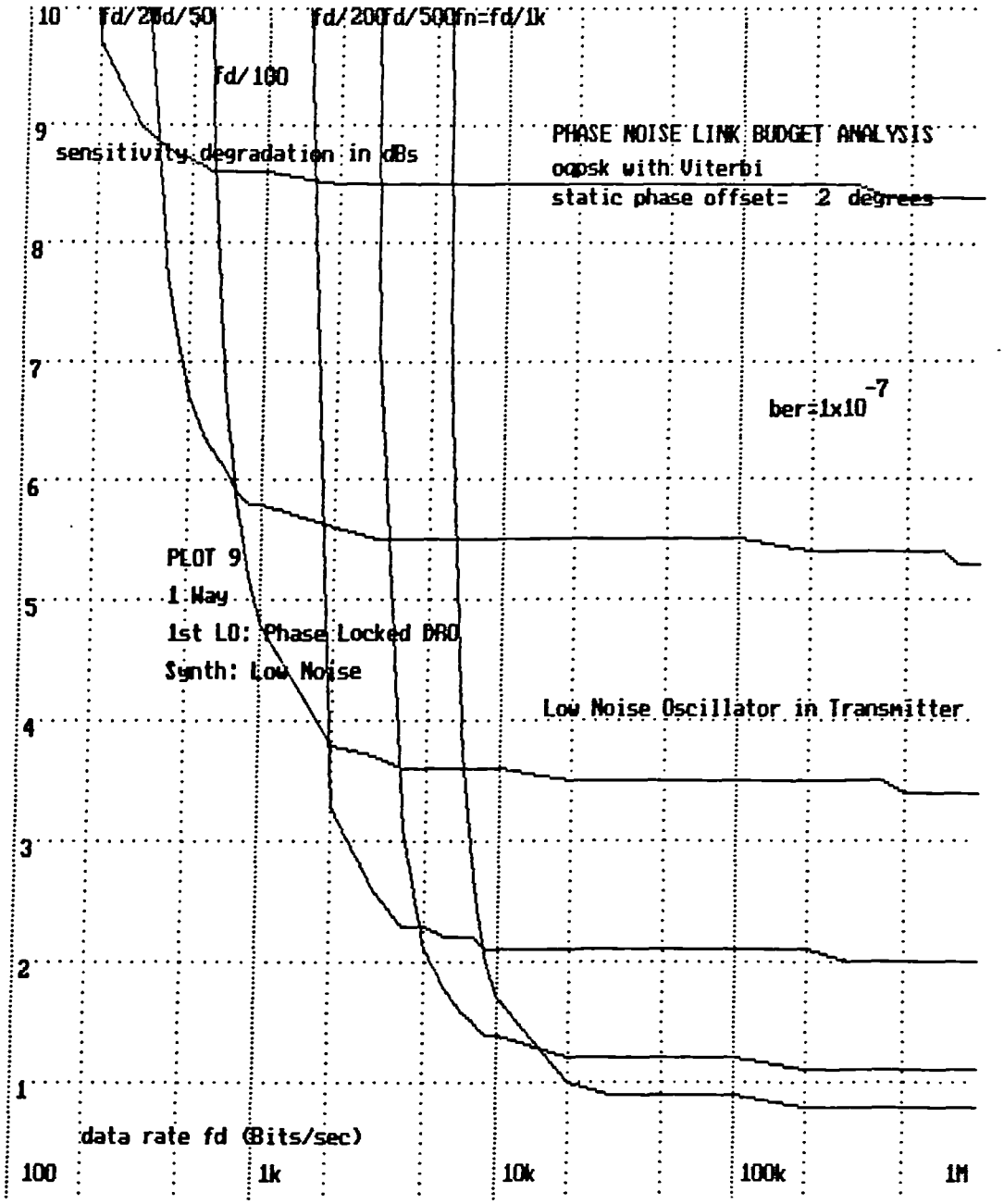


Fig 9.33 Plot 9 Phase noise degradation: Viterbi
QPSK, Phase Locked DRO First LO, low noise synthesiser

9.8.4 One way system with state of the art LOs

If state of the art synthesisers and reference oscillators are used, there was little change from the results displayed in plots 7 (fig 9.31) and 8 (fig 9.32) for the low noise synthesiser case. As the ground station was a major contributor to the overall phase jitter, any improvement in the receiver synthesiser would result in little change to the overall phase jitter.

9.8.5 2-way Systems

More care has to be taken in the design of 2-way systems as the local oscillators in the transmitter all add to the phase noise.

9.8.5.1 Single chip synthesisers

For the case of two way systems employing single chip synthesisers, the performance for coded BPSK is shown in plot 10 (fig 9.34). A phase locked first LO is used in this case. Degradation occurs even for uncoded BPSK, for data rates of between 10kbits/s and 100 kbits/s. If Viterbi is used, as with plot 10, degradation occurs for any data rate below 1 Mbits/s.

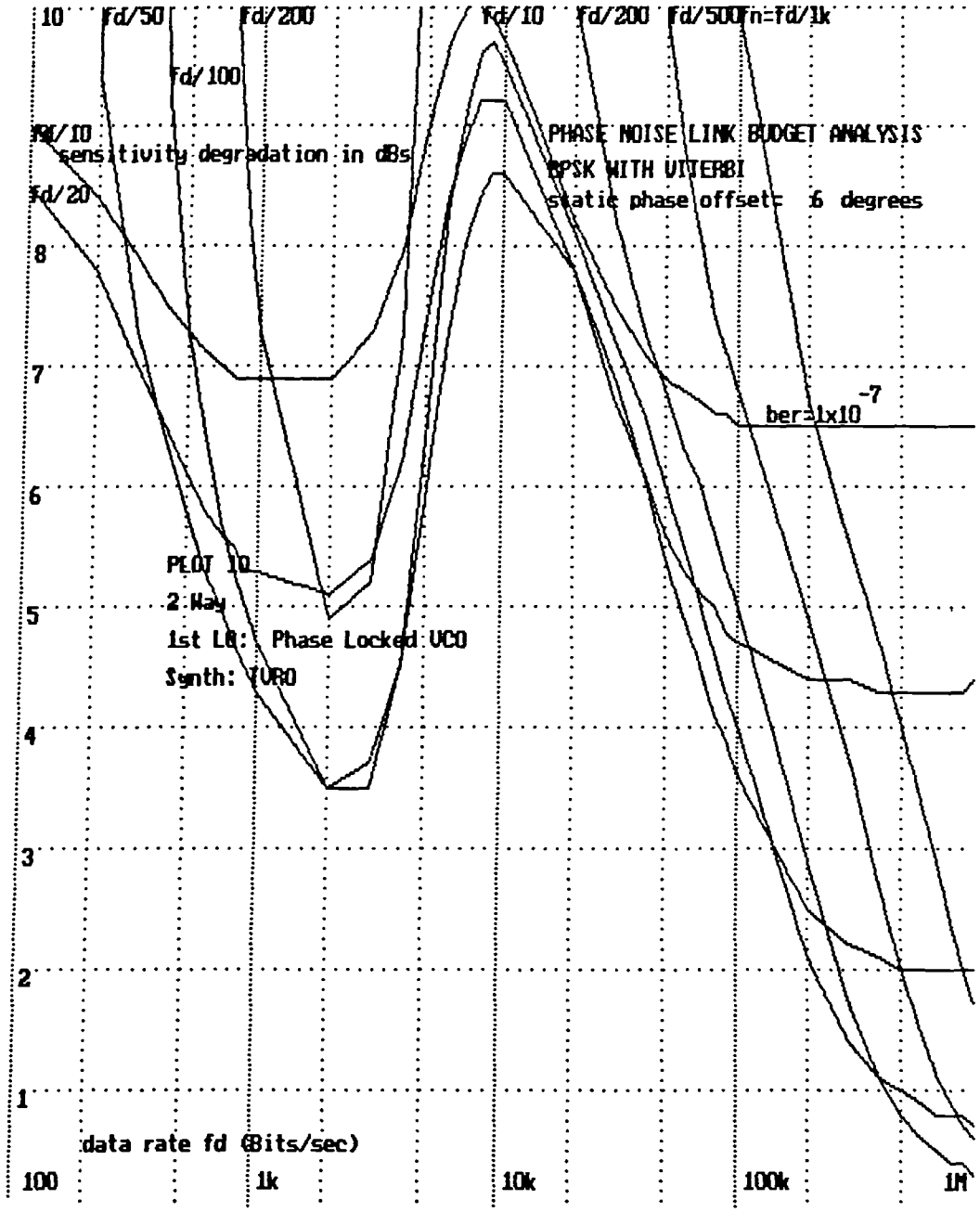


Fig 9.34 Plot 10 Phase noise degradation: Viterbi BPSK, 2 Way system Phase Locked VCO First LO, low cost synthesiser

9.8.5.2 Low noise synthesisers

If low noise synthesisers are used, then for a 2-way system, according to plot 11 (fig 9.35), the point at which degradation occurs for a Viterbi system is below 1 kbits/s. This is an improvement on the one way system and is due to the reduced phase noise of the transmitter over that of the ground station.

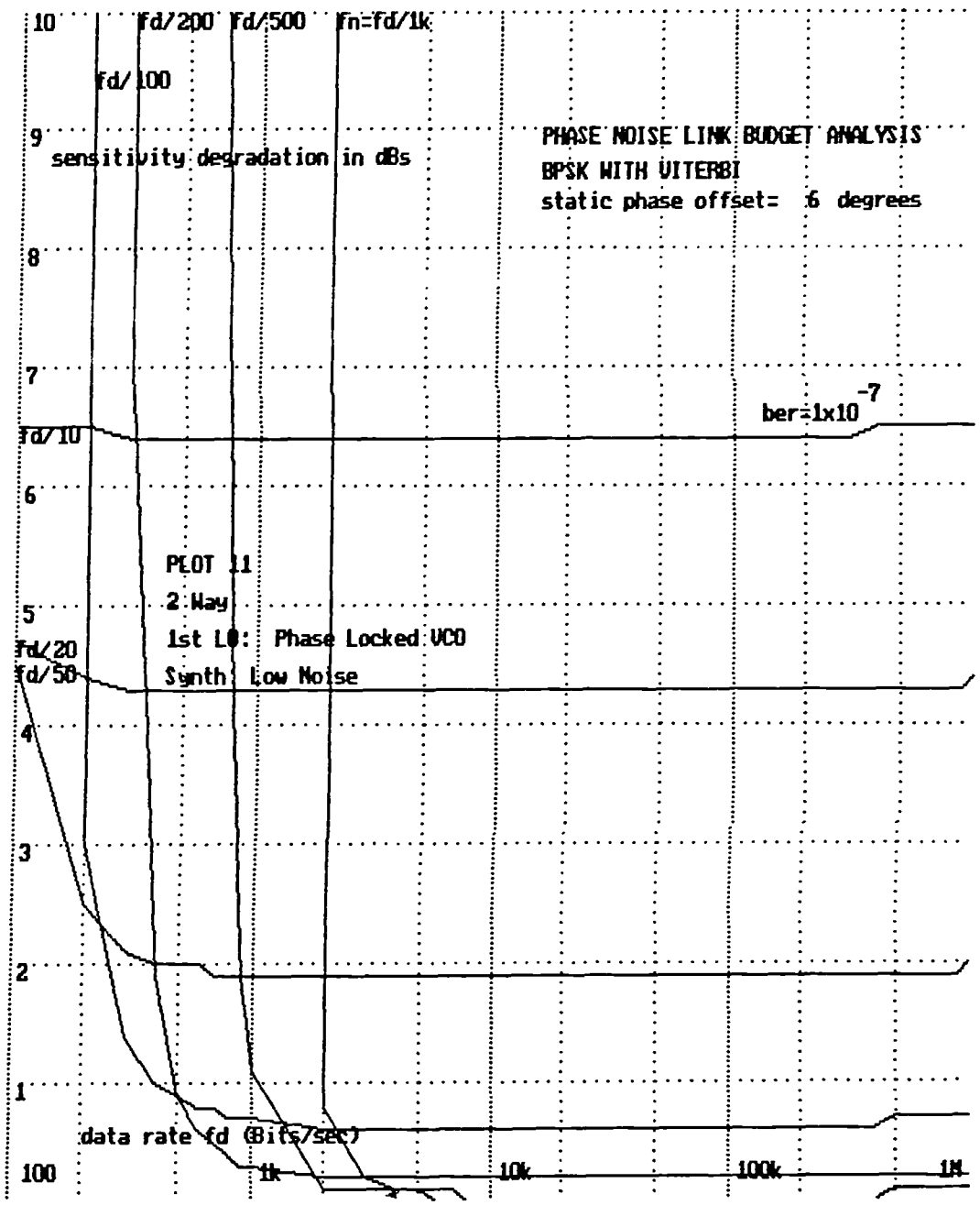


Fig 9.35 Plot 11 Phase noise degradation: 2 Way system, Viterbi BPSK, Phase Locked VCO First LO, low noise synthesiser

9.8.5.3 Direct modulation transmitter

Direct modulation transmitters allow the reduction of local oscillators to one. Modulation is applied to a direct digital synthesiser, and, in addition, a low phase noise crystal reference is used in both transmitter and receiver. Therefore significant reduction in total system phase noise is possible. For uncoded BPSK, degradation is less than 1 dB at data rates of 100 bits/s. With Viterbi, shown in plot 12 (fig 9.36), degradation rapidly increases for data rates of less then 500 bits/s. For uncoded offset QPSK the corresponding data rate is 2 kbits/s plot 13 (fig 9.37), and for offset QPSK with Viterbi, 10 kbits/s (plot 14, fig 9.38).

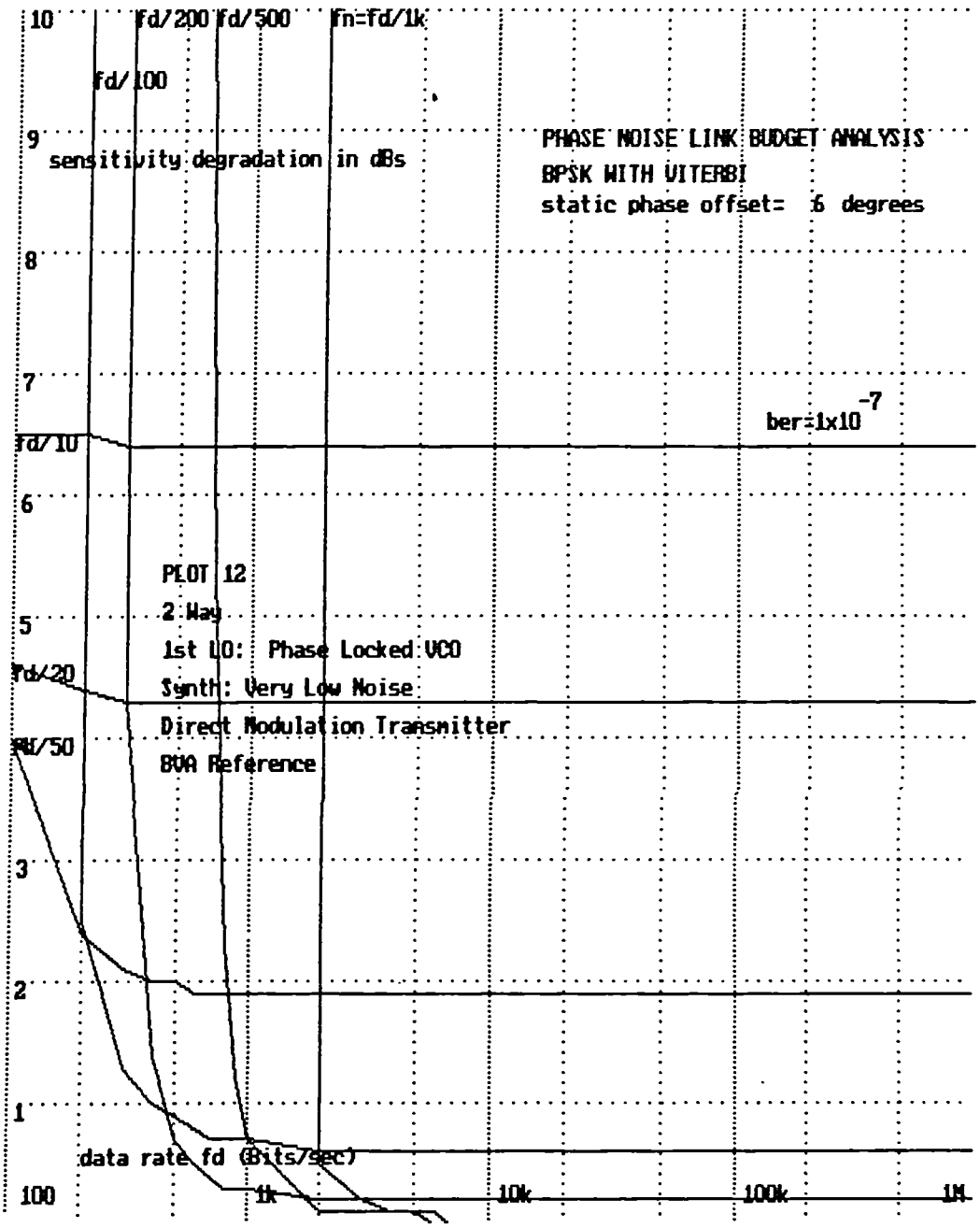


Fig 9.36 Plot 12 Phase noise degradation:
2 Way system, Viterbi BPSK, Direct modulation synthesiser

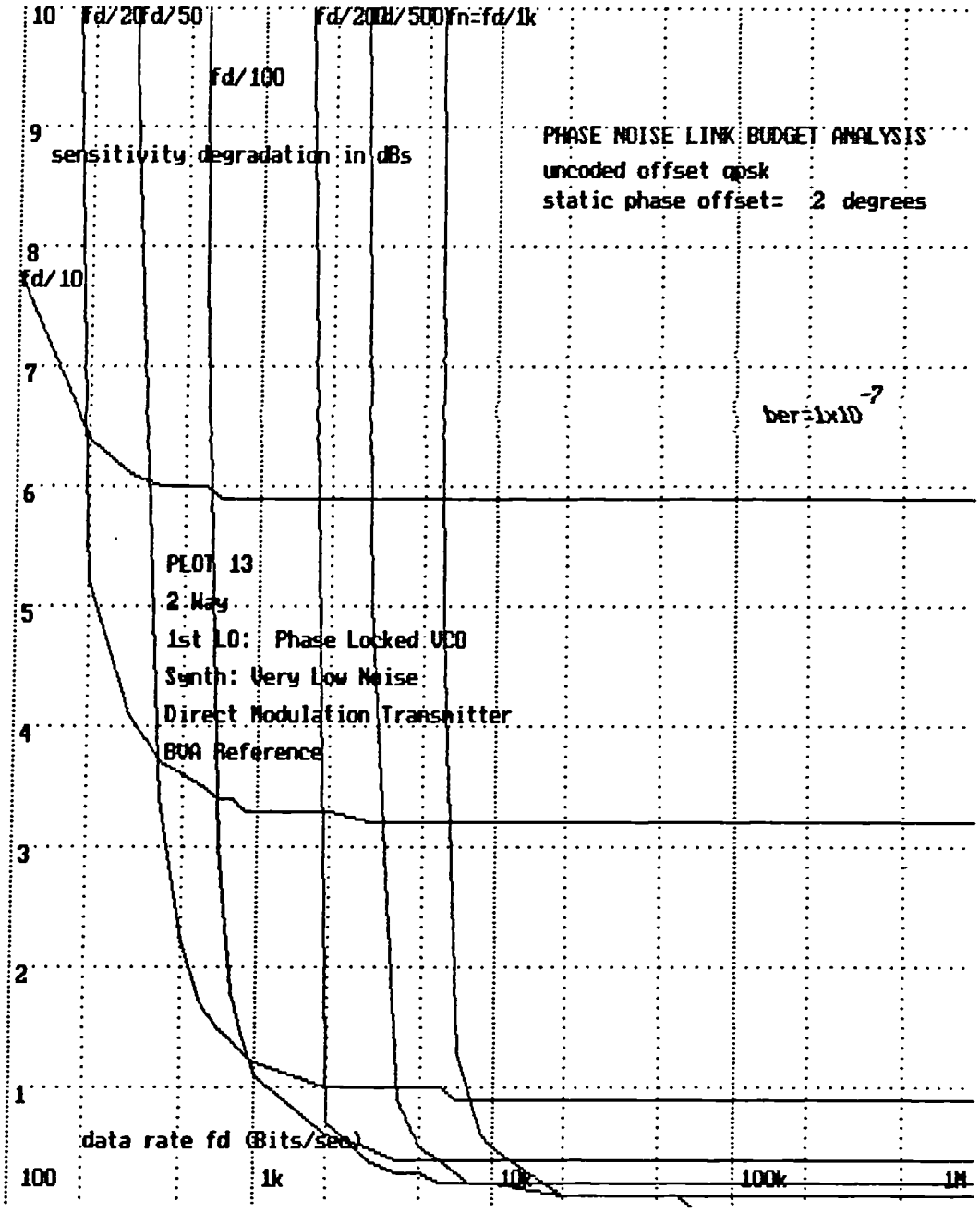


Fig 9.37 Plot 13 Phase noise degradation:
2 Way system, Uncoded QPSK, Direct modulation synthesiser

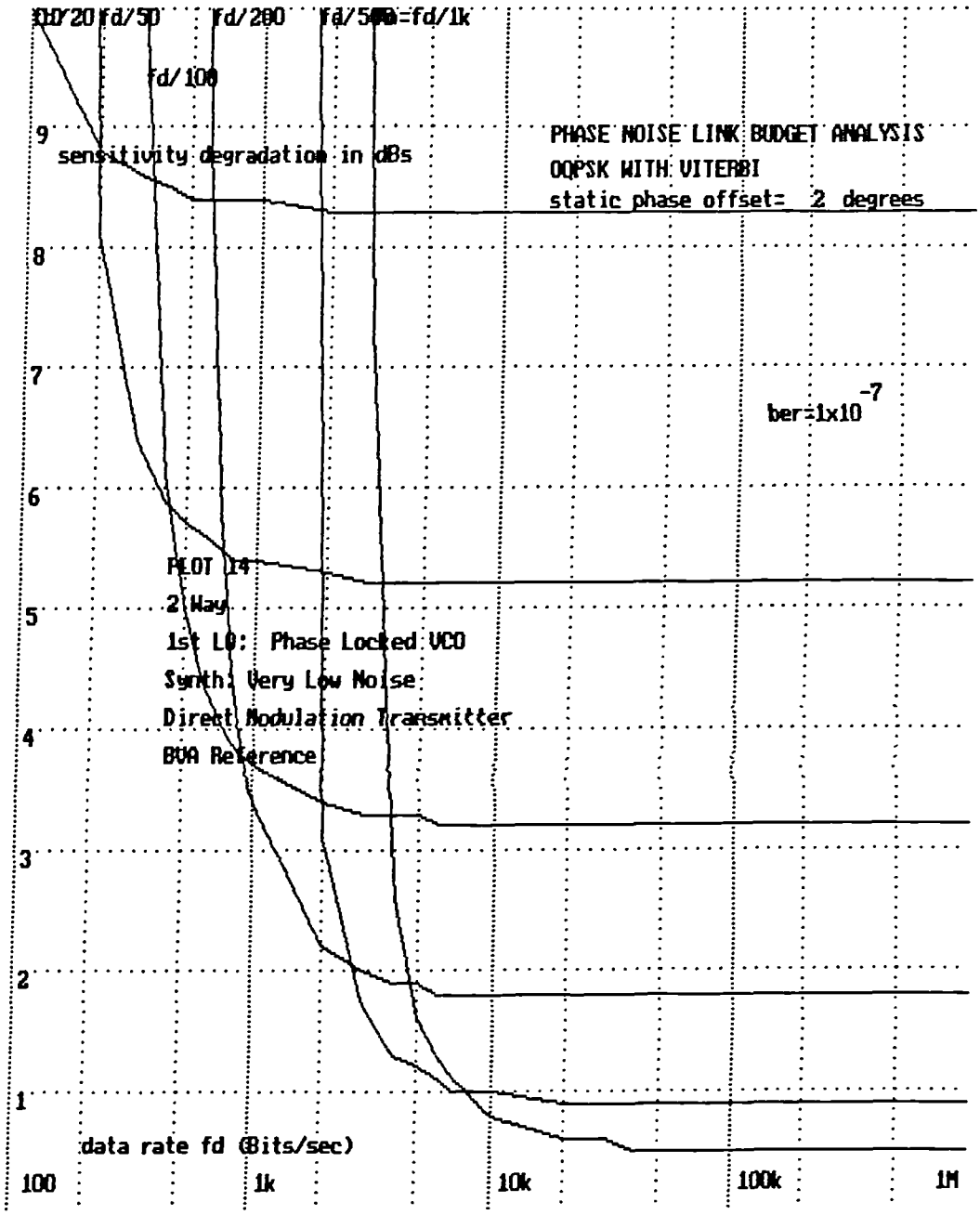


Fig 9.38 Plot 14 Phase noise degradation:
2 Way system, Viterbi QPSK, Direct modulation synthesiser

9.8.6 Effect of using phase locked DROs and low noise-floor synthesisers

The effect of using a phase locked DRO is a reduction in the far-from-carrier phase noise. It is not practicable to reduce the phase noise of the VCO in the synthesiser because of the wide tuning range requirement, therefore a reduction in synthesiser noise floor will be required. Plot 8 displays the effect on a Viterbi offset QPSK system of using VCOs for local oscillators. The degradation begins to increase for data rates above 200 kbits/s. Below this figure the effect of improving far from carrier phase noise will be negligible.

Plot 9 (fig 9.33) displays the effect of using a phase locked DRO and a low phase noise floor synthesiser; the degradation no longer rises for high data rates.

9.9 System performance summary

For digital satellite communications systems, a phase noise link budget calculation is required alongside the conventional thermal noise link budget. For coherent PSK there is a contradiction in requirements for the carrier loop bandwidth: a narrow loop bandwidth is required to remove thermal noise, and a wide loop bandwidth required to remove phase noise. The steeply rising BER curves of decoding schemes such as Viterbi mean that they are especially sensitive to additional phase errors as a result of phase noise, and any coding gain may be lost due to inadequate phase noise performance.

With forward error correction schemes, the signal to noise ratio at the point of carrier recovery may be extremely small, and therefore the performance of the carrier recovery multiplier may be critical. The intersection of the squaring loss section of the curve with the normal large *C/N* curve as discussed in §6.3.2 may give a useful figure of merit to the squarer performance.

Sources of phase noise include the crystal reference oscillator f^{-3} multiplied up by 20 log *N* and the synthesiser excess noise. The use of single chip CMOS synthesisers tends to give excessive BER degradation. Synthesiser excess phase noise also results in the demodulator being more sensitive to CRL static phase offsets. The $1/f$ component of the synthesiser excess noise is of great significance for BER degradation. Vibration can also be a problem as shown in §5.8 when close stepping synthesisers are used unless expensive measures are taken with the VCOs. By implementing the author's low spurious DDS technique discussed in chapter 8, it is possible to have wideband phase locked loops and low cost VCOs throughout the synthesiser design. This should result in drastically reduced contribution to the phase noise budget from vibration induced phase noise. A fine stepping synthesiser could remove the requirement for a wide tuning range VCXO, thereby removing the $1/f^3$ noise from this source.

Although the phase noise of the local oscillators in the ground terminals could be improved, there is an ultimate limit to the phase noise contributions to the jitter, that due to the satellite transponder oscillators. An example of the phase jitter contribution of the transponder phase noise is given in §9.10 while illustrating the phase noise link budget of a typical satellite data link. The satellite transponder oscillators are not alterable once the

satellite is in service. In the calculations of link performance undertaken with this work, the transponder specification limit was taken as the phase noise contribution to the system. Therefore, the results obtained above may be pessimistic, especially for low phase noise synthesiser systems, as individual transponder performance may be better than specification. It is worth noting that for future satellite transponders, benefits could be gained by fitting a state of the art crystal resonator to the reference oscillator in order to guarantee optimum performance with complex modulation schemes. The predicted figures however, give the worst case performance that can be expected regardless of the individual transponder used.

In contrast with coherent modulation schemes, as exposed in §6.6.2, the problems of non coherent systems increase with data rate. For very low data rates (<100bits/s), non coherent systems may offer significant performance advantages. Differential demodulation techniques may be more robust in terms of reference resonator phase noise, but may be more critical in terms of synthesiser phase noise and discrete spurious unwanted signals.

Application of the direct modulation scheme to the satellite data systems resulted in notable improvements in performance, particularly with respect to QPSK with Viterbi. Not only was the phase noise of the synthesisers much reduced, but a reduction of the total number of oscillators resulted in reduction of overall link phase noise. The improvement to the phase noise performance of the synthesisers resulted partly from the use of a direct digital synthesiser and partly from the use of step recovery comb generators. Using the DDS enabled low phase noise to be achieved together with fine step sizes. Use of step recovery diodes enabled an overall frequency coverage greater than that possible from usage of DDS alone. If care is taken in the design of step recovery circuits, as discussed in chapter 7, superior phase noise performance to other commonly used techniques can be achieved. Another advantage of these synthesiser techniques is the use of wide loop bandwidths enabling greater immunity from vibration effects. The problem of increased sensitivity degradation at high data rates due to VCO phase noise can be solved by the use of a YIG oscillator. Such oscillators enable a unique combination of wide tuning range and moderate phase noise levels.

Having obtained results from a computer aided phase noise analysis, measurements taken on an actual satellite data system will be discussed in the following section.

9.10 Measurement of phase noise effects on system performance

As part of the Pandata program [Garret, 1986] a satellite modem receiver was built and used to evaluate local oscillator effects on a BER performance. Input data was conveyed at 20.48 kbits/s. The modem employed half rate seven segment Viterbi decoding with convolutional encoding. A VCXO drives a phase locked oscillator, which constitutes the first local oscillator. This oscillator forms the VCO in a long loop type carrier recovery loop.

A conventional analogue type demodulator was used incorporating the squarer described in chapter 4. Two alternative local oscillator schemes were tried for the second and third local oscillators. One such line up included PMR-type CMOS single ICs. An alternative line-up included synthesisers designed for low phase noise and included the two phase detector technique described in chapter 5.

Using a specially calibrated modem test set-up, the equipment BER was measured under a range of signal to noise ratios. The measured BER results were plotted giving the phase noise degradation plot of fig9.39. The left curve is the theoretical curve for the BER assuming perfect carrier recovery and no intersymbol interference.

A measured curve taken with the 2-phase detector synthesiser is displayed in the centre. This curve includes degradations due to differential encoding and filter matching. At the right hand side, a curve shows the results obtained by using the single chip CMOS synthesisers as local oscillators. The steep upward curve at the top may be due to carrier unlocking giving bursts of errors. An average of 10 BER measurements were taken to improve accuracy. Referring to fig9.28, for a 6° static phase error, the degradation in sensitivity for a BER of 10^{-6} for an information rate of 20kbits per second was approximately 1dB for the CMOS synthesiser. The phase noise analysis program gave a sensitivity degradation of 1.5dB, a discrepancy of 0.5dB, but the measured figure does not account for any phase noise contributions from the satellite transponder and transmitter. To illustrate the relative contributions of the various phase noise sources in more detail, table9.3 displays the results from applying the phase noise analysis to the modem described in this chapter.

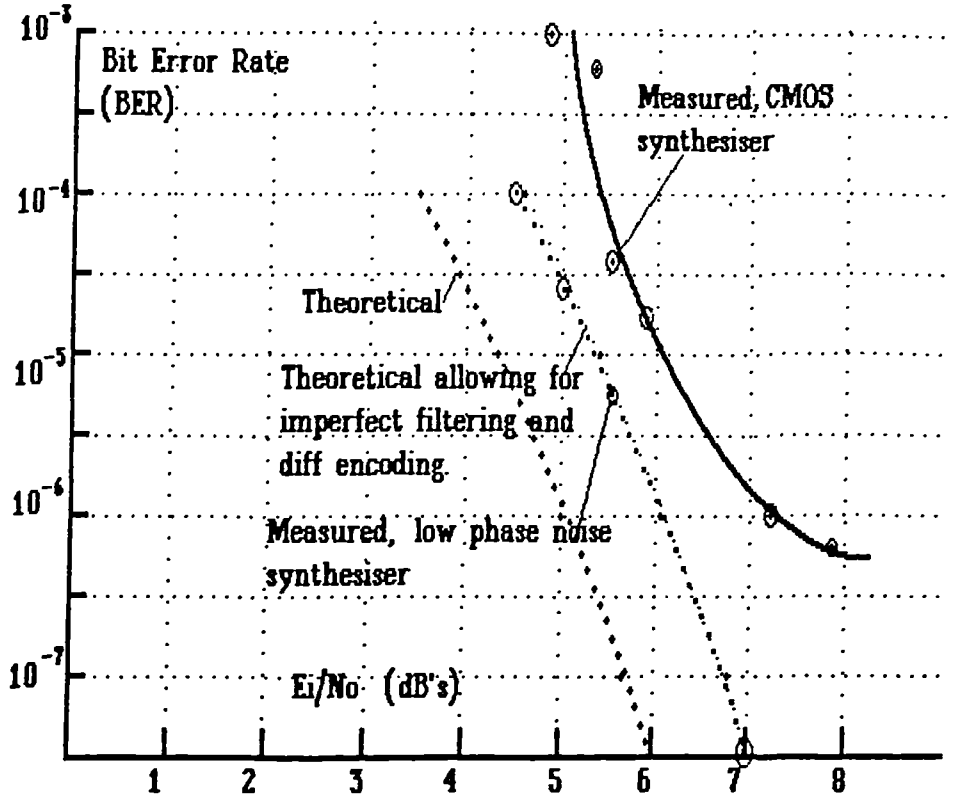


Fig 9.39 Measured BER curves for satellite modem using Viterbi soft decision

TABLE 9.3

	CMOS SYNTH	*LOW NOISE SYNTH*
Fine synth	2.1°	0.69°
coarse synth	7.6°	0.28°
1st LO	0.5°	0.5°
ground stat	4.0°	4.0°
sat transpond	3.0°	3.0°
total 1way	9.3°	5.1°
2way	11.56°	3.13°

The CMOS synthesiser contributed vastly more to the phase jitter than the specially designed low noise synthesisers or the first local oscillator in the downconverter. Despite the fact that the first local oscillator was at the highest frequency, the fact that a simple phase locked oscillator was used rather than a close frequency stepping synthesiser resulted in lower phase noise levels. The satellite transponder and ground station make a relatively high contribution of 5° to the overall phase noise budget. If CMOS synthesisers are used throughout a 2 Way link, the phase noise budget accumulates to an excessive 11.56°, but if a low phase noise direct modulation transmitter is used, the phase noise is a much lower 3.13°, and is still dominated by the satellite transponder phase noise.

Another point of note was that with the CMOS synthesisers, the setting up adjustments for the demodulator were far more critical for phase offset, DC offsets and soft decision levels than for the low noise synthesiser. This could be expected as the phase noise adds extra error margins. In terms of dynamic phase noise performance, the CMOS synthesiser gave bursts of high error rates and even carrier recovery lock loss when the unit was subject to moderate vibration levels. Vibration was not a problem with the low noise synthesiser. Such problems could be accentuated by the narrow phase locked loop bandwidths used in the CMOS synthesiser in order to optimise the static phase noise performance and reduce reference feedthrough spurious.

9.11 Conclusions

This chapter has demonstrated possible improvements to satellite system performance gained from application of the synthesiser techniques discussed earlier in this thesis. Improvement of the spurious response of direct digital synthesis (DDS) presented already in chapter 8 has enabled much improvement in system performance to be demonstrated, together with considerable simplification. Having an acceptable DDS performance has enabled us to propose a direct modulation scheme *that has only one local oscillator* in the transmitter.

The receiver was unfortunately not as easily simplified as the transmitter. However, a direct digital synthesiser was suggested for implementation in a local oscillator that could be used for signal tracking instead of a VCXO with much improvement in oscillator $1/f^3$ noise. It was proposed that further simplifications could be envisaged with the development of a DDS that can be clocked at microwave frequencies. In this case it may be possible to have a direct output at microwave with out any intermediate conversion.

In order to demonstrate these improvements to system performance it was necessary to analyse satellite communication systems for the effects of phase noise. The design study concentrated on coherent demodulation schemes. Systems are normally specified in terms of a certain bit error rate. System designers are therefore interested primarily in the sensitivity degradation for a fixed bit error rate. This will have direct implications for the system link budget. The aim was therefore to produce a system phase noise link budget analysis which could be performed alongside and possibly iteratively with the normal system link budget. Integrations were carried out under the phase noise curves of all the local oscillators in the system taking account of the carrier recovery loop (CRL) response. Such an integration resulted in a value of carrier recovery jitter for each local oscillator.

This jitter was summed and converted into BER degradation by means of the BER curves produced in chapter 6. As a new value of signal to noise ratio is reached, changes to the thermal noise jitter component of CRL jitter occur. This change means that the computer program undertook several iterations before the correct value of sensitivity degradations were reached. Sensitivity degradations were plotted over a wide range of data rates using the carrier recovery loop bandwidth as a parameter.

The free running DRO oscillator gave poor performance even with uncoded BPSK over most data rates. However, when a phase locked first LO was used, uncoded BPSK was shown to be not sensitive to synthesiser phase noise. With coded BPSK, and all offset QPSK schemes, performance degradation was evident unless low phase noise synthesisers were used. In particular, coded QPSK demanded the use of the lowest noise levels of all the synthesiser schemes studied. For very low data rates, even the use of state of the art crystal oscillators resulted in significant degradation. In this case, it may be necessary to use non-coherent demodulation techniques.

When the lowest phase noise local oscillator configuration was selected for the terminal, the performance was ultimately limited by the satellite transponder phase noise. If the satellite transponder phase noise could be reduced, then benefits could be gained for the higher order modulation schemes. As a result of the work in this chapter, a case can be made for revising the specification for transponder phase noise so that maximum advantage can be gained from improvements in synthesised local oscillator technology.

A satellite modem terminal was tested with different synthesised local oscillators for BER performance. Measurements revealed that for a 20.48 kbits/s modem using BPSK with Viterbi, an additional penalty of 1 dB in sensitivity was incurred by the use of single IC PMR type synthesisers. Such a level of sensitivity loss agreed with predictions from the analysis described in this chapter. Under vibration, the degradation was even worse, with the CRL intermittently losing lock.

9.12 Further Work

The split modulation scheme suggested in this chapter must be simulated and tested to evaluate any performance degradation from imperfections in the signal constellation. Such a scheme could then be built and tested in an actual link. Simulation of the above could be extended to include the use of a very fine stepping DDS with a view to eliminating the use

of any analogue tuned oscillator in the carrier recovery loop. Dither interpolation (see chapter 8) would be required to eliminate limit cycle oscillations between frequency steps.

By modifying the integrations in the above analysis it may be possible to predict phase noise degradation effects for non coherent demodulation schemes.

The phase noise analysis results presented in this chapter could be compared with a simulation. In order to perform a suitable simulation, a suitable model of Gaussian distributed $1/f$ noise would be required and also it is necessary to test the accuracy of any Gaussian distributed noise source used in the simulation.

The phase noise analysis program needs to be written into a complete package complete with a user friendly interface, such as Microsoft Windows, and marketed as a design tool for satellite communication System Engineers. Such an analysis program could be made more flexible by expanding it to include non-coherent PSK and FSK demodulation techniques.

9.13 References

Avantek 1990 data sheet for IFD50010.

Benn, H.P. & Jones, W.J. 1989 A fast hopping frequency synthesiser. *Conference Proceedings Conference Publication 303, 2nd international IEE conference on frequency control and synthesis, April 1989 ,Leicester.* p. 69.

Besson, R. & Peier, U. 1980 Further advances on BVA quartz resonators. *Proc. 34th Annual Frequency Control Symposium 1980,* pp 175 182.

Britten, P.D. & Martin, J.B. 1989 Frequency synthesisers for the Prodat Aeronautical Terminal. *IEE conference on frequency control and synthesis, Leicester 1989.*

Dalquist, G. & Bjorck, A. 1974 *Numerical Methods,* chap. 6, p. 222. Englewood Cliffs, N.J.: Prentice-Hall.

Davarian, F. & Sumida, J. 1989 A multipurpose digital modulator. *IEEE comms magazine.* Feb. 1989. pp36-45

Eutelsat 1987 Eutelsat SMS specification for Ground Station, *Document no BS 7-40 Rev. 1E,* vol IV, P31

Eutelsat 1989 Eutelsat II specification for Satellite data link equipment, *Document no Eut.PS.ASCA 0054/E110* Issue 5 P35

Garrett, P., Firman, D. & Hodson, K. Data distribution by satellite. *Journal of the IERE.* Vol. 58, No. 3, pp. 109-116.

GCEL 1990 Specification RE0749 for a Frequency synthesiser for a data communications system. *GCEL, Bangalore, India.*

General Microwave 1988 *General Microwave data book for components and instruments*, p. 5.

Heron R., Marston, P. & Garrett, P. 1989 The Development of a coded 8 PSK modem using digital signal processors. *International Journal of Satellite Communications*, Vol. 7, pp. 67-77.

Holmes, J.K. 1982 Coherent spread spectrum systems. chap. 5, p. 130. Wiley.

Inmos 1989 Rapid carrier acquisition using parallel processing techniques. *Transputer Application notes 1989.*

Marston, P. 1987 Software development for a TMS320 based demodulator to be incorporated into the Skyphone project modem. *Internal publication CSR Ltd Ilkley.*

McCune, E. 1987 Direct digital synthesis and the numerically controlled modulated oscillator. *Proceedings of RF Technology 1987.* p. 414.

Papoulis, A. 1965. *Probability, random values and stochastic processes,* NY: McGraw-Hill P266, Chap 8.

Payne, J. June 1984 Synthesisers- An equation for cost effectiveness. *Microwaves and RF* Vol 23, No 6, p. 89.

Plessey 1988 *Plessey digital signal processing handbook.* Application brief AB 02 p. 79.

Rohde, U. 1983 *Digital PLL frequency synthesisers, theory and design.* chap. 2, p. 86. N.J.: Prentice Hall Inc.

Saul, P.H. & Taylor, D.G. 1989 A 2GHz Clock Direct Frequency Synthesiser. *IEE Conference on Frequency Control and Synthesis Leicester 1989*

Scott, R.I.H. & M.J. Underhill, M.J. 1980 F.M. modulation of frequency synthesisers. *IERE International conference on land mobile radio, Conference Proceedings 1980, Lancaster.* p.183-191.

Vaughan, R.G ,Scott, N.L & White, D.R. 1991 The theory of bandpass sampling. *IEEE Transactions on signal processing* Vol. 39, No 9, pp. 1973-1984.

Wilson, M.P. & Tozer, T.C. 1989 The effect of local oscillator phase noise in low data rate satellite receivers. *IEE Colloquium digest 1989/114, "Modems and codecs for satellite Communications" October 1989, London.*

Zavrel, R.J. 1988 Digital modulation using the NMCO. *RF Design* March 1988 p. 27-32.

Zeigler, R. 1988 Statistical analysis of Allan Variance, ageing, phase noise, and gravitational sensitivity of quartz crystal frequency standards, *RF Expo West,* Anaheim, California, Feb 1988.

10 Conclusions and further work

10.1 Conclusions

This work began by investigating the origins of phase noise and it was shown that at close to carrier offset frequencies there is a particular problem with flicker noise, especially with respect to oscillators. Measured results on oscillators often give worse phase noise figures than would be expected from application of straightforward oscillator theory; this has been traced to the effect of the resonator in producing phase noise in addition to that of the amplifier. Phase noise effects become significantly worse as the tuning range of oscillators increases; although some of this may be explained by the reduced loaded Q of the oscillator tuned circuit, the predominant effect was shown to be due to the tuning element itself. As the frequency of oscillators is increased, the phase noise degradation was found to be worse than the $20\log N$ factor; at higher frequencies loaded Qs of the oscillator resonators are in general lower, and the flicker noise levels of the active devices higher.

The simplest type of synthesised downconverters on the market are for satellite TVRO applications, consisting of a free running microwave oscillator at the front end and an effectively free-running wide tuning range VCO at one of the subsequent stages. Since it was shown that this approach gave far from satisfactory results for most low data rate modulation schemes, guidelines had to be produced to aid the selection of suitable synthesisers for satellite data communications systems. In the course of such action, a threshold effect was noticed on the link BER for increasing levels of phase noise and it became clear that a phase noise link budget was required to be calculated concomitantly with the usual communications link budget. For improved signal to noise ratios, a reduction in the above mentioned threshold has been found to accompany lower Bit Error Rates(BER); thus the expected extrapolation to lower bit error rates would not occur in the presence of phase noise. When coded channels are used, the link is even more sensitive to phase noise because more of the phase noise link budget is taken up by the increased

level of thermal noise induced jitter which results from squaring loss in the carrier recovery process. In addition to the phase noise, other problems such as phase "hits" and vibration can have an adverse effect upon the link. Especially when higher order modulation schemes are used, it was shown that the close to carrier phase noise performance of a crystal oscillator transferred to the microwave local oscillators is critical. It was found that a tuneable oscillator needs to be present within the carrier recovery loop; this oscillator should be capable of capturing the input signal over a frequency range sufficiently wide to allow for all uncertainties in the system. Unfortunately conventional wide tuning range analogue oscillators cannot provide satisfactory close to carrier phase noise levels for higher order modulations schemes.

A detailed survey has been undertaken into synthesiser performance which identified a number of limitations, and some respective solutions were proposed. The commonly used divide by *N* phase locked loop synthesiser in general gives high phase noise levels and is prone to instability as a result of phase detector non-linearity. These problems were shown to be overcome for a synthesiser with coarse frequency step size by means of a two phase detector approach, using the divide by *N* loop to find lock and a Step Recovery Diode (SRD) sampling phase detector to maintain lock. Although the latter device may show chaotic behaviour under certain circumstances, it can be used to obtain much better phase noise performance providing that the synthesiser reference frequency is high. Simulation software was developed for the SRD comb generator and was shown to be capable of predicting chaotic modes of operation. In addition, the effect of noise and spurious signals was shown to be enhanced for increasing offset from carrier frequencies.

In general, satellite data system downconverters and upconverters require finer frequency step size than can be provided by the above single loop solution. Therefore other techniques were considered and Direct Digital Synthesis (DDS) was found to provide a solution to the problem of microphony and phase hits. DDS can provide such fine frequency resolution that the problem of tracking frequency uncertainties in a satellite link can be solved. However, the discrete spurious sideband levels from existing DDS clocked at high speeds were excessive for most local oscillator applications.

Considerable investigation culminated in the development of techniques which reduced the close to carrier spurious signals. Using a DDS modified to include two DACs and a random offset it was possible to vastly reduce the discrete spurious signal levels by converting them to broadband noise (decorrelation). The resulting noise sidebands are then frequency independent. Such a modified DDS can effectively become a broadband tuneable oscillator with the close to carrier phase noise performance of a fixed frequency crystal oscillator.

A suitable combination for a fine resolution microwave synthesiser was found to be a modified DDS feeding a YIG phase locked oscillator. YIG oscillators are capable of excellent phase "hit" performance by virtue of their mechanical rigidity. A further advantage of the above described hybrid synthesiser is that the SRD sampling phase detector is operated at zero offset frequency thus the SRD enhancement of noise is avoided.

A method of combining the synthesiser described above with the upconverter in the transmitter was proposed. This utilises the phase modulation capability of the DDS. In PSK systems if the baseband modulation is resolved into phase and amplitude modulation, and the AM component applied at the synthesiser microwave output, the upconversion has to transmit phase modulation only. Considerable simplification may then be achieved by substituting a wideband PLL for the several stages of mixers, filters and amplifiers normally required for upconversion.

Software was written to enable the prediction of link sensitivity degradation from a given synthesiser performance. This showed that system performance improved with reduction in synthesiser phase noise levels only up to a certain limit, which was determined by the satellite transponder phase noise. There is thus clearly a case for a reduction of future satellite transponder phase noise levels to enable the use of more bandwidth efficient modulation schemes.

10.2 Summary of original work

This thesis presents a new coherent approach to the problems of phase noise in satellite communications systems; some relevant material was previously available in a somewhat piecemeal form, spread throughout different publications. An original aspect of this approach is the consideration of the effect of synthesised local oscillators, rather than local oscillators in general, as sources of phase noise. Such a strategy elicits a detailed investigation of synthesiser performance with a view to synthesiser applications in satellite communications systems; this seems a promising alternative to the general applications approach usually taken. A number of key areas of concern relating to synthesiser performance is highlighted, and solutions developed to some of these problems.

One of the above highlighted problems is discussed in chapter 3, that is the contribution of the resonator to the phase noise of high Q oscillators such as crystal and SAW oscillators. This is shown to be predominant over other sources such as those in the maintaining amplifier circuit. It is shown here that a contradiction arises among various authors' findings as to whether RF flicker noise is device dependent or not. A general consensus of opinion indicates that Ga As devices are worse with respect to generation of flicker noise.

The study of synthesiser performance included a detailed investigation of suitable synthesiser architectures for satellite communications usage which is covered in chapter 4. Resulting from this are recommendations for a unique hybrid of those synthesiser techniques which is most suited to the particular demands of satellite communications work.

Chapter 5 brings together in one section guidelines for synthesiser component design with the aim of avoiding the problems frequently observed within synthesisers. Some of these guidelines are the author's own work, and others are taken from various publications. Among the problems covered are: aliasing of spectral components and noise by limiters and dividers; the problem of phase frequency detector linearity and phase noise; and injection locking in phase locked loops. A method of overcoming the problems of the phase frequency detector was developed during the course of this work. The detector is shown in chapter 5 to give improved performance. Software has been written using an original approach to analyse a PLL synthesiser in the time domain. This software was used to model the effect of injection locking and to show the effect on vibration induced phase noise of using a third order type 3 loop. Investigation of phase detectors led to the development of a novel image rejecting phase detector which is especially suitable for transfer loops in synthesisers as a result of its property of rapid rejection of the unwanted image frequency in such circuits.

A comparison of various frequency multiplication techniques in terms of phase noise occurring in excess of that expected from the $20\log N$ rule is presented here. In addition to this, a method giving only $10\log N$ increase in phase noise and based upon non-coherent sources is discussed.

In chapter 6, the expertise gained from the study of synthesisers is used to predict the effect of using synthesised local oscillators on a satellite data link. Here is presented a concise account of the effect of phase noise upon a satellite data link using coherent demodulation, a topic not often covered in literature on satellite data systems.

An in depth study is presented in chapter 7 of the SRD comb generator. No other publication was found to reveal this much detail on these important devices. SRDs are receiving a resurgence of interest due to the availability of integrated microwave sampling phase detectors using SRDs. This chapter is thus of particular relevance to modern synthesiser design. One novel aspect of this discussion is the splitting of multiplier excess phase noise into two sources: the enhancement of noise already present by more than the theoretical multiplication ratio, and noise indigenous to the devices. In some cases the contribution of the former can result in severe increase of phase noise levels due to the onset of chaotic behaviour. Chapter 7 constitutes a breakthrough in the study of these devices since no evidence has been found of chaos theory previously being used to explain SRD behaviour. Software has been written to perform a time domain simulation of the SRD comb generator to illustrate the chaotic modes of behaviour, and to investigate the effect on the enhancement of phase noise levels. Such software is used to estimate the effect of statistical fluctuations in carrier recombination upon the indigenous phase noise of the SRD.

The application of DDS to frequency synthesis has up to now been hampered by the preponderance of spurious products that arise during the process of generating a synthesised analogue signal. During the course of this work it was found that the spurious products could be much reduced by the process of DAC decorrelation, and this became the subject of a patent application. Such a method converts the localised unwanted spurious signal to random broadband phase noise. The phase noise density of such noise is a negligible contribution to the overall phase noise of a satellite data link. Widespread possibilities therefore exist for application of this technique to such links. The technique described above resulted in reduction of the spurious glitch spectrum of the DAC to such an extent that it became possible to apply a further technique not previously applied to this form of DDS, viz. interpolative dither. By applying interpolative dither together with DAC decorrelation it is possible to achieve unprecedented spurious signal levels with 8 bit DACs.

Having developed a DAC spurious reduction technique, it is possible to propose new applications for DDS. One application proposed in chapter 9 is to form an integrated transmitter synthesiser approach. The novel way of achieving this suggested in chapter 9 is to split the modulation into phase and amplitude components, applying the amplitude component at the final transmitter frequency and the phase component to the DDS. Previous methods apply the AM component digitally within the DDS. Transmitter design should be greatly simplified using the new method because the requirement for linear upconversion will be avoided. This method reduces system phase noise levels by reducing the total number of local oscillators to one.

Finally a novel approach to link budget analysis is suggested in chapter 9. Software was developed to calculate the impact of local oscillator phase noise upon link sensitivity. The novel feature of this software is that the calculation of the thermal noise jitter is performed iteratively from the result of the calculation of system sensitivity, since the thermal noise level decreases with the receiver sensitivity. This enables the program to more accurately evaluate the effect of phase noise on systems that use forward error correction.

10.3 Further work

The issue of flicker noise has still not been properly resolved. There is in particular a requirement for further investigation into flicker effects within frequency multipliers, dividers and phase detectors as discussed in chapter 5. Further optimisation with the aid of computer simulations will be required to ensure fast frequency changes with the 2-phase detector method. The problem of injection locking requires investigation to enable the non linear effects to be included in the time domain simulation and so enable accurate calculation of the lockup transients.

For the system analysis for phase noise covered in chapter 6, the analysis assumed that most of the phase jitter is close to carrier and therefore is within the carrier recovery loop bandwidth. Therefore, the Tikhonov distribution used may have to be modified if most of the phase jitter lies outside the CRL bandwidth as in the case of a synthesiser with frequency independent phase noise characteristics.

The split modulation scheme of chapter 9 could be simulated and built for evaluation. If a fine stepping DDS is to be used, then it should be possible to eliminate any analogue tuning required in the CRL.

Modifications to the phase noise link budget analysis program discussed in chapter 9 are recommended to enable the analysis of non-coherent modulation schemes. A continuation of this software development programme would be to add a user friendly interface to the software and market the complete package as an invaluable design tool for system design engineers. This phase noise analysis could be further validated by comparison with a signal processing simulation of the link. However, a means of simulating Gaussian 1/f noise would have to be found.

To enable the SRD simulation program of chapter 7 to accurately predict phase noise levels, some further information is required. A value is required for the levels of statistical fluctuations in the diode carrier lifetime.

Having demonstrated a working SRD simulation program, it could be used to guarantee the stability of the comb generator by investigating the effect of different reference signal waveshapes. Chapter 7 raised the suggestion that there may be an optimum drive waveform that guarantees stability.

Although the spurious reduction techniques demonstrated in chapter 8 proved viable, a prototype high speed modified direct digital synthesiser needs to be built and evaluated. To make the technique viable commercially, the modified DDS would need to be integrated into a custom logic array. The cost of committing such a design to a custom device rises with increasing clock speed. Some market research is therefore necessary to establish the maximum clock speed that will ensure an adequate return on the initial investment made. This DDS design could then be incorporated into the DDS/YIG synthesiser which is proposed in chapter 4 and also recommended for construction and evaluation.

Appendix

A.1 Introduction

The appendix gives pseudocode and descriptions for the software written during the course of preparation for this thesis.

Turbo Pascal was used as the main language, designed to execute on a IBM PS2 compatible computer with a 33MHZ clock speed 80386 as the CPU, a 80387 numerics co-processor, and 4 MByte of dynamic RAM. Unfortunately, the maximum data files accessible by Turbo Pascal is 64 kbyte, and therefore supplementary programs written in 80386/80387 assembler had to be written in order to handle the large data files created by time domain simulations.

For clarity, the source code is omitted, but pseudocode is presented based on ADA type constructs [Young, 1984]. For the important sections of code, data flow diagrams and structure charts using standard software engineering notation [Sommerville, 1989] is given. The data flow diagrams illustrate how data is handled by the algorithms within the code, and structure charts illustrate how each section of code relates to the program as a whole.

A.1.1 Pseudocode for global packages

```
Package Getextm is

    -- This package contains an assembler code procedure which stores blocks of
    -- data in extended memory, which would not be accessible if assembler code
    -- were not used.


    Procedure Store_extended_mem(ext_mem_add    : in :    LONGINT;
                                 block_size             : in :
    INTEGER;
                                 data_array             : in :
    COMPLEX)  is
    begin
    -- Ext_mem_add is the address in extended memory where the incoming data
    -- is stored.
    -- Block_size is the logarithm to the base 2 of the number of bytes data to be stored.
    -- Data_array is the data to be stored, this is an array of complex numbers.
    -- This procedure stores a data block at the given address in extended memory.

    -- This procedure is called by the following:
    -- SRD simulation program, SRD_SIMULATOR in the package SRDSIM,
    -- PLL simluation program, PLL_SIMULATOR in the package PLL_SIMULATOR,
    -- DDS simulation program, DDS_SIMULATOR in the package DDS_SIMULATOR.
    -- The data stored by this procedure is always a time domain file which is used as
    -- input to an FFT.
    end;
end getextm.

Package REAL_TYPES is

-- Package to declare real number types
type SINGLE is a 4-byte floating point IEEE standard number;
type REAL is the 6-byte standard Turbo Pascal floating point number;
type DOUBLE is an 8-byte floating point IEEE standard number;
type EXTENDED is a 10-byte floating point IEEE standard number;

Package NETTYPE is

-- Nettype is a package holding global type declarations
-- for the SRD and PLL simulation programs

-- DATARR is a type defining a 2-dimensional array.
type DATARR is array [inds,inds] of EXTENDED;
type VECARR is array [inds] of EXTENDED;
type INDARR is array [inds] of INDNEG;

type COMPONENT_VALS is record
    l,l2,c1,cd,rx,rf,rsour        :    EXTENDED;
end record;

    --ELEMENTREC is a record type which holds nodal currents and
    --voltages.
    type ELEMENTREC is
        record
            i,i1,i2,ec1,ec2,vl2,vd          :          EXTENDED;
        end record;
end Package Nettype;

Package  netvars is

-- This package holds global variables for the SRD and
-- PLL simulation programs
with nettypes;

-- Declare reference waveform
edriv          :    EXTENDED;
-- Declare file pointer for file which stores values used to plot
-- Feigenbaum diagram. This file pointer is assigned to the datafile
-- 'Fegvals.dat' in the main program.
time_file      :    FILE;
-- Declare offset  representing position in above datafile.
addr           :    LONGINT;
end package netvars;

Package  gplot is

    -- This package contains code for graphics and plotting.

end package gplot;
```

A.2 SRD Time domain simulation program

A.2.1 Introduction

SRDSIM is a program developed as part of this work to perform a step wise linear solution of the differential equations which describe the SRD impulse generator circuit. A brief description of the salient algorithms will be given here followed by a brief description of program structure and the programs outlined in pseudocode.

The following notation will be used:-

y	Variable tested against boundary condition
y(n)	Final value of variable tested against boundary condition
y(n_1)	Initial value of variable tested against boundary condition
y'(n)	Derivative (gradient) of y(n)
t	Time variable
ddt	Present value of time step
ddt_1	Previous value of time step

A.2.2 Time step

The value of the time step used is of the order of the transition time of the diode, typically 50 to 100nsec. A variable time step mechanism is not provided because the value of the higher order derivatives that form the local truncation errors of the integration remained relatively constant throughout the cycle. Unless iterations are being carried out against the boundary conditions, the final nodal values at the end of a time step (tres) are assigned to the initial nodal values (tres_1) before the next time step and the value of time (t) is incremented by the value of the time step (ddt). If, during iteration, the value of t is not incremented, then the initial nodal values are unchanged before the start of the next time step calculations.

A.2.3 Newton-Raphson iteration

A test to determine the sign of y is carried out at each time step. To prevent limit cycle oscillations, the changeover between the forward and reverse modes and vice versa must be accurately defined; to enable this a Newton-Raphson iteration is carried out at the end of each conduction and each reverse component of the cycle to find the exact transition point. The transition point is used to determine the firing angle and phase noise levels.

A.2.4 Newton-Raphson iteration control

Fig A2.1 illustrates the steps taken upon encountering the boundary condition. Shown here are the initial nodal values (the record tres_1) and the final nodal values (tres). The final values contains the negative *y* value, which indicates that the time has gone past the boundary condition of zero *y*. On encountering the first negative *y* value, the gradient y_n' of the curve between the previous two points (tres and tres_1) is calculated and this gradient is used in the Newton-Raphson calculation below. First the old value of time step, ddt is assigned to ddt_1, then a Newton-Raphson interpolation is carried out to estimate the point in time at which *y* is zero. This point is given by a time step ddt back from the time at the end of the calculation that has just completed, ddt being given by:-

$$ddt = -\frac{y_n}{y_n'} \qquad (A2.1)$$

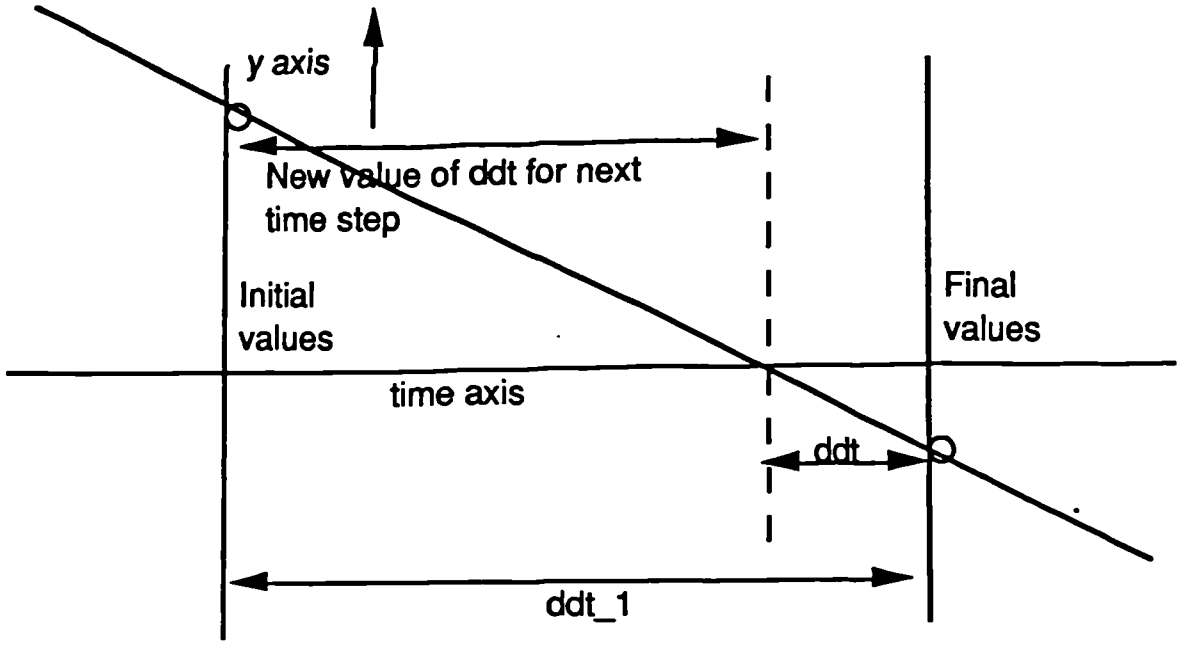


Fig A2.1 Time domain simulation encountering a boundary condition during the first iteration

Variable ddt is then updated as follows:-

ddt := ddt_1 - ddt

thus ddt becomes the time step from the start of the calculation just completed to the estimated zero y value. The first iteration is now complete, and the second iteration is begun with the updated value of ddt. Time (*t*) is not incremented, therefore the initial nodal values at the start of the second iteration are unchanged.

A test is again carried out for negative values of charge. If a negative value of charge (y) is obtained for the second and subsequent iterations, the value of ddt calculated by equation A2.1 for the first iteration is now calculated by:-

$$ddt = -\frac{2y_n}{y_n'} \qquad \text{(A2.2)}$$

This results in the new value of ddt being projected back an equal distance in time on the opposite side of the estimated zero point. A regula falsi iteration is then carried out with the initial nodal values not updated before final value solutions are calculated.

If the value of *y* is positive after the iteration, a full Newton-Raphson interpolation is carried out; thus a new time step ddt is calculated as indicated in equation A2.1 preceding the next iteration. This time the initial nodal values are updated with the previous iteration's final nodal values resulting in the initial nodal values moving much closer to the exact boundary condition point. In summary, positive values of y enable a full Newton-Raphson interpolation, and negative values result in a *regula falsi interpolation. As* Newton-Raphson iterations converge much faster, it is desirable that as many iterations as possible are Newton-Raphson. The reason for the projection back with double the time step using equation *A2.2 is to force a positive value of* y which in turn will force Newton-Raphson iterations. When the value of ddt falls below the value of time step window (t_{window} in §7.5.3 and represented by the variable window in the program) the iterations are stopped and the simulation switches mode. The value of a constant is assigned to the window.variable.

A.2.5 Structure of software

In the main program, the bulk of code is contained within a loop; this loop is performed once for each time step as illustrated in the data flow diagram A2.2. The program consists of a core package, SRDSIM which loops round for each time step.

Code from other packages is accessed which deal with either the reverse or conduction modes depending upon the settings of control flags. A block diagram of the structure of the complete program is given in fig A2.2. Data flow during program execution is given by figs A2.3 to A2.7 for the different objects. For these figures, the rounded edge boxes represent a transformation of data, the square boxes represent file storage, and the circle represents interaction with the outside world. Psuedo-code for the main program is given in section A2.6 below and sections A2.7 to A2.11 give the Psuedo-code for the packages. Apart from essential algorithms, text will be used to describe the processes undertaken. In section A2.12 the pseudocode for the tridiagonal matrix linear algebra solving package will be given.

The exitation waveforms used in the simulation are all sinewaves with options of either added phase noise, A.M noise, or additive noise.

The reverse package contains code which deals with the reverse mode as shown in the dataflow diagram of fig A2.8 and is composed of four parts:-

i) Initialisation,- initialise variables such as alpha

ii) Exitation - Adds noise to input waveform

iii) Time step solution - derives final nodal values from initial nodal values

iv) Boundary value test - testing for boundary condition

For each time step calculation, code from the Reverse or Conduction packages is called by the main loop. Initialisation (see above) occurs once at the point of starting the reverse mode, and a value of the firing angle α is obtained and processed depending upon the plot option chosen. During the reverse part of the cycle, the code from the exitation package is implemented first, this provides the current instantaneous drive level. Following this, the code from the REVSOLV package (see below) is executed, which calculates the final nodal values from the initial nodal values and the time step *ddt*. *Finally*, a test is performed against the boundary conditions.

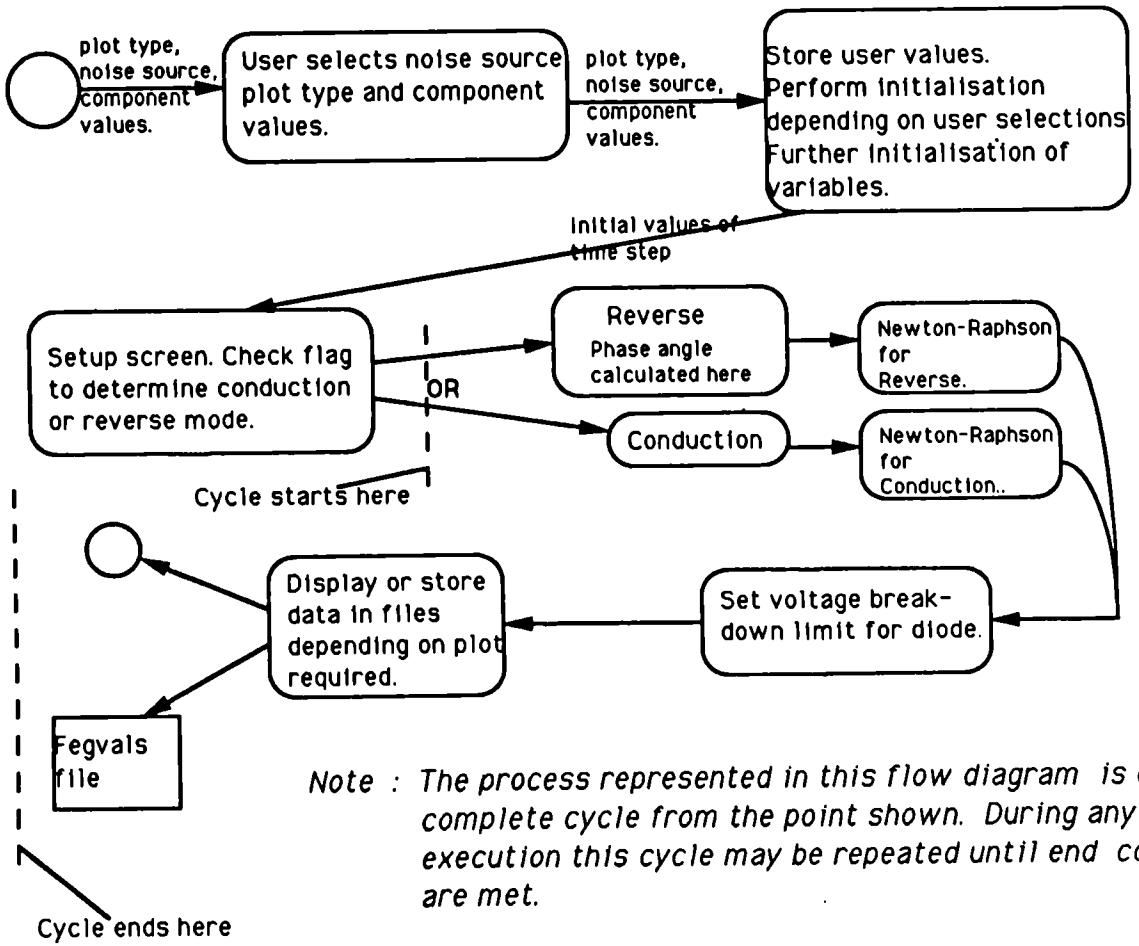
The conduction mode follows similar steps to the reverse mode, but with the addition of two extra steps for determining the intrinsic charge level q and the DC current flow I_{dc} Self bias levels are calculated in the initialisation section of conduction, which is entered only as the first calculation of the mode is performed.

There is an exit point on the main loop where the value of time is compared with an end point condition depending upon the plotting option selected.

The REVSOLV package implements the equations listed as equation number 7.38 to 7.40 in section 7. These calculate the co-efficients to the linear solving matrices of equation 7.37 and passes them to the *tridiagonal solving package TRISOLV*. When the TRISOLV code has been executed, the linear algebra solutions are converted by REVSOLV to give the final nodal values, which then used by either reverse or conduction software.

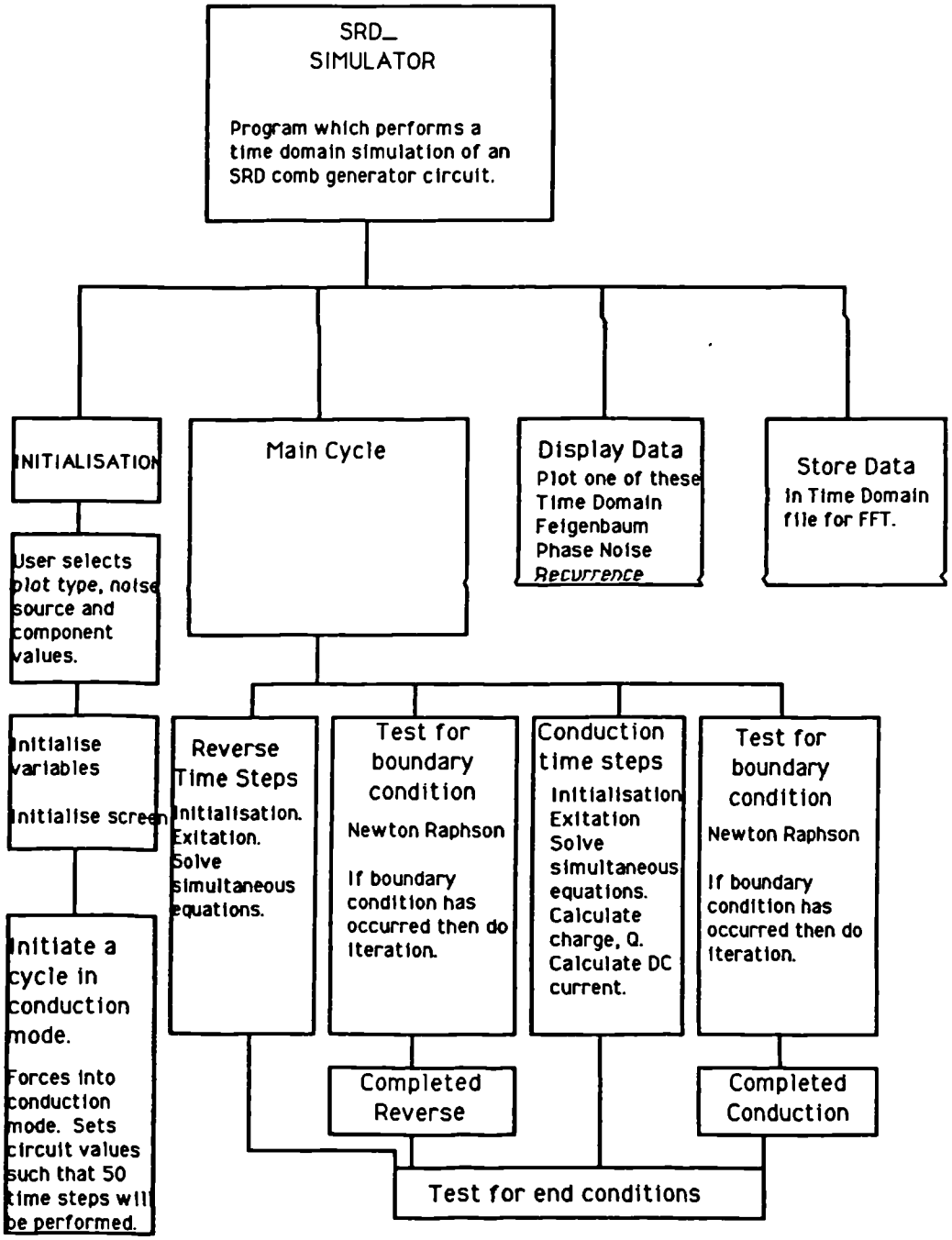
The TRISOLV package was adapted from the linear solving package given by Strang [1980]. This adaption was achieved by omitting the inner loops in the upper and lower decomposition routines. As the inner loops increase, matrix elements are selected from either near the top right hand corner of the matrix, or near the lower left hand corner. Since these are zero in a tridiagonal matrix, these loops can be omitted. Unlike algorithms by other authors [e.g. Sedgewick, 1988], the partial pivoting facility has been retained, but the upper and lower decomposition matrices must be two strips wide, rather than a single strip without partial pivoting.

MAIN LOOP - SRD SIMULATION



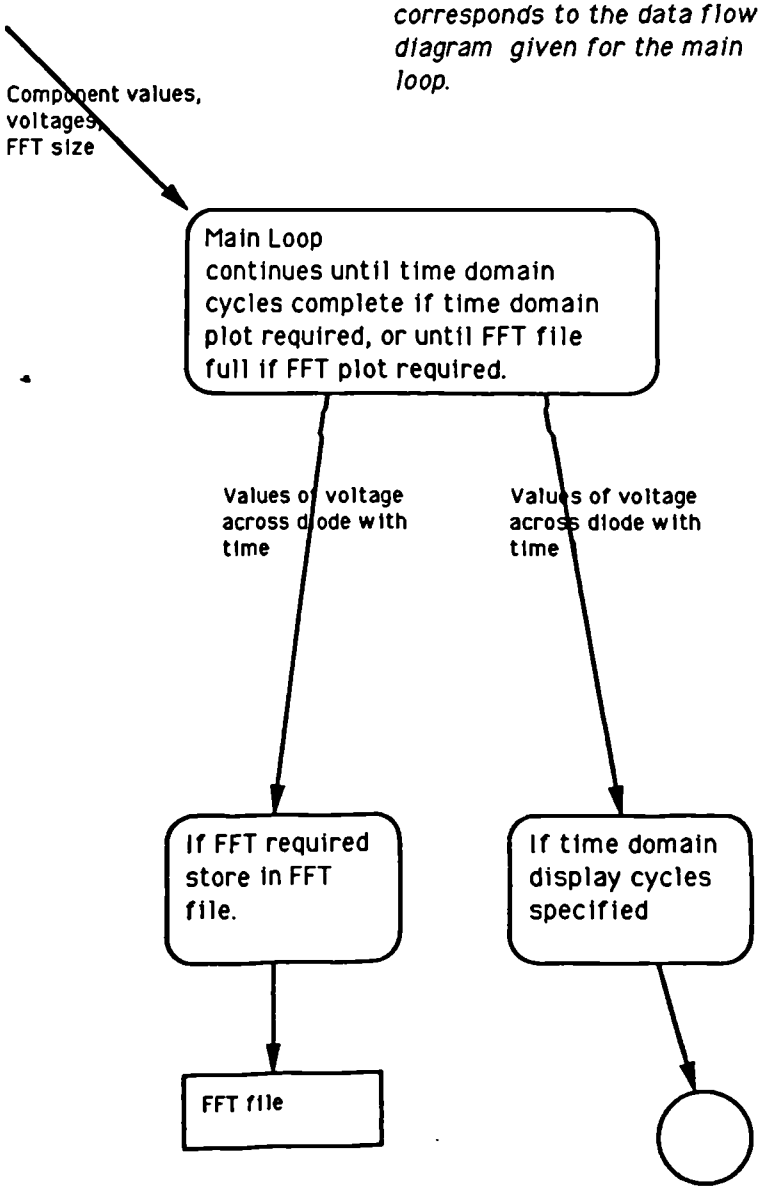
Note : The process represented in this flow diagram is one complete cycle from the point shown. During any single execution this cycle may be repeated until end conditions are met.

Structure Chart for SRD Simulation Program

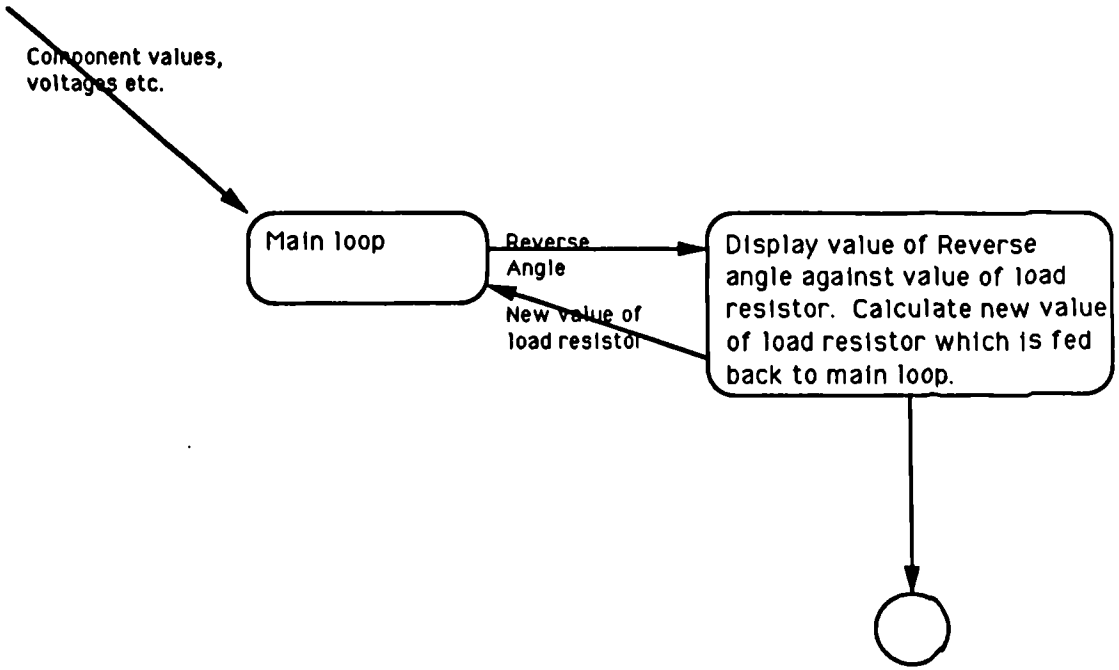


Time Domain and FFT - SRD Simulation

Note : The Main Loop operation corresponds to the data flow diagram given for the main loop.

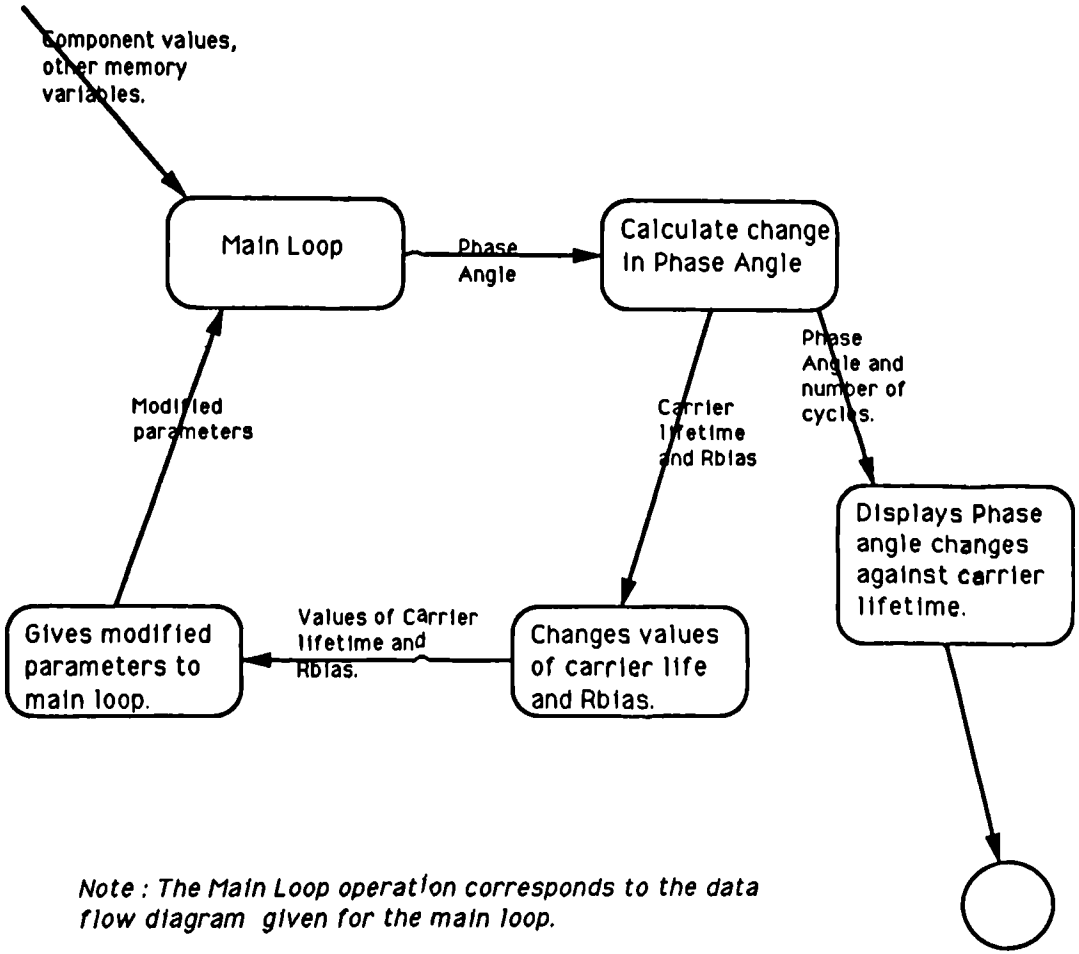


Feigenbaum - SRD Simulation



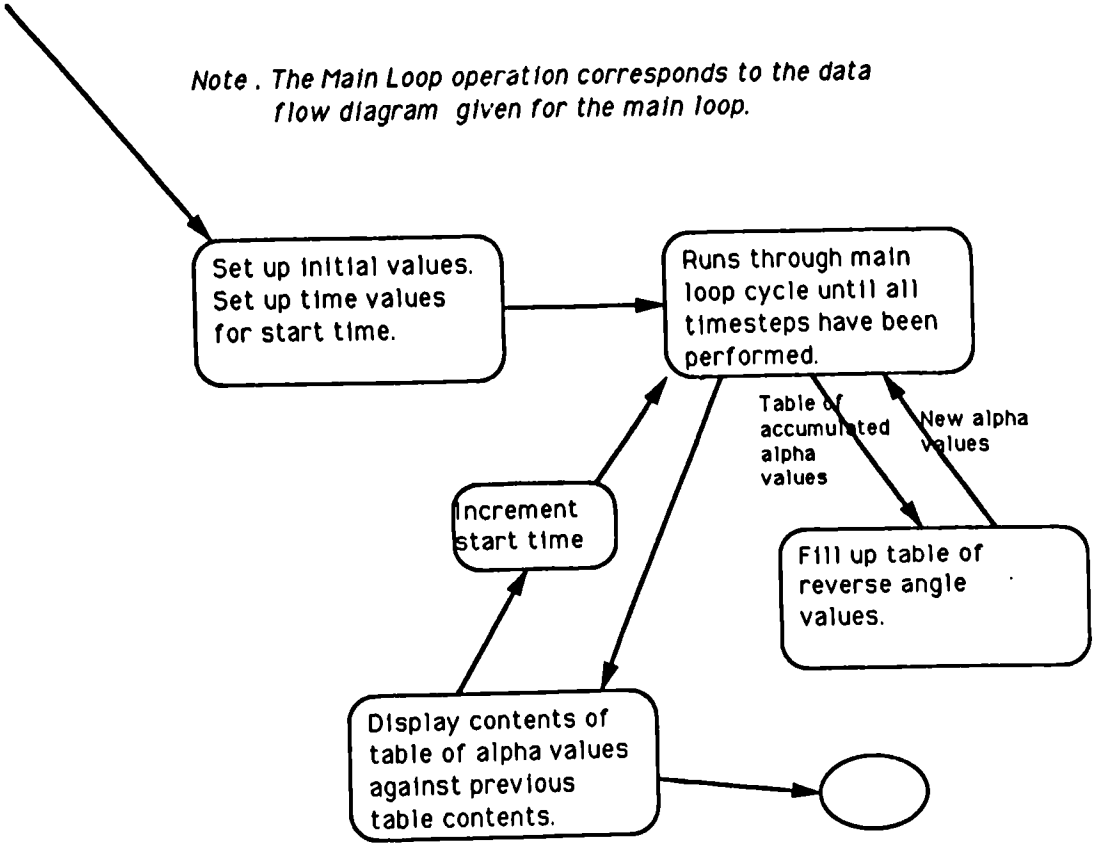
Note : The Main Loop operation corresponds to the data flow diagram given for the main loop.

Phase Noise - SRD Simulation

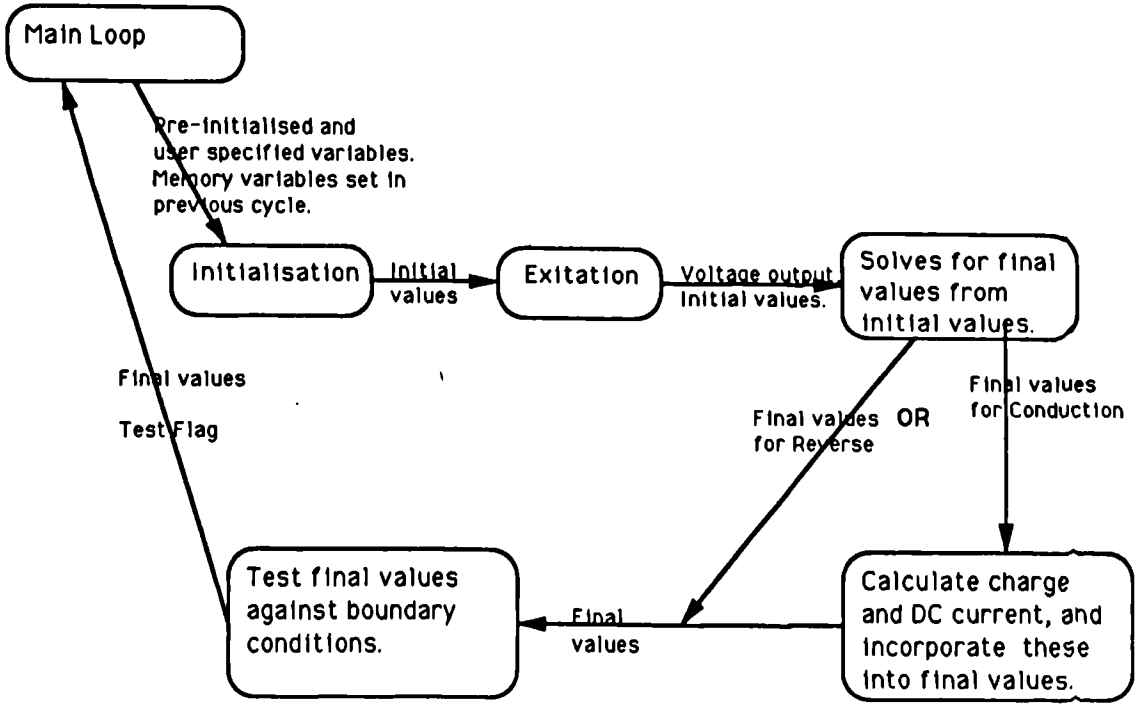


Note : The Main Loop operation corresponds to the data flow diagram given for the main loop.

Recurrence - SRD Simluation



The Conduction and Reverse Cycles - SRD Simulation



Note : The Conduction and Reverse cycles are the same except that charge and DC current are calculated in the Conduction but not in the Reverse cycle.

The Main Loop operation corresponds to the data flow diagram given for the main loop.

A.2.6 Pseudocode for main SRD simulation program

```
Package body SRDSIM is

with CRT, DOS, GRAPH,PRINTER,GRAPHPRN,NETTYPES, NETVARS,   REVSOLV,
GPLOT, USER_INPUT;

    -- This package contains code to perform simulation of a SRD Comb
    -- Generator.
    --Time domain simulation that solves the SRD network over small
    --discrete steps of time.The calculated voltages and currents are
    --displayed on the screen and the output is stored in a time
    --domain file of fftsize for FFT analysis. The time domain file is
    --stored in extended memory.
    --Tres is a record containing the nodal currents and voltages for
    --the network.

    type INDEXP is INTEGER range 1..256;          --4096

    type COMPLTYPE is (r,j);
    --Declare Complex number array type.
    type COMPLEX is array (COMPLTYPE) of SINGLE;
    --Declare integer subrange of 4096 points.
    type POINTS is INTEGER range 0..4095;
   type  PHASARR is array(INDEXP) of EXTENDED;
   type  CNTARR is array(INDEXP) of INTEGER;
    type ELEMENTARRAY is array(1..4) of ELEMENTREC;
    type PLOT_OPTIONS is (time_domain, FFTrans, Feigenbaum,
                                        phase_noise,recurrence);


    --DECLARE VARIABLES.
    --summary of the important variables given below.
    -- Network component values are declared in user_in as these values are entered
    -- by the user.

-- Declare Initial and final values of nodal voltages and currents
    Tres, tres_1  :     ELEMENTREC;

-- Declare Stored carrier charge;
    Q                 :     EXTENDED;
```



```
Procedure interpolation(yn_1,
                        xn_1,
                        yn,
                            xn  : in EXTENDED;
                        absdelddt : out EXTENDED)        is

-- Procedure finds the exact point at which the diode mode changes.
-- This is done by performing Regulo-Falsi and  Newton-Raphson
-- interpolations.

ddt_1,dt_dv,ddtx,delddt      :     EXTENDED;

begin
    -- ddt_1 is the old value of timestep

    ddt_1 := ddt;
    inc(iteration);

    -- Inverse gradient of curve, dt_dv
    dt_dv:=((xn_1 - xn)/(yn_1 - yn));
    if iteration > 20 then
        -- Here call procedure to turn off graphics mode.
        -- Here write to screen  'Newton Raphson convergence error';
        EXIT;
        -- Exit and give runtime error.
    end  if;

    -- Test for negative y,step back an equal amount into the + region for y

    if (iteration > 1) and (yn < 0) then
        ddtx  :=  2*yn*dt_dv;
    ddt := ddt-ddtx;
    else
        ddt:=-yn*dt_dv;
    if iteration  = 1 then
        ddt:=ddt_1+ddt;
        end  if;
    end if;
```

```
    delddt := ddt_1-ddt;
    absdelddt := abs(delddt);
    end Interpolation;

Function Exitation return EXTENDED is
    begin
    -- Returns the intantaneous value of drive voltage.
    -- Selects the relevant type of noise source and adds in the noise voltage.
    return -- returns variable holding instantaneous value of drive voltage.
    end Exitation;


Procedure Reverse is
    -- Calculates the reverse part of the diode cycle and terminates when the diode
becomes
    -- forward biased.

    acctest  :   EXTENDED;
    revres   :   ELEMENTREC;

    begin
    if not testfl then
        -- This block operates once in every cycle at the start of the reverse part of the
        -- cycle and so is used to measure firing angle and change any appropriate
    tcl:=round(fr*(t-t__1));     -- tcl is no of cycles between pulses
        t__1 := t;
        prevcycles := wholecycles;
        wholecycles := trunc(cycles);
        case plot_choice is
            when phase_noise =>
            -- Allow 10 cycles to elapse to allow transients to die
                -- away before making a phase measurement. After the first 10 cycles,
a value of alpha is stored and carrier lifetime, Tau is changed by a small amount. After the
second 10 cycles, a new value of alpha is obtained and subtracted from the first value, this
phase change is used to estimate the phase noise. This phase noise is plotted, and the
next value of TAU to be plotted is fetched, and the whole process is repeated again.

            when Feigenbaum   =>
          If wholecycles > prevcycles then
                Increment resistance values ready for next step
                rset := component_list.rx+1;
        end if;
        angtest := frac(cycles);
        -- Measure values of alpha, and plot against load resistance;
        alpha := 2*pi*angtest;  -- accurate value of alpha
        when recurrence  =>
        angtest := frac(cycles+0.25);
        --Store values of alpha measured in linear array alpharr
        alpha := 2*pi*angtest;  {accurate value of alpha}
        alpharr[alphind]:=2*pi*angtest;  {accurate value of alpha}
        inc(alphind);
    end case;

    -- Select new random values for noise variables.
    case noise_select  is

        when 1,3,4  =>   vni := 1e-2*(2*(random)-1);
        when 2 =>
         Vni := 1e-2*(2*(random)-1)/sqrt(2);
      Vni2:=1e-2*(2*(random)-1)/sqrt(2);
    end case;
    tres.ec2 := vbar;
    testfl := TRUE;
end if;

if updateflag = TRUE then
    -- If the interpolation algorithm is invoked, do not update start
    -- variables.
    tres_1 := tres;
else
    tres := tres_1;
end if;

t_1:=t;

-- If interpolating, previous values must be stored.
-- Updateflag controls whether calculations are to continue
-- from the initial or final values of previous timestep.
-- Final values are used mid region, or when Newton-Raphson interpolations taken.
-- When regula falsi interpolations are performed, then initial values are used.
```

```
    -- This is the input carrier signal.
    edriv := exitation;

    -- Solution block
    solverev(revcoef,ddt,component_list,tres);

    -- Testing for end of reverse cycle
    t0 := t + ddt;

    -- Invoke linear interpolation for end of reverse cycle
        If ((tres.ec2>vbar) and (tres.i>0)) then
            srdflag:= TRUE;
            updateflag := FALSE;
            revflag := TRUE;
        else
            updateflag := TRUE;
            t := t + ddt;
        end if;
     end Reverse;

Procedure Conduction is

    -- Calculates the forward cycle of the diode.

    begin

    -- Testfl determines whether the first calculation of the  forward mode is taken place.
If      so, the self bias levels are calculated from the level of DC current, Idc

    If testfl then
        -- Calculate self bias levels, qtot is total charge accumulated during conduction.
        tcycle := t-toldcycle;
        component_list.rf := rfor;
        If tcycle > 0 then
        -- Average current over 1 cycle to find DC current.
        idc := qtot/tcycle;
        end if;
    qtot := 0;
        toldcycle := t;
        --Calculate new self bias voltage;
    edc := idc*rbias;
    component_list.rx:=rset;
        end if;
    end if;
    --The conduction processing is similar to the reverse processing apart from holding
    --the junction reverse capacitance voltage EC2 constant at VBAR and calculating new
    --values of stored carrier charge Q and reverse current Idc.  Also, the boundary
    --condition test is for the stored charge to be less than zero.
    testfl:=FALSE;

    -- Updateflag controls whether calculations are to continue
    -- from the initial or final values of previous timestep.
    -- Final values are used mid region, or when Newton-Raphson interpolations taken.

    -- When regula falsi interpolations are performed, then initial values are used.
    If updateflag then
    -- Allowing for finite lifetime, q is modified to allow for carrier recombination.
    Iav := (tres.I+io)/2;      -- Find charge Q from integration Idt
    decayfunc := exp(-ddt/Tau);
    {Equation 7.45}
    Q := Q*decayfunc+Iav*Tau*(1-decayfunc);
    -- Total charge summation, used to calculate DC current through
        -- diode so enabling self bias levels to be determined
        qtot := iav*ddt+qtot;    -- add for bias
    end if;

end Conduction;


Procedure User_select is

begin
    -- Allows user to select type of plot required. User selects one of the following :
    -- TIME DOMAIN
    -- FEIGENBAUM
    -- FFT
    -- PHASE NOISE
    -- RECURRENCE
    --Allows user to select type of noise required. User selects one of the following:-
    --BASEBAND ADDITIVE NOISE
    --RF ADDITIVE NOISE
```

```
    --AM NOISE
    --PHASE NOISE
    --BROADBAND ADDITIVE NOISE

end User_select;



-------------------------------------------------------------------------
-- BEGINNING OF MAIN PROGRAM
-------------------------------------------------------------------------

PROGRAM SRD_SIMULATOR is

    --Begin main program.
    --SRD_SIMULATOR is Main Program to simulate a SRD Comb
    --Generator.


begin

    -- Ask user to choose plot  and noise.
    user_select;
        -- Ask user to verify or change constant values used during processing.
    User_chk_params;
    --Determine starting point
    torig := Arcsin(vbar/epeak)/(2*PI*FR);
    randomize;
    --Initial conditions block
    --Nodal currents and Voltages Final value plane
    TRES.I1:=0;
    TRES.VD:=0.7;
    TRES.vl2:=0;
    TRES.Ec2:=0.7;
    TRES.i2:=0;
    TRES.i:=0;

    --Nodal currents and Voltages Initial value plane
    TRES_1.EC1:=0;
    TRES_1.ec2:=0.7;
    TRES_1.i:=0;

    TRES_1.ec2:=0.7;
    TRES_1.vl2:= 0;
    tstartcond:=0;

    idc:=0;
    TRES.i2:=0;
    TRES.ec1:=0.7;
    startflag:=TRUE;
    revcoef:=xnum;
    q:=0;
    WINDOW:=1e-20;
    timestop:=false;
    vnoi:=0;
    taunoi:=2.5e-9;
    TAU:=100E-9;
    UPDATEFLAG:=TRUE;
    iteration:=0;
    --Address of file for FFT
    tt:=0;
    TRES_1.vl2:=0;
    revflag:=FALSE;
    startflag:=TRUE;
    VBAR:=0.7;
    testfl:= TRUE;
    edc:=0;
    io:=0;
    --add for bias
    starttest:=1/(2*fr);
    --1/(8*fr)
    TMAX:=M/FR;
    tmin:=(m-20)/fr;
    tfft:=10/fr;
    --FFT Increment in time
    fft:=cyc/(fr*fftsize);
    --TMAX/100
    alphind:=1;
    Qo:=0;
    Repeatfl:=false;
    srdflag:=true;
```

```
    startloop:=0;

    --Screen scaling parameters
    Q:=0;
    --Call Procedures to set up graphics screen and graticule
    SET_SCREEN;
    GRATICULE;
    --Calculate starting point
    ESTART:=VBAR/EPEAK;
    t:=ARCSIN(ESTART)/(2*PI*FR);

--Main loop containing calculation for each time increment DDT.

    case plot_choice is
        when time_domain  FFTrans, Feigenbaum => loopsize := 1
        when  phase noise                                          =>loopsize
:=2
        when  recurrence                                  =>loopsize :=29
    end  case;

STARTSIZE: loop
    alphind:=1;
    loopflag := FALSE;
    firstflag := TRUE;
    taucount := 0;
    increment(startloop);
    phasefl := true
    -- In source we initialise Tres and tres_1 here.

    Repeatfl := FALSE;
    srdflag := TRUE;
     timestop:=FALSE
    updateflag := true
    iteration := 0;
    tt := 0;
    rbias0 := rbias;
    testflag := TRUE;
    edc := 0;
    --Allow 10 reference cycles before starting FFT;
    tfft := 10/fr
    wholecycles := 0;
```



```
    fft := cyc/(fr*fftsize)
    starttest := 1/(2*fr)
    case plot choice is

        Feigenbaum        =>
                              component_list.rx:=rstart;
                              noise_select:=Noise_off;
                              --- Here, assign pointer variable to access dos file
                              -- 'Fegvals.dat', which will store coordinates of display
for                           -- Feigenbaum diagram.
                              assign(time_file,'f:\fegvals.dat');
                              -- Prepare file so that data can be written to it.
                              rewrite(time_file,8);
        phase_noise   =>
                              if tstep = 1 then
                                  rbias0:=0;
                              end  if;
                              tau := taumin;
                              taud_1 := tauplot.tmax;
                              taud := tauplot.tmax;
                              --turn noise sources off.
                              noise_select := Noise_off;

        recurrence    =>
                               noise_select:=Noise_off;
                              m:=6;

    end  case;

    srdplot.TMAX :=  M/FR;
    srdplot.tmin  :=  (m-20)/fr;

    t := torig;
    --Step forward starting time with outer loop to effectively change starting conditions
    if (plot_choice = recurrence) then
        t := torig+0.03*tstep/fr-0.06/fr;
    end  if;

    toldcycle := t;
    ddt:=dt;
```

```
loopflag := FALSE;

TIMSTEP: loop
    --dt is default step size
DDT := DT;
    mm := t*fr;
    --Force initial simulation cycle into conduction mode
    if startflag=TRUE then
        --Start flag is set for the initial starting period when diode is
        --forced into conduction mode
        srdflag := TRUE;
        if t>starttest then
            startflag := FALSE;
        end if;
    end if;
    --srdflag determines whether diode is in conduction or reverse
    --mode.

    if srdflag = FALSE then
        REVERSE
    else
        CONDUCTION;
    end if;

    if ((revflag) and (t>1e-8)) then
        --This section carries out Newton Raphson interpolation
        --against the boundary copndition of TRES_1.ec2=vbar for
        --the reverse mode Revflag indicates that the variable is

        --near enough to the boundary condition for interpolation.

        REVERSE_NEWTON: loop
            interpolation(vbar-TRES_1.ec2,
                                t_1,vbar-TRES.ec2,
                                t0,TESTDT);
            reverse;
            --Window is the error limit window for the interpolation.
            if ddt<WINDOW then
                TESTDT:=0;
            end if;
            exit when TESTDT< WIND;
        end loop REVERSE_NEWTON;
    end if;
    revflag:=FALSE;


    if ((Forflag) and (t>1e-8)) then
        --This routine carries out Newton Raphson interpolation
        --against the boundary condition of q=0 for the conduction
        --mode FORFLAG indicates that the variable is near enough
        --to the boundary condition for interpolation.  Similar to previous routine

    end if;

    Forflag:=FALSE;
    UPDATEFLAG:=true;
    -- Resetting iteration because it will have been changed by
    -- Newton-Raphson.
    iteration:=0;
    if ((t < 1e-8) and (q < 0)) then
        t:=t+ddt;
    end if;

    --Set voltage breakdown limit for diode =Vbr
    if TRES.VD < -Vbr then
        TRES.VD := Vbr;
    end if;

    if ((t > tfft) and (plot_choice = FFTrans)) then  -- Take FFT sample.

        -- Linear interpolation between calculation points to give vlin which is
        -- used for the FFT point.

        vlin := srdplot.volts_1 + (srdplot.volts - volts_1)*(tfft-time_1)/(t -
time_1);
        a[r] := srdplot.vlin/(10*vmax);
        a[j] := 0;
        store_extended_mem(tt,8,a);
        tt := tt + 1;
        tfft := tfft + fft  { increment for fftpoint  }
    endif;
```

```
        case plot_choice is
            -- This case statement picks the current value of plot_choice
            -- (entered by the user).
            when Time_domain    =>      -- Plots points on time domain graph, then
if
                                                    -- number of specified
cycles exceeded then
                                                    -- set loopflag is set
TRUE, so main loop will
                                                    -- be terminated.

            when FFTrans        =>              -- If time domain file full then
loopflag set
    -- TRUE.
            when FEIGENBAUM     =>      -- If last value of load resistance plotted is
                                                                -- greater than
the maximum specified load
                    -- resistance then loopflags set TRUE.
        when PHASE_NOISE    =>  -- If last value of Tau value plotted is equal to
                                                    -- specified value then loopflag
is set TRUE.
            when RECURRENCE     =>      -- If the array alpharr is full then loopflag
is
                                                                -- set TRUE.
        end case;
        exit when loopflag

    end loop TIMESTEP;


        -- If recurrence is selected, then each element of alpharr is plotted against the
        -- previous element position.
        -- This process is repeated at the end of each inner loop for the values of
        -- the step selected by the outer loop
exit when startloop = loopsize

        --End of outer loop.
    end loop STARTSIZE;

    --Now loop to hold display until key is pressed.
    loop
        exit when keypressed;
    end loop;
    --Now produce hard copy if required.
    --Hardcopy(1);
end SRD_SIMULATOR;
end package SRDSIM;
```

A.2.7 Pseudocode for revsolv package

```
Package Revsolv is
with   nettype,netvars,trisolv;

-- This package contains procedures which obtain the final value plane from the initial
value
-- plane for each time step.

solrev,
revvec          :    VECARR;

procedure solverev (revcoef       :in:          DATARR;
            xtr           :in:          EXTENDED;
            component_values    :in:          COMPONENT_VALS;
            nodal_variables   :in out:    ELEMENTREC)   is

begin
-- Coding of equations 7.39 to 7.41 in Chapter 7 of main text. This is a linear
-- approximation of the differential equations.
-- This procedure calls Trisolve to solve a linear tridiagonal simulateous system
-- of equations. The solutions to these equations are returned to this procedure.
-- The initial values of nodal voltages and currents (nodal_variables in above parameter
-- list) are passed in to this procedure which changes them to their final values.
end solverev;

end Package Revsolv.
```

A.2.8 Pseudocode for tridiagonal linear equation solving package

```
Package trisolv is

with nettype;
```

```
-- This package contains solves the linear system Ax=B where a is the coefficient
-- matrix, and B is the dependent vector This is a shortened version of a linear
-- algebra solving program as contained in STRANG
-- This package allows high speed processing of a tridiagonal matrix that is
-- of the form :
--          x x 0 0 0.....
--          x x x 0 0.....
--          0 x x x 0.....
--          0 0 x x x.....
-- by  cutting out all the elements which are zero.


Procedure Solvtrilinal (Coeffarr    : in:     DATARR;
                        Yarr    : in:     VECARR;
                        SOLS    : in:     IND;
                        Xarr    : in out :  VECARR) is

begin
-- Takes in the coefficients of the simultaneous equations as coeffarr (in above
-- parameter list) and dependent variable as Yarr and produces the solutions which
-- are elements in the array Xarr which is passed out of this procedure.
end Solvtrilineal;


end Package Trisolv;
```

A2.9 Pseudocode for SRD user interface package

```
Package usr_in is

--This package contains global type and variable declarations used in the main program
-- which accesses this package.  Also within this package is code providing user interface
-- whereby  component values can be selected by the user before the main processing
-- is implemented.

with CRT, NETTYPE, NETVARS;

-- The variables declared below can be checked and modified by the user at runtime
-- before the main processing is implemented.

    -- Network component values
    component_list    :    COMPONENT_VALS;
```



```
    -- Epeak is source amplitude.
        epeak          :    EXTENDED;
    --RD is reverse bulk resistance
        RD         :    EXTENDED;
    --Tau is semiconductor carrier lifetime
        TAU            :    EXTENDED;
    --rstart and rend are start and finishing load resistances for feigenbaum plot
        rstart         :    EXTENDED;
        rend           :    EXTENDED;
    --Fr is the reference frequency
        Fr         :    EXTENDED;
    --Vni is the peak noise voltage
        Vni            :    EXTENDED;
    --Taunoi is the noise timeconstant
        Taunoi     :    EXTENDED;
    --FFTsize is the total number of points on the FFT
        fftsize        :    LONGINT;
    -- Cyc is the total number of reference cycles in the FFT
        cyc        :    INTEGER;
    -- Rbias is the self bias resistance
        Rbias          :    EXTENDED;
    -- Taumin is the minimum lifetime value for the carrier lifetinme-phase noise pl0t
        taumin     :    EXTENDED;
    -- Taumax is the maximum lifetime value for the carrier lifetinme-phase noise pl0t
        taumax     :    EXTENDED;



Procedure Usr_chk_params  is

begin

-- Procedure enables user to read component values to be used by
-- the program,and change them if required.  The variables are read
--  from the file usr_prms.dat and written back after updating.
-- They will not need to be read again by the main program because
-- they will have been assigned to the above memory variables which
-- the main program can access.
end Usr_chk_params;
                                end package Usr_in.
```

A.3 PLL Time domain simulation program

A.3.1 Introduction:

PLL_SIMULATOR is a program which uses a step wise linear method to solve the differential equations which describe a $+N$ synthesiser PLL with a phase frequency detector. A brief description of the salient algorithms will be given here followed by a brief description of program structure. User selectable options exist for injection lock modelling or conversion to a type three loop. A structure chart for the program packages is given as fig A3.1.

The following notation will be used:

PVflag	Flag set when PV exceeds 2π
PRflag	Flag set when PV exceeds 2π
PV	Divided down VCO phase input to phase detector
PR	Reference input to phase detector
t	Time variable
ddt	Present value of time step
ddt_1	Previous value of time step

A.3.2 Time step

The value of the time step used is of the order of the transition time of the logic to be used in the system, typically 10ns. A variable time step mechanism is provided to reduce the step size near the critical 2π point since this is the point where most of the changes to the variables occur during any single reference cycle. As with the SRD simulator, Newton_Raphson interpolations are carried out against a boundary condition to prevent limit cycle oscillations arising due to the time step resolution of the simulator. For the PLL simulator the boundary condition occurs when the divided down VCO phase (PV in program) reaches 2π.

A.3.3 Phase frequency detector

The simulation of the phase frequency detector is implemented in software according to the state machine diagram of fig A3.2. The state of the phase detector flip flops is represented by flags PVflag and PRflag in the program, in the state machine diagram these correspond to VCO phase and reference phase respectively. If the reference phase exceeds 2π first then PRflag is set, or if the divided down VCO phase exceeds 2π first,

then PVflag is set. When both flags are set, they are subsequently reset. These flags become pulse width proportional controllers for the corresponding current sources.

A.3.4 Main program

The main program is formed into a loop which repeats itself for each time step as does the SRD simulator and is represented by fig A3.3. Pseudocode for the main program is given in §A3.7. Outputs to the FFT file and screen are managed within this loop, along with the phase frequency detector operation. The loop calculations for each time step are contained within the PLL calculation procedure PLL_CALCULATION.

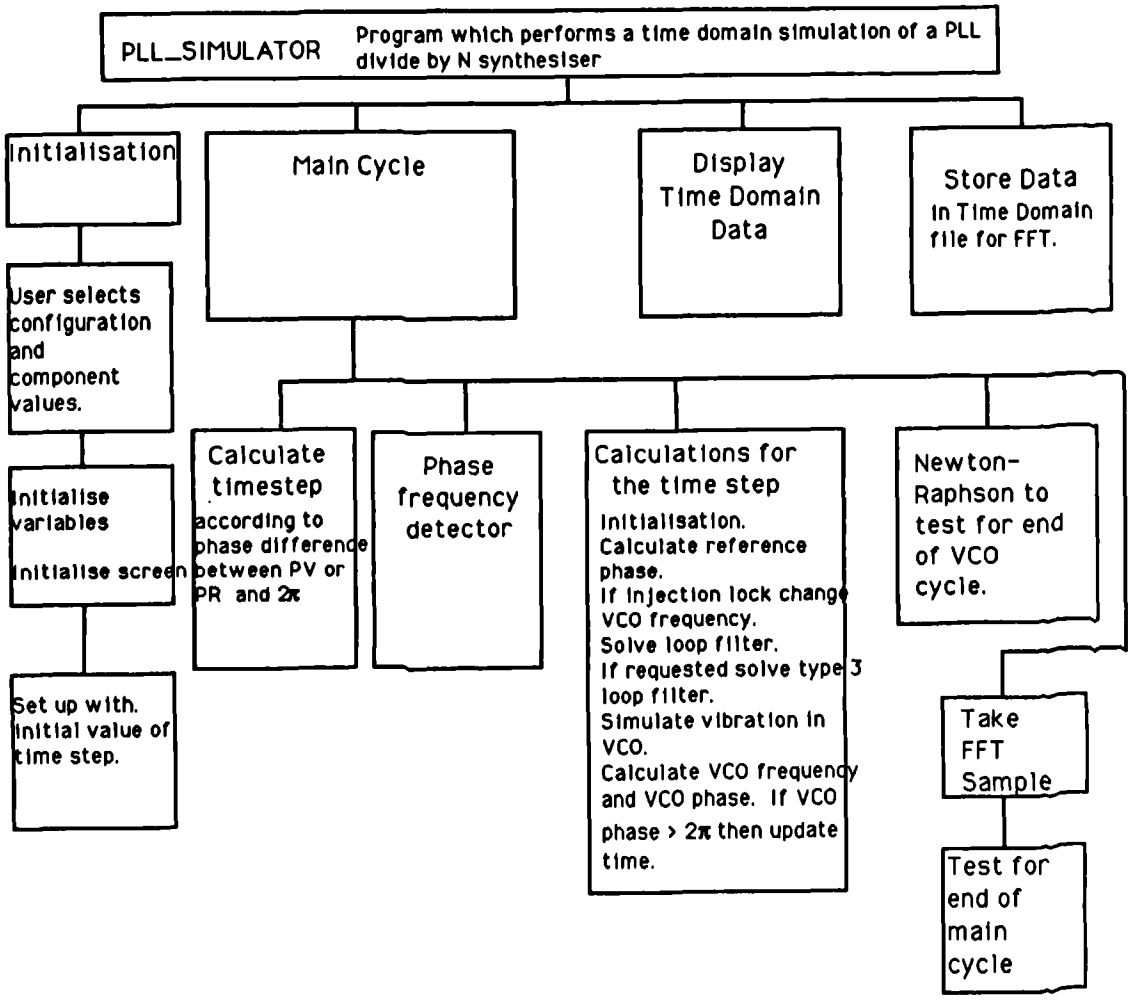
A.3.5 PLL calculation package

Fig A3.4 represents the procedure PLL_CALCULATION. The calculations pertaining to the relevant section of the loop, fig 5.25 are performed sequentially here. Pseudocode for this procedure is given in §A3.7. In common with the SRD simulation package, each time step begins with a local initialisation, however the PLL calculation package code follows this with calculation of the reference phase, and subsequent testing to determine whether the reference phase exceeds phase exceeds 2π. A user selectable option exists here to use the difference between the VCO phase and reference phase to first order phase lock the VCO in order to simulate spurious injection locking. The proportional integral loop filter calculation is performed next by package PLLOOPF (§A3.8) according to equations 5.24 to 5.26 of §5.5.5.2, giving a voltage output across C2. In most practical PLL implementations a perfect integrator is not possible, therefore a leakage current is allowed to flow from the integrator input, the leakage being proportional to the loop filter output voltage. A user defined option exists to cascade an identical loop filter after the main loop filter, so forming a type three loop as described in §5.8.2. Leading on from this is a facility to frequency modulate the VCO to simulate effects of vibration, then a pole is introduced to the VCO tuning input to simulate the finite time response from tuning input changes to changes in VCO frequency.

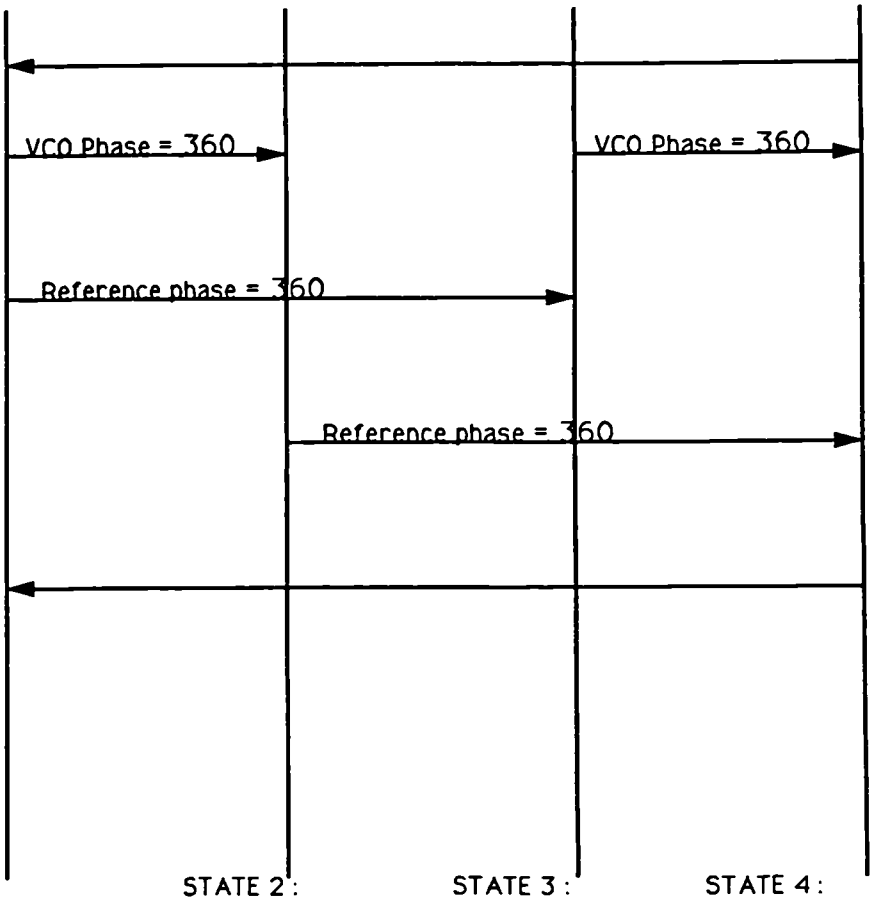
A.3.6 Outputs

VCO control voltage and VCO phase are taken as outputs to be plotted, the VCO phase is also stored in extended memory to enable FFT processing of the output. By taking an FFT, an estimation of the response of the PLL to phase noise may be obtained. An estimation of the PLL settling time may be calculated by observing the time taken for the VCO phase to reach a steady state value.

Structure Chart for PLL_Simulator Program

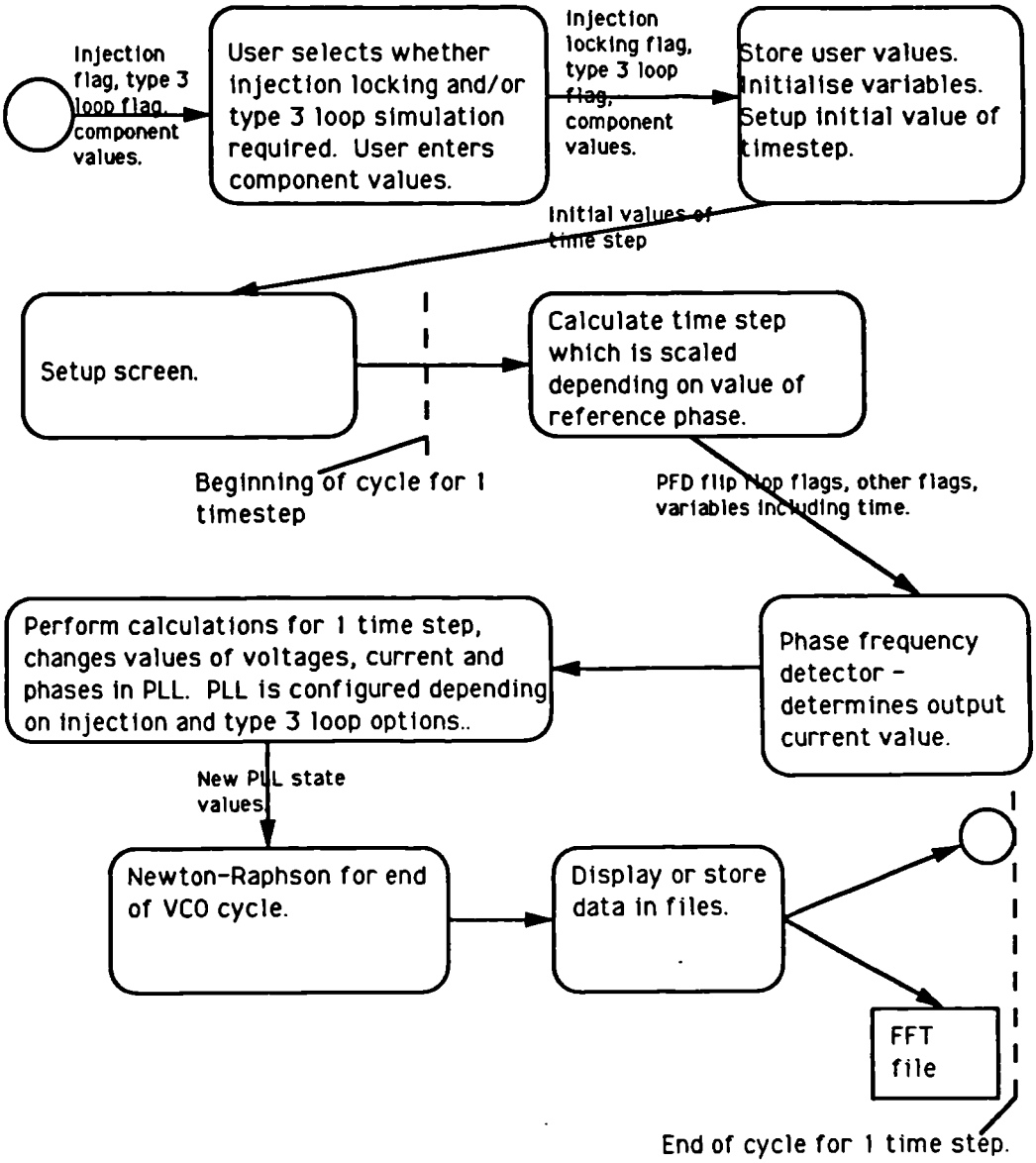


State Machine for Frequency Detector - PLL Simulation



STATE 1 :	STATE 2 :	STATE 3 :	STATE 4 :
VCO Phase FALSE	VCO Phase TRUE	VCO Phase FALSE	VCO Phase TRUE
Reference Phase FALSE	Reference Phase FALSE	Reference Phase TRUE	Reference Phase TRUE

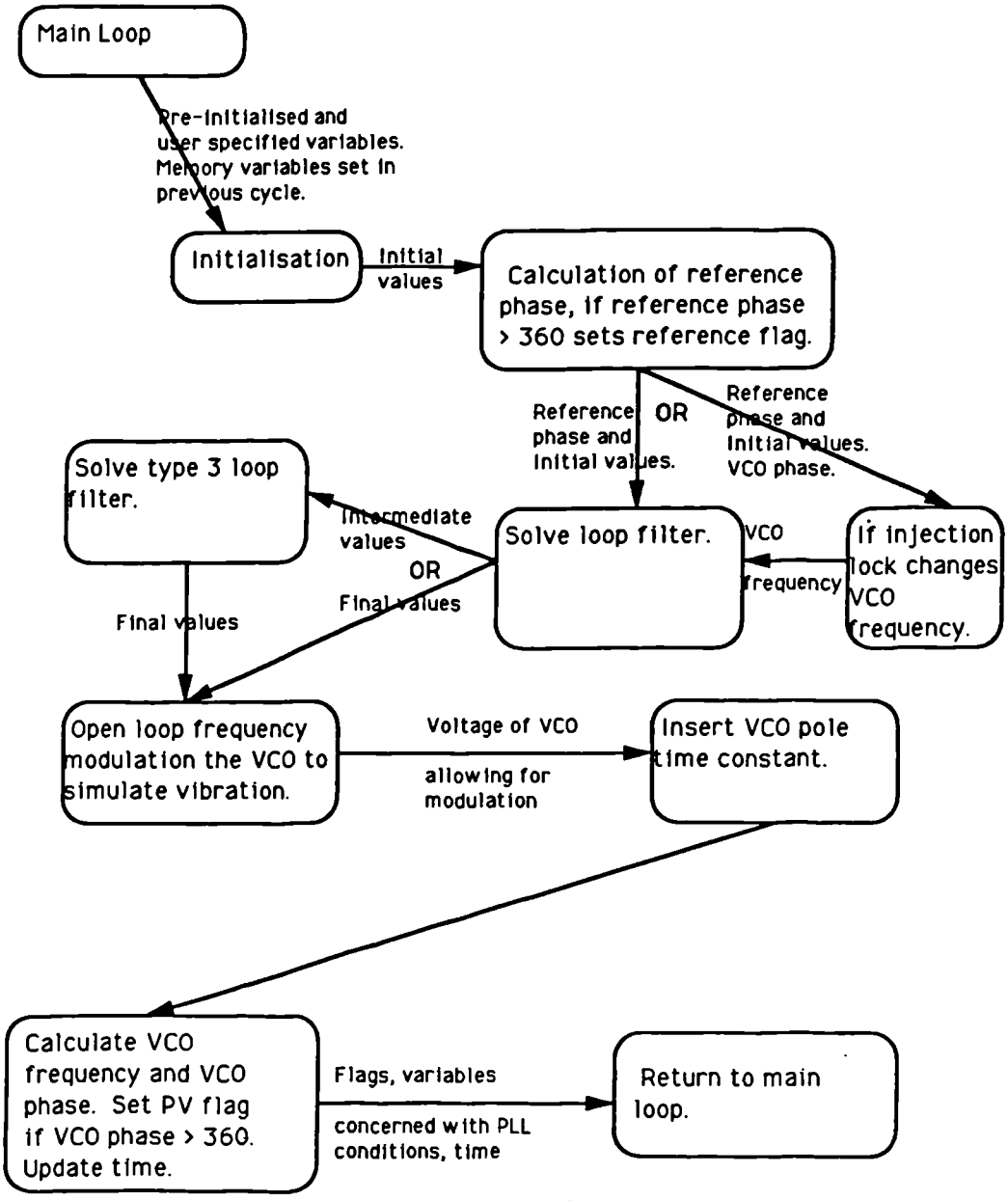
Main Loop - PLL_Simulator



Note:

The process represented in this flow diagram is one complete cycle between the points shown. During any single execution this cycle may be repeated until end conditions are met.

Calculation Details in One Time step - PLL_Simulator



```
Package body PLL_SIMULATOR

with CRT,DOS,GRAPH,printer,graphprn,plloopf,gplot,netvars,nettype,getextm;

-- Program to simulate a +N Loop PLL Synthesiser

type INDEXp is 1..256;
type COMPLTYPE is (r,j);

type COMPLEX is array[COMPLTYPE] of SINGLE;
type POINTS is 0..4095;

-- DECLARE VARIABLES USED BY MAIN PROGRAM AND PROCEDURES IN
-THIS PACKAGE.

numb            :   INTEGER;
grdriver,
grmode,
tot,
fftmax,
iteration,
errcode,
FFT_cycle_no    :   INTEGER;
fft_count,
fftsize         :   LONGINT;
a           :   COMPLEX;
t,t_window      :   EXTENDED;
DDT,
vlin,fft,tfft,
rx,gi           :   EXTENDED;
F2,
V,testdt,
inj_lock_angle  :   EXTENDED;

testp           :   EXTENDED;;
pllplot     :   DISPLAYPARAMS;
loop_vals,
loop_vals_1,
loop_vals2_1,
loop_vals2      :   LOOPNET;

delta_v,pr,pr_1,
pv,fv,
eff_varactor_volts,
ddt0,kv, Vcc,
pv_1, ix,i_,
ileak, ileak2, fdev,
fmod            :   EXTENDED;

updateflag,PRFLAG,
PVflag,prflag_1,
pvflag_1,
interpolation_flag,
inject_option,
type_3      :   BOOLEAN;

-Procedure interpolation (dv_dt,
                yn  in :            EXTENDED;
                absdelddt in out :  EXTENDED)           is

-- Newton-Raphson interpolation procedure
-- This stores time domain data in extended memory proir to performing an in place FFT
-- on the data.

-- The incoming parameter dv_dt is the time derivative

ddt_1, ddtx, delddt     :   EXTENDED;

begin
-- ddt_1 is the old value of timestep
ddt_1 := ddt;
inc(iteration);
if iteration > 20 then
    -- Here, call procedure to turn off graphics mode.
    -- Here, write to screen 'Newton Raphson convergence error'
    EXIT;
    -- Exit and give runtime error.
endif;

if (iteration > 1) and (yn < 0) then
    -- Test for negative y,step back an equal amount into the + region for y.
    ddtx := 2*yn/dv_dt;
```

```
        ddt := ddt-ddtx;
    else
        ddt := -yn/dv_dt;
        if iteration = 1 then
            ddt := ddt_1 + ddt;
        endif;
    endif;
    delddt := ddt_1 - ddt;
    absdeldt := abs(delddt);

    end interpolation;

    Procedure PLL_CALCULATION is

    -- Calculation of PLL time domain equations for each value of timestep DDT.

    -- Declare variables internal to this procedure.
    acctest,
    inj_phase_error,
    sininjerr,
    vcopulling,
    vtotal          :    EXTENDED;

    begin
    -- Variables are updated at the start of each time step here.

    if updateflag then
        -- For Regulo-Falsi interpolation, do not update start variables.

        loop_vals2_1 := loop_vals2;
        loop_vals_1 := loop_vals;
        pv_1 := pv;
        pvflag_1 := pvFlag;
        prflag_1 := prflag;
    else
        pvflag:=pvflag_1;
        prflag:=prflag_1;
        loop_vals2:=loop_vals2_1;
        loop_vals:=loop_vals_1;
    endif;

    -- Now calculate reference phase.

    PR := PR_1 + 360*FR*DDT;

    if PR > 360 then
        -- Linear interpolation applied to find exact point of phase detector triggering.
        -- Linear interpolation formula for end of reference cycle.
        ddt := ddt*(360-pr_1)/(pr-pr_1);
        prflag := TRUE;    -- PR flag indicates that 360 deg is reached
        pr:=0;
    endif;

    If inject_option then
        -- Optional injection locking block
        -- This block of code applies correction to VCO frequency relative to the phase of an
        -- injected signal at synthesiser reference frequency.

        if ((pv > 5) and (pv < 355)) then
            -- Model injection locking as a first order phase lock loop
            -- with injection locking angle relative to the true phase locking
            -- angle of inj_lock_angle, giving a frequency pulling effect on the
            -- VCO of vcopulling

            inj_phase_error   := (pllplot.p +inj_lock_angle)*2*pi/360;

            sininjerr := sin(inj_phase_error);
            VCOpulling := Inj_lock_bandwidth*sininjerr;
            f1 := f2 - vcopulling;
        endif;
    endif;
    --- Access loop filter equations are performed within the procedure Solve_loop_filter
    which
    -- is now called.
    -- Input to the loop filter is Ix and the output is Ec2
    Solve_loop_filter(rx,c1,c2,Ix,ddt,dt,loop_vals);

    -- Next, apply power supply and ground limits for VCO input.

    if loop_vals.ec2 > Vcc then
        loop_vals.ec2 := Vcc;
```

```
endif;

if loop_vals.ec2 < 0 then
    loop_vals.ec2:=0;
endif;

-- Optional type three loop filter block - if user has selected a type 3 loop filter this block
-- is executed.
If Type_3 then
-- Switch in an extra loop filter for a type3 loop (3 poles near zero Hz)
--Apply leak current to simulate an imperfect integrator
    Ileak2 := loop_vals2.ec2/R4;
    i_:= Gi*(v-Vcc/2)-Ileak2;
    Solve_loop_filter(r2,c3,c4,I_,ddt,dt,loop_vals2);
    -- power supply and ground limits for VCO input.
    if loop_vals2.ec2 > Vcc then
        loop_vals.ec2 := Vcc;
    endif;

    if loop_vals2.ec2 < 0 then
        loop_vals.ec2 := 0;
    endif;

    v := loop_vals2.ec2;

else
--Bypass second loop filter for type two loop
    v:=loop_vals.ec2;
endif;

-- Open loop frequency modulate tne VCO to simulate vibration
-- with peak deviation fdev, and frequency fmod
Vtotal := V+(fdev/kv)*SIN(2*PI*fmod*T);

-- Insert VCO pole time constant vcoconst
delta_V := Vtotal - eff_varactor_volts;
delta_V := delta_V*(1-(exp(-ddt/vcoconst)));
eff_varactor_volts := eff_varactor_volts+delta_V;

-- Calculate VCO frequency, fv.
FV:=F1+(KV*eff_varactor_volts);

-- Calculate of VCO phase
pv := pv_1+360*ddt*FV/N;        --Integration due to vco

If pv > 360 then
    interpolation_flag:=TRUE;
    updateflag:=FALSE;
else
    updateflag:=TRUE;
    pr_1:=pr;
    t := t+ddt;
endif;
end  pll_calculation;

-----------------------------------------------------------------------------------------
-- BEGINNING OF MAIN PROGRAM
-----------------------------------------------------------------------------------------
PROGRAM PLLDOC is

-- This program performs a time domain simulation of a phase locked loop.

begin

-- Initialise variables

-- Not shown here but in source, we initialise fields in pllplot record (concerned with
-- plotting) to zero.

-- Not shown here but  in source, we initialise all of the fields in the loop_vals record,
-- which represent loop filter voltages and currents, to zero.

-- Initialise flags
interpolation_flag := FALSE;
updateflag := TRUE;
pvflag := FALSE;
prflag := FALSE;

-- Initialise reference and VCO phases and output of phase detector current to zero.
-- Set initial value of timestep.
pr:=0;
pv:=0;
```

```
pr_1:=0;
pv_1:=0;
Ix:=0;

-- Ask user to verify or change constant values during processing.
User_chk_params;

-- gi is gain block between loop filters
gi := 1/rx;
r2 := rx;

-- Inj_lock_angle is the phase of the injection lock
-- relative to the phase locking phase

Inj_lock_angle := 180;

t_window := 1e-20;
FFT_cycle_no := 2;
iteration := 0;
t := 0;
fft_count := 0;
M := 20;
pllplot.TMAX := M/FR;
pllplot.tmin := (m-20)/fr;
tfft := 10/fr;
fft := FFT_cycle_no/(fr*fftsize);   -- FFT Increment in time

-- Not shown here, but in source we set up the graphics mode for vdu display.

-- Now begin main loop for duration of time which user has selected.

while  t <= pllplot.tmax loop
    ddt := dt;

    -- Timestep control according to distance from the reference clock
    if (pr  > 350) then
        ddt := dt*(0.001+0.0999*abs(360-pr));
    endif;

    if pr < 10 then
        ddt := dt*(0.001+((abs(pr))*0.0999));
    endif;

    -- Now begin Phase-Frequency comparator

    -- ileak is imperfect integrator leakage
    Ileak := loop_vals.ec2/R3;

    If ((pvflag) and (prflag)) then
        pvflag := FALSE;
        prflag := FALSE;
        ix := Ileak;
    endif;

--Phase detector output is proportionally switched current Ix - now assign a value to this
-- depending on flag state.

    If ((NOT pvflag) and (prflag)) then
        Ix:=ip;
    endif;

    If ((pvflag) and (NOT prflag)) then
        Ix := -ip;
    endif;

    -- Call procedure to form main PLL simulation calculation over one timestep.
    pll_calculation;

    -- Now perform interpolation to find exact point at which pv = 360 degrees
    If ((interpolation_flag) and (t > 1e-8)) then
        loop
            --Time derivative of the VCO phase is its frequency
            interpolation(-Fv*360/N,360-pv,testdt);
            pll_calculation;
            if ddt < t_window then
                testdt := 0;
            endif;
            exit when (testdt < t_window)
        end  loop;

        -- Finished interpolating, therefore pv is 360 degrees, therefore set pvflag true.
```

```
        pvflag:=TRUE;
        pv:=0;
    endif;

    interpolation_flag := FALSE;
    updateflag := TRUE;
    iteration := 0;
    pllplot.volts := V;
    pllplot.phase := (pv-pr)*N;
    pllplot.time := t;

    If t > tfft then

        -- Take FFT sample.
        -- Linear interpolation between calculation points to give vlin

        pllplot.vlin:=pllplot.volts_1+(pllplot.phase-volts_1)*(tfft-time_1)/(t-
time_1);
        a[r] := vlin/(10*pllplot.vmax);
        a[j] := 0;
        store_extended_mem(fft_count,8,a);
        fft_count := fft_count+1;
        tfft:=tfft+fft;              --increment for fftpoint
    endif;

    If t < pllplot.tmax
        If NOT PVflag and prflag then
            -- Assigning values in display parameters record to valuse to be plotted
            pllplot.phase := pv-pr-360 ;
        endif;

        If ((pvflag = TRUE) and (prflag = FALSE)) then
            pllplot.phase := pv-pr+360 ;
        endif;

    -- Plot VCO phase and VCO control voltage against time.

    DISPLAY(pllplot);
    endif;
```



```
    -- In source but not shown here, we save previous plot points so that line can be
    -- drawn.
end loop;        -- End of main loop.

while NOT keypressed loop;
end loop;

-- In source code but not shown here, we send graph to printer and then turn off graphics
-- mode.
end plldoc;
```

A.3.8 Pseudocode for PLL loop filter section

```
Package plloopf is

--This package contains global type and variable declarations used in the main program
-- which accesses this package. Also within this package is code providing user interface
-- whereby component values can be selected by the user before the main processing
-- is implemented.

with TRISOLVE, NETTYPE, NETVARS;

type loopnet is
    record
        ec1,
        ec2,
        i,
        i1        EXTENDED;
    end record;

Procedure solve_loop_filter(R      :in:          EXTENDED;
                            C1     :in:          EXTENDED;
                            C2     :in:          EXTENDED;
                            Ix     :in:          EXTENDED;
                            ddt    :in:          EXTENDED;
                            dt     :in:          EXTENDED;
                            loopf  :in out:      LOOPNET)      is

    -- Coding of equations 5.24 to 5.26 of Section 5.5.5.1 to solve the loop filter in the
```

```
    -- time domain. The solutions of these are returned to the calling procedure, which
    -- is pll_sim.

end solve_loop_filter;
```

A.3.9 Pseudocode for the PLL user interface

```
Package pll_usr_in is

--This package contains global type and variable declarations used in the main program
-- which accesses this package. Also within this package is code providing user interface
-- whereby component values can be selected by the user before the main processing
-- is implemented.

with CRT, NETTYPE, NETVARS;

-- The variables declared below can be checked and modified by the user at runtime
-- before the main processing is implemented.

        FR,                     Phase comparison frequency

        Vcc,                    Positive supply voltage

        C1,                     Loop filter capacitor

        C2,                     Loop filter cap

        Rx,                     Loop filter resistor

        F1,             VCO frequency at zero tuning voltage

        KV,                     VCO Gain (Varactor tuning sensitivity)

        vcoconst,               Vco time constant

        IP,             Charge pump integrator current

        Inj_lock_bandwidth,     Injection locking bandwidth

        fdev,                   Peak deviation of oscillator modulation
frequency
                                due to vibration

        fmod    :       EXTENDED;  Modulation frequency due to vibration

        N,                         Division ratio of divider in PLL

        M       :       INTEGER;   Number of cycles of time domain
                                   simulation

        fftsize,                   FFT file size

        fftmax,         LONGINT;   Maximum point of FFT plot (FFTsize plus
                                   time to allow starting transients
to decay)


Procedure Usr_chk_params is

begin

-- Procedure enables user to read component values to be used by
-- the program,and change them if required. The variables are read
--  from the file pllusr_prms.dat and written back after updating.
-- They will not need to be read again by the main program because
-- they will have been assigned to the above memory variables which
-- the main program can access.
end Usr_chk_params;


end package Usr_in.
```

A.4 DDS simulation

A.4.1 Program overview

DDS_SIMULATOR is a program which simulates a direct digital synthesiser (DDS). This program produces a time domain file in extended memory which can then be used as an input to a FFT. The program is designed to simulate the use of non-ideal DACs.

Code for the simulation is organised into a main program which performs the simulation, with subsidiary packages for DAC simulation, EPROM look up table calculation, and storage in extended memory. A structure chart for the DDS simulation program is given as figA4.1.

The bulk of code in the main program is held in a loop which is repeated once every clock cycle. Because this is a clocked digital system no interpolation between the discrete increments in time is required. On commencement of the main program and before the loop is entered, the EPROM look up table is built, and the tables holding DAC switching current characteristics (in record DACDYNAMIC) are calculated in order to reduce the computational load within the main loop. A data flow diagram showing the main loop is displayed as figA4.2 and closely resembles the DDS architecture of fig4.18. The main loop exactly follows the logical structure defined by decorrelation method 2 in §8.4.4 and incorporates phase and amplitude truncation dithers as described in §8.5.3 and §8.5.4. These spurious signal reduction mechanisms can be disabled or enabled by altering flags in the code.

The analogue values produced by the simulation are stored in a time domain file in extended memory in preparation for a FFT.

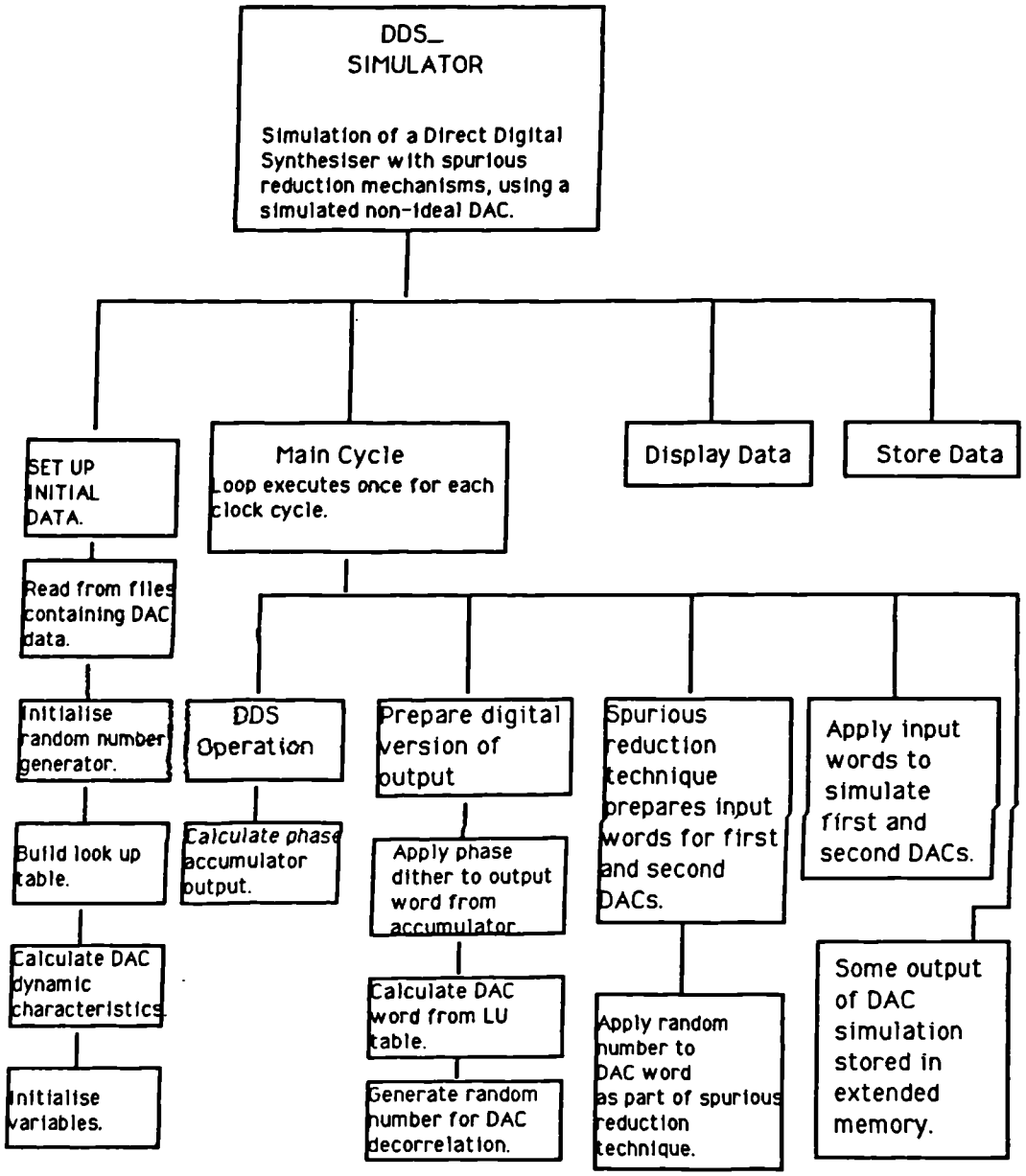
A.4.2 DAC simulation

For the DAC simulation, files are created by a program which simulates a production run, of which a description only is given here. This program generates a random spread in the DAC characteristics between the tolerance limits specified in §8.9.6.2. For each DAC in the simulated production run a record holding the characteristics is stored in a hard disk data file (with extension .DAT). Before commencement of a DDS simulation, two DAC characteristic files are selected from the simulated production run. The characteristics stored are static current levels corresponding to each bit, and spreads in the time constants and switching propagation delays for all bits.

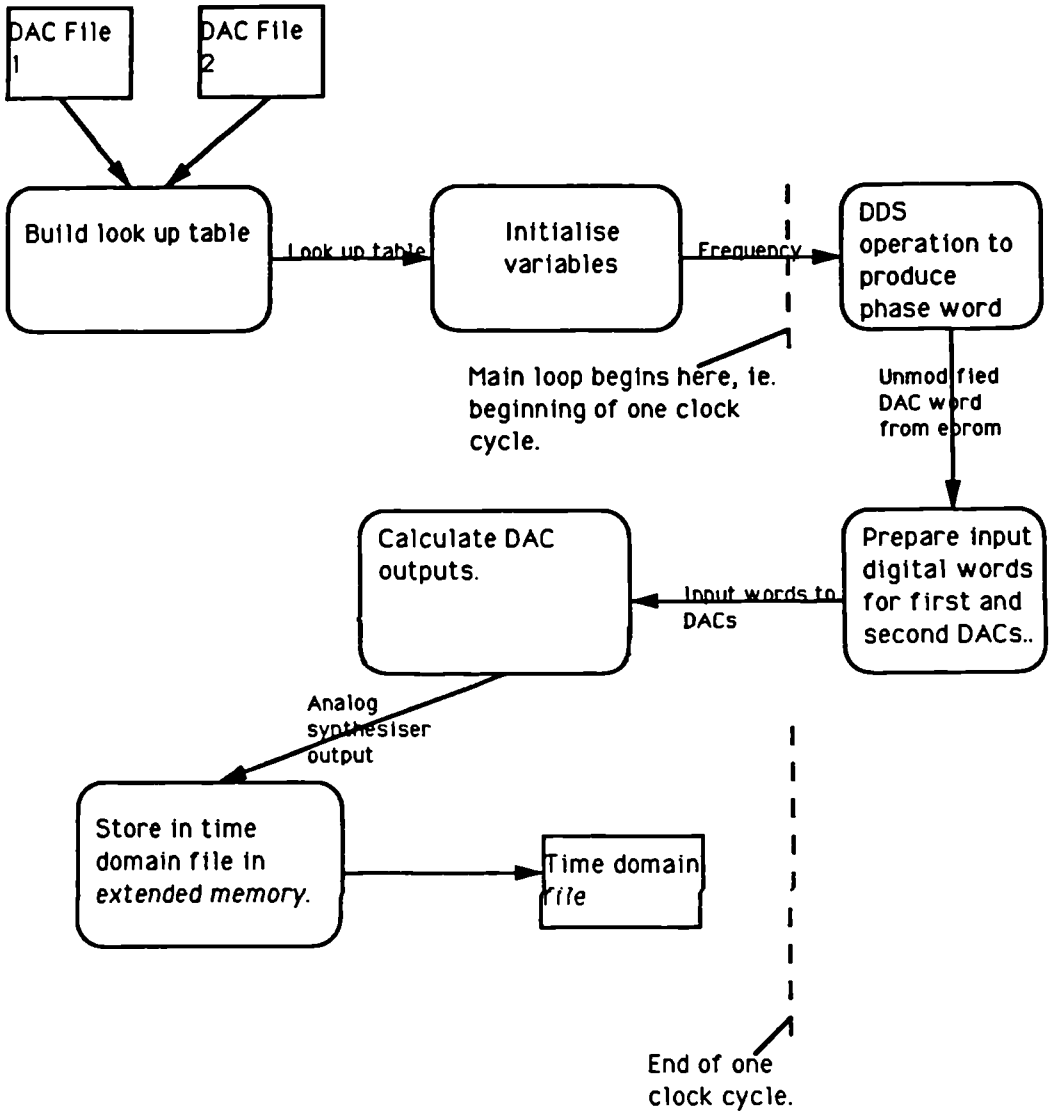
Immediately prior to simulation, the DAC files are read into a record which is subsequently used to create the DAC simulation. When the main program commences, the first task is to calculate errors due to switching transients on each bit as given by equation 8.63. Two arrays are generated in this process: one corresponding to each bit switching from off to on, and the other corresponding to switching from on to off. These arrays are stored in a record of switching characteristics (DACDYNAMIC as mentioned earlier).

During the course of the main loop, the actual analogue output is calculated from the static and dynamic DAC characteristics so far determined. As discussed in §8.9.6.2, each bit of the DAC word is compared with the corresponding bit of the appropriate previous clock cycle DAC word and if there is a change, the contribution from the switching characteristics record (DACDYNAMIC) is summed in. Further adjustment to the output is necessary to account for digital signal edges capacitative coupling through the current switches in the DAC; this coupling is calculated according to equation 8.65. This leads to the requirement for calculation of a further contribution (DIG_FEEDTHROUGH in pseudocode), which is added to the DAC current along with the switching current error as described above. The calculated DAC currents and errors for all the bits are then summed according to equation 8.64 to form the DAC analogue output.

Structure Chart for DDS_Simulator Program



Main Loop - DDS_Simulator



Note:

The process represented in this flow diagram is one complete cycle between the points shown. During any single execution this cycle may be repeated until end conditions are met.

A.4.3 Pseudocode for DDS simulation

Package DDS is

```
    -- Package contains main program and procedures to simulate a direct digital
    --synthesiser with various spurious reduction mechanisms introduced, a simulated non
    -- ideal DAC is used.

with ffttypes,CRT,DOS,GRAPH,printer,exfftvar,getextm;
type ACREC is
    record
        loww,
        highw       :   WORD;
    end record;

type    DAC is array [0..7] of EXTENDED;
type POINTS is 0..4095;
type PROM is array[POINTS] of BYTE;
type EQUALISETYPE is (amplitude,phase,both);
type DOMAIN is (time,freq);

type    DACDYNAMIC is
    record
        ion,
        ioff        :   DAC;
    end;

    type DACCHARS is
        record
        tponf,
        tpofff,
        tauf,
        idac        :   DAC;
        Clh,
        Chl         :   EXTENDED;
    end record;
```

```
-- Now declare variables common to main program and procedures in this package.
time_file       :   FILE ;
counte,
phaseword   :   WORD;
promval         :   PROM;

dither,
dacword,
dac2word,
t_1,
T2_1,
randmsb,
randno,
overflow,
dac1_msb,
dac2_msb        :   BYTE;

numb            :   INTEGER;
accout,
Cache_addr,
tot,
fftsize,
fftmax,
accumulator,
frequency,
accumask        :   LONGINT;
aluword,
alu,
cacheseg        :   INTEGER;
T,
Vmax            :   EXTENDED;
v               :   SINGLE;
iout,
i2out,
Fr,
f1,
DT          :   EXTENDED;
freqcy,
ditherval,
isum,
Vstep           :   EXTENDED;
```

```
    Decorrelation,
    Dither_option,
    FFT_sampling    :   BOOLEAN;
    dac_file        :   FILE of DACCHARS;
    dac_clocked_1,
    dac_clocked_2   :   DACDYNAMIC;
    dac_vals,
    dac_vals2       :   DACCHARS;


Procedure eprom (costable    :out:    prom)  is
-- This procedure builds the EPROM cosine look up table with 12 bit phase input
-- and 8bit word to the DAC at the output.
-- Declare variables local to this procedure.
    byt         :   BYTE;
    addressline :   WORD;
    yyt         :   EXTENDED;
begin
for addressline in 0  4095 loop
    yyt := 0.5 + 254*(0.5+0.5*cos(addressline*2*pi/4096));
    byt := trunc(yyt) + 1;
    costable[addressline] := byt;
end  loop;
end  eprom;


Procedure dynamic_array is

-- This procedure calculates DAC dynamic errors from data stored in files of type
-- DAC_FILE2 in records of type DAC_VALS.

-- Declare variables.
time_on,
time_off,
tau     :   EXTENDED;
dacarrref   :   BYTE;

begin
for  dacarrref in 0..7 loop

    -- Retrieve DAC switch propagation delays - time_on and time_off from file.
    time_on := dac_vals.tponf[dacarrref];
    time_off := dac_vals.tpofff[dacarrref];

    -- Assign  DAC switch transient time constant - tau.
    tau := dac_vals.tauf[dacarrref];

    -- The following 2 statements allow for errors in the switching.
    dac_clocked_1.Ion[dacarrref] := dac_vals.idac[dacarrref]*
                                        (dt-time_on-tau)/dt;
    dac_clocked_1.ioff[dacarrref] := dac_vals.idac[dacarrref]*
                                        (Time_off+tau)/dt;
end  loop;
end dynamic_array;


Procedure dynamic_array2 is

-- This procedure calculates DAC dynamic errors from data stored in files of type
-- DAC_FILE in records of type DAC_VALS.

-- Declare variables.
time_on,
time_off,
tau     :   EXTENDED;

dacarrref   :   BYTE;

begin
for dacarrref in 0..7 loop

    -- Retrieve DAC switch propagation delays - time_on and time_off from file.
    time_on := dac_vals.tponf[dacarrref];
    time_off := dac_vals.tpofff[dacarrref];

    -- Assign  DAC switch transient time constant - tau.
    tau := dac_vals.tauf[dacarrref];

    -- The following 2 statements allow for errors in the switching.
    dac_clocked_2.Ion[dacarrref] := dac_vals2.idac[dacarrref]*
```

```
                                                    (dt-time_on-tau)/dt;
    dac_clocked_2.ioff[dacarrref] := dac_vals2.idac[dacarrref]*
                                                    (Time_off+tau)/dt;
end  loop;
end dynamic_array2;



Procedure dac_dynamic(idacsum    :out:   EXTENDED) is

-- Procedure to simulate a clocked DAC

-- Declare variables.
shiftbit,
testbit,
testbit_1                :    BYTE;
dig_feedthrough1,
dig_feedthrough0     :    EXTENDED;

one                          : constant      BYTE := 1;

begin
dig_feedthrough1 := Vstep*dac_vals.Clh/dt;
dig_feedthrough0 := Vstep*dac_vals.Chl/dt;

-- dig_feedthrough represents digital edges coupling through to the
-- analogue output by either mutual coupling or spikes in the
-- switching circuitry.

-- Compares the Present Dacword with the previous value of Dacword to find
-- which bits are changed.  If a bit changes, the simulation couples a
-- contribution from that corresponding digital step to the analogue output.

idacsum := 0;
for shiftbit in 0..7 loop

    testbit := dacword shr shiftbit;
    testbit := testbit and one;

    -- t_1 is the value of dacword on the previous clock cycle.
    testbit_1 := t_1 shr shiftbit;

    testbit_1 := testbit_1 and one;

    if testbit_1 = testbit then
        if testbit>0 then
            -- Add in contribution of static DAC current from individual bit.
            idacsum := idacsum+ dac_vals.Idac[shiftbit];
        endif;
    else
        if testbit = 1 then
            -- Transition from zero to one, allow switch on transient in current
            idacsum:=idacsum+  dac_clocked_1.Ion[shiftbit]
                        -dig_feedthrough1;
        else
            -- Transition from one to zero, allow switch off transient in current.
            idacsum := idacsum+ dac_clocked_1.Ioff[shiftbit]
                        +dig_feedthrough0;
        endif;
    endif;
end  loop;

-- Now store calculated value of dacword for next clock cycle.
t_1:=dacword;

end dac_dynamic;



Procedure dac_dynamic2(idacsum   :out:    EXTENDED);

-- Procedure to simulate a clocked DAC.

-- Declare variables.
shiftbit,
testbit,
testbit_1     :    BYTE;
dig_feedthrough1,
dig_feedthrough0       :    EXTENDED;
```

```
one                         : constant      BYTE := 1;

begin
dig_feedthrough1 := Vstep*dac_vals.Clh/dt;
dig_feedthrough0 := Vstep*dac_vals.Chl/dt;

-- dig_feedthrough represents digital edges coupling through to the
-- analogue output by either mutual coupling or spikes in the
-- switching circuitry.

-- Compares the Present Dacword with the previous value of Dacword to find
-- which bits are changed. If a bit changes, the simulation couples a
-- contribution from that corresponding digital step to the analogue output.

idacsum := 0;
for shiftbit in 0..7 loop
    testbit := dacword shr shiftbit;
    testbit := testbit and one;

    -- t2_1 is the value of dacword on the previous clock cycle.
    testbit_1 := t2_1 shr shiftbit;
    testbit_1 := testbit_1 and one;

    if testbit_1 = testbit then
        if testbit>0 then
            -- Add in contribution of static DAC current from individual bit.
            idacsum := idacsum+ dac_vals2.Idac[shiftbit];
        endif;
    else
        if testbit = 1 then
            -- Transition from zero to one, allow for switch on transient in current
            idacsum:=idacsum+  dac_clocked_2.Ion[shiftbit]
            -dig_feedthrough1;
        else
            -- Transition from one to zero, allow for switch off transient in current.
            idacsum := idacsum+  dac_clocked_2.Ioff[shiftbit]
            +dig_feedthrough0;
        endif;
    endif;
end  loop;
```



```
-- Now store calculated value of dacword for next clock cycle.
t2_1:=dac2word;          -- stores previous value of dacword

end dac_dynamic2;
```

BEGINNING OF MAIN PROGRAM

```
PROGRAM DDS_SIMULATOR is

-- Beginning of main program.

begin
-- DACVALS.DAT and DACVALS2.DAT are files of randomly selected DAC
-- characteristics from a simulated production run. There are 2 separate files because
-- the characteristics are slightly different in each.

-- In the source, we begin by reading the record dac_vals  from disk based DAC file
-- DACVALS.DAT
-- read(dac_file,dac_vals);

-- Now we read record dac_vals2 from DACVALS2.DAT
read(dac_file,dac_vals2);

-- The records dac_vals and dacvals2 now contain coefficients for dac simulation.

-- Now call Pascal function which initialises a random number generator.
Randomize;

-- Now call procedure to build look up table.
eprom(promval);

-- Initialise variables
accumulator:=32640;
V:=0;
DT:=1/Fr;
F1:=15E6;
T_1:=0;
```

```
T2_1:=0;

--Assign a value of FFT size to the variable fftsize.
fftsize:=262144;

-- Initialise segment address.
cacheseg:=0;

-- Calculate reference frequency from clock period.
FR:=1/dt;

--Define logic swing voltage, 0.9 for ECL
Vstep:=0.9
FFT_sampling:=FALSE;

-- Selection of spurious signal reduction processing
Decorrelation:=TRUE;
Dither_option:=TRUE;

-- Mask off higher bits of ALU word to make 16 bits
alu := $00ff;
accumask := $0000ffff;

-- f1 is the output frequency of the synthesiser
freqcy := f1*(fftsize-1)/fr;
frequency := round(freqcy);
t:=0;
Vmax:=2;

-- Make fftmax large enough to allow starting transients to disappear.
fftmax := fftsize+500;

-- Now begin main loop which executes once for each clock cycle.

for tot in 1..fftmax loop

    -- T is simulated time, DT is time for one clock period.
    T := T+DT;

    -- DDS operation
    accumulator := accumulator+frequency;

-- 16 bit wrap around when accumulator overflows
accumulator := accumulator and accumask;

-- Select random number for dither
if dither_option then
    -- random is a Pascal function which selects a random number
    dither := random(256)
else
    dither := 0;
end if;

-- Phaseword is output of accumulator.
phaseword := acrec(accumulator).loww;

-- Now calculate output of accumulator with added dither
phaseword := phaseword+dither;

-- Use upper 12 bits of phaseword (Eprom LU table has 12 bit resolution)
phaseword := phaseword shr 4;

-- dacword is DAC word output from EPROM
dacword := promval[phaseword];

-- Generate further random number for DAC decorrelation
if decorrelation then
    randno := random(256)
else
    randno := 0;
end if;

-- Examine msb of random number.
randmsb := randno and 128;

-- Mask out msb. In the hardware the MSB is separated here from the other 7 bits
-- randno represents these 7 bits, randmsb represents the MSB.
randno := randno and 127;

-- DAC DECORRELATION ALU SECTION

-- Apply randno and dacword to ALU, add or subtract depending upon MSB of
```

```
-- random number.
aluword := alu;
if randmsb>0 then
     aluword := randno + dacword;
else
     aluword := dacword - randno;
end if;

-- Rounding (amplitude) dither is selected up or down randomly.
ditherval := random(2);

if ((ditherval>=1) and (randmsb=0)) then
     aluword := aluword-1;
end if;

-- look at the high order byte for overflow, which is type byte
overflow := hi(aluword);

-- FIRST DAC MSB PROCESSING BEGINS HERE.
-- aluword can now go to first DAC
dacword := lo(aluword);

-- If no overflow no DAC MSB forcing.
if (overflow>0) then
     if ( randmsb>0) then
          -- Force DAC MSB to 1
          dacword := dacword or 128
     else
          -- Force DAC MSB to 0
          dacword := dacword and 127;
     end if;
end if;

-- FINISHED PROCESSING FOR FIRST DAC, SO BEGIN PROCESSING FOR
-- SECOND DAC.

if randmsb > 0 then
     -- If dither >= 1 then 2s compliment on add,otherwise 1s compliment.
     randno := not randno;
     randno := randno and 127;
     if ditherval >= 1 then
          inc(randno);
     end if;
end if;
dac2word := randno;
-- 7 lsbs of randno now ready for input to second DAC
-- Now prepare MSB of input to second DAC.
-- Raise MSB of DAC
if (((randmsb=0) and (overflow=0)) or (( randmsb>0) and(overflow>0))) then
     dac2word := dac2word or 128;
end if;

-- Second DAC word now prepared.

-- Summation of DAC outputs
dac_dynamic(iout);
dac_dynamic2(i2out);
isum := iout+i2out-1;

-- Video DACs operate into 75 Ohm load
v := isum/75;

if not FFT_sampling then
     -- By the time fft sampling begins the program has been through
     -- 500 clock cycles.
     Cache_addr := tot-500;
     if Cache_addr>0 then
          FFT_sampling := TRUE;
          TD_Value[Cache_addr,r] :=  v/(10*vmax);
          TD_value[Cache_addr,j] := 0;
          Cache_addr := 2;
     end if;
else
     -- Time domain file is cached in 2K portions and then stored in extended
     -- memory.
     TD_value[Cache_addr,r] :=  v/(10*vmax);
     TD_value[Cache_addr,j] = 0;
     Cache_addr := Cache_addr+1;
     if Cache_addr>2048 then
          store_extended_mem (cacheseg,11,TD_value); --11 log tob 2 value
ofcachesize
          Cache_addr := 1;
```

```
            cacheseg := cacheseg+2048;
        end if;
    end if;

end loop;

-- In source hardcopy produced here.
while not keypressed
end loop;

-- In source turn off graphics mode.
end DDS_Simulator;
```

A.4.4 Pseudocode for DDS types declaration package

```
Package ffttypes is

-- This package contains type declarations for variables which are used
-- in the fftvars package, and in the FFT and DDS simulation software.

-- Declare type to hold complex number, COMPLTYPE
type COMPLTYPE is (r,j);

type COMPLEX is array[COMPLTYPE] of SINGLE;
type COMPLEXDOUB is array[COMPLTYPE] of DOUBLE;
type POINTS is 1..2048;
type COMPLXARR is array[POINTS] of COMPLEX;
type DOMAIN is (time,freq);

end ffttype;
```

A.4.5 Pseudocode for DDS vars declaration package

```
Package exfftvar is

-- This package holds global variable declarations which are used by DDS and
-- FFT simulation software.

with ffttypes;

first           :   BOOLEAN;
error,
tapn,
cntreg,
tapp,
samples,
imon,
mmon            :   INTEGER;
fftsize,
accno,
efef            :   LONGINT;

time_file       :   FILE ;
aa,
bb          :   COMPLXARR;
a           :   COMPLEX;
counte          :   WORD;
end extfftvar;
```

A5 Phase noise analysis program

A5.1 Introduction to phase noise analysis program

This appendix gives details of the link budget degradation program which analyses the effect of local oscillators on satellite communications systems. Most of the functional details have been covered in §9.7, therefore only a brief description will be given here, together with the pseudocode and data flow diagrams.

A5.2 Main program

A structure chart relating to this program is given as fig9.15 in §9.7. The main program is concerned principally with plotting the graph of degradation against data rate on a logarithmic axis. The data flow within the main process is shown in fig A5.1. There is a facility in the main program for permanent storage of the plotted data to enable rapid re-creation of the plots at a later date. Pseudocode for the main program is given in §A5.7.

On commencement of execution of the main program the user is first requested to enter whether the plot will be calculated or simply read from a previously stored file. If calculation is chosen, the user is further prompted for a choice of static phase offset and modulation type. If the replot option is chosen, the stored plot file is read from the permanent storage media into memory. On completion of this step, the computer display is setup and then plotting of data commences. Finally, if the calculation option is chosen, the plot files are stored to permanent storage media then whatever the selected option, a hardcopy of the plot is produced if requested.

A5.3 Main loop

The main loop is executed within the main program after initial setup of data as can be from figs A5.1 and A5.2. The function of the main loop is to provide a logarithmic increment in the value of data rate which is plotted against degradation for a given value of carrier recovery loop bandwidth. Seven such values are acquired by executing the loop seven times. Before commencement of these seven loop cycles, one dummy run of the loop is performed which establishes the horizontal logarithmic graticule. To obtain a value of degradation the MAIN_CALCULATION code is executed. If the conditions for a particular data rate are such that no meaningful value of sensitivity degradation can be obtained, calculations are aborted and no points plotted for that value of data rate.

A5.4 Main calculations

The main calculations produce a value of sensitivity degradation from the present value of data rate and selected modulation type. A data flow diagram for the main calculations code is given as fig A5.3. Firstly the link data rate is established as a function of the input / output data rate and modulation type, the latter is user selected and may be coded or uncoded. The software proceeds to calculate a value of carrier recovery (CRL) filter bandwitdh as a function of link data rate. The integration calculations for each local oscillator are then performed with the effect of obtaining a phase jitter value for each local oscillator as described in §6.4.2, these values being assigned to a data structure for later use. If, during these integration calculations an excessive value of jitter is produced, the calculations are aborted and no points plotted. Finally, the degradation is calculated from the value of phase jitter produced by the integrations. Pseudocode for the MAIN_CALCULATION procedure which contains code for the main calculation is given in §A5.7.

A5.5 Local oscillator calculations

Dedicated packages perform integration for each local oscillator. The data flow, which is common to all these packages, is given in fig A5.4 and a description of the two types of local oscillator integration given in §9.7.2.7 and §9.7.2.8. Each time a local oscillator package is invoked, the relevant phase noise data is read from the phase noise data base on the permanent storage media. Pseudocode for the local oscillator integration packages is given in §A5.9 and §A5.10.

A5.6 Degradation calculations

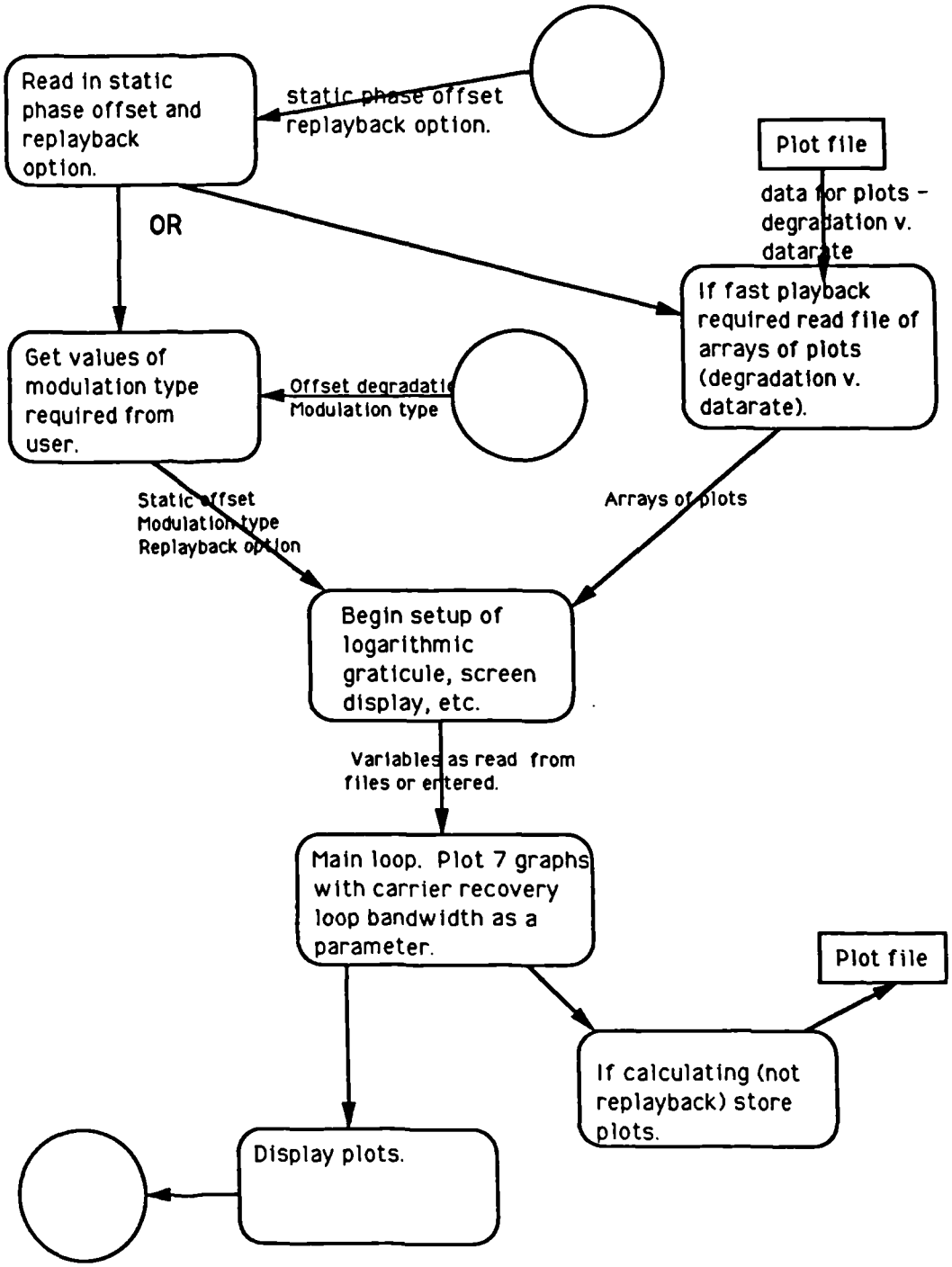
The package BERCALC performs calculation of the sensitivity degradation resulting from the calculated values of phase jitter and the user selected value of bit error rate (BER). The data flow diagram for this package is given as fig A5.5. This package performs iterative calculations of E_b/n_o corresponding to the user selected BER value, in both the presence and absence of LO phase noise in the manner described in §9.7.2.3 and §9.7.3. Integration of the probability distribution of the recovered carrier phase values is performed numerically by Simpson's rule. For each iteration of E_b/n_o in the presence of phase noise, the thermal noise calculation package is executed in order to obtain a value of thermal phase jitter on the recovered carrier. This code is described in §9.7.2.4. If, at any point the recovered carrier phase jitter is excessive, the calculation is aborted, and execution returns to the main unit. BERCALC also contains code for the following mathematical functions:-

Marcum Q function Q(x)

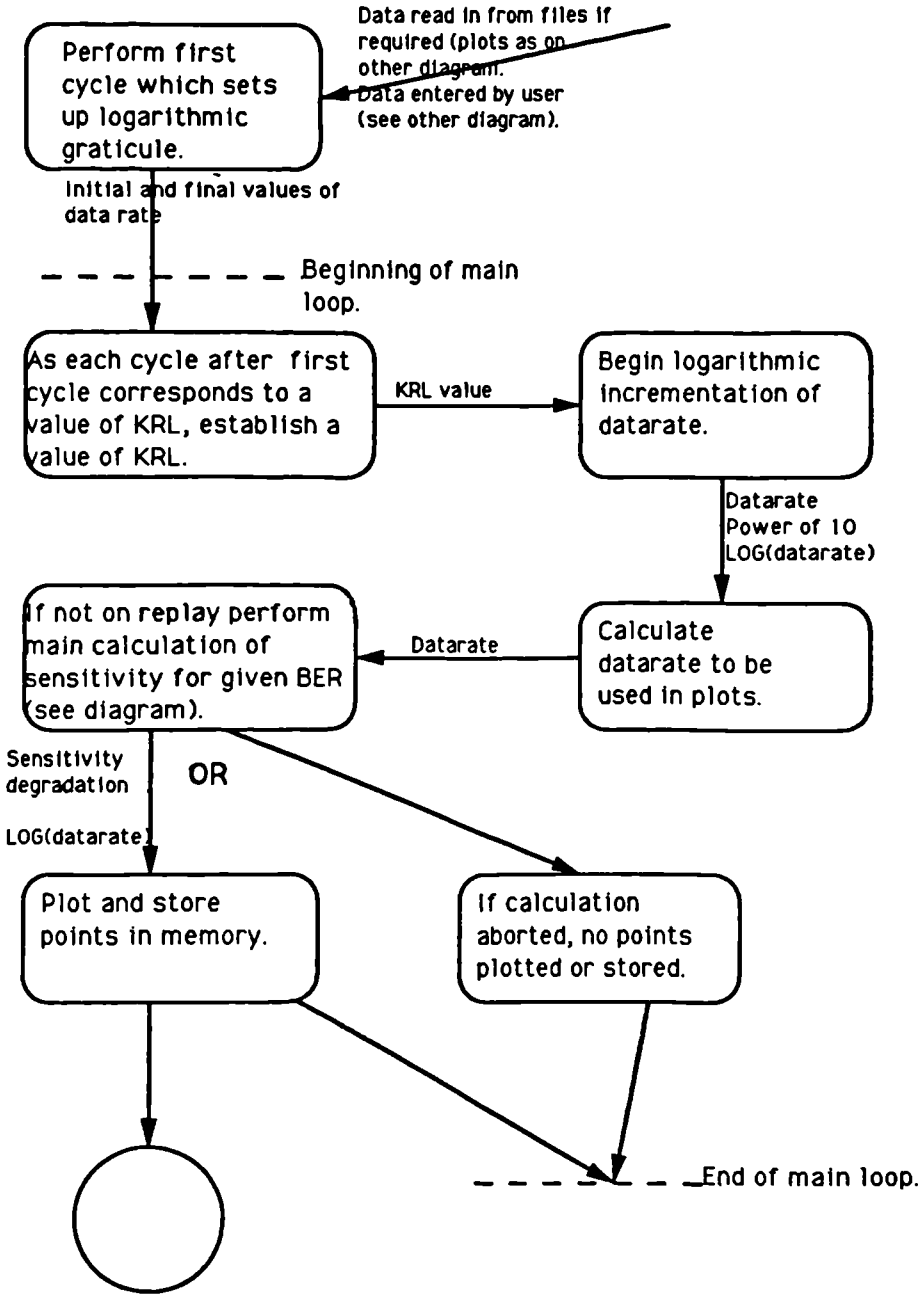
Modified bessel functiuon	Io(x)
Complementary error function	erfc(x)
Tikhonov distribution function	Tk(x)
Viterbi curve fit polynomial	Vitpoly(x)
Simpson's rule integration	

Pseudocode for the BERCALC package and the thermal jitter calculation THERMALJ is given as §A5.8 and §A5.11 respectively.

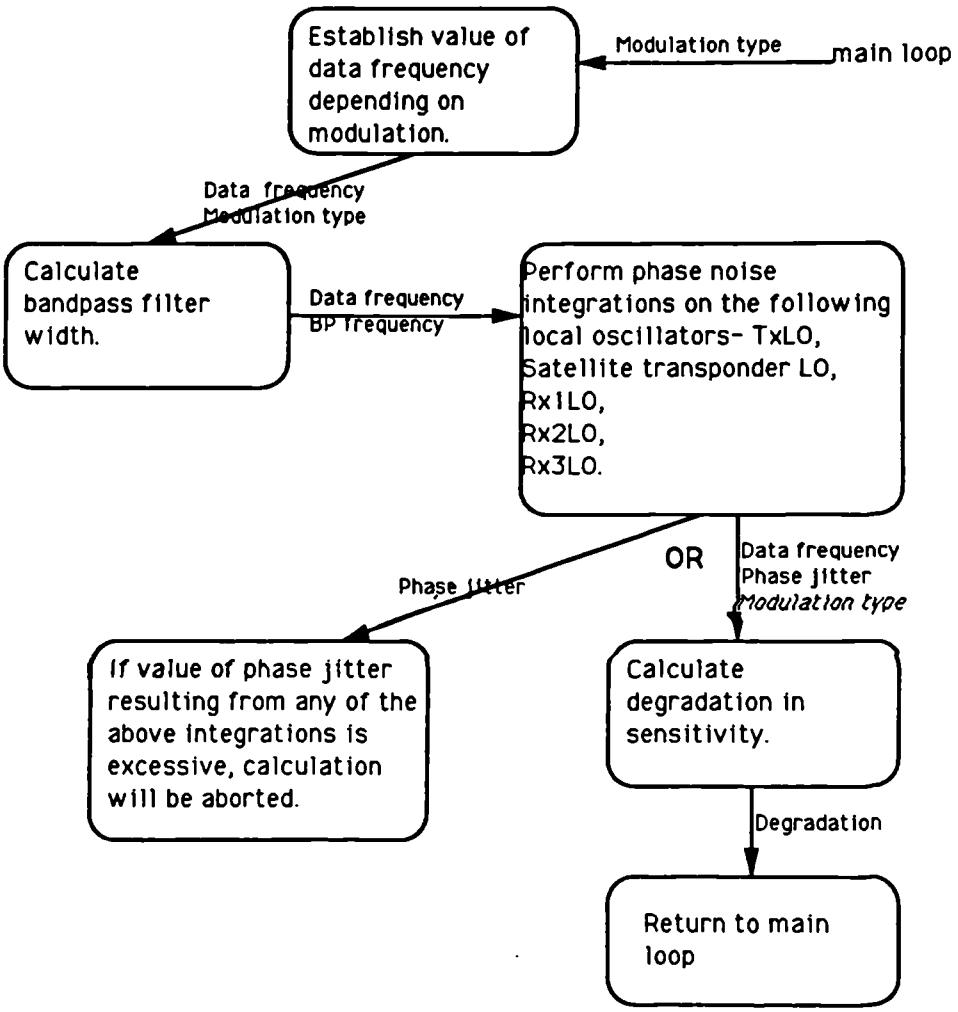
Main Process - Datarate Degradation



Main Loop - Datarate Degradation

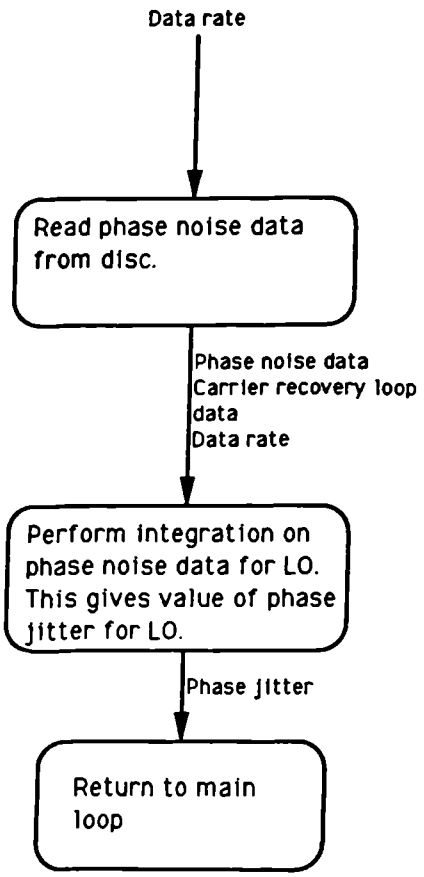


Main Calculations Of Sensitivity For Given BER - Datarate Degradation

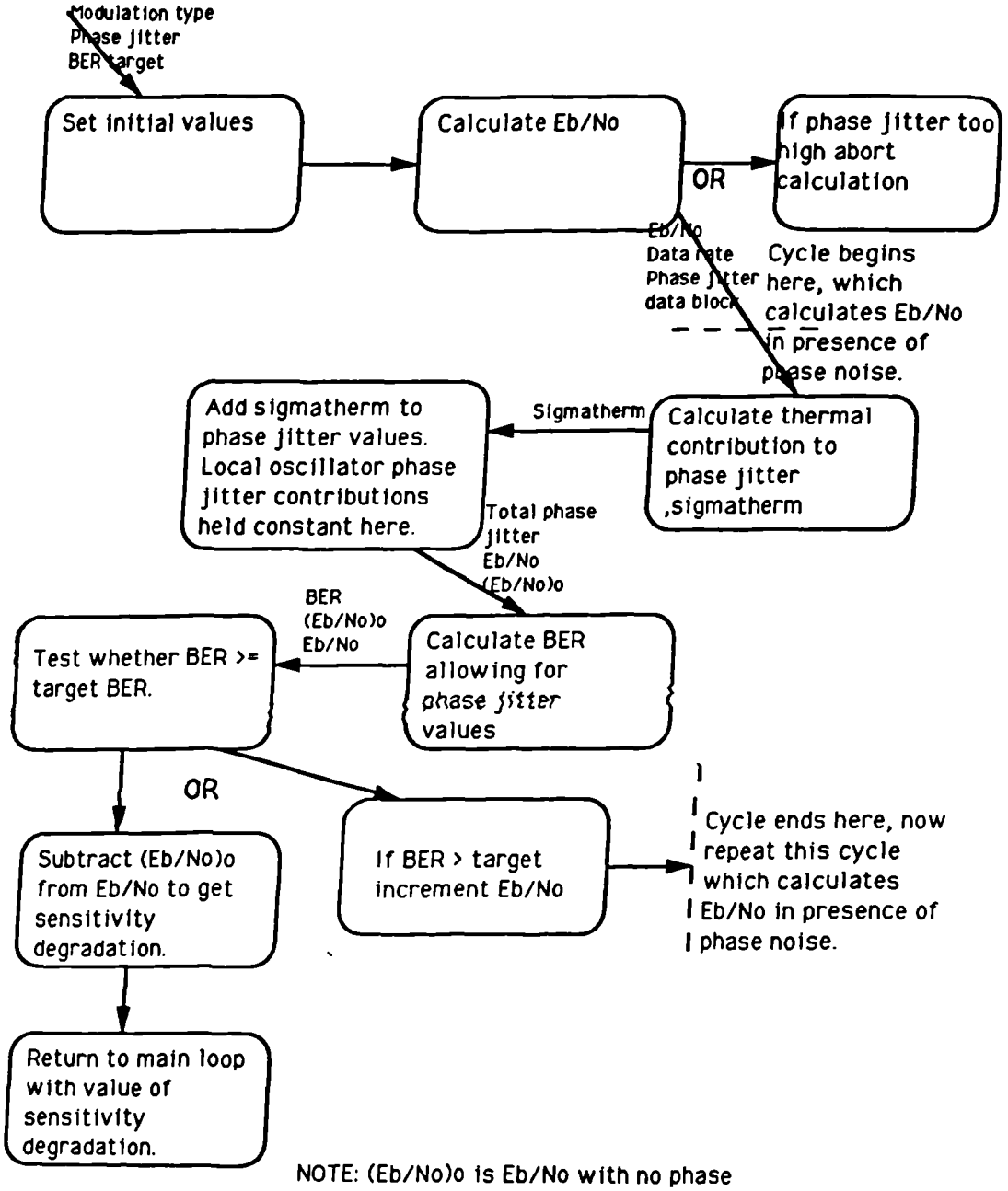


Phase integration on local oscillators

NOTE: This data flow is the same for each LO. However the method of integration varies depending on whether LO is a synthesiser or fixed oscillator.



Calculation of Sensitivity Degradation for a Given Phase Jitter



NOTE: (Eb/No)o is Eb/No with no phase noise.

A5.7 Pseudocode for phase noise link budget degradation calculations, main program

```
Package body datarate_degradation

with CRT,DOS,GRAPH,printer,tranphas,satphas,lo1pha,lo2pha,lo3pha,bercalc,
    globs_tv,datastor,dataplay,graphprn,plotdata;

-- This package gives plot of phase degradation using coherent PSK.
-- The graph obtained is of sensitivity degradation (y axis) against data rate.

-- Declare variables used by main program and procedures in this package.

x,y,
lvb                 :   INTEGER;
grdriver,
grmode,
errcode,
fn,COUNT,
DT,
offsetdisp,
R_P                 :   INTEGER;
VMIN,
VMAX,
TMAX,
T, Tx,
Vx, Px,
XT, LT,
LTMAX,
TOFF,
LOGTOFF             :   REAL;

MUL,
mulstat,
tesmax,
logberate           :   REAL;
lp,
NUM,
offsetstr           :   STRING;
dispflag,
dummy,
tracestart          :   BOOLEAN;
modulation_type     :   CHAR;
modulation          :   MOD_SCHEME;
resultrecord,
resplayback         :   RESULTSBLOCK;

sigmavals           :   PHAS_JITTER;

Procedure main_calculation is
-- This procedure calls the units that perform the phase noise
-- integrations for their respective local oscillators.
-- Phase jitter variance values are then obtained for each local
-- oscillator, and finally another unit is called which returns
-- a value of bit error rate for the particular modulation scheme in use.
-- If any of the integration units returns an excessive value of phase
-- jitter, given by variable thetamax, the remaining calculations
-- and plotting are aborted for that particular value of datarate.

begin
limflag := FALSE;
-- When half rate Viterbi decoding scheme is used, the data rate
-- over the link will be twice the data rate at the input and the
-- output of the system.

case modulation is
    when bpsk,oqpsk                          =>
                        dat_freq := lt;
    when viterbi_bpsk, viterbi_oqpsk         =>
                        dat_freq := 2*lt;
end case;

-- Calculate pre-carrier recovery bandpass filter width.
bandpass := 250*dat_freq/40;

-- Now implement phase noise integration package for transmit local oscillator.
transmitlo(sigmavals);
if sigmavals.trans>thetamax then
    -- Calculation is aborted when limflag is true.
```

```
    limflag := TRUE;
else
    -- Now implement phase noise integration packages satellite transponder local
    --oscillators.
    satlo(sigmavals);
    if sigmavals.sat>thetamax then
        limflag := TRUE;
    else
        -- Now implement phase noise integration package for receiver first LO.
        receivelo1(sigmavals);
        if sigmavals.lo1>thetamax then
            limflag:=true
        else
            -- Now implement phase noise integration package for receiver second LO.
            receivelo2(sigmavals);
            if sigmavals.lo2>thetamax then
                limflag := TRUE;
            else
                -- Now implement phase noise integration package for receiver third
LO.
                receivelo3(sigmavals);
                if sigmavals.lo3>thetamax then
                    limflag := TRUE;
                else
                    pskcalc(sigmavals,berate,degraddb,modulation);
                end if;
            end if;
        end if;
    end if;
end if;
end main_calculation;

procedure display_setup is

-- Procedure sets up graphics for display.

end display_setup;


Procedure read_result_file(valsplaback       : resultsblock);

-- Procedure reads record containing coordinates of lines
-- on plot of degradation (dB) against data rate (bps).
end read_result_file;

-----------------------------------------------------------------------
-- BEGINNING OF MAIN PROGRAM
-----------------------------------------------------------------------

PROGRAM DATARATE_DEGRADATION is
-- Mulstat is the starting value of datarate,
-- ltmax is the final value.
-- berate is the bit error rate used in the design study.

begin
-- Initialse variables.
Vx:=0;
Px:=0;
degraddb:=0;
LTMAX:=1000000;

MULstat:=100;
fn:=1;
toff:=LTMAX/MULstat;
berate:=1e-7;
-- Write message to screen 'static offset value in degrees?'
-- Read in value of offsetdeg
-- Write message to screen 'calculating plots[0] or replaying stored plots[1]?'
-- Read in value of R_P

If (R_P=1) then
    read_result_file (resplayback);
else
    -- Write to screen 'B=bpsk,v=viterbi_bpsk,o=offset_qpsk, q=viterbi_offset QPsk'
    -- Read in value of modulation_type
    case modulation_type
                'B'  =>  modulation := bpsk;
                'v'  =>  modulation := viterbi_bpsk;
                'o'  =>  modulation := oqpsk;
                'q'  =>  modulation := viterbi_oqpsk;
    end case;
```

```
    -- Theteamax is level of phase jitter at calculations are aborted.

    case modulation_type is
                'B'  =>  thetamax := 12;
                'v'  =>  thetamax := 12;
                'o'  =>  thetamax := 8;
                'q'  =>  thetamax := 8;
    end case;
end if;

-- Calculate data rate start and finish values
-- Take log to base 10 of toff and MULstat
tmax := LN(toff)/LN(10);
logtoff := LN(MULstat)/LN(10);

display_setup;

-- Calculate horizontal linear graticule
graticule(vmax,vmin);

tracestart := FALSE;
KRL := 0;

-- Plot 7 graphs with carrier recovery loop bandwidth as a parameter
-- the zero value of peram plots the logarithmic horizontal graticule

for peram in 0 to 7 loop
    -- mul is the factor of 10 multiplier used to give logarithmic plots
    -- KRL is the ratio of carrier recovery loop bandwidth to datarate
    mul := mulstat;
    case peram is

        -- KRL is ratio of carrier recovery loop bandwidth to data rate, this
        -- ratio is different for each plot.

        0   =>  dummy := TRUE; -- dummy run to set up graticle
        1   =>  KRL     :=   1000;
        2   =>  KRL := 500;
        3   =>  KRL := 200;
        4   =>  KRL := 100;
        5   =>  KRL := 50;
        6   =>  KRL := 20;
        7   =>  KRL := 10;
    end case;

    if peram>0 then
        dummy := FALSE;
        tracestart := FALSE;
        refr := 0;

        while LT <= LTMAX loop
            -- Outer loop which repeats for each decade in datarate

            DT := 0;
            while DT <= 8 loop
                -- inner loop which provides the ten calculation poinst per
                -- decade of datarate.
                -- increment reference adress for datastorage array
                inc(refr);
                -- ten points are plotted per decade of datarate
                DT := 1 + DT;
                LT := DT*MUL;    -- mul is power of 10, dt is 1,2,3...

                if ((NOT dummy) and (R_P = 0)) then
                    -- If 0 then store points in record (record contains
                    -- 7 arrays of plot points), otherwise retrieves
                    -- record from previous calculation.
                    main_calculation;

                    -- Calculate distance along X axis for log plot
                    T := LN(LT)/LN(10);
                    T := T-LOGTOFF;

                    if dummy then
                        -- First time in main loop so plot graticule
                        if (DT = 1) or (DT = 2) or (DT = 5) then
                            LOGGRAT(dt,t);
                        end if;
                    end if;
                    if r_p = 1 then          -- Playback=1,record=0
                        -- replay stored calculation results
                        replayback(resplayback);
```

```
    degraddb := v;
end  if;

if NOT dummy then
    v := degraddb;
else
    v := 10;
    -- Calculate and store in array if calculation requested
    -- resultrecord of arrays, each array contains the calculated
    -- values for each curve
    restorage(resultrecord);
    p := 10;

    if ((NOT tracestart) or (dispflag)) then
        Vx := V;
        Px := P;
        tX := T;

        if dispflag then
            Vx := 29;
        end  if;
    end  if;

    -- display only if calculation valid

    if ((NOT dummy) and (NOT limflag)) then
        -- Plot start and finishing points depending
        -- on value of tracestart.
        DISPLAY(Tx,Vx,Px,T,V,P,krl,tracestart);
        Vx := V;
        Tx := T;
        Px := P;
    end  if;
dispflag := limflag;

tracestart := TRUE;
tesmax := 0.95*ltmax;
if lt>tesmax then
    dt := 9;
    lt := 2*ltmax;
end  if;
                end  if;
            end  loop          -- while DT <= 8;
            MUL:=MUL*10
        end  loop          -- while LT <= LTMAX
    end  if;
end  loop;        -- Outer loop for peram 0 to 7

if R_P=0 then
    -- file starage at end of calculation
    -- In code here write resultrecord to file 'f:plot.dat'
end  if;

hardcopy(1);

while NOT keypressed loop
end  loop;

end datarate_degradation;
end package datarate_degradation.
```

A5.8 Pseudocode for BER-sensitivity degradation package

```
Package bercalc is
with CRT,DOS,printer,globs_tv,thermalj;


-- Declare variables

a,b,
sigma,
sigmadeg,
sigmadeg1,
z,thetaoff,
dbeb_no,
dbeb_nox,
zx,eb_no,
```

```
eb_noe,ber,
vmax,vmin,
tmax,tmin,
thetarad      :   EXTENDED;
grdriver,
grmode,
pox,poy,
poz           :   INTEGER;

c             :   INTEGER;

-------------------------Maths functions ---------------------------

function Q (x   :   EXTENDED)   return  EXTENDED;

-- This function calculates the Q function according to Abromobwitz
-- and Stegun formula, equation 6.30.

 p  : constant    extended := 0.2316419 ;
b1  : constant    extended := 0.3193811530;
b2  : constant    extended := -0.356563782;
b3  : constant    extended := 1.781477937;
b4  : constant    extended := -1.821255978;
b5  : constant    extended :=1.330274429;

-- Declare variables for this function.
t,polyn,
pix,expo,
exfunc,
funcnum       :   EXTENDED;

begin
pix:=(1+p*x);
t:=1/pix;

-- Error trapping required to prevent floating point overflow.
polyn:=b1*t+b2*t*t+b3*t*t*t+b4*sqr(t)*sqr(t)+b5*sqr(t)*sqr(t)*t;
expo:=(x*x*-1)/2;

-- Modified for error trapping

if expo < -1000 then
    expo:=-1000;          -- overflow trap
    exfunc:=exp(expo);
    funcnum:=exfunc*polyn;
    q:=funcnum/sqrt(2*pi);
end Q;

function erfc (x : in     EXTENDED):     return  EXTENDED is
-- Returns a value of erfc(x)

begin
erfc:=2*q(x*sqrt(2));
end erfc;

function vitpoly (x : in     EXTENDED)   return  EXTENDED is
-- This function calculates polynomial fit to published
-- Viterbi ber curve as described in section %%%

coef0    : constant EXTENDED := -0.508;
coef1    : constant EXTENDED := -0.149;
coef2    : constant EXTENDED := -0.586;
coef3    : constant EXTENDED := +0.184;
coef4    : constant EXTENDED := -0.019;

-- Declare variables for this procedure

polyres,
polytest          :   EXTENDED;

begin
polyres:= coef0 + coef1*x + coef2*x*x + coef3*x*x*x + coef4*x*x*x*x;
if polyres<-100 then
    polyres:=-100;
end if;

polytest:= exp(ln(10)*polyres);

if polytest> 0.5 then
    polytest:=0.5;
end if;
```

```
vitpoly:=polytest;
end vitpoly;


function Io (x    : in:     EXTENDED)        return  EXTENDED is

-- Returns modified Bessel function order zero.
-- Algorithm obtained from formulas listed in
-- Dwight(1961, chap 10 p195-196).

-- Declare variables for function

test,
power        :    INTEGER;
itest,coef,
denom,
powvar,
term,Ios,
plop,
expx         :    EXTENDED;

begin

if x<10 then
     -- Use normal series
     -- Initialisatise variables
     powvar:=1;
     Ios:=1;
     power:=1;
     denom:=1;

     while Itest >= 1e-6 loop

          -- Calculate each term in the series
          for test  in 1..power loop
               powvar := x*x*powvar;
               denom := 2*test*2*test*denom;
          end  loop;

          term := powvar/denom;
          powvar := 1;
          denom := 1;
          Ios := Ios+term;
          Itest := term/Ios;
          inc (power);
     end  loop;          -- while Itest >= 1e-6;

     Io := Ios;

else
     -- x > 10 therefore do asymptotic series.
     power:=1;Ios:=1; powvar:=1; denom:=1;
     plop := sqrt(2*pi*x);
     expx := exp(x);
     coef := expx/plop;

     while Itest >= 1e-6 loop

          for test in 1..power loop
               powvar := sqr(2*test-1)*powvar;
               denom := test*8*x*denom;
          end  loop;

          term := powvar/denom;
          powvar := 1;
          denom := 1;
          Ios := Ios+term;
          Itest := term/Ios;
          inc (power);

     end  loop;          -- while Itest >= 1e-6;

     Ios:=Ios*coef;
     Io := Ios;
end if;
end Io;



function tkbpsk (alpha,
                 piox,
                 x              : in:     EXTENDED)        return  EXTENDED is
```

```
-- Declare variables for this function

pt,
pexp    :    EXTENDED;
-- Calculates distribution according to
-- Tikonhov distribution formula between
-- -pi/2 and pi/2, see equation 6.10

begin
pexp := exp(alpha*cos(2*x));
pt := pexp/(pi*piox);
tkbpsk := pt;
end tkbpsk;

function tkqpsk (alpha,
                 piox,
                 x        : in:        EXTENDED) return EXTENDED is

-- Declare variables

pt,pexp :    EXTENDED;

-- This fucntion calculates distribution according to
-- Tikonhov distribution formula between -pi/4
-- and pi/4, see equation 6.10.

-- Tikonhov distribution formula.

begin
pexp := exp(alpha*cos(4*x));
pt := 2*pexp/(pi*piox);
tkqpsk := pt;
end tkqpsk;


function db (x   : in:    EXTENDED) return EXTENDED is

-- This function converts power to dB.

begin
```



```
dB := 10*ln(x)/ln(10);
end db;


procedure integrand_BPSK (alpha,
                          piox    : in :    EXTENDED;
                          x,
                          integfun  :in out:        EXTENDED)      is

-- This procedure contains formula that is to be
-- integrated, see equation 6.14.

-- Declare variables

eb_noeff,
ebnoal,
temp,temp2,
temp3       :    EXTENDED;

begin
ebnoal := cos(thetarad+x);
eb_noeff := eb_no*ebnoal*ebnoal;
temp := sqrt(eb_noeff);
temp2 := tkbpsk(alpha,piox,x);
temp3 := erfc(temp);
integfun := temp2*temp3/2;
end integrand_BPSK;

Procedure integrand_Vbpsk (alpha,
                           piox          : in:    EXTENDED;
                           x,
                           integfun      : in out:        EXTENDED)
   is

-- This procedure contains the integrand for BPSK
-- with Viterbi using equations 6.8 and 6.34.

-- Declare variables
eb_noeff,
ebnoal,
temp,temp2,
```

```
temp3          :    EXTENDED;

begin
ebnoal := cos(thetarad+x);
eb_noeff := eb_no*ebnoal*ebnoal;
if eb_noeff<0.0001 then
    eb_noeff:=0.0001;
end if;

temp := db(eb_noeff);
temp2 := tkbpsk(alpha,piox,x);
temp3 := vitpoly(temp);
integfun := temp2*temp3;
end integrand_Vbpsk;



Procedure integrand_oqpsk (alpha,
                                    piox    :in:    EXTENDED;
                                    x,
                                    integfun        :in out:        EXTENDED)
    is

-- This procedure contains the integrand for offset QPSK,
-- as given by equations 6.8, 6.28 and 6.32.

-- Declare variables
eb_noeff1,
eb_noeff2,
ebnoalc,
ebnoals,
temp1,temp2,
temp3,
pqpsk,
pbpsk,
eb_noeffb       :    EXTENDED;

begin
ebnoalc := cos(thetarad+x);
ebnoals := sin(thetarad+x);
eb_noeff1 := sqrt(2*eb_no)*(ebnoalc+ebnoals);
eb_noeff2 := sqrt(2*eb_no)*(ebnoalc-ebnoals);

temp1 := Q(eb_noeff1);
temp3 := tkqpsk(alpha,piox,x);
temp2 := Q(eb_noeff2);
pqpsk := 0.5*( temp1+temp2);
eb_noeffb := sqrt(2*eb_no)*ebnoalc;
pbpsk := Q(eb_noeffb);

integfun := 0.5*(pbpsk+pqpsk)*temp3;
end integrand_oqpsk;


Procedure integrand_Voqpsk (alpha,
                                    piox    :in:    EXTENDED;
                                    x,
                                    integfun        :in out:        EXTENDED) is
-- This procedure contains the integrand for offset QPSK
-- with Viterbi as given by equations 6.8, 6.28, 6.32 and 6.34.

-- Declare variables.

eb_noeff1,
eb_noeff2,
ebnoalc,
ebnoals,
temp1,temp2,
temp3,tempdb1,
tempdb2,pbpsk,
pqpsk,eb_noeffb,
tempbpsk        :    EXTENDED;

begin
ebnoalc := cos(thetarad+x);
ebnoals := sin(thetarad+x);
eb_noeff1 := eb_no*(ebnoalc+ebnoals)*(ebnoalc+ebnoals);
if eb_noeff1<0.0001 then
    eb_noeff1:= 0.0001;
end if;

eb_noeff2 := eb_no*(ebnoalc-ebnoals)*(ebnoalc-ebnoals);
```

```
if eb_noeff2<0.0001 then
    eb_noeff2:=0.0001;
end if;

tempdb1 := db(eb_noeff1);
tempdb2 := db(eb_noeff2);

temp1 := vitpoly(tempdb1);
temp3 := tkqpsk(alpha,piox,x);
temp2 := vitpoly(tempdb2);
pqpsk := 0.5*( temp1+temp2);
eb_noeffb := eb_no*ebnoalc*ebnoalc;
if eb_noeffb<0.0001 then
    eb_noeffb:=0.0001;
end if;

tempbpsk := db(eb_noeffb);
pbpsk := vitpoly(tempbpsk);
integfun := 0.5*(pbpsk+pqpsk)*temp3;

end integrand_Voqpsk ;


Procedure integral (alpha,
                    piox  :in:        EXTENDED;
                    lolim,
                    hilim,
                    integres   :in out:        EXTENDED;
                    steps  :in:                INTEGER;
                    modulation         :in:    MOD_SCHEME);

-- Performs integration according to Simpsons rule between limits lolin,
-- hilim, for function in integran, for a number of steps defined by
-- steps.  Passes out the result as integres.

-- Declare variables.

h,intvar1,
intvar2,intvar3,
x,integfun        :   EXTENDED ;
pnt,n,
m,intest          :   INTEGER;

begin
n := 2*steps;
h := (hilim-lolim)/n;
pnt := 0;
intvar3 := 0;

while pnt <= n loop

    x := lolim+(hilim-lolim)*pnt/n;          -- x:=dx in integral

    -- even value of pnt, m=2, odd value of pnt,m=4
    intest := pnt div 2;
    if 2*intest=pnt then
        m:=2;
    else
        m:=4;
    end if;

    if ((pnt=n) or (pnt=0)) then
        m:=1;
    end if;

    case modulation is

        -- This case statement selects which integrand to use.

        when Bpsk          =>
                                integrand_bpsk (alpha, piox, x, integfun);
        when Viterbi_Bpsk  =>
                                integrand_Vbpsk(alpha, piox, x, integfun);
        when oqpsk         =>
                                integrand_oqpsk(alpha, piox, x, integfun);
        when Viterbi_Oqpsk =>
                                integrand_voqpsk(alpha, piox, x, integfun);
    end case;

    intvar2 := integfun *m*h/3;
    intvar3 := intvar3+intvar2;
```

```
    pnt := pnt+1
end  loop;        -- while pnt <= n

integres := intvar3;
end integral;

function antidb (x    :in:      EXTENDED) return EXTENDED;
-- Finds power from a db value.

begin
    antidb := exp(ln(10)*x/10);
end antidb;

------------------------------ end of maths functions ----------------------------------
Procedure pskcalc (sigma          : in :    PHAS_JITTER;
                   bertarg        : in      EXTENDED;
                   dbdeg          : out     EXTENDED;
                   modulation     : in:     MOD_SCHEME)      is

-- This is top procedure of this package, and it is called by
-- a procedure in the package Datarate_degradation.
-- This procedure performs calculation of degradation in
-- sensitivity from recovered carrier phase jitter with a
-- coherent PSK system.

-- Declare variables

ber0,
 deb_no0,
sigmasqr,
sigmasqr1,
alpha,
sigmarad,
piox,
low,
 high,
integres,
db_ebnoe              :    EXTENDED;
interval,
mod_factor        :    INTEGER;

begin

-- Convert fixed offset to radians
thetarad := offsetdeg*2*pi/360;

-- Starting point Eb/no is 4dB
dbeb_no := 4;

-- Interval = 1 gives coarse stepping of iterations, 2 gives
-- fine stepping

for interval in 1..2 loop
    -- This outer loop evaluates whether Eb/no is stepped in coarse
    -- steps or in fine steps.

    while ber0 >= bertarg loop

        -- This loop calculates the Eb/no (the variable deb_no0) sensitivity
        -- with a perfect recovered carrier. Using the value of Eb/no the
        -- bit error rate (the variable ber0) is calculated and this BER
        -- is compared with a target BER (the variable bertarg). The loop stops
        -- when calculated BER is less than target BER.

        -- Calculate actual Eb/no from the corresponding value in dB.
        eb_no := antidb (dbeb_no);

        -- eb_noe is the effective Eb/no allowing for a static phase error
        -- thetarad in the recovered carrier

        eb_noe := eb_no*sqr(cos(thetarad));

        -- Calculate bit error rate for zero carrier phase jitter, ber0

        case modulation is
                when   bPsk, oqpsk      =>
                                        ber0 := (erfc(sqrt(eb_noe)))/2;   -- Eqution
6.1
                when Viterbi_Bpsk,
                     Viterbi_oQpsk      =>
                                        ber0 := vitpoly(db_ebnoe);          --
Equation 6.34
```

```
        end case;

        if (interval = 1) then
                dbeb_no := dbeb_no+1;
        else
                dbeb_no := dbeb_no+0.1;
        end if;

    end loop;   -- while ber0 >= bertarg (bit error rate target)

    if interval = 1 then
        dbeb_no := dbeb_no-2;
    else
        dbeb_no := dbeb_no-0.1;
    end if;

end loop;   -- interval 1 to 2

deb_no0 := dbeb_no;

-- deb_no0 is the Eb/no in dB for the specified erroer rate with
-- no recovered carrier jitter
eb_no0 := antidb (dbeb_no);

-- obtain value for thermal contribution to phase jitter

case modulation is
    when   BPsk,
           Viterbi_Bpsk      =>  thermalBPSK;
    when   oQpsk,
           Viterbi_oQpsk =>      ThermalQpsk;
end case;

sigmasqr1 := sqr(sigma.sat)+sqr(sigma.trans)+sqr(sigma.lo1)+
                sqr(sigma.lo2)+sqr(sigma.lo3);
 -- sigmadeg1 is the toal value of phase noise jitter
sigmadeg1 := sqrt(sigmasqr1);

 --LO noise is irreducable at this stage so therefore this is
-- not calculated in the iterations that follow.
```



```
if sigmadeg1>thetamax then
    -- phase jitter too high; abort calculation
  limflag := TRUE;
  -- return to calling procedure
else
    -- Mod_factor is introduced to correct the probability distritributions
    -- for the fact that CRL phase detection takes place at a multiple of the
    -- carrier frequency.

    case modulation is
        BPsk,
        Viterbi_Bpsk          =>  mod_factor := 2;
        oQpsk,
        Viterbi_oQpsk     =>  mod_factor := 4;
    end case;

    for interval in 1..2 loop
        -- repeat loop iteration - first time around loop stepping
        -- Eb/no with coarse steps and second time around
        --  loop stepping Eb/no in fine steps.

        while ber >= bertarg loop
            -- Iteration now follows the phase noise curve

            --eb_no0 is the presently calculated
        -- value of Eb/no

            eb_no0 := antidb (dbeb_no);

            -- Calculate value of thermal noise phase jitter for
            -- each iteration.

            case modulation is
                BPsk,
                Viterbi_Bpsk                => thermalBPSK;

                oQpsk,
                Viterbi_oQpsk     => ThermalQpsk;
            end case;

            sigmasqr := sqr(sigmathe)+sqr(sigmadeg1);
```

```
    -- sigmadeg is the total jitter on recovered carrier
    sigmadeg := sqrt(sigmasqr);        -- equation 6.34a
    sigmarad:=sigmadeg*2*pi/360;

    -- alpha is the signal to noise ratio as used by equation 6.11

    alpha := 1/(mod_factor*mod_factor*sigmarad*sigmarad);

    -- piox is the value of the modified bessel function
    -- corresponding to the value of alpha
    Piox := Io(alpha);
    eb_no := antidb (dbeb_no);        -- converts from dB to power

    -- Now perform BER equations which allow for carrier
    -- phase jitter.

    low := -pi/mod_factor; high:=pi/mod_factor;
    -- Perform numeric integration from -pi/2 to pi/2 to
    -- find value for ber.

    integral  (alpha,piox,low,high,integres,100,modulation);
    -- Now assign result to BER
    ber:=integres;

    if interval = 1 then
        -- coarse steps
        dbeb_no := dbeb_no+1;
    else
        -- fine steps
        dbeb_no := dbeb_no+0.1;
 end if;

    -- Loop ends when BER is less than target.
end  loop;          -- while ber >= bertarg

if  interval  = 1 then
    dbeb_no := dbeb_no-2;
else
    dbeb_no := dbeb_no-0.1;
end  if;
```



```
    end  loop;          -- interval 1 to 2

    -- Sensitivity degradation in dB is the difference between the
    -- sensitivity for the ideal carrier recovery and carrier recovery
    -- with phase noise.

   dbdeg := dbeb_no-deb_no0;
end  if;

end pskcalc;
end package bercalc;
```

A5.9 Pseudocode for local oscillator phase noise curve integration package

```
Package tranphas is
-- This package contains code to calculate jitter contributions from
-- transmitter ground station local oscillator.

with CRT,DOS,globs_tv;

--- The record phaseblock contains phase noise parameters for
-- transmit local oscillator and details of carrier recovery
-- loop.  This record is read from a file on the hard disk.

type PHASEBLOCK_TRANS is record


    n,   :    INTEGER;          Number of phase noise curve points

    krl_nato_freq,          Carrier recovery loop
                                natural frequency Hz
    crldamp       :    REAL;    Carrier recovery loop damping
                                  factor
    --The following arrays store points of frequency
    --against phase noise
```

```
    fnum,                       Phase noise curve frequency
                                point

    PNUM                        Phase noise value
                        :       array[1..100] of REAL;
    b               Number of Simpson's rule
                    Integration calculation points per decade
    :   INTEGER;

end record;

-- Declare file containing above record.

phase_file    :    file of PHASEBLOCK;


Procedure transmitlo(sigma      : in out :    PHAS_JITTER)      is

phase_vals    :    PHASEBLOCK;

begin

-- Performs integration of the product of the local oscillator phase noise curve
-- and the error response of the carrier recovery loop (CRL).
-- The phase noise curve is as described in section 9.7.2.7 for an oscillator
-- where the phase noise is given for a range of offset from carrier frequencies.
-- Logarithmic interpolation is applied to enable a continous phase noise
-- function to be formed for integration as described by equation (9.3).
-- This function is multiplied by the error function E(s) of the carrier
-- recovery loop, equation (6.38) and the resultant is integrated numerically
-- by Simpson's rule and the summation rule of equation (9.1) up to an
-- offset from carrier frequency of the link datarate.
-- On completion of the integration, a value of phase jitter is assigned to
-- the corresponding field in the phase jitter type record sigma. The phase
-- noise points and the CRL parameters are read from a file of type
-- phase_file prevously stored on the hard disk.

-- Declare a variable of type phaseblock which is used in this
this procedure.

end transmitlo;
```



```
end package tranphase.
```

A5.10 Pseudocode for synthesised local oscillator integration package

```
package lo2pha is

-- This package contains code to calculate jitter contributions
-- from a synthesised local oscillator in the receiver.

with CRT,DOS,globs_tv;

type PHASEBLOCK_LO2 is record
    vcoh_point,             VCO 1/f**3 phase noise 1Hz
                                        intercept point

    pd_floor,                   Phase detector noise floor

    fnx,                        Synthesiser loop natural
                                    frequency in Hz

    pdh_point,              Phase detector noise
                                    1/f 1Hz intercept

    krl_nato_freq,          Carrier recovery loop
                                natural frequency Hz

    pdnat_freq,                 Synthesiser loop natural
                                    frequency in Hz

    dampsynt,                   Synthesiser damping factor
    crldamp     :   REAL;       Carrier recovery loop damping
                                    factor
    b               Number of Simpson's rule
                    Integration calculation points per decade

    b
```

```
    :   INTEGER;
end record;

type PHASEBLOCK_LO2 is record
    vcoh_point,
    pd_floor,
    fnx,
    pdh_point,
    pdnat_freq,
    dampsynt,
    crldamp          :        REAL;
    b                :        INTEGER;
end record;


-- Declare file containing above record.

phase_file    :    file of PHASEBLOCK_LO2;

Procedure receivelo2(sigma   :in  out:     PHAS_JITTER) is

phase_vals    :    PHASEBLOCK_LO2;

begin

-- Performs integration of the product of the local oscillator phase noise curve
-- and the error response of the carrier recovery loop (CRL).
-- The phase noise curve is as described in section 9.7.2.8 for a synthesised
-- local oscillator where the synthesiser configuration is known. The
-- synthesiser is assumed to be a third order type two single PLL. The phase
-- noise sidebands of this PLL include contributions from the summation
-- of the digital logic phase noise multiplied by the transfer function and from
-- the VCO phase noise multiplied by the synthesiser loop error function. The
-- overall phase noise of the synthesiser is as defined in equations 9.4 and 9.6
-- of section 9.7.2.8.

-- This overall phase noise sideband function is multiplied by the
-- error function E(s) of the carrier recovery loop, equation (6.38) and
-- the resultant is integrated numerically by Simpson's rule and the summation
-- rule of equation (9.1) up to an offset from carrier frequency of the link datarate.
-- On completion of the integration, a value of phase jitter is assigned to the
-- corresponding field in the phase jitter type record sigma. The synthesiser
-- parameters and component phase noise contributions together with the
-- CRL parameters are read from a file of type phase_file prevously stored
-- on the hard disk.

end receivelo2;
end package lo2pha.
```

A5.11 Pseudocode for thermal jitter package

```
Package thermalj is
-- This package contains code which calculates jitter contributions from
-- the carrier recovery loop response to thermal noise

with CRT,DOS,globs_tv;


Procedure thermalBPSK        is

begin

-- This procedure performs calculation of phase jitter contributions BPSK
-- from thermal jitter for a squaring loop according to equation 6.27 of
-- section 6.3.4, and assigns resulting value of phase jitter to variable sigmathe.
-- Assumes the use of a Gaussian presquarer filter.
-- Calculation derived from curve in Oberst & Schilling paper.

end thermalBPSK;


Procedure thermalQPSK        is

begin

-- This procedure performs calculation of phase jitter contributions QPSK
-- from thermal jitter for a quartic loop according to  equation
-- 6.33 of section 6.3.5, and assigns resulting value of phase jitter to
```

```
-- variable sigmathe. Assumes the use of a Gaussian presquarer filter.
-- Calculation derived from curve in Oberst & Schilling paper.

end thermalQPSK;

end package thermalj.
```

A5.12 Pseudocode for global type and variable declaration package

```
Procedure Globs_tv      is
-- This package contains global type and var declarations for variables which are used
-- in the DATARATE_DEGRADATION package.

with Globs_tv;
-- Declare types
type COMPLTYPE is (r,j);
type POINTS is 1..256;
type DISPSTORAGE is array[POINTS] of REAL;
type FLAGSTORAGE  is array[POINTS] of BOOLEAN;
type MOD_SCHEME is
        (BPSK, VITERBI_BPSK, OQPSK, VITERBI_OQPSK)
type PHAS_JITTER is record
    trans,sat,lo1,lo2,lo3       :    EXTENDED;
end record;

type RESULTSBLOCK is record
    arrdeg1,arrdeg2,arrdeg3,arrdeg4,arrdeg5,
        arrdeg6,arrdeg7   :    DISPSTORAGE;
    arrlim1,arrlim2,arrlim3,arrlim4,arrlim5,
        arrlim6,arrlim7: FLAGSTORAGE;
end record;

--Declare global variables
DAT_FREQ, BANDPASS :REAL;
dat_freq,
checkvarr,
thetamax, v,
bandpass :          REAL
degraddb,
thetaoff,
offsetdeg,
berate,
eb_no0,
sigmathe: EXTENDED;
limflag,
checkvarb:
boolean;
refr,
peram,
krl: EXTENDED;
--Declare file for tempory storage of results before or
--after storage or retrieval from the hard disk.
result_file : file of resultsblock;
end globs_tv;
```

A.6 References

Young, S.J. 1984 *An introduction to ADA*, Halstead press.

Sommerville, I. 1989 *Software Engineering*, . California: Addison-Wesley.

Strang, G. 1980 *Linear Algebra and its Applications*, Appendix C, pp. 371-375. 2nd ed., London: Acedemic Press.

Sedgewick, R 1988 *Algorithms*, Chap 37, p. 542. 2nd ed., NY : Addison-Wesley.

Appendix

B Published papers

Wilson, M.P. 9th May 1988 Low cost synthesised sources for VSAT frequency converter applications. *IEE Colloquium on Microwave components in telecommunications, London*

Wilson, M.P. & Tozer, T.C. 1989 Synthesisers for low data rate satellite receivers. *IEE Second Frequency Control and Synthesis Symposium.* Conference Paper Number **303.**

Wilson, M.P & Tozer, T.C. October 1989 The effect of Local Oscillator Phase Noise in Low Data-Rate Satellite Receivers. *IEE Colloquium Digest no 1989/114, Modems and Codecs for Satellite Communications", London.* p. 4/1

Wilson, M.P. 1990 Signal generation using digital to analogue conversion. *European patent application no 91302926.0*

Wilson M & Tozer T, 1991. Spurious reduction techniques for direct digital synthesis *Colloquium on Direct Digital Synthesis, Digest*. No 1991/172, Bradford

Wilson M & Tozer T, 1991. Computer simulation of SRDiode comb generators. *Proceedings of RF Expo West, Santa Clara*

Lee, B.S., Hardstone, J. & Wilson, M P. 1991 Phase locked loop oscillator control circuit. *GB patent application no 9113682.0*

Wilson M & Tozer T, 1991. Spurious reduction techniques for direct digital synthesis *Colloquium on Direct Digital Synthesis, Digest*. No 1991/172, Bradford

LOW COST SYNTHESISED SOURCES FOR VSAT FREQUENCY CONVERTER APPLICATIONS

Martin Wilson

VSAT SOURCES

This program of development has been concerned with the production of low cost downconverters for very small aperture (VSAT) receivers.

VSAT receivers are often used to receive narrow band data signals in a low carrier to noise environment; especially so if forward error correction is used which reduces the carrier power needed for a given bit error rate. In such cases narrow carrier recovery loop bandwidth is required [1]. As a result of this, low close to carrier phase noise is required from any LO's in the downconverters.

It is tempting to use a proprietary low noise block downconverter (LNB) used for the SHF to UHF conversion stage (Fig1). The LNB employs a dielectric resonator oscillator (DRO) as the SHF local oscillator (LO). The next stage of downconversion employs a simple two chip UHF synthesiser as the second LO.

The LNB system presents problems to the VSAT demodulator due to:-

1) The frequency uncertainty of the DRO (± 1 MHz) means that the demodulator acquisition tim can be unacceptably long for a narrow carrier recovery loop bandwidth.

2) The synthesiser and DRO phase noise result in excessive demodulator carrier phase slipping when used with a narrow carrier recovery loop bandwidth.

3) The phase noise is compounded by the presence of phase "jumps" which occur due to disturbances in DRO components, particularly because the DRO, with its high Q resonator, is subject to high flicker noise [2].

As an alternative the DRO can be substituted by an externally synthesised LO using a digital divider and phase detector. A wide tuning range VCO is used as a UHF reference oscillator which employs a low Q resonator, such that its phase noise is reduced by phase locking to a UHF reference. Close to carrier phase noise then becomes dominated by the crystal resonator of the UHF reference. In the critical region around the edge of the carrier recovery loop bandwidth, the phase detector/divider chain phase jitter is also important. A diagram of the phase - frequency detector is shown in Fig. 2 and was chosen because of its self acquisition properties.

PREDICTION OF DIGITAL DIVIDER AND DETECTOR PHASE NOISE

If the digital divider and detector are used to phase lock a microwave source, the phase noise floor of the digital devices dominate the resultant spectrum. This type of synthesiser system is edge driven, and can therefore be modelled considering a single direction transition. It would be very difficult to accurately model the phase jitter effects of digital logic because of the different internal states that exist, and the dependence upon IC internal state device characteristics. It is, however, possible to predict a general rule that can be applied to a particular logic technology from a few measurements at different frequencies. The edge transition results in a finite sampling time

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window τ, repeating at a reference frequency F_r which effectively samples the broadband noise floor of the input devices of the logic gates. The noise sidebands at multiples of F_r are aliased back and are added on a power basis (Fig 3). Assuming a flat noise spectrum, the noise contribution from each multiple of F_r is multiplied by the sampling function:-

$$P_{nF_r} = P_{F_r} \frac{(\sin^2 (\pi n F_r \tau)}{(\pi n F_r \tau)^2} \qquad (1)$$

where n is the multiple of reference frequency F_r , P_{F_r} is noise power at the reference frequency and P_{nF_r} is noise power at the n th harmonic of the reference frequency. In most cases $F_r << 1/\tau$.

The sampling of the noise results in a time jitter $\Delta\tau$ on the signal. This time jitter is proportional to the sampled noise voltage such that ;

$$\Delta\tau \alpha V_n$$

The *number of times the broadband noise is folded* around the reference frequency is inversely proportional to the reference frequency so there the noise power (root noise voltage) is increased in inverse proportion to the reference frequency;

$$\Delta\tau \alpha \frac{1}{F_r^{1/2}} \qquad (2)$$

Within the loop bandwidth, the time jitter $\Delta\tau$ is transferred directly to the output frequency (F_{out}).

The phase noise at the output frequency F_{out} is given by :-

$$\mathcal{L}_F = 2 (\Delta\tau\pi F_{out})^2 \qquad (3)$$

$\mathcal{L}_F$ is noise power spectral density (watts/Hz). Substituting (2) into (3) gives ;

$$\mathcal{L}_F \alpha \frac{1}{F_r} F_{out}^2$$

PHASE NOISE PREDICTION

By normalising F_r and F_{out} to 1 Hz, a general formula can be used to predict the phase noise performance of a digital divider/phase detector system [3] ;

$$\mathcal{L}_F = K (dbc) - 20 \log_{10} (F_{out}) + 10 \log_{10} (F_r) (dbc/Hz) \qquad (4)$$

In equation (4) K is the constant of proportionality, arising from the previous equation (3). Its value depends upon logic technology and is typically -180 dbc/Hz for HCMOS and -215 dbc/Hz for FAST TTL.

In addition, low frequency flicker noise is sampled by the transitions and therefore, below a certain offset frequency, the phase noise takes on a $(F_{mod})^{-1}$ dependence, where F_{mod} is the modulation frequency of the data signal consequently. The noise power density $\mathcal{L}_F$ increases 10 dB for each decade drop in modulation frequency. It is this effect which causes the principle degradation in low bit rate systems. In GaAs logic systems, although τ is very much reduced, the high flicker noise makes them unsuitable for use in systems that require good close to carrier phase noise.

Based on these observations, a fully synthesised downconverter using ECL variable modulus prescalers and fast logic dividers and phase detectors for first and second LOs can be considered. The phase performance (curve 3 of Fig 5) is barely acceptable, however, and additional problems arise due to current consumption and operating termperature range.

AN IMPROVED DESIGN

The addition of a well designed analogue phase detector to the two chip synthesisers as shown in Fig 4 results in a reduction in close to carrier phase noise (curve 4 of Fig 5). The self locking properties of the digital phase frequency comparator is initially used to acquire lock. When locking has taken place the analogue phase detector gives fine control of the VCO phase. As a result the dividers and digital phase detector are then removed from the loop. High noise CMOS components can be used, giving a number of advantages as follows ;

(i) Lower component cost

(ii) Lower current consumption

(iii) Smaller space requirements

(iv) Reduced electromagnetic interference problems.

(v) The use of a fixed prescaler rather than a variable modulus pre-scaler gives greater design flexibility.

(vi) Linear and predictable phase detector characteristics.

(vii) Reduction of reference spurious and mains related sidebands.

(viii) Operation at temperatures down to -30°C.

REFERENCES

1 PUCEL, A . *The GaAs FET Oscillator, Its Signal And Noise Performance. Proceedings of the 40th Annual Control Symposium, 1986.*

2 ROBINS. W.P. *Phase Noise In Signal Sources - IEE Press 1982*

3 UTSI. P.A.U. *Phase Noise In Digital PLL due to detectors and dividers - IEE Conference on Land Mobile Radio, March 1983, Leeds.*

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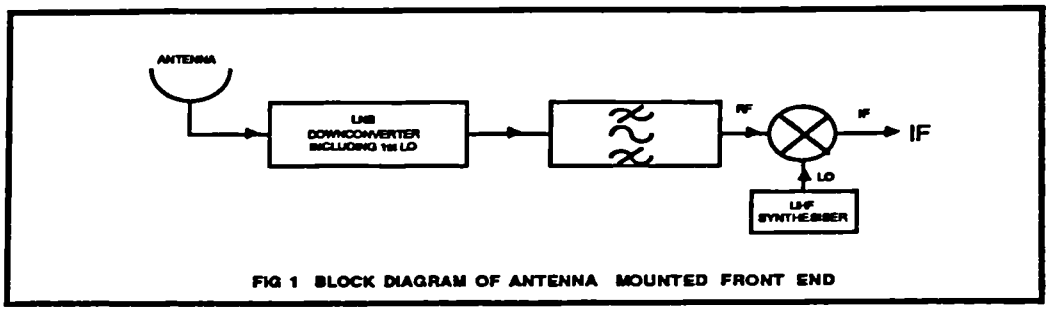


FIG 1 BLOCK DIAGRAM OF ANTENNA MOUNTED FRONT END

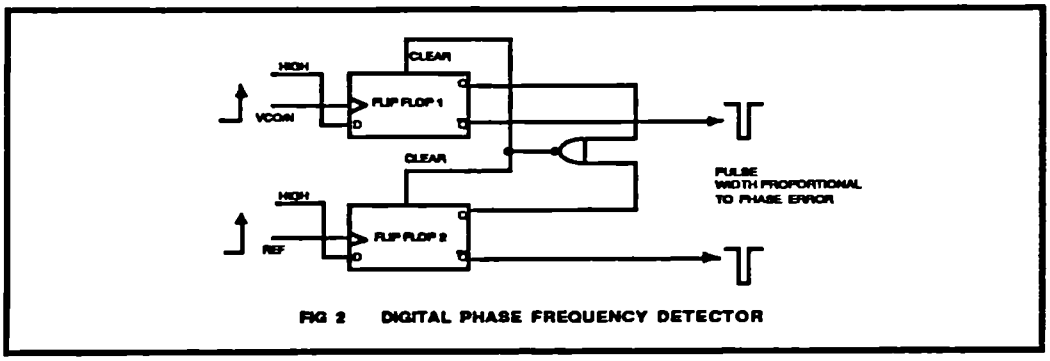


FIG 2 DIGITAL PHASE FREQUENCY DETECTOR

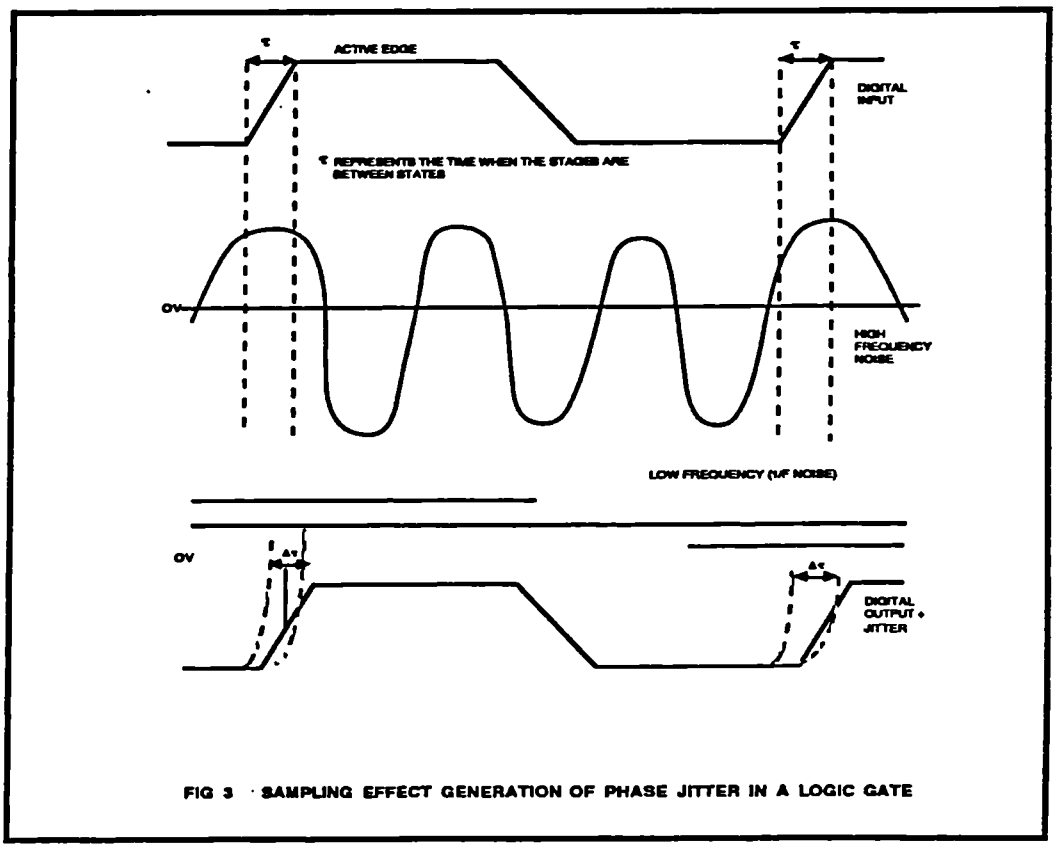


FIG 3 SAMPLING EFFECT GENERATION OF PHASE JITTER IN A LOGIC GATE

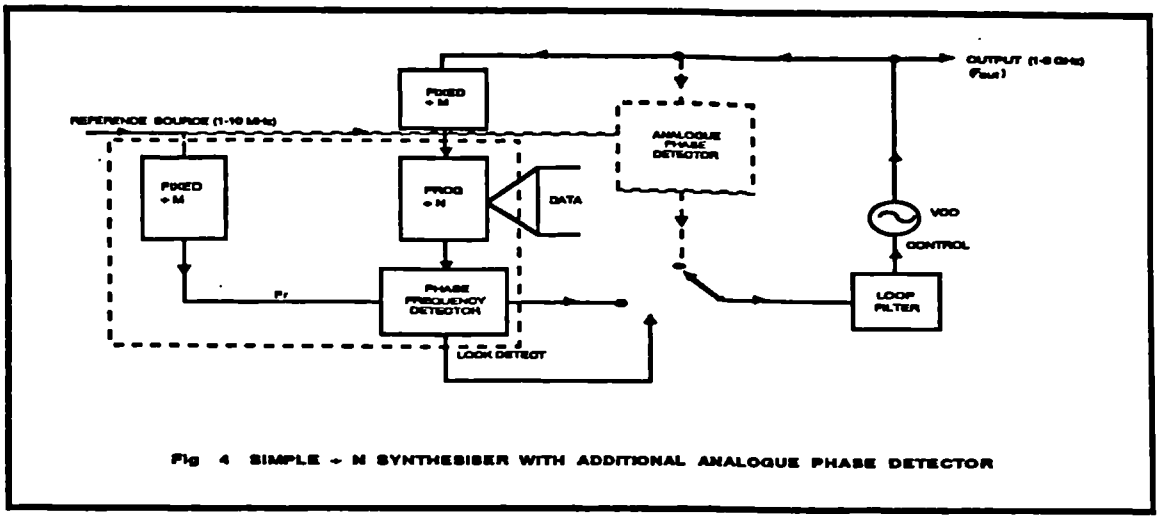


Fig 4 SIMPLE ÷ N SYNTHESISER WITH ADDITIONAL ANALOGUE PHASE DETECTOR

Fig 5 (below) Phase Noise Contributions for Various LO Implementations.

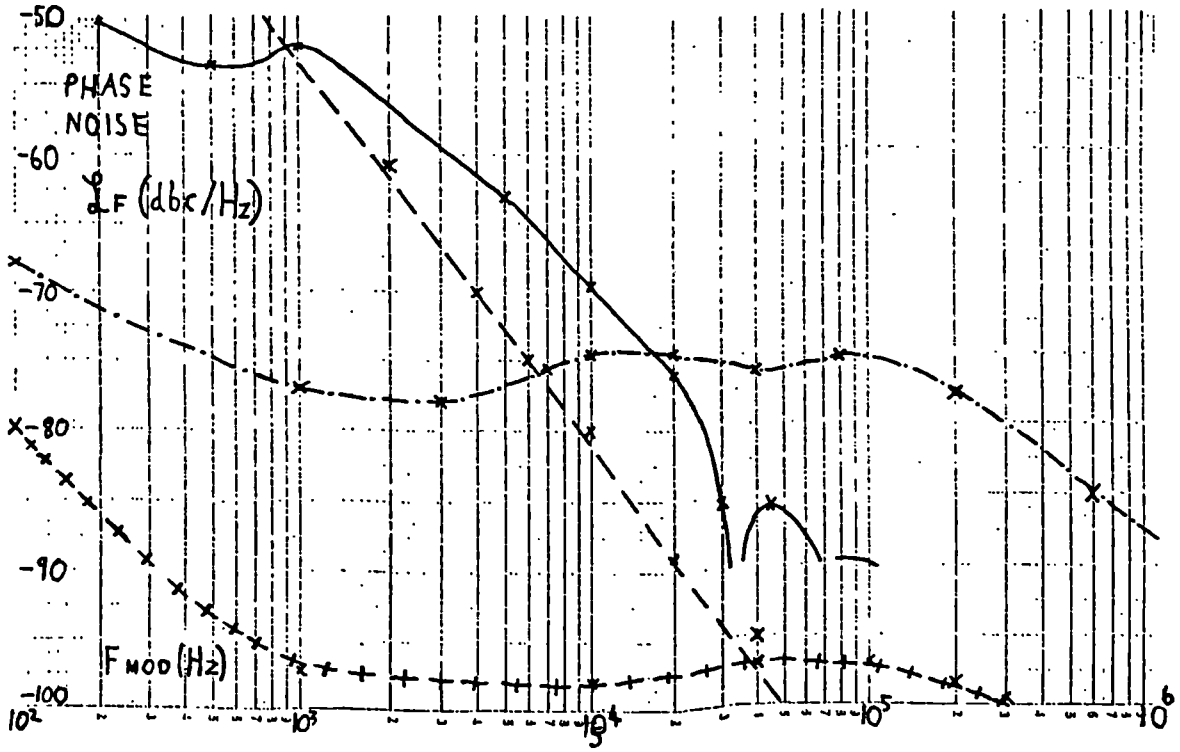
Key:

1 ———— Phase noise of 1st generation UHF synthesiser

2 ---------- Phase noise of SHF DRO Local Oscillator

3 -•-•-•-•-•- Phase noise of fully synthsised downconverter using FAST TTL logic

4 ++++++++++++ Phase noise of synthesised downconverter using twin phase detector technique



SYNTHESISERS FOR LOW DATA-RATE SATELLITE RECEIVERS

M.P. Wilson*& and T. C. Tozer&

*Communication Systems Research Ltd
&University of York, UK

INTRODUCTION

There is currently considerable interest in application of very small aperture terminals (VSATs) to business or mobile satellite communications. Such systems are well established in the USA, and are poised to expand into Europe, particularly as regulatory constraints are relaxed.

Because of the small antenna gain and associated low carrier-to-noise density, these terminals operate at a low data-rate (typically no higher than 64 kbit/s, and often considerably less). This places stringent requirements upon the phase noise produced by receiver downconverter local oscillators, which must also be frequency agile for flexible channel assignment, and producable at low cost.

As a result of the proliferation of consumer television receive-only (TVRO) systems, very inexpensive synthesised satellite receivers are widely available. However, although these may provide a satisfactory noise figure, they are frequently unsuitable for use in low data-rate communications due to their poor close-to-carrier phase noise. Here we examine some of the requirements and trade-offs for VSAT receivers.

The effects of synthesiser phase noise and thermal phase noise upon data demodulation are identified, together with the conflicting requirements placed upon the receiver's carrier recovery loop. The origins of phase noise in single-loop synthesisers are outlined, and its elements characterised. This leads to the derivation of some design criteria and parameters, and resulting performance is illustrated in the implementation of VSAT receivers.

PHASE NOISE CONSIDERATIONS

It is important to define exactly what is required in terms of phase noise within a particular system, and to avoid expensive over-specification. The VSAT system performance will aim to work close to the limits set by the basic link budget, in terms of satellite EIRP, antenna gain, and receiver LNB (low-noise block downconverter) noise figure. All of these are at a considerable premium, and a high price is demanded for any link margin as compensation for phase noise degradation of the bit error-rate (BER).

Many VSAT data systems may use error correction coding, such as convolutional codes with Viterbi decoding. The coding gain advantage further reduces the already low carrier-to-noise density in the receiver, placing very stringent requirements upon the demodulator design. Furthermore, the slope of the error curve with E_b/N_o can be very steep leaving little margin for uncertain degradations.

Figure 1 illustrates a typical receiver outline. Two or more stages of downconversion may be employed, (eg from a signal at 14 GHz to intermediate frequencies (IFs) at1 GHz and 70 MHz). The function of the carrier recovery loop (CRL) is to regenerate a carrier reference from the incoming signal, which is then used for coherent demodulation. Data modulation with binary phase shift keying (BPSK) is considered here, although the principles may be extended to QPSK, which is also commonly used.

The CRL is a squaring loop, or equivalently a Costas Loop [1], employing a phase-locked-loop (PLL) with transfer function H(s). Two components of noise are present at the input to the CRL:

a) *Oscillator phase noise* introduced by the downconverter stages. This noise component lies predominantly close-to-carrier and hence within the CRL's loop bandwidth (typically a few 10's of Hz). Thus to a large extent the loop can track this phase noise;

b) *Thermal noise.* This noise component has a flat spectrum, and will not be tracked.

Figure 2 [from ref.2] illustrates the degradation of BER due to the combination of thermal noise (N_o) and additional phase jitter. This jitter is manifest differentially at the inputs to the demodulating multiplier, and has variance σ_T^2 (radian^2). The jitter is due to two effects:

(i) Phase noise appearing differentially between the signal input and the CRL output. The difference arises because the CRL substantially tracks the phase jitter arising from the downconversion synthesiser(s);

(ii) Thermal phase noise appearing on the recovered carrier, which is not coherent with the signal input thermal noise by virtue of the effect of squaring circuit within the CRL.

It is clear that errors will occur as σ_T approaches the phase distance between symbols, and that the situation becomes more demanding for QPSK and higher orders of modulation. (In practice, the performance shown in Figure 2 may be further aggravated by non-linearities and cycle slips at low carrier-noise levels within the CRL).

The receiver designer has to face a trade-off in parameters for the CRL, which requires a wide loop bandwidth to track local oscillator phase noise and a narrow loop bandwidth to minimise thermal noise effects. Further design constraints may be imposed by acquisition and Doppler tracking requirements.

OSCILLATOR PHASE NOISE EFFECTS

Synthesiser phase noise is introduced at each stage of down-conversion in the receiver, and the phase noise powers will add. (It cannot be assumed that the contributions from each stage will be the same, and one may expect significantly greater phase noise from the higher frequency source, at say 12 GHz).

This phase noise lies mostly close-to-carrier, and it is this portion which will predominate over the other products produced by the squaring loop. In other words, the loop will largely track this jitter, such that the inputs to the demodulating mixer are not substantially uncorrelated.

The squarer itself is relatively wideband, and so the reponse of the CRL to this phase noise is determined approximately by H(s). Hence this phase noise contribution differentially to the demodulator multiplier is determined by:

$$1 - [H(s)]_{CRL} = [E(s)]_{CRL} \qquad \text{...(i)}$$

where E(s) is the PLL's error function [3].

The contribution of downconverter synthesiser phase noise to the differential jitter at the demodulator may be represented as:-

$$\sigma_p^2 = \int_{f=0}^{f=f_d} 2\mathcal{L}(f)\, |[E(s)]^2|_{CRL}.df \quad \text{(radian}^2\text{)} \qquad \text{....(ii)}$$

where $\mathcal{L}(f)$ is the phase noise power-density to carrier power ratio, and f_d is the data rate, taken to be a practical upper limit of integration.

The form of $\mathcal{L}(f)$ is very much dependent upon the particular synthesiser and its architecture, and there is no universally applicable result for this function. Some factors determining $\mathcal{L}(f)$ are discussed later.

In order to minimise σ_p^2, $|[E(s)]^2|_{CR}$ should be made as small as possible, which implies $[H(s)]_{CRL} \rightarrow 1$, and hence the PLL natural frequency ω_n chosen to be high [3]. This conflicts with the thermal noise requirement upon ω_n, as detailed below.

THERMAL PHASE NOISE EFFECTS

Besides the direct impact upon E_b/N_o, additive thermal noise gives phase jitter which is modified by the CRL, which is unable to fully track it. This gives rise to a differential input to the demodulator multiplier, and degradation of the data bit error rate (BER).

If the level of noise within the CRL bandwidth is high, then non-linear effects such as the addition of orthogonal amplitude modulation components of the noise also become significant. Cycle slipping also becomes a problem at low carrier-to-noise levels. In order to minimise cycle slipping, a high damping factor ζ in the CRL is desirable, and a value of 1·3 is generally chosen [4, 5].

The squaring function within the CRL gives rise to the product (noise) × (signal), which has a low correlation with the thermal noise additive upon the data signal. This decorrelated noise is subject to the CRL transfer function H(s).

The loss introduced by the squarer is dependent upon the shape of the bandpass filter preceeding it. For the particular case of a Gaussian pre-squarer bandpass filter of bandwidth B_p, we have [6]:-

$$\left(\frac{C}{N_o}\right)_{out} = \frac{B_p\sqrt{2}\left(\frac{C}{B_pN_o}\right)_{in}^2}{1+4\sqrt{2}\left(\frac{C}{B_pN_o}\right)_{in}} \qquad \text{....(iii)}$$

where C is the carrier power and N_o the thermal noise power density.

Thus the normalised thermal phase-noise power density following the squarer is given by:-

$$\mathcal{L}(f)_t = \frac{1}{2}\left(\frac{B_pN_o}{\sqrt{2}C} + 4\right)\frac{N_o}{C} \qquad \text{....(iv)}$$

Here the first term in the brackets represents the squaring loss. $\mathcal{L}(f)_t$ around the recovered carrier component will be flat over the relatively narrow bandwidth of the CRL frequency response H(s), after which $\mathcal{L}(f)_t$ is characterised by:

$$L(f)_t = \frac{1}{2}\left(\frac{B_p N_o}{\sqrt{2}C} + 4\right)\frac{N_o}{C}|H(s)|^2$$

...(v)

Since the output of the CRL will be halved in frequency to recover the actual carrier, the corresponding phase jitter variance applied to the demodulator is reduced by a factor of 4, and is given by:-

$$\sigma_t^2 = \left(\frac{B_p}{4\sqrt{2}}\frac{N_o}{C} + 1\right)\frac{N_o}{C}\int_{f=0}^{f=\infty}|H(s)|^2.\,df$$

....(vi)

Assuming a second order PLL, the integral in equation (vi) is equal to its equivalent noise bandwidth B_L , which is also given [7] by:-

$$B_L = \frac{\omega_n}{2}\left(\zeta + \frac{1}{4\zeta}\right) \quad \text{Hz}$$

....(vii)

where ζ is the loop damping factor.

For the particular case of $\zeta = 1.3$ (which is usually chosen, as described above),

$$B_L = \frac{3}{4}\omega_n \quad \text{Hz}$$

....(viii)

Therefore the natural frequency ω_n of the CRL may be related to the specified thermal noise jitter σ_t as follows:-

$$\omega_n = \frac{4}{3}\frac{\sigma_t^2}{\left(\frac{B_p}{4\sqrt{2}}\frac{N_o}{C} + 1\right)\frac{N_o}{C}}$$

....(ix)

With a given allowance for σ_t^2, ω_n may then be chosen. It is seen that a small ω_n is required, and thus a compromise is necessary between that value of ω_n required to minimise thermal noise phase jitter, and the tracking requirements due to local oscillator phase jitter.

SYNTHESISER STRUCTURE AND PHASE NOISE

The usual, and the most economical, synthesiser implementation for VSAT downconverters is the single PLL method. In order to maintain a fine frequency resolution over a large frequency range, a number of stages may be required. Each stage has its own loop synthesiser, with the higher local oscillator frequencies coarse stepping and the lower frequency oscillators fine stepping. Figure 3 shows the architecture of a single loop synthesiser; the loop consists of dividers and an edge triggered phase-frequency comparator.

Figure 4 displays the typical phase noise spectrum of such a synthesiser, which comprises a number of distinct regions. The f^{-3} region closest to the carrier is due to crystal resonator noise (multiplied up to the final output frequency). The f^{-1} and f^{0} regions arise from the active devices employed in both the phase-frequency comparator (and associated dividers) and the loop filter. The outer f^{-3} region represents the free-running voltage-controlled-oscillator (VCO) phase noise.

There appear to be several phenomena giving rise to the f^{-1} flicker noise in logic circuits, and this subject is felt to be an area requiring further investigation. The transition from the f^{-1} region to the white noise floor (f^{-0}) region for the logic jitter increases in frequency as the phase comparison frequency is increased. With CMOS comparators at a 25 kHz comparison frequency, for example, this transition point is approximately 50 Hz from carrier.

The phase noise contribution from the loop filter itself can be minimised with careful design. However, the jitter from the comparator and associated logic circuitry will remain as the principal contributor to the phase noise; this is exacerbated because the phase comparison in the synthesiser is often accomplished at a low frequency. The jitter may become a significantly large fraction of a radian when translated to the output frequency in the microwave region.

The mechanism for the generation of phase noise within logic circuitry has many sources [8], and i can be difficult to determine its value. However, it is possible to predict the phase noise levels for a particular phase detector logic technology and configuration, based upon observed measurements at a single frequency. This analysis is outlinec below. (The same criteria may be also applied tc oscillators, limiters, sine- to square- wave converters, and pulse generators used elsewhere within synthesisers).

LOGIC JITTER PHASE NOISE FLOOR

At the input stage of a logic gate, broadband noise is present up to an effective cut-off frequency determined by the input device and its technology, and this can be very high (eg 5 GHz) for TTL and ECL. This broadband noise will only contribute during the switching transition time τ . This ocurs once per cycle at the comparison frequency f_c (=1/T), as shown in Figure 5. The output noise spectrum may be expressed from consideration of the product of the input noise with a window function which is unity during time τ, and zero elsewhere.

Let the input noise power spectral density be γ_i (watts/Hz). The effective duty cycle is τ /T, and hence the output noise power spectral density is proportional to $\gamma_i \tau / T = \gamma_i \tau f_c$.

It is clear from the above that the phase noise is reduced as τ is diminished. This can be achieved with high speed logic with fast transition times, provided that γ_i is otherwise unchanged. The close-to-carrier phase noise at the synthesiser output will be contributed by several gates in the synthesiser loop. This phase noise will be multiplied up from the comparison frequency f_c to the output frequency f_{out}.

The phase noise contributions from each logic gate will add. Representing the normalised phase noise power-density (from the output of the phase detector) as $\mathcal{L}(f)_{opd}$, and the oscillator output power as C, then:-

$$\mathcal{L}(f)_{opd} = \frac{\gamma_i \tau f_c}{C} \left(\frac{f_{out}}{f_c}\right)^2 \quad \text{....(x)}$$

This result will also be subject to the transfer function of the synthesiser loop filter, $H(s)_{syn}$.

The overall phase noise will manifest itself as BER degradation in the receiver, determined by the CRL in the demodulator as outlined previously. It is therefore necessary to arrange to have as few active gates as possible in the synthesiser loop, and effectively reduce them in number through re-synchronisation techniques.

With the above relationship, it is possible to predict the synthesiser output phase noise for a particular output frequency and comparison frequency, for a given configuration and logic technology. Representing the logic contribution to the phase noise floor (f^0 region in Figure 4) as $\mathcal{L}(f)_{opd}$ dBc/Hz, then:-

$$\mathcal{L}(f)_{opd} = K_n + 20 \text{ Log } f_{out} - 10 \text{ Log } f_c \quad \text{dBc/Hz} \quad \text{...(xi)}$$

where K_n is a constant determined by the configuration and logic technology used, f_{out} is the synthesiser output frequency and f_c the synthesiser comparison frequency.

Based on measurements taken, the following values for K_n were determined for a typical single loop synthesiser with commonly used edge-triggered phase-frequency comparators:

K_n = - 200 dBc/Hz for fast CMOS

- 205 dBc/Hz for ECL and low-power schottky TTL

- 215 dBc/Hz for Fast series TTL.

(CMOS using MC145151, ECL using 10,000 series, LS series TTL, and 74F series TTL respectively).

The range shown here of 15 dB can be very significant in terms of resulting system performance. It is worth noting that although ECL has a fast switching speed, this advantage is offset by a high level of input noise γ_i. These results are supported independently by Utsi in [9].

CASE STUDY DESIGN EXAMPLE

The total phase noise produced by the synthesiser can be represented in terms of the f^0 floor $\mathcal{L}(f)_{opd}$, f^{-1} flicker noise region (closest to the carrier in Figure 4), and the VCO phase noise (f^{-3} region). The synthesiser normalised phase noise power-density can be expressed as:-

$$\mathcal{L}(f)_{p_{out}} = |H(s)_{syn}|^2 \left(\mathcal{L}(f)_{opd} + \left[\mathcal{L}(f)_{\substack{flicker \\ f=1}}\right]\frac{1}{f}\right) + \left(|1 - H(s)_{syn}|^2\right)\left[\mathcal{L}(f)_{\substack{vco \\ f=1}}\right]\frac{1}{f^3}$$

....(xii)

Here $\mathcal{L}(f)_{opd}$ is the phase noise contribution of the logic jitter, and the subsequent term represents the flicker noise normalised to that at 1 Hz offset from carrier. $\mathcal{L}(f)_{vco(f=1)}$ is the VCO phase noise extrapolated to 1 Hz offset, and $H(s)_{syn}$ is the synthesiser PLL transfer function.

The resultant synthesiser RMS phase jitter appearing differentially at the demodulator may now be determined numerically from equation (ii).

The above criteria are illustrated by a synthesiser having a 2 GHz output frequency, and using CMOS logic with a phase comparator operating at 50 kHz. The contribution to the output phase noise from logic jitter, $\mathcal{L}(f)_{opd}$. is then -61 dBc/Hz, from equation (xi). The synthesiser is observed to have a VCO phase noise of -40 dBc/Hz at 1 kHz offset.

The receiver operates at a data rate of 40 kbit/s and E_b/N_o of 6 dB, with half-rate Viterbi decoding. A value of σ_t is chosen initially to obtain a suitable compromise between BER degradation and the acquisition time of the CRL. The CRL employs a Gaussian pre-squarer filter with B_L = 200 kHz, ω_n = 31 Hz and ζ = 1.3. The above parameters may be typical of a VSAT receiver. The following demodulator jitter figures result:

σ_t thermal jitter	=	3.0°
σ_p phase noise jitter	=	10.7°
σ_T RSS total jitter	=	11.1°

In practice several iterations of the calculation may be performed in order to find the value of CRL ω_n that gives the lowest value of σ_T. As may be observed from the BER curves (Figure 2), the above parameters produce a degradation of about 1 dB in a BPSK system, and would have a very significant effect upon a QPSK or higher order modulation system.

The use of Fast TTL logic instead of CMOS in the synthesiser would result in a lowering of σ_p to 4.9°, giving a reduction in σ_T to 5.7°. Negligible degradation would then ensue for BPSK, although there would still be severe degradation for QPSK.

These results imply that the present generation of low-cost single chip CMOS synthesisers have severe limitations for low data rate downconverters.

CONCLUSIONS

Phase noise is a significant parameter in low data-rate receivers such as VSAT terminals. Both thermal noise and phase noise from downconversion synthesisers affect demodulators employing a carrier recovery loop (CRL), giving degradation of BER performance. Each places conflicting demands upon loop bandwidth of the CRL.

Single loop synthesisers are simple and attractive as downconverter local oscillators, but their phase noise can be excessively large for data receivers. It is possible to predict levels of phase noise from given configurations as a function of the logic technology employed. Synthesiser phase-frequency detectors may be critical design components. Some low cost synthesiser designs may prove inadequate in this respect to meet receiver BER requirements.

REFERENCES

[1] Holmes, J.K., "Coherent spread spectrum systems". J Wiley & Sons 1982. Chap 5, p 129

[2] *ibid.* Chap 6, p 284

[3] Blanchard, A., "Phase locked loops and their application to coherent receiver design". J Wiley & Sons 1976. Chap 6, p 105

[4] *ibid.* Chap 12, p 323

[5] Robins, W.P., "Phase noise in signal sources". Peter Perigrinus 1982. Chap 10 p 251

[6] Oberst, J.F. & Schilling, D.L, "The SNR of a frequency doubler". IEEE Trans Comm. Technology. Feb 1971 pp 97 - 99

[7] Gardner, F.M., "Phase lock techniques" Wiley, New York, (2nd edn) 1979. Chap 3, p 20.

[8] Robins, W.P., "Synthesiser phase jitter contributed by TTL and ECL components". Proceedings IEE Colloq on "Low Phase Noise Oscillators & Synthesisers", 23 January 1986.

[9] Utsi, P.A.V., "Phase noise in digital PLLs due to detectors and dividers". Proceedings IEE Conf. on "Land Mobile Radio", Leeds, March 1983.

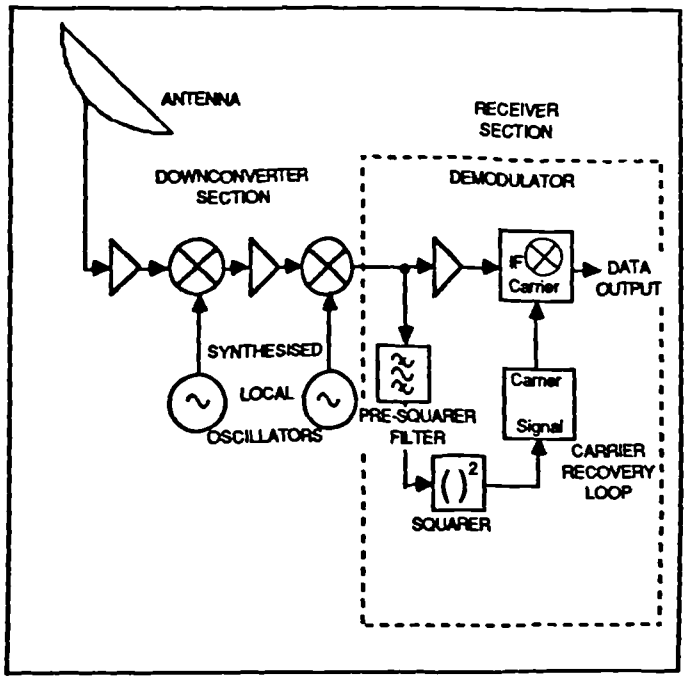


Figure 1 Simplified outline of VSAT receiver

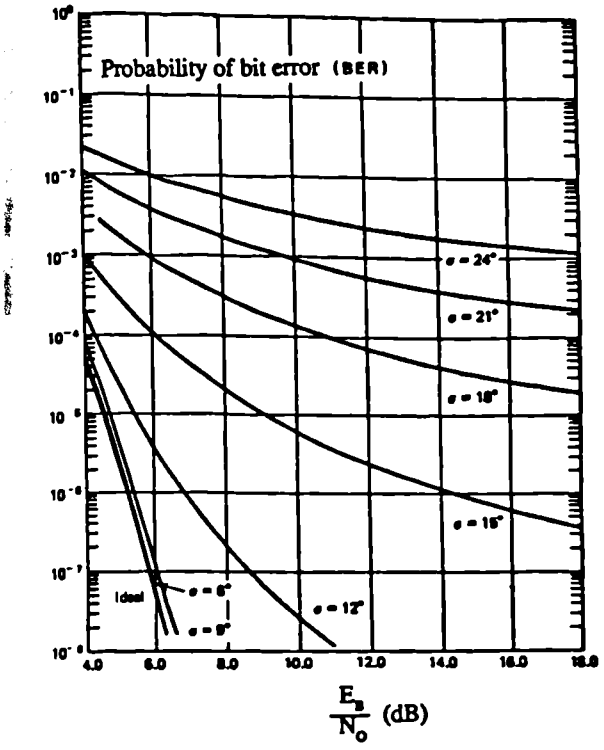


Figure 2 BER as a function of E_b/N_o and phase jitter. (From ref [2]; 3° static phase error, 1/2 rate Viterbi decoding)

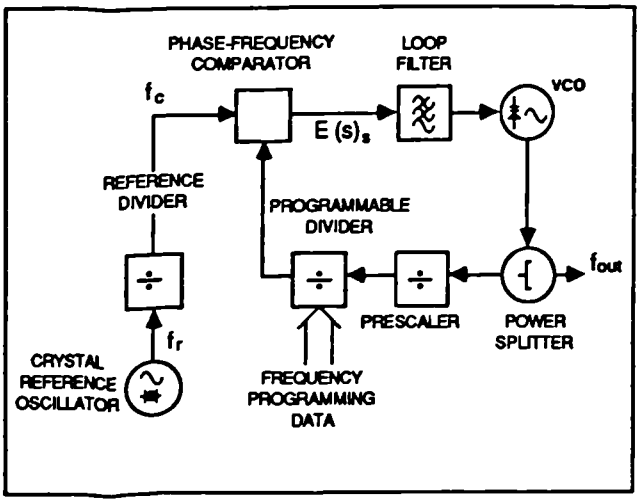


Figure 3 Single loop PLL synthesiser

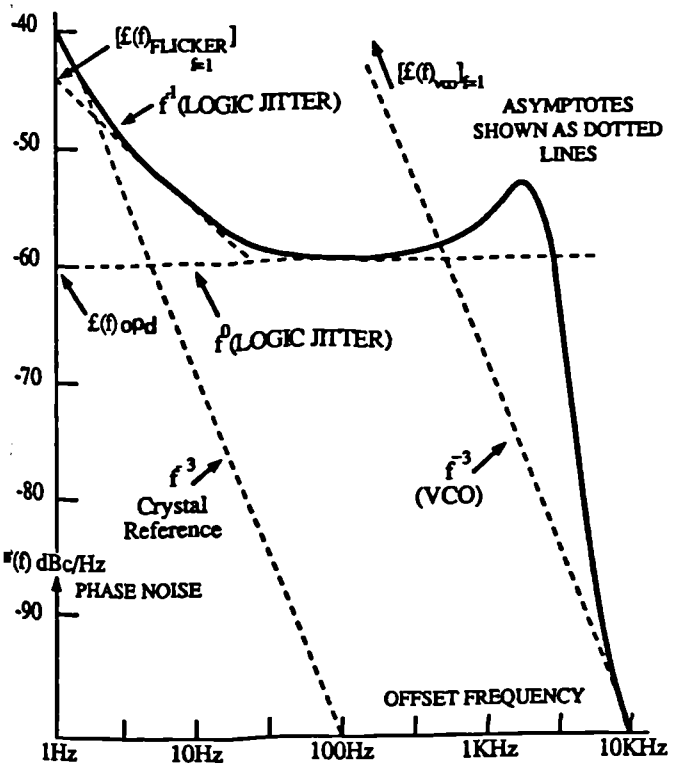


Figure 4 Typical phase noise asymptotes for single loop synthesiser

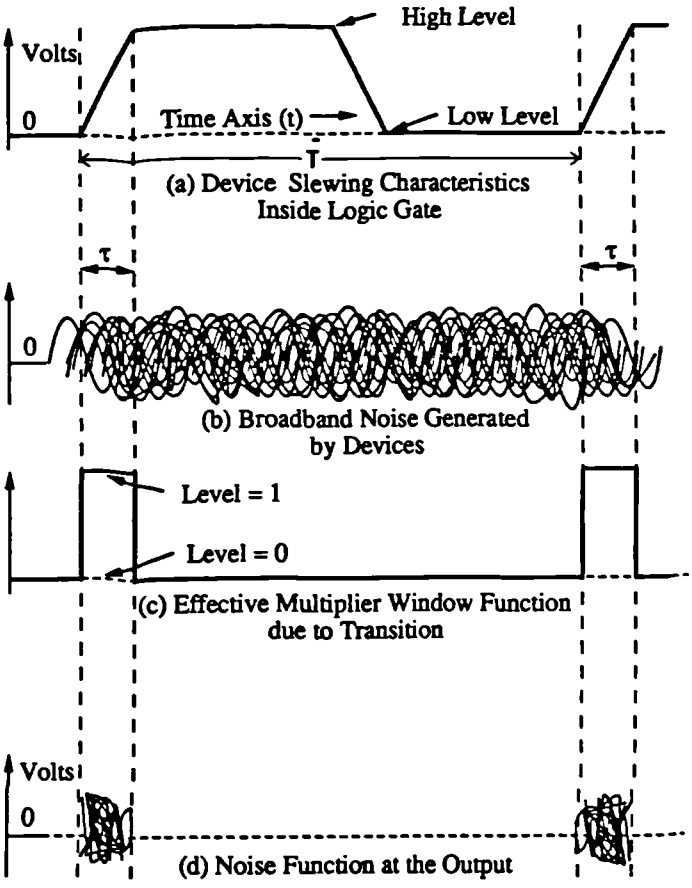


Figure 5 The effect of noise generated in a logic gate

THE EFFECT OF LOCAL OSCILLATOR PHASE NOISE IN LOW DATA-RATE SATELLITE RECEIVERS

M. P. Wilson & T. C. Tozer

1. Introduction

The development of Very Small Aperture Terminals (VSATs) is leading to critical appraisal of the origins and effects of phase noise within modems. Because of their small antenna gain and associated low carrier-to-noise density, these terminals operate at a low data-rate (typically no higher than 64 kbit/s, and often considerably less); this places stringent requirements particularly upon the phase noise produced by receiver downconverter local oscillators, which must be not only low cost but frequency agile for flexible channel assignment.

Very inexpensive synthesised satellite receivers are becoming readily available, as a result of the mass production of consumer television receive-only (TVRO) systems. However, although these may provide a satisfactory noise figure, they are frequently unsuitable for use in low data-rate communications due to their poor close-to-carrier phase noise.

The origins of phase noise in single-loop synthesisers are outlined here, and the effects of oscillator phase noise and thermal phase noise upon data demodulation are identified, together with the conflicting requirements placed upon the receiver's carrier recovery loop. Some design criteria and parameters are outlined, and performance illustration given for the implementation of a VSAT receiver.

Figure 1 illustrates a typical receiver outline. Two or more stages of downconversion may be employed, (eg from a signal at 14 GHz to IFs at 1 GHz and 70 MHz). Data modulation with BPSK is considered here, although the principles may be extended in general to QPSK. The carrier recovery loop (CRL) is taken to be a squaring loop, or equivalently a Costas Loop, employing a phase-locked-loop (PLL).

2. Synthesisers and Phase Noise

(a) Architecture

The usual, and the most economical, synthesiser implementation for VSAT downconverters is the single PLL method. In order to maintain a fine frequency resolution over a large frequency range, a number of stages may be required. Each stage has its own loop synthesiser, with the higher local oscillator frequencies coarse stepping and the lower frequency oscillators fine stepping. Figure 2 shows the architecture of a single loop synthesiser; the loop consists of dividers and an edge triggered phase-frequency comparator.

The typical phase noise spectrum of such a synthesiser is displayed in Figure 3 , and comprises a number of distinct regions. The f^{-3} region closest to the carrier is due to crystal resonator noise (multiplied up to the final output frequency). The f^{-1} and f^{0} regions arise from the active devices employed in both the phase-frequency comparator (and associated dividers) and the loop filter. The outer f^{-3} region represents the free-running VCO phase noise.

There appear to be several phenomena giving rise to the f^{-1} flicker noise in logic circuits, and this subject is felt to be an area worthy of further investigation. The transition from the f^{-1} region to the white noise floor (f^{0}) region for the logic jitter increases in frequency as the phase comparison frequency is increased. With CMOS comparators at a 25 kHz comparison frequency, for example, this transition point is approximately 50 Hz from carrier.

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The phase noise contribution from the loop filter itself (eg op amp components) can be minimised with careful design. However, the jitter from the comparator and associated logic circuitry will remain as the principal contributor to the phase noise; this is exacerbated because the phase comparison in the synthesiser is often accomplished at a low frequency. The jitter may become a significantly large fraction of a radian when translated to the output frequency in the microwave region.

(b) *Vibration & Microphony*

In addition to static phase noise, vibration also creates phase uncertainties within the oscillators. The reference crystal oscillator vibration appears at the output modified by the transfer function H(s) of the synthesiser phase locked loop. The synthesiser VCO microphony contribution, generally the predominant component[1], is modified by the error function E(s) of this PLL. For a second order type one PLL this error function is determined as follows[2]:

$$|E(s)|_{synth} = \left(\frac{\frac{\omega^4}{\omega_n^4} + \frac{\omega^2}{K^2}}{1 + (4\zeta^2 - 2)\frac{\omega^2}{\omega_n^2} + \frac{\omega^4}{\omega_n^4}} \right)^{\frac{1}{2}} \quad \text{...(i)}$$

$$\text{where} \quad E(s) = 1 - H(s) \quad \text{...(ii)}$$

Here ω_n is the loop natural frequency, ζ is the damping factor, and $K = K_{amp}K_{pd}K_{vco}/N$, where K_{amp} is the loop amplifier gain, K_{pd} is the phase detector gain, K_{vco} is the VCO gain, and N is the division ratio of the synthesiser dividers. When $\omega << \omega_n$, the denominator $\rightarrow 1$. For a second order type two loop, K effectively $\rightarrow \infty$, and the term $\omega^2/K^2 \rightarrow 0$.

In order to minimise $|E(s)|_{synth}$, it is necessary to maximise ω_n and K. The maximum value of ω_n depends on the reference frequency chosen, for a single loop synthesiser. Traditionally the value of ω_n is determined by the requirement to equalise the reference and VCO contributions to the output phase noise[3]. The requirement upon ω_n for vibration performance can increase its value away from this point, increasing the contribution of reference phase noise. Although the value of K would make little difference to the static phase noise, it can have considerable influence on the vibration performance. This is as a result of the effect on the value of $|E(s)|$ at low frequencies.

For a second order type two loop, $K = \infty$ and $|E(s)|$ decreases at 40 dB per decade with reducing frequency below ω_n. For a type one loop, an open loop pole exists at $\omega_p = \omega_n^2/K$ and it can be observed from eqn (i) that below this point $|E(s)|$ decreases @ 20 dB per decade. The suppression of low frequency vibration in the VCO would be less than anticipated in this case. The problem would be exacerbated in a loop with large division ratio N, as can be observed from the expression for K, above, due to the finite DC gain of the loop amplifiers.

(c) *Choice of Logic Technology*

The mechanism for the generation of phase noise within logic circuitry has many sources[4], and it can be difficult to determine its value. However, it is possible to predict the phase noise levels for a particular phase detector logic technology and configuration, based upon observed measurements at a single frequency. This analysis is outlined below.

At the input stage of a logic gate, broadband noise is present up to an effective cut-off frequency determined by the input device and its technology, and this can be very high (eg 5 GHz) for TTL and ECL. This broadband noise will only contribute during the switching transition time τ, which occurs once per cycle at the synthesiser comparison frequency f_c (=1/T). The output noise spectrum may be expressed from consideration of the product of the input noise with a window function which is unity during time τ, and zero elsewhere.

Let the input noise power spectral density be γ_i (watts/Hz). The effective duty cycle for which the noise is effective is τ /T, and hence the output noise power spectral density is proportional to $\gamma_i \tau / T = \gamma_i \tau f_c$.

It is clear from the above that the phase noise is reduced as τ is diminished. This can be achieved with high speed logic with fast transition times, provided that γ_i is otherwise unchanged. The close-to-carrier phase noise at the synthesiser output will be contributed by several gates in the synthesiser loop. This phase noise will be multiplied up from the comparison frequency f_c to the output frequency f_{out}.

The phase noise contributions from each logic gate will add. Representing the normalised phase noise power-density (from the output of the phase detector) as $\mathcal{L}(f)_{opd}$, and the oscillator output power as C, then:-

$$\mathcal{L}(f)_{opd} \propto \frac{\gamma_i \tau f_c}{C} \left(\frac{f_{out}}{f_c}\right)^2 \qquad \text{...(iii)}$$

This result will also be subject to the transfer function of the synthesiser loop filter, $H(s)_{syn}$.

The overall phase noise will manifest itself as BER degradation in the receiver, determined by the CRL in the demodulator as outlined previously. It is therefore necessary to arrange to have as few active gates as possible in the synthesiser loop, and effectively reduce them in number through re-synchronisation techniques.

With the above relationship, it is possible to predict the synthesiser output phase noise for a particular output frequency and comparison frequency, with a given configuration and logic technology. Representing the logic contribution to the phase noise floor (f^0 region in Figure 3) as $\mathcal{L}(f)_{opd}$ dBc/Hz, then:-

$$\mathcal{L}(f)_{opd} = K_n + 20 \text{ Log } f_{out} - 10 \text{ Log } f_c \quad \text{dBc/Hz} \qquad \text{...(iv)}$$

where K_n is a constant determined by the configuration and logic technology used,.

Based on measurements taken, the following values for K_n were determined for a typical single loop synthesiser with commonly used edge-triggered phase-frequency comparators:

K_n =
- 200 dBc/Hz for fast CMOS
- 205 dBc/Hz for ECL and low-power Schottky TTL
- 215 dBc/Hz for Fast series TTL.

(CMOS using MC145151, ECL using 10,000 series, LS series TTL, and 74F series TTL respectively).

The range shown here of 15 dB can be very significant in terms of resulting system performance. It is worth noting that although ECL has a fast switching speed, this advantage is offset by a high level of input noise γ_i. These results are supported independently by Utsi[5].

3. Effects of Phase Noise on Demodulator Design

(a) *Bit Error Rate Degradations*

The combination of thermal noise (N_0) and additional phase jitter each give rise to degradation of BER. The jitter is manifest differentially at the inputs to the demodulating multiplier, and has variance σ_T^2 (radian^2). It is due to two effects:

(i) Phase noise appearing differentially between the signal input and the CRL output: the difference arises because the CRL does not totally track the phase jitter arising from the downconversion synthesiser(s);

(ii) Thermally-derived phase noise appearing on the recovered carrier, which is not coherent with the signal input thermal noise by virtue of the effect of squaring circuit within the CRL.

It is clear that errors will occur as σ_T approaches the phase distance between symbols, and that the situation becomes more demanding for QPSK and higher orders of modulation. (In practice, the performance may be further aggravated by non-linearities and cycle slips at low carrier-noise levels within the CRL).

The receiver designer has to face a trade-off in parameters for the CRL, which requires a wide loop bandwidth to track local oscillator phase noise and a narrow loop bandwidth to minimise thermal noise effects. Further design constraints may be imposed by acquisition and Doppler tracking requirements.

(b) *Oscillator Phase Noise*

Synthesiser or oscillator phase noise is introduced at each stage of down-conversion in the receiver, and the phase noise jitters will add on an RSS basis. (It cannot be assumed that the contributions from each stage will be the same, and one may expect significantly greater phase noise from the higher frequency source, at say 12 GHz). Such local oscillator phase noise is not substantially decorrelated by the squaring circuit[6].

The phase noise power-density to carrier power ratio $L(f)$ can be determined for each oscillator. The resulting differential jitter at the inputs to the demodulator is given by:-

$$\sigma_p^2 = \int_{f=0}^{f=f_d} 2L(f)\ |[E(s)]^2|_{CRL}.df \qquad (\text{radian}^2) \qquad \ldots(v)$$

where $E(s)$ is the error function of the CRL (= 1 - $H(s)$), and f_d is the data rate, as a practical upper limit of integration. The total phase noise derived differential phase jitter σ_{pRSS} is then the RSS of the several values of σ_p derived above.

The form of $L(f)$ is very much dependent upon the particular synthesiser and its architecture, and there is no universally applicable result for this function.

In order to minimise σ_p^2, $|[E(s)]^2|_{CRL}$ should be made as small as possible, which implies $[H(s)]_{CRL} \rightarrow 1$, and hence the carrier recovery PLL natural frequency ω_n chosen to be high[3]. This conflicts with the thermal noise requirement upon ω_n, as detailed below.

(c) *Thermally-derived Phase Noise*

Besides the direct impact upon E_b/N_0, additive thermal noise gives phase jitter which is modified by the CRL, which is unable to fully track it. This gives rise to a differential input to the demodulator multiplier, and degradation of the BER.

If the level of noise within the CRL bandwidth is high, then non-linear effects such as the addition of orthogonal amplitude modulation components of the noise also become significant. Cycle slipping also becomes a problem at low carrier-to-noise levels: in order to minimise cycle slipping, a high damping factor ζ in the CRL is desirable, and a value of 1·3 is generally chosen[7,8].

The squaring function within the CRL gives rise to the product (noise) × (signal), which has a low correlation with the thermal noise additive upon the data signal. This decorrelated noise is subject to the CRL transfer function H(s). The performance can be analysed in terms of the CRL parameters, including the shape of the pre-squarer bandpass filter. For the particular case of a Gaussian pre-squarer BPF of bandwidth B_p[9], it can be shown with some analysis that the additional jitter due to thermal noise, σ_t, can be related to ω_n as follows:-

$$\sigma_t^2 = \frac{3\,\omega_n}{4}\left(\frac{B_p}{\sqrt{2}}\frac{N_o}{C} + 1\right)\frac{N_o}{C} \qquad \text{...(vi)}$$

With a given allowance for σ_t^2, ω_n may then be chosen. It is seen that a small ω_n is required, and thus a compromise is necessary between that value of ω_n required to minimise thermal noise phase jitter, and the tracking requirements due to local oscillator phase jitter.

4. Design Example

The total phase noise produced by the synthesiser can be represented in terms of the f^0 floor $\mathcal{L}(f)_{opd}$, f^{-1} flicker noise region (closest to the carrier in Figure 3), and the VCO phase noise (f^{-3} region). The synthesiser normalised phase noise power-density can be expressed as:-

$$\mathcal{L}(f)_{opd} = \left|H(s)_{syn}\right|^2\left(\mathcal{L}(f)_{opd} + \left[\mathcal{L}(f)_{flicker_{f=1}}\right]\frac{1}{f}\right) + \left|1 - H(s)_{syn}\right|^2\left[\left[\mathcal{L}(f)_{vco_{f=1}}\right]\frac{1}{f^3}\right] \qquad \text{...(vii)}$$

Here $\mathcal{L}(f)_{opd}$ is the phase noise contribution of the logic jitter, and the subsequent term represents the flicker noise normalised to that at 1 Hz offset from carrier. $\mathcal{L}(f)_{vco_{f=1}}$ is the VCO phase noise extrapolated to 1 Hz offset, and $H(s)_{syn}$ is the synthesiser PLL transfer function.

The above criteria are illustrated by a synthesiser having a 2 GHz output frequency, and using CMOS logic with a phase comparator operating at 50 kHz. The contribution to the output phase noise from logic jitter, $\mathcal{L}(f)_{opd}$, is then -61 dBc/Hz, from equation (iv). The synthesiser is observed to have a VCO phase noise of -40 dBc/Hz at 1 kHz offset.

The receiver operates at a data rate of 40 kbit/s and E_b/N_0 of 6 dB, with half-rate Viterbi decoding. A value of σ_t is chosen initially to obtain a suitable compromise between BER degradation and the acquisition time of the CRL. The CRL employs a Gaussian pre-squarer filter with B_L = 200 kHz, ω_n = 31 Hz and ζ = 1.3. The above parameters may be typical of a VSAT modem.

The following demodulator jitter figures result:

σ_t thermal jitter	=	6.0°
σ_p phase noise jitter	=	10.7°
σ_T RSS total jitter	=	12.3°

In practice several iterations of the calculation may be performed in order to find the value of CRL ω_n that gives the lowest value of σ_T. As may be observed from the BER curves (Figure 4)[10], the above parameters produce a degradation of about 2 dB in a BPSK system, and would have a very significant effect upon a QPSK or higher order modulation system.

The use of Fast TTL logic instead of CMOS in the synthesiser would result in a lowering of σ_p to 4.9°, giving a reduction in σ_T to 7.8°. Negligible degradation would then ensue for BPSK, although there would still be severe degradation for QPSK. These results imply that the present generation of low-cost single chip CMOS synthesisers have severe limitations for low data rate downconverters.

5. Conclusions

Phase noise is a significant parameter in low data-rate modems for VSAT applications. Both thermal noise and phase noise from synthesisers affect demodulators employing a carrier recovery loop, giving degradation of BER performance. Each places conflicting demands upon loop bandwidth of the CRL.

Single loop synthesisers are simple and attractive as downconverter local oscillators, but their phase noise can be excessively large for data receivers. It is possible to predict levels of phase noise from given configurations as a function of the logic technology employed. Synthesiser phase-frequency detectors may be critical design components, and some low cost synthesiser designs may prove inadequate in this respect to meet receiver BER requirements.

Vibration and microphony need to be taken into account, in addition to static phase noise.

6. References

[1] Payne, John B., "Cost Effective Synthesiser Design" Microwaves & RF, June 1984, p 89.

[2] Blanchard, A., "Phase locked loops and their application to coherent receiver design". J Wiley & Sons 1976. Chap 6, p 105

[3] Robins, W.P., "Phase noise in signal sources". Peter Perigrinus 1982. Chap 7 p 94

[4] Robins, W.P., "Synthesiser phase jitter contributed by TTL and ECL components". Proceedings IEE Colloq on "Low Phase Noise Oscillators & Synthesisers", 23 January 1986.

[5] Utsi, P.A.V., "Phase noise in digital PLLs due to detectors and dividers". Proceedings IEE Conf. on "Land Mobile Radio", Leeds, March 1983.

[6] Wilson, M.P. & Tozer, T. C., "Synthesisers for low data-rate satellite receivers". Proceedings IEE Conf. on "Frequency control & synthesis", Leicester, May 1989.

[7] Ref [2], Chap 12, p 323

[8] Ref [3], Chap 10 p 251

[9] Oberst, J.F. & Schilling, D.L, "The SNR of a frequency doubler". IEEE Trans Comm. Technology. Feb 1971 pp 97 - 99

[10] Holmes, J.K., "Coherent spread spectrum systems". J Wiley & Sons 1982. Chap 6, p284

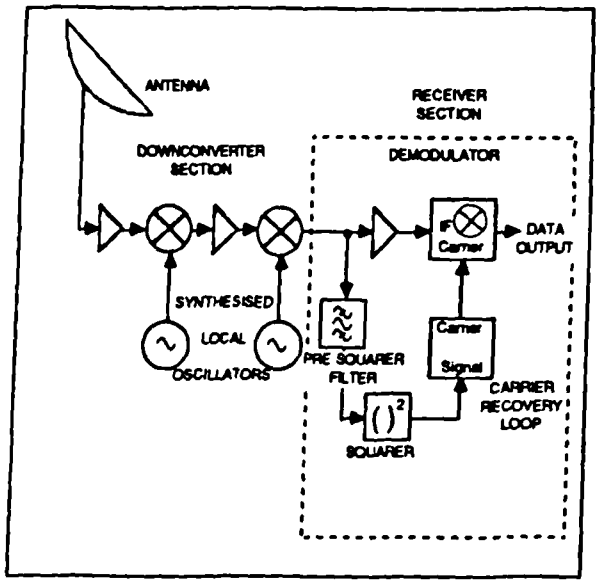

Figure 1 Simplified outline of VSAT receiver

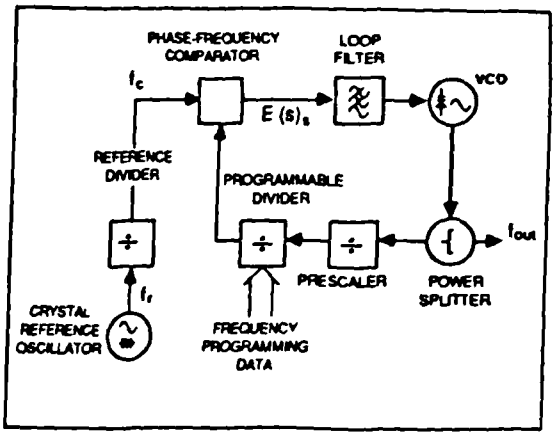

Figure 2 Single loop PLL synthesiser

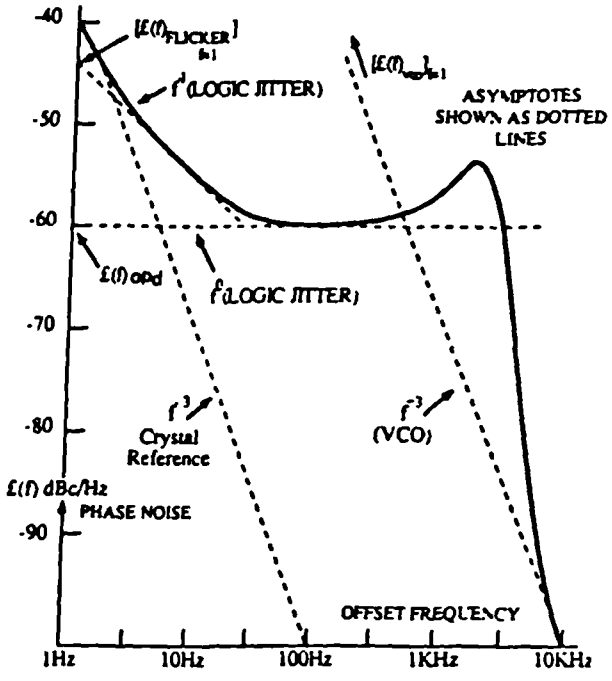

Figure 3 Typical phase noise asymptotes for single loop synthesiser

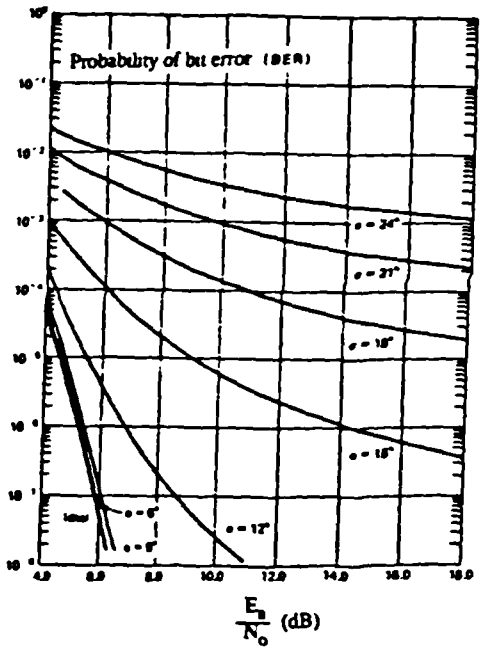

Figure 4 BER as a function of E_b/N_0 and phase jitter. (From [10]. 3° static phase error, 1/2 rate Viterbi decoding)

BRITISH PATENT APPLICATION

FCSL013

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Title: SIGNAL GENERATION USING DIGITAL-TO-ANALOGUE CONVERSION

Application No:

Filing Date:

SIGNAL GENERATION USING DIGITAL-TO-ANALOGUE CONVERSION

This invention relates to the generation of continuous analogue signals from repeated application of digital numbers to digital-to-analogue conversion means and in particular to mitigation of the effects of distortion in such analogue signals caused by the digital-to-analogue conversion means.

The invention is particularly, but not exclusively, concerned with the generation of analogue signals at specific frequencies, so-called frequency synthesis, and mitigating the production of spurious frequencies inherent in such analogue signal distortion.

The invention may be applied to so-called direct digital synthesis, in which the digital-to-analogue conversion means delivers an analogue signal of appropriate frequency, and to phase locked loop synthesis, in which in a phase locked loop, incorporating a voltage controlled oscillator, a circuit controlling loop phase error incorporates digital-to-analogue conversion means in a manner similar to direct digital synthesis.

The basic form of direct digital synthesiser with which the invention is concerned is illustrated at 10 in Figure 1 and comprises a system clock 11, a digital number generator 12 which provides a number, conventionally identified as K, representing the frequency to be synthesised, an accumulator 13 to which the number is added at each system clock cycle to provide a series of "phase" numbers increasing linearly with time and a digital function generator 14, such as a read only memory (ROM), which defines the form of the signal to be generated, for example sinusoidal, as a further series of numbers. All the numbers are formed as digital binary words and a digital-to-analogue converter (DAC) 15 generates a series of analogue values corresponding to the numbers represented by the words which in time define the signal having a waveform defined by function generator 14 and at a frequency defined by the value of number K. The output of the DAC 15 may be passed by way of an anti-aliasing filter 16.

It is convenient to, and at times this specification will refer to, numbers synonymously with the digital binary words representing those numbers unless the context of the description makes it more appropriate to consider the structure of the words themselves.

Such basic form of direct digital frequency synthesiser and modifications thereto are described in UK Specification No. 2121627B.

It is also a feature of such basic form of direct digital frequency synthesiser, and also described in the above referenced UK patent specification, that the analogue signal generated is not confined to the desired frequency represented by number K but it also accompanied by unwanted spectral components or spurii attributable to DAC operation. Furtheremore if truncation of the digitial word length is required for any component, such truncation also adds spurious spectral components, although dominated by those related to the DAC.

Spurious generation in the DAC may be due inter alia to differential non-linearity, switching transient errors and quantisation errors. Switching transient errors manifested as energy present at the DAC output are particularly troublesome with synthesisers having a high clock speed able to operate at high clock speeds used to generate high frequency signals.

It has been proposed to use a high speed sample-and-hold device to the output of the DAC to remove switching transients by sampling only after the DAC has settled for each input word. However, in generating high frequencies, the duration of each output level may be shorter than the settling time of the DAC so that even high speed sample-and-hold devices, which may themselves introduce an unacceptable cost penalty, may be unable to satisfactorily remove switching transients.

It has also been suggested in US patent specification No. 4410954 to avoid the problems caused by DAC use by omitting the function generator and DAC. However, the elimination of the DAC results in low overall signal-to-noise ratio and phase noise sidebands unacceptable for most communications systems or

where frequency hopping is required.

In order to address the error mechanisms due to DAC operation the above mentioned UK patent No. 2121627B identifies that the high levels of spurii arise from correlation of errors due to repetition of an error at a particular DAC step each time a particular word is output from the function generator. That specification proposes to relieve the effect by 'randomising' the digital-to-analogue conversion by control of the DAC whereby for any particular phase numbers produced by the accumulator the DAC response to the function generated is pseudo-randomly varied to try to spread the hitherto correlated narrow-band spurii at frequencies close to the sought frequency across the frequency band as wide-band noise.

Several arrangements are proposed therein but all are restricted to being a random choice between two sets of devices having slightly different chacateristics and are believed to provide insufficient relief for use in generating very high signal frequencies that in practice require system clock frequencies in the GHz range and high rates of frequency changing.

One form of the 'randomising' proposed comprises the use of two DACs with switching means randomly placing one DAC or the other in circuit. If each is responding to the same digital function generator word the DACs must operate with ostensibly the same characteristics and randomisation is due only to the actual differences which exist between nominally identical devices. If each DAC is paired with an individual function generator then the DAC and/or its operating reference can be adjusted to provide considerably different error response than the other. However, there is a limit to how different from each other the DACs can be whilst accurately converting the principal signal and with any selected pair of devices the randomness is confined to a band representing the difference in their characteristics. Furthermore, there is the need to provide switching which may prove difficult to engineer for generating very high frequencies without also introducing undesirable transient energy effects.

As an alternative to switching between different DAC devices that patent proposes to use a scaling DAC with randomly varied scale control and DAC reference. Although the switching is absent a multiplying DAC is required which cannot operate as fast as a fixed reference DAC and is unsuitable for generating very high frequencies.

Single phase-locked loop frequency synthesisers are also well known per se, the loop oscillator frequency being controlled by phase comparison of a reference frequency and one provided by division of the oscillator output frequency by a number N, the resultant phase difference drifting until at a phase angle 2π with respect to the reference frequency it self-corrects with a repetitive phase jitter characteristic of such circuits. Any VCO phase jitter due to other sources can be corrected provided they are within the loop bandwidth. The frequency division is performed in a digital counter circuit and by definition the number N is an integral and the smallest frequency interval that can be generated, or frequency resolution, is limited by the integral number step and the reference frequency. Achieving a high frequency resolution by means of a low reference frequency is not always practicable as it requires a small loop bandwidth and results in slow loop response, conflicting with requirements of high loop speed and wide bandwidth for noise rejection.

It has become common practice to avoid the conflict by effectively introducing fractions of the integer N, by so-called fractional-N synthesis. In this technique the divider is switched at intervals from divide-by-N to divide-by-(N+1) for a cycle of the reference frequency signal, the interval being determined in accordance with what is in effect the integral of a fractional frequency instruction, also usually defined by a digital number. The integration takes place in a digital accumulator, overflow of which effects the aforementioned one cycle change of divisor from N to (N+1), but although simple in concept, it suffers a drawback in that alteration of the divisor results in additional phase

perturbations or jitter. Because such additional perturbations are directly related to the residual content of the overflowed accumulator, the effect can be mitigated by deriving an analogue representation of this residual content in a digital-to-analogue converter (DAC) and either injecting it into the loop at the output of the phase comparator or applying it to a phase modulator which restores the phase of the divided VCO signal applied to the phase comparator. Such a configuration is illustrated schematically in Figure 11 and described in more detail hereinafter.

It has been suggested that mitigating this additional jitter by such analogue signal is only practicable when the phase detector is operated at frequencies significantly below its potential maximum. This is due, at least in part, to non-linearity of the DAC and repeated use of DAC steps.

It will be appreciated that the source of the number representing the fractional frequency instruction, or alternatively stated, the desired oscillator output frequency, the accumulator and DAC comprise the elements of a direct digital synthesiser substantially as described above but which, by virtue of its direct connection between linearly increasing accumulator output and DAC, generates over a period of time an analogue signal having a sawtooth waveform.

Notwithstanding the specific nature of the circuits described above for generating signals of specific frequency, it is an object of the present invention to provide a method of mitigating effects of distortion on an analogue signal derived from repeated application of digital numbers to digital-to-analogue conversion means and a circuit arrangement for generating an analogue signal in which such effects are mitigated. Further objects of the invention relate to the provision of specific direct digital frequency synthesis and phase locked loop synthesis circuit arrangements.

According to a first aspect of the present invention a method of reducing the effects of distortion in an analogue signal derived by repetitively accumulating digital numbers as a function of time and subjecting the results of accumulation,

representing phase of the analogue signal, as phase related numbers to digital-to-analogue conversion, comprises the steps of producing digital random or pseudorandom numbers (as herein defined) in synchronism with the accumulation of phase related numbers, modifying values of phase related numbers in accordance with the values of the random numbers, applying the randomly modified phase related numbers and the random numbers to conversion means so as to derive analogue values directly related thereto and combined in such a manner as to eliminate the effect of the random numbers from the analogue signal derived as a function of time from the analogue values.

The method may be applied to the synthesis of analogue signals having particular frequencies defined by the digital numbers, in particular to so-called direct digital synthesis (DDS), by combining analogue values resulting from conversion, and phase locked loop synthesis (PLLS) by utilising the analogue values resulting from conversion in loop phase correction.

In accordance with a second aspect of the present invention a circuit arrangement for deriving an analogue signal comprises system clock means, a digital frequency number generator responsive to the system clock means to generate in each clock cycle a digital number representative of the frequency of a signal to be generated by the arrangement, a digital accumulator operable repetitively to accumulate to a predetermined total digital frequency numbers generated as phase increments of the signal and to provide each new total as a phase number representing the current signal phase value, means responsive to a phase number to provide a digital function number representative of an amplitude value of the signal to be generated at the current phase value, random or pseudorandom (as herein defined) digital number generating means, arithmetic logic means operable to modify at least some digital function numbers each by a generated random digital number, and conversion and combining means responsive to digital numbers provided by the arithmetic logic means and by the random digital number generating means to derive and combine in the analogue domain signal values directly dependent on said digital number

ABSTRACT

SIGNAL GENERATION USING DIGITAL-TO-ANALOGUE CONVERSION

A circuit for generating an analogue signal by way of digital-to-analogue conversion, such as a direct digital frequency synthesiser (Fig. 3) of the type including a frequency number generator 12, phase number accumulator 13, function number generator 14, such as a look-up table of sine values, and DAC 15 mitigates the production of analogue signal errors, manifested as spurious frequency signals, by modifying the digital number representing each function value with a random digital number added or subtracted in ALU 22. The randomly modified function number and random digital number are converted to analogue values in DAC 15 and further DAC 28 respectively and the analogue values combined to remove the effect of the random number. Because conversion in DAC 15 is spread randomly over all DAC levels, even when the function number is not, any conversion errors associated with any DAC steps which by repeated use would be manifested as spurious frequency signals are decorrelated to broadband noise. Less troublesome correlations due to function number truncation may be mitigated by limited random dithering of the phase number (Fig. 6) and randomly dithering rounding of the function number (Fig. 5).A similar circuit (110, Fig.10) generating a sawtooth signal may be employed in improving phase control linearity in a phase locked loop frequency synthesiser.

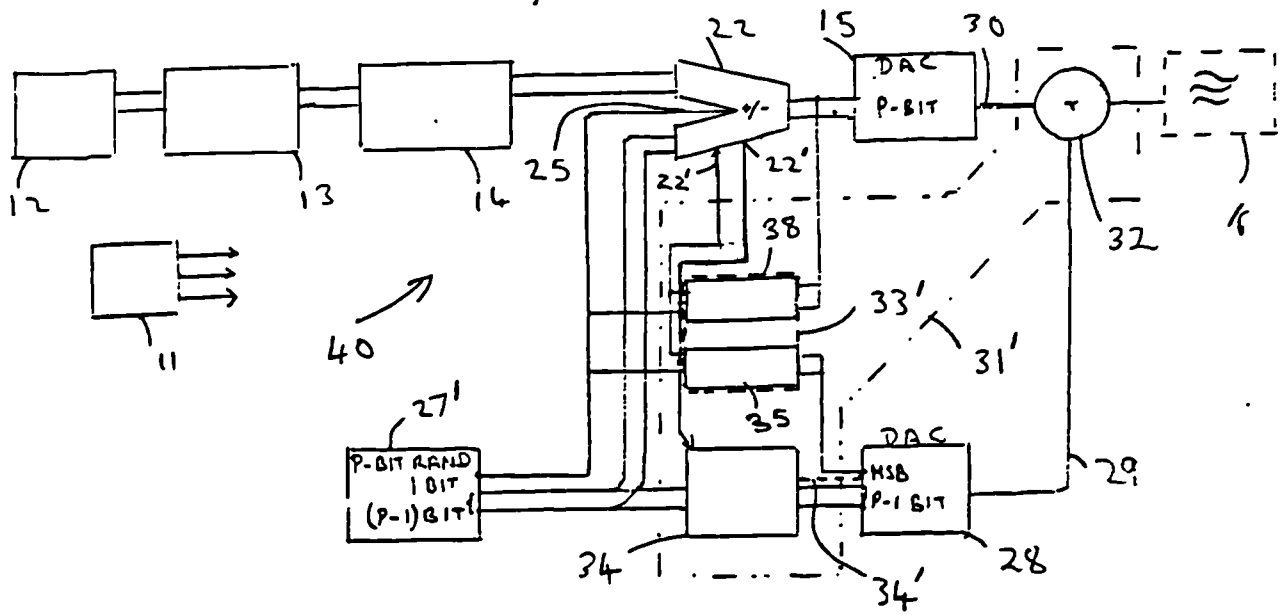

FIG 4

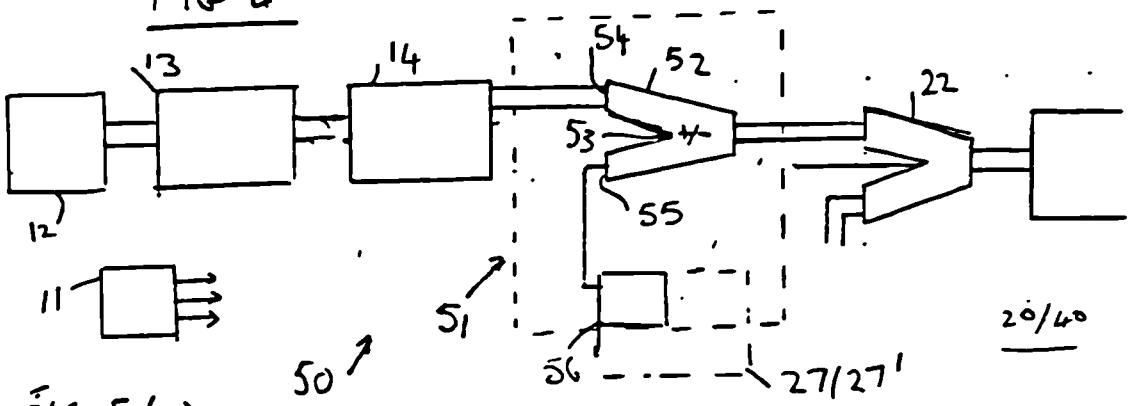

FIG. 5(a)

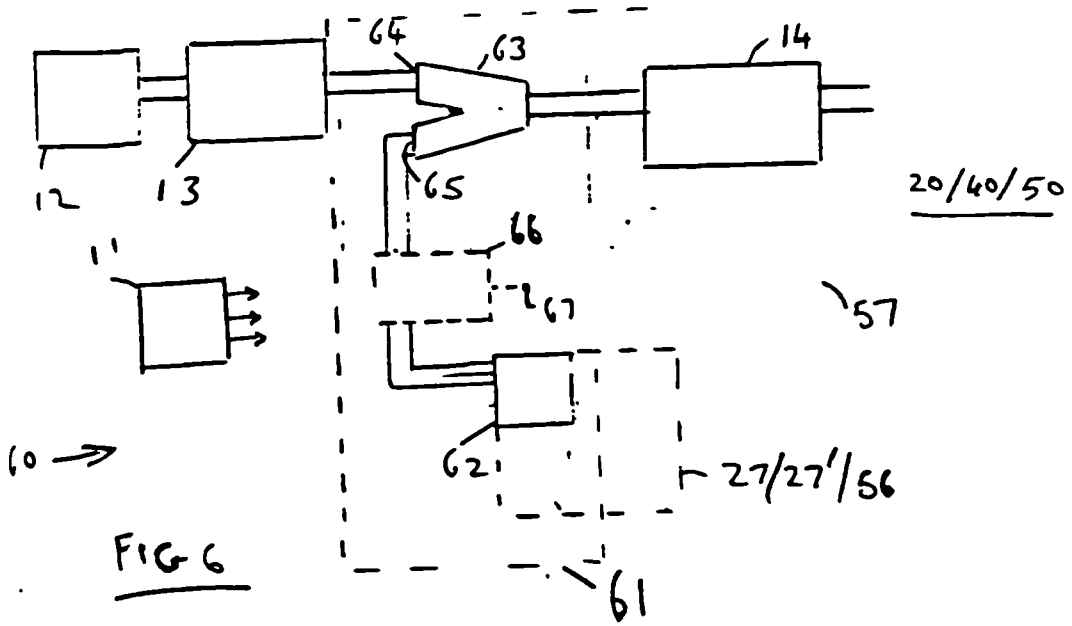

FIG 6

COMPUTER SIMULATION OF SRDiode COMB GENERATORS

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Abstract

This paper examines the performance of Step Recovery Diodes used as frequency comb generators. A model is produced and a computer simulation derives the circuit behaviour. The resulting Phase Noise performance is analysed and it is shown how the performance of such comb generators can be chaotic.

1 Introduction

1.1 The step recovery diode as a means of frequency multiplication

In order to generate stable microwave signals at frequencies around 30GHz some form of frequency multiplication must be employed. There are many methods of frequency multiplication, with varying levels of implementation difficulties and phase noise performance. One useful such implementation involves a Step Recovery Diode (SRD).

The step recovery diode can be embedded in either a comb generator or a frequency multiplier. In a comb generator, the abrupt pulses across the diode are connected directly to the output. Such narrow pulses result in a large series of harmonics of steadily decreasing level, known as a comb. Fig 1a displays a typical local oscillator configuration comprising crystal reference oscillator and comb generator. In a Multiplier, an idler circuit (resonant circuit allowing a signal path) at the desired output frequency allows all harmonics to mix together within the diode, resulting in concentration of signal power at this frequency.

SRDs are well covered in the literature, particularly with reference to frequency multipliers [1,2,3,4]. Large value frequency multiplications are possible within a single stage as a result of an abrupt non-linear SRD transfer characteristic. Good noise performance is possible due to the simplicity of the circuit and high signal levels. Published work on the stability and noise performance of SRDs is scarce; however, the comb generator must be correctly designed to optimise the noise performance, particularly when the drive frequency is low.

We will show that this abrupt non-linearity is also responsible for period doubling chaos which can result in unstable operation. We have observed that an apparently normally operating comb generator can suddenly display high phase noise or instability as a result of a change of external parameters such as power supply voltage or temperature. We will demonstrate how this can occur with the aid of a Feigenbaum diagram.

1.2 Phase noise in SRD circuits

With conventional methods of frequency multiplication which use a single oscillator as the source, the phase noise at the input is increased by a factor $20\log(f_{out}/f_{in})$ at the output at a constant offset from carrier frequency [5]. Unless the noise sidebands become so great that the small angle criterion is violated, the spectral profile will remain unchanged. The above ratio represents the best that can be achieved with a noise free multiplier. In practice there will be additional noise internally generated from the multiplier, known as "excess noise" [6].

In the past, the phase noise contribution of crystal oscillator sources tended to dominate the noise from multipliers, and the above model was sufficient. However, more recently, there have been requirements for stable signal sources at frequencies to above 100GHz. While the quality of reference source oscillators has much

improved, the excess phase noise of the comb generator or frequency multiplier can no longer be considered negligible.

2 Step Recovery Diode.

2.1 The case for modelling

The comb generator can be represented by a second order non-linear differential equation and a forcing function. An analysis of the comb generator is compounded by the fact that solving the differential equation can result in 3 separate solution sets [7]:-

1) Frequency generation at harmonics of the driving frequency (the forcing function);
2) Frequency generation at subharmonics of the driving frequency, and at their harmonics (parametric oscillation);
3) Chaotic operation (spectral break-up).

For a harmonic comb generator, only the first case is desirable. We will also show that, at the boundary between solutions, an increase in phase noise is possible.

The situation is further complicated by the parameters that are capable of influencing the output, viz:-

1) Drive level;
2) Forcing function;
3) Bias level;
4) Diode carrier lifetime;
5) Choice of circuit components.

As a result of the complexity of the problem we decided to consider computer modelling of the circuit. Linear analysis packages commercially available do not cater for SRDs and cannot be adapted to calculate phase noise. A computer program

that accomplishes a non-linear simulation of the SRD impulse generator is described. This was written in PASCAL, and implemented on a PC.

2.2 The SRD model

The step recovery diode has a doping profile as displayed in fig 1b, and the capacitance-voltage characteristic is as displayed in fig 2. During the forward conduction phase, charge carriers are injected into the depletion region and the diode displays a very low on resistance. When the drive voltage reverses the carriers are swept out of the intrinsic (I) region; while carriers are being removed from the I layer, the diode will then continue to display a low impedance. Upon removal of all these carriers, there is an abrupt seizure of diode current, which results in the diode entering the high impedance reverse bias mode. The diode then displays the reverse biased junction capacitance C_d. A change in the current flow of up to 10^9 amps per second is a consequence of the impedance switch. Any inductance results in large voltage spikes as in fig 3, and spectral energy will be generated at frequencies of greater than 100GHz as a result of the spikes. Large multiplication ratios can therefore be performed in a single step, a most important property of an SRD circuit. Fig 3 displays the waveforms of the SRD comb generator.

There are two parts to the cycle, the conduction phase and the impulse phase. In the case of the latter phase, a damped resonant circuit is formed by the drive inductance, diode capacitance, and load resistance. Ringing of the output voltage commences as shown in the top half of fig 3. If the diode remained in the intrinsic state, then the output voltage would continue to ring as shown by the dotted line. As soon as the forward barrier voltage of the diode is exceeded however, the diode begins to conduct. As a result of the very low on resistance of the diode, the ringing waveform becomes severely overdamped, giving a very slow decay of the SRD voltage after this point. A critical factor in determining the phase noise

characteristics of the comb generator is the conduction angle α; this is the angle between the reversal of the input drive voltage and the start of the impulse phase.

3 SRD Simulation program

3.1 Description

A time domain simulation is carried out which is split into conduction and impulse phases. The two are separated by a boundary condition related to carrier storage within the device. The conduction phase continues while carriers are present in the intrinsic layer, whereas the impulse phase begins when all carriers are removed from the intrinsic layer. Fig 4a shows a circuit diagram of the comb generator where inductor L_d provides the impulse when current flow is interrupted by the SRD.

3.2 Conduction phase

Conduction analysis commences when the SRD is forward biased, and finishes when all the charge carriers are swept out of the intrinsic layer. Fig 4b shows the model used for the conduction phase. The diode equivalent circuit consists of a resistor representing the junction bulk resistance in series with a battery representing the barrier potential of the SRD junction. External components include the impulse inductance L_d and the source resistance R_{source}. The elements L_∞ and R_{bias} are used for developing the self bias.

At each small increment in time Δt, voltage and current values at the circuit nodes in fig 4 are calculated [8]. The voltage across the inductor is given by:-

$$V_L = -L\frac{dI}{dt} \qquad (1)$$

The current due to applied voltage V_L is given by:-

$$I = L\int_{t_{-1}}^{t_0} V_L \, df \qquad (2)$$

The integration may be approximated by the trapezoidal rule:-

$$I = I_0 + \frac{(V_L+V_{L0})\Delta t}{2L} \qquad (3)$$

or a current change from I_0 to I. V_{L0} and V_L are corresponding values for the voltages across the inductor.

By Kirchoff's law,the voltage across the inductor can be calculated as:-

$$V_L = E_t - V_d \qquad (4)$$

where Vd is the drop across the diode. The diode terminal voltage can be readily determined as:-

$$V_d = IR_f + \phi \qquad (5)$$

where ϕ represents the diode junction barrier voltage, approximately 0.7 volts.
The total charge q that has accumulated in the diode can now be calculated, but this charge decays according to [9]:-

$$q = q_0 \exp\left(\frac{-t}{\tau}\right) \qquad (6)$$

The effect of the carrier lifetime τ is modelled by the convolution of the carrier decay function with the applied current I. A modified value of the carrier concentration at the end of each step results. It can be shown that the convolution of the decay function with the forward current gives:-

$$q = \left(\frac{I+I_0}{2}\right)\tau\left(1-\exp\left(\frac{-t}{\tau}\right)\right)+q_0\exp\left(\frac{-t}{\tau}\right) \qquad (7)$$

The source voltage is assumed to be:-

$$E = E_{pk}\sin(2f_r t) \qquad (8)$$

In order to take into account the source resistance R_{source},

$$E_t = E - IR_{source} \qquad (9)$$

where E_t is the source terminal voltage.

When the accumulated carrier concentration charge reaches zero, the program switches to the impulse phase.

3.3 Impulse phase

In this mode, the SRD model is represented as in fig 4c. This consists of the junction capacitance C_d, the reverse bias diode loss, R_d and the load R.

Current through a capacitor can be represented as:-

$$I = C\frac{dV}{dt} \tag{10}$$

Integration is carried out to find the voltage across the diode junction capacitance as with the inductor in the conduction phase. The trapezoidal rule is used again to obtain a linear equation:-

$$V_c = V_{co} + \frac{(I+I_0)\Delta t}{2C} \tag{11}$$

Application of Kirchoff's laws to the reverse biased diode model leads to 3 linear equations to define 3 unknowns, derived from:-

$$E_c = E_{c0} + \left(\frac{(I-I_1+I_0-I_{10})\,\Delta t}{2C_d}\right) \tag{12a}$$

$$V_d = E_c + \left(\frac{(I-I_1)\,\Delta t}{R_d}\right) \tag{12b}$$

$$I = I_0 + \left(\frac{(V_L+V_{L0})\,\Delta t}{2L_d}\right) \tag{12c}$$

$$V_d = I_1 R \tag{12d}$$

$$V_L = E_{term} - V_d \tag{12e}$$

These equations are arranged in matrix form, and are solved simultaneously according to $\mathbf{AX} := \mathbf{B}$ where **A** and **B** are matrices and **X** is the solution vector. Termination of the impulse phase occurs when the current through the diode

changes sign to a forward direction and the diode junction voltage is greater than zero. The program then returns to the conduction phase.

This program in its basic form will provide a time domain simulation of a SRD comb generator. In order to obtain a frequency domain spectrum of the simulated signal the output file was subjected to a 4096 point fast fourier transform (FFT). The solution results are discussed further in §5.

4 SRD Phase Noise

4.1 The phase noise model

Extensive literature searches failed to reveal an analysis of the phase noise of the SRD multiplier, therefore one was produced by the author.

The sources of noise are:-

1)	Additive thermal noise	white
2)	Avalanche noise	white
3)	Microplasma noise	$1/f^2$
4)	Recombination noise	$1/f$
5)	AM to PM noise	$1/f$ and white.

The signal levels at the input to the multiplier are generally large (≈+20dBm) so that the additive thermal noise is small compared with the signal (eg, -160dBc/Hz at 5GHz output frequency). Noise performance is, however, critically dependent upon signal level [10].

Avalanche breakdown results in high levels of white noise [11] if the firing voltage peaks are excessive due to high drive levels. Microplasma noise can result in a f^{-2} relationship with offset frequency; this in turn causes excessive close to carrier phase noise. If the drive level is optimised for maximum output power, the phase noise may be degraded due to breakdown effects. A 500 MHz multiplier

specified for +27dBm drive level was found to give optimum noise performance at +24dBm [11].

Recombination noise occurs as a result of statistical variations in carrier lifetime [12]. In the intrinsic layer, some of the carriers recombine rather than become swept out of the layer; as a result, more carriers are swept into the I layer during the forward conduction than are swept out during reverse recovery. Some rectification takes place, and a small D.C current, I_{dc} flows. The percentage of carriers that recombine in a cycle of input can be calculated [13], giving the average storage time as: $t_a = 1/2f$. The DC current flow is $I_{dc} = I_{pac}/\omega\tau$, where I_{pac} is the peak ac current.

This recombination results in a reduction in the charge that must be removed from the I region. A premature termination of the recovery period therefore results. The ratio of charge lost in the recovery period q_0 to the total charge q_t is:-

$$\frac{q_0}{q_t} = \frac{2\pi}{\tau\omega} \qquad (14)$$

Assuming that the recovery current is approximately constant around the impulse time, then the ratio of charge lost to total charge is equal to the ratio of phase advance α' to firing angle α_o. Charge loss indicates the fraction of a cycle that the impulse point has moved, therefore α_o is a constant representing the value of α corresponding to infinite lifetime:-

$$\alpha = \alpha_o\left(1+\frac{1}{f\tau}\right) \qquad (15)$$

If a step change in τ occurs due to phase noise, the rate of change of τ is:-

$$\frac{d\tau}{dt} = \upsilon\tau \qquad (16)$$

where υ is a constant at particular offset frequency from carrier. The resultant change in α is :-

$$\frac{d\alpha}{dt} = \left(\frac{d\alpha}{d\tau}\right).\left(\frac{d\tau}{dt}\right) = \frac{\alpha\upsilon}{f\tau} \qquad (17)$$

This represents the phase noise introduced by a step recovery diode due to recombination, provided $f >> 1/\tau$.

4.2 Effect of biasing

If self bias were used to enhance the output power of the multiplier, the value of the bias voltage would vary due to changes in the recombination current I_{dc}. This current is determined by τ, the carrier lifetime. τ fluctuates as a predominantly $1/f$ process [14], therefore the value of self-bias voltage will also fluctuate. Firing angle variation occurs as a result of its dependence upon the lifetime, and flicker phase noise is therefore generated. The relationship between bias voltage and firing angle is [15]:-

$$E_c+\phi = E \sin\left(\alpha_o - \pi\omega\sqrt{\left(\frac{4R_d^2LC^2}{4R_d^2C-L}\right)}\right) \qquad (18)$$

where V is the bias voltage, ϕ is the diode junction barrier potential, E is the applied signal voltage, C is the reverse capacitance of the diode, L_d is the driving inductance, and R_d is the load resistance.

4.3 AM to PM conversion

This is another principal mechanism for phase noise generation in SRD multipliers. A variation in amplitude of the drive signal results in some variation in the firing angle [15] and might arise from mutual conductance variation due to $1/f$ effects in the driver transistor. Amplitude and wave shape of the drive waveform should be selected for minimum AM to PM conversion.

4.4 Parametric enhancement

The negative real admittance component of a device that displays non-linear capacitance voltage effects is [16]:-

$$G = \frac{-\pi f_o n C_V}{n+1} \qquad (19)$$

where n is determined by the junction properties of the diode used ($n = \frac{1}{2}$ for abrupt junction diodes).

The voltage capacitance for a junction diode can be described as:-

$$C(V) = K_s\left(\frac{\phi - V_s}{\phi - V}\right)^n \qquad (20)$$

where C_d is the capacitance measured at some dc voltage V_d and ϕ is the diode contact potential (approximately 0.7V). With a step recovery diode, the capacitance voltage curve is extremely steep, resulting in a large n value. Therefore if $n \to \infty$, then:-

$$\left(\frac{n}{n+1}\right) \to 1$$

and equation (19) becomes:-

$$G = -\pi f_o C_V \qquad (21)$$

where C_v is the capacitance at the DC operating point.

The presence of this negative conductance indicates that the device is susceptible to oscillation. There are problems in using this equation however to determine stability: negative resistance is essentially a small signal parameter, and cannot be easily fitted to the heavily non-linear operation of the SRD multiplier/comb generator.

SRD comb generators do exhibit parametric gain [17], and this can increase the noise level already present. Such peaking effects were investigated by adding noise to the input as shown in fig 1a, and the effect was also simulated in software with random noise values added to the driving waveform.

4.5 Instabilities

It has been suggested [17] that the presence of resonances in the band at which the negative resistance exists is the cause of parametric instabilities. These resonances are called idler resonances.

However we have observed that it is possible to obtain parametric instabilities even when there were no idler circuit elements intentionally designed into the circuit. The assumption that idler elements are necessary may be as a result of an over simplistic consideration of negative resistance effects only. Parametric effects arise as a result of non-linear differential equations, and this unstable chaotic behaviour is described in §5 below.

5 Results of the SRD Simulation

5.1 Component values

A computer simulation of the equations in §3 was run in its basic form, without attention to phase noise effects. The results are displayed in figs 6 and 9, and are discussed below. Values of components used in the simulations are given in table 1 below.

Table 1

Point on Fig 13		Point A	Point B	Point C	Point D
Reverse capacitance	C_d	2.2pF	2.2pF	2.2pF	2.2pF
Reverse resistance	R_d	3Ω	3Ω	3Ω	3Ω
Forward resistance	R_f	5Ω	5Ω	5Ω	5Ω
Minority carrier lifetime	τ	100ns	100ns	100ns	100ns
Impulse inductance	L_d	80nH	80nH	80nH	80nH
Load resistance	R	50Ω	120Ω	500Ω	1500Ω
Source resistance	R_{source}	10Ω	10Ω	10Ω	10Ω
Peak drive voltage	E_{peak}	4 volts	4 volts	4 volts	4 volts
Drive frequency	f_{ref}	100MHz	100MHz	100MHz	100MHz

5.2 Comb generator stability and chaotic behaviour

In order to investigate comb generator stability, we obtained a plot of firing angle α against load resistance R which is displayed in fig 13. The diagram is of particular interest as it resembles a class of solutions displaying chaotic behaviour known as Feigenbaum structures [19].

This behaviour originates from the population of stored charge carriers in the device, and the carrier storage effect [20] is a physical manifestation of the above solutions. The fact that a Feigenbaum diagram is produced implies that some form of recursion or feedback mechanism must be present, together with a non-linear function. The value of α determines the number of charge carriers generated in the conduction phase; these in turn determine the value of α in the next cycle, and so on. The non-linearity is introduced by the discontinuity between the conduction and impulse regions. Period doubling at the onset of the chaotic behaviour is a characteristic of this particular phenomenon, hence the subharmonic generation.

It would seem that the Feigenbaum Diagram enables a more global approach to the problem of phase noise analysis since it can include carrier storage division, not easily accounted for by parametric (negative resistance) analysis.

The effect of carrier storage division is that oscillation can occur at sub-multiples of the driver frequency f_{ref}. Although it is possible to harness this property to undertake frequency division as well as multiplication [18], in general these spurious modes are undesirable. Even if oscillations cannot occur, the parametric gain will result in enhancement of either the SRD noise or driver circuit noise (see fig 5). At frequencies close to the desired signal the negative resistance is reduced due to finite carrier lifetime. We observed, however, that this "parametric gain" is closely linked to the distance from splits in the Feigenbaum Diagram. Referring to fig 13, the single line at the left represents stable harmonic generation. As the locus

of α approaches the first split, peaking in the noise floor between harmonic combs becomes evident. At point B there is a large change in α for a small change in input conditions, leading to phase noise problems. The phase noise extends to the carrier rather than being confined to localised peaks. as can be observed in fig 8. This phenomenon is known as a splitting or Bifurcation point and can result in high phase noise and phase "hits".

If a large peak occurs at any frequency, in some systems the noise will appear at baseband due to non linear intermodulation effects, and performance degradation could result.

For low noise frequency multiplication it is vital that the bifurcation points be avoided. We have built a comb generator in order to compare our simulation results with measurements. Fig 7 displays a spectrum analyser plot of this generator operating near such a point, where the high phase noise can be seen. Fig 8 displays a 4096 point FFT of the results of a time domain simulation of the same circuit. The operating points of figs 6 and 7 are represented by point B on the Feigenbaum Diagram.

In fig 6 a time domain simulation of a correctly functioning comb generator with one impulse per cycle of input is displayed. An impulse occurs when the charge is removed from the intrinsic layer, and the diode impedance rapidly rises. Point A on the Feigenbaum diagram represents a stable comb generator with a single value of α. An FFT of the above simulation is displayed in fig 5.

Increasing the value of load resistance results in the onset of parametric oscillations in the form of carrier storage division [20], as demonstrated in fig 9. Each alternate impulse is lost when more carriers are injected into the intrinsic region for the part of the input cycle when the diode current is positive (forward), than can be removed when the diode current is negative (reverse). Fig 9 can be compared with fig 10 which is a digital sampling oscilloscope plot of our test bench SRD comb

generator undergoing carrier storage division. The lighter trace illustrates the drive voltage, corresponding to point C on the Feigenbaum diagram (fig 13), where the single locus represents stable period doubling.

Fig 11 illustrates an FFT of the time domain simulation file corresponding to point D on the Feigenbaum diagram (fig 13). In fig 11 the period doubling parametric oscillations are no longer stable and chaotic operation of the comb generator is observed. Although fig 11 assumes the appearance of broadband noise, this is not the case. The shape is actually a result, characteristic of chaotic systems, of the fact that a small change in input conditions results in a large change of output form. SRD comb generators could be an ideal candidate on which to focus study of chaotic systems.

An additional problem is that more than one impulse may be produced per cycle when the drive frequency is reduced (to 35MHz in this simulation). This is due to the oscillatory effect of drive inductance and diode capacitance driving the diode into reverse bias before the commencement of the subsequent input cycle. An unstable spectrum can also be a result of crossing into the above described mode.

Rather than implying that SRD comb generators are destined to become a problem, this work indicates the ease of simulating the comb generator and thus predicting whether problems may occur.

5.3 Using simulation to calculate phase noise

Having established a stable configuration, the phase noise can be predicted. The program calculates the firing angle α, which is used to calculate the phase noise. In order to improve the accuracy, linear interpolation is used in between discrete time steps at the termination of the conduction cycle. Any change in value of the following will change the firing angle:-

1) Carrier lifetime;

2) Drive level;

3) Diode model value fluctuations (resistance and capacitance).

A conversion factor is determined for carrier lifetime fluctuations to phase noise by applying a step change to the carrier lifetime and observing the change in α. The lifetime change would need to be determined from either measurement or noise theory. For ease of comparison a constant phase noise level of -115dBc/Hz was assumed at 1Hz from carrier [21]. Fig 12 displays a plot of reciprocal carrier lifetime against phase noise, other parameters remaining constant, with and without self bias. The value of bias resistor is changed to keep a constant bias level of 1 volt. The results are intended to apply at 1Hz from carrier. These figures can be applied to other offset frequencies by applying a factor $-10\log_{10}(f)$.

If no bias is used, the phase noise angle varies approximately according to the reciprocal of lifetime, as predicted from equation (17) above. If bias is used, the program indicates a higher level of phase noise, less dependent upon lifetime.

6 Further work and conclusions

6.1 Further Work

It is intended to continue this work with simulation of different embedding circuitry and drivers for the SRD comb generators or multipliers. The effect of other phase noise sources will be included, and different driving waveforms will be simulated in order to determine the effect upon stability and phase noise.

Accurate simulation would depend upon absolute values of phase noise contribution from carrier lifetimes being obtained via semiconductor theory or measurement. It would also be helpful to compare the results with actual phase noise measurement of practical comb generators.

6.2 Conclusions

A computer program has been written that can simulate an SRD comb generator circuit. This successfully demonstrated instability effects with such generators. Time domain simulation was initially carried out, followed by a conversion to the frequency domain by FFT. In addition a Feigenbaum diagram of the firing angle was produced. This showed similarities with classic period doubling chaotic effects: by the use of this diagram, particular combinations of circuit parameters to be avoided can be shown. The results compare favourably with those obtained from a comb generator built for test purposes. We therefore recommend that the Feigenbaum diagram be a suitable tool for use in the design of SRD comb generators.

Contributions to phase noise performance of SRD comb generators by carrier lifetime fluctuations have been assessed. For the optimum phase noise performance, simulation and theory indicate that a long lifetime diode and zero bias are desirable.

7 References

[1] Various authors, "Harmonic generation using step recovery diodes," *Hewlett Packard application note* 920.

[2] B. Pontius, "One step high order Frequency Multipliers," *Hewlett Packard application note AN416*, Hewlett Packard, Palo Alto, 1967.

[3] G. D. Lean,"Versatile microwave source," *Wireless world*, p. 56, Sept 1978.

[4] S. Hamilton & R. Hall, "Shunt mode generation using step recovery diodes," *Hewlett Packard technical note*, p. 65, 1967.

[5] J. Grebenkemper, "Tutorial on phase noise," *Watkins Johnson application note*, p. 5, 1982.

[6] V. Manassewitsch, "*Frequency synthesisers, theory and design*," chap. 2 p. 119, Wiley, New York, 1985.

[7] M. I. Sobhy *et al*, "Chaotic Behavior of Microwave Circuits", *European Microwave Conference, 1990"*pp 363-368.

[8] F. Kuo, "*Network Analysis and Synthesis,*" Chap. 5 p. 120, Wiley, 1966.

[9] A.S. Grove, "*Physics and Technology of Semiconductor Devices,*" Chap. 5 p 121, Wiley, New York, 1967.

[10] Dieter Scherer, "Generation of low phase noise microwave signals," *Hewlett Packard RF and Microwave symposium and exhibition notes,* 1981, p. 21.

[11] T. Watanabe & Y. Fakatsu, "Characteristics of Semiconductor Noise Generated in Varactor Frequency Multipliers," *Review of the Electrical Communication Laboratory,* vol. 15 nos 11-12, Nov.-Dec. 1967, p. 760.

[12] *ibid* p. 753.

[13] Various authors, "Harmonic generation using step recovery diodes," *Hewlett Packard application note* 920, p. 10.

[14] M.J.Buckingham, "*Noise in Electronic Devices and Systems,*" Chap. 5, p. 128, Wiley, New York, 1983.

[15] S Hamilton R Hall, "Shunt mode Harmonic generation using Step Recovery Diodes," *Hewlett Packard technical note* 1967, p. 70.

[16] V. Manassewitsch, "*Frequency synthesisers, theory and design,*" chap. 6, p. 369 New York: Wiley 1985.

[17] Various authors, "Harmonic generation using step recovery diodes," *Hewlett Packard application note,* 920, p. 25.

[18] R. Pritchard, "*Thesis on microwave dividers,*" Leeds University, UK, 1985 p. 64.

[19] K. Becker & M. Dorfler, "*Dynamical systems and Fractals,*" Chap. 2 p. 40 Cambridge University Press 1990.

[20] W. D. Ryan & H. Williams, "The carrier storage frequency divider, a steady state analysis," *IEE Transactions on Circuit Theory,* pp. 396-403, Sept. 1964.

[21] R. Muat, *Hewlett Packard Symposium on Phase Noise,* notes 1986 p. 24.

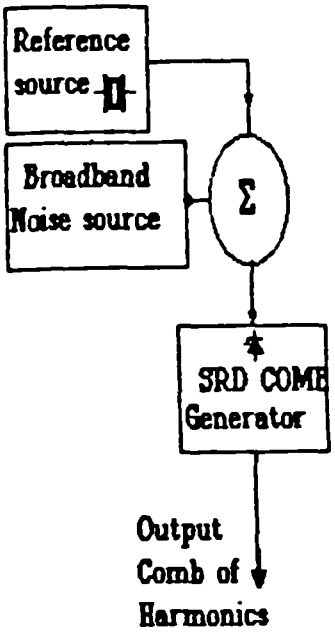


Fig 1a Block diagram of test setup and simulation

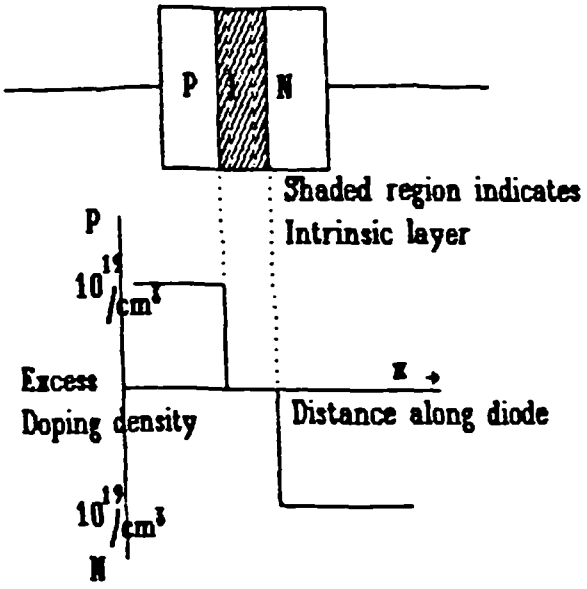


Fig 1b Doping profile of Step recovery diode.

Co is the reverse capacitance measured at Va

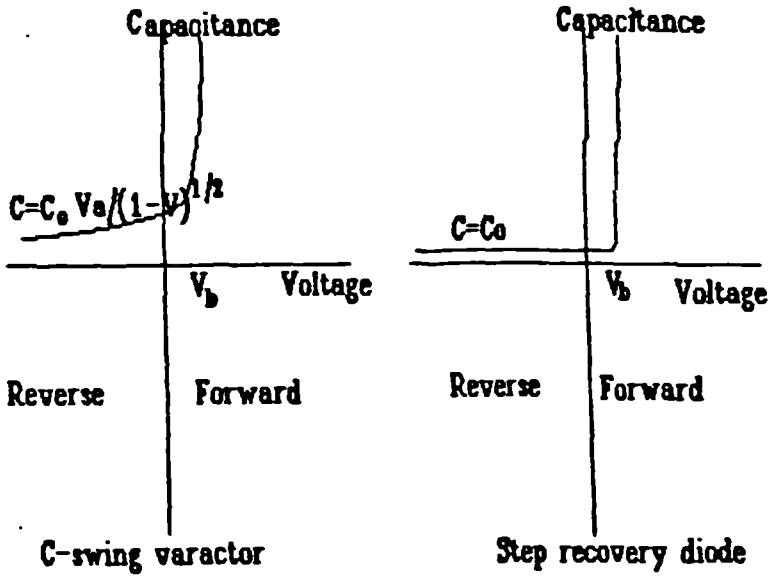


Fig 2 Capacitance voltage characteristic of a varactor and a SRD

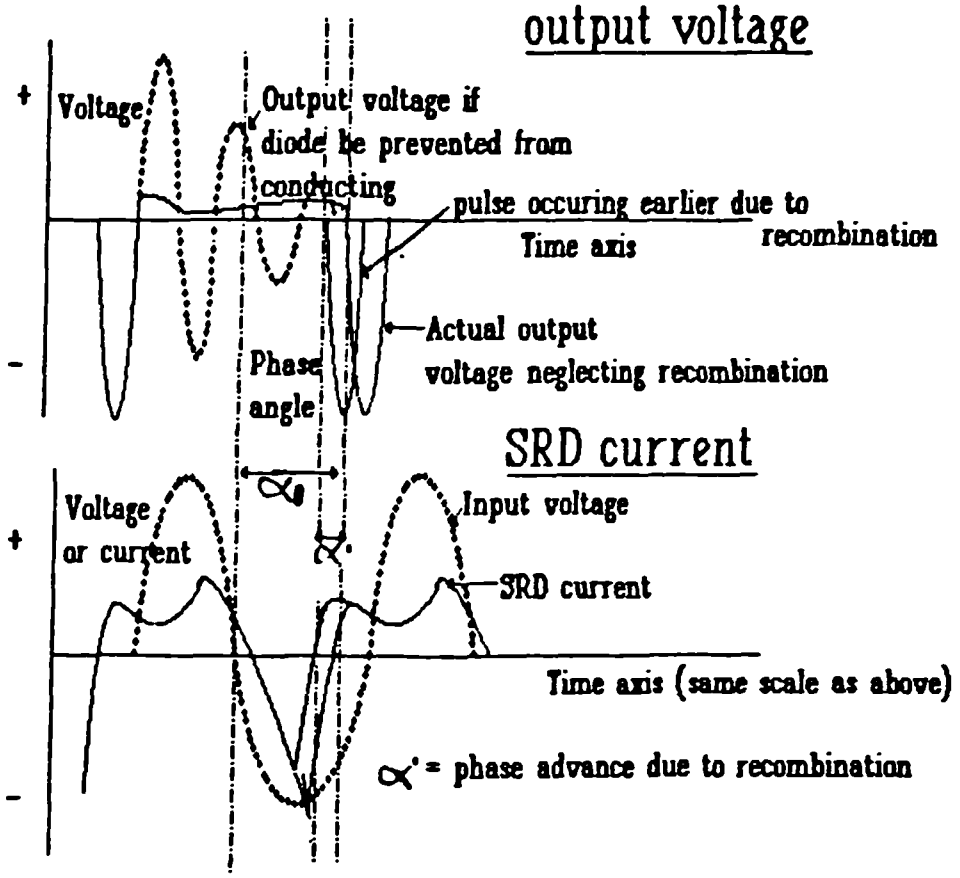


Fig 3 Current and voltage plots for a SRD comb generator

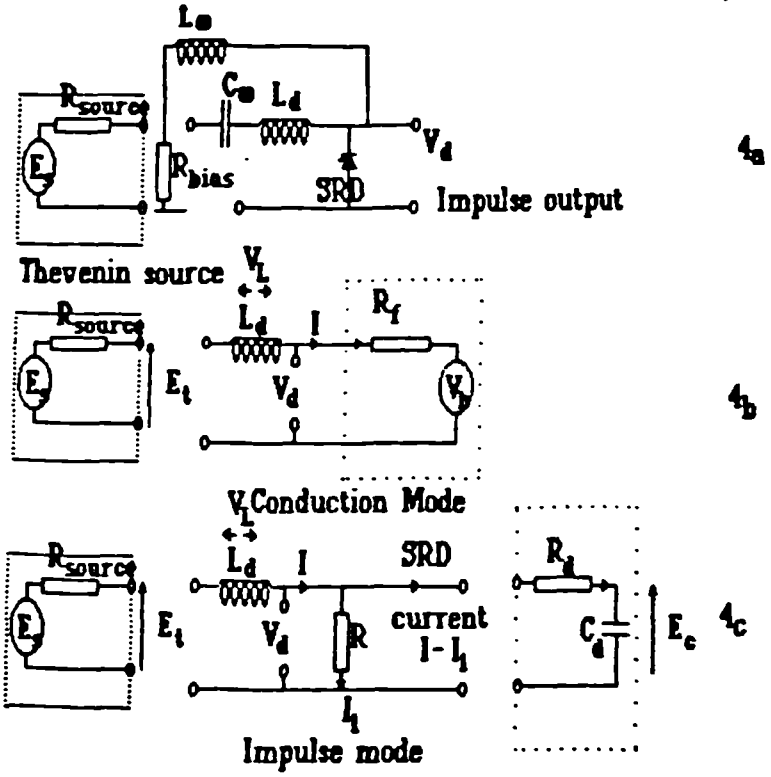


Fig 4 Step recovery diode equivalent circuits used in simulation

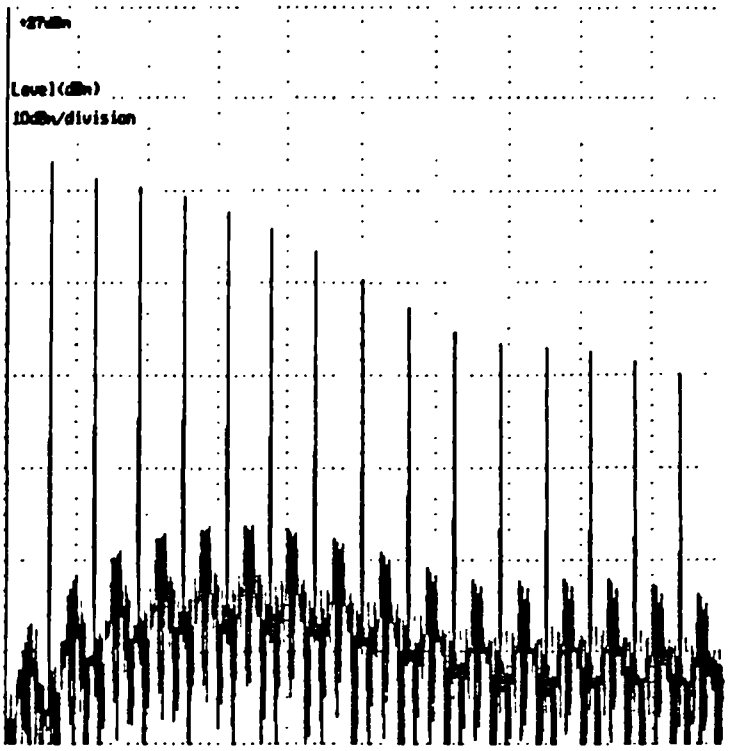


Fig 5
FFT of Correctly functioning comb generator

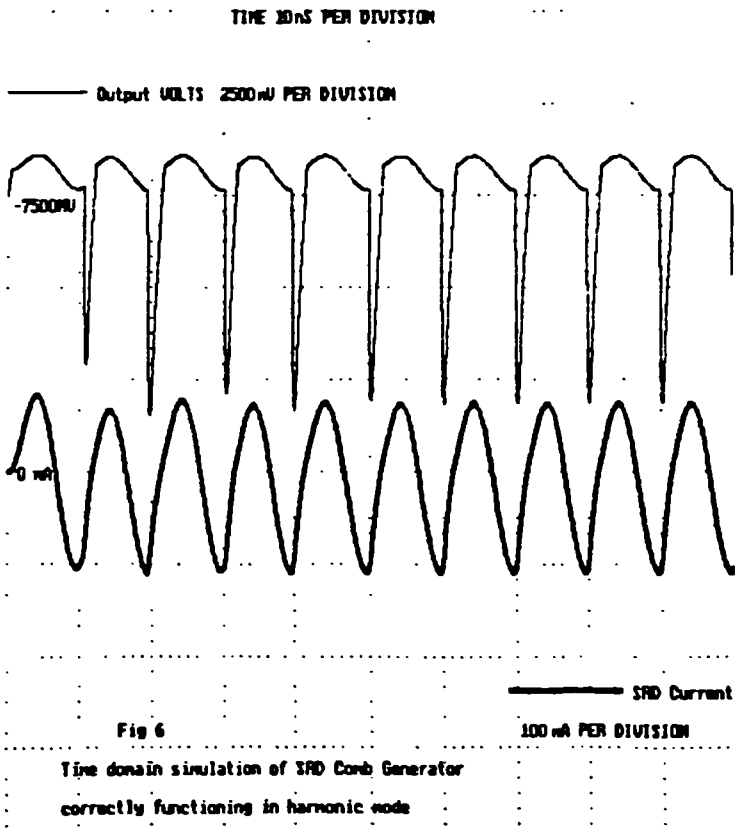


Fig 6
Time domain simulation of SRD Comb Generator
correctly functioning in harmonic mode

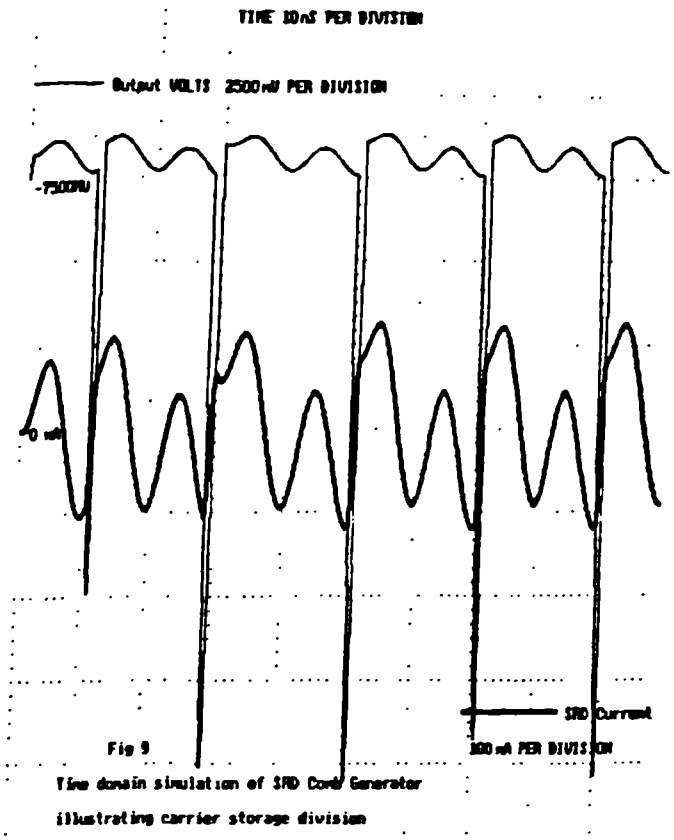
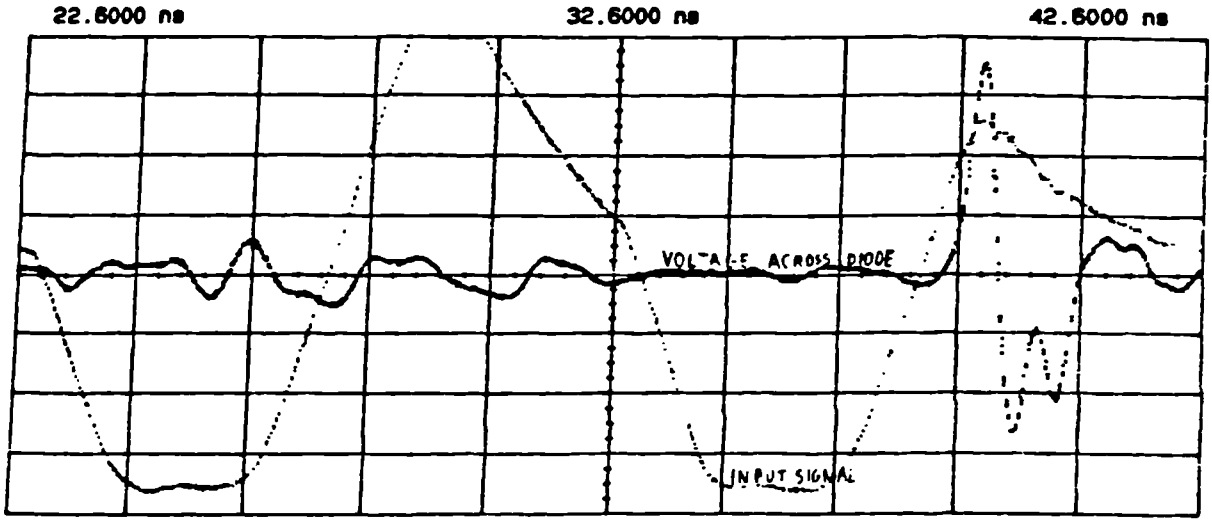


Fig 9
Time domain simulation of SRD Comb Generator
illustrating carrier storage division



Timebase = 2 ns/div Vertical = 2 v/div

Fig 10 Digital storage oscilloscope plot of actual comb generator illustrating carrier storage division.

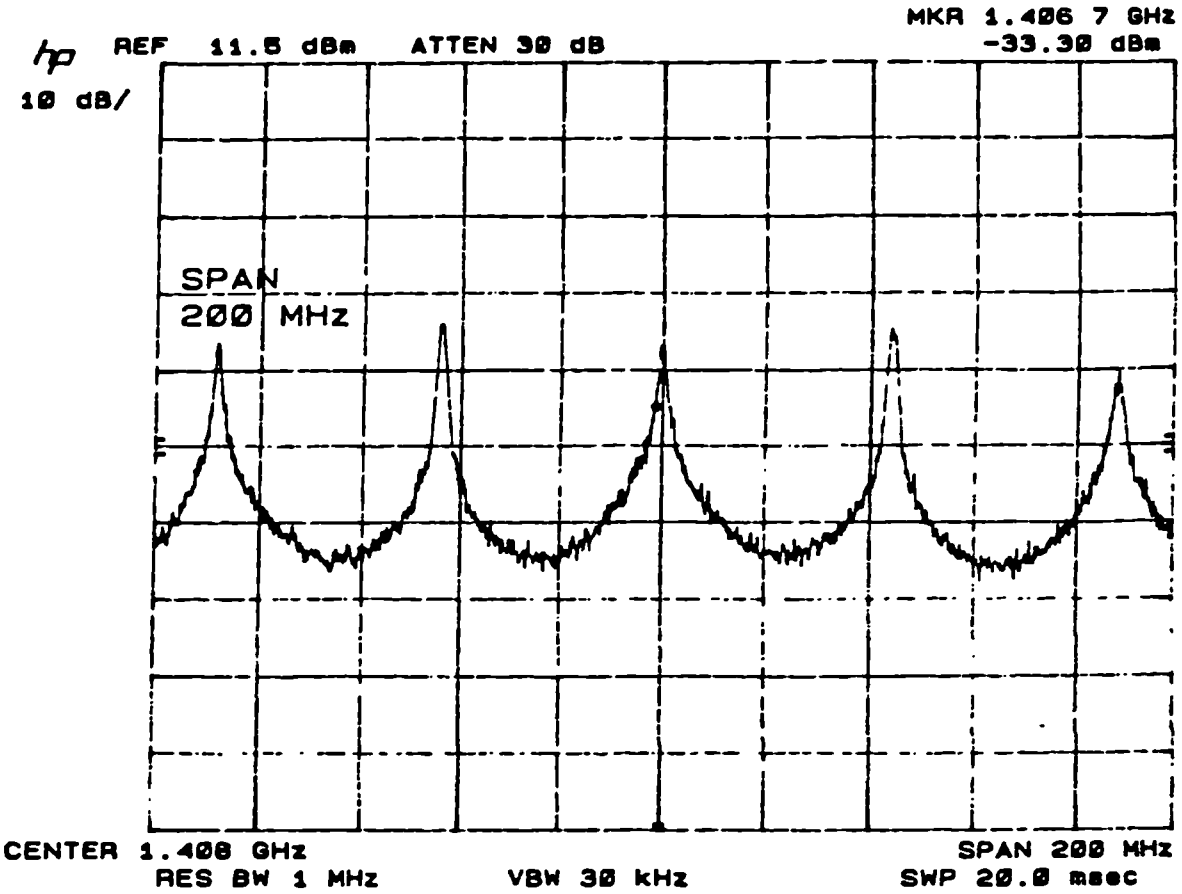


Fig 7 Spectrum analyser plot of noisy comb generator near bifurcation point

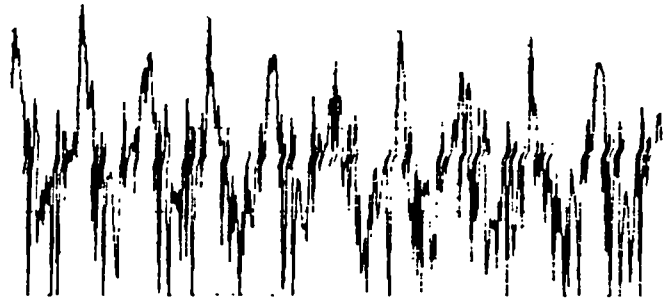


Fig 8
FFT of comb generator operating at bifurcation point
This results in poor phase noise performance

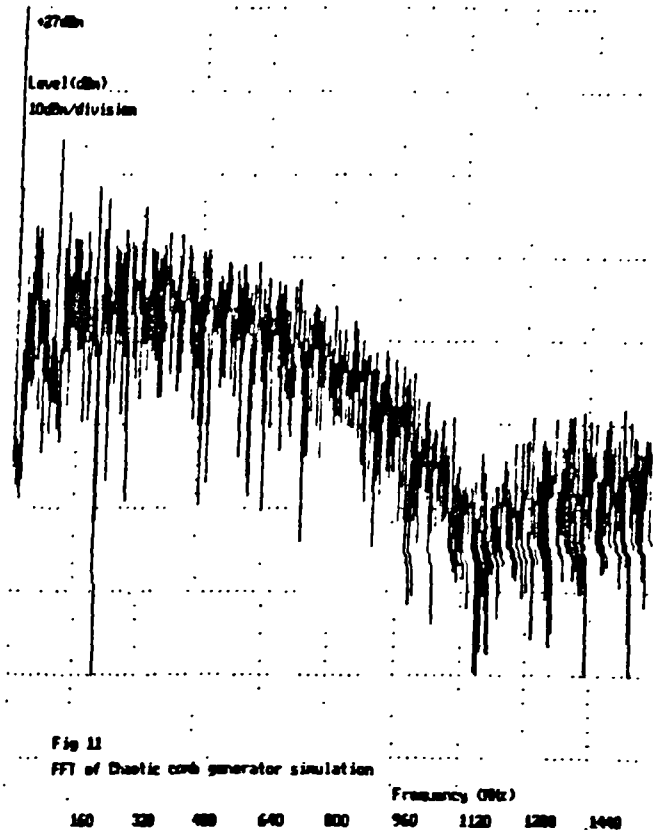


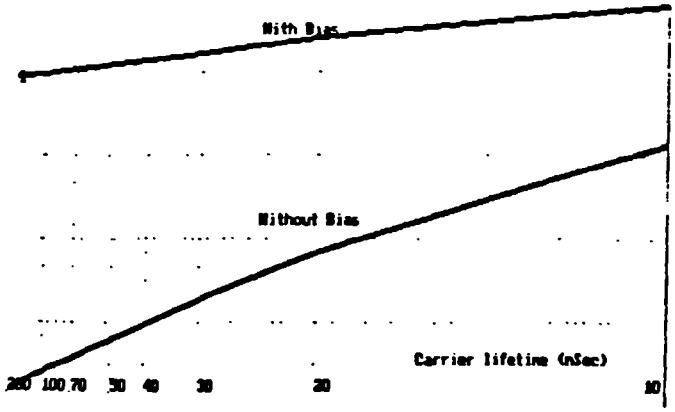
Fig 11
FFT of Chaotic comb generator simulation

Frequency (MHz)

2.5

Fig 12
Plot of phase noise against lifetime calculated for
STD Comb Generator drive frequency of 180 MHz

2 Phase jitter (microrads/ Hz)



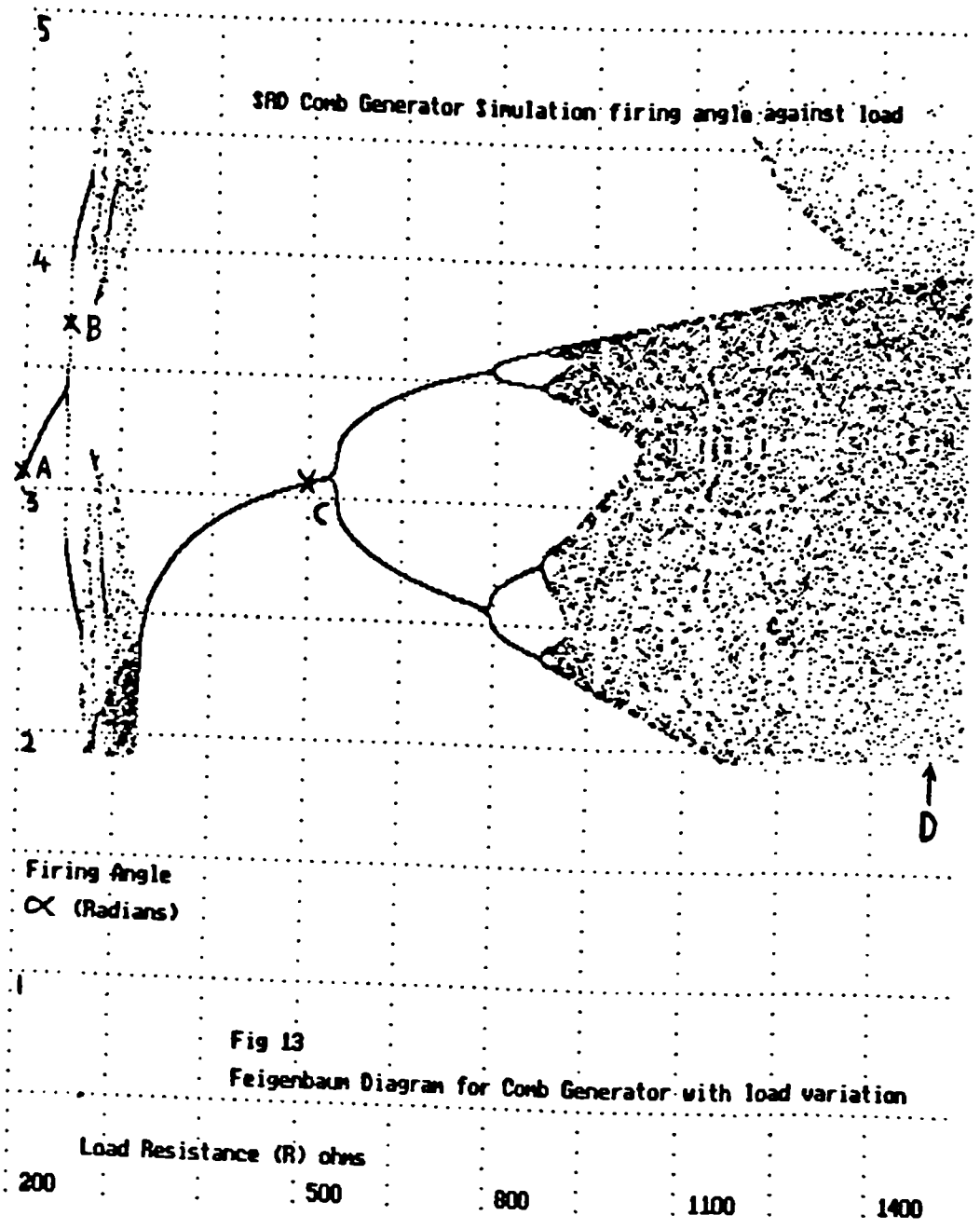


Fig 13

Feigenbaum Diagram for Comb Generator with load variation

BRITISH PATENT APPLICATION

P-COMM001 .AA

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Title: *IMAGE-REJECTING PHASE DETECTOR*

Application No: *9113682.0*

Filing Date: *25th June 1991*

ABSTRACT

PHASE-LOCKED LOOP OSCILLATOR CONTROL CIRCUIT

A fixed-frequency oscillator (12) provides a signal to a phase-shifting network (22) which provides two signals of the same fixed frequency but in phase quadrature. Two mixer (20, 21) are provided, to each of which is applied an output from a voltage-controlled oscillator (10) and a separate one of the two phase quadrature signals. A phase detector (13) responds to the outputs of the mixers (20, 21) and to a reference signal from a further oscillator (14) to provide an output voltage for application to the voltage-controlled oscillator (10) to control the frequency thereof.

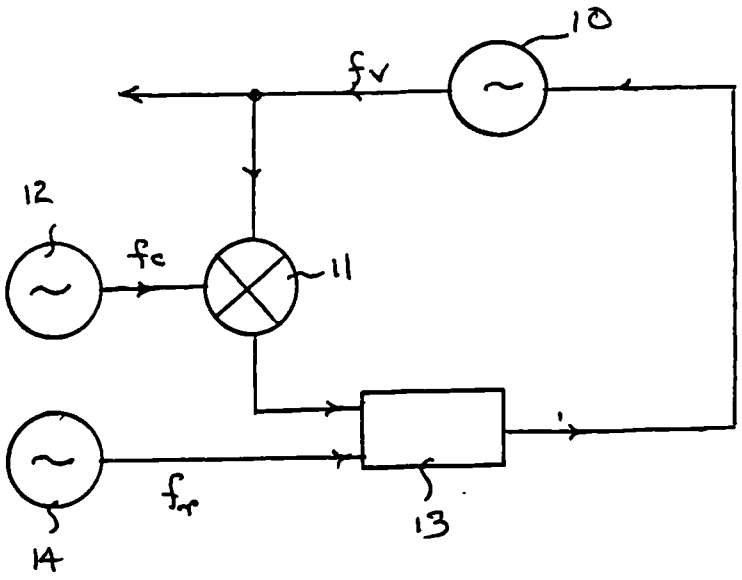

FIG 1

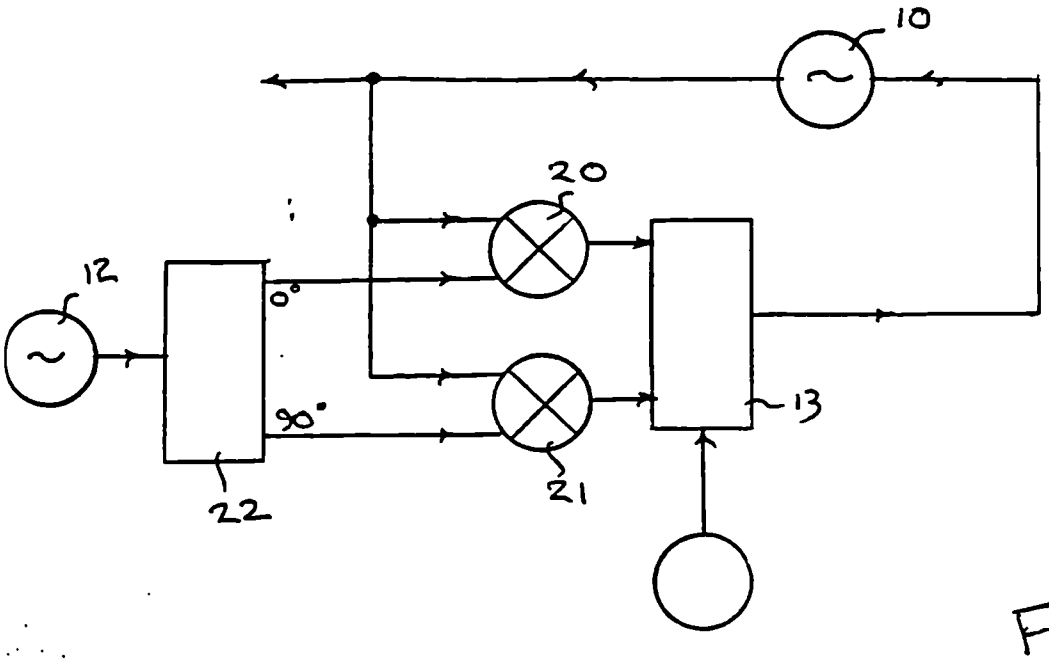

FIG 2.

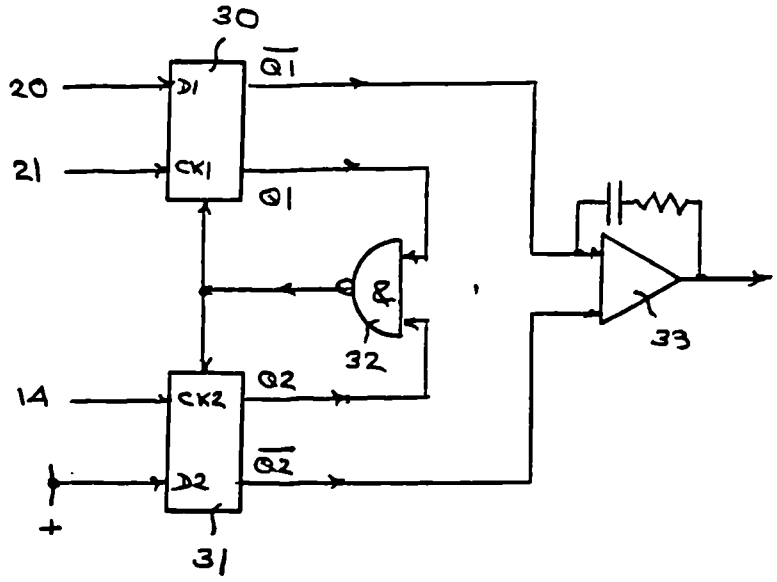
30
20
21
14
D1
CK1
Q1
Q1
&
32
33
CK2
Q2
D2
Q2
+
31

FIG 3

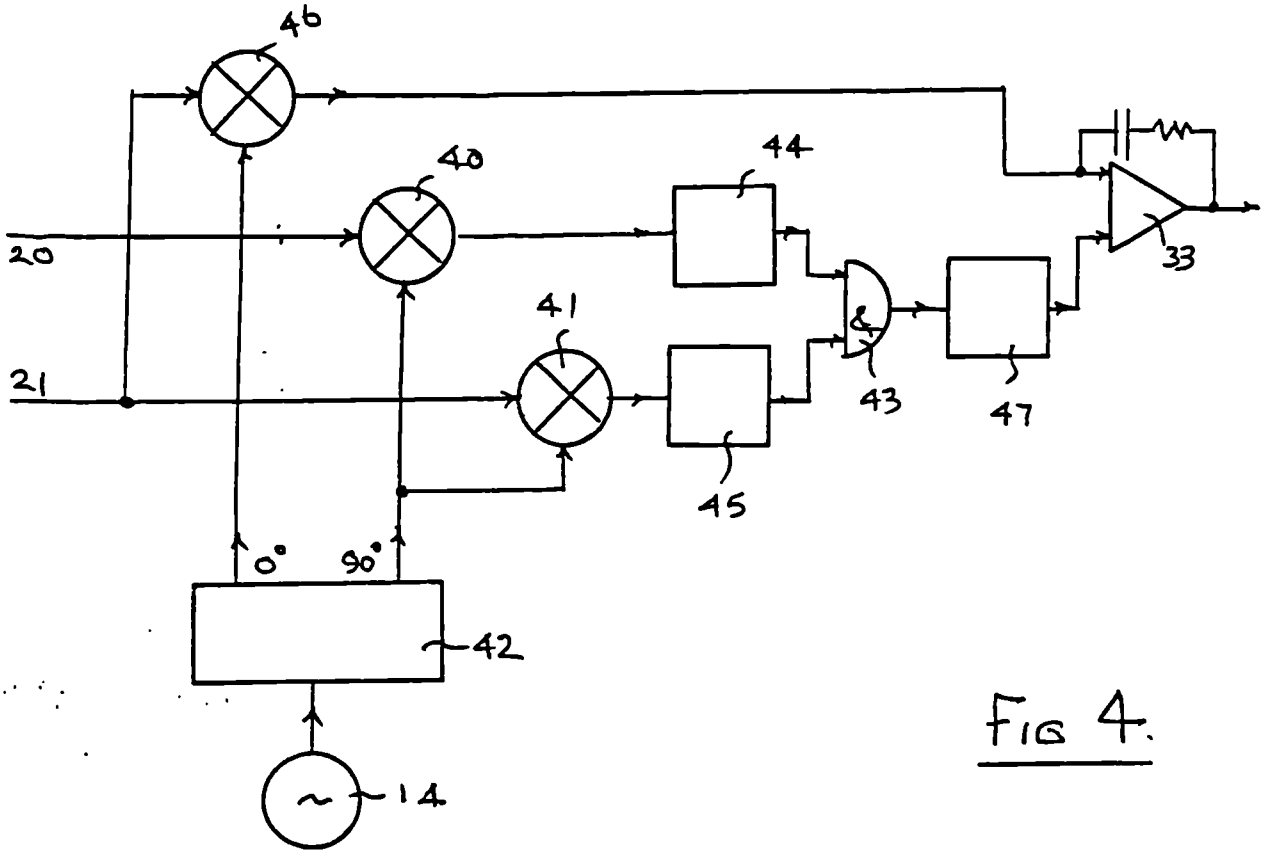
46
40
44
20
41
21
&
43
47
33
45
0°
90°
42
14

FIG 4.

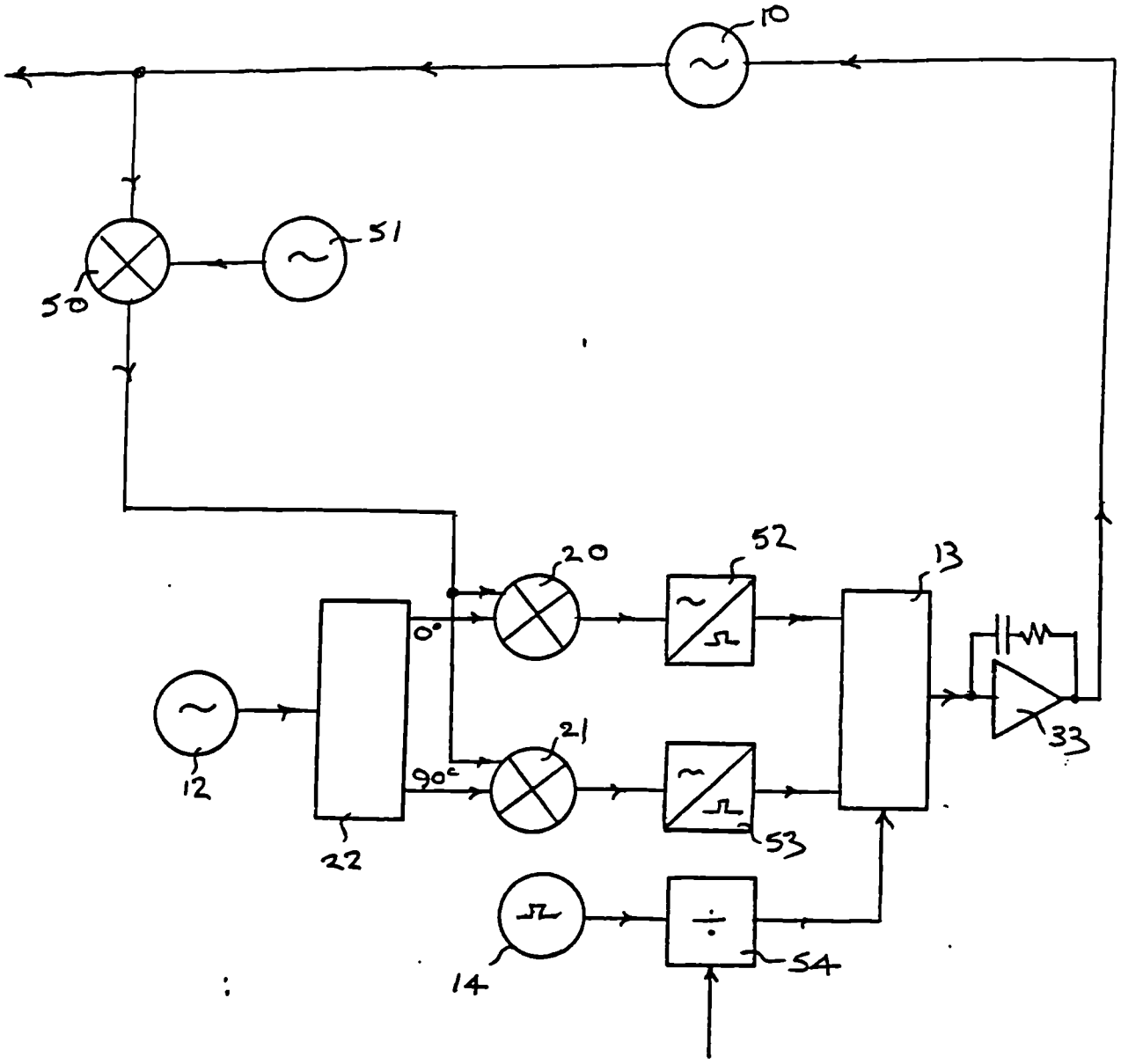

FIG 5.

SPURIOUS REDUCTION TECHNIQUES FOR DIRECT DIGITAL SYNTHESIS

* M.P. Wilson and T.C. Tozer

Introduction

The major problem with fine step size synthesisers is achieving low phase noise concomitant with immunity to vibration and low levels of spurious signals. Direct digital synthesis will provide low phase noise and immunity to vibration, but the spurious performance at present often leaves something to be desired. This has led to a possible solution for which a patent has been applied for [1]. The proposed DDS implementation takes place largely in the digital domain which enables a high level of integration.

Origin of DDS spurious signals

Apart from quantization, the main sources of errors are DAC polynomial linearity errors and switching transients. The output of a practical DAC may be represented as:-

$$V_{out}=V_{ref}((Q/(2T-1))E_p(Q)$$

where V_{ref} is the DAC reference voltage, Q the digital input word, T the full scale digital world, and $E_p(Q)$ a polynomial which represents non-linearity errors of the DAC. This polynomial will produce harmonics of the intended sinewave, which are aliased by the sampling frequency f_{ref} to produce spurious signals [2]. It is independent of f_{ref} and represents the integral non-linearity (INL) and differential non-linearity (DNL). The effect of these errors is displayed in fig 1 which shows a typical DAC transfer function.

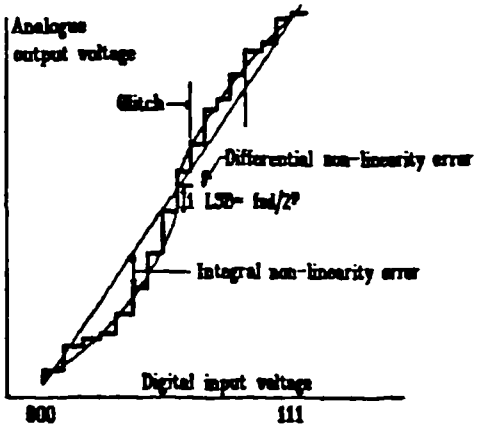

Fig 1 DAC non-linearity errors

Because not all the DAC current sources switch simultaneously, transients are introduced which are unrelated to the analogue level transitions [3]. This has the effect of introducing an additional error polynomial $S_p(Q)$ which can be expressed in terms of the averaged value of the transients over one f_{ref} period. The actual values in the polynomial are dependent upon the level transitions involved and f_{ref}. $S_p(Q)$ represents dynamic non-linearity effects of the DAC and is distinguishable from DNL and INL in that the base spectrum before aliasing changes with output frequency.

---

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The Proposed Technique

The proposed DAC decorrelation technique aims to randomise the error polynomials so that there is no correlation of errors from one cycle of the DAC characteristic to the next. In the time domain, decorrelation produces the effect shown in fig 2. A pseudo-random number is added or subtracted to the look up table output by means of an ALU placed at the digital port of the DAC. The decorrelation process acting upon a typical DAC transfer function can be observed. A DAC output level at point A becomes A' and that at point B, B'. By the analogue subtraction of a compensating signal from a second DAC, the signal is restored to the correct level. On a subsequent cycle of signal, for the same intended output point, the random number offset will be different, leading to a different values of A' and B'. Errors will therefore not correlate between adjacent cycles.

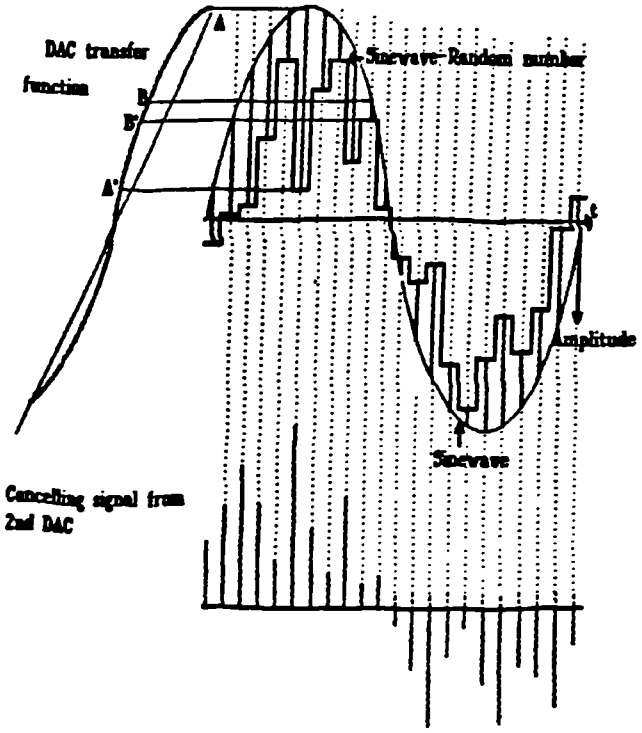

Fig 2 DAC decorrelation over one DDS cycle

The effective output of the analogue circuitry is the average of all levels over which the decorrelation is applied. After sampling at the clock frequency, the noise, rather than the harmonics, are folded back over the signal output range. Effectively, the reconstructed sampled data signal becomes a sinewave plus noise rather than sinewave plus harmonics. In order to completely randomise the polynomials, every level of the DAC should be used at random to generate each level of desired output signal. Therefore the added decorrelation factor must be uniform across all DAC levels, and be cancelled in the post DAC analogue section by means of another DAC. The pseudo-random number generator can be of any of the standard techniques with the main requirement of a long repetition cycle.

Implementation

In practice complete decorrelation of the DAC is difficult to achieve as the average value of all the DAC levels would need to be zero. Therefore a compromise must be reached where some weighting of the DAC decorrelation distribution is allowed. This weighting should be designed to be effective on the lowest order term possible in the error polynomials, ie integral non-linearity [4]. Two methods of implementation of the decorrelation technique have been investigated, and are described below.

In the first method a P-1 bit random number is subtracted (if the trigonometric word is positive) or added (if the trigonometric word is negative) to the main DAC input, thus preventing ALU

overflows. The random number is also fed to the second DAC, and the output of the DACs are summed such that the desired output signal is recreated; it is seen that the random number component number is effectively removed. A residual error signal remains, but the error pattern becomes non-repetitive. Fig 3 demonstrates the technique.

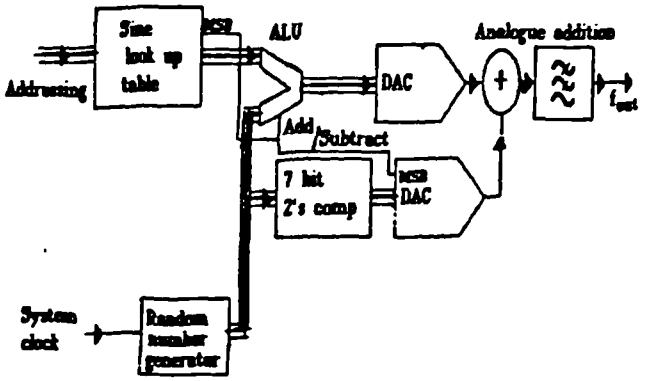

Fig 3 Decorrelation of DACS by means of pseudo-random number

The output from the post look-up table DAC can be observed uppermost on fig 4a: the sinewave is regenerated by adding in the output of DAC2.

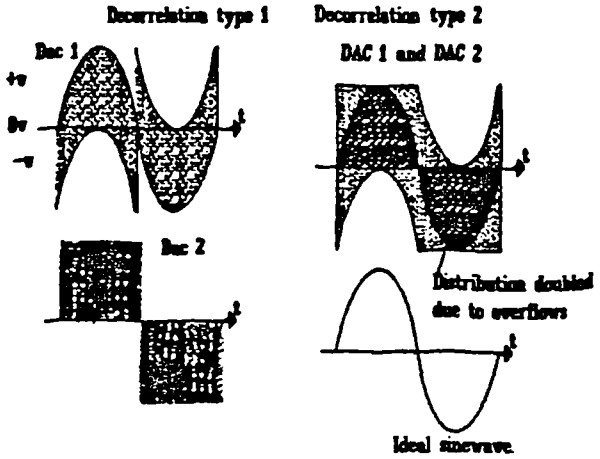

Fig 4a Probability distribution of DAC values, no overflows

Fig.4b Probability distribution with overflows

With this technique, only the upper or lower half of the DAC is being decorrelated and there is a possibility of a repetitive discontinuity at the zero voltage level. Due to these factors, the improvement in spurious levels was expected to be limited, and it was confirmed by measurement that there is a limit to spurious improvement of approximately 10dB.

To facilitate further reduction of spurious levels, the method was modified to allow the ALU to overflow after the addition of the pseudo random number. Such an arrangement allows the modified DAC word to fold back into the DAC output range, as indicated in fig 4b. This method allows a smooth cross-over at the midpoint of the DAC range, resulting in a reduction of high order spurious products.

In order to reduce the spurious products generated by truncation errors, interpolative dither is also added between DAC quantization steps. If an 8 bit output look up table is driven from a 12 bit phase address, then the number of input steps per output step varies from 5 at zero level to 163 at the waveform peaks. There is obviously a trade off between dither and added phase noise. Unlike that of a squarewave synthesiser, the length between steps in phase is independent of frequency word, so the dither random number level can be fixed. The reason why dither has not previously been applied to sinewave synthesisers is that the effect of DAC

non-linearities dwarfs the contribution due to DAC quantization errors [5]; dither effects would be ineffectual if DAC non-linearities are allowed to remain. However the effects of DAC decorrelation are such that the possibility of benefits from dither can be considered. Fig 5 displays the method of adding phase and amplitude dither.

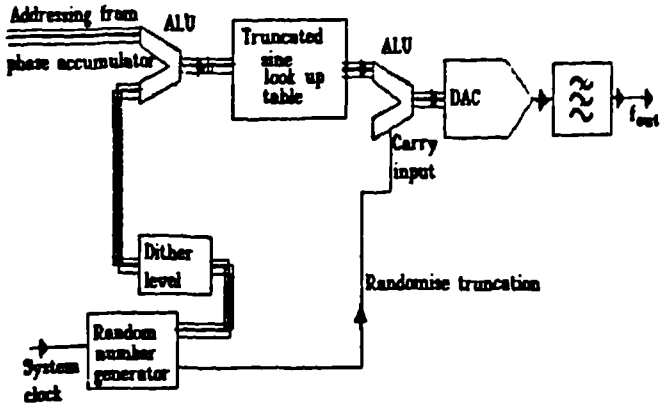

Fig 5 Sine DDS with dither

Results

An experimental DDS was built implementing the techniques described here. DAC 0800 chips were used, updated at a frequency of 7.6MHz. Spurious signal levels were measured by means of a HP8566B spectrum analyser, and are displayed in fig 6.

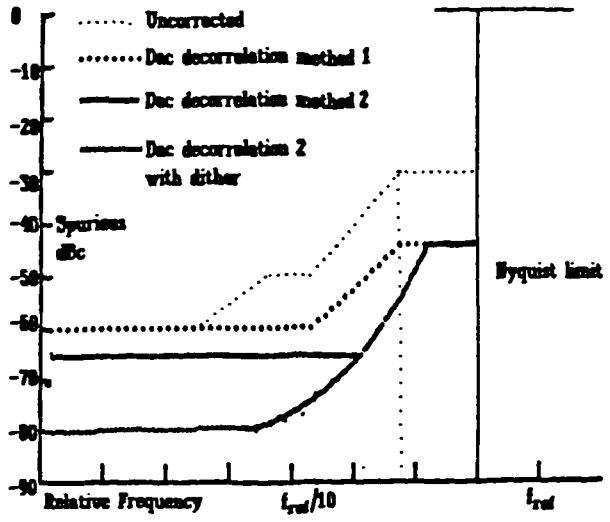

Fig 6 Measured performance of various DDS spurious reduction techniques. F_{ref} = 7.643MHz

Without the spurious reduction technique, the performance of the DAC 0800 is noticeably poor, and high order spurious products abound in the output spectrum. With the spurious reduction technique, there is a substantial reduction in the level of spurious products amounting to 30 dB over part of the usable DDS output frequencies. Allowing overflows made a substantial difference to the spurious spectrum, as did truncation dither for the lower frequency ranges. Fig 7 shows a spectrum analyser display of the synthesiser output at 1.529MHz with no spurious reduction techniques (faint trace), and with DAC decorrelation and interpolative dither (bold

trace). All measured spurious signal reduction effects were verified by computer simulations. However, the low order spurious signals were reduced further in the simulation than the measurements suggest. The discrepancies may be due to INL effects in the DAC, but further investigations are required of this.

Further work

To complete this program, the following work is recommended:-

* The construction of a circuit with a faster clock frequency and better DACs;
* Committing the design to a custom VLSI to reduce size and component count;
* Investigate why low order spurious levels are higher than theory or simulation suggests.

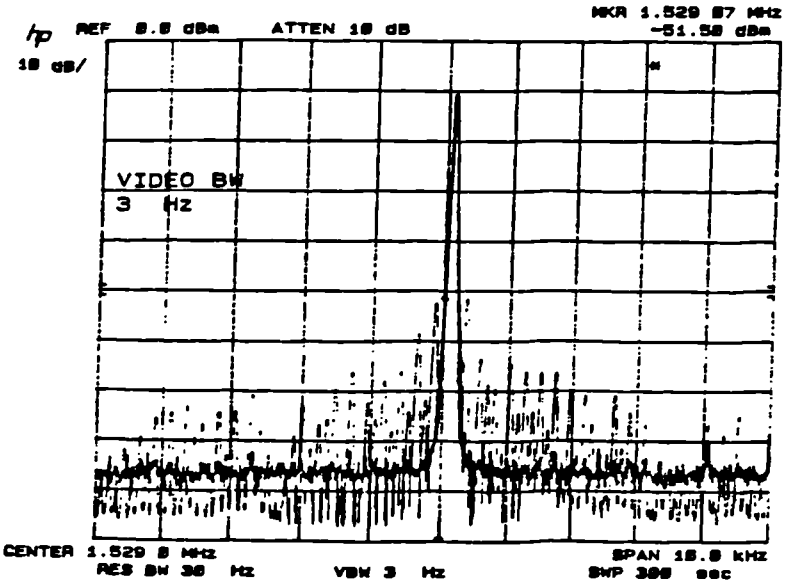

Fig 7 Spectrum analyser plot without and with spurious reduction techniques

Conclusions

A method of randomising the transfer functions of DACS used in DDS and achieving a consequent reduction in spurious signal levels has been demonstrated. After this DAC transfer function decorrelation, it was possible to use interpolative dither to reduce the effect of truncation errors. By the combination of these techniques together with a 8-bit DAC it was possible to obtain spurious signal levels lower than -70dBc in relation to the carrier over much of the useful output range of the DDS.

References

[1] Wilson, M.P "Signal generation using analogue-to-digital conversion", European patent application 91302926.0

[2] Wheatley, C.E. and Phillips,"Spurious suppression in direct digital synthesisers", *D.E. USA Eradcom May 1981* FT. Monmouth NJ0770

[3] Harris inc. "Definition of DAC Specifications", *Harris Linear and Data Conversion Handbook* 1982 p5.20.

[4] Zavrel, R "Digital Modulation using the Numerically Controlled Modulated Oscillator", *RF Design*, Sept 1987 pp27-31.