HIGH EFFICIENCY BASE DRIVE DESIGNS FOR POWER CONVERTERS USING SILICON CARBIDE BIPOLAR JUNCTION TRANSISTORS

By

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List of Abbreviations and Acronyms

AC	Alternative Current
CCM	Continuous Current Mode
DCM	Discontinuous Current Mode
DUT	Device Under Test
DC	Direct Current
EMF	Electro-Motive Force
EMC	Electro-Magnetic Compatibility
ER	Energy Recovery
FPGA	Field-Programmable Gate Array
HV	High Voltage
IGBT	Insulated Gate Bipolar Transistors
IMGT	IGBT and MOSFET Gated Transistor
JFET	Junction Field Effect Transistor
MJTE	Multistep Junction Termination Extension
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
NPT	Non Punch Through
NTC	Negative Temperature Coefficient
PCB	Printed Circuit Board
PF	Power Factor
PT	Punch Through
PWM	Pulse Width Modulation
RBSOA	Reverse Biased Safe Operation Area
RMS	Root Mean Square
SiC BJT	Silicon Carbide Bipolar Junction Transistor
SiO_2	Silicon dioxide
SPICE	Simulation Program with Integrated Circuit Emphasis
ZVS	Zero Voltage Switching

Nomenclature

Symbol	Description	Unit
C_{BC}	junction depletion capacitance between base and collector	F
C_{BE}	junction depletion capacitance between base and emitter	F
C_{CS}	collector to substrate capacitance	F
C_{pulse}	pulse capacitor in the base drive	F
C_3	pulse capacitor in the energy recovery base drive simulation circuit	F
D_{max}	the maximum duty cycle	%
D_{SW1}	duty cycle of SW1 in the active base drive	%
D_{SW3}	duty cycle of SW3 in the active base drive	%
E_c	critical electric field strength	MV/cm
E_g	energy band gap	eV
E_{on}	turn-on energy loss	J
E_{off}	turn-off energy loss	J
E_{tot}	total switching energy loss	J
I_B	base current	A
$i_{B(t)}$	time-variant base current	A
$I_{b,AV}$	average value of the base current	A
I_{bRMS}	RMS value of the base current	A
I_{b_con}	base current in the conventional base drive	A
I_{b_active}	base current in the active base drive	A
I_C	collector current	A
I_D	current sourced from the driver power supply	A
I_{DC}	base DC current for the conduction	A
I_E	emitter current	A
$i_{in}(t)$	input current of the integrated converter	A
I_L	inductor current in the energy recovery base	A

	driver	
$i_{L,peak}$	inductor peak current in the integrated converter	A
$i_{L,average}$	inductor average current in the integrated converter	A
I_{nc}	current caused by the electrons swept into the collector	A
I_{ne}	current caused by the electrons injection into the base	A
I_{pe}	current caused by the holes injection into the base	A
I_S	saturation current	A
I_{short}	short circuit current when Q1 and Q2 are both turned on	A
L_1	inductor used in the active base drive	H
L_{Par}	parasitic inductance	nH
N_a	acceptor density	cm^{-3}
N_d	donor density	cm^{-3}
P_{BE}	base-emitter power loss	W
P_{ER}	power saving due to the energy recovery	W
$P_{C_{BE}}$	power fed to the base-emitter capacitor	W
$P_{C_{pulse}}$	power fed by DC source due to C_{pulse} in the conventional base drive	W
P_{con_loss}	power loss of the conventional base drive power supply	W
$P_{on-state\ loss}$	conduction loss of the power devices	W
P_{Q1}	power loss of Q1	W
P_R	resistive loss in the conventional base drive	W
P_{R_1}	R_1 loss in the active base drive	W
P_{pro_loss}	energy recovery base drive loss	W
$P_{turn-on\ loss}$	turn-on loss of the power devices	W
$P_{turn-off\ loss}$	turn-off loss of the power devices	W

$Q_{B(t)}$	charges in the base region	C
Q_F	excess carrier charges stored in the base	C
r_C	collector internal resistance	Ω
r_E	emitter internal resistance	Ω
r_B	base internal resistance	Ω
R_1	base resistor used to set up base DC current	Ω
R_2	base terminal damping resistor in the energy recovery driver	Ω
R_3	damping resistor in the energy recovery driver	Ω
R_L	load resistor of the integrated converter	Ω
R_{SW1}	the on-state resistance of the switch (SW1)	Ω
T_F	half switching period of the integrated converter	s
T_{on}	conduction time	s
T_s	switching period of the integrated converter	s
T_{SW3}	switching period of SW3 in the active base drive	s
T_{heat}	heating period	s
$V_{ac}(t)$	input AC power supply voltage	V
$V_{CE,Q1}$	collector-emitter voltage of Q1	V
$V_{CE,Q2}$	collector-emitter voltage of Q2	V
V_{BC}	base-collector voltage	V
V_{BE}	base-emitter voltage	V
$V_{be(sat)}$	voltage drop across the base-emitter junction during the on-state	V
V_{ce_active}	collector-emitter voltage during the conduction driven by the active base drive	V
V_{CE}	collector-emitter voltage	V
V_{C1}	C1 voltage in the active base drive	V
V_{ce_con}	collector-emitter voltage during the conduction driven by the conventional drive	V

V_{DD}	base drive supply voltage	V
V_{out}	output voltage of the integrated converter	V
V_{pulse}, V_c	voltage across of C_{pulse} during the conduction	V
V_{peak}	peak value of the AC input voltage	V
W_{in}	input energy of the integrated converter	J
W_{out}	output energy of the integrated converter	J
f_s	switching frequency	Hz
α_F	common-base current gain	
β	common-emitter current gain	
β_R	reverse current gain	
ε	dielectric constant	
λ	thermal conductivity	W/cmK
ρ	charge density	C/m^3
μ_n	electron mobility	cm^2/Vs
μ_p	hole mobility	cm^2/Vs
τ_F	forward transit time	s
x_n	space charge width in n region	m
x_p	space charge width in p region	m
v_{sat}	saturation velocity	10^7cm/s
ω_d	angular frequency	rad/s

Abstract

This thesis explores the base driver designs for Silicon Carbide Bipolar Junction Transistors (SiC BJTs) and their applications for power converters. SiC is a wide bandgap semiconductor which has been the focus of recent researches as it has overcome the several of physical restrictions set by the silicon material. Compared with silicon bipolar devices, SiC BJTs have several advantages including a higher maximum junction temperature, higher current gain and lower switching power losses. Transient power losses are low and temperature-independent in a wide range of junction temperatures. With junction temperature capable of being between 25ºC to 240ºC, SiC BJTs have been of great interest in industry. As a current-driven device, the base driver power consumption is always a major concern. Therefore, high efficiency base drive designs for SiC BJT need to be investigated before this power device can be widely used in industry.

Due to the base drive loss analysis, the pulse capacitor that is used in a conventional base drive is the main contributor to power consumption under high switching frequency and low base current conditions. The energy recovery concept can reduce the power losses associated with this capacitor. This concept is firstly used for a SiC BJT drive design. Based on this concept, a drive design termed as the energy recovery base drive is proposed. The experimental results demonstrate lower driver losses compared with the conventional base drive. The proposed driver is verified in a 1.7kW boost converter switching at various frequencies.

An active base drive has been firstly proposed to reduce the resistive power losses that dominate the total driver power consumption for applications which implement low switching frequency and high duty cycle. Even if a high-voltage power supply is used in the active base drive unit for fast switching, a low voltage branch composing of a voltage step-down function supplies the required DC base current to maintain the conduction of the BJT. Low driver losses, low switching and conduction losses are achieved experimentally. The integrated converter, which adopts motor winding inductance instead of a bulky and heavy discrete inductor in a conventional power converter, has been developed as a platform to verify both the boundary theory analysis for the converter and the functionality of the active base driver.

Publications

Hui Zhu, Mark Sweet, E.M. Sankara Narayanan, "A Comparison of Switching Characteristics between SiC BJT and Si IGBT at Junction Temperature above 200ºC," PCIM Asia 2015; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management; 24-26 June 2015

Content of Chapter 2 is based on this publication.

Hui Zhu, Mark Sweet, E.M. Sankara Narayanan, "Base drive energy recovery for a silicon carbide bipolar junction transistors," IET Power Electronics, Volume 8, Issue 12, December 2015, p. 2429 – 2434

Content of Chapter 3 is based on this publication.

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Contents

1 Power Semiconductor Devices and Drivers

Nowadays, electrical power demand worldwide increases dramatically. The environmental pressure forces the development of renewable energy technologies in order to reduce pollutions resulting from burning fossil fuels. One of many initiatives is to popularize the usage of the electrical vehicle. A key element in all modern electrical vehicles is a power inverter.

A power electronics inverter is designed to convert DC power stored in the battery to AC power, which can be used to supply an electrical machine for the torque production. High efficiency inverters play a role in increasing the mileage of an electrical vehicle for a given battery capacity. The emergence of wide bandgap semiconductors, such as silicon carbide (SiC), is challenging the market domination of silicon-based power devices. Due to its high critical electric field, low switching and conduction losses, SiC devices have become of great interest in both academia and industry. In [1], Franke has compared the total power losses for three different 1200V/6A devices: SiC BJT, SiC JEFT and Si IGBT. Both SiC devices show lower total losses than the Si IGBT and reduced temperature dependencies. Moreover, SiC BJTs offer the lowest losses although it requires a DC base current to keep it conducting. In [2], the switching power losses has been compared between three types of 1200V/20A power devices: SiC MOSFET, SiC JEFT and Si IGBT. The reduction of switching losses is evaluated, with the lowest loss achieved by SiC-based devices. In terms of the continuous operation performance, a DC/DC power converter using SiC and Si devices has been built for the test in [3, 4]. The loss was reduced by 50.8% with the SiC MOSFET converter compared with Si IGBT's. In [5-8], the power converters using SiC BJT as the main switch demonstrated higher converter efficiency than its SiC JFET, Si MOSFET and Si IGBT counterparts. At very high current and voltage, SiC BJTs exploit the advantages of low conduction losses due to the absence of large drift resistance which cannot be avoided by a MOSFET device. Therefore, it is well suited to an inverter application which is used in the electrical vehicle to control high currents at high voltages. However, the power losses of a SiC BJT driver are highest among those devices. Therefore, a high efficiency base driver design is an important consideration to achieve the very highest level of efficiency in power converters and in particular to fully realise the advantages of SiC device technologies.

In this chapter, modern power semiconductor devices are discussed from the device structure, operating principle, material properties and drive technology. Device power losses and driver

complexity are compared between different types of the power devices. Improved performances introduced by new material properties are addressed, along with different structural parameters.

1.1 Aim and Objectives

With the emergence of the wide bandgap material such as SiC, power devices based on these materials have demonstrated faster switching performance, lower conduction losses and higher junction temperature capability compared to their established Silicon counterparts. Of the various device types realised in SiC, BJTs have experimentally shown to offer lower device loss than other SiC-based power devices for high power applications. Given their lower loss and high junction temperature characteristics, SiC BJTs have been identified as suitable for applications in harsh environments and/or environments in which cooling cannot readily be achieved. However, the base drive losses for a SiC BJT device are much higher than an equivalent MOSFET or IGBT due to the requirement for continuous base current to be supplied to the base terminal. This base drive issue has been recognised as a major shortcoming of SiC BJTs. This thesis aims to tackle this shortcoming in order to make SiC BJTs a more attractive candidate technology for next-generation power converters. To this end, the aims and objectives of the research reported in this thesis are:

- To provide an in-depth understanding of the impact of base drive behaviour on the performance and competitiveness of SiC BJTs.
- Propose and design novel base drive circuits for SiC BJTs which are capable of high efficiency operation.
- To demonstrate experimentally improved performance of representative SiC BJT based switching converters.
- To provide design guidelines for energy recovery base drive and active base drive circuits which allow competitive SiC BJT converters to be realised.

1.2 Bipolar Junction Transistor

A simplified one dimensional structure of a Bipolar Junction Transistor (BJT) is shown in Figure 1-1[9]. This is used to explain the operation principle of the device. The structure consists of three layers, doped in alternate n type and p type layers, forming a three terminal device. These layers and their electrical contacts are termed as Emitter (E), Base (B) and

Collector (C). Two junctions, J_1 and J_2, are formed between different doping layers. The doping profile from p-type to n-type can be either abrupt or linearly graded, depending of the process technology used. The doping type changing over a very small distance, compared to the spatial extent of the depletion region, is defined as an abrupt junction. It is also called step junction. A linearly graded function is more realistic for the junction as the doping profile changes gradually. The majority carries on one side intend to diffuse across the junction to the opposite side when they are contacted. Due to this process, a space charge region (also known as depletion layer) is created on either side of the interface between p-doped and n-dope region. This region consists of fixed the ionized impurities which are not able to move. However, due to the removal of free carriers they are not electrically neutral and an electric field exists.

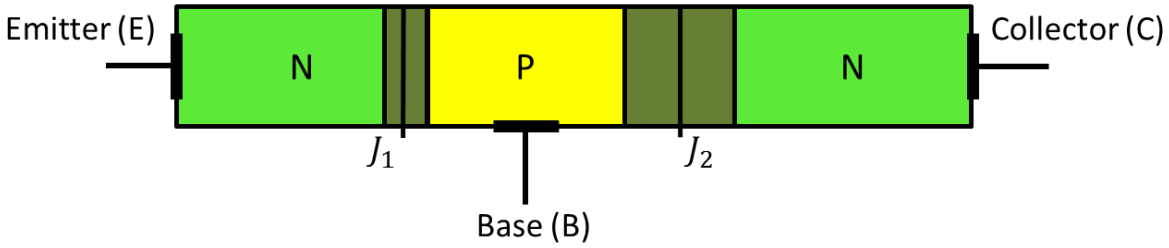


Figure 1-1 One dimensional model of a BJT

1.2.1 Forward active operation

Figure 1-2 shows a common base configured NPN transistor biased in the forward active mode together with the energy band diagram. The negative voltage applied to the emitter junction forward biases the emitter-base junction and the positive bias applied to the collector puts the collector-base junction in reverse bias. As illustrated by the energy band diagram in Figure 1-2, due to the forward biased base-emitter junction, electrons are injected into the base region causing current I_{ne} and holes are injected from the base to the emitter causing current I_{pe}. Due to the relatively low doping concentration, the minority carriers injected into the base, electrons, are mostly swept into the collector which generates current I_{nc}, rather than recombining in the base region; this due to two reasons: in order to increase current gain the base layer is designed to be very thin compared with the electron diffusion length and that the emitter doping concentration is significantly higher than that of the base to maximise injection efficiency. Since holes thermally generated in the collector-base space charge region

is low, the drift current I_{pc} can be neglected. Therefore, three terminal currents of the BJT working in forward active region are given by:

$$I_B = -I_C - I_E = -I_{nc} + I_{ne} + I_{pe} \quad \textbf{1-1}$$

Where I_B, I_C and I_E are base, collector and emitter current.

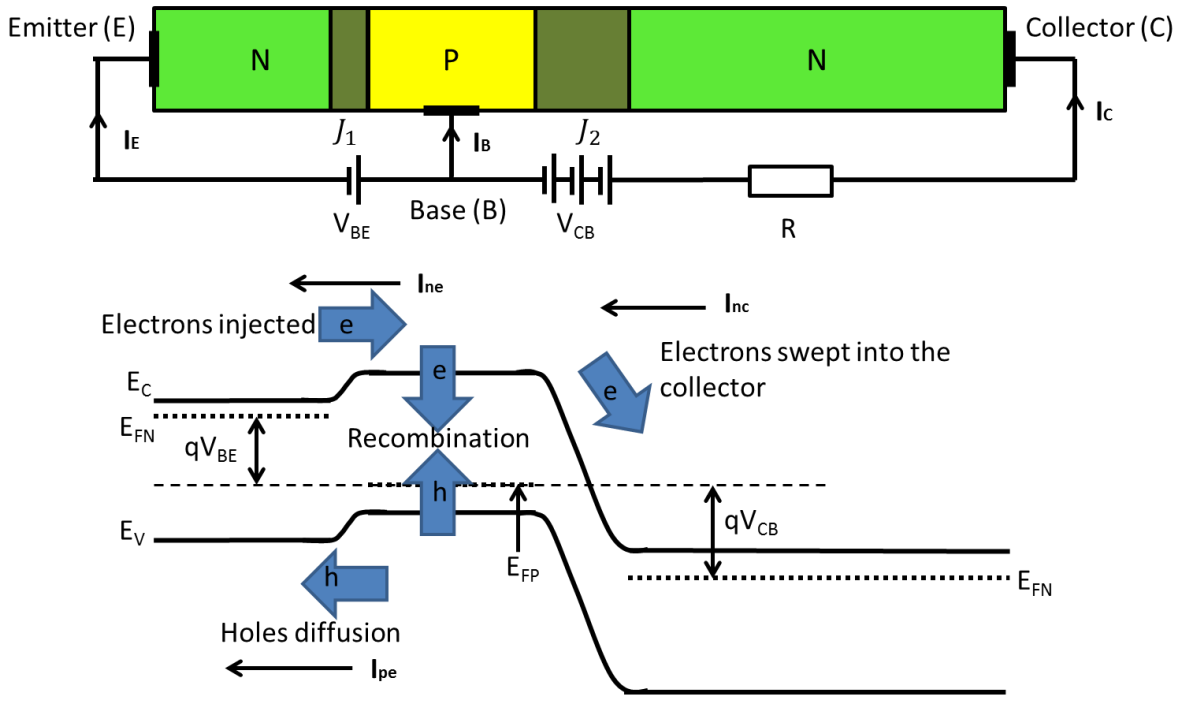


Figure 1-2 Common-base configuration [9]

In the majority power electronic applications, the BJT is connected in a common-emitter configuration, as shown in Figure 1-3. Unlike the common base, V_{BE} and V_{CE} are all referencing to the emitter rather than the base terminal. In this configuration the collector-base junction V_{CB}, is not directly controlled, however the operation principle of the common base configuration still applies.

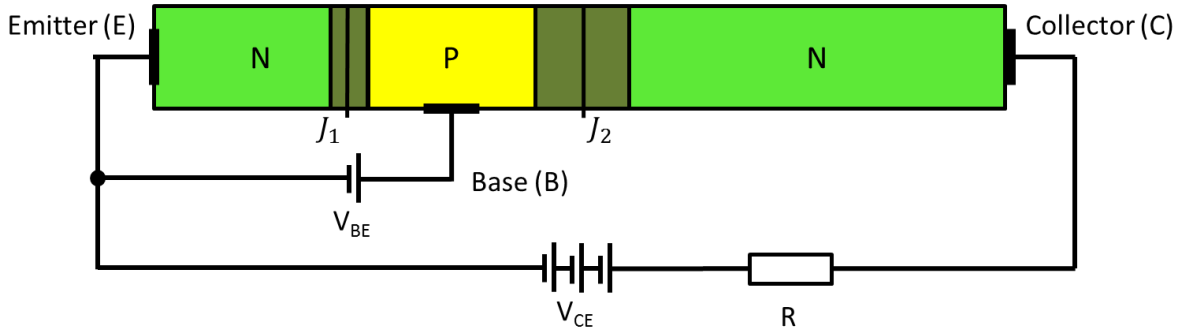


Figure 1-3 Common-emitter configuration [9]

The output current voltage (I-V) characteristic for a common-emitter BJT is shown in Figure 1-4. As the collector voltage is increased, a positive base current indicates that base-emitter junction is forward biased in the first quadrant, or in the saturation region. As the collector voltage exceeds the base potential, the base-collect junction becomes reverse biased and the BJT is operated in the forward active region, as shown in Figure 1-4. When the device enters the forward active region, current saturates. However, with increasing collector-emitter voltage, current slowly increased, which is termed as the Early Effect. With the increasing collector voltage, the depletion region formed at J_2 extends and effectively reduces the base width. This has two consequences. Firstly, carriers entering the base-collector electric field are swept out at a faster rate and secondly, due to the reduced effective base width recombination is reduced and increase gain as carriers leaving the base region increase. These two factors effectively increase the transistor gain with applied voltage and cause an increase in collector current.

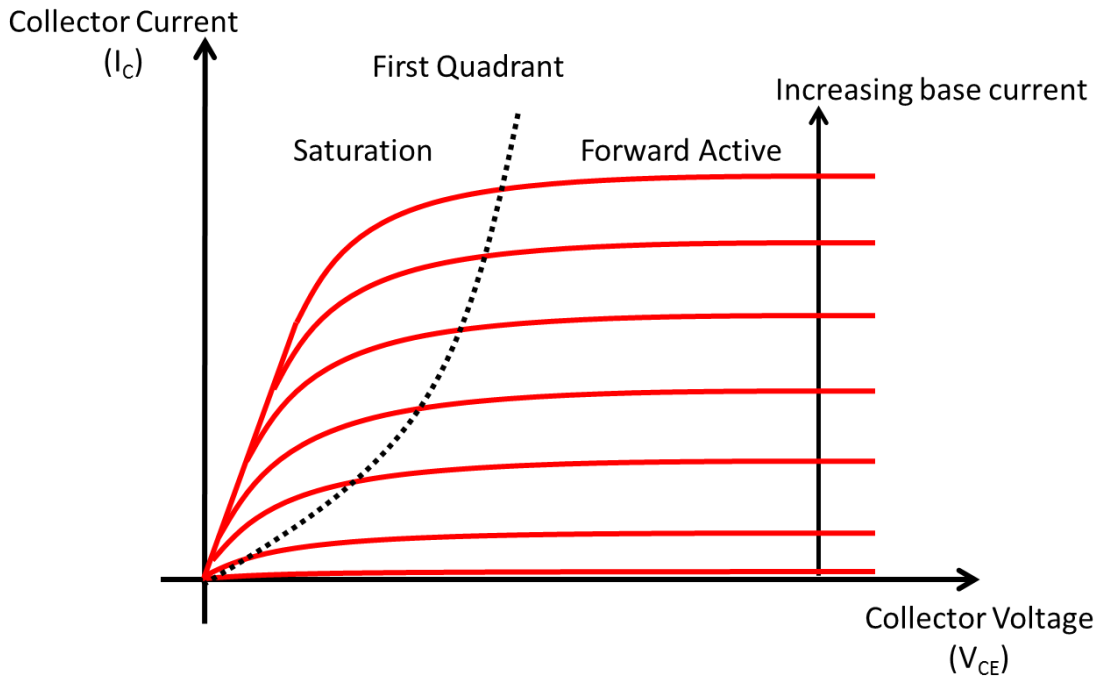


Figure 1-4 I-V characteristic of the BJT in common-emitter configuration [9]

When the BJT is working in the active region, excess carrier charges are stored in the base, termed as Q_F and given by:

$$\tau_F = \frac{Q_F}{I_C} \qquad \textbf{1-2}$$

Where τ_F is the forward transit time. Its accurate value must be measured from the experiment for a specific device. Q_F has to be removed from the base prior to turning off the device. Therefore, the switching speed is slowed down due to large stored excess carrier charges in base.

The common-emitter current gain is defined by the input base current I_B and output collector current I_C:

$$\beta = \frac{I_C}{I_B} \qquad \textbf{1-3}$$

Several factors should be noted when fabricating the BJT in order to achieve a high current gain β, such as the space charge recombination rate and surface recombination. Both of the recombination mechanisms reduce the number of electrons coming across the base to arrive

at the collector. Their influences on the current gain have been analysed and compared under different collector current densities [10].

1.2.2 Voltage blocking characteristics

The basic BJT structure contains two p-n diodes constructed back-to-back in series. Hence, the BJT only conducts in first and third quadrants. When the voltage reaches the breakdown voltage, the leakage current through the BJT starts to rise dramatically as shown in Figure 1-5. The third quadrant breakdown voltage is lower than that in the first quadrant in a high voltage structure due the asymmetrical design, which will be elaborated on the next section.

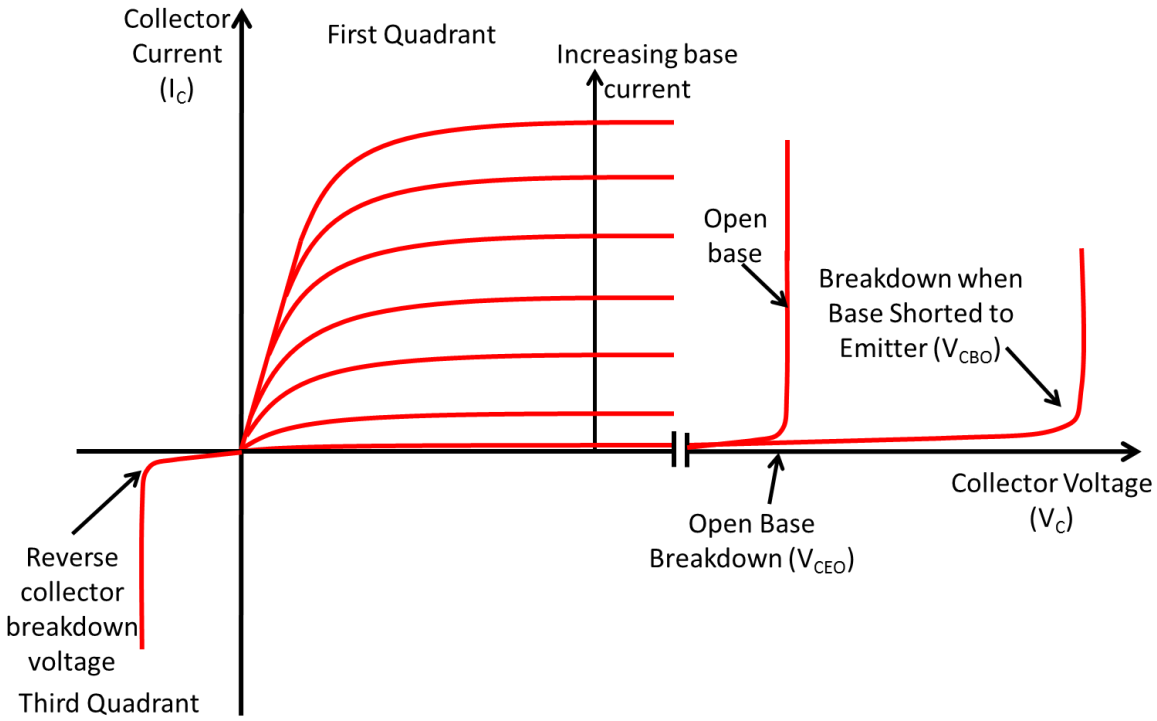


Figure 1-5 Typical electrical BJT characteristic [9]

When operated in the first quadrant, breakdown voltages are dependent on the configuration of the BJT. When the emitter and base are shorted and positive voltage is added on the collector, the device structure can be simplified into a reverse bias diode, as shown in Figure 1-6a. The applied voltage is supported by the space charge region. The spatial variation of the charge density ρ is shown in Figure 1-6b, which penetrates into both the p and n regions of the junction, x_p and x_n respectively. The space charge width W, is the summation of x_p and x_n

and an electric field is generated due to the existence of the uncompensated positive and negative charge at each side of the junction, as shown in Figure 1-6c. Using Poisson's equation, the electric field at each side of the junction can be determined:

$$\frac{dE}{dx} = \frac{-qN_a}{\varepsilon} \qquad -x_p < x < 0$$
$$= \frac{qN_d}{\varepsilon} \qquad 0 < x < x_n \qquad \textbf{1-4}$$

Where N_a and N_d are the acceptor and donor density; ε is the dielectric constant of the semiconductor; q is the magnitude of the electron charge.

Integration from $-x_p$ to x_n, results in the electric field distribution into the n and p side of the junctions:

$$E(x) = \frac{-qN_a(x + x_p)}{\varepsilon} \qquad -x_p < x < 0$$
$$= \frac{qN_d(x - x_n)}{\varepsilon} \qquad 0 < x < x_n \qquad \textbf{1-5}$$

The electric field profile is shown in Figure 1-6c. The peak electric field E(x) occurs at the metallurgical junction (x=0) where the fixed positive and negative charges are at their maximum as indicated by Equation 1-5. Integrating Equation 1-5 from $-x_p$ to x_n obtains the applied bias to the junction voltage V:

$$V = -\int_{-x_p}^{x_n} E(x)dx = \frac{qN_a x_p^2 + qN_d x_n^2}{2\varepsilon} \qquad \textbf{1-6}$$

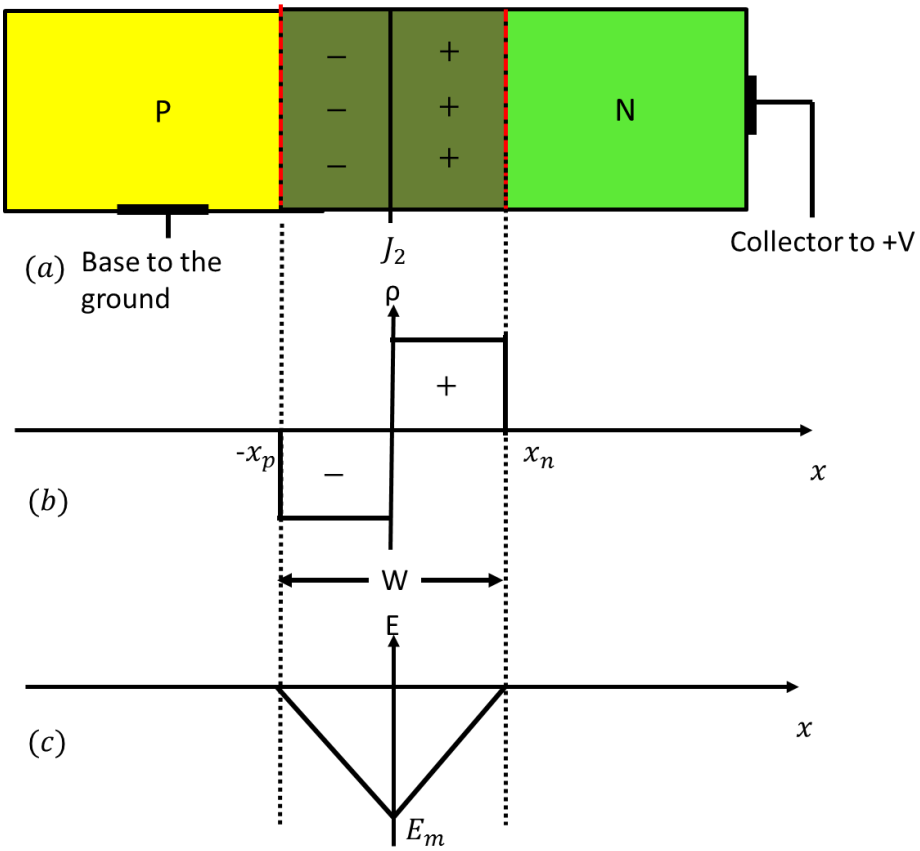


Figure 1-6 Base-emitter shorted breakdown

Due to charge neutrality, the quantity of the positive charges in the depletion region must equal the total negative charges:

$$qN_a x_p = qN_d x_n \qquad \textbf{1-7}$$

When E_m in the space charge region reaches the critical field E_C with an increasing base-emitter voltage, a free electron is accelerated to gain enough kinetic energy to break an electron bond. This impact ionisation generates an electron-hole pair. This newly generated electron is excited to the conduction band from the valence band and enables current flow. Once this process begins to act as a chain, a large current is following through the junction and large power dissipation will destroy the device. Setting E_m=E_C and solving Equations from 1-5 to 1-7 for the breakdown voltage BV_{BD} yields:

$$BV_{BD} = \frac{\varepsilon(N_a + N_d)E_C^2}{2qN_aN_d} \qquad \textbf{1-8}$$

A material with high critical electric field strength can withstand a high breakdown voltage according to their proportional relationship.

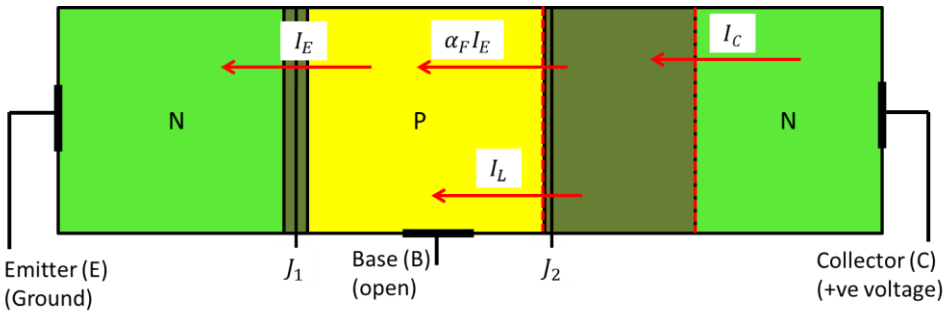


Figure 1-7 Base open breakdown [9]

When the base is open and the emitter is connected to ground as shown in Figure 1-7, leakage current I_L is flowing through the emitter-base junction. Due to the injection of minority carries across the forward biased base-emitter junction (I_E), a collector current equalling $\alpha_F I_E$ is produced, where α_F is referred to as the common-base current gain defined in Equation 1-9. As β_F is intended to be very large (typically 20-70 for SiC BJT), α_F could be as small as unity. Since I_L must flow through the emitter, it will increase the total leakage current from the collector to the emitter. As a result, the breakdown voltage is reduced and the open base breakdown voltage (V_{CEO}) is smaller than the open emitter breakdown voltage (V_{CBO}). When the BJT is working in the third quadrant, the emitter-base junction is reversed biased. J_1 is able to block the reverse voltage due to the p-n junction structure. However, the base-emitter region is characterised for the high current gain, not for the high breakdown voltage.

$$\alpha_F \equiv \frac{I_C}{I_E} = \frac{I_C}{I_B + I_C} = \frac{\beta_F}{1 + \beta_F} \qquad \textbf{1-9}$$

1.3 High voltage transistor

Compared with low voltage devices, high voltage power semiconductor devices are more complicated in their structures. Modifications are made in order to make them capable of blocking high voltage and conducting high current. According to Equation 1-8, the breakdown voltage is inversely proportional to the doping density and thickness, assuming

that the material critical electric field is unchanged. Therefore, to achieve high breakdown voltage the doping concentration in the drift region would need to be reduced and the thickness of it increased to expand the depletion region, as shown in Figure 1-8a [11]. The operation and working modes are identical to the simplified structure in Figure 1-1. Due to the low doping concentration, compared to the base region, the electric field is almost entirely contained within the lightly doped N^- or drift region. Due to the high base doping density, the depletion is confined in a narrow space in the base. Therefore, the width of the base layer can be shortened in high voltage BJT design. As analysed above, reduced base width leads to an increased current gain.

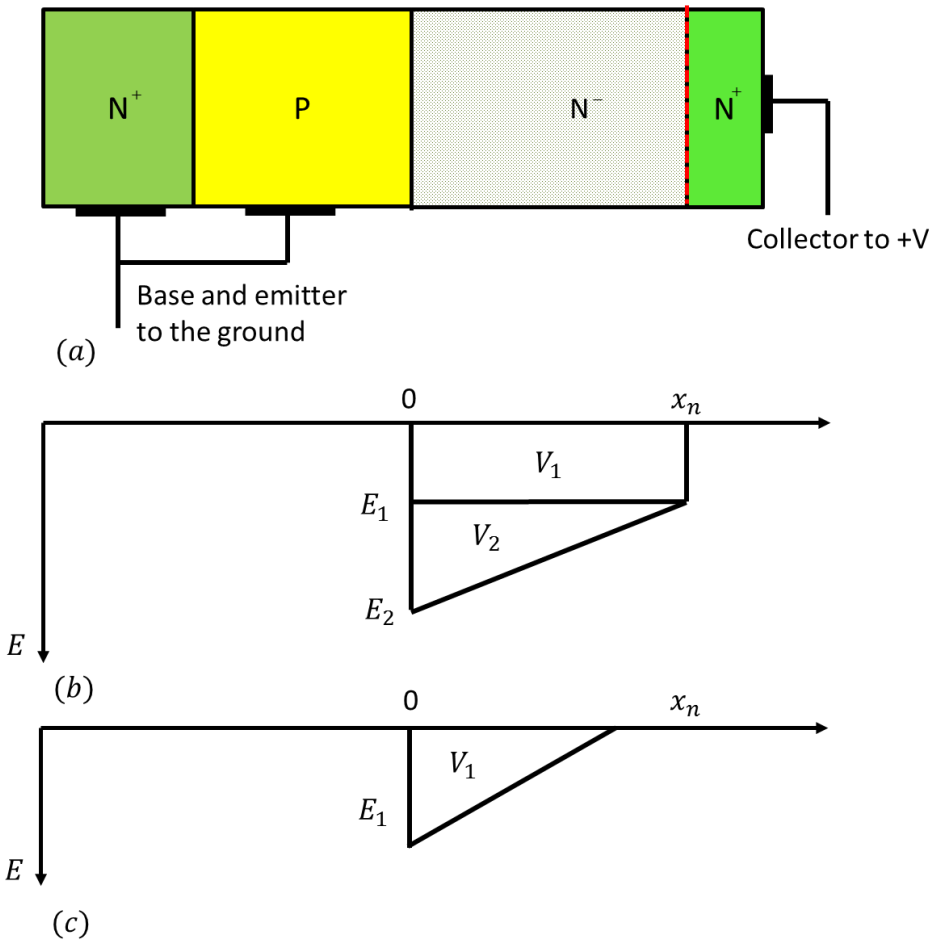


Figure 1-8 A high voltage BJT structure

If the depletion region touches the N^+ layer eventually at the breakdown voltage, it is not able to widen any further since the high doping area restricts its growth. This is termed as a punch-

through (PT) design. The electric field is shown in Figure 1-8b, which describes the electric field of PT structure. As shown, the profile is composed of two components with the peak electric field value of E_1 and E_2. E_2 is due to the ironised donor in the lightly doped drift region N^- and the area of the triangular component represents V_1. The flatten area is due to the heavily doped N^+ which blocks the voltage (V_2) and it stops the depletion region extending further. The total area of the triangular and rectangular represents the breakdown voltage V_1+V_2. If the drift width is longer than the depletion width at the breakdown voltage, it is called non-punch-through (NPT) BJT, as the electric field shown in Figure 1-8c.

When the BJT is turned on, excess charges are injected into the drift region from the forward biased junction, therefore resistance is substantially reduced. This effect is termed as conductivity modulation and increasing the current capability of BJT device compared to unipolar MOSFETs. However, these charges need to be removed during the switching transient, resulting in current tails and increased switching losses, compared to unipolar counterparts.

1.4 SPICE model for a BJT device

Circuit simulation tools such as SPICE are widely used in modern design practice for circuit before committing the design to a hardware prototype. An accurate model of the electrical components and efficient simulation environment can assist designers in observing and understanding critical issues beforehand and increase the likelihood of a successful hardware prototype. In this thesis, simulation models for BJT needs be developed mathematically for accurate and realistic circuit simulation.

One of the BJT models was “Ebers-Moll” model, which was developed in 1954 [12]. That is easy to use and effective in describing the DC performance of a BJT. However, it does not capture many aspect of performance, such as the Early effect and any charge storage effects. These effects are captured in the Gummel-Poon model [13]. Gummel-Poon introduces the Gummel number, which takes many of the subtleties into account that affect collector current. The Gummel-Poon model will be discussed later in this section. The Eber-Moll model decomposes the BJT as two back-to-back diodes sharing a common node. Taking an NPN BJT as an example, I_C is controlled by both V_{BE} and V_{BC} as shown in Figure 1-9. The currents through two junctions are determined by their forward biased voltage. Firstly we assume that $V_{BE} \neq 0$ and $V_{BC} = 0$. Based on the calculations for the collector and base current:

$$I_C = I_S(e^{\frac{qV_{BE}}{kT}} - 1) \quad \textbf{1-10}$$

$$I_B = \frac{I_S}{\beta_F}(e^{\frac{qV_{BE}}{kT}} - 1) \quad \textbf{1-11}$$

Where I_S is defined as the saturation current and kT is the thermal energy.

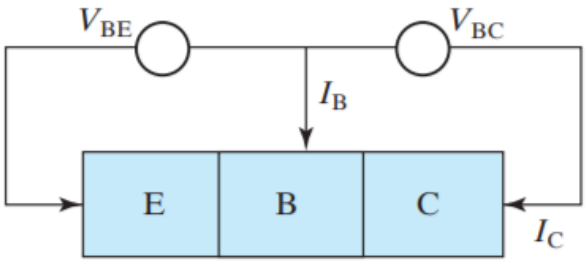


Figure 1-9 npn BJT Eber-Moll model [14]

If the bias condition is reversed, then $V_{BE} = 0$ and $V_{BC} \neq 0$. The function of the emitter and collector has exchanged. Therefore, the terminal currents can be written in the same pattern:

$$I_E = I_S(e^{\frac{qV_{BC}}{kT}} - 1) \quad \textbf{1-12}$$

$$I_B = \frac{I_S}{\beta_R}(e^{\frac{qV_{BC}}{kT}} - 1) \quad \textbf{1-13}$$

$$I_C = -I_E - I_B = -I_S(1 + \frac{1}{\beta_R})(e^{\frac{qV_{BC}}{kT}} - 1) \quad \textbf{1-14}$$

Where β_R is defined as the reverse current gain. Unlike the forward current gain β_F, β_R is intended to be very small due to low doping concentration of the collector. Whenever the BJT is working normally, the equations above can be superimposed:

$$I_C = I_S(e^{\frac{qV_{BE}}{kT}} - 1) - I_S(1 + \frac{1}{\beta_R})(e^{\frac{qV_{BC}}{kT}} - 1) \quad \textbf{1-15}$$

$$I_B = \frac{I_S}{\beta_F}\left(e^{\frac{qV_{BE}}{kT}} - 1\right) + \frac{I_S}{\beta_R}(e^{\frac{qV_{BC}}{kT}} - 1) \quad \textbf{1-16}$$

Apart from the static IV characteristic shown in Figure 1-4, the dynamic performance of a BJT is equally important, especially in a switching application. It requires that a BJT must switch rapidly in order to reduce switching power losses. When the BJT is turned on, the base-emitter junction is forward-biased leading to the excess holes stored in the BJT. Due to the charge neutrality, the excess electrons, Q_F, are equal to the excess holes.

The Gummel-Poon model is widely used in the SPICE because of its advantages in describing dynamic performance. It is fundamentally an Ember-Moll model with additional electrical circuit components to represent the charge storage and parasitic resistances as shown in Figure 1-10. Q_R and Q_F are voltage-dependent capacitors used to describe the excess carrier charges, which is relative to the transit time and collector current. Therefore, the dynamic performance of a BJT can be modelled more accurately. C_{BC} and C_{BE} are the junction depletion capacitances between the base, collector and emitter. C_{CS} is the collector to substrate capacitance. As will be apparent from this electrical model for BJT, fast switching can be achieved by ensuring rapid charging of the various capacitors. This is a key consideration in the design of gate drivers.

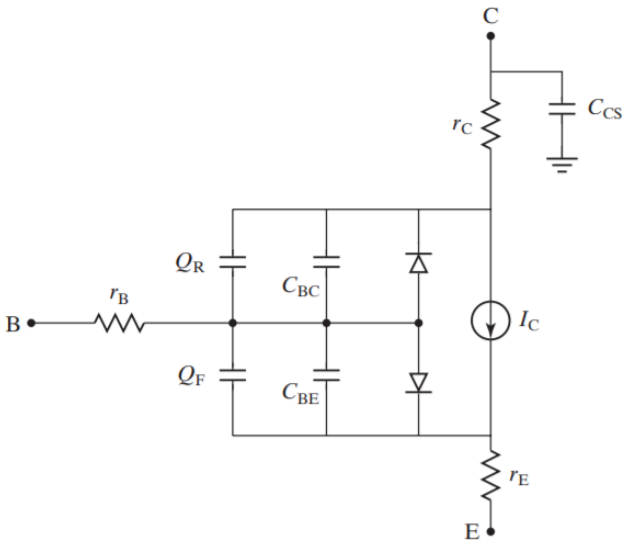


Figure 1-10 Gummel-Poon model for the circuit simulation

Table 1-1 compares the main differences in terms of the parameters in the SPICE model for Si BJT and SiC BJT of comparable ratings. The Si BJT (NPN type) is made by STMicroelectronics (Part number: 2N3771) with maximum collector emitter voltage at 1000V and maximum DC collector current 15A [15, 16]. The SiC BJT is manufactured by

TranSiC (Part number: BT1220AB-P1) with maximum collector emitter voltage at 1200V and maximum DC collector current 20A [17, 18]. The parameters in the table are all critical for accurately modelling the current gain of the devices.

Table 1-1 Main differences in SPICE model for Si and SiC BJT

Parameter	Definition	Initial Value at 27°C	
		Si BJT	SiC BJT
IS	Transport saturation current (I_S)	7.4×10^{-13} (A)	5.2×10^{-48} (A)
BF	Ideal maximum forward beta (β_F)	41.88	74
EG	Energy gap (E_g)	1.11 (eV)	3.2 (eV)

1.5 SiC BJTs and other SiC based power devices

Compared to silicon (Si), silicon carbide (SiC) has different electrical properties, as summarised in Table 1-2 [19-23]. These material properties for SiC make the wide bandgap material more suitable for many aspects of power semiconductor performance and their structural layout when compared to silicon alternatives.

Table 1-2 Electrical properties comparison between Si and 4H-SiC (T=300K)

Electrical Property	Si	4H-SiC
E_g (eV)	1.1	3.26
E_c (MV/cm)	0.3	2.2
v_{sat} (10^7cm/s)	1	2
μ_n (cm^2/Vs)	1430	947
μ_p (cm^2/Vs)	460	140
λ (W/cmK)	1.5	5
ε_r	11.8	10

As a wide energy band gap material, the bandgap (E_g) of SiC is three times higher than its Si counterpart, as shown in Table 1-2. It will influence the saturation current amplitude. The intrinsic carrier concentration, n_i, which is a fundamental semiconductor parameter, is

dependent upon temperature and the energy gap of the material. This parameter defines the thermally generated electron-hole pairs and affects the maximum operational temperature of the devices, as this limits is defined when the intrinsic carrier concentration is equal to the doping density [24, 25]. As shown in Figure 1-11, the intrinsic carrier concentration of SiC is much lower than Si and remains lower over the temperature range. Due to this property, SiC is more suitable than Si material for high temperature application [10] and the maximum junction temperatures of SiC is up to 350ºC [26]. Apart from the intrinsic concentration, the high thermal conductivity (ƛ) allows SiC devices to dissipate heat faster from the junction compared with Si, which reduces the size and weight of cooling system.

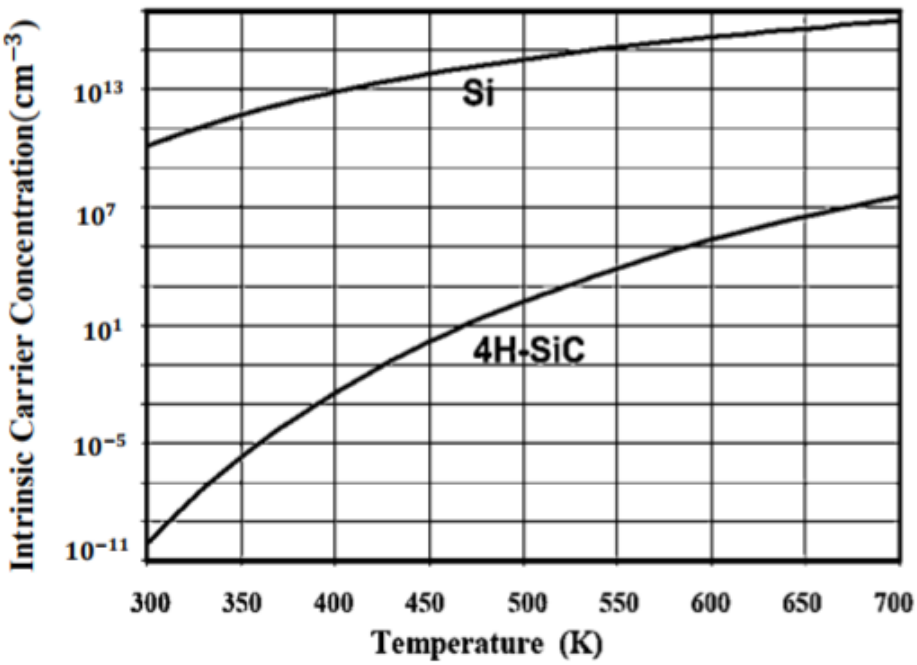


Figure 1-11 Comparison of Si and 4H-SiC intrinsic carrier concentration [27]

Due to high critical electric field strength (E_c), the doping density for each layer in the device can increase under the same breakdown voltage according to Equation 1-8. Therefore SiC power devices can be designed to achieve low on-state resistance, which can in principle be 300 times lower than its Si counterpart [28]. The parameters μ_n and μ_p are termed as electron mobility and hole mobility respectively. The drift current density is proportional to the carrier mobility whereas the resistivity of a semiconductor is inversely proportional to the mobility at a given doping density and temperature. v_{sat} is the saturation velocity, which is the maximum carrier velocity.

A range of SiC-based transistors have been manufactured since the emergence of SiC JFETs in 2008 [29-31]. After overcoming many obstacles, such as material defects [32], SiC MOSFETs gained popularity in 2011 due to their fast switching speeds and simple gate drive design. However, due to the poor thermally grown oxide quality, these devices have been shown to suffer threshold voltage instability at high ambient temperatures [33]. Both unipolar devices, SiC JFETs and SiC MOSFETs, have shown non-linear on-state resistance increase at high junction temperatures [3] due to various thermal coefficients for different layers [34]. In comparison, SiC BJTs exhibit virtually temperature-independent switching performance and low switching losses [3] due to a low level of stored charges within the device. Compared with the commonly commercialised SiC Schottky diode, three-terminal power device fabrication cost is much higher due to the limited wafer size [35].

A cross-section of a NPN vertical SiC BJT is shown in Figure 1-12. A 4H-SiC version on this structure shows a breakdown voltage of approximately 600V [36]. A lightly doped drift region n^- is sandwiched between the base and collector layers in increase breakdown voltage. Due to the high critical electric field strength, the base doping can be very high, reducing the base width. This increases the transistor gain and simplifies the base drive circuit.

A multistep junction termination extension (MJTE) is used for the base-collector junction to improve the blocking capability [37]. Due to lightly doped drift region, the depletion between the base and collector junction predominantly extents into the collector side operated in the off state. Compared with the traditional implanted emitter Si BJT, the SiC structure uses an epitaxial growth and etch process due to the low diffusion coefficient and activation energies of silicon carbide dopants [36].

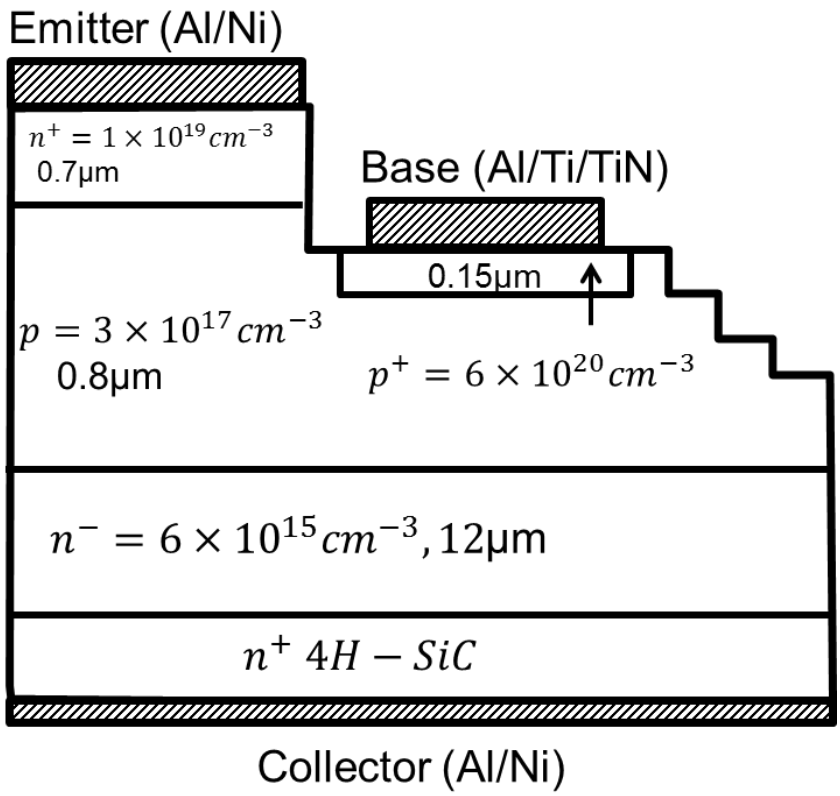


Figure 1-12 4H-SiC BJT cross-section [36]

1.6 Alternative power device structures in SiC

In addition to the power BJT structure, alternative power devices have been designed and applied in industry with different characteristics. The most basic power device structure is a diode in which one-way current conduction is passively controlled by the direction and magnitude of the applied voltage. Beside traditional pn junction diodes structure, various diode structures have been proposed in order to achieve different voltage-current characteristics, such as Zener diode [38, 39], PIN diode [40], photodiode [41] and Schottky diode [42, 43]. Generally, in power electronic applications only Schottky diodes are widely used due to the lower knee voltage, compared to the PiN counter parts and close to zero switching losses.

I. MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors)

A vertical power MOSFET design is shown in Figure 1-13a. As shown, the device is built around an n- drift region of sufficient thickness and doping concentration to achieve the voltage rating of the device. The source and drain terminals are formed with n+ type regions

to provide low ohmic contact to the structure. The cathode cell is formed with a p type region where the n-channel will be formed during the on-state. It is important to note that this region would be connected to ground via a p+ contact to avoid turning on the parasitic transistor and enhance the structures safe operating area.

If a positive potential is applied to the drain and the source electrode is held at ground, the application of a flat band voltage on gate metal gives zero-band bending at p body interface as shown in the energy band diagram in Figure 1-13b. Since there is no net electric field existing in the interface area, the energy band is flat. Increasing the gate voltage, the conduction band (E_c) and valence band (E_v) are bending due to the electric field generated at the SiO_2 and p body interface. Depletion region is formed and full of negative charges. If the gate voltage continues increasing above threshold voltage, the conduction band is pulled close to the fermi level (E_F), more states will be occupied by the electrons in this band which forms an inversion layer with high conductivity and low resistance on the surface of the p body region. This allows electrons to flow from source to drain providing a two dimensional current flow path (I_D), as shown in Figure 1-13a.

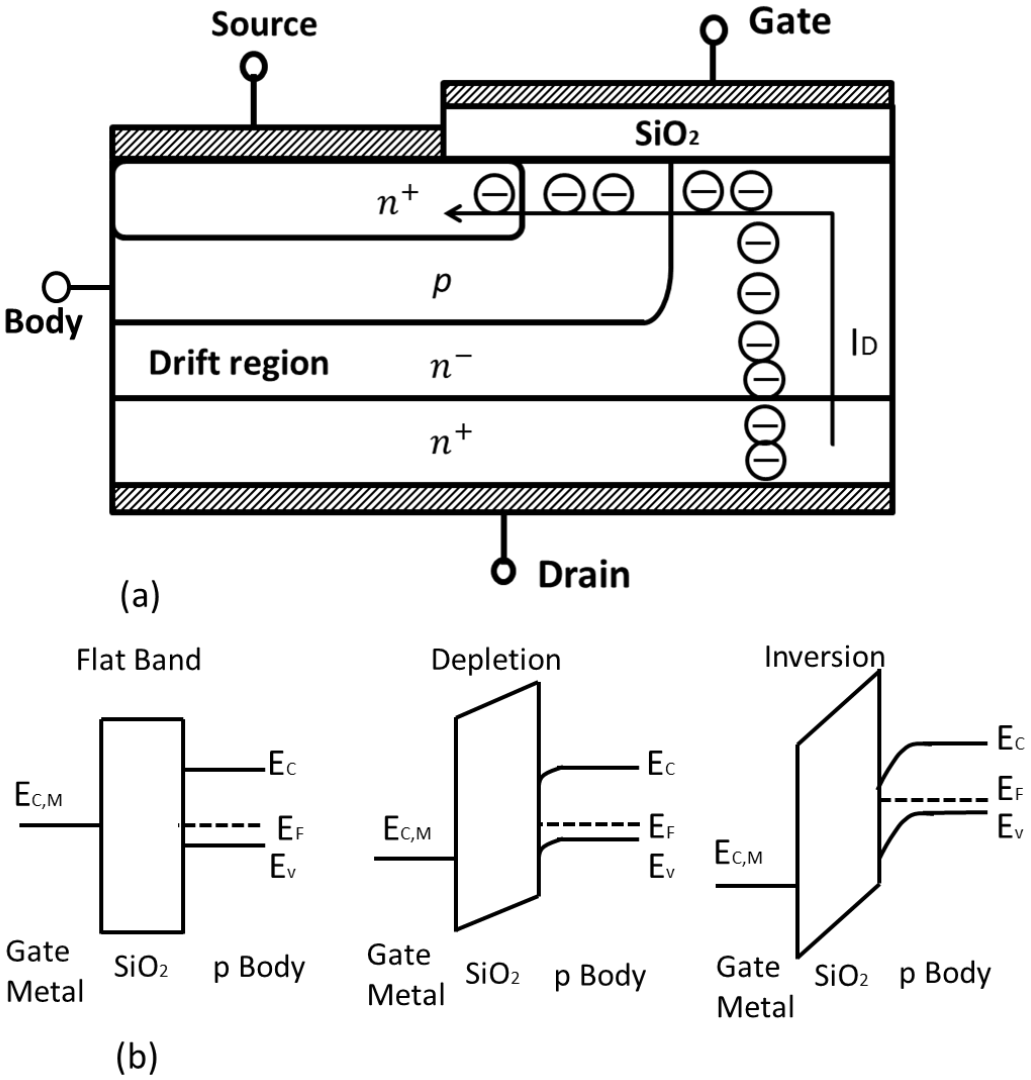


Figure 1-13 Vertical MOSFETs cross sectional view

II. IGBTs (Insulated Gate Bipolar Transistors)

The vertical cross section of an IGBT is shown in Figure 1-14, like the MOSFET, it is a three terminals and four layers device. The only difference between the two structures is the additional p+ anode at the backside of the IGBT. Like the power MOSFET, gate voltage controls the formation of an inversion layer on the surface of the p type semiconductor underneath the SiO_2 gate dielectric. When the applied voltage exceeds threshold voltage, the n-channel effectively connects the n^+ and drain drift n^- region. As the anode potential is increased beyond the knee voltage of the n buffer/p anode layers, holes are injected into the

n- drift region, and reduced the layer resistance by the conductivity modulation process, as shown in Figure 1-14.

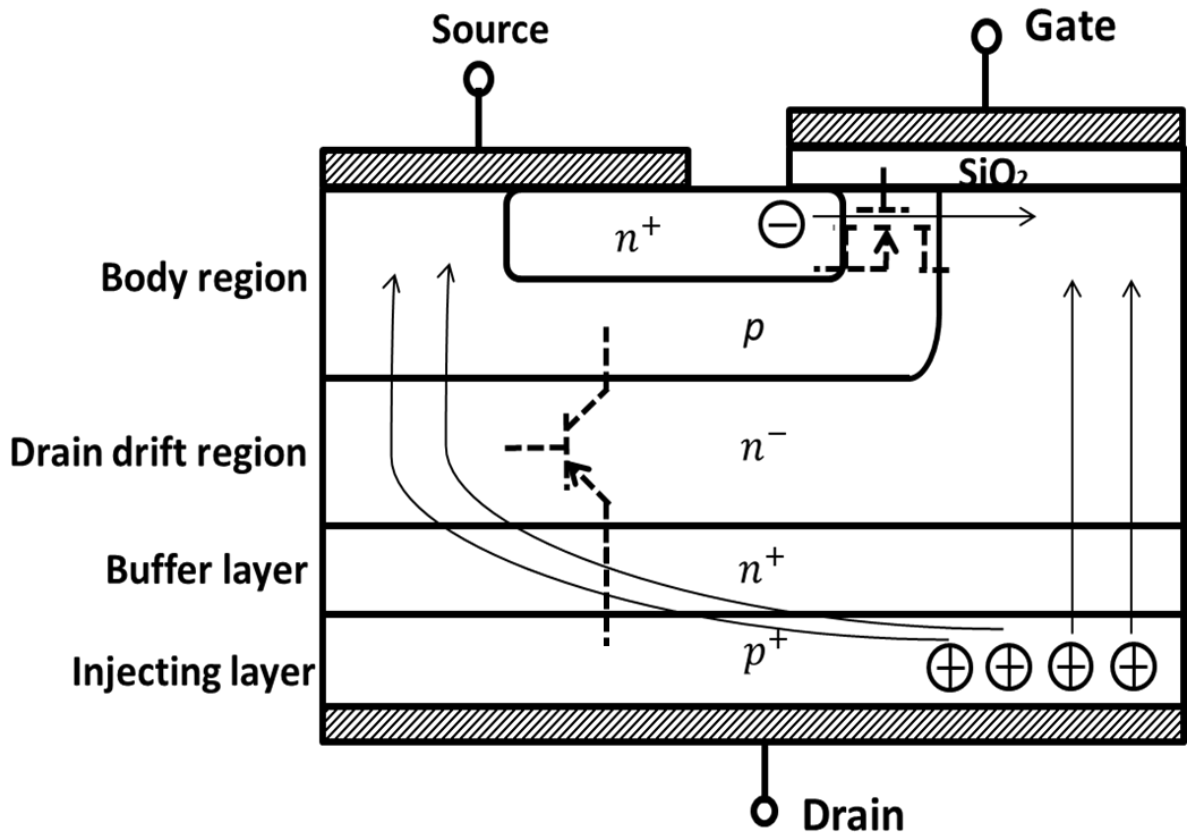
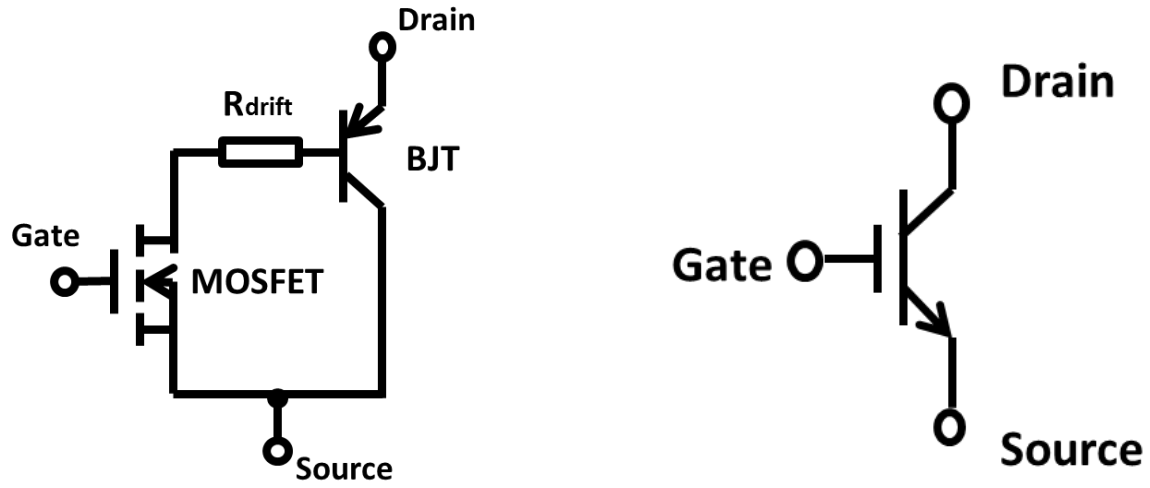


Figure 1-14 IGBT vertical cross section view

Depending upon the gain of the transistor and the density of MOSFET cathode cells, the IGBT can be considered either as a MOSFET in series with a P-iN diode or a transistor driven by a MOSFET. Traditionally, in terms of SPICE modelling the device is considered as the latter, as shown in Figure 1-15a, therefore its operation principle is identical to the BJTs operation principles, as described above. Since IGBT combines the operational principles of both the BJT and MOSFET the device exhibits high input impedance and low effective on-state resistance under high current operation. However, compared to MOSFETs, the IGBT would exhibit a knee voltage which will be dependent upon the band gap of the semiconductor used, ~3V for silicon carbide, and that switching losses would tend to be

higher due to plasma removal/establishment during the turn on/off transients; however this is dependent upon the carrier lifetime and drift region parameters.



(a) (b)

Figure 1-15 (a) IGBT equivalent circuit and (b) circuit symbol

1.7 Comparison of device technology

1.7.1 Power losses comparison

The power losses of the power devices are critical for the decision making when designing a converter for a specific application. The power consumptions of a power device directly influence the system efficiency, cooling system size and control strategy. In terms of device losses, it composes of two components, on-state and switching power loss. Different device technologies and material systems have specific advantages and disadvantages which are dependent upon the operation states.

In order to compare power losses accurately, test condition and methodology must be identical. The switching power losses of power semiconductor devices are conventionally performed by the double pulse test as shown in Figure 1-16. The switch can be a MOSFET, IGBT or a BJT, which is used as an example in this section. A base current I_B is provided to switch the BJT from its blocking to on-state. A high voltage source, V_{DC}, is used to supply the energy required by an inductive load and stress the BJT when it is turned off. A free-wheeling diode (D) is used to clamp the voltage and maintain the load current I_o when the BJT is turned off. The time constant of the inductive load is designed to be much larger than

the switching period so that it can be assumed as a constant current source during the switching process.

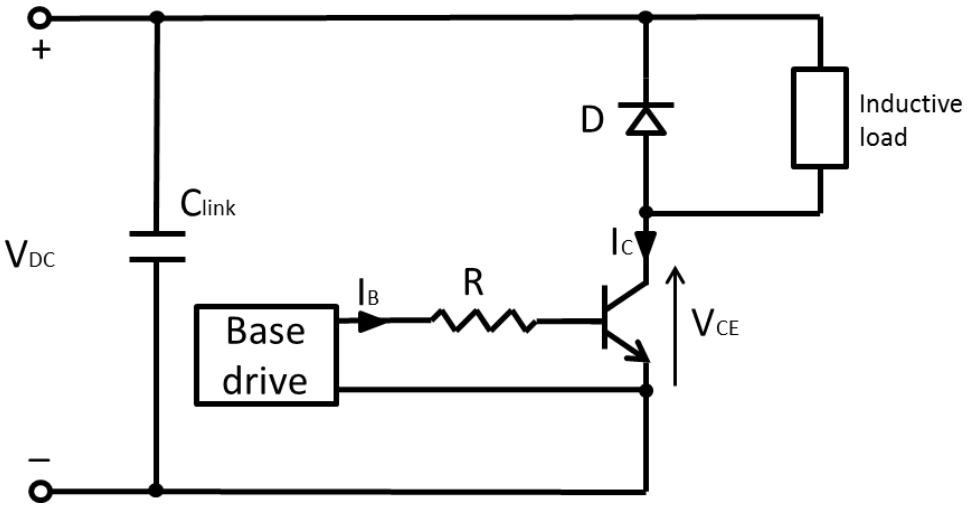


Figure 1-16 Double pulse test with an inductive load

Figure 1-17 shows a simplified turn-on transient of a BJT showing the base current (I_B), collector current (I_C) and collector-emitter voltage (V_{CE}) as a function of time. Initially the base-emitter space charge capacitance must be discharged in order to forward bias the base-emitter junction. This manifests itself as a turn-on delay time $t_d(on)$ after the base current rises. Following the discharge, carries are injected into the base and the collector current ($I_C(t)$) increases quickly. After t_{on1}, the collector current equals the load current I_o. The voltage $V_{CE}(t)$ is constant during this period since the diode D is clamping it to V_{DC} and the BJT is working in the active region. During t_{on2}, $V_{CE}(t)$ drops quickly without clamping because there is no current through the diode. When the B-C junction becomes forward biased, the BJT is entering the saturation region in t_{on3}. Since the current gain reduces in this region, the voltage drop rate is slow than previous. At the end of the turn-on process, the BJT is in its conduction mode with a constant on-state voltage, $V_{CE}(sat)$ under constant current I_o.

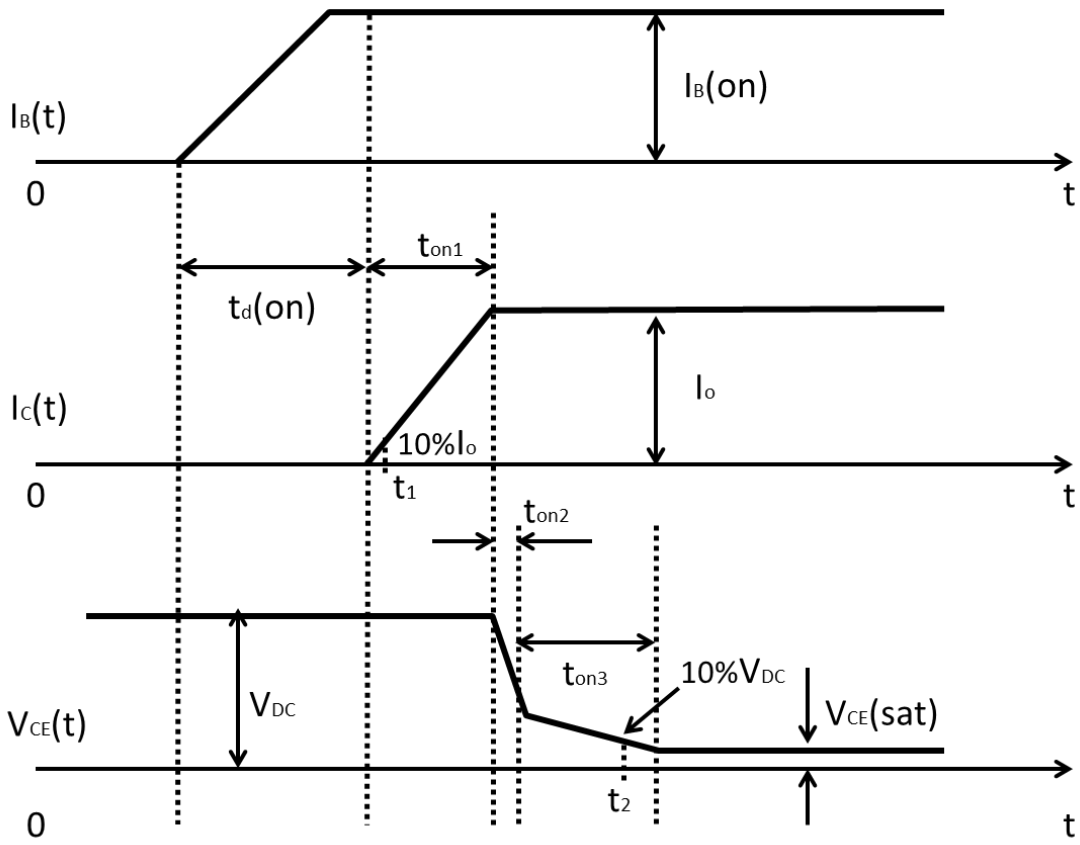


Figure 1-17 BJT turn-on waveforms

The turn-on power loss of the turn-on is defined as:

$$P_{turn-on\ loss} = \frac{1}{t_2 - t_1}\int_{t_1}^{t_2} V_{CE}(t) \times I_C(t)dt \qquad \textbf{1-17}$$

Where t_1 and t_2 are defined by 10% of the maximum collector current and voltage respectively, as shown in Figure 1-17.

The total on-state losses are given by:

$$P_{on-state\ loss} = \frac{1}{T}\int_{0}^{DT} V_{CE}(t) \times I_C(t)dt \qquad \textbf{1-18}$$

Where D is the duty cycle of each switching period T.

When the BJT is conducted, charges are stored in the device, as a result of conductivity modulation; significant charge is stored in the drift region. In order to turn off the device, this

charge must be removed before the device can be turned off. The turn-off waveform of a typical BJT is shown in Figure 1-18. A negative base current is used to speed up this process by removing some of the stored charge from the base region. During t_d(off), part of the excessive charges in the drift region are swept out by the negative base current. Any charges left in the base and drift region can still support the collector current. With this process carrying on, it takes t_{off1} time interval to remove stored charges at the collector and base end. Afterwards, the BJT enters into the active region and V_{CE}(sat) rises quickly. At the end of t_{off2}, the BJT is in cut-off and the current is commutating into the free-wheeling diode. After a time interval $t_{off}3$, charges in the BJT are completely removed by the negative base current and junctions are reverse biased. If the base current transits very quickly into the negative value at the beginning, the charges in the base are removed fast and emitter current goes to zero fast accordingly. There will be stored charges in the drift region at this point. They can only rely on the internal recombination and negative base current when this happens. The removal process would be very long, which creates a current "tail" and increases the turn-off losses inevitably, as shown in Figure 1-19. The turn-off power loss is defined by Equation 1-17 by changing annotation to 'turn-off loss', with the parameters shown in Figure 1-18.

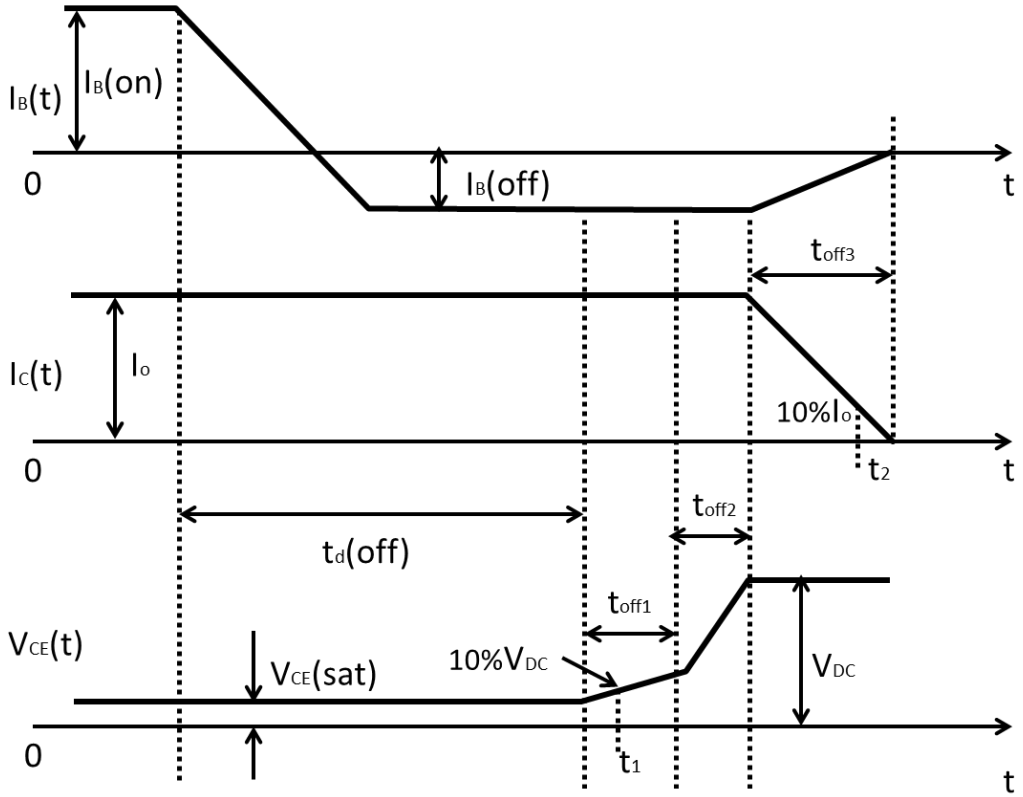


Figure 1-18 BJT turn-off waveforms

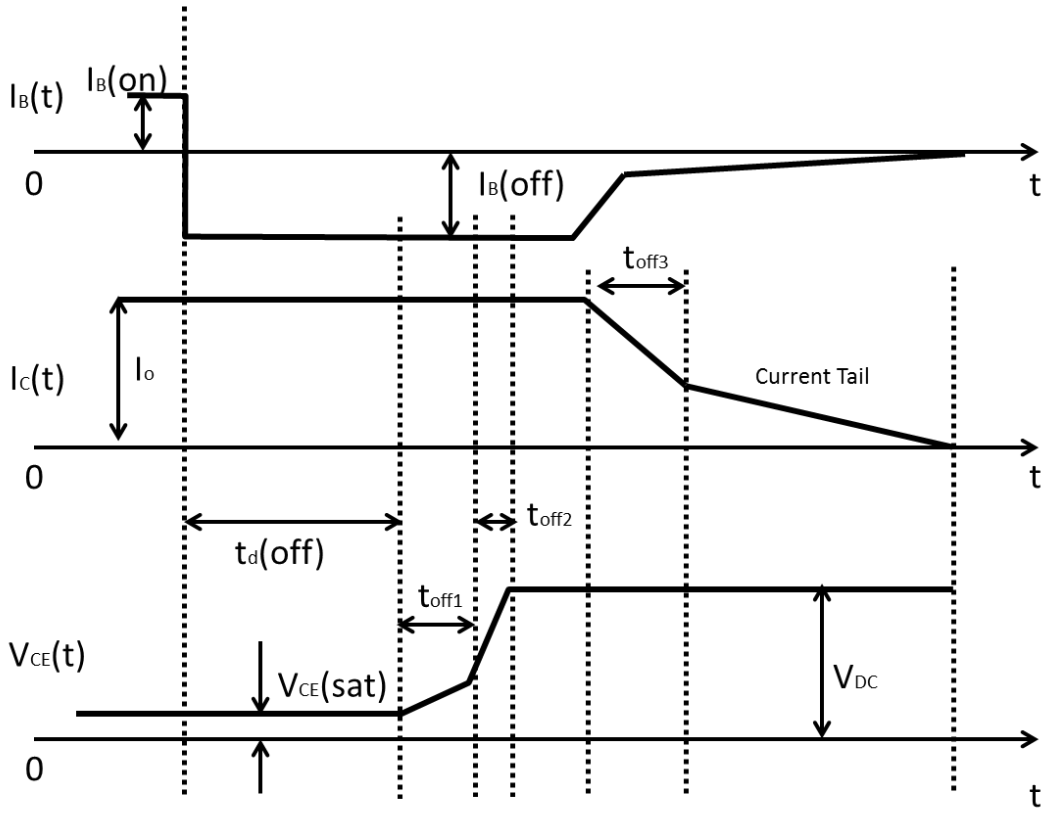


Figure 1-19 BJT turn-off waveforms with the collector current tail

Compared to the unipolar device MOSFET, the BJT and IGBT have to remove excess carriers stored in the drift region before they are completely turned off. As shown in Figure 1-18, $V_{CE}(t)$ is at the maximum value during the carrier removal process. Therefore, high switching off loss is a genuine disadvantage in bipolar device technologies. However, on-state losses of a high-breakdown-voltage MOSFET are higher than the BJT. In order to bear high voltage, the drift region is designed to be large resulting in high on-state resistance. For the BJT and IGBT, the conductivity modulation process significantly reduces the resistance of the n- drift region; therefore their effective on-state resistance is very small. When the BJT is made from SiC, the minority carrier lifetime is very short and drift regions are very thin, when compared to silicon counterparts. That means few charges are stored in the device when it is turned off and the device does not exhibit a current tail. The turn-off loss is reduced significantly and the total switching losses are approximately the same as a SiC MOSFET.

1.7.2 Driver design for power semiconductor devices

1.7.2.1 Gate driver design for the MOSFET

Due to the high input impedance of the MOS gate structure, MOSFET devices are defined as a voltage-controlled device. The gate driver should be able to supply a positive voltage higher than the threshold value during turn-on process and maintain at a constant voltage level during on-state. As the gate drive unit is charging/discharging an effective input gate capacitor, the driver consumes little power which makes the control circuit small and simple. Figure 1-20 shows a generic gate drive design for MOSFETs. In order to control the speed of charging and discharging gate capacitance, a gate resistor R_{gate} is placed between the gate terminal and gate drive unit. The control signal (V_G) is provided from a logic source with low voltage power supply. In order to isolate high voltage (HV) from logic part of the circuit, an isolator unit is used. The voltage supply (V_{DD}) for the isolator and MOSFET gate terminal is usually generated by a Switching Mode Power Supply (SMPS) due to its high efficiency and large insulation voltage. Due to its fast switching frequency when operating, Electromagnetic Compatibility (EMC) must be complied with when designing the PCB layout in the industry. Two BJTs with high current capability are used as a buffer in the drive circuit for high peak current during the turn-on and -off period. A boost capacitor (C) is connected between V_{DD} and source of the MOSFET in order to offset V_{DD}. In this configuration, the gate voltage is always referenced to the source terminal and the high voltage is isolated from the logic part. Therefore, this gate driver is specifically applied for high side MOSFET.

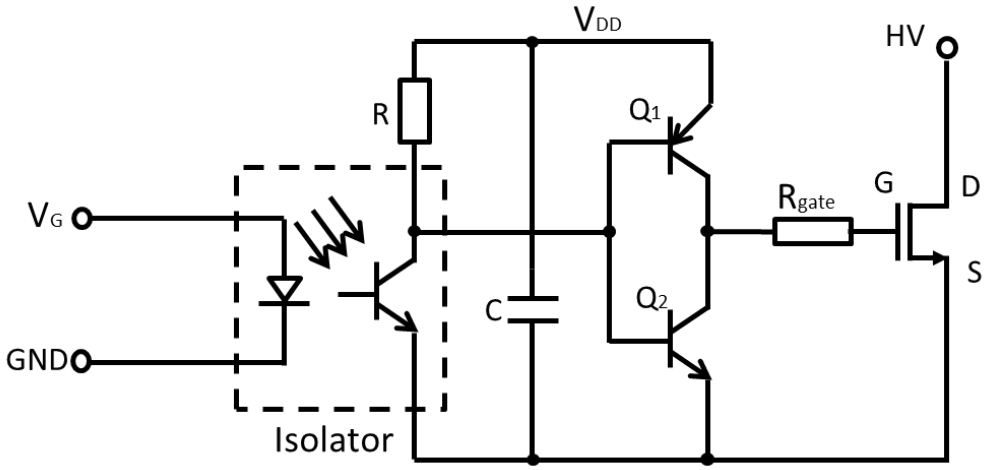
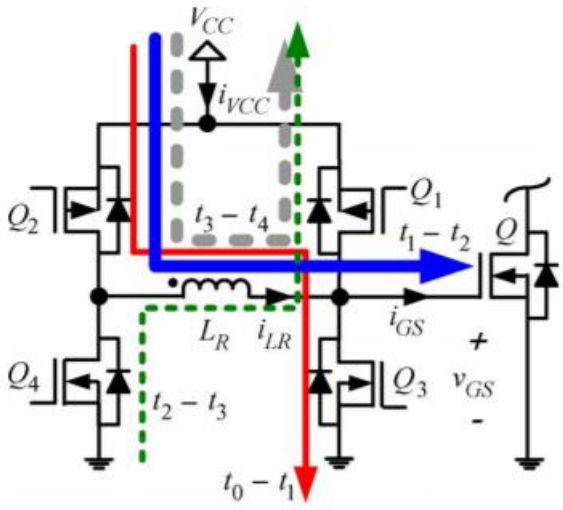
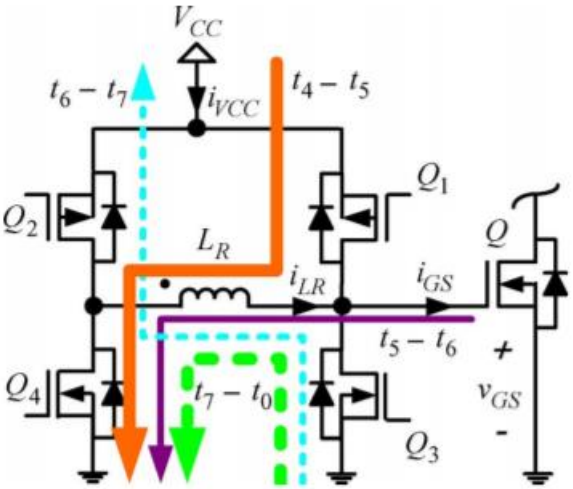


Figure 1-20 Gate driver design for MOSFETs

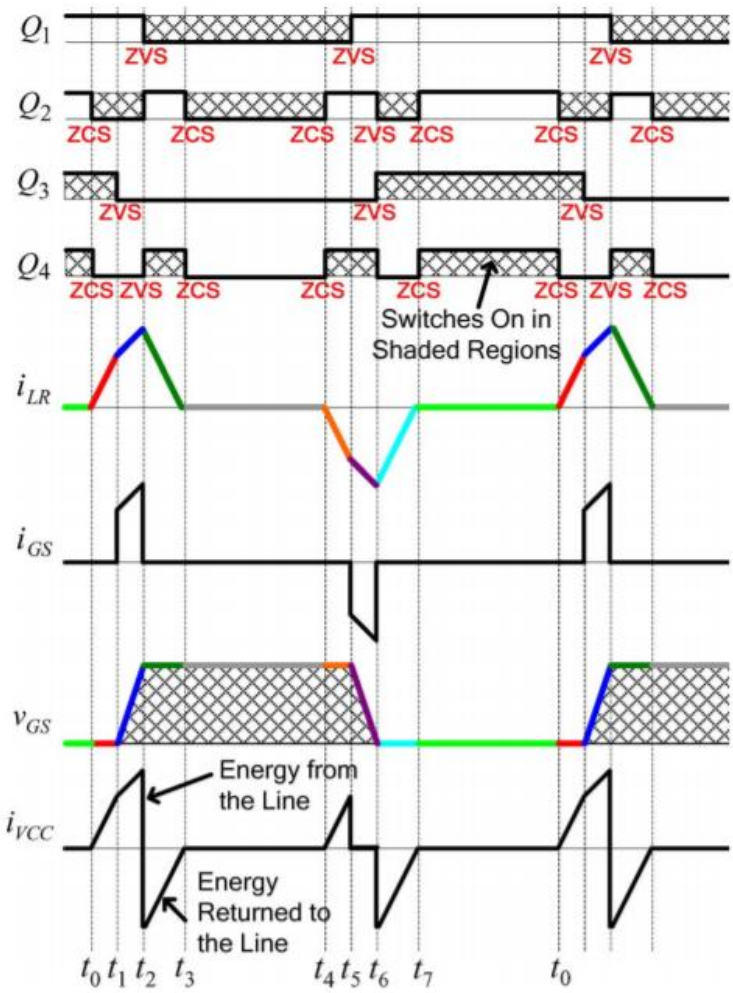
In order to reduce the power loss of a MOSFET driver, a resonant gate driver structure is proposed in [44], which implements the energy recovery concept in the design. The control signals of the proposed circuit and current waveforms are shown in Figure 1-21 [44]. Before turning on the MOSFET (Q, IRF6691), the inductor (L_R) is pre-charged during t_0-t_1. By turning off Q3, the current is re-directed into the gate of MOSFET Q and it turns on MOSFET Q during t_1-t_2 at the peak value of the inductor current. The gate capacitance of MOSFET Q is charged over the threshold rapidly and hence the turn-on loss reduces. During the conduction interval t_2-t_3, the energy in L_R is discharging back to V_{CC}. Before turning off MOSFET Q, L_R is pre-charged with negative current during the interval t_4-t_5 with the current path shown in Figure 1-21 (b). At i_{LR} negative peak value, Q1 is turning off and the energy in the gate capacitance of MOSFET Q is transferred into L_R. During t_6-t_7, the energy in L_R is transferred back to the supply of V_{CC} as the negative i_{VCC} indicates. In this way the energy recovery from L_R and the gate capacitor has been achieved. The experimental results presented in [44] indicate that 51% of the gate energy was recovered with the proposed gate driver for a V_{CC} of 5V. Based on the energy recovery concept and principles, more resonant gate driver designs for either Si or SiC MOSFET have been proposed in [45-47]. The experimental results in [44] demonstrate a reduced driver losses as well as switching losses due to a positive/negative current peak generated by the inductor in the driver.



(a) Turn-on operation



(b) Turn-off operation



(c) Circuit signal waveforms

Figure 1-21 The circuit operation and waveforms (current paths shown in (a) and (b) identified by time interval)

Commercial MOSFET drivers available in the market have various sizes, packages and pin numbers. Since the MOSFET is a voltage controlled device, it is necessary to consider in detail the specifications of the peak current and the output voltage in addition to the continuous sourcing capability. Several widely used commercial drivers are referenced in [48-52]. Taking the IR2110 [48] as an example, the typical connection to power devices is shown in Figure 1-22. It is capable of driving high side and low side MOSFETs with independent output channels (HO and LO). High side floating voltage (V_B) is referenced to the source of high side MOSFET with a boost capacitor connected between floating supply voltage (V_B) and floating offset voltage (V_S).

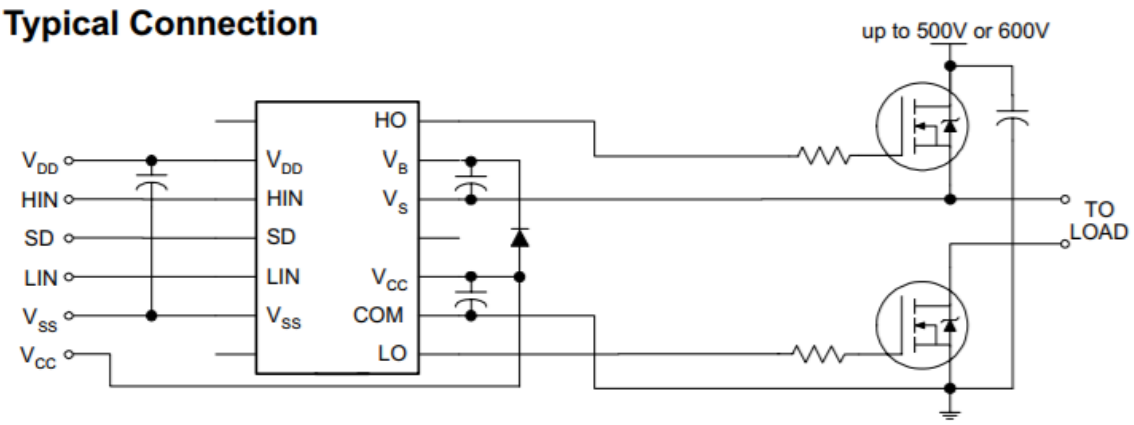


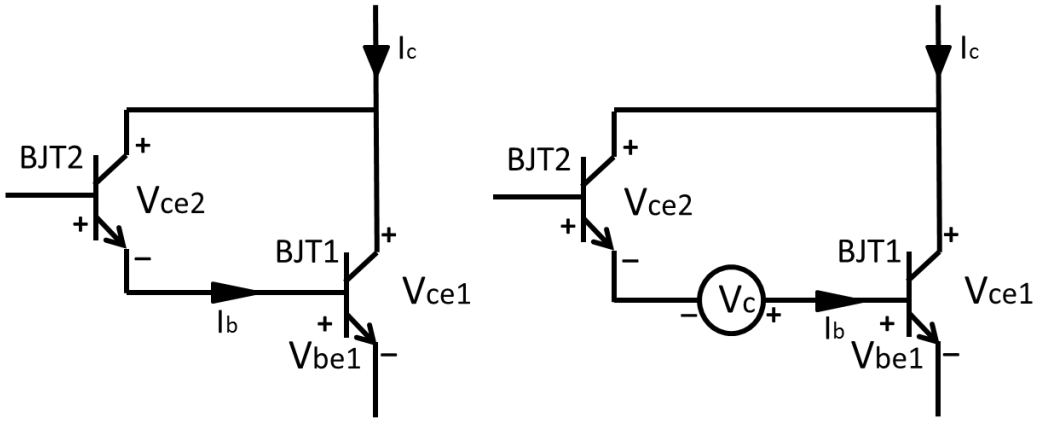
Figure 1-22 Typical connection of a MOSFET drive IC [48]

1.7.2.2 Base driver design for the BJT

Unlike the voltage driven devices, such as MOSFETs and IGBTs, BJTs are current driven power devices. Continuous current needs to be supplied to the base to maintain conduction. Therefore, the driver design is different from those for MOSFET' described above. In order to reduce the switching losses, some additional specifications need to be satisfied for the Si BJT driver designs, such as an overcurrent for fast turn-on, a negative base current and base voltage for fast turn-off, and a clamping circuit to avoid saturating [53].

A widely implemented base drive is called the Darlington configuration which can prevent a Si BJTs from working in the hard saturation mode and provide proportional base current as shown in Figure 1-23a [54]. It has the advantages of high current gain equalling the product of the two Si BJT gains and no current tail since Si BJT1 is always working in the active

region without any excess charges stored in the drift region. However, it suffers high on-state power losses, especially under a high collector current, since V_{ce1} always equals $V_{ce2} + V_{be1}$. A low voltage and high current isolated power supply Vc can be inserted in between two BJTs, as shown Figure 1-23b, in order to reduce the on-state voltage drop across Si BJT1. However, the BJT drive using the compensated Darlington configuration inevitably experiences hard saturation and large turn-off losses due to the current tail issue. Since Si BJTs are replaced by Si MOSFETs and Si IGBTs in most of applications, Si BJT drivers are only developed in academic area and hardly found in the market. The commercialized drivers are usually composed of a totem-pole circuit with a Darlington transistor as its output stage in order to provide high current capability [55, 56].



(a) Conventional Darlington (b) Compensated Darlington

Figure 1-23 Two different structures for Darlington configurations

There are several drive strategies proposed to control Si BJTs. One option is where a base current is supplied and coupled directly with a transformer [57-59]. This option provides galvanic isolation between the low voltage and high voltage sides of the base drive unit, a continuous negative base current can be supplied to achieve for fast turn-off and an overshoot voltage for to speed up the turn-on process. Proportional base drivers have been proposed in [60-62]. Here the base current is proportional to the collector current and is provided by a transformer, this avoids overdriving the BJT and reduces the driver power losses. All these base drive options at bulky are very inefficient and are complex to control.

1.7.3 The base driver design issues for SiC BJTs

BJTs are controlled by providing a continuous DC current into the base terminal. The base driver power loss is much greater than their voltage-controlled counterparts, such as MOSFETs. This is one of the many reasons why BJTs have been replaced for the majority of applications. However, with the emergence of wide band gap semiconductor materials such as SiC, high voltage transistors are starting to appear in the market place as an alternative structure of SiC MOSFET. It is reported that there is an absence of hard conductivity modulation in SiC BJTs, even though the saturation voltage drop between the collector and emitter is very low [63]. Since there is no current tail, the base drive design for SiC BJTs does not need to prevent the BJT from working in hard saturation and neither is it necessary to be too concerned of excess carriers in the drift region. Therefore, traditional silicon BJT drives can be made simpler when designed for SiC BJT as these issues do not exist. For example, SiC BJTs have demonstrated a gain value above 100 and a square Reverse Biased Safe Operating Area (RBSOA) [64, 65]. This means a substantial reduction base current compared to a silicon BJT counterpart rated for the same high voltage. Therefore the base drive design must be modified significantly using different driver topologies, which has become a new challenge for SiC BJTs.

A conventional base drive specifically for a SiC BJT is shown Figure 1-24. The pulse capacitor (C_{pulse}) and R_2 forms low impedance between the base and V_{DD} or ground which will generate current peaks during turn-on and turn-off. The transient speed is mainly dependent on how fast charges can be injected and extracted from the base. Therefore, the current peaks into and out of the base terminal is necessary for fast transients.

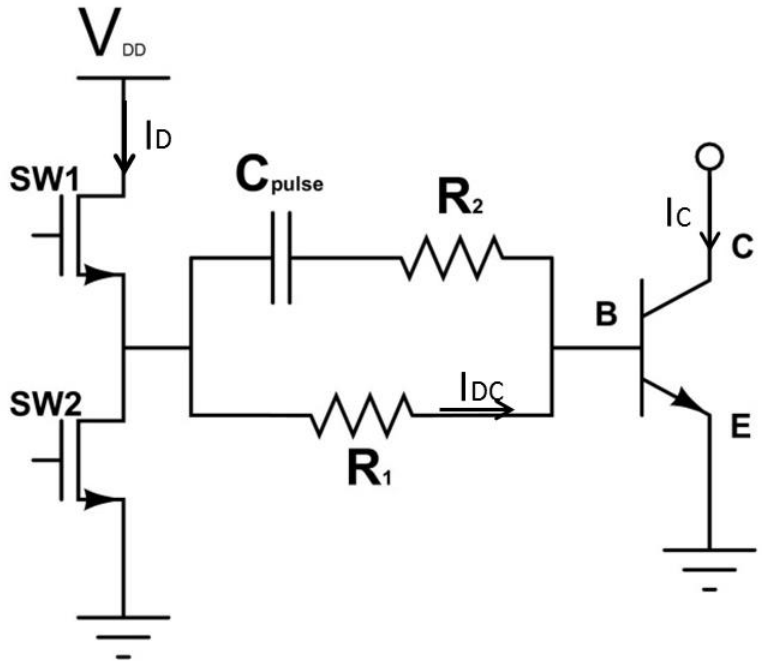


Figure 1-24 A conventional base driver for SiC BJT

A DC current I_{DC} is supplied through resistor R_1 to maintain the base current during the on-state period. The value is defined by Equation 1-19, where β is the current gain of the BJT and I_C is the collector current. Since the fabrication technology is immature and the cost is much higher than the Si based devices, SiC BJTs are not commercialised and manufactured in large volume. Therefore, the tolerance of the current gain is not provided by the supplier. Only the nominal value at different junction temperatures is provided on the datasheet. To ensure that the device does not enter the forward active mode at the maximum junction temperature, the minimum current gain is used from the datasheet. The ratio of I_C and β is multiplied by a factor 1.5 to provide enough margin in order to accommodate the tolerances on the nominal gain values. This factor is provided of x1.5 was drawn from the application note [66] from the device supplier:

$$I_{DC} = 1.5\, {}^{I_C}/_{\beta} \qquad \textbf{1-19}$$

The total power losses of the driver (P_{con_loss}) consist of the losses due to the base resistor (P_R) (Equation 1-21), the base-emitter junction (P_{BE}) (Equation 1-22), the speed up capacitor

($P_{C_{pulse}}$) (Equation 1-23) and the base/emitter junction capacitor ($P_{C_{BE}}$) (Equation 1-24). V_{DD} and I_D are the DC power supply voltage and average current, respectively.

$$P_{con\_loss} = V_{DD} I_D = P_R + P_{BE} + P_{C_{pulse}} + P_{C_{BE}} \quad \textbf{1-20}$$

$$P_R = I_{bRMS}^2 (R_1 + R_{SW1}) \quad \textbf{1-21}$$

Where I_{bRMS}^2 is the RMS value of the base current and R_{SW1} is the on-state resistance of the upper switch (SW1).

$$P_{BE} = I_{b,AV} \cdot V_{be(sat)} \quad \textbf{1-22}$$

Where $I_{b,AV}$ is the average value of the base current and $V_{be(sat)}$ is the voltage drop across the base-emitter junction during the on-state which is approximately 3V for SiC BJTs [17]. The base-emitter junction losses (P_{BE}) are independent of the switching frequency.

The power consumption by charging and discharging the pulse capacitor is dependent on the switching frequency. The power fed by DC source due to C_{pulse} is shown as:

$$P_{C_{pulse}} = C_{pulse} \cdot V_{pulse}^2 \cdot f_s \quad \textbf{1-23}$$

Where V_{pulse} is the voltage across of C_{pulse} during the conduction and f_s is the switching frequency of SW1 and SW2.

The power fed to the base emitter capacitance (C_{BE}) is shown as:

$$P_{C_{BE}} \approx C_{BE} \cdot V_{be(sat)}^2 \cdot f_s \quad \textbf{1-24}$$

Based on the assumption that the base emitter capacitance (C_{BE} (6-16 nF)) is almost constant and small, $P_{C_{BE}}$ can be neglected in the analysis, even at high switching frequencies.

Figure 1-25 shows the power losses audit for a conventional SiC BJT driver shown in Figure 1-24, operating at a 40% duty cycle in the simulation. Various I_{DC} is obtained by changing R_1 in Figure 1-24. The pulse capacitor losses ($P_{C_{pulse}}$), derived from Equation 1-23, increase with the switching frequency whereas the power losses (P_R) and (P_{BE}) are constant. Unlike

P_R and P_{BE}, which is dependent upon base current (I_{DC}), $P_{C_{pulse}}$ increases linearly with the switching frequency. For a low base current such as 0.1A, $P_{C_{pulse}}$ dominates the losses when the switching frequencies are above 80kHz. If the base current was increased to 1.5A, the capacitor power consumption is much lower in the range of 50 -- 200kHz. In order to reduce resistor power losses, the voltage supply (V_{DD}) needs be as low as possible. However, if it is low, the device is more susceptible to voltage fluctuation caused by the coupling of the emitter due to the emitter stray inductance and base-emitter capacitance. Emitter parasitic inductance voltage is dependent on di/dt when the BJT is switching. This voltage change can be coupled to the base terminal through base-emitter capacitance and influence the base current. Furthermore, reducing V_{DD} would increase switching losses as a portion of the fast switching base current is sourced from it. Therefore, a trade-off exists between the base drive losses and switching performance of the BJT in the conventional base driver design.

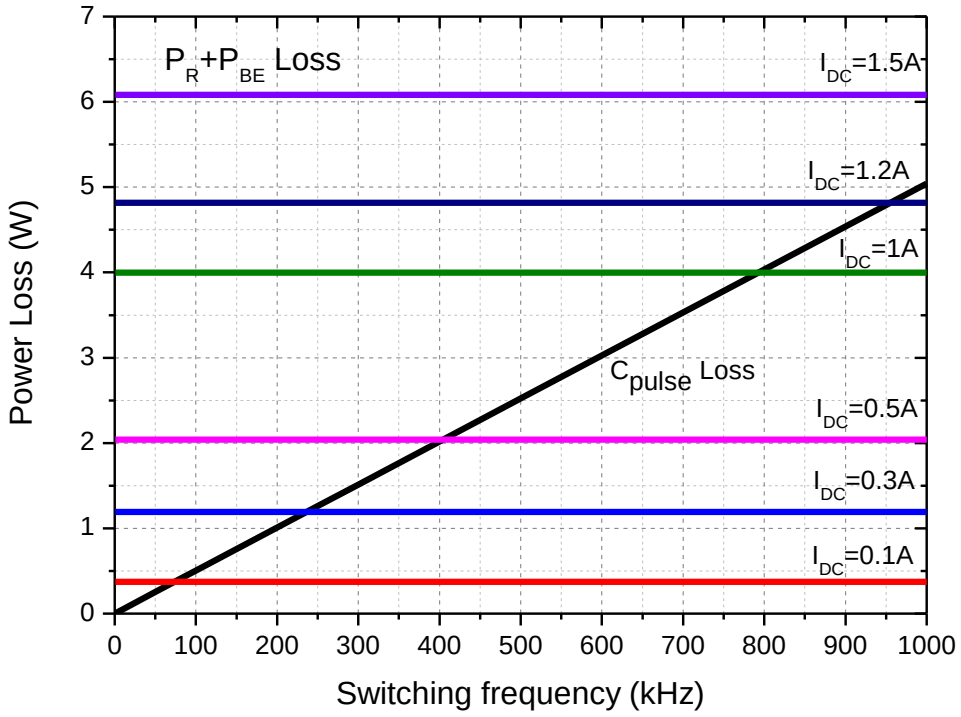
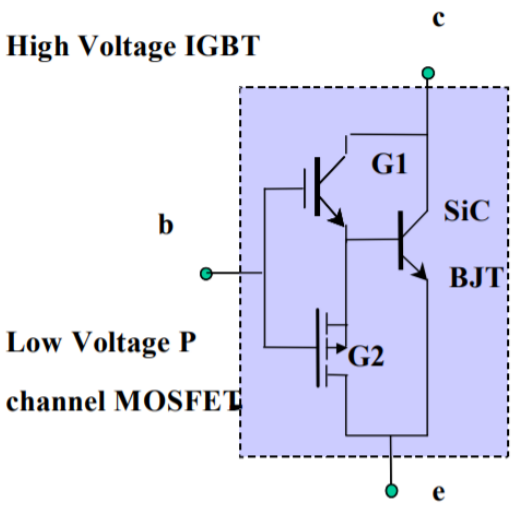


Figure 1-25 Power consumption simulation analysis in the conventional base driver relating to the switching frequency (V_{DD}=10V; C_{pulse}=100nF; R_2=1.5Ω)

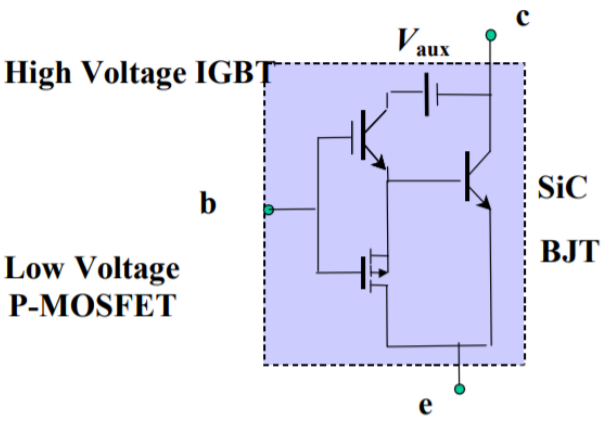
1.7.4 Alternative base drive techniques for SiC BJTs

A method to reduce driver power consumption is a fundamental concern in driver design. This section discusses and reviews several solutions.

IMGT base driver – An IGBT and MOSFET Gated Transistor structure base driver was proposed in [67]. It is based on the same principle as a Darlington configuration which is shown in Figure 1-23. The base current is supplied as part of the collector current of SiC BJT through IGBT (G1) when the logic signal at terminal b is over the threshold voltage turning on G1. The base power loss is only equal to the IGBT drive loss. Moreover, the base current is proportional to the BJT collector current as Darlington's configuration operates. The disadvantages of this base driver are clear: a high voltage IGBT is needed and the voltage drop of the BJT during conduction is high. In order to reduce on-state power loss, an auxiliary voltage (V_{aux}) source was proposed, as shown in Figure 1-26 (b). Compared with the structure in (a), the collector-emitter voltage of the SiC BJT has reduced by V_{aux} when it is conducting. This base driver concept has been verified in a 5kW soft switching SiC BJT inverter [68].



(a) Basic IMGT structure



(b) IMGT with auxiliary power source

Figure 1-26 IMGT base driver structure for SiC BJT [67]

Discretized proportional base driver – This type of drive was proposed in [69, 70]. In this topology, different parallel resistors are located within the driver in order to adjust and control the amplitude of the DC current, as shown in Figure 1-27. Resistors R1 to RN are used to set up DC base current during the conduction interval. Switches (SW1-SWN) are connected in series with each resistor to open or close a current path to the base terminal. The excessive base current can be avoided by using discrete base current levels. However, the resistor network and their gate drivers occupy a large board area and the additional gate drivers for switches (from SW1 to SWN) also increase the board complexity and power losses. With this option, only a few discrete DC base currents can be selected which is limited by the number of the resistors and, when the collector current reaches the device's maximum rated value, all of the resistors need to be connected in the circuit to provide a large DC base current. Under such conditions, its power consumption is the same as a conventional driver. Further improvement for this structure in order to switch the SiC BJT faster, would be a dynamic power stage with a RC current path to generate current peaks during the transient process. This base driver was verified in a DCDC converter applied in an ideal electrical vehicle in [69] with a steady state base driver loss reduction of 60% compared to a signal level driver.

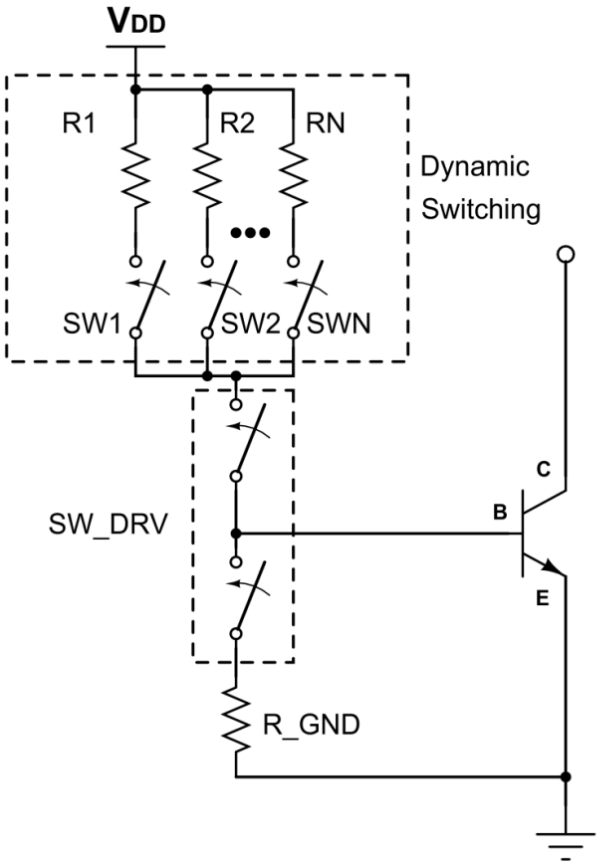


Figure 1-27 Discretized proportional base driver (adapted from [69])

Current source base driver – A current source base driver integrating an air-core inductor was introduced in [71] as shown in Figure 1-28. Prior to the turn-on stage of the BJT, switches SW2 and SW3 are turned on to charge an inductor (L) to an intended current peak from t1 to t2, as shown in Figure 1-29. When the desired current peak is achieved in the inductor, SW2 will turn off to divert this large current to the base terminal from t2 to t3, forcing a rapid turn-on process. From t3 to t4, the energy in L is completely transferred to the base and then only DC base current is provided by V_{DD}, set by R1 and R2 as shown in Figure 1-28 after t4. Since the negative voltage source ($-V_{DD}$) is used; the negative current peak is generated at t5 for a fast turn off.

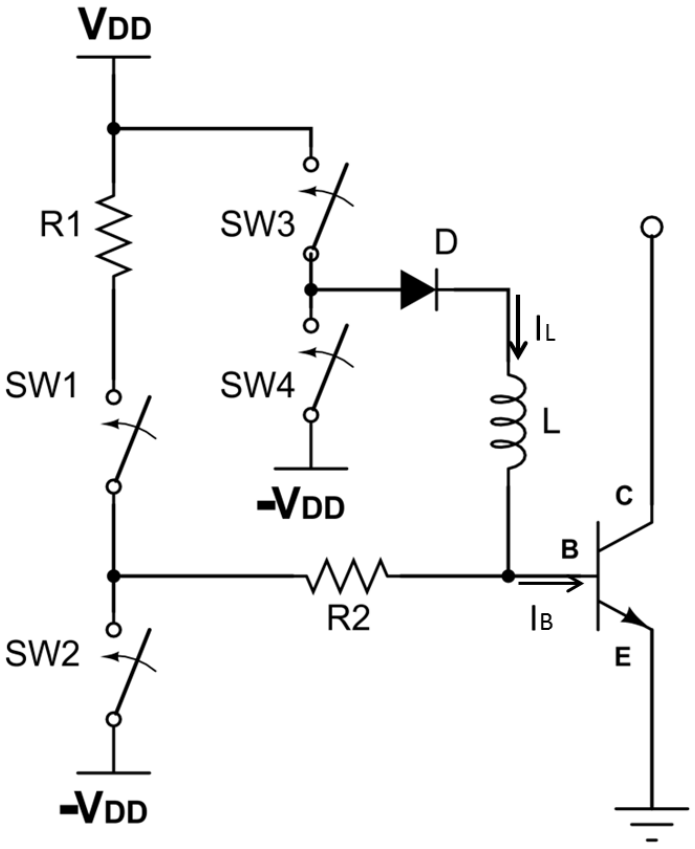


Figure 1-28 Current source base driver (adapted from [71])

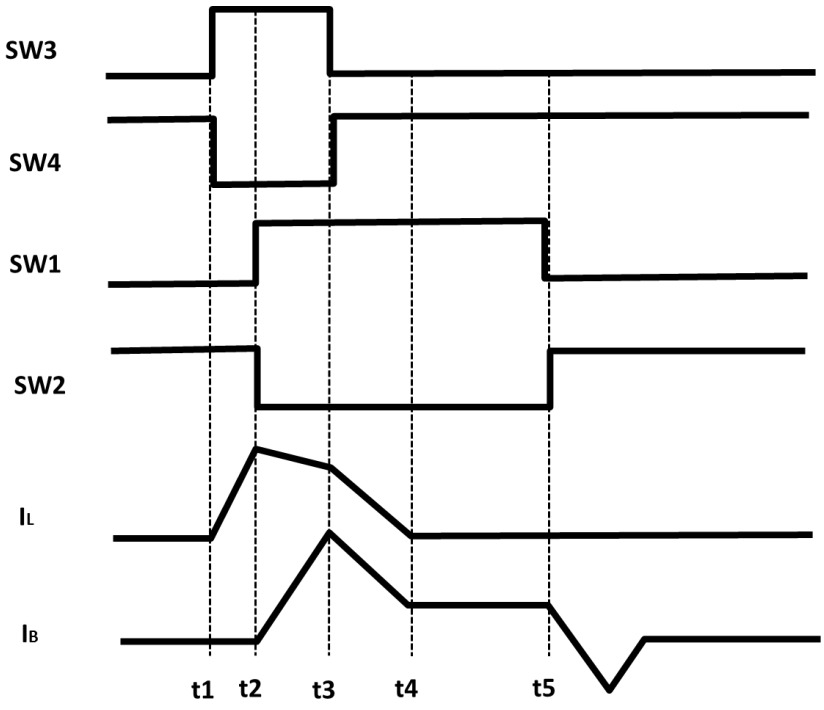


Figure 1-29 Operation principle

Compared with the conventional base driver, the RC current branch is replaced by an inductor (L) and diode (D) to generate a current peak. This inductor can be seen as an energy buffer to limit the circuit ringing induced by the parasitic inductance. Moreover, the current suppled from this inductor can be kept constant even if the base voltage fluctuates because of fast transients. So a low power supply (V_{DD}) (5V referred in [71]) can be used on board, reducing the resistor power losses on R1, which is the main advantage of the design. No energy regeneration for the inductor is required and the regeneration could make the design very complex [72]. But for the turn-off process, a negative voltage needs to be used to speed up the transient to reduce the switching losses, which inevitably increases the amount of electrical components and board size.

Dual-source supply driver – This new base driver design is based on a dual-source DC power supply configuration, as shown in Figure 1-30 [73]. A low voltage (V_L) supplies a DC base current for the conduction state while high voltage (V_H) for C_{pulse}-R path is used to increase the transient speed by generating high current peaks. A low resistance (R_1) can be chosen to match this low voltage supply (V_L) to supply a desired base current. P_R in Equation 1-21, which dominants the driver power losses, can be significantly reduced with a small R_1. Therefore, the base driver efficiency is improved while the switching losses of SiC BJTs decrease. That has been experimentally verified and applied in a 6kW DC/DC converter [74]. The parallel connection of the SiC BJT was implemented to achieve a high converter efficiency of 98.5%. The base driver unit described takes 10% of the total power losses.

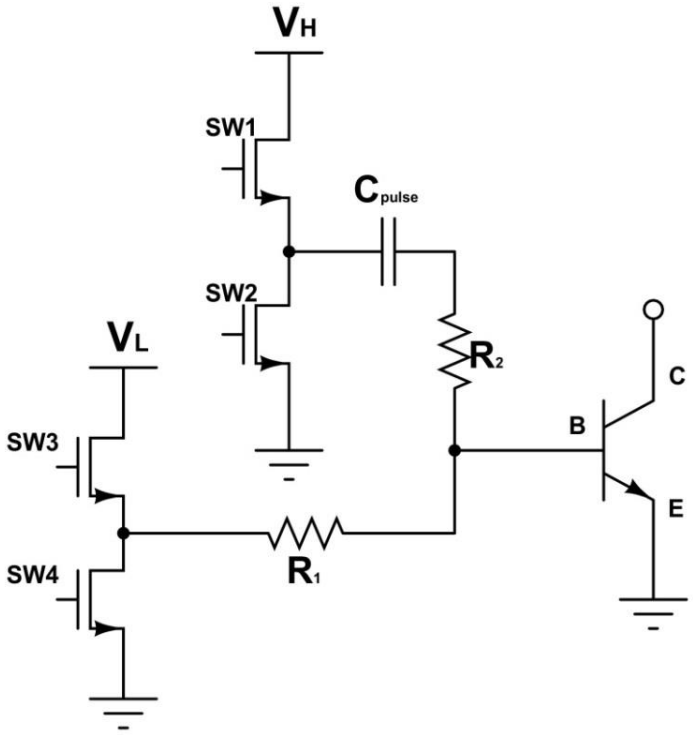


Figure 1-30 Dual-source DC power supply base driver [73]

One disadvantage for this technique is that more components are required compared with the conventional base driver, thus increasing the circuit board area. According to Equation 1-23, with the high voltage (V_H), the capacitor power losses can become dominant under a middle range switching frequencies when DC base current (I_{DC}) is low, as shown in Figure 1-25. Another disadvantage is that the base current in Figure 1-30 is not able to change with the junction temperature or collector current, so the overdriving occurs when the BJT is not operating under full load conditions.

The prototype PCB design and measured base current waveform for this drive are shown in Figure 1-31 and Figure 1-32 respectively. There is only one input voltage level of 15V on the PCB used as the high supply voltage, V_H. A commercial 15V to 5V DC/DC converter from TRACO (Part number: TMA 1505S) as shown in Figure 1-31 provides a low voltage stage, V_L, to the board. Figure 1-32 shows the measurement results of a 330mA base current, I_{DC}, which is used to maintain the conduction of the BJT with 1.5A peak current. Assuming the junction temperature is 150°C with current gain 25 as the worst case, this drive can maintain 5.5A collector current while keeping the on-state losses low. Using a separate high voltage branch offers improvements in switching speed and it does not influence the on-state

performance. Appendix 8-1 and Appendix 8-2 give details of the circuit schematic and PCB layout design of the dual-source DC power supply base driver.

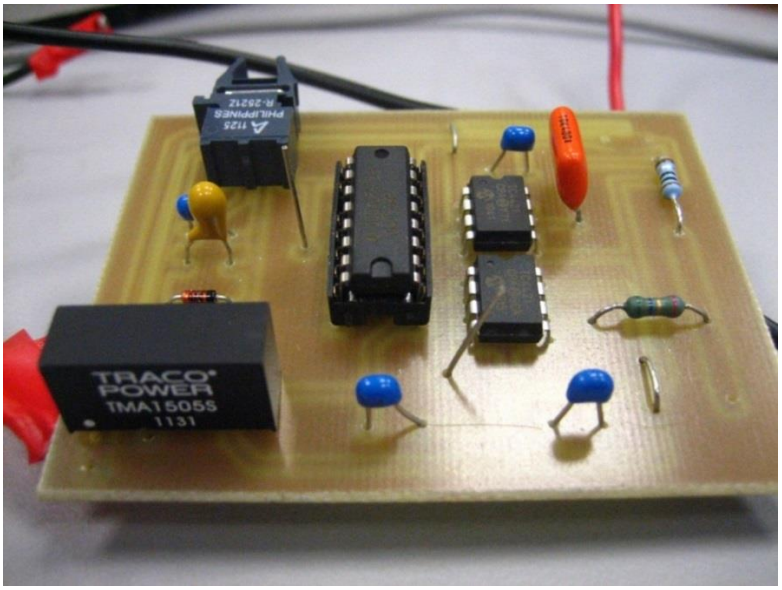


Figure 1-31 PCB fabrication of the dual-source DC power supply base driver

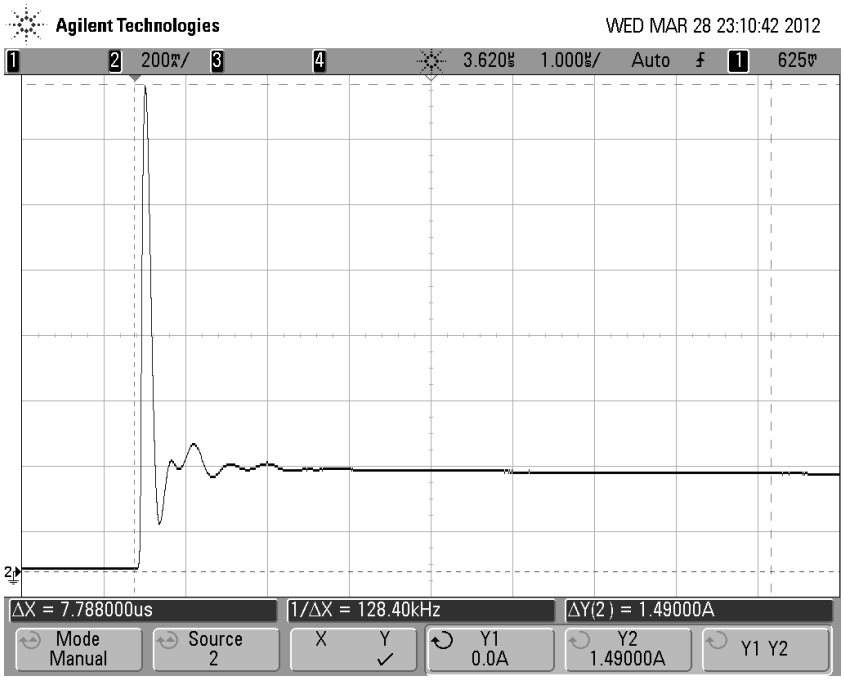


Figure 1-32 Base current measurement from the dual-source DC power supply base driver (200mA/ and 1μs)

Single inductor driver –This optimized base driver configuration has been proposed and applied to a resonant inverter [75], as shown in Figure 1-33. This base drive features a buck DC-DC converter, composed of SW1, SW2 and L. The output current of this converter is fed to the BJT as a base current. The duty cycle of switches SW1 and SW2 is controlled to supply a required DC base current according to the load condition. The inductor (L) is used to store the current by charging and discharging during the BJT on-state. Due to the absence of the discrete resistor, the driver losses are significantly reduced compared with other driver structures. The winding resistive loss needs to be taken into account when the DC base current is very high. The driver can provide the adjustable currents to the base which avoids the overdriving problem. Since this design lacks the dynamic stage for fast switching, the transient power losses inevitably increase. A resonant inverter is a suitable application for the driver, considering a zero-voltage switching (ZVS) which originally possesses a very low turn-off power loss. The experimental results show the fact that the converter with SiC BJT has achieved the highest efficiency driving by the proposed base driver, comparing with a Si IGBT converter. However, for the hard switching or high frequency applications, little advantages are seen in terms of base drive power loss.

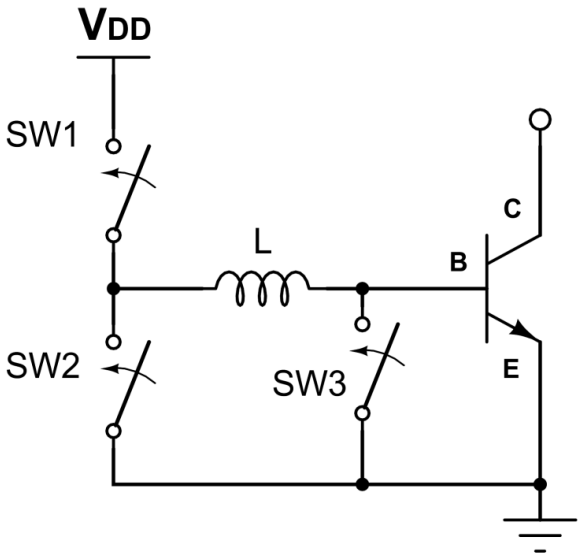


Figure 1-33 Proposed base driver design for the resonant inverter (adapted from [75])

Proportional base driver – A current transformer is used to provide a proportional base current in order to maintain the on-state of SiC BJTs in this design, as illustrated in Figure 1-34. The collector current is coupled directly to the base through diode (D1) and the secondary winding of the transformer does not have any resistors in its path in order to minimize the base driver power losses [76]. When SW1 is turned on at t1, Figure 1-35, a positive peak current is generated due to the low RC impedance. After a short delay, the collector current I_C begins to rise at t2 causing positive voltage across the winding P1. I_{D1} starts to flow due to the positive P2 winding voltage. From t3 to t4, collector current increases slowly so that I_{D1} drops to a low level, dependent on the winding number ratio between the primary and secondary. When SW2 is turned on at t4, the BJT starts to turn off. The current gain decreases when the collector current is low, so a minimum current needs to be fed into the base from R_1 under light load conditions in order to keep the BJT conducting. The primary winding brings the extra inductance into the power line which will degrade the switching speed, enhance the ringing effect and stress on the device. Transformer overheating is another issue if the drive current is high. In [77], the author has applied this proportional base driver in a 2.52kW buck converter, which has achieved efficiency of 99.3%. The base driver loss only occupies 2% of the total losses.

Two other structures in [78] and [79] implement a proportional base current without this transformer. Instead, the collector current or collector-emitter voltage is measured and used as a control factor to adjust the base current. The disadvantages of these drives are the requirements of high bandwidth current transducer, complex sensing and control circuit. In addition to the re-design of the base driver circuits reviewed above, it has been proposed to use on-step commutation algorism for the inverter control [80]. This eliminates the dead-time effect and reduces the turn-on time of each BJT switch in one cycle. Unnecessary conduction time of the BJT is minimized and the driver losses reduce accordingly.

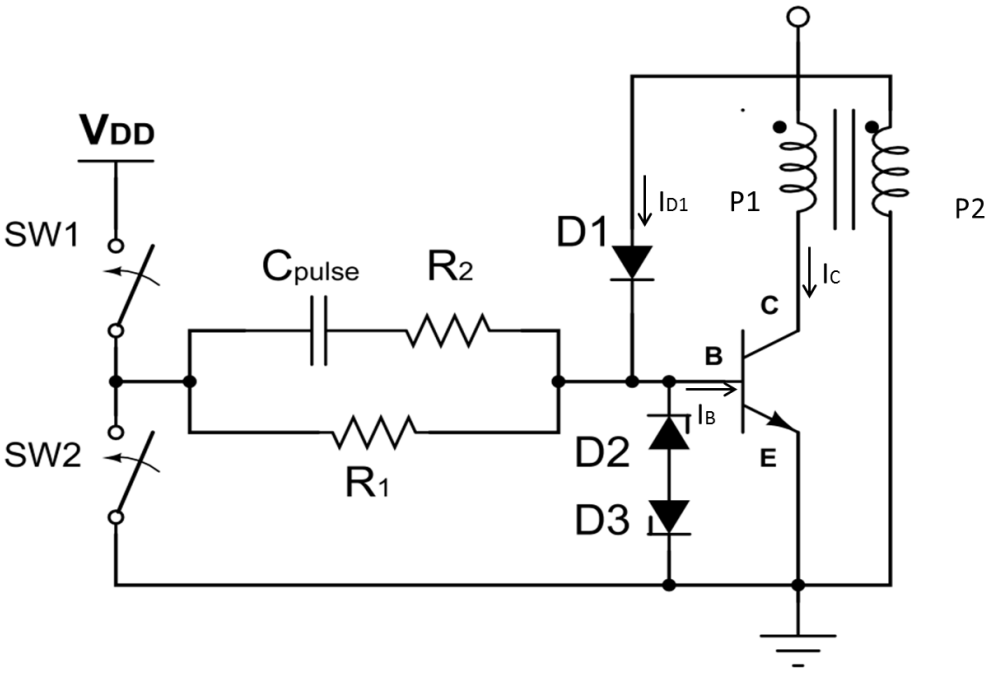


Figure 1-34 Proportional base driver (adapted from [76])

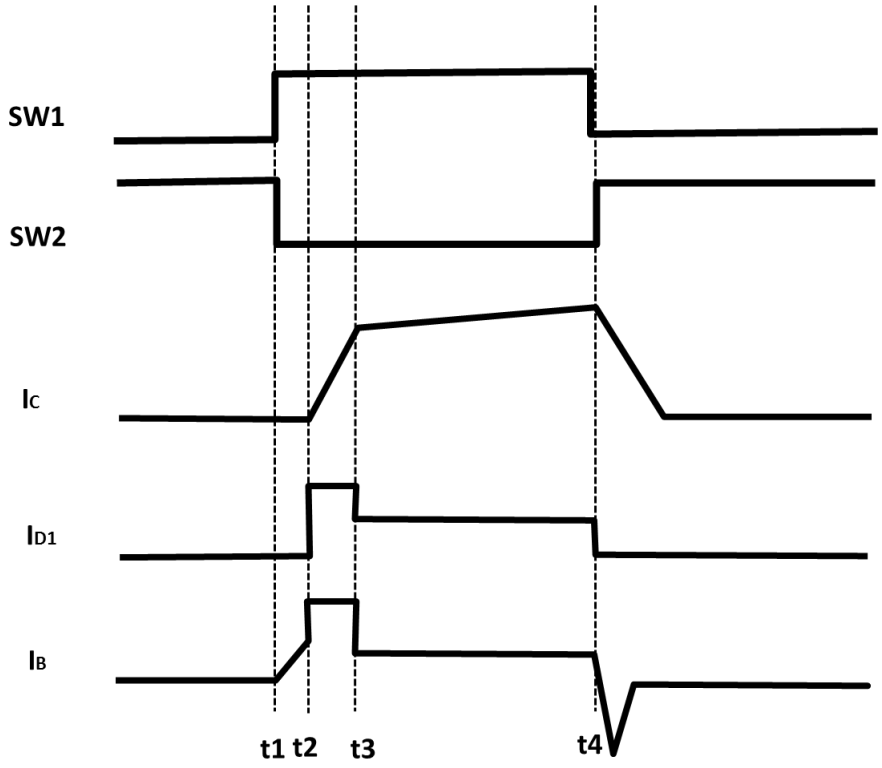


Figure 1-35 Time scheme of the proportional base driver

1.8 Conclusions

Various power devices have been introduced in this chapter with their structures and operation principles. Driver technologies are applied on the different devices based on the requirements for tuning on and off. The superior performance of SiC BJTs, due to the wide band gap material properties and n-p-n robust device structure, has been described in Chapter 1. Compared with the voltage-driven power devices, the high power losses of the base driver is one of the weaknesses of SiC BJTs. Several novel drive designs targeting to improve the efficiency and reduce switching losses are reviewed.

The SiC BJT can operate at a high junction temperature. Chapter 2 explores switching performances at high junction temperatures for SiC BJTs with comparisons to Si IGBT. The self-heating methodology is adapted to achieve high junction temperature in the experiment. The experimental results indicate that SiC BJTs are suitable to high temperature applications.

As shown in Figure 1-25, the power losses of the pulse capacitor (C_{pulse}) at high switching frequencies dominates when the DC base current is low. The energy in the capacitor can be recovered instead of draining all the charges to the ground. This idea is firstly used in the base drive design for SiC BJT in Chapter 3 for high frequency applications. The boost converter using the SiC BJT driven by the proposed circuit is prototyped and discussed in Chapter 3.

For low frequency applications, an active base driver design is firstly proposed in Chapter 4. The design is able to change the base current's amplitude and, thus, reduce the driver loss. A separate current path is included to enable fast switching. A comparison between the conventional driver and the active base driver is presented and discussed. The proposed base driver is verified in an integrated converter.

Chapter 5 proposed an integrated converter design including the theoretical analysis and hardware prototype. SiC BJT is used as a power switch in the converter, which is driven by the active base driver unit.

Finally, Chapter 6 comes to the conclusion of the thesis and possible future work based on the current research.

The drive designs and implementations considered in Chapter 2-5 are all original and first proposed by the author.

2 Comparison of Switching Characteristics between SiC BJTs and Si IGBTs at High Junction Temperatures

2.1 Introduction

Semiconductor device power losses manifest itself as heat generation which needs to be removed from the device packaging to maintain the junction temperature below their maximum operating conditions. Therefore a cooling system is required to dissipate heat away from the device packaging and into the ambient. As the size of the cooling system is proportional to the dissipated energy, a device with high junction temperature capability will effectively reduce the size and complexity of the cooling system. SiC can withstand higher maximum junction temperatures and has a low intrinsic carrier concentration at high temperature, which reduces the leakage current when the devices are operating in their off state [81].

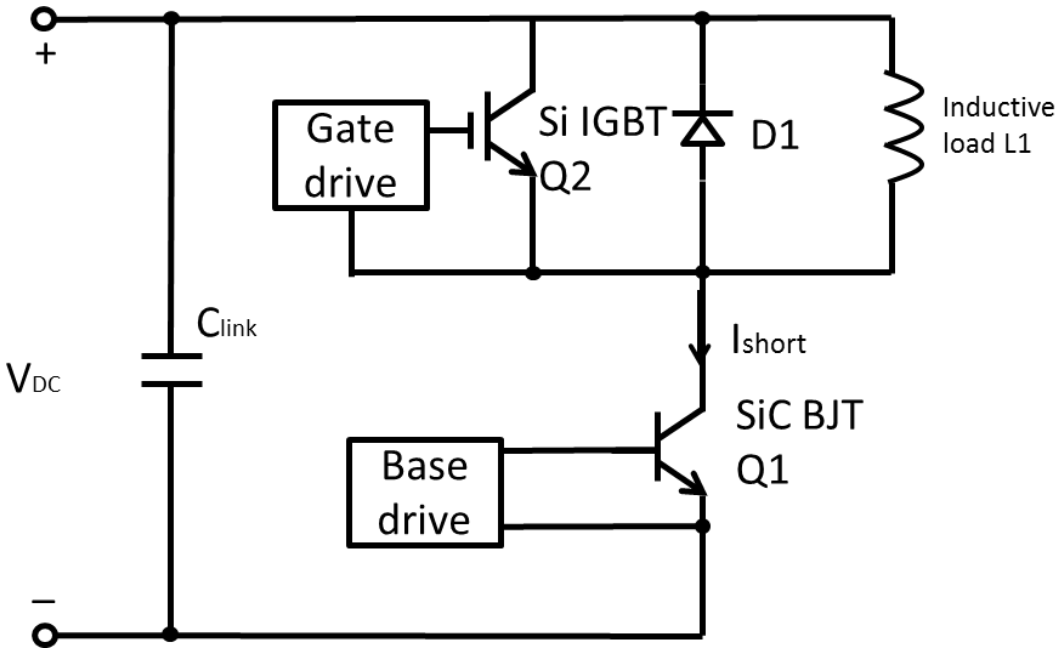
One of the main advantages of silicon carbide is the increased maximum operational temperature, due to its wide bandgap, compared to silicon, and the resultant low intrinsic carrier concentration. MOSFET, JFET and BJT, are commercially available in SiC, each of these has its own limitations with respect to operational temperature. For an example, the maximum operational temperature of the power MOSFET structure have been shown to be limited at 200ºC due to the reliability of oxide-related issues [35]. However, the leakage current is almost negligible at high junction temperature for SiC MOSFET [82]. SiC JFET devices are generically normally on, however normally off structure are available on the market. Even though cascading the structure with a low voltage MOSFET can re-configure the device to become normally off, the additional MOSFET increases the on-state resistance and maximum operational temperature is limited by the silicon component [83]. Due to its inherently normally off behaviour and the absence of gate oxides, the bipolar junction transistor structure overcomes these limitations of MOSFETs and JFET structures. Therefore, the structure is more suitable for high temperature operation, compared to alternative SiC technology.

2.2 Self-heating methodology for double pulse inductive switching

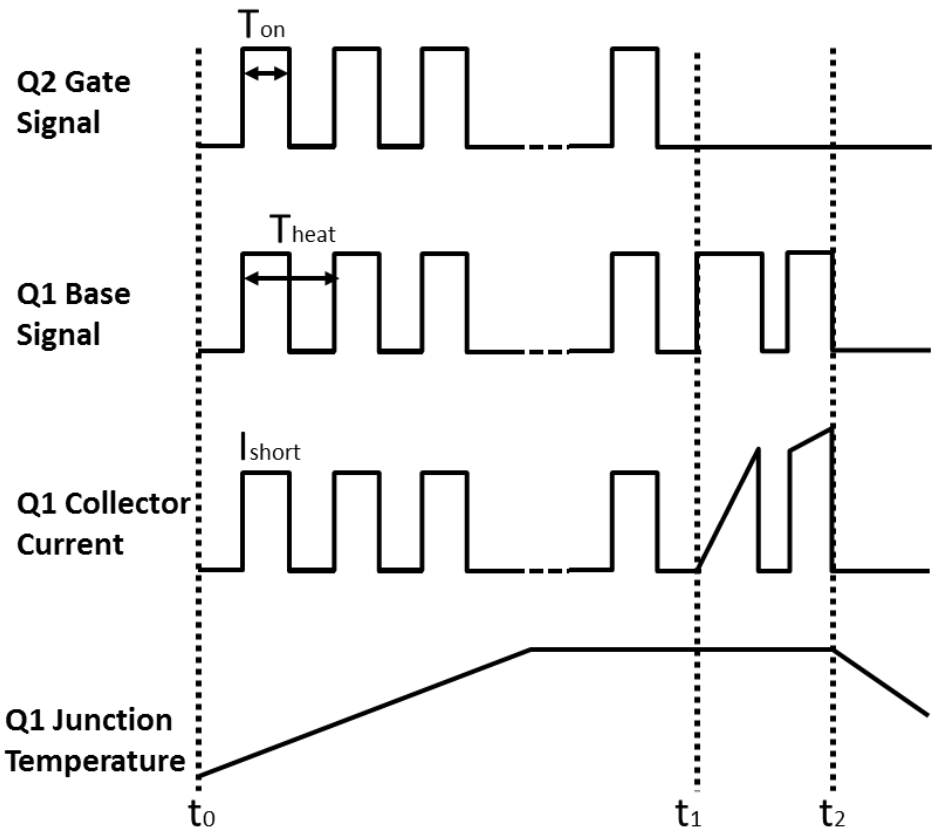
In order to evaluate the SiC BJT switching performance under high junction temperatures, the device is self-heated above the test temperature where the circuit is re-configured to measure

inductive switching losses. This methodology requires no hot plate to heat the device externally and therefore reducing stray inductance from routing electrical connections.

Figure 2-1 shows the test circuit and time scheme of critical signals. By turning on Q2 and Q1 at the same time forces the devices into a short circuit conditions as shown in Figure 2-1b. As the saturation characteristic of the silicon IGBT is chosen to have significantly higher current saturation, current is limited by the BJT operating in the active mode. Due to the presence of both high current and voltage, Q1 is heated up by controlling the applied short current (I_{short}), short circuit time (T_{on}) and time period t_0-t_1. To increase the thermal capacity of the device Q1 a copper block is attached to the backside which has an embedded thermocouple. Therefore after a temperature above the test temperature is achieved, the thermal time constant (temperature dropped 1% after 1s) of Q1 is slower than that of the double pulsed switching transient, therefore the junction temperature would be close to the case temperature, due to the significantly higher thermal time constant compared to the semiconductor die. As the device is in a cooling cycle, the circuit is re-configured so that the IGBT gate is de-activated and switching times of Q1 is adjusted to achieve the test condition. When the test temperature is reached and becomes stable at t_1, the device is activated into a double pulse test and the turn on/off energy losses are recorded during time period t_1-t_2.



(a) Circuit schematic



(b) Time scheme

Figure 2-1 Self-heating circuit diagram for SiC BJT

The gate drive of Q2 is powered by a ±15V source, whose zero potential is referenced to the BJT's collector. The schematic and PCB layout designs for this high side IGBT Q2 gate driver are shown in Appendix 8-11 and Appendix 8-12. The power loss of Q1 is given by:

$$P_{Q1} = \frac{I_{short} \cdot V_{CE,Q1} \cdot T_{on}}{T_{heat}} \quad \textbf{2-1}$$

Where I_{short} is the short circuit current when Q1 and Q2 are both turned on for a period T_{on} in one heating cycle T_{heat}.

2.3 Operation and experimental set up

In the test rig, the copper bus bars are shown in Figure 2-2 are used to replace cables to connect the electrical components. DC de-coupling capacitors are added to the test circuit to ensure the fast turn on/off current edges are sourced locally, thus reducing parasitic inductance and bypassing AC noise. A small length of wire is attached to the emitter terminal of the BJT for positioning the current transducer. The base drive circuit is a conventional drive with a speed up capacitor, as discussed in section 1.7.3.

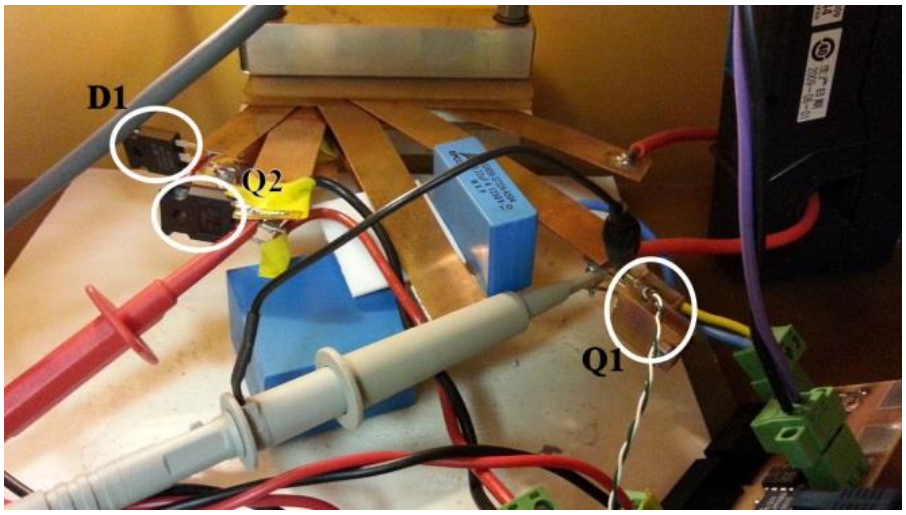


Figure 2-2 Self-heating and switching test set up

V_{DC} in the experiment was set to 600V, a typical test and operating condition for the 1200V breakdown voltage device, which is Q1(SiC BJT) [17], whereas the continuous collector current is ramped up to 20A. The IGBT used in [84] had the same breakdown voltage but a continuous collector current of 90A. When Q2 is turned on as a short across the load, the short current amplitude is limited by Q1 and therefore Q1 undergoes significant self-heating. D1 is a 1200V/100A SiC Schottky diode made by GeneSiC due to its low reverse current which is 25μA at 1200V/25°C. The continuous DC current is 100A for this diode. The maximum junction temperature can be 175°C. DC power supply and L1 is embedded in a switching test rig, as shown in Figure 2-3. The load inductor is constructed using an air core with a single layer of winding to minimise parasitic capacitance across the windings. The DC-link voltage is supplied from a rectified output from a transformer with multiple output taps fed from a variac at the primary winding. The rig provides three connections; across the load inductance for connection of Q1 and free wheel diode and at a ground plane where the current sensor is positioned. The power connection is in a bus-bar layout to minimise stray inductance between the DC-link capacitance and Q1. Control logic signals are generated from a FPGA, located outside of the test rig. Galvanic isolation between the low voltage and high voltage sides of the test rig is facilitated by an optical emitter and receiver.

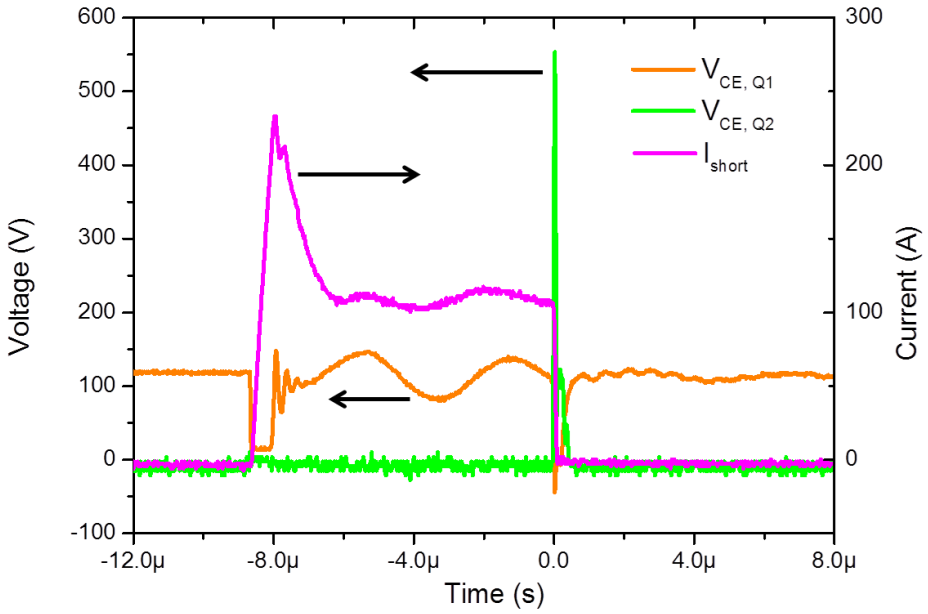
Figure 2-3 Experiment set up using a switching test rig

2.3.1 Short circuit test for SiC BJT

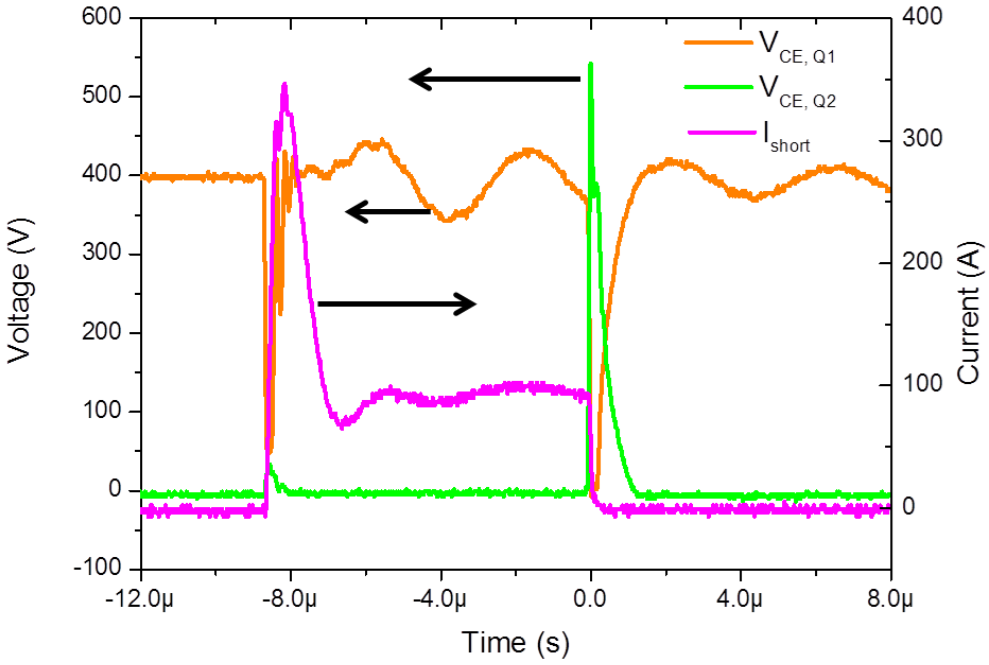
In the absence of a short circuit provided by the device manufacturer, single pulse short circuit testing was performed on Q1. The same test circuit was used to establish the short circuit performance of the device, both Q1 and Q2 were controlled together so that Q1 would enter into a short circuit mode whereas Q1 would control fault current and act as a current limiter. Short circuit testing was performed with a single short pule of 9μs at a very low frequency to reduce the effects of accumulative power heating.

Figure 2-4 shows typical short circuit behaviour of Q1 under various DC-link voltages. A low impedance path provides a base current spike during BJT's turn-on process as specified in last chapter. This large current forces the BJT working in the saturation region with low resistance, which results in a current spike through Q1 and Q2 at the beginning as shown in the figure. As time increases the device enters the active mode of operation and short-through current reduces to a stable state. During this time, there is a slight oscillation of $V_{CE,Q1}$ due to

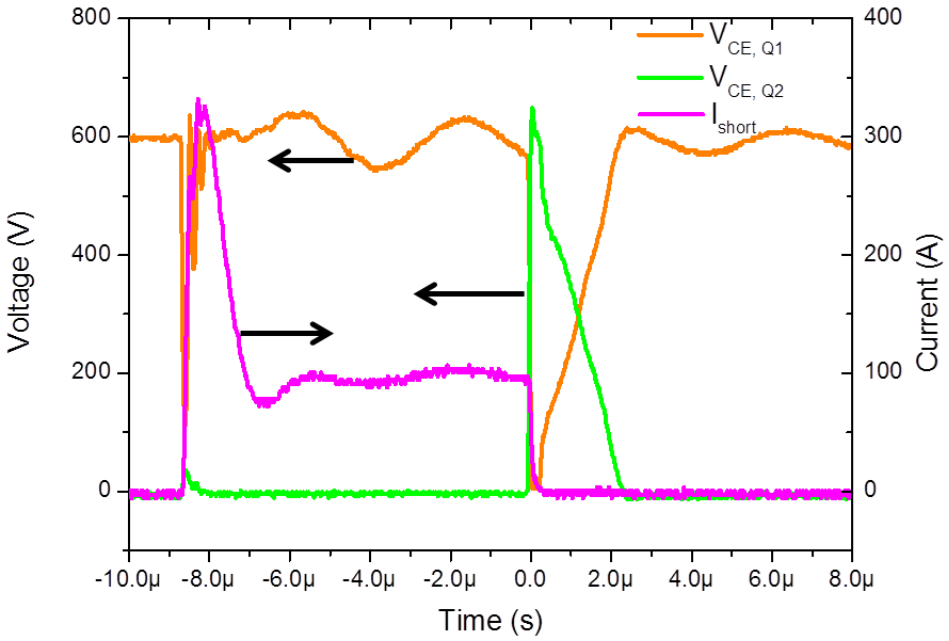
the resonance between the DC-link capacitance and parasitic inductance induced by the wire connecting Q1 and Q2. The wire is required to enable the current transducer to measure the short current.



(a) $V_{CE,Q1}$ = 120V, I_{short} = 100A and T_{on} = 9µs



(b) $V_{CE,Q1}$ = 400V, I_{short} = 100A and T_{on} = 9µs

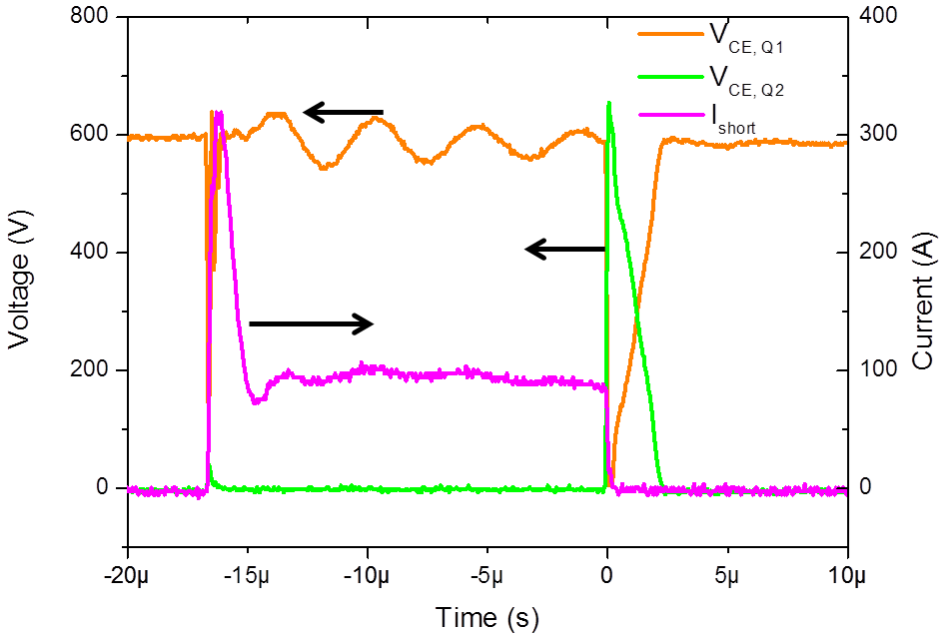


(c) $V_{CE,Q1}$ = 600V, I_{short} = 100A and T_{on} = 9µs

Figure 2-4 SiC BJT short circuit performance

Under these tests, the SiC BJT can survive a 9µs short circuit period up to 100A at 600V when driven by a 1.6A base current. Due to the constant base current, the short current does not change, although the voltage is increasing from 120V to 600V. At 100A collector current, $V_{CE,Q2}$ is only few volts due to the large current capability of the selected IGBT. As shown, under these conditions the Early Effect is insignificant for the SiC BJT.

If the short circuit time is increased from 9µs to 17µs, as shown in Figure 2-5, the device fails after several test cycles. The failed device demonstrates an open circuit characteristic implying a failure of the wire bonds of the device. This provides a maximum limit for the self-heating approach prior to the inductive load double pulse test.



$V_{CE,Q1}$ = 600V, I_{short} = 100A and T_{on} = 17µs

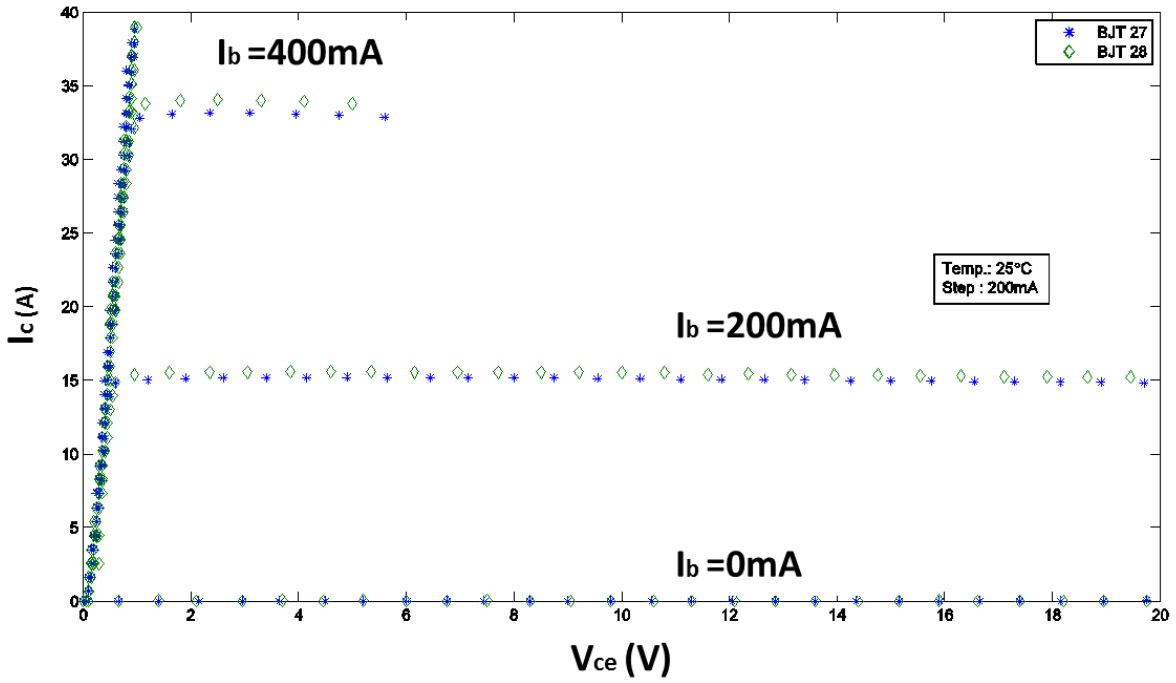
Figure 2-5 SiC BJT short circuit performance with longer time period

2.3.2 I-V characteristics and tolerance of two SiC BJT samples

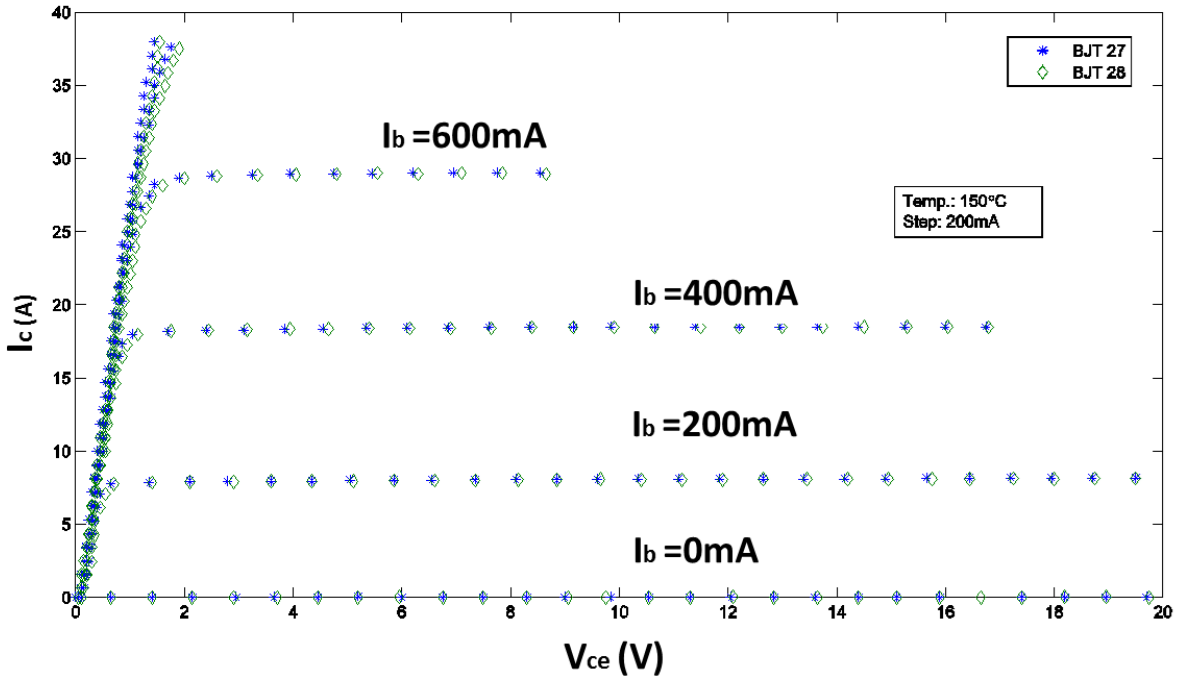
A number of pre-production 1200V/20A SiC BJT samples were supplied from Transic/Fairchild. Due to the device infancy, only a primary datasheet is provided by the manufacturer, therefore to establish the electrical characteristics of the devices, DC characterisation was performed using a Tecktronix 371A interfaced with a Thermo-stream. Three terminals of the BJT are directly connecting to the ports of Tecktronix, which will supply a stepped base current (I_b) from 0mA to 800mA and increase the collector-emitter voltage (V_{ce}) gradually for each step of base currents. During this process, the collector current (I_c) is measured to plot the I-V characteristic of the BJT as shown Figure 2-6. The SiC BJT samples were placed into a temperature controlled chamber where the temperature was adjustable. The internal temperature of the chamber was maintained at the set-point for ten minutes by the thermos-stream unit to ensure the junction temperature be the same as the chamber temperature. Figure 2-6 shows the I-V characteristics of the BJTs at 23°C, 150°C and 193°C for base currents ranging from 0mA to 800mA in steps of 200mA.

The curves of two samples, named BJT 27 and BJT 28, are almost overlap at collector current levels of 20A for a temperature range of 25°C to 193°C. The collector-emitter saturation voltage is measured at 0.5V, 0.8V and 1V for a collector current 20A and temperature of

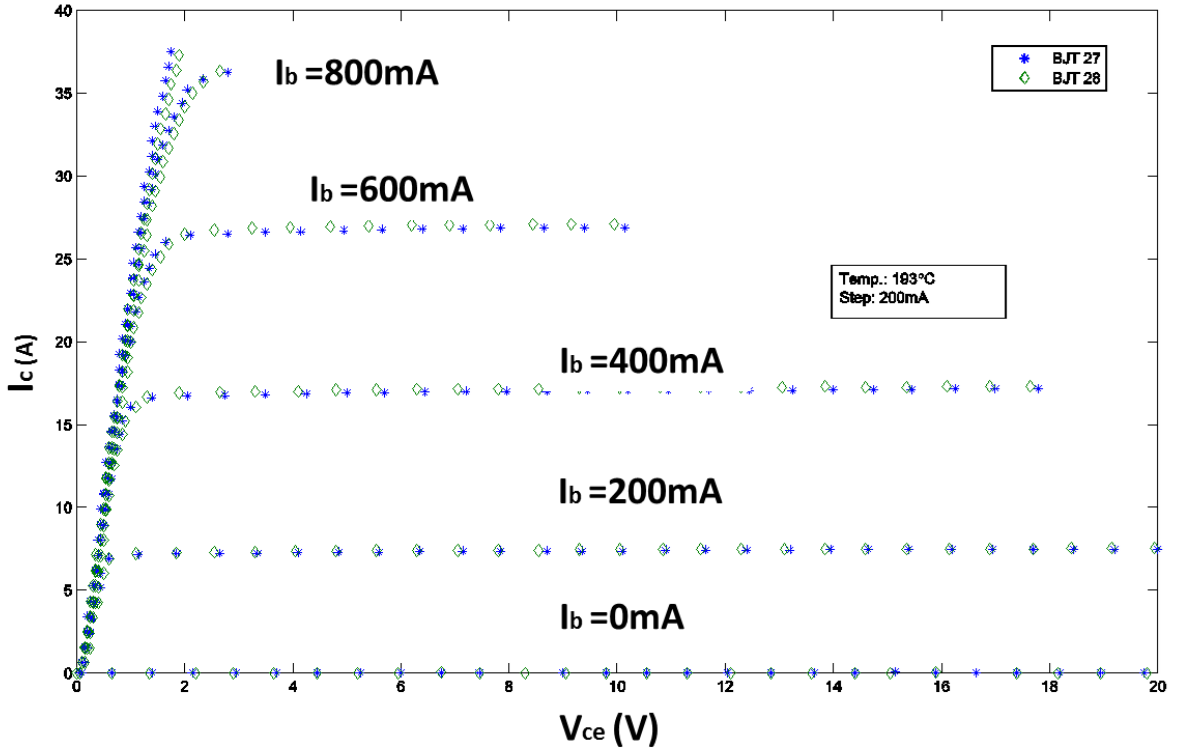
25°C, 150°C and 193°C. This would result in an increasing on-state power loss at high temperature. For the same base current, due to the reduction of current gain, the collector current in the active region reduces with the junction temperature. Therefore, the device requires an over current rating of the base drive so that the device does not enter the active mode during high temperature operation. Comparing the measured I-V characteristics with the one given in the datasheet, the samples used in the experiment are representative of devices at the minimum end of the device tolerance.



(a) 25°C junction temperature



(b) 150°C junction temperature



(c) 193°C junction temperature

Figure 2-6 I-V characteristics comparison of two SiC BJT samples

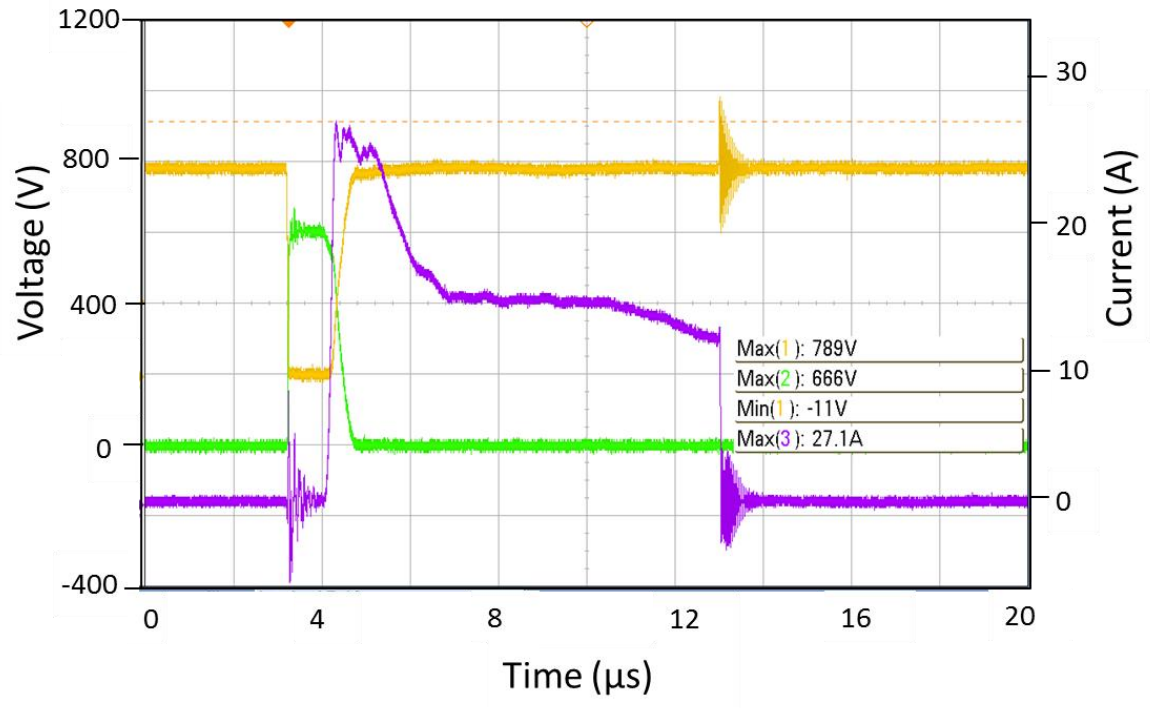
2.4 Switching performance of the SiC BJT at high junction temperatures

In order to reduce the power loss in Q2, as shown in Figure 2-1, the DC-link voltage (V_{DC}) should be predominantly supported across Q1 when both device (Q1 and Q2) are turned on. The power loss P_{Q1} of the BJT, Equation 2-1, is dependent on heating period (T_{heat}) and short circuit current level (I_{short}). Q1 collector current (I_{short}) is controlled by the base current. Due to the short circuit safe operating area limits, I_{short} should be set below 20A which is the rated value in the datasheet. The base current was therefore reduced from 1.6A to 0.15A and 0.29A by increasing the base driver resistor R_1 in Figure 1-24. Even though the base current is the same (0.15A), the case temperature can be changed by varying heat period (T_{heat}) as shown in Table 2-1. The test can be repeated once the device temperature dropped to the ambient temperature as the short current during the experiment is not over 20A and the maximum case temperature is lower than 250°C. The SiC BJT under test is still functional. In terms of the gate and base signal sequence, Q1 is turned on earlier than Q2 to avoid large turn-on surge current, which could over stress Q1. For all tests a constant collector voltage of 600V was used with a fixed on pulse of 10μs, as shown in Table 2-1. To self-heat the device, the period of this pulse was varied until the back-plate temperature was above the test temperature. Due to the large thermal time constant of the copper header attached to the device, the junction temperature is at a quasi-steady state during the duration of the double switched test to establish turn on and off losses. For the 240ºC case temperature, the base current was increased to 0.29A in order to pass 18A through the BJT, close to its rated current. Most of the applications are designed to operate the device at equal to or smaller than their rating current to ensure the performance and device lifetime. The program for the FPGA to generate control signals is listed in Appendix 8-13.

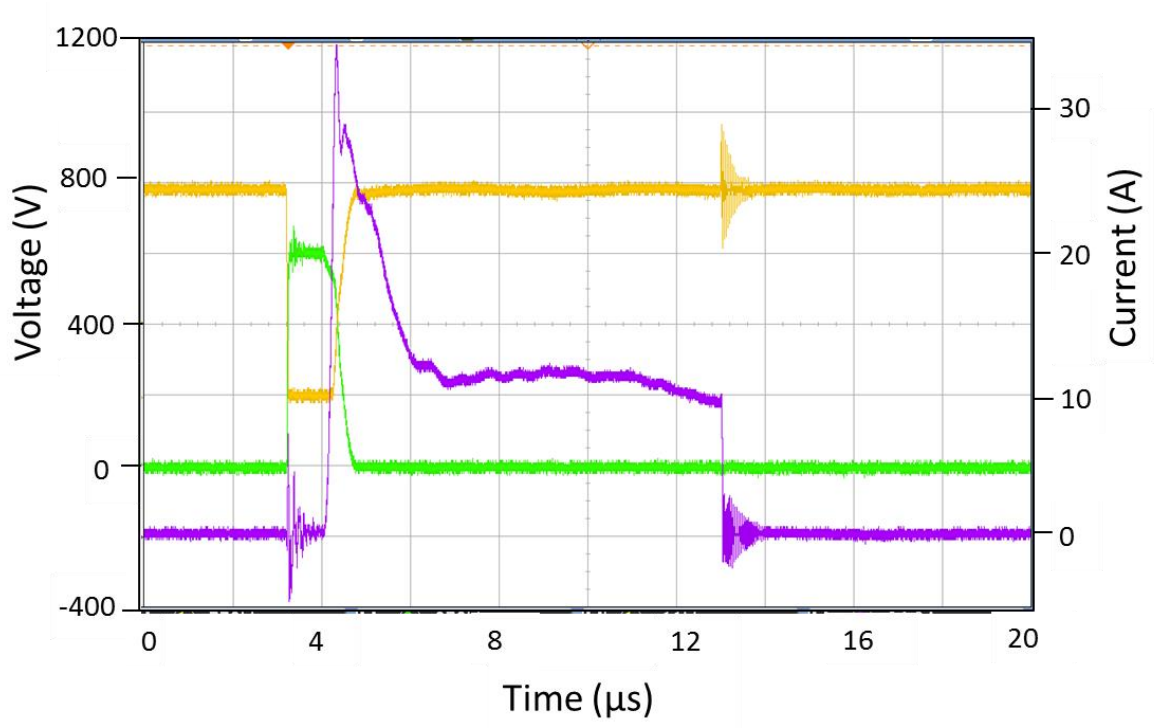
Table 2-1 Heating devices with various T_{heat} for SiC BJT

$V_{CE,Q1}$ (V)	I_{short} (A)	T_{on} (μs)	T_{heat} (ms)	Base current (A)	P_{Q1} (W)	Max. case temperature (ºC)
600	14	10	90	0.15	1.1	45
600	11	10	15.5	0.15	6.6	115
600	18	10	8.99	0.29	14	240

After several thousand heating periods, the case temperature is which is monitored by a thermocouple, remained fixed. Due to the high thermal capacitance of the copper block, the case temperature can be maintained for one second after self-heating ceased. During this period, the switching test is re-configured for the double pulse inductive test. Figure 2-7 shows voltage and current waveforms when Q1 and Q2 are both conducting. The short current (I_{short}) is recorded for all tests. Due to the different junction temperature in (a) and (b), I_{short} is changed although the base current remains the same. At high junction temperature, the resistance of the SiC BJT becomes larger which reduces I_{short} in Figure 2-7(b). Moreover, the current is found to decrease at the end of the waveform (CH3) due to the junction temperature rising with time. According to the different heating times T_{heat} in Table 2-1, the maximum case temperatures increase from 45ºC to 240ºC. The peak collector current is much lower than that in Figure 2-5 due to the modification to the turn-on sequence of Q1 and Q2. Due to the speed up circuit in the base drive, a peak collector current is observed in all tests due to the base current peak for fast turn-on.



(a) 45ºC junction temperature



(b) 115ºC junction temperature

Figure 2-7 Voltage-current waveforms during the heating process for SiC BJT: CH1 (Yellow): $V_{CE,Q1}$, CH2 (Green): $V_{CE,Q2}$, CH3 (Purple): I_{short}

The base current increases to 290mA in order to support a higher short circuit current (I_{short}) of 18A as shown in Figure 2-8. In the following tests, the device was switched at this current level for the transient loss measurement.

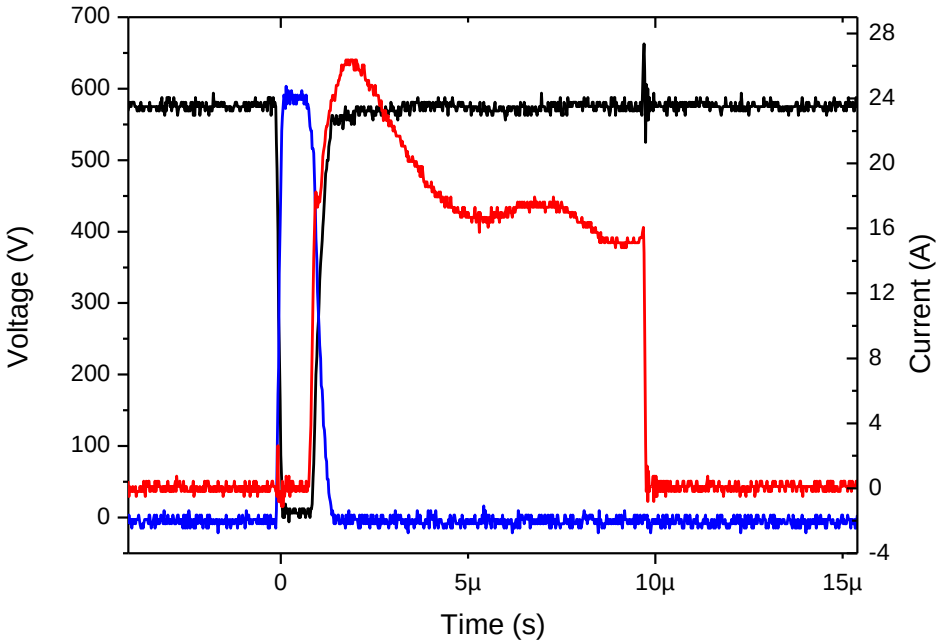


Figure 2-8 Voltage-current waveforms during the heating process for 240°C junction temperature: Black line: $V_{CE,Q1}$, Blue line: $V_{CE,Q2}$, Red line: I_{short}

When the copper block is above the set-point, Q2 and Q1 are turned off to prepare for the double pulse test. During the double pulse switching test, Q2 is held off and Q1 is turned on until the current of the load inductor (L1) is 18A, as shown in Figure 2-9. The Q1 collector current termed ($I_{C,Q1}$) is shown on channel 3 (CH3) in the figure. Then Q1 is turned off and L1 current freewheels through D1. After 40µs Q1 is turned on again, diverting the free wheel current into Q1 and enabling an inductive turn on measurement, as explained in Chapter 1. After a short period of time (40µs), so that the turn on transient is captured, the device is turned off and the inductive energy is discharged via the free wheel diode prior to the next test.

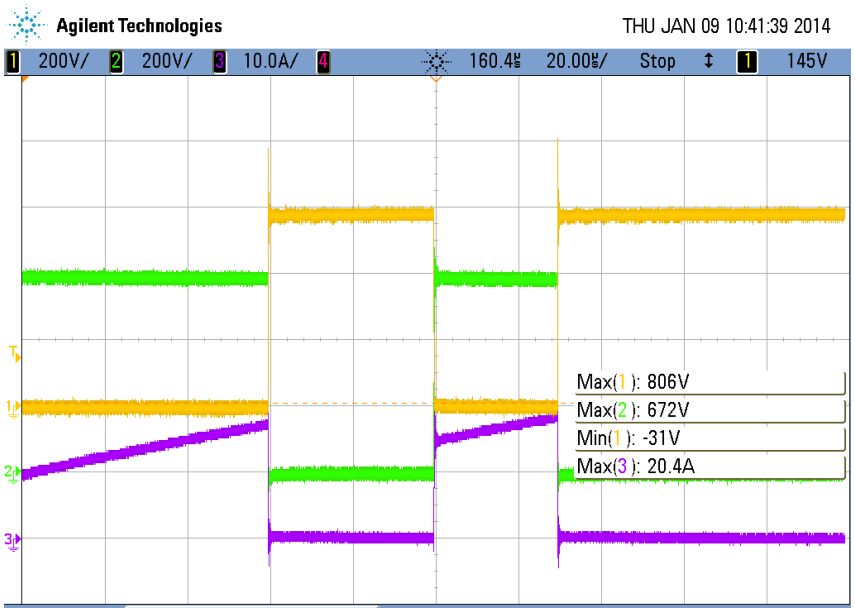
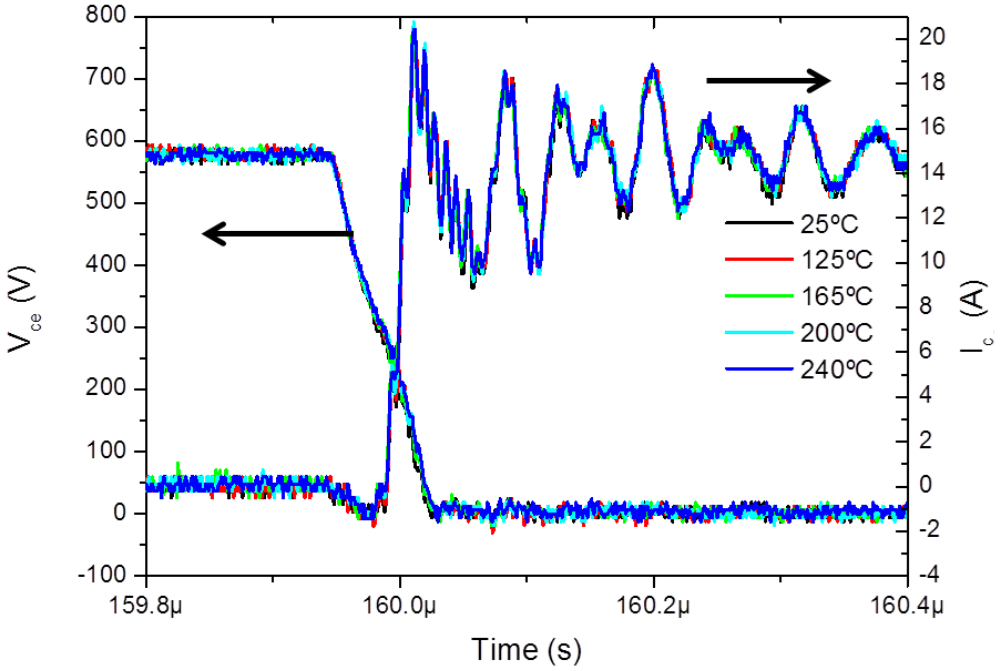


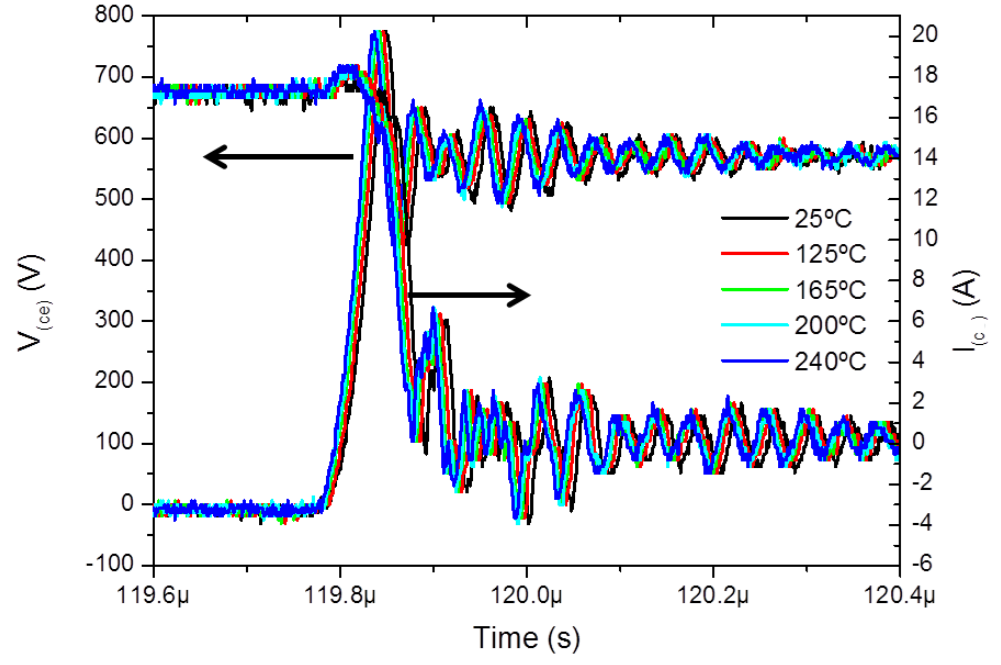
Figure 2-9 Double pulse switching test for SiC BJT at 240ºC: CH1 (Yellow): $V_{CE,Q1}$, CH2 (Green): $V_{CE,Q2}$, CH3 (Purple): $I_{C,Q1}$

Figure 2-10 shows turn on and off characteristics for a 1200V/20A SiC BJT device at a junction temperature of 25ºC-240ºC. As shown, the switching process has a weak dependency upon junction temperature. During the turn on process, Figure 2-10a, collector voltage falls from 600V and collector current increases gradually, even though current gain is reduced and surface recombination is larger at high temperatures. Here the base drive has been design to deliver 1.6A to ensure that the device operates in its saturation mode and turns on quickly.

As shown in Figure 2-10b, the current values drop from 18A and the collector-emitter voltage rises to 600V during the turn-off transient. The turn-off energy losses are reduced at high junction temperatures compared with that at the low temperature, possibly as a results of the improved base ohmic contact resistance [35]. The switching speeds are quantified by the value of di/dt and dv/dt. The deviation between 10% and 90% of the steady value are used as limits for the gradients. The measured di/dt in Figure 2-10a is 2.34×10^3A/µs and the dv/dt in Figure 2-10b is 17.86×10^3V/µs. The resonance in the circuit is noticeable due to the fast switching speed of SiC BJT. Although the experimental set up has already intended to reduce and minimize loop parasitic inductance, high frequency components are still introduced by large dv/dt and di/dt.



(a) Turn-on waveforms



(b) Turn-off waveforms

Figure 2-10 Switching characteristics of SiC BJT at various junction temperatures

2.5 Switching performances comparison between Si IGBT and SiC BJT

In order to compare the switching performances of the SiC BJT and traditional Silicon devices, a Si IGBT rated at 1200V/20A [85] is tested at different junction temperature. The breakdown voltage is 1200V and the continuous collector current is rated at 20A for this IGBT. Identical methodologies and time scheme as used for both devices, a circuit schematic of the test IGBT is shown in Figure 2-11. The schematic and layout design for the low side Si IGBT Q1 gate driver can be found in Appendix 8-14 and Appendix 8-15, respectively.

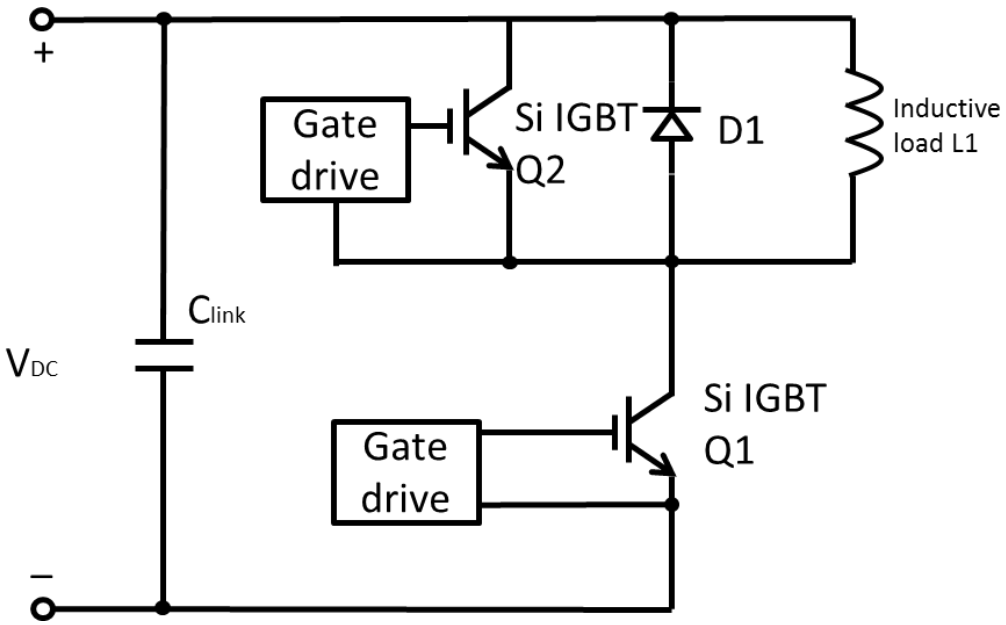


Figure 2-11 Self-heating circuit diagram for Si IGBT

Table 2-2 shows the short circuit parameters for self-heating the IGBT devices from 50°C to 160°C. The collector current (I_{short}) is controlled by the gate voltage of Q1. These conditions were used to increase junction temperature prior to the double pulse testing.

Table 2-2 Heating devices with various T_{heat} for Si IGBT

$V_{CE,Q1}$	I_{short}	T_{on}	T_{heat}	Gate voltage	P_{Q1}	Max. case temperature
(V)	(A)	(µs)	(ms)	(V)	(W)	(ºC)
600	20	10	80	6.9	1.5	50
600	20	10	27	6.77	4.4	100
600	21	10	15.5	6.52	8	160

After self-heating, the circuit is re-configured to perform a double pulse switching test. Figure 2-12 shows a typical switching waveform of an IGBT post self-heating whereas Figure 2-13 shows the turn on/off transients with respect to the temperature.

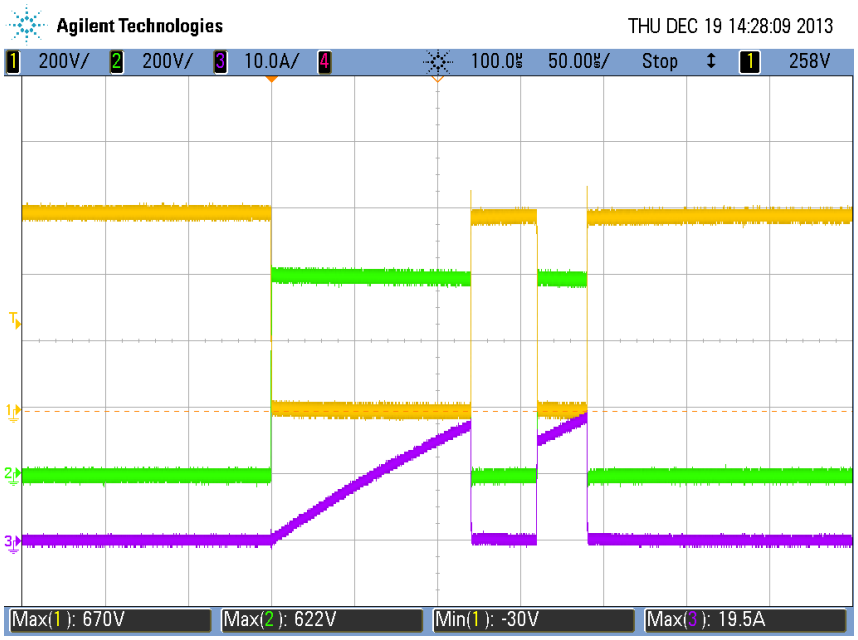
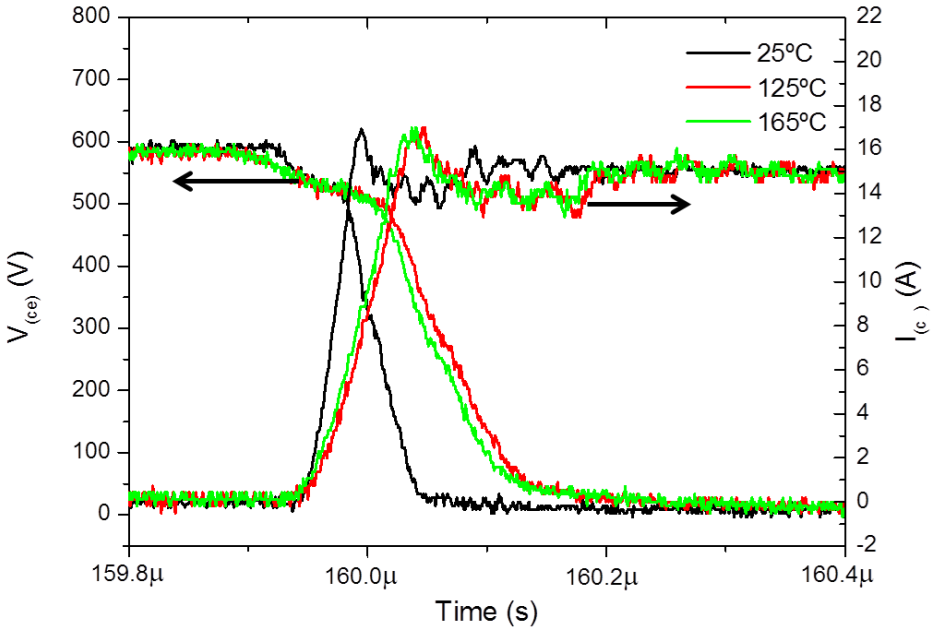
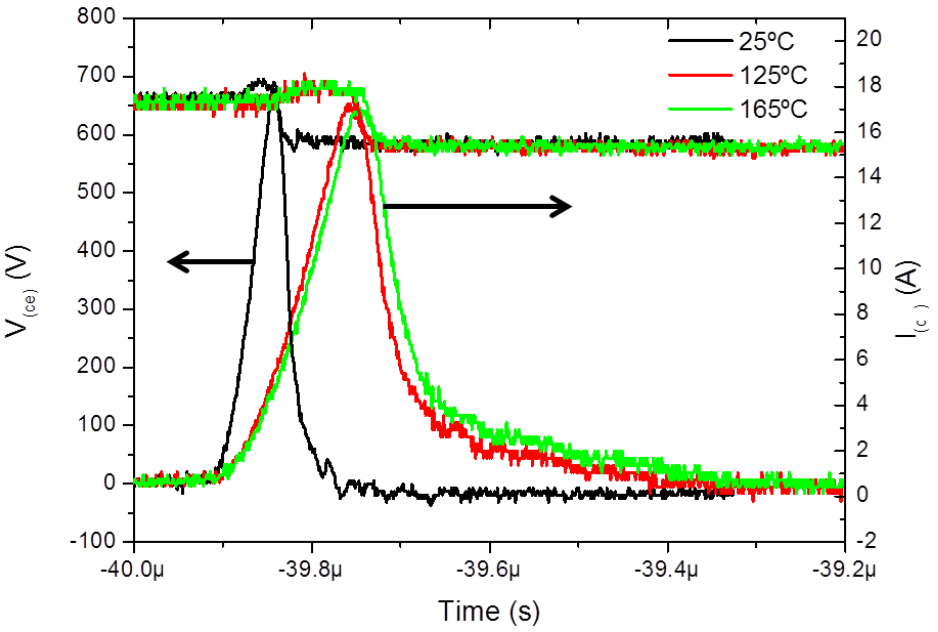


Figure 2-12 Double-pulse switching test for Si IGBT at 160ºC: CH1 (Yellow): $V_{CE,Q1}$, CH2 (Green): $V_{CE,Q2}$, CH3 (Purple): $I_{C,Q1}$

During the turn-on process, as shown in Figure 2-13a, V_{ce} falls from 600V and the collector current starts to increase gradually. Carrier lifetime, mobility and the MOS-gate threshold are temperature dependant in Si devices, therefore switching losses are temperature dependant for the Si IGBT, unlike the BJT. The switching times for both turn-on and turn-off become longer as junction temperatures increases. The di/dt shown in Figure 2-13a is 0.2×10^3A/µs and the dv/dt shown in Figure 2-13b is 5.7×10^3A V/µs at a junction temperature of 165ºC, 3-10 times smaller than those obtained from SiC BJT. The switching test rig used for Si IGBT is the same as that for SiC BJT's. However, the resonance is obviously much less due to the slower switching speed compared with SiC BJTs.



(a) Turn-on waveforms



(b) Turn-off waveforms

Figure 2-13 Switching characteristics of Si IGBT at various junction temperatures

The total switching energy losses for Si IGBTs and SiC BJTs are summarized in Figure 2-14. The power losses are calculated using Equation 1-17. For these tests, the maximum junction

temperatures of the Si IGBT are limited to 165ºC. Moreover, the switching losses of SiC BJTs are much lower than Si IGBTs from 25ºC to 240ºC and they are insensitive to the junction temperatures. The total power losses of SiC BJT are even lower than the turn-on losses of Si IGBT. These advantages make SiC BJT a competitive candidate in high frequency and high temperature applications. In terms of driver losses, the BJT consumes 422µJ for 10µs period, which is much greater than the IGBT's loss of ~20µJ, in large part due to its current driven characteristic.

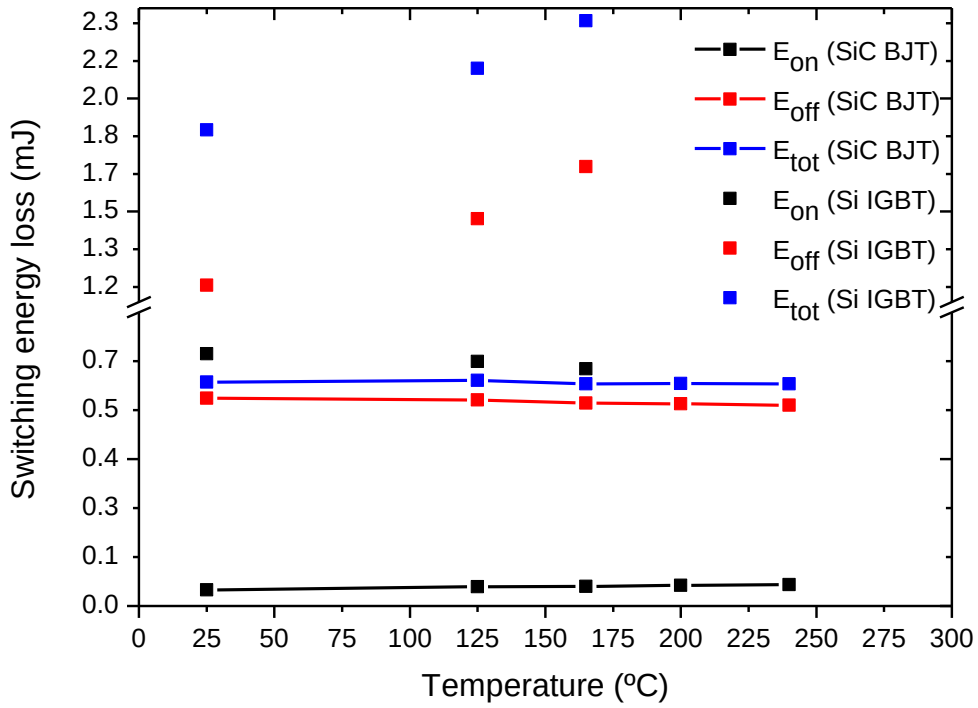


Figure 2-14 Switching energy losses comparison between SiC BJTs and Si IGBTs

In [65], the author compares 1200V SiC BJT with Si IGBT at various collector currents under the room temperature. The total switching losses of the SiC BJT is some 11 times lower than a corresponding Si IGBT at a collector current of 4.5A. In [1], the experimental results show that the switching losses of the SiC BJT is 22W less than the Si IGBT's at 150°C, 40kHz and 6A 600V, which corresponds to a switching loss reduction of ~46%. In [4], the SiC BJT has the total switching losses of approximately 550µJ and the Si IGBT has approximately 2mJ at 25°C and 20A collector current. However, none of these published studies operated the SiC

BJT at 240ºC and measured the switching losses. Testing at 240°C is undertaken in this chapter and extends the knowledge base for SiC BJTs.

2.6 Summary

This chapter has demonstrated that the switching characteristics of SiC BJTs at junction temperatures up to 240ºC. The implementation of a self-heating method for a SiC BJT has been shown to provide an effective test method.

Measured switching power losses have been shown with a double pulse test circuit at 600V/18A with respect to junction temperature. The switching speed was found to be very fast (90 ns-120 ns) for the SiC BJT and almost constant across the temperature range considered. The switching test for the Si IGBT was implemented at junction temperature 165ºC for comparison. The switching speed of the SiC BJT was shown to be 3-10 times shorter than that of the Si IGBT. Especially at high junction temperatures, the switching energy losses of the Si IGBT are almost four times larger than that of the corresponding SiC BJT's. In terms of switching performances, SiC BJTs offer the advantage of reduced power losses and temperature independency, at the expense of significant base drive losses. The base driver design which forms the focus of Chapter 3 will provide an energy recovery solution to reduce the driver losses for a high switching frequency application.

3 A Base Driver with the Energy Recovery Circuit for SiC BJT

In this chapter, for the first time, implementation of an energy recovery circuit into the base drive for the SiC BJT is demonstrated. The operating modes of the energy recovery circuit are analysed on step-by-step basis. The electrical circuit is simulated using LTSpice for both verification and estimation of driver power losses. Both simulation and experimental results confirm the driver loss reduction compared with a conventional base drive.

3.1 Introduction

Power electronic converters based on SiC device technologies have demonstrated significant advantages over Si counterparts due to a combination of low on-state losses and faster switching speeds [5, 86-89] making the device a promising candidate for future power electronic applications. For fast switching speeds the capacitance C_{pulse} in the conventional base driver, as discussed in Chapter 1 has to be large. This capacitor dissipates significant power in high frequency applications. When the base current is low, the capacitor power loss can even dominant. In order to minimize the influence of voltage fluctuation at the base terminal, which is coupled from the emitter parasitic inductance during the transient period, high DC voltage in the base drive is required, which inevitably increases the capacitance power loss within the speed up circuit. A 1.7kW DC/DC converter using SiC BJTs driven by the proposed base driver is built with a wide switching frequency ranges from 62.5kHz to 250kHz, providing a platform to evaluate the performances of the converter based on a SiC BJT and the proposed base drive.

3.2 Functionality of the proposed base drive

3.2.1 Operation modes

The schematic of the energy recovery base driver is shown in Figure 3-1a along with a timing diagram for a complete cycle. Symbols shown in time scheme can be found in the following analysis. The energy recovery function causes the power supply current, I_{DD}, to have a negative current value as the energy flows into the supply. Compared to the traditional base drive, as shown in Figure 1-24, the additional electrical components utilized in the proposed structure are diodes (D1, D2), inductor (L) and MOSFETs (SW2, SW3).

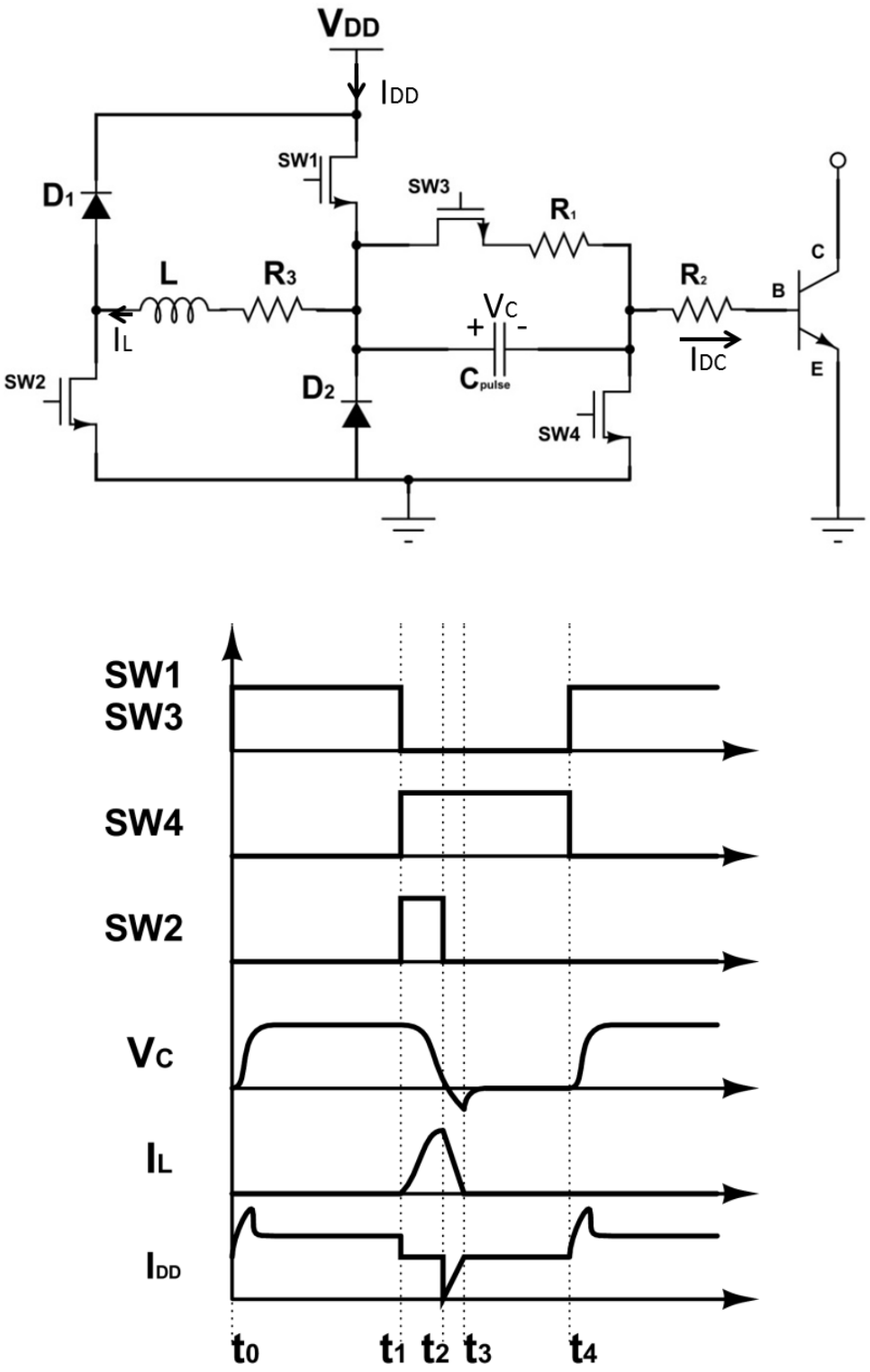


Figure 3-1a Equivalent circuit of the energy recovery base drive and typical time scheme

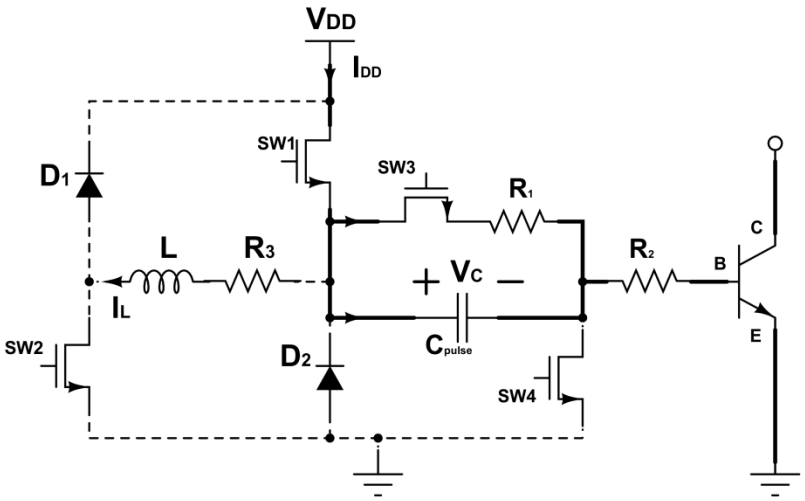


Figure 3-1b Equivalent circuit of the energy recovery base drive during Mode 1

Mode 1: t_0--t_1 (Figure 3-1b)

Initially the BJT is considered to be in its off-state. In order to turn the SiC BJT on, a gate signal is applied to turn SW1 and SW3 on while SW2 and SW4 are off. This causes a base current to flow through SW3, R_1 and C_{pulse}, as shown Figure 3-1b. The power supply current (I_{DD}) provides a peak current to the base drive for fast switching as shown in Figure 3-1a. During this mode the energy recovery portion of the drive is inactive and the circuit operates in a similar manner as a conventional drive, Figure 1-24. During the on-state operation of the BJT, the pulse capacitor is effectively charged to the level of the power supply (V_{DD}) minus the voltage dropped across the base resistor (R_2) and the emitter base junction. DC base current (I_{DC}), which maintains the on-state of the BJT, is set up by R_1 and R_2.

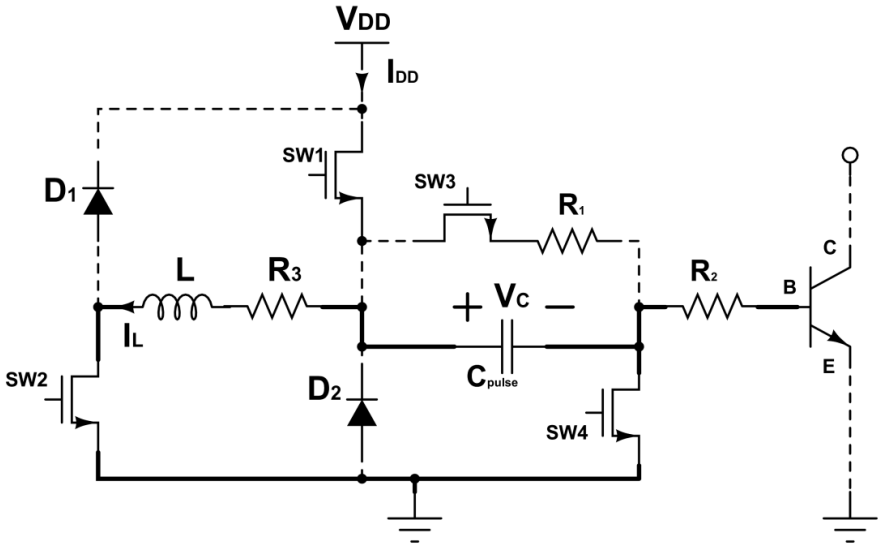


Figure 3-1c Equivalent circuit of the energy recovery base drive during Mode 2

Mode 2: t_1--t_2 (Figure 3-1c)

After its on-state, the turn-off process starts by switching SW1 and SW3 off, interrupting the base current and connecting the base terminal to the emitter potential. Whilst SW1 and SW3 are maintained in the off-state, SW2 and SW4 are turned on which directs the energy stored in C_{pulse} into the inductor (L), as shown in Figure 3-1c. If we assume that SW2 and SW4 are turned on at t_1, the inductor current (I_L) and capacitor voltage (V_C) can be obtained as:

$$I_L = \frac{V_{DD} - V_{be(sat)}}{\omega_d L} e^{-\alpha t} \sin(\omega_d t) \quad \textbf{3-1}$$

$$V_c = \frac{V_{DD} - V_{be(sat)}}{\omega_d} \omega \cdot e^{-\alpha t} \sin(\omega_d t + \theta) \quad \textbf{3-2}$$

Where

$$\omega = \frac{1}{\sqrt{LC_{pulse}}} \quad \textbf{3-3}$$

$$\omega_d = \sqrt{\omega^2 - \alpha^2} \quad \textbf{3-4}$$

$$\alpha = \frac{R_3}{2L} \quad \textbf{3-5}$$

And then

$$tan\,\theta = \frac{\omega_d}{\alpha} = \frac{\sqrt{\omega^2 - \alpha^2}}{\alpha} = \sqrt{\frac{4L}{C_{pulse}R_3^2} - 1} \quad \textbf{3-6}$$

Where $V_{be(sat)}$ is the base-emitter saturation voltage. The inductor stores maximum energy at t_2, as shown in Figure 3-1a. This time interval (t_2-t_1) can be obtained by solving Equation 3-1 considering $\frac{dI_L}{dt} = 0$:

$$t_2 - t_1 = \theta/\omega_d \quad \textbf{3-7}$$

In an ideal case, there are only C_{pulse} and L in the path and no resistance (R_3=0). The maximum inductor current will occur when the capacitor voltage is equal to zero. However, for the case in which a damping resistor (R_3) is inserted, there is a change in the phase angle between voltage and current in LC. In such case, the capacitor voltage reaches zero at $t = (\pi - \theta)/\omega_d$. A non-zero capacitor voltage (V_c) will influence the peak of the turn-on base current in the next cycle. From this point of view, according to Equations 3-6 and 3-7, the variations of the inductance (L) and capacitance (C_{pulse}) will impact both the turn-on power loss of the BJT and the maximum energy recovery rate. When the capacitor voltage (C_{pulse}) becomes negative at t_2, as shown in Figure 3-1a, the current freewheels through SW2, D2, L, R_3. Due to V_C clamping to a negative potential, the resonance between inductor and capacitor will stop. The freewheeling period must be as short as possible to reduce the power losses in this current path.

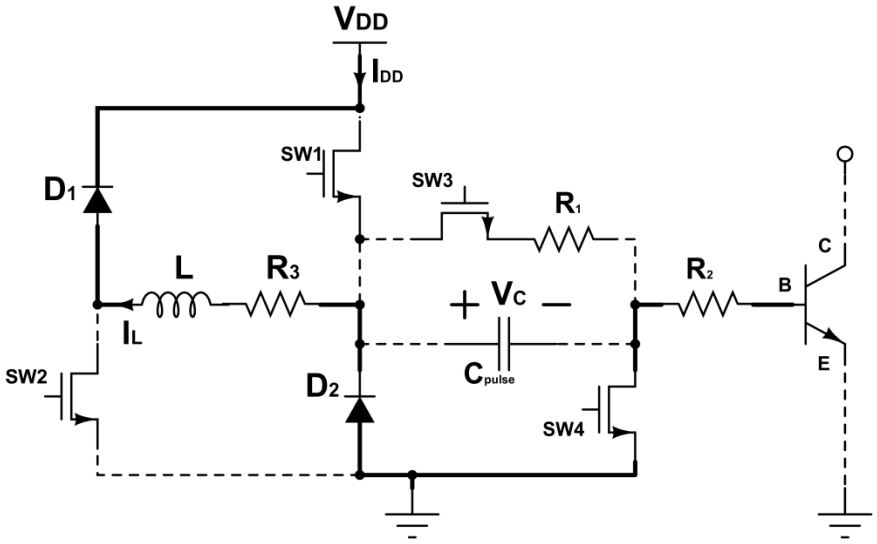


Figure 3-1d Equivalent circuit of the energy recovery base drive during Mode 3

Mode 3: t_2--t_3 (Figure 3-1d)

Mode 3 occurs when SW2 is turned off to divert the inductor stored energy back to the voltage supply via D_2 and D_1, as shown in Figure 3-1d. Due to the resonance between C_{pulse} and L, the voltage of V_C becomes negative when all the energy is transferred into L. At this point (t_2), the current flows through D_2. The effective resistance of the components in the current flow path reduce the efficiency of the energy recovery circuit. The current in the inductor flows back to V_{DD}, creating a negative current pulse added onto power supply current (I_{DD}) as shown in Figure 3-1a.

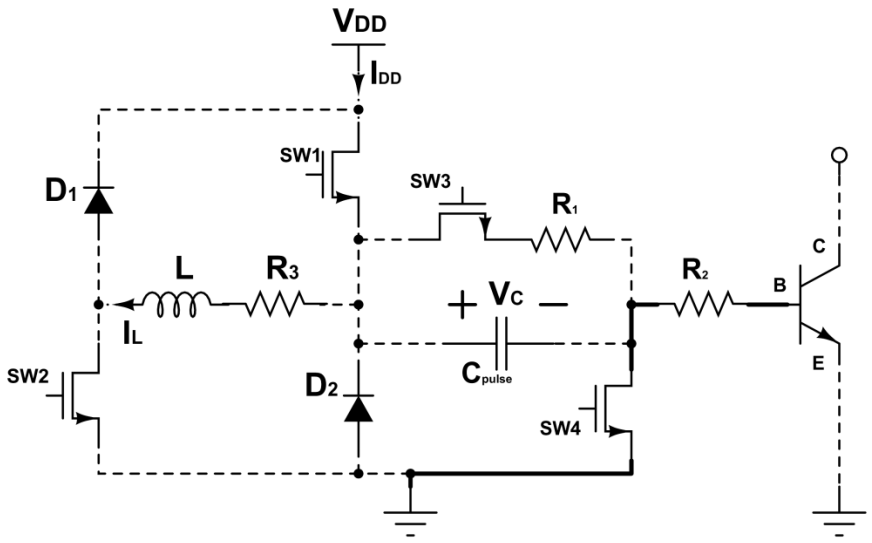


Figure 3-1e Equivalent circuit of the energy recovery base drive during Mode 4

Mode 4: t_3--t_4 (Figure 3-1e)

Once the energy stored in the inductor had been transferred into the voltage supply, the circuit operates in Mode 4. R_2 and R_3 are used to dampen any resonance introduced by the stray inductance or capacitance. At the point the energy recovery is completed, the circuit is ready for the next turn-on signal for the next cycle (Mode 1). According to the BJT datasheet, the base-emitter capacitance is only 16nF, this is almost six times smaller than C_{pulse}. Moreover, the base-emitter saturation voltage is around 3.2V, which is lower than the voltage of the capacitor (C_{pulse}). The associated energies illustrate that in order to recovery the energy stored in base-emitter capacitor (C_{BE}), the cost is too high for such small amount of energy.

3.2.2 Driver loss analysis from the simulation

The power loss and energy recovery efficiency have been analysed in LTSpice. In order to simulate the circuit accurately, a representative SiC BJT model provided by the manufacturer is used [18] and listed in Table 3-1:

Table 3-1 BT1220 NPN SPICE model

Parameters	Description	Units	Value
IS	Transport saturation current	A	5.1×10^{-48}
BF	Ideal maximum forward beta	no unit dimension	74
NF	Forward mode ideality factor	no unit dimension	1
ISE	Base-emitter leakage saturation current	A	7.56×10^{-26}
NE	Base-emitter leakage emission coefficient	no unit dimension	2
BR	Ideal maximum reverse beta	no unit dimension	0.16
RB	Zero-bias (maximum) base resistance	Ohm	0.076
RC	Collector ohmic resistance	Ohm	0.0175
XTI	IS temperature effect exponent	no unit dimension	3
XTB	Forward and reverse beta temperature coefficient	no unit dimension	-1.1
EG	Bandgap voltage (barrier height)	eV	3.2
TRC1	First order temperature coefficient for RC	1/°	4×10^{-3}
CJE	Base-emitter zero-bias p-n capacitance	F	5.72×10^{-9}
VJE	Base-emitter built-in potential	V	2.9
MJE	Base-emitter p-n grading factor	no unit dimension	0.5
CJC	Base-collector zero-bias p-n capacitance	F	2.5×10^{-9}
VJC	Base-collector built-in potential	V	2.9
MJC	Base-collector p-n grading factor	no unit dimension	0.5

I-V characteristics of the model are compared with the data extracted from the datasheet. As shown in Figure 3-2, the SPICE model can replicate reasonably well the device datasheet performance with different current base and have the identical current gain.

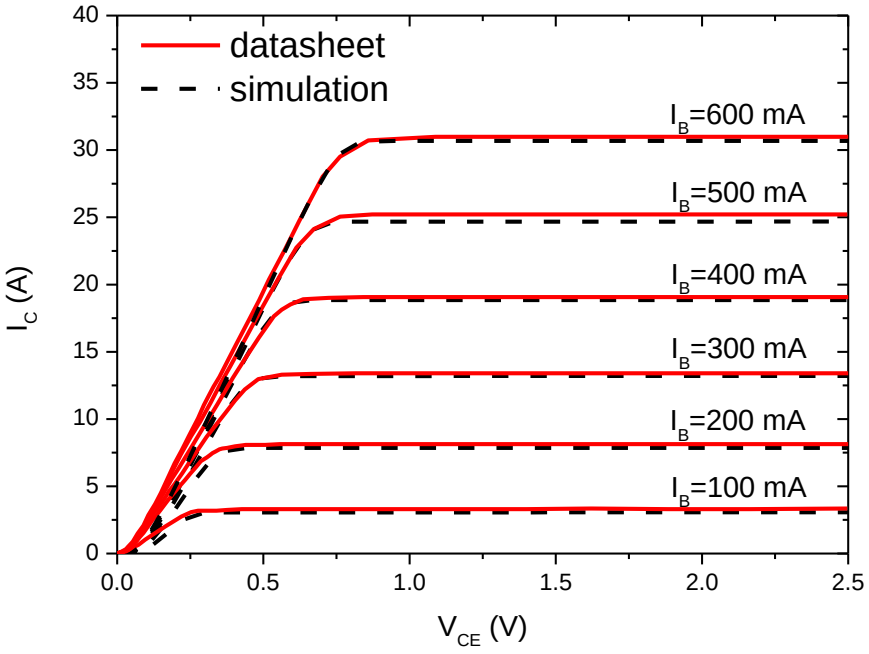
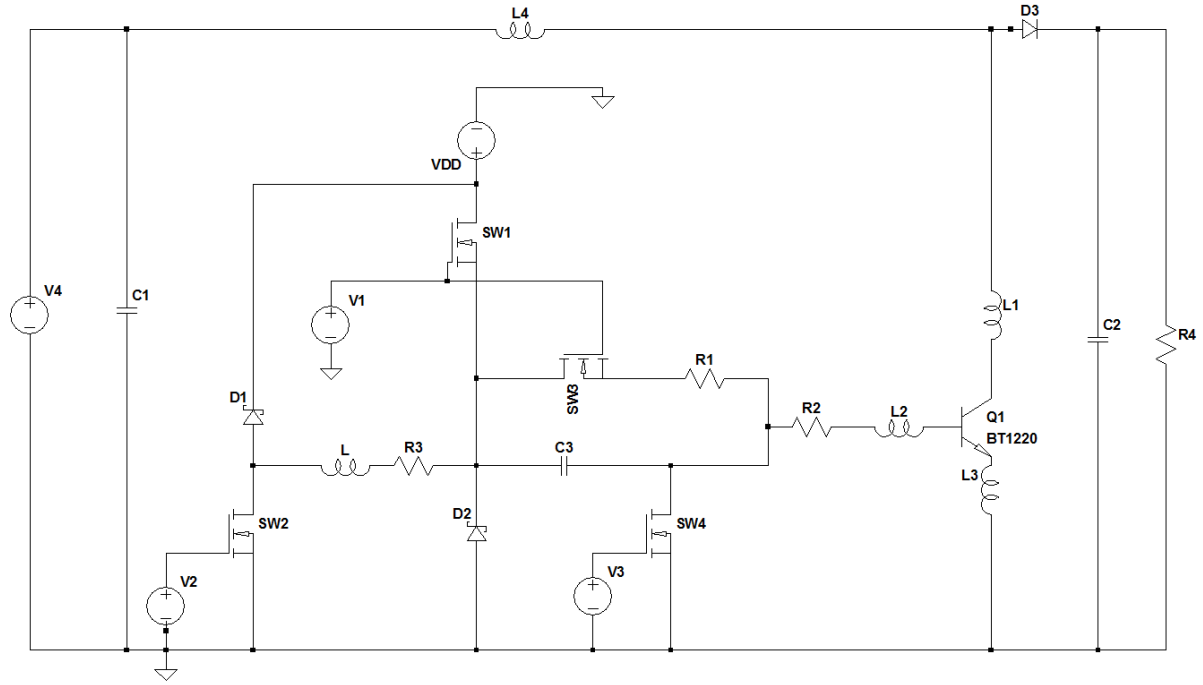
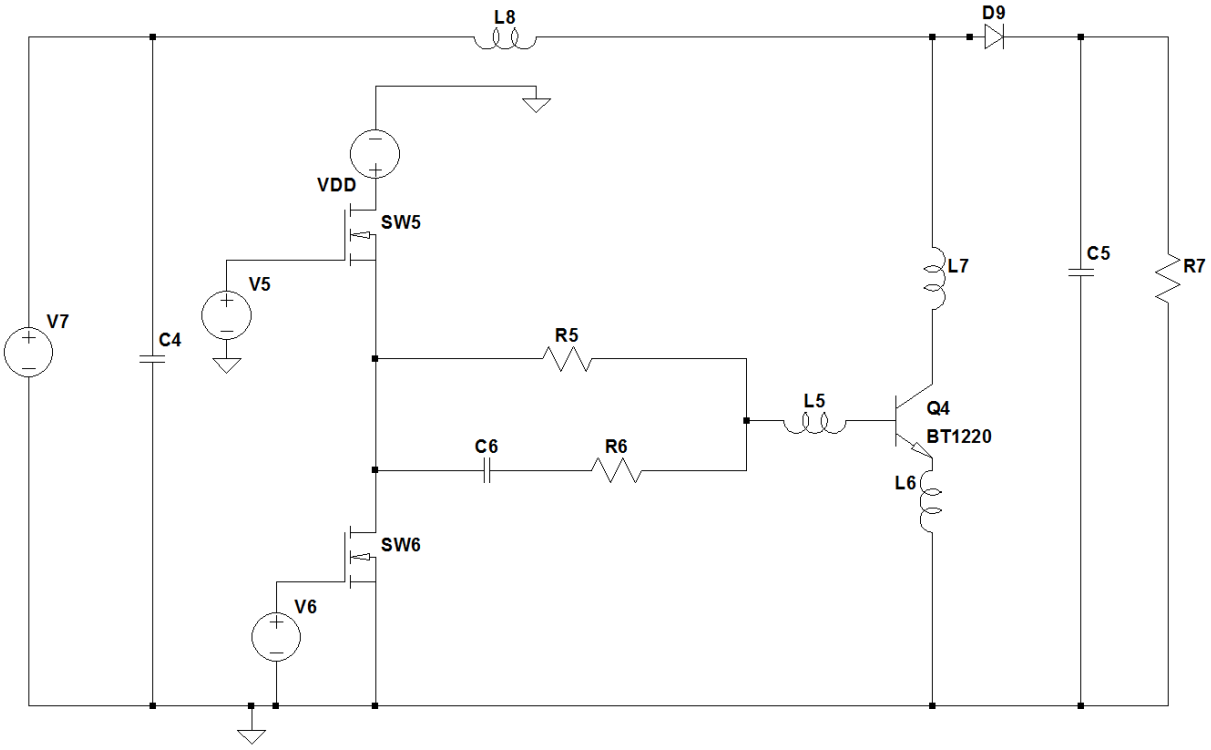


Figure 3-2 SiC BJT simulation model I-V characteristics

The proposed base drive design circuit schematic is shown in Figure 3-3a. For simulation purposes, the driver is applied to a DC/DC boost converter. Compared to the conventional base driver shown in Figure 3-3b, the additional diodes (D_1 and D_2), switch (SW2) and inductor (L) are used to recover energy from the pulse capacitor (C_{pulse}) back to the DC line (V_{DD}). The power loss caused by these additional components decreases the efficiency of the energy recovery circuit. Power losses of all low voltage MOSFETs (SW1-4) and diodes (D1-2) are included since they are not ideal devices in simulation. Transient performances and on-state voltage drops are based on the real device specifications. DC/DC converter design and parameters will be elaborated in next section.



(a) Energy recovery circuit



(b) Conventional base driver

Figure 3-3 Simulation circuit for the energy recovery base driver and conventional driver for the SiC BJT

The parasitic inductances introduced by the package of the BJT taken from the datasheet are included in the simulation as shown in Figure 3-3. The parasitic inductance, L2 (25nH), is added to the base terminal which leads to resonance with the pulse capacitor; L1 and L3 are attached to the collector and emitter terminals result in the electrical stress on the BJT during the switching transients. Attenuation resistor R_2 is added close to the base terminal to reduce the resonance effect in the energy recovery circuit. It will consume the power during the energy recovery if it is put in series with C_3 as the conventional driver does in Figure 3-3b. Moreover, this resistor controls the base peak current during turn-on.

Table 3-2 Simulation parameters of the energy recover base drive

DC power supply	V_{DD} = 10 V
Base resistor	R_1=15 Ω
Damping resistor	R_2=1.5 Ω
	R_3=0.18 Ω
Pulse capacitor	C_3 = 100 nF
Inductor	L = 1μH
Diode (D_1,D_2)	NXP PMEG2005
Switch (SW1-4)	IRLML6246

The SPICE models of the electrical components in the base driver are listed in Table 3-2 for Figure 3-3a. The maximum collector current of Q3 and Q4 in the simulation is 10A and assume that the junction temperature is kept below 100°C. The current gain under these conditions is approximately 35. Therefore, the DC base current (I_{DC}) needs to be 420mA, which is calculated based on Equation 1-19. The total resistance of R_1 and R_2 is 16.5Ω when the power supply, V_{DD}, equals to 10V for the required I_{DC}. The initial base current peak can be described as an exponential function:

$$i_{B(t)} = \frac{V_{DD} - V_{be(sat)}}{R_{SW1} + R_2} \times e^{-\frac{t}{(R_{SW1}+R_2)C_3}} \quad \textbf{3-8}$$

Where R_{SW1} is the on-state resistance of the MOSFET 1 (SW1), which is 45mΩ.

By integrating Equation 3-8, the charge injected into the base yields:

$$Q_{B(t)} = C_3 \times (V_{DD} - V_{be(sat)}) \times (1 - e^{-\frac{t}{(R_{SW1}+R_2)C_3}}) \quad \textbf{3-9}$$

We can solve this equation for t:

$$t = -(R_{SW1} + R_2) \times C_3 \times \ln(1 - \frac{Q_B}{(V_{DD} - V_{be(sat)})C_3}) \quad \textbf{3-10}$$

$Q_{B(t)}$ for the SiC BJT used in the thesis at 500V is 180nC. The turn-on time of t can be found by putting the parameters into Equation 3-10, which results in 45.9ns for the proposed design. Given the values of L, C_3 and R_3 in Table 3-2, the conduction time of SW2 is set to 510ns by solving Equations 3-3 to 3-7 for $t_2 - t_1$. Therefore, 510ns is required as the minimum off-time to complete the whole energy recovery process. If the application does not need to switch the SiC BJT, the energy recovery driver is able to provide DC base current to keep it conducting. However, many applications, such as inverters, need to turn on and off the BJT and insert a dead-time to ensure no short-through in a leg. The maximum duty cycle for the energy recovery driver yields:

$$D_{max} = \big(1 - f(t_2 - t_1)\big) \times 100\% \quad \textbf{3-11}$$

Where f is the switching frequency and $t_2 - t_1$ is the on-time of SW2 as specified in Equation 3-7.

Before committing the energy recovery driver to hardware, it is necessary to ensure correct operation of the system. If the maximum duty cycle does not meet the requirement of the design, it is possible to modify the value of the inductance of L in Figure 3-3a to either increase or reduce $t_2 - t_1$so as to adjust D_{max}. It is also possible to change the capacitance of C_3. However, this will inevitably affect the turn-on time. The maximum duty cycle is plotted in Figure 3-4 with parameters set in the simulation in Table 3-2.

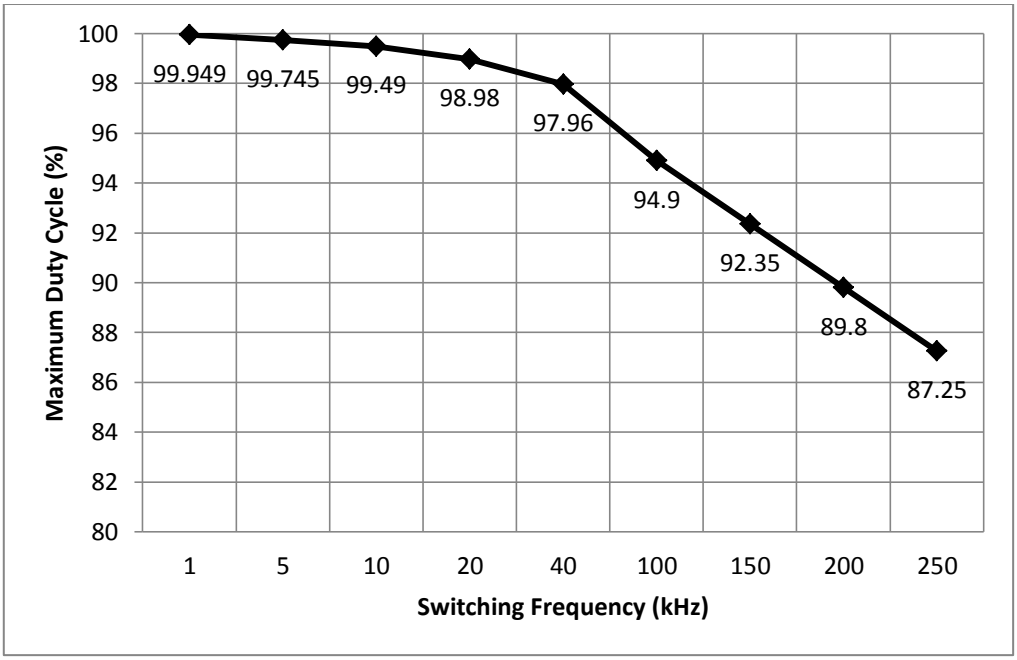


Figure 3-4 Maximum Duty Cycle vs. Frequency

The conventional base driver is simulated as the circuit is shown in Figure 3-3b for the purposes of comparison with the proposed base driver. The parameters of each component are listed in Table 3-3 following the same selection steps introduced above to satisfy the same specifications for the DC base current and peak current.

Table 3-3 Simulation parameters of the conventional base drive

DC power supply	V_{DD} = 10 V
Base resistor	R_5=16.5 Ω
Damping resistor	R_6=1.7 Ω
Pulse capacitor	C_6 = 100 nF
Switch (SW5,6)	IRLML6246

Figure 3-5 shows simulation waveforms for the proposed base driver shown in Figure 3-3a at Pulse Width Modulation (PWM) frequency of 250kHz. The voltage of the pulse capacitor (V_C) is charged during the turn-on to approximately 6.5V (in Mode 1). At the same time, the power supply provides a current peak to the base for fast switching. The inductor starts to store energy transferred from C_{pulse}, causing current I_L begins to rise (Mode 2); this time period can be calculated by Equation 3-7. After V_C has been discharged, inductor current, and

hence stored energy, flows back from the inductor into the power supply, causing a negative current pulse on I_{DD} (Mode 3). Finally, the current I_{DD} and $I_L$become zero, as shown in Mode 4 and the circuit is ready for the next pulse. The duty cycle in the simulation and experiment has been set to 40%. Base on Equation 1-23, the power losses of the pulse capacitor is only related to the capacitor voltage, capacitance value and the switching frequency.

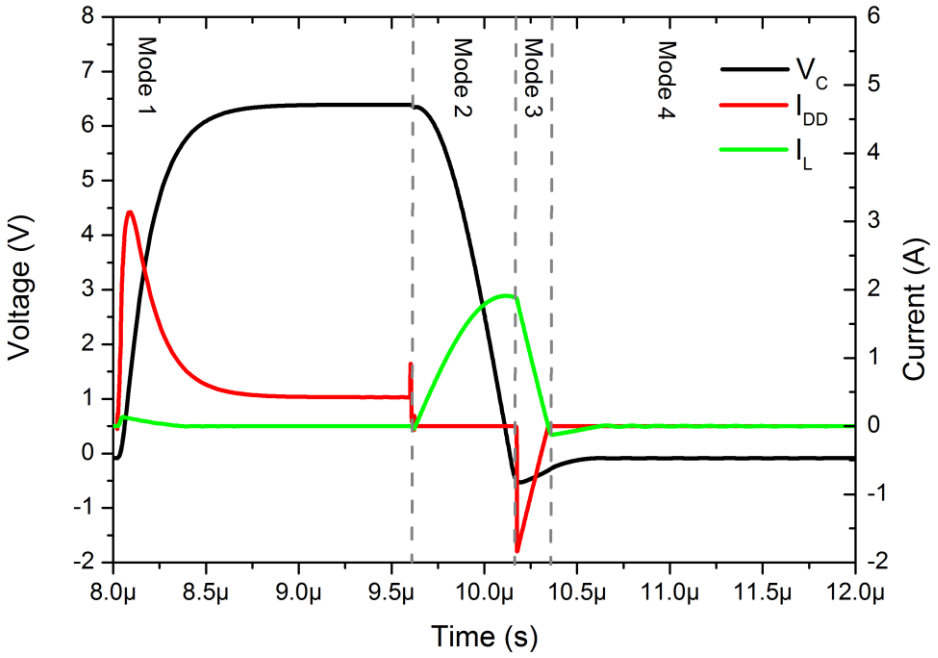


Figure 3-5 Energy recovery waveforms in the simulation for the energy recovery base drive

The base current peak value strongly depends on the capacitance of C_3 and resistance of R_2 in the schematic in Figure 3-3a. The tolerance of C_3 is ±20% and R_2 is ±10% in the prototype. The effect of component tolerances on performance was a series of combinations, i.e. (+110%R_2, +120%C_3), (+110%R_2, 80%C_3), (90%R_2, +120%C_3), (90%R_2, 80%C_3) and (R_2, C_3). The base peak current waveforms obtained from the simulation are shown in Figure 3-6, taking the tolerances into the consideration. As shown in the figure, the maximum base peak current (red line) occurs when C_3 is 20% larger and R_2 is 10% lower than their normal values respectively. The minimum base peak current (green line) appears when C_3 is 20% lower and R_2 is 10% larger than their normal values. The blue line shows the current waveform with normal values of C_3 and R_2. The difference is 0.7A between red and green lines. All the rest of results using the other combinations will fall in the range between red and green lines.

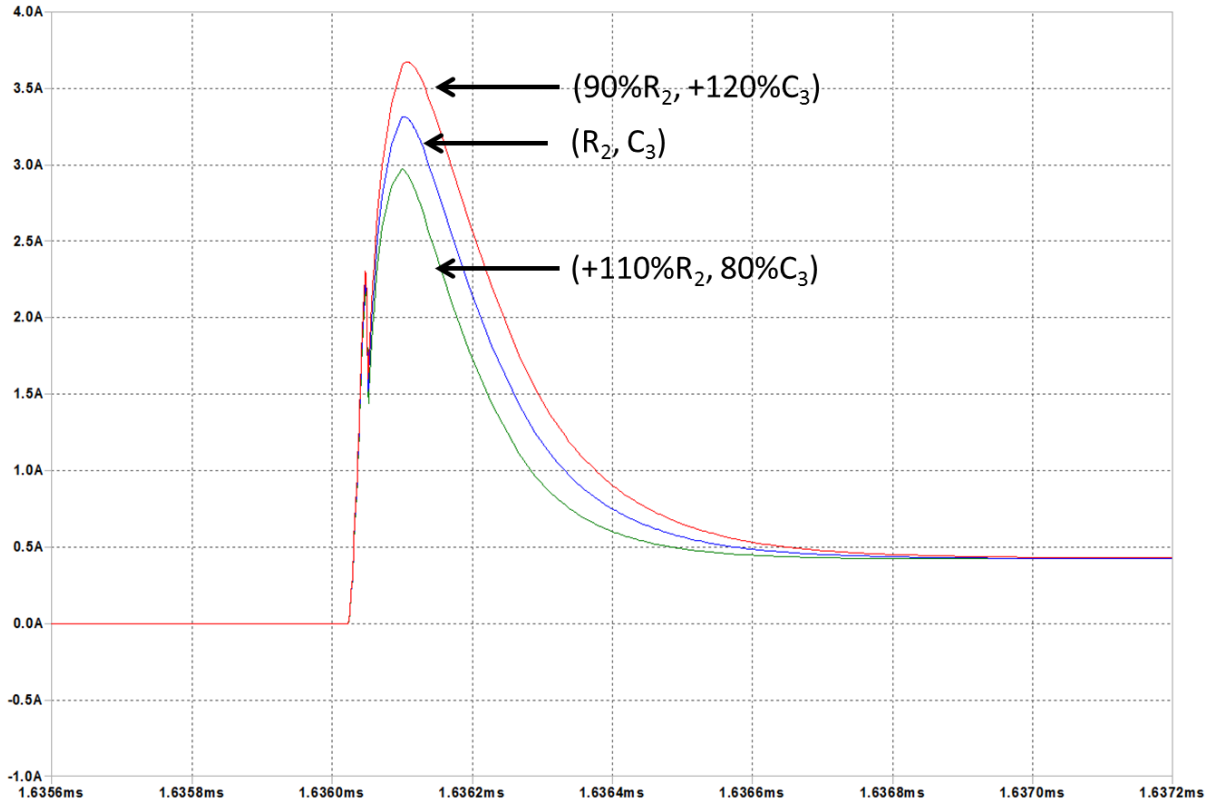


Figure 3-6 Simulated influence of component tolerance on base current waveforms

Power losses for a conventional base drive (P_{con_loss}), as shown in Figure 3-3b, and the proposed (P_{pro_loss}) base drive, as shown in Figure 3-3a, with respect to PWM switching frequency are shown in Figure 3-7. Both P_{pro_loss} and P_{con_loss} are simulation results obtained from LTSpice. Due to the strong frequency-dependency, total driver losses increase linearly with the frequency as indicated in simulation results, Figure 3-7. The power saving (P_{ER}) due to the energy recovery function can be defined as:

$$P_{ER} = P_{con\_loss} - P_{pro\_loss} \qquad \textbf{3-12}$$

If the duty cycle changes, the energy stored in the boost capacitor will not be influenced as discussed in Chapter 1. Therefore, the power (P_{ER}) does not change. The total power losses for both drivers increase due to larger resistance losses. At very low switching frequencies, losses will be very close to each other since the capacitance power losses are low. At high switching frequencies, the conventional driver will not turn on the BJT efficiently. This aspect of behavior is illustrated in the following section.

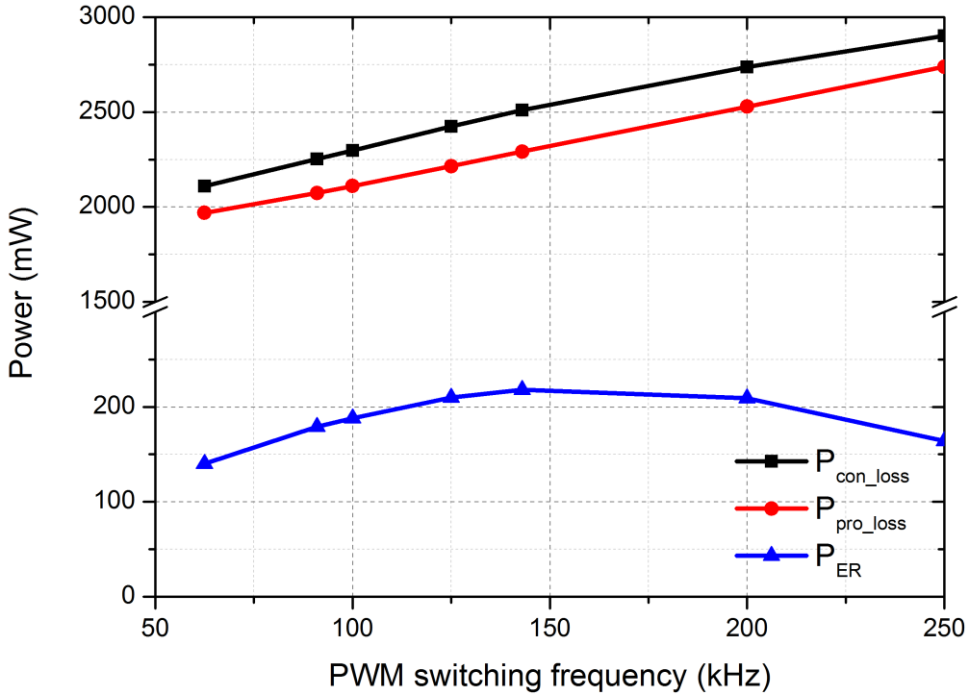


Figure 3-7 Power losses vs. switching frequency in simulation

Additional electrical components can increase P_{pro_loss} and consequently reduce P_{ER}. However, it is worth noting that these losses contribute a small proportion of total power consumption. Simulation power losses of additional devices, D_1, D_2, SW2, SW3, R_3 and inductor L are listed in Table 3-4.

Table 3-4 Power losses of additional components in the energy recovery circuit

	63kHz	**143kHz**	**200kHz**	**250kHz**	**Unit**
D_1	5.4	11.92	16.67	20.85	mW
D_2	6.5	14	19.5	24.6	mW
SW2	5.4	12.15	17	21.3	mW
SW3	6.12	6.39	6.6	6.7	mW
R_3	14.6	32.7	45.5	57	mW
L	3.5	7.8	10.9	13.6	mW

The power consumption of the resistors is frequency-independent and can only be reduced by decreasing the resistance (R_1, R_2) or the base driver power supply (V_{DD}). Since the power loss of capacitor C_{pulse} is strongly related to switching frequency (f_s), theoretically the recovered power (P_{ER}) should increase with switching frequency. However simulation shows that the energy recovered reduces when switching frequency is increased beyond 143kHz.

Figure 3-8 shows the supply current (I_{DD}) and pulse capacitor voltage (V_C) in a conventional base drive at the switching frequency of 250kHz. The initial pulse capacitor voltage (V_C) is 1V at the beginning of the turn-on process. This consequently reduces the power loss of the capacitor due to the reduction of pulse capacitor voltage. Therefore, P_{ER} decreases due to reduced capacitance loss at high switching frequencies. In terms of turn-on loss, a non-zero pulse capacitor voltage (V_C) results in a reduced current peak and consequently a slower switching speed. Compared to a 4.5A peak drive current for the proposed circuit, as shown in Figure 3-5, this reduced to approximately 3.4A for a conventional base drive unit as shown in Figure 1-24. Therefore, the maximum applicable switching frequency, which is around 150kHz found in the simulation, is internally limited by a long discharge time constant of the pulse capacitor (C_{pulse}) for a conventional base drive structure.

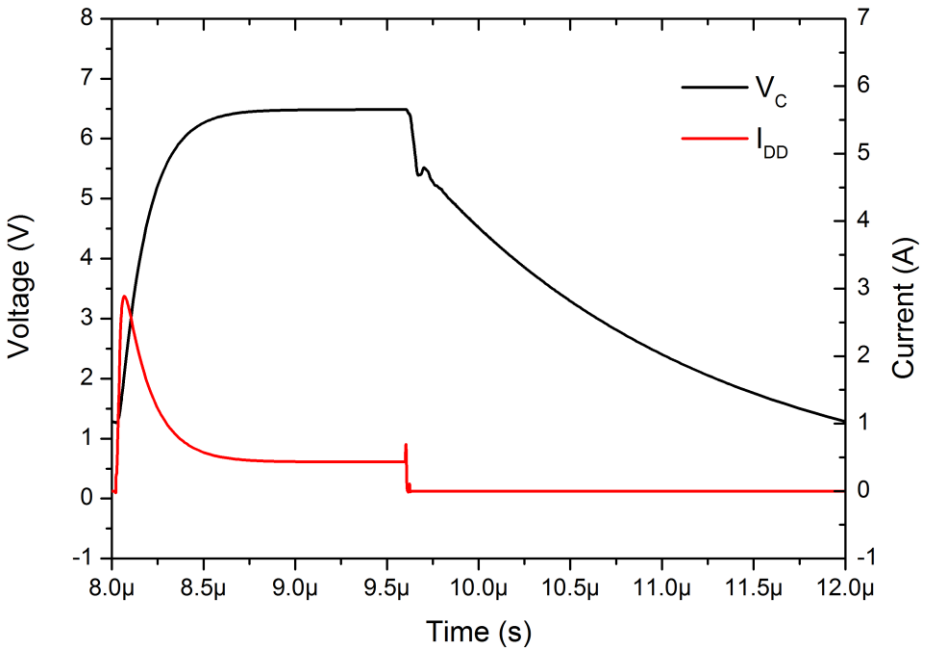


Figure 3-8 Power supply current (I_{DD}) and pulse capacitor voltage (V_C) in the conventional base driver

3.2.3 Simulation for the boost converter with proposed drive and control loop

A boost converter with a closed control loop is simulated in LTSpice, as the schematic shown in Figure 3-9. The energy recovery circuit is used to drive SiC BJT in this application and the drive circuit itself has been analysed in the simulation in the last section. The converter is capable of regulating its output voltage at 500V from 300V DC input with the proposed control circuit, which is mainly composite of: re-scaling resistors (R6 and R8) for the feedback of the output voltage ($V_{feedback}$), three comparators (U1-3) to generate PWM signals ($V_{control\_H}$ and $V_{control\_L}$) and three reference voltage sources (V5, V6 and V7). In order to regulate Vout1 at 500V, $V_{feedback}$ needs to be controlled to within 2V by the closed-loop. Therefore, the reference voltage V7 is set to 2V in Figure 3-9. C3 and U1 form a basic integrator to integrate the error between $V_{feedback}$ and V7 which can effectively avoid SW1 and SW4 from continuously working in 0% or 100% duty cycle situation. The output of U1 is comparing with a triangle wave voltage V3, the frequency of which is 62.5kHz. The output of U2 is a PWM signal to control SW1. V1, V2 and V3 are level-shifters to boost the control signal to 15V to switch on the MOSFETs. U3 is used to invert $V_{control\_H}$ to generate $V_{control\_L}$ PWM signal for SW4. As to avoid SW1 and SW4 from turning on at the same time, V5 with a positive value can delay the inverting process of $V_{control\_H}$.

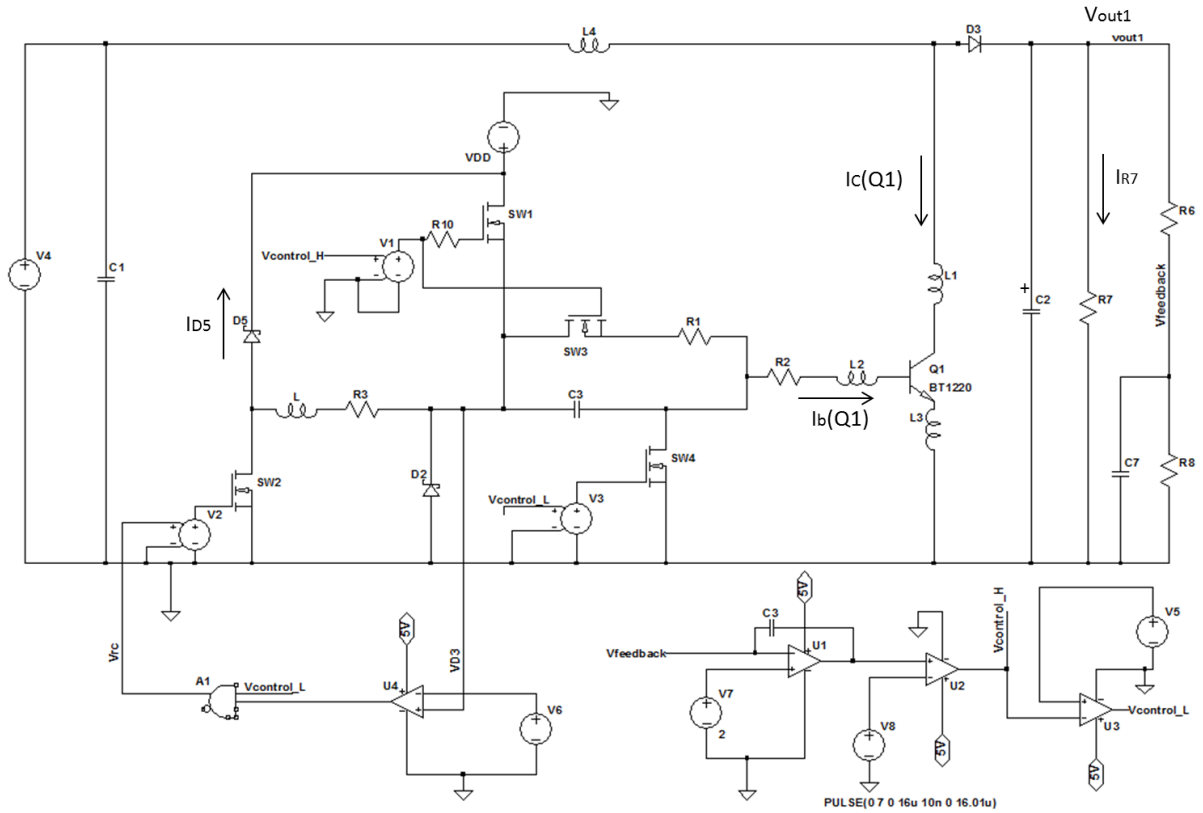
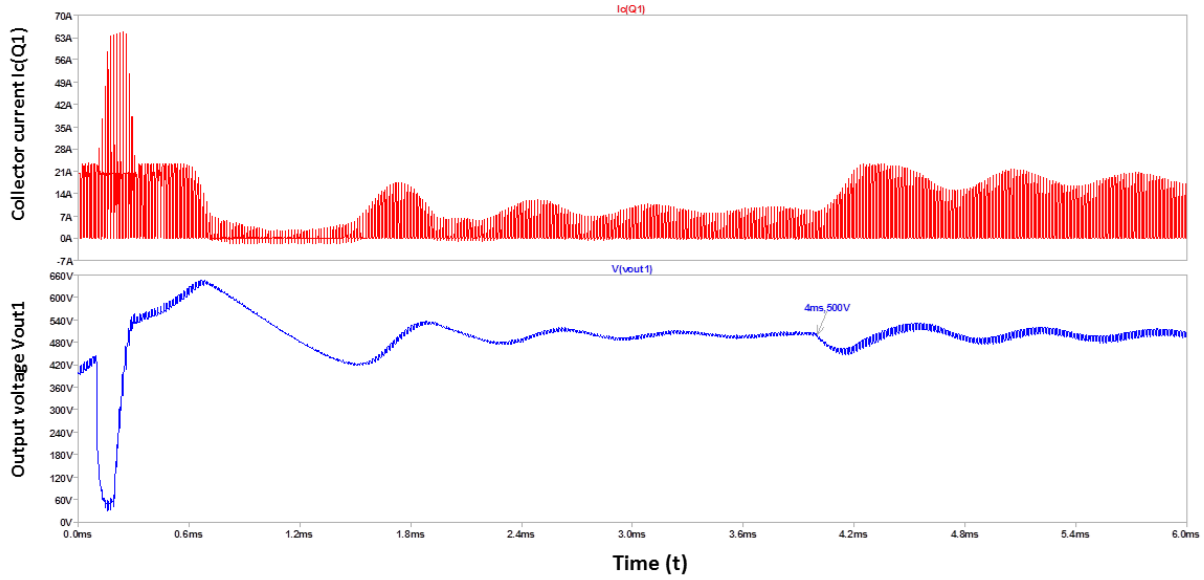


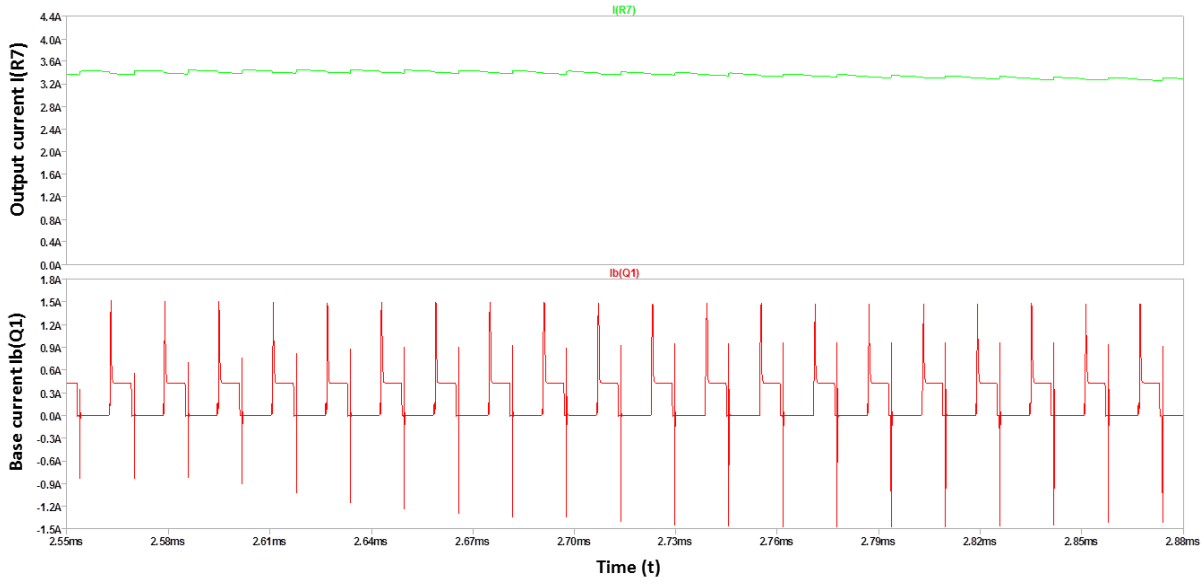
Figure 3-9 Converter simulation circuit

In order to validate the closed-loop design, the step response of the converter is simulated with the proposed driver technology. The load resistance of R7 will change at different time points in the simulation to create various load currents. . The response to a step-change in load is shown in Figure 3-10a, which includes the collector current of the SiC BJT (I_C(Q1)) and the converter output voltage (V_{out1}). An initial voltage of 400V was set to the output capacitor (C2) for fast simulation and the initial resistance of R7 is 150Ω in the simulation. At 100µs time point in Figure 3-10a, R7 is changed to 1Ω, which forms a low impedance path and reduced the output voltage (Vout1) to a minimum 30V for 100µs. Since the design is not supposed to accommodate such high current to the load, the output voltage reduces to a low level and the collector current overshoots An initial state of the converter for the step response has been achieved with such low output voltage. Afterwards R7 changes back to 150Ω and the output voltage increases quickly to its regulated voltage. During this process, the converter increase its duty cycle of $V_{control\_H}$ in order to provide power quickly to the load R7, which inevitably raises the collector current (I_C(Q1)) however still below 20A. When the output voltage is regulated at 500V at 2.7ms, the duty cycle is stable at 33% with the output

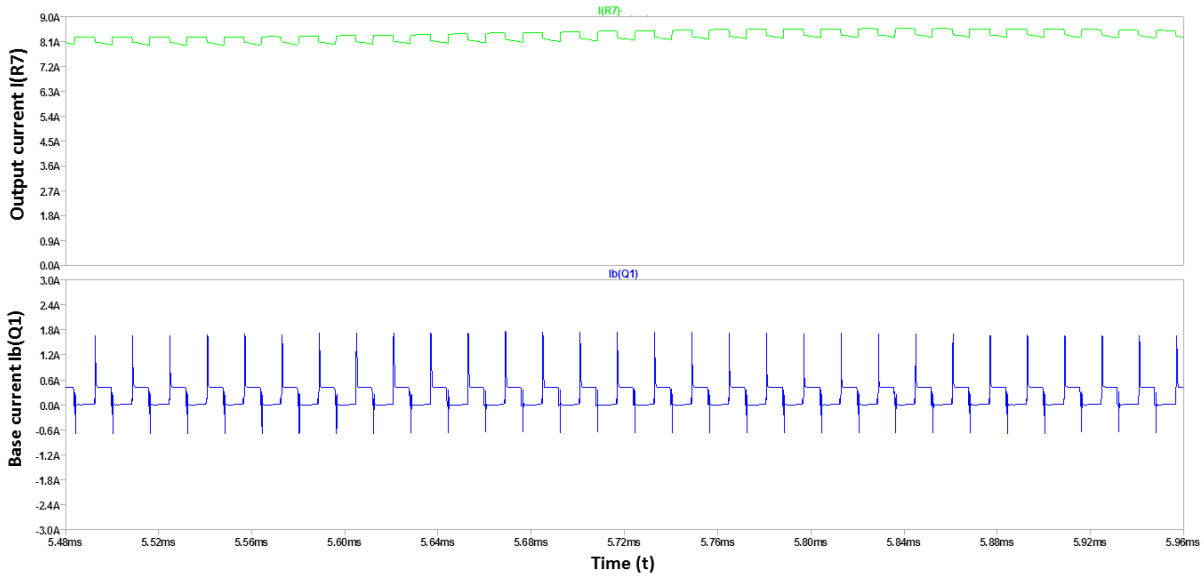
current 3.3A, as shown in Figure 3-10b. At time point 4ms as shown in Figure 3-10a, R7 is set to 100Ω, requiring 8.3A output current. When the output voltage becomes stable again at 500V at 5.5ms, the duty cycle of the base current is 51%, as shown in Figure 3-10c. Therefore, the control mechanism and the gate driver are functional and capable of adjusting the duty cycle to maintain the output voltage at 500V.



(a) Step response of the converter



(b) 33% duty cycle for 3.3A output current



(C) 51% duty cycle for 8.3A output current

Figure 3-10 Step response and duty cycle variation simulation results for the boost converter

The operation of the energy recovery circuit is not affected by the step change of the load and operates correctly to provide adequate base current to the SiC BJT as shown in Figure 3-11. In order to transfer the energy stored in the pulse capacitor (see Mode 2 and Mode 3 as described in section 3.2.1), the switch (SW2) in Figure 3-9 must be turned on at the same time when SW4 is turning on, and SW2 must be turned off as soon as the diode (D2) cathode voltage (V_{d3}) is negative. These requirements can be satisfied by using an AND gate (A1), as shown in Figure 3-9. The implementation of this time sequence can be seen in Figure 3-11: the gate signals of SW2 and SW4 (V_{rc} and $V_{control\_1}$ respectively) start to rise at the same time to turn on simultaneously; after a short time period, SW2 is turned off by a low V_{rc} when V_{d3} is negative (-514mV as measured in the simulation). Therefore, SW4 is triggered by two measured parameters ($V_{control\_1}$ and V_{rc}) at the real-time instead of a fixed pre-set value. A positive current pulse (I_{D5}) through D5 (in Figure 3-9) is observed which implies that the energy has been successfully regained by the power supply without being influencing by the control loop and the operation of the converter.

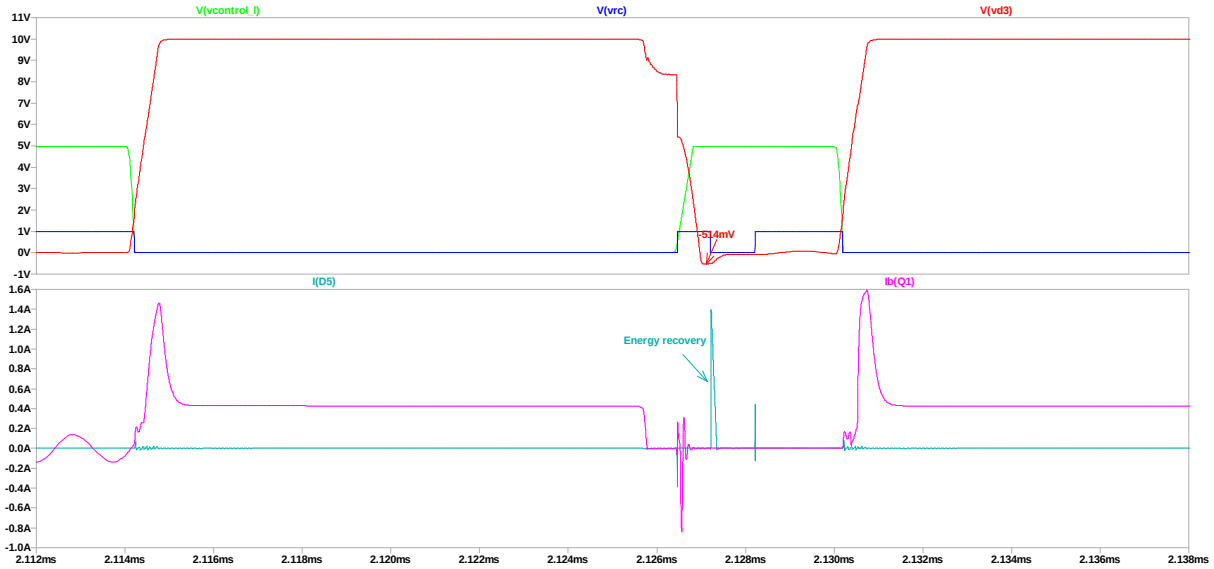


Figure 3-11 Energy recovery waveforms in the simulation

3.2.4 Verification of the energy recovery concept

In order to verify the energy recovery concept, a PCB prototype based on the circuit diagram shown in Figure 3-1a was manufactured, as shown in Figure 3-12. The detailed layout is shown in Appendix 8-3. Only the base driver was manufactured and tested. This board was not used in a power converter/inverter in this section and it is an open-collector configuration for the SiC BJT.

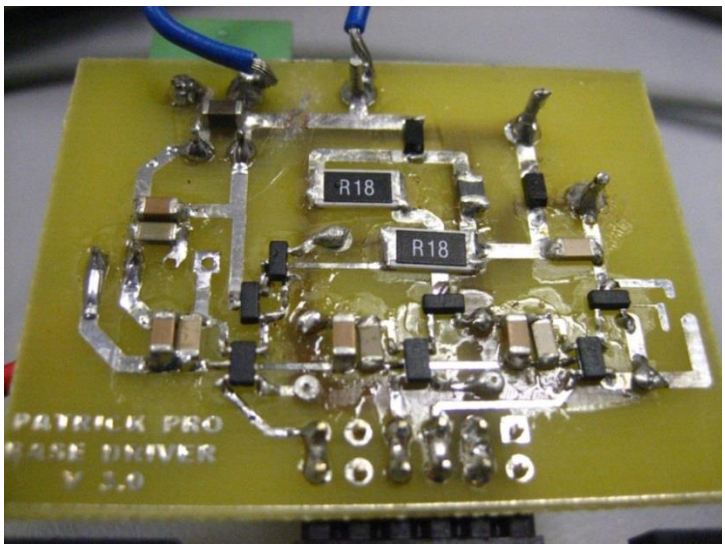


Figure 3-12 Energy recovery concept validation circuit

Discrete MOSFETs are used as switches (SW1-4, IRLML6246). The switches in the drive must be able to handle a continuous current of 1.6A which peaks at ~10A. In order to minimize the parasitic inductance and capacitance introduced by the tracks, the circuit has to be optimized. In order to keep the track lengths short, components are placed as close as possible and the surface mount type of the package is chosen to reduce the parasitic inductance. Relative parameters are shown in Equation 3-13 [90].

$$L_{Par} = 2l\left(Ln\left(\frac{2l}{w}\right) + 0.5 + \frac{0.2235w}{l}\right) \qquad \textbf{3-13}$$

Where the units of parasitic inductance, L_{Par}, is in nH, and w and l are the track width and length, measured in centimetres. In order to substantially reduce the total length of copper tracks, the converter circuit and base driver circuit are integrated into one PCB.

Figure 3-13 Measured base current waveform in the energy recovery circuit

The measured base current waveform and the energy recovery current are shown in Figure 3-13 and Figure 3-14, respectively. As shown in Figure 3-13, the positive and negative current peaks are 1.16A and -0.8A respectively, whereas the DC current for the conduction is 0.4A.

As shown in Figure 3-14, the peak recovery current is approximately 650mA for 100ns. The DC voltage (5V) has an oscillation associated by the recovery current. It has no effect for the base drive operation since DC voltage source is disconnected from the base terminal during the recovery stage.

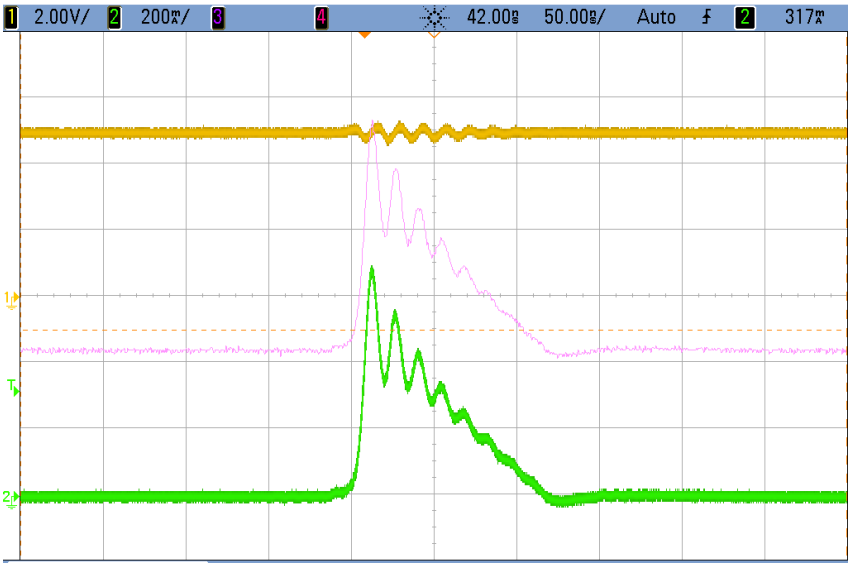


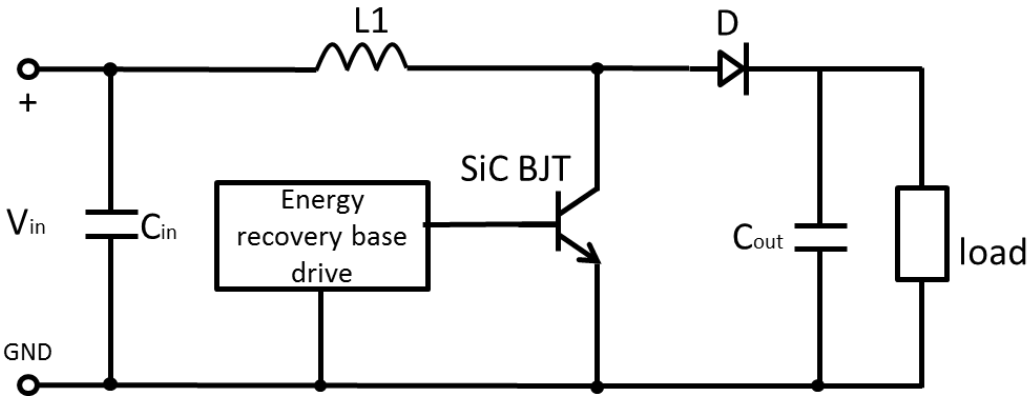
Figure 3-14 Energy recovery current measured for the validation circuit board. Channel 1 (Yellow) is DC input voltage which is 5V and Channel 2 (Green) is the recovery current back to DC source. The pink waveform is Channel1*Channel2

3.3 1.7kW boost converter prototype using SiC BJT and SiC Schottky diode with the energy recovery base drive

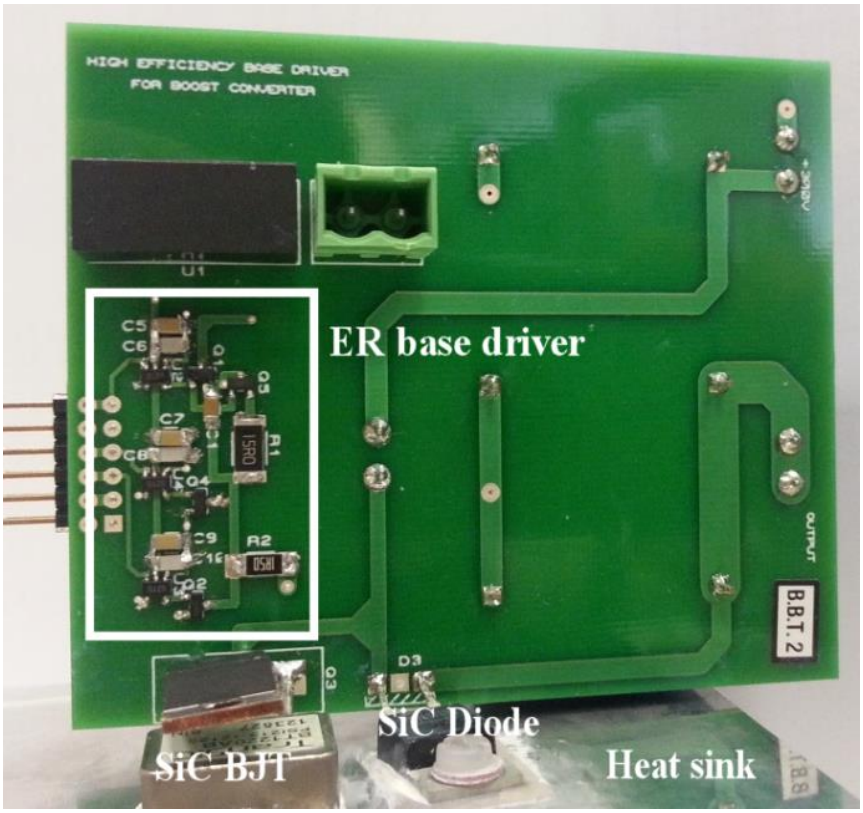
3.3.1 Boost converter using energy recovery base driver

A 1.7kW DC/DC boost converter is designed using SiC BJT driven by the proposed drive circuitry. A simplified circuit diagram of the considered converter is shown in Figure 3-15a. The converter takes an input voltage of 300V and boosts this up to 500V at a 40% duty cycle which is generated from a Nexys™2 Spartan-3E FPGA. Figure 3-15b and c show the top and bottom sides of the DC-DC converter, highlighting the energy recovery base driver, power devices, input and output capacitors and the PWM signal input. Since the energy recovery process occurs in the off-state period and does not influence the control strategy, the converter was running open-loop in the experiment with a fixed duty cycle to provide a constant power. The converter output was set to 500V in the experiment. The closed-loop

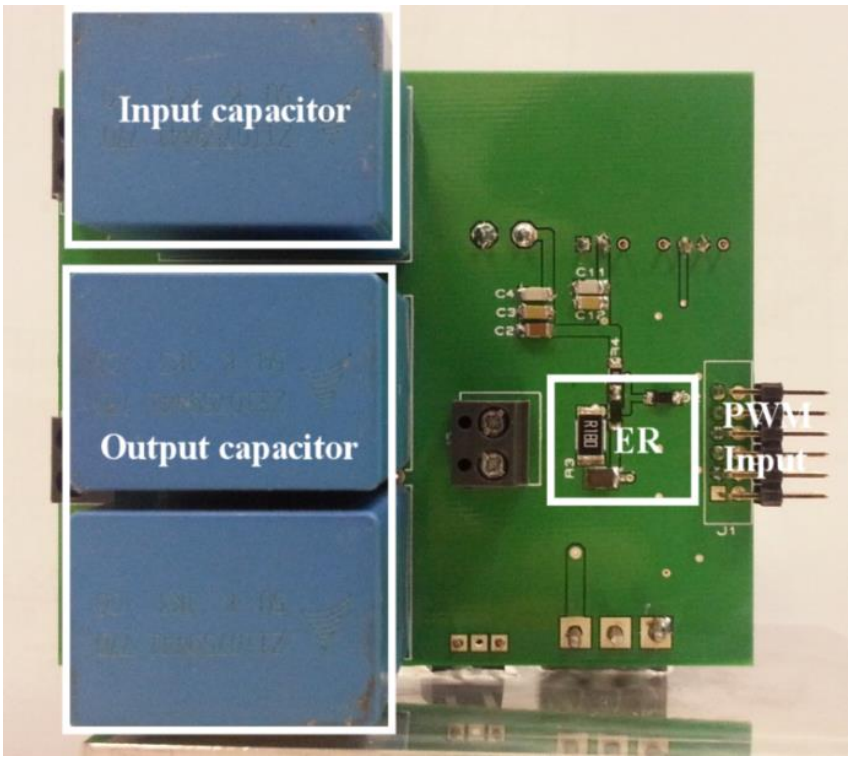
control implemented in the simulation studies proved that a traditional PWM control could be used, if required, to regulate the converter output. The power devices are attached to an air-cooled heat sink to maintain the junction temperature of the SiC BJT and the diode within their maximum rated values. The components of the base driver used in the experiment were in the same as those used in the preceding the simulation (section 3.2.2) with the models sourced from device manufactures, as shown in Table 3-2. The converter parameters are listed in Table 3-5. Since the SiC BJT is rated at 1200V, the input/output capacitors must be able to withstand a voltage higher than that, i.e. 1300V. In order to keep voltage stable and ripple minimum, the capacitance of the capacitors was selected to be as high as possible in series with the same package. L1 was manufactured in-house. To ensure the DCDC converter works in a continuous mode and reduce the peak current in the inductor, the inductance of the inductor was chosen to be 0.3mH. The highest switching frequency employed was 250kHz and hence the inductance cannot be very high as to keep the inductor size small. The equations and process of designing a conventional boost converter in the continuous mode can be easily found in the textbook and they are not specified in this thesis. The circuit schematic and PCB layout design are provided in Appendix 8-5 and Appendix 8-6.



(a) Schematic of a boost converter



(b) Topside



(c) Bottom side

Figure 3-15 Boost converter schematic and PCBA using the energy recovery driver

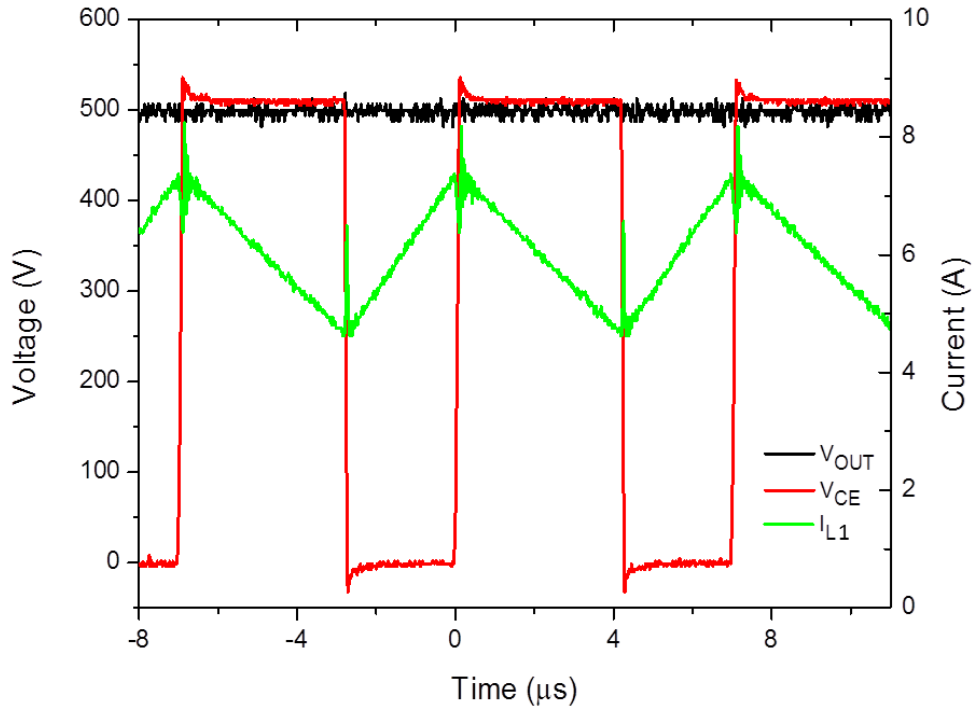
Table 3-5 Parameters of the converter

Output power rating	1.73kW
Input/Output voltage	300/500V
Load current	3.47A
Duty cycle	40%
Switching frequency	Max. 250kHz
Input capacitance	5μF/1300V
Output capacitance	2·5μF/1300V
Inductance	0.3mH/12A
SiC BJT [17]	1200V/20A
SiC schottky diode	1200V/10A
PWM generator	Spartan 3E FPGA
Heat sink	0.12°C/W
Fan for heat sink	130m^3/h
Fan for load	3·170m^3/h

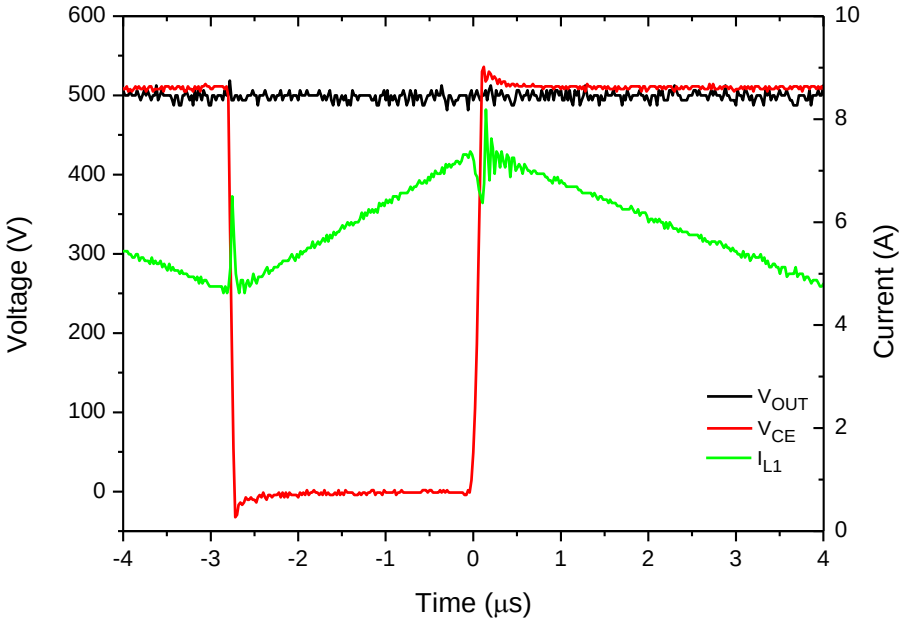
The tolerances of the pulse capacitor and recovery inductor used in these experiments were ±20% which needs to be considered while setting up the gate signal for SW2 in Figure 3-1a. According to Equation 3-6, θ is proportional to C_{pulse} and L. Deviations from the nominal values of L and C_{pulse} affect the result of Equation 3-6, leading to a new timing set up for SW2. As shown in Figure 3-1a, SW2 will turn on at the same point as SW4 and conduct for t_2-t_1, which is calculated in Equation 3-7. Unlike the capacitor, the inductance may show non-linear properties at fast transients and the core may saturate at large current. Inappropriate selection of the inductor can lead to a high switching power loss and low efficiency of the energy recovery function. A wire-wound chip power inductor was used with a Ni-Zn ferrite core rating at 2.4A. This provides the benefits of having a high self-resonant frequency and constant inductance value over a wide range of frequencies.

Figure 3-16 shows a typical switching cycle, which includes the collector voltage of the BJT (V_{CE}), power inductor current (I_{L1}) and the output DC voltage (V_{OUT}) operating at a switching frequency of 143kHz. As shown in Figure 3-16, the converter is boosting the input voltage up to 500V whereas the average inductor current is measured at 6.3A, below the saturation point. The excessive voltage across the BJT during turn-off is less than 30V which only

minimally stresses the device. The parasitic inductance between the collector of the BJT and cathode of the diode causes this voltage spike due to the high current slew rate. The consideration of the parasitic inductance reduction contributes to this low voltage peak. Due to the large output capacitor, the output voltage ripples are kept below 10V. The switching resonance in the inductor current can still be observed, as shown in Figure 3-16b. However, since the resonance is completely damped after ~250ns for turn-on and ~400ns for turn-off, this does not significantly affect the SiC BJT or causes any components of the converter to experience voltage break-down.



(a)



(b)

Figure 3-16 Typical switching waveforms of DCDC converter (different timescales)

Figure 3-17 shows the housing for the prototype boost converter used in the experimental testing. The power supply and resistive load are connected from the outside of the housing by cables whereas the converter circuit board, heat sink, control signal generator FPGA and power inductor are separated in case of any contact during the converter operation. A DC fan is attached at the rear of the heat sink in order to provide air flow inside of the housing and to draw heat outside. The high frequency inductor (0.3mH) was designed and manually wound (33 turns) with a design point of a 12A saturation current. Since the switching frequency can be up to 250kHz, the skin effect needs to be considered in the inductor design which increases the number of wires in each strand. The design process and specifications of the inductor are detailed in Appendix 8-7.

Figure 3-17 The boost converter in housing

3.3.2 Energy recovery base driver

Figure 3-18 shows the pulse capacitor (C_{pulse}) in Figure 3-1, voltage (V_c) and the power supply current (I_{DD}) in the energy recovery base drive. The base current, which is identical to I_{DD} during the turn-on period (4.0μs to 5.6μs), provides a peak current 2.7A; which is generated by C_{pulse} to increase the transient speed. Compared with the simulation results in Figure 3-5, the peak current is lower. In the simulation, all the values of the components are nominal values with no account of component tolerance. However in the experiment, component tolerance cannot be eliminated. Figure 3-6 has shown the simulated influence of the tolerance only caused by C_{pulse} and R2 on the base peak current.

The pulse capacitor (C_{pulse}) is charged to V_c when the turn-on process starts and discharged to zero when the energy recovery occurs from 5.6μs to 6.1μs, which agrees with the simulation results in Figure 3-5. A negative peak current 1.5A can be observed in the supply (I_{DD}) after V_c became zero, as predicted from the simulation results. The switching frequency for Figure 3-18 is 250kHz at an ambient temperature of 25°C.

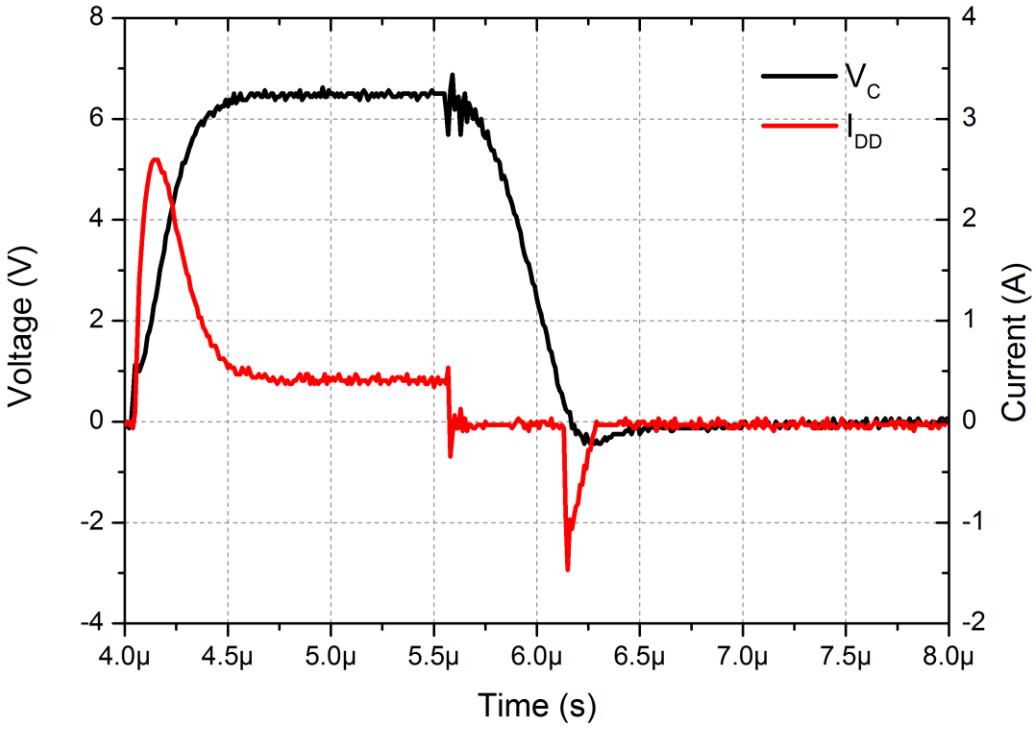


Figure 3-18 Measured energy recovery waveforms for the proposed energy recovery base drive circuit

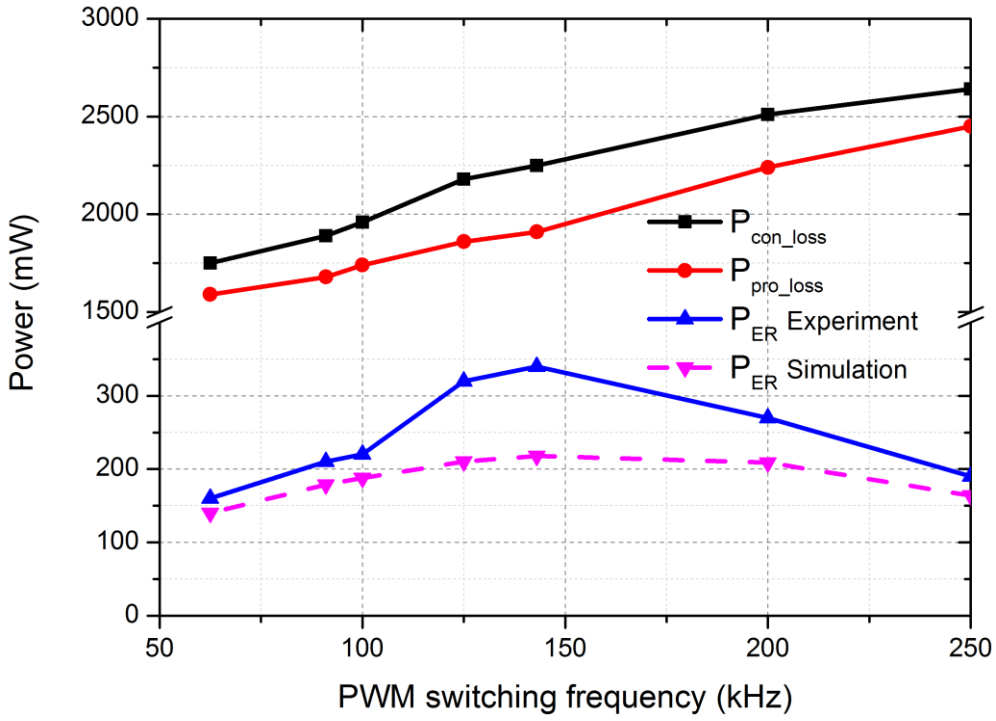


Figure 3-19 Power loss measurement in the experiment for the proposed and conventional base drives

Experimental results of the total power loss in the energy recovery base drive (P_{pro_loss}), a conventional base driver (P_{con_loss}) and the power saved (P_{ER}) with respect to switching frequency are shown in Figure 3-19. The conventional base driver circuit and the converter are shown in Figure 3-3b. The power saved (P_{ER}) decreases above 143kHz which has a similar trend observed as the simulation studies in Figure 3-7. The tolerances in values of L and C in hardware and simulation results in the gap between the two power recovery (P_{ER}) curves. The boost capacitor voltage (V_C) at the end of each cycle does not become zero, as shown in Figure 3-20 at high switching frequency 250kHz. So the power loss due to the pulse capacitor (C_{pulse}) decreases leading to a reduced base drive loss (P_{con_loss}). Based on Equation 3-12, the energy recovered (P_{ER}) decreases. However, the peak current is lower than that in the proposed base drive, which slows down the turn-on speed. Compared to the simulation results in Figure 3-8, the voltage waveforms match to each other and the base current peak is lower in the experiment due to the component tolerance as demonstrated in Figure 3-6.

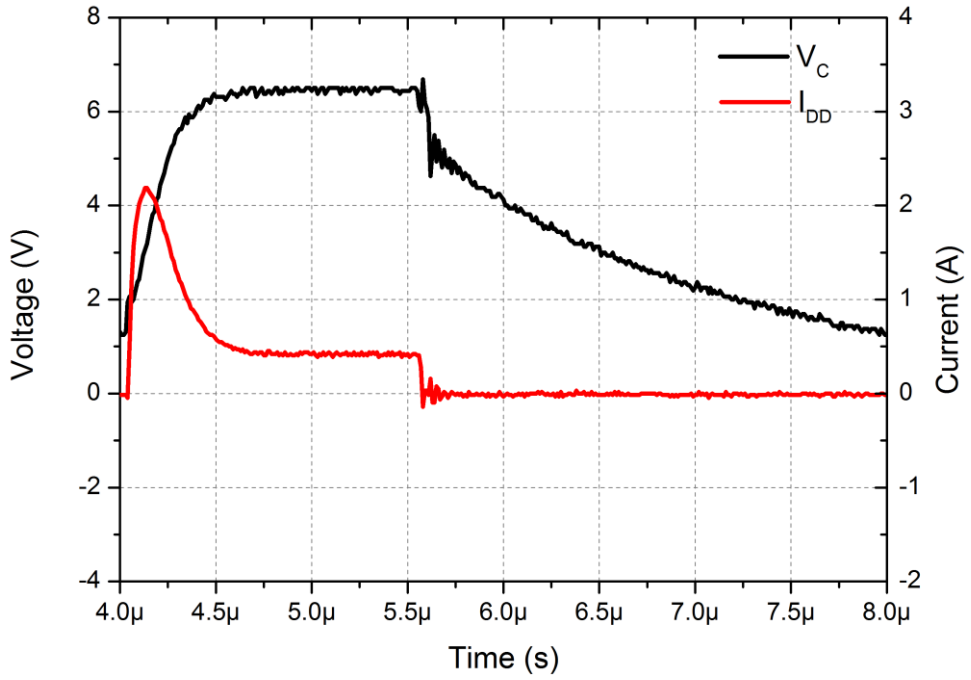


Figure 3-20 Power supply current I_{DD} and pulse capacitor voltage (V_C) of the conventional base drive when operated at 250kHz

3.3.3 Efficiency and power saving analysis

The base drive and the converter system losses are both measured with respect to boost converter switching frequency from 63kHz to 250kHz. The switching power losses of the SiC BJT increase proportionally which inevitably raises the converter power losses as shown in Figure 3-21. The converter losses shown are the difference between the measured input power and output power. Input power can be measured by the DC power supply. The output power is calculated by V^2/R_{Load}, where V is the output rms voltage of the converter and R_{Load} is the load resistance in Figure 3-15a. R_{Load} is measured during the experiment and cooled by fans below its derating temperature. The temperatures of the power devices, SiC BJT and SiC Schottky diode shown in Figure 3-15b, are kept in their safety region due to the air cooling design. The heatsink temperature is around 40°C during the experiment.

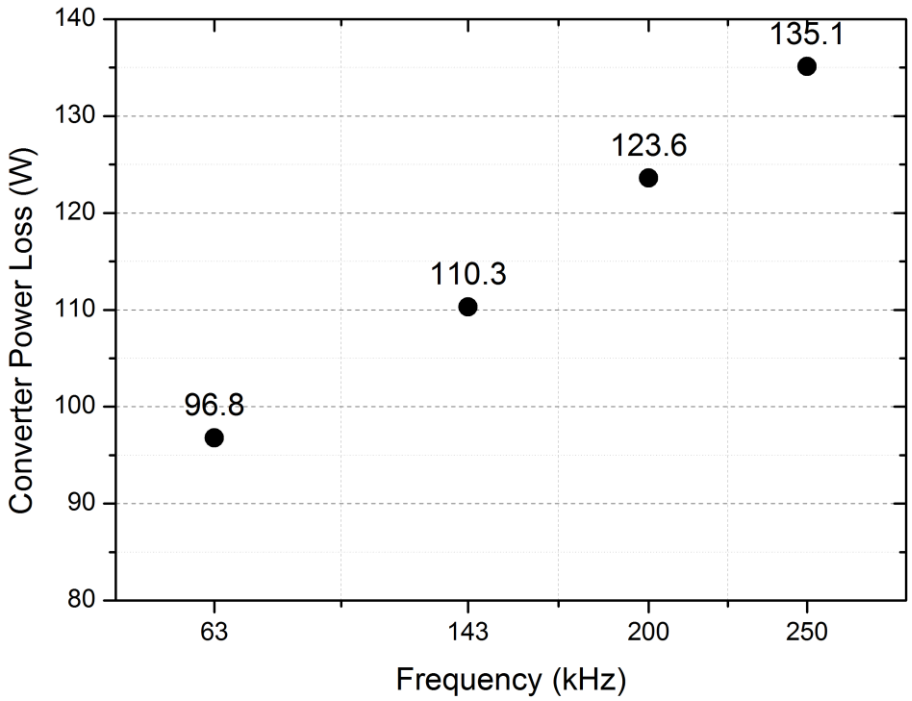


Figure 3-21 Measured converter power losses as a function of switching frequency

The converter efficiency is shown in Figure 3-22. The output power is fixed at a full-load of 1.7kW. The efficiency dropped to 92.8% as the inductor and switching loss increases proportionally with switching frequency. Moreover, the junction temperature of the SiC BJT does not affect the switching losses. However, the on-state losses of the SiC BJT increase at

higher junction temperature with implications for the converter efficiency. If the load current decreases, the base current required should be reduced at the same time to drive lower collector current of the BJT. The resistive loss of the driver decreases accordingly. However, the loss caused by the pulse capacitor (C_{pulse}) does not change. The power saving rate (η) is defined in Equation 3-14. P_{ER} equals ($P_{con_{loss}} - P_{pro_{loss}}$) as defined in Equation 3-12. The power recovered compared to the total conventional base driver, increases from 9.1% at 62.5kHz to 15.1% at 143kHz using the proposed base drive. Beyond 143kHz the power saving rate η begins to decrease due to the reasons mentioned previously in section 3.2.2.

$$\eta = {}^{P_{ER}}/_{P_{con\_loss}} \cdot 100\% \qquad \textbf{3-14}$$

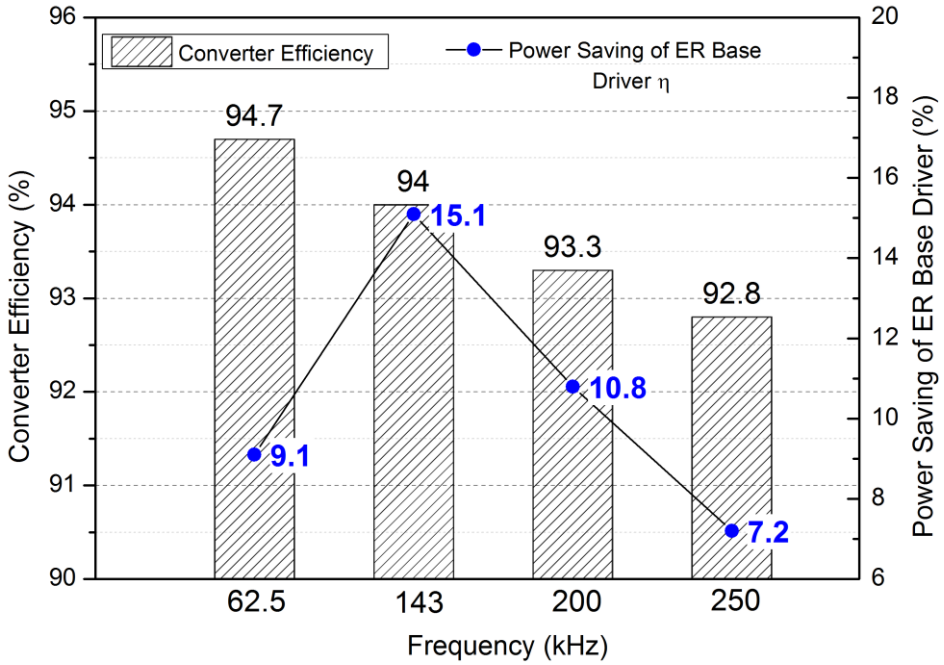


Figure 3-22 Converter efficiency and power saving of the base driver in the experiment using proposed energy recovery base driver

3.3.4 Discussion on a typical industrial application

For the converter with the energy recovery circuit aims for a mass production in the industry, advanced control technology, as shown in Figure 3-23, should be implemented. The output

voltage is rescaled by two series resistors down to a low voltage signal ($V_{feedback}$), which can be received by a µcontroller (microcontroller). According to the feedback voltage, the controller adjusts the duty cycle of the output PWM signal to regulate the output voltage at a required level. This primary function was implemented by a pure analogue circuit using comparators chips and accurate reference voltage in a traditional control design. However, in modern industry, a power system like DC/DC converter requires sophisticated functions and protections to achieve a robust design. In order to monitor and process multiple signals in a limited board size, a µcontroller is to be used, as shown in Figure 3-23. To protect the SiC BJT, the collector current must be kept below its maximum peak value by reducing the duty cycle of the base signal. The current is measured through a shunt resistor (R_{shunt}) and compared with the threshold stored in the µcontroller. When the SiC BJT is turned off, the energy recovery function in the base drive needs a time period (t_3-t_1 in Figure 3-1) to finish the recovery process. The voltage of D2 in Figure 3-1 is monitored by the µcontroller to ensure the process is complete and the SiC BJT is ready to be turned on at any time afterward.

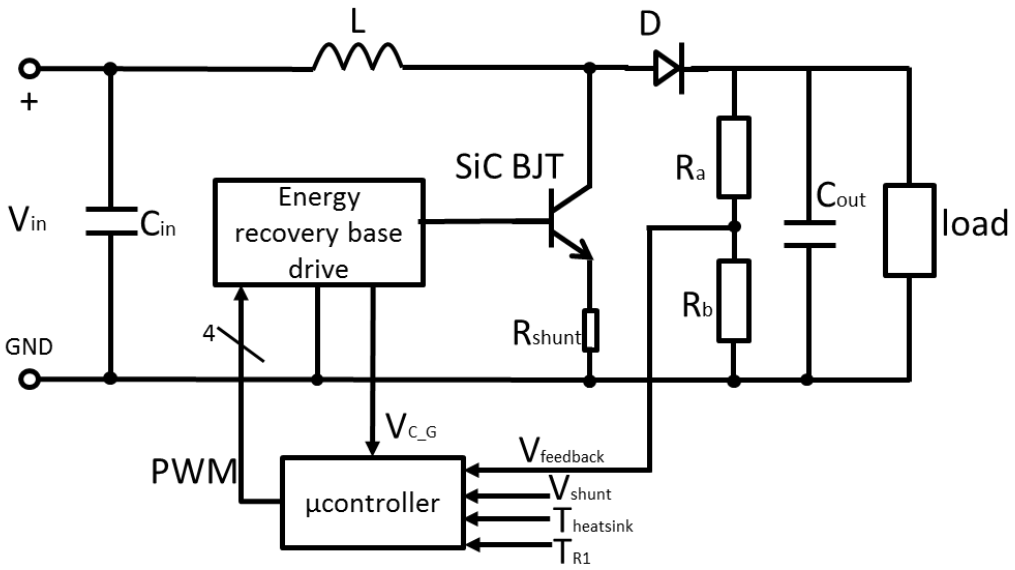


Figure 3-23 Top level system design for an industrial application

Except for monitoring the electrical parameters such as voltage and current, temperature information must be feedback by a temperature sensor such as a NTC thermistor to avoid any thermal damages. The junction temperature of the power device is not able to be measured directly. Instead, the heatsink temperature ($T_{heatsink}$) is sampled to estimate the junction temperature for the protection purpose. The temperature of the base resistor R_1 in Figure 3-1

is monitored to ensure that the resistor is working in its thermal safety region and a real-time resistance can be looked up in the µcontroller according to its package temperature. The control mechanism in Figure 3-23 can prevent from over-stressing the power device, which are found to result in device failure or degradation [91-93], by shutting down the system when an overvoltage or overcurrent is detected.

3.4 Summary

This chapter demonstrates the implementation of an energy recovery circuit to a SiC BJT base drive unit to reducing the drive losses, especially for higher switching frequency applications. The simulation is carried out to verify the energy recovery concept and provides estimation on components' power losses. The energy recovery concept has also been implemented in the gate driver design for a MOSFET as analysed in Chapter 1. It is used to save the energy in the gate capacitor.

A 1.7kW boost converter has been built using the proposed base driver to control a SiC BJT. The switching frequency of the boost converter was varied from 63kHz to 250kHz, with the switching loss of the BJT and the pulse capacitor loss in the driver both increasing proportionally with the frequency. The maximum drive power saving achieved experimentally with the energy recovery driver is 15.1% at 143kHz switching frequency. Beyond 143kHz, the power saving then starts to decrease due to the pulse capacitor power loss reduction in the conventional drive unit. This pulse capacitor power loss reduction consequently influences the turn-on performance. Electrical measurements of the proposed energy recovery circuit show 7.2% energy has been recovered in the total power loss of the base drive at 250kHz with a converter efficiency of 93%. Since the energy recovery process will take a period of time to transfer energy, the minimum off time is required dependent on the L-C values in the design. This inevitably limits the maximum frequency and duty cycle of the converter application.

Compared with the gate drive design for the voltage-driven device MOSFETs, the size of the base drive for a SiC BJT is larger due to the heat dissipation requirement for large driver losses. The DC fan needs to be attached to the drive board if the resistive loss and base current are too high for dissipation by natural convection or conduction to the enclosure. Chapter 4 will demonstrate a base driver design to reduce the power loss on the resistor, especially for a low switching frequency and higher duty cycle applications. The base drive

design will additionally keep switching losses of the SiC BJT as low as the conventional driving technology.

4 An Active Base Driver Design for SiC BJT

4.1 Introduction

In terms of the base driver efficiency, the losses associated with maintaining the device in its on-state condition dominates the overall drive performance. In order to reduce the DC power loss of the base driver, the voltage supply level (V_{DD}) should be set as low as possible, as shown previously in Figure 1-24. However, if V_{DD} is too low, the device is more susceptible to voltage fluctuation during transients caused by current transient which are coupled from emitter stray inductance. The base current reduces due to this base terminal fluctuation and the turn-on delay time increases. Furthermore reducing this supply voltage (V_{DD}) would increase switching losses as a portion of the fast switching base current is sourced from the DC supply. If a high V_{DD} is chosen, R_1 in Figure 1-24 needs to be high proportionally. This results in large resistive power losses and driver losses as yielded in Equation 1-20 and 1-21. Therefore a trade-off exists between base drive losses and BJT switching performance for a conventional base driver structure. Hence, there is considerable motivation to reduce V_{DD} and R_1 in order to reduce driver losses while keep the switching losses of the BJT low.

This chapter presents an active base driver design, consisting of the integration of a buck converter into the circuit. This circuit is able to provide a base drive, which is proportional to the collector current. A separate circuit delivers a peak current to the device during transients. This proposed base drive configuration effectively de-couples the transient and steady state requirements whilst not showing any detrimental effects on device performance.

4.2 Function of the active base driver

Figure 4-1 shows a typical timing diagram for a typical operational period of the active base drive unit while the equivalent circuit is shown in Figure 4-2a. Compared to the conventional drive, the proposed circuit integrates a low power buck converter, composing of a switch (SW3), diodes (D1 & D2), inductor (L1) and a capacitor (C1). The proposed base driver is able to provide various base current by adjusting the output voltage of this buck converter. During the turn-on period, the voltage of C1 is reduced from V_{DD} to V_{C1}, which causes the voltage across R_1 to reduce. Therefore, the resistance of R_1 should decrease to supply the same amount of the base current I_{DC}. The power losses on R_1 reduce although the base current does not change.

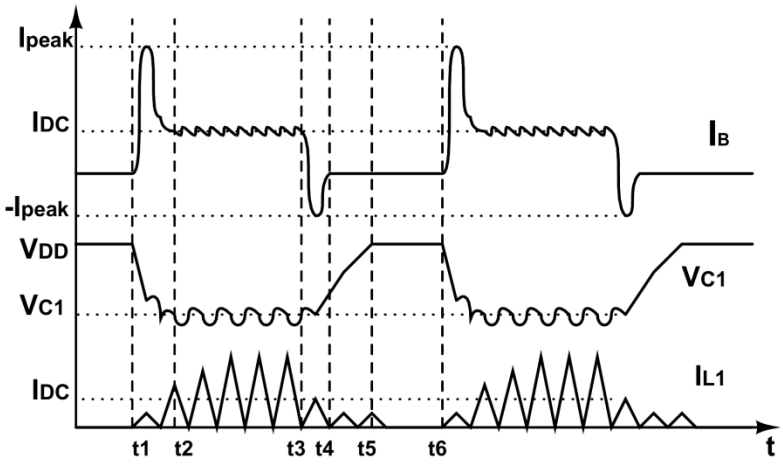


Figure 4-1 Representative critical operating waveforms

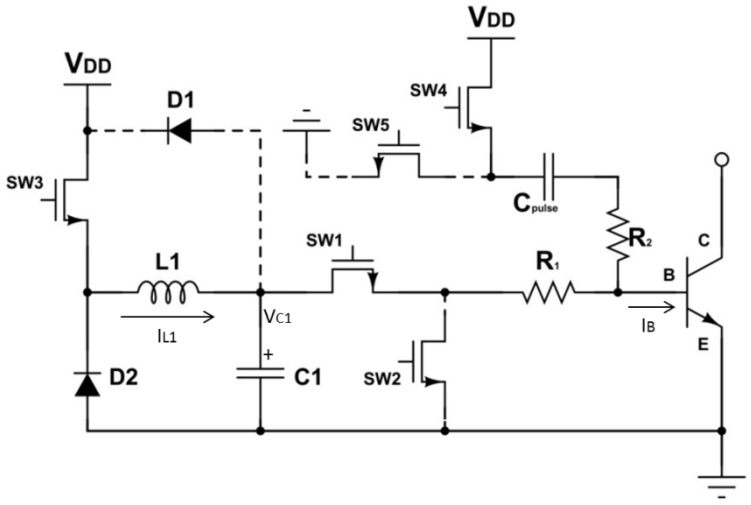


Figure 4-2a: Transient turn-on equivalent circuit during t_1-t_2

Operation during t_1-t_2 :

Prior to activation the BJT is in the off state and the base is connected to ground by SW2, as shown in Figure 4-1. At t_1 SW1 and SW4 are turned on and SW2 is turned off, this provides a peak current to achieve faster switching times of the BJT. At this point the drive is similar to a conventional base driver.

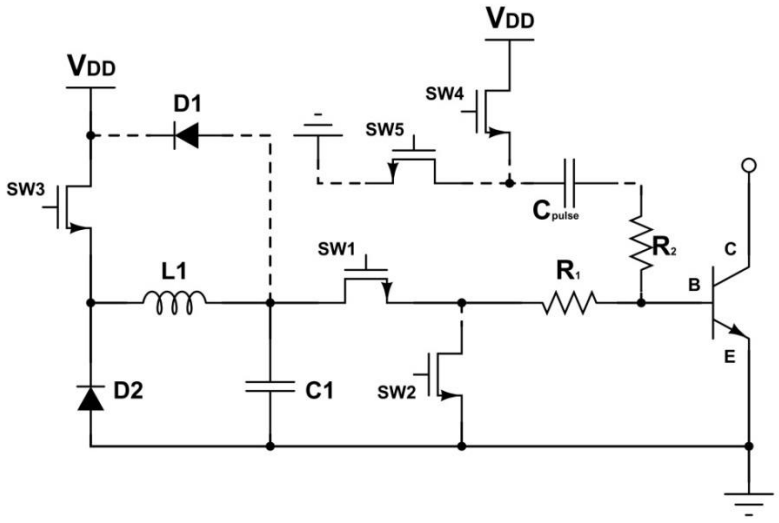


Figure 4-2b: On-state equivalent circuit during t_2-t_3

Operation during t_2-t_3 :

After the turn-on transient, a continuous DC base current (I_{DC}), which is the DC component of I_B in Figure 4-1, is provided to maintain the on-state of the BJT. This current is determined by the ratio of capacitor voltage (V_{C1}) and base resistance (R_1), which equals the average value of inductor current (I_{L1}) during t_2-t_3 in Figure 4-1. By modulating the duty cycle of SW3, the capacitor voltage (V_{C1}), estimated by Equation 4-1, can be lower than power supply voltage (V_{DD}). Consequently the base resistance (R_1) should be reduced in order to set a base current identical to that directly sourced from high supply voltage. Compared to the conventional base drive, the power loss in the resistor (P_{R_1}) reduces with its value as shown by Equation 4-2, where D_{SW1} is the duty cycle of switch SW1. Diode (D1) is used to free wheel the current; protecting the circuit in case the inductor current changes abruptly.

$$V_{C1} = \frac{V_{DD}}{\frac{2L_1 I_{DC}}{D_{SW3}^2 V_{DD} T_{SW3}} + 1} \quad \textbf{4-1}$$

Where the duty cycle of SW3 is D_{SW3} with switching period T_{SW3}

$$P_{R_1} = I_{DC}^2 R_1 D_{SW1} \quad \textbf{4-2}$$

In the active base drive the capacitor voltage (V_{C1}) can change with duty cycle and switching frequency of SW3 as shown by Equation 4-1. Unlike the conventional driver circuit, which is controlled by a fixed supply voltage (V_{DD}), the proposed drive can adapted by controlling SW3. Therefore, the base current can be tailored depending upon the collector current demand or junction temperature of the BJT: avoiding the over driven conditions which demands a 1.5 times increase in drive current to prevent operating the device in the active region.

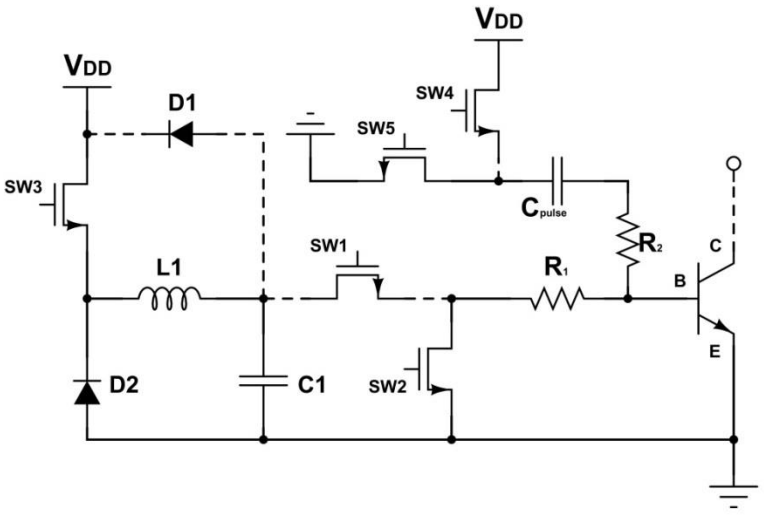


Figure 4-2c: Transient turn-off equivalent circuit during t_3-t_4

Operation during t_3-t_4 :

After the BJT has been conducting for a time period t_2-t_3, the drive prepares to switch it off. To turn off the BJT, as described in Figure 4-2c, the gate voltage is removed from SW1 and SW4 while the gate signal is supplied to SW2 and SW5. C_{pulse}-R_2 branch generates a negative current peak ($-I_{peak}$) to reduce the turn-off power losses during t_3-t_4.

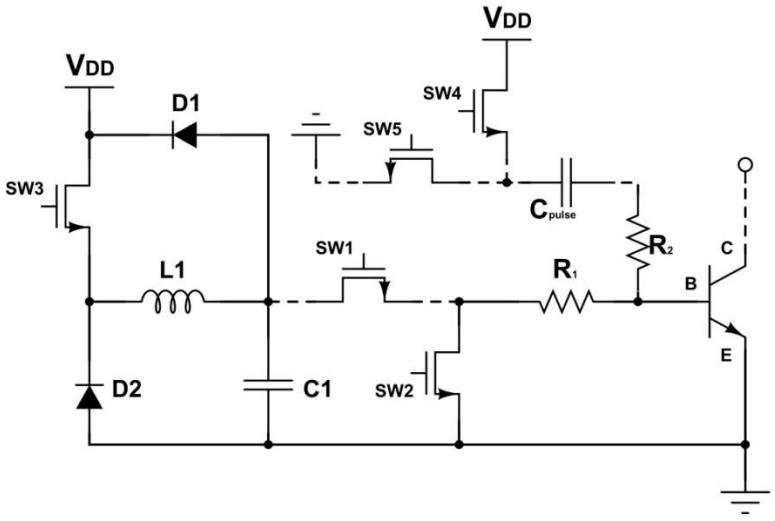


Figure 4-2d: Off state equivalent circuit during t_4-t_6

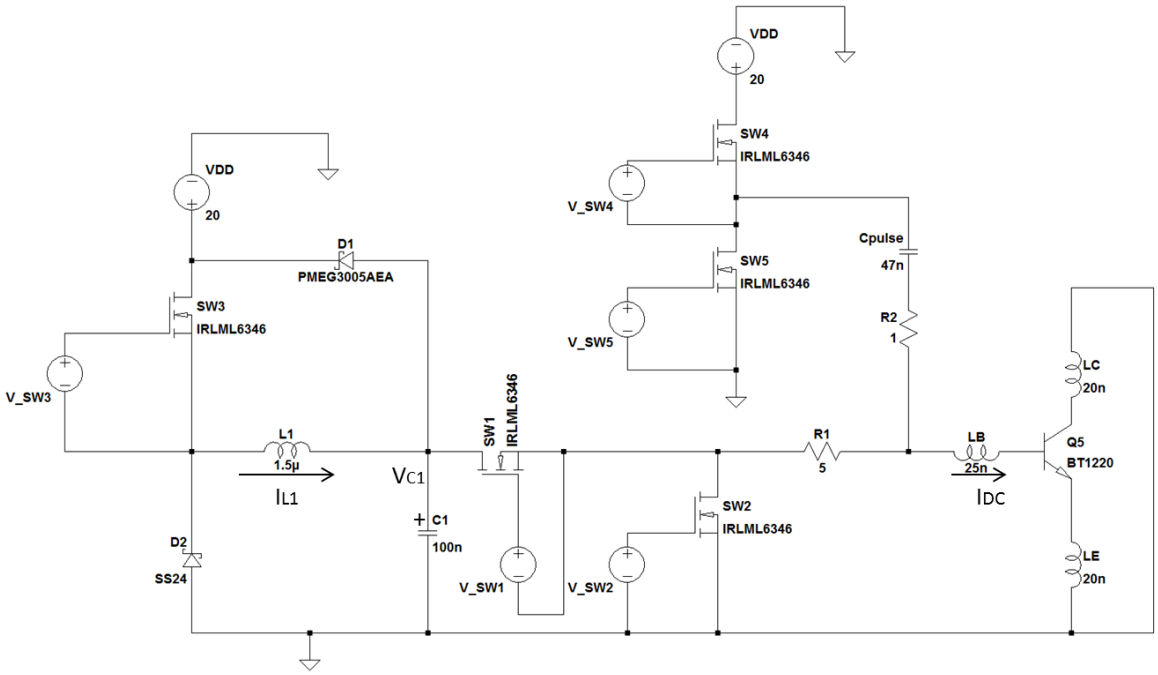
Operation during t_4-t_6 :

Following the turn-off transient, the BJT goes into its blocking mode. SW1 disconnects the DC power from the base terminal and SW2 is turned on: grounding the base terminal via R_1 as shown in Figure 4-2d, the BJT is operated in its shorted base off state condition. The capacitor voltage (V_{C1}) rises during the time period t_4-t_5 due to energy transferred from the inductor. Without power dissipation in the base resistor, the buck converter output voltage V_{C1} will increase to V_{DD} at t_5 and keep constant until the end of the period at t_6. The driver can work at 100% duty cycle and the switching frequency for the SiC BJT is not limited by the driver.

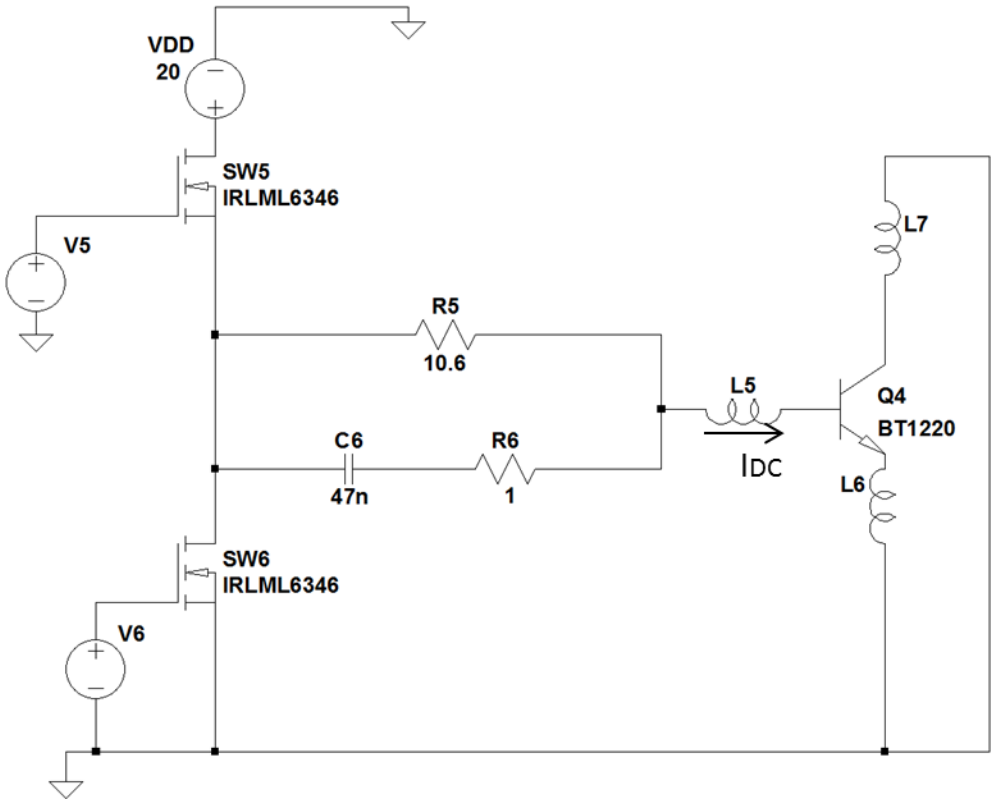
4.3 Active base driver implementation in the simulation

A simulation schematic of the proposed driver is shown in Figure 4-3a with components used. A switching frequency of 67kHz was used for SW1, SW2, SW4 and SW5 whereas this was increased to 1.1MHz for SW3 in order to minimize the base current ripple and he capacitance of C1. All the switches (SW1-5) are the same MOSFET, i.e. IRLML6346. The total gate charge is 6.8nC for the MOSFET used in the simulation and the gate voltage is 12V. Therefore each gate capacitance loss is 5mW at switching frequency 67kHz. Compared with the total driver losses, it is negligibly small. Three low power MOSFET switches are additional for the active base driver. In order to compare the base drive losses between the

active base drive and the conventional design which is shown in Figure 4-3b, both drive units are simulated to supply the identical DC base current (I_{DC}) of 1.6A from a 20V power supply (V_{DD}). C6 and R6 are identical to C_{pulse} and R2 to generate the same transient peak current for fast switching. According to Equation 3-10, the turn-on time can be shorter than 45ns. In order to provide 1.6A I_{DC}, R5 is set to 10.6Ω as shown in Figure 4-3 for the conventional base driver. For the active base driver, we are aiming for 11V V_{C1}. When the switching frequency of SW3 (T_{SW3}) is 1.1MHz and L1 is 1.5μH, the duty cycle is 49% calculated by Equation 4-1 for 1.6A I_{DC}. The peak current rating of the diode D2 should be higher than two times of I_{DC} and the voltage rating should be higher than 20V. Since V_{C1} is lower than V_{DD}, R1 in Figure 4-1a is only 5Ω, which is twice smaller than R5 in Figure 4-1b. The result of Equation 4-2 becomes smaller. Under 100% duty cycle, the power loss of R1 is 12.8W. Therefore, the resistor will be in a larger package in order to dissipate heat effectively.



(a) The active base driver

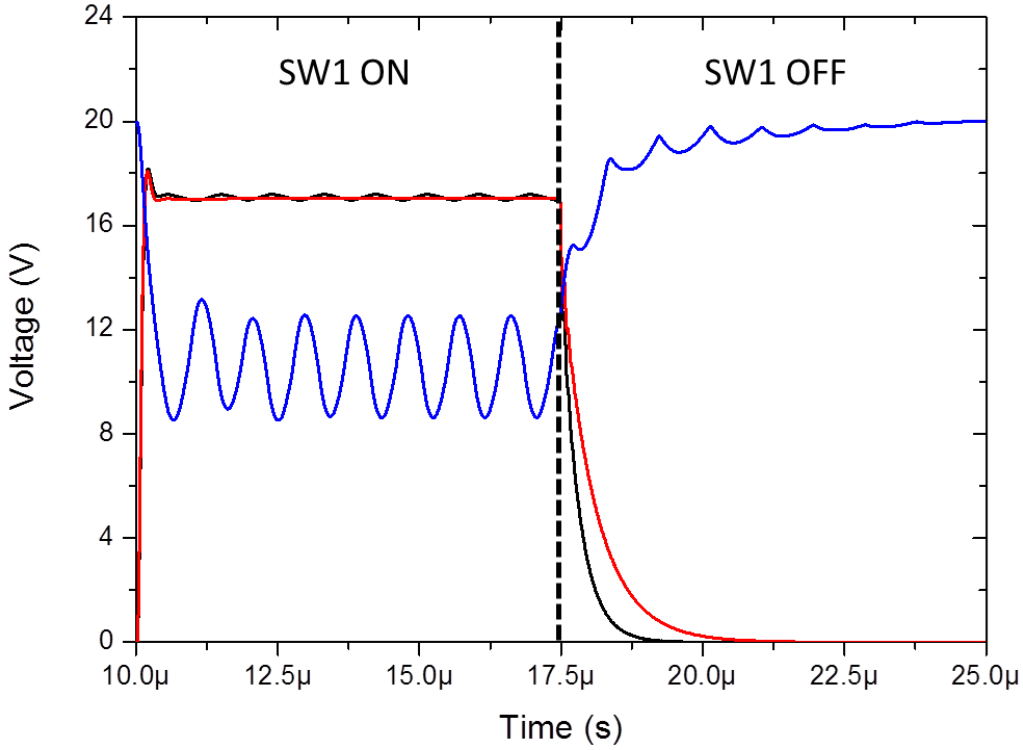


(b) The conventional base driver

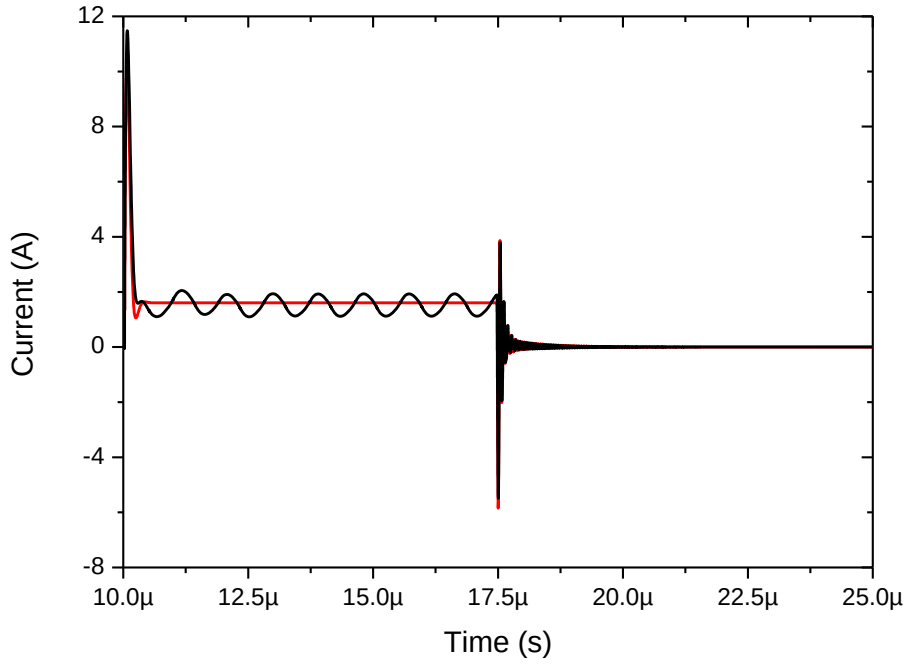
Figure 4-3 Simulation circuit models for the varous base drivers

Figure 4-4a compares the drive output for the conventional and active base drive circuit. The blue curve shows the output of the buck converter output (V_{C1}) is approximately 11V. As shown, the voltage across the pulse capacitor (C_{pulse}) falls to zero 1.2µs faster in the proposed design compared with the conventional drive due to the smaller R1. This ensures that the maximum duty cycle and switching frequency can be increased for this drive. The buck converter output voltage (V_{C1}) can reach to V_{DD} during the BJT off-state period.

The DC base current (I_{DC}) is set to 1.6A with ripples in the active base driver to conduct 20A collector current, which is the black curve in Figure 4-4b. The current ripple is caused by the switching of SW3 to charge and discharge the energy in the inductor to the base terminal of the BJT. The peak current during the switching transient, as shown in Figure 4-4b, are identical for both drivers. The simulated total power losses for the proposed drive and conventional drive are 10W and 17W respectively showing that the proposed drive scheme reduces power losses by 41%.



(a) Blue (capacitor voltage V_{C1} in Figure 4-3), black (pulse capacitor voltage in the active base driver), red (pulse capacitor voltage in the conventional base driver)



(b) Black (DC base current I_{DC} in the active base driver), red (DC base current I_{DC} in the conventional base driver)

Figure 4-4 Simulated waveforms from the base drive for the active and conventional design

The initial peak current supplies the base-collector and base-emitter charges when the device is turned on, which is dependent upon R_1, C_{pulse} and V_{DD} [66]. Therefore, the drive can optimise the switching performance by defining V_{DD} when R_2 and C_{pulse} are constant. However, the value of V_{DD} affects drive and device performance as a large value results in large drive losses whereas if this value is too low, it causes large switching delay time and high switching losses.

Due to the lack of industrial applications for SiC BJTs, there is no universal accepted V_{DD} value. The base drive loss has been compared in simulation between conventional and active drive units over a wide range of supply voltages (V_{DD}), as shown in Figure 4-5. Here, V_{DD} is varied between 7-30V at a 49% duty cycle applied to SW3, Figure 4-3. A base drive current (I_{DC}) of 1.6A is selected for both drives. As shown in Figure 4-5, the conventional base drive consumes greater power when compared to the active drive, regardless of the selected supply voltage (V_{DD}). Due to the non-linear relationship between V_{DD} and V_{C1}, Equation 4-1, the active base driver shows a non-linear trend. In order to achieve low switching power losses, V_{DD} is chosen to be 20V.

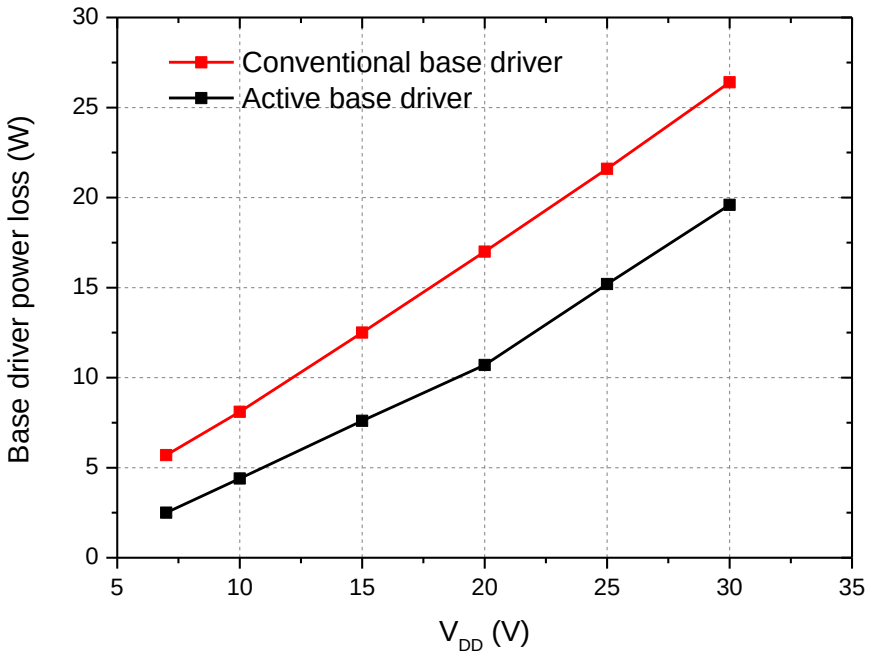


Figure 4-5 Base driver power loss comparisons subject to different driving voltage (V_{DD})

4.4 A control method for providing proportional base current

Based on the function analysis in previous section, the active base drive is capable of adjusting its output current to the base. A control method is proposed in this section, which can ensure driver to provide a proportional base current to the collector current while maintaining a minimum collector-emitter saturation voltage. Figure 4-6 shows the original active base drive circuit with the control loop for the simulation. The collector current of the SiC BJT is dependent on the load resistance, which is composed of a resistor bank between high DC voltage source (V_{dc}) and the SiC BJT (Q5). The resistors (R4-R7) are connected into the circuit one after another in an order to generate various collector current for the test. R3 is used as a current sensor to translate a current value to a voltage parameter (V_{Ic}), as shown in Figure 4-6. Under different collector currents, the current gain changes non-linearly as shown in the datasheet[17] and in Figure 4-7 and Appendix 8-8. Therefore, the base current must be adjusted with the collector current to avoid both over drive and insufficient drive. The base current in the active base driver is controlled by changing the voltage of C1 by varying the duty cycle of SW3, as given by Equation 4-1. A voltage source B1 is modelled to use the collector current as one of the variables and then it is compared with a triangle wave voltage (Vtri) by an amplifier (U2). By doing this, the positive input of U2 is relative to V_{Ic}, which equals to I_c sensed by a 1Ω resistor. When I_c increases, V_{Ic} becomes larger at the same time. Then the duty cycle of SW3 increases to supply a higher base current I_b to track the change of I_c. The output of U2 is used as a control signal (a PWM signal) for SW3, as shown in Figure 4-6. The coefficients in B1 function, such as 0.4 and -0.2 are manually determined and optimized in order to track current gain under various collector currents. By fitting the base current values in the simulation to the current gain vs. collector current characteristics in the datasheet, these two factors are proved to be capable of controlling the base current and maintaining low conduction losses of the BJT. This feature will be explored in the following section.

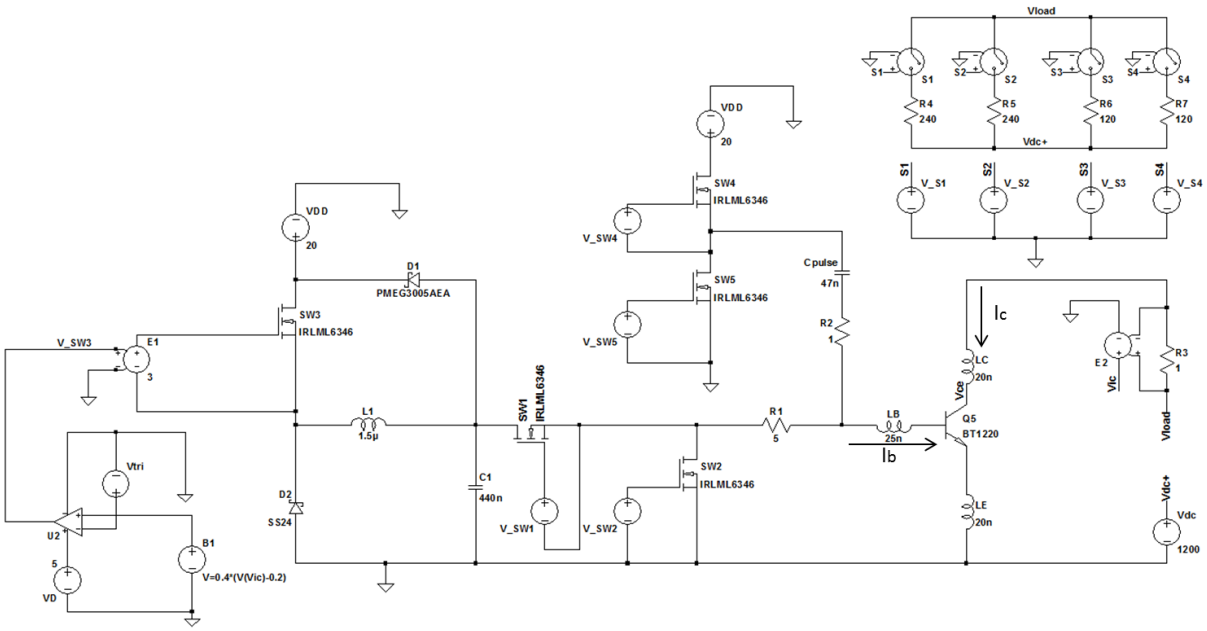


Figure 4-6 Control loop design for the proportional base current

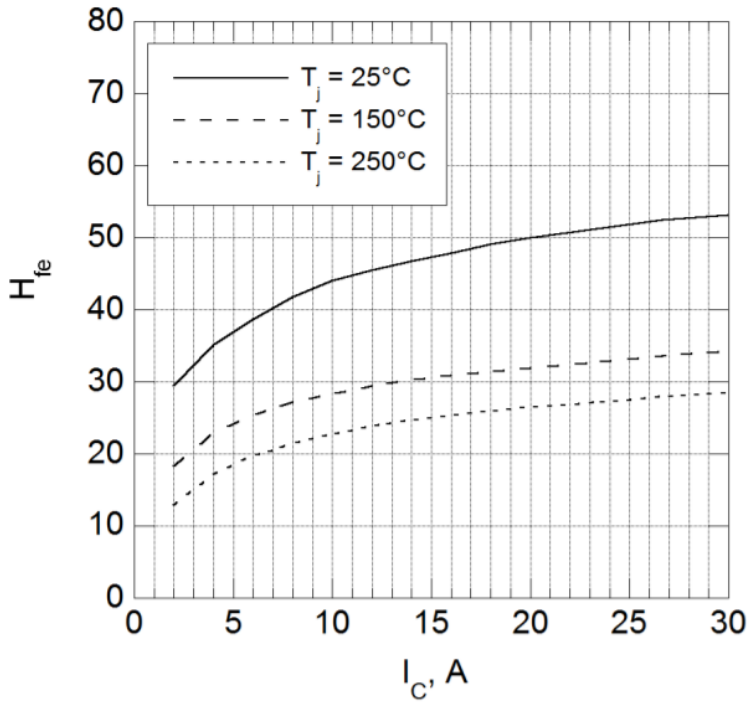


Figure 4-7 Current gain (H_{fe}) vs. collector current

During the simulation at 25°C, load resistor R4 is connected into the circuit at a time of 0ms. In this case, the collector current is approximate 5A with 1200V DC power supply (V_{dc}) if the

BJT is conducting with adequate base current. Afterwards, R5, R6 and R7 are connected into the circuit in sequence at time point 35µs, 90µs and 135µs in the simulation. As a result, the collector currents (I_c(Q5)) increase from approximate 5A to 30A after 135µs, as shown in Figure 4-8. The base current (I_b(Q5)) increases proportionally according to the collector current. The collector-emitter voltage (V_{ce}) is zoomed in to measure low saturation voltage.

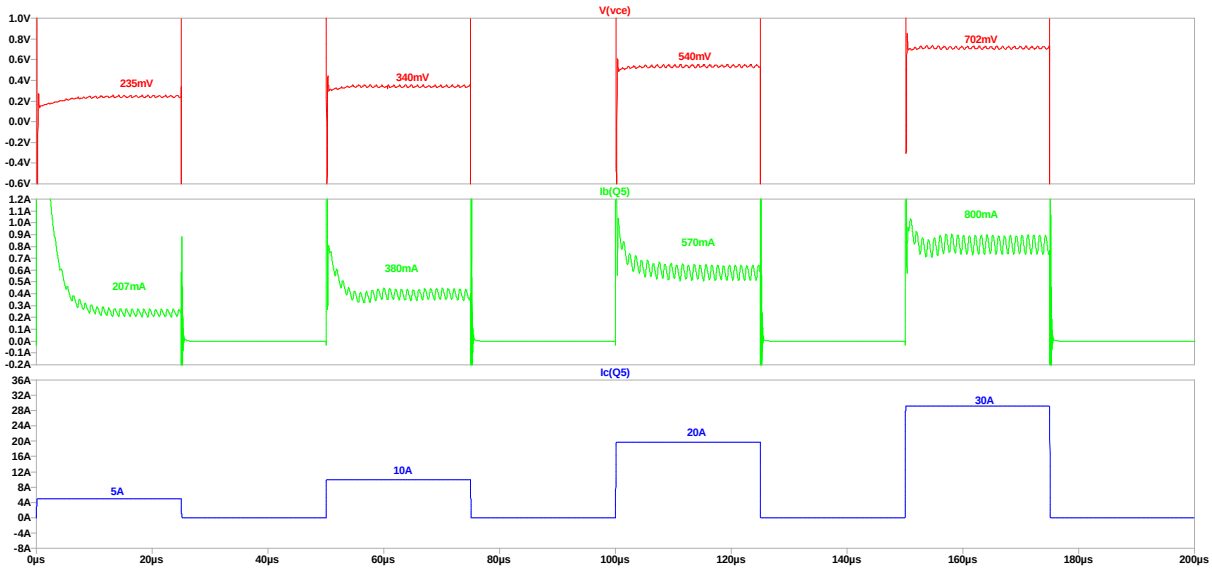


Figure 4-8 Simulation results with the proportional base current

The base current required in the conventional drive (I_{b_con}) is given by Equation 1-19 at 25°C, with I_C equalling 30A and at the worst current gain β of 50 [17], as the results shown in Table 4-1. The corresponding saturation voltage (V_{ce_con}) is looked up from the datasheet [17] with 0.9A base current. The proportional base current (I_{b_active}) and saturation voltage (V_{ce_active}) are measured from the simulation results in Figure 4-8. The comparison implies that the active base drive can provide adequate proportional base current while maintaining low saturation voltage using proposed control method.

Table 4-1 Base currents and saturation voltages comparison at 25°C

I_C (A)	I_{b_con} (A)	V_{ce_con} (V)	I_{b_active} (A)	V_{ce_active} (V)
5	0.9	0.16	0.21	0.24
10	0.9	0.25	0.38	0.34
20	0.9	0.50	0.57	0.54
30	0.9	0.72	0.80	0.70

4.5 Experimental verification for the active base driver

4.5.1 Circuit design for the active base driver

A prototype used to verify the proposed active base driver is shown in . The circuit schematic and PCB layout can be found in Appendix 8-9 and Appendix 8-10, respectively. This circuit is fabricated to drive a 1200V/20A SiC BJT, BT1220AB-P1 [17]. The base resistor R_1 has been selected to supply a continuous base current of 1.6A, which is sufficient to maintain the device in its saturation mode of operation at a collector current of 20A and a junction temperature of 250°C. Galvanic isolation between the control and drive board is realised with an optical connection. Commercial integrated DC-DC converters provide the voltage levels required by the optical receivers and the gate voltages for the MOSFETs.

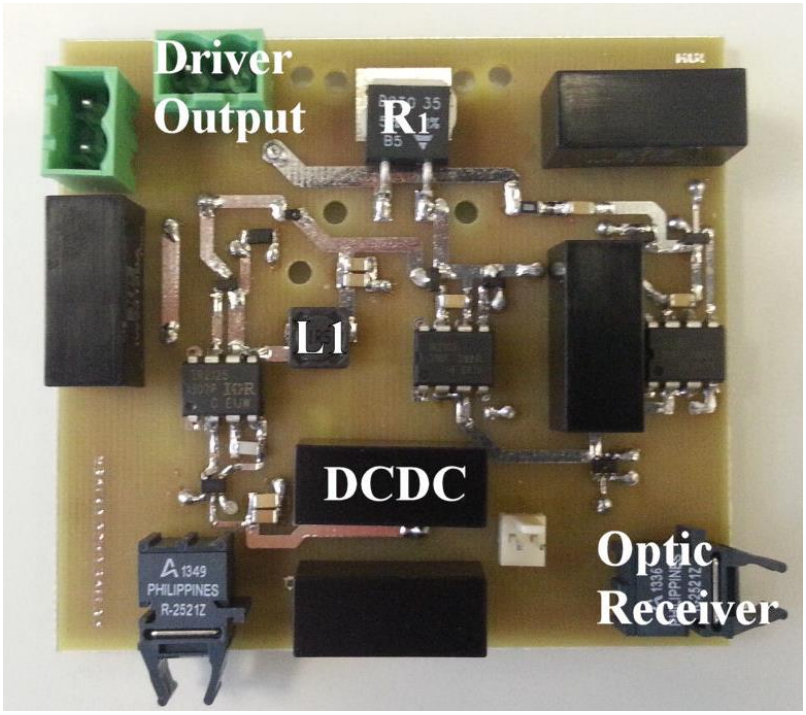


Figure 4-9 Prototype board for the active base driver

Key components which have been selected in the previous section, including voltage and current ratings, are shown in Table 4-2. A DC power supply of 20V is used for both conventional and proposed base driver in order to achieve fast switching in an inductive double-pulse switching test.

Table 4-2 Components in the active base driver

Component	Property	Manufacture
Power Resistor (R_1)	5Ω, 35W	VISHAY SFERNICE
Resistor (R_2)	1 Ω	YAGEO
Capacitor (C_{pulse})	47nF	AVX
Capacitor (C1)	100nF	AVX
Inductor (L1) series resistance	15mΩ	MULTICOMP
Inductor (L1)	1.5μH	MULTICOMP
DCDC Converter	20V to 12V	XP POWER
DCDC Converter	20V to 5V	XP POWER
Optical Receiver	Optical to electrical signal	Versatile link
Switch (SW1,2,3,4,5)	30V/2.7A	International Rectifier
Switch on resistance	45mΩ	International Rectifier
Diode (D1)	60V/200mA	NXP
Diode (D2)	60V/2A	NXP

In the conventional drive design, the base current is fixed, therefore even at low junction temperatures when the device gain is high, the base current will be 1.6A. Unlike the conventional base drive unit, the proposed driver can vary its base current (I_{DC}) in the experiment, by changing the duty cycle of SW3 as shown in Figure 4-10. Figure 4-10 varies the duty cycle of SW3 from 24% to 46% whereas measured base currents are shown in Figure 4-11. As shown, for this change in duty cycle the base current ranges from 0.8A to 1.6A and the amplitude of the current peak is unaffected.

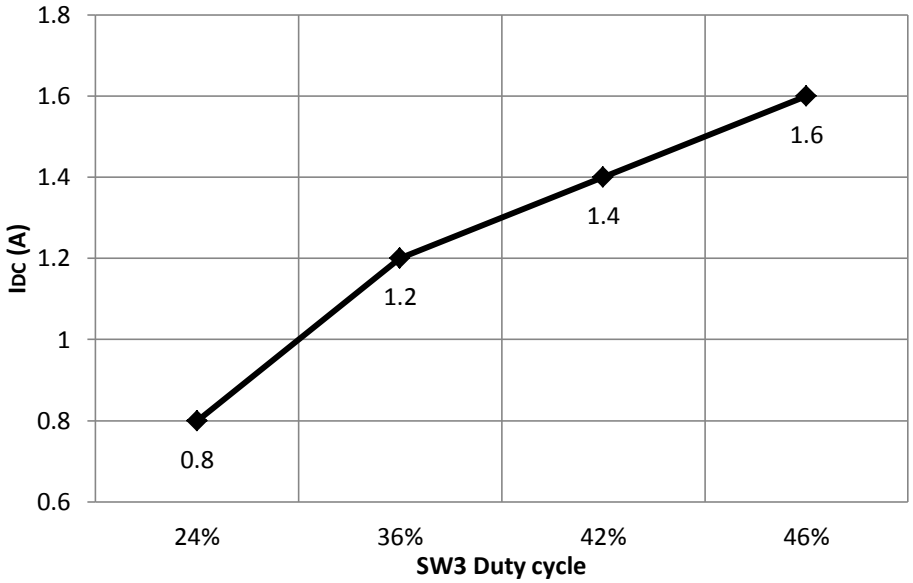


Figure 4-10 SW3 duty cycle and I_{DC}

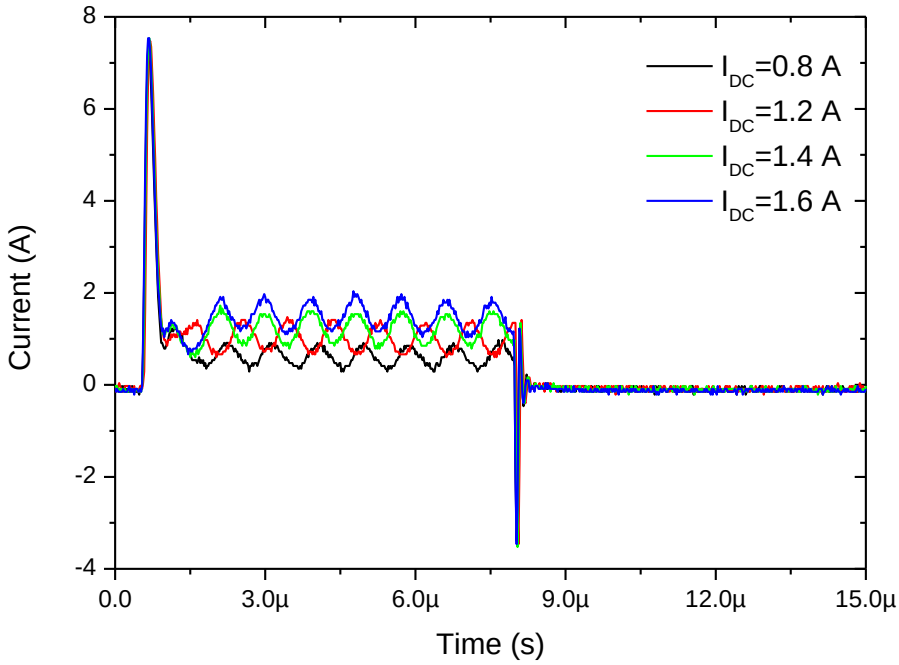


Figure 4-11 Measured base current values with various duty cycles for SW3

4.5.2 Power loss comparison between the proposed and conventional base driver

Based on Equation 4-2, the active base driver losses depend on the base current I_{DC} and R_1 assuming that the switching frequency of SW1 and input voltage V_{DD} are fixed. Figure 4-12 compares the measured and simulated total power losses of the active base driver and a

conventional drive at a switching frequency of 67kHz and 50% duty cycle of SW1. The base currents can vary from 0.8 to 1.6A while only 1.6A can be supplied by the conventional base driver. The simulation conditions are shown in Figure 4-3 for the open collector configuration. The differences between the simulation and measured results are due to two reasons. The first one is that in the simulation the gate drivers (V_SW1 to V_SW5) in Figure 4-3a are ideal and the total base driver losses do not take these powers into account. In the experiment, those powers are all supplied by V_{DD} and included in the total power consumptions. The second one is caused by the tolerances of the components. It also influences the base peak current amplitude as demonstrated in Chapter 3. The power losses for the active base drive are reduced by 32% at a base current of 1.6A when compared to a conventional drive in the experiment. In circumstances where the SiC BJT is operating at a junction temperature of 25°C, a drive current (I_{DC}) of 0.8A is sufficient to keep the BJT conduction losses low, according to Equation 1-19. When 0.8A is provided by the proposed base drive, the power losses reduce by 69% compared to the conventional drive, as shown in Figure 4-12.

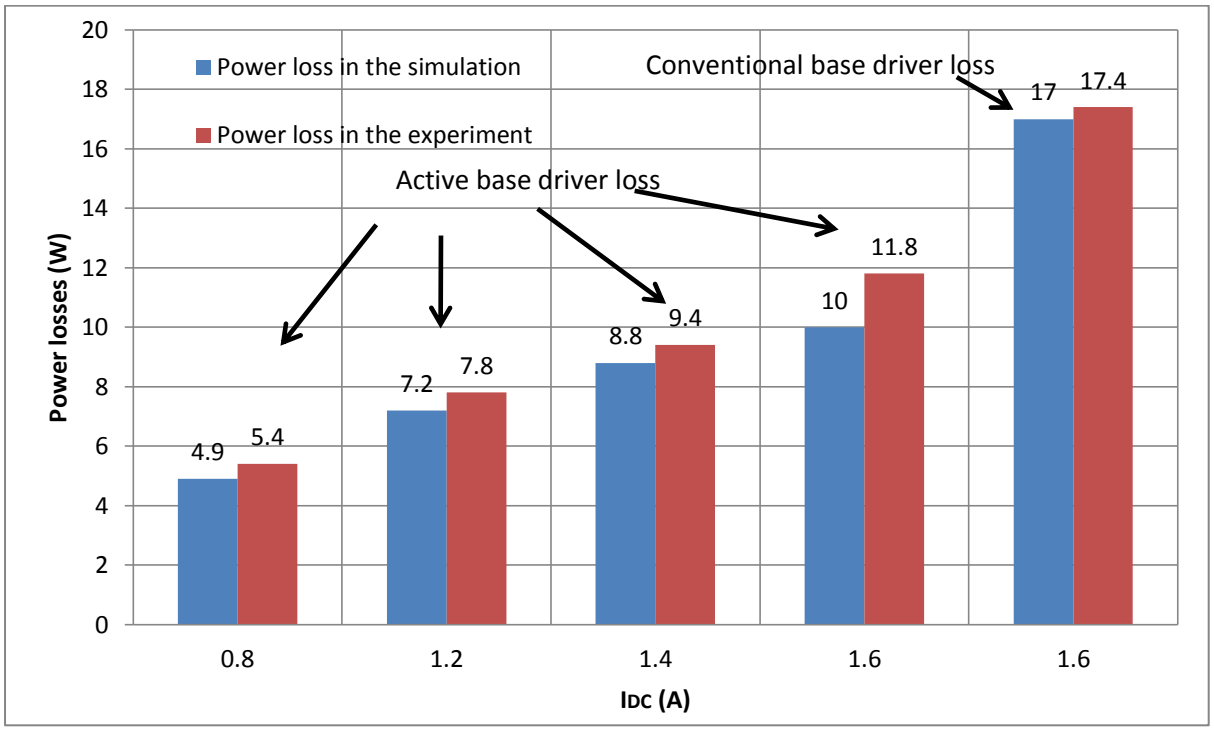
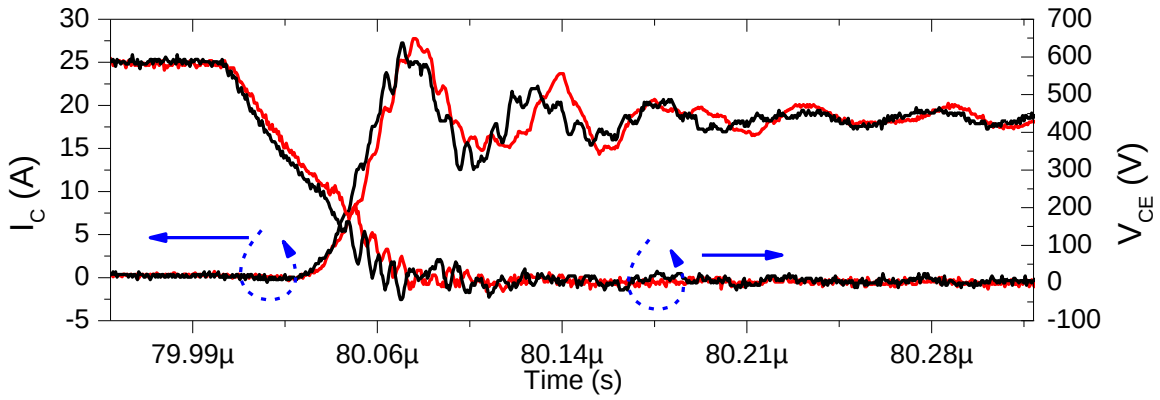


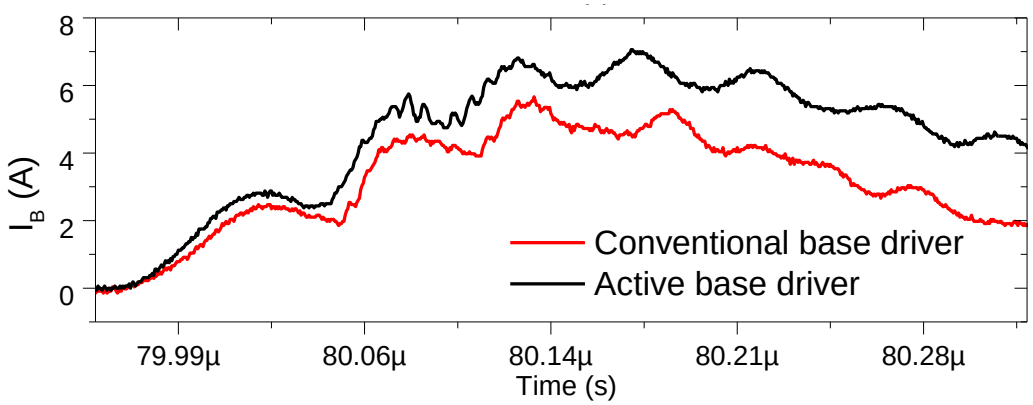
Figure 4-12 Base driver power loss comparison with 50% duty cycle of SW1 at switching frequency 67kHz

4.5.3 Switching performance using the active base driver

To investigate the impact of the proposed drive upon the BJT transient losses, both driver configurations, as shown in Figure 1-24 and Figure 4-2, were used in a double pulse switching test. The test process is the same as described in section 1.6.1 of Chapter 1 in order to obtain the switching energy losses for the BJT. Under these tests the ambient temperature of the DUT is set to be 25°C. All the tests are under the same conditions to benchmark the proposed base driver against the conventional approach.



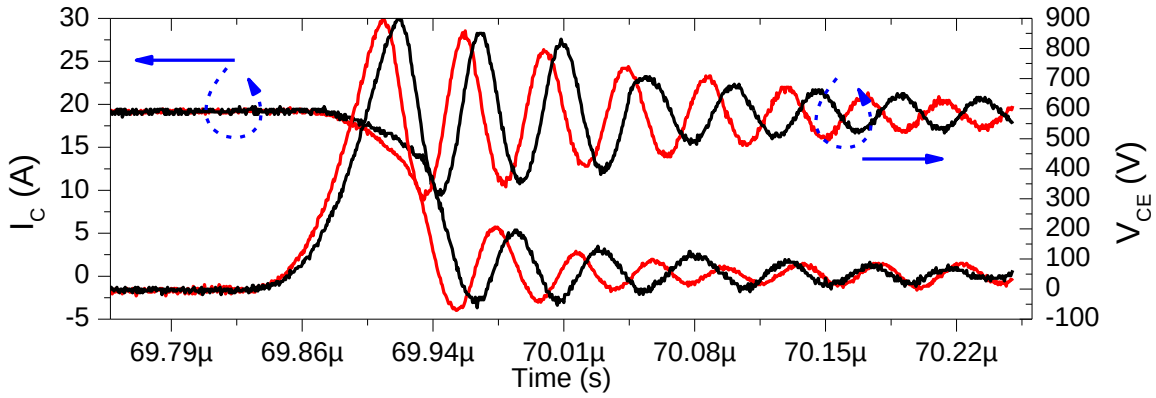
(a) Turn-on performances using the active base driver (black line) and using the conventional base driver (red line)



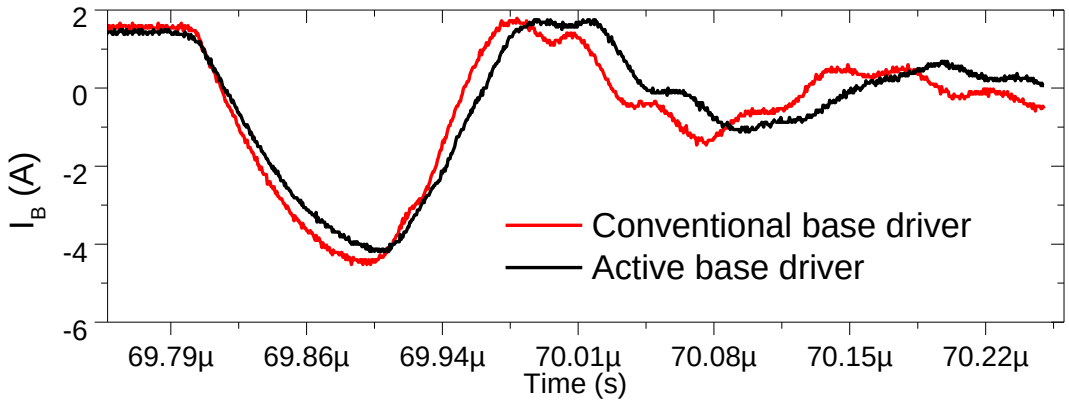
(b) Positive base current peak during turn-on

Figure 4-13 Turn-on performance and base current waveforms with I_{DC}=1.6A

Figure 4-13 compares the turn-on speed of both drives when delivering 1.6A into the base of the SiC BJT. As shown, the proposed driver is slightly faster than the conventional driver due to the slightly higher drive current which is caused by a smaller R1. The higher the base current, the quicker the SiC BJT turns on. As the case in the simulation in Figure 4-3, R1 was set to 5Ω and R5 to 10.6Ω for the conventional driver to supply the same base current. V_{C1} equals to V_{DD} at the turn-on point since there is no load for the buck converter during the off state. This gives a turn-on loss of 19μJ for the proposed active base driver compared to 38μJ of the conventional driver.



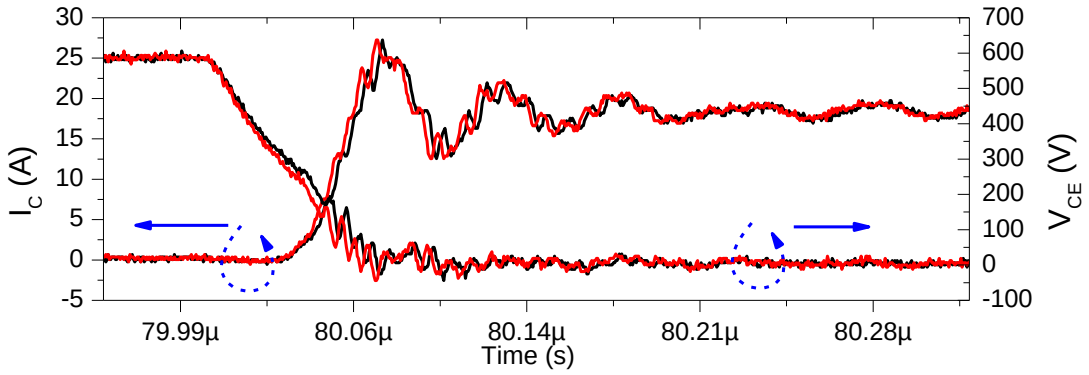
(a) Turn-off performances using the active base driver (black line) and using the conventional base driver (red line)



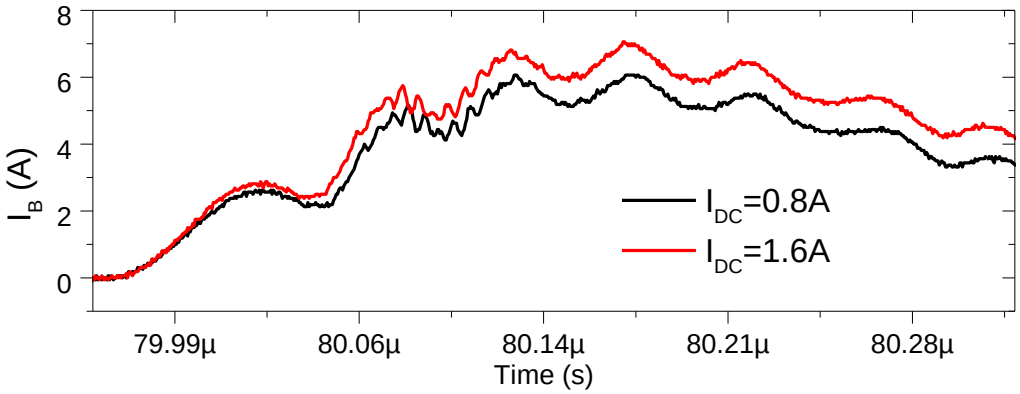
(b) Negative base current peak during turn-off

Figure 4-14 Turn-off waveforms and base current waveforms with I_{DC}=1.6A

Figure 4-14 compares the turn-off performance of the BJT driven by both base drivers. The proposed active base driver has slightly lower and delayed negative peak current flowing through the base due to the switching period of SW1 to disconnect power from R_1. As addressed in Chapter 1, the delayed base signal can result in an increase of the switching losses. Therefore, in this case it has increased the turn-off loss to 617µJ from to 556µJ of the conventional driver. The total switching energy losses are 636µJ using the active base drive compared to 594µJ for the conventional driver.

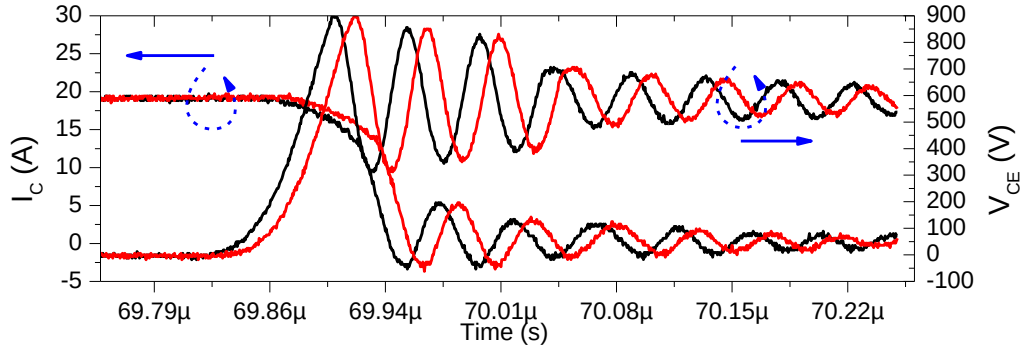


(a) Turn-on performances with base current I_{DC}=0.8A (black line) and base current I_{DC}=1.6A (red line)

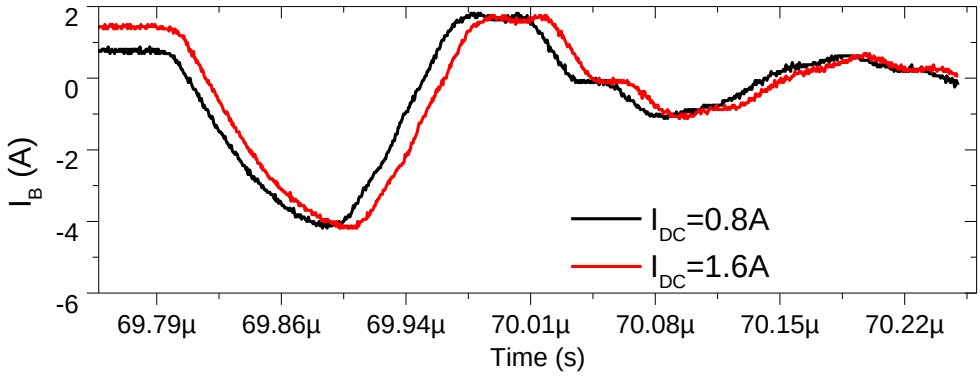


(b) Positive base current during turn-on in the active base driver

Figure 4-15 Turn-on performance using the active base driver and base current waveforms with two different levels of I_{DC}



(a) Turn-off performances with base current I_{DC}=0.8A (black line) and base current I_{DC}=1.6A (red line)



(b) Negative base current during turn-on in the active base driver

Figure 4-16 Turn-off performances using the active base driver and base current waveforms with two different I_{DC}

Figure 4-15 and Figure 4-16 compare the turn-on and off switching performance of the SiC BJT using the active base drive configured to provide 1.6A and 0.8A into the base during the on-state. There is little deviation of the switching performance proving that lower base current is able to switch the SiC BJT efficiently at low junction temperature. Since the transient and DC current paths have been de-coupled in the active drive, a fast switching speed can be achieved. Therefore, the trade-off between a low drive voltage (V_{DD}) and high switching losses have been de-coupled.

4.5.4 On-state performance

The base current also influences the on-state power losses as well as the switching performance. SiC BJTs have the lowest on-state resistance in the SiC power device family [3] from 25°C to 175°C junction temperature if an adequate base current is supplied, which is dependent upon the current gain of the BJT and collector current.

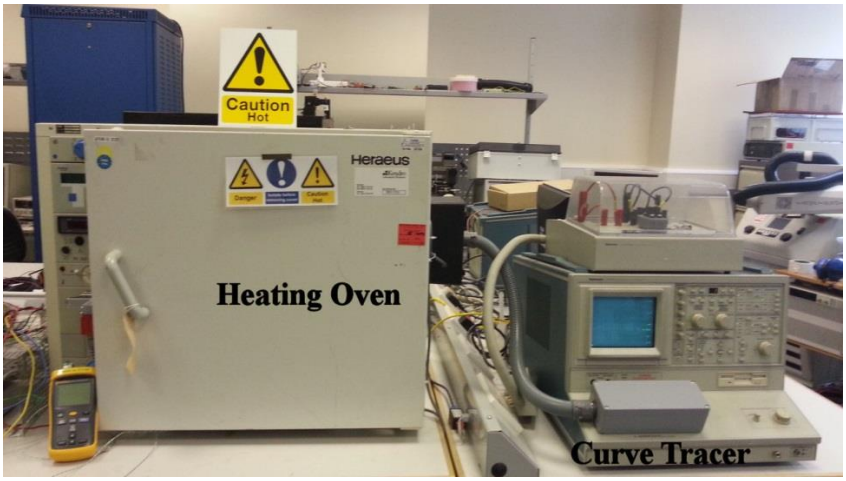


Figure 4-17 On-state performance experiment set-up

In order to measure the static characteristics at elevated temperatures with respect to base current, the SiC BJT is located within an oven with its three terminals connected to an external curve tracer (Tecktronix 371A), as shown in Figure 4-17. During the experiment, the oven can heat its internal temperature up to 200°C. The device is left in the oven which temperature is regulated at a certain level for 15 minutes to ensure the junction temperature stable prior to DC characterisation.

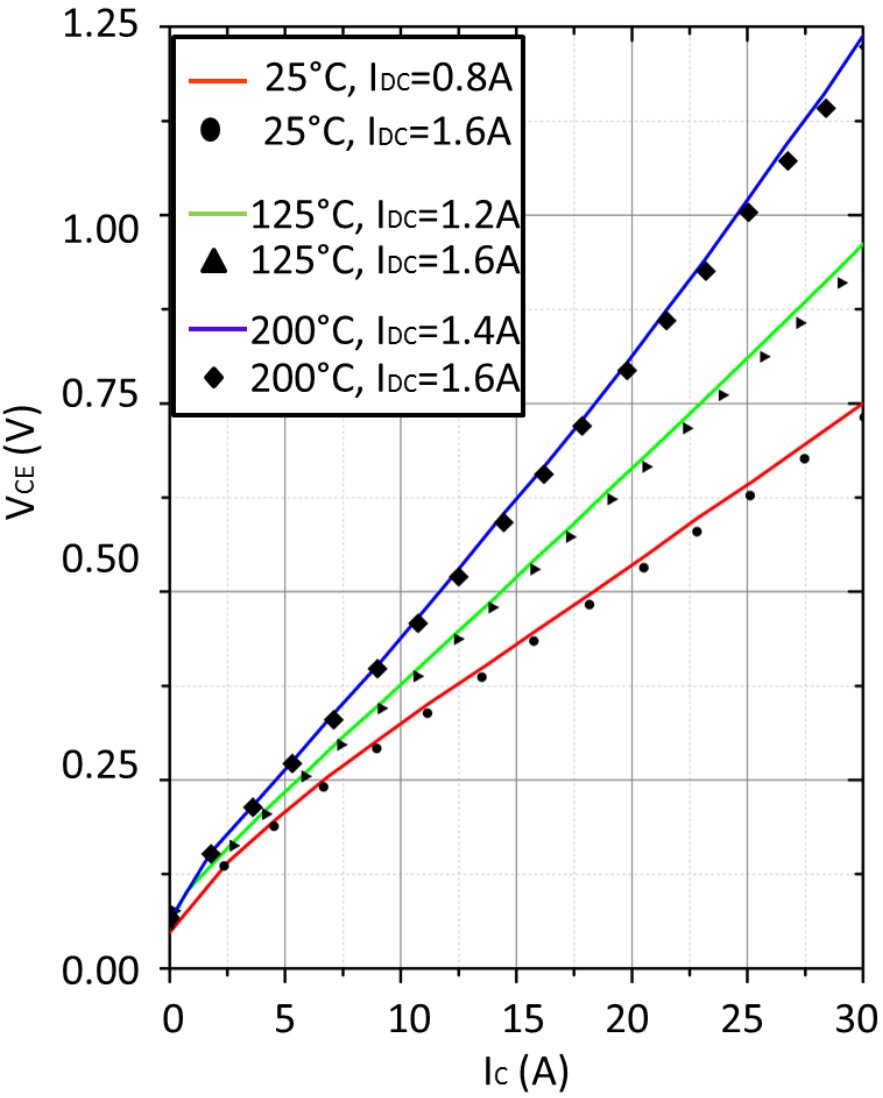


Figure 4-18 On-state performances with different junction temperatures

The output characteristic at junction temperatures of 25°C, 125°C and 200°C are shown in Figure 4-18 when supplied by a constant base current between 0.8-1.6 A. As shown, smaller base drive current can be used at low junction temperatures whilst maintaining a low collector-emitter voltage drop. Therefore a reduced base current provided by the active base drive will not degrade the conduction performance of the BJT. At the same time, it leads to lower base drive losses, which can be reduce by a maximum of 69% when compared to a conventional base drive at 25°C as can be found out in Figure 4-12.

4.6 Summary

In this chapter the performance of the active base drive for a SiC BJT has been presented. Experimental measurements for the proposed active base drive circuit have shown complete de-coupling between the on-state and transient requirement of the driver. This has enabled the base drive voltage to be reduced to minimize the power losses during BJT conduction period, achieved by controlling the duty cycle of a buck converter.

Comparisons with a traditional base drive show a minimum of 32% reduction of losses when considering a maximum required base current of 1.6A. The proposed base drive is able to adjust the base current by varying the duty cycle of the specific switch. Compared to a conventional base drive, this could increase energy saving substantially when considering a life cycle of product if the majority of its time is spent under partial loading conditions. The transient and conduction performance of the BJT show the minimum degradation in terms of the power losses using the proposed circuit compared to the conventional technique.

5 An Integrated Converter Design Using SiC BJT

5.1 Introduction

In this chapter, the function and feasibility of the proposed active base drive has been verified within the context of an integrated converter, designed to transform AC to DC power using a SiC BJT as a switch. Figure 5-1 shows a typical motor drive system used in an electrical vehicle, if a DC voltage source such as battery cells is used a load and the mechanical force is provided by a three-phase permanent magnetic motor. Permanent magnetic motor takes the advantages of its high power density, efficiency and excellent dynamic performance [94-101].

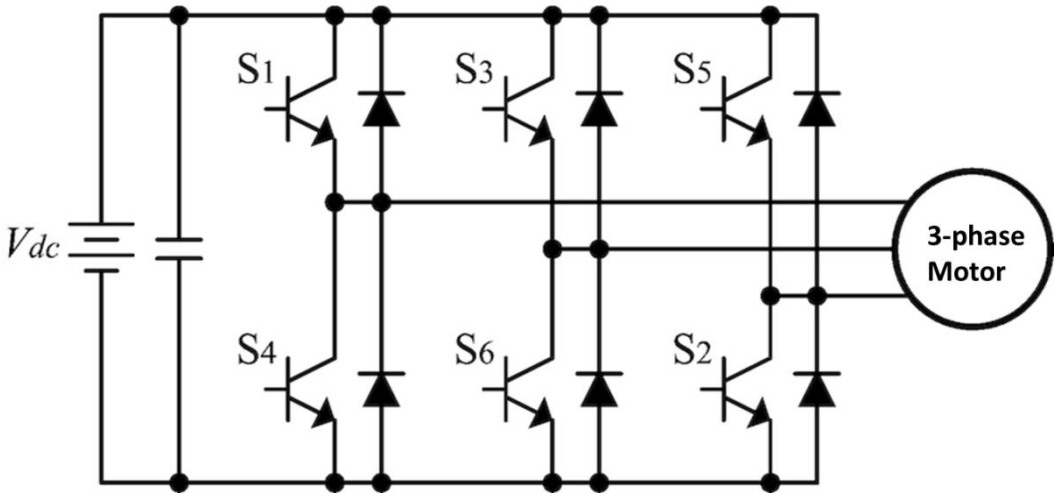


Figure 5-1 A typical Inverter motor drive

When a vehicle driver hits the brake, the back-EMF will be lower than the battery voltage at low vehicle speed and the energy is not able to be transferred to the battery. An integrated converter as shown in Figure 5-2 is applied to transfer AC energy from one phase of the motor to DC power during this process.

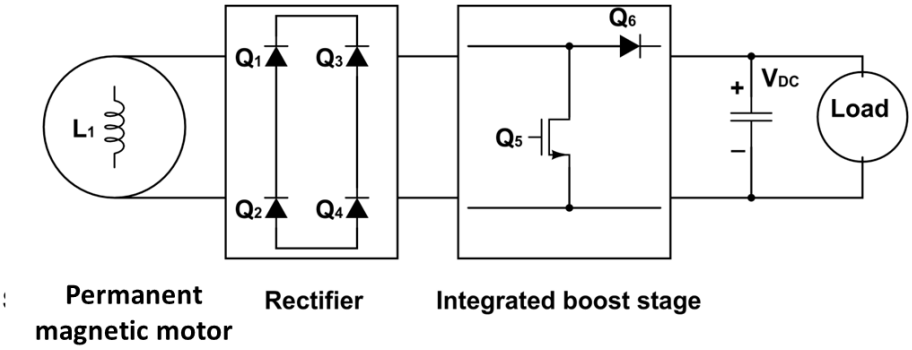


Figure 5-2 An integrated converter design with a single coil

5.2 Theoretical analysis on Discontinuous Current Mode (DCM) and Continuous Current Mode (CCM) boundary

In the analysis for the integrated converter concept, an AC power supply, V_{ac}, is connected in series with an inductor, L, as shown in Figure 5-3. The power switch Q_1 is controlled by a PWM signal to achieve demanded DC voltage.

When Q_1 is turned on, half of the bridge rectifier is conducting to build up the inductor (L) current. Due to the bridge rectifier, the direction of the current can only flow one-way: from AC source to the collector of Q_1 when it is turned on. At the output side, the diode (D_1) blocks the current flowing from the output capacitor (C_{out}). Therefore, the output voltage is always positive when referenced from the ground and a DC voltage is provided to the load R_L. When Q_1 is turned off, the energy stored in L is transferred to the load through the diode (D_1) and charges the output capacitor at the same time. The operation is similar to a boost converter except that the DC source is replaced by an AC source in the integrated converter.

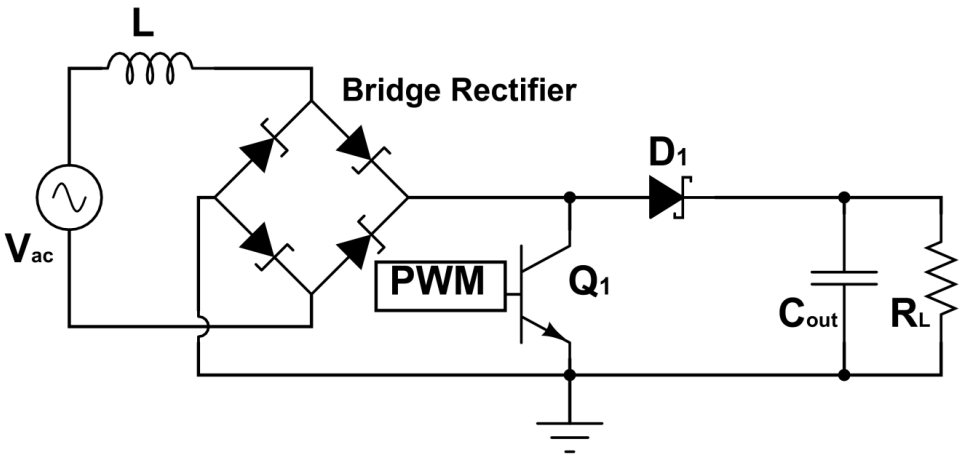


Figure 5-3 Schematic of the single phase integrated converter

5.2.1 Discontinuous conduction mode boundary

During converter operation, the current through the inductor L can be continuous or discontinuous, depending on various circuit parameters. Several assumptions are made when defining the boundary condition between these two working modes: Discontinuous and Continuous Modes (DCM and CCM).

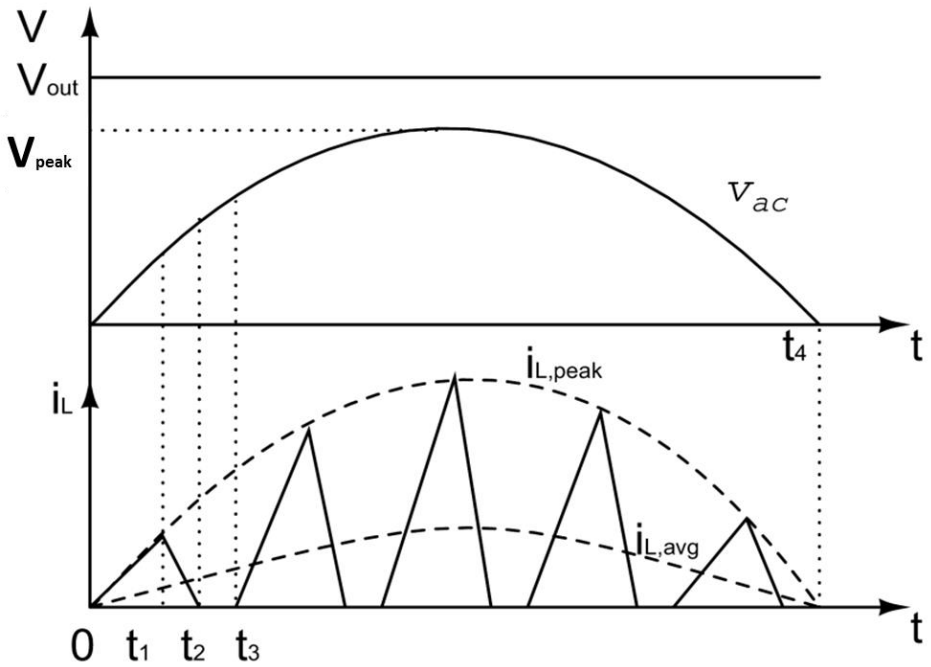


Figure 5-4 Discontinuous current mode (DCM) waveforms

Figure 5-4 shows schematic representation of typical current-voltage waveforms with respect to time for DCM where the inductor current i_L flows discontinuously and ends at zero in each period. As is the case with almost all power converters, the switching frequency of the converter is much higher than AC source frequency. During a switching cycle, if the current does not return to zero, it is designated as a CCM. The output capacitor (C_{out}) is assumed to be very large, so the output voltage (V_{out}) is considered to be constant with insignificant ripple voltage in the steady state. One half period of the input voltage (V_{ac}) is adequate to explain the operations of the converter. The input voltage (V_{ac}) is defined as:

$$V_{ac}(t) = V_{peak} \sin \omega_F t \quad \textbf{5-1}$$

Where V_{peak} is the amplitude and ω_F is the angular frequency where the interval from 0 to t_4 is half of the period T_F.

The other time intervals, as shown in Figure 5-4, can be defined based on the duty cycle D ($0 \leq D \leq 1$) and switching period T_s of the switch Q_1:

$0\text{-}t_1$: DT_s

$0\text{-}t_2$: $D_1 T_s$

$0\text{-}t_3$: T_s

And

$$D_1 = D + \Delta \quad \textbf{5-2}$$

Δ is the duty cycle difference between D_1 and D. Both D and D_1 are in the range of 0 to 1. In the DCM, the inductor current must end up at zero within one switching period. The voltage-second value must be equal during $0\text{-}t_1$ and $t_1\text{-}t_2$ which results in:

$$V_{ac}(t)DT_s + (V_{ac}(\mathrm{t}) - V_{out})(D_1 - D)T_s = 0 \quad \textbf{5-3}$$

and by solving Equation 5-3 we can have:

$$1 - \frac{V_{ac}(t)}{V_{out}} = \frac{D}{D_1} \quad \textbf{5-4}$$

Due to the condition that D_1 is less than1,

$$1 - \frac{V_{ac}(t)}{V_{out}} \geq D \quad \textbf{5-5}$$

Therefore:

$$\frac{V_{out}}{V_{ac}(t)} \geq \frac{1}{1-D} \quad \textbf{5-6}$$

The voltage gain α of the integrated converter is defined as:

$$\frac{V_{out}}{V_{peak}} = \alpha \quad \textbf{5-7}$$

Based on Equations 5-6 and 5-7, it can be shown that:

$$|\sin \omega_F t| \leq \alpha(1-D) \quad \textbf{5-8}$$

Therefore, the condition for DCM is required to be:

$$\alpha(1-D) \geq 1 \quad \textbf{5-9}$$

Beyond the boundary given by Equation 5-9, the converter would be operating in CCM.

When the peak voltage (V_{peak}) is constant, the relation between voltage gain (α) and duty cycle (D) is explored in the following assuming the converter is working in DCM.

According to Equations 5-2 and 5-4, it can be found that:

$$\frac{V_{out}}{V_{peak} \sin \omega_F t} = \frac{\Delta + D}{\Delta} \quad \textbf{5-10}$$

Therefore

$$\Delta = \frac{D}{\frac{\alpha}{\sin \omega_F t} - 1} \quad \textbf{5-11}$$

When the voltage gain is sufficient to ensure $\frac{\alpha}{\sin \omega_F t} \gg 1$,

$$\Delta \approx \frac{D}{\alpha} \sin \omega_F t \quad \textbf{5-12}$$

Therefore the peak current ($i_{L,peak}$) of the inductor, shown in Figure 5-4, for one switching cycle is obtained:

$$i_{L,peak} = \frac{V_{ac}(t) D T_s}{L} \quad \textbf{5-13}$$

The average current ($i_{L,average}$) of the inductor in each switching equals the input average current from AC power supply. The area of the triangle is divided by the period time in Figure 5-4 and combining Equation 5-10 to 5-13 yields the average current:

$$i_{in}(t) = i_{L,average} = \frac{i_{L,peak}}{2}(D + \Delta) = \frac{V_{peak} \sin \omega_F t \, D^2 T_s}{2L} \frac{\alpha + \sin \omega_F t}{\alpha} \quad \textbf{5-14}$$

The input energy drawn from AC source is the integral of the input voltage $V_{ac}(t)$ and current $i_{in}(t)$ over half period (T_F):

$$W_{in} = \int_0^{\frac{T_F}{2}} V_{ac}(t) i_{in}(t) dt = \frac{V_{peak}^2 D^2 T_s}{2L\alpha} \int_0^{\frac{T_F}{2}} (sin^2 \omega_F t)(\alpha + \sin \omega_F t) dt \quad \textbf{5-15}$$

$$= \frac{V_{peak}^2 D^2 T_s}{2L\alpha} \frac{3\pi\alpha + 8}{6\omega_F} = \frac{V_{peak}^2 D^2 T_s (3\pi\alpha + 8) T_F}{24\pi L\alpha}$$

The output energy to the resistive load R_L in Figure 5-3 can be obtained:

$$W_{out} = \frac{T_F}{2} \frac{V_{out}^2}{R_L} \quad \textbf{5-16}$$

Assuming the converter efficiency is represented by η,

$$W_{out} = \eta W_{in} \quad \textbf{5-17}$$

Solving Equations 5-15, 5-16 and 5-17, the voltage gain α is dependent on the duty cycle (D), inductance (L), load resistance (R_L), system efficiency (η) and switching period (T_s) when the converter is working in the DCM. The voltage gain of α can be theoretically estimated by Equation 5-18.

$$R_L \eta D^2 T_s (3\pi\alpha + 8) = 12\pi L\alpha^3 \quad \textbf{5-18}$$

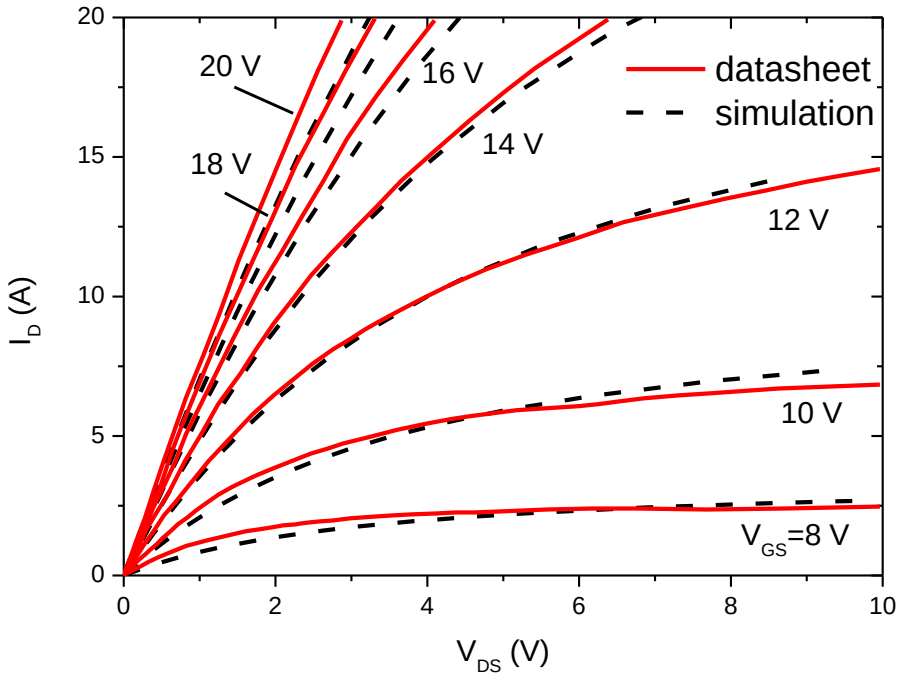
5.2.2 Circuit simulation for the integrated converter

The integrated converter, as shown in Figure 5-2, was simulated using LTSpice. SiC diodes and SiC BJT are used in the simulation; the SPICE models were obtained from the device manufacturers, GeneSiC and TranSiC [18, 102]. In order to compare performances of different power devices, a SiC MOSFET is used in the integrated converter simulation with its SPICE model based on a ROHM product [103]. Some key parameters from the datasheet are summarized in

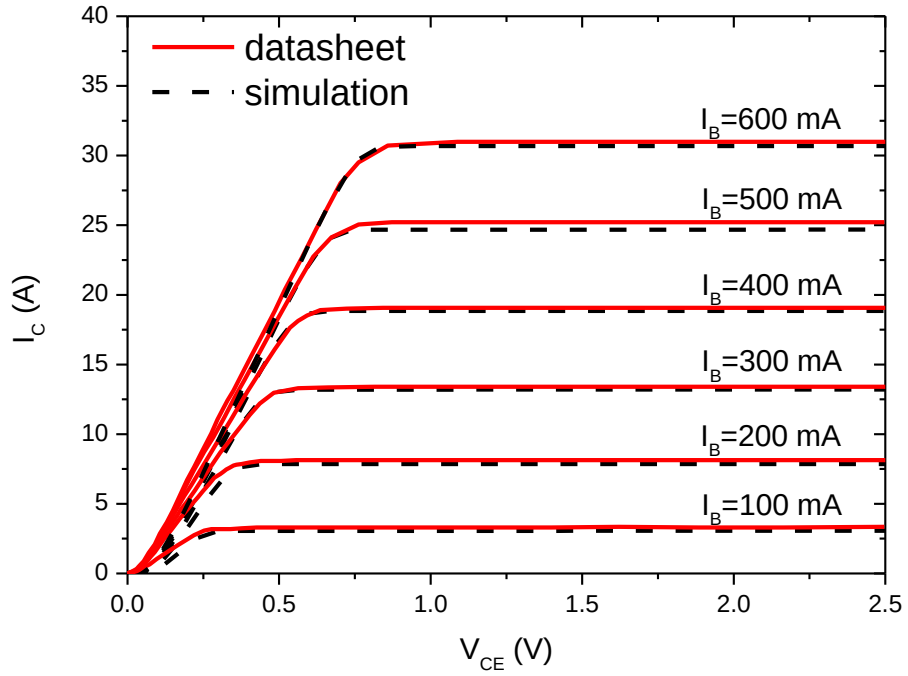
Table 5-1 Comparisons of SiC BJT and SiC MOSFET key parameters

	SiC BJT	SiC MOSFET
Maximum Drain-Source voltage (V)	1200	1200
Continuous Drain Current (A) @25°C	22	20
Maximum Base Current (A)	3	NA
Gate Threshhold Voltage (V)	NA	2.8

Drain current (I_D) vs. drain-source voltage (V_{DS}) in the simulation, with respect to different gate-source voltages (V_{GS}), is shown in Figure 5-5a at a junction temperature 25ºC. A slight disagreement is shown between the datasheet and the simulation results when operated under high gate voltages. In terms of the SiC BJT as shown in Figure 5-5b, the simulation model can accurately describe the device performance.



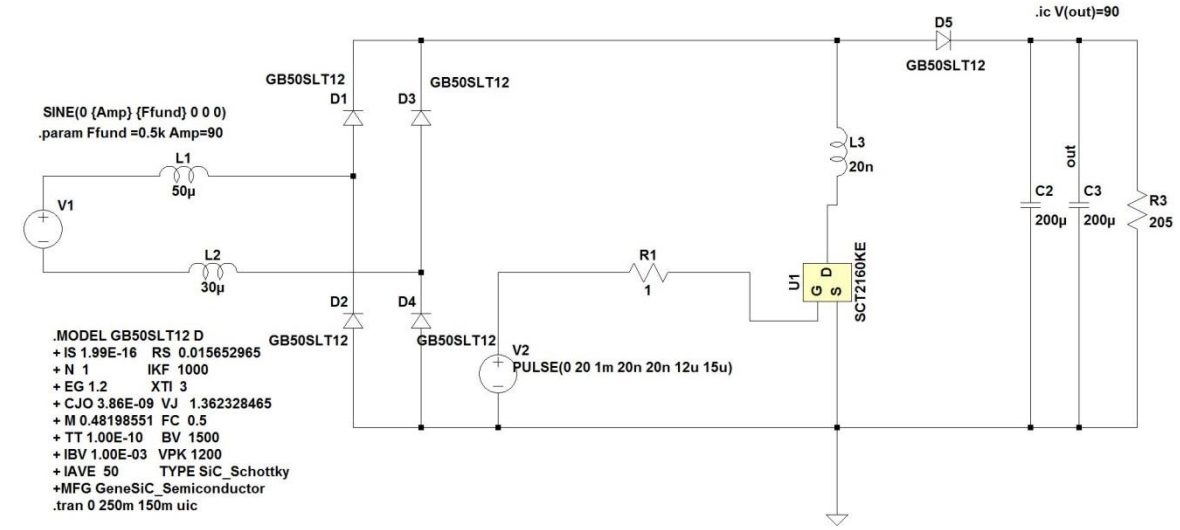
(a) I-V characteristics of SiC MOSFET from ROHM



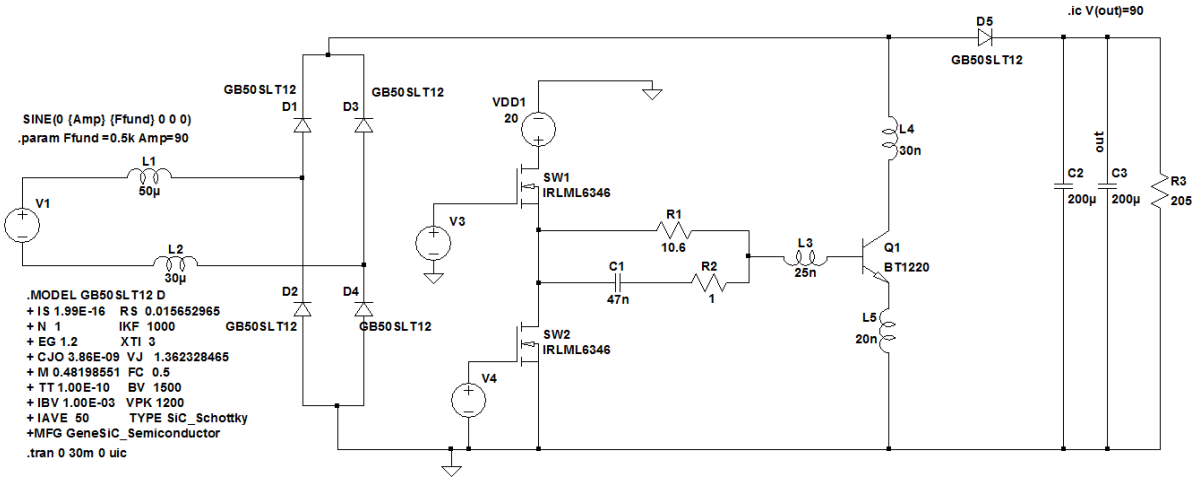
(b) I-V characteristics of SiC BJT from TranSiC

Figure 5-5 Comparisons between simulation results and characteristics from datasheets

As shown in Figure 5-6, the SiC MOSEFT is simply driven from a DC supply voltage via a gate resistor while the SiC BJT is driven by a conventional base driver at the junction temperature 25ºC. The control PWM signals are both generated from a pulse source (V2) with amplitude 20V. The peak value (V_{peak}) of the AC input (V1) is set to 90V with a fundamental frequency of 500Hz. The package parasitic inductances can influence the switching performance in terms of the current peak and electrical resonance so they are included in the simulation for accurate results. The load is composed of a 400µF output capacitor and 205Ω resistor which is sufficient to maintain the peak current of the switch Q1 to be lower than its rated value of 20A.



(a) Converter simulation schematic with SiC MOSFET



(b) Converter simulation schematic with SiC BJT

Figure 5-6 Integrated converter simulation circuit

Based on Equations 5-9 and 5-18, the various duty cycles of Q1 lead to different output voltages and operation modes of the converter. Therefore the converter can supply various powers to the load. In order to compare with the performance between the SiC BJT and SiC MOSFET, the inductors and capacitors in the simulation are selected as ideal components without any power consumptions. The converter efficiency is defined as the ratio of input power to output power. As shown in Figure 5-7, under full power conditions, the converter using SiC BJT is more efficient than that of the SiC MOSFET. Under high output power conditions, the power devices must conduct high current. As shown in Figure 5-5, the voltage

drops across the SiC BJT and SiC MOSFET are 0.5V and 3V respectively when 20A flows through the device. Therefore, the conduction losses of the SiC MOSFET are six times higher than the SiC BJT. As a result, the converter efficiency drops rapidly with increasing power as shown in Figure 5-7. The converter efficiency slowly decreases when using SiC BJT since its voltage drop increases only by 0.5V at 20A collector current. Therefore, the integrated converter is implemented using the SiC BJT as a switch in order to achieve lower power losses.

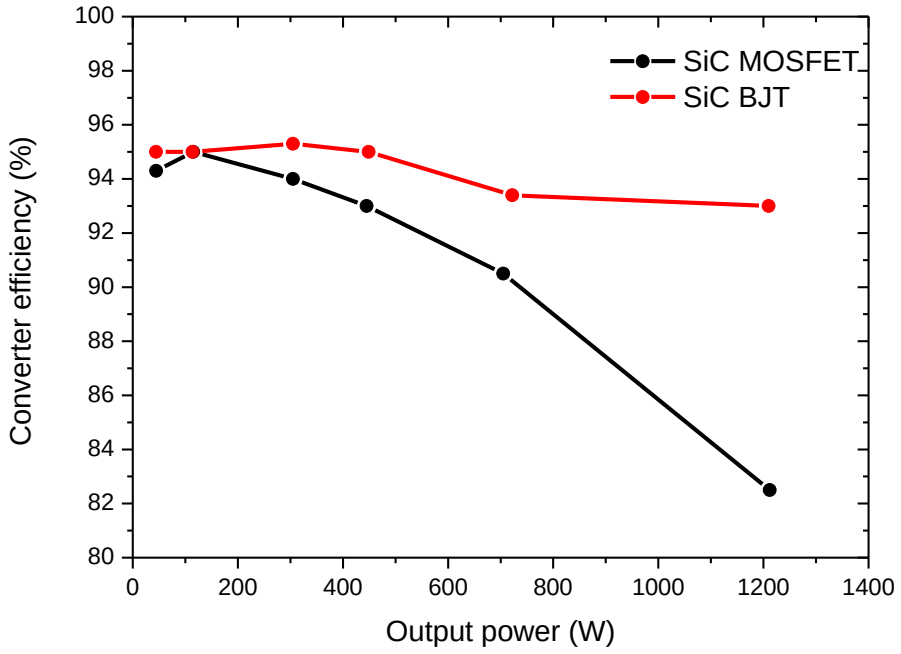


Figure 5-7 Integrated converter efficiency comparisons from simulations

Figure 5-8shows that the voltage gain (α in Equation 5-7) changes with the duty cycle, which shows that the output voltage of the converter is proportional to the duty cycle. Using the condition defined in Equation 5-9, CCM and DCM are estimated, given α and D obtained from the simulation. The mode estimation is shown in Figure 5-8, which completely matches the simulation results. Figure 5-9 shows the simulation waveforms for the duty cycles of 10%, 40% and 70%..

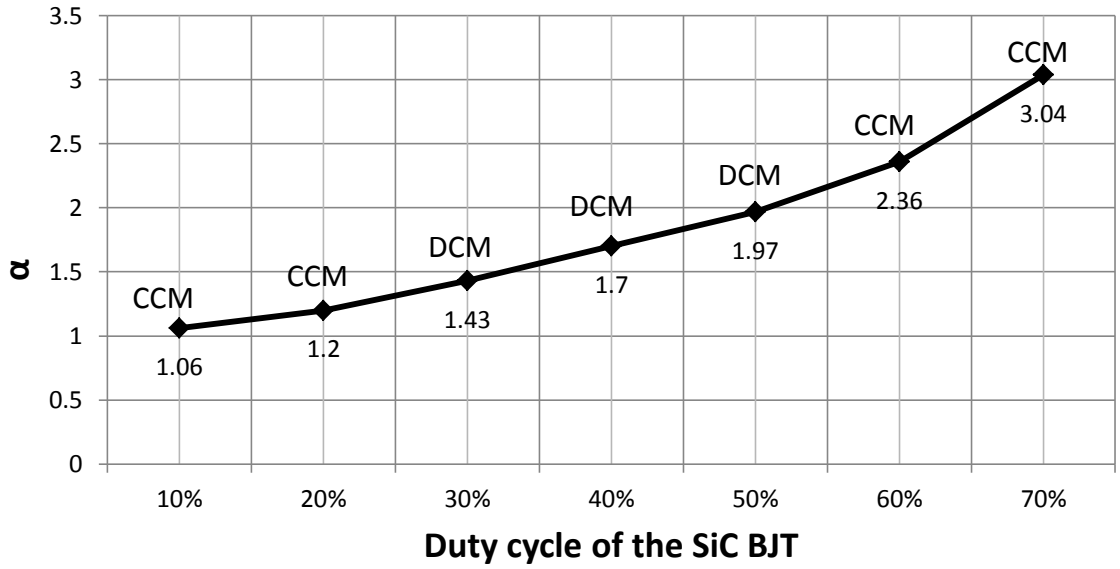
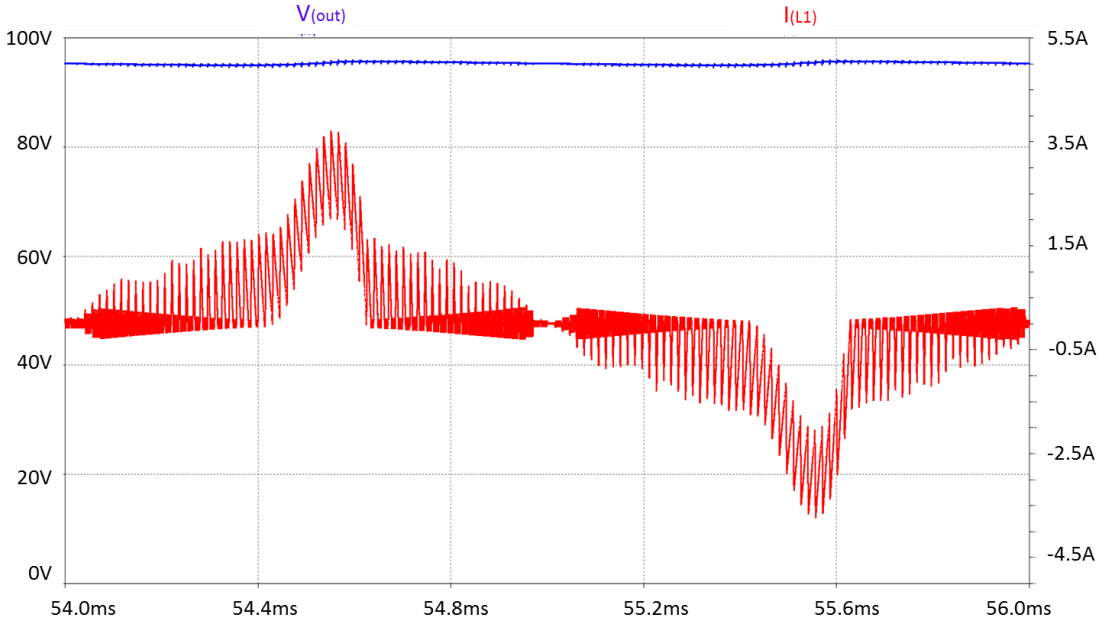
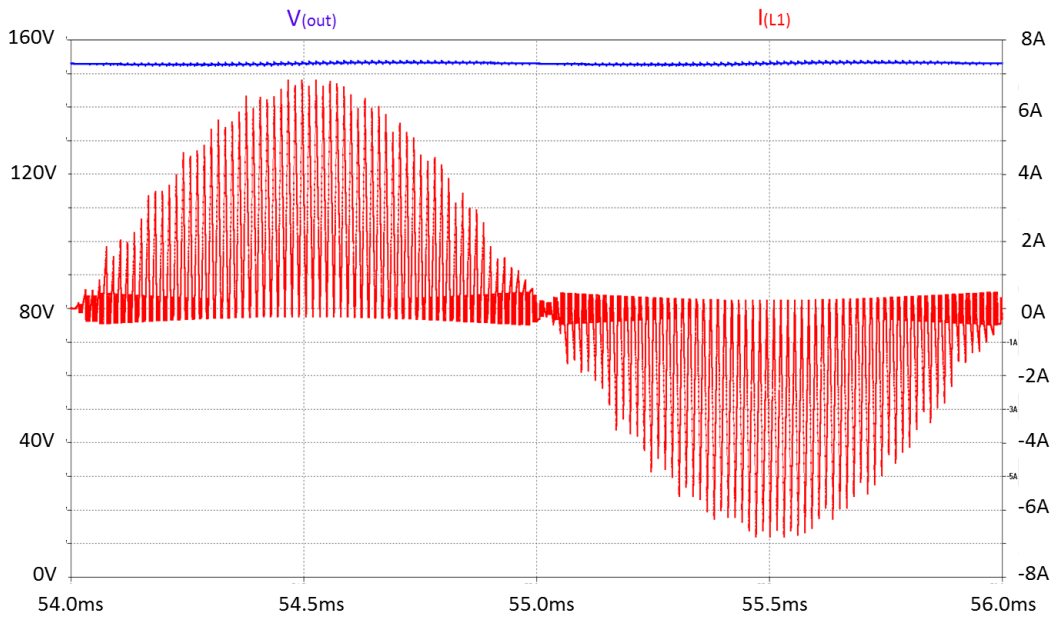


Figure 5-8 Voltage gain and duty cycle

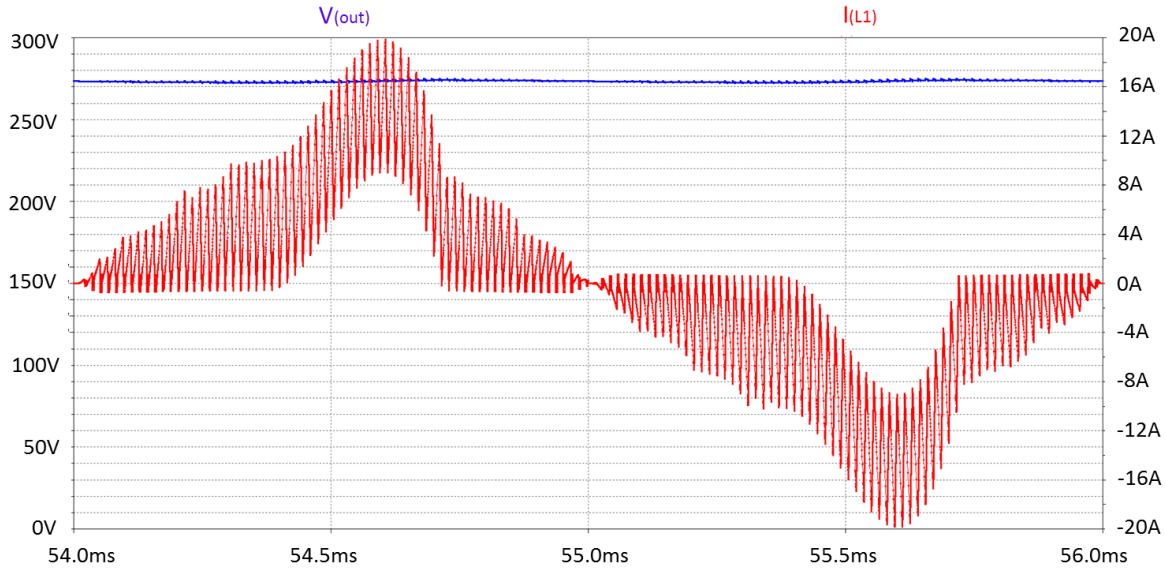


(a)

10% duty cycle



(b) 40% duty cycle



(c) 70% duty cycle

Figure 5-9 Output voltage and L1 current waveforms

5.2.3 Use of the active base driver for the integrated converter in simulations

In order to compare the power losses between the conventional and active base drivers and their influences on the wider system efficiency, the integrated converter using the active base driver was simulated in LTSpice using circuit diagram is shown in Figure 5-10. The corresponding circuit for the conventional driver is shown in Figure 5-6b. The parameters for both drivers are identical to those used in Figure 4-3, i.e. supplying 1.6A base current to drive

20A collector current through the SiC BJT. As shown in Figure 5-9c, with 70% duty cycle the maximum current is 20A which remains within the rating of the SiC BJT. This leads to a full load power of 357W.

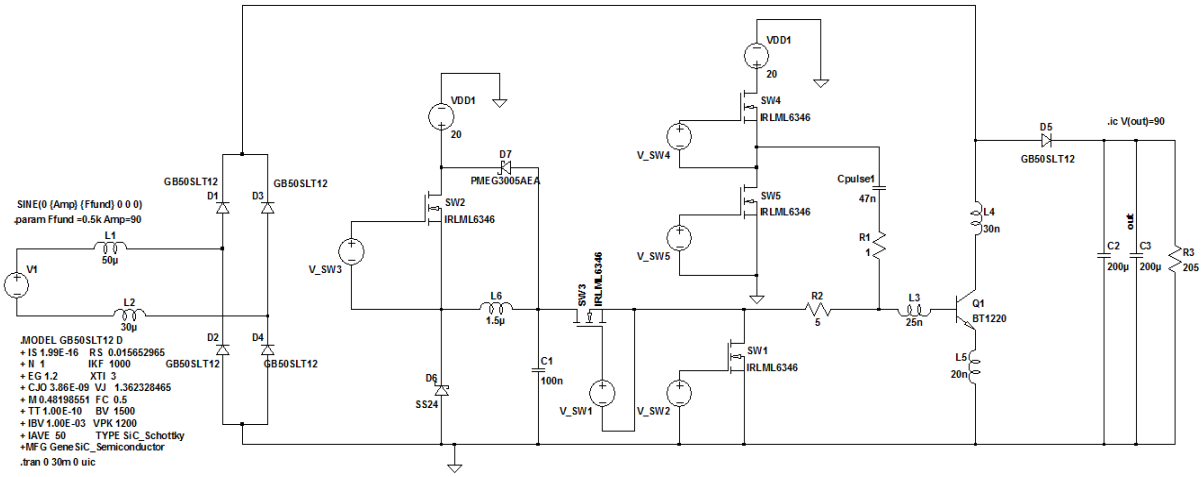


Figure 5-10 The integrated circuit using the active base driver

The predicted power losses of the drivers in the simulation are plotted in Figure 5-11 with various duty cycles. The output powers of the converter are 44W, 75W, 146W and 357W for the duty cycles of 10%, 30%, 50% and 70%. Under any situation, the active base driver consumes less power than the conventional driver.

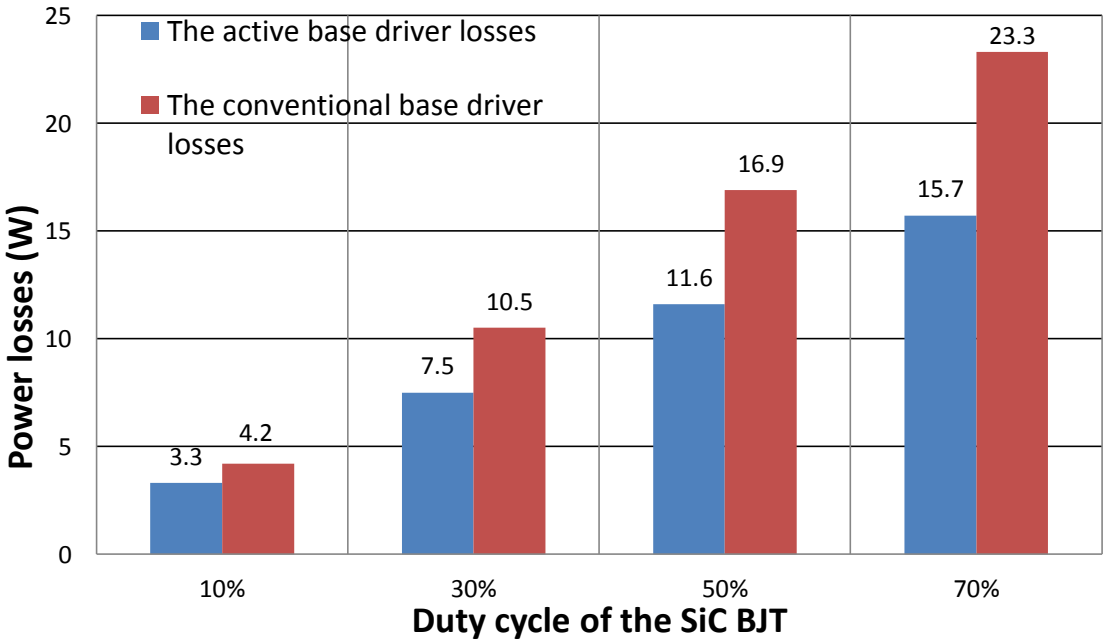


Figure 5-11 Driver losses

Taking into account of the driver losses, the whole converter system efficiency is compared in Figure 5-12 for both partial loads and full load. When the load is very light, the driver losses occupy a large portion of the system losses. Therefore, the efficiency drops quickly for output powers from 44W to 75W. When the output power increases, driver losses are not dominant compared with the system power and the efficiency increases.

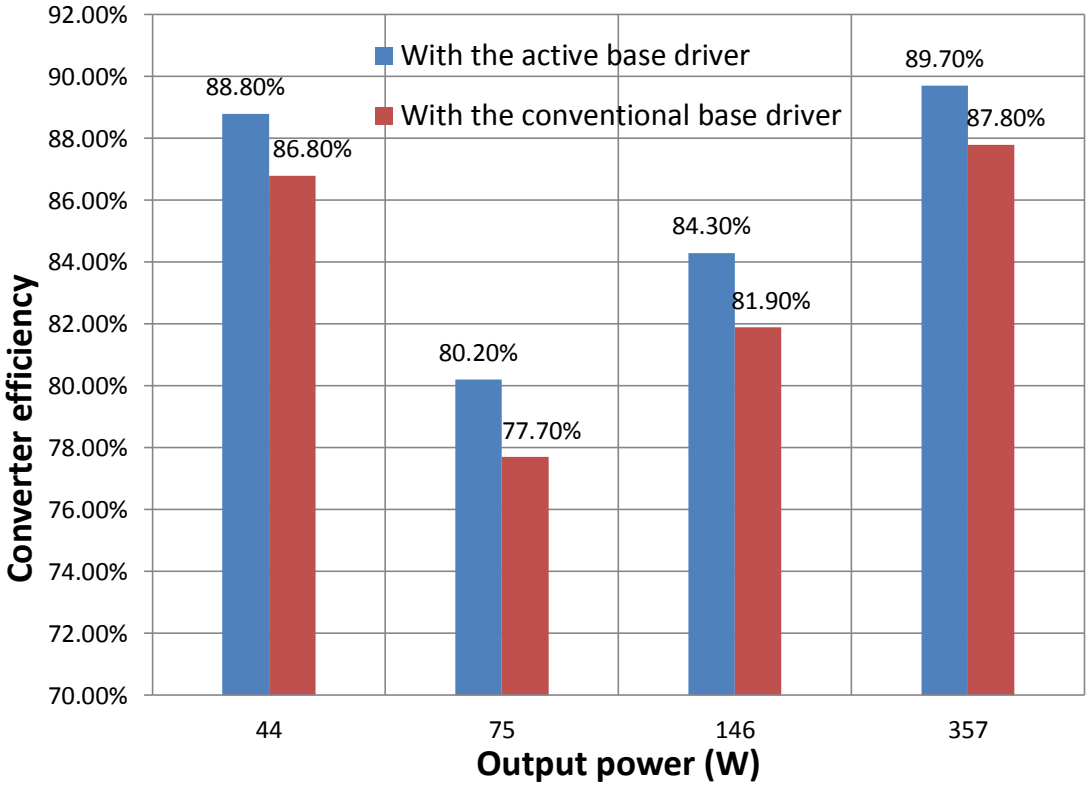


Figure 5-12 Converter system efficiency

5.3 Hardware prototype using SiC BJT

A hardware prototype for generating experimental results was designed and constructed. The corresponding circuit schematic is shown in Figure 5-6b in this section. The integrated converter is operated in either CCM or DCM with various duty cycles and output voltages. Figure 5-13 shows the top level design of the integrated converter system. The power devices, including diodes and the SiC BJT, are attached to a heat sink with a DC-powered fan forming a forced air cooling system to ensure the losses are effectively dissipated as quickly and efficiently as possible. The blue blocks shown in the diagram are housed within a polycarbonate box [104] for protection purposes.

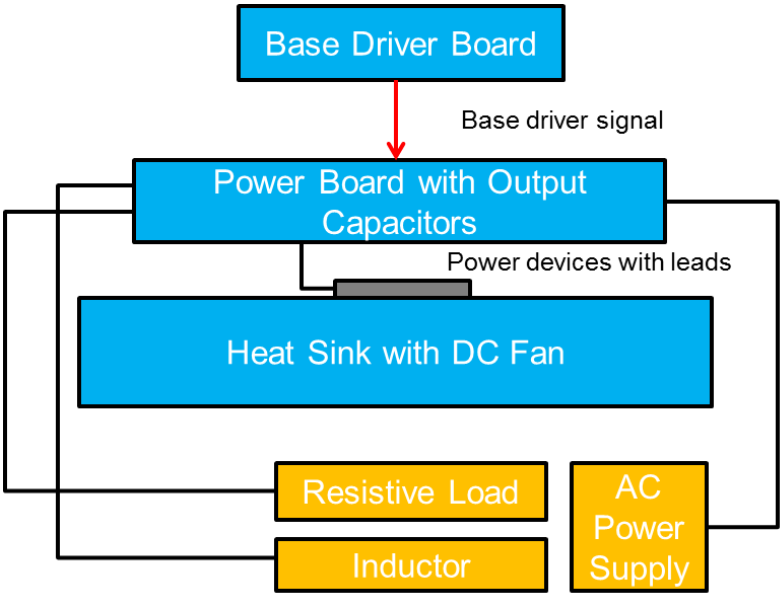
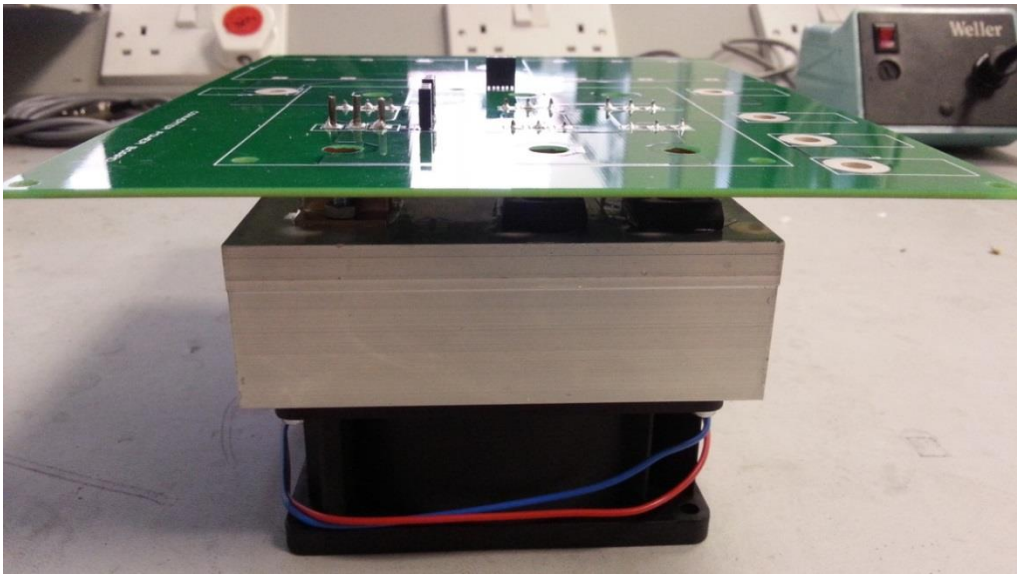
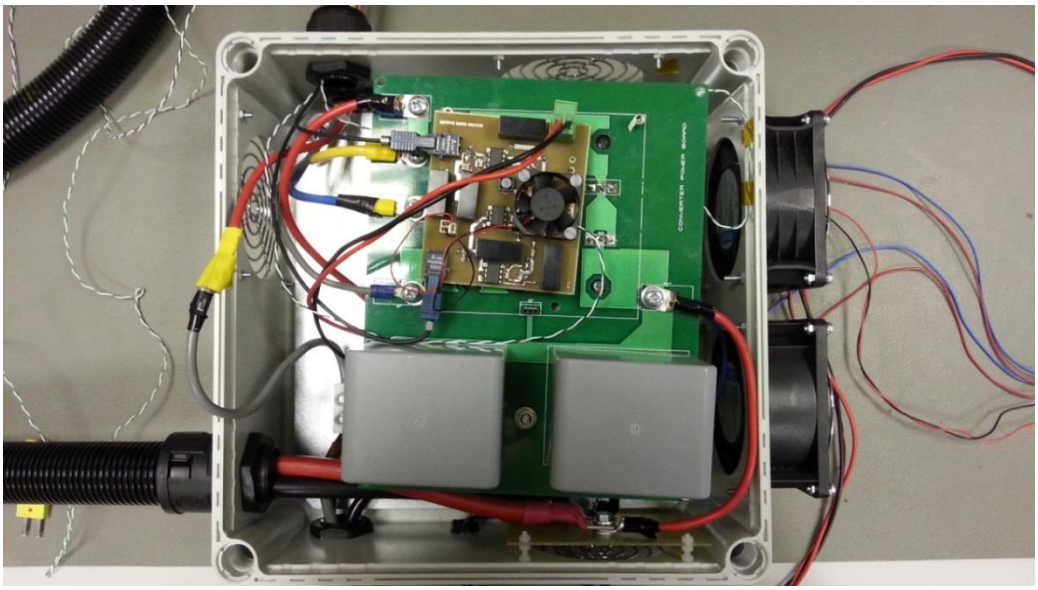


Figure 5-13 Converter hardware structure diagram

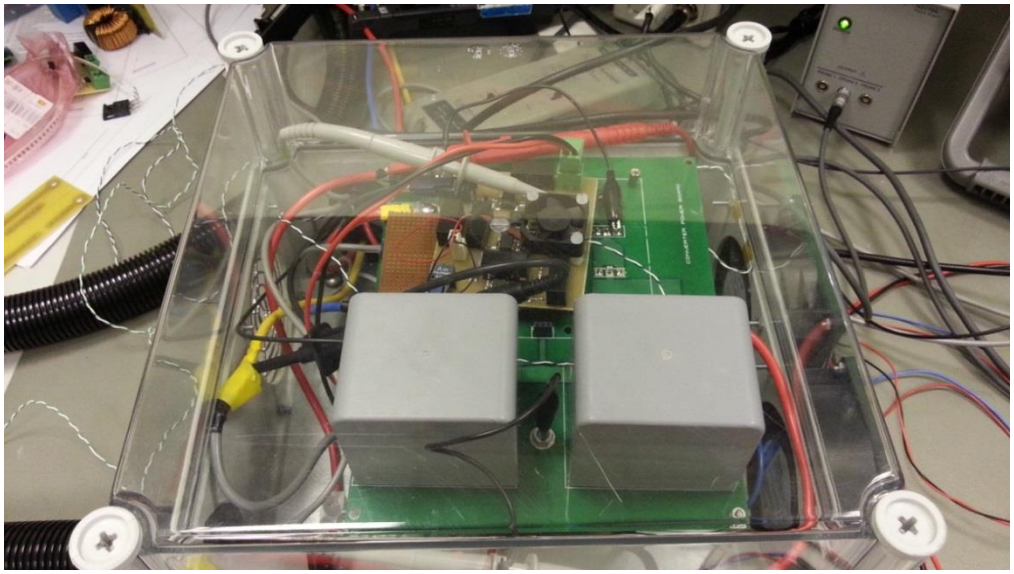
Figure 5-14a shows the hardware prototype corresponding to the structure diagram in Figure 5-13 without the base drive. The active base driver proposed in Chapter 4, is used to provide base current to turn on and turn off the SiC BJT in the converter. A DC fan attached to the heat sink is mounted onto the bottom metal plate of the housing which can be configured as a common ground during the operation, as shown in Figure 5-14b. Two extra DC fans attached to the enclosure side wall to encourage forced air circulation into and extraction from the test circuit. Two thermo-couples are attached onto the base drive resistor and heat sink respectively to monitor temperature. Figure 5-14c shows the configuration for the test with the transparent cover and probes. The driver board is plugged onto the power PCB. A low power DC fan is required to dissipate the resistor heat in the driver. The schematic and layout designs for this PCB are shown in Appendix 8-18 and Appendix 8-19. In this design large ground planes are used on the PCB to reduce current loop inductance and dissipate heat from power device leads.



(a)



(b)



(c)

Figure 5-14 Integrated converter hardware: (a) side view (b) top view (c) top view with the conver on

The electrical devices and cooling system components of the prototype are summarized in Table 5-2. The peak value (V_{peak}) and the sine wave frequency (f_F) of AC input power supply is 90V and 500Hz, respectively. The temperature of load resistors is kept constant at 25°C by an air cooling system to avoid resistance temperature-dependent variation. The junction-ambient temperature thermal resistance is 1.12 ºC/W, which is the summation of junction-case resistance and heat sink resistance shown in Table 5-2. Assuming that the maximum output power is 1.2kW; the efficiency of the converter is 90% (lower than the worst simulation result); and all the losses are caused by the SiC BJT, the maximum junction temperature is 159.4°C at an ambient temperature of 25°C. This is lower than the maximum junction temperature that limits the SiC BJT. Therefore, the selected heatsink is capable of effectively dissipating heat from its sources.

Table 5-2 Hardware parameters

	Value	Manufacturer
AC power supply	Max. 1.5kVA	California Instruments 3001Lx
SiC Diode	1200V/30A	ROHM schottky diode [105]
SiC BJT	1200V/20A	TranSiC [17]
Output capacitor	200µF	VISHAY ROEDERSTEIN [106]
Resistive load	205Ω	Hill stone HLB 290-12
Inductor	80µH	Made in house
DC fan	Max. 280 m^3/h	EBM PAPST 3212JN [107]
Heat sink	0.12 ºC/W	H S MARSTON 890SP-01000-A-100 [108]

5.4 Experimental results analysis

The duty cycles were varied from 10% to 70%. The simulation results for the output voltage and power factor (PF) and the measured results from the experiment are summarized in Figure 5-15. The operation modes are observed from the experiment. The voltage source in the simulation is assumed to be ideal whereas in the experiment the power source has limited impedance and the simultaneous current causes the voltage glitches as shown in Figure 5-16. All of these factors will affect the PF measurement results. In the experiment, the power factor is measured by AC power supply and it is almost 0.97 while the converter is operating in DCM, this slightly reduces at a high output voltage. On the contrary, the low duty cycle leads to a small power factor, which usually results in internal power losses of the AC power supply. When the converter is working with such low power factor, it requires an additional power factor correction circuit at the front end. The output voltage increases with the duty cycle, but it is non-linear as expected from Equation 5-18.

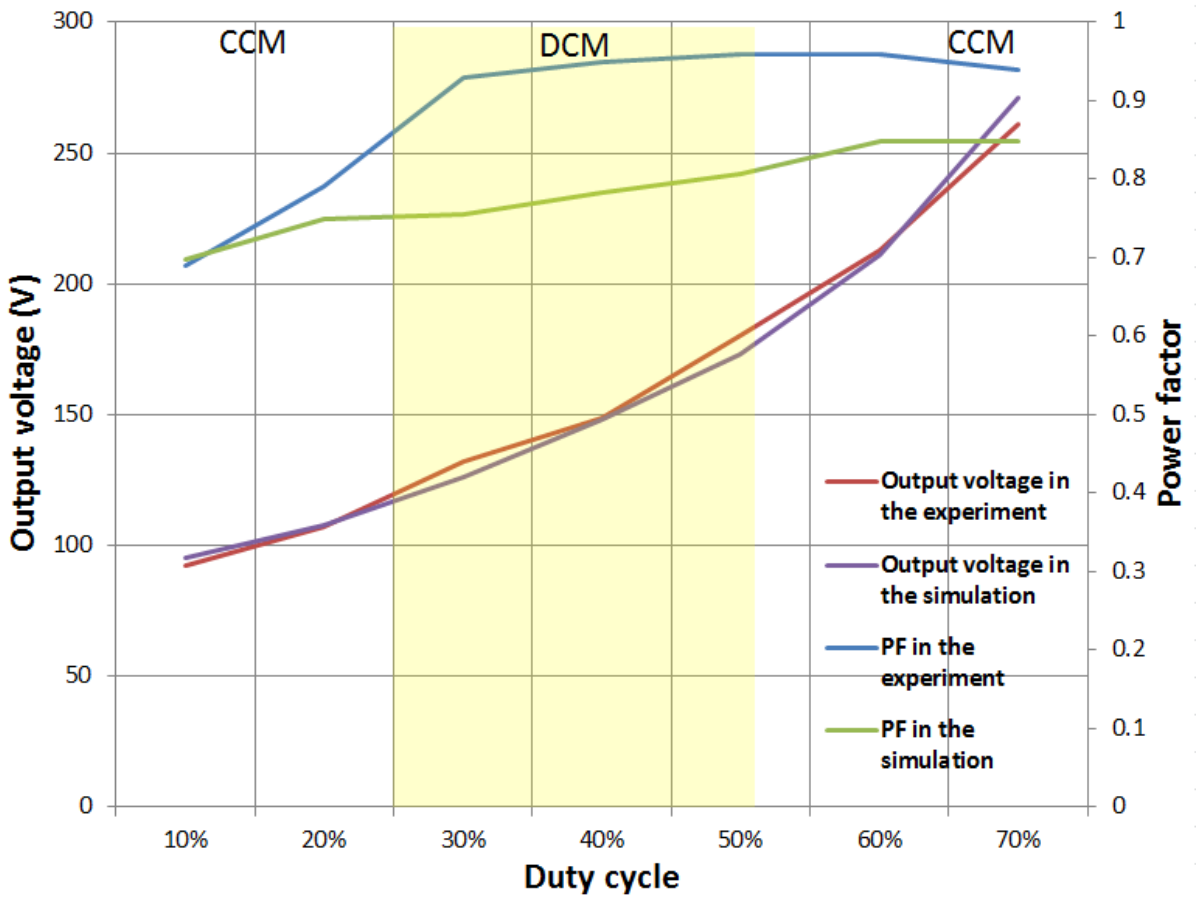
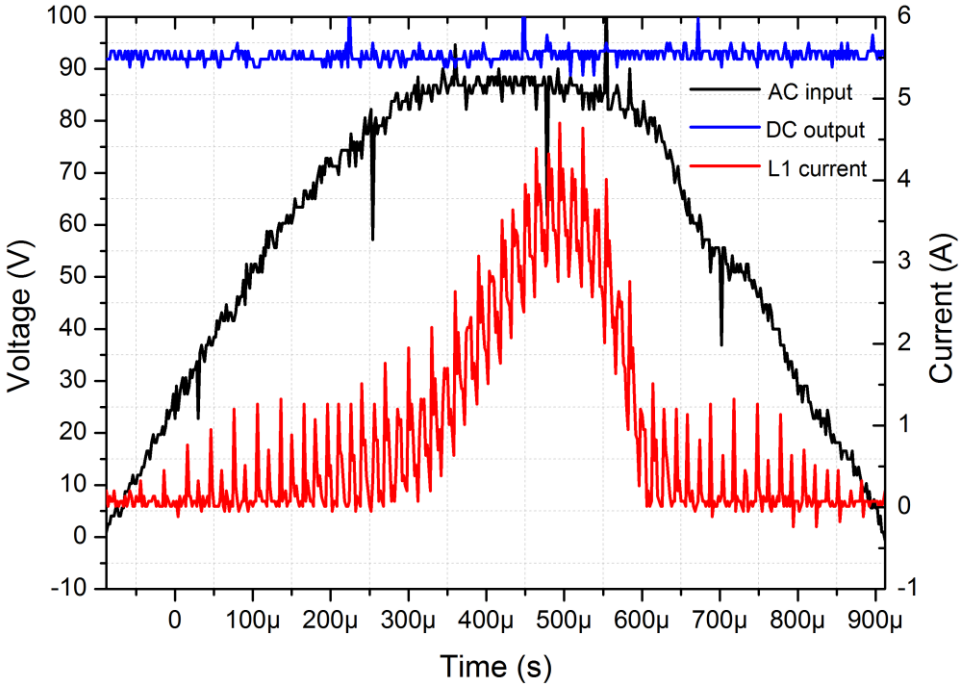


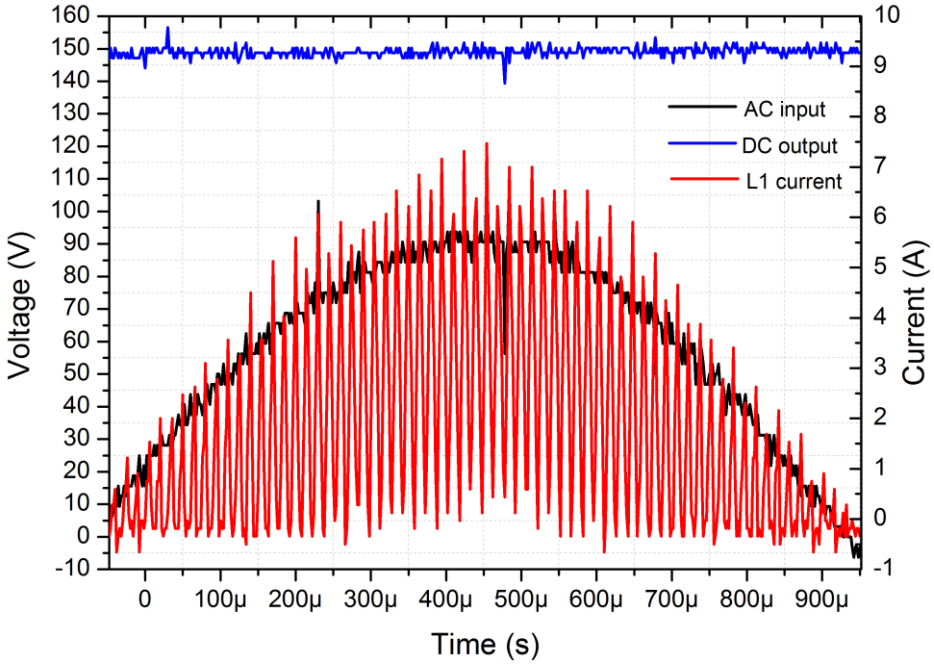
Figure 5-15 Power factor of the power supply and converter output voltage

Figure 5-16 shows the input voltage, output voltage and inductor current with 10%, 40% and 70% duty cycles. The operation modes vary from CCM to DCM then back to CCM again, matching the simulation results. The output voltages in the simulation are 94V, 152V and 271V with 10%, 40% and 70% duty cycle whereas in the experiment they 93V, 150V and 267V. From the peak current point of view, they are 4.1A, 6.9A and 20A in the simulation whereas they are 4.5A, 7.1A and 22A in the experiment. The difference between the results is modest which can be caused by the tolerance of the components in the experiment. When the duty cycle is 10%, the inductor current is very small and discontinuous especially under low input voltage. As a result, the current distortion is very bad with low power factor as measured. So it does not follow the sinusoid. Since the inductor is one of the motor windings in an electrical car, there is no space for a bulky filter in permanent magnetic motor. Therefore no input filter is fitted at the front end of the design to ease the current distortion. Due to fast switching speed and high collector current sourced from the power supply, distortion occurs, which adds glitches to the voltage waveform as observed in the

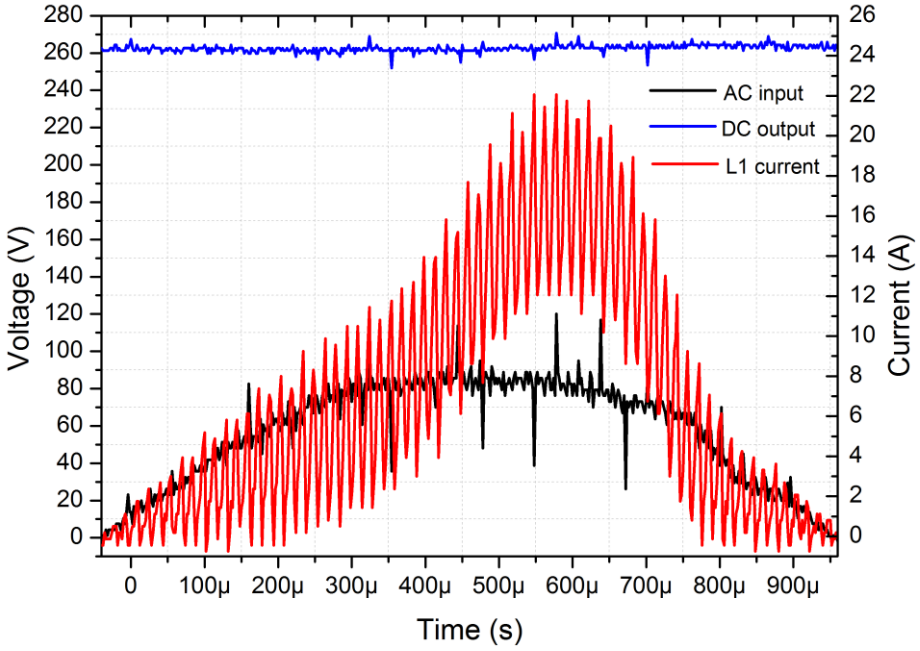
measurement in Figure 5-16. In addition, the input current, equalling to L1 current, is highly distorted using a low duty cycle for switching which results in a low power factor, as shown in Figure 5-16a.



(a) 10% duty cycle



(b) 40% duty cycle



(c) 70% duty cycle

Figure 5-16 Measured converter operation with various duty cycles

The base current is 1.6A provided by the proposed driver to give adequate margins for the current gain tolerance. The temperature of the base resistor (R_1 in Figure 4-2) is 74°C as measured in the experiment. Therefore, a DC cooling fan is necessary. The converter efficiency, due to the driver losses, decreases by 8.6% and 16%, using the proposed and conventional driver unit respectively. If the inductor comprises the winding of the motor in the future, the iron losses in the magnetic flux conducting parts need to be reduced to relieve the burden on the motor cooling system.

5.5 Summary

The integrated converter with the diode rectifier is proposed to convert AC power to a boosted DC voltage, which is an essential function required in an electrical vehicle during the re-generation process. The simulation and experimental results are presented to verify the function of the proposed converter and the feasibility of the active base drive. A small deviation between the simulation and experimental results demonstrates that the device models used in the simulation were accurate and representative. According to the simulation results in LTSpice, the converter efficiency using SiC BJT is maximum 8% higher than that

using SiC MOSFET when the output power is 1200W. In a full power range up to 1200W, the efficiency of a SiC BJT converter is always higher than that of a SiC MOSFET converter as verified in the simulation. The integrated converters, driven by the active base drive and conventional base drive, are simulated in section 5.2.3. The losses of the active base drive are lower than the conventional one under various duty cycles meanwhile the converter efficiency using the active drive is higher accordingly under various output powers.

Two operation modes, CCM and DCM, are defined and analysed quantitatively with equations. The active base drive has been used in the integrated converter to drive SiC BJT due to its high drive efficiency as presented in Chapter 4. The proposed base drive increase the system efficiency by 7.4% (16%-8.6%=7.4%) compared with using conventional base drive. The cooling system designed in the prototype can effectively dissipate the heat generated from the power devices and base drive resistor, which guarantees all the electrical components working within their thermal margins during normal operation cycles. It has been demonstrated that the base driver losses constitute a large portion of the total system losses; high power converters using SiC BJT can easily achieve higher efficiency than lower power converters.

6 Conclusion

6.1 Conclusions

The fabrication and commercialization of wide band gap power devices has progressed significantly in the last decades. SiC is a promising member in the wide bandgap semiconductor family where it has overcome several of the limitations of Si, e.g. thermal conductivity, critical electric field strengths and intrinsic carrier concentration. It has been shown to offer the advanced performance, especially in high switching frequency and high temperature applications [109-112]. Due to the fast switching speed, low on-state conduction loss, absence of the gate oxide, lack of the second breakdown, high breakdown voltage and current gain, SiC BJT has recently attracted significant interest.

The use of the bipolar junction structures in power conversion system always tends to be impeded by high power consumption and subsequent complex driver design because of the current driven characteristic. Therefore, means of achieving low power loss base driver is likely to be an important factor in the uptake of SiC technology.

The key contributions of this thesis are highlighted in this chapter.

a) High junction temperature switching test [113]

The switching losses of the SiC BJT have been measured experimentally at junction temperature above 200ºC. As a baseline for the comparison, a Si IGBT with the same voltage/current rating as SiC BJT was tested at a maximum junction temperature of 165ºC, a limit constrained by the material properties. A short-circuit current was used periodically to heat up the device under test. The switching power loss of SiC BJT was found to be independent to the junction temperature and is much lower than that of Si IGBT which performs poorly at high junction temperatures in the experiment.

b) Energy recovery concept realization in the base driver design [114]

The capacitor in the conventional base driver needs to generate a high current peak for fast switching. However, its power loss increases significantly in proportion to the switching frequency and supply voltage. An energy recovery function was proposed to save the energy stored in the capacitor and therefore improve the driver efficiency. A 1.7kW boost converter was prototyped to validate the function of the energy recovery base driver and investigate the

performances of the SiC BJT subject to different switching frequencies. The maximum power saving was shown to be 15.1% at 143kHz switching frequency.

c) The active base driver design

For applications requiring a large base current and high duty cycle, the resistor in the energy recovery base drivers of Chapter 3 is a major power consumer in the driver unit. The base current that is required to maintain BJT conduction is dependent upon the worst case conditions: the minimum current gain at high junction temperature. Considering the converter with a light load or in a low temperature environment, the base driver provides the excessive DC current compared to that actually needed. The active base driver design can adjust the base current instead of the fixed value that is used in a conventional drive in order to reduce the resistor power loss.

During the transient period in the switching process, a separate current path is used to generate high peak current for fast switching which is composed of RC elements. The transient and conduction performance of SiC BJT is minimally degraded when using the proposed circuit compared to the conventional technique. The active base driver is evaluated in an integrated AC-DC converter.

d) SiC BJT application in the integrated converter

The fundamental analysis on operation modes and boundary has been presented for the integrated converter, which takes the advantage of weight reduction and high integration. The system's robustness is enhanced since every phase channel can work independently. The theoretical model, simulation results and experimental measurements correlate with each other.

The active base driver provides the base current to switch the SiC BJT in the converter. The whole system efficiency is 7.4% higher than that using the conventional driver with 1.4A base current.

6.2 Further work

A few extensions to the research can be explored in the future. High performances at junction temperature above 200ºC have been demonstrated in Chapter 2 for SiC BJTs. In order to drive the SiC BJT effectively, the drive unit must be closely connected to the device in the

high temperature environment. All the electrical and passive components in the drive unit are Si-based and not able to survive when the junction temperatures are above 170 ºC. This is particularly the case for the capacitor, whose the rated temperature is much lower than that of the semiconductor IC. So the base driver with the capability of working under high temperatures warrants further explorations.

The proposed active base driver in the thesis is designed to drive BJTs. The driver is able to provide multiple voltage levels, which can also be used to turn on the voltage-controlled device such as MOSFETs. The transient speed of the MOSFET is adjustable if the driver can supply various voltage levels to the gate. The active base driver can be converted to a multi-functional drive unit for both voltage-controlled and current-controlled power devices.

Advanced control technologies are going to be implemented to the converters and drives in the future if the proposed designs are going to be commercialized. Traditional analogue control can be used with the cost of large board size, complex tolerance consideration and high components' expenses. Digital control with a microcontroller seems to be the preferred solution. Parameters such as the device case temperature, the output voltage and the inductor current are monitored and the data are sent to the controller. Based on this information, the microcontroller is able to generate suitable duty cycles to switch the SiC BJT. This requires both software and hardware design.

7 Reference

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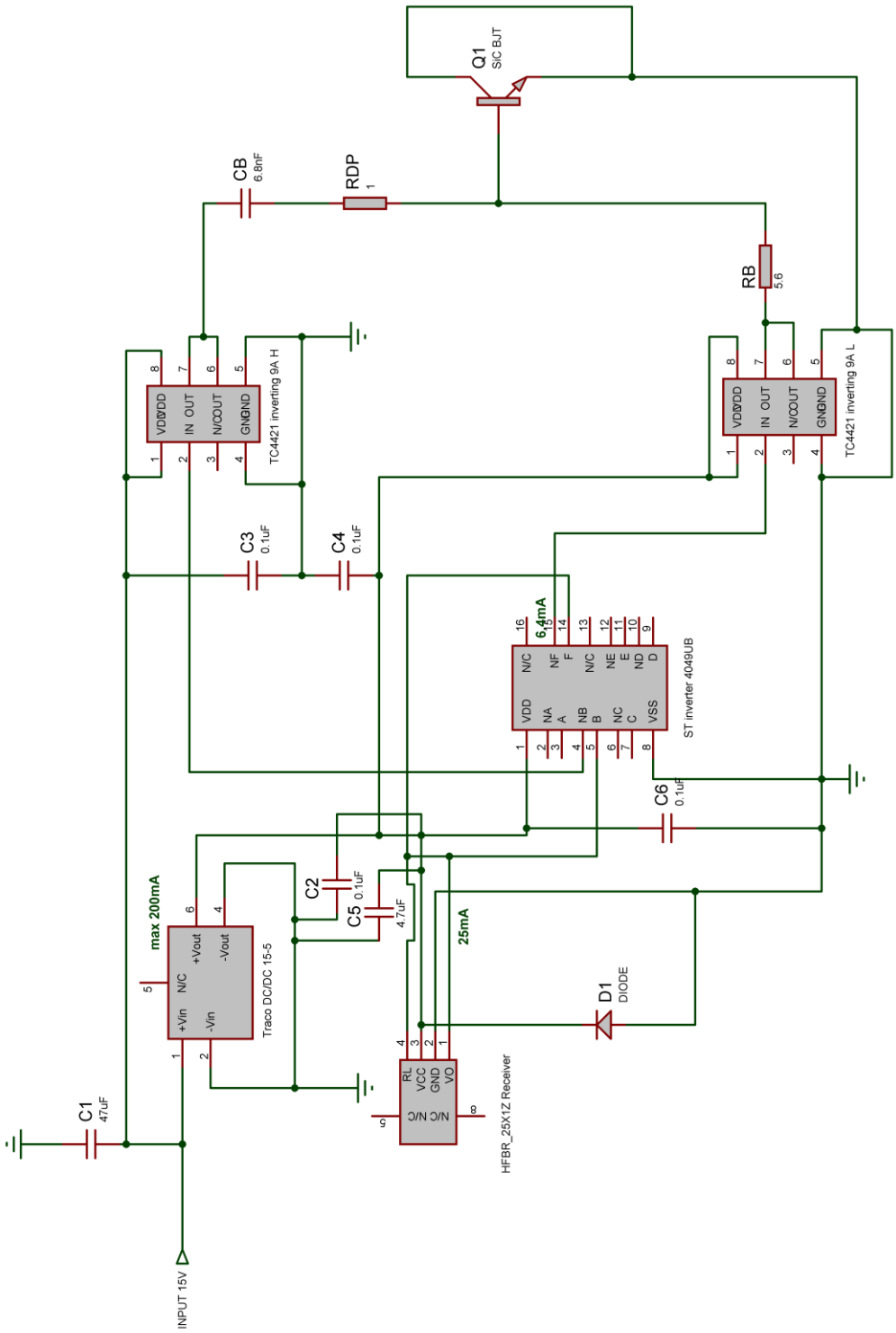
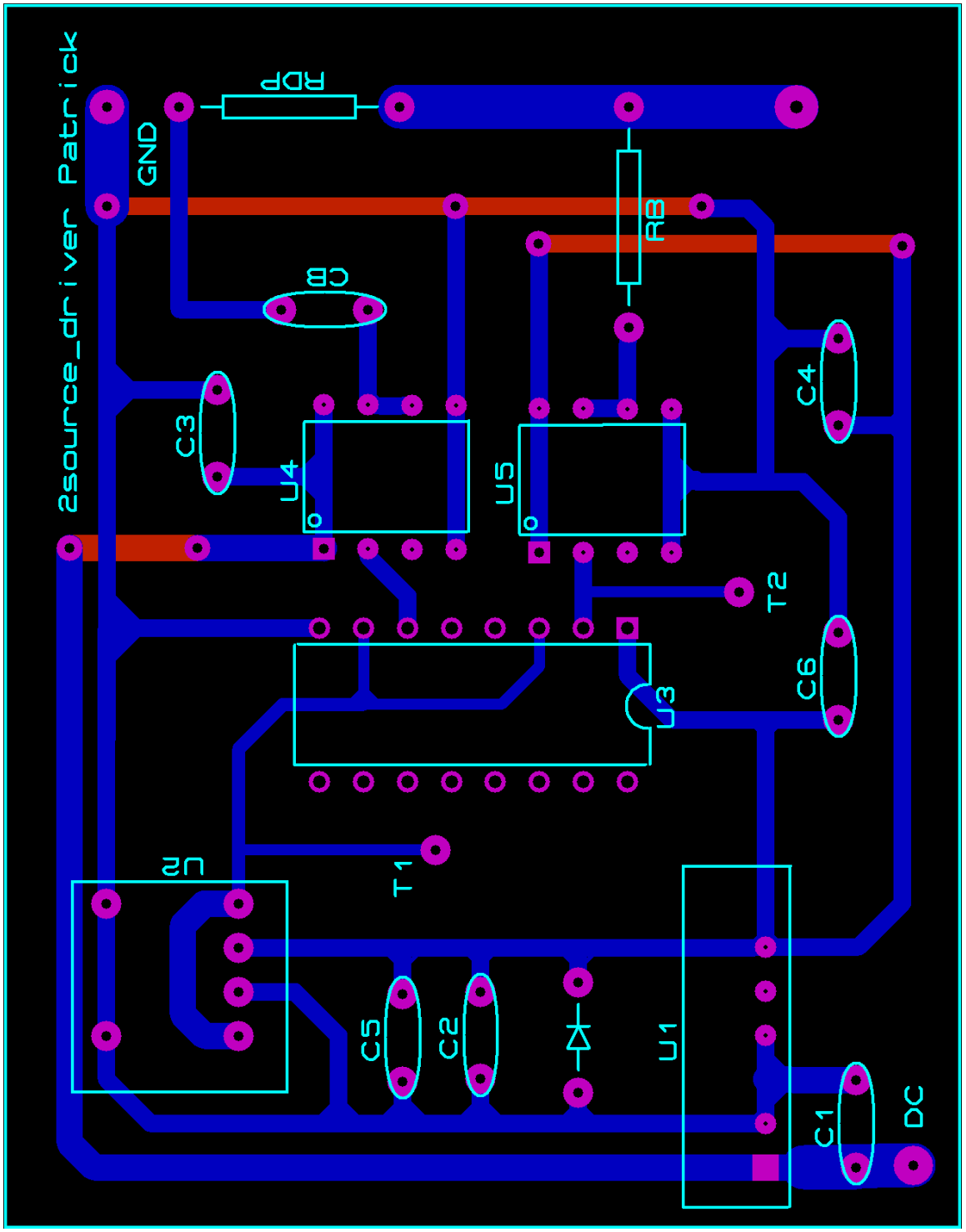
[115] EPCOS, "Ferrites and accessories: ETD 59/31/22 Core and accessories," datasheet, 2006.
[116] EPCOS, "Ferrites and accessories: SIFERRIT material N87," datasheet, 2006.
[117] TI, "Section 2 Magnetic Core Characteristics," the training material.
[118] TI, "Section 5 Inductor and Flyback," the training material.
[119] TI, "Section 3: Windings," the training material.
[120] Xilinx, "Xilinx ISE Design Suite 13.4 Manuscript."

8 Appendix List

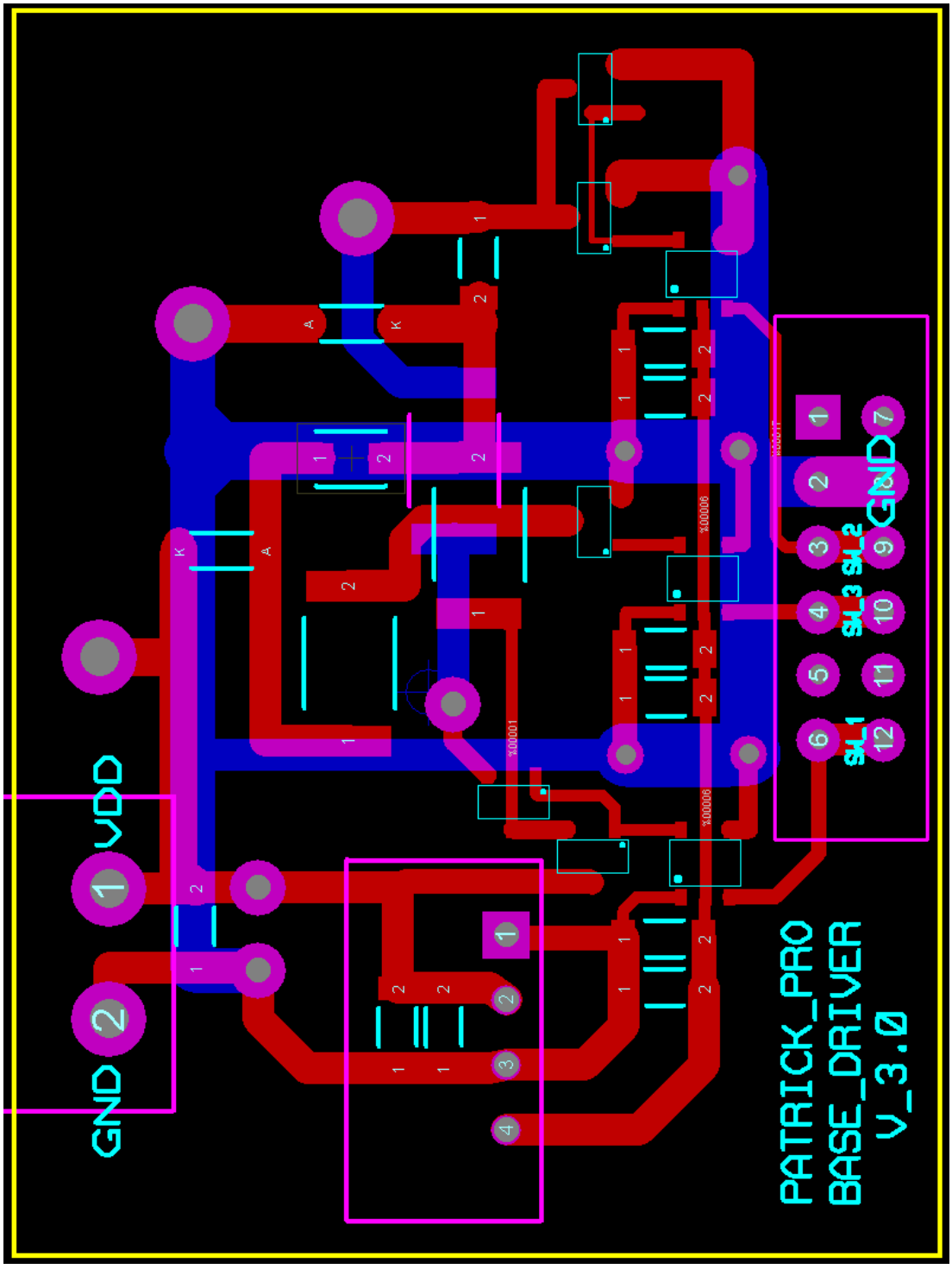
Appendix 8-1 Schematic design for a Dual-source DC power supply base driver



Appendix 8-2 Printed Circuit Board design for Dual-source DC power supply base driver



Appendix 8-3 Energy recovery concept validation board design of the base driver



Appendix 8-4 Coding for the boost converter using the energy recovery driver

Coding for the control signals of the boost converter using the energy recovery base driver from FPGA:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;
library UNISIM;
use UNISIM.VComponents.all;
entity frequency_sel is
port(
    clk,reset: in std_logic;
     switch   : in std_logic_vector(2 downto 0);
     sw_1,sw_2,sw_3 : out std_logic);
end frequency_sel;
architecture Behavioral of frequency_sel is
signal sw11,sw21,sw31,sw12,sw22,sw32,sw13,sw23,sw33,sw14,sw24,sw34,
sw15,sw25,sw35,sw16,sw26,sw36,sw17,sw27,sw37,sw18,sw28,sw38          :std_logic;
begin
generation_unit1:  entity work.frequency_gen
                    generic map(N=>250)
                    port map (clk=>clk, reset=>reset, sw1=>sw11, sw2=>sw21, sw3=>sw31);
generation_unit2:  entity work.frequency_gen
                   generic map(N=>300)
                    port map (clk=>clk, reset=>reset, sw1=>sw12, sw2=>sw22, sw3=>sw32);
generation_unit3: entity work.frequency_gen
                   generic map(N=>350)
                   port map (clk=>clk, reset=>reset, sw1=>sw13, sw2=>sw23, sw3=>sw33);
generation_unit4: entity work.frequency_gen
                   generic map(N=>400)
```

```
                        port map (clk=>clk, reset=>reset, sw1=>sw14, sw2=>sw24, sw3=>sw34);
generation_unit5: entity work.frequency_gen
                        generic map(N=>500)
                        port map (clk=>clk, reset=>reset, sw1=>sw15, sw2=>sw25, sw3=>sw35);
generation_unit6: entity work.frequency_gen
                        generic map(N=>550)
                        port map (clk=>clk, reset=>reset, sw1=>sw16, sw2=>sw26, sw3=>sw36);
generation_unit7: entity work.frequency_gen
                        generic map(N=>800)
                        port map (clk=>clk, reset=>reset, sw1=>sw17, sw2=>sw27, sw3=>sw37);
generation_unit8: entity work.frequency_gen
                        generic map(N=>200)
                        port map (clk=>clk, reset=>reset, sw1=>sw18, sw2=>sw28, sw3=>sw38);
process (clk,reset)
begin
 if reset='1' then
            sw_1<='0';
            sw_2<='0';
            sw_3<='0';
 elsif (clk'event and clk='1') then
    case switch is
        when "001" =>
            sw_1<=sw11;
            sw_2<=sw21;
            sw_3<=sw31;
         when "010" =>
            sw_1<=sw12;
            sw_2<=sw22;
            sw_3<=sw32;
```

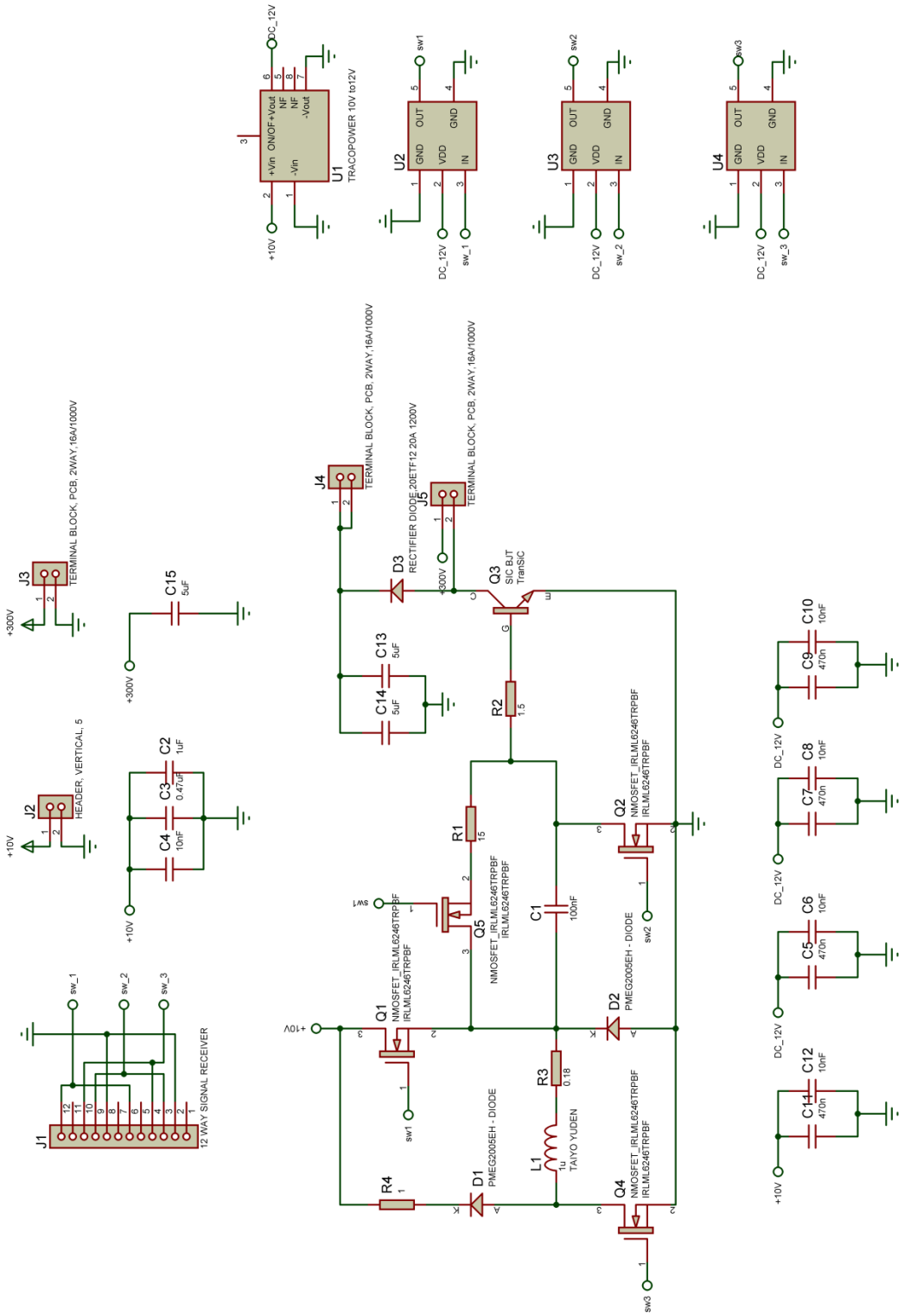
```
when "011" =>
    sw_1<=sw13;
    sw_2<=sw23;
    sw_3<=sw33;
 when "100" =>
    sw_1<=sw14;
    sw_2<=sw24;
    sw_3<=sw34;
when "101" =>
    sw_1<=sw15;
    sw_2<=sw25;
    sw_3<=sw35;
when "110" =>
    sw_1<=sw16;
    sw_2<=sw26;
    sw_3<=sw36;
when "111" =>
    sw_1<=sw17;
    sw_2<=sw27;
    sw_3<=sw37;
when "000" =>
    sw_1<=sw18;
    sw_2<=sw28;
    sw_3<=sw38;
  when others =>
    sw_1<='0';
    sw_2<='0';
    sw_3<='0';
                        end case;
```

```
end if;
end process;
end Behavioral;
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;
entity frequency_gen is
generic(N:integer:=500);
port(
      clk,reset: in std_logic;
      sw1,sw2,sw3: out std_logic);
end frequency_gen;
architecture Behavioral of frequency_gen is
begin
process(clk,reset)
variable contsw1a :integer range 0 to (2*N/5)-2:=(2*N/5)-2;
variable contsw1b :integer range 0 to (3*N/5)+1:=(3*N/5)+1;
variable delaysw1 :integer range 0 to 1:=1;
begin
if reset='1' then
 contsw1a:=(2*N/5)-2;
 contsw1b:=(3*N/5)+1;
 sw1<='0';
 delaysw1:=1;
elsif (clk'event and clk='1') then
 if delaysw1 /= 0 then
        sw1<='0';
                              delaysw1:=delaysw1-1;
    elsif contsw1a /= 0 then
```

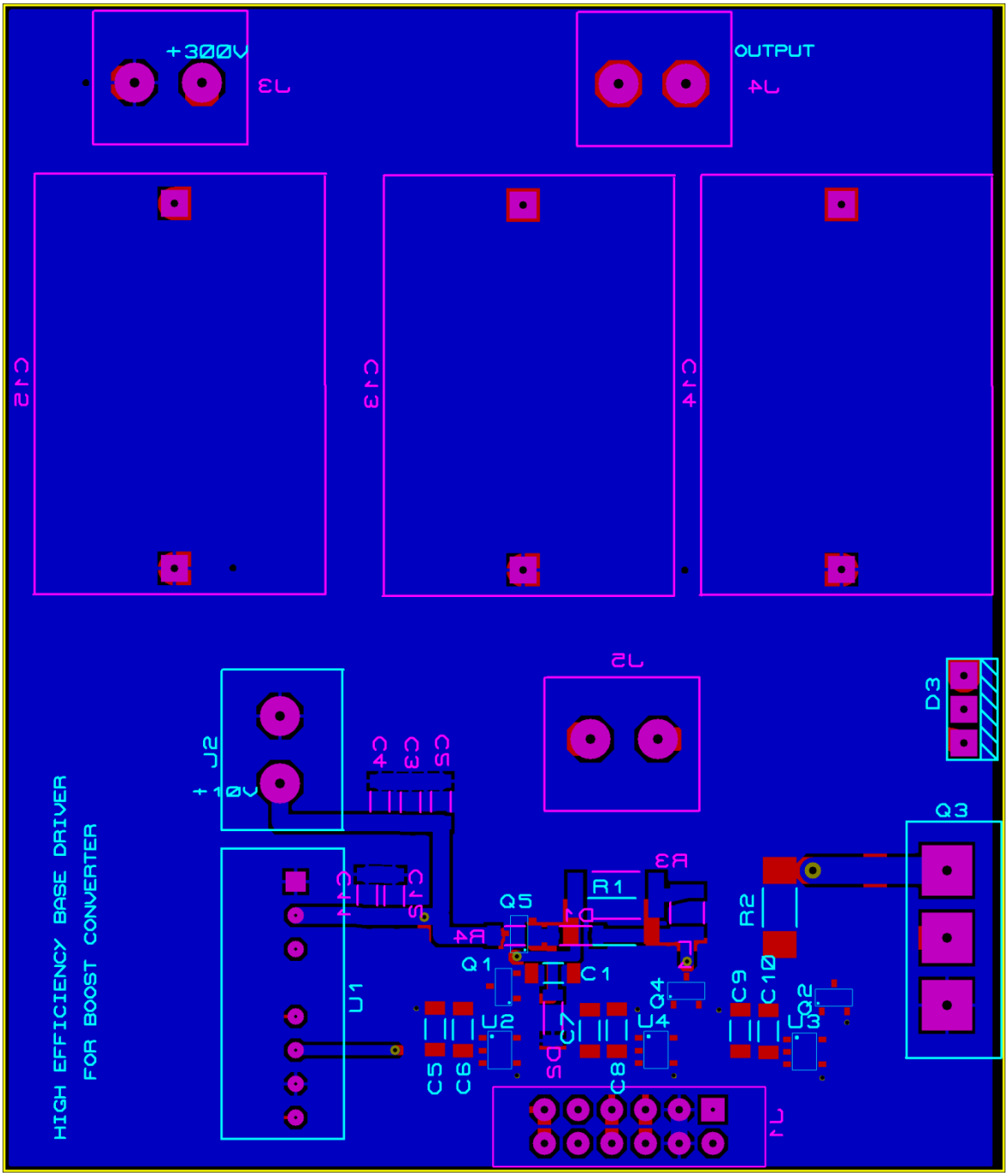
```
   sw1<='1';
            contsw1a:=contsw1a-1;
            elsif contsw1b /= 0 then
            sw1<='0';
            contsw1b:=contsw1b-1;
            else contsw1a:=(2*N/5)-2;
        contsw1b:=(3*N/5)+1;
end if;
end if;
end process;
process(clk,reset)
variable contsw2a  :integer range 0 to 2*N/5:=2*N/5;
variable contsw2b  :integer range 0 to (3*N/5)-1:=(3*N/5)-1;
begin
if reset='1' then
 contsw2a:=2*N/5;
 contsw2b:=(3*N/5)-1;
sw2<='0';
elsif (clk'event and clk='1') then
           if contsw2a /= 0 then
            sw2<='0';
            contsw2a:=contsw2a-1;
            elsif contsw2b /= 0 then
            sw2<='1';
            contsw2b:=contsw2b-1;
                    else contsw2a:=2*N/5;
        contsw2b:=(3*N/5)-1;
end if;
end if;
```

```
end process;
 process(clk,reset)
variable delaysw3 :integer range 0 to 2*N/5:=2*N/5;
variable contsw3a  :integer range 0 to 25:=25;
variable contsw3b  :integer range 0 to N-26:=N-26;
begin
if reset='1' then
 contsw3a:=25;
 contsw3b:=N-26;
 delaysw3:=2*N/5;
 sw3<='0';
elsif (clk'event and clk='1') then
 if delaysw3 /= 0 then
        sw3<='0';
           delaysw3:=delaysw3-1;
            elsif contsw3a /= 0 then
            sw3<='1';
            contsw3a:=contsw3a-1;
            elsif contsw3b /= 0 then
            sw3<='0';
            contsw3b:=contsw3b-1;
            else contsw3a:=25;
        contsw3b:=N-26;
end if;
end if;
end process;
end Behavioral;
```

Appendix 8-5 The schematic design of the boost converter with energy recovery base driver



Appendix 8-6 The PCB drawing of the boost converter with the energy recovery base driver



Appendix 8-7 12A maximum current rating inductor design process and specifications

The design requirements for the power inductor in the boost converter are defined as following:

Inductance L: 0.3 mH

Peak current I_{peak} =12A

Max. current ripple I_r =4A

Average current I_{av} =6A

The core is selected depending on the material and air gap length. Tentatively ETD59 (E shape) [115] is used with SIFERRIT material N87 (base material is MnZn) [116] from EPCOS. The critical specific parameters are listed as following:

Air gap area A_e: 368 mm^2

Air gap length l_g: 1.5 mm

Window area A_n: 365.6 mm^2

Max. material flux density B_{Max} =390 mT (@100°C)

In the calculation, the maximum flux density is chosen to be 300 mT making sure it works in the linear region in B-H plot. Assuming the core is saturation limited, the maximum swing flux density B_s is obtained by:

$$B_s = B_{Max}\frac{I_r}{I_{peak}} = 0.1\ T \quad \textbf{8-1}$$

Looking up for core loss at 50 mT flux in the datasheet [116] in P_v—B plot, the relative core losses P_v is less than rule of thumb 100 mW/cm^3 under the convention cooling in nature [117, 118]. So the core is not limited by core loss. The number of turns N is calculated by Equation **8-2**.

$$N = \frac{LI_r}{A_e B_s} = 33 \quad \textbf{8-2}$$

To achieve the inductance required, the air gap length needs to be calculated as in Equation 8-3 with N from Equation **8-2**.

$$l_g = \frac{u_0 A_e N^2}{L} = 1.64\ mm \quad \textbf{8-3}$$

u_0 is commonly called the vacuum permeability which is $4\pi \cdot 10^{-7}$ H/m. The required gap length from 8-3 is very near to the physical value of ETD59 N87 core.

The maximum copper wire area is estimated according to the experience by Equation 8-4.

$$A_{Max} = \frac{0.4 A_n}{N} = 4.483\ mm^3 \quad \textbf{8-4}$$

So the maximum diameter of the wire is D_{Max} =2.389 mm.

The switching frequency for the boost converter is adjustable in the experiment from 63 kHz to 250 kHz. At a high ac frequency put through the inductor, the skin effect on the winding wires will happen. The ac current density is much higher on the conductor surface than that inside causing the power loss increase. The penetration depth D_{dep} into the conductor can be calculated in Equation **8-5** for copper at 111 kHz and 100°C [119].

$$D_{dep} = \frac{7.6}{\sqrt{f}} = 0.23\ mm \quad \textbf{8-5}$$

Therefore, the diameter of the wire needs to be reduced for low power dissipation on copper. Due to the usage of multiple strands of wires in parallel, the copper loss and the current density on each strand decrease. Each strand diameter is 0.28 mm selected in the lab. So the number of the strands N_s is obtained:

$$N_s = \frac{D_{Max}}{0.28} = 68 \quad \textbf{8-6}$$

Accordingly, the current density in each strand is reasonable in engineering:

$$J = \frac{I_{av}}{N_s \pi (\frac{0.23}{2})^2} = 2.1\ A/mm^2 \quad \textbf{8-7}$$

The picture of the wound inductor is shown in Figure 8-1 and measured by LCR tester in Figure 8-2.

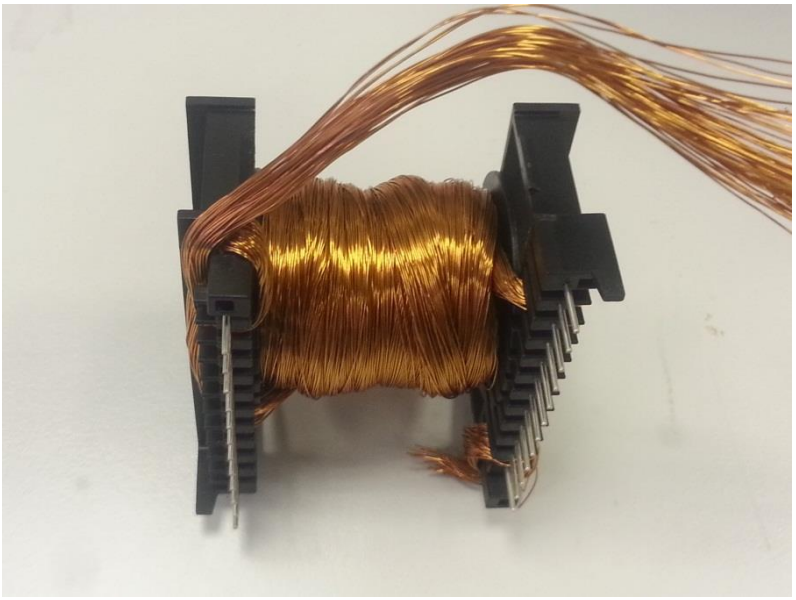


Figure 8-1 Wound inductor

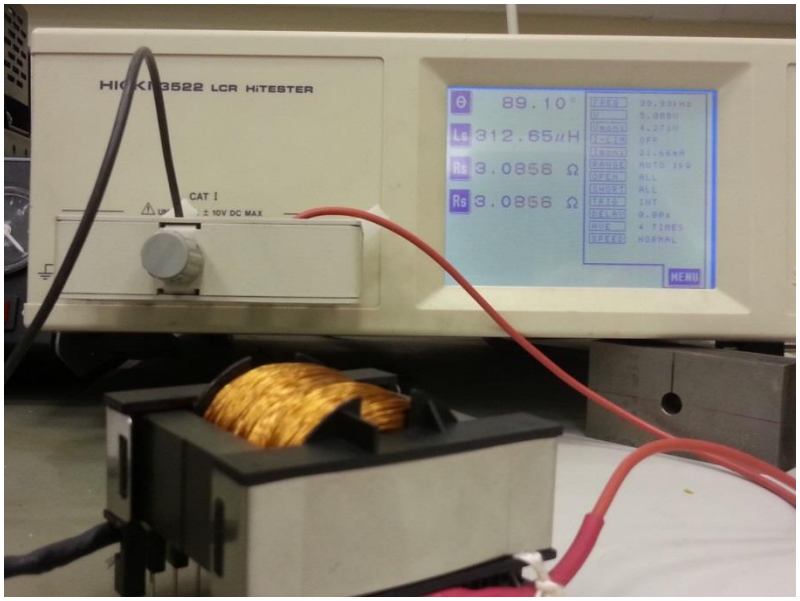


Figure 8-2 Measurement results for inductor with the accessories

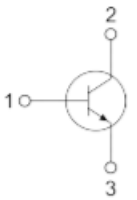
Appendix 8-8 BitSiC BT1220AB-P1

BitSiC BT1220AB-P1

The BitSiC1206 is a 20 A power transistor developed and manufactured for high temperature operation. These NPN bipolar junction transistors made of Silicon Carbide utilizes the latest BitSiC-technology developed by TranSiC. This transistor is ideally suited for switched power applications as the BitSiC offer very low on state losses along with a distinctly low temperature dependent fast switching characteristic.

V_{CEO}	1200V
$T_{j(max)}$	+250ºC
$V_{CE(SAT)}$	1V (20A, 250ºC)
$R_{ON(SAT)}$	50mΩ (250ºC)

TranSiC's BitSiC is inherently resistant to radiation and short circuit and lacks the troublesome secondary breakdown. Power and control electronics can now be designed for temperatures up to +250ºC. This new technology opens up a new field of high voltage applications operated at high ambient temperatures for example within demanding industries such as Oil and Gas and Aerospace.



Features

- High operating junction temperature 250ºC
- Fast and temperature independent switching
- Wide reverse bias SOA
- Excellent capability to withstand short-circuit.
- Excellent immunity to cosmic rays

Typical applications:

- High temperature DC/DC converters
- High temperature AC/DC inverters
- High temperature Motor drives
- High temperature actuator controls

Maximum ratings, at T = 25°C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Collector-Emitter Voltage	V_{CEO}		1200	V
Emitter-Collector Voltage	V_{EC}		30	
Collector-Base Voltage	V_{CBO}		1200	
Emitter-Base Voltage	V_{EBO}		30	
Collector current	I_C	DC	20	A
	I_{CM}	t_P < 10 ms	40	
	I_{CP}	non rep. t_P < 300 µs	-	
Base current	I_B	DC	3	
	I_{BM}	t_P < 10 ms	6	
	I_{BM}	non rep. t_P < 300 µs	-	
Storage temperature	T_{stg}		-55 to 100	ºC
Operating junction temperature	T_j		250	
Maximum power dissipation	P_{TOT}	TO-258, T_c = 25ºC	-	W
Mounting torque		TO-258, M4 Screw	-	Ncm

Electrical characteristics, at Tj = 25°C, unless otherwise specified

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Collector cut-off current	I_{CEO}	Open base T_J = 25°C V_{CE} = 600 V V_{CE} = 1200 V T_J = 150°C V_{CE} = 600 V V_{CE} = 1200 V		 - - - -		nA
DC Current gain	h_{FE}	Pulse duration = 300 µs V_{CE} = 2.5 V T_J = 25°C I_C = 3 A I_C = 20 A T_J = 150°C I_C = 3 A I_C = 20 A		 20 50 15 35		
Collector-Emitter saturation Voltage	$V_{CE(SAT)}$	Pulse duration = 300 µs I_C = 20 A , I_B = 2 A T_J = 25°C T_J = 150°C T_J=250°C		 0.5 0.75 1.0		V
Collector-Emitter on-state resistance	$R_{ON(SAT)}$	Pulse duration = 300 µs I_C = 6 A , I_B = 600 mA T_J = 25°C T_J = 150°C T_J = 250°C		 25 38 50		mΩ
Base-Emitter saturation voltage	$V_{BE(SAT)}$	Pulse duration = 300 µs I_C = 20 A I_B = 2 A T_J = 25°C T_J = 150°C T_J = 250°C		 3.25 3 2.9		V

Dynamic characteristics, at Tj = 25°C, f = 100kHz, unless otherwise specified

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Base-Collector capacitance	C_{BC}	V_{CB} = 0 V V_{CB} = 40 V V_{CB} = 1200 V		2500 650		pF
Base-Emitter capacitance	C_{BE}	V_{BE}=0 V V_{BE}=3.2 V		6 16		nF
Collector-Emitter capacitance	C_{CE}			- - -		pF
Base-Collector charge	Q_{BC}	V_{CB}=800 V		230		nC
Base-Emitter charge	Q_{BE}	V_{BE}=3.2 V		22		
Total Base charge	Q_{BTOT}					
Collector-Emitter charge	Q_{BE}			-		

Thermal characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Thermal resistance junction - case	R_{thJC}	TO-258 Isolated		1.0		°K/W
Thermal resistance junction - ambient	R_{thJA}	TO-258 Isolated		-		
Thermal resistance junction - pin	R_{thJP}	TO-258 Isolated		-		

Switching characteristics, Inductive load, Tj = 25°C

Parameter	Symbol	Conditions [1]	Typ	
Turn-on delay time	$t_{d(on)}$	V_{CE} = 800V, I_{CE} = 20A, I_{BE} on and off = 6A T_j = 25°C	8	ns
Turn-on voltage fall time	t_f		28	
Turn-off delay time	$t_{D(OFF)}$		10	
Turn-off voltage rise time	t_r		19	
Turn on energy	E_{ON}		310	µJ
Turn off energy	E_{OFF}		147	
Total switching energy	E_{TS}		457	
Turn-on delay time	$t_{d(on)}$	V_{CE} = 800V, I_{CE} = 20A, I_{BE} on and off = 6A T_j = 250°C	8	ns
Turn-on voltage fall time	t_f		32	
Turn-off delay time	$t_{D(OFF)}$		24	
Turn-off voltage rise time	t_r		20	
Turn on energy	E_{ON}		330	µJ
Turn off energy	E_{OFF}		158	
Total switching energy	E_{TS}		488	

[1] Switch wave forms and energies were measured using a double pulse setup. Three parallel 8A silicon carbide schottky diodes, Infineon IDH08S120, were used as free wheeling diode. Please see figures A-B and the application note TSC-TR005 BitSiC Charateristics for details and circuit schematics. Driver passive values used, R1 1Ω, C1 44nF, R2 17Ω.

Application support

The development of application support documents for the BitSiC transistors is an continuously on going process. Currently available are application notes describing a simple driver circuit and the switching behaviour of the transistors. There is also a SPICE model of the transistor available. Please contacts us to receive more information on this topic.

Typical performance curves

Measurements performed under pulsed condition tp= 300 µs and at T = 25 ºC unless otherwise specified.

Figure 1, I-V Characteristics 25°C

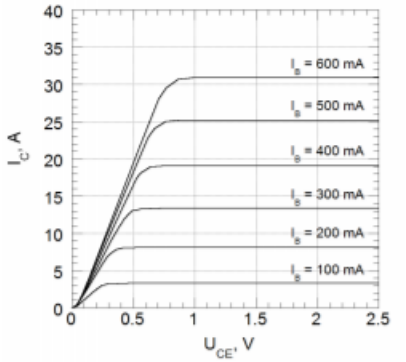


Figure 2, I-V Characteristics 150°C

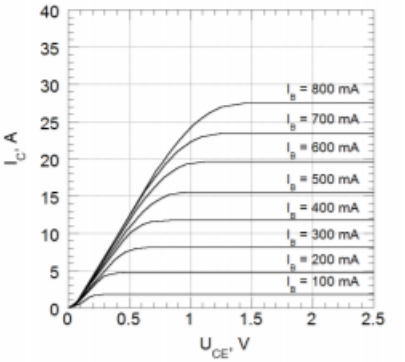


Figure 3, I-V Characteristics 250°C

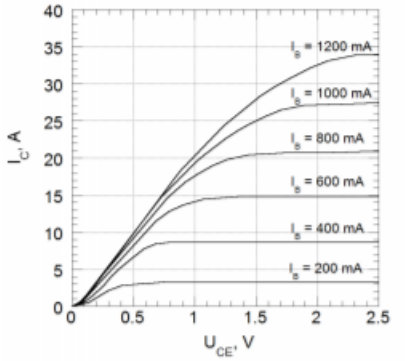


Figure 4, $U_{BE(SAT)}$ - T_j

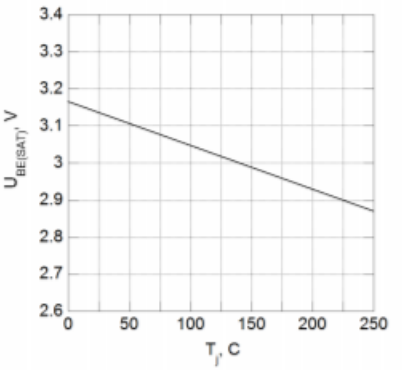


Figure 5, $U_{BE(SAT)}$ - I_C

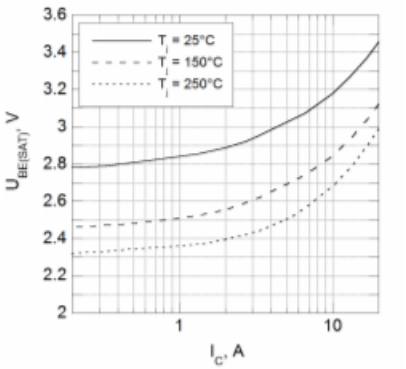
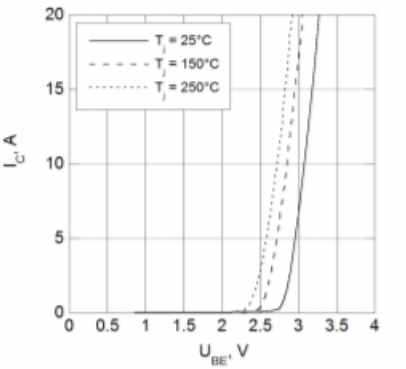


Figure 6, I_C - U_{BE}



Typical performance curves

Measurements performed under pulsed condition tp= 300 µs and at T = 25 ºC unless otherwise specified.

Figure 7, $U_{CE(SAT)}$ - I_C

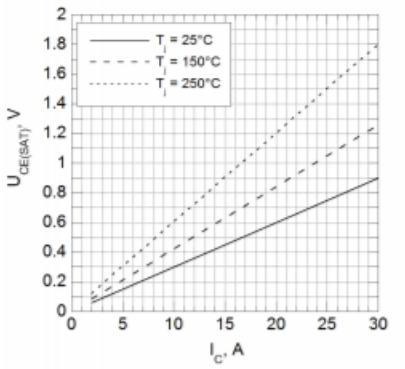


Figure 8, $U_{CE(SAT)}$ - T_j @ I_C = 20A

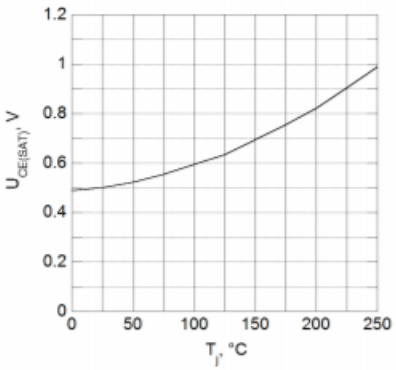


Figure 9, h_{FE} - I_C

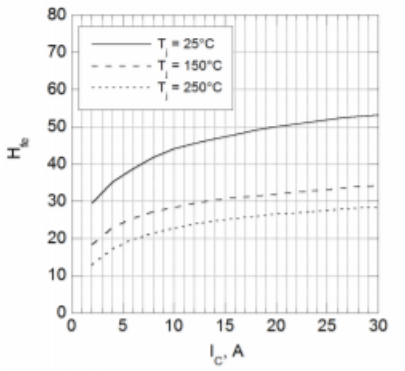


Figure 10, h_{FE} - T_j @ I_C = 20A

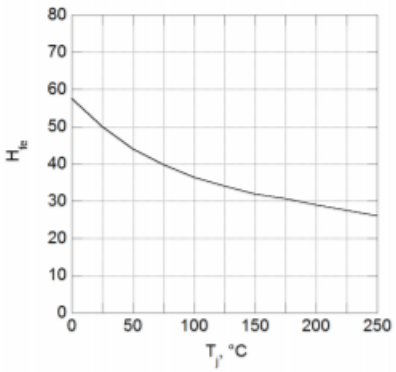


Figure 11, h_{FE} - I_C (Low currents)

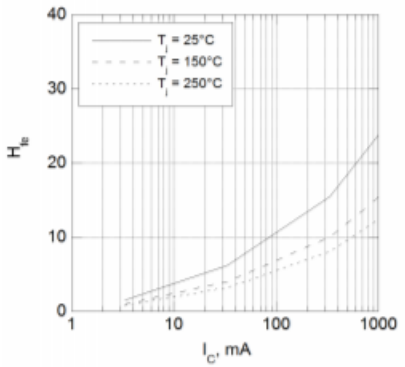
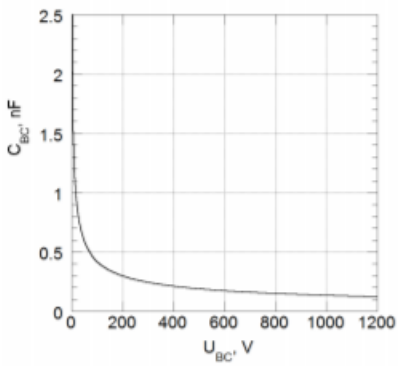


Figure 12, C_{BC} - U_{BC}



Typical performance curves

Measurements performed under pulsed condition tp= 300 µs and at T = 25 ºC unless otherwise specified.

Figure 13, Q_{BC} - U_{BC}

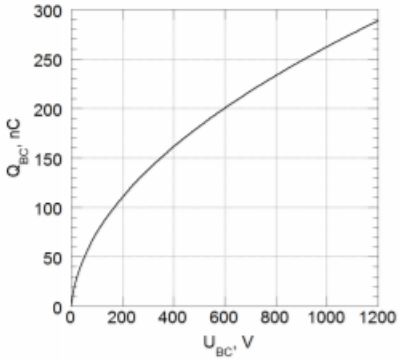


Figure 14, E_{ON} - I_C @ U_{DC} = 800V

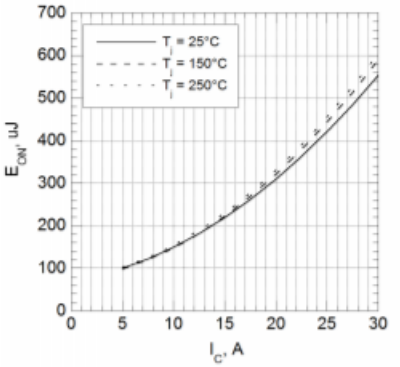


Figure 15, E_{OFF} - I_C @ U_{DC} = 800V

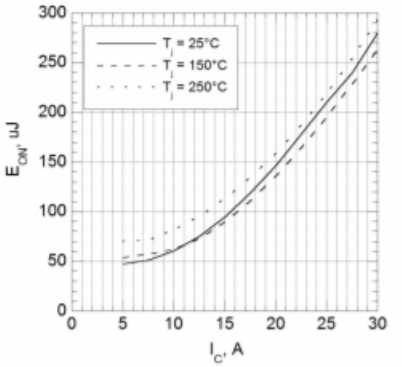


Figure 16, Turn-on @ U_{DC} = 800V, I_C = 20A, T_j = 250°C

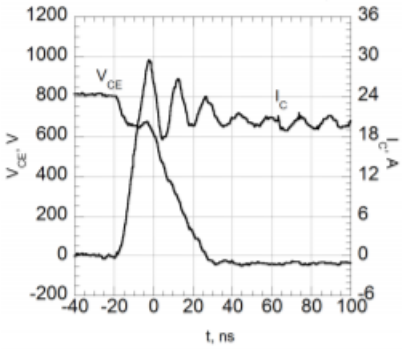
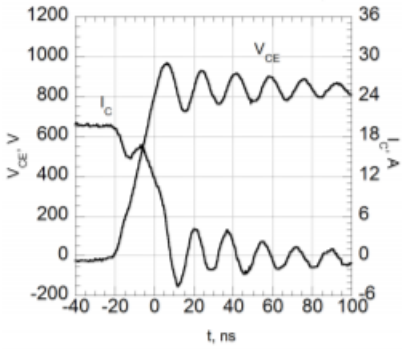


Figure 17, Turn-off @ U_{DC} = 800V, I_C = 20A, T_j = 250°C



Schematics

Figure A, Switch circuit schematic

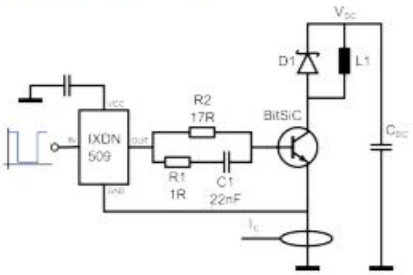
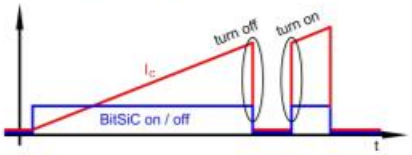
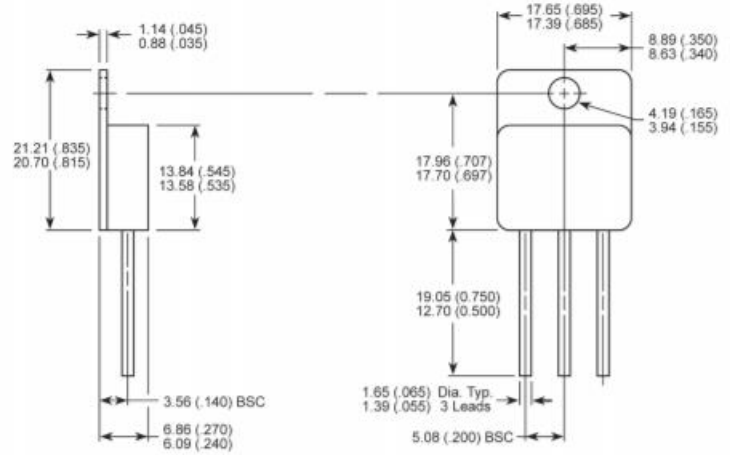


Figure B, Double pulse



TO-258 Isolated, outline and dimensions



Dimensions in Millimeters and (Inches)

Part numbering

Part number	Package
BT1220AB-P1	TO-258

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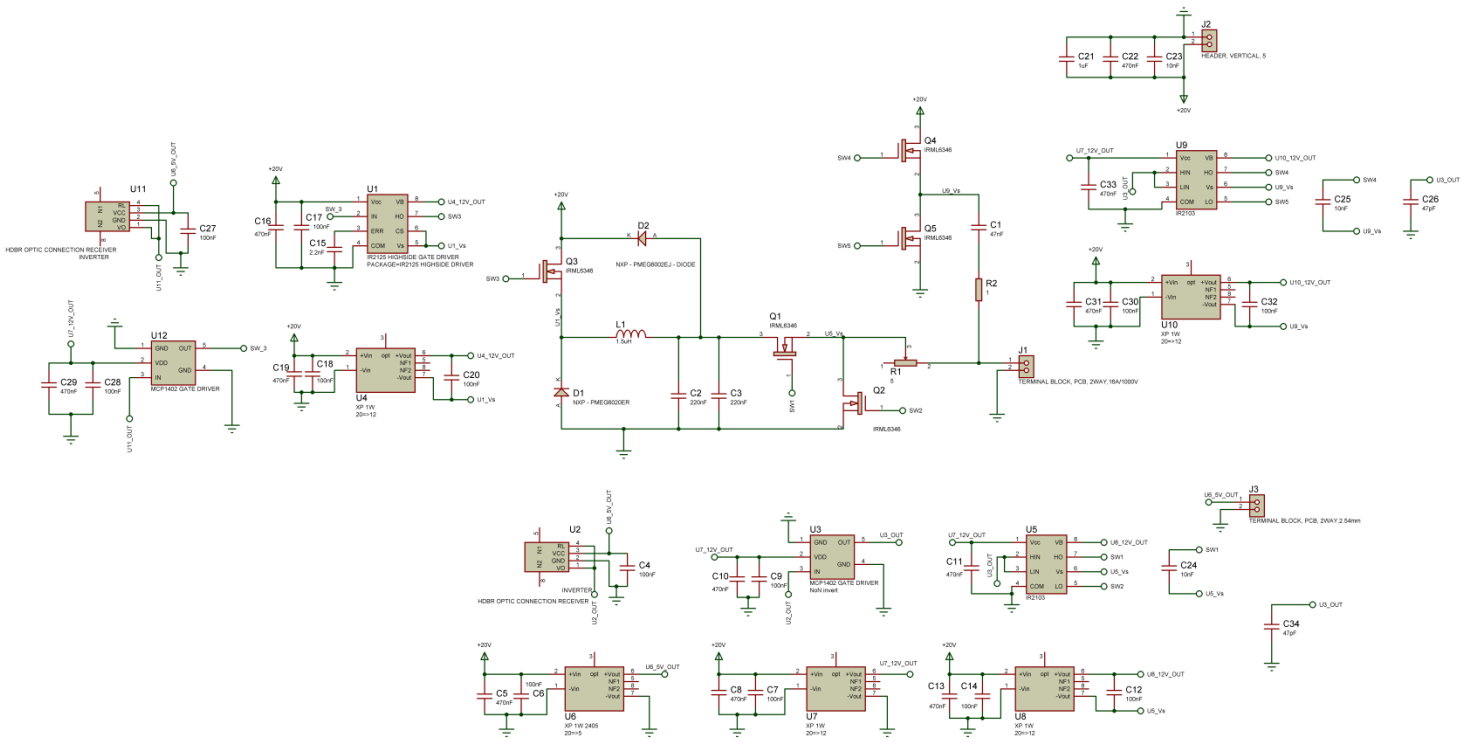
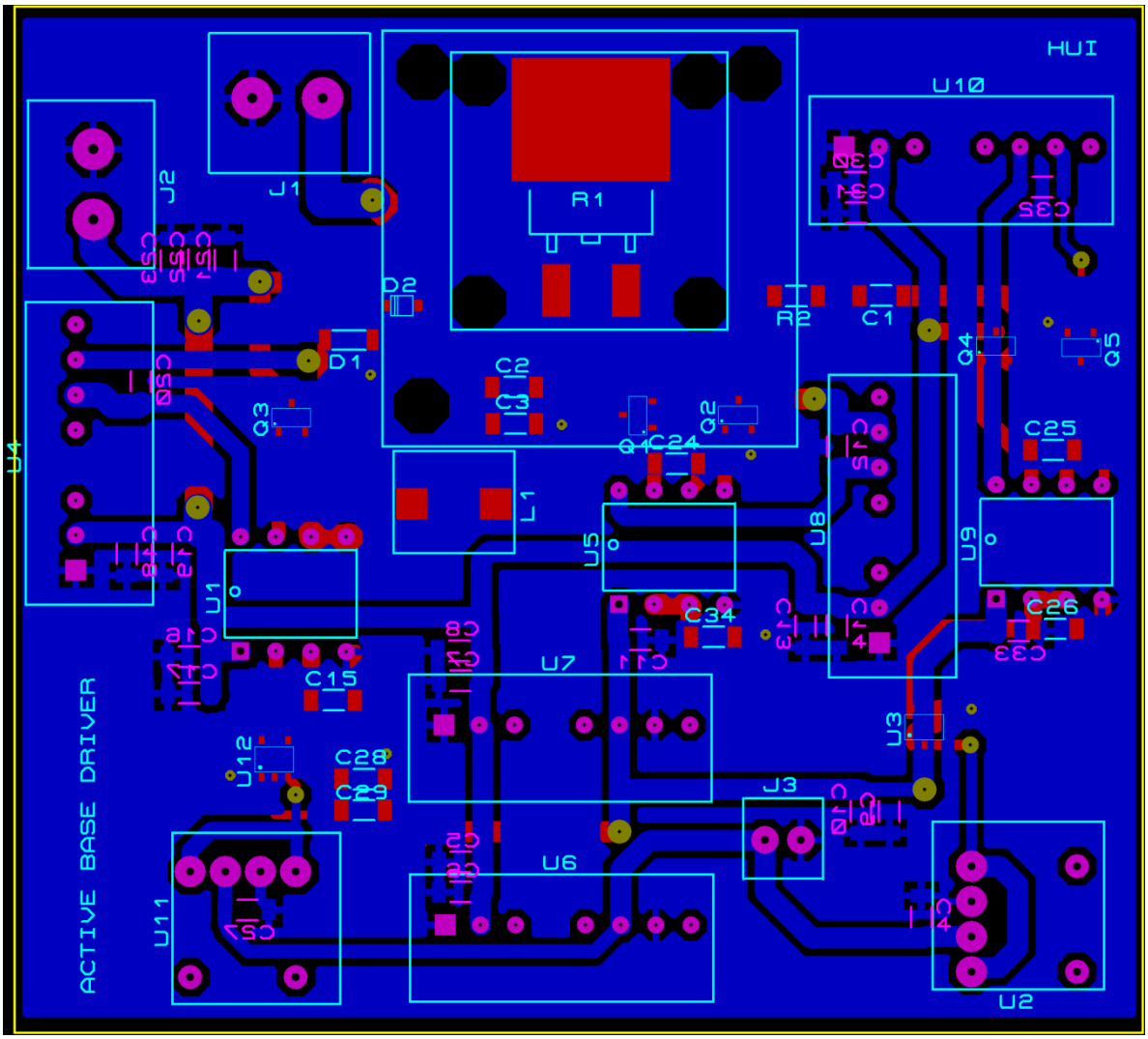
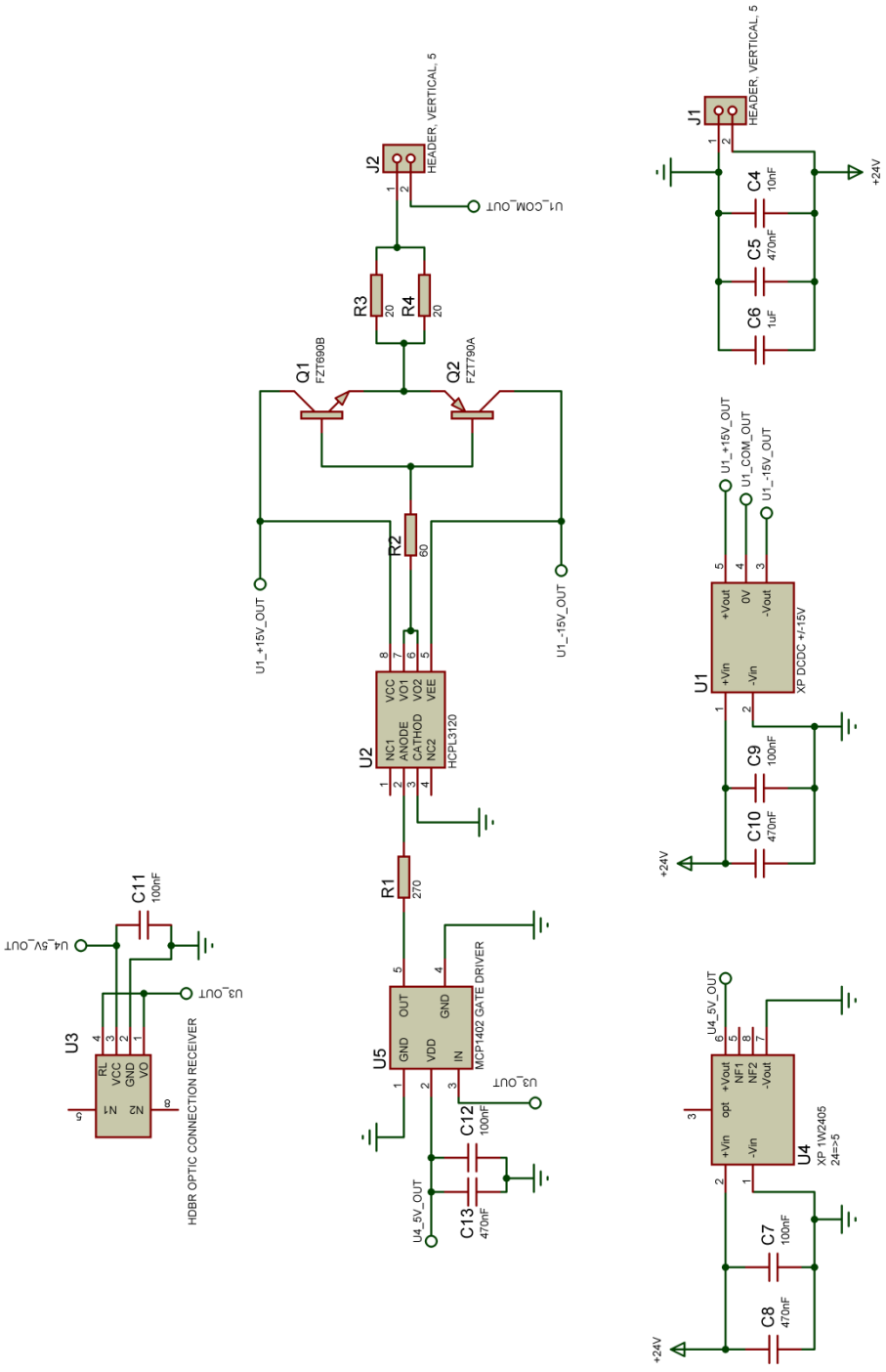
Appendix 8-9 The schematic design for the active base driver


U11
HDBR OPTIC CONNECTION RECEIVER
INVERTER
C27
100nF
U1
IR2125 HIGHSIDE GATE DRIVER
PACKAGE=IR2125 HIGHSIDE DRIVER
C16
470nF
C17
100nF
C15
2.2nF
U4_12V_OUT
SW3
U1_Vs
U12
MCP1402 GATE DRIVER
C29
470nF
C28
100nF
SW_3
U4
XP 1W
20=>12
C19
470nF
C18
100nF
C20
100nF
D2
NXP - PMEG6002EJ - DIODE
Q3
IRML6346
L1
1.0uH
D1
NXP - PMEG6020ER
C2
220nF
C3
220nF
Q1
IRML6346
Q4
IRML6346
Q5
IRML6346
SW4
SW5
U9_Vs
C1
47nF
R2
1
R1
5
J1
TERMINAL BLOCK, PCB, 2WAY, 16A/1000V
Q2
IRML6346
SW1
SW2
J2
HEADER, VERTICAL, 5
C21
1uF
C22
470nF
C23
10nF
U9
IR2103
C33
470nF
C25
10nF
C26
47pF
U10
XP 1W
20=>12
C31
470nF
C30
100nF
C32
100nF
U2
INVERTER
HDBR OPTIC CONNECTION RECEIVER
C4
100nF
U3
MCP1402 GATE DRIVER
NoN invert
C10
470nF
C9
100nF
U5
IR2103
C11
470nF
C24
10nF
J3
TERMINAL BLOCK, PCB, 2WAY, 2.54mm
C34
47pF
U6
XP 1W 2405
20=>5
C5
470nF
C6
100nF
U7
XP 1W
20=>12
C8
470nF
C7
100nF
U8
XP 1W
20=>12
C13
470nF
C14
100nF
C12
100nF

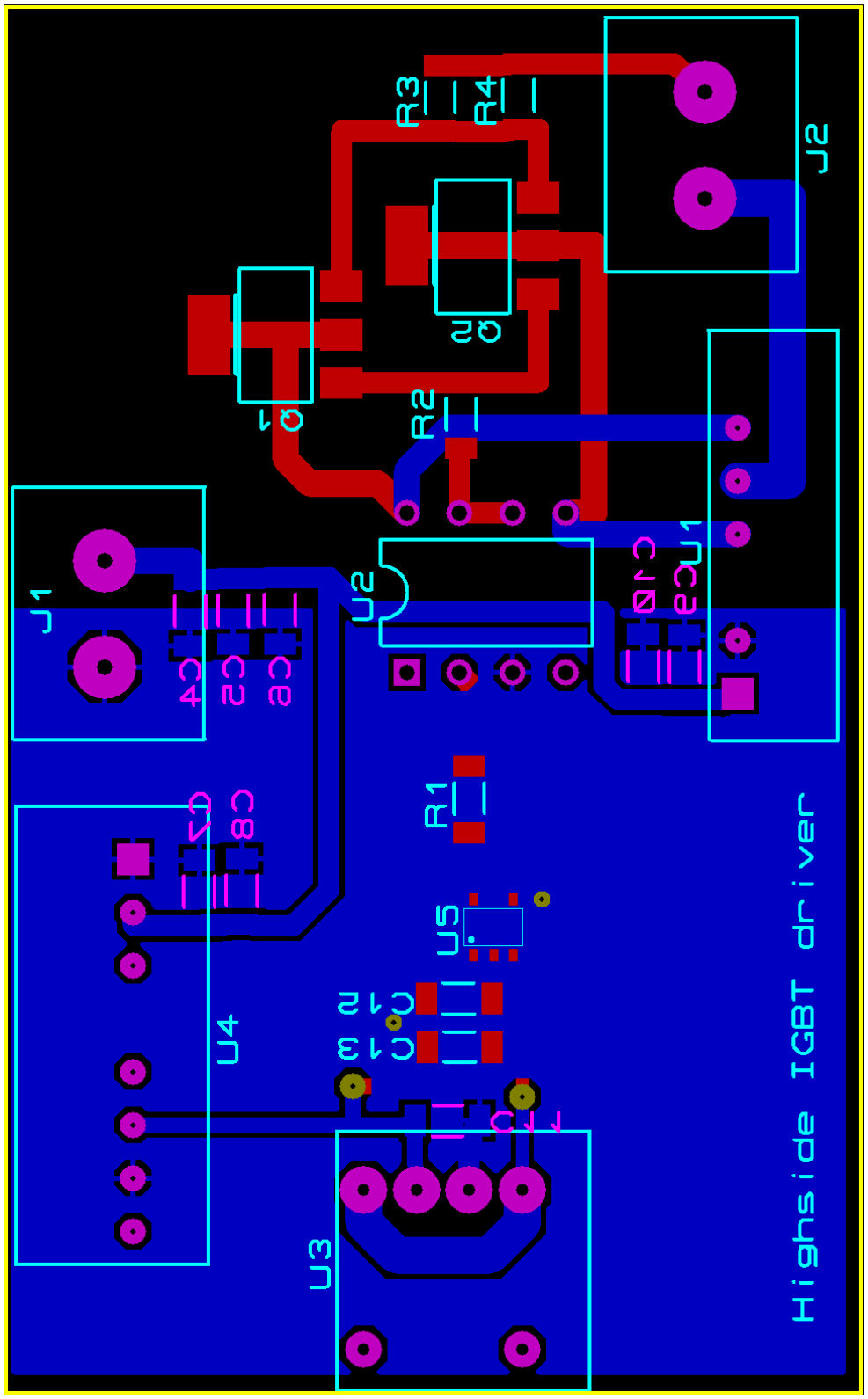
Appendix 8-10 The PCB drawing for the active base driver



Appendix 8-11 The schematic design for the high side Si IGBT Q2 gate driver



Appendix 8-12 The PCB layout design for the high side Si IGBT Q2 gate driver



Appendix 8-13 The code for FPGA generating control signals in Chapter 3

The code for FPGA generating control signals for heating process and switching test is listed as:

```
library IEEE;

use IEEE.STD_LOGIC_1164.ALL;

use IEEE.NUMERIC_STD.ALL;

library UNISIM;

use UNISIM.VComponents.all;

entity BJT_IGBT is

port(

clk,reset,reset_board: in std_logic;

switch   : in std_logic_vector(2 downto 0);

sw_3,O_sw_IGBT,O_sw_BJT : out std_logic);

end BJT_IGBT;

architecture Behavioral of BJT_IGBT is

signal sw31, sw32, sw33, sw34, sw35, sw36, sw37,sw30,sw_IGBT0,sw_IGBT1,sw_IGBT2,sw_IGBT3,sw_IGBT4,sw_IGBT5,sw_IGBT6, sw_IGBT7,

sw_BJT0,sw_BJT1,sw_BJT2,sw_BJT3,sw_BJT4,sw_BJT5,sw_BJT6,sw_BJT7,reset_o
        :std_logic;

begin

Debounce :entity work.debounce

port map (clk=>clk,reset=>reset_board,sw=>reset,db=>reset_o);

generation_unit0:  entity work.heating_control

generic map(N_IGBT=>0,

N_BJT_low1=>0,

N_BJT_high1=>3500,

N_BJT_low2=>500,

N_BJT_high2=>800,

N_sw3=>10,
```

N_heating_period=>0)

port map (clk=>clk, reset=>reset_o, sw3=>sw30,sw_IGBT=>sw_IGBT0,sw_BJT=>sw_BJT0);

generation_unit1: entity work.heating_control

generic map(N_IGBT=>0,

N_BJT_low1=>0,

N_BJT_high1=>3500,

N_BJT_low2=>500,

N_BJT_high2=>800,

N_sw3=>12,

N_heating_period=>0)

port map (clk=>clk, reset=>reset_o, sw3=>sw31,sw_IGBT=>sw_IGBT1,sw_BJT=>sw_BJT1);

generation_unit2: entity work.heating_control

generic map(N_IGBT=>0,

N_BJT_low1=>0,

N_BJT_high1=>3500,

N_BJT_low2=>500,

N_BJT_high2=>800,

N_sw3=>15,

N_heating_period=>0)

port map (clk=>clk, reset=>reset_o, sw3=>sw32,sw_IGBT=>sw_IGBT2,sw_BJT=>sw_BJT2);

generation_unit3: entity work.heating_control

generic map(N_IGBT=>0,

N_BJT_low1=>0,

N_BJT_high1=>3500,

N_BJT_low2=>500,

N_BJT_high2=>800,

N_sw3=>18,

N_heating_period=>0)

```
port map (clk=>clk, reset=>reset_o, sw3=>sw33,sw_IGBT=>sw_IGBT3,sw_BJT=>sw_BJT3);

generation_unit4: entity work.heating_control

generic map(N_IGBT=>0,

N_BJT_low1=>0,

N_BJT_high1=>3500,

N_BJT_low2=>500,

N_BJT_high2=>800,

N_sw3=>23,

N_heating_period=>0)

port map (clk=>clk, reset=>reset_o, sw3=>sw34,sw_IGBT=>sw_IGBT4,sw_BJT=>sw_BJT4);

generation_unit5: entity work.heating_control

generic map(N_IGBT=>0,

N_BJT_low1=>0,

N_BJT_high1=>3500,

N_BJT_low2=>500,

N_BJT_high2=>800,

N_sw3=>26,

N_heating_period=>0)

port map (clk=>clk, reset=>reset_o, sw3=>sw35,sw_IGBT=>sw_IGBT5,sw_BJT=>sw_BJT5);

generation_unit6: entity work.heating_control

generic map(N_IGBT=>0,

N_BJT_low1=>0,

N_BJT_high1=>3500,

N_BJT_low2=>500,

N_BJT_high2=>800,

N_sw3=>30,

N_heating_period=>0)
```

```
port map (clk=>clk, reset=>reset_o, sw3=>sw36,sw_IGBT=>sw_IGBT6,sw_BJT=>sw_BJT6);

generation_unit7: entity work.heating_control

generic map(N_IGBT=>0,

N_BJT_low1=>0,

N_BJT_high1=>3500,

N_BJT_low2=>500,

N_BJT_high2=>800,

N_sw3=>35,

N_heating_period=>0 )

port map (clk=>clk, reset=>reset_o, sw3=>sw37,sw_IGBT=>sw_IGBT7,sw_BJT=>sw_BJT7);

process (clk,reset_o)

begin

if reset_o='1' then

O_sw_IGBT<='0';

O_sw_BJT<='0';

sw_3<='0';

elsif (clk'event and clk='1') then

case switch is

when "001" =>

O_sw_IGBT<=sw_IGBT1;

O_sw_BJT<=sw_BJT1;

sw_3<=sw31;

when "010" =>

O_sw_IGBT<=sw_IGBT2;

O_sw_BJT<=sw_BJT2;

sw_3<=sw32;

when "011" =>

O_sw_IGBT<=sw_IGBT3;
```

```
O_sw_BJT<=sw_BJT3;
sw_3<=sw33;
when "100" =>
O_sw_IGBT<=sw_IGBT4;
O_sw_BJT<=sw_BJT4;
sw_3<=sw34;
when "101" =>
O_sw_IGBT<=sw_IGBT5;
O_sw_BJT<=sw_BJT5;
sw_3<=sw35;
when "110" =>
O_sw_IGBT<=sw_IGBT6;
O_sw_BJT<=sw_BJT6;
sw_3<=sw36;
when "111" =>
O_sw_IGBT<=sw_IGBT7;
O_sw_BJT<=sw_BJT7;
sw_3<=sw37;
when "000" =>
O_sw_IGBT<=sw_IGBT0;
O_sw_BJT<=sw_BJT0;
sw_3<=sw30;
when others =>
O_sw_IGBT<='0';
O_sw_BJT<='0';
sw_3<='0';
end case;
end if;
end process;
```

```
end Behavioral;


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.numeric_std.ALL;
entity debounce is
port ( reset,sw : in  STD_LOGIC;
clk : in  STD_LOGIC;
db : out  STD_LOGIC);
end debounce;
architecture Behavioral of debounce is
constant N :integer:=19;
signal q_reg,q_next: unsigned (N-1 downto 0);
signal m_tick : std_logic;
type eg_state_type is (zero,wait1_1,wait1_2,wait1_3,one,wait0_1,wait0_2,wait0_3);
signal state_reg,state_next: eg_state_type;
begin
process(clk,reset)
begin
if reset='1' then
q_reg <= (others=>'0');
elsif (clk'event and clk = '1') then
q_reg <= q_next;
end if;
end process;
q_next<=q_reg+1;
m_tick<='1' when q_reg=0 else
'0';
process(clk,reset)
```

```
begin
if (reset='1') then
state_reg<=zero;
elsif (clk'event and clk='1') then
state_reg<=state_next;
end if;
end process;
process (state_reg,sw,m_tick)
begin
state_next<=state_reg;
db<='0';
case state_reg is
when zero =>
if sw='1' then
state_next<=wait1_1;
end if;
when wait1_1 =>
if sw='0' then
state_next<=zero;
else
if m_tick='1' then
state_next <=wait1_2;
end if;
end if;
when wait1_2=>
if sw='0' then
state_next<=zero;
else
if m_tick='1' then
```

```
state_next <=wait1_3;
end if;
end if;
when wait1_3=>
if sw='0' then
state_next<=zero;
else
if m_tick='1' then
state_next <=one;
end if;
end if;
when one=>
db<='1';
if sw='0' then
state_next<=wait0_1;
end if;
when wait0_1=>
db<='1';
if sw='1' then
state_next<=one;
else
if m_tick='1' then
state_next <= wait0_2;
end if;
end if;
when wait0_2=>
db<='1';
if sw='1' then
state_next<=one;
```

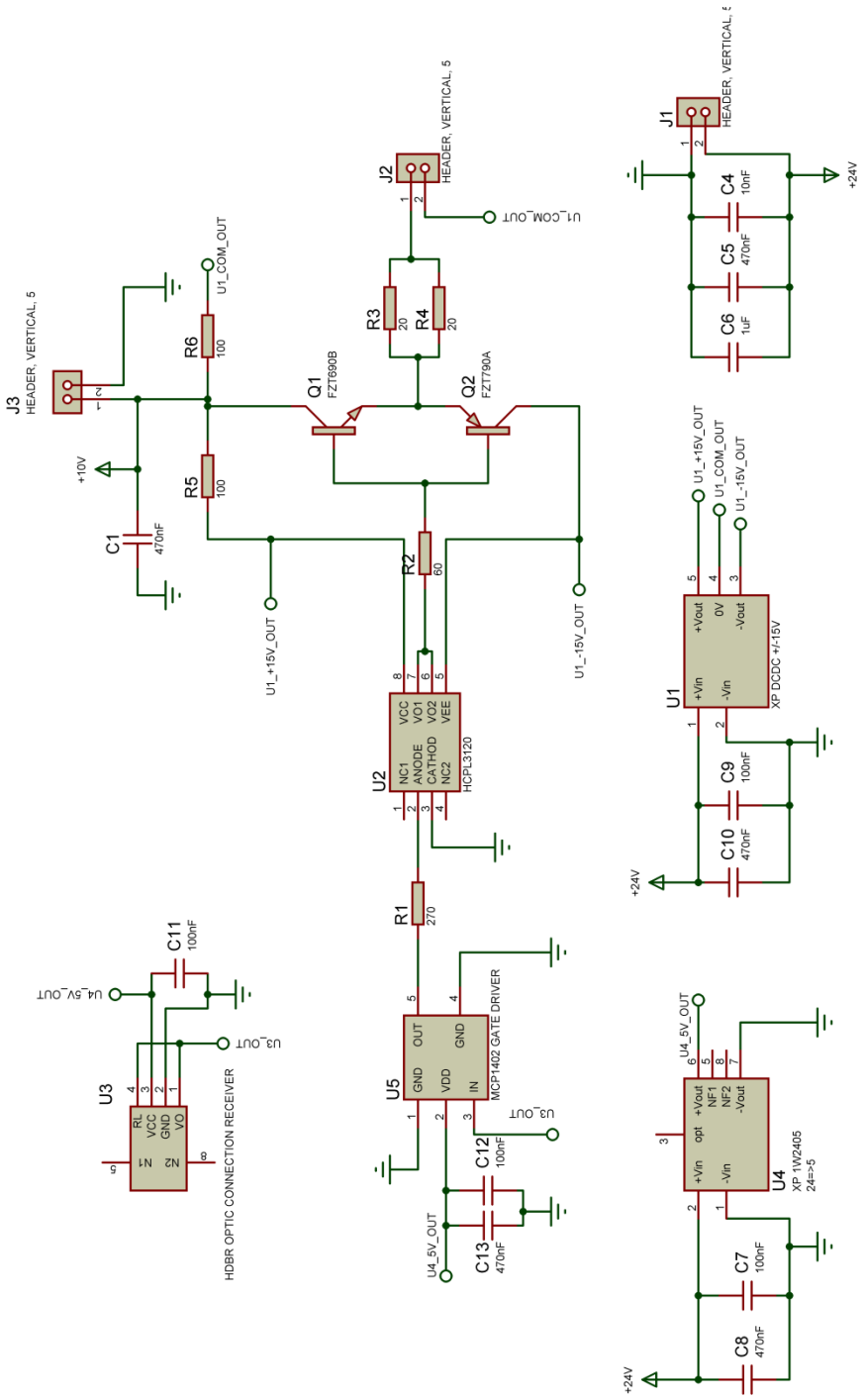
```
else
if m_tick='1' then
state_next <= wait0_3;
end if;
end if;
when wait0_3=>
db<='1';
if sw='1' then
state_next<=one;
else
if m_tick='1' then
state_next <= zero;
end if;
end if;
end case;
end process;
end Behavioral;[120]

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;
entity heating_control is
generic(N_IGBT:integer:=500;
N_BJT_low1:integer:=100;
N_BJT_high1:integer:=250;
N_BJT_low2:integer:=100;
N_BJT_high2:integer:=250;
N_sw3:integer:=50;
N_heating_period:integer:=10);
```

```
port(
clk,reset: in std_logic;
sw_IGBT,sw_BJT,sw3: out std_logic);
end heating_control;
architecture Behavioral of heating_control is
begin
process(clk,reset)
variable con_BJT_low1  :integer range 0 to N_BJT_low1;
variable con_BJT_high1  :integer range 0 to N_BJT_high1;
variable con_BJT_low2  :integer range 0 to N_BJT_low2;
variable con_BJT_high2  :integer range 0 to N_BJT_high2;
variable con_IGBT  :integer range 0 to N_IGBT;
variable con_sw3a  :integer range 0 to N_sw3;
variable con_sw3b  :integer range 0 to 49-N_sw3:=49-N_sw3;
variable sw_IGBT_delay  :integer range 0 to 15;
variable heating_period :integer range 0 to N_heating_period;
begin
if reset='1' then
con_sw3a:=N_sw3;
con_sw3b:=49-N_sw3;
sw3<='0';
elsif (clk'event and clk='1') then
if con_sw3a /= 0 then
sw3<='1';
con_sw3a:=con_sw3a-1;
elsif con_sw3b /= 0 then
sw3<='0';
con_sw3b:=con_sw3b-1;
else con_sw3a:=N_sw3;
```

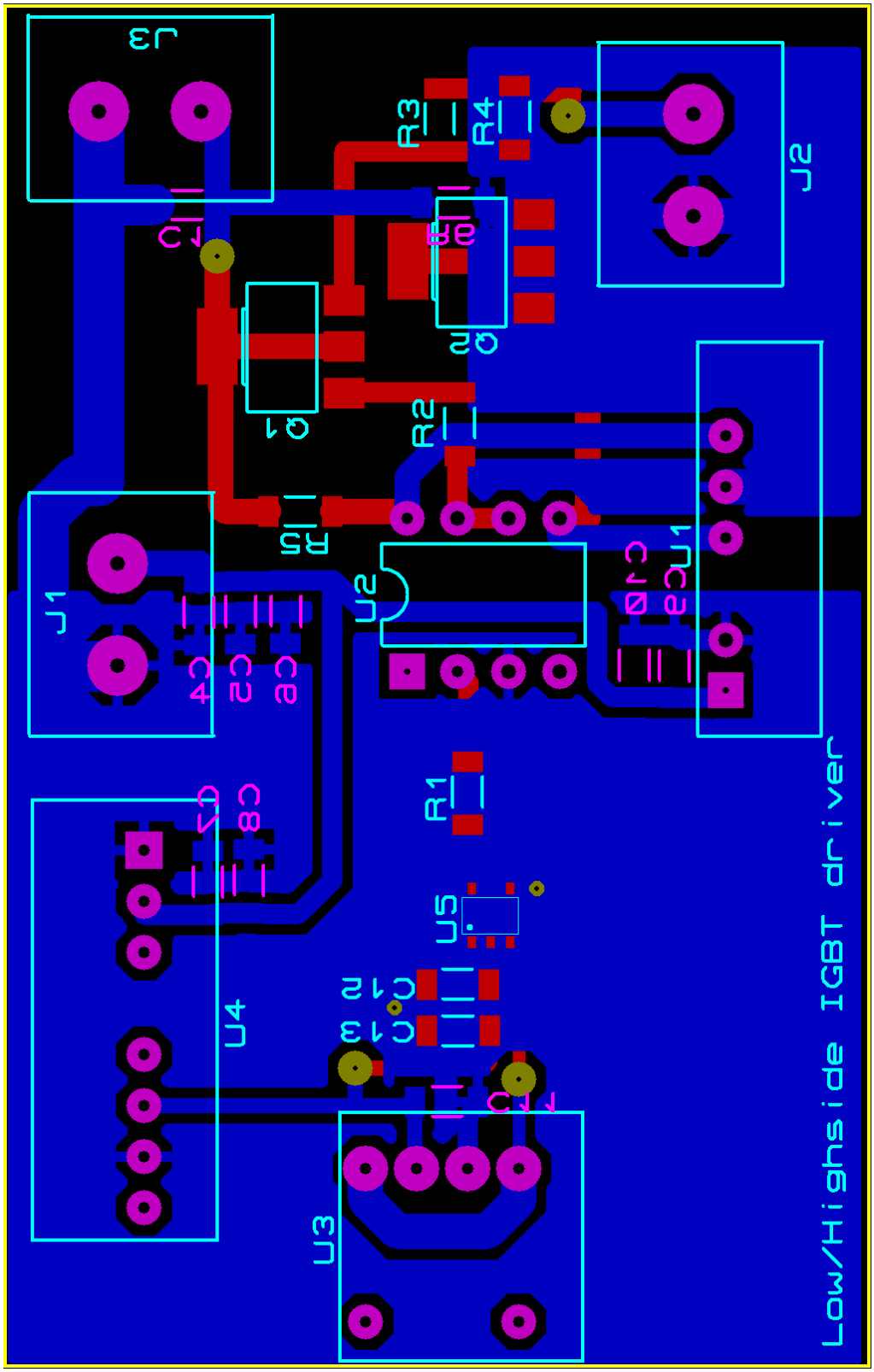
```
con_sw3b:=49-N_sw3;
end if;
end if;
if reset='1' then
heating_period:=N_heating_period;
sw_IGBT_delay:=15;
con_IGBT:=N_IGBT;
sw_IGBT<='0';
con_BJT_low1:=N_BJT_low1;
con_BJT_high1:=N_BJT_high1;
con_BJT_low2:=N_BJT_low2;
con_BJT_high2:=N_BJT_high2;
sw_BJT<='0';
elsif (clk'event and clk='1') then
if con_IGBT /= 0 and sw_IGBT_delay /=0 then
sw_IGBT<='0';
sw_BJT<='1';
con_IGBT:=con_IGBT-1;
sw_IGBT_delay:=sw_IGBT_delay-1;
elsif con_IGBT /= 0 then
sw_IGBT<='1';
sw_BJT<='1';
con_IGBT:=con_IGBT-1;
elsif con_BJT_low1 /=0 then
sw_IGBT<='0';
sw_BJT<='0';
con_BJT_low1:=con_BJT_low1-1;
elsif heating_period /=0 then
heating_period:=heating_period-1;
```

```
sw_IGBT_delay:=15;
con_IGBT:=N_IGBT;
con_BJT_low1:=N_BJT_low1;
elsif con_BJT_high1 /=0 then
sw_IGBT<='0';
sw_BJT<='1';
con_BJT_high1:=con_BJT_high1-1;
elsif con_BJT_low2 /=0 then
sw_IGBT<='0';
sw_BJT<='0';
con_BJT_low2:=con_BJT_low2-1;
elsif con_BJT_high2 /=0 then
sw_IGBT<='0';
sw_BJT<='1';
con_BJT_high2:=con_BJT_high2-1;
else
sw_IGBT<='0';
sw_BJT<='0';
end if;
end if;
end process;
end Behavioral;
```

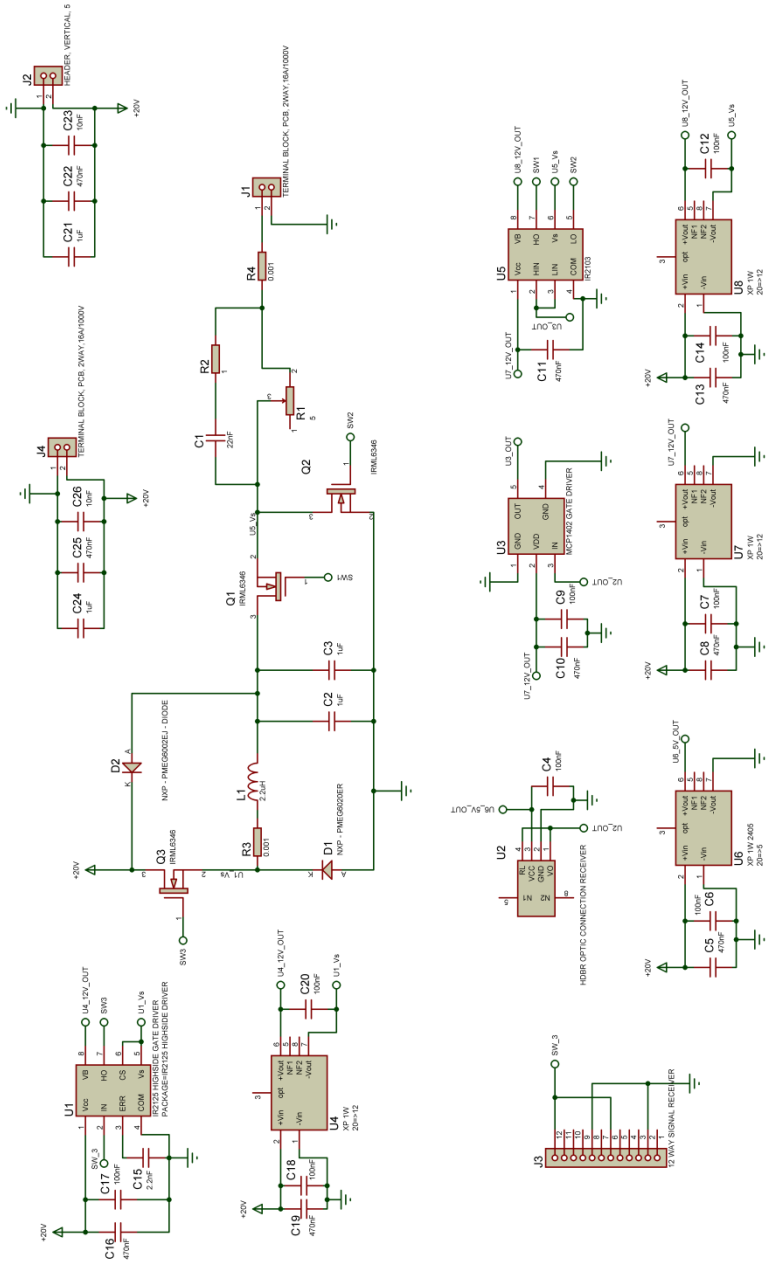
Appendix 8-14 The schematic design for the low side Si IGBT Q1 gate driver



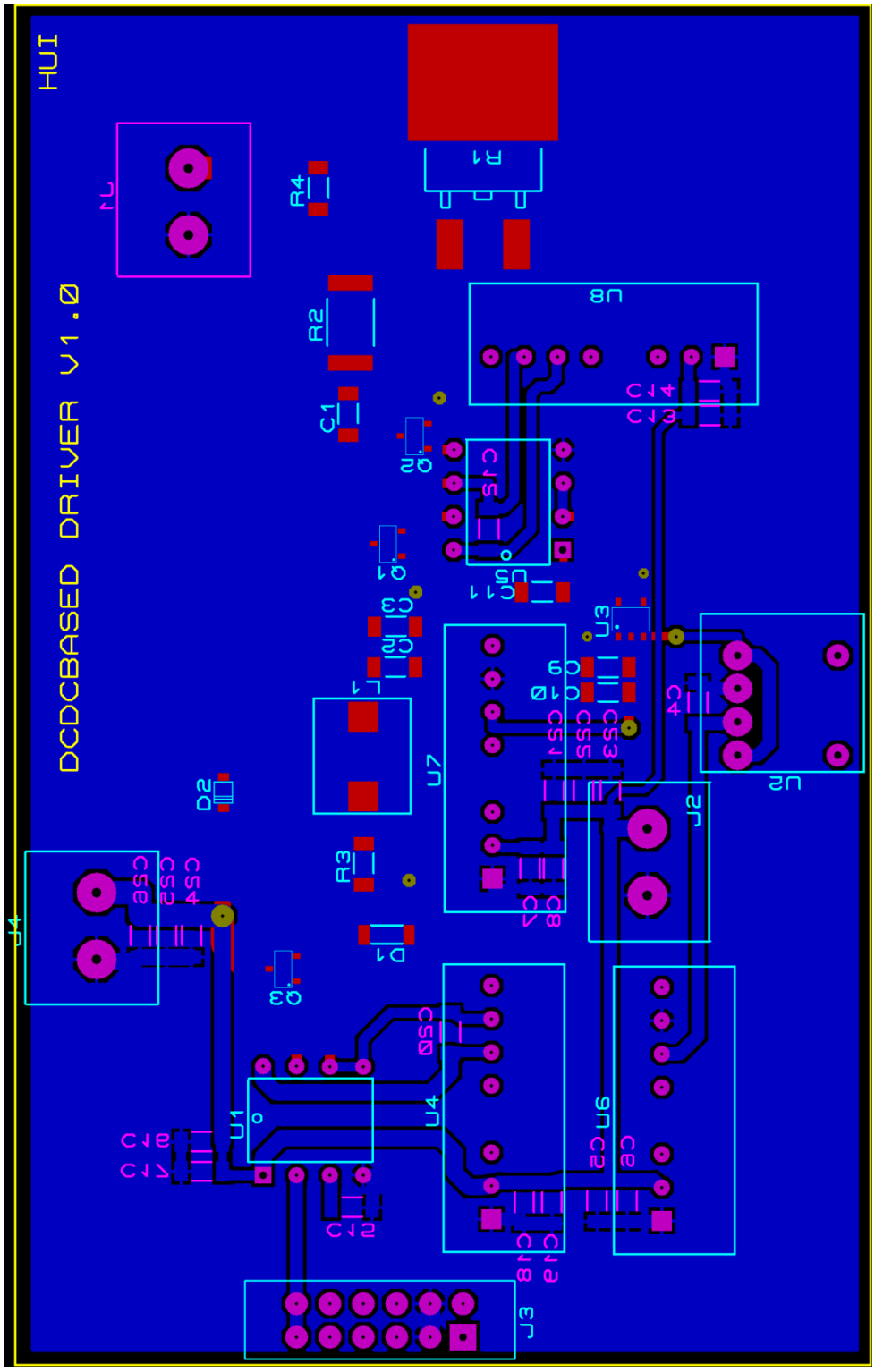
Appendix 8-15 The PCB layout design for the low side Si IGBT Q1 gate driver



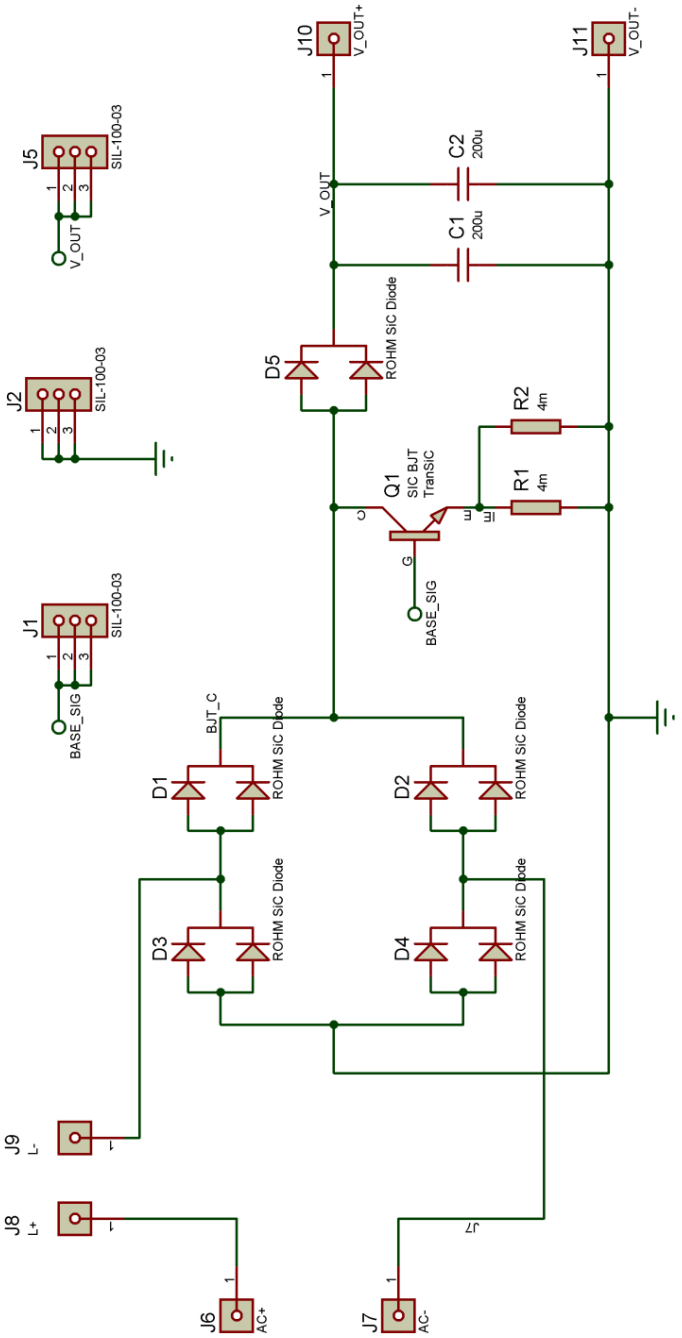
Appendix 8-16 The schematic design for the active base driver without a separate peak current path



Appendix 8-17 The PCB layout design for the active base driver without a separate peak current path



Appendix 8-18 Integrated converter power board schematic



Appendix 8-19 Integrated converter power board layout