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Uncertainty and Disturbance Estimator Design to Shape and Reduce the Output Impedance of Inverter

By:

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Abstract

Power inverters are becoming more and more common in the modern grid. Due to their switching nature, a passive filter is installed at the inverter output. This generates high output impedance which limits the inverter ability to maintain high power quality at the inverter output.

This thesis deals with an impedance shaping approach to the design of power inverter control. The Uncertainty and Disturbance Estimator (UDE) is proposed as a candidate for direct formation of the inverter output impedance. The selection of UDE is motivated by the desire for the disturbance rejection control and the tracking controller to be decoupled. It is demonstrated in the thesis that due to this fact the UDE filter design directly influences the inverter output impedance and the reference model determines the inverter internal electromotive force.

It was recently shown in the literature and further emphasized in this thesis that the classic low pass frequency design of the UDE cannot estimate periodical disturbances under the constraint of finite control bandwidth. Since for a power inverter both the reference signal and the disturbance signal are of periodical nature, the classic UDE low-pass filter design does not give optimal results. A new design approach is therefore needed.

The thesis develops four novel designs of the UDE filter to significantly reduce the inverter output impedance and maintain low Total Harmonic Distortion (THD) of the inverter output voltage. The first design is based on a frequency selective filter. This filter design shows superiority in both observing and rejecting periodical disturbances over the classic low pass filter design. The second design uses a multi-band stop design to reject periodical disturbances with some uncertainty in the frequency. The third solution uses a classic low pass filter design combined with a time delay to match zero phase estimation of the disturbance at the relevant spectrum. Furthermore, this solution is combined with a resonant tracking controller to reduce the tracking steady-state error in the output voltage. The fourth solution utilizes a low-pass filter combined with multiple delays to increase the frequency robustness. This method shows superior performance over the multi-band-stop and the time delayed filter in steady-state. All the proposed methods are validated through extensive simulation and experimental results.

Contents

1. INTRODUCTION.....	1
1.1 Motivation.....	1
1.2 Research aims and objectives.....	3
1.3 The novelty of the contribution.....	5
1.4 Thesis structure	7
1.5 REFERENCES.....	8
2. BACKGROUND	11
2.1 The basic power inverter	11
2.2 Typical designs of inverter output filter.....	14
2.3 The Pulse Width Modulation	14
2.3.1 Sinusoidal Pulse Width Modulation.....	14
2.3.2 Double update modulation	15
2.3.3 Modeling of PWM switching cycle	16
2.4 Design of inverter current loop considering the switching cycle model.....	17
2.5 Inverter output impedance.....	20
2.5.1 Direct feedback design to influence inverter output impedance.....	21
2.5.2 The output impedance of a generic single degree of freedom closed-loop controlled power inverter	23
2.6 The effect of output impedance on the power quality at the inverter output	25
2.7 Overview of inverter control techniques.....	26
2.7.1 Proportional-resonant control.....	26
2.7.2 Repetitive control	28
2.7.3 Other control methods.....	29

2.8 Disturbance observer based design	30
2.8.1 Frequency domain design of disturbance observer	31
2.8.2 Uncertainty and Disturbance Estimator	32
2.8.3 Extended State Observer	33
2.9 Conclusion.....	34
2.9 REFERENCES.....	35
3. Preliminary Studies on Application of UDE to Power Inverter Control.....	45
3.1 Introduction	45
3.2 UDE Overview	46
3.3 Proposed cascaded controller	47
3.3.1 Current compensator design.....	48
3.3.2 Modelling the inverter voltage plant for UDE control design	49
3.4 UDE based voltage controller design.....	51
3.6 UDE filter design for reducing the output impedance	51
3.7 UDE filter design for parallel operation.....	52
3.8 Simulation results	54
3.8.1 Standalone operation	54
3.8.2 Parallel operation.....	56
3.9 Experimental results.....	59
3.10 Conclusion.....	61
3.11 References	62
4. Publication number 1 - Design of a UDE Frequency Selective Filter to Reject Periodical Disturbances.....	67

5. Publication number 2 - Uncertainty and Disturbance Estimator based Controller Equipped with a Multi-Band-Stop Filter to Improve the Voltage Quality of Inverters.....	68
6. Publication number 3 – UDE-Based Controller Equipped with a Time-Delayed Filter to Improve the Voltage Quality of Inverters	71
7. Publication number 4 – UDE-Based Controller Equipped with a Multiple-Time- Delayed Filter to Improve the Voltage Quality of Inverters	73
8. Conclusions and future work.....	74
8.1 Conclusions	74
8.2 Future work	76
8.2.2 Frequency domain design of extended state observer.....	76
8.2.3 UDE based shunt active power filter.....	79
8.3 REFERENCES.....	81
Appendix A- Publications 9 and 10... ..	82

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List of abbreviations

AC	Alternating Current
CSI	Current Source Inverter
DC	Direct Current
DOB	Disturbance Observer
DSP	Digital Signal Processor
DR	Diode Rectifier
EMF	Electro-Motive Force
ESO	Extended State Observer
FSF	Frequency Selective Filter
LG	Loop Gain
LUD/TUD	Lumped/Total Uncertainty and Disturbance
LPF	Low-Pass Filter
MBS	Multi-Band Stop
MTD	Multiple Time Delay
PCC	Point of common coupling
PI	Proportional Integral
PR	Proportional Resonant
PWM	Pulse Width Modulation
SPWM	Sinusoidal Pulse Width Modulation
TD	Time Delay
TDC	Time Delay Control
THD	Total Harmonic Distortion
UDE	Uncertainty and Disturbance Estimator
UPS	Uninterruptable Power Supply
VSI	Voltage Source Inverter
ZOH	Zero-Order Hold

Nomenclature

A_n, B_n, C_n	Nominal state space model matrices
A_T, B_T, C_T	Augmented state space model matrices
\tilde{c}	Command signal
C	Capacitance
$C_I(s)$	Current loop compensator transfer function
$C_n(s)$	Nominal controller transfer function
$C_{PR}(s)$	Proportional resonant compensator transfer function
$C_R(s)$	Resonant compensator transfer function
$C_{RP}(s)$	Repetitive compensator transfer function
$C_V(s)$	Voltage loop compensator transfer function
d	Disturbance input
e	Error signal
e_z	ESO estimation error
f_c	Cut-off frequency
g_u	UDE filter
$H_{ZOH}(s)$	Zero order hold transfer function
i_L	Inductor current
i_L^*	Inductor current reference
i_o	Output current
K_I	Integral gain
K_L	Observer gain
K_P	Proportional gain
K_{PI}	PI controller gain
K_r	Resonant gain
k_U	UDE filter gain
L	Inductance
L_I	Current loop gain
m	Delay index
$P(s)$	Plant transfer function
$P_I(s)$	Current plant model transfer function

$P_n(s)$	Nominal plant transfer function
$P_V(s)$	Voltage plant transfer function
$Q(s)$	DOB filter transfer function
r	Controller output signal
R	Resistance
R_I	Current loop output parallel resistance
S_{1-4}	Switch state
T_c	Computation time
$T_I(s)$	Current tracking transfer function
$T_V(s)$	Voltage tracking transfer function
t_{on}	Transistor on time
T_{PWM}	PWM delay
T_{sw}	Switching cycle time
u	Duty cycle / system input (depends on context)
u_d	Lumped uncertainty and disturbance
u_o	Output bridge voltage
V_{DC}	DC bus voltage
v_o	Output voltage
v_o^*	Reference voltage
$W(s)$	Repetitive control filter transfer function
w	Disturbance model state vector
W, V	Disturbance state space model matrices
x	State-vector
\hat{x}	Estimated state vector
X_I	Current loop output parallel impedance
x_m	Reference model state vector
$y_o(t)$	System output
$y_o^*(t)$	System output reference
z	Augmented state vector
\hat{z}	Estimated augmented state vector
$Z_I(s)$	Current loop parallel impedance
$Z_m\{\cdot\}$	Modified Z transform operator
$Z_O(s)$	Output impedance
$Z_V(s)$	Virtual impedance feedback transfer function

Z_{Σ}	Total output impedance
ζ	Damping ratio
τ_d	Repetitive control time delay
τ_I	PI controller time constant
Φ_M	Phase margin
ω_0	Fundamental frequency or grid frequency
ω_{bw}	Reference model bandwidth
ω_n	Natural frequency
ω_U	UDE filter bandwidth

For signals represented both time-domain and s-domain, z-domain, or frequency domain, lower case represents time domain signals and uppercase s, z or frequency domain signals.

1. INTRODUCTION

1.1 Motivation

Modern utility grids are required to integrate various types of energy sources (e.g., wind, solar, energy storage facilities and other renewable sources) as a result of the demand for sustainable energy in Europe and also as a result of the European Commission's decision to reduce the amount of greenhouse and toxic gas emissions (Knopf, Nahmmacher and Schmid, 2015).

The majority of renewable energy sources and storage devices need power processing to be interfaced into the grid or to a local load. Among the most common renewable sources, are photovoltaic cells and wind turbines. The photovoltaic system is a direct current (DC) source and hence needs a DC to alternating current (AC) conversion. Wind turbines are an AC source, and so they can be interfaced into the grid passively using asynchronous generators. However, to increase the energy harvesting efficiency, the majority of modern turbines are using double conversion topology, which includes an AC to DC rectifier combined with an inverter to feed the energy into the grid.

Another type of application for inverters used in microgrids is energy storage. The need for energy storage facilities in microgrids is to increase the grid redundancy and to smooth the power demand over time. Most of the energy storage devices are based on batteries and supercapacitors which are both DC sources. Another type of common energy storage is based on flywheels. In the main, flywheel-based energy storage is an AC system. However, these are variable frequency sources and hence need double conversion (AC to DC to AC). Hence the inverter is a fundamental power processing device in AC smart grids.

DC to AC conversion plays a crucial part in many other applications such as in uninterruptible power supplies, variable speed motor drives, active power filters. Hence the AC/DC conversion is the fundamental device for the integrity of the smart grid.

In low voltage applications (under 1000V), this is mainly done by power inverters (Zhong and Hornik, 2013). In recent years, as more and more renewable (Apergis and Payne, 2010) and storage sources are interfaced into power grids, the electrical power conversion is shifting from being based on electrical machines to a power electronics based conversion. This is due to growth in the integration of distributed renewable sources and addition of electric inertia into the grid using electrical energy storage devices. In 2017 out of 260GW of new power generation capacity installation 98GW were solar based generation and 52GW wind based generation (Europe, 2017). In solar application, many of the local distributed installations

are photovoltaic devices driven by power inverters and for the wind industry many generators are connected to double conversion which includes an inverter as a front interface. Moreover, the sharp reduction in the cost of battery manufacturing costs from about 1000\$/kWh in 2010 to about 300\$/kWh in 2016 (Robson and Bonomi, 2018) drove many inverter applications as well. While this is yet to expand to applications such as load balancing, current deployment focuses on application such as frequency regulation and peak shaving. Despite that, it is expected for the price to drop to 75\$/kWh by 2030 (Curry and Bloomberg New Energy Finance, 2017), this expected to lead to more grid storage facilities to be installed and to integration of more inverters to the grid.

In general, the DC-AC conversion is carried out using a transistor bridge which can generate a number of fixed voltage levels followed by a filter made of passive components. In this way, the inverter output voltage is driven by the transistor bridge, and then the switching harmonics are filtered by the output filter. The output voltage can be driven at open-loop, but this may lead to poor performance. Therefore closed-loop controllers are utilised to regulate its output voltage.

One of the critical elements in the DC to AC conversion is the power quality of the inverter. Power quality of an AC voltage source is defined by the voltage stability, phase balance (for multi-phase systems) and the Total Harmonic Distortion (THD) of the output voltage of the AC source.

Many ways are proposed for maintaining high power quality at the output of inverters. Some are topology driven such as multi-level inverters where the inverter has many possible fixed voltage levels at the bridge output. This helps to both reduce the switching frequency and the size of the output LC filter. However, this type of inverters contains large amount of switches. Therefore, they are in general less popular than the classic H-bridge or neutral clamped inverters. Other ways to improve power quality are control algorithms, where the main challenge is to achieve good power quality under the PWM bandwidth and computational power constraints.

In power inverters, the voltage stability mainly depends on the strength of the DC source and the energy stored in the DC-link capacitance. However, the THD depends mainly on the harmonic distortion levels of the drawn current and the inverter output impedance.

High THD levels lead to low efficiency of electric motors, ageing of electrical machinery insulation, shortening of electrical equipment useful life (Abbas and Saqib, 2007) and other problems such as overloading of power factor correction capacitors as a result of resonance

with the grid impedance and derating of the grid infrastructure. As a result of these, technical regulations limit the voltage THD at 5% (Yousefpoor *et al.*, 2012; Zhong and Hornik, 2013).

To limit the inverter electro-magnetic interference and to attenuate the switching frequency of the inverter, an output filter is installed at the output of the inverter. This filter determines the passive output impedance of the inverter. Unlike in mechanical generators, where the output inductance of the generator is decreased as the size of the generator increases, the passive impedance of the inverter often increases with the power rating. These are mainly due to the limitations of the power switches and because efficiency requirements limit the switching frequency of the inverter. These in return decreases the output filter cross-over frequency and increases the passive output impedance.

1.2 Research aims and objectives

Many control strategies have been proposed to regulate the inverter output voltage, one of the main criteria to judge them is the output THD of the inverter. The state of the art controller design for inverters is carried out by either applying a non-linear control algorithm such as sliding mode and hysteresis controllers or by using linear compensators such as proportional resonant and repetitive compensators. All of them are offered as a single degree of freedom design which leads to the tracking performance of these controllers to be coupled with the disturbance rejection performance (Chen *et al.*, 2016). Moreover, many of these control schemes are demonstrated using either a bulky capacitor at the output to reduce the passive output impedance, or using a direct measurement of the load current and feeding it forward to the controller.

Disturbance observers are the most widely employed two degrees of freedom control structures (Aharon, Shmilovitz and Kuperman, 2018a). Their main feature is that they allow the designer to separate the design of the disturbance rejection controller from the tracking controller. Power inverters are characterized by a strong disturbance coming from the output current, and hence one of the critical tasks of the inverter is to minimize the load current impact on the output voltage quality.

In this work, the possibility of using the Uncertainty and Disturbance estimator (UDE) technique (Sanz *et al.*, 2016), is explored for estimating the output current of an in inverter and to reduce the impact of harmonic currents on the output voltage of the inverter by reducing the output impedance of the inverter.

The UDE is a robust control technique that estimates the model deviation, uncertainties, and the disturbance input to the controlled system. It can deliver accurate tracking when time-

delays and nonlinearities are present in a system (Kuperman and Zhong, 2009, 2011). Moreover, the UDE controller decouples the controller tracking ability from the disturbance rejection performance through the design of the UDE filter. A second decoupling occurs in the frequency domain where the UDE filter design attenuates the low frequency disturbances and the UDE reference model determine the high frequency disturbance rejection and noise attenuation. However, the UDE filter bandwidth is limited by the actuator dynamics (Kuperman, 2015) and therefore in the case where the expected disturbance bandwidth is close to the actuator bandwidth a straightforward implementation is not always possible.

The main advantage of the UDE with power electronics is the ability to control the disturbance rejection without affecting the tracking performance which gives it a two degrees of freedom nature (Zhong, Kuperman and Stobart, 2011). This is achieved by using the UDE to estimate unknown disturbance inputs and use them as a feedforward term to cancel the disturbance effect on the output. This fact opens the possibility to directly influence the output impedance of the inverter by feeding back an accurate estimation of the inverter output current. Moreover, unlike in schemes where the internal inductor current is fed back to the controller, this approach permits the reduction of the inverter output impedance significantly.

This research aims to build on the UDE theory design a novel designs of disturbance observer to estimate the strong disturbance arising from the load current. The primary goals to achieve in such a design are

- (i) Robustness to load current and low output distortion.
- (ii) Robustness to frequency deviation. Low THD at varying base frequency.
- (iii) Stable operation at no-load and load switching.
- (iv) Good transient response - Low overshoot and short settling times.

1.3 The novelty of the contribution

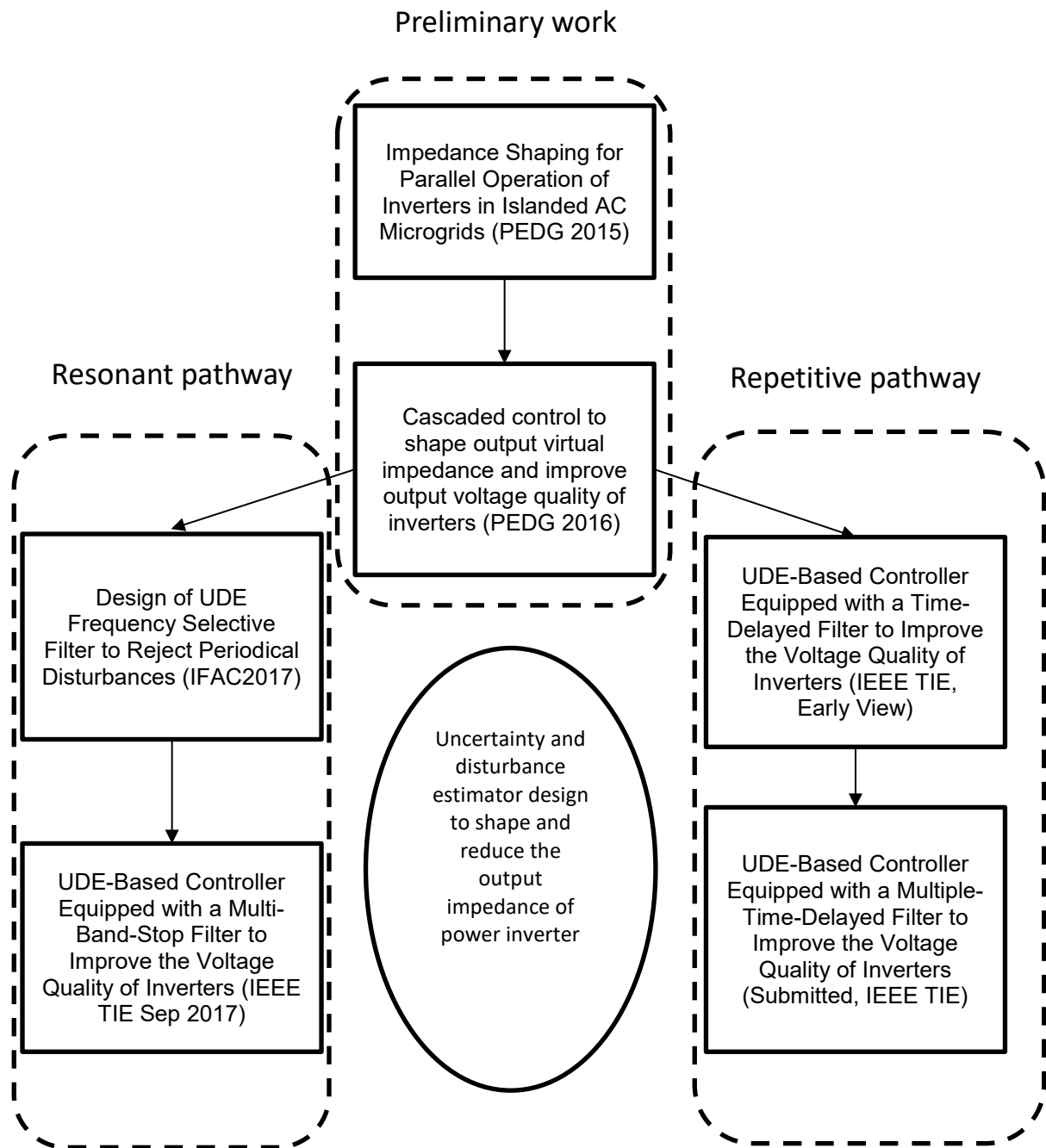


Fig 1.1 the thesis overview

The solutions developed to address the research aims and objectives are technically linked and schematically shown in Fig 1.1, with each paper contribution identified within it. This is also reflected in the thesis structure.

The thesis seeks to demonstrate that the two degrees of freedom design of the Uncertainty and Disturbance Estimator (UDE) can both reject disturbances and nominalize the tracking performance of an inverter. Where the tracking performance defines the inverter internal voltage source equivalent to the electromotive force in generators, and the disturbance rejection performance determines the output impedance. It also builds upon the classic UDE filter designed for rejecting constant disturbances and developed for dealing with the more challenging periodical disturbances. It harnesses the relation between the UDE filter designs and the closed loop output impedance of a power inverter in developing novel disturbance rejection solutions.

Many filter designs have been proposed to improve the disturbance rejection of the UDE (Zhong, Kuperman and Stobart, 2011; Chandar and Talole, 2014). However, as explained in (Kuperman, 2015; Aharon, Shmilovitz and Kuperman, 2018b, 2018a), finite actuator bandwidth introduces a constraint on both the UDE filter design and the reference model design.

In the voltage source inverter cascaded loop design, the current closed-loop control serves as the actuator for the voltage loop. The current controller closed-loop bandwidth is limited by the pulse-width modulation transport and computation delays. These constitute a limited control bandwidth constraint for the voltage controller design.

In this thesis four novel UDE designs are proposed for dealing with periodical disturbances, taking into account both the bandwidth of the periodical disturbance and the finite bandwidth limitation coming from the current closed-loop controller.

The solution is then divided into two pathways as shown in Fig 1.1 The first pathway is the resonant pathway, where the filter is designed as a chain of zero-phase bandpass filters. In this pathway two solutions are proposed; (i) a filter made of second-order resonant filter chain (ii) a multi-band solution which can deal with periodical disturbance with some uncertainty in the fundamental frequency.

The second pathway is the repetitive pathway, in the first solution, it is offered to combine resonant reference model aimed to eliminate the steady-state error in the tracking performance with a high order filter followed by a delay to match zero phase action in the relevant expected spectrum of the disturbance. The second solution offers a design combining multiple delays to increase the controller robustness to uncertainty in the fundamental period of the system.

1.4 Thesis structure

The thesis is organized as follows. The background section is dedicated to the description of the technical background concepts that are required to provide the relevant context to the work described in further chapters. These include the inverter structure followed by a discussion and description of pulse width modulation, the inverter output impedance, description of the design of the internal current regulator and an overview of various control techniques and disturbance observers.

Chapter 3 tackles the problem of the high passive output impedance. In the chapter, it is demonstrated that by using the UDE combined with advanced modulation techniques it is possible to reduce the closed loop inverter output impedance below the output filter passive impedance and hence to achieve a lower THD value when the inverter is loaded with a non-linear load. It also addresses the problem of power sharing among parallel inverters in the presence of current harmonics. By using a direct implementation of the UDE to a power inverter, it is demonstrated that the current is shared in relation to the UDE filter bandwidth.

Chapter 4 addresses the problem of designing a disturbance observer for periodical disturbances under bandwidth limitation. The paper describes the method of using frequency selective filter design to achieve an accurate estimation of the disturbance input while maintaining sufficient stability limits. In this chapter, it is demonstrated that the estimation error of the proposed disturbance observer is lower in magnitude than the classic low pass filter design. The chapter is published as a paper in IFAC 2017 conference proceedings.

Chapter 5 focuses on the issue of designing a disturbance observer for an inverter with uncertain output frequency. The proposed solution is to use a high order multi-band stop design to significantly reduce the inverter output impedance around frequency regions of interest. Furthermore, it is proposed to design the UDE filter by shaping the desired impedance and derive the UDE filter from it. The chapter is published as an article in the IEEE Transactions on Industrial Electronics.

Chapter 6 addresses two critical issues arising from the work in chapter 5. The first issue is the effort required to design and implement the proposed filter and the second issue is the transient performance of the controller. The chapter describes the methods of using a delay to design a low-pass filter with zero phase delay at the points of interests. Experimental results are given to demonstrate the successes of the method. The results are then compared to the results in chapter 5. The chapter is published as an article in IEEE Transaction on Industrial Electronics.

Chapter 7 addresses the frequency robustness of the design proposed in chapter 6. In this chapter it is proposed to use multiple delays to shape the output impedance of the inverter and by this to increase the frequency robustness of a time-delayed filter. The resulting algorithm, performance is then demonstrated through experimental results and compared to both the multi-band stop design offered in chapter 5 and the time delayed filter offered in chapter 6 both in terms of transient response and frequency robustness.

The thesis concludes with a summary of its findings and future directions for research.

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2. BACKGROUND

2.1 The basic power inverter

A power inverter is a converter which converts DC power to AC power (Prince, 1925; Owen, 1996). This power converter operates in discrete states. A single phase full bridge inverter is capable of driving four different discrete states. Fig 2.1 shows the electrical structure of the single phase full bridge inverter. The inverter has two main parts, the switching H-bridge, and the output filter. The function of the H-bridge is to generate an alternating voltage at u_o using its discrete states and the function of the output filter is to filter the high frequency components of the modulation. The gate driver is an electronic device which drives the power transistor gates in accordance with the controller output. To prevent the H-Bridge from short-circuiting the DC source, switches S_1, S_2 and S_3, S_4 are operating in complementary. For example when S_1 is on S_2 is off and vice versa. The same rule applies to switches S_3 and S_4 . This resembles two binary states which can generate three different voltages across the bridge terminals. Table 2.1 shows the different possible states of the H-bridge output, where S_1 and S_3 are the high side switches, u_o is the bridge voltage and V_{DC} is the DC-link voltage.

Table 2.1. The inverter H-bridge states

S_1	S_3	u_o
On	Off	V_{DC}
Off	On	$-V_{DC}$
Off	Off	0
On	On	0

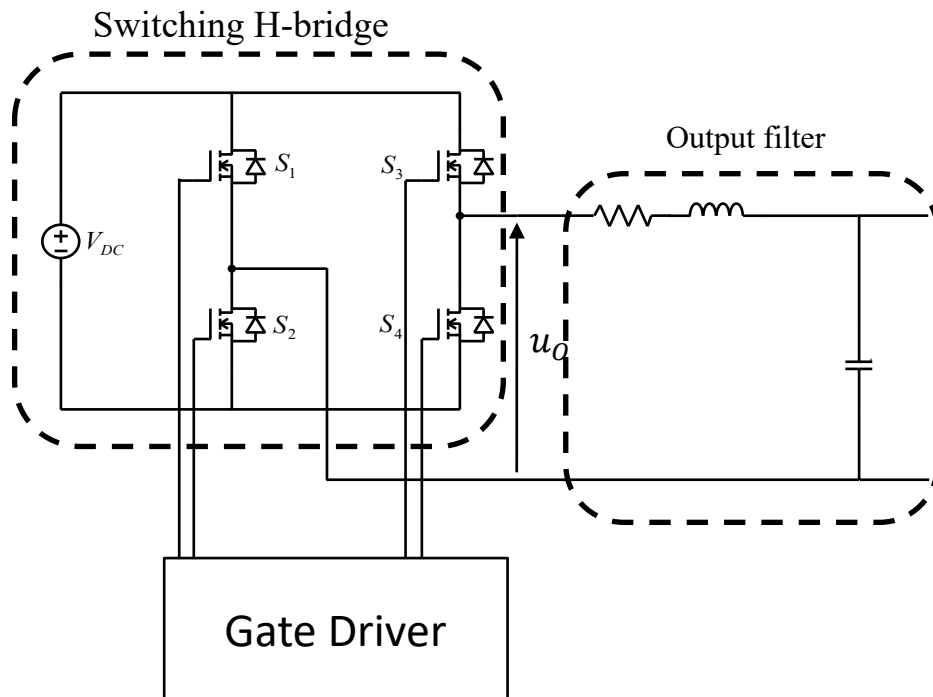


Fig 2.1 the electrical structure of the single phase power inverter

In low power application, square wave or modified square wave may be acceptable (Mythili and Kayalvizhi, 2013) and the DC power source is inverted to AC by switching between V_{DC} to $-V_{DC}$. In the case of modified square wave zero states are added in order to reduce switching stress and to minimize the 3rd harmonic (Nayak and Hoft, 1975). Fig 2.2 shows the sketches of square wave and modified square wave and Fig 2.2.3 shows the corresponding spectrum. The concept extends with to Sinusoidal Pulse Width Modulation (SPWM) that results in that the more pulses there are, more harmonics are reduced. In high power application, the output of the inverter is expected to be close to a pure sine wave and therefore the output of the inverter in this case has to be sine modulated (Power Society, 2014). A more detailed description of the SPWM is given in section 2.3.1. There are two main types of inverters (i) is the Current Source Inverter (CSI) mainly used to drive high power motors (Phillips, 1972), and (ii) is the Voltage Source Inverter (VSI) (Twining and Holmes, 2003). The basis of the division is the type of the energy storage element in the DC bus (Wu *et al.*, 2008) or whether the DC bus is a voltage source or a current source (Peng, 2003). VSIs can be either current controlled as in (Nabae, Ogasawara and Akagi, 1986) or voltage controlled as in (Chen and Chu, 1995).

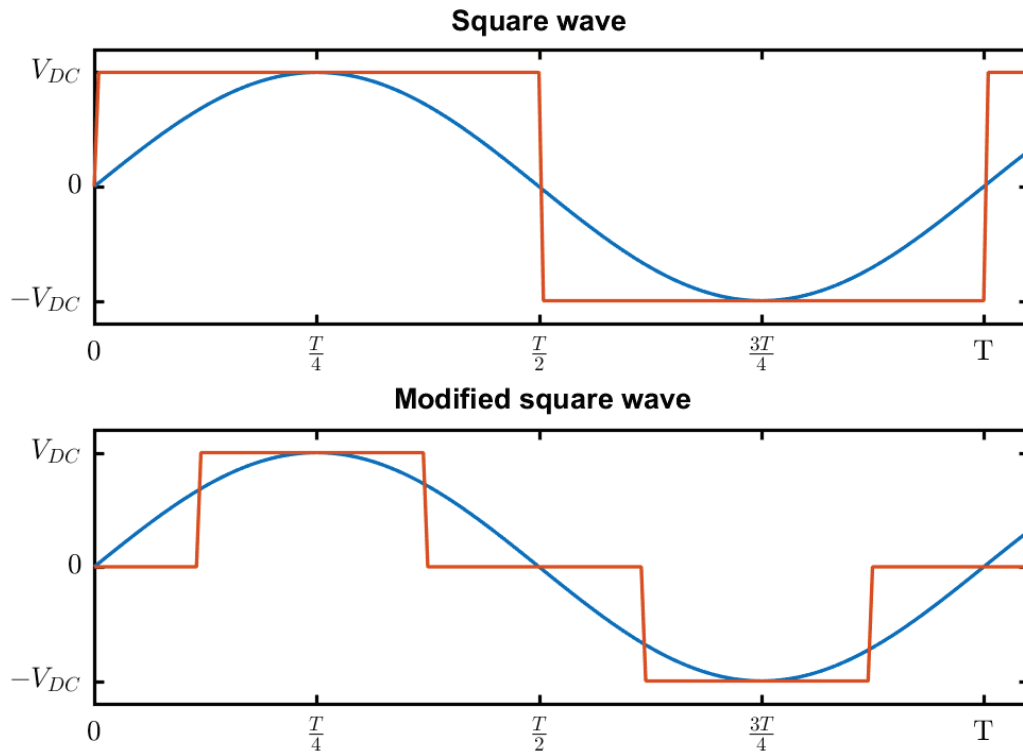


Fig 2.2 Waveform sketches for square wave and modified sine wave

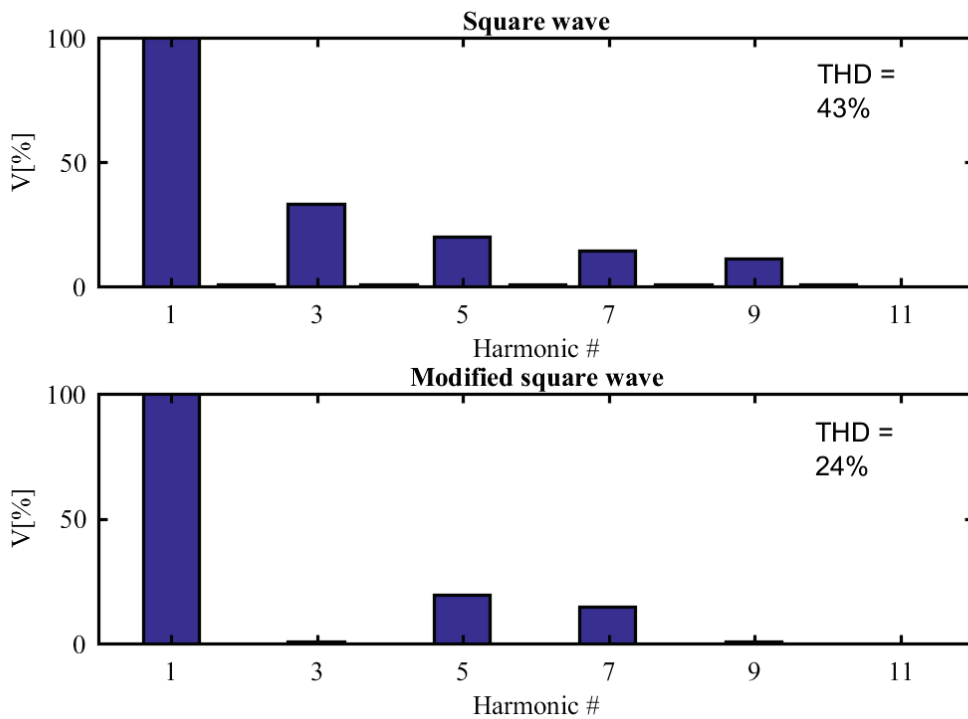


Fig 2.3 The harmonic spectrum of typical square wave and modified square wave

2.2 Typical designs of inverter output filter

The primary purpose of the inverter output filter is to attenuate the switching ripple coming from the H-bridge (Loh and Holmes, 2005). There are three common types of inverter output filters. The L, LC and LCL filters, where L denotes an inductor and C capacitor. The L filter is used in grid-tied current controlled inverters to attenuate the output current ripple while the LC and LCL are designed for both current controlled (Moran, Ziogas and Joos, 1989) and voltage controlled inverters (Weiss *et al.*, 2004). The LCL filter is mainly adopted when a grid interface is desired, to reduce inrush currents when the inverter is connected. In this thesis, the LC filter is adopted since the proposed inverter acts in standalone operation.

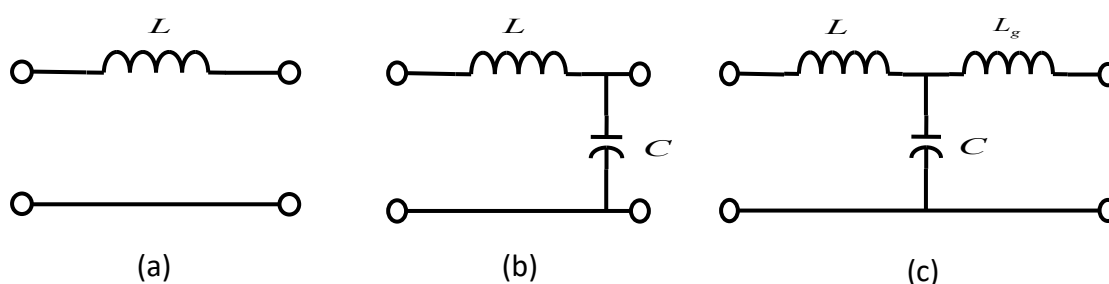


Fig 2.4 Circuit representation of the inverter output filter for (a) L filter, (b) LC filter (c) LCL filter.

The LC filter cut off frequency is calculated as

$$f_c = \frac{1}{2\pi\sqrt{LC}} \quad (2.1)$$

To attenuate the effect of the switching frequency on the output voltage f_{SW} , the cut-off frequency f_c of the output filter, has to be much smaller than the switching frequency.

2.3 The Pulse Width Modulation

2.3.1 Sinusoidal Pulse Width Modulation

The pulse width modulated signal is generated by comparing a carrier signal to the modulating signal. The carrier signal can be either a sawtooth wave or a triangular signal. The bipolar PWM generates a sine averaged signal by switching the bridge voltage between $+V_{DC}$ to $-V_{DC}$. The unipolar modulator is modulating the output signal using the three possible output states (V_{DC} , 0, $-V_{DC}$) (Tal, 1976). Fig 2. 2.5 shows the inverter bridge output for both bipolar and unipolar modulators.

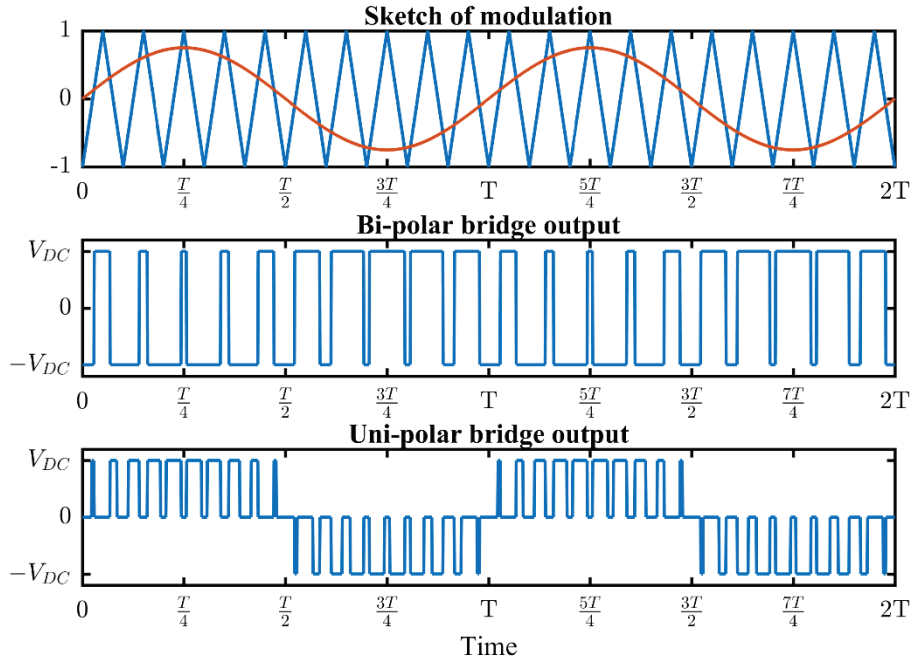


Fig 2.5 Unipolar vs Bipolar SPWM modulation for an inverter

Even though unipolar modulation is more straightforward to implement, the switching stress is lower at this mode as a result of the fact that only one leg is switched at each cycle. These lead to the efficiency of the unipolar modulated inverter being higher (Lai and Ngo, 1995). Therefore it is chosen to be the modulation method in the thesis.

2.3.2 Double update modulation

Many PWM methods are proposed to generate a pure sine wave at the output of the inverter. The main differences between those techniques are the carrier wave shape and the PWM update intervals. The PWM carrier can be either triangular or sawtooth shape (Van de Sype, K De Gusseme, *et al.*, 2004) and the update intervals can be either single update or double update. In single update the PWM duty cycle is updated once in a switching cycle and in double update the PWM duty cycle is updated twice in a switching cycle (Deng, Oruganti and Srinivasan, 2005). There are two main delay sources in the PWM signal, namely, the sampling, and the transport delay (Holmes *et al.*, 2009). While the first is associated with the digital controller delay and therefore doesn't exist in analog modulators, the latter is associated with both digital and analog modulation.

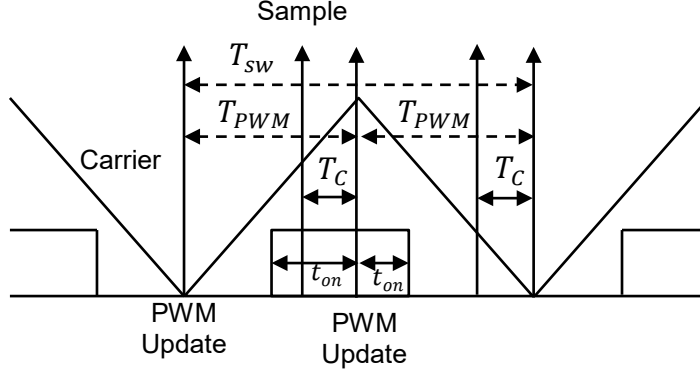


Fig 2.6. Double update modulated PWM

The double update PWM reduces the transport delay by half through updating the output duty cycle twice in each switching period. In the digital controller, the duty cycle is updated twice, first at the beginning of the switching cycle and the second at the modulated signal peak. Fig 2.6 shows a digital switching cycle where T_c is the computation delay, T_{sw} is the switching cycle, T_{PWM} is a half cycle and PWM update marks the update intervals of the duty cycle.

2.3.3 Modeling of PWM switching cycle

In the literature accurate models of uniformly sampled PWM are offered for both s-domain (Van de Sype, K De Gusseme, *et al.*, 2004) and z- domain (Van de Sype, K. De Gusseme, *et al.*, 2004) These models take into account the impact of the duty cycle operation point over the time delay. However, according to (Buso and Mattavelli, 2015), in the case of the inverter, an approach of uniformly sampled PWM can be adopted. In this approach, the inverter H-bridge can be modeled as a Zero-Order Hold (ZOH) followed by the output filter and the DSP sampling and communication time can be modeled as an extra delay block.

Fig 2.6 shows the timing model of the switching cycle. During t_{on} the bridge average output voltage is

$$\bar{u}_o(kT) = u(kT) \cdot V_{DC}, u(kT) \in [-1,1] \quad (2.2)$$

where $u(kT)$ is either the sampled duty cycle or a variable which depends on the modulation and inverter bridge topology, k is the sample number and $\bar{u}_o(kT)$ is the average H-bridge voltage over a PWM cycle. The majority of power inverters are buck type, therefore, $u(kT)$ is bounded between $-1, 1$ (Kerkman *et al.*, 1991). According to (Mattavelli *et al.*, 2008) during the switching cycle, the inverter behaves as a ZOH. The ZOH s-domain transfer function is

$$H_{ZOH}(s) = \frac{1 - e^{-sT}}{s} \quad (2.3)$$

where T is the window length of the ZOH and equals to the PWM update interval time length.

In the case of the double update modulation, the ZOH window length T_{PWM} equals to half of the switching cycle length. Taking into account the computation delay and the Laplace form of (2.3) the H-bridge output voltage is

$$U_o(s) = U(s) \cdot V_{DC} \cdot H_{ZOH}(s) \cdot e^{-sT_c} \quad (2.4)$$

where T_c is the computation delay.

2.4 Design of inverter current loop considering the switching cycle model

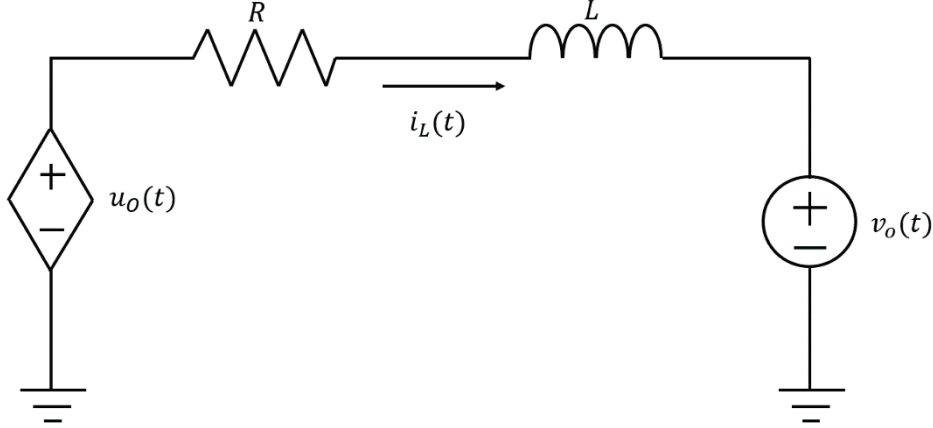


Fig 2.7 Equivalent circuit for controlling the inductor current

In a cascaded control scheme, the LC circuit is divided into two equivalent circuits. The first equivalent circuit, shown in Fig 2.7, controls the LC filter inductor current and used as the actuator for driving the output capacitor voltage. Applying Kirchoff's voltage law to this circuit the loop equation is

$$L \frac{di_L}{dt} + i_L R = u_o - v_o \quad (2.5)$$

The input to output transfer function in the s-domain is

$$\frac{I_L(s)}{U_o(s)} = \frac{1}{Ls + R} \quad (2.6)$$

Combining (2.6) with (2.4) yields the current regulator plant as

$$P_I(s) = \frac{1 - e^{-sT_{PWM}}}{s} \cdot \frac{V_{DC}}{Ls + R} \cdot e^{-sT_c} \quad (2.7)$$

In the case where T_c is an integer multiple of T_{PWM} , the control time delay can be modelled as a sum of unit delays. However, when T_c is a fraction of T_{PWM} , then the modified z-transform (Jury, 1964) has to be used. By considering the delay index m as

$$m = 1 - \frac{T_c}{T_{PWM}}, m \in [0, 1] \quad (2.8)$$

and, from (2.7) and (2.8) the modified z-transform of the plant model combined with the PWM is,

$$P_I(z, m) = (1 - z^{-1}) \mathcal{Z}_m \left\{ \frac{1}{s} \cdot \frac{V_{DC}}{Ls + R} e^{-s(1-m)T_{PWM}} \right\} = \frac{V_{DC}}{R} \cdot \frac{z(1 - e^{-\frac{R}{L}mT_{PWM}}) - e^{-\frac{R}{L}T_{PWM}} + e^{-\frac{R}{L}mT_{PWM}}}{z(z - e^{-\frac{R}{L}T_{PWM}})}, \quad (2.9)$$

where $\mathcal{Z}_m\{\cdot\}$ is the modified z-transform operator. Note that when $m = 1$, equation (2.9) becomes the z-transform of the output LC filter and when $m = 0$, equation (2.9) becomes the z-transform of the LC filter with a unit delay at the input.

In the case where $T_c \ll T_{PWM}$ the system can be treated as first order and a deadbeat response can be achieved. In this case, $m \approx 1$ and (2.9) reduces to

$$P_I(z) = \frac{V_{DC}}{R} \frac{1 - e^{-\frac{R}{L}T_{PWM}}}{z - e^{-\frac{R}{L}T_{PWM}}} \quad (2.10)$$

By choosing the controller gain K_P as

$$K_P = R \cdot \frac{e^{-\frac{R}{L}T_{PWM}}}{1 - e^{-\frac{R}{L}T_{PWM}}}, \quad (2.11)$$

and manipulating the current loop compensator C_I to

$$C_I = \frac{K_P}{V_{DC}} \quad (2.12)$$

the current controller closed-loop transfer function becomes,

$$T_I(z, m) = \frac{C_I(z) \cdot P_I(z, m)}{1 + C_I(z) \cdot P_I(z, m)}. \quad (2.13)$$

Combining (2.10-2.13) the current regulator closed loop transfer function becomes,

$$T_I(z) = e^{-\frac{R}{L}T_{PWM}} \cdot z^{-1} \quad (2.14)$$

showing that a dead-beat response had been achieved for the current regulator.

Transferring (2.14) to s-domain yields,

$$T_I(s) \approx e^{-\frac{R}{L}T_{PWM}} e^{-sT_{PWM}}. \quad (2.15)$$

Equation (2.15) demonstrates the minimum possible current loop delay is achieved.

In the general case, where T_c is significant, m has to be considered during design. In this case, the closed loop becomes a second order system. In the case of $m > 0$, the damping ratio is taken into account when choosing the appropriate current feedback gain K_P . Let's define

$$\alpha \equiv e^{-\frac{R}{L}T_{PWM}} \quad (2.16)$$

choosing (2.12) as the controller yields the controller loop gain as

$$L_I(z) = C_I(z) \cdot P_I(z, m) = \frac{K_P}{R} \cdot \frac{z(1 - \alpha^m) - \alpha + \alpha^m}{z(z - \alpha)} \quad (2.17)$$

The gain K_P can be tuned graphically using the root locus method. A root locus for a system where $R = 0.5\Omega$ and $L = 3mH$ for different values of m is shown in Fig 2.8. The stability limit is marked on the chart as the unit circle and the limit between underdamping to overdamping is marked as damping ratio of 0.707.

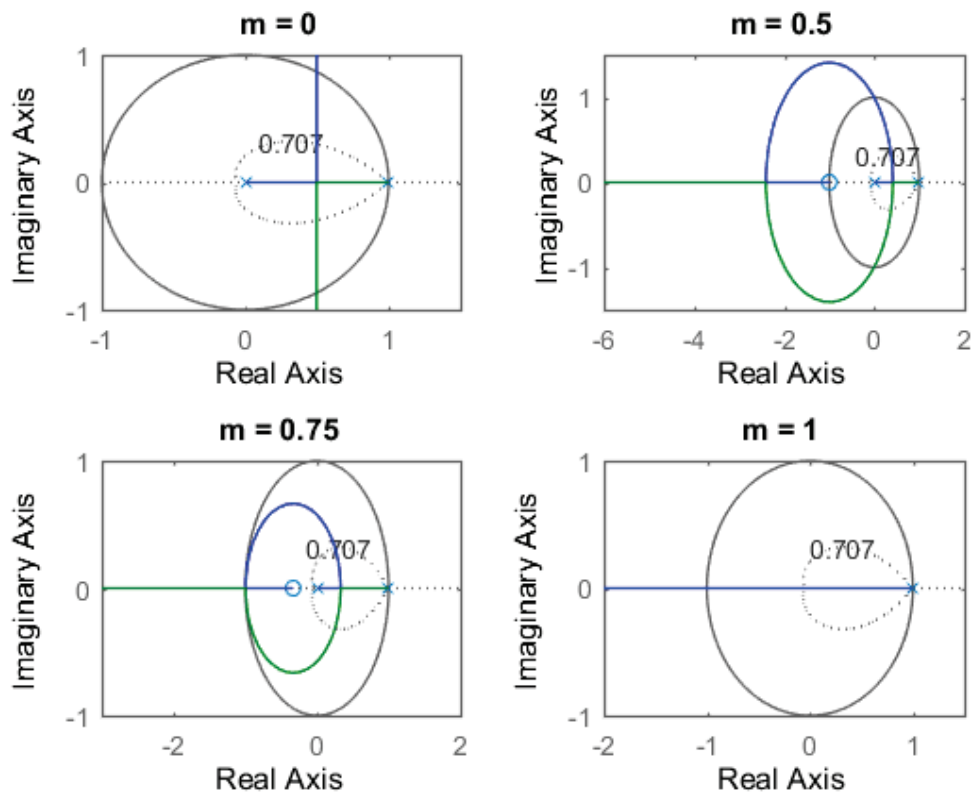


Fig 2.8 Root locus of the closed-loop transfer function with varying controller gain in the z -domain

Table 2.2 Gain and bandwidth values derived from the root locus of Fig 2.8

m	Gain at $\zeta = 0.707$	BW ¹ at $\zeta = 0.707$ [kHz]
0	30	1.6
0.5	43	2.25
0.75	59	3
1	90	5

¹ In the context of this thesis, the BW is defined as the crossover frequency of the loop gain.

The relation between the damping ratio to the system phase margin for a second order system is given in (Nise, 2007) as

$$\Phi_M = \tan^{-1} \left(\frac{2\zeta}{\sqrt{-2\zeta + \sqrt{1+4\zeta^4}}} \right), \quad (2.18)$$

where Φ_M is the phase margin and ζ is the closed loop system damping ratio. Therefore every constant phase margin can be mapped to a particular damping ratio. Using the direct relation between z-domain to s-domain $z = e^{sT}$, the constant damping ratio lines can be mapped to the z-domain as (Ogata, 1995)

$$z = e^{-\zeta\omega_n T} \cdot e^{j\omega_n \sqrt{1-\zeta^2} \cdot T}, \zeta \in [0,1] \quad (2.19)$$

where T is the sampling time and ω_n is the natural frequency. Once the gain design is complete, the closed-loop current controller transfer function becomes

$$T_i(z, m) = \frac{K_p}{R} \cdot \frac{z(1-\alpha^m) + \alpha^m - \alpha}{z^2 + \frac{K_p}{R} \left(1 - \alpha^m - \frac{R}{K_p} \alpha\right) z + \frac{K_p}{R} (\alpha^m - \alpha)}, \quad (2.20)$$

which is a second order system. The design guidelines in this section for the current controller design are adopted in this thesis. The current closed-loop regulator serves as an internal loop in the design of the proposed voltage controller in the thesis. As identified, the voltage regulator will be bandwidth constrained as a results of the current controller inner loop dynamics.

2.5 Inverter output impedance

The inverter output impedance defines the ratio between the inverter output current to the voltage. In inverters operating at open loop, it is mainly influenced by the output filter design. In inverters where the output voltage is closed-loop controlled, it is influenced by both the output filter and the controller parameters.

The shaping and knowledge of an inverter output impedance is essential for power flow control (Li and Kao, 2009; He and Li, 2011; Mahmood, Michaelson and Jiang, 2015), fault current limiting (Moon and Johnson, 1999; Vilathgamuwa, Loh and Li, 2006; Paquette A. D. and Divan, 2015), and load sharing.

2.5.1 Direct feedback design to influence inverter output impedance

In most cases the passive output impedance of inverter is inductive, this results from the inductance of the output filter (Zeng, 2016). In inverters operating at very low voltage

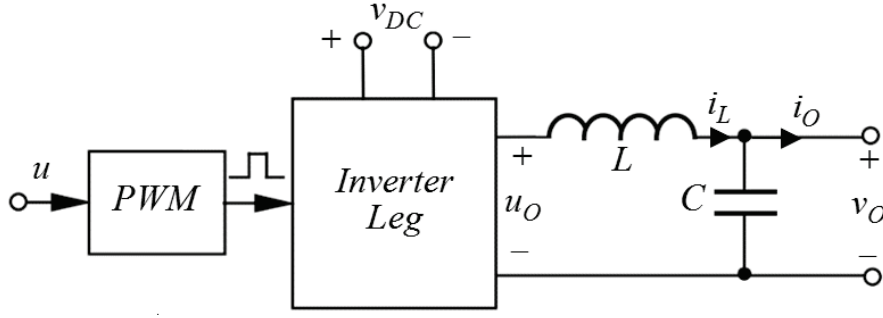


Fig 2.9 A diagram of a typical inverter leg equipped with LC output filter

microgrids (under 50V), as a result of the line impedance it is expected for the passive output impedance to be of resistive nature. (Li and Kao, 2009). One of the common methods to control inverter output impedance is to use the inverter inductor current as a feedforward term. This can be done to force resistive impedance (Guerrero *et al.*, 2004, 2005, 2006), capacitive impedance (Zhong and Zeng, 2011, 2014) or high order impedance (Matas *et al.*, 2010).

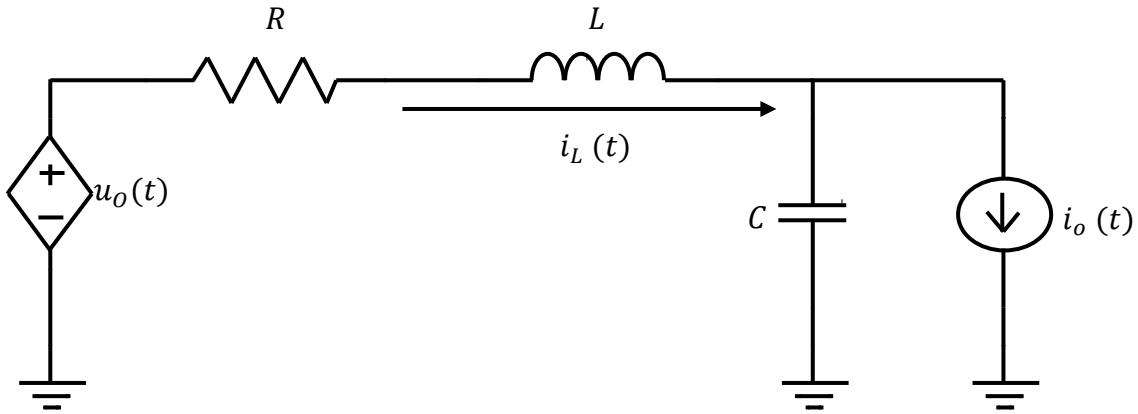


Fig 2.10 An equivalent circuit of a power inverter

Fig 2.9 shows a diagram of an inverter leg equipped with an LC low pass filter and Fig 2.10 shows an equivalent circuit prevalent in the analysis of power inverters (Tuladhar *et al.*, 1997; Zhong, 2013b) where $u_o(t)$ is the average voltage output of the switching bridge. When the bandwidth of the control signal is low compared to the switching frequency, the output voltage of the switching bridge is

$$u_o(t) = L \frac{di_L}{dt} + Ri_L + v_o \quad (2.21)$$

(Patel and Agarwal, 2008; Sun, 2011; Zhong and Hornik, 2013), where v_o is the output voltage. Taking the Laplace transform of (2.21) and rearranging the output voltage of the inverter yields

$$V_o(s) = U_o(s) - Z_o(s) \cdot I_L(s) \quad (2.22)$$

with

$$Z_o(s) = sL + R. \quad (2.23)$$

Note that in this case, the output capacitor is considered to be a part of the load as described in (Zhong and Hornik, 2013).

Looking at (2.23) and (2.22) when $|j\omega L| \gg R$ the inverter passive output impedance is mainly inductive. If R is large, the output impedance will be resistive but this is impractical as high output resistance will lead to a deterioration in efficiency.

Fig 2.11 shows a virtual impedance feedback using the inductor current measurement. Note that u_o is the average H-bridge output voltage. The duty cycle term u is calculated directly from u_o using (2.2) and fed into the modulator. From Fig 2.11

$$U_o(s) = V_o^*(s) - Z_v(s) \cdot I_L(s) \quad (2.24)$$

where $V_o^*(s)$ is the inverter desired internal voltage source and $Z_v(s)$ is the desired output impedance. Combining (2.22) and (2.24) and rearranging leads to

$$V_o(s) = V_o^*(s) - (Z_o(s) + Z_v(s)) \cdot I_L(s), \quad (2.25)$$

and the total output impedance of the inverter is the sum of the passive output impedance and the virtual impedance

$$Z_\Sigma(s) = Z_o(s) + Z_v(s) \quad (2.26)$$

In the case where $|Z_v(j\omega)| \gg |Z_o(j\omega)|$ the total output impedance $Z_\Sigma \approx Z_v$. In the case where pure lossless virtual resistance is desired, Z_v can be fixed into constant value. Capacitive and

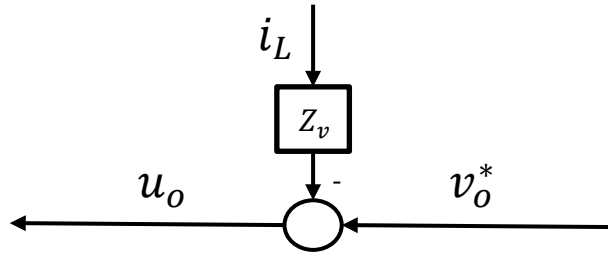


Fig 2.11 Controller designed to directly shape the inverter output impedance by feeding the inductor current.

inductive virtual impedances can be achieved by feeding back either the integral or the derivative of the inductor current.

This method has two main drawbacks, the first is the fact that the minimum virtual impedance magnitude is limited by the passive impedance and the second is that the output capacitor current is not taken into account.

2.5.2 The output impedance of a generic single degree of freedom closed-loop controlled power inverter

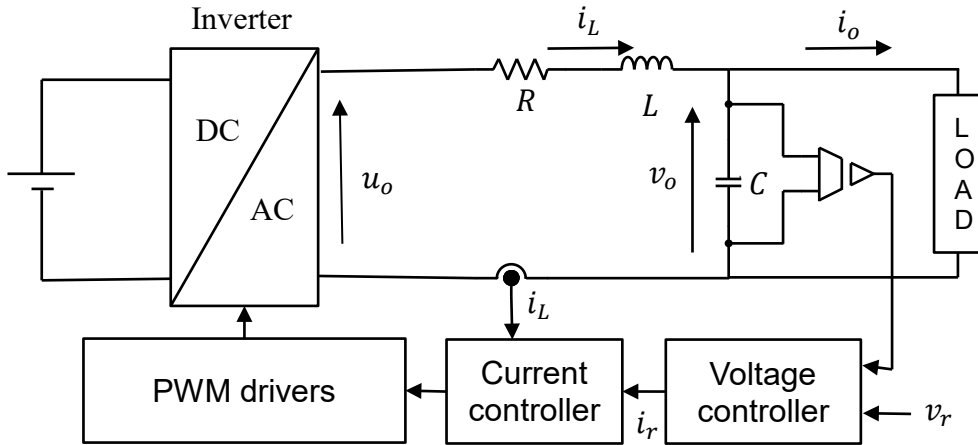


Fig 2.12 A schematic diagram of a dual-loop controlled inverter

Fig 2.12 shows the schematic diagram of a cascaded loop controlled inverter. This inverter contains a switching bridge followed by LC filter, and Fig 2.13 shows the model of a cascaded loop controlled inverter followed by an LC filter.

In a cascaded loop controlled inverter, the inductor current is used as a feedback for the current controller and

$$U_o(s) = C_I(s) \left(I_L^*(s) - I_L(s) \right). \quad (2.27)$$

where $C_I(s)$ is the current controller compensator and $I_L^*(s), I_L(s)$ are the inductor reference current and the measured current respectively. The voltage is regulated by setting the reference to the current regulated as

$$I_L^*(s) = C_V(s) \left(V_o^*(s) - V_o(s) \right). \quad (2.28)$$

where $C_V(s)$ is the voltage controller compensator and $V_o^*(s), V_o(s)$ are the output reference voltage and the output voltage respectively. Combining (2.27) with (2.28) yields,

$$U_o(s) = C_V(s) \cdot C_I(s) \left(V_o^*(s) - V_o(s) \right) - C_I(s) I_L(s). \quad (2.29)$$

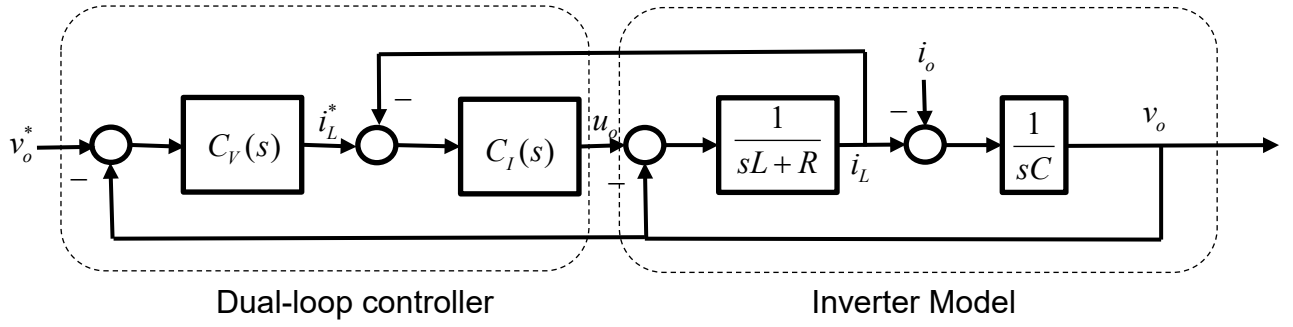


Fig 2.13 Model and control schematic of a cascaded loop controlled inverter

Comparing (2.29) to (2.24), it appears the cascaded loop control is a single closed loop control with an additional impedance term (He and Li, 2012), where C_I acts as the virtual impedance term Z_v . However, this is not the final impedance term as the inductor current **contains** both the load and output capacitance currents. Moreover, substituting (2.29) into (2.22) yields,

$$V_o(s) = \frac{C_V(s)C_I(s)}{1 + C_V(s)C_I(s)} V_o^*(s) - \underbrace{\frac{C_I(s) + Z_o(s)}{1 + C_V(s)C_I(s)}}_{Z_\Sigma} I_L(s), \quad (2.30)$$

which shows that the total output impedance Z_Σ yet depends on the filter passive impedance. In many cases, to simplify the design of the cascaded loop control, the outer loop is designed under the assumption that the current loop dynamics are faster than the voltage loop dynamics (Ying-Yu, 1995). Using this assumption the current and voltage loop can be decoupled in the frequency domain and tuned independently (Vilathgamuwa, Perera and Choi, 2002). In this case, well within the bandwidth limitation of the current closed-loop, it is possible to assume that

$$i_L^*(t) \approx i_L(t) . \quad (2.31)$$

where i_L^* is the current regulator reference signal. Taking (2.31) into account the simplified form of the output voltage is

$$V_o(s) = \frac{I_L^*(s) - I_o(s)}{sC} \quad (2.32)$$

where I_o is the inverter load current. Combining (2.32) with (2.28) yields,

$$V_o(s) = \frac{P_V(s)C_V(s)}{1 - P_V(s)C_V(s)} V_o^*(s) - \frac{P_V(s)}{1 - P_V(s)C_V(s)} I_o(s) , \quad (2.33)$$

where P_V is the voltage plant and

$$P_V = \frac{1}{sC}. \quad (2.34)$$

From (2.34) the total output impedance in low-bandwidth is

$$Z_{\Sigma}(s) = \frac{P_V(s)}{1 - C_V(s)P_V(s)}. \quad (2.35)$$

and the closed loop tracking transfer function is

$$T_V(s) = \frac{P_V(s)C_V(s)}{1 - P_V(s)C_V(s)} \quad (2.36)$$

In this type of design, the voltage tracking performance is coupled to the output impedance through C_V and the compensator design affect both the internal source and the output impedance. As a rule of thumb the voltage controller design bandwidth is limited to one-tenth of current controller closed loop bandwidth.

2.6 The effect of output impedance on the power quality at the inverter output

An equivalent circuit of a power inverter is shown in Fig 2.14. The output voltage of the inverter is

$$V_o(s) = V_o^*(s) - Z_{\Sigma}(s)I_o(s). \quad (2.37)$$

In the case where non-linear load is connected at the output of an inverter the expected steady-state current is

$$i_o = \sum_{n=1}^{\infty} I_n \sin(n\omega_0 t + \theta_n) \quad (2.38)$$

where ω_0 is the inverter output base (mains) frequency.

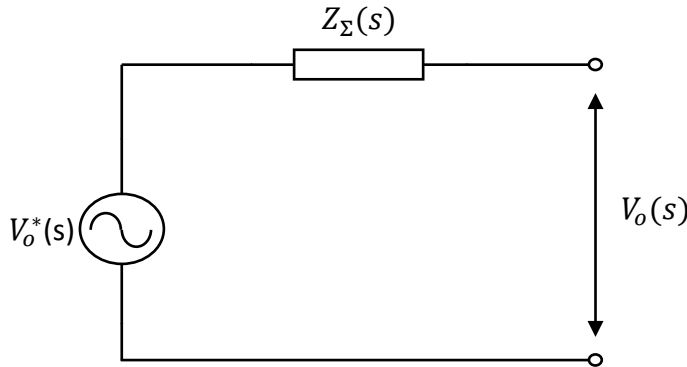


Fig 2.14 An equivalent circuit model of power inverter

Analysis of the effect of harmonic currents of a non-linear load on the output voltage can be done separately for each frequency (Zhong *et al.*, 2012; Zhong, 2013a). Therefore the output voltage of the inverter at each harmonic is

$$V_o(jn\omega_0) = V_o^*(jn\omega_0) - Z_\Sigma(jn\omega_0) \cdot I_o(jn\omega_0) \quad (2.39)$$

and the expected Total Harmonic Distortion is

$$THD_v(\%) = \frac{\sum_{n=2}^{\infty} |V_o(jn\omega_0)|}{|V_o(j\omega_0)|} \cdot 100\% \quad (2.40)$$

From (2.37-2.40) it is understood that the inverter output impedance plays a crucial role in the determination of the inverter output voltage THD.

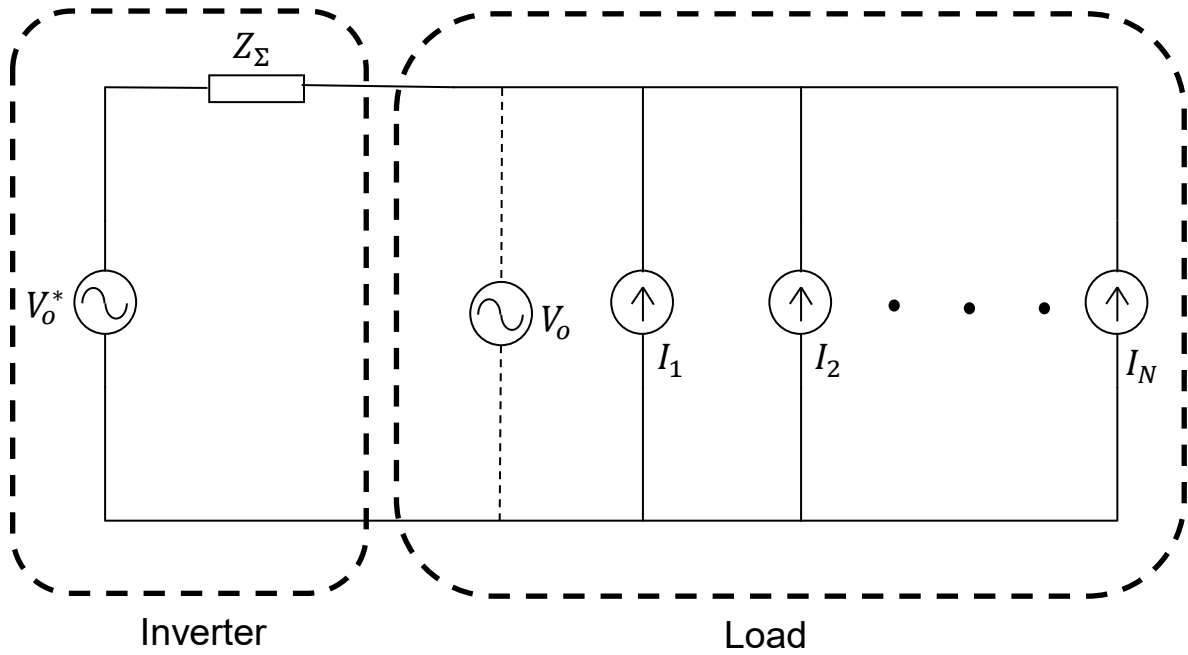


Fig 2.15 Model of inverter connected to a non-linear load

2.7 Overview of inverter control techniques

The voltage regulation of a power inverter is a fundamental design factor in the control of the power inverter. One of the common challenges is to maintain high power quality when loaded with non-linear loads. Many approaches have been proposed in the literature to regulate the output voltage quality and improve its quality. The main approaches are reviewed in the follows.

2.7.1 Proportional-resonant control

In the case of power inverters, the controller has to both track and reject sinusoidal signals. Straightforward use of PI controller is not possible as this will lead to both steady-state tracking

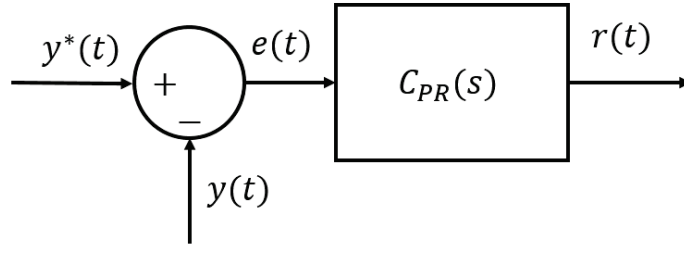


Fig 2.16 Schematic diagram of proportional resonant compensator

error and limited disturbance rejection. This is due to a finite gain in the fundamental frequency (Yuan *et al.*, 2002; Blaabjerg and Chen, 2006). A schematic diagram of PR controller is shown in Fig. 2.16 where $y^*(t)$ is the output reference, $y(t)$ is the output signal, $e(t)$ is the error signal and $r(t)$ is the controller output. The PR controller for single frequency is derived from the generalized integrator theory as follows.

Consider the error signal

$$e(t) = A \sin(\omega t) \quad (2.41)$$

where ω is the frequency of the sinusoidal signal to track, similarly to integral controllers for direct signal, the desired output of the controller is the amplitude integration of the error input (Yuan *et al.*, 2002) e.g.

$$r(t) = A \cdot t \sin(\omega t) \quad (2.42)$$

The Laplace transforms of (2.41) and (2.42) are,

$$E(s) = A \frac{\omega}{s^2 + \omega^2} \quad (2.43)$$

$$R(s) = A \frac{\omega s}{(s^2 + \omega^2)^2} \quad (2.44)$$

The desired resonant compensator $C_R(s)$ is derived by dividing (2.44) by (2.43),

$$C_R(s) = \frac{R(s)}{E(s)} = \frac{s}{s^2 + \omega^2} \quad (2.45)$$

The PR compensator is a combination of proportional gain and a generalized integrator its term is given by

$$C_{PR}(s) = K_P + K_r \frac{s}{s^2 + \omega^2} \quad (2.46)$$

where K_P is the proportional gain and K_r is the generalized integrator gain. These design parameters should be chosen with accordance to the stability limits and the desired tracking and disturbance rejection performance (Kuperman, 2015). In the case where the disturbance

or the signal to track is expected to contain harmonics (2.46) becomes a multi-resonant compensator of the form

$$C_{PR}(s) = K_P + \sum_{h=1}^N K_{rh} \frac{s}{s^2 + (\omega h)^2} \quad (2.47)$$

where h is the harmonic order and N is the number of parallel resonant compensators (Timbus, Teodorescu, *et al.*, 2006). In the literature, these type of controllers are implemented in a single degree of freedom which leads to coupling between disturbance rejection and tracking performance in a similar way to the coupling shown in section 2.5.2 In this thesis a two degrees of freedom multi-resonant type controller is proposed in chapter 4. It is worth to note that this type of controllers are sensitive to frequency deviations. Adaptive mechanism are reported in the literature (Timbus, Ciobotaru, *et al.*, 2006). However those are changing the compensator parameters in accordance with the frequency variations. A two degrees of freedom frequency robust multi-resonant controller is proposed in chapter 5 of this thesis.

2.7.2 Repetitive control

The repetitive controller is based on the internal model principle (Bin Zhang *et al.*, 2008; Hornik and Zhong, 2010b). The fundamental idea is that the compensator is made of a positive feedback inner loop consists of a low-pass filter cascaded with a single period delay. In this way, the compensator gain is close to infinite at the multiples of the delay frequency within the bandwidth of the low-pass filter. From Fig 2.17 The transfer function of the repetitive compensator is

$$C_{RP}(s) = \frac{1}{1 - W(s)e^{-\tau_d s}} \quad (2.48)$$

where $W(s)$ is a low pass filter designed to limit the compensator bandwidth and to increase the system stability. Following (2.48) the poles of the compensator $C_{RP}(s)$ are the solution of

$$W(j\omega) = e^{-j\omega\tau_d} \quad (2.49)$$

In (Zhong and Hornik, 2013) it is shown that when $W(s)$ is chosen as first order low-pass filter, the compensator poles can be approximated using the Lambert function presented in (Corless *et al.*, 1996) and that the delay time is chosen by the pole approximation. In chapter 6 of this thesis it is shown that in the general case of choosing $W(s)$ as an n-th order low pass filter, the time delay can be chosen so that the sum of the filter delay and the repetitive delay will add up to a single period delay at the fundamental frequency for the rejection of all the harmonics up to the bandwidth of the filter $W(s)$ or to half a period delay for the rejection of odd harmonics (Costa-Castello, Grino and Fossas, 2004; Zhou *et al.*, 2006).

This type of controller shows good results when the frequency is constant. However, they are highly sensitive to frequency variations. Methods to improve the robustness of this type of control includes adaptive mechanism which updates the internal filter with accordance to variations in the fundamental frequency (Hornik and Zhong, 2010a) and using high order repetitive control (Ramos, Costa-castello and Josep, 2015). However, the update of the internal filter requires the measurement or computations of the frequency and the proposed high order repetitive controllers be of a single degree of freedom structure which leads to a coupling between tracking performance to disturbance rejection performance. A two degrees of freedom multiple delay repetitive type controller is proposed in chapter 7 of the thesis.

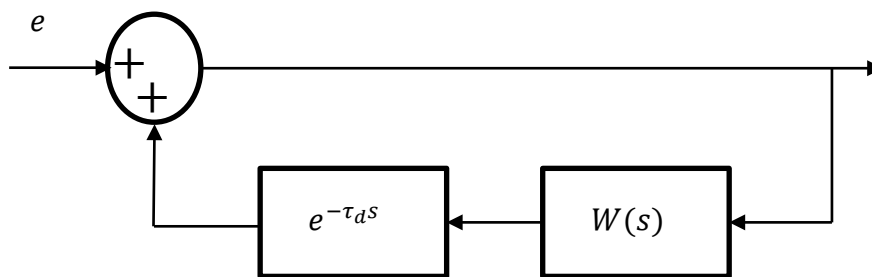


Fig 2.17 Schematic diagram of repetitive compensator

2.7.3 Other control methods

Hysteresis control is one of the simplest non-linear controllers, it is mainly used to regulate the inverter inductor current (Kang and Liaw, 2001; Krismadinata, Rahim and Selvaraj, 2007). The main idea behind it is to create a hysteresis band for the inductor current which switches the voltage between $-V_{DC}$ to V_{DC} in order to keep the current within the hysteresis band by using a simple control law. The hysteresis band is divided to an upper band and a lower band when the current crosses the upper band then the inverter bridge is switched to $-V_{DC}$ and when the current crosses the lower band then the inverter bridge is switched to V_{DC} . The upper band is usually the reference current plus a margin value and the lower band is the reference current minus a margin value.

Sliding mode control is one the most common non-linear controllers applied in power inverters (Tai and Chen, 2002; Kukrer, Komurcugil and Doganalp, 2009; Komurcugil *et al.*, 2016). The main idea behind it is to define a sliding surface within the state phase plane and switch between the inverter bridge discrete states accordingly. Among its strongest points are simple implementation and robustness to both disturbances and parameter variations. However,

varying switching frequency, chattering around the sliding surface are among its drawbacks and might prevent it from being used for inverter control in industrial applications.

A Lyapunov based approach has been proposed by (Komurcugil *et al.*, 2015) has shown good results, yielding low THDs which suggests that the method output impedance is low. However, the approach is directly measuring the inverter load current, and hence a feedforward approach may achieve similar results.

A deadbeat control for single phase power inverters is proposed in (Kawamura, Chuarayapratip and Haneyoshi, 1988; Mohamed and El-Saadany, 2008; Zeng and Chang, 2008) This control method guarantees the convergences of the closed-loop system within a finite time. However, the method heavily depends on the knowledge of the inverter parameters and sensitive to system parameter uncertainties (Timbus *et al.*, 2009).

A model predictive control which includes an estimation of the output current has been proposed for three-phase inverter in (Cortes *et al.*, 2009). This controller optimizes the next switching sequence to minimize the tracking error. However, the assumption that the load current has no dynamics can lead to a good result only at a very high PWM and sampling frequency, and the controller has to solve an optimization problem at each switching cycle which may suggest a need for an high-performance microcontroller.

2.8 Disturbance observer based design

The majority of controlled systems contain uncertainties in their models, disturbances and noise inputs. In the case where the disturbance is measurable, it can be fed forward to the control signal to suppress its impact on the system output. However, in many cases, the disturbance input to the controller cannot be measured for various reasons.

Single degree of freedom controllers have many design targets to meet such as stability, tracking performance, disturbance rejection, and robustness. Over the years disturbance observer based design has been developed independently for different applications (Chen *et al.*, 2016). This observer can be divided into two main types; the first type considers the disturbance as an unknown input and the second is an extended state observer, where the disturbance observer is modeled as a system state.

The main reason for using the two degrees of freedom design is that the decoupling between the disturbance rejection and the tracking performance makes it a straightforward method for designing a separate disturbance rejection and tracking controller. Moreover in the case of inverters the reference has energy in the base frequency but the disturbance may contain

energy in both the base frequency and its multiplies. This makes two degrees of freedom design even more attractive for inverter control.

2.8.1 Frequency domain design of disturbance observer

The frequency domain design of the disturbance observer has been proposed by (Ohishi, 1983)² and described in (Oboe, 2018). The fundamental idea in it, is that the lumped disturbance which contains the disturbance input uncertainty and noise, can be estimated as long as they are bandwidth limited signals.

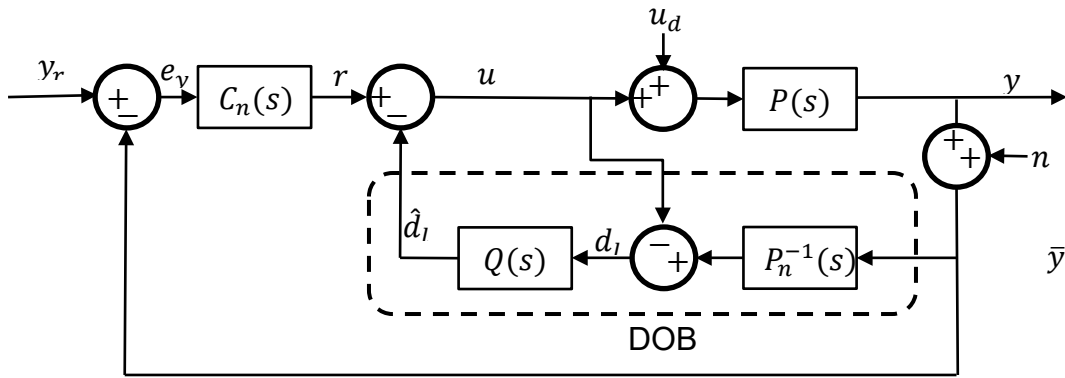


Fig 2.18 Control diagram of disturbance observer based controller

Fig 2.18 shows a schematic diagram of disturbance observer two degrees of freedom control. $P(s)$ and $P_n(s)$ are the true plant and the nominal plant, $C_n(s)$ is the nominal compensator and $Q(s)$ is a low-pass filter and u is the system input. In this control method u_d represents the lumped disturbance. The lumped disturbance contains three elements; the nominal model mismatch, the measurement noise and the disturbance input and equals to

$$U_d(s) = \Delta P(s)Y(s) + D(s) + P_n^{-1}(s)N(s). \quad (2.50)$$

where,

$$\Delta P(s) = P_n^{-1}(s) - P^{-1}(s), \quad (2.51)$$

and represents the model uncertainty and $N(s)$ is the measurement noise. Since u_d is not causal, the disturbance observer output approximates u_d by passing it through a the low pass filter $Q(s)$ and

$$\hat{U}_d(s) = Q(s) \cdot U_d(s). \quad (2.52)$$

² The source article is in Japanese

The output of the system is

$$Y(s) = (U(s) + D(s)) \cdot P(s) \quad (2.53)$$

Combining (2.50-2.53) yields,

$$Y = \frac{P \cdot P_n}{P_n(1-Q) + P} \cdot R + \frac{P_n \cdot P \cdot (1-Q)}{P_n(1-Q) + P} \cdot D + \frac{P \cdot P_n \cdot Q}{P_n^2(1-Q) + P \cdot P_n} \cdot N, \quad (2.54)$$

and in the frequency range where $Q(j\omega) \approx 1$ (2.54) reduces to

$$Y(s) = P_n(s) \cdot R(s) + N(s) \quad (2.55)$$

which is the nominal system. The nominal controller $C_n(s)$ can then be designed in accordance with the desired tracking performance.

2.8.2 Uncertainty and Disturbance Estimator

The UDE was first proposed in (Sanz *et al.*, 2016). The UDE is an improvement of the Time Delay Control (TDC) developed by (Youcef-Toumi and Ito, 1990) which uses a time delay to estimate the non-causal derivatives of the inverse system. The fundamental idea behind it is to force the controlled system to have a nominal system dynamics. The design of the UDE is proceeds as follows.

Consider a linear system of the form

$$\dot{x} = (A_n + \Delta A)x + (B_n + \Delta B)u + d \quad (2.56)$$

where A_n and B_n denotes the nominal system and ΔA and ΔB are the model uncertainties (equivalent to ΔP in 2.51). The lumped disturbance and uncertainty is

$$u_d = \Delta Ax + \Delta Bu + d \quad (2.57)$$

which can be derived as

$$u_d = \dot{x} - A_n x - B_n u. \quad (2.58)$$

However, \dot{x} is not implementable due to causality issues hence the estimated disturbance is

$$\hat{u}_d(t) = u_d \star g_u \quad (2.59)$$

where g_u is the impulse response of the stable filter $G_u(s)$, which is similar to DOB design just in the time domain. The UDE implementation has two constraints, the first is that all the system states have to be known or measurable and the second is that the system has to be in canonical form due to the pseudo inverse operation on the control law (Sanz *et al.*, 2016) more details on the UDE approach can be found at chapter 3 of this thesis.

2.8.3 Extended State Observer

The Extended State Observer (ESO) is an extension of the classic state observer to estimate both the unmeasurable states of the system and all the states of the disturbance dynamics. Under certain conditions, a disturbance can be observed in cases where the disturbance is expected to satisfy a known n -th order ordinary linear differential equation (Johnson, 1970).

Consider a linear system of the form

$$\begin{aligned}\dot{x} &= A_n x(t) + B_n (u(t) + d(t)) \\ y &= C_n x(t)\end{aligned}\quad (2.60)$$

where A_n and B_n are the state and input matrices and C_n is the output vector. Under the assumption that the disturbance dynamics can satisfy a known linear differential equation, the disturbance dynamics can be modeled by the following exogenous system,

$$\begin{aligned}\dot{w}(t) &= Ww(t) \\ d(t) &= Vw(t)\end{aligned}, \quad (2.61)$$

where w is a vector representing the disturbance internal states and W and V are the disturbance model state and output matrices respectively. Augmenting (2.61) with (2.60) to a combined system yields,

$$\begin{aligned}\dot{z}(t) &= A_T z(t) + B_T u(t) \\ y(t) &= C_T z(t)\end{aligned}\quad (2.62)$$

where,

$$z(t) = [x(t) \quad w(t)]^T, A_T = \begin{bmatrix} A_n & B_n V \\ 0 & W \end{bmatrix}, B_T = [B_n^T \quad 0]^T, C_T = [C_n \quad 0] \quad (2.63)$$

Further assuming that both $(W, B_0 V)$ and (A_T, C_T) are observable (Guo and Chen, 2005), the following extended observer is designed as

$$\begin{aligned}\dot{\hat{z}}(t) &= A_T \hat{z}(t) + B_T u(t) + K_L (\hat{y}(t) - y(t)) \\ \hat{y}(t) &= C_T \hat{z}(t)\end{aligned}, \quad (2.64)$$

where $\hat{z}(t) = [\hat{x}(t) \quad \hat{w}(t)]^T$ and K_L is the observer gain. From (2.61-2.63) the disturbance is estimated as

$$\hat{d}(t) = [0 \quad V] \cdot \hat{z}(t). \quad (2.65)$$

The ESO estimation error is

$$e_z(t) = z(t) - \hat{z}(t). \quad (2.66)$$

and the error dynamics are

$$\dot{e}_z(t) = (A_T - K_L C_T) e(t) \quad (2.67)$$

Assuming that the pair (A_n, B_n) is controllable the extended disturbance observer control law is

$$u(t) = -\hat{d}(t) + K_I \int_0^t (x^*(\tau) - \hat{x}(\tau)) d\tau + K_P (x^*(t) - \hat{x}(t)) \quad (2.68)$$

where K_P is the proportional state feedback gain K_I is the integral state feedback gain and x^* is the state reference. It is interesting to note that in the case where all the system states are known the functionality of the extended state observer is the same as that of the disturbance observer in the sense that the design includes the determination of the disturbance dynamics as in eq. (2.61) and a nominal controller as in eq. (2.68). Furthermore, the requirement for the disturbance dynamics to be known is in some sense equivalent to the requirement of the UDE and DOB methods for the disturbance to be included in the bandwidth of their filter, e.g. for $Q(s) \approx 1$ at the expected disturbance bandwidth.

2.9 Conclusion

In this chapter it has been discussed that one of the best solutions for designing an inverter controller where both the inverter internal EMF and output impedance are designed separately is to use a two degrees of freedom controller. However, DOB based two degrees of freedom controllers in the existing literature are designed to observe and therefore reject disturbances with either slow varying dynamics or in some cases periodical containing single harmonic. The main body of the thesis shows several novel two degrees of freedom controller designs for rejecting periodical disturbances and tracking periodical signals.

The next chapter shows the impact of the inverter output impedance on harmonic power sharing in parallel operation of inverters and superiority of UDE based design over using the inverter inductor current as a feedforward term. Chapter 4 shows a multi resonant implementation of UDE to estimate and reject harmonic disturbances. Chapter 5 shows frequency a robust design of UDE controller to reject periodical disturbances with varying period times. Chapter 6 shows combined design of time-delay UDE filter with resonant tracking controller and chapter 7 shows design containing multiple delays to reject periodical disturbance with varying period times. The thesis is concluded at chapter 8 with directions for future work.

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3. Preliminary Studies on Application of UDE to Power Inverter Control

3.1 Introduction

Power electronics are essential to integrate renewable energy sources, storage equipment and Uninterruptable Power Supply (UPS) systems to the grid. The operation of power inverters plays a key role in modern micro-grids (Lasseter, 2002) and emerges several challenges, i.e. to keep the system stable, to maintain high output voltage quality and to be able to define the closed loop virtual impedance for different applications such as parallel operation (Guerrero, Vicuña, Garc'ia, Matas, Castilla and Miret, 2005; Guerrero, Matas, De Vicuña, Castilla and Miret, 2006), oscillation damping (Lazzarin, Bauer and Barbi, 2013), fault current limiting (Paquette and Divan, 2015; Konstantopoulos, Zhong and Ming, 2016).

Limiting the magnitude of an inverter impedance is essential in order to maintain low voltage THD at the inverter output and to bypass the harmonic currents. In the literature, various methods have been proposed for inverters connected to a load to bypass harmonic currents and maintain high power quality at the output of the inverter. Since power quality improvement is of major importance, Proportional Resonant (PR) controllers have been designed and represent a well-established method where a voltage feedback is used for compensating the harmonic current (Castilla, Miret, Matas, de Vicuna and Guerrero, 2009). However, the PR method is not robust to deviations in the fundamental frequency (Hornik and Zhong, 2011) and requires high computational power, which results from the need of separate parallel compensators for each harmonic. Another method for compensating harmonic currents is to add an integration of the current feedback to the voltage signal. This method creates a closed loop capacitive output impedance to compensate the harmonic currents (Zhong and Zeng, 2014) but may suffer from instability issues in the presence of inductive loads and is only capable to compensate for a single harmonic. Moreover, as shown in chapter 2 direct shaping of the inverter output impedance using the inductor feedback is limited by the natural output impedance of the system.

The knowledge of output impedance is also crucial for load sharing. One of the key issues in parallel operation of inverters is to share the load current proportionally to the inverter size (Zhong, 2013; Zhong and Hornik, 2013). Many methods for achieving this goal are based on the droop controller (Tuladhar, Jin, Unger and Mauch, 1997, 2000; Zhong, 2013). However, those are heavily dependent on the knowledge of the output impedance. Moreover, classic droop controllers are used as a form of PLL used for power sharing in the fundamental

frequency (Zhong and Boroyevich, 2013) and in the absence of harmonic current regulation the harmonic current sharing is expected to be related to the inverter output impedance.

In this chapter a UDE based virtual impedance scheme is proposed. In (Zhong, Kuperman and Stobart, 2011) it has been proven that using the UDE control strategy, the closed-loop system has two degrees of freedom, and therefore the virtual impedance can be shaped as part of the controller design. Moreover, the output impedance can be shaped to be lower than the output LC filter impedance to improve the output power quality. It is also shown that the use of UDE for voltage regulation can shape and reduce the virtual output impedance of the inverter. The reduction of the output impedance is demonstrated through a comparison to inductor feedforward method and the output impedance accuracy is demonstrated by the current distribution of parallel operating inverters.

3.2 UDE Overview

The UDE controller uses an estimation of the model deviation and of the external disturbance by calculating them from the nominal model equations (Zhong, Kuperman and Stobart, 2011). To further explain this, consider the linear, time-invariant plant

$$\dot{x}(t) = A_n x(t) + B_n u(t) \quad (3.1)$$

where $x(t) = [x_1(t) \cdots x_n(t)]^T \in \mathfrak{R}^n$ is the state vector and $u(t) \in \mathfrak{R}^m$ denotes the input. The deviated dynamics associated with (3.1) are described by

$$\dot{x}(t) = (A_n + \Delta A)x(t) + (B_n + \Delta B)u(t) + d(t) \quad (3.2)$$

where ΔA , ΔB are the model deviation from the nominal matrices A_n and B_n respectively and $d(t)$ is the disturbance. Let

$$\dot{x}_m(t) = A_m x_m(t) + B_m \tilde{c}(t) \quad (3.3)$$

be the desired reference tracking model where $[x_{m1}(t) \cdots x_{mn}(t)]^T \in \mathfrak{R}^m$ is the desired state and $\tilde{c}(t)$ is the command signal. According to (Zhong, Kuperman and Stobart, 2011), defining the error as $e = x_m - x$ and forcing the error dynamics as $\dot{e} = A_m e$ the desired tracking can be achieved using the control law

$$Bu(t) = A_m x(t) + B_m \tilde{c}(t) - A_n x(t) - \hat{u}_d(t) \quad (3.4)$$

with \hat{u}_d defined as

$$\hat{u}_d(t) = g_U(t) \star u_d(t) \quad (3.5)$$

where $g_U(t)$ is an impulse response of a low-pass filter, $u_d(t)$ is the lumped uncertainty and disturbance and

$$u_d(t) = \Delta Ax(t) + \Delta Bu(t) + d(t) = \dot{x}(t) - Ax(t) - Bu(t) \quad (3.6)$$

If the following criterion holds (Zhong and Rees, 2004):

$$[I - B \cdot B^+] \cdot [A_m X + B_m \tilde{c}(t) - A_n X - \Delta AX - d(t)] = 0 \quad (3.7)$$

where B^+ is the pseudo inverse of B , then according to (Zhong, Kuperman and Stobart, 2011) the reference is tracked. Note that if B is square invertible matrix, then the condition is always satisfied. Defining

$$H_m(s) = (sI - A_m)^{-1} B_m, \quad (3.8)$$

the controlled state of (3.1) can be written as in (Zhong, Kuperman and Stobart, 2011)

$$X(s) = H_m(s) \tilde{C}(s) + H_d(s) B \cdot B^+ U_d(s) \quad (3.9)$$

where $X(s)$ is the Laplace transform of $x(t)$ and

$$H_d(s) = (sI - A_m)^{-1} (1 - G_U(s)). \quad (3.10)$$

A closer look at (3.9) shows that indeed, using the UDE strategy, the disturbance rejection is decoupled from the reference tracking through the design of $G_U(s)$.

3.3 Proposed cascaded controller

The proposed controller forms a cascaded as shown in Fig 3.1. The inner loop controls the inverter current i_L by regulating the duty-cycle. The outer loop controls the capacitor voltage

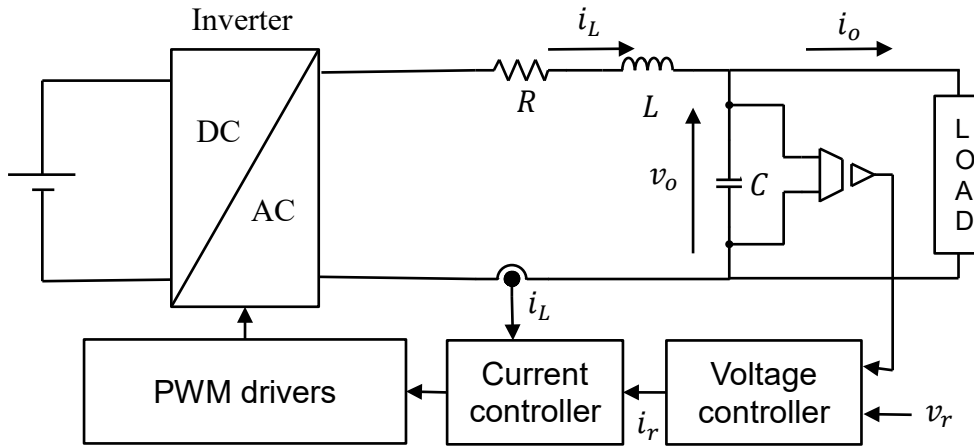


Fig 3.1 Cascaded control structure

v_o , by regulating the inner loop reference. The capacitor voltage is the system output. Since the inverter voltage is implemented digitally, the internal delays of the PWM must be taken into

account. The main task of the current loop design is to achieve a very high bandwidth in order to consider it as a unity-gain loop (Maffezzoni, Schiavoni and Ferretti, 1990).

Because of the high bandwidth required for the current control loop, the PWM and digital control time delays should be taken into account. In order to minimize these incorporated delays, an asymmetric PWM method has been adopted (Deng, Oruganti and Srinivasan, 2005). In this method, the PWM comparator register is updated twice in each switching cycle. The first update is at the beginning of the cycle, determining the transistor ON time and the second is when the counter reaches the maximum. The second time determines the transistor OFF time. This results in the PWM update frequency being double the switching frequency. More information about the modulation technique can be found in section 2.3.2.

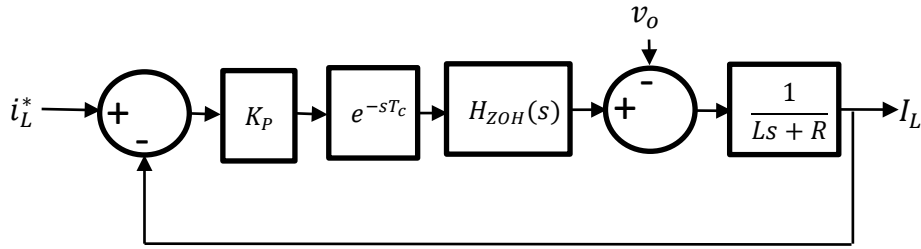


Fig 3.2 Current loop diagram

3.3.1 Current compensator design

Figure 3.2 shows the closed loop model of the current controller with a proportional compensator. This model incorporates the PWM modulation model represented by $H_{ZOH}(s)$, the control time delay represented by e^{-sT_c} and the filtering process represented by $G_{LC}(s)$. The PWM is approximated as Zero Order Hold (ZOH) (Buso and Mattavelli, 2015), the ZOH is defined in the s-domain as

$$H_{ZOH}(s) = \frac{1 - e^{-sT_{PWM}}}{s} \quad (3.11)$$

where T_{PWM} is the PWM delay and depends on both the modulation technique and switching frequency. The transfer function from the inverter H-bridge voltage to the inductor current is

$$\frac{I_L(s)}{U_o(s)} = \frac{1}{Ls + R} \quad (3.12)$$

In a bandwidth much lower than the PWM frequency the ZOH piecewise signal can be approximated as continuous and

$$P_I(s) = \frac{1}{Ls + R} \quad (3.13)$$

and when choosing the current compensator to be

$$C_I(s) = K_P, \quad (3.14)$$

the inductor closed loop transfer function becomes,

$$I_L(s) = \frac{K_P}{R + K_P} \cdot \frac{1}{\frac{L}{R + K_P} s + 1} I_L^*(s) - \frac{1}{R + K_P} \cdot \frac{1}{\frac{L}{R + K_P} s + 1} V_o(s) \quad (3.15)$$

where K_P is the current compensator static gain and for PI control of the form

$$C_I(s) = K_{PI} \frac{1 + \tau_I s}{s}, \quad (3.16)$$

the inductor current is

$$I_L(s) = \frac{1 + \tau_I s}{\frac{L}{K_{PI}} s^2 + \left(\frac{\tau_I K_{PI} + R}{K_{PI}} \right) s + 1} I_L^*(s) - \frac{1}{K_{PI}} \cdot \frac{s}{\frac{L}{K_{PI}} s^2 + \left(\frac{\tau_I K_{PI} + R}{K_{PI}} \right) s + 1} V_o(s) \quad (3.17)$$

More information about proportional current compensator design considering the PWM model is in section 2.4.

3.3.2 Modelling the inverter voltage plant for UDE control design

The voltage loop design starts from modelling the output voltage dynamics. Looking at Figure 3.1, the dynamics are described from

$$C \frac{dv_o}{dt} = i_L - i_o \quad (3.18)$$

In a more accurate model, the output impedance of the current loop is represented as a parallel branch to the current source (Wang, Hu, Yuan and Sun, 2015). In the case of a proportional controller, the output admittance branch is derived from (3.15) as

$$Z_I^{-1}(s) = \frac{I_L(s)}{V_o(s)} = \frac{1}{R + K_P} \cdot \frac{1}{\frac{L}{R + K_P} s + 1} \quad (3.19)$$

and in the case of PI control its derived from (3.17) as

$$Z_I^{-1}(s) = \frac{I_L(s)}{V_o(s)} = \frac{1}{K_{PI}} \cdot \frac{s}{\frac{L}{K_{PI}} s^2 + \left(\frac{\tau_I K_{PI} + R}{K_{PI}} \right) s + 1} \quad (3.20)$$

For proportional controller, in the low frequency range where $\omega \ll \frac{R + K_P}{L}$, the output admittance of the closed loop current regulator is approximated to be resistive with

$$R_I = R + K_P, \quad (3.21)$$

and for PI control, in the low frequency range where $\omega \ll \sqrt{\frac{K_{PI}}{L}}$ the output admittance can be considered capacitive with

$$X_I = \frac{K_{PI}}{\omega}. \quad (3.22)$$

when K_{PI} is sufficiently large the output admittance of the current regulator can be considered as infinite. However, in most cases it should be considered as a parallel capacitive impedance to the output. The equivalent circuit of the current close loop with proportional controller is shown in Figure (3.3a).

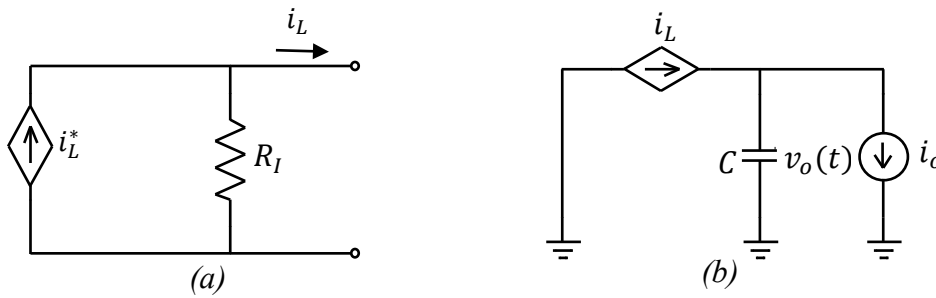


Fig 3.3 Equivalent circuits of (a) the current closed loop (b) The voltage plant

From figure (3.3b)

$$i_L = i_L^* - \frac{v_o}{R_I}. \quad (3.23)$$

Combining (3.23) with (3.18) yields

$$\dot{v}_o(t) = -\frac{1}{CR_I}v_o(t) + \frac{1}{C}i_L^*(t) - \frac{1}{C}i_o(t) \quad (3.24)$$

which is a first order model in the form of (3.2) where v_o is the controlled state, i_L^* is the control input, i_o is the disturbance and

$$A_n = -\frac{1}{R_I C}, B_n = \frac{1}{C}, d(t) = -\frac{1}{C}i_o(t) \quad (3.25)$$

In the case where R_I sufficiently large or when the system is controlled by PI and is well within the current regulator bandwidth A can be considered as 0 and the current regulator admittance can be considered as part of the unknown part of ΔA .

3.4 UDE based voltage controller design

To adjust the tracking performance a first order reference model is used as

$$\dot{x}_m(t) = -\omega_{bw}x_m(t) + \omega_{bw}v_o^*(t) \quad (3.26)$$

where ω_{bw} is the bandwidth of the tracking controller for the inverter and v_r is the reference voltage to track. To achieve suitable tracking performance, the tracking bandwidth should be higher than the reference signal bandwidth.

From (3.4) and (3.5) the resulting control law for the system in the s-domain is

$$I_L^*(s) = \frac{C \cdot \omega_{bw}}{1 - G_U(s)} V_o^*(s) - \frac{C(\omega_{bw} + G_U(s) \cdot s)}{1 - G_U(s)} V_c(s) + C \underbrace{\frac{1}{C \cdot R_L}}_{A_n} V_o(s), \quad (3.27)$$

where $G_U(s)$ is a LPF as in (3.5) and I_L^* is the current reference. Note that A_n depends on the design. The output voltage is derived from (3.9), (3.10) and (3.23) as

$$V_c(s) = \frac{\omega_{bw}}{s + \omega_{bw}} V_o^*(s) - \frac{1 - G_U(s)}{C(s + \omega_{bw})} I_o(s) \quad (3.28)$$

Looking at (3.26) the output of the UDE controlled inverter can be modelled as an EMF source connected in series with its output impedance and the output voltage can be rewritten as

$$V_c(s) = E(s) - I_o(s)Z_o(s) \quad (3.29)$$

where $E(s)$ is the internal EMF source of the inverter. From (3.28) and (3.29) it follows that

$$E(s) = \frac{\omega_{bw}}{s + \omega_{bw}} V_o^*(s) \quad (3.30)$$

and the closed loop output impedance is

$$Z_o(s) = \frac{1 - G_U(s)}{C(s + \omega_{bw})} \quad (3.31)$$

Note that $Z_o(s)$ is decoupled from the tracking performance by $G_U(s)$. $G_U(s)$ can be shaped according to (Kuperman, Zhong and Stobart, 2010) to meet the desired output impedance.

3.6 UDE filter design for reducing the output impedance

For the case of reduction of the inverter output impedance, the UDE filter is chosen to both shape the output impedance magnitude and to balance the characteristics between resistive and inductive impedance. This is done by choosing the UDE filter as

$$G_U(s) = \frac{\omega_U \cdot k_U}{s + \omega_U}, k_U \in [0,1] \quad (3.32)$$

From (3.31) the output impedance of the inverter becomes

$$Z_o(s) = \frac{s + \omega_U(1 - k_U)}{C(s + \omega_{bw})(s + \omega_U)} \quad (3.33)$$

At low frequencies where $\omega \ll \omega_U$ and $\omega \ll \omega_{bw}$

$$Z_o(j\omega) \approx \frac{j\omega}{C\omega_{bw}\omega_U} + \frac{1 - k_U}{C\omega_{bw}}. \quad (3.34)$$

Therefore, X_o can be approximated as

$$X_o = \frac{\omega}{C\omega_{bw}\omega_U} \quad (3.35)$$

and R_o can be approximated as

$$R_o = \frac{1 - k_U}{C\omega_{bw}}. \quad (3.36)$$

Equation (3.35) and (3.36) shows that the tuning of ω_{bw} and k_U defines both the output impedance magnitude and characteristics (e.g. inductive or resistive). Note that ω_{bw} and ω_U are bounded by the stability margins which are determined by the time-delay and bandwidth of the closed-loop current controller.

3.7 UDE filter design for parallel operation

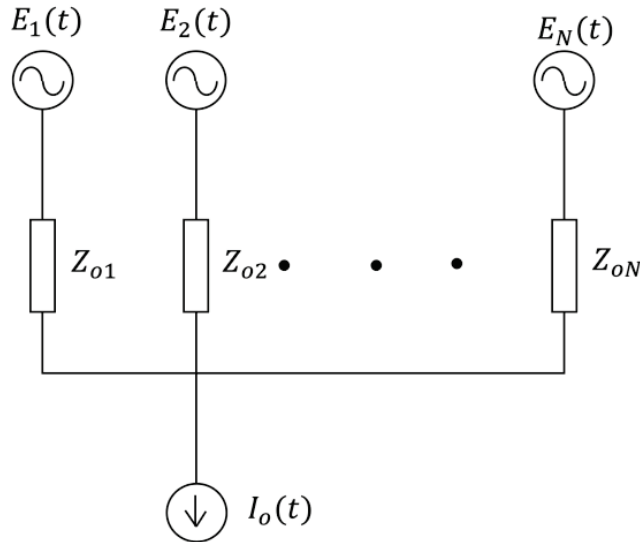


Fig 3.4 Equivalent circuit of N inverters connected in parallel.

Figure 3.4 shows the equivalent circuit of N inverters connected in parallel. It is clear that if the EMF of each unit is identical in phase and amplitude, the current sharing between the inverters depends on the internal impedance as described by the equation

$$I_i(jn\omega_0) = \frac{Z_{oi}^{-1}(jn\omega_0)}{\sum_{i=1}^N Z_{oi}^{-1}(jn\omega_0)} I_o(jn\omega_0) \quad (3.37)$$

where $n\omega_0$ is the relevant harmonic angular frequency and $Z_{oi}^{-1}(jn\omega_0)$ is the inverter admittance at the relevant harmonic frequency. To cancel the pole created by the tracking controller k_U is chosen as

$$k_U = 1 - \frac{\omega_{bw}}{\omega_U} \quad (3.38)$$

and the UDE filter becomes

$$G_U(s) = \frac{\omega_U - \omega_{bw}}{s + \omega_U}. \quad (3.39)$$

Substituting (3.39) to (3.33) yields the output impedance

$$Z_o(s) = \frac{1}{C(s + \omega_U)} \quad (3.40)$$

where (3.40) is the final form of the inverter output impedance. Consider N parallel inverters where the output capacitor of each inverter is $C_i, i = 1 \dots N$ and the filter bandwidth of each inverter is $\omega_{Ui}, i = 1 \dots N$. The output admittance of each inverter is

$$Z_{oi}^{-1}(s) = C_i(s + \omega_{Ui}) \quad (3.41)$$

which is the inverse of (3.38). The total system output admittance is

$$\sum_{i=1}^N Z_{oi}^{-1}(s) = (C_1 + \dots + C_N)s + (C_1 \cdot \omega_{U1} + \dots + C_N \cdot \omega_{UN}) \quad (3.42)$$

and the relative output impedance of each unit is

$$\frac{Z_{oi}^{-1}(s)}{\sum_{i=1}^N Z_{oi}^{-1}(s)} = \frac{C_i(s + \omega_{Ui})}{(C_1 + \dots + C_N)s + (C_1 \cdot \omega_{U1} + \dots + C_N \cdot \omega_{UN})}. \quad (3.43)$$

Consider ω_{max} to be the maximum expected significant harmonic frequency, if the constraint

$$\min(\omega_{Ui}) \gg \omega_{max} \quad (3.44)$$

is satisfied, then the current ratio of two parallel units can be evaluated as

$$\frac{I_i}{I_j} \approx \frac{C_i \omega_{Ui}}{C_j \omega_{Uj}}, \quad i = 1, \dots, N, \quad j = 1 \dots N, \quad j \neq i. \quad (3.45)$$

3.8 Simulation results

3.8.1 Standalone operation

In order to demonstrate this method, a voltage source inverter followed by an LC filter is simulated. The non-linear load consists of a rectifier followed by a capacitor and a resistive load, the capacitor size is $570\mu F$ and the output resistor is 100Ω . The parameters of the system can be found in Table 3.1 In the simulation, the current controller is designed to achieve dead-beat response in order to keep the bandwidth of the internal loop as high as possible. This is done to keep the UDE filter bandwidth well inside the current controller spectrum. The control signal is the duty-cycle of the PWM, The duty cycle is updated twice in each switching cycle and determining the on-time and the off-time of the transistor in accordance to the asymmetric modulation method described in chapter 2. The simulation results are demonstrating promising results and the THD under the non-linear load is significantly reduced (2.15%), when compared to the feed forward impedance design described in chapter 2 where the feedforward gain Z_v is chosen as 0 to minimise the output impedance of the inverter. Figure 3.4 shows the steady-state voltage and current waveform for UDE controlled inverter compared to the feed-forward controller. Figure 3.5 shows the spectral analysis for the output voltage, in which the UDE harmonics are well suppressed.

Table 3.1 Inverter and controller parameters stand alone simulation.

Parameter	Value
R	0.5Ω
L	$3mH$
K_p	89
ω_{bw}	$2 \cdot \pi \cdot 500 \frac{Rad}{s}$
C	$27\mu F$
ω_U	$2 \cdot \pi \cdot 2000 \frac{Rad}{s}$
k_U	0.93

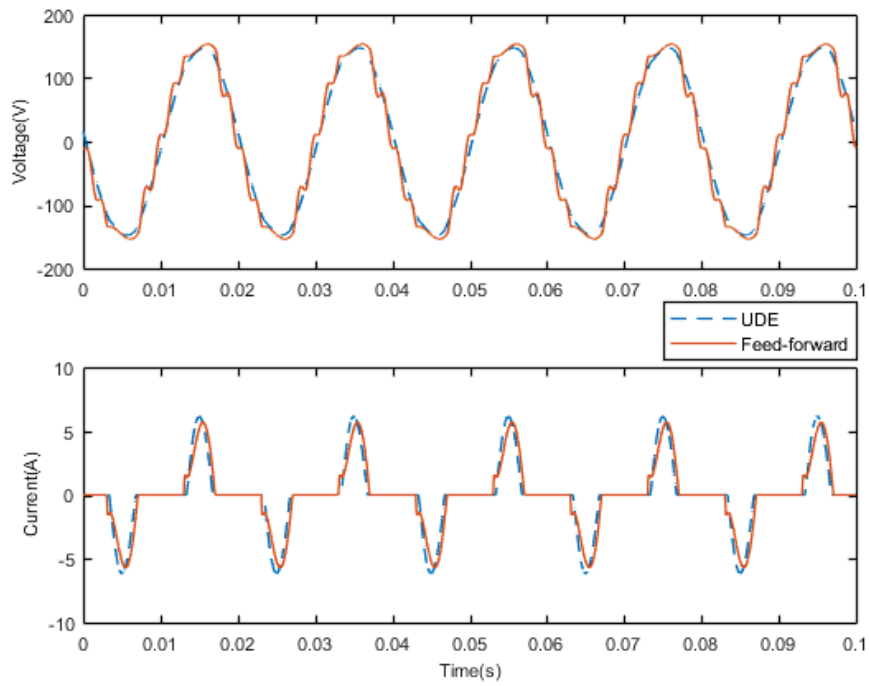


Fig 3.4 Voltage and current of the non-linear load under the UDE and under feed-forward control.

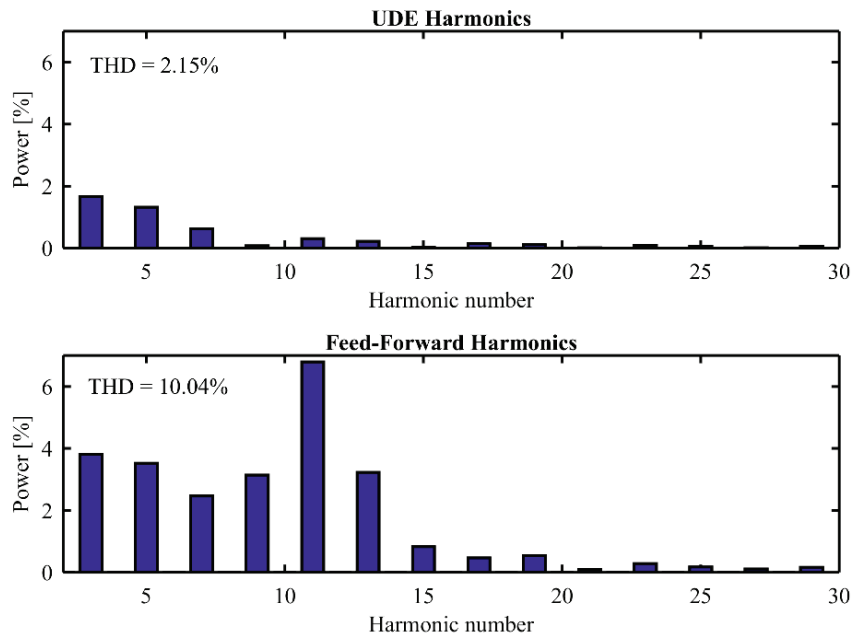


Fig 3.5 Simulation results, output voltage spectra

3.8.2 Parallel operation

A Simulink based simulation has been conducted utilizing two UDE controlled inverters and a rectifier load all connected in parallel. A diagram of the simulation model is in Figure 3.6,

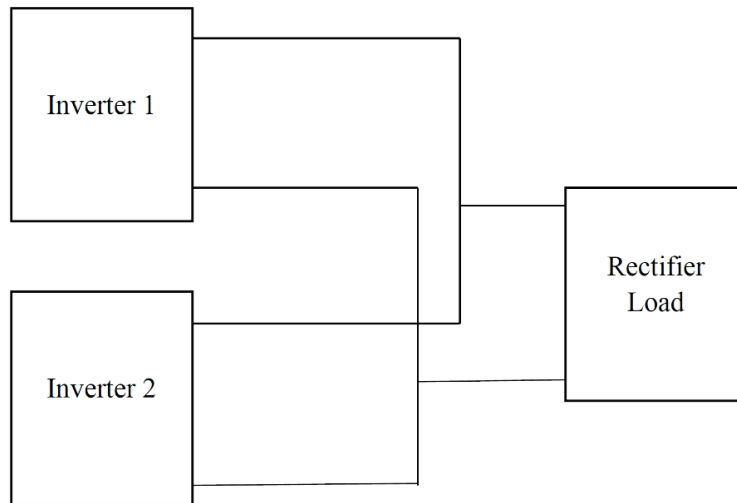


Fig 3.6 Simulation system diagram

the properties of the simulated inverters are summarized in Table 3.2. Note that the inverters k_U is chosen in accordance with (3.38). The rectifier load is made of ideal diode bridge connected to parallel RC load with $R = 150\Omega, C = 1mF$. The inverters current regulators were given a different gains in order to show that the output impedance is independent of the current regulator. The simulation results shows the

Table 3.2 Simulated inverters parameter

Parameter	Value
R	0.5Ω
L	$1mH$
C	$50\mu F$
V_{DC}	$400V$
f_{sw}	$25kHz$
$K_{P,inverter 1}$	44
$K_{P,inverter 2}$	40
ω_{bw}	$1000 \cdot \pi$
$\omega_{U,inverter 1}$	$2000 \cdot \pi$
$\omega_{U,inverter 2}$	$4000 \cdot \pi$

current distribution between two parallel inverters. To generate the same EMF for both inverters a PLL loop has been designed for each of the inverters and the same reference model has been used for both inverters. Figure 3.7 shows the inverter output impedance over a relevant

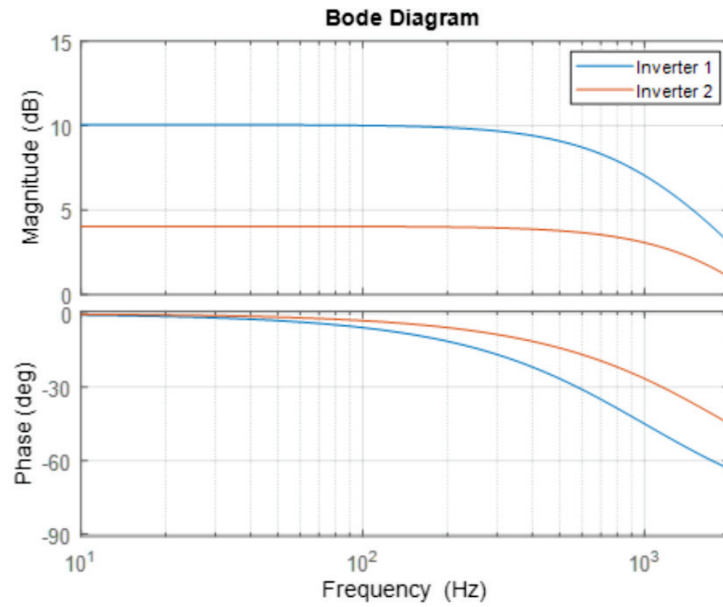


Fig 3.7 Inverters output impedance bode diagram

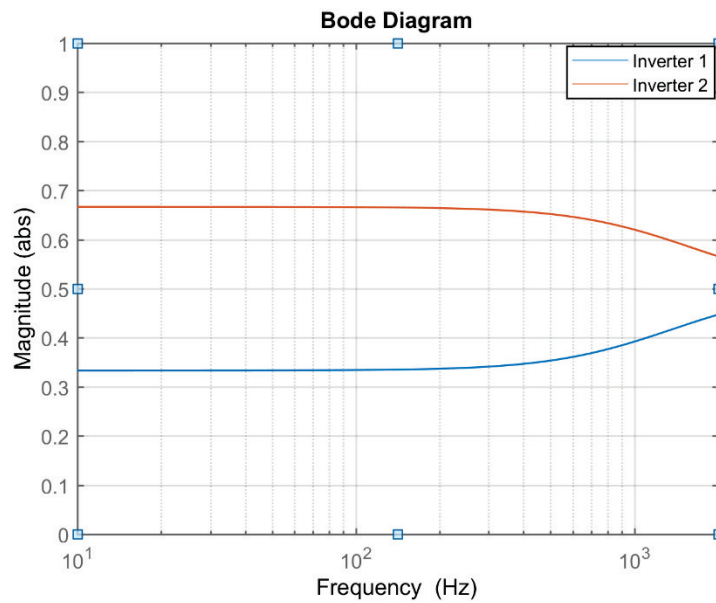


Fig 3.8 Relative impedance of inverter output

spectrum. Figure 3.8 shows the admittance related the total admittance. The output voltage in the point of common coupling of both inverters is shown in Figure 3.9 and the time domain

current wave is shown in Figure 3.10 demonstrating a current distribution in accordance with the UDE filter bandwidth as in (3.45).

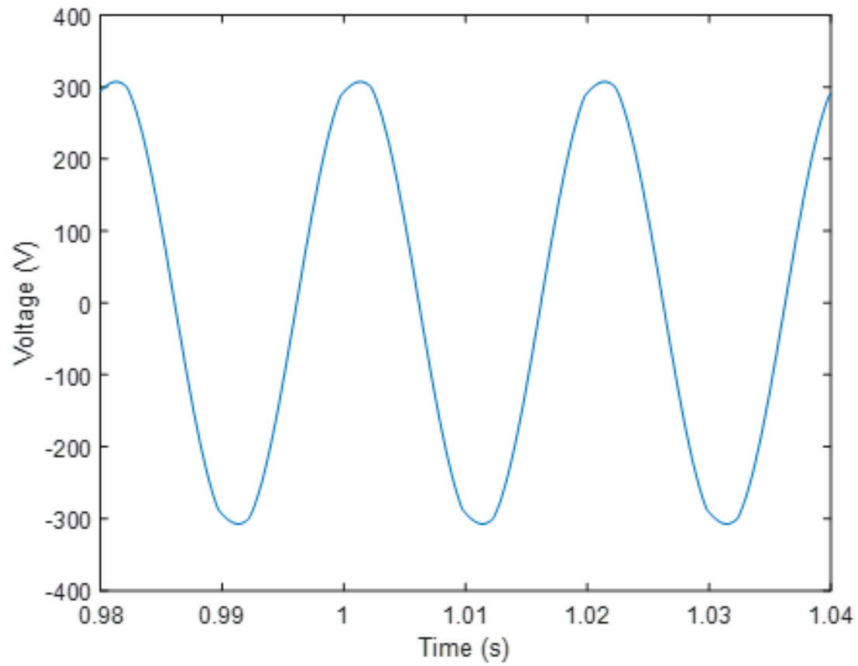


Fig 3.9 Steady-state output voltage of the inverters.

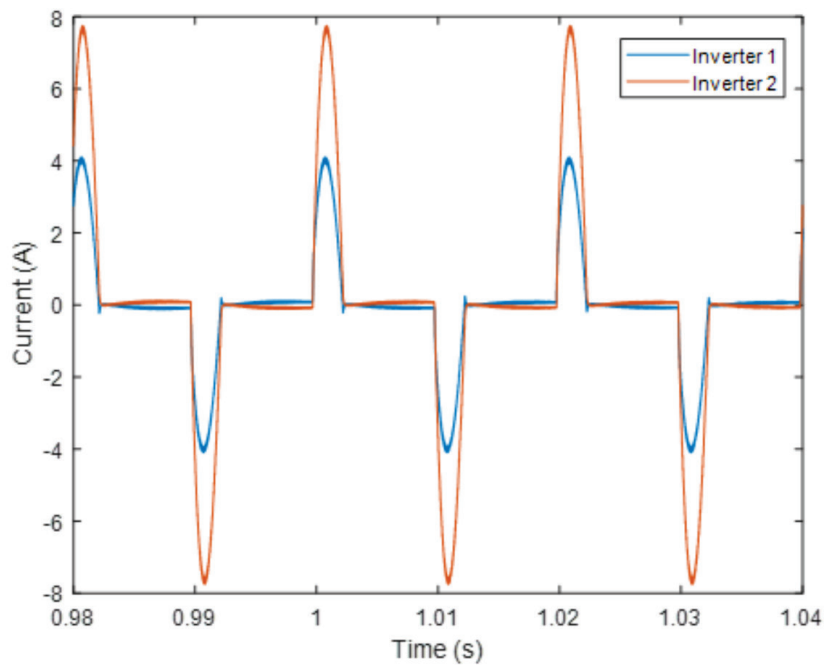


Fig 3.10 Steady-state output currents of the inverters in the simulated systems.

3.9 Experimental results

To validate the proposed theory, a laboratory prototype has been built. The experimental setup consists of a modified TI TMDSHV1PHINVKIT kit and the control algorithm is implemented over TI F28M35 control core. The laboratory prototype has been powered by a laboratory high voltage DC power supply. The DC-Bus voltage has been set to 190V. The controller code has been generated using Simulink automatic code generation tools and therefore the computation delay of the current controller has a minimum value of $0.33T_{PWM}$. Therefore the controller gain is limited and as a result of that, the current controller closed loop bandwidth is limited as well. The experimental setup parameters are given in Table 3.3. The load is made of a diode rectifier followed by parallel RC load. The output resistor of the load is 100Ω and the parallel capacitor is $960\mu F$. As shown from the results the load Crest Factor (CF) is 3.25. The output voltage THD for the proposed controller is 3.7% for the first 29 harmonics. The experimental results are compared to a virtual impedance controller with inductor current feedback. In the experimented feed-forward controller a small virtual impedance is added in order to damp the LC filter resonance as in (Dahono, Bahar, Sato and Kataoka, 2001). Figure 3.11 shows the UDE controlled output vs the load current, Figure 3.12 shows the output voltage for a feed-forward controller and Figure 3.13 shows a comparison of the spectral content of the output voltage for both control methods.

Table 3.3 Experimental setup parameters

Parameter	Value
R	0.5Ω
L	$3mH$
C	$27\mu F$
V_{DC}	$190V$
f_{sw}	$15kHz$
K_P	59
ω_{bw}	$1000 \cdot \pi$
ω_U	$3000 \cdot \pi$
k_U	0.95

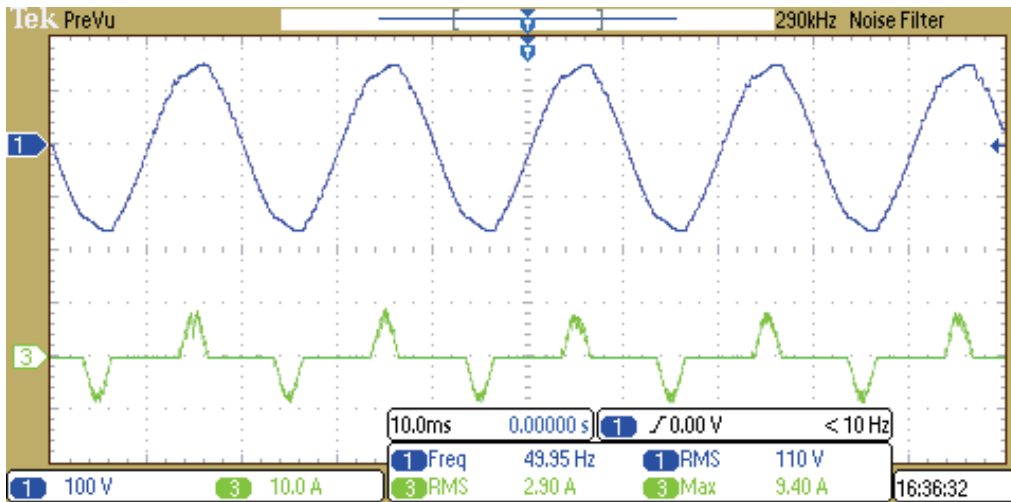


Fig 3.11 Output voltage and current of UDE controlled inverter

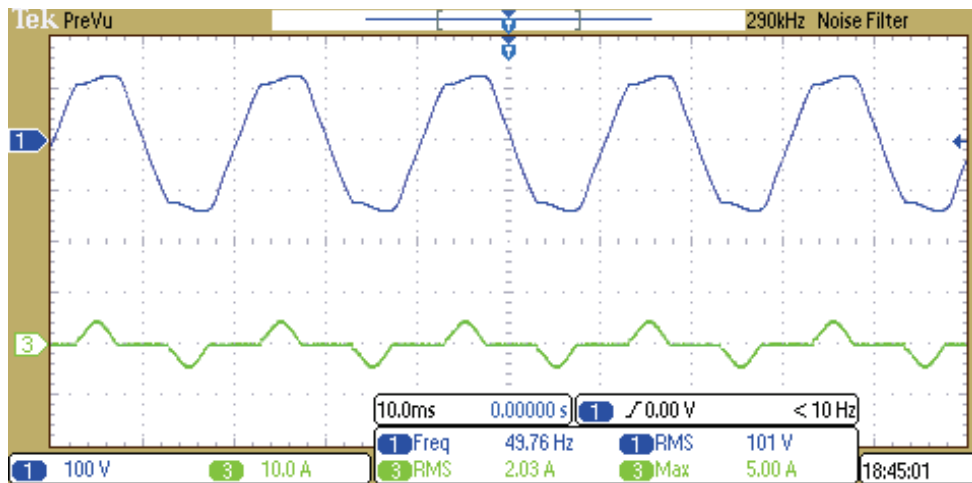


Fig 3.12 Output voltage and current of inverter with virtual impedance loop.

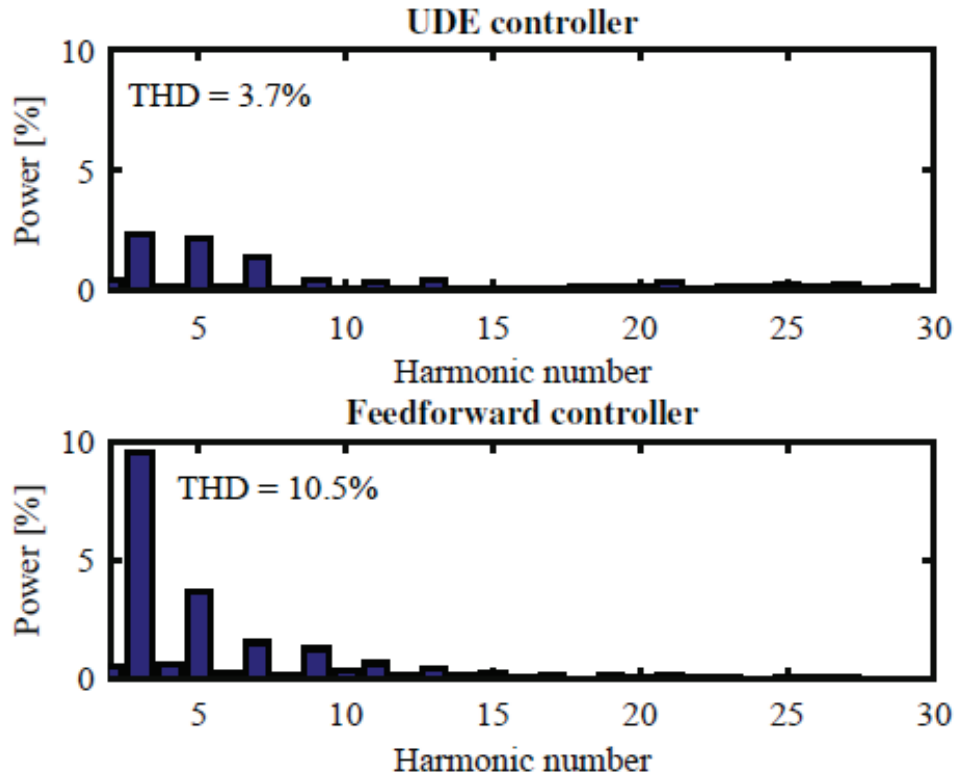


Fig 3.13 Output voltage spectrum of both UDE controller and feedforward virtual impedance.

3.10 Conclusion

This chapter reveals the features of the use of the UDE controller for inverter control. The chapter shows systematic UDE design for power inverter voltage regulation. It is shown that the design of the UDE filter is affecting both the out impedance characteristics and size. The method is then demonstrated through both parallel operation simulation and the output voltage quality comparison of an inverter with direct virtual impedance loop and a UDE controlled inverter. Despite the fact that a UDE controlled inverter shows better results than an inverter with virtual impedance loop. The results in this chapter are demonstrated for light load only. This is resulted from the bandwidth limitation coming from the current loop design and the modulation transport delay. In the next chapters the bandwidth limitation is discussed and a few filter solutions are proposed.

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4. Design of a UDE Frequency Selective Filter to Reject Periodical Disturbances

Publication number 1

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Nomenclature

A, B	State-space model matrices
A_m, B_m	Reference model matrices
B^+	Pseudo-inverse of B
C	Output filter capacitance
d	Disturbance input
e	State error vector
ude	Estimated uncertainty and disturbance
g	Impulse response of the UDE filter
$H_d(s)$	UDE disturbance rejection transfer function
$H_f(s)$	UDE low-frequency disturbance rejection transfer function
$H_{FB}(s)$	Feedback transfer function
$H_{FF}(s)$	Feedforward transfer function
$H_k(s)$	UDE high-frequency disturbance rejection transfer function
$H_M(s)$	UDE tracking transfer function
i_L	Inductor current
L	Output filter inductance
$\mathcal{L}^{-1}\{\cdot\}$	Inverse Laplace operator
$L_g(s)$	Voltage loop gain
$R(s)$	Laplace transform of the reference signal
$T_I(s)$	Current loop tracking transfer function
u	System input
u_d	Lumped disturbance and uncertainty

v_o	Output voltage
x	State vector
x_m	Reference model state vector
ω_f	UDE filter bandwidth
ω_{max}	Current tracking bandwidth
ω_R	Reference model bandwidth

For signals represented in time-domain and in s-domain or z-domain, lower case represents time domain signals and uppercase s or z domain signals.

List of amendments to the original published version

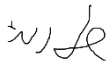
1. L_v is defined in the text as a loop gain
2. The typo “the first seven harmonics” has been fixed to “the first six harmonics”
3. Equations (12) and (14) has been corrected to include only single minus sign
4. Equation (17) added index i
5. ω_0 has been defined in the text as the base frequency
6. The inverse Laplace transform notation has been changed from $L^{-1}\{\cdot\}$ to $\mathcal{L}^{-1}\{\cdot\}$

Statement of contribution for the author Shlomo Gadelovits

The author Shlomo Gadelovits proposed the frequency selective filter to achieve good disturbance rejection performance under limited bandwidth. He also performed all the presented simulations and wrote the main body of work.

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Design of a UDE Frequency Selective Filter to Reject Periodical Disturbances

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Abstract: In this paper a new filter design for the Uncertainty and Disturbance Estimator (UDE) is proposed to reject periodical disturbances when a limited bandwidth is required for the control output. The motivation comes from several applications where the system actuator may introduce a bandwidth limitation, as a result of internal delays, or when the actuator itself is a limited bandwidth closed-loop system. When the traditional UDE approach is applied in these systems, the stability requirements impose a limitation over the effective bandwidth of the UDE filter and therefore disturbances cannot be fully rejected by the filter. In the case where the expected disturbance is periodical with a known fundamental frequency, the proposed UDE filter is designed as a chain of filters to match selected bands of the expected disturbance spectrum and fully reject them while maintaining the desired stability margins. A design example of a power inverter application is investigated and extensive simulation results are provided to verify the proposed UDE filter design.

Keywords: Uncertainty and disturbance estimator, disturbance rejection, limited bandwidth design, power systems, stability margins.

1. INTRODUCTION

The UDE control theory was first proposed in (Zhong and Rees, 2004) to achieve disturbance rejection of a system with uncertainties and external disturbances. This theory has been evolved from the time delay control problem, which has been investigated in (Youcef-Toumi and Ito, 1987, 1990), to overcome the need of calculating derivatives of system states and to cancel the need of a delay in the controller. Successful applications of the UDE approach include several practical examples, such as servo control (Ren et al., 2017), wind turbine control, (Ren and Zhong, 2013), inverter power flow control (Wang et al., 2016) and DC-DC voltage regulation (Kuperman, 2013).

One of the crucial stages in the implementation of the UDE controller is the design of the UDE filter (Kuperman et al., 2010), since the filter design plays a key role in the disturbance rejection performance. In the literature, several types of low-pass filters (LPFs) have been proposed for UDE controllers such as first-order filters (Kuperman et al., 2010), high-order filters (Shendge and Patre, 2007), the α -filter (Chandar and Talole, 2014), etc, to further improve the disturbance rejection. These methods provide very good results when either the disturbance is constant or when the disturbance spectrum is clearly inside the UDE filter bandwidth. However, in many applications, the actuator bandwidth is limited due to the sampling frequency or due to the actuator's internal structure, which imposes a bandwidth limitation for the UDE filter design

(Kuperman, 2015) and therefore the LPF design may result in a degraded performance. In addition, in the case where the plant model is not given in the canonic form, a cascaded multi-loop structure has to be applied in order to comply with the UDE constraint that is related to the calculation of a pseudo-inverse matrix, as described in (Zhong and Rees, 2004). In the case of a multiloop control architecture when the expected disturbance is in the low frequency range, the control loops can be decoupled in the frequency domain by limiting the outer loop bandwidth to a lower decade (Maffezzoni et al., 1990). However, in applications that include voltage or current regulation of an inverter stage (Gouraud et al., 1997; Rioual et al., 1996), rotational machinery speed, torque or position regulation (Tomizuka, 2008), the expected disturbance is periodical and may contain a known harmonic spectrum. Hence, if the disturbance harmonic content is not clearly inside the UDE filter bandwidth, it will not be attenuated completely. Nevertheless, when the UDE filter is designed as LPF, the transfer function of the disturbance to the output reaches a peak gain around the geometric average of the reference model and the UDE filter bandwidths.

In this paper a new approach to the UDE filter design is proposed. In this approach, the UDE filter is designed as a Frequency Selective Filter (FSF) where each expected disturbance harmonic is attenuated by the filter without violating the bandwidth limitations. It is shown in the paper that the suitable filter design is achieved by selecting

the desired disturbance rejection function. A design example of an inverter output voltage regulation is presented where the inverter is driven by a limited bandwidth current regulator. Simulation results of the inverter connected to nonlinear load are provided to validate the theory and a comparison between the proposed FSF and the LPF methods is presented.

The paper is organized as follows: Section 2 provides an overview of the UDE approach. The proposed design for the UDE filter is presented in Section 3, where it is explained how the periodical disturbance is rejected. A practical example of an inverter application is investigated in Section 4 and extensive simulation results are provided to verify the effectiveness of the proposed method. Finally, in Section 5, some conclusions are drawn.

2. OVERVIEW OF THE UDE-BASED APPROACH

Consider a linear time-invariant single-input-single-output system of the form

$$\dot{x}(t) = (A + \Delta A(t))x(t) + (B + \Delta B(t))u(t) + d(t), \quad (1)$$

where ΔA , ΔB represent the system uncertainties and $d(t)$ is an unmeasurable disturbance. The main task is to track a reference signal independently from the system uncertainties or the external disturbance. Hence, a reference model is designed as

$$\dot{x}_m(t) = A_m x_m(t) + B_m r(t), \quad (2)$$

where $r(t)$ is the desired reference and A_m , B_m are the state-space matrices of the desired dynamics. Consider the error vector

$$e(t) = \begin{bmatrix} x_{m1} - x_1 \\ x_{m2} - x_2 \\ \dots \\ x_{mn} - x_n \end{bmatrix} \quad (3)$$

where n is the system order. Then the main challenge is to find a control law which guarantees the stable error dynamics

$$\dot{e}(t) = A_m e(t). \quad (4)$$

Based on the UDE approach (Kuperman et al., 2010), such a controller takes the form

$$u(t) = B^+(A_m x(t) + B_m r(t) - Ax(t) - ude(t)), \quad (5)$$

where $B^+ = (B^T B)^{-1} B^T$ is the pseudo inverse of B . The term $ude(t)$ is calculated from the system uncertainties and disturbances as

$$ude(t) = u_d(t) \star g(t), \quad (6)$$

where $g(t)$ is the impulse response of the UDE filter, \star is the convolution operator and $u_d(t)$ is the calculated disturbances and uncertainties. The term $u_d(t)$ is obtained from (1) as

$$u_d(t) = \Delta A(t)x(t) + \Delta B(t)u(t) + d(t) = \dot{x}(t) - Ax - Bu. \quad (7)$$

It is worth noting that the UDE solution includes a pseudo-inverse term and therefore the constraint

$$[I - BB^+] \cdot [A_m x + B_m r(t) - Ax - \Delta A(t)x - d(t)] = 0 \quad (8)$$

must be met (Zhong and Rees, 2004). According to the analysis in (Zhong et al., 2011), the state dynamics of the UDE-controlled system becomes

$$X(s) = H_m(s)R(s) + H_d(s)B \cdot B^+ U_d(s), \quad (9)$$

where

$$H_m(s) = (sI - A_m)^{-1} B_m \quad (10)$$

and

$$H_d(s) = (sI - A_m)^{-1} (1 - G(s)). \quad (11)$$

From (11) there is $H_d(s) = H_k(s)H_f(s)$ with $H_k(s) = (sI - A_m)^{-1}$ and $H_f(s) = (1 - G(s))$. Combining (5), (7) and (6), yields the UDE-based control law

$$u(t) = -B^+ \left(Ax(t) + \mathcal{L}^{-1} \left\{ \frac{sG(s)}{1 - G(s)} \right\} \star x(t) - \mathcal{L}^{-1} \left\{ \frac{1}{1 - G(s)} \right\} \star (A_m x(t) + B_m r(t)) \right), \quad (12)$$

where $\mathcal{L}^{-1}\{\cdot\}$ the inverse Laplace operator. Note here that the reference model should be chosen in accordance to the desired tracking bandwidth and transient performance.

3. PROPOSED UDE FILTER TO REJECT PERIODICAL DISTURBANCE

Consider a plant system of the form of (1) operated by an actuator with a maximum actuator input bandwidth of ω_{max} . Given that the UDE approach, described in the previous section, is applied to this system in order to follow a reference model, the control signal u has to satisfy the bandwidth requirement. Therefore

$$|U(j\omega)| < \frac{1}{\sqrt{2}}, \quad \in \omega > \omega_{max}. \quad (13)$$

From (12), the Laplace form of $u(t)$ after rearranging the terms becomes

$$U(s) = B^+ \underbrace{\left(\frac{1}{1 - G} \right)}_{H_{FF}(s)} B_m R(s) - \underbrace{\left(B^+ A - \frac{1}{1 - G} \cdot B^+ A_m + B^+ \frac{sG}{1 - G} \right)}_{H_{FB}(s)} X(s) \quad (14)$$

where $H_{FF}(s)$ is the feedforward term and $H_{FB}(s)$ is the feedback. Fig. 1 shows the equivalent control loop where $T(s)$ is the actuator transfer function, $P(s)$ is the plant model and $D(s)$ is the disturbance and uncertainty in the input. Looking at Fig. 1, the corresponding loop gain L_g is

$$L_g(s) = H_{FB}(s) \cdot T(s) \cdot P(s). \quad (15)$$

To ensure closed-loop system stability, the loop-gain has to meet the minimum stability margins.

Additionally, according to (11), the dynamics of the disturbance are affected both by the choice of the reference model and by the design of the UDE filter. In (Zhong et al., 2011) it is proven that $u_d(t)$ is attenuated twice, since at

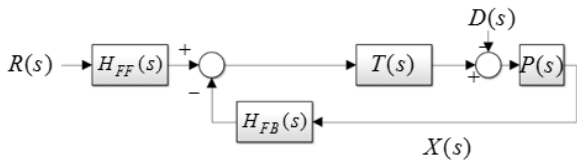


Figure 1. Equivalent loop diagram

the low frequency range it is attenuated by $H_f(s)$ and at the high frequency range by $H_k(s)$, as shown at Fig. 2. It is clear from (11) that when $G(s)$ equals to unity the disturbance is fully rejected. However, the main trade-off in the filter design is between performance and control signal bandwidth (Kuperman, 2015). By increasing the UDE filter bandwidth, the bandwidth of the UDE control signal u increases which eventually decreases the stability margins of the system.

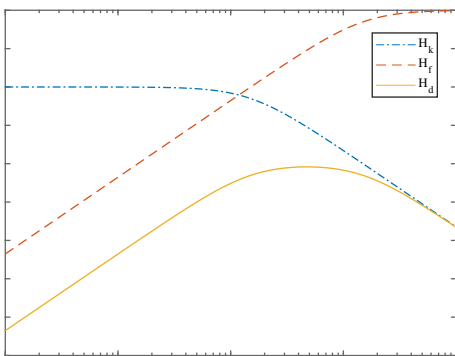


Figure 2. Sketch of low pass filter design

Hence, the main task is to design the UDE filter accordingly in order to reject the disturbance under a limited bandwidth of the control signal and guarantee the desired stability margins. In this paper, a periodical disturbance $d(t)$ that appears in the n harmonics of the rated frequency ω is considered, i.e.

$$d(t) = \sum_{i=1}^n d_i \sin(i\omega t + \theta_i). \quad (16)$$

In order to reject this disturbance, the proposed filter $H_f(s)$ is designed as a chain of Butterworth band stop filters of the form

$$N_i(s) = \frac{s^2 + \omega_{Hi} \cdot \omega_{Li}}{s^2 + (\omega_{Hi} - \omega_{Li})s + \omega_{Hi} \cdot \omega_{Li}}, \quad (17)$$

where ω_H and ω_L are the high and low limit of the stop band, respectively. The filter $H_f(s)$ is then calculated as the product of (17) as follows

$$H_f(s) = \prod_{i=1}^n N_i(s). \quad (18)$$

In order to guarantee the input bandwidth requirement, as a rule of thumb, the frequency ω_H of the n -th band stop filter should be less than ω_{max} . Then, the resulted UDE filter is obtained from $H_f(s)$ as

$$G(s) = 1 - H_f(s) \quad (19)$$

The resulted filter $H_f(s)$ is illustrated in Fig. 3 for the first six harmonics, which are considered to be inside

the bandwidth of the control signal. The resulting Bode diagram of the Frequency Selective Filter (FSF) $G(s)$ is shown in Fig. 4. It is observed that the filter reaches a unity gain and zero phase at the desired frequencies. This results in $H_d(s) \rightarrow 0$ at the disturbance signal harmonics which leads to a clear rejection of the periodical disturbance.

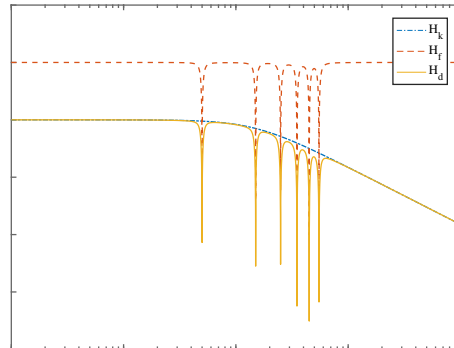


Figure 3. Sketch of the frequency selective filter design

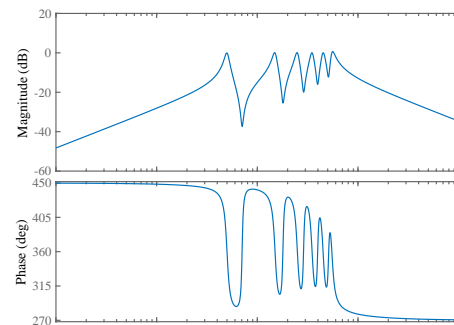


Figure 4. Frequency selective filter $G(s)$

4. DESIGN EXAMPLE

4.1 Power inverter output voltage regulator

Consider an AC inverter leg followed by an LC filter as shown in Fig. 5, where u_o is the inverter voltage that represents the control input, i_L is the inductor current, v_o is the output voltage and i_o is the load current. The parasitic resistances of the capacitor and the inductor are neglected for brevity. The inverter is connected to a load and the main task is for the inverter output voltage v_o to track the pure sinusoidal reference signal

$$r(t) = V_M \sin(\omega_0 t), \quad (20)$$

at the base frequency ω_0 independently from the load disturbances, i.e. to reject linear and nonlinear periodical loads. This represents a common scenario in inverter applications where the load voltage should be equal to $r(t)$ by rejecting additional harmonic components that occur from the load dynamics. Using Kirchoffs laws, the inverter model dynamics are given as

Table 1: Inverter parameters

Parameter	Value	Units
C	10	μF
ω_{max}	$2\pi \cdot 2000$	rad/s
ω_0	$2\pi \cdot 50$	rad/s

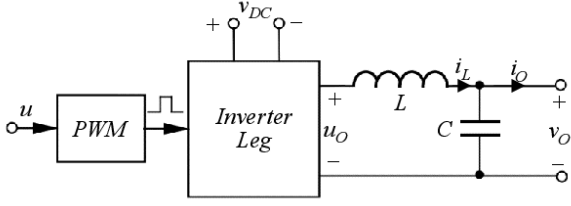


Figure 5. Schematic of a single-phase inverter with an output filter

$$\begin{aligned} L \frac{di_L}{dt} &= u_o(t) - v_o(t) \\ C \frac{dv_o}{dt} &= i_L(t) - i_o(t). \end{aligned} \quad (21)$$

To comply with (8) and apply the UDE for the output voltage regulation, a cascaded control loop design is adopted. Hence, the dynamics (21) can be investigated only using the second equation

$$\frac{dv_o}{dt} = \frac{1}{C}i_L(t) - \frac{1}{C}i_o(t), \quad (22)$$

where $i_L(t)$ is the output of a closed loop inductor current regulator which serves as the actuator for the voltage dynamics (22) and $C^{-1}i_o(t)$ is the load current disturbance (see Fig. 6). Because of the PWM and digital control delay, the maximum allowed bandwidth of the current regulator reference $i_L^*(t)$ is limited by a defined ω_{max} . In many cases the closed loop current regulator can be approximated as first order LPF of the form

$$T_I(s) = \frac{\omega_{max}}{s + \omega_{max}}. \quad (23)$$

Following (22) it yields that

$$A = 0, B = C^{-1}$$

and $x \equiv v_o$. Given the reference signal $r(t)$ from (20), the

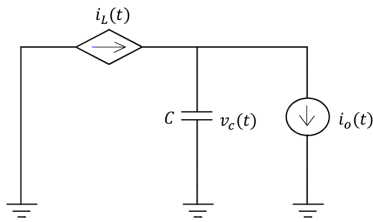


Figure 6. Equivalent circuit of output voltage dynamics

reference model dynamics are designed according to (2) as

$$\dot{x}_m(t) = -\omega_R x_m(t) + \omega_R r(t), \quad (24)$$

where ω_R is the bandwidth of the reference model and as a rule of thumb is chosen to be 10 times larger than the reference signal frequency. to ensure low tracking error. Note that (Ren et al., 2017) has recently proposed a design of the reference model for AC signal, to overcome the gap between the reference model output to the reference signal. The UDE control law is obtained from (12) as

$$I_L^*(s) = \frac{C}{1-G}(\omega_R(X(s) - R(s)) - sGX(s)). \quad (25)$$

Combining (15), (23), (25) and the Laplace transformation of (22), the loop gain results in

$$L_V(s) = \frac{\omega_R + sG(s)}{s(1-G(s))}T_I(s). \quad (26)$$

4.2 UDE filter design

The UDE filter is designed based on two requirements: i) meet the minimum stability margins and ii) reject the disturbances in the output within the relevant spectrum. In order to ensure stability, the UDE filter is designed for a minimum Phase Margin (PM) of 45° and a minimum 6dB Gain Margin. Note from (22) that the disturbance is amplified by C^{-1} which is the inverse of the output capacitor size. In the presented inverter case, given the value of the capacitor, the disturbance is amplified by 100dB. To verify the efficiency of the proposed FSF method, three different cases for the UDE filter are investigated: a) setting $G(s) = 0$, b) using a low-pass filter and c) using the proposed FSF.

Case 1: $G(s) = 0$

When the UDE filter is chosen to be $G(s) = 0$, the corresponding loop gain $L_V(s)$ results from (23) and (26) in

$$L_V(s) = \frac{\omega_R}{s} \cdot \frac{\omega_{max}}{s + \omega_{max}}. \quad (27)$$

In this case the bandwidth of the reference model is maximized to the allowable stability margins and is set to $\omega_R = 2\pi \cdot 2800 \text{ rad/s}$. The left column of Fig. 7(a) shows the loop gain with the required stability margin and Fig. 7(b) shows the Bode diagram of the transfer function of the disturbance to the output voltage.

Case 2: Using a low-pass filter

In this case, the bandwidth of the reference model ω_R is set to be $2\pi \cdot 500 \text{ rad/s}$ in order to ensure suitable tracking. In order to demonstrate the trade-off between the filter design, two low pass filters with a different order (order-1 and order-2) are tested. The considered low pass filters are shown in Table 2. The middle column of Fig. 7(a) shows the loop gain of the cascaded system for the first and second-order filter. It is clear that by increasing the filter order, the cut-off frequency reduces and also the low-frequency disturbance rejection is improved. On the other hand, the use of a high order filter deteriorates the medium frequency disturbance rejection, as reflected from the middle column of Fig. 7(b).

Table 2: Tested Low Pass Filters

Order:	$G(s)$	ω_f
1	$\frac{\omega_f}{s + \omega_f}$	$2\pi \cdot 850$
2	$\frac{\frac{2}{\sqrt{2}}\omega_f + \omega_f^2}{s^2 + \frac{2}{\sqrt{2}}\omega_f + \omega_f^2}$	$2\pi \cdot 350$

Case 3: Using the proposed FSF

As in the case for the low-pass filter, the bandwidth for the reference model is chosen to be $2\pi \cdot 500 \text{ rad/s}$. The design of the FSF filter begins by calculating the desired $H_f(s)$ as in Section 3. In the case of the inverter, in

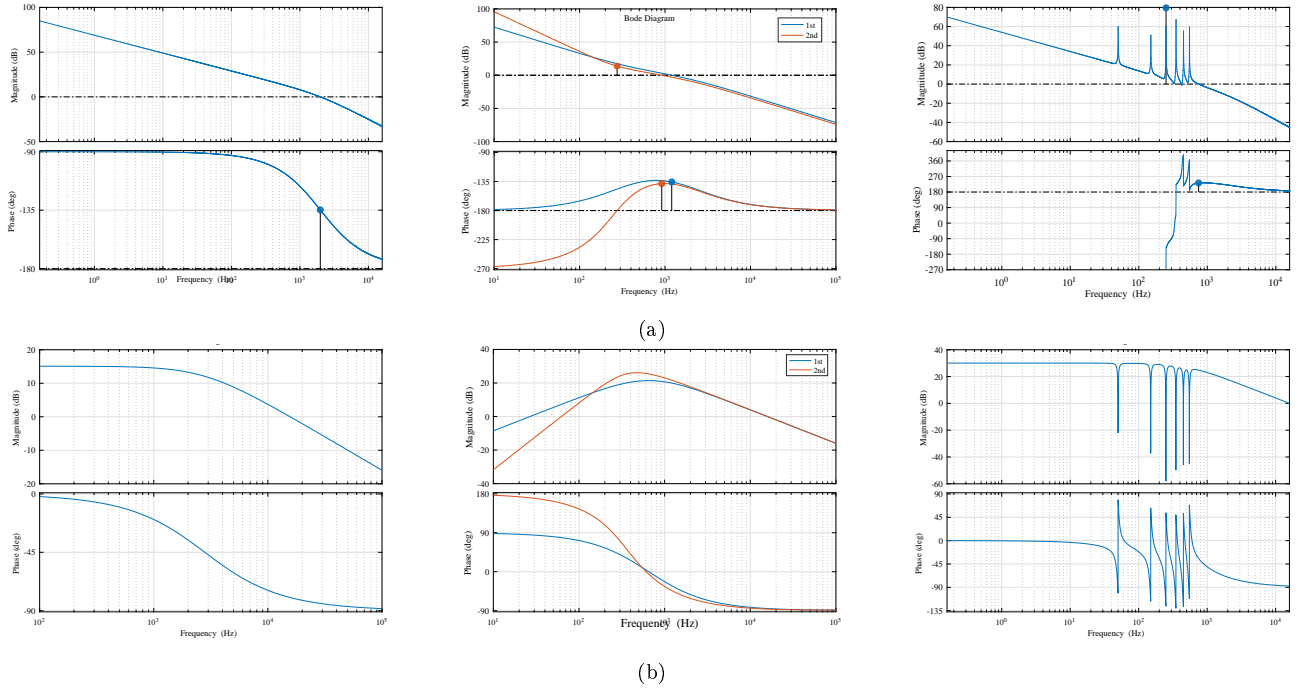


Figure 7. Bode Diagrams with $G(s) = 0$ (left column), 1st and 2nd order low-pass filters (middle column) and the proposed FSF (right column): (a) Loop-Gain and (b) Disturbance to output.

order to reduce the disturbance around the harmonics, the filter $H_f(s)$ has been calculated as a stop band around 50Hz and its odd harmonics up to the 11-th. The right column of Fig. 7(a) shows the disturbance to output bode where it is clearly shown the signal attenuation around the selected frequencies and Fig 7(b) reveals the loop gain Bode diagram of the cascaded system.

4.3 Simulation results

Simulation was carried out using the system presented in Section 4.1 connected to a nonlinear load, which consists of a diode rectifier connected to an RC load with $R_L = 50\Omega$ and $C_L = 570\mu\text{F}$. The reference voltage signal contains a single harmonic of 50Hz with amplitude of 155V having the form of (20). Fig. 8 shows the simulation results for the various filter designs. The left column of Fig. 8 shows the load current which is proportional to the system disturbance input ($d(t) = C^{-1}i_o(t)$). The middle column of Fig 8 shows the the error signal between the reference model output and the output voltage. The right column of Fig. 8 shows the spectrum of the output voltage where the harmonics are represented as a percentage of the fundamental component. It is observed that with the proposed FSF, all the harmonics of the output voltage up to the 11-th are completely attenuated opposed to the traditional low-pass filter design, thus significantly improving the total harmonic distortion of the output. In addition the error signal $e(t)$ is significantly reduced thus without increasing the UDE filter bandwidth.

5. CONCLUSION

In this paper a new filter design for UDE controllers is revealed. It is shown that in a case where the actuator bandwidth is limited and the disturbance is expected to

contain harmonics, it is better to design the UDE filter to match the unity value around the expected spectral content. The approach is investigated and compared to the traditional low pass filter design. Simulation results are provided to validate the theory.

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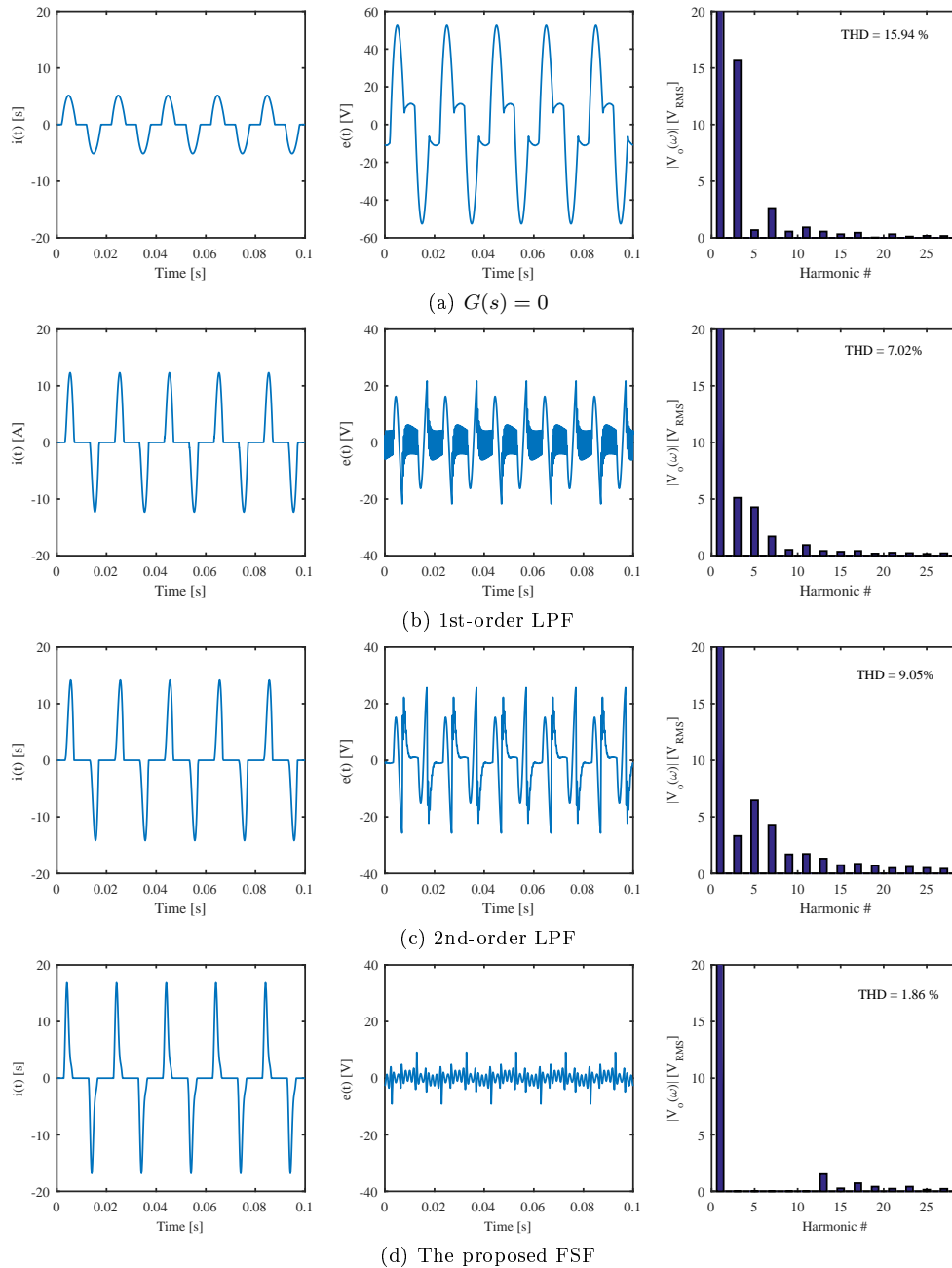


Figure 8. Simulation results for UDE control utilizing different filters

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5. Uncertainty and Disturbance Estimator based Controller Equipped with a Multi-Band-Stop Filter to Improve the Voltage Quality of Inverters

Publication number 2 -

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Nomenclature

C	Capacitance
C_L	Load capacitance
C_n	Nominal capacitance
e_o	Error signal
g	UDE filter impulse response
$H_{FB}(s)$	Feedback transfer function
$H_{FF}(s)$	Feedforward transfer function
$H_n(s)$	Band stop filter transfer function for harmonic n
i_L	Inductor current
i_L^*	Inductor current reference
i_{L0}^*	Tracking controller output
i_O^d	Lumped disturbance current
\hat{i}_O^d	Estimated lumped disturbance current
K_{PI}	Current compensator proportional gain
K_{PV}	Voltage controller compensator proportional gain
L	Inductance
L_I	Current loop-gain
L_V	Voltage loop gain
R_L	Load resistance
T_C	Computation delay time

T_d	Delay time
T_I	Closed loop current tracking transfer function
T_{PWM}	PWM delay time
T_s	Switching cycle time
u'	Current regulator output
u_o	Inverter bridge voltage
v_{DC}	DC bus voltage
v_o	Output voltage
v_o^*	Output voltage reference
v_{OR}	Voltage reference model internal state and output
$Z_O(s)$	Output impedance
ω_F	UDE filter bandwidth
ω_R	Reference model bandwidth

For signals represented in time-domain and in s-domain or z-domain, lower case represents time domain signals and uppercase s or z domain signals.

List of amendments to the original published version

1. The sentence following equation (24) has been changed from “reference model (8)” to “reference model (9)”
2. Figure 3 has been validated

Statement of contribution for the author Shlomo Gadelovits

The author Shlomo Gadelovits proposed the use of high order filters as UDE filters to minimise the output impedance of the inverter around the harmonics. He also designed and obtained results for all the experiments shown in the paper and wrote the main body of work.

Shlomo Y Gadelovits



Alon Kuperman



Qing-Chang Zhong



Visakan Kadirkamanathan



UDE-based Controller Equipped with a Multi-Band-Stop Filter to Improve the Voltage Quality of Inverters

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Abstract—In this paper, a method to directly shape the output impedance of an inverter is proposed to reduce the total harmonic distortion of the output voltage, based on the uncertainty and disturbance estimator (UDE)-based robust control framework. It is shown that, because of the two-degree-of-freedom feature of the UDE-based control strategy, the UDE filter directly affects the inverter output impedance. A multi-band-stop filter instead of a commonly adopted low-pass filter is then proposed to directly minimize the output impedance around the harmonics to reduce the effect of nonlinear loads and assure robustness to frequency variations. Two trade-offs are revealed: one between filter bandwidth and stability and the other between robustness and the number of harmonics suppressed. The effectiveness of the proposed control strategy is fully supported by experimental results.

Index Terms—Photovoltaic generators, maximum power point tracking, perturbation frequency.

I. INTRODUCTION

INVERTERS (also known as DC-to-AC converters) play an extremely important role in sustainable energy applications such as distributed generation; hybrid, hybrid electric and more electric transportation; smart grids etc. In addition, they are widely employed in uninterruptible power supplies, home appliances (induction heaters, air conditioners, refrigerators) and variable frequency drives. In other words, inverters have become a key component of many energy-conversion-related applications.

Many research activities are being carried out on important control problems associated with inverters [1]. Minimizing the total harmonic distortion (THD) of output inverter voltage

under nonlinear loads is one of the common challenges for these control problem. Deadbeat [2] and hysteresis [3] controllers as well as sliding-mode [4], observer [5] and Lyapunov function [6], [7] based approaches have been utilized to improve the voltage THD in addition to selective harmonic elimination [8], repetitive [9], harmonic voltage injection [10], model predictive [11] and offset-free robust tracking [12] control strategies. Recently, output impedance based strategies have become popular due to its influence on load sharing between several inverters operating in parallel. It was shown that output impedance of an inverter changes according to the control strategy adopted [1, 13] and may hence be reduced to enhance output voltage quality [14]. Since mainstream inverters possess low-frequency inductive output impedance, resistive [15] and capacitive [16] impedance was achieved by corresponding control methods to simplify the task of compensating load harmonics. Nevertheless, in the presence of nonlinear loads, only the values of output impedance at harmonic frequencies are of particular interest while the values at the rest of bandwidth is irrelevant for THD minimization. Multiresonant controllers were proposed to minimize the relevant output impedance [17]; however, due to the fact that fundamental frequency deviations may occur, not only the output impedance should be minimized around harmonic frequencies but also robustness to frequency deviations (note that the base frequency ω_0 deviation of $\Delta\omega_0$ becomes $n\Delta\omega_0$ around the n -th harmonic) must be assured as well.

In this paper, in order to directly influence the output impedance only at the regions of interest, dual-loop control structure is adopted [18], [19]. However, unlike typical cases [20], both loops are not decoupled due to limited available control bandwidth and therefore affect each other. Consequently, coupling effect between two loops is dealt with by considering the closed loop transfer function of the inner loop when designing the outer loop, avoiding loop decoupling constraint. It should be emphasized, that dual-loop control arrangement typically yield good performance (an interested reader is referred to [21] for detailed comparison of dual loop inverter control structures). However, PID compensators are typically utilized in multiloop control arrangements, enforced by e.g. feedforward actions, characterized by the two following drawbacks: infinite gain is achieved at DC only, calling for increased control bandwidth to reduce steady state error at non-zero frequencies and coupling between tracking and disturbance rejection due to single degree of freedom.

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$$u(t) = \frac{1}{v_{DC}(t)}(u'(t) + v_o(t)), \quad (3)$$

the current plant may be described by

$$\frac{di_L(t)}{dt} = L^{-1} \left(\frac{v_{DC}(t)}{v_{DC}(t-T_d)} (u'(t-T_d) + v_o(t-T_d)) - v_o(t) \right) \quad (4)$$

$$\approx L^{-1} u'(t-T_d),$$

as T_d^{-1} is much higher than bandwidths of v_{DC} and v_o . Since the modified plant is nearly disturbance-free, proportional controller

$$u'(t) = K_{PI} (i_L^*(t) - i_L(t)) \quad (5)$$

with $i_L^*(t)$ denoting inductor current reference signal, is selected. Current loop gain and complementary sensitivity function are then obtained as

$$L_I(s) = \frac{K_{PI} L^{-1}}{s} e^{-T_d s} \quad (6)$$

and

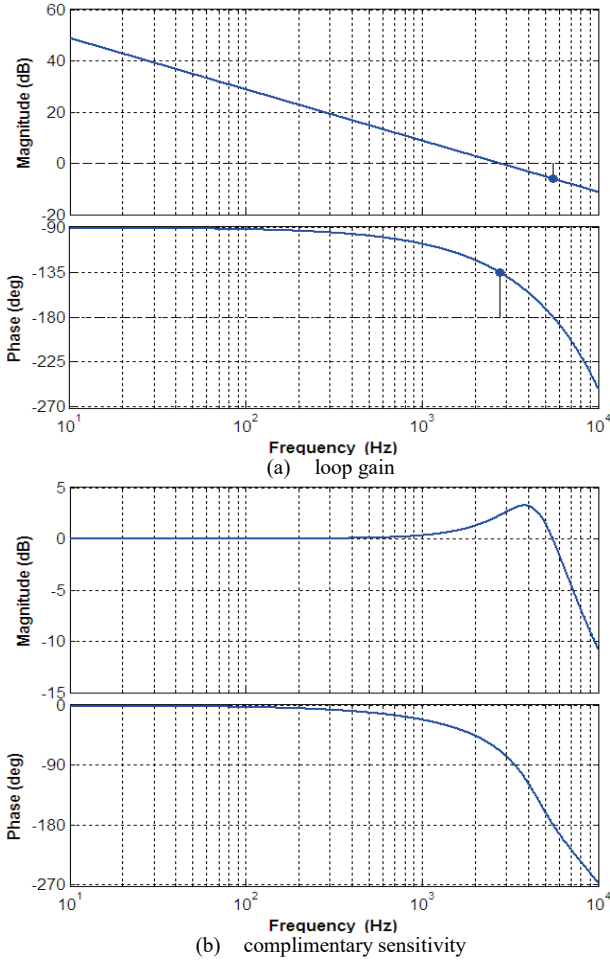


Fig. 3. Current loop performance merits for $K_{PI} = 59$ and $T_d = 45 \mu s$.

$$T_I(s) = \frac{L_I(s)}{1 + L_I(s)} = \frac{K_{PI} L^{-1}}{s e^{T_d s} + K_{PI} L^{-1}}, \quad (7)$$

respectively. Selecting $K_{PI} = 59$ leads to current loop bandwidth of 2762 Hz with 45° phase margin and 6 dB gain margin, as shown in Fig. 3a. Fig. 3b gives the Bode diagram of the complementary sensitivity function, which is of extreme

importance for voltage controller design, since $T_I(s)$ serves as voltage loop actuator.

C. Voltage controller

Note that i_L^* rather than i_L is set by the voltage controller, i.e. the current closed loop controller $T_I(s)$ must be properly taken into account. Output voltage dynamics may be rewritten as

$$\frac{dv_o(t)}{dt} = C^{-1} (i_L(t) - i_o(t)) \quad (8a)$$

$$= (C_n^{-1} + \Delta C^{-1}) (i_L^*(t) + \Delta i_L(t) - i_o(t)) = C_n^{-1} (i_L^*(t) - i_o^d(t)),$$

where C_n and ΔC respectively denote nominal and uncertain parts of C , $i_L = i_L^* + \Delta i_L$ with Δi_L representing inductor current tracking error and

$$i_o^d(t) = -C_n \Delta C^{-1} i_L^*(t) - (1 + C_n \Delta C^{-1}) (\Delta i_L(t) - i_o(t)) \quad (8b)$$

expresses the total lumped uncertainty and disturbance current.

Define the desired closed-loop behavior of v_o by the output of a linear time-invariant stable reference model

$$\dot{v}_{OR}(t) = -\omega_R v_{OR}(t) + \omega_R v_o^*(t) \quad (9)$$

with v_o^* denoting the output voltage reference signal and $\omega_R > 0$. The controller goal is to drive the error between the reference model and inverter outputs

$$e_o(t) = v_{OR}(t) - v_o(t) \quad (10a)$$

to zero by forcing the following stable error dynamics,

$$\frac{de_o(t)}{dt} = -\omega_R e_o(t). \quad (10b)$$

Combining (8) - (10) results in

$$i_L^*(t) = K_{PV} (v_o^*(t) - v_o(t)) + i_o^d(t) \quad (11)$$

with $K_{PV} = C_n \omega_R$. The control action (11) cannot be applied directly since i_o^d is unknown. This problem is dealt with as follows. Note that according to (8a),

$$i_o^d(t) = i_L^*(t) - C_n \frac{dv_o(t)}{dt} \quad (12)$$

Obviously, (12) cannot be substituted in (11) as is. A UDE-based approach replaces i_o^d in (11) with its filtered estimate, given by

$$\hat{i}_o^d(t) = i_o^d(t) * g(t) = \left(i_L^*(t) - C_n \frac{dv_o(t)}{dt} \right) * g(t), \quad (13)$$

where $g(t)$ is the impulse response of a frequency-selective linear time-invariant filter $G(s)$ and $*$ is the convolution operator. The control law is then derived as (cf. Fig. 4)

$$i_L^*(t) = i_{L0}^*(t) + \hat{i}_o^d(t) \quad (14)$$

$$= K_{PV} (v_o^*(t) - v_o(t)) + \left(i_L^*(t) - C_n \frac{dv_o(t)}{dt} \right) * g(t).$$

It is interesting to note that the voltage controller structure resembles that of a classical disturbance observer (DOB) [36] based compensator, consisting of nominal controller (here, K_{PV}) and disturbance observer (here, UDE). Therefore, even though proportional nominal controller is used in the subsequent derivations to shape the tracking response, a more advanced compensator (e.g. PID, PR etc) may in general replace K_{PV} .

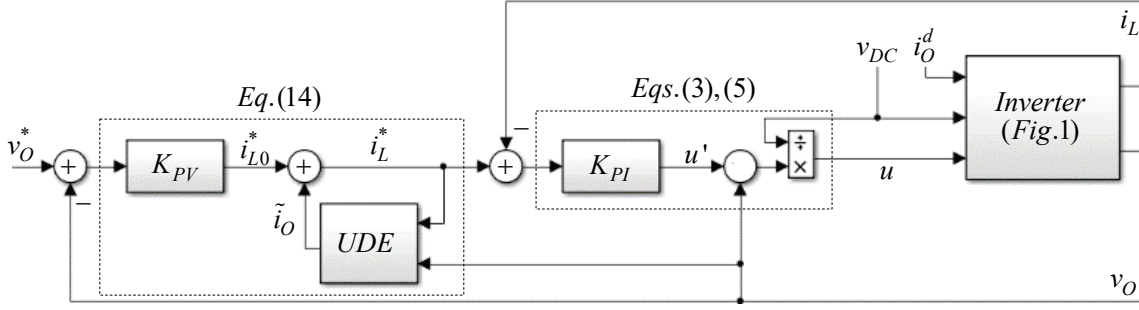


Fig. 4. The proposed control structure.

Taking Laplace transform of (14) and rearranging, there is

$$I_L^*(s) = C_n \underbrace{\left(\frac{\omega_R}{1-G(s)} V_O^*(s) \right)}_{H_{FF}(s)} - \underbrace{\left(\frac{\omega_R + sG(s)}{1-G(s)} V_O(s) \right)}_{H_{FB}(s)}. \quad (15)$$

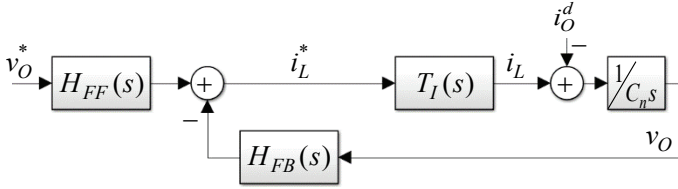


Fig. 5. Equivalent voltage loop diagram.

The overall voltage loop structure is shown in Fig. 5 with $T_I(s)$ playing the actuator role. Corresponding loop gain is then

$$L_V(s) = \frac{\omega_R + sG(s)}{s(1-G(s))} T_I(s), \quad (16)$$

indicating infinite gain at DC and frequencies associated with the roots of $1-G(s)$. Substituting (15) into (8) and rearranging results in the following closed-loop dynamics,

$$V_O(s) = \frac{H_{FF}(s)T_I(s)}{s + H_{FB}(s)T_I(s)} V_{OR}^*(s) - \frac{C_n^{-1}}{s + H_{FB}(s)T_I(s)} I_O^d(s). \quad (17)$$

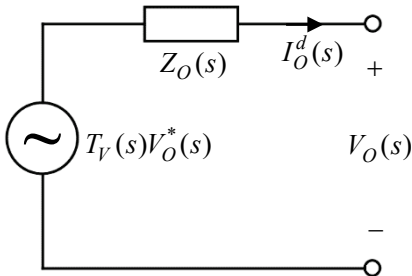


Fig. 6. Equivalent model of the single-phase inverter.

The inverter under the proposed closed loop control can then be modeled as a series connection of voltage source $T_V(s)V_O^*(s)$ and an output impedance $Z_O(s)$, as shown in Fig. 6, taking the voltage $V_O(s)$ as the output voltage and the current $I_O^d(s)$ as the output current. Obviously, it is expected that $T_V(s) \rightarrow 1$ in order to achieve good tracking performance and

$Z_O(s) \rightarrow 0$ in order to achieve good disturbance rejection at relevant frequencies. For the case of tracking problem, assume the total uncertainty and disturbance current and output voltage reference are given by

$$i_O^d(t) = \sum_{n=1}^{\infty} I_n \sin(n\omega_0 t + \phi_n) \quad (18)$$

and

$$v_O^*(t) = V_M^* \sin \omega_0 t, \quad (19)$$

respectively. Then, there is

$$\begin{aligned} v_O(t) &= V_M^* \sin \omega_0 t - \sum_{n=1}^{\infty} I_n |Z_O(n\omega_0)| \sin(n\omega_0 t + \phi_n + \arg Z_O(n\omega_0)) \\ &= v_{O1}(t) + v_{OH}(t), \end{aligned} \quad (20)$$

where

$$\begin{aligned} v_{O1}(t) &= V_M^* \sin(\omega_0 t) - I_1 |Z_O(\omega_0)| \sin(\omega_0 t + \phi_1 + \arg Z_O(\omega_0)) \\ &= V_1 \sin(\omega_0 t + \theta) \end{aligned} \quad (21)$$

with

$$\begin{aligned} V_1 &= \sqrt{(V_M^*)^2 + (I_1 |Z_O(\omega_0)|)^2 - 2V_M^* I_1 |Z_O(\omega_0)| \cos(\phi_1 + \arg Z_O(\omega_0))} \\ \theta &= \tan^{-1} \frac{\omega_0 |Z_O(\omega_0)| \sin(\phi_1 + \arg Z_O(\omega_0))}{I_1 |Z_O(\omega_0)| \cos(\phi_1 + \arg Z_O(\omega_0)) - V_M^*}; \end{aligned}$$

and

$$v_{OH}(t) = -\sum_{n=2}^{\infty} I_n |Z_O(jn\omega_0)| \sin(n\omega_0 t + \phi_n + \arg Z_O(jn\omega_0)). \quad (22)$$

It should be emphasized that v_{O1} and v_{OH} are orthogonal and hence decoupled. As is well known, the quality of the output voltage is typically quantified by the total harmonic distortion (THD) defined as

$$THD_V = \frac{\sqrt{\sum_{n=2}^{\infty} (I_n |Z_O(jn\omega_0)|)^2}}{V_1}. \quad (23)$$

Obviously, it is mainly influenced by the magnitude of output impedance at harmonic frequencies (typically odd multiples of base frequency in single phase systems and $6n \pm 1$ in three-phase applications). Hence, it is desirable to reduce the latter as much as possible in order to minimize THD_V . Nevertheless, observing (21) reveals that even if THD_V is minimized, v_O and v_O^* may still differ due to the voltage drop on the output

impedance at base frequency $|Z_O(\omega_0)|$. Consequently, it is desirable to reduce $|Z_O(n\omega_0)|$ for $n = 1 \dots N$ with N denoting the order of the highest load harmonic possessing significant energy.

III. DESIGN OF UDE-BASED VOLTAGE CONTROLLER

In case $T_I(s) = 1$, (17) reduces to

$$V_O(s) = \underbrace{\frac{\omega_R}{s + \omega_R}}_{T_V(s)} V_{OR}(s) - \underbrace{\frac{C_n^{-1}}{s + \omega_R} (1 - G(s))}_{Z_O(s)} I_O^d(s). \quad (24)$$

Hence, voltage loop complementary sensitivity function $T_V(s)$ follows that of reference model (9) while tracking is decoupled from disturbance rejection by $G(s)$, as expected from [23]. In addition, output impedance $Z_O(s)$ is formed by series connection of two frequency-selective filters: $Z_{O1}(s) = C_n^{-1}(s + \omega_R)^{-1}$ and $Z_{O2}(s) = 1 - G(s)$. This means the output impedance can be designed by selecting a suitable UDE-filter $G(s)$. Apparently, in case $C_n^{-1} > \omega_R$, the magnitude of $Z_{O1}(s)$ is greater than 0dB for frequencies below $\omega = \sqrt{C_n^{-2} - \omega_R^2}$. Therefore, in order to reduce the output impedance, ω_R should be increased as much as possible (this would also improve tracking). Alternatively, output impedance may be reduced by imposing $Z_{O2}(s)$ as close to zero as possible at relevant frequencies. Unfortunately, since $T_I(s)$ serves as the voltage loop actuator, available control bandwidth for given stability margins is limited. Therefore, tracking – disturbance rejection trade-off is expected to appear. The design is then carried out as follows. First, minimum tracking bandwidth $\omega_{R,MIN}$ is set. Then, $G(s)$ is selected to minimize the magnitude of $Z_O(s)$ while respecting minimum allowed stability margins. In the subsequent analysis, $\omega_{R,MIN} = 10 \cdot \omega_0$ is designated to assure decent tracking and minimum stability margins are set to 45° and 6dB, respectively.

A. Maximizing tracking bandwidth

As mentioned above, two-degrees-of-freedom control structures possess tracking/disturbance rejection trade-off. In case disturbance rejection is compromised, tracking may be enhanced. It is therefore possible to maximize the tracking bandwidth by setting $G(s) = 0$. The loop gain is then given by

$$L_V(s) = \frac{\omega_R}{s} \frac{K_{PI} L^{-1}}{se^{T_d s} + K_{PI} L^{-1}} \quad (25)$$

and hence $\omega_R = \omega_{R,MAX} = 2\pi \cdot 1196$ rad/s may be achieved, bringing the system to the 6dB gain margin limit, as shown in Fig. 7a. Unfortunately, the resulting output impedance magnitude would be higher than 0dB for frequencies below $2\pi \cdot 5170$ rad/s (cf. Fig. 7b), i.e. all the significant base frequency multiples harmonics of the load current will be amplified.

B. Typical UDE filters based design

Most of the applications employing UDE-based controllers utilize first order low pass Butterworth filters. Nevertheless, as stated in [23], [37] increasing filter order/decreasing relative degree/increasing cutoff frequency improve disturbance rejection. Unfortunately, it is further shown than under

bandwidth constraints, trade-off exists between the three. The consequences of utilizing different low pass Butterworth filters as UDE filters were investigated by applying the filters summarized in Table II (only strictly proper filters were considered in order to assure implementability of $sG(s)$ in (15)).

TABLE II.
LOW PASS BUTTERWORTH FILTERS

order	$\omega_R/2\pi$	$\omega_F/2\pi$	$G(s)$
0	1196	0	0
1	500	664	$\frac{\omega_F}{s + \omega_F}$
20	500	530	$\frac{\omega_F^2}{s^2 + 1.41\omega_F \cdot s + \omega_F^2}$
21	500	393	$\frac{1.41\omega_F s + \omega_F^2}{s^2 + 1.41\omega_F s + \omega_F^2}$
32	500	279	$\frac{2\omega_F s^2 + 2\omega_F^2 s + \omega_F^3}{s^3 + 2\omega_F s^2 + 2\omega_F^2 s + \omega_F^3}$
43	500	215	$\frac{2.61\omega_F s^3 + 3.41\omega_F^2 s^2 + 2.61\omega_F^3 s + \omega_F^4}{s^4 + 2.61\omega_F s^3 + 3.41\omega_F^2 s^2 + 2.61\omega_F^3 s + \omega_F^4}$

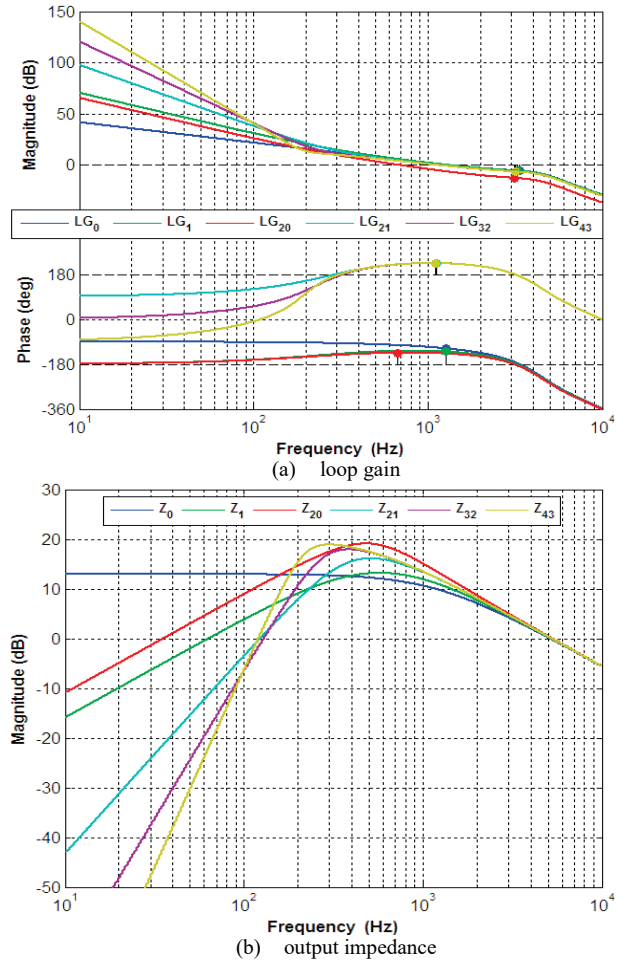


Fig. 7. Voltage loop performance merits utilizing filters of Table II.

The tracking bandwidth was set to $\omega_{R,MIN}$ and then filter cutoff frequency satisfying the above-set minimum stability margins was determined. Figs. 7a and 7b demonstrate corresponding loop gains (LG) and output impedances, respectively. Two important conclusions may be then drawn:

- Even though the cutoff frequency of the filter $G_{20}(s)$ is higher than that of $G_{21}(s)$, disturbance rejection capabilities of the latter are better, i.e. decreasing relative degree increases disturbance rejection. Hence, only filters with relative degree of one were considered further.

- Increasing filter order forces reducing the cut-off frequency yet improves low-frequency disturbance rejection (see the value of output impedance magnitude at base frequency). Unfortunately, medium-frequency disturbance rejection is deteriorated (the values of output impedance magnitude at [100Hz, 2000Hz] frequency range are higher than 0dB). Consequently, increasing filter order does not necessarily reduce THD, which eventually depends on the harmonic content of load current.

To conclude, utilizing low pass UDE filters under given bandwidth restrictions is insufficient to reduce the output impedance below 0dB at frequency range where load current is expected to possess significant energy.

C. Shaping of the output impedance

Note that $Z_{O2}(s)$ rather than $G(s)$ directly affects the output impedance. Therefore, it is suggested to select $Z_{O2}(s)$ and then derive the UDE filter as $G(s) = 1 - Z_{O2}(s)$. Since output impedance minimization is required only at base frequency multiples, it is proposed to construct $Z_{O2}(s)$ as a bank of series connected band-stop filters,

$$Z_{O2}(s) = \prod_{n=1}^N H_n(s), \quad (26)$$

where n -th harmonic filter stop band is given by $[n\omega_0/k, n\omega_0/k]$ with $k < 1$, of which the ideal shape is shown in Fig. 8. Obviously, in order to increase filter robustness to fundamental frequency variations, the bandwidth of each filter should be maximized, i.e. k should be chosen as small as possible. Unfortunately, it is impossible to freely increase the overall stop band of $Z_{O2}(s)$ without violating the minimum stability margins due to limited available control bandwidth. Consequently, maximum attainable stop band is shared by n filters, i.e. trade-off exists between the number of series connected filters (N) and the bandwidth of each filter (k).

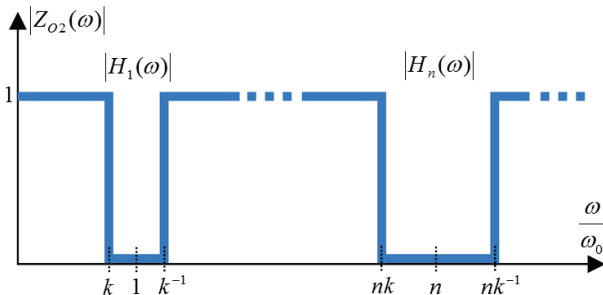
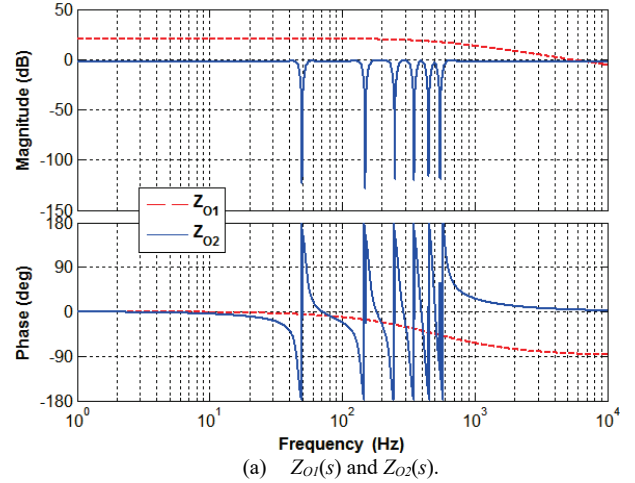


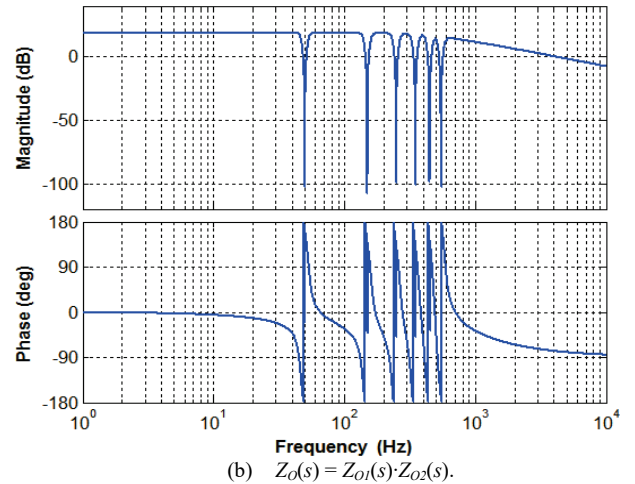
Fig. 8. Ideally desired magnitude of $Z_{O2}(s)$.

In this work, elliptic band-stop filters were employed due to their ability to attain a given transition width with the smallest order [38]. $Z_{O2}(s)$ was constructed by series connection of 6 second-order filters ($n = 1, 3, 5, 7, 9, 11$) with pass-band and stop-band ripples of 0.35dB and 60dB, respectively. In order to comply with minimum stability margins, the smallest attainable value of k was found to be

0.89. The magnitude response of designed $Z_{O2}(s)$ is shown in Fig. 9a together with that of $Z_{O1}(s) = C_n^{-1}(s+\omega_{R,MIN})^{-1}$ and the resulting output impedance is depicted in Fig. 9b. It is interesting to note that $Z_O(s)$ is resistive at harmonic frequencies. Since the magnitude Z_{O1} remains around 20dB throughout the region of interest, the worst-case magnitude of the impedance around harmonic frequencies is -40dB, as shown in Fig. 10.



(a) $Z_{O1}(s)$ and $Z_{O2}(s)$.



(b) $Z_O(s) = Z_{O1}(s) \cdot Z_{O2}(s)$.

Fig. 9. Output impedance and its components.

Note that compared to the $G(s) = 0$ case, the magnitude of output impedance is above 0dB for all but six relevant frequencies below $2\pi \cdot 5170$ rad/s. Nevertheless, values of output impedance magnitude at frequencies other than in the vicinity of harmonic frequencies are not important. Hence, any harmonic load is expected to be well rejected by the inverter. Moreover, it is apparent that the magnitude of the impedance remains below -10dB in case the base frequency deviates ± 1 Hz around its nominal value, demonstrating the robustness. Bode plot of the corresponding UDE filter $G(s) = 1 - Z_{O2}(s)$ is shown in Fig. 11. It is important to emphasize that the latter possesses unity magnitude and zero phase at the first six base frequency multiples, as desired. Fig. 12 demonstrates the resulting loop gain. It is interesting to note that the gain margin of ~ 6 dB is the limiting factor and not the phase margin ($\sim 65^\circ$).

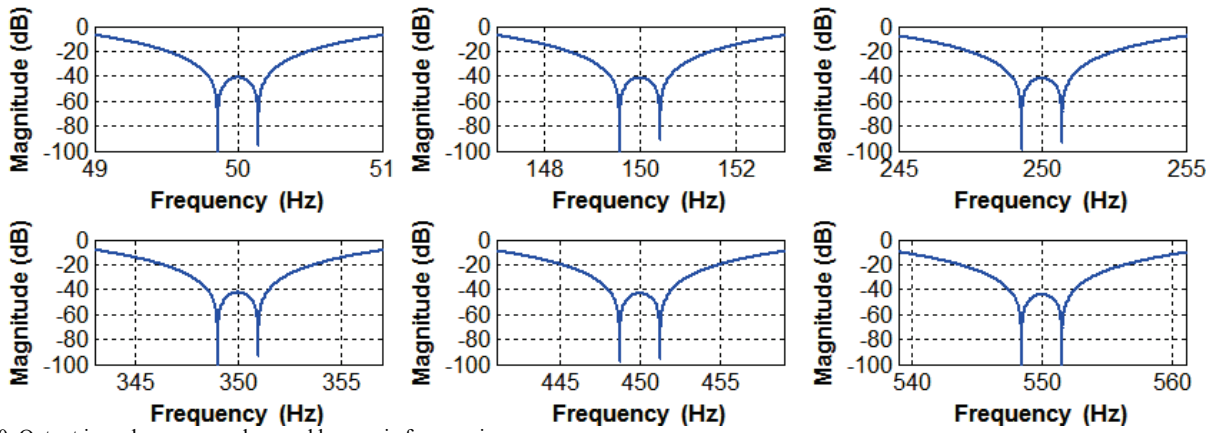


Fig. 10. Output impedance zoomed around harmonic frequencies.

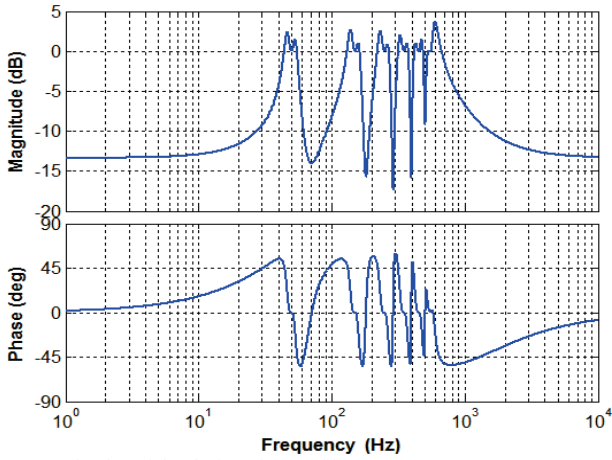


Fig. 11. Bode plot of the designed UDE filter $G(s) = 1 - Z_{O2}(s)$.

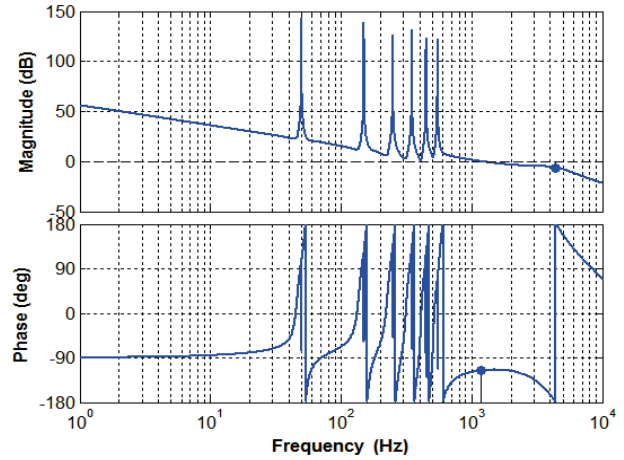


Fig. 12. The resulting voltage loop gain.

IV. EXPERIMENTAL VERIFICATION

In order to validate the proposed control system, modified Texas Instruments High Voltage Single Phase Inverter Development Kit (TIDK) was utilized. The inverter was initially loaded by a 33Ω resistor to establish a baseline; then, the resistor was replaced by a diode rectifier (DR) with heavy RC load, as shown in Fig. 13a. Corresponding nonlinear load parameter values summarized in Table III. Inverter parameters of the experimental setup match the values given in Table I. The control system was implemented digitally using Concerto F28M35 control card. The setup is pictured in Fig. 13b.

TABLE III.
NONLINEAR LOAD PARAMETER VALUES

Parameter	Value	Units
Load resistance, R_L	50	Ω
Load capacitance, C_L	940	μF

In the first experiment, current loop performance was examined by verifying the step response under short-circuit conditions. The result is shown in Fig. 14. According to the target current loop bandwidth of 2762Hz, $288\mu s$ is the expected five-time-constants transient duration, which is well verified.

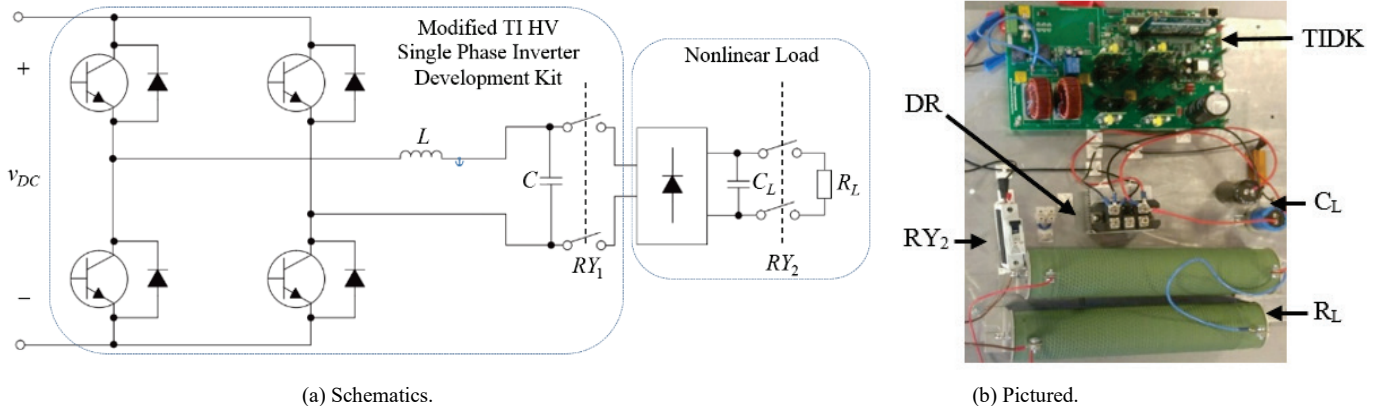


Fig. 13. Experimental hardware with nonlinear load connected.

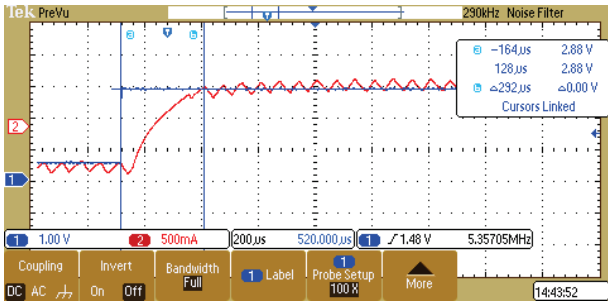
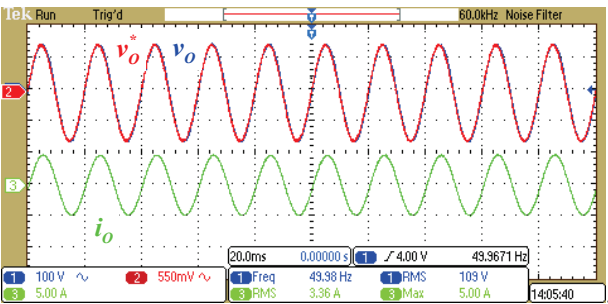
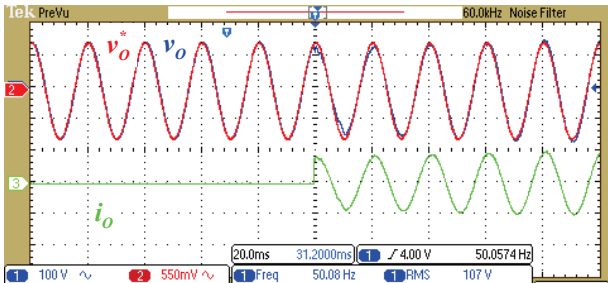


Fig. 14. Experimental results: Current-loop step response.

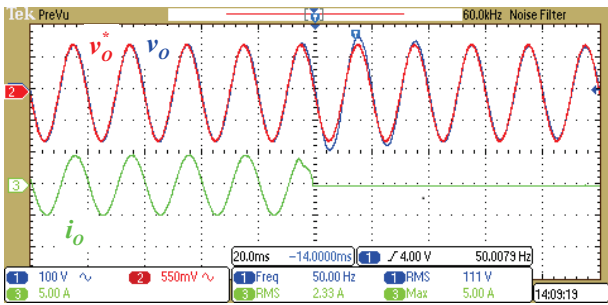
In the second experiment, nominal base frequency system operation was validated under both linear and nonlinear loads. Output voltage reference signal was set to (19) with $V_M^* = 110\sqrt{2}V$. Steady state, operation, no-load to full-load and full-load to no-load transitions are depicted in Figs. 15 and 16 for linear and nonlinear loads, respectively.



(a) steady state.



(b) no-load to full-load transition.

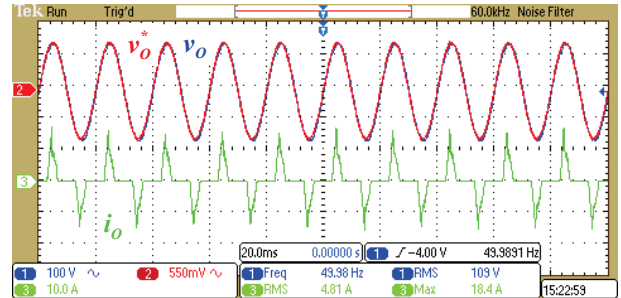


(c) full-load to no-load transition.

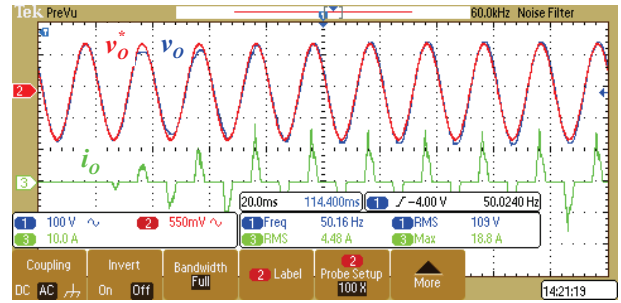
Fig. 15. Experimental results: Operation under linear load, nominal base frequency.

It may be concluded that the system operates well under both types of load in steady state. Fig. 17 demonstrates respective experimental frequency domain distributions and total harmonic distortions of the output voltage. The linear load case $THD_V = 0.87\%$ may actually serve as a baseline,

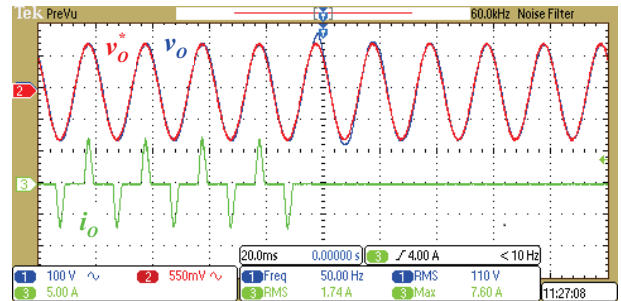
defining the noise floor. Observing the results of operation under nonlinear load, while taking the baseline into account, it may be concluded that voltage harmonics up to 11th are nearly absent, as planned. Corresponding experimental THD_V was obtained as 2.05%, validating excellent control algorithm performance.



(a) steady state.



(b) no-load to full-load transition.



(c) full-load to no-load transition.

Fig. 16. Experimental results: Operation under nonlinear load, nominal base frequency.

On the other hand, it takes around one cycle for the system to settle in both cases. This transient performance is satisfactory but might not be optimal due to the relatively large convergence time of the multi-band-stop-filter utilized. This is the price to pay for the excellent steady state performance.

For the sake of comparison, the system was also tested under nonlinear loading employing typical UDE controller with first and third order low pass Butterworth filters (cf. Table II). Corresponding frequency domain distributions (time-domain results are omitted for brevity) and THD_V values are depicted in Fig. 18 and compared to steady state operation with the multi-band-stop filter. Apparently, UDE controller equipped with the proposed filter outperforms the classical one for both low pass filter types.

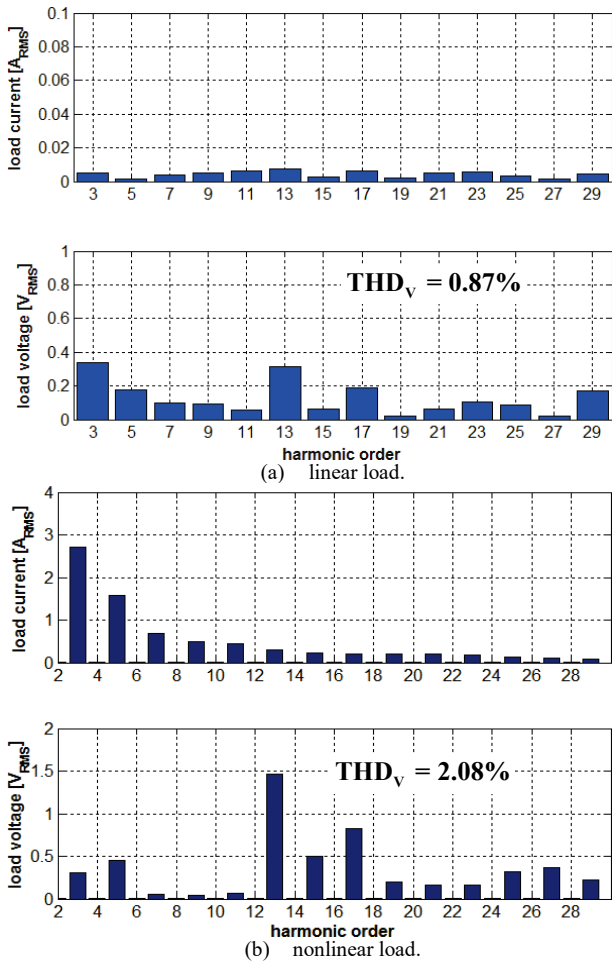


Fig. 17. Experimental results: Spectra of output voltage and current.

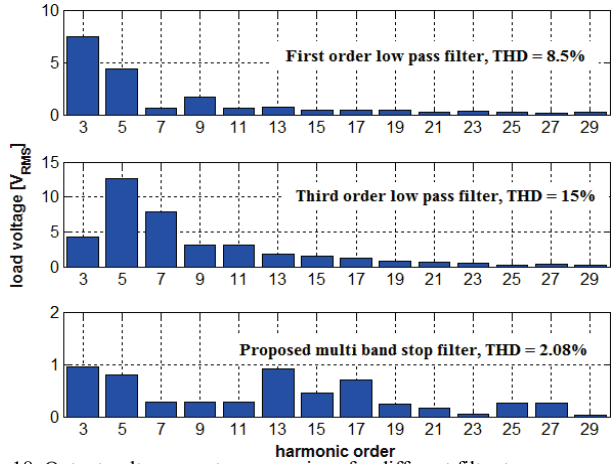


Fig. 18. Output voltage spectra comparison for different filter types.

In the last experiment, steady-state operation of nonlinearly loaded system was inspected under fundamental frequency deviation up to ± 1 Hz to verify the robustness. Experimental results are shown in Fig. 19 with corresponding values of THD_V summarized in Fig. 20 along with their corresponding simulated values. Apparently, THD_V remains low despite base frequency variations and is in good agreement with simulations.

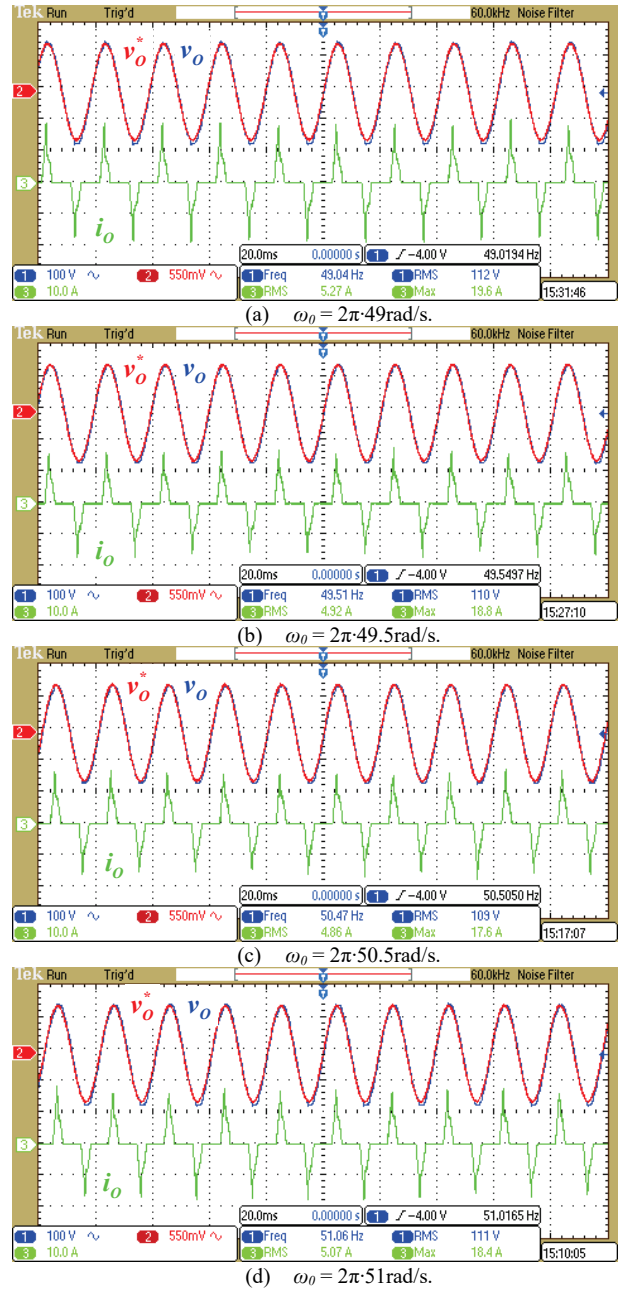


Fig. 19. Experimental results. Steady state operation under ± 1 Hz base frequency deviation.

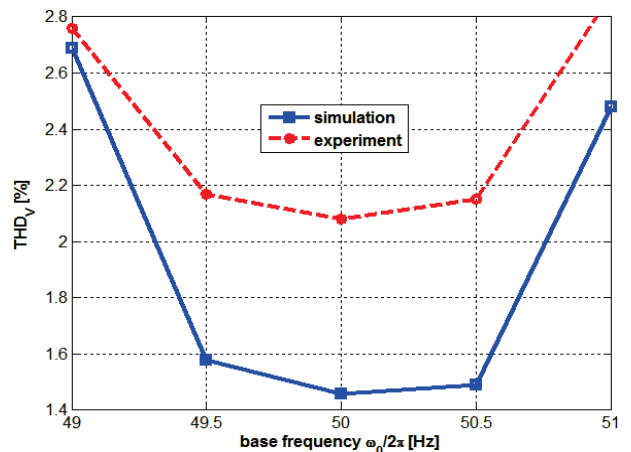


Fig. 20. Simulated and experimental THD_V under base frequency deviation.

V. CONCLUSIONS

It has been shown in the paper that it is possible to directly construct inverter output impedance utilizing uncertainty and disturbance estimator algorithm, owing to its two-degree-of-freedom structure. Once desired tracking performance is established, it is possible to shape the output impedance by selecting a proper filter. In case output impedance minimization is desired to reduce the total harmonic distortion of the output voltage, multi-band-stop filter structure may be utilized. Moreover, robustness to base frequency variation was assured by increasing the bandwidth of each filter. Nevertheless, if other output impedance manipulation is looked-for, respective filter may be in general designed. It was shown that several trade-offs exist due to limited control bandwidth and should be properly managed to achieve the best results. Theoretical findings were well-validated by experimental results.

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6. UDE-Based Controller Equipped with a Time-Delayed Filter to Improve the Voltage Quality of Inverters

Publication number 2 –

Gadelovits, Shlomo Yaakov, et al. "UDE-Based Controller Equipped with a Time-Delayed Filter to Improve the Voltage Quality of Inverters." *IEEE Transactions on Industrial Electronics* (2018).

Nomenclature

a, b	System model equation coefficients
a_n, b_n	System nominal model equation coefficients
C	Output filter capacitance
$C_I(s)$	Current loop compensator transfer function
C_n	Nominal output capacitance
$C_t(s)$	Tracking controller compensator transfer function
d	Total uncertainty and disturbance
f	Disturbance input
g_f	Impulse response of UDE filter
$H_f(s)$	Disturbance rejection transfer function
$H_{FB}(s)$	Voltage controller feedback transfer function
$H_{FF}(s)$	Voltage controller feedforward transfer function
i_L	Inductor current
i_o	Output current
K_{PI}	PI controller gain
$\mathcal{L}^{-1}\{\cdot\}$	Inverse Laplace operator
L	Output filter inductance
$L_f(s)$	Disturbance rejection controller loop-gain
$LG_I(s)$	Current loop gain
$L_t(s)$	Tracking loop gain
$L_{tot}(s)$	Overall loop gain
T_0	Base frequency period time
T_d	Time delay
$T_I(s)$	Current loop tracking transfer function

T_y	Closed loop tracking transfer function
u	System input
u'	Current loop output
u_d	Disturbance rejection controller output
u_t	Tracking controller output
v_{DC}	DC bus voltage
v_o	Output voltage
$W(s)$	Low pass filter
y	System output
y^*	System output reference
Z_o	Inverter output impedance
ΔT	Filter time delay at base frequency
τ_I	PI controller time-constant
ϕ	Phase
ω_0	Base frequency
ω_F	UDE filter bandwidth
ω_t	Magnitude convergence rate

For signals represented both time-domain and s-domain, z-domain, or frequency domain, lower case represents time domain signals and uppercase s, z or frequency domain signals.

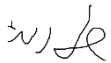
List of amendments to the original published version

1. All the missing underbraces has been corrected
2. The inverse Laplace transform notation has been changed from $L^{-1}\{\cdot\}$ to $\mathcal{L}^{-1}\{\cdot\}$
3. In page 5, τ has been changed to τ_1

Statement of contribution for the author Shlomo Gadelovits

The author Shlomo Gadelovits proposed to add half cycle-delay to the classic UDE filter low-pass design in order to reduce the filter phase to zero around the odd-harmonics and to improve the transient performance. He also designed and obtained results for all the experiments shown in the paper and wrote the main body of work.

Shlomo Y Gadelovits



Alon Kuperman



Qing-Chang Zhong



Visakan Kadiramanathan



UDE-Based Controller Equipped with a Time-Delayed Filter to Improve the Voltage Quality of Inverters

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V. Kadiramanathan, and A. Kuperman, *Senior Member, IEEE*

Abstract—In this paper, a two-degrees-of-freedom control structure is proposed to minimize both total harmonic distortion and tracking error of inverter output voltage, based on resonant tracking controller and modified uncertainty and disturbance estimator (UDE). Owing to the two-degree-of-freedom feature of the proposed control strategy, tracking and disturbance rejection tasks are decoupled and treated almost independently. A time-delay action is introduced into a commonly adopted low-pass UDE filter to minimize the output impedance magnitude around the odd harmonics, typical to nonlinear loads. Once the disturbance is properly rejected, a tracking resonant controller is designed to force the output of the nominal system to follow a sinusoidal reference with near-zero amplitude and phase error. The performance of the proposed control structure is fully verified by experimental results.

Index Terms—Uncertainty and disturbance estimator, inverter, resonant control, voltage quality, two degrees of freedom control.

I. INTRODUCTION

DC-AC converters (or inverters) have recently become a crucial element in power conversion associated applications [1]. Consequently, a vast amount of research is being conducted in the field of inverters control. Among others, reducing the total harmonic distortion (THD) and minimizing the output voltage tracking error of inverter feeding a nonlinear load are common control tasks. A variety of control strategies have been proposed in the literature to cope with the THD improvement problem [2] – [12]. It was recently understood, that THD minimization task is directly related to inverter output impedance [1]. In [13], the output impedance of an inverter was shown to be influenced by the control strategy adopted. Therefore, reducing the output impedance magnitude may enhance output voltage quality [1], [14] – [16]. It should be emphasized that when driving nonlinear loads, only the values of inverter output impedance magnitude at harmonic frequencies are of interest for THD reduction. Moreover, in single-phase inverters, odd harmonics only should be treated. In [17] – [23], multi-resonant controllers were proposed to reduce the output voltage THD by minimizing output impedance magnitude at multiples of the base operating frequency. However, classical multi-resonant control structures are of the single-degrees-of-freedom type and hence do not allow decoupling of tracking and disturbance rejection.

Disturbance observer (DOB) based controllers [24] – [26] are probably the most widely used two-degrees-of-freedom structure, allowing the aforementioned decoupling to be attained. There, the DOB nominalizes the system [27] by estimating and compensating the total uncertainty and disturbance while a tracking controller is only concerned with forcing the nominal system to follow the reference precisely. In [28], a subset of DOB named Uncertainty and Disturbance Estimator (UDE) was utilized to solve the problem of inverter output voltage quality. UDE was initially proposed in [30], elaborated in [31] – [38] and applied to a variety of control tasks [39] – [48]. Its functionality is based on the assumption that appropriate filtering can approximate any continuous uncertainty and disturbance and then compensate it by opposite phase injection. It was shown in [28] that the two-degrees-of-freedom controller may directly impose disturbance rejection through the output impedance by appropriate filter design without sensing the output current. In addition, the proposed multi-band-stop-filter structure was capable of both reducing the value of output impedance magnitude around the regions of interest and provided robustness to fundamental frequency variations. The main drawbacks of the method proposed in [28] is the effort required to obtain the required filter type and order, in addition to cumbersome structure, whose complexity increases according to the amount of harmonics to be treated (similar to multi-resonant controllers).

In this paper, a UDE-based controller equipped with a different filter is proposed to tackle the disturbance rejection task. The proposed filter resembles a classical UDE filter with a slight modification based on introducing a time delay into the estimator structure [49]. This results in a repetitive-like action [50], translated into enhanced disturbance rejection capabilities at base frequency multiples, as desired. The proposed filter is easy to implement and the resulting structure is of low complexity. In order to cope with the tracking task, a resonant controller (rather than proportional one in [28]) is utilized, allowing the transient response to be shaped according to prescribed behavior [51]. A combination of resonant and repetitive control was used in [52] – [54] using different control structures, yielding excellent performance and providing additional motivation to this work. Performance comparison between the system in [28] and the one proposed here reveals the superiority of the latter in terms of both output voltage THD and settling time under the same operating conditions. On the other hand, the robustness to base frequency variations of the former is superior to that of the algorithm proposed here.

The rest of the paper is organized as follows. The proposed control algorithm is presented in general form in Section II, while its application to enhancing voltage quality of inverters is described in Section III. Experimental validation of the proposed method is given in Section IV and conclusions are drawn in Section V.

II. THE PROPOSED ALGORITHM

Consider a stable uncertain linear SISO system with disturbance,

$$\begin{aligned} \dot{y}(t) &= -ay(t) + b(u(t) + f(t)) \\ &= -(a_n + \Delta a)y(t) + (b_n + \Delta b)(u(t) + f(t)), \end{aligned} \quad (1)$$

where $y(t)$ is the system output, a_n and Δa are nominal (or known) and unknown parts of $a > 0$, respectively, $u(t)$ is the control input, b_n and Δb are nominal (or known) and unknown parts of b , respectively, and $f(t)$ is the external disturbance. The system output $y(t)$ is desired to track a reference signal given by

$$y^*(t) = A \sin \omega_0 t \quad (2)$$

while rejecting the disturbance described by

$$f(t) = \sum_{n=1}^{\infty} F_n \sin(n\omega_0 t + \phi_n). \quad (3)$$

Rearranging (1), there is

$$\dot{y}(t) = -a_n y(t) + b_n (u(t) + d(t)) \quad (4)$$

with

$$d(t) = b_n^{-1} (-\Delta a y(t) + \Delta b u(t) + b f(t)) \quad (5)$$

denoting the total uncertainty and disturbance (TUD). Note that according to (2), (3) and (5), TUD may be expressed as

$$d(t) = \sum_{n=1}^{\infty} D_n \sin(n\omega_0 t + \theta_n). \quad (6)$$

In order to accomplish both above mentioned goals, it is proposed to utilize a two-degree-of-freedom structure by splitting the control signal as

$$u(t) = u_t(t) + u_d(t), \quad (7)$$

where $u_t(t)$ and $u_d(t)$ denote the outputs of tracking controller and disturbance observer, respectively. It is shown next that both controllers may be designed independently as long as the total available control bandwidth is not violated.

A. Disturbance observer

Substituting (7) into (4), there is

$$\dot{y}(t) = -a_n y(t) + b_n (u_t(t) + u_d(t) + d(t)) \quad (8)$$

If $u_d(t) \approx -d(t)$, then the TUD would be cancelled and the system would become nominalized. However, $d(t)$ contains uncertain and non-measurable terms, hence it should be properly estimated. Note that TUD may be derived from (8) as

$$d(t) = b_n^{-1} (\dot{y}(t) + a_n y(t)) - u_t(t) - u_d(t). \quad (9)$$

Unfortunately, (9) cannot be utilized because of causality issues. UDE-based control estimates the TUD by passing it through a linear filter $G_f(s)$, possessing near-unity gain and near-zero phase over the frequency range where the energy of $d(t)$ is non-zero, i.e.

$$u_d(t) = d(t) * g_f(t), \quad (10)$$

where '*' is the convolution operator and $g_f(t)$ is the impulse response of $G_f(s)$. Combining (8) – (10) and rearranging gives

$$\begin{aligned} u_d(t) &= \mathcal{L}^{-1} \left\{ \frac{G_f(s)}{H_f(s)} (-P_n^{-1}(s)Y(s) + U_t(s)) \right\} \\ &= \mathcal{L}^{-1} \left\{ L_f(s) (-P_n^{-1}(s)Y(s) + U_t(s)) \right\} \end{aligned} \quad (11)$$

with $\mathcal{L}^{-1}\{\cdot\}$ symbolizing the inverse Laplace transform operator, $Y(s)$ and $U_t(s)$ denoting Laplace transforms of $y(t)$ and $u_t(t)$, respectively, $L_f(s) = G_f(s)/H_f(s)$ signifying disturbance rejection loop gain and

$$H_f(s) = 1 - G_f(s), \quad P_n(s) = \frac{b_n}{s + a_n}. \quad (12)$$

Further substituting (11) into (8) results in

$$\dot{y}(t) = -a_n y(t) + b_n (u_t(t) + \mathcal{L}^{-1} \{ D(s) \cdot H_f(s) \}), \quad (13)$$

with $D(s)$ denoting the Laplace transform of $d(t)$. According to (13), in the case of $G_f(s) = 1$ (or $H_f(s) = 0$) at multiples of the base frequency ω_0 , the TUD will be rejected completely (cf. (3)).

In order to design suitable $G_f(s)$, note first that the following holds in steady state,

$$d(t) = d(t - T_0) \quad (14)$$

with $T_0 = 2\pi/\omega_0$, i.e.

$$u_d(t) = d(t - T_0) \quad (15a)$$

Or

$$U_d(s) = D(s) \cdot \underbrace{e^{-T_0 s}}_{G_f(s)} \quad (15b)$$

may be utilized as an estimate of TUD, i.e.

$$H_f(s) = 1 - e^{-T_0 s}, \quad (16)$$

which is a time-delayed filter extensively investigated in [55–57].

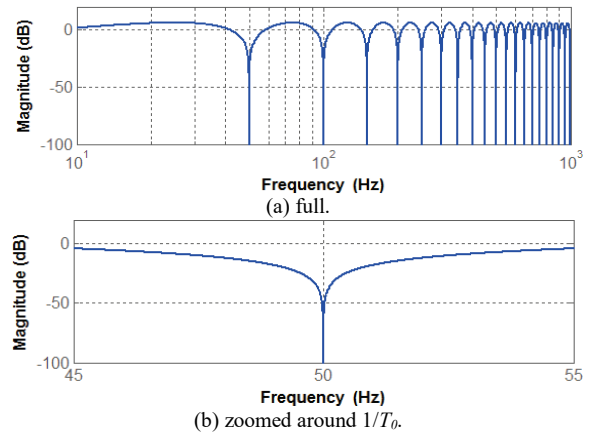


Fig. 1. Bode diagram of $|H_f(s)|$ in (16) for $T_0 = 20$ ms.

Bode diagram of (16) is shown in Fig. 1 for $T_0 = 20$ ms. It is evident that $H_f(s)$ possesses zero magnitude at 50 Hz multiples, as desired. Unfortunately, the filter is characterized by infinite bandwidth as well and therefore cannot be realized as is. It is possible to restrict the filter bandwidth by modifying (15) as

$$u_d(t) = d(t - T_0) * w(t) \quad (17a)$$

or

$$U_d(s) = D(s) \cdot \underbrace{e^{-T_0 s} W(s)}_{G_f(s)} \quad (17b)$$

with $w(t)$ and $W(s)$ denoting impulse response of a low-pass filter and its corresponding Laplace transform. This gives

$$H_f(s) = 1 - e^{-T_0 s} W(s). \quad (18)$$

However, $G_f(s) \neq 1$ for any practical $W(s)$ at multiples of ω_0 .

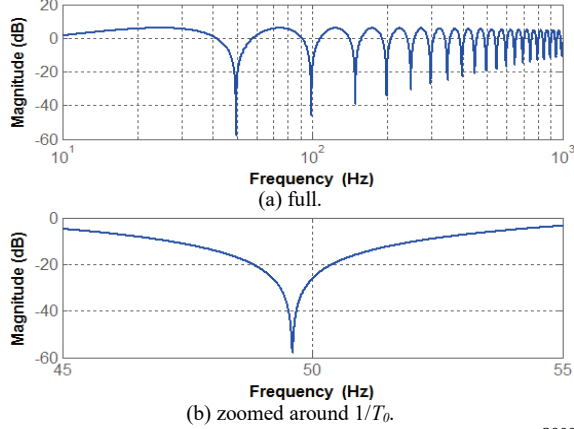


Fig. 2. Bode diagram of $|H_f(s)|$ in (18) for $T_0 = 20$ ms and $W(s) = \frac{2000\pi}{s+2000\pi}$.

As a result, the magnitude of $H_f(s)$ would be different than zero at these frequencies. A Bode diagram of (18) is shown in Fig. 2(a) for $T_0 = 20$ ms and $W(s) = \frac{2000\pi}{s+2000\pi}$. As shown in Fig. 2(b), the valleys of $|H_f(s)|$ are now shifted to the left from desired positions, their corresponding values are nonzero and they are increasing for higher frequencies. While the latter may be acceptable in practical systems since D_n in (6) decreases as n increases, non-accurate valley positions may significantly deteriorate the disturbance rejection performance. The valley position shift is caused by the filter-induced phase lag. Therefore, it is suggested to reduce the delay time in (17) as

$$u_d(t) = d(t - (T_0 - \Delta T)) * w(t) \quad (19a)$$

or

$$U_d(s) = D(s) \cdot \underbrace{e^{-(T_0 - \Delta T)s} W(s)}_{G_f(s)}, \quad (19b)$$

where ΔT is the delay of $W(s)$ at ω_0 . This gives

$$H_f(s) = 1 - e^{-(T_0 - \Delta T)s} W(s). \quad (20)$$

A Bode diagram of (20) is shown in Fig. 3(a) for $T_0 = 20$ ms, $W(s) = \frac{2000\pi}{s+2000\pi}$ and $\Delta T = -\frac{1}{\omega_0} \text{tg}^{-1}\left(\frac{\omega_0}{2000\pi}\right)$. It is evident from Fig. 3(b) that the position of the valleys of $|H_f(s)|$ are restored to the desired locations.

In case the TUD in (6) possesses odd symmetry, it would contain odd harmonics only [58]. Then, (14) may be rewritten as

$$d(t) = -d\left(t - \frac{T_0}{2}\right) \quad (21)$$

and (19) becomes

$$u_d(t) = -d\left(t - \left(\frac{T_0}{2} - \Delta T\right)\right) * w(t) \quad (22a)$$

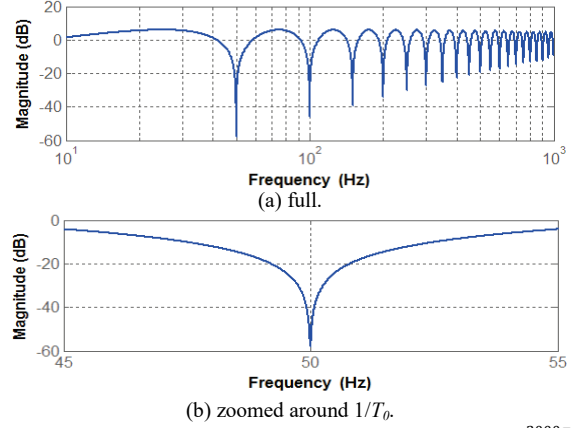


Fig. 3. Bode diagram of $|H_f(s)|$ in (20) for $T_0 = 20$ ms, $W(s) = \frac{2000\pi}{s+2000\pi}$ and $\Delta T = -\frac{1}{\omega_0} \text{tg}^{-1}\left(\frac{\omega_0}{2000\pi}\right)$.

$$W(s) = \frac{2000\pi}{s+2000\pi} \text{ Or } U_d(s) = D(s) \cdot \underbrace{\left(-e^{-\left(\frac{T_0}{2} - \Delta T\right)s} W(s)\right)}_{G_f(s)}. \quad (22b)$$

This gives

$$H_f(s) = 1 + e^{-\left(\frac{T_0}{2} - \Delta T\right)s} W(s). \quad (23)$$

Bode diagram of (23) is shown in Fig. 4(a) for $T_0 = 20$ ms, $W(s) = \frac{2000\pi}{s+2000\pi}$ and $\Delta T = \frac{1}{2000\pi}$. The valleys of $|H_f(s)|$ are located at odd multiples of ω_0 , as shown in Fig. 4(b). The values of $|H_f(s)|$ valleys are similar to these of (20), however for the case of digital implementation the amount of memory used to implement the delay in (23) is half of that needed for implementing (20).

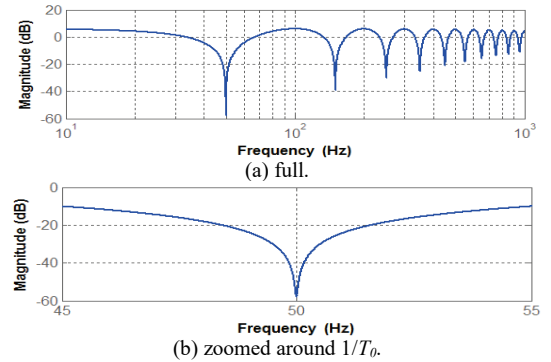


Fig. 4. Bode diagram of $|H_f(s)|$ in (23) for $T_0 = 20$ ms, $W(s) = \frac{2000\pi}{s+2000\pi}$ and $\Delta T = -\frac{1}{\omega_0} \text{tg}^{-1}\left(\frac{\omega_0}{2000\pi}\right)$.

TABLE I
VALUES OF ΔT FOR BUTTERWORTH FILTERS OF DIFFERENT ORDERS

Order	$G_f(s)$	ΔT
1	$\frac{\omega_F}{s + \omega_F}$	$-\frac{1}{\omega_0} \text{tg}^{-1}\left(\frac{\omega_0}{\omega_F}\right)$
2	$\frac{\omega_F^2}{s^2 + \sqrt{2}\omega_F \cdot s + \omega_F^2}$	$-\frac{1}{\omega_0} \text{tg}^{-1}\left(\frac{\sqrt{2}\omega_0\omega_F}{\omega_F^2 - \omega_0^2}\right)$
3	$\frac{\omega_F^3}{s^3 + 2\omega_F s^2 + 2\omega_F^2 s + \omega_F^3}$	$-\frac{1}{\omega_0} \text{tg}^{-1}\left(\frac{2\omega_F^2\omega_0 - \omega_0^3}{\omega_F^3 - 2\omega_0^2\omega_F}\right)$

It is interesting to explore the influence of increasing filter order on disturbance rejection loop gain. Table I summarizes Butterworth filter $G_f(s)$ of orders 1 – 3 and corresponding values of ΔT . Bode diagrams of $H_f(s)$ for $T_0 = 20$ ms and $\omega_F = 2000\pi$ rad/s are shown in Fig. 5(a) for the three filters in Table I along with zooms around the first (Fig. 5(b) and third (Fig. 5(c)) base frequency multiples.

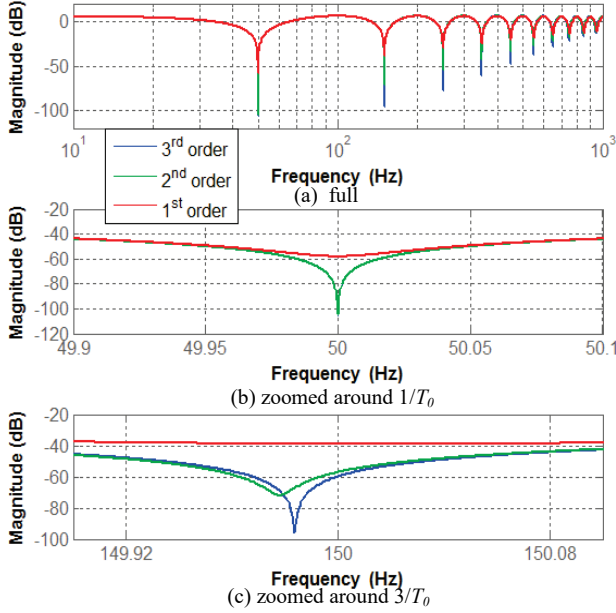


Fig. 5. Bode diagram of $|H_f(s)|$ in (23) for $T_0 = 20$ ms and different $W(s)$ and ΔT from Table I.

The following may be observed:

- Increasing the filter order above 1 greatly improves the disturbance rejection at relevant frequencies.
- The values of $|H_f(\omega_0)|$ are quite similar for UDE utilizing second and third order filters.
- Higher order filter utilization leads to better disturbance rejection at higher base frequency multiples.
- Location of resonant peaks is shifted for $n \geq 3$. This is due to the fact that the phase shift correction via ΔT is performed according to $n = 1$. Therefore, in case rejection of n^{th} harmonic is the most significant, ΔT should be calculated accordingly.

B. Tracking controller

If the system is properly nominalized by the disturbance rejection controller, then $u_d(t) \approx -d(t)$ and

$$\dot{y}(t) \approx -a_n y(t) + b_n u_i(t). \quad (21)$$

In order to make sure that $y(t)$ follows the reference (2), the desired response is formulated as

$$y(t) = (1 - e^{-\omega_r t}) y^*(t) = A(1 - e^{-\omega_r t}) \sin \omega_0 t, \quad (22)$$

with ω_r denoting the magnitude convergence rate. Hence,

$$T_y(s) = \frac{Y(s)}{Y^*(s)} = \frac{2\omega_r s + \omega_r^2}{(s + \omega_r)^2 + \omega_0^2} \quad (23)$$

is the desired complementary sensitivity function with $Y^*(s)$ symbolizing the Laplace transform of $y^*(t)$, indicating that transient response influences the envelope only without

affecting either frequency or phase. On the other hand, if the output of the tracking controller $C_i(s)$ is given by

$$u_i(t) = \mathcal{L}^{-1} \left\{ C_i(s) (Y^*(s) - Y(s)) \right\}, \quad (24)$$

then

$$T_y(s) = \frac{C_i(s) P_n(s)}{1 + C_i(s) P_n(s)} = \frac{L_t(s)}{1 + L_t(s)} \quad (25)$$

with $P_n(s)$ defined in (12) and $L_t(s)$ symbolizes tracking loop gain, derived from (23) as

$$L_t(s) = \frac{2\omega_r s + \omega_r^2}{s^2 + \omega_0^2}. \quad (26)$$

An interested reader is referred to [51] for detailed analysis of (26). Combining (23) with (25) taking into account (12) yields tracking controller transfer function,

$$C_i(s) = P_n^{-1}(s) L_t(s) = \frac{(s + a_n)(2\omega_r s + \omega_r^2)}{b_n (s^2 + \omega_0^2)}. \quad (27)$$

Note that the obtained controller is characterized by infinite gain at ω_0 as expected, yet is derived intuitively rather than following the generalized integrator theory. The overall control action $u(t)$ is then described by (7) with (11) and (24). Rearranging, it may be expressed in a two-degrees of freedom form as

$$u(t) = y^*(t) * L^{-1} \{ H_{FF}(s) \} - y(t) * L^{-1} \{ H_{FB}(s) \} \quad (28)$$

with

$$H_{FF}(s) = \frac{C_i(s)}{1 - G_f(s)}, \quad H_{FB}(s) = \frac{C_i(s) + G_f(s) P_n^{-1}(s)}{1 - G_f(s)}. \quad (29)$$

The total nominal loop gain of the system is then given by

$$L_{tot}(s) = P_n(s) H_{FB}(s) = \frac{L_t(s)}{1 - G_f(s)} + L_f(s). \quad (30)$$

For the boundary case of $G_f(s) = 0$ (no disturbance rejection loop), $L_{tot}(s) = L_t(s)$. On the other hand, in case $\omega_r = 0$ (no tracking loop), $L_{tot}(s) = L_f(s)$. Hence, for a given desired phase margin (or control bandwidth), trade-off between disturbance rejection (set by the bandwidth of $L_f(s)$) and tracking (set by the bandwidth of $L_t(s)$) is expected and must be taken into account when designing the controller.

III. APPLICATION TO IMPROVING THE VOLTAGE QUALITY OF INVERTERS

Consider a single-phase LC filter based inverter, powered from a dc source v_{DC} . The inverter feeds a nonlinear load, drawing current given in general form by

$$i_Q(t) = \sum_{\substack{n=1 \\ \text{odd}}}^{\infty} I_n \sin(n\omega_0 t + \varphi_n) \quad (31)$$

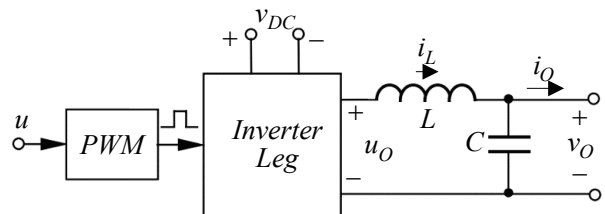


Fig. 6. A single-phase inverter.

The control signal u is converted into a PWM signal, driving the converter leg as shown in Fig. 6. The inverter leg output voltage, inductor current and capacitor voltage are denoted as v_o , i_L and v_o , respectively. The control goal is forcing the inverter output voltage

$$v_o(t) = \sum_{\substack{n=1 \\ \text{odd}}}^{\infty} V_n \sin(n\omega_0 t + \psi_n), \quad (32)$$

to track the reference given by

$$v_o^*(t) = V_M \sin \omega_0 t \quad (33)$$

by operating with unity displacement factor (achieved by the tracking controller) while minimizing the total harmonic distortion (ensured by disturbance observer), defined by

$$THD_V = V_1^{-1} \sqrt{\sum_{\substack{n=3 \\ \text{odd}}}^{\infty} V_n^2} = V_1^{-1} \sqrt{\sum_{\substack{n=3 \\ \text{odd}}}^{\infty} (I_n |Z_{On}|)^2}, \quad (34)$$

where $|Z_{On}| = |Z_O(jn\omega_0)| = |V_n/I_n|_{V_M=0}$ denotes the value of inverter output impedance magnitude at n -th multiple of base frequency. Obviously, it is desired to have $|Z_{On}| \rightarrow 0$ in order to achieve good disturbance rejection at relevant frequencies. In order to cope with the task, it is proposed to utilize a cascaded dual-loop control structure (similarly to [28]), utilizing a PI controller as an inner (inductor current) loop compensator (P controller was utilized in [28]) and a two-degrees-of-freedom controller, revealed in the preceding Section, as the outer (capacitor voltage) loop regulator. Table II summarizes the numerical values of system parameters, used in the simulations and experiments presented later.

TABLE II
NOMINAL SYSTEM PARAMETER VALUES

Parameter	Value	Units
Switching frequency, T_s^{-1}	15	<i>kHz</i>
Filter inductance, L	3.4	<i>mH</i>
Filter capacitance, C_n	30	μF
Base frequency, ω_0	100π	<i>rad/s</i>
DC link voltage, v_{DC}	195	<i>V</i>
Reference magnitude, V_M	$110\sqrt{2}$	<i>V</i>

A. Inner loop controller design and analysis

Inductor current dynamics are given by

$$L \frac{di_L(t)}{dt} = u(t - T_d) v_{DC}(t) - v_o(t) \quad (35)$$

with T_d denoting the overall sampling and switching delay. Defining an auxiliary control input $u'(t)$ so that

$$u(t) = \frac{1}{v_{DC}(t)} (u'(t) + v_o(t)), \quad (36)$$

while assuming that T_d^{-1} is much higher than bandwidth of v_{DC} , the current plant is linearized as

$$L \frac{di_L(t)}{dt} \approx u'(t - T_d) + \underbrace{v_o(t - T_d) - v_o(t)}_{\Delta v_o}. \quad (37)$$

In order to attenuate the remaining disturbance Δv_o , proportional-integrative controller

$$C_I(s) = K_{PI} \left(\frac{1 + \tau_I s}{s} \right) \quad (38)$$

is utilized, i.e. $u'(t) = \mathcal{L}^{-1} \left\{ C_I(s) (i_L^*(s) - i_L(s)) \right\}$. Current loop gain and complementary sensitivity function are then obtained as

$$LG_I(s) = \frac{K_{PI} (1 + \tau_I s)}{L s^2} e^{-T_d s} \quad (39)$$

and

$$T_I(s) = \frac{I_L(s)}{I_L^*(s)} = \frac{K_{PI} L^{-1} (1 + \tau_I s)}{s^2 e^{T_d s} + K_{PI} L^{-1} \tau_I s + K_{PI} L^{-1}}, \quad (40)$$

respectively, with $I_L^*(s)$ denoting inductor current reference signal, generated by the outer loop controller.

The design of $C_I(s)$ is then carried out following [59]. Adopting double-update PWM and sampling as close as possible to the PWM update instance, total transport and computation delay of $T_d = 45 \mu s$ may be achieved [28], leading to $K_{PI} = 7.94 \cdot 10^4$ and $\tau_I = 6.53 \cdot 10^{-4}$. This gives current loop bandwidth of 2450Hz with 45° phase margin and 7dB gain margin, as shown in Fig. 7. Complementary sensitivity function actually acts as voltage loop actuator and must be taken into account during outer loop compensator design.

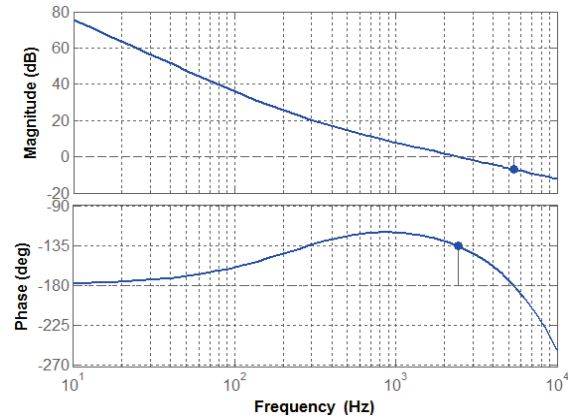


Fig. 7. Current loop gain Bode diagram.

B. Voltage controller design and analysis

Output voltage dynamics are given by

$$\frac{dv_o(t)}{dt} = \underbrace{(C_n^{-1} + \Delta C)}_C (i_L(t) - i_o(t)), \quad (41)$$

i.e. referring to (4), $a_n = 0$, $b_n = C_n^{-1}$, $y(t) = v_o(t)$, $u = i_L(t)$, $P_n(s) = (C_n s)^{-1}$ and $d(t) = C_n (C_i o(t) - \Delta C i_L(t))$. The two-degrees-of-freedom controller (cf. Fig. 8) design details are hence as follows.

B1. Tracking controller

The tracking controller should be designed so that the tracking loop gain crossover frequency is at least ten times higher than the resonant frequency [51], i.e.

$$|L_c(j10\omega_0)| = 1. \quad (42)$$

Substitution into (26) yields $\omega_c \approx 4.8\omega_0$. Combining (24), (27) and (42) yields the output of the tracking controller as [51]

$$u_r(t) = \mathcal{L}^{-1} \left\{ \underbrace{C_n \frac{9.6\omega_0 s^2 + 23\omega_0^2 s}{s^2 + \omega_0^2}}_{C_c(s)} (V_o^*(s) - V_o(s)) \right\}. \quad (43)$$

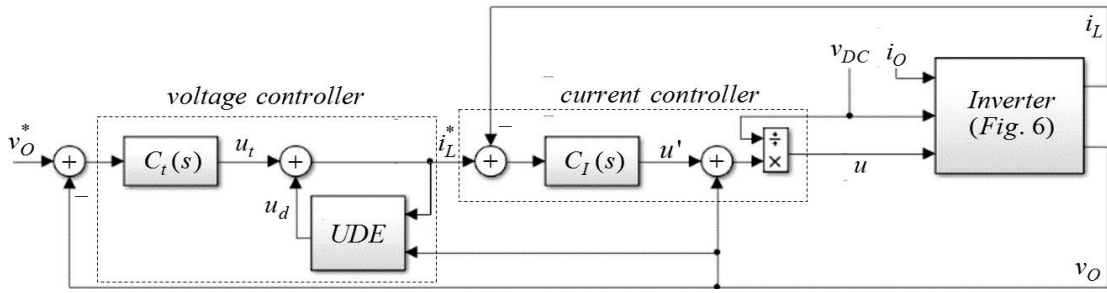


Fig. 8. Block diagram of the proposed control structure.

B2. Disturbance observer

According to (11), disturbance observer output is given by

$$u_d(t) = \mathcal{L}^{-1} \left\{ \frac{G_f(s)}{1-G_f(s)} (-C_n s V_o(s) + U_i(s)) \right\} \quad (44)$$

with $G_f(s)$ listed in Table I and $u_i(t)$ defined in (43). The current reference is then formed by the sum of (43) and (44) (cf. (8)) as

$$i_L^*(t) = \mathcal{L}^{-1} \left\{ -C_n \frac{s G_f(s)}{1-G_f(s)} V_o(s) + \frac{1}{1-G_f(s)} U_i(s) \right\}. \quad (45)$$

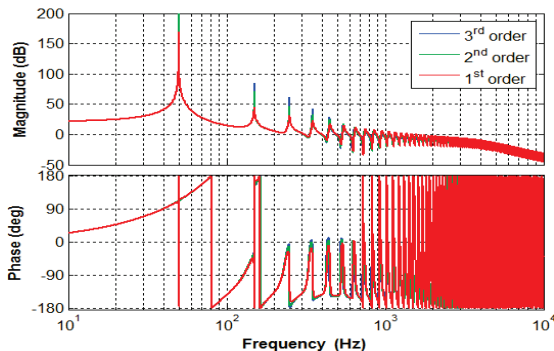
In order to determine the maximum attainable value of ω_F , required for disturbance rejection filter $G_f(s)$ selection, recall that i_L^* rather than i_L is set by the voltage controller. Therefore, current loop complementary sensitivity function $T_I(s)$ acts as the voltage loop actuator and must be properly taken into account by modifying the total nominal loop gain of the system as

$$L_{tot}(s) = T_I(s) \left(\frac{L_t(s)}{1-G_f(s)} + L_f(s) \right). \quad (46)$$

Corresponding inverter output impedance is derived as [28]

$$\begin{aligned} Z_o(s) &= \frac{1-G_f(s)}{sC(1+G_f(s)(T_I(s)-1)) + C_t(s)T_I(s)} \\ &= \frac{1}{\underbrace{sC + C_t(s)}_{Z_i(s)}} (1-G_f(s)) = Z_i(s)H_f(s), \end{aligned} \quad (47)$$

formed by two terms: $Z_i(s)$, related to the plant and tracking controller and $H_f(s)$, related to UDE filter.


 Fig. 9. Bode diagram of $L_{tot}(s)$ in (46) for the filters in Table I with cutoff frequencies in Table III.

Since significant parameter variations are not expected in the voltage plant, phase margin (PM) of 30° and gain margin (GM) of 5dB are chosen as minimum values for stability assurance. If larger margins are required the system may be redesigned at the expense of slight reduction of ω_t or ω_F . Resulting values of ω_F along with the resulting stability margins are summarized in Table III. Bode diagram of corresponding overall loop gain $L_{tot}(s)$ is given in Fig. 9. It is well-evident that rising the filter order increases the loop gain magnitude (i.e. improves the system disturbance rejection capability) at odd multiples of ω_0 . The output impedance $Z_o(s)$ and its forming terms (cf. (47)) are shown in Fig. 10 for the 3rd order filter. As expected, $H_f(s)$ possesses resistive behavior at odd multiples of ω_0 while $Z_o(s)$ is capacitive at ω_0 and slightly inductive at odd multiples of ω_0 due to influence of $Z_i(s)$.

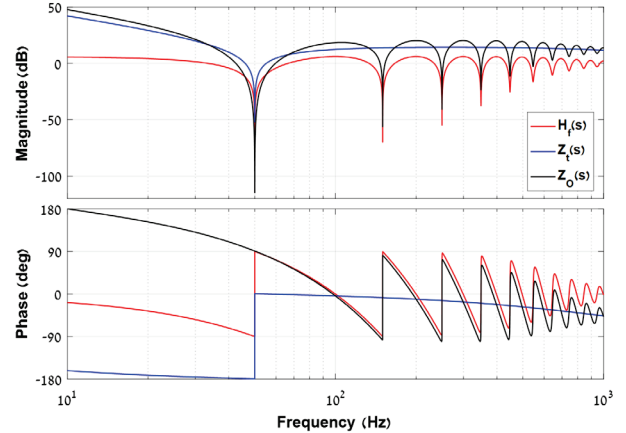

 Fig. 10. Bode diagram of $|Z_o(s)|$ in (47) for the filters in Table I with cutoff frequencies in Table III.

TABLE III
CUT-OFF FREQUENCIES AND STABILITY MARGINS FOR BUTTERWORTH FILTERS OF DIFFERENT ORDERS

Order	ω_F , rad/s	PM, °	GM, dB
1	$2\pi \cdot 690$	30	5
2	$2\pi \cdot 670$	30	10.4
3	$2\pi \cdot 640$	30	12.6

IV. VERIFICATION

In order to confirm the revealed control structure, modified Texas Instruments High Voltage Single Phase Inverter Development Kit (TIDK) was employed. Inverter parameters are similar to the values given in Table II. The control system was implemented digitally using a Concerto F28M35 control card. Experimental setup is shown in Fig. 11.

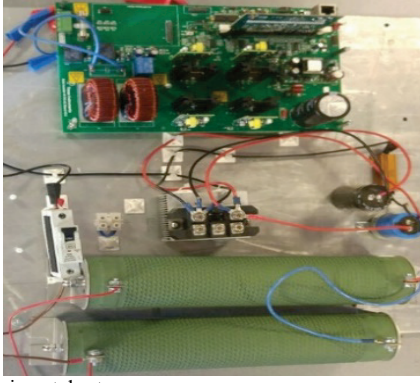


Fig. 11. Experimental setup.

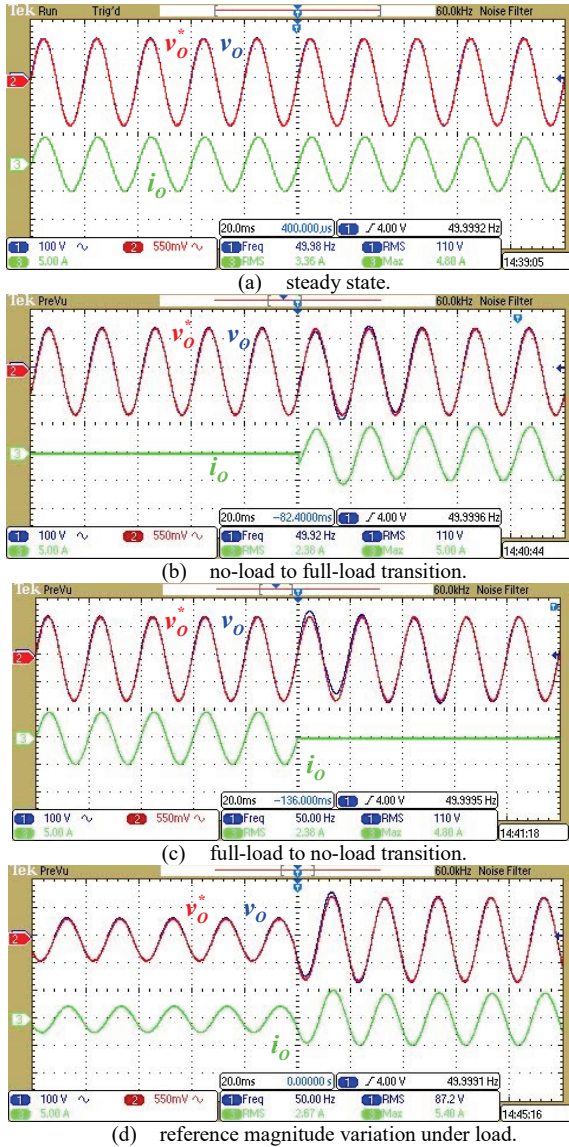


Fig. 12. Experimental results: Operation under linear load.

A. Operation with linear load

In order to examine the operation with linear load, the inverter was terminated by a 33Ω resistor. A third order Butterworth filter based UDE was employed. Fig. 12 presents the results of steady state operation (Fig. 12(a)) as well as full

load to no load (Fig. 12(b)) and no load to full load (Fig. 12(c)) transitions. In addition, Fig. 12(d) demonstrates the system response to reference magnitude variation from 50% to 100% of nominal value. It may be concluded that the system performs well in both steady state and transient regimes. Output voltage THD under linear load was found to be 0.87%.

B. Operation with nonlinear load

In order to inspect the operation under nonlinear load, the 33Ω resistor was replaced by a diode rectifier, driving a 50Ω , $940\mu\text{F}$ parallel RC load (250W) with a crest factor of 3.2~3.5, depending on the inverter internal impedance. For testing transients, the load resistor has been replaced with 100Ω resistor to limit the inrush current. Performance utilizing, first, second and third order Butterworth filter based UDEs were examined. Fig. 13 presents the time domain results of steady state operation while Fig. 14 compares respective experimental frequency domain distributions and total harmonic distortions of the output voltage for all three cases. As predicted, THD_v reduces with the increase of filter order, which mainly affects the 3rd and 5th harmonics.

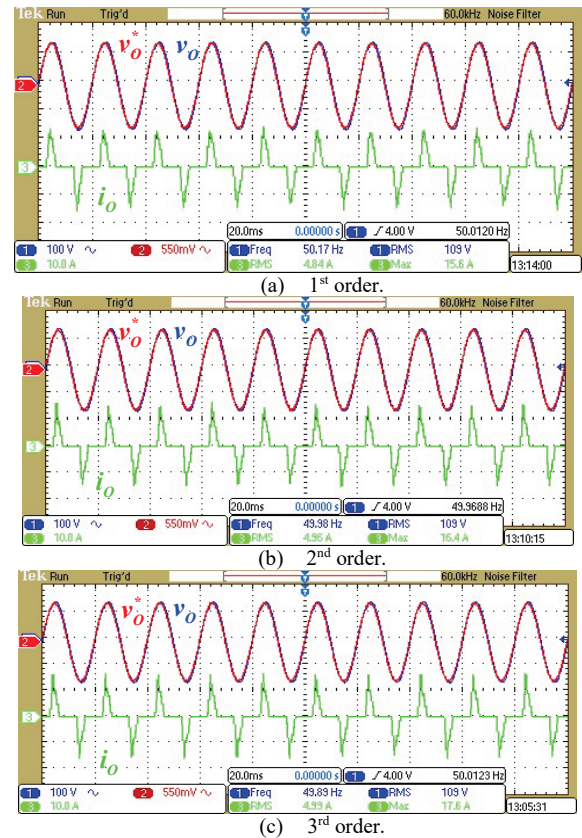

 Fig. 13. Experimental results: Steady-state operation under nonlinear load for different orders of $G(s)$.

Fig. 15 presents the full load to no load and no load to full load transitions for the third order Butterworth filter based UDE. The no load to full load transient is usually the worst one to expect. The settling time here is formed by a half-cycle-delay, used in the UDE, filter response time and load transient. According to the results, the performance may be

considered satisfactory when the impressive steady state performance is taken into account.

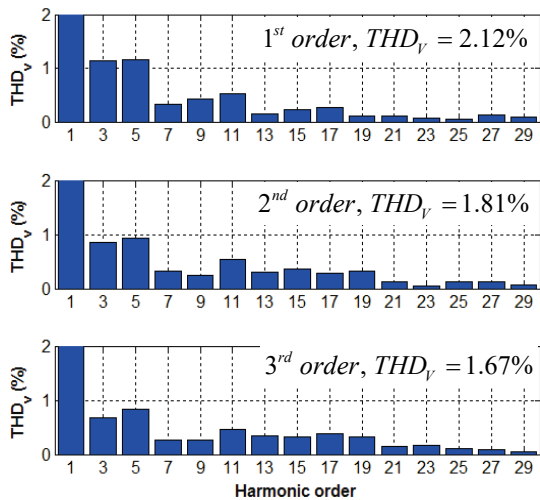


Fig. 14. Experimental results: Output voltage spectra comparison for different orders of $G_v(s)$.

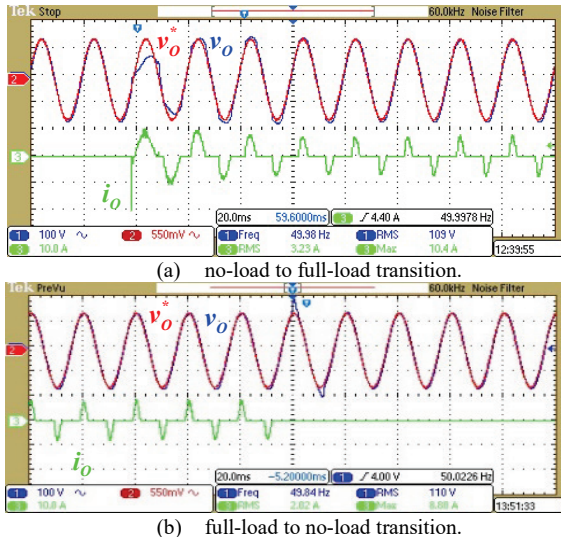


Fig. 15. Experimental results: Transient performance under nonlinear load for 3rd order Butterworth filter based UDE.

Steady-state system operation under nonlinear load system was also verified under fundamental frequency deviation up to ± 1 Hz to examine the robustness. Experimental results are shown in Fig. 16 with corresponding values of THD_v indicated. THD_v is noticeably affected by base frequency variations.

C. Comparison with multi-band-stop filter based UDE

As mentioned above, in a recent paper [28] a similar dual-loop control structure was proposed, utilizing a proportional controller as a current loop regulator and a different two-degree of freedom regulator as a voltage controller. A proportional nominal voltage loop tracking controller was employed, while a UDE equipped with a multi-band-stop filter was utilized for disturbance rejection. The hardware setup and other operational parameters (switching frequency and load) were similar to the ones in this paper.

Performance comparison results of control structure in [28] and the one proposed in the paper (utilizing a 3rd order Butterworth filter) is summarized in Fig. 17. Frequency domain distributions and total harmonic distortions of the output voltage are compared in Fig. 17(a) for nominal base frequency operation. It may be concluded that the control structure proposed in this paper outperforms the one in [28] in terms of THD_v . However, if the base frequency were to vary, the algorithm in [28] becomes superior to the one proposed here, as shown in Fig. 17(b). This is because the control structure in [28] was designed especially for ensuring robustness to base frequency variations. The algorithm proposed in this paper outperforms the one in [28] in terms of transient response speed as well, as shown in Fig. 17(c),

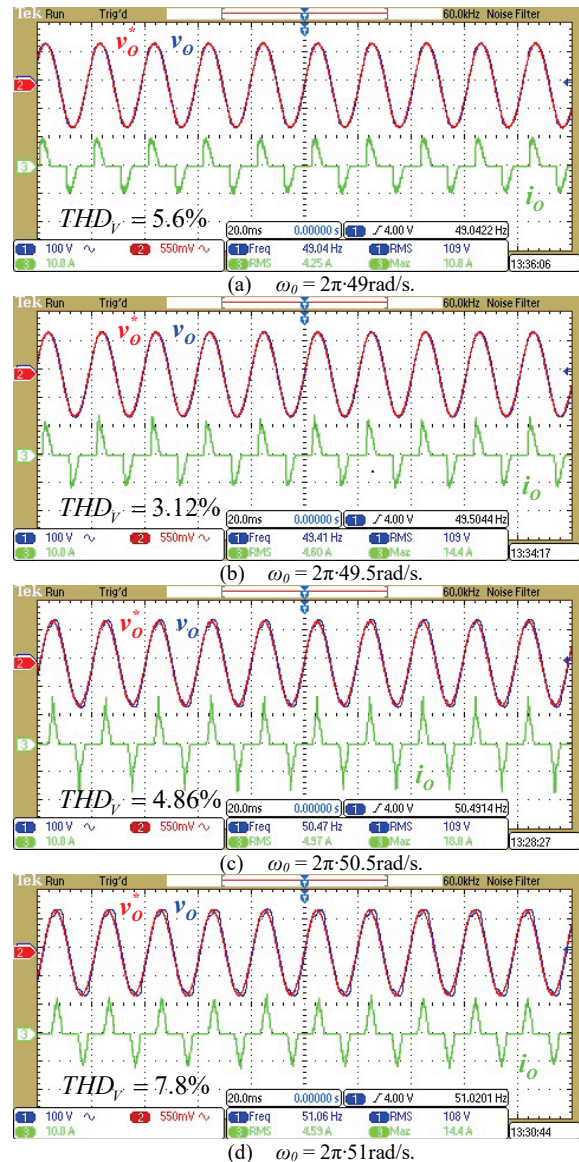


Fig. 15. Experimental results. Steady state operation under ± 1 Hz base frequency deviation.

which presents the output voltage tracking errors for no load to full load to no load transients.

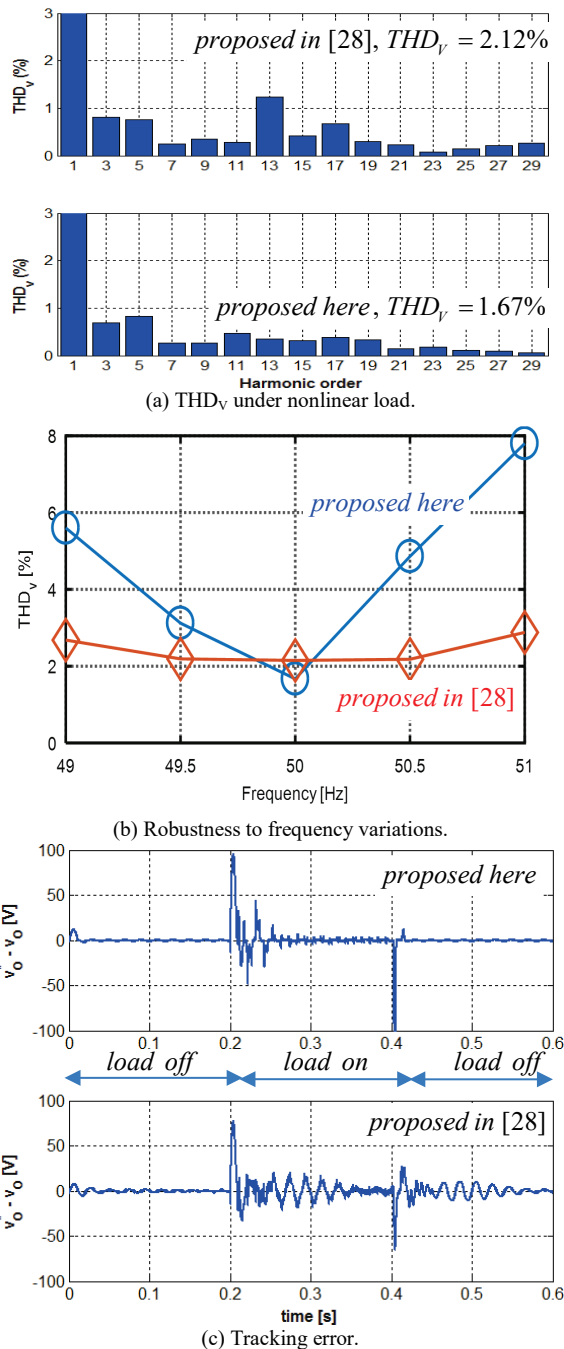


Fig. 16. Results of comparison with the method proposed in [28].

V. CONCLUSIONS

In this paper, a two-degrees-of-freedom control structure was proposed for enhancing the output voltage quality of inverters, allowing tracking and disturbance rejection problems to be decoupled. A modified Uncertainty and Disturbance Estimator, based on time-delay filter, was utilized to tackle the disturbance rejection task. Employing the proposed filter has led to minimization of inverter output impedance magnitude around the harmonics of interest, leading to enhanced disturbance rejection capabilities. Once the total uncertainty and disturbance was accurately estimated and eliminated by the proposed disturbance observer, it was possible to impose desired tracking performance by a suitable

resonant tracking controller, designed according to prescribed nominal transient behavior. Theoretical findings were fully supported by experimental results. Possibility to improve robustness to base frequency variations using multiple delay filters [55] - [57], [60] will be examined in future work.

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7. UDE-Based Controller Equipped with a Multiple-Time-Delayed Filter to Improve the Voltage Quality of Inverters

Publication number 4 –

Submitted to IEEE transaction on industrial electronics

Nomenclature

C	Output filter capacitance
C_n	Inverter nominal capacitance
$C_t(s)$	Tracking controller compensator transfer function
f	System disturbance input
$G_f(s)$	UDE filter
G_{fM}	Multiple-time delayed filter
$H_f(s)$	Disturbance rejection transfer function
H_{fM}	Multiple time delayed disturbance rejection function
i_d	Lumped disturbance current
i_L	Inductor current
i_L^*	Inductor current reference
i_{Ld}^*	Estimated lumped disturbance current
i_{Lt}^*	Voltage tracking controller output
i_o	Output current
K	Time-delay weights vector
K_{PI}	Inverter current control proportional gain
K_{PV}	Inverter voltage control proportional gain
L	Output filter inductance
L_n	Nominal system loop-gain
$P(s)$	System plant
$P_n(s)$	Nominal plant
$Q(s)$	Low-pass filter
R_{H1}	Frequency robustness factor
T_0	Phase delay time at base frequency
T_a	Actuator tracking transfer function

T_l	Inductor current tracking transfer function
u_c	System controlled input
u_{cd}	LUD estimator output
u_{ct}	Tracking controller output
u_d	Lumped Uncertainty and Disturbance (LUD)
v	Inverter control input
v_o	Output voltage
y	System output
y^*	System output reference
Z_o	Inverter output impedance
ω_0	Base frequency
ω_F	UDE filter bandwidth
ω_t	Magnitude convergence rate


List of amendments to the original published version

1. The original figures had been replaced from script format to PNG scans in order to improve their quality
2. The inverse Laplace transform notation has been changed from $L^{-1}\{\cdot\}$ to $\mathcal{L}^{-1}\{\cdot\}$

Statement of contribution for the author Shlomo Gadelovits

The author Shlomo Gadelovits proposed to add a chain of delays in order to create frequency robust UDE filter. He also proposed to force the delay chain derivatives to zero in order to improve frequency robustness based on past work done on hard drive motor controllers in a single degree of freedom. He also designed and obtained the results for all the experiments shown in the paper and wrote the main body of work.

Shlomo Y Gadelovits



Alon Kuperman



Qing-Chang Zhong



Visakan Kadirkamanathan



Dauren Insepov



UDE-Based Controller Equipped with a Multiple-Time-Delayed Filter to Improve the Voltage Quality of Inverters

Abstract—In this paper, a two-degrees-of-freedom control algorithm based on uncertainty and disturbance estimator (UDE), aimed to minimize the total harmonic distortion of inverter output voltage is proposed, possessing enhanced robustness to base frequency variations. A multiple-time-delay action is combined with a commonly utilized low-pass UDE filter to increase the range of output impedance magnitude minimization around odd multiples of base frequency and to reject harmonics of typical single-phase nonlinear loads. Marginal robustness improvement achieved by increasing the number of time delays is quantified analytically and revealed to be independent of delay order. The performance of the proposed control approach and its superiority over two recently proposed methods is successfully validated by experimental results.

Index Terms—Uncertainty and disturbance estimator, time-delayed filter, inverter, voltage quality, two degrees of freedom control.

I. INTRODUCTION

POWER inverters are a key element associated with DC-AC energy conversion applications [1]. Therefore, the research related to the field of inverters control is ongoing and extremely popular. Minimizing the total harmonic distortion (THD) of DC-AC power converters feeding nonlinear loads is one of the fundamental challenges [2] – [12]. The challenge of THD reduction is equivalent to inverter output impedance minimization and is therefore closely related to the algorithm utilized for output voltage control [13]. In fact, reducing the magnitude of inverter output impedance around frequencies associated with load energy improves the output voltage quality [14] – [16]. In case single-phase inverter feeds a nonlinear load, inverter output impedance magnitude at odd harmonic frequencies is relevant for THD minimization, while in case of three-phase conversion, $6n \pm 1$ harmonic components are of interest. In [17] – [20] and [20] – [23], multi-resonant and repetitive controllers were utilized, respectively, to minimize inverter output voltage THD. Unfortunately, typical multi-resonant and repetitive control methods possess single-degrees-of-freedom structure, thus imposing coupling between tracking and disturbance rejection. On the other hand, disturbance observer (DOB) based methods [24] – [26] employ two-degrees-of-freedom structures, allowing elimination of the above-mentioned coupling. DOB-based controllers estimate and cancel the lumped uncertainty and disturbance to "nominalize" the plant [27], letting the tracking controller to shape the tracking response of the nominal system.

Uncertainty and Disturbance Estimator (UDE), developed in [28] – [36] and verified to be capable of successfully coping with a variety of control tasks in [37] – [46], is a subset of

DOB. It was demonstrated in [47], that UDE-based controllers may impose disturbance rejection by direct shaping of output impedance via suitable filter design. There, UDE controller equipped with a multi-band-stop-filter (MBS) was utilized to tackle the challenge of inverter output voltage quality enhancement. In [48], UDE controller equipped with a time-delayed-filter (TD) was proposed to improve its ability to approximate and eliminate signals characterized by periodic behavior and applied in [49] to single-phase inverter output voltage quality enhancement. Performance comparison between systems based on the two filters above under similar operating conditions indicated the superiority of TD in terms of both output voltage THD and settling time and the supremacy of MBS in terms of robustness to base frequency variations. Therefore, this paper mainly aims to improve the performance of UDE based controller equipped with a time-delayed-filter in terms of robustness to base frequency variations by increasing the number of delays in the time-delayed-filter, i.e. utilizing a multiple-time-delayed filter (MTD) rather than single-time-delayed filter, employed in [48] and [49].

It must be emphasized that utilizing a TD-based UDE yielded results somewhat similar to repetitive-like action [50]. Yet, as indicated in [48], the proposed method possesses significant fundamental difference owing to the two-degrees-of-freedom structure. Nevertheless, due to revealed similarities, design rules and underlying constraints of odd-harmonic repetitive control [51] – [53] are very helpful in designing TD-based UDE. Methods to improve the robustness of TD-based UDE to base frequency variations by increasing the number of delays in the time-delayed-filter were proposed in [54] – [56], elaborated in [57] and applied to control of power converters (still utilizing single-degree-of-freedom structure) in [58] – [61]. Here, similar enhancement is adopted to equip the UDE with MTD while maintaining the two-degrees-of-freedom structure to improve the robustness to base frequency variations.

The rest of the paper is organized as follows. The proposed UDE-based controller is revealed in detail in Section II. Application to improving output voltage quality of inverters is described in Section III. Experimental verification of the proposed methodology is demonstrated in Section IV. The paper is concluded in Section V.

II. UDE-BASED CONTROLLER

Consider a stable, minimum-phase uncertain plant P with disturbance,

$$y(s) = P(s)u(s) = \underbrace{(P_n(s) + \Delta P(s))}_{P(s)} \underbrace{(u_c(s) + f(s))}_{u(s)}, \quad (1)$$

where y is the system output, P_n and ΔP are nominal and uncertain parts of P , respectively, u is the plant input, u_c is the

control input and $f(t)$ is the external disturbance, satisfying

$$f(t) = \sum_{n=1, \text{odd}}^{\infty} F_n \sin(n\omega_0 t + \phi_n). \quad (2)$$

Reference signal to be tracked by the system output $y(t)$ is given by

$$y^*(t) = R \sin \omega_0 t. \quad (3)$$

Rearranging (1) yields

$$y(s) = P_n(s)(u_c(s) + u_d(s)) \quad (4)$$

with

$$u_d(s) = f(s) + P_n^{-1}(s)\Delta P(s)u(s) \quad (5)$$

symbolizing the lumped uncertainty and disturbance (LUD), which may be expressed (cf. (1)-(4)) as

$$u_d(t) = \sum_{n=1, \text{odd}}^{\infty} D_n \sin(n\omega_0 t + \theta_n). \quad (6)$$

Tracking and disturbance rejection requirements are proposed to be met simultaneously by employing a two-degree-of-freedom control structure with a split control signal

$$u_c(t) = u_{ct}(t) - u_{cd}(t) \quad (7)$$

with $u_{ct}(t)$ and $u_{cd}(t)$ symbolizing the output of tracking controller and LUD estimator, respectively. In case the LUD estimator is properly designed, then $u_{cd}(t) \approx u_d(t)$ and (4) reduces to

$$y(s) = P_n(s)u_{ct}(s), \quad (8)$$

i.e. the plant is nominalized [27] and the tracking controller may be designed according to nominal desired behavior. It was shown in [62], [63] that tracking controller and LUD estimator designs may be decoupled under the restriction of available control bandwidth and desired stability margins.

A. LUD estimator equipped with multiple-time-delayed filter

According to (4), the LUD is given by

$$u_d(s) = P_n^{-1}(s)y(s) - u_c(s). \quad (9)$$

UDE-based controllers reconstruct the LUD in (6) by passing (9) through a linear filter $G_f(s)$, ideally characterized by unity gain and zero phase at odd multiples of ω_0 ,

$$u_{cd}(s) = u_d(s)G_f(s) = \left(P_n^{-1}(s)y(s) - \underbrace{(u_{ct}(s) - u_{cd}(s))}_{u_c(s)} \right) G_f(s). \quad (10)$$

Rearranging, the LUD estimate is given by

$$u_{cd}(s) = \frac{G_f(s)}{1 - G_f(s)} (P_n^{-1}(s)y(s) - u_{ct}(s)), \quad (11)$$

making use of system output, tracking control input and nominal plant model only. Moreover, substituting (10) into (4) gives

$$y(s) = P_n(s) \left(u_{ct}(s) + u_d(s) \underbrace{(1 - G_f(s))}_{H_f(s)} \right). \quad (12)$$

Apparently, if $G_f(s)$ possesses unity gain and zero phase at odd multiples of ω_0 , then corresponding $H_f(s) = 0$ and LUD in (6) will be fully attenuated.

Since the LUD in (6) contain odd harmonics only, then

$$u_d(t) = -u_d(t - \frac{T_0}{2}) \quad (13)$$

with $T_0 = \frac{2\pi}{\omega_0}$, or

$$u_d(s) = -u_d(s)e^{-\frac{T_0}{2}s}. \quad (14)$$

Unfortunately, (13) cannot be utilized as is due to infinite bandwidth. Therefore, (14) is combined with a low-pass filter $Q(s)$ to limit the signal bandwidth, yielding the LUD estimate given by

$$u_{cd}(s) = u_d(s) \left(\frac{-Q(s)e^{-\frac{T_0}{2}\Delta T}}{G_{f1}(s)} \right) \quad (15)$$

with ΔT denoting the delay of $Q(s)$ at ω_0 [48]. The resulting $G_{f1}(s)$ is referred to as time-delayed filter in [49]. Within the pass band of $Q(s)$,

$$H_{f1}(s) = 1 - G_{f1}(s) = 1 + e^{-\frac{T_0}{2}s} \quad (16)$$

with corresponding magnitude given by

$$|H_{f1}(j\omega)| = \left(2 + 2 \cos\left(\frac{T_0}{2}\omega\right) \right)^{\frac{1}{2}}. \quad (17)$$

Therefore,

$$|H_{f1}(jn\omega_0)| = \begin{cases} 0, & \text{odd } n \\ 2, & \text{even } n \end{cases} \quad (18)$$

and

$$|H_{f1}(j\omega)| \leq 1 \text{ for } n - \frac{1}{3} \leq \frac{\omega}{\omega_0} \leq n + \frac{1}{3}, n \text{ odd}. \quad (19)$$

Bode diagram of $|H_{f1}(j\omega)|$ versus normalized frequency ω/ω_0 is depicted in Fig. 1.

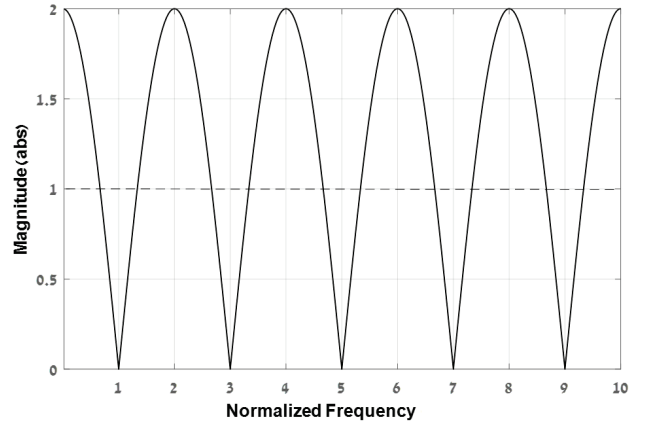


Fig. 1. Bode diagram of $|H_{f1}(s)|$.

In order to improve the LUD estimator robustness to frequency variations, note that (13) may be generalized as

$$u_d(t) = (-1)^m u_d(t - m\frac{T_0}{2}), m = 1, 2, 3... \quad (20)$$

or

$$u_d(s) = (-1)^m u_d(s)e^{-m\frac{T_0}{2}s}. \quad (21)$$

Furthermore, (21) can be rewritten as

$$u_d(s) = \sum_{m=1}^M k_m (-1)^m u_d(s) e^{-\frac{T_0}{2}s} \quad (22)$$

with

$$\sum_{m=1}^M k_m = 1. \quad (23)$$

Again, (22) cannot be utilized as is due to infinite bandwidth. Combining with a low-pass filter $Q(s)$ yields the LUD estimate given by

$$u_{cd}(s) = u_d(s) \left(\underbrace{Q(s) \sum_{m=1}^M k_m (-1)^m e^{-\left(\frac{T_0}{2} - \Delta T\right)s}}_{G_{fM}(s)} \right). \quad (24)$$

The resulting $G_{fM}(s)$ is thereafter referred to as multiple-time-delayed filter. Coefficients k_m are selected following [55], [56] to reduce the sensitivity of $G_{fM}(s)$ to frequency variations around odd multiples of ω_0 by forcing

$$\left. \frac{d^l G_{fM}(s)}{ds^l} \right|_{s=jn\omega_0, n \text{ odd}} = 0, l = 1, 2, \dots, M-1, \quad (25)$$

yielding the following system of $M-1$ equations,

$$\sum_{m=1}^M m^l k_m = 0, l = 1, 2, \dots, M-1. \quad (26)$$

Combining (26) with (23), the solution is given in a matrix form by

$$\mathbf{K} = \mathbf{A}^{-1} \mathbf{B}, \quad (27)$$

where $\mathbf{K} = (k_1, k_2, \dots, k_M)^T$ is a $M \times 1$ vector, $\mathbf{A} = \{a_{ij}\}$ is a $M \times M$ matrix with $a_{ij} = j^{i-1}$ and $\mathbf{B} = (1, 0, \dots, 0)^T$ is a $M \times 1$ vector. Values of k_m for $l = 2, 3, 4$ and 5 are summarized in Table I. Within the pass band of $Q(s)$ (i.e. for $Q(s) = 1$),

$$H_{fM}(s) = 1 - G_{fM}(s) = 1 - \sum_{m=1}^M k_m (-1)^m e^{-\frac{T_0}{2}s} \quad (28)$$

with corresponding magnitude given by

$$|H_f(j\omega)| = \left(2 + 2 \cos\left(\frac{T_0}{2}\omega\right) \right)^{\frac{1}{2}M}. \quad (29)$$

TABLE I
WEIGHTING COEFFICIENTS OF MULTIPLE-TIME-DELAYED FILTERS

M	k_1	k_2	k_3	k_4	k_5
1	1	--	--	--	--
2	2	-1	--	--	--
3	3	-3	1	--	--
4	4	-6	4	-1	--
5	5	-10	10	-5	1

Therefore,

$$|H_{fM}(jn\omega_0)| = \begin{cases} 0, & \text{odd } n \\ 2^M, & \text{even } n \end{cases} \quad (30)$$

and

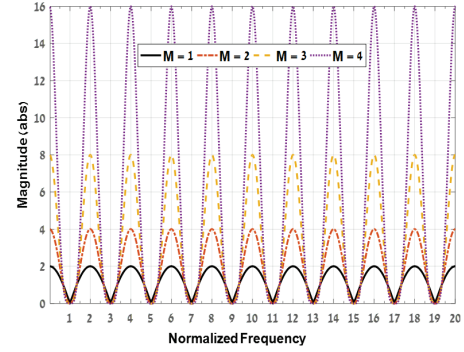
$$|H_{fM}(j\omega)| \leq 1 \text{ for } n - \frac{1}{3} \leq \frac{\omega}{\omega_0} \leq n + \frac{1}{3}, n \text{ odd}, \quad (31)$$

i.e. (31) is independent of M . Bode diagram of $|H_{fM}(j\omega)|$ versus normalized frequency ω/ω_0 is depicted in Fig. 2 for $M = 1, 2, 3, 4$. It may be concluded that increasing the number

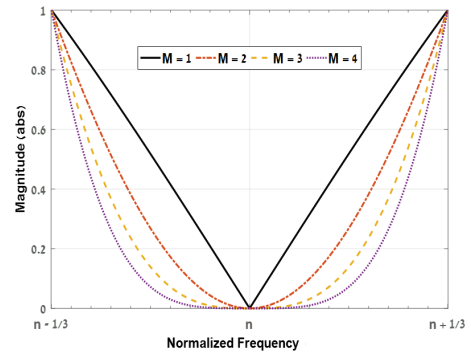
of delays from M to $M+1$ leads to robustness improvement of

$$R_{H1}(j\omega) = \frac{|H_{fM}(j\omega)|}{|H_{fM+1}(j\omega)|} = |H_{f1}(j\omega)|^{-1} = \left(2 + 2 \cos\left(\frac{T_0}{2}\omega\right) \right)^{\frac{1}{2}} \quad (32)$$

within frequency range given in (31) irrespectively of M , as shown in Fig. 3.



(a) full view



(b) zoomed around odd n

Fig. 2. Bode diagram of $|H_{fM}(s)|$ with $Q(s) = 1$ for different values of M .

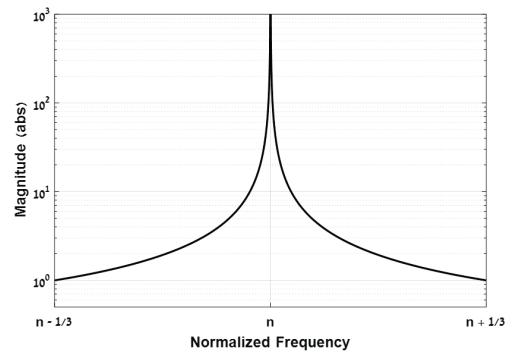


Fig. 3. Bode diagram of $|R_{H1}(s)|$ zoomed around odd n .

Application of a non-ideal low-pass filter $Q(s)$ with cut-off frequency ω_F influences $H_{fM}(s)$ as follows: for $\omega \ll \omega_F$, (29) – (32) remain valid while for $\omega \rightarrow \omega_F$ performance degradation takes place, as pointed out in [48]. Bode diagram of $|H_{fM}(j\omega)|$ combined with a $\omega_F = 20\omega_0$ first-order Butterworth filter versus normalized frequency is depicted in Fig. 4 for $M = 1, 2, 3, 4$ to demonstrate the effect of non-ideal $Q(s)$ application. Consequently, the bandwidth of $Q(s)$ should

be as high as possible to preserve idealized behavior given by (29) – (32) for as many harmonics as possible.

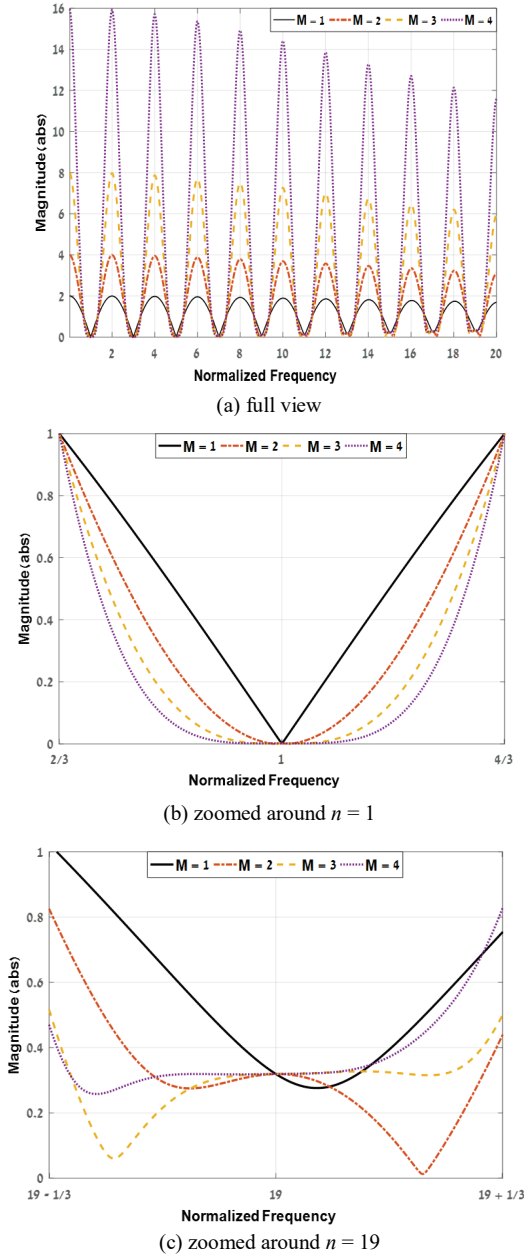


Fig. 4. Bode diagram of $|H_M(s)|$ with $Q(s) \neq 1$ for different values of M .

B. Tracking controller

Once (8) is valid, the plant is LUD-free and tracking controller $C_t(s)$ may be selected according to desired nominal tracking performance. In general, to assure zero steady-state tracking error, a proportional-resonant controller should be selected for a reference given by (3) [64]. Nevertheless, in case the nominal plant is a pure integrator (typical for power electronic converters under cascaded current-voltage control), proportional controller may be sufficient in case available control bandwidth is much higher (decade or more) than ω_0 . The output of tracking controller $C_t(s)$ is given by

$$u_{ct}(s) = C_t(s)(y^*(s) - y(s)). \quad (34)$$

C. Combined control action

Following (7), the control signal $u_c(t)$ is formed by the difference between (34) and (24) as

$$u_c(s) = C_t(s)(y^*(s) - y(s)) - \frac{G_{fM}(s)}{1 - G_{fM}(s)} \left(P_n^{-1}(s)y(s) - C_t(s)(y^*(s) - y(s)) \right). \quad (35)$$

Rearranging, there is

$$u_c(s) = \frac{C_t(s)}{1 - G_{fM}(s)} y^*(s) - \frac{C_t(s) + G_{fM}(s)P_n^{-1}(s)}{1 - G_{fM}(s)} y(s). \quad (36)$$

In case an actuator $T_a(s)$ is present, plant input and output are given by

$$u(s) = u_c(s)T_a(s) + u_d(s) \quad (37)$$

and

$$y(s) = \frac{P_n(s)C_t(s)}{1 + P_n(s)C_t(s)} y^*(s) + \frac{(1 - G_{fM}(s))P_n(s)}{(1 + P_n(s)C_t(s))T_a(s)} u_d(s), \quad (38)$$

respectively. Apparently, in case the energy content of $u_d(s)$ is concentrated at multiples of ω_0 , system output would follow the desired tracking behavior in steady state. Overall control block diagram is depicted in Fig. 5.

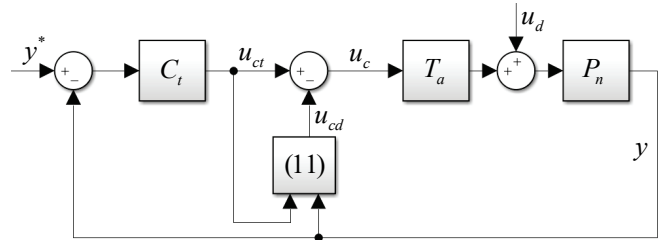


Fig. 5. Overall block diagram of the proposed control structure.

Nominal system loop gain is derived as

$$L_n(s) = \frac{P_n(s)C_t(s) + G_{fM}(s)}{1 - G_{fM}(s)} T_a(s) = \frac{2\omega_s s + \omega_i^2}{s^2 + \omega_0^2} + Q(s) \sum_{m=1}^M k_m (-1)^m e^{-\left(\frac{T_0}{2} - \Delta T\right)s} \quad (39)$$

$$= \frac{2\omega_s s + \omega_i^2}{s^2 + \omega_0^2} + Q(s) \sum_{m=1}^M k_m (-1)^m e^{-\left(\frac{T_0}{2} - \Delta T\right)s} T_a(s).$$

As recently shown in [62], [63], trade-off between tracking and disturbance rejection would always appear due to finite available control bandwidth and must be accordingly accounted upon selection of ω_i , M and $Q(s)$.

III. APPLICATION TO IMPROVING THE VOLTAGE QUALITY OF INVERTERS

A single-phase inverter with LC filter, fed from a dc source v_{DC} is shown in Fig. 6. Inverter leg voltage, inductor current and output voltage are denoted as u_o , i_L and v_o , respectively. PWM signal, modulated by the control input v drives the converter leg. Practical nonlinear loads, connected to inverter output terminals, draw currents $i_o(t)$ satisfying (2). On the other hand, output voltage reference is of the form (3). A cascaded dual-loop control structure is utilized (similarly to [47], [49]). Inductor current dynamics is given by

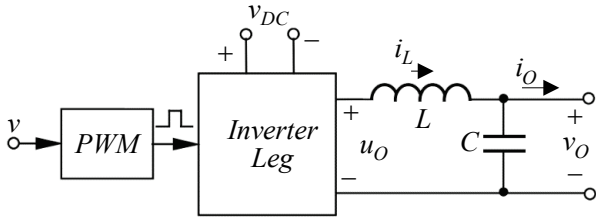


Fig. 6. Single-phase LC-filter based inverter.

$$\frac{di_L(t)}{dt} = L^{-1} (v(t - T_d)v_{DC}(t) - v_O(t)), \quad (40)$$

with T_d symbolizing the total sampling and switching delay. The control input is selected as

$$v(t) = \frac{1}{v_{DC}(t)} \left(K_{PI} (i_L^*(t) - i_L(t)) + v_O(t) \right), \quad (41)$$

where $i_L^*(t)$ is inductor current reference signal and K_{PI} is proportional gain. Complementary sensitivity function is then obtained as

$$T_I(s) = \frac{i_L(s)}{i_L^*(s)} = \frac{K_{PI} L^{-1}}{s e^{T_d s} + K_{PI} L^{-1}}. \quad (42)$$

Consider an inverter of Fig. 6 with numerical values of relevant parameters summarized in Table II. Setting K_{PI} to 59 yields a 2762 Hz bandwidth current loop with 45° phase margin and 6dB gain margin [47]. Bode diagram of the resulting current loop complementary sensitivity function $T_I(s)$ is given in Fig. 7.

 TABLE II
 NOMINAL SYSTEM PARAMETER VALUES

Parameter	Value	Units
Switching frequency, T_s^{-1}	15	<i>k</i> Hz
Filter inductance, L	3.4	<i>m</i> H
Filter capacitance, C_n	30	μ F
Base frequency, ω_0	100π	rad/s
DC link voltage, v_{DC}	195	V
Reference magnitude, V_1	$110\sqrt{2}$	V

Output voltage dynamics may then be expressed by

$$\frac{v_O(s)}{y(s)} = \frac{1}{C_n s} \left(\frac{i_L^*(s)}{u_c(s)} T_I(s) + \frac{i_d(s)}{u_d(s)} \right) \quad (43)$$

with $C = C_n + \Delta C$ and

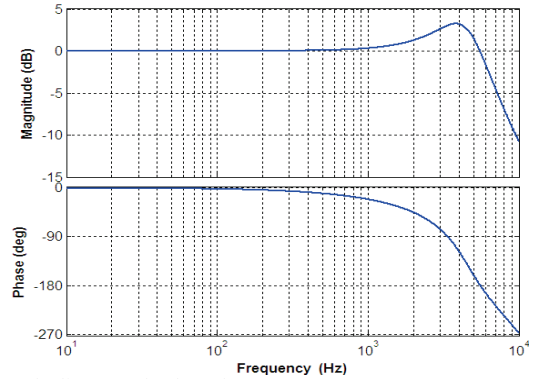
$$i_d(s) = -i_O(s) + C_n^{-1} \Delta C_n^{-1} (i_L^*(s) T_I(s) + i_O(s)). \quad (44)$$

From (2), (3) and (38), output voltage is given by

$$v_O(t) = \sum_{n=1, \text{ odd}}^{\infty} V_n \sin(n\omega_0 t + \psi_n), \quad (45)$$

i.e. in order to track the reference (3) with $R = V_1$, then ψ_1 and V_n (for $n > 1$) should be minimized. In other words, inverter output voltage should be in phase with the reference (tracking controller goal) and harmonic distortion free (disturbance observer goal). Total harmonic distortion of the output voltage is defined by

$$THD_V = \sqrt{\sum_{n=3, \text{ odd}}^{\infty} \left(\frac{V_n}{V_1} \right)^2} = V_1^{-1} \sqrt{\sum_{n=3, \text{ odd}}^{\infty} (I_{dn} |Z_O(jn\omega_0)|)^2}, \quad (46)$$


 Fig. 7. Bode diagram of voltage loop actuator $T_I(s)$.

where I_{dn} is the n -th harmonic magnitude of $i_d(t)$ (cf. (44)) and

$$Z_O(s) = \frac{H_{fM}(s) P_n(s)}{(1 + P_n(s) C_i(s)) T_a(s)} \quad (47)$$

is the inverter output impedance. Obviously, since $H_{fM}(s)$ is designed according to (28), then $|Z_O(jn\omega_0)| \rightarrow 0$, i.e. low (ideally zero) THD may be expected.

The control input in (43) is split as

$$\frac{i_L^*(s)}{u_c(s)} = \frac{i_{Ll}^*(s)}{u_{cl}(s)} - \frac{i_{Ld}^*(s)}{u_{cd}(s)}, \quad (48)$$

where the first term on the right-hand side denotes the tracking controller output given by

$$i_{Ll}^*(s) = K_{PV} (v_O^*(s) - v_O(s)) \quad (49)$$

with proportional gain K_{PV} and the second one symbolizes the disturbance observer output, given by

$$i_{Ld}^*(s) = \frac{G_{fM}(s)}{1 - G_{fM}(s)} (C_n s v_O(s) - u_{cl}(s)). \quad (50)$$

The filter $G_{fM}(s)$ was defined in (24) with $Q(s)$ selected as a third-order Butterworth filter (see the discussion on filter order selection in [49])

$$Q(s) = \frac{\omega_F^3}{s^3 + 2\omega_F s^2 + 2\omega_F^2 s + \omega_F^3}, \quad (51)$$

yielding

$$\Delta T = \frac{1}{\omega_0} \text{tg}^{-1} \left(\frac{2\omega_F^2 \omega_0 - \omega_0^3}{\omega_F^3 - 2\omega_0^2 \omega_F} \right). \quad (52)$$

Since the only voltage plant parameter is the capacitance C , whose value is not expected to undergo significant variations, phase margin (PM) of 30° and gain margin (GM) of 5dB are sufficient for stability assurance. If required, larger stability margins may be attained by trading off tracking bandwidth (i.e. K_{PV}) or ω_F .

It was shown in [49] that for $M = 1$, increasing the order of $Q(s)$ imposes ω_F reduction for given stability margin constraints. Here, the filter order remains unchanged and the number of delays M is increased from 1 to 3. For each number of delays, maximum ω_F is searched for until one of the stability margins limits is reached. The results are summarized in Table III and Bode diagrams of corresponding nominal loop gains $L_n(s)$ (cf. (40)) for $M = 1, 3$ and $K_{PV} = 0.236$ (i.e. tracking loop bandwidth of 2500π rad/s) are presented in Fig. 8. As expected, rising the number of delays increases the loop gain robustness) around odd multiples of

ω_0 while trading off the peak gain at these frequencies due to decreased ω_F [47], [65]. In practice, slight peak gain reduction has a negligible influence on performance since the output impedance at relevant harmonics is below the system noise level.

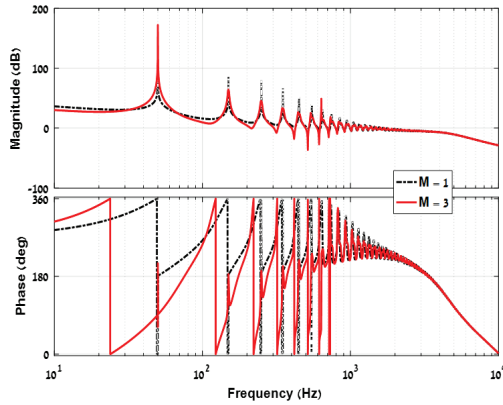


Fig. 8. Bode diagrams of $L_n(s)$ for $M = 1, 3$.

TABLE III
FILTER BANDWIDTHS AND STABILITY MARGINS FOR DIFFERENT NUMBER OF DELAYS

M	ω_F , rad/s	PM , °	GM , dB
1	$2\pi \cdot 840$	38	5
2	$2\pi \cdot 640$	30	5.3
3	$2\pi \cdot 590$	30	5.3

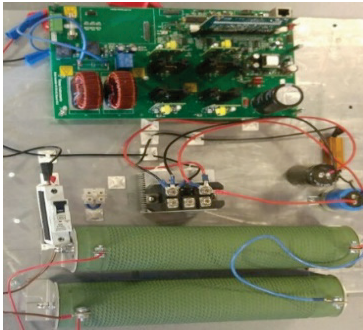


Fig. 9. Experimental setup.

IV. VERIFICATION

In order to verify the feasibility of the proposed UDE-based filter equipped with a multiple-time-delayed filter, modified Texas Instruments High Voltage Single Phase Inverter Development Kit (TIDK) with parameters in Table I was utilized. The proposed control structure with $M = 3$ and $\omega_F = 2\pi \cdot 590$ rad/s (cf. Table III) was executed in digital form by a Concerto F28M35 control board. Experimental setup is depicted in Fig. 9.

A. Operation with linear load

In order to verify the performance under linear load, a 33 Ω resistor was connected across inverter output terminals. Fig. 10(a) presents the steady state operation waveforms, Fig. 10(b) and 10(c) demonstrate full load – to – no load and no load – to – full load transitions, respectively, and Fig. 10(d)

shows the response to 50% – to – 100% reference magnitude step change.

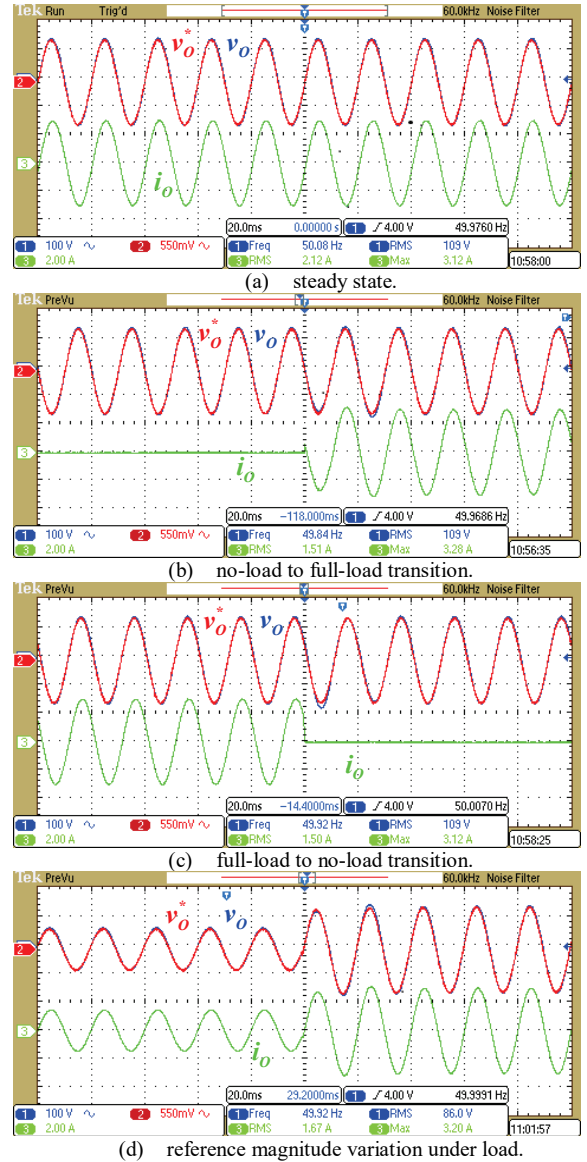


Fig. 10. Experimental results: Operation with linear load.

Apparently, satisfactory performance is evident in both steady state and transients. Under linear load, the system achieved output voltage THD of 0.88% in steady state operation.

B. Operation with nonlinear load

In order to verify the steady-state performance under nonlinear load, the 33 Ω resistor was removed and swapped with a full-bridge diode rectifier, terminated by a 50 Ω (250W)/940 μ F parallel RC load with a crest factor of ~ 3.35 . Fig. 11(a) presents respective reference and output waveforms. For transient performance testing, the 50 Ω resistor was replaced with a 100 Ω one to limit the inrush current. Fig. 11(b) and 11(c) demonstrate full load – to – no load and no load – to – full load transitions, respectively.

Under nonlinear load, the system achieved output voltage THD of 1.78% in steady state operation.

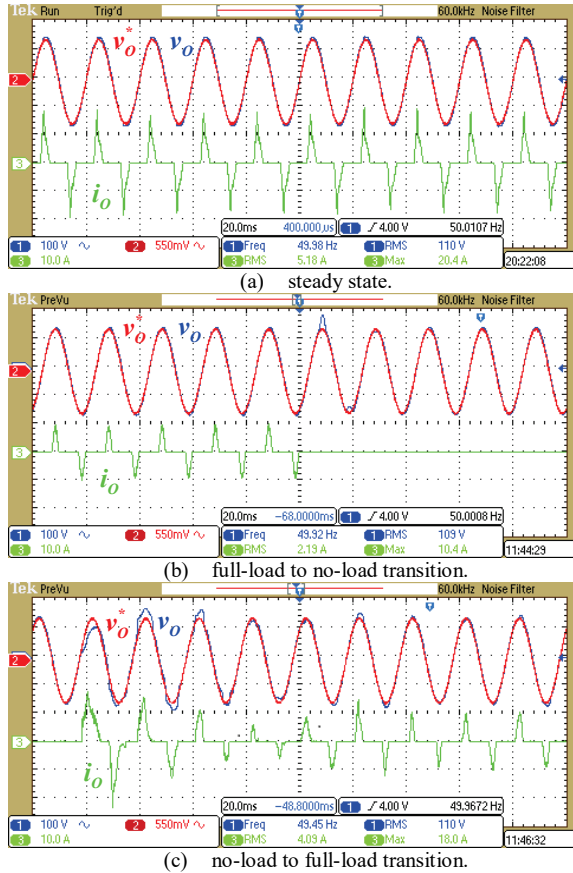


Fig. 11. Experimental results: Steady-state operation with nonlinear load.

C. Robustness to base frequency variations

In order to verify the robustness to base frequency variations, steady-state system operation under nonlinear load was examined for fundamental frequency deviations of ± 2 Hz. Experimental results are shown in Fig. 12 for the range of ± 1 Hz (which are likely to occur) and corresponding THD_V values are presented in Fig. 13 for fundamental frequency deviations of ± 2 Hz. It may be concluded that the system is indeed robust to frequency deviations of ± 1 Hz. Nevertheless, the THD_V attains its minimum below 50Hz and is asymmetrical. This is well expected from both the fact that ΔT in (24) accounts for the first harmonic only while the valleys of $|H_f(s)|$ at higher multiples of ω_0 are slightly displaced. Moreover, it is expected from Fig. 4(b) that for $M=3$, higher load harmonics would be better rejected around harmonic multiples than at their exact position. In order to verify this observation, the filter (24) was re-designed assuming base frequency of 50.25 Hz rather than 50Hz.

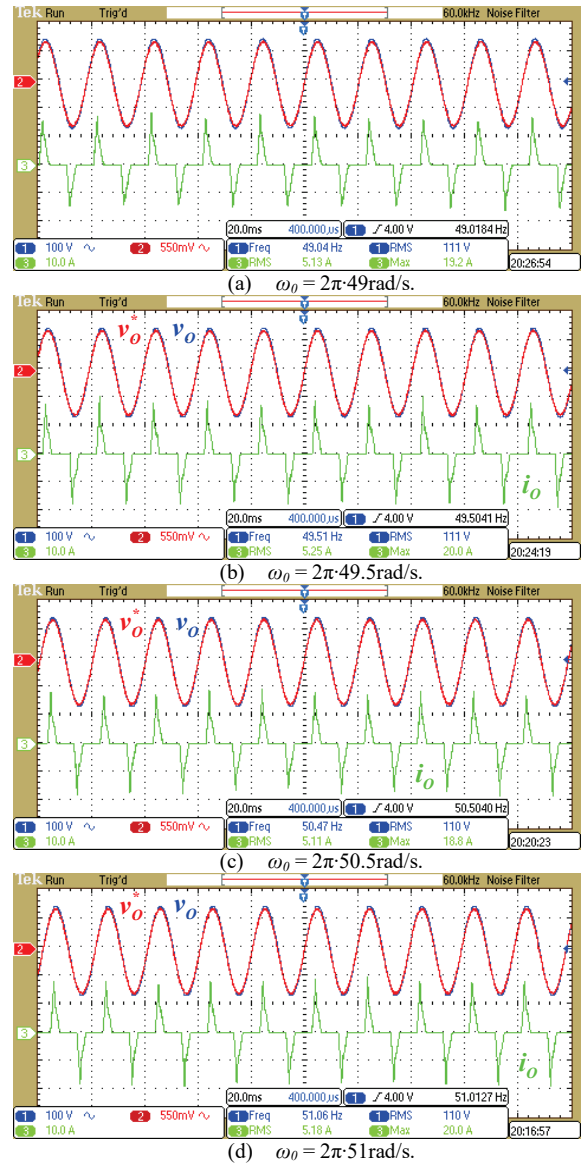


Fig. 12. Experimental results. Steady state operation with nonlinear load under ± 1 Hz base frequency deviation.

Corresponding THD_V values are presented in Fig. 13 for fundamental frequency deviations of ± 2 Hz. As the result of re-design, the THD_V curve was shifted to the right with corresponding value at 50Hz reduced from 1.78% to 1.67% and became more symmetrical.

D. Comparison with multi-band-stop and single-time-delayed filters based UDE

As mentioned above, in [47] and [49] similar dual-loop control structures were proposed, utilizing different two-

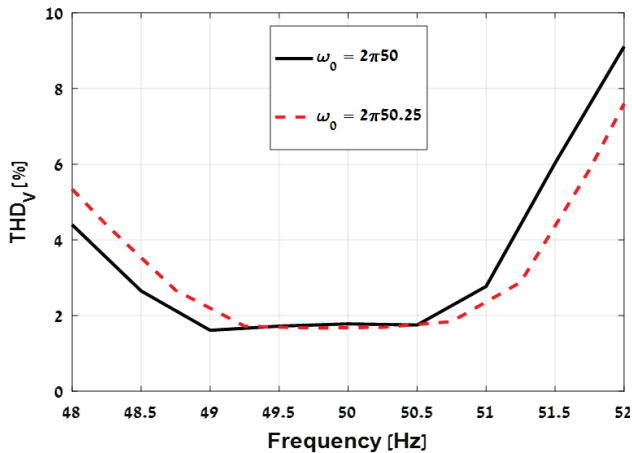


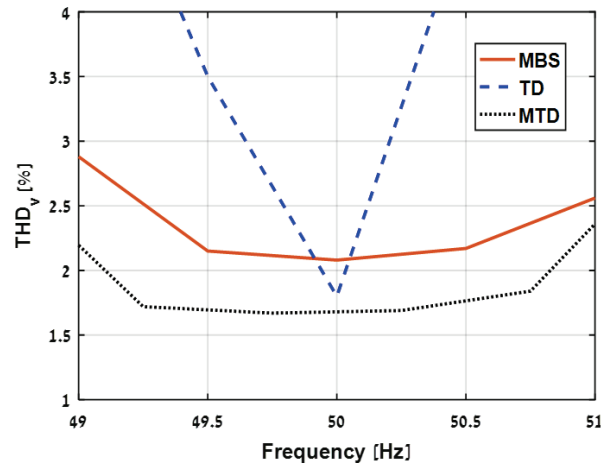
Fig. 13. Experimental results. Robustness to ± 2 Hz base frequency deviations.

degree-of-freedom regulator as voltage controller. In [47], a UDE equipped with a multi-band-stop filter was utilized for disturbance rejection while in [49] a UDE equipped with a single-time-delayed filter was employed. The hardware setup and other operational parameters (switching frequency and load) were similar to the ones in this paper.

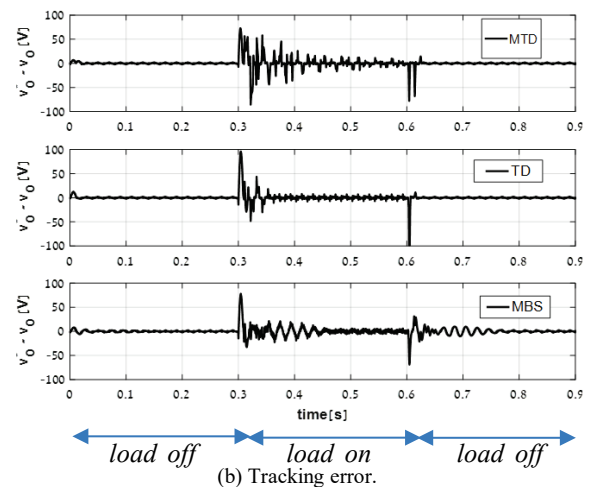
Outcomes of performance comparison of control structures in [47] (denoted as MBS), [49] (denoted as TD) and the one proposed here (denoted as MTD) are summarized in Fig. 14. Apparently, MTD is superior both in case the base frequency remains nominal and in case ω_0 is expected to vary, as shown in Fig. 14(a). Fig. 14(b) demonstrates tracking errors of output voltage for no load - to - full load - to - no load transients. In terms of transient response speed, MTD outperforms MBS while being inferior to TD, as expected due to increase amount of delay utilized.

V. CONCLUSIONS

In this paper, a two-degrees-of-freedom control structure based on UDE controller equipped with a multiple-time-delayed filter was suggested, aimed to improve the output voltage quality of DC-AC converters by minimizing the inverter output impedance magnitude around odd harmonics of base frequency. Compared to previously proposed UDE controllers equipped with multiple-band-stop and single-time-delay filters, the proposed control structure has yielded lower THD_v for both nominal and varied based frequency. On the other hand, due to the adoption of multiple time delays, the transient response is slightly prolonged compared to the single-time-delayed filter yet still better than that of multiple-band-stop-filter.



(a) Robustness to frequency variations.



(b) Tracking error.

Fig. 14. Results of comparison with methods proposed in [47] and [49].

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8. Conclusions and future work

8.1 Conclusions

Power quality has a key role in maximizing both the efficiency and the capacity of AC power sources. The transformation of the grid from generator based sources to inverter-based sources enhances the need for better voltage regulation.

In this thesis, two degrees of freedom design was applied to the control of power inverters. As shown throughout, the main challenge in controlling a power inverter is to reject the periodical disturbances, whilst ensuring that the controller bandwidth is limited. The method chosen for this work is based on a sub class of the disturbance observer called the Uncertainty and Disturbance Estimator (UDE). The key reason for using this method is that it had been found that the two degrees of freedom structure enables the option to (i) design a voltage source where the controller reference model together with the reference signal determines the internal voltage source and (ii) the design of the UDE filter determines the inverter closed loop output impedance. A number of increasingly sophisticated methods resulted from this approach.

The third chapter of the thesis based over (Gadelovits *et al.*, 2015; Gadelovits, Zhong and Kadiramanathan, 2016) uses a simple parallel operation scheme to demonstrate that the inverter output impedance is determined by the UDE design. It was shown that when connecting two inverters in parallel and giving them the same voltage reference, the current is shared in relation to the UDE filter bandwidth. This fact demonstrated that the power inverter closed loop output impedance is related mainly to the UDE filter design. Moreover, chapter three shows implementation of a UDE in closed loop and compared the maximum improvement achievable using the UDE equipped with a first-order low-pass filter operating near the stability limit. The UDE output THD was compared to an open loop and a feed-forward scheme where the inductor current is fed-forward to create a small virtual output impedance. This small virtual impedance had been created to dampen the filter resonance oscillation. The results showed a THD improvement related to the decrease in the output impedance and emphasized the need for an improved AC design.

The rest of the thesis dealt with the design of the UDE filter including the bandwidth constraint. In chapter 2 it was discussed that the inverter switching bridge combined with the current regulator acted as a limited bandwidth actuator for the voltage

regulator. Therefore, the classic low pass filter based design of the UDE proposed in chapter 3 did not give optimal results within the stability limits imposed by the actuator.

Four different design solutions through two different routes had been proposed in this thesis for dealing with the bandwidth constraint while maintaining the two-degrees of freedom design nature of the UDE based controller.

The problem description and the first solution had been presented in chapter four (Gadelovits *et al.*, 2017a). The solution aimed to shape the output impedance and to derive the UDE filter directly from it. The synthesized filter derived from the desired impedance was shaped as cascaded Butterworth filters, which formed the frequency selective filter. Simulation results for this method showed that a low magnitude error between the reference model output to the system output when compared to the traditional low pass filter design.

The second solution proposed in this thesis and presented in chapter five (Gadelovits *et al.*, 2017b) is to shape the output impedance using a set of elliptic filters. This method has shown good robustness to variations in the base frequency of the inverter voltage reference. This feature can be crucial in grid-tied or parallel operating inverters equipped with droop controllers. It is also demonstrated in the chapter that the low pass UDE filter design possess a trade-off between disturbance rejection at low frequency to the disturbance at the harmonics region.

The third solution (Gadelovits *et al.*, 2018) proposed in chapter six was aimed at simplifying the first two controllers' cumbersome structure. Here, it was shown that the controller two degrees of freedom structure, permitted a combination of resonant tracking controller and a time-delayed design of the UDE filter to be used. This solution achieved both good tracking performance and minimized the inverter output impedance at the point of interest. It also demonstrated that a good transient performance can be achieved by using a half-cycle delay instead of a full cycle delay in the case when the periodical disturbance is expected to have an odd symmetry.

The fourth solution proposed aimed at expanding the solution of (Gadelovits *et al.*, 2018) to deal with uncertain period times, and was presented in chapter seven. It was shown that by using a chain of three delay a frequency robust controller is achieved using a simple structure made of a single low pass filter and three period delays. The proposed UDE filter design also gave lower voltage THDs compared to the filter proposed in chapter four and five and smoother transients when compared to the filter proposed in chapter four. A comparison of the performance of the proposed algorithms was also made.

8.2 Future work

Two main directions for future work been identified as a direct offshoot of this thesis contributions. The first is a further enhancement of the proposed UDE filter design described in this thesis as a part of the extended state observer. The second is a direct application of the inverter control methods developed in the thesis for the design of an active power filter without a load current sensor. From the application point of view, since the two degrees of freedom design is separately determining the internal electromotive force and the output impedance of the inverter, it is possible to design an inverter with high impedance at the fundamental frequency and very low impedance at the harmonics region. This fact opens the possibility to design an active power filter without measuring the inverter output current. A brief overview of each direction of the ideas is explained below.

8.2.2 Frequency domain design of extended state observer

Similar to the design of the frequency selective filter for UDE. A filter based design can be developed for the Extended State Observer (ESO) structure. The ESO has additional design benefits over the UDE. (i) The ESO can observe both unmeasured states and disturbances and therefore not all the states have to be measured or be known. (ii) Unlike in the UDE case, the inverter can be modelled as a second-order system with a single control loop and (iii) in some cases the observer can generate a separate input for each observed harmonic which can be used for monitoring. However, the ESO may be more sensitive to model uncertainties and the design of the ESO for estimating periodical disturbances may be less intuitive. This is mainly because the design of the ESO is done in the time domain. In the case of an inverter, the observed disturbance can be fed back into the controller to reduce the inverter output impedance. The proposed design procedure is explained in the following.

Consider an inverter connected to a non-linear load similar to the one shown in chapter 2 Fig 2.9. The canonical state space model of the inverter is

$$\begin{aligned}\dot{x}(t) &= A_n x(t) + B_n u(t) + B_d d(t) \\ y(t) &= C_n x(t)\end{aligned}\tag{9.1}$$

where,

$$A_n = \begin{bmatrix} 0 & 1 \\ -\frac{1}{LC} & -\frac{R}{L} \end{bmatrix}, B_n = \begin{bmatrix} 0 \\ \frac{1}{LC} \end{bmatrix}, B_d = \begin{bmatrix} 0 \\ -\frac{1}{C} \end{bmatrix}, C_n = [1 \quad 0], \tag{9.2}$$

and

$$x(t) = [v_o(t) \quad \dot{v}_o(t)]^T, d(t) \approx \frac{R}{L} i_o(t) + \dot{i}_o(t), \quad (9.3)$$

L is the output filter inductance C is the output capacitance and u_o is the inverter bridge average voltage. The DC bus voltage is assumed to be constant. As shown in (8.3) the model states of the inverter in the canonical form are the output voltage and its derivative and not the output voltage and inductor current which are usually measurable. The derivative can be measured from the output capacitor current. However, the capacitor current carries high frequencies and high noise levels and the derivation of the capacitor current depends on a precise knowledge of the capacitor size.

As discussed in chapter 2 section 2.8.3 the disturbance input for the ESO is generated by an exogenous system of the form

$$\begin{aligned} \dot{w}(t) &= Ww(t) \\ d(t) &= Vw(t) \end{aligned} \quad (9.4)$$

The output current of an inverter is a periodical disturbance and therefore it can be written as a Fourier series of the form

$$i(t) = \sum_{k=1}^n (I_p \sin(n\omega_0 t) + I_q \cos(n\omega_0 t)). \quad (9.5)$$

It is worth to note that the disturbance input the inverter canonical model given in (8.1)-(8.3) contains both the output current and its derivative despite that $d(t)$ has the same periodical structure as (8.5) and hence $d(t)$ can be written as

$$d(t) = \sum_{k=1}^n P_k \sin(n\omega_0 t) + Q_k \cos(n\omega_0 t), \quad (9.6)$$

where P_k and Q_k are the Fourier coefficients of the disturbance. From (8.6) it is clear that each harmonic can be represented as the solution of the following ordinary differential equation

$$\frac{d^2 w_k}{dt^2} + (n\omega_0)^2 w_k = 0 \quad (9.7)$$

where k is the harmonic order. It is worth noting here that in some cases in the literature the first derivative of the disturbance is assumed to be zero. In the case of inverters, this assumption is true only if the switching and sampling frequencies are significantly higher than the disturbance observer bandwidth. High power rated inverters are limited in their switching frequency due to switching losses. Therefore in many cases, this assumption is not correct. From (8.7) the disturbance state matrix for each harmonic is

$$W_n = \begin{bmatrix} 0 & 1 \\ -(n\omega_0)^2 & 0 \end{bmatrix}. \quad (9.8)$$

The full disturbance state matrix is then derived by augmenting a few harmonics together in the form

$$W = \begin{bmatrix} W_1 & 0 & 0 \\ 0 & \ddots & 0 \\ 0 & 0 & W_n \end{bmatrix}, w = [w_1 \quad \dot{w}_1 \quad \cdots \quad w_n \quad \dot{w}_n]^T \quad (9.9)$$

To comply with (8.7) the output matrix is

$$V = [1 \quad 0 \quad \cdots \quad 1 \quad 0], V \in R^{2n}, \quad (9.10)$$

and the augmented system is

$$\begin{aligned} \dot{z}(t) &= Az(t) + Bu(t) \\ y(t) &= Cz(t) \end{aligned}, \quad (9.11)$$

where,

$$z(t) = [x(t) \quad w(t)]^T, A_T = \begin{bmatrix} A_n & B_d V \\ 0 & W \end{bmatrix}, B = [B_n^T \quad 0]^T, C = [C_0 \quad 0]. \quad (9.12)$$

The extended state observer design is

$$\begin{aligned} \dot{\hat{z}}(t) &= A_T \hat{z}(t) + B_T u(t) + K_L (\hat{y}(t) - y(t)) \\ \hat{y}(t) &= C_T \hat{z}(t) \end{aligned} \quad (9.13)$$

where K_L is the observer gain vector $[K_{Lx} \quad K_{Lw}]$. The ESO estimation error is defined as

$$e_z(t) = z(t) - \hat{z}(t) \quad (9.14)$$

and similarly to the classic Luenberger observer the estimation error dynamics is

$$\dot{e}_z(t) = (A - K_L C) e_z(t). \quad (9.15)$$

The estimated disturbance is calculated from the state estimator state vector as

$$\hat{d}(t) = [0 \quad V] \hat{z}(t). \quad (9.16)$$

A further enhancement of this proposed direction can be achieved by using a multi-band pass design. In this design, the dynamical disturbance model is directly derived from the design of a high order bandpass filter. This solution may increase the observer robustness to uncertainty in the fundamental frequency of the periodical disturbance. The filter can be designed in accordance with the recommendations found in (S. Y. Gadelovits *et al.*, 2017), where the filter was made of a chain of elliptic filters. The proposed disturbance dynamical model is derived from the high order filter as follow.

Consider a generic stable high order filter of the form

$$G(s) = \frac{b_{n-1}s^{n-1} + b_{n-2}s^{n-2} + \cdots + b_0}{s^n + a_{n-1}s^{n-1} + \cdots + a_0}, \quad (9.17)$$

where the filter pass band is designed to match the expected disturbance spectrum. The corresponding exogenous disturbance model is derived using a canonical state space representation as,

$$W = \begin{bmatrix} 0 & 1 & 0 & \cdots & 0 \\ 0 & 0 & 1 & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \cdots & 1 \\ -a_0 & -a_1 & -a_2 & \cdots & -a_{n-1} \end{bmatrix}, w = [w_1 \quad w_2 \quad \cdots \quad w_{n-1}]^T, V = [b_0 \quad b_1 \quad \cdots \quad b_{n-1}] \quad (9.18)$$

where,

$$w_k = \frac{d^{(k-1)}w}{dt^{(k-1)}} \quad (9.19)$$

By augmenting the derived disturbance exogenous system into the extended state observer as in (8.12), an accurate estimation of the periodical disturbance is expected to be achieved. This as long as the disturbance is within the disturbance model bandwidth.

8.2.3 UDE based shunt active power filter

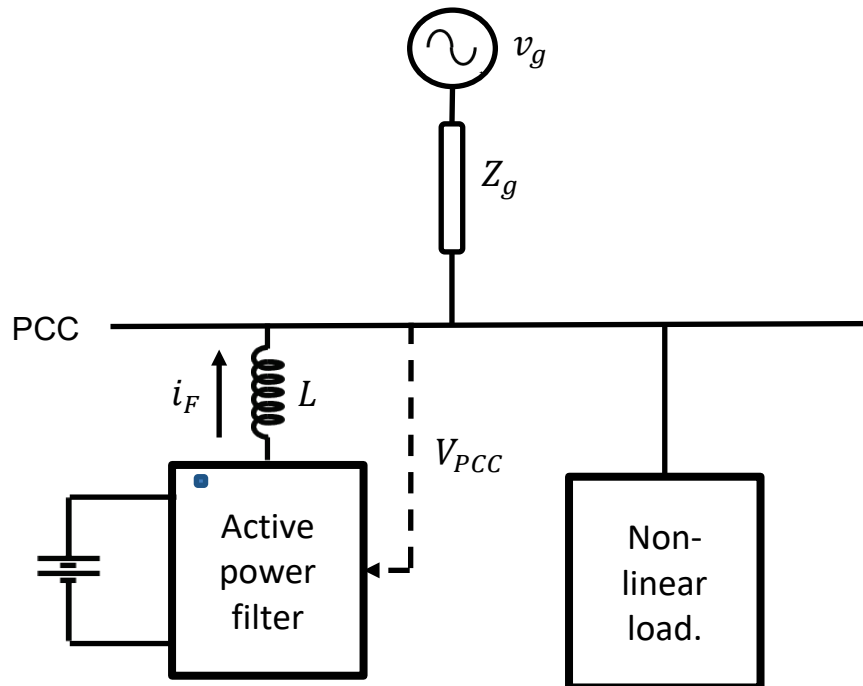


Fig 8.1 Diagram of weak grid section where a non-linear load is connected in parallel with an active power filter.

An active power filter is a device designed to locally compensate the influence of the harmonic currents on the voltage THD at the Point of Common Coupling (PCC). The active power filter is supplying the load harmonic current by injecting the harmonic currents at negative phase. Active power filter can be a critical element in locations where the grid connection is weak, and therefore the grid impedance is high. Fig 8.1 shows a schematic diagram of an active power filter connected at the point of common connection of a weak grid. In the classic active power filter design, the controller uses the measurement of the load or grid current to generate the harmonic compensation current. This sensor can be eliminated by using a disturbance observer to shape the inverter output impedance.

One of the fundamental results of the UDE is its ability to shape the inverter output impedance directly and therefore a UDE controlled inverter can be designed to have high impedance at the grid fundamental frequency and very low impedance at the compensated harmonic region. In chapter 3 it was discussed that the harmonic current can be analyzed at each frequency separately and it was demonstrated that the output current of two inverters in parallel is shared with relation to their output impedance. This is true as long as their internal source generates the same voltage. In the case of the UDE based active power filter the impedance is determined by the design of the UDE filter and as shown in this thesis can be significantly reduced around the frequency region of interest. The load current can be shared in a way where the majority of the harmonic current is comes from the active power filter. This can be achieved by designing an inverter with very low impedance at the harmonics and a high impedance at the fundamental frequency.

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Appendix A

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Impedance Shaping for Parallel Operation of Inverters in Islanded AC Microgrids

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Abstract—This paper proposes a new decentralized control strategy for parallel inverters operating in an islanded Microgrid. The proposed technique uses the Uncertainty and Disturbance Estimation (UDE) strategy in order to generate a virtual output impedance while keeping the voltage of the internal Electro-Motive Force (EMF) source equal for all the inverters in the system. The system achieves accurate current sharing over a broad spectrum, which is proportional to the inverter capacity. Simulation results are provided to illustrate the performance of this method.

Index Terms—Parallel operation of inverters, virtual impedance, droop control, proportional load sharing.

I. INTRODUCTION

Parallel operation of inverters in AC microgrids is essential for the Distributed Generators (DG) to be able to share loads. In islanded microgrids load sharing is usually crucial for the stability of the entire power system. The key issue in parallel operation of inverters in islanded grids is to share the load current proportionally to the power rating of the inverter units, see [1], [2]. Load sharing in microgrids has been widely investigated in, e.g. [2], [3], [4], [5], [6], [7]. The control strategies of paralleled inverters can be divided into centralized controllers and decentralized controllers. Centralized controllers provide better accuracy, but demand communication channels between the units. For example, in master slave control, as in [8], one inverter acts as a voltage source and the rest act as controlled current sources feeding the load proportional to their power rating capacity. Decentralized controllers have no communication lines between the units and therefore, they are more redundant.

The main decentralized control strategy for parallel operation is the voltage-frequency droop control, see, e.g., [3], [9]. This control strategy achieves high reliability, since no communication interconnections are needed between the units. This method

is characterized by voltage and frequency deviation due to the load effect. Other drawbacks of this methods consist of the high dependency on the actual output impedance of the inverter, the poor ability to share harmonic currents and the slow transient response due to the need of real-time active and reactive power calculation. The impedance dependence and low accuracy of the load sharing can be solved by using the robust droop controller, as in [1], [2]. The harmonic current sharing is usually sorted out by adding a virtual harmonic impedance loop to the droop controller [9]. In [10] a new droop controller for sharing harmonic currents has been proposed. The main feature of this method is the ability to use the free capacity of the inverter to compensate the harmonic current. All of these methods demand high computation power, output current measurement, and have slow transient responses.

In this paper a new virtual impedance scheme is proposed, using the UDE control. In [11] it has been proven that, using the UDE control strategy, the closed-loop system has two degrees of freedom, and therefore a virtual impedance can be shaped. It has been shown that in some systems, the tracking performance and the disturbance rejection performance can be decoupled. Using this feature of the algorithm, we achieve a continuous output impedance, while maintaining the EMF equal for all the units. Furthermore, the achieved virtual output impedance is able to share the fundamental and harmonic currents proportional to the inverter capacity. This new method for power distribution between parallel operating inverters is a change of paradigm. Instead of looking into the tracking performance of the system, this controller manipulates the disturbance rejection performance in order to achieve the desired performance. The main advantages of this method are the wide bandwidth of the current sharing, the lack of need for real time power computation and the lack of virtual impedance loop.

The paper is organized as follows. Section II describes

the general design process of the UDE controller. Section III describes the dual loop modelling of the inverter. Section IV describes the controller design process. Section V analyses the current sharing with respect to the filter design, and Section VI shows preliminary simulation results. The paper ends with a Conclusions section.

II. UDE CONTROLLER BRIEF OVERVIEW

The UDE controller uses an estimation of the model deviation and of the disturbance by calculating it from the model equation [12], [11], [13], [14]. Consider a linear, time-invariant plant

$$\dot{x}(t) = Ax(t) + Bu(t), \quad (1)$$

where $x(t) = [x_1(t) \dots x_n(t)]^T \in \mathbb{R}^n$ is the state and $u(t) \in \mathbb{R}^m$ denotes the input. The deviated dynamics associated to (1) are described by

$$\dot{x}(t) = (A + \Delta A)x(t) + (B + \Delta B)u(t) + d(t), \quad (2)$$

where ΔA , ΔB are the model deviations from the nominal matrices A and B respectively, and $d(t)$ is the disturbance. The desired reference tracking model is

$$\dot{x}_m(t) = A_m x_m(t) + B_m \tilde{c}(t), \quad (3)$$

where $x_m(t) = [x_{m1}(t) \dots x_{mn}(t)]^T \in \mathbb{R}^n$ is the state of the tracking model and $\tilde{c}(t) \in \mathbb{R}^m$ is the reference to be tracked. Consider the model error,

$$e = \begin{bmatrix} x_{m1} - x_1 \\ x_{m2} - x_2 \\ \dots \\ x_{mn} - x_n \end{bmatrix}. \quad (4)$$

According to [11], the control law is

$$Bu(t) = A_m x(t) + B_m \tilde{c}(t) - Ax(t) - ude(t), \quad (5)$$

with $ude(t)$ defined in the s -domain by

$$UDE(s) = U_d(s) \cdot G(s), \quad (6)$$

where $UDE(s)$ is the Laplace transform of the signal $ude(t)$, $G(s)$ is a low-pass filter (LPF) and $U_d(s)$ is representing the uncertainties and external disturbances of the system and is given at the time domain as (2),

$$u_d(t) = \Delta Ax(t) + \Delta Bu(t) + d(t) = \dot{x}(t) - Ax(t) - Bu(t). \quad (7)$$

If the following criterion holds [12]

$$[I - BB^+] \cdot [A_m X + B_m \tilde{c}(t) - AX - \Delta AX - d(t)] = 0, \quad (8)$$

where B^+ is the pseudo inverse of B . Then the error dynamics, according to [11], is

$$\dot{e}(t) = A_m e(t). \quad (9)$$

Note that if B is a square invertible matrix, then the condition is always satisfied. Defining

$$H_m(s) = (sI - A_m)^{-1} B_m, \quad (10)$$

the controlled state of (2) can be written as [11]

$$X(s) = H_m(s) \tilde{C}(s) + H_d(s) B \cdot B^+ U_d(s), \quad (11)$$

where $X(s)$ is the Laplace transform of $x(t)$ and

$$H_d(s) = (sI - A_m)^{-1} (1 - G(s)). \quad (12)$$

A closer look at (11), shows that, indeed, using this UDE strategy, the disturbance rejection is decoupled from the reference tracking.

III. MODELLING THE INVERTER FOR UDE CONTROL DESIGN

Consider a single phase inverter followed by an LC output filter shown in Figure 1a., where $u(t)$ is the average inverter voltage over one switching cycle [15], $I_o(t)$ is the load current, $I_L(t)$ and $V_c(t)$ are the inductor current and capacitor voltage, respectively. $I_L(t)$ and $V_c(t)$ represent the system states. In order to meet criterion (8), a dual loop approach is used, where two cascaded control loops are derived as in [16]. The inner current control model can be shown in Figure 1b which should meet the requirements

$$\omega_i \gg \omega_v \quad (13)$$

and

$$\left\| \frac{I_L(s)}{V_c(s)} \right\| \ll \left\| \frac{V_c(s)}{I_o(s)} \right\|, \quad (14)$$

where ω_i and ω_v are the bandwidths of current and voltage loops, respectively. The inner current loop can be designed based on different strategies such as those described in [17] and [18]. Note that condition (14) should be satisfied only at the relevant design spectrum.

The schematic model of single phase inverter is shown in Figure 1a. It can be divided into two sub-models given in Figure 1b and Figure 1c. The former is used to control the inductor current and the latter is used to control the output voltage.

From the current loop control the state equation is

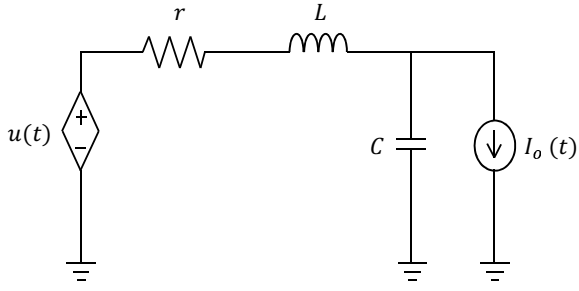
$$\dot{I}_L(t) = \frac{u(t) - I_L(t)r - V_c(t)}{L}, \quad (15)$$

where L is the inductance and r denotes the resistance of the inductor. Since the analysis of the inner loop is beyond the scope of this paper, we assume that the constraints (13) and (14) are satisfied.

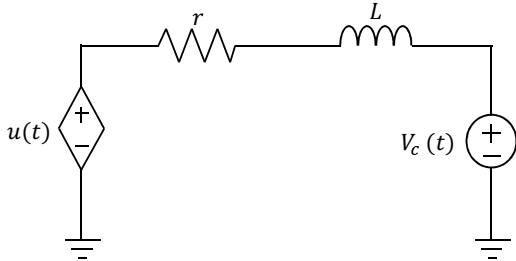
Similarly, the system in Figure 1c can be modelled as

$$\dot{V}_c(t) = \frac{I_L(t) - I_o(t)}{C}, \quad (16)$$

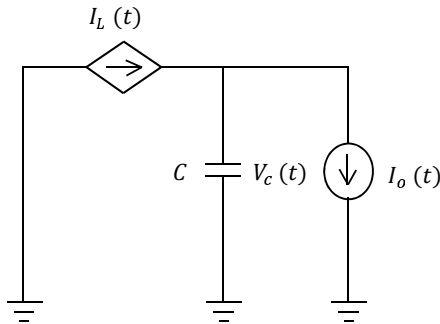
where C is the output capacitance. From (16), the state space model of the system is given by equations of the form (2), with



(a) Single phase inverter plant schematic



(b) Inner current model for control



(c) Outer voltage model for control

Figure 1: System schematic

$$A = 0, B = \frac{1}{C}, d(t) = -\frac{1}{C}I_o(t), \quad (17)$$

Note that condition (8) is automatically satisfied for the above system.

IV. CONTROLLER DESIGN

To adjust the tracking performance a first order reference model is used from

$$\dot{x}(t) = -\omega_{bw}x(t) + \omega_{bw}c(t), \quad (18)$$

where ω_{bw} is the bandwidth of the tracking performance for the system (2) and $c(t)$ is the reference signal. To achieve suitable tracking performance, the tracking bandwidth should be higher than the reference signal bandwidth.

From (5) and (6) the resulting control law for the system, in s -domain, is

$$I_L^*(s) = \frac{C \cdot \omega_{bw}}{1 - G(s)} \tilde{C}(s) - \frac{C(\omega_{bw} + G(s) \cdot s)}{1 - G(s)} V_c(s), \quad (19)$$

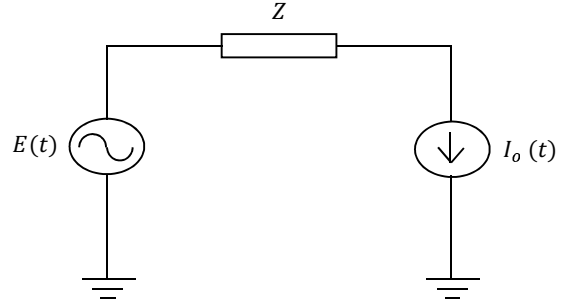


Figure 2: Inverter output model

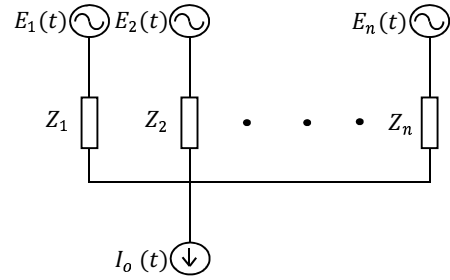


Figure 3: Parallel operation model of N inverters

where $G(s)$ is a low pass filter and $I_L^*(s)$ is the input reference for the current controller. Using this control law, the output voltage is derived from (11) as

$$V_c(s) = \frac{\omega_{bw}}{s + \omega_{bw}} \tilde{C}(s) - \frac{1 - G(s)}{C(s + \omega_{bw})} I_o(s). \quad (20)$$

By Figure 2, note that at the point where the load is connected, the voltage is

$$V_c(s) = E(s) - I(s)Z(s), \quad (21)$$

where $E(s)$ is the internal EMF source of the inverter. From (20) and (21), it follows that

$$E(s) = \frac{\omega_{bw}}{s + \omega_{bw}} \tilde{C}(s) \quad (22)$$

and the virtual output impedance is

$$Z(s) = \frac{1 - G(s)}{C(s + \omega_{bw})}. \quad (23)$$

Note that $Z(s)$ is independent of the tracking performance of the system. $G(s)$ can be shaped according to [13] to meet the desired output impedance. In Figure 3, the schematic diagram of N inverters operating in parallel is shown. It is clear that if the EMF of each unit is identical in phase and amplitude, the current sharing between depends on the internal impedance as described by the equation

$$I_i(s) = \frac{Y_i(s)}{\sum Y_i(s)} I_o(s), \quad i = 1, \dots, N, \quad (24)$$

where $Y_i(s)$, $i = 1, \dots, N$ is the output admittance of the inverter i and $\sum Y(s)$ denotes the total admittance of the N parallel inverters.

V. FIRST ORDER FILTER DESIGN FOR PARALLEL OPERATION

As concluded in Section IV, the current sharing depends on the relative output impedance of each inverter connected to the bus¹. To cancel the pole created by the tracking performance (23) we choose a filter of the form

$$G(s) = \frac{\omega_f - \omega_{bw}}{s + \omega_f}. \quad (25)$$

Substituting (25) into (23) yields

$$Z(s) = \frac{1}{C(s + \omega_f)}, \quad (26)$$

where (26) is the final form of the output impedance. Note that $Z(s)$ is similar to the impedance of an RC filter.

Consider N parallel operated inverters where the output capacitor of each inverter is C_i , $i = 1, \dots, N$ and the filter bandwidth of each inverter is ω_{fi} , $i = 1, \dots, N$. Then the total output admittance is

$$\sum Y_i(s) = (C_1 + \dots + C_N)s + (C_1 \cdot \omega_{f1} + \dots + C_N \omega_{fN}) \quad (27)$$

and the relative impedance of each unit is

$$\frac{Y_i(s)}{\sum Y_i(s)} = \frac{C_i(s + \omega_{fi})}{(C_1 + \dots + C_N)s + (C_1 \cdot \omega_{f1} + \dots + C_N \omega_{fN})}, \quad (28)$$

$i = 1, \dots, N$. Consider ω_{sys} the maximum harmonic order of the shared current. If the constraint

$$\omega_{fi} \gg \omega_{sys}, \quad i = 1, \dots, N, \quad (29)$$

is satisfied, then the current ratio of two parallel units can be evaluated as

$$\frac{I_i}{I_j} \simeq \frac{C_i \omega_{fi}}{C_j \omega_{fj}}, \quad i = 1, \dots, N, \quad j = 1, \dots, N, \quad i \neq j. \quad (30)$$

VI. SIMULATION RESULTS

A Simulink-based simulation is conducted utilizing two UDE controlled inverters and a rectifier load, all connected in parallel. The simulation results emphasize the current distribution between the two parallel inverters, see Table I for the LC filter characteristics of the inverters, The UDE controller characteristics of the inverters are shown in Table II, the inverter simulation model is given in Figure 4 and the entire system schematic is given at Figure 5. The inverter output voltage is the voltage across the output capacitor. To generate the same EMF for both inverters, a PLL loop has been designed for each of them, and the same reference model has been used for both. Note that the UDE characteristics have been chosen to meet the requirements (13) and (14).

Figure 6 shows the inverters output impedance over a relevant spectrum (1st – 31st harmonics). Figure 7 shows the admittance related to the total system admittance over the same spectrum as in Figure 6. Note that the related admittance is predicting the current distribution between the units as in (24) and (28). Figure 8 shows the steady-state output currents of the simulated system and Figure 9 shows the output voltage.

¹We only consider cases when the feeder impedance is negligible.

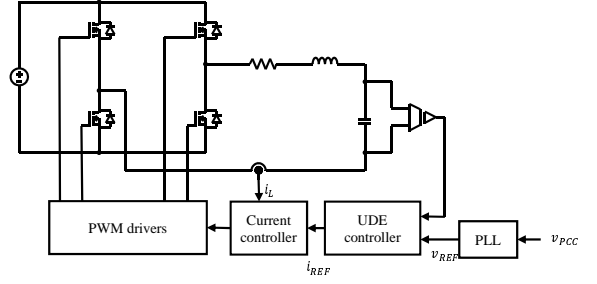


Figure 4: Inverter simulation model

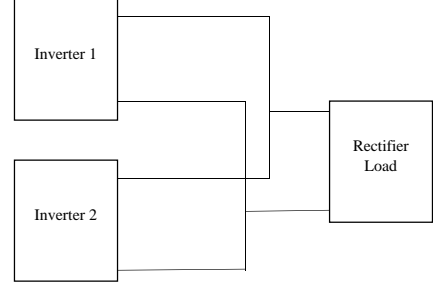


Figure 5: Simulated system schematics

VII. CONCLUSIONS

This paper proposes a new method for power distribution between parallel operating inverters. This method represents a change of paradigm, since instead of looking into the tracking performance of the system, this controller manipulates the disturbance rejection performance to achieve the desired performance. The main advantages of this method are the wide bandwidth of the current distribution, the lack of need for real time power calculation and the lack of virtual impedance loop. The transient performance of such systems may be further investigated with regards to the presence of pulsating loads and switching sources. Another subject to be addressed in future work is the case when the feeder impedance cannot be neglected. Furthermore, the system can achieve more robust performance by changing the UDE filter in real time subject to specific grid changes.

Table I: Inverter output filter data

Component:	Units:	Value:
r	Ω	0.5
L	mH	1
C	μF	50

Table II: UDE controller characteristics

Component:	Form:	Data:
reference model	as in (18)	$\omega_{bw} = 500\pi$
$G_{inverter1}$	$\frac{\omega_f - \omega_{bw}}{s + \omega_f}$	$\omega_f = 2000\pi$
$G_{inverter2}$	$\frac{\omega_f - \omega_{bw}}{s + \omega_f}$	$\omega_f = 4000\pi$

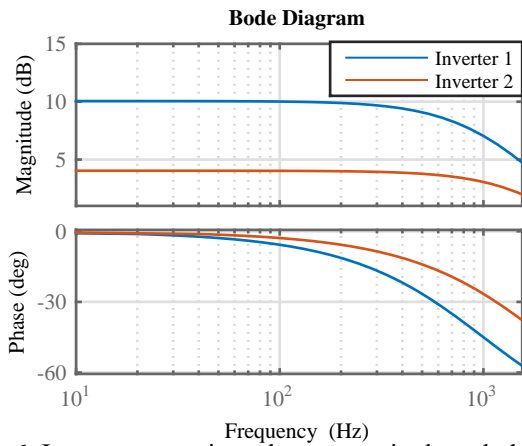


Figure 6: Inverter output impedance magnitude and phase bode diagram

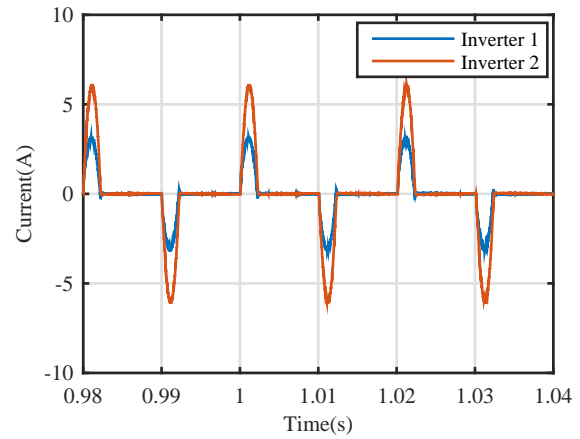


Figure 8: Steady-state output currents of the inverters in the simulated system

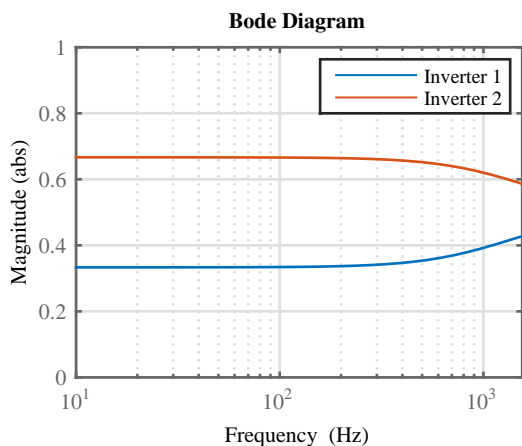


Figure 7: Relative admittance of inverter output

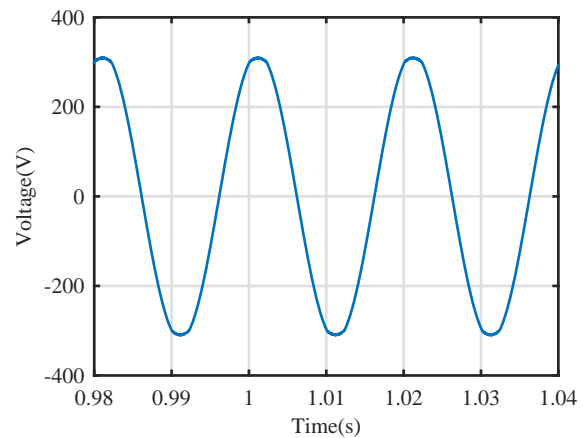


Figure 9: Output Voltage showing no distortions under the UDE control scheme

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Cascaded control to shape output virtual impedance and improve output voltage quality for power inverter

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Abstract—In this paper, a cascaded control scheme for single-phase inverters connected to a load is proposed to improve the power quality and shape the output impedance. The proposed strategy consists of a proportional controller in the inner loop and the Uncertainty and Disturbance Estimator (UDE) in the outer loop. An advanced modulation method is adopted to minimize the control implementation delay and both the current and the voltage control loops are analytically investigated. Simulation and experimental results are presented to validate the theory.

Index Terms—Uncertainty and Disturbance Estimator (UDE), Virtual impedance, Power inverter, Interruptible Power Supply (UPS), Voltage Source Inverter (VSI).

I. INTRODUCTION

Power electronics are essential to integrate renewable energy sources, storage equipment and Uninterruptable Power Supply (UPS) systems to the grid. The operation of power inverters plays a key role in modern micro-grids [1] and emerges several challenges, i.e. to keep the system stable, to maintain high output voltage quality and to be able to define the closed loop virtual impedance for different applications. In the literature, various methods have been proposed for inverters connected to a load to bypass harmonic currents and maintain high power quality at the output of the inverter. Since power quality improvement is of major importance, Proportional Resonant (PR) controllers have been designed and represent a well established method where a voltage feedback is used for compensating the harmonic current [2]. However, the PR method is not robust to deviations in the fundamental frequency [3] and requires high computational power, which results from the need of separate filters for each harmonic. Another method for compensating harmonic currents is to add an integration of

the current feedback to the voltage signal. This method creates a closed loop capacitive output impedance to compensate the harmonic currents [4] but may suffer from instability issues in the presence of inductive loads. Furthermore, several advanced control schemes have been developed based on Lyapunov methods and sliding techniques which result in an enhanced inverter performance [5], [6], but they introduce an increased complexity in their implementation [7].

In this work, by designing the voltage controller using the UDE algorithm a very low THD can be obtained without the need of several harmonic filters. Nevertheless, the output impedance can be designed based on the controller parameters to match various applications such as parallel operation [8]–[10], oscillation damping [11], [12], fault current limiting [13], [14], etc. The paper also shows that by using an asymmetric pulse-width-modulation (PWM) technique, the current closed loop time delay is designed to be equal to half of a switching cycle. Both simulation and experimental results of an inverter connected to a high peak current non-linear load are provided to verify the proposed control strategy.

The paper is organized as follows: Section II provides a general overview of the UDE controller and Section III describes the proposed cascaded controller. Analysis of the internal current loop, including the asymmetric modulation technique and time-delay reduction method is given in Subsection III-A and description of the UDE control design is given in Subsection III-B. Simulation and experimental results for a system with high natural output impedance are presented in Section IV and Section V, respectively.

II. UDE OVERVIEW

The UDE controller uses an estimation of the model deviation and of the external disturbance by calculating them from the nominal model equations [15], [16]. To further explain this, consider the linear, time-invariant plant

$$\dot{x}(t) = (A + \Delta A)x(t) + (B + \Delta B)u(t) + d(t), \quad (1)$$

where $x(t) = [x_1(t) \dots x_n(t)]^T \in \mathbb{R}^n$ is the state vector and $u(t) \in \mathbb{R}^m$ denotes the input. ΔA , ΔB are the model deviations from the nominal matrices A and B respectively, and $d(t)$ is the disturbance. Let

$$\dot{x}_m(t) = A_m x(t) + B_m \tilde{c}(t) \quad (2)$$

be the desired reference tracking model where $x_m(t) = [x_{m1}(t) \dots x_{mn}(t)]^T \in \mathbb{R}^n$ is the desired state and $\tilde{c}(t) \in \mathbb{R}^m$ is the reference to be tracked. According to [16], the desired tracking can be achieved using the control law

$$Bu(t) = A_m x(t) + B_m \tilde{c}(t) - Ax(t) - ude(t), \quad (3)$$

with $ude(t)$ defined in the s domain by

$$UDE(s) = U_d(s) \cdot G_U(s), \quad (4)$$

where $UDE(s)$ is the Laplace transform of the signal $ude(t)$ and $G_U(s)$ is a low-pass filter (LPF). $U_d(s)$ represents the uncertainties and external disturbances of the system and, according to (1), is given in the time domain as

$$u_d(t) = \Delta Ax(t) + \Delta Bu(t) + d(t) = \dot{x}(t) - Ax(t) - Bu(t). \quad (5)$$

If the following criterion holds [15]:

$$[I - BB^+] \cdot [A_m X + B_m \tilde{c}(t) - AX - \Delta AX - d(t)] = 0, \quad (6)$$

where B^+ is the pseudo inverse of B , then according to [16] the reference is tracked. Note that if B is a square invertible matrix, then the condition is always satisfied. Defining

$$H_m(s) = (sI - A_m)^{-1} B_m, \quad (7)$$

the controlled state of (1) can be written as [16]

$$X(s) = H_m(s) \tilde{C}(s) + H_d(s) B \cdot B^+ U_d(s), \quad (8)$$

where $X(s)$ is the Laplace transform of $x(t)$ and

$$H_d(s) = (sI - A_m)^{-1} (1 - G_{UDE}(s)). \quad (9)$$

A closer look at (8) shows that, indeed, using this UDE strategy, the disturbance rejection is decoupled from the reference tracking.

III. PROPOSED CASCADED CONTROLLER

The proposed controller forms a cascaded control structure as shown in Figure 1. The inner loop controls the inverter current i_L , by regulating the duty-cycle. The outer loop controls the capacitor voltage v_c , by regulating the inner loop reference. The capacitor voltage is the system output. Since the inverter voltage is implemented using PWM and the controller is implemented digitally, the internal delays of the system, must be taken into account as it is explained in the sequel. The main task of the current loop design is to achieve a very high bandwidth in order to consider it as a unity-gain loop [17].

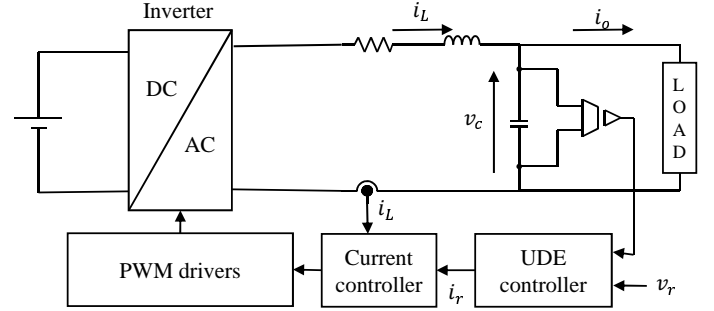


Figure 1: Cascaded control structure

A. Internal current loop

Because of the high bandwidth required for the current control loop, the PWM and digital control time delays should be taken into account. In order to minimize these incorporated delays, an asymmetric PWM method has been adopted [18]. In this method, the PWM comparator register is updated twice in each switching cycle. The first update is at the beginning of the cycle, determining the transistor ON time and the second is when the counter reaches the maximum. The second time determines the transistor OFF time. This results in the PWM update frequency being double the switching frequency.

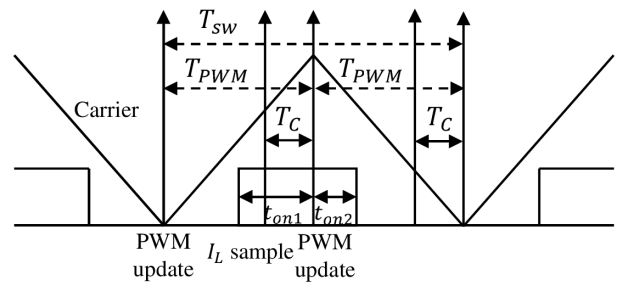


Figure 2: Asymmetric PWM switching cycle timing

In the literature there are exact models of uniformly sampled PWM inverters in both the s -domain [19] and the z -domain [20]. These models take into account the impact of the duty-cycle operation point over the time delay. Despite this fact, the PWM cycle can be modeled as a zero-order-hold (ZOH)

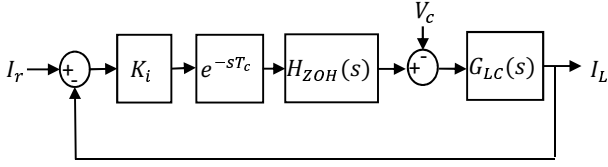


Figure 3: Current control loop.

without significant difference [21]. In a case of digitally implemented PWM, an approach of uniformly sampled PWM should be considered [22]. In this approach, the VSI is modeled as a ZOH followed by the output filter and the DSP sampling and computation time are then modeled as an extra delay.

In Figure 2 a switching cycle is presented, where T_{SW} is a one switching cycle, T_{PWM} is a half switching cycle, T_c is the current control task computation time, t_{on1} is the on time at the first half of the switching cycle and t_{on2} is the on time at the second half of the switching cycle.

Figure 3 shows the closed loop model of the current controller with a proportional compensator. This model incorporates the PWM modulation model, the control time delay and the filtering process.

The ZOH in the s-domain is defined as

$$H_{ZOH}(s) = \frac{1 - e^{-sT_{PWM}}}{s}, \quad (10)$$

where T_{PWM} is the asymmetric PWM sampling frequency and is equal to $T_{PWM} = \frac{T_{sw}}{2}$ [18], where T_s is the switching frequency. The transfer function from the inverter voltage to the inductor current is

$$G_{LC}(s) = \frac{1}{Ls + r}. \quad (11)$$

Using (10) and (11), the process to control is modelled as

$$P(s) = \frac{1 - e^{-sT_{PWM}}}{s} \cdot \frac{1}{Ls + r} e^{-sT_c}. \quad (12)$$

In the case where T_c is a multiple of T_{PWM} , the control time delay can be modelled as a unit delay. However, when T_c is a fraction of T_{PWM} , then the modified zeta-transform [23] has to be used. By considering m as

$$m = 1 - \frac{T_c}{T_{PWM}} \in [0, 1], \quad (13)$$

then from (12) and (13), the modified z-transform is

$$P(z, m) = (1 - z^{-1}) Z_m \left\{ \frac{1}{s} \cdot \frac{1}{Ls + r} e^{-s(1-m)T_{PWM}} \right\} \\ = \frac{1}{r} \cdot \frac{z(1 - e^{-\frac{r}{L}mT_{PWM}}) - e^{-\frac{r}{L}T_{PWM}} + e^{-\frac{r}{L}mT_{PWM}}}{z(z - e^{-\frac{r}{L}T_{PWM}})}, \quad (14)$$

where $Z_m\{\}$ is the modified z transform operator. Please note that when $m = 1$, (14) becomes the zeta transformation of the LC filter transfer function and when $m = 0$, (14) is the zeta transformation of the LC filter transfer function with a unit delay at the input. By using a proportional compensator which has single multiply and accumulate operation, a very small T_c

can be chosen. Note that if $T_c \ll T_{PWM}$ then $m \approx 1$. In this case, from (14) the closed loop transfer function is

$$P_i(z) = \frac{\frac{k_i}{r}(1 - e^{-\frac{r}{L}T_{PWM}})}{(z - e^{-\frac{r}{L}T_{PWM}}) + \frac{k_i}{r}(1 - e^{-\frac{r}{L}T_{PWM}})}. \quad (15)$$

Choosing the controller gain to be

$$k_i = \frac{re^{-\frac{r}{L}T_{PWM}}}{1 - e^{-\frac{r}{L}T_{PWM}}}, \quad (16)$$

the closed loop transfer function becomes

$$P_i(z) = \frac{e^{-\frac{r}{L}T_{PWM}}}{z}, \quad (17)$$

which leads to a deadbeat response. Transferring the closed loop transfer function to the s-domain shows that current loop can be represented in the s-domain as a delay, i.e.

$$P_i(s) \approx e^{-\frac{r}{L}T_{PWM}} e^{-sT_{PWM}}. \quad (18)$$

At the low frequency range where $\omega \ll \frac{2\pi}{T_{PWM}}$ and the term $-\frac{r}{L}T_{PWM}$ is sufficiently small, (14) is approximated by a Taylor expansion as

$$P_i(s, m) \approx \frac{m(1 + sT_{PWM}) + 1 - m}{(1 + sT_{PWM})(sL + r)}. \quad (19)$$

From (19) it is clear that at low frequencies (as a rule of thumb where $\omega < \frac{2\pi}{10 \cdot T_{PWM}}$) the system can be approximated as

$$P_i(j\omega) \approx \frac{1}{j\omega L + r}, \quad (20)$$

even when $m = 0$ (full cycle delay). From (20), the closed loop transfer function is

$$I_L(s) = \frac{k_i}{r + k_i} \cdot \frac{1}{\frac{L}{r+k_i}s + 1} I_r(s) - \frac{1}{r + k_i} \cdot \frac{1}{\frac{L}{r+k_i}s + 1} V_c(s) \quad (21)$$

Which is later used to design the voltage closed-loop.

B. Voltage loop design

The voltage loop design starts from modeling the output voltage dynamics. Looking at Figure 1, the dynamics are described from

$$C \frac{dv_c}{dt} = i_L - i_o. \quad (22)$$

In a more accurate model description, the output impedance of the current loop is represented as a parallel branch to the current source [7]. In the case of a proportional controller, as in the present work, the output admittance branch is derived from (21) as

$$Y_i(s) = \frac{1}{r + k_i} \cdot \frac{1}{\frac{L}{r+k_i}s + 1}. \quad (23)$$

In the low frequency range where $\omega \ll \frac{r+k_i}{L}$, the output impedance is approximated to be resistive with $R_i = r + k_i$. Using (21) and (22) it yields

$$\dot{v}_c(t) = -\frac{1}{C \cdot R_i} v_c(t) + \frac{1}{C} i_r(t) - \frac{1}{C} i_o(t), \quad (24)$$

which is a first order model in the form of (1) where v_c is the controlled state i_r the control input and i_o is the disturbance input. Hence, the UDE control design can be applied which includes two design steps. The first step is to choose a reference model for the system and the second step is to choose the UDE filter. In the case of an inverter with an LC filter and a closed loop current control, the output derived from (8) is

$$V_c(s) = H_m(s) \cdot V_r(s) + H_d(s) \cdot I_o(s). \quad (25)$$

Note that since the system order is 1, then $B \cdot B^+ = 1$. A close look at (25) shows that it is similar to the Ohm's law for a voltage source

$$V_o = E - Z_o I_o. \quad (26)$$

(25) and (26) demonstrate that under UDE control the internal EMF is determined by the reference model and the output impedance by the UDE filter. The UDE control design starts from choosing a reference model. Because the model is a first order, the main criterion of the reference model is to contain the spectral content of the reference signal. Hence, a first order model is adopted of the form

$$\dot{x}(t) = -\omega_r x(t) + \omega_r v_r(t), \quad (27)$$

where ω_r is the reference model bandwidth and v_r is the reference signal. The second phase of design is to choose the UDE filter. This is chosen from the desired closed loop output impedance. Taking the first order form for the UDE filter, it results in a filter of the form

$$G_U(s) = \frac{\omega_U \cdot k_U}{s + \omega_U}, \quad k_U \in [0, 1]. \quad (28)$$

From (9) and (28) the output impedance of the system becomes

$$Z_o(s) = \frac{s + \omega_U(1 - k_U)}{C(s + \omega_r)(s + \omega_U)}, \quad (29)$$

which shows that ω_U and k_U determine the output impedance characteristics. At low frequencies where $\omega \ll \omega_r$ and $\omega \ll \omega_U$,

$$\begin{aligned} Z_o &\approx \frac{j\omega}{C\omega_r\omega_{UDE}} + \frac{(1 - k_{UDE})}{C\omega_r}, \text{ with} \\ X_o &\approx \frac{\omega}{C\omega_r\omega_U}, \quad R_o \approx \frac{1 - k_U}{C\omega_r}. \end{aligned} \quad (30)$$

From (3) and (4) the resulting input to the current controller is

$$I_r(s) = C \left(\frac{\omega_r}{1 - G_U(s)} V_r(s) - \frac{\omega_r + sG_U(s)}{1 - G_U(s)} V_c(s) - \frac{1}{C \cdot R_i} V_c(s) \right). \quad (31)$$

Note that ω_r and ω_U are bounded by the stability margins which are determined by the time-delay from the closed-loop current controller.

IV. SIMULATION RESULTS

In order to demonstrate this method, a voltage source inverter followed by an LC filter is simulated. The non-linear load consists of a rectifier followed by a capacitor and a resistive load, the capacitor size is $570\mu F$ and the output resistor is 100Ω . The parameters of the system can be found in Table I.

In the simulation, the current controller is designed to achieve dead-beat response in order to keep the bandwidth of the internal loop as high as possible. This is done to keep the UDE filter bandwidth well inside the current controller spectrum. The control signal is the Duty-cycle of the PWM, The Duty cycle is updated twice in each switching cycle and determining the on-time and the off-time of the transistor in accordance to the asymmetric modulation method described in Section III. The simulation results are demonstrating promising results and the THD under the non-linear load is significantly reduced (2.15%), compared to the feed forward operation. Figure 4 shows the steady-state voltage and current waveform for UDE controlled inverter compared to the feed-forward controller. Figure 5 shows the spectral analysis for the output voltage, in which the UDE harmonics are well suppressed.

Table I: System and controller parameters

Parameters	Values
R	0.5Ω
L	$3mH$
K_i	89
ω_r	$2 \cdot \pi \cdot 500 \frac{rad}{sec}$
C	$27\mu F$
m	0.975
ω_U	$2 \cdot \pi \cdot 2000 \frac{rad}{sec}$
k_U	0.93

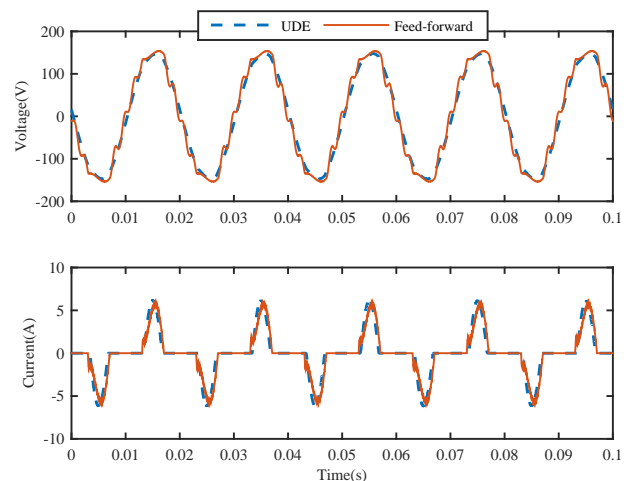


Figure 4: Voltage and current of the non-linear load under the UDE and under feed-forward control

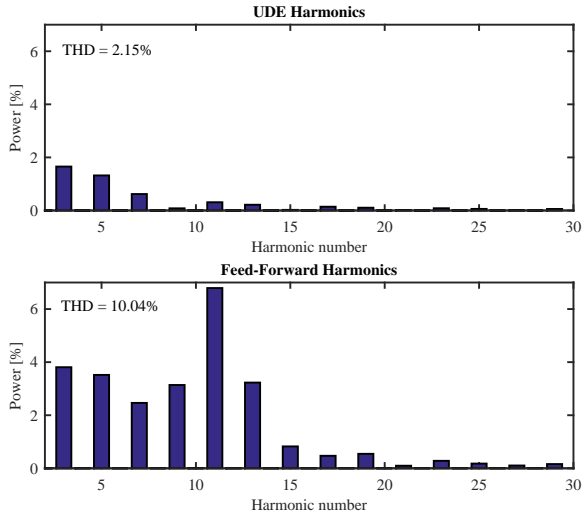


Figure 5: Voltage harmonic content - non-linear load

V. EXPERIMENTAL RESULTS

To validate the proposed theory, a laboratory prototype has been built. The experimental setup consists of a modified TI TMDSHV1PHINKIT kit and the control algorithm is implemented over TI F28M35 control core. The laboratory prototype has been powered by a laboratory high voltage DC power supply. The DC-Bus voltage has been set to 190V. The controller code has been generated using Simulink automatic code generation tools and therefore the computation delay of the current controller has a minimum value of $0.33T_{PWM}$ ¹. Therefore the controller gain is limited and as a result of that, the current closed loop bandwidth is limited as well. The experimental setup parameters are given in Table II. The load is made of a diode rectifier followed by parallel RC load. The output resistor of the load is a 100Ω and the parallel capacitor is $960\mu F$. As shown from the results the load Crest Factor (CF) is 3.25. The output voltage THD for the proposed controller is 3.7% for the first 29 harmonics. The voltage RMS value is kept at 110V without a dedicated loop as a result of the low closed-loop output impedance. The experimental results are then compared to a feed-forward controller with current feedback. In the experimented feed-forward controller a small virtual impedance is added in order to damp the LC filter resonance as in [24]. Figure 6 shows the UDE controlled output voltage vs the load current, Figure 7 shows the output voltage for a feed-forward controller and Figure 8 shows the spectral output analysis of both control methods, In which the voltage harmonics for the UDE are well suppressed.

¹To the authors' knowledge a faster computation time is achievable by avoiding automatic code generation

Table II: Experimental setup parameters

Parameters	Values
R	0.5Ω
L	$3mH$
K_i	59
ω_r	$2 \cdot \pi \cdot 500 \frac{rad}{sec}$
C	$27\mu F$
m	0.66
ω_U	$2 \cdot \pi \cdot 1500 \frac{rad}{sec}$
k_U	0.95
V_{DC}	190V

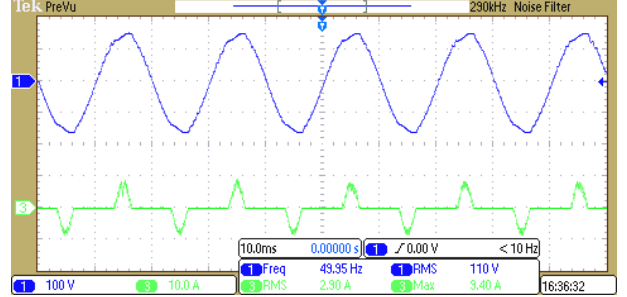


Figure 6: Experimental results for the UDE: output voltage vs load current

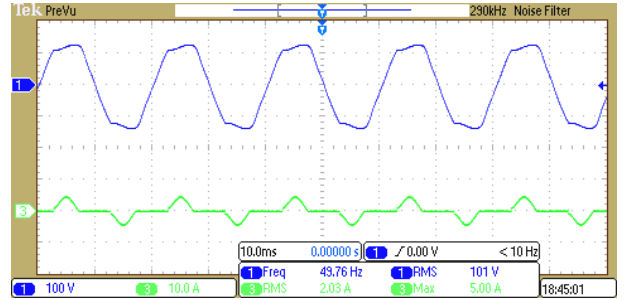


Figure 7: Experimental results for feed-forward controller: output voltage vs load current

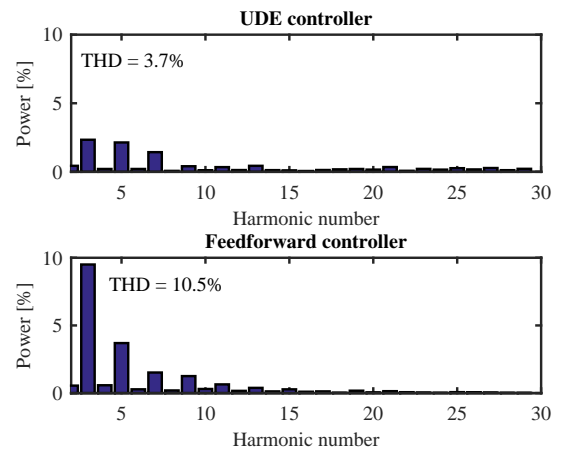


Figure 8: UDE controlled inverter vs feed-forward output voltage harmonics

VI. CONCLUSION

In this paper a new cascaded controller for a voltage source inverter is revealed. By using the UDE algorithm for the voltage loop and a proportional controller for the inner current loop, a very low THD is achieved. An analysis of the closed loop output impedance of the proposed controller is attached. Both simulation and experimental results of the proposed method are provided and compared to feed-forward control without current feedback for the simulation results and with current feedback for the experimental system. The results are clearly showing a suppression of the voltage harmonic content. The proposed controller offers high power quality and suitable output impedance shaping.

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