The University Of Sheffield.

Double Resonant High-Frequency Converters for Wireless Power Transfer

By:

Rui Zhao

A thesis submitted in partial fulfilment of the requirements for the degree of Doctor of Philosophy

The University of Sheffield
Faculty of Engineering
Electronic and Electronical Engineering Department

July 2018

Summary

This thesis describes novel techniques and developments in the design and implementation of a low power radio frequency (40kHz to 1MHz) wireless power transfer (WPT) system, with an application in the wireless charging of autonomous drones without physical connection to its on-board Battery Management System (BMS). The WPT system is developed around a matrix converter exploiting the benefits such as a small footprint (DC-link free), high efficiency and high power density. The overall WPT system topology discussed in this thesis is based on the current state-of-the-art found in literature, but enhancements are made through novel methods to further improve the converter's stability, reduce control complexity and improve the wireless power efficiency. In this work, each part of the system is analysed and novel techniques are proposed to achieve improvements.

The WPT system design methodology presented in this thesis commences with the use of a conventional full-bridge converter. For cost-efficiency and to improve the converters stability, a novel gate drive circuit is presented which provides self-generated negative bias such that a bipolar MOSFET drive can be driven without an additional voltage source or magnetic component. The switching control sequences for both a full-bridge and single phase to single phase matrix converter are analysed which show that the switching of a matrix converter can be considered to be the same as a full-bridge converter under certain conditions. A middleware is then presented that reduces the complexity of the control required for a matrix converter and enables control by a conventional full-bridge controller (i.e. linear controller or microcontroller).

A novel technique that can maximise and maintain in real-time the WPT efficiency is presented using a maximum efficiency point tracking approach. A detailed study of potential issues that may affect the implementation of this novel approach are presented and new solutions are proposed. A novel wireless pseudo-synchronous sampling method is presented and implemented on a prototype system to realise the maximum efficiency point tracking approach. Finally, a new hybrid wireless phase-locked loop is presented and implemented to minimise the bandwidth requirements of the maximum efficiency point tracking approach. The performance and methods for implementation of the novel concepts introduced in this thesis are demonstrated through a number of prototypes that were built. These include a matrix converter

and two full WPT systems with operating frequencies ranging from sub-megahertz to megahertz level. Moreover, the final prototype is applied to the charging of a quadcopter battery pack to successfully charge the pack wirelessly whilst actively balancing the cells. Hence, fast battery charging and cell balancing, which conventionally requires battery removal, can be achieved without re-balance the weight of the UAV.

Publications

Some of the work contained in this thesis has been disseminated at the following international conferences and in learned society journals:

[P1] **R. Zhao**, D.T. Gladwin and D.A. Stone, "Cost Efficient Sub-megahertz Matrix Converter Employing a Conventional Simple Controller," PCIM Asia 2015; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, 2015.

[P2] **R. Zhao**, D.T. Gladwin, D.A. Stone, "Wireless Power System Appling a Microcontroller Dominated Matrix Converter," Industrial Electronics Society, IECON 2015-41st Annual Conference of the IEEE, 2015

[P3] **R. Zhao**, D.T. Gladwin, D.A. Stone, "Maximum efficiency point tracking for resonant wireless power transfer," IET Power Electronics Machines and Drives, PEMD, 2016.

[P4] **R. Zhao**, D.T. Gladwin, D.A. Stone, "Phase shift control based Maximum Efficiency Point Tracking in resonant wireless power system and its realization," Industrial Electronics Society, IECON 2016-42nd Annual Conference of the IEEE, 2016.

[P5] **R. Zhao**, D.T. Gladwin, D.A. Stone, "A Hybrid Wireless PLL for Phase Shift Control Based Maximum Efficiency Point Tracking in Resonant Wireless Power Transmission Systems," Industrial Electronics Society, IECON 2017-43nd Annual Conference of the IEEE, 2017.

[P6] **R. Zhao**, D.T. Gladwin, D.A. Stone, “Kilohertz Double Resonant Wireless Power System using Simple Controller Dominated Matrix Converter," Submitted to IET Power Electron., 2017.

Acknowledgements

Acknowledgements

Firstly, I would like to thank my supervisors Dan Gladwin and David Stone for their inventive, enthusiastic support and guidance throughout the 4 years of my PhD. In particular, as a Chinese who speaks English as a second language, their patience and tolerance have been wholly appreciated. Furthermore, cogniscent of their immensely busy schedules, I am highly appreciative of their help in providing me critical advice and guidance throughout my PhD and with my thesis. I am honoured to be one of their students and feel highly fortunate to have had their close and expert supervision.

Many thanks to all members in the Electrical Machines and Drives group, where work for this thesis was carried out, for their friendly encouragement and support and for the academic, emotional and fundamental support during my time in the UK; In particular, I would like to place on record my thanks to James Green, Guang-Jin Li, Chi Wa Tsang, Jonathan Gomez, Jonathan Davidson, Shahab Nejad and David Hewitt. I must also make a note of thanks to Peter Barton and others who have helped proofread my work.

Of critically importance, I make special acknowledgement to my family. In particular to my parents for their love and encouragement throughout my study, and indeed my grandfather, who guided me to be an electronic enthusiast whilst I was a child. Finally, I must thank my wife for her love and unconditional support. She has given every coulomb of herself to support me wholeheartedly, allowing me to complete my studies.

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1. Introduction and Motivation

There is an increasing demand for more power and energy stored in the portable devices that we use in our everyday lives, however, this has been unmatched by advances in electrochemical battery technology to maximise the potential. This limitation has not only impacted on technological development but has also hindered improvements to our quality of life through the use of zero-emission transportation. In recent years, the issues with battery technologies have become increasingly apparent due to increased marketing and awareness, and indeed the uptake of Electric Vehicles (EVs) and Wearable Electronics (WEs). Users are acutely aware of limitations in the distance that EVs can travel before requiring a charge, and similarly with WEs, these devices often need to be charged daily. There has been a massive increase in the use of quadcopter based drones; from basic use and flying for fun, to carrying out search and rescue missions in hazardous areas. These smaller drones are commonly battery powered, operated by a human controller and have typical flying times of fifteen minutes to an hour. Companies such as Amazon have a desire to use drones to fly autonomously beyond the visual line of sight (BVLoS) of an operator to deliver packages to customers. Although advanced wireless communication technologies have enabled these devices to travel longer distances, they are still restricted in their flying time by the energy stored in the battery and hence need to be recharged, commonly achieved via charging cables. Using wireless power can simplify the process of charging drones and extend flying ranges through operator-less charging at remote locations.

Wireless power transfer (WPT), which could remove the device's "last cable", is in increasing demand. In addition to increased portability, for applications with higher power demand, wireless power offers improved connectivity and convenience, together with higher charging speeds and robustness [1-1].

Whilst there is already a market for applications of wireless power transfer that includes EVs, and Unmanned Aerial Vehicle (UAV) charging, there are a number of other emerging applications

in the industrial, commercial and biomedical fields [1-2, 3, 4, 5, 6, & 7]. Between March and June of 2016, the number of electric vehicles registered in the UK increased by 253% compared to 2014 and 49% compared to 2015 [1-8, 1-9]. While for other battery-power electronics, such as UAVs, according to BI Intelligence, between 2015 and 2020, commercial drones for the civilian market will increase at a Compound Annual Growth Rate (CAGR) of 19% [1-10]. These acknowledgements demonstrate a clear requirement and prospect for the deployment of effective and rapid wireless charging technologies.

Through many years of development, WPT systems can now be achieved using several methods such as lasers, microwaves and coupled fields [1-11]. The first generation of commercial WPT utilises coupled inductance for low power wireless charging (i.e. mobile phone charging) [1-12], but this technology is acknowledged as having low charging efficiencies and only operates over limited distances. Higher energy efficiency and extended distances can be realised by using Strongly Coupled Magnetic Resonance (SCMR) [1-13]. SCMR utilises the mutual inductance between the transmitting coil and receiving coils to transfer power from several watts to kilowatts [1-14, 1-15].

The performance of an SCMR system is highly dependent on the efficiency of the power electronic converter used to drive the transmitter side of the system [1-16]. Conventionally, a two-stage converter approach is taken, but a number of deficiencies have been reported such as the physical size, instability of the DC-link [1-17] and low power factors on the input [1-18, 1-19]. The disadvantages of multistage converters can be resolved by the application of a force-commutated matrix converter [1-20]. The matrix converter for any given AC input can produce a different AC output with arbitrary frequency and magnitude [1-21]. Compared with multistage converters, research shows matrix converters have better performance, power/size ratio, and robustness, particularly for high power and high voltage applications [1-22].

To achieve a high-efficiency, a WPT system must operate at an optimised frequency equal to the self-resonant frequency of the power receiver [1-23]. However, the self-resonant frequency of

the power receiver is calculated by its capacitance and inductance (LC resonator as an example), which can vary with changes in temperature, load impedance, and physical fluctuations [1-11, 1-23, 1-24]. Controlling these factors across the various applications that WPT is likely to be employed is challenging, therefore a WPT system that can operate under a wide range of conditions, and automatically maximise and maintain its efficiency is required.

1.1. Thesis outline

This thesis details novel developments and design techniques of radio frequency (40 kHz to 1 MHz) direct converters (matrix converter) for induction heating and wireless power transfer, with the aim of simplifying the control requirements, and improving the wireless power efficiency and reliability under varying conditions. A review of the state-of-the-art for wireless power transfer systems and the underlying enabling technologies is provided in Chapter 2.

Chapter 3 introduces a novel gate driver design that can provide a negative driving voltage for turning-off MOSFETs used in the converter. The negative voltage generation circuit does not contain any magnetic components (i.e. inductor or transformer) or integrated circuit. With the help of an extra MOSFET and 8 other components, both a boosted high-side turn-on and bipolar drive can be implemented. The new design solves the complexity and cost of implementing a negative voltage turn-off in a non-isolated gate driver design. The gate drive design can be applied to a wide range of commonly used converter topologies, such as buck, buck-boost, half-bridge, full bridge etc., where a solid turn-off can be achieved without changes to the converter design or addition of costly components.

Chapter 4 describes a method of reducing control complexity of a matrix converter through the use of middleware to allow control from a low-cost microcontroller or analogue controller. The methodology proposed reduces the number of power devices that the controller needs to drive by using logic gate circuitry, with the control now required, reduced to that effectively of a full-bridge converter. To demonstrate the methodology, two types of application are investigated: induction heating and wireless power transfer, with the latter requiring higher frequency stability.

Chapter 5 analyses the requirements for tracking the real-time resonant frequency to maintain the efficiency of a WPT system. By using hardware-in-the-loop techniques it examines the practicalities of measuring a changing secondary resonant frequency and matching this on the primary. A method is proposed with practical results that minimises the phase difference of the

transmitting current against the phase of the receiving the voltage to maximise efficiency.

In Chapter 6 the difficulties of wireless phase comparison are considered and it is shown that wireless digital stored synchronous sampling is one effective method to provide pseudo real-time phase difference measurements. Practical methods of wireless pseudo synchronous triggering mechanisms for the digital storage synchronous sampling are discussed, and two physical topologies that can be used in different applications are presented. The design elements of a high-density wireless power receiver are discussed and a prototype is built to demonstrate the phase comparison circuitry. By using this wireless power receiver, a novel wireless power system is complete using the matrix driven power transmitter from Chapter 5. The demonstrator shows off the microcontroller based matrix converter and the maximum efficiency point tracking methodology using phase comparison.

The phase comparison methods introduced in Chapter 6 have high wireless communication bandwidth requirements that may not be practical in some applications. Chapter 7 proposes a novel wireless phase locked loop that uses the frequency domain to reduce the bandwidth requirements. The methodology is detailed and the results presented through both simulation and in hardware.

1.2. Contributions

This thesis proposes novel control and design methodologies to improve converter stability, reduce control complexity and to maximise efficiency under different load conditions in real-time of strong coupled magnetic resonance-based wireless power systems. In particular, the work presented herein has been disseminated in internationally recognised publications. The main contributions are summarised as below:

- A new gate drive circuit is introduced to provide a negative voltage for turn-off with limited discrete components. By adding 6 extra components to a high side gate driver or 9 components to a half-bridge driver, a non-isolated negative voltage can be generated to turn-off the desired MOSFET. So that the driving performance and stability, especially for driving a SiC MOSFET, can be significantly improved.

- A novel logic gate constructed middleware [P1] is proposed to reduce the control complexity of a matrix converter. The middleware sits between a basic controller (i.e. microcontroller and linear controller) and the matrix switch and enables the AC switch formed matrix converter to be controlled as if it was a full bridge converter.

- The matrix converter is adapted to the design of wireless power system [P2]. By implementing the proposed simply controlled matrix converter, a wireless power system featured both cost-effective and improved robustness can be achieved. Meanwhile, a high power density wireless power receiver is introduced, where the transmitted power can be utilised for UAV, EV charging and/or powering.

- A novel resonant frequency tracking methodology for wireless power receiver [P3] is proposed to improve both the wireless power efficiency and its interference immunity. By comparing the phase of transmitting current and receiving voltage, the real-time resonant frequency of the power receiver can then be estimated. The effect of component tolerance on efficiency, where the components are randomly selected, is improved by up to 8%. A

new practical phase shift control based maximum efficiency point tracking design [P4] is detailed to implement the resonant frequency tracking methodology.

- To achieve the desired maximum efficiency point tracking, a novel wireless pseudo synchronous triggering mechanism [P4] for the wireless digital storage synchronous sampling is proposed. This design introduces a new approach to synchronously sampling targeted signals, where those signals can be separately sampled from different systems without physical connections between them.
- A novel wireless phase locked loop with reduced communication bandwidth requirement [P5] is developed to establish a PLL-like control scheme. By converting the phase difference to the frequency domain, and removing the high order harmonics, the bandwidth requirement can be reduced by up to 90%.

1.3. References

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2. Background

2.1. Gate driver for MOSFET base converter

Along with the development of semiconductor technology, the widely-used DC to DC converter is trending towards increasing its switching frequency to mega-hertz level [2-1 and 2-2]. Using higher switching frequency reduces the size of passive components and therefore increases the power density [2-1]. However, several issues can be found in applications fitted with high-frequency switching technology. Those issues include, but are not limited to high switching losses, dV/dt causes false triggering, and un-optimised overdrive [2-3, 2-4 and 2-5].

2.1.1. Gate energy loss

For a MOSFET based converter, the operation of a MOSFET is essentially controlled by charging and discharging its gate parasitic capacitor [2-3]. In a conventional converter, as per the schematic shown in Figure 2.1, the total driving loss can be calculated using the following equation.

$$P_{Gate} = f_s \times V_{Drv} \times \int_0^{\frac{1}{f_s}} I_{Drv}\, dt = f_s \times V_{Drv} \times Q_{Gate} \qquad (1-1)$$

Where f_s is the switching frequency, V_{Drv} is the driving voltage, I_{Drv} is the instantaneous driving current, Q_{Gate} is the total gate charge.

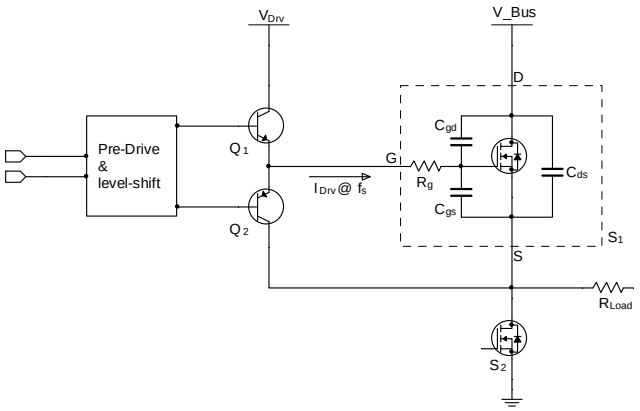

Figure 2.1. Conventional push-pull gate drive circuit with parasitic components of MOSFET.

In order to reduce the driving loss or recover energies from the gate parasitic capacitor, several resonant gate drivers have been introduced [2-6 to 2-12]. In brief, the resonant gate driving approach uses an LC resonant circuit to charge and discharge the gate parasitic capacitor, while "C" is the equivalent gate capacitance and "L" is normally a separate discrete component [2-5]. Some researches [2-15, 2-8] use the leakage inductance of a driving transformer, however, most of those circuits are proposed only for a single switch. The majority use a discrete component for the inductor required in the LC circuit [2-6, 2-7, 2-13 and 2-14], as this avoids potential manufacture variations. To be implemented in a half-bridge application (also includes synchronous rectified buck converter), two identical sets of components are required [2-4]. Furthermore, even [2-4] provided a coupled-inductor based single magnetic component solution; the size and PCB footprint requirements are still an issue. Moreover, to avoid any simultaneous turned-on of both high-side and low-side switches, the timing control for those resonant gate drivers can be challenging due to component tolerances.

2.1.2. False triggering caused by dv/dt

With the trend of increasing the switching frequency, the rising time and falling time when driving a MOSFET is decreased, which has the effect of increasing the voltage slew rate (dv/dt) on the switch node [2-5]. As shown in Figure 2.2, using the full-bridge converter (only half bridge is shown) as an example, at the instant when S1 is turned-on, the voltage at the switching node S will be increasing with a very high slew rate. With such a big voltage change over the limited time, the high dV/dt and corresponding current change will inject a pulsed voltage (V_{pulse}) into the gate parasitic capacitor of S2 [2-5]. In the worst case, V_{pulse} becomes high enough to exceed the gate threshold (V_{gs}) of S2, and S2 will be turned on. In the last decade, this problem became significantly important with the introduction of the HEX MOSFET and the Logic MOSFET that can be turned-on by a logic level voltage.

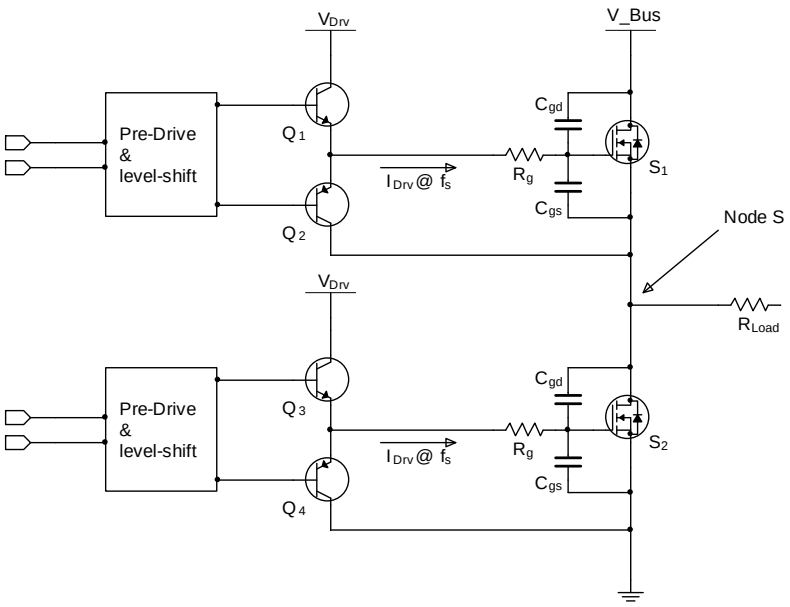

Figure 2.2. Half-bridge of a full-bridge converter showing its switching node S.

Most gate drivers in "totem-pole' topologies, as shown in Figure 2.3, use diodes to adjust the rising and falling time [2-16], which may not able to create a low impedance path to keep the MOSFET off due to its dynamic impedance. Meanwhile, in more recent resonant gate driver designs [2-8, 2-9, 2-14 and 2-15], the gate terminal is left open after been turned-off, which significantly increases the risk of being falsely turned-on. Other designs like [2-13] provide a current path by using a separate MOSFET but this requires precise timing control.

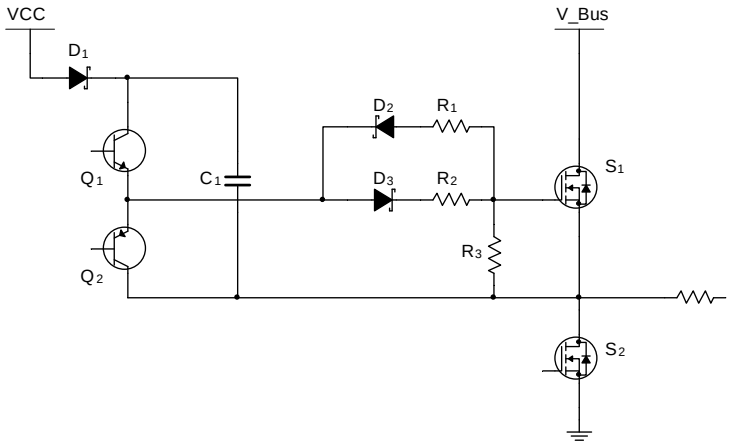

Figure 2.3. Gate driver using totem-pole topologies.

2.1.3. V_{gs} overdriving

As illustrated above, the driving power losses will be increased with higher switching frequencies. To prevents false triggers, in practice, a circuit may use a high driving voltage (V_{Drv}) and utilise MOSFETs with higher V_{gs}. However, although a higher V_{Drv} may reduce the on-state resistance (R_{ds}), the gate driving efficiency will be compromised according to [2-5]. In comparison, using a MOSFET with a low V_{gs}, then if V_{Drv} is minimised to ensure a definite turn-on, high enough to be free from component tolerance and any potential parasitic elements, then the turn-on power loss will be maximised [2-5]. To prevent the MOSFET from the false triggering, a small negative voltage can be applied to maintain the off status of the semiconductor. However, to generate the required negative voltage may be challenging, particularly in a high-frequency converter where the negative biasing current may reach several hundreds of milliamps, numerically.

2.1.4. Generate required negative biases

As concluded above, using negative bias to turn-off a MOSFET has several advantages, particularly for wide bandgap devices that switch at a higher voltage. In the following sections, from literature sources, several approaches to obtain the required negative voltage will be presented.

For low power applications where the total gate charge Q_g is limited, a charge pump may be used to generate the required negative bias. As shown in Figure 2.4, by switching the semiconductor devices in a defined sequence, energy can be transferred between the power supply and the storage capacitors so that it generates an inverted output. In detail, when S1 and S3 are turned-on, C_P will be charged to the supply voltage VCC. Then, S1 and S3 will be turned-off, and S2 and S4 turned-on. The positive side of C_P will be grounded via S2 so that C_r will be charged by C_P through S4 [2-17]. Initially, C_r is charged to half of the voltage storage on C_P but finally will be charged to –VCC in several cycles. The output source of a charge pump is

actually its output capacitor C_r, hence the restriction in using a charge pump is the limited current rating.

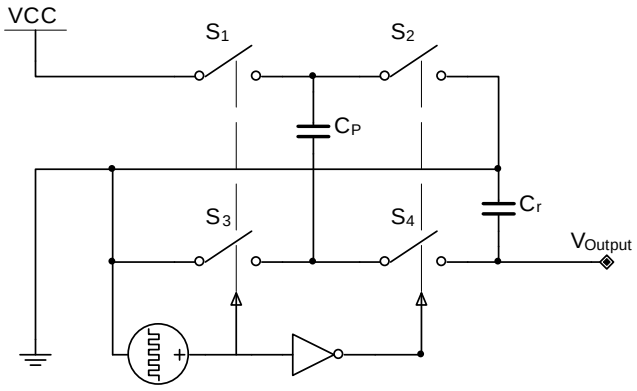

Figure 2.4. Simplified schematic of a charge pump with an inverted output.

For high power applications, i.e. driving MOSFETs with higher Q_g, DC-DC converters with an inverter configuration can be applied. A buck-boost converter is shown in Figure 2.5, when S1 is turned-on, energy will be stored in L_1. At the instant when S_1 is turned-off, D_1 forces the current keeps flowing its original way and charges C_{Output}. The main restriction when using a DC-DC converter for negative voltage generation is the physical space requirements and cost, as these converters normally consist of a dedicated controller and magnetic components. Based on a calculation done by TI Webench, a 5V to -5V inverting converter will occupy at least 346 mm^2 of PCB footprint. Furthermore, the electromagnetic interference (EMI) issues of an inverted buck-boost converter are worth considering since both its input and output are fluctuating.

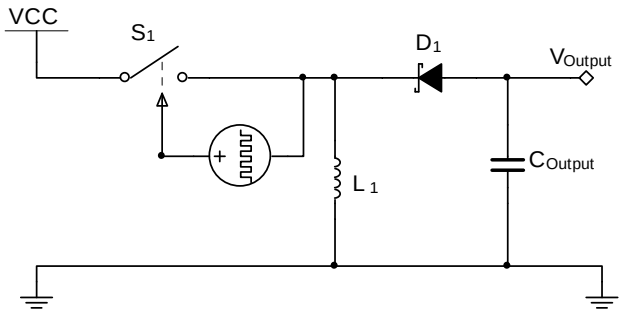

Figure 2.5. Simplified schematic for the non-isolated inverting converter.

Researchers have presented some approaches to generate a negative bias without using dedicated converter controllers or magnetic components [2-18]. This approach is shown in Figure 2.6; by using 8 additional MOSFETs, bipolar driving of a half-bridge is achieved. The circuit connected between the MOSFET and gate driver is a discrete charge pump that is driven by the gate driver's output and therefore, the physical size of this approach may be a disadvantage. Furthermore, by using an additional MOSFET pair, which ensures the MOSFET is turned off/on, the extended propagation delay and switching time will limit the maximum switching frequency of the converter [2-18].

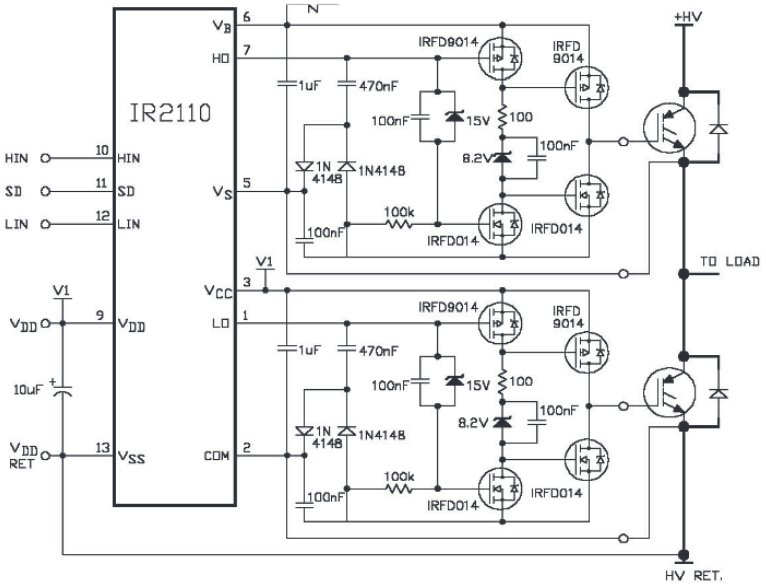

Figure 2.6. Half-bridge driver with negative bias generation [2-18].

2.2. Magnetic-coupled wireless power transfer

The modern wireless power system can be realised by using several methods such as lasers, microwaves or coupled fields [2-19]. The first generation of commercial wireless power systems utilised coupled inductance for low power wireless charging (i.e. mobile phone charging) [2-20], which is known to have a low power transfer efficiency with limited charging distance. Higher efficiency and extended distances can be realised by using Strongly Coupled Magnetic Resonance (SCMR) [2-21]. SCMR utilises the mutual inductance between the transmitting coil and receiving coils to transfer energies from several watts to kilowatts [2-22 and 2-23]. The SCMR in based on fundamental physics laws including [2-24]:

Ampere's Law: A magnetic field will be generated around a conductor which is carrying electric current.

Faraday's Law: A voltage will be generated in a coil which is located in an alternating magnetic field.

Tesla's Work: coupled magnetic resonance will cause electromagnetic power transfer across the air.

Two types of wireless power applications are generally considered: a stationary charge system allows a fast battery charge when the object stays at the desired location; an "On the fly" method provides the opportunity to power an object whilst it is moving [2-25]. In either case, the performance of a wireless power system is highly reliant on its power converter, transmitting and receiving coil design, coil relative position, and the frequency matching between the receiving resonator and output of the driving converter [2-26].

2.2.1. Circuit topologies

SCMR systems feature two resonators working as power transmitters and power receivers, which can be simplified and considered as two LC circuits. Utilising two simple LC circuits, there are four basic topologies

that can be constructed to implement a SCMR system, since each LC resonator can be parallel or series connected. A primary design objective of a wireless power system is to maximise its power transfer ability and efficiency. The design process needs to consider all the elements of the system from converter to coil design. The compensation of the inductance of transmission coil should be considered first since the extra capacitors will affect the circuit topology and control approaches [2-27]. The four possible topologies have been shown in Figure 2.7. Several approaches have been proposed to the component selection in order to optimize the circuit design:

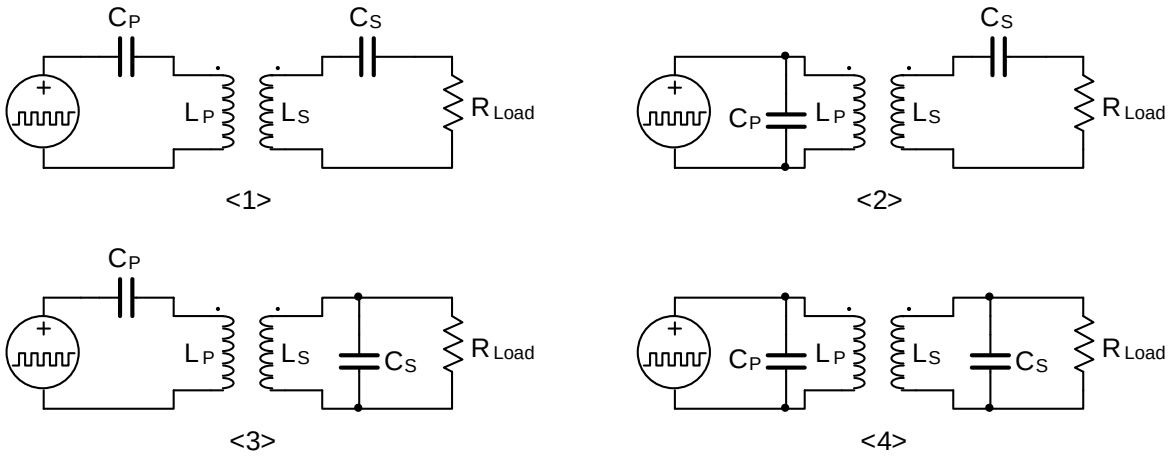

Figure 2.7. Four different compensation topologies for SCMR based design

Series connected primary side can be chosen for the variable load since the C_P (primary side resonant capacitor) located on the primary side will not be affected by the changing R_{Load} (represents the load) [2-28].

If the distance between two coils may vary, both series connected primary and series connected secondary are suggested, since both C_P and C_S (secondary side resonant capacitor) are independent of the magnetic coupling [2-29].

For a fixed load and magnetic coupling, the best topology for the secondary side can be chosen based on the load value and the inductance of the secondary coil [2-30].

For the detailed analysis and optimisation (i.e. the parasitic capacitance cannot be negligible) the parallel connected secondary side should be chosen since the parasitic parallel capacitance of the inductor can be added to C_S. [2-31].

In addition, other topologies and compensation networks like adaptive matching have been introduced in [2-32 and 2-33]. However, the series to series topology is popular because of its insensitivity to component and geometric tolerances [2-34].

2.2.2. Coil topology

The transmitter and receiver of an SCMR system can be considered as an electrical transformer [[2-35]. The structure of the Tx/Rx coil can be varied. In addition to the conventional circular coils, researchers [[2-36 and 2-37] also shown rectangular winding in their design. For simplicity and considering the applications discussed in this thesis, circular coils were chosen for this research.

2.2.3. Efficiency

Based on the series to series topology introduced above, shown in Figure 2.8, the efficiency of the targeted SCMR system can be calculated by the equation (1-2): [2-38]

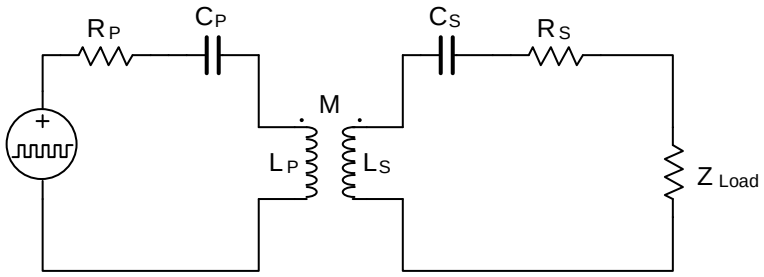

Figure 2.8. SCMR under analyses with double series capacitor connection

$$\eta = \frac{P_{load}}{P_{Trans}}$$

$$= \frac{R_{load}}{R_P\frac{(X_S+X_{load})^2+(R_S+R_{load})^2}{\omega^2M^2}+(R_S+R_{load})} \qquad (2-2)$$

Where the $X_S = \omega L_S - \frac{1}{\omega C_S}$ and $Z_{load} = R_{load} + jX_{load}$.

2.2.4. Power capability

Moving away from an ideal coupling model, a practical system includes both the transmission coupling and the power converter, and therefore requires the inclusion of the source impendence Z_S. For a given Z_S, the maximum power capability can then be calculated by using the following equation:

$$P_{load} = \frac{R_{load}}{2} \frac{|Es|^2}{|\frac{(Z_S + Z_1)(Z_2 + Z_{load})}{\omega M} + \omega M|} \quad (2-3)$$

For a purely resistive power source and load, which approximates to $X_{load}=X_S=0$, and perfectly resonant coils set, the equation illustrated above can be further simplified, and is suitable for most situations.

$$P_{load} = \frac{R_{load}}{2} \frac{|Es|^2}{|\frac{R_S R_{load}}{\omega M} + \omega M|} \quad (2-4)$$

2.2.5. Power converter requirement

An SCMR system can be operated over a wide range of frequencies, with higher frequencies offering greater power transmission and longer distances. However, the frequency will be limited by the power converter and existing radio frequency regulations. Hence, to achieve the desired power rating, optimisation of the operating frequency according to the coil inductance should be prioritized, where the relationship between the maximum power transfer and the coil inductance has been shown by researcher [2-38] in Figure 2.9.

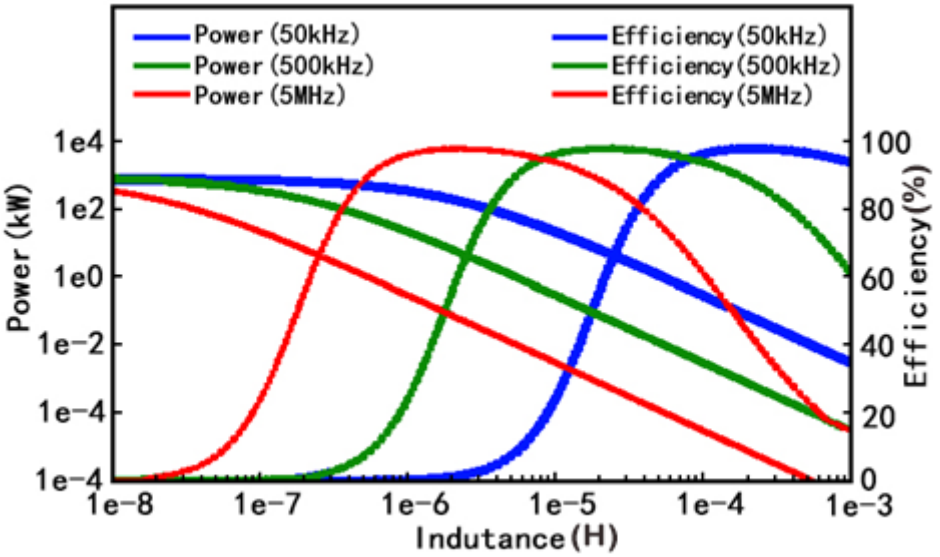

Figure 2.9. Maximum load power rating versus the inductances of the coils [2-38].

Current studies show that a low-frequency system (between 10 kHz to 500 kHz) could deliver kilowatts of power, with efficiencies greater than 70 percent [2-39 to 2-42]. The low frequency leads to lower switching losses and a reduced cost of the power converter stage. There are two kinds of power converters are typically used for WPT systems, two-stage AD-DC-AC converter and direct AC-AC matrix converter.

2.3. Two Stage Variable Duty-cycle Variable Frequency (VDVF) converter

To drive the transmitting coil of a wireless power system, a Variable Duty-cycle Variable Frequency (VDVF) converter should be implemented. The sinusoidal voltage required by the transmitting coil can be achieved by using Sinusoidal Pulse Width Modulation (SPWM) technology or load resonant conversion. Since the switching frequency of an SPWM converter will be several times higher than its output frequency, a load resonant converter is often chosen in order to achieve a higher output frequency and reduce switching losses.

More recently, load resonant converter topologies have been implemented and these topologies

can be divided into two groups. Firstly, a two-stage AC-DC-AC converter usually consists of a rectifier and a DC-AC inverter, with some internal energy storage components. Secondly, a single stage AC to AC converter that converts mains AC power into another AC power source with a defined voltage and frequency directly, and features bi-directional switches.

2.3.1. Voltage source back to back resonant converter

In general, two stage converters contain a rectification stage and an inversion stage. The rectification stage converts the mains AC power into DC, and after being buffered and filtered by an energy storage capacitor, the DC voltage is chopped by a full-bridge with a set frequency.

2.3.1.1. Theory of operation

The two-stage resonant converter, which features an intermediate DC link, was reported in 1986 [2-43]. As can be seen from Figure 2.10, in addition to the optional Power Factor Correction (PFC) stage, the two-stage converter typically consists of a full-bridge inversion stage and a diode-based rectification stage, which may cause discontinuous input current and unwanted harmonic pollution on the utility supply. The grid power will be rectified to a fluctuating DC voltage and filtered by a capacitor or LC filter, which also decouples the input from the output [2-44]. The widely-used LC filter for a DC link consists of limited inductance but a large capacitance so that the loss across the inductor can be minimised. After filtering, an H-bridge inverter at the output generates an AC output with the desired frequency and/or duty cycle. When applied to a resonant load with the self-resonant frequency similar to the frequency of the pulse output, sinusoidal current will flow through the load.

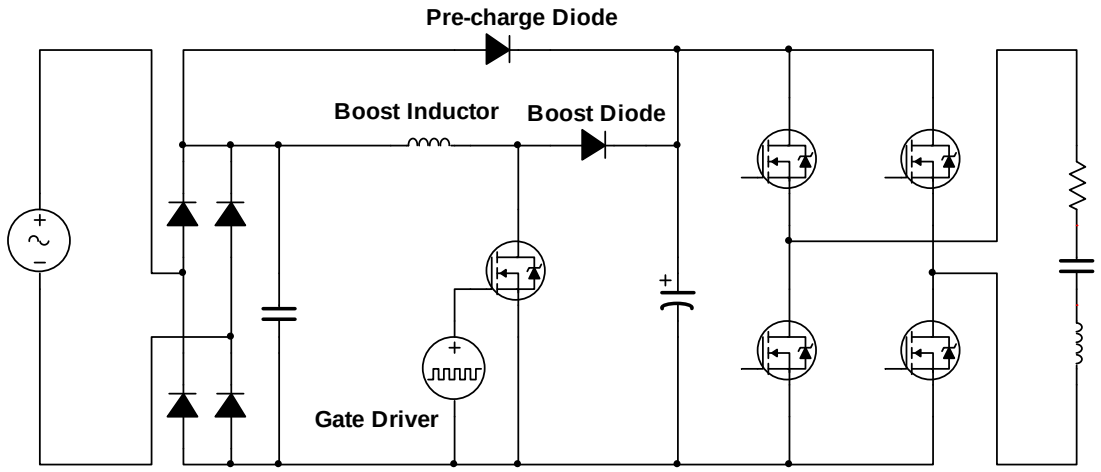

Figure 2.10. Block schematic for a typical AC-DC-AC converter with Continuous Conduction Mode (CCM) Power Factor Correction

Generally, the VDVF resonant converter can be controlled by implementing one of many modulation approaches. Pulse Width Modulation (PWM) and Pulse Density Modulation (PDM), which control the output duty cycle without affecting the output frequency, are suitable control candidates for WPT systems. PDM modulation has the advantage of an expanded soft switching range [2-41], however, the output frequency of a PDM modulated converter will be limited by its multiple switching operations. Furthermore, soft switching techniques such as Zero Voltage Switching (ZVS) have been introduced, these are widely employed in these circuits to lower switching losses and increase system efficiency [2-45 and 2-46].

2.3.2. Matrix converter

Traditionally, the power converter for a WPT system was formed by two-stage AC-DC-AC converters as described above. The input rectification stage is typically formed from diodes or thyristors, and may cause harmonic pollution onto the utility supply, due to the discontinuous input current [2-47, 2-48]. As a solution to this, Power Factor Correction (PFC) technologies have been widely-used [2-47]. However, the PFC circuit will not only introduce additional losses and costs but will also impact on the system's bidirectional performance [2-45]. Furthermore, most AC-DC-AC converters utilise a capacitor-based DC-link for energy storage and filtering [49]. For applications with renewable sources or energy storage, multistage converters (with DC links) have the advantage of direct interfacing to DC sources via the DC link [2-49 and 2-50]. However, the capacitors used on the DC link may be bulky and affect overall system lifetime, reduce power density and affect efficiency and reliability [2-51].

2.3.2.1. Advantage of using a matrix converter

The disadvantages of multistage converters can be resolved by the application of a force-commutated matrix converter [2-44]. The input to a matrix converter is an AC source and it can produce a different AC output with arbitrary frequency and magnitude [2-52]. According to work presented by [2-44 and 2-53 to 2-57], the matrix converter offers the following advantages.

a) Allows for a greater differential between input and output voltage

b) Low Total Harmonic Distortion (THD)

c) Flexible phase control between current and voltage

d) No intermediate energy storage components

e) Four quadrant operation

f) Suitable for harsh environments.

Additionally, [2-58 and 2-59] show the conduction losses of matrix converter are typically lower than the conventional back to back converter. Furthermore, based on the marketing analysis provided by Yaskawa, the matrix converter meets the requirements for many applications and is further desirable due to its bi-directional energy flow [2-60]. Research also shows the matrix converter has a better performance for high power and high voltage application [2-61], which has great potential in the converters' market [2-62].

The matrix converter can be further divided into direct matrix converters and indirect matrix converters (as shown in Figure 2.11 (a) and (b) respectively), both of which have the functionality to convert voltage and frequency simultaneously [2-44]. The direct matrix converter was firstly introduced by Venturini and Alesina in 1980 and its performance confirmed by Rodriguez and Kastner in 1985 [2-42 and 2-63]. Since the indirect matrix converter is similar to the voltage source back to back converter [2-60], direct matrix converters are the ones mainly considered here. Additionally, most commercially produced matrix converters are based on direct converter topologies [2-60].

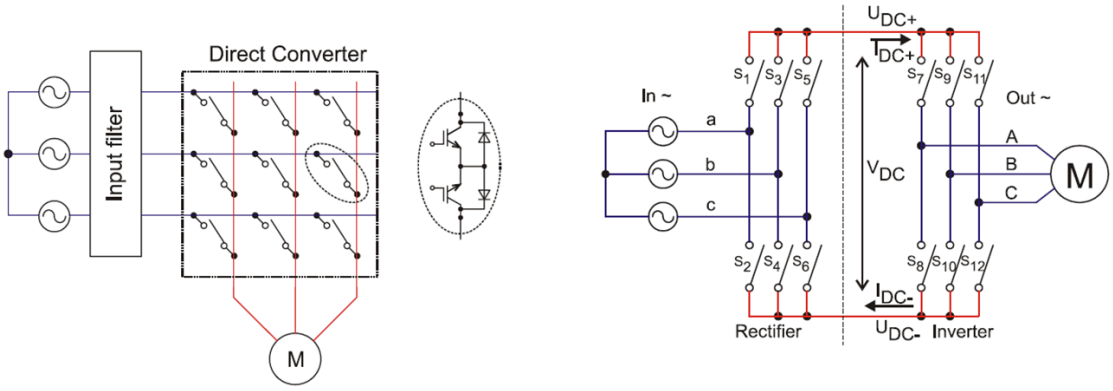

Figure 2.11. (a) Direct matrix converter (b) Indirect virtual DC-link matrix converter [2-64].

Although many detailed studies of matrix converters have already been carried out [2-65 to 2-67], the control of a matrix converter still requires hardware that can implement very fast, low latency control. The requirements for control are typically realised by Digital Signal Processors (DSPs) together with Field Programmable Gate Arrays (FPGAs) [2-68 and 2-69]. These expensive controllers limit the application of matrix converter based WPT devices, particularly for consumer products where cost and size are often critical.

2.3.2.2. Bi-directional switch

The power switches utilised in matrix converters require bi-directional conducting and blocking capability [2-70]. Several switch topologies have been introduced that offer these features, with Figure 2.12 showing a single transistor based bi-directional switch. Easy control can be considered as its main advantage, since the single transistor requires only one isolated power supply and gate driver [2-71]. However, the conduction losses and voltage drops of this topology are significant since three semiconductors will be connected in series in each direction of conduction [2-70]. Furthermore, the current path of this topology cannot be controlled, which limits the commutation techniques that can be implemented in the converter [2-71].

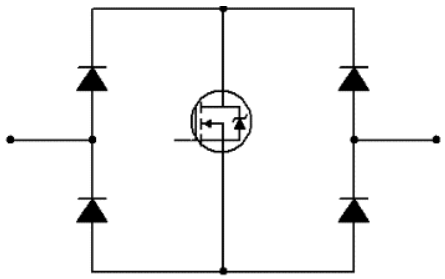

Figure 2.12. Single MOSFET based bi-directional switch

Figure 2.13 (left) illustrates a bi-directional switching cell formed by Reverse Blocking IGBTs (RBIGBTs). Compared with Figure 2.12, the RBIGBT solution offers more than 70 percent conduction loss reduction [2-72]. However, the disadvantages are higher switching losses and limited switching frequency [2-70].

With the demands of reducing switching losses, [2-73 and 2-74] provide an improved switching cell topology, which is shown in the Figure 2.13 (right). However, the switching frequency of the IGBTs is still limited, which may not able be to provide an adequate frequency for the WPT application.

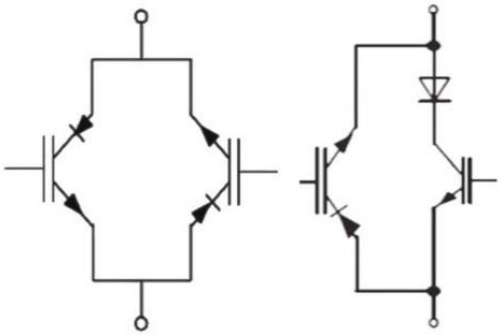

Figure 2.13. RBIGBT based bi-directional switches.

The topologies shown in Figure 2.14 consist of two devices. The switching device provides the forward conduction path and the parasitic diode provides reverse conduction ability in each device [2-71]. Independent control of the direction of current can be realised by using those topologies. In addition to conventional MOSFETs (shown in Figure 2.14), SiC FET, JFET and GaN can also be used, these provide the advantages of fast-switching and lossless operation [2-75 and 2-76]. However, JFET solutions are still limited by their cost performance, and SiC solutions suffer from the robustness issues caused by gate oxides [2-77].

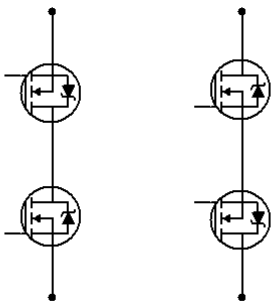

Figure 2.14. MOSFET based bi-directional switch

2.3.2.3. Bi-Directional Switch Driver

The simplified drive circuit of a bi-directional switch is shown in Figure 2.15. Negative voltage swing is incorporated, to avoid inadvertent turn on. Also, due to the high frequency of the WPT system; low propagation delay signal isolators are used.

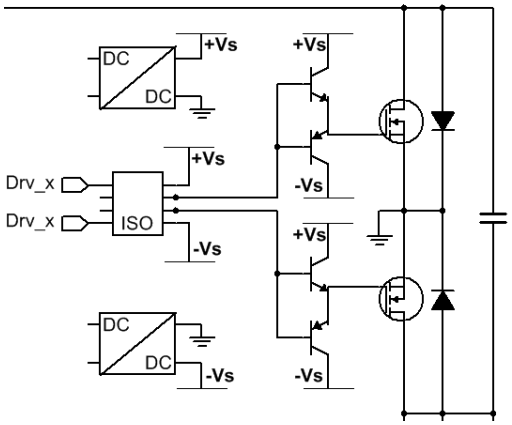

Figure 2.15: Simplified drive circuit of a bi-directional switch

Additionally, to drive JFET based power switches, a +20V and -5 bipolar power supply is required [2-78]. However, for some SiC devices that are normally-on, the establishment time of the isolated power supply needs careful design, as this may cause an inadvertent short-circuit during power up if the supply takes too long to stabilise. Researchers have introduced several approaches to prevent the power-on failure, such as very fast power supplies [2-79], constant negative voltage [2-80], redundant turn-off circuits [2-80] and self-powered driver circuits [2-81].

2.3.2.4. Input filter of a matrix converter

Although the matrix converter provides the “all-silicon” solution to realise power conversion without intermediate energy storage components, the modulation of the matrix converter will inject high order harmonics into the grid, this requires extra circuitry to be filtered out [2-82]. The researchers in [2-83] describe a differential EMC filter and [2-84] introduce a small dc-link based filter for indirect matrix converter, however LC filters are still conventionally selected due

to simplicity and cost-efficiency. Based on [2-70 and 2-85] and the discussions therein, the filter design should comply with the following requirements:

- Maintain high power factor.
- Low Electromagnetic Interference (EMI).
- Provide sufficient voltage to the switch matrix.
- Minimal voltage drop across the LC filter.
- Minimal loss over the damping resistor.

To determine the harmonics injected into the grid, [2-86] presents an analytical method for the input current of a matrix converter based on its modulation. [2-75] describes a complex Fourier transform based approach to analyse the input current harmonics, whilst [2-76] provides a simulation module based current ripple estimation methodology. Furthermore, a design of multi-stage LC filter with different constraints has been illustrated by [2-87].

A step-by-step procedure is provided in [2-88] to design an LC filter for matrix converter. The design transforms a direct converter into an in-direct converter and then designs an LC filter for this in-direct converter. The design starts with the calculation and determination of several basic parameters:

- The ratio between the fundamental component of the input current and the average current over the virtual DC-link (M_I);
- The ratio between the fundamental component of the output voltage and the average voltage over the virtual DC-link (M_V);
- Load impedance ($|Z_L|=V_O/I_O$) and the power factor angle of the load ϕ_O .

Then from the filter's point of view, the effective resistance of the desired matrix converter can be calculated as R_E

$$\mathrm{R}_E = \frac{V_{in}}{I_{in}} = \frac{|Z_L|}{2.25(M_I^2 M_V^2)\cos(\varphi_o)} \qquad (2-5)$$

Where $V_{in}\ and\ I_{in}$ represent the Input voltage and input current respectively. So that the input RMS current can be obtained as a function of load power factor as follows:

$$I_{RMS}^2 = 0.5365 M_I M_V I_O^2 (0.828 + 0.828 cos2\varphi_o + 0.154 sin2\varphi_o) \qquad (2-6)$$

Where I_O is the output current. Then the RMS switching current can be calculated by removing the fundamental component from the I_{RMS} as shown below:

$$I_{RMS\_SW}^2 = I_{RMS}^2 - (1.1 M_I M_V I_O cos\varphi_0)^2 \qquad (2-7)$$

After determining the maximum ripple level on both input current and input voltage together with the maximum power loss, the inductor, capacitor and damping resistor for the targeted filter can be obtained by solving equation set introduced in [2-88]. Also, the grid side switching current I_{gRMS_SW} should be controlled in order to maintain the THD requirement on the grid which is listed in IEEE519 [2-77].

$$I_{gRMS\_SW} = \frac{I_{inRMS\_SW}}{\sqrt{1 + \frac{(1-\omega_S^2 LC)^2 - 1}{(1 + \frac{\omega_S^2 L^2}{R_d^2})}}} \qquad (2-8)$$

$$V_{inRMS\_SW} = \frac{I_{inRMS\_SW}}{\sqrt{\left(\omega_S C - \frac{1}{\omega_S L}\right)^2 + \frac{1}{R_d^2}}} \qquad (2-9)$$

$$\frac{P_{loss}}{P} = \frac{I_{gRMS}}{V_{gRMS}} \left(\frac{\omega_g^2 L^2 R_d}{\omega_a^2 L^2 + R_d^2}\right) \qquad (2-10)$$

Where ω_S is the switching frequency, ω_g is the mains power frequency.

2.4. Summary

In this chapter, the background and presented research for this thesis have been provided. The first section of this chapter described the methodology and design of conventional gate drivers and analysed their inadequacies. To achieve an effective gate driving that equipped with simplicity and cost-efficiency, a novel gate drive topology with self-driven negative bias will be discussed in chapter 3. This chapter also describes the fundamental knowledgebase of how to achieve magnetic-coupled wireless power transfer, including different circuit topologies and basic calculations. In the last section of this chapter, the two-stage VDVF converter has also been discussed, which will be used to discover the approach of how to modify the control of such VDVF converter so that single stage direct matrix converter can be controlled using a controller designed for VDVF converter.

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3. Non-isolated gate driver with self-driven negative bias generator

3.1. Introduction

A WPT system requires the transmission resonator to be driven by a fixed frequency square or trapezoidal waveform from a power converter. It has been discussed in Chapter 2 that the converter specification is fundamental to the reliable and efficient operation of a WPT system. This thesis introduces a number of novel enhancements to the converter and its control. In this chapter a conventional converter is considered to introduce a novel self-driven negative bias generator that can also be applied to other converters types. As discussed in the chapter 2, a semiconductor based high frequency converter may suffer from the miss-triggering faults caused by high dV/dt. As discussed in Chapter 2, a semiconductor based high frequency converter may suffer from the miss-triggering fault caused by high dV/dt. A bipolar gate driver generally solves the miss-triggering issue but conventional solutions require additional power supplies to provide the negative voltage. The novel gate driver integrated with self-driven negative bias generator presented in this chapter can provide bipolar gate driving capability without the need for a separate negative voltage supply.

This chapter describes the novel self-driven negative bias generator applied to a conventional half or full-bridge gate driver and used in a reference design converter for analysis. Starting with the design of the topology, with its specifications shown in Table 2.1, the theory of component selection for the power electronics and control, will be introduced. Simulation and experimental results of the prototype, are then presented, along with detailed analysis into the output waveform, start-up performance and comparisons between component selections.

Table 2.1. Specifications of the full-bridge converter based wireless power converter

Working frequency		20-2000 kHz
Power rating		300W
Gate driving	Turn On	+15V
	Turn Off	-5V
Control sensor	Current	Low side 0.01Ω shunt resistor
	Voltage	11:1 voltage divider
Protections	Over voltage (transient)	Transient Voltage Suppression (TVS) diode
	Over voltage (long term)	Gas Discharge Tube (GDT) and Varistor (MOV) blow the fuse
	Over current (soft)	MCU controlled
	Over current (hard)	Fuses
	Input reverse	Forward biasing the TVS
	Output over current	MCU controlled

3.2. Bipolar gate driving using conventional gate driver

As described in Chapter 2, in the transient of a turn-on and turn-off of a FET, a mistrigger could occur since there is a large voltage change across the power switch (high dV/dt). To avoid using gate overdrive and high V_{gs} FETs and IGBTs, which may prevent the miss-triggering issue, it is good practice to use a negative voltage to turn-off the FETs and IGBTs for medium to high power converters, especially for wideband gap materials such as SiC or GaN power devices. To supply the required negative voltage, an additional DC-DC power supply (or isolated DC-DC power supply for an isolated driver) is customary, as shown in Figure 3.1. These additional power supplies are undesirable in terms of footprint and additional cost, and suffer from limited lifetime due to utilising electrolytic capacitors.

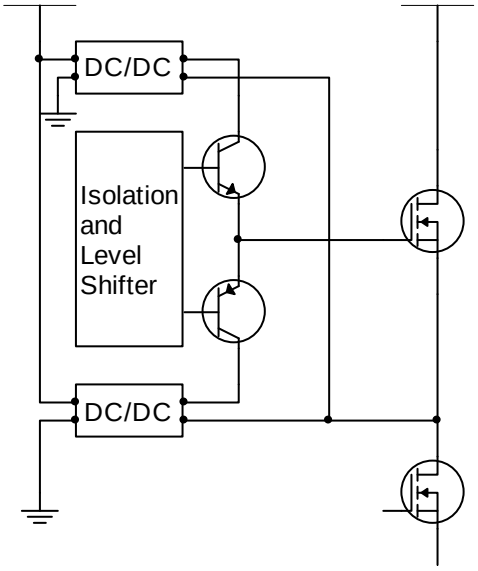


Figure 3.1. The conventional approach to achieve bipolar driving.

For a widely-used non-isolated full-bridge drive, a boost driver is widely used to generate the high voltage required for high-side MOSFET driving, which normally consists of a boost diode and boost capacitor as shown in Figure 3.2. The boost capacitor will be charged during the low-side MOSFET being turned-on, ensuring that the boost capacitor can charge the Gate of high-side MOSFET when the low-side FET is turned-off.

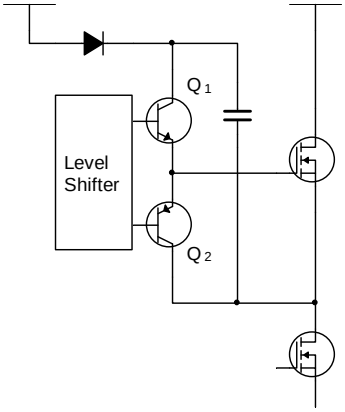


Figure 3.2. Boosted approach for high side driving.

From Figure 3.2 it can be seen that while the high side MOSFET is being turned-off, Q_2 will pull together its Gate terminal to its Sink terminal, resulting in 0 V across its Drain and Source terminal. The boost circuit replaces the DC-DC supply that provides the positive bias. However, it is still required to have a separate power supply to provide a negative bias.

3.3. Self-driven negative bias generation in high-side-only application

The schematic of the proposed novel gate driver is shown in Figure 3.3. Compared with the conventional boosted driver, only six components: C2, D2, R1, R2, R3, Q3 are added.

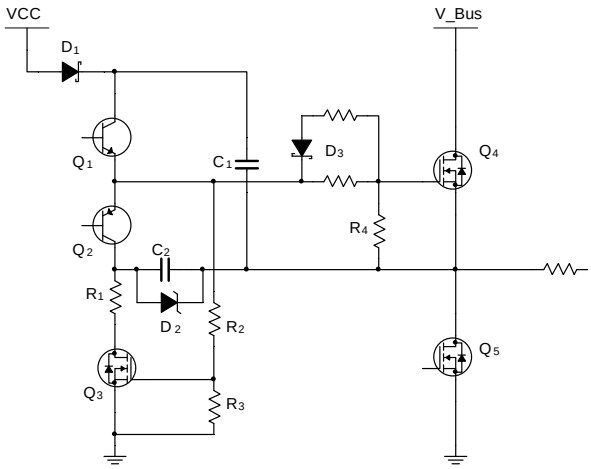


Figure 3.3. Schematic of the proposed bipolar gate driver.

Based on the schematic shown in Figure 3.3, the operating sequences are now described, where 'Sx' denotes the sequence number.

S0, before Q_4 is turned-on and whilst Q_5 is turned-on: C_1 is charged by VCC through D_1 so that the energy used to turn on Q_4 is stored in C_1. The voltage on C_1 can be approximated as VCC – V_{FD} where V_{FD} is the forward voltage drop of D_1 when the switching period of the full-bridge is lower than T_p given as:

$$T_p = 5(R_{DS} + \Delta R_{DS} \times T) \times C_1 \qquad (3-1)$$

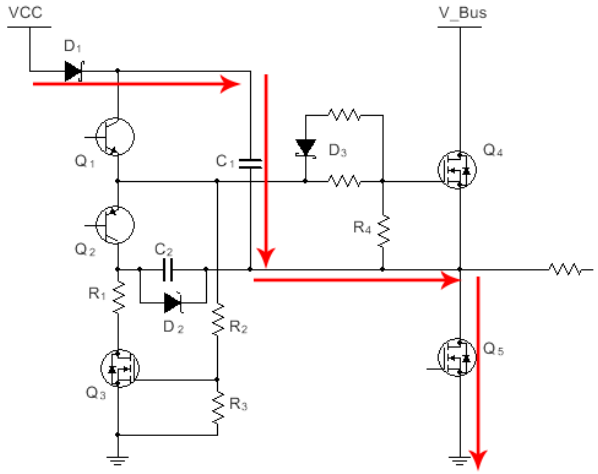


Figure 3.4. Simplified schematic of the proposed bipolar gate driver, stage 0.

S1, when Q_1 is turned-on and Q_5 is turned-off: C_1 will be discharged through Q_1, and the energy stored in C_1 will be applied to the Gate terminal of Q_4. Since C_1 is referenced to the sink terminal of Q_4, a voltage equal to VCC will be applied across the gate and sink terminal of Q_4, Q_4 is turned-on and similarly, Q_3 is turned-on. Since the voltage used to drive Q_4 (approximately V_Bus+VCC) is normally higher than the maximum V_{GS} voltage, a voltage divider consisting of R_2 and R_3 is used to provide a drive voltage for Q_3. The resistance of R_2 and R_3 can be calculated by using the following equation, where V_{th} is the voltage desired for drive Q_3.

$$R_2 = \frac{(VCC + V_{bus} - V_{th}) \times R_3}{V_{th}} \qquad (3-2)$$

Meanwhile, when Q_4 and Q_3 are turned-on, V_Bus will be applied to the series connected C_2 and

R_1; C_2 will therefore be charged. Whilst C_2 is being charged, R_1 limits the current flow through Q_3 and C_2 to avoid a surge current and protect the Zener diode. The voltage rating of Q_3 should be higher than V_Bus-V_{D2}. The voltage across C_2 is set by the Zener diode D_2; the voltage across C_2 will rise to the reverse breakdown threshold voltage of D_2, the Zener diode will be broken down and C_2 will stop charging with a voltage across it of $-V_{D2}$.

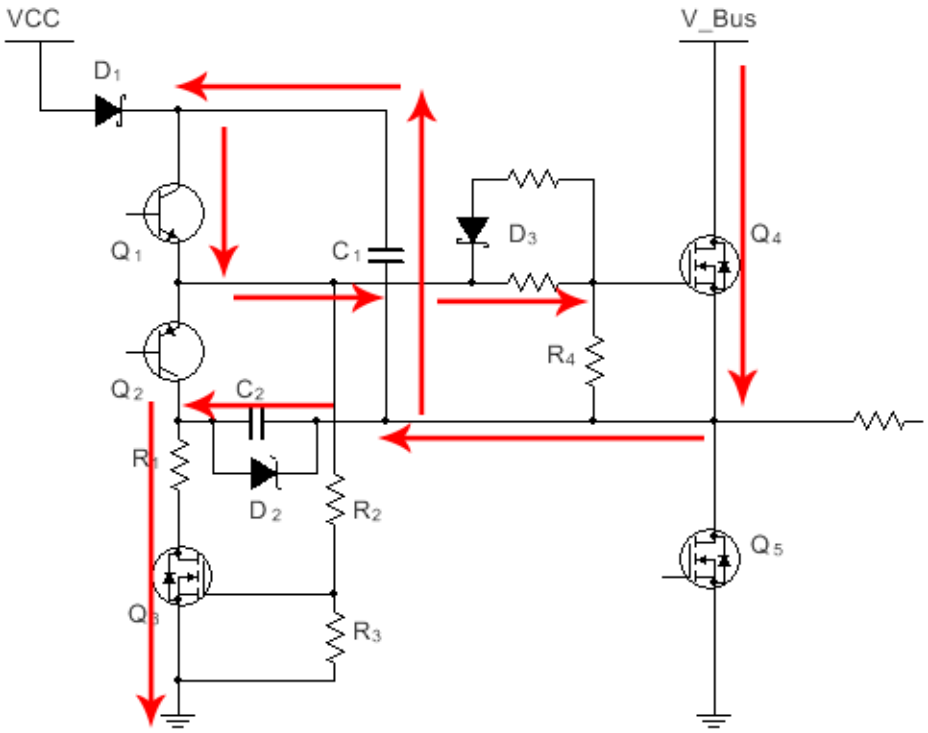


Figure 3.5. Simplified schematic of the proposed bipolar gate driver, stage 1.

S2, dead-time, while Q_2 is turned-on: C_2 will be discharged through Q_2. Since the positive side of C_2 is connected to the sink terminal of Q_4, a negative voltage will be applied to the Gate terminal of Q_4. The gate charge on Q_4 is therefore depleted through the gate resistors and D_3. As the capacitance of C_2 is much higher than the gate capacitance of Q_4, the negative voltage is maintained on the gate of Q_4 to ensure a solid turn-off.

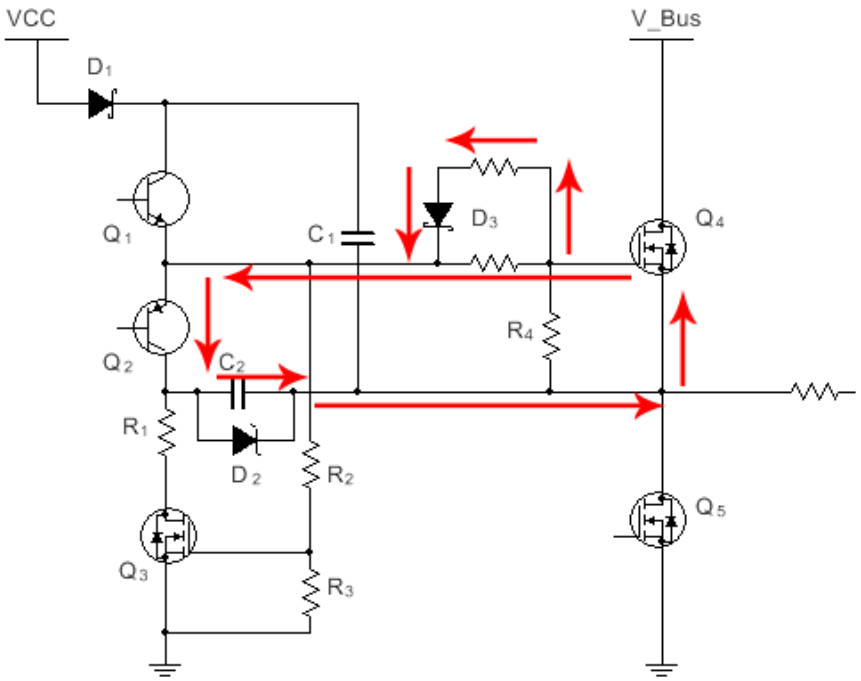


Figure 3.6. Simplified schematic of the proposed bipolar gate driver, stage 2.

S3, when Q_4 remains off and Q_5 is turned-on: C_2 will maintain a negative voltage onto the gate of Q_4, and C_1 will be charged through D_1.

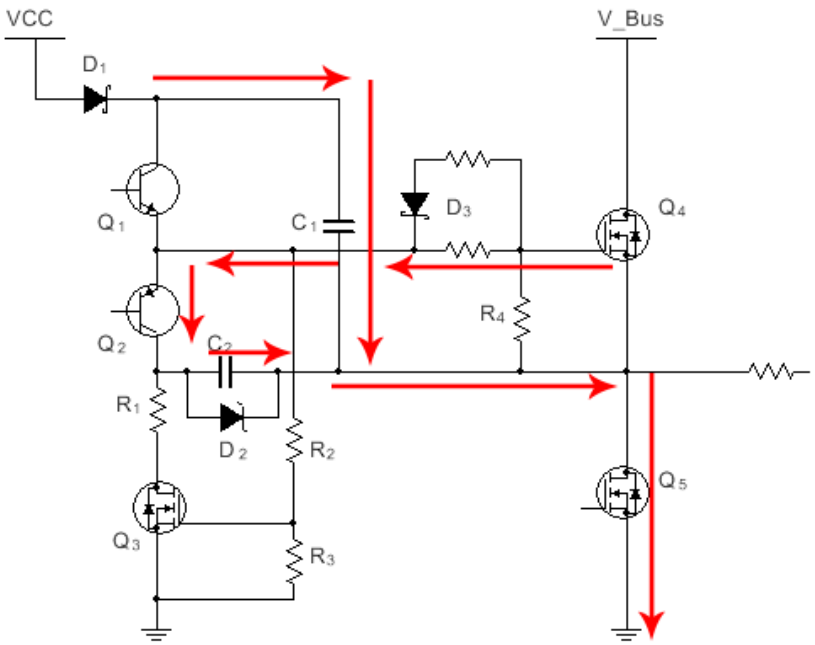


Figure 3.7. Simplified schematic of the proposed bipolar gate driver, stage 3.

S4, dead-time, Q_4 remains off and Q_5 turned-off: C_2 maintains a negative voltage onto the gate of Q_4 but C_1 is now fully charged and ready to turn Q_4 on.

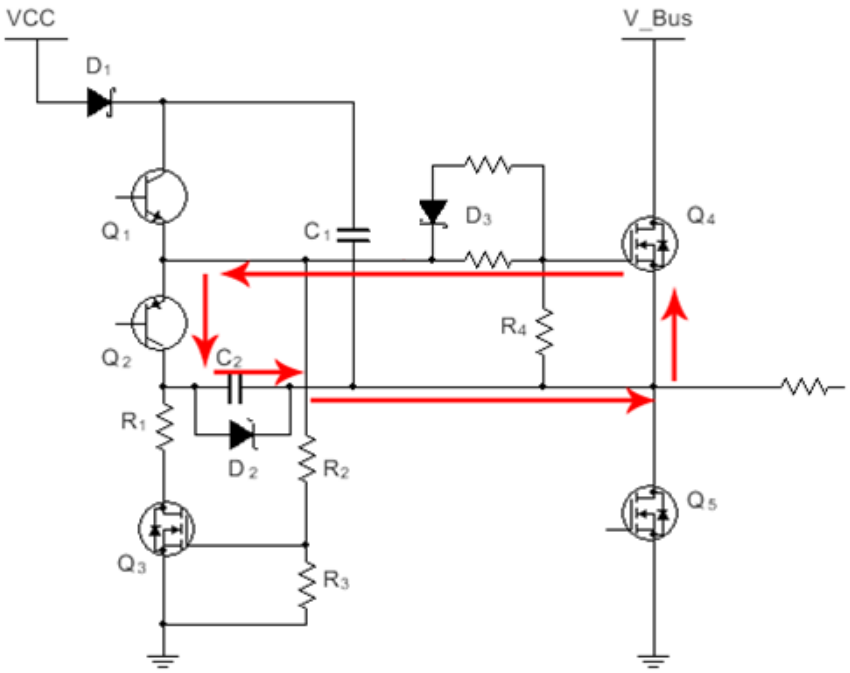


Figure 3.8. Simplified schematic of the proposed bipolar gate driver, stage 4.

As can be seen from the sequence of operation, C_1 acts as the positive power source and C_2 acts as the negative power source. When C_1 discharges to turn Q_4 on, C_2 will be charged. Whereas during C_2 discharges to turn Q_4 off, C_1 will be charged. Since the power source that charges C_2 is V_Bus, the additional negative bias generator will not consume power from VCC, hence the output capability of the power supply, providing VCC, is unaffected and the power drawn from V_Bus is negligible.

3.4. Negative bias for both high side and low side driving

In the design of high power converters either half-bridge or full-bridge topologies are desired. By using the technique introduced above, a self-driven negative bias generator can be expanded to full-bridge or half-bridge application. In this section, the theory of operation will be described, with current flows related to the turn-on operation coloured in red, and current flow related to

turn-off operation coloured in green.

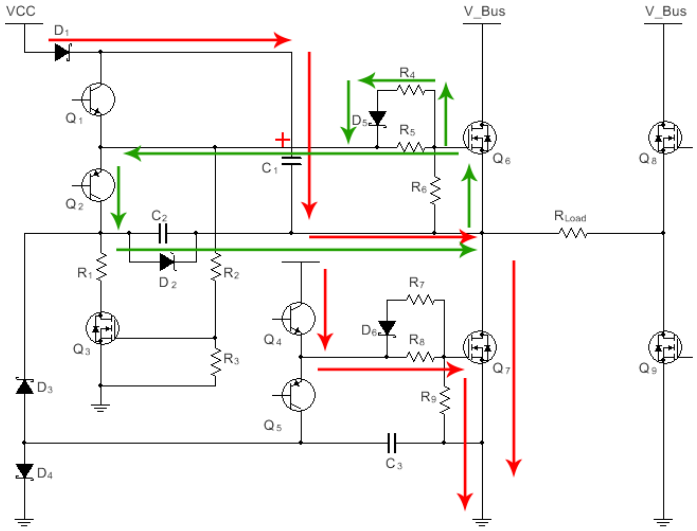


Figure 3.9. Simplified schematic of the negative bias generator for bridged converter, S0.

S0, low side on: The drive sequence starts by the turn on of the low side MOSFET Q_7, as shown in Figure 3.9. When Q_4 is switched on, the low side MOSFET Q_7 will be turned-on, creating a path from VCC to charge C_1. Meanwhile, Q_2 is switched on to turn Q_6 off, the Zener diode D_2 may be forward biased depending on the charged stored on the gate of the high side MOSFET Q_6.

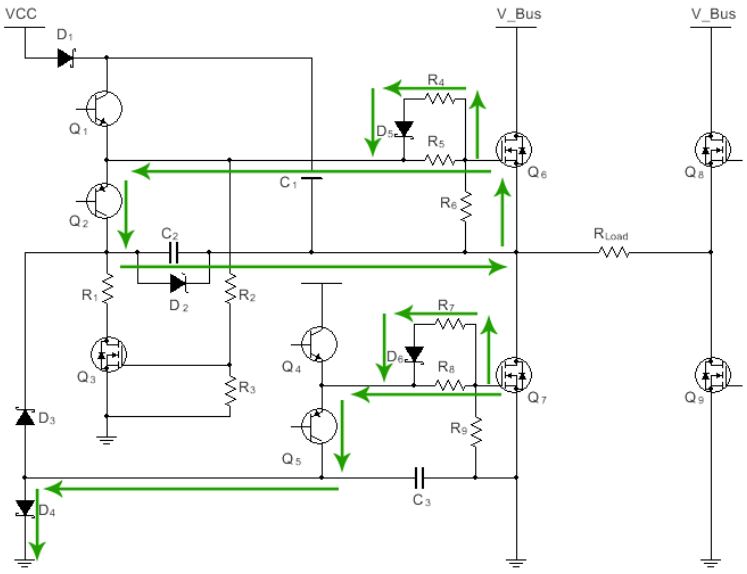


Figure 3.10. Simplified schematic of the negative bias generator for bridged converter, S1.

S1, dead-time: Q_7 will be turned-off by switch on of Q_5, where Q_6 maintains its previous state. Since there is no charge stored in C_3, Schottky diode D_4 may be forward biased depending on the charge stored on the gate of the low side MOSFET Q_7. This will keep Vgs applied on Q_7 lower or equal to the forward voltage of D_4, of approximately 0.35-0.5 V.

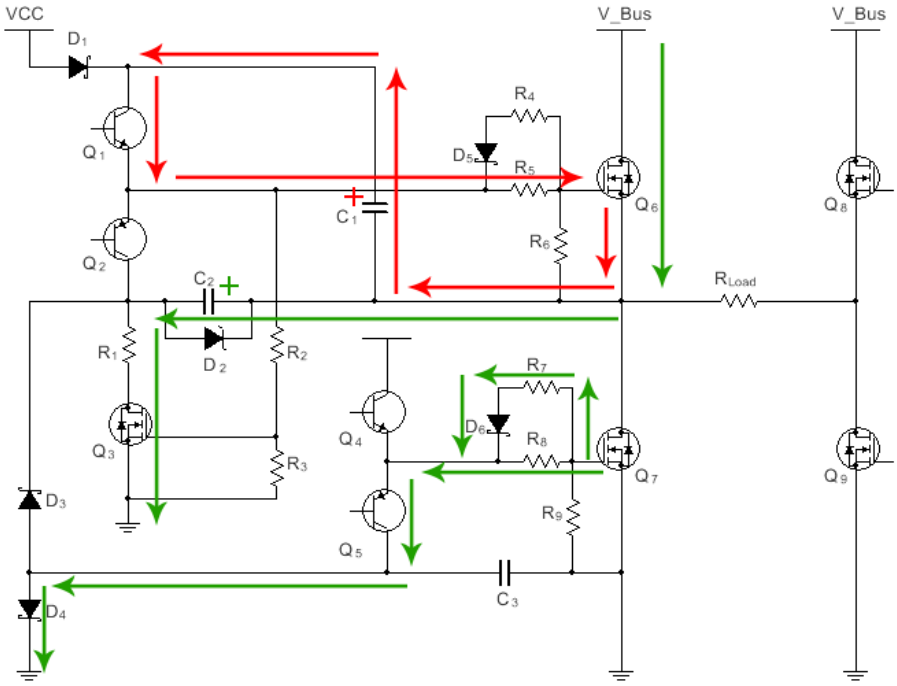


Figure 3.11. Simplified schematic of the negative bias generator for bridged converter, S2.

S2, high side on: As shown in Figure 3.11, Q_6 will be turned-on by switch on of Q_1, where Q_7 maintains its previous state. When Q_1 is switched on, Schottky diode D_1 will be reverse biased and therefore the gate of Q_6 is held high by the discharging of C_1. Meanwhile, a small amount of current sourced by V_Bus will flow from Q_6 to Q_3 and charge C_2. Since a Zener diode is connected in parallel with C_2, C_2 will charge to the Zener voltage of D_2. The value of R_1 is calculated by the power rating of D_2 at a worst case duty cycle (assumed as 100%, where Q_3 and Q_6 keep conducting) and the start instant of charging C_2 (where all current flows through the reverse biased D_2). A lower value of R_1 will introduce more losses but is desired at higher frequency or lower duty cycle, as a higher value of R_1 may cause insufficient negative bias.

$$R_1 = \frac{V_{Bus} - I_{load} * R_{DS_{On\,Q6}} - I_{D2\,MAX} * R_{DS_{On\,Q3}} - V_{D2}}{I_{D2\,MAX}} \qquad (3-3)$$

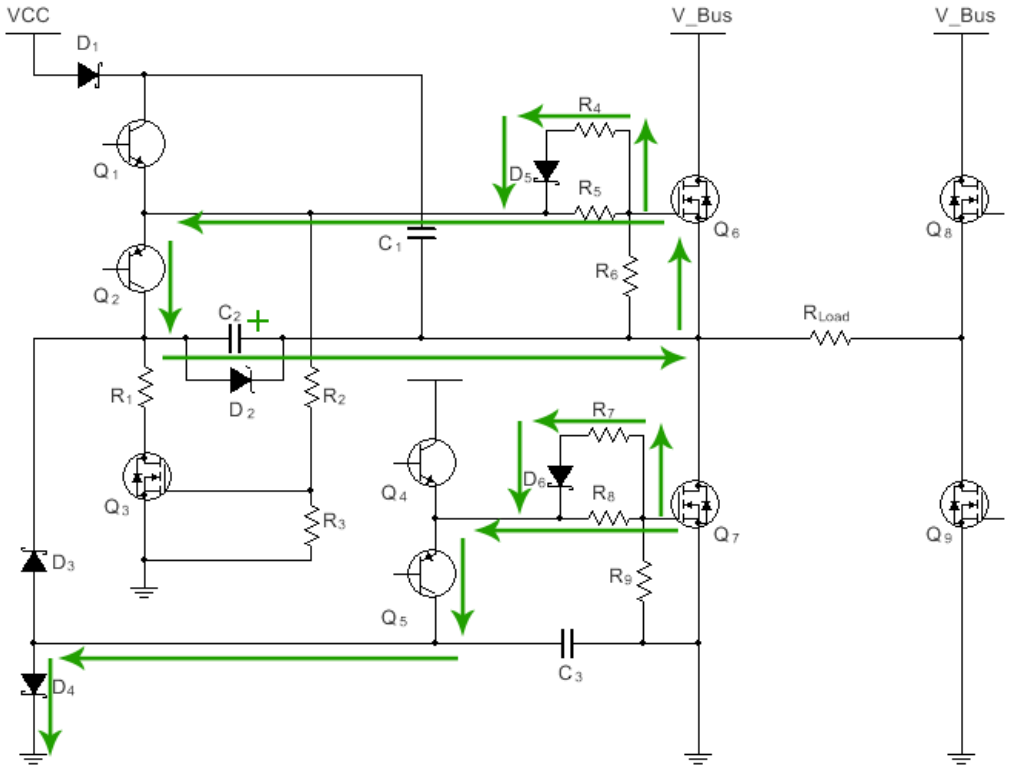


Figure 3.12. Simplified schematic of the negative bias generator for bridged converter, S3.

S3, dead-time: Q_6 will be turned-off by switch on of Q_2, and Q_7 remains at its previous state. As C_2 was charged in S2, during this second dead-time, the gate of Q_6 will be negatively biased by the discharging of C_2. Hence, the minimum value of C_2 should be several times higher than the gate capacitance, the calculation of C_2 will be illustrated in later steps, since the charge stored in C_2 will not only power Q_6 with negative bias but also charge C_3.

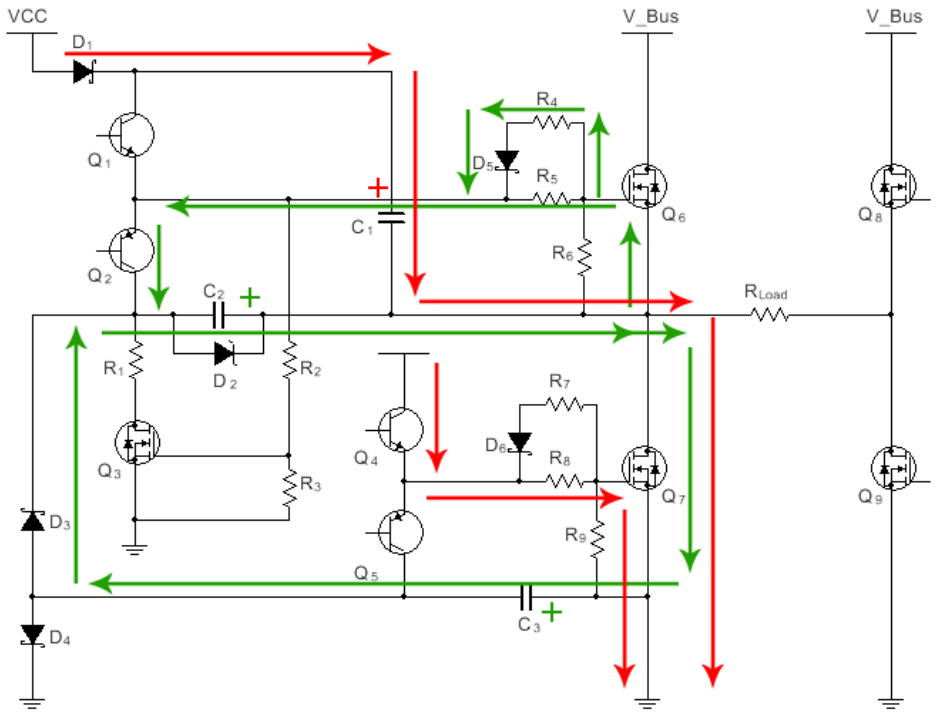


Figure 3.13. Simplified schematic of the negative bias generator for bridged converter, S4.

S4, low side on: Q_4 is switched on and causing Q_7 to be turned-on, whilst C_2 maintains a negative bias on the gate of Q_6. As illustrated in S1, C_1 will be charged by the current path created though Q_7 and D_1. Meanwhile, C_3 will also be charged through the discharge of C_2. Taking the ground as a reference point, the voltage on the collector of Q_2 will be several volts below ground, this forward biases D_3 and creates a current path through Q_7 to charge C_3. The actual voltage on C_3 in a non-phase-shifted converter that can be approximated as:

$$V_{C3} = \frac{C2 * \left(V_{D2} * \frac{C2}{C2 + C_{Gate6}} - I_{Load} * R_{DS}\right) * \left(1 - e^{-\frac{F}{R_{DS} * C2 * D}}\right)}{C2 + C3} \qquad (3-4)$$

Where F is the switching frequency, D is the duty cycle of Q_7, R_{DS} is the on state resistance of Q_7, I_{Load} is the load current, C_{Gate6} is the gate capacitance of Q_6.Hence, for a given C_3 the required minimum capacitance of C_2 can be calculated by using the equation above.

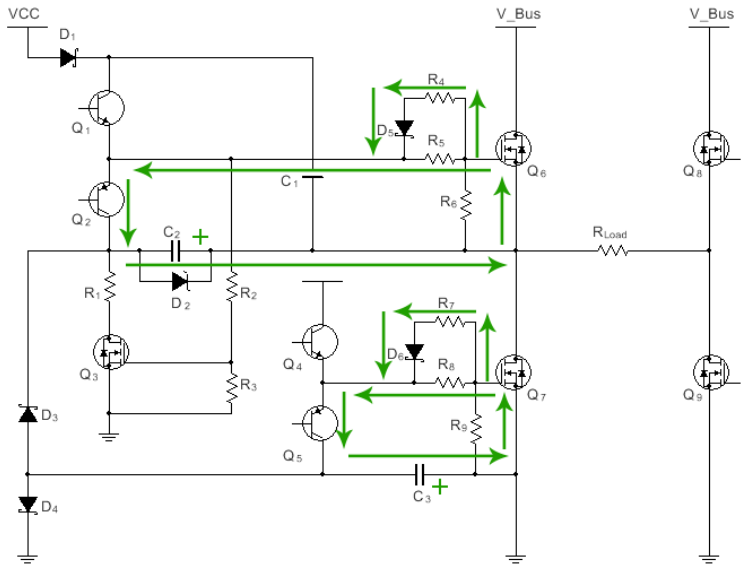


Figure 3.14. Simplified schematic of the negative bias generator for bridged converter, S5.

S5, dead-time: Q_7 will be turned-off by the switch on of Q_5, whilst Q_6 remains off. Q_7 is now negatively biased through the discharging of C_3 via Q_5. At this stage, all the capacitors that used to provide a negative bias to a power switches have been charged (may not be fully charged), so that when a power switch is turned-off, a negative bias will be applied to a Gate to Source terminal.

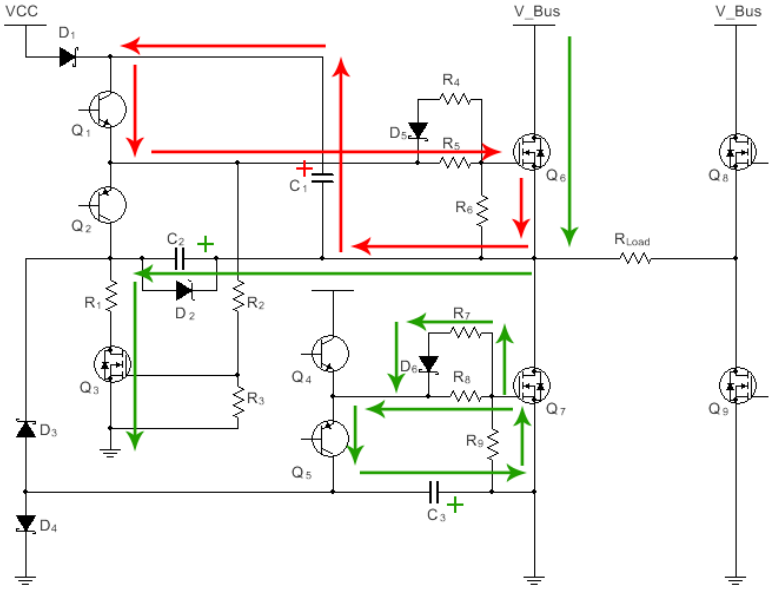


Figure 3.15. Simplified schematic of the negative bias generator for bridged converter, S6.

S6, high-side on: The high-side power switch Q_6 is turned-on by switch Q_1 on whilst Q_7 remains off. This step is quite similar to S2, however the potential that keeps Q_7 off is now a negative bias sourced by C_3 instead of pulling the Gate of Q_7 to ground as shown in Figure 3.11.

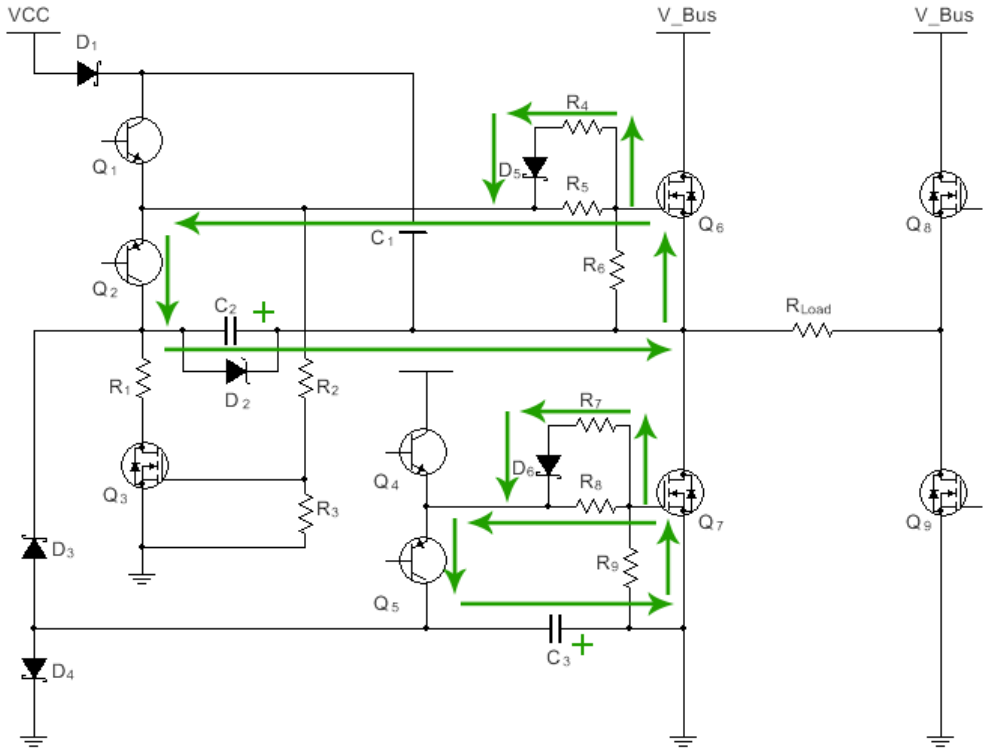


Figure 3.16. Simplified schematic of the negative bias generator for bridged converter, S7.

S7, dead-time: Q_6 will be turned-off by the switch on of Q_2 whilst Q_7 remains off. After this step, the switching sequence will go back to S4 and repeat then on from S4 to S7, with all the capacitors that are used to provide negative bias having been charged.

3.5. Challenges when using a modern integrated gate driver chip

Using a discrete high side and low side gate driver is less common in modern converter design, a typical integrated gate driver application circuit is shown in Figure 3.9. When using a modern gate driver chip, the desired negative bias generator can cause problems in a non-isolated application. As can be seen from the non-isolated full-bridge converter, the logical PWM signal from the controller is referenced to the common ground; specifically the PWM controller and the gate driver have the same ground. As a result, the logic signal will be higher than its normal level by the value of negative bias across C3. Therefore, when using a negative bias generator, the ground of the gate driver must be separated from the controller's ground to avoid the signal voltage seen on the gate driver exceeding its maximum input voltage. Moreover, during start up, this level difference will increase over a period of time, and therefore makes it impossible to use a simple voltage divider.

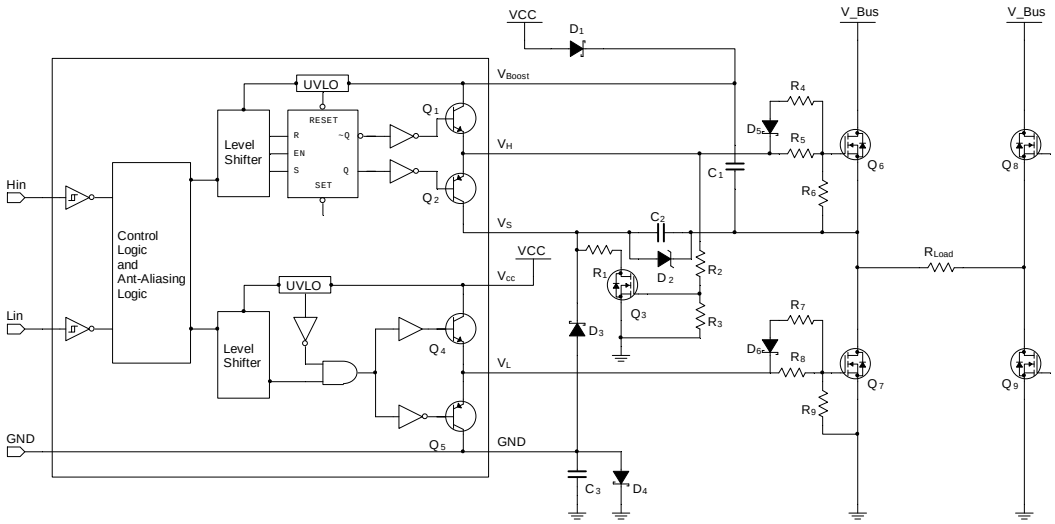


Figure 3.17. Simplified schematic when using a non-isolated modern gate driver.

A typical method to solve this problem is to use an optocoupler or digital isolator. By completely separating the ground of the gate driver and the PWM controller, the level difference issue will be eliminated. Although this will increase the circuit complexities, the proposed design still only requires one isolated power supplier compared with two voltage rails in a conventional design.

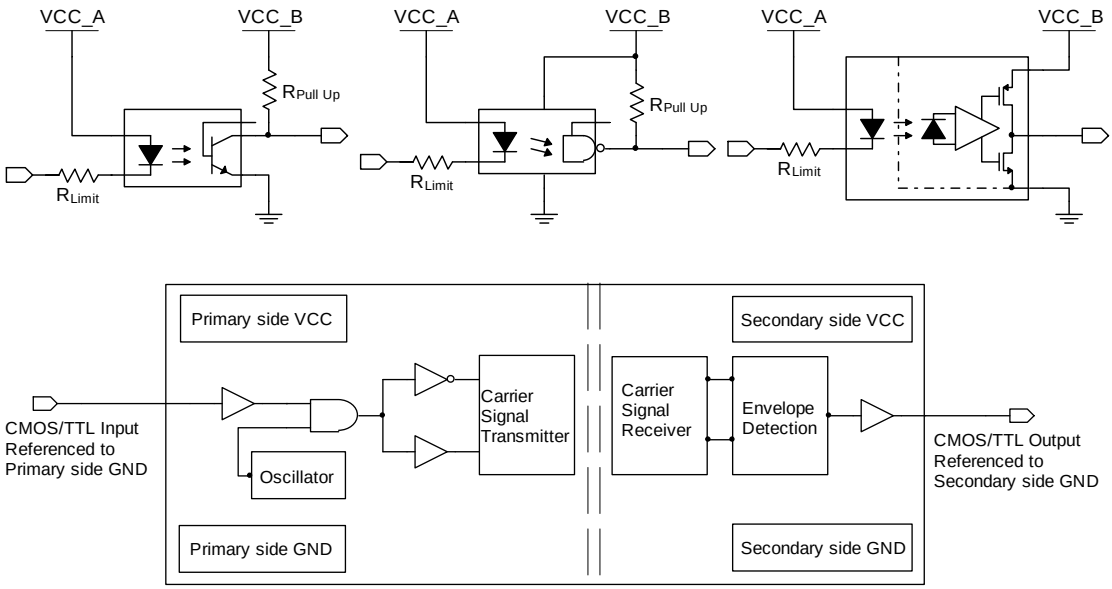


Figure 3.18. Using an optocoupler or digital isolator as a level shifter.

The optocoupler introduces a propagation delay, which will vary from device to device, making the dead-time control more complicated, particularly in high-frequency applications. An improved solution can be found by using an Op-Amp, shown in Figure 3.19. Since the output of the Op-Amp is always referenced to its ground, the signal level between the output of the Op-Amp and the common ground between the Op-Amp and the gate driver can be regulated.

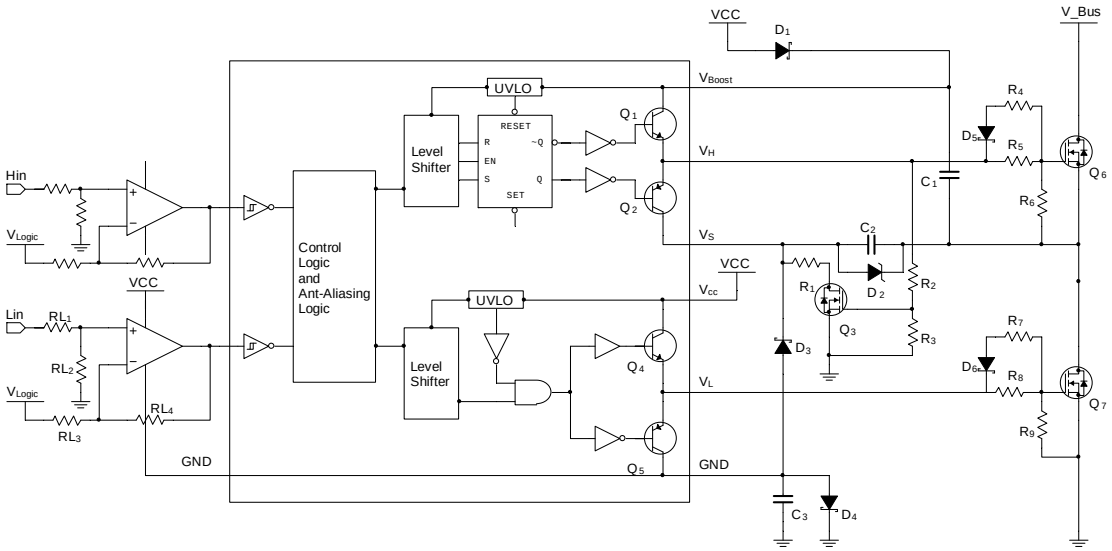


Figure 3.19. Using an Op-amp as a level shifter.

3.5. Overview of the prototype converter design

To demonstrate the concepts introduced in this thesis a prototype full-bridge converter was built that could be used to drive the wireless power transmitting coil. The following section will provide an overview of the design methodology, with the hardware divided into three sections; the full-bridge converter, the digital control and the power supply.

3.5.1. The full-bridge conversion stage

This single-phase full-bridge converter draws power from a DC power source which will then be used to charge two lead acid batteries. As the battery voltage can go up to 27.6V, power switches with 60V breakdown ability are implemented. NTMFS5H600, are chosen as the switching MOSFET which are fitted with fast intrinsic diodes (28ns typical in this case). The MOSFET chosen are featured as low R_{ds}=9.2 mΩ, low Q_g= 4.5nC and low input capacitance C_{iss} =880pF, so that both conduction losses and driver losses can be minimised. At room temperature, the NTMFS5H600has a current capability of 50A, which reduces to 35A at 100 degree Celsius (the estimated maximum operating temperature of those MOSFETs). Furthermore, the desired negative voltage generation circuit was implemented to provide -5V drive bias to ensure a solid turn off. The basic topology of the desired full-bridge conversion stage includes a power source providing power to the boosted high-side driving, logic-driven gate drivers, resistors controlling the gate charging speed, and additional circuitries providing negative bias.

3.5.1.1. Gate driving

Half of the complementary bridge is shown in Figure 3.20.

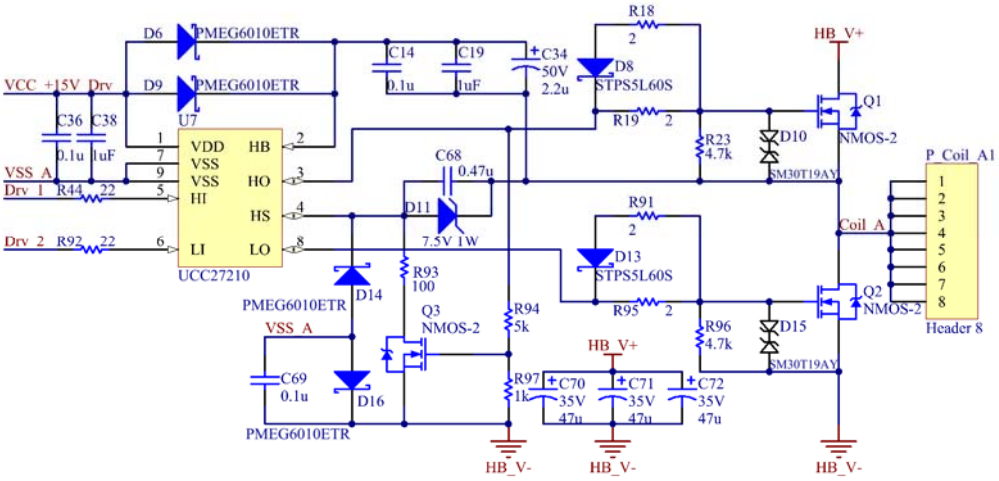


Figure 3.20. Conversion circuirtry of the prototype converter, showing its half-bridge.

Since the switching frequency of the MOSFET is initially designed to switch at a frequency of up to 2MHz, the drive chip is chosen to have a minimal rise and fall time, along with a short propagation delay. When choosing the gate driver, its output rising and falling time together with the propagation delay should be considered to minimise the dead-time required. A Texas Instruments UCC27210 series gate driver was chosen as it provides 7.2ns raising and 5.5 falling times, 18ns propagation delay and 2ns difference between channels. In the schematic diagram (Figure 3.20), R18 and R91 are used to adjust the turn-off time whilst similarly, R19 and R95 are used to adjust the turn-on time. Other, additional components to note are D10 and D15, these Transient Voltage Suppression (TVS) diodes are implemented to protect the gate from unexpected charge accumulation as well as protect the gate driver from MOSFET Drain-Gate breakdown.

3.5.1.2. 15V Power supply for the gate driver

In order to allow scope for further optimizations with respect to MOSFET selection, the power

supply for the gate driver was overrated to be able to provide 15V DC at 5A. As shown in Figure 3.21, the 15V 5A power supply consists of two parts: a 15V buck converter operating at 200KHz providing a +15V output and an auxiliary buck converter switching at 500kHz to provide a +7V auxiliary power for the +15V buck converter. There are two reasons for this unusual design; firstly the LTC1624 in the schematic has an internal 5.6V linear regulator for the top side MOSFET driver supply, however, for the particular MOSFET chosen, 5.6V drive voltage may cause insufficient turn-on. Secondly, when the system is operating at 24 V input voltage, this linear regulator will generate excessive heat that will trigger the thermal cut-off functionality of the PWM controller. Although increasing the PCB polygon area or adding an extra heatsink could remove the heat, an auxiliary power supply is clearly the optimum solution as it also solves the insufficient turn-on issue caused by the 5.6V internal drive voltage.

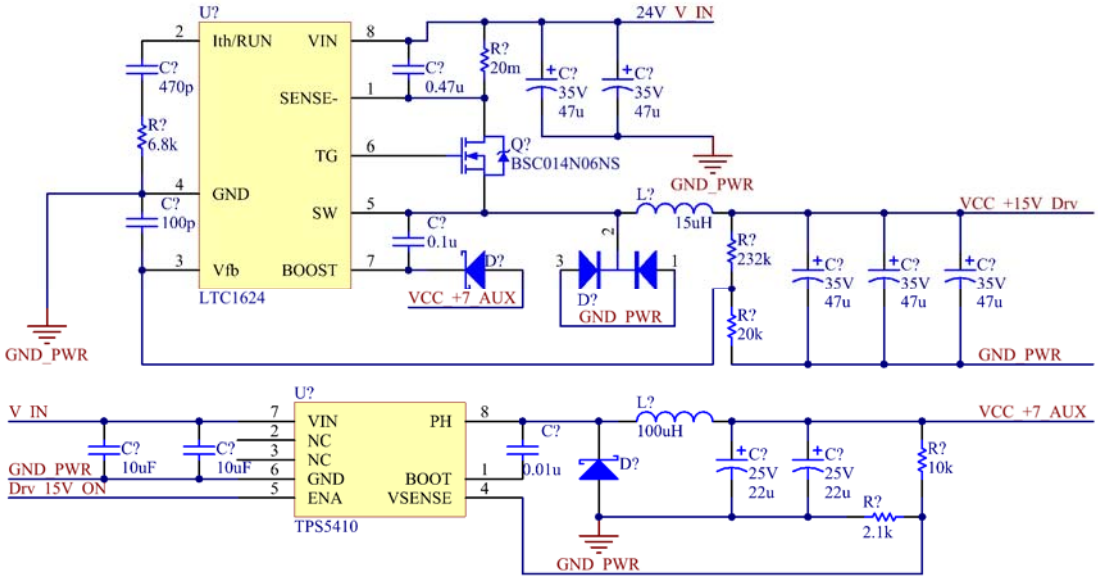


Figure 3.21. Schematic of 15V power supplier for gate driver.

3.5.2. Digital controller and sensors

In this design, the control is implemented on an STM32 ARM Cortex-M4 microcontroller, shown in Figure 3.22. By utilising its on-board data converters, a simple shunt resistor can be used for current sensing and voltage dividers for voltage sensing. Meanwhile, an Organic Light-Emitting Diode (OLED) display with push buttons forms a user interface to control the output power and frequency of the desired converter, as shown in Figure 3.22. An infrared remote receiver provides extra remote adjustment capability.

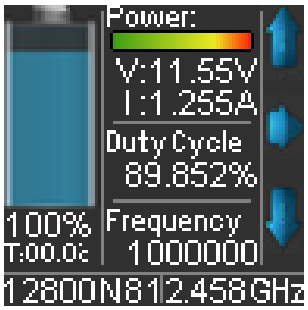


Figure 3.22. User interface of the desired converter showing its controls.

3.5.2.1. On-board microcontroller

As can be seen from Figure 3.23, differential inputs of the internal ADC are utilised to sample the input current and voltage required. Two timers are used to generate the required phase-shifted full-bridge PWM signals, each pair are complementary (labelled as TIMx_CHx and TIMx_CHxN) and programmable dead-times are implemented. Furthermore, a Universal Asynchronous Receiver/Transmitter (UART) and Inter-Integrated Circuit (I2C) bus are provided on an external connector to provide flexibility in integrating the prototype into other systems.

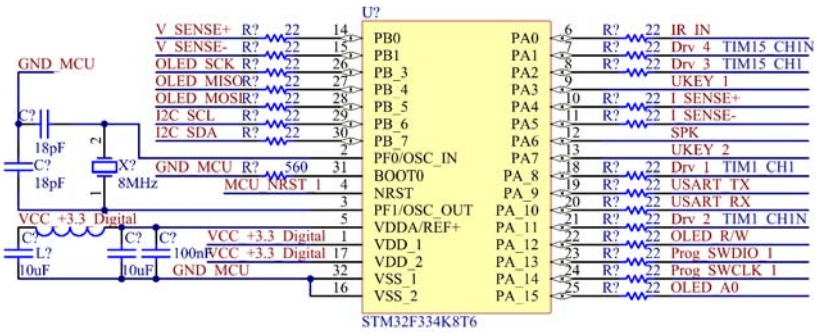


Figure 3.23. Schematic of controller dominated in this design.

3.5.2.2. Input voltage and current sensing

The input voltage is sampled through a voltage divider, as shown in Figure 3.24. There are two considerations for the design of this voltage divider which consists of 8 resistors instead of the more conventional 2 resistor design. Firstly, the 8 resistor network significantly reduces the risk of a microcontroller breakdown caused by a detached low-side resistor, where the input voltage will directly connect to the microcontroller. Secondly, the redundant high-side resistor reduces the risk of lost power control, resulting in a dramatic output power increase, caused by a poorly contacted high-side resistor.

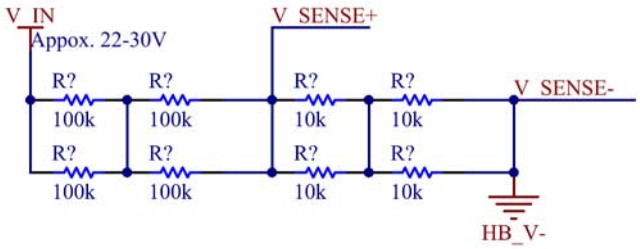


Figure 3.24. Resistor network used for voltage divider.

To minimise the size of the PCB board area and to simplify track routing, a shunt resistor is used for current sensing. As shown in Figure 3.25, the current sensing amplifier provides a 20 V/V voltage gain so that at the designed maximum power (20V, 15A input) the output of the current sensing amplifier is approximately 3V, which is within the input voltage limits of the ADC. A

separate linear regulator is used to provide +5V power to the amplifier. Since the MAX4080 current sense amplifier only draws 75μA of current, use of a linear regulator to obtain 5 volts from a 24 volt input can be considered to be efficient without the need to implement a switching regulator.

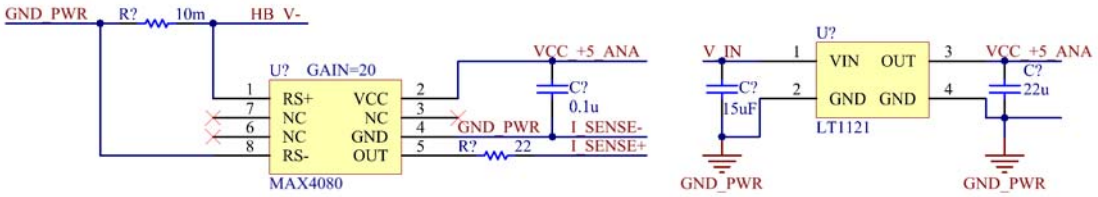


Figure 3.25. Current sensing amplifier and its linear power regulator.

3.5.2.3. User interface

A basic user interface is designed to control the output power while monitoring the system status. The user feedback is presented on a 96*96 OLED display and a 13mm speaker, as shown in Figure 3.26.

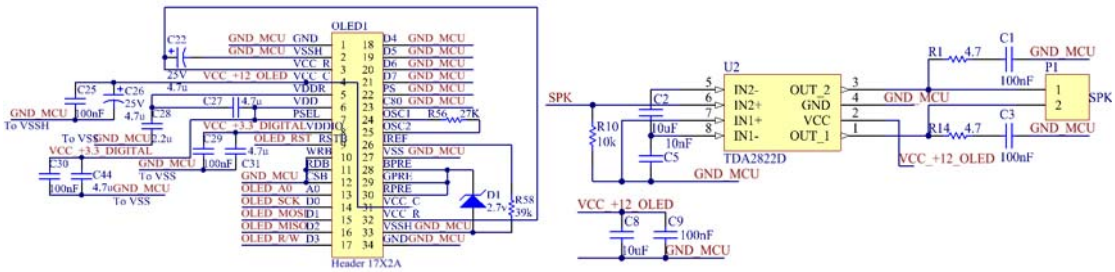


Figure 3.26. Schematic of the OLED display and class AB BTL amplifier drives the speaker.

For the user input, two methods are designed. For basic controls such as to increase or decrease the output power, the on-board button switches are used, whereas for more complex control of functionality this is achieved via an infrared remote controller. The schematic for one of the button switches and the infrared receiver is shown in Figure 3.27.

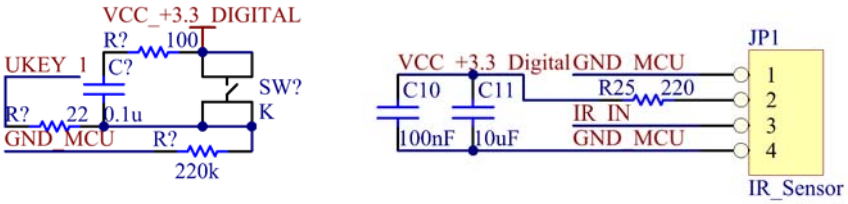


Figure 3.27. Schematic of the Push button switch and IR receiver.

3.5.2.4. Power supply for the microcontroller and user interface

Most of the digital components in this prototype require a 3.3V power supply with an additional 12V needed to supply the OLED display. As shown in Figure 3.28, both the 3.3V rail and 12V rail use a step-down buck converter switching at 700 kHz, with each using a different feedback resistor to achieve the desired output voltage.

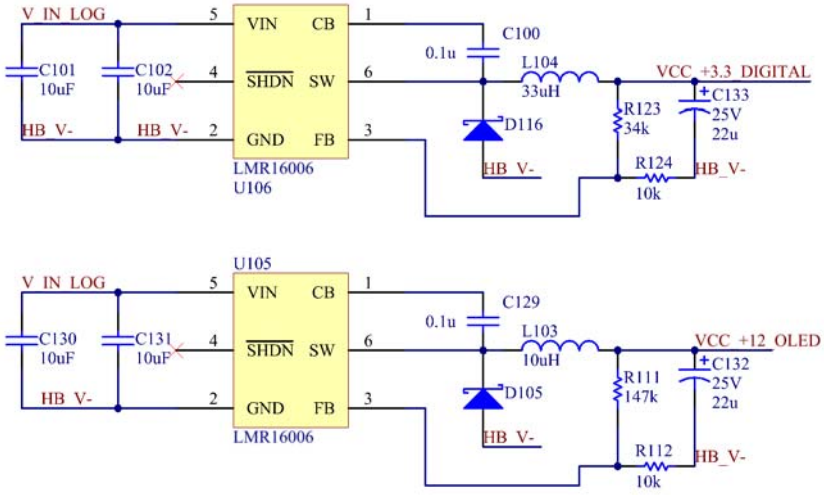


Figure 3.28. Switching regulator provides 3.3V and 12V digital power.

3.5.3. Input protection

The prototype design incorporates a two step protection as shown in Figure 3.29. Firstly, a small transient voltage will be absorbed by the TVS diode connected at the input connector. At a time when a significant over voltage happens, the Gas Discharge Tube (GDT) will start to discharge

and blows the fuse. The reason for using a GDT in series with a varistor, is to protect the GDT from degradation caused by repeated negligable discharge, which subsequently means a smaller varistor can be implemented.

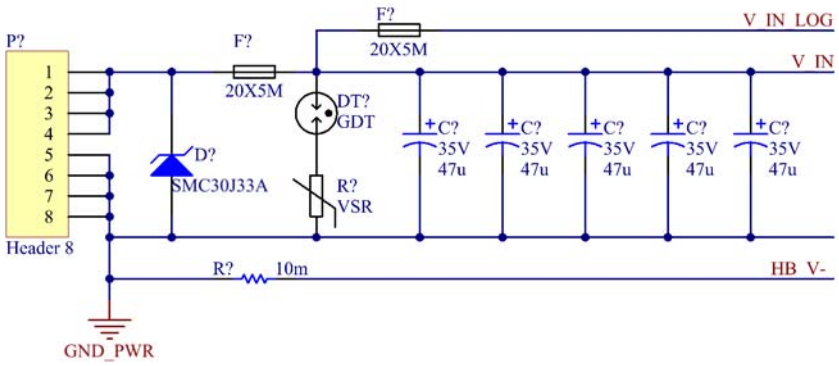


Figure 3.29. System power input and protections.

3.5.4. The layout and finished prototype converter

The prototype converter is routed on a 92mm*78mm, double side, 1 ounce copper PCB. The overall thickness of the PCB together with components is controlled to around 6mm. Attention has been taken to reduce the loop area of all high dv/dt connections. As shown in Figure 3.30, which shows the top layer copper of the full-bridge section.

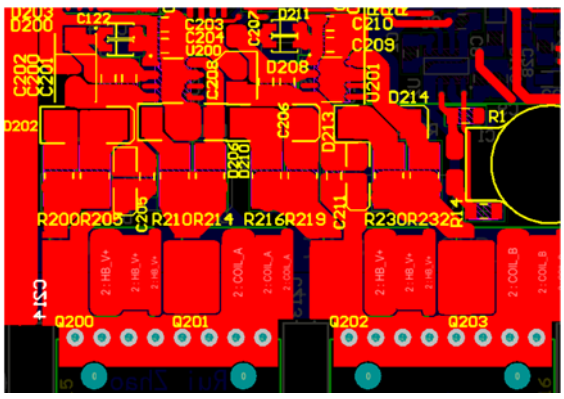


Figure 3.30. Layouts at the gate driver and full-bridge section.

To reduce the parasitic inductance of the capacitor as well as reduce the overall height, the prototype uses multiple small capacitors connected in parallel to support the ripple current. The assembled prototype is shown in Figure 3.31

Figure 3.31. Assembled prototype converter showing its capacitor array.

3.6. Evaluation result

The prototype converter shown in Figure 3.31 has been evaluated with a 24V input. In order to achieve better negative biasing performance, the lower side MOSFET should be turned on first. Using the schematic shown in Figure 3.17, Figure 3.32 shows the voltage across C_2 during start-up. As can be seen from the Figure, the desired negative voltage can be achieved in rapidly dependant on the duty cycle of Q_6 and corresponded C_2 and R_1. Using this voltage, Figure 3.33 shows the gate driving voltage across Gate-Source terminal of Q_6. Figure 3.33 clearly demonstrates that even after several cycles from start-up, some negative voltage has appeared on the gate driving output.

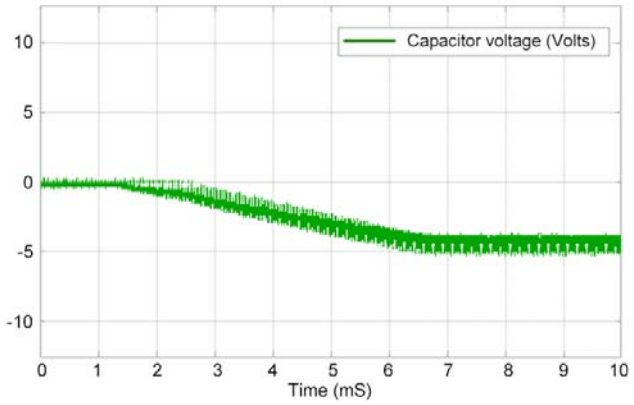


Figure 3.32. The voltage measured across C_2 demonstrating its charging progress.

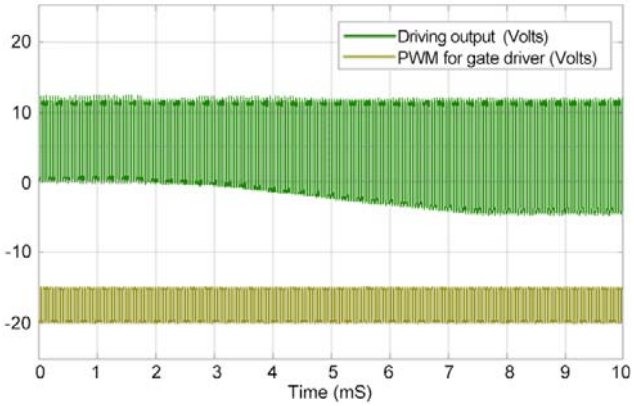


Figure 3.33. Gate driving output (Green) and logical gate drive signal (Yellow), showing the establishment of bipolar driving voltage.

The minimum negative bias applied to the MOSFET will depend on the duty cycle of high-side MOSFET, which also represents the duty cycle of C_2. The Zener diode D_2 can only limit the minimum biasing level when designed duty cycle is achieved so that sufficient energy is stored into C_2. If the duty cycle of the charging C2 is lower than the designed value, negative voltage with lower amplitude will be applied. The following Figure 3.34 shows the different negative biasing levels at different duty cycles.

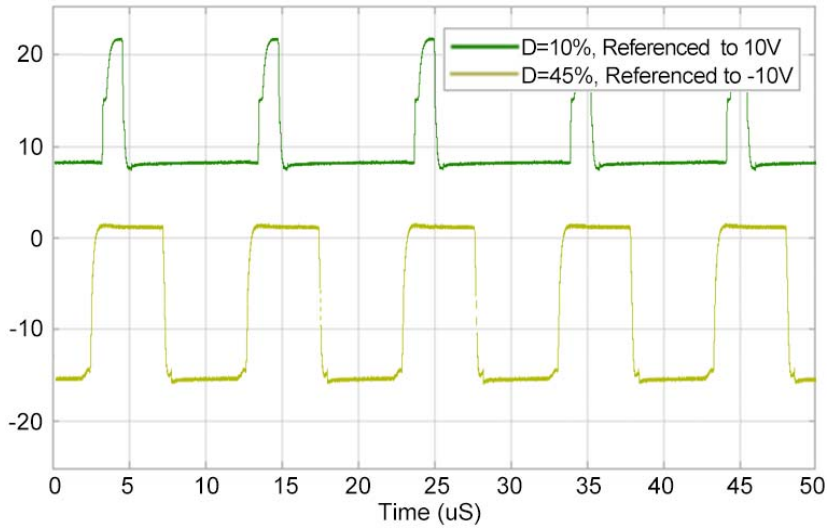


Figure 3.34. Gate driving output showing the different biasing level verse duty cycle.

Figure 3.35 and Figure 3.36 demonstrate the relationship between duty cycle (X-axis) and the minimum biasing level (Y-axis), when using different combinations of C_2 and R_1. As can be seen from the following Figures, using smaller C_2 or R_1 will give a greater biasing level but increase the power consumption across R_1 and D_2.

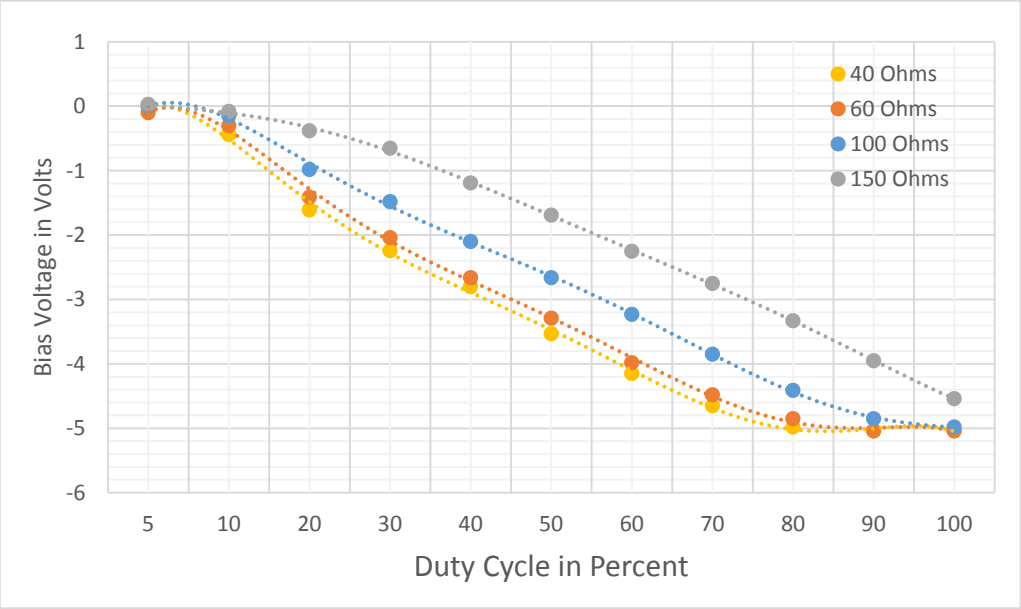


Figure 3.35. Biasing level verse duty cycle when using different R_1; C_2=1uF.

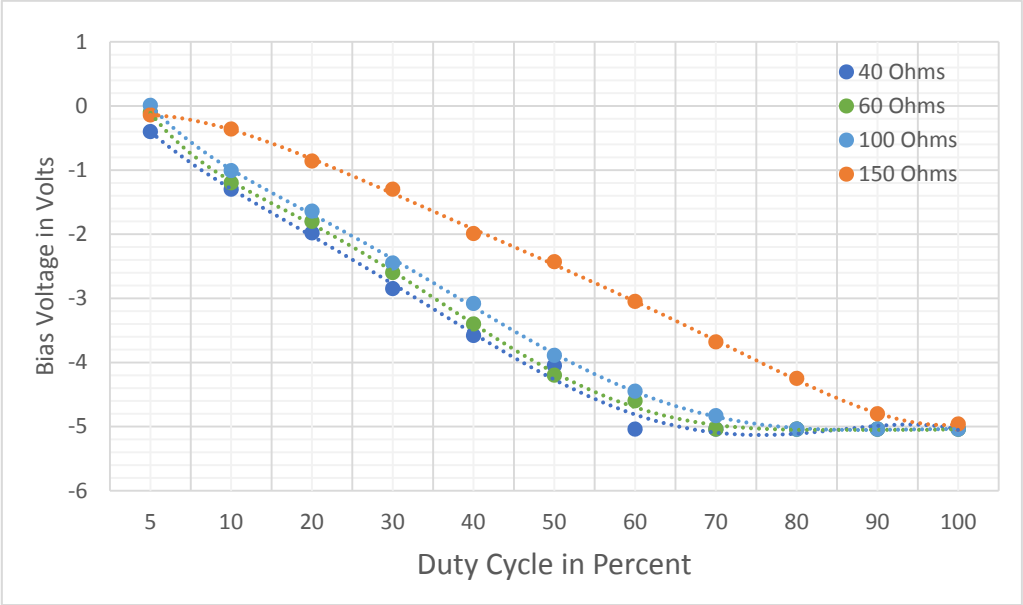


Figure 3.36. Biasing level verse duty cycle when using different R_1; C_2=0.1uF.

3.7. Summary

This chapter has described the design and operation of a technique for generating a negative bias for MOSFET bipolar driving in non-isolated MOSFET driving and demonstrated how the desired negative voltage can be obtained. This chapter also describes the approach of how to modify a conventional gate drive so that bipolar gate driving can be achieved using a conventional gate driver with limited discrete components. The evaluation has shown that by using the negative bias generator, negative voltage for MOSFET gate driving can be acheived without using a charge pump and switching regulator. Using a full-bridge as an example, while the desired negative bias generator guaranteed a solid turn-off, using MOSFETs with lower V_{gs} and driving them using an optimised turn-on voltage could significantly reduce the driving loses. Several key components can be calculated using equations provided in this chapter while the level shifting issues can be eliminated using those isolated or non-isolated solutions provided in 3.4.1. Finally, the methodology introduced in this chapter can also be used in other gate driving topologies and isolations to remove the need for a power source that provides negative voltage.

4. Microcontroller implemented matrix converter

4.1. Introduction

Using the conventional converter introduced in Chapter 3 requires bulky DC intermediate components and suffers from other issues as illustrated in Chapter2. A matrix converter can convert an input AC voltage into the desired output in a single stage avoiding the need for a DC link. However, the control to drive a single phase matrix converter is more complex requiring two drive signals for a bidirectional switch and has four independent switches that need to sequenced according to the input waveform. Conventional controllers (i.e. linear controller, microcontroller or FPGA) are generally not suited for matrix converter designs due to its complexity and cost associated. Off-the-shelf microcontrollers are generally do not have the dedicated modules to deliver the 8 driving signals required by the switch matrix, also the control oriented microcontrollers are not fast or reliable enough to control the switch matrix by using programmable IO mode. Considered about the cost and design complexity when utilising a FPGA as converter controller, in this chapter a new methodology is presented to design a matrix converter using conventional controllers.

The novel approach consists of a conventional full bridge converter controller (i.e. linear controller, MCU-based controller etc.), a middleware, the switch matrix, the grid power interface, and the resonant load. As it will be shown in this chapter, the conventional full-bridge converter controller can drive the switch matrix of a single phase matrix converter. Since the AC switch implemented on a given matrix converter has four-quadrants continuity, this chapter initially focuses to establish the logical transfer function of AC switch in terms of the input voltage and load current. Beginning with the comparisons between the AC switch matrix and DC switch matrix, the separated projections of two full-bridge converters onto a single phase matrix converter will be discussed, followed by the drive signal logic. The analysis of the logic signal is then used to create a truth table to inform the circuit design. Simulation results are evaluated using reference designs to investigate parameter selection and implications of operation.

Finally, a hardware prototype is built based on a common matrix converter topology with the proposed middleware and conventional controller for analysis.

4.2. Overview of Microcontroller dominated matrix converter

Conventionally, the control of a matrix converter requires hardware that can implement very fast, low latency control, typically realised using Digital Single Processors (DSPs) together with Field Programmable Gate Arrays (FPGAs). Figure 4.1 shows a simplified schematic of a FPGA dominated single phase to single phase matrix converter.

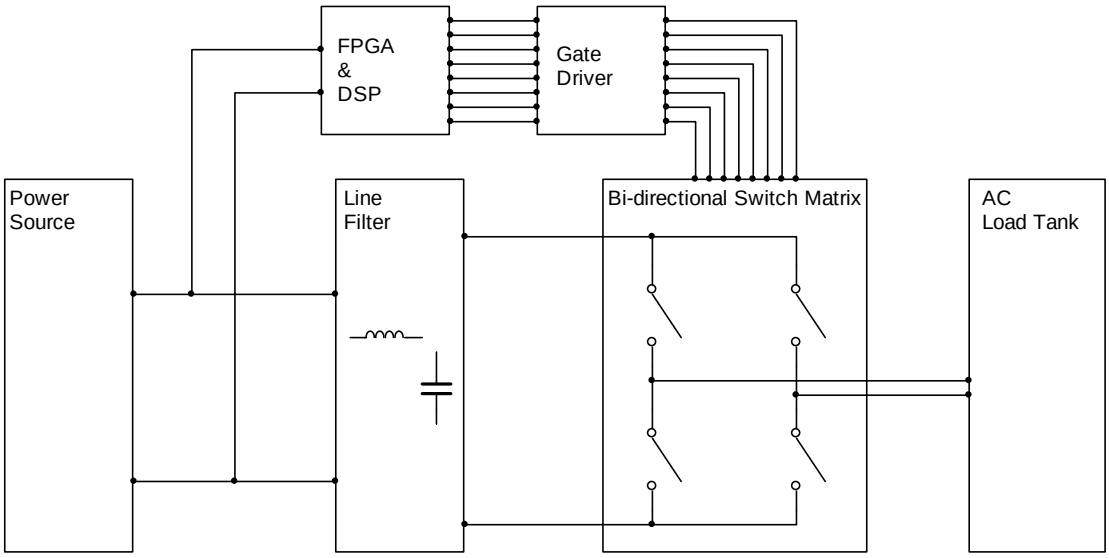


Figure 4.1. Typical topology for a FPGA dominated matrix convert (simplified).

The use of an FPGA has a number of disadvantages in terms of programming complexity, power consumption, cost and size; the latter two been particularly important for consumer products. Conventionally, an analogue controller or microcontroller control forms the basis of a simple and cost-efficient converter design. Hence, in this chapter, a microcontroller dominated matrix controller design will be introduced. By adding a single logic chip to a conventional full-bridge design, this solution enables the use of a low cost widely-used PWM controller to control the operation of a matrix converter. In addition to carrying the intrinsic advantages of traditional matrix converters, the design greatly reduces its complexity and cost.

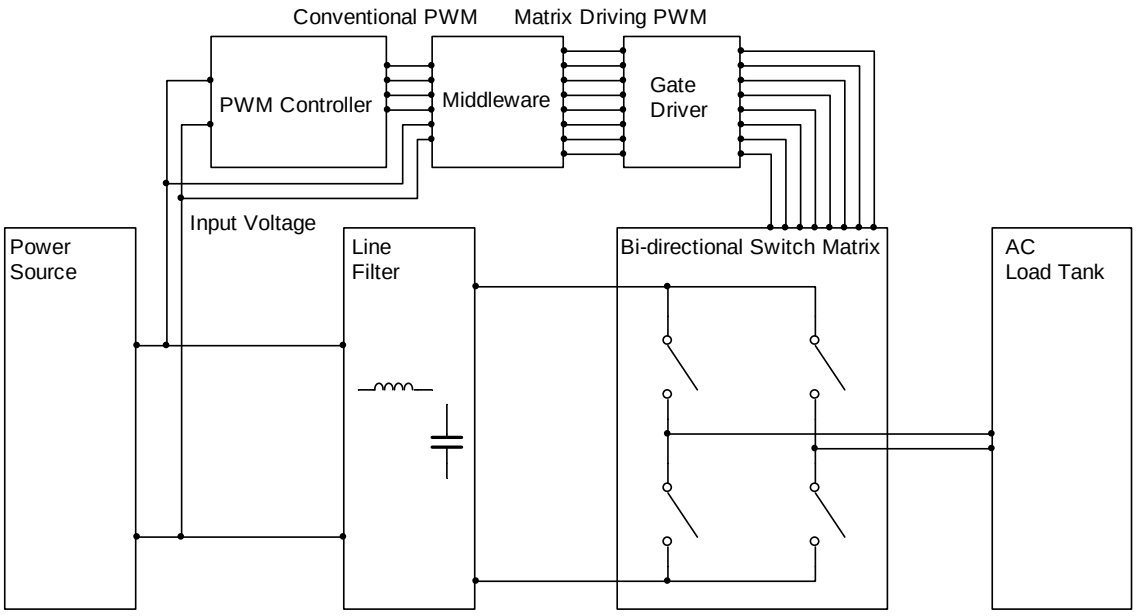
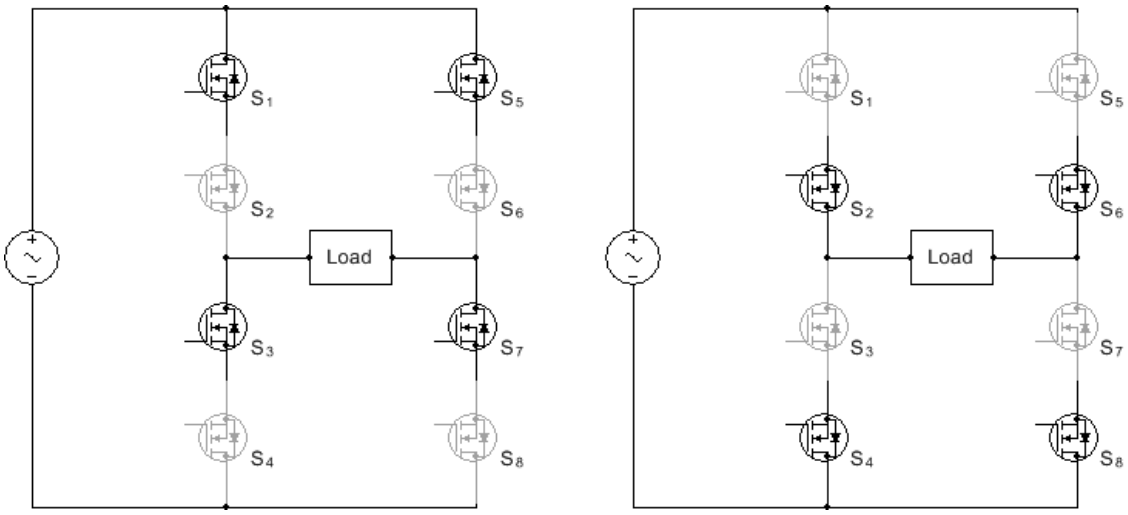


Figure 4.2. Block diagram of proposed converter

4.3. Signal Allocation and Distribution Circuit

Figure 4.3 shows the proposed microcontroller dominated matrix converter. The fundamental principle is that by considering the sign of the input voltage (Vin), therefore having split the input waveform into two halves, a single-phase to single-phase matrix converter can be considered as an integration of two full bridge converters, one for each half waveform. In the simplest condition, two drive signals (PWM1 and 2) can be used to control a full bridge converter, which can also be used to drive a single-phase matrix converter during one-half of the input waveform.



(a) Vin above zero (b) Vin below zero

Figure 4.3. Equivalent circuit of a single phase matrix converter depends on its input voltage

In order to generate the drive signals and control the operation of the matrix converter, the polarity of the input voltage is used to divide the switch matrix into two full-bridges as shown in table 4.1.

Table 4.1. Matrix switching on the time domain of input voltage.

	$T \in (2\pi x, 2\pi x + \pi)$	$T \in (2\pi x + \pi, 2\pi x + 2\pi)$
$V=V_p \sin(T)$	V>0	V<0
Active Switches	S1, S3, S5, S7	S2, S4, S6, S8

When the sign of the input voltage is positive, as shown in Figure 4.3 (a), S2, S4, S6 and S8 are turned on, the matrix converter can be considered as a full-bridge converter which is formed from S1, S3, S5 and S7. Under these circumstances, the drive signals of each power switch are shown in Table 4.2.

Table 4.2. Assignments between controller outputs and desired MOSFET when Vin is above the x-axis

Power Switch	Drive signal
S1	PWM1
S2	Constant On
S3	PWM2
S4	Constant On
S5	PWM3
S6	Constant On
S7	PWM4
S8	Constant On

By contrast to the previous situation, when the sign of input voltage goes negative, as shown in Figure 4.3(b), a full-bridge converter now consists of S2, S4, S6 and S8 while S1, S3, S5 and S7 are turned on. Table 4.3 shows the desired drive signals

Table 4.3. Assignments between controller outputs and desired MOSFET when Vin is negative

Power Switch	Drive signal
S1	Constant On
S2	PWM4

S3	Constant On
S4	PWM3
S5	Constant On
S6	PWM2
S7	Constant On
S8	PWM1

The drive signal allocation logic can be found by combining Table 4.2 and Table 4.3 together and taking the input voltage sign logic into consideration. If Vin=1 is defined as positive input voltage and Vin=0 is defined as negative input voltage, the following truth table 4.4 can be established.

Table 4.4. Truth table for gate signals

Power Switches	Vin>0	PWM 1 or 2	Drive Outputs to power switch
S1, S3, S5 and S7	1	1	1
	1	0	0
	0	1	1
	0	0	1
S2, S4, S6 and S8	1	1	1
	1	0	1
	0	1	1
	0	0	0

The truth table can be translated into the following logic gate structure (Figure 4.4) which consists of 4 ‘OR’ gates and 2 inverters. However, if the comparator used to determine the sign of input voltage provides both Vin>0 and inverted Vin>0, the logic structure shown in Figure 4.4, can be further reduced to a 4 ‘OR’ gates.

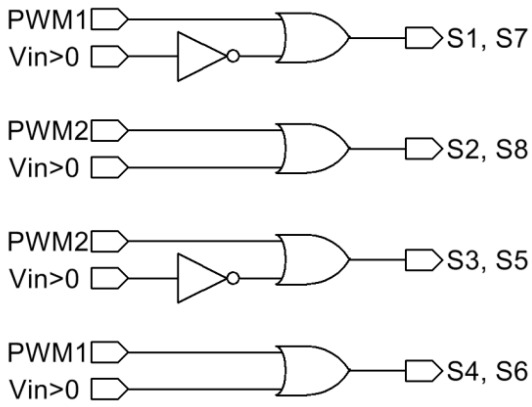


Figure 4.4. Logic Gate topology of the proposed drive signal allocation circuit

Based on the logic structure shown in Figure 4.4, a 'middleware' logic system can be proposed in order to realize the microcontroller based control scheme. As shown in Figure 4.5, the middleware takes the full-bridge control signal from the microcontroller and then generates the required drive signals according to the input voltage polarity. The circuit consists of two 4 channel logic OR gates and a 6 channel logic inverter.

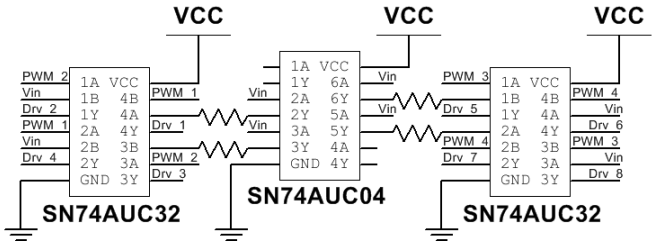


Figure 4.5. Proposed middleware utilizing 3 x Quadruple 2-Input Positive-OR Gate ICs

4.4. Working modes of the microcontroller dominated matrix converter

The principle operation of the proposed matrix converter is similar to a phase-shifted full bridge converter. With S2, S4, S6, S8 constantly turned on while the input voltage is in the positive part of the cycle, and S1, S3, S5, S7 turned on while the input voltage is in the negative part of the cycle, the operation waveforms of the proposed matrix converter are as shown in Figure 4.6. Dependant on the converter's input status, drive signal 1 and 2 are allocated to the lagging legs, S1, S3, S6 and S8, while drive signals 3 and 4 are allocated to the corresponded leading legs, as shown in Figure 4.7.

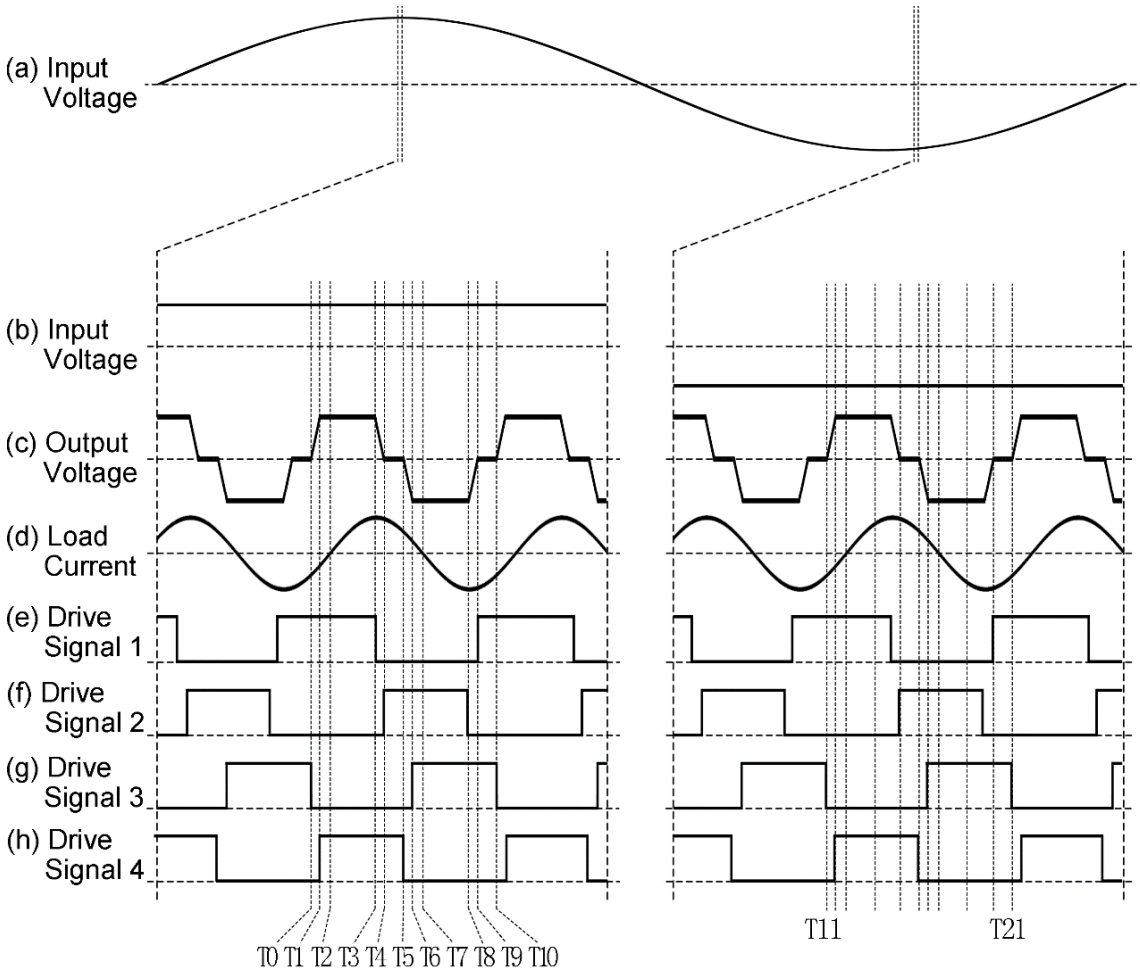


Figure 4.6. Operation waveforms of the proposed matrix converter.

By using the phase-shifted control signals from a microcontroller or linear controller, the working modes of the proposed single-phase matrix converter can be illustrated in the following steps.

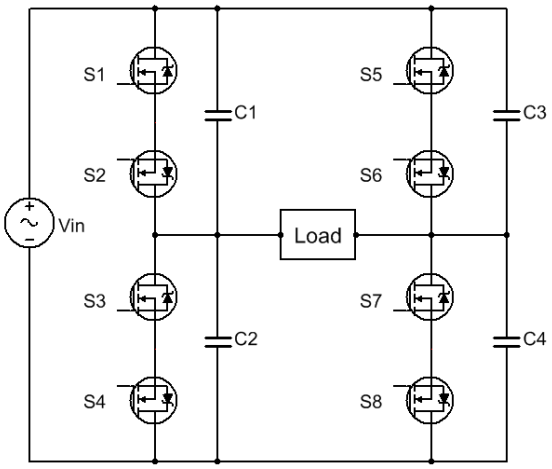


Figure 4.7. Simplified schematic of the proposed matrix converter.

t<T0: Before T0, there is current flow through S1, S2, S5 and S6. Therefore C1 and C3 are discharged and the voltage across C1 and C3 can be, as an estimation, be zero. This instantaneous status is shown in Figure 4.8.

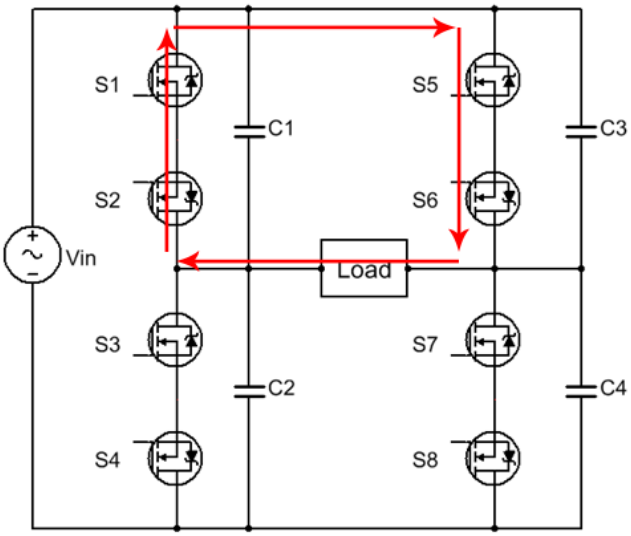


Figure 4.8. Current status of a single phase to single matrix converter, at t<T0.

T0-T1: Figure 4.9 shows Vin on its positive half cycle, S2, S4, S6 and S8 are permanently turned on, the drive signals 1 and 2 are allocated to S1 and S3, whilst the drive signals 3 and 4 are

allocated to S5 and S7. At t=T0, S5 will be turned off and S1 will maintain it's on status, and the freewheeling current now flows through the body diode of S7. At the instance of turn S5 off, C3 will be charging so that S5 is turned off in zero voltage status. Meanwhile, before carrying current through S7 and S8, C4 will be firstly discharged and prepare for a zero voltage turn on for S7. This will also insert a dead-time before turn S7 on.

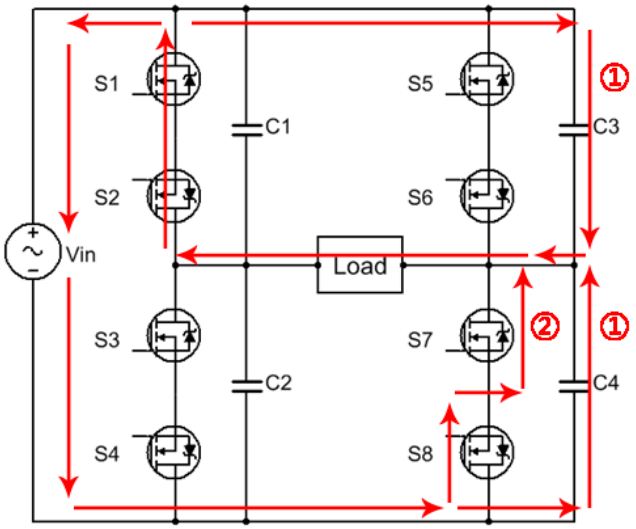


Figure 4.9. Current status of a single phase to single matrix converter, at T0<t<T1.

T1-T2: As shown in Figure 4.10, with Vin on its positive half cycle, S2, S4, S6 and S8 remain permanently turned on, the drive signals 1 and 2 are allocated to S1 and S3, whilst the drive signals 3 and 4 are allocated to S5 and S7. At t=T1, S7 will be turned on in zero voltage mode since its body diode has been forward biased. Now, the junction of S7 will carry the current flow. At t=T2, the load current will reach its zero crossing point.

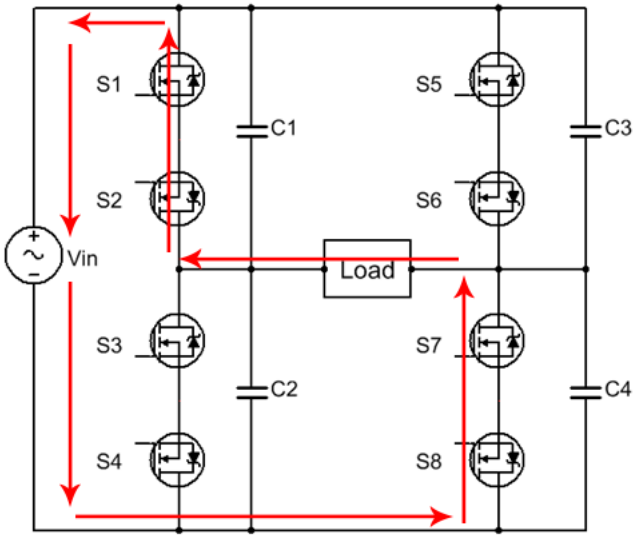


Figure 4.10. Current status of a single phase to single matrix converter, at T1<t<T2.

T2-T3: All signals remain its previous status. The load current will keep flowing in the direction shown in Figure 4.11.

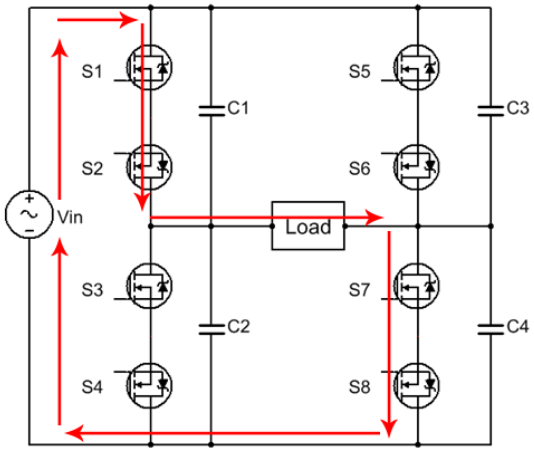


Figure 4.11. Current status of a single phase to single matrix converter, at T2<t<T3.

T3-T4: As shown in Figure 4.12, with Vin on its positive half cycle, S2, S4, S6 and S8 remain permanently turned on, drive signal 1 and 2 allocated to S1 and S3, drive signal 3 and 4 allocated to S5 and S7. At t=T3, S1 will be turned off, the load current will find its path through the body diode of S3. At the transient when S5 is turning off, C1 will start charging and forms a small voltage change across S1 and S2. After S1 been turned off, C2 will be begin charging during the dead-time before S3 is turned on. After S3 is turned on, the load voltage will be provided by C2

discharging.

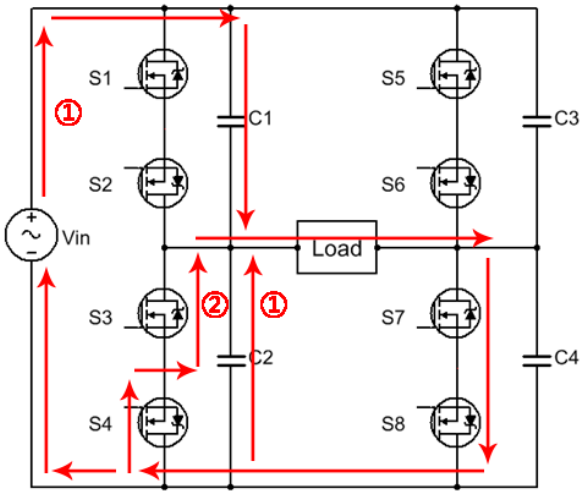


Figure 4.12. Current status of a single phase to single matrix converter, at T3<t<T4.

T4-T5: As shown in Figure 4.13, with Vin on its positive half cycle, S2, S4, S6 and S8 are constantly turned on, drive signal 1 and 2 allocated to S1 and S3, drive signal 3 and 4 allocated to S5 and S7. At t=T4, S3 will be turned on in zero voltage mode since its body diode has been forward biased. Now, the junction of S3 will carry its current flow.

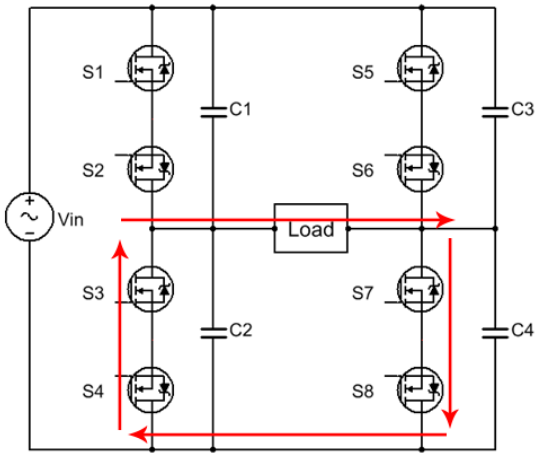


Figure 4.13. Current status of a single phase to single matrix converter, at T4<t<T5.

T5-T6: As shown in Figure 4.14, with Vin on its positive half cycle, S2, S4, S6 and S8 are permanently turned on, drive signals 1 and 2 are allocated to S1 and S3, whilst drive signals 3 and 4 are allocated to S5 and S7. At t=T5, S7 will be turned off in zero voltage mode by the

charging of C4 and force the load current flow through S5 and S6. Before the body diode of S5 is fully forward biased, C3 will be discharged in terms of preparation for the turn-on of S5.

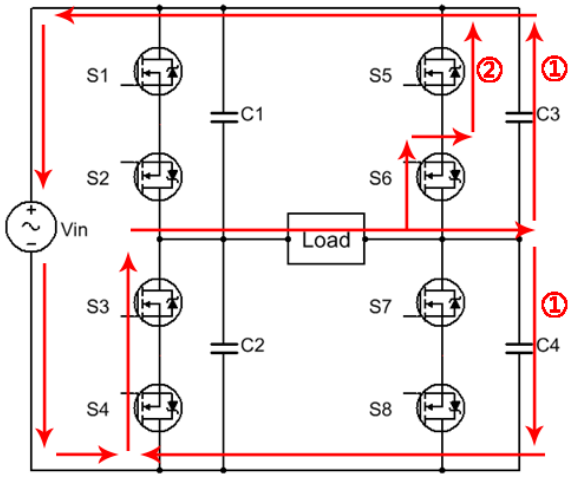


Figure 4.14. Current status of a single phase to single matrix converter, at T5<t<T6.

T6-T7: As shown in Figure 4.15, Vin on its positive half cycle, S2, S4, S6 and S8 are permanently turned on, drive signals 1 and 2 are allocated to S1 and S3, whilst drive signals 3 and 4 allocated to S5 and S7. At t=T6,

S5 will be turned on in zero voltage mode since its body diode has been forward biased. Most of the current will be carried by the junction of S5 with a minimum conduction loss. The load current will keep conducting in its positive cycle until t=T2 when the load current will reach its zero crossing point.

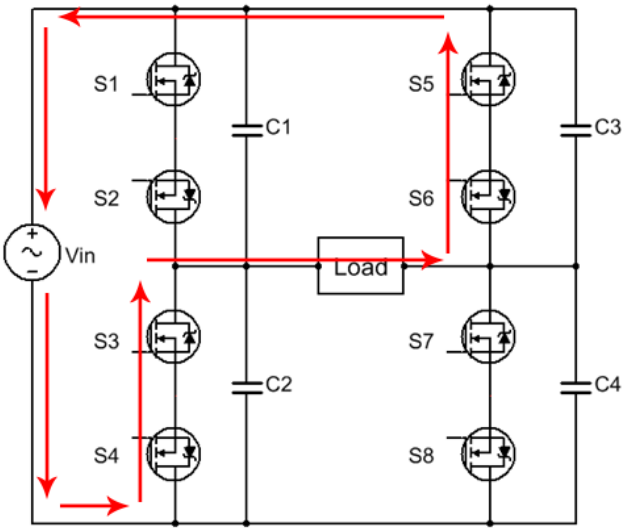


Figure 4.15. Current status of a single phase to single matrix converter, at T6<t<T7.

T7-T8: After t=T7, the load current will switch to its negative cycle. By keeping all the switches in their previous states, power will be delivered to the load. The new current flow can be found in Figure 4.16.

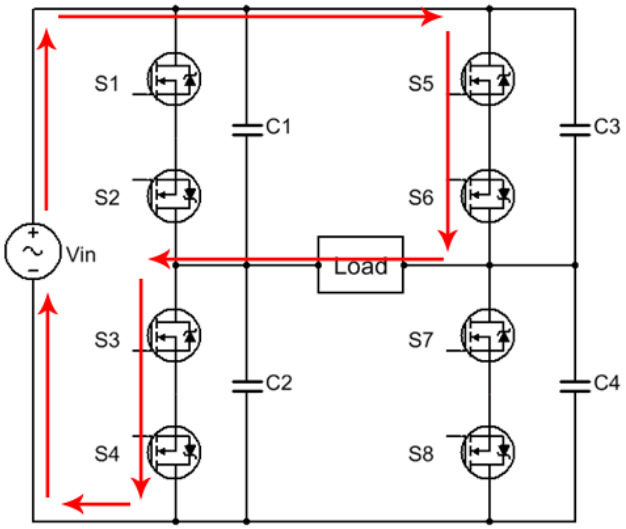


Figure 4.16. Current status of a single phase to single matrix converter, at T7<t<T8.

T8-T9: As shown in Figure 4.17, with Vin on its positive half cycle, S2, S4, S6 and S8 are permanently turned on, drive signals 1 and 2 are allocated to S1 and S3, whilst drive signals 3 and 4 allocated to S5 and S7. At t=T8, S3 will be turned off, in the very short period of time after

S3 has been turned off, C1 will discharge to supply the load current. After C1 is fully depleted, the parasitic diode of S1 will be forward biased and carry the load current from then on. Meanwhile, C2 will be charged after S3 and S4 are turned off, so that S3 will be turned-off in zero voltage condition.

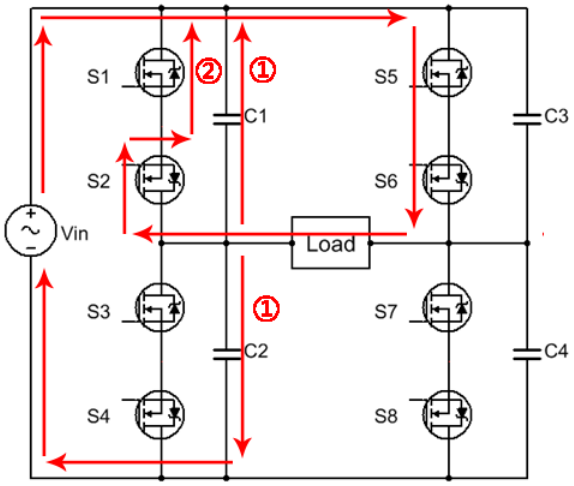


Figure 4.17. Current status of a single phase to single matrix converter, at T8<t<T9.

T9-T10: As shown in Figure 4.18, with Vin on its positive half cycle, S2, S4, S6 and S8 are permanently turned on, drive signals 1 and 2 are allocated to S1 and S3, whilst drive signals 3 and 4 are allocated to S5 and S7. At t=T9, S1 will be turned on at zero voltage since the diode of S1 has been forward biased.

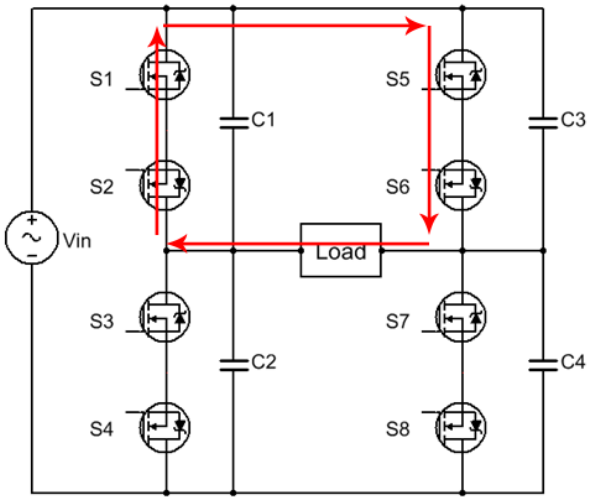


Figure 4.18. Current status of a single phase to single matrix converter, at T9<t<T10.

As can be seen from the description and Figures above, while the input voltage is above its zero crossing level, the middleware will keep the unrelated MOSFETs (i.e. S2, S4, S6 and S8) fully on. By keeping those MOSFETs on it is only necessary to control the remaining four MOSFETs, which is similar to a conventional full bridge converter. Under the same methodology, while the input voltage is below the zero crossing level, the middleware will permanently turn S1, S3, S5 and S7 on and remap the drive signals from S1 to S8, S3 to S6, S5 to S4 and S2 to S7. Hence, the operation modes while the input voltage in its opposing polarity are homologous to the explanations above. By doing the allocation and mapping in simple glue logic, the AC switch matrix is isolated and black-boxed to the conventional controller (i.e. microcontroller or linear controller) with respect to both the drive and feedback signals.

4.5. Design of a microcontroller dominated single phase to single phase matrix converter

In order to evaluate the proposed design, a single phase to single phase matrix converter has been built for verification. In this section, the prototype hardware will be described and software algorithm discussed. The built prototype converter is shown in Figure 4.19.

Figure 4.19. Prototype of proposed single-phase matrix converter

4.5.1. Prototype overview

A block diagram of the prototype matrix converter is shown in Figure 4.20. The power is sourced from a single phase AC mains power (i.e. 240 R.M.S, 50Hz in the UK) with filtering. The polarity of the input voltage is measured with the output (1 or 0) being passed to the middleware. A basic microcontroller is programmed with a control algorithm for a conventional full bridge converter with phase-shift control, the four output drive signals are distributed into the middleware. The middleware then maps these phase-shifted control signals to eight outputs which are connected to drive the 8 MOSFETs of a 2 x 2 switch matrix.

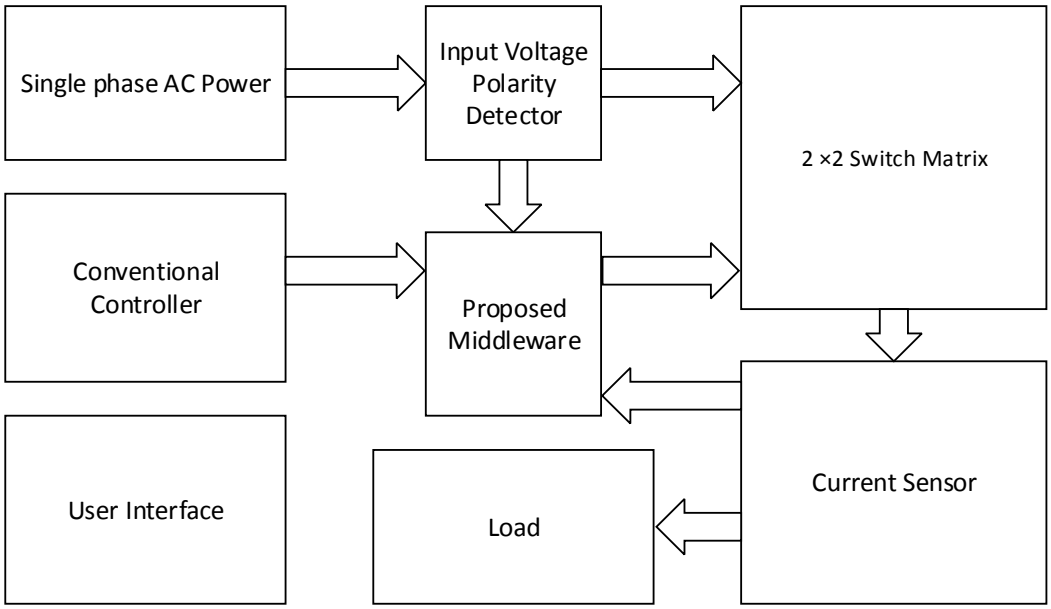


Figure 4.20. Block diagram of the matrix converter prototype

4.5.2. The hot side interface

The hot interface (AC mains connected) includes circuitry for over voltage and over current protection, sensors for power measurement, a relay-based switch for on-off control, and an inline filter to improve the system power factor.

4.5.2.1. The input protection

As shown in Figure 4.21, two-stages of protection are implemented. First, the small transient voltage will be absorbed by the bi-directional TVS diode connected after the Positive Temperature Coefficient (PTC) resettable fuse. When a transient occurs, the bi-directional TVS will fall into conduction regardless of the polarity of the input voltage and trigger the PTC. Meanwhile, when a long-term over voltage occurs, the GDT will start to discharge and blow the fuse. The main consideration of using a GTD in series of a varistor is using the varistor as an arc extinguisher. When the input voltage exceeds the overall hold-off voltage, both the varistor and GDT will conduct, so that the voltage across the varistor will start dropping and the varistor will turn into an isolator and extinguish the arc. The size and power rating for both the varistor and

GDT can therefore be minimised. Meanwhile, this connection also protects the GDT from degradation caused by repeated semi discharges where the current flow through the GDT does not trigger the main fuse.

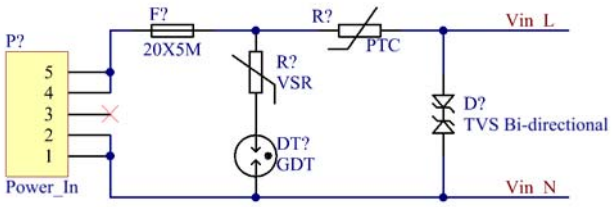


Figure 4.21. Input protection for the prototype converter.

4.5.2.2. The high side current sensing for power control

The primary control loop in this prototype is a constant power control loop, which samples the input power and voltage to calculate the power consumed. Compared to measuring the high-frequency output, the supply input measurement is less accurate, however it is simple to implement also allows monitoring of reactive power. In this design, the current flows through a CDS4050 transducer and gives 0.6V full range voltage output. Following the current transducer, an op-amp is implemented to amplify the current signal to an amplitude of 3.6 V peak, which is within range to be sampled by the system controller. The main consideration when choosing the op-amp is the offset voltage and its drift. For a generic op-amp, a 20mV input offset can cause a 400 W power control uncertainty.

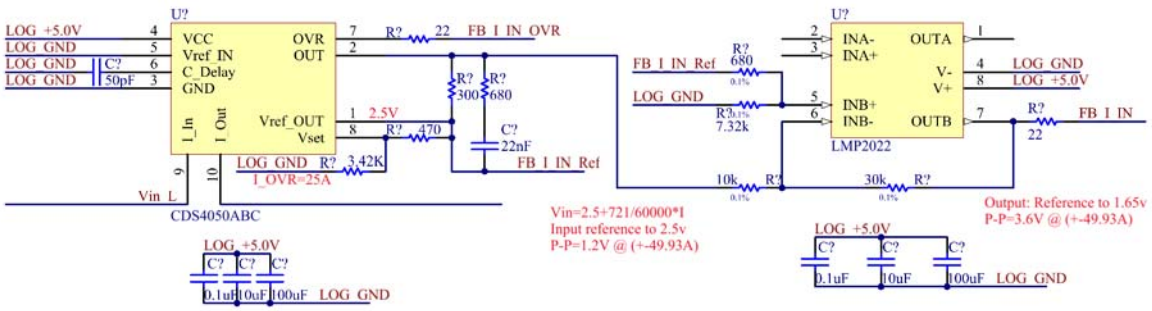


Figure 4.22. The high side current sensor and corresponded amplifier.

4.5.3. The switch matrix

Based on the analyses in chapter 1, the AC switch used in this design is formed by two back-to-back connected MOSFET. In order to drive this back-to-back connected MOSFET pair, an isolated drive solution is used. Two isolated power supplies commonly referenced to the middle point of this MOSFET pair, which provide a voltage swing between +15V and –9V to turn the MOSFET on and off, whilst a digital isolator feeds the control signal from the microcontroller to the gate drive chip. The gate drives comprise of two IXD609 low-side drivers which can provide a 9A peak source and sink current. A schematic showing half of the switch matrix is shown in Figure 4.23. As may be seen from the schematic the digital isolator is referenced to -9V instead of a commonly used 0V due to the same ground being required for the gate driver. Hence, a local linear regulator is used to regulate the 0V to -4V to power the isolator.

For a system designed to work at hundreds of kilo hertz, the propagation delay and the variance of this across the multiple drivers should be considered. The dead-time is initially programmed as 1uS, with the minimum allowed dead-time calculated by using the following equation, and us the value of T_{D_1} or T_{D_2} whichever is bigger:

When turn-off followed by turn-on

$$T_{D_1} = 2 \times T_{ISO_{VAR}} + 2 \times T_{DRV_{VAR}} + T_{Drv+} + T_{DRV_{RISE}} + T_{FET+} + T_{FET_{RISE}} - T_{Drv-} - T_{FET-} \qquad (4-1)$$

When turn-on followed by turn-off

$$T_{D_2} = 2 \times T_{ISO_{VAR}} + 2 \times T_{DRV_{VAR}} + T_{Drv-} + T_{DRV_{FALL}} + T_{FET-} + T_{FET_{FALL}} - T_{Drv+} - T_{FET+} \qquad (4-2)$$

Where $T_{ISO_{VAR}}$ is the Part-to-part skew time variance for the isolator. $T_{DRV_{VAR}}$ is the channel-to-channel variance between gate drivers. T_{Drv+} and T_{Drv-} are the turn-on and turn-off delay of the gate driver. $T_{DRV_{RISE}}$ and $T_{DRV_{FALL}}$ are the rising and falling time of the gate driver. $T_{FET_{RISE}}$ and $T_{FET_{FALL}}$ are the rising and falling time of the MOSFET. Using the Figure from the device's datasheet, T_{D_1} and T_{D_2} can be calculated as:

$$T_{D_1} = 2 \times 4.9 + 2 \times 20 + 40 + 35 + 95 + 158 - 42 - 290 = 45.8\text{nS} \qquad (4-3)$$

$$T_{D_1} = 2 \times 4.9 + 2 \times 20 + 42 + 25 + 435 + 180 - 40 - 105 = 586.8\text{nS} \qquad (4-4)$$

Ladder resistors and the blocking diode are used to adjust the turn-on and turn-off time for each MOSFET independently. For protection, a 4.7k resistor is connected between the gate and source of each MOSFET providing terminal protection, whilst a TVS diode is also connected in parallel to the 4.7k resistor to protect the MOSFET during a driver power supply failure. Furthermore, there is a varistor connected between the source and drain of each MOSFET providing over voltage protection.

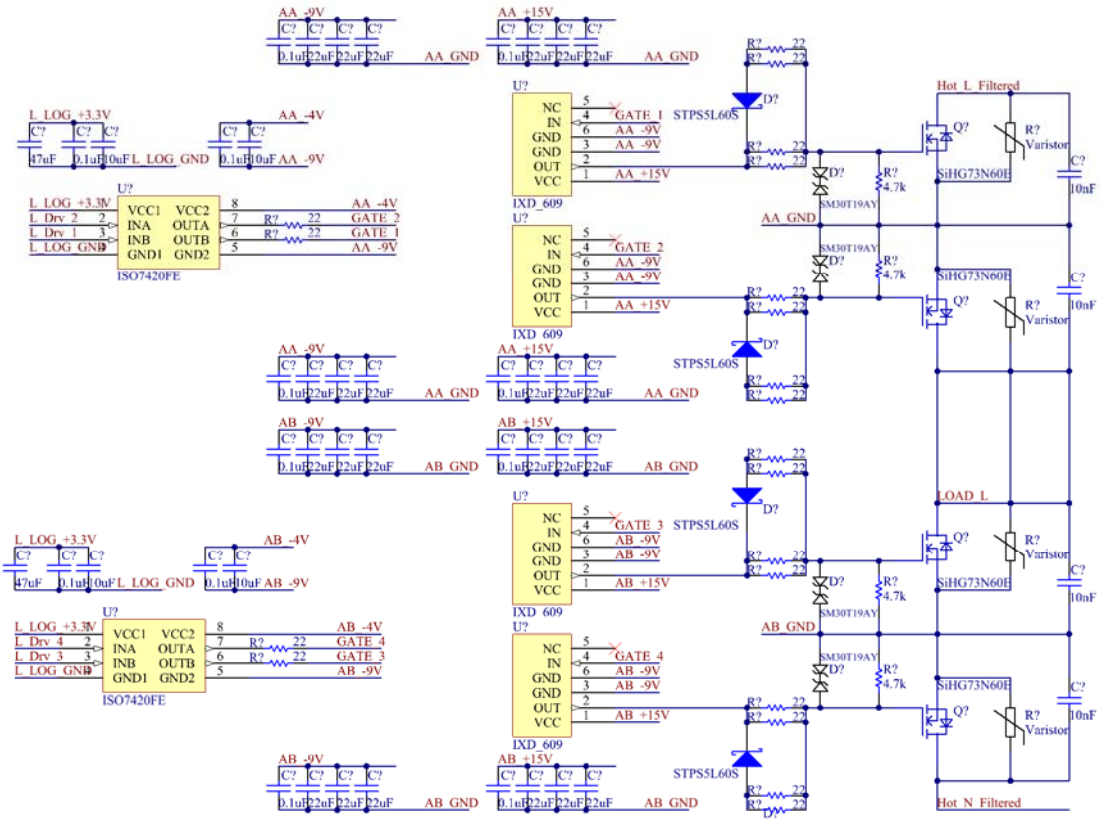


Figure 4.23. Schematic of the switch matrix, showing half of its total 8 MOSFETs.

To meet the power requirements of the circuit shown above (Figure 4.23), a total of 6 power sources are required. As shown in Figure 4.24 below, each group of 3 power supplier provides +15V turn-on voltage, -9V turn-off voltage and -4V logic power.

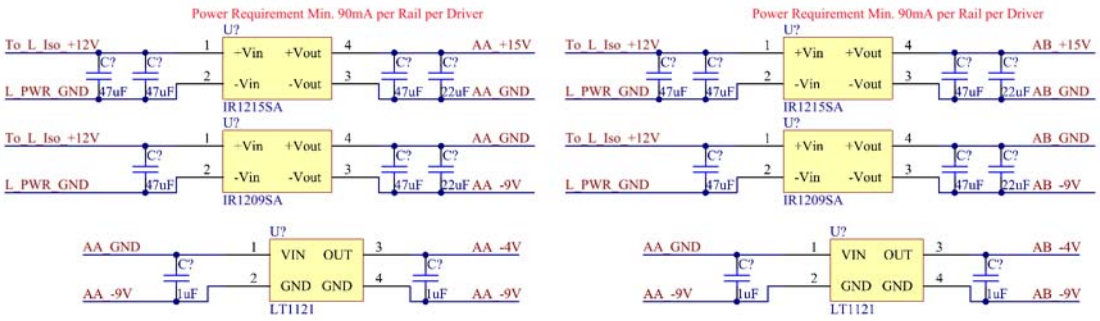


Figure 4.24. Schematic for two groups of power supplies for the MOSFET drive circuits

4.5.4. The middleware and input polarity detection

As the core of this microcontroller dominated matrix converter, the middleware requires 4 PWM signals from the microcontroller and a sign signal indicating the input voltage polarity. The input polarity detector schematic is shown in Figure 4.25. Not shown in the Figure is that the line voltage first passes through a trim capacitor for compensating the phase shift caused by the parasitic inductance of the current limiting resistor, the input capacitance of the comparator, and junction capacitance of the clamping diodes. On the hot side, the ladder-connected resistor network provides extra failsafe capability where the clamping diodes limit the voltage applied to the comparator. The comparator then generates both signals indicating the polarity of the input voltage and its complement. Those signals connect to the microcontroller via a digital isolator. The primary consideration is the speed (i.e. propagation delay) of the comparator and the digital isolator, the AD8561 used in this design and ISO7420 give a total propagation delay of 16ns which is negligible to a resonant converter working at hundred kiloHertz.

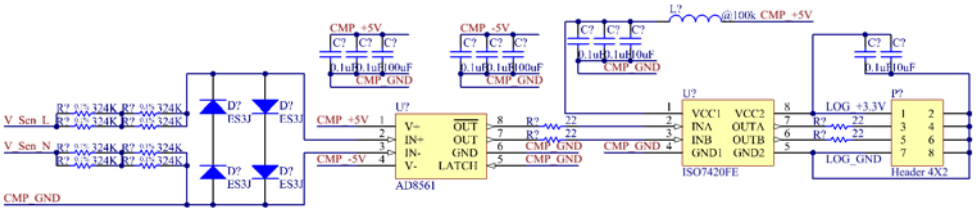


Figure 4.25. Schematic for the input voltage polarity detector.

The input voltage polarity detector is powered by a bipolar ±5V linear regulated power source, as shown in Figure 4.26. The main consideration for using a linear regulated power source is to avoid the switching noise from switch mode buck converters, which may affect the comparator where its power supply rejection ratio is limited. Also by using a conventional transformer, its poor high-frequency response could provide further resistance to the high-frequency noise from the AC power side.

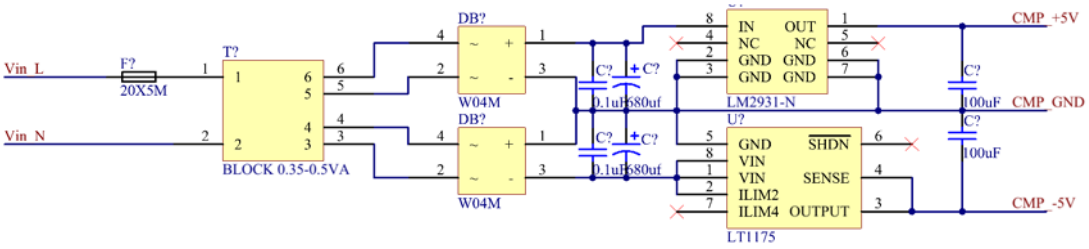


Figure 4.26 Power supplier for the input voltage polarity detector.

By feeding the input voltage polarity signal and the PWM signals from the microcontroller to the circuit shown in Figure 4.27, the required drive signals for the switch matrix can be generated. It is only required to use eight NOR-gates, therefore the middleware can be easily implemented with negligible cost and complexity.

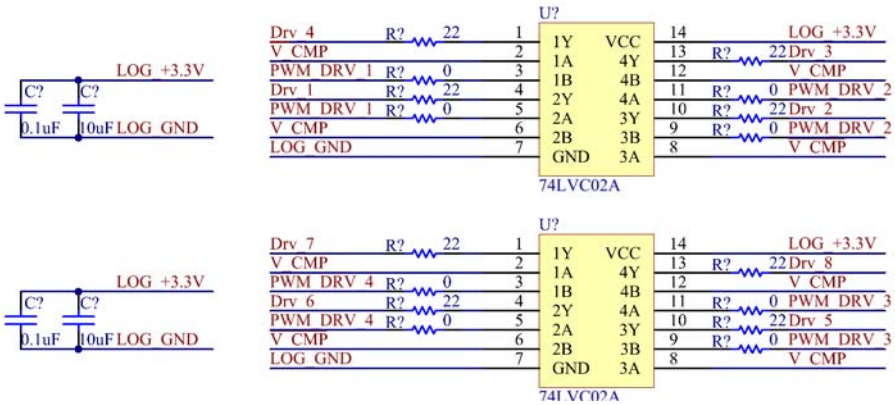


Figure 4.27. Schematic of the NOR gates based middleware.

4.5.5. The microcontroller

The microcontroller utilised in this prototype is an STM32F103VGT6 arm Cortex®-M3 processor. Figure 4.28 displays the LCD user interface when the microcontroller is running the proposed algorithm. The digital logic circuitry, including the user interface of this design, are fully isolated from the AC power supply by using digital isolators and optocouplers. With those isolations, the prototype converter is controlled by infrared remote controller and touch screen.

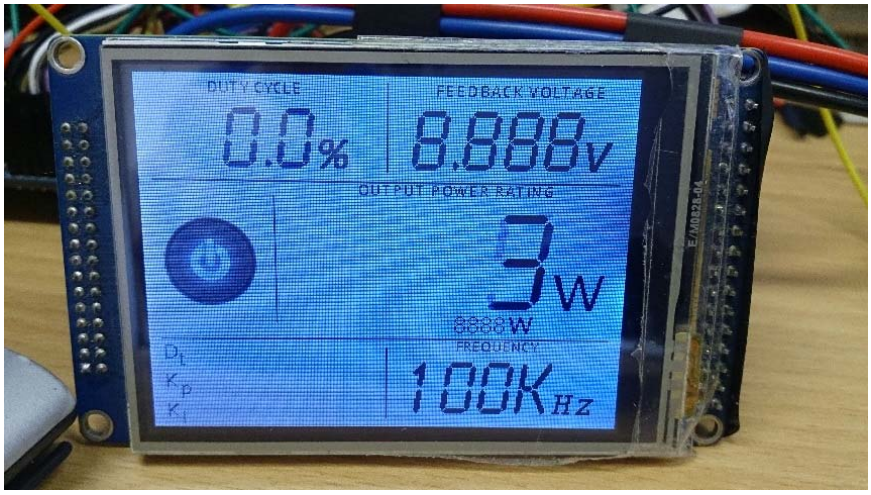


Figure 4.28. The user interface of the prototype converter.

4.6. Simulation and evaluations

4.6.1. Simulation

The converter shown in Figure 4.20 was modelled in the software package National Instruments Multisim. In the following section, the simulation setup and results will be provided.

4.6.1.1. Simulation setup

The Figure 4.29 shows the simulated schematic with the modified signal allocation and distribution circuit. During simulation, the zero crossing signal is provided by a comparator that is powered by a bipolar 5V supply. The comparator stage converts the output to TTL and provides a TTL logic high when the input voltage is positive, and logic low when the input voltage is negative. Additionally, the power switches are represented by eight voltage controlled ideal switches since the simulation is mainly focussed on the control of the converter instead of the working behaviour of the power switches. Also shown in Figure 4.29, the logic gate based middleware is presented as ideal switch-based logic, which assumes TTL level voltages in order to increase the simulation speed.

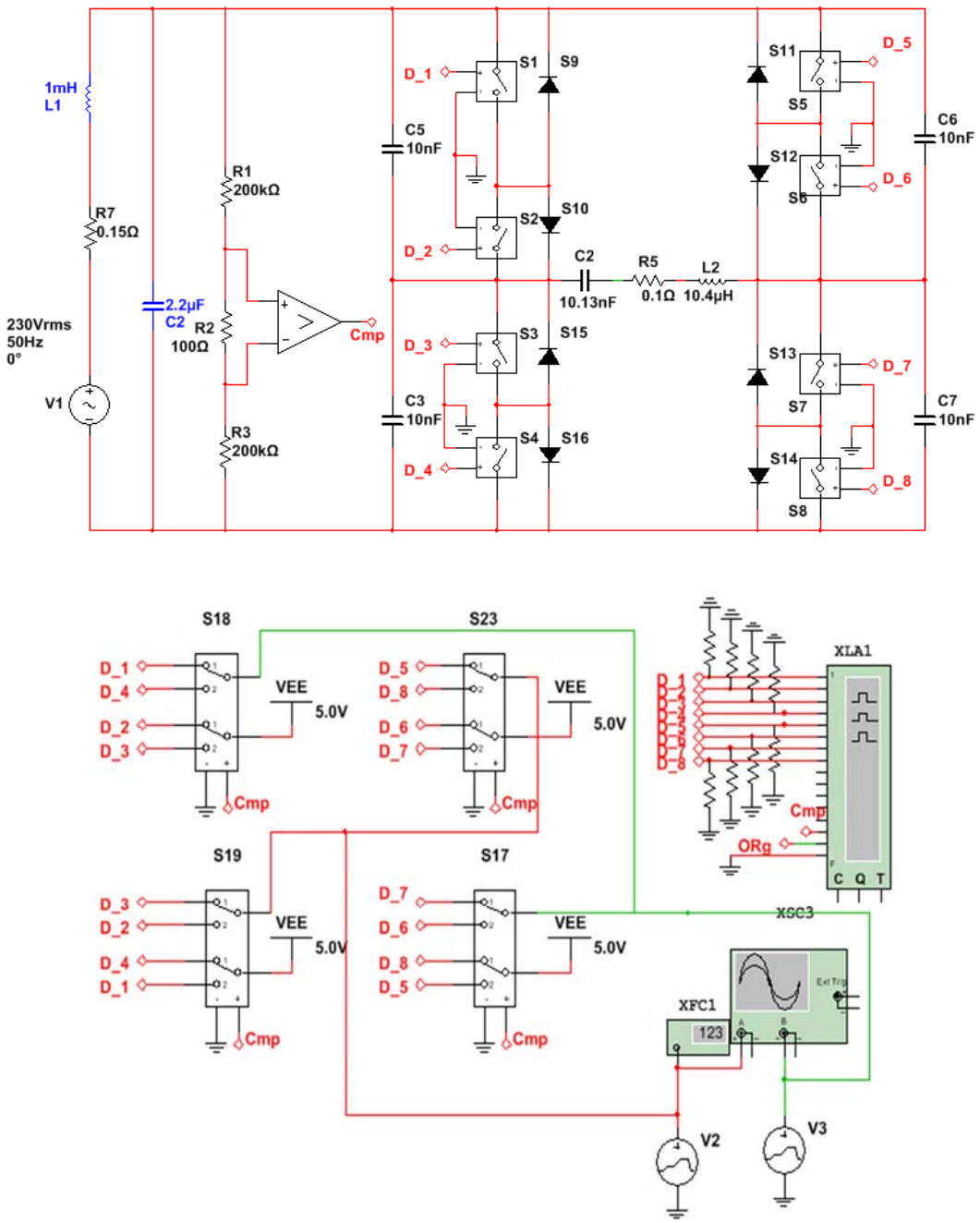


Figure 4.29. Simulated schematic of proposed induction heating system

4.6.1.2. Simulation result

For functionality testing using the simulation software, the phase-shifted drive signal has been replaced by PWM signals with constant duty cycle. Using the in-built logic analyser, Figure 4.30

shows the drive signals for the switch matrix before and after the input voltage changes its polarity from negative to positive. The Figure clearly shows that the middleware correctly provides the drive signals based on the input voltage and PWM outputs from the microcontroller.

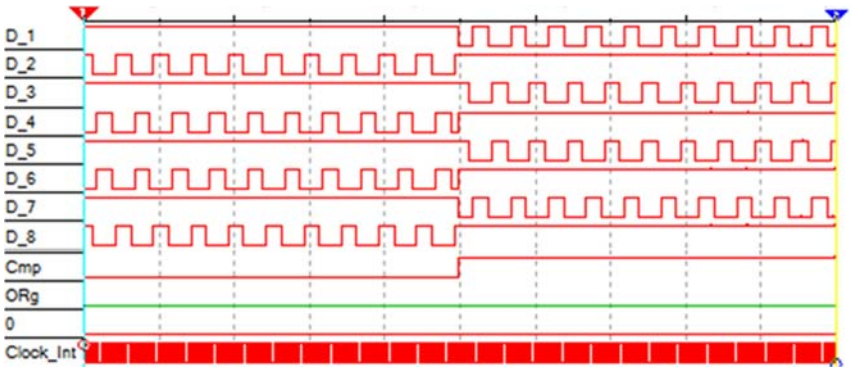


Figure 4.30. Simulated drive signals corresponded to the input voltage polarity.

The simulated waveform is provided by two virtual oscilloscopes. Based on the gate drive sequences showed above (Figure 4.30), Figure 4.31 shows the simulated output voltage and load current waveform, showing the expected near-sinusoidal load current (blue).

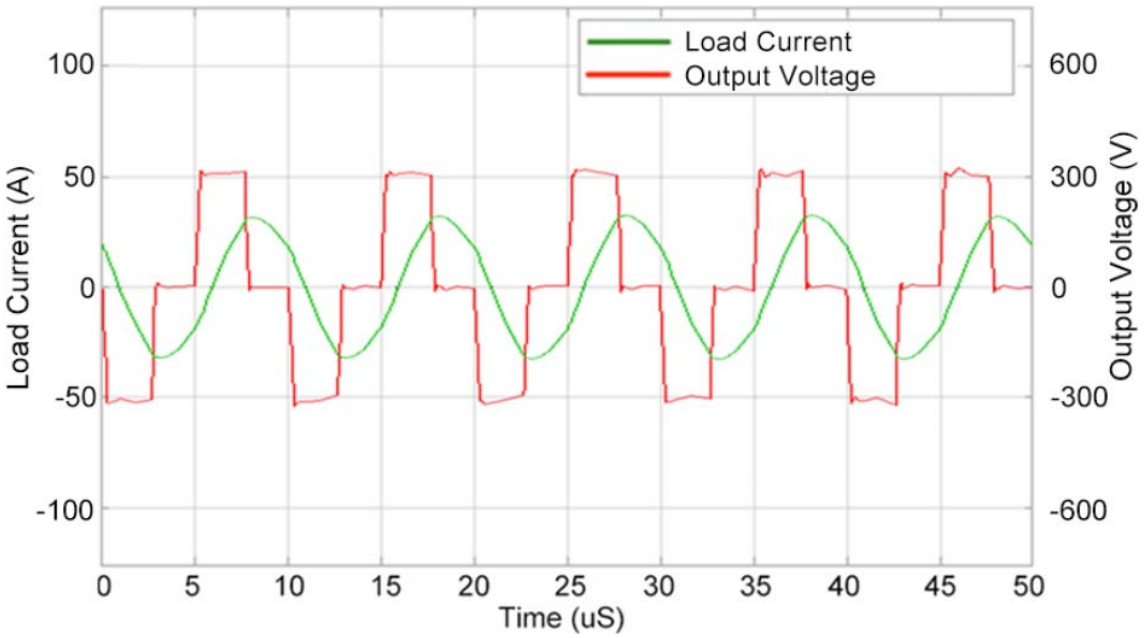


Figure 4.31. Simulated Results for the proposed matrix converter at 100 kHz

Figure 4.32 illustrates the simulated waveforms (input voltage and corresponding output) over a longer timescale, and as can be seen without a power control loop, the converter's output is continuously changing with the corresponded instantaneous input voltage. Meanwhile, it also can be noticed that the input voltage polarity detector provides the correct logic level to the allocation and mapping of the middleware circuit.

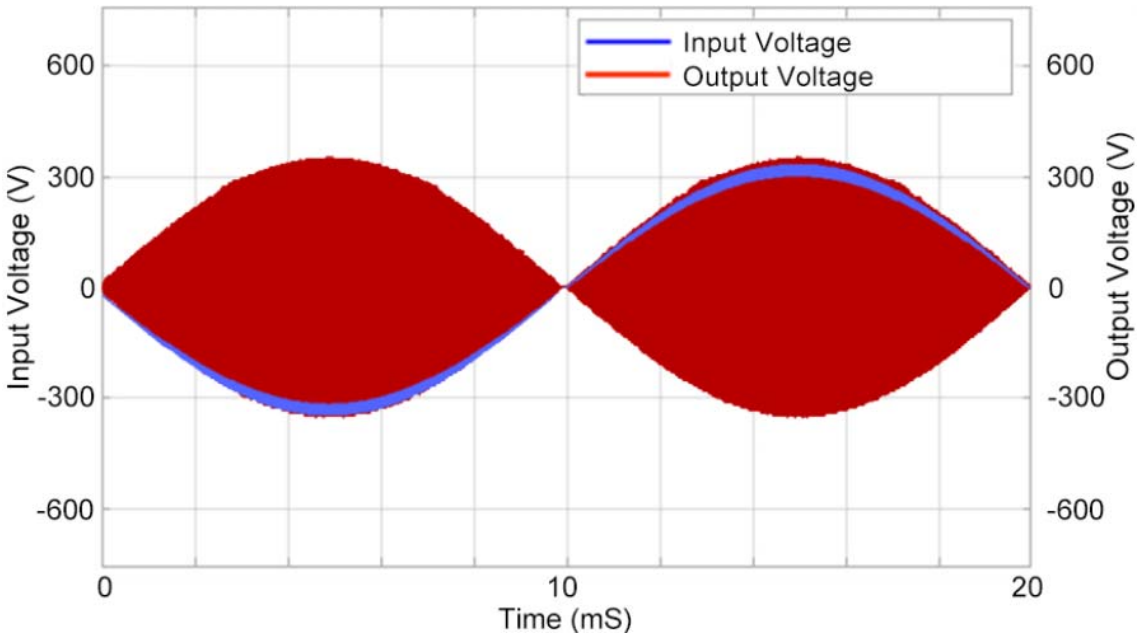


Figure 4.32. Simulated results for the matrix converter under test at 100 kHz

4.6.2. Hardware evaluation

The converter discussed above has been evaluated with an RMS input voltage of 230V. A simple LC resonant tank consisting of a 47uH inductor and 69nF (47nF in parallel with 22nF) capacitor was used as the test load. Figure 4.33 shows the waveforms consisting of the input voltage and corresponding output, the converter is driven by a 100kHz PWM signal. The converter's output follows according to the input voltage and is continuously changing with the corresponded instantaneous input voltage

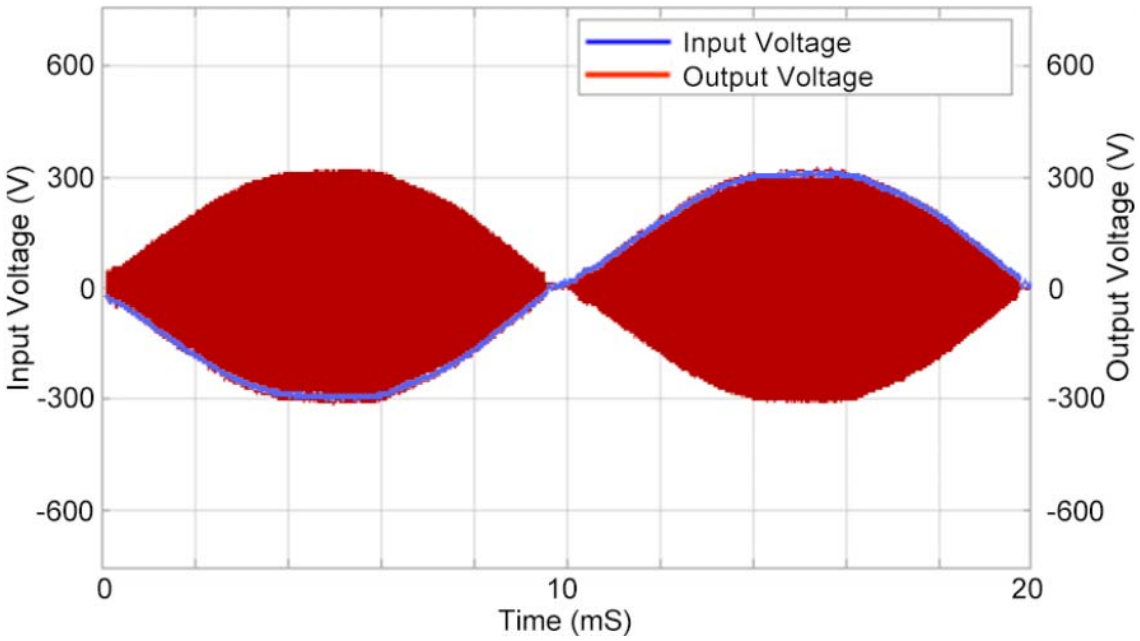


Figure 4.33. Measured results for the proposed matrix converter at 100 kHz

Based on the drive signals shown in Figure 4.6, Figure 4.34 shows the waveforms of the output voltage and coil current; the expected sinusoidal current flows through the load.

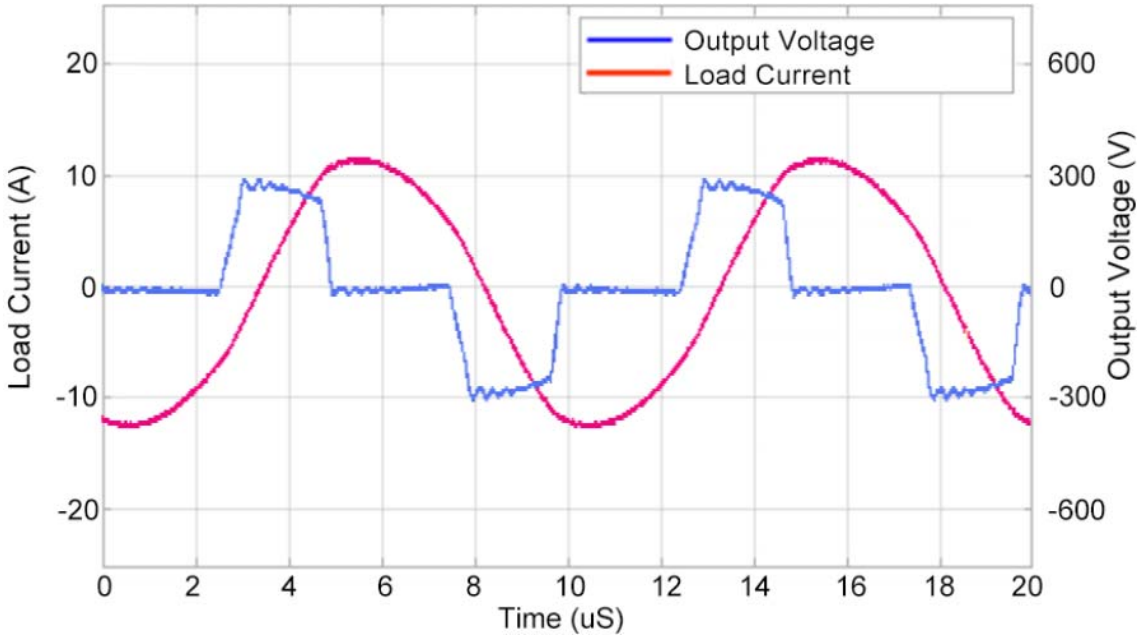


Figure 4.34. Measured result for the proposed matrix converter at 100 kHz.

Figure 4.35 illustrates the measured waveform consisting of the output voltage and corresponded output current. As may be seen from the waveforms, without the closed power control loop, the converter's output is continuously changing with the corresponding instantaneous output current.

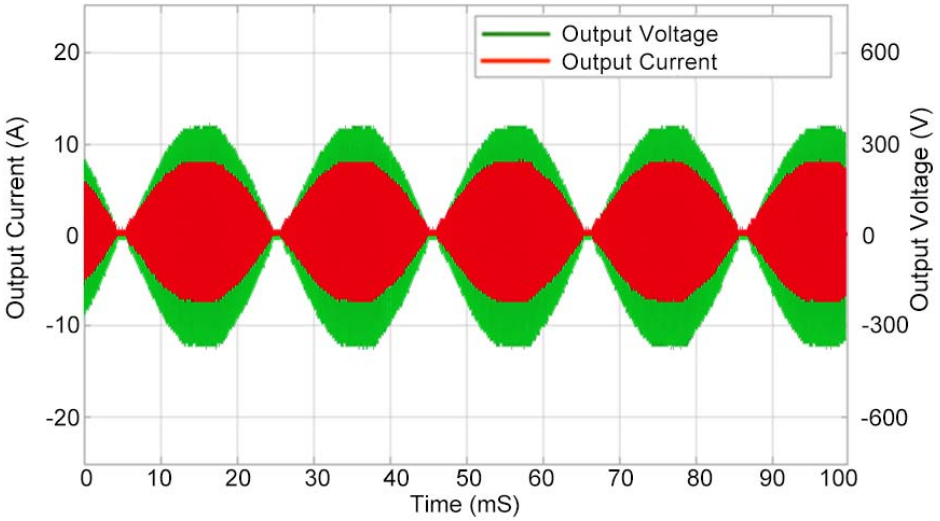


Figure 4.35. Measured results for the proposed matrix converter at 100 kHz.

The prototype converter has also been designed to work across a wide range of frequencies, Figure 4.36 shows the output voltage and load current waveforms of the prototype converter driven by 500 kHz PWM signals.

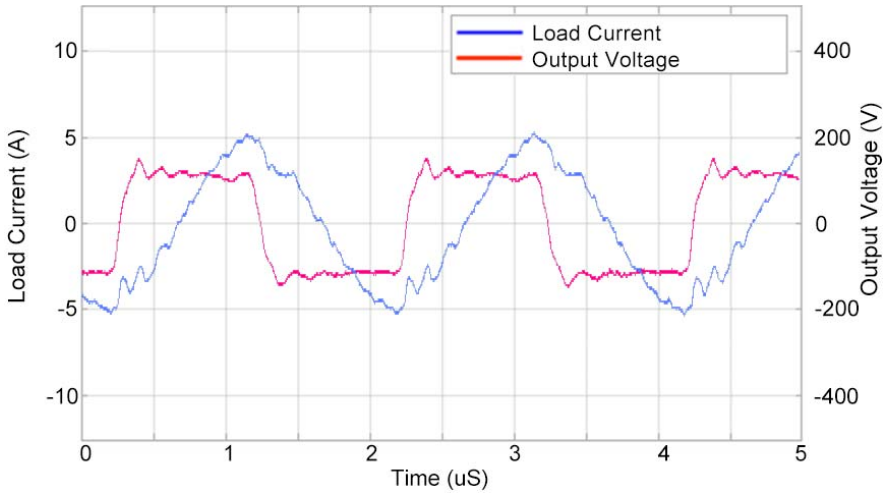


Figure 4.36. Measured results for the proposed single-phase matrix converter at 500 kHz.

One of the most significant advantages of the matrix converter is that the input power factor can be fully controlled. Figure 4.37 shows the input current waveform of the proposed converter, which may be seen as the expected sinusoidal waveform (the current waveform was measured by a current probe).

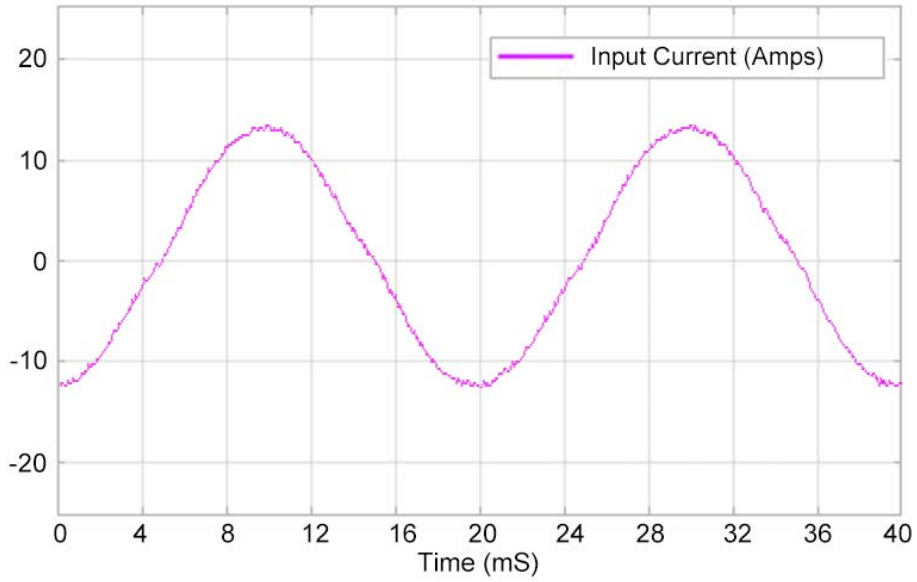


Figure 4.37. The input current waveform of proposed single-phase matrix converter.

4.7. Summary

In this chapter, the implementation of the full-bridge controller based matrix converter by using logic gate based drive signal allocation circuit is presented. The allocation circuit is flexible for any single phase to single phase matrix converter. A matrix converter to be used for evaluation has been built and evaluated. As can be seen from the test result, the logic chip based drive signal allocation and mapping middleware, properly distributes and allocates the drive signal from a conventional controller to the power switches of single-phase matrix converter. This proves the methodology of employing a widely-used PWM controller through middleware to control the operation of a matrix converter, and also provides a simple and cost-efficient approach to utilize the advantages of single-phase matrix converters.

5. Matrix converter controlled wireless power system and its WPT power receiver

5.1. Introduction

Charter 4 provided an analysis of middleware based single phase matrix converter design that allows a matrix converter to be controlled as if it was a full-bridge converter. However, to achieve the design of a matrix converter based wireless power system, several modifications and improvements need to be made. This chapter will describe the frequency selection in terms of balancing the switching frequency of the power converter and the physical size of the transmitting and receiving coil. Then the design of the coil itself will be presented where two types of coil will be introduced. The topology of the desired wireless power system will then be described.

The resonant frequency of the receiver may vary with tolerances in manufacture or changing conditions at the load. In this chapter, an experimentally obtained mechanism will be introduced which provides the necessary approach to control the frequency of the converter to match the resonant frequency of the receiver on-the-fly. Meanwhile, the next section of this chapter introduces a novel wireless WPT receiver design. The new design provides a high function density, as it provides 300W power conversion and can actively balance charge up multiple battery cells on a PCB sized 55*78.5 mm.

5.2. The wireless power transceiver coil

To evaluate the design of a WPT system, the wireless power transceiver load should first be considered. In this section, the design of the wireless power load and construction of its receiver coil will be described.

5.2.1. Choosing the load inductance based on the resonant frequency.

As illustrated in Chapter 2.2, Figure 2.9 shows the trade-off at different frequencies of system efficiency and power capability with respect to coil inductance (at a fixed quality factor of 10). The chart shows that a large inductor is required at the lower switching frequency to maximise the efficiency whilst a smaller inductor value is required at the higher frequency. As the switching frequency will be limited by the driving converter, the first step when designing a wireless power system is to determine at which frequency the system will operate on. Generally, at a very low operating frequency, the converter could operate at a better efficiency, but the transmitter and receiver coil require such a large inductance that an air cored coil may physically be large and heavy. At high operating frequency, the size and weight of the transmitter and receiver coil can be reduced but the efficiency of the power converter will be lower due to the increased switching losses. Especially, for a wireless power system that is rated at tens of kilowatts, the selection of power switch will be limited to high power but low-speed semiconductors.

The prototype WPT system in this thesis is designed for a power rating of up to 3kW for technical validation and may be expanded to tens of kilowatts, where IGBTs may be deployed for the power converter. Considering that the operating frequency of an IGBT is generally below 100 kHz, an operating frequency at 50 kHz level is selected.

5.2.2. Design of the Secondary resonator

By referencing Figure 2.9, in order to achieve maximum efficiency and loading ability, well balanced coil inductance can be calculated at around 100 uH. However, in order to reduce the

size and conduction loss of the transmitting and receiving coil, 50 uH coils are implemented which reduce weight and size by 50 percent, but sacrifice 10 percent efficiency and loading ability in doing so.

The second resonator, essentially an LC resonant tank, should be designed first since the transmission frequency of the matrix converter depends on the resonant frequency of the second resonator. Since the quality factor of the circuit is relatively large, a non-polarized high voltage rating film capacitor should be considered as the resonant capacitor. The receiving coils, however, can be differently shaped, in order to feature a proper magnetic circuit for the specific application. Meanwhile, in order to pick up the fluctuated magnetic field from the air, a planar coil may be chosen as appropriate, since at the operating frequencies of the given wireless power system, the conductor core does not contribute significantly to the overall current rating. Bundled thin conductor may have to be applied to prevent the skin effect introduced losses. However, for low power applications, a PCB coil could be used and has the benefit of being easy to manufacture and low cost. For high power applications a Litz wire base planar coil can be implemented, whereby the inductance can be calculated using the following equation:

$$\mathrm{L(uH)} = \frac{25(R_o + R_i)^2 N^2}{76R_0 - 36R_i} \qquad (5-1)$$

Where, R_o is the outer diameter (m) of the coil, R_i is the inner diameter (m) of the coil, and N is the number of turns which will be calculated from the given coil inductance.

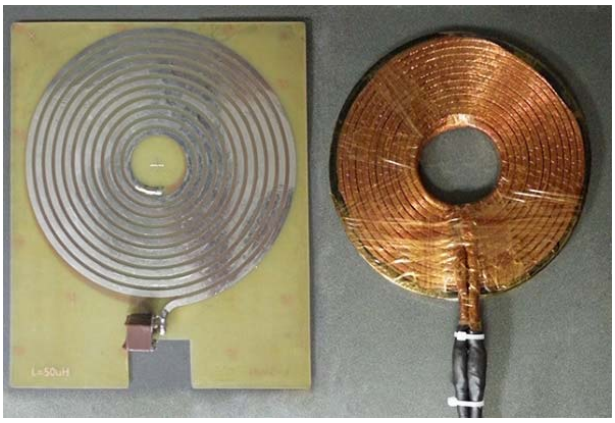


Figure 5.1. PCB coil and Litz wire coil for WPT system

Two types of coils were used in this design, as shown in Figure 5.1. The PCB coil shown on the left side is made by 1 oz fibreglass reinforced PCB then topped with solder. The overall thickness is about 200μm, 35μm from the original copper with 150μm topped tin. The effective skin depth of this PCB based coil can be calculated by using the equation below, which is around 300μm, the uncertainties are mainly due to composite materials and the uneven solder topping.

$$\delta = \sqrt{\frac{\rho}{\pi \times f \times \mu}} \qquad (5-2)$$

Where ρ is the resistivity of the conductor in $\Omega\mathrm{m}$; f is the frequency in Hertz; μ is the absolute magnetic permeability of the conductor. The absolute magnetic permeability $\mu = \mu_o \text{ x } \mu_r$. Where $\mu_o = 4\pi \text{ x } 10^{-7}$ H/m

On the right hand of Figure 5.1, the Litz wire constructed power coil design is shown, this is for higher power systems. The coil is made using a 52 core twisted Litz wire with each independent strand 250μm in diameter. Since the equivalent diameter can also be calculated as 1.8 mm, this 2.5mm^2 copper wire can carry approximately 25 Amps of current.

5.2.3. The design of the first resonator

The coil of the first resonator acts as the power transmitter. In this design, the first resonator is a serial LC resonant circuit, with a resonant frequency higher but close to the resonant frequency of the second resonator. The output of the matrix converter is a square wave with a frequency equal to the resonant frequency of the second resonator. Hence, the first resonator will operate in its inductive region to realise zero voltage switching, and sinusoidal current will flow through the coil to generate a magnetic field. Meanwhile, heat-resistant materials, such as Kapton tape and Polytetrafluoroethylene (PTFE) sheet have been chosen, since the circulating current of the prototype converter may exceed 30A and the coil temperature may exceed 150 degrees in heavy circulated conditions, as shown in Figure 5.2.

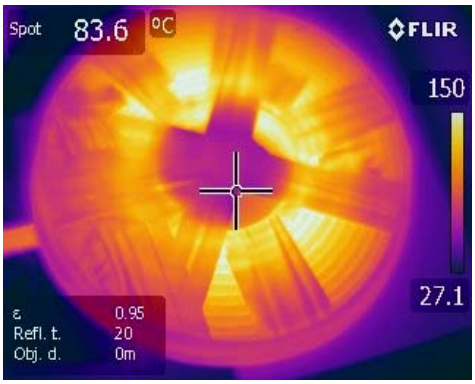


Figure 5.2. Thermal image of a working Litz wire coil.

5.3. A wireless power system utilising the matrix converter

The wireless power system discussed in this chapter is dominated by the matrix converter described in Chapter 5. By connecting the wireless power transmitter illustrated in the section5.1, matrix converter dominated wireless transfer can be realized.

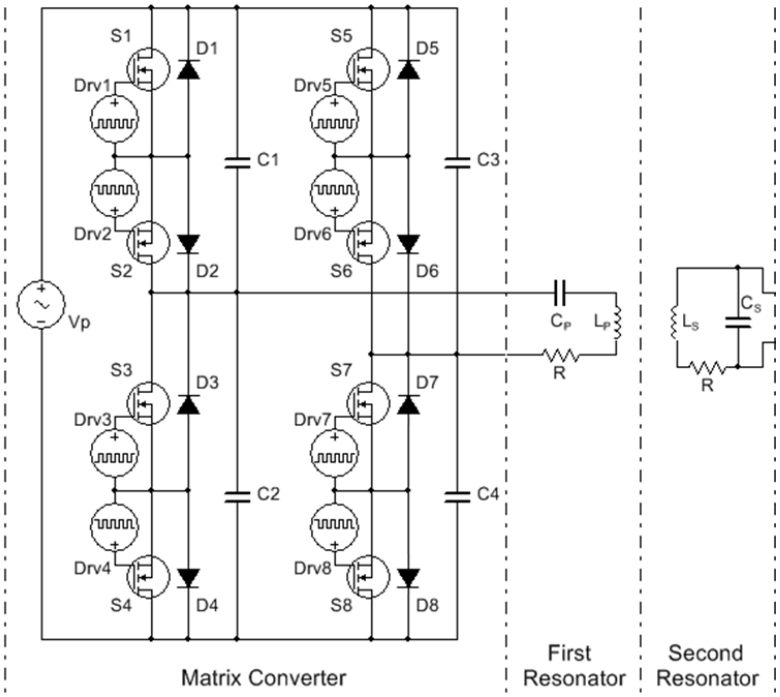


Figure 5.3. Simplified schematic of the proposed wireless power system, showing the connections.

A simplified schematic can be found in Figure 5.3 that shows the proposed topology of the WPT system. The matrix converter is implemented using an STM32F407 microcontroller as described in Chapter 5. The four PWM signals from the microcontroller are fed into the middleware and the resultant eight drive signals are then used to drive the switch matrix as shown in Figure 5.4. The switch matrix of this prototype is formed by eight SiHG33N60 MOSFETs. The output of the switch matrix is connected to a resonant tank that consists of a 50uH planar coil and 220nF film capacitor. On the receiver side, a parallel resonator formed by a 200nF film capacitor and 50uH planar coil is constructed to receive the power.

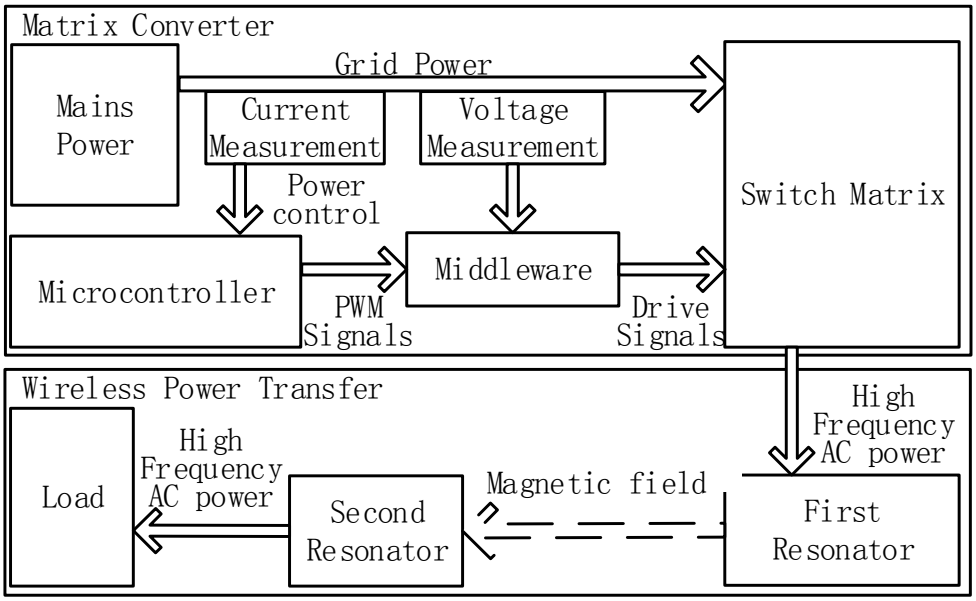


Figure 5.4. Block diagram of proposed WPT system.

The wireless power system discussed above has then been built and evaluated with an RMS input voltage of 230V. The prototype hardware and the position of the coils are shown in Figure 5.5, with the coils being approximately 15 cm apart. On the transmitting side, the coil on the bottom radiates the required magnetic field, whilst on the receiving side, the top coil picks up the magnetic field and resonates with the transmitting coil.

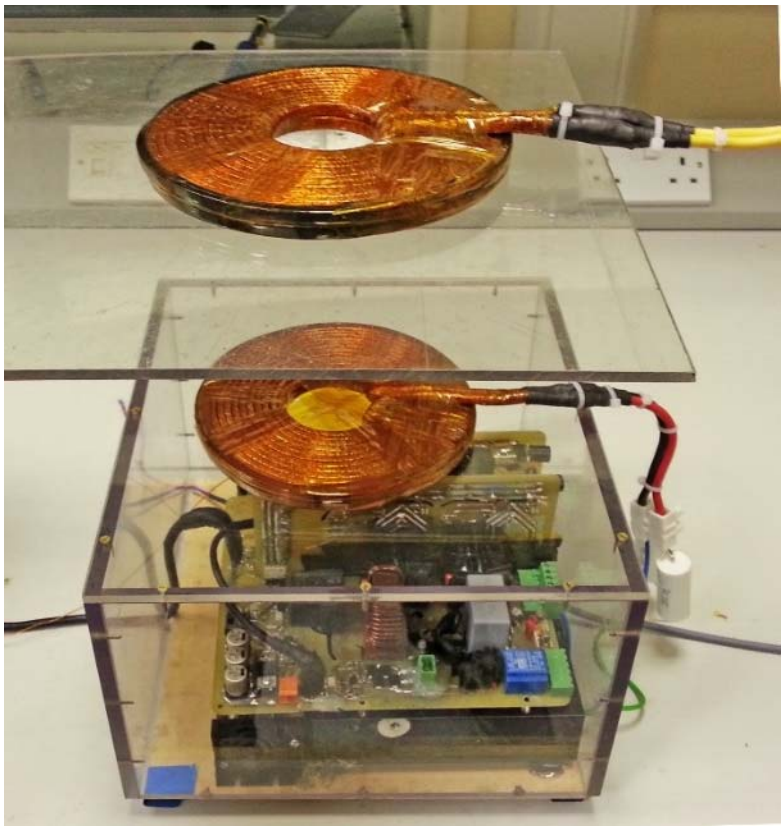


Figure 5.5. Prototype wireless power system.

5.4. Tuning the wireless power system to better performance

As discussed in Chapter 2, maximum system efficiency is achieved when $\mathrm{F_O}$ (converter output frequency) is equal to the self-resonant frequency of the LC resonator ($\mathrm{F_{LC}}$) which is formed by the receiving coil and its resonant capacitor.

$$\mathrm{F_O} = \mathrm{F_{LC}} \qquad (5-3)$$

The frequency split phenomenon of SCMR based wireless power needs to be considered, which explains the two optimised operation frequencies (F_{LP} and F_{HP}, for lower optimised operation frequencies and higher optimised operation frequencies) that can be found in a WPT system. Several kinds of regulation control approaches can be implemented for wireless power application such as: (a) Low-Frequency Control (LFC), (b) High-Frequency Control (HFC), (c) Pre-regulation, and (d) Post-regulation [5-1].

The LFC method controls the output frequency (F_O) of the converter from 0 to F_{LP} where the output voltage will increase and researches its maximum point when $F_O = F_{LP}$ [5-2 and 5-3]. Similarly, the HFC approach controls the converter output frequency from F_{HP} to a higher frequency, where the output voltage decreases from its maximum to zero. Base on the working theory illustrated above, both LFC and HFC approach requires given F_{HP} or F_{LP} which need individual measurement and calculation. Moreover, the optimum working points are still rarely achievable due to the changes of inductance or capacitance caused by temperature variations, mutual inductance and component tolerances.

During experimentation, a phenomenon was observed that shows the matching of F_O and real-time self-resonant frequency can also be achieved by comparing the phase difference between the current of the first resonator and the output voltage of the second resonator. Using this approach would negate the need to measure the real resonant frequency. Figure 5.6 shows the relationship between the system efficiency (this includes the power converter and the wireless power transmission) and the phase shift angle of transmitting current (It) and receiving voltage (Vr). As can be seen, the system efficiency is proportional to the phase difference between It and Vr.

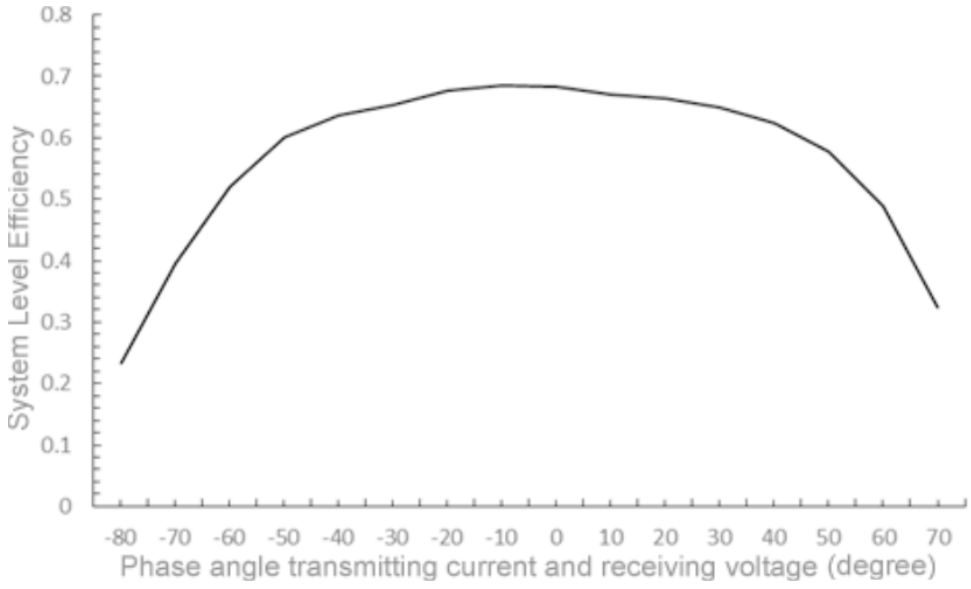


Figure 5.6. System efficiency against phase shift angle of transmitting current and the receiving voltage.

Figure 5.7 shows the Figure zoomed in about the x-axis towards zero degrees, showing a 60-degree span highlighting that when the phase shift angle is tuned to approximately zero degrees, the system achieves its maximum efficiency.

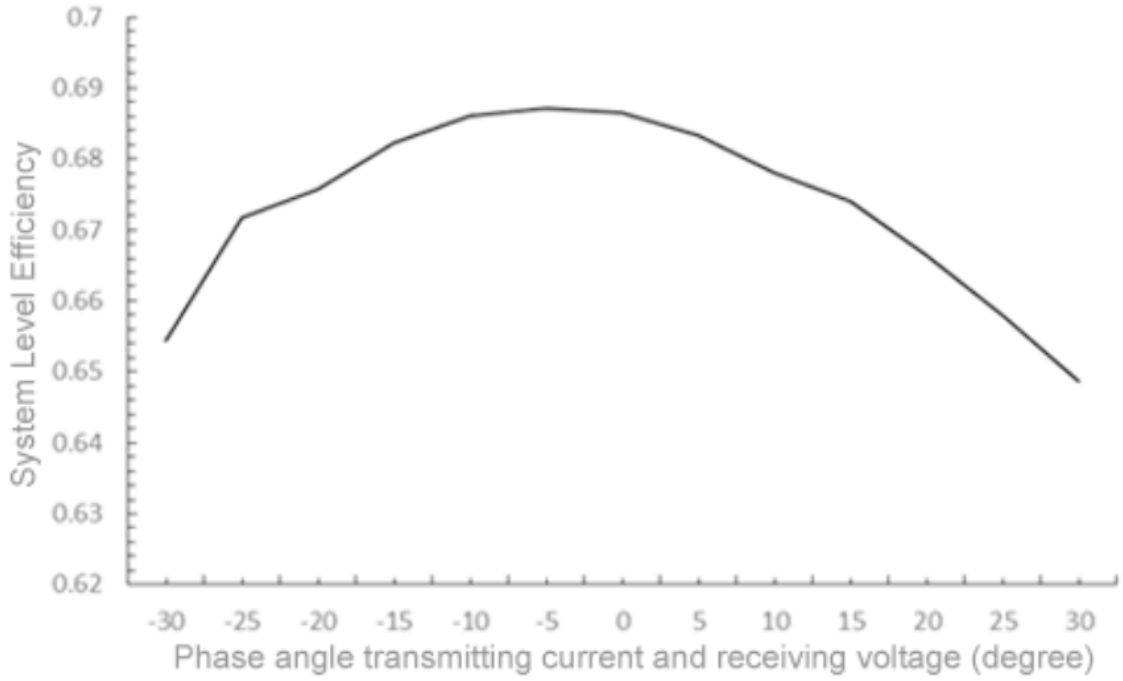


Figure 5.7. System efficiency against phase shift angle of transmitting current and the receiving voltage in the 60-degree span.

As shown in Figure 5.8, by using an oscilloscope to continuously measure the transmitting current and receiving voltage, during the test and evaluation, the phase angle between the transmitting current and receiving voltage has been tuned to the minimum in order to obtain the optimised operation point. Based on this approach, the following chapter establishes a closed-loop controller to automatically adjust the transmitting frequency without manual intervention.

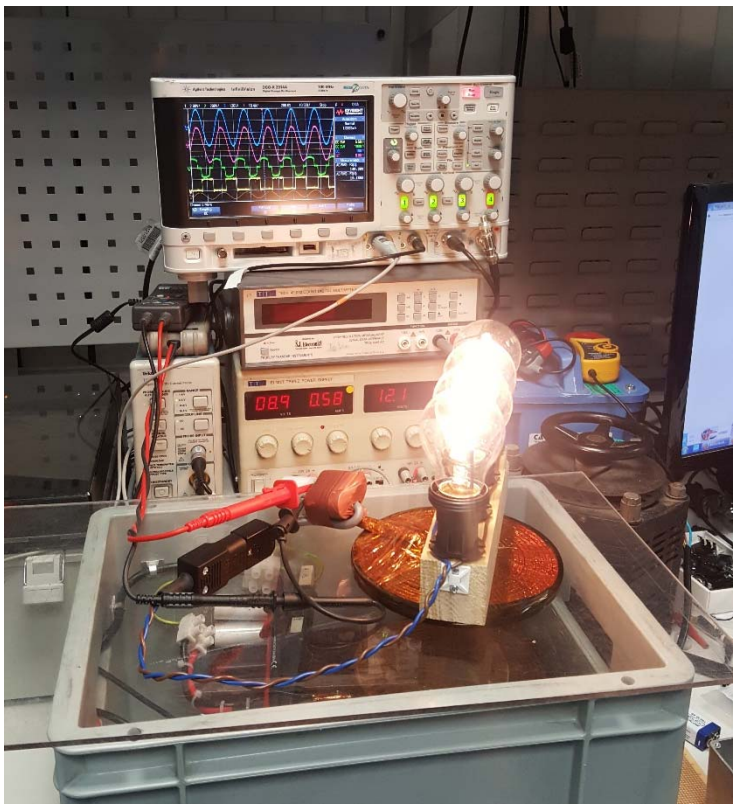


Figure 5.8. Tuning the wireless power system with the help of an oscilloscope.

5.5. The WPT receiver

In order to demonstrate the WPT system, a novel WPT receiver was designed to charge the battery of a drone. The WPT receiver was designed to be provided with 330W rated power and to fit on the underside of a drone using a PCB size of 55*78.5 mm (Figure 5.9). The PCB included a 15A fully programmable battery charger that could charge a 5000mAh drone battery at fast charge rate whilst being able to deliver additional power to the motors to enable the drone to hover. The onboard Battery Manage System (BMS) could measure the real-time current, voltage, and state of charge of the battery and the power consumed by the motors. Using this data and real-time cell voltages, the circuit could actively balance the battery cells using 0.5A active balancing current. The PCB incorporates 128Mb of on-board RAM with room for expansion using an SD card that can provide storage for data logging. This data and other information can be

transmitted through the onboard 433.92 MHz Amplitude Shift Keying (ASK) modem. Furthermore, a GPS IC mounted on the PCB provides altitude data to the BMS and timing signal for the maximum efficiency point tracking algorithm that will be discussed in a later section. A PCI-E slot is available to add daughter cards. In the following section, an overview of this receiving module is provided.

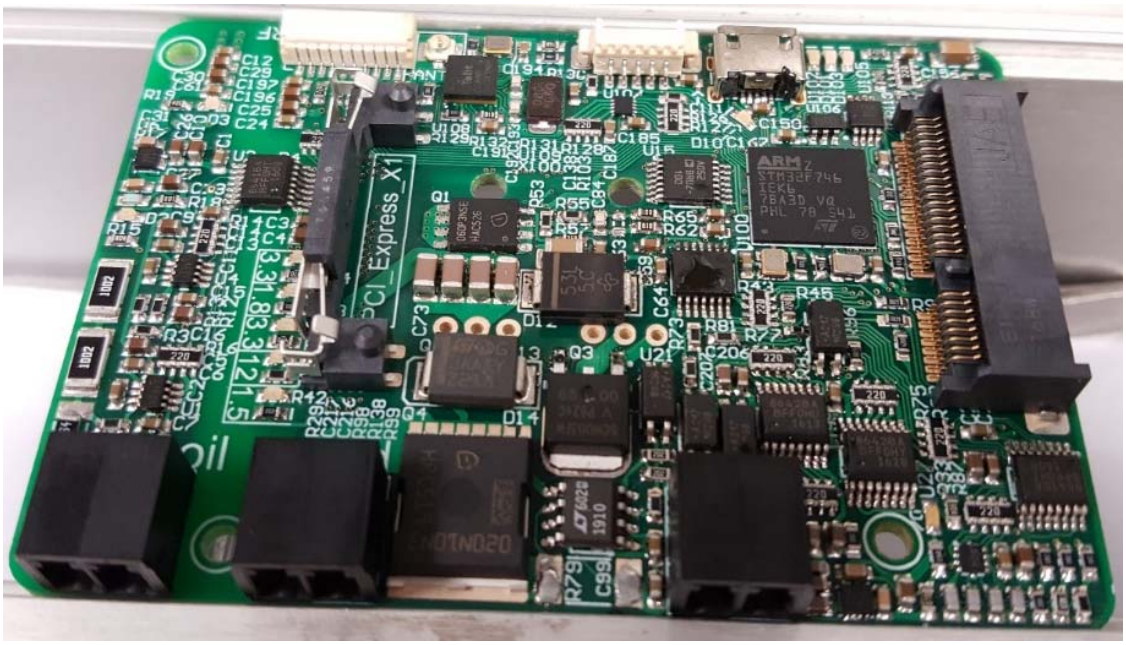


Figure 5.9. Desired WPT receiver

5.5.1. The receiving resonator interface

The high-frequency AC power from the receiving resonator is firstly rectified by a diode bridge then an LC filter will filter out the fluctuating voltage and provide a DC voltage of approximately 350V. This DC voltage is then fed into a measurement and isolation circuit as shown in Figure 5.10 below. The isolated DC to DC converter is implemented (one the back side of the PCB) to convert the 350V DC voltage to 12.5V DC. As shown in Figure 5.10, a ladder resistor network divides the input DC voltage by a ratio of 1:197, so that the maximum voltage fed into the data converter is 1.78V and given a margin of 52V (maximum input voltage of the data converter is 2.048V) for any overshoots or transients. Compared with a conventional two resistor voltage

divider, using a ladder resistor network provides extra protection to the data converter if one of the lower resistors is disconnected. A digital isolator is used to isolate the high voltage side from the microcontroller. For safety consideration, on the PCB, a creep distance of 4mm is established to avoid any possible arcs or leakages, as shown in Figure 5.11. The measurement that this circuit provides, feeds into a hill climbing method to track the maximum efficiency point as will be described in Chapter 6.

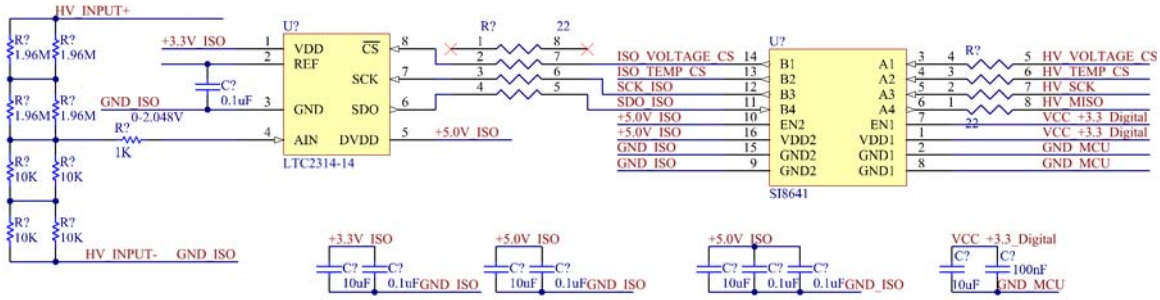


Figure 5.10. Input voltage measurement and isolation.

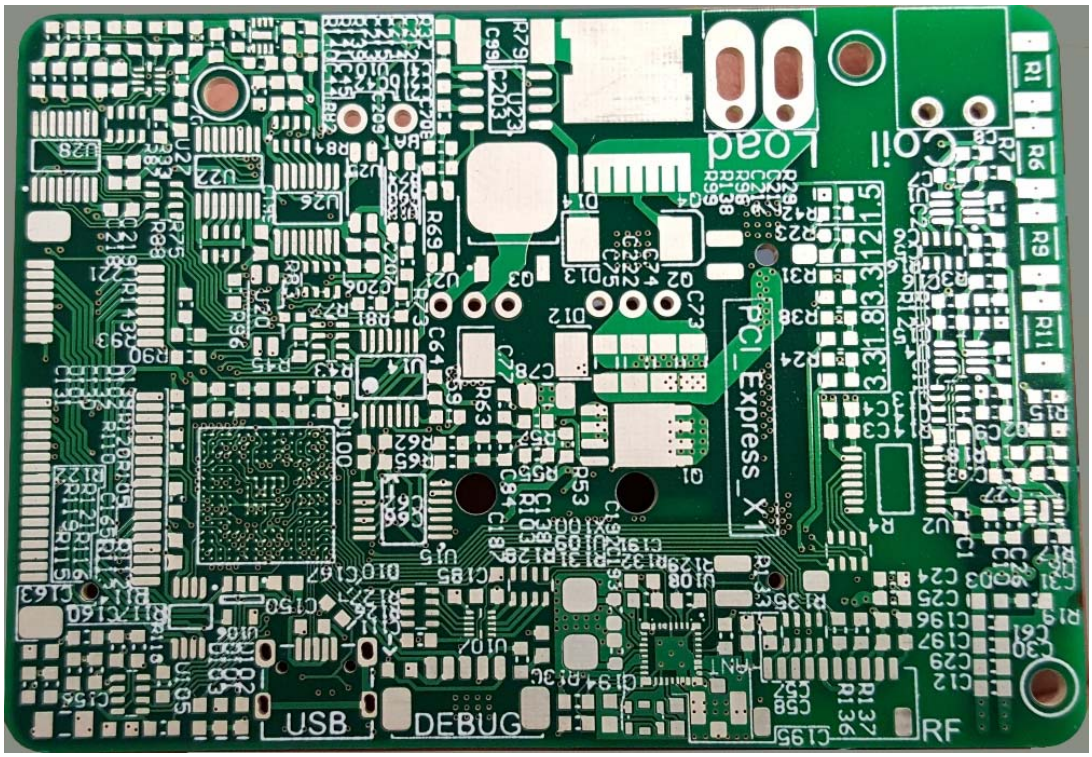


Figure 5.11. The receiver PCB, the creep area is from the label “RF” to the top screw hole.

5.5.2. The battery charger

Since the application of this WPT receiver is designed for drones, fast charging the onboard battery with sufficient current is desired, and the ability to adjust the charging current and terminal voltage is also necessary. In order to provide 15A battery charging capability, this design utilises a constant voltage, constant current battery charger controller with external switches. A separate buck converter controller is implemented instead of using the microcontroller for safety purposes, since the buck converter controller could keep regulating the charging progress even if the microcontroller is frozen. The synchronised buck controller operates at 550 kHz to convert its 12.5V DC input to charge the battery with higher than 90% efficiency. The P-type MOSFET fitted can isolate the battery when no power is applied to the WPT receiver and prevent the battery from depletion caused by reverse powering the system.

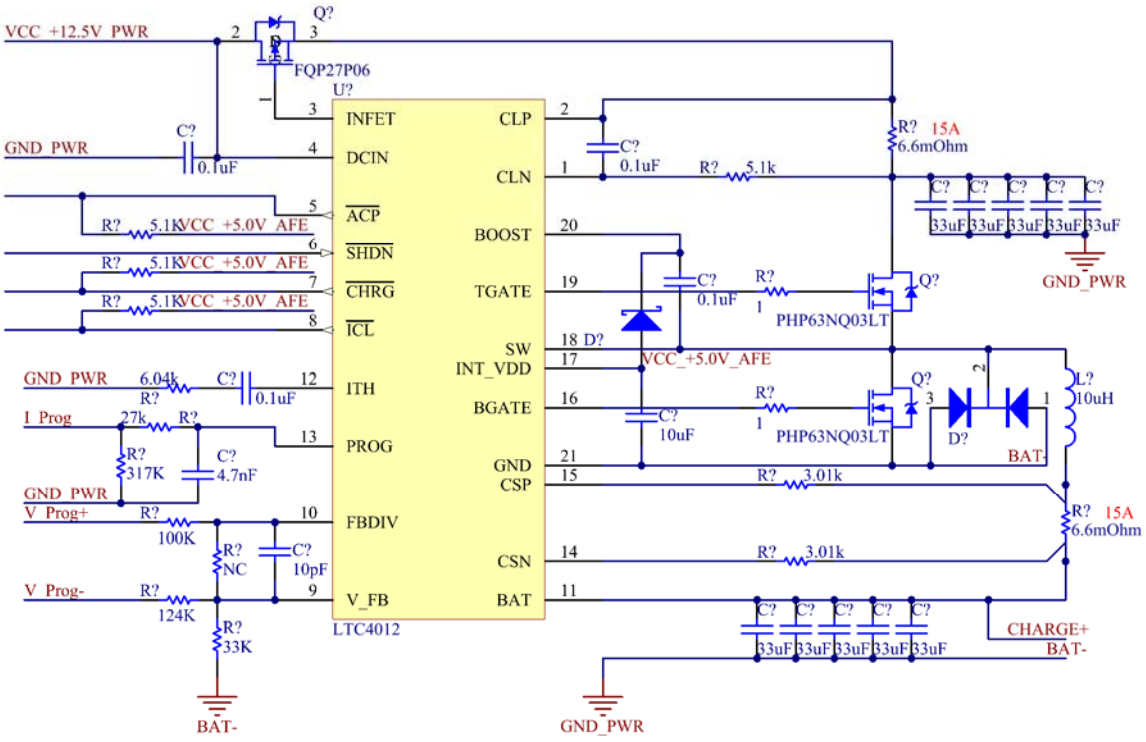


Figure 5.12. The synchronised buck converter used for battery charger.

Initially, the charging terminal voltage and maximum charging current are programmed through

the resistors connected to PROG and V_FB pins. In order to program the charging voltage and current on-the-fly, two digital potentiometers are used to adjust the resistance that appears on the targeted pins, shown in Figure 5.13.

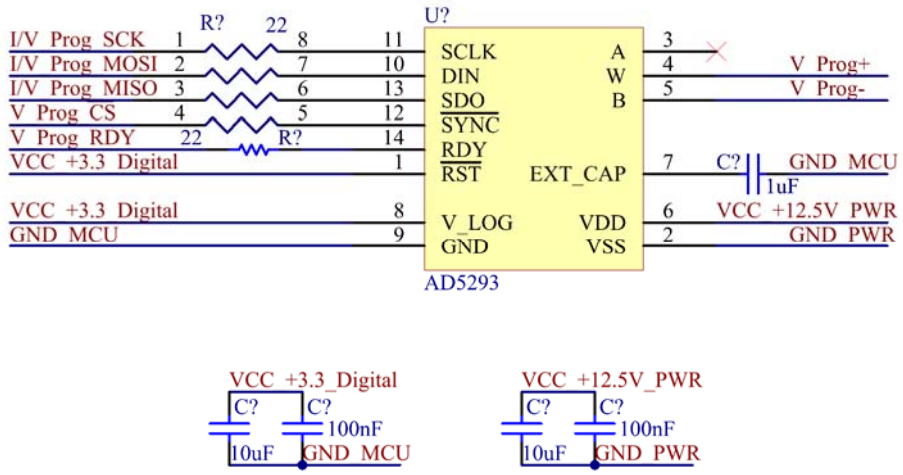


Figure 5.13. The digital potentiometer fitted to program the charger's terminal voltage.

5.5.3. Battery balancer

The desired WPT receiver is fitted with an active battery balancing algorithm. Before the battery pack can be balanced, measurements to the voltage of each cell are required. The following schematic in Figure 5.14 shows the circuitries used to measure the cell voltages. In order to utilise a single-ended data converter, all the measured voltages are referenced to the battery ground. By dividing the serial-connected cell voltages by 1/2, 1/3 and 1/4 the individual cell voltages can be then calculated by subtracting the cell voltage ahead of it. The cell voltages are sampled at 16 bits in length which gives a voltage resolution better than 1mV. To avoid ground noise that affects the sampling accuracy, the digital signals are isolated so that the current will only return via their locally fitted LDO regulator which reduces the ground layer complexity.

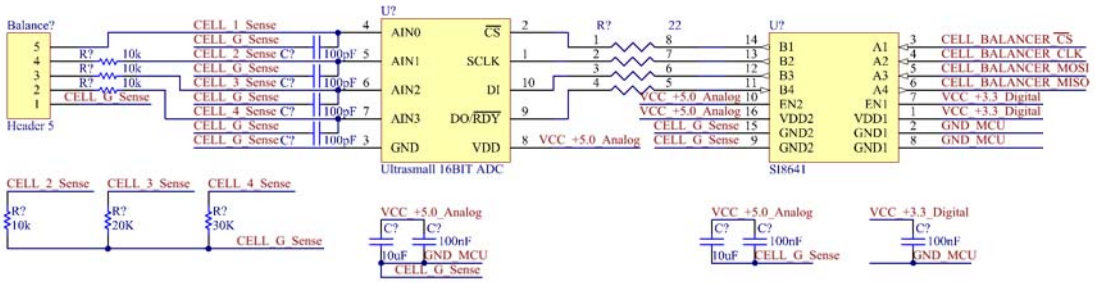


Figure 5.14. Data converter for cell voltage measurement.

By comparing the cell voltage measured above, cells with higher voltage can then be individually discharged. Figure 5.15 shows the active balancer featured in this design. By using optocouplers with solid-state relay output, each cell of the battery pack can be easily discharged by switching on its corresponding optocoupler. Two 15 ohm surface mount resistors connected in parallel then dissipate the superfluous energy which reduces the power dissipated in each resistor to around 1 watt.

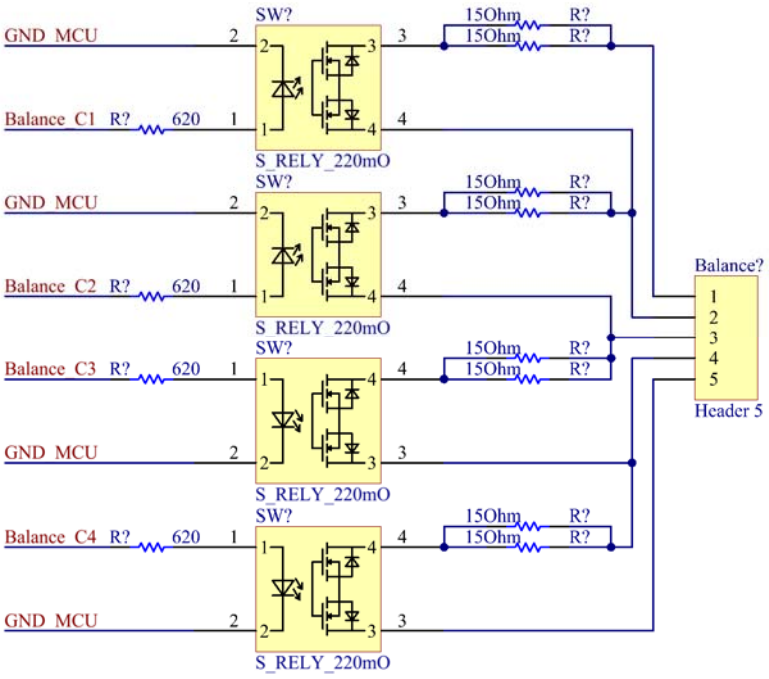


Figure 5.15. Ultra-small active balancer with 500mA balancing current.

5.5.4. Power, charge and energy monitor for battery charging and discharging

In order to enable the onboard BMS to monitor and control the status of the battery pack, several parameters need to be measured and recorded. As can be seen from Figure 5.16, by means of its internal 20X amplifier, the differential input of the data converter is used for current measurement where the signal can be directly coupled from the 6.6mΩ shunt resistor. The positive input of the differential input also works as the voltage measurement node; whilst there will be voltage errors caused by the shunt resistor, these will be removed later by the measurement software. Using the measured voltage and current value, together with the 8MHz timing base, the corresponding charge and energy data can then be calculated. Utilising a separate monitor circuit off-loads multiple floating-point calculations from the microcontroller. Moreover, using a specialised chip will also improve the measurement accuracy, since the timer used to calculate charge rate and energy will not be interrupted or delayed as may happen in the microcontroller.

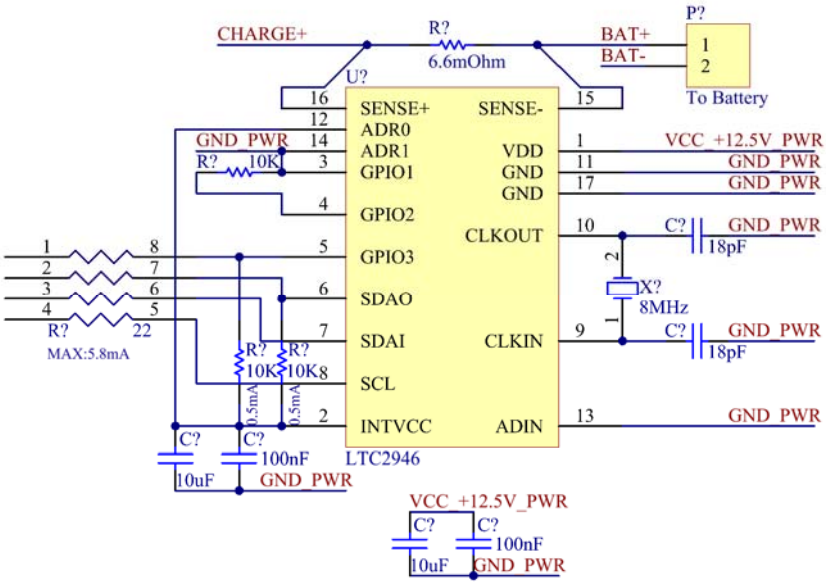


Figure 5.16. System monitor implemented for current, voltage, charge and energy measurement.

5.5.5. Discharging Power Path Control

A potential use case of the WPT receiver may require charging the battery whilst the drone hovers using power through its motors, therefore the WPT receiver should be able to deliver power in excess of that required to charge the battery. By using a high-side MOSFET driver, the onboard microcontroller can select whether the motors are to be powered by the battery or directly by the WPT receiver. The high-side driver also senses the current flow through the switch and cut-off the MOSFET when the current exceeds 15A and provides a resettable fuse mechanism. Before the MOSFET driver, a monitoring circuit similar to the schematic shown in Figure 5.17 is incorporated to measure the current, voltage etc. that flows through to the load.

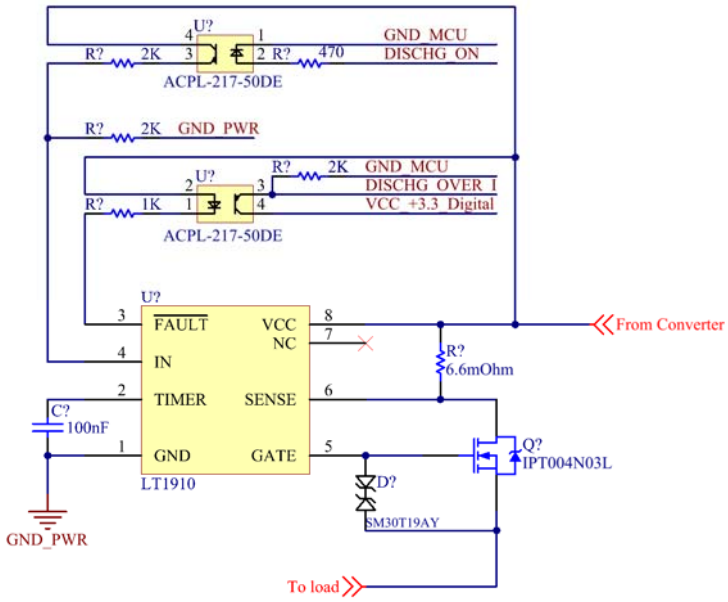


Figure 5.17. High side switch for load power path control

5.5.6. Data storage

Two types of storages devices are designed to storage the measurement along with flying and charging. The serial-connected flash memory showing on the left hand of Figure 5.18 provides

128MB of readily accessible non-volatile memory. No file system has been instantiated to access the onboard memory so that this data can easily be used by the BMS algorithm. Limited by the physical size of the onboard flash memory, mass data accumulated during operation is transferred to the SD card. A FAT32 file system is deployed onto the SD card so that the card can be accessed by using a computer. The software implemented on the microcontroller generates data files written in an open Extensible Markup Language (XML) format, this allows the data to be structured in an appropriate way for analysis offline.

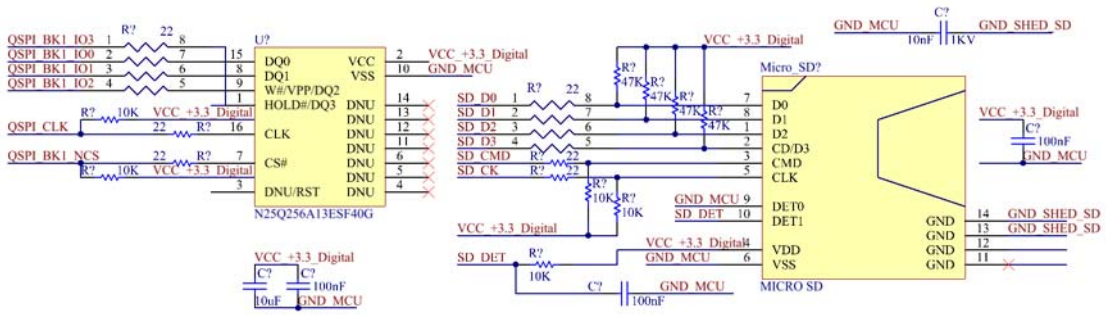


Figure 5.18. Onboard system memory.

5.6. Evaluation and verification

The prototype WPT system using the drone receiver board described in this chapter is fitted to a drone. The drive signal from the microcontroller is shown in Figure 5.19. This phase shift controlled signal controls the switch matrix through the middleware introduced in Chapter 4 and generates a high-frequency AC output that drives the power transmitter.

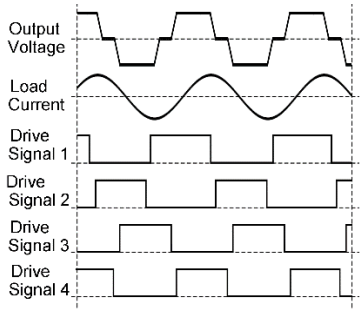


Figure 5.19. Phase-shifted drive signal from the microcontroller.

Figure 5.20 shows the physical construction of the quadcopter test platform and as can be seen the receiving coil is installed under the drone. The white wire on the left-hand side is the antenna for the 433.92MHz communication.

Figure 5.20. Evaluation of the WPT receiver on a drone platform, showing the example topology of the docking (wireless distance < 20cm) charging approach.

Based on the drive signals shown in Figure 5.19, Figure 5.21 shows the evaluated waveform depicting the converter's output voltage and the current flow through the transmitting coil. As shown in the waveforms, the sinusoidal current flows through the coil, this leads to a generated magnetic field in the transmitter coil.

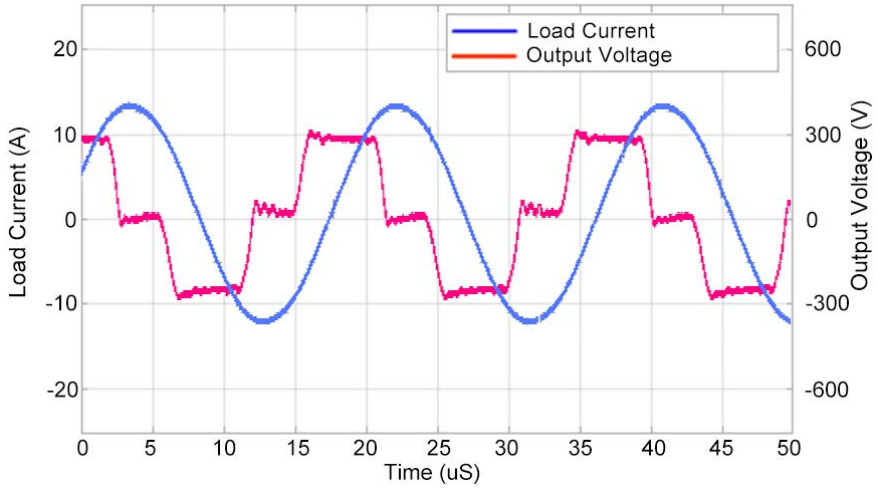


Figure 5.21. Measured result for output voltage and coil current.

On the receiving side, the coil picks up the magnetic field and resonates with the transmission coil. Figure 5.22 shows the transmitting voltage and receiving voltage waveform.

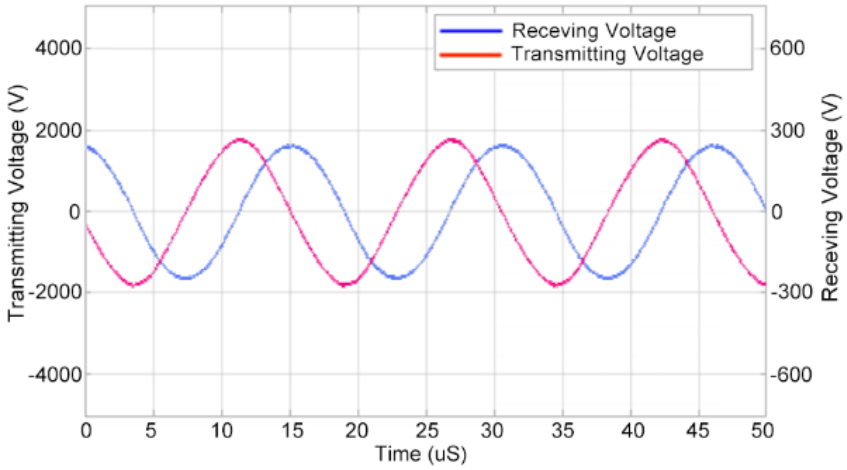


Figure 5.22. Transmitting and receiving voltage.

When the load is directly applied to the WPT receiver, the coil voltage drops as current rises. Figure 5.23 shows the voltage and current waveform of the wireless system working at 1kW output power. Both the transmitting and receiving side are shown.

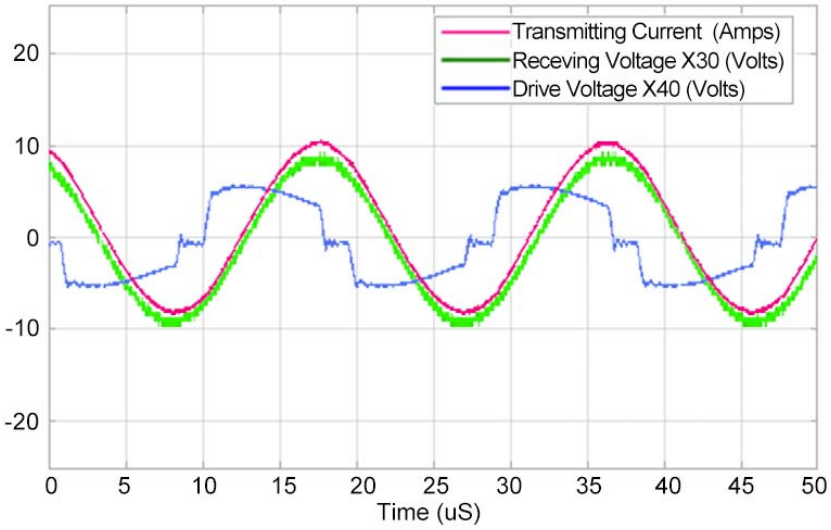


Figure 5.23. The waveform of WPT system. (Green: Output Voltage from the receiver; Blue: Output voltage from the converter; Red: Transmitting resonant current.

5.7. Summary

In this chapter, the realization of matrix converter based wireless power system is presented. The matrix converter is controlled by a generic microcontroller with simple middleware consisting of a number of logic gates. A wireless power system to be used for evaluation has been built, and it has been shown that the design effectively transfers energy from an AC power source to the desired load. The microcontroller based control methodology in this chapter provides a low-cost approach to devices where traditional forms of control would be prohibitively complex and expensive. This chapter also provides a practical approach to tuning the power transmitter and its local converter so that the output frequency of the power converter could match the resonant frequency of the receiving LC resonator and improve efficiency. Using this mechanism, a new maximum efficiency point tracking methodology will be developed in next chapter, which provides automatic compensation to components tolerance, mutual inductance and temperature introduced resonant frequency changes.

5.8. Reference

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[5-2] B. H. Waters, et al., “Powering a ventricular assist device (VAD) with the free-range resonant electrical energy delivery (FREE-D) system,” Proc. IEEE, vol. 100, no. 1, pp. 138–149, Jan. 2012.

[5-3] T. Riccardo and A. Costanzo, “State-of-the-art of contactless energy transfer (CET) systems: design rules and applications,”Wireless Power Transfer, vol.1, pp. 10-20, Mar. 2014.

6. Phase Shift Control Based Maximum Efficiency Point Tracking (MEPT) in Resonant Wireless Power System

6.1. Introduction

Having investigated the resonant frequency turning methodology in Chapter 5, it was shown that the resonant frequency of the power receiver can be estimated by maintaining a constant phase angle between the transmitting current and the receiving voltage. Similar to the Maximum Power Point Tracking (MPPT), the resonant frequency turning methodology could contribute to the system efficiency and establish a MEPT control approach. However, several issues have to be overcome in order to apply this methodology. This chapter will investigate the technical challenges when designing a wireless power system that can maximise efficiency its efficiency through control. Specifically, the complexity of wirelessly comparing the phase of two analogue signals and the communication bandwidth requirements to implement a phase shift controlled maximum efficiency point tracking controller.

As introduced in the previous chapter, the basic topology of a wireless power system utilising MEPT consists of the drive converter, transmitting resonant tank, receiving resonant tank, and the circuitries for transmitting current and receiving voltage monitoring with its phase angle detection. This chapter then addresses a small modification to the phase signal comparison allowing those two signals to be sampled on both the power transmitter and receiver independently without the need for use of wired communications for the measurement. Specifically, this chapter proposes several novel topologies of pseudo synchronised sampling techniques for phase comparison, which subsequently lead to increased accuracy, real-time efficiency maximisation and simplicity respectively.

Firstly, a novel SCMR based wireless power system, based on the single-phase matrix converter designed in Chapter 4, is developed to implement the methodology introduced in Chapter 5. The

operation of two commonly triggered data converters will be discussed, with several methods proposed for generating the trigger signal and compared. Modifications to the sampling circuit will be presented yielding improvements by using binarised buffering techniques, where the controller complexity can be significantly reduced.

This chapter then presents an evaluation of the performance improvement of the prototype wireless power system, with emphasis on the tolerance to coil alignment and passive components. In summary, based on application-oriented considerations, such as component tolerance and temperature variation, the phase shift control based maximum efficiency point tracking approach significantly enhances the system reliability. It is also shown that the proposed maximum efficiency point tracking approach provides extra stability on components tolerances, leading to increased component options.

6.2. Overview

An important consideration when designing a wireless power system is its efficiency. From the operating principles of a general SCMR based wireless power system (described in Chapter 2), its operation is clearly dominated by the frequency match between transmitting frequency and the resonant frequency of the WPT receiver. Thus, tracking the receiver's resonant frequency is desirable to ensure high efficiency and reliable operation of an SCMR wireless power system. Futhermore, it can enable the WPT system to manage movement in the transceiver and receiver coils and changes in the load conditions at the receiver [6-1]. Based on the series to series topologies shown in Figure 2.8 the efficiency of the SCMR system can be considered as equation (2-2) [6-2]:

The equation 2-2 shows that the efficiency of a wireless power system depends on the coupling coefficient and load condition [6-3], [6-4]. In addition to the varying load conditions, the coupling coefficient is also unpredictable as it relates to the physical positions of transmitting and receiving coils [6-5].

In order to improve the transmitting efficiency or extend the transmitting distance, several techniques have been developed, [6-6] describes an auxiliary DC-DC converter implemented Maximum Efficiency Point Tracking (MEPT) methodology which aims to maintain an optimum resistance. [6-7] describes a dynamic impedance matching approach which employs a semiconductor switch based matching circuit. Furthermore, several types of research also focus on the design of wireless power system, such as the converter topologies or coil structures [6-8], [6-9]. However, these techniques are either bulky or introduce significant losses. Other research has shown that High-quality factor (High Q) coils can be used to further increase the system efficiency [6-10]. However, these high Q coils have been shown to be more sensitive to the environment [6-11], and therefore require advanced tracking and compensation techniques to ensure the output frequency of the transmitter is tuned to the same frequency of the receiving resonant tank [6-11]. Recent research in this field has shown that wireless power systems can

achieve relatively high efficiencies but the proposed designs lack robustness when presented with unstable loads or geometric changes [6-12].

Using the method presented in Chapter 4, which maximises efficiency by minimising the phase angle between the transmitting current and the receiving voltage, this chapter, proposes a novel MEPT methodology that provides a practical means to track the wireless system's optimised operating point on the fly to maintain the wireless power system at a high efficiency independent of the load and operating environment. In the following sections, the relationship between transmitting current and receiving voltage is analysed, from which the theory for MEPT is then developed with a system design for implementation highlighted. Finally, a prototype wireless power system is built in order to evaluate and verify the methodology proposed in this chapter and the results are presented.

6.3. System topology

The detailed control signal topology is shown in Figure 6.1. On the transmitter side, the transmitting current signal will first be measured using a current transducer. The output of the current transducer will be amplified and then level shifted in order to be sampled by the data converter. As shown in Figure 6.2, two signals are required for the data converter, the sample timing signal provides the timing base for the data converter and the latch signal for the First In, First Out (FIFO) memory. The converted digital data is then stored in the Tx FIFO and can be accessed by the microcontroller (MCU).

Meanwhile, the power receiver will process the receiving voltage signal in a similar manner and the resultant data is transferred back to the power transmitter circuit by an ISM RF transceiver. Using the signals from the Tx FIFO and the voltage signal from the RF transceiver, the MCU can then calculate the phase difference.

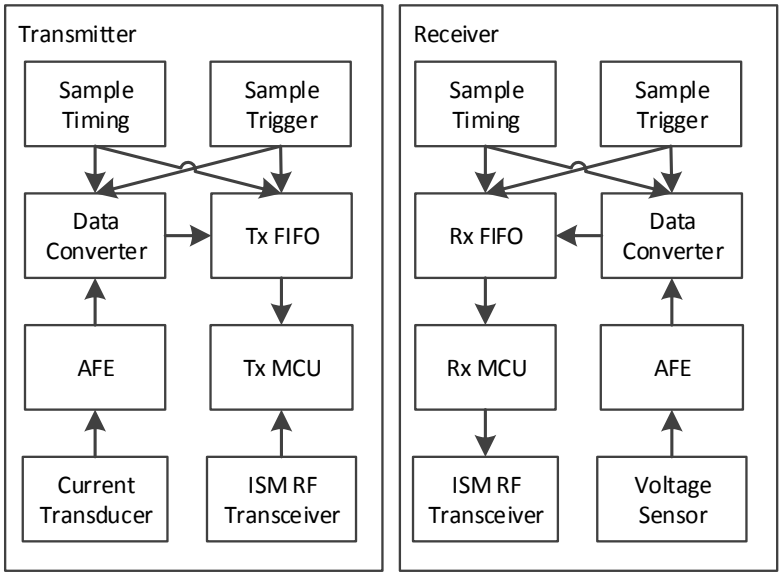

Figure 6.1. The topology of the control signals in a typical phase shift control based MEPT system.

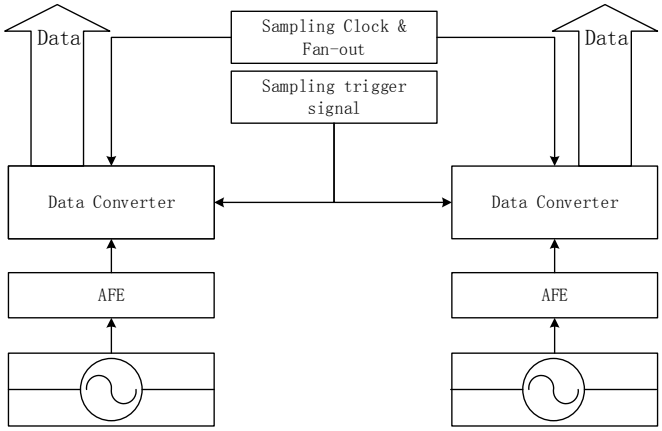

Figure 6.2. Simplified topology for a generic synchronous sampling circuit.

In other devices that require synchronous sampling such as oscilloscopes, its multiple data converters are normally clocked from a fan-outed central clock source. By issuing a “sample start” signal, multiple data converters then start sampling their respected analogue input. Neglecting the mismatched propagation delay caused by PCB traces that vary in length, the data converters will sample their analogue signal at the exact same instance. Hence the phase difference between signals can be easily measured by comparing the digital samples. Compare this approach to the topology shown in Figure 6.1, the challenge in realising the phase shift control based MEPT is being able to sample the transmitting current and receiving voltage simultaneously in two separate circuits that are physically seperated.

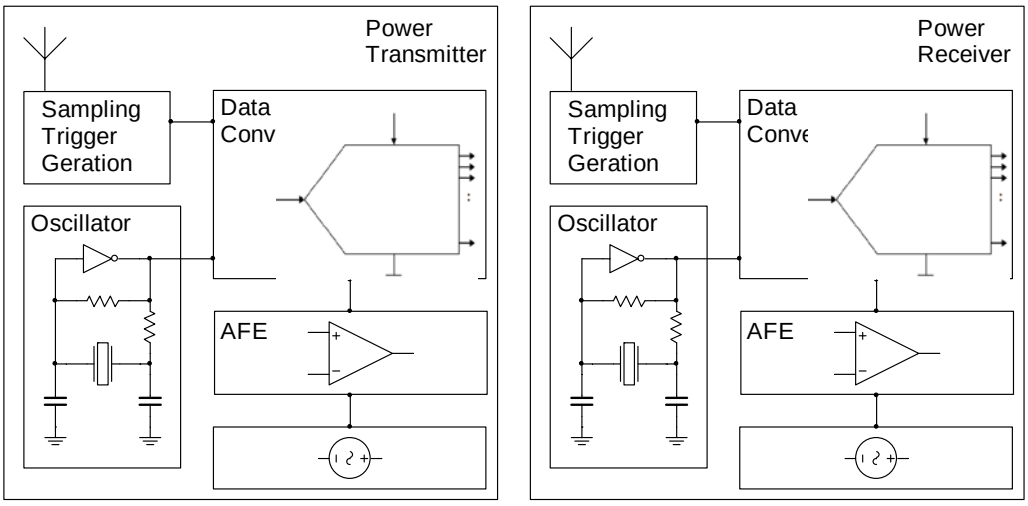

Figure 6.3. Desired pseudo synchronous sampling using separate sampling clock.

The compromise approach to realise a pseudo-synchronous sampling is to externally provide the mandatory sampling trigger signal while keeping the sampling clock locally generated. The approach is described as a pseudo method since the samples are not truly synchronised. For two data converters that require a sample clock at F_{ADC}, the maximum timing difference between two sets of data acquired is $(2 * F_{ADC})^{-1}$, which may be negligible in this specific application. Therefore, the final step is to ensure the two data converters can receive the sample trigger signal simultaneously, even if there is no physical connection between them. Different to a conventional acquisition system where the sampling trigger signal is provided by the system controller, in this design, the sample trigger signal is provided by an auxiliary circuit. Several approaches are described in the next sections.

6.4. Sample trigger signal generation

In this section, two methodologies are proposed that could be used to generate the desired synchronised sample trigger signal. One approach relays an on-board high precision clock source and utilises an on-board PLL to generate the required sampling trigger signal. Once the clock source has been factory-synchronised, the wireless power system only requires periodic calibration to keep the desired signal in-sync. This approach could also utilise radio time signals, such as the UKs MSF, to replace the precision clock source so that no calibration is required. However, the radio signal is restricted by location and environment, and increases the system complexity. The other method is to use diffracted infrared light or a split beam laser, by detecting the light at both ends, two sample trigger signals can then be generated. By sending the light signal from the power receiver, the system complexity and bill of material can be reduced.

6.4.1. Clock-based trigger signal generator

The first method enables the auxiliary circuits to operate independently without any direct communication between the two. The solution is to use an external common clock source or onboard precision clock sources. Figure 6.4 shows the topology of the targeted trigger signal

generator.

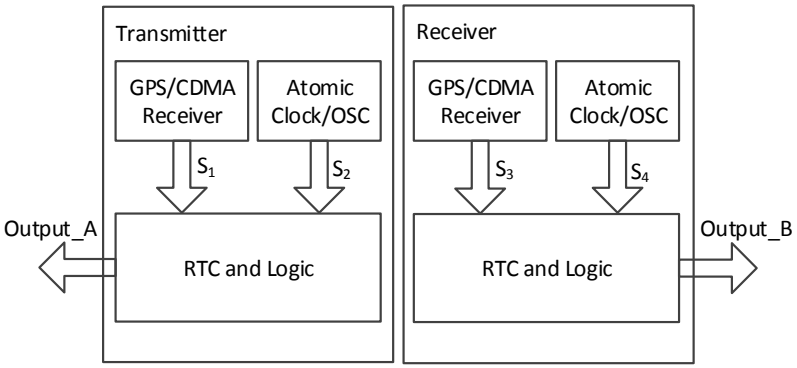

Figure 6.4. Topology of the clock based trigger signal generator

The signal generator shown above can be considered as a precision alarm. The two outputs will be synchronized since the Real-Time Clocks (RTCs), installed both in the transmitter and receiver, are clocked by satellite synchronization signals or onboard precision oscillators.

If a satellite synchronization signal is used, the logic section (can be a controller or programmable logic) acquires the UTC output from the GPS receiver and gives a periodic trigger output based on the timer setting (i.e. every 300mS). Since the difference between the outputs of GPS receivers is negligible, those two trigger outputs can also be considered as synchronized. The advantage of using a satellite synchronization signal is that it is highly robust and requires no calibration. The trigger signals can also be considered as precisely synchronized since the trigger timing is a relay of the clock on the satellite which is generated from a rubidium or a hydrogen atomic clock. In addition to using satellite timing, a ground time signal service can also be used, their millisecond level second ticks can also be used for timing base signal.

For those applications where satellite signals are not available, onboard atomic clocks or precision oscillators can be used. During manufacture, the onboard RTC will be initialised to the UTC (or any given time), after calibration the system will be clocked by its onboard clock source and provide the trigger output periodically. For example, atomic clock sources are accurate at the level of parts in 10^{-12} (i.e. SA.33 atomic clock manufactured by microsemi^{TM}) however, the system may require periodical calibrations within its lifespan. This method is considered

expensive due to the cost of the source components required and is suited to high-end applications where high-speed direct communication between the receiving and transmitter is neither possible or desirable.

6.4.2. Optical-based trigger signal generator

The second method relies on communication between the transmitter and the receiver at a very high rate allowing a single trigger source to be used thus eliminating the high cost of clock sources in the previous method. As can be seen in Figure 6.5, a base trigger signal will be generated by the transmitter to drive several laser diodes. The laser beam generated will travel to the laser detector on the receiver board where the circuit will then produce a trigger signal for sampling. To ensure synchronous sampling, the transmitter also has a laser detector to pick up the laser beam after passing through an attenuated waveguide., which ensures delays seen by the receiving sampling circuit are the same as the transmitter sampling circuit.

$$T_2 + T_3 \approx T_4 + T_5 \qquad (2)$$

This laser-based approach has two issues restricting its implementation in real-world applications. Firstly, the position of the transmitter's laser diodes must be directed at the receivers' laser detector, the practicalities of this will depend on the application. Secondly, the laser signal may be interfered by external light sources which may limit the environmental conditions that the WPT system can operate in.

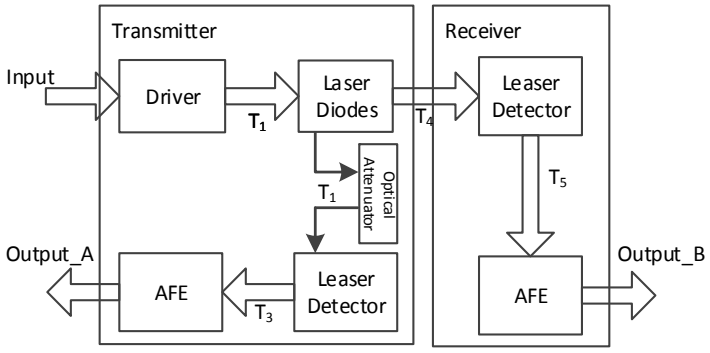

Figure 6.5. Topology of the laser-based trigger signal generator

6.5. Prototype design

A prototype WPT system has been designed based on the approach illustrated in section 5.2 using the topology shown in Figure 6.6. The prototype can deliver 300W to the receiver wirelessly.

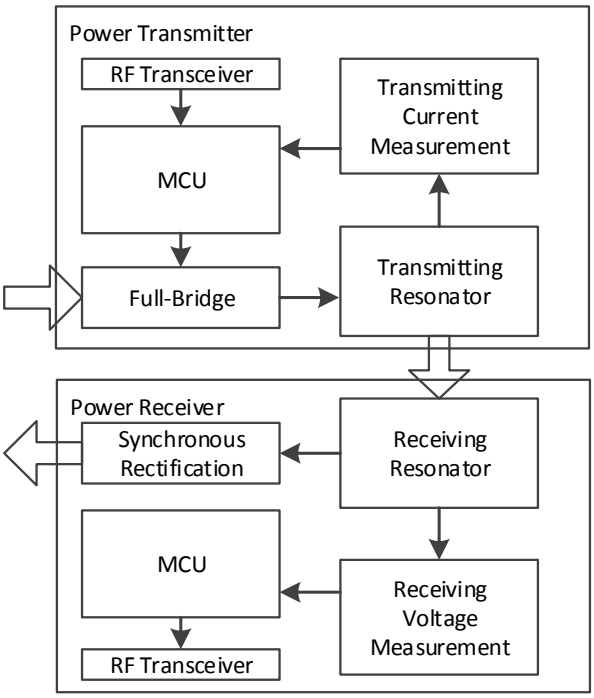

Figure 6.6: Topology of the prototype WPT system employing phase shift based MEPT.

The prototype is shown to be connected to the driving converter of the power transmitter shown in Figure 6.7, which described in Chapter 3.

Figure 6.7: Prototype WPT transmitter employing phase shift based MEPT.

6.6. Hardware design

By solving the triggering issues, a phase detector methodology now needs to be designed. As illustrated in the previous sections, to compare the phase difference of two waveforms, an analogue phase detector has the advantage of simplicity but requires precise tuning and balancing. A digital phase detector may accurately detect the phase angle, but requires an advanced programmable silicon device incorporating high-speed low propagation delay inputs. Furthermore, the frequency of the signal carrying the detected phase angle will have the same frequency of power converter's switching frequency. Directly transmitting a signal in such a frequency requires high bandwidth transceiver which will significantly increase the system complexity.

In order to realise the proposed control algorithm on a simple microcontroller, a mixed signal front-end is designed so that the system only requires limited digital processing ability and exploits the advantages of analogue based phase detector design. A detailed topology of the receiving side design can be found in the following Figure. In the following of this chapter, a brief overview of the hardware design represents the topology showing in Figure 6.8 will be provided.

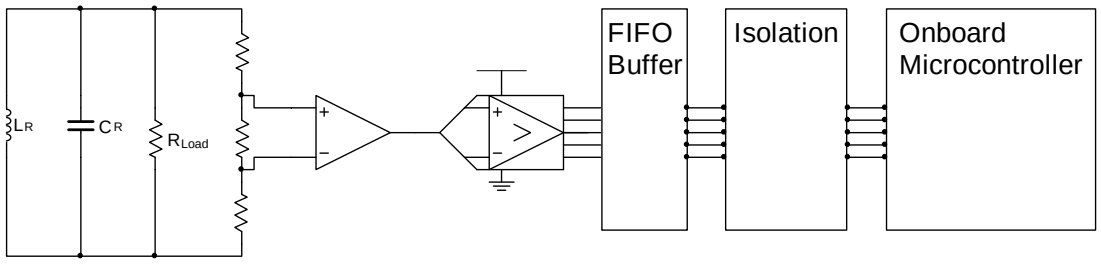

Figure 6.8. The topology of the proposed receiving side hardware design.

6.6.1. Analogue front-end for the receiving voltage signal sampling

The receiving coil will have a high voltage across it and there will be considerable noise pick up, therefore, the entire analogue section and the corresponding sampling circuit is locally referenced to the negative side of the receiving coil. Hence, to drive the differential amplifier

used to sample the receiving voltage signal and provide sufficient voltage swing, a single-ended to differential amplifier should be implemented to convert the single-ended signal, measured from the other side of the coil, to a differential out that drives the high-speed data converter. Conventionally, an integrated single ended to differential amplifier would be used but these do not meet the bandwidth requirement. To avoid using a current feedback amplifier, two separate high-speed voltage fed amplifiers are used that form an op-amp buffer. Figure 6.9 shows the analogue front-end design, the two 40Ω and 1.6kΩ resisters determine the input stage gain on the differential input, the value of the resistors are relatively small as required by the high slew rate feedback while the 2 pF ceramic capacitors compensate for the phase response. The gain of those amplifiers is set to 40 to meet the ADA4895's minimum stable gain requirement. By driving the op-amps with a bipolar signal and power supply, this data converter driver provides 6V voltage swing with 0V common mode offset. The diodes connected to the output of the amplifier were designed to clamp the signal to protect the data converter, however, they are not used in the prototype hardware due to the junction capacitance causing a undesired delay.

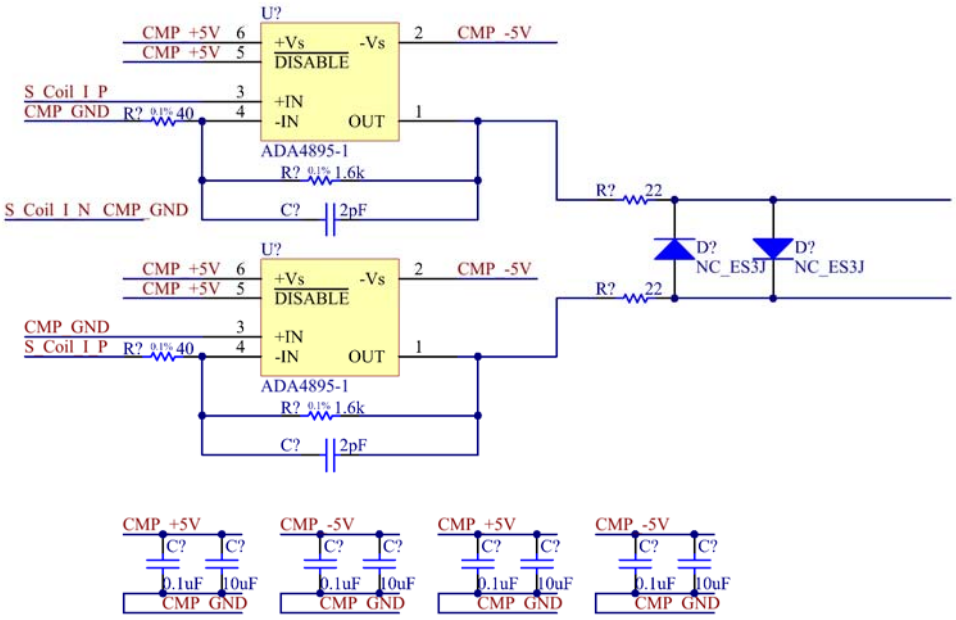

Figure 6.9. Analogue front-end design for the receiving voltage signal.

6.6.2. The data converter

Commonly used high-speed data converters are either multi-bit pipelined ADCs or sigma-delta ADCs. In this application, the amplitude of the input signal has a negligible effect on the required phase difference since the target signal is known as a sinusoidal or sinusoidal-like signal. Hence, the data converter implemented in this design is a simple comparator as shown in Figure 6.10. Ferrite beads and ceramic capacitors are used to filtering the power supplies so that reduce the noise coupled from the power supplier. The noise on the input signal is inevitable and results as a bounced digital output, which will be debounced in the microcontroller by a simple averaging algorithm.

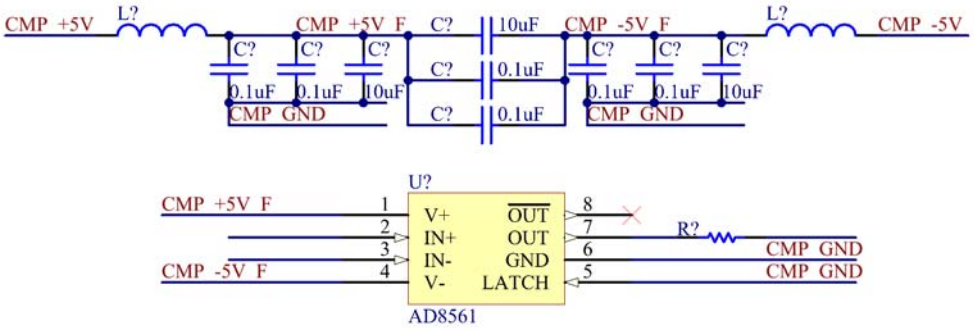

Figure 6.10. Simple comparator used as the data converter.

6.6.3. Data buffer

For a WPT system operating at 1MHz, the base frequency of the digital output from the comparator will also be at 1MHz, which is the minimum I/O frequency if this signal will be processed by a logical device. To observe the noise on the corresponded analogue signal and debounce the digital output, higher I/O throughput will be required. Furthermore, in order to measure the phase angle, a timer will be required that is triggered at the falling and rising edge. For a reasonable resolution, the time base of this timer will be 100 times higher than the frequency of the signal to be processed. To avoid using a gigahertz level FPGA, as shown in Figure 6.11, a First-In-First-Out (FIFO) buffer was implemented.

As can be seen from Figure 6.11, the comparator continuously provides a binary converted signal representing the status of the receiving coil voltage. When the synchronous trigger signal, Sync_Start is applied to the FIFO, data recording will begin until the FIFO is full. The data will be recorded at the clock frequency applied to 1WRTCLK and 2WRTCLK, which is generated from a 60MHz oscillator. For a 1MHz WPT system, the FIFO chip can store 512 samples at 60MHz which gives a record length of 8.5uS or 8.5 cycles of the receiving coil voltage waveform.

Based on the shared trigger source methodology described earlier, at the instance when the FIFO on the receiving side starts to record data, the same FIFO in the power transmitter will also start to record data. This mechanism provides a simple approach to implement wireless pseudo synchronous sampling, with the data converters using two asynchronous sampling clocks. For this specific application, the maximum sampling clock difference will be 8.333 nS, which happened when one clock signal in advance of another by half of it period, and introduces 0.83% of the phase error.

On the other side of the FIFO buffer, the Sync_IR signal will inform the microcontroller of the end of sampling. Then the microcontroller initialises the read of the FIFO by issuing the Sync_Read signal, and then by providing the clock signal externally, using the 768kHz oscillator shown, the microcontroller can read the data similar to a Serial Peripheral Interface (SPI) exchange of data. The external clock meets the requirements for isolation but also solves potential synchronisation issues using an internal clock. Using an internal clock would require isolation, the propagation delay introduced by a required optocoupler or digital isolator would mean that the signal will be ahead of the data signal by twice the propagation delay, which may cause the clock and data to be out of sync.

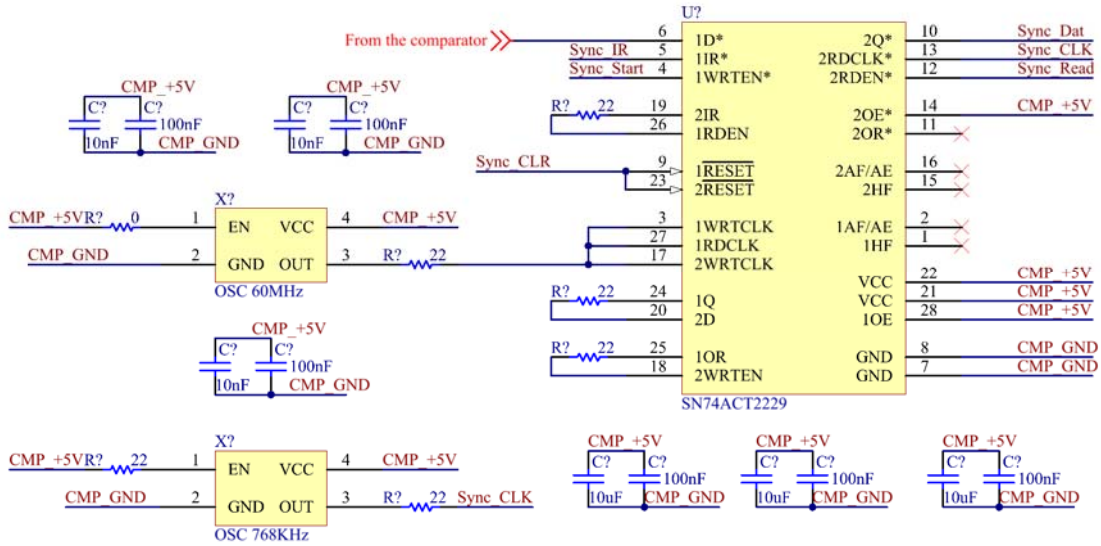

Figure 6.11. 1-bit width 512bits synchronous FIFO buffer.

6.6.4. Isolation the microcontroller from the high voltage coil

As described above, the analogue front-end, data converter and FIFO buffer are both referenced to the negative side of the receiving coil, which raises the risk of exposure to the high voltage across the receiving coil. In this design, optocouplers are implemented to isolate the high voltage side from the MCU as shown in Figure 6.12. As can be seen from the schematic, all signals are inverted, this is due to the optocouplers using the ground of the photodetector as the ground of one infrared light-emitting diode. Those optocouplers provide 15Mbit data throughput between the isolated area and the controller.

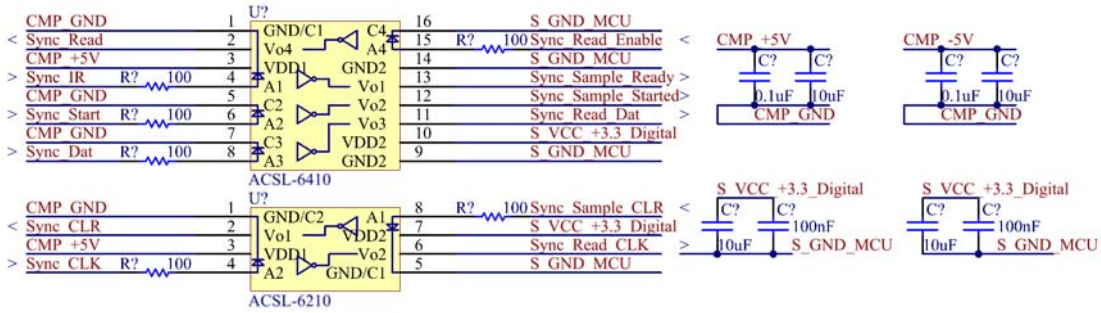

Figure 6.12. Optical isolation between the high voltage side and the microcontroller.

6.6.5. The receiving side microcontroller

Based on the design decisions introduced above, the receiving side only requires a simple low-speed microcontroller for data transfer. In this design, an STM32F334K8T6 was implemented, which was primarily used to read the FIFO buffer, reconstruct the data and then send the data to the power transmitter using an ISM transceiver or ultrasound modulation.

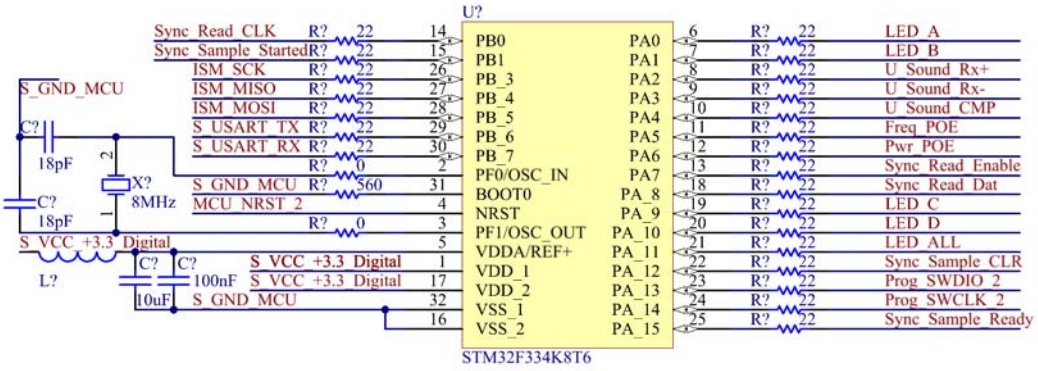

Figure 6.13. Simplified schematic showing the microcontroller used on the power receiver.

6.6.6. Isolated power supply

The power supply for the power receiver circuit is an off-the-shelf isolated DC-to-DC power supply that converts the received voltage to 3.3V DC to power the microcontroller, and a 12V DC voltage source powering an OLED display for the user interface. To power the isolated circuits, another isolated DC to DC power supply is required. Based on the size and volume consideration, the power supply shown in Figure 6.14 is implemented. At the core of this desired power supply is an unregulated DC to DC power supply working at 800 KHz, by using its on-chip transformer, the whole isolated power source can provide the required 2W of power while only occupying approximately 0.5mm^3 of space.

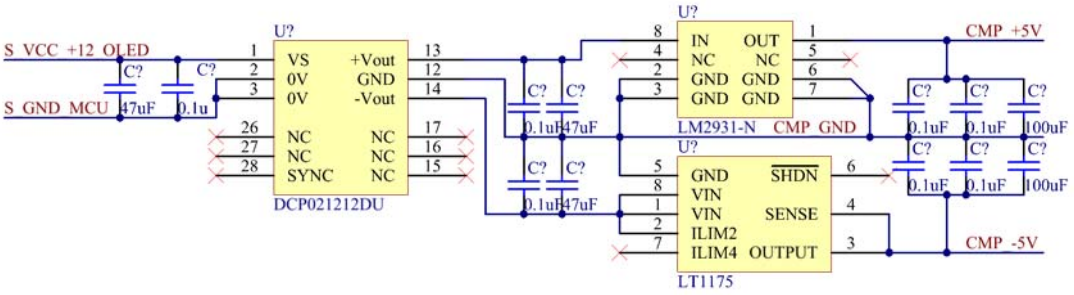

Figure 6.14. Lightweight isolated power supplier desired in this design.

6.7. Test and evaluation

The matrix converter for the prototype was designed to provide a switched voltage output with frequencies ranging from 500 kHz to 1MHz. Figure 6.15 shows the output voltage and current waveform of the drive converter. As can be seen from Figure 6.15, the converter can provide the required high-frequency voltage output which is connected to the transmitting resonator and generates the required sinusoidal current within the desired frequency region.

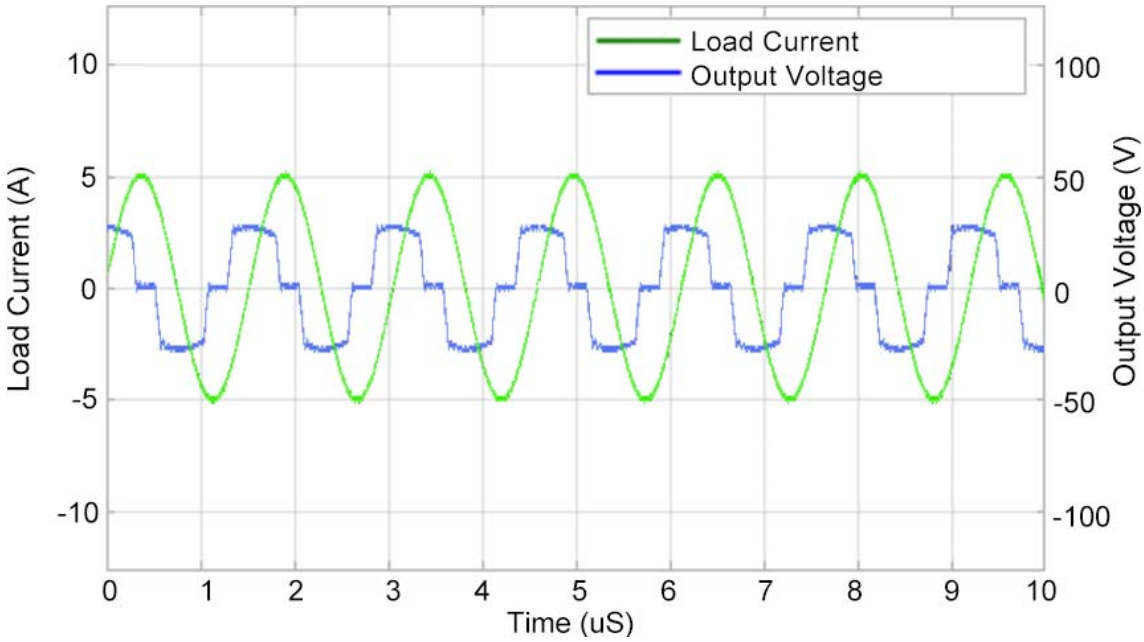

Figure 6.15: Output voltage and current waveform from the converter with proposed attachment enabled.

In order to evaluate the MEPT approach introduced in this chapter, the transmitting current is externally measured by a current probe and the receiving voltage is measured by a differential probe. Those measurements are fed into an oscilloscope where the phase difference can be visualized. The following Figures show the waveform from the oscilloscope at the maximum efficiency point.

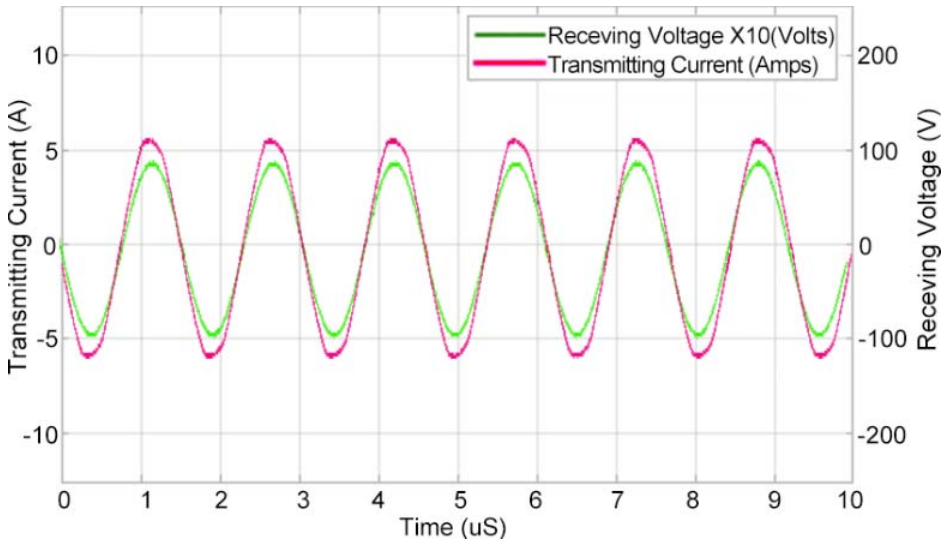

Figure 6.16: Oscilloscope capture shows the transmitting current and receiving voltage at maximum efficiency point.

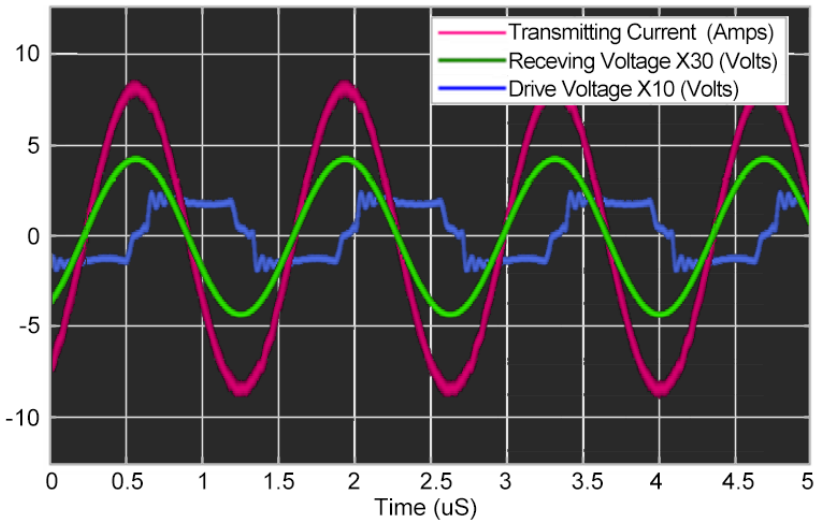

Figure 6.17. Oscilloscope capture shows the operating waveform at the optimal point.

In order to simulate the changes in the self-resonant frequency of the receiver, additional capacitances are applied to the load. The additional capacitance forces the self-resonant frequency lower than the original self-resonant frequency, which will affect the efficiency of the WPT system. The results presented in Figure 6.18 show the comparison of the efficiencies of the WPT with (Blue), and without (orange) MEPT control. As may be seen from Figure 6.18, without MEPT control, the system efficiency diverges from the optimised efficiency level. With MEPT system control the output frequency is varied and the WPT system maintains its efficiency level.

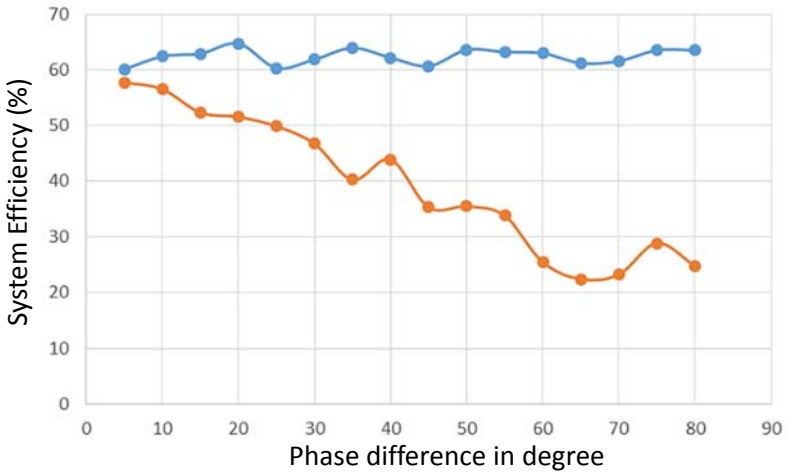

Figure 6.18. Comparison between the power system with (Green) and without (Orange) MEPT.

6.8. Summary

This chapter introduced a novel maximum efficiency point tracking methodology and presented its implementation. The novel approach to maximise the efficiency by dynamically matching the converter's output frequency with the receiver's resonant frequency is demonstrated to be effective. However, to provide the synchronous sampling, a wireless synchronous triggering mechanism to trigger two physically separated data converters are required. Two methods are then proposed in the chapter to realise wireless pseudo synchronous triggering mechanisms, the first assumes no direct communication between the data converters and instead relies on a synchronised time source. The second method uses a laser to establish a high-speed communication link so that a common trigger source can be used. The first method is appropriate where no direct communication is possible but utilises expensive components therefore limited to high-end applications. The second method relies on having a line of sight between the receiver and transmitter but is much lower in cost.

Using those synchronised trigger signals, a novel wireless digital storage synchronous sampling is proposed. The proposed approach could synchronously sample two or more signals, where those signals are separated in different sub-systems with no physical connections in between.

A prototype wireless power system has been built for evaluation of the MEPT methodology and results presented showing that the efficiency of the WPT system can be maintained under varying load conditions. By implementing the MEPT methodology presented in this chapter the wireless power system can be used to achieve WPT in systems where the load may vary, the relative coil positions may alter, and environmental conditions may fluctuate.

6.9. References

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7. A Hybrid Wireless PLL for WPT system

7.1. Introduction

In the previous chapter a wireless power system with a phase shift control based maximum efficiency point tracking controller is evaluated showing improved efficiency and reliability. However, the proposed approach still requires communication bandwidth at the megahertz level, where the cost and complexity of the RF transceiver will be high. In this chapter, a PLL-like control is developed, featuring very limited communication bandwidth requirements, to allow the transmitting frequency of a given wireless power system to be locked into its corresponding power receiver.

After briefly reviewing a conventional PLL, this chapter begins with the introduction of a two-stage phase detector. By calculating the phase difference between a given reference common signal, the transmitting current, and receiving voltage, the phase difference between transmitting current and receiving voltage can be obtained by performing a reverse operation. Furthermore, by analysing the data in its frequency domain, the effective data can be compressed by rejecting its higher order harmonics. Thus a wireless PLL utilising very limited communication bandwidth can be established. The resulting wireless power system with wireless PLL implemented is verified by measurement on a prototype, with analysis into the accuracy of control. The wireless PLL is demonstrated to provide the same performance improvement, compared to the maximum efficiency point tracking approach illustrated in Chapter 6, but consumes less than ten percent of the communication bandwidth resources. It is also shown that describing the phase difference in its frequency domain, and removing the higher order harmonics, will not significantly degrade the wireless PLL's performance.

7.2. A brief overview about the conventional PLL

The typical structure of a basic PLL includes a phase detector, loop filter and Voltage Controlled Oscillator (VCO). The phase detector provides a signal which describes the phase difference between its two inputs. The output of the phase detector is then fed into a loop filter to provide DC levels indicating the phase difference, where the DC level will be used to control a VCO to provide the output [7-1, 7-2]. For most widely used PLL, the performance can be characterised by the loop filter [7-3]. Figure 7.1 shows a typical PLL driven induction heating system. As can be seen from the Figure, the phase difference between the output voltage of the half bridge and the resonant current is calculated. The phase difference is then used to control the VOC so that when the load condition is changed (i.e. the distances between the work head and the heating target is changed) the PLL will lock the phase difference between those two signals and keep the system resonant.

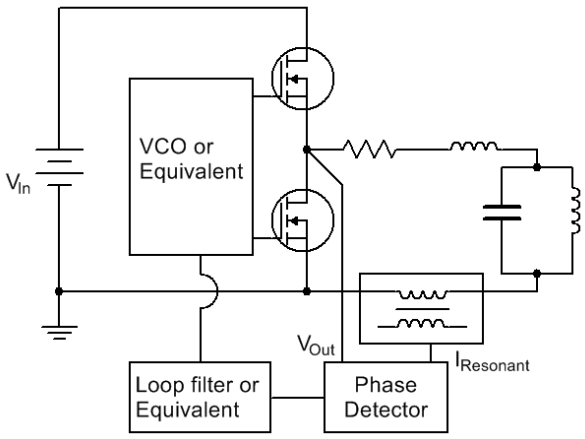

Figure 7.1. PLL dominated induction heating system.

Significant research over the years has been carried out on variations of the parameters of PLL systems such as its output frequency, loop bandwidth and lock time [7-4]. Based on the components used, PLLs can be categorised into three groups. Conventional analogue PLL is the first generation and mainly used in communication systems, where the entire PLL is formed by analogue components [7-4]. In order to reduce the external components and improve a PLL's

tolerance and stability, an all-digital PLL that substitutes function blocks by digital components has been introduced [7-5]. The final group is hybrid PLLs, these consist of both analogue and digital function blocks, thus providing extra flexibility with optimised hardware cost. A simplified block diagram of a hybrid PLL for induction heating is shown in Figure 7.2. In this hybrid system, the traditional VOC has been replaced by an MCU so that a more complex control such as full bridge PWM/PDM with dead time control can be realised.

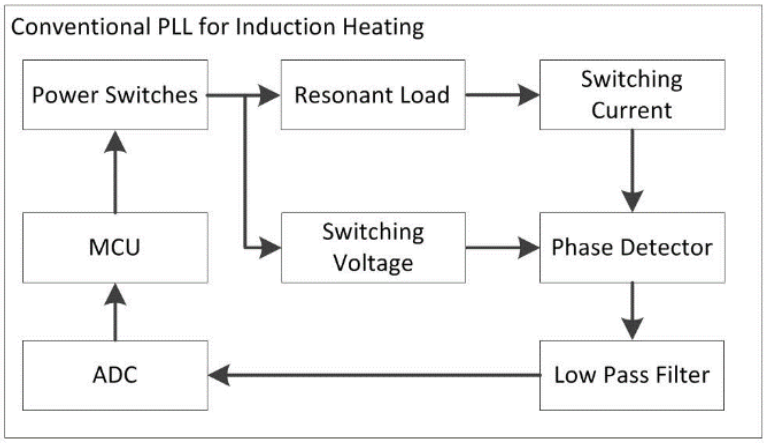

Figure 7.2. Simplified Block diagram of an induction heating system with hybrid PLL applied.

7.3. Theory and topology of wireless PLL

As illustrated in Figure 7.2, the PLL compensates for the load condition and maintains the converter at its resonant frequency. However, in a WPT system, the switching frequency of the drive converter should be close to the resonant frequency of the power transmitter, and also equal to the resonant frequency of the power receiver. For the simplified schematic shown in Figure 7.3, $F_{SW} = \frac{1}{2\pi\sqrt{L_R * C_R}}$ should be fulfilled in order to achieve maximum transfer efficiency.

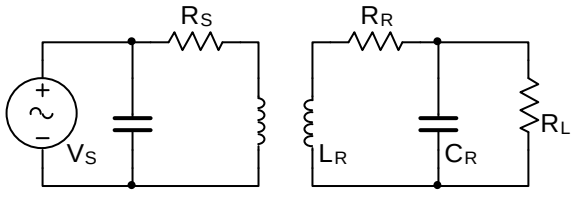

Figure 7.3. Simplified schematic of an SCMR based wireless power system.

When implementing a PLL into a WPT system, the challenge is how to calculate the phase difference between the current in the transmitting coil and voltage at the receiver coil. The difficulty is to wirelessly transfer one signal in real time so that those two signals can be analogously or digitally compared, without requiring a very high bandwidth communication link. One solution is to use data converters, where the transmitting current and receiving voltage are sampled using two commonly clocked data converters. This simplified approach yields the phase difference by comparing the zero-crossing points of those two sampled data arrays resulting in a lower bandwidth requirement. However, for those two data converters that are located independently in the transmitter and receiver, a wireless common trigger has to be provided as discussed in chapter 6, which requires complicated timing control and measurement.

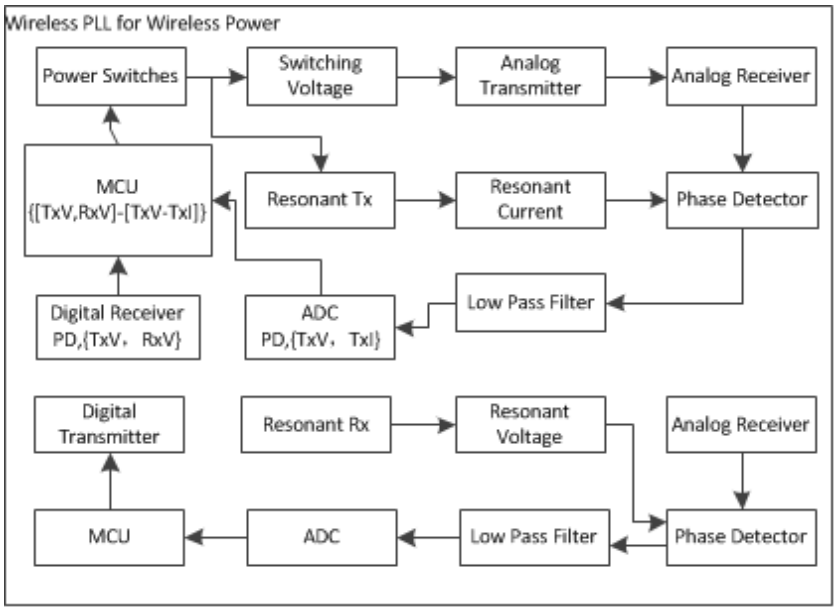

Figure 7.4. Simplified block diagram of a wireless PLL.

To negate the need for a common timing source, this chapter proposes a novel wireless two-stage phase detector named HyWi-FFTPLL as shown in Figure 7.4. In contrast to a wired phase detector where the phase difference of two signals are compared or triggered directly, this wireless PLL uses a third signal for common reference and calculates the desired phase difference as a two-stage process. The transmission of the common reference does require a minimum

bandwidth but this can be reduced by using a signal frequency equal to $F_O/2$ where F_O is the switching frequency of the power converter. The proposed example in this chapter utilises the local output voltage signal of the transmitter as this third reference signal to simplify the evaluation progress. The detailed topology for the transmitter circuit is shown in Figure 7.5.

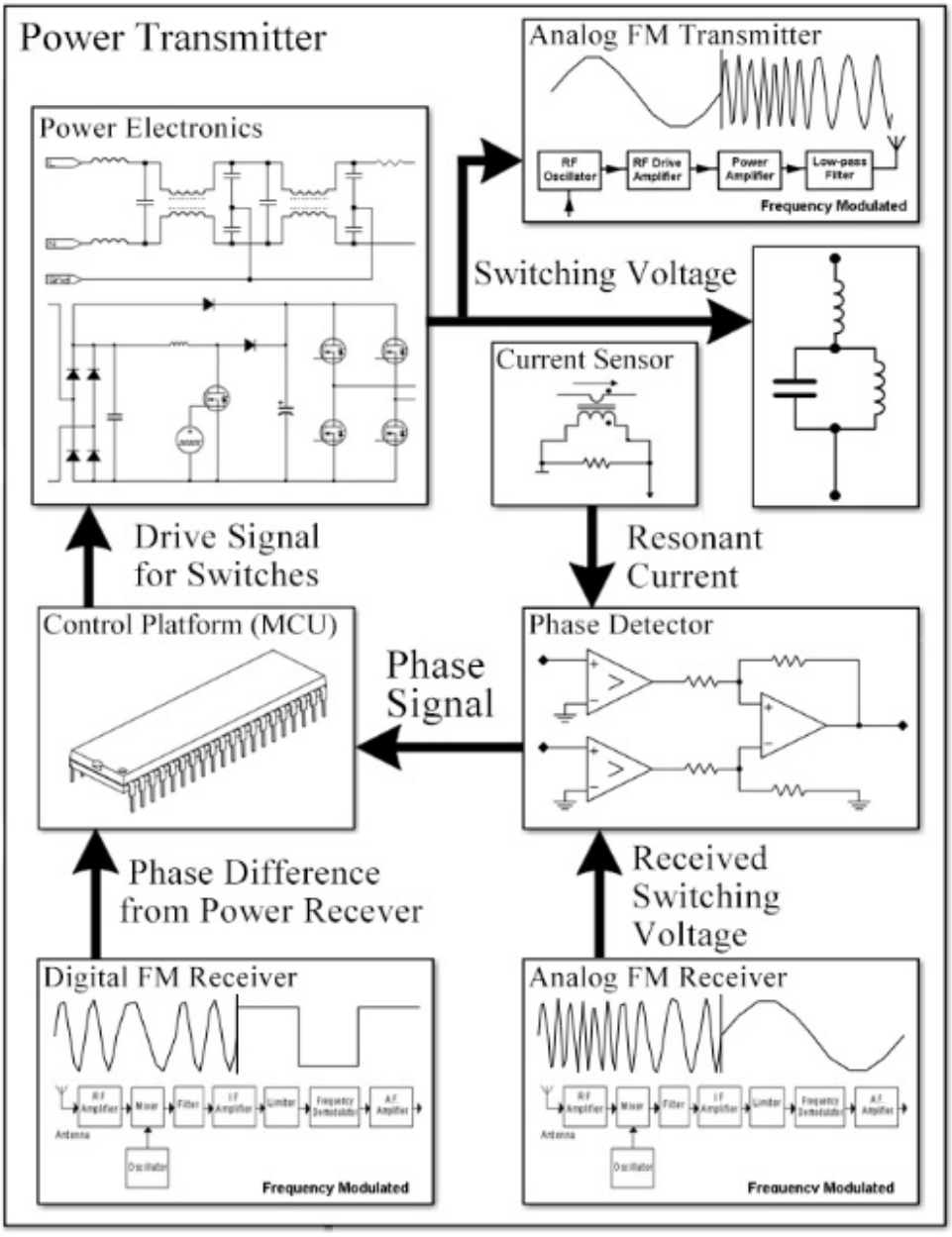

Figure 7.5. HyWi-FFTPLL on its Transmitter Side.

As shown in Figure 7.5, the basic function on the transmitter side is to compare the phase

difference between the local switching voltage and resonant current, which is similar to the operation of a conventional PLL. The local switching voltage is sent via an analogue transmitter to the receiver as it is required as the third reference on the receiver side. The receiver will receive this signal with a propagation delay. It is therefore important to measure the phase difference at the transmitter between the local switching voltage and resonant current with this propagation delay added, this is achieved by passing the switching voltage signal through an analogue transmitter-receiver bridge. Furthermore, a quantization- subtraction phase detector is used since the proposed HyWi-FFTPLL represents the phase difference on its frequency domain to reduce the communication bandwidth so that the amplitude information has less contribution to the phase detected.

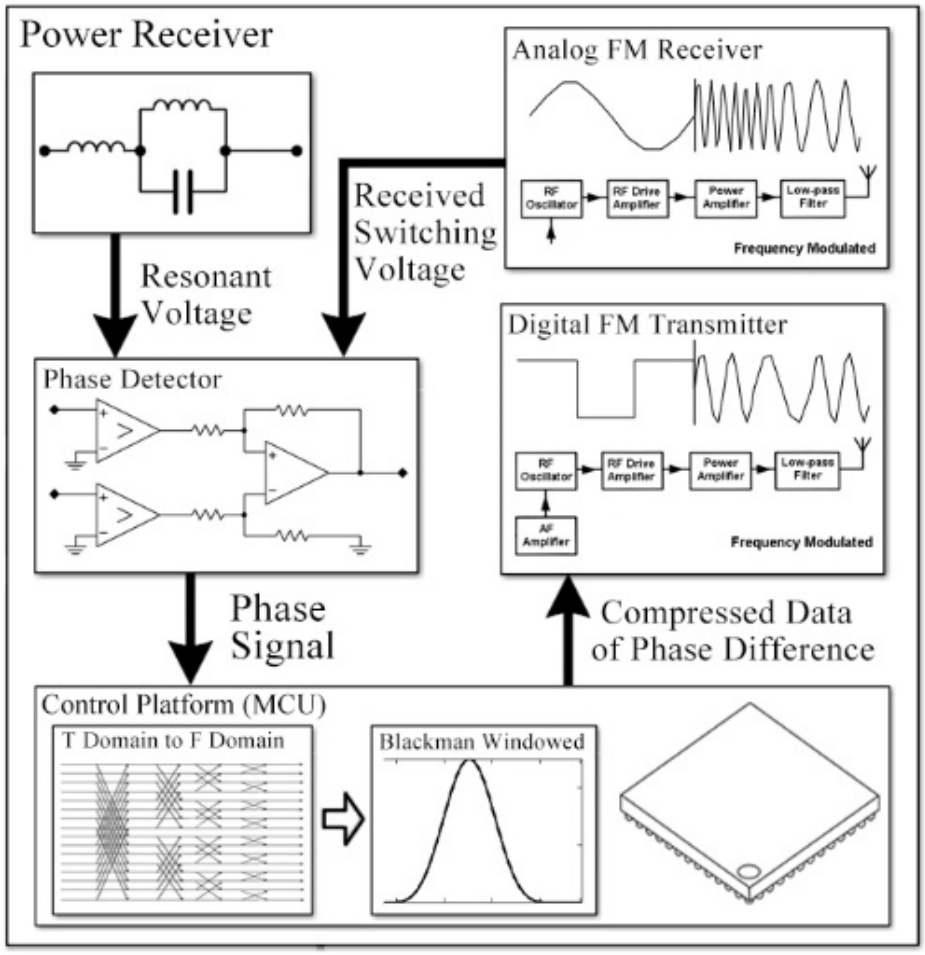

Figure 7.6. HyWi-FFTPLL on its Receiver Side.

The receiver side of the HyWi-FFTPLL is relatively simple and therefore potentially low cost. As shown in Figure 7.6, the receiver side requires an analogue receiver where the switching voltage of the transmitter side can be acquired. Meanwhile, the resonant voltage waveform can be measured locally from the receiving coil. The phase difference between the switching voltage and resonant voltage can then be calculated. This result then needs to be relayed back to the power transmitter but requires a high bandwidth. The proposed method in this chapter is to translate the phase signal from the time domain to the frequency domain. The data quantity is then reduced by removing its higher order harmonic components by using a Blackman window that reduces leakage. Finally, the desired frequency data can be sent back to the power transmitting side by using a digital ISM transmitter that uses a communication link at least 10 times lower in bandwidth than for a time-based signal transmission.

7.4. Simulation

Based on the system topology introduced in the previous section, a Simulink model has been built to verify the design. The simulation diagram is shown in Figure 7.7. In the simulation model, waveforms of a simple resonant converter are simulated. The current waveform is generated from a delayed sinewave and the undelayed sinewave is compared with zero so that a corresponding voltage waveform, which leads to the resonant current can be obtained. The detailed waveform is shown in Figure 7.8.

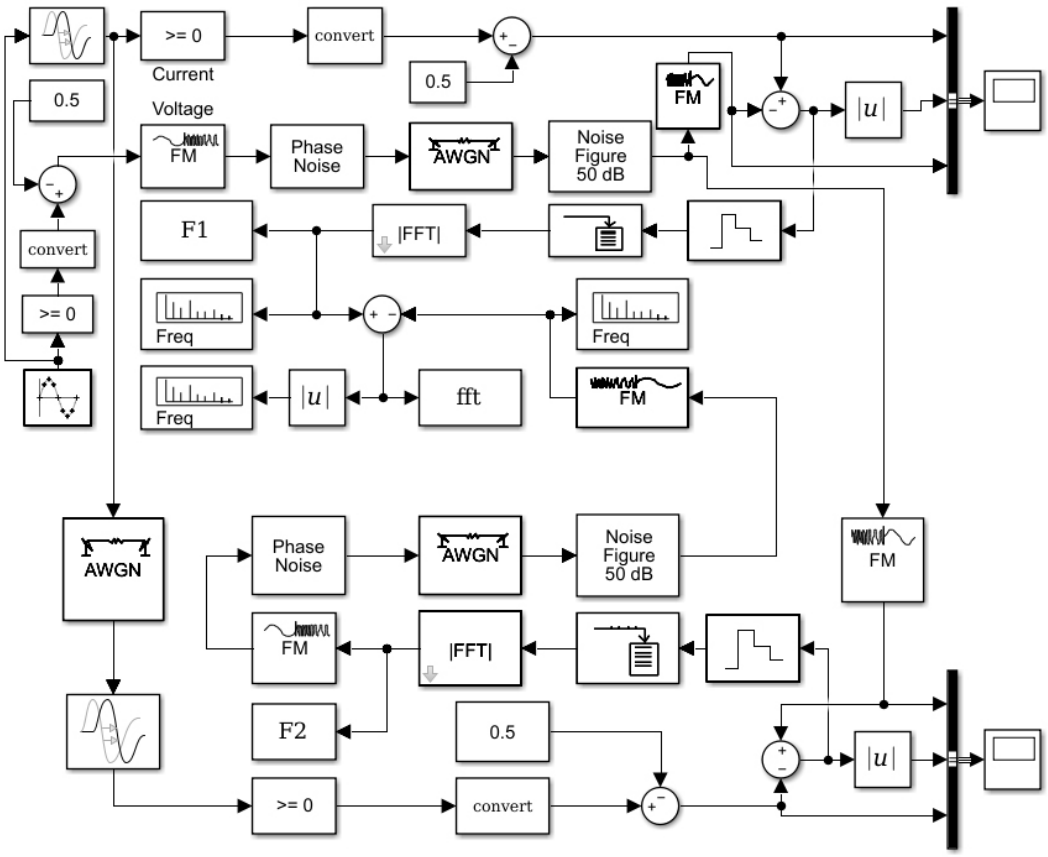

Figure 7.7. Simulink schematic of HyWi-FFTPLL.

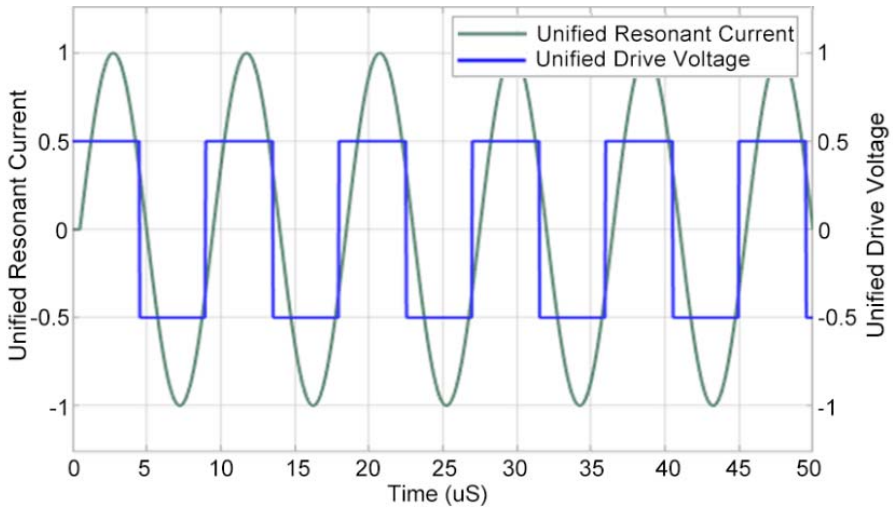

Figure 7.8. Simulated waveforms represents the converter

During simulation, the wireless channel of the drive voltage is simulated using an analogue FM modulator-demodulator pair with the addition of phase noise, white noise, thermal noise and antenna noise. The waveform of the power transmitter side is shown in Figure 7.9. By feeding the phase difference signal into the microcontroller located at the power transmitter, the phase data can be converted into its frequency domain by performing a Fast Fourier Transform (FFT).

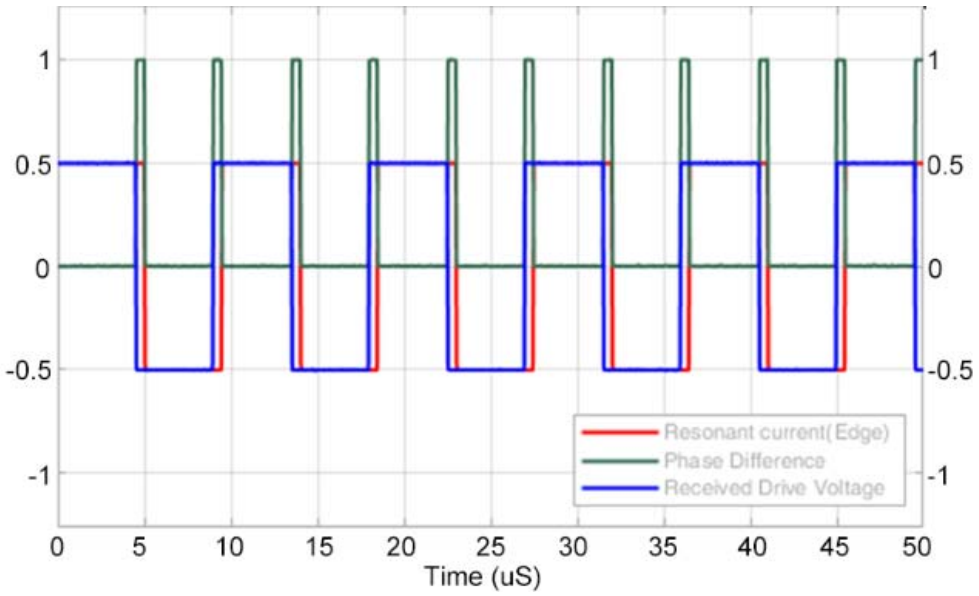

Figure 7.9. Simulated transmitting side waveforms.

On the power receiver side, the transmitted voltage signal is simulated by an FM modulator-demodulator pair with the addition of noise as was added to the transmitter. Meanwhile, the phase difference between the transmitting current and receiving voltage is simulated by adding a transport delay to the transmitting current, as the receiving resonator is excited by the transmitting magnetic field, which is in turn excited by the transmitting current. Consequently, the phase difference can be obtained by comparing the received drive voltage and the receiving resonant voltage.

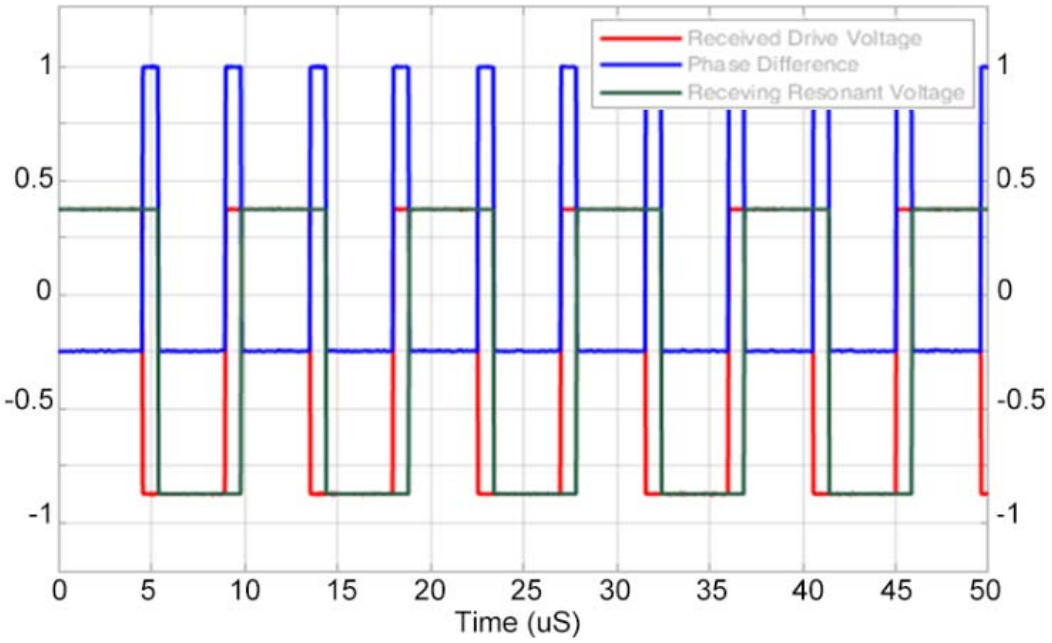

Figure 7.10. Simulated receiving side waveforms.

The phase difference obtained on the power receiver side will be sampled by the power receiver's onboard microcontroller. By performing an FFT, the phase difference in the frequency domain can be obtained. Since the higher order harmonics are not necessary to obtain the amplitude of the phase difference, the amount of data being sent back to the transmitter can be significantly reduced. Finally, the data obtained from the power receiver is transferred back to the power transmitter by using a digital Phase-Shift Keying (PSK) modulator-demodulator pair. On the power transmitter side, the two-phase differences in the frequency domain, transmitting current to drive voltage, and receiving voltage to drive voltage, are compared. Hence, a spectrum matrix representing the amplitude of the phase difference between transmitting current and receiving voltage can be obtained. Figure 7.11 shows the resulting spectrum for different phase shifts between transmitting current and receiving voltage.

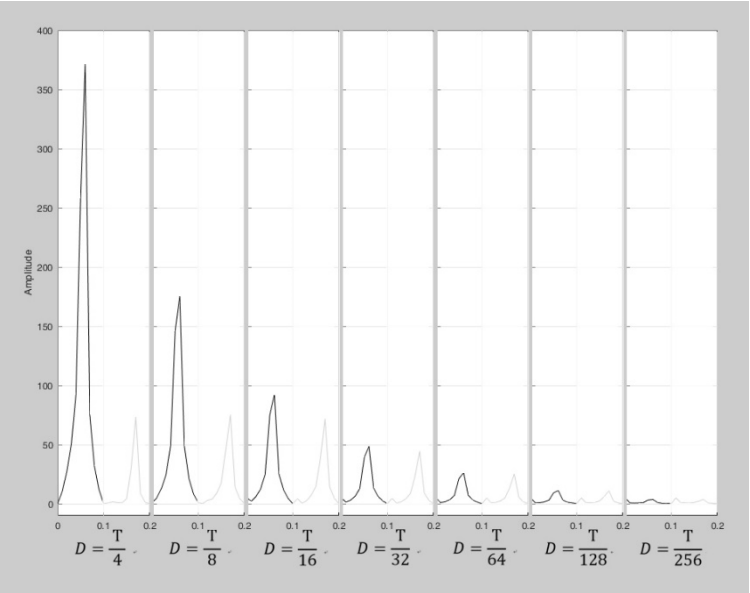

Figure 7.11. Spectrum showing amplitudes when phase difference applied.

As illustrated in Figure 7.11, the spectrum amplitude follows a downward trend when decreasing the phase shift between transmitting current and receiving voltage. Meanwhile, only a 100 element array of type float is transferred between the power transmitter and power receiver. This model successfully simulates the proposed HyWi-FFTPLL methodology, demonstrating the relatively low bandwidth requirements compared to that of sending sampled waveforms in the time domain.

7.5. Hardware design

A prototype PLL has been built as shown in Figure 7.12, the circuitry is designed to functionality for the analogue signal processing and wireless commutation. The left section of the breadboard contains the desired oscillator that generates the phase reference signal. The slew rate of this digital signal can be adjusted and transmitted by using the ISM transmitter shown with the green antenna.

The right side of the circuit belongs to the power receiver. The RF receiver module with the blue antenna receives the phase reference signal (transmitter voltage) and calculates the local phase

difference between the reference signal and the receiver voltage. Meanwhile, the transmitter current is fed into the middle section of the breadboard, where the phase reference signal, that is received using the brown antenna, is compared to the transmitting current to calculate the phase difference. Finally, the two calculated phase differences are sampled by the microcontroller installed in the power transmitter and then used to calculate the phase difference between the transmitting current and receiving voltage.

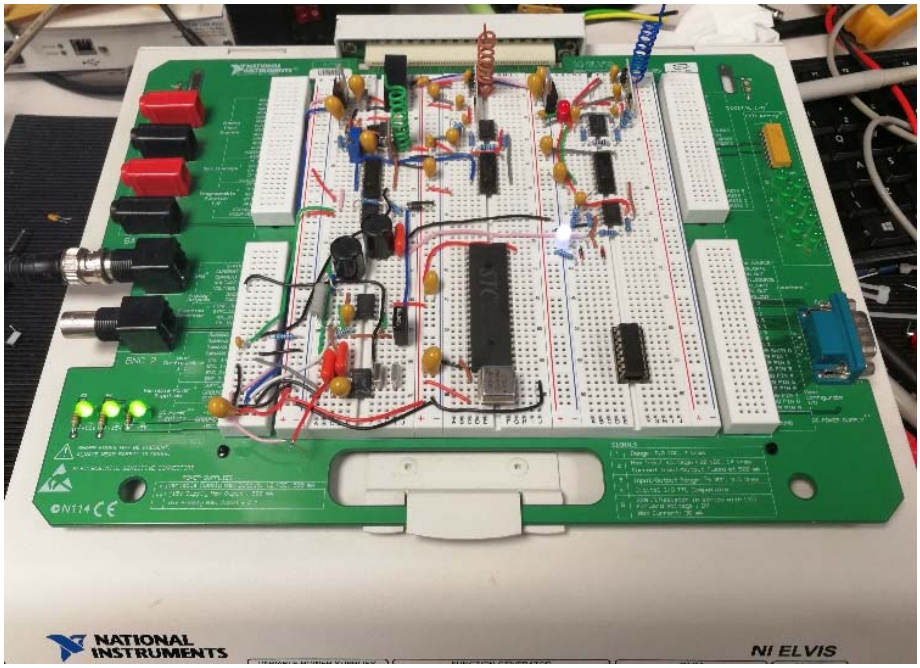

Figure 7.12. An early prototype of test platform for HyWi-FFTPLL.

7.6. Test and evaluation

The transmitter and receiver prototypes are designed to form a WPT system with fast battery charging capability. The power transmitting circuits drive a transmitting coil that is centrally aligned with a corresponded receiving coil. The receiving coil is therefore terminated to the prototype shown in Figure 7.13, at where the power can be utilised.

Figure 7.13. Wireless Power receiver showing connection to the prototype HyWi-FFTPLL shown in Figure 7.12 through the cable on the left.

Figure 7.14 shows the output voltage and current waveform of the drive converter. As can be seen from the plot, the converter can provide the desired high-frequency voltage output (blue), which drives the transmitting LC resonator, generating a sinusoidal current (purple) that can be quantised to 1-bit data (green).

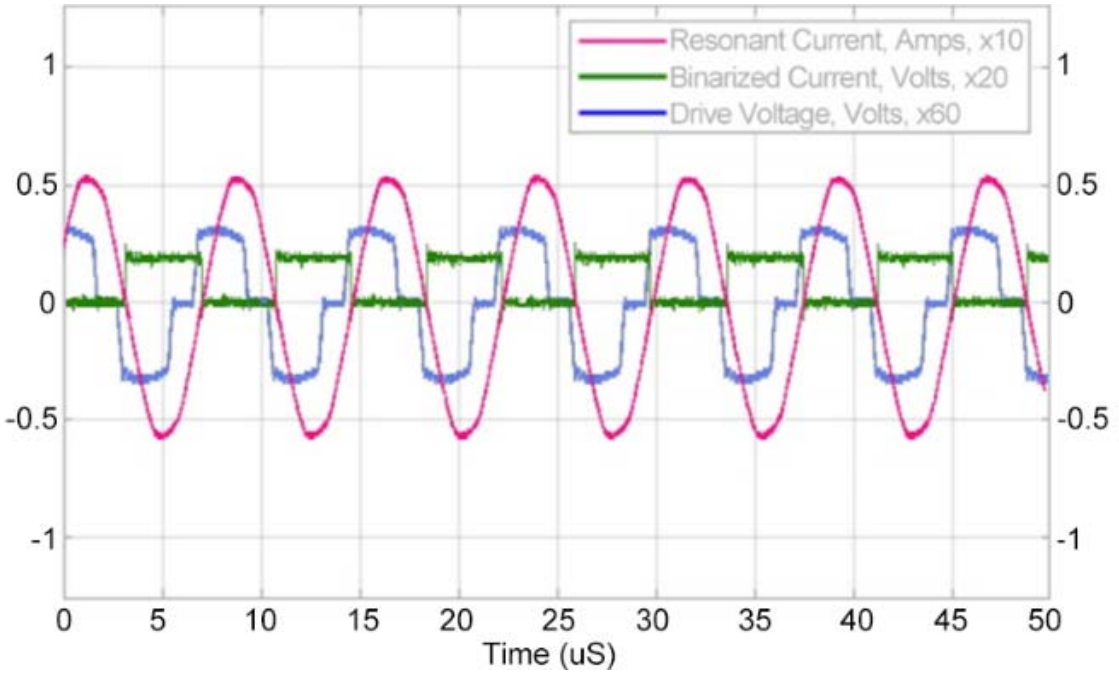

Figure 7.14. Output voltage and current waveforms from the power transmitter.

In order to evaluate the wireless PLL methodology introduced in this chapter, the transmitting current and receiving voltage are externally measured by an oscilloscope using a current probe and differential probe. By visualising the phase difference between the transmitting current and receiving voltage, the correct functionality of the wireless PLL can be verified. Since changes in a self-resonant frequency can be difficult to control, changes in self-resonant frequency are performed by connecting several polyester capacitors to the receiving resonator. The additional capacitance pulls the resonant frequency lower than its original value. By comparing the phase difference before and after the additional capacitor is connected, the performance of wireless PLL can be evaluated.

The results are presented in Figure 7.15, the PLL tracks the phase change and controls the output frequency of the transmitting microcontroller. The waveform shows negligible phase difference between transmitting current and receiving voltage. Hence the system efficiency can be maintained.

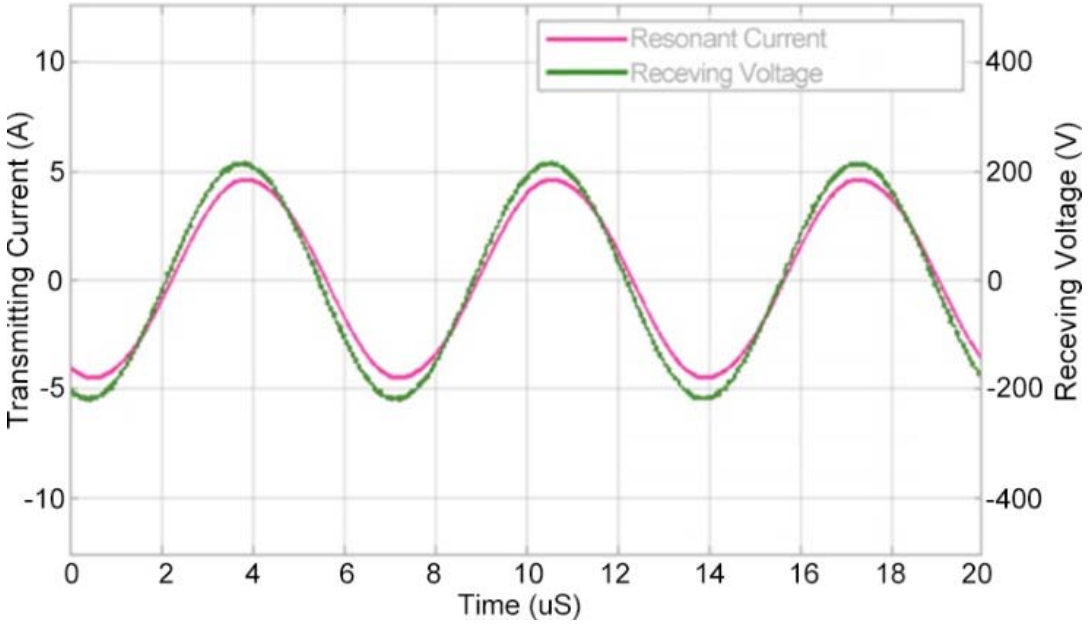

Figure 7.15. Oscilloscope capture shows the transmitting current and receiving voltage.

7.7. Summary

This chapter introduced a novel wireless PLL for a WPT system to track the maximum efficiency point. The approach to performing a PLL wirelessly by a two-stage phase detector is demonstrated to be effective. To transfer the data generated from the conventional edge-triggered phase detector, a high bandwidth transceiver pair is required. In this research, a FFT dominated method is proposed to reduce this requirement. The desired method calculates the phase difference using the frequency domain instead of the time domain, and by ignoring the harmonic components the amount of data to be transmitted can be further minimised. The desired method has been explored using Simulink, and a prototype WPT system has been built for validation. The results presented shown that the phase of transmitter voltage and receiver current can successfully be locked, meaning that the maximum efficiency can be achieved under varying load conditions. Hence, a WPT system implementing the desired wireless PLL methodology could be used in real world applications and to maximise the WPT efficiency.

7.8. References

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8. Conclusion and further work

8.1. Conclusion

The thesis presents the work carried out to analyse, design and evaluate novel hardware and control methodologies to improve WPT systems. The outputs of the works contribute to the state of the art in WPT system design offering improvements in system reliability, reduced control complexity and methods to maximise efficiency in real-time with varying loads. In addition, the novel work presented can be applied to other applications such as induction heating or conventional power supplies. The findings have been peer-reviewed for presentation at learned society conferences and submitted for publication into journals.

State-of-the-art gate drive topologies were reviewed in Chapter 2, with the review showing that a conventional gate driver may suffer from false triggers and significant driving loss while new resonant gate driving approaches could reduce this driving loss but suffer from physical size constraints and control timing issues. A better solution can be achieved by using a well-optimised turn-on voltage and a small negative turn-off voltage but this requires a separate negative voltage supplier. Hence, in Chapter 3, a novel negative voltage generation circuit was introduced. By adding 18 additional components to a commonly found full bridge gate driving circuit, this discrete solution can generate the required negative voltage to achieve bipolar gate driving. Detailed descriptions of the operating theory were provided covering both high-side-only, half-bridge, and full bridge application. The potential issues when applying the desired circuit are analysed with solutions provided. An overview of the wireless transmitter design unitising the desired circuit is illustrated and calculations of key components are provided with experimental results shown the driving voltage versus different component combinations. The wireless power transmitter is built to demonstrate the driving waveform, start-up capability and improved overall performance.

To further improve the WPT system performance, reduce the size and improve reliability, a

matrix converter was selected to drive the wireless power system over a two-stage design. The advantage of using a matrix converter, such as improved efficiency, reduced size and enhanced robustness, was investigated in Chapter 2. However, the state-of-the-art matrix converter requires a complex and costly controller, which limits its deployment. Hence, in Chapter 4, a novel logic gate constructed middleware is proposed. The middleware enables the design of matrix converters by using controllers that are originally designed for full bridge converters. The working theory of the proposed middleware is described, along with logical table and equations. The simulation results are obtained and presented using spice simulation tools. Using the proposed middleware, a microcontroller dominated matrix converter was designed and built. The evaluation results showed the desired waveforms that demonstrate the circuit worked as expected, distributing and allocating the drive signal from a conventional controller to the power switches of single-phase matrix converter.

The matrix converter was then expanded to the design of a wireless power system in Chapter 5. By implementing the proposed matrix converter, a cost-effective wireless power system featuring reduced size and improved robustness was achieved. Furthermore, the design and implementation of a wireless power receiver for the later experiments were also described, featuring a high level of integration for control and power density. A description of its functionality along with designs and operations were provided. Meanwhile, the relationship between efficiency and phase angle of transmitting current against receiving voltage is analysed, showing that by minimising this phase difference improves system efficiency. Evaluation results of the matrix converter based WPT system using both the desired power receiver and simple rectifier were given which demonstrated that both power transmitter, receiver, and the whole system is operated as expected.

In Chapter 6, a novel resonant frequency tracking methodology for a wireless power receiver was proposed. The new approach estimates the real-time resonant frequency of the power receiver and provides feedback, based on which a practical phase shift control based maximum efficiency point tracking design can be implemented together with a novel wireless pseudo

synchronous triggering mechanism. The detailed working theory of pseudo synchronous triggering methodology is provided and later extended to a design of wireless digital storage synchronous sampling system, which allows the synchronous sampling of signals without physical connection between them. These methodologies were implemented into a design of a WPT system. A prototype was built that demonstrated the ability of both resonant frequency locking and the possibility of using components with higher tolerance.

Finally, Chapter 7 introduced a novel wireless phase locked loop methodology suited for WPT systems. Using the new control approach, a PLL-liked control scheme, which locks the transmitting frequency and resonant frequency of the power receiver, can be deployed. It is described how the phase difference is reported in the frequency domain, which significantly reduces the bandwidth requirement for a wireless feedback. The reduced bandwidth requirement also allows simplified data transceiver design, so that reduce the complexity and cost of deploying this phase shift control based maximum efficiency point tracking technology. Simulation results demonstrated the operations of sub-systems and presented the reduced communication bandwidth results. A prototype is built which connected to the existing wireless power system introduced in the previous chapters. Evaluation results presented show that the phase of transmitter voltage and receiver current can be successfully locked, meaning that the maximum efficiency can be achieved under varying load conditions. Hence, a wireless power system implementing the desired wireless PLL methodology could be used in applications with changing environmental conditions, coil positions and variable loads.

8.2. Further work

The research introduced in this thesis has presented a significant number of contributions to the state-of-the-art for WPT systems. There are a number of areas where further advances could be made based on the contributions contained herein.

8.2.1. Wireless charging for non-stationary objects.

In a wireless power system, the mutual inductance between the transmitting coil and receiving coil will vary along with the changes in distance and overlapped areas between coils. The mutual inductance also affects the resonant frequency of the power receiver, which is why WPT systems are not an obvious technology for moving objects. As described in Chapter 6, the maximum efficiency point tracking methodology could track the resonant frequency of the receiving resonator. Hence, for wireless powering non-stationary objects, utilising the maximum efficiency point tracking approach may able to compensate the mutual inductance introduced resonant frequency changes and maintain a reasonable efficiency to wirelessly powering a moving object.

8.2.2. Employing GaN power devices for wireless power transfer.

In recent years, GaN has shown promising benefits in power converter design. Its high switching frequency, low switching losses and high power density make it an ideal candidate to be employed in power converters used for wireless power transfer. The middleware described in chapter 4 may also be extended to be used with GaN power switches.