Analysis and Control of Modular Multilevel Cascaded Converter-Based Flexible AC Transmission Systems

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Abstract

Power quality issues are becoming more pronounced since the majority of modern day loads draw harmonic currents and consume reactive power. Increasing connection of renewable sourced generators to the utility network exacerbates the situation due to their use of power electronic converters for grid interfacing and their unpredictable generating nature. A particular challenge also lies in unbalanced current drawing, due to large single-phase loads, such as traction drives and renewable energy sourced generators. Such current accumulation may result in the voltage imbalance at the point of common coupling, posing threats to system stability and safe operation. The Flexible AC Transmission Systems (FACTs) such as shunt-connected active power conditioners (APC) can be used not only to eliminate the harmonics, but also compensate reactive power, hence enhance power quality. However for medium/high voltage applications the conventional two-level voltage source converter (VSC)-based types require bulky step-up transformers and high switching frequencies which are costly and inefficient.

This thesis investigates the use of Modular Multilevel Cascaded Converters (MMCC) to function as APCs under balanced and unbalanced load conditions. The particular topology explored employs a 5-level full-bridge flying capacitor converter as the sub-module, owing to its increased availability of switching states. The benefits of modularity and scalability offered by an MMCC make it an ideal topology to improve the power quality of medium/high voltage power grid.

For effective harmonic current mitigation high performance reference current extraction is important. The work proposes a novel technique which uses cascaded notch filters to identify a selection of dominant low-order harmonics in the load current, combining with a predictive + derivative current control scheme the method can offer accurate and fast harmonic current cancellations. This method has shown that it outperforms the conventional synchronous reference frame-based low-pass filtering scheme.

For an MMCC-based APC, inner capacitor voltage imbalance may occur particularly under unbalanced and distorted currents which can lead to converter failure. A new PWM scheme, the carrier permutation phase-shift PWM (CP PS-PWM), is proposed. The method rotates multiple triangular carrier waves to each voltage levels in a fixed sequence at the end of each fundamental period. This method has shown to mitigate the MMCC intra-cluster voltage imbalance effectively.

The MMCC phase voltage imbalance has been an issue for unbalanced compensation. To mitigate the problem an MMCC-APC in star connection needs a common zero sequence voltage injection and that in delta connection requires a zero sequence current injection. These may limit the operation ranges of the device, particularly when current is distorted. Analysis and comparison of the two configurations under

both unbalanced and distorted currents are performed. Experimental verifications are carried out, and the superiority of the delta configured MMFCC-APC is validated.

A key contribution of the work also lies in the development of an MMFCC-based Unified Power Flow Controller (UPFC). The new device has a direct AC-AC configuration. It has one terminals of the MMFCC shunt-connected directly to the power lines, and the other terminals are connected to the AC output ends of the two-level voltage source converter which is serially-connected in the transmission lines through a transformer. The work develops a complete control scheme for this MMFCC-UPFC to achieve transmission line power flow control. Simulation studies of this device on a simple two voltage sourced power network has shown that it performs as desired under varying real and reactive power flow demands.

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List of Abbreviations

AC	Alternating Current
DC	Direct Current
PCC	Point of Common Coupling
FACTs	Flexible AC Transmission Systems
HVDC	High Voltage DC Transmission
SVC	Static VAR Compensator
STATCOM	Static Synchronous Compensator
TCSC	Thyristor Controlled Series Capacitor
SSSC	Static Synchronous Series Compensator
UPFC	Unified Power Flow Controller
APF	Active Power Filter
APC	Active Power Conditioner
NPC	Neutral Point Clamped Converter
CHB	Cascaded H-Bridge
FCC	Flying Capacitor Converter
PLL	Phase Locked Loop
SRF-PLL	Synchronise Reference Frame PLL
DDSRF	Decoupled Double Synchronous Reference Frame PLL
MMCC	Modular Multilevel Cascaded Converter
MMFCC	Modular Multilevel Flying Capacitor Converter
SSBC	Single Star Bridge Cell
SDBC	Single Delta Bridge Cell
DSBC	Double Star Bridge Cell
DSCC	Double Star Chopper Cell
PS-PWM	Phase Shift-Pulse Width Modulation
PD-PWM	Phase Deposition-Pulse Width Modulation
ADC	Analogue to Digital Converter
DSP	Digital Signal Processor

Symbols

f_1	Grid voltage fundamental frequency
f_s	Switching frequency
T_s	Sampling period
V_s	Supply side voltage
V_R	Receiving side voltage
I_s	Supply side current
V_c	Converter side voltage
i_c	Converter side current
i_L	Load side current
M_a	Amplitude modulation index
M_f	Frequency modulation index
τ	Coefficient for the predictive controller derivative term
C_{DC}	DC capacitor voltage
C_{SM}	Submodule flying capacitor voltage
V_{DC_avg}	Average value of three-phase module DC capacitor voltages
I^+, I_p	Positive sequence current
I^-, I_n	Negative sequence current
I_1	Fundamental current element
I_h	h^{th} harmonic current element
K_{ir}	Degree of current imbalance
V_o, v_o	Zero sequence voltage
I_o, i_o	Zero sequence current

Chapter 1 Introduction

1.1 Background Literature

With the rapid population growth and worldwide economic development in the 21st century, both the consumption and installation of electric power are increasing continuously. Meanwhile, the conventional generation units relying on fossil fuels are gradually becoming obsolete due to the high amount of greenhouse gas emissions. This leads to the widespread use of renewable energy sources and power electronic devices. As a consequence the proliferation of power electronic controlled equipment in distribution systems, such as switch-mode power supplies, diode or thyristor controlled rectifiers, etc., brought about some undesirable effects. One of these is the drawing of harmonic current from the utility grid. Besides this, the surge in the input of power from a host of small, grid-connected renewable energy generators exacerbates the situation [1-5].

Harmonic distortion inevitably worsens the quality of power supplied to consumers, and affects power system operational stability, reliability and efficiency. There are also the issues of unbalanced voltage and current affecting normal operation of power networks, especially due to fault conditions across the distribution lines and large single-phase loads such as a 25 kV traction drive connections [6]. As the number of rail electrical locomotives increases, the requirement of traction power supply system is higher, consequently the issue of imbalance and harmonics problems are becoming more critical [7-9]. These issues cause devices malfunction, high losses but low power factor.

The use of passive compensators such as capacitor banks and filters cannot completely compensate the power quality issues due to the traction load variations. There is a cost-effective solution called Flexible AC Transmission Systems (FACTs) [10], which is based on the power electronic infrastructure. These are not only for effective controlling the voltage and power flow of the network, but also for suppressing the harmonics efficiently. The key technology for attaining such aims is by using static equipment in AC transmission lines to provide more power control as well as green-field networks and have minimal environmental impact [11]. Since it uses static power electronic elements instead of mechanically moving parts, the response can be much faster than conventional devices such as a synchronous condenser.

1.2 Power-line Harmonics and Conventional Suppression Methods

1.2.1 Problems associated with harmonics

Products such as variable speed drives, switch mode power supplies and arc furnaces are familiar for domestic and industrial applications. However, they also introduce large amounts of harmonic currents into the power systems which have brought a series of problems.

Transformers and machines: When a current containing harmonics flows into a transformer, the winding copper losses will increase due to the total RMS current increases. Meanwhile, since the harmonics frequency is relative higher than the fundamental current, the transformer core losses will be increased as well. This additional losses will lead to the overheating of transformer, which reduce its efficiency and lifetime, even pose a potential fire risk. Similarly, the harmonics can have the damage on AC machines.

Conductors: The harmonic current flowing into conductors experiences a higher effective resistance, as a consequence the I^2R losses will increase [12]. On the other hand, the conductor current transmission capability is decreased due to a phenomenon called 'skin effect' [13]: The current tends to flow near the conductor's surface since its density becomes less uniform when frequency increased.

Besides, all the large capacitors (such as capacitive compensator) with high frequencies current flowing will present a relative low reactance. This leads to the magnitude of current flowing through the capacitors increasing and may damage the devices. Likewise, the existence of harmonics may affect the voltage quality at PCC, hence the connected loads will increase their losses but reduce the performance even failure.

1.2.2 Standards for limitation of current harmonics

The Institute of Electrical and Electronics Engineers. IEEE has stipulated a certain regulation IEEE-519 (2014) [14] on the level of current harmonics. Table 1.1 shows a selection of this document, which specify the maximum harmonic current that the consumer can inject into the grid. The IEEE-519 is an international standard which is adopted by many countries. However, since the power system infrastructures in each country are quite different, the Energy Networks Association produces an Engineering Recommendation (ER) G5/4-1 [15] standard for the UK harmonic distortion limits. Table 1.2 shows the harmonics current limits based on a typical supply network with fault level of 10MVA from this G5/4-1 standard.

Table 1.1 IEEE 519-2014 Current Distortion Limits (<69kV)

Maximum Harmonic Current Distortion (% of I_L)						
Individual Harmonic Order (Odd Harmonics)						
$I_{SC}{}^a/I_L{}^b$	$3\leq h\leq 11$	$11\leq h\leq 17$	$17\leq h\leq 23$	$23\leq h\leq 35$	$35\leq h\leq 50$	TDD[c]
< 20	4.0	2.0	1.5	0.6	0.3	5.0
20 < 50	7.0	3.5	2.5	1.0	0.5	8.0
50 < 100	10.0	4.5	4.0	1.5	0.7	12.0
100 < 1000	12.0	5.5	5.0	2.0	1.0	15.0
>1000	15.0	7.0	6.0	2.5	1.4	20.0

a: I_{SC} = maximum short-circuit current at PCC

b: I_L = maximum demand load current (fundamental frequency component) at the PCC under normal load operating conditions

c: TDD = Total Demand Distortion

Table 1.2 ER G5/4-1 Maximum Permissible Harmonic Current Emissions Limits

Harmonic order	Frequency (Hz)	Current in RMS (A)	Harmonic order	Frequency (Hz)	Current in RMS (A)
1	*50*	-	27	*1350*	*0.5*
3	*150*	*48.1*	29	*1450*	*3.1*
5	*250*	*28.9*	31	*1550*	*2.8*
7	*350*	*41.2*	33	*1650*	*0.4*
9	*450*	*9.6*	35	*1750*	*2.3*
11	*550*	*39.4*	37	*1850*	*2.1*
13	*650*	*27.8*	39	*1950*	*0.4*
15	*750*	*1.4*	41	*2050*	*1.8*
17	*850*	*13.6*	43	*2150*	*1.6*
19	*950*	*9.1*	45	*2250*	*0.3*
21	*1050*	*0.7*	47	*2350*	*1.4*
23	*1150*	*7.5*	49	*2450*	*1.3*
25	*1250*	*4.0*			

1.2.3 Conventional suppression methods

The conventional suppression methods are normally based on passive filtering techniques, which are consist of capacitors, inductors and/or resistors. Meanwhile, the combinations can vary from a simple RL filter connected in series with the line, to a more complex LC filter to tuned for a particular harmonic frequency band, namely as band-pass and band-stop filters. These techniques are effective, however, they brought several shortcomings including large size, expensive and the limited compensating characteristics imposed by the filter and its ineffectiveness in regulating the amount and type of harmonics it needs to compensate [16]; for example, passive

filter parameters are difficult to change dynamically in order to remove harmonics of varying frequencies [17].

1.3 Flexible AC Transmission Systems

The FACTs are installed to regulate the network power flow quality at different critical points, and were initially devices such as phase-shifting transformers, fixed or mechanical switched inductors, and capacitors. When the requirement for flexibility became higher, more and more devices were proposed and became part of the FACTs family. Currently they can be classified into three groups containing shunt and series compensation which means the FACTs devices are connected in parallel or series with a power system to improve the electricity quality, as shown in the Table 1.3 below.

Table 1.3 FACTs Devices

	Shunt-connected	Series-connected
First Generation	Static VAR Compensator (SVC)	Thyristor Controlled Series Capacitor (TCSC)
Second Generation	Static Compensator (STATCOM)	Static Synchronous Series Compensator (SSSC)
Third Generation	Unified Power Flow Controller (UPFC)	

1.3.1 Static VAR Compensator

The first generation of the grid shunt-connected devices is called the Static VAR Compensator (SVC). The fixed value inductor or capacitor banks are connected in parallel with the lines to absorb or generate reactive power for the grid via the thyristor valves, while the former called thyristor controlled reactor (TCR) and the latter is thyristor switched capacitor (TSC), as shown in Fig. 1.1. The effective values of their susceptance are controlled by the power electronic switches.

It can be seen that both TCR and TSC are simple and cost-effective devices; however, this technology requires the calculation of the number of switched-in or off inductors and capacitors every time instant. Also because of the thyristor switching and the inductor's properties, the TCR needs a shunt capacitor filter to reduce low frequency current harmonics, which increases the power loss and cost. TSC has the advantage of producing no harmonics, but it is difficult to limit the capacitor's charging current during switch-on transients. The Siemens, ABB and GE Grid companies still produce this device commercially [18-20].

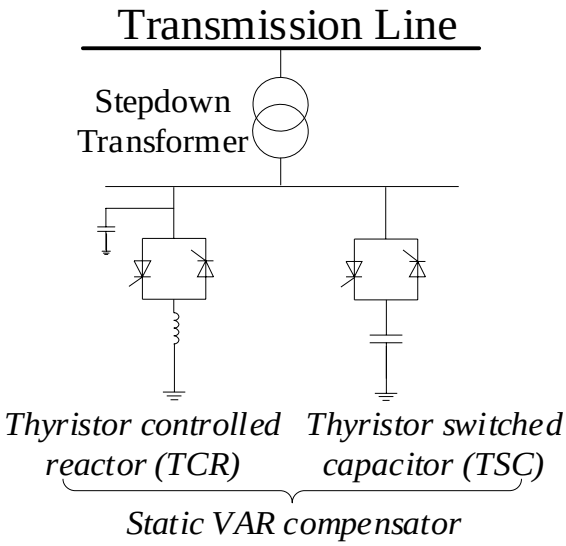


Fig. 1.1 Static VAR Compensator

1.3.2 Static Synchronous Compensator

The second generation of the shunt-connected compensator called the Static synchronous compensator (STATCOM), was proposed in the 1980s, and became widely developed in the 1990s [21], resulting in several large capacity examples being installed in a number of countries: ±80MVar in Japan (1991) [22]; ±100Mvar in USA (1995) [23] and ±8MVar in a 24MW wind farm in Denmark (1997) [24]. In its basic form a STATCOM consists of a voltage source converter (VSC) with a DC energy storage device, mostly a capacitor, and associated control circuit. It is connected in shunt with the AC system and often through a stepdown transformer, as shown in Fig. 1.2.

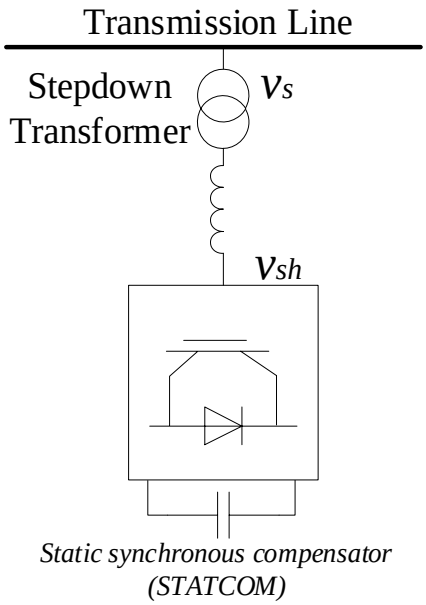
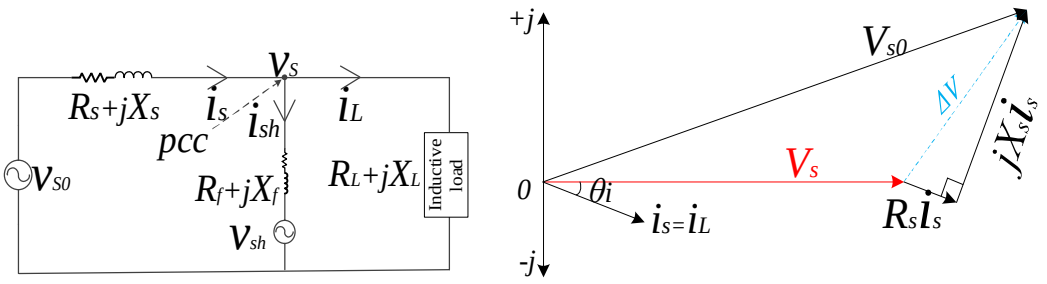


Fig. 1.2 Static synchronous compensator (STATCOM)

The simplified circuit of a balanced power network with a STATCOM connecting to the point of common coupling (PCC) is shown in Fig. 1.3. It represents a voltage source v_s supplying for the load with impedance $Z_L = R_L + jX_L$ via a transmission

line with impedance $Z_s = R_s + jX_s$. Without the STATCOM, the source current i_s flows from the voltage source end to the load end and lags the PCC voltage, as shown in Fig. 1.3(b), where the PCC voltage is regarded as reference, $v_s = V_s\angle 0°$.



(a) (b)

Fig. 1.3 (a) Simplified circuit of a balanced power network; (b) the circuit phasor diagram without STATCOM compensation

With the STATCOM compensating for reactive power, the network can achieve either voltage regulation $|V_s| = |V_{s0}|$ or unity power factor $\theta_i = 0$. The phasor diagrams of these two operation modes are as shown in Fig. 1.4: the converter injected current i_{sh} will add into the original load current i_L in order to control the current i_s flowing through the transmission line impedance. When the i_s is controlled to be leading V_s by θ_{i_sh}, as shown in Fig. 1.4(a), the magnitude of PCC voltage $|V_s|$ can be the same as $|V_{s0}|$. Similarly, the i_s can be controlled to be in phase with V_s by changing the STATCOM injected reactive current, as shown in Fig. 1.4(b).

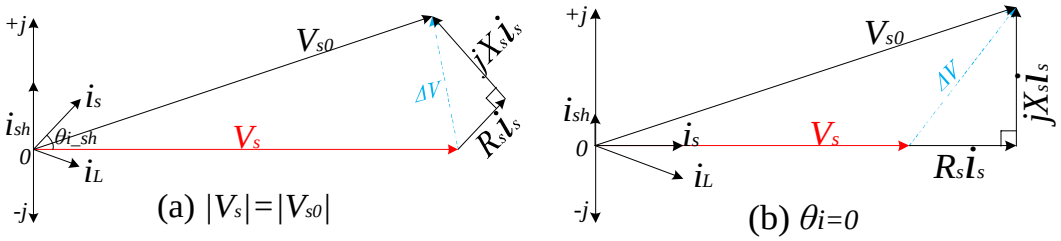


Fig. 1.4 STATCOM reactive power compensations: (a) Voltage regulation and (b) unity power factor

1.3.3 Thyristor Controlled Series Capacitor

The Thyristor Controlled Series Capacitor (TCSC) is the first generation of series-connected compensation device, which is a combination of thyristor controlled capacitors and reactors. It is normally installed in between two nodes in a transmission system, providing the dynamic control of line reactance as shown in Fig. 1.5.

The TCSC became commercially applied since 1990s in the transmission lines at the 345kV Kanawa River Substation, the 230kV Kayentta Substation and 500kV Slatt Substation respectively [25-27]. In nowadays, the TCSC devices are still available for customers from ABB and Siemens [28, 29].

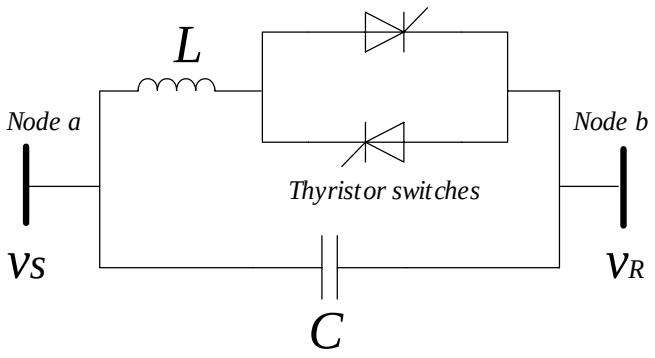


Fig. 1.5 Thyristor controlled series capacitor (TCSC)

1.3.4 Static Synchronous Series Compensator

The Static Synchronous Series Compensator (SSSC) is the second generation of series connected compensation products. Its main form is comprised of a DC source and VSC connected to the transmission line through a series transformer, as shown in Fig. 1.6. The SSSC laboratory applications appear in [30-32] while its commercial products are not as common as the other FACTs devices, and are mostly found as early installed parts of UPFCs, such as at the Inez Substation and Kangjin Substation [33, 34].

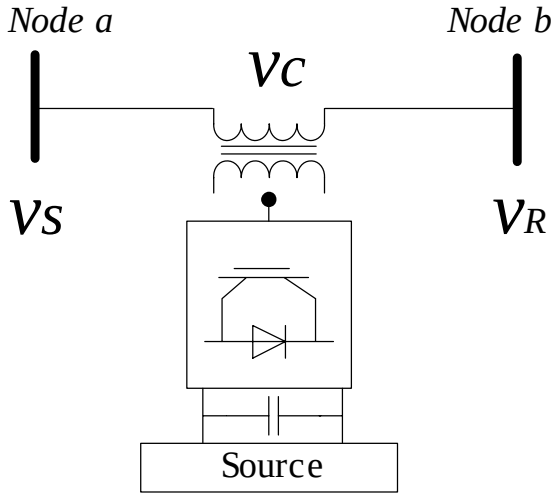


Fig. 1.6 Static synchronous series compensator (SSSC)

The simplified circuit of a balanced power network with SSSC connection is shown in Fig. 1.7(a). It represents a transmission line in between of two nodes denoted by voltage sources v_s and v_R. The SSSC can be regarded as a controllable voltage source v_c connected in series of the line, which injects a variable magnitude and 0-360° angle. The line impedance is $Z_s = R_s + jX_s$. Fig. 1.7(b) shows the corresponding phasor diagram where the sending end voltage is regarded as the reference, $v_s = V_s\angle 0°$. Since the v_c is controllable, the effective v_R and line impedance can be changed thus the line power flow is controllable. The SSSC compensation can be concluded in three main modes or any combination of the three. The details will be introduced in the Chapter 6.

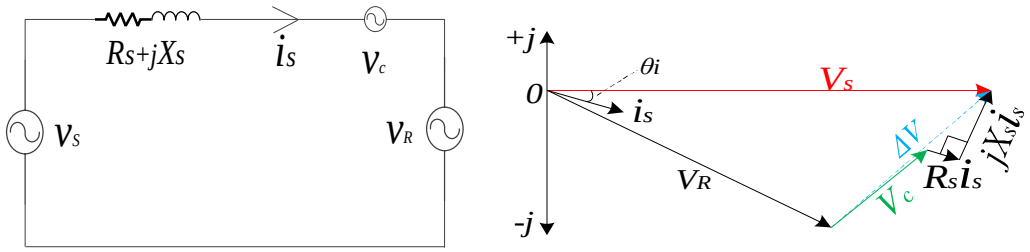


Fig. 1.7 (a) Simplified circuit of a balanced power network with SSSC connection and (b) the corresponding phasor diagram

1.3.5 Unified Power Flow Controller

The third generation FACTs device is called the Unified Power Flow Controller (UPFC), as shown in Fig. 1.8. It is a combination of STATCOM and SSSC, which means it is the most versatile device among FACTs. A UPFC can realise simultaneous voltage regulation, line impedance compensation and phase angle adjustment, hence achieving flexible independent control of real and reactive power flow along the compensated transmission lines and increasing power transfer capability and dynamic stability margins.

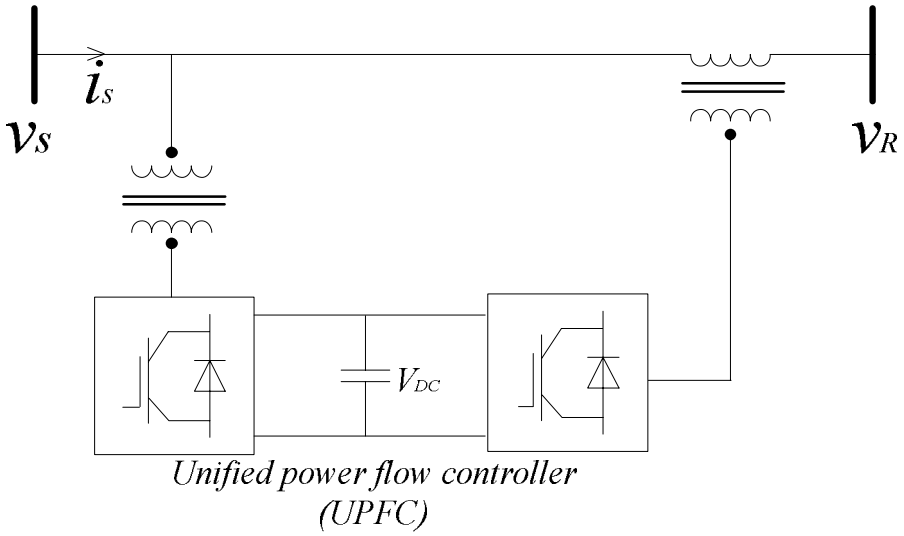


Fig. 1.8 Unified Power Flow Controller (UPFC)

Fig. 1.9(a) shows the simplified circuit of a balanced power network with the UPFC system. v_{s0} and v_R denote the voltages at two nodes while v_s is the voltage at the PCC. The series connected controller of the UPFC, v_c, controls the real and reactive power flow of the line whilst the shunt connected controller v_{sh} regulates the PCC voltage and maintains the DC-link capacitor at its nominal voltage value. Fig. 1.9(b) shows the corresponding phasor diagram where the PCC voltage is regarded as the reference. The details will be introduced in the Chapter 6.

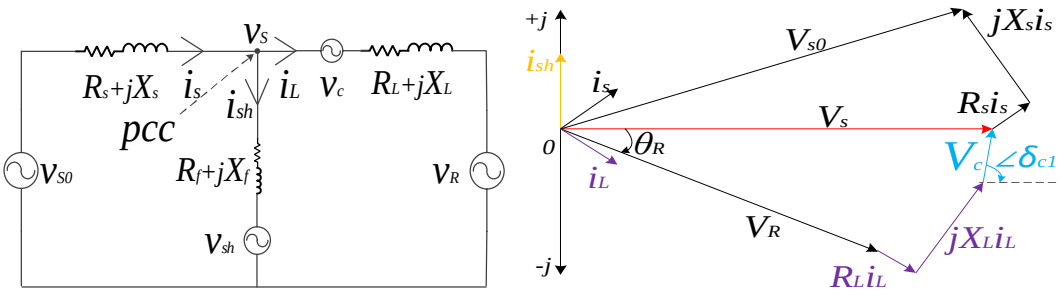


Fig. 1.9 (a) Simplified circuit of a balanced power network with UPFC system and (b) the corresponding phasor diagram

1.3.6 Active Power Filters

The evolution of FACTs devices has also promoted the development of power electronics-based active filtering techniques. Modern active filtering is superior in performance, smaller in physical size and more flexible compared with traditional filters. Besides, the active filters designed for power conditioning are not only for harmonic filtering, but also referred to as reactive power control for power factor correction and voltage regulation, load balancing control etc., and hence also can be recognised as ‘active power filters’, ‘active power conditioners’, ‘active power quality conditioners’, etc. [35].

An Active Power Filter (APF) is largely based on a voltage source converter (VSC), with a DC link capacitor connected at its input for stabilising its operation while it is controlled to generate the current harmonics required by the load bus [36, 37]. Similar to FACTs, the APF can be classified into two groups according to their circuit configurations: shunt active filters and series active filters [38], as shown in Fig. 1.10.

A shunt active filter, same configuration with STATCOM, can provide current harmonics elimination, load imbalance correction and reactive power compensation. As shown in Fig. 1.10(a), under an appropriate control strategy, the distorted load current is feedback into the converter hence the device will inject a compensating current to the PCC thus achieving harmonics cancellation.

The series active filter configuration is same with SSSC, as shown in Fig. 1.10(b). Similarly, it will inject a controllable voltage through the series transformer into the network in order to suppress the voltage harmonics. It also can be applied for reactive power compensation, eliminate voltage sag/swell, and unbalanced voltage compensation [39]. However, the series device cannot be used for current imbalance issues.

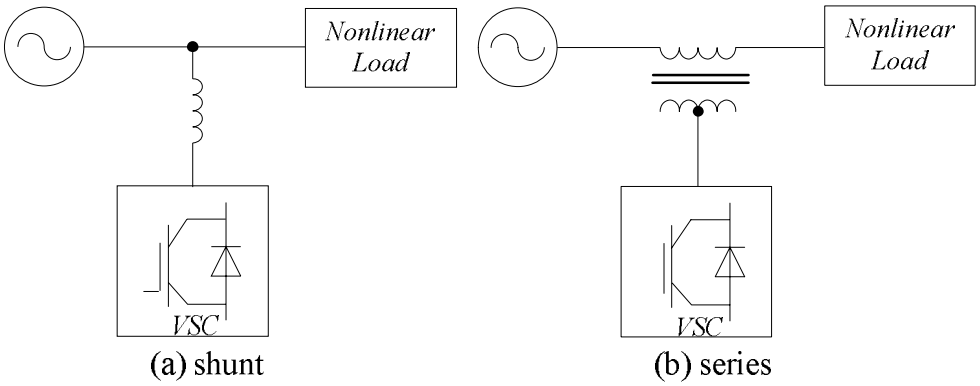


Fig. 1.10 Active Power Filter configurations

1.4 Multilevel Converter Topologies

The introduction of multilevel converters offers the replacement of conventional two-level converters in the medium power level applications such as FACTs. The concept of these converters can date back to the early 1970's [40] and the configurations are formed by multiple semiconductor switches, clamping diodes or capacitors and one DC source. It can be seen that the voltage pressures of the DC source are distributed by all the switches hence the requirement on each switch will significant reduce. Also, the resultant AC voltage output waveform is synthesized by multiple distinctive levels hence less harmonics and losses can be achieved. The well-known multilevel converters include the Neutral point clamped (NPC), the Flying capacitor converter (FCC) and Cascaded H-bridge (CHB) [40-49]. However, although the multilevel converters have been well-developed, they still present certain challenges such as cost and control complexity [41].

1.4.1 Neutral Point Clamped Converter (NPC)

The neutral point clamped converter (NPC) was original proposed by Nabae et al. in the 1980s [50]. It is also referred to as the 'Diode clamped converter' or 'Multipoint clamped converter', due to the didoes 'clamped' between each semiconductor switch and the neutral point. Fig. 1.11 shows a 3-phase 5-level NPC converter circuit, where each phase contains four switches and two clamped diodes to produce the multilevel voltage outputs. In a consequence, the NPC converter has been widely adopted in the medium voltage applications (2.3 to 6.6 kV) [41].

However, this topology has drawbacks of high cost when more voltage levels were required; each voltage level is produced by a pair of switches and two extra clamped diodes per leg. Therefore, extending this circuit means the increasing number of diodes, which is less attractive.

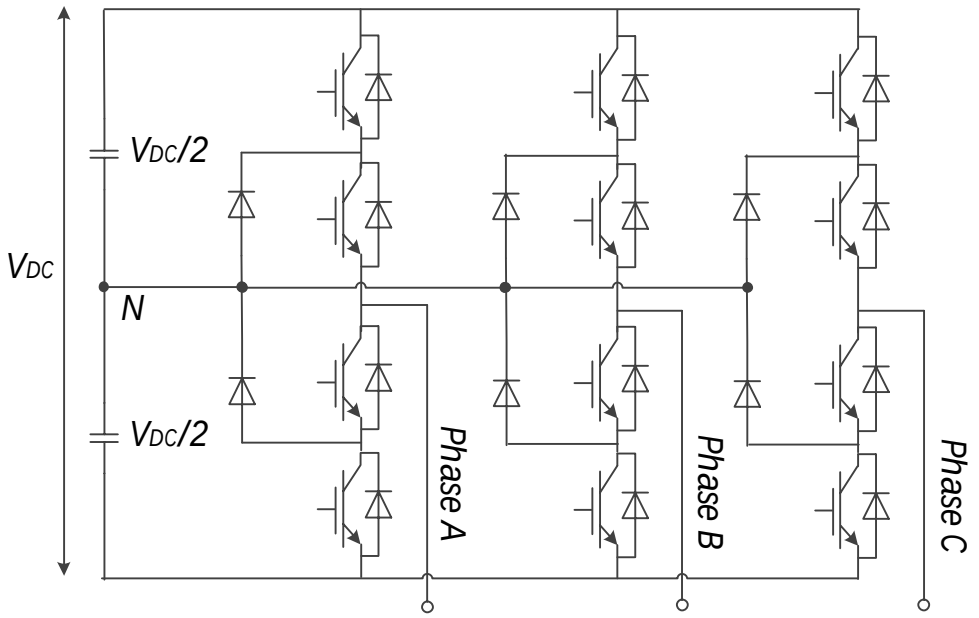


Fig. 1.11 3-phase 5-level NPC converter topology

1.4.2 Cascaded H-Bridge (CHB)

This topology was proposed by Marchesoni et al. in 1990 [51]. It is consist of several 2-level H-bridge converter cells connecting in series for each phase. Fig. 1.12 shows a 5-level CHB converter circuit, which contains 6 H-bridge converters in total. The major drawback of this circuit is that each cell has its own DC power supply, which means the DC voltage balancing becomes an indispensable issue.

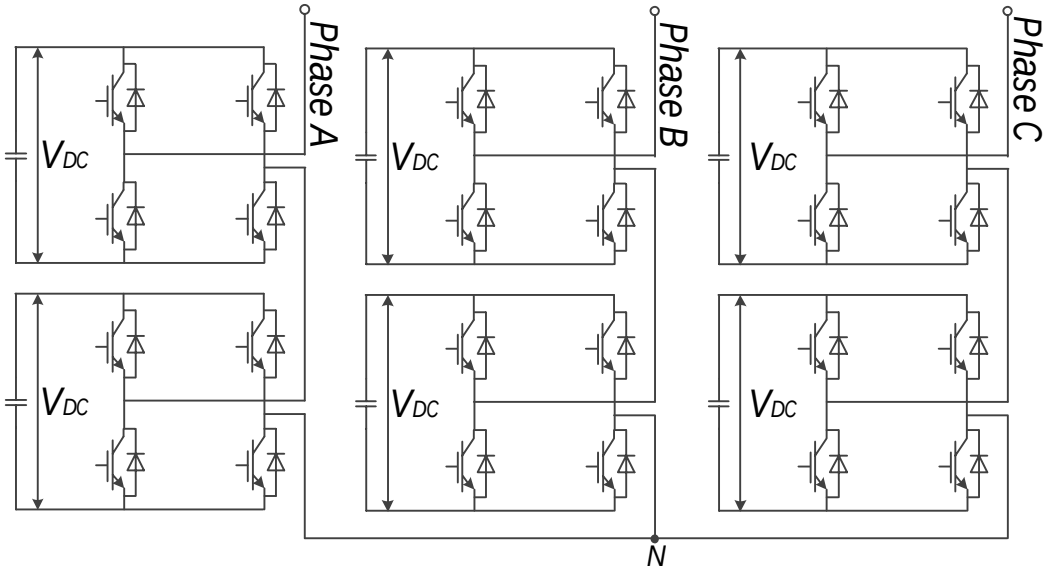


Fig. 1.12 3-phase 5-level CHB converter topology

1.4.3 Flying Capacitor Converter (FCC)

The flying capacitor converter (FCC) was developed by Meynard and Foch in 1992 [45]. Similar with NPC, this topology uses capacitors to instead of the clamped didoes,

namely ‘flying capacitors’, as shown in Fig. 1.13. The adoption of more capacitors in such circuit requires for more space, more cost and more concerns of voltage balancing issues. However, the flying capacitors provide benefit of additional ‘redundant’ switching states for the same voltage output levels, which helps to sharing the switching stress among the whole device.

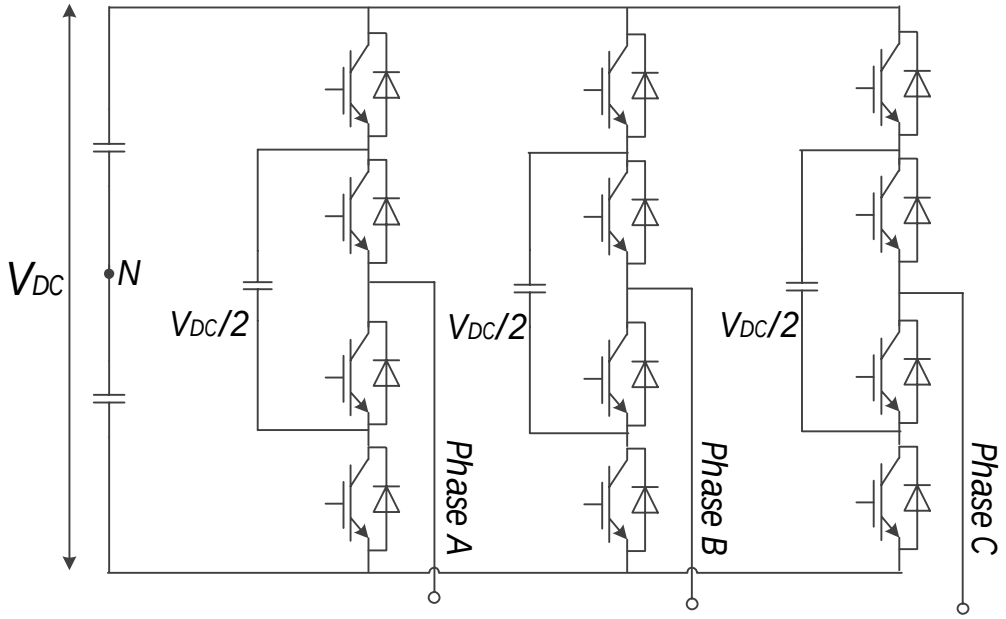


Fig. 1.13 3-phase 5-level FCC converter topology

1.5 Grid Voltage Synchronisation Techniques

Power electronics converter-based devices used for grid power control, such as FACTs, should be effective regardless the power system voltage quality changes. This requires the device terminal voltage to be synchronised with the grid voltages fast and accuracy. The synchronisation schemes should hold the following features:

- Be robust when the grid voltage quality is poor such as voltage distortion, or even unbalanced such as voltage sags and swells;
- Track the grid voltage frequency and angle precisely no matter how they changed;
- Remain synchronised to gird voltage under distorted condition by filtering the harmonics.

The grid synchronisation schemes can be divided into open-loop and closed-loop methods, as shown in Fig. 1.14.

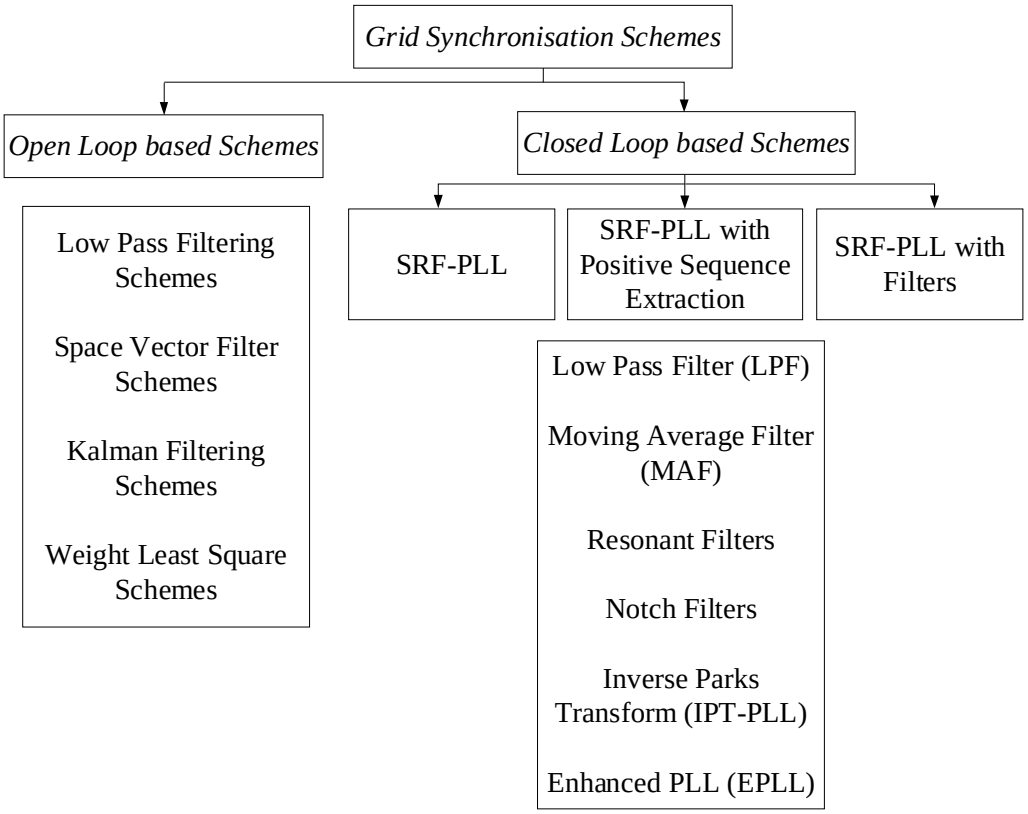


Fig. 1.14 Grid synchronisation schemes

1.5.1 Open-Loop Schemes

The open-loop schemes estimate the fundamental voltage component frequency and phase angle directly by processing instantaneous samples. However, the results are highly sensitive to noise and dependent on signal filtering ability [52]. As listed in Fig. 1.14, five different open-loop schemes are reviewed and compared [52].

- **Low Pass Filtering Schemes**: The grid voltage feedback signals are filtered via a Low-pass filter and the phase lag are compensated by a co-ordinate transformation matrix. The drawback is that the lower cut-off frequency cause the response slower and high sensitivity to voltage unbalance or phase jumps.
- **Space Vector Filter Schemes**: This scheme is based on the grid voltage signals in α-β frame. It behaves well when phase jumps and harmonic distortion occur, but introduces a phase-shift when the gird frequency varies.
- **Kalman Filtering Schemes**: This scheme can work in distorted and unbalanced system without introducing any phase jumps, however, the shortcoming is their higher convergence time [53], difficulty in selecting the optimal weighting matrices and computationally intensive.
- **Weight Least Square Schemes**: This scheme is suitable for unbalance situation and used to estimate the positive and negative sequence separately. However, it is sensitive to harmonic distortions [54].

1.5.2 Closed-Loop Schemes

The closed-loop schemes operate in a closed-loop structure hence the error can be regulated to zero. A basic structure of the closed-loop scheme is shown in Fig. 1.15, consists of the phase detector (PD), loop filter (LF) and voltage controlled oscillator (VCO) three fundamental parts. The PD is usually implemented by applying a Park transformation and measures the phase difference between the input and output signals. Then the LF provides a constant error signal for the VCO to generate phase angle output.

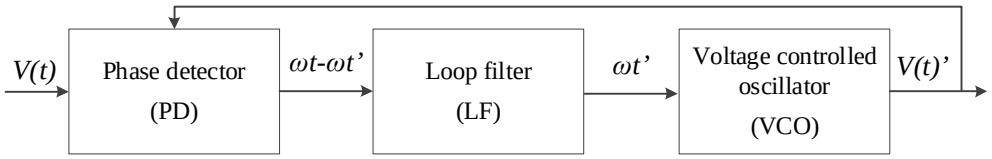


Fig. 1.15 Basic structure of closed-loop PLL schemes

Fig. 1.14 shown that the most well-known and spread closed-loop methods are based on the synchronous reference frame PLL (SRF-PLL) [55, 56]. Similar approaches with equivalent drawbacks are the pq-PLL, which are based on the instantaneous real and imaginary power theory [57, 58]. They can be divided into following categories.

- **SRF-PLL**: This scheme works well for balanced voltage condition, however, 2nd order harmonic may be introduced in an unbalanced voltage condition. Hence, the loop filter bandwidth can be reduced but increase further delay.
- **SRF-PLL with Filters**: The above scheme can be adjusted by adding an additional filter before the Loop filter. This includes low-pass filters [59][60] moving average filters [61, 62], resonant filters [63] and notch filters [60]. The drawback is that additional delay may be incurred by adding the extra filter.
- **SRF-PLL with Positive Sequence Extraction**: This scheme is particular suitable for unbalanced voltage conditions. It relies on extracting the voltage positive sequence component before sending to the phase detector. Various PLL schemes that use this scheme include the decoupled double synchronous reference frame (DDSRF) and cascaded delay signal cancellation (CDSC-PLL).

Furthermore, the SRF-PLL can be extended to the decoupled double second order general integrator-phase locked loop (DSOGI-PLL) scheme. In this subsection, the SRF-PLL with Filters, DDSRF-PLL and the DSOGI-PLL are discussed while the SRF-PLL is applicable for balanced systems, DDSRF-PLL is applicable for unbalanced systems.

1.5.2.1 Synchronous Reference Frame-Phase Lock Loop (SRF-PLL)

To estimate the angular position of the rotating reference frame which is the grid voltage vector, the SRF-PLL forces its output signal to synchronize with the input voltage reference signal in both angle and frequency [64]. As shown in Fig. 1.16, the three-phase voltage is firstly transformed into *dq* SRF form through Park's transformation (as shown in Equation 1.1) and then the *q*-component signal is employed as the input to a Loop Filter which is typically a PI controller, to minimize

the frequency (phase angle) error [59]. However, the input 3-phase voltage signal could be noisy or unbalanced in practice which introduces some sort of harmonics into the converting *dq* components, therefore a low-pass filter (LPF) is required before the PI controller for the purpose of achieving more precise DC signal for the loop.

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \sin(\theta) & \sin(\theta - \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3}) \\ \cos(\theta) & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{1.1}$$

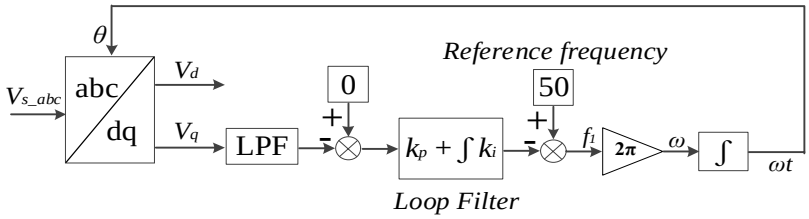
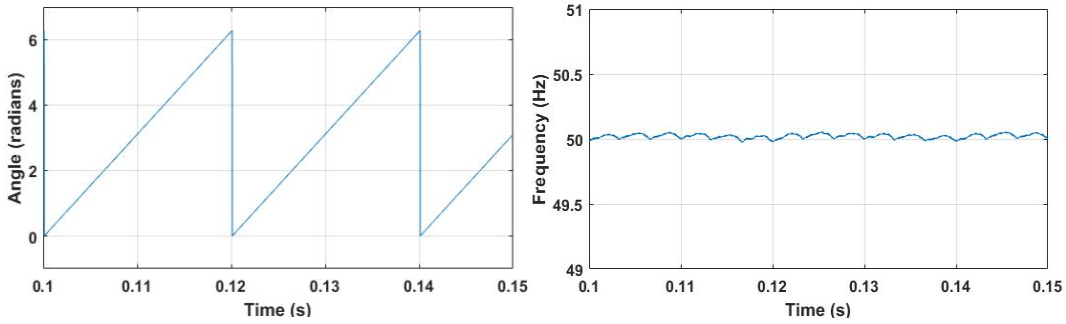


Fig. 1.16 SRF-PLL block diagram

Fig. 1.17 shows the results of SRF-PLL generated phase angle $\theta=\omega t$ and frequency f_1 for a 50Hz balanced grid voltage, whilst the former increases from 0 to 2π (6.283) every 0.02sec cycle and the latter keeps steady with small ripples at 50Hz.



(a) (b)

Fig. 1.17 SRF-PLL output (a) angle $\theta=\omega t$ and (b) frequency f_1=50Hz

1.5.2.2 Decoupled Double Synchronous Reference Frame-Phase Lock Loop (DDSRF-PLL)

When the system is unbalanced, the SRF-PLL cannot generate a precise angle due to the input voltage feedback containing negative sequence component and being noise. The reduced of LPF bandwidth may mitigate the issue but will introduce further delay. In 2007, P Rodríguez et.al. proposed the Decoupled Double Synchronous Reference Frame-PLL scheme (DDSRF-PLL) for unbalanced applications [65], which adopts two synchronous reference frames, dq^{+1} rotating with positive angular velocity ω and dq^{-1} rotating with negative angular velocity $-\omega$ respectively, namely double synchronous reference frames (DSRF). The corresponding phasor diagram is shown below.

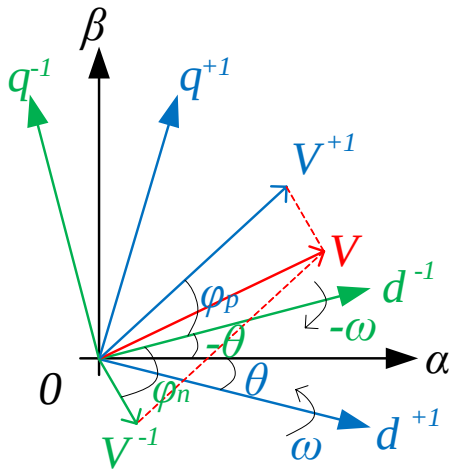


Fig. 1.18 Double synchronous reference frames

Fig. 1.18 indicates that the unbalanced voltage vector v can be decomposed into positive and negative sequence vectors in the dq^{+1} and dq^{-1} rotating frames respectively. The equations of the two vectors are expressed as

$$v_{dq}^{+} = \begin{bmatrix} v_d^{+} \\ v_q^{+} \end{bmatrix} = V^{+} \begin{bmatrix} \cos\varphi_p \\ \sin\varphi_p \end{bmatrix} + V^{-} \left[T_{dq}^{+}\right] \begin{bmatrix} \cos\varphi_n \\ \sin\varphi_n \end{bmatrix} \tag{1.2}$$

$$v_{dq}^{-} = \begin{bmatrix} v_d^{-} \\ v_q^{-} \end{bmatrix} = V^{-} \begin{bmatrix} \cos\varphi_n \\ \sin\varphi_n \end{bmatrix} + V^{+} \left[T_{dq}^{-}\right] \begin{bmatrix} \cos\varphi_p \\ \sin\varphi_p \end{bmatrix} \tag{1.3}$$

where $\left[T_{dq}^{+}\right] = \left[T_{dq}^{-}\right]^{T} = \begin{bmatrix} \cos 2\omega t & \sin 2\omega t \\ -\sin 2\omega t & \cos 2\omega t \end{bmatrix}$. Equations (1.2) and (1.3) illustrate that the both the positive and negative vectors containing not only DC component, but also 2ω cross-coupling oscillatory terms.

The block diagram of the DDSRF-PLL is shown in Fig. 1.19. It is actually an extension of SRF-PLL. After the unbalanced vector signal be decomposed into the two frames, the oscillatory terms shown in above equations will be cancelled by the decoupling network. Consequently the signals sending into the SRL-PLL become absolute DC. More details will be discussed in the Chapter 4.

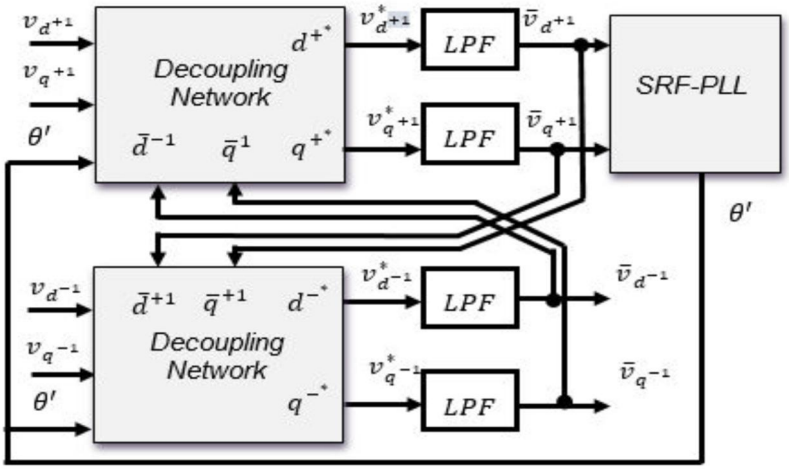


Fig. 1.19 Block diagram of Decoupled Double Synchronous Reference Frame-PLL

1.5.2.3 Decoupled Second Order General Integrator-Phase Locked Loop (DSOGI-PLL)

This is another scheme for unbalanced system, which contains four main parts as shown in Fig. 1.20. (1) Clark transformation; (2) Second Order Generalized Integrator – Quadrature Signal Generator (SOGI-QSG); (3) Positive-Negative Signal Calculator (PNSC) and (4) SRF-PLL [66].

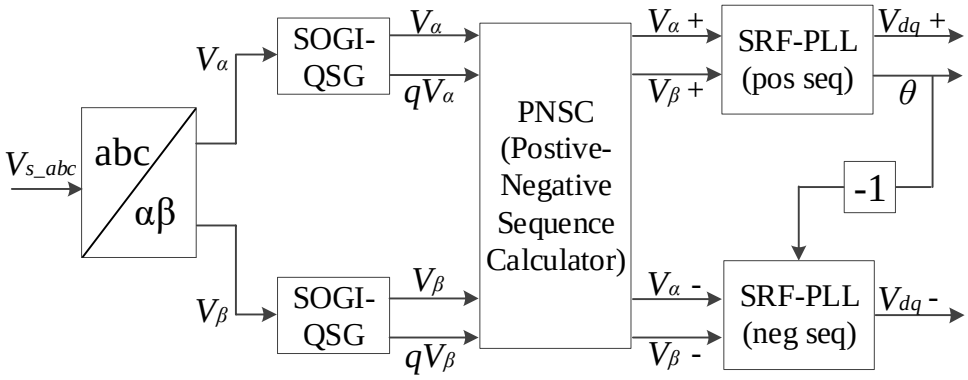


Fig. 1.20 Block diagram of Decoupled Second Order General Integrator-PLL

The grid voltage is firstly transformed into quadrature signals by the QSG based on the SOGI. Then the signals are sent to the PNSC in order to extract the positive and negative sequence signals separately. Finally the signals are fed into the SRF-PLL and generate corresponding angle signals.

Compare the above three schemes, it is clear that the SRF-PLL is the simplest to implement, which is the most suitable for balanced voltage condition; for the DDSRF and DSOGI PLLs, they both can work under unbalanced voltage condition. However, the DSOGI is more complicated than DDSRF, and it requires the grid frequency acting as a feedforward control variable signal, which means the performance of this scheme may degrade if the grid frequency is differing from the nominal value; In DDSRF scheme, the cross-coupling terms can reduce the output signal oscillations but the LPFs may reduce the response speed during transient state. In this thesis, the SRF-PLL and DDSRF-PLL are chosen to be implemented for the balanced and unbalanced conditions respectively.

1.6 Aims, Objectives and Thesis Structure

The overall aim of this research is to investigate the applications a Modular Multilevel Cascaded Converter (MMCC) as an Active Power Conditioners (APC) and Unified Power Flow controller (UPFC) to compensate for harmonics and unbalanced load current, control the line real and reactive power flow respectively. The key objectives of this research work are to:

- Investigate and compare different MMCC topologies and configurations in terms of footprint, cost and control complexity;
- Analyse and compare different multilevel pulse width modulation (PWM) schemes for the applications of MMCC;

- Develop a carrier permutation PS-PWM to prevent the MMCC intra-cluster submodule capacitor voltages drifting away;
- Develop a harmonic current and negative sequence current extraction scheme which is suitable for unbalanced harmonic load compensation;
- Analyse, simulate and experimentally validate a MMFCC-based APC system for balanced and unbalanced nonlinear load compensation;
- Design and simulate a MMFCC-based UPFC system for transmission line real and reactive power flow control.

The structure of the thesis is as follow:

Chapter 2 reviews the details of existing various MMCC submodule topologies and configurations. An evaluation of the MMCC configurations with different submodule topologies is presented based on their footprint, cost and performance. Furthermore, two different multilevel PWM schemes are introduced and compared in this chapter in terms of their harmonics bands and THDs.

Chapter 3 presents an MMFCC-based APC which is capable of performing both active power filtering and reactive power control for a balanced power system containing complex load. A novel carrier permutation PS-PWM scheme was proposed to avoid the unbalanced of intra-cluster submodule capacitor voltages. Meantime, the abrupt rate-of-change in generation of current harmonics was solved by a predictive controller with a derivative action method. Finally, the simulated results were presented.

Chapter 4 analyses the MMFCC-based APC application for simultaneously compensating load reactive power, eliminating load current harmonics and rebalancing load current at the supply end. Two different reference current extraction schemes were proposed and compared in terms of harmonics tracking speed and accuracy. Meantime, two zero sequence components are applied for star and delta-connected configurations to overcome the inter-cluster voltage balancing issues separately. This chapter also revealed a better MMCC configuration for cancelling harmonics and compensating unbalanced component.

Chapter 5 discusses the experimental setup and validation of the MMFCC for harmonics and unbalanced current compensation. The MMFCC digital control system were presented. The experimental results based on the star and delta configured MMFCC were finally presented and compared.

Chapter 6 presents a novel MMCC-based UPFC system in order to achieve higher flexibility but lower losses. The operating principle of this novel device and corresponding control schemes were explained. Finally, the simulated results were presented.

Chapter 7 summarises the findings during the research and provides the future research recommendations.

The summary of novelty is claimed as follow:

- A carrier permutation PS-PWM scheme for the MMCC intra-cluster submodule voltage balancing control;
- A predictive controller with derivative action method for minimizing the delay between converter and reference currents;
- A low-pass filter based and a cascaded notch filter based reference current extraction schemes for the MMCC working under unbalanced harmonics condition;
- An MMCC inter-cluster voltage balancing control based on zero sequence voltage and current injections for SSBC and SDBC respectively;
- The comparison of SSBC and SDBC in terms of unbalanced harmonic current compensations;
- A novel MMCC-based UPFC system for the grid power flow control.

Chapter 2 Modular Multilevel Cascaded Converters and Multilevel PWM Schemes

2.1 Introduction

Modular MultiLevel converters proposed originally by Leniscar and Marquardt as M2LC in [67], for medium/high voltage and power applications, have now gained attention from industry. Their applications are seen in grid-connected converters, STATCOMs, HVDC transmission systems and medium voltage drives. The basic configuration of this topology stems from the classical cascaded H-bridge converter (CHB). This uses a two-level H-bridge converter as the basic module and connects several such modules in a series chain to form a phase limb. With this structure, it brought a number of favourable features; an MMCC is modular, hence it is easy to scale up the voltage level, and has voltage waveforms with very low harmonic contents. The very simple cell structure also reduces the manufacturing costs. It is also fault-tolerant as it can be reprogrammed to bypass a faulty module or to generate reduced voltage. The switching and clamping devices used for this topology are rated at submodule level, so that reduced voltage stress device ratings can be used. There were different names proposed and applied for this converter topology and in 2010, Akagi reviewed and classified this family of converters in [68], adopted 'Modular Multilevel Cascaded Converter' (MMCC) as the representative.

There are several MMCC submodule (SM) topologies and this chapter presents a detailed review of those which have been well-applied by researchers, including the 2-level half bridge converter, 3-level H-bridge converter, 5-level flying capacitor and 5-level neutral point clamped topologies. For each of these topologies, the flexibility in controlling the operation of the converter is analysed through a complete investigation of the available operating states of all its switching devices. Various MMCC configurations with different submodule topologies are compared with a view to finding the best type for STATCOM applications; the factors considered include the footprint, cost and performance (redundancy and control complexity). This chapter also reviews the pulse width modulation schemes for MMCCs with a comparison of harmonic levels and THDs at different switching frequencies.

2.2 MMCC Submodule Topologies

The phase limb of an MMCC consists of a stack of submodules (SMs) with a buffer inductor connected either on the top or bottom of the chain. The inductor limits the in-rush current to the device during faults and start-up, and also filters harmonics caused by the PWM switching. The various types of SMs will now be analysed.

2.2.1 Two-level half-bridge converter submodule

The configuration of a half-bridge (chopper) converter SM is shown in Fig. 2.1(a), where there is a pair of complementary switches, S_{1a} and S_{2a}, with their respective anti-parallel diodes. The switches are serially linked with each other and a DC energy storage unit (i.e. capacitor, super-capacitor or battery) is connected across them. Each SM can produce two voltage output levels, namely 0 V when S_{2a} is on and S_{1a} is off, and $+V_{DC}$ when S_{1a} is on and S_{2a} is off. When there is an inductive load in the AC side of the circuit, the output current lags the voltage and flows through diodes D_{2a} while S_{1a} is turned off. The current flowing through the module capacitor C_{DC} is bi-directional due to the anti-parallel diodes: when the AC side is a load, current flows from converter to the AC terminal, the converter operates in inversion mode and capacitor is discharged; Conversely when the AC side is a source current flowing direction is reversed, the converter operates in rectification mode and the capacitor is charged up. Hence, this submodule type allows a 2-quadrant power transfer operation (AC to DC, DC to AC), as shown in Fig. 2.1(b).

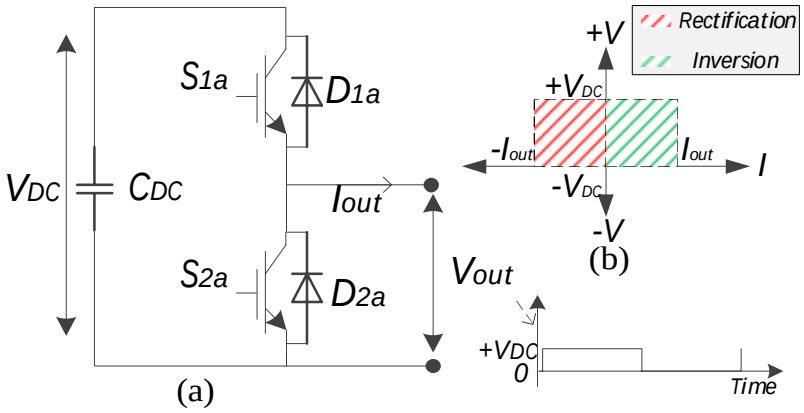


Fig. 2.1 (a) Half-bridge SM circuit; (b) Operating quadrants

2.2.2 Three-level H-bridge converter submodule

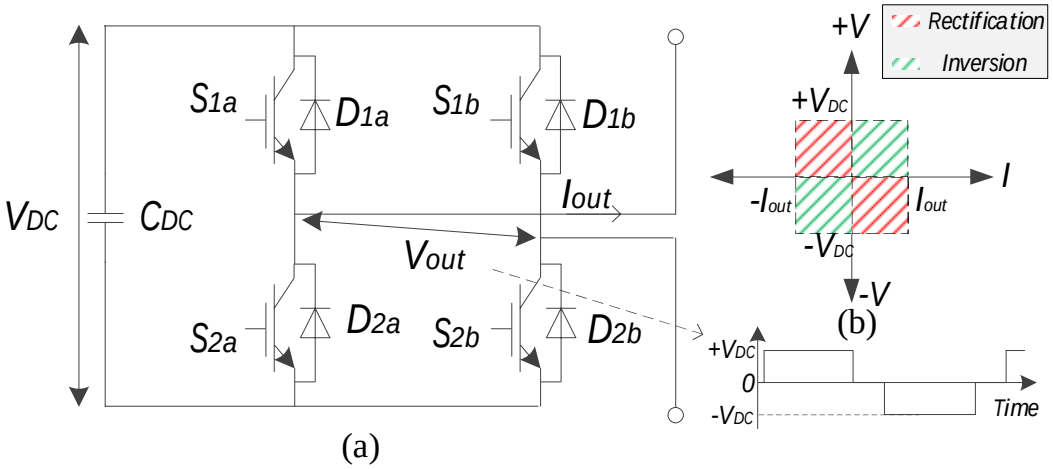


Fig. 2.2 (a) H-bridge SM circuit; (b) Operating quadrants

The H-Bridge as a chained converter submodule was proposed by Robicon Corporation in the mid-1990s for a medium-voltage motor drive [69]. Meanwhile, Lai and Peng presented the investigation of STATCOM applications based on the cascaded H-Bridge (CHB) MMCC [46]. As shown in Fig. 2.2(a), this circuit has four switches (S_{1a}, S_{2a} and S_{1b}, S_{2b}) with their antiparallel diodes, forming two parallel arms. The output terminals are the centre points of the two arms. The voltage across these terminals has a 3-level bipolar waveform as shown in Fig. 2.2(b). Similar to that in the previous subsection, an analysis of the current flow can be made and the power transfer between V_{DC} and V_{out} terminals is found to be bidirectional. This can be achieved when V_{out} is either positive or negative and thus the converter is capable of operating in 4 quadrants. Notably the H-bridge has redundant switching states when producing the zero output voltage.

2.2.3 Three-level flying capacitor (FC) half-bridge submodule

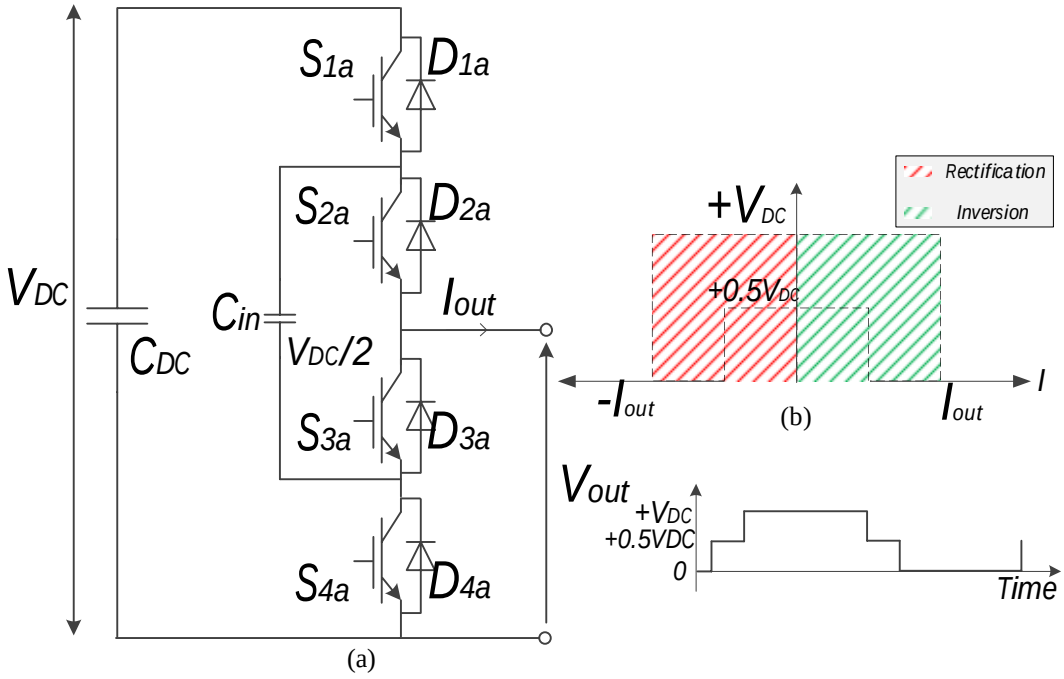


Fig. 2.3 (a) FC half-bridge SM circuit; (b) Operating quadrant

As shown in Fig. 2.3(a), the 3-level FC half-bridge submodule circuit comprises 2 pairs of complementary switches, (S_{1a}, S_{4a}) and (S_{2a}, S_{3a}) where each switch still has an anti-parallel diode connected. An inner capacitor, C_{in}, is connected across the inner complementary switch S_{2a} and S_{3a} while the outer module capacitor, C_{DC}, is connected across all the four switches. This topology can generate 3 unipolar voltage levels, namely 0, $+0.5V_{DC}$ and $+V_{DC}$. The outcome from the analysis on the current flow is similar to the case in Section 2.2.1 and thus, the 2-quadrant rectifying and inverting mode operations are depicted in Fig. 2.3(b).

2.2.4 Five-level full-bridge flying capacitor converter submodule

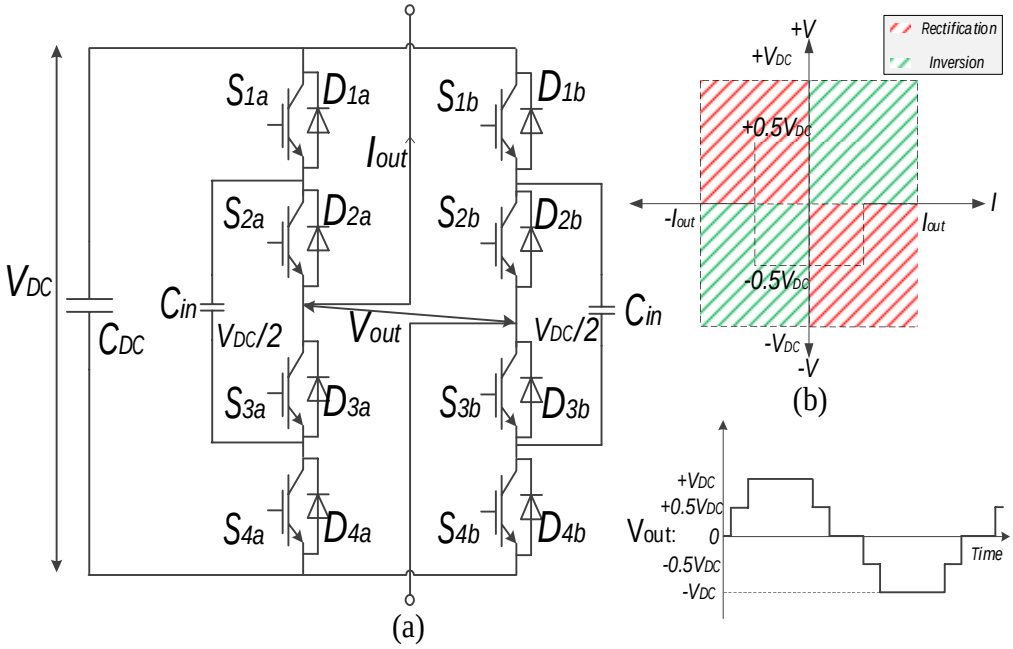


Fig. 2.4 (a) Full-bridge FCC SM circuit; (b) Operating quadrant

The configuration of a 5-level full-bridge FCC SM is shown in Fig. 2.4(a), where there are 4 pairs of complementary switches (S_{1a} , S_{4a}), (S_{2a} , S_{3a}), (S_{1b} , S_{4b}) &(S_{2b} , S_{3b}) and again each switch has an anti-parallel diode. Two inner flying capacitors are connected respectively across the two inner complementary switches S_{2a} - S_{3a} and S_{2b} - S_{3b}. Only one outer capacitor C_{DC} is required. The voltage across each of the two inner capacitors is half of that across the outer SM capacitor. This SM can produce 5 voltage levels from positive to negative and has 4-quadrant operation (as depicted in Fig. 2.4(b)). The complete switching states with freewheeling states for the FCC SM can be up to 32 as illustrated in the Appendix A.1. This feature allows the FCC to provide additional 'redundant' switching states comparing with other SMs when building the same voltage distinctive levels. Consequently, the switching stress can be shared to the whole device more averagely.

Currently, researches on the applications of using FCC as MMCC SM has received relatively less attention than the others topologies. However, its advantages make it is still worth to be studied. Hence, this topology has been researched and validated extensively by the University of Leeds.

2.2.5 Five-level neutral point clamped (NPC) converter submodule

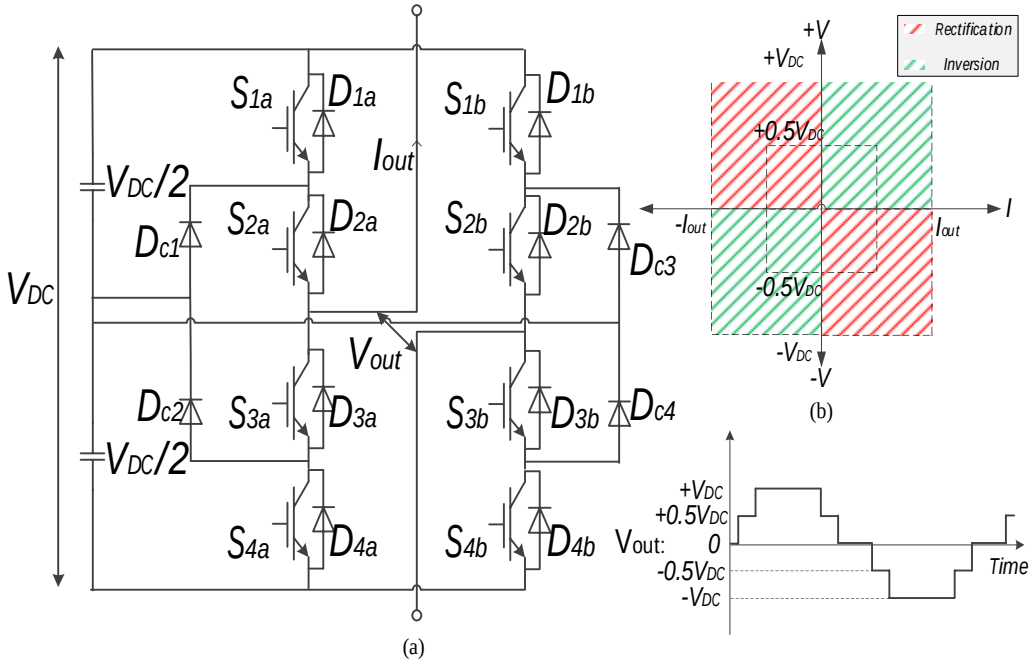


Fig. 2.5 (a) NPC SM circuit; (b) Operating quadrant

The 5-level NPC configuration was proposed by Baker [70, 71] and Nabae et al [50] in the 1980s, and the application of this topology in MMCCs was proposed by M. Carpaneto [72]. It is similar in operation to the 5-level FCC circuit, while 4 extra 'clamping' diodes are required and their connections are shown in Fig. 2.5. The complementary switches of this topology are still the same as in the FCC, they are (S_{1a}, S_{4a}), (S_{2a}, S_{3a}), (S_{1b}, S_{4b}), (S_{2b}, S_{3b}) with their anti-parallel diodes. The 4 additional diodes are D_{c1}, D_{c2}, D_{c3} and D_{c4}. They clamp the voltage nodes between the series connected switches to the DC-link mid-point. This topology allows a 5-level voltage output and 4-quadrant operation (as shown in Fig. 2.5(b)).

2.3 Three-Phase Modular Multilevel Converter Configurations

The three-phase MMCC family has been reviewed and classified by Hirofumi Akagi [68] into the following categories: Single-Star Bridge Cells (SSBC), Single-Delta Bridge Cells (SDBC), Double-Star Bridge Cells (DSBC) and Double-Star Chopper Cells (DSCC). The former two are characterised in the 'no common DC-link' group while the latter two are in the 'common DC-link' group. Their significant differences in configurations result in major variations of their performances and applications. There is also the Double Delta cell type which is not considered here because its benefits are not substantial enough to draw academic or industry's interests while its price is much higher compared with other configurations.

2.3.1 Single star bridge cells

The circuit diagram of a 3-phase single star bridge cell is shown in Fig. 2.6, which may comprise ***n*** SMs connected in series in each phase. The number of SMs is dependent on the grid voltage rating. The 3-phase arms are connected together at one end to form the neutral point and the other phase ends are connected to the 3-phase grid via a filtering inductor. Each of the SMs can be either a 3-level HB converter, or a 5-level FC or NPC converter or their hybrid configurations. The half-bridge chopper cannot be used in this type due to its unipolar output voltage feature.

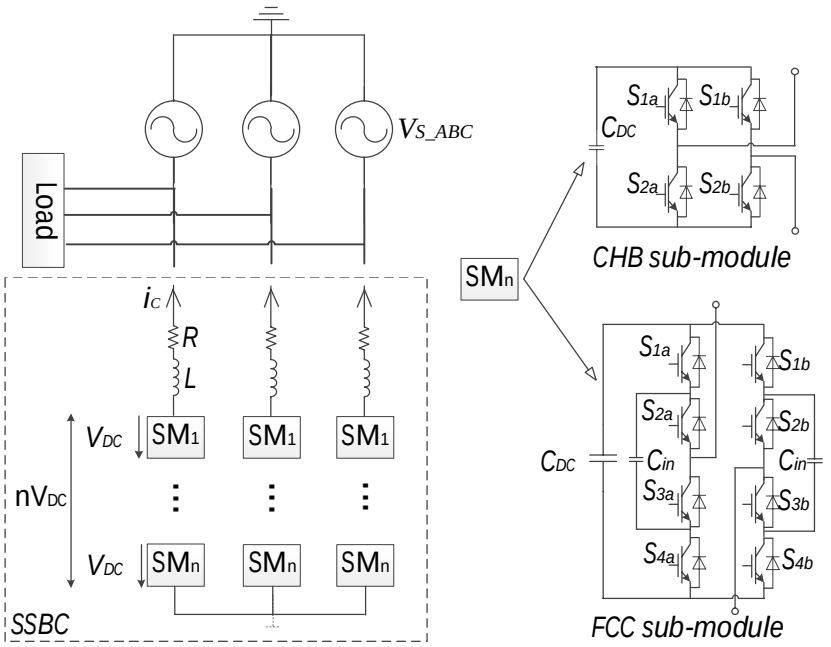


Fig. 2.6 Single star bridge cell

The fundamental phase voltage of a SSBC (before the filter) can be expressed as:

$$v_c(t) = nM_iV_{DC}\sin(\omega t + \theta_{vc}) \quad (2.1)$$

where n, M_i, θ_{vc} and V_{DC} represent, respectively, the number of SMs, amplitude modulation index, phase angle relative to the AC reference voltage and the submodule DC voltage. Modulation index M_i can vary from zero to a maximum of $4/\pi$ in the maximally overmodulated condition where all the modules generate co-phased square waves of zero – to – peak amplitude V_{DC}. M_i and the phase angle θ_{vc}, are determined by the switch control signals.

Considering the SSBC circuit with an R-L filter per phase, connected to the grid with voltage $v_s(t)$, and current flow between them $i_c(t)$, the dynamic equation for the converter terminal voltage can be given as

$$v_c(t) = v_s(t) - Ri_c(t) - L\frac{di_c(t)}{dt} \quad (2.2)$$

Substituting $v_c(t)$ by Equation (2.1) in the above formula, Equation (2.2) can be re-written as:

$$\frac{di_c(t)}{dt} = \frac{v_s(t) - nM_iV_{DC}\sin(\omega t+\theta_{vc})}{L} - \frac{R}{L}i_c(t) \quad (2.3)$$

Since the active power transfer between the DC and the AC side of the converter should be equivalent if losses can be neglected, the following equation of the power per cluster can be derived, where V_c and I_c are the RMS values of the AC side voltage and current waveforms.

$$nV_{DC}I_{DC} = V_cI_c \tag{2.4}$$

Thus, the time variation of the submodule DC voltage can be expressed as

$$\frac{dV_{DC}}{dt} = \frac{v_ci_c}{nC_{DC}V_{DC}} = \frac{M_i \sin(\omega t+\theta_{vc})\times i_c}{C_{DC}} \tag{2.5}$$

The state space model of SSBC output current i_c and DC voltage V_{DC} can be written as $\dot{x} = Ax + Bu$

where $\dot{x} = \begin{bmatrix} \frac{di_c}{dt} \\ \frac{dV_{DC}}{dt} \end{bmatrix}$, $A = \begin{bmatrix} -\frac{R}{L} & -\frac{nM_i \sin(\omega t+\theta_{vc})}{L} \\ \frac{M_i*\sin(\omega t+\theta_{vc})}{C_{DC}} & 0 \end{bmatrix}$, $u = \begin{bmatrix} v_s \\ 0 \end{bmatrix}$ and $B = \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & 0 \end{bmatrix}$.

2.3.2 Single delta bridge cells

The configuration of a 3-phase single delta bridge cell is shown in Fig. 2.7. Similar to SSBC, each phase arm (AB, BC and CA) contains ***n*** number of SMs in series, but the three phase arms are connected in a delta form rather than being connected at one end to form a common neutral point. An SDBC-based STATCOM has a clear advantage of being more capable in compensating unbalanced load current compared to the SSBC [73]; this feature will be analysed in detail in Chapter 4.

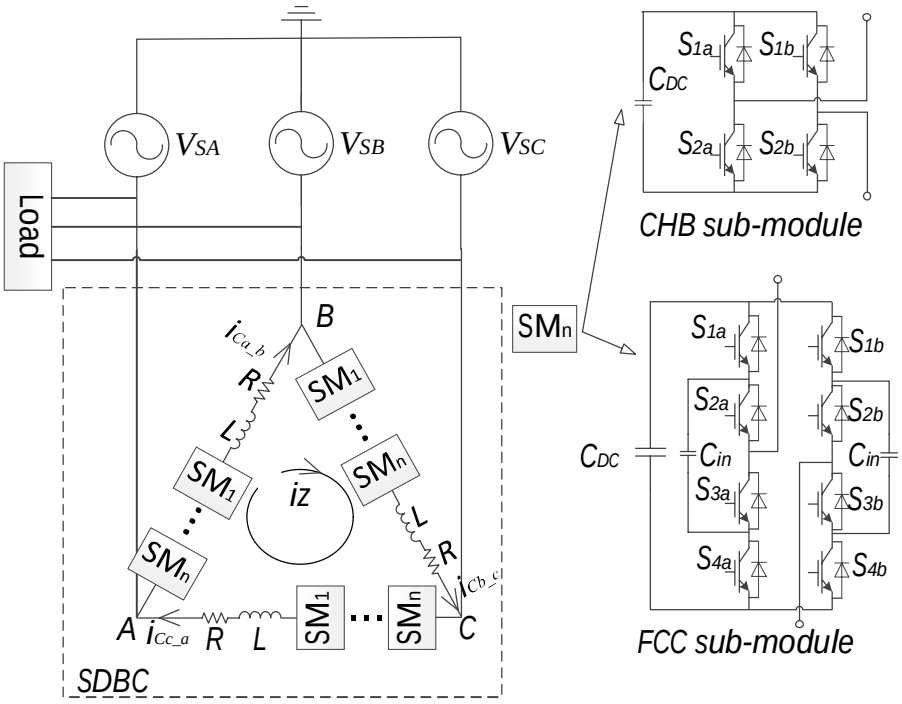


Fig. 2.7 Single delta bridge cell

The terminal voltages of a SDBC, $v_{cA\_B}, v_{cB\_C}, v_{cC\_A}$, should match with the grid phase voltages. The converter currents, $i_{ca\_b}, i_{cb\_c}, i_{cc\_a}$, flowing between its

terminals to the grid phase lines, are $\sqrt{3}$ times the currents flowing through each phase arm. The state space model of the SDBC has the same form as that of the SSBC model as expressed below.

$$\begin{bmatrix} \frac{di_{ci}}{dt} \\ \frac{dV_{DC}}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & -\frac{nM_i \sin(\omega t+\theta_{vc}+\frac{\pi}{6})}{L} \\ \frac{M_i * \sin\left(\omega t+\theta_{vc}+\frac{\pi}{6}\right)}{C_{DC}} & 0 \end{bmatrix} \begin{bmatrix} i_{ci} \\ V_{DC} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} v_{si} \\ 0 \end{bmatrix} \quad (2.6)$$

As mentioned, since there is no neutral point in the SDBC configuration, a circulating current i_Z would flow within the clusters of three phase arms. The triplen harmonic components in the current can circulate within the SDBC phase arms but are not injected to the grid, and this feature enables the SDBC to filter the triplen harmonic and its multiples.

The circulating current shown in Fig. 2.7 can be written as

$$i_z = \frac{1}{3}(i_{ca\_b} + i_{cb\_c} + i_{cc\_a}) \quad (2.7)$$

This i_z can play an essential role in the balancing of active powers for the three clusters, which enables the SDBC to control active and reactive power under unbalanced load conditions.

2.3.3 Double star cells

There are two types; Double Star Bridge Cells (DSBC) and Double Star Chopper Cells (DSCC). The former uses H-bridges as submodules and the latter uses simple two-level half-H-bridges (chopper), as shown in Fig. 2.8. The choice of them is based on the application requirements, but both have a common dc-bus and hence have been widely adopted by industry for HVDC systems.

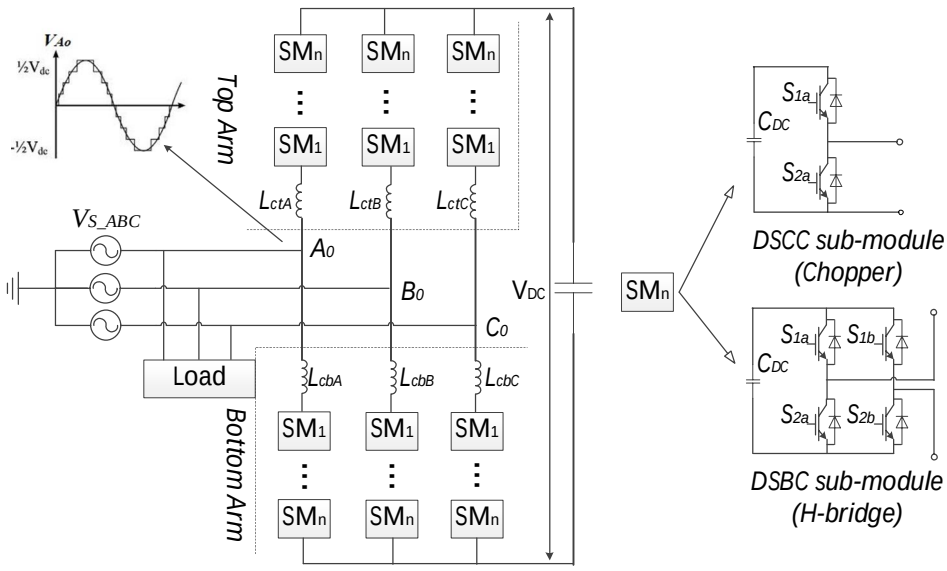


Fig. 2.8 Double star cells

Both the DSBC and DSCC are formed by six arms, three upper ones and three lower ones. The upper three are tied at one end and connected to the positive DC bus, while the lower three are tied to the negative DC bus, hence forming two star-connected

configurations. The other ends of the three upper and lower arms are tied according to their respective phases, through arm reactors L_{ctA}, L_{ctB}, L_{ctC}, L_{cbA}, L_{cbB} and L_{cbC} which are important for filtering and controlling circulating current. The three paired arms formed are connected to the three phase AC source at A_0, B_0 and C_0 as shown in Fig. 2.8. The number of chained SMs in each arm depends on the voltage rating requirements.

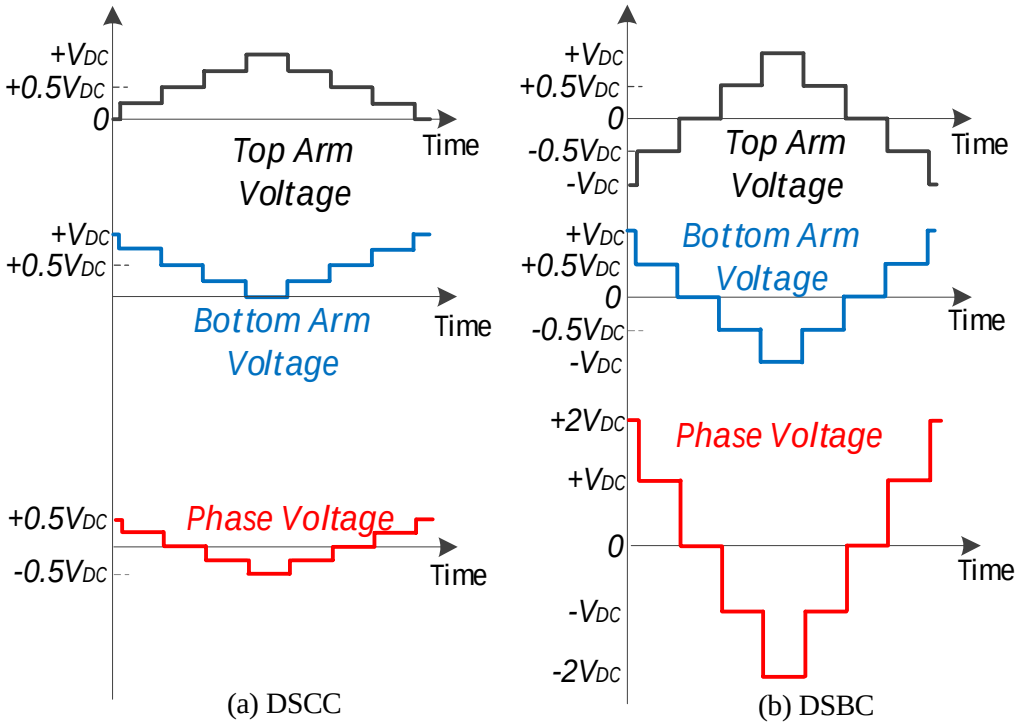


Fig. 2.9 Voltage waveforms of top, bottom arms and phase voltage for (a) DSCC and (b) DSBC

For DSCC, each half-bridge submodule produces only a two-state output voltage; $+V$ or 0, where V is the voltage of the SM capacitor as discussed in subsection 2.2.1. In normal operation each arm of a phase limb synthesises one half of a sine wave at the AC terminal. For synthesising the sine wave positive half cycle of terminal voltage, the SMs in the upper arms of each phase limb have their S_{1a} off and S_{2a} on sequentially to give '0' states, while the lower arm SMs all are in '$+V$' state. Conversely for generating the negative half cycle, the upper arm SMs are all in '$+V$' state while the SMs in lower arm are in '0' state, as shown in Fig. 2.9(a).

For the DSBC the individual H-bridge SM can produce a three-state output voltage: 0, $+V$ and $-V$. The main attractive features are: the magnitude of the phase voltage generated by the DSBC is twice that of the DSCC while both cells are equally rated (Fig. 2.9(b)); the DSBC can provide both buck and boost functions for the DC-link voltage, thus making it suitable for a grid-connected inverter with a variable DC source voltage condition, such as obtained from renewable energy sources [74].

The three main merits of the DSBC and DSCC are summarised as

- Phase arms having multiple capacitors giving distributed capacitive energy storage;
- Modular structure facilitates assembly, voltage scaling up or down, and fault maintenance;
- Lower switching frequencies for AC voltage with low THD.

The DSBC carries the disadvantage that it requires a higher number of switching devices and hence it costs more. However, the DSBC can isolate the DC buses from AC side by turning off all the switches and thus is able to block large short circuit current flowing from AC side to DC buses when a fault occurs on the DC side, while the DSCC cannot disconnect both sides and has the corresponding shortcoming of not being able to block short circuit current. This is an uncontrollable short circuit which can cause irreversible damage if not interrupted or limited.

2.3.4 Emerging hybrid converter topologies

The MMCC utilisations have recently received more attention in HVDC and FACTs applications due to their ability to synthesise nearly pure sinusoidal waveforms. For the necessities of higher efficiency, lower cost and DC-fault blocking capability, academic and industrial researchers proposed the hybrid converter topologies: parallel-hybrid configuration and series-hybrid configuration, while an example of these is the Alternate Arm Converter (AAC) [75] and the Series Bridge Converter (SBC) [76].

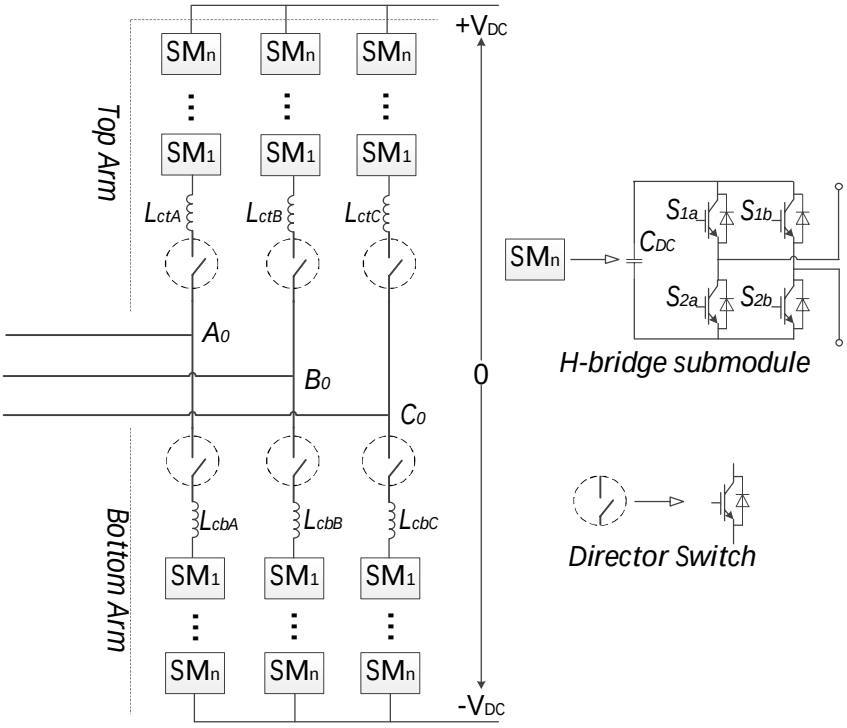


Fig. 2.10 Alternate Arm Converter (AAC) schematic diagram

AAC offers one solution to the DC fault vulnerability. The schematic of an AAC is as illustrated in Fig. 2.10. Similar to the DSBC discussed in the previous subsection,

each phase limb comprises two arms connected in series, and each arm has a stack of H-bridge submodules and a Director Switch (DS). In steady-state operation, to synthesize the positive half of a sine wave, the upper DS is turned on and all SMs in this arm, which have three switching states '*+V*', '0' and '*-V*', are in '*+V*' states. Meanwhile the lower arm DS is off and SMs are in '*-V*' state. For negative half wave, the lower arm DS is turned on and SMs are in '*+V*' states, while the upper arm DS is off and its SMs are in '*-V*' states.

The advantage of producing the AC voltage by using the appropriate arm while 'turning off' the opposite arm in every half fundamental cycle is in enabling it to be built with fewer cells than a normal MMC, hence achieving lower losses.

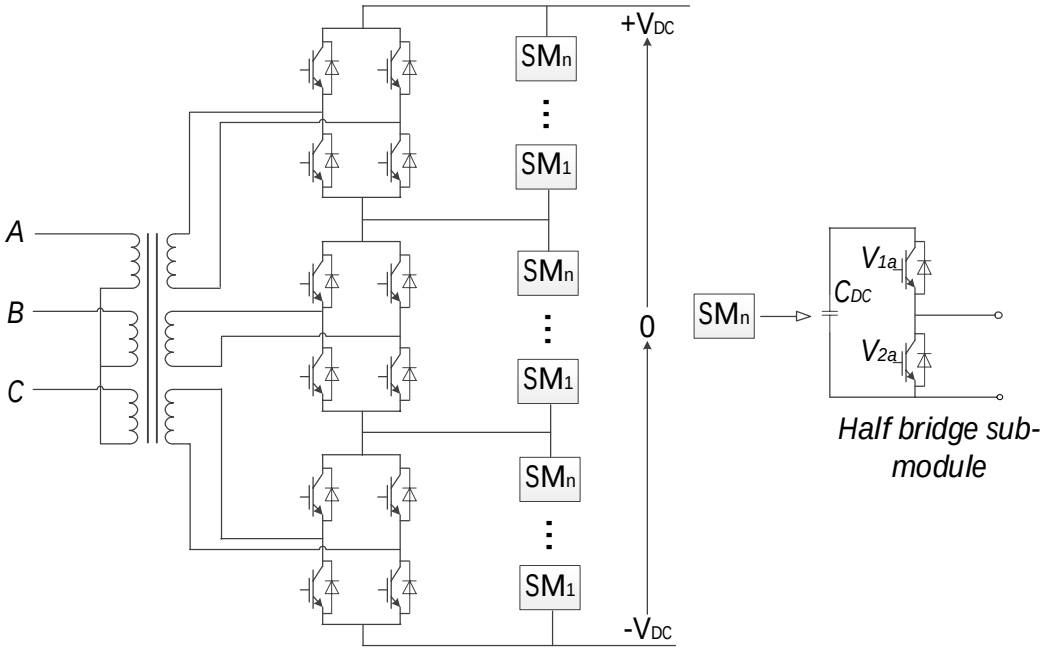


Fig. 2.11 Series Bridge Converter (SBC) schematic diagram

Fig. 2.11 shows the SBC circuit, which is made up of an H-bridge circuit connected in parallel with a series string of module (chain-link) for each phase. Each 'chain-link' will produce a full wave rectified multilevel waveform and then 'inverted' into a sinusoidal AC waveform and displaced 120º of phase angle from each other by the H-bridge arrangement. Such topology helps to reduce drastically the switching loss of the H-bridge IGBT.

2.4 Comparison of MMCC configurations

The various MMCC configurations and submodule topologies discussed in the previous sections are now compared from the aspects of footprint, cost, and performance in the application to a STATCOM system.

Footprint: The footprint of a power electronic device is important, particularly to those applications which have space limitations, such as an aerospace component, electrical vehicles and offshore wind power systems;

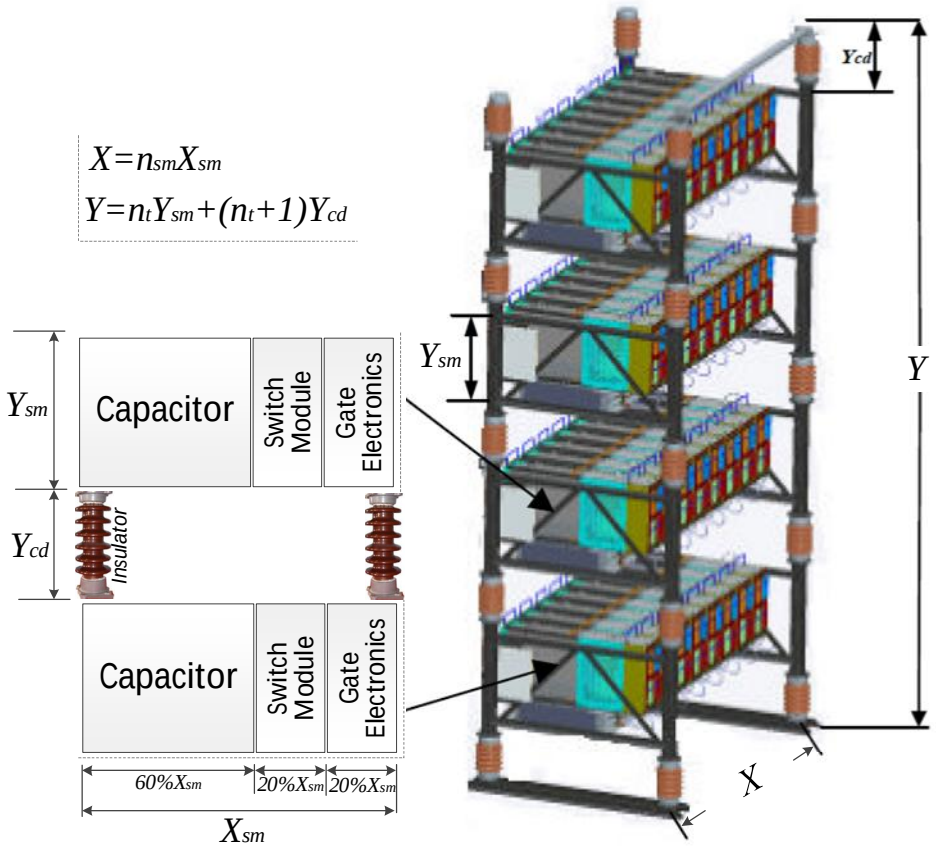


Fig. 2.12 MMCC footprint

In this section, MMCC footprint calculation is based on the height and width of the platform, as shown in Fig. 2.12. X is the total width of the platform which is according to the width of a SM, X_{sm}, and numbers per tier n_{sm}, while Y is the total height, which is based on the height of a SM, Y_{sm}, the insulation clearance gap distance between tiers Y_{cd} and the number of tiers n_t (n_t is limited by the local building height and set as fixed values of 6 or 7 for all cases here [77]).

Therefore, the footprint of MMCC can be calculated as

$$XY = [n_t Y_{sm} + (n_t + 1)Y_{cd}]n_{sm}X_{sm} \quad (2.8)$$

where $Y_{cd} = \text{USCD} * \text{voltage rating}/n_t$, USCD is the unified specific creepage distance and specified as 3.5cm/kV in IEC60185 Standard [78]. Y_{sm} is based on a Heat Sink, and has the largest size of 20cm, and X_{sm} is assumed to be three times of the height which equals to 60cm.

Cost: The overall cost is evaluated according to the prices of all components and numbers of them which are different according to the types of SMs and MMCC configurations;

Performance: Performance involves not only the number of switching states of different types of SMs to give the same voltage output (redundancy), but also the control complexity. The redundancy calculation is based on the submodule number and rectification and inversion switching state numbers, and the control complexity is based on the total number of arithmetic calculations required.

The selection of the key components for a MMCC application is based on an 11kV distribution system and is listed in Table 2.1. The switching devices and components selected and their costs are based on references from the Farnell website. The comparison of the two-level half bridge submodule (2L-Half Bridge), three-level cascaded H-bridge submodule (3L-HB) and five-level flying capacitor converter submodule (5L-FC) from the above aspects are shown in Table 2.2.

Table 2.1 Key components for MMCC submodule analysis

Component	*Manufactor Part No.*	*Rating*	*Cost (£)*	*Size*
IGBT Switch Module	Infineon IKW30N60TFKSA1	600V, 30A	7.5	20% of submodule*
Capacitor	EETED2G561EA (Panasonic)	400V, 560μF	10.54	Typical 50%-60% of submodule [79]
Gate Electronics	Actel ProASIC3 FPGA Board	Only key parts are considered	6.75	20% of submodule
	LEM LV 25-P Voltage Transducer		59.93	
	Gate drive & Isolation (ACPL-332J; MEV1S0515SC)		12.85	
Heat Sink	Fisher elektronics SK105/105SA	R_{th}=2K/W	6.58	-

* The submodule here is considered as a 2L-half bridge cell card.

Table 2.2 Comparison of different MMCC configurations

		SSBC		*SDBC*		*DSBC*	*DSCC*
		3L- HB	5L-FC	3L- HB	5L-FC	3L-HB	2L-Half Bridge
Footprint	SM Qty.	28	14	48	24	56	112
	Tiers No.(n_t)	7	7	6	6	7	7
	XY (m^2)	5.3	7.5	9.5	13.5	10.6	17.7
Cost (£)		4187.12	5429.48	7177.92	9307.68	8374.24	13104.0
Performance	Redundancy	112	392	192	672	224	224
	Control complexity	Cluster control		Cluster control		Top & Bottom arm cluster control	
		Submodule control		Submodule control		Submodule control	
		-		-		Common DC-link control	
		-		-		Circulating current control	

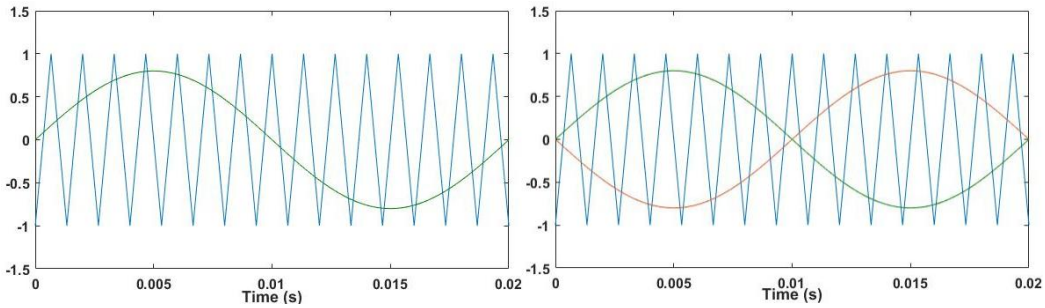
Table 2.2 summarizes the different metrics for variable MMCC configurations with different converter topologies as submodules. It can be concluded that the SSBC using 3-level H-bridge cells as SMs can provide the smallest footprint, lowest cost while 5-level FC cells provide more redundancy. For SDBC type, even though the control complexity is the same as SSBC, its footprint, and cost are all higher than SSBC regardless using 3-level H-bridge or 5-level flying capacitor as SMs because that $\sqrt{3}$ voltage output ratio for delta connection comparing with Y connection requires more SM numbers. The double star configurations are mainly for HVDC application. Not only do they occupy more space and cost more than the single star types, but also they provide less redundancy but higher control complexity, thus they are the least attractive for STATCOM and APF applications.

2.5 Multilevel Pulse Width Modulation Schemes

2.5.1 Basic sine-triangle PWM for full bridge converter

The Pulse Width Modulation (PWM) schemes are widely used for voltage source converters (VSC), for synthesising the desired waveforms in switch-mode operation [80]. The sine-triangle PWM control method compares the desired sinusoidal reference signal with a triangle carrier waveform at a frequency much higher than the reference signal as shown in Fig. 2.13(a) and (b). The intersections of these two signals determine the durations of the mark and space of the resultant switch control pulse signals. Two important parameters are used in this scheme; one is the amplitude modulation index $M_{a,}$ which is defined as the ratio of the reference signal magnitude over the carrier waveform magnitude. The other is the frequency modulation index M_f defined as the carrier frequency f_c over the reference signal frequency f_s which is commonly 50Hz.

The PWM algorithm may use one sinusoidal reference waveform, and is called bipolar PWM, as shown in Fig. 2.13(a). It may also use two reference waveforms which are 180° phase displaced and have the same magnitude, as shown in Figure 2.13(b) and this is the unipolar scheme.



(a) (b)

Fig. 2.13 (a) Bipolar PWM and (b) Unipolar PWM when M_a=0.8, M_f=15

Applying bipolar PWM to control the full bridge converter in Fig. 2.14(a), a pulse signal turns on both S_{1a} and S_{2b}, while S_{1b} and S_{2a} are off, a gap signal turns off S_{1a}

and S_{2b} and turn on S_{1b} and S_{2a}. The output AC voltage swings from $+V_{DC}$ to $-V_{DC}$ at the frequency of triangular carrier wave as shown in Fig. 2.14(b) upper figure. In contrast the unipolar PWM controls the left and right-hand-side (RHS) pairs of switches separately, hence it is more complicated. The pulse train determined by the sine wave with zero phase angle is applied to the left-hand-side (LHS) two switches which are complementary and that generated by its counterpart controls the RHS two complementary switches. The resultant AC terminal voltage waveform is as shown in Fig. 2.14(b) bottom figure.

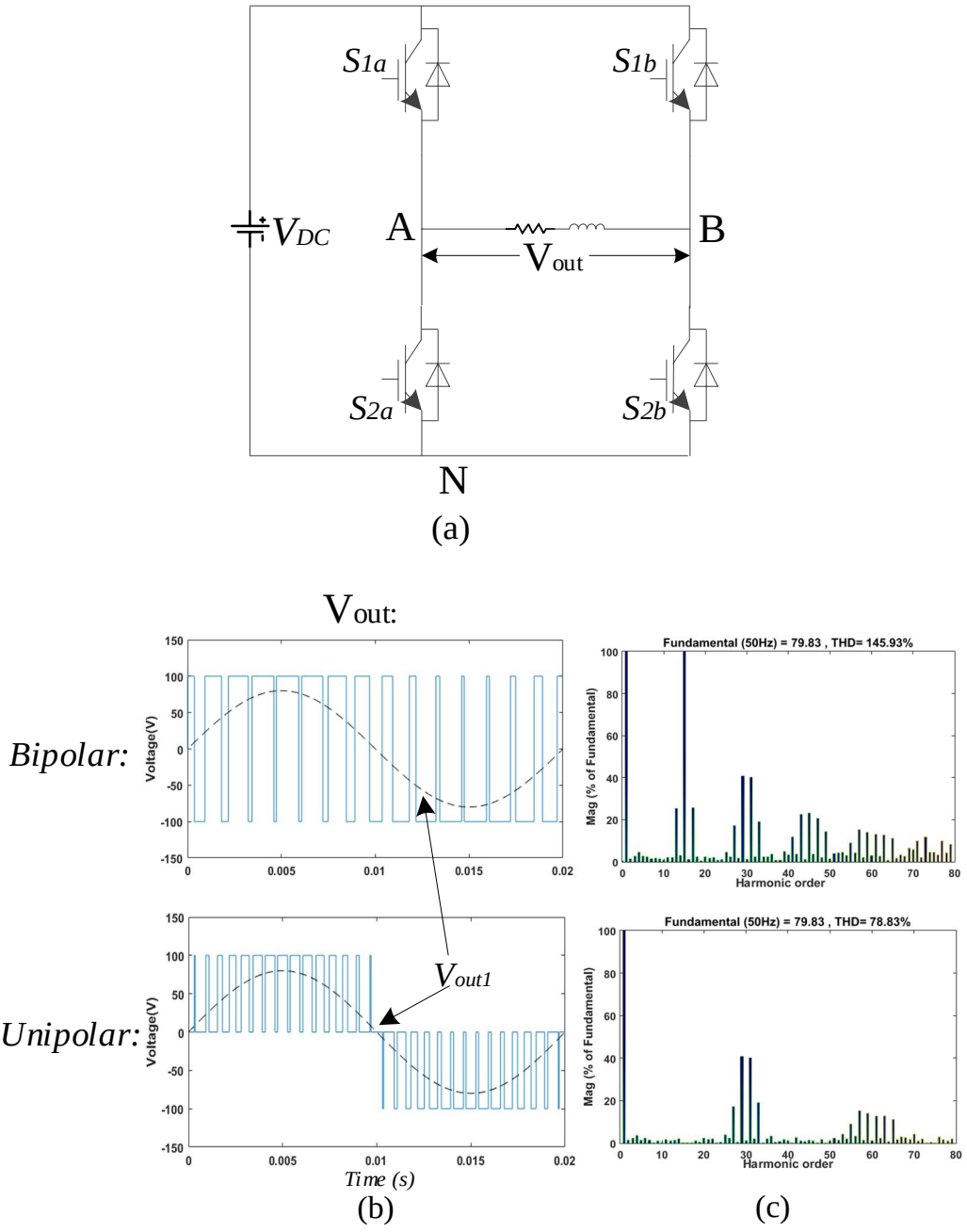


Fig. 2.14 Bipolar & Unipolar sine-triangle PWM applied to the full bridge converter and the corresponding AC terminal voltage waveform with their harmonic spectra

Comparing these two schemes the unipolar PWM scheme has clear advantages over its bipolar counterpart as seen in Fig. 2.14. The unipolar PWM results in the output

voltage waveform having much higher harmonic frequencies than that of bipolar scheme, even though the switches operate at the same frequency which is determined by the carrier wave. The spectra in Fig. 2.14(c) also show that the harmonics in the bipolar PWM output voltage appear centred around M_f and its multiples can be defined as

$$h = j(M_f) \pm k. \tag{2.9}$$

where h is the harmonics order in the output voltage waveform, both j and k are integers, and when j is an odd integer, k is even and vice versa.

In the unipolar PWM output voltage, the harmonics are moved to the neighbourhood of $2M_f$ and its multiples are re-defined as

$$h = j(2M_f) \pm k \tag{2.10}$$

where k is an odd integer.

Also the dominant components around M_f disappear, thus resulting in a significant reduction of harmonic content. Therefore, the unipolar PWM helps to reduce converter output voltage waveform harmonics effectively compared with its bipolar counterpart while switching frequencies are the same [81]. Hence, all the applications introduced in this thesis will adopt the unipolar PWM scheme. Its derivative multilevel PWM schemes, Phase Shifted-PWM and Phase Disposed-PWM, are analysed in detail in the following subsections for the control of modular multilevel cascaded converters.

2.5.2 Multilevel sine-triangle PWM schemes

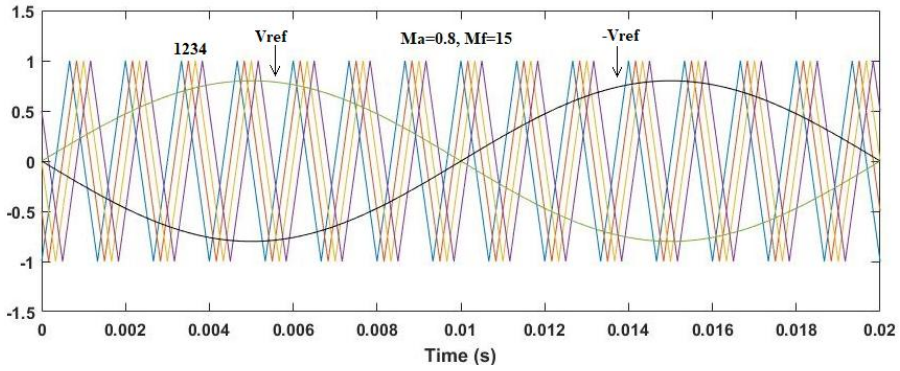
The sine-triangle PWM extension to more than two levels involves dividing the sine wave reference into distinct bands where the number of bands equals the number of complementary switch pairs in the inverter. The sinusoidal reference is then compared with each triangular carrier and the sum of the comparator signals form the voltage level command for the inverter.

There are in general two main types of carrier-based schemes; one relies using multiple carriers which encompass the whole sinusoidal reference signal range but are all out of phase from each other. This scheme is commonly referred to as Phase Shift (PS) multilevel PWM [82]. The other uses a strategy which disposes multiple carriers, which are all in phase, in contiguous bands and this is commonly referred to as Phase Disposition (PD) multilevel PWM [83]. This has been extended to include other disposed carrier placements, but in the work here only the basic PD and PS schemes are considered.

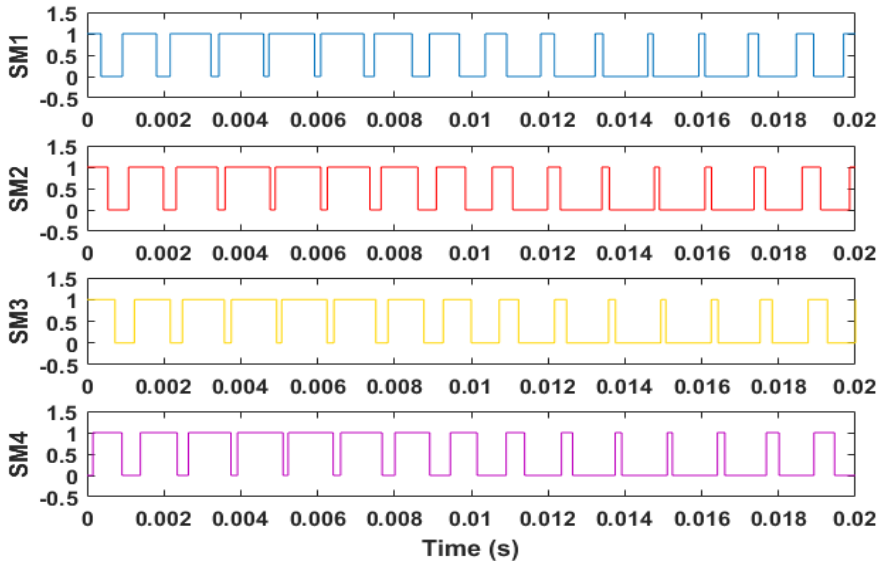
2.5.2.1 Phase Shift-PWM

The Phase Shift-PWM (PS-PWM) technique relies on having multiple triangle carrier waves which are phase shifted relative to each other. The number of carriers is the same as the output voltage wave distinct levels from 0 to peak minus 1. For example, a 5-level (0, $\pm 0.5V_{DC}$, $\pm V_{DC}$) output voltage waveform is generated by four H-bridge

submodules connected in series in one arm, so 4 triangle carriers are required, as shown in Fig. 2.15(a) and the corresponding generated pulse signals are shown in Fig. 2.15(b) while the controlled circuit is shown in Fig. 2.16. Each triangle carrier takes responsibility of controlling one SM: for the top first SM_1, carrier 1 (blue) compared with the reference voltage waveform V_{ref} generates pulse signals to control the complementary switches S_{1a}, S_{2a}, while it also compared with the reference counterpart $-V_{ref}$ to control S_{1b}, S_{2b}; the carrier 2 (red) compared with $\pm V_{ref}$ controls the SM_2 two complementary switch pairs S_{3a}, S_{4a} and S_{3b}, S_{4b}; the other two carriers 3 (yellow) and 4 (purple) thus control the SM_3 and SM_4 in the same order. The phase shift value between each individual triangle carrier is calculated as $\left(\frac{180^0}{N-1}\right)$, where N is the voltage levels from 0 to positive peak and is 5 in this case.



(a)



(b)

Fig. 2.15 (a) PS-PWM Four phase shift carriers with the reference waveforms for 5-level CHB-MMCC and (b) Corresponding generated pulse signals

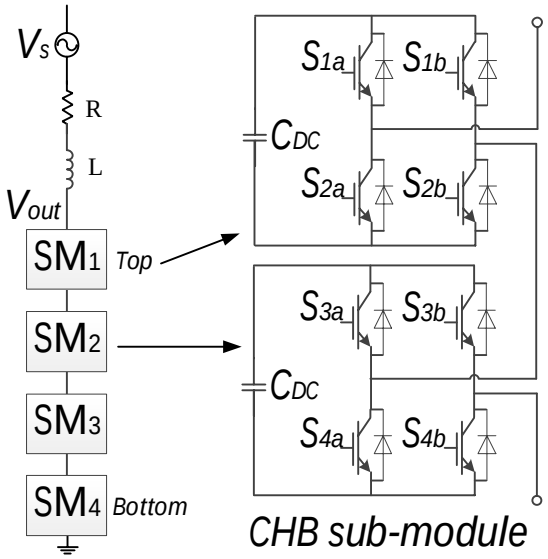


Fig. 2.16 One arm of a 5-level CHB-MMCC circuit

In PS-PWM, the lowest harmonic order equals the product of the number of carriers, the number of reference signals and M_f, which in the case of four carriers for four SMs it is $8M_f$. Other harmonics are at the sidebands around $8M_f$ and its multiples and they are all odd ones. Thus the harmonic orders h and their frequencies f_h are derived from Equation (2.10) and given as

$$h = j(8M_f) \pm k \tag{2.11}$$

$$f_h = \left(j(8M_f) \pm k\right) f_1 \tag{2.12}$$

where f_1 is the reference signal frequency;

j=1, 2, 3, 4, ….is the coefficient of modulation frequency;

k= 1, 3, 5, 7, ….is the odd number.

Clearly from the above, with higher switching frequency, M_f is higher and all harmonic frequencies are pushed higher, which is beneficial to the converter in terms of smaller filter size and lower cost, but at the expense of higher switching frequency hence higher losses. The advantage of MMCC is that it can have a higher number of SMs to obtain higher harmonic frequencies with lower switching frequency. A measure of the harmonics performance of the voltage waveforms is based on the Total Harmonics Distortion (THD) value. This is defined as the ratio of the root of the sum of all the harmonic components' amplitudes squared over the fundamental element amplitude. The formula for THD is given as

$$THD = \frac{\sqrt{V_2{}^2 + V_3{}^2 + \cdots}}{V_1} \tag{2.13}$$

The 5-level CHB-MMCC one arm circuit is shown in Fig. 2.16 above and in the corresponding simulation study of the MMCC is connected to a 3-phase AC source with V_s=160V, through a R-L filter with R=1Ω and L=1mH, hence the DC capacitor voltages are maintained at 100V for M_a=0.8. The output phase voltages and line voltages with their corresponding harmonics spectra for a carrier switching frequency

of 1 kHz are shown in Fig. 2.17. It can be observed that the 3rd order harmonic and its multiples are eliminated in the line voltage, so the value of k in Equation (2.11) becomes 1, 5, 7, 11… for line voltage harmonics order and frequency calculation.

Switching Frequency = 1 kHz. $M_f = 20$, first side bands appear at:

$$f_{159} = (8 \times 20 - 1) \times 50 = 7950\ Hz,\ f_{161} = (8 \times 20 + 1) \times 50 = 8050\ Hz$$

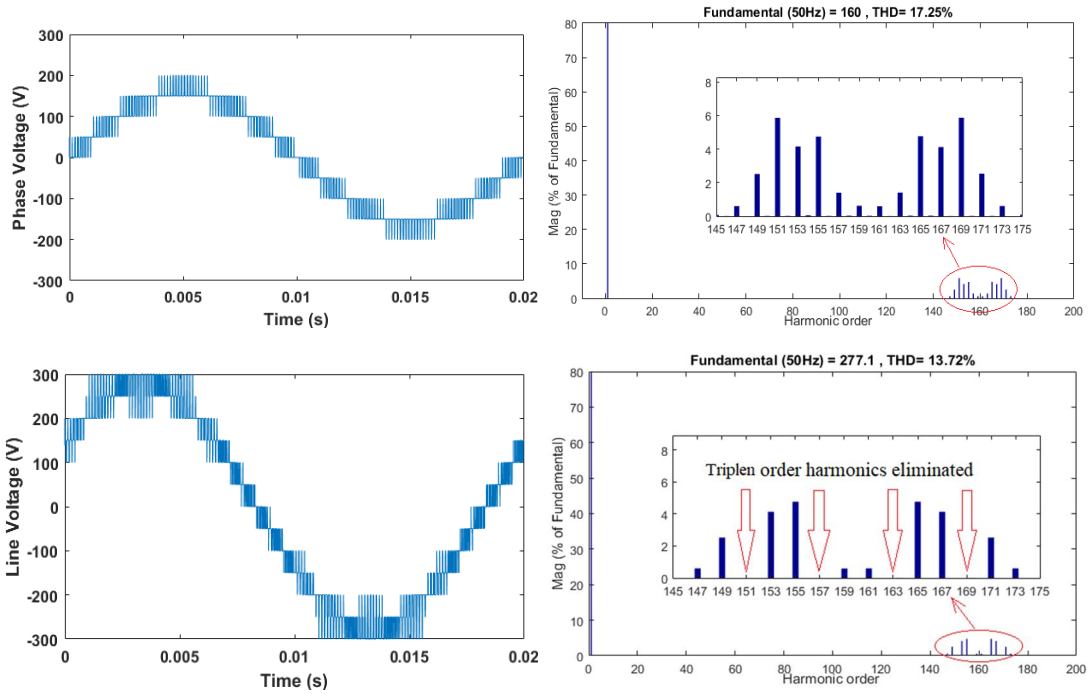


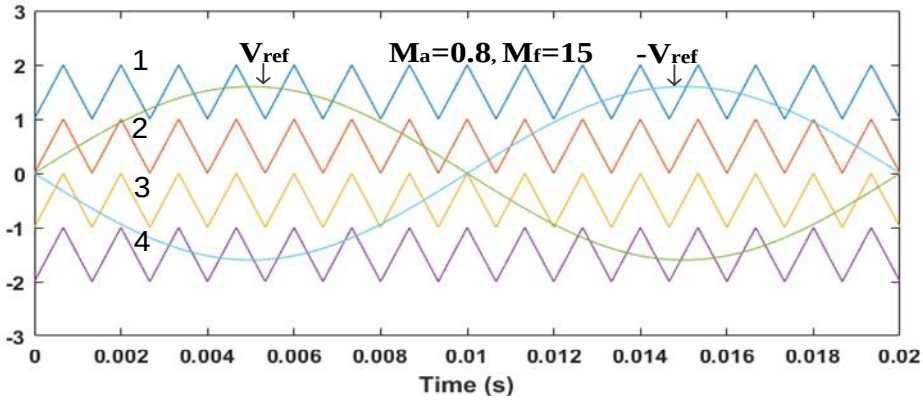
Fig. 2.17 5-level MMCC output phase voltage (upper) and line voltage (bottom) with their harmonics spectra for PS-PWM when f_c=1 kHz

From the above result, it is clear that either phase voltage or line voltage of the MMCC has reduced THD significantly, since the PS-PWM for MMCC pushes the switching harmonics into the higher frequency band and brings benefits of reducing filtering requirements. Hence f_c=1kHz is enough for all the 5-level MMCC applications.

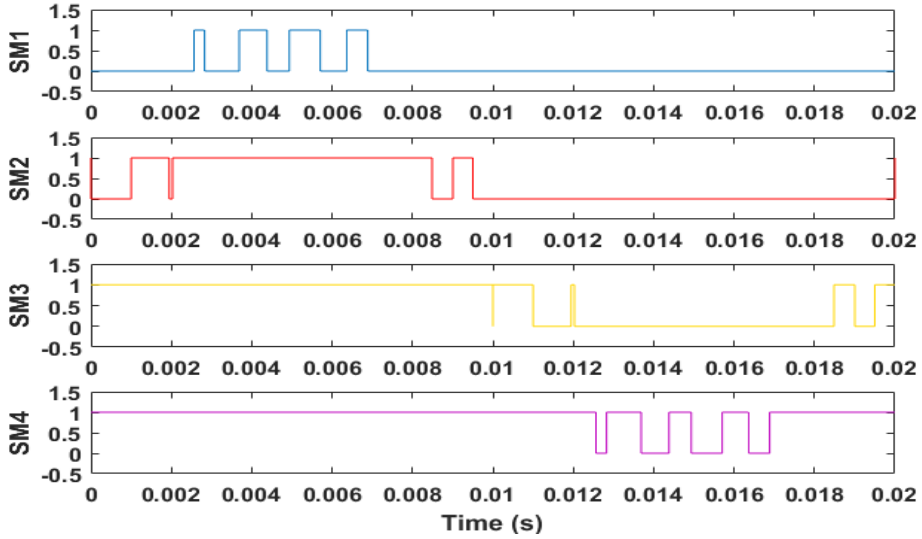
2.5.2.2 Phase Disposed-PWM

Besides PS-PWM, the Phase Disposed-PWM (PD-PWM) has also been applied for 5-level CHB-MMCC (shown in Fig. 2.16), which still relies on 4 triangular wave carriers but all in phase with disposition in contiguous bands instead of phase shifting, as shown in Fig. 2.18(a). Similarly with the PS-PWM scheme, each triangle carrier takes responsibility for controlling one submodule and the corresponding pulse waveforms are shown in Fig. 2.18(b): carrier 1 (blue) compared with converter reference voltage waveform V_{ref} generates pulse signals to control the SM1 complementary switches S_{1a}, S_{2a}, while it also compared with the reference counterpart $-V_{ref}$ to control the other leg S_{1b}, S_{2b}; the carrier 2 (red) compared with $\pm V_{ref}$ controls the SM2 two complementary switch pairs S_{3a}, S_{4a} and S_{3b}, S_{4b}; Carriers 3 (yellow) and 4 (purple) control the other two submodules in the same order. However, one significant difference of this scheme from the PS-PWM is that, from the pulses figure, it can be found that the top and bottom signals' switching frequency

are higher than the middle two, which means the 4 SMs switch unequally causing unequal utilization and losses.



(a)



(b)

Fig. 2.18 Four phase disposed carriers for 5-level CHB-MMCC

In the Fig. 2.18, all the triangle carriers are in the same phase and so, the equation for the phase voltage harmonic orders and the corresponding frequency calculation are the same with the basic sine-triangle unipolar PWM expression, while the *k* value for the line voltage are still 1, 5, 7… because of the 3rd harmonics elimination. Thus, Equations (2.11) and (2.12) become

$$h = j(2M_f) \pm k \tag{2.14}$$

$$f_h = \left(j\left(2M_f\right) \pm k\right)f_1 \tag{2.15}$$

where

f_1 is the reference signal frequency

j=1, 2, 3, 4, ….is the coefficient of modulation frequency;

k= 1, 3, 5, 7.... is the odd number;

When switching frequency = 1 kHz, $M_f = 20$, first side bands appear at:

$f_{39} = (2 \times 20 - 1) \times 50 = 1950\,Hz$, $f_{41} = (2 \times 20 + 1) \times 50 = 2050\,Hz$

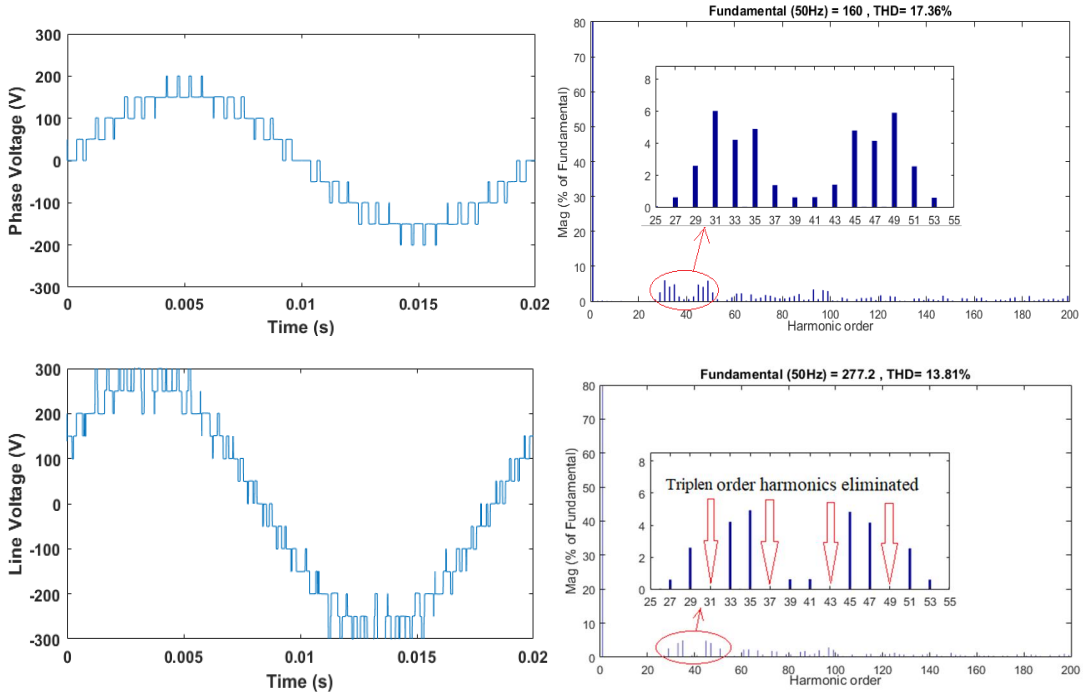


Fig. 2.19 5-level MMCC output phase voltage (upper) and line voltage (bottom) with their harmonics spectra for PD-PWM when f_s=1 kHz

A comparison of the voltage harmonics spectra of the MMCC with PS and PD-PWM is shown in Table 2.3. It can be concluded that the output voltage with PD-PWM has a lower total frequency modulation ratio and hence harmonics order side bands for equivalent carrier switching frequency compared with PS-PWM, which results in the increasing of voltage THDs and as well as the filter requirement. Therefore, PS-PWM has a better harmonics distortion performance than PD-PWM in MMCC applications.

Table 2.3 Comparison of the THDs of 5-level CHB-MMCC output voltage with PS and PD-PWM

	Total Frequency modulation ratio $\sum M_f$		THD of output phase voltage (%)		THD of output line voltage (%)	
	PS-PWM	PD-PWM	PS-PWM	PD-PWM	PS-PWM	PD-PWM
f_s= 1000 Hz	160	40	17.25	17.36	13.72	13.81

2.6 Summary

This chapter presented a review of the principles of Modular Multilevel Cascaded Converters from its submodule topologies and varied configuration aspect; the submodule topologies introduced in this chapter are the 2-level half bridge converter, 3-level H-bridge converter and 5-level flying capacitor converter, with the operating quadrants and switching states comparisons to highlight the degrees of freedom and comprehensive switching states. The MMCC configurations analysed are generally classified as single star or delta bridge cells and double star cells, while the double star can be applied with all the submodules above but the single star type can be applied only with 3-level H-bridge and 5-level flying capacitor submodules, since the half bridge submodule generates unipolar output voltage. An evaluation of the various MMCC configurations with different submodule topologies is presented based on their footprint, cost and performance (redundancy and control complexity). It has been concluded that the SSBC is the best choice for STATCOM application because it has the smallest size, least cost and simplest control complexity. However, a more detailed comparison of SSBC and SDBC applications under unbalanced conditions will be presented in the Chapter 4. Furthermore, the Phase Shift-PWM and Phase Disposed-PWM multilevel pulse width modulation schemes are introduced in this chapter. A comparison of harmonics band and THDs for the same switching frequency using these two schemes was also presented and it has been shown that PS-PWM has the potential to outperform PD-PWM in MMCC applications.

Chapter 3 Active Power Conditioner using MMFCC under Balanced Load Conditions

3.1 Introduction

This chapter presents the development of a FCC-based MMCC to function as a STATCOM which not only compensates the reactive power but also eliminates harmonic currents flowing in the power distribution lines. Harmonic current flowing in the utility network severely affects the quality of supplied power. Key contributors to its presence in distribution networks are the nonlinear single-phase and three-phase loads connected on the lines. These are either identifiable or unidentifiable harmonic loads. The identifiable ones are often those industrial loads drawing large current such as phase-controlled three-phase rectifiers and variable speed drives. When the network current is polluted by these loads, the source of pollutant can be traced and hence adequate suppression measures can be applied. The unidentifiable ones are often low power single-phase nonlinear domestic loads. Individually they draw very low harmonic currents but collectively harmonic currents accumulate to reach a significant level. Eliminating all these harmonics can be a challenge to a STATCOM. The key issues are extracting the harmonic elements in the load current accurately and eliminating them to a low residual level. With a MMCC-based-STATCOM there are also the challenges of balancing module capacitor voltages since the harmonic currents vary constantly.

This chapter will analyse the levels and contents of harmonic currents drawn by a selection of typical unidentifiable as well as identifiable loads found in domestic and commercial settings. The results of this analysis will assist the effective harmonic extraction and hence the compensation. A harmonic extraction technique is presented which uses a low-pass filter. With this technique an MMFCC-based Active Power Conditioner will then be developed to suppress the harmonic currents and compensate reactive power in a simulated small distribution system. The control strategy including harmonic and reactive current elimination scheme will be described. A voltage control scheme will be developed for balancing the submodule intra-cluster capacitor voltages under distorted load current.

3.2 Study of Harmonic-Generating Loads

The harmonic-generating loads which draw nonlinear currents from the grid have long existed in many forms in both industrial and domestic environments. A selection of such common devices and appliances were investigated to illustrate the levels of harmonic current caused by modern-day loads.

3.2.1 Unidentifiable harmonic loads

3.2.1.1 Single-phase diode rectifier

A load is considered nonlinear when its impedance changes with the applied voltage [84]. The changing impedance means that the current drawn by this load is non-sinusoidal even when it is connected to a sinusoidal AC voltage source. A conventional single-phase diode rectifier with DC output capacitor filter is shown in Fig. 3.1, and exemplifies a typical non-linear load. The AC current I_s drawn from the voltage source driving this circuit is shown in Fig. 3.2(a). Due to the charging action of the capacitor, the AC source current is very pulsatory and results in a significant Total Harmonic Distortion (THD), which is 94.81% as shown in Fig. 3.2(b). These harmonics components only appear in the odd orders, while their magnitudes decrease with frequency. Therefore, the 3rd, 5th and 7th harmonics are dominant in the source current and this phenomenon also exists in practical distribution systems because many appliances require a DC power supply and thus contain rectifiers connected to the AC distribution line.

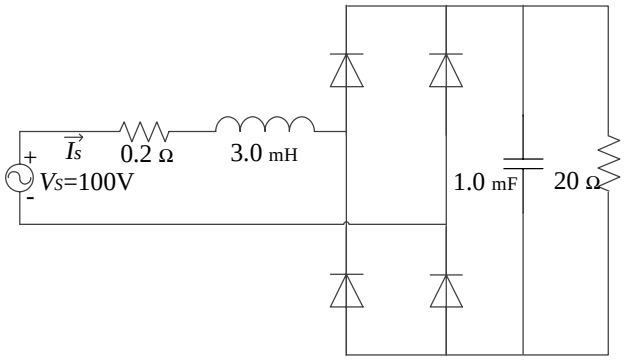
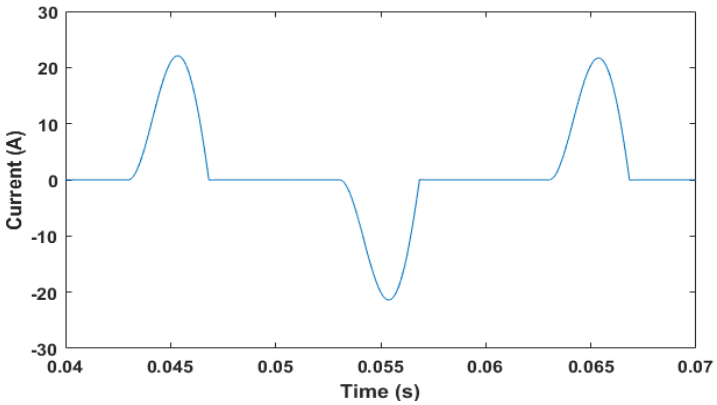
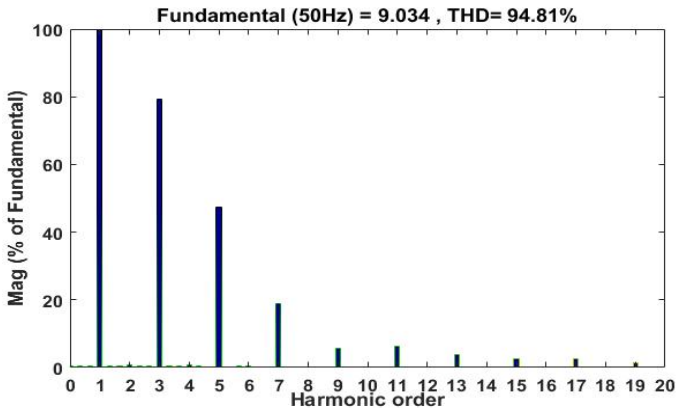


Fig. 3.1 Single-phase diode rectifier with output filter



(a)



(b)

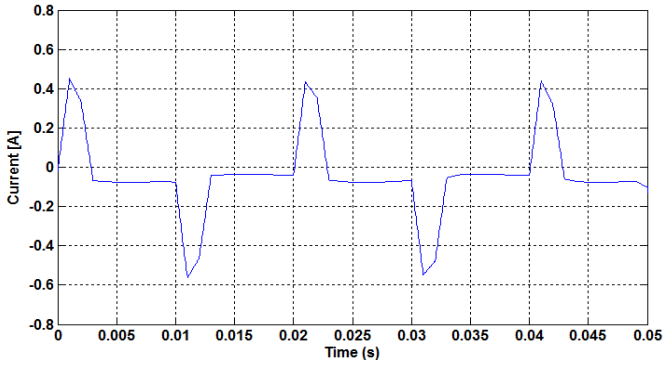
Fig. 3.2 (a) AC current waveform and its (b) harmonics spectrum

3.2.1.2 Domestic harmonic loads

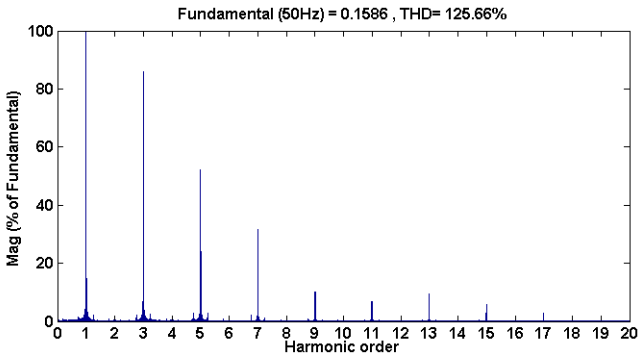
This subsection gives several examples of common domestic low-power appliances which draw non-sinusoidal currents from a distribution line. In practical situations, many such appliances may be connected to the line simultaneously, thus drawing excessive magnitudes of low-order harmonic current components and affecting the power system.

LCD Monitor:

The steady-state current waveform of a typical computer LCD monitor with Switched-mode power supply (SMPS) is shown in Fig. 3.3(a) while its harmonic spectrum is shown in Fig. 3.3(b). The highly distorted current waveform has similar characteristicsto the previous single-phase rectifier result; its 3rd order harmonics magnitude is as high as 80% of the fundamental component and accordingly, the THD value is 125.66%. This piece of equipment reflects a good example of distorted current drawn by common domestic appliances. A single such device may only draw 0.12A 3rd order harmonics current from the system; however, large commercial or institutional installations such as university computer clusters may contain many hundreds of similar equipment items and the cumulative effects of the 3rd order harmonics will become more critical.



(a)

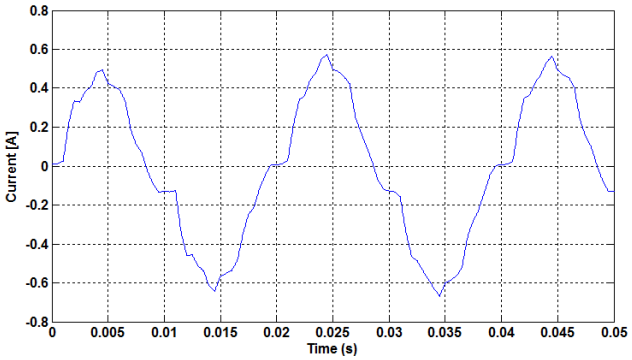


(b)

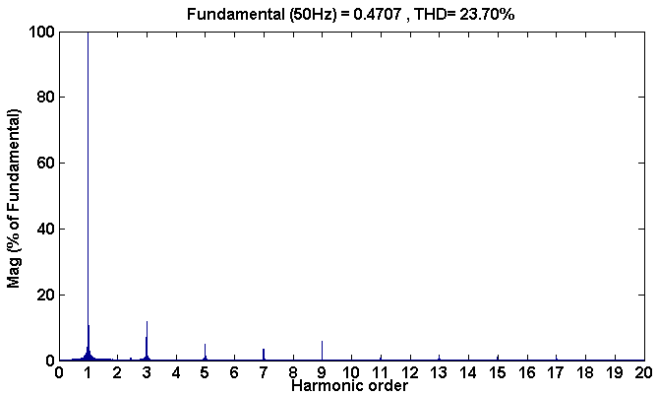
Fig. 3.3 (a) LCD monitor steady-state current waveform and (b) its harmonic spectrum

Desktop PC:

Fig. 3.4(a) shows the steady-state current waveform of a typical desktop personal computer (PC) with an SMPS connecting with an Active Power Factor Correction (PFC) circuit. The latter normally consists of a boost converter, whose main function is to control the input AC current to be close to sinusoidal instead of a sharply pulsed waveform like the previous result, and keep the output DC voltage constant [85, 86], thus a bulky passive filter can be eliminated. Consequently, the drawn current harmonic spectrum is as shown in Fig. 3.4(b) while its THD is reduced to a relatively low value of 23.7%.



(a)



(b)

Fig. 3.4 (a) Desktop PC steady-state current waveform and (b) its harmonic spectrum

3.2.2 Thyristor controlled rectifier load

3.2.2.1 Single-phase controlled rectifier

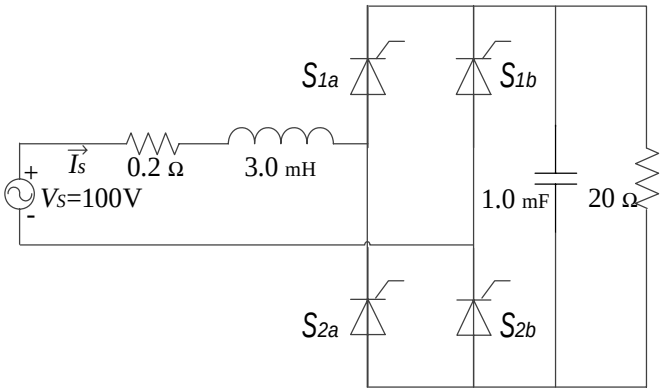
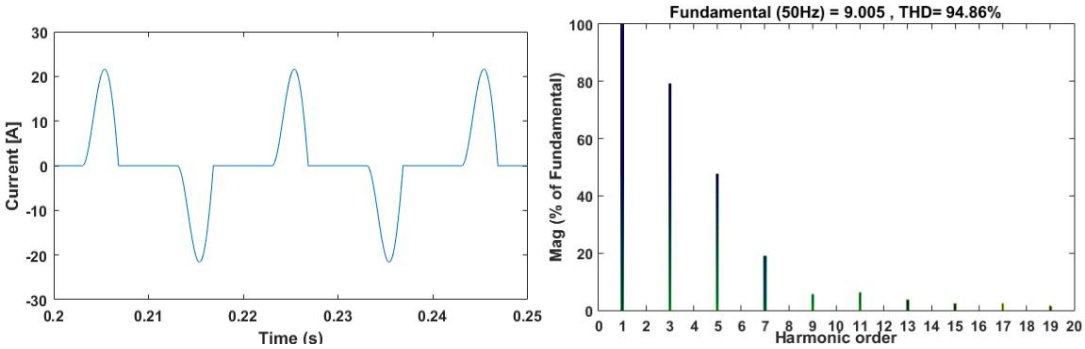
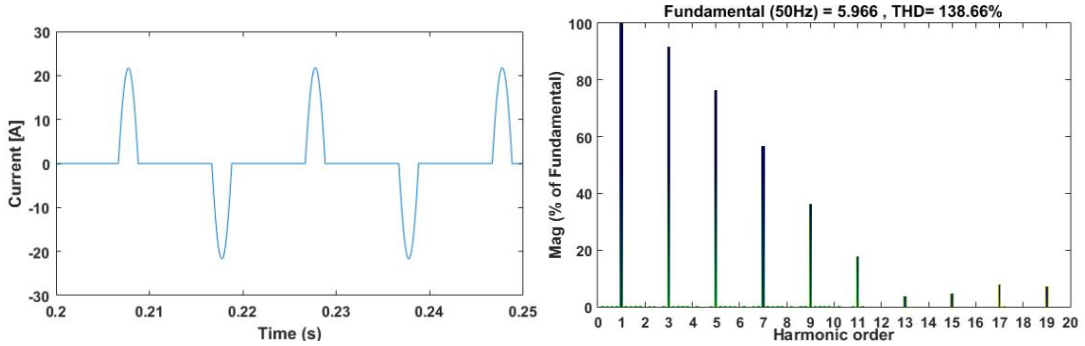


Fig. 3.5 Single-phase thyristor controlled rectifier circuit

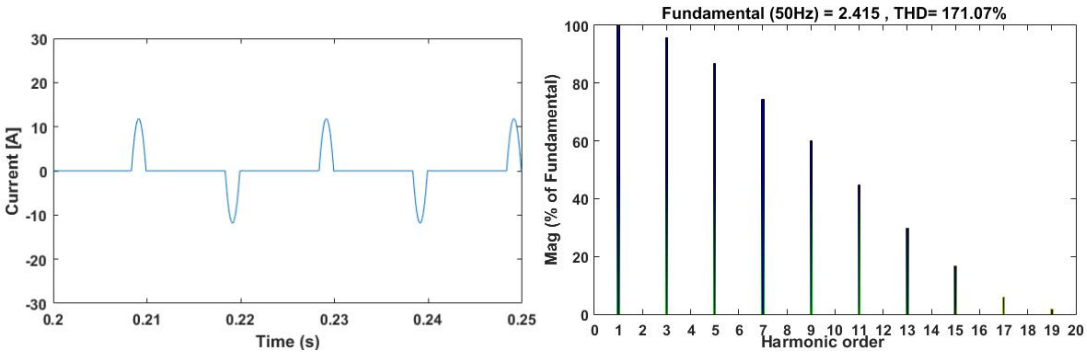
The configuration of a single-phase thyristor controlled rectifier is shown in Fig. 3.5. The difference between this circuit and the diode rectifier is that the 4 uncontrollable diodes are replaced by controllable thyristors, thus the DC output can be adjustable. This is widely used for loads requiring variable output such as DC motor drives and electric heaters. As the firing angle α of the switching signals changes from 0° to 150°, the AC current I_S waveforms and corresponding THDs are shown in Fig. 3.6 and Table 3.1 respectively.



(a) α=0°



(b) α=120°



(c) α=150°

Fig. 3.6 AC current waveform and its harmonics spectrum when (a) α=0°; (b) α=120°; (c) α=150°

Table 3.1 The AC currents for the single-phase thyristor controlled rectifier

Firing angle α	0°	120°	150°
50Hz	9.0	5.97	2.42
150Hz	7.13 (79.2%)	5.47 (91.6%)	2.31 (95.5%)
250Hz	4.28 (47.6%)	4.55 (76.2%)	2.09 (86.4%)
350Hz	1.70 (18.9%)	3.38 (56.6%)	1.80 (74.4%)
450Hz	0.51 (5.7%)	2.15 (36.0%)	1.45 (59.9%)
550Hz	0.57 (6.3%)	1.06 (17.8%)	1.08 (44.6%)

(Unit: Ampere)

As shown in the above figure and table, as the firing angle increases, the 50Hz fundamental current magnitude decreases from 9A to 2.42A. However, the AC current THD increases from 94.86% to 171.07%, and the percentages of the 3rd, 5th, 7th, 9th and 11th harmonics magnitude over the fundamental component magnitude also increase respectively.

3.2.2.2 Three-phase controlled rectifier

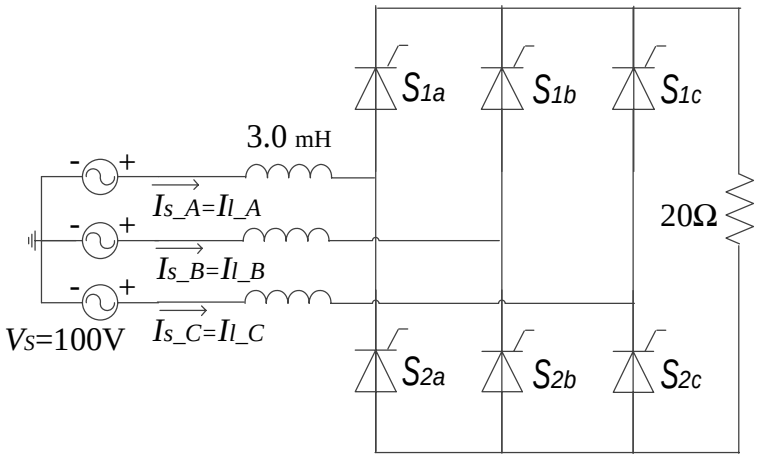
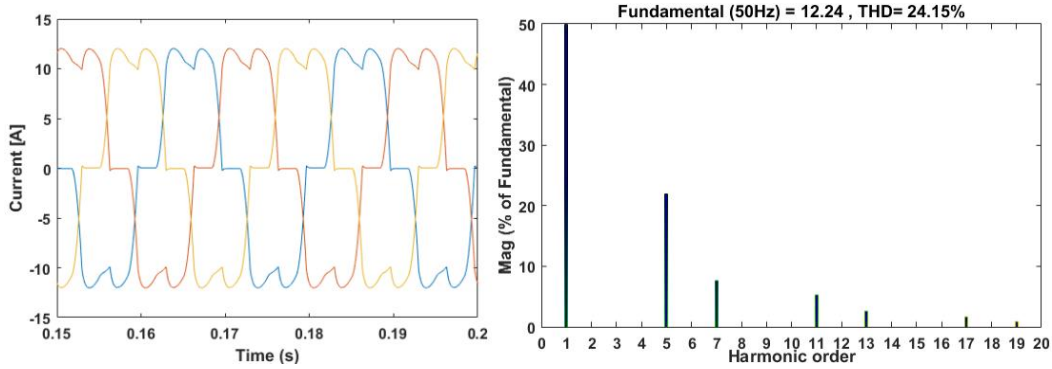
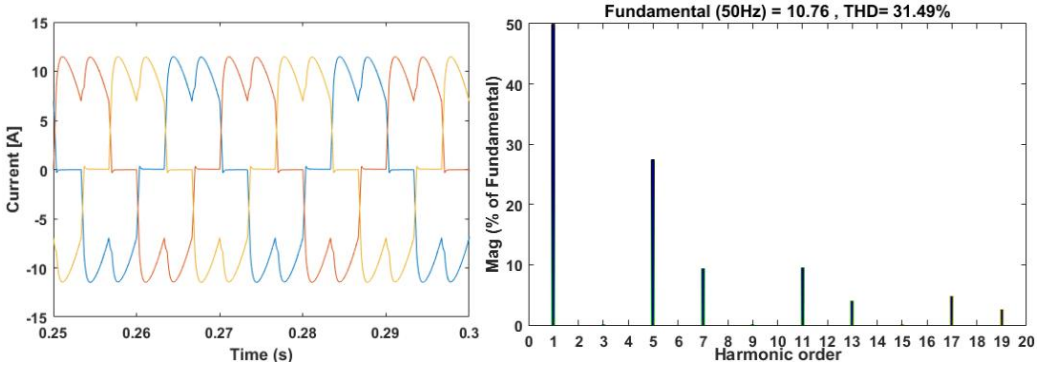


Fig. 3.7 3-phase thyristor controlled rectifier circuit

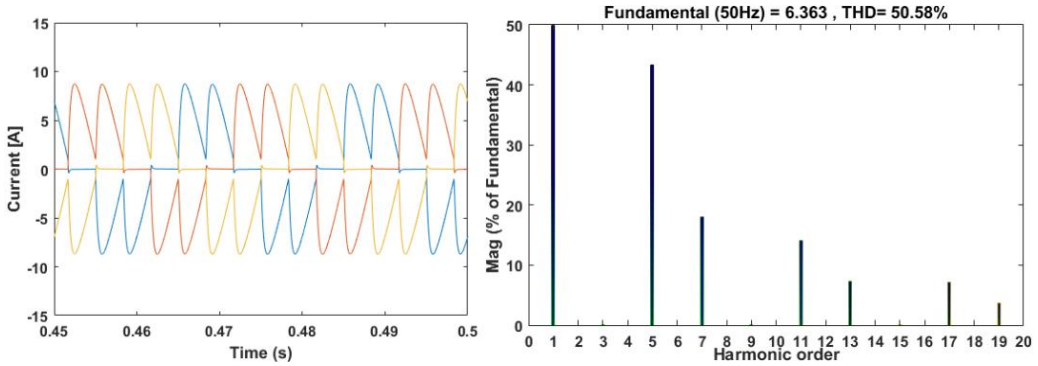
A 3-phase thyristor controlled rectifier circuit is shown in Fig. 3.7. The voltage source V_s has an RMS value of 100V at 50Hz and the load on the DC side is set as a 20Ω resistor. The study has been carried out with the firing angle α changing from 0° to 60°, as shown in Fig. 3.8.



(a)α=0°



(b)α=30°



(c)α=60°

Fig. 3.8 AC current waveform and its harmonic spectrum when (a) α=0°; (b) α=30°; (c) α=60°

Table 3.2 The AC currents for the 3- phase thyristor controlled rectifier

Firing angle α	0°	30°	60°
50Hz	12.24	10.76	6.36
250Hz	2.69 (21.9%)	2.95 (27.4%)	2.75 (43.25%)
350Hz	0.94 (7.7%)	1.0 (9.3%)	1.15 (18.0%)
550Hz	0.65 (5.3%)	1.03 (9.5%)	0.90 (14.1%)
650Hz	0.32 (2.6%)	0.44 (4.1%)	0.47 (7.3%)

(Unit: Ampere)

The current waveforms shown in Fig. 3.8 (a)-(c) and figures listed in Table 3.2 show the results of the 3-phase AC current when the firing angle changes from 0° to 60°. In Fig. 3.8(a), it can be seen that the current contains considerable harmonic components when α=0° and its THD is 24.15% with the 5th order harmonic most significant. The current distortion becomes worse when α=30° with THD = 31.49% and waveforms shown in Fig. 3.8(b). The worst case happens when α=60° and THD=50.58%. In Table 3.2, the fundamental current magnitude decreases from 12.24A to 6.36A, while the percentages of the 5th, 7th, 11th and 13th harmonic components increase especially for the 5th harmonic, its percentage to the fundamental reaches 43.24% at α=60° which is the highest. The 3rd harmonic and its multiples in the three phase currents are absent in this case, as they are cancelled between phases in a balanced three-phase system.

3.3 Harmonic Current Extraction

To eliminate load current harmonics as analysed above by using a STATCOM-based Active Power Conditioner (APC), one of the key issues is to extract the dominant harmonic elements from the measured load current accurately. There are two categories of harmonic extraction techniques: time-domain and frequency-domain. The latter is based on Fourier analysis to extract the required harmonics elements, which is effective but computationally intensive to the processor. Therefore, this scheme is rare to be implemented while the time-domain extraction technique is more popular [87].

3.3.1 Existing extraction techniques

Instantaneous reactive power theory-based schemes

The most widely-adopted time-domain extraction technique is based on the instantaneous reactive power theory, proposed by Akagi [88]. By using this scheme, the grid voltage and current are firstly transforming into α-β stationary components hence the corresponding real and reactive instantaneous power can be defined as

$$p = v_\alpha i_\alpha + v_\beta i_\beta$$
$$q = v_\alpha i_\beta + v_\beta i_\alpha \quad (3.1)$$

Consequently, the compensating current can be expressed as

$$\begin{bmatrix} i_{c\alpha} \\ i_{c\beta} \end{bmatrix} = \begin{bmatrix} v_\alpha & v_\beta \\ -v_\beta & v_\alpha \end{bmatrix}^{-1} \times \begin{bmatrix} \tilde{p} \\ q \end{bmatrix} \tag{3.2}$$

where $\tilde{p}$ is the AC component of the instantaneous active power. The harmonic current reference thus may be calculated. However, it can be seen from above equations that the instantaneous power calculation is dependent on a harmonic-free voltage, which means this scheme is not suitable for distorted and unbalanced voltage conditions.

Cross vector theory-based scheme

The cross vector theory defines the instantaneous real power and three instantaneous imaginary powers [89][90]. Consequently, instantaneous reactive power can be expressed in the *abc* frame as

$$q = v \times i = \begin{bmatrix} q_a \\ q_b \\ q_c \end{bmatrix} = \left(\begin{vmatrix} v_b & v_c \\ i_b & i_c \end{vmatrix} \begin{vmatrix} v_c & v_a \\ i_c & i_a \end{vmatrix} \begin{vmatrix} v_a & v_b \\ i_a & i_b \end{vmatrix} \right)^t \tag{3.3}$$

while it can be defined in the *α-β-0* frame as

$$\begin{bmatrix} p \\ q_0 \\ q_\alpha \\ q_\beta \end{bmatrix} = \begin{bmatrix} v_0 & v_\alpha & v_\beta \\ 0 & -v_\beta & v_\alpha \\ v_\beta & 0 & -v_0 \\ -v_\alpha & v_0 & 0 \end{bmatrix} \begin{bmatrix} i_0 \\ i_\alpha \\ i_\beta \end{bmatrix} \tag{3.4}$$

Assuming the neural is isolated, the voltages are balanced, so the extraction current can be expressed as

$$\begin{aligned} i_{ca} &= i_{La} - \frac{v_a * p}{(v_a^2 + v_b^2 + v_c^2)} \\ i_{cb} &= i_{Lb} - \frac{v_b * p}{(v_a^2 + v_b^2 + v_c^2)} \\ i_{cc} &= i_{Lc} - \frac{v_c * p}{(v_a^2 + v_b^2 + v_c^2)} \end{aligned} \tag{3.5}$$

where i_{La}, i_{Lb}, i_{Lc} are the load currents and i_{ca}, i_{cb}, i_{cc} are the compensating currents.

Moving average process scheme

This scheme is based on the synchronise reference frame (SRF) [91]. It is assumed that the harmonic load is balanced and even harmonics are not presented [92]. After transformed into *dq* frame, the odd order harmonics become multiples of 6, hence they all have a zero average value over 1/6 of the fundamental period. The filters are substituted by blocks that calculate the moving average

$$Moving_{average\_i_d} = \frac{6}{T} \int_{t-\frac{T}{6}}^{t} i_d dt \tag{3.6}$$

Adaptive interference cancelling scheme

This scheme has the ability of adaptive and hence keeps the system always in the best operating state [93]. The AC source voltage and load current fundamental elements are mutually correlated, while the voltage acts as reference input and the load current

as primary input, hence the harmonic signals can be extracted by subtracting the fundamental components.

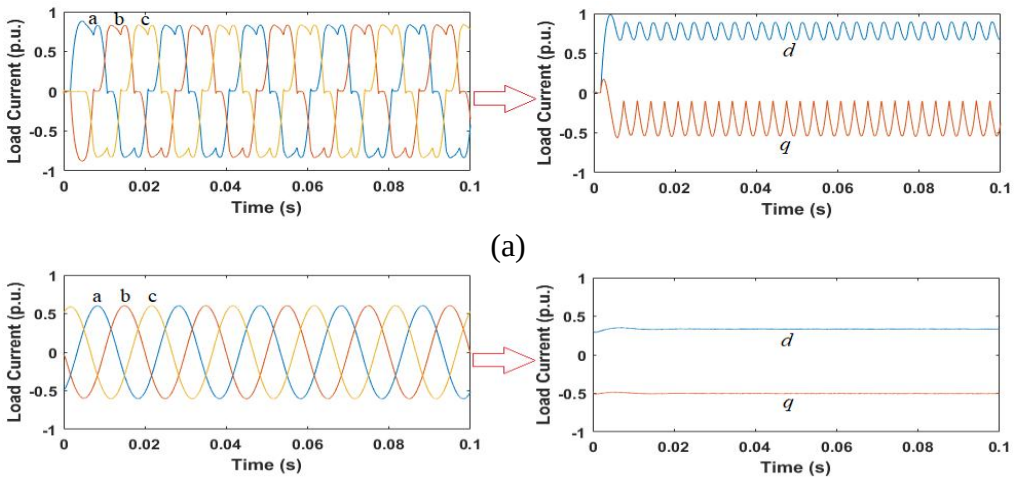
3.3.2 Low-pass filter-based extraction technique

The above extraction techniques have their own drawbacks such as requiring of AC source voltages feedback or complicated to implement. An alternative approach is realised by applying a low-pass filter-based harmonic current extraction scheme using the synchronise reference frame (SRF). It does not require any information from the grid voltage hence the harmonics voltage cannot affect the extracting performance. This scheme is based on transforming the distorted current waveforms using a *dq* SRF frame and applying a low-pass filter (LPF) for stopping all harmonics in the current vector. Transformation of the measured three-phase currents I_{l_a}, I_{l_b} and I_{l_c} requires knowing the angular position of the rotating reference frame which can be identified using the synchronous reference frame phase locking loop (SRF-PLL) technique introduced in the Chapter 1 [64, 94].

Once the phase angle θ of the grid reference voltage vector is identified using SRF-PLL, the measured three-phase load current I_{l_a}, I_{l_b} and I_{l_c}, forming a vector in the *abc* stationary reference frame, can be transformed to its equivalent *dq* elements in the reference frame rotating synchronously with the grid voltage frequency using the Park transformation matrix as follows:

$$\begin{bmatrix} I_{l\_d} \\ I_{l\_q} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \sin(\theta + \varphi_i) & \sin(\theta - \frac{2\pi}{3} + \varphi_i) & \sin(\theta + \frac{2\pi}{3} + \varphi_i) \\ \cos(\theta + \varphi_i) & \cos(\theta - \frac{2\pi}{3} + \varphi_i) & \cos(\theta + \frac{2\pi}{3} + \varphi_i) \end{bmatrix} \begin{bmatrix} I_{l\_a} \\ I_{l\_b} \\ I_{l\_c} \end{bmatrix} \quad (3.7)$$

where φ_i is the phase angle between the load current and reference voltage vectors. Note that through the above transformation, I_{l_d} and I_{l_q}, in general, contain a set of (h–1) order harmonics where h is the order of harmonics present in I_{l_a}, I_{l_b} and I_{l_c}, as shown in Fig. 3.9(a), the 50 Hz fundamental frequency waveforms are transformed into DC forms while the harmonics of 3rd order and above with frequencies of 150Hz and above are thus transformed into 2nd order harmonics at 100Hz and above.



(a)

(b)

Fig. 3.9 Thyristor controlled rectifier load current from *abc* to *dq* transformation waveforms

It is desirable that I_{l_d} and I_{l_q} only contain DC components, implying that I_{l_a}, I_{l_b} and I_{l_c} only contain the grid fundamental frequency ω, as shown in Fig. 3.9(b). Therefore, two low-pass filters (LPF) are applied to stop the harmonic components, as shown by block diagram in Fig. 3.10. The transfer function of a LPF is given as

$$T(s)_{LPF} = \frac{\omega_0}{s+\omega_0} \tag{3.8}$$

where ω_0 defines the cut-off frequency. Hence all the harmonics with frequencies equal or higher than ω_0 will be attenuated and those lower than ω_0, ideally will pass through the filter. For example, the magnitudes of the 2nd order harmonic in I_{l_dq}, corresponding to the 3rd order harmonic in I_{l_abc}, and above would be attenuated, with $\omega_0 \leq 2\pi \times 100$ rad/s. It needs to be mentioned that the 3rd order harmonic in the thyristor controlled rectifier load is absent when load current is balanced, but will start to appear in an unbalanced case; this will be analysed in the next chapter.

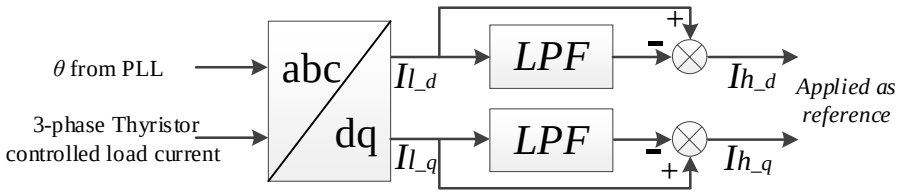


Fig. 3.10 LPF current harmonics extraction block diagram

Subsequently the filtered current elements can be subtracted respectively from their original input current elements I_{l_d} and I_{l_q}, hence leading to the resultant two current elements containing only the harmonics. These can be used as the references for an APC current controller, as shown in Fig. 3.10.

To verify the accuracy of this technique, one can simply subtract the above extracted currents directly from the original measured nonlinear load current without involving a voltage source inverter. The resultant current waveforms are as shown in Fig. 3.11, with thyristor firing angle α set to 0° initially and being changed to 30° at 0.7sec and then to 60° at 0.8sec. As can be seen, the resultant filtered current waveforms are virtually sinusoidal, with their THDs for all α angles maintained below 2%.

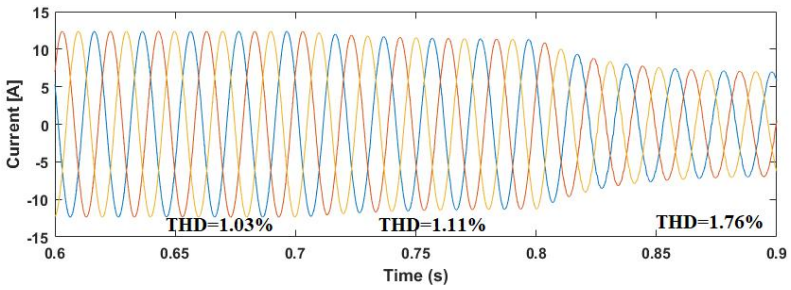


Fig. 3.11 LPF filtered result for 3-phase harmonics current

Clearly this scheme is effective in extracting current harmonics with frequencies higher than the fundamental from any measured load currents. It is used for the MMFCC-APC control scheme as presented in the following.

3.4 Control of a MMFCC-based APC

3.4.1 Configuration of the load network and the MMFCC-APC

To develop control strategies suitable for a Modular Multilevel Flying Capacitor Converter to function as an Active Power Conditioner, a particular load network for an MMFCC-APC is proposed as shown in Fig. 3.12. This has been designed specifically to emulate the impacts of nonlinear loads which draw harmonic currents from the grid source, such as 3-phase thyristor rectifier loads combined with normal inductive loads. Both of these loads are connected in parallel on Bus 2 as illustrated in Fig. 3.12 depicting a more practical case where a distribution system may consist of various types of load. To address the load harmonics issues, the MMFCC-APC is designed to improve the waveform quality of the current drawn from the incoming feeder which is represented by V_{S0_abc}, and obtain unity power factor simultaneously at Bus 1 which has been assigned as the point of common coupling (PCC). Currently, there is negligible line impedance between Buses 1 and 2 representing the case where the device is installed nearer to the loads than to the feeder.

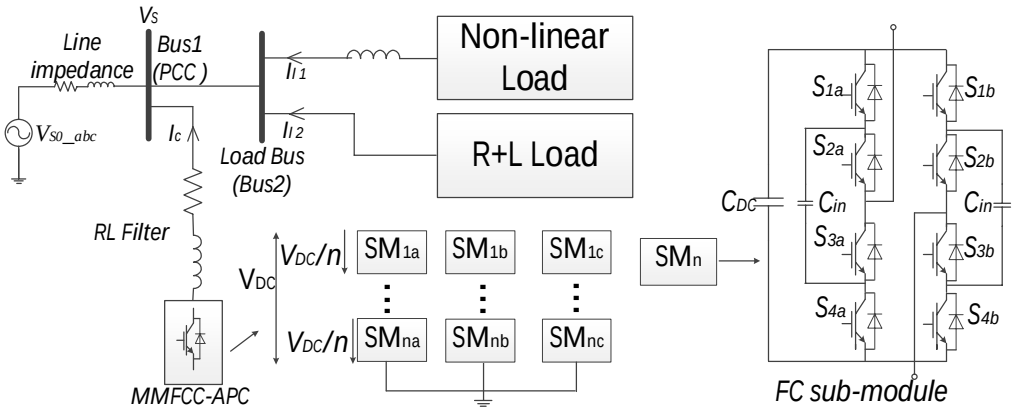


Fig. 3.12 Circuit configuration of MMFCC-APC

The MMFCC configuration used is also shown in Fig. 3.12; it is a three-phase single star configuration where each phase arm is a chain of 5-level flying capacitor converter (FC) sub-modules (SMs), which have been introduced in Chapter 2. With multiple modules in series, each only switches at a reduced frequency, hence having low switching losses, and a high total voltage can be attained. For this case, each chain synthesizes nine voltage levels ($0, \pm 0.25V_{DC}, \pm 0.5V_{DC}, \pm 0.75V_{DC}, \pm V_{DC}$) hence requiring two FC SMs in each phase. For practical industrial applications where the PCC voltage magnitude may be in the many tens of kilovolt range, the number of SMs is higher while the per module DC-link voltage is still kept to be relatively close to that investigated in this thesis.

The low-pass R-L filter connected between the PCC and MMFCC-APC is necessary for eliminating the harmonics due to converter switching and it may also represent the interfacing transformer equivalent impedance when the latter is used. The resistance and inductance parameter values should be carefully chosen since these can affect the accuracy of device current controller tracking, and hence the harmonics elimination performance. Generally, the harmonic and reactive currents caused by the load will

be compensated by the MMFCC-APC, in order that the PCC side current approximates to the ideal sinusoidal form with unity power factor.

3.4.2 Control schemes

The overall control scheme for the MMFCC-APC system is shown in Fig. 3.13 and is divided into four main parts: harmonics current extraction and reactive power compensation, model-based predictive current control, overall intra-cluster capacitor voltage balancing control, and a carrier-permutation phase shift (PS) pulse width modulation scheme.

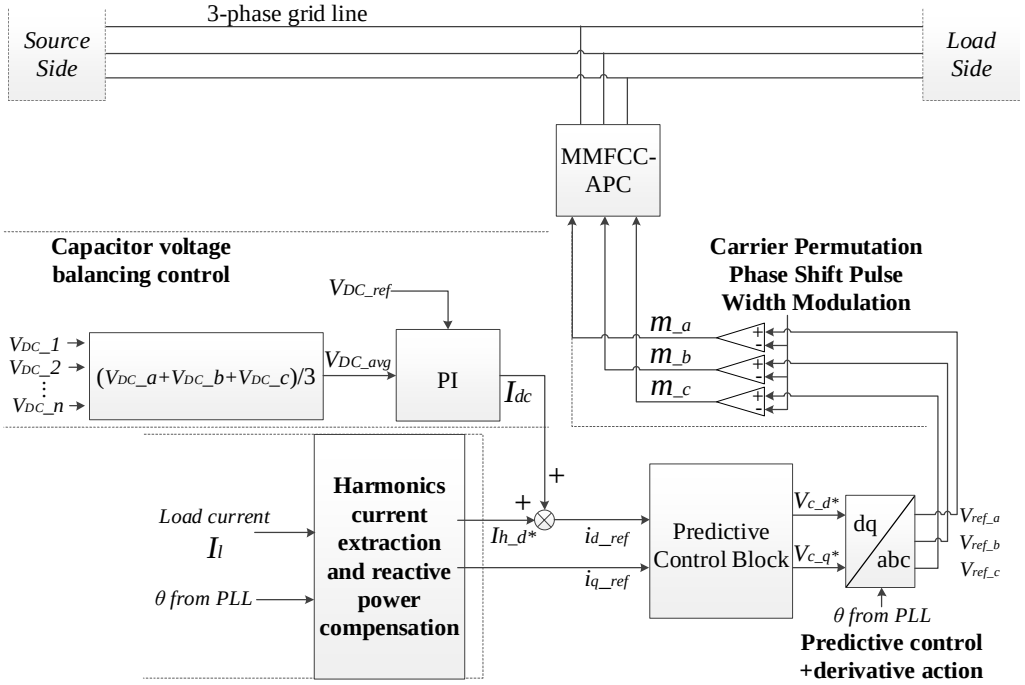
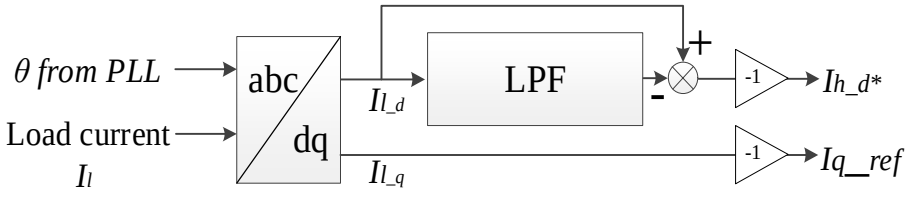


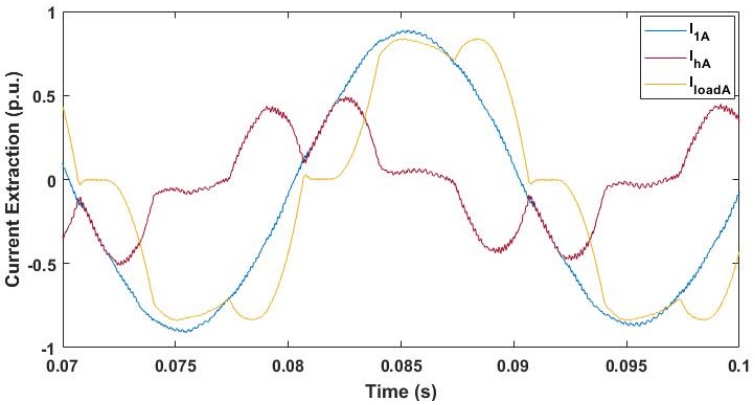
Fig. 3.13 Control schemes of the APC system

3.4.2.1 Current reference extraction

By using the low-pass filter-based extraction scheme described in the Section 3.3, all higher order harmonics in *d*-component can be extracted from the measured load current I_l, as shown in Fig. 3.14(a). To eliminate reactive current, make load current flowing from PCC to be in phase with the three phase voltages, the load current *q*-component $I_{l\text{-}q}$ is taken directly without filtering. This, together with the harmonics in the *d*-component forms the *dq* reference current for the converter current controller. Fig. 3.14(b) shows the measured phase A load current I_l, extracted harmonic and filtered phase A load current.



(a)



(b)

Fig. 3.14 (a) Harmonic extraction and reactive power compensation control block and (b) corresponding current harmonics extraction from phase A load current

3.4.2.2 Predictive current control

A. Operation Principle

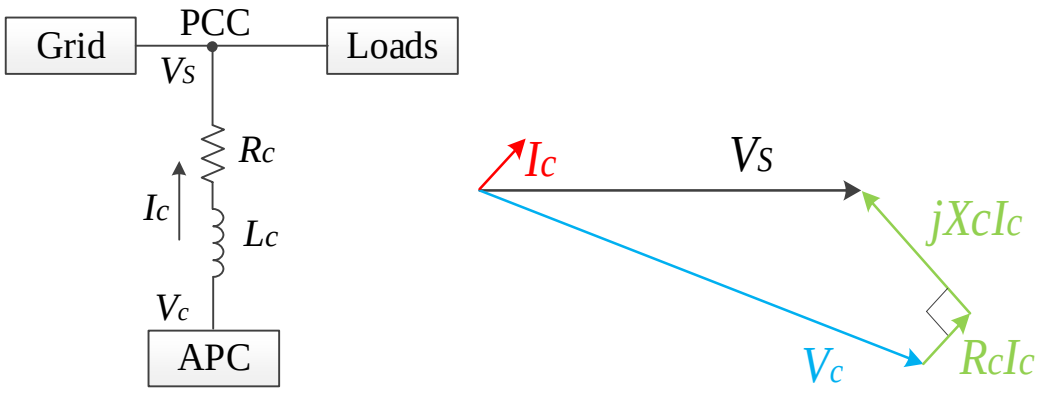


Fig. 3.15 (a) APC block diagram and (b) phasor diagram

The circuit of the system shown in Fig. 3.12 can be simplified as illustrated in Fig. 3.15(a) with its phasor diagram shown in Fig. 3.15(b), giving the following grid-connected converter's space vector equation.

$$\overrightarrow{V_S} - \overrightarrow{V_c} = L_c \frac{d\vec{\imath}_c}{dt} + R_c\vec{\imath}_c \qquad (3.9)$$

When implemented in a real digital system, a small sampling period T_s is chosen and defined as the time between the k^{th} and $(k+1)^{th}$ samples, hence the $\frac{d\vec{\imath}_c}{dt}$ can be expressed as

$$\frac{d\vec{\imath}_c}{dt} = \frac{\Delta\vec{\imath}_c}{T_s} = \frac{\vec{\imath}_c(k+1) - \vec{\imath}_c(k)}{T_s} \qquad (3.10)$$

Since the next sampling period current $\vec{\imath}_c(k+1)$ cannot be known in advance, it is replaced by the current reference value $\overrightarrow{\imath_c^*}(k)$. After substituting (3.10) into (3.9) and re-arrangement, the required reference voltage at the next sampling period can be derived as (3.11) and the completed *dq* voltage equations are given as (3.12).

$$\overrightarrow{V_c^*}(k) = \overrightarrow{V_S}(k) - \left[\frac{L_c}{T_s}\right]\overrightarrow{\imath_c^*}(k) + \left[\frac{L_c}{T_s} - R_c\right]\vec{\imath}_c(k) \qquad (3.11)$$

$$\begin{bmatrix} \overrightarrow{V_{c\_d}}^{*}(k) \\ \overrightarrow{V_{c\_q}}^{*}(k) \end{bmatrix} = \begin{bmatrix} \overrightarrow{V_{s\_d}}(k) \\ \overrightarrow{V_{s\_q}}(k) \end{bmatrix} - \begin{bmatrix} \frac{L_c}{T_s} & 0 \\ 0 & \frac{L_c}{T_s} \end{bmatrix} \begin{bmatrix} \overrightarrow{\iota_{c\_d}^{*}}(k) \\ \overrightarrow{\iota_{c\_q}^{*}}(k) \end{bmatrix} + \begin{bmatrix} \frac{L_c}{T_s} - R_c & -\omega L_c \\ \omega L_c & \frac{L_c}{T_s} - R_c \end{bmatrix} \begin{bmatrix} \overrightarrow{\iota_{c\_d}}(k) \\ \overrightarrow{\iota_{c\_q}}(k) \end{bmatrix} \quad (3.12)$$

The V_c^* is regarded as the reference voltage for the MMFCC and is used for generating the PWM signals. Using this the converter reference current tracking and the corresponding source current after harmonic extraction are shown in Fig. 3.16 which are not desirable.

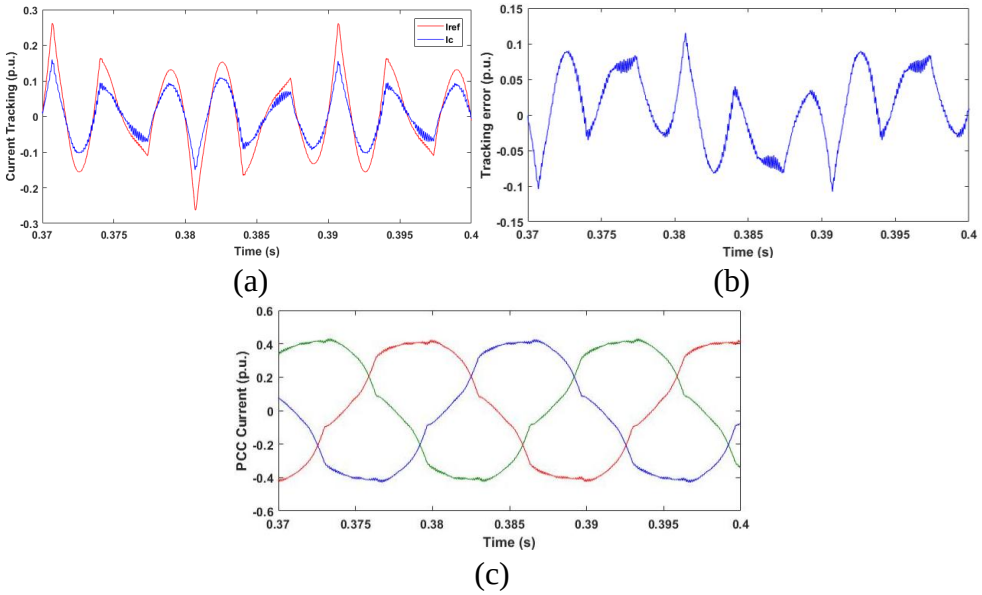


Fig. 3.16 (a) Simulated converter current reference tracking waveforms; (b) Reference tracking error; (c) Three-phase source current at PCC

There is clearly a tracking error between the converter and reference currents especially when load current changes sharply, which causes the three phase source current to be distorted. This is due to the delay stemming from the predictive controller's inherent feature, a 1-sample time delay is imposed to the control action. Also the use of an LPF with low bandwidth for harmonic reference current extraction incurs further delay.

B. Adding Derivative Action

The effective way is by adding a derivative term in the conventional predictive control algorithm. This is realised by using the reference current at the last sample and comparing its value with that at the current sample; the derivative value of the reference current can be obtained by evaluating the ratio of the difference between them over the sample time. Adding this derivative term to the original reference value a new reference current for the compensator is obtained, as shown below.

$$\overrightarrow{\iota_c^*}'(k) = \overrightarrow{\iota_c^*}(k) + \tau \frac{\overrightarrow{\iota_c^*}(k) - \overrightarrow{\iota_c^*}(k-1)}{T_s} \quad (3.13)$$

The equation shows a coefficient τ being used to scale the derivative term. The value of τ needs to be carefully chosen for achieving the desired compensation effect; in this study, through trial and error, $0 < \tau < 0.1$ was found to be sufficient in all cases.

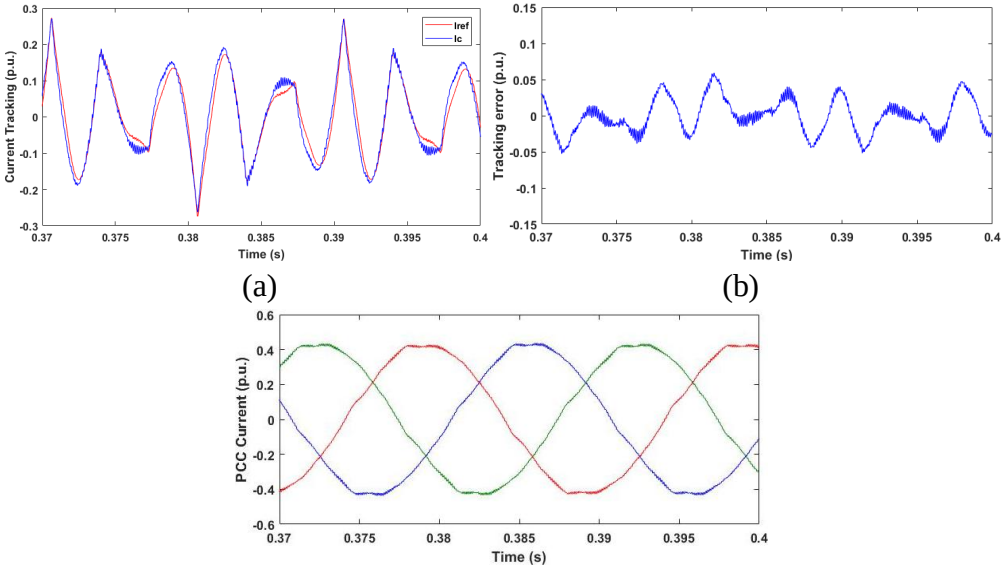
Thus, the MMFCC reference voltage vector can be expressed as (3.14) and the completed *dq* voltage equations are given as (3.15).

$$\overrightarrow{V_c}^*(k) = \vec{V_s}(k) - \left[\frac{L_c}{T_s} + \tau\frac{L_c}{{T_s}^2}\right]\vec{\imath_c^*}(k) + \tau\frac{L_c}{{T_s}^2} \times \vec{\imath_c^*}(k-1) + \left[\frac{L_c}{T_s} - R_c\right]\vec{\imath_c}(k) \tag{3.14}$$

The equivalent *dq* form of equation (3.14) is:

$$\begin{bmatrix}\overrightarrow{V_{c\_d}}^*(k)\\ \overrightarrow{V_{c\_q}}^*(k)\end{bmatrix} = \begin{bmatrix}\overrightarrow{V_{S\_d}}(k)\\ \overrightarrow{V_{S\_q}}(k)\end{bmatrix} - \begin{bmatrix}\frac{L_c}{T_s}\left(1+\frac{\tau}{T_s}\right) & 0\\ 0 & \frac{L_c}{T_s}\left(1+\frac{\tau}{T_s}\right)\end{bmatrix}\begin{bmatrix}\overrightarrow{i_{c_d}^*}(k)\\ \overrightarrow{i_{c_q}^*}(k)\end{bmatrix}$$
$$+\begin{bmatrix}\tau\frac{L_c}{{T_s}^2} & 0\\ 0 & \tau\frac{L_c}{{T_s}^2}\end{bmatrix}\begin{bmatrix}\overrightarrow{\imath_{c_d}^*}(k-1)\\ \overrightarrow{\imath_{c_q}^*}(k-1)\end{bmatrix} + \begin{bmatrix}\frac{L_c}{T_s} - R_c & -\omega L_c\\ \omega L_c & \frac{L_c}{T_s} - R_c\end{bmatrix}\begin{bmatrix}\overrightarrow{\imath_{c_d}}(k)\\ \overrightarrow{\imath_{c_q}}(k)\end{bmatrix} \tag{3.15}$$

Applying this control algorithm, the reference current tracking is as shown in Fig. 3.17(a) and (b). Fig 3.17(c) shows the corrected source side current. All these waveforms show significant improvement as compared to those in Fig. 3.16.



(a) (b)

(c)

Fig. 3.17 (a) Simulated converter current reference tracking waveforms; (b) Reference tracking error; (c) Three phase source current at PCC with modification (τ = 0.02)

3.4.2.3 Intra-cluster capacitor voltage control

This controls the voltages of all submodule capacitors within a phase cluster, which drift due to converter losses using the well-known and applied feedback DC voltage control. In an MMFCC the average voltage of all submodules is evaluated firstly by calculating per phase average voltage as

$$V_{DC\_(abc)} = \frac{1}{n_{SM}}\sum_{i=1}^{n_{SM}} V_{DC\_i(abc)} \tag{3.16}$$

where n_{SM} equals the number of SM in each phase limb. The total average is then derived as

$$V_{DC\_avg} = \frac{V_{DC\_a}+V_{DC\_b}+V_{DC\_c}}{3} \quad (3.17)$$

The resultant values applied to a PI controller with the reference voltage V_{DC_ref}, which is determined by the nominal DC voltage value for each SM. The output reference current signal I_{dc} from this controller is added onto the $I^*_{h\_d}$ to form the converter reference current I_{d_ref}. Consequently, the reference signal is applied for the PS-PWM scheme which has the advantage of giving lower THD with a relatively low switching frequency. Furthermore, the PS-PWM also gives a natural voltage balance to the FC module inner flying capacitors [80], and thereby the need for feedback control of their voltages is normally eliminated. However, the compensating of harmonics distorts the converter reference voltage and causes the capacitors voltage to drift away, so the conventional PS-PWM needs to be modified.

3.5 Carrier Permutation Phase Shift PWM Scheme for MMFCC

3.5.1 Capacitor natural balancing ability

An investigation on the impact of PS-PWM schemes for the MMFCC-APC is essential so that an insight into the submodule inner capacitor voltages natural balancing capability can be obtained. This will lead to the strategy for ensuring zero net charge exchange between the capacitors and the AC side terminals over one or several fundamental cycles. The capability can be further divided into the following two keys and illustrated in Fig. 3.18:

- **Capacitor voltage drift**: this is due to the capacitor charging and discharging patterns unequal in each fundamental cycle, causing its mean voltage to drift away from the nominal value over a number of fundamental cycles;
- **Capacitor voltage deviation from the mean level**: this is the charging and discharging capacitor voltage variation over single fundamental cycle, which magnitude normally depends on the capacitance and PWM schemes applied.

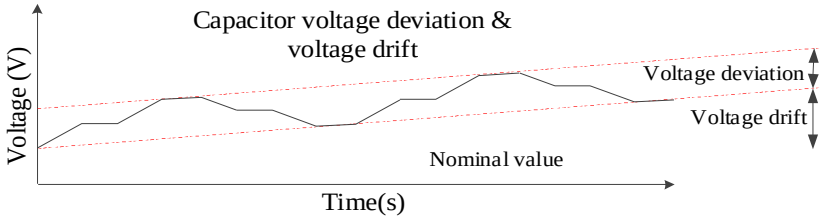


Fig. 3.18 Capacitor voltage drift and voltage deviation diagram

3.5.2 Conventional Phase Shift -PWM

The ideal sinusoidal voltage reference for PS-PWM with M_f=5, and the corresponding MMFCC phase A intra-cluster upper SM flying capacitor C_{SM1a} voltage waves, are shown in Fig. 3.19. As noticed, the voltage reference signals are purely sinusoidal in the fundamental cycle presented, therefore capacitors are charged and discharged equally and maintained at their nominal value 50V, resulting in zero voltage drift. Meanwhile the capacitor voltages deviations are within a small range of the nominal value, which gives an acceptable spectral quality of voltage output.

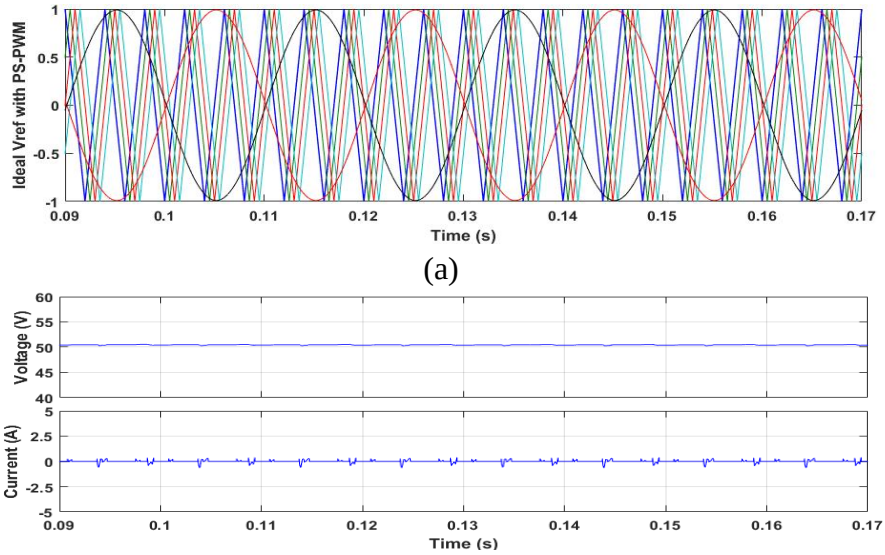


Fig. 3.19 (a) Ideal voltage reference signal for MMFCC with conventional PS-PWM and (b) corresponding MMFCC-APC phase A intra-cluster upper SM flying capacitor C_{SM1a} actions in 4 cycles

However in the case when the MMFCC is used to compensate load harmonic currents, the phase voltage is distorted, and its inherent balance property may not hold. Fig. 3.20(a) shows the phase A reference voltage compared with four carrier waveforms. The distorted reference signal causes imbalance in the SM capacitors' charging and discharging currents, and hence the total net charge transferred over one cycle is non-zero. At steady state this charge imbalance occurs repeatedly, causing the module capacitor voltages to deviate from their nominal levels despite additional feedback control of SM voltage. Fig. 3.20(b) shows the upper SM flying capacitor C_{SM1a} voltage drift.

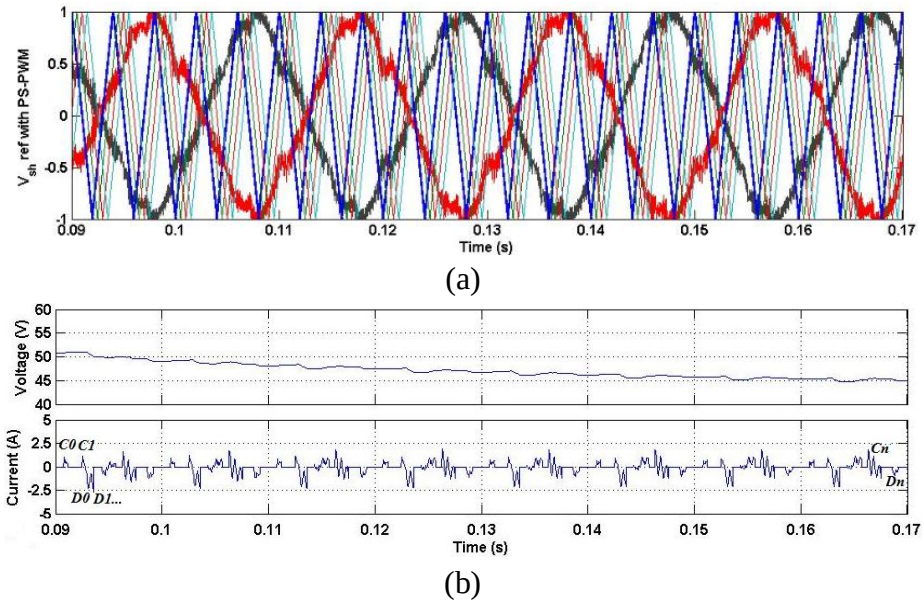


Fig. 3.20 (a) Voltage reference signal for MMFCC with conventional PS-PWM and (b) corresponding MMFCC-APC phase A intra-cluster upper SM flying capacitor C_{SM1a} actions in 4 cycles

The voltage and current waveforms of phase A upper first SM capacitor C_{SM1a} over 4 fundamental cycles from 0.09sec to 0.17sec are shown in Fig. 3.20(b). The states of charging and discharging this capacitor are counted as C0, C1…Cn and D0, D1…Dn, hence the net charges accumulated in this capacitor can be evaluated. This evaluation enables calculation of the total charges flowing through the capacitor during this period as Q_{total} given in (3.18)-(3.19). In this example Q_{total} during 0.09sec to 0.17sec is 0.026C. This results in the capacitor discharging and voltage decreasing gradually, as shown in Fig. 3.20(b), the capacitor voltage waveform. For a wider time range, the MMFCC submodule flying capacitor voltages in each phase are shown in Fig. 3.21, in which can be seen that they all drift away from the nominal value.

$$Q_{(CorD)} = \sum_{i=0}^{n}\left(\int_{t_a}^{t_b}\left(I_{(CorD)_i} * t\right)dt\right) \tag{3.18}$$

$$Q_{total} = Q_C - Q_D = \sum_{i=0}^{n}\left(\int_{t_a}^{t_b}\left(I_{C_i} * t\right)dt\right) - \sum_{i=0}^{n}\left(\int_{t_c}^{t_d}\left(I_{D_i} * t\right)dt\right) \tag{3.19}$$

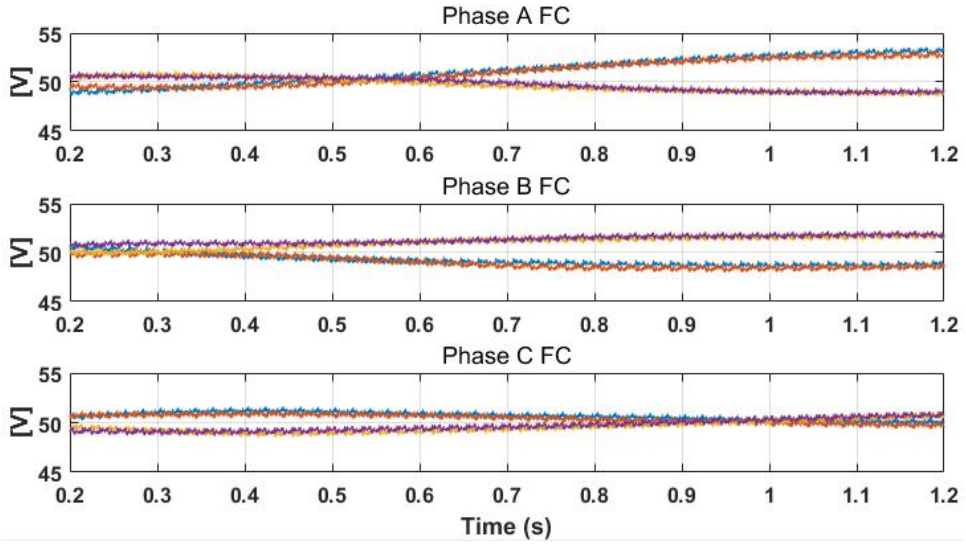
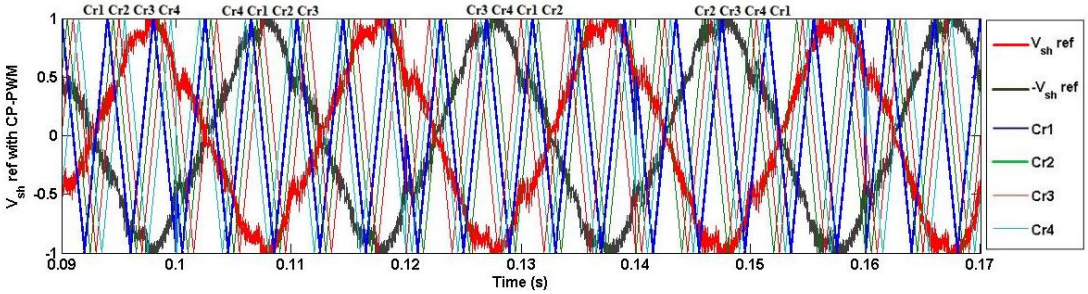


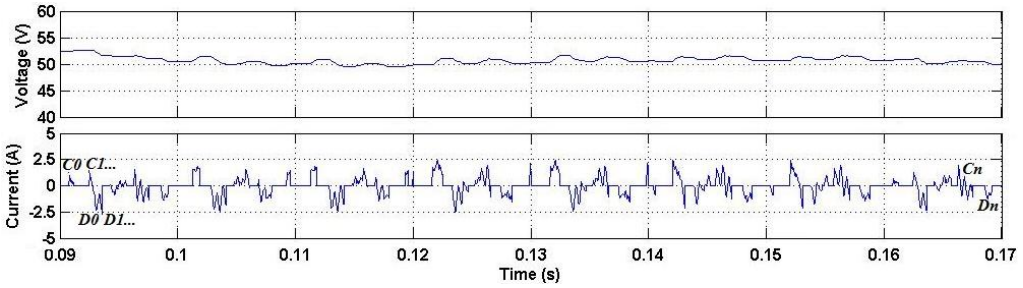
Fig. 3.21 SM FC voltages with conventional PS-PWM

3.5.3 Carrier Permutation Phase Shift-PWM

A Carrier Permutation PS-PWM (CP PS-PWM) method is proposed to prevent the inner capacitor voltage drift. Following the PS-PWM principle this method still uses multiple triangular carrier waveforms, but instead of applying each of them in a fixed sequence cycle by cycle they are cyclically permuted one position forward at the end of each fundamental cycle. Naturally with four carrier waves in this example a complete permutation cycle takes four fundamental cycles or 0.08sec, as shown in Fig. 3.22(a). This enables the charging and discharging current through the SM capacitors to vary from cycle to cycle according to the reference voltage pattern, and hence greatly reduces the drift.



(a)



(b)

Fig. 3.22 (a) Voltage reference signal for using the CP PS-PWM method for MMFCC-APC, and (b) corresponding phase A intra-cluster upper SM flying capacitor C_{SM1a} actions in 4 cycles

As shown in Fig. 3.22(b), with CP PS-PWM, the charging and discharging patterns for the same capacitor C_{SM1a} in a phase limb change from cycle 1 to cycle 4. The total charge accumulated for the same capacitor as above is now less than before and the net charge flowing out of the capacitor is 0.00045C which is much lower than before, thus demonstrating the effectiveness of this new method. The capacitor voltage drops from 52 to 50 V in the interval 0.09sec to 0.11sec, and after the carrier waveform swap, increases back to a higher value. As a result the capacitor voltage floats around its nominal value within a small range, as shown in Fig. 3.22(b). For a wider time range, the 12 flying capacitor voltage waveforms of the three phases are shown in Fig. 3.23. Comparing with Fig. 3.21, the voltages are all stable and around 50V. This proves that the CP PS-PWM scheme can effectively prevent the inner flying capacitor drifting away from the nominal value when the voltage reference is distorted.

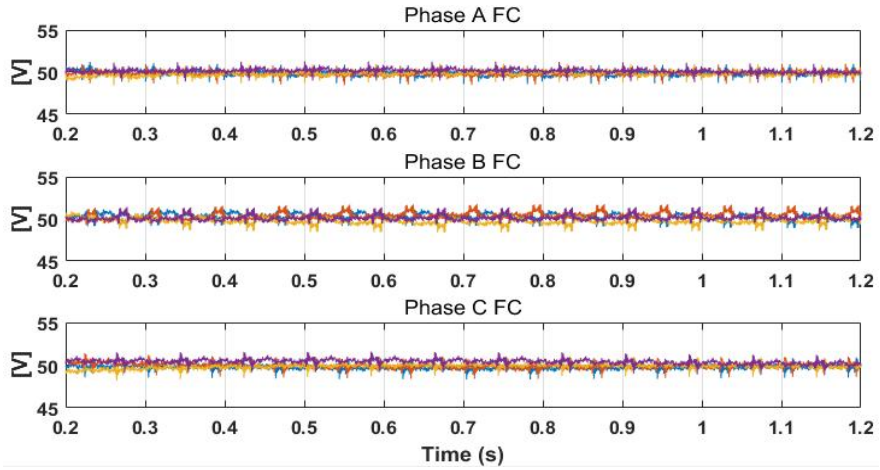


Fig. 3.23 SM FC voltages with CP PS-PWM

3.6 Simulation Study

The proposed MMFCC-APC is simulated where the APC system and corresponding control strategies are implemented using SIMULINK/MATLAB. The parameters of the simulated system and device are listed in Table 3.3 and the configuration is shown in Fig. 3.24. V_{S0} and the load are constitutive elements of a 3-phase balanced system; the former is considering at a distribution environment such as universities, so it is rated 110V, 3.3KVA, 50Hz and the latter contains a three phase full bridge thyristor-controlled rectifier in parallel with a three phase R+L load of power factor 0.83. The analysis of these loads parameters is shown in the next subsection. The firing angle $\boldsymbol{\alpha}$ varies from 0° to 60°, giving different load current harmonic distortion conditions. The R-L filter for the converter is selected according to (3.20) to satisfy both fast response and give low enough cut-off frequency to eliminate switching harmonics (126.53Hz).

$$f_c = \frac{R_c}{2\pi L_c} \tag{3.20}$$

$$= \frac{1.59}{2\pi \times 0.002} = 126.53\,Hz$$

The MMFCC per phase total DC voltage is rated at 200V, hence each 5-level FCC submodule DC capacitor voltage is 100V, while it is chained with two submodule converters in each phase. The capacitance is chosen according to the maximum energy required to provide, which is determined by the compensating active and reactive powers. In the MMFCC system, the total stored energy can be expressed as (3.21) and (3.22) in terms of per MVA of the MMCC rating. Thus, the capacitance is derived as (3.23). In [95], the authors evaluated that an energy of 30-40 kJ/MVA is required in order to restrict capacitor voltage ripples within 10% of its nominal value. So, for an MMCC of 18 KVA, 800V, the estimated capacitance of DC capacitor is 1 mF.

$$E_{MMCC} = \frac{3N}{2} C_{DC} {V_{DC}}^2 \tag{3.21}$$

$$E_S = \frac{3N}{2S} C_{DC} {V_{DC}}^2 \tag{3.22}$$

$$C_{DC} = \frac{2SE_S}{3N{V_{DC}}^2} \tag{3.23}$$

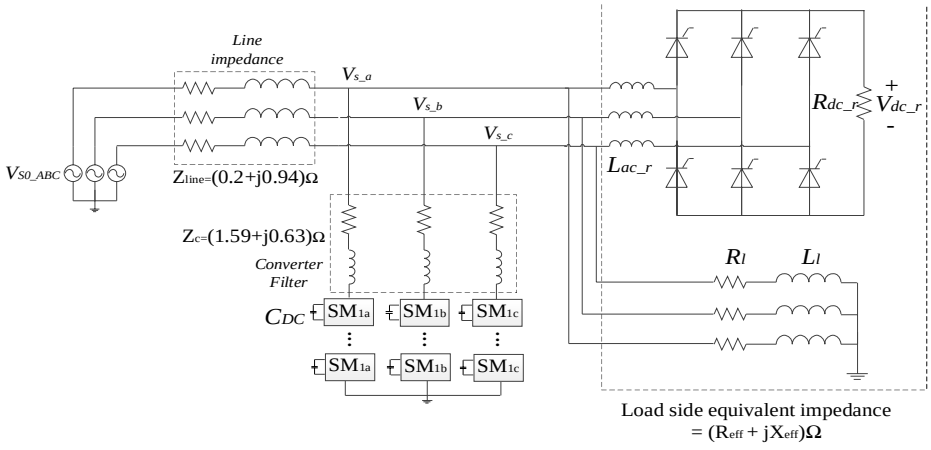


Fig. 3.24 Power system configuration

Table 3.3 MMFCC-APC system parameters

Components		Value
PCC Side	Source end voltage V_{S0}	110 V
Distribution Line	Aluminium PI TX line (d= 10mm, l=1.1km)	R_{line} = 0.2 Ω L_{line} = 3mH
Load Side	3-Phase Thyristor Rectifier	R_{dc_r} = 20Ω L_{ac_r} = 8.3mH
	Firing angle α	0°; 30°; 60°
	R+L Load	R_l = 10Ω L_l = 48mH
Converter Side	RL Filter	R_c = 1.59Ω L_c = 2mH
	DC capacitor	C_{DC}= 1.12 mF
	DC voltage V_{dc} in each sub-module	100 V
	Switching frequency f_s	1 kHZ

3.6.1 Three-phase harmonic rectifier load

The three-phase harmonic load is represented by a full-bridge thyristor-controlled rectifier, which draws nonlinear current with low-order harmonics from the PCC. The levels of load current distortion can be adjusted by thyristor firing angle α whilst the effective impedance of the rectifier also changes; from Table. 3.3, the value of DC side resistance R_{dc_r} and AC side inductance L_{ac_r} of the rectifier are known as *20Ω* and *8.3mH* respectively, and the R-L load parameters are R_l = *10Ω*, L_l = *48mH*. Therefore the power factor (*PF*) can be derived and calculated as 0.83 when α is 0° from the following equations:

The power transfer between the AC and DC sides of the rectifier can be derived in (3.24) by eliminating losses.

$$\frac{V_S^2}{R_{ac\_r}} = \frac{V_{dc\_r}^2}{R_{dc\_r}} \tag{3.24}$$

Substituting V_{dc_r} with PCC voltage [96] and thus:

$$V_{dc\_r} = 1.35 \times \sqrt{3} V_S \cos\alpha \tag{3.25}$$

$$R_{ac\_r} = \frac{R_{dc\_r}}{5.47 \cos^2\alpha} \tag{3.26}$$

$$R_{eff} = \frac{R_{dc\_r} R_l}{R_{dc\_r} + 5.47 R_l \cos^2\alpha}\ ;\ X_{eff} = 100\pi \frac{L_{ac\_r} L_l}{L_{ac\_r} + L_l} \tag{3.27}$$

Therefore, the PF can be derived as (3.28).

$$PF = \frac{R_{eff}}{\sqrt{(R_{eff})^2+(X_{eff})^2}} \quad (3.28)$$

When α is 0°, the R_{eff} and X_{eff} are calculated as 2.677Ω and 2.223Ω respectively, hence the power factor is 0.83.

3.6.2 Performance of MMFCC-APC with balanced nonlinear load

3.6.2.1 Scenario 1: Harmonics Compensation

The harmonic compensation performance of the APC is analysed under different load conditions. These are carried out by changing the firing angle of the thyristor controlled load thus creating various harmonic distortion levels: three operating scenarios are tested where the firing angle α is set at 0° initially, then changed to 30° at 0.1sec and 60° at 0.2sec.

PCC side current responses

The currents drawn from the PCC source side without and with harmonic control are respectively compared as shown in Figs. 3.25 and 3.26. At the start, α is 0°, the currents are seen as to be distorted (Fig. 3.25 section (a)) since it is the case without harmonics compensation. Meanwhile, for the same time period and firing angle α as that in Fig. 3.25, Fig. 3.26 shows the APC switched on to perform the filtering function; the current distortions are all eliminated in section (**a***). When α changes to 30° at 0.1 sec and 60° at 0.2 sec, again all the harmonics shown in Fig. 3.25 are filtered as can be seen in Fig. 3.26. The corresponding harmonic spectra and their corresponding THDs are presented in Fig. 3.27. It can be observed that the THD reduces significantly when the APC is in operation, as shown in Figs 3.27(a*), (b*) and (c*).

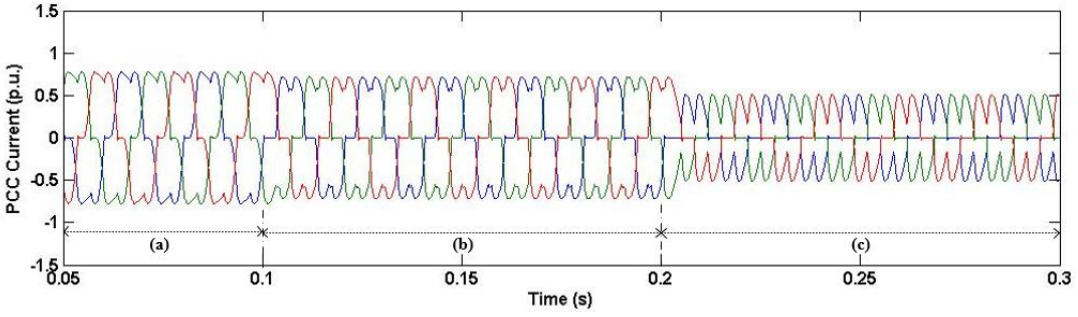


Fig. 3.25 Uncompensated PCC source current when α changes from 0° to 60°

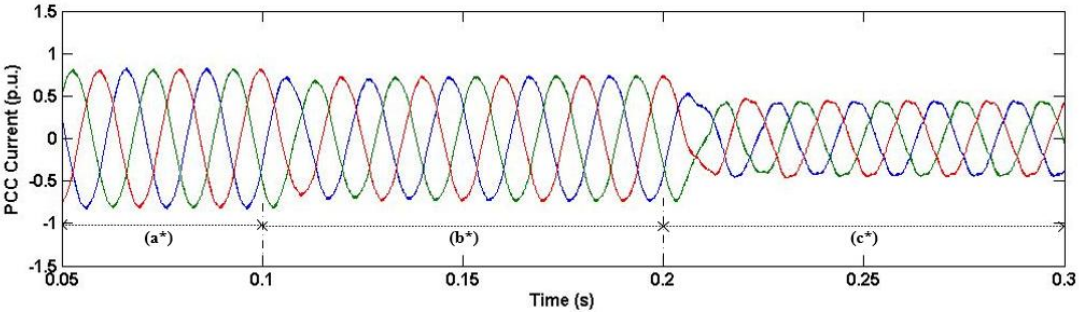


Fig. 3.26 Compensated PCC source current when α changes from 0° to 60°

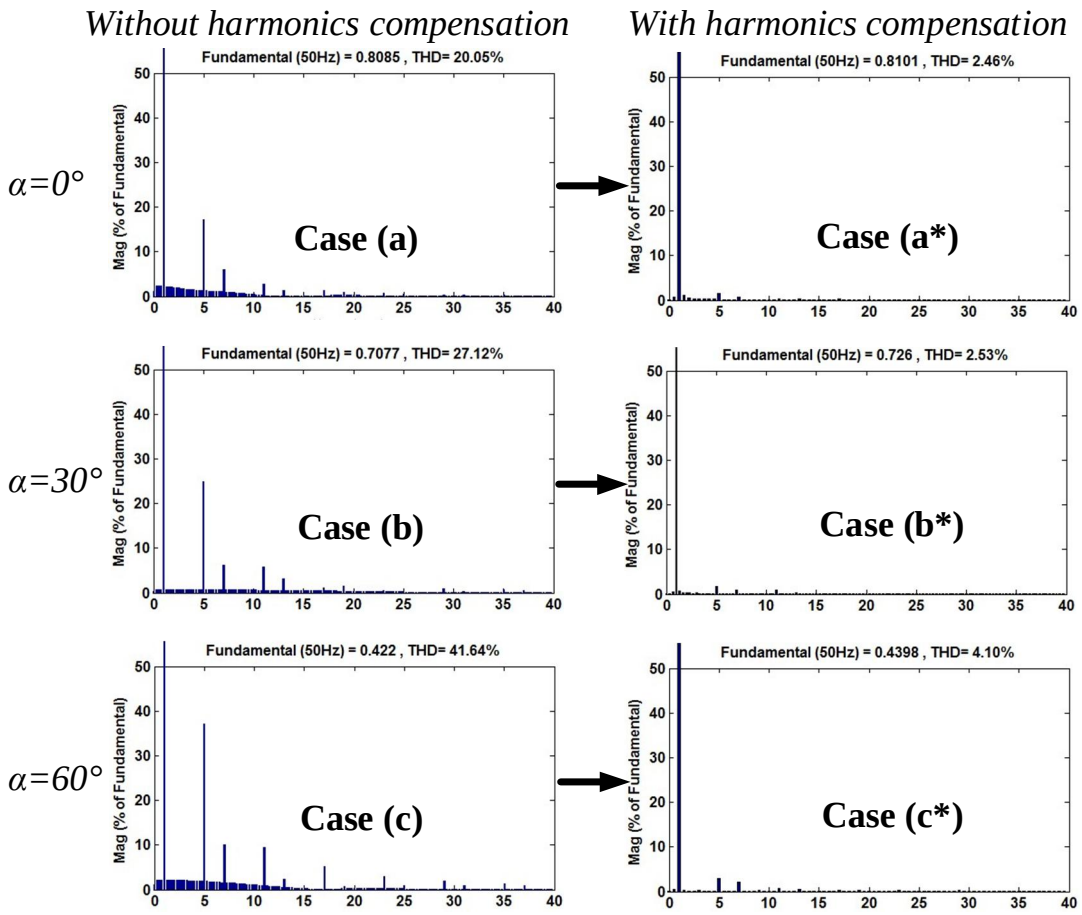
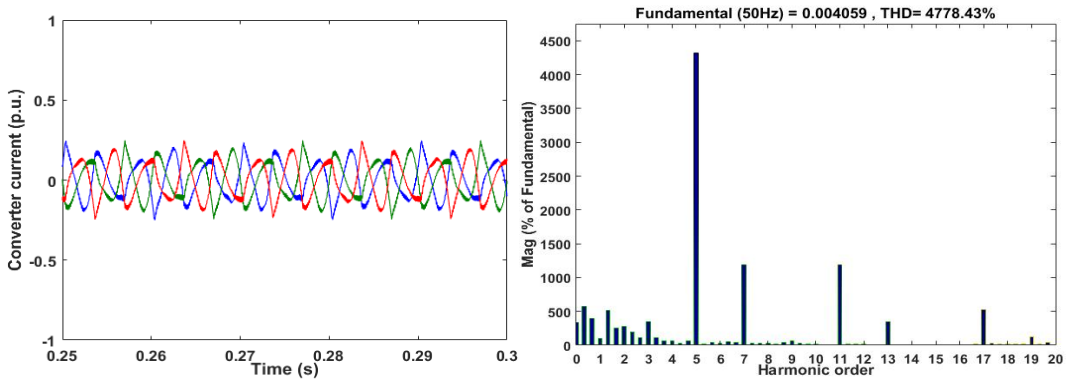


Fig. 3.27 Source harmonic current spectra for different simulation scenarios

APC side responses

Fig. 3.28(a) shows the three-phase current waveforms measured at the APC terminals. In contrast to the PCC current waveforms, the APC currents are highly distorted and only contain harmonic components without the fundamental. Fig. 3.28(b) presents the harmonic spectrum with high magnitudes of lower order harmonics of 5^{th}, 7^{th} and 11^{th}. The THD of the phase current is clearly very high. Fig. 3.29 shows the 3-phase converter phase voltage with 9 distinctive levels.



(a) (b)

Fig. 3.28 (a) APC voltage and current waveforms and (b) its harmonic spectrum

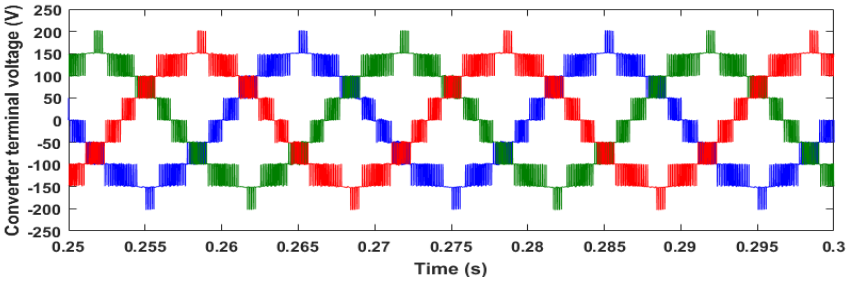


Fig. 3.29 3-phase converter voltage waveforms

Submodule capacitors voltage responses

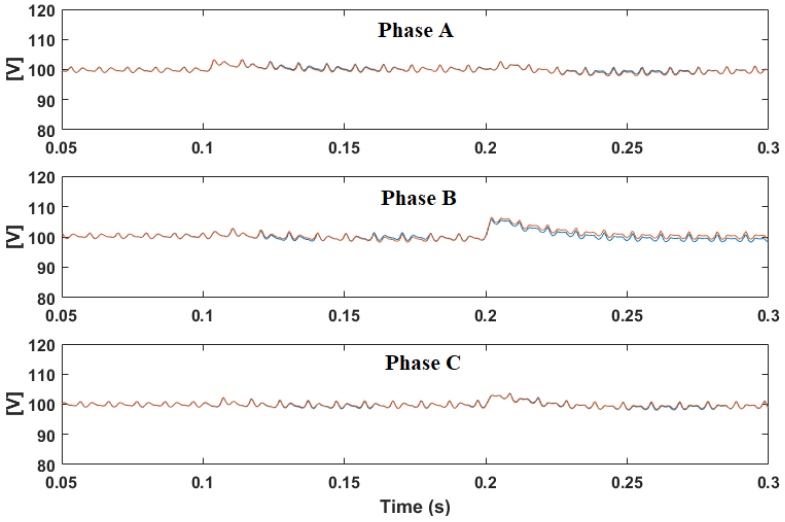


Fig. 3.30 Submodule DC capacitors voltage waveforms

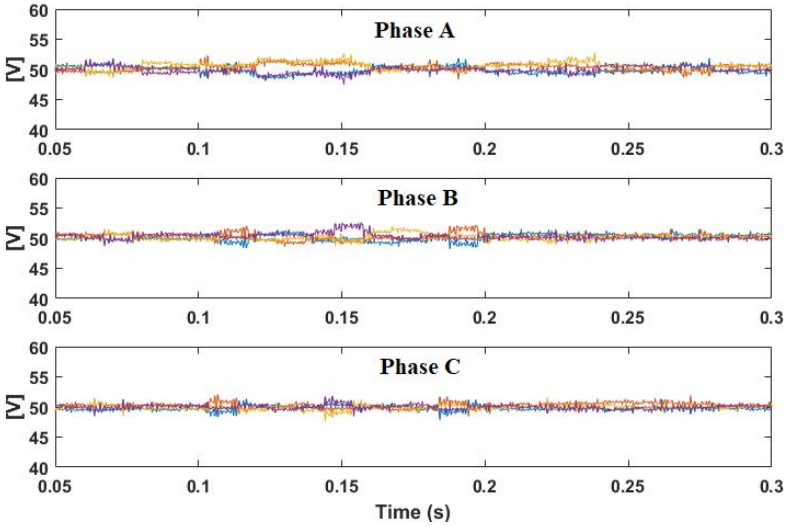


Fig. 3.31 Submodule inner flying capacitors voltage waveforms

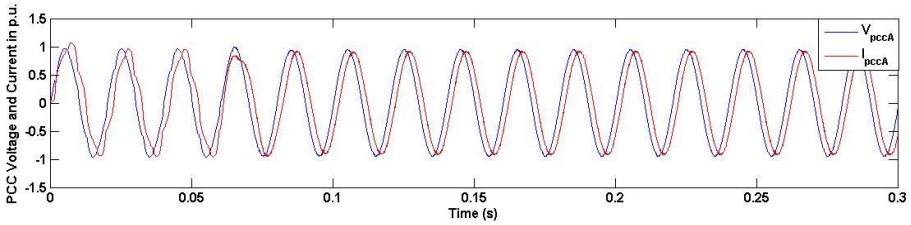
Figs. 3.30 and 3.31 show the MMFCC submodule DC and inner flying capacitors voltage waveforms which are well balanced at their respective nominal values of 100V and 50V, with little ripple seen respectively. When the firing angle α changes from 0° to 30° at 0.1 sec and 60° at 0.2 sec, the DC capacitor voltage oscillations can be seen but the ripple percentages are still maintained to the level below 10% of 100V, corresponding to the requirement set by ABB [97].

3.6.2.2 Scenario 2: Unity Power Factor Correction

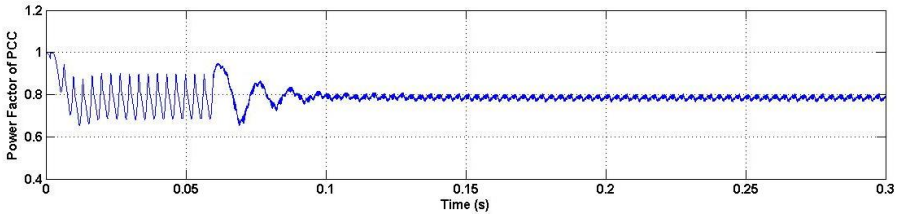
The performance of the APC for simultaneous harmonics compensation and reactive power control was also studied. To do this, another two cases are simulated and compared; one is only for harmonics control without reactive current compensation and the other is for both which is introduced at t = 0.06sec while the firing angle is set at 0° for both cases.

PCC voltage and source current

The first case is depicted in Fig. 3.32 and, as expected without reactive current control but with harmonic elimination the source currents are smooth enough, but lagging the PCC voltages in (a) and the power factor is maintained at 0.8 as shown in (b). When reactive power control is incorporated in the APC at t = 0.2sec, a unity power factor is achieved as shown in Fig. 3.33(a) and (b). Also smooth and fast transient responses for both compensations can be observed.

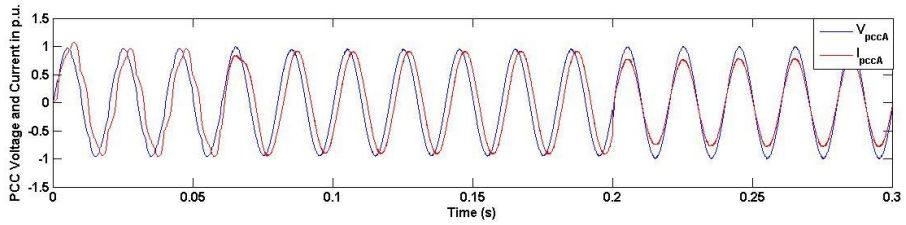


(a)

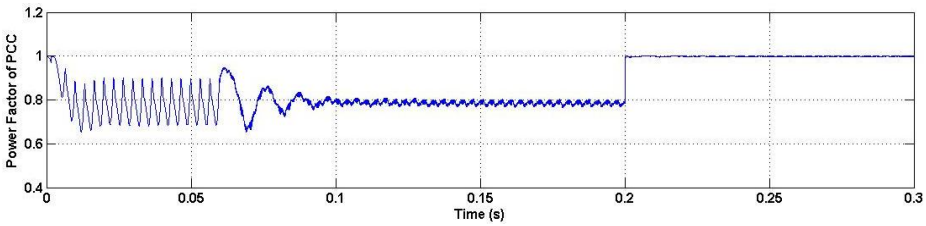


(b)

Fig. 3.32 (a) PCC voltage and current and (b) PCC power factor variation with harmonics control but without reactive power compensation



(a)

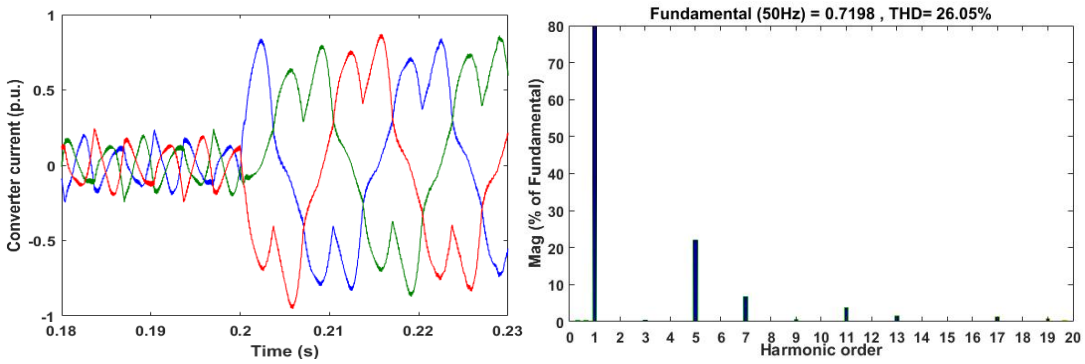


(b)

Fig. 3.33 (a) PCC voltage and current and (b) PCC power factor variation with both harmonics control and reactive power compensation

APC voltage and current responses

Fig. 3.34 shows the 3-phase current waveforms measured at the APC side terminals. From 0.18sec to 0.2sec, the APC only controls PCC current harmonics and thus the converter current remains the same as with the Fig. 3.28 result when α=0°,. It contains only harmonics but no fundamental (50Hz) waveform. However, when the APC controller commands the device to compensate both harmonics and reactive power, the current will start to draw reactive component (which is 50Hz AC current) and its magnitude will also increase from 0.2p.u to 0.8p.u. The harmonics spectrum is shown in Fig. 3.34(b).



(a) (b)

Fig. 3.34 (a) APC current waveforms (b) harmonic spectrum (during 0.21-0.23sec)

Submodule capacitors voltage responses

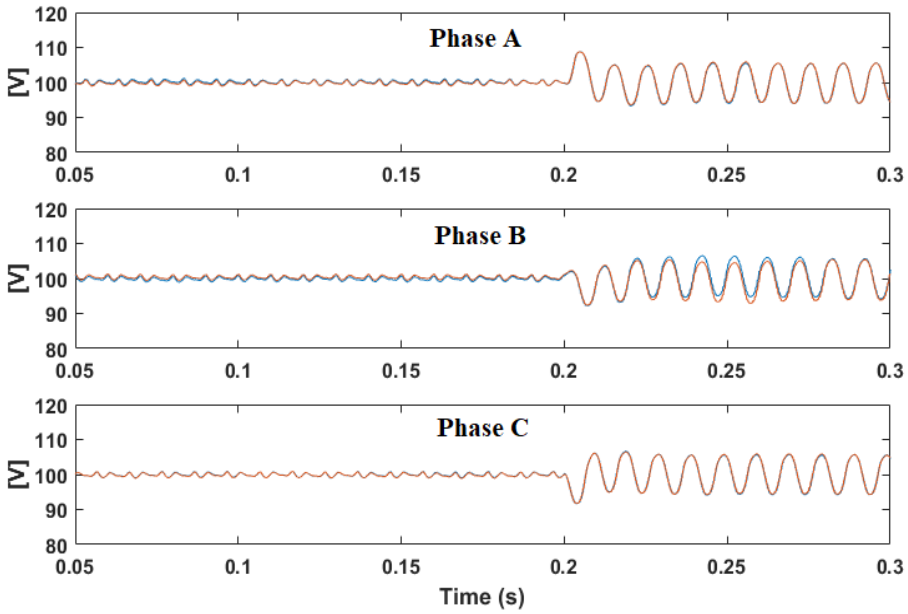


Fig. 3.35 Submodule DC capacitors voltage waveforms

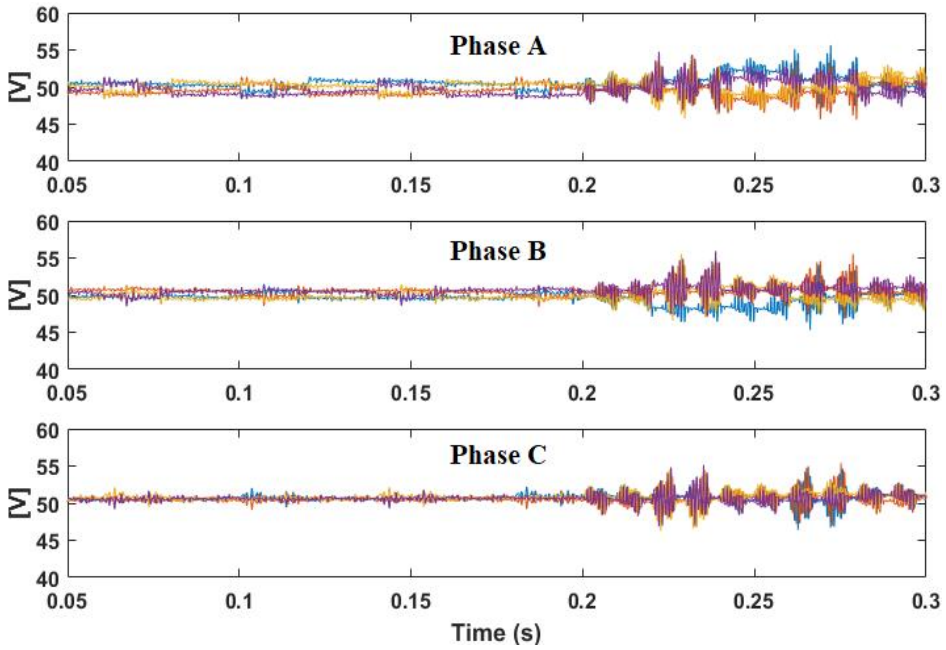


Fig. 3.36 Submodule inner flying capacitors voltage waveforms

Fig. 3.35 and 3.36 show respectively the corresponding DC submodule and inner flying capacitor voltage waveforms which are all maintained at their nominal values of 100V and 50V. However, as the APC starts to eliminate harmonics and compensate reactive power for the grid simultaneously, the voltage ripple across both the DC capacitors and the inner flying capacitors will increase but the voltages still remain within 10% of nominal values.

3.7 Summary

This chapter presented an active power conditioner which is capable of performing both active power filtering and reactive power control, based on using an MMFCC to cope with a nonlinear load and a complex inductive load situation in a balanced power system. The converter switching is based on a carrier permutation PS-PWM method implemented to avoid the unbalance of intra-cluster submodule capacitor voltages. Meantime, the abrupt rate-of-change in generation of current harmonics is solved by a predictive controller with a derivative action method. The final simulation results show that high quality harmonics filtering can be achieved for the specimen systems so far studied, while fast transient response can be obtained with and without reactive power compensation.

Chapter 4 Active Power Conditioner using MMFCC under Unbalanced Load Conditions

4.1 Introduction

The proliferation of power electronic controlled equipment in distribution systems has brought some undesirable effects. One of these is the drawing of harmonic current from the utility grid and the other is unbalanced load current, due to large single-phase loads, such as traction drives, and renewable energy sourced generators. An MMCC can be used to not only eliminate the harmonics, but also compensate the unbalanced load current. However, the key issue for accurate and highly dynamic compensation is that it relies on high performance reference current extraction. The low-pass filter used for balanced current operation in Chapter 3 is insufficient for the unbalanced case, and a new efficient method with higher precision is required.

There is also a particular challenge posed to an MMCC-APC when compensating unbalanced current; this is that supplying unbalanced components results in unequal power flowing through the MMCC three phase limbs. This results in phase cluster DC voltages drifting away from their nominal value since the DC link capacitors per phase are separated. This is called the inter-cluster voltage unbalance. It leads to distorted currents being injected into the grid, and can also overstress or even damage the switching devices.

This chapter starts by analysing load current harmonic levels and contents under different load imbalance cases, and comparing the results with those under balanced load conditions. This leads to a general analysis of harmonics in an unbalanced load. Following the analysis this chapter presents two harmonic plus unbalanced current extraction methods; one is the existing low-pass filter-based approach and the other is a new notch filter-based technique. The theme of the chapter also includes the control methods needed for an MMCC-APC to suppress not only load reactive and harmonic current but also the unbalanced elements. The MMFCC topology is still considered and its three phases in either star (called SSBC) or delta (SDBC) connections are considered. The control schemes combining both current control algorithm and inter-cluster voltage balancing scheme for both connections will be discussed.

4.2 Analysis for Three-phase Network Supplying Non-linear and Unbalanced Load

This section investigates network current harmonic characteristics when load current is unbalanced. To emulate a variety of unbalanced load conditions, three different unbalanced cases are simulated as shown in Fig. 4.1. Case A has a single phase R-L load represented by Z_1 connected to phase A of the supply line and to ground, which creates a higher fundamental phase current flowing to phase A than to the other phases.

This is a common situation in practice, for example, a traction drive may be fed from only a single-phase supply. In Case B, a resistor R_2 is connected in series with phase A of the thyristor load, causing a lower current drawn to this phase. In Case C the resistor R_2 is still connected in phase A, while an impedance Z_2 is connected in phase B at the supply end representing transmission line impedance imbalance, hence the unbalance happens in two phases simultaneously.

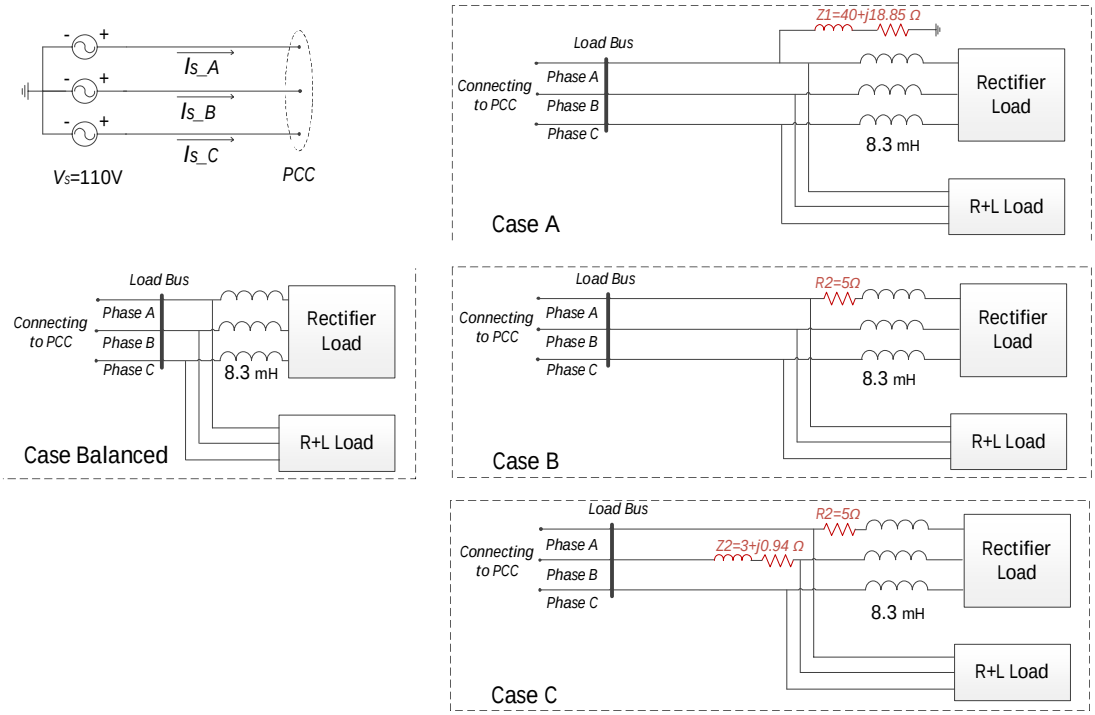


Fig. 4.1 Illustrations of different unbalanced load cases studied

For ease of comparison, a three-phase balanced case presented in Chapter 3 is used; the magnitudes of fundamental and dominant low order current harmonics in each phase are listed and their THDs are evaluated as shown in Table 4.1.

Table 4.1 Analysis of currents of the 3-phase harmonic load for balanced load

Firing angle α	**0°**	**30°**	**60°**
50Hz	8.85	7.93	5.10
150Hz	0	0	0
250Hz	1.26	1.51	1.38
350Hz	0.41	0.43	0.28
450Hz	0	0	0
550Hz	0.19	0.32	0.37
THD	15.24%	20.54%	29.06%

(Unit: Ampere)

4.2.1 Case A: nonlinear load with additional load on one phase

The three-phase current I_{s_ABC} in this case is as shown in Fig. 4.2. The harmonic analysis is carried out for the firing angle α at 0°, 30° and 60°. The harmonic magnitudes and THDs are listed in Table 4.2.

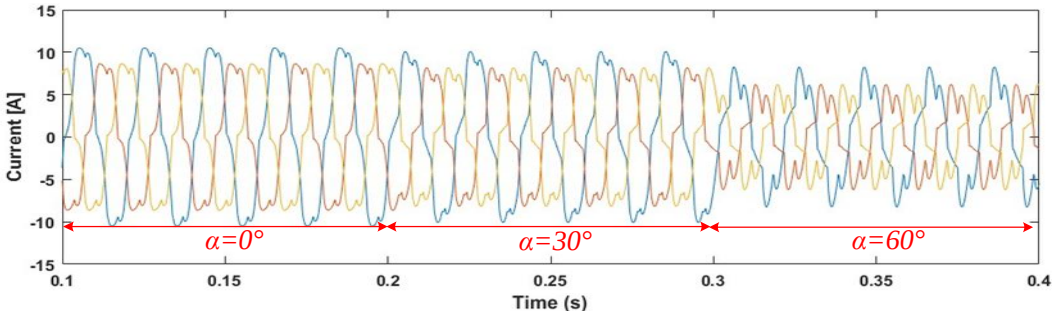


Fig. 4.2 AC current waveforms when α changes from 0° to 60° for Case A

(Phase A: blue, Phase B: red, Phase C: yellow)

Table 4.2 Magnitudes of major current harmonic elements for Case A

Firing angle α	0°	30°	60°
50Hz	10.88	9.95	7.06
	8.85	7.93	5.1
	8.85	7.93	5.1
150Hz	0	0	0
	0	0	0
	0	0	0
250Hz	1.26	1.51	1.38
	1.26	1.51	1.38
	1.26	1.51	1.38
350Hz	0.41	0.43	0.28
	0.41	0.43	0.28
	0.41	0.43	0.28
450Hz	0	0	0
	0	0	0
	0	0	0
550Hz	0.19	0.32	0.37
	0.19	0.32	0.37
	0.19	0.32	0.37
THD	12.39%	16.36%	20.99%
	15.24%	20.52%	29.06%
	15.24%	20.52%	29.06%

(Unit: Ampere)

It can be seen that the phase A fundamental current magnitude is always higher than that of the other two phases while all the harmonics magnitudes are balanced. Consequently, the THD of Phase A is lower than the other two phases. The key features for this case can be summarised as follows:

- Comparing with the balanced case, phase A draws higher fundamental current, due to the additional load on this phase. The magnitudes of all harmonic components across the three phases are the same.

- The fundamental current imbalance results in THDs for phase A being lower than the other two phases.
- The triplen harmonics are absent in this case because the harmonics are balanced and there is no neutral line.

4.2.2 Case B: Nonlinear load with one phase different

In this case, a 5 Ω resistor is connected into phase A line of the three-phase rectifier load. This emulates the situation when one phase of the nonlinear load draws less current. The 3-phase distorted AC current waveform is shown in Fig. 4.3 for the firing angle α at 0°, 30° and 60°. Table 4.3 gives the detailed results of the analysis in terms of the harmonic magnitudes at different frequencies and the corresponding THD levels.

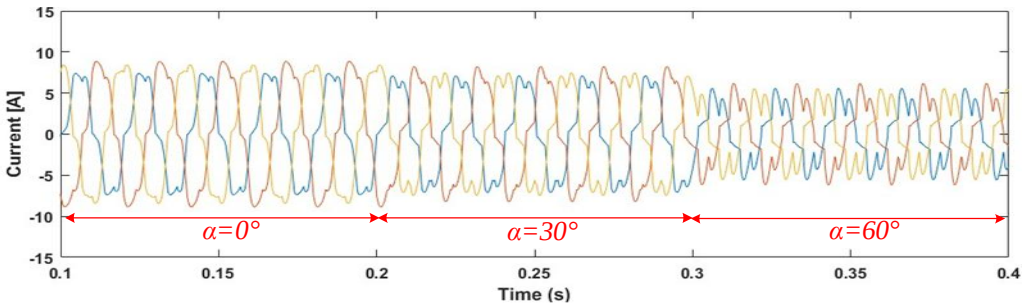


Fig. 4.3 AC current waveforms when α changes from 0° to 60° for Case B

(Phase A: blue, Phase B: red, Phase C: yellow)

Table 4.3 Magnitudes of major current harmonic elements for Case B

Firing angle α	0°	30°	60°
50Hz	7.35	6.79	4.47
	8.73	7.54	4.85
	8.56	7.38	4.68
150Hz	0.39	0.05	0.02
	0.5	0.46	0.29
	0.5	0.48	0.29
250Hz	1.16	1.33	1.21
	0.91	1.33	1.22
	1.01	1.41	1.34
350Hz	0.17	0.32	0.31
	0.57	0.43	0.31
	0.44	0.45	0.28
450Hz	0.16	0.05	0.01
	0.08	0.07	0.03
	0.15	0.1	0.04
550Hz	0.11	0.34	0.34
	0.06	0.29	0.33
	0.12	0.29	0.36
THD	17.16%	21.09%	29.4%
	13.72%	20.36%	27.87%
	14.40%	21.77%	31.32%

(Unit: Ampere)

The harmonic characteristics in this case can be summarised as follows:

- The magnitudes of fundamental and harmonic current elements for all three phases are reduced and they are all unbalanced. The magnitudes of the 5th harmonic for all phases and firing angles are the highest.
- The triplen harmonics are present due to their also being unbalanced in the three phases;
- When α increases from 0° to 30° to 60°, the differences between the highest and lowest current magnitudes among the three phases are reduced from 1.38A to 0.75A to 0.38A (fundamental components) and consequently the unbalance level of the load is reduced.

4.2.3 Case C: Nonlinear load with two phase impedances different

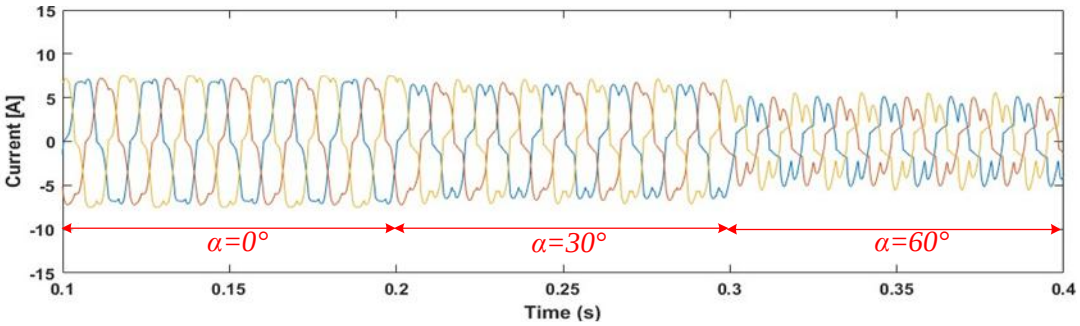


Fig. 4.4 AC current waveforms when α changes from 0° to 60° for Case C

(Phase A: blue, Phase B: red, Phase C: yellow)

Table 4.4 Magnitudes of major current harmonic elements for Case C

Firing angle α	0°	30°	60°
50Hz	7.29	6.56	4.31
	7.12	6.29	4.1
	7.98	6.86	4.42
150Hz	0.28	0.21	0.13
	0.26	0.25	0.13
	0.25	0.11	0.09
250Hz	0.99	1.2	1.11
	0.8	1.06	0.97
	0.91	1.32	1.22
350Hz	0.26	0.37	0.27
	0.33	0.31	0.24
	0.43	0.39	0.26
450Hz	0.04	0.02	0.02
	0.06	0.03	0.01
	0.08	0.01	0.02
550Hz	0.14	0.28	0.31
	0.08	0.24	0.26
	0.13	0.29	0.33
THD	14.74%	20.25%	28.17%
	12.86%	18.73%	25.76%
	13.25%	20.88%	29.71%

(Unit: Ampere)

In this case, the unbalance occurs due to additional impedance added on two phases. Consequently, phase A and B current magnitudes are lower than that of phase C, as shown in Fig. 4.4. According to Table 4.4, harmonic components in Case C have features similar to those in Case B.

In general, different load imbalance cases result in different levels of current imbalance and harmonic distortions. These can be grouped into two categories: When the unbalance happens due to a single-phase linear load connected on one of the phases (Case A), it only affects the fundamental current magnitude of the connected phase, while the other two phases' fundamental components are unchanged and the harmonics across the three phases are still balanced. However if the unbalance is caused by impedance differences in one or two lines feeding the three-phase load (Cases B and C respectively), both the fundamental and harmonics will be unbalanced and the triplen harmonics start to appear.

4.2.4 Analysis of unbalanced fundamental, symmetrical and asymmetrical harmonics

4.2.4.1 Unbalanced fundamental current

The three-phase fundamental current can be expressed by Equation (4.1):

$$\begin{aligned} i_{1A} &= I_{1A}\cos(\omega t + \varphi_I) \\ i_{1B} &= I_{1B}\cos(\omega t + \varphi_I - \tfrac{2\pi}{3}) \\ i_{1C} &= I_{1C}\cos(\omega t + \varphi_I + \tfrac{2\pi}{3}) \end{aligned} \tag{4.1}$$

where φ_I is the phase angle difference between the PCC voltage and current phasors. With current imbalance, they can be decomposed, according to Fortescue's theorem as shown in Fig. 4.5, to three symmetrical phasor systems, namely positive sequence, negative sequence and zero sequence as given by Equation (4.2). The negative phase sequence (-ve) is reversed from positive sequence (+ve), while the zero sequence three phases share the same magnitude and phase angle. The relationship between +ve, -ve and zero sequence systems is derived in Appendix B.1.

$$i_{ABC} = I^+ + I^- + I^0 = i^+\begin{bmatrix}\cos(\omega t + \varphi_{Ip}) \\ \cos(\omega t - \frac{2\pi}{3} + \varphi_{Ip}) \\ \cos(\omega t + \frac{2\pi}{3} + \varphi_{Ip})\end{bmatrix} + i^-\begin{bmatrix}\cos(\omega t + \varphi_{In}) \\ \cos(\omega t + \frac{2\pi}{3} + \varphi_{In}) \\ \cos(\omega t - \frac{2\pi}{3} + \varphi_{In})\end{bmatrix} + i^0\begin{bmatrix}\cos(\omega t + \varphi_{I0}) \\ \cos(\omega t + \varphi_{I0}) \\ \cos(\omega t + \varphi_{I0})\end{bmatrix} \tag{4.2}$$

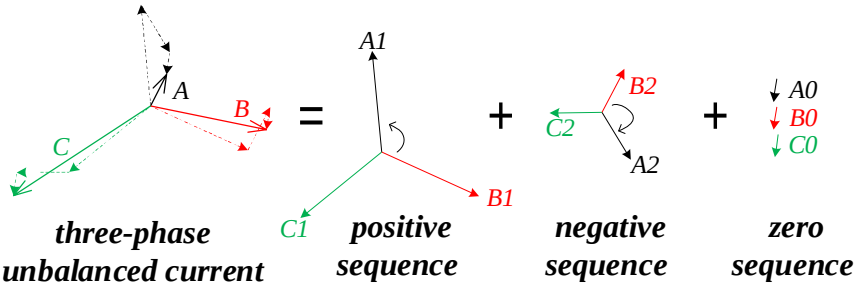


Fig. 4.5 Three-phase unbalanced current with its symmetrical components

The 3-phase current vector can be expressed in the α-β frame by using the Clark transformation as

$$i_{\alpha\beta} = \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = [T_{\alpha\beta}] i_{ABC} = I^+ \begin{bmatrix} \cos(\omega t + \varphi_{Ip}) \\ \sin(\omega t + \varphi_{Ip}) \end{bmatrix} + I^- \begin{bmatrix} \cos(-\omega t + \varphi_{In}) \\ \sin(-\omega t + \varphi_{In}) \end{bmatrix} \quad (4.3)$$

where $[T_{\alpha\beta}] = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}$. Note that, with no neutral connection, zero sequence is cancelled.

Projection of $i_{\alpha\beta}$ on positive and negative synchronous reference frames, rotating at $+\omega$ and $-\omega$ respectively leads to i_{dq}^+ and i_{dq}^- which are expressed as

$$i_{dq}^+ = \begin{bmatrix} i_d^+ \\ i_q^+ \end{bmatrix} = [T_{dq}{}^{+1}] i_{\alpha\beta} = I_1^+ \begin{bmatrix} \cos\varphi_{Ip} \\ \sin\varphi_{Ip} \end{bmatrix} + I_1^- \begin{bmatrix} \cos 2\omega t & \sin 2\omega t \\ -\sin 2\omega t & \cos 2\omega t \end{bmatrix} \begin{bmatrix} \cos\varphi_{In} \\ \sin\varphi_{In} \end{bmatrix} \quad (4.4)$$

$$i_{dq}^- = \begin{bmatrix} i_d^- \\ i_q^- \end{bmatrix} = [T_{dq}{}^{-1}] i_{\alpha\beta} = I_1^- \begin{bmatrix} \cos\varphi_{In} \\ \sin\varphi_{In} \end{bmatrix} + I_1^+ \begin{bmatrix} \cos 2\omega t & -\sin 2\omega t \\ \sin 2\omega t & \cos 2\omega t \end{bmatrix} \begin{bmatrix} \cos\varphi_{Ip} \\ \sin\varphi_{Ip} \end{bmatrix} \quad (4.5)$$

where $[T_{dq}{}^{+1}] = \begin{bmatrix} \cos\omega t & \sin\omega t \\ -\sin\omega t & \cos\omega t \end{bmatrix} = [T_{dq}{}^{-1}]^T$.

With reference to above expressions, one can see the cross coupling between *d*-*q* axis signals of both synchronous reference frames. The positive *d* and *q* components contain an AC component at twice the fundamental frequency, ω, with the amplitudes equal to the negative sequence DC term. Likewise the negative *d* and *q* components have an AC element of 2ω having the same magnitude as the positive DC term. The cross coupling of –ve fundamental elements to +ve element at the synchronous reference frame creates challenges to harmonic extraction, since 2ω terms need to be eliminated. This will be discussed later.

4.2.4.2 Symmetrical harmonics

For balanced harmonic current (like the balance current case in Chapter 3 and the Case A), only odd harmonics are present. Even harmonics are disregarded since they arise from asymmetry between positive and negative half-cycles and are negligible in most power systems.

The lowest few odd harmonics, such as 3rd, 5th and 7th, can be expressed as (4.6)-(4.8).

$$\begin{aligned} i_{3A} &= I_{3A} \cos 3\omega t \\ i_{3B} &= I_{3B} \cos 3(\omega t - \tfrac{2\pi}{3}) = I_{3B} \cos 3\omega t \\ i_{3C} &= I_{3C} \cos 3(\omega t + \tfrac{2\pi}{3}) = I_{3C} \cos 3\omega t \end{aligned} \quad (4.6)$$

$$\begin{aligned} i_{5A} &= I_{5A} \cos 5\omega t \\ i_{5B} &= I_{5B} \cos 5(\omega t - \tfrac{2\pi}{3}) = I_{5B} \cos(5\omega t + \tfrac{2\pi}{3}) \\ i_{5C} &= I_{5C} \cos 5(\omega t + \tfrac{2\pi}{3}) = I_{5C} \cos(5\omega t - \tfrac{2\pi}{3}) \end{aligned} \quad (4.7)$$

$$
\begin{aligned}
i_{7A} &= I_{7A}\cos 7\omega t \\
i_{7B} &= I_{7B}\cos 7(\omega t - \tfrac{2\pi}{3}) = I_{7B}\cos(7\omega t - \tfrac{2\pi}{3}) \\
i_{7C} &= I_{7C}\cos 7(\omega t + \tfrac{2\pi}{3}) = I_{7C}\cos(7\omega t + \tfrac{2\pi}{3})
\end{aligned}
\tag{4.8}
$$

It can be seen from the above that the third harmonic has three phase currents which are all in phase with one another and have equal magnitude. Hence they exist as a zero-sequence element only, and cancel each other on phase line. In fact this applies to all triple harmonics. The 5th harmonic has three phase currents with the same magnitude and the same phase differences between each other, but the phase sequence is the reverse of that of the applied voltage, hence it is a negative-sequence vector only. For the 7th harmonic its three phase currents also have the same magnitude and the phase differences between each other are equal, but the phase sequence is positive, so it exists as a positive-sequence vector. From all these instances it is clear that under symmetrical conditions the harmonics can be categorized, according to h = 1, 2, 3…, into three groups; (6h-3) the zero sequence harmonics, (6h+1) the +ve and (6h-1) the –ve. Only the third order and triplen harmonics are zero-sequence harmonics and all the other symmetrical harmonics are either +ve or -ve sequences.

4.2.4.3 Asymmetric harmonics

With the harmonics being unbalanced across three phases (Cases B and C), the triple harmonics start to appear and all the other odd harmonic components are asymmetrical. Thus they may consist of positive, negative and zero-sequence components regardless of their orders.

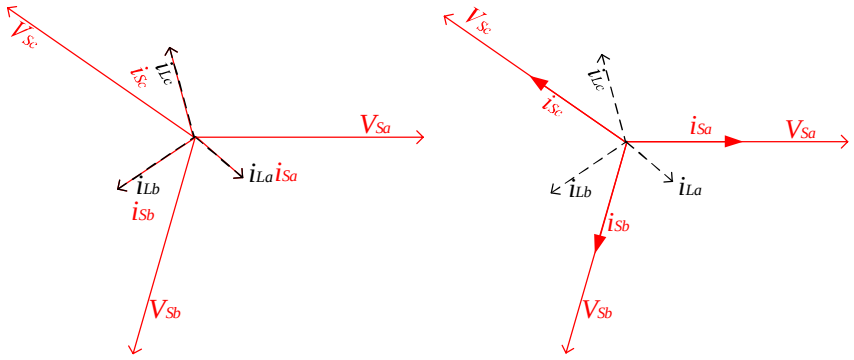
$$
\begin{aligned}
i_{hA} &= I_{hA}\cos h(\omega t + \varphi_{Ih}) \\
i_{hB} &= I_{hB}\cos h(\omega t + \varphi_{Ih} - \tfrac{2\pi}{3}) \\
i_{hC} &= I_{hC}\cos h(\omega t + \varphi_{Ih} + \tfrac{2\pi}{3})
\end{aligned}
\tag{4.9}
$$

Consequently these elements need to be extracted for harmonic elimination.

4.3 Unbalanced and Harmonic Current Cancellation

4.3.1 Current compensation requirement

Let the three-phase voltage, V_s, at PCC as the reference phasor, the current phasor from/to the PCC is i_s, and the total load current is i_L. A 3-phase network phasor diagram can be shown as shown in Fig. 4.6(a), where V_s and i_s are drawn in red and load current i_L in black. Without any voltage sources at load end, nor harmonic compensation, i_s should have the same magnitude and phase shift as that of i_L which is unbalanced and phase lagging V_S by $\varphi_{IP,}$ hence they overlap.



(a) (b)

Fig. 4.6 The phasor diagram of (a) 3-phase network voltage and unbalanced current and (b) when it achieves rebalanced current and unity power factor

To achieve unity power factor, with balanced as well as harmonic-free current operation for the network, i_s should ideally be in phase with V_s, with neither -ve sequence fundamental element nor ±ve sequence harmonics. This requires that MMCC-based APC cancels not only all the harmonic and fundamental reactive current elements, but also the negative sequence current of the grid line, the resultant i_s being

$$i_{\alpha\beta} = I_1^+ \begin{bmatrix} \cos(\omega t) \\ 0 \end{bmatrix} \tag{4.10}$$

Consequently, the phasor diagram can be illustrated as that in Fig. 4.9(b). It can be seen that i_s is now rebalanced and in phase with V_s.

4.3.2 Current reference generation schemes

The current reference generation scheme should be able to extract all the harmonics, fundamental reactive current elements and -ve sequence current. There are time domain and frequency domain extraction schemes proposed in the past few years. In frequency domain, the most widely adopted scheme is based on Fast Fourier Transform (FFT) harmonic detecting and extraction [98], which takes large computations and slow response speed under time-varying condition in order to improve accuracy [99]. In the time domain there are two solutions: one is based on the composite observers which can extract reference accurate without transformation coordination [100, 101], while the most existing schemes are based on the instantaneous reactive power theory [90, 102-104].

4.3.2.1 Composite observer-based scheme

The block diagram of this scheme is shown in Fig. 4.7, which is based on using the voltage and current composite observers [105]. The observer is a closed loop model of the system, with an open loop part consisting of N controlled digital oscillators connected in shunt as sub-blocks for both the fundamental signal and each order harmonic. This scheme is complex due to a lot of calculations, also it requires for time unvaried frequency and harmonics, hence it is not widely applied in industries.

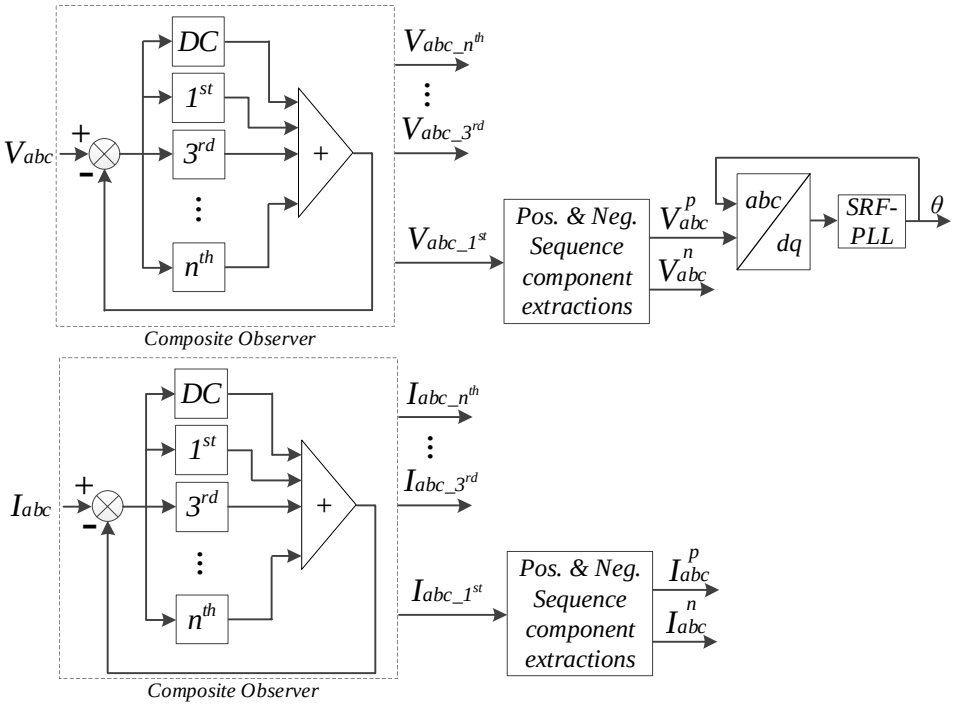


Fig. 4.7 Composite observer-based scheme

4.3.2.2 Instantaneous reactive power theory-based scheme

This scheme is as shown in Fig. 4.8. Based on the Clark transformation and instantaneous power calculation, the oscillating real and imaginary powers $\tilde{p}$ and $\tilde{q}$ can be extracted and used for calculating the converter reference current.

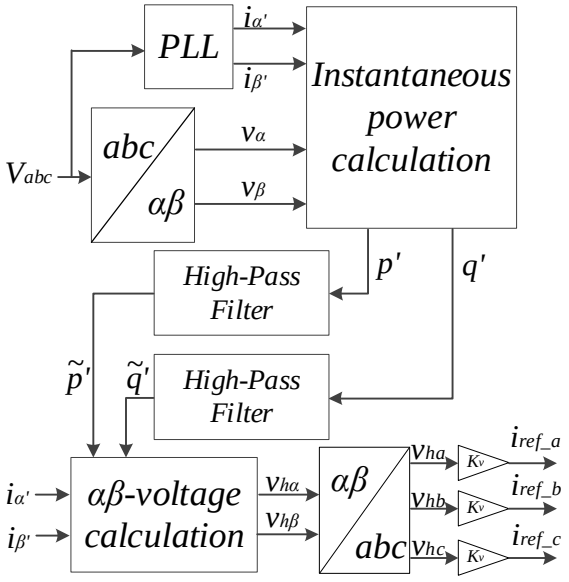


Fig. 4.8 Instantaneous reactive power theory-based scheme

This is the most popular method for harmonics detection and extraction, however, the drawback of this method shown in the last chapter has indicated that the voltage distortion and/or unbalance may cause an imprecise power calculation and as well as reference current generation, therefore, an extra +ve sequence voltage detector may

be required which increases computational effort. Furthermore, these schemes are based on the stationary reference frame hence not suitable for the SRF.

It can be seen that the existing schemes not only having their own benefits but also the drawbacks. Meantime, the DDSRF discussed in Chapter 1 [106] make it possible to extend the work based on the SRF. In this thesis, there are two schemes been proposed; one is based on the low-pass filter scheme as presented in Chapter 3, and the other is the new band-stop filter-based method.

4.3.2.3 Proposed Low-pass filter-based scheme

Implementation of this scheme for unbalanced case differs to that in Chapter 3 since it needs to extract unbalanced fundamental and harmonics in the load current simultaneously. In this case PLL should identify both +θ and -θ of source voltage, and using Park transformation the measured load current can be decomposed into its equivalent +ve and –ve *dq* elements in rotating reference frame. As has been shown in Equations (4.4) and (4.5) the resultant *dq* current elements contain not only DC and (*h*-1) terms (where *h* is the harmonics order), but also significant 2ω oscillatory cross coupling terms between +ve and –ve sequence currents. To eliminate the 2ω cross coupling terms present in both current elements, the DDSRF is applied. As shown in Fig. 4.9, DDSRF block in the figure processes the input i_{dq}^{+} and i_{dq}^{-} using Equation (4.11):

$$\begin{cases} \bar{i}_{load\_dq}^{*\ +} = [F]\{i_{dq}^{+} - [T_{dq}^{+2}]\bar{i}_{dq}^{-}\} \\ \bar{i}_{load\_dq}^{*\ -} = [F]\{i_{dq}^{-} - [T_{dq}^{-2}]\bar{i}_{dq}^{+}\} \end{cases} \tag{4.11}$$

where $[F] = \begin{bmatrix} LPF(s) & 0 \\ 0 & LPF(s) \end{bmatrix}$, $[T_{dq}^{+2}] = [T_{dq}^{-2}]^{T} = \begin{bmatrix} \cos 2\omega t & \sin 2\omega t \\ -\sin 2\omega t & \cos 2\omega t \end{bmatrix}$ and $LPF(s) = \frac{\omega_f}{s+\omega_f}$, $\omega_f < 628.3$ rad/s.

The derivation of the above is shown in Appendix B.2. The resultant $\bar{i}_{load\_dq}^{*\pm}$ are current elements comprising +ve *d* and *q* fundamental and harmonic current and –ve *d* and *q* fundamental and harmonic current. Except the +ve *d* fundamental, all other elements need to be in the reference current. To extract harmonic elements in the +ve sequence current *dq* components, two low-pass filters, as described in the Chapter 3, are applied. The obtained $I_{h\_d}^{*}$ and $I_{h\_q}^{*}$ are summed up with the decoupled +ve sequence *q*-component. These signals, together with the decoupled -ve sequence *dq* elements, form the reference current for the MMFCC-APC. It is worth noting that there is still a +ve *d* component, $I_{1\_d}^{+}$, produced from the overall capacitor voltage control loop which must be added on to the reference current as illustrated in Fig.4.9.

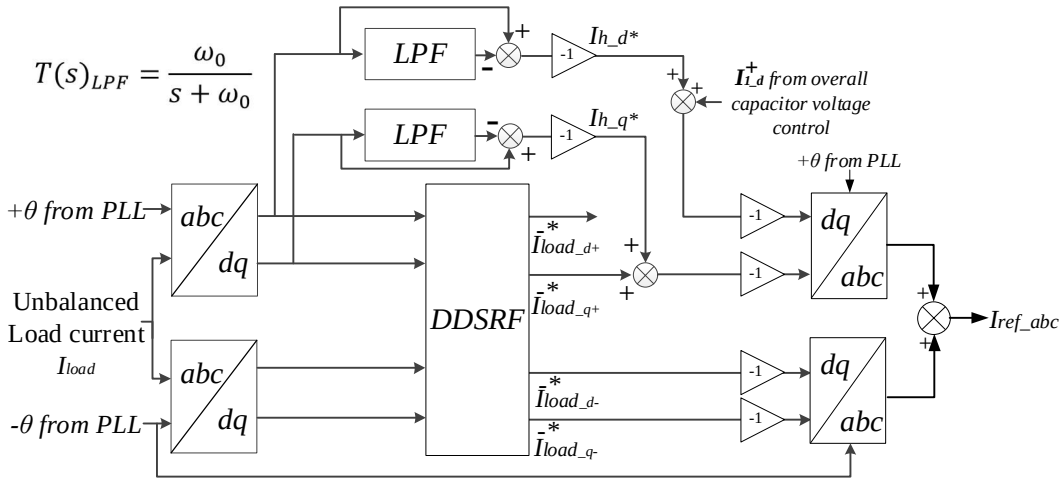


Fig. 4.9 LPF-based harmonic and reactive power extraction scheme

As already stated in the previous chapter, this scheme can extract all current harmonic elements with frequencies higher than the fundamental and able to cope with harmonic changes due to load variations. However it is less accurate due to very low filter bandwidth. Another drawback of this scheme is due to the DDSRF. The decoupling process is designed to eliminate the 2ω oscillation terms between the $\pm(dq)$ frames. However, as discussed in Cases B and C, the 3rd harmonic component in the load current cannot be ignored when the harmonics are also unbalanced in a three-phase system. These 3rd harmonic currents will be converted into 2ω terms and also be eliminated by the DDSRF during Park transformation, which causes a reference extraction error; thus making an APC not mitigating harmonics precisely.

4.3.2.4 Proposed NF-based scheme

This method uses a number of band-stop Notch filters (NF) cascaded to stop all dominant frequency elements in a few specific bands.

The transfer function of a simple Notch filter (NF) is given in Equation (4.12).

$$T(s)_{NF} = \frac{s^2+\omega_0^2}{s^2+2\sigma\omega_0 s+\omega_0^2} \quad (4.12)$$

It is a second-order element where ω_0 defines the centre frequency it is desired to stop; for example, if the 5th harmonic is set as the notch frequency to be notched (i.e. remove 5th harmonic), then the stopped angular frequency ω_0 = 1571 rad/s. Fig. 4.10 illustrates the Bode plot of the 5th harmonic NF magnitude which shows that at 250 Hz the log magnitude tends to -∞; σ is the damping ratio which determines the width of the notch; the closer it is to 0, the steeper the notch is. In this case σ around 0.05 gives a narrow notch most suitable for stopping the 5th harmonic.

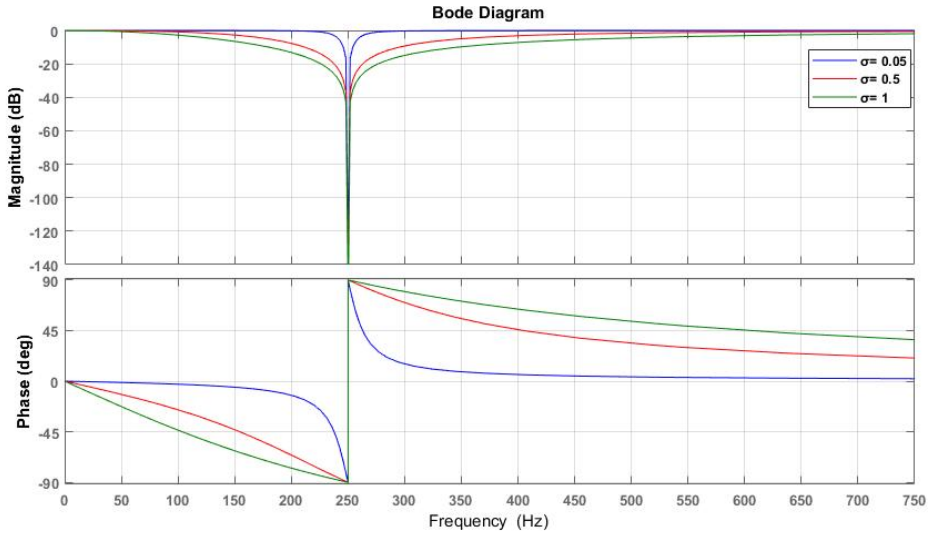
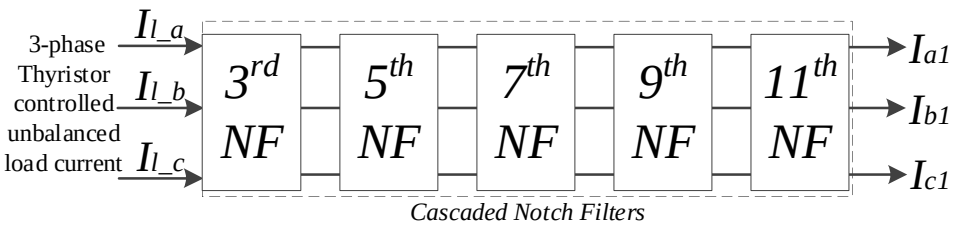
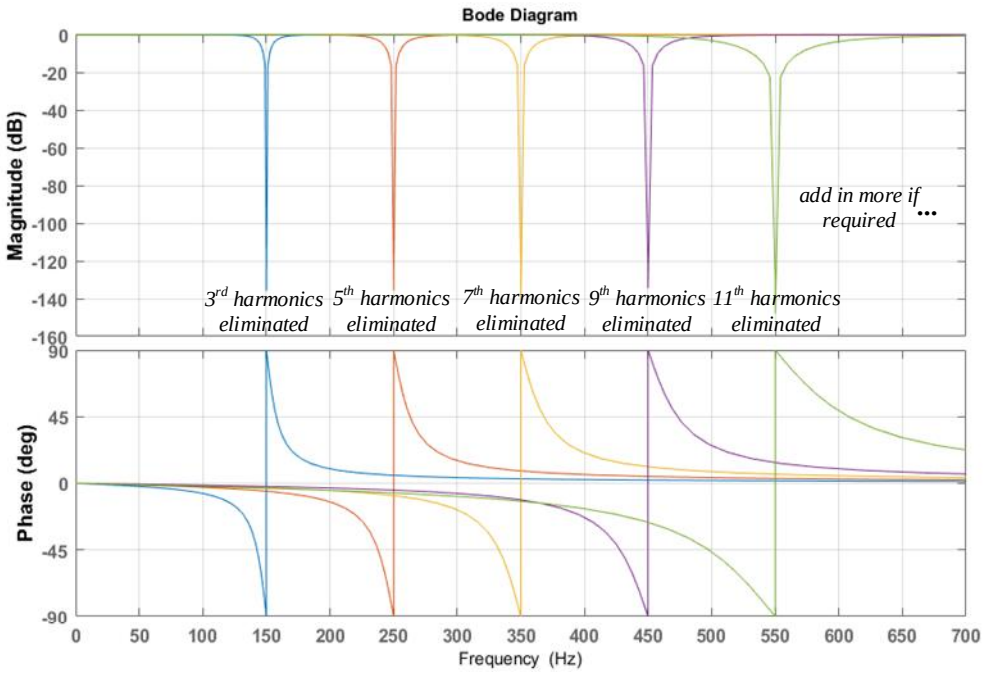


Fig. 4.10 NF bode plots

The analysis of the unbalanced fundamental and harmonic cases in Section 4.2 has shown that the 3rd, 5th, 7th, 9th and 11th are the most significant major harmonics which are required to be suppressed. In order to extract these harmonics simultaneously, five NFs with their corresponding ω_0 values can be connected in series, i.e. $\omega_0 = n \times 50 \times 2\pi, (n = 3,5,7,9,11)$, as shown in Fig. 4.11(a). The Bode plot of this cascaded NF is shown in Fig. 4.11(b). With such a NF this scheme provides the selectivity of harmonics elimination, which means in reality that the number of NFs can be flexibly adjusted according to the harmonic contents which are significant in the load current.



(a)



(b)

Fig. 4.11 (a) Cascaded NF block diagram and (b) corresponding NFs bode plot

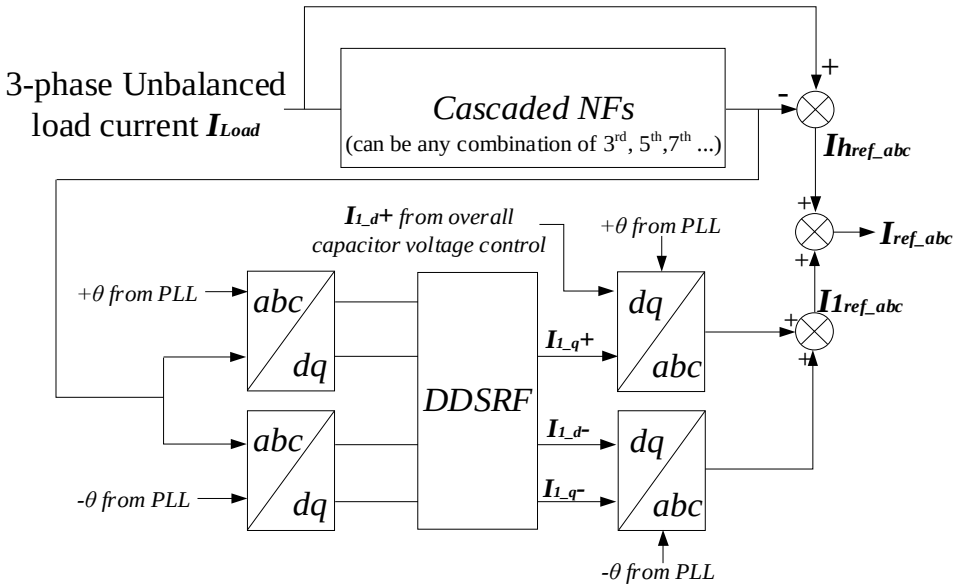


Fig. 4.12 NF-based harmonic extraction and reactive power compensation extraction scheme

The schematic diagram of this reference current extraction scheme is shown in Fig. 4.12. The load current being processed by the cascade-NF filter is subtracted from the original measured value so as to obtain the harmonic part of the reference current I_{href_abc}. To extract the fundamental reactive and negative sequence elements of the load current, the NF filtered current, which is mainly fundamental plus higher order harmonics with negligible amplitudes, needs to be further processed. This is by transforming it into +ve and –ve sequence *d-q* elements and eliminating the double frequency cross coupling terms using DDSRF, hence $I_{1\_d}^{+}$, $I_{1\_q}^{+}$, $I_{1\_d}^{-}$ and $I_{1\_q}^{-}$ are

obtained. Except, $I_{1\_d}^{+}$, the load real current component, all the other three elements form the fundamental part of the reference current. Again the reference current generated from the overall capacitor voltage control loop needs to be added into the overall reference current, for maintaining capacitor voltage balance. All fundamental elements are then transformed back to the *abc* stationary frame. The resultant I_{1ref_abc} are summed up with the I_{href_abc} and become the converter reference current signal I_{ref_abc}.

4.3.2.5 Comparison of two reference current extraction schemes

Comparing the NF-based scheme with the LPF-based scheme, the main advantages of the former are as follows:

- ***Higher speed in reference current elimination***: the NF-based scheme it can focus on a few lower-order major harmonics only. The lowest bandwidth is higher than for that of LPF. This reduces time delay between the original and extracted reference currents, hence enable the controller to eliminate harmonics fast;
- ***Flexible in harmonic element selection***: the NF-based scheme can adjust notch frequencies flexibly, according to the harmonics to be eliminated. For example, in Case A, triple harmonic and their multiples are absent, hence the 3rd and 9th NF filters can be removed from the NF block;
- ***Higher precision in harmonic extraction***: with the LPF-based scheme, the 3rd harmonic is transformed into 2nd harmonic via the Park transformation; but will not be eliminated by the DDSRF for decoupling +ve and –ve fundamental components, hence will not be extracted from the load current. This causes the harmonic extraction error. Using the NF scheme it can extract all the unwanted harmonics using *abc* frame directly, no *dq* transformation is applied, hence 3rd harmonic can be extracted.

Fig. 4.13 compares three-phase current waveforms and variations of their THDs in Case B after their harmonic elements are eliminated using the two different schemes respectively. It can be seen that the NF-based scheme (red) can extract the harmonics more accurately and faster than the LPF-based scheme (blue). This is particularly evident from 3-phase current THDs; at steady states the THDs from the NF scheme are lower showing it extracts higher percentages of harmonics than its counterpart. During transient states, when α changes from 0° to 30° and 30° to 60°, THDs due to the NF-based scheme change faster in response to the waveform changes and settle down quicker.

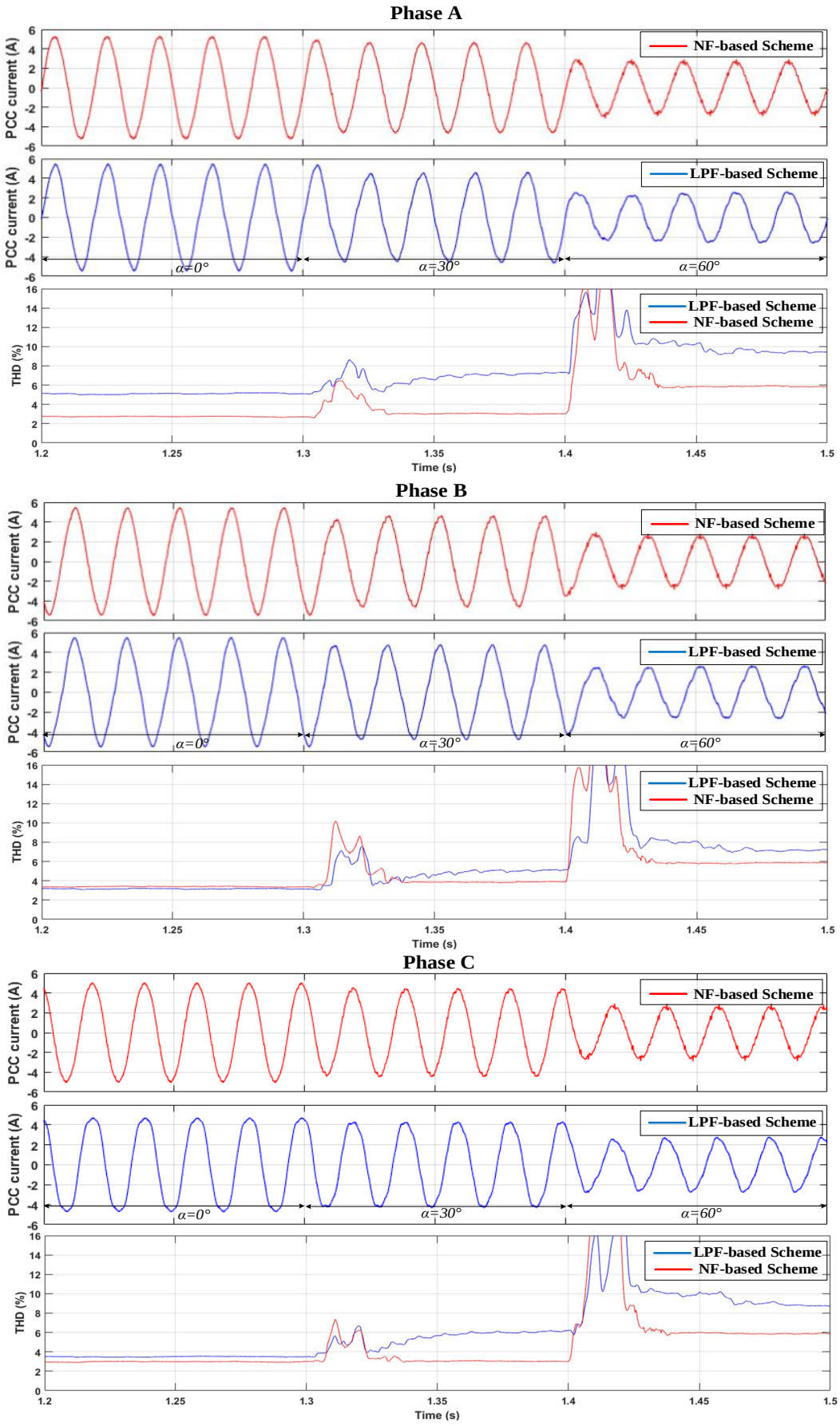


Fig. 4.13 Three phases compensated currents and their THD comparison under NF and LPF-based schemes

4.4 MMFCC-APC for Unbalanced Load Compensation

4.4.1 System configuration

The MMFCC-APC applied for the unbalanced load system operation has the same configuration as that used in the balanced application discussed in Chapter 3. The 5-level FC is still used as the submodule and two such submodules are connected in series per phase. The MMFCC three-phase limbs may be in either star (SSBC) or delta (SDBC) connection as shown in Fig. 4.14. It will be shown later that they have different performances in compensating unbalance and harmonics in load current.

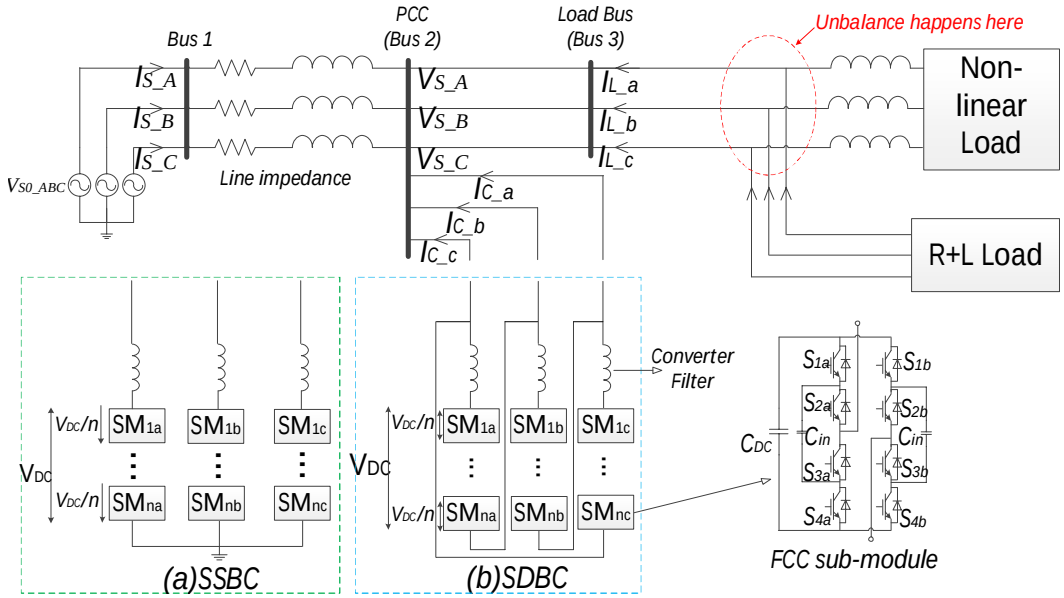


Fig. 4.14 3-phase MMFCC-APC system with (a) SSBC and (b) SDBC configuration

As illustrated in Fig. 4.14 Bus 1 is connected to a balanced three-phase AC voltage source representing the power grid; Bus 2 is the Point of Common Coupling (PCC), connected with the MMFCC-APC and a load bus. The load bus is supplying a three-phase thyrisor-controlled rectifier load representing the harmonic current generating source, and a balanced R-L load emulating a common inductive load. The load imbalance created corresponds to the cases illustrated in Section 4.2.

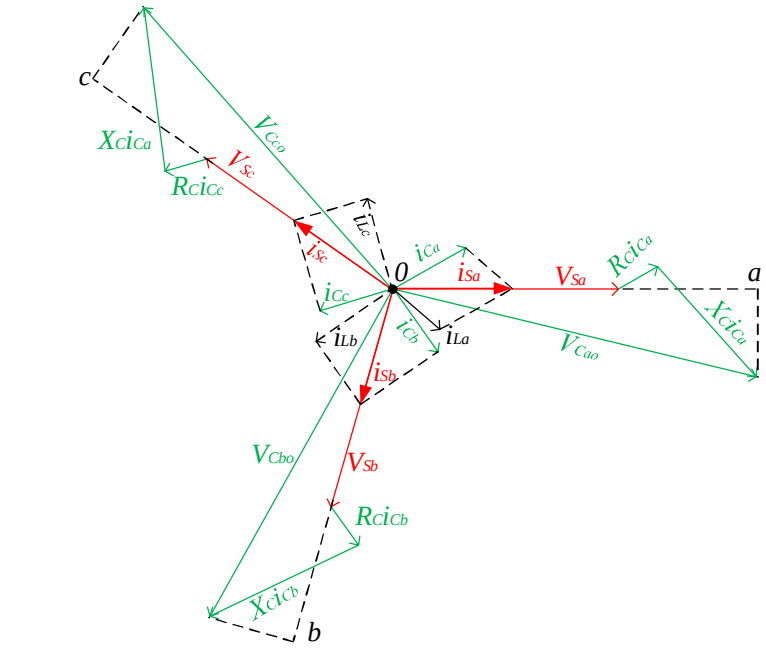
4.4.2 Operating principle

To ensure harmonic free and balanced current at the source end, the MMFCC-APC should supply a desired 3-phase compensating current to the PCC using one of the reference current extraction schemes described in section 4.3. Here the NF-based scheme is preferred. The current control scheme used follows the predictive plus derivative controller as that applied for balanced system operation discussed in Chapter 3.

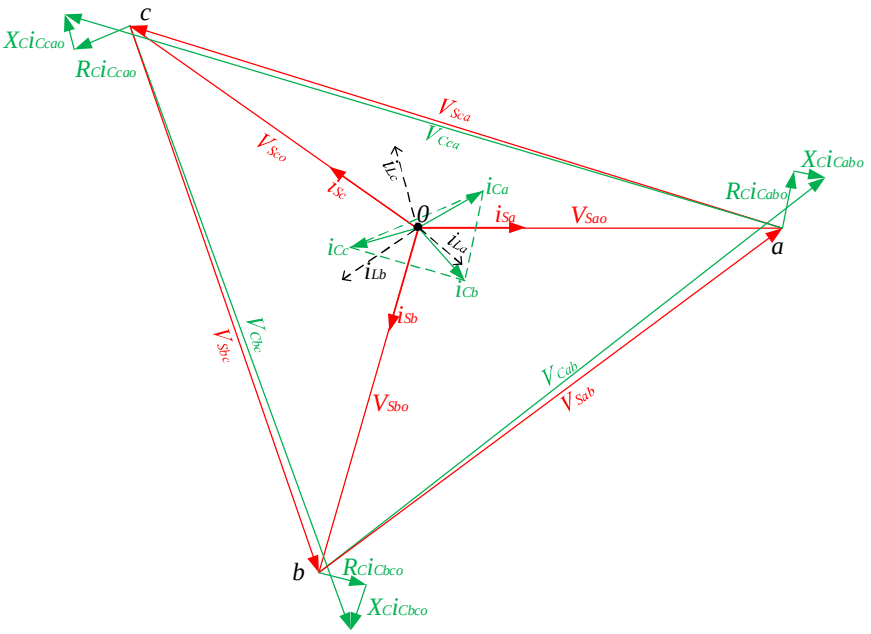
Figs. 4.15(a) and (b), respectively, shows the phasor diagrams for SSBC and SDBC configurations. The red lines represent source voltages V_{Sabc} and currents I_{Sabc}, black lines are for load currents I_{Sabc} which are unbalanced and lagging the source voltages. The green lines in the two figures are for converter currents I_{Cabc}, and voltage V_{Cabc} which are sum of the source voltage V_{Sabc} and voltage drops caused by the impedance

R_C and X_C between the converter and PCC lines. Assuming desired control is obtained the 3-phase source currents should ideally be balanced and in phase with the PCC voltages, as illustrated in the figures.

There is an issue specific to the MMCC-based APC or STATCOM when used to compensate unbalanced current in the network hence rebalancing the source current. That is that the process causes imbalanced power flowing between the MMFCC three phase clusters. This problem has been investigated by various researchers [107, 108]. The method developed is to use an additional DC voltage balancing control scheme named inter-cluster voltage control as discussed in the next section.



(a)



(b)

Fig. 4.15 phasor diagrams for 3-phase voltages and currents in controlled by MMCC-APC in (a) SSBC and (b) SDBC connection

4.5 Inter-cluster DC Voltage Balancing Control with Zero Sequence Component Injections

The MMFCC-based APC needs to overcome per phase DC-link voltage imbalance, the situation arises when the converter compensates unbalanced load current. This is caused by the stacked submodules of each phase having their DC sources isolated from each other, so no active power exchange between phases is possible. Consequently DC-link voltages may drift away from their rated levels, resulting in converter malfunction and leading to distorted currents injected into the grid, overstressing or even damaging the devices. The inter-cluster voltage control approach is designed to maintain the DC-link voltages of three phases being balanced. For an SSBC-MMCC the method injects a sinusoidal zero-sequence voltage in the converter neutral point. For an SDBC-MMCC a sinusoidal zero-sequence current is applied. Note that this differs from the intra-cluster capacitor voltage balance control discussed in Chapter 3 which overcomes unequal DC-link voltages between sub-modules within one phase.

4.5.1 Analysis of instantaneous phase power imbalance

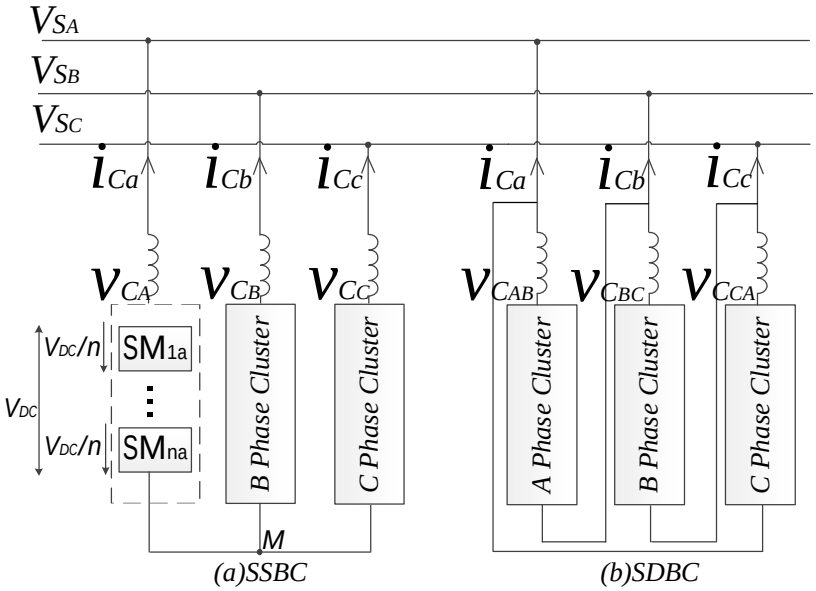


Fig. 4.16 Simplified configuration of (a) SSBC and (b) SDBC

The DC voltage imbalances between three phases are due to the MMFCC operating under unbalanced load condition, thus the average active power flowing through the converter three phase limbs are not zero. Analysis of the non-zero active power is shown below without taking into account the harmonics in the three phase currents. Considering the control method for MMCC-APC under unbalanced but harmonic free load, the phase voltages at the PCC and the currents from the converter phases to the grid are expressed respectively as

$$v_{Sm} = V_{s\_1}^{+} \sin\left(\omega t + \varphi_{Vp} - k * \frac{2}{3}\pi\right) + V_{s\_1}^{-} \sin\left(-\omega t + \varphi_{Vn} - k * \frac{2}{3}\pi\right) \quad (4.13)$$

$$i_{Cm} = I_{c\_1}^{+} \sin\left(\omega t + \varphi_{Ip} - k * \frac{2}{3}\pi\right) + I_{c\_1}^{-} \sin\left(-\omega t + \varphi_{In} - k * \frac{2}{3}\pi\right) \quad (4.14)$$

where k is 0, 1 and 2 and m represents phases A, B and C. $V_{s\_1}^{+}$ and $V_{s\_1}^{-}$ are the +ve and –ve sequence fundamental PCC voltage magnitudes, while $I_{c\_1}^{+}$ and $I_{c\_1}^{-}$ are the +ve and –ve sequence fundamental converter current magnitudes respectively. According to [109], the average active power thus can be calculated as

$$P_m = \frac{1}{2\pi}\int_0^{2\pi}(v_{Sm} i_{Cm})\, dt \tag{4.15}$$

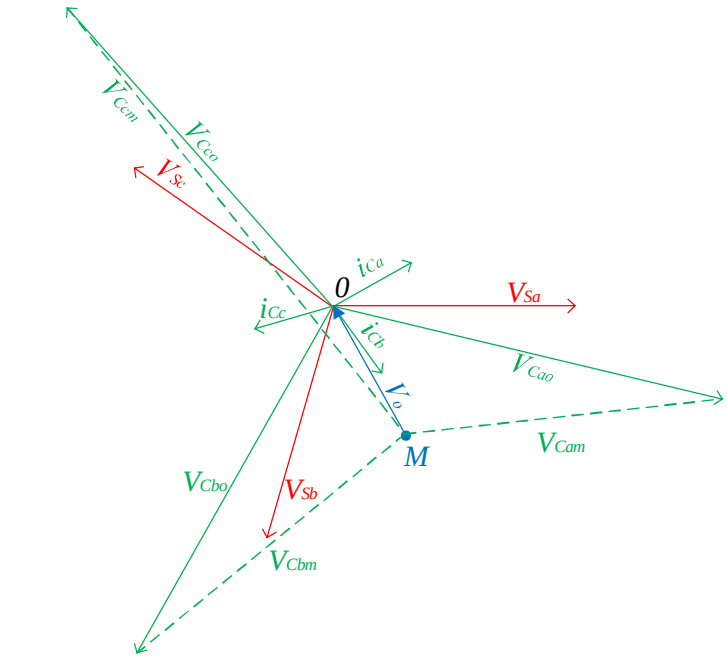
Hence the average active power flowing through the per phase limb can be expressed as

$$P_m = \frac{1}{2} * [\underbrace{V_{s\_1}^{+} I_{c\_1}^{+} \cos(\varphi_{Vp} - \varphi_{Ip}) + V_{s\_1}^{-} I_{c\_1}^{-} \cos(\varphi_{Vn} - \varphi_{In})}_{P_m^{++} \text{ and } P_m^{--}} \underbrace{-V_{s\_1}^{+} I_{c\_1}^{-} \cos\left(\varphi_{Vp} + \varphi_{In} + k * \frac{2}{3}\pi\right) - V_{s\_1}^{-} I_{c\_1}^{+} \cos\left(\varphi_{Vn} + \varphi_{Ip} + k * \frac{2}{3}\pi\right)}_{P_m^{+-} \text{ and } P_m^{-+}}] \tag{4.16}$$

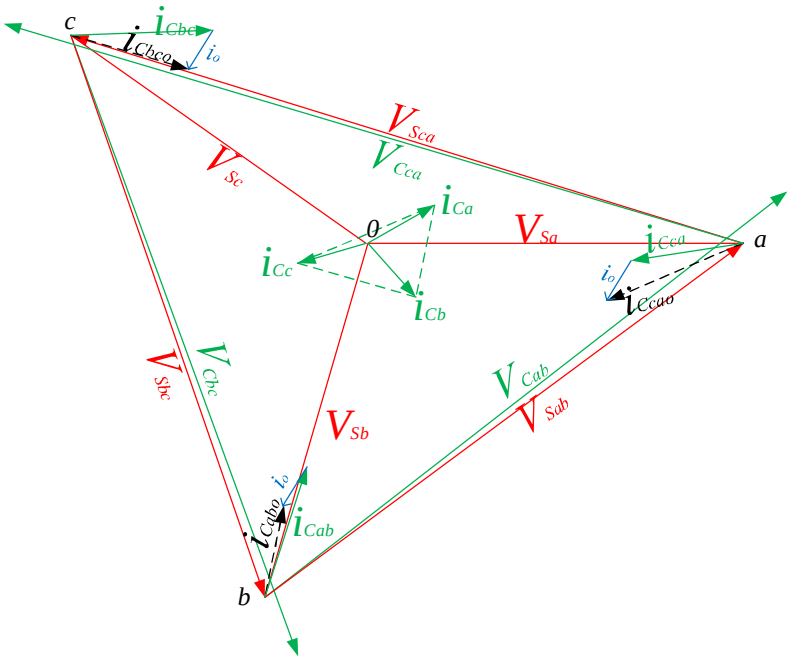
In the above equation, P_m^{++} and P_m^{--} are due to the products of +ve sequence voltage and current, and -ve sequence voltage and current, which are balanced, thus are summed to zero. P_m^{+-} and P_m^{-+} represent the cross products of +ve sequence voltage and -ve sequence current, and -ve sequence voltage and +ve sequence current. These two power terms are causing unequal power flow in the converter three phase limbs and resulting in the SM capacitor voltage drifting away from the nominal value.

4.5.2 Estimations of zero sequence components

To overcome this problem hence maintaining phase voltage balance, the inter-cluster balancing control scheme injects a common sinusoidal zero sequence voltage/current into the converter phase limbs. This intends to mitigate the two cross product terms P_m^{+-} and P_m^{-+}, but does not affect compensating current fed to the grid. For SSBC a zero sequence voltage v_o is injected, which is represented by the blue vector shown in Fig. 4.17 (a). Consequently, the initial converter voltages v_{cmo} (m=a, b, c) are changed to v_{cmM} with the neutral point shifting from *0* to *M*; For SDBC the injecting component is a zero sequence current, i_o, shown as blue vector in Fig. 4.17 (b). It circulates between converter three phase clusters, enabling power sharing between them but does not corrupt the current waveform injected into the grid. Analysis and derivations of voltage v_o and current i_o are detailed as below.



(a)



(b)

Fig. 4.17 3-phase voltage and current phasor diagram with (a) zero sequence voltage injection for SSBC and (b) zero sequence current injection for SDBC

A. For SSBC:

The instantaneous zero sequence voltage is: $v_o = V_o \sin(\omega t + \varphi_o)$ where ωt is the synchronous angle θ derived from PLL. Adding v_0 the SSBC per phase voltage can be derived as

$$v_{CmM} = v_{Sm} + v_o = V_{s\_1}^{+} \sin\left(\omega t + \varphi_{Vp} - k * \frac{2}{3}\pi\right) + V_{s\_1}^{-} \sin\left(-\omega t + \varphi_{Vn} - k * \frac{2}{3}\pi\right) + V_o \sin(\omega t + \varphi_o) \quad (4.17)$$

where *m*=**a**, **b**, **c**. Substituting v_{Sm} in Equation (4.15) by v_{CmM} above, the instantaneous active power can be re-calculated as $p_{Cm} = v_{CmM} i_{Cm}$. Excluding balanced active power terms P_m^{++} and P_m^{--} since they add to zero, the unbalanced power terms can be expressed as:

$$P_{Cm} = \frac{1}{2} * [P_m^{+-} + P_m^{-+} + \underbrace{V_o I_{c\_1}^{+} \cos\left(\varphi_o - \varphi_{Ip} + k * \frac{2}{3}\pi\right) - V_o I_{c\_1}^{-} \cos\left(\varphi_o + \varphi_{In} - k * \frac{2}{3}\pi\right)}_{P_{Cm}^{o+} \text{ and } P_{Cm}^{o-}}] \quad (4.18)$$

It is clear that an adequate evaluation of v_o can lead to last two power terms on the right hand side of Equation (4.18) cancel $P_m^{+-}$and P_m^{-+}, hence $P_{Cm} = \frac{1}{2}(P_m^{+-} + P_m^{-+} + P_{Cm}^{o+} + P_{Cm}^{o-})$ equals 0. Thus the zero sequence voltage magnitude and angle are derived given as

$$v_o = \frac{2P_{Ca} - X_{a3}}{\cos\varphi_o * X_{a1} + \sin\varphi_o * X_{a2}} \quad (4.19)$$

$$\varphi_o = \tan^{-1}\left(\frac{X_{a1}(2P_{Cb} - X_{b3}) - X_{b1}(2P_{Ca} - X_{a3})}{X_{b2}(2P_{Ca} - X_{a3}) - X_{a2}(2P_{Cb} - X_{b3})}\right) \quad (4.20)$$

Derivations of v_0 and φ_0 are given in Appendix B.3.

B. For SDBC:

Injecting zero sequence current $i_o = I_o \sin(\omega t + \varphi_o)$ into the MMFCC in SDBC, it circulates within the three phase clusters. Hence, the line voltage and cluster current for SDBC can be derived as

$$v_{Cm} = \sqrt{3}\left(V_{s\_1}^{+} \sin\left(\omega t + \varphi_{Vp} + \frac{\pi}{6} - k * \frac{2}{3}\pi\right) + V_{s\_1}^{-} \sin\left(-\omega t + \varphi_{Vn} + \frac{\pi}{6} - k * \frac{2}{3}\pi\right)\right) \quad (4.21)$$

$$i_{Cm0} = i_{Cm} + i_o = \frac{1}{\sqrt{3}}\left(I_{c\_1}^{+} \sin\left(\omega t + \varphi_{Ip} + \frac{\pi}{6} - k * \frac{2}{3}\pi\right) + I_{c\_1}^{-} \sin\left(-\omega t + \varphi_{In} + \frac{\pi}{6} - k * \frac{2}{3}\pi\right)\right) + I_o \sin(\omega t + \varphi_o) \quad (4.22)$$

where *m*=**ab**, **bc**, **ca**. The instantaneous active power can be re-calculated as $p_{Cm} = v_{Cm} i_{Cm0}$. Similarly, by ignoring the P_m^{++} and P_m^{--} the unbalanced power can be written as Equation (4.23) with zero sequence current injection.

$$P_{Cm} = \frac{1}{2} * [P_m^{+-} + P_m^{-+} + \underbrace{V_{s\_1}^{+} I_o \cos\left(\varphi_{Vp} + \frac{\pi}{6} - \varphi_o + k * \frac{2}{3}\pi\right) - V_{s\_1}^{-} I_o \cos\left(\varphi_{Vn} + \frac{\pi}{6} + \varphi_o - k * \frac{2}{3}\pi\right)}_{P_{Cm}^{o+} \text{ and } P_{Cm}^{o-}}] \quad (4.23)$$

Adequate magnitude and phase angle values for i_o given as

$$i_o = \frac{2P_{Ca} - X_{a3}}{\cos\varphi_o * X_{a1} + \sin\varphi_o * X_{a2}} \quad (4.24)$$

$$\varphi_o = \tan^{-1}\left(\frac{X_{a1}(2P_{Cb} - X_{b3}) - X_{b1}(2P_{Ca} - X_{a3})}{X_{b2}(2P_{Ca} - X_{a3}) - X_{a2}(2P_{Cb} - X_{b3})}\right) \quad (4.25)$$

should lead to terms P_m^{o+}, P_m^{o-} canceling $(P_m^{+-} + P_m^{-+})$ in Equation (4.23) hence achieving phase cluster voltage balance.

The instantaneous zero sequence current needs to be converted into voltage command v_{com} through a proportional gain, as shown in (4.26).

$$v_{com} = K_{Pio}\left[-\frac{(i_{ab}+i_{bc}+i_{ca})}{3} + I_o \sin(\omega t + \varphi_o)\right] \quad (4.26)$$

4.5.3 Implementation of inter-cluster voltage balance control

This is illustrated by the block diagram shown in Fig. 4.18. This comprises two parts; computation of unbalanced powers due to $(P_m^{+-} + P_m^{-+})$ according to Equations (4.18) and (4.23) and evaluation of compensating power from the measured phase limb SM capacitor voltages. Using the combined results the zero sequence voltage v_o for SSBC can be calculated by Equations (4.19) and (4.20). If it is for SDBC the zero sequence current i_o is evaluated by Equations (4.24) and (4.25). The resultant compensating voltage v_{com} is then applied as a part of the reference voltage to control the converter switches.

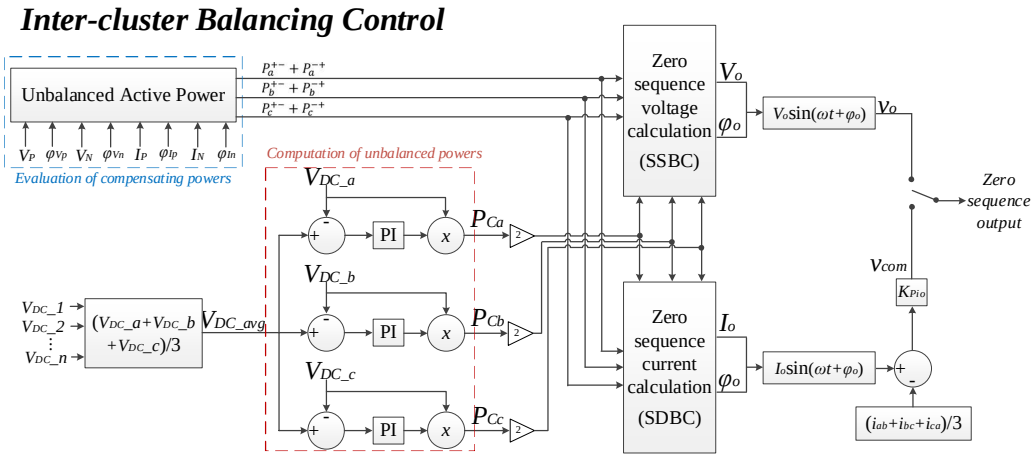


Fig. 4.18 Block diagram of Inter-cluster voltage Balancing control

4.6 Overall Control Schematic

The MMFCC-APC overall control schematic for load unbalanced system operation is shown in Fig. 4.19. There are three essential parts;

- the reference current extraction and current feedback control part,
- the inter-cluster voltage balance control part described in the previous sub-section and
- intra-cluster capacitor voltage control part.

The Notch Filter-based reference current extraction is used so that the MMFCC is capable to compensate the unbalanced source current and eliminate a few dominant harmonics. The extracted reference current is fed into the current control block, as will be described in the next subsection. The intra-cluster capacitor voltage control and Carrier Permutation PS-PWM are necessary for maintaining submodule capacitor voltages equal.

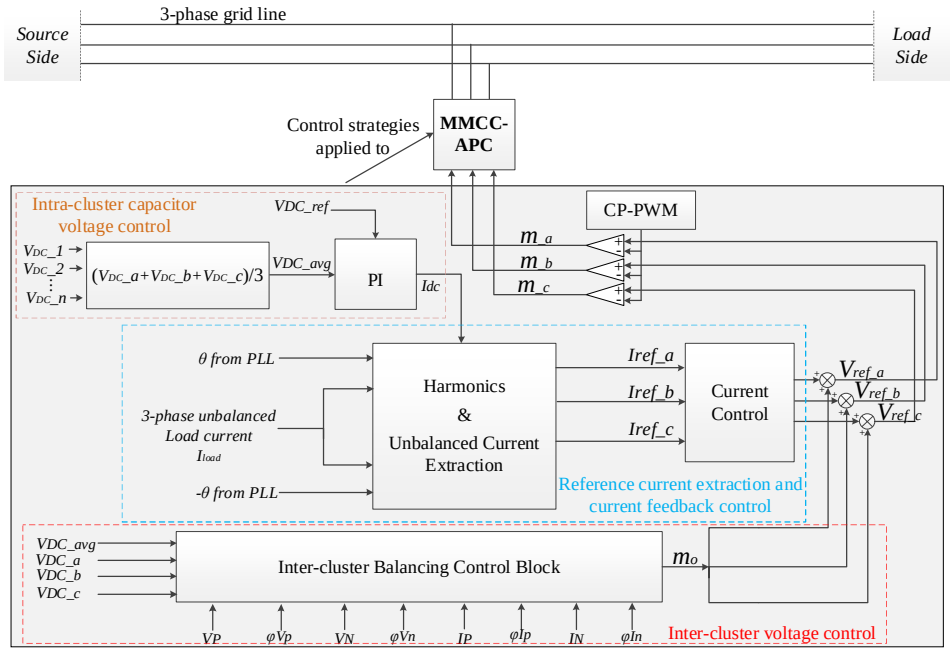


Fig. 4.19 Blocks diagram of overall control scheme

4.6.1 Current control using predictive controller with derivative action

As been stated previously the current controller, as shown in Fig. 4. 20, here adopts the same predictive control plus derivative action as the one used in the balanced harmonic compensation case presented in Chapter 3. The only difference is that the control algorithm is applied to control three-phase sinusoidal currents individually, rather than their equivalent *d-q* elements. The benefit of this approach is that it avoids converting the measured converter current i_{c_abc} to its equivalent *d-q* form, which encounters +ve and –ve sequence elements double frequency cross coupling terms. The feedback i_{c_abc} is distorted and unbalanced since the converter's functions are cancelling the harmonics and –ve sequence current elements in the load current. Application of the predictive controller to three phase currents separately using directly the feedback converter three phase current i_{c_abc} ensures accurate control and reduces computational procedure.

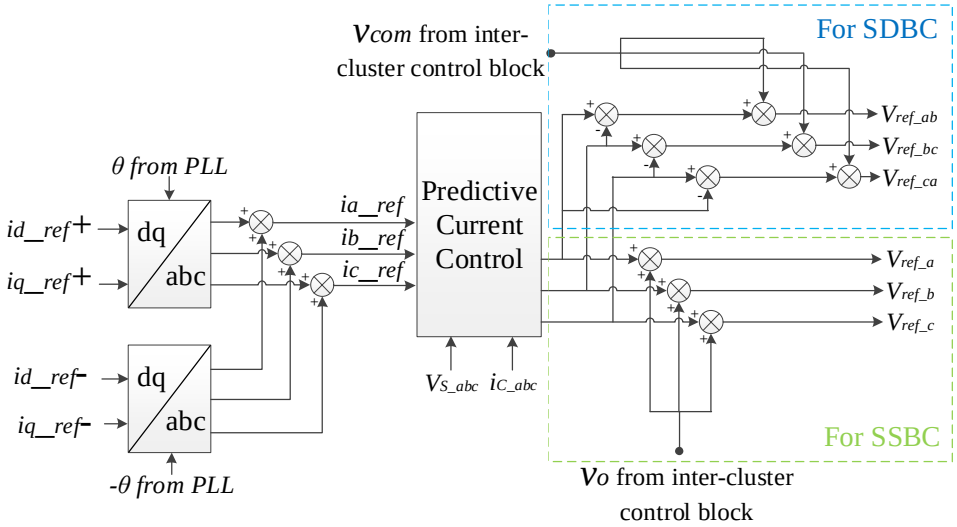


Fig. 4.20 Predictive current control block diagram

To calculate three phase converter reference voltages, Equation (3.8) given in Chapter 3 is used. For SDBC, the R_c and L_c in this equation are replaced by $\frac{R_c}{3}$ and $\frac{L_c}{3}$ respectively. The reference voltages calculated, are summed with zero sequence components and applied to the PWM block.

4.7 Simulation Study

The proposed system as shown in Fig. 4.14 and its corresponding control schemes are verified through SIMULINK/MATLAB. The parameters used in the simulated system are listed in Table 4.5; Three-phase voltage rating at PCC is 110V, 3.3KVA, 50Hz; the MMFCC contains two SMs in each phase, while the module capacitor per SM is 50V for SSBC and 60V for SDBC. The levels of harmonics in the load current are varied by changing the firing angle $\boldsymbol{\alpha}$ of the 3-phase thyristor rectifier. The R+L load is chosen to have a power factor of 0.8.

A fixed value resistor is inserted in phase A line to create the load current imbalance. It is worth noting to measure the degree (level) of current imbalance a parameter $K_{ir} = \frac{I_1^-}{I_1^+}$ is defined, where $I_1^-$is the -ve sequence fundamental component and I_1^+ is the +ve fundamental sequence. When $I_1^- = 0$, $K_{ir} = 0$, the current is balanced; on the other hand, when K_{ir}=1, or 100%, I_1^-=I_1^+ and the current is severely unbalanced.

In this simulation study K_{ir} varies from 0.4 to 0.7 in order to measure the APC operating ranges and compare the performance differences between APC with SSBC and SDBC configurations. It will be shown that excessive levels of load imbalance would lead to the MMFCC working in over-modulation mode and hence not be able to function properly.

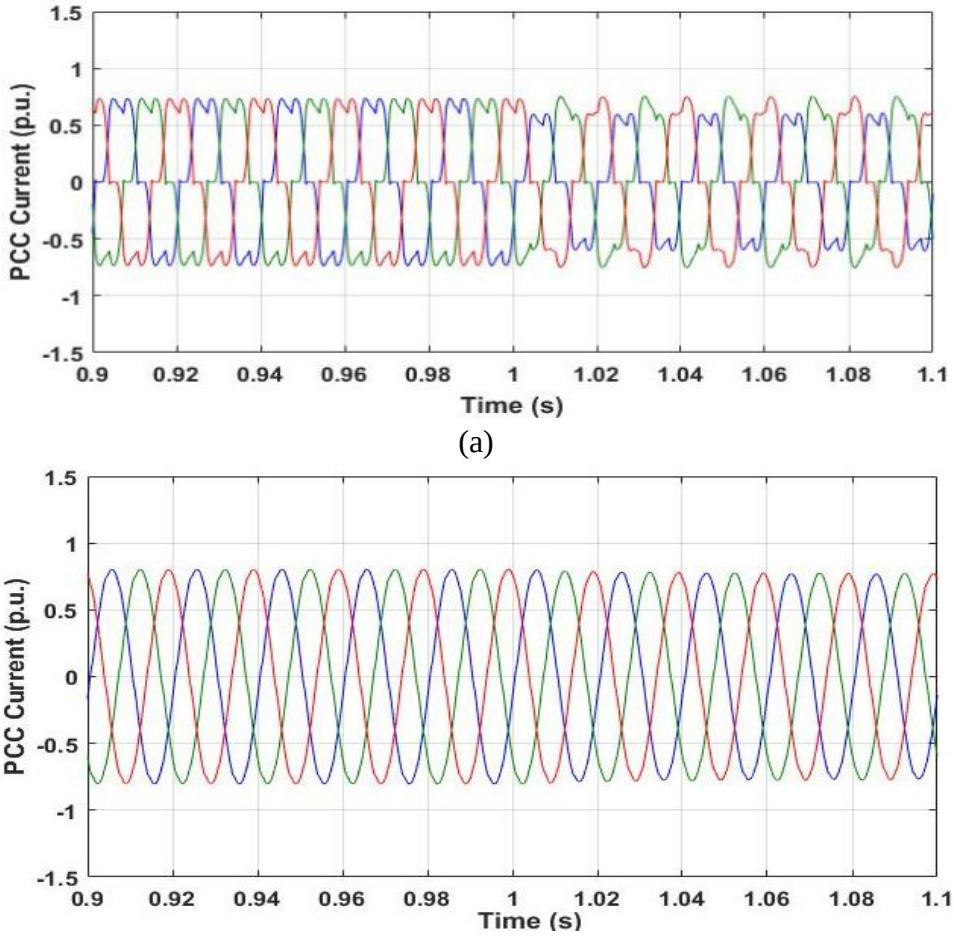
Table 4.5 MMFCC-APC system parameters

Components		**Value**
PCC Side	Source end voltage V_{S0}	60 V
Distribution Line	Aluminium PI TX line (d= 10mm, l=1.1km)	R_{line} = 0.2 Ω L_{line} = 3mH
Load Side	3-Phase Thyristor Rectifier	R_{dc_r} = 20Ω L_{ac_r} = 8.3mH
	Firing angle α	0°; 30°; 60°
	R+L Load	R_l = 10Ω L_l = 48mH
	Extra resistor on Phase A	R=5Ω
Converter Side	RL Filter	R_c = 1.59Ω L_c = 2mH
	DC capacitor	C_{DC}= 1.12 mF
	DC voltage V_{dc} in each sub-module	50 V (SSBC)
		60V (SDBC)
	Switching frequency f_s	1 kHZ

4.7.1 Simulation results

4.7.1.1 PCC source current and APC compensating current waveforms

Fig. 4.21 shows the 3-phase source current waveforms at PCC without and with MMFCC-APC control applied. The load current is initially balanced with the firing angle to rectifier α=0°. At 1.0 sec. load current imbalance is imposed and the level of unbalance K_{ir}= 0.36. The current waveforms, without compensation, are shown in (a) and those in (b) are the PCC current due to MMFCC-APC compensation, which are perfectly balanced and sinusoidal.



(a)

(b)

Fig. 4.21 Three-phase PCC current (a) without MMFCC-APC compensation and (b) with MMFCC-APC compensation
(Phase A: blue, Phase B: green, Phase C: red)

Fig. 4.22 shows the corresponding APC 3-phase compensating current waveforms. Initially from 0.9 to 1.0sec, the load is balanced hence APC compensates harmonic current and reactive power only; when load imbalance is imposed at 1.0sec, APC reacts to balance the current at the source end as well, thus its compensating currents become unbalanced.

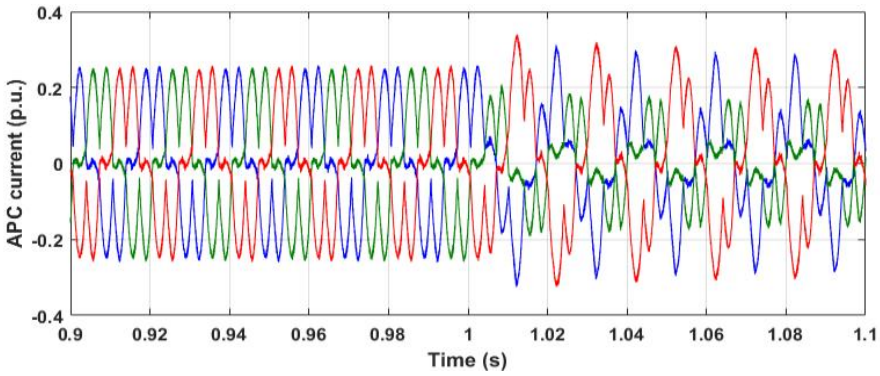
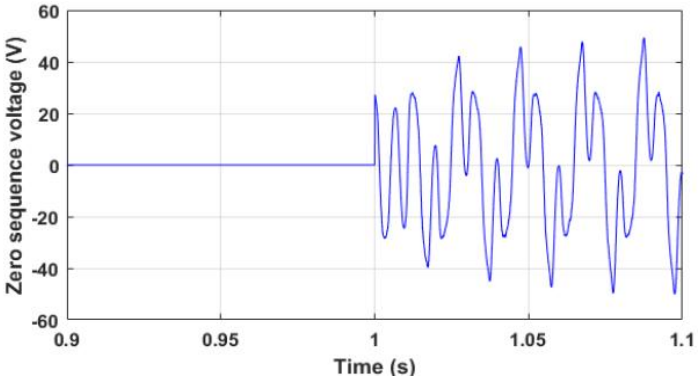


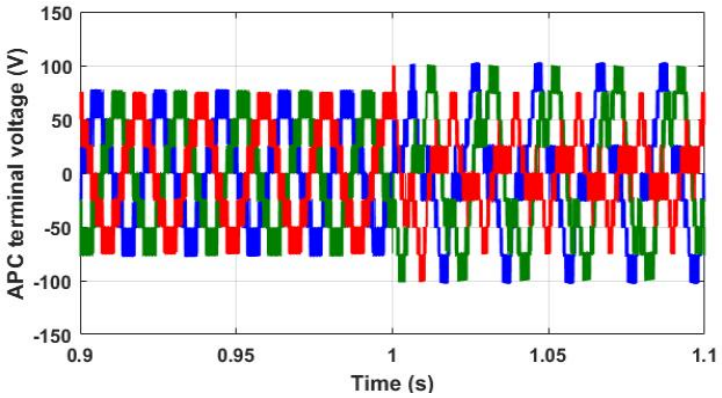
Fig. 4.22 APC current response

4.7.1.2 Star-connected MMFCC (SSBC)

Fig. 4.23 shows the injected zero sequence voltage and MMFCC terminal voltages when in SSBC configuration. It can be seen that the amplitude of zero sequence voltage waveform in Fig. 4.23(a) is high (nearly 50V) compared to the rated PCC voltage, when in unbalanced load operation from 1.0sec. It is important to note that v_o injected in each phase will be cancelled at grid line-line voltages. The PWM modulated MMFCC 3-phase terminal voltage is shown in Fig. 4.23(b). Clearly the reference phase voltages under unbalanced load current condition are unbalanced in order to maintain the source current at PCC being balanced. With zero sequence voltage added, phase A voltage magnitude is the highest, reaching nearly 100V whilst phase C is the lowest.



(a)

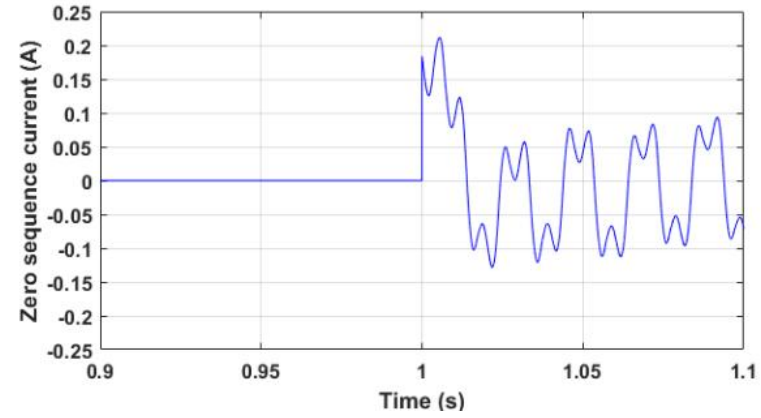


(b)

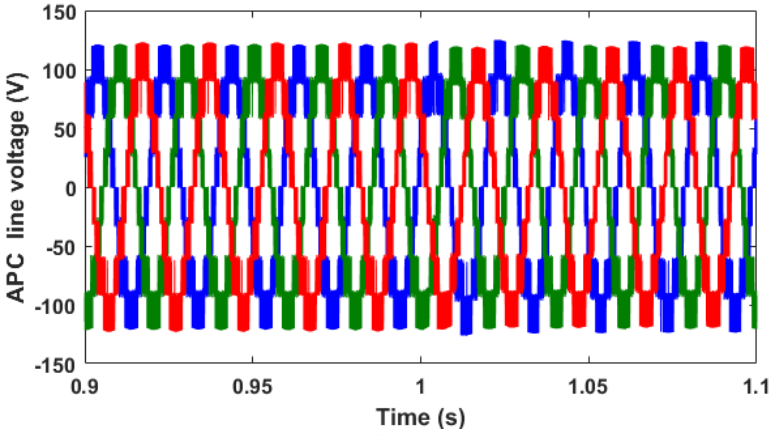
Fig. 4.23 (a) Zero sequence voltage and (b) three-phase terminal voltages for **SSBC** (Phase A: blue, Phase B: green, Phase C: red)

4.7.1.3 Delta-connected MMFCC (SDBC)

For this connection, the injecting component is zero sequence current, as shown in Fig. 4.24(a). The waveform is also distorted due to the harmonics compensation, but it will only circulating within the converter phases to ensure the cluster active power balanced and has no effect on the grid current. The PWM modulated MMFCC 3-phase line voltage for SDBC is shown in Fig. 4.24(b), which is balanced and shows 9 voltage levels distinct from peak to peak.



(a)



(b)

Fig. 4.24 (a) Zero sequence current and (b) three-phase line voltage for **SDBC** (Phase A: blue, Phase B: green, Phase C: red)

4.7.2 Compensation performance comparisons

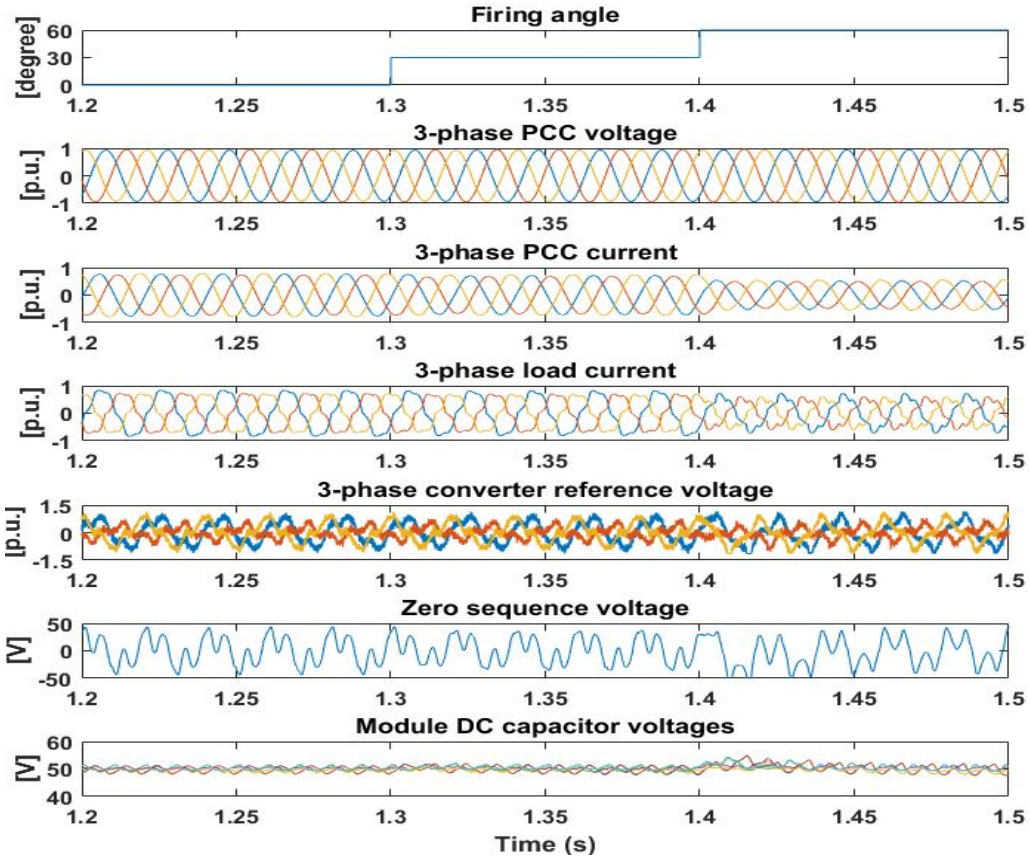
4.7.2.1 Load current having balanced harmonics + unbalanced fundamental (Case A):

Performance comparisons are carried out for MMFCC-APC in SSBC and SDBC. The firing angle of the rectifier load is set to 0° initially and changes to 30° at 1.3 sec. then 60° at 1.4 sec. The load imbalance is set to give K_{ir}= 0.4. Voltage and current waveforms for both connections are shown respectively in Fig. 4.25 (a) and (b), and they demonstrate that both connections are working in terms of eliminating harmonics and rebalance current at source side. However SDBC connection performs better in general than SSBC. This can be seen from the converter three-phase terminal voltages, for SSBC they are unbalanced and the maximum value is higher than that for SDBC. The THD values of source side three-phase current due to both SSBC and SDBC are also compared. These are listed in Table 4.6 for different load firing angles, and also illustrated using bar chart depicted in Fig. 4.27. They show that in general SSBC results in higher THDs due to higher distortion of converter terminal voltage, hence poorer performance in harmonic elimination than its counterpart. The differences between the SSBC and SDBC in THD values increase as the load firing angle α increases.

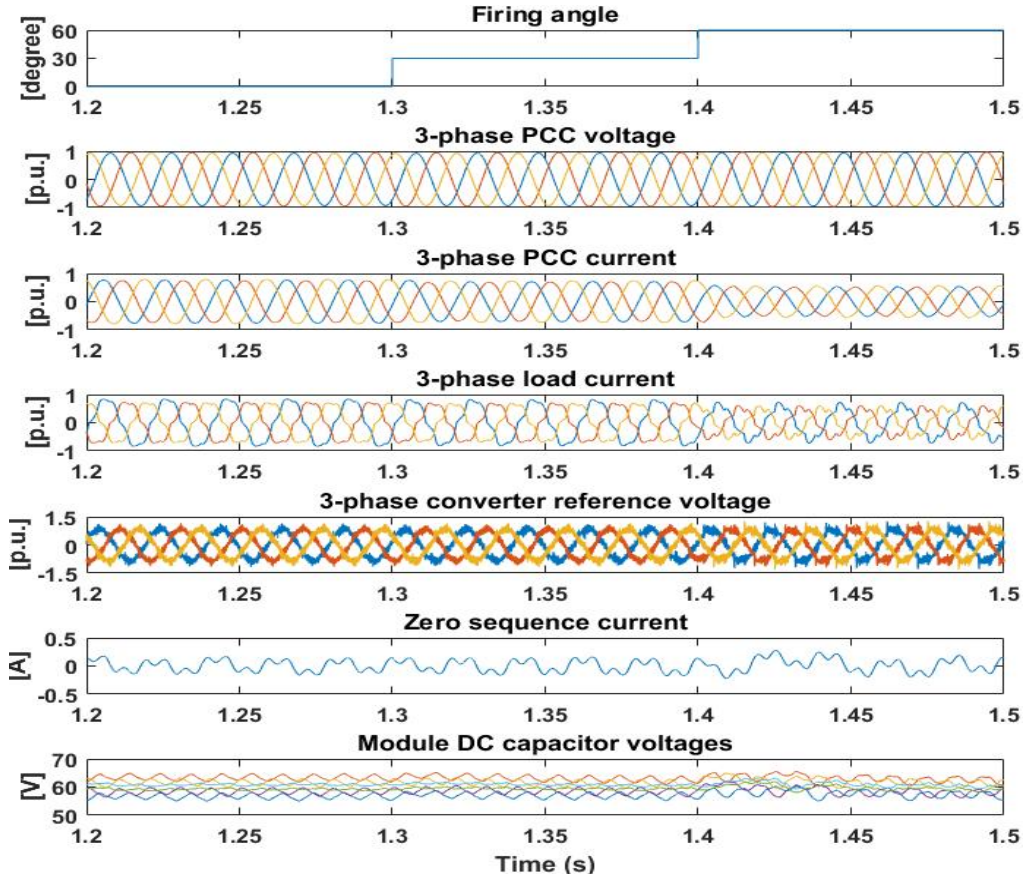
4.7.2.2 Load current having unbalanced harmonics + unbalanced fundamental (Case B&C):

When both harmonics and fundamental element in the load current are unbalanced, the voltages and current waveforms collected under the control of MMFCC-APC in either SSBC or SDBC are as shown in Figs. 4.24 (a) and (b) respectively. The levels of load current harmonics increase and the shapes of three-phase load current waveforms also deteriorate with the firing angle changing from 0° to 60°. Nevertheless with MMFCC-APC in action, in either SSBC or SDBC, the 3-phase source currents at PCC are all well balanced and with very low harmonic distortion. Only the converter reference voltages are shown differences; for SSBC three phase voltages are severely distorted and unbalanced, whilst that for SDBC are balanced with low levels harmonic distortion. The module capacitor voltages in both configurations are maintained at their nominal values.

There are also differences in the THDs of the source currents after harmonics extraction as shown in Table 4.7 and Fig. 4.28. When the firing angle is 0°, the level of harmonic distortion is low, current THDs for both SSBC and SDBC are comparable. However with the firing angle increased to 60°, the 3-phase source currents with SDBC operation have lower THDs comparing that from using SSBC operation.

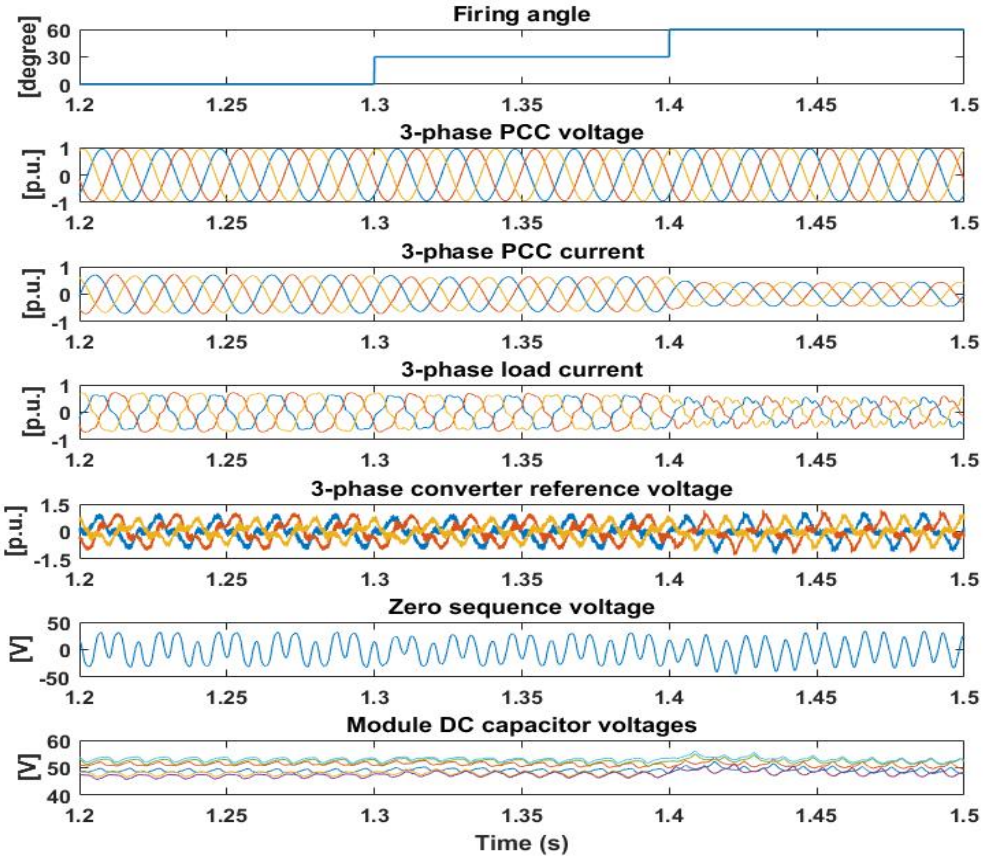


(a)

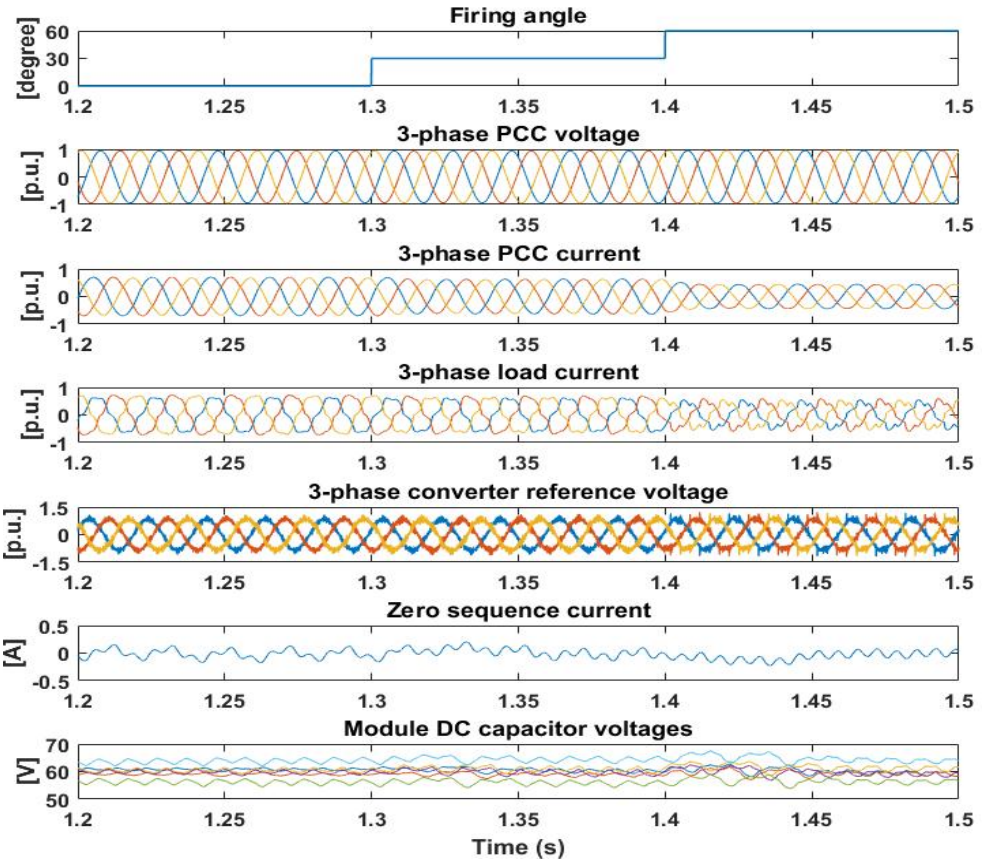


(b)

Fig. 4.25 Harmonic elimination performance of (a) **SSBC-APC** (b) **SDBC-APC** for Case A



(a)



(b)

Fig. 4.26 Harmonic elimination performance of (a) **SSBC-APC** (b) **SDBC-APC** for Case B

Table 4.6 The THDs of the 3-phase source current for Case A
(Phase A: blue, Phase B: red, Phase C: yellow)

Firing angle α	0°	30°	60°
SSBC	1.69%	2.09%	3.05%
	1.91%	2.17%	3.39%
	1.75%	2.11%	3.11%
SDBC	1.46%	1.86%	2.55%
	1.56%	1.87%	2.72%
	1.51%	1.85%	2.62%

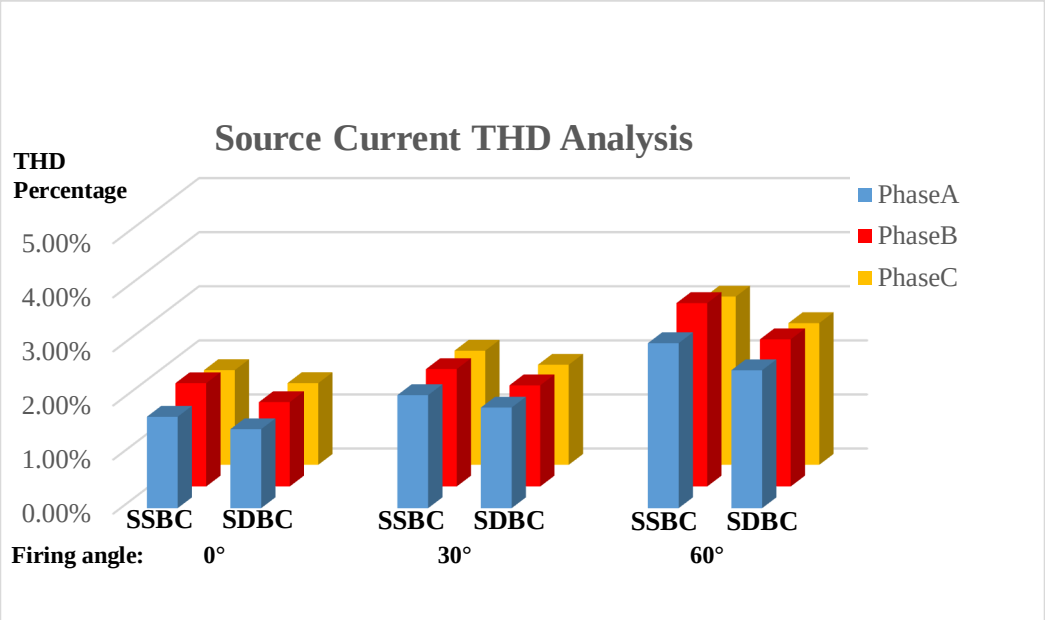


Fig. 4.27 The THDs of the 3-phase source current for Case A

Table 4.7 The THDs of the 3-phase source current for Case B

(Phase A: blue, Phase B: red, Phase C: yellow)

Firing angle α	0°	30°	60°
SSBC	2.86%	2.43%	2.51%
	2.68%	2.80%	2.97%
	2.10%	2.43%	3.05%
SDBC	2.83%	2.42%	1.93%
	2.44%	2.27%	2.25%
	2.15%	2.07%	2.49%

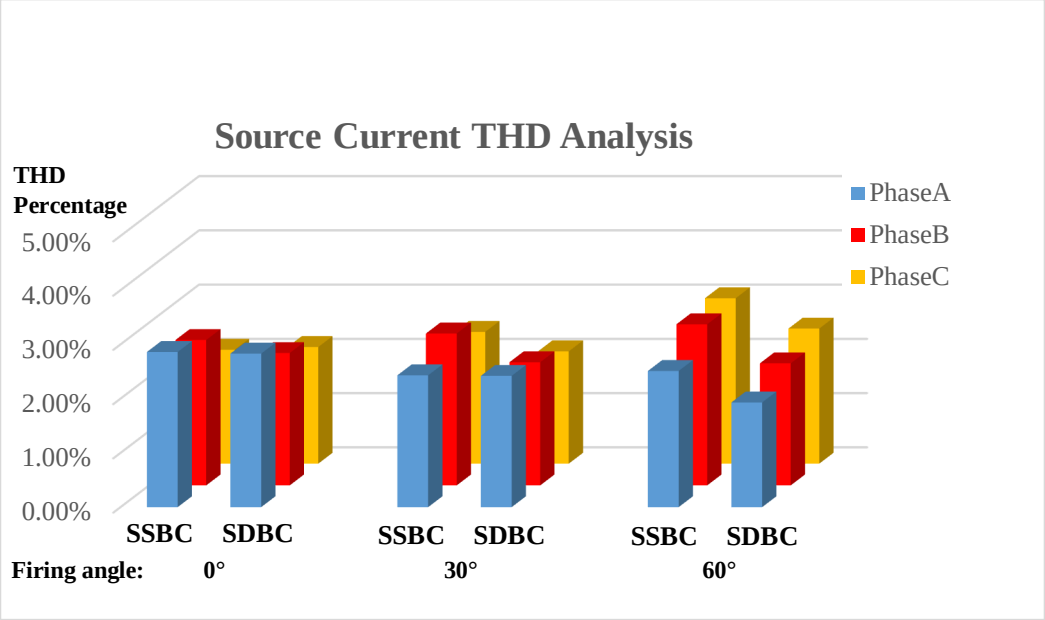


Fig. 4.28 The THDs of the 3-phase source current for Case B

4.7.3 Load current with increased levels of imbalance

The operation ranges of the MMFCC-APC in SSBC and SDBC are compared under the conditions of variable degrees of load current imbalance. A higher level of imbalance, measured by K_{ir}, would need an increased zero sequence component to rebalance the converter phase cluster active power, this may consequently, push the converter voltage/current over their rating limits, leading to converter malfunction.

Table 4.8 Resistor values and corresponding K_{ir}

R	***K*ir**
9.5 Ω	0.4
12.5 Ω	0.5
17.5 Ω	0.6
21.5 Ω	0.7

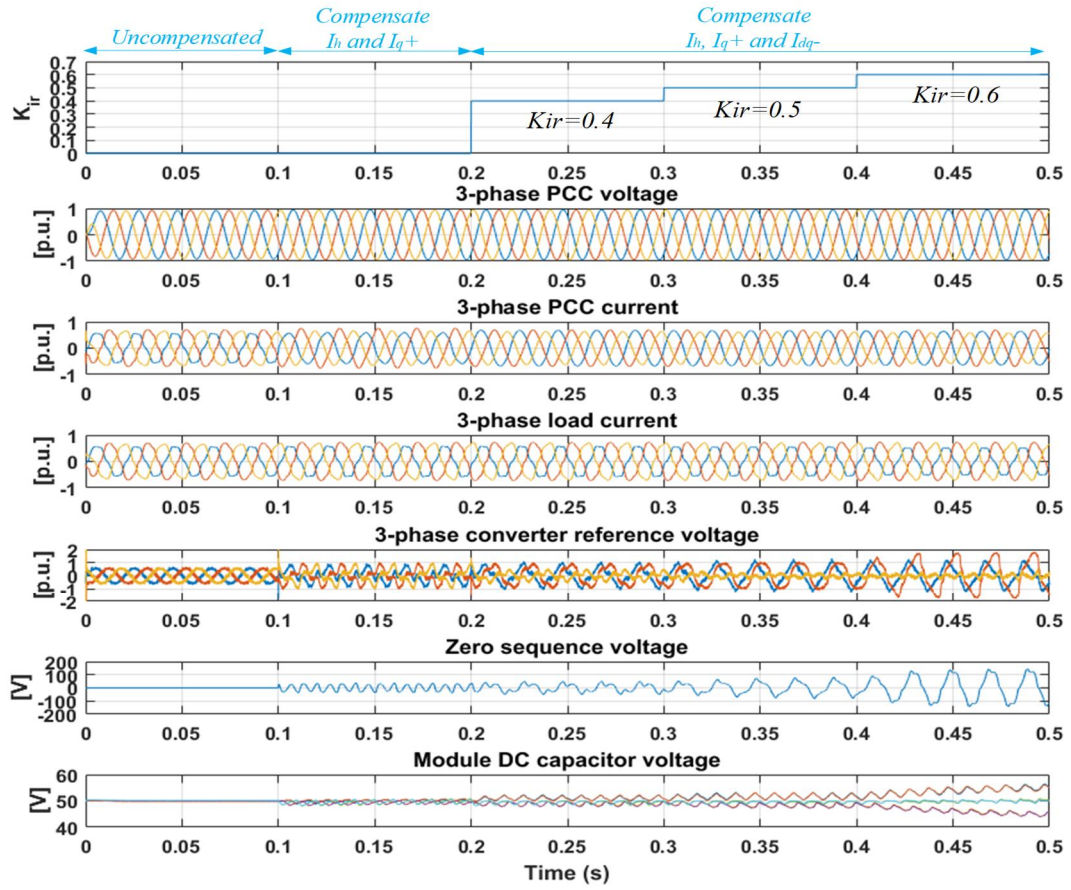
In this simulation, the degree of imbalance is set by connecting different resistors as listed in Table 4.8 to the thyristor load phase A, hence K_{ir} changes in step from 0 to 0.6 and 0.7. The firing angle α is maintained to 0° throughout. Fig. 4.29(a) and (b) show all V/I waveforms obtained for SSBC and SDBC-APC respectively.

As can be seen in Fig. 4.29(a) for SSBC, between 0< t <0.1sec APC is not in action, the PCC current waveforms are unbalanced and not in phase with the voltage. From t >0.1 sec, APC is turned on to perform reactive current compensation and harmonic elimination, resulting in the PCC current being in phase with the PCC voltage and sinusoidal, but phase currents are still unbalanced. In this case the converter three reference voltages are increased and distorted, but with near equal magnitudes. From t>0.2sec, the device is set to supply load required reactive current, eliminate

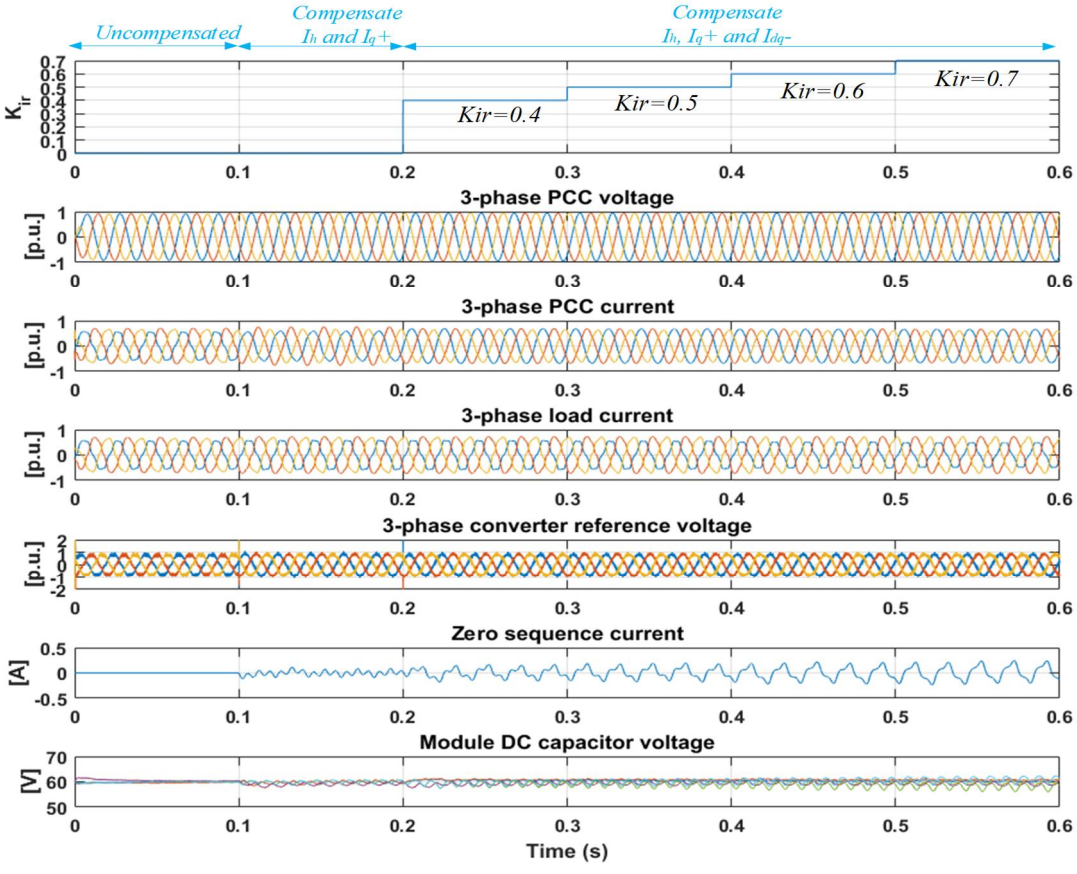
harmonics as well as rebalancing the 3-phase current. During 0.2<t<0.4sec when K_{ir} changes from 0.4 to 0.5, the PCC current is shown to be balanced and sinusoidal. The converter reference voltage is naturally increased and unbalanced. The zero sequence voltage is now increased and 6 module DC voltages are maintained balanced. Further increase Kir to 0.6, the controller's capability in compensating unbalanced current reaches its limit. This can be seen from the converter phase reference voltages which are severely unbalanced and the maximum phase B voltage is nearly twice the rated value. The three-phase source PCC current can no longer be maintained balanced, and some DC capacitor voltages cannot be controlled, they drift away from their nominal value. The high phase B voltage is due to high zero sequence voltage value, in this case the ratio is $(v_{conv}*+v_o)/(2\times V_{DC})>1$, converter is in over-modulation mode.

In contrast, the SDBC has an extended operating range, i.e. it can operate under higher levels of load imbalance. As shown in Fig. 4.29(b), when K_{ir} increases to 0.7, the PCC current is still maintained balanced and sinusoidal. The converter's 6 submodule DC capacitor voltages are controlled within 10% of the nominal value. The converter terminal reference voltages are balanced and the zero sequence current are below the rated level. Thus, the superiorities of the SDBC over SSBC are evident and can be summarised as follows:

- Better performance in harmonic elimination; this has been demonstrated using different levels of load current harmonics by increasing thyristor firing angle. The source current THDs due to MMFCC-SDBC control always give lower value comparing with SSBC operation.
- Higher capability in load current imbalance control; this has been demonstrated above, the SDBC can maintain source current balanced despite the high level of load current imbalance.



(a)



(b)

Fig. 4.29 Operating behaviour of (a) **SSBC-APC** (b) **SDBC-APC**

4.8 Summary

The chapter presented the application of the MMFCC-APC for simultaneously compensating load required reactive power, eliminating load current harmonics and rebalancing load current at the supply end. A new reference current extraction scheme was proposed which uses cascaded notch filters to eliminate only a selection of dominant low order harmonics in the load current. The method has been shown to have higher speed in tracking the harmonic variations and higher accuracy compared to its low-pass filter counterpart. The complete control strategy for an MMFCC-APC in both SSBC and SDBC connections was described. The inter-cluster voltage balance issue due to phase power imbalance caused by compensating unbalanced load current was explained. It has been shown that for an SSBC-based APC a zero sequence voltage was required to be added to phase limbs and for a delta-connected (SDBC) APC a zero sequence current was necessary to overcome the problem. The performance of these two types of APCs has been studied and compared via simulation. The results have shown that in terms of harmonic elimination SDBC is more effective in cancelling harmonic elements resulting in source current having lower THDs than that from SSBC. The study has also revealed that the SDBC has an extended range in unbalanced load compensation. In the studied example it was able to operate normally when the level of load imbalance K_{ir} reaches 0.7; in contrast the SSBC could not perform properly when K_{ir} is 0.6. Under severely unbalanced conditions the magnitude of zero sequence voltage could be higher than the rated phase voltage value pushing the phase voltage over its rating limit, causing converter to work in over-modulated mode and thus malfunction.

Chapter 5 Experimental MMFCC-APC

5.1 Introduction

The control schemes developed and presented in the previous chapters require experimental validation. This chapter describes the use of a scaled-down experimental MMFCC built by previous researchers [110-113] in the School of Electronic and Electrical Engineering, University of Leeds to function as an active power conditioner. A brief description of the hardware rig together with its measurement and DSP and FPGA-based control units will be given. A software program for controlling the MMFCC implemented by DSP was developed by the author, and this will be explained in detail. The experimental results for the MMFCC in both star and delta connections are presented and analysed.

5.2 Experimental System Hardware

5.2.1 Overview

A block diagram of the complete MMFCC hardware layout is shown in Fig. 5.1. It comprises the following five parts: the MMFCC circuit consisting of six sub-modules; the digital control unit which contains the Digital Signal Processor (DSP) and Field Programmable Gate Array (FPGA); the measurement and power supply units.

The configuration of the MMFCC power circuit is as shown in Fig. 5.2. There are six submodules, two per phase. A modular approach has been applied in building this submodule circuitry; i.e each of the submodules is constructed using 4 half H-bridge converter circuits called cell cards as shown in the left-hand-side of Fig. 5.2. Linking two such cards in series forms a half-bridge 3-level flying capacitor converter circuit, and wiring two such FC circuits in parallel to share one DC-source forms a full-bridge 5-level FC sub-module as shown in Fig. 5.3. The benefits for such a construction are clear, i.e. ease of circuit testing, debugging and maintenance. There are altogether 24 such cell cards for the MMFCC constructed.

The measurement unit contains 9 AC voltage transducers (LEM LV 25-P) with a conversion ratio 1:2.5 [114]. These are grouped in three to measure respectively source, load and converter side three-phase voltages. 9 AC current transducers (LEM LA 55-P) with a conversion ratio of 1:1000 [115] are used. They are also in groups of three for measuring three-phase currents at the source, load and converter sides respectively. There are also 6 breakout connectors for flying capacitor voltages of 6 submodules from the MMFCC.

The digital control unit receives all measured analogue signals, converts them into their digital equivalents and applies them to the control software which generates the reference voltage signals. The FPGA card receives these signals and generates PWM switching pulses to drive the MMFCC switches.

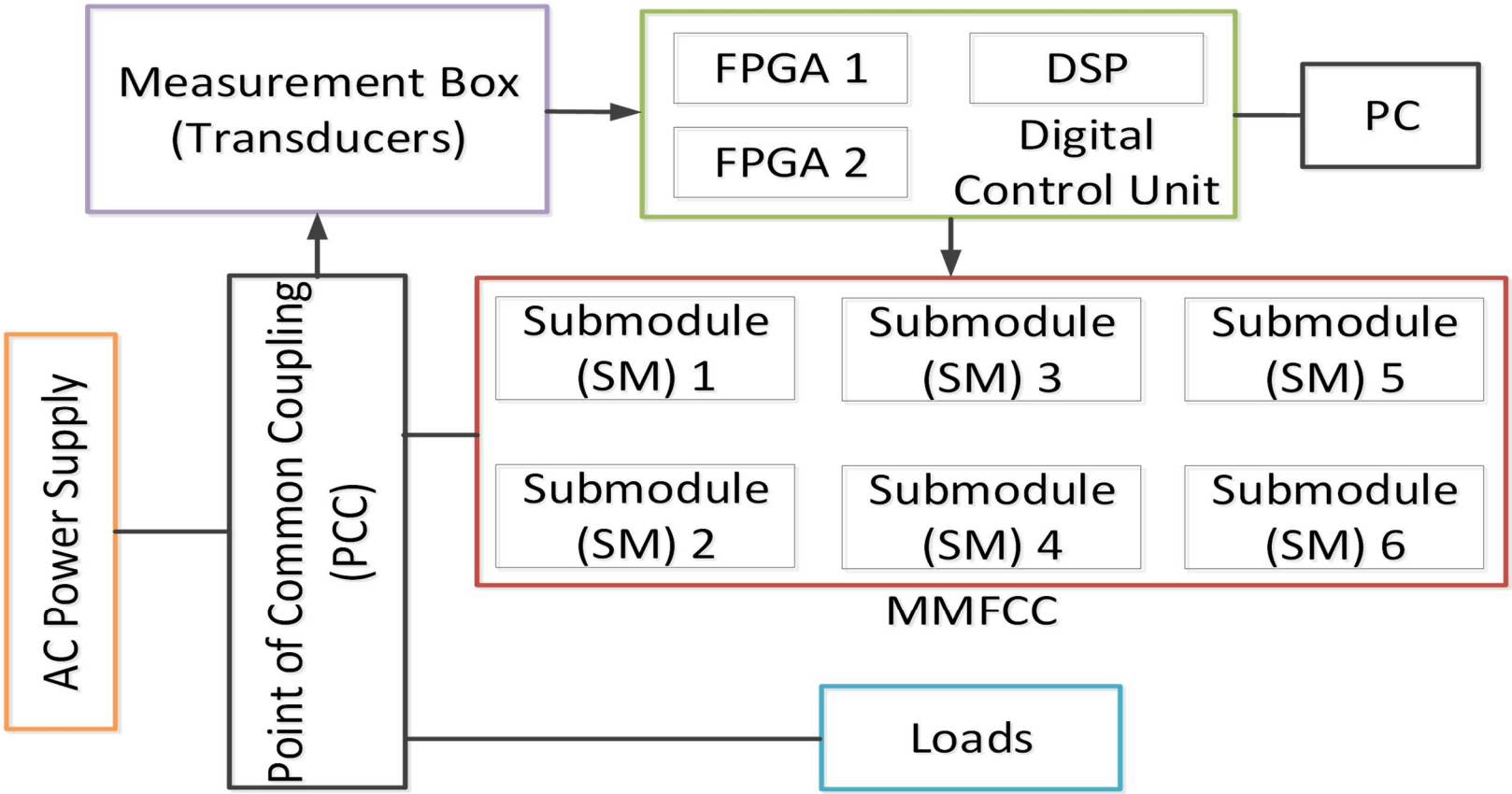


Fig. 5.1 Hardware block diagram

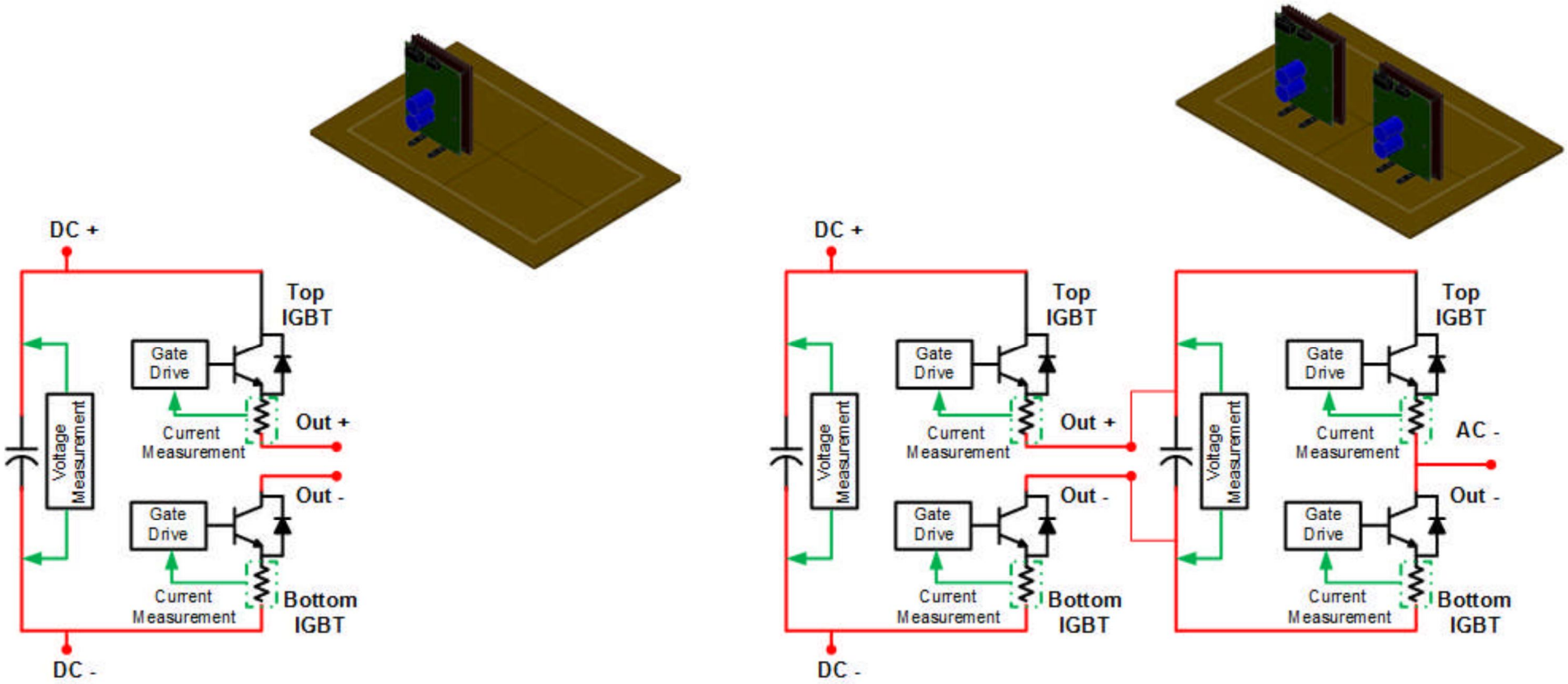


Fig. 5.2 (a) FC half-bridge cell and (b) 3-level FC half-bridge

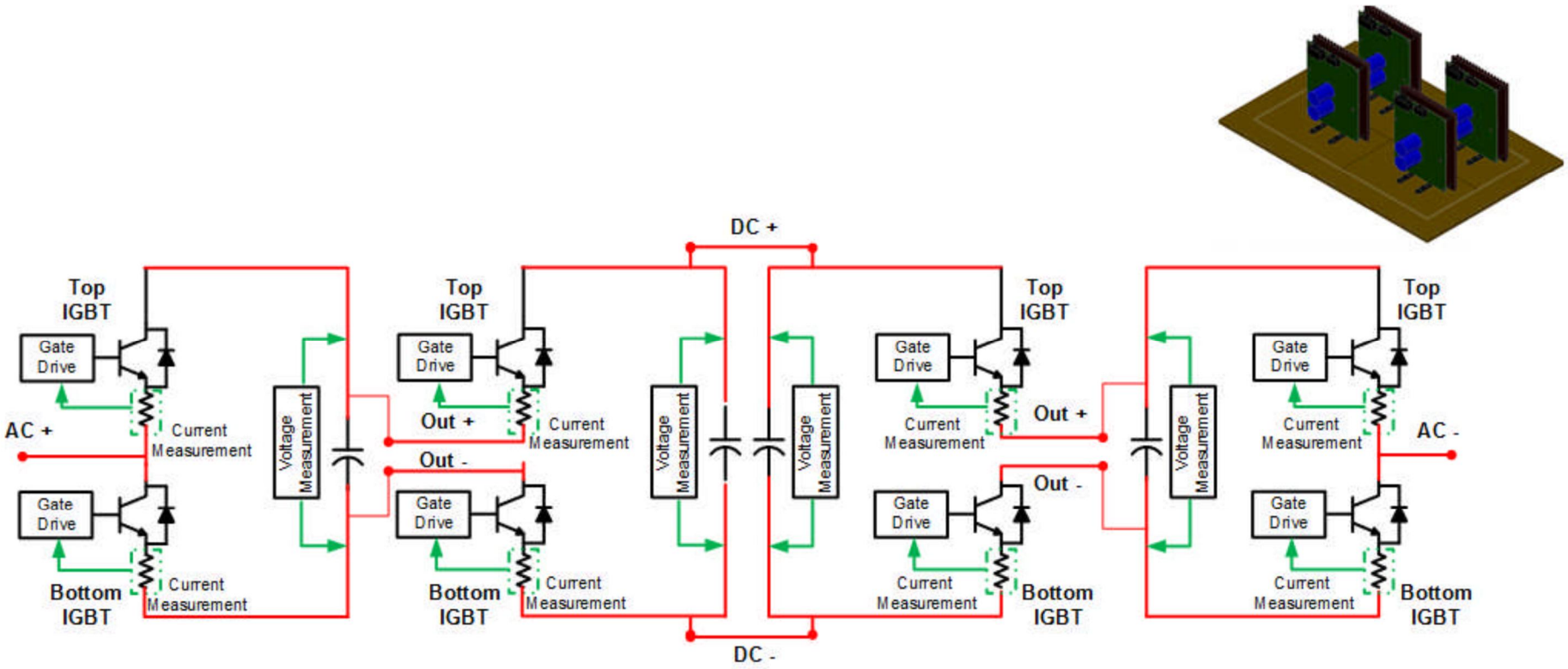


Fig. 5.3 5-level FC full bridge SM

5.2.2 MMFCC cell card power circuit

The detailed circuit diagram of the MMFCC half-bridge cell card [116] is as shown in Fig. 5.4. It is comprised of two Infineon 600V-30A IGBTs [117] and one Panasonic large-can aluminium electrolytic capacitor [118], as well as an isolated 15V DC-DC converter to power the gate drive circuits, over current protection, voltage and current sensing circuits. Each cell card is a surface mount double layer printed circuit board (PCB) and is shown in Appendix C.1. The protection adopts S-R latching circuit to reset the circuitry when over voltage and current fault occurs.

The switching pulses from control board to gate drives are transfered by a fibre optic transmitter-reciver, which provides galvanic isolation between the digital and analogue signals. The circuit is based on the Avago's technologies HBFR-1521 transmitter and HBFR-2531 recivers [119] and powered by a 5V power supply, which is the main supply source for the cell card, as shown in Fig. 5.5. Besides, the voltage transducers for capacitor voltage measurement are supplyed by a ±15V power supply, and the protection circuit is supplied by the 3.3V generated from the linear voltage regulator. The switching devices and capacitor parameters are listed in Appendix C.2.

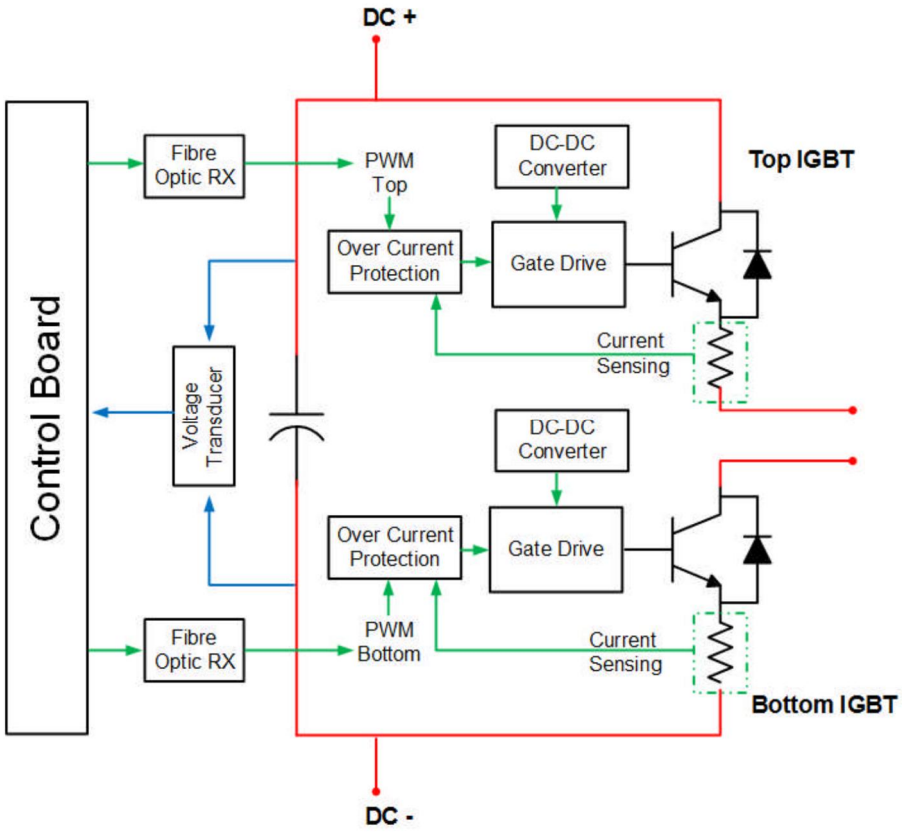


Fig. 5.4 Cell card power circuit

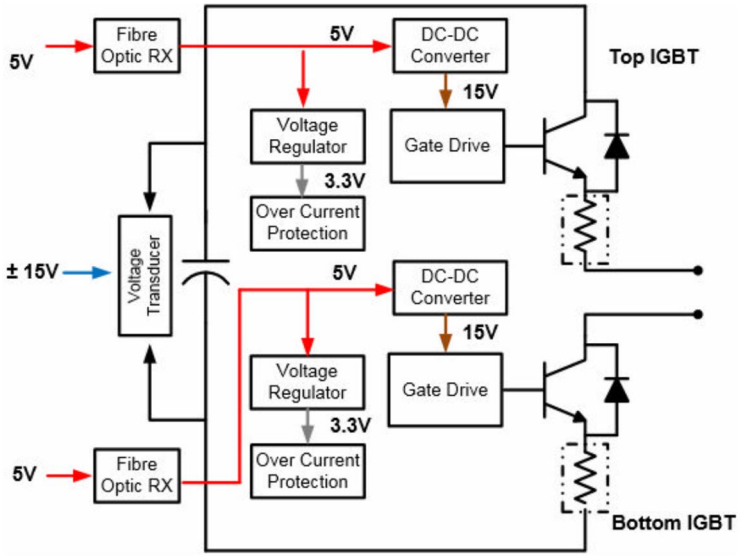


Fig. 5.5 Cell card power supply layout

5.2.3 Digital control system unit

The digital control system consists of an ACTEL (Now Microsemi) ProAsic III FPGA [120] module and a Texas Instrument 32 bit floating point DSP [121]. The two units are communicated through the external memory interface (EMIF), while a host port interface (HPI) daughter card is used for monitoring the EMIF. The measured data acquired from voltage and current transducers are converted into digital form with these two units in order to process the APC control actions.

5.2.3.1 FPGA cards

The FPGA cards are populated on a printed circuit board designed by the Power Electronics, Machine and Control Group (PEMC) at the University of Nottingham. It sits on the 32 bit EMIF and communicates with the DSP via a 32 bit data bus and a 7 bit address bus. The FPGA cards carry out two main functions:

(a) Sampling and transmitting the measured signals of voltage and current transducers to DSP through an interrupt routine;

(b) Translating the control actions from DSP back to PWM signals for the MMCC. Then the signals will be conveyed to each gate drive through the fibre optic breakout boards and transmitters. Fig. 5.6 shows the FPGA cards connected with fibre optic breakout board.

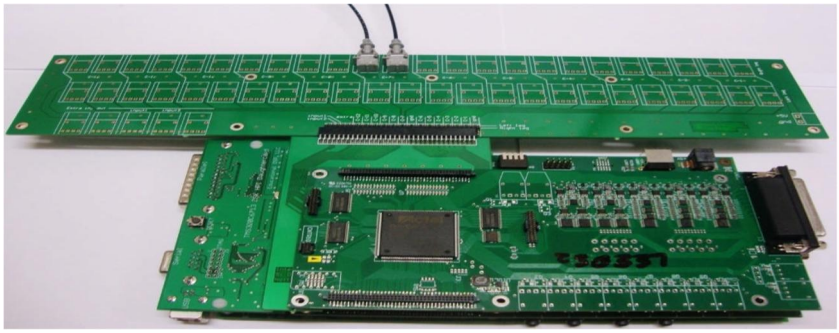


Fig. 5.6 FPGA cards connected with fibre optic breakout board

Modulation unit

The modulation unit is created based on the FPGA program in order to controlling the generation of carrier permutation phase shifted PWM (CP PS-PWM) signals for the semiconductor switches. It comprises both the triangle carrier generation and pulses generation.

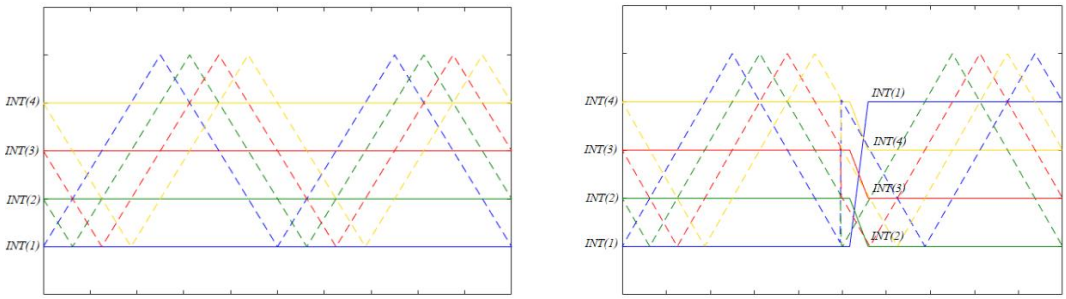
For the conventional PS-PWM applied on the 9-level MMFCC, four triangle carriers are required and they are 45° phase shifted from each other. Therefore the modulation unit will produce the required carrier phase initialisation integers $INT(n)$ according to the following expressions

$$UPLIM = \frac{f_{clk}}{2 \times f_{car}} \tag{5.1}$$

$$INT(n) = \frac{n-1}{n_{max}} \times UPLIM \tag{5.2}$$

where $UPLIM$ is carrier upper limit, f_{clk} is the clock frequency and fixed at 10MHz, f_{car} equals to carrier frequency and sets as 1kHz, n is the number of carriers.

Hence, the four carrier initialisations $INT(1-4)$ can be illustrated by the four straight lines in Fig. 5.7(a), while the carriers are represented by the dotted lines in the same colour sequence. For CP PS-PWM, the permutations between carriers can be implemented by swapping the $INT(n)$, as shown in Fig. 5.7(b). The first dotted carrier (blue) will swap to the 4th carrier's position when the $INT(1)$ moves to $INT(4)$'s position. In such a manner, a complete $INT(n)$ permutation cycle of CP PS-PWM is shown in Fig. 5.8.



(a) (b)

Fig. 5.7 (a) PS-PWM carrier initialisations (b) Permutation of carriers and their initialisations

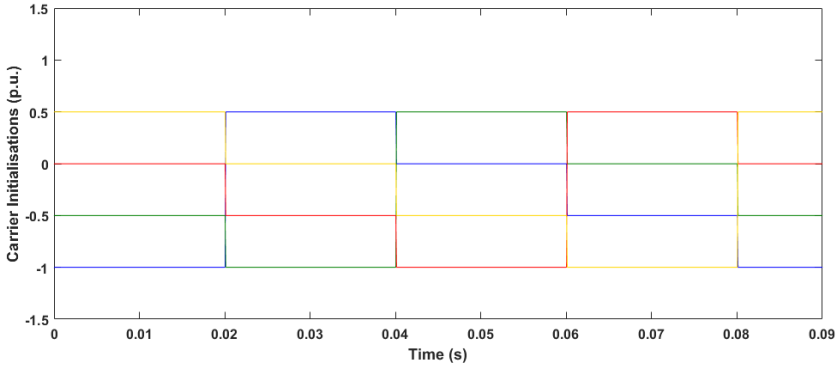


Fig. 5.8 Carrier initialisations in a complete permutation cycle (0.08sec)

5.2.3.2 Digital signal processor

The DSP used is TMS320C6713, a high speed floating point processor with 225MHz clock frequency from Texas Instrument. It is built on Harvard architecture and operating up to eight times per instruction. The DSP is connected to PC via a DSP LLC DSK6713HPI HPI interface daughter card. This enables the real time access of data variables to the external memory during DSP operation. The DSP is a 'Master' control centre and its main functions can be concluded as two:

(a) Receiving and translating the 16 bit A/D signals from FPGA to the applied MMCC control actions;

(b) Sending reference signals to the FPGA to compare with carriers and generate pulses signals.

To enhance the MMCC control accuracy, the A/D signals from FPGA need to be calibrated and converted back to their original values in the DSP according to the equations (5.3) - (5.5).

$$S_{norm} = (S - S_{mid}) / S_{mid} \tag{5.3}$$

$$S_{mid} = (S_{pk-pk} / 2) - S_{pk} \tag{5.4}$$

$$S_{actual} = S_{norm} \times C_f \tag{5.5}$$

where S is the A/D signal from FPGA, S_{mid} is the midpoint of signal without transducer offsets, S_{norm} is the normalised signal and C_f is the transducer conversion ratio.

5.2.3.3 Software program structure

The main program routine, which is for initialising all the variables and setting the EMIF, contains two main sub routines:

(a) FPGA Sub Routine: This routine resets the FPGA and set the interrupt services to be ready for the (b) routine. Then, the watchdog timer is enabled and PWM signal dead time is setup. Thereafter, the carrier initial values are sent to registers and ready for the external interrupt triggered;

(b) PWM Sub Routine: This routine happens when the external interruption is on. It reads the A/D measured signal form FPGA and calibrate them into control variables in DSP. Then the control actions are performed and consequently reference signals are produced. Lastly the references are transmitted back to FPGA for generating pulses signals.

Fig. 5.9 flow chart shows the detailed of the program main routine and sub routine.

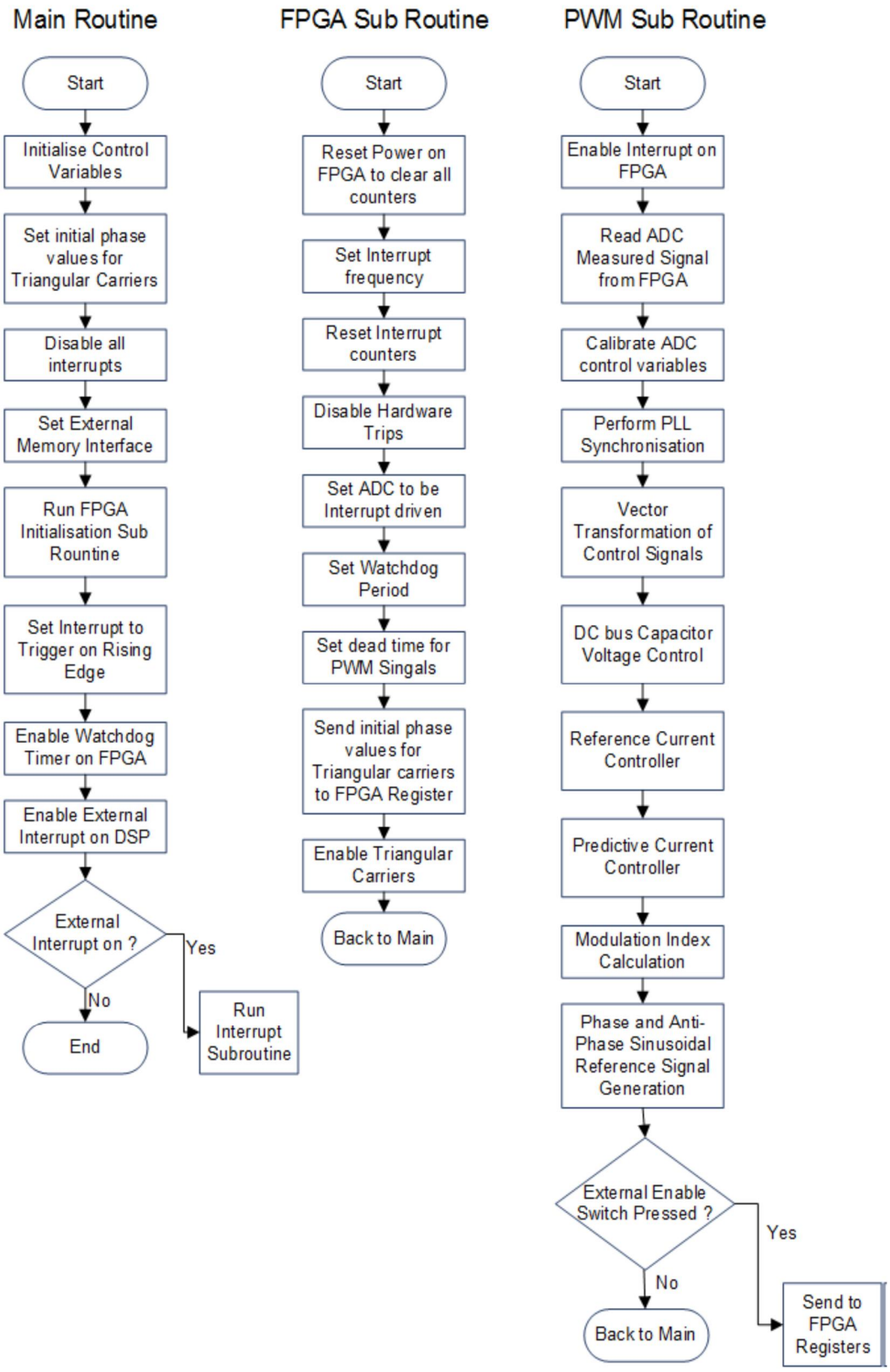


Fig. 5.9 Program main routine and sub routine

5.3 Power System Configuration

The constructed experimental power system circuit diagram is shown in Fig. 5.10. It can be categorized into three main parts:

- The PCC side: it connected to an 110V 3-phase laboratory voltage supply via an isolated transformer and transmission line impedance.
- The load side: it consists of a 3-phase 20Ω, 5A rheostats and 50mH, 5A inductors to represent the inductive load which draws reactive power from the system. Besides, a three-phase diode rectifier is shunt-connected on the load bus to represent the nonlinear load which consumes current harmonics. To emulate different degree of unbalance, an extra rheostat is connected on the load bus phase A.
- The converter side: this part includes the built test prototype 3-phase 9-level MMFCC and a RL filter representing a simplified model of converter transformer.

All the three parts are connected together at the Point of Common Coupling (PCC). The parameters of the system components are listed in Table 5.1. Fig. 5.11 shows the photograph of the rig.

Table 5.1 Experimental system component parameters

Components		**Value**
PCC Side	3-phase voltage source	*1.8 kVA (60 V, 10A)*
Distribution Line	Aluminium PI TX line (d=10mm, l=1.1km)	R_{line} *= 0.5 Ω;* L_{line} *= 2mH*
Load Side	3-Phase Diode Rectifier R+L Load	*1.8 kVA (60 V, 10A)* R_{dc_r} *= 20Ω;* L_{ac_r} *= 8.3mH* R_l *= 10Ω;* L_l *= 48mH*
Converter Side	RL Filter DC capacitor in each sub-module Switching frequency	*1.5 kVA (100 V, 5A)* R_c *= 1.59Ω;* L_c *= 2mH* V_{dc}*= 400V;* C_{dc}*= 1.12 mF (utilized at 50V)* *1 kHZ*

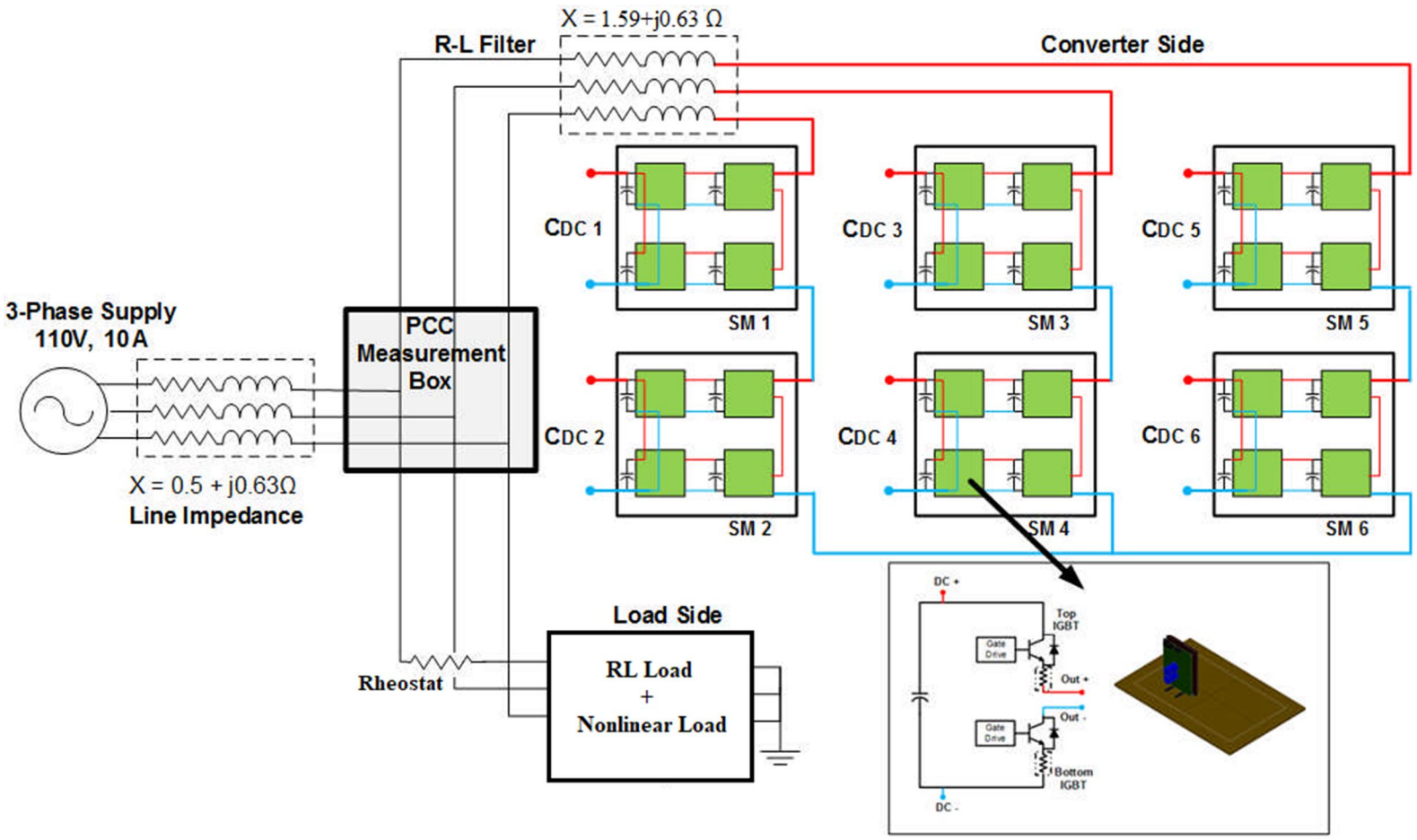


Fig. 5.10 Experimental power system circuit diagram

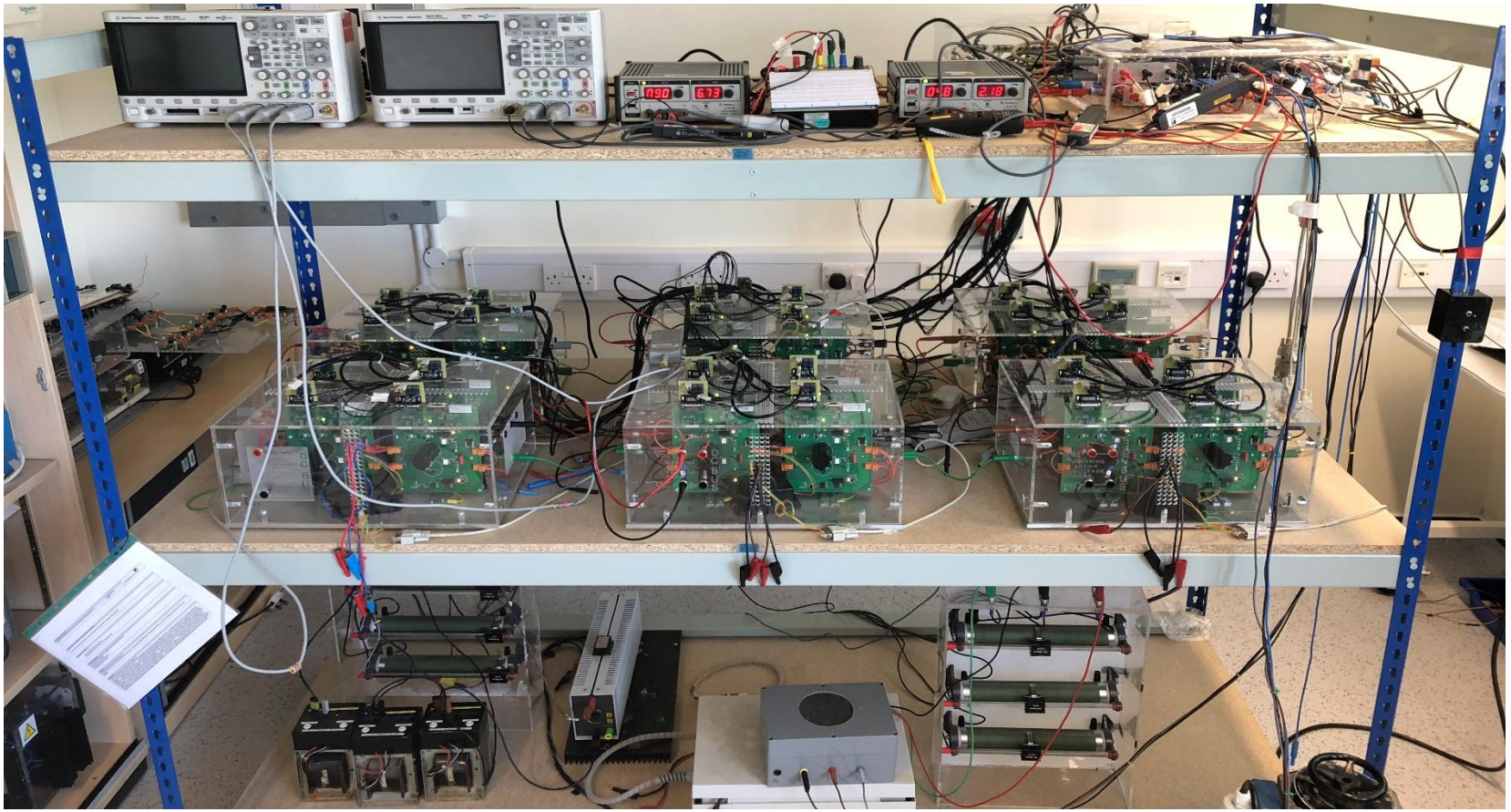


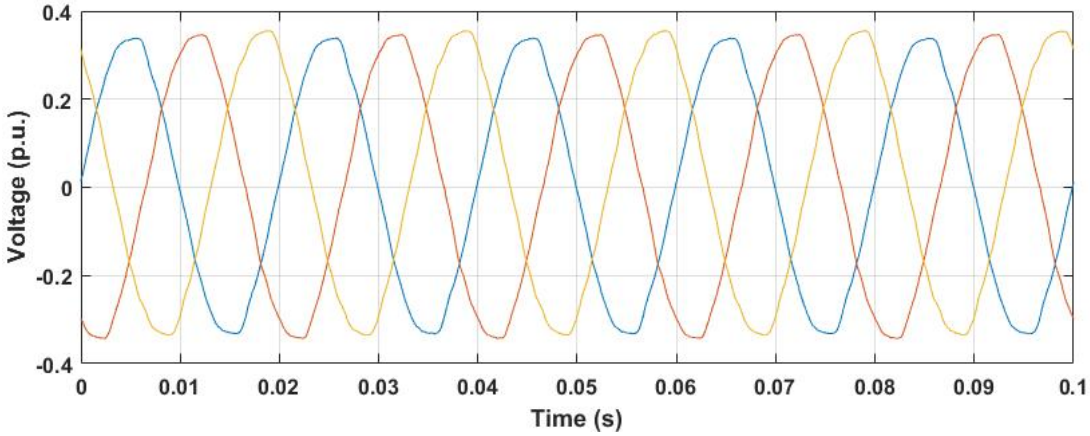
Fig. 5.11 Experimental rig photograph

5.4 Control System Implementation

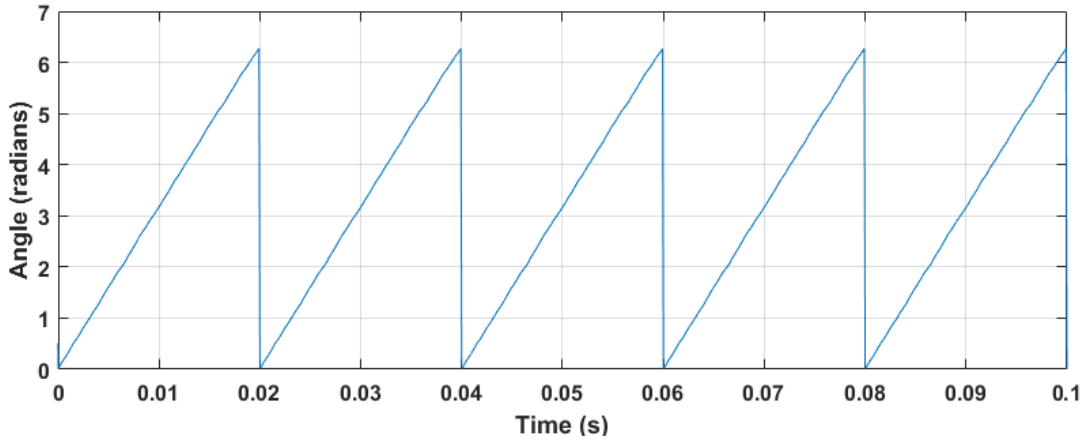
The real-time control scheme to enable the MMFCC to compensate unbalanced harmonics current is implemented on the DSP and FPGA as illustrated in the previous section.

5.4.1 Grid synchronization

In this implementation, the 3-phase voltage of the system is balanced hence the synchronous reference frame phase lock loop scheme is applied. The measured 3-phase grid voltage is shown in Fig. 5.12 (a) and the PLL generated phase angle is shown in Fig. 5.12(b).



(a)



(b)

Fig. 5.12 Synchronised (a) 3-phase grid voltage and (b) angle

5.4.2 Discrete PI controller for sub-module capacitor voltage balancing control

The proportional and integral control is adopted to control the converter DC capacitor voltages. A discretised version is developed based on the derivation shown as below so that the controller can be implemented during the interrupt routine.

$$V_{error} = V_{ref} - V_{actual} \tag{5.6}$$

$$V_{errori} = (V_{error} + V_{error\_prev})/T_S \tag{5.7}$$

$$I_{dc} = K_p(V_{error} + \frac{V_{errori}}{T_i})T_S \quad (5.8)$$

where V_{error} is the proportional error, V_{errori} is the integral error, T_i is the integration time constant, T_S is the sampling time and K_p is the proportional gain. $K_p = 0.5$, $T_i = 0.1$ hence to achieve a fast settling time, small overshoot and minimum steady state error. The resultant output I_{dc} is the reference signal that using for controlling the converter DC capacitor voltages.

5.4.3 Capacitor pre-charge control

The capacitor pre-charge control is implemented by controlling the active power absorbed by the converter whilst setting the reactive power reference to be zero. This enables the device capacitors to be charged up to its nominal level before the compensating operation starts. Fig. 5.13 shows the control block diagram, where I_{dc} is the reference signal generated from the PI controller.

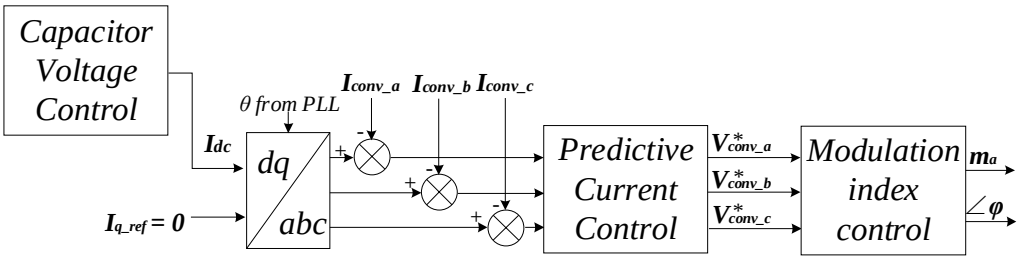


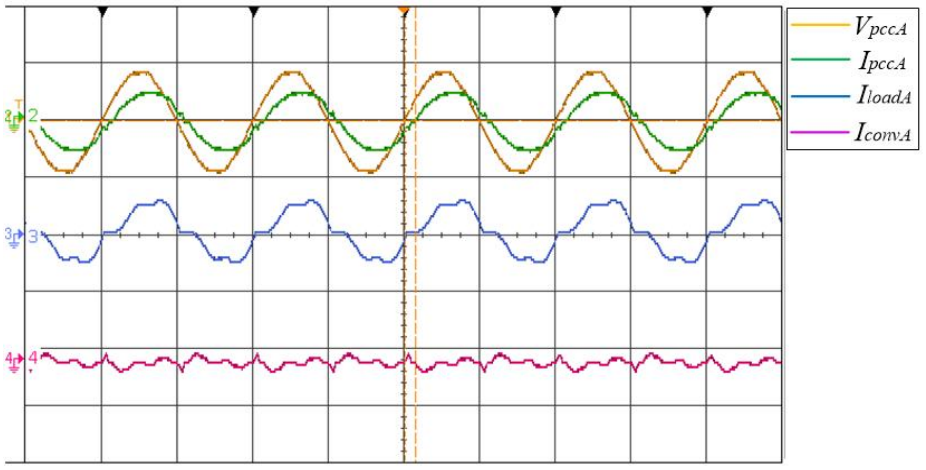
Fig. 5.13 Capacitor pre-charge control block

5.5 Results and Discussion

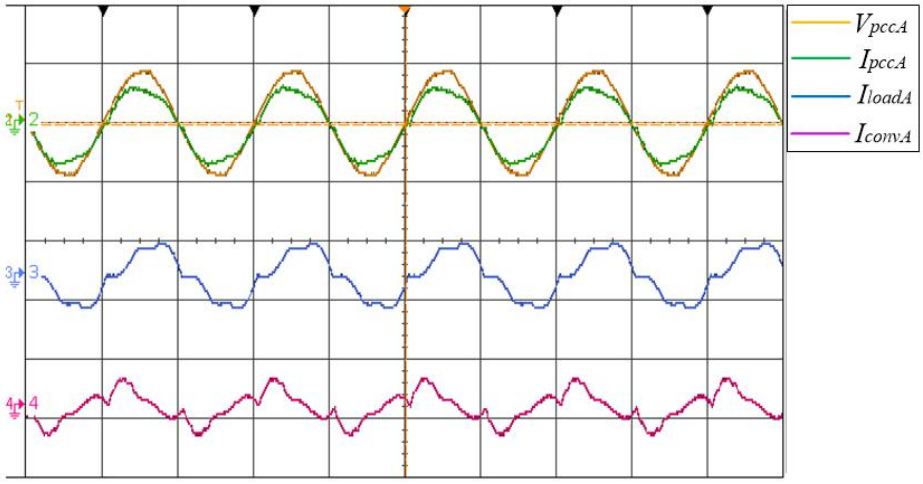
The experimental results of the MMFCC-APC compensation under balanced and unbalanced harmonic conditions are shown in this section. For balanced situation, the rectifier and inductive load are shunt connected to draw reactive power with harmonic distorted currents. For unbalanced case, both star and delta-connected MMFCC are verified to compensate for reactive power, eliminate harmonics and rebalance load current at the supply side simultaneously.

5.5.1 MMFCC-APC for balanced non-linear load condition

During the time interval 0 < t <1.2 sec the MMFCC is in pre-charge mode, so that its submodule capacitors are charged up to their required voltage levels. Between time interval 1.2 sec < t < 2.2 sec, the MMFCC functions to eliminate harmonics in supply current, I_{pcc}. As can be seen from oscilloscope obtained shown in Fig. 5.14(a), phase A supply current I_{pccA} is sinusoidal while the load current, I_{loadA}, is distorted, and the converter compensating current, I_{convA}, contains only the low order harmonics. From t = 2.2sec, the MMFCC compensates for both harmonics and reactive power, as shown in Fig. 5.14(b). The supply side current becomes in phase with the PCC voltage and I_{convA} contains not only harmonics, but also fundamental frequency component, which is the reactive current required to be injected to the grid. More details are downloaded from the DSP as illustrated in the following part.



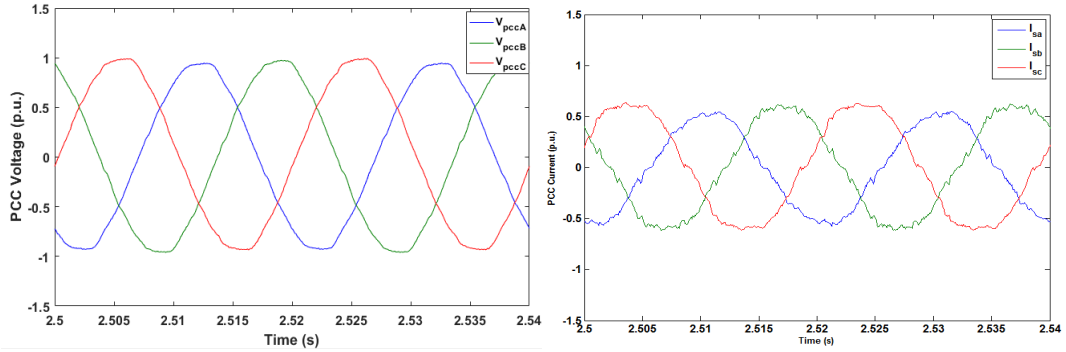
(a)



(b)

Fig. 5.14 Oscilloscope results of MMFCC compensates (a) for harmonics only and (b) for both harmonics and reactive power

PCC side results: Fig. 5.15 shows the waveforms of 3-phase balanced PCC voltages and supply side currents from DSP. Including the phase A shown on the oscilloscope in the previous figure, the 3 phase currents are all sinusoidal and balanced with little ripples and the magnitude is about 0.6 p.u. (3A).



(a) (b)

Fig. 5.15 3-phase (a) PCC voltage (b) source current

Load side results: The waveforms of balanced 3-phase nonlinear load current are shown in Fig. 5.16 and the magnitude is 0.6p.u. (3A).

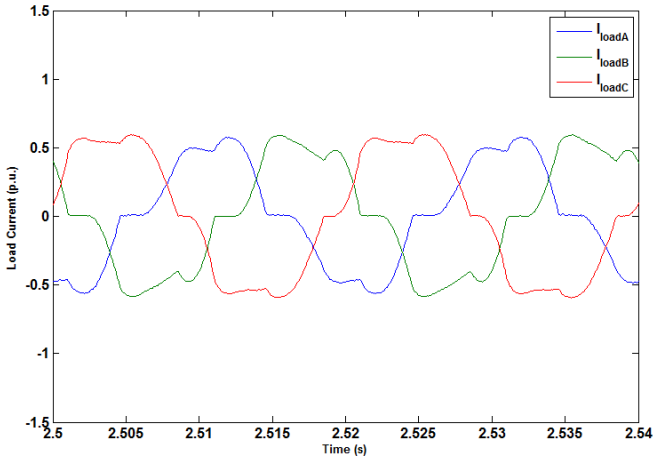
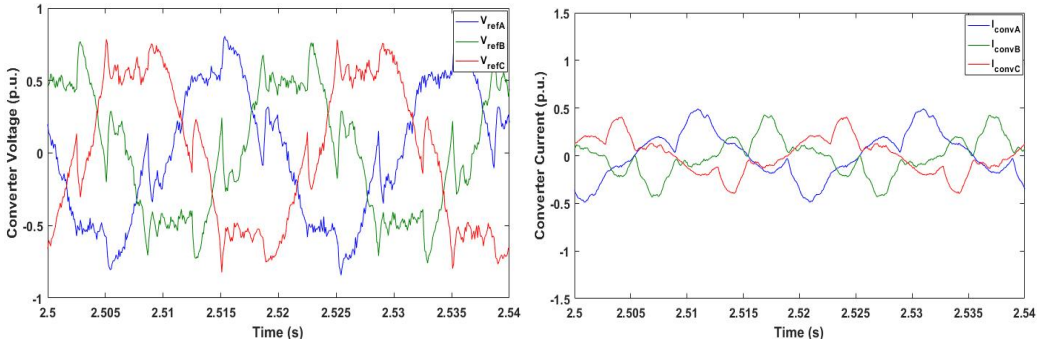


Fig. 5.16 3-phase load current

Converter side results: As the MMFCC required to generate high rate-of-change harmonics current, the 3-phase distorted reference voltage and current are shown in Figs. 5.17 (a) and (b), while the magnitudes are around 0.75p.u. and 0.5p.u. respectively. Fig. 5.18 shows the waveforms of 6 module DC capacitor voltages, which are pre-charged to their nominal value 1p.u. from 0 to 1.2sec; during 1.2sec to 2.2sec, the device only compensates for harmonics thus the ripples of the DC capacitor waveforms are smaller than when it compensates for both harmonics and reactive power.



(a) (b)

Fig. 5.17 3-phase converter (a)reference voltage and (b)current

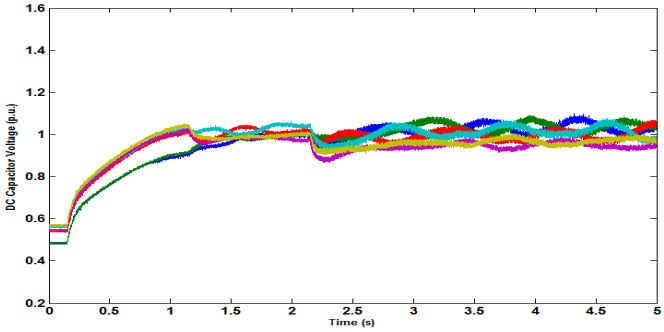


Fig. 5.18 6 Module DC capacitor voltage waveforms

5.5.2 MMFCC-APC under unbalanced non-linear load condition

The MMFCC-APC's capability of compensating harmonics and unbalanced current has been validated experimentally for both SSBC and SDBC configurations. The capacitors rating and control gain parameters of these two configurations are listed in Table 5.2, which are designed to satisfy the specifications of zero steady-state error, fast transient performance (< 2ms) and minimum overshoot (< 5%).

Table 5.2 Capacitor and control gain parameters

Parameters	*SSBC*	*SDBC*
DC capacitor in each sub-module	*Utilized at 50V*	*Utilized at 80V*
Overall DC capacitor proportional gain K_{p_dc}	*0.6*	*0.5*
Overall DC capacitor integral gain K_{i_dc}	*6*	*5*
Cluster capacitor proportional gain K_{pc}	*0.2*	*0.05*
Cluster capacitor proportional gain K_{ic}	*1*	*1*
Circulating current proportional gain K_{pio}	-	*30*

The following describes tests on the practical MMFCC-APC rig, and investigates and compares the operating ranges of the SSBC and SDBC configurations under two different control requirements respectively, i.e. compensating reactive power and unbalanced load without harmonic cancellation (Fig. 5.19 for SSBC, Fig. 5.21 for SDBC), and with harmonic cancellation (Fig.5.20 for SSBC, Fig.5.22 for SDBC). The order of display in all sets of figures is as follows: (a) shows $\boldsymbol{K_{ir}}$ variation, (b) and (c) are waveforms of the supply voltages and currents denoted respectively as $\boldsymbol{V_{Sabc}}$ and $\boldsymbol{I_{Sabc}}$; Graph (d) shows converter phase cluster reference voltages, $\boldsymbol{V_{Cabc}}$* and the converter cluster currents, $\boldsymbol{I_{Cabc}}$ are displayed in (e). The imposed zero sequence component for balancing three phase powers denoted as $\boldsymbol{V_o}$ (or $\boldsymbol{I_o}$) is displayed in (f) and finally the 6 module DC capacitor voltages, $\boldsymbol{V_{DC}}$ are in (g).

In Fig. 5.19, the device functions as a conventional STATCOM by supplying reactive current to the grid according to load drawing value and, if required, may eliminate load current negative sequence element. From 0<t<0.1 second, the device is not active, hence the PCC current waveforms shown in Fig.5.19(c) are not in phase with the voltage in (b) and unbalanced. At 0.1<t<0.2, reactive current compensation is performed leading to current shown in (c) being in phase with the PCC voltage in (b), but still unbalanced. In this case the converter compensating current, $\boldsymbol{I_{Cabc}}$, shown in (e) increased. From t>0.2 second, the SSBC-APC is set to supply load required reactive current as well as eliminating current imbalance up to the level measured by $\boldsymbol{K_{ir}}$= 0.4 to 0.6. During 0.2<t<0.4 when $\boldsymbol{K_{ir}}$ changes from 0.4 to 0.5, the PCC current

$\boldsymbol{I_{Sabc}}$ are shown balanced and in phase with $\boldsymbol{V_{Sabc}}$ in (b). The converter terminal voltage $\boldsymbol{V_{Cabc}}$ (in (d)) and current $\boldsymbol{I_{Cabc}}$ (in (e)) are naturally all increased and unbalanced. The zero sequence voltage $\boldsymbol{V_o}$ (in (f)) is increased and 6 module DC voltages (in (g)) are maintained balanced. Further increase $\boldsymbol{K_{ir}}$ to 0.6, the controller capability is reaching the limit, 3-phase PCC current is significantly distorted and DC capacitor voltages start to drift away from their nominal value.

When harmonics compensation function is added to the MMCC, the device in SSBC configuration operating range changes. Fig. 5.20 shows the waveforms of all the variables displayed in the same order as that in Fig. 5.20 when $\boldsymbol{K_{ir}}$ changes from 0 to 0.5. As can be seen, during time 0<t<0.1 second, SSBC-APC does not perform any control, PCC current $\boldsymbol{I_{Sabc}}$ is unbalanced, not in phase with $\boldsymbol{V_{Sabc}}$ in (b) and corrupted with harmonics. From 0.1 <t <0.2 second, controller performs both reactive current compensation and harmonic current cancellation, but not to balance the load current. PCC current $\boldsymbol{I_{Sabc}}$ is shown sinusoidal and in phase with $\boldsymbol{V_{Sabc}}$ in (b), but three phase values are unbalanced, hence $\boldsymbol{V_o}$ is zero and $\boldsymbol{V_{DC}}$s are balanced. $\boldsymbol{V_{Cabc}}$ and $\boldsymbol{I_{Cabc}}$ are shown harmonic distortion since MMCC injects harmonic current to cancel those in the load current. From 0.2<t<0.3 second, MMCC compensates unbalanced current up to $\boldsymbol{K_{ir}}$ = 0.4 while simultaneously supplies load reactive current and eliminates harmonics. As can be seen from $\boldsymbol{I_{Sabc}}$ waveforms in (c), good control is obtained, $\boldsymbol{I_{Sabc}}$ is well-balanced with little harmonic corruptions and in phase with the PCC voltage. The converter phase voltage and current $\boldsymbol{V_{Cabc}}$ and $\boldsymbol{I_{Cabc}}$, are all increased in this case. $\boldsymbol{V_o}$ in (f) is none zero to balance phase cluster voltage. However further increasing $\boldsymbol{K_{ir}}$ to 0.5, PCC current $\boldsymbol{I_{Sabc}}$ cannot be maintained balanced as that in the previous case shown in Fig. 5.20. This is due to that the magnitude of the injected zero sequence voltage $\boldsymbol{V_o}$ increases significantly and becomes distorted. Fig. 5.23 shows the $\boldsymbol{V_o}$ when compensating unbalanced current (up to level of $\boldsymbol{K_{ir}}$ = 0.5) without and with harmonics cases. Clearly in the first case $\boldsymbol{V_o}$ is noise free and its magnitude evaluated for cancelling the circulating power is low (about ±20 Volts). However in the latter case, $\boldsymbol{V_o}$ is distorted and its magnitude is higher (±40 Volts). This pushes the highest converter phase voltage magnitudes above the rated levels as shown in Fig. 5.23. Consequently the phase cluster DC voltages drift apart since $\boldsymbol{V_o}$ cannot cancel the unbalanced phase power. In contrast to previous case shown in Fig. 5.19, it is clear that the operating range of SSBC configured MMCC-APC is reduced when compensating both load current imbalance and harmonic contents.

The operating behaviours of SDBC configured MMCC-APC under the two different conditions are shown in Fig. 5.21 and 5.22. The most obvious superiority of this configuration over SSBC is that its capability of dealing with high $\boldsymbol{K_{ir}}$. Hence, the reduced operating range drawback of SSBC when compensating both load current imbalance and harmonics is overcome by the SDBC configuration, as shown in Fig. 5.21(g) and 5.22(g). The module DC capacitor voltages are maintained within 10% of their nominal value when $\boldsymbol{K_{ir}}$ up to 0.6, whether the device compensate for only current imbalance or both imbalance and harmonics.

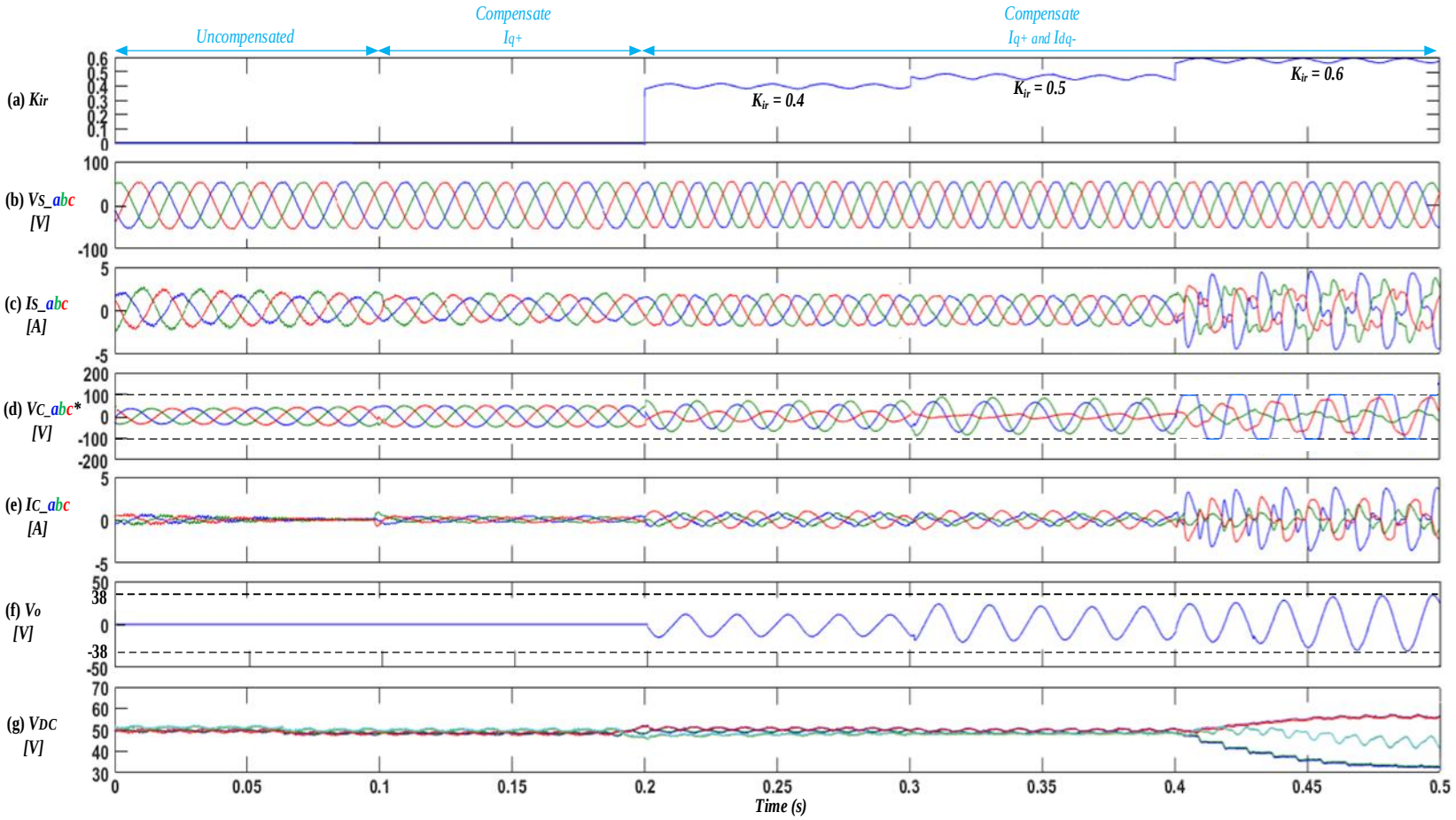


Fig. 5.19 SSBC Compensation of load current imbalance without harmonics

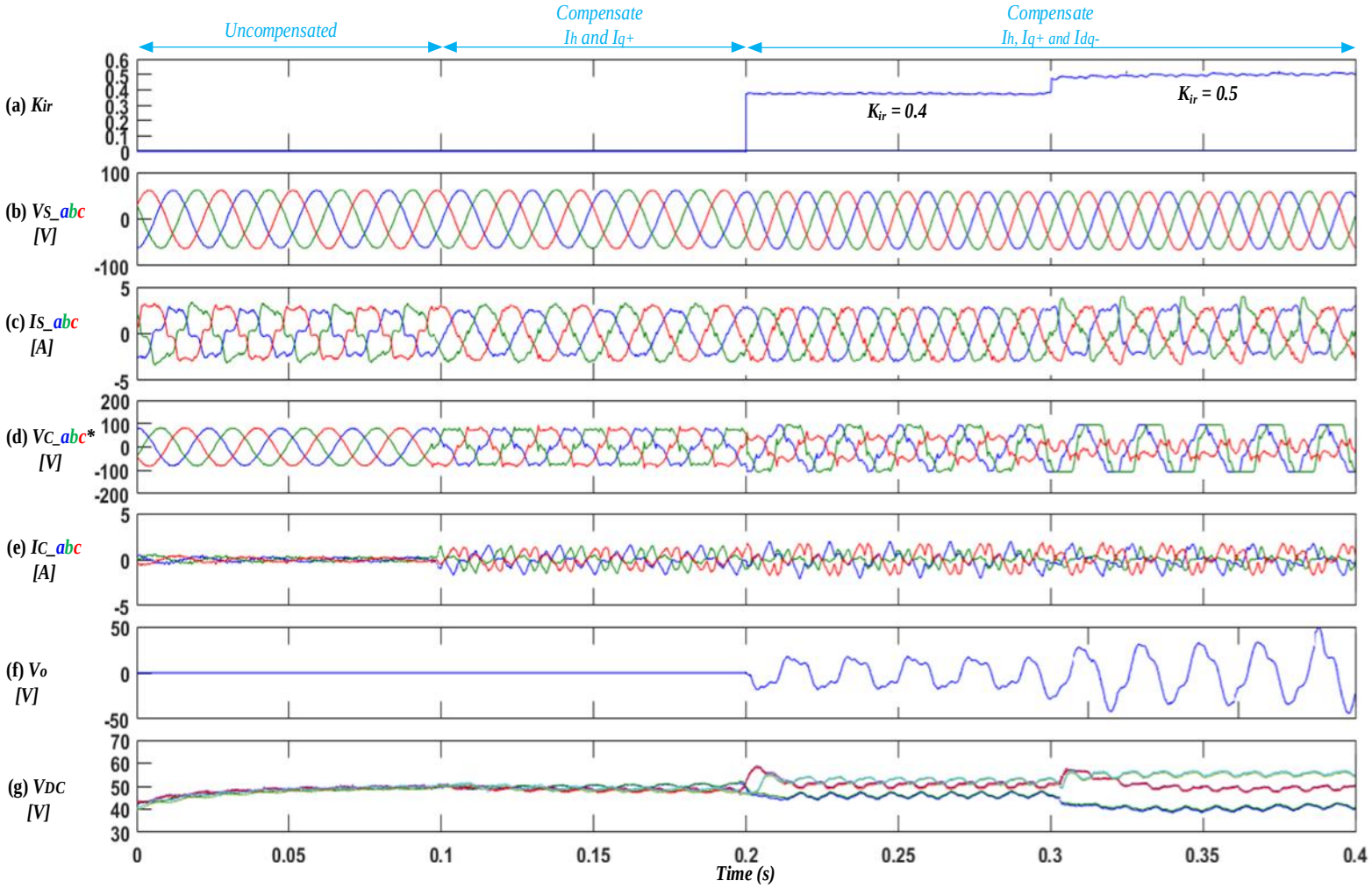


Fig. 5.20 SSBC Compensation of both load current harmonics and imbalance

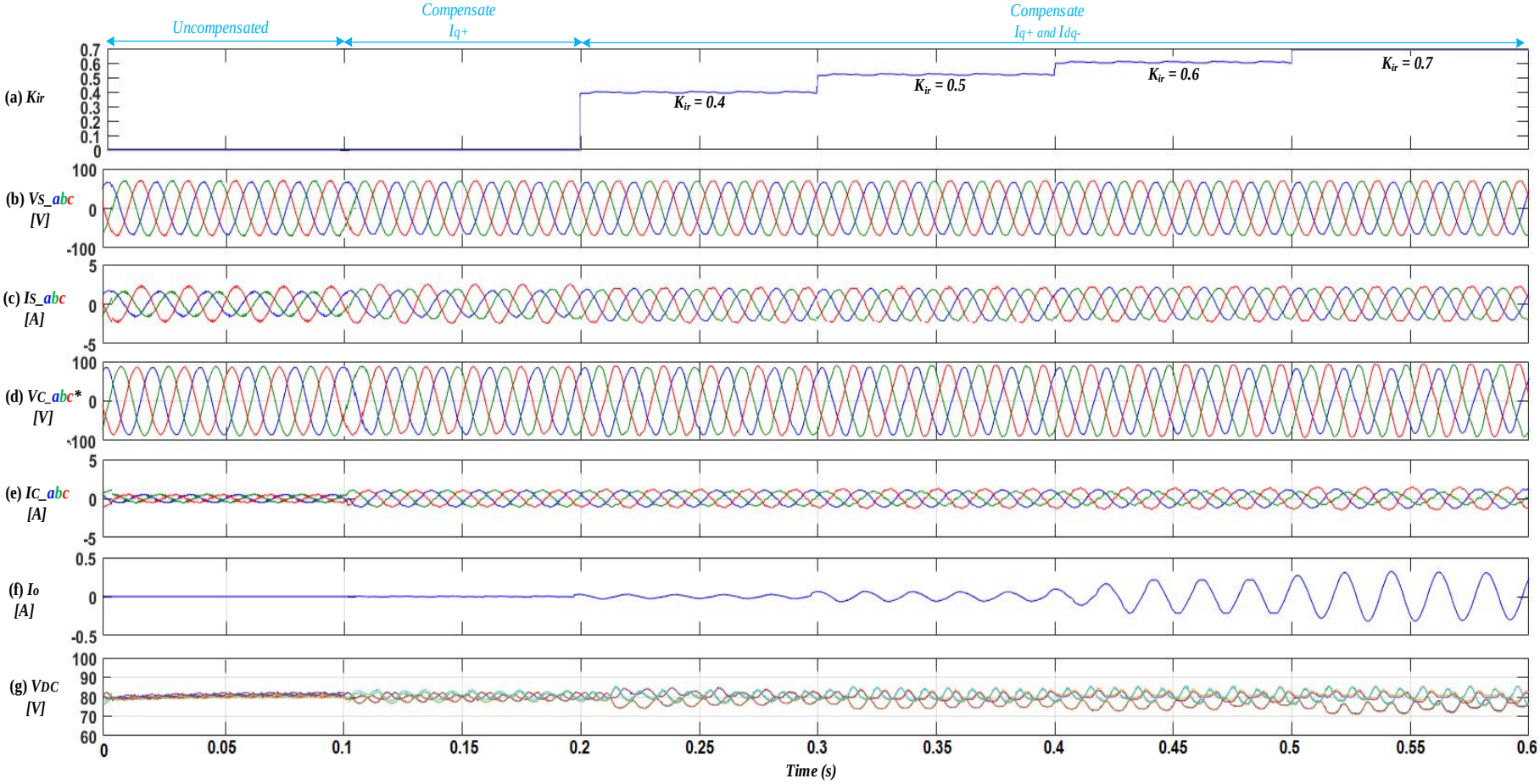


Fig. 5.21 SDBC Compensation of load current imbalance without harmonics

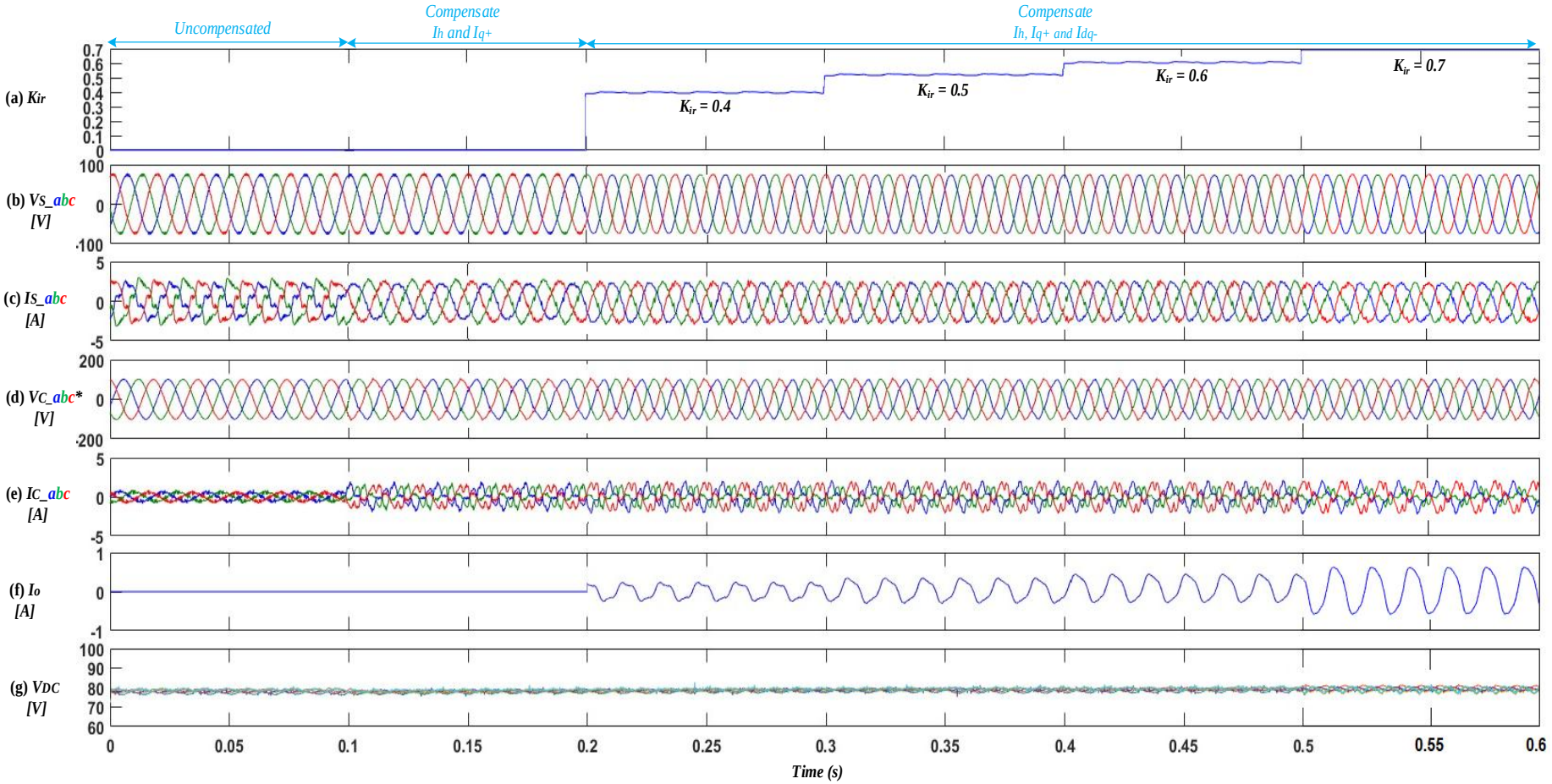
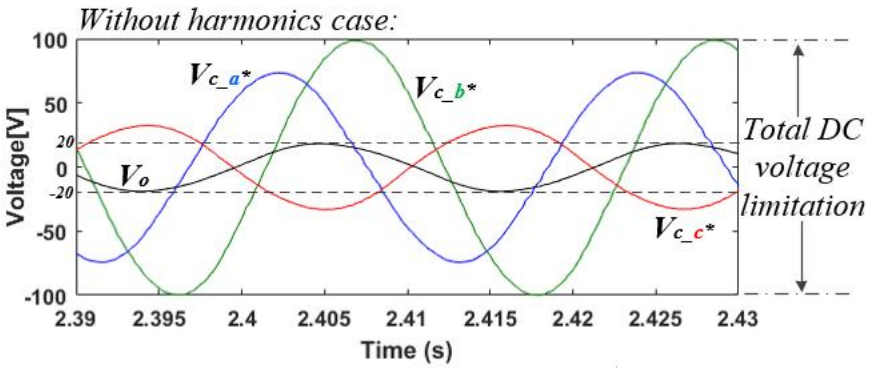
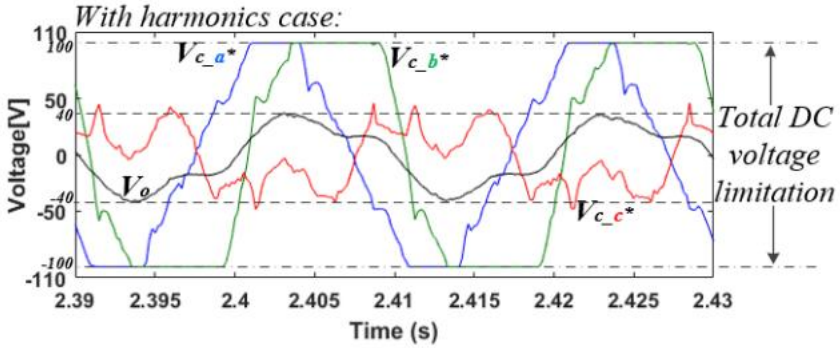


Fig. 5.22 SDBC Compensation of both load current harmonics and imbalance



(a)



(b)

Fig. 5.23 SSBC configured MMCC-APC cluster reference voltage with injecting $\boldsymbol{V_o}$ (a) without harmonics extraction (b) with harmonics extraction

5.5.3 Comparison between simulation and experimental results

The simulation and experimental results of both star and delta connected MMCC-APC have been performed under the same condition. It can be seen that the source current at PCC becomes balanced and sinusoidal and in phase with PCC voltage after compensated by the APC in both simulated and experimental work. For the delta configuration, the results show a fully compensation performance while for the star configuration, the operating range of $\boldsymbol{K_{ir}}$ are within 0.5 under both simulation and experiment tests.

The main differences are:

- In the SSBC experimental results, the DC capacitor voltages will drift away from their nominal value very fast and the compensating current will collapse once the device reaches 100V; in the SSBC simulation results, the converter DC capacitor voltages drift away slowly hence the compensating current will distort gradually.
- In both test conditions, the zero sequence components will distort as long as the device starts to eliminate harmonics current.
- The compensated source current waveforms of the experimental results are less ideal than simulation results because that switching devices and loads are not ideal.

5.6 Summary

This Chapter discussed the experimental setup and validation of the MMFCC for harmonics and unbalanced current compensation. The configuration of MMFCC and the digital control system were presented. The results based on the star and delta configured MMFCC were presented and compared, which confirmed that the SDBC can provide a wider operation range when dealing with unbalanced current, regardless the device eliminate harmonics or not.

Chapter 6 MMFCC-based Unified Power Flow Controller

6.1 Introduction

This chapter will present the development of an MMFCC to function as a Unified Power Flow Controller (UPFC) which controls the power flow in a transmission lines. The UPFC is the most versatile device among the Flexible AC Transmission Systems (FACTS) [122]; it is able to realise simultaneous voltage regulation, line impedance compensation and phase angle adjustment, and hence achieves flexible independent control of real and reactive power flows along the compensated transmission lines and increased power transfer capability margins [123, 124].

In this chapter, the conventional two-level 'back-to-back' converter-based UPFC will be presented in order to analyse its power flow margins. A new MMFCC-based UPFC will be proposed to work in a higher voltage system without the use of a step-up transformer. This UPFC is configured to have an MMFCC shunt connected to the power lines directly, and a two-level voltage source converter serially connected in the lines through a transformer. The control strategies will be derived, and the simulation results will be discussed. A balanced system is assumed throughout this chapter.

6.2 Voltage Source Converter-based UPFC System

A VSC-based UPFC is a device having two voltage source converters (VSCs), connected 'back-to-back' through a common DC-link as shown in Fig. 6.1. The VSC_1 is connected in parallel with the transmission line named as sending end through a voltage step-up transformer. The VSC_2 is connected in series with the line through a series transformer. The power terminal on the right-hand-side of Fig.6.1 is named as receiving end, though direction of power flow can be flexibly changed according to the control requirement. In general VSC_1 provides bidirectional reactive power exchange to maintain the transmission line voltage within the required range; it also absorbs real power to maintain the DC-link capacitor voltage balanced. VSC_2 can inject an AC voltage V_{c1} to the transmission line via the transformer with variable magnitude and a phase displacement of 0-360°. The phase displacement of the inserted voltage, with respect to the transmission line current, determines the exchange of real and reactive power with the AC system. The analysis of the two VSCs will be carried out in the following subsections.

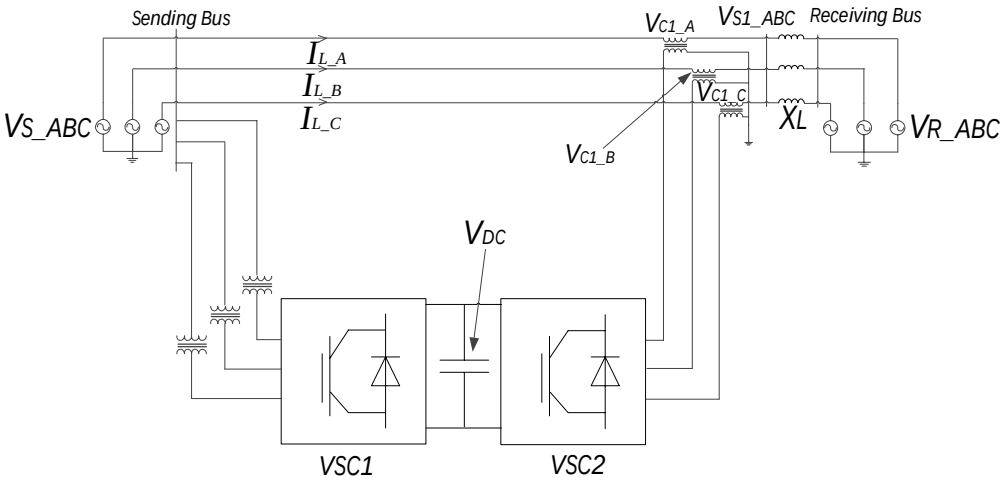


Fig. 6.1 VSC-based UPFC circuit diagram

6.2.1 Principle of power flow control

Assuming the voltages on both sending and receiving ends are maintained at constant levels, then the control of power flow can be adjusted by changing the transmission line impedance. Fig. 6.2 shows the one-line equivalent circuit representation and its corresponding phasor diagram of a simple two source ends three-phase system. According to Kirchhoff's voltage law, the sending end voltage phasor $\overrightarrow{V_s}$ can be expressed as

$$\overrightarrow{V_s} = \overrightarrow{V_R} + \overrightarrow{I_L}(R_L + jX_L) \tag{6.1}$$

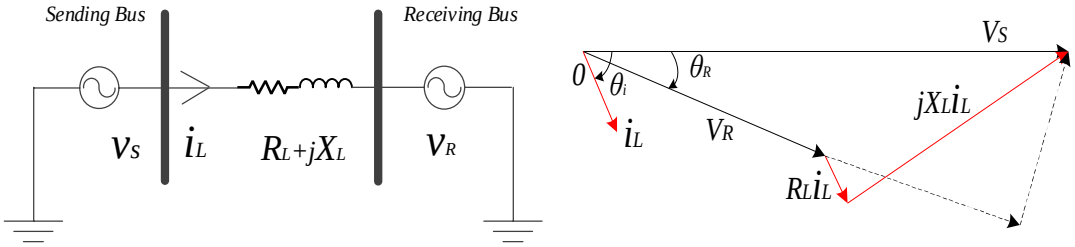


Fig. 6.2 (a) Single line diagram with two voltage source ends and (b) corresponding phasor diagram

where $\overrightarrow{V_R}$ is the receiving end voltage phasor, $R_L + jX_L$ are the line impedance, R_L is normally can be neglected in a transmission line since its value is much smaller than the inductive value. $\overrightarrow{I_L}$ is the current phasor flowing between the line. The apparent, real and reactive powers leaving/receiving on the sending bus can be expressed as:

$$S_s = \overrightarrow{V_s}\overrightarrow{I_L}^* \tag{6.2}$$

$$P_s = \frac{V_s V_R}{X_L} \sin\theta_R \tag{6.3}$$

$$Q_s = \frac{V_s}{X_L}(V_s - V_R \cos\theta_R) \tag{6.4}$$

while those on the receiving bus are

$$S_R = \overrightarrow{V_R}\overrightarrow{I_L}^* \quad (6.5)$$

$$P_R = \frac{V_S V_R}{X_L}\sin\theta_R \quad (6.6)$$

$$Q_R = \frac{V_S}{X_L}(V_S\cos\theta_R - V_R) \quad (6.7)$$

The above equations show that the real and reactive power flows are mainly the functions of voltage magnitudes, power angle θ_R between $\overrightarrow{V_S}$ and $\overrightarrow{V_R}$ at both bus ends, and the reactance X_L of the line:

- Equations (6.3) and (6.6) illustrate that the real power flow is highly depend on the power angle θ_R and reactance X_L;
- Equations (6.4) and (6.7) indicate that the reactive power flow is highly depend on the voltage difference $(\overrightarrow{V_S} - \overrightarrow{V_R})$ and reactance X_L.

Consequently, the power flow can be regulated by injecting a series voltage $\overrightarrow{V_c}$ into the transmission line to control the parameters $\overrightarrow{V_S}$, $\overrightarrow{V_R}$, θ_R and X_L, as shown in the Fig. 6.3.

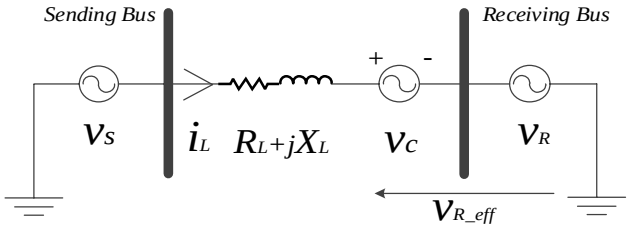


Fig. 6.3 Single line diagram with injected series voltage

The injected voltage $\overrightarrow{V_c}$ can vary between 0° to 360° and be concluded in three main modes, as shown in Fig. 6.4. In practice $\overrightarrow{V_c}$ can be regulated to have the combined effect of these three [125].

- With $\overrightarrow{V_c}$ perpendicular to $\overrightarrow{V_R}$ (Fig. 6.4(a)), the power angle θ_R is adjusted effectively with minimal $\overrightarrow{V_R}$ magnitude changes, hence in this mode the main object is real power control;
- With $\overrightarrow{V_c}$ in phase with $\overrightarrow{V_R}$ (Fig. 6.4(b)), the $\overrightarrow{V_R}$ magnitude is tuned effectively while θ_R remains the same, thus achieve reactive power control mode;
- With $\overrightarrow{V_c}$ in quadrant with $\overrightarrow{I_L}$ (Fig. 6.4(c)), the series voltage source acts as an inductive/capacitive elements when it leads/lags $\overrightarrow{I_L}$ by 90°. Therefore, the effective line impedance can be controlled and as well as the losses.

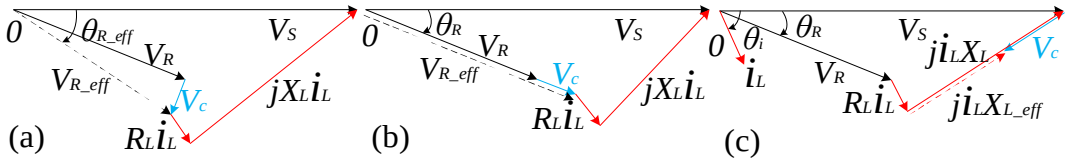


Fig. 6.4 Power flow control phasor diagrams: (a) phase shifting and real power control; (b) voltage magnitude and reactive power control; (c) line impedance control

6.2.2 Series-connected VSC - SSSC model and control principle

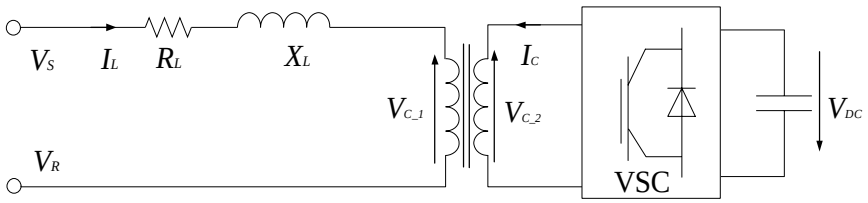


Fig. 6.5 Single line system with VSC-SSSC circuit

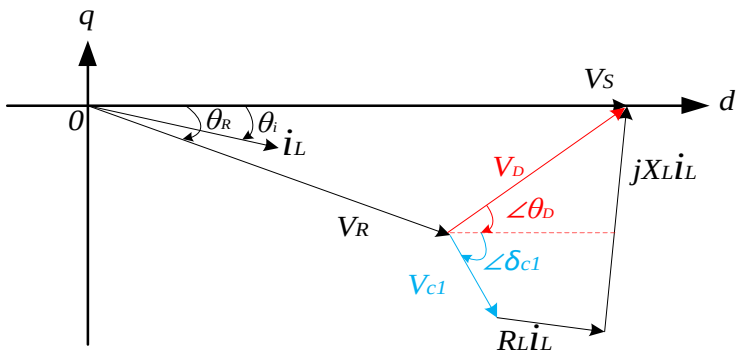


Fig. 6.6 SSSC phasor diagram

The series connected VSC of the UPFC, also known as the Static Synchronous Series Compensator (SSSC), belongs to the family of FACTs. A single-line equivalent circuit of this series connected converter is as shown in Fig. 6.5 and the corresponding phasor diagram is drawn in Fig. 6.6. The sending bus V_s is set as the reference phasor and the phase angle between the receiving bus voltage V_R and sending bus V_S is θ_R, and the series transformer inductance and resistance are negligible compared to transmission line impedance. The SSSC injects a series voltage $V_{c1}\angle\delta_{c1}$between the two buses to control the transmission line real and reactive power flow. The magnitude of V_{c1} is determined by the VSC terminal voltage and transformer ratio while its angle δ_{c1} can vary between 0-360°. Therefore, it can have any of the three modes illustrated in the previous subsection.

With a fixed rating SSSC (determined by the VSC DC side voltage V_{DC} and transformer ratio) it is important to observe the maximum controllable power flow margin between the two buses by this device, which relates on the transmission line impedance. On the other hand knowing the transmission line power margins helps to predict the suitable SSSC ratings. Such evaluation reveals the indication of SSSC cost when a specific power margin is given.

6.2.2.1 Assessment of power flow operation range

The following study investigates the relationship between the power margins and SSSC terminal voltage magnitude V_{c1} and its phasor's angle $\angle\delta_{c1}$. According to the phasor diagram shown in Fig. 6.6, the equations below can be derived.

$$\overrightarrow{V_D} = \overrightarrow{V_s} - \overrightarrow{V_R} = \overrightarrow{V_{c1}} + R_L\overrightarrow{i_L} + L_L\frac{d\overrightarrow{i_L}}{dt} \tag{6.8}$$

Taking $\overrightarrow{V_s}$ as the reference vector in synchronous reference frame, the voltage difference between V_s and V_R in dq form can be expressed as

$$\begin{cases} V_{Dd} = V_s - V_R \cos\theta_R \\ V_{Dq} = V_R \sin\theta_R \end{cases} \tag{6.9}$$

$$\theta_D = \tan^{-1} \frac{V_R \sin\theta_R}{V_s - V_R \cos\theta_R} \tag{6.10}$$

Having SSSC connected into the transmission line the relationship between its voltage V_{c1}, line current i_L and its impedance can be illustrated as

$$\begin{cases} V_{Dd} = V_{c1} \cos\delta_{c1} + R_L i_L \cos\theta_i - X_L i_L \sin\theta_i \\ V_{Dq} = V_{c1} \sin\delta_{c1} + R_L i_L \sin\theta_i + X_L i_L \cos\theta_i \end{cases} \tag{6.11}$$

The current of the equation (6.11) can be further derived as

$$\begin{cases} i_L \cos\theta_i = i_{Ld} = \frac{R_L(V_s - V_{Rd} - V_{c1d}) + X_L(V_{Rq} - V_{c1q})}{R_L^2 + X_L^2} \\ i_L \sin\theta_i = i_{Lq} = \frac{R_L(V_{Rq} - V_{c1q}) - X_L(V_s - V_{Rd} - V_{c1d})}{R_L^2 + X_L^2} \end{cases} \tag{6.12}$$

Since V_s is the reference, the real and reactive power flowing into the transmission line can be calculated as

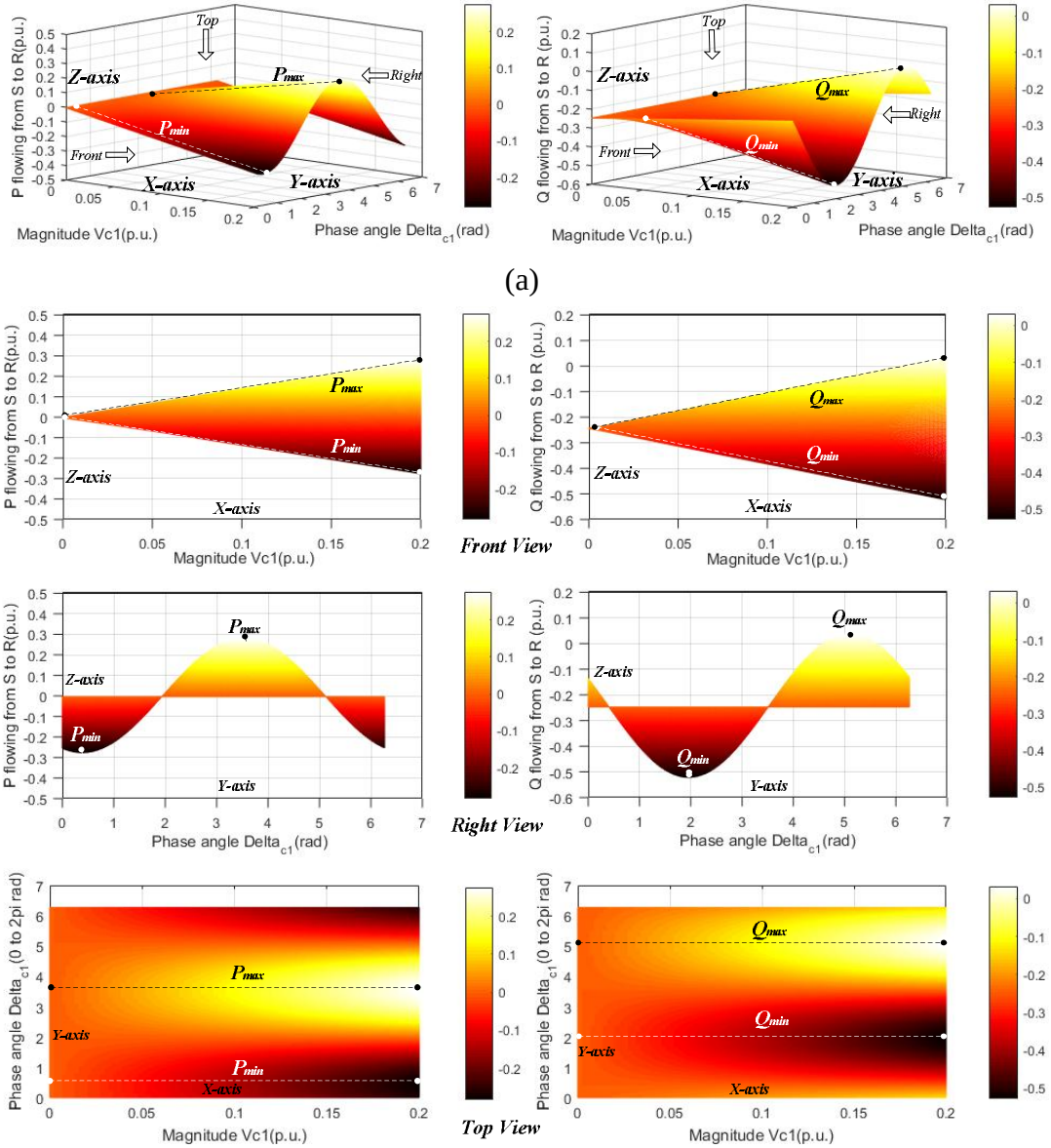
$$P_s = \frac{3}{2} \times \left(V_{sd} i_{Ld} + V_{sq} i_{Lq}\right) = \frac{3}{2} V_s i_{Ld} \tag{6.13}$$

$$Q_s = \frac{3}{2} \times \left(V_{sd} i_{Lq} - V_{sq} i_{Ld}\right) = \frac{3}{2} V_s i_{Lq} \tag{6.14}$$

Assuming the sending bus V_s is 11kV while the receiving bus voltage V_R is 5% magnitude dropped and 10° delayed; the transmission line length is 50km with resistance of 0.13Ω/km and reactance of 0.053Ω/km at 50Hz according to the UK power networks line impedance parameters under different voltage levels listed in the Appendix D.1. Hence the equivalent impedance of the line is (6.5+j2.65) Ω. The corresponding transmission line power rating is around 18.5MVA from summer to winter [126].

Consequently, taking 11kV and 18.5MVA as the base voltage and power respectively, assuming the VSC power rating is 20% of the power network, the relationship between the SSSC voltage magnitude V_{c1}, its phasor angle $\angle\delta_{c1}$ and the transmission line real power P_s and reactive power Q_s at sending end can be drawn graphically via 3-D plots, as shown in Fig. 6.7(a). The *X*-axis is the v_{c1} magnitude in p.u., *Y*-axis is the δ_{c1} phase angle and *Z*-axis is either P_s or Q_s in p.u.. The 3-D diagram confirms that the real and reactive power boundaries exist, where the black dotted lines refer to the +ve maximum power values transfer from sending to receiving bus (+ve margin, P_{max} and Q_{max}) while the white dotted lines denote those from receiving to sending bus (-ve margin, P_{min} and Q_{min}), thus the margins of the real and reactive power flowing can be known respectively. In Fig. 6.7(b), the view directions of the 3-D plot are from front, right and top respectively. From the different views it can be concluded two points as follow:

- The margins are increased/decreased relating to the injected SSSC voltage magnitude. They are proportional to the V_{c1};
- The SSSC voltage phasor angles are fixed when transfer maximum real or reactive power. Table 6.1 lists the SSSC angles $\angle\delta_{c1}$ which correspond to the real and reactive power margins.



(a)

Fig. 6.7 (a) 3-D Plot of power flow margin of transmission line with SSSC operation (b) Different views of the 3-D Plot

Table 6.1 SSSC angles of the real and reactive power margins of transmission line

Real power P	+ve margin	$\angle\delta_{c1} = 3.49rad$
	-ve margin	$\angle\delta_{c1} = 0.38rad$
Reactive power Q	+ve margin	$\angle\delta_{c1} = 5.10rad$
	-ve margin	$\angle\delta_{c1} = 1.95rad$

6.2.2.2 SSSC power flow control

The control of power flow along the transmission line using SSSC is based on the assumption that the sending end voltage is balanced and maintained at constant rated level and is set as the reference with V_{Sq} = 0. Real and reactive powers P_s and Q_s are determined by the sending end voltage and current flowing through the line. Fig. 6.8 shows the control block diagram. The required *P* and *Q* are applied as references and thus the *dq* reference current components i_{Sd}^*, i_{Sq}^* can be derived according to Equations (6.13) and (6.14). Note these are the transmission line current values, and can be converted to the converter side current values according to the series transformer turns ratio. Once the reference currents are obtained the predictive control algorithm presented in chapter 3 is adopted to generate the reference voltage for the control of VSC. Thus the required reference voltage vector V_{c1}^* at the next sampling time instant can be calculated according to the Equation (6.15), while its *dq* form are given as (6.16).

$$\overrightarrow{V_{c1}^*}(k) = \overrightarrow{V_s}(k) - \overrightarrow{V_R}(k) - \left[\frac{L_L}{T_s}\right]\overrightarrow{\imath_s^*}(k) + \left[\frac{L_L}{T_s} - R_L\right]\overrightarrow{\imath_s}(k) \tag{6.15}$$

$$\begin{bmatrix}\overrightarrow{V_{c1\_d}^*}(k)\\ \overrightarrow{V_{c1\_q}^*}(k)\end{bmatrix} = \begin{bmatrix}\overrightarrow{V_{s\_d}}(k)\\ \overrightarrow{V_{s\_q}}(k)\end{bmatrix} - \begin{bmatrix}\overrightarrow{V_{R\_d}}(k)\\ \overrightarrow{V_{R\_q}}(k)\end{bmatrix} - \begin{bmatrix}\frac{L_L}{T_s} & 0\\ 0 & \frac{L_L}{T_s}\end{bmatrix}\begin{bmatrix}\overrightarrow{\imath_{s\,d}^*}(k)\\ \overrightarrow{\imath_{s\,q}^*}(k)\end{bmatrix} + \begin{bmatrix}\frac{L_L}{T_s} - R_L & -\omega L_L\\ \omega L_L & \frac{L_L}{T_s} - R_L\end{bmatrix}\begin{bmatrix}\overrightarrow{\imath_{s\,d}}(k)\\ \overrightarrow{\imath_{s\,q}}(k)\end{bmatrix} \tag{6.16}$$

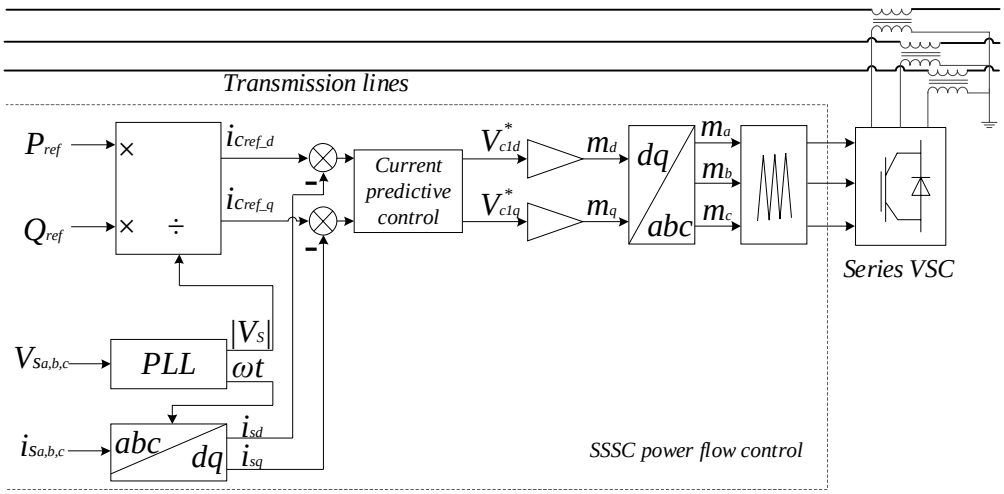
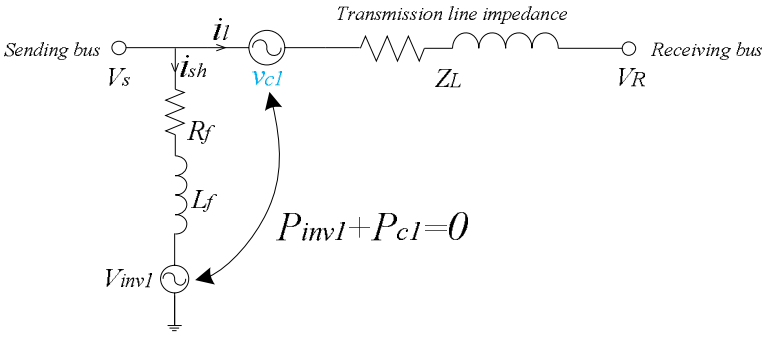


Fig. 6.8 SSSC power flow control block diagram

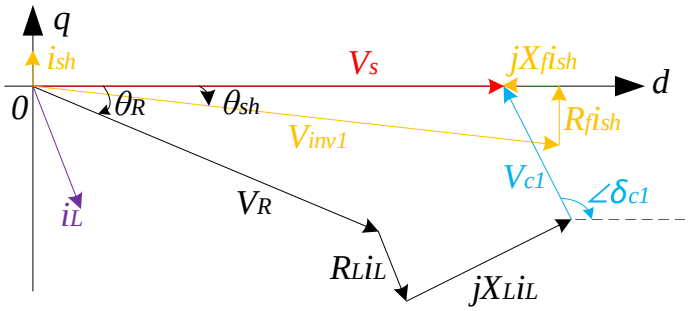
6.2.3 UPFC control

As explained above, a UPFC is a combination of two VSCs: one functions as a STATCOM and the other as a SSSC. The one-line simplified circuit of the UPFC is shown in Fig. 6.9(a). Assuming the transmission line sending bus V_s is constant and balanced. The shunt VSC V_{inv1} is connected to V_S through an interface transformer with equivalent resistance R_f and inductance L_f, while the other VSC V_{c1} is connected with the transmission line via a series transformer. The shunt VSC draws real power from the grid and supports for the series VSC via their DC-link. The real power exchange between two VSCs should be zero. Meantime, power flow of the

transmission line is controlled by the V_{c1} and the margins are the same as the SSSC explained in the previous subsection.



(a)



(b)

Fig. 6.9 UPFC (a) simplified circuit and (b) its phasor diagram

The phasor diagram for system with the UPFC is shown in Fig. 6.9(b). The sending end voltage is taken as the reference hence its phase angle is 0°. The shunt VSC voltage is $V_{inv1}\angle\theta_{sh}$. The magnitude and angle of the line current i_s flowing from sending to receiving end can be controlled through adjusting the series VSC voltage $V_{c1}\angle\delta_{c1}$. The voltage equation set for the two converters can be derived as

$$\begin{cases} \overrightarrow{V_{inv1}} = \vec{V_s} - R_f\vec{i}_{sh} - L_f\dfrac{d\vec{i}_{sh}}{dt} \\ \overrightarrow{V_{c1}} = \vec{V_s} - \vec{V_R} - R_L\vec{i_s} - L_L\dfrac{d\vec{i_s}}{dt} \end{cases} \tag{6.17}$$

where R_L and L_L represent transmission line impedance, neglecting series transformer internal impedance. Applying the predictive control algorithm for both converters to regulate their corresponding currents, the reference voltage equations for STATCOM VSC and SSSC VSC are given as Equation (6.18). The overall control system block diagram is shown in Fig. 6.10, as can be seen the SSSC control part is same as that in Fig. 6.8.

$$\begin{cases} \overrightarrow{V_{inv1}}^{*}(k) = \vec{V_s}(k) - \left[\dfrac{L_f}{T_s}\right]\overrightarrow{i_{sh}^{*}}(k) + [\dfrac{L_f}{T_s} - R_f]\overrightarrow{i_{sh}}(k) \\ \overrightarrow{V_{c1}}^{*}(k) = \vec{V_s}(k) - \vec{V_R}(k) - \left[\dfrac{L_L}{T_s}\right]\overrightarrow{i_s}^{*}(k) + [\dfrac{L_L}{T_s} - R_L]\vec{i_s}(k) \end{cases} \tag{6.18}$$

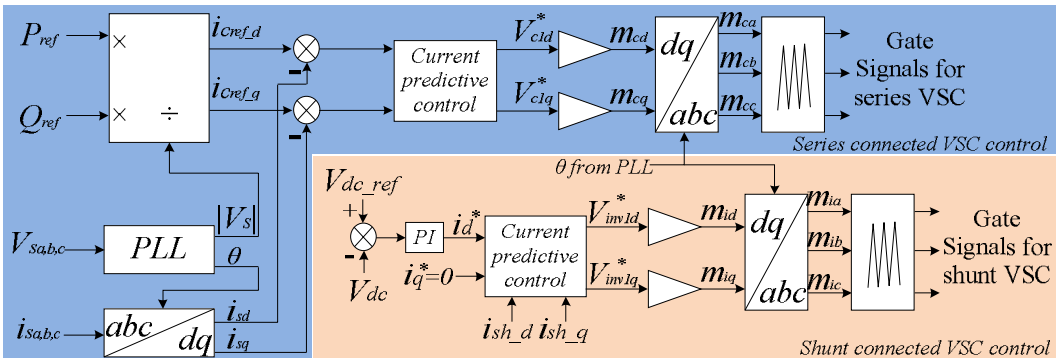


Fig. 6.10 UPFC control system blocks diagram

6.3 MMCC-based UPFC system

For voltages higher than 11kV, a step-up transformer is necessary for STATCOM part of UPFC to provide voltage matching and galvanic isolation between the VSC and transmission line. However, the requirement of a bulky transformer increases cost, losses and footprint [127]. To eliminate the disadvantages several alternative UPFC topologies have been investigated [128-132], but they still have drawbacks such as requiring bulky transformers on both sides. For example, the authors in [129] proposed a direct power control for a three-phase matrix converter-based unified power flow controller which allows the direct power conversion without any DC storage links; another configuration proposed in [131] adopts multiple small-size single-phase converters to instead of the large three-phase series converter in the UPFC. The large number of series converters provides redundunacy hence reliabiltiy, but the cost also increases. In 2012, the authors of [132] designed an UPFC application based on the Double-Star Chopper Cell (DSCC) moular multilevel converter (MMC). In this structure, both the shunt and series sides are comprised of DSCCs and they are connected via a common DC link, therefore, the converter switching frequency is reduced and as well as losses. However, the applying of double-star increase a lot cost, footprint and control complexicity.

This section proposes a novel configuration of UPFC based on a single-star modular multilevel cascaded converter (MMCC) [110-113]. The MMCC has the flexibility of meeting the required voltage levels without using a transformer. Its other benefits are well-known including the modular structure and reduced converter switching frequency hence losses and cost. The structure of this MMCC-based UPFC and its working principle are presented as follow.

6.3.1 Circuit configuration

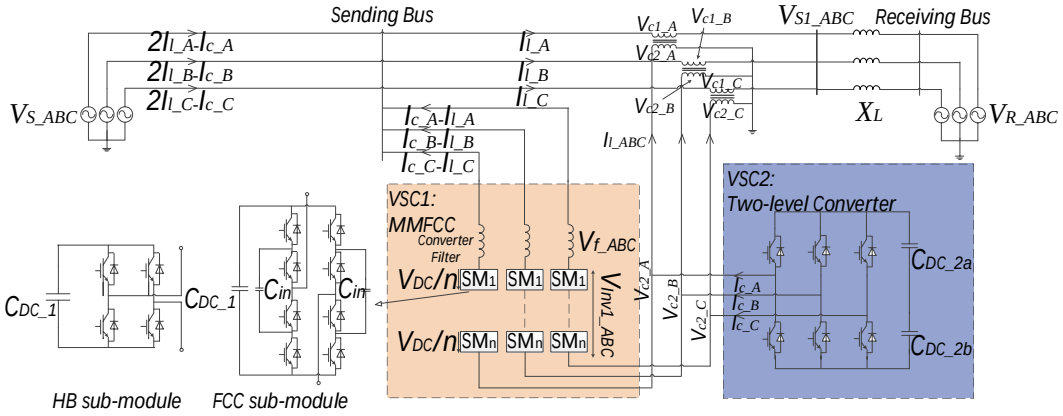


Fig. 6.11 3-phase transmission system with novel MMCC-UPFC circuit diagram

The structure of the MMCC-based UPFC is shown in Fig. 6.11. The VSC2 is still a three-phase 2-level voltage source inverter and its 3 phases' AC sides are connected to a transformer whose primary side windings are connected in series with the transmission lines. A 3-phase MMFCC is shunt connected with the transmission line in Fig. 6.11 as VSC1. Each SM is the same as the APC introduced in the previous chapters. According to device voltage ratings, more than two SM numbers may be added to meet the 11kV line voltage rating. Unlike the conventional UPFC, there is no DC-link shared between the two VSCs and they are linked instead on the AC side. This structure has the following features:

- Full modularity and flexibility in adjusting voltage levels since each submodule can be individually controlled and bypassed when fault occurs.
- Shunt connected to the transmission line through an inductor filter, thus no transformer at the shunt part is required.
- Not shared capacitors between the shunt MMCC and the series VSC, but each SM has its own capacitors.

6.3.2 Phasor diagram and operating principle

The equivalent circuit of the proposed MMCC-UPFC with its voltage and current phasor diagram are illustrated in Figs. 6.12 and 6.13. Assume the series transformer is Y-Y connected and turns ratio is 1 in order to simplify the control scheme but not affect the operation principle. A desired $V_{c2}\angle\delta$ determined by the line power flow values is generated at the converter side. This will be converted to $V_{c1}\angle\delta$ of the same phase angle and magnitude at the transmission line side. The current flowing out from the series-connected converter is $\overrightarrow{I_c}$, which should be in quadrature with its voltage $\overrightarrow{V_{c2}}$, assuming zero real power in and out of converter hence it is entirely reactive.

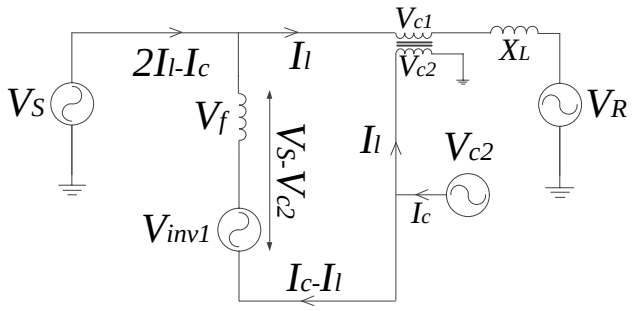


Fig. 6.12 MMCC-UPFC equivalent circuit

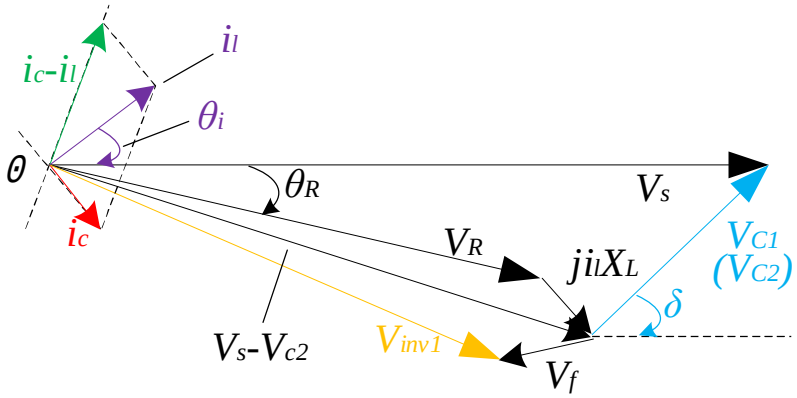


Fig. 6.13 UPFC voltage and current phasor diagram

Moreover, the shunt converter voltage $\overrightarrow{V_{inv1}}$ is in between of the sending bus voltage $\overrightarrow{V_S}$ and series converter voltage $\overrightarrow{V_{c2}}$ thus can be written as $(\overrightarrow{V_s} - \overrightarrow{V_{c2}})$ excluding inductor filter voltage drop $\overrightarrow{V_f}$. Assuming no real power flow the current injected to the line by the MMCC is according to the series converter and transmission line current as $(\overrightarrow{I_c} - \overrightarrow{I_l})$, which should also be perpendicular with its voltage $\overrightarrow{V_{inv1}}$, and therefore entirely reactive.

Though both current flows in both MMCC and series VSC are assumed reactive to their respective voltages, losses in both inverter devices exist which needs to be compensated hence maintain their capacitor voltage balance. Thus an additional real power control is required in order to compensate the losses, which is expected to generate exact current for the purpose of zero active power exchange between the two converters.

6.4 Analysis of MMCC-UPFC System Control

6.4.1 Series converter reference voltage generation

In the Subsection 6.2.2.2, the series VSC reference voltage calculation is based on using the current predictive control scheme, however, the series VSC generated voltage is required to be quadrant with its current in this MMCC-UPFC system, hence this scheme is no longer suitable. This subsection shows an alternative way to calculate the reference voltage of series VSC.

Since the control of transmission line power flow depends on the voltage $\overrightarrow{V_{c1}}$ which is transformed from the series converter generated voltage $\overrightarrow{V_{c2}}$ (Note that all the calculations take the sending bus voltage $\overrightarrow{V_s}$ as the reference), the equation for real and reactive powers flowing under the UPFC control can be derived as

$$P_{ref} + jQ_{ref} = \overrightarrow{V_R}\overrightarrow{I_l}^* = \overrightarrow{V_R}\left(\frac{\overrightarrow{V_S}-\overrightarrow{V_R}-\overrightarrow{V_{c1}}}{jX_L}\right)^* = \left[\frac{V_R V_{c1}\sin(\theta_R-\delta)-V_S V_R \sin\theta_R}{X_L}\right] + j\left[\frac{V_S V_R\cos\theta_R - V_R^2 - V_R V_{c1}\cos(\theta_R-\delta)}{X_L}\right] \tag{6.19}$$

Initially, without the UPFC control, the power flow of the transmission line under the same condition is

$$P_0 + jQ_0 = \frac{-V_S V_R \sin\theta_R}{X_L} + j\frac{V_S V_R\cos\theta_R - V_R^2}{X_L} \tag{6.20}$$

Therefore, the 'injected' real and reactive power by the UPFC device can be calculated as

$$\begin{cases} P_C = P_{ref} - P_0 = \frac{V_R V_{c1}\sin(\theta_R-\delta)}{X_L} \\ Q_C = Q_{ref} - Q_0 = \frac{-V_R V_{c1}\cos(\theta_R-\delta)}{X_L} \end{cases} \tag{6.21}$$

From the above equation set, the required magnitude V_{c1} and angle δ can be illustrated as

$$V_{c1} = \frac{X_L}{V_R}\sqrt{P_C^2 + Q_C^2} = \frac{X_L}{V_R}\sqrt{\left(P_{ref} + \frac{V_S V_R\sin\theta_R}{X_L}\right)^2 + \left(Q_{ref} - \frac{V_S V_R\cos\theta_R - V_R^2}{X_L}\right)^2} \tag{6.22}$$

$$\delta = \theta_R - \arctan\left(\frac{P_C}{Q_C}\right) = \theta_R - \arctan\left(\frac{P_{ref}+\frac{V_S V_R\sin\theta_R}{X_L}}{Q_{ref}-\frac{V_S V_R\cos\theta_R - V_R^2}{X_L}}\right) \tag{6.23}$$

The series converter reference voltage $\overrightarrow{V_{c\_ref}}$ thus can be derived by the above magnitude V_{c1} and its angle δ, $\overrightarrow{V_{c\_ref}} = V_{c1}\angle\delta$.

6.4.2 Shunt MMCC reference current generation

According to the previous subsection, the series converter generated voltage is $\overrightarrow{V_{c2}}\angle\delta$, $\angle\overrightarrow{I_c} = \delta - 90°$. The $\overrightarrow{I_c}$ magnitude thus can be derived as follow.

The active power flowing into the shunt MMCC is assumed to be zero and the Equation (6.24) hence can be derived.

$$P_1 = 0 = \left(\overrightarrow{V_s} - \overrightarrow{V_{c2}} - \overrightarrow{V_f}\right)\times\left(\overrightarrow{I_c} - \overrightarrow{I_l}\right) = \left(\overrightarrow{V_s} - \overrightarrow{V_{c2}} - Z_f\left(\overrightarrow{I_c} - \overrightarrow{I_l}\right)\right)\times\left(\overrightarrow{I_c} - \overrightarrow{I_{ll}}\right) = Z_f {I_c}^2 - V_s I_c\sin\delta + V_s I_l\cos\theta_i + Z_f {I_l}^2 - V_{c2} I_l\cos(\delta-\theta_i) \tag{6.24}$$

Therefore, I_c can be regarded as the only unknown of the above quadratic equation.

$$\Delta = (V_s \sin\delta)^2 - 4Z_f(V_s I_l \cos\theta_i + Z_f {I_l}^2 - V_{c2} I_l \cos(\delta - \theta_i)) \quad (6.25)$$

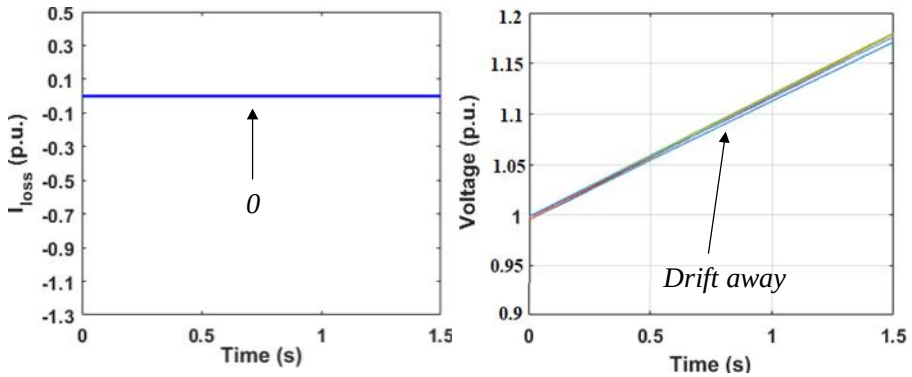
The equation is effective only when $\Delta \geq 0$, otherwise there is no solution of I_c, which means the UPFC cannot work under that condition.

$$I_c = \frac{V_s \sin\delta \pm \sqrt{\Delta}}{2Z_f} \quad (6.26)$$

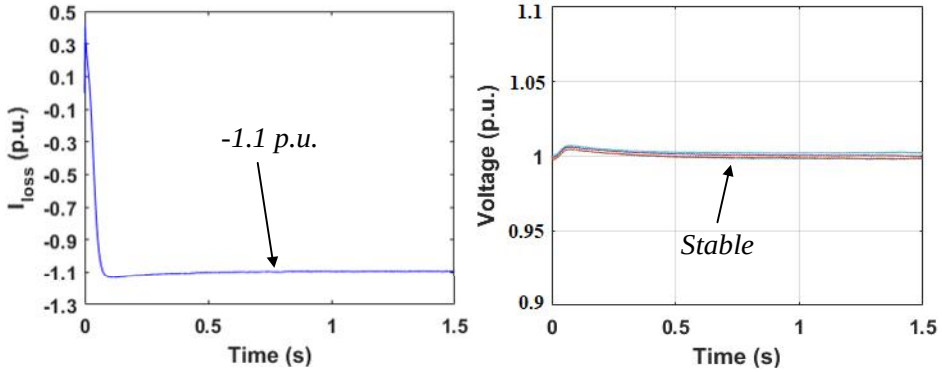
Therefore, $\overrightarrow{I_c} = \frac{V_s \sin\delta \pm \sqrt{\Delta}}{2Z_f} \angle\delta - 90°$ and the shunt MMCC generating current $(\overrightarrow{I_c} - \overrightarrow{I_l})$ can also be decided.

However, the converter losses which draws real power cannot be neglected, hence its voltage and current cannot be absolute quadrature and always have a phase shift smaller than 90°. An additional overall DC capacitors voltage control is added into the control scheme to compensate this part of real power losses. This prevent the DC capacitors of the MMCC and series converter drifting away from their nominal values.

To compensate the phase shift it is necessary to calculate the total converter losses conductance G_{loss} which draws real power, this is achieved by using the average of total SM DC capacitor voltages comparing with the reference value, consequently the output is regulated to the real power losses P_{loss} through a PI controller, and then being divided by the square of MMCC voltage rms value. Then, the product of G_{loss} and the MMCC voltage $\overrightarrow{V_{inv1}}$ is the current $\overrightarrow{I_{loss}}$ which should be in phase with $\overrightarrow{V_{inv1}}$ hence can be regarded as active component. It is required for compensating the losses and added into the $(\overrightarrow{I_c} - \overrightarrow{I_l})$ to generate the corresponding reference current I_{ref}. Fig. 6.14 shows the comparative results without and with the additional DC capacitors voltage control loop, which can be found that the DC capacitors voltage can be maintained at their nominal value when the I_{loss} added in while it will drift away when the current is zero.



(a)



(b)

Fig. 6.14 The I_{loss} current (left) and MMCC submodule DC capacitor voltages (right) (a) without and (b) with overall DC capacitor voltage control

After the shunt MMCC reference current decided, the predictive controller is adopted to generate its reference voltage V_{inv1}^{*}, which is based on the equations given by (6.17) and (6.18).

6.5 MMCC-UPFC control strategies

The overall control strategies and corresponding flowchart are illustrated in Figs. 6.15 and 6.16. The implemented control scheme is divided into two main parts:

- Control the series converter AC voltages in order to regulate the power flows from sending to the receiving buses at the desired values. This requires calculating the required V_{c_ref} according to the reference real and reactive power commands. V_s is set as the reference voltage of the series converter.
- Regulate the current flow through the shunt MMCC for regulating the sending line voltage at the constant required level. This requires calculating the $(\vec{I_c} - \vec{I_l})$. For maintaining both SM and series converter DC capacitor voltages balanced, it requires calculating $\overrightarrow{I_{loss}}$ via feedback control of the overall DC capacitor voltage.

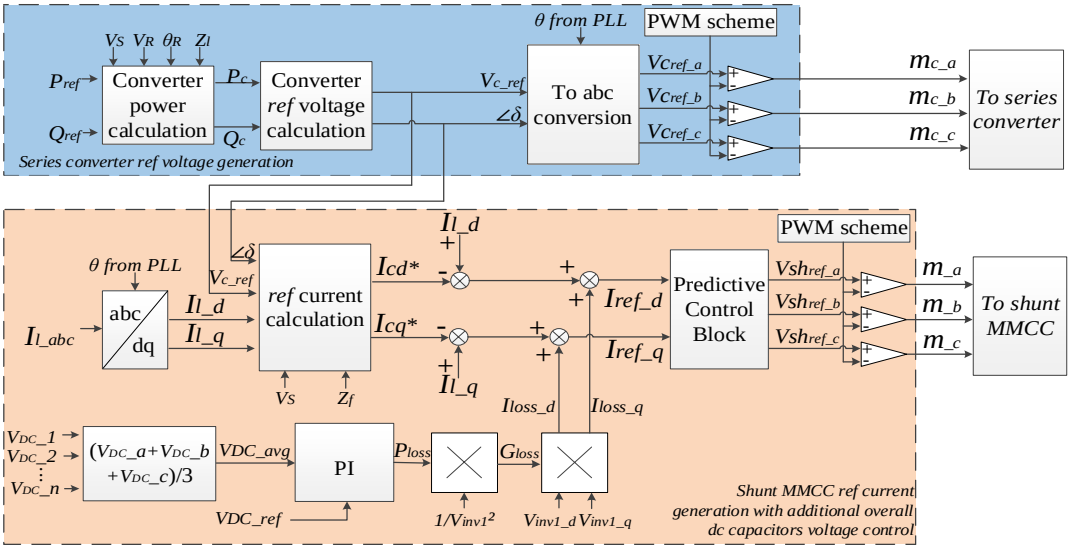


Fig. 6.15 MMCC-UPFC control block diagram

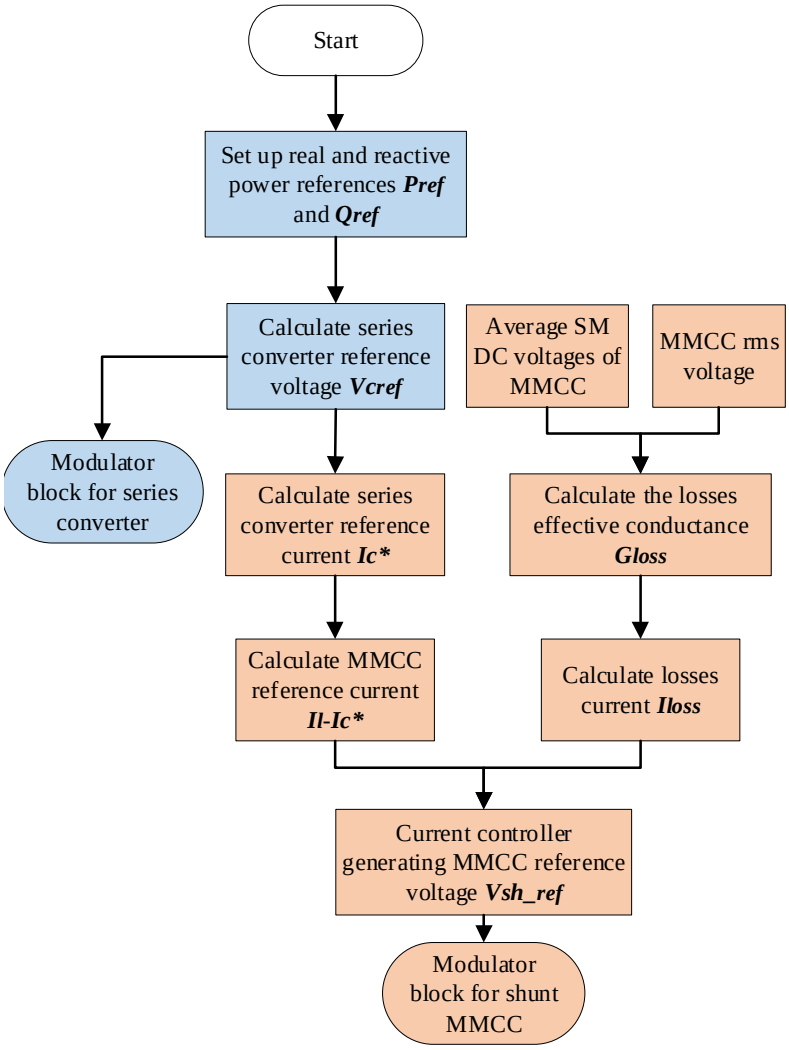


Fig. 6.16 Flowchart of MMCC-UPFC control schemes

The flowchart shows the routine for implementing the UPFC control scheme: It sets up the P_{ref} and Q_{ref} commands and then calculates series VSC reference voltage. Then, the MMCC reference current is derived in order to maintain zero active power exchange. Meantime, an extra feedback current I_{loss} is also added into the MMCC reference current to compensate for the real power losses. Thereafter, the MMCC reference voltage is calculated and send to modulator.

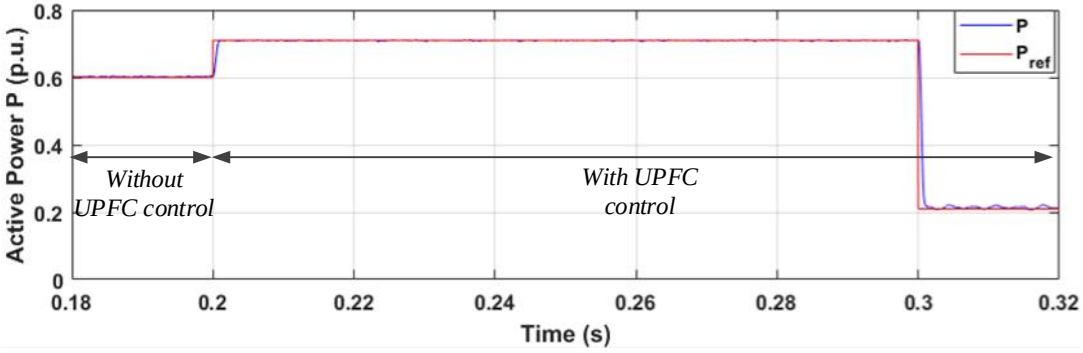
6.6 Simulation Results

The proposed MMFCC-UPFC shown in Fig. 6.11 and the corresponding control schemes are verified through SIMULINK/MATLAB. The parameters of the power transmission system are listed in Table. 6.2: Three-phase voltage rating at the sending bus is 11kV, 50Hz; the MMFCC total DC voltage rating is 12.8kV containing 32 FCC submodules in each phase, while the DC capacitor voltage per submodule is 400V and the floating flying capacitors are rated at 200V. The series converter contains one DC capacitor and its voltage rating is 800V.

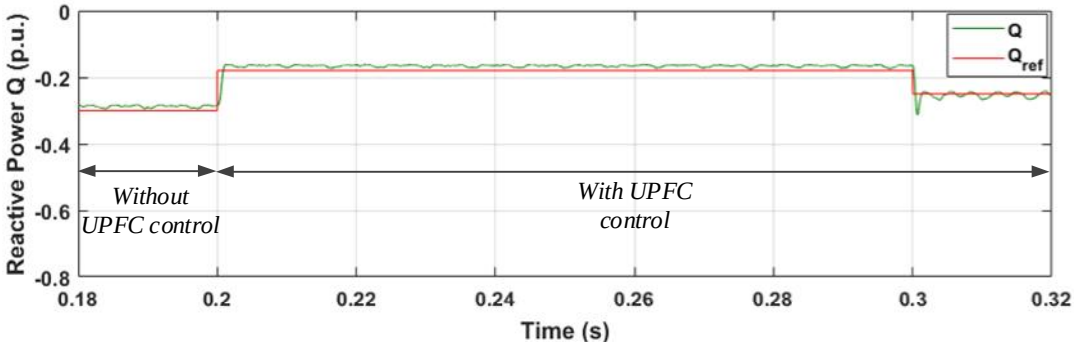
Table 6.2 MMCC-based UPFC circuit parameters

Components		Rating
PCC Side	3-Phase Source voltage V_s	11kV
	Fundamental frequency f_0	50 Hz
Transmission Line	Transmission line impedance Z_L	6.5Ω, 8.4mH
MMCC Side	Switching frequency f_{C1}	250 Hz
	SM numbers per phase	32
	RL Filter	1 Ω, 1.0 mH
	SM DC capacitor C_{dc}	1120 μF
	SM Flying capacitor C_{fc}	560 μF
	Nominal SM DC voltage V_{dc}	400 V
	3-Phase Rated Power S	18.5 MVA
Series Converter Side	Switching frequency f_{C2}	4 kHz
	Series transformer turn ratio $n_1:n_2$	10:1
	Series converter DC capacitor C_{dc_series}	560μF
	Nominal series converter DC voltage V_{dc_series}	622V

To validate the MMFCC-UPFC's ability in power flow control, the receiving end voltage is set to 10.45kV and phase angle 10° initially without MMFCC-UPFC, so the real and reactive power of the transmission line are 0.6p.u. and -0.3p.u from sending bus to receiving end. At 0.2 sec, the MMFCC-UPFC is switched on and the command real and reactive powers are changed to 0.71p.u. and -0.18p.u. As shown in Fig. 6.17, under UPFC control, the real and reactive powers transmitted to the receiving bus follow the command values closely. Similarly at 0.3sec the real power drops to 0.21p.u. and the reactive power changes to -0.25 p.u. according to the set reference values. Fig. 6.18 shows the corresponding UPFC real and reactive power P_c and Q_c injected to the line. Clearly the MMFCC-UPFC device can control both real and reactive powers of the transmission line to the required values precisely and fast.

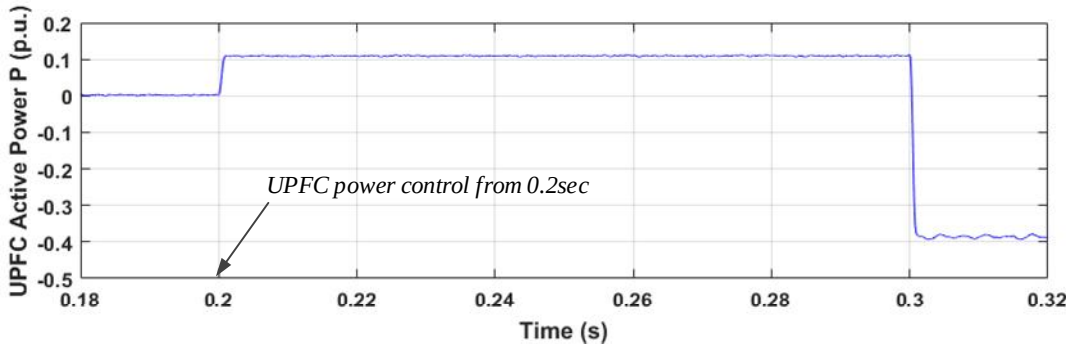


(a)

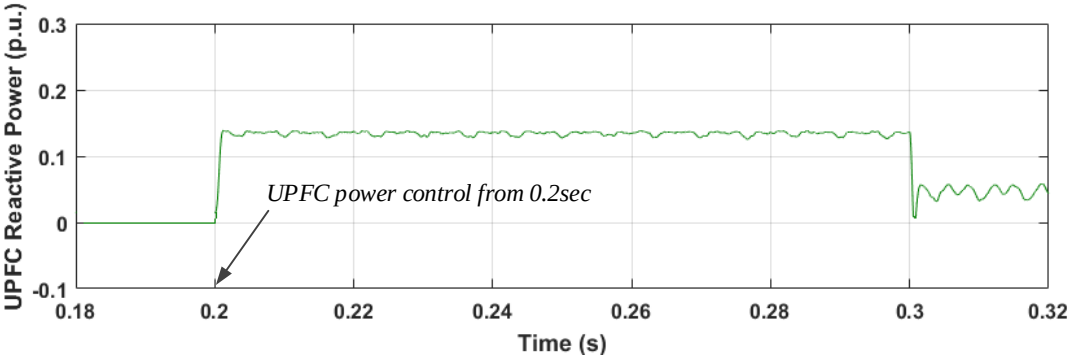


(b)

Fig. 6.17 Transmission line (a) Real power P and (b) Reactive Power Q with their reference commands



(a)



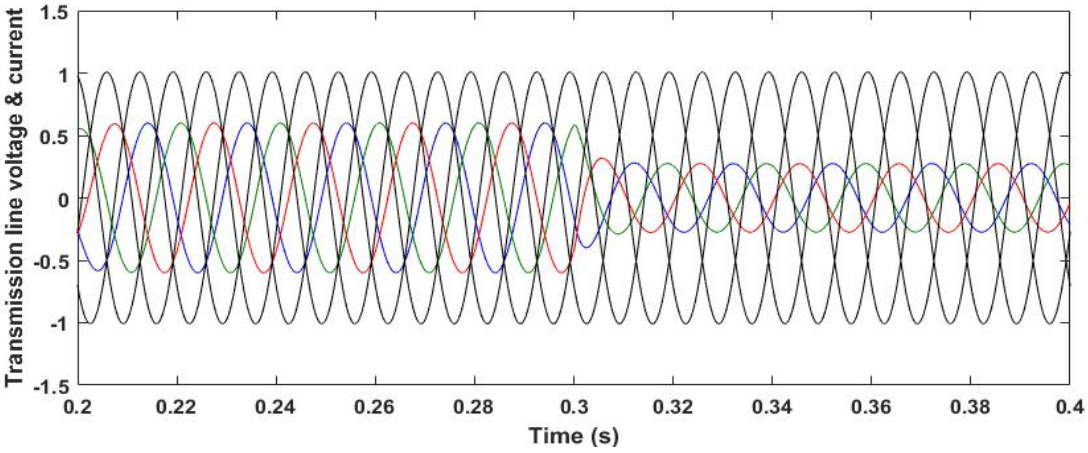
(b)

Fig. 6.18 MMFCC-UPFC (a) Real power P_c and (b) Reactive Power Q_c

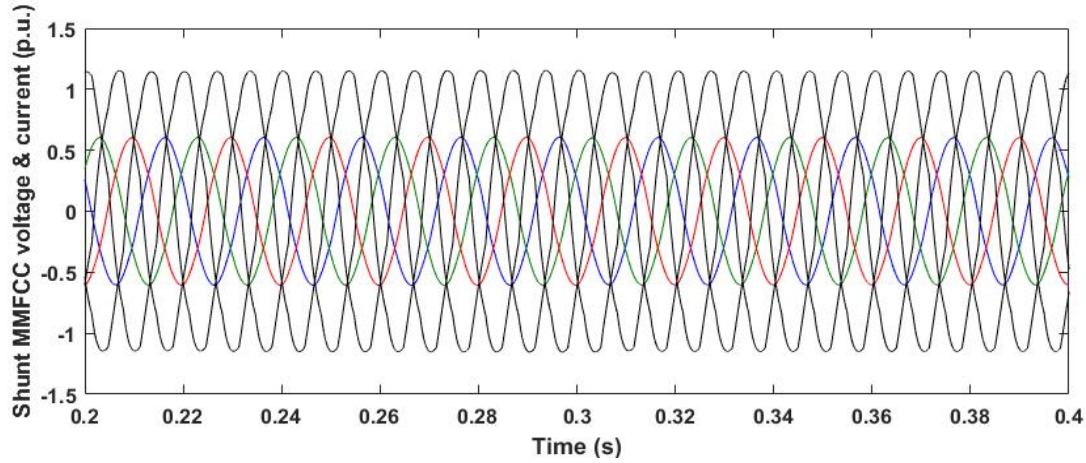
Fig. 6.19 shows the corresponding 3-phase voltages with their currents of the transmission line, UPFC shunt and series part respectively. As expected, the MMFCC controls its current (Fig.6.19(b)) to be equal to the difference between transmission line current (Fig.6.19(a)) and series converter's current (Fig.6.19(c)), which is ($\vec{I_c} - \vec{I_l}$). At 0.3sec, the magnitude of transmission line current reduced to around 0.3 p.u. due to the changing of real and reactive power command values, consequently the series part current decreases while the shunt part current remains the same, which indicates that the control schemes of both shunt and series converters are chained well and responding fast.

Meantime, Fig. 6.19 also illustrates that at the steady state the AC voltages of the two converters are in quadrature with their currents hence no active power exchange in

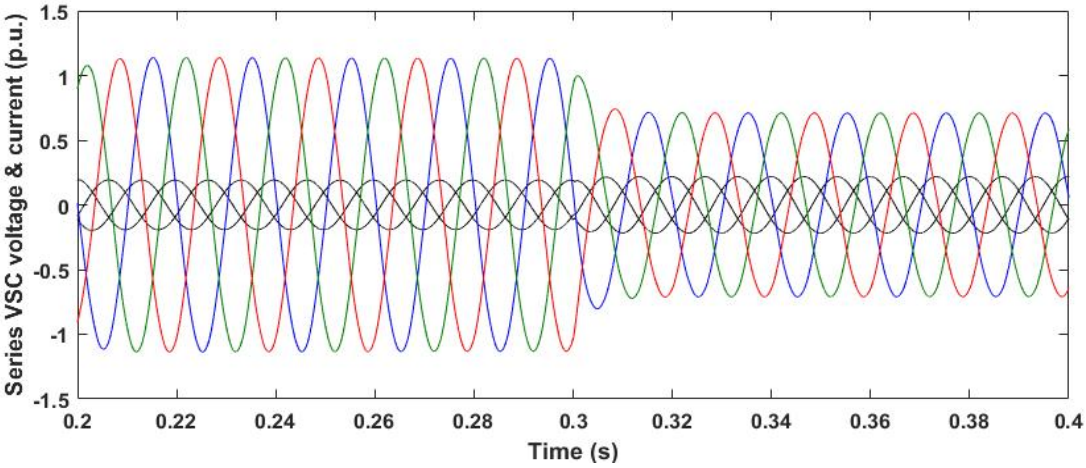
both converters, while the shunt MMFCC is inductive and series VSC is capacitive. Therefore, the MMFCC module DC capacitor voltages and the series VSC voltage are well maintained at their nominal value 1p.u. respectively, as shown in Fig. 6.20. Finally, the 3-phase MMFCC terminal multilevel voltage waveform is shown in Fig. 6.21.



(a) Transmission line 3-phase voltage (black) and current

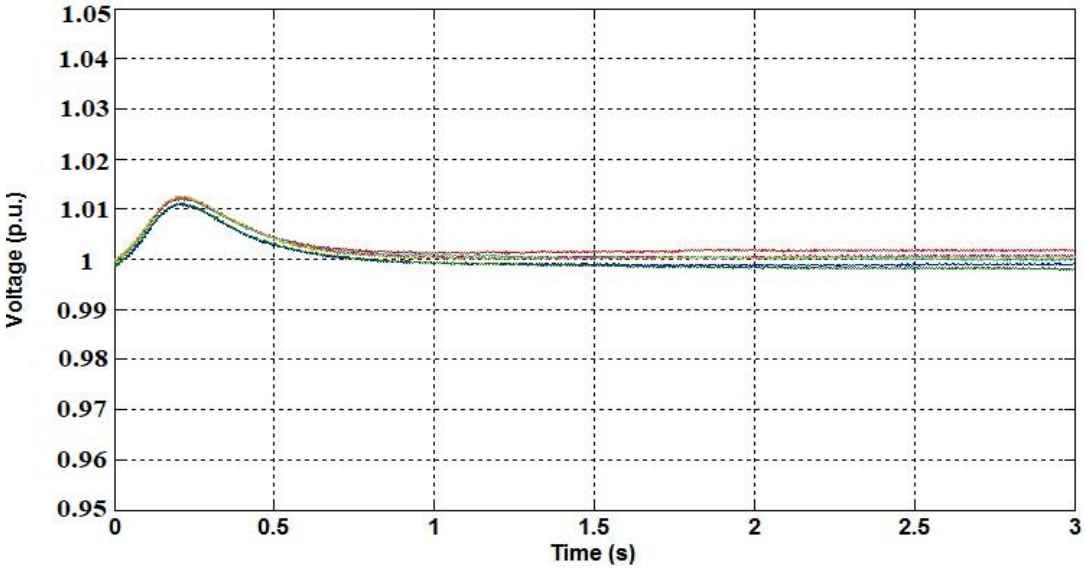


(b) Shunt part 3-phase voltage (black) and current

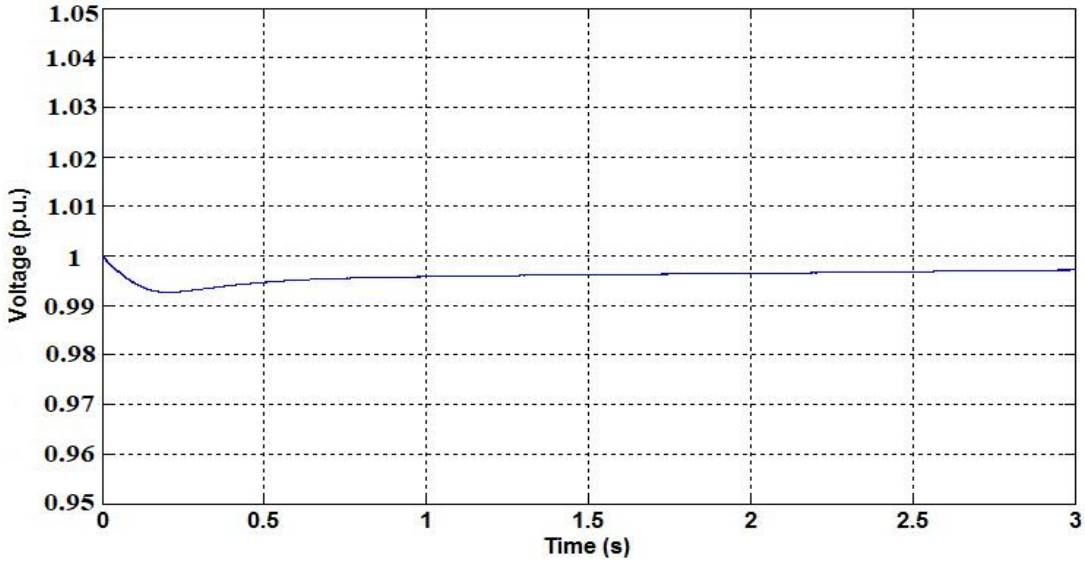


(c) Series part 3-phase voltage (black) and current

Fig. 6.19 MMFCC-UPFC system simulated 3-phase voltages and currents



(a)



(b)

Fig. 6.20 (a) Shunt MMCC and (b) series converter DC capacitors voltage

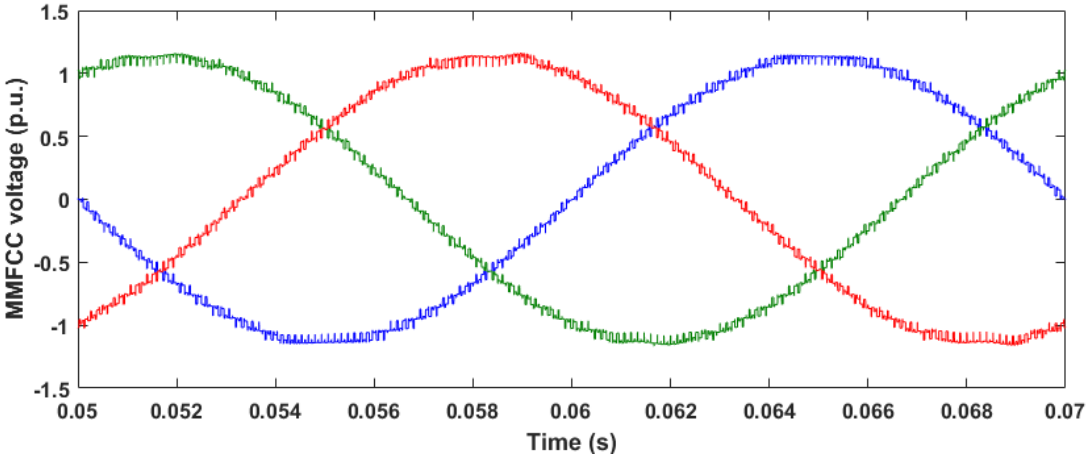


Fig. 6.21 3-phase MMFCC multilevel voltage waveform

6.7 Summary

A modular multilevel converter based unified power flow controller (UPFC) was proposed in this chapter to provide high flexibility, lower losses power flow control in the transmission system and remedy the disadvantages of conventional UPFC. The operating principle of this novel device and corresponding control schemes of the series converter voltage generation and shunt converter (MMCC) current regulation were explained. An overall DC capacitors voltage control is implemented to compensate the losses and ensures zero active power exchange between the two converters thus their DC capacitors voltage can be well balanced. Simulation results have shown that the device can react precisely to control the transmission line power to the required levels.

Chapter 7 Conclusions and Future Recommendations

7.1 Conclusions

This research has investigated the applications of Modular Multilevel Flying Capacitor Converter (MMFCC). One is as an Active Power Conditioner (APC) to compensate for harmonics, reactive power and unbalanced load current; the other is as a Unified Power Flow Controller (UPFC) to control the transmission line real and reactive power flow respectively. To the author's knowledge, no study has investigated the use of an MMCC for such FACTs applications. The research on MMFCC-based APC/UPFC via simulations and experimental validation has shown its capability of improving grid current/power quality, which helps to fill the knowledge gap in existing MMCC FACTs applications.

The main contributions and achievements of this research are summarised below:

- An investigation and comparison of different MMCC configurations and various submodule topologies in terms of footprint, cost and performance. From the assessment, it has been concluded that the single star configuration is the best choice for FACTs applications because of relative smaller size, lower cost and simpler control complexity compared to double star. Furthermore, the harmonics band and THDs comparison between the Phase Shift-PWM and Phase Disposed-PWM multilevel pulse width modulation schemes were also presented and it has been shown that PS-PWM has the potential to outperform PD-PWM in MMCC applications.

- A study was carried out to present a carrier permutation PS-PWM method applied on the MMFCC-based active power conditioner to avoid the unbalance of intra-cluster submodule capacitor voltages. Meantime, the abrupt rate-of-change in generation of current harmonics was solved by a predictive controller with a derivative action method. Finally, the simulation and experimental validations of the high quality harmonics filtering and reactive power control results were presented and agreed well with each other.

- One of the significant contributions of this research work is the development of a new reference current extraction scheme, which uses cascaded notch filters to eliminate only a selection of dominant low order harmonics in the load current. The method has been shown to have higher speed in tracking the harmonic variations and higher accuracy compared to the low-pass filter based scheme when the harmonics among the current three phases are unbalanced.

- For the MMFCC-based APC, the inter-cluster voltage balance issue due to phase power imbalance caused by compensating unbalanced load current was solved by injecting a common zero sequence voltage to the phase limbs of the SSBC-APC

and a zero sequence current for the SDBC-APC. The performance of these two types of APCs has been studied and compared via both simulation and experimental validation, shown that the SDBC has an extended operating range in unbalanced load compensation for level of load imbalance K_{ir} reaches 0.7 while SSBC could not perform properly when K_{ir} is 0.6.

- Another important contribution of this work is the design of a MMCC-based UPFC to provide real and power flow control in the transmission system. Unlike the UPFC using conventional converter topology, it has the advantages of full modularity and flexibility in adjusting voltage levels since each submodule can be individually controlled and bypassed when fault occurs, and no bulky transformer at the shunt part is required hence losses reduced. Finally, simulation results were presented and have shown that the device can react precisely to control the transmission line power to the required levels.

At the time of writing, three published conference papers have been derived from the work based on Chapter 3, 4 and 6. Two journal publications are under consideration based on Chapter 4 and 6. One journal paper is in preparation.

7.2 Future Recommendations

The current research can still be improved and extended to future research work. Suggestions are summarised as follow:

- The chosen of coefficient τ to scale the derivative term for the modified predictive controller method can be modified online via an adaptive intelligent algorithm. Consequently, the converter current controller can respond faster and provide a more accurate current regulation ability regardless how the load current harmonics change.

- Furthermore, the research of MMCC-based FACTs can be extended to the series-connected compensator and active power filter to control power flow in the grid and eliminate voltage harmonics.

- In addition, an investigation of how to improve the distorted zero sequence voltage waveform in SSBC can be made in order to extend the device operating range with regard to the level of load imbalance K_{ir}.

- Finally, the two-level voltage source converter in the series part of MMFCC-UPC can be replaced by a multilevel converter, thus more flexibility and lower losses can be achieved. However, additional control scheme in terms of capacitor voltage balancing may be required to improve the system reliability.

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Appendix A.1 Five-level Flying Capacitor Converter Submodule Operating States

State Inversion (IN) Rectification (RC)	Switching device state				Diode state				Output voltage V_{out}
	S_{1a}	S_{2a}	S_{3a}	S_{4a}	D_{1a}	D_{2a}	D_{3a}	D_{4a}	
	S_{1b}	S_{2b}	S_{3b}	S_{4b}	D_{1b}	D_{2b}	D_{3b}	D_{4b}	
IN	1	1	0	0	0	0	0	0	$+V_{DC}$
	0	0	1	1	0	0	0	0	
RC	0	0	0	0	1	1	0	0	
	0	0	0	0	0	0	1	1	
IN	0	0	1	1	0	0	0	0	$-V_{DC}$
	1	1	0	0	0	0	0	0	
RC	0	0	0	0	0	0	1	1	
	0	0	0	0	1	1	0	0	
IN	1	1	0	0	0	0	0	0	$+0.5V_{DC}$
	0	0	1	0	1	0	0	0	
RC	0	0	0	0	1	1	0	0	
	1	0	0	0	0	0	1	0	
IN	1	1	0	0	0	0	0	0	$+0.5V_{DC}$
	0	0	0	1	0	1	0	0	
RC	0	0	0	0	1	1	0	0	
	0	1	0	0	0	0	0	1	
IN	1	0	0	0	0	0	1	0	$+0.5V_{DC}$
	0	0	1	1	0	0	0	0	
RC	0	0	1	0	1	0	0	0	
	0	0	0	0	0	0	1	1	
IN	0	1	0	0	0	0	0	1	$+0.5V_{DC}$
	0	0	1	1	0	0	0	0	
RC	0	0	0	1	0	1	0	0	
	0	0	0	0	0	0	1	1	
-	1	1	0	0	0	0	0	0	0
	0	0	0	0	1	1	0	0	
-	0	0	0	0	1	1	0	0	
	1	1	0	0	0	0	0	0	
-	0	0	1	1	0	0	0	0	0
	0	0	0	0	0	0	1	1	
-	0	0	0	0	0	0	1	1	
	0	0	1	1	0	0	0	0	
-	0	0	1	0	1	0	0	0	0
	1	0	0	0	0	0	1	0	
-	1	0	0	0	0	0	1	0	
	0	0	1	0	1	0	0	0	
-	0	1	0	0	0	0	0	1	0
	0	0	0	1	0	1	0	0	
-	0	0	0	1	0	1	0	0	
	0	1	0	0	0	0	0	1	
IN	1	0	0	0	0	0	1	0	0
	0	0	0	1	0	1	0	0	
RC	0	0	1	0	1	0	0	0	
	0	1	0	0	0	0	0	1	
RC	0	0	0	1	0	1	0	0	0
	1	0	0	0	0	0	1	0	
IN	0	1	0	0	0	0	0	1	
	0	0	1	0	1	0	0	0	
	0	0	1	0	1	0	0	0	

IN	0	0	1	1	0	0	0	0	-0.5V_{DC}
RC	1	0	0	0	0	0	1	0	
	0	0	0	0	0	0	1	1	
IN	0	0	0	1	0	1	0	0	-0.5V_{DC}
	1	1	0	0	0	0	0	0	
RC	0	1	0	0	0	0	0	1	
	0	0	0	0	1	1	0	0	
IN	0	0	1	1	0	0	0	0	-0.5V_{DC}
	1	0	0	0	0	0	1	0	
RC	0	0	0	0	0	0	1	1	
	0	0	1	0	1	0	0	0	
IN	0	0	1	1	0	0	0	0	-0.5V_{DC}
	0	1	0	0	0	0	0	1	
RC	0	0	0	0	0	0	1	1	
	0	0	0	1	0	1	0	0	

Appendix B.1 Relationship of 3-phase Unbalanced Current

The 3-phase unbalanced current can be illustrated as

$$\begin{cases} i_a = i_{a1} + i_{a2} + i_{a0} \\ i_b = i_{b1} + i_{b2} + i_{b0} \\ i_c = i_{c1} + i_{c2} + i_{c0} \end{cases} \quad \text{(B.1)}$$

For the symmetrical systems, the phase shift from each other is 120° and may use a complex operator h=1∠120° to represent. Thus the positive sequence and negative sequence current phasors can be derived as (B.2) and (B.3) when considering I_{a1} and I_{a2}as reference.

$$\begin{cases} i_{a1} = I_{a1}\angle 0° \\ i_{b1} = I_{a1}\angle 240° = h^2 I_{a1} \\ i_{c1} = I_{a1}\angle 120° = h I_{a1} \end{cases} \quad \text{(B.2)}$$

$$\begin{cases} i_{a2} = I_{a2}\angle 0° \\ i_{b2} = I_{a2}\angle 120° = h I_{a2} \\ i_{c2} = I_{a2}\angle 240° = h^2 I_{a2} \end{cases} \quad \text{(B.3)}$$

Hence, the (B.1) equation can be re-written as

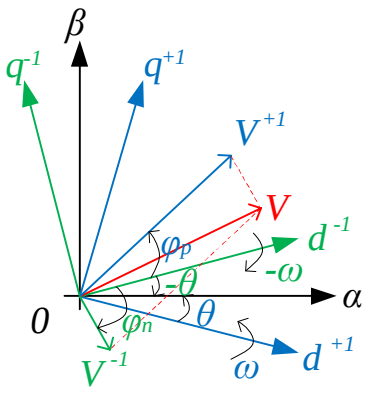
$$\begin{cases} i_a = I_{a1} + I_{a2} + I_{a0} \\ i_b = h^2 I_{a1} + h I_{a2} + I_{a0} \\ i_c = h I_{a1} + h^2 I_{a2} + I_{a0} \end{cases} \quad \text{(B.4)}$$

In matrix form, this can be expressed as

$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ h^2 & h & 1 \\ h & h^2 & 1 \end{bmatrix} \begin{bmatrix} I_{a1} \\ I_{a2} \\ I_{a0} \end{bmatrix} \quad \text{(B.5)}$$

Appendix B.2 Decoupled Double Synchronous Reference Frame-Phase Lock Loop

This PLL scheme is proposed by [2], which adopts two synchronous reference frames, dq^{+1} rotating with positive angular velocity ω and dq^{-1} rotating with negative angular velocity $-\omega$ respectively, namely double synchronous reference frames (DSRF). The corresponding phasor diagram is shown below.



Using the Clarke transformation, the unbalanced voltage vector can be given as

$$v_{\alpha\beta} = \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = v^+_{\alpha\beta} + v^-_{\alpha\beta} = V^+ \begin{bmatrix} \cos(\omega t + \varphi_p) \\ \sin(\omega t + \varphi_p) \end{bmatrix} + V^- \begin{bmatrix} \cos(-\omega t + \varphi_n) \\ \sin(-\omega t + \varphi_n) \end{bmatrix} \quad \text{(B.6)}$$

According to the above DSRF, (B.6) can be further expressed as

$$\begin{aligned} v^+_{dq} &= \begin{bmatrix} v^+_d \\ v^+_q \end{bmatrix} = \begin{bmatrix} \overline{v}^+_d \\ \overline{v}^+_q \end{bmatrix} + \begin{bmatrix} \tilde{v}^+_d \\ \tilde{v}^+_q \end{bmatrix} \\ &= \underbrace{V^+ \begin{bmatrix} \cos\varphi_p \\ \sin\varphi_p \end{bmatrix}}_{DC\ terms} + \underbrace{V^- \begin{bmatrix} \cos 2\omega t & \sin 2\omega t \\ -\sin 2\omega t & \cos 2\omega t \end{bmatrix} \begin{bmatrix} \cos\varphi_n \\ \sin\varphi_n \end{bmatrix}}_{AC\ terms} \end{aligned} \quad \text{(B.7)}$$

$$\begin{aligned} v^-_{dq} &= \begin{bmatrix} v^-_d \\ v^-_q \end{bmatrix} = \begin{bmatrix} \overline{v}^-_d \\ \overline{v}^-_q \end{bmatrix} + \begin{bmatrix} \tilde{v}^-_d \\ \tilde{v}^-_q \end{bmatrix} \\ &= \underbrace{V^- \begin{bmatrix} \cos\varphi_n \\ \sin\varphi_n \end{bmatrix}}_{DC\ terms} + \underbrace{V^+ \begin{bmatrix} \cos 2\omega t & -\sin 2\omega t \\ \sin 2\omega t & \cos 2\omega t \end{bmatrix} \begin{bmatrix} \cos\varphi_p \\ \sin\varphi_p \end{bmatrix}}_{AC\ terms} \end{aligned} \quad \text{(B.8)}$$

It can be seen that both +ve and –ve sequence *dq* voltage contain the AC cross coupling terms. These 2ωt matrices can be symbolised by

$$\left[T^{+2}_{dq}\right] = \left[T^{-2}_{dq}\right]^T = \begin{bmatrix} \cos 2\omega t & \sin 2\omega t \\ -\sin 2\omega t & \cos 2\omega t \end{bmatrix} \quad \text{(B.9)}$$

Hence the equations (B.7) and (B.8) can be rewritten as

$$\begin{aligned} v^+_{dq} &= \overline{v}^+_{dq} + \left[T^{+2}_{dq}\right]\overline{v}^-_{dq} \\ v^-_{dq} &= \overline{v}^-_{dq} + \left[T^{-2}_{dq}\right]\overline{v}^+_{dq} \end{aligned} \quad \text{(B.10)}$$

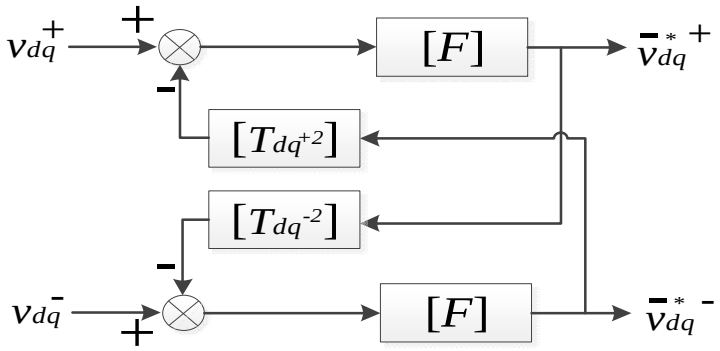
As a result, the estimated values at the output of the DDSRF are

$$\begin{aligned} {\overline{v}^*_{dq}}^+ &= [F]\{v^+_{dq} - \left[T^{+2}_{dq}\right]\overline{v}^-_{dq}\} \\ {\overline{v}^*_{dq}}^- &= [F]\{v^-_{dq} - \left[T^{-2}_{dq}\right]\overline{v}^+_{dq}\} \end{aligned} \quad \text{(B.11)}$$

where

$$[F] = \begin{bmatrix} LPF(s) & 0 \\ 0 & LPF(s) \end{bmatrix} \text{ and } LPF(s) = \frac{\omega_f}{s+\omega_f}.$$

The corresponding block diagram [3] is shown below.



Appendix B.3 Derivation of Zero Sequence Components

The cluster balancing based on zero sequence voltage injection is given by Equation (B.12).

$$2P_{Cm} - (P_m^{+-} + P_m^{-+}) = P_{Cm}^{o+} + P_{Cm}^{o-} \tag{B.12}$$

For **SSBC**, substitute Phase *A* and Phase *B* into (D.1) as a set of equation to solve v_o and φ_o.

Phase A:

$$\begin{aligned}
&2P_{Ca} - \left(-V_{s_1}^{+} I_{s_1}^{-} \cos(\varphi_{Vp} + \varphi_{In}) - V_{s_1}^{-} I_{s_1}^{+} \cos(\varphi_{Vn} + \varphi_{Ip})\right) \\
&= V_o I_{s_1}^{+} \cos(\varphi_o - \varphi_{Ip}) - V_o I_{s_1}^{-} \cos(\varphi_o + \varphi_{In}) \\
&= V_o \cos\varphi_o \left(I_{s_1}^{+} \cos\varphi_{Ip} - I_{s_1}^{-} \cos\varphi_{In}\right) + V_o \sin\varphi_o \left(I_{s_1}^{+} \sin\varphi_{Ip} + I_{s_1}^{-} \sin\varphi_{In}\right)
\end{aligned} \tag{B.13}$$

which sets to be equivalent to $2P_{Ca} - X_{a3} = V_o \cos\varphi_o * X_{a1} + V_o \sin\varphi_o * X_{a2}$, where

$X_{a1} = \left(I_{s\_1}^{+} \cos\varphi_{Ip} - I_{s\_1}^{-} \cos\varphi_{In}\right)$;

$X_{a2} = \left(I_{s\_1}^{+} \sin\varphi_{Ip} + I_{s\_1}^{-} \sin\varphi_{In}\right)$;

$X_{a3} = \left(-V_{s_1}^{+} I_{s_1}^{-} \cos(\varphi_{Vp} + \varphi_{In}) - V_{s_1}^{-} I_{s_1}^{+} \cos(\varphi_{Vn} + \varphi_{Ip})\right)$.

Phase B:

$$\begin{aligned}
&2P_{Cb} - \left(-V_{s_1}^{+} I_{s_1}^{-} \cos\left(\varphi_{Vp} + \varphi_{In} + \tfrac{2}{3}\pi\right) - V_{s_1}^{-} I_{s_1}^{+} \cos\left(\varphi_{Vn} + \varphi_{Ip} + \tfrac{2}{3}\pi\right)\right) \\
&= V_o I_{s_1}^{+} \cos\left(\varphi_o - \varphi_{Ip} + \tfrac{2}{3}\pi\right) - V_o I_{s_1}^{-} \cos\left(\varphi_o + \varphi_{In} - \tfrac{2}{3}\pi\right) \\
&= V_o \cos\varphi_o \left[I_{s_1}^{+} \cos(\varphi_{Ip} - \tfrac{2}{3}\pi) - I_{s_1}^{-} \cos\left(\varphi_{In} - \tfrac{2}{3}\pi\right)\right] + V_o \sin\varphi_o \left[I_{s_1}^{+} \sin\left(\varphi_{Ip} - \tfrac{2}{3}\pi\right) + \right. \\
&\left. I_{s_1}^{-} \sin(\varphi_{In} - \tfrac{2}{3}\pi)\right]
\end{aligned} \tag{B.14}$$

which sets to be equivalent to $2P_{Cb} - X_{b3} = V_o \cos\varphi_o * X_{b1} + V_o \sin\varphi_o * X_{b2}$, where

$X_{b1} = \left(I_{s_1}^{+} \cos(\varphi_{Ip} - \tfrac{2}{3}\pi) - I_{s_1}^{-} \cos\left(\varphi_{In} - \tfrac{2}{3}\pi\right)\right)$;

$X_{b2} = \left(I_{s_1}^{+} \sin\left(\varphi_{Ip} - \tfrac{2}{3}\pi\right) + I_{s_1}^{-} \sin(\varphi_{In} - \tfrac{2}{3}\pi)\right)$;

$X_{b3} = \left(-V_{s\_1}^{+} I_{s\_1}^{-} \cos\left(\varphi_{Vp} + \varphi_{In} + \tfrac{2}{3}\pi\right) - V_{s\_1}^{-} I_{s\_1}^{+} \cos\left(\varphi_{Vn} + \varphi_{Ip} + \tfrac{2}{3}\pi\right)\right)$.

For **SDBC**, substitute *AB* and *BC* into (B.12) as a set of equation to solve i_o and φ_o.

AB:

$$
\begin{aligned}
&2P_{Cab} - \left(-V_{s\_1}^{+} I_{s\_1}^{-} \cos\left(\varphi_{Vp} + \varphi_{In} + \frac{\pi}{3}\right) - V_{s\_1}^{-} I_{s\_1}^{+} \cos\left(\varphi_{Vn} + \varphi_{Ip} + \frac{\pi}{3}\right)\right) \\
&= V_{s\_1}^{+} I_o \cos\left(\varphi_{Vp} - \varphi_o + \frac{\pi}{6}\right) - V_{s_1}^{-} I_o \cos\left(\varphi_{Vn} + \varphi_o + \frac{\pi}{6}\right) \\
&= I_o \cos\varphi_o \left(V_{s\_1}^{+} \cos(\varphi_{Vp} + \frac{\pi}{6}) - V_{s\_1}^{-} \cos(\varphi_{Vn} + \frac{\pi}{6})\right) + I_o \sin\varphi_o \, (V_{s\_1}^{+} \sin(\varphi_{Vp} + \frac{\pi}{6}) \\
&\qquad + V_{s\_1}^{-} \sin(\varphi_{Vn} + \frac{\pi}{6}))
\end{aligned}
\tag{B.15}
$$

which sets to be equivalent to $2P_{Cab} - X_{a3} = I_o \cos\varphi_o * X_{a1} + I_o \sin\varphi_o * X_{a2}$, where

$X_{a1} = \left(V_{s\_1}^{+} \cos(\varphi_{Vp} + \frac{\pi}{6}) - V_{s\_1}^{-} \cos(\varphi_{Vn} + \frac{\pi}{6})\right)$;

$X_{a2} = (V_{s\_1}^{+} \sin(\varphi_{Vp} + \frac{\pi}{6}) + V_{s\_1}^{-} \sin(\varphi_{Vn} + \frac{\pi}{6}))$;

$X_{a3} = \left(-V_{s\_1}^{+} I_{s\_1}^{-} \cos\left(\varphi_{Vp} + \varphi_{In} + \frac{\pi}{3}\right) - V_{s\_1}^{-} I_{s\_1}^{+} \cos\left(\varphi_{Vn} + \varphi_{Ip} + \frac{\pi}{3}\right)\right)$.

BC:

$$
\begin{aligned}
&2P_{Cbc} - \left(-V_{s\_1}^{+} I_{s\_1}^{-} \cos(\varphi_{Vp} + \varphi_{In} + \pi) - V_{s\_1}^{-} I_{s\_1}^{+} \cos(\varphi_{Vn} + \varphi_{Ip} + \pi)\right) \\
&= V_{s\_1}^{+} I_o \cos\left(\varphi_{Vp} - \varphi_o + \frac{\pi}{6} + \frac{2\pi}{3}\right) - V_{s\_1}^{-} I_o \cos\left(\varphi_{Vn} + \varphi_o + \frac{\pi}{6} - \frac{2\pi}{3}\right) \\
&= I_o \cos\varphi_o \left(V_{s\_1}^{+} \cos(\varphi_{Vp} - \frac{\pi}{2}) - V_{s\_1}^{-} \cos(\varphi_{Vn} - \frac{\pi}{2})\right) + I_o \sin\varphi_o \, (V_{s\_1}^{+} \sin(\varphi_{Vp} - \frac{\pi}{2}) \\
&\qquad + V_{s\_1}^{-} \sin(\varphi_{Vn} - \frac{\pi}{2}))
\end{aligned}
\tag{B.16}
$$

which sets to be equivalent to $2P_{Cbc} - X_{b3} = I_o \cos\varphi_o * X_{b1} + I_o \sin\varphi_o * X_{b2}$, where

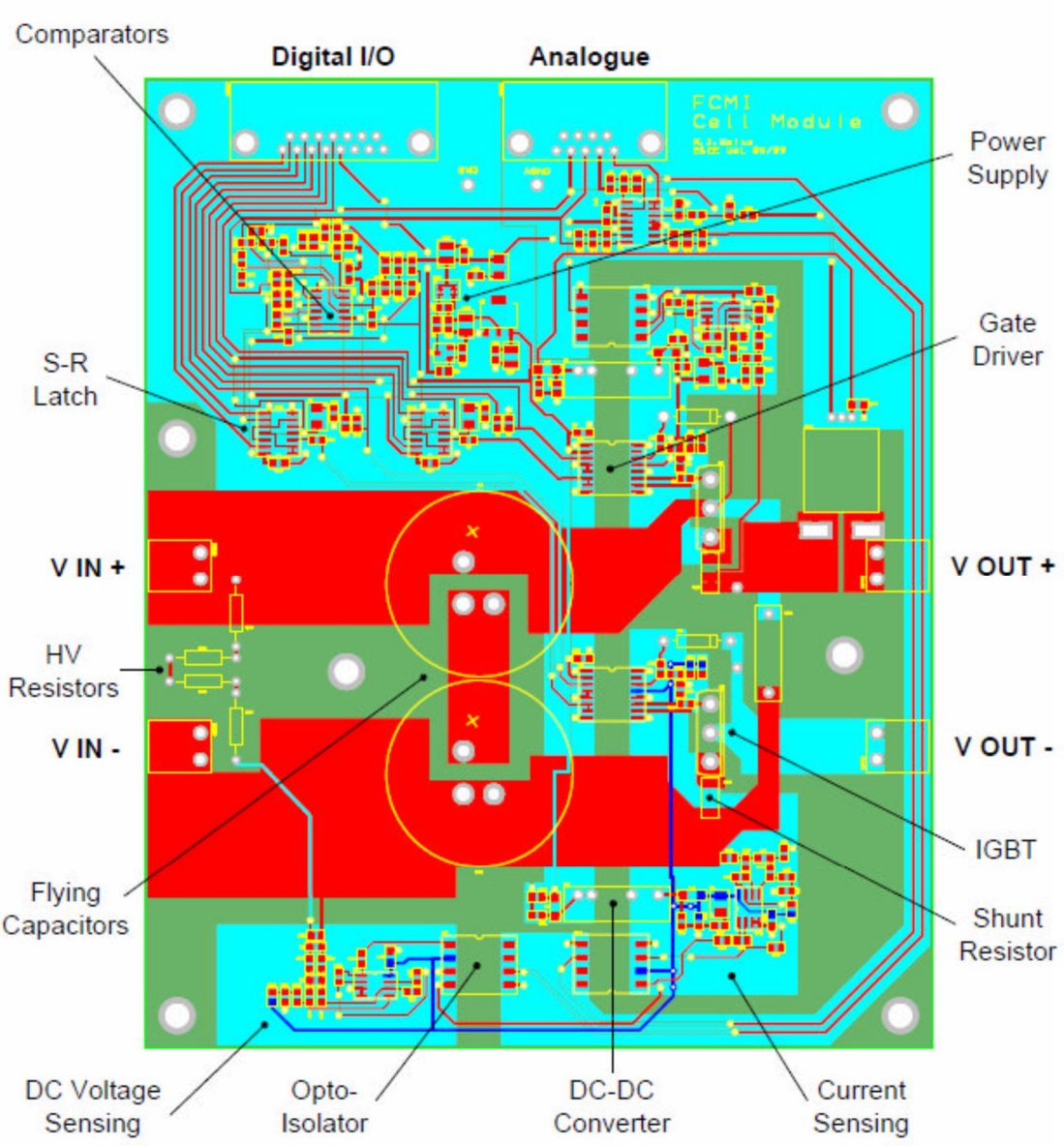
$X_{b1} = \left(V_{s\_1}^{+} \cos(\varphi_{Vp} - \frac{\pi}{2}) - V_{s\_1}^{-} \cos(\varphi_{Vn} - \frac{\pi}{2})\right)$;

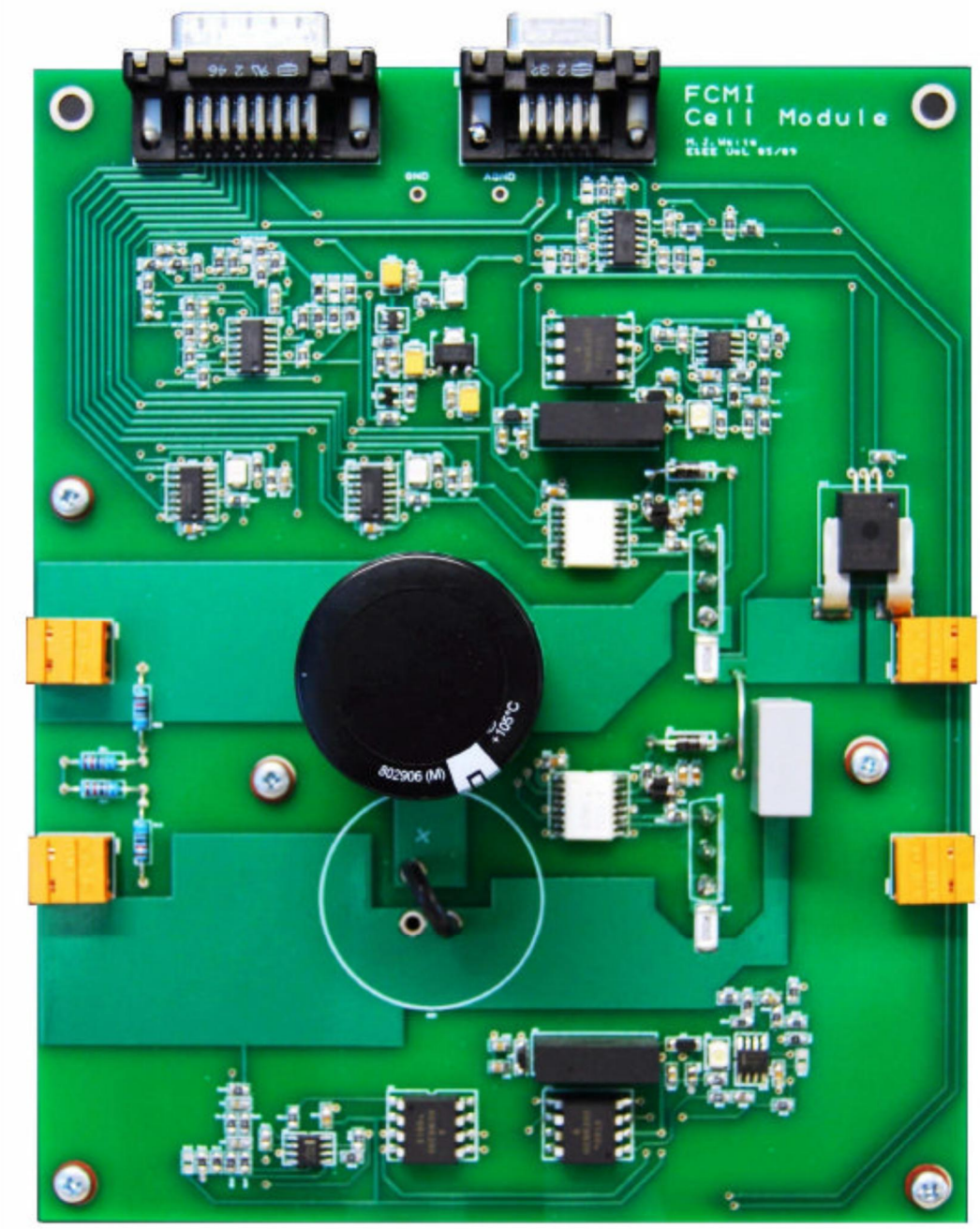
$X_{b2} = (V_{s\_1}^{+} \sin(\varphi_{Vp} - \frac{\pi}{2}) + V_{s\_1}^{-} \sin(\varphi_{Vn} - \frac{\pi}{2}))$;

$X_{b3} = \left(-V_{s\_1}^{+} I_{s\_1}^{-} \cos(\varphi_{Vp} + \varphi_{In} + \pi) - V_{s\_1}^{-} I_{s\_1}^{+} \cos(\varphi_{Vn} + \varphi_{Ip} + \pi)\right)$.

Hence, the equation set is $\begin{cases} 2P_{C1} - X_{a3} = M_o \cos\varphi_o * X_{a1} + M_o \sin\varphi_o * X_{a2} \\ 2P_{C2} - X_{b3} = M_o \cos\varphi_o * X_{b1} + M_o \sin\varphi_o * X_{b2} \end{cases}$, where M_o could be either zero sequence voltage V_o or current I_o.The magnitude and angle are solved and shown in Section 4.5.2.

Appendix C.1 Cell Card PCB Board Circuit and Photograph




FCMI
Cell Module
802906 (M)

Appendix C.2 Cell Card Capacitor and IGBT Characteristics

	Parameter	Value
Capacitor	Capacitance	560 μF± 20%
	Maximum working voltage	400 V_{DC}
	Maximum surge voltage	450 V_{DC}
	Maximum RMS ripple current (120 Hz)	5.52 A
	Maximum RMS ripple current (10 kHz)	7.70 A
	Lifetime	3000 h
IGBT Switch	Maximum collector-emitter voltage V_{CE}	600 V
	Maximum DC collector current I_c	30 A
	Short-circuit collector $I_{c(sc)}$	275 A
	Short-circuit withstand time t_{sc}	5 μs
	Collector-emitter saturation voltage $V_{CE(sat)}$	1.5 – 1.9 V
	Gate-emitter threshold voltage $V_{GE(Th)}$	4.1 – 5.7 V
	Total turn-on time t_{on}	44 – 50 ns
	Total turn-off time t_{off}	300 – 382 ns

Appendix D.1 UK Power Networks Line Impedance Parameters under Different Voltage Levels

Table. Line impedance parameters in different voltage level [133-136]

	Reactance (Ω/km)	Resistance (Ω/km)
11 kV	0.053-0.056	0.130-0.411
33 kV	0.303-0.310	0.100-0.300
132 kV	0.404-0.410	0.068-0.155
275 kV	0.323-0.335	0.034-0.077
400 kV	0.27-0.323	0.017-0.034