The University Of Sheffield.

Novel Approaches to Power Efficient GaN and Negative Capacitance Devices

A thesis submitted for the degree of

Doctor of Philosophy

By:

Ashwani Kumar

December 2018

Department of Electronic and Electrical Engineering

The University of Sheffield

Acknowledgement

I would like to express my sincerest gratitude and appreciation to my supervisor, Prof. Maria Merlyne De Souza for everything, starting from offering me the opportunity to join her team, to her valuable guidance, support, and encouragement during the course of my doctoral research.

I would like to acknowledge ENIAC-JU project E2SG for funding the first year of my research. A special thanks to Ms. Sara Gawthorpe, Ms. Hilary Levesley, Ms. Frances G. Bright, Ms. Dianne Webster, Dr. Kevin Jackson, Dr. Nathan Porter, Mr. Fahmi Mohammad, and Ms. Kim Brechin who have helped me regarding the departmental formalities.

I want to thank the past and present members of our team: Premlal Pillai, Mirza Rasheduzzaman, Asiel N. Corpus-Mendoza, Nagaditya Poluri, and Xiaoyao Song for their support and a good company.

I wish to thank my property owners, Dr. Piya Gamage and Susila Gamage, and their friend Dr. Rohan Tittagala, who helped me with moving in and getting settled in Sheffield, and are one of the humblest and kindest persons I have met.

Finally, I am grateful to my mother Ms. Omwati and my late father Mr. Prathvi Singh, for their hardships and being a constant source of inspiration for me. My final thanks goes to my siblings for their inestimable support and continual encouragement over the years.

Ashwani Kumar

List of Publications

Journals:

1. **A. Kumar**, P. B. Pillai, X. Song, and M. M. De Souza, “Negative Capacitance beyond ferroelectric switches,” *ACS Applied Materials and Interfaces*, vol. 10, no. 23, pp. 19812–19819, May 2018.
2. P. B. Pillai, **A. Kumar**, X. Song, and M. M. De Souza, “Diffusion-Controlled Faradaic Charge Storage in High-Performance Solid Electrolyte-Gated Zinc Oxide Thin-Film Transistors,” *ACS Appl. Mater. Interfaces*, vol. 10, no. 11, pp. 9782–9791, Mar. 2018. DOI: 10.1021/ACSAMI.7B14768.
3. **A. Kumar** and M. M. De Souza, “Impact of channel thickness on the performance of an E-mode p-channel MOSHFET in GaN,” *Appl. Phys. Lett.*, vol. 112, no. 15, pp. 153503-1–153503-4, Apr. 2018.
4. H. Amano *et al.*, “The 2018 GaN power electronics roadmap,” *J. Phys. D. Appl. Phys.*, vol. 51, no. 16, pp. 163001-34–163001-35, Apr. 2018.
5. **A. Kumar** and M. M. De Souza, “Modelling the threshold voltage of p-channel enhancement-mode GaN heterostructure field-effect transistors,” *IET Power Electron.*, vol. 11, no. 4, pp. 675–680, Apr. 2018.
6. **A. Kumar** and M. M. De Souza, “An E-Mode p-Channel GaN MOSHFET for a CMOS Compatible PMIC,” *IEEE Electron Device Lett.*, vol. 38, no. 10, pp. 1449–1452, Oct. 2017.

Conferences:

1. J. Zhou, **A. Kumar**, and M. M. De Souza, “Influence of an underlying 2DEG on the performance of a p-channel MOSHFET in GaN,” *International Workshop on Nitride Semiconductors* (IWN 2018), Kanazawa, Japan. Nov 2018.

2. **A. Kumar** and M. M. De Souza, “On the Dynamic characteristics of Ferroelectric and Paraelectric FETs,” *Proc of the 2nd Electron Devices Technology and Manufacturing* (EDTM 2018), Kobe, Japan. Mar 2018 (Oral Presentation).
3. **A. Kumar** and M. M. De Souza, “Enhancement mode p-channel devices for GaN CMOS,” *International Conference on Optimisation of Electrical & Electronic Equipment Aegean Conference on Electrical Machines* (OPTIM-ACEMP 2017), Brasov, Romania, May 2017.
4. **A. Kumar** and M. M. De Souza, “Mechanism of Turn-Off Operation in E-mode p-channel MOSHFET in GaN,” *UK Semiconductors* (UKS 2017), Sheffield, United Kingdom, July 2017 (Oral Presentations, Session G-O-8, 12 Jul 2017).
5. **A. Kumar** and M. M. De Souza, “Extending the bounds of performance in E-mode p-channel GaN MOSHFETs,” *Proc of the 62nd International Electron Devices Meeting* (IEDM 2016), Dec. 2016, pp. 7.4.1-7.4.4.
6. **A. Kumar**, P. B. Pillai, and M. M. De Souza, “Comparative Characteristics of High Performance ZnO Thin Film Transistors,” *6th International Symposium on Transparent Conductive Material* (TCM 2016), Platanias-Crete, Greece, Oct 2016 (Oral Presentation, Session 14B, 13 Oct 2016).
7. **A. Kumar** and M. M. De Souza, “Theoretical Modelling of 2DEG and 2DHG in III-Nitride based heterostructures” *Proc of the 13th International Seminar on Power Semiconductors* (ISPS 2016), Prague, Czech Republic, Sep 2016 (Poster Presentation, 1 Sep 2016).
8. **A. Kumar** and M. M. De Souza, “Theoretical modelling of 2DHG in Oxide/GaN/AlGaN/GaN heterostructures,” *UK Semiconductors* (UKS 2016), Sheffield, United Kingdom, July 2016 (Poster Presentations, Session G-P-14, 6 Jul 2016).

Abstract

Recent emergence of data-driven and computation hungry algorithms has fuelled the demand for energy and processing power at an unprecedented rate. Semiconductor industry is, therefore, under constant pressure towards developing energy efficient devices. A Shift towards materials with higher figure-of-merit compared to Si, such as GaN for power conversion is one of the options currently being pursued. A minimisation in parasitic and static power losses in GaN can be brought about by realising on-chip CMOS based gate drivers for GaN power devices. At present, p-channel MOSHFETs in GaN show poor performance due to the low mobility and the severe trade-off between $|I_{ON}|$ and $|V_{th}|$.

For the first time, it is shown that despite a poor hole mobility, it is possible to improve the on-current as well as minimise $|I_{ON}|$ - $|V_{th}|$ trade-off, by adopting a combination of techniques: using an AlGaN cap, biased two-dimensional electron gas, and shrinking source-gate and gate-drain access region and channel lengths. As part of this work, a novel vertical p-channel heterojunction tunnel FET (TFET) utilising polarisation induced tunnel junction (PITJ) is also explored, which unlike common TFETs, shows non-ambipolar transfer characteristics and a better electrostatic control over the tunneling region via the gate.

Meeting the ever-increasing demand for computation would require continuous scaling of transistor physical dimensions and supply voltage. While a further reduction in physical dimension is expected to come from adopting a vertical integration scheme, scaling in supply voltage would require achieving sub-60 mV/dec of subthreshold swing. The two common approaches to achieve this are TFETs and negative capacitance

(NC) FETs, where the NC operation is commonly associated with ferroelectric materials.

This work develops a model to explain sub-60 mV/dec, observed in Ta_2O_5/ZnO thin-film-transistors, which is governed by the motion of oxygen ions inside Ta_2O_5, leading to NC under dynamic gate bias sweep.

Table of Contents

Chapter 1 Introduction 1

1.1. Overview 1

1.2. Making Power Conversion Energy Efficient 1

1.3. Satisfying Growing Demand for Computation 5

1.3.1. Achieving subthreshold swing below $\mathbf{60}\ \boldsymbol{mV/dec}$ 6

1.3.2. Beyond Von Neumann Architecture 8

1.4. Objective of This Work 11

1.5. Outline of the Thesis 11

1.6. References 13

Chapter 2 MOSFET and Steep-Switching Devices 16

2.1. Operation of A Metal-Oxide-Semiconductor (MOS) FET 16

2.1.1. Body Factor of a MOS 17

2.1.2. Boltzmann Limit and Subthreshold Operation of a MOSFET 19

2.2. Sub-60 mV/dec Switching, Body Factor, and Negative Capacitance 21

2.3. Operation of a TFET 23

2.4. Physics of Ferroelectric Materials 25

2.4.1. Equivalent Series R-C Circuit Model 29

2.5. Operation of a FE-FET 30

2.6. Operation of a PE-FET 33

2.7. Summary 34

2.8. Reference 35

Chapter 3 Fundamentals of GaN and Heterostructure Devices 38

3.1. Why GaN? 38

3.2. Polarisation and Polarisation Sheet Charge 39

3.3. Polarisation Effects in AlN/GaN and Their Alloys 40

3.4. Polarisation Induced Two Dimensional Carrier Gases 44

3.5. Operation of MOS in GaN Heterostructures 47

3.5.1. Threshold Voltage Expression and C-V Characteristics 48

3.6. Achieving Normally-Off Operation in n-channel MOSHFET 50

3.7. Summary 52

3.8. Reference 52

Chapter 4 Modelling the Threshold Voltage for p-channel E-mode GaN HFETs.57

4.1. Simulation Model and Heterostructures 59

4.2. Derivation of Threshold Voltage Expression 65

4.2.1. Conventional Heterostructure 65

4.2.2. Alternate Heterostructure with an AlGaN Cap 67

4.3. Analysis of the Conventional Heterostructure p-Channel MOSHFET 69

4.4. Analysis of the Alternate Heterostructure p-Channel MOSHFET 74

4.5. Summary 82

4.6. References 83

Chapter 5 An E-Mode P-Channel GaN MOSHFET for a CMOS Compatible PMIC 88

5.1. Introduction 88

5.2. Methodology and Settings 91

5.3. Impact of Gate Length on Performance 91

5.4. Impact of Channel Thickness on the Performance of an E-Mode p-Channel MOSHFET in GaN 98

5.5. Summary 103

5.6. References 104

Chapter 6 A Non-ambipolar p-channel GaN Heterostructure Tunnel FET with high on/off ratio 108

6.1. Introduction 108

6.2. Modelling Tunneling Transport 110

6.3. Non-ambipolar Operation of P-Channel GaN HTFET 112

6.4. Optimised Cylindrical P-Channel GaN HTFET 114

6.5. Analysis of Tunnel Distance 118

6.6. Summary 120

6.7. References 121

Chapter 7 Negative Capacitance beyond Ferroelectric Switches 125

7.1. Introduction 125

7.2. Results 129

7.3. Summary 144

7.4. References 146

Chapter 8 Conclusions and Future Work 151

8.1. Concluding Remarks 151

8.2. Future Work 152

Appendix 155

Chapter 1 Introduction

1.1. OVERVIEW

The international demand for energy is on a constant rise. This is in part due to the staggering growth of economy in developing nations such as India, China, and in Africa that is resulting in expansion of industrial, transportation, commercial sectors and human consumption. A recent explosion in data-driven and compute-hungry techniques, such as deep learning and cryptocurrency mining constitutes another major part of higher demand for energy. The aggregate energy consumption in mining bitcoins, a form of cryptocurrency, is currently at a whopping 73 TWh, surpassing the energy consumption of entire countries such as Czech Republic or Austria [1]. Owing to an increasing demand for data-driven services, energy consumption of data centres in U.S. alone is estimated to be 73 PWh by 2020 according to Lawrence Berkeley National Laboratory [2], thereby underscoring the urgent need for efficient energy systems.

1.2. MAKING POWER CONVERSION ENERGY EFFICIENT

Owing to a well-established manufacturing base, various forms of power converters, AC/AC, AC/DC, DC/AC, or DC/DC, have traditionally relied upon silicon as the basic semiconductor for power devices. However, it is apparent that more efficient semiconductors are required for sustainable development of society. Table 1.1 highlights the electronics and thermal properties along with different figure-of-merits (FOMs) of some of the promising semiconductor materials for power applications.

Table 1.1. Electronic properties of different materials, data obtained from [3]–[6], hole mobility values for GaN in bulk and 2DHG are from [7], [8], and FOM parameters are from [9], [10], respectively.

Parameters	Description	Si	4H-SiC	GaN	Diamond
ε_r	Dielectric coefficient	11.7	9	10	5.5
$E_G\ (eV)$	Band gap	1.1	3.26	3.39	5.45
$n_i\ (cm^{-3})$	Intrinsic carrier density	1.5×10^{10}	8.2×10^{-9}	1.9×10^{-10}	1.6×10^{-27}
$v_{sat}\ (10^7\ cm/s)$	Electron saturation velocity	1	2	2.5	2.7
μ_n ($\mathrm{cm^2/Vs}$)	Electron mobility	1350	900	1200 (Bulk) 2000 (2DEG)	2200
μ_p ($\mathrm{cm^2/Vs}$)	Hole mobility	450	50	81 (Bulk) 43 (2DHG)	1600
$\mathcal{E}_{br}(MV/cm)$	Breakdown electric field	0.3	2.0	3.3	5.6
$\lambda(W/cmK)$	Thermal conductivity	1.5	4.5	1.3	20
BFOM ($\varepsilon_r \mu_n \mathcal{E}_{br}^3$)	Baliga's FOM	1	500	2414	8964
HMFOM ($\sqrt{\mu_n}\mathcal{E}_{br}$)	Huang's materials FOM	1	8	15	28

Both the FOMs in the above table have been normalised with respect to Si. Here BFOM is equivalent to the inverse of the conduction loss with specific area, therefore is relevant to those cases where the switching loss is dominated by conduction loss. Whereas HMFOM, which is the inverse of total loss, also includes the switching losses during charging and discharging of the input capacitance of the power transistor.

Among the materials listed in Table 1.1, GaN is particularly unique, because of its polarisation properties that lead to formation of two-dimensional electron and hole gases (2DEG and 2DHG) with high sheet density $\sim 10^{13}\ cm^{-3}$ without applying any external bias. In addition, despite having a bulk electron mobility smaller than Si, the 2DEG in GaN exhibits an electron mobility of $2000\ cm^2/Vs$, ~ 50 % higher compared to Si. As observed by M. Shur *et al.* [11] in their theoretical analysis, a better suppression of the piezoelectric scattering, resulting from a high concentration of electron gas and a reduction of ionized impurity scattering in the absence of doping are responsible for the high mobility of the 2DEG. Mobility is therefore primarily limited by polar optical

phonon scattering. On the other hand, such a theoretical study of hole mobility of 2DHG in GaN is still non-existent. The values listed in Table 1.1 for the hole mobility in bulk and 2DHG are the best experimental values observed to date. As a result of this highly conducting 2DEG along with higher breakdown electric field and saturation velocity means that GaN devices can operate at higher voltages and frequency at a fraction of the size of silicon power devices.

In high frequency power conversion, increasing the frequency reduces the size and volume of various other circuit elements in the system, such as transformers, filters and inductors. This helps to reduce the weight, bill of materials and thereby the cost of power systems. Increasing the frequency of operation in power MOSFETs, however leads to a rise in switching loss, as

$$Loss \propto \frac{\sqrt{f}}{FOM} \tag{1.1}$$

Since FOM remains fixed for a given material, Eq. (1.1) indicates a material with higher FOM becomes necessary to suppress the increase in loss as the frequency of operation becomes higher.

Fig. 1.1 elucidates device losses in Si and GaN with respect to frequency. Owing to the much higher BFOM in GaN compared to Si, GaN based devices facilitate smaller conduction losses. Moreover, the rise in device loss with frequency occurs at a smaller rate in GaN than Si, owing to a higher HMFOM. This makes GaN devices inherently advantageous in efficiency despite the higher frequency in comparison to silicon as indicated in this figure.

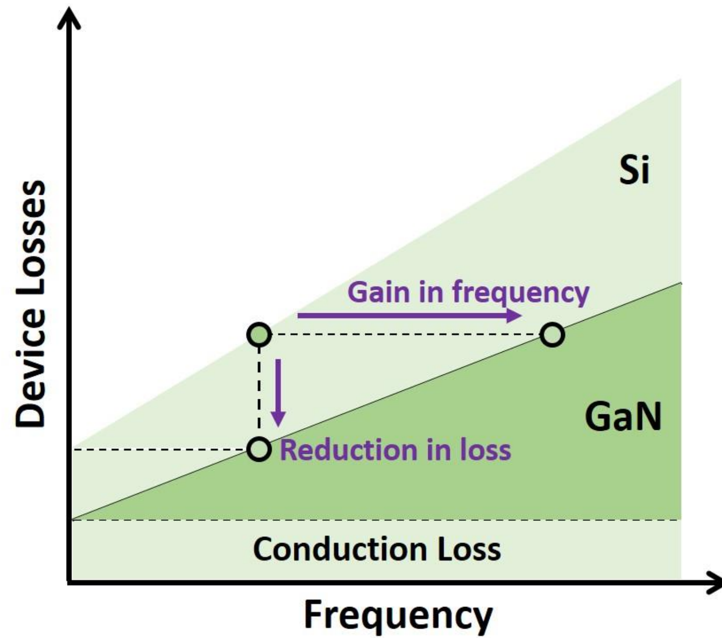

Fig. 1.1. Comparison of device losses, conduction and switching losses, for GaN and Si.

Table 1.1 also shows that the material properties and FOM of diamond far exceed the properties of Si or GaN. However, owing to economic reasons and difficulty in achieving n-type doping in diamond, the commercialisation of diamond based power devices is not expected any time soon.

One downside of GaN power devices is that currently the gates of these devices are driven by Si based CMOS, located discretely, though more recently GaN ICs based on n-type logic gate drivers have also come into the market [12]. This lack of integrated CMOS gate driver introduces chip-to-chip delay and parasitic inductance to the gate drive loop, resulting in slow operation with higher loss and instability. A further improvement is required by integrating power device and CMOS based gate driver on the common GaN chip to harness the full material benefits of GaN.

However, the mobility of holes in GaN remains poor, $7.8 - 81\ cm^2/Vs$ in bulk [7] and $10 - 43\ cm^2/Vs$ for 2DHG [8] at room temperature, which severely degrades the performance of monolithic CMOS in GaN [13], thereby prohibiting applications of GaN based logic and CMOS for driving power converters. Novel solutions are therefore

required to improve hole mobility or realise a p-channel device with a higher hole mobility material heterogeneously integrated with GaN.

1.3. Satisfying Growing Demand for Computation

Besides electrical power conversion in all its forms, a large fraction of energy consumption accrues from the demand for computation. This has historically been made possible by Moore's law, which states that the number of transistors on an integrated chip doubles approximately every 2 years [14]. Moore's law has served both as a motivation and guide for semiconductor industry in setting targets for the next generation of transistors. As a result, the size of the transistors became smaller, which led to an increase in their performance, whilst reducing the cost of manufacture.

The targets for feature size along with other physical and electrical characteristics for each of the technology nodes are dictated by the International Technology Roadmap for Semiconductors (ITRS), which has successfully predicted the evolution of transistor properties over the few decades. Figs. 1.2 (a) and (b) show the forecast for physical gate length L_G, subthreshold swing (SS), the on-current I_{ON}, and maximum power consumption (supply voltage $V_{DD} \times I_{ON}$), for each technology node up to 2030, according to ITRS Executive Reports, 2015 [15]. By the year 2021, L_G is expected to shrink to $10\ nm$, at which point, a further scaling in L_G will not be possible until the next decade due to adverse short-channel effects and higher channel leakage current. A further scaling of physical dimension is expected to come from adopting a vertical gate all around device structure.

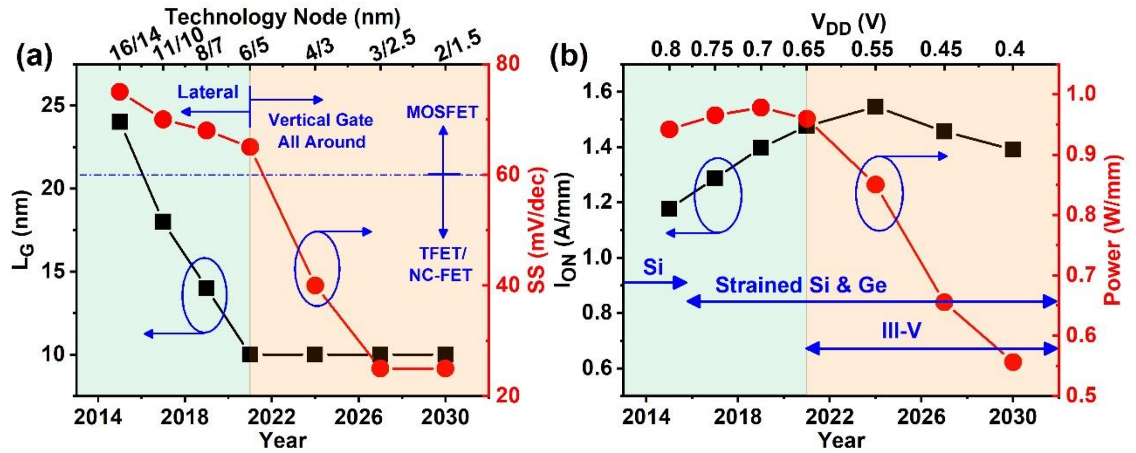

Fig. 1.2. Targets for the (a) gate length, sub-threshold slope, (b) on-current and power over the next decade, as predicted by ITRS 2.0, Executive Summary 2015 [15].

Despite a higher on-current, a reduction in power is expected due to scaling of supply voltage and a reduction in subthreshold swing. After year 2021, two important technological shifts become necessary for ensuring high performance even at lower V_{DD}:

1. Employing tunneling or negative capacitance phenomena to bring SS below $60\ mV/dec$
2. Realising beyond von Neumann architectures at hardware level

1.3.1. Achieving subthreshold swing below 60 mV/dec

In a conventional MOSFET, due to Boltzmann distribution of carriers, a change in the carrier density in a semiconductor channel is limited to $\sim \exp(q\Psi_s/kT)$ with respect to the surface potential Ψ_s, which results in a drain current unable to change by more than an order of magnitude for a change in surface potential by 60 mV. This implies that for a given I_{ON} and at a fixed SS, a reduction in the supply voltage comes at a cost of a higher off-current I_{OFF}, leading to an off-state power consumption, as shown in Fig. 1.3. Therefore, reducing SS beyond this limit of $60\ mV/dec$ in conventional MOSFET becomes crucial for the continued scaling of supply voltage and power consumption. Tunnel FETs (TFETs), where the transport of carriers between source and drain is enabled by quantum mechanical band-to-band tunneling over a potential barrier, have

been demonstrated to overcome this limit. Nevertheless, the performance of these transistors has been historically poorer than their CMOS counterparts [16], which is due to tunneling that introduces additional series resistance in the source and drain path. To date, the best reported electrical characteristics have been achieved in a vertical nanowire InAs/GaAsSb/GaSb TFET, showing an on-current of $0.31\ mA/mm$ at $60\ mV/dec$ of SS [17]. In addition to poor on-current, TFETs also suffer from ambipolarity, which refers to their inability to remain in off-state for one of the polarities of the applied gate bias, further restricting their applicability in complementary logic [18].

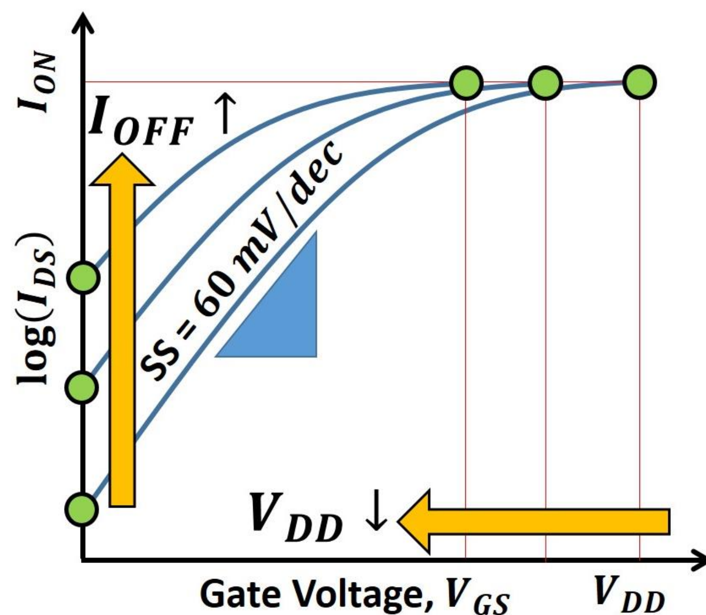

Fig. 1.3. Schematic of transfer characteristics for a MOSFET showing that scaling of the supply voltage causes the off-current to become higher.

Ferroelectric FETs (FE-FETs) and other negative-capacitance FETs provide an alternative approach to lower SS below $60\ mV/dec$. In these FETs, the gate dielectric in the transistor is replaced by a material with inherent instability, i.e. exhibiting a two-valley energy profile rather than a parabolic energy profile, observed in ordinary dielectric. Owing to this instability, the resulting insulator capacitance becomes negative for a range of applied gate bias. This produces an amplification in the potential at the

surface of the semiconductor relative to the applied gate bias, leading to steeper drain-current characteristics.

1.3.2. Beyond Von Neumann Architecture

The von Neumann framework, where the memory and processing units are physically separated from each other, has been the underlying architecture behind contemporary high level programming languages, where variables in the program represent memory locations, algebraic and logical operations describe a single or a set of instructions to be performed by the processing unit, control statements mimic jump instructions, and assignment statements are a representation of fetch and store operations. Despite its prevalent use, this architecture has many limitations, such as information is processed sequentially, the speed at which any logic or algebraic operation can be performed remains limited to the maximum speed at which the data can be transferred between memory and processing units, which also leads to a significant loss of power in data transfer, where a small operation needs to be performed over a large amount of data. The time delay caused by data transfer between the memory and processor introduces a bottleneck on the maximum speed in this architecture referred to as memory wall [19].

Many avenues have been proposed and developed to surpass the limitations of von Neumann computing. Fig. 1.4 shows a chart of approaches based upon how information is processed, as reported by IRTS in [20]. These can be broadly divided into "Program-Centric" and "Data-Centric", which can be further decomposed depending upon whether the outcome of a calculation is deterministic or non-deterministic. "Program-Centric" refers to the processors which take a program as an input, which contains a set of instructions provided by a designer and execute these instruction on the available input to generate an output. As shown, a Program-Centric framework can be sub-divided into von Neumann architecture, where instructions are executed from a stored program in a

sequential order, and non-von Neumann architectures, where instructions can be executed in parallel, for instance in field-programmable gate array (FPGA) or the same device is utilised to carry out both processing and storage, such as in a memristor [21], which exhibits a state dependent resistance.

Fig. 1.4. Different categories for computing architecture, as published by ITRS in [20].

On the other hand, a Data-Centric approach, also a non-von Neumann computing framework, uses available input data to learn and extract meaningful features that have proven to be useful in performing a variety of tasks, such as summarising news or reports, categorising documents, recognising objects in an image, performing semantic analysis, processing natural language or recognising speech, and generating responses. Brain inspired artificial neural networks (ANN) [22] have recently surpassed the limitation of other traditional approaches based on either von Neumann or non-von Neumann architectures. Deep neural networks with multiple stacked layers of neurons have

recently achieved significant improvements in the accuracy in these tasks, matching or even outperforming human-level accuracy in some of the complex world problems such as image and speech recognition [23], [24], autonomous driving [25], and medical diagnosis [26]. Further improvements in the accuracy, in deep networks require aggressively increasing the depth and size of these networks, demonstrating a need for ever-increasing computational capacity and large volume of memory required to store the analogue strength (weights) of a synapse connecting the neurons.

In the state-of-the-art deep networks, the number of weight parameters are usually of the order of millions [27], However, Si based CMOS implementation of ANNs with SRAM as the synaptic memory places a severe limitation on the maximum available on-chip memory. Moreover, this approach also consumes a large amount of power due to the continuous data transfer between memory and processing units during the operation.

In an alternative hardware platform, non-volatile memory (NVM) with analog or multi-state memory capabilities have been proposed for providing weight storage [28]. NVM typically consists of a memristor, realised using different approaches such as: phase change materials [29], formation/rupture of a conducting filament/bridge [30], magnetic tunnel junction [31], ferroelectric materials [32] or ferroelectric tunnel junction [33]. Compared to six-transistor (6T) cell in a typical SRAM, the one-transistor-one-resistor (1T1R) cell in NVM permits realisation of potentially higher density memory storage, removing the need for off-chip memory to store large number of weights. Currently, the research in this area has focused upon realising networks of synaptic devices, with connectivity and power consumption equivalent of a human brain, which consists of 10^{10} synapses yet only consumes $\sim 10\,W$ [34]. The following section introduces the fundamentals of such neural networks and discusses one of the widely used learning algorithms to train these networks.

1.4. Objective of This Work

The focus of this work is two-fold. First, assessing the limits of performance of a p-channel device in GaN that is highly desired for the realisation of a complementary switch in GaN that can provide an integrated gate drivers for GaN power devices. Here we explore GaN heterostructures based lateral FET and a vertical tunnel FET, employing a polarisation induced tunnel junction. The second major contribution focuses on new physics of negative capacitance, beyond ferroelectric FETs. This is demonstrated by developing novel theory that explains steep switching in solid-electrolyte Ta_2O_5/ZnO thin-film transistors (TFTs), as part of this work.

1.5. Outline of the Thesis

The thesis is organised as follows:

In this Chapter 1 the need for energy-efficient devices and a growing demand for processing speed is introduced. Currently available solutions to meet these demands beyond 2021 are discussed. Finally, the role of this work in addressing these challenges is presented.

In the introductory Chapters 2 and 3, the operation of MOSFET and various techniques to overcome the 60 mV/dec limit of SS, via band-to-band tunneling, negative capacitance, are presented to provide the reader a background on the theory of Tunnel FETs and negative capacitance FETs. In Chapter 3, the physics of GaN, operation of metal-oxide-semiconductor (MOS) in GaN heterostructures, and approaches to realise normally-off operation in n-channel GaN heterostructure devices are discussed.

In Chapters 4 and 5 the limitations of conventional p-channel enhancement mode (E-mode) GaN MOS heterostructure FET (MOSHFET) are discussed. A modified p-channel device with an AlGaN cap for overcoming and extending the performance of these

devices is proposed. It is revealed in Chapter 4 that the device with the AlGaN cap suffers from higher leakage current as the thickness of the channel increases. Utilisation of a biased 2DEG along with an AlGaN cap is demonstrated to resolve this issue.

Chapter 6 introduces a novel p-channel vertical TFET in GaN that relies upon polarisation properties of GaN for its tunneling operation. From TCAD simulations, it is shown that this device, unlike conventional TFETs, does not suffer from ambipolarity in the transfer characteristics. The presented device also shows promise for achieving a much smaller tunnel distance with a better control than is possible in conventional TFETs.

In Chapter 7, a novel physics based model that explains sub-60 mV/dec of switching in a Ta_2O_5/ZnO solid-electrolyte FET is developed. It is shown that the motion of mobile oxygen ions inside Ta_2O_5 ions under a dynamic gate bias sweep causes the capacitance across Ta_2O_5 to become negative, leading to sub-60 mV/dec of switching.

In Chapter 8, concluding remarks are presented and future directions for this work are discussed.

1.6. References

[1] "Bitcoin Energy Consumption Index - Digiconomist." [Online]. Available: https://digiconomist.net/bitcoin-energy-consumption. [Accessed: 01-Dec. 2018].

[2] A. Shehabi, S. J. Smith, N. Horner, I. Azevedo, R. Brown, J. Koomey, E. Masanet, D. Sartor, M. Herrlin, and W. Lintner, "United States Data Center Energy Usage Report," 2016.

[3] U. K. Mishra, Shen Likun, T. E. Kazior, and Yi-Feng Wu, "GaN-Based RF Power Devices and Amplifiers," *Proc. IEEE*, vol. 96, no. 2, pp. 287–305, Feb. 2008. DOI: 10.1109/JPROC.2007.911060.

[4] M. S. Shur, *Handbook Series on Semiconductor Parameters Volume 1*. 1996. DOI: 10.1142/2046-VOL1.

[5] C. Claeys and E. Simoen, *Germanium-Based Technologies*. 2007. DOI: 10.1016/B978-0-08-044953-1.X5000-5.

[6] A. Elasser and T. P. Chow, "Silicon carbide benefits and advantages for power electronics circuits and systems," *Proc. IEEE*, vol. 90, no. 6, pp. 969–986, Jun. 2002. DOI: 10.1109/JPROC.2002.1021562.

[7] M. Zhong, J. Roberts, W. Kong, A. S. Brown, and A. J. Steckl, "p-type GaN grown by phase shift epitaxy," *Appl. Phys. Lett.*, vol. 104, no. 1, p. 012108, Jan. 2014. DOI: 10.1063/1.4861058.

[8] B. Reuters, H. Hahn, A. Pooth, B. Holländer, U. Breuer, M. Heuken, H. Kalisch, and A. Vescan, "Fabrication of p-channel heterostructure field effect transistors with polarization-induced two-dimensional hole gases at metal–polar GaN/AlInGaN interfaces," *J. Phys. D. Appl. Phys.*, vol. 47, no. 17, p. 175103, Apr. 2014. DOI: 10.1088/0022-3727/47/17/175103.

[9] N. Kaminski, "State of the art and the future of wide band-gap devices," in *2009 13th European Conference on Power Electronics and Applications*, Sep. 2009.

[10] A. Q. Huang, "New Unipolar Switching Power Device Figures of Merit," *IEEE Electron Device Lett.*, vol. 25, no. 5, pp. 298–301, May 2004. DOI: 10.1109/LED.2004.826533.

[11] M. Shur, B. Gelmont, and M. Asif Khan, "Electron mobility in two-dimensional electron gas in AIGaN/GaN heterostructures and in bulk GaN," *J. Electron. Mater.*, vol. 25, no. 5, pp. 777–785, May 1996. DOI: 10.1007/BF02666636.

[12] D. Kinzer, "GaNFast^{TM} Power ICs Enable Breakthroughs in Adapter Performance," *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2018. [Online]. Available: https://www.navitassemi.com/wp-content/uploads/2015/03/APEC-2018-Ind-Session-Semiconductors-Dan-Kinzer-3-7-18.pdf. [Accessed: 10-Dec. 2018].

[13] R. Chu, Y. Cao, M. Chen, R. Li, and D. Zehnder, "An Experimental Demonstration of

GaN CMOS Technology," *IEEE Electron Device Lett.*, vol. 37, no. 3, pp. 269–271, Mar. 2016. DOI: 10.1109/LED.2016.2515103.

[14] G. E. Moore, "Cramming more components onto integrated circuits," *Electronics*, vol. 38, no. 8, pp. 114–117, 1965. DOI: 10.1109/JPROC.1998.658762.

[15] International Technology Roadmap for Semiconductors (ITRS), "Executive Reports 2015," *ITRS*. [Online]. Available: http://www.itrs2.net/itrs-reports.html. [Accessed: 10-Dec. 2018].

[16] H. Lu and A. Seabaugh, "Tunnel Field-Effect Transistors: State-of-the-Art," *IEEE J. Electron Devices Soc.*, vol. 2, no. 4, pp. 44–49, Jul. 2014. DOI: 10.1109/JEDS.2014.2326622.

[17] E. Memisevic, J. Svensson, M. Hellenbrand, E. Lind, and L.-E. Wernersson, "Vertical InAs/GaAsSb/GaSb tunneling field-effect transistor on Si with S = 48 mV/decade and Ion = 10 μA/μm for Ioff = 1 nA/μm at Vds = 0.3 V," in *2016 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2016, p. 19.1.1-19.1.4. DOI: 10.1109/IEDM.2016.7838450.

[18] D. B. Abdi and M. J. Kumar, "Controlling ambipolar current in tunneling FETs using overlapping gate-on-drain," *IEEE J. Electron Devices Soc.*, vol. 2, no. 6, pp. 187–190, 2014. DOI: 10.1109/JEDS.2014.2327626.

[19] W. A. Wulf and S. A. McKee, "Hitting the memory wall: implications of the obvious," *ACM SIGARCH Comput. Archit. News*, vol. 23, no. 1, pp. 20–24, Mar. 1995. DOI: 10.1145/216585.216588.

[20] International Technology Roadmap for Semiconductors (ITRS), "Beyond CMOS (Emerging Research Devices)," *ITRS*, 2015.

[21] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," *Nature*, vol. 453, no. 7191, pp. 80–83, May 2008. DOI: 10.1038/NATURE06932.

[22] K. L. Priddy and P. E. Keller, *Artificial Neural Networks: An Introduction*. SPIE press, 2005.

[23] O. Russakovsky, J. Deng, H. Su, J. Krause, S. Satheesh, S. Ma, Z. Huang, A. Karpathy, A. Khosla, M. Bernstein, A. C. Berg, and L. Fei-Fei, "ImageNet Large Scale Visual Recognition Challenge," *Int. J. Comput. Vis.*, vol. 115, no. 3, pp. 211–252, Dec. 2015. DOI: 10.1007/S11263-015-0816-Y.

[24] W. Xiong, J. Droppo, X. Huang, F. Seide, M. Seltzer, A. Stolcke, D. Yu, and G. Zweig, "The microsoft 2016 conversational speech recognition system," in *2017 IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP)*, Mar. 2017, pp. 5255–5259. DOI: 10.1109/ICASSP.2017.7953159.

[25] C. Chen, A. Seff, A. Kornhauser, and J. Xiao, "DeepDriving: Learning Affordance for Direct Perception in Autonomous Driving," in *2015 IEEE International Conference on*

Computer Vision (ICCV), Dec. 2015, pp. 2722–2730. DOI: 10.1109/ICCV.2015.312.

[26] A. Esteva, B. Kuprel, R. A. Novoa, J. Ko, S. M. Swetter, H. M. Blau, and S. Thrun, "Dermatologist-level classification of skin cancer with deep neural networks," *Nature*, vol. 542, no. 7639, pp. 115–118, Feb. 2017. DOI: 10.1038/NATURE21056.

[27] G. Huang, Z. Liu, L. van der Maaten, and K. Q. Weinberger, "Densely Connected Convolutional Networks," in *2017 IEEE Conference on Computer Vision and Pattern Recognition (CVPR)*, Jul. 2017, pp. 2261–2269. DOI: 10.1109/CVPR.2017.243.

[28] T. Chang, Y. Yang, and W. Lu, "Building neuromorphic circuits with memristive devices," *IEEE Circuits Syst. Mag.*, vol. 13, no. 2, pp. 56–73, 2013. DOI: 10.1109/MCAS.2013.2256260.

[29] J. Lin, A. Annadi, S. Sonde, C. Chen, L. Stan, K. V. L. V Achari, S. Ramanathan, and S. Guha, "Low-Voltage Artificial Neuron using Feedback Engineered Insulator-to-Metal-Transition Devices," pp. 2–5, 2016.

[30] S. Menzel, U. Bottger, M. Wimmer, and M. Salinga, "Physics of the Switching Kinetics in Resistive Memories," *Adv. Funct. Mater.*, vol. 25, no. 40, pp. 6306–6325, 2015. DOI: 10.1002/ADFM.201500825.

[31] A. Jaiswal, A. Agrawal, and K. Roy, "In-situ, In-Memory Stateful Vector Logic Operations based on Voltage Controlled Magnetic Anisotropy," *Sci. Rep.*, vol. 8, no. 1, pp. 1–12, 2018. DOI: 10.1038/S41598-018-23886-2.

[32] Z. Fan, J. Chen, and J. Wang, "Ferroelectric HfO2-based materials for next-generation ferroelectric memories," *J. Adv. Dielectr.*, vol. 06, no. 02, p. 1630003, Jun. 2016. DOI: 10.1142/S2010135X16300036.

[33] A. Chanthbouala, V. Garcia, R. O. Cherifi, K. Bouzehouane, S. Fusil, X. Moya, S. Xavier, H. Yamada, C. Deranlot, N. D. Mathur, M. Bibes, A. Barthélémy, and J. Grollier, "A ferroelectric memristor," *Nat. Mater.*, vol. 11, no. 10, pp. 860–864, 2012. DOI: 10.1038/NMAT3415.

[34] D. Kuzum, R. G. D. Jeyasingh, and H. S. P. Wong, "Energy efficient programming of nanoelectronic synaptic devices for large-scale implementation of associative and temporal sequence learning," *Tech. Dig. - Int. Electron Devices Meet. IEDM*, pp. 693–696, 2011. DOI: 10.1109/IEDM.2011.6131643.

Chapter 2 MOSFET and Steep-Switching Devices

This introductory chapter is dedicated to device operation and evolution of the metal-oxide-semiconductor (MOS) field effect transistor (FET) that forms a basis of discussion in subsequent chapters. Sections 2.1 & 2.2 introduce the physics of operation of a MOSFET and conditions for achieving sub-60 mV/dec switching. This leads on to properties of steep-switching devices, Tunnel FET (TFET), Ferroelectric FET (FE-FET), and Paraelectric FET (PE-FET) discussed in sections 2.3 – 2.6, which will serve as a basis for chapters 6 and 7. Finally, section 2.7 provides a summary of this chapter.

2.1. Operation of a Metal-Oxide-Semiconductor (MOS) FET

Fig. 2.1 (a) presents a schematic of a conventional n-channel MOSFET with a device width of W and channel or gate length L, fabricated on an acceptor-doped or p-type semiconductor. The two heavily donor-doped or n+-type regions define the source and drain, whereas the region in between forms the channel. Since the channel is p-type, it acts as a barrier between the n-doped source and drain. Hence applying a bias across drain and source V_{DS} does not produce a current through the device. An oxide separated gate is employed to electrostatically control the density of electrons within the channel. The band diagrams along the intercept $Z - Z'$ are displayed in Figs. 2.1 (b)-(d) under various bias conditions of the gate. Fig. 2.1 (b) shows the band diagrams in flat band condition, where ϕ_m and ϕ_S indicate the work functions of metal and semiconductor, while ϕ_F is the energy of the Fermi level with respect to the valence band of the semiconductor. In the flat band condition, the electric field within the oxide and semiconductor becomes zero. A gate bias V_{GS} equal to the difference of work functions $\phi_m - \phi_s = \phi_{ms}$, also referred as flat band voltage $V_{FB}(= \phi_{ms})$, is required to achieve this condition.

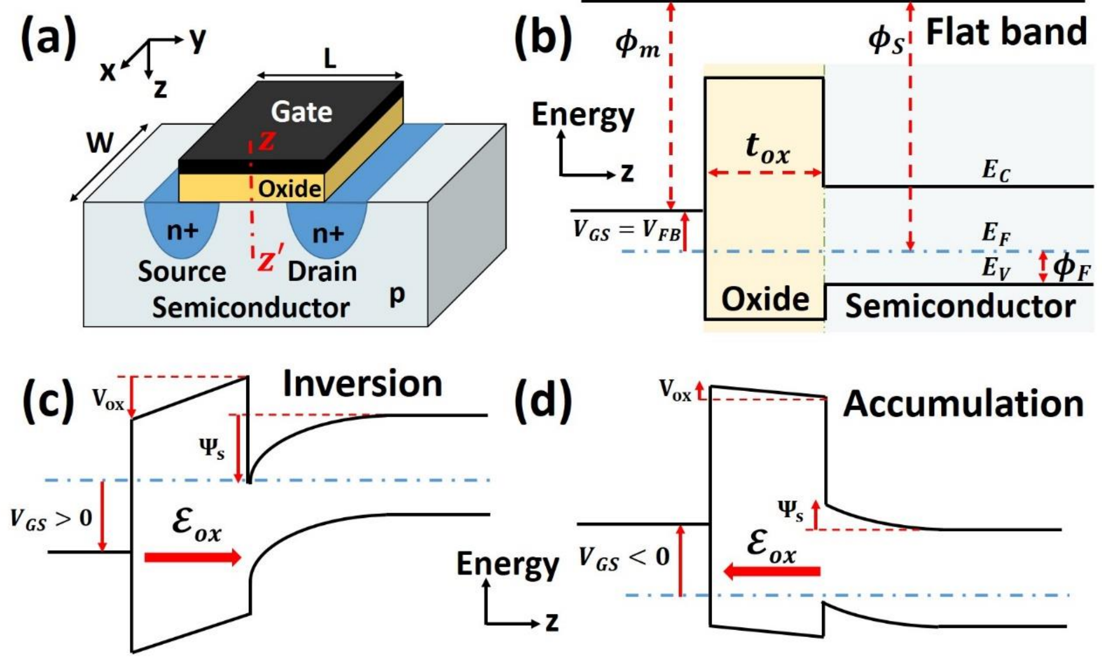

Fig. 2.1. (a) Schematic of an n-channel metal-oxide-semiconductor FET (MOSFET). The energy band diagrams along $Z - Z'$ directions in (b) flat band, (c) inversion, and (d) accumulation conditions, respectively.

2.1.1. Body Factor of a MOS

If a positive gate bias is applied, the energy of the Fermi level in the gate reduces by eV_{GS}, leading to a reduction in the energy of the conduction and valence bands in oxide and semiconductor, with part of the applied bias dropping across the oxide V_{ox} and the remaining as surface potential Ψ_s at the surface of the semiconductor, as shown in Fig. 2.1 (c). This can be expressed as

$$V_{GS} = \phi_{ms} + V_{ox} + \Psi_s \tag{2.1}$$

If a positive V_{GS} is applied such that the energy difference between the conduction band and Fermi level at the surface remains larger than ϕ_F, the energy difference between the valence band and Fermi level under flat band condition (see Fig. 2.1 (b)), the carriers in the channel remain depleted. This corresponds to the depletion condition.

To determine the change in gate bias required to produce a unit change in the surface potential ($dV_{GS}/d\Psi_s$), also referred as body factor m, we differentiate both side of Eq.

(2.1) with respect to Ψ_s

$$m = \frac{dV_{GS}}{d\Psi_s} = 1 + \frac{dV_{ox}}{d\Psi_s} = \frac{1}{1 - \frac{dV_{ox}}{dV_{GS}}} \tag{2.2}$$

Where $d\phi_{ms}/d\Psi_s = 0$ since ϕ_{ms} is a constant. As seen from Figs. 2.1 (c) and (d), since for a regular gate oxide both V_{ox} and Ψ_s always change in the same direction, $dV_{ox}/d\Psi_s$ in the above equation always remains > 0, which leads to $m > 1$, indicating that the change in Ψ_s remains smaller than that in the gate bias.

At a certain positive gate bias, the energy of the bands at the surface of the semiconductor drops such that the energy difference between the conduction band and Fermi level becomes less than ϕ_F, causing this region to become n-type. Since the surface of the semiconductor transforms from p-type, consisting of holes, to an n-type with a layer of electrons, this condition is referred to as inversion. As shown in Fig. 2.1 (c), a further increase in positive gate bias leads to the conduction band at the surface of the semiconductor sinking below the Fermi level, which leads to the formation of an e- quantum well, resulting in a two-dimensional confinement of electrons. Since an equal but positive charge is also created at the gate, this makes the entire metal-oxide-semiconductor stack to act as a capacitor, referred as MOS capacitor.

At a certain positive gate bias, the conduction band at the surface of the semiconductor sinks below the Fermi level, causing the formation of an e- quantum well, leading to a two-dimensional confinement of electrons. Since the channel transforms from a p-type semiconductor, consisting of holes, to n-type with a sheet of electrons, this condition is referred to as inversion. Since an equal but positive charge is also created at the gate, this makes the entire metal-oxide-semiconductor stack to act as a capacitor, referred as MOS capacitor.

In inversion, the sheet of electrons at the channel interface forms an electrical path

between n+ doped source and drain, thereby switching the device in the on-state. At this point, an application of V_{DS} results in I_{DS}, depending upon the density of the carriers in the channel. On the other hand, an application of negative bias on the gate raises the energy of the valence band inside the channel, bringing it closer to Fermi level, as shown in Fig. 2.1 (d), which results in an accumulation of holes at the surface of the semiconductor. Since in this mode, the channel remains p or p+, it obstructs any flow of electrons between the n+-doped source and drain regions and the device continuous to remains in off-state. Further explanations on the physics of MOS can be found in textbooks [1], [2].

2.1.2. Boltzmann Limit and Subthreshold Operation of a MOSFET

In the depletion and weak inversion conditions, since the electron concentration in the channel remains small, the carrier transport is dominated by the diffusion of electrons from source to drain region, which can be described as [2]

$$I_{DS} \propto -D_n \frac{dN}{dt} \propto \frac{N(0) - N(L_G)}{L_G} \quad (2.3)$$

Where D_n is the diffusion coefficient for the electrons, $N(0)$ and $N(L_G)$ are the sheet carrier densities at source and drain edges of the gate. $N(0)$ can be shown to have an exponential dependence upon the surface potential at the semiconductor, as $N(0) \propto \exp(q\Psi_s/k_BT)$, where k_B is Boltzmann constant, T is the temperature, and q is the elementary charge, while $N(L_G)$ is described as $N(0)\exp(-qV_{DS}/k_BT)$. Substituting the values for $N(0)$ and $N(L_G)$ in Eq. (2.3), yields

$$I_{DS} \propto \exp\left(\frac{q\Psi_s}{k_BT}\right)\left(1 - \exp\left(-\frac{qV_{DS}}{k_BT}\right)\right) \approx \exp\left(\frac{q\Psi_s}{k_BT}\right) \quad (2.4)$$

This exponential dependence upon the surface potential can also be interpreted from the band diagrams depicted in Figs. 2.2 (a) and (b) at zero and positive gate biases, respectively. At zero gate bias, the channel acts as a potential barrier for the carriers in

the source region and prevents their diffusion across the channel, as indicated in Fig. 2.2 (a). However, as the gate bias is increased, a resulting increase in surface potential Ψ_s in the channel reduces the energy of conduction and valence bands in the channel (see Fig. 2.1 (c)), leading to a lowering of the barrier and a corresponding increase in the diffusion of the carriers, thus producing an exponential rise in the drain current, as shown in Fig. 2.2 (b).

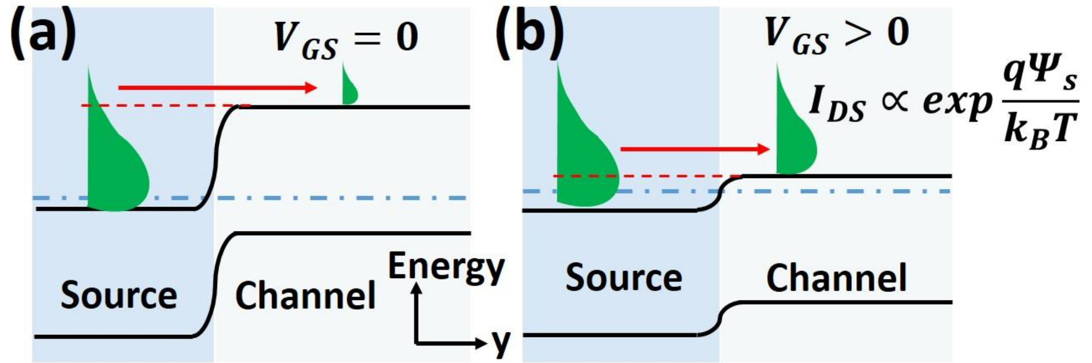

Fig. 2.2. The band diagrams in source and channel regions of the semiconductor along the oxide/semiconductor interface for (a) zero and (b) positive gate bias.

Taking the logarithm of both sides of Eq. (2.4) and differentiating with respect to Ψ_s, yields

$$\frac{d\log_{10} I_{DS}}{d\Psi_s} \approx \frac{q}{2.3\, k_B T} \tag{2.5}$$

Taking the reciprocal of the above equation

$$n = \frac{d\Psi_s}{d\log_{10} I_{DS}} \approx \frac{2.3\, k_B T}{q} \tag{2.6}$$

where n, which is a measure of the change in Ψ_s required to produce a decade of change in I_{DS}, is defined as the transport factor. From the above equation, the transport factor is approximately equal to 2.3 $k_B T/q$, referred to as the *Boltzmann limit*, indicating that at room temperature n cannot be smaller than 60 mV/dec. This suggests that in the case of a thermionic emission a change of 60 mV in Ψ_s is required to produce a decade

of change in the drain current.

From a knowledge of the body factor and transport factor, the subthreshold swing (SS), which is defined as the change in the gate bias required to produce a decade of change in the drain current, $dV_{GS}/dlog_{10}I_{DS}$, can be expressed as [3]

$$SS = \frac{dV_{GS}}{d\log_{10} I_{DS}} = \frac{dV_{GS}}{d\Psi_s}\frac{d\Psi_s}{d\log_{10} I_{DS}} = m \times n \tag{2.7}$$

As observed from Eqs. (2.2) and (2.6), $m > 1$ and $n \approx 60\, mV/dec$ at room temperature, therefore, it follows from Eq. (2.7) that SS always remains greater than $60\, mV/dec$ in a conventional MOSFET. This places a fundamental limit upon the operation of a MOSFET and leads a higher drain leakage current as the supply voltage is reduced, as discussed in Fig. 1.3 of Chapter 1.

2.2. SUB-60 MV/DEC SWITCHING, BODY FACTOR, AND NEGATIVE CAPACITANCE

Overcoming the limit of $60\, mV/dec$ of subthreshold swing of a Metal–Oxide–Semiconductor Field Effect Transistor (MOSFET) is accepted as the next evolution of CMOS scaling projected for future logic devices [3]–[5]. One of the two main approaches to achieve SS smaller than $60\, mV/dec$ is to reduce n below $60\, mV/dec$. This can be obtained by adopting a fundamentally different transport mechanism, such as band-to-band quantum mechanical tunneling in tunnel FETs (TFETs), instead of thermionic emission in a MOSFET as discussed in the next section.

The second method to achieve $SS < 60\, mV/dec$ is to enhance the coupling of the gate to the semiconductor such that the body factor m, becomes less than unity. Factors governing the value of the body factor can be understood from the relationship between the applied gate and channel surface potential, which in its simplest form is given as

$$V_{GS} = \phi_{ms} + \frac{Q_{ch}}{C_{ins}} - \frac{Q_{ox}}{C_{ins}} + \Psi_s \tag{2.8}$$

where ϕ_{ms} represents the work function difference between the gate and semiconductor, C_{ins} is the unit area capacitance of the gate insulator, Q_{ox} is the sheet charge density at the interface of the oxide and the semiconductor, and Q_{ch} is the sheet charge density in the semiconductor. Taking the derivative of Eq. (2.8) with respect to Ψ_s gives

$$\frac{dV_{GS}}{d\Psi_s} = \frac{d\phi_{ms}}{d\Psi_s} + \frac{d}{d\Psi_s}\left(\frac{Q_{ch}}{C_{ins}}\right) - \frac{d}{d\Psi_s}\left(\frac{Q_{ox}}{C_{ins}}\right) + 1 \tag{2.9}$$

In the case of a conventional MOSFET as ϕ_{ms}, C_{ins} and Q_{ox} are constants, the above equation reduces to

$$m = \frac{dV_{GS}}{d\Psi_s} = 1 + \frac{1}{C_{ins}}\frac{dQ_{ch}}{d\Psi_s} = 1 + \frac{C_{dep}}{C_{ins}} \geq 1 \tag{2.10}$$

where $dQ_{ch}/d\Psi_s$ in the subthreshold regime is the depletion capacitance C_{dep}. In terms of voltage across the oxide, the body factor can be written as

$$m = \frac{1}{\frac{d\Psi_s}{dV_{GS}}} \Rightarrow m = \frac{1}{\frac{d(V_{GS} - \phi_{ms} - V_{ox})}{dV_{GS}}} \Rightarrow m = \frac{1}{1 - \frac{dV_{ox}}{dV_{GS}}} \tag{2.11}$$

Since for a regular dielectric material as the gate insulator, C_{ins} and C_{dep} are always non-negative, body factor from Eq. (2.10) always remains greater than 1, leading to a subthreshold swing $> 60\ mV/dec$. It follows from Eq. (2.11), an $m > 1$ results in $0 < dV_{ox}/dV_{GS} < 1$ i.e. a change in the voltage across the dielectric is always smaller than the change in applied gate bias and remains in-phase with V_{GS}. On the other hand, in a FE-FET, where a ferroelectric material is utilised as the gate dielectric, C_{ins} is replaced with C_{FE}, which can become negative, as will be shown in section 2.4, resulting in $m < 1$, or equivalently $SS < 60\ mV/dec$ [6].

2.3. OPERATION OF A TFET

Unlike MOSFETs where the source to drain path consists of n-p-n or p-n-p doped semiconductor regions for n-type and p-type devices, TFETs employ a p-i-n or n-i-p doped semiconductor structure, where source and drain regions are doped degenerately of opposite polarity, as depicted in Fig. 2.3 (a). At zero gate bias, due to presence of the intrinsic channel, a bias across source and drain V_{DS} does not result in any drain-current and the device remains in the OFF-state, as seen from the band diagram in Fig. 2.3 (b). An application of a positive gate bias lowers the energy of valence and conduction bands in the channel region, which causes an overlap of the conduction band in the channel with the valence band in the source region across a small distance, typically less than $10\ nm$. This enables the carriers in these regions to tunnel between these bands across the potential barrier introduced by the bandgap, via a band-to-band quantum mechanical tunneling (BBT), as indicated by the red arrow in Fig. 2.3 (c). Therefore, the device switches to the ON-state, and allows conduction, upon the application of V_{DS}. Fig. 2.3 (d) shows the band diagram for a negative gate bias that raises the energy level of bands in the channel region. As marked by a red arrow in this figure, a similar overlap between the valence band in the channel and conduction band in drain facilitates BBT between these regions, and causes the device to turn-on. Therefore, unlike MOSFETs which are non-ambipolar (i.e. turn-on either with positive or negative gate bias only) TFETs are ambipolar devices and can be turned on via non-zero gate bias in either direction of the bias. Ambipolarity is one of the main challenges with TFETs that leads to a higher leakage and makes their operation unreliable in CMOS logic applications.

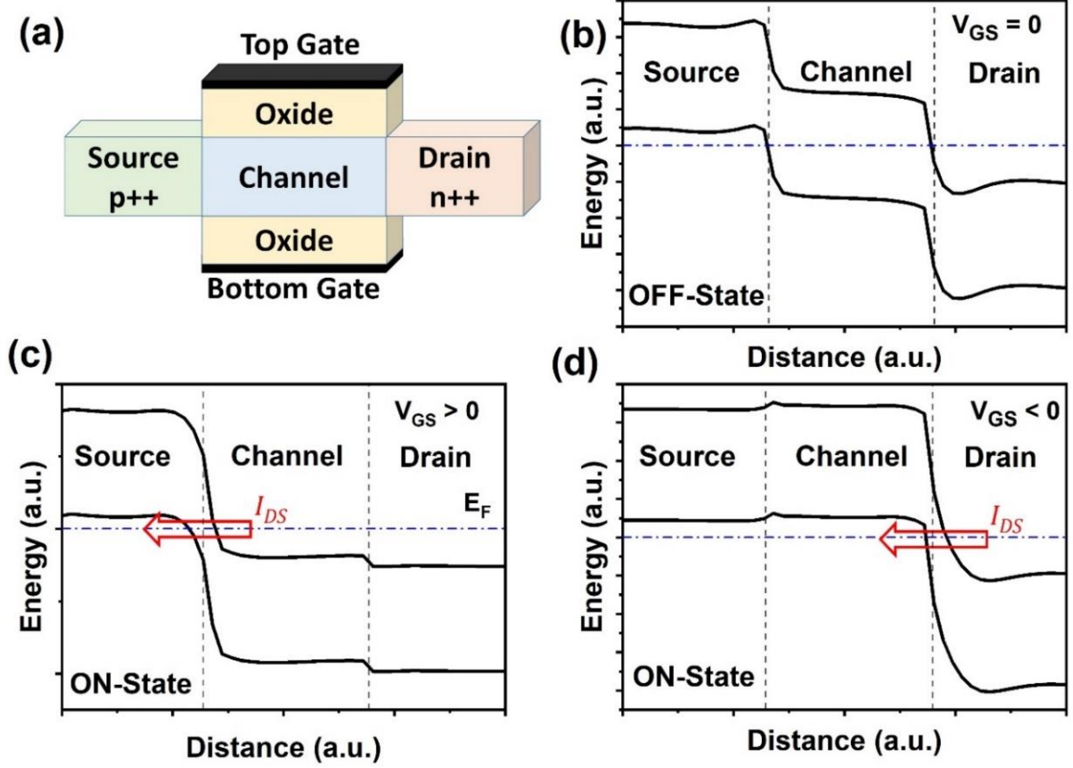

Fig. 2.3. (a) Schematic of typical double gate TFET, and the typical band diagrams at (b) $V_{GS} = 0$, (c) $V_{GS} > 0$, and (d) $V_{GS} < 0$.

Since the transport in a TFET is provided by BBT, fundamentally different from MOSFET, the device can potentially achieve a transport factor n (Eq. (2.6)) below $2.3k_BT/q$, bringing SS below $60\ mV/dec$. The tunneling probability $\mathcal{T}_{WKB}$ across a potential barrier of height $\mathcal{V}(x)$ can be described under a Wentzel-Kramers-Brillouin (WKB) approximation as [2]:

$$\mathcal{T}_{WKB} \approx \exp\left(-2\int_0^{D_{Tun}} |\kappa(x)| dx\right) \tag{2.12}$$

where, D_{Tun} is the band-to-band tunneling distance and $|\kappa(x)| = \sqrt{2m^*\mathcal{V}(x)\ /\ \hbar}$ is the absolute value of the wave vector of carriers of effective mass m^* inside the tunnel barrier. It can be observed from Eq. (2.12) that the tunneling probability, responsible for the current in the device, decays exponentially with D_{Tun}. Consequently, the drain current in TFETs has been historically worse than in CMOS. Table 2.1 summarises the

reported experimental results for minimum SS and the corresponding ON-current I_{ON} for the TFETs achieving SS$< 60\ mV/dec$. Whereas, the highest drain-current TFET with SS still below $60\ mV/dec$ has been reported to be in the range of $1 - 10\ \mu A/mm$ [7], orders of magnitude lower than the desired $\sim 1\ A/mm$. Therefore, attempts are being made to shrink D_{Tun}, by incorporation of a highly doped pocket in the channel, which increases the field at the point of tunneling [8]. In addition, semiconductor materials with dissimilar bandgaps, e.g. heterostructures of III-V compound semiconductors and their alloys, have been utilised to lower the barrier height, which have demonstrated a significant improvement in SS over Si-TFETs [9].

Table 2.1. Experimental results for TFETs with subthreshold swing below $60\ mV/dec$.

Reference	**Material System**	SS_{min} **(mV/dec)**	I_{ON} **(mA/mm) with** SS_{min}
J. Appenzeller *et al.* 2004 [10]	Carbon-nanotube	40	0.01
W. Y. Choi *et al.* 2007 [11]	Silicon	53	~10
T. Krishnamohan *et al.* 2008 [12]	Strained-Ge/Si	50	0.1
K. Tomioka *et al.* 2012 [13]	Si/InAs Nanowire	21	1
L. Knoll *et al.* 2013 [14]	Strained-Si Nanowire	30	10
E. Memisevic *et al.* 2016 [9]	InAs/GaAsSb/GaSb	48	~20

2.4. PHYSICS OF FERROELECTRIC MATERIALS

The approach of including a layer of ferroelectric material between the gate and semiconductor channel is another potential way for reducing the operating voltage in CMOS, as discussed in chapter 1. The unique negative capacitance phenomenon in a ferroelectric can provide voltage amplification at the semiconductor channel that can lead to a body factor less than unity, resulting in the subthreshold swing of transfer

characteristics beyond that conceivable in conventional MOSFETs. In this section, we will review the properties of Ferroelectric materials, the two phases of these materials, namely ferroelectric (below Curie temperature) and paraelectric (above Curie temperature), describe the negative capacitance, R-C circuit equivalent models for these materials, and how they affect the operation of an FET, when employed as a gate oxide.

Ferroelectric materials consist of domains of electric dipoles, which can respond to and change their direction of polarisation according to the applied external bias. Unlike ordinary dielectrics where the free energy density U follows a quadratic relationship with respect to the sheet charge density that appears across its terminals, the free-energy density in a typical ferroelectric material is described by a polynomial equation as [15]

$$U = \alpha P^2 + \beta P^4 + \gamma P^6 - P\mathcal{E} \tag{2.13}$$

Where $\alpha(= 1/\varepsilon_r\varepsilon_0)$ is equivalent to the inverse of the dielectric permittivity from the common relationship between electric field $\mathcal{E}$ and polarisation, β and γ are material dependent constants, $\mathcal{E}$ is the electric field, and P is the sheet charge density due to polarisation. In a ferroelectric, α remains less than zero, which results in two local minima from Eq. (2.13), positive and negative spontaneous polarisation states [16], as shown in Fig. 2.4 (a) at $\mathcal{E} = 0$. Therefore, without an external electric field, a ferroelectric contains a remnant polarisation P_R, corresponding to one of the minima in $U - P$ curve. α in a ferroelectric material exhibits temperature dependence, which following the Curie-Weiss law ($\epsilon_r = C/(T - T_{ph})$), can be described as [16]

$$\alpha = \frac{T - T_{ph}}{\varepsilon_0 C} \tag{2.14}$$

C is the Curie constant, T_{ph} is equal to or lower than the Curie temperature. While the temperature is less T_{ph}, α remains negative, and the material exhibits the ferroelectric phase. However, as the temperature exceeds T_{ph}, the increase in thermal energy disrupts

the alignment of the electric domains in the material, leading to a loss of polarity in the absence of an external electric field, which corresponds to the paraelectric phase, with α greater than zero. U vs. P for a paraelectric material reduces to a single valley energy profile, with a minimum at $P = 0$ when electric field is zero, as shown in Fig. 2.4 (b). Therefore, unlike ferroelectrics, paraelectrics do not contain any remnant polarisation in the absence of an electric field.

In the presence of an electric field, however, these curves become tilted due to the dependence of U upon $\mathcal{E}$ in Eq. (2.13), as indicated by the brown arrows in Figs. 2.4 (a) & (b), resulting in one of the minima to become more favourable in the case of a ferroelectric, or causing the minimum to shift from the origin for the case of a paraelectric, leading to a development of finite polarisation.

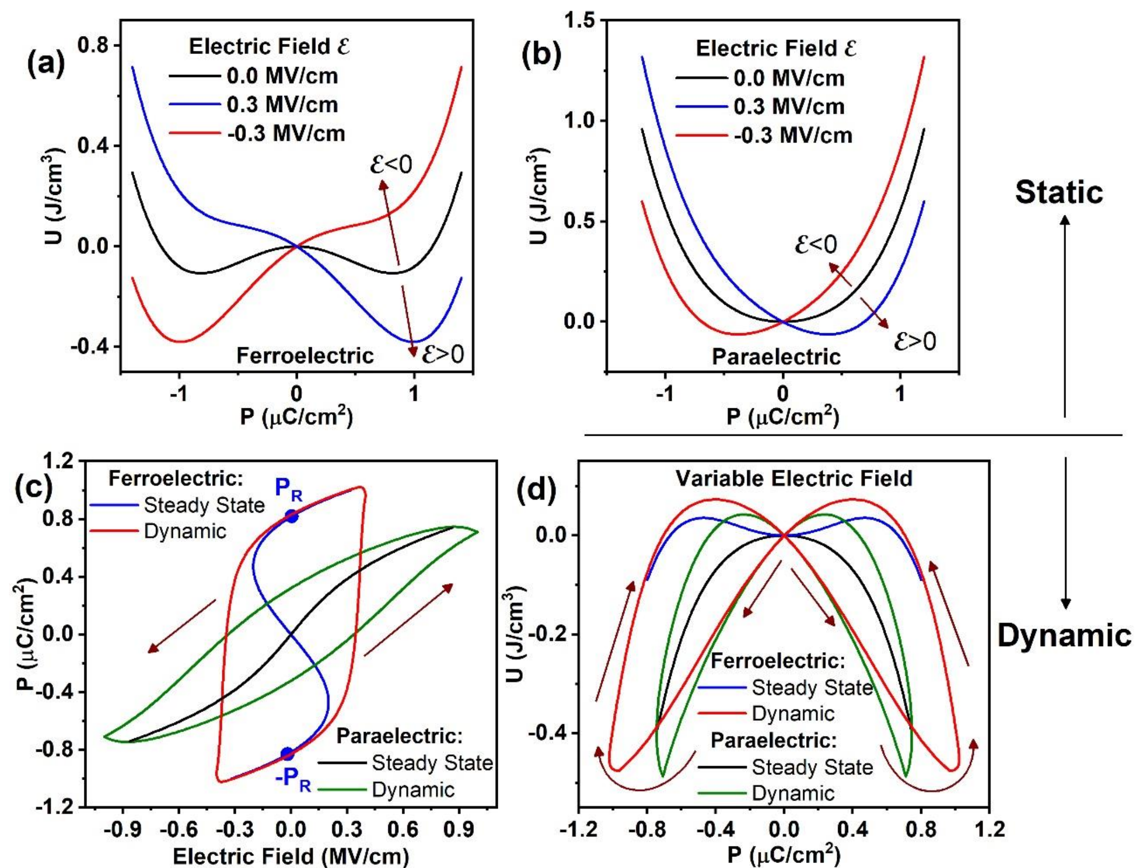

Fig. 2.4. Simulated energy profiles, U for (a) the ferroelectric and (b) paraelectric phases as a function of polarisation, P at different electric fields. (c) Comparison of P vs. electric field for

FE and PE in steady state and under the dynamic sweep of the electric field with a frequency of $50\ MHz$, and (d) corresponding U vs. P for ferroelectric and paraelectric where the electric field changes as shown in (c). Here, $\alpha = -3.2 \times 10^{11} cm/F$ for ferroelectric and $3.2 \times 10^{11} cm/F$ for paraelectric, while β and γ of $6.8 \times 10^{23} cm^5/FC^2$ and 0 for both ferro- and para- electrics are used.

The dynamic behaviour of ferroelectric or paraelectric under continuously varying $\mathcal{E}$ is described by the Landau-Khalatnikov (L-K) equation as [17]

$$\rho \frac{dP}{dt} = -\frac{dU}{dP} \tag{2.15}$$

Substituting U from Eq. (2.13) leads to the desired relationship between $\mathcal{E}$ and P

$$\rho \frac{dP}{dt} = -2\alpha P - 4\beta P^3 - 6\gamma P^5 + \mathcal{E} \tag{2.16}$$

where ρ is a damping coefficient associated with the material, which determines the switching rate or a hysteresis in the dynamic behaviour of a ferroelectric material. P vs. $\mathcal{E}$ from Eq. (2.15) in the steady state i.e. ($dP/dt = 0$) and under dynamic $\mathcal{E}$ are plotted in Fig. 2.4 (c). In the steady state, the P vs. $\mathcal{E}$ curve in ferroelectric exhibits an 'S' shaped characteristic with a negative-slope ($dP/d\mathcal{E} < 0$) around the origin, which is an unstable region, and causes the polarisation to settle into one of two residual states at $\mathcal{E} = 0$, marked by $\pm P_R$ in Fig. 2.4 (c). P vs. $\mathcal{E}$ in a paraelectric does not show such a region with negative slope. Therefore, P remains zero at zero electric field. This dissimilarity however, vanishes under a dynamic sweep, where both ferro- and para- electrics show non-zero P at $\mathcal{E} = 0$, giving rise to an anti-clockwise hysteresis. This hysteresis arises because the term $\rho\ dP/dt$ in Eq. (2.16) slows down the maximum rate of change in P, introducing a delay in the change in P with respect to a change in the electric field. This leads to a non-zero polarisation at zero electric field with an anti-clockwise hysteresis. Fig. 2.4 (d) compares the U vs. P characteristics of both materials in steady state and dynamic conditions, as electric field changes according to that shown in Fig. 2.4 (c). Fig.

2.4 (d) further confirms the similarity of the two materials under dynamic operation.

2.4.1. Equivalent Series R-C Circuit Model

Since the parallel plate capacitance of a layer of dielectric is related to its stored energy density as $C = \left(t\frac{d^2U}{dQ^2}\right)^{-1}$, where t is the layer thickness or distance between the electrodes, we can apply the same procedure to obtain an expression for the unit-area capacitance of a ferroelectric or paraelectric $C_{F/P}$, while substituting U from Eq. (2.13) with $\mathcal{E}$ equals to zero, which leads to

$$C_{F/P}^{-1} = t(2\alpha + 12\beta Q^2 + 24\gamma Q^4) \tag{2.17}$$

where P is expressed as the sheet charge density Q that appears across the terminals of insulator of thickness t. Since the double derivative of any given curve becomes negative wherever the curve becomes convex (a local maximum), $C_{F/P}$ becomes negative, where U vs. P in Fig. 2.4 (a) shows a maximum (see black curve around origin). This also corresponds to the region of P vs. $\mathcal{E}$ plot in Fig. 2.4 (c), where its slope becomes negative.

Utilising Eq. (2.17), it is possible to construct an equivalent non-linear RC circuit from Eq. (2.16) [15]. If V is the bias applied across an insulator of thickness t, substituting $\mathcal{E} = V/t$, $Q = P$, and $C_{F/P}$ from Eq. (2.17) into Eq. (2.16)

$$V = \rho t\frac{dQ}{dt} + \int \frac{dQ}{C_{F/P}} = RI + \int \frac{dQ}{C_{F/P}} \tag{2.18}$$

Eq. (2.18) represents a series non-linear RC circuit with $R = \rho t$ with $C_{F/P}$ described according to Eq. (2.17). Owing to the delay introduced by this series RC circuit, originating from the finite response of polarisation with respect to external electric field, we observe a remnant polarisation for a paraelectric in Fig. 2.4 (c) under dynamic electric field. However, an important distinction is that while in a paraelectric, the non-linear

capacitor, always remains positive, it can become negative for a ferroelectric in a certain range of operation, owing to $\alpha < 0$ for this material.

2.5. Operation of a FE-FET

A flow diagram for simulating the dynamic characteristics for either FE- or PE- FET is illustrated in Fig. 2.5 (a). At a given gate bias, first a value of Ψ_s is guessed, and the corresponding sheet charge density in the channel Q_{ch} is obtained by solving the one-dimensional Poisson equation along with the density of carriers, which is determined by integrating the density of states in the channel together with the potential dependent Fermi-Dirac distribution of carriers within the channel. This procedure can be summarised as $Q_{ch} = f(\Psi_s)$, as shown in Fig. 2.5 (a). The values for Q_{ch} and $V_{ox}(= V_{GS} - \phi_{ms} - \Psi_s)$ are substituted into L-K equation (Eq. (2.16)) to generate a new value for Ψ_s, which is used in the subsequent calculation of Q_{ch}. This process is repeated until the change in Ψ_s becomes smaller than some desirable tolerance. For each of the applied gate bias point, the entire procedure is repeated to obtain the final value for Q_{ch}. From the converged values of Q_{ch}, the drain current I_{DS} is obtained simply as:

$$I_{DS} = \mu \frac{W}{L} Q_{ch} V_{DS} \tag{2.19}$$

where μ is the mobility of carriers in the semiconducting channel, W and L are the width and length of the device, and V_{DS} is the drain to source bias. The results for I_{DS} from Eq. (2.19) of an FE-FET at different scan frequencies of gate bias are plotted in Fig. 2.5 (b). Owing to the instability in the FE, steep switching is observed during both the forward and backward sweeps of gate bias. It has been explained in the literature by a sudden change in the polarisation state of the FE that causes a change in the density of carriers in channel and results in amplification [18]. At low frequency, the slope dV_{ox}/dV_{GS} becomes less than zero during both directions of the sweep of V_{GS}, resulting

in a body factor $m < 1$, according to Eq. (2.11). At higher frequency, the counter-clockwise hysteresis in the transfer characteristics of the device follows from the ferroelectric properties, observed in Fig. 2.4 (c), following the L-K equation. The increase in the hysteresis with frequency arises from the finite time taken by the ferroelectric domains to respond to the changing electric field, controlled by ρ in Eq. (2.16). A high remnant polarisation in the ferroelectric maintains the surface potential of the channel Ψ_s during the reverse sweep, while the majority of the reduction in applied gate voltage is dropped across the ferroelectric, V_{ox}, which thereby achieves a minimum in Fig. 2.5 (c). However, as the gate voltage is further reduced, a change in the state of polarisation leads to a depletion in the channel and a corresponding reduction in Ψ_s, while V_{ox} increases to its initial value. This increase in V_{ox} during a reduction of V_{GS} leads to $dV_{ox}/dV_{GS} < 0$, thereby producing $m < 1$ from Eq. (2.11). Fig. 2.5 (d) reveals a $SS < 60\ mV/dec$ at low frequency in both the forward and backward directions of V_{GS}. With an increase in frequency, the increase in the width of the hysteresis in the transfer characteristics becomes larger. As a result, SS during the forward sweep degrades, increasing above 60 mV/dec at a frequency of $\sim 3\ MHz$, while in the backward sweep, it becomes as low as $\sim 5\ mV/dec$. Employing a ferroelectric material to boost the SS does not always guarantee a sub-60 mV/dec operation. Since a ferroelectric affects the body factor, the amplification depends upon the performance of the underlying MOSFET via the factor $n(= d\log I_{DS}/d\Psi_s)$. Moreover, the observed SS in FE-FETs can fluctuate owing to non-idealities such as multi-domain ferroelectricity, diverse polarisation [19] or gate leakage [20].

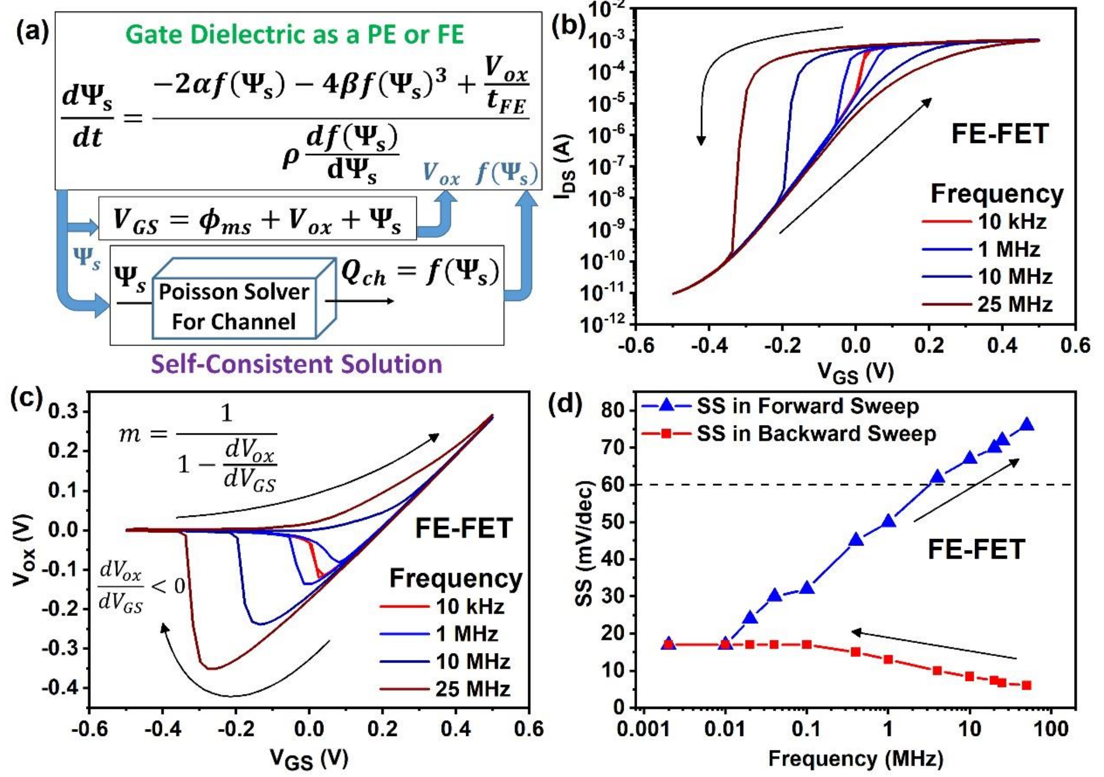

Fig. 2.5. (a) A flow diagram showing the self-consistent coupling of the L-K equation with the semiconductor channel for computing the drain current in FE- or PE- FET. (b) Simulated transfer characteristics, (c) voltage across the ferroelectric gate insulator V_{ox} vs. the applied gate bias V_{GS} at different frequency of gate bias sweep. (d) SS vs. scan frequency in both directions of gate bias sweep for a ferroelectric FET (FE-FET). A sub-60 mV/dec switching is present at low frequency (where hysteresis virtually disappears). At higher frequency, the width of the hysteresis increases and the switching becomes more gradual because of the finite rate of change in the polarisation controlled by the parameter ρ in Eq. (2.16). where α, β, γ, and ρ of $-3.2 \times 10^{11} cm/F$, $6.8 \times 10^{23} cm^5/FC^2$, 0, 3000 $\Omega\, cm$ are used.

Fig. 2.6 highlights reported results in ferroelectric FETs meant for mainstream CMOS applications. Many of these are based on devices with long channel lengths, while the drain current does not exceed 6 mA/mm, at least 3 orders of magnitude lower than the accepted benchmark ($\sim 1\ A/mm$).

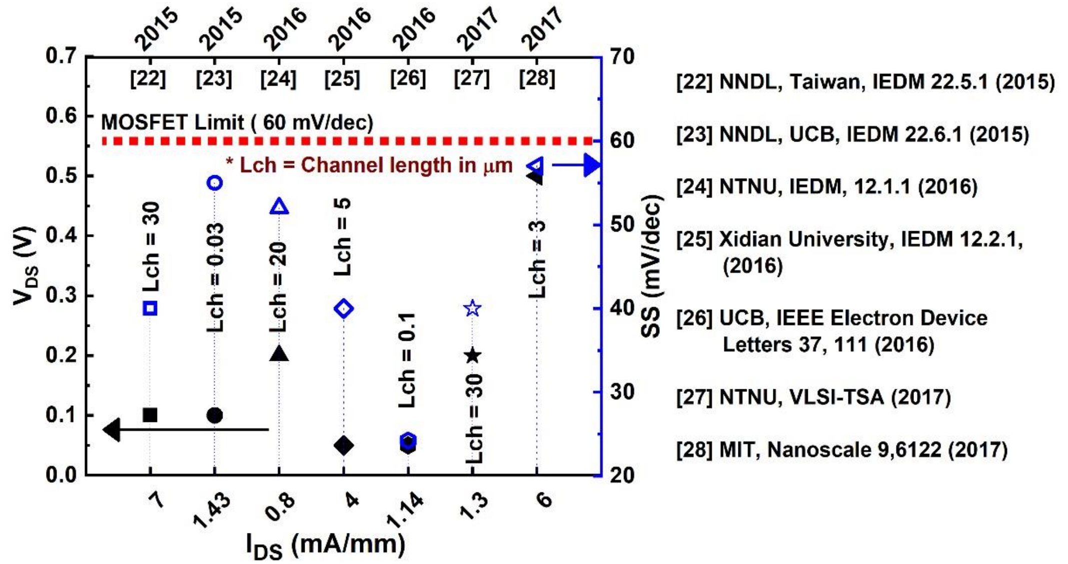

Fig. 2.6. Recent experimental results of reported ferroelectric FETs for CMOS applications. [21]–[27]

2.6. Operation of a PE-FET

The operation of a paraelectric (PE) –FET can also be simulated in a similar fashion to a FE-FET by simply replacing the ferroelectric by a paraelectric (PE) material. The transfer characteristics of a PE-FET, plotted in Fig. 2.7 (a), show no steep-switching at low scan frequency of V_{GS}, but the slope of the drain-current becomes steeper during the backward sweep as the frequency is increased. Further investigation of the V_{ox} vs. V_{GS} in Fig. 2.7 (b) reveals that at low frequency, the slope dV_{ox}/dV_{GS} remains positive, resulting in $m > 1$. At higher frequency, dV_{ox}/dV_{GS} turns negative only in the backward sweep, leading to $m < 1$ (Eq. (2.11)). Fig. 2.7 (c) indicates that the SS remains greater than $60\ mV/dec$ at low frequency in both forward and backward directions of V_{GS} sweep, but become less than $60\ mV/dec$ in the backward sweep as the frequency of gate bias sweeps exceeds $12\ MHz$ (for this value of ρ). As we observed, the capacitance for a PE in Eq. (2.17) always remains greater than zero, implying that the observed sub-$60\ mV/dec$ of switching originates from a different mechanism. In fact, owing to the equivalent series R-C circuit representation of L-K equation in Eq. (2.18), the

paraelectric insulator introduces a delay in propagating the variations in V_{GS} to the surface of the semiconductor, causing a phase difference between V_{GS} and Ψ_s. Due to this phase difference, the change in Ψ_s becomes greater than the corresponding change in V_{GS} at high frequency, that is $dV_{GS}/d\Psi_s < 1$, or equivalently $dV_{ox}/dV_{GS} < 1$, from Eq. (2.2) since $\Psi_s = V_{GS} - \phi_{ms} - V_{ox}$. Consequently, sub-60 mV/dec switching in the dynamic characteristics of PE-FETs is possible via an equivalent R-C type behaviour represented by an equivalent circuit based on the L-K equation during the backward scan of the gate bias depending upon the frequency.

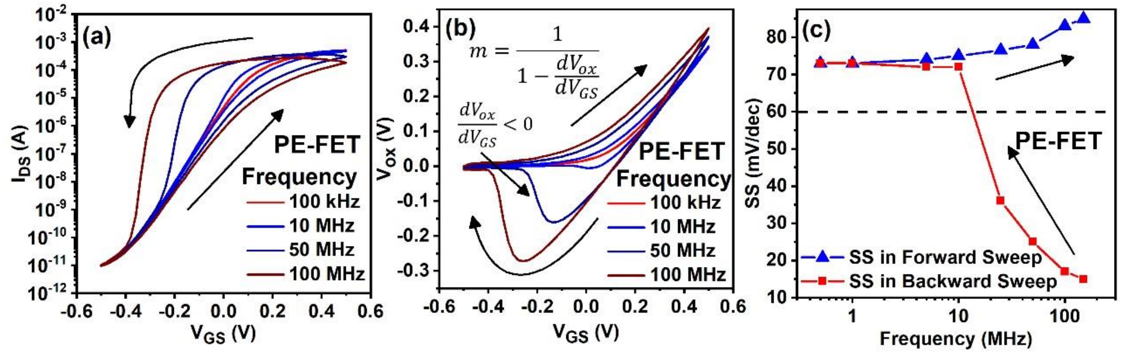

Fig. 2.7. (a) Simulated transfer characteristics of a PE-FET with gate scan frequency (b) Voltage across the paraelectric gate insulator V_{ox} vs. the applied gate bias V_{GS}, and (c) SS vs. frequency of gate bias sweep in forward and reverse directions for a PE-FET. No steep-switching at low frequency is present in either forward or backward direction of sweep. At a scan frequency > 15 MHz, the device shows a $SS < 60\ mV/dec$ in the backward sweep for chosen parameters, where α, β, γ, and ρ of $3.2 \times 10^{11} cm/F$, $6.8 \times 10^{23} cm^5/FC^2$, 0, and 3000 $\Omega\ cm$ are used.

2.7. SUMMARY

In this chapter, we have reviewed the operation of MOSFET, physics of steep switching devices such as a tunnel and ferroelectric FET (TFET and FE-FET) and their distinction from paraelectric FETs. We have demonstrated that under dynamic conditions the energy well profiles of FE-FETs and PE-FETs can be somewhat indistinguishable, but the frequency dependence of the SS is a useful method of identifying the physics of operation of these two FETs. These concepts will provide a foundation for the discussion

of this work in the subsequent chapters.

2.8. REFERENCE

[1] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*. Cambridge University Press, 2002. DOI: 10.1109/LED.2004.837581.

[2] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*. John Wiley & Sons, 2006.

[3] A. M. Ionescu and H. Riel, "Tunnel field-effect transistors as energy-efficient electronic switches," *Nature*, vol. 479, no. 7373, pp. 329–337, Nov. 2011. DOI: 10.1038/NATURE10679.

[4] D. E. Nikonov and I. A. Young, "Overview of Beyond-CMOS Devices and a Uniform Methodology for Their Benchmarking," *Proc. IEEE*, vol. 101, no. 12, pp. 2498–2533, Dec. 2013. DOI: 10.1109/JPROC.2013.2252317.

[5] International Technology Roadmap for Semiconductors (ITRS), "More Moore," *ITRS*, 2015. [Online]. Available: http://www.itrs2.net/itrs-reports.html. [Accessed: 10-Dec. 2018].

[6] S. Salahuddin and S. Datta, "Use of Negative Capacitance to Provide Voltage Amplification for Low Power Nanoscale Devices," *Nano Lett.*, vol. 8, no. 2, pp. 405–410, Feb. 2008. DOI: 10.1021/NL071804G.

[7] H. Lu and A. Seabaugh, "Tunnel Field-Effect Transistors: State-of-the-Art," *IEEE J. Electron Devices Soc.*, vol. 2, no. 4, pp. 44–49, Jul. 2014. DOI: 10.1109/JEDS.2014.2326622.

[8] H. Y. Chang, B. Adams, P. Y. Chien, J. Li, and J. C. S. Woo, "Improved subthreshold and output characteristics of source-pocket Si tunnel FET by the application of laser annealing," *IEEE Trans. Electron Devices*, vol. 60, no. 1, pp. 92–96, 2013. DOI: 10.1109/TED.2012.2228006.

[9] E. Memisevic, J. Svensson, M. Hellenbrand, E. Lind, and L.-E. Wernersson, "Vertical InAs/GaAsSb/GaSb tunneling field-effect transistor on Si with S = 48 mV/decade and Ion = 10 μA/μm for Ioff = 1 nA/μm at Vds = 0.3 V," in *2016 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2016, p. 19.1.1-19.1.4. DOI: 10.1109/IEDM.2016.7838450.

[10] J. Appenzeller, Y.-M. Lin, J. Knoch, and P. Avouris, "Band-to-Band Tunneling in Carbon Nanotube Field-Effect Transistors," *Phys. Rev. Lett.*, vol. 93, no. 19, p. 196805, Nov. 2004. DOI: 10.1103/PHYSREVLETT.93.196805.

[11] Woo Young Choi, Byung-Gook Park, Jong Duk Lee, and Tsu-Jae King Liu, "Tunneling Field-Effect Transistors (TFETs) With Subthreshold Swing (SS) Less Than 60 mV/dec," *IEEE Electron Device Lett.*, vol. 28, no. 8, pp. 743–745, Aug. 2007. DOI:

10.1109/LED.2007.901273.

[12] T. Krishnamohan, D. Kim, S. Raghunathan, and K. Saraswat, “Double-Gate Strained-Ge Heterostructure Tunneling FET (TFET) With record high drive currents and <60mV/dec subthreshold slope,” in *2008 IEEE International Electron Devices Meeting*, Dec. 2008, vol. 67, no. May 2006, pp. 1–3. DOI: 10.1109/IEDM.2008.4796839.

[13] K. Tomioka, M. Yoshimura, and T. Fukui, “Steep-slope tunnel field-effect transistors using III-V nanowire/Si heterojunction,” in *2012 Symposium on VLSI Technology (VLSIT)*, Jun. 2012, pp. 47–48. DOI: 10.1109/VLSIT.2012.6242454.

[14] L. Knoll, Q.-T. Zhao, A. Nichau, S. Trellenkamp, S. Richter, A. Schafer, D. Esseni, L. Selmi, K. K. Bourdelle, and S. Mantl, “Inverters With Strained Si Nanowire Complementary Tunnel Field-Effect Transistors,” *IEEE Electron Device Lett.*, vol. 34, no. 6, pp. 813–815, Jun. 2013. DOI: 10.1109/LED.2013.2258652.

[15] A. I. Khan, K. Chatterjee, B. Wang, S. Drapcho, L. You, C. Serrao, S. R. Bakaul, R. Ramesh, and S. Salahuddin, “Negative capacitance in a ferroelectric capacitor.,” *Nat. Mater.*, vol. 14, no. 2, pp. 182–6, 2015. DOI: 10.1038/NMAT4148.

[16] S. Gevorgian, *Ferroelectrics in Microwave Devices, Circuits and Systems: Physics, Modeling, Fabrication and Measurements*. London: Springer London, 2009. DOI: 10.1007/978-1-84882-507-9.

[17] L. D. Landau and I. M. Khalatnikov, “On the anomalous absorption of sound near a second order phase transition point,” in *Dokl. Akad. Nauk SSSR*, vol. 96, 1954, pp. 469–472.

[18] J. Zhou, G. Han, Q. Li, Y. Peng, X. Lu, C. Zhang, J. Zhang, Q.-Q. Sun, D. W. Zhang, and Y. Hao, “Ferroelectric HfZrOx Ge and GeSn PMOSFETs with Sub-60 mV/decade Subthreshold Swing, Negligible Hysteresis, and Improved IDS,” in *2016 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2016, p. 12.2.1-12.2.4. DOI: 10.1109/IEDM.2016.7838401.

[19] J. Jo and C. Shin, “Negative Capacitance Field Effect Transistor With Hysteresis-Free Sub-60-mV/Decade Switching,” *IEEE Electron Device Lett.*, vol. 37, no. 3, pp. 245–248, Mar. 2016. DOI: 10.1109/LED.2016.2523681.

[20] A. I. Khan, U. Radhakrishna, K. Chatterjee, S. Salahuddin, and D. A. Antoniadis, “Negative Capacitance Behavior in a Leaky Ferroelectric,” *IEEE Trans. Electron Devices*, vol. 63, no. 11, pp. 4416–4422, 2016. DOI: 10.1109/TED.2016.2612656.

[21] M. H. Lee, P.-G. Chen, C. Liu, K. Chu, C.-C. Cheng, M.-J. Xie, S.-N. Liu, J.-W. Lee, S.-J. Huang, M.-H. Liao, M. Tang, K.-S. Li, and M.-C. Chen, “Prospects for ferroelectric HfZrOx FETs with experimentally CET=0.98nm, SSfor=42mV/dec, SSrev=28mV/dec, switch-off 0.2V, and hysteresis-free strategies,” in *2015 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2015, p. 22.5.1-22.5.4. DOI:

10.1109/IEDM.2015.7409759.

[22] K.-S. Li, P.-G. Chen, T.-Y. Lai, C.-H. Lin, C.-C. Cheng, C.-C. Chen, Y.-J. Wei, Y.-F. Hou, M.-H. Liao, M.-H. Lee, M.-C. Chen, J.-M. Sheih, W.-K. Yeh, F.-L. Yang, S. Salahuddin, and C. Hu, "Sub-60mV-swing negative-capacitance FinFET without hysteresis," in *2015 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2015, vol. 2016–Febru, p. 22.6.1-22.6.4. DOI: 10.1109/IEDM.2015.7409760.

[23] M. H. Lee, S.-T. Fan, C.-H. Tang, P.-G. Chen, Y.-C. Chou, H.-H. Chen, J.-Y. Kuo, M.-J. Xie, S.-N. Liu, M.-H. Liao, C.-A. Jong, K.-S. Li, M.-C. Chen, and C. W. Liu, "Physical thickness 1.x nm ferroelectric HfZrOx negative capacitance FETs," in *2016 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2016, p. 12.1.1-12.1.4. DOI: 10.1109/IEDM.2016.7838400.

[24] J. Zhou, G. Han, Q. Li, Y. Peng, X. Lu, C. Zhang, J. Zhang, Q.-Q. Sun, D. W. Zhang, and Y. Hao, "Ferroelectric HfZrOx Ge and GeSn PMOSFETs with Sub-60 mV/decade subthreshold swing, negligible hysteresis, and improved Ids," in *2016 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2016, p. 12.2.1-12.2.4. DOI: 10.1109/IEDM.2016.7838401.

[25] A. I. Khan, K. Chatterjee, J. P. Duarte, Z. Lu, A. Sachid, S. Khandelwal, R. Ramesh, C. Hu, and S. Salahuddin, "Negative Capacitance in Short-Channel FinFETs Externally Connected to an Epitaxial Ferroelectric Capacitor," *IEEE Electron Device Lett.*, vol. 37, no. 1, pp. 111–114, Jan. 2016. DOI: 10.1109/LED.2015.2501319.

[26] M. H. Lee, P.-G. Chen, S.-T. Fan, C.-Y. Kuo, H.-H. Chen, S.-S. Gu, Y.-C. Chou, C.-H. Tang, R.-C. Hong, Z.-Y. Wang, M.-H. Liao, K.-S. Li, M.-C. Chen, and C. W. Liu, "Negative capacitance FETs with steep switching by ferroelectric Hf-based oxide," in *2017 International Symposium on VLSI Technology, Systems and Application (VLSI-TSA)*, Apr. 2017, pp. 1–2. DOI: 10.1109/VLSI-TSA.2017.7942466.

[27] A. Nourbakhsh, A. Zubair, S. Joglekar, M. Dresselhaus, and T. Palacios, "Subthreshold swing improvement in MoS 2 transistors by the negative-capacitance effect in a ferroelectric Al-doped-HfO 2 /HfO 2 gate dielectric stack," *Nanoscale*, vol. 9, no. 18, pp. 6122–6127, 2017. DOI: 10.1039/C7NR00088J.

Chapter 3 Fundamentals of GaN and Heterostructure Devices

This chapter introduces the material properties of GaN and describes the physics of devices based on GaN hetersotructures. This chapter is organised as follows. Sections 3.1 – 3.4 are dedicated to an introduction to GaN, polarisation properties of GaN, and formation of polarisation induced two dimensional electron and hole gases (2DEG & 2DHG). In sections 3.5 – 3.6, the operation of MOS in GaN heterostructures and n-channel MOS heterostructure FETs (HFETs) are introduced that underlie the theory of p-channel MOSHFETs in chapters 4 and 5 of this work.

3.1. WHY GAN?

Si based MOSFET devices have greatly affected various aspects of our lives. MOSFETs have been used as signal amplifiers, low power or high power switches. However, the modest mobility (~1400 cm^2/Vs), low band gap (1.1 eV) and small breakdown voltage (~0.3 $MVcm^{-1}$) of Si limit the performance of Si-based RF and power devices. Therefore, other materials with superior properties compared to Si are required for high efficiency power conversion. Unique features of GaN, such as wide band gap, high breakdown voltage, saturation velocity, and high polarisation properties, make it one of the most promising candidates among other options, such as SiC and diamond.

GaN and other group III-nitrides, such as AlN, InN, and their alloys, are pyroelectric materials, exhibiting spontaneous and piezoelectric polarisation. The discontinuity in polarisation at a hetero-interface between pairs of these materials results naturally in a polarisation sheet charge at this interface, which can lead to formation of two dimensional electron or hole gas (2DEG or 2DHG) of carrier density $\sim 10^{13}\ cm^{-2}$ without requiring doping or application of external bias. Because of very high density of

electrons in 2DEG that has been found to suppress scattering [1], the mobility of electrons in the 2DEG ($\sim 2000\ cm^2/Vs$) is significantly higher than in bulk GaN ($\sim 1200\ cm^2/Vs$) [2]. Heterostructure field effect transistors (HFETs) utilising 2DEG as channel have demonstrated a current gain cut-off frequency of over $300\ GHz$ [3], [4]. The wide band gap (~3.4 eV), large breakdown (2 $MVcm^{-1}$) and thermal conductivity (1.5 $W/cm\ K$) of GaN make it a suitable material for high power applications. HFETs with a power density of up to $\sim 40\ W/mm$ have been demonstrated [5].

3.2. Polarisation and Polarisation Sheet Charge

In order to understand the pyroelectric properties of wurtzite materials and their alloys, it is helpful to define relevant quantities and introduce basic concepts. In the case of a bulk homogeneous insulator placed in an electric displacement field D. The electric field $\mathcal{E}$ and induced polarisation P inside the insulator are related to the displacement field by the following relationship

$$D = \epsilon\mathcal{E} + P \tag{3.1}$$

where ϵ is the dielectric constant of the medium. D is related to the external charge density ρ by Gauss' Law as

$$\nabla . D = \rho \tag{3.2}$$

Solution of Eq. (3.2) requires a knowledge of the boundary conditions. If we consider the case of a finite solid, the boundary condition at the surface or at a heterointerface between two different materials plays an important role. In this case, Eq. (3.2) can be modified to represent a relationship between a change in the displacement vector ($\Delta D = D_2 - D_1$) normal to the surface or heterointerface and external sheet charge density σ at the surface or the heterointerface as follows

$$\Delta D = \sigma \tag{3.3}$$

It should be noted here that σ is of external origin and does not include the

polarisation charges. The discontinuity in the polarisation ΔP at the heterointerface or the surface can be defined by the polarisation sheet charge density σ_P as

$$\Delta P = -\sigma_P \tag{3.4}$$

In the absence of an external sheet charge, i.e. $\Delta D = 0$, changes in the electric field can be described from Eqs. (3.1) and (3.3) as

$$\epsilon_2 \mathcal{E}_2 - \epsilon_1 \mathcal{E}_1 = -\Delta P \tag{3.5}$$

Substituting ΔP from Eq. (3.4) into Eq. (3.5), one obtains

$$\epsilon_2 \mathcal{E}_2 - \epsilon_1 \mathcal{E}_1 = \sigma_P \tag{3.6}$$

Where ϵ_2 and ϵ_1 are dielectric constants of the two mediums at either side of the boundary. Eq. (3.6) is the desired relationship that relates the change in electric field to the polarisation sheet charge, owing to the discontinuity in the net polarisation in two mediums.

3.3. Polarisation Effects in AlN/GaN and Their Alloys

In contrast to GaAs, which crystallizes into zinc blende (cubic) phase, III-nitrides besides their equilibrium wurtzite phase, also exhibit two cubic polymorphs, a zinc-blende phase and a high-pressure rocksalt phase. Figs. 3.1 (a) and (b) show the crystal structure for zinc blende GaAs and wurtzite GaN, respectively. Only the wurtzite phase of these nitrides is pyroelectric, that is in addition to a stress dependent piezoelectric polarisation P_{pz}, these materials also contain a spontaneous polarisation P_{sp} along $[0001]$ or c-axis of a hexagonal crystal structure. Therefore, the net polarisation in wurtzite phase of GaN or AlN can be described as the sum of two polarisations, as

$$P = P_{sp} + P_{pz} \tag{3.7}$$

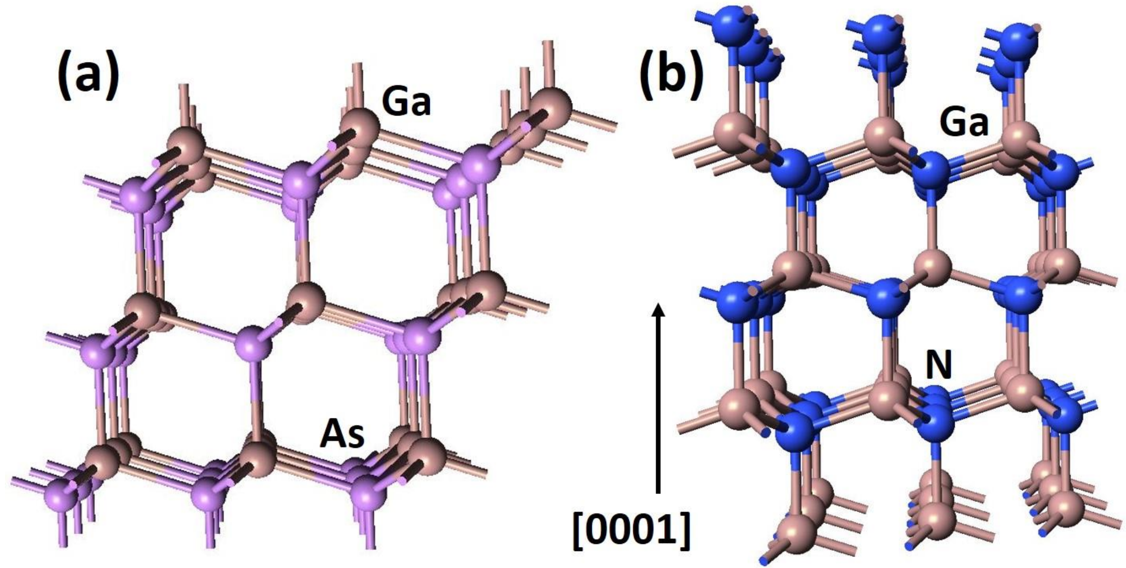

Fig. 3.1. Schematic diagrams of (a) zinc blende GaAs, and (b) wurtzite GaN crystal structures.

To determine the spontaneous polarisation for GaN and AlN, Bernardini *et al.* [1], [2] used Berry-Phase approach, where Berry-Phase refers to the phase of the quantum mechanical wave function. In Berry-Phase (or geometric phase) technique, the system is adiabatically transformed from a non-polar zinc-blende structure to the polar wurtzite structure, the polarisation charge is calculated by integrating the total current that flows during this transformation, where the current itself is calculated from the phase evolution of the wave function [6]. On the other hand, Bechstedt *et al.* [3] used Density Functional Theory with local density approximation (DFT-LDA). DFT provides a computationally efficient way to solve Schrodinger equation for a many-body system, by mapping it to a one-body system, utilising Kohn-Sham approach. In DFT electron density is used as the fundamental property unlike other methods, e.g. Hartree-Fock method, which directly aim to solve the many-body wave function but are computationally inefficient. Whereas LDA in DFT provides a way to approximate exchange-correlation potential term in Kohn-Sham equation [7]. Based upon their studies the recommended values of P_{sp} for AlN, GaN and InN along with other parameters are summarised in Table 3.1. The value

of P_{sp}, for a ternary alloy, such as $Al_xGa_{1-x}N$, obtains an intermediate value of the spontaneous polarisation of GaN and AlN. Prior to year 2000, P_{sp} of AlGaN was assumed to be a linear interpolation of P_{sp}'s of component materials, depending upon the Al mole fraction x. Later a discrepancy between the predicted and experimental values of sheet charge at the interface of $Al_{0.3}Ga_{0.7}N$/GaN structures was observed [8]. Ambacher *et al.* [9] employed a Berry phase approach based upon the density functional theory with plane-wave ultrasoft pseudopotential method in order to obtain the polarisation values of $Al_xGa_{1-x}N$ and $In_xGa_{1-x}N$ alloys to the second order in x as

$$\begin{aligned} P_{sp}^{AlGaN} &= -P_{sp}^{AlN}x - P_{sp}^{GaN}(1-x) + 0.021x(1-x)\frac{C}{m^2} \\ P_{sp}^{InGaN} &= -P_{sp}^{InN}x - P_{sp}^{GaN}(1-x) + 0.037x(1-x)\frac{C}{m^2} \end{aligned} \tag{3.8}$$

Piezoelectric polarisation is a strain dependent quantity whose direction and magnitude depend upon the nature of strain, i.e. whether it is compressive or tensile. The strain could arise from an external mechanical stress or from the lattice mismatch when a layer of one material with different lattice constant is grown on top of the base material. For example, when a layer of AlGaN with 0.26 Al mole fraction is pseudomorphically grown on relaxed GaN, it develops a biaxial tensile stress of 3GPa [8]. The piezoelectric polarisation of $Al_xGa_{1-x}N$, under a bi-axial tensile strength can be described by the following expression [10]

$$P_{pz}^{GaN} = 2\frac{a-a_0}{a_0}\left(e_{31} - e_{33}\frac{C_{13}}{C_{33}}\right) \tag{3.9}$$

where $\frac{a-a_0}{a_0}$ refers to the in-plane strain, e_{31} and e_{33} are piezoelectric coefficients, and C_{13} and C_{33} are elastic constants. Table 3.1 summarizes reported values of different parameters required for the calculations of the net polarisation for AlN, GaN and InN.

Table 3.1. Lattice Constants, spontaneous, piezoelectric polarisation and dielectric constants of AlN, GaN, and InN.

Wurtzite	AlN	GaN	InN
a_0	3.112 [h i]	3.189 [h i]	3.548 [h i]
	3.083, 3.122 [o p]	3.144, 3.207 [o p]	
c_0	4.982	5.185	5.7505
c_0/a_0	1.601	1.627	1.612
	1.619 [a]	1.634 [a]	1.627 [a]
	1.6015, 1.6041 [o p]	1.6302, 1.6297 [o p]	
u	0.380 [a]	0.376 [a]	0.377 [a]
P_{sp}	-0.081 [a i]	-0.029 [a i]	-0.032 [a i]
	-0.090 [h]	-0.034 [h]	-0.042 [h]
	-0.097, -0.090 [o p]	-0.031, -0.033 [o p]	
e_{33}	1.46 [a k]	0.73 [a k]	0.97 [a k]
	1.55 [b]	1 [c]	0.81 [h]
	1.29 [e]	0.65 [d]	0.97 [i]
	1.5 [h]	0.63 [e]	
	1.79 [i]	0.67 [h]	
		1.27 [i]	
e_{31}	-0.60 [a k]	-0.49 [a k]	-0.57 [a k]
	-0.58 [b]	-0.36 [c]	-0.41 [h]
	-0.38 [e]	-0.33 [d]	
	-0.53 [h]	-0.32 [e]	
	-0.5 [i]	-0.34 [h]	
		-0.35 [i]	
C_{13}	108 [l]	103 [l]	
	127 [h]	100 [h]	94 [h]
	120 [j]	158 [j]	92 [j]
	112, 97 [n]	98, 79 [n]	95, 78 [n]
C_{33}	373 [l i]	405 [l]	
	382 [h]	392 [h]	200 [h]
	395 [j]	398 [i]	224 [I j l]
	372, 337 [n]	267 [j]	234, 210 [n]
		403, 354 [n]	
ϵ_{11}	9.0	9.5	
ϵ_{31}	10.7	10.4	14.6

[a]Ref. [11]	[b]Ref. [12]	[c]Ref. [13]	[d]Ref. [14]
[e]Refs. [15] and [16]	[f]Ref. [17]	[g]Ref. [18]	[h]Ref. [19]
[i]Ref. [20]	[j]Ref. [21]	[k]Ref. [22]	[l]Ref. [23]
[m]Ref. [24]	[n](LDA, GGA) Ref. [25]	[o](LDA, GGA) Ref. [26]	[p](LDA, GGA) Ref. [27]

The linear interpolation of piezoelectric coefficients and elastic constants produces piezoelectric polarisation which is a non-linear function of Al-mole contents, x, and can be described as [9]

$$P_{pz}^{AlGaN/GaN} = [-0.0525x + 0.0282x(1-x)]\frac{C}{m^2} \qquad (3.10)$$

3.4. Polarisation Induced Two Dimensional Carrier Gases

When a thin film of AlGaN is grown on GaN along [0001] direction, because of a change in polarisation at the heterojunction, a positive bound sheet charge is created at the interface. Electrons begin to accumulate at the interface to compensate for the bound charge, even without any doping or application of the external voltage. Consequently, a two dimension electron gas (2DEG) forms at the interface

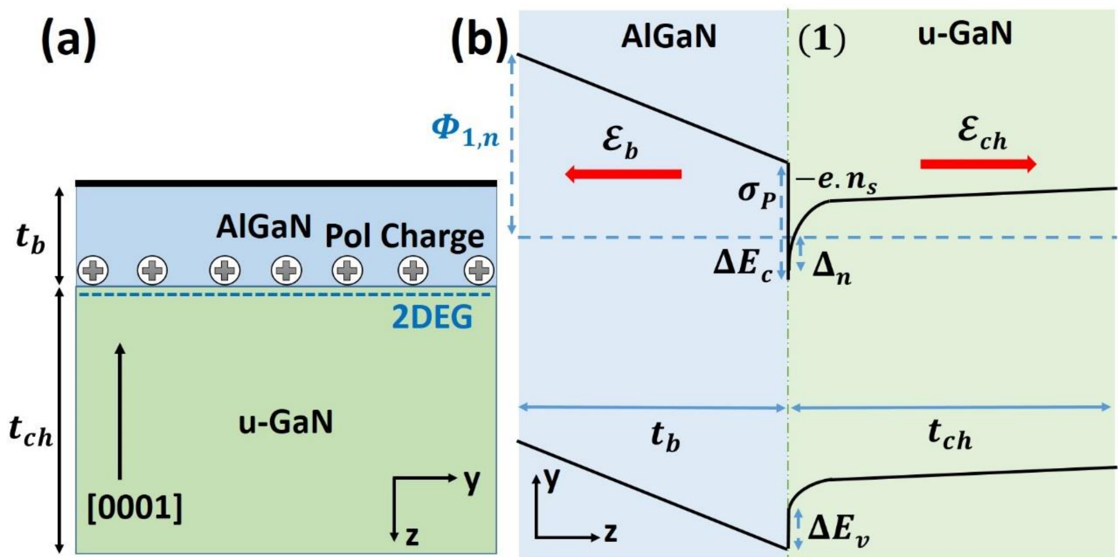

Fig. 3.2. (a) Schematic diagram of typical AlGaN/GaN heterostructures, and (b) the corresponding band diagrams, the polarisation charge density σ_P and 2DEG density n_s have been marked at the AlGaN/GaN heterointerface.

Fig. 3.2 (a) shows a typical AlGaN/GaN heterostructure, and the corresponding schematic band diagrams are shown in Fig. 3.2 (b). For sufficient thickness of the AlGaN barrier, a conduction band quantum well (QW) forms at the heterointerface. In order to predict the density of electrons in a 2DEG and determine the spatial distribution of electrons within the QW, coupled Schrodinger and Poisson equations are solved numerically, taking into account the polarisation effects [28]. For the electrons in the conduction band of GaN, an effective mass based Schrodinger in one dimension along z-direction, can be described as follows [28]–[30]

$$\begin{aligned} & -\frac{\hbar^2}{2}\frac{d}{dz}\left(\frac{1}{m(z)}\cdot\frac{d}{dz}\right)\psi_i(z) \\ & +(eV(z)+\varDelta E_C(z))\psi_i(z)=E\psi_i(z) \end{aligned} \tag{3.11}$$

where

$m(z)$ position dependent effective mass;

$V(z)$ electrostatic potential;

$\varDelta E_C(z)$ conduction band discontinuity;

$\varphi(z)$ electron wave function;

E electron energy.

The presence of polarisation effects implies that the Poisson equation has to be solved for the displacement field $D(z)$ following Eqs. (3.1) & (3.2), leading to

$$\begin{aligned} \frac{d}{dz}D(z) &= \frac{d}{dz}\left(-\epsilon(z)\frac{d}{dz}V(z)+P(z)\right) \\ &= e\cdot(p(z)-n(z)+N_D^+-N_A^-) \end{aligned} \tag{3.12}$$

where

$\epsilon(z)$ position-dependent dielectric constant;

$P(=P_{sp}+P_{pz})$ total polarisation;

$n(p)$ electron (hole) charge concentration;

$N_D^+ (N_A^-)$ ionized donor (acceptor) density.

Eqs. (3.11) and (3.12) are solved iteratively with the relevant boundary conditions, where in the first step potential $V(z)$ is obtained using Eq. (3.12) from an initial guess of the mobile charge concentration and then inserted into Eq. (3.11) to obtain the energy levels and electron wave functions of the systems. The new electron density is calculated by integrating density of states with Fermi function for each location z. The final value of electron density in 2DEG as a function of location $n_{2DEG}(z)$ can be obtained from the electron density $n_i(z)$ corresponding to a wave functions ψ_i^* for the ith quantum energy level, as

$$n_{2DEG}(z) = \sum_i n_i\,(z)\psi_i^*(z)\psi_i(z) \tag{3.13}$$

For performing self-consistent solution of Schrodinger and Poisson equations, 1D Poisson tools, developed by G. Snider [31], has been used. Fig. 3.3 (a) shows the impact of spontaneous and piezoelectric polarisation on the conduction band edge at the AlGaN/GaN heterointerface. Without any polarisation charges, the conduction band remains above the Fermi level, however, as the piezoelectric and spontaneous polarisation effects are introduced, the conduction band sinks below the Fermi level and a degenerate 2DEG forms to compensate for the positive polarisation sheet charge at the heterointerface.

Fig. 3.3 (b) shows the effect of increasing the Al mole fraction into AlGaN layer on the density of the 2DEG. Increasing the Al mole fraction raises the density of sheet charge due a larger difference between the polarisation properties of AlGaN and GaN.

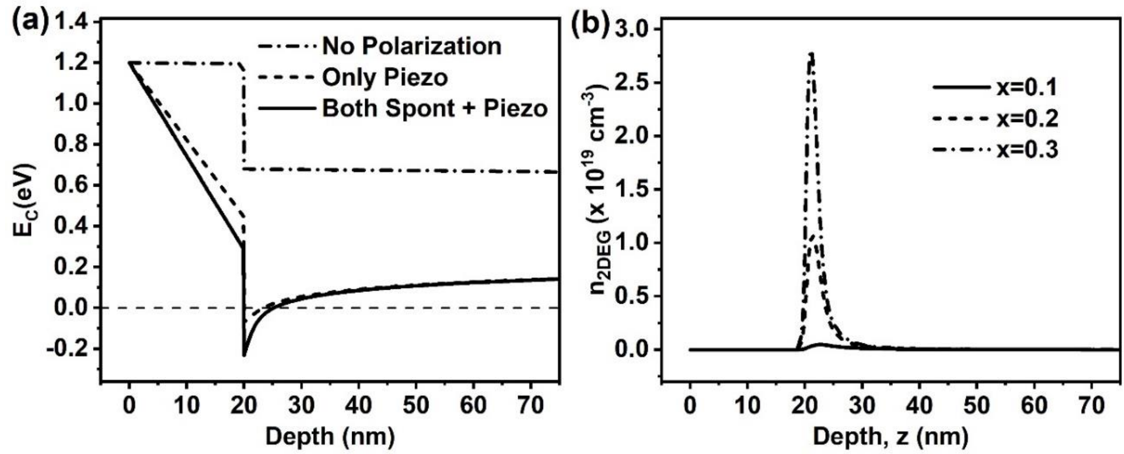

Fig. 3.3. (a) Impact of introducing polarisation effects upon the conduction band of AlGaN/GaN heterostructures. (b) Effect of increasing the Al mole concentration x upon the density of 2DEG at the heterointerface (Simulated using 1D Schrodinger Poisson tool [31]).

A similar analysis can be applied to obtain the density and shape of the 2DHG, arising as a result of negative polarisation at the GaN/AlGaN heterointerface. Yet an effective mass based Schrodinger equation is insufficient for holes because of the presence of three closely spaced valence bands, heavy-hole, light-hole, and crystal-hole, near the zone centre (Γ). A more accurate approach consists of the solution of six-band $k \cdot p$ method that considers contribution of three valence bands closest to the Fermi level, each with +1/2 and -1/2 spins [32] or 8 bands $k \cdot p$ method that also includes the contribution from the nearest conduction band [33]. The contribution of the other remote bands is included as a perturbation term in the model.

3.5. Operation of MOS in GaN Heterostructures

The oxide separated gated heterostructure in GaN is equivalent to the MOS in Si-based MOSFETs. Unlike a MOS structure in Si however, a 2DEG exists even at zero gate bias, owing to the presence of polarisation sheet charge at the interface between AlGaN and GaN. Fig. 3.4 (a) shows the schematic of a gated MOS heterostructure, where an oxide or insulator, typically Al_2O_3 or SiN, separated gate is used to modulate the density of the 2DEG and suppress the leakage current through the gate, which helps lower

the energy losses during switching. The corresponding band diagrams plotted in Fig. 3.4 (b) show that an application of gate bias V_G lowers the energy of conduction and valence bands with respect to the Fermi level in the device by eV_G.

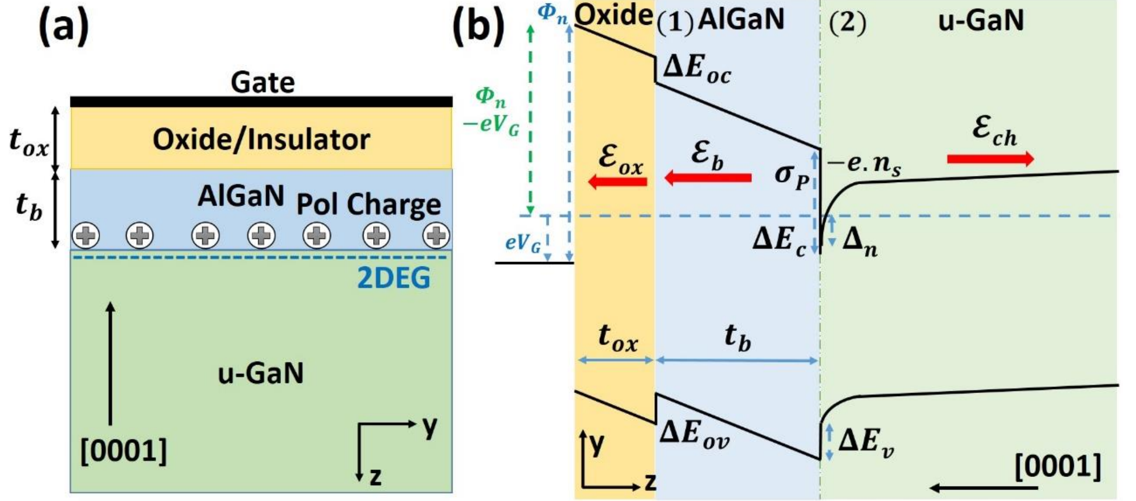

Fig. 3.4. (a) Schematic diagram of a metal-oxide semiconductor (MOS) in GaN heterostructure, and (b) the corresponding band diagrams, the polarisation charge density σ_P and 2DEG density n_s have been marked at the AlGaN/GaN heterointerface.

3.5.1. Threshold Voltage Expression and C-V Characteristics

Due to the presence of 2DEG at zero gate bias, the n-channel HFETs utilising 2DEG in a MOS exhibit normally-on or depletion mode (D-mode) behaviour. Therefore, in order to turn these devices off, negative gate bias needs to be applied, which raises the energy of the bands in Fig. 3.4 (b) such that the conduction band at AlGaN/GaN heterointerface no longer crosses the Fermi level, i.e. the height of electron quantum well Δ_n becomes zero.

To derive an expression for the threshold voltage V_{th}, V_G at $\Delta_n = 0$, we begin from the gate towards the AlGaN/GaN interface and note down the changes in the conduction band relative to the Fermi level, as

$$\phi_n - eV_G - t_{ox}\mathcal{E}_{ox} - \Delta E_{oc} - t_b\mathcal{E}_b - \Delta E_c + \Delta_n = 0 \qquad (3.14)$$

Applying Gauss' law at interfaces marked as (1) and (2) in Fig. 3.4 (b) results in

$$\varepsilon_{ox}\mathcal{E}_{ox} = \varepsilon_b\mathcal{E}_b \tag{3.15}$$

$$\varepsilon_b\mathcal{E}_b + \varepsilon_{ch}\mathcal{E}_{ch} = \sigma_P - en_s \tag{3.16}$$

Where ε_{ox}, ε_b, and ε_{ch} are the relative permittivities in the oxide, AlGaN barrier and GaN channel. To simplify the solution, we assume the thickness of the GaN channel to be large enough such that $\mathcal{E}_{ch} \approx 0$. Substituting this in Eq. (3.16) leads to

$$\varepsilon_b\mathcal{E}_b \approx \sigma_P - en_s \tag{3.17}$$

At $V_G = V_{th}$, we have $\Delta_n = 0$, which in turn indicates density of 2DEG is also zero, i.e. $en_s \approx 0$. Solving Eqs. (3.14), (3.15) & (3.17), with these substitutions yields the desired expression for V_{th}

$$V_{th} = -\frac{\sigma_P}{e}\left(\frac{1}{C_{ox}} + \frac{1}{C_b}\right) - \frac{\Delta E_{occ}}{e} + \frac{\phi_n}{e} \tag{3.18}$$

Where C_{ox} $(= \varepsilon_{ox}/t_{ox})$ and C_b $(= \varepsilon_b/t_b)$ are the unit-area capacitances in the oxide and AlGaN layers, $\Delta E_{occ}(= \Delta E_{oc} + \Delta E_c)$ is the total band-offset in the conduction band, from oxide to GaN. Eq. (3.18) indicates that V_{th} becomes smaller as the polarisation charge density σ_P introduced by AlGaN layer increases. The simulated capacitance-voltage characteristics of this heterostructure, as shown in Fig. 3.5, confirm this behaviour predicted by Eq. (3.18). The bias point at which the capacitance shows a decrease corresponds to the required threshold bias to deplete the 2DEG. As can be observed, a higher σ_P, resulting from an increase in Al mole fraction in the barrier layer x_b, reduces the voltage point at which the 2DEG is depleted.

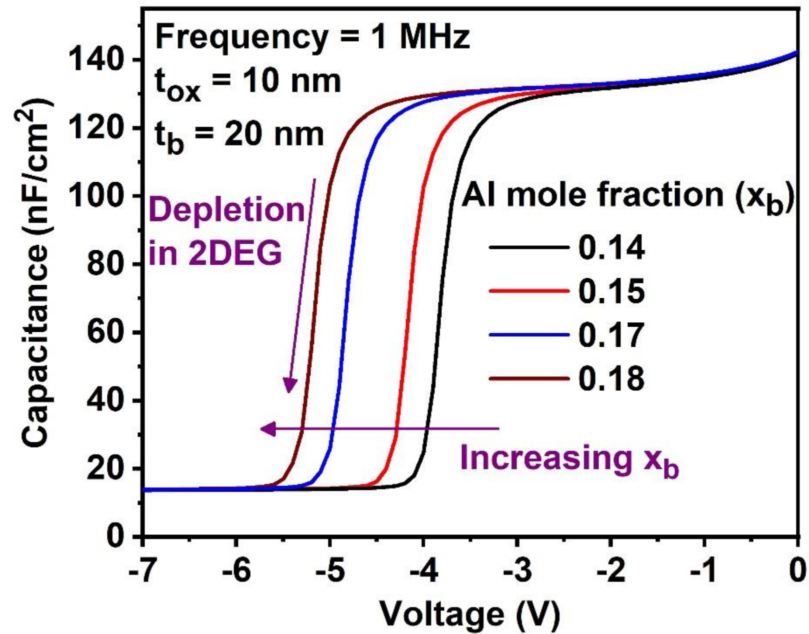

Fig. 3.5. Capacitance-voltage characteristics of the MOS heterostructure in Fig. 3.4 (a) at different Al mole fraction x_b in the barrier layer, where t_{ox} and t_b represent the thicknesses of the oxide and barrier layers (Simulated using 1D Schrodinger Poisson tool [31]).

3.6. Achieving Normally-Off Operation in n-channel MOSHFET

Polarisation properties of GaN are beneficial for obtaining a high density 2DEG without a bias, resulting in D-mode operation. However, in some power applications, such as automotives, where the devices are subjected to a substantially high electromagnetic inference (EMI) normally-off or enhancement mode (E-mode) power devices with positive threshold voltage are preferred. Moreover, a higher on-off current ratio is achieved in E-mode devices compared to their D-mode counterparts.

One of the three main techniques below are adopted to enable E-mode operation in GaN:

1) Recessed Gate – In this technique, first a recess through AlGaN barrier is created by selectively removing part of AlGaN via etching. Subsequently, an oxide layer is

grown followed by a deposition of gate metal stack, as shown in Fig. 3.6 (a). In this device either none or only a thin layer of AlGaN exists under the gate. The 2DEG under the gate remains depleted, thereby facilitating normally-off operation.

2) Ion Implantation – In this method, negative ions, for instance F^{-} ions, are implanted into the AlGaN barrier or oxide layers, as illustrated in Fig. 3.6 (b). The negative charge in the AlGaN repels the electrons along the interface of AlGaN and GaN channel, leading to the depletion of 2DEG.

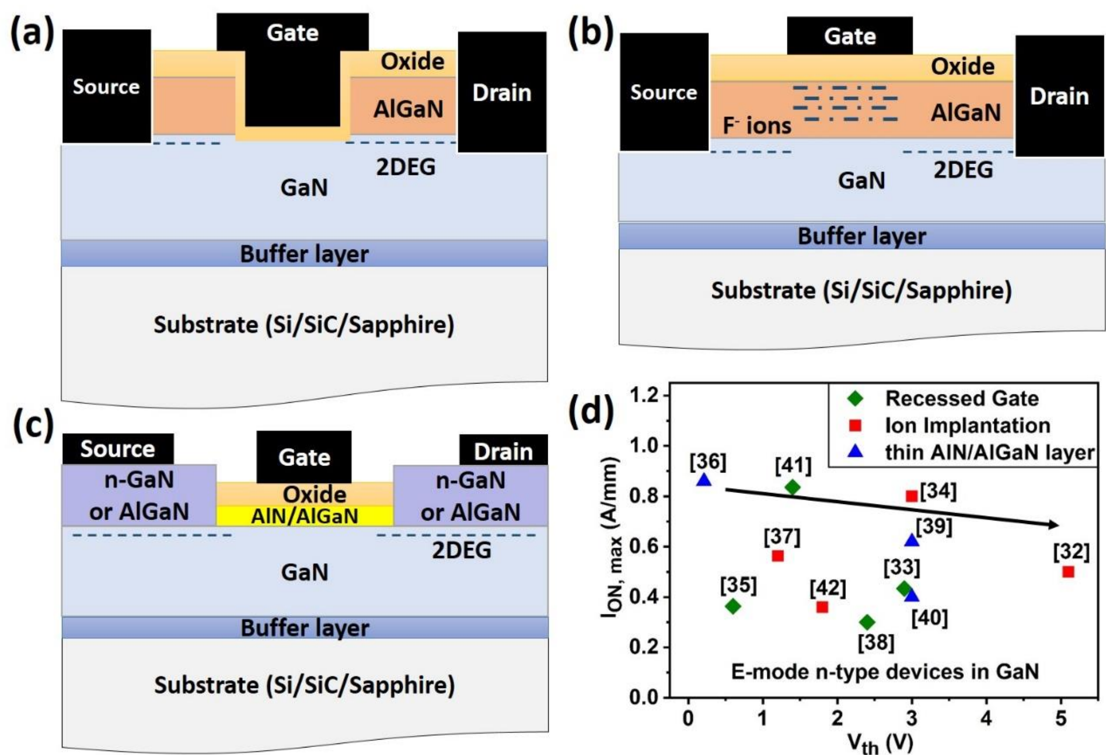

Fig. 3.6. Techniques to realise E-mode operation in n-channel MOSHFETs in GaN. (a) Recessed gate, (b) F^{-} ion or negative charge implantation, and (c) thin AlN or AlGaN cap layer ($< 5\ nm$). (d) Reported results for maximum on-current and corresponding threshold voltage for each of these techniques. [34], [35], [44], [36]–[43]

3) Thin AlN/AlGaN layer – This device geometry is shown in Fig. 3.6 (c). Here a heterostructure with a barrier layer of AlN or AlGaN of thickness $\leq 5\ nm$ is used. The small thickness of AlGaN does not provide sufficient band bending to enable the formation of e- QW along the interface of AlGaN/GaN channel, necessary for the

formation of the 2DEG. Hence, the 2DEG remains depleted. In the source and drain regions, layers of AlGaN or donor-doped GaN are regrown followed by the deposition of source and drain contact to realise ohmic contact to the GaN channel.

Fig. 3.6 (d) provides a summary of reported results for n-channel E-mode MOSHFETs in GaN, where normally-off operation is achieved using one of the techniques described above. It can be observed that the maximum drain current $I_{ON,max}$ tends to reduce as the threshold voltage V_{th} becomes larger, as indicated by the arrow. This is because a higher V_{th} requires the energy of the conduction band in the channel to be sufficiently greater than the energy of the Fermi level when the gate bias is kept zero. This however, makes it difficult for the gate bias to bring the energy of the conduction band down to form an e- QW (see Fig. 3.4 (b)).

3.7. SUMMARY

In this chapter, we have reviewed the material properties of GaN, AlN and InN and their alloys. The operation of MOS in GaN heterostructures, corresponding $C-V$ characteristics, and a derivation of threshold voltage are described. The techniques to achieve normally-off operation in n-channel MOSHFETs in GaN have also been discussed.

3.8. REFERENCE

[1] M. Shur, B. Gelmont, and M. Asif Khan, "Electron mobility in two-dimensional electron gas in AIGaN/GaN heterostructures and in bulk GaN," *J. Electron. Mater.*, vol. 25, no. 5, pp. 777–785, May 1996. DOI: 10.1007/BF02666636.

[2] U. K. Mishra, Shen Likun, T. E. Kazior, and Yi-Feng Wu, "GaN-Based RF Power Devices and Amplifiers," *Proc. IEEE*, vol. 96, no. 2, pp. 287–305, Feb. 2008. DOI: 10.1109/JPROC.2007.911060.

[3] D. S. Lee, X. Gao, S. Guo, D. Kopp, P. Fay, and T. Palacios, "300-GHz InAlN/GaN HEMTs With InGaN Back Barrier," *IEEE Electron Device Lett.*, vol. 32, no. 11, pp. 1525–1527, Nov. 2011. DOI: 10.1109/LED.2011.2164613.

[4] Y. Yue, Z. Hu, J. Guo, B. Sensale-Rodriguez, G. Li, R. Wang, F. Faria, T. Fang, B. Song,

X. Gao, S. Guo, T. Kosel, G. Snider, P. Fay, D. Jena, and H. Xing, "InAlN/AlN/GaN HEMTs With Regrown Ohmic Contacts and f_T of 370 GHz," *IEEE Electron Device Lett.*, vol. 33, no. 7, pp. 988–990, Jul. 2012. DOI: 10.1109/LED.2012.2196751.

[5] Y. -f. Wu, M. Moore, A. Saxler, T. Wisleder, and P. Parikh, "40-W/mm Double Field-plated GaN HEMTs," in *2006 64th Device Research Conference*, Jun. 2006, pp. 151–152. DOI: 10.1109/DRC.2006.305162.

[6] C. Wood and D. Jena, Eds., *Polarization Effects in Semiconductors*. Boston, MA: Springer US, 2008. DOI: 10.1007/978-0-387-68319-5.

[7] D. S. Sholl and J. A. Steckel, *Density Functional Theory*. Hoboken, NJ, USA: John Wiley & Sons, Inc., Mar. 2009. DOI: 10.1002/9780470447710.

[8] O. Ambacher, B. Foutz, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy, a. J. Sierakowski, W. J. Schaff, L. F. Eastman, R. Dimitrov, A. Mitchell, and M. Stutzmann, "Two dimensional electron gases induced by spontaneous and piezoelectric polarization in undoped and doped AlGaN/GaN heterostructures," *J. Appl. Phys.*, vol. 87, no. 1, p. 334, 2000. DOI: 10.1063/1.371866.

[9] O. Ambacher, J. Majewski, C. Miskys, A. Link, M. Hermann, M. Eickhoff, M. Stutzmann, F. Bernardini, V. Fiorentini, V. Tilak, B. Schaff, and L. F. Eastman, "Pyroelectric properties of Al(In)GaN/GaN hetero- and quantum well structures," *J. Phys. Condens. Matter*, vol. 14, no. 13, pp. 3399–3434, Apr. 2002. DOI: 10.1088/0953-8984/14/13/302.

[10] O. Ambacher, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy, W. J. Schaff, L. F. Eastman, R. Dimitrov, L. Wittmer, M. Stutzmann, W. Rieger, and J. Hilsenbeck, "Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face AlGaN/GaN heterostructures," *J. Appl. Phys.*, vol. 85, no. 6, p. 3222, 1999. DOI: 10.1063/1.369664.

[11] F. Bernardini, V. Fiorentini, and D. Vanderbilt, "Spontaneous polarization and piezoelectric constants of III-V nitrides," *Phys. Rev. B*, vol. 56, no. 16, pp. R10024–R10027, Oct. 1997. DOI: 10.1103/PHYSREVB.56.R10024.

[12] K. Tsubouchi, K. Sugai, and N. Mikoshiba, "AlN Material Constants Evaluation and SAW Properties on AlN/$Al_2O_3$and AlN/Si," in *1981 Ultrasonics Symposium*, 1981, pp. 375–380. DOI: 10.1109/ULTSYM.1981.197646.

[13] G. D. O'Clock and M. T. Duffy, "Acoustic surface wave properties of epitaxially grown aluminum nitride and gallium nitride on sapphire," *Appl. Phys. Lett.*, vol. 23, no. 2, pp. 55–56, Jul. 1973. DOI: 10.1063/1.1654804.

[14] M. A. Littlejohn, J. R. Hauser, and T. H. Glisson, "Monte Carlo calculation of the velocity-field relationship for gallium nitride," *Appl. Phys. Lett.*, vol. 26, no. 11, pp. 625–627, Jun. 1975. DOI: 10.1063/1.88002.

[15] K. Shimada, T. Sota, and K. Suzuki, "First-principles study on electronic and elastic properties of BN, AlN, and GaN," *J. Appl. Phys.*, vol. 84, no. 9, pp. 4951–4958, Nov. 1998. DOI: 10.1063/1.368739.

[16] K. Shimada, T. Sota, K. Suzuki, and H. Okumura, "First-Principles Study on Piezoelectric Constants in Strained BN, AlN, and GaN," *Jpn. J. Appl. Phys.*, vol. 37, no. Part 2, No. 12A, pp. L1421–L1423, Dec. 1998. DOI: 10.1143/JJAP.37.L1421.

[17] A. S. Barker and M. Ilegems, "Infrared Lattice Vibrations and Free-Electron Dispersion in GaN," *Phys. Rev. B*, vol. 7, no. 2, pp. 743–750, Jan. 1973. DOI: 10.1103/PHYSREVB.7.743.

[18] F. Bernardini, V. Fiorentini, and D. Vanderbilt, "Polarization-Based Calculation of the Dielectric Tensor of Polar Crystals," *Phys. Rev. Lett.*, vol. 79, no. 20, pp. 3958–3961, Nov. 1997. DOI: 10.1103/PHYSREVLETT.79.3958.

[19] J. Piprek, *Semiconductor Optoelectronic Devices: Introduction to Physics and Simulation*. Academic Press, Elsevier, 2003.

[20] I. Vurgaftman and J. R. Meyer, "Band parameters for nitrogen-containing semiconductors," *J. Appl. Phys.*, vol. 94, no. 6, p. 3675, 2003. DOI: 10.1063/1.1600519.

[21] S. L. Chuang, "Optical gain of strained wurtzite GaN quantum-well lasers," *IEEE J. Quantum Electron.*, vol. 32, no. 10, pp. 1791–1800, Oct. 1996. DOI: 10.1109/3.538786.

[22] S. L. Chuang and C. S. Chang, "A band-structure model of strained quantum-well wurtzite semiconductors," *Semicond. Sci. Technol.*, vol. 12, no. 3, pp. 252–263, Mar. 1997. DOI: 10.1088/0268-1242/12/3/004.

[23] A. F. Wright, "Elastic properties of zinc-blende and wurtzite AlN, GaN, and InN," *J. Appl. Phys.*, vol. 82, no. 6, pp. 2833–2839, Sep. 1997. DOI: 10.1063/1.366114.

[24] A. Zoroddu, F. Bernardini, P. Ruggerone, and V. Fiorentini, "First-principles prediction of structure, energetics, formation enthalpy, elastic constants, polarization, and piezoelectric constants of AlN, GaN, and InN: Comparison of local and gradient-corrected density-functional theory," *Phys. Rev. B*, vol. 64, no. 4, p. 045208, Jul. 2001. DOI: 10.1103/PHYSREVB.64.045208.

[25] S. P. Łepkowski, J. A. Majewski, and G. Jurczak, "Nonlinear elasticity in III-N compounds: Ab initio calculations," *Phys. Rev. B*, vol. 72, no. 24, p. 245201, Dec. 2005. DOI: 10.1103/PHYSREVB.72.245201.

[26] I. A. Supryadkina, K. K. Abgaryan, D. I. Bazhanov, and I. V Mutigullin, "Study of the polarizations of (Al,Ga,AlGa)N nitride compounds and the charge density of various interfaces based on them," *Semiconductors*, vol. 47, no. 12, pp. 1621–1625, Dec. 2013. DOI: 10.1134/S106378261312018X.

[27] I. Supryadkina, K. Abgaryan, D. Bazhanov, and I. Mutigullin, "Ab initio study of macroscopic polarization of AlN, GaN and AlGaN," *Phys. status solidi*, vol. 11, no. 2,

pp. 307–311, Feb. 2014. DOI: 10.1002/PSSC.201300756.

[28] F. Sacconi and A. Di Carlo, "Spontaneous and piezoelectric polarization effects on the output characteristics of AlGaN/GaN heterojunction modulation doped FETs," *Electron Devices, IEEE …*, vol. 48, no. 3, pp. 450–457, 2001.

[29] Lijun Xue, Ming Liu, Yan Wang, Yang Xia, Zhijing He, Long Ma, Lihui Zhang, Baoqin Chen, and Zhiping Yu, "Investigation on the sources of 2DEG in Al/sub x/Ga/sub 1-x/N/GaN HEMT," in *Proceedings. 7th International Conference on Solid-State and Integrated Circuits Technology, 2004.*, 2004, vol. 2, pp. 1011–1014. DOI: 10.1109/ICSICT.2004.1436677.

[30] Y. Chang, Y. Zhang, Y. Zhang, and K. Y. Tong, "A thermal model for static current characteristics of AlGaN/GaN high electron mobility transistors including self-heating effect," *J. Appl. Phys.*, vol. 99, no. 4, p. 044501, 2006. DOI: 10.1063/1.2171776.

[31] G. L. Snider, "1D Poisson." Version beta 8j1 build B08i001 http://www3.nd.edu/~gsnider. [Accessed: 10-Dec. 2018], University of Notre Dame.

[32] and R. A. A. D. J. Dugdale, S. Brand, "Direct calculation of k.p parameters for wurtzite AlN, GaN, and InN," *Phys. Rev. B*, vol. 44, no. April, pp. 0–103, 2000. DOI: 10.1063/1.2756072.

[33] S. Chuang and C. Chang, "K· P Method for Strained Wurtzite Semiconductors," *Phys. Rev. B*, vol. 54, no. 4, pp. 2491–2504, 1996. DOI: 10.1103/PHYSREVB.54.2491.

[34] C.-T. Chang, T.-H. Hsu, E. Y. Chang, Y.-C. Chen, H.-D. Trinh, and K. J. Chen, "Normally-off operation AlGaN/GaN MOS-HEMT with high threshold voltage," *Electron. Lett.*, vol. 46, no. 18, pp. 1280–1281, Sep. 2010. DOI: 10.1049/EL.2010.1939.

[35] B. Lu, O. I. Saadat, and T. Palacios, "High-Performance Integrated Dual-Gate AlGaN/GaN Enhancement-Mode Transistor," *IEEE Electron Device Lett.*, vol. 31, no. 9, pp. 990–992, Sep. 2010. DOI: 10.1109/LED.2010.2055825.

[36] M. Kanamura, T. Ohki, T. Kikkawa, K. Imanishi, T. Imada, A. Yamada, and N. Hara, "Enhancement-mode GaN MIS-HEMTs with n-GaN/i-AlN/n-GaN triple cap layer and high-κgate dielectrics," *IEEE Electron Device Lett.*, vol. 31, no. 3, pp. 189–191, 2010. DOI: 10.1109/LED.2009.2039026.

[37] H. Chiu, J. Wu, C. Yang, F. Huang, and H. Kao, "Low-Frequency Noise in Enhancement-Mode GaN MOS-HEMTs by Using Stacked $Al_2O_3/Ga_2O_3/Gd_2O_3$ Gate Dielectric," *IEEE Electron Device Lett.*, vol. 33, no. 7, pp. 958–960, Jul. 2012. DOI: 10.1109/LED.2012.2194980.

[38] T. Huang, X. Zhu, and K. M. Lau, "Enhancement-Mode AlN/GaN MOSHFETs on Si Substrate With Regrown Source/Drain by MOCVD," *IEEE Electron Device Lett.*, vol. 33, no. 8, pp. 1123–1125, Aug. 2012. DOI: 10.1109/LED.2012.2198911.

[39] J. J. Freedsman, T. Kubo, and T. Egawa, "High Drain Current Density E-Mode

Al2O3/AlGaN/GaN MOS-HEMT on Si With Enhanced Power Device Figure-of-Merit 4 x 10^8 V^2Ohm^{-1} cm^{-2}," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3079–3083, Oct. 2013. DOI: 10.1109/TED.2013.2276437.

[40] J. J. Freedsman, T. Egawa, Y. Yamaoka, Y. Yano, A. Ubukata, T. Tabuchi, and K. Matsumoto, "Normally-OFF Al_2O_3/AlGaN/GaN MOS-HEMT on 8 in. Si with Low Leakage Current and High Breakdown Voltage (825 V)," *Appl. Phys. Express*, vol. 7, no. 4, p. 041003, Apr. 2014. DOI: 10.7567/APEX.7.041003.

[41] R. Brown, A. Al-Khalidi, D. Macfarlane, S. Taking, G. Ternent, I. Thayne, and E. Wasige, "Novel high performance AlGaN/GaN based enhancement-mode metal-oxide semiconductor high electron mobility transistor," *Phys. status solidi*, vol. 11, no. 3–4, pp. 844–847, Feb. 2014. DOI: 10.1002/PSSC.201300179.

[42] M. Blaho, D. Gregušová, Š. Haščík, M. Jurkovič, M. Ťapajna, K. Fröhlich, J. Dérer, J.-F. Carlin, N. Grandjean, and J. Kuzmík, "Self-aligned normally-off metal-oxide-semiconductor n ++ GaN/InAlN/GaN high electron mobility transistors," *Phys. status solidi*, vol. 212, no. 5, pp. 1086–1090, May 2015. DOI: 10.1002/PSSA.201431588.

[43] J. Wei, S. Liu, B. Li, X. Tang, Y. Lu, C. Liu, M. Hua, Z. Zhang, G. Tang, and K. J. Chen, "Low On-Resistance Normally-Off GaN Double-Channel Metal-Oxide-Semiconductor High-Electron-Mobility Transistor," *IEEE Electron Device Lett.*, vol. 36, no. 12, pp. 1287–1290, Dec. 2015. DOI: 10.1109/LED.2015.2489228.

[44] J. W. Roberts, P. R. Chalker, K. B. Lee, P. A. Houston, S. J. Cho, I. G. Thayne, I. Guiney, D. Wallis, and C. J. Humphreys, "Control of threshold voltage in E-mode and D-mode GaN-on-Si metal-insulator-semiconductor heterostructure field effect transistors by in-situ fluorine doping of atomic layer deposition Al2O3 gate dielectrics," *Appl. Phys. Lett.*, vol. 108, no. 7, pp. 072901-1-072901-5, Feb. 2016. DOI: 10.1063/1.4942093.

Chapter 4 Modelling the Threshold Voltage for p-channel E-mode GaN HFETs

As described in chapter 3, spontaneous polarisation and piezoelectric strain along the [0001] orientation are main contributors to the high density two dimensional electron gas (2DEG) of density (>$10^{13} cm^{-2}$) at an interface of AlGaN/GaN in GaN High Electron Mobility Transistors (HEMTs). This high mobility, naturally occurring, conducting channel lends itself more easily to high performance depletion mode (D-mode) devices that find applications in high frequency and power [1]–[3], that have contributed to GaN being considered as one of the fastest growing semiconductors today [4]. Similarly, a negative polarisation charge at the GaN/AlGaN heterointerface can generate a two dimensional hole gas (2DHG), which behaves as a semiconducting field plate for effective control of electric field crowding at the gate edge of power devices [5].

The 2DHG has more recently, sparked interest towards realisation of p-channel GaN heterosturcture field effect transistors (p-HFETs). A high performance E-mode p-HFET is desirable to enable complimentary logic in III-nitrides [6], [7], for monolithic integration of power convertor system for power applications [8], [9].

Despite a low mobility of holes in wurtzite GaN, $\sim 16\ cm^2/Vs$ at room temperature [10]–[13], because of a high density 2DHG of $\sim 5 \times 10^{13}\ cm^{-2}$, p-channel HFETs with a maximum on-current $|I_{ON}|$ of $150\ mA/mm$ in depletion mode (D-mode) were demonstrated by Li *et al.* in [6]. Nevertheless, it is precisely this high density that makes it difficult to deplete, and results in an on-off current ratio of ~ 1 order in magnitude. For realising an enhancement mode (E-mode) p-channel HFET with a high $|V_{th}|$, a low density of the 2DHG of $\sim 6 \times 10^{11}\ cm^{-2}$ led to degradation in the on-current by two orders of magnitude [14]. The maximum on-current of an enhancement-mode (E-mode)

p-channel HFETs reported experimentally to date, lies in the range of $0.3 - 9\ mA/mm$ [6], [9], [14], [15], with a maximum reported $|V_{th}|$ of $|-2.5|\ V$ [6], as shown in Fig. 4.1. Akin to the I_{ON} vs. V_{th} behaviour in normally-off n-channel MOSHFET, described in Fig. 3.6 (d) of chapter 3, $|I_{ON}|$ in p-channel MOSHFET also shows degradation, as the device behaviour is shifted towards E-mode with large $|V_{th}|$. One of the widely understood reasons for this behaviour is that conditions for increased polarisation charge, required to increase $|I_{ON}|$, leads to difficulty in depleting the charge in E-mode, to give low $|I_{OFF}|$, hence leading to poor I_{ON}/I_{OFF} and a low $|V_{th}|$. Nevertheless, an E-mode p-channel HFET with a $|V_{th}|$ of $|-1|\ V$ to $|-2|\ V$ and low off-current $|I_{OFF}|$ is desirable to reduce static power consumption, simplify the circuit complexity, and enable fail-safe operation [16].

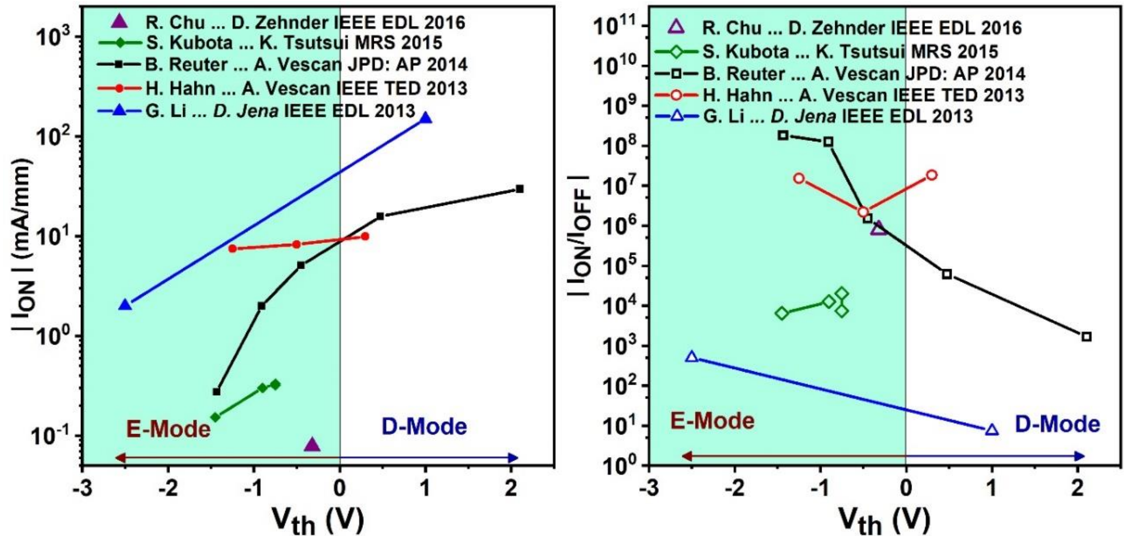

Fig. 4.1. The electrical characteristics of the state-of-the-art normally-off p-channel HFETs reported to date.

The current work consolidates our understanding of the mechanisms of achieving effective high $|V_{th}|$ in p-channel HFETs in GaN on a polarisation superjunction platform that is fully compatible with power device fabrication [5]. An analytical expression for the $|V_{th}|$ in terms of material parameters and geometry is demonstrated for two potential

candidate structures for p-channel E-mode operation, described as (i) a conventional heterostructure without an AlGaN cap and (ii) an alternate heterostructure with an AlGaN cap, that has been shown to provide additional flexibility for addressing the trade-off between the $|V_{th}|$ and on-current by us in [17]. The expressions proposed in this work may be easily used in back-of-envelope calculations to design the V_{th} by adjusting the Al mole fraction in the AlGaN cap layer. Subsequently, it is demonstrated that in GaN, achieving a low negative threshold voltage, i.e. high $|V_{th}|$ requires a reduction of the thickness of oxide and GaN channel layers (contrary to well-known behaviour of MOSFETs in silicon), which can lead to a significant gate leakage and degradation in the reliability. Furthermore, we present an analysis of an alternate heterostructure to facilitate normally-off operation in p-channel MOSHFETs in GaN. This structure incorporates an AlGaN cap layer beneath the gate to deplete the 2DHG underneath the gate. This concept was first introduced by F. J Kub *et al.* [18]. For the first time, we demonstrate that the device incorporating an AlGaN cap presents the possibility to "break" the trade-off between $|I_{ON}|$, $|V_{th}|$, and I_{ON}/I_{OFF} in E-mode p-channel MOSHFETs, that exists even in this modified structure. An analytic model of the V_{th} in terms of thickness of oxide and channel layers (t_{ox} & t_{ch}), and polarisation charge σ_P that gives a rule of thumb prediction of the V_{th} is presented.

4.1. SIMULATION MODEL AND HETEROSTRUCTURES

The two devices based upon conventional and alternate heterostructures (HS1 and HS2), examined in this work, are shown in Figs. 4.2 (a) and (b), respectively. Both the devices from bottom to the top, consist of a GaN buffer, AlGaN barrier, and GaN channel layers along the [0001] direction with the GaN buffer in a relaxed state. Due to the lattice mismatch between AlGaN and GaN, a strain is developed within AlGaN barrier layer, during its pseudomorphic growth upon the buffer. The lattice constant a_0 for AlGaN,

with an Al mole fraction x is estimated by linearly interpolating between the lattice constants for GaN and AlN, which are typically 3.189 Å and 3.112 Å [19]. Thus the strain in AlGaN can be described as $(a_{0,AlGaN} - a_{0,GaN})/a_{0,GaN} \approx 2.4x$ %.

Since AlGaN is lattice matched to the GaN buffer, the GaN channel layer above the AlGaN remains relaxed. Owing to strain induced piezoelectric polarisation and the difference in spontaneous polarisation, a polarisation sheet charge density σ_b is created at the bottom and top interfaces of AlGaN barrier. In the alternate heterostructure an additional strain is developed within the AlGaN cap on top of the relaxed GaN channel, which depends upon the Al mole fraction in the cap layer. As a result of the polarisation difference between the AlGaN cap and channel layer, an additional polarisation sheet charge density σ_{cap} is created along the cap/channel interface in Fig. 4.2 (b). By adjusting the Al mole fraction in the cap layer, σ_{cap} can be modified, providing an additional handle in either controlling or depleting the 2DHG in the GaN channel under the gate.

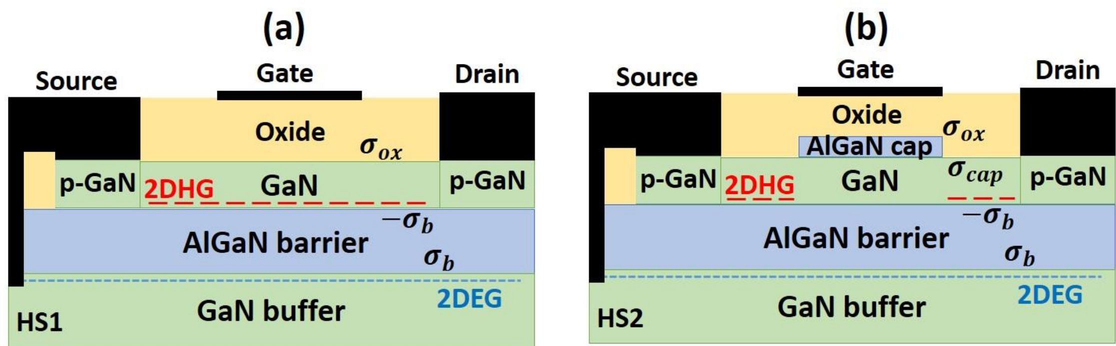

Fig. 4.2. p-channel GaN MOSHFETs on (a) conventional heterostructure (HS1) and (b) alternate heterostructure (HS2).

The approach of utilising an AlGaN cap layer is similar to the one introduced in [18] for achieving normally-off p-channel GaN HFET, where the polarisation charge introduced by AlGaN cap layer counterbalances the polarisation introduced by AlGaN barrier. As opposed to the devices presented in [18], the source contact in our devices is split into a top contact to the p-GaN and a bottom contact to the underlying 2DEG. This

ensures that the underlying 2DEG always remains grounded with source, since non-saturating $I_{DS} - V_{DS}$ charactersitics were observed in the device with conventional heterostructure when the 2DEG was left floating, as reported by Nakajima *et al.* [20], and shown here in the reproduced Fig. 4.3. Therefore the mechanism of depleting the 2DHG and electrostatics with respect to the potential value of the underlying 2DEG in these devices are expected to differ substantially as will be demonstrated in the subsequent chapter.

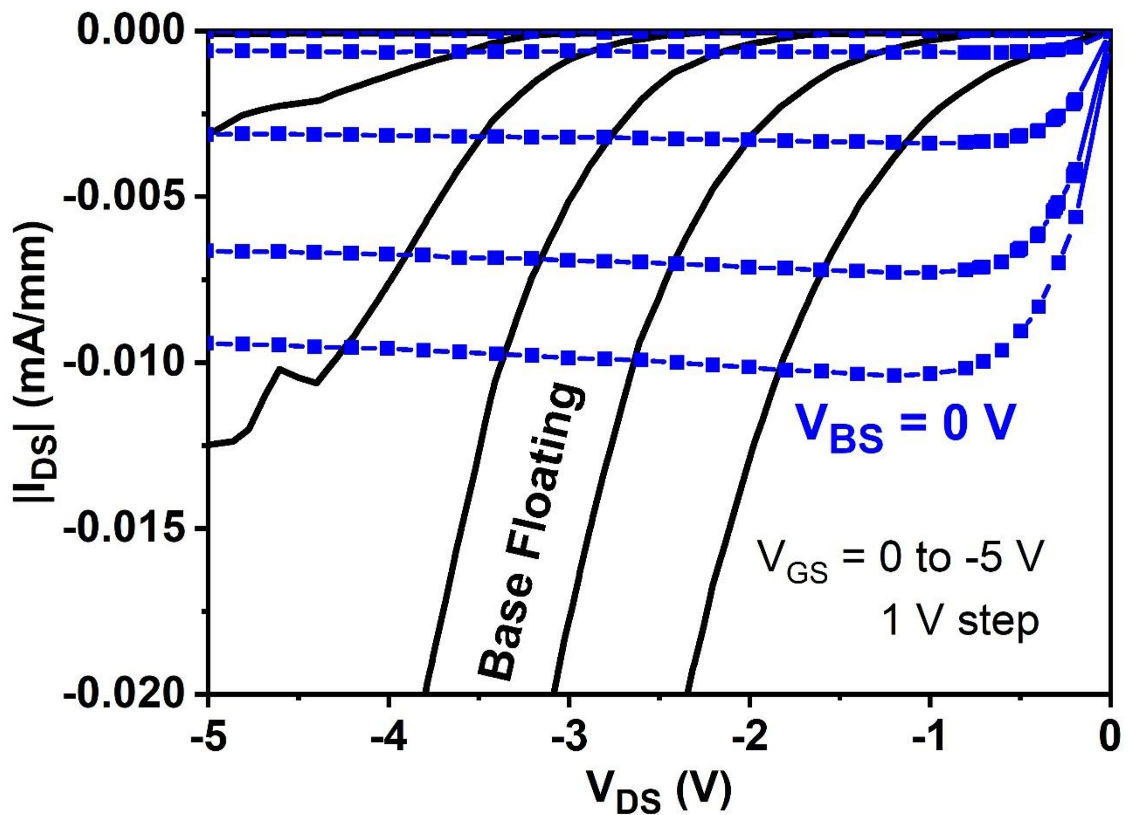

Fig. 4.3. Reported measurement of $I_{DS} - V_{DS}$ characterstics for different V_{GS}, for fabricated p-channel MOSHFET in conventional heterostructure, where dashed lines for the device with floating 2DEG, while the plots in blue curves and squares represent the case where 2DEG is kept grounded (Reproduced Fig. 7 (a) with the permission from [20] Copyright (2018) by the Institution of Engineering and Technology (IET)).

The two devices are simulated using Silvaco TCAD [21], where Poisson equation is self-consistently solved with carrier continuity equation. Shockley-Read-Hall and Augur recombination are employed to model trap kinetics. The low field mobility is described

by the Albrecht model [22], whereas a nitride specific field dependent model is used under high field [23]. The maximum hole mobility at room temperature is limited to $16\ cm^2/Vs$ [10]. At the interface of oxide with GaN or AlGaN, the charge and trap densities of $2.8 \times 10^{12} cm^{-2}$ and $2 \times 10^{12} cm^{-2}$, respectively, are considered.

Owing to a difficulty in achieving a good ohmic contact to p-GaN, the reported results of resistivity of contacts to p-GaN, differ by 4 orders of magnitude for different metals, alloys and metal stacks, as presented in Fig. 4.4. Moreover, due to the progress in GaN based optoelectronics devices, ohmic p-GaN contacts with good thermal stability and optical properties such as high transparency or reflectivity are also desired. As indicated in this figure, these contacts are categorised into three different classes, metallic, transparent, and reflective, which are suitable for electronics, solar or LED applications, respectively.

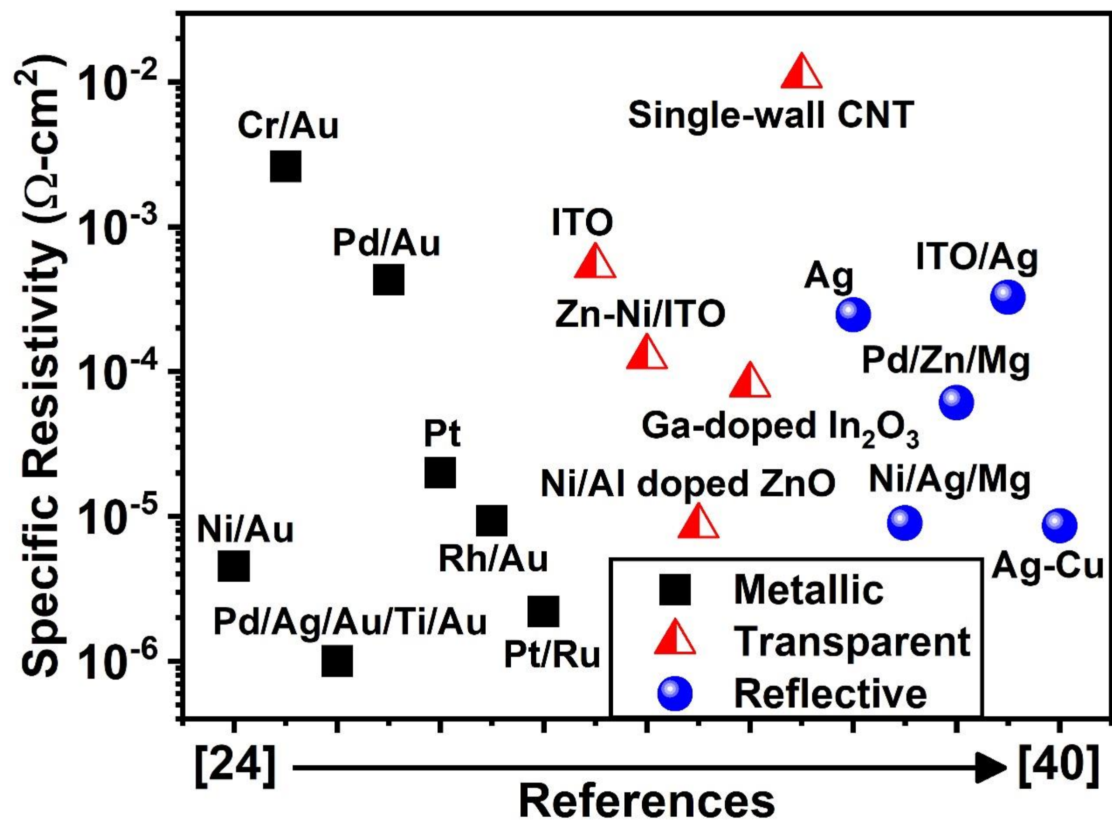

Fig. 4.4. The reported results for specific contact resistivity for different kinds of ohmic contacts to p-GaN. [24]–[40]

Without additional requirements of transparency or reflectivity, metallic contacts, in general achieve lowest specific resistivity, with an average value $\sim 10^{-5} \Omega\, cm^2$. To the best of our knoweldge, the lowest ohmic p-GaN contact of $\sim 10^{-6} \Omega\, cm^2$ is reported for Pd/Ag/Au/Ti/Au metal stack annealed at $800\ °C$ in N_2 [33], where it was suggested that after the annealing Au and Ag formed an alloy that reacted with the surface of p-GaN to form a p+ region at the interface. Since the average contact resistivity of p-GaN contacts is reported to be $\sim 10^{-4}\ \Omega\, cm^2$[41], this value of contact resistivity is used for both source and drain contacts to p-GaN in our simulations. A comparison of our simulation model with experimental results reported in [42] for the device with conventional heterostructure is presented in Fig. 4.5, showing a good agreement.

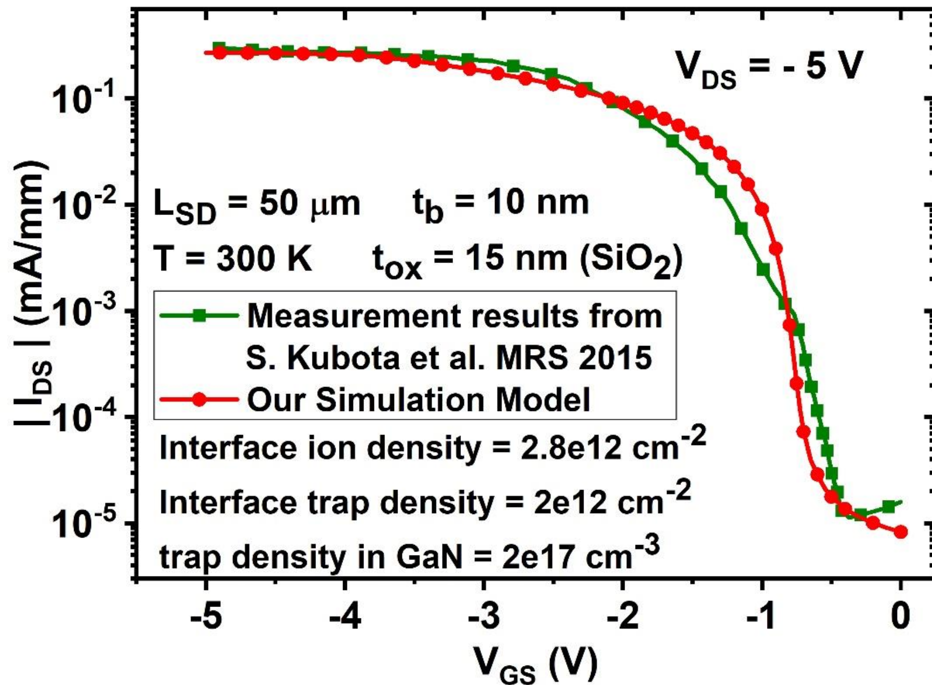

Fig. 4.5. Verification of our simulation model for conventional heterostructure with the $I_{DS} - V_{GS}$ experiment data reported in [42] (reused with the permission from the author of [42]).

The heterostructure stacks for the two devices under the gated regions and the corresponding schematic band diagrams based on simulations are displayed in Figs. 4.6 (a) – (d), which emphasize the distinct features, such as conduction and valence band

offsets at the interfaces of oxide/GaN and AlGaN/GaN heterointerfaces, and the electron and hole quantum wells.

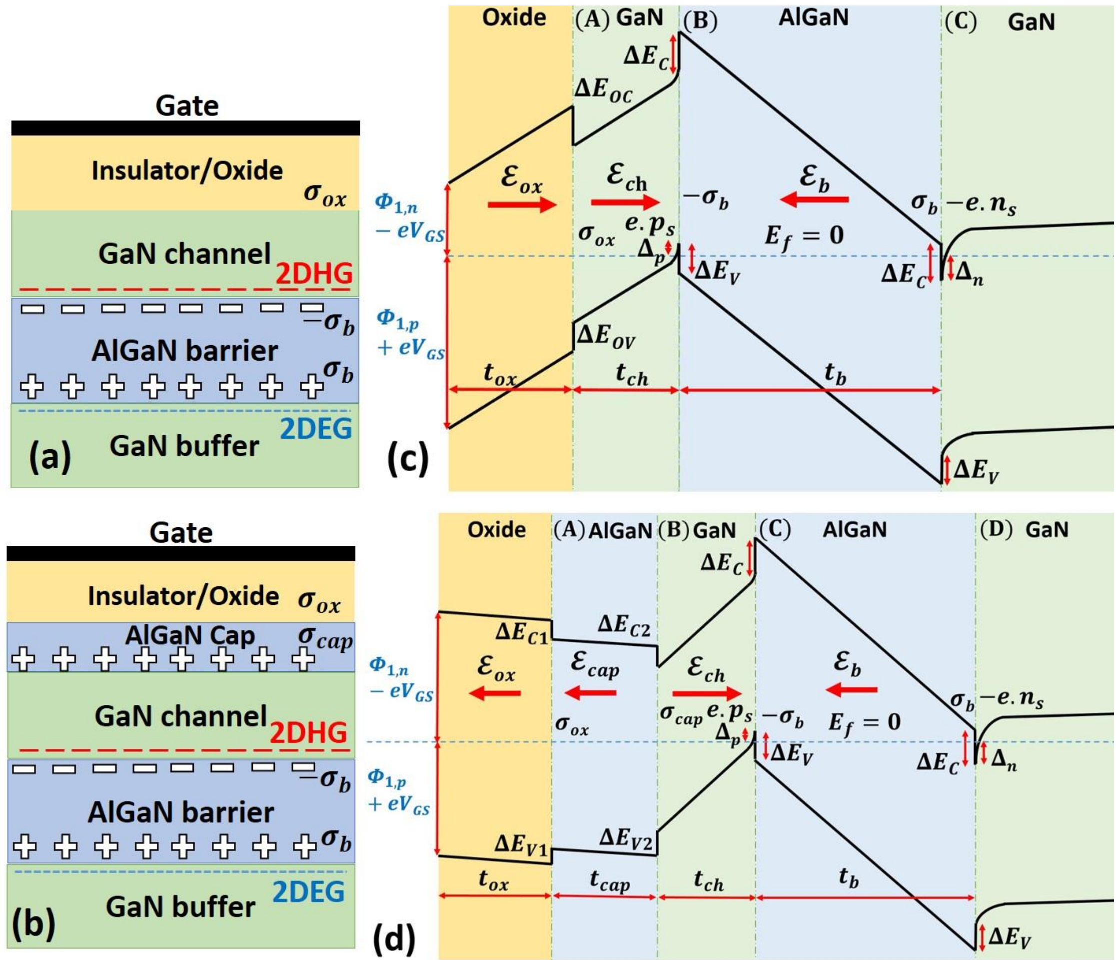

Fig. 4.6. Schematic cross-sections beneath the gate of the conventional and alternate heterostructures (without and with AlGaN cap respectively) and corresponding band diagrams. (a) Conventional heterostructure from top to bottom consisting of oxide/insulator, undoped GaN channel, AlGaN barrier, and GaN buffer layers, (b) Alternate heterostructure from top to bottom consisting of oxide/insulator, AlGaN cap layer, undoped GaN channel, AlGaN barrier, and GaN buffer layers, (c) Energy band diagrams of the conventional heterostructure, (d) Energy band diagrams of the alternate heterostructure

In deriving an expression for V_{th}, a procedure similar to that employed by H. Hahn *et al.* in [43] is adopted. In this approach, first the charge densities at various interfaces are evaluated by the application of Gauss' Law under the electrostatic constraints introduced by the heterostructure. Threshold voltage is defined as the gate bias at which

the electron or hole density for a n-channel or p-channel device, respectively, becomes zero. Moreover, the thicknesses of GaN channel and AlGaN cap layers are kept sufficiently small to prevent formation of any undesirable electron or hole quantum wells at any of the interfaces between the oxide, GaN channel, and the AlGaN cap layers in the initial results presented in this chapter.

4.2. DERIVATION OF THRESHOLD VOLTAGE EXPRESSION

4.2.1. Conventional Heterostructure

Following the valence band in Fig. 4.6 (c) and moving from the gated surface of the oxide on the left to the interface of the GaN channel/AlGaN barrier, marked as (B), on the right, the energy relative to the Fermi level E_f can be written as

$$-\frac{\Phi_{1,p}}{e} - V_{GS} + t_{ox}\mathcal{E}_{ox} + \frac{\Delta E_{OV}}{e} + t_{ch}\mathcal{E}_{ch} = \frac{\Delta_p}{e} \quad (4.1)$$

where $\Phi_{1,p}$ is the barrier height of the valence band at the gate/oxide interface, ΔE_{OV} is the valence band offset between the oxide and GaN channel, t_{ox} and t_{ch} are thicknesses of the oxide and GaN channel respectively, $\mathcal{E}_{ox}$ and $\mathcal{E}_{ch}$ represent the electric field within the oxide and GaN channel layers, respectively, and Δ_p is the height of the hole quantum well (QW). Applying Gauss' law at interfaces (A) and (B), respectively, leads to

$$\epsilon_{ch}\mathcal{E}_{ch} - \epsilon_{ox}\mathcal{E}_{ox} = \sigma_{ox} \quad (4.2)$$

$$\epsilon_{ch}\mathcal{E}_{ch} + \epsilon_b\mathcal{E}_b = \sigma_b - e \cdot p_s \quad (4.3)$$

where ϵ_{ox}, ϵ_{ch}, and ϵ_b are the permittivities of oxide, GaN channel, and AlGaN barrier layers, $\mathcal{E}_b$ is the electric field within the barrier layer, σ_{ox} is the unpassivated sheet charge or net sheet charge density along the oxide and channel interface, σ_b is the net polarisation sheet charge density between the GaN channel and AlGaN barriers at interface (B), and p_s represents the density of 2DHG. It can be inferred from Fig. 4.6 (c), that for both hole and electron quantum wells (QWs) (Δ_n & Δ_p) to simultaneously exist,

the electric field within the AlGaN barrier must be large enough to provide a band bending equivalent to the energy of the bandgap of GaN (E_G^{GaN}) over the thickness of the barrier t_b, which can be expressed as

$$t_b \mathcal{E}_b \approx \frac{E_G^{GaN}}{\mathrm{e}} \tag{4.4}$$

In order to eliminate the explicit electric field dependence in Eqs. (4.2) and (4.3), first $\mathcal{E}_b$ is substituted from Eq. (4.4) into Eq. (4.3)

$$\epsilon_{ch}\mathcal{E}_{ch} = \sigma_b - e \cdot p_s - C_b \frac{E_G^{GaN}}{e} \tag{4.5}$$

where $C_b = \epsilon_b / t_b$ is the unit area capacitance associated with the barrier layer. Rewriting Eq. (4.2) by substituting $\epsilon_{ch}\mathcal{E}_{ch}$ from Eq. (4.5) gives

$$\epsilon_{ox}\mathcal{E}_{ox} = \sigma_b - \sigma_{ox} - e \cdot p_s - C_b \frac{E_G^{GaN}}{e} \tag{4.6}$$

Finally, the dependence of the electric field in Eq. (4.1) can be eliminated by substituting $\mathcal{E}_{ch}$ from Eq. (4.5) and $\mathcal{E}_{ox}$ from Eq. (4.6), which results in

$$V_{GS} = \left(\sigma_b - e \cdot p_s - C_b \frac{E_G^{GaN}}{e}\right)\left(\frac{1}{C_{ox}} + \frac{1}{C_{ch}}\right) - \frac{\sigma_{ox}}{C_{ox}} - \frac{\Phi_{1,p}}{e} + \frac{\Delta E_{OV}}{e} - \frac{\Delta_p}{e} \tag{4.7}$$

Where $C_{ox}(= \epsilon_{ox}/t_{ox})$ and $C_{ch}(= \epsilon_{ch}/t_{ch})$ are the unit area capacitances in the oxide and channel layers. Defining $C_{oc} = (1/C_{ox} + 1/C_{ch})^{-1}$ as the equivalent unit area capacitance offered by the oxide and channel layers, and following the definition of threshold voltage as the gate bias at which the height of the hole QW Δ_p must be zero and $e \cdot p_s$ should be negligibly small compared to σ_b [43], Eq. (4.7) can be expressed as

$$V_{th} = \frac{\sigma_b}{C_{oc}} - \frac{C_b}{C_{oc}}\frac{E_G^{GaN}}{e} - \frac{\sigma_{ox}}{C_{ox}} - \frac{\Phi_{1,p}}{e} + \frac{\Delta E_{OV}}{e} \tag{4.8}$$

From Eq. (4.8), it can be inferred that a higher polarisation charge at the GaN channel and AlGaN barrier heterointerface drives the threshold voltage upwards, i.e. into a D-mode regime. Moreover, an increase in barrier thickness (i.e. reduction of C_b) means a

relatively smaller band bending across the barrier required for the formation of both electron and hole quantum wells simultaneously, driving the device towards a D-mode regime. A detailed description of the impact of the other parameters is presented in the subsequent section.

4.2.2. Alternate Heterostructure with an AlGaN Cap

A similar procedure can be followed to obtain an expression of the V_{th} in the heterostructure with the AlGaN cap layer (Fig. 4.6 (b)). Here we present only the key steps while highlighting important differences. Considering the band diagram in Fig. 4.6 (d), the variations of energy of the valence band, as before, can be represented as

$$-\frac{\Phi_{1,p}}{e} - V_{GS} - t_{ox}\mathcal{E}_{ox} + \frac{\Delta E_{V1}}{e} - t_{cap}\mathcal{E}_{cap} + \frac{\Delta E_{V2}}{e} + t_{ch}\mathcal{E}_{ch} = \frac{\Delta_p}{e} \quad (4.9)$$

Where t_{cap} is the thickness of the AlGaN cap layer, $\mathcal{E}_{cap}$ is the electric field within this layer, ΔE_{V1} and ΔE_{V2} are valence band offsets at the interfaces of oxide/cap and cap/channel, respectively, $\Delta E_{V1} + \Delta E_{V2} = \Delta E_{OV}$, the net valence band offset between the oxide and GaN channel, as in the conventional structure. Moreover, as opposed to Eq. (4.1), the term $t_{ox}\mathcal{E}_{ox}$ in Eq. (4.9) bears a negative sign. This is owing to the fact that in this heterostructure, there is an additional polarisation sheet charge density σ_{cap}, introduced by the AlGaN cap layer, which is responsible for a change in the direction of electric field in the oxide layer [17]. An application of Gauss' law at the interfaces (A), (B), and (C) gives

$$\epsilon_{ox}\mathcal{E}_{ox} - \epsilon_{cap}\mathcal{E}_{cap} = \sigma_{ox} \quad (4.10)$$

$$\epsilon_{cap}\mathcal{E}_{cap} + \epsilon_{ch}\mathcal{E}_{ch} = \sigma_{cap} \quad (4.11)$$

$$\epsilon_{ch}\mathcal{E}_{ch} + \epsilon_{b}\mathcal{E}_{b} = \sigma_{b} - e \cdot p_s \quad (4.12)$$

Where ϵ_{cap} is the dielectric constant of the AlGaN cap layer. Equation (4.4) is still applicable in the barrier layer, as long as the band bending is sufficient to form both

electron and hole QWs simultaneously. Employing Eqs. (4.4) and (4.10)-(4.12) to remove the electric field dependence in Eq. (4.9), leads to

$$V_{GS} = \left(\sigma_b - e \cdot p_s - C_b \frac{E_G^{GaN}}{e}\right)\left(\frac{1}{C_{ox}} + \frac{1}{C_{cap}} + \frac{1}{C_{ch}}\right) - \sigma_{cap}\left(\frac{1}{C_{ox}} + \frac{1}{C_{cap}}\right) - \frac{\sigma_{ox}}{C_{ox}} - \frac{\Phi_{1,p}}{e} + \frac{\Delta E_{OV}}{e} - \frac{\Delta_p}{e} \tag{4.13}$$

Where $C_{cap}(= \epsilon_{cap}/t_{cap})$ is the unit area capacitance offered by the AlGaN cap layer. Defining $C_{occ} = \left(1/C_{ox} + 1/C_{cap} + 1/C_{ch}\right)^{-1}$, $C_{ocp} = \left(1/C_{ox} + 1/C_{cap}\right)^{-1}$, and at $V_{GS} = V_{th}$ substituting, Δ_p as zero as well as assuming $e \cdot p_s$ to be negligible in comparison with σ_b, Eq. (4.13) reduces to the desired expression as

$$V_{th} = \frac{\sigma_b}{C_{occ}} - \frac{C_b}{C_{occ}} \frac{E_G^{GaN}}{e} - \frac{\sigma_{cap}}{C_{ocp}} - \frac{\sigma_{ox}}{C_{ox}} - \frac{\Phi_{1,p}}{e} + \frac{\Delta E_{OV}}{e} \tag{4.14}$$

Eq. (4.14) is similar to Eq. (4.8) except for the additional term $-\sigma_{cap}/C_{ocp}$ which results from the additional polarisation sheet charge introduced by the AlGaN cap layer that helps bring V_{th} down to the desired negative levels for an E-mode p-channel device. In order to compare the predicted threshold voltage from Eqs. (4.8) and (4.14) with simulated results, all the parameters in the equations are kept same as mentioned in the user manual of the TCAD [44]. These parameters along with the polarisation charge model are summarised in Table 4.1.

Table 4.1. Parameters used in the calculation of the threshold voltage from Eqs. (4.8) and (4.14) for the two heterostructures examined in this work.

Parameters	Values
$\Phi_{1,p}$ (eV)	4.9
ΔE_{OV} (eV)	2.15
E_G^{GaN} (eV)	3.43
ϵ_{ox} (Al_2O_3)	$9.3\epsilon_0$
ϵ_{ch}	$8.9\epsilon_0$
ϵ_b or ϵ_{cap} $(Al_xGa_{1-x}N)$	$8.5x\epsilon_0 + 8.9(1-x)\epsilon_0$
σ_{ox} $(oxide/GaN)$	$0.1\sigma_b$
σ_{ox} $(oxide/AlGaN)$	$0.1\sigma_{cap}$
σ_b or $\sigma_{cap} = \lvert\Delta P_{sp}\rvert + \lvert\Delta P_{pz}\rvert$	
P_{sp} (GaN) (C/m^2)	-0.034
P_{sp} $(Al_xGa_{1-x}N)$ (C/m^2)	$-0.09x - 0.034(1-x)$
P_{pz} $(Al_xGa_{1-x}N) = 2\frac{a(x)-a_0}{a_0}\left(e_{31} - \frac{C_{13}}{C_{33}}e_{33}\right)$	
a_0 (Å) (GaN)	3.189
a $(Al_xGa_{1-x}N)$ (Å)	$3.112x + 3.189(1-x)$
e_{33} $(Al_xGa_{1-x}N)$ (C/m^2)	$1.5x + 0.67(1-x)$
e_{31} $(Al_xGa_{1-x}N)$ (C/m^2)	$-0.53x - 0.34(1-x)$
C_{13} $(Al_xGa_{1-x}N)$ (GPa)	$127x + 100(1-x)$
C_{33} $(Al_xGa_{1-x}N)$ (GPa)	$382x + 392(1-x)$

4.3. Analysis of the Conventional Heterostructure p-Channel MOSHFET

A common approach to improve $|I_{ON}|$ in the conventional heterostructure in Fig. 4.5 (a) is to increase the Al mole fraction within the barrier layer x_b. Fig. 4.7 (a) compares the transfer characteristics of the device at different x_b. An increase in x_b, results in an increase in polarisation charge at both the top and bottom AlGaN interfaces, allowing a higher band bending across the AlGaN barrier, as shown in Fig. 4.7 (b). As a result, the energy of the valence band at the top GaN/AlGaN interface rises, thus facilitating the formation of the hole quantum well, which results in low $|V_{th}|$ and high off-current $|I_{OFF}|$ (defined as the absolute drain to source current at $V_{DS} = -5\ V$ and $V_{GS} = 0$). As shown in shown in Fig. 4.7 (c), a fourfold increase in $|I_{ON}|$ (defined as the absolute drain to source current at $-5\ V$ of V_{GS} and V_{DS}) is observed at higher x_b, owing to a higher density

of the 2DHG, shown in Fig. 4.7 (d).

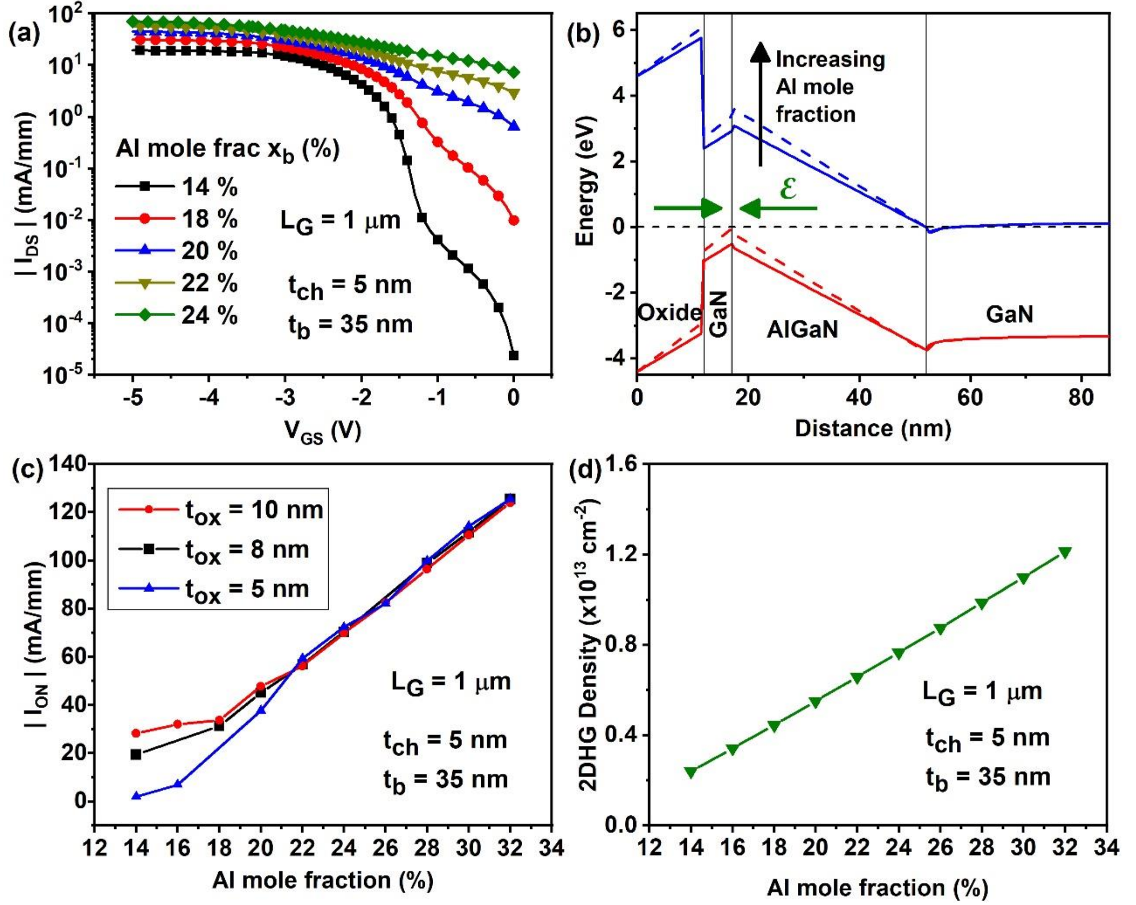

Fig. 4.7. (a) Comparison of simulated transfer characteristics of conventional heterostructure at different Al mole fraction in the barrier layer x_b, (b) Change in the energy band diagram in conventional heterostructure beneath the gate with x_b, (c) on-current $|I_{ON}|$ vs. x_b at different oxide (Al_2O_3) thicknesses t_{ox}, (d) the density of 2DHG vs. x_b for conventional heterostructure.

An increase in $|V_{th}|$ can be achieved by recessing the GaN layer [15]. In Fig. 4.8, we examine the dependence of $|V_{th}|$ upon t_{ox} and t_{ch}. From the simulated transfer characteristics, V_{th} is extracted by drawing a tangent to the drain current corresponding to a maximum transconductance g_{max} in the transfer characteristics on a linear scale and checking its intercept at the axis of the gate bias (g_{max} method). A decrease in t_{ox} leads to an improvement in both the I_{ON}/I_{OFF} and $|V_{th}|$, as shown Fig. 4.8 (a). This is because a smaller t_{ox} lowers the valence band energy relative to the Fermi level at the GaN channel/AlGaN barrier interface, as shown in Fig. 4.8 (b). Therefore, a higher $|V_{GS}|$ is

now required to increase the valence band energy level for the formation of the 2DHG at this interface. For the simulation of the electrical properties in Silvaco TCAD, the entire device structure is divided into non-uniform meshes, as shown in Fig. 4.8 (c), where the mesh spacing is selected such that the changes in the drain current become nominal for a further reduction in mesh spacing. This is confirmed in Fig. 4.8 (d), which shows the drain current behaviour as the mesh spacing is scaled by various scaling factors. As observed, for a further reduction in the mesh spacing via a scaling factor of less than unity the variation in drain current remains small ($\sim 1\ mA/mm$). However, as the mesh spacing is increased with a scaling factor of greater than 1, the maximum value of I_{DS} drops significantly, thus justifying the employed mesh spacing.

Since the electric field in both oxide and channel layers is pointed along the same direction, as marked by the green arrow, pointing from left to right in Fig. 4.8 (b), a reduction in t_{ch} also produces an increase in $|V_{th}|$, identical to t_{ox}, as shown in Fig. 4.8 (e). Fig. 4.8 (e) also indicates that both t_{ch} and t_{ox} are required to be smaller than 5 nm to achieve a $|V_{th}|$ of more than $|-1.5|\ V$ at an Al composition of 18%, for example.

Due to the formation of hole quantum well, the quantum confinement effects, which are ignored in the present analysis, could displace the centroid of hole gas away from the interface between GaN channel and AlGaN barrier. If this displacement is large, it could effectively change the distance between the gate and 2DHG, producing a shift in V_{th}. The sensitivity of V_{th} towards these effects is studied in Fig. 4.8 (f), where V_{th} values for different thicknesses of oxide obtained by ignoring and considering the quantum confinement effects are plotted. As confirmed in this figure, for the range of thicknesses of oxide and channel layers of our interest, the variation in V_{th} owing to these effects remains trivial. Therefore, it is safe to ignore quantum confinement effects in the present study.

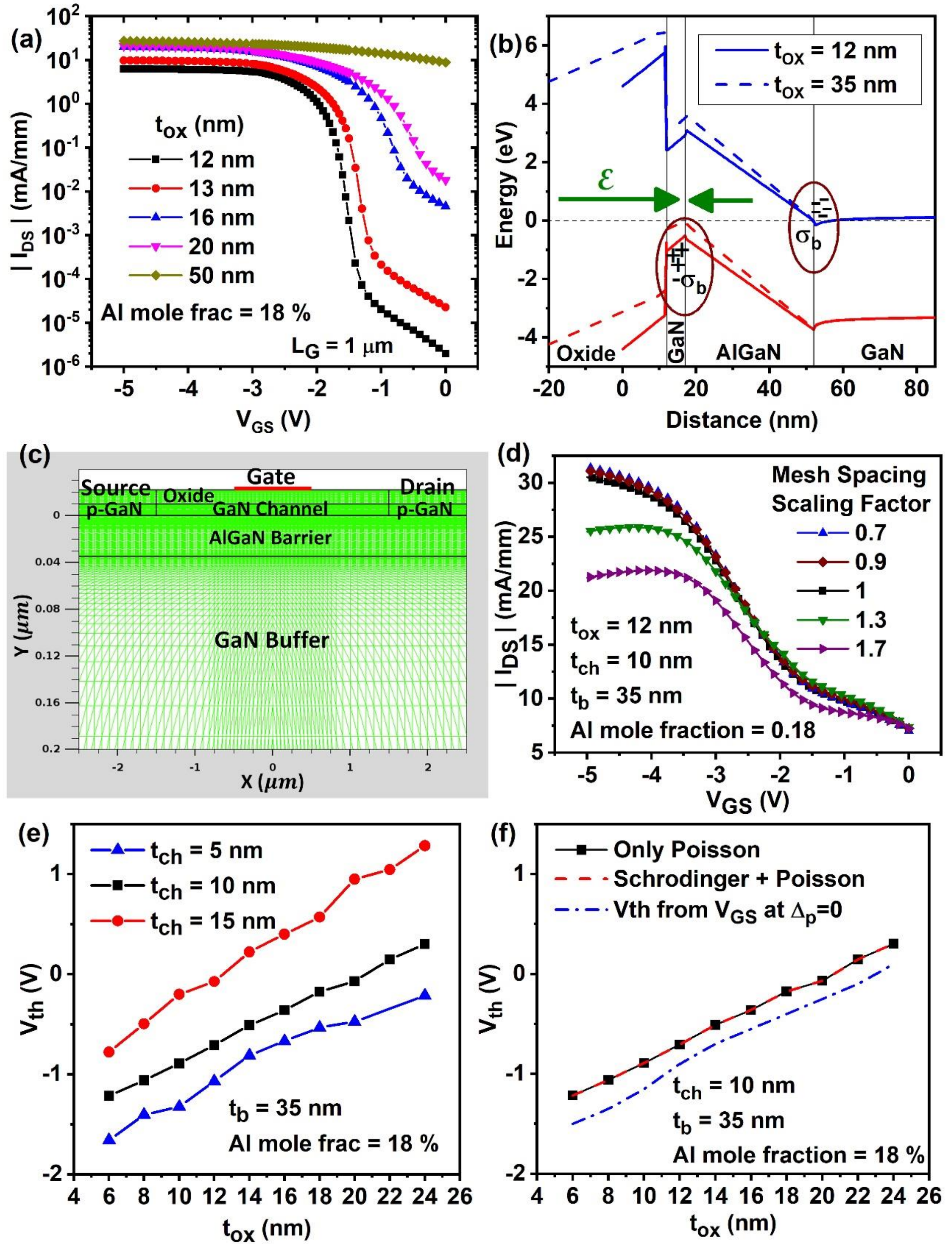

Fig. 4.8. (a) Comparison of simulated transfer characteristics and (b) energy band diagrams beneath the gate at different oxide (Al_2O_3) thicknesses t_{ox} in conventional heterostructure. (c) The placement of non-uniform mesh used in the simulation of this device. (d) Sensitivity of drain current to different mesh spacing. (e) Comparison of the threshold voltage V_{th} vs. t_{ox} at different channel thicknesses t_{ch}. (f) The behaviour of V_{th} obtained without and with quantum confinement effects and by reading V_{GS} for which the energy of the valence band along GaN channel/AlGaN barrier interface becomes equal to the Fermi level i.e. Δ_p becomes zero.

Fig. 4.8 (f) also shows the plot of the V_{th} obtained from the V_{GS} at which the energy of the valence band along the interface between GaN channel and AlGaN barrier approaches the energy of Fermi level, that is the value of V_{GS} for which the height of hole QW Δ_p becomes zero. Due to a high-energy tail of Fermi-Dirac distribution at high temperature, holes begin to accumulate in the valence band even before its energy matches with the Fermi level, thus the device is driven in the on-state. Therefore, as noted in this figure, the value of $|V_{th}|$ obtained from reading V_{GS} at $\Delta_p = 0$ remains $\sim|0.2|\ V$ larger than the one obtained using g_{max} method.

The derived threshold voltage in Eq. (4.8) for the conventional heterostructure is verified with the threshold voltage extracted from the simulated transfer characteristics in Figs. 4.9 (a) and (b). V_{th} predicted from Eq. (4.8) shows a good agreement with the simulated V_{th} for all range of t_{ch} and x_b in Figs. 4.9 (a) and (b). As opposed to the p-channel MOSFET in Si, $|V_{th}|$ of this device improves as the thickness of the channel or oxide is reduced. This contrasting behaviour is a result of the direction of the electric field between the gate and the 2DHG, as marked by the arrows in Fig. 4.6 (c), which is opposite in GaN to that of a p-channel MOSFET in Si. A reduction in the Al mole fraction in the barrier lowers the polarisation sheet charge density, which in turn leads to a reduction in the density of 2DHG. Hence, an improvement in $|V_{th}|$ is observed with a reduction in x_b. This behaviour of $|V_{th}|$ with a change in either t_{ch} or x_b has also been demonstrated experimentally in p-channel HFETs [14], [15]. The deviation between the prediction from Eq. (4.8) and the simulation at higher x_b results from a change in the ionized trap density, which has been ignored in Eq. (4.8) for simplicity.

A plot of I_{ON}/I_{OFF} against V_{th}, as x_b is varied (Fig. 4.9 (c)), shows a reduction from over 6 orders of magnitude to less than 1, with a reduction in $|V_{th}|$, indicating the trade-off that exists as the device moves from E- to D- mode as explained earlier. Furthermore,

$|I_{ON}|$ also reduces to less than half as the device turns from D-mode to E-mode irrespective of t_{ox} (Fig. 4.9 (d)), demonstrating the severity of the trade-off between $|I_{ON}|$ and $|V_{th}|$ which places a limit upon the conventional heterostructure in achieving E-mode behaviour with large $|I_{ON}|$ and high $|V_{th}|$ in p-channel GaN MOSHFETs.

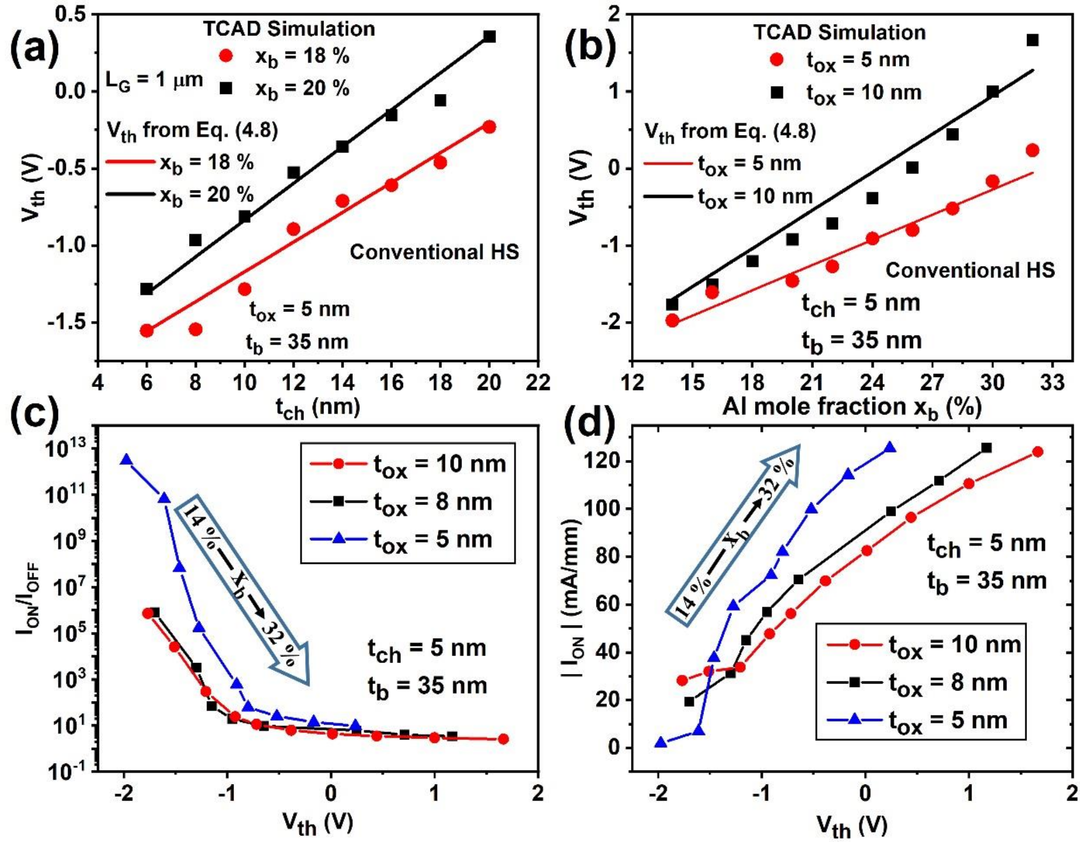

Fig. 4.9. Comparison of (a) V_{th} vs. t_{ch} for the conventional heterostructure at different Al mole fractions in the barrier x_b and (b) V_{th} vs. Al mole fraction x_b at different oxide (Al_2O_3) thicknesses t_{ox}, from simulation and Eq. (4.8). On-off current ratio I_{ON}/I_{OFF} is plotted against V_{th} for conventional heterostructure (HS) in (c), and $|I_{ON}|$ is plotted against V_{th} in (d) as x_b is varied at different values of t_{ox}. I_{ON}/I_{OFF} improves with a reduction in V_{th}, however the on-current also reduces as the device turns from D-mode to E-mode.

4.4. Analysis of the Alternate Heterostructure p-Channel MOSHFET

The above limitations are addressed here via the alternate heterostructure (Fig. 4.6 (b)), which employs an additional AlGaN cap layer, sandwiched between the insulator

and the GaN channel layer. The AlGaN cap introduces a positive polarisation charge (σ_{cap}) between cap/channel layer to modulate the electric field within the oxide and the AlGaN cap, as displayed in the corresponding band diagrams in Fig. 4.10 (a). If σ_{cap} exceeds a certain value (σ_{crit}), the electric field within the oxide and AlGaN cap layers reverses its direction, which, unlike in conventional heterostructure, causes the $|V_{th}|$ to rise with an increase in t_{ox}, as shown in Fig. 4.10 (b).

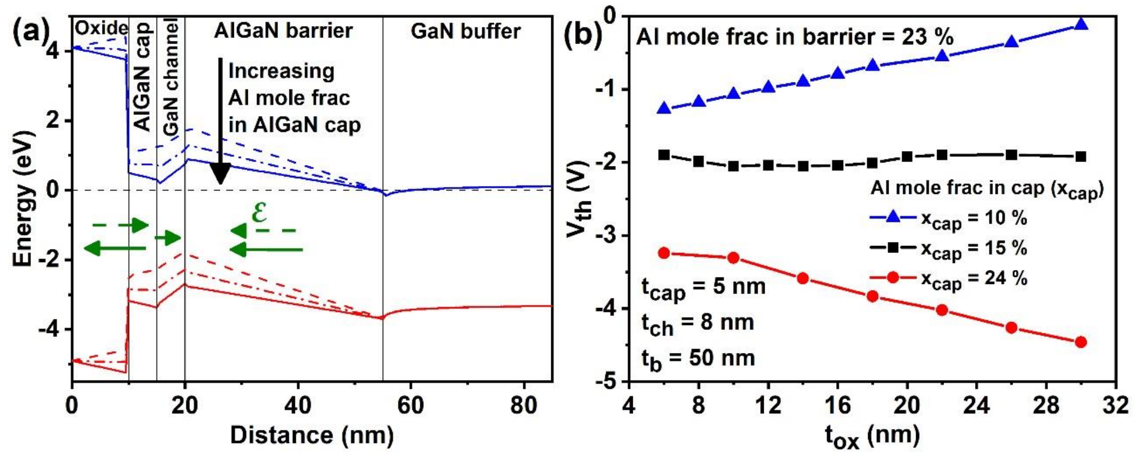

Fig. 4.10. (a) Variation in the energy band diagram for alternate heterostructure under the gate with a change in Al mole fractions in AlGaN cap. (b) V_{th} vs. t_{ox} (Al_2O_3) at different Al mole fraction in cap layer x_{cap}. With a rise in x_{cap}, behavior of V_{th} with t_{ox} becomes opposite to that in conventional heterostructure.

An increase in x_{cap} also lowers the valence band energy in the GaN channel (Fig. 4.10 (a)), leading to an increase in $|V_{th}|$, irrespective of the t_{ox}, as shown in Fig. 4.11 (a). The simulation results for V_{th} are in close agreement with those predicted by Eq. (4.14), as shown by the solid lines in Figs. 4.1 (a) and (b). Fig. 4.11 (b) shows clear evidence that increasing the Al mole fraction in the cap attempts to compensate the higher polarisation charge introduced by increasing the Al mole fraction in AlGaN barrier layer.

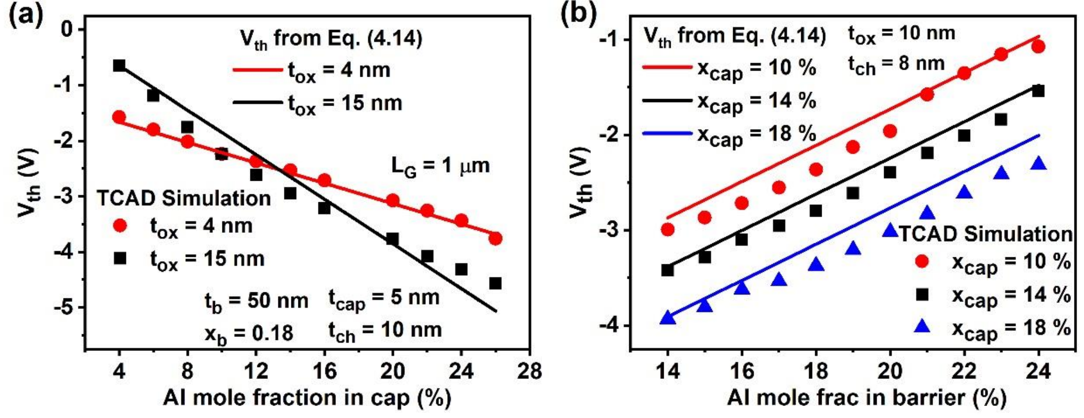

Fig. 4.11. (a) Comparison of V_{th} vs. x_{cap} in the alternate heterostructure with a channel thickness of 10 nm and an AlGaN cap at different oxide thicknesses t_{ox} from simulation and Eq. (4.14). (b) Comparison of V_{th} vs. Al mole fraction in barrier x_b at different Al mole fraction in cap x_{cap}.

Fig. 4.11 (a) also shows an intersection or cross-over point between the curves at different t_{ox}, which corresponds to x_{cap} in the range of $10 - 14\%$, below which the device behaves similar to a conventional structure i.e. a smaller $|V_{th}|$ at higher t_{ox}. An increase in x_{cap} beyond the cross-over point leads to an increase in the polarisation sheet charge at the interface of the AlGaN cap/GaN channel which causes the electric field in the oxide and the cap layers to now point towards the gate (Fig. 4.6 (d)), resulting in an increased $|V_{th}|$ at higher t_{ox}. To find out the polarisation sheet charge density in the cap layer corresponding to this cross-over $\sigma_{cap,co}$, we can solve for $\epsilon_{ox}\mathcal{E}_{ox}$ utilising Eqs. (4.4) and (4.10) – (4.12) while assuming a negligible density of hole gas, which leads to

$$\epsilon_{ox}\mathcal{E}_{ox} = \sigma_{ox} + \sigma_{cap} - \sigma_b + C_b \frac{E_G^{GaN}}{e} \tag{4.15}$$

The electric field within the oxide at the cross-over value of σ_{cap} must vanish. Hence substituting $\mathcal{E}_{ox}$ in Eq. (4.15) to zero, yields

$$\sigma_{cap,co} = \sigma_b - \sigma_{ox} - C_b \frac{E_G^{GaN}}{e} \tag{4.16}$$

This change in the behaviour of threshold voltage with the oxide thickness at higher x_{cap} is also apparent in Fig. 4.10 (b), at small x_{cap} the device shows a decrease in $|V_{th}|$

as t_{ox} becomes larger. However, as x_{cap} increases beyond the cross-over value of polarisation charge density in the cap $\sigma_{cap,co}$, as defined in Eq. (4.16), the behaviour of $|V_{th}|$ vs. t_{ox} in the alternate structure becomes opposite to that observed in the conventional one, where $|V_{th}|$ always reduces with an increase in t_{ox} (see Fig. 4.8 (e)). This work is the first to provide this insight into the reversal of V_{th} vs. t_{ox} behaviour at different Al mole fractions in AlGaN cap.

Results from Figs. 4.8 (e) and 4.9 (a) for the conventional structure indicate that a reasonable level of V_{th} ($\sim -1.5\ V$) can be obtained either by reducing the thicknesses of oxide and channel layers to $< 8\ nm$ and x_b (~18 %), which can put considerable strain on manufacturing processes particularly due to the control of Mg doping required. A reduction in t_{ch} and t_{ox} increases the electrical field along the vertical direction and causes a higher gate leakage current, while a reduction in x_b lowers the polarisation charge, necessary for producing a high density of 2DHG, thus resulting in a degradation in the on-current. In contrast, the threshold voltage in the alternate structure is not restricted by these limitations. By adjusting the x_{cap} in the AlGaN cap layer, the term σ_{cap}/C_{ocp} in Eq. (4.14), can be altered to produce a sufficiently large V_{th}. Moreover, once σ_{cap} is higher than its cross-over value in Eq. (4.16), a thicker oxide layer can be used to further increase the $|V_{th}|$. An increase in x_{cap}, however, also suppresses $|I_{ON}|$ (Fig. 4.12 (a)), due to an overall reduction in negative polarisation charge beneath the gate, leading to a reduction in 2DHG density under the gate. An increase in σ_{cap} at higher x_{cap} can effectively deplete the 2DHG under the gate leading to an improvement in the I_{ON}/I_{OFF}, by 14 orders of magnitude, as shown in Fig. 4.12 (b).

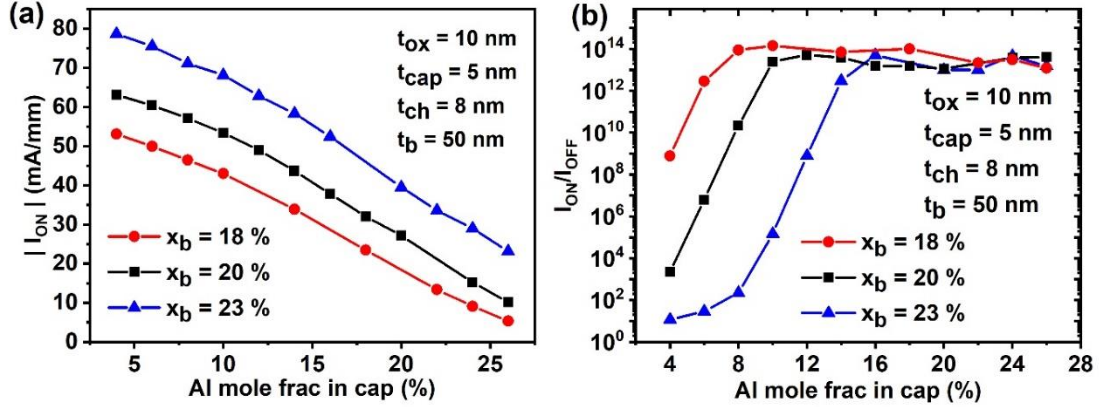

Fig. 4.12. (a) On-current vs. x_{cap} at different Al mole fraction in AlGaN barrier layer x_b, and (b) on-off current ratio with respect to x_{cap} at different x_b in alternate heterostructure.

Fig. 4.13 (a) shows $|I_{ON}|$ vs. V_{th} as x_b varies from 14 to 24 % for different values of x_{cap}. It can be seen that the trade-off between $|I_{ON}|$ and $|V_{th}|$, observed in the conventional heterostructure (Fig. 4.9 (d)) is also present in this heterostructure. However, if x_b varies for different values of x_{cap}, in Fig. 4.13 (a), as indicated by the green arrows, both $|I_{ON}|$ and $|V_{th}|$ can be made to increase simultaneously, thus overcoming the trade-off. Fig. 4.13 (b) shows one such example where x_{cap} varies with x_b as $1.8x_b - 0.25$. In contrast to Fig. 4.9 (d), $|I_{ON}|$ increases with $|V_{th}|$, reaching a maximum of $|-60|\ mA/mm$ at $|V_{th}|$ of $|-2.4|\ V$, at an oxide thickness of 6 nm used in these settings. This result is one of the most important findings of this thesis.

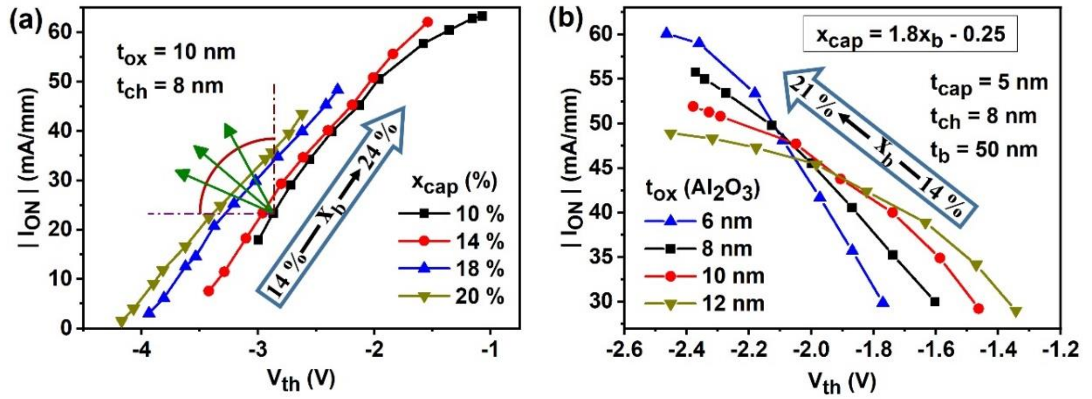

Fig. 4.13. (a) $|I_{ON}|$ vs. V_{th} as x_b is varied at different x_{cap} in alternate heterostructure, green arrows mark the directions along which both $|I_{ON}|$ and $|V_{th}|$ show an increase, (b) $|I_{ON}|$ vs. V_{th} along one of such directions, where x_{cap} is varied as $1.8x_b - 0.25$, at different Al_2O_3 thicknesses t_{ox} in alternate heterostructure.

In Fig. 4.14 (a), the transfer characteristics obtained from the p-channel MOSHFETs with HS1 and HS2 are compared for two different V_{th}. In both of these cases, the turn-on for HS1 occurs at smaller V_{GS} than for HS2 with a steeper slope. This is because without the additional AlGaN cap layer in HS1, the gate, which is now closer to the channel, can effectively modulate the hole gas density within the GaN channel across the oxide layer. However, due to the trade-off between $|I_{ON}|$ and $|V_{th}|$ in HS1, the $|I_{ON}|$ drops sharply to 20 mA/mm from 42 mA/mm as $|V_{th}|$ increases form $|-1.4|\ V$ to $|-2.3|\ V$. Moreover, since comparatively smaller x_b is used in HS1 to obtain a large $|V_{th}|$, $|I_{ON}|$ shows a saturation at higher V_{GS} due to the limited density of the 2DHG arising from a small polarization charge. Whereas an $|I_{ON}|$ of $\sim 50\ mA/mm$ is achieved at V_{th} of $|-2.3|\ V$ for HS2 which is more than double compared with HS1, demonstrating its superior performance over conventional heterostructure at higher $|V_{th}|$. The drain current characteristics in log scale at $V_{th} = -2.3\ V$ for HS2 are plotted in Fig. 4.14 (b), showing a potential for achieving high on-off current ratio of 10^{14}, and a subthreshold

swing (SS) of 85 mV/dec. Despite a high polarisation charge, a good SS is achieved in these devices. Since the polarisation charge, which is only dependent upon the lattice mismatch between AlGaN and GaN and does not change with a change in bias, i.e. $d\sigma_P/d\Psi_s = 0$, it does not contribute to SS.

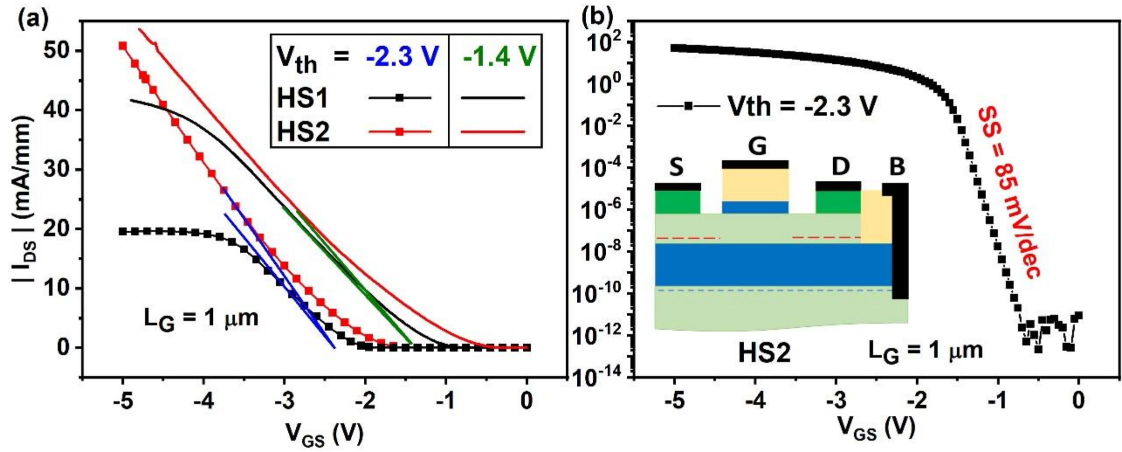

Fig. 4.14. (a) Comparison of transfer characteristics between two p-channel MOSHFETs employing heterostructure 1 (HS1) and heterostructure 2 (HS2). (b) Transfer characteristics in log scale for HS2 at $V_{th} = -2.3\ V$.

Figs. 4.15 (a) & (b) show the on-current and on-off current ratio with respect to change in the threshold voltage for p-channel MOSHFETs with both structures ($L_G = 1\ \mu m$) at the same oxide, channel, and barrier thicknesses. In the case of the conventional structure, the threshold voltage is varied by changing the Al mole fraction in the AlGaN barrier layer, while in the AlGaN cap structure, the V_{th} is controlled by adjusting the Al mole fraction in AlGaN cap with x_b kept fixed at $\sim 23\%$, as shown.

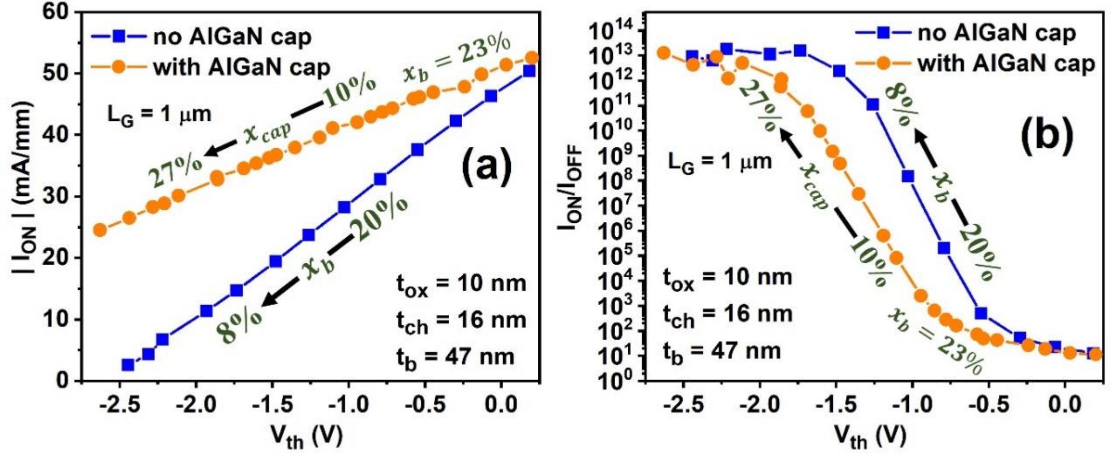

Fig. 4.15. Comparison of electrical performance of p-channel MOSHFETs with and without the AlGaN cap layer as a function of threshold voltage. (a) On-current $|I_{ON}|$ *vs.* threshold voltage V_{th}, (b) On-Off current ratio I_{ON}/I_{OFF} *vs.* threshold voltage V_{th}.

With an increase in $|V_{th}|$ in Fig. 4.15 (a), the on-current reduces, as expected in a conventional device, due to the overall reduction in the density of 2DHG in all regions including the access regions. For the alternate structure, an increase in x_{cap} depletes the 2DHG only under the gate, thus not affecting the series resistance of the access regions of the contacts. Thus, $|I_{ON}|$ drops more sharply with the increase in $|V_{th}|$ for the conventional device.

On-off current ratio, which we have defined as the ratio of the currents in the on-state ($V_{GS} = -5\ V$) and off-state ($V_{GS} = 0\ V$) of a normally-off p-channel device, shows a rise by orders of magnitude with an increase in $|V_{th}|$ in Fig. 4.15 (b). Since the devices do not turn-off completely when V_{th} is close to $0\ V$, hence a poor on-off current ratio of ~ 1 is observed. As $|V_{th}|$ increases, a higher on-off current ratio in the conventional structure arises from a smaller off-current or leakage current due to a low density of 2DHG. Additionally, the gate retains better electrostatic control in modulating the charge density in the channel giving an $I_{ON}/I_{OFF} \sim 3$ order of magnitude higher compared to the AlGaN cap device for V_{th} in the range of $[-0.75, -1.5]\ V$. However, at even higher $|V_{th}|$, $> |-2.0|\ V$, a higher polarisation charge introduced by the AlGaN cap layer

effectively depletes the 2DHG under the gate, thus suppressing the off-current, which results in both the devices showing a similar on-off current ratio.

4.5. SUMMARY

The threshold voltage characteristics of two candidate GaN heterostructures for p-type devices in GaN are examined with the help of analytical threshold voltage expressions derived in this work and TCAD simulations. We have demonstrated that in p-channel GaN MOSHFETs based upon the conventional heterostructure, a high $|V_{th}|$ comes at the expense of ultrathin oxide and channel layers while reducing Al mole fraction in the AlGaN barrier layer. These methods however can increase the leakage and degrade the device performance. Moreover, the on-current of the device drops to less than 50% as the device turns from D-mode to E-mode, creating a trade-off between on-current level and threshold voltage. An alternate heterostructure, consisting of an AlGaN cap layer on top of GaN channel with an underlying grounded 2DEG is explored here that shows potential to completely eliminate the trade-off highlighted in the devices on the conventional heterostructures, for a range of the mole fraction in the AlGaN cap. This approach is similar to the negative ion implantation technique for enabling normally-off operation in n-channel MOSHFETs. However, in the present case the positive charge to deplete in 2DHG under the gate originates from the polarisation difference between AlGaN cap and GaN channel.

The derived threshold voltage equation for this geometry proves that this heterostructure can potentially achieve a higher $|V_{th}|$ by adjusting the Al mole fraction in the AlGaN cap layer. It is demonstrated that by suitably adjusting the Al mole fraction in cap AlGaN layer the dependence of V_{th} upon oxide thickness can be reversed, and by appropriately adjusting mole fractions in both cap and barrier layers the trade-off observed in conventional heterostructure can also be minimized, which should no doubt

lead to higher performance than any E-mode p-channel GaN HFETs reported to date. A comparison between the two structures indicates that the trade-off in the alternate structure is much weaker even when mole fraction in AlGaN barrier is kept fixed. Hence, the alternate heterostructure shows a promising on-current of $\sim 30\ mA/mm$ at $|V_{th}|$ of $|-2|\ V$, which is more than double than that achievable in the device without the AlGaN cap layer. While the on-off current ratio for the AlGaN cap structure remains lower at threshold voltage below $|-2|\ V$, it shows an improvement with an increase in the $|V_{th}|$, becoming equivalent to the one achieved for a conventional heterostructure without AlGaN cap, $\sim 10^{12}$, at $|V_{th}|$ of greater than $|-2|\ V$.

4.6. REFERENCES

[1] U. K. Mishra, Shen Likun, T. E. Kazior, and Yi-Feng Wu, "GaN-Based RF Power Devices and Amplifiers," *Proc. IEEE*, vol. 96, no. 2, pp. 287–305, Feb. 2008. DOI: 10.1109/JPROC.2007.911060.

[2] D. Shibata, R. Kajitani, M. Ogawa, K. Tanaka, S. Tamura, T. Hatsuda, M. Ishida, and T. Ueda, "1.7 kV / 1.0 mΩcm^2 normally-off vertical GaN transistor on GaN substrate with regrown p-GaN/AlGaN/GaN semipolar gate structure," in *2016 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2016, p. 10.1.1-10.1.4. DOI: 10.1109/IEDM.2016.7838385.

[3] O. I. Saadat, J. W. Chung, E. L. Piner, and T. Palacios, "Gate-First AlGaN/GaN HEMT Technology for High-Frequency Applications," *IEEE Electron Device Lett.*, vol. 30, no. 12, pp. 1254–1256, Dec. 2009. DOI: 10.1109/LED.2009.2032938.

[4] H. Ishida, R. Kajitani, Y. Kinoshita, H. Umeda, S. Ujita, M. Ogawa, K. Tanaka, T. Morita, S. Tamura, M. Ishida, and T. Ueda, "GaN-based semiconductor devices for future power switching systems," in *2016 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2016, p. 20.4.1-20.4.4. DOI: 10.1109/IEDM.2016.7838460.

[5] A. Nakajima, Y. Sumida, M. H. Dhyani, H. Kawai, and E. M. Narayanan, "GaN-Based Super Heterojunction Field Effect Transistors Using the Polarization Junction Concept," *IEEE Electron Device Lett.*, vol. 32, no. 4, pp. 542–544, Apr. 2011. DOI: 10.1109/LED.2011.2105242.

[6] G. Li, R. Wang, B. Song, J. Verma, Y. Cao, S. Ganguly, A. Verma, J. Guo, H. G. Xing, and D. Jena, "Polarization-Induced GaN-on-Insulator E/D Mode p-Channel

Heterostructure FETs," *IEEE Electron Device Lett.*, vol. 34, no. 7, pp. 852–854, Jul. 2013. DOI: 10.1109/LED.2013.2264311.

[7] H. Hahn, B. Reuters, S. Kotzea, G. Lukens, S. Geipel, H. Kalisch, and A. Vescan, "First monolithic integration of GaN-based enhancement mode n-channel and p-channel heterostructure field effect transistors," in *72nd Device Research Conference*, Jun. 2014, vol. 60, no. 10, pp. 259–260. DOI: 10.1109/DRC.2014.6872396.

[8] A. Nakajima, S. Nishizawa, H. Ohashi, H. Yonezawa, K. Tsutsui, K. Kakushima, H. Wakabayashi, and H. Iwai, "One-chip operation of GaN-based P-channel and N-channel heterojunction field effect transistors," in *2014 IEEE 26th International Symposium on Power Semiconductor Devices & IC's (ISPSD)*, Jun. 2014, pp. 241–244. DOI: 10.1109/ISPSD.2014.6856021.

[9] R. Chu, Y. Cao, M. Chen, R. Li, and D. Zehnder, "An Experimental Demonstration of GaN CMOS Technology," *IEEE Electron Device Lett.*, vol. 37, no. 3, pp. 269–271, Mar. 2016. DOI: 10.1109/LED.2016.2515103.

[10] A. Nakajima, Y. Sumida, M. H. Dhyani, H. Kawai, and E. M. S. Narayanan, "High Density Two-Dimensional Hole Gas Induced by Negative Polarization at GaN/AlGaN Heterointerface," *Appl. Phys. Express*, vol. 3, no. 12, p. 121004, Dec. 2010. DOI: 10.1143/APEX.3.121004.

[11] A. Nakajima, P. Liu, M. Ogura, T. Makino, K. Kakushima, S. Nishizawa, H. Ohashi, S. Yamasaki, and H. Iwai, "Generation and Transportation Mechanisms for Two-Dimensional Hole Gases in GaN/AlGaN/GaN Double Heterostructures," *J. Appl. Phys.*, vol. 115, no. 15, p. 153707, Apr. 2014. DOI: 10.1063/1.4872242.

[12] P. Kozodoy, M. Hansen, S. P. DenBaars, and U. K. Mishra, "Enhanced Mg doping efficiency in Al0.2Ga0.8N/GaN superlattices," *Appl. Phys. Lett.*, vol. 74, no. 24, pp. 3681–3683, Jun. 1999. DOI: 10.1063/1.123220.

[13] A. Nakajima, P. Liu, M. Ogura, T. Makino, S. Nishizawa, S. Yamasaki, H. Ohashi, K. Kakushima, and H. Iwai, "Temperature-Independent Two-Dimensional Hole Gas Confined at GaN/AlGaN Heterointerface," *Appl. Phys. Express*, vol. 6, no. 9, p. 091002, Sep. 2013. DOI: 10.7567/APEX.6.091002.

[14] B. Reuters, H. Hahn, A. Pooth, B. Holländer, U. Breuer, M. Heuken, H. Kalisch, and A. Vescan, "Fabrication of p-channel heterostructure field effect transistors with polarization-induced two-dimensional hole gases at metal–polar GaN/AlInGaN interfaces," *J. Phys. D. Appl. Phys.*, vol. 47, no. 17, p. 175103, Apr. 2014. DOI: 10.1088/0022-3727/47/17/175103.

[15] H. Hahn, B. Reuters, A. Pooth, B. Hollander, M. Heuken, H. Kalisch, and A. Vescan, "p-Channel Enhancement and Depletion Mode GaN-Based HFETs With Quaternary Backbarriers," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3005–3011, Oct. 2013.

DOI: 10.1109/TED.2013.2272330.

[16] S. Yang, S. Huang, M. Schnee, Q.-T. Zhao, J. Schubert, and K. J. Chen, "Fabrication and Characterization of Enhancement-Mode High-κ LaLuO3-AlGaN/GaN MIS-HEMTs," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3040–3046, Oct. 2013. DOI: 10.1109/TED.2013.2277559.

[17] A. Kumar and M. M. De Souza, "Extending the bounds of performance in E-mode p-channel GaN MOSHFETs," in *2016 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2016, p. 7.4.1-7.4.4. DOI: 10.1109/IEDM.2016.7838368.

[18] F. J. Kub, T. J. Anderson, A. D. Koehler, and K. D. Hobart, "Inverted p-channel III-nitride field effect transistor with hole carriers in the channel," U.S. Patent No. 9,275,998, Aug. 2015.

[19] O. Ambacher, B. Foutz, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy, a. J. Sierakowski, W. J. Schaff, L. F. Eastman, R. Dimitrov, A. Mitchell, and M. Stutzmann, "Two dimensional electron gases induced by spontaneous and piezoelectric polarization in undoped and doped AlGaN/GaN heterostructures," *J. Appl. Phys.*, vol. 87, no. 1, p. 334, 2000. DOI: 10.1063/1.371866.

[20] A. Nakajima, S. Kubota, K. Tsutsui, K. Kakushima, H. Wakabayashi, H. Iwai, S. Nishizawa, and H. Ohashi, "GaN-based complementary metal–oxide–semiconductor inverter with normally off Pch and Nch MOSFETs fabricated using polarisation-induced holes and electron channels," *IET Power Electron.*, vol. 11, no. 4, pp. 689–694, 2018. DOI: 10.1049/IET-PEL.2017.0376.

[21] "Silvaco TCAD Atlas." Version V3.44.1R https://www.silvaco.com/products/tcad.html. [Accessed: 10-Dec. 2018].

[22] J. D. Albrecht, R. P. Wang, P. P. Ruden, M. Farahmand, and K. F. Brennan, "Electron transport characteristics of GaN for high temperature device modeling," *J. Appl. Phys.*, vol. 83, no. 9, p. 4777, 1998. DOI: 10.1063/1.367269.

[23] M. Farahmand, C. Garetto, E. Bellotti, K. F. Brennan, M. Goano, E. Ghillino, G. Ghione, J. D. Albrecht, and P. P. Ruden, "Monte Carlo simulation of electron transport in the III-nitride wurtzite phase materials system: binaries and ternaries," *IEEE Trans. Electron Devices*, vol. 48, no. 3, pp. 535–542, Mar. 2001. DOI: 10.1109/16.906448.

[24] C.-S. Lee, Y.-J. Lin, and C.-T. Lee, "Investigation of oxidation mechanism for ohmic formation in Ni/Au contacts to p -type GaN layers," *Appl. Phys. Lett.*, vol. 79, no. 23, pp. 3815–3817, Dec. 2001. DOI: 10.1063/1.1425065.

[25] F. G. Kalaitzakis, N. T. Pelekanos, P. Prystawko, M. Leszczynski, and G. Konstantinidis, "Low resistance as-deposited Cr⁄Au contacts on p-type GaN," *Appl. Phys. Lett.*, vol. 91, no. 26, p. 261103, Dec. 2007. DOI: 10.1063/1.2828044.

[26] J.-H. Lim, E.-J. Yang, D.-K. Hwang, J.-H. Yang, J.-Y. Oh, and S.-J. Park, "Highly

transparent and low resistance gallium-doped indium oxide contact to p-type GaN," *Appl. Phys. Lett.*, vol. 87, no. 4, p. 042109, Jul. 2005. DOI: 10.1063/1.1999012.

[27] K. Lee, Z. Wu, Z. Chen, F. Ren, S. J. Pearton, and A. G. Rinzler, "Single Wall Carbon Nanotubes for p-Type Ohmic Contacts to GaN Light-Emitting Diodes," *Nano Lett.*, vol. 4, no. 5, pp. 911–914, May 2004. DOI: 10.1021/NL0496522.

[28] J.-O. Song, J. S. Kwak, Y. Park, and T.-Y. Seong, "Ohmic and degradation mechanisms of Ag contacts on p-type GaN," *Appl. Phys. Lett.*, vol. 86, no. 6, p. 062104, Feb. 2005. DOI: 10.1063/1.1863441.

[29] H. W. Jang, J. H. Son, and J.-L. Lee, "Highly reflective low resistance Ag-based Ohmic contacts on p-type GaN using Mg overlayer," *Appl. Phys. Lett.*, vol. 90, no. 1, p. 012106, Jan. 2007. DOI: 10.1063/1.2430405.

[30] D.-H. Kim, W. C. Lim, J.-S. Park, and T.-Y. Seong, "Highly thermally stable Pd/Zn/Ag ohmic contact to Ga-face p-type GaN," *J. Alloys Compd.*, vol. 588, pp. 327–331, Mar. 2014. DOI: 10.1016/J.JALLCOM.2013.11.044.

[31] W.-K. Hong, J.-O. Song, H.-G. Hong, K.-Y. Ban, T. Lee, J. S. Kwak, Y. Park, and T.-Y. Seong, "Highly Reflective and Low Resistance Indium Tin Oxide/Ag Ohmic Contacts to p-Type GaN for Flip-Chip Light Emitting Diodes," *Electrochem. Solid-State Lett.*, vol. 8, no. 11, p. G320, 2005. DOI: 10.1149/1.2056467.

[32] J. H. Son, G. H. Jung, and J.-L. Lee, "Enhancement of light reflectance and thermal stability in Ag–Cu alloy contacts on p-type GaN," *Appl. Phys. Lett.*, vol. 93, no. 1, p. 012102, Jul. 2008. DOI: 10.1063/1.2956417.

[33] V. Adivarahan, A. Lunev, M. A. Khan, J. Yang, G. Simin, M. S. Shur, and R. Gaska, "Very-low-specific-resistance Pd/Ag/Au/Ti/Au alloyed ohmic contact to p GaN for high-current devices," *Appl. Phys. Lett.*, vol. 78, no. 18, pp. 2781–2783, Apr. 2001. DOI: 10.1063/1.1353813.

[34] J.-L. Lee, M. Weber, J. K. Kim, J. W. Lee, Y. J. Park, T. Kim, and K. Lynn, "Ohmic contact formation mechanism of nonalloyed Pd contacts to p -type GaN observed by positron annihilation spectroscopy," *Appl. Phys. Lett.*, vol. 74, no. 16, pp. 2289–2291, Apr. 1999. DOI: 10.1063/1.123827.

[35] C. Huh, S.-W. Kim, H.-M. Kim, D.-J. Kim, and S.-J. Park, "Effect of alcohol-based sulfur treatment on Pt Ohmic contacts to p -type GaN," *Appl. Phys. Lett.*, vol. 78, no. 13, pp. 1942–1944, Mar. 2001. DOI: 10.1063/1.1358356.

[36] J. O. Song, D.-S. Leem, J. S. Kwak, O. H. Nam, Y. Park, and T.-Y. Seong, "High-quality nonalloyed rhodium-based ohmic contacts to p-type GaN," *Appl. Phys. Lett.*, vol. 83, no. 12, pp. 2372–2374, Sep. 2003. DOI: 10.1063/1.1613991.

[37] J.-S. Jang, S.-J. Park, and T.-Y. Seong, "Metallization scheme for highly low-resistance, transparent, and thermally stable Ohmic contacts to p -GaN," *Appl. Phys. Lett.*, vol. 76,

no. 20, pp. 2898–2900, May 2000. DOI: 10.1063/1.126510.

[38] T. Margalith, O. Buchinsky, D. A. Cohen, A. C. Abare, M. Hansen, S. P. DenBaars, and L. A. Coldren, “Indium tin oxide contacts to gallium nitride optoelectronic devices,” *Appl. Phys. Lett.*, vol. 74, no. 26, pp. 3930–3932, Jun. 1999. DOI: 10.1063/1.124227.

[39] S. W. Chae, K. C. Kim, D. H. Kim, T. G. Kim, S. K. Yoon, B. W. Oh, D. S. Kim, H. K. Kim, and Y. M. Sung, “Highly transparent and low-resistant ZnNi/indium tin oxide Ohmic contact on p-type GaN,” *Appl. Phys. Lett.*, vol. 90, no. 18, p. 181101, Apr. 2007. DOI: 10.1063/1.2731672.

[40] J. O. Song, K.-K. Kim, S.-J. Park, and T.-Y. Seong, “Highly low resistance and transparent Ni/ZnO ohmic contacts to p -type GaN,” *Appl. Phys. Lett.*, vol. 83, no. 3, pp. 479–481, Jul. 2003. DOI: 10.1063/1.1591236.

[41] J. Chen and W. D. Brewer, “Ohmic Contacts on p-GaN,” *Adv. Electron. Mater.*, vol. 1, no. 8, p. 1500113, Aug. 2015. DOI: 10.1002/AELM.201500113.

[42] S. Kubota, R. Kayanuma, A. Nakajima, S. Nishizawa, and H. Ohashi, “P-channel AlGaN/GaN MOSFETs for Normally-Off Operation,” in *Material Research Society*, Nov. 2015, p. RR1.02.

[43] H. Hahn, “Threshold Voltage Engineering of GaN-based n-Channel and p-Channel Heterostructure Field Effect Transistors,” RWTH Aachen University, 2014.

[44] Silvaco Inc., *Atlas User’s Manual*. Silvaco International Software, Santa Clara, CA, USA, Aug. 2016.

Chapter 5 An E-Mode P-Channel GaN MOSHFET for a CMOS Compatible PMIC

In the previous chapter, introduction of positive polarisation charge by utilising an AlGaN cap layer between the gate oxide and channel with an underlying grounded 2DEG is shown to be one of the promising techniques to deplete a two-dimensional hole gas (2DHG) to achieve an E-mode p-channel GaN MOSHFET. Here, we analyse the impact of gate length and channel thickness upon the operation of a low power E-mode p-channel GaN MOSHFET utilising AlGaN cap via TCAD simulations. The challenges of achieving negative threshold voltage with the scaling of gate length are addressed by adjusting the mole fraction of an AlGaN cap layer beneath the gate. An inverter consisting of the proposed p-channel GaN MOSHFET with a gate length of $0.25\ \mu m$ shows promise of a CMOS compatible Power Management IC in the MHz range.

However, a key issue with a device employing an AlGaN cap is the off-state leakage in this device increases by orders of magnitude for channel layers thicker than 20 nm, which cannot be controlled by adjusting the Al mole fraction in cap layer alone. Biasing the two-dimensional electron gas (2DEG) beneath the 2DHG, as employed by A. Nakajima *et al.* [1] helps alleviate this limitation at the cost of a reduction in on-current. Scaling the access regions and combining the two techniques, AlGaN cap and biased 2DEG, allows maximum benefit in terms of on-state current, negative threshold voltage and on/off current ratio.

5.1. Introduction

Among the various techniques for overcoming the trade-off between the on-resistance and breakdown voltage in a high power device in GaN, polarisation superjunction (PSJ) technology [2], [3] is considered as the equivalent of CoolMOS in

silicon [4]. The presence of a polarisation induced 2DHG above the 2DEG across the barrier layer forms a superjunction, where the charge compensation provided by 2DHG facilitates a nearly constant electric field in the region between these gases [3]. This approach can effectively prevent current collapse by suppressing the non-linear distribution of the electric field around the drain-side gate edge, thus improving reliability. GaN HFETs utilising PSJ with the breakdown voltage exceeding $2\ kV$ along with an on-resistance of $31.5\ \Omega\ mm$ have already been demonstrated [5].

The next challenge for GaN power devices is integration of the gate driver and power device, to reduce the parasitic loop inductance and facilitate high frequency switching in converters [6], [7]. Additionally, complementary logic with normally-off (E-mode) operation is preferred to reduce static power consumption, simplify circuitry and for fail-safe operation [8]. Therefore, a p-channel E-mode GaN MOSHFET is desirable.

The inherent use of the 2DHG in a PSJ heterostructure (GaN/AlGaN/GaN or GaN/AlInGaN/GaN) makes it an option for a platform for such integration. The operation of both p-channel and n-channel devices has been attempted on this platform [6], [9]. Achieving E-mode operation in GaN is challenging because the polarisation induced 2DEG or 2DHG first needs to be depleted at zero gate voltage. In n-channel GaN HFETs or MOSHFETs, among the various techniques to implement E-mode behaviour, as introduced in chapter 3, the recessed gate [10]–[12], or ion implantation [13]–[15] methods can be employed on a PSJ platform. E-mode operation of p-channel HFETs has been attempted via recessed gate [7], [16], [17], which is also compatible with PSJ platform. However, as shown in the previous chapter achieving a $|V_{th}| > |-2\ V|$ (for example in fail-safe applications such as automotive), via recessed gate alone, requires the thickness of the oxide and GaN channel layers to be reduced to $\sim 5\ nm$ for an AlGaN barrier with Al mole fraction of $18\ \%$, leading to challenges in manufacturing and

reliability. In an alternate approach, the polarisation charge introduced by the AlInGaN (or AlGaN) barrier layer can be reduced by adjusting the mole fraction of the component materials [18]. This approach has been shown to yield a high on-off current ratio of $\sim 10^8$, with an on-current density of $\sim 0.3\, mA/mm$ and a V_{th} of $\sim -1.5\, V$. Nevertheless, a reduction in the polarisation charge also leads to a reduction in the density of 2DEG, thus affecting the performance of other n-channel devices on the platform. In the approach from R. Chu *et al.* [7], the GaN layer beneath the AlGaN barrier that contains the 2DEG is etched away, and AlGaN/GaN layers regrown to generate a 2DHG layer for p-type conduction. On the other hand, A. Nakajima *et al.* [19] use a bias voltage on the underlying 2DEG to modulate the threshold voltage of a p-channel device. This helps to obtain saturated $I_{DS} - V_{DS}$, since non-saturated $I_{DS} - V_{DS}$ characteristics are observed with a floating 2DEG. In chapter 4, we have examined an alternative heterostructure that utilises an AlGaN cap [20] beneath the gate for implementing a high performance normally-off p-channel MOSHFET [21], [22]. In this work, the dependence of the electrical characteristics of a p-channel GaN MOSHFET on gate length and switching speed of the inverter utilising this device are investigated on a platform that is fully compatible with a power device in PSJ technology. The substrate parameters are closely aligned to those reported in [7], [16]. Subsequently, we evaluate the limits of capability of such a p-channel MOSHFET in GaN when integrated with power devices for power converter on a chip. We use simulations to analyse the benefits of a combination of techniques to achieve an optimum device performance, despite limitations of the poor mobility of holes. A modified AlGaN cap device with a biased 2DEG is proposed in this work, to aid the operation of the AlGaN cap in depleting the 2DHG under the gate and thus resolving one of the important problems that prohibit manufacture of the AlGaN cap structure as proposed in [20].

5.2. METHODOLOGY AND SETTINGS

Fig. 5.1 highlights a schematic of an integration platform consisting of a low power CMOS device and a high power PSJ MOSHFET. In comparison to the previous chapter, we consider a p-GaN/GaN/AlGaN/GaN heterostructure with layer specifications consisting of, from top to bottom, 30 nm Mg-doped p-GaN, 20 nm undoped GaN, $\sim 47-48$ nm AlGaN barrier with Al mole fraction of 23%, and a 1.5 μm GaN buffer on a substrate [23]. Additionally, following the work of A. Nakajima *et al.* [19], the 2DEG is kept grounded. All simulations are carried out using the TCAD model, introduced in the previous chapter.

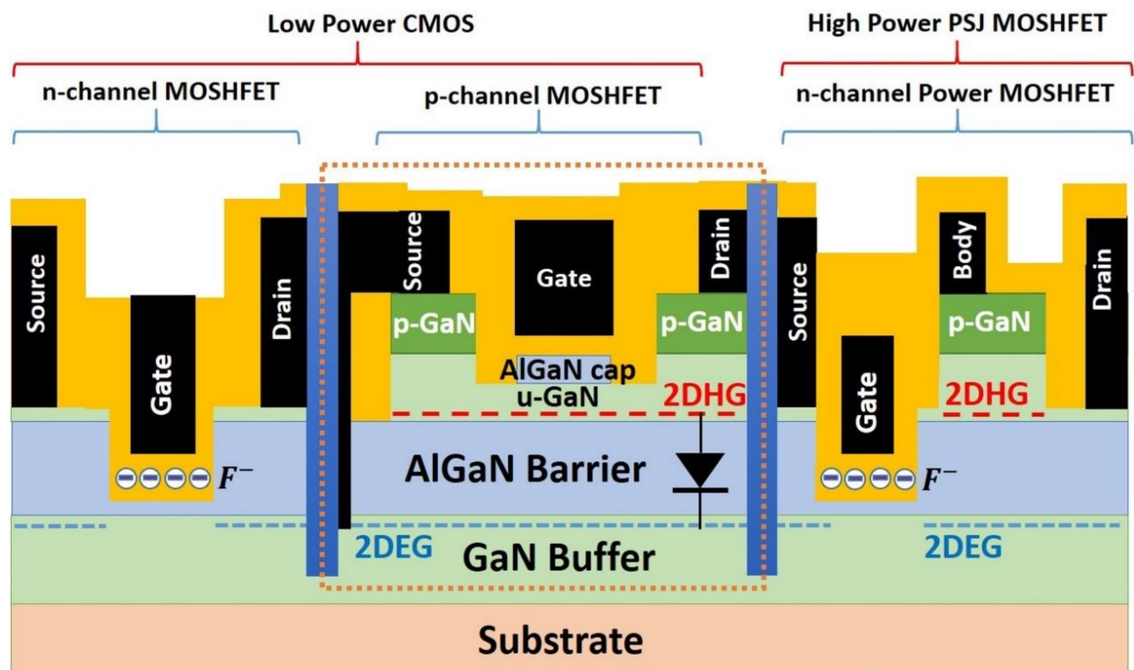

Fig. 5.1. Schematic of a common GaN/AlGaN/GaN platform consisting of low power CMOS and High Power PSJ MOSHFET. The 2DEG is connected to ground. A combination of the 2DHG, AlGaN barrier, and 2DEG forms a diode that remains reverse biased.

5.3. IMPACT OF GATE LENGTH ON PERFORMANCE

E-mode operation in a conventional heterostructure without an AlGaN cap is examined by comparing the band diagrams at two different thicknesses of the oxide and

channel layers (t_{ox} & t_{ch}) in Fig. 5.2 (a). Thinner oxide and GaN channel are required so that, sharp band bending in these layers can prevent the valence band at the GaN/AlGaN heterointerface from crossing the Fermi level, thus giving E-mode behaviour.

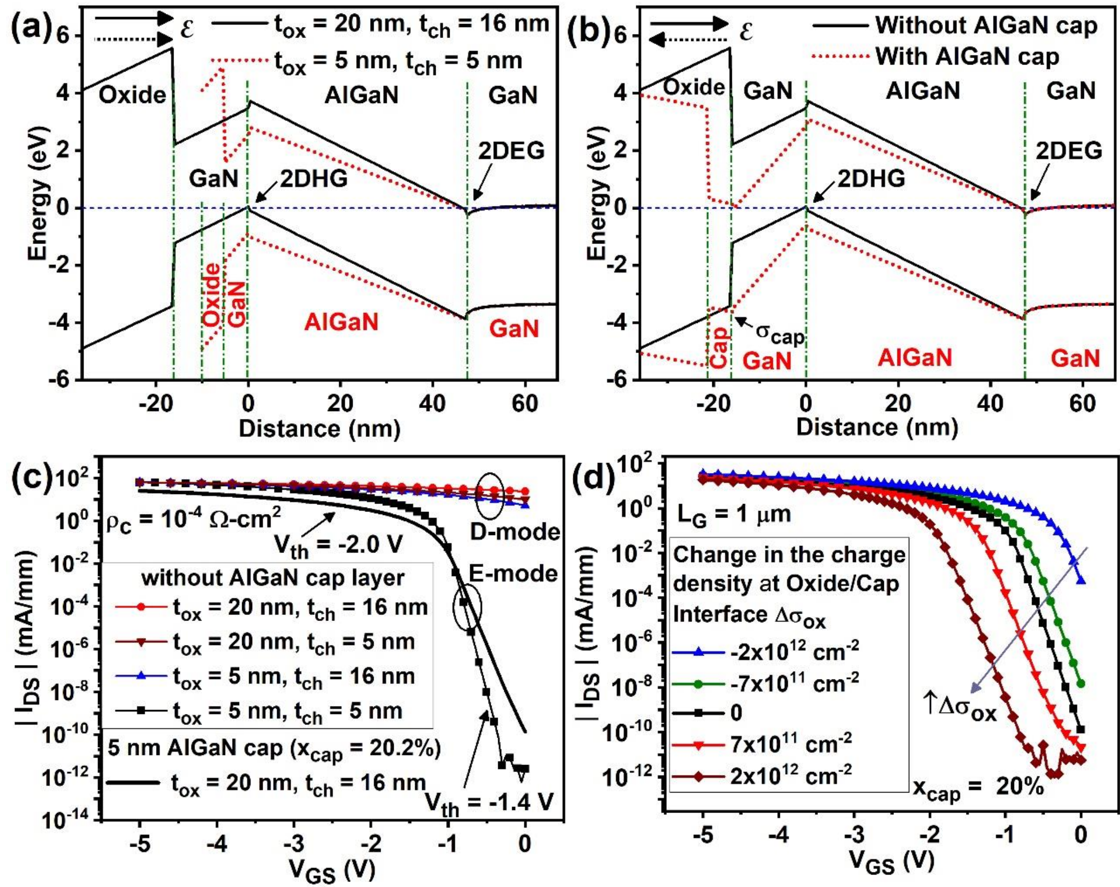

Fig. 5.2. (a) Comparison of the band diagram at two thicknesses of oxide and channel in a structure without an AlGaN cap, (b) Comparison of the band diagram with and without an AlGaN cap, (c) Simulated $I_{DS} - V_{GS}$ characteristics showing the dependence on thickness of the oxide and channel layers, with and without the AlGaN cap layer, (d) Simulated impact of trap charge density at the interface of the oxide and AlGaN cap.

In contrast, inclusion of an AlGaN cap introduces a positive polarisation charge at the heterointerface between the AlGaN cap and the GaN channel, σ_{cap}, which can be controlled by changing the Al mole fraction in the cap layer x_{cap}. A comparison of the band diagrams with and without the AlGaN cap in Fig. 5.2 (b), illustrates that a presence of the polarisation charge σ_{cap} increases band bending in the GaN channel, leading to elimination of the hole quantum well at the GaN/AlGaN interface. This consequently

leads to E-mode operation for thicker layers of the channel and oxide in comparison to that in the conventional structure. It can also be noted in Fig. 5.2 (b) that the introduction of σ_{cap} alters the direction of the electric field in the oxide. This is of crucial benefit that reverses the behaviour of $|V_{th}|$ with respect to t_{ox} as opposed to that in the conventional device, discussed in previous chapter.

The transfer characteristics of devices in Fig. 5.2 (c) reveal that without the presence of the AlGaN cap, the thicknesses of the oxide and GaN channel layers (t_{ox} & t_{ch}) need to be reduced to $\sim 5\ nm$ to increase the $|V_{th}|$ to $|-1.4|\ V$. Such low values introduce considerable constraints on the manufacturability of the conventional structure (without an AlGaN cap). Owing to the trade-off between $|V_{th}|$ and $|I_{ON}|$, the maximum drain current $|I_{ON}|$, for the structure with AlGaN cap, at a higher $|V_{th}|$ of $|-2\ V|$ remains smaller ($25\ mA/mm$) than that of the structure without an AlGaN cap at a smaller $|V_{th}|$ of $|-1.4\ V|$ ($62\ mA/mm$). The trap charge at the interface of the oxide and AlGaN cap could vary due to processing or during device switching. Fig. 5.2 (d) compares the transfer characteristics with the change in the net trap density at the interface of the oxide/AlGaN cap σ_{ox}, showing that a large variation in σ_{ox} ($> 7 \times 10^{11} cm^{-2}$) can significantly affect the V_{th} and on-off current ratio of the device.

As shown in Fig. 5.1, a combination of the 2DHG, AlGaN barrier, and 2DEG acts as a p-n diode, where the AlGaN barrier of $47\ nm$ acts as a depletion region between the 2DEG and 2DHG. With negative voltage on the drain and gate, this diode remains reverse biased, and leakage current through the 2DEG in this condition has been experimentally shown to be $\sim 10\ nA/mm$ through the AlGaN barrier [24]. This agrees with negligible values in the simulations.

The behaviour of the threshold voltage with the Al mole fraction x_{cap}, in Fig. 5.3 (a), depicts a rise in $|V_{th}|$ with x_{cap}. At higher x_{cap}, the band bending in the GaN channel

becomes more pronounced due to an increase in polarisation σ_{cap}, leading to a lowering of the valence band at the GaN channel/AlGaN barrier interface. A $|V_{th}|$ of $|-3.0\ V|$ is achievable for an x_{cap} of 23%.

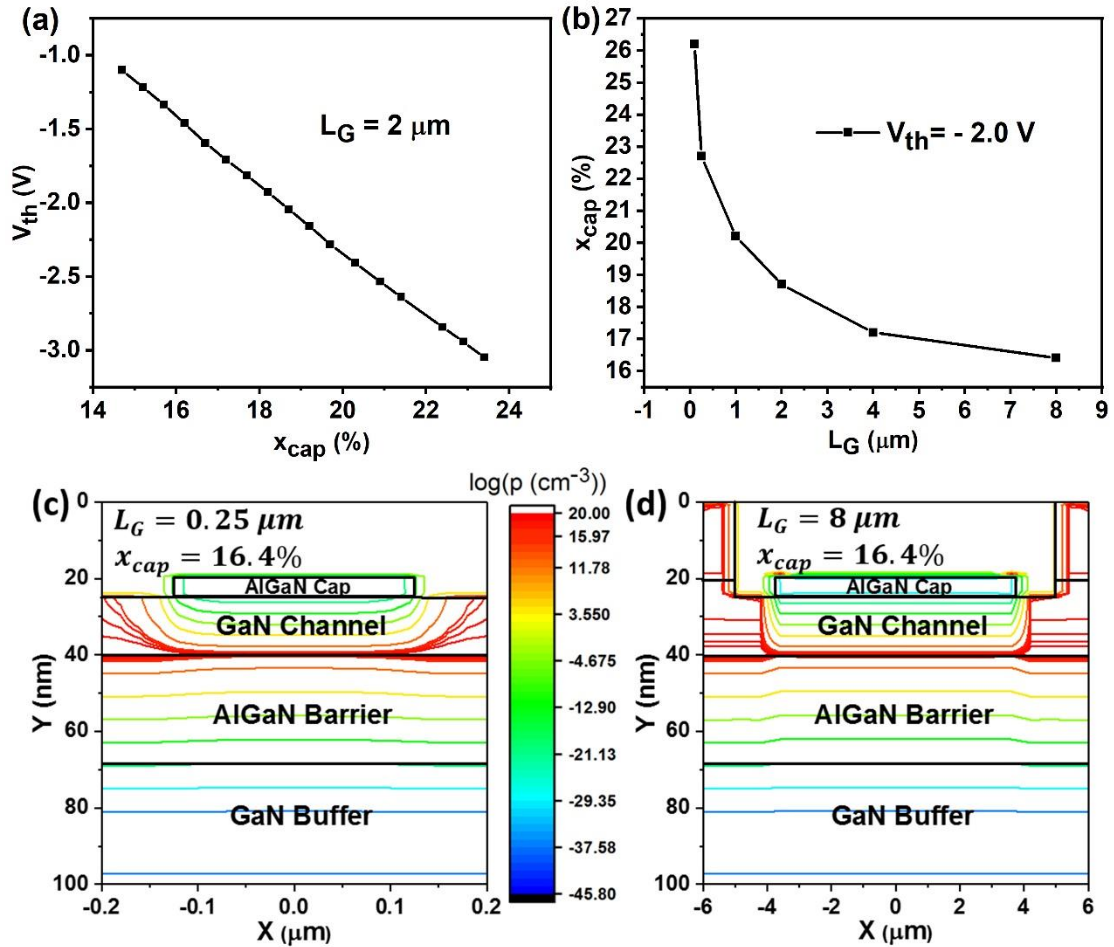

Fig. 5.3. (a) Threshold voltage V_{th} *vs.* Al mole fraction in the AlGaN cap layer x_{cap}. (b) x_{cap} *vs.* gate length L_G to maintain a fixed V_{th} of $-2\ V$. (c) and (d) are the contour plots of the hole density in devices with gate lengths of 0.25 μm and 8 μm, respectively.

In comparison to silicon, the V_{th} of the current heterostructure is not just dependent upon the vertical thicknesses but also severely upon the gate length L_G. It is seen in Fig. 5.3 (b) that with reduction of L_G, a higher x_{cap} is required to maintain the $|V_{th}|$ at $|-2\ V|$. To understand this behaviour, the contour plots of the device cross section under zero gate bias are presented in Figs. 5.3 (c) & 5.3 (d) for two different gate lengths (0.25 μm and 8 μm). The dependency between V_{th} and L_G arises from the fact that a 2DHG forms

at the bottom interface of the GaN channel which is farther from the gate rather than at the top interface. Hence, even though holes in the vicinity of the top interface in the GaN channel are depleted irrespective of the gate length, as shown in Figs. 5.3 (c) & 5.3 (d), there is a finite penetration of holes under the gate at the bottom interface of the channel. It is observed from Figs. 5.3 (c) & 5.3 (d) that at smaller L_G, the relative penetration of holes at the bottom interface of the GaN channel under the AlGaN cap is higher, leading to a degradation in $|V_{th}|$. Hence, x_{cap} needs to be raised from $16.4\ \%$ to $26.2\ \%$ as the gate length is reduced from 8 μm to $0.10\ \mu m$ to maintain V_{th} at a fixed value of $-2.0\ V$ (Fig. 5.3 (b)).

As shown in Fig. 5.4, utilising a smaller channel length not only increases $|I_{ON}|$ (defined as $|I_{DS}|$ at $V_{GS} = V_{DS} = -5\ V$) but also leads to an improvement in on-off current ratio I_{ON}/I_{OFF} for devices with identical V_{th}. With smaller L_G, the length of the region depleted of 2DHG in the GaN channel also becomes smaller, leading to a reduction in the total sheet resistance between the drain and source. Therefore, $|I_{ON}|$ of the device improves at smaller L_G, achieving a maximum of $37\ mA/mm$ at L_G of $0.10\ \mu m$. The improvement in I_{ON}/I_{OFF} emerges from a higher x_{cap} at smaller L_G to maintain the threshold voltage. The rise in σ_{cap} with higher x_{cap} suppresses the relative penetration of holes under the gate thereby minimizing the leakage current. Hence, the ratio of I_{ON}/I_{OFF} shows an improvement from ~ 2 to ~ 12 orders of magnitude as L_G shrinks from 8 μm to $0.25\ \mu m$. However, at the shorter gate length ($0.10\ \mu m$), a higher σ_{cap}, necessary to maintain the same V_{th} no longer suffices to suppress the relative penetration of holes under the gate. This increases the off-current of the device, resulting in a degradation in the on-off current ratio by an order of magnitude. Hence a gate length of $0.25\ \mu m$ can be considered optimal.

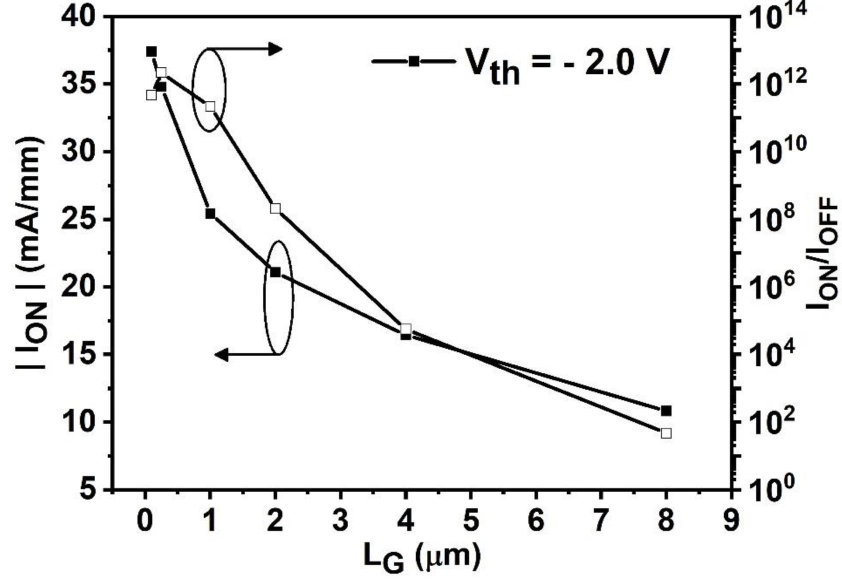

Fig. 5.4. Behaviour of the on-current $|I_{ON}|$ and I_{ON}/I_{OFF} with gate length L_G as x_{cap} is changed to keep a fixed threshold voltage V_{th} of $-2.0\ V$.

The circuit diagram for calculating the rise time and switching speed of an inverter, using mixed mode simulations is shown in Fig. 5.5 (a). The rise time for a load capacitor C_L is calculated as $t_{Rise} = \int_0^{0.9\times V_{DD}} dV \cdot C_L/I_{DS}$. The total load capacitance for a fan-out of 5 at the output is estimated as:

$$C_L \approx 5\left(1+\frac{W_n}{W_p}\right)C_{GS,max} + \left(1+\frac{W_n}{W_p}\right)C_{DS,max} \quad (1)$$

where $C_{GS,max}$ and $C_{DS,max}$ are the maximum values of the gate and drain capacitances for the p-channel GaN MOSHFET, and the factor $\left(1+W_n/W_p\right)$ accounts for n- and p-channel devices with W_n and W_p widths. With W_n/W_p of $1/10$, the rise time t_{Rise} of devices, with and without the AlGaN cap, are extracted from the transient simulations of output voltage V_{OUT} with time in Fig. 5.5 (b) at a gate length of $0.25\ \mu m$. A 3 times higher t_{Rise} for the device without the AlGaN cap is the result of thinner oxide and channel layers, which leads to much higher $C_{GS,max}$, $2.0\ pF/mm$, compared to $0.3\ pF/mm$ for the device with AlGaN cap. $C_{DS,max}$ for the two devices remains $\sim 1.5\ pF/mm$, higher than $C_{GS,max}$ in the device with AlGaN cap, owing to the parasitic

capacitance introduced by the underlying 2DEG, which is estimated to be $\sim 1.23\ pF/mm$ from the simulation of C_{DS} at different thickness of AlGaN barrier t_b, as illustrated in Fig. 5.5 (c). Assuming both p-channel and n-channel have similar rise and fall times at W_n/W_p of $1/10$, the switching speed f_{sw} of the inverter described as:

$$f_{sw} = (t_{Rise} + t_{Fall})^{-1} \approx (2 \cdot t_{Rise})^{-1} \quad (2)$$

yields a value of $\sim 625\ MHz$ for a C_L corresponding to a fanout of 5.

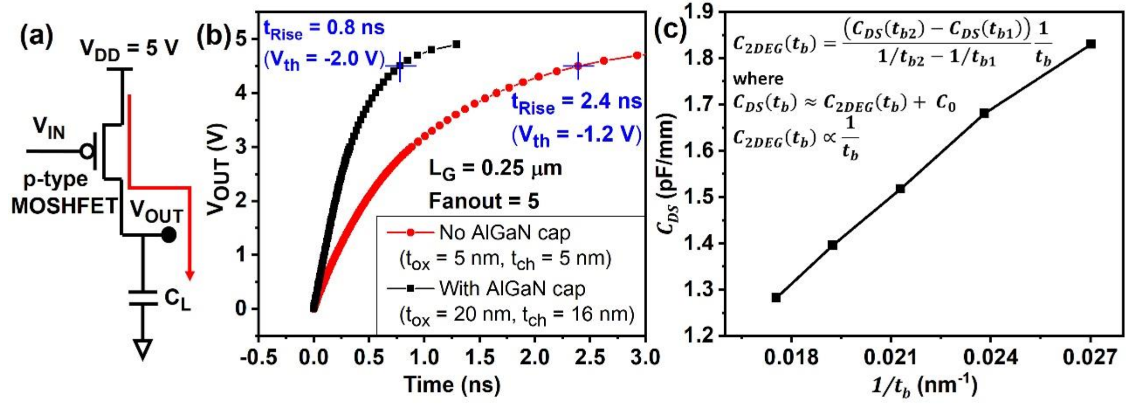

Fig. 5.5. (a) Circuit diagram for calculating the rise time, (b) Output voltage or variation of the load voltage in devices without and with AlGaN cap *vs.* time as the input voltage is switched from $5\ V$ to $0\ V$ at $t = 0$, (c) drain-to-source capacitance (C_{DS}) vs. inverse of the AlGaN barrier thickness (t_b^{-1}) for the extraction of the capacitance contributed by the 2DEG (C_{2DEG}) to the C_{DS}.

Compared to a t_{Rise} of $670\ ns$, reported by R. Chu *et al.* [7] for their fabricated p-channel device, a significantly smaller t_{Rise} is the result of much smaller on-resistance (R_{on}) and load capacitor of $143\ \Omega \cdot mm$ and $3.3\ pF/mm$ compared to their values of $1314\ \Omega \cdot mm$ and C_L estimated $\approx T_{Rise}/2.2R_{on} = 231\ pF/mm$, respectively from their work. Our smaller on-resistance is the result of higher on-current facilitated by lower access resistances and depletion beneath the channel, facilitated by the AlGaN cap. If their value of C_L of $231\ pF/mm$ were employed, the corresponding rise time is predicted to be $56\ ns$, an improvement of at least a factor of 10 in switching speed.

5.4. Impact of Channel Thickness on the Performance of an E-Mode p-Channel MOSHFET in GaN

The transfer characteristics of a p-channel device with grounded 2DEG, at different channel thicknesses, t_{ch}, are displayed in Fig. 5.6 (a). Here, x_{cap} is adjusted such that the threshold voltage remains at $-2\ V$ irrespective of t_{ch}, as shown in the inset. An increase in x_{cap} is required at higher t_{ch}, which reduces the density of 2DHG under the gate and leads to reduction in the on-state current $|I_{ON}|$ from its maximum value of $35\ mA/mm$, as shown in the inset (Fig. 5.6 (a)). Moreover, the off-state current $|I_{OFF}|$ ($|I_{DS}|$ at $V_{GS} = 0, V_{DS} = -5\ V$) at zero gate bias in the transfer characteristics shows an increase by orders of magnitude with increase in t_{ch}.

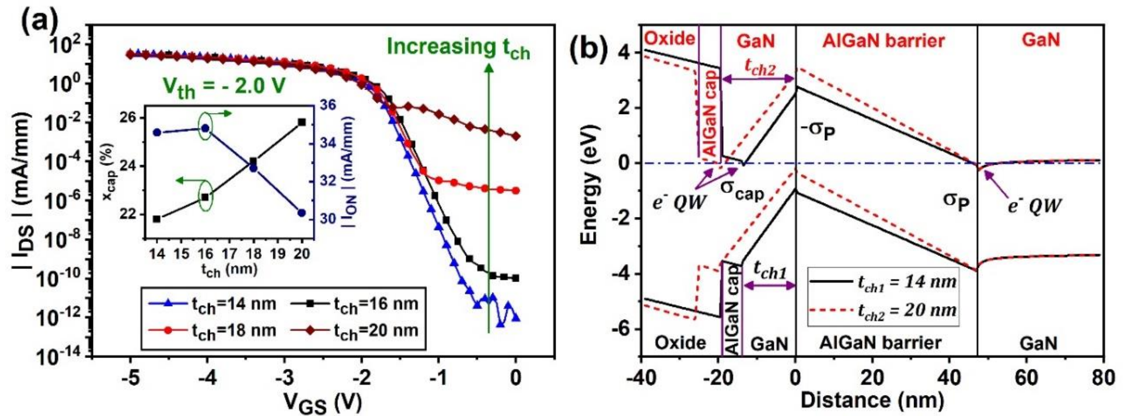

Fig. 5.6. (a) Comparison of the simulated transfer characteristics with a variation in thickness of the GaN channel at a fixed threshold voltage of $-2\ V$ for a p-channel AlGaN capped device with grounded 2DEG. The inset shows the Al mole fraction in the AlGaN cap layer x_{cap} required to maintain the V_{th} at $-2\ V$ for different t_{ch} and the corresponding on-current. (b) Simulated Band diagrams at two different thicknesses of GaN channel.

This behaviour can be understood by analysing the band diagrams at two different thicknesses of channel layer, as shown in Fig. 5.6 (b). For a thinner channel ($14\ nm$), the band bending introduced by σ_{cap} adequately maintains the valence band at the interface of the GaN channel and AlGaN barrier layer sufficiently below the Fermi level, resulting in a depletion of holes along this interface. However, for a thicker channel, an additional

e^{-} QW develops at the top interface of the GaN channel, where an increase in x_{cap} no longer has any impact in further lowering the valence band in the channel. Thus as the channel layer becomes thicker, the valence band at the GaN and AlGaN barrier interface comes close to the Fermi level as shown in the figure for $t_{ch} = 20\ nm$. This leads to a finite density of holes at this interface, responsible for an increase in the off-state current. A channel thickness of $\leq 20nm$ is also reported by F. J Kub *et al.* [20] for preventing the simultaneous formation of both hole and e^{-} QW, providing a further validation of our model. Owing to this mechanism, the device produces an ideal on/off ratio of 10^{11} for thicknesses of the channel layer $< 18\ nm$. This channel thickness sets a limit upon its manufacturability, arising from the difficulty in controlling the diffusion of Mg ions [25] from the doped p-GaN layer that is required to form the ohmic contacts to the source and drain. The presence of the diffused Mg ions in the GaN channel layer would contribute to an increase in leakage current and mobility degradation from Coulomb scattering that are not accounted in these simulations, but would, in practise, make the device difficult to realise. Moreover, achieving a precise channel thickness via etching is also not preferable due to the difficulty in reliably reproducing etching depth with uniform surface [26], [27].

As a solution to the increasing leakage current with the thicker channel, we modify the present device geometry following the work of Nakajima *et al.* [1], as shown in Fig. 5.7, which features an additional contact for applying a suitable bias over the 2DEG. A biased 2DEG assists the AlGaN cap to effectively suppress the 2DHG under the gate, thereby reducing the off-state leakage in E-mode operation. As before, we consider a p-GaN/GaN/AlGaN/GaN stack as the baseline heterostructure that, from top to bottom (along $[000\bar{1}]$), consists of $20\ nm$ Mg-doped p-GaN, $20\ nm$ undoped GaN, $47\ nm$ AlGaN barrier with Al mole fraction of 23%, and a $1.5\ \mu m$ GaN buffer on a

substrate. Al_2O_3 is used as a gate oxide with a thickness of 20 nm, while the gate length L_G is kept fixed at 0.25 μm. The lengths of the access regions between source and gate L_{SG} and gate and drain L_{GD} are initially kept at 1 μm, unless specified otherwise.

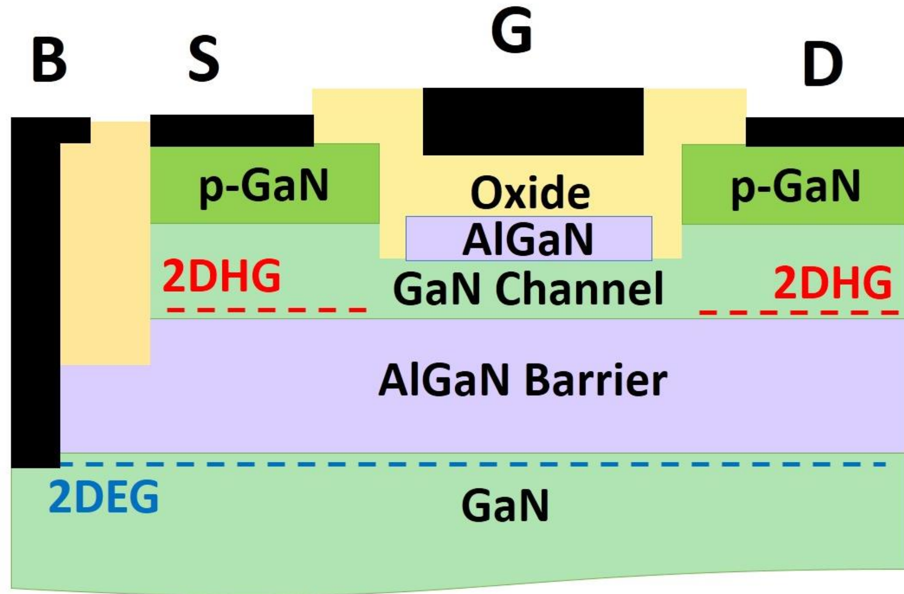

Fig. 5.7. Schematic of the modified p-channel E-mode device with AlGaN cap, where the 2DEG is biased via an additional base contact (marked B).

Our modified device with an additional base contact to the 2DEG overcomes the restrictions imposed by channel thickness. In the modified device, an application of a suitable potential to the underlying 2DEG, V_B can be used as an additional handle in modulating the density of the 2DHG in the channel across the AlGaN barrier. Since the technology to contact the 2DEG is already well established in commercial n-channel GaN devices, the present device is more favourable in terms of manufacturability. It clearly avoids the problems associated with the manufacturing of undoped GaN channel layers with overlying Mg doped contact regions to problematically small values ($<$ 18 nm). The transfer characteristics of this device as plotted in Fig. 5.8 reveal that $|I_{OFF}|$ can be suppressed with an increase in V_B, even with a thicker channel ($\approx$ 30 nm) and a lower x_{cap} (10 %). An increase in V_B helps lower the threshold voltage below zero, driving the device towards E-mode. However, the on-current of the device shows a sharp

decrease with V_B, dropping to $\sim 15\ mA/mm$, half of its original value, as V_{th} changes from $0\ V$ to $-2\ V$, as shown in the inset.

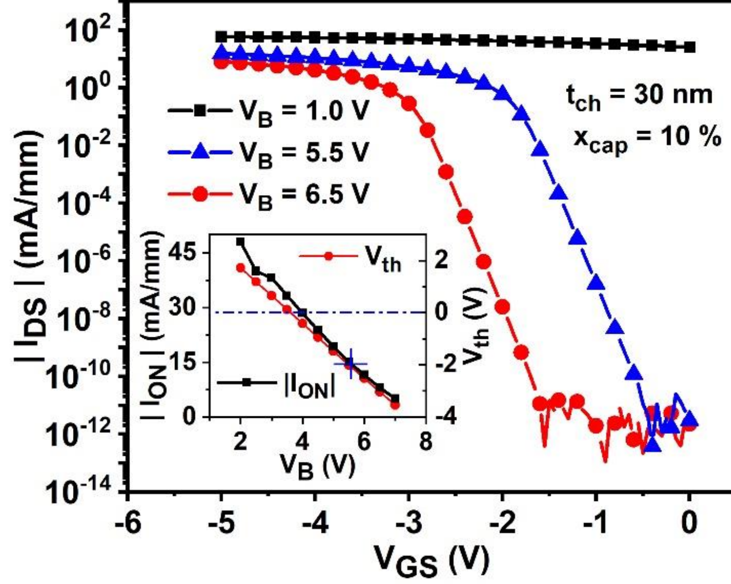

Fig. 5.8. Simulated transfer characteristics at different base to source bias V_B applied to the 2DEG in the modified device in Fig. 5.7 for 30 nm of channel thickness and 10 % of Al mole fraction in the AlGaN cap. The inset shows the corresponding on-current and threshold voltage behaviour with respect to V_B.

The high sensitivity of the on-current to V_B arises from a distinction in the way in which the density of the hole gas is affected by the biased 2DEG in comparison to the AlGaN cap. Figs. 5.9 (a) and (b) reveal the behaviour of the density of the 2DHG with respect to x_{cap} and V_B in different regions of the device. Since the AlGaN cap layer only resides under the gate, a change in x_{cap} only affects the density in the gate region, whereas the density in the access regions remains unaffected, as seen from Fig. 5.9 (a). A biased 2DEG behaves as a secondary gate for the 2DHG, which acts across the AlGaN barrier, thereby affecting the density of 2DHG in both channel and access regions, as observed in Fig. 5.9 (b). This reduction in the density of the 2DHG in the access region increases the resistance of the source to drain path, which results in the observed decrease in $|I_{ON}|$ with V_B.

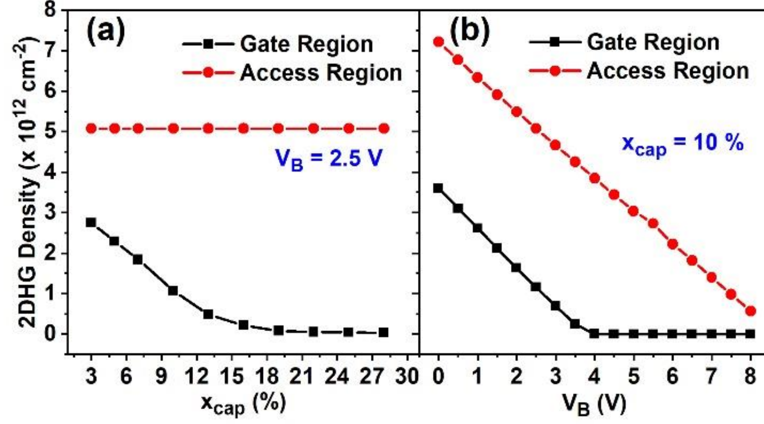

Fig. 5.9. The simulated density of 2DHG in the gate and access regions with respect to a change in (a) Al mole fraction in AlGaN cap x_{cap} and (b) base voltage V_B.

One way to reduce the sensitivity of $|I_{ON}|$ with V_B and lower the impact of resistance introduced by the access regions is to minimise the lengths of the access regions. Fig. 5.10 shows the transfer characteristics of an optimum device, where the lengths of both the access regions between the source and gate and gate and drain are kept at $300\ nm$.The inset shows a comparison of the transfer characteristics of this device with a change in trap charge density $\sigma_{cap/GaN}$ at the interface between the AlGaN cap and GaN channel. Owing to a reduction in the resistance of the access regions, the present device shows a maximum drain current of $28\ mA/mm$ at a $V_{th} = -2\ V$, which is almost double that achieved for a device with longer access regions ($L_{SG} = L_{GD} = 1\ \mu m$) in Fig. 5.8. Despite a thicker channel of $30\ nm$, the on-off current ratio of the device is maintained at 10^8 (black curve with square symbols in the inset), a 4 order of magnitude gain over a device utilising only an AlGaN cap and a thinner channel of $20\ nm$ (see Fig. 5.6). A higher on-state current is also the result of a higher x_{cap} and a lower V_B in contrast with the device in Fig. 5.8, where an x_{cap} of 10 % and V_B of 5.5 V is used for the same threshold voltage. A higher x_{cap} coupled with smaller V_B tends to favour the localised depletion of 2DHG under the gate rather than in the entire source to drain path. As shown in the inset, the trap density at the AlGaN cap/GaN channel needs to be kept at minimum such that the

variation in $\sigma_{cap/GaN}$ owing to the presence of traps is maintained well below $7 \times 10^{11} cm^{-2}$ to not significantly affect the device characteristics.

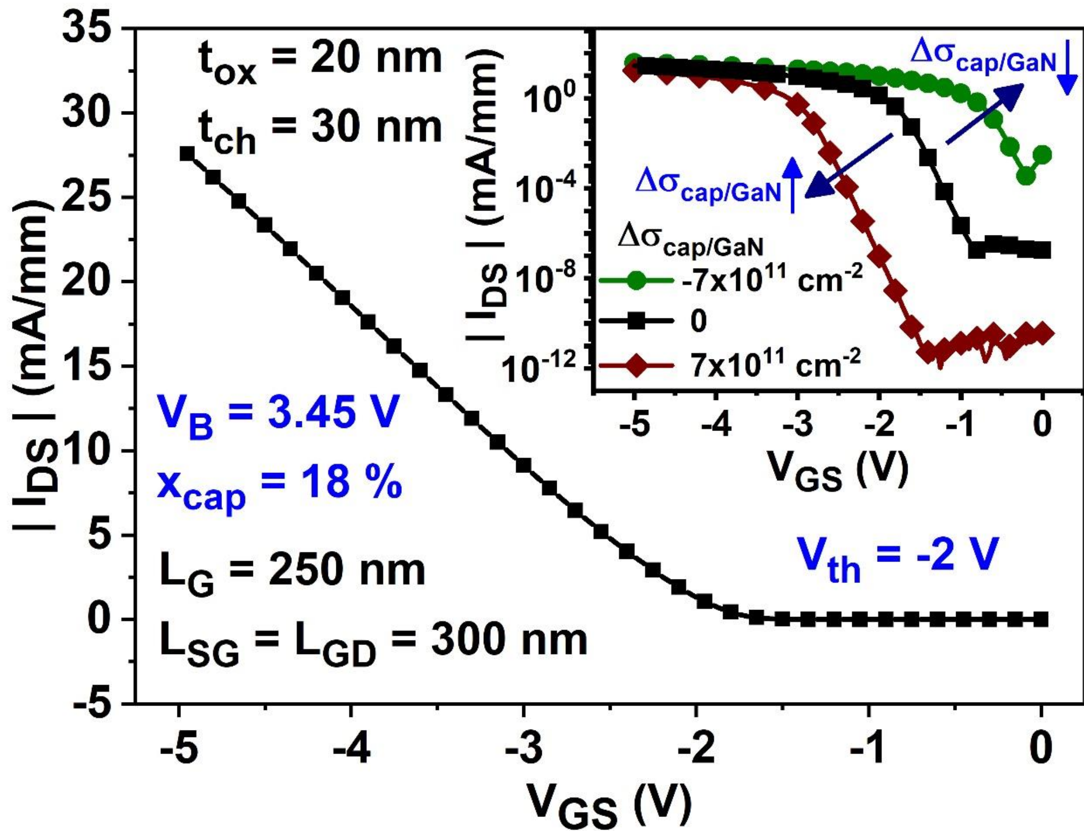

Fig. 5.10. The simulated transfer characteristics of an optimum device with a threshold voltage of $-2\ V$, featuring an AlGaN cap with Al mole fraction of 18 % at a potential of 3.45 V applied to the 2DEG. The inset shows the change in transfer characteristics due to a variation in trap charge at the interface between the regrown AlGaN cap and GaN channel.

5.5. SUMMARY

A low voltage p-channel E-mode GaN MOSHFET on a GaN/AlGaN/GaN platform suitable for integration with PSJ Power devices is investigated. The E-mode operation is realised using a thin AlGaN cap layer between the GaN channel with an underlying grounded or biased 2DEG and gate dielectric that suppresses the penetration of holes beneath the gate. The technique not only improves the on-current but also suppresses the leakage current, leading to orders of magnitude improvement in on-off ratio at short gate lengths. The simulated inverter offers promise of CMOS integrated gate drivers for MHz

switching of power conversion circuits in GaN.

In conclusion, we have discussed potential solutions for achieving an E-mode p-channel device in GaN, necessary for a CMOS based power convertor in a Power Management Integrated Circuit (PMIC). Our analysis reveals that the technology employing an AlGaN cap is best suited for realising E-mode operation with highest on-current, yet it suffers from a high off-state current as the thickness of the channel is increased to $20\,nm$. Introducing an additional contact bias to the 2DEG acts as a secondary gate for controlling the density of 2DHG in the channel and allows saturated characteristics of the device. This mechanism coupled with the AlGaN cap effectively eliminates the problem of higher off-state current observed at a thicker channel layer while still promising a higher on-current.

5.6. REFERENCES

[1] A. Nakajima, S. Kubota, K. Tsutsui, K. Kakushima, H. Wakabayashi, H. Iwai, S. Nishizawa, and H. Ohashi, "GaN-based complementary metal–oxide–semiconductor inverter with normally off Pch and Nch MOSFETs fabricated using polarisation-induced holes and electron channels," *IET Power Electron.*, vol. 11, no. 4, pp. 689–694, 2018. DOI: 10.1049/IET-PEL.2017.0376.

[2] A. Nakajima, Y. Sumida, M. H. Dhyani, H. Kawai, and E. M. Narayanan, "GaN-Based Super Heterojunction Field Effect Transistors Using the Polarization Junction Concept," *IEEE Electron Device Lett.*, vol. 32, no. 4, pp. 542–544, Apr. 2011. DOI: 10.1109/LED.2011.2105242.

[3] H. Hahn, B. Reuters, S. Geipel, M. Schauerte, F. Benkhelifa, O. Ambacher, H. Kalisch, and A. Vescan, "Charge balancing in GaN-based 2-D electron gas devices employing an additional 2-D hole gas and its influence on dynamic behaviour of GaN-based heterostructure field effect transistors," *J. Appl. Phys.*, vol. 117, no. 10, pp. 104508-1-104508–8, Mar. 2015. DOI: 10.1063/1.4913857.

[4] X. Chen, "Semiconductor power devices with alternating conductivity type high-voltage breakdown regions," U.S. Patent No. 5,216,275, Jun. 1993.

[5] H. Kawai, S. Yagi, S. Hirata, F. Nakamura, T. Saito, Y. Kamiyama, M. Yamamoto, H. Amano, V. Unni, and E. M. S. Narayanan, "Low cost high voltage GaN polarization

superjunction field effect transistors," *Phys. status solidi*, vol. 214, no. 8, p. 1600834, Aug. 2017. DOI: 10.1002/PSSA.201600834.

[6] A. Nakajima, S. Nishizawa, H. Ohashi, H. Yonezawa, K. Tsutsui, K. Kakushima, H. Wakabayashi, and H. Iwai, "One-chip operation of GaN-based P-channel and N-channel heterojunction field effect transistors," in *2014 IEEE 26th International Symposium on Power Semiconductor Devices & IC's (ISPSD)*, Jun. 2014, pp. 241–244. DOI: 10.1109/ISPSD.2014.6856021.

[7] R. Chu, Y. Cao, M. Chen, R. Li, and D. Zehnder, "An Experimental Demonstration of GaN CMOS Technology," *IEEE Electron Device Lett.*, vol. 37, no. 3, pp. 269–271, Mar. 2016. DOI: 10.1109/LED.2016.2515103.

[8] S. Yang, S. Huang, M. Schnee, Q.-T. Zhao, J. Schubert, and K. J. Chen, "Fabrication and Characterization of Enhancement-Mode High-κ LaLuO3-AlGaN/GaN MIS-HEMTs," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3040–3046, Oct. 2013. DOI: 10.1109/TED.2013.2277559.

[9] H. Hahn, B. Reuters, S. Kotzea, G. Lukens, S. Geipel, H. Kalisch, and A. Vescan, "First monolithic integration of GaN-based enhancement mode n-channel and p-channel heterostructure field effect transistors," in *72nd Device Research Conference*, Jun. 2014, vol. 60, no. 10, pp. 259–260. DOI: 10.1109/DRC.2014.6872396.

[10] W. Huang, Z. Li, T. P. Chow, Y. Niiyama, T. Nomura, and S. Yoshida, "Enhancement-mode GaN Hybrid MOS-HEMTs with $R_{on,sp}$ of 20 mΩ-cm^2," in *2008 20th International Symposium on Power Semiconductor Devices and IC's*, May 2008, pp. 295–298. DOI: 10.1109/ISPSD.2008.4538957.

[11] B. Lu, O. I. Saadat, and T. Palacios, "High-Performance Integrated Dual-Gate AlGaN/GaN Enhancement-Mode Transistor," *IEEE Electron Device Lett.*, vol. 31, no. 9, pp. 990–992, Sep. 2010. DOI: 10.1109/LED.2010.2055825.

[12] J. Wei, S. Liu, B. Li, X. Tang, Y. Lu, C. Liu, M. Hua, Z. Zhang, G. Tang, and K. J. Chen, "Low On-Resistance Normally-Off GaN Double-Channel Metal-Oxide-Semiconductor High-Electron-Mobility Transistor," *IEEE Electron Device Lett.*, vol. 36, no. 12, pp. 1287–1290, Dec. 2015. DOI: 10.1109/LED.2015.2489228.

[13] C.-T. Chang, T.-H. Hsu, E. Y. Chang, Y.-C. Chen, H.-D. Trinh, and K. J. Chen, "Normally-off operation AlGaN/GaN MOS-HEMT with high threshold voltage," *Electron. Lett.*, vol. 46, no. 18, pp. 1280–1281, Sep. 2010. DOI: 10.1049/EL.2010.1939.

[14] B. Zhang, S. Tan, J. Xu, Z. Dong, G. Yu, Y. Cai, L. Xue, H. Chen, K. Hou, D. Zhao, Y. Wang, S. Liu, and K. J. Chen, "5.3A/400V normally-off AlGaN/GaN-on-Si MOS-HEMT with high threshold voltage and large gate swing," *Electron. Lett.*, vol. 49, no. 3, pp. 221–222, Jan. 2013. DOI: 10.1049/EL.2012.3153.

[15] J. W. Roberts, P. R. Chalker, K. B. Lee, P. A. Houston, S. J. Cho, I. G. Thayne, I. Guiney,

D. Wallis, and C. J. Humphreys, “Control of threshold voltage in E-mode and D-mode GaN-on-Si metal-insulator-semiconductor heterostructure field effect transistors by in-situ fluorine doping of atomic layer deposition Al2O3 gate dielectrics,” *Appl. Phys. Lett.*, vol. 108, no. 7, pp. 072901-1-072901-5, Feb. 2016. DOI: 10.1063/1.4942093.

[16] S. Kubota, R. Kayanuma, A. Nakajima, S. Nishizawa, and H. Ohashi, “P-channel AlGaN/GaN MOSFETs for Normally-Off Operation,” in *Material Research Society*, Nov. 2015, p. RR1.02.

[17] H. Hahn, B. Reuters, A. Pooth, B. Hollander, M. Heuken, H. Kalisch, and A. Vescan, “p-Channel Enhancement and Depletion Mode GaN-Based HFETs With Quaternary Backbarriers,” *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3005–3011, Oct. 2013. DOI: 10.1109/TED.2013.2272330.

[18] B. Reuters, H. Hahn, A. Pooth, B. Holländer, U. Breuer, M. Heuken, H. Kalisch, and A. Vescan, “Fabrication of p-channel heterostructure field effect transistors with polarization-induced two-dimensional hole gases at metal–polar GaN/AlInGaN interfaces,” *J. Phys. D. Appl. Phys.*, vol. 47, no. 17, p. 175103, Apr. 2014. DOI: 10.1088/0022-3727/47/17/175103.

[19] A. Nakajima, S. Kubota, R. Kayanuma, K. Tsutsui, K. Kakushima, H. Wakabayashi, H. Iwai, S. Nishizawa, and H. Ohashi, “Monolithic Integration of GaN-based Normally-off P- and N-channel MOSFETs,” in *13th International Seminar on Power Semiconductors (ISPS’16)*, 2016.

[20] F. J. Kub, T. J. Anderson, A. D. Koehler, and K. D. Hobart, “Inverted p-channel III-nitride field effect transistor with hole carriers in the channel,” U.S. Patent No. 9,275,998, Aug. 2015.

[21] A. Kumar and M. M. De Souza, “Modelling the threshold voltage of p-channel enhancement-mode GaN heterostructure field-effect transistors,” *IET Power Electron.*, vol. 11, no. 4, pp. 675–680, Apr. 2018. DOI: 10.1049/IET-PEL.2017.0438.

[22] A. Kumar and M. M. De Souza, “An E-Mode p-Channel GaN MOSHFET for a CMOS Compatible PMIC,” *IEEE Electron Device Lett.*, vol. 38, no. 10, pp. 1449–1452, Oct. 2017. DOI: 10.1109/LED.2017.2747898.

[23] A. Nakajima, P. Liu, M. Ogura, T. Makino, K. Kakushima, S. Nishizawa, H. Ohashi, S. Yamasaki, and H. Iwai, “Generation and Transportation Mechanisms for Two-Dimensional Hole Gases in GaN/AlGaN/GaN Double Heterostructures,” *J. Appl. Phys.*, vol. 115, no. 15, p. 153707, Apr. 2014. DOI: 10.1063/1.4872242.

[24] A. Nakajima, M. H. Dhyani, E. M. S. Narayanan, Y. Sumida, and H. Kawai, “GaN based Super HFETs over 700V using the polarization junction concept,” in *2011 IEEE 23rd International Symposium on Power Semiconductor Devices and ICs*, May 2011, pp. 280–283. DOI: 10.1109/ISPSD.2011.5890845.

[25] I. P. Smorchkova, E. Haus, B. Heying, P. Kozodoy, P. Fini, J. P. Ibbetson, S. Keller, S. P. DenBaars, J. S. Speck, and U. K. Mishra, “Mg doping of GaN layers grown by plasma-assisted molecular-beam epitaxy,” *Appl. Phys. Lett.*, vol. 76, no. 6, pp. 718–720, Feb. 2000. DOI: 10.1063/1.125872.

[26] Bin Lu, Min Sun, and T. Palacios, “An Etch-Stop Barrier Structure for GaN High-Electron-Mobility Transistors,” *IEEE Electron Device Lett.*, vol. 34, no. 3, pp. 369–371, Mar. 2013. DOI: 10.1109/LED.2012.2237374.

[27] Y. Ohmaki, M. Tanimoto, S. Akamatsu, and T. Mukai, “Enhancement-Mode AlGaN/AlN/GaN High Electron Mobility Transistor with Low On-State Resistance and High Breakdown Voltage,” *Jpn. J. Appl. Phys.*, vol. 45, no. No. 44, pp. L1168–L1170, Nov. 2006. DOI: 10.1143/JJAP.45.L1168.

Chapter 6 A Non-ambipolar p-channel GaN Heterostructure Tunnel FET with high on/off ratio

An alternate mechanism to achieve a non-ambipolar Tunnel FET (TFET) is proposed in this chapter. The method relies on polarisation charge induced in semiconductors, such as group III nitrides, to enhance the electric field across the junction and facilitate unidirectional tunneling based on polarity of applied gate bias. This also enables enhanced control over the tunneling distance, reducing it significantly in comparison to a conventional tunnel FET.

6.1. INTRODUCTION

Increasing attention is being divested currently in low resistance tunnel junctions in III-nitrides in order to improve the efficiency of visible and ultraviolet light-emitting diodes (LEDs) [1]–[3] by elimination of p-type contacts in GaN [4]–[6]. Forming a tunnel junction in GaN with a low tunnel resistance is challenging, in part due to the large band gap that increases the tunneling barrier height and electric field required to produce sharp band bending. An increasing diffusion of Mg ions at high temperature [7] and a large activation energy of $174\,meV$ [8] also make it difficult to obtain degenerately doped p-type GaN, necessary to form a tunnel junction with abrupt band bending. Therefore, a thin layer of either AlN [9], [10], InGaN [11]–[13] or InN [14] is sandwiched between p- and n- type GaN regions to introduce additional polarisation charge at each of its interfaces to raise the electric field between the p- and n- type regions, thereby facilitating tunneling. This type of tunnel junction which is aided by the polarisation charge is referred as polarisation-induced tunneling junction (PITJ) [10].

PITJ with a thin InN in a novel n-channel tunnel FET (TFET) in GaN, has shown promise of an on-current of $60\,mA/mm$ in the simulated fin geometry and a SS of

$\sim 20\ mV/dec$ with an ON/OFF current ratio ~ 5 orders of magnitude in a sidewall-gated cylindrical geometry [14]. In another TCAD based simulation study an inline-gated rectangular TFET with InN based PITJ demonstrated an on-current of 73 mA/mm with a SS of 15 mV/dec, and an ON/OFF ratio of 5 orders of magnitude [15].

Recent progress in p-type doping in excess of $10^{20} cm^{-3}$ facilitated by low temperature MBE growth has led to demonstration of a direct tunnel junction between degenerately doped p- and n-type GaN [6], [16]. This device achieved a differential resistivity of $1 \times 10^{-5} \Omega\ cm^2$ [16], an order of magnitude lower than the lowest reported resistivity in a PITJ using $In_{0.25}Ga_{0.75}N$ [13]. Based on this study the realisation of GaN based TFETs without PITJs, can also be envisioned. In this chapter however, we focus solely upon analysis of TFETs utilising PITJ for facilitating transport, and highlight its unique characteristics compared to conventional TFETs.

Conventional TFETs suffer from poor on-current, because the tunneling mechanism introduces an additional resistance in the source-drain path relative to a MOSFET. To date, no one has yet demonstrated a TFET of comparable current level to a MOSFET with subthreshold slope (SS) below $60\ mV/dec$ [17]. The best reported electrical characteristics were achieved in a vertical nanowire InAs/GaAsSb/GaSb TFET, which showed an ON-current of $0.31\ mA/mm$ at $60\ mV/dec$ of SS [18]. At a minimum SS of $48\ mV/dec$ the maximum current degraded to $67\ nA/\mu m$ in this device. It is well known that conventional TFETs suffer from ambipolarity which results in high off-current [19] and limits their applicability in complementary circuits [20]. To address ambipolarity, short-gated TFET [21], asymmetric doping, and band gap engineering [22], have been proposed.

In this chapter, a p-channel heterostructure tunnel FET (HTFET), utilising a thin layer of AlN as a PITJ, is introduced. Despite the larger band gap of AlN which results in

higher tunneling resistance in comparison to InGaN or InN, a thin layer of AlN is adopted in this work [5]. A significant lattice mismatch between GaN and InN $> 10\%$ [23] results in strain that can introduce challenges to the growth of InN or InGaN on GaN. In comparison, a lattice mismatch $< 2.5\ \%$ between GaN and AlN [23] implies that up to 5 nm of fully strained AlN can be grown on GaN without the introduction of microcracks [24].

6.2. MODELLING TUNNELING TRANSPORT

All results are obtained using Silvaco TCAD [25], where the inbuilt non-local band-to-band tunneling (BBT) model along with III-nitride specific field dependent mobility model [26], [27], Shockley-Read-Hall, and Augur recombination are selected for the tunneling current and device electrical characteristics. Unlike the local tunneling models, where the tunneling rate at each point is calculated from the localised value of electric field, a non-local BBT model that includes a local variation of energy bands is employed in the interests of accuracy [27]. In all simulations, the maximum hole mobility is limited to $16\ cm^2/Vs$ [28], while an activation energy of $174\ meV$ is used for acceptor dopants, consistent with the reported activation energy of Mg in GaN.

In conventional tunneling devices, such as Zener diodes in Si, high band bending is achieved via two degenerately doped regions located adjacently, facilitating carrier tunneling through the energy band gap. Fig. 6.1 (a) and the inset therein show the simulated energy band diagrams for a degenerately doped p-n junction in GaN. The depletion width at the junction in this case, is more than $10\ nm$, which greatly suppresses band to band tunneling of carriers on either side. To overcome this, a thin layer of AlN is sandwiched between the p- and n- type regions (inset Fig. 6.1 (b)), which introduces polarisation charge σ_P at each of its interfaces with GaN. This results in a high electric field across AlN ($\sim 12\ MV/cm$ [10]), thereby providing a sharp band bending to enable

band-to-band tunneling, as observed in the band diagram Fig. 6.1 (b). This mechanism has been utilized to implement tunnel diodes and light emitting diodes [9]–[11].

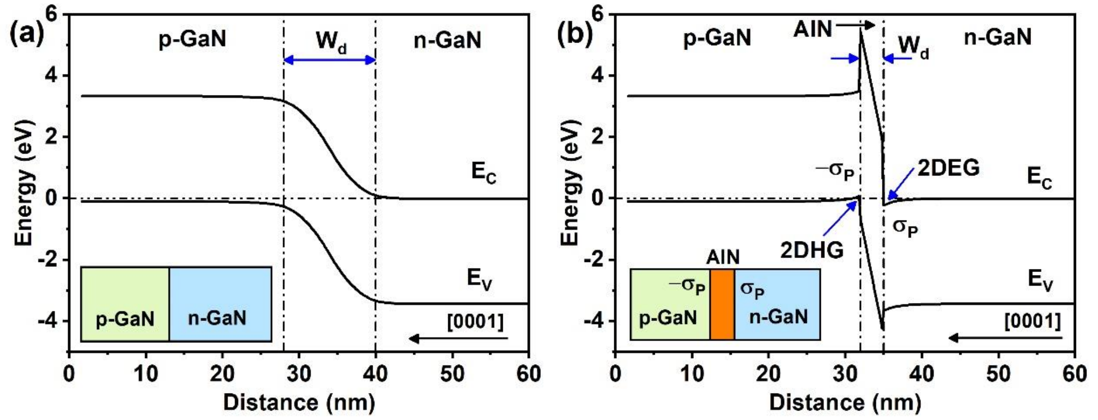

Fig. 6.1. Simulated energy band diagram of (a) a vertical p-n junction in GaN (inset) and (b) p-n junction with AlN barrier (inset). The polarisation charge at the AlN/GaN interface helps reduce the depletion width to facilitate tunneling.

The tunneling rate via the non-local BBT model is benchmarked by adjusting the effective electron tunnel mass m_e and hole tunnel mass m_h, using reported I-V data for a $56 \times 56\, \mu m^2$ GaN tunnel diode with a 2.8 nm AlN barrier and Ni/Au and Ti/Au ohmic contacts for p- and n- GaN, shown in Fig. 6.2 (a) from [10]. This device showed a total specific resistivity (including the tunnel resistance) of $\sim 0.14\ \Omega\ cm^2$. The effective masses for this set of simulations is $m_e = 0.2$ and $m_h = 1.0$ for GaN and $m_e = 0.314$ and $m_h = 0.69$ for AlN, in agreement with reported values for wurtzite GaN and AlN [23], [29]. Fig. 6.2 (b) shows the simulated I-V results for different contact resistivity values of the p-GaN contact. A good match between the model and experimental results is achieved with a contact resistivity anywhere between $10^{-2} - 10^{-1} \Omega\, cm^2$, which agree with contact resistivities in the range of $10^{-4} - 10^{-1} \Omega\, cm^2$ for Ni/Au [30], [31]. Since contacts to p-GaN, with ρ_c as low as $10^{-6} \Omega \cdot cm^2$ have been realised with a proper choice of metal stack, as shown in Fig. 4.4 of Chapter 4, we optimistically employ $10^{-6}\ \Omega\ cm^2$ as the contact resistance in all the simulations of p-channel HTFET.

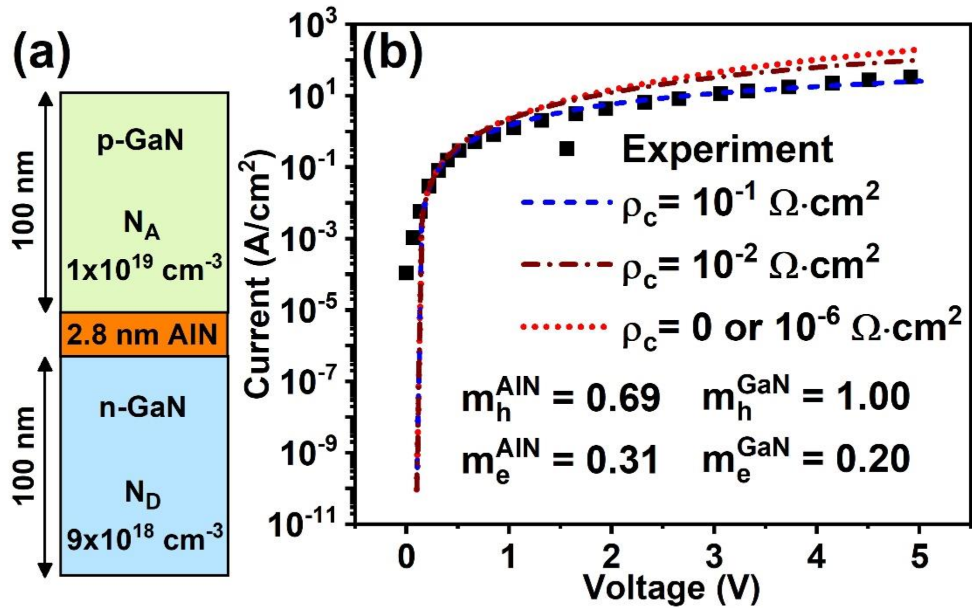

Fig. 6.2. (a) Schematic of a $56 \times 56\, \mu m^2$ GaN Zener diode with a 2.8 nm AlN barrier layer sandwiched between p-GaN and n-GaN. (b) Comparison of our simulation model with the reported experiment data reported from [10] (Reused data from Fig. 3 (a) with permission from [10] Copyright (2009) by the American Physical Society).

6.3. Non-ambipolar Operation of P-Channel GaN HTFET

Fig. 6.3 (a) shows a schematic diagram of the p-channel GaN heterostructure tunnel FET (HTFET), with its vertical direction along [0001]. From the bottom, the structure consists of a 56 nm n-GaN source, 2 nm AlN tunneling barrier, 15 nm undoped GaN (u-GaN) channel and 27 nm p-GaN. The energy of carriers in the u-GaN channel is modulated by a 2 nm Al_2O_3 separated gate, either in rectangular geometry with double gate or cylindrical geometry with gate-all-around. Unless stated otherwise, the width of the device in either rectangular or cylindrical geometry is kept at 10 nm, in-line with the minimum reported GaN nanowire widths of 14 nm or 10 nm reported in experiment [32], [33]. As shown in the corresponding band diagram in Fig. 6.3 (b), the u-GaN acts as channel and maintains the valence band sufficiently lower than both the hole quasi fermi level ($h^+\ QFL$) as well as the conduction band in the n-GaN, thus preventing the tunneling of carriers when the gate bias is zero.

A negative gate bias, raises the energy of the bands in the channel, moving the valence band closer to the hole quasi fermi level (h^+ QFL), as shown in Fig. 6.3 (c), which leads to an increase in hole concentration. At sufficiently large negative gate bias, the valence band in the channel aligns with the conduction band of n-GaN, hence enabling tunneling across the AlN barrier, as indicated by the arrow in Fig. 6.3 (c) and turning the device on. On the other hand, a positive gate bias reduces the energy levels of the conduction and valence bands in the u-GaN channel, as shown in Fig. 6.3 (d). However, since no AlN layer is present at the interface between p-GaN and u-GaN, the band bending between p-GaN and u-GaN occurs over a large distance, which greatly suppresses the tunneling current. Thus the device is maintained in the off-state.

The drain to source current I_{DS} with respect to V_{GS} for a rectangular or fin geometry is plotted in Fig. 6.3 (e) for a device or channel width of 10 nm. In contrast to the n-channel GaN HTFET reported in [14] where the channel is also doped, utilisation of u-GaN as a channel layer reduces the leakage by 10 orders of magnitude. However, the bias requirement of this device also increases to raise the energy of the valence band for alignment with the conduction band across the AlN layer. A lightly doped channel could also be employed to reduce the operating bias of this device. As can be observed, the drain current remains orders of magnitude lower at positive gate bias than at negative gate bias, thus confirming non-ambipolar behaviour, as indicated by the band diagrams (Fig. 6.3 (d)). Owing to the wide band gap nature of GaN, the off-current of the device remains much lower at $|10^{-14}|$ mA/mm even for a small channel length of 15 nm. A large band gap of AlN however, also introduces a large tunneling barrier height, which makes it difficult for the charge carriers to tunnel across the AlN. Hence the maximum drain current or on-current remains limited to 0.5 mA/mm in a fin geometry.

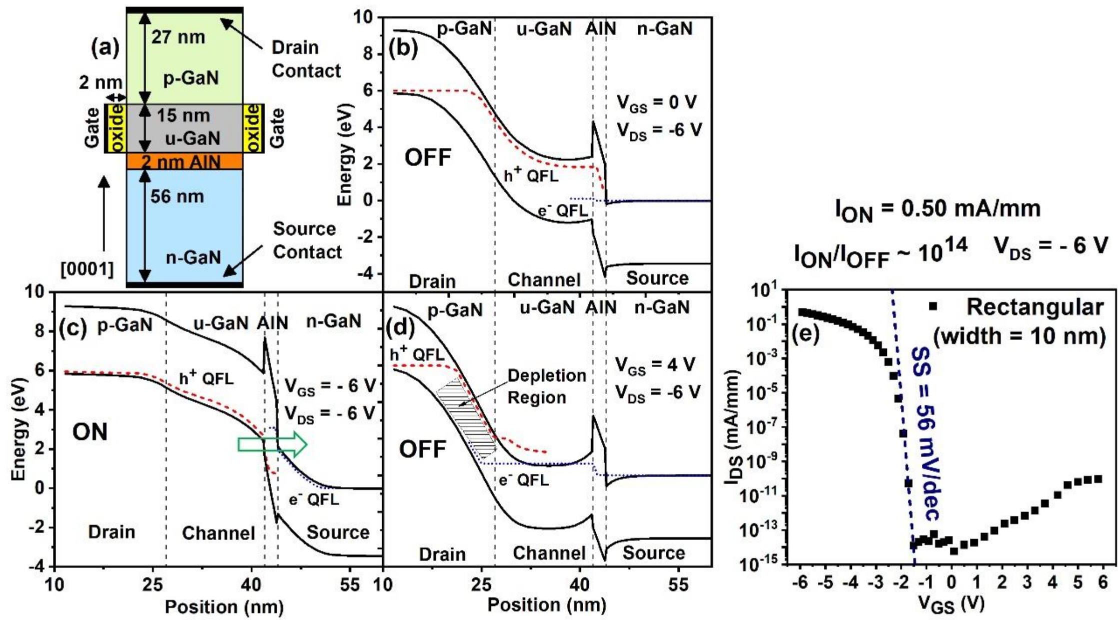

Fig. 6.3. (a) Schematic diagram of a p-channel GaN heterojunction tunnel FET (HTFET), and its simulated band diagrams along $[000\bar{1}]$ (b) at zero gate bias (off-state), (c) negative gate bias (on-state) and (d) positive gate bias (off-state), and (e) transfer characteristics showing non-ambipolar behaviour, similar to a p-channel MOSFET.

6.4. Optimised Cylindrical P-Channel GaN HTFET

The most common technique to improve the on-current in TFETs is to introduce a highly doped pocket of opposite polarity in the vicinity of the source edge of the channel to enhance the electric field across the tunneling junction [34], [35]. Moreover, a better electrostatic gate control is expected in cylindrical or nanowire geometry. Hence, in this section, we analyse the electrical characteristics of an optimised cylindrical GaN HTFET, which utilises a thin ($\sim 2\ nm$) and highly doped ($N_A = 3 \times 10^{19} cm^{-3}$) pocket at the interface between channel and an AlN barrier of 1.7 nm thickness of GaN HTFET, as shown in Fig. 6.4, while rest of the dimensions are kept same as that for the device in Fig. 6.3 (a).

The electrical characteristics of the p-channel GaN HTFET are presented in Figs. 6.4 (a) and (b), respectively. The current is normalised to the diameter of the cylindrical geometry. Owing to the thin p-GaN pocket, the maximum drain on-current $|I_{ON}|$ in Fig.

6.4 (a) is more than double in comparison to a rectangular device without the pocket (Fig. 6.3 (e)). An improved gate control in the cylindrical geometry also leads to a much steeper subthreshold slope (SS) of $32\ mV/dec$, in the absence of defect or trap states. In the absence of the thin AlN layer at the top edge of the gate, a positive gate bias alone is insufficient to produce a large band bending at this interface, hence the device continues to remain non-ambipolar. In Fig. 6.4 (b), it can be noted that a higher $|V_{DS}|$ is required to turn-on the device as $|V_{GS}|$ is increased. This is because a high $|V_{GS}|$ not only raises the energy of the valence band in the channel but also increases the energy of the conduction band in n-GaN across the AlN barrier layer (Fig. 6.3 (c)), thus requiring a higher $|V_{DS}|$ to align the bands to turn the device on.

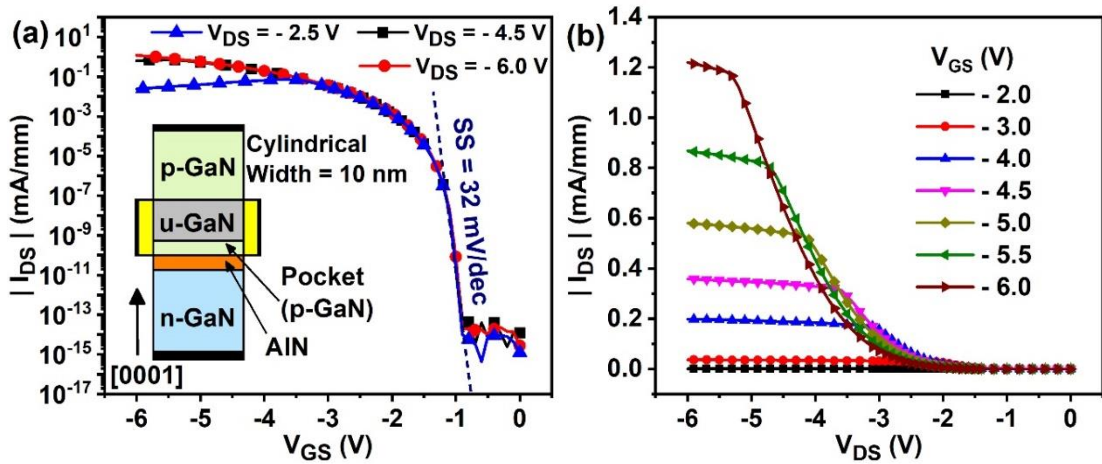

Fig. 6.4. Optimised (a) $I_{DS} - V_{GS}$ and (b) $I_{DS} - V_{DS}$ characteristics for the cylindrical p-channel GaN HTFET with a 2 nm pocket and 1.7 nm AlN barrier layer.

A further increase in $|I_{ON}|$ can be achieved by increasing the device width W, as shown in Fig. 6.5. However, this increase comes at the cost of increase in SS and leakage current, which arises from an inability of the gate to maintain the same potential across a wider channel. For a channel width greater than $22\ nm$, the device begins to conduct even at zero gate bias, resulting in a reduction in I_{ON}/I_{OFF} and an increase in SS above $60\ mV/dec$.

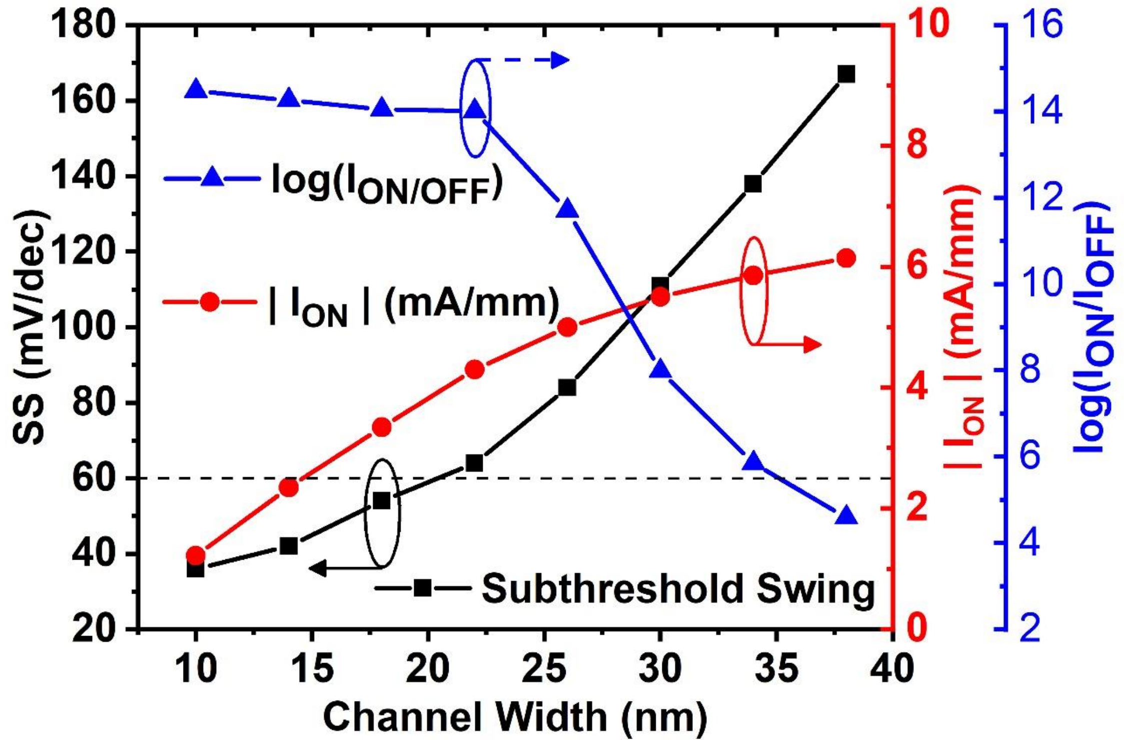

Fig. 6.5. Variations of $|I_{ON}|$, SS and $log(I_{ON}/I_{OFF})$ with respect to device width.

To analyse the sensitivity of the transfer characteristics to the mobility of holes μ_h, the transfer characteristics at different μ_h are investigated in Fig. 6.6, where $14.6\ cm^2/Vs$ corresponds to the default value for the hole mobility. As expected the drain current shows a proportional relationship with a change in μ_h. However, as can be inferred from the inset of this figure, with an order of magnitude change in μ_h, the variation in drain current remains limited to $\sim 10 - 20\%$. This relative insensitivity of the drain current to the hole mobility arises due to the presence of tunneling mechanism in TFETs, which, unlike MOSFETs, introduces an additional resistance R_{tunnel} in series with the channel resistance $R_{channel}$. R_{tunnel}, which is strongly dependent upon the tunneling masses for electrons and holes, plays a dominant role in the determination of the drain current.

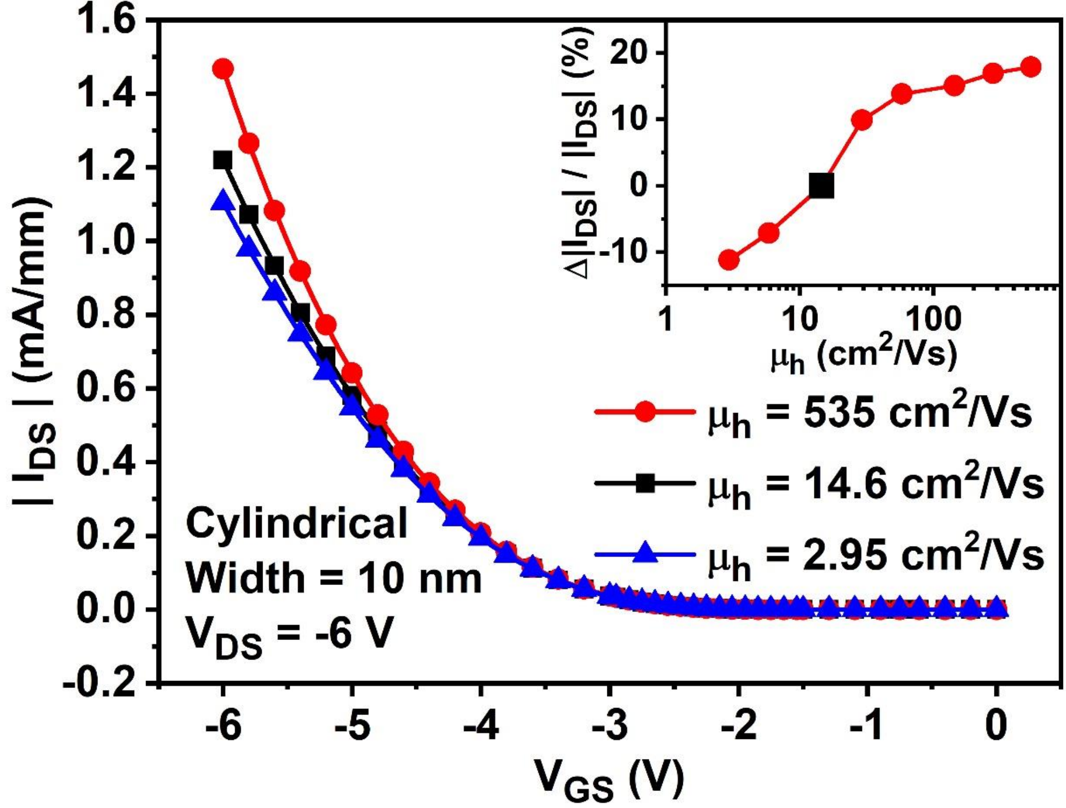

Fig. 6.6. Sensitivity of the simulated transfer characteristics to the mobility of holes μ_h in the cylindrical p-channel HTFET. Inset shows the relative variation in the drain current with μ_h.

Fig. 6.7 (a) shows how the different regions in a p-channel HTFET contribute to the total on-resistance, R_{ON} $(= V_{DS}/|I_{ON}|)$, of the device. To determine the value of the tunnel resistance of an optimised cylindrical device (Fig. 6.4 (a)), R_{ON} is plotted as a function of gate to drain length L_{GD} and channel length L_G, in Figs. 6.7 (b) and (c), respectively.

The contribution of the drain resistance R_{drain} to R_{ON} from the slope of R_{ON} vs. L_{GD} in Fig. 6.7 (b), yields an extracted R_{drain} for an L_{GD} of 27 nm, of $71.4\ \Omega\ mm$. Similarly the channel resistance $R_{channel}$ obtained from the slope of R_{ON} vs. L_G is $\sim 913\ \Omega\ mm$ at $L_G = 15\ nm$. Owing to a high electron mobility ($\sim 800\ cm^2/V \cdot s$) in comparison to the hole mobility ($\sim 16\ cm^2/V\ s$) in GaN, the contribution of the source resistance, R_{source}, is negligible in the present case. Therefore, R_{tunnel} is simply obtained as $R_{ON} - R_{drain} - R_{channel}$, which for an AlN barrier of 1.7 nm results in $\sim 3.93\ k\Omega\ mm$, corresponding to

a specific resistivity of $\sim 3.09 \times 10^{-4}\, \Omega\, cm^2$, for this cylindrical device, which is comparable to the best value for the tunnel resistivity of $1.2 \times 10^{-4} \Omega\, cm^2$ in a polarisation induced tunnel diodes reported for GaN/InGaN/GaN hetero-tunnel junction [13].

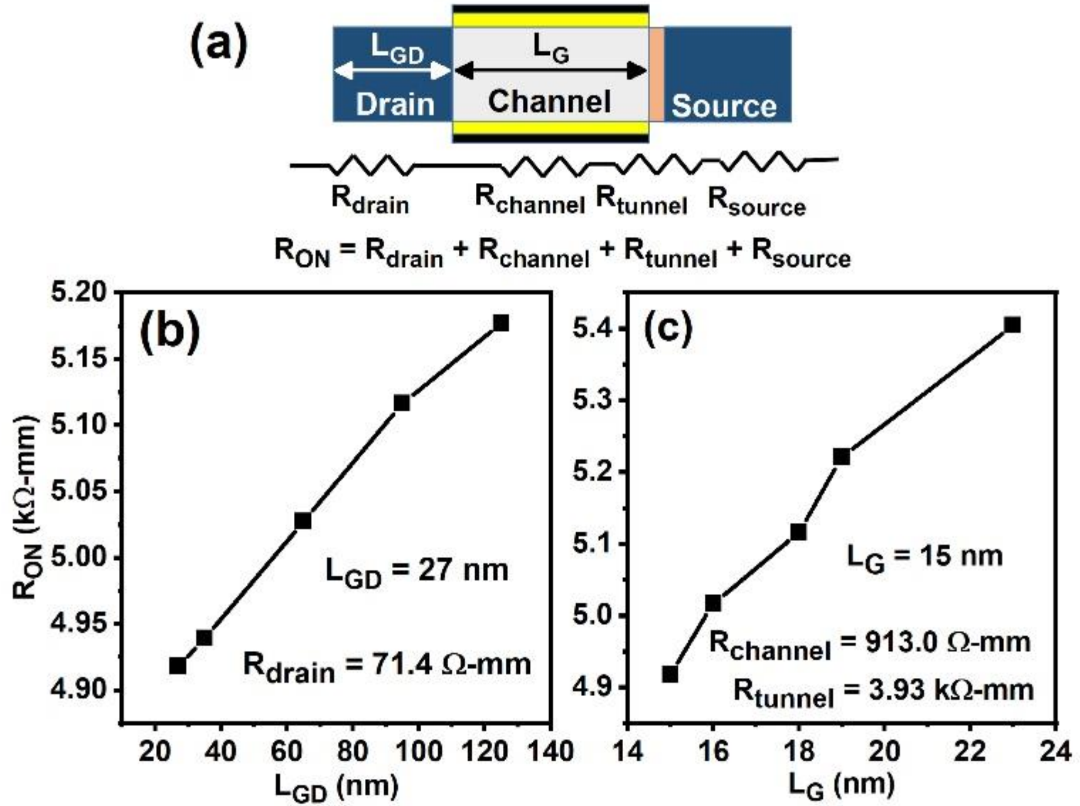

Fig. 6.7. (a) Contribution of different regions to the total on-resistance (R_{ON}) of the device. Variation of on-resistance with respect to (b) channel length and (c) gate to drain length, where the gate to source length and the device width are kept fixed at 56 nm and 10 nm, respectively.

6.5. ANALYSIS OF TUNNEL DISTANCE

To contrast the operation of the PITJ HTFET from a conventional TFET, employing group IV semiconductor such as Si, in Figs. 6.8 (a) and (b), the band diagrams during the OFF and ON states are compared with a conventional double gated p-i-n TFET in Si. The figures indicate the tunnel distance, defined as the minimum horizontal distance between the valence and conductance bands. In Fig. 6.8 (a), with an increase of gate bias in a silicon TFET, the tunnel distance reduces from 6.1 nm to 3.5 nm as the device

switches from OFF to ON. However as the tunnel distance gets smaller, the tunneling region also moves away from the gated channel region therefore resulting in a weaker gate control.

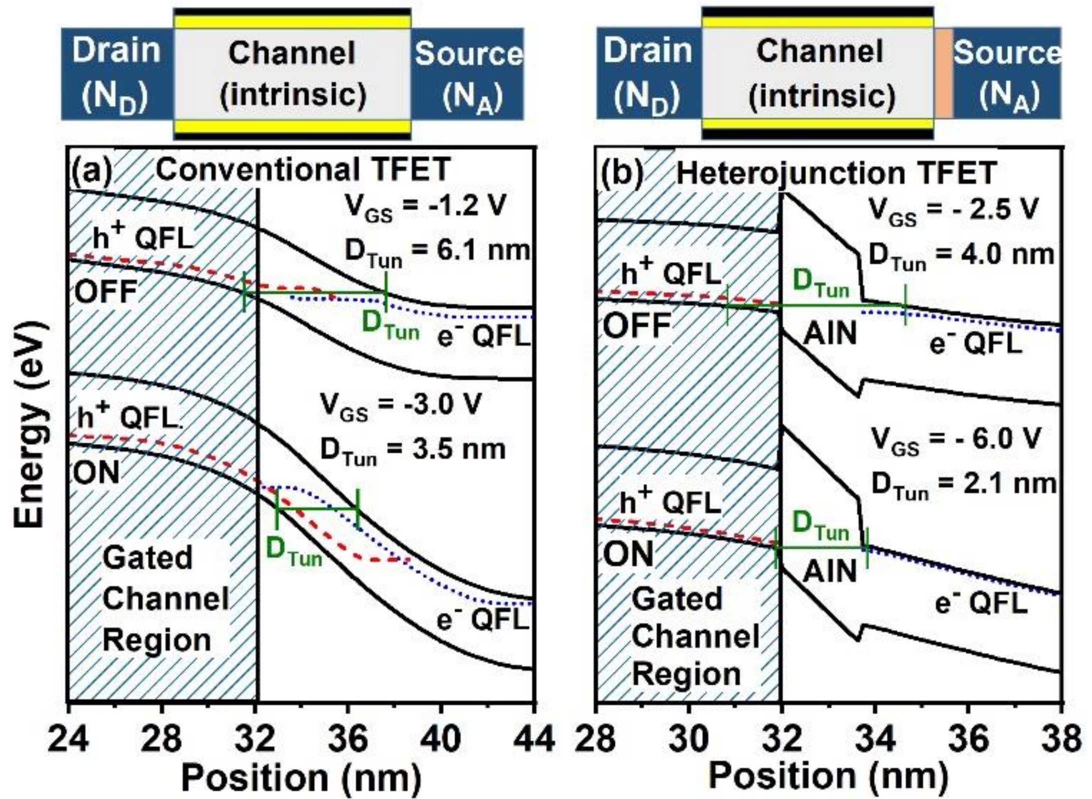

Fig. 6.8. Comparison of the band diagrams in ON- and OFF- states of a (a) conventional TFET on Si and (b) a heterojunction TFET on GaN.

In the case of an HTFET in Fig. 6.8 (b), since tunneling occurs only across the AlN barrier layer, the location of the tunneling region does not depend upon the value of gate bias. Therefore, a better control over the tunneling region is achieved resulting in a smaller tunnel distance than is possible in a conventional TFET.

To further highlight the distinction in operation, the transfer characteristics and tunneling distances of the two devices are compared in Fig. 6.9. Due to a large bandgap even though the maximum on-current is smaller, a wider band gap in GaN as well as a better control of the tunneling distance, limited only by the thickness of the tunnel barrier, lead to a higher ON/OFF current ratio and a steeper SS.

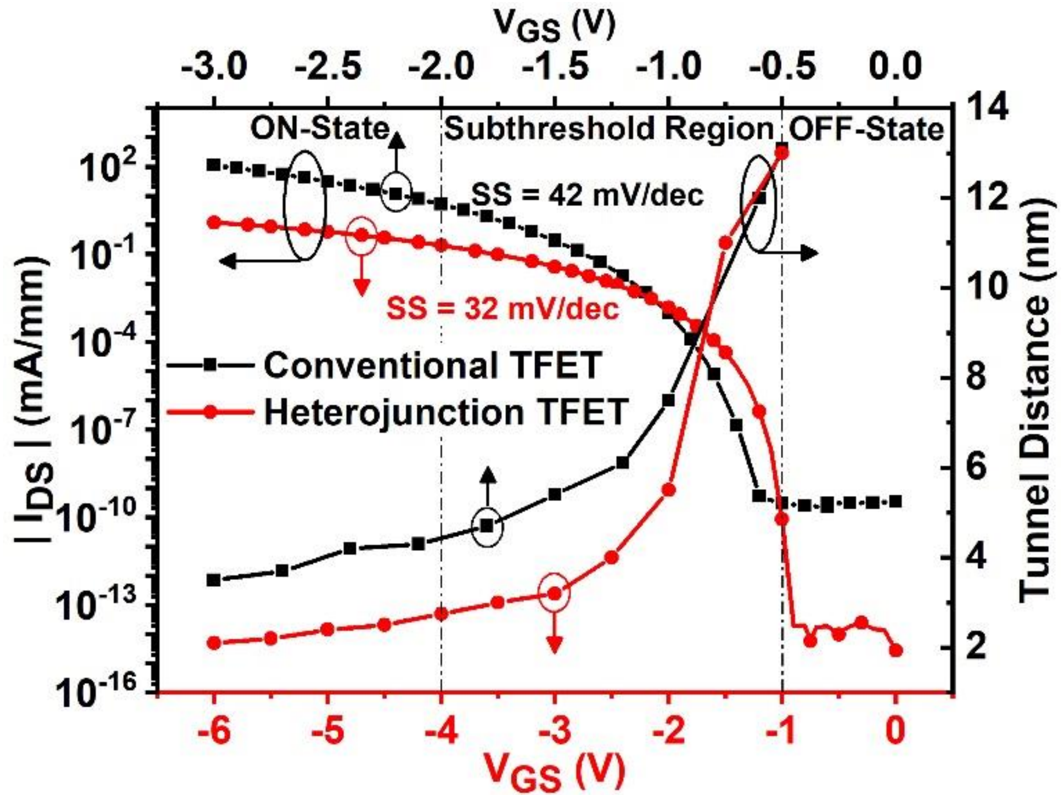

Fig. 6.9. Variations of the drain current and tunnel distance with respect to gate bias for a conventional TFET in Si and a heterojunction TFET in GaN.

6.6. Summary

In summary, an analysis of a p-type heterojunction TFET in GaN reveals that owing to a polarisation induced tunnel junction to enable carrier transport, transfer characteristics do not suffer from ambipolarity. Unlike common p-channel MOSHFETs in GaN, the transfer characteristics show normally-off operation with a threshold voltage greater than $|-4|\ V$, along with a subthreshold swing of 36 mV/dec. Despite a low hole mobility and a tunneling mechanism, which raises the resistance of the source and drain path, the device is able to achieve a drain-current $\sim 1.2\ mA/mm$ with an ON/OFF current ratio of $\sim 10^{14}$ at a much smaller footprint of $< 20\ nm \times 20\ nm$, making an array of such devices can serve as a viable candidate for achieving high performance low power p-channel MOSHFET on GaN. In addition, since the region of tunneling is pinched to the location of the PITJ, a better electrostatic control over the tunneling region via the

gate and reduction in the tunnel distance by a factor of 2 are shown in the present device compared to the conventional TFETs. Although the present mechanism is only explained utilising AlN to realise the polarisation induced tunnel junction, further improvements in the on-current and reduction in the supply voltage are expected for the PITJ based on smaller band gap materials such as InGaN or InN instead of AlN.

6.7. REFERENCES

[1] F. Akyol, S. Krishnamoorthy, and S. Rajan, “Tunneling-based carrier regeneration in cascaded GaN light emitting diodes to overcome efficiency droop,” *Appl. Phys. Lett.*, vol. 103, no. 8, pp. 1–5, 2013. DOI: 10.1063/1.4819737.

[2] F. Akyol, S. Krishnamoorthy, Y. Zhang, and S. Rajan, “GaN-based three-junction cascaded light-emitting diode with low-resistance InGaN tunnel junctions,” *Appl. Phys. Express*, vol. 8, no. 8, 2015. DOI: 10.7567/APEX.8.082103.

[3] Y. Zhang, S. Krishnamoorthy, J. M. Johnson, F. Akyol, A. Allerman, M. W. Moseley, A. Armstrong, J. Hwang, and S. Rajan, “Interband tunneling for hole injection in III-nitride ultraviolet emitters,” *Appl. Phys. Lett.*, vol. 106, no. 14, pp. 2–7, 2015. DOI: 10.1063/1.4917529.

[4] M. F. Schubert, “Polarization-charge tunnel junctions for ultraviolet light-emitters without p -type contact,” *Appl. Phys. Lett.*, vol. 96, no. 3, pp. 1–4, 2010. DOI: 10.1063/1.3280866.

[5] S. Krishnamoorthy, T. F. Kent, J. Yang, P. S. Park, R. C. Myers, and S. Rajan, “GdN nanoisland-based GaN tunnel junctions,” *Nano Lett.*, vol. 13, no. 6, pp. 2570–2575, 2013. DOI: 10.1021/NL4006723.

[6] M. Malinverni, D. Martin, and N. Grandjean, “InGaN based micro light emitting diodes featuring a buried GaN tunnel junction,” *Appl. Phys. Lett.*, vol. 107, no. 5, 2015. DOI: 10.1063/1.4928037.

[7] I. P. Smorchkova, E. Haus, B. Heying, P. Kozodoy, P. Fini, J. P. Ibbetson, S. Keller, S. P. DenBaars, J. S. Speck, and U. K. Mishra, “Mg doping of GaN layers grown by plasma-assisted molecular-beam epitaxy,” *Appl. Phys. Lett.*, vol. 76, no. 6, pp. 718–720, Feb. 2000. DOI: 10.1063/1.125872.

[8] P. Kozodoy, H. Xing, S. P. DenBaars, U. K. Mishra, A. Saxler, R. Perrin, S. Elhamri, and W. . Mitchel, “Heavy doping effects in Mg-doped GaN,” *J. Appl. Phys.*, vol. 87, no. 4, pp. 1832–1835, 2000. DOI: 10.1063/1.372098.

[9] M. Grundmann and U. Mishra, “Multi-color light emitting diode using polarization-induced tunnel junctions,” *Phys. Status Solidi*, vol. 4, no. 7, pp. 2830–2833, 2007. DOI:

10.1002/PSSC.200674878.

[10] J. Simon, Z. Zhang, K. Goodman, H. Xing, T. Kosel, P. Fay, and D. Jena, "Polarization-Induced Zener Tunnel Junctions in Wide-Band-Gap Heterostructures," *Phys. Rev. Lett.*, vol. 103, no. 2, p. 026801, 2009. DOI: 10.1103/PHYSREVLETT.103.026801.

[11] S. Krishnamoorthy, D. N. Nath, F. Akyol, P. S. Park, M. Esposto, and S. Rajan, "Polarization-engineered GaN/InGaN/GaN tunnel diodes," *Appl. Phys. Lett.*, vol. 97, no. 20, 2010. DOI: 10.1063/1.3517481.

[12] M. Kaga, T. Morita, Y. Kuwano, K. Yamashita, K. Yagi, M. Iwaya, T. Takeuchi, S. Kamiyama, and I. Akasaki, "GaInN-Based Tunnel Junctions in n–p–n Light Emitting Diodes," *Jpn. J. Appl. Phys.*, vol. 52, no. 8S, p. 08JH06, 2013. DOI: 10.7567/JJAP.52.08JH06.

[13] S. Krishnamoorthy, F. Akyol, P. S. Park, and S. Rajan, "Low Resistance GaN / InGaN / GaN Tunnel Junctions," *Appl. Phys. Lett.*, vol. 102, 2013.

[14] A. Seabaugh, S. Fathipour, W. Li, H. Lu, J. H. Park, A. C. Kummel, D. Jena, S. K. Fullerton-Shirey, and P. Fay, "Steep subthreshold swing tunnel FETs: GaN/InN/GaN and transition metal dichalcogenide channels," in *2015 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2015, p. 35.6.1-35.6.4. DOI: 10.1109/IEDM.2015.7409835.

[15] W. Li, S. Sharmin, H. Ilatikhameneh, R. Rahman, Y. Lu, J. Wang, X. Yan, A. Seabaugh, G. Klimeck, D. Jena, and P. Fay, "Polarization-Engineered III-Nitride Heterojunction Tunnel Field-Effect Transistors," *IEEE J. Explor. Solid-State Comput. Devices Circuits*, vol. 1, no. March, pp. 28–34, Dec. 2015. DOI: 10.1109/JXCDC.2015.2426433.

[16] F. Akyol, S. Krishnamoorthy, Y. Zhang, J. Johnson, J. Hwang, and S. Rajan, "Low-resistance GaN tunnel homojunctions with 150 kA/cm 2 current and repeatable negative differential resistance," *Appl. Phys. Lett.*, vol. 108, no. 13, p. 131103, Mar. 2016. DOI: 10.1063/1.4944998.

[17] H. Lu and A. Seabaugh, "Tunnel Field-Effect Transistors: State-of-the-Art," *IEEE J. Electron Devices Soc.*, vol. 2, no. 4, pp. 44–49, Jul. 2014. DOI: 10.1109/JEDS.2014.2326622.

[18] E. Memisevic, J. Svensson, M. Hellenbrand, E. Lind, and L.-E. Wernersson, "Vertical InAs/GaAsSb/GaSb tunneling field-effect transistor on Si with S = 48 mV/decade and Ion = 10 μA/μm for Ioff = 1 nA/μm at Vds = 0.3 V," in *2016 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2016, p. 19.1.1-19.1.4. DOI: 10.1109/IEDM.2016.7838450.

[19] U. E. Avci, D. H. Morris, and I. A. Young, "Tunnel field-effect transistors: Prospects and challenges," *IEEE J. Electron Devices Soc.*, vol. 3, no. 3, pp. 88–95, 2015. DOI: 10.1109/JEDS.2015.2390591.

[20] D. B. Abdi and M. J. Kumar, "Controlling ambipolar current in tunneling FETs using

overlapping gate-on-drain," *IEEE J. Electron Devices Soc.*, vol. 2, no. 6, pp. 187–190, 2014. DOI: 10.1109/JEDS.2014.2327626.

[21] A. S. Verhulst, W. G. Vandenberghe, K. Maex, and G. Groeseneken, "Tunnel field-effect transistor without gate-drain overlap," *Appl. Phys. Lett.*, vol. 91, no. 5, p. 053102, 2007. DOI: 10.1063/1.2757593.

[22] T. Krishnamohan, D. Kim, S. Raghunathan, and K. Saraswat, "Double-Gate Strained-Ge Heterostructure Tunneling FET (TFET) With record high drive currents and <60mV/dec subthreshold slope," in *2008 IEEE International Electron Devices Meeting*, Dec. 2008, vol. 67, no. May 2006, pp. 1–3. DOI: 10.1109/IEDM.2008.4796839.

[23] I. Vurgaftman and J. R. Meyer, "Band parameters for nitrogen-containing semiconductors," *J. Appl. Phys.*, vol. 94, no. 6, p. 3675, 2003. DOI: 10.1063/1.1600519.

[24] A. Adikimenakis, K. E. Aretouli, E. Iliopoulos, A. Kostopoulos, K. Tsagaraki, G. Konstantinidis, and A. Georgakilas, "High electron mobility transistors based on the AlN/GaN heterojunction," *Microelectron. Eng.*, vol. 86, no. 4–6, pp. 1071–1073, Apr. 2009. DOI: 10.1016/J.MEE.2009.02.004.

[25] "Silvaco TCAD Atlas." Version V3.44.1R https://www.silvaco.com/products/tcad.html. [Accessed: 10-Dec. 2018].

[26] M. Farahmand, C. Garetto, E. Bellotti, K. F. Brennan, M. Goano, E. Ghillino, G. Ghione, J. D. Albrecht, and P. P. Ruden, "Monte Carlo simulation of electron transport in the III-nitride wurtzite phase materials system: binaries and ternaries," *IEEE Trans. Electron Devices*, vol. 48, no. 3, pp. 535–542, Mar. 2001. DOI: 10.1109/16.906448.

[27] Silvaco Inc., *Atlas User's Manual*. Silvaco International Software, Santa Clara, CA, USA, Aug. 2016.

[28] A. Nakajima, P. Liu, M. Ogura, T. Makino, K. Kakushima, S. Nishizawa, H. Ohashi, S. Yamasaki, and H. Iwai, "Generation and Transportation Mechanisms for Two-Dimensional Hole Gases in GaN/AlGaN/GaN Double Heterostructures," *J. Appl. Phys.*, vol. 115, no. 15, p. 153707, Apr. 2014. DOI: 10.1063/1.4872242.

[29] P. Rinke, M. Winkelnkemper, a. Qteish, D. Bimberg, J. Neugebauer, and M. Scheffler, "Consistent set of band parameters for the group-III nitrides AlN, GaN, and InN," *Phys. Rev. B*, vol. 77, no. 7, p. 075202, Feb. 2008. DOI: 10.1103/PHYSREVB.77.075202.

[30] J.-K. Ho, C.-S. Jong, C. C. Chiu, C.-N. Huang, C.-Y. Chen, and K.-K. Shih, "Low-resistance ohmic contacts to p-type GaN," *Appl. Phys. Lett.*, vol. 74, no. 9, p. 1275, 1999. DOI: 10.1063/1.123546.

[31] J. O. Song, J.-S. Ha, and T.-Y. Seong, "Ohmic-Contact Technology for GaN-Based Light-Emitting Diodes: Role of P-Type Contact," *IEEE Trans. Electron Devices*, vol. 57, no. 1, pp. 42–59, 2010. DOI: 10.1109/TED.2009.2034506.

[32] C. B. Maliakkal, N. Hatui, R. D. Bapat, B. A. Chalke, A. A. Rahman, and A. Bhattacharya,

"The Mechanism of Ni-Assisted GaN Nanowire Growth," *Nano Lett.*, vol. 16, no. 12, pp. 7632–7638, 2016. DOI: 10.1021/ACS.NANOLETT.6B03604.

[33] X. Chen, J. Li, Y. Cao, Y. Lan, H. Li, M. He, C. Wang, Z. Zhang, and Z. Qiao, "Straight and Smooth GaN Nanowires," *Adv. Mater.*, vol. 12, no. 19, pp. 1432–1434, Oct. 2000. DOI: 10.1002/1521-4095(200010)12:19<1432::AID-ADMA1432>3.0.CO;2-X.

[34] V. Nagavarapu, R. Jhaveri, and J. C. S. Woo, "The Tunnel Source (PNPN) n-MOSFET: A Novel High Performance Transistor," *IEEE Trans. Electron Devices*, vol. 55, no. 4, pp. 1013–1019, Apr. 2008. DOI: 10.1109/TED.2008.916711.

[35] H. Y. Chang, B. Adams, P. Y. Chien, J. Li, and J. C. S. Woo, "Improved subthreshold and output characteristics of source-pocket Si tunnel FET by the application of laser annealing," *IEEE Trans. Electron Devices*, vol. 60, no. 1, pp. 92–96, 2013. DOI: 10.1109/TED.2012.2228006.

Chapter 7 Negative Capacitance beyond Ferroelectric Switches

Negative capacitance transistors are a unique class of switches capable of operation beyond the Boltzmann limit to realise sub-thermionic switching. Until now, the negative capacitance effect has been predominantly attributed to devices employing an unstable insulator with ferroelectric properties, exhibiting a two-well energy landscape, in accordance with Landau theory. The theory and operation of a solid electrolyte Field Effect Transistor (SE-FET) of subthreshold swing less than $60\ mV/dec$ in the absence of a ferroelectric gate dielectric is demonstrated in this work. Unlike ferroelectric FETs that rely on a sudden switching of dipoles to achieve negative capacitance, we demonstrate the modelling of a distinctive mechanism that relies on the accumulation and dispersion of ions at the interfaces of the oxide, leading to a subthreshold slope (SS) as low as $26\ mV/dec$, first reported in [1] and [2]. The frequency of operation of these unscaled devices lies in a few milli-Hertz, because at higher or lower frequencies, the ions in the insulator are either too fast or too slow to produce voltage amplification. This is unlike Landau switches, where the SS remains below $60\ mV/dec$ even under quasi-static sweep of the gate bias. The proposed FETs show a higher on-current with thicker oxide in the entire range of gate voltage, clearly distinguishing their scaling laws from those of ferroelectric FETs. Our theory validated with experiment, demonstrates a new class of devices capable of negative capacitance that opens up alternate methods of steep switching beyond the traditional approach of Ferroelectric or memristive FETs.

7.1. Introduction

Complementary Metal Oxide Semiconductor (CMOS) technology is the main driver of the contemporary information age. Its pervasiveness has been delivered by an

exponential increase in processing power of a chip via a continuous reduction in the physical dimensions of transistors by almost a factor of half, every 18 months, according to Moore's law. Despite continuous downscaling, a proportional reduction in the supply voltage has been a greater challenge since the last decade, resulting in higher density chips with increased power consumption today. As introduced in chapter 2, this limitation arises because the drain to source current, I_{DS} is exponentially dependent on the semiconductor surface potential (Ψ_s) [3], i.e., $I_{DS} \propto exp\ (q\Psi_s/k_BT)$, requiring Ψ_s to change by at least $\sim 60\ mV$ for an order of magnitude (a decade) change in I_{DS}. Overcoming this Boltzmann limit ($60\ mV/dec$) of the sub-threshold swing (SS) of a Metal–Oxide–Semiconductor Field Effect Transistor (MOSFET) is considered as a possible continuation of CMOS scaling for future logic devices [4]–[7]. Broadly speaking, beyond the relationship between Ψ_s and I_{DS} as indicated above, the SS is affected by how well the gate can be coupled to the semiconductor, via the body factor m, where V_{GS} is the applied potential at the gate, distributed across the gate dielectric and the semiconductor region of a typical transistor as

$$V_{GS} = \phi_{ms} + V_{ox} + \Psi_s \qquad (7.1)$$

Where ϕ_{ms} represents the difference in work function between the gate and semiconductor, and V_{ox} is the potential drop across the dielectric. In such a case, for a constant ϕ_{ms}, m, the body factor can be expressed as $m = dV_{GS}/d\Psi_s$. If the capacitances associated with the gate dielectric and the semiconductor are represented as C_{ins} and C_{sc} respectively, the body factor m is equal to $1 + C_{sc}/C_{ins} > 1$, giving rise to a subthreshold swing [4], $SS = m \times 2.3k_BT/q = m\ \times n > 60\ mV/dec$ in conventional transistors. A change in the surface potential ($d\Psi_s$) larger than the change in the applied gate bias (dV_{GS}) is required to achieve $m < 1$.

A number of alternative approaches, broadly considered subsets of "Steep Subthreshold devices", are now being contemplated to achieved $m < 1$. Techniques that result in $m < 1$, also largely referred to as Landau switches [8], are of great significance to technology, as they result in low operating voltages and thereby reduced power consumption of electronic circuits. Amongst such techniques, reported to date, the most promising for future technology nodes are ferroelectric FETs (FE-FETs) [9], [10], initiated by the pioneering work of Salahuddin and Datta in 2008 [11], though others, such as piezoelectric FETs [12], [13], nanoelectromechanical FETs (NEMFETs) [14]–[16], and phase-FETs [17], [18], employing a resistive switch have also been reported. There are two important distinctions in approach amongst the various mechanisms that are described. In one case, the net capacitance between the gate and the semiconductor channel is boosted by introducing a material in the gate dielectric stack with an inherent instability, such as in a FE-FET or a NEMFET [8], depicted in Fig. 7.1 (a). In these FETs, the energy profile of the gate dielectric stack exhibits a dual energy-well that upon transition from one well to the other, leads to a negative capacitance $C_{FE/NEM}$. In the second case, the abrupt switching of a resistive switch in series with the current flow path, between a low resistance state (LRS) and a high resistance state (HRS), is utilised to produce steep switching. The resistive switch is typically realised either with a material exhibiting insulator-to-metal transition (IMT) such as vanadium dioxide [17] or a memristor element, as in Fig. 7.1 (b), realised either via a phase change memory (PCM), electrochemical metallization memory (ECM), or valence change memory (VCM) [19]. In PCMs, a change in the phase of a material, e.g. GeTe or Sb_2Te_3, from the amorphous to crystalline or vice-versa 'sets' or 'resets' the device in the LRS or HRS. The ECM consists of an active electrode of Ag or Cu and a counter electrode of e.g. Pt separated by an insulating layer of solid electrolyte, e.g. SiO_2 or Ta_2O_5, where resistive switching

from the HRS to the LRS takes place via migration of metallic ions from the active electrodes into the insulator, thus forming a conducting filament [20]. In the case of a VCM, the movement of negatively charged oxygen ions or positively charged vacancies in the thin film ($\sim 10\ nm$) of, for example TaOx, HfOx, or TiOx, results in the formation/dissolution of a vacancy rich conducting filament that is responsible for resistive switching [21].

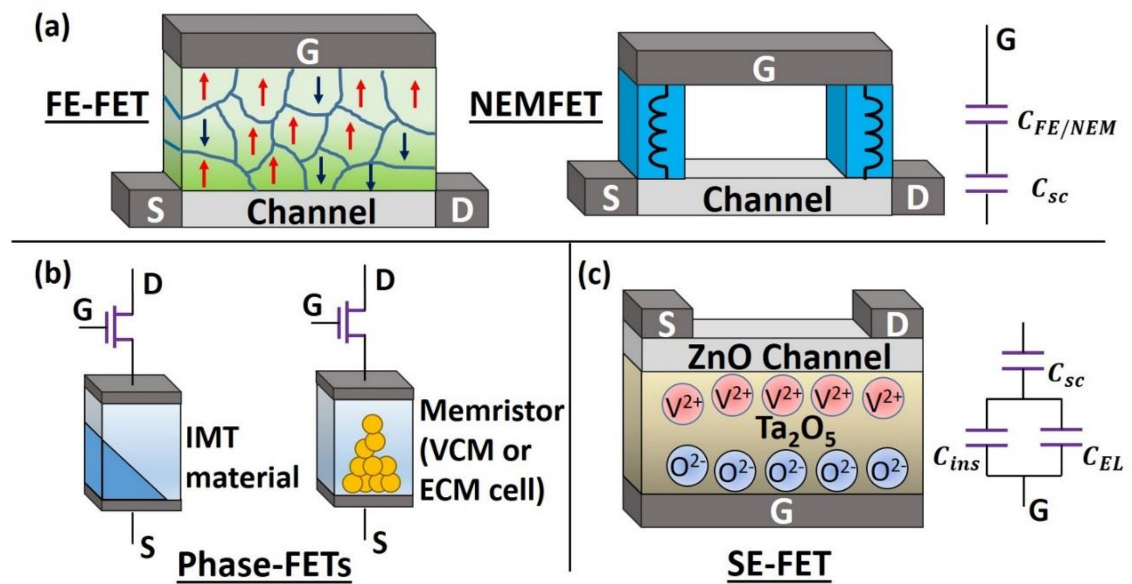

Fig. 7.1. Various schemes for sub-60 mV/dec switching. (a) Device schematic of a FE-FET (LHS) and a NEMFET (RHS) where due to either the switching of domains in the FE-FET, or electromechanical motion of the gate in the NEMFET, $C_{FE/NEM}$ becomes negative, resulting in a body factor $m = 1 + C_{sc}/C_{FE/NEM} < 1$ and $SS < 60\ mV/dec$. (b) Phase-FETs, where a resistive switch either consisting of a material exhibiting insulator-to-metal phase transition (IMT) (LHS) or a memristor (VCM or ECM) (RHS) is included in the current path of an ordinary FET. (c) Schematic of a $\mathrm{Ta_2O_5/ZnO}$ device and the equivalent gate circuit model of the MOS capacitor, indicating charge separation of oxygen ions and vacancies at respective opposite interfaces of the Ta_2O_5. An additional capacitance C_{EL} arises as a result, in parallel with the gate dielectric capacitor C_{ins}.

In this work, we demonstrate an alternate Negative Capacitance mechanism to achieve steep switching characteristics but only under dynamic operation in Ta_2O_5/ZnO solid electrolyte (SE-) FETs, shown in Fig. 7.1 (c). As indicated in this figure, the

presence of doubly charged mobile oxygen ions and vacancies in the Ta_2O_5, induces a sheet charge at the interface of Ta_2O_5 and ZnO, which gives rise to an additional electrolytic capacitance, indicated by C_{EL} in the equivalent circuit diagram. We develop a theoretical framework that provides evidence that under a dynamic sweep of the gate bias, C_{EL} achieves a negative value such that $|C_{EL}| > C_{ins}$, leading to sub-60 mV/dec switching, yet without the involvement of any ferroelectric material or filamentary processes in the gate insulator.

7.2. **RESULTS**

Our alternate mechanism for steep switching is demonstrated in bottom gated three-terminal thin-film transistors fabricated in-house by our team, as shown in Fig. 7.1 (c). A conducting Indium Tin Oxide (ITO, 20 Ω/square) is used as gate, thicknesses of 120 and $275\ nm$ of tantalum oxide (Ta_2O_5) of dielectric constant $\epsilon_{Ta_2O_5} \approx 20.8$ are deposited as the gate insulator and $40\ nm$ of zinc oxide as channel, via RF sputtering as reported in ref [1]. The sputtered Ta_2O_5 results in an amorphous phase, as the temperature required for crystallisation is more than 1000 K [22]. The transfer characteristics data, supplied for the purpose of this work, consist of the drain-current in the forward and backward directions at scan rates of gate voltage ranging from $2.17\ mHz$ to $15.65\ mHz$, obtained using an Agilent B1500 in Fig. 7.2 (a). During the backward sweep, a two-fold reduction in the average subthreshold swing is observed when the scan rate is reduced from $15.65\ mHz$ to $2.17\ mHz$, while the gate leakage current of the device always remains below $1\ nA$, as displayed in the inset. Unlike the conventional clockwise hysteresis associated with charge trapping at oxide/semiconductor interfaces that leads to a reduction in the drain current during the backward sweep [23], the anticlockwise hysteresis in the transfer characteristics, as well as its dependence on the scan rate, indicates the presence of an electric field dependent memory effect arising from

ionic motion in the insulator that closely resembles the flipping of electric dipoles in a ferroelectric FET [24]. In the present case, factors governing the value of m can be understood from the relationship of the surface potential of the channel in response to an applied gate voltage, which in its simplest form is given as

$$V_{GS} = \phi_{ms} + \frac{Q_{ch}}{C_{ins}} - \frac{Q_{ox}}{C_{ins}} + \Psi_s \quad (7.2)$$

C_{ins} is the unit area capacitance of the gate insulator, Q_{ox} is the sheet charge density at the interface of the oxide and semiconductor, and Q_{ch} is the sheet charge density in the semiconductor. In the present case, due to accumulation-dispersion of ions and vacancies within the gate dielectric under dynamic sweep of the gate voltage, the charge in the insulator, Q_{ox} varies with the applied gate bias. This can be expressed by first taking the derivative of Eq. (7.2) with respect to Ψ_s, and rewriting the derivative of Q_{ox} with respect to V_{ox} with an application of the chain rule, as:

$$\frac{dV_{GS}}{d\Psi_s} = \frac{d\phi_{ms}}{d\Psi_s} + \frac{1}{C_{ins}}\frac{dQ_{ch}}{d\Psi_s} - \frac{1}{C_{ins}}\frac{dV_{ox}}{d\Psi_s}\frac{dQ_{ox}}{dV_{ox}} + 1 \quad (7.3)$$

By defining $dQ_{ch}/d\Psi_s = \mathrm{C}_{sc}$ as the unit area capacitance associated with the semiconductor and $dQ_{ox}/dV_{ox} = \mathrm{C}_{EL}$ as a unit area differential electrolytic capacitance, equating $d\phi_{ms}/d\Psi_s$ to zero for a constant ϕ_{ms}, and substituting V_{ox} from Eq. (7.1), the above equation can be simplified to the desired expression, as

$$m = 1 + \frac{C_{sc}}{C_{EL} + C_{ins}} \quad (7.4)$$

Where m $(= dV_{GS}/d\Psi_s)$ is the body factor, C_{EL} is defined as dQ_{ox}/dV_{ox}. In the present case, if the rate of change of vacancies dQ_{ox}/dt at the interface of Ta_2O_5 with the semiconductor is higher than the rate of change of bias across the oxide dV_{ox}/dt, the resulting C_{EL} turns negative with a magnitude greater than C_{ins}, resulting in m less than unity according to Eq. (7.4). Electrolyte gated transistors have been used in the past to

achieve high carrier densities [25], realise non-volatile memories [26], reduce operating voltage [27], or reduce subthreshold slope but only down to 82 mV/dec [28] to our knowledge.

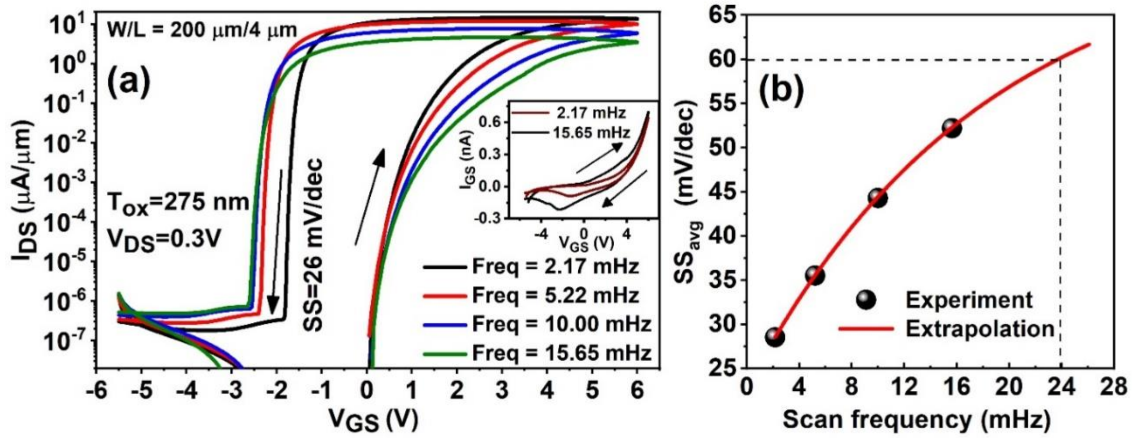

Fig. 7.2. Measured Transfer characteristics and subthreshold swing. (a) Dependence of the switching properties of fabricated ZnO/Ta_2O_5 SE-FETs on the scan rate of the gate voltage and the corresponding gate current characteristics. Transfer characteristics are captured under forward and reverse sweeps for frequencies ranging from 2.17 mHz to 15.65 mHz, corresponding to scan rates of 0.05 V/s − 0.36 V/s. A steep subthreshold swing of 26 mV/dec is obtained corresponding to the lowest sweep frequency. Corresponding gate currents for two gate bias sweeps are plotted in the inset. (b) Dependence of the subthreshold swing extracted from the $I_{DS} - V_{GS}$ characteristics in (a) in the reverse sweep, on the scan frequency. The subthreshold slope begins to exceed 60 mV/dec beyond 23 mHz of the gate sweep in the reverse direction.

Whilst negative capacitance under dynamic conditions has been observed in materials ranging from crystalline to amorphous inorganic semiconductors and organic compounds [29], [30], it has previously been attributed to minority carrier flow, interface states, slow transient time of the carriers, or space charge [30]. This is the first instance of dynamic negative capacitance at a suitable scan rate to obtain a $SS < 60\ mV/dec$ in thin film transistors [1]. As the gate sweep frequency is increased beyond ∼20 mHz, a sub-60 mV/dec of SS disappears as shown in Fig. 7.2 (b), as the phenomenon requires ionic motion within the insulator to equilibrate with the applied gate electric field. This

chapter attempts to develop a model to explain these characteristics.

The dynamic drain current characteristics of the SE-FET are evaluated by self-consistently coupling the electronic charge density in the ZnO semiconductor with the variable Q_{ox}, owing to the field dependent motion of oxygen ions inside Ta_2O_5. Ta_2O_5 amongst other oxides such as HfO_2 and TiO_x, is widely known to contain oxygen ions and vacancies whose dynamics have been utilised to explain the resistive switching behaviour in valence change memory (VCM) cells. In our model, the motion of ions is modelled as the drift and diffusion of doubly charged negative oxygen ions [31] in the Ta_2O_5 solid electrolyte (SE) under an electric field, where the drift velocity of the ions subjected to an external electric field $\mathcal{E}_{ox}$ is described by the point ion model of Mott and Gurney [32], [33] as

$$v_d = af \exp - \frac{E_a}{kT} \sinh \frac{q_z a \mathcal{E}_{ox}}{kT} \tag{7.5}$$

Where a is the effective hopping distance, which is of the order of interatomic distance ($\sim 0.2 - 0.5\ nm$ [19]), E_a is the height of the potential barrier, and f is the attempt frequency.

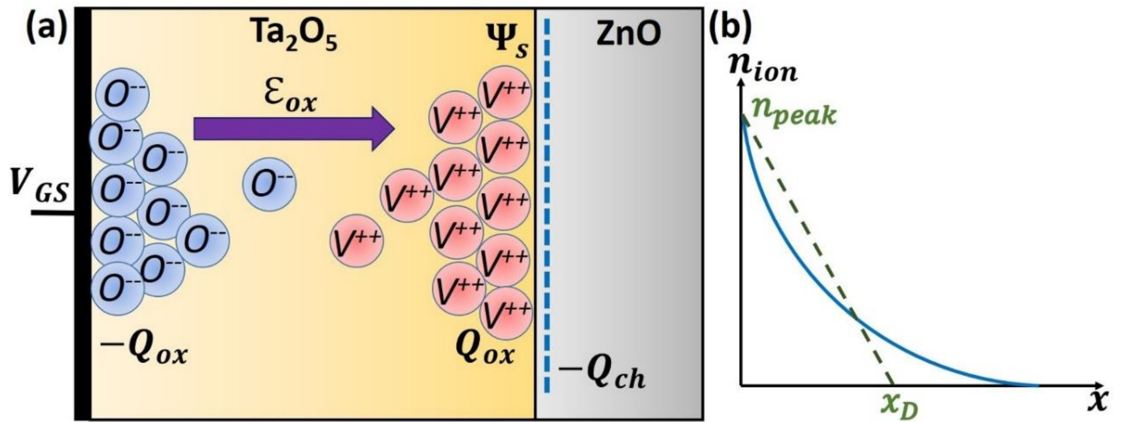

Fig. 7.3. (a) Schematic showing the accumulation of oxygen ions and vacancies at opposite interfaces of the insulator. (b) An arbitrary ion profile across the interface and its linear approximation.

Referring to Fig. 7.2 (a), since the applied gate bias and hence the voltage across the

insulator V_{ox}, which determines the $\mathcal{E}_{ox}$ remain much lower than the maximum gate bias during the majority of operation, equation (7.5) can be safely linearly approximated as

$$v_d = \mu_{ion}\mathcal{E}_{ox} \tag{7.6}$$

Where μ_{ion} defined as $q_z a^2 f \exp(-E_a/kT)\ /kT$ is the mobility of oxygen ions. The rate of change of sheet charge density at an interface dQ_{ox}/dt is governed by a balance between the drift and diffusion current densities:

$$\frac{dQ_{ox}}{dt} = q_z n_{ion}\, \mu_{ion}\mathcal{E}_{ox} - q_z D\nabla n_{ion} \tag{7.7}$$

First term on the right hand side is the drift term, described by Eq. (7.6), n_{ion} is the concentration of ions, $q_z = -2e$ is the charge on the oxygen ions, where the $\mathcal{E}_{ox}$ causes the ions to accumulate at an interface, leading to the formation of interface sheet charge Q_{ox} at the opposite interfaces of Ta_2O_5, as shown in Fig. 7.3 (a). The second term in the above equation accounts for the diffusion, where D is the diffusion coefficient of the oxygen ions, related to the mobility μ_{ion} via the Nernst-Einstein relation [34], [35] as $D = (kT/q_z)\,\mu_{ion}$.

To simplify the solution of Eq. (7.7), we assume that the density of oxide ions decays linearly away from the interface, as shown in Fig. 7.3 (b), which leads to:

$$\nabla n_{ion} \approx \frac{n_{peak}}{x_D} = \frac{1}{q_z}\frac{2Q_{ox}}{x_D^2} \tag{7.8}$$

Where n_{peak} and x_D are the average charge concentration and average diffusion thickness from the interface as indicated in Fig. 7.3 (b). Upon substitution of D and ∇n_{ion}, back into Eq. (7.7), the desired relationship for the rate of change of interface oxide charge is obtained as

$$\frac{dQ_{ox}}{dt} = q_z\mu_{ion}n_{ion}\frac{(Q_{ch} - Q_{ox})}{\epsilon_{ox}} - \frac{kT}{q_z}\mu_{ion}\cdot\frac{2Q_{ox}}{x_D^2} \tag{7.9}$$

Where the $\mathcal{E}_{ox}$ is replaced with $(Q_{ch} - Q_{ox})/\epsilon_{ox}$ using the Gauss' law and ϵ_{ox} is the

dielectric constant of the insulator. This equation is self-consistently coupled with the electronic charge density in the ZnO channel Q_{ch}. In our work in Ref. [2], μ_{ion} and x_D are kept fixed, however a better agreement between the experiment and the model is obtained for μ_{ion} and x_D that change according to $\mathcal{E}_{ox}$ and Q_{ox} inside Ta_2O_5, described as

$$\mu_{ion} = \frac{\mu_{ion,0}}{\left[1 + \left(\frac{\mu_{ion,0}\mathcal{E}_{ox}}{v_{sat}}\right)^{\beta}\right]^{\frac{1}{\beta}}} \tag{7.10}$$

$$x_D = \frac{x_{D,0}}{1 - \left(\frac{Q_{ox}}{Q_{ox,0}}\right)^2} \tag{7.11}$$

A summary of parameters used in the modelling of ions in Ta_2O_5 is presented in Table A1, appendix. The distribution of electronic density inside ZnO is evaluated by solving 1 D Poisson along with the charge density, which is obtained by integrating the density of band and trap states of ZnO with the Fermi function. The net sheet charge density in the channel Q_{ch} is calculated by summing the sheet charge densities in the conduction band and the trap states [36], Q_{free} and Q_{loc}. The trap states within the band gap of ZnO are modelled using acceptor- and donor-like tail, deep, and Gaussian density, as depicted in Fig. 7.4. The parameters used in the model are described in Tables A1 and A2 in the appendix.

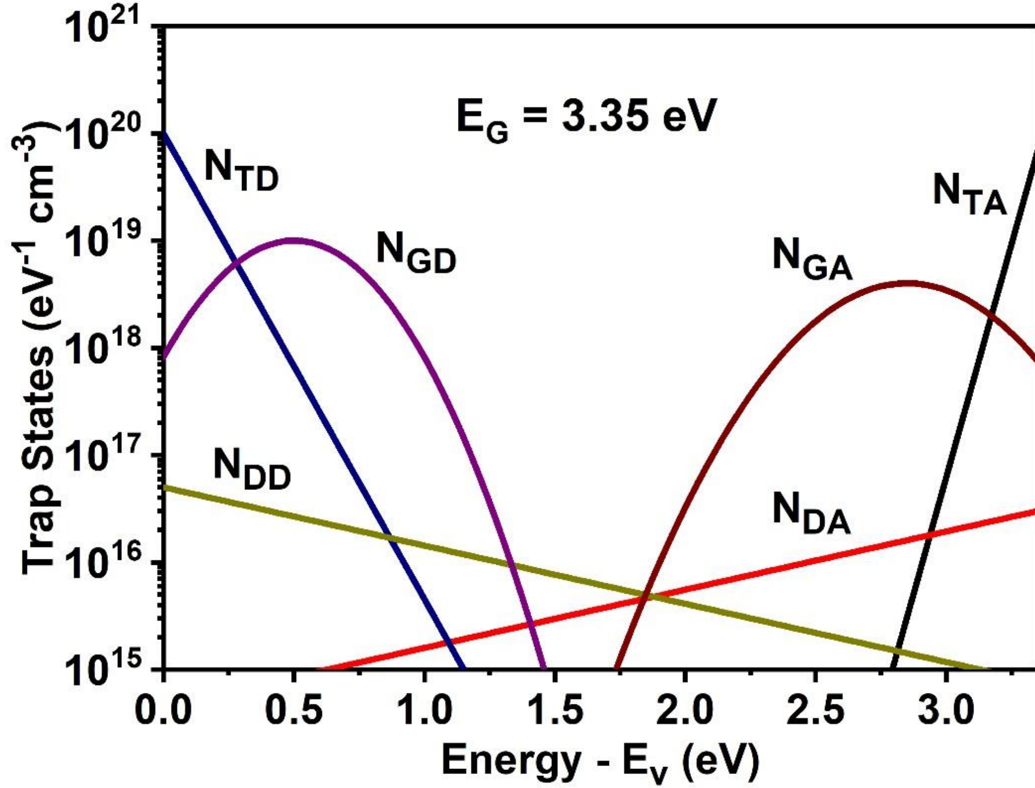

Fig. 7.4. The distribution of acceptor- and donor- like trap state densities considered in the band gap of ZnO. Refer to Table A2 in the appendix for a description of these parameters.

From a knowledge of sheet charge densities within ZnO, the dynamic transfer characteristics of this device at a given source to drain voltage, V_{DS} are obtained under the gradual channel approximation as [37]

$$I_{DS} = \mu_{ZnO} \cdot \left(\frac{Q_{free}}{Q_{ch}}\right) \cdot \frac{W}{L} Q_{free} \cdot V_{DS} \tag{7.12}$$

Where μ_{ZnO} is the band electron mobility of ZnO, W and L are the width and length of the ZnO channel.

Apart from oxygen ions, some metal cations such as W, Ta, Ti, and Hf can also participate in the oxygen exchange reactions by diffusing from the metal contact into the insulator in the vicinity of the interface, which can affect the electrical properties of thin films ($\sim 7\ nm$) of Ta_2O_5 [38]. However, Indium Tin Oxide (ITO), employed as a bottom gate, is known for its electrical and chemical stability and has been used for preventing

the diffusion of specific metallic ions [39]. While there is some evidence of diffusion of Indium ions inside an organic material after a long-term operation in Organic LEDs [40] and in some polymers [41], to the best of my knowledge no evidence is available for the diffusion of such ions from Indium Tin Oxide (ITO) or ZnO into other oxides. We, therefore, neglect the role of other mobile specifies in our analysis.

Fig. 7.5 (a) shows a comparison of the simulated transfer characteristics with the supplied experimental transfer characteristics during the forward and backward gate sweeps at a scan frequency of $10\ mHz$ for a Ta_2O_5 thickness of $275\ nm$, with a SS of $35\ mV/dec$. This thickness and scan rate are selected due to a wider hysteresis that makes it easy to visualise regions of internal voltage amplification ($a \rightarrow b$ and $c \rightarrow d$) in the figures. During the forward sweep, the doubly charged oxygen ions are driven towards the gate/Ta_2O_5 while the positively charged vacancies are accumulated at the Ta_2O_5/ZnO interface, resulting in a build-up of positive interface charge density Q_{ox} at this interface, as shown in Fig. 7.5 (b). During the backward scan of the gate bias, as V_{GS} is reduced from its maximum point, Q_{ox} continues to rise to its maximum value at a gate bias of $\sim 2.5\ V$, highlighted by the dashed circle in Fig. 7.5 (b), well below the maximum applied voltage of $6\ V$. This is attributed to the delay in achieving its steady state value, owing to the poor mobility of oxygen ions, estimated as $1 \times 10^{-11} cm^2/Vs$ via Chronoamperometry measurements of the gate current [23] described using the Cottrell equation [42] (See Table A1 in the appendix for a summary of model parameters). This build-up of Q_{ox} also helps to maintain the sheet charge density Q_{ch} in the semiconductor channel, and therefore a higher drain current in the reverse sweep. Until point a, the surface potential of the channel is maintained by Q_{ch}, while the entire drop in gate potential occurs across Ta_2O_5. Beyond point a, as V_{GS} reduces further, a sudden depletion in Q_{ox} (see inset Fig. 7.5 (b)), causes the drain current to drop sharply as the

channel is forced into depletion. The energy profiles (U vs. Q_{ch}), obtained by integrating Q_{ch} with respect to bias V_{ox} across the Ta_2O_5, are plotted in Figs. 7.5 (c) and (d) during the forward and backward sweeps of gate bias. Owing to the accumulation and sudden depletion of the mobile oxygen ions, the energy profiles show inflection points in the regions marked $c \rightarrow d$ and $a \rightarrow b$, leading to $d^2U/dQ_{ch}^2 < 0$ in these regions. The corresponding inverse unit area capacitances, plotted in Figs. 7.5 (e) and (f), show C_{EL} less than zero in these regions, with a magnitude greater than C_{ins} ($\sim 67\ nF/cm^2$, measured from MIM structures), which also causes the total capacitance $C_{tot}(= C_{ins} + C_{EL})$ to become negative. Following Eq. (7.4), this leads to a body factor less than unity. The reason why a sub-60 mV/dec switching is only present during $a \rightarrow b$ in the backward sweep but not during $c \rightarrow d$ in the forward sweep, is because Q_{ox} remains negative during the transition from $c \rightarrow d$ (see Fig. 7.5 (b)), a polarity which depletes the carriers in the channel. Therefore, the device shows no switching in this region and continues to remain in the off-state. This parallel system of capacitance C_{tot} is stabilised by the capacitance of the ZnO semiconductor, which appears in series with Ta_2O_5 gate insulator, since the required condition for stability $|C_{EL} + C_{ins}| > C_{sc}$ is satisfied.

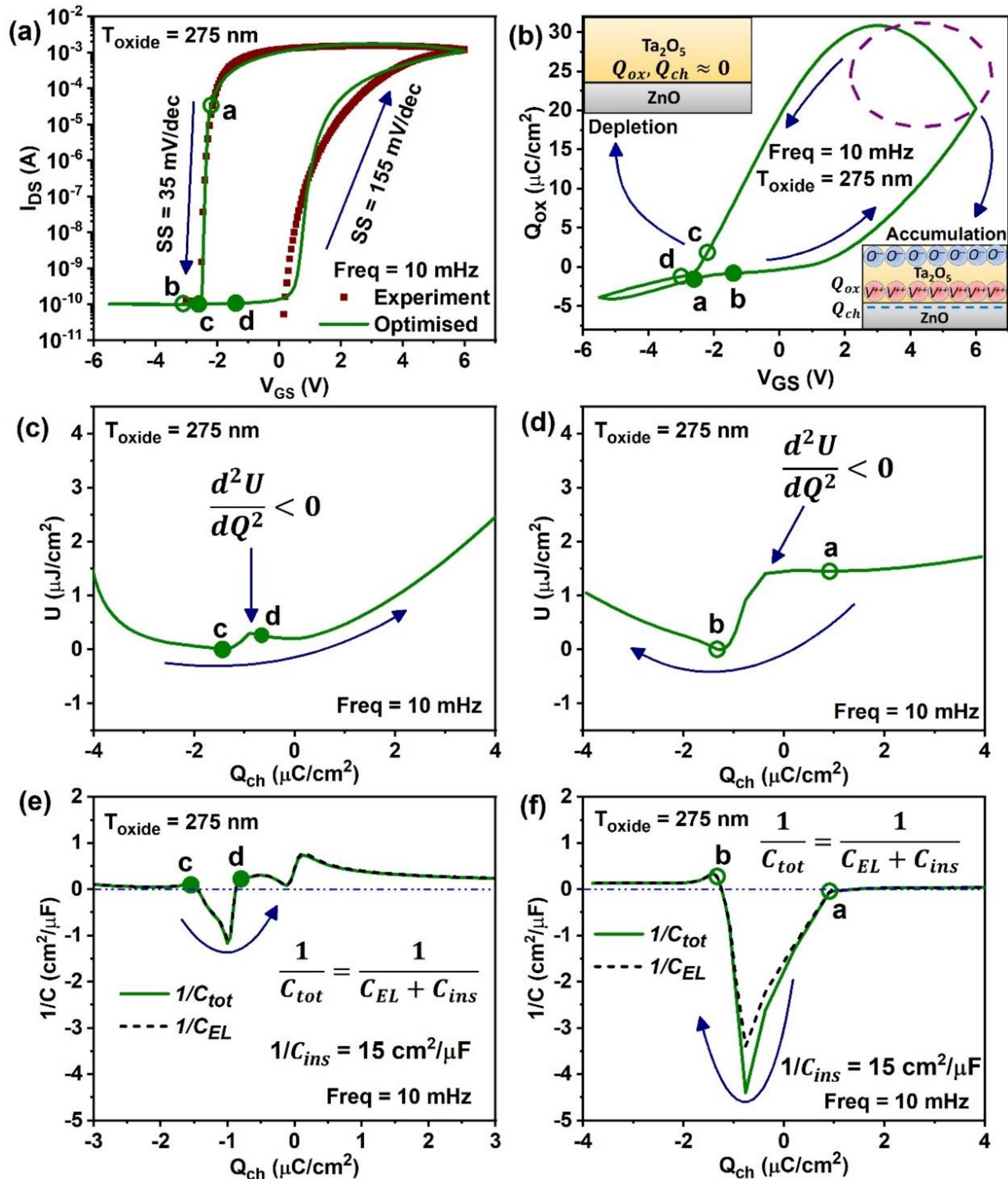

Fig. 7.5. Electrical properties and simulated energy profiles to demonstrate the origin of sub-$60\, mV/dec$ of SS. (a) Comparison of simulated and measured transfer characteristics of a $Ta_2O_5/\ ZnO$ SE-FET for an oxide thickness of $275\ nm$, at a scan frequency of $10\ mHz$. (b) Plot of sheet charge density Q_{ox} at the interface of the dielectric and the semiconductor with applied gate bias. Potential energy profiles during (c) forward and (d) backward gate sweeps are indicated by arrows. The corresponding inverse unit area capacitance with respect to sheet charge density in the channel during (e) forward and (f) backward gate sweeps.

The electrical characteristics of an SE- and an FE-FET under quasi-static gate bias sweep, are compared in Figs. 7.6 (a) and (b) for the forward and backward sweeps of the

gate bias. In Fig. 7.6 (a), since the ions in the SE have sufficient time to respond to an infinitesimally small scan rate, the hysteresis observed previously, now vanishes, the build-up of Q_{ox} remains limited only by the balance between drift (responsible for accumulation) and diffusion (responsible for depletion) of ions. The steep-switching also vanishes, since Q_{ox} simultaneously increases or decreases alongside the gate bias under equilibrium and the energy profile reduces to a single energy-well without any inflection point, as shown in the inset of Fig. 7.6 (a). In stark contrast, in an equivalent FE-FET simulated in Fig. 7.6 (b), the existence of a double energy-well profile, as shown in the inset gives rise to hysteresis in transfer characteristics, even if the bias is swept quasi-statically. Moreover, while the SS in the present device becomes greater than 60 mV/dec under quasi-static operation, it continues to remain less than 60 mV/dec in a FE-FET. This distinction that is directly based upon their underlying mechanisms, sets both types of devices apart.

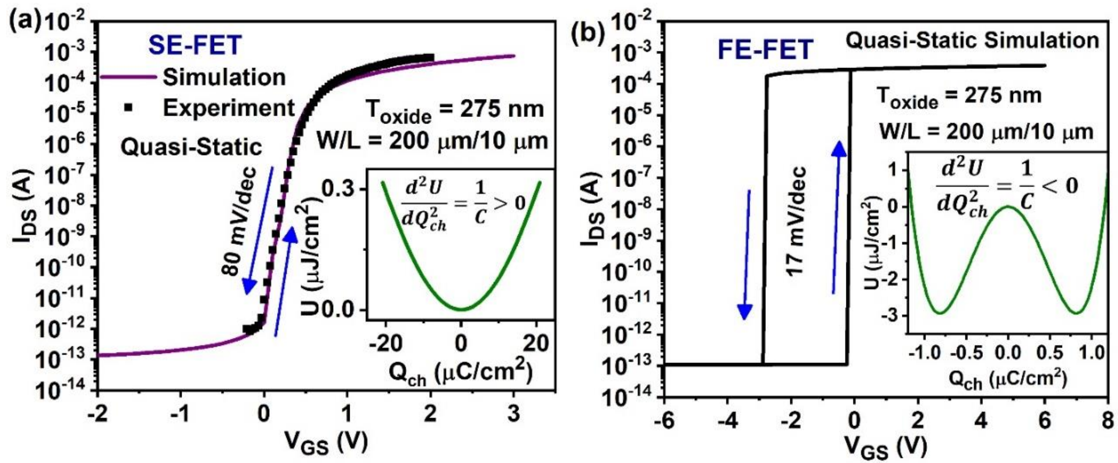

Fig. 7.6. Quasi-static transfer characteristics for SE- and FE- FETs. Comparison of transfer characteristics of an (a) SE-FET (Experimental data supplied by Xiaoyao Song, University of Sheffield) and (b) FE-FET both at a scan frequency of 33 μHz where the device characteristics tend towards their corresponding quasi-static behaviour, FE-FET is simulated using $\alpha = -3 \times 10^{11}\ cm/F$, $\beta = 6.8 \times 10^{23} cm^5/FC^2$, $\gamma = 0$, and $\rho = 4 \times 10^{11}\ \Omega\ cm$.

The mechanism of vacancy migration inside Ta_2O_5 is limited to thin films of Ta_2O_5 or TaO_x ($\sim 5 - 20\ nm$) [21], [38], [43]–[47], where a migration of ions and vacancies

leads to the formation of a vacancy rich conductive filament inside Ta_2O_5, much smaller than the thickness of our films. The measured gate current characteristics of the order of a few nanoamperes eliminate the possibility of any filamentary process (*cf.* inset, Fig. 7.2 (a)). Moreover, the temperature dependence of the transfer characteristics, as presented in Fig. 7.7, further supports our claim that the observed phenomena is due to the movements of oxygen ions. According to the point ion model of Mott and Gurney, a rise in the temperature results in a higher mobility of the ions. Therefore, at a higher temperature, the higher mobility of ions contributes to a larger Q_{ox}, which produces an increase in the drain current during the forward bias. This enhancement with respect to a change in gate bias also leads to an earlier depletion of Q_{ox} during the reverse sweep, resulting in a smaller hysteresis.

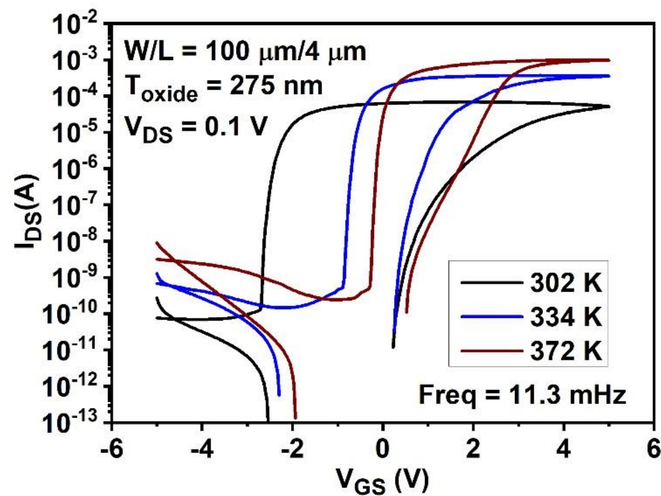

Fig. 7.7. The experimental temperature dependence of the transfer characteristics (measured by Dr. Premlal B. Pillai, University of Sheffield), showing a reduction in the hysteresis and an increase in the maximum drain current with temperature owing to an increase in the mobility of the oxygen ions inside Ta_2O_5.

The distinction in operation of our device is further established via an examination of the dynamic characteristics with frequency. The SS during the forward and backward gate bias sweep in the entire frequency range is summarised in Figs. 7.8 (a) and (b). The model of an SE-FET in Fig. 7.8 (a) exhibits $SS < 60\ mV/dec$ only in the frequency

range $\sim 2.2 - 20\ mHz$ highlighted by the oval, showing good agreement in both forward and backward sweeps with experiment. The value of steep switching during the backward sweep is sensitive to the maximum accumulated Q_{ox} and its subsequent depletion as the gate bias is reduced. As the frequency of gate sweep is increased further, the transfer characteristics of SE-FETs tend towards that of a thin film transistor (TFT) with an ordinary insulator as the gate dielectric at higher frequency. Moreover, close to the quasi-static gate bias operation, SS is $80\ mV/dec$, attesting to the excellent quality of the interface. In contrast, the dependence of the SS of a simulated FE-FET shown in Fig. 7.8 (b) reveals values less than $60\ mV/dec$ for both forward and backward scans up to $\sim 10\ \mu Hz$, where the device tends towards the quasi-static mode with both forward and backward sweep having identical slopes, for $\rho = 3 \times 10^{12}\ \Omega\ cm$. Beyond this point, the hysteresis between the forward and backward transfer characteristics becomes larger due to the finite delay in the switching of domains as determined by ρ, which leads to an increase/decrease in SS during the forward/backward sweeps respectively. As the frequency of gate sweep increases from 50 to $60\ mHz$, the response of the domains in the ferroelectric with respect to the applied gate bias become smaller due their incapability to follow the fast changing gate bias. This results in a decrease in the polarisation charge, which directly corresponds to a smaller drain current. Consequently, in this range of sweep frequency, the subthreshold swing of the device in both forward and backward directions shows an increase, due to the smaller changes in the drain current with applied gate bias. At a sweep frequency of $60\ mHz$ or beyond, the domains in the ferroelectric stop responding to the changes in gate bias, leading to constant carrier density in the channel. Thus the drain current no longer shows any switching with gate bias. Although not shown, the hysteresis of the SE-FET becomes zero at very low and high sweep frequencies where the SS for both forward and backward sweeps become

identical, whereas the hysteresis in a FE-FET, if not stabilised, can persist even for identical SS in the forward and backward sweeps, as seen in Fig. 7.6 (b).

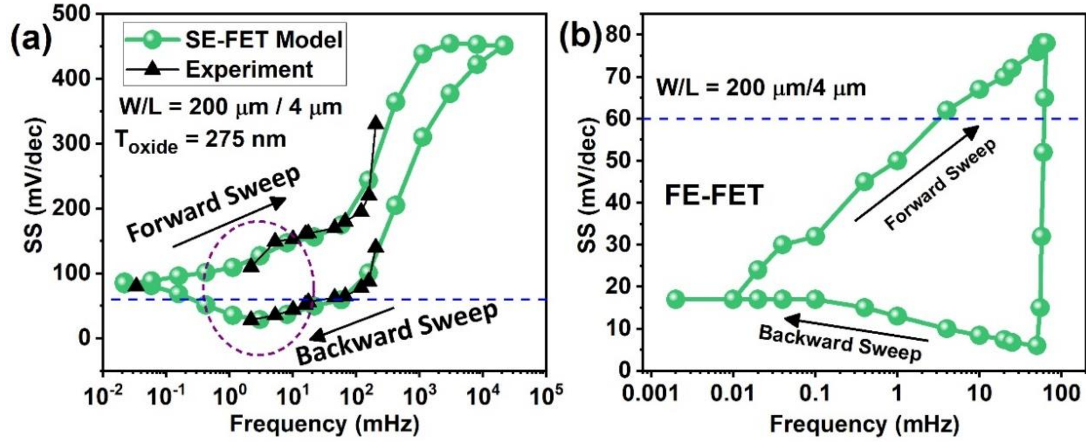

Fig. 7.8. Subthreshold swing (SS) vs. frequency of SE- and FE- FETs. (a) SS of an SE-FET with frequency of scan rate in the forward and backward directions of gate bias. (b) SS versus frequency of a FE-FET (simulated using $\alpha = -3.2 \times 10^{11}\ cm/F$, $\beta = -6.8 \times 10^{23} cm^5/FC^2$, $\gamma = 0$, and $\rho = 3 \times 10^{12}\ \Omega\ cm$) showing a below 60 mV/dec of switching at low frequency of operation in both forward and backward sweeps in contrast to the SE-FET (Experimental data supplied by Dr. Premlal B. Pillai and Xiaoyao Song, University of Sheffield).

Finally, Fig. 7.9 (a) shows a comparison of transfer characteristics during the backward scan of a SE-FET obtained from the model and measurement at different oxide thicknesses at a scan rate of $0.05\ V/s$. An increased drain to source on-current for the higher oxide thickness suggests the presence of higher sheet density of oxide ions Q_{ox} due to an increased number of mobile species, as shown in Fig. 7.10. The value of n_{ion} and x_D used in the simulation for calibration are listed in Table A1 in appendix. The scaling behaviour of an SE-FET is contrary to the scaling laws of FE-FETs of the same thickness, especially in the region of subthreshold switching, illustrated in Fig. 7.9 (b). FE-FETs show a cross-over point in their scaling [48] with a greater insulator thickness effectively reducing the electric field and thereby the polarisation due to alignment of dipoles, leading to a smaller density of carriers in the channel.

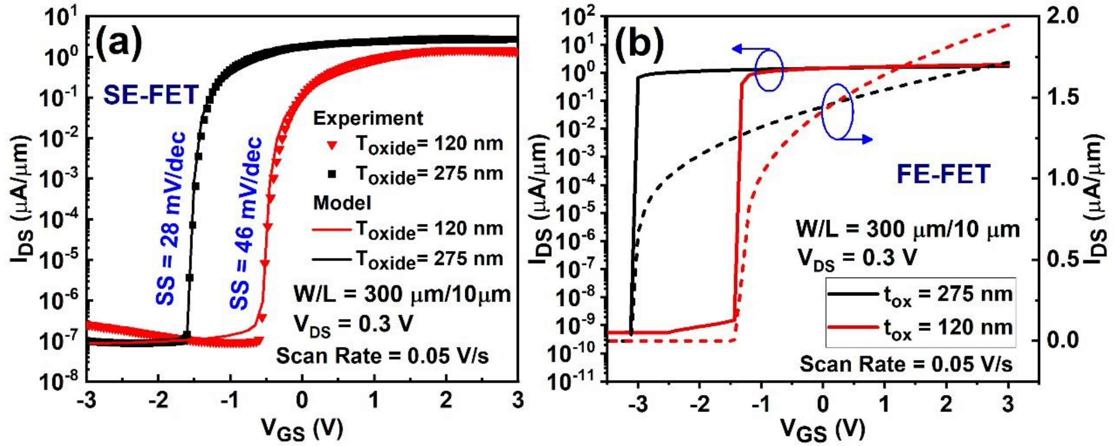

Fig. 7.9. Comparison of the SE-FET and FE-FET transfer characteristics at different gate dielectric thicknesses. (a) Experimental (supplied by Dr. Premlal B. Pillai) and modelled transfer characteristics in the reverse sweep of SE-FETs with oxide thicknesses of 120 and 275 nm and corresponding simulated behaviour, showing higher maximum on-current of 3.63 $\mu A/\mu m$ for the thicker insulator and 1.8 $\mu A/\mu m$ for thinner, at a gate-bias of 3 V, while the SS is 28 mV/dec and 48 mV/dec for both respectively. (b) shows the dependence of the ON current in log and linear scales in a FE-FET which follows a conventional scaling rule, i.e, thicker oxide device revealing lower on-current, while the SS for both the thicknesses is $\sim 16\ mV/dec$ (simulated using $\alpha = -3 \times 10^{11}\ cm/F$, $\beta = 6.8 \times 10^{23} cm^5/FC^2$, $\gamma = 0$, and $\rho = 4 \times 10^{11}\ \Omega\ cm$). A cross-over point with gate voltage is observed in the characteristics.

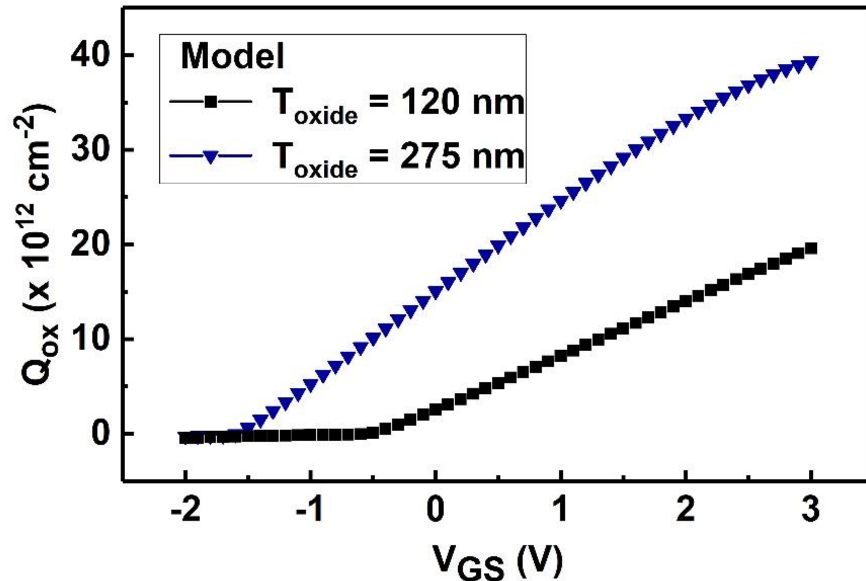

Fig. 7.10. Variation of sheet density of oxide ions at an interface for two different oxide thicknesses, demonstrating consistency of material parameters across a range of thicknesses.

An extrapolation of drain current characteristics and SS characteristics obtained from our simulation model to smaller thicknesses of Ta_2O_5, as provided in Fig. 7.11 (a) and (b), indicates that at $20\ nm$, hysteresis in the drain current shrinks to $\sim 0.2\ V$, while the SS no longer remains smaller than $60\ mV/dec$, in the backward sweep.

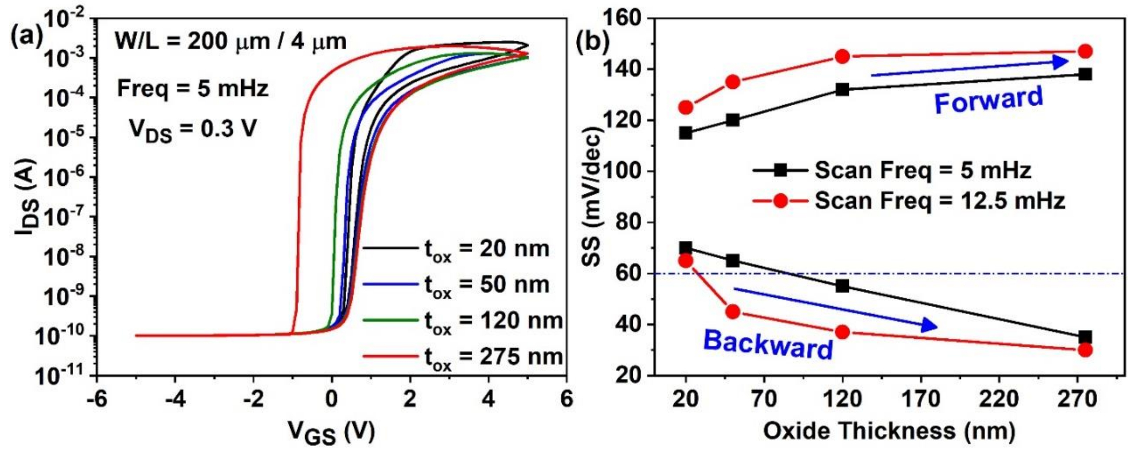

Fig. 7.11. (a) Simulated transfer characteristics, and (b) SS characteristics at different thicknesses of Ta_2O_5 layer.

The presence of hysteresis in SE-FETs aligns well with applications such as biological synapses in neuromorphic applications [1]. These devices are ideally suited for logic-in-memory via crossbar arrays rather than conventional CMOS. From a knowledge of the density and mobility of oxygen ions, the presented model can be used to predict device behaviour, i.e. the amount of hysteresis and swing for a particular sweep frequency of gate bias. The model shows that frequency of operation is directly proportional to the mobility of oxygen ions μ_{ion}. For example, an order of magnitude boost in μ_{ion} will increase the scan frequency by an order, to produce electrical characteristics with the same swing. Therefore, by adjusting μ_{ion}, e.g. with temperature, these devices can be operated at even higher frequency, e.g. $\sim 1\ Hz$, a desirable frequency in neuromorphic applications.

7.3. Summary

The theory and mechanism leading to a new class of negative capacitance FETs is

unveiled here using an example of a Ta_2O_5/ZnO FET. It is shown that the field driven motion of ions and vacancies in the gate insulator (Ta_2O_5) leads to an accumulation of charge at the interface of the semiconductor. The dispersion of this charge during the reverse sweep, without any filamentary process, creates a negative differential capacitance, responsible for steep switching as low as $26\ mV/dec$ in the mHz range in these devices via a body factor effectively less than unity. Here we prove irrevocably that the switching behaviour observed in our case, is primarily different from the mechanism arising from a dual energy landscape responsible for the switching in FE-FETs, by scrutinising the relationship of SS with the frequency in the forward and backward directions. Distinct characteristics of SE-FET identified in this work demonstrate a representative class of devices with a solid/liquid electrolyte as gate insulator, whose performance can be tuned via control of the diffusivity of ions. This class of materials therefore opens up unique opportunities for optimisation of device performance via control of interfacial phenomena in semiconductor devices.

7.4. REFERENCES

[1] P. Balakrishna Pillai and M. M. De Souza, “Nanoionics-Based Three-Terminal Synaptic Device Using Zinc Oxide,” *ACS Appl. Mater. Interfaces*, vol. 9, no. 2, pp. 1609–1618, Jan. 2017. DOI: 10.1021/ACSAMI.6B13746.

[2] A. Kumar, P. Balakrishna Pillai, X. Song, and M. M. De Souza, “Negative Capacitance beyond Ferroelectric Switches,” *ACS Appl. Mater. Interfaces*, vol. 10, no. 23, pp. 19812–19819, Jun. 2018. DOI: 10.1021/ACSAMI.8B05093.

[3] S. Datta, *Quantum Transport: Atom to Transistor*. Cambridge: Cambridge University Press, 2005. DOI: 10.1017/CBO9781139164313.

[4] A. M. Ionescu and H. Riel, “Tunnel field-effect transistors as energy-efficient electronic switches,” *Nature*, vol. 479, no. 7373, pp. 329–337, Nov. 2011. DOI: 10.1038/NATURE10679.

[5] International Technology Roadmap for Semiconductors (ITRS), “More Moore,” *ITRS*, 2015. [Online]. Available: http://www.itrs2.net/itrs-reports.html. [Accessed: 10-Dec. 2018].

[6] D. E. Nikonov and I. A. Young, “Overview of Beyond-CMOS Devices and a Uniform Methodology for Their Benchmarking,” *Proc. IEEE*, vol. 101, no. 12, pp. 2498–2533, Dec. 2013. DOI: 10.1109/JPROC.2013.2252317.

[7] International Technology Roadmap for Semiconductors (ITRS), “Executive Reports 2015,” *ITRS*. [Online]. Available: http://www.itrs2.net/itrs-reports.html. [Accessed: 10-Dec. 2018].

[8] A. Jain and M. A. Alam, “Prospects of Hysteresis-Free Abrupt Switching (0 mV/decade) in Landau Switches,” *IEEE Trans. Electron Devices*, vol. 60, no. 12, pp. 4269–4276, Dec. 2013. DOI: 10.1109/TED.2013.2286997.

[9] V. V. Zhirnov and R. K. Cavin, “Nanoelectronics: Negative capacitance to the rescue?,” *Nat. Nanotechnol.*, vol. 3, no. 2, pp. 77–78, Feb. 2008. DOI: 10.1038/NNANO.2008.18.

[10] J. H. Park, G. S. Jang, H. Y. Kim, K. H. Seok, H. J. Chae, S. K. Lee, and S. K. Joo, “Sub-kT/q Subthreshold-Slope Using Negative Capacitance in Low-Temperature Polycrystalline-Silicon Thin-Film Transistor,” *Sci. Rep.*, vol. 6, no. 1, p. 24734, Jul. 2016. DOI: 10.1038/SREP24734.

[11] S. Salahuddin and S. Datta, “Use of Negative Capacitance to Provide Voltage Amplification for Low Power Nanoscale Devices,” *Nano Lett.*, vol. 8, no. 2, pp. 405–410, Feb. 2008. DOI: 10.1021/NL071804G.

[12] H. W. Then, S. Dasgupta, M. Radosavljevic, L. Chow, B. Chu-Kung, G. Dewey, S. Gardner, X. Gao, J. Kavalieros, N. Mukherjee, M. Metz, M. Oliver, R. Pillarisetty, V. Rao, S. H. Sung, G. Yang, and R. Chau, “Experimental observation and physics of

'negative' capacitance and steeper than 40mV/decade subthreshold swing in Al0.83In0.17N/AlN/GaN MOS-HEMT on SiC substrate," in *2013 IEEE International Electron Devices Meeting*, Dec. 2013, p. 28.3.1-28.3.4. DOI: 10.1109/IEDM.2013.6724709.

[13] R. K. Jana, G. L. Snider, and D. Jena, "On the possibility of sub 60 mV/decade subthreshold switching in piezoelectric gate barrier transistors," *Phys. Status Solidi Curr. Top. Solid State Phys.*, vol. 10, no. 11, pp. 1469–1472, 2013. DOI: 10.1002/PSSC.201300280.

[14] O. Y. Loh and H. D. Espinosa, "Nanoelectromechanical contact switches," *Nat. Nanotechnol.*, vol. 7, no. 5, pp. 283–295, 2012.

[15] J. O. Lee, Y.-H. Song, M.-W. Kim, M.-H. Kang, J.-S. Oh, H.-H. Yang, and J.-B. Yoon, "A sub-1-volt nanoelectromechanical switching device.," *Nat. Nanotechnol.*, vol. 8, no. 1, pp. 36–40, 2013.

[16] J. H. Kim, Z. C. Y. Chen, S. Kwon, and J. Xiang, "Three-terminal nanoelectromechanical field effect transistor with abrupt subthreshold slope," *Nano Lett.*, vol. 14, no. 3, pp. 1687–1691, 2014. DOI: 10.1021/NL5006355.

[17] N. Shukla, A. V Thathachary, A. Agrawal, H. Paik, A. Aziz, D. G. Schlom, S. K. Gupta, R. Engel-Herbert, and S. Datta, "A steep-slope transistor based on abrupt electronic phase transition," *Nat. Commun.*, vol. 6, p. 7812, Aug. 2015. DOI: 10.1038/NCOMMS8812.

[18] J. Song, J. Woo, S. Lee, A. Prakash, J. Yoo, K. Moon, and H. Hwang, "Steep Slope Field-Effect Transistors With Ag/TiO 2 -Based Threshold Switching Device," *IEEE Electron Device Lett.*, vol. 37, no. 7, pp. 932–934, Jul. 2016. DOI: 10.1109/LED.2016.2566661.

[19] S. Menzel, U. Bottger, M. Wimmer, and M. Salinga, "Physics of the Switching Kinetics in Resistive Memories," *Adv. Funct. Mater.*, vol. 25, no. 40, pp. 6306–6325, 2015. DOI: 10.1002/ADFM.201500825.

[20] S. Tappertzhofen, I. Valov, T. Tsuruoka, T. Hasegawa, R. Waser, and M. Aono, "Generic relevance of counter charges for cation-based nanoscale resistive switching memories," *ACS Nano*, vol. 7, no. 7, pp. 6396–6402, 2013. DOI: 10.1021/NN4026614.

[21] A. Wedig, M. Luebben, D.-Y. Cho, M. Moors, K. Skaja, V. Rana, T. Hasegawa, K. K. Adepalli, B. Yildiz, R. Waser, and I. Valov, "Nanoscale cation motion in TaOx, HfOx and TiOx memristive systems," *Nat. Nanotechnol.*, vol. 11, no. 1, pp. 67–74, 2015. DOI: 10.1038/NNANO.2015.221.

[22] C. Xu, Q. Xiao, J. Ma, Y. Jin, J. Shao, and Z. Fan, "High temperature annealing effect on structure, optical property and laser-induced damage threshold of Ta2O5 films," *Appl. Surf. Sci.*, vol. 254, no. 20, pp. 6554–6559, 2008. DOI: 10.1016/J.APSUSC.2008.04.034.

[23] P. Balakrishna Pillai, A. Kumar, X. Song, and M. M. De Souza, "Diffusion-Controlled Faradaic Charge Storage in High-Performance Solid Electrolyte-Gated Zinc Oxide Thin-

Film Transistors," *ACS Appl. Mater. Interfaces*, vol. 10, no. 11, pp. 9782–9791, Mar. 2018. DOI: 10.1021/ACSAMI.7B14768.

[24] Z. Ye, Y. Yuan, H. Xu, Y. Liu, J. Luo, and M. Wong, "Mechanism and Origin of Hysteresis in Oxide Thin-Film Transistor and Its Application on 3-D Nonvolatile Memory," *IEEE Trans. Electron Devices*, vol. 64, no. 2, pp. 438–446, 2017. DOI: 10.1109/TED.2016.2641476.

[25] P. Gallagher, M. Lee, T. A. Petach, S. W. Stanwyck, J. R. Williams, K. Watanabe, T. Taniguchi, and D. Goldhaber-Gordon, "A high-mobility electronic system at an electrolyte-gated oxide surface," *Nat. Commun.*, vol. 6, p. 6437, Mar. 2015. DOI: 10.1038/NCOMMS7437.

[26] J. Yoon, W. K. Hong, M. Jo, G. Jo, M. Choe, W. Park, J. I. Sohn, S. Nedic, H. Hwang, M. E. Welland, and T. Lee, "Nonvolatile memory functionality of ZnO nanowire transistors controlled by mobile protons," *ACS Nano*, vol. 5, no. 1, pp. 558–564, 2011. DOI: 10.1021/NN102633Z.

[27] B. Nasr, D. Wang, R. Kruk, H. Rosner, H. Hahn, and S. Dasgupta, "High-Speed, low-voltage, and environmentally stable operation of electrochemically gated zinc oxide nanowire field-effect transistors," *Adv. Funct. Mater.*, vol. 23, no. 14, pp. 1750–1758, 2013. DOI: 10.1002/ADFM.201202500.

[28] A. Lu, J. Sun, J. Jiang, and Q. Wan, "Low-voltage transparent electric-double-layer ZnO-based thin-film transistors for portable transparent electronics," *Appl. Phys. Lett.*, vol. 96, no. 4, p. 043114, Jan. 2010. DOI: 10.1063/1.3294325.

[29] J. Shulman, Y. Y. Xue, S. Tsui, F. Chen, and C. W. Chu, "General mechanism for negative capacitance phenomena," *Phys. Rev. B - Condens. Matter Mater. Phys.*, vol. 80, no. 13, pp. 1–6, 2009. DOI: 10.1103/PHYSREVB.80.134202.

[30] H. H. P. Gommans, M. Kemerink, and R. A. J. Janssen, "Negative capacitances in low-mobility solids," *Phys. Rev. B*, vol. 72, no. 23, p. 235204, Dec. 2005. DOI: 10.1103/PHYSREVB.72.235204.

[31] Y.-F. Wang, Y.-C. Lin, I.-T. Wang, T.-P. Lin, and T.-H. Hou, "Characterization and Modeling of Nonfilamentary Ta/TaOx/TiO2/Ti Analog Synaptic Device," *Sci. Rep.*, vol. 5, no. 1, p. 10150, Sep. 2015. DOI: 10.1038/SREP10150.

[32] N. F. Mott and R. W. Gurney, *Electronic processes in ionic crystals*. Oxford : Clarendon Press, 1940.

[33] S. Kim, S.-J. Kim, K. M. Kim, S. R. Lee, M. Chang, E. Cho, Y.-B. Kim, C. J. Kim, U.-I. Chung, and I.-K. Yoo, "Physical electro-thermal model of resistive switching in bi-layered resistance-change memory.," *Sci. Rep.*, vol. 3, p. 1680, 2013. DOI: 10.1038/SREP01680.

[34] W. Nernst, "Zur Kinetik der in Lösung befindlichen Körper," *Zeitschrift für Phys.*

Chemie, vol. 2U, no. 1, pp. 613–637, Jan. 1888. DOI: 10.1515/ZPCH-1888-0274.

[35] A. Einstein, "Über die von der molekularkinetischen Theorie der Wärme geforderte Bewegung von in ruhenden Flüssigkeiten suspendierten Teilchen," *Ann. Phys.*, vol. 322, no. 8, pp. 549–560, 1905. DOI: 10.1002/ANDP.19053220806.

[36] Y. W. Jeon, I. Hur, S. Kim, Y. Kim, M. Bae, H. K. Jung, D. Kong, W. Kim, J. Kim, H. Jang, J. Jang, J. Lee, D. M. Kim, and D. Hwan, "Physics-Based SPICE Model of a-InGaZnO Thin Film Transistor Using Verilog-A," *IEEE Electron Device Lett.*, vol. 33, no. 1, pp. 59–61, 2011. DOI: 10.1109/LED.2011.2172184.

[37] Y. W. Jeon, S. Kim, S. Lee, D. M. Kim, D. H. Kim, J. Park, C. J. Kim, I. Song, Y. Park, U. I. Chung, J. H. Lee, B. Du Ahn, S. Y. Park, J. H. Park, and J. H. Kim, "Subgap density-of-states-based amorphous oxide thin film transistor simulator (DeAOTS)," *IEEE Trans. Electron Devices*, vol. 57, no. 11, pp. 2988–3000, 2010. DOI: 10.1109/TED.2010.2072926.

[38] W. Kim, S. Menzel, D. J. Wouters, Y. Guo, J. Robertson, B. Roesgen, R. Waser, and V. Rana, "Impact of oxygen exchange reaction at the ohmic interface in Ta2O5-based ReRAM devices," *Nanoscale*, vol. 8, no. 41, pp. 17774–17781, 2016. DOI: 10.1039/C6NR03810G.

[39] C. M. Liu, W. L. Liu, W. J. Chen, S. H. Hsieh, T. K. Tsai, and L. C. Yang, "ITO as a Diffusion Barrier Between Si and Cu," *J. Electrochem. Soc.*, vol. 152, no. 3, pp. G234–G239, Apr. 2005. DOI: 10.1149/1.1860511.

[40] S. T. Lee, Z. Q. Gao, and L. S. Hung, "Metal diffusion from electrodes in organic light-emitting diodes," *Appl. Phys. Lett.*, vol. 75, no. 10, pp. 1404–1406, 1999. DOI: 10.1063/1.124708.

[41] A. R. Schlatmann, D. W. Floet, A. Hilberer, F. Garten, P. J. M. Smulders, T. M. Klapwijk, and G. Hadziioannou, "Indium contamination from the indium-tin-oxide electrode in polymer light-emitting diodes," *Appl. Phys. Lett.*, vol. 69, no. 12, pp. 1764–1766, 1996. DOI: 10.1063/1.117478.

[42] A. J. Bard and L. R. Faulkner, *Electrochemical Methods: Fundamentals and Applications*. Wiley, 2001.

[43] M. Moors, K. K. Adepalli, Q. Lu, A. Wedig, C. Bäumer, K. Skaja, B. Arndt, H. L. Tuller, R. Dittmann, R. Waser, B. Yildiz, and I. Valov, "Resistive Switching Mechanisms on TaOx and SrRuO3 Thin-Film Surfaces Probed by Scanning Tunneling Microscopy," *ACS Nano*, vol. 10, no. 1, pp. 1481–1492, Jan. 2016. DOI: 10.1021/ACSNANO.5B07020.

[44] I. Valov, E. Linn, S. Tappertzhofen, S. Schmelzer, J. van den Hurk, F. Lentz, and R. Waser, "Nanobatteries in redox-based resistive switches require extension of memristor theory," *Nat. Commun.*, vol. 4, p. 1771, Apr. 2013. DOI: 10.1038/NCOMMS2784.

[45] M. Lübben, P. Karakolis, V. Ioannou-Sougleridis, P. Normand, P. Dimitrakis, and I.

Valov, “Graphene-Modified Interface Controls Transition from VCM to ECM Switching Modes in Ta/TaOx Based Memristive Devices,” *Adv. Mater.*, vol. 27, no. 40, pp. 6202–6207, Oct. 2015. DOI: 10.1002/ADMA.201502574.

[46] A. Siemon, T. Breuer, N. Aslam, S. Ferch, W. Kim, J. van den Hurk, V. Rana, S. Hoffmann-Eifert, R. Waser, S. Menzel, and E. Linn, “Realization of Boolean Logic Functionality Using Redox-Based Memristive Devices,” *Adv. Funct. Mater.*, vol. 25, no. 40, pp. 6414–6423, Oct. 2015. DOI: 10.1002/ADFM.201500865.

[47] K. Skaja, C. Bäumer, O. Peters, S. Menzel, M. Moors, H. Du, M. Bornhöfft, C. Schmitz, V. Feyer, C. L. Jia, C. M. Schneider, J. Mayer, R. Waser, and R. Dittmann, “Avalanche-Discharge-Induced Electrical Forming in Tantalum Oxide-Based Metal-Insulator-Metal Structures,” *Adv. Funct. Mater.*, vol. 25, no. 46, pp. 7154–7162, 2015. DOI: 10.1002/ADFM.201502767.

[48] J. P. Duarte, S. Khandelwal, A. I. Khan, A. Sachid, Y. Lin, H. Chang, S. Salahuddin, and C. Hu, “Compact models of negative-capacitance FinFETs: Lumped and distributed charge models,” in *2016 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2016, vol. 5, no. 2, p. 30.5.1-30.5.4. DOI: 10.1109/IEDM.2016.7838514.

Chapter 8 Conclusions and Future Work

8.1. CONCLUDING REMARKS

This thesis explores potential pathways for continual improvement in energy efficiency and processing capabilities of semiconductor devices and provides possible solutions to the societal challenges over the coming decade. Chapter 1 introduces these challenges and possible solutions and their applicability. In particular, two main directions for achieving these goals are discussed: 1) Realisation of high performance p-channel MOSHFET in GaN to implement an on-chip power CMOS based gate driver for power devices, and 2) employing band-to-band tunnelling or negative capacitance mechanisms to achieve less than 60 mV/dec of subthreshold swing. A summary of ideas covered in different chapters of this thesis is as follows:

1. In chapter 2, the operation of a paraelectric FET is described, whereby it is demonstrated that these device can also exhibit sub-60 mV/dec of operation, during the backward sweep of a dynamic gate bias.
2. In chapters 4 and 5, the performance of p-channel devices in GaN is analysed. The inherent presence of 2DHG coupled with poor mobility of holes in GaN in conventional p-channel devices in GaN leads to severe trade-off between on-current and threshold voltage, making it difficult to maintain high performance in the E-mode operation of the device. Utilisation of AlGaN cap and biasing the underlying 2DEG are shown to locally deplete the 2DHG under the gate and reduce the off-current, making it feasible to have high $|V_{th}|$ and $|I_{ON}|$.
3. In chapter 6, a vertical p-channel tunnel FET in GaN for achieving less than 60 mV/dec of subthreshold swing is proposed. Due to a large band gap, the utilisation of polarisation charge to facilitate band-to-band tunneling becomes

necessary in GaN. Whilst the conventional TFETs suffer from ambipolarity, the transfer characteristics of the presented device show ambipolar-free characteristics, owing to the polarisation induced tunnelling junction (PITJ). Moreover, a study of the band diagrams at different gate biases confirms a better electrostatic control over the region of tunnelling, which remains pinched to the location of the PITJ. In contrast, in a conventional TFET, the region of tunnelling tends to move away as the gate bias is increased, thereby making it difficult for the gate to modulate the tunnelling region.

4. In chapter 7, another mechanism of surpassing 60 mV/dec of subthreshold swing is explored that relies upon the generation of negative capacitance in the gate dielectric. The materials with inherent instability, such as ferroelectrics, are popularly known to exhibit the negative capacitance. Ferroelectric FETs, employing a ferroelectric material in the gate dielectric stack have been demonstrated to achieve sub-60 mV/dec of switching in the literature. In this chapter, a novel mechanism of achieving the negative capacitance operation in Ta_2O_5/ZnO solid-electrolyte (SE)-FET, which originates from the movements of oxygen ions inside Ta_2O_5, is explored and modelled.

8.2. FUTURE WORK

Apart from the calibration of the model with the experimental results, the analysis carried out in chapters 4, 5, and 6 has been for the most part theoretical. Therefore, an immediate next step for these works is to fabricate proposed p-channel MOSHFET with AlGaN cap and p-channel HTFET employing PITJ and analyse additional issues that might arise in the realisation of these devices and factors that can deteriorate the performance of these devices in practice. Examples of such difficulties can be associated with the uncertainty in the thickness of GaN channel in p-channel MOSHFET, resulting

from the poor control of etching while selectively removing the p-GaN layer before a regrowth of AlGaN cap, or introduction of various defects during the fabrication, such as traps and dislocations and resulting trap-assisted tunneling that could degrade the subthreshold swing in the case of TFET.

Advancements in the growth of gate oxide are necessary to control and lower the impact of trap states at various interface between oxide/AlGaN cap and oxide/GaN, while at the same time lower the gate leakage current through the oxide, for a reliable and replicable operation of these devices. The MOCVD growth of Mg doped p-GaN layer currently suffers from, large activation energy $(120 - 200\ meV)$ of Mg dopants and memory effect, leading to poor hole density in p-GaN and a broader doping profile. Moreover, during the epitaxial growth at high temperature, Mg ions can diffuse into the GaN layer underneath, thus contributing to the leakage current and affecting the minimum thickness that can be achieved in manufacture. Hence, novel doping techniques are required to obtain p-GaN layers capable of producing high hole density as well as sharper doping profile.

Other possibilities to boost the performance of p-type devices in GaN include improving the hole mobility by tailoring the valence band structure in GaN, for example by application of stress to lower the effective mass of holes; an E-mode operation with high $|V_{th}|$ can be obtained by introduction of positive ions directly in the gate oxide to deplete the hole gas underneath, thereby eliminating the regrowth of AlGaN cap altogether.

The negative capacitance phenomena in Ta_2O_5/ZnO TFT reported in chapter 7, is currently limited to only small (mHz) frequency range. To make this phenomenon work at higher frequency would require a boost in the mobility of oxygen ions present within Ta_2O_5. This can be achieved by either altering the growth conditions for Ta_2O_5 or

utilising alternative solid-electrolyte with higher mobility of ionic species. On the modelling side, the presented model for SE-FET is currently one-dimensional; it only accounts for changes in the ionic and carrier densities along the vertical directions. This greatly limits the applicability of the model where the role of other factors along the lateral direction are of interest, such as, non-uniform distribution of V_{DS} along the channel and capacitance introduced by the source and drain contact pads.

Currently, the model only takes into account the movement of oxygen ions, assuming that an accumulation of ions at one interface results in the formation of an equivalent mirror charge at the opposite interface due to the vacancies, while ignoring the motion of these vacancies. This assumption holds good owing to the comparatively smaller mobility of oxygen vacancies, however, a more accurate approach would require including the dynamics of both oxygen ions and vacancies. In addition, the model assumes the profile of accumulated oxygen ions at the gate-insulator interface decays linearly in order to simplify the diffusion term in the drift-diffusion equation. This could result in the model unable to properly capture the rise or decay of the drain current with time during a pulsed gate bias measurement. Therefore, a complete solution is demanded that self-consistently couples the drift-diffusion phenomenon of doubly charged ions and vacancies inside the gate dielectric with the Fermi distribution of electrons inside the semiconductor.

Appendix

Table A1. Parameters for Ta_2O_5 used in the drift-diffusion model presented in Chapter 7.

Input Parameters		
Parameters	**Values**	
$\epsilon_{Ta_2O_5}$	20.8	
$\mu_{ion,0}\ (cm^2/Vs)$	1×10^{-11}	
$v_{sat}\ (cm/s)$	3.64×10^{-6}	
β	0.5	
$Q_{ox,0}\ (\mu C/cm^2)$	37	
Thickness $Ta_2O_5\ (nm)$	**120**	**275**
$n_{ion}\ (cm^{-3})$	1.3×10^{18}	5.2×10^{18}
$x_{D,0}\ (nm)$	20	22

The reported $\mu_{ion,0}$ in the above table corresponds to a diffusion coefficient $D(= kT\mu_{ion}/q_z)$ of $1.3 \times 10^{-13} cm^2/s$, which is in good agreement with the theoretically computed diffusion coefficient ($= 3.5 \times 10^{-13} cm^2/s$) for oxygen vacancy migration [1], and cross-verified using Chronoamperometry data of gate current that can be defined using the Cottrell equation [2] which has been reported elsewhere [3]. The value of diffusion thickness x_D is obtained by matching the model results with experiment.

Table A2. Parameters for ZnO used in the 1D Poisson solver.

Parameter	Value	Description
N_{TA}	$6.75 \times 10^{19} eV^{-1} cm^{-3}$	Acceptor-like tail state
kT_{TA}	$0.05\ eV$	Acceptor-like tail state slope
N_{DA}	$3.0 \times 10^{16} eV^{-1} cm^{-3}$	Acceptor-like deep state
kT_{DA}	$0.8\ eV$	Acceptor-like deep state slope
N_{GA}	$4 \times 10^{18} eV^{-1} cm^{-3}$	Acceptor-like Gaussian state
μ_{GA}	$0.5\ eV$	Mean of acceptor-like Gaussian state
σ_{GA}	$0.39\ eV$	Standard deviation of acceptor-like Gaussian state
N_{TD}	$1 \times 10^{20} eV^{-1} cm^{-3}$	Donor-like tail state
kT_{TD}	0.1 eV	Donor-like tail state slope
N_{DD}	$5 \times 10^{16} eV^{-1} cm^{-3}$	Donor-like deep state
kT_{DD}	0.8 eV	Donor-like deep state slope
N_{GD}	$1 \times 10^{19} eV^{-1} cm^{-3}$	Donor-like Gaussian state
μ_{GD}	$0.5\ eV$	Mean of donor-like Gaussian state
σ_{GD}	$0.32\ eV$	Standard deviation of donor-like Gaussian state
N_C	$1e19\ cm^{-3}$	conduction band density of states
N_V	$8e16\ cm^{-3}$	valence band density of states
E_G	$3.35\ eV$	band gap
μ_{ZnO}	$4\ cm^2/Vs$	electron mobility
ϵ_{ZnO}	7.5	dielectric constant

The key factors affecting the drain current in amorphous oxide semiconductors (AOS) are the density of acceptor-like tail states N_{TA} and corresponding tail-state slope kT_A.We have considered values which lie in the range commonly reported for ZnO and $InGaZnO$ TFTs, $1.3 \times 10^{19} - 2.85 \times 10^{20}\ eV^{-1}cm^{-3}$ for N_{TA}, and $0.030 - 0.059\ eV$ for kT_A [4]–[6]. The values of acceptor- and donor- like deep states and donor-like tail states (N_{DA}, N_{DD}, N_{TD}) their corresponding slopes (kT_{DA}, kT_{DD}, kT_{TD}), are adjusted from the values in Ref. [7] to match with experiment. Conventional techniques are unsuitable to extract the mobility of these transistors due to enhancement and memory effects. A value of 4 cm^2/Vs was obtained by a fit to the drain current [8], [9].

REFERENCES

[1] H. Jiang and D. A. Stewart, "Enhanced oxygen vacancy diffusion in Ta2O5 resistive memory devices due to infinitely adaptive crystal structure," *J. Appl. Phys.*, vol. 119, no. 13, p. 134502, Apr. 2016. DOI: 10.1063/1.4945579.

[2] A. J. Bard and L. R. Faulkner, *Electrochemical Methods: Fundamentals and Applications*. Wiley, 2001.

[3] P. Balakrishna Pillai, A. Kumar, X. Song, and M. M. De Souza, "Diffusion-Controlled Faradaic Charge Storage in High-Performance Solid Electrolyte-Gated Zinc Oxide Thin-Film Transistors," *ACS Appl. Mater. Interfaces*, vol. 10, no. 11, pp. 9782–9791, Mar. 2018. DOI: 10.1021/ACSAMI.7B14768.

[4] K. Takechi, M. Nakata, T. Eguchi, H. Yamaguchi, and S. Kaneko, "Application of the Meyer–Neldel Rule to the Subthreshold Characteristics of Amorphous InGaZnO4 Thin-Film Transistors," *Jpn. J. Appl. Phys.*, vol. 48, no. 7, p. 078001, Jul. 2009. DOI: 10.1143/JJAP.48.078001.

[5] F. Torricelli, J. R. Meijboom, E. Smits, A. K. Tripathi, M. Ferroni, S. Federici, G. H. Gelinck, L. Colalongo, Z. M. Kovacs-Vajna, D. de Leeuw, and E. Cantatore, "Transport Physics and Device Modeling of Zinc Oxide Thin-Film Transistors Part I: Long-Channel Devices," *IEEE Trans. Electron Devices*, vol. 58, no. 8, pp. 2610–2619, Aug. 2011. DOI: 10.1109/TED.2011.2155910.

[6] S. Lee, K. Ghaffarzadeh, A. Nathan, J. Robertson, S. Jeon, C. Kim, I.-H. Song, and U.-I. Chung, "Trap-limited and percolation conduction mechanisms in amorphous oxide semiconductor thin film transistors," *Appl. Phys. Lett.*, vol. 98, no. 20, p. 203508, May 2011. DOI: 10.1063/1.3589371.

[7] Y. W. Jeon, I. Hur, S. Kim, Y. Kim, M. Bae, H. K. Jung, D. Kong, W. Kim, J. Kim, H. Jang, J. Jang, J. Lee, D. M. Kim, and D. Hwan, "Physics-Based SPICE Model of a-InGaZnO Thin Film Transistor Using Verilog-A," *IEEE Electron Device Lett.*, vol. 33, no. 1, pp. 59–61, 2011. DOI: 10.1109/LED.2011.2172184.

[8] K. Nomura, T. Kamiya, and H. Hosono, "Highly stable amorphous In-Ga-Zn-O thin-film transistors produced by eliminating deep subgap defects," *Appl. Phys. Lett.*, vol. 99, no. 5, pp. 10–13, 2011. DOI: 10.1063/1.3622121.

[9] P. F. Carcia, R. S. McLean, and M. H. Reilly, "High-performance ZnO thin-film transistors on gate dielectrics grown by atomic layer deposition," *Appl. Phys. Lett.*, vol. 88, no. 12, pp. 2004–2007, 2006. DOI: 10.1063/1.2188379.