

All-GaN Integrated Cascode Configuration

by

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Abstract

GaN based power device, due to its superior material properties, have attracted much attention. Remarkable progresses have been made in realising normally-off operations and improving the overall performance as power switches. GaN + Si cascode features reduced Miller-effect that improves the switching speed and hence efficiency compared to conventional Si MOSFETs. This study proposes a novel all-GaN integrated cascode combining the advantages of the GaN enhancement mode device and the cascode configuration.

An all-GaN integrated cascode heterojunction field effect transistor was designed and fabricated for power switching applications. A threshold voltage of +2 V was achieved using a fluorine implant treatment and a metal-insulator-semiconductor gate structure. An output current of 300 mA/mm was optimised by matching the current drivability of the enhancement and depletion mode parts. For the first time, we demonstrate the switching speed advantage of the cascode over equivalent GaN standalone devices using double pulse tester at 200 V.

A comprehensive understanding of switching behaviour of an integrated cascode is presented. Analysis shows that speed advantage originates from the reduced Miller-effect leading to larger charging (discharging) current of the output capacitance. A small ratio of the gate driving current to the load current was found to enhance the advantage. However, the additional capacitance loss at the internode needs to be minimised.

Field plate geometries were found to be effective in suppressing the dynamic R_{on} and reducing the Miller capacitance. Experimental and simulated results suggested that the cascode with a field plate connected to the source can significantly suppress the additional capacitance energy loss at the internode due to the reduced drain-source capacitance of the depletion mode device. While devices with the field plate connecting to the E-mode gate exhibit an improved switching controllability via gate resistance during turn-off.

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1 Introduction

1.1 Introduction to AlGaN/GaN heterostructure field effect transistors

In the past two decades, GaN based power transistors have been intensively investigated due to the superior material properties, as shown in Table 1-1 [1-2]. Compared to Si, with larger bandgap (E_g), higher breakdown field (E_{br}) and higher electron saturation velocity (v_{sat}) allows its power devices to have higher breakdown voltage and can operate at higher frequency [1]. GaN is also advantageous over SiC, another wide bandgap material with similar material properties, due to the ability to form heterojunctions and achieve heterostructure field effect transistors (HFETs). AlGaN/GaN based HFETs feature high sheet carrier concentration and electron mobility (μ_n) at the same time due to the presence of a two-dimensional electron gas (2DEG) at the interface of the heterostructure. While the conventional Si and SiC metal oxide semiconductor field effect transistors (MOSFETs) can achieve similar carrier concentration in the inversion layer compared to that in the 2DEG, AlGaN/GaN HFETs have significantly high electron channel mobility ($\sim 2000 \text{ cm}^2/\text{Vs}$), up to 50 times larger compared to that ($\sim 40 \text{ cm}^2/\text{Vs}$) for SiC MOSFETs [2]. This leads to lower channel resistance and higher current density for the AlGaN/GaN HFETs. These altogether have made GaN devices one of most promising candidates to replace Si based in high power high frequency applications.

Table 1-1 Selected material properties related to power devices

	E_g (eV)	E_{br} (MV/cm)	v_{sat} (cm/s)	μ_n (cm^2/Vs)
Si	1.1	0.3	1E7	1350
GaN	3.39	3.3	2.5E7	2000 (2DEG)
SiC	3.26	3.0	2E7	700

1.1.1 Basic AlGaN/GaN HFETs

Figure 1-1 shows a simplified schematic diagram of an AlGaN/GaN HFET. The basic layer structure of the device consists of a substrate (Si in this study), a buffer layer to accommodate the lattice mismatch between the substrate and GaN, an unintentionally doped GaN layer and an AlGaN barrier. With the proper thickness of AlGaN ($\sim 20 \text{ nm}$) and Al composition ($\sim 30\%$) [3], A 2DEG is formed at the

interface of the AlGa_N/Ga_N layer (in the Ga_N layer) and serves as the channel of the device. On top of the structure, two ohmic metal source and drain contacts are formed to make electrical contact to the 2DEG and one Schottky contact, called the gate, is deposited to control the channel conductivity. The device normally displays a depletion-mode (D-mode) operation due to the high carrier density of the 2DEG which cannot be depleted by an unbiased Schottky gate [2].

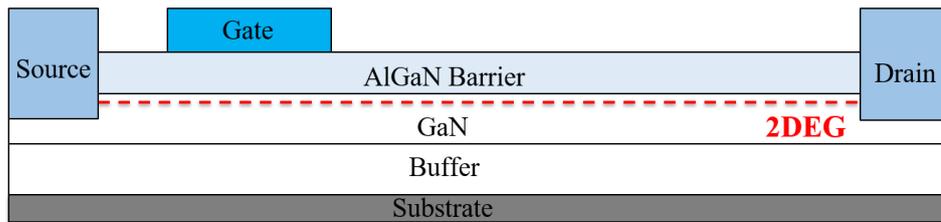


Figure 1-1 Schematic of a typical AlGa_N/Ga_N HFET.

1.1.2 Origin of the 2DEG

The formation of the 2DEG originates from the spontaneous polarisation and the piezoelectric polarisation. The spontaneous polarisation is material related and exists due to the lack of inversion symmetry in the Wurtzite structure of Ga_N [3]. As shown in Figure 1-2(a), the Ga-N bond along the c-axis (0001) is shorter than other three bonds, due to the smaller height of the tetrahedron compared to that of a regular tetrahedron [2]. As a result, the spontaneous polarisation is produced. It peaks along c-axis (0001) and induces negative charge at the Ga-face (0001) and positive charge at the N-face nitrides (000-1). In addition, it is larger in AlN compared to Ga_N and increases with Al composition [3]. On the other hand, systems with cubic crystal structure such as GaAs has no spontaneous polarisation along any direction because the sp^3 tetrahedron is regular tetrahedron [2], as illustrated in Figure 1-2(b). For Ga-face AlGa_N/Ga_N heterostructures as shown in Figure 1-3, the spontaneous polarisation is negative and points towards the substrate [3]. Due to the polarisation difference in the AlGa_N and Ga_N layer, the negative charge in the Ga_N layer at the interface can only partially compensate the positive charge in the AlGa_N barrier, leaving a net positive charge at the interface of the AlGa_N/Ga_N heterostructure [3]. Electrons accumulate and are confined at the interface of the AlGa_N/Ga_N layer due to this positive polarisation charge and the 2DEG is formed. The piezoelectric polarisation, on the other hand, mainly exists in the AlGa_N barrier

due to the smaller lattice constant of AlGa_xN compared to GaN, leading to a tensile strain in the AlGa_xN layer [3]. It is parallel with the spontaneous polarisation and thus increases the total polarisation effect. Unlike AlGaAs/GaAs HFET, which does not have the polarisation effect because of cubic crystal structure and needs doping to optimise the band offset, AlGa_xN/GaN HFET utilises this polarisation effect to form 2DEG, and thus does not have to worry about about the problems caused by doping such as impurity scattering.

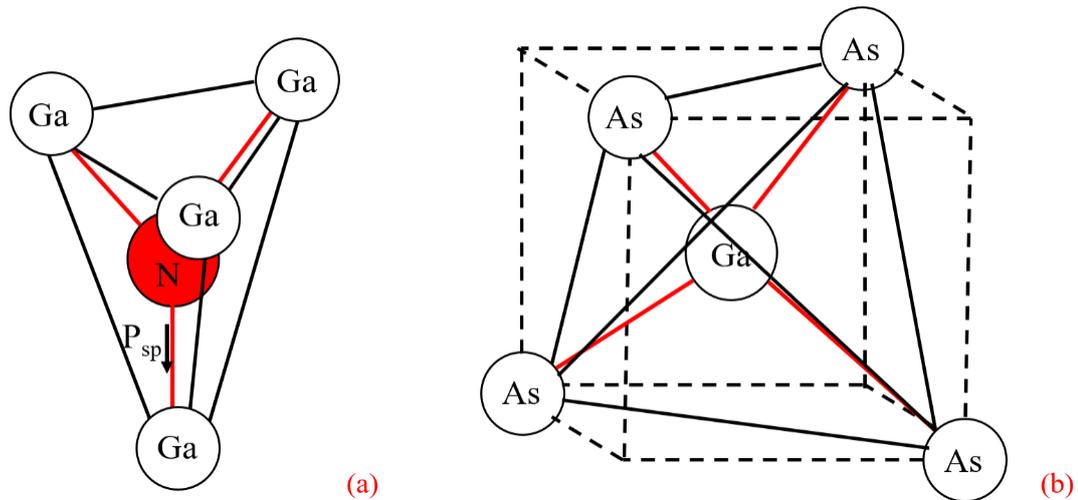


Figure 1-2 Schematic diagram of (a) a Ga tetrahedron in hexagonal wurtzite GaN and (b) a tetrahedron in zinc blende GaAs.

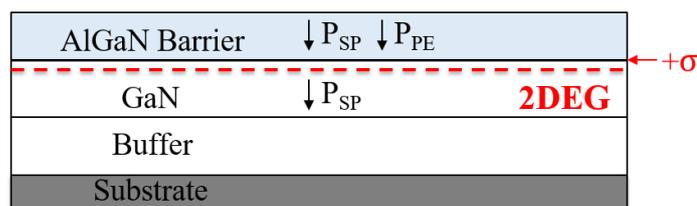


Figure 1-3 Polarisation effect in Ga-face AlGa_xN/GaN heterostructure.

To maintain the charge neutrality in the structure under the condition of no external electric field, the following expression is valid, assuming a completely un-doped AlGa_xN layer and no buffer charges,

$$\sigma_{surface} = qn_s \cdot \quad (1-1)$$

Where $\sigma_{surface}$ is the total ionised donor-like surface states and n_s is the carrier density in the 2DEG [4]. Therefore, the source of electrons in the 2DEG is believed to be the donor-like surface states in the AlGaN barrier [4]. A 2DEG concentration of 10^{13}cm^{-2} can be typically achieved with Al mole fraction of 20% and AlGaN thickness of 20 nm [3].

The band diagram of the AlGaN/GaN heterostructure at equilibrium is shown in Figure 1-4. The constant slope across the AlGaN layer results from the polarisation effect, which leads to a net negative charge at the surface and a net positive charge at the interface. ΔE_C is the conduction band offset between AlGaN and GaN. The discontinuity of the conduction band forms the quantum well in the GaN layer at the interface with an approximately triangular shape.

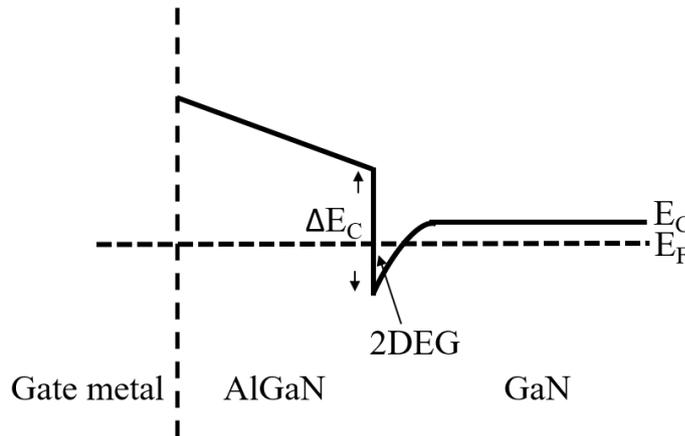


Figure 1-4 Conduction band diagram of AlGaN/GaN heterostructure.

1.1.3 Important parameters

1.1.3.1 Drain current (I_{DS})

I_{DS} represents the drain current of the HFET and can be estimated by the following equation,

$$I_{DS} = n_s * q * v_{eff} \quad (1-2)$$

where n_s is the sheet density, q is the electronic charge and v_{eff} the effective electron velocity. The drain current increases linearly at low drain-source bias (limited by the channel and contact resistances) and saturates after the gate-drain junction starts to pinch-off, at which point the current is limited by the almost constant injection rate

of channel electrons into the channel depletion region. Compared to a standard FET, the sheet concentration, n_s , can be high with a correspondingly high v_{eff} (mobility) and hence higher channel conductance. n_s can be increased by maximising the polarisation effect and optimising the barrier thickness, and thus the maximum current drivability can be improved. I_{DS} is often normalised to unit gate width (mA/mm) to compare between different devices.

1.1.3.2 On resistance (R_{on})

R_{on} determines the conduction loss and thus is critical for power switching devices. It is extracted from the linear region of the I-V characteristic. R_{on} consist of the ohmic contact resistance and the channel resistance. Channel resistance can be trade-off with breakdown voltage, by optimising the gate drain separation. While ohmic contact resistance can be reduced by improving the ohmic metal deposition technique. R_{on} is often normalised to unit gate width (Ω *mm) for comparison.

1.1.3.3 Breakdown voltage (V_{br})

V_{br} refer to the voltage at which the off-state leakage current exceeds a certain level (e.g. 1 μ A/mm). It is also important to power switching devices as it determines the maximum voltage handling. V_{br} can be improved by increasing the gate drain separation, at the expense of increased R_{on} . GaN HFETs for power applications also implements field plates to modulate the electric field underneath to improve the breakdown voltage. Optimisation of the field plate geometries is required to control the field plate induced capacitance.

1.1.3.4 Gate charge (Q_G)

Due to the non-linearity of the intrinsic capacitance with the increase of the drain bias, Q_G is often used instead, as the main indicator of the switching speed and switching energy loss for the device. Together with the on-resistance, the product (R_{on} * Q_G) represents the Figure of Merit for power switching devices. Q_G can be extracted by the integration of gate current over charging time during turn-on switching transient. Alternatively, Q_G can be estimated by the integration of capacitance over drain voltage during C-V measurements. Optimisation of the field plate geometries is important to minimise the gate charge and improve the switching speed.

1.2 Development of AlGaIn/GaN HFETs towards power switches

1.2.1 Enhancement-mode operation

Power applications require an enhancement-mode (E-mode) operation for the device due to safety reasons when a power failure occurs [2]. A higher threshold voltage (V_{th}) preferably above +3 V is favourable for better noise immunity. [5] has discussed the Miller turn-on issue that can cause unwanted turn-on of the device and increase the energy loss in typical inductive load power switching applications. On the other hand, the conventional AlGaIn/GaN HFETs are originally D-mode devices due to the high carrier density in the 2DEG and requires additional negative gate bias to pinch off. As a result, numerous efforts have been made in demonstrating the E-mode operation at the early stages of the development of AlGaIn/GaN power devices [6-16].

Applying a p-GaN or p-AlGaIn layer between the gate metal and AlGaIn barrier to achieve E-mode operation was first reported in [6]. This technology requires an additional p-type layer (GaN or AlGaIn) grown on top of the AlGaIn barrier [6-8]. The p-type is achieved by doping with Mg to replace the Ga atom [2] [7-8]. Figure 1-5(a) shows a schematic diagram of a typical p-GaN HFET. The p-type layer is etched away except for the region between the gate metal and AlGaIn barrier. As a result, the conduction band of the AlGaIn at the AlGaIn/GaN interface is lifted above Fermi level and E-mode operation can be achieved, as illustrated in the conduction band diagram in Figure 1-5(b). The threshold voltage can be shifted up to +2 V without any gate dielectric [7] and over +7 V with a metal-insulator-semiconductor (MIS) gate structure [8]. The drawbacks are the limited solubility of Mg doping, the selective etching of the p-type layer and gate leakage issue due to the turn-on of p-type gate at high gate bias. Nevertheless, it is a relatively easy process with fewer fabrication steps. Also, there is no need for a gate dielectric, which would otherwise cause a V_{th} instability issue due to the interfacial traps between the gate dielectric and AlGaIn barrier [17]. Therefore, it has become one of the major E-mode techniques and has been adopted for the first commercially available GaN standalone E-mode devices such as EPC eGaN devices, GaNsystem 650 V power devices and Panasonic gate injection transistors (GIT) [7].

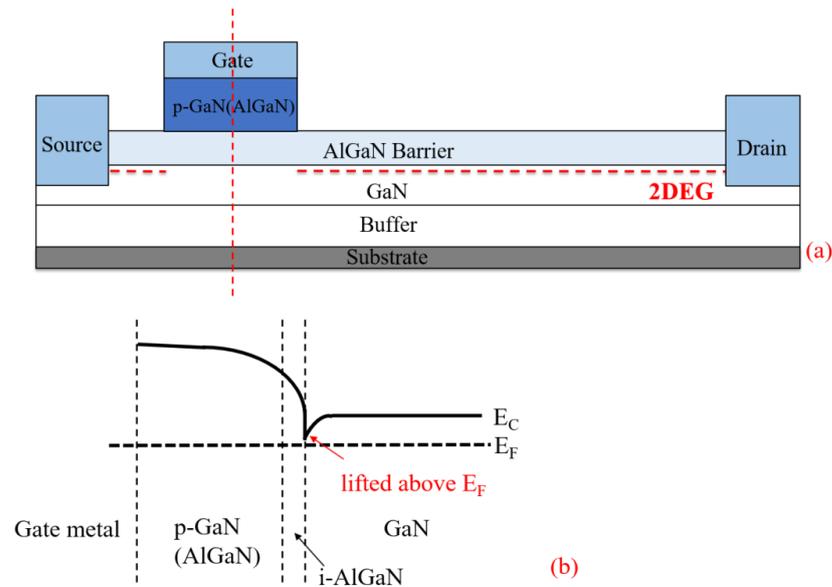


Figure 1-5 (a) A schematic diagram of a p-GaN(AlGaN) HFET and (b) an illustration of the conduction band along the gate.

Alternatively, fluorine treatment in the gate region in the AlGaN barrier can also achieve E-mode operation for GaN HFETs, as firstly reported in [9]. The technology utilises CF_4 based plasma to treat the AlGaN layer and incorporate fluorine ions into the barrier. Figure 1-6(a) shows the device structure of fluorine treated GaN E-mode device. The fluorine ions have strong electronegativity and act as fixed negative charge, therefore modulate the energy band of the AlGaN barrier and the 2DEG, as shown in the corresponding conduction band diagram in Figure 1-6(b). A positive threshold voltage of +0.9 V can be achieved as reported in [9] with F- implantation only. Compared to the p-type gate technology, the fluorine treatment has less requirement in growth as it does not require a p-type layer which is difficult to grow and also challenging to selective etch. However, for better noise immunity in power switching applications, an MIS gate structure is required to further increase the threshold voltage to over +3 V [18-19]. The use of a gate dielectric can cause V_{th} instability issues and becomes the major limitation of the fluorine based technique [17]. In addition, the stability of the F- ions in the AlGaN barrier under electrical and thermal stress may need further investigation [10].

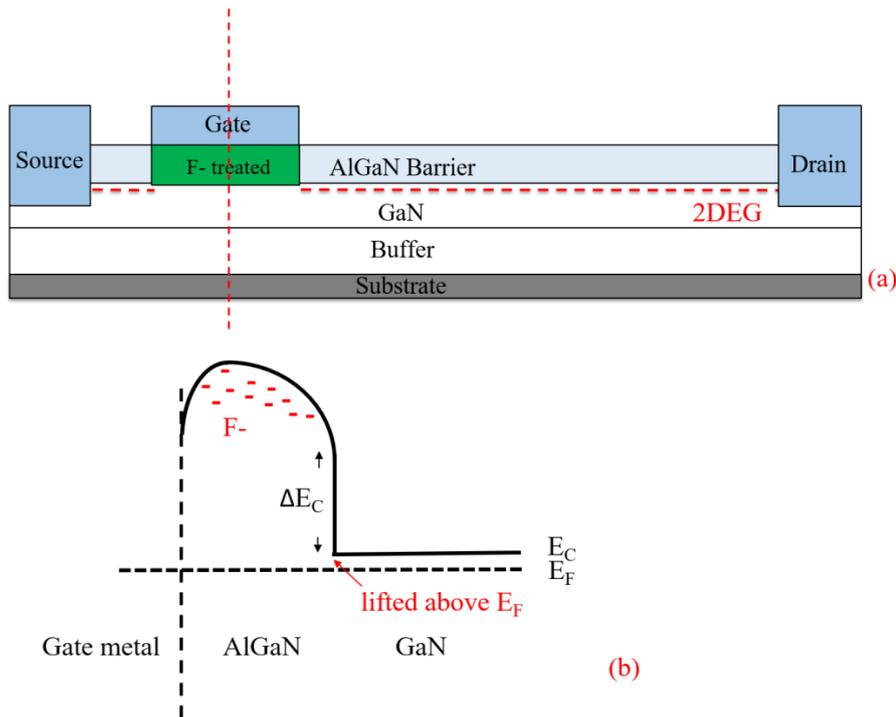


Figure 1-6 (a) A schematic diagram of a fluorine implanted GaN HFET and (b) an illustration of the conduction band along the gate.

Other techniques including gate-recessing [11], GaN MOSFET [12-15], and thin AlGaN barrier [16] can achieve E-mode operation in GaN HFETs by either reducing the AlGaN barrier thickness or completely removing the AlGaN barrier at the gate region. Figure 1-7(a) shows a schematic diagram of the recessed-gate GaN HFETs. The decreased AlGaN thickness causes the reduction in 2DEG density [2], and hence the threshold can be shifted to positive values [11]. The AlGaN barrier under the Schottky gate is often dry etched by inductive coupled plasma reactive ion etching (ICPRIE) or reactive ion etching (RIE). As a result, the gate-recessing approach is subject to dry etching plasma damage, which increases the gate leakage and limits the breakdown voltage [9]. Compared to the conventional gate recessing method, GaN MOSFET techniques fully recess the gate by completely removing the AlGaN barrier, as shown in Figure 1-7(b). A gate dielectric is then deposited, and an inversion layer can be created to form the channel of the device at high gate bias. It is a robust technique to achieve E-mode operation with threshold voltage close to +3 V, reported by different groups [12-13]. However, this approach can suffer from low channel mobility and may not be able to exploit the full potential of GaN HFETs.

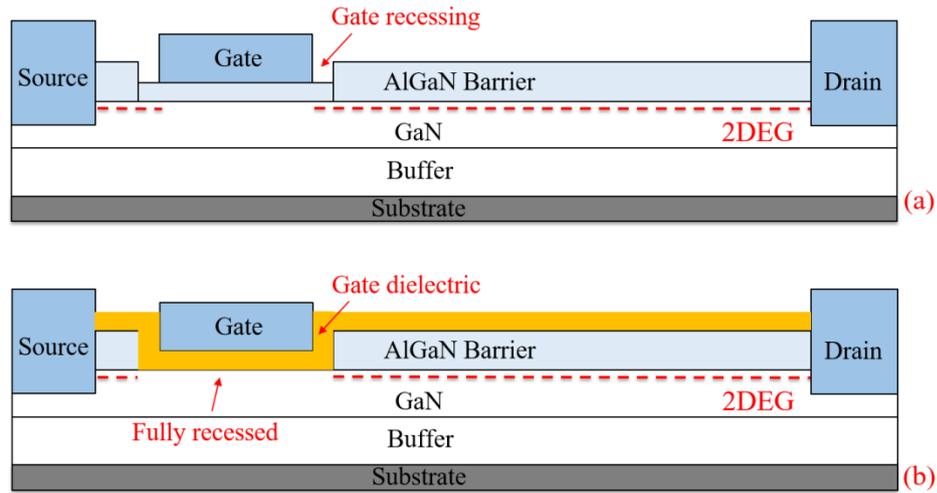


Figure 1-7 Schematic diagram of E-mode GaN HFETs with (a) gate recessing and (b) GaN MOSFET technique.

1.2.2 Buffer design for high voltage operation

Recent improvements in the buffer structure to withstand high voltage is critical to the development of AlGaIn/GaN power transistors [20-22]. Figure 1-8 shows a widely adopted buffer layer structure on a Si substrate for high voltage AlGaIn/GaN HFETs [20-22]. Si substrates are the main scope in this study due to its large wafer size and are CMOS compatible, leading to much lower cost compared to SiC or sapphire substrates [21]. To start the growth, a nucleation layer of AlN is used to form a barrier between Si and Ga to avoid their reaction at high growth temperature [20]. This is followed by a strain relief layer of either a superlattice [22] or compositionally graded AlGaIn layer [20] to accommodate the large lattice and thermal expansion coefficient mismatch between Si and GaN. The strain relief layer introduces compressive stress to compensate the tensile stress caused by the cooling process during growth, and hence minimises the wafer bowing and reduces cracks. A semi-insulating C-doped GaN buffer with doping level above 10^{18} cm^{-2} is often used upon the strain relief layer to enhance the resistivity of the buffer and prevent lateral ‘punch through’ at high voltage (600 V) [21-22]. C acts as deep-acceptor and is needed in the buffer to compensate the nitrogen vacancies, which are believed to be the main source of donors which decrease the breakdown voltage. Before the AlGaIn barrier, an unintentionally doped GaN layer is grown to keep the C acceptor away from the 2DEG as it can reduce the 2DEG density [20].

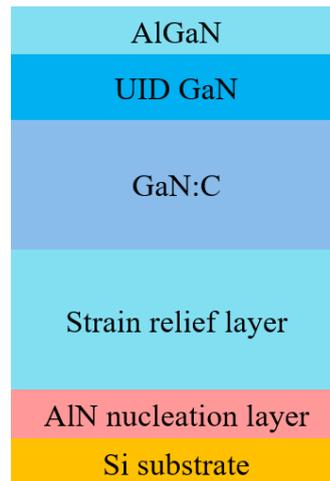


Figure 1-8 A typical C-doped buffer layer structure for AlGaN/GaN power transistors.

1.2.3 Optimisation for low switching energy loss

600 V GaN HFETs are reported to be over 20 times less in the input switching figure of merit ($R_{on} * Q_{iss}$) and close to 10 times less in output switching figure of merit ($R_{on} * Q_{oss}$) compared to the best 600 V Si SJ MOSFET [23]. The comparison suggests that GaN HFETs can operate at much higher frequency. This can bring advantages as the value of the impedances of the passive components, capacitors and inductors, drop and increase, respectively, with the increase of the operating frequency. The effectiveness of these components to reduce ripple therefore increases with frequency and the required physical size reduces compared to that at lower frequencies [23-25]. However, as the switching frequency increases, the switching energy loss starts to dominate compared to the conduction loss [23]. As a result, the overall efficiency drops and eventually limits the operating frequency. In addition, the physical size of the heat sinks in the system may need to increase to accommodate the additional heat dissipation, if the efficiency drops with the increased switching frequency. Therefore, improvements in the switching speed are required to minimise the switching energy loss for high frequency operation.

For high voltage operation, the switching speed of the standalone GaN transistor is often dominated by the Miller capacitance (C_{GD}), which will be discussed in detail in the next section. Therefore, efforts have been focused on the suppression of C_{GD} to improve the switching speed of the device. Figure 1-9 shows the diagram of a typical GaN HFET with field plates (FPs). The gate-connected field plate (GFP) is often

deposited together with the gate metal to form a ‘T’ shaped gate. It is important for high voltage devices as it modulates the field at the corner of the gate during off-state, and thus improves the breakdown voltage. The penalty is an increased C_{GD} since the effective capacitance area increases compared to the devices without GFP. To reduce the Miller capacitance, a common approach is to implement a source-connected field plate (SFP) [1]. The SFP screens the 2DEG and increases the distance from the 2DEG to the gate, leading to a reduction in C_{GD} . However, C_{GD} is still subject to high voltage and the Miller effect can still cause problems when operating at high drain bias. An alternative way is to form a cascode configuration, which is the focus of this study and is discussed in detail in Section 1.4.

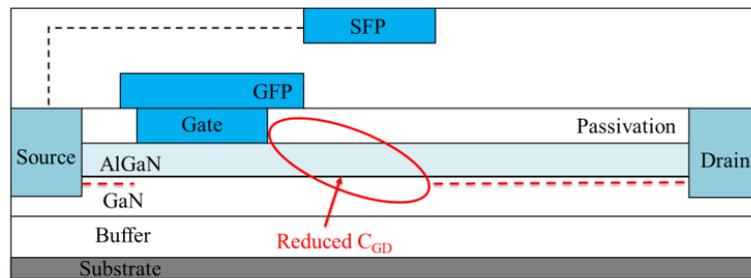


Figure 1-9 A schematic diagram of a typical GaN HFET with field plates (FPs). Implementing a source-connected field plate (SFP) effectively increases the capacitance distance during off-state, and thus reduces the Miller capacitance.

1.3 Miller effect in standalone devices for power switching

Miller effect or Miller capacitance effect is widely known for RF amplifiers [26]. It describes the virtual increase of the physical feedback capacitor connected between the input and output. Figure 1-10 shows a diagram of an ideal amplifier with a negative gain of $-G$ and feedback capacitance impedance of $1/sC$ (s is the complex frequency variable).

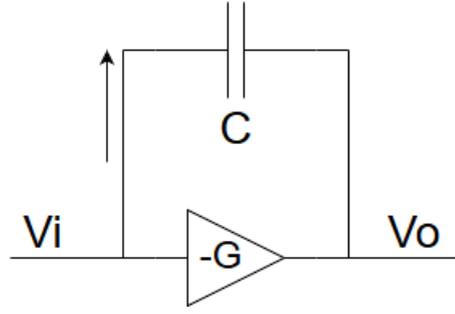


Figure 1-10 A schematic diagram of an ideal amplifier with a negative gain of $-G$ and a feedback capacitance C .

The effective input capacitance (C_M) of the system in Figure 1-10 can be derived by,

$$\frac{1}{sC_M} = \frac{V_i}{I} = \frac{V_i}{(V_i - V_o) * sC} = \frac{V_i}{(V_i + G * V_i) * sC} \quad (1-3)$$

So, we have,

$$C_M = (1 + G) * C \quad (1-4)$$

Therefore, C_M is increased by a factor of $(1+G)$ due to the positive feedback from the output to the input, which represents the Miller effect.

The Miller effect also applies to power switching devices and is described as the positive feedback from the drain to the gate during the switching transient [27-28], as shown in Figure 1-11. During the output voltage (V_o) transition, a dv/dt associated feedback current is generated through the gate-drain capacitance (C_{GD}). In either turn-on or turn-off transient, the feedback current has the same polarity as the gate current, and thus adds to the total current in the gate loop. Miller effect can limit the switching speed when the current drivability of the gate driver is insufficient and cannot provide the maximum feedback current. C_{GD} of the power switch is also known as the Miller capacitance.

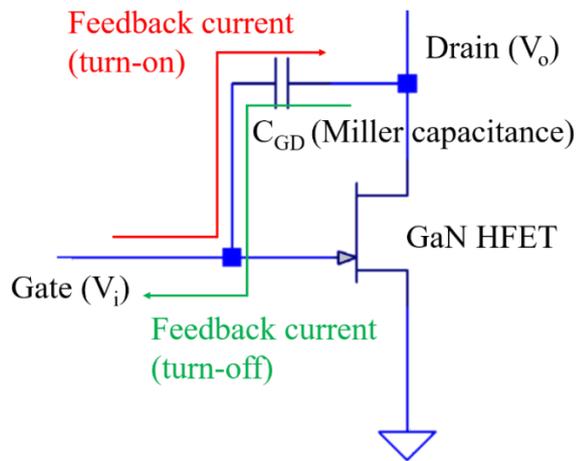


Figure 1-11 A schematic diagram illustrating the Miller capacitance and the Miller effect in a GaN power transistor during switching transient.

The influence of the Miller capacitance on the switching performance of a power transistor can be interpreted by considering either the switching transient of the drain voltage, or the switching energy loss [28].

Figure 1-12 shows a typical turn-on waveforms of the gate voltage (V_{GS}), drain voltage (V_{DS}) and drain current (I_{DS}) during inductive load switching. The process starts with a delay time before the V_{GS} reaches the threshold voltage of the device (V_{th}). The channel current of the device begins to increase until V_{GS} reaches a plateau voltage (V_p). This is also called the Miller plateau at which V_{GS} is clamped and V_{DS} starts to drop until the end of the plateau [28]. Note that the Miller effect does not necessarily limit the switching speed during the Miller plateau and this applies to both turn-on and turn-off transitions. For turn-on, Miller effect controls the speed when the gate current is insufficient and the total channel current during the Miller plateau is less than the current drivability of the device. In this case, the feedback current (discharging current) is limited by the gate current, and hence the speed of the voltage transient depends on the gate current capability and the Miller capacitance. An increase in the Miller capacitance can significantly extend the plateau time, while the drain-source capacitance has much less influence on the switching speed [28]. On the other hand, if the gate current is sufficient, the feedback current will reach its maximum value determined by the current drivability of the device. In this case, the discharging of the Miller capacitance is limited by the device

channel current instead of the gate current. After V_{DS} reaches its on-state, the gate current flows into the input capacitance again for V_{GS} to increase to the applied level.

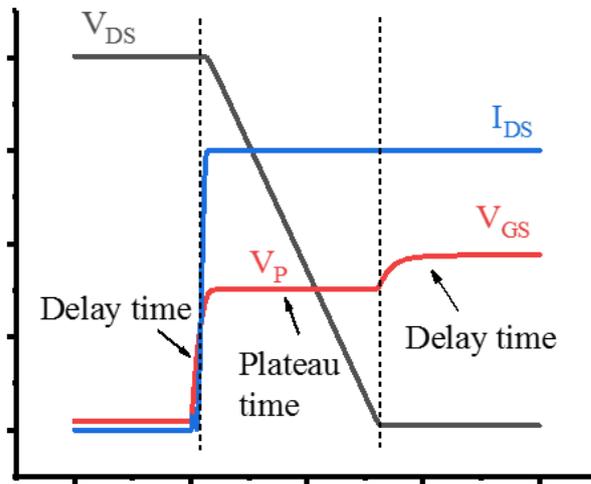


Figure 1-12 A typical turn-on waveforms of the gate voltage (V_{GS}), drain voltage (V_{DS}) and drain current (I_{DS}) during inductive load switching for a standalone device.

Figure 1-13 shows the turn-off waveforms of V_{GS} , V_{DS} and I_{DS} . Similarly, the process starts with a delay time before the V_{GS} drops to the plateau voltage (V_p). During the plateau time, the Miller capacitance and C_{DS} are charged up at the same rate via the load current. As a result, V_{DS} starts to increase. Similarly, whether or not the Miller effect will affect the speed of the voltage transient depends on the gate driving current capability. We first assume the gate driver can provide a gate current up to the load current. In this case, I_{DS} is fully utilised to charge the Miller capacitance and C_{DS} . The switching time solely depends on the load current and the total output charge involved in switching the device. C_{GD} and C_{DS} are equally important in determining the output charge, and hence the switching speed. However, in practice, the gate driving current will have a limit, depending on the quality of the driver, and is usually much smaller compared to the load current. Therefore, I_{DS} cannot be fully utilised in charging C_{GD} and C_{DS} , due to the current path through C_{GD} being limited by the gate driving current. In such a case, the Miller capacitance becomes the dominant parameter that determines the switching speed during Miller plateau [28]. After V_{DS} reaches its off-state value, the gate current starts to discharge the input capacitance again until V_{GS} finishes.

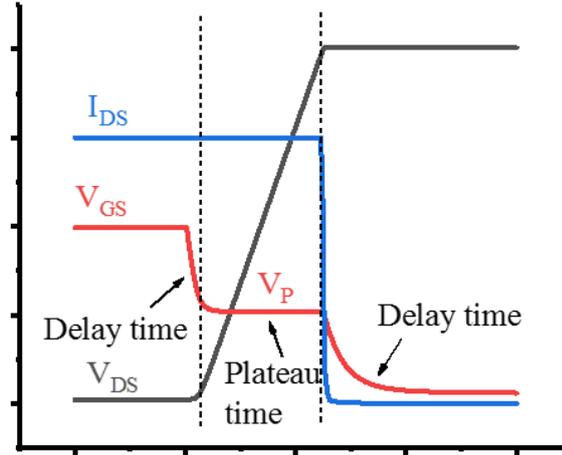


Figure 1-13 A typical turn-off waveforms of the gate voltage (V_{GS}), drain voltage (V_{DS}) and drain current (I_{DS}) during inductive load switching for a standalone device.

Besides the switching speed of the device, the switching energy loss can also reflect the influence of the Miller effect. Figure 1-14 shows typical inductive load switching waveforms highlighting the switching energy loss during turn-on and turn-off due to the overlap between V_{DS} and I_{DS} [23].

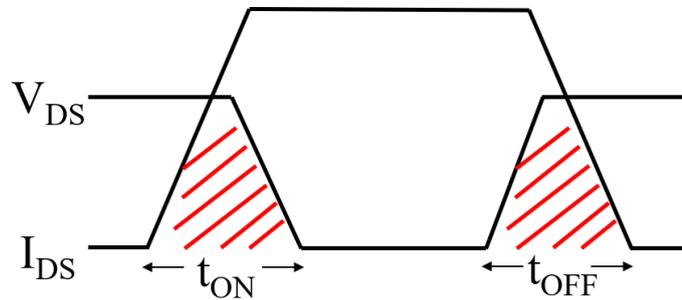


Figure 1-14 A typical inductive load switching waveform with the switching energy loss in turn-on and turn-off highlighted.

The switching loss of the device can be calculated by,

$$P_{sw} = \frac{1}{2} * V_{DD} * I_{load} * t_{ON} * f_{sw} + \frac{1}{2} * V_{DD} * I_{ch} * t_{OFF} * f_{sw} + \frac{1}{2} * C_{oss} * V_{DD}^2 * f_{sw} \quad (1-5)$$

where V_{DD} is the operating voltage, I_{load} is the load current, I_{ch} stands for the device channel current during turn-off, t_{ON} (t_{OFF}) is turn-on (off) time, C_{oss} is the output

capacitance of the device (consisting of C_{GD} and C_{DS}) and f_{sw} is the switching frequency.

The first term in (1-5) represents the switching loss due to the presence of the load current in the channel. The Miller capacitance has a significant influence on this turn-on switching loss by limiting the turn-on speed (t_{ON}). The second term refers to turn-off switching loss due to presence of a channel current during the voltage rise time. This current only exist when the gate driving current capability is less than the load current, as discussed previously. The gate driver needs to sink the charging current from the Miller capacitance to achieve an optimum switching speed. However, usually it is not capable of handling the full load current and therefore it eventually limits the turn-off speed, leading to an increase in this turn-off switching loss. The last term is the output capacitance loss during turn-on and turn-off. This capacitance loss is independent of the switching speed and the Miller effect [24-25]. This analysis shows that the Miller capacitance (C_{GD}) can significantly limit the switching speed and hence switching energy loss of the standalone device in power switching applications.

1.4 Cascode configuration

1.4.1 Generic cascode configuration

The generic cascode configuration consists of two transistors (Q1 and Q2) connected in series as shown in Figure 1-15. The gate of Q1 is connected to the source of Q2. The high voltage during the off-state is blocked by the top transistor (Q1) and, as a result, there is no feedback path from the drain to the gate in the cascode structure. The effective Miller capacitance becomes the C_{GD} of the lower transistor (Q2), which is only subject to a low voltage at the internode, determined by the V_{th} of Q1, as highlighted in Figure 1-15. The reduced Miller effect improves the gain of RF devices when incorporated into a cascode configuration and has been widely adopted in various RF applications [27-29].

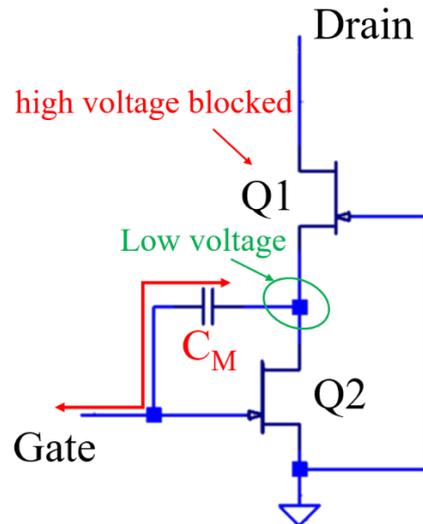


Figure 1-15 A schematic diagram of a generic cascode configuration that reduces the Miller effect by shifting the Miller capacitance to a low voltage node.

1.4.2 GaN plus Si cascode configuration

The concept of the cascode in GaN power transistors was first introduced by Transphorm in 2013 [30], with the release of their 1st generation GaN plus Si hybrid cascode device, which then became the first commercially available GaN HFET based 600 V power transistor [31]. The device consists of a high voltage D-mode GaN HFET and a low voltage Si MOSFET in a cascode connection, as shown in Figure 1-16. The V_{th} is determined by the Si MOSFET while the blocking voltage is decided by the GaN HFET. One of the major advantages of the GaN plus Si cascode is the ease of E-mode operation for GaN HFETs [30]. In addition, the device is compatible with most of the standard low-cost gate drivers for the Si MOSFET gate [30].

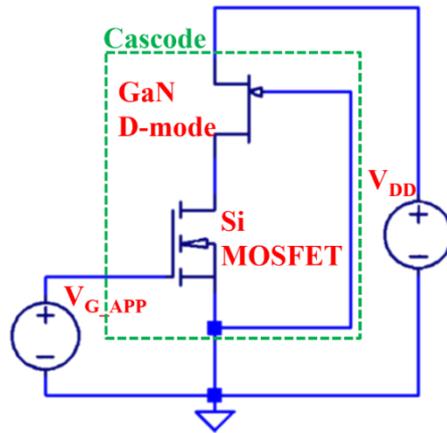


Figure 1-16 A schematic diagram of the GaN plus Si cascode configuration.

The switching performance of the GaN + Si cascode device has been intensively investigated using various power switching topologies, in comparison with Si MOSFETs and GaN standalone E-mode devices [31-34]. The reduced Miller effect in the cascode configuration and the small intrinsic capacitances in the GaN HFETs allow the GaN plus Si to operate at much higher frequency with lower switching energy loss compared to the state-of-art Si MOSFET [31]. The GaN plus Si cascode device exhibits a 95% efficiency at 200 kHz switching frequency in a PFC (Power factor corrected) with LLC converter [31]. The Si MOSFET can achieve similar efficiency of 94 % but needs to switch at much lower frequency (50 kHz). This results in 65 % less volume in the cascode based system [31]. Similar observations were reported with soft switching topology (Zero Voltage Switching) in [32]. The cascode device shows higher efficiency compared to the state-of-art Si MOSFET at 500 kHz. The reduced Miller effect in the cascode, leading to a negligible turn-off switching loss, is considered responsible for the advantage [32].

However, the GaN plus Si cascode device becomes less advantageous when compared with equivalent standalone GaN E-mode device [33]. Over 50 % larger turn-on energy loss is observed for the cascode device compared to two standalone E-mode devices by switching in a half bridge circuit at 400 V [33]. In a typical half bridge topology formed by GaN plus Si cascode transistors, as shown in Figure 1-17, the body diode (formed by a p-n junction) of the Si device for both transistors can change the state from conducting to non-conducting. As a result, an additional reverse conducting current is required to change the charge distribution in the p-n

junction when the body diode is switched from on-state to off-state. This reverse recovery time induces additional energy loss, leading to disadvantages to the hybrid cascode compared to GaN standalone device, and is claimed to be the main reason for the increase in turn-on energy loss [33]. While in turn-off, the cascode device can still have less energy loss when the load current is increased above a certain value. The increased load current relative to the gate driver current capability leads an enhanced Miller effect in the standalone device [33]. On the other hand, due to the nature of the cascode connection (with reduced Miller effect), the turn-off switching energy loss has little dependence on the increased load current. The switching waveforms measured in [34] shows a longer delay time of 12.5 ns and 33.5 ns (turn-on and turn-off) for the cascode device compared to 5.5 ns and 17.5 ns for the GaN standalone device. This is due to relatively larger intrinsic capacitance in the low voltage Si MOSFET compared to the GaN E-mode device. These experimental results indicate that the use of Si MOSFET may negate the advantage of the cascode configuration when compared with GaN standalone E-mode device.

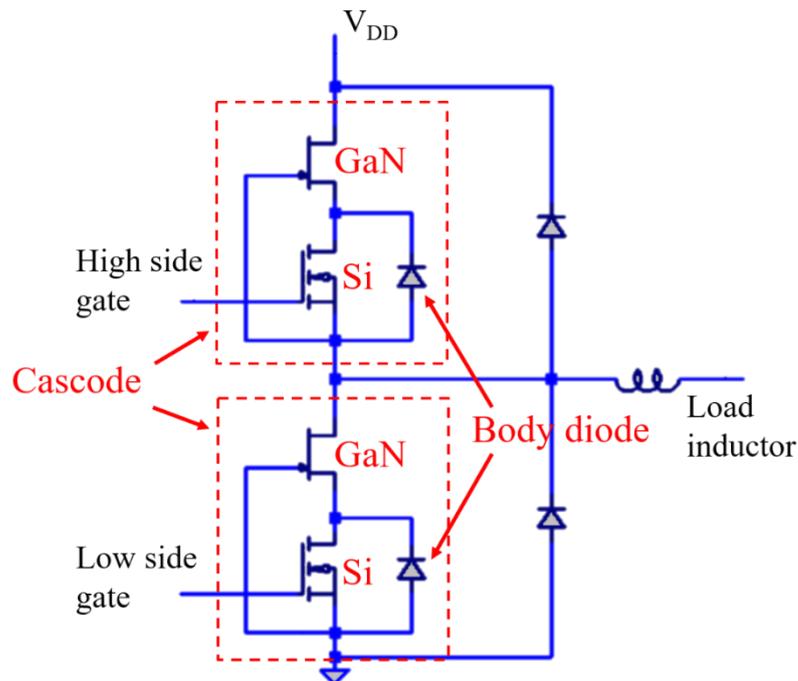


Figure 1-17 A diagram of a typical half bridge circuit formed by two GaN plus Si cascode transistors.

1.4.3 Motivation of the all-GaN integrated cascode configuration

Several drawbacks can be found in the GaN plus Si cascode configuration and need to be addressed in order to compete with GaN standalone E-mode devices. Firstly, the use of the Si device induces large input capacitances and reverse recovery charge due to the body diode, which can negate the speed advantage brought by the reduced Miller effect in the cascode connection. Table 1-2 shows the comparison between a state-of-art 600 V Si SJ MOSFET, a GaNsystem 650 V power transistor, a Panasonic X-GaN power transistor and a Transphorm GaN plus Si cascode device [35-38].

Table 1-2 Comparison between Si SJ MOSFET, GaNsystem E-mode, Panasonic E-mode and Transphorm cascode. Device parameters are at room temperature taken from datasheets.

	Rating (V)	R_{on} (m Ω)	$R_{on} * Q_g$ (m Ω nC)	$R_{on} * Q_{oss}$ (m Ω μ C)	$R_{on} * Q_{rr}$ (m Ω μ C)
Si SJ MOSFET (IPL60R065C7)	600	56	3800	23.5	312.5
GaNsystem (GS66508B)	650	63	365.4	3.6	0
Panasonic X-GaN (PGA26E07BA)	600	70	350	3.15	0
Transphorm Cascode (TPH3205WS)	600	63	1701	3.9	8.568

The cascode device is advantageous over the state-of-art Si SJ MOSFET in both input Figure of Merit ($R_{on} * Q_g$) and output Figure of Merit ($R_{on} * Q_{oss}$). However, compared to standalone E-mode device, the hybrid cascode configuration suffers from over 4 times larger $R_{on} * Q_g$ and an additional reverse recovery loss ($R_{on} * Q_{rr}$). The additional Q_{rr} originates from the body-diode in the low voltage Si MOSFET and can increase the turn-on switching energy loss significantly [33], while the larger Q_g is due to the intrinsic capacitances in the Si MOSFET and effectively increases the energy loss in the gate driver during charging and discharging the input capacitances.

Secondly, the connection between the discrete GaN and Si devices can induce parasitic inductance to the device [39-40]. Wire bonding is normally used to connect the low voltage Si and the high voltage GaN HFET [40]. Figure 1-18 shows the possible parasitic inductance caused by the bonding wire within the cascode. These packaging induced parasitic inductance can be as low as a few nH, but can still cause large ringing effects, especially under high current operation [33]. An advanced packaging method was proposed in [40]. The drain electrode of the Si MOSFET is

directly stacked on top of the source of the GaN HFET. This effectively eliminates the wire bond at the internode and hence L1 in Figure 1-17 can be minimised. However, careful design is needed due to the difficulty in the proposed approach.

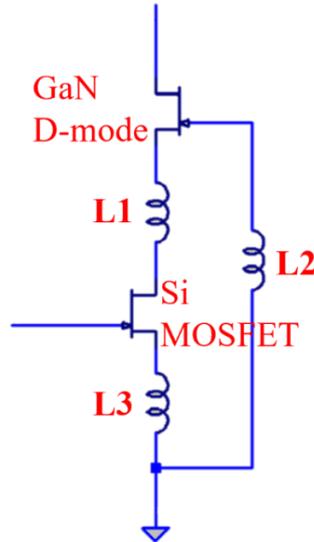


Figure 1-18 A schematic diagram showing the parasitic inductance induced by the connections between the GaN D-mode device and Si MOSFET.

Finally, optimisation of the GaN plus Si cascode often requires external components, which bring additional challenge to the device packaging. The interaction between the low voltage and high voltage device can affect the energy stored at the internode, and hence the actual performance of the cascode device [41-44]. Therefore, optimisations are often needed to address the matching between the two parts in the cascode. For instance, the voltage at the internode can increase above the avalanche breakdown of the body diode in the Si MOSFET during the off-state, leading to an increased conduction loss (through the body diode) [41]. To suppress the internode voltage at the off-state, an external capacitor is proposed and connected between the internode and the source of the cascode [41]. However, additional parasitic inductance is also added to accommodate this external capacitor.

1.5 Overview of thesis

In this thesis, we propose an all-GaN integrated cascode configuration by replacing the low voltage Si MOSFET with a low voltage GaN E-mode device. Due to monolithical integration, the relatively ‘slow’ Si device is eliminated, as is the

parasitic inductance between the two transistors. The optimisation of the cascode configuration may also benefit from the full integration without the worry of additional parasitics.

The main objective of this study is to demonstrate the suitability of the all-GaN integrated cascode configuration for high voltage, high frequency operation. This is attempted by establishing the speed advantage of the integrated cascode over the equivalent standalone GaN E-mode device, and understanding the switching behaviour as well as the complex matching issues of the cascode device. The work involved in this study includes device design and fabrication, DC and switching characterisation, theoretical analysis, and SPICE simulation. The main contributions to the new knowledge includes the first-time demonstration of high voltage all-GaN integrated cascode configuration, the theoretical analysis of integrated cascode switching behaviour and the field plate optimisation in the integrated cascode devices. The thesis is outlined as follows.

In chapter 2, the design and the fabrication procedure of the integrated cascode device is presented. Various DC and dynamic characterisation techniques are described.

In chapter 3, an all-GaN integrated cascode configuration is demonstrated. An optimisation by engineering the D-mode threshold voltage to achieve the maximum output current for the integrated cascode is presented. The switching performance is compared with an equivalent GaN standalone device at 200 V using an inductive load double pulse tester. A speed advantage of 33% is observed and the origin of the advantage is explored by TCAD and SPICE simulation.

In chapter 4, an analytical study on the switching behaviour of an all-GaN integrated cascode configuration is presented. Mathematical equations are derived for the switching speed of the cascode device and are verified with LTSPICE simulation results. The origin of the speed advantage for the integrated cascode is explored theoretically. Important device parameters which lead to an optimum switching performance of the cascode are identified. Detailed guidelines toward the optimisation of the integrated cascode is presented.

In chapter 5, the influence of the FP design in the all-GaN cascode configuration is discussed. The suppression of the dynamic R_{on} effect is compared between devices with various FP geometries. The correlation between the FP geometries and the intrinsic capacitances is analysed using high voltage capacitance-voltage (CV) results. Three different FP connections are proposed for the all-GaN integrated cascode configuration and their influence on the switching performance are explored by experimental and SPICE simulation results.

Chapter 6 is the conclusion of the thesis. Several relevant future studies are also suggested.

1.6 References

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2 Methodology

2.1 Introduction

This chapter describes methodologies involved in this study including fabrication techniques, characterisation techniques and LTSPICE simulation for the all-GaN integrated cascode devices.

2.2 Fabrication techniques

The AlGaIn/GaN epitaxy used were grown on 6-inch Si substrate, by Cambridge University. Figure 2-1 shows a standard wafer structure.



Figure 2-1 Typical layer structure for all-GaN integrated cascode device.

The fabrication of the all-GaN integrated cascode devices were done in the EEE semiconductor cleanroom, the University of Sheffield. The large area cascode devices (from gate width of 1mm to 32mm) were fabricated by Dr Kean Boon Lee. The author was involved in small area (up to gate width of 100um) cascode device fabrication, and was mainly responsible for device characterisation and simulation.

Figure 2-2(a) – (k) shows the diagrams of the device layer structure after each stage of the fabrication process. Compared to the standard GaN HFETs, the cascode device monolithically integrates the E-mode and D-mode gate, and therefore the

fabrication sequence is carefully designed and is discussed in detail in the following sections.

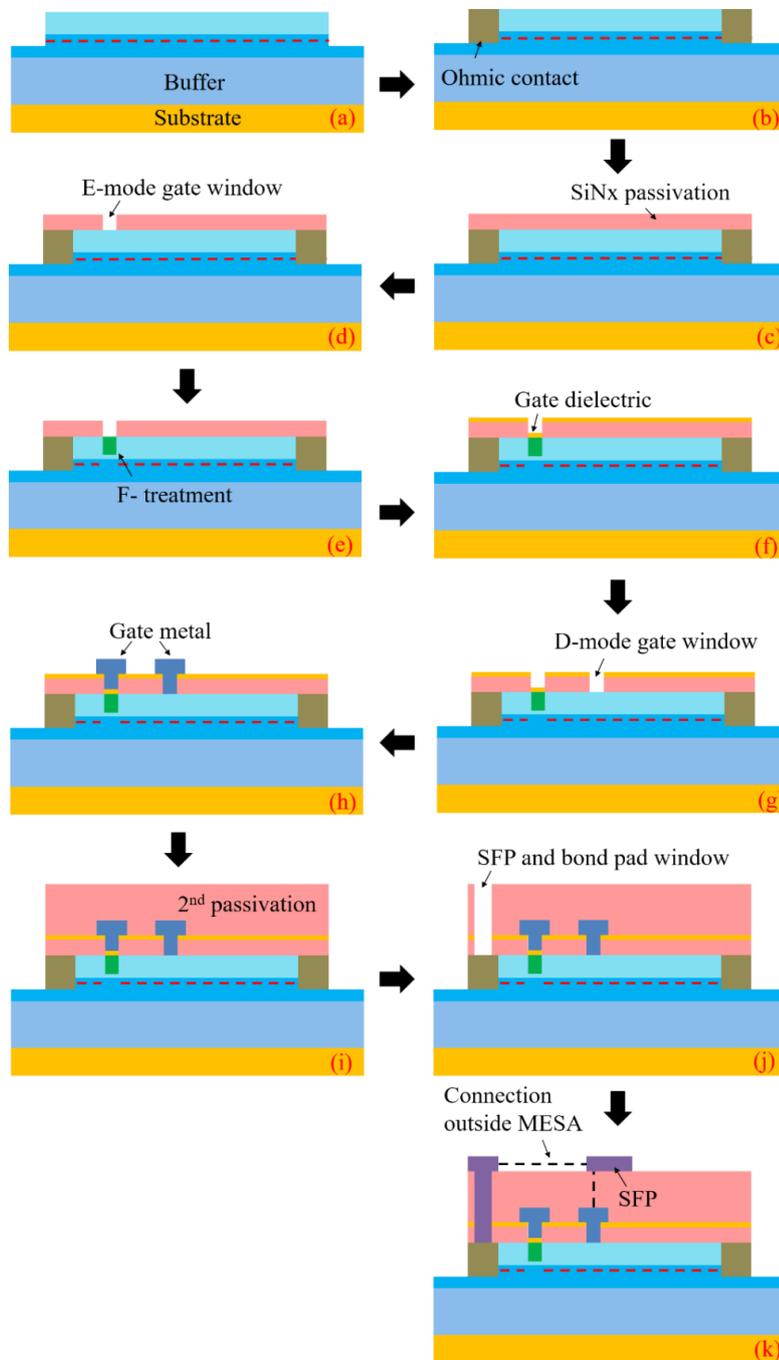


Figure 2-2 Fabrication procedure of the all-GaN integrated cascode device including (a) Mesa isolation, (b) ohmic deposition, (c) 1st passivation, (d) E-mode gate foot definition, (e) F-treatment, (f) gate dielectric deposition, (g) D-mode gate definition, (h) gate metal deposition, (i) 2nd passivation, (j) SFP and bond pad window opening, (k) SFP and bond pad formation.

2.2.1 Sample preparation

2.2.1.1 Sample cleaving

Most of the samples in the study are cleaved manually using a diamond tip scribe. The sample is put on a clean filter paper with its backside up. The cleaving is done on the substrate to protect the epitaxial layer. We use a glass slide to clamp the sample and then use the scribe to draw a deep straight line. After that, a second glass slide wrapped with filter paper is put underneath the sample and on one side of the line. By manually holding one side and pushing downwards on the other, we can break the sample into two along the cleaved straight line. A third glass slide can be used to avoid pushing the sample by hand. We repeat the process until a desired size is produced. After cleaving, it is important to put the rest of the wafer back to the wafer container and mark the position of the taken piece. This is to take the wafer variation into consideration during the future characterisation.

2.2.1.2 Three-step cleaning

It is important to clean the sample using solvents after every fabrication step to minimise the physical particles on the surface and chemical contamination especially oxides. Our cleaning procedure is listed as following:

- 1) Dip the sample into room temperature n-butyl acetate and put it on a filter paper. Room-temperature n-butyl acetate is used to prevent drying and leaving stains on the surface.
- 2) Wipe the surface using cotton buds with n-butyl to remove physical particles. Special attention is paid to the edges and corners due to the damage after cleaving.
- 3) Dip the sample into boiling n-butyl acetate for 20s. The bubbling can help with removing the physical particles.
- 4) Dip the sample into room-temperature acetone for 20s to minimise the contamination and grease.
- 5) Dip the sample into isopropyl alcohol (IPA) for 20s to further clean and avoid acetone drying on the surface and leaving stains. After that, blow dry the sample using a nitrogen gun.

Step 1 and 2 can only be conducted after sample cleaving. Once the fabrication process starts, cotton buds should be avoided to ensure the patterns on the surface are intact during cleaning. Step 3, 4 and 5 are used afterwards as our standard three-step cleaning procedure.

2.2.2 Mesa isolation

Mesa isolation is essential to isolate each cell by etching away the channel (2DEG). It involves two steps i) define the Mesa area and ii) inductively coupled plasma (ICP) dry etching.

2.2.2.1 Mesa lithography

We first mount the sample on a small square glass slide approximately 2 mm^2 with a small amount of wax. The glass slide helps the spinner and the mask aligner to firmly hold the sample. After that, the sample is pre-baked for several seconds on a $100 \text{ }^\circ\text{C}$ hot plate to dehydrate. Positive photoresist SPR350 is used and gives around $1 \text{ }\mu\text{m}$ thick after spinning at 4000 rpm. The type of photoresist and the speed of spinning can vary depending on the type of use. A larger photoresist thickness may affect the edge sharpness of the pattern, and thus is not suitable for defining small features. On the other hand, the photoresist needs to be thick enough to withstand the etching process. After spinning, the sample is post-baked for 1 min at $100 \text{ }^\circ\text{C}$ to improve the sensitivity to the light of the photoresist.

Photolithography is employed to define the patterns using a Karl Suss mask aligner (UV300 or UV400) and our own chromium mask-set. The exposure time is around 12.5 s for UV300 and 5 s for UV400. A test piece is usually used before the sample to estimate the best exposure time, as the intensity of the UV light can vary each time. After exposure, we dip the sample in MF26A developer for 30 s and gently shake it for another 30 s. This is to remove those photoresists which have been exposed to the UV light. It is important to shake the sample gently in the developer, because the transferred pattern may move out of its position. Finally, the sample is rinsed in the deionised water and gently dried with nitrogen gun. If the exposure or alignment is not satisfactory, we can remove the residual photoresist by three-step cleaning and repeat the process.

2.2.2.2 Inductively coupled plasma reactive-ion etching (ICP-RIE)

ICP-RIE, as a type of dry etching, is used to achieve a high-fidelity transfer of photoresist pattern. It is important to prepare the chamber first by running a chamber clean recipe to minimise any contamination. The etch depth is between 500-600 nm to ensure the 2DEG is etched away where it is not required. The recipe used for Mesa etching is shown in Table 2-1. A laser point measurement system is often used to monitor the etch depth during the process. Figure 2-2(a) illustrates the layer structure of the sample after etching.

Table 2-1 ICP recipe for Mesa etching.

Cl ₂ flow rate	15 sccm
Ar flow rate	4 sccm
ICP power	450 W
RF power	50 W
Pressure	5 mtorr
DC bias	190 V
Etch time	6 mins

EKC 830 resist stripper is used to clean the remaining photoresist. We dip the sample in resist stripper and heat it to 100 °C on a hot plate for 5 mins. After that, the sample is treated in an ultra-sonic bath for 5 mins, followed by three-step cleaning. A Dektak system is used to measure the etch depth after cleaning the sample.

2.2.3 Ohmic deposition

2.2.3.1 Lithography

After Mesa etching, a similar lithography process is conducted to define the ohmic patterns. To improve the quality of alignment and exposure, the sample needs to be as close to the mask as possible during alignment. Therefore, an additional step of edge-bead removal of the photoresist is necessary. After developing the photoresist, the sample is ashed in an oxygen plasma asher to remove the residual photoresist in the ohmic region. Lastly, an acid treatment (HCL:DI water = 1:1) for 1 min is conducted to remove the oxide contaminant on the surface.

2.2.3.2 Metal deposition

A thermal evaporator Edwards coating system E306A is used for metal deposition. It utilises resistive heating to melt the prepared metal in an evacuated chamber. The evaporated metal then falls onto the surface of the sample as well as a crystal monitor, which detects the thickness of the deposited metal.

Ti/Al/Ni/Au 20nm/120nm/20nm/45nm is used for the ohmic contacts. Metals are firstly weighed and boiled in heated n-butyl to remove particles. After that, we insert the prepared metals into tungsten coils and load the coils into the chamber. Ti and Ni, compared to Al and Au, have higher melting points, and therefore are installed further away (12 cm) to protect the sample from high temperature.

After metal deposition, the sample is left in acetone for 12 hours as a lift-off process. Acetone removes the photoresist and thus the metal on top of the photoresist. In some cases when the lift-off results are not as expected, an ultrasonic bath with the sample dipped in acetone for several minutes is used to further remove the remaining metal.

2.2.3.3 Rapid thermal annealing (RTA)

After three-step cleaning, the sample is annealed by RTA. During the annealing process, Ti/Al diffuses into the semiconductor and forms TiN/AlN, which reduces the contact resistance and enables the ohmic behaviour. Meanwhile, Ni is an effective diffusion barrier and stops Au from penetrating into the semiconductor [1]. As a result, Au remains on top and prevents oxidation of the Ti and Al. A multi-step annealing of 400 °C for 1 min, 700 °C for 3 mins and 830 °C for 30 s is used to give an optimised edge acuity and reasonable ohmic contact resistance. Figure 2-2(b) illustrates the layer structure after ohmic contact formation.

It is necessary to measure some of the Transmission Line Model (TLM) structures across the sample after annealing, to make sure the ohmic contact is working. The fabrication process should be stopped if TLM structures does not give ohmic behaviour. More detailed illustration of measurement will be given in the Characterisation techniques Section.

2.2.4 1st passivation

After ohmic contact formation, a nominally 50 nm SiN_x is deposited by a Plasma-therma 790 series plasma enhanced chemical vapour deposition (PECVD), as shown in Figure 2-2(c). The deposition rate is around 10 nm/min, with base temperature of 60 °C and chamber wall temperature of 300 °C. This 1st passivation layer is important for supporting the GFP and suppress surface related dynamic R_{on} issue [2]. The thickness of the 1st passivation determines the intrinsic capacitance of the device, which will be discussed in detail in Chapter 5.

2.2.5 E-mode Gate foot definition

Photolithography is carried out to define the E-mode gate foot for F- treatment. The exposure is extremely important at this stage because any discontinuity along the gate foot could cause non-pinch-off in the channel, which affects the threshold voltage and increases drain-source leakage. The sample is ashed for 2 mins to remove the residual photoresist after developing.

The SiN_x at the gate foot is etched away by ICP-RIE with a CHF₃ based recipe. The gas flow is set to be 40 sccm with the RF power of 100 W, giving an etch rate of around 5 nm/min. A laser end point detector is used to monitor the etching process. We normally over etch the sample for 2min after the etch stop, to take the consideration of the non-uniformity of the surface. Figure 2-2(d) shows the layer structure after E-mode gate foot opening.

2.2.6 F- treatment

F- treatment is conducted directly after the gate foot opening with the same CHF₃ based recipe but RF power increased to 150 W, as shown in Figure 2-2(e). The time of the treatment strongly depends on the condition of the sample and the ICP machine. Therefore, we run a few test samples each time to optimise the F- treatment duration. 14-mins treatment is often used and can provide a positive threshold of 0.5 V while maintaining reasonable channel current and transconductance. Three-step cleaning is used to remove the residual photoresist after F- treatment.

2.2.7 Gate dielectric deposition

PECVD is used to deposit a nominally 20 nm gate dielectric (SiN_x) to form a metal-insulator-semiconductor (MIS) structure on the E-mode gate, as shown in Figure

2-2(f). The gate dielectric suppresses the gate leakage current and increases the threshold. In addition, it enhances the gate voltage swing by preventing the turn-on of the Schottky gate at forward bias (+2 V).

2.2.8 D-mode gate definition

Similar to the process described in Section 2.2.5, a photolithography step is carried out to define the D-mode gate foot. The etching of the SiN_x (nominally 120 nm) is done by ICP-RIE with the CHF₃ based recipe. Depending on the design of the cascode structure, a Schottky D-mode gate can be done by completely etching away the SiN_x, alternatively, a MIS D-mode gate structure can be achieved by a timed etching of the SiN_x according to the etch rate, leaving nominally 10 – 20 nm. Detailed discussion on both D-mode gate options are presented in Chapter 3. Figure 2-2(g) shows an example of a cascode structure with a Schottky D-mode gate.

A post etch anneal at 500 °C for 5 mins under N₂ ambient by RTA is conducted to recover the plasma damage on both E-mode and D-mode gate foot after D-mode gate foot opening.

2.2.9 Gate Metal deposition

Similar to the process described in 2.2.3, a photolithography step is firstly carried out by the UV300 mask aligner. The opening includes both E-mode and D-mode gate as they are deposited at the same time. The gate metal opening is larger than the gate foot to take account of the potential misalignment and to ensure that the gate foot is fully covered by the gate metal.

After photolithography, Ni/Au (20nm/200nm) is deposited by the thermal evaporator to form the gate. Figure 2-2(h) shows the deposited T-shape gate for both E-mode and D-mode parts. The T-shape gate reduces the spreading resistance of the gate and acts as the GFP that modulates the electric field near the gate.

2.2.10 2nd passivation

A 300 nm SiN_x is then deposited by PECVD as the 2nd passivation layer, as shown in Figure 2-2(i). The process is the same as described in Section 2.2.4. The 2nd passivation provides the insulating layer for interconnects of multi-finger devices and supports the SFP. The thickness of 2nd passivation determines the intrinsic capacitance of the device and will be discussed in detail in Chapter 5.

2.2.11 SFP and bond pad formation

The openings for the SFP and bond pad shown in Figure 2-2(j) are achieved by a reactive-ion etching (RIE) tool. RIE is similar to ICP-RIE but with less ion energy because it is not plasma enhanced. After etching, a three-step cleaning is conducted.

Ti/Au (20/120 nm) is used for the SFP and bond pad. The metal preparation and the deposition process are similar to that described in Section 2.2.3. Figure 2-2(k) shows the final structure of the all-GaN integrated cascode after depositing the SFP and bond pad metal. The SFP is necessary for high voltage operation as well as for engineering the intrinsic capacitance of the device. The bond pad makes it easy to probe the device for on-wafer characterisation. Note that the bond pad layer can be done separately with thicker Au (400 nm), which improves the adhesion of the pad and the gold wire when doing wire bonding in Sheffield or flip chip bonding in Nottingham University.

2.2.12 Wire bonding

In order to perform sensible switching measurements of the fabricated device, wire bonding is carried out in-house to eliminate the use of on-wafer probes which can introduce high inductance which limits the switching performance of the device.

Firstly, the sample is further cleaved into a small piece leaving the target device as close to the edge as possible. This is to reduce the length of the bonding wire, and thus the series resistance and inductance. The cleaving process is the same as described in Section 2.2.1. After that, the sample as well as the bonding board are cleaned using the three-step cleaning. We then put some gold epoxy on the bonding board and mount the sample onto the PCB. The PCB is baked at 180 °C in an oven for 2 hours to secure the sample.

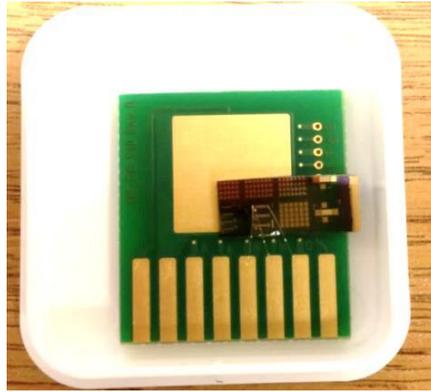


Figure 2-3 An optical image of a wire bonded device.

The connection process is carried out using a wire-bonder machine. We firstly install the sample on the sample holder and heat it to 100 °C. The high temperature makes it easier for the gold wire to stick onto the pads on the bonding board. By adjusting the bonding force, time and ball size, solid bonds can be made between the device and the bonding boarding. Figure 2-3 shows and example of a wire bonded device.

2.3 Characterisation techniques

2.3.1 Current-Voltage (I-V) measurements

Current-Voltage (I-V) measurements are used to characterise the DC performance of GaN HFETs. Several source-measure units (SMUs) are required depending on the type of I-V measurements and the number of terminals involved. Instead of using the default software that is provided by the SMU manufacturers, we use self-designed programs based on LabView. There are several advantages in using self-designed characterisation programs. Firstly, different SMU models, including a 20 W high voltage (1000 V) single channel Keithley SMU 2410, a 40 W high current (3 A) dual channel Keithley SMU 2602B and a 10 W Keithley SMU 236 come with incompatible software. Self-designed programs can link these SMUs together to achieve the required measurements. Moreover, the flexibility in modifying those programs offer great benefits to the users with customised functions that cannot be included in the default software. In addition, it is easy to maintain, update and optimise due to the full control over the designed programs. In this section, we describe the principle and design details of two-terminal, three-terminal and four-terminal I-V measurements, respectively.

2.3.1.1 Two-terminal measurements

Figure 2-4 shows the schematic diagram of a TLM measurement. A set of identical ohmic contacts with different gap spacing are fabricated. We ground one of the ohmic pads for each gap spacing, and sweep the voltage from -2 V to +2 V on the other one using SMU 2410. The measured I-V characteristic follows a resistive behaviour assuming a good ohmic contact. The total resistance (R_{total}) consists of two contact resistance (R_c) and a sheet resistance (R_{sh}) of the specific gap spacing. Therefore, we have

$$R_{total} = 2 * R_c + R_{sh} * \frac{L}{W} . \quad (2-1)$$

Where L is the gap spacing and W is the width of the ohmic pad. By measuring the TLM with different gap spacing, R_c and R_{sh} per unit width can be calculated using (2-1).

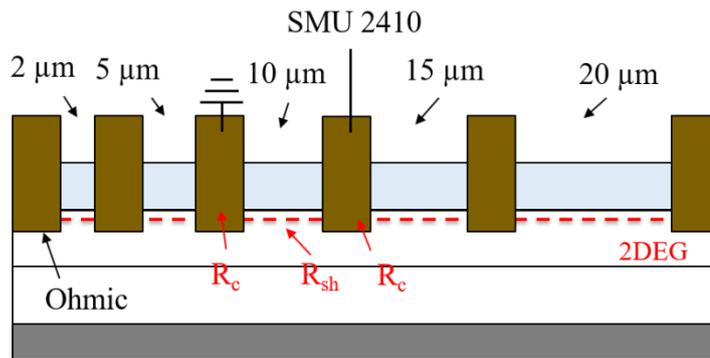


Figure 2-4 A schematic diagram of a TLM structure.

Figure 2-5 shows a simplified programming flowchart for the 2-terminal measurements. SMU 2410 is initialised to its default status at the beginning of the program to ensure its memory is cleared. Apart from TLM measurement, the high voltage 2-terminal breakdown (e.g. breakdown of the diode structure) can also be performed depending on choice of the measurement type. After that, SMU loads the compliance and input values of the voltage. The measurement repeats until the last measurement is done. After that, SMU turns off the output and data are plotted automatically with an option to save for future use. If the compliance is reached during the current reading, the program automatically stops to protect the SMU and the device. Figure 2-6 shows the user interface of the 2-terminal measurement

program based on LabView. The 3-terminal and 4-terminal programs in the later sections will have similar style of user interface and will not be shown to avoid redundancy.

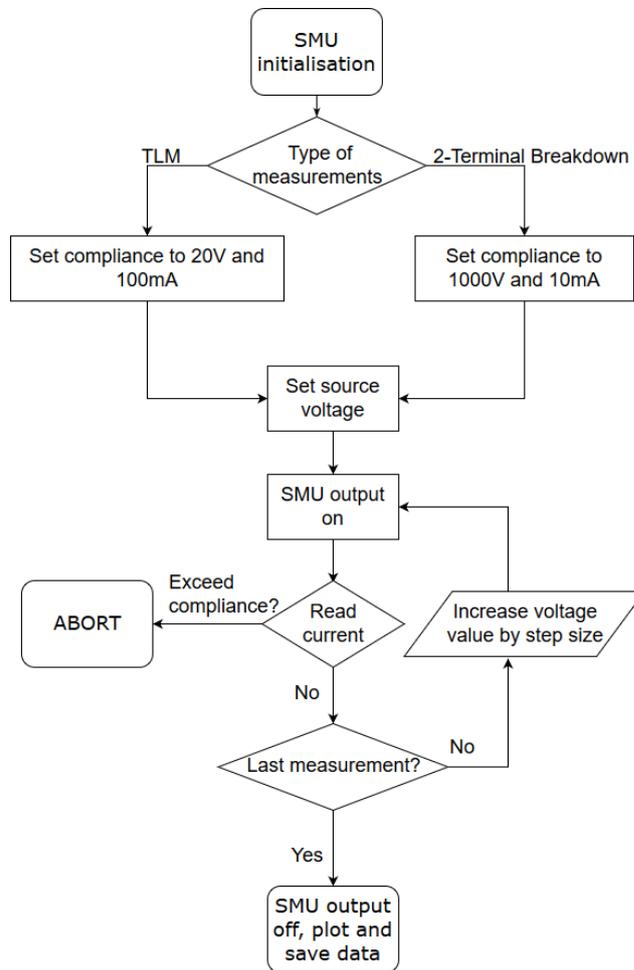


Figure 2-5 Programming flowchart of the 2-terminal measurement.

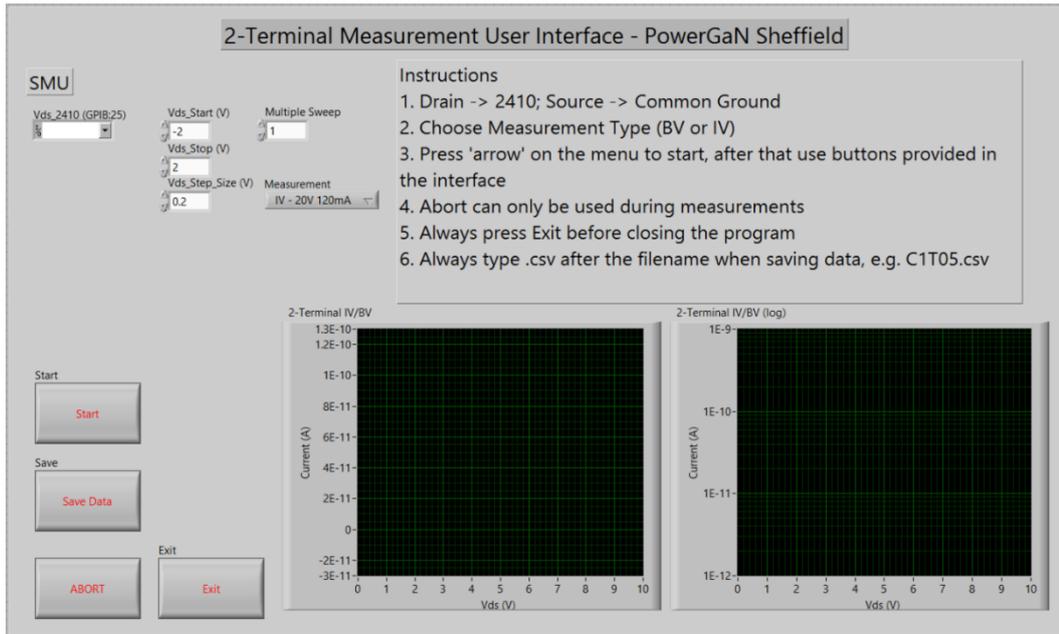


Figure 2-6 User Interface of the 2-terminal measurement program.

2.3.1.2 Three-terminal measurements

The 3-terminal measurements consist of gate transfer and output characteristic measurements. Figure 2-7 shows the schematic diagram of the 3-terminal setup. The drain of the device is connected to SMU 2410 and the gate is connected to SMU 2602B. The source is grounded. During a gate transfer measurement, the drain electrode is biased at +10 V, while the gate can be swept from -10 V to +10 V depending on the threshold voltage of the device. The results are plotted as gate voltage versus drain current, indicating the current drivability and the threshold voltage of the device. During an output characteristic measurement, the gate electrode is biased and stepped from -10 V to +10 V depending on demand, while the drain is swept from 0 V to +20 V at each step of the gate bias. The results are plotted as drain voltage versus drain current. The on-resistance (R_{on}) of the device can be extracted from the output characteristic, assuming the drain current increases linearly at low drain bias through origin. The current at $V_{DS} = 1$ V is normally used, and the R_{on} can be extracted by,

$$R_{on} = \frac{1}{I} * W \quad (2-2)$$

where I is the current reading at $V_{DS} = 1$ V and W is the gate width. The extracted R_{on} is in Ω *mm.

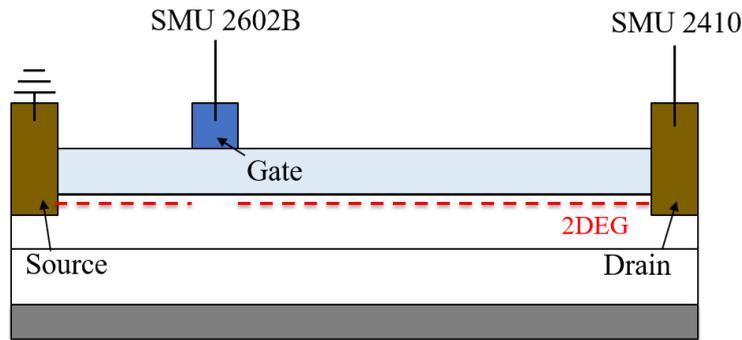


Figure 2-7 A schematic diagram of a 3-terminal measurement.

Figure 2-8 shows the programming flowchart of the gate transfer measurement. The principle is similar with the 2-terminal measurement as described in the previous section. However, the 3-terminal program involves multiple SMUs. Communication between different SMUs is achieved by a time-delay approach. After SMU 2410 turns on and performs one measurement, a 10 ms delay is introduced to inform SMU 2602B to start the gate measurement. In the meantime, SMU 2410 holds its output voltage and waits until the delay time in the SMU 2602B loop completes. This time-based approach enables the communication between multiple SMUs and creates accurate synchronisation of the measurement actions.

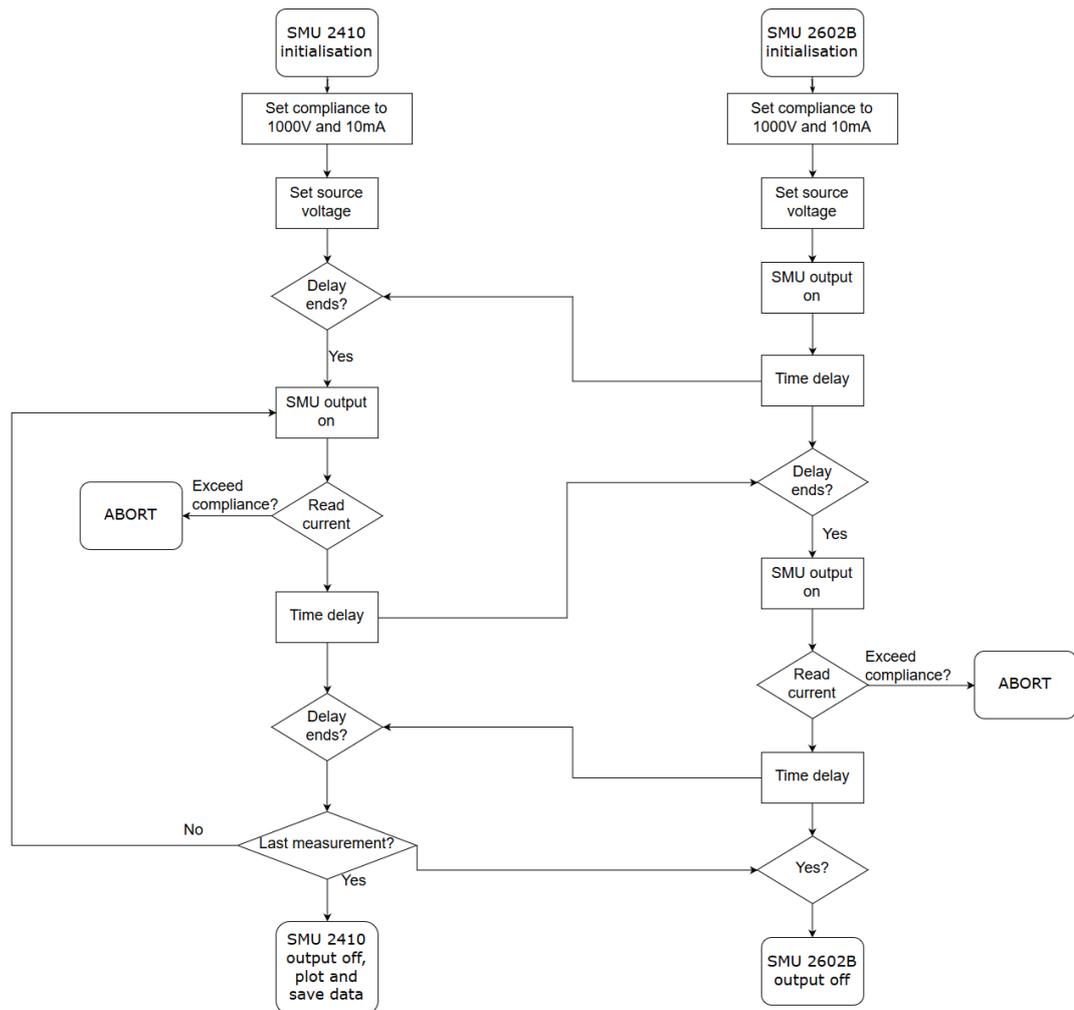


Figure 2-8 Programming flowchart of the gate transfer measurement.

2.3.1.3 Four-terminal measurements

Figure 2-9 shows the schematic diagram of the 4-terminal breakdown measurement. The drain of the device is connected to SMU 2410 and swept from 0 V to 1000 V depending on breakdown of the device. The gate is pinched off by SMU 2602B. The source and the substrate are configured as ampere meters using SMU 2602A and SMU 236, respectively. Current through the drain, gate, source and substrate are all monitored to provide complete information on the leakage profile during off-state at high voltage. The detailed cause of breakdown can also be indicated by comparing those individual currents. The LabView program involves the link of four SMUs and has similar principle as described in the previous section.

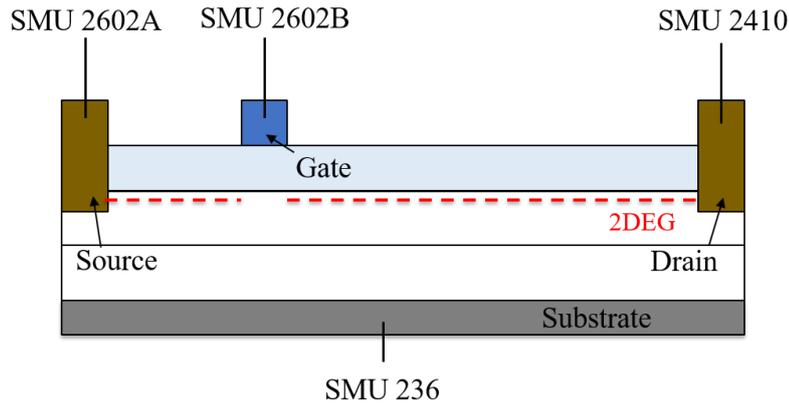


Figure 2-9 A schematic diagram of a 4-terminal breakdown measurement.

2.3.2 Double pulse tester (DPT)

A DPT with an inductive load was designed and used to characterise the hard-switching performance of the GaN HFETs. It simulates the realistic power switching application where the load is often inductive (e.g. a motor). In addition, DPT only generates two pulses which makes the waveform easy to capture and eliminates any heating effect during the measurement. Figure 2-10 illustrates the circuit diagram of the DPT measurement.

An example of measured waveform is shown in Figure 2-11. Two pulses are supplied to the gate of the device, as indicated in the yellow curve. The first pulse is usually longer and is to build up current in the load inductor to a desired value. The length of the first pulse can be calculated by,

$$t = \frac{L \cdot I_{load}}{V_{DD}} \quad (2-3)$$

Where I_{load} is the desired load current, V_{DD} is the drain voltage and L is the inductance of the load inductor. The turn-off transient is measured at the end of the first pulse when the load current reaches the desired value. After that, a short delay is introduced before the start of the second pulse to accommodate the turn-off time of the device. The turn-on time is then measured at the beginning of the second pulse with the same inductor current, assuming the short delay between two pulses does not lead to a reduction in the inductor current. The length of second pulse needs to be larger than the turn-on time of the device.

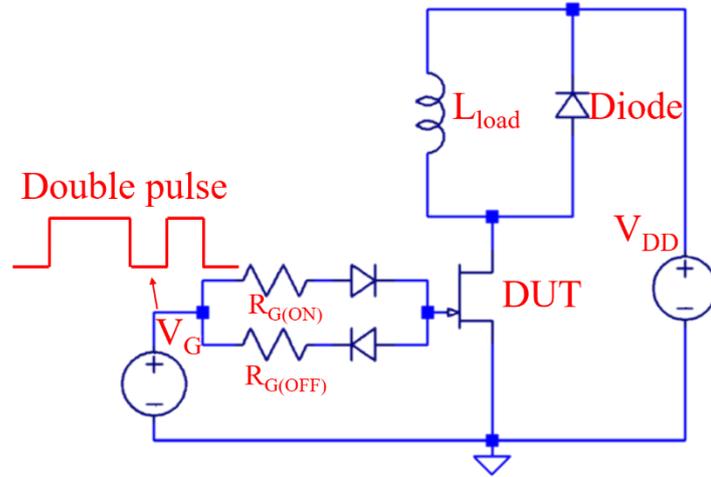


Figure 2-10 Circuit diagram of the DPT hard-switching measurement.

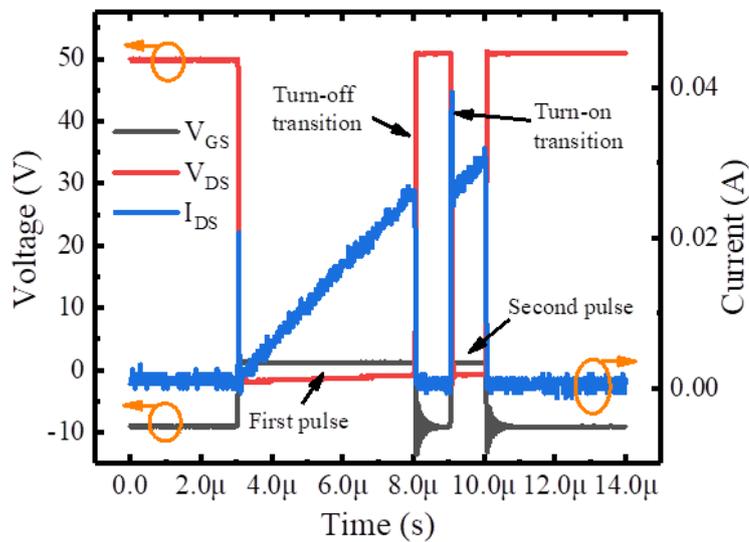
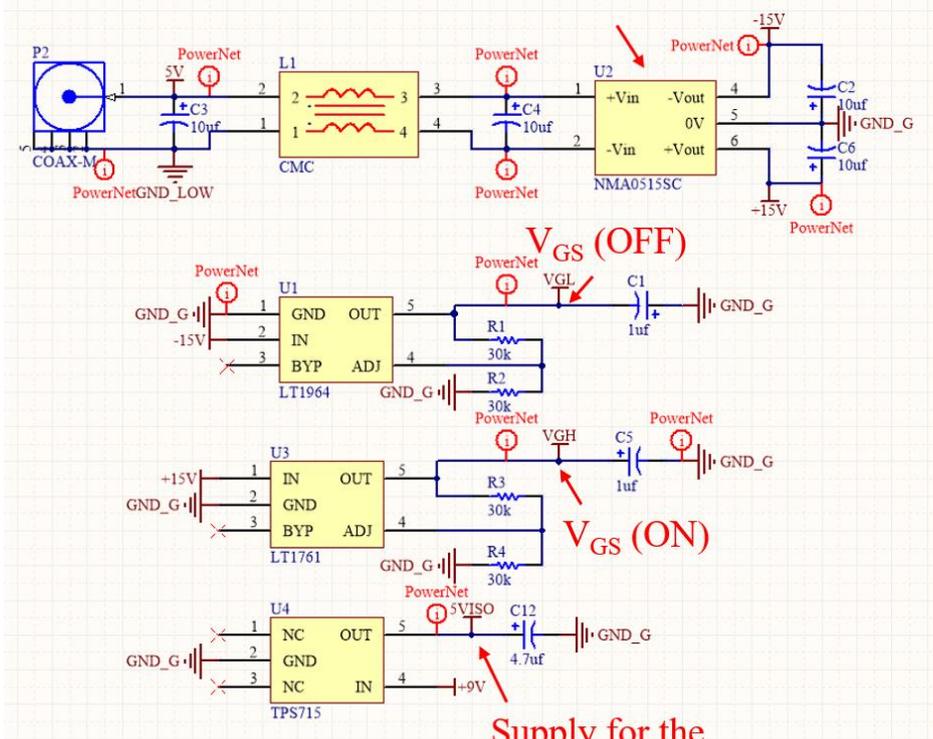


Figure 2-11 An example of measured switching waveforms using DPT.

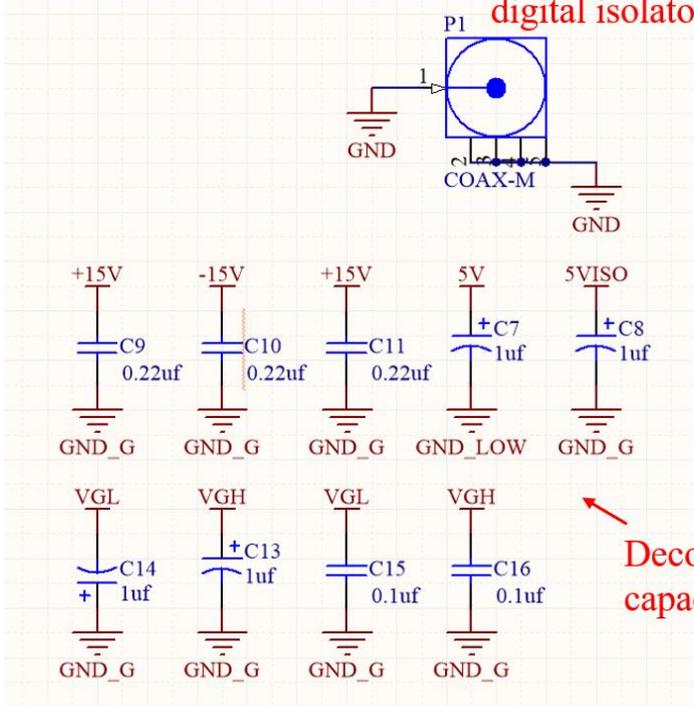
Figure 2-12 shows the schematic of the designed DPT circuit board. Figure 2-12(a) shows the power supply part for the PCB. The design requires one additional power supply of 5 V to provide the power for several integrated circuits (ICs) on the board. An isolated DC-DC converter (Murata NMA0515SC) is used to separate the ground between the power supply and the PCB, and therefore prevents any noises in the mains from coupling into the ground of the DPT. The on-state and off-state supply voltage to the gate are provided by the LT1761 and LT1964 voltage regulators, respectively. Their voltage swing can be modified from -15 V to +15 V and are

suitable for both D-mode and E-mode devices. TPS715 is used to provide +5 V to the digital isolator in the gate driving circuit. A set of decoupling capacitances shown in Figure 2-12(b) are used to stabilise each input and output voltage in the power supply part. Figure 2-12(c) shows the gate driver design and Figure 2-12(d) shows the load of the DPT. The double pulse is provided by a Rigol pulse generator through a BNC connector and a digital isolator (ADuM3100) is used to separate the ground of the mains and the PCB. LM5114 from Texas Instruments is used as the gate driver, which can provide a maximum sink current of 7.6 A and a peak source current of 1.4 A. The drain voltage is also supplied through a BNC connector by SMU 2410. A DC-link capacitor bank of 80 μF in total capacitance is used to handle the current transients in the drain loop during switching. Both drain and gate voltage are measured via BNC connector and the current is monitored by a high band-width current sensor (T&M SDN-414-10).

Isolated DC-DC converter



Supply for the digital isolator (a)



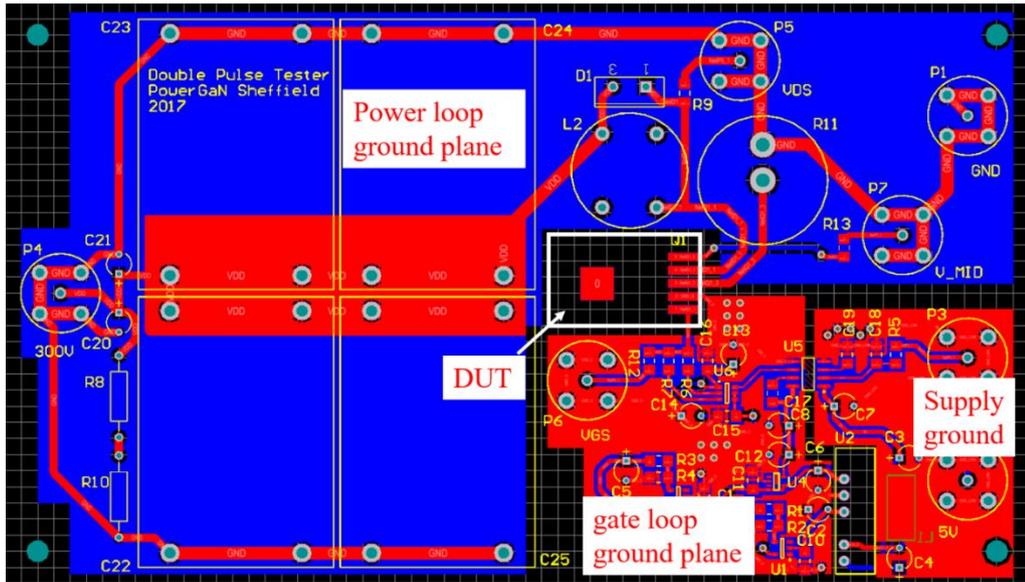


Figure 2-13 Full PCB layout of the DPT.

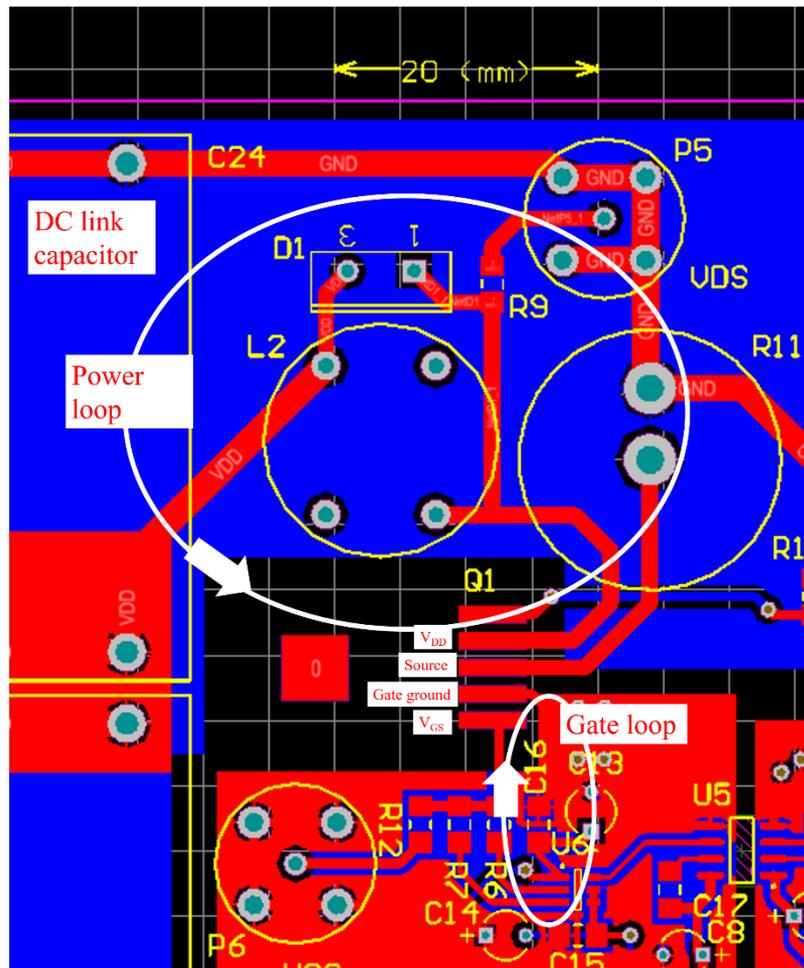


Figure 2-14 Zoom-in picture of the DUT area in the DPT with the gate loop and drain loop highlighted.

2.3.3 Dynamic R_{on} setup

The dynamic R_{on} is an important indicator for GaN based power transistors as it determines the actual conduction loss during switching. Our designed dynamic R_{on} setup simulates the real switching application by introducing a controllable stress in both time and level, before turning on the device for R_{on} measurements.

Figure 2-15 shows the circuit diagram of the dynamic R_{on} setup. Before the measurement, the Si MOSFET is turned on, while the DUT is kept off. After that, both the stress voltage (V_{stress}) and the on-state voltage ($V_{on-state}$) are turned on. At this point, the potential at A is low and is determined by $V_{on-state}$. Therefore, the time after turning on both voltages will not affect the measurement. The large load resistance (33 k Ω) is used to limit the current when the Si MOSFET is on, and thus reduces heating. At the beginning of the measurement, we manually trigger a pulse to the Si MOSFET to turn it off for a desired stress time. The DUT remains off and the potential at A and B increases to V_{stress} . This is the stress stage where the DUT sees the high voltage for a desired stress time. At this stage, the low voltage power supply is protected by the SiC diode. After stressing, the Si MOSFET is turned back on again and the potential at A and B fall back to the on-state value. After 1 μ s of turning on the Si MOSFET, a synchronised pulse is applied to the DUT to turn on the device for 100 μ s. The time gap is to accommodate the turn-on transient of the Si MOSFET. The voltage at A and B are measured at the beginning of this synchronised pulse and the on-resistance can be calculated by the voltage at B together with the current through the 50 Ω resistor, which is given by

$$R_{on} = \frac{50 \cdot V_B}{V_A - V_B} . \quad (2-4)$$

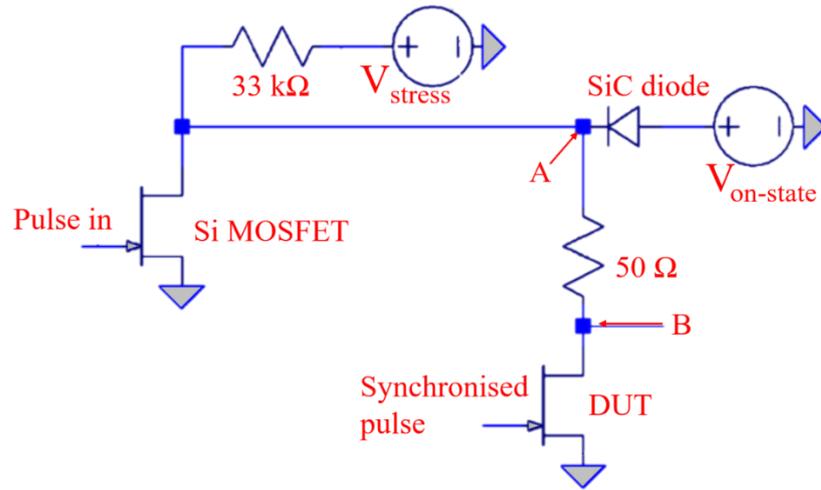


Figure 2-15 Circuit diagram of the dynamic Ron measurement setup.

2.3.4 High voltage capacitance measurement

The intrinsic capacitance including C_{GD} , C_{DS} and C_{GS} are important for estimating the device switching performance and switching figure of merit. Due to pinch-off of the GFP and SFP in the lateral GaN HFETs with an increased drain bias (V_{DD}), C_{GD} and C_{DS} are voltage dependent. High voltage capacitance measurements are used to extract the non-linear capacitance profile, which can be used in the SPICE simulation and converted into input and output charge of the device.

In power transistor, the output capacitance (C_{oss}), reverse capacitance (C_{rss}) and the input capacitance (C_{iss}) are often measured instead of C_{GD} , C_{DS} and C_{GS} . The following relationships are valid,

$$C_{oss} = C_{GD} + C_{DS} \quad (2-5)$$

$$C_{rss} = C_{GD} \quad (2-6)$$

$$C_{iss} = C_{GD} + C_{GS} \quad (2-7)$$

As most of the LCR meter cannot provide a DC bias above 40 V, external circuits are developed for the measurement of C_{oss} , C_{rss} and C_{iss} , as shown in Figure 2-16. To measure C_{oss} , a positive AC signal with 1 MHz frequency and 50 mV amplitude is applied to the drain through a large capacitor of 5 μ F in a 'bias tee', as highlighted in

Figure 2-16(a). The large capacitor in the 'bias tee' provides low impedance path for the AC signal, and protects the LCR meter by blocking the high voltage from the DC

power supply. The value needs to be large enough compared to the measuring capacitance to maintain the measurement accuracy. A high DC bias sweeping from 0 V to 300 V is applied to the drain through a series connection of a large inductor (500 mH) and a resistor (4 k Ω) in the 'bias tee'. The resistor and the inductor together prevent the AC signal from going into the DC power supply. The same 'bias tee' structure can be found on the gate and the source of the DUT. The Low of the LCR output is connected to both gate and source via 'bias tee'. Additional negative gate bias can be applied for D-mode device measurement. To measure C_{rss} as shown in Figure 2-16(b), the source of the device is grounded. Thus, any AC current passing through C_{DS} is coupled to the ground and will not be measured by the LCR meter. To measure C_{iss} , C_{DS} is shorted by connecting both drain and source to the LCR High, as shown in Figure 2-16(c). Note that we usually measure C_{iss} at zero drain bias as C_{GS} has little dependence on the drain voltage. A negative gate bias can be applied to the gate for measuring D-mode devices.

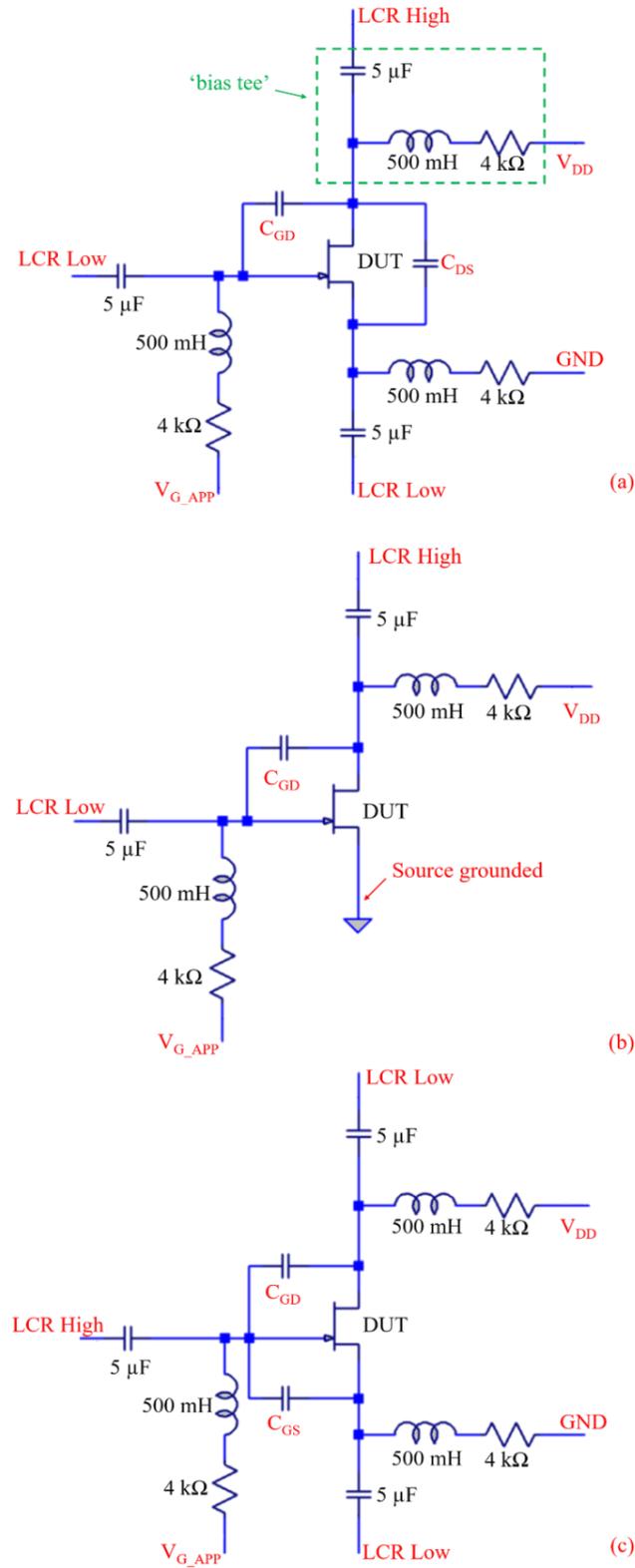


Figure 2-16 Circuit diagrams of high voltage CV setup for the measurement of (a) C_{oss} , (b) C_{rss} and (c) C_{iss} .

2.4 SPICE simulation

SPICE (Simulation Program with Integrated Circuit Emphasis) simulation offers great benefits to the understanding and optimisation of the all-GaN integrated cascode devices. In this study, LTSPICE software is used to simulate the influence of the D-mode threshold voltage on the DC output current of the integrated cascode device (Chapter 3) and to understand the switching behaviour of the cascode in comparison with standalone device (Chapter 4).

Traditional Si JFET model is used to model our fabricated GaN HFETs, due to the lack of commercial GaN SPICE physical models. The Si JFET model [3] in LTSPICE is derived from the FET model of Shichman and Hodges [4], therefore cannot accurately predict the DC and switching performance of GaN HFETs. However, it provides reasonable approximation while the main purpose of applying SPICE simulation in this study is to understand the behaviour of a cascode configuration, which does not require precise modelling of GaN HFETs.

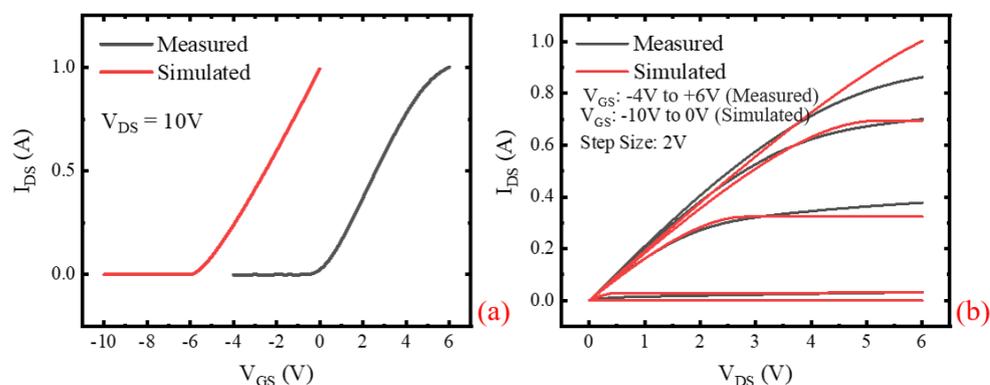


Figure 2-17 Comparison of (a) gate transfer and (b) I-V characteristics between measured and simulated results (using Si JFET model) for an 8mm standalone E-mode device.

Table 2-2 Parameters used in LTSPICE for an 8mm standalone E-mode device.

Threshold (V_{th})	-6 V
Gate swing	10 V (-10V to 0V)
Trans-conductance (g_m)	0.2 S
On-resistance (R_{on})	4.8 Ω

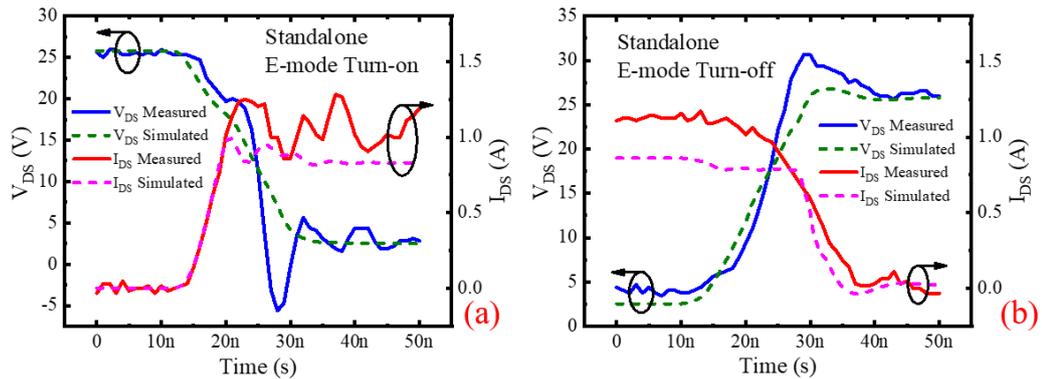


Figure 2-18 Comparison of 25V switching waveforms between measured and simulated results (using Si JFET model) during (a) turn-on and (b) turn-off for an 8mm standalone E-mode device.

Figure 2-17 show the comparison between measured and simulated gate transfer and I-V characteristics of an 8 mm standalone E-mode GaN HFET. The device parameters used for the JFET model are extracted from the measured DC characteristics and are listed in Table 2-2. Note that the JFET model does not allow positive gate bias, therefore the E-mode operation is simulated by keeping the same gate swing for the JFET and GaN HFET. The simulated DC characteristics well match with the experimental results, despite a slight difference in the maximum current in I-V characteristics which could be caused by heating during actual measurement. Figure 2-18 shows the comparison of the turn-on and turn-off switching waveforms between simulated and measured results of the same 8 mm E-mode device. The device is measured using a double pulse tester under drain voltage of 25 V and load current of 1 A. The capacitive parameters for simulation are extracted by C-V measurement. However, the non-linearity of the intrinsic capacitance is not considered which may be the reason for the slight mismatch

between the simulated and experimental results. Overall, the results show a good approximation when using JFET model to simulate GaN HFET.

2.5 Reference

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3 200 V All-GaN Integrated Cascode Configuration

3.1 Introduction

The review of GaN plus Si cascode in Chapter 1 has suggested the suitability of the cascode device for high power and high frequency switching applications due to the mitigation of the Miller effect, leading to an improved switching speed and reduced switching losses [1-2]. However, a few issues have been reported that may negate the speed advantage in the GaN plus Si hybrid cascode devices [3-6]. Firstly, the use of a Si device has been reported to cause an increased delay time in both turn-on and turn-off due to large intrinsic capacitance [1]. As a result, the GaN plus Si cascode becomes less advantageous when compared to the GaN standalone devices. Secondly, the connections between the Si MOSFET and GaN devices result in increased parasitic inductance, which can cause excessive ‘ringing’ effects at fast switching speed thus limiting high frequency operation [5-6]. This brings challenges to the packaging design as reported by several studies on the effect of improved packages for the hybrid cascode devices [5-8]. In addition, the non-integrated cascode structure relies on adding external components when addressing issues such as capacitance mismatch, which will be discussed in detail in Chapter 5. Applying an external capacitor between the drain and gate of the Si device was proposed in [3] and [4] to match the capacitance in the hybrid cascode device and prevent avalanche in the Si device, however, at the expense of additional parasitic inductance and careful designs in the device packaging are required.

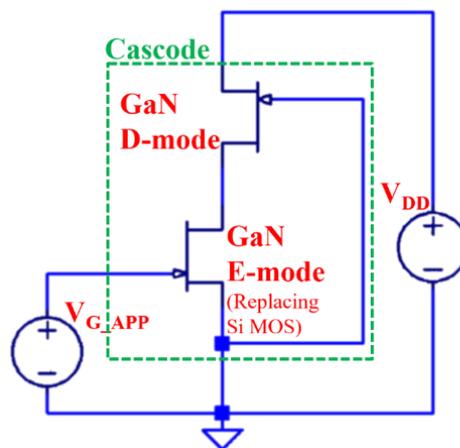


Figure 3-1 Schematic of an all-GaN integrated cascode device.

Therefore, we proposed an all-GaN integrated cascode device by replacing the Si MOSFET with a low voltage GaN E-mode device, as shown in Figure 3-1, so that the issues above can be addressed and the switching speed can be improved. The parasitic inductance can also be minimized by monolithic integration, reducing the oscillation during the turn-off operation [4]. A GaN plus Si fully integrated cascoded diode has been reported, as an integration of GaN based two terminal device [9]. While for three terminal devices, only a few studies on the integrated cascode structure have been reported and are limited to RF applications [10] and [11]. Additionally, there has been no analysis of the interrelationships between the E and D-mode devices, which is required to enable full optimization of the cascode design for switching applications. It is challenging to apply cascode to power switching applications where the conduction loss is more important, due to its intrinsically larger R_{on} compared to the conventional standalone device. However, as the switching frequency increases and the switching energy loss starts to dominate, the integrated cascode structure is expected to be more efficient.

In this Chapter, the design and fabrication of an all-GaN integrated cascode configuration for switching applications are described. The DC characteristics are presented with an analysis of the optimisation requirements for an improved DC output current. The switching performance is explored and compared with equivalent GaN standalone devices. The operational principle of the cascode is discussed and the unique switching mechanism highlighted.

3.2 Experimental

3.2.1 Design and fabrication

Figure 3-2 shows the structures of an all-GaN integrated cascode device and a GaN standalone device. The GaN/AlGaIn/GaN heterojunction structure was grown at Cambridge University on a 6-inch Si substrate using metal-organic chemical vapour deposition. All-GaN monolithically integrated cascode devices were fabricated using a standard GaN HFET fabrication process, as described in Chapter 2. Firstly, mesa isolation was performed by inductively coupled plasma etching to define the device area. An ohmic metal stack (Ti/Al/Ni/Au) was deposited and annealed at 830 °C to form the source and drain contacts. A typical contact resistance of 0.7 $\Omega \cdot \text{mm}$ was obtained from transmission line model measurements. Devices were passivated with

70 nm SiN_x using plasma enhanced chemical vapour deposition (PECVD) and a 1.5 μm gate window was opened by etching through the SiN_x layer using reactive ion etching (RIE) for both the E-mode and D-mode gate. A CHF₃ plasma-treatment in an RIE system was performed on the E-mode gate window to implant fluorine and shift the threshold voltage, V_{th} , from negative to positive [12]. A nominally 20 nm thick SiN_x layer was deposited using PECVD prior to the T-shaped Ni/Au gate metal formation step to form a metal-insulator-semiconductor (MIS) gate structure in the E-mode section. A Schottky gate was used for the D-mode part of the cascode structure. A gate-connect field plate (GFP) was formed on the gate of the D-mode part in the cascode configuration. Finally, devices were passivated with 300 nm of PECVD SiN_x before the formation of the source-connected field plate (SFP), and Ti/Au bond pads were deposited after via opening in this SiN_x. Devices with gate widths, W_g , of 100 μm and 8 mm were fabricated. For comparison, equivalent GaN standalone devices (E-mode and D-mode) were also fabricated at the same time.

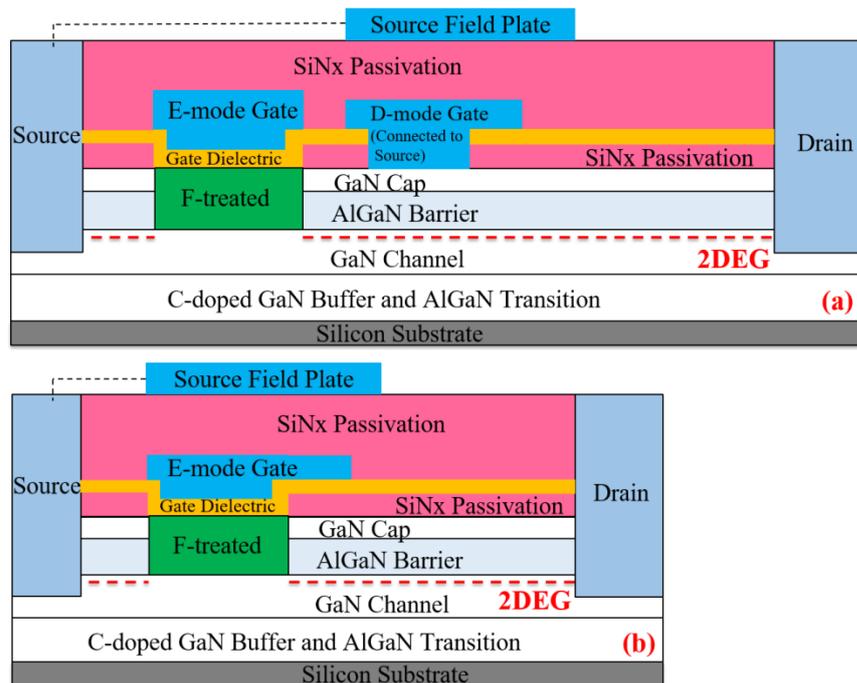


Figure 3-2 Device structure of (a) an all-GaN integrated cascode device and (b) a GaN standalone device with source field plate.

Figure 3-3 shows the optical image of a 100 μm integrated cascode device. Compared to the typical GaN standalone device, the cascode structure features an additional Schottky gate, which acts as the gate of the D-mode device and blocks the

high voltage. The D-mode gate is internally connected to the source of the E-mode part. Both structures have a gate length of $1.5 \mu\text{m}$, GFP extension (L_{GFP}) of $1 \mu\text{m}$ and SFP (L_{SFP}) extension of $2 \mu\text{m}$. The source-drain separation (L_{SD}) of the standalone and the cascode devices are $16 \mu\text{m}$ and $22.5 \mu\text{m}$ (additional $1.5 \mu\text{m}$ D-mode gate length and $5 \mu\text{m}$ gap between D-mode and E-mode gates), respectively.

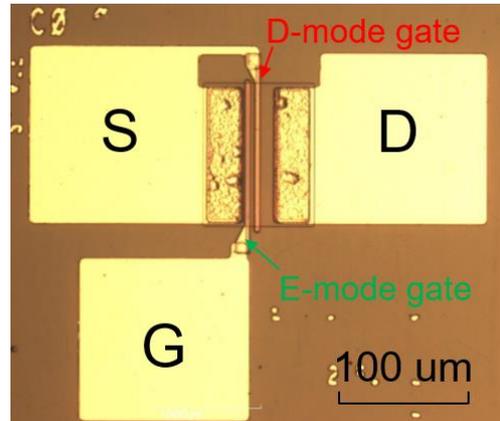


Figure 3-3 Monolithically integrated AlGaN/GaN HFET cascode configuration with gate width of $100 \mu\text{m}$.

3.2.2 DC characteristics

Figure 3-4 shows the I-V characteristic of the cascode device at $V_{DS} = 10 \text{ V}$ and V_{GS} sweeping from -4 V to $+10 \text{ V}$. An on-resistance (R_{on}) of $27 \Omega \cdot \text{mm}$ (normalized to the gate width) is measured from the cascode device, which is higher than other reported lateral standalone devices. The higher R_{on} is a result of larger device area ($1.5 \mu\text{m}$ D-mode gate length and $5 \mu\text{m}$ gap between D-mode and E-mode gates) to accommodate both D-mode and E-mode parts.

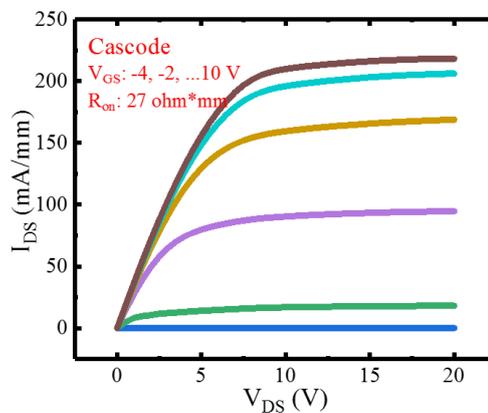


Figure 3-4 I-V characteristic of a $100 \mu\text{m}$ gate width cascode device.

Figure 3-5 shows the gate transfer characteristics of 100 μm standalone D-mode, E-mode and cascode devices. The all-GaN integrated cascode device has a positive V_{th} of +2 V with an output current of 200 mA/mm at $V_{DS} = 10$ V and $V_{GS} = +10$ V. The standalone D-mode device with a Schottky gate has a V_{th} of -5.5 V and an output current around 575 mA/mm at $V_{DS} = 10$ V and $V_{GS} = +2$ V, while the E-mode device has the same V_{th} as the cascode but a higher output current close to 300 mA/mm. Since both the E-mode and D-mode parts have the same W_g , the output current of the cascode structure is limited by the section with the lower current drivability, which is the E-mode part in this case. However, a lower output current of the cascode device compared to its equivalent standalone E-mode device is observed and this indicates that some optimisation of the design is required to achieve the maximum cascode current.

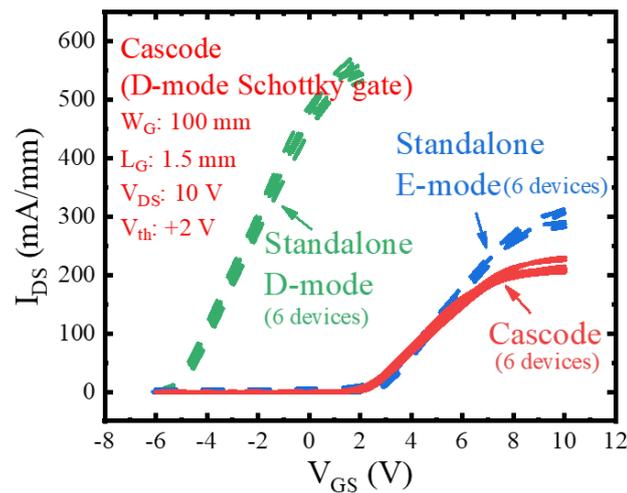


Figure 3-5 Gate transfer characteristics of all-GaN integrated cascode devices together with equivalent standalone E-mode devices and standalone D-mode devices (6 devices for each).

To facilitate the full understanding of how the cascode configuration works, particularly the voltage transients from off-state to on-state between the E-mode and D-mode, a cascode device with an additional ohmic pad between the D-mode gate and the E-mode gate was fabricated, as shown in Figure 3-6. This layout does not change the I-V characteristics due to the negligible contact resistance of the ohmic

pad compared to the total R_{on} , but allows the potential between the D-mode gate and the E-mode drain (V_{DS-E}) to be monitored.

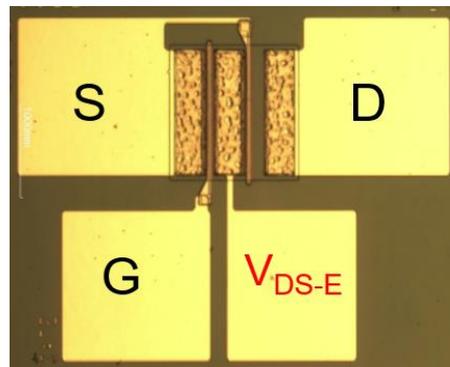


Figure 3-6 An optical image of a 100 um cascode device with an additional pad connecting to the internode.

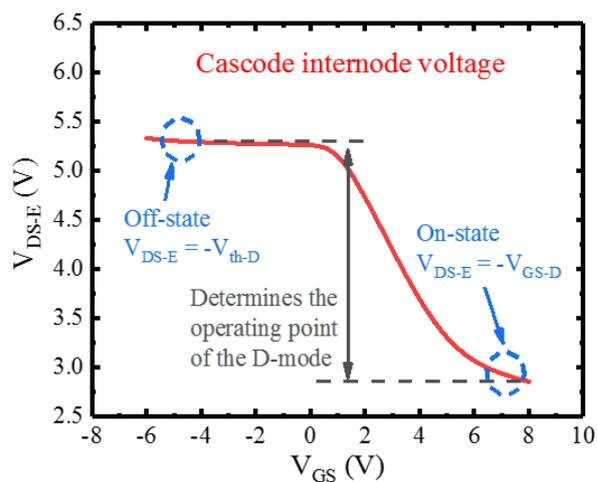


Figure 3-7 The internode voltage (V_{DS-E}) measured as a function of E-mode gate bias. The difference between and on and off-state value determines the operating point of the D-mode device and can limit the output current of the cascode.

Figure 3-7 illustrates the measured internode voltage (V_{DS-E}) as a function of the E-mode gate bias, V_{GS-E} . During the off-state ($V_{GS-E} < V_{th-E}$), $V_{DS-E(OFF)}$ is equal to 5.3 V, which is the magnitude of the D-mode threshold voltage (V_{th-D}), and the channel under the D-mode gate metal is fully depleted. When V_{GS-E} increases to the on-state ($V_{GS-E} > V_{th-E}$), V_{DS-E} drops and the channel under both D-mode and E-mode gates begin to conduct. At the on-state ($V_{GS} = +8$ V), $V_{DS-E(ON)}$ is equal to 2.8 V, which is effectively the gate voltage of the D-mode device ($-V_{GS-D}$), and is determined by the

on-state current (I_{DS-C}) and the on resistance of the E-mode device (R_{on-E}). During on-state, the D-mode is operating at ($V_{DS-E(ON)} < V_{DS-E(OFF)}$), which is roughly 2.5 V. As a result, the output current of the cascode device is limited to 200 mA/mm, according to the estimated operating point of the D-mode part shown in Figure 3-5. Therefore, the on-state internode voltage determined by the E-mode on-resistance may limit the operating point of the D-mode part for a mismatched cascode and leads to the decrease in the output current.

To explore the potential solution, we first assume that the cascode device is able to provide its maximum output current, which is also the E-mode maximum current $I_{DS-E,max}$. The voltage drop across the E-mode device during on-state is then given by,

$$V_{DS-E(on)} = I_{DS-E,max} * R_{on-E} . \quad (3-1)$$

Now we consider the D-mode device at its on-state, for a matched cascode, we should have

$$g_{m-D} * (-V_{DS-E(on)} - V_{th-D}) \geq I_{DS-E,max} . \quad (3-2)$$

By substituting (3-1) into (3-2), and rearranging, we get

$$-V_{th-D} \geq I_{DS-E,max} * \left(\frac{1+g_{m-D}*R_{on-E}}{g_{m-D}} \right) . \quad (3-3)$$

To optimise the output current of the cascode device, one could reduce the R_{on} of the E-mode part or increase the g_m of the D-mode part, so that (3-3) is fulfilled for a given V_{th-D} . However, R_{on} is ultimately limited by channel and contact resistances and hence is difficult to control, while g_{m-D} can also be difficult to improve further. Alternatively, a more elegant solution is to engineer V_{th-D} and hence control $V_{DS-E(ON)}$ to ensure the D-mode device is biased at the desired V_{GS} during the on-state. However, a more negative V_{th-D} beyond the optimum voltage also increases $V_{DS-E(OFF)}$ and hence increases the total energy stored at the internode of the cascode during switching. This may contribute to an increased switching loss, which is analysed in detail in Chapter 4. Therefore, it is vital to optimise the D-mode V_{th} to match the output current of both E-mode and D-mode sections for maximum overall current.

3.2.3 Output current optimization

An LTSPICE simulation of the all-GaN cascode based on a Si JFET model was conducted to verify the analysis in the previous section and to estimate the optimum V_{th-D} for the maximum overall current. Figure 3-8 shows the schematic diagram of the simulation circuit. The device parameters used in the simulation were extracted experimentally as shown in Table 3-1. Capacitive elements were not considered for the DC simulations.

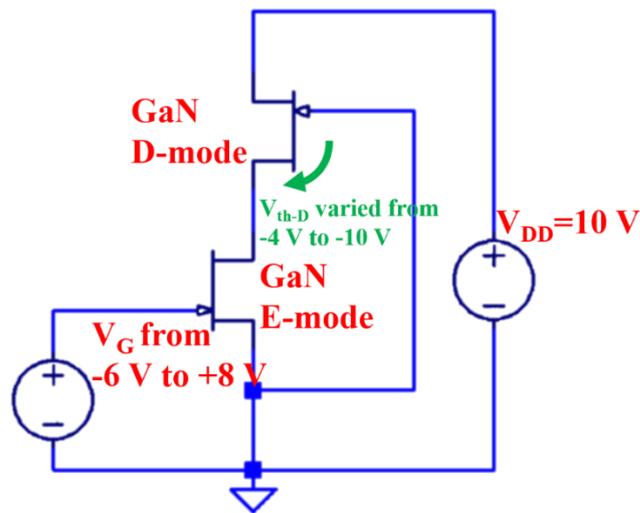


Figure 3-8 Simulation circuit used to study the influence of the D-mode V_{th} on the output current of the cascode device.

Table 3-1 Summary of device parameters used in LTSPICE for V_{th} engineering.

	D-mode part	E-mode part
Gate width (W_g)	100 μm	100 μm
Trans-conductance (g_m)	150 mS/mm	75 mS/mm
On-resistance (R_{on})	13 $\Omega \cdot \text{mm}$	14 $\Omega \cdot \text{mm}$
Threshold voltage (V_{th})	-4 V to -10 V	+2 V

Figure 3-9 shows the simulated output current of a cascode device with varying V_{th-D} . The output current increases with increasing (negative) V_{th-D} as a result of increasing $V_{DS-E(ON)}$ as discussed above. The simulated current reaches its maximum value at a V_{th-D} of -9.2 V. At this point, the left hand side equals the right hand side in (3-3) and

hence the D-mode operates at V_{GS-D} such that it can just provide itself with the maximum current (E-mode). Further increase (negative) in V_{th-D} does not increase the drain current, which is limited by the E-mode part.

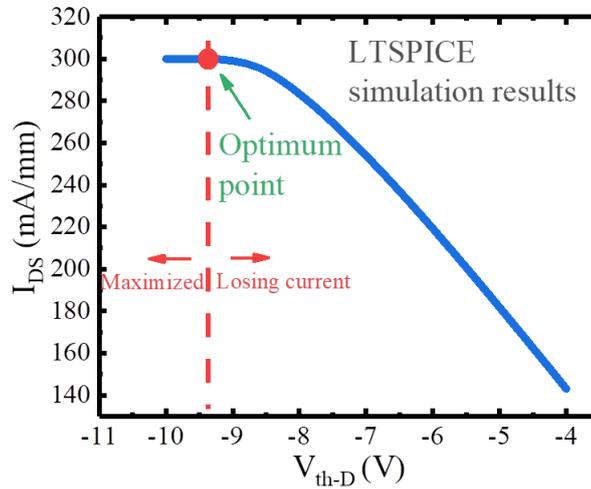


Figure 3-9 Simulation results of drain current indicating an optimum D-mode V_{th} that leads to the maximum output current.

In order to verify the simulated results, two cascode structures were fabricated: one with a Schottky gate structure for the D-mode part and the other one with a nominally 10 nm PECVD SiN_x MIS gate to shift V_{th-D} more negative, as shown in Figure 3-10. Figure 3-11 compares V_{th} of GaN standalone D-mode devices with a MIS gate and Schottky gate. V_{th} of the D-mode devices is shifted from -5.5 V to -8.5 V with the MIS gate. This shift originates from the reduction in the effective capacitance between the gate metal and the 2DEG underneath the gate. For a certain amount of charge in the 2DEG that needs to be removed to pinch off the channel, a larger gate voltage is required with the reduced capacitance.

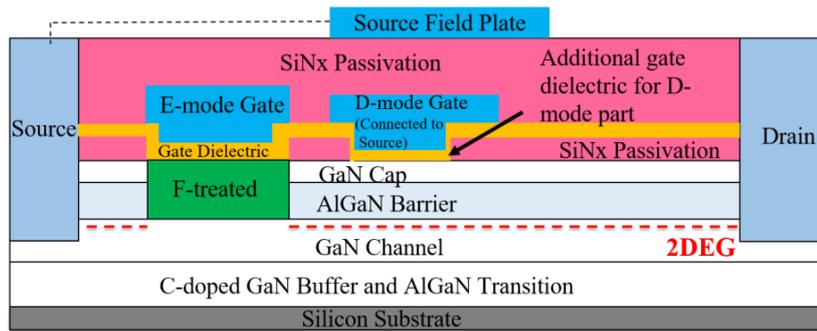


Figure 3-10 Device structure of an all-GaN integrated cascode device with a MIS gate on the D-mode part.

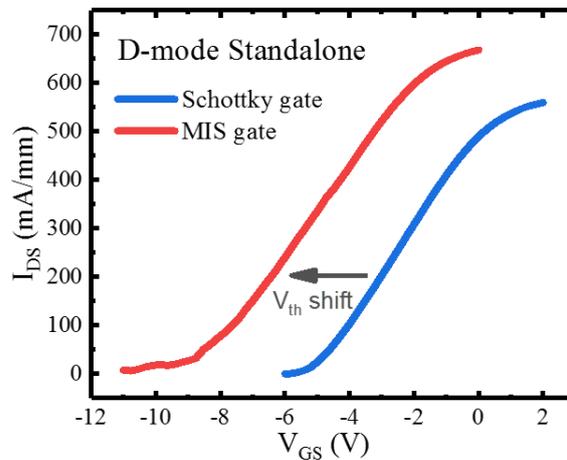


Figure 3-11 An increase in the threshold voltage of the D-mode with MIS gate compared to Schottky gate.

The internode voltage shown in Figure 3-12 indicates an improved operating voltage of the D-mode part. As a result, the output current of the cascode configuration, as shown in the gate transfer characteristics in Figure 3-13, has been successfully improved from 150 to 300 mA/mm for the device with a D-mode MIS gate which is at a similar level as the GaN standalone E-mode device at $V_{GS} = 10$ V. This shows an excellent agreement with the simulated results and highlights the importance of matching both D-mode and E-mode to provide the maximum output current in the cascode devices.

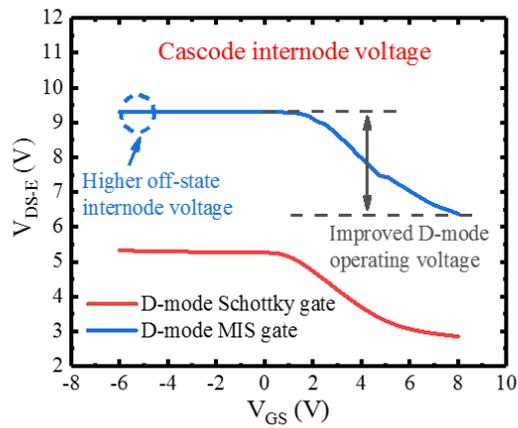


Figure 3-12 An increased operating point of the D-mode part is observed for the cascode with a MIS gate D-mode section.

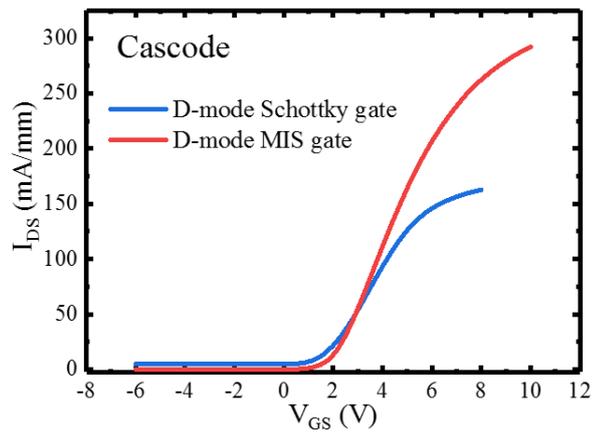


Figure 3-13 Cascode output characteristics showing an improved current from the optimised cascode structure.

3.2.4 Switching performance

8 mm gate width multi-finger gate all-GaN integrated cascode (Figure 3-14) and standalone devices were used for comparing the switching performance. The DC gate transfer characteristics of both devices are shown in Figure 3-15. Note that the normalised current of both structures are much smaller than that measured for the 100 μm devices in the previous section. This scaling issue is due to a combination of the measurement system resistance, device self-heating and series resistance of the gate. Figure 3-16 shows the four terminal breakdown results of the 8 mm cascode

device upto 150 V. The device is capable of high voltage operation, despite a slight high leakage current close to mA range dominated by the source current.

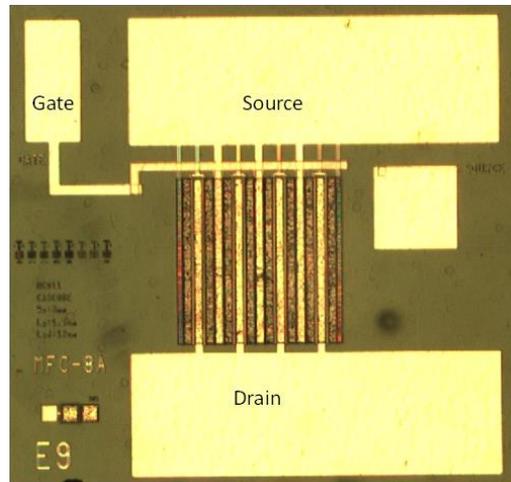


Figure 3-14 An optical image of an 8mm all-GaN integrated cascode device.

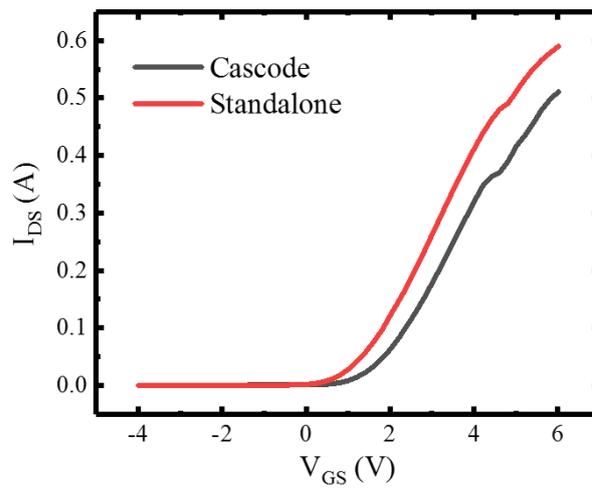


Figure 3-15 Gate transfer characteristics of an 8mm integrated cascode and an 8mm standalone device.

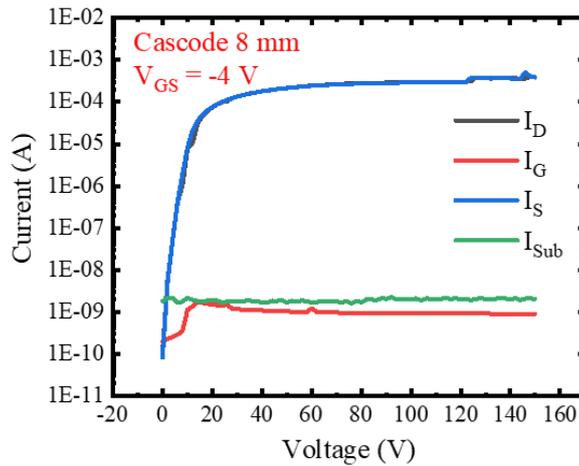


Figure 3-16 Four terminal breakdown measurement results of an 8mm integrated cascode device.

A double pulse tester (DPT) with an inductive load, as described in Chapter 2, was used to test the hard-switching performance of the devices. Figure 3-17 shows the simplified circuit diagram of the measurement setup of the DPT for the devices. A 0.5 mH inductive load was used to deliver a 0.4 A load current and a commercial gate driver supplying a voltage from -4 V to +6 V was used to switch on the device. A high gate resistor (100 Ω) was used for both $R_{G(ON)}$ and $R_{G(OFF)}$ to limit the gate drive current and hence slow the switching speed to better enable the switching comparisons. The load current to peak gate current ratio was around 10:1. Schottky diodes were used in both gate and load loops to minimise the reverse recovery time. The devices were wire bonded to a printed circuit board for the measurement which is shown in Figure 3-18. While it is difficult to maintain the same geometry of the bonding wires of the two devices, they are kept as close as possible. The gate voltage, drain current and drain voltage were monitored and recorded by a LeCroy WaveSurfer oscilloscope.

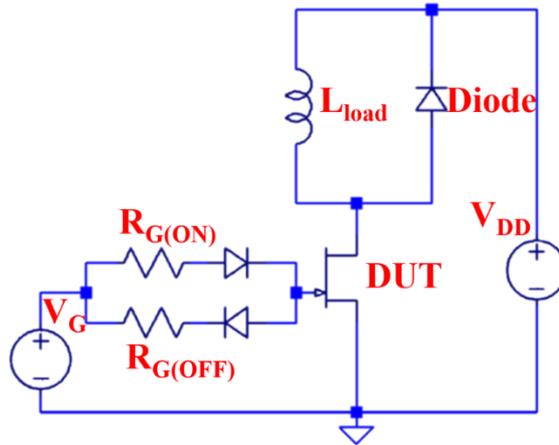


Figure 3-17 Circuit diagram of Double Pulse Tester for switching speed measurement.

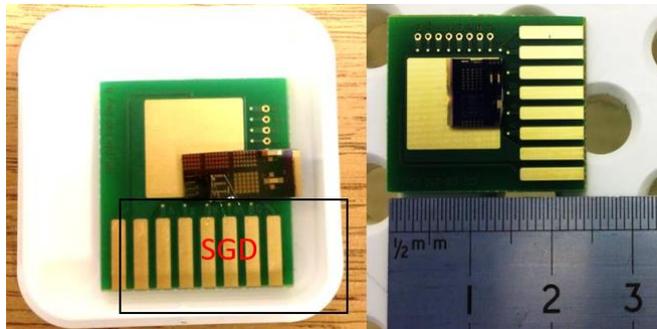


Figure 3-18 An optical image of the wire bonded device.

The switching speed of both cascode and GaN standalone devices were measured at 200 V drain bias. Detailed switching analysis of the cascode configuration is presented in Chapter 4. Therefore, in this section, we will simplify the explanation of the switching waveforms and extract the voltage and current rise (fall) time for comparison. Figure 3-19(a) shows the turn-on transition of the cascode and the standalone device. From $t_0 - t_1$, the current in the cascode (I_{DS}) rises up to the load current value after V_{GS} of both the E-mode and D-mode parts reach the value that can provide the load current. After that, the voltage of the cascode (V_{DS}) drops to the on-state voltage during $t_1 - t_2$. The overshoot of the current during the interval $t_1 - t_2$ is due to the discharge of the parallel capacitance in the load loop. Figure 3-19(b) shows the turn-off transition. From $t_0 - t_2$, V_{DS} rises up first to 200 V after V_{GS} falls below V_{th} . In the interval of $t_0 - t_1$, I_{DS} steps down from the load current due to the charging of the parasitic parallel capacitance in the load loop [1-2]. The ringing effect during $t_0 - t_2$ is caused by the parasitic inductance in the circuit. The

standalone device shows an increased ringing amplitude compared to the cascode which could be caused by differences in the wire bonding geometry detail. However, this should have little influence on the comparison. V_{DS} reaches 200 V at t_2 , where I_{DS} starts to drop and the turn-off transition ends at t_3 .

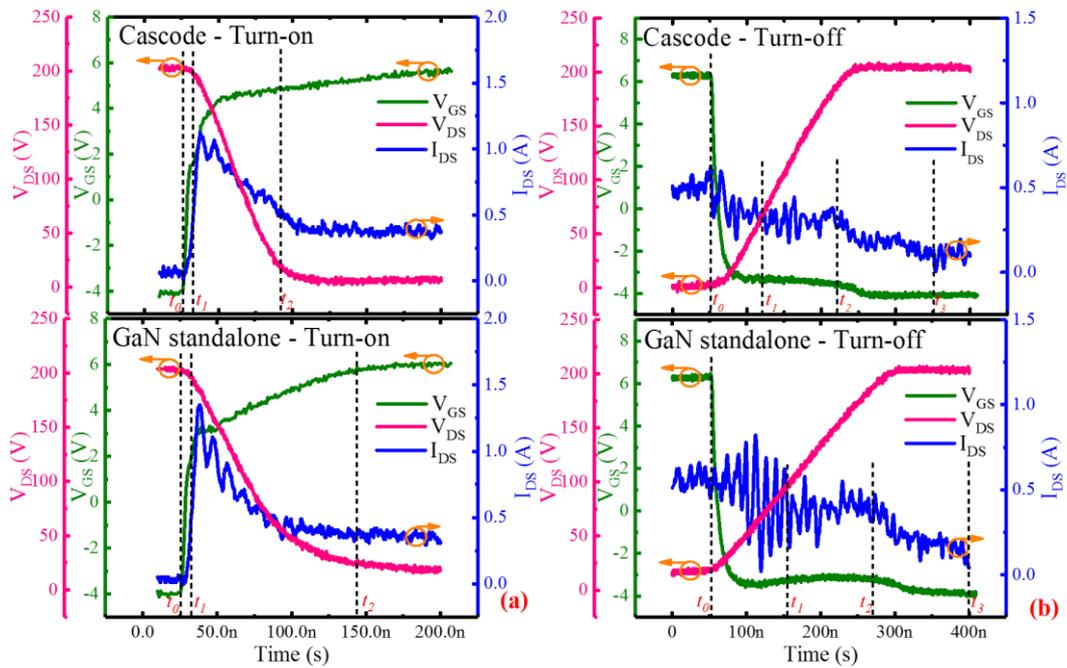


Figure 3-19 200V (a) turn-on and (b) turn-off switching waveforms for 8 mm cascode and 8 mm GaN standalone devices.

Results of switching speed and energy loss for both devices are summarized in Table 3-2. The rise/fall times of V_{DS} and I_{DS} are extracted from 10% of their peak values to 90%. The energy loss is calculated by the integration of the $I \cdot V$ product during the switching transition period. For the first time, we demonstrate a faster switching speed of the all GaN integrated cascode device compared to the GaN standalone device, resulting in approximately 35% and 21% less in the turn-off and turn-on switching energy losses, respectively.

Table 3-2 Summary of switching results at 200 V for the all-GaN integrated cascode and GaN standalone devices.

		Cascode	GaN standalone
<i>Turn-on</i>	<i>Current rise time (t_{r_I})</i>	5 ns	5 ns
	<i>Voltage fall time (t_{f_V})</i>	51 ns	104 ns
	<i>Turn-on energy loss (E_{on})</i>	5.55 μJ	7.02 μJ
<i>Turn-off</i>	<i>Current fall time (t_{f_I})</i>	110 ns	110 ns
	<i>Voltage rise time (t_{r_V})</i>	134 ns	200 ns
	<i>Turn-off energy loss (E_{off})</i>	9.39 μJ	14.41 μJ

3.3 Discussion

Inspection of Figure 3-10 reveals the possibility of the D-mode gate acting as a SFP due to the MIS structure. To understand the operational difference between the integrated cascode configuration and the standalone device, a TCAD simulation based on our device structures was carried out by Dr Kean Boon Lee, as shown in Figure 3-20(a) and (b). The device geometries including FP extensions used in the simulation are based on our fabricated devices. A 2DEG concentration of $1.2 \times 10^{13} \text{ cm}^{-2}$ is assumed with AlGa_{0.3}N barrier thickness of 25 nm. F- dopant level of $5 \times 10^{18} \text{ cm}^{-3}$ is used and is assumed uniformly distributed across the AlGa_{0.3}N barrier under E-mode MIS gate. As the D-mode gate is located on (for Schottky gate) or close to the semiconductor (for MIS gate) in the cascode, the channel under the D-mode gate will be fully depleted before the channel between the D-mode and E-mode gates as the off-state drain bias increases. Once the channel under the D-mode gate is depleted (V_{th} for the Schottky and the MIS gate is 5 V and 9 V, respectively), the region between the D-mode and E-mode gates is effectively shielded from the drain bias and the 2DEG is retained as observed in the TCAD simulation in Figure 3-20(c) and (e). This leads to reduction in the Miller effect as the Miller capacitance becomes the gate-drain capacitance of the E-mode part (C_{GD-E}) and is only subject to a relatively low voltage (which is equal to the D-mode gate V_{th}) and not the full drain bias during switching. On the other hand, the GaN standalone device does not exhibit such behaviour as the depletion region extends continuously from the gate towards the drain as shown in Figure 3-20(d) and (f) at high drain voltage. As a result, C_{GD} is subject to the high drain voltage during the switching processes. Therefore, the

fundamental difference between the cascode and the standalone device is the presence of 2DEG in the region between D-mode and E-mode gates during the off-state in the cascode, which leads to the reduced Miller-effect and the unique switching mechanism.

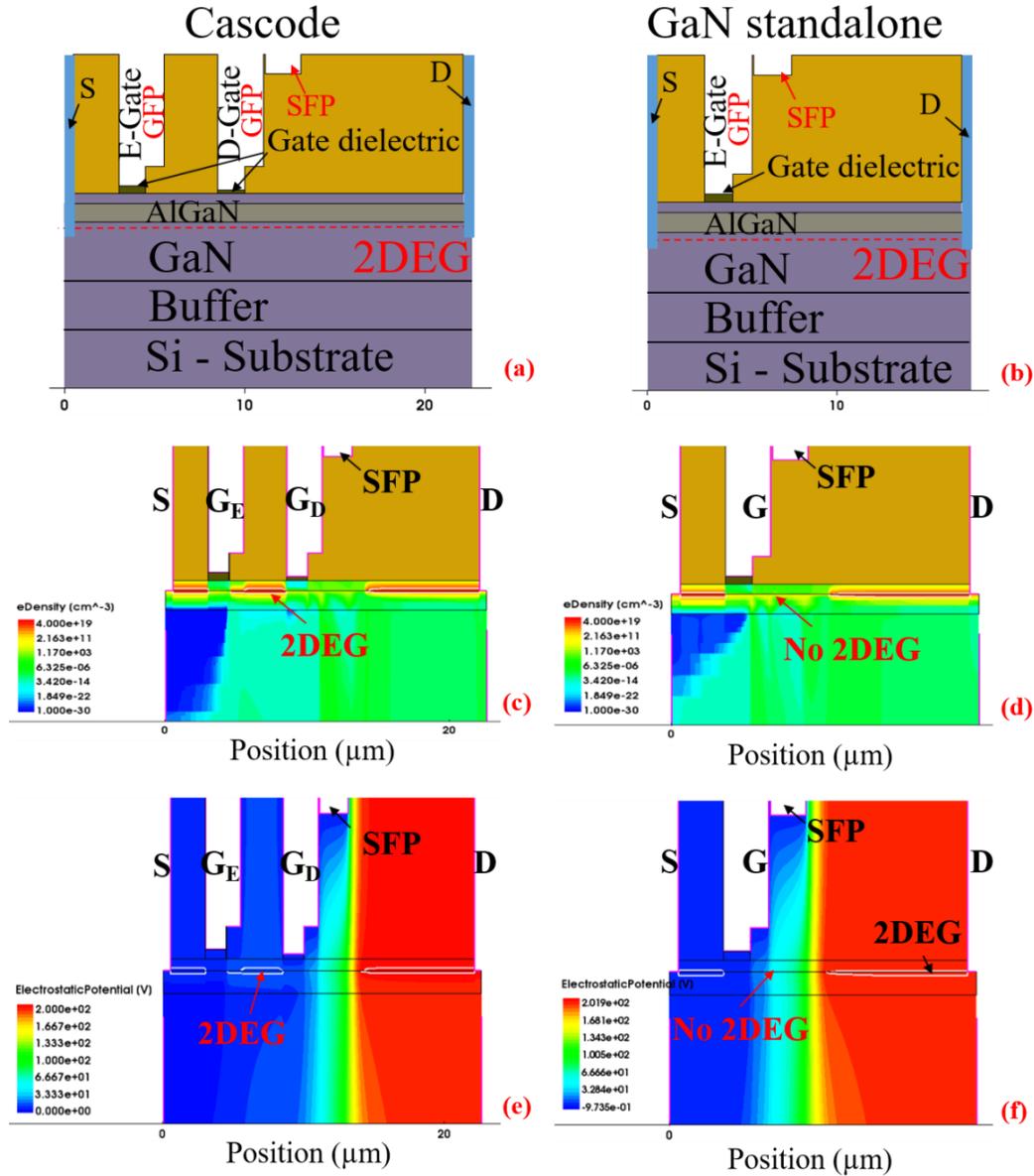


Figure 3-20 Device structures of (a) cascode and (b) standalone device used in TCAD simulation. TCAD simulation of electron density for (c) integrated cascode and (d) GaN standalone device during off-state at $V_{DS} = 200$ V and $V_{GS_E-mode} = 0$ V. TCAD simulation of electrostatic potential for (e) integrated cascode and (f) GaN standalone device during off-state at $V_{DS} = 200$ V and $V_{GS_E-mode} = 0$ V. The integrated cascode device is with $L_{SD} = 22.5$ μm , $L_{GD} = 12$ μm , $L_{GFP} = 1$ μm and $L_{SFP} = 2$ μm . The GaN standalone device is with $L_{SD} = 16$ μm , $L_{GD} = 12$ μm , $L_{GFP} = 1$ μm and $L_{SFP} = 2$ μm . A uniform fluorine concentration with sheet density of 1.2×10^{13} cm^{-2} in the AlGaIn barrier under E-mode MIS gate was used in the simulation.

The detailed analysis on the switching behaviour of the cascode and the origin of the speed advantage is presented in Chapter 4. In this section, we will highlight the reduced Miller-effect and the fundamental charging mechanisms of both devices, leading to the observed differences in the switching speeds.

During turn-on, because the effective Miller capacitance is shifted to C_{GD-E} at the internode, the majority of the energy stored in the output capacitance of the cascode device is dissipated with no Miller-effect. In addition, the energy stored in C_{DS-D} is discharged through the D-mode channel only, as shown in Figure 3-21(a). Therefore, the fact that our D-mode device has a higher trans-conductance (g_m) and current drivability, which enables a larger discharging current within the D-mode channel, also contributes to the faster turn-on speed for the cascode device. During turn-off, the output capacitance of the cascode device is charged up to the high voltage by the full load current which is normally higher than the current in the gate loop, while the charging process of the output capacitance is limited by the current at the gate node in the standalone device as illustrated in Figure 3-21(b). This larger charging current difference is the main reason for the cascode device to be more advantageous in turn-off compared to turn-on, as observed in our experimental and in [1], [13] and [14]. The turn-off advantage strongly depends on the load current to peak gate current ratio [1]. With a good gate driver and small gate resistor to provide sufficient gate current, Miller effect will not control the switching speed, and thus the switching performance of the standalone device is expected to be comparable to that of cascode device [8]. However, in this case the cascode device would still benefit from a lower di/dt in the gate loop to achieve the same switching speed. In addition, the availability of gate drivers with current capability close to the load current is limited in high current applications.

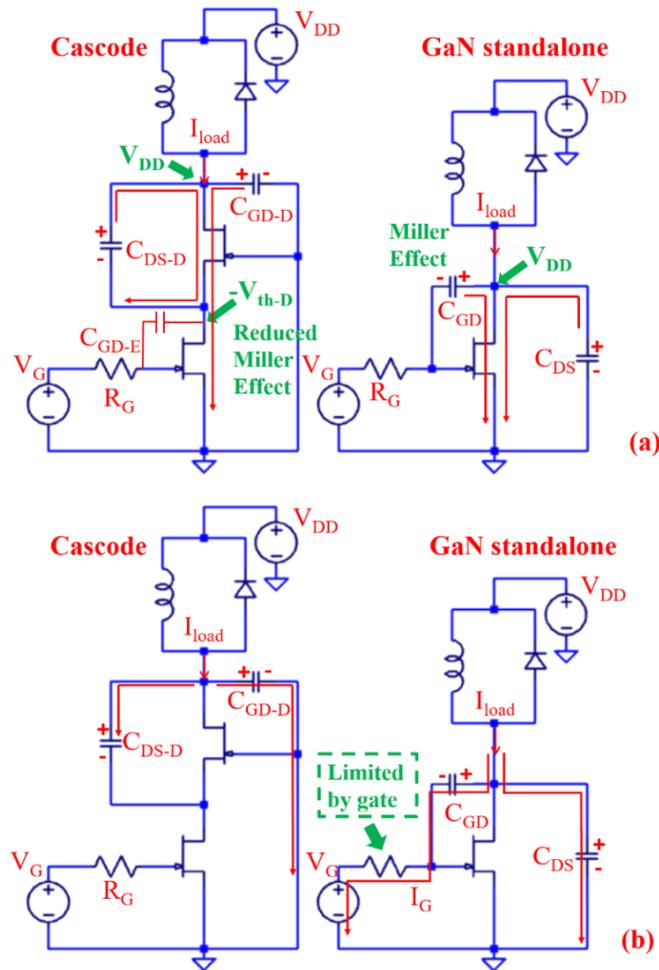


Figure 3-21 The charging and discharging paths of the output capacitance in the cascode device and GaN standalone device with SFP during (a) turn-on process and (b) turn-off process

These observations show that, for practical high frequency and high power switches, the cascode device will have lower switching losses compared to the equivalent standalone device. The price to pay for this advantage is a slightly more complex structure and a higher specific on-resistance, which could be the reason that few studies were reported for GaN or SiC systems on the integrated cascode structures for power applications. However, in applications where switching energy loss is the main concern, the integrated cascode structure can be more suitable with better efficiency.

3.4 Conclusion

The all-GaN integrated cascode configuration is an excellent candidate for high frequency high power applications due to the reduced Miller effect and reduced parasitics. Devices were fabricated with a positive V_{th} of +2 V and output current of 300 mA/mm. Careful optimization of the D-mode device threshold voltage is required to achieve maximum cascode current drivability, which equals the output current of its E-mode part. The fundamental operational difference between an integrated cascode device and GaN standalone device is discussed using TCAD simulation. This shows that the presence of the 2DEG in the region between D-mode and E-mode gates during the off-state is the key to enable the device cascode switching behaviour. For the first time, we demonstrate the relatively faster switching speed and 35% (21%) less in turn-off (turn-on) switching energy loss under 200 V hard switching measurement for the all-GaN integrated cascode devices compared to the equivalent GaN standalone devices. The advantage originates from the reduced effective Miller-capacitance and the unique switching mechanisms in the cascode configuration. Compared with the GaN standalone device, the cascode can achieve a given switching frequency but with less current requirement in the gate driving circuit. As power increases, a greater benefit will accrue from switches incorporating a cascode structure.

3.5 References

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4 An analytical study on the switching behaviour of the all-GaN integrated cascode

4.1 Introduction

The result in Chapter 3 implies the suitability of the all-GaN integrated cascode configuration for high power and high frequency applications. However, the conditions and the mechanisms needed for the integrated cascode to explain the switching advantage have not been fully understood. In addition, the design criteria for an all-GaN integrated cascode configuration with optimum switching performance has not been discussed. Therefore, a theoretical analysis of the switching behaviour of the integrated cascode configuration is necessary to predict the switching performance, and thus identify both the origin of the speed advantage and the optimisation criteria.

There are a few theoretical studies on the hybrid cascode structure including GaN HFET + Si MOSFET and SiC JFET + Si MOSFET [1-3]. In [1], the author presents an analytical loss model of the GaN + Si cascode configuration and verifies it by comparing with experimental results. By using the equations derived, the switching loss at each switching stage can be estimated. In [2], the switching behaviour of a SiC JFET + Si MOSFET cascode has been divided into several stages and analysed mathematically. The work in [3] was focused on the effective output capacitance in the hybrid cascode structure and presented optimisation methods for a reduced switching energy loss based on derived capacitance equations. However, the switching time of the cascode cannot be estimated from those studies and there is insufficient theoretical comparison with the standalone device to explore the origin of the speed advantages. Our initial study in [4] addressed the time-dependent equations for each stage of the cascode switching process but was based on a gate driver with a constant current source. A voltage source gate driver better simulates realistic switching behaviour and thus predict the switching performance which can be feedback to the device design stage.

In this Chapter, the switching behaviour of the all-GaN integrated cascode device was analysed under a voltage source gate driver. The turn-on and turn-off switching

processes were discussed individually and the switching time for each stage calculated. The derived time-dependent equations were verified with LTSPICE simulation. Theoretical voltage switching time and switching energy loss comparisons between the integrated cascode and the equivalent standalone device were conducted. The conditions and the mechanisms for the integrated cascode to show switching advantages were explored. Key device parameters that affect the switching performance of the cascode were identified and the design criteria of the all-GaN integrated cascode for optimum switching performance is presented. These analyses will enable prediction of the cascode switching speed and provide guidelines on how to optimise the cascode for the best switching performance.

4.2 Switching analysis of an all-GaN cascode configuration

In this section, the turn-on and turn-off switching process of an all-GaN integrated cascode is analysed theoretically. The equivalent circuit of the current flow for charging (discharging) the intrinsic capacitances at each stage is presented. Time-dependent equations for each stage are derived, assuming switching under a typical inductive load condition without any external influences as shown in Figure 4-1. For simplicity, the freewheel diode is assumed to be ideal with a zero reverse recovery capacitance. The gate driver is also regarded as ideal, supplying a step voltage from the off-state gate-source voltage ($V_{G-APP(OFF)}$) to the on-state gate-source voltage ($V_{G-APP(ON)}$). To simulate practical situations, the gate driving current are assumed insufficient compared to the load current. Therefore, the switching transitions in the analysis are assumed to be affected by the Miller effect. The E-mode part and the D-mode part in the cascode are assumed to have the same current drivability.

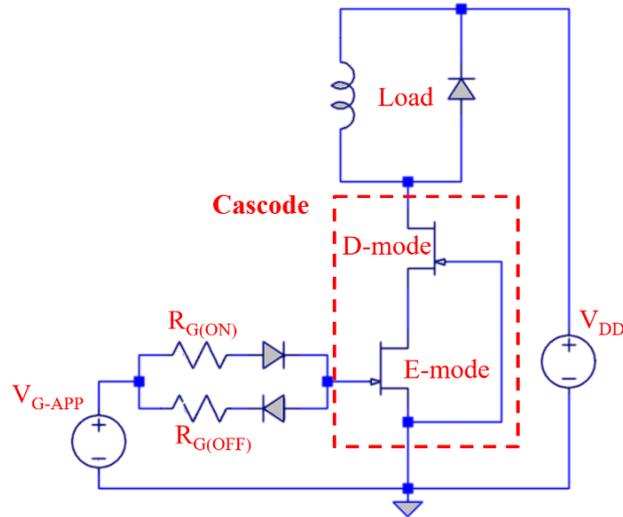


Figure 4-1 Circuit diagram of an inductive load switching setup for the all-GaN integrated cascode configuration.

4.2.1 Turn-on

Figure 4-2 shows the ideal waveforms of the gate-source voltage of the cascode (V_{GS}), drain-source voltage of the cascode (V_{DS-C}), drain current of the cascode (I_{DS-C}), D-mode channel current (I_{ch-D}) and drain-source voltage of the E-mode part (V_{DS-E}) for an all-GaN integrated cascode configuration during the turn-on transition. V_{DS-E} is highlighted and plays an important role in the cascode switching behaviour because it is effectively the gate-source voltage of the D-mode device. The ideal waveforms are generated using LTSPICE to illustrate the turn-on process of the cascode, and will be verified quantitatively in the later discussion (Section 4.3.1). The whole process is divided into 6 time intervals ($t_1 - t_6$ as highlighted in Figure 4-2) which will be discussed individually and defined according to the changes in charging and discharging current flow. The equivalent circuit of the capacitive current flow through intrinsic capacitance at each stage is shown in Figure 4-3 – Figure 4-8.

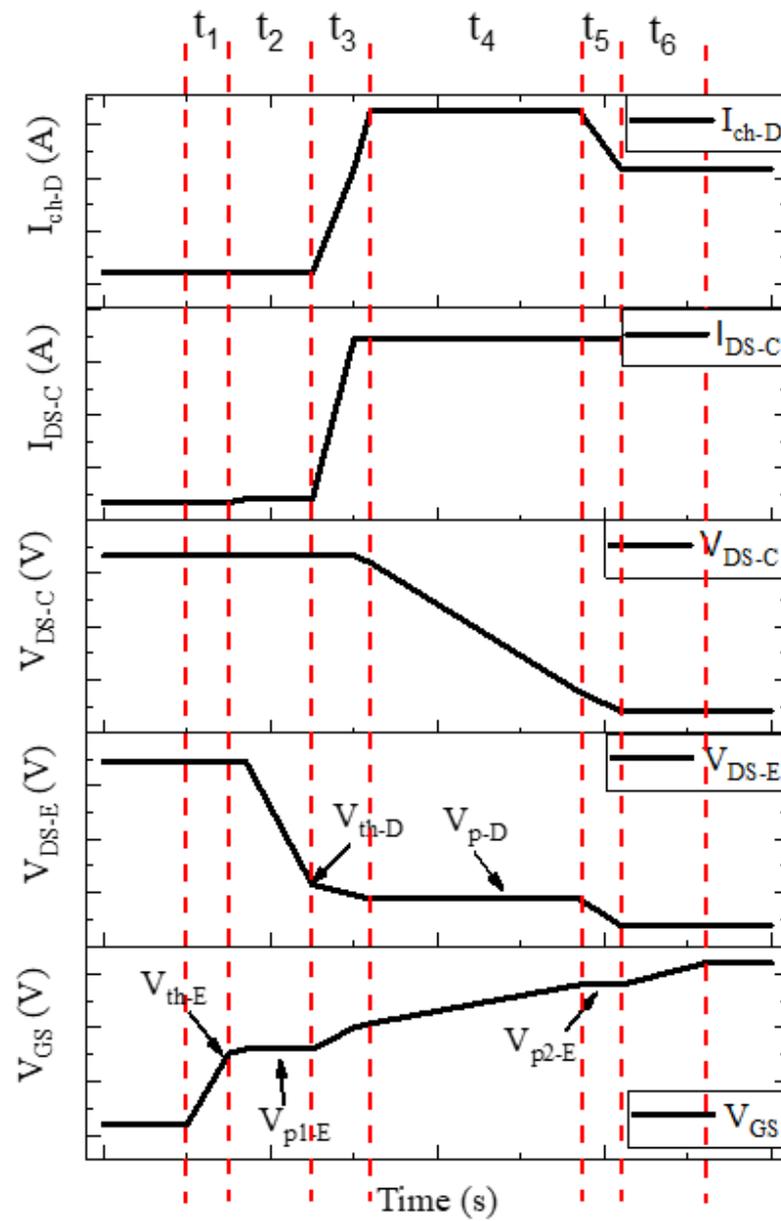


Figure 4-2 Ideal switching waveforms of I_{ch-D} , I_{DS-C} , V_{DS-C} , V_{DS-E} and V_{GS} of the all-GaN integrated cascode device during turn-on process.

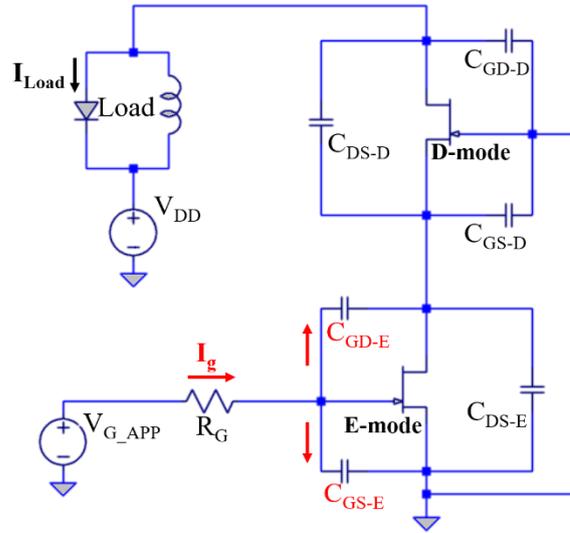


Figure 4-3 The equivalent circuit of the capacitive current flow through intrinsic capacitance during t_1 in turn-on process.

t_1 : An ideal step voltage is assumed and applied to the gate at the beginning of t_1 and the gate voltage (V_{GS}) starts to rise. Both the gate-source (C_{GS-E}) and gate-drain capacitances (C_{GD-E}) of the E-mode part are charged up, as shown in Figure 4-3. V_{GS} reaches the threshold voltage of the E-mode part (V_{th-E}) at the end of t_1 . The gate current is given by

$$I_g = \frac{V_{G_APP(ON)} - V_{GS}}{R_g} = C_{GS-E} * \frac{dV_{GS}}{dt} + C_{GD-E} * \frac{dV_{GS}}{dt} \quad (4-1)$$

where I_g is,

$$I_g = \frac{V_{G_APP(ON)} - V_{GS}}{R_g} \quad (4-2)$$

Therefore, we have

$$\frac{dV_{GS}}{V_{G_APP(ON)} - V_{GS}} = \frac{dt}{(C_{GS-E} + C_{GD-E}) * R_g} \quad (4-3)$$

This equals to

$$-\ln(V_{G_APP(ON)} - V_{GS}) = \frac{t}{(C_{GS-E} + C_{GD-E}) * R_g} + k \quad (4-4)$$

At $t = 0$, $V_{GS} = V_{G_APP(OFF)}$, therefore

$$k = -\ln(V_{G_APP(ON)} - V_{G_APP(OFF)}) \quad (4-5)$$

t can then be derived by,

$$t = [C_{GS-E} + C_{GD-E}] * R_g * \ln\left(\frac{V_{G_APP(ON)} - V_{G_APP(OFF)}}{V_{G_APP(ON)} - V_{GS}}\right) \quad (4-6)$$

(4-6) illustrates the time that V_{GS} takes to reach a certain voltage, and is given by,

$$t_1 = [C_{GS-E} + C_{GD-E(OFF)}] * R_g * \ln\left(\frac{V_{G_APP(ON)} - V_{G_APP(OFF)}}{V_{G_APP(ON)} - V_{th-E}}\right) \quad (4-7)$$

where C_{GD-E} is denoted as $C_{GD-E(OFF)}$ as V_{DS-E} is in its off-state during t_1 .

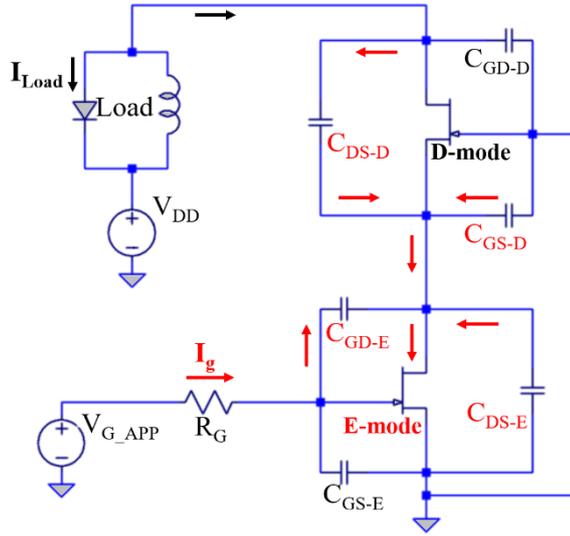


Figure 4-4 The equivalent circuit of the capacitive current flow through intrinsic capacitance during t_2 in turn-on process.

t_2 : During t_2 , V_{GS-E} continues to increase until it reaches its first plateau voltage V_{p1-E} . t_2 is the effective Miller plateau time for the cascode device during the turn-on process. The entire gate current goes into C_{GD-E} to discharge the capacitance during the plateau time. V_{DS-E} also drops because of the discharging of C_{GD-E} , C_{DS-E} , C_{GS-D} and C_{DS-D} . The discharging process is illustrated in Figure 4-4. t_2 finishes when V_{DS-E} reaches the threshold voltage of the D-mode part ($-V_{th-D}$) and the channel of the D-mode part begins to conduct. Note that the small transient time from $V_{GS-E} = V_{th-E}$ to $V_{GS-E} = V_{p1-E}$ is considered negligible for simplicity. The influence of the assumption will be discussed in detail in the later *verification* section.

Four individual current paths go together into the E-mode channel, so we have,

$$I_{ch-E}(t_3) = g_{m-E} * (V_{p1-E} - V_{th-E}) = I_{C_{GD-E}(t_2)} + I_{C_{DS-E}(t_2)} + I_{C_{GS-D}(t_2)} + I_{C_{DS-D}(t_2)} \quad (4-8)$$

where g_{m-E} is the transconductance of an equivalent E-mode device calculated in the linear region and $I_{GD-E}(t_3)$ is equal to the gate current, given by

$$I_{C_{GD-E}(t_3)} = \frac{V_{G-APP(ON)} - V_{p1-E}}{R_g} . \quad (4-9)$$

Because C_{GD-E} , C_{DS-E} , C_{GS-D} and C_{DS-D} must be discharged at the same rate,

$$I_{C_{DS-E}(t_3)} = \frac{C_{DS-E}}{C_{GD-E}} * \frac{V_{G-APP(ON)} - V_{p1-E}}{R_g} \quad (4-10)$$

$$I_{C_{GS-D}(t_3)} = \frac{C_{GS-D}}{C_{GD-E}} * \frac{V_{G-APP(ON)} - V_{p1-E}}{R_g} \quad (4-11)$$

$$I_{C_{DS-D}(t_3)} = \frac{C_{DS-D}}{C_{GD-E}} * \frac{V_{G-APP(ON)} - V_{p1-E}}{R_g} . \quad (4-12)$$

By substituting (4-9), (4-10), (4-11) and (4-12) into (4-8), we get

$$g_{m-E} * (V_{p1-E} - V_{th-E}) = \frac{V_{G-APP(ON)} - V_{p1-E}}{R_g} + \frac{C_{DS-E}}{C_{GD-E}} * \frac{V_{G-APP(ON)} - V_{p1-E}}{R_g} + \frac{C_{GS-D}}{C_{GD-E}} * \frac{V_{G-APP(ON)} - V_{p1-E}}{R_g} + \frac{C_{DS-D}}{C_{GD-E}} * \frac{V_{G-APP(ON)} - V_{p1-E}}{R_g} . \quad (4-13)$$

The plateau voltage V_{p1-E} can then be calculated using,

$$V_{p1-E} = \frac{(C_{GD-E(OFF)} + C_{DS-E(OFF)} + C_{GS-D(OFF)} + C_{DS-D(OFF)}) * V_{G-APP(ON)} + g_{m-E} * R_g * C_{GD-E(OFF)} * V_{th-E}}{(g_{m-E} * R_g + 1) * C_{GD-E(OFF)} + C_{DS-E(OFF)} + C_{GS-D(OFF)} + C_{DS-D(OFF)}} . \quad (4-14)$$

The current through the E-mode channel can then be derived as,

$$I_{ch-E}(t_2) = \frac{(C_{GD-E(OFF)} + C_{DS-E(OFF)} + C_{GS-D(OFF)} + C_{DS-D(OFF)}) * (V_{G-APP(ON)} - V_{th-E}) * g_{m-E}}{(g_{m-E} * R_g + 1) * C_{GD-E(OFF)} + C_{DS-E(OFF)} + C_{GS-D(OFF)} + C_{DS-D(OFF)}} . \quad (4-15)$$

t_2 can be estimated using,

$$t_2 = t_{C_{GD-E}(t_3)} = \frac{Q_{GD-E}(t_3)}{I_{C_{GD-E}(t_3)}} = \frac{\int_{-V_{th-D}}^{V_{DS-E(off)}} C_{GD-E} dV}{\frac{V_{G-APP(ON)} - V_{p1-E}}{R_g}} \quad (4-16)$$

By substituting (4-14) into (4-16), we get

$$t_2 = \frac{[(g_{m-E}R_g + 1)C_{GD-E(OFF)} + C_{DS-E(OFF)} + C_{GS-D(OFF)} + C_{DS-D(OFF)}][V_{DS(OFF)} + V_{th-D}]}{g_{m-E}[V_{G-APP(ON)} - V_{th-E}]} \quad (4-17)$$

where $V_{DS-E(OFF)}$ will be calculated in the turn-off section. Due to Miller-effect, the equation for t_2 suggests a greater influence from C_{GD-E} compared to other capacitances at the internode.

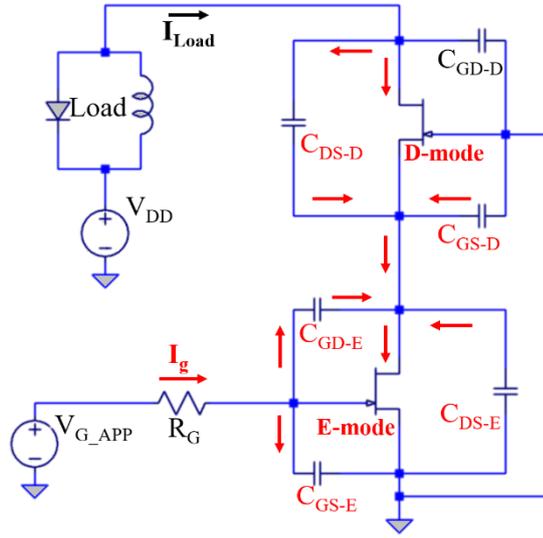


Figure 4-5 The equivalent circuit of the capacitive current flow through intrinsic capacitance during t_3 in turn-on process.

t_3 : t_3 is the current rise time of the cascode device during turn-on. The D-mode channel current ($I_{ch-D}(t_3)$) starts to increase as V_{DS-E} drops below $-V_{th-D}$. Since a current of $I_{ch-E}(t_2)$ determined by (4-15) already exists in the channel of the E-mode part, $I_{ch-D}(t_3)$ will try to ‘catch up’ with I_{ch-E} to maintain the same current level in both E-mode and D-mode parts before increasing together with I_{ch-E} . The charging (discharging) process is illustrated in Figure 4-5. t_3 finishes when both channel currents reach I_{load} . At the end of t_3 , V_{GS} and V_{DS-E} reach the values that ensure the E-mode and D-mode parts, respectively, can provide the load current. In practical high voltage switching applications, the drain voltage transient often dominates the total

switching time. Therefore, in this study, we ignore the influence of the current transient and assume t_3 is negligibly small.

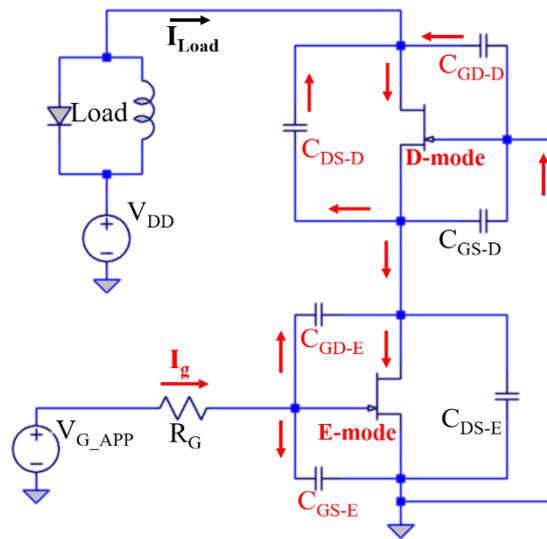


Figure 4-6 The equivalent circuit of the capacitive current flow through intrinsic capacitance during t_4 in turn-on process.

t_4 : As soon as the load current is built up in the channel, the freewheel diode is turned off. As a result, the drain voltage (V_{DS-C}) starts to drop. t_4 is the voltage fall time of the cascode as well as the plateau time of the D-mode device during the turn-on process. During t_4 , V_{DS-E} is clamped at its plateau voltage (V_{p-D}). The gate current only charges the input capacitance of the E-mode part (C_{GS-E} and C_{GD-E}) while the output capacitance of the cascode (C_{GD-D} and C_{DS-D}) discharge through the D-mode channel. Only the discharging current of C_{GD-D} goes into the E-mode device as shown in Figure 4-6. Therefore, V_{p-D} is determined by the product of E-mode on-resistance (R_{on-E}) and the current rating of the D-mode device, which effectively is also the maximum current of the cascode ($I_{max,c}$) based on the assumption of the same current drivability in both E/D mode devices. t_4 finishes when $(V_{DS-C} - V_{p-D})$ is just enough to provide the D-mode part with the maximum current. Note that the short capacitive transient time before V_{DS-E} reaches V_{p-D} during t_4 is ignored for simplicity.

V_{p-D} is given by,

$$V_{p-D} = I_{max,c} * R_{on-E} \cdot \quad (4-18)$$

And t_4 can be estimated by,

$$t_4 = \frac{Q_{oss}}{I_{max,c} - I_{load}} \cdot \quad (4-19)$$

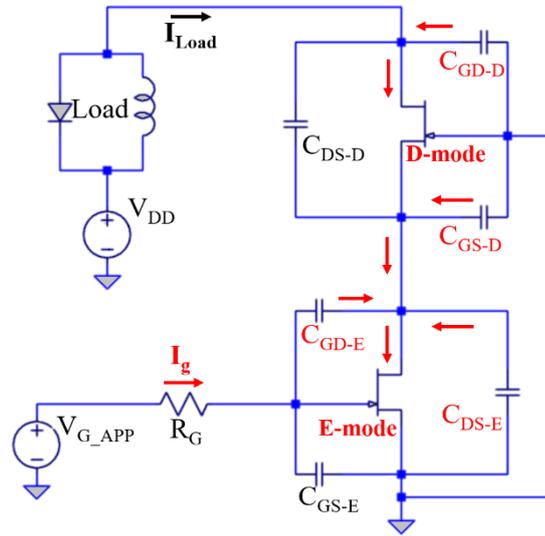


Figure 4-7 The equivalent circuit of the capacitive current flow through intrinsic capacitance during t_5 in turn-on process.

t_5 : t_5 is the second plateau time for the E-mode device during turn-on. The entire gate current goes into C_{GD-E} to discharge the capacitance, leading to the drop of V_{DS-E} . V_{DS-C} drops at the same rate to maintain the current constant in the D-mode channel. The equivalent discharging current flow is illustrated in Figure 4-7. t_5 finishes when V_{DS-E} reaches its on-state ($I_{load} * R_{on-E}$) and, at the same time, V_{DS-C} reaches ($I_{load} * R_{on-c}$). Note that t_5 is often not observable due to the small difference between V_{p-D} and $V_{DS-E(ON)}$. Therefore, t_5 is assumed to have little influence on the switching performance.

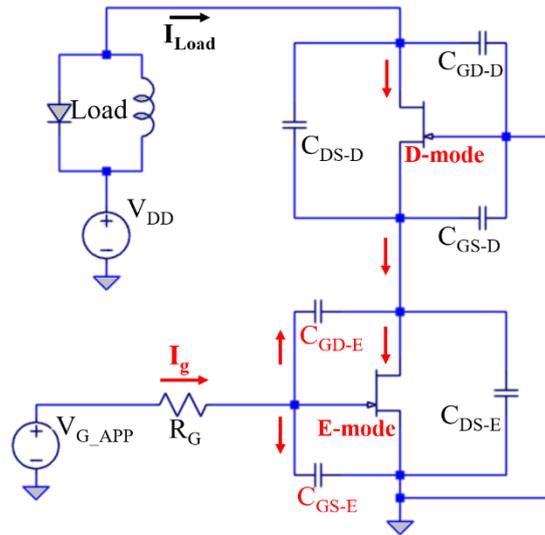


Figure 4-8 The equivalent circuit of the capacitive current flow through intrinsic capacitance during t_6 in turn-on process.

t_6 : t_6 starts as soon as both V_{DS-E} and V_{DS-C} reach their on-state value, and finishes when V_{GS-E} reaches $V_{G_APP(ON)}$. t_6 is a similar process as t_1 , but with both channel carrying the load current as illustrated in Figure 4-8. The switching time of t_6 is ignored since the main switching stage is finished and there is little switching energy loss during t_6 .

4.2.2 Turn-off

Figure 4-9 shows the ideal waveforms of V_{GS} , V_{DS-C} , I_{DS-C} and V_{DS-E} for an all-GaN integrated cascode configuration during turn-off transition. The ideal waveforms are generated using LTSPICE to illustrate the turn-off process of the cascode, and will be verified quantitatively in the later discussion (Section 4.3.1). The whole process is divided into 6 time intervals ($t_1 - t_6$ as highlighted in Figure 4-9) and will be discussed individually. The equivalent circuit of the capacitive current flow through intrinsic capacitance at each stage is shown in Figure 4-10 – Figure 4-14.

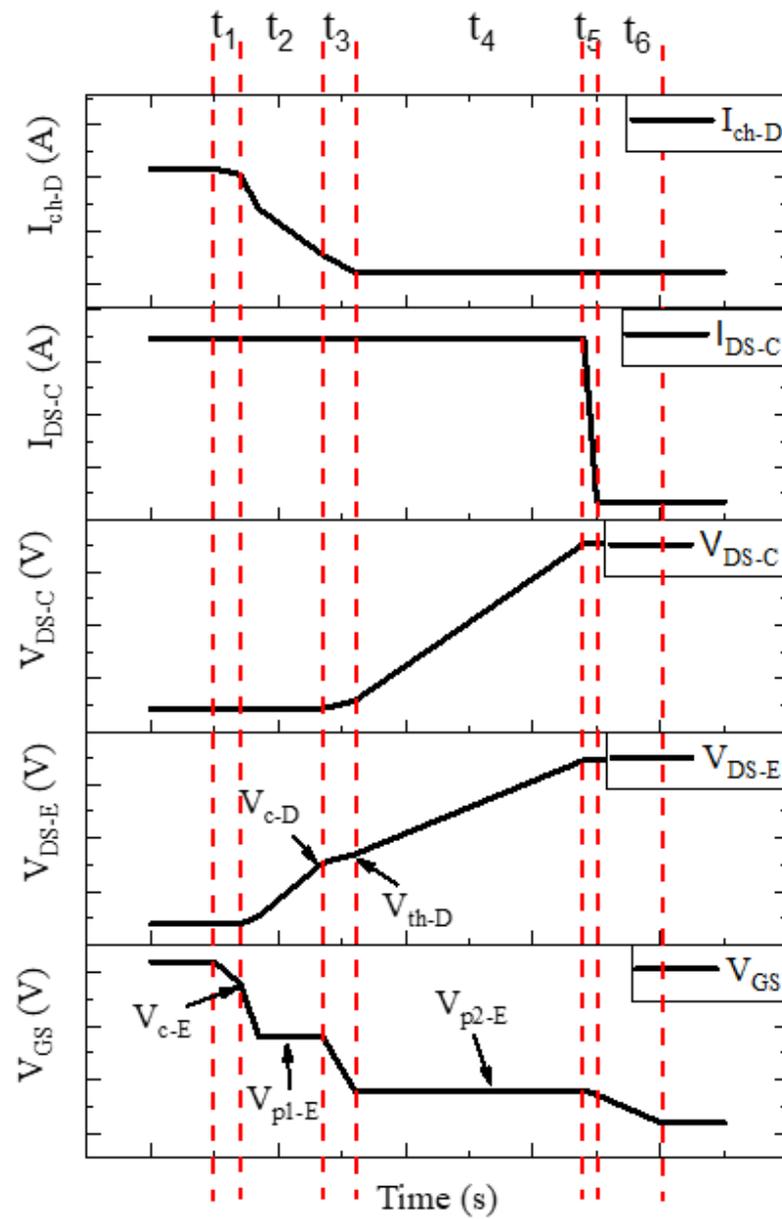


Figure 4-9 Ideal switching waveforms of I_{ch-D} , I_{DS-C} , V_{DS-C} , V_{DS-E} and V_{GS} of the all-GaN integrated cascode device during turn-off process.

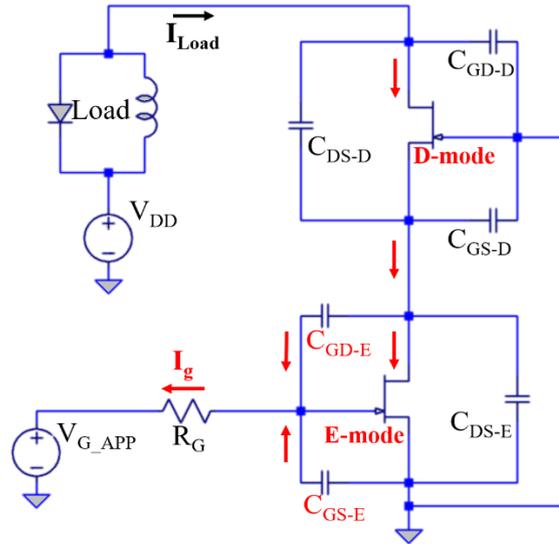


Figure 4-10 The equivalent circuit of the capacitive current flow through intrinsic capacitance during t_1 in turn-off process.

t_1 : An ideal step down voltage is assumed and applied to the gate at the beginning of t_1 . Both C_{GS-E} and C_{GD-E} are discharged from the gate node, as shown in Figure 4-10. The discharging current through C_{GD-E} comes from the channel current of the E-mode device (I_{ch-E}). As a result, V_{GS-E} starts to drop as does I_{ch-E} . t_1 finishes when V_{GS-E} reaches its critical voltage (V_{c-E}) that can provide the E-mode device with the appropriate channel current at the end of t_1 ($I_{ch-E}(t_1)$).

V_{c-E} is determined by the amount of reduced current in the E-mode channel at the end of t_1 . At $V_{GS-E} = V_{c-E}$,

$$I_{ch-E}(t_1) = g_{m-E} * (V_{c-E} - V_{th-E}) . \quad (4-20)$$

In addition,

$$I_{C_{GD-E}(t_1)} = I_{load} - I_{ch-E}(t_1) = \frac{V_{c-E} - V_{G-APP(OFF)}}{R_g} * \frac{C_{GD-E}}{C_{GS-E} + C_{GD-E}} . \quad (4-21)$$

Therefore, we have

$$V_{c-E} = \frac{(C_{GS-E} + C_{GD-E(ON)}) * R_g * [I_{load} + g_{m-E} * V_{th-E}] + C_{GD-E(ON)} * V_{G-APP(OFF)}}{C_{GD-E(ON)} + (C_{GS-E} + C_{GD-E(ON)}) * g_{m-E} * R_g} . \quad (4-22)$$

The time-dependent equation for t_1 can be derived using the same approach as t_1 in the turn-on process, and is given by

$$t = [C_{GS-E} + C_{GD-E}] * R_g * \ln \left(\frac{V_{G-APP(ON)} - V_{G-APP(OFF)}}{V_{GS-E} - V_{G-APP(OFF)}} \right) . \quad (4-23)$$

t_1 can be estimated by,

$$t_1 = [C_{GS-E} + C_{GD-E(ON)}] * R_g * \ln \left(\frac{V_{G-APP(ON)} - V_{G-APP(OFF)}}{V_{c-E} - V_{G-APP(OFF)}} \right) . \quad (4-24)$$

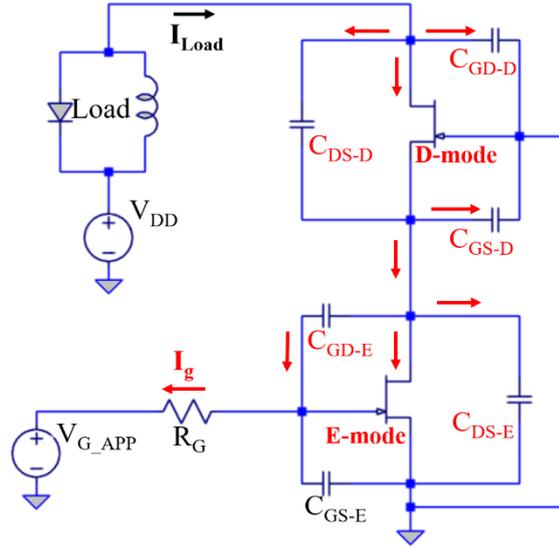


Figure 4-11 The equivalent circuit of the capacitive current flow through intrinsic capacitance during t_2 in turn-off process.

t_2 : As V_{GS-E} decreases below V_{c-E} , the E-mode device cannot support its channel current ($I_{ch-E(t_1)}$), and thus part of $I_{ch-E(t_1)}$ begins to charge up C_{GD-E} and C_{DS-E} from the drain side of the E-mode device. As a result, V_{DS-E} starts to increase during t_2 . V_{DS-C} also increases slightly as the difference between V_{DS-E} and V_{DS-C} is determined by the on-state resistance of the D-mode device (R_{on-D}) and the D-mode channel current (I_{ch-D}). As a result, I_{ch-D} reduces during t_2 as part of the current goes into C_{GD-D} and C_{DS-D} . The equivalent circuit of the current flow is shown in Figure 4-11. t_2 ends when V_{DS-E} reaches its critical voltage (V_{c-D}) that can just provide the D-

mode channel current ($I_{ch-D}(t_2)$). We assume V_{GS-E} is clamped at its first plateau voltage (V_{p1-E}) during t_2 despite the fact that there is a capacitive transient period before it reaches V_{p1-E} . This assumption will induce inaccuracy in the estimation of t_2 , and influence will be discussed in detail in the later *verification* section.

At $V_{GS-E} = V_{p1-E}$ there is no current discharging C_{GS-E} and C_{GD-E} from the gate node and the entire gate current is consumed by charging up C_{GD-E} from its drain side, so we have

$$I_g = I_{C_{GD-E}(t_2)} = \frac{V_{p1-E} - V_{G-APP(OFF)}}{R_g} . \quad (4-25)$$

The load current remains constant during t_2 , so

$$I_{load} = I_{C_{GD-D}(t_2)} + I_{C_{DS-D}(t_2)} + I_{ch-D}(t_2) \quad (4-26)$$

where $I_{ch-D}(t_2)$ and $I_{C_{DS-D}(t_2)}$ together provide the charging current for C_{GS-D} , C_{GD-E} and C_{DS-E} . If we assume the E-mode channel current $I_{ch-E}(t_2)$ is negligibly small, then

$$I_{C_{DS-D}(t_2)} + I_{ch-D}(t_2) = I_{C_{GS-D}(t_2)} + I_{C_{DS-E}(t_2)} + I_{C_{GD-E}(t_2)} . \quad (4-27)$$

By substituting (4-27) into (4-28), we get

$$I_{load} = I_{C_{GD-D}(t_2)} + I_{C_{GS-D}(t_2)} + I_{C_{DS-E}(t_2)} + I_{C_{GD-E}(t_2)} . \quad (4-28)$$

We know that C_{DS-D} , C_{GD-E} and C_{DS-E} must be charged at the same rate. In addition, C_{GD-D} is also charged at the same rate to maintain a constant voltage drop across the D-mode device as its channel current remains constant when V_{GS-E} is clamped at V_{p1-E} . So the following is valid,

$$\frac{I_{C_{GS-D}(t_2)}}{C_{GS-D}} = \frac{I_{C_{DS-E}(t_2)}}{C_{DS-E}} = \frac{I_{C_{GD-E}(t_2)}}{C_{GD-E}} = \frac{I_{C_{GD-D}(t_2)}}{C_{GD-D}} \quad (4-29)$$

Therefore,

$$I_{C_{GS-D}}(t_2) = \frac{C_{GS-D}}{C_{GD-E}} * I_{C_{GD-E}}(t_2) \quad (4-30)$$

$$I_{C_{DS-E}}(t_2) = \frac{C_{DS-E}}{C_{GD-E}} * I_{C_{GD-E}}(t_2) \quad (4-31)$$

$$I_{C_{GD-D}}(t_2) = \frac{C_{GD-D}}{C_{GD-E}} * I_{C_{GD-E}}(t_2) \quad (4-32)$$

By substituting (4-25), (4-30), (4-31) and (4-32) into (4-28), we get,

$$I_{load} = \frac{C_{GD-E} + C_{DS-E} + C_{GS-D} + C_{GD-D}}{C_{GD-E}} * \frac{V_{p1-E} - V_{G-APP(OFF)}}{R_g} . \quad (4-33)$$

V_{p1-E} can be calculated using,

$$V_{p1-E} = \frac{I_{load} * C_{GD-E(ON)} * R_g + (C_{GD-E(ON)} + C_{DS-E(ON)} + C_{GS-D(ON)} + C_{GD-D(ON)}) * V_{G-APP(OFF)}}{(C_{GD-E(ON)} + C_{DS-E(ON)} + C_{GS-D(ON)} + C_{GD-D(ON)})} . \quad (4-34)$$

At the end of t_2 , V_{DS-E} reaches V_{c-D} , which is given by

$$I_{ch-D}(t_2) = g_{m-D} * (-V_{c-D} - V_{th-D}) \quad (4-35)$$

where $I_{ch-D}(t_2)$ can be calculated by (4-26). Note that $I_{C_{DS-D}}(t_2)$ can be regarded as negligible since the voltage across C_{DS-D} during the plateau period is constant. Therefore, we have

$$g_{m-D} * (-V_{c-D} - V_{th-D}) = I_{load} - I_{C_{GD-D}}(t_2) \quad (4-36)$$

By combining (4-25), (4-32) and (4-36), we get

$$V_{c-D} = - \frac{(C_{GD-E(ON)} + C_{DS-E(ON)} + C_{GS-D(ON)}) * I_{load}}{(C_{GD-E(ON)} + C_{DS-E(ON)} + C_{GS-D(ON)} + C_{GD-D(ON)}) * g_{m-D}} - V_{th-D} . \quad (4-37)$$

Therefore, t_2 can be estimated by

$$t_2 = \frac{(V_{c-D} - I_{load} * R_{on-E}) * C_{GD-E}}{\frac{V_{p1-E} - V_{G-APP(OFF)}}{R_g}} . \quad (4-38)$$

By substituting (4-34) and (4-37) into (4-38), we get,

$$t_2 = \frac{-(C_{GD-E(ON)} + C_{DS-E(ON)} + C_{GS-D(ON)}) * I_{load}}{I_{load} * g_{m-D}} - \frac{(C_{GD-E(ON)} + C_{DS-E(ON)} + C_{GS-D(ON)} + C_{GD-D(ON)}) * g_{m-D} * (V_{th-D} + I_{load} * R_{on-E})}{I_{load} * g_{m-D}} \quad (4-39)$$

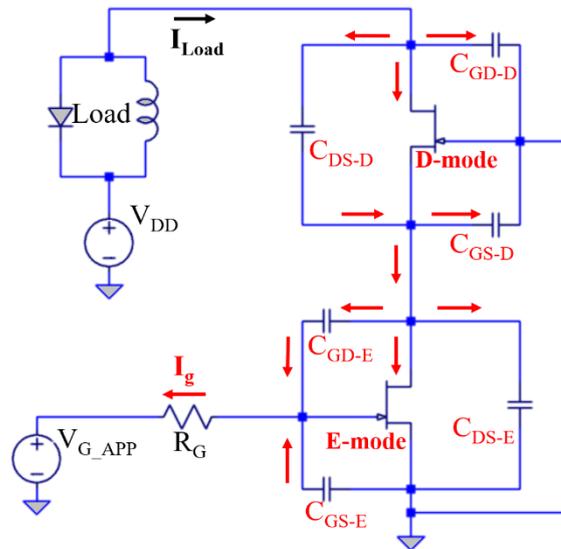


Figure 4-12 The equivalent circuit of the capacitive current flow through intrinsic capacitance during t_3 in turn-off process.

t_3 : t_3 is the time from $V_{DS-E} = V_{c-D}$ to $V_{DS-E} = -V_{th-D}$. At the beginning of t_3 , since the D-mode channel cannot provide its full channel current $I_{ch-D}(t_2)$, part of the channel current starts to flow into the output capacitance of the cascode device (C_{GD-D} and C_{DS-D}). In the meantime, V_{DS-E} , as the input voltage of the D-mode device, continues to increase to match with the reduced I_{ch-D} , as shown in Figure 4-12. t_3 ends when I_{ch-D} completely shifts to the output capacitance and becomes zero. Here, we assume the current transition time is negligibly small and has little influence on the overall switching performance.

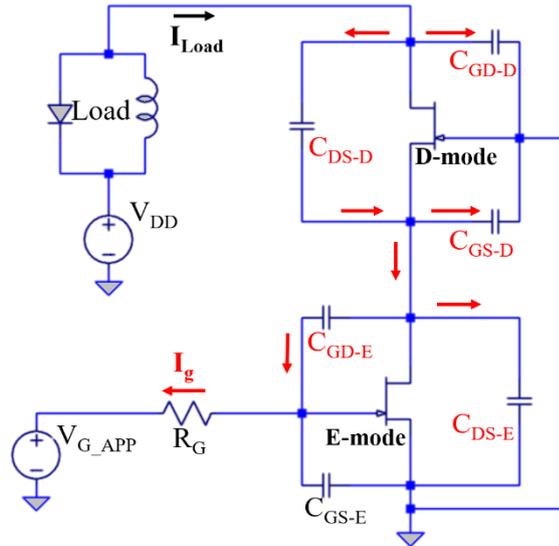


Figure 4-13 The equivalent circuit of the capacitive current flow through intrinsic capacitance during t_4 in turn-off process.

t_4 : t_4 is the voltage rise of the cascode during turn-off. During t_4 , the entire load current (I_{load}) charges the output capacitance of the cascode device and V_{DS-C} increases at its maximum rate. In addition, V_{DS-E} increases, assisted by the capacitance current of C_{DS-D} ($I_{C_{DS-D}(t_{3,2})}$) charging up C_{GS-D} , C_{DS-E} and C_{GD-E} from the internode of the cascode device. V_{GS-E} is assumed clamped at its second plateau voltage (V_{p2-E}). The equivalent circuit of the charging (discharging) process is shown in Figure 4-13. t_4 finishes when V_{DS-C} reaches its off-state voltage V_{DD} . At the same time, V_{DS-E} stops increasing and stays at $V_{DS-E(OFF)}$.

t_4 can be directly calculated using I_{load} since the full load current is used to charge up the output capacitance,

$$t_4 = \frac{Q_{OSS}}{I_{load}} \quad (4-40)$$

It is important to find out the value of $V_{DS-E(OFF)}$ as it determines the energy store at the internode of the cascode and is also needed to feedback to t_2 of the turn-on section. The expression for $V_{DS-E(OFF)}$ will depend on the status of the E-mode channel current (I_{ch-E}). Here, we consider the maximum value of $V_{DS-E(OFF)}$, i.e. when there is no I_{ch-E} during t_4 . More detailed discussions will be presented in the *Discussion* section. The assumption we made is,

$$V_{p2-E} < V_{th-E} . \quad (4-41)$$

Thus,

$$I_{ch-E}(t_4) = 0 . \quad (4-42)$$

We know that,

$$I_{C_{GD-D}}(t_4) + I_{C_{DS-D}}(t_4) = I_{load} \quad (4-43)$$

where $I_{C_{DS-D}}(t_4)$ is responsible for the voltage changes on both sides of C_{DS-D} and is given by,

$$I_{C_{DS-D}}(t_4) = C_{DS-D} * \frac{dV_{DS-C}}{dt} - C_{DS-D} * \frac{dV_{DS-E}}{dt} . \quad (4-44)$$

Therefore, (4-43) can be rewritten as,

$$I_{load} = C_{GD-D} * \frac{dV_{DS-C}}{dt} + C_{DS-D} * \frac{dV_{DS-C}}{dt} - C_{DS-D} * \frac{dV_{DS-E}}{dt} . \quad (4-45)$$

$I_{C_{DS-D}}(t_4)$ is also the current to charge up V_{DS-E} during t_4 , so we have

$$I_{C_{DS-D}}(t_4) = I_{C_{GS-D}}(t_4) + I_{C_{DS-E}}(t_4) + I_{C_{GD-E}}(t_4) . \quad (4-46)$$

As C_{GS-D} , C_{DS-E} and C_{GD-E} are charged at the same rate, we have

$$\frac{I_{C_{GS-D}}(t_4)}{C_{GS-D}} = \frac{I_{C_{DS-E}}(t_4)}{C_{DS-E}} = \frac{I_{C_{GD-E}}(t_4)}{C_{GD-E}} . \quad (4-47)$$

Because V_{GS-E} is clamped at V_{p2-E} , the entire gate current is consumed by C_{GD-E} .

Thus, we have

$$I_{C_{GD-E}}(t_4) = \frac{V_{p2-E} - V_{G-APP(OFF)}}{R_g} = C_{GD-E} * \frac{dV_{DS-E}}{dt} . \quad (4-48)$$

By substituting (4-47) and (4-48) into (4-46), we get

$$I_{C_{DS-D}}(t_4) = C_{DS-D} * \frac{dV_{DS-C}}{dt} - \frac{C_{DS-D}}{C_{GD-E}} * \frac{V_{p2-E} - V_{G-APP(OFF)}}{R_g} . \quad (4-49)$$

Rearranging (4-48) and (4-49), we get

$$\frac{dV_{DS-E}}{dt} = \frac{V_{p2-E} - V_{G-APP(OFF)}}{R_g * C_{GD-E}} \quad (4-50)$$

$$\frac{dV_{DS-C}}{dt} = \frac{I_{C_{GD-E}(t_{3,2})}}{C_{DS-D}} + \frac{V_{p2-E} - V_{G-APP(OFF)}}{R_g * C_{GD-E}} \quad (4-51)$$

Substituting (4-50) and (4-51) into (4-49), we get,

$$I_{C_{DS-D}(t_4)} = \frac{C_{DS-D} * C_{GD-E} * R_g * I_{load} - C_{DS-D} * C_{GD-D} * (V_{p2-E} - V_{G-APP(OFF)})}{C_{GD-E} * R_g * (C_{GD-D} + C_{DS-D})} \quad (4-52)$$

By combining (4-47) and (4-48), we also have,

$$I_{C_{GS-D}(t_4)} = \frac{C_{GS-D}}{C_{GD-E}} * \frac{V_{p2-E} - V_{G-APP(OFF)}}{R_g} \quad (4-53)$$

$$I_{C_{DS-E}(t_4)} = \frac{C_{DS-E}}{C_{GD-E}} * \frac{V_{p2-E} - V_{G-APP(OFF)}}{R_g} \quad (4-54)$$

By substituting (4-48), (4-52), (4-53) and (4-54) into (4-46), we get,

$$\frac{C_{DS-D} * C_{GD-E} * R_g * I_{load} - C_{DS-D} * C_{GD-D} * (V_{p2-E} - V_{G-APP(OFF)})}{C_{GD-E} * R_g * (C_{GD-D} + C_{DS-D})} = \frac{(C_{GD-E} + C_{DS-E} + C_{GS-D}) * (V_{p2-E} - V_{G-APP(OFF)})}{C_{GD-E} * R_g} \quad (4-55)$$

Therefore, V_{p2-E} can be estimated as

$$V_{p2-E} \approx \frac{C_{DS-D} * C_{GD-E} * R_g * I_{load}}{(C_{GD-E} + C_{DS-E} + C_{GS-D}) * (C_{GD-D} + C_{DS-D}) + C_{DS-D} * C_{GD-D}} + V_{G-APP(OFF)} \quad (4-56)$$

By substituting (4-56) into (4-48), we get,

$$I_{C_{GD-E}(t_4)} = \frac{C_{DS-D} * C_{GD-E} * I_{load}}{(C_{GD-E} + C_{DS-E} + C_{GS-D}) * (C_{GD-D} + C_{DS-D}) + C_{DS-D} * C_{GD-D}} \quad (4-57)$$

$V_{DS-E(OFF)}$ can be derived from,

$$(V_{DS-E(OFF)} + V_{th-D}) * C_{GD-E} = I_{C_{GD-E}(t_4)} * t_4 \quad (4-58)$$

and is given by

$$V_{DS-E(OFF)} = \frac{Q_{OSS} * C_{DS-D}}{(C_{GD-E} + C_{DS-E} + C_{GS-D}) * (C_{GD-D} + C_{DS-D}) + C_{DS-D} * C_{GD-D}} - V_{th-D} . \quad (4-59)$$

Note that the capacitances in (4-56) and (4-59) have dynamic values due to the change of V_{DS-C} during t_4 .

t_5 : t_5 is the load current fall time during turn-off. Due to the unique turn-off mechanism, at the end of t_4 , V_{DS-E} which effectively controls the channel of the D-mode device will be larger than $-V_{th-D}$. As a result, the D-mode channel is completely pinched off before entering t_5 . Therefore, t_5 can be regarded as negligible for the cascode device.

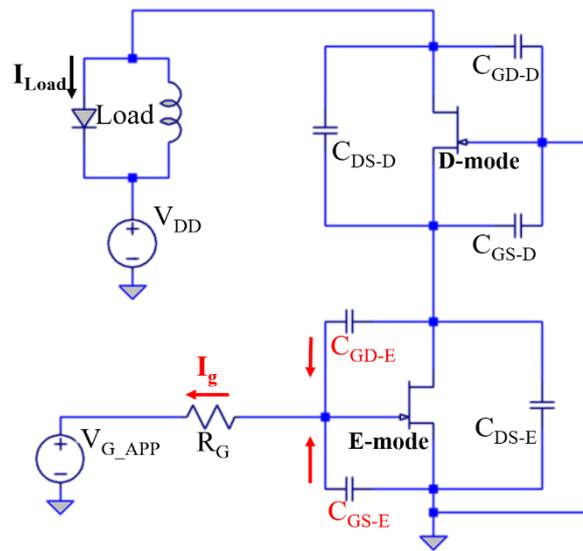


Figure 4-14 The equivalent circuit of the capacitive current flow through intrinsic capacitance during t_6 in turn-off process.

t_6 : t_6 is the last stage of the turn-off process where V_{GS-E} reaches its off-state bias ($V_{G_APP(OFF)}$) from V_{p2-E} . The full load current is conducting in the freewheel diode and the cascode device is completely switched off, as shown in Figure 4-14. The switching time of t_6 is ignored for simplicity.

4.3 Discussion

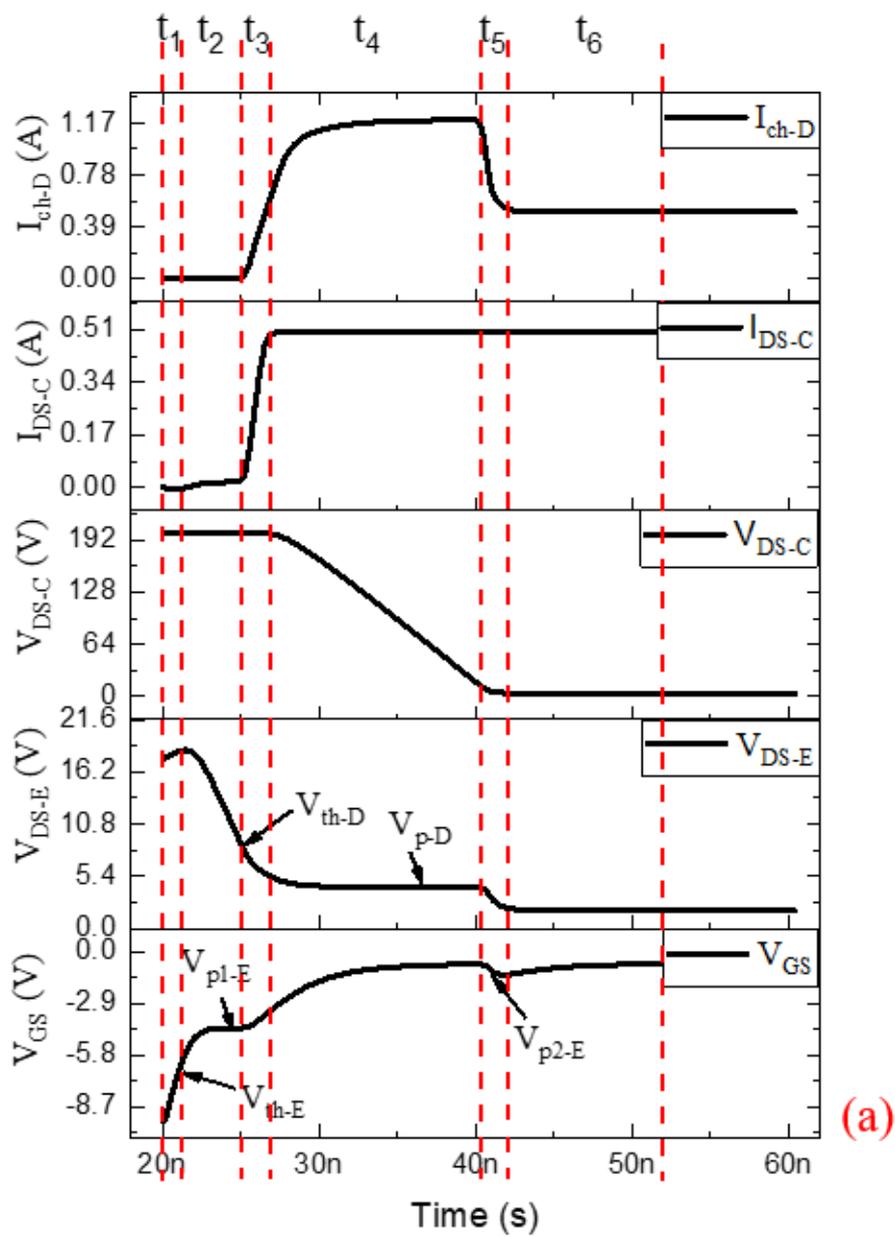
4.3.1 Verification

The derivations were verified with simulated results based on LTSPICE. Parameters used in the LTSPICE simulation are summarised in Table 4-1. A few assumptions have been made in choosing the parameters for the simulation in order to simplify

the comparison. The inductive load is assumed ideal with a current source carrying 0.5 A load current and an ideal freewheel diode with zero parallel capacitance. In addition, the non-linearity of all the intrinsic capacitance and the g_m are not considered. The capacitance values listed are the off-state values with device pinched-off at 200 V drain bias, while the g_m for both E-mode and D-mode parts are assumed at their peak values. Note that E-mode threshold voltage of -6 V is used with gate swing from -10 V to 0 V. This is to simulate the realistic E-mode device with threshold voltage of +2 V and gate swing from -4 V to +6 V.

Table 4-1 Parameters used in LTSPICE to produce simulated switching results for an integrated cascode configuration.

Parameters	Values (Cascode)
<i>Drain voltage (V_{DD})</i>	200 V
<i>Load current (I_{load})</i>	0.5 A
<i>Gate voltage (V_{G_APP})</i>	-10 V to 0 V
<i>Gate resistance (R_G)</i>	50 Ω
<i>E-mode threshold voltage (V_{th_E})</i>	-6 V
<i>E-mode on-resistance (R_{on_E})</i>	2.8 Ω
<i>E-mode trans-conductance (g_{m_E})</i>	0.12 S
<i>E-mode gate-drain capacitance (C_{GD_E})</i>	20 pf
<i>E-mode gate-source capacitance (C_{GS_E})</i>	30 pf
<i>E-mode drain-source capacitance (C_{DS_E})</i>	30 pf
<i>D-mode threshold voltage (V_{th_D})</i>	-8 V
<i>D-mode on-resistance (R_{on_D})</i>	3.2 Ω
<i>D-mode trans-conductance (g_{m_D})</i>	0.12 S
<i>D-mode gate-drain capacitance (C_{GD_D})</i>	40 pf
<i>D-mode gate-source capacitance (C_{GS_D})</i>	30 pf
<i>D-mode drain-source capacitance (C_{DS_D})</i>	5 pf
<i>Current rating of the cascode ($I_{max,c}$)</i>	1 A



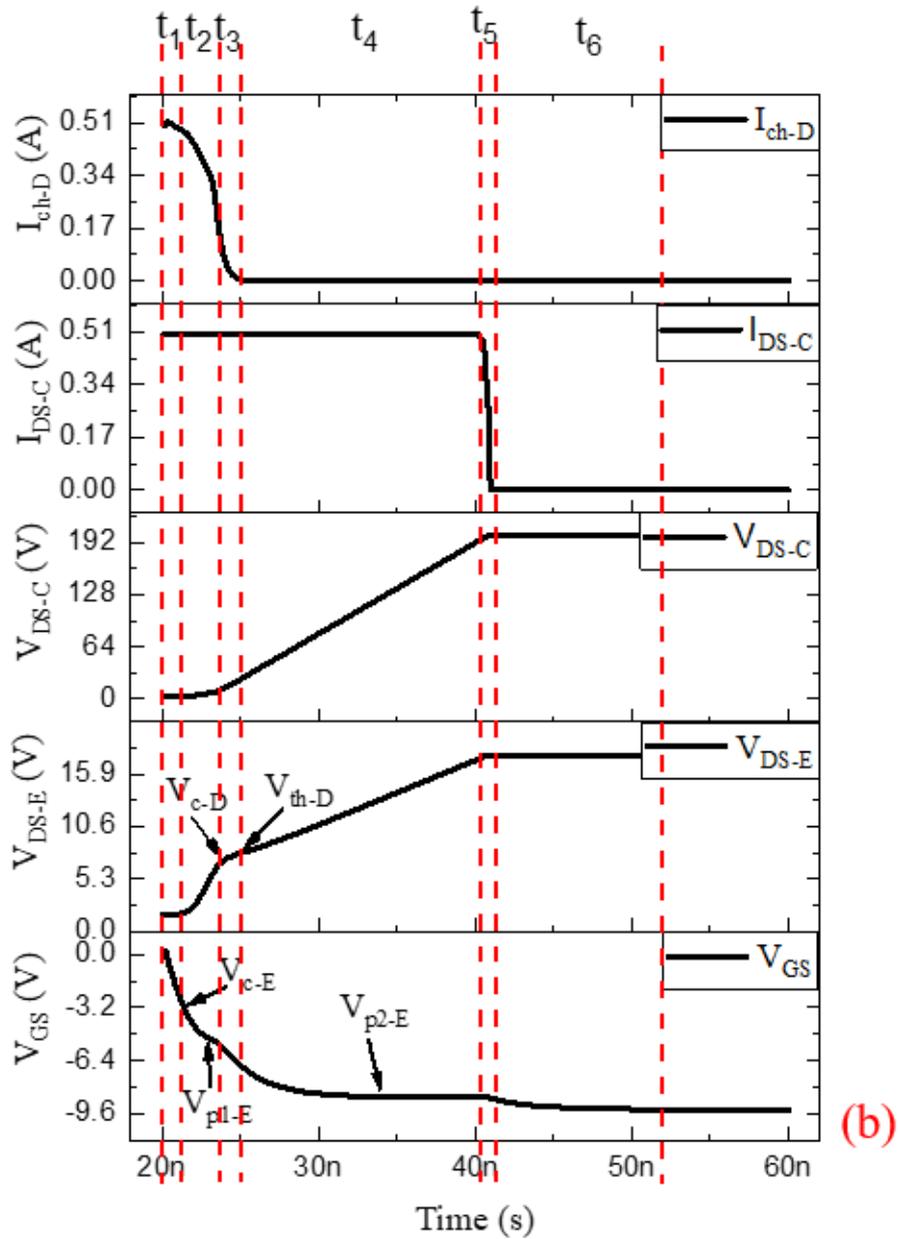


Figure 4-15 Simulated waveforms of I_{ch-D} , I_{DS-C} , V_{DS-C} , V_{DS-E} and V_{GS} during (a) turn-on and (b) turn-off.

Figure 4-15(a) and (b) shows the simulated waveforms for turn-on and turn-off, respectively. The switching stages discussed in previous sections for both turn-on and turn-off can be identified and are marked out in the simulated waveforms. The transient of V_{DS-C} dominates in both turn-on and turn-off, while the current transition is negligibly small. These show a good agreement of the theoretical analysis and simulation results. However, some of the plateau voltage cannot be observed clearly

in the simulated switching waveforms, for instance, the first plateau voltage of V_{GS} during t_2 in turn-off. This is caused by the relatively large capacitive transient time (due to large R_G) that dominates t_2 .

Table 4-2 Comparison between simulated and calculated results for turn-on process.

Parameters	Simulated results	Calculated results
t_1	1.24 ns	1.27ns
t_2	3.9 ns	3.65 ns
V_{p1-E}	-4.16 V	-3.2 V
$I_{ch-E(t_2)}$	0.286 A	0.276 A
t_4	15.7 ns	18 ns

Table 4-3 Comparison between simulated and calculated results for turn-off process.

Parameters	Simulated results	Calculated results
t_1	0.73 ns	0.46 ns
V_{C-E}	-1.63 V	-1.67 V
t_2	3.18 ns	0.784 ns
V_{C-D}	5.76 V	5.71 V
t_4	15.16 ns	18 ns
V_{p2-E}	-8.7 V	-9.3 V
$V_{DS-E(OFF)}$	17.6 V	19.84 V

Table 4-2 and Table 4-3 show the comparison of the simulated and calculated results during turn-on and turn-off process, respectively. Overall, the calculated results of each switching stages match with the simulated results, suggesting that the equations derived can give good estimations of the switching time as well as the important voltage values during both turn-on and turn-off for the integrated cascode device. The noticeable mismatch is the t_2 during turn-on. In our theoretical analysis, we assume zero capacitive transient time, and hence V_{GS} can reach V_{p-E1} instantly leading to a maximum charging current of C_{GD-E} throughout the time t_2 . As a result, the calculated value is much smaller compared to the simulated value since t_2 is limited by the capacitive transient in the simulation as discussed with Figure 4-6(b). Nevertheless, it has negligible influence on the overall switching speed.

4.3.2 Comparison of the switching speed

In this section, a mathematical comparison will be presented to explore the origin of the speed advantages for the cascode over the equivalent standalone E-mode device. The voltage transient time will be used for the comparison. The switching time extractions of the standalone device are modified from the equations developed for Si MOSFET by B. J. Baliga [7]. The voltage fall time ($t_{vf,e}$) and rise time ($t_{vr,e}$) of the standalone device are estimated as,

$$t_{vf,e} \approx \frac{Q_{OSS}*[C_{GD}+C_{DS}+C_{GD}*g_m*R_g]}{(C_{GD}+C_{DS})*[g_m*(V_{G-APP(ON)}-V_{th})-I_{load}]} \quad (4-60)$$

$$t_{vr,e} \approx \frac{Q_{OSS}*[C_{GD}+C_{DS}+C_{GD}*g_m*R_g]}{(C_{GD}+C_{DS})*[g_m*(V_{th}-V_{G-APP(OFF)})+I_{load}]} \quad (4-61)$$

(4-61) has a condition given by,

$$R_g > \frac{(C_{GD}+C_{DS})*(V_{th}-V_{G-APP(OFF)})}{C_{GD}*I_{load}} \quad (4-62)$$

The voltage fall time ($t_{vf,c}$) and rise time ($t_{vr,c}$) of the cascode device are given by (4-19) and (4-40), respectively.

$$t_{vf,c} \approx \frac{Q_{OSS}}{I_{max,c}-I_{load}} \quad (4-63)$$

$$t_{vr,c} \approx \frac{Q_{OSS}}{I_{load}} \quad (4-64)$$

Assuming both devices have the same output capacitance and current drivability, the speed advantage of the cascode during turn-on and turn-off will depend on the value of the gate resistance, which effectively is the quality of the gate driver. Both (4-60) and (4-61) reflect the Miller-effect in the standalone device, leading to the dependency of the charging (discharging) current with the gate loop. While the cascode device (with a reduced Miller-effect) is not limited by the gate loop during the drain voltage transient time. (4-62) is basically the condition for the device to show advantages when incorporated into a cascode configuration. (4-62) can be easily met when I_{load} is large (e.g. $I_{load} > 20$ A), which indicates the suitability of the cascode device for high power high frequency applications.

4.3.3 Comparison of the switching energy loss

It is important to understand that the advantage in the switching speed of the drain voltage (V_{DS-C}) does not necessarily lead to an advantage in switching energy loss. This is because the switching loss in the E-mode part cannot be revealed from the waveforms of V_{DS-C} and I_{DS-C} [1]. In this section, we compare the switching loss for both structures.

The total switching energy loss of the E-mode-only device ($P_{sw,e}$) can be estimated as,

$$P_{sw,e} \approx \frac{1}{2} * (C_{GD} + C_{DS}) * V_{DD}^2 * f_{sw} + \frac{1}{2} * I_{load} * V_{DD} * t_{vf,e} * f_{sw} + \frac{1}{2} * I_{ch} * V_{DD} * t_{vr,e} * f_{sw} \quad (4-65)$$

where f_{sw} is the switching frequency, $t_{vf,e}$ is given by (4-60) and $t_{vr,e}$ is given by (4-61). The first term represents the output capacitance energy losses, the second term is the channel switching loss due to the presence of the load current and voltage during turn-on and the last term is the energy losses dissipated through the device channel during turn-off, assuming (4-62) is valid.

The total switching energy loss of the cascode device ($P_{sw,c}$) can be derived as,

$$P_{sw,c} \approx \frac{1}{2} * (C_{GD-D} + C_{DS-D}) * V_{DD}^2 * f_{sw} + \frac{1}{2} * I_{load} * V_{DD} * t_{vf,c} * f_{sw} + \frac{1}{2} * (C_{GS-D} + C_{GD-E} + C_{DS-E}) * V_{DS-E(OFF)}^2 * f_{sw} \quad (4-66)$$

where $t_{vf,c}$ is given by (4-63) and $V_{DS-E(OFF)}$ is given by (4-59). The first term represents the output capacitance energy loss, the second term is the channel switching loss due to the presence of the load current and the voltage during turn-on and the last term is the capacitance energy loss at the internode ($P_{int,c}$).

Compared to the equivalent standalone device, the cascode configuration has the advantages of zero channel switching loss during turn-off due to the full utilisation of the load current to charge the output capacitance, and less turn-on switching loss when the voltage fall time is faster. However, it suffers from the additional

capacitance loss at the internode, as shown in the last term in (4-66). By replacing $V_{DS-E(OFF)}$ with (4-59), $P_{int,c}$ can be approximated to,

$$P_{int,c} \approx \frac{1}{2} * \frac{V_{DD}^2 * C_{DS-D}^2}{C_{GD-E} + C_{DS-E} + C_{GS-D}} * f_{sw} \quad (4-67)$$

(4-67) indicates the importance of controlling the ratio between C_{DS-D} and $(C_{GS-D} + C_{GD-E} + C_{DS-E})$ to suppress the additional energy loss. One can increase the $(C_{GS-D} + C_{GD-E} + C_{DS-E})$, but may cause a longer delay time during switching, which can affect the switching frequency. Alternatively, minimising C_{DS-D} can also reduce this internode energy loss, but we can only trade-off C_{DS-D} with C_{GD-D} by engineering the source field plate. The influence of the individual intrinsic capacitance will be discussed in a later section.

4.3.4 Suppression of $V_{DS-E(OFF)}$

$V_{DS-E(OFF)}$ is determined from the voltage rise time during turn-off, given by (4-59). It is an important parameter which has a significant influence on the reverse blocking state of the E-mode part and the switching performance of the cascode [4]. Firstly, $V_{DS-E(OFF)}$ determines the potential drop across the E-mode device during off-state. With a higher $V_{DS-E(OFF)}$, the requirement of the breakdown voltage for the E-mode device will be increased and can limit other parameters such as intrinsic capacitance and on-resistance in the E-mode device depending on the strategy to improve the device breakdown voltage. In addition, $V_{DS-E(OFF)}$ is a dominant parameter of the voltage delay time, t_2 , during turn-on shown in (4-17), which represents the (reduced) Miller-effect of the cascode device. A higher $V_{DS-E(OFF)}$ can negate the speed advantage of the cascode as the effective Miller capacitance C_{GD-E} will be subject to a higher voltage. Therefore, it is advantageous to suppress $V_{DS-E(OFF)}$ for a minimal Miller-effect and moderate breakdown voltage requirement. The suppression of $V_{DS-E(off)}$ can be mainly achieved by engineering of the capacitance ratio between C_{DS-D} and $(C_{GS-D} + C_{GD-E} + C_{DS-E})$ as discussed in the previous section.

4.3.5 Choice of V_{th-D}

The importance of engineering the V_{th-D} to improve the output current of the integrated cascode device has been demonstrated [1]. In this section, the influence of V_{th-D} on the switching performance will be discussed.

During turn-on, an excessively negative V_{th-D} can increase the time delay, t_5 , which leads to an increase in the turn-on energy loss through the cascode channel. During turn-off, a more negative V_{th-D} beyond the DC optimum value as defined in Chapter 3 will cause a larger V_{c-D} , according to (4-37). This effectively increases the turn-off delay time (t_2). In addition, V_{th-D} determines the minimum value of the $V_{DS-E(OFF)}$, as shown in (4-59), and thus affects the additional internode energy loss in the cascode.

In summary, achieving the DC optimum V_{th-D} is essential to increase the output current of the cascode, but it needs a careful control to avoid both an increase in the switching energy loss and limitation in the operating frequency.

4.3.6 Choice of capacitance

Intrinsic capacitances determine the switching speed of the cascode and the additional energy loss shown in (4-67). Therefore, it is crucial to identify the importance of each capacitor and understand the designing criteria for the optimum switching speed.

C_{GS-E} : C_{GS-E} , together with C_{GD-E} , forms the input capacitance of the E-mode part. It is determined by the distance between the gate and the channel and the FP geometries, and it mainly affects the change in V_{GS-E} .

C_{GD-E} : As one of the input capacitances of the E-mode device, C_{GD-E} also has an influence on the V_{GS-E} transition. More importantly, it is the effective Miller capacitance for the cascode device, as it gives a positive feedback from the load loop to the gate loop. The reduced Miller-effect in the cascode structure originated from the fact that C_{GD-E} is subject to $V_{DS-E(OFF)}$, which is much lower compared to the drain voltage of the cascode [2, 4]. However, C_{GD-E} still has a greater influence on the delay time t_2 during turn-on, compared to other capacitances shown in (4-17). Therefore, it is advantageous to trade-off C_{GD-E} with C_{DS-E} by implementing one or multiple SFPs on the E-mode device.

C_{DS-E} and C_{GS-D} : Together with C_{GD-E} , C_{DS-E} and C_{GS-D} are the effective input capacitance of the D-mode device. Geometrically, C_{DS-E} and C_{GS-D} have the same function, since the gate of the D-mode part is connected to the source of the cascode. Large value of $(C_{DS-E} + C_{GS-D})$ can lead to a reduced energy loss at the internode which is critical to the cascode device, according to (4-67). Therefore, it is

advantageous to trade-off both capacitance for a minimum C_{GD-E} , as discussed previously.

C_{GD-D} and C_{DS-D} : C_{GD-D} and C_{DS-D} are the output capacitance of the cascode device. The value of C_{GD-D} and C_{DS-D} depend on the field plate geometries of the D-mode part. They are subject to the high drain voltage, and thus have the most significant influence on the switching performance. They are equally important for drain voltage transient time during turn-on and turn-off. C_{DS-D} is the dominant parameter for the additional capacitance energy loss at the internode as shown in (4-67). Therefore, it is preferable to trade-off C_{GD-D} for a smaller C_{DS-D} . The ratio between C_{GD-D} and C_{DS-D} can be engineered by different D-mode SFP connections, as highlighted in Figure 4-16.

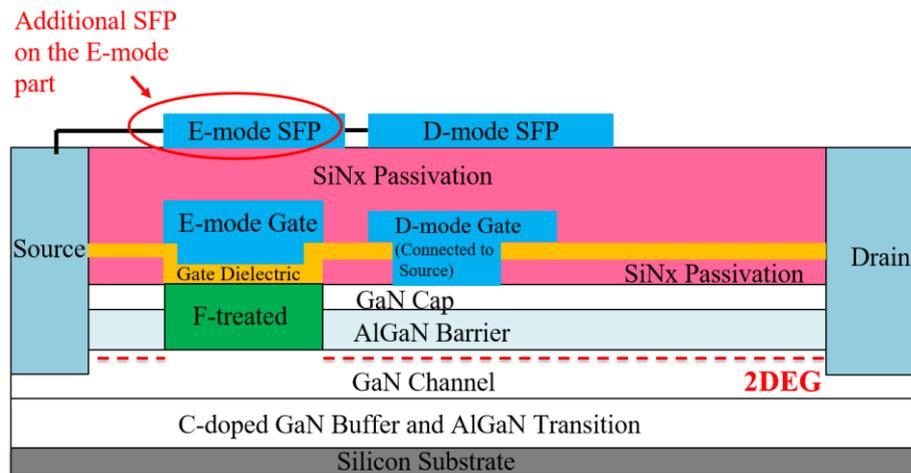


Figure 4-16 Device structure of integrated cascode with additional SFP on the E-mode part.

4.4 Conclusion

An analytical study on the switching behaviour of an all-GaN integrated cascode configuration has been presented. The turn-on and turn-off process were divided into several stages according to the change in the charging and discharging current flow. Time-dependent equations for each stage have been derived and verified with LTSPICE simulation results and the switching speed based on the drain voltage transient time has been compared mathematically with an equivalent GaN standalone

E-mode device. Analysis show that the speed advantages of the integrated cascode device originates from the reduced Miller-effect and the unique switching mechanisms, but will depend on the current capability of the gate driver. The derivation of the critical gate resistance is given, where the standalone device starts to suffer from the Miller effect and the cascode configuration becomes faster. A theoretical comparison of the switching energy loss between the cascode and standalone device has also been presented. The cascode device features less current voltage overlap loss due to reduced Miller effect, but needs careful control over the additional capacitance energy loss at the internode. The suppression of the additional energy loss can be achieved by reducing the ratio between the drain-source capacitance of the D-mode part and the sum of all capacitances at the internode. In addition, the D-mode V_{th} should not be over engineered beyond the optimum value to achieve the highest DC output current, otherwise additional capacitance energy loss occurs. Finally, the drain-source capacitance of the D-mode part and the gate-drain capacitance of the E-mode part are the two most important intrinsic capacitances to be minimised for the optimum switching performance.

4.5 References

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5 Field plate design in the all-GaN integrated cascode configuration

5.1 Introduction

An all-GaN integrated cascode configuration was demonstrated with a superior switching performance at 200 V compared to the equivalent standalone device and the switching behaviours are analysed in previous Chapters. However, further optimisations of the integrated cascode are still required to address several known issues from experience in the conventional GaN plus Si cascode device [1-4]. Firstly, due to the mismatch in intrinsic capacitances between the Si and GaN devices and the body diode in the Si MOSFET, the Si device can be driven into avalanche mode, causing additional switching energy loss [1]. Moreover, the mismatched capacitances together with the parasitic inductance may cause large oscillations during turn-off under high current operation [2]. In addition, the turn-off speed of the cascode configuration is reported to be uncontrollable via the gate resistance (R_g), which can cause an issue when control over the switching speed is required to suppress the ringing effect [3-4]. Adding an external capacitor between the drain and gate of the Si device was proposed in [1] and [2] to match the capacitance in the hybrid cascode device and prevent avalanche in the Si device. Likewise, an external capacitor between the gate and the drain of the cascode was used to solve the controllability issue [4]. However, the use of external components requires additional parasitic inductance and careful designs in the device packaging. On the other hand, the integrated cascode configuration can address both capacitance matching and switching controllability problems internally with different FP structures.

FPs are implemented for high voltage GaN HFETs to extend the breakdown voltage and suppress the dynamic R_{on} issues which can lead to an increased conduction loss of the device [5-6]. They also increase the intrinsic capacitances, and thus need careful design to maintain a good output figure of merit $R_{on} * Q_{oss}$ for the device [7]. In this Chapter, the field plate design in the all-GaN integrated cascode configuration is systematically studied. We first explore the influence of the FP extensions on suppressing the dynamic R_{on} effect of the device. After that, we briefly analyse the dynamic characteristic of the intrinsic capacitance in a GaN standalone E-mode

device with multiple FPs. Lastly, three different FP structures are proposed for the integrated cascode device, to address the issues of capacitance mismatch and the uncontrollability via R_g during turn-off transition.

5.2 Influence of field plate geometries on dynamic R_{on}

In this section, the mechanism of dynamic R_{on} in the GaN HFETs is briefly discussed. The dynamic R_{on} and ‘back-gating’ measurements were conducted to compare the device performance with the different FP geometries. D-mode standalone devices are used, as the results from standalone devices are transferrable to the integrated cascode configuration.

5.2.1 Origin of dynamic R_{on} in GaN HFETs

GaN HFETs features low on-state resistance compared to Si devices, due to the superior material properties and high carrier density in the 2DEG. However, the increase in R_{on} , known as dynamic R_{on} , during high voltage switching operations can negate this advantage and needs to be addressed with proper device designs.

The dynamic R_{on} , also known as current collapse, can be affected by the traps at the surface and in the buffer of GaN HFETs [8-9]. Figure 5-1 shows a schematic illustrating the surface induced current collapse [9-11]. In the off-state, during high voltage switching, electrons can be injected from the gate to the surface states, assisted by the peak electric field at the corner of the gate. The trapped negative charge forms a virtual gate that reduces the 2DEG and cannot be removed instantly after the device is turned on. As a result, the on-resistance of the device is increased until the charge is completely de-trapped.

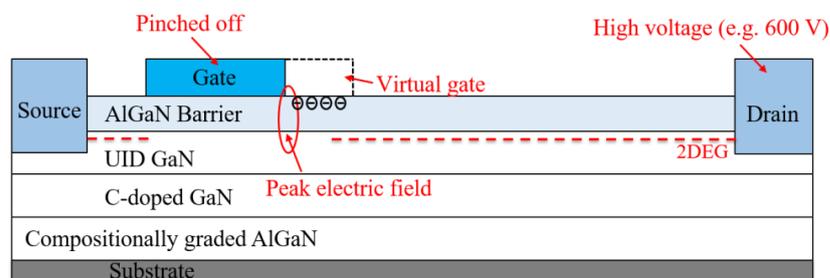


Figure 5-1 A schematic diagram illustrating the surface induced current collapse in GaN HFETs.

The buffer related current collapse is reported to be related to the excess traps in the buffer region and the paths to those traps [12-14]. Figure 1-1 shows an example of GaN HFET with C-doped buffer to illustrate the buffer trapping effect. Due to the presence of the leakage path between the drain and the C-doped region, a hole current can be injected into the C-doped layer during the off-state [14]. Due to the lack of a leakage path within the unintentionally doped (UID) GaN layer, a net negative charge accumulates and gets trapped in the geometric capacitance of the C-doped layer [14]. As a result, the 2DEG is reduced and the R_{on} increases when the device is switched on. Depending on the paths available for those negative charges to de-trap, the recovery process can be long compared to the on-state time of the switching cycle.

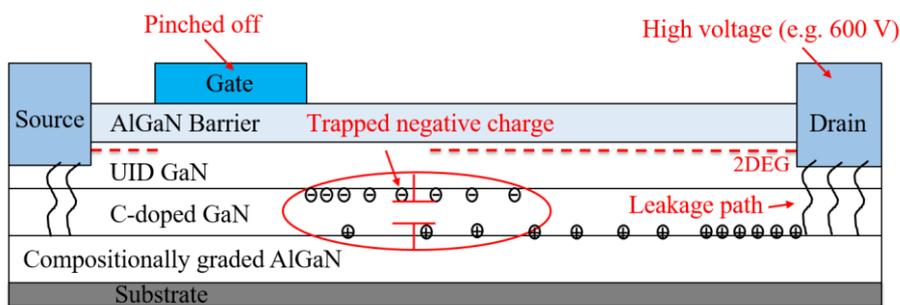


Figure 5-2 An illustration of the buffer related current collapse in GaN HFETs with a C-doped buffer structure.

5.2.2 Experimental

Two samples are fabricated, denoted as sample A and B. Sample A is based on a Fe-doped buffer structure (Figure 5-3(a)), while sample B is with a C-doped buffer layer (Figure 5-3(b)). The reason to have two different buffer structures is to distinguish the effect of surface related and buffer related current collapse, which will be discussed in a later section. The standard GaN HFET fabrication process, as described in Chapter 2, was used for both samples. In addition, we varied the GFP extension from 0 μm to 6 μm and the SFP extensions from 0 μm to 10 μm for the devices on both samples. The GFP extension is defined from the edge of the gate and SFP extension is defined from the edge of the GFP, as illustrated in Figure 5-4. There are slight differences in the DC characteristic of the devices fabricated in sample A and B, due to different layer structures. However, the influence of FP extensions on suppressing the dynamic R_{on} effect should not be affected.

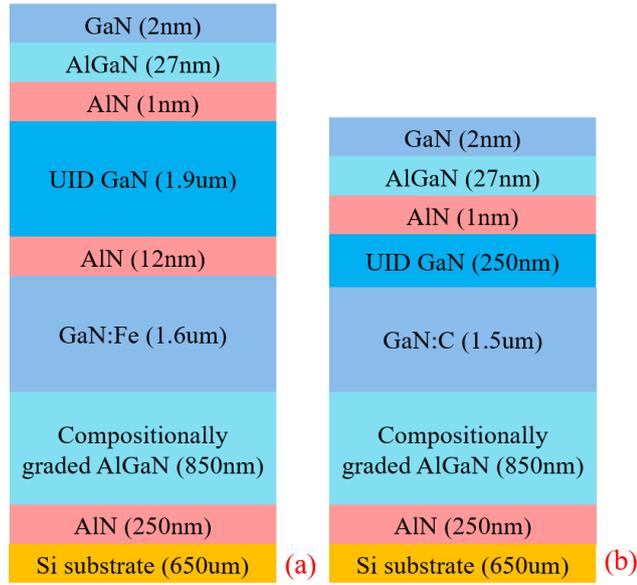


Figure 5-3 Buffer layer structure of (a) Fe-doped for sample A and (b) C-doped for sample B.

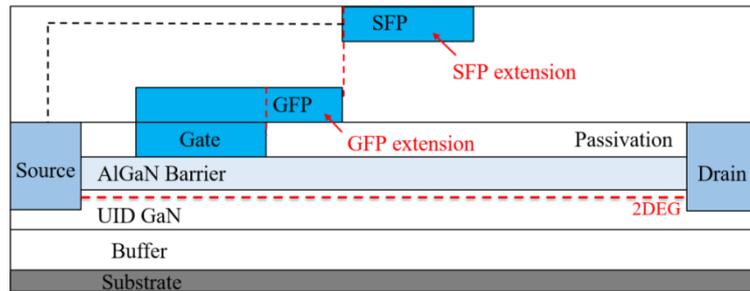


Figure 5-4 A schematic diagram showing the definition of the GFP and SFP extensions.

5.2.3 Results and discussion

Dynamic R_{on} measurements were carried out for both samples. Figure 5-5 shows the schematic of the measurement, while the setup details are described in Chapter 2. The device was pinched off initially at $V_{GS} = -7$ V. A constant stressing voltage (V_{DD}) starting from 50 V was applied to the drain of the device during its pinch-off state, as shown in Figure 5-5(a). After 500 ms stress, we removed the high voltage on the drain and applied 1 V before turning on the device with $V_{GS} = 0$ V (Figure 5-5(b)). The R_{on} of the device was measured 1 μ s after stress removal by monitoring the current through a current sensing resistor. The measurement was repeated with increased V_{DD} up to 500 V. The dynamic R_{on} was compared to the device DC on-resistance and plotted against the stress voltage.

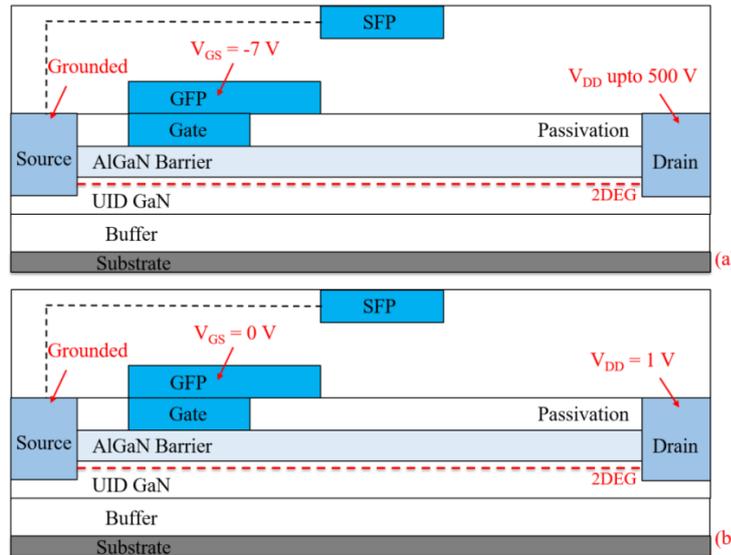


Figure 5-5 A schematic diagram showing the (a) off-state stressing stage and (b) on-state stage of the dynamic R_{on} measurement process.

Figure 5-6(a) shows the dynamic R_{on} results of the devices with different GFP extensions in sample A. All three devices are with no SFP. A clear trend of suppressing the dynamic R_{on} effect with the increased GFP extension is observed. With a 1 μm GFP extension, the dynamic R_{on} rises to 2.7 times higher compared to $R_{on}(DC)$ after stressing at 300 V, while the dynamic R_{on} is significantly reduced to 1.6 times with a longer GFP of 3 μm . Figure 5-6(b) shows the SFP extension dependency, where the GFP is fixed at 1 μm . A similar behaviour is observed for the SFP and 1.4 times increase in the R_{on} was achieved with an extremely large SFP extension of 10 μm . The results show that both GFP and SFP can effectively suppress the dynamic R_{on} effect in sample A. However, the suppression seems to be limited at around 1.4 times and it is unclear whether FPs have influence on surface related or buffer related current collapse.

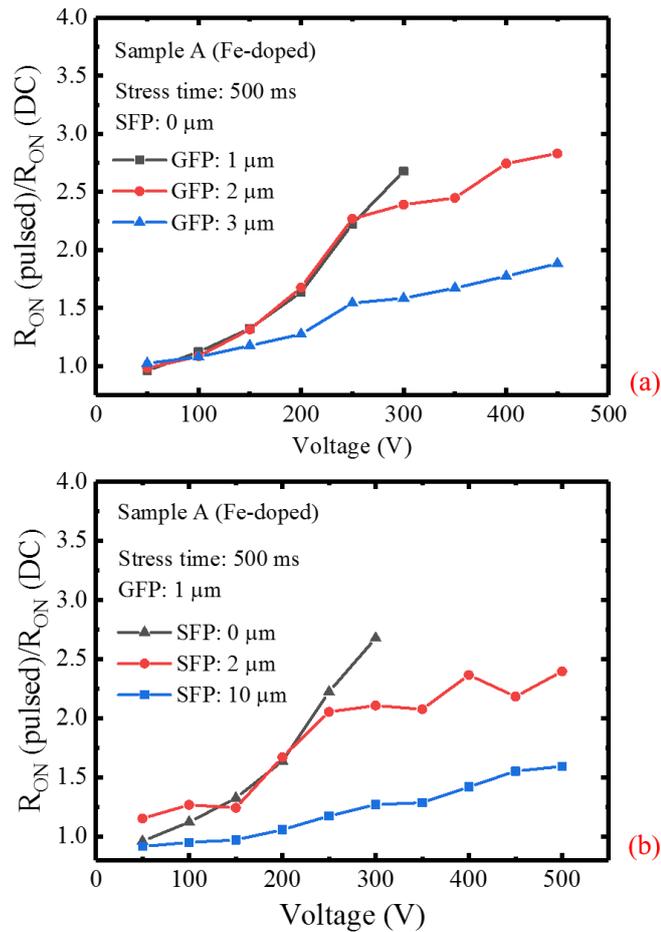


Figure 5-6 Dynamic $R_{on}/R_{on}(DC)$ results for sample A showing the dependence of (a) GFP extension and (b) SFP extension.

Figure 5-7(a) shows the dynamic R_{on} results for sample B with different GFP extensions. A different behaviour compared to sample A is observed. There is a limited influence on the suppression of the dynamic R_{on} with the increase of the GFP extension to 6 μm . Dynamic R_{on} appears around 2.6 times larger than $R_{on}(DC)$ for all three devices after stressing at 400 V. Similar results are measured for different SFP extensions, as shown in Figure 5-7(b). The suppression of the dynamic R_{on} seems to be limited to 2.6 times for sample B.

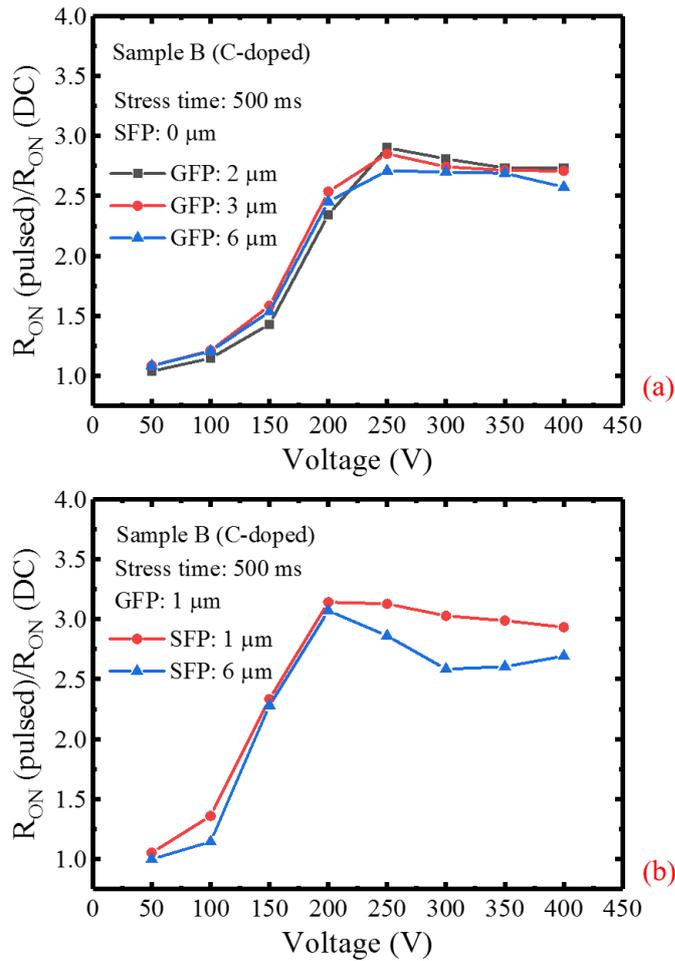


Figure 5-7 Dynamic $R_{on}/R_{on}(\text{DC})$ results for sample B showing the dependence of (a) GFP extension and (b) SFP extension.

To understand the reason for the different behaviour in sample A and sample B, a ‘back-gating’ measurement was conducted to extract the buffer component of the current collapse effect. Two ohmic pads with 10 μm gap spacing is used to monitor the ‘back-gating’ effect, as illustrated in Figure 5-8. The substrate was stressed with a negative bias to simulate the positive high voltage stress applied to the transistor, while the TLM structure was biased at 1 V. The 2DEG with 1 V potential screens the surface states and thus the electric field assisted surface trapping can be neglected in the ‘back-gating’ measurement. We varied the stress time and stress voltage at the substrate. The TLM current was measured 50 μs after removing the negative stress. We then converted the TLM current into the channel resistance and compared the results to the channel resistance at no stress. The results of stressed channel resistance/DC are plotted against the stress time.

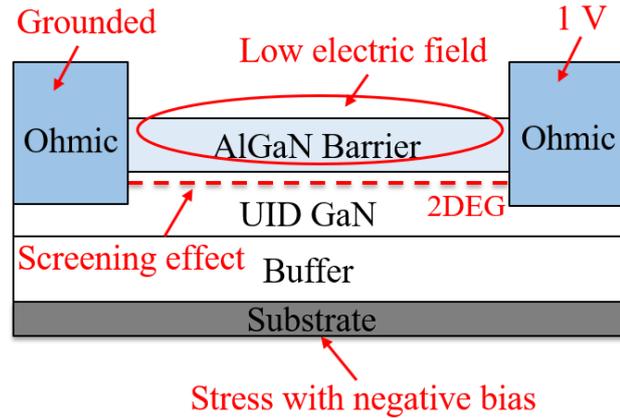


Figure 5-8 A schematic diagram showing the ‘back-gating’ measurement.

Figure 5-9(a) and (b) shows the ‘back-gating’ measurement results of sample A and sample B, respectively. The buffer related current collapse effect is less in sample A compared to sample B. This is probably because sample A has a leakier buffer (Figure 5-10) that increases the number of paths available to the traps and reduces the charge transport time, as discussed by [14]. More importantly, both results show that the increase in the channel resistance saturates with stress time, which is around 1.4 times for sample A and 2.6 times for sample B. The reason is not fully understood yet, but could be due to the full occupation of the traps in the buffer. These figures represent the maximum contribution from the buffer to the dynamic R_{on} effect and tie up with the limits of suppressing the dynamic R_{on} using FPs for both samples, as shown in Figure 5-6 and Figure 5-7.

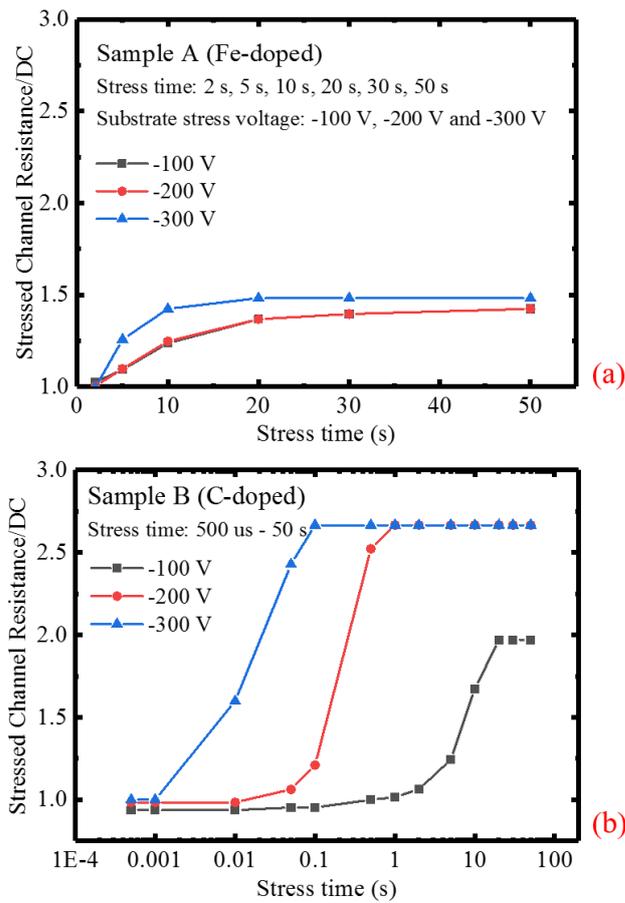


Figure 5-9 Results of 'back-gating' measurement for (a) sample A and (b) sample B, with different substrate stress voltage and stress time.

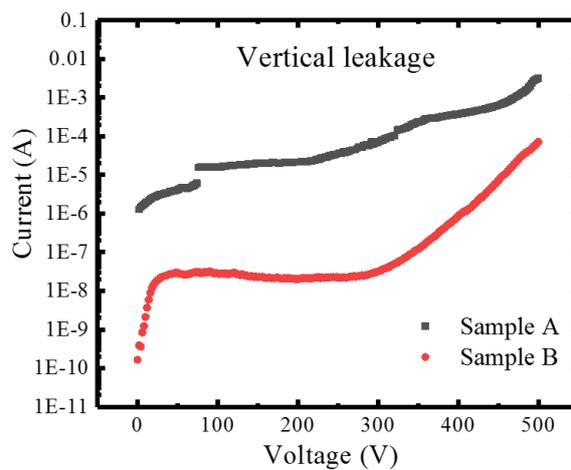


Figure 5-10 Results of vertical leakage measurement for sample A and sample B.

These results suggest that the FPs can effectively reduce the surface induced current collapse due to the modulation of the electric field near the surface. However, they have limited influence on the buffer related current collapse. One should be cautious when designing the FP extensions as over-design can result in the increase of the intrinsic capacitances leading to slower switching speed [6], with little improvements on the dynamic R_{on} caused by the buffer. The optimum design of the GFP and SFP geometries needs to take consideration of the breakdown voltage, the intrinsic capacitances and the surface induced dynamic R_{on} effect.

5.3 Intrinsic capacitance of the GaN HFETs with FPs

Intrinsic capacitances of the GaN HFETs are correlated with the entire vertical configuration of the device including the AlGaN barrier, the surface states, the passivation and the geometries of the FPs [15-16]. FPs modulate the depletion region, and therefore changes the dynamic characteristics of the output capacitance and the switching performance of the device [15-16]. In this section, we highlight the role of FPs and briefly analyse their influence on the intrinsic capacitances.

High voltage CV measurements were carried out on a 2 mm gate width standalone GaN E-mode. The device was fabricated using our standard GaN HFET fabrication process with $L_{GFP} = 1 \mu\text{m}$ and $L_{SFP} = 2 \mu\text{m}$. The reverse capacitance (C_{rss}) and output capacitance (C_{oss}) were extracted versus V_{DS} , with V_{GS} held below the threshold voltage. The input capacitance (C_{iss}) was measured at $V_{DS} = 0 \text{ V}$ since C_{GS} has little dependence on the drain voltage. The setup details for measuring C_{oss} and C_{rss} are described in Chapter 2.

C_{oss} and C_{rss} were measured at $V_{DS} = 200 \text{ V}$ and gave values of 4 pF and 3.5 pF respectively, as shown in Figure 5-11. The pinch-off voltage of the GFP and SFP were around 25 V and 100 V, respectively. The measured capacitances are higher compared to the results reported in the literature [6]. The large intrinsic capacitance observed in our device is due to the combination of the non-optimised FP structures and parasitic capacitance in the setup. However, the dynamic behaviour of the capacitance with increased drain voltage should not be affected.

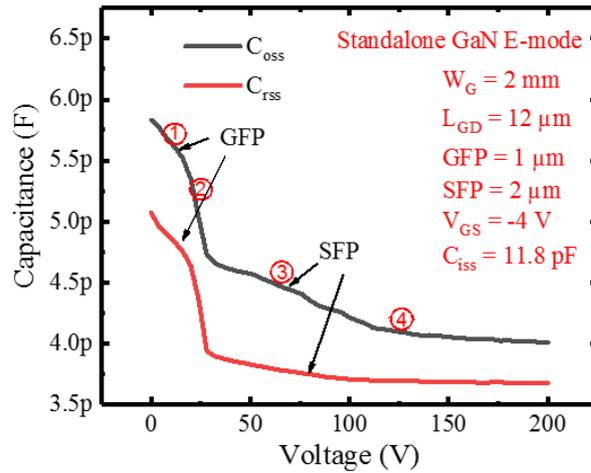


Figure 5-11 Results of C_{iss} , C_{oss} and C_{rss} for a 2 mm GaN standalone E-mode device up to 200 V.

The dispersion of the capacitance characteristics (C_{oss} and C_{rss}) is divided into four stages, based on the change of the depletion region with the increased drain voltage. At stage 1 ($V_{DS} < 25$ V), as shown in Figure 5-12(a), the region underneath the GFP starts depleting and the vertical depletion towards the substrate dominates [16]. As a result, the 2DEG in the GFP region is reduced, but is not completely depleted as the drain voltage is smaller than the pinch-off voltage of the GFP. C_{GD} can be estimated as the total capacitance between the GFP and the 2DEG underneath. It remains relatively constant as shown in the measurement results, the slight reduction results from the lateral depletion process towards the drain of the device that reduces the 2DEG length under the GFP, and thus the effective area of C_{GD} . C_{DS} at stage 1 remains unchanged, and is determined by the total capacitance between the SFP and the 2DEG. Note that C_{DS} underneath the gate region is considered negligible due to the large gate length (1.5 μm) compared to the height of the SFP (300 nm).

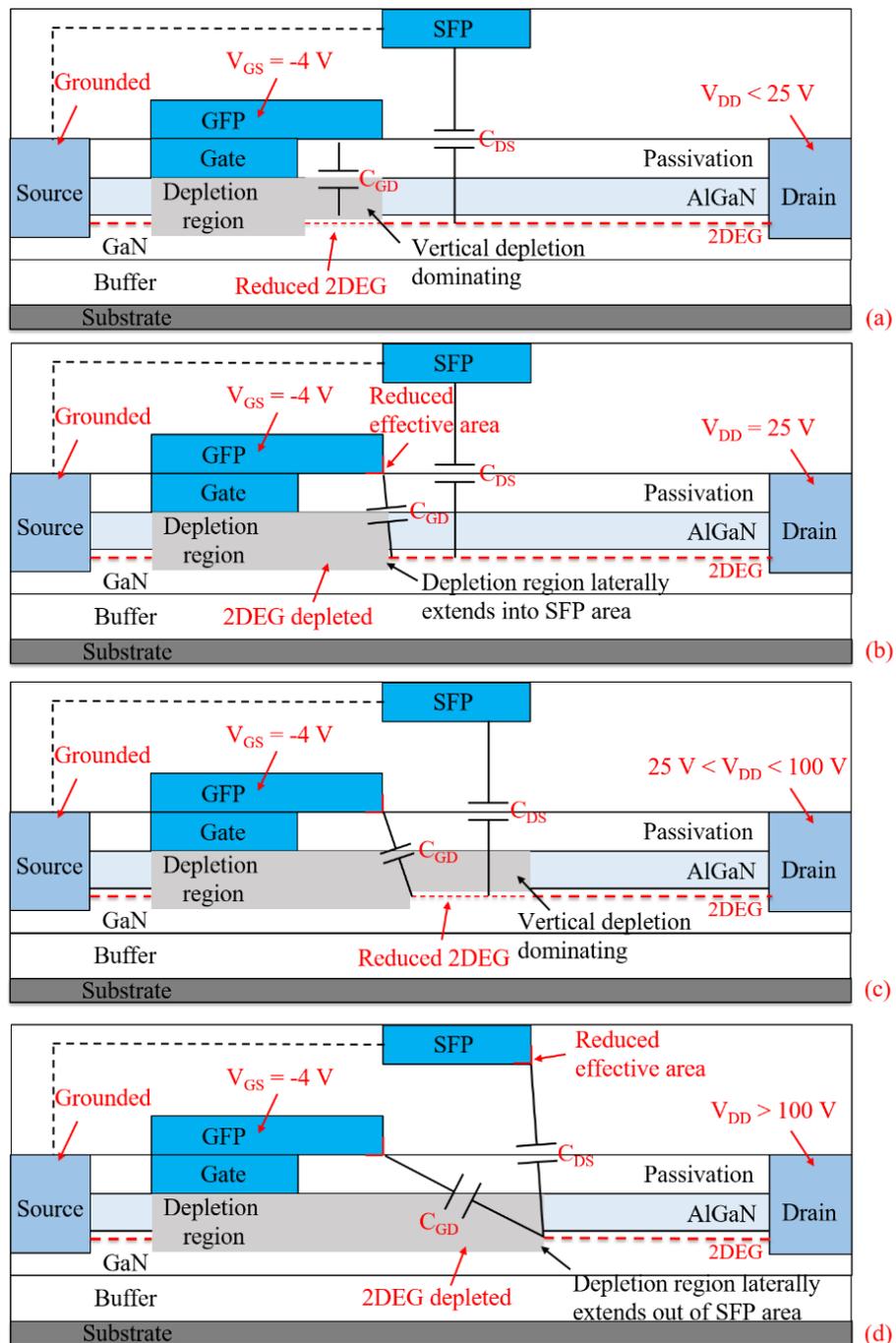


Figure 5-12 A schematic diagram showing the extension of the depletion region leading to the change in the output capacitance (C_{GD} and C_{DS}) during (a) $V_{DS} < 25$ V, (b) $V_{DS} = 25$ V, (c) $25 < V_{DS} < 100$ V and (d) $V_{DS} > 100$ V.

At stage 2 ($V_{DS} = 25$ V), the drain voltage is equal to the pinch-off voltage of the GFP, leading to a complete depletion underneath, as shown in Figure 5-12(b). C_{GD} drops significantly as the 2DEG moves out of the edge of the GFP and the effective area of C_{GD} reduces [17], while C_{DS} remains constant. During stage 3 (25 V $< V_{DS} <$

100 V), the region underneath the SFP starts to deplete, as shown in Figure 5-12(c). Likewise, the vertical depletion dominates and leads to the reduction of the 2DEG in the SFP region. Meanwhile, the lateral depletion process pushes the 2DEG further away towards the drain of the device. As a result, both C_{GD} and C_{DS} decrease slightly and the slope of capacitance (C_{rss} and C_{oss}) reflects reduced 2DEG length under the SFP. At stage 4 ($V_{DS} > 100$ V), as the drain voltage increases beyond the pinch off voltage of the SFP, the 2DEG underneath the SFP is completely depleted, as shown in Figure 5-12(d). As a result, C_{GD} further reduces because of the increased distance between the GFP and the 2DEG. Similarly, C_{DS} decreases due to the reduction in the effective capacitance area.

Increasing the GFP extension may improve the suppression of the dynamic R_{on} , as observed in the previous section, however, C_{GD} , which is the Miller capacitance for the standalone device, also increases proportionally before the GFP is pinched off (stage 1). On the other hand, increasing the SFP extension can reduce the Miller capacitance after the SFP is pinched-off (stage 4), because the 2DEG is depleted further away from the GFP. The penalty to pay is an increased C_{DS} . Therefore, in the standalone device, multiple FPs are preferred to trade-off C_{DS} for smaller C_{GD} , and to suppress the dynamic R_{on} at the same time [18]. While in the integrated cascode device, the design criteria of the FPs is different and is discussed in the later sections.

5.4 Influence of FP connections on the all-GaN integrated cascode configuration

The FP of the D-mode part in the integrated cascode configuration has the flexibility to connect to different locations without the worry of the Miller-effect, as the effective Miller capacitance is shifted to the gate-drain capacitance of the E-mode part (C_{GD-E}). In addition, different connections redistribute the FP induced capacitance in the integrated cascode device and can have significant influences on its switching performance, as suggested in the theoretical analysis in chapter 4. There have been few studies or discussion on the FP connections in the GaN plus Si cascode device. Therefore, in this section, we propose three different FP connections and compare their influence on the switching performance of the device. Several known issues reported for conventional GaN plus Si cascode can be addressed,

including the capacitance matching between the D-mode and E-mode parts and the controllability of turn-off speed via gate resistance.

5.4.1 Design and fabrication

Figure 5-13 depicts the structure of the integrated cascode configuration with three different FP connections (to the source of the cascode, to the internode pad or to the gate of the E-mode part), which are highlighted as Op 1, 2 and 3, respectively. The additional capacitance induced by the FP with different locations is denoted as C_{FP} in the equivalent circuit shown in Figure 5-14. The FP in Op 1 and 2 redistributes the output capacitance of the cascode device by having the C_{FP} either in parallel with C_{GD-D} or C_{DS-D} . In Op 3, with the FP connected to the gate of the E-mode part, C_{FP} acts as a feedback capacitor from the drain to the gate of the cascode device and induces additional Miller-effect.

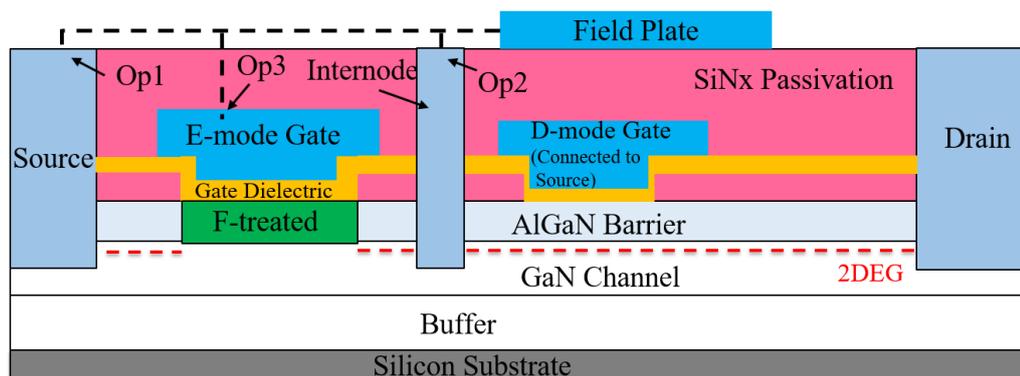


Figure 5-13 A schematic diagram of an all-GaN integrated cascode device with three different field plate connections.

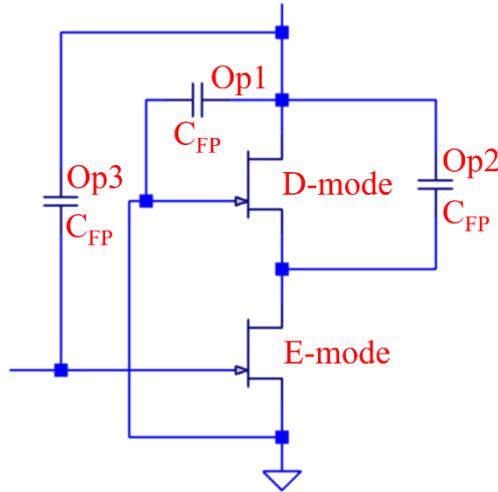


Figure 5-14 An equivalent circuit of the capacitance induced by three source field plate designs (C_{FP}).

Multi-finger cascode devices were fabricated accordingly, based on the fabrication process described in Chapter 2.

Figure 5-15 shows an optical image of the fabricated large area device. Devices were with $L_{GD} = 12 \mu\text{m}$, $L_{GFP} = 1 \mu\text{m}$ and $L_{SFP} = 2 \mu\text{m}$ and were kept the same for all three options. An additional bond pad to access the internode of the cascode was added to the multi-finger cascode, enabling the potential at the internode to be monitored during the switching measurement. Cascode devices with $W_G = 8 \text{ mm}$ showed negligible difference in the DC characteristics between the three options, as shown in Figure 5-16. The negative threshold is due to the non-optimisation of the F-treatment. A standalone D-mode device was also fabricated with V_{th} around -6 V .

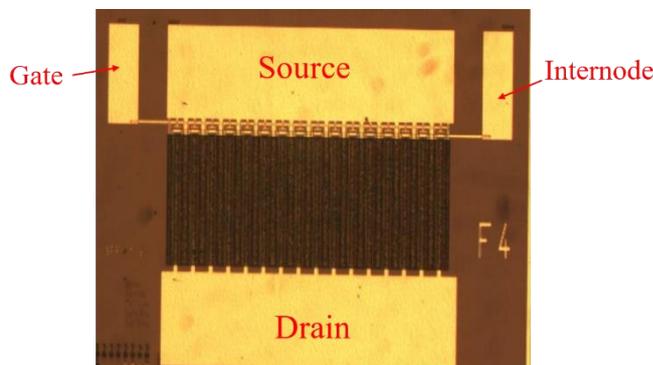


Figure 5-15 An optical image of a multi-finger integrated cascode device with an additional internode pad.

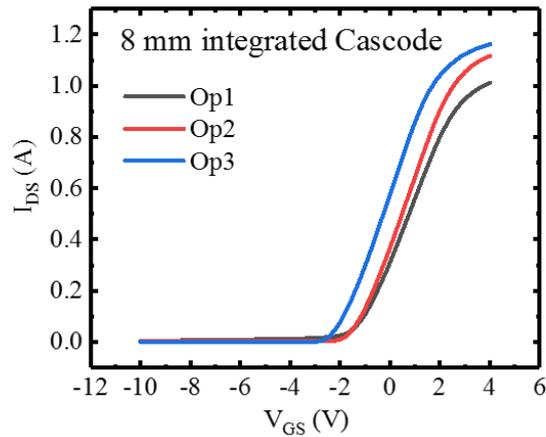


Figure 5-16 Gate transfer characteristics of 8 mm cascode devices with three different FP connections.

On-wafer switching measurements were carried out on the 8 mm cascode devices using a double pulse tester with an inductive load carrying a load current of 0.5 A. The measurement setup is the same as described in Chapter 2, but the device was on-wafer probed instead of wire-bonded. The gate resistance R_G was varied from 50 Ω to 330 Ω . The drain voltage was limited to 100 V due to leakage issues in the sample.

5.4.2 Capacitance matching

Double pulse switching tests with $V_{DS} = 100$ V, $I_{DS} = 0.5$ A, $V_{GS} = -6$ V to +4 V and $R_G = 50$ Ω were conducted for Op 1 and Op 2. Figure 5-17 shows comparison of the internode voltage waveform during the turn-on transition. Due to the relatively long probe cable of 1 m used to connect source, gate and drain electrodes, the switching measurement was subject to high parasitic inductance resulting in a large ringing effect, and therefore the switching speed was not sensible. However, the difference in the internode voltage during the off-state can still be observed. Op 2 shows an increased off-state internode voltage of 8.5 V compared to Op 1, which gives around -6 V (threshold voltage of the D-mode device). The theoretical analysis in Chapter 4 suggested that this internode voltage represents additional energy loss in the cascode compared to the standalone device, and thus needs to be minimised. The difference between Op 1 and Op 2 seems insignificant, however, the problem for Op 2 can become severe when operation at high voltage (600 V) as the internode voltage increases with an increased drain bias.

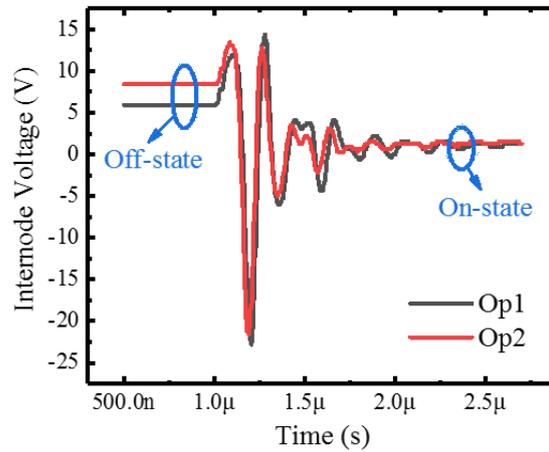


Figure 5-17 Internode voltage for Op 1 and Op 2 during the turn-on transition in the double pulse switching with $V_{DS} = 100\text{ V}$, $I_{DS} = 0.5\text{ A}$, $V_{GS} = -6\text{ V}$ to $+2\text{ V}$ and $R_G = 50\ \Omega$.

A SPICE simulation of the double pulse switching measurement was carried out to verify the experimental results and the interpretation. Table 5-1 shows the parameters used in the simulation. Device DC parameters were based on the measured values, while the capacitance values were estimated from our CV measurement shown in Figure 5-11. The output capacitance was assumed constant, which may affect the accuracy of the switching speed but should be reasonable for comparison. The only difference between Op 1 and Op 2 is the distribution of the output capacitance. We assume Op 1 has a negligible D-mode drain-source capacitance (0.5 pF), as discussed in Section 5.3. The load condition is assumed ideal using a 0.5 A current source and an ideal freewheel diode.

Table 5-1 Device parameters of an 8 mm cascode configuration used in LTSPICE.

Device parameters	Op 1	Op 2
<i>Drain voltage (V_{DD})</i>	100 V	-
<i>Load current (I_{load})</i>	0.5 A	-
<i>DC resistance (R_{dc})</i>	4.7 Ω	-
<i>Gate voltage (V_{gs})</i>	-6 V to +4 V	-
<i>Turn-on gate resistance (R_{g_on})</i>	50 Ω	-
<i>Turn-off gate resistance (R_{g_off})</i>	50 Ω	-
<i>E-mode threshold voltage (V_{th-E})</i>	-2 V	-
<i>E-mode on-resistance (R_{on-E})</i>	2.8 Ω	-
<i>E-mode trans-conductance (g_{m-E})</i>	0.2 S	-
<i>E-mode gate-drain capacitance (C_{GD-E})</i>	20 pf	-
<i>E-mode gate-source capacitance (C_{GS-E})</i>	30 pf	-
<i>E-mode drain-source capacitance (C_{DS-E})</i>	4 pf	-
<i>D-mode threshold voltage (V_{th-D})</i>	-6 V	-
<i>D-mode on-resistance (R_{on-D})</i>	3.2 Ω	-
<i>D-mode trans-conductance (g_{m-D})</i>	0.4 S	-
<i>D-mode gate-drain capacitance (C_{GD-D})</i>	23.5 pf	24 pf
<i>D-mode gate-source capacitance (C_{GS-D})</i>	30 pf	-
<i>D-mode drain-source capacitance (C_{DS-D})</i>	0.5 pf	4 pf
<i>'Miller capacitance' (C_{GD})</i>	0 pf	0pf

Figure 5-18 shows the simulated results at $V_{DD} = 100$ V. The switching speed could not match with the experimental due to the ideal environment assumed in the simulation. However, the internode voltage shows consistency with the observation from the measurement, as the internode voltage solely depends on the intrinsic capacitances and the drain voltage. We then increase the drain voltage to 600 V. As shown in Figure 5-19, the internode voltage of Op 2 increases dramatically to 40 V, but stays below 10 V for Op 1. Therefore, Op 1 is preferred due to the suppression of the capacitance energy loss at the internode.

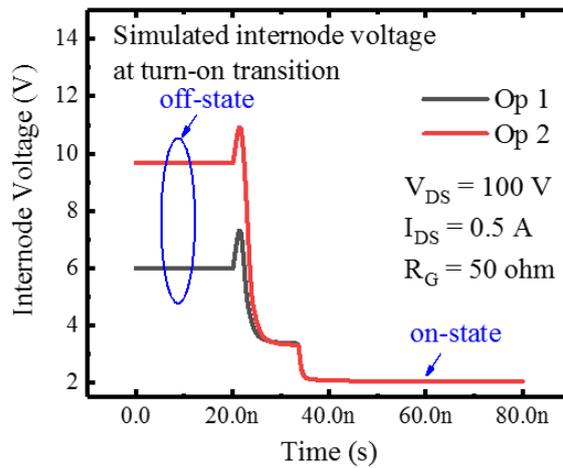


Figure 5-18 Simulated internode voltage of the cascode configuration with Op 1 and Op 2 at 100 V.

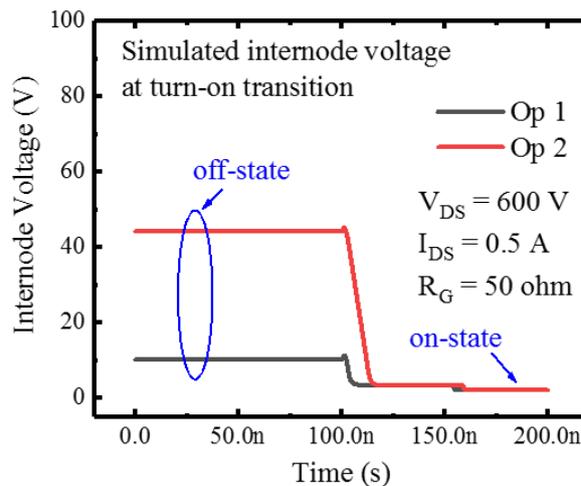


Figure 5-19 Simulated internode voltage of the cascode configuration with Op 1 and Op 2 at 600 V.

Matching the capacitance is important to minimise the additional energy loss at the internode for the integrated cascode device or the Si MOSFET avalanche loss for GaN plus Si cascode [1]. The experimental and simulated results suggest that the integrated cascode can internally address the issue, without the worry of additional parasitics, by engineering the SFP locations. Op 1 with the FP of the D-mode part connected to the source of the cascode device effectively reduces C_{DS-D} , leading to a suppression of the off-state internode voltage and thus the capacitance energy loss.

5.4.3 Turn-off switching controllability via R_G

Double pulse switching measurements with $V_{DS} = 50$ V, $I_{DS} = 0.5$ A, $V_{GS} = -6$ V to +4 V were carried out for Op 1 and Op 3. Figure 5-20 shows the comparison between Op 1 and Op 3 in terms of the turn-off controllability over the gate resistance R_G . Op 1 exhibits little change in the voltage rise time when gate resistance is increased from 220 Ω to 330 Ω , indicating the non-controllability via R_G during turn-off. While in Op 3, the rise time of the drain voltage is suppressed by approximately 8 ns with the increased R_G , due to the additional ‘Miller capacitance’ induced by the FP.

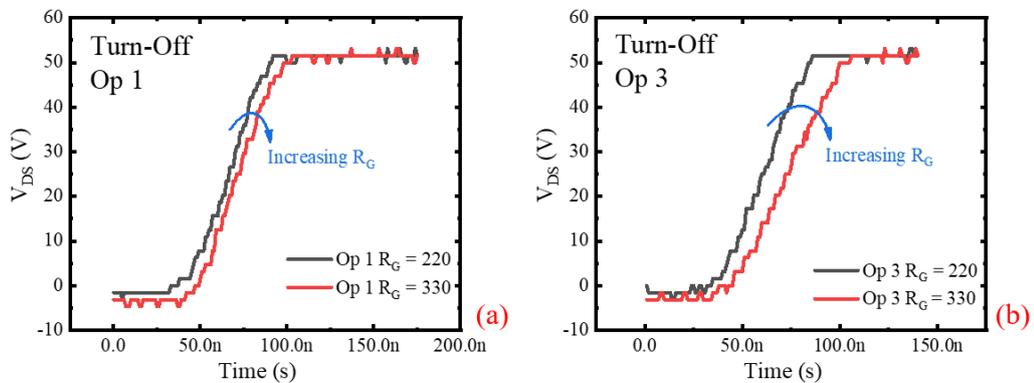


Figure 5-20 Switching waveform of V_{DS} for (a) Op 1 and (b) Op 3, at $V_{DS} = 50$ V, $I_{DS} = 0.5$ A and $R_G = 220$ and 330 Ω .

The controllability can be further improved with an increased FP induced Miller capacitance. A SPICE simulation of the double pulse switching was conducted. Table 5-2 shows the differences in the device parameters between Op 1 and Op 3, where Op 3 has additional ‘Miller capacitance’ between the drain and the gate of the cascode device. The rest of the device parameters were based on Table 5-1.

Table 5-2 Differences in the parameters used for Op 1 and Op 3 in SPICE simulation.

Device parameters	Op 1	Op 3
<i>D-mode gate-drain capacitance</i> (C_{GD-D})	23.5 pf	20 pf
<i>‘Miller capacitance’</i> (C_{GD})	0 pf	4pf

Figure 5-21 shows the simulated results of the voltage rise time for Op 1 and Op 3 with R_G increased from $220\ \Omega$ to $330\ \Omega$ ($22\ \Omega$ step size). The simulation ties up with the experimental results showing a non-controllability in Op 1, but a suppression of $5\ \text{ns}$ in Op 3 when R_G increased to $330\ \Omega$. The slightly less influence on the controllability in the simulation is possibly due to the inaccuracy in the estimation of C_{SFP} . We then varied the C_{SFP} in Op 3 from $4\ \text{pF}$ to $16\ \text{pF}$ in the simulation. An improvement of the controllability was observed as shown in Figure 5-22. Depending on the actual dv/dt requirements in the application, C_{SFP} is adjustable in the real device fabrication and can be increased by either increasing the FP extension, reducing dielectric thickness underneath or adding a second FP.

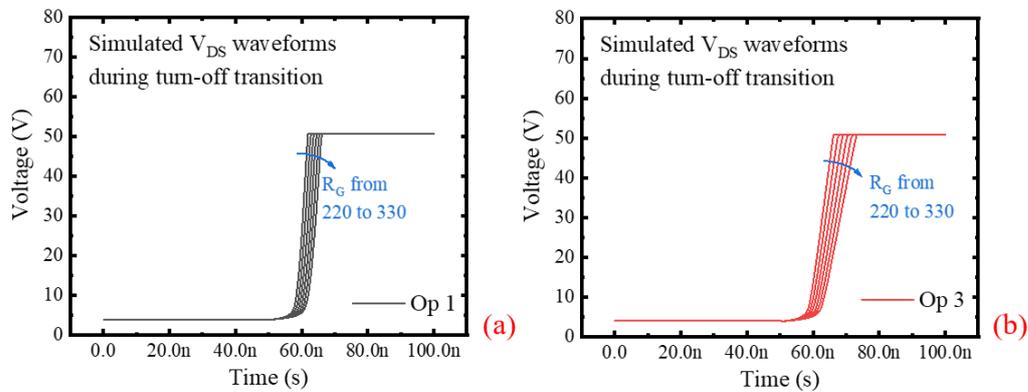


Figure 5-21 Simulated results of the voltage rise time for (a) Op 1 and (b) Op 3 with R_G increased from $220\ \Omega$ to $330\ \Omega$ ($22\ \Omega$ step size).

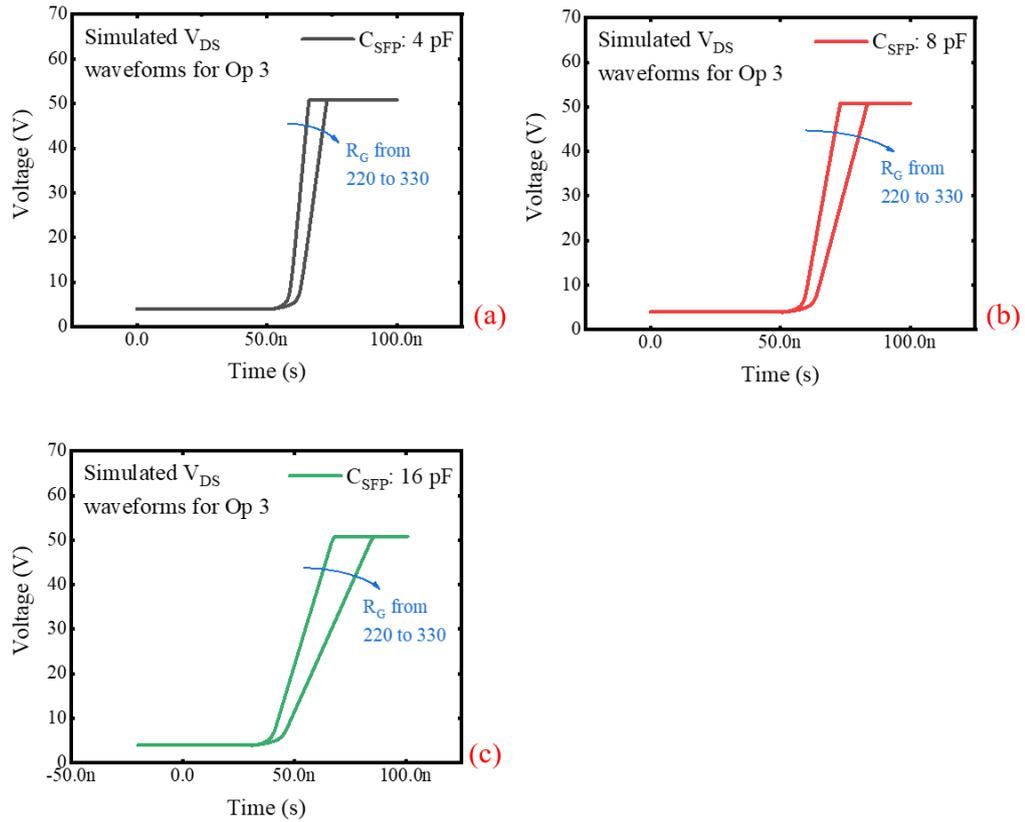


Figure 5-22 Simulated results of Op 3 with different SFP induced capacitance (a) 4 pF, (b) 8 pF and (c) 16 pF, showing an improved controllability via R_G with increased C_{SFP} .

5.5 Conclusion

In this chapter, we explored the influences of FP structures on the performance of the all-GaN integrated cascode configuration. Devices with various FP geometries were fabricated. Dynamic R_{on} and ‘back-gating’ measurements were designed and conducted to examine the surface and buffer related current collapse in the devices. Experimental results show that the surface related dynamic R_{on} can be sufficiently suppressed by increasing the FP extensions or implementing multiple field plates. However, there is a tradeoff between the FP extensions and the intrinsic capacitances of the device. An analysis to identify the role of FPs in the dynamic characteristics of the intrinsic capacitances was presented based on the high voltage CV measurement of the fabrication device. Multiple field plates are preferable to achieve low surface related dynamic R_{on} and reduced Miller capacitance at the same time.

We compared three different FP connections in GaN integrated cascode transistors for switching applications. Experimental and simulated results show that a FP connected to the source terminal of the cascode is preferable for higher switching efficiency due to the suppression of the internode voltage during the off-state and reduces additional intrinsic capacitance energy loss. The FP connected to the E-mode gate can improve the cascode switching controllability via R_G during turn-off and reduce dv/dt in the drain loop.

5.6 References

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6 Conclusion and recommendations for future work

6.1 Conclusion

We have demonstrated an all-GaN integrated cascode configuration for high power and high frequency applications. A positive threshold voltage of +2 V is achieved by F- treatment under the E-mode gate region plus a MIS gate structure with nominally 20 nm SiN_x. A maximum output current of 300 mA/mm is achieved and is equal to the standalone E-mode device fabricated using the same technology. The output current handling of the integrated cascode device is improved by engineering the V_{th} of the D-mode part towards more negative (-8.2 V) with a MIS gate structure. TCAD simulation shows that the 2DEG between the E-mode and the D-mode gate is the key to distinguish between the integrated cascode and the standalone device with a SFP, which enables cascode switching behaviour for the device. The high voltage all-GaN integrated cascode configuration exhibits a faster switching speed and 35% (21%) less in turn-off (turn-on) switching energy loss under 200 V hard switching measurement using a double pulse tester, compared to the equivalent GaN standalone devices. The advantage originates from the reduced effective Miller-capacitance and the unique switching mechanisms in the cascode configuration. Compared to equivalent standalone E-mode devices, practical power switches show faster switching when incorporated into the cascode structure. The penalty to pay is a slightly more complicated design and higher on-state resistance.

An analytical study has been presented aimed at a comprehensive understanding of the switching behaviour of the all-GaN integrated cascode device. Mathematical equations are derived for the turn-on and turn-off process and are verified with SPICE simulation results. Derived equations show that the speed advantage of the cascode device originates from larger charging and discharging current through the output capacitance. The cascode configuration is able to use the maximum channel current and the full load current for turn-on and turn-off, respectively. In both cases the switching speed of the standalone device can be limited the gate driving current. The derivation of the critical gate resistance is given, where the standalone device starts to suffer from the Miller effect and the cascode configuration becomes faster compared to the standalone device. A theoretical comparison of the switching energy

loss between the cascode and standalone device has also been presented. The cascode device features less current voltage overlap loss due to faster switching speed, but needs careful control over the additional capacitance energy loss at the internode. The suppression of the additional energy loss can be achieved by reducing the ratio between the drain-source capacitance of the D-mode part and the sum of all capacitances at the internode. In addition, the D-mode V_{th} should not be over engineered beyond the optimum value to achieve the highest DC output current, otherwise additional capacitance energy loss occurs. Finally, the drain-source capacitance of the D-mode part and the gate-drain capacitance of the E-mode part need to be minimised for the optimum switching performance. The analysis provides a thorough understanding of the cascode device for future optimisation and facilitates prediction of the device's switching performance.

FPS play an important role in suppressing the dynamic R_{on} and control the intrinsic capacitances of the cascode device. Devices with various FP geometries were fabricated and dynamic R_{on} measured with 'back-gating'. Experimental results suggest that the surface related dynamic R_{on} effect can be significantly suppressed with larger field plate extensions. For the standalone device, multiple FPS are preferred to control the Miller capacitance, compared to a single FP structure with long extension. While the FP design in the integrated cascode configuration does not need to be concerned about the Miller capacitance, it needs to consider the capacitance matching between the E-mode and D-mode devices, and the controllability over the voltage rise time during turn-off. The internode and the gate of the E-mode cascode devices with a FP were designed and fabricated. Compared to the device with the FP connected the internode, the source-connected one exhibits a reduced internode voltage (equal to $-V_{th-D}$) at the off-state due to minimised drain-source capacitance in the D-mode part, leading to a smaller capacitance energy loss. The simulated results suggest that this advantage increases considerably when operating at higher drain bias. Experimental and simulated results show that the turn-off switching speed can be controlled by connecting the FP to the gate of the E-mode device, which creates a 'Miller capacitance' to the integrated cascode device. Compared to the conventional GaN plus Si cascode, the all-GaN integrated cascode configuration can internally match the capacitance and improve the switching

controllability with different SFP locations, without the worry of additional parasitics from external components.

6.2 Recommendations for future work

The all-GaN integrated cascode configuration proposed in this study is not limited to any E-mode technologies for GaN HFETs. It will be interesting to look at the integrated cascode device with other E-mode technique e.g. p-type gate, and compared the performance between the equivalent p-type gate standalone devices. The author suspects that the p-type gate device may have a higher internal gate resistance due to the p-GaN layer used underneath the gate metal. The cascode device shows considerably increased speed advantages when the total gate resistance is high (low gate drive current) in the equivalent standalone device. Therefore, the high gate resistance p-type based GaN standalone devices may still be suitable for a cascode configuration.

The switching performance in this study was measured using a standard double pulse tester. It is necessary to explore the performance in various power modules such as DC-DC converters, to confirm the advantages over the standalone devices, and to identify the applications where cascode can be more suitable.

The measurement setups used in this study can be further improved for higher measurement resolution. For example, the double pulse tester can be optimised by having a freewheel diode with lower parallel capacitance and faster gate driver, and thus the switching speed of the device can be better observed. A more advanced high voltage CV measurement setup is needed to monitor the very low intrinsic capacitance (<1 pF at 200 V) for GaN HFETs. A faster pulsed measurement setup is also preferred to observe the dynamic R_{on} effect within the hundreds of ns range after the stress is removed. The improved measurement ability will enable a more accurate understanding of the devices.

Future work can also be done to improve the accuracy of the analytical study for the cascode device. The dynamic characteristic of the transconductance and the intrinsic capacitance can be considered. In addition, the fact that the D-mode device has a higher current drivability compared to the E-mode device can be included, although

the ultimate goal is to achieve the E-mode device without any degradation. The current difference in the D-mode and E-mode part may vary the optimisation criteria for the integrated cascode device.

Beside the three different FP connections discussed in this study, a biased FP can be an option for both standalone and integrated cascode devices. It will be interesting to compare devices with conventional FP structures and a FP either biased with a positive voltage or grounded to the system ground. A positively bias FP can effectively reduce the pinch-off voltage of the FP without changing the FP geometries, and thus the induced capacitance. However, due to the reduced pinch-off voltage, the total output charge can be reduced, which may lead to an improved switching figure of merit. A device with a separately grounded FP can be useful in some particular applications. For example, the FP induced drain-source capacitance of the high side power switch in a half bridge topology, may act as a bypass capacitance with no contribution to the switching speed if the SFP is connected to the system ground instead of the source of the device. The penalty to have an additional SFP connection is the added parasitics and needs careful design in the device packaging.

Lastly, comparing the different pinch-off voltages of the FPs on the device switching performance will be a useful future study. The lower pinch-off voltage often means that the FPs are closer to the surface, leading to higher capacitance. At the same time, the lower FP pinch-off voltage allows the capacitance to drop at a lower drain voltage. Therefore, the influence on the total charge remains unknown and could be explored with different dielectric thickness underneath the FPs.