EMC Performance of Field Programmable Gate-Arrays: Effects of I/O Standards and Attributes on the Radiated Emissions Spectrum

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Abstract

This research investigates what impact the I/O standards & attributes of a Field Programmable Gate Array have on the radiated emissions spectrum. FPGAs are used in countless digital applications. The use of a Spartan-6 FPGA gives a good representation of a general device with Xilinx being the market leader in supplying FPGAs for a variety of industries. The logic standard, drive strength and edge rate are examined for their impact on that radiated emissions produced. Digital integrated circuits are a well-known and documented source of Electromagnetic Interference due to the fast transitions of period signals. A practical and theoretical understanding of the behaviour of clock signals in the time and frequency domains has been established. The impact of phenomena such as overshoot and ringing from practical signals has been considered for its impact on the emissions spectrum and how this deviates from the theoretical expectations. Logic standard, drive strength and edge rate have been assessed comparatively to determine their influence of peak emissions produced. Of the logic standards tested the LVTTL standard recorded the highest level of EMI across all I/O logic standards approximately 4dB higher than the equivalent CMOS standards. The LVTTL standard recorded the largest variation in emissions across the available I/O driver settings with approximately a 14dB increase from the minimum to maximum I/O driver settings. The LVCMOS logic standards recorded on average across the 3.3 volts, 2.5 volts, 1.8 volts, 1.5 volts and 1.2 volts logic, a maximum change to EMI of approximately 10dB from the minimum to maximum driver settings. Each category of the variable I/O driver settings has been assessed independently to assess the level of change to emissions produced. Average levels of EMI produced under each I/O driver setting have also been obtained and presented to give engineers and designers an indication of how decisions made within the design process can influence the level of emissions produced. It is hoped that this research will provide as a useful tool when designing with programmable integrated circuits such as the Spartan-6 FPGA and the potential EMC impact on the radiated emissions spectrum.

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Finally, I would like to dedicate this research to the memory of my mother Susan Boden. If not for you moments like this would not have been possible. I am forever grateful.

Declaration

I declare that this thesis is a presentation of original work and I am the sole author. This work has not previously been presented for an award at this, or any other, University. All sources are acknowledged as References.

1 Introduction

This report investigates the effect of Field Programmable Gate Arrays (FPGAs) on the electromagnetic (EM) spectrum, more specifically the peak levels of emissions they produce in the near field under the range of I/O (input/output) driver settings available within the chosen device.

The introduction of FPGAs has brought about a new generation of circuits and systems. Faster I/O and bidirectional data buses, coupled with RAM blocks allows a design engineer to implement complex digital computations within a single integrated circuit (IC). The freedom of functionality within this device has led to its use in countless applications of digital circuitry throughout industry and academia. Digital circuits are a well-documented source of Electromagnetic Interference (EMI) due to the harmonic content of pulsed waveforms with fast transitions [1], [2]. The level of EMI produced by a digital circuit is influenced by a number of additional factors other than the edge rate of signals, for example choice of components, clock frequency, circuit layout, shielding and even circuit design [1]. One of the difficulties a designer faces is that these factors are not adequately quantified in terms of their contribution to a circuit's Electromagnetic Compatibility (EMC) performance. A significant effort is being made throughout industry and academia to understand how the evolution of integrated circuits has influenced their EMC performance and how best to manage and mitigate any EMI produced through various EMC design techniques [3], [4]. EMC design techniques for designers are either an unknown or not given sufficient consideration until after the fundamental design decisions that will affect the level of emissions have been made. In reality, the later into the design process that EMC is considered the greater the costs are of implementing the necessary design techniques to achieve EMC compliance. Within this project, logic standard, drive strength and edge rate are examined for their impact on the radiated emissions spectrum when varied across their respective ranges within a Spartan-6 FPGA device. The aim is to equip a designer with the ability to quantify any increase to the EMI produced from changes made to the I/O driver settings of an FPGA. Having this quantitative knowledge will not only help to identify the sources of EMI within a digital circuit; it will also allow the designer to make informed decisions within the conceptual design phase on how to reduce the overall EMI a system may produce. The further into a design that EMC is considered the greater the costs are of implementing the methods of reducing EMI or improving EM immunity, furthermore to this the available fixes that the designer can implement without massive cost is reduced as the development lifecycle progresses.

1.1 EMI from Digital Circuits & Systems

There are many contributing factors to EMI generated by digital circuits; clock signals have been identified as one of the more significant [1], [2]. An 'ideal' clock signal possesses instantaneous and symmetrical rise and fall times making it the perfect square wave. A perfect square wave in practice is not achievable, as it not possible to transition from '0' to '1' in an infinitely small time. Practical clock signals exhibit characteristics that take it away

from the approximation of 'ideal' [5]. The rise and fall times of a practical clock signal are finite in time, making the signal shape more representative of a trapezoidal waveform. In addition to possessing finite rise and fall times, practical clock signals exhibit effects such as ringing and rounding of the transitional edges. Ringing results in overshoot and undershoot on the peaks and troughs of the signal as the potential settles at its intended state. The rounding of the transitional edge, curves the signal as it approaches the intended state increasing the overall rise time of the signal. An approximation of a square wave clock signal is illustrated in Figure 1, identifying the intrinsic properties that will form the basis of the theoretical frequency domain behaviour calculations to allow comparison against the practically obtained results.

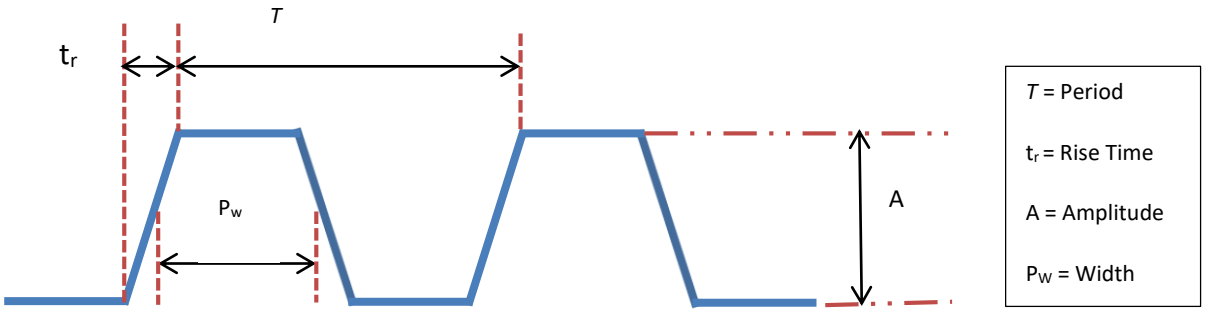


Figure 1: Properties of a Clock Waveform [5], [6]

If the rise and fall times are symmetrical, the harmonic current $I_{(n)}$ at the n^{th} harmonic is:

$$\boldsymbol{I(n) = 2A\left(\frac{(P_w)}{T}\right)\left(\frac{\sin n\pi\left(\frac{(P_w)}{T}\right)}{n\pi\left(\frac{(P_w)}{T}\right)}\right)\left(\frac{\sin n\pi\left(\frac{t_r}{T}\right)}{n\pi\left(\frac{t_r}{T}\right)}\right)}$$

Equation 1: Fourier Transform Equation [6]

The Fourier series of an 'ideal' square wave gives an accurate representation of the sum of sinusoids at the fundamental and harmonic frequencies [7]. The spectrum behaviour of a periodic signal is calculated using the amplitude 'A' of the time domain signal and the equation contains two $\frac{\sin(x)}{(x)}$ functions using the pulse width and the rise time of the signal to calculate the additional behaviour that introduce the minima seen within the comb spectrum in Figure 2. A square wave signal possessing symmetrical rise and fall times contains an infinite number of odd harmonics. The amplitude of these harmonics is determined by the frequency, edge rates and amplitude of the periodic signal being examined. The introduction of even harmonics into the frequency spectrum occurs when the rise and fall times of a clock signal are asymmetrical. In the frequency domain, a periodic signal as shown in Figure 1 has a line or comb spectrum envelope. An approximation of this straight-line envelope and spectral behaviour is illustrated in Figure 2, identifying the decay rates of the harmonic amplitude. The amplitude of the harmonics $I_{(n)}$ remains constant until a first break point of $F_1 = \frac{1}{\pi P_w}$. Beyond this first break point the amplitude of $I_{(n)}$ decays at a rate of

approximately 20dB/decade until a second frequency break point of $F_2 = \frac{1}{\pi t_r}$, at which point $I_{(n)}$ begins to decay at a rate of 40dB/decade [1]. One of the major differences between the theoretical and practical frequency domain behaviour is that square wave signals with instantaneous rise and fall times only exhibit the one break point F_1, and would decay at a rate of 20dB/decade until the harmonics were at a level that they fall below the noise floor.

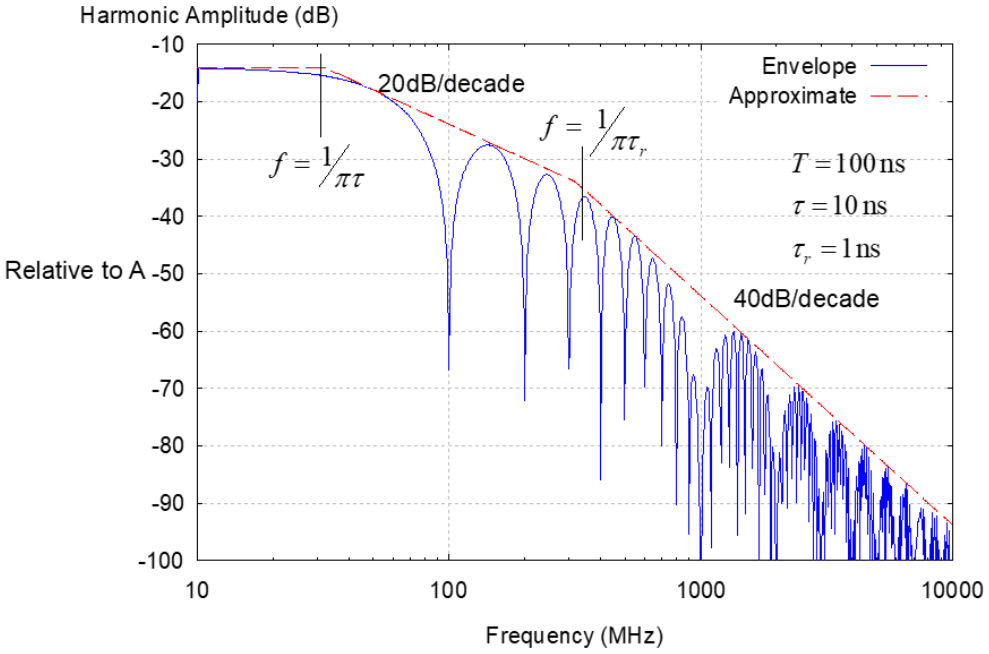


Figure 2: Frequency Domain Behaviour of a Periodic Signal [5], [6]

From the relationship between edge rate and spectral properties, it becomes apparent that the properties of a signal will significantly influence the peak level of emissions produced by a circuit or system. The faster the edge rates of a signal the greater amplitude of harmonics further along the EM spectrum. The only way to ensure any EMI would not cause a non-compliant system is to develop an understanding of how design choices, such as the logic standard and edge rate and drive strength of signals impacts upon the frequency spectrum and ultimately how to design for EMC compliance and signal integrity.

1.1.1 EMI from Practical Signals

Applying periodic signals to practical circuitry further takes the signal away from the 'ideal' approximation illustrated in Figure 1. In addition to practical signals possessing finite switching times, the signal will present with ringing (oscillations) or rounding of the edges of a signal transition. These effects are present within digital signals due to the component values of physical hardware, for example a capacitor, inductor, wire or a PCB trace. A PCB trace will have an inductance L, capacitance C and a resistance R value giving it an L-C-R circuit response. Having accurate L-C-R models, as illustrated in Figure 3, to predict how practical circuitry will respond to high frequency clock signals has been identified as one of the critical components in high-speed circuit design [8].

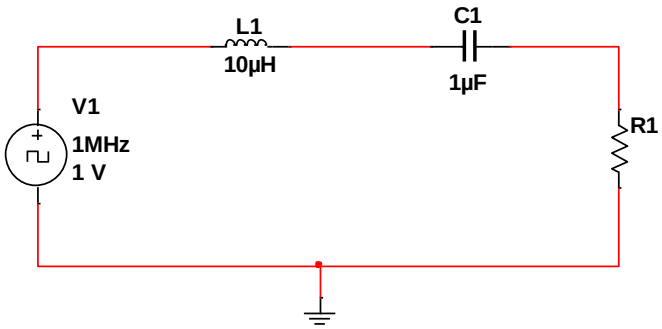


Figure 3: L-C-R Circuit Example

Theoretically simulating the behaviour of an L-C-R circuit gives an indication of the phenomena that occurs when applying signals of this nature to practical circuitry. Using the circuit illustrated in Figure 3, the source voltage is set to be V_1 = 1V, the capacitance C = 1µF, the inductor L = 10µH and the resistor values for the underdamped (UD), critically damped (CD) and over damped (OD) responses are R_{UD} = 40Ω, R_{CD} = 200Ω and R_{OD} = 1kΩ. Using MATLAB, the behaviour of an L-C-R circuit is modelled to examine the step response with 3 different values of damping resistance. Figure 4 illustrates the different step responses of an L-C-R circuit with an increasing damping resistance to control the properties of the signal.

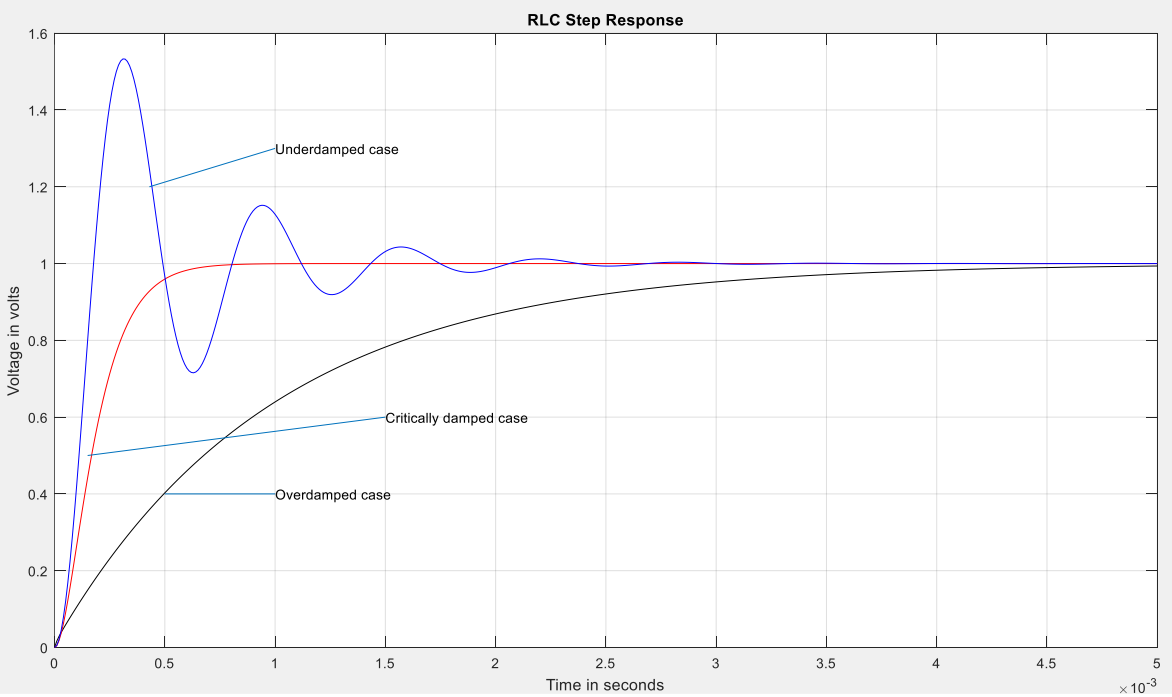


Figure 4: L-C-R Step Response

The blue trace shows the underdamped step response illustrating ringing on the peak of the signal. In relation to the signals produced by the FPGA, this case is likely to occur when using an excessive drive strength and 'Fast' edge rate setting, resulting in excessive drive current. The red trace shows the critically damped case, which is likely to occur when using a low-end drive strength setting and 'slow' edge rate. Finally, the critically damped case shows when the damping resistance is too high and the rise time of the signal is drastically increased. This case

is unlikely to occur when outputting signals from the FPGA as the damping resistance is unlikely to be this excessive on the PCB designed for this project, yet it is included for illustrative purposes of all cases of an L-C-R circuit response. The impact of these effects on the frequency spectrum will vary between each case. The underdamped case, with the ringing on the peak and troughs of the signal, will introduce additional harmonics into the spectrum at the frequency in which it is oscillating. The critically and overdamped case increases the overall rise time of the signal. As a result of damping the signal the harmonics that are present within the frequency domain will be attenuated ultimately altering the EMC performance of the system and integrity of the signals produced. The frequency response of an L-C-R circuit must be taken into account when designing high speed digital circuits. The reactance of the inductor and capacitor shown in Equation 2 and Equation 3 respectively will impact upon the signal applied and ultimately its frequency domain behaviour. As the frequency of the harmonics increases the inductive reactance (X_L) increases the capacitive reactance (X_C) decreases.

$$X_L = 2\pi f L$$

Equation 2: Inductive Reactance

$$X_C = \frac{1}{2\pi f C}$$

Equation 3: Capacitive Reactance

This relationship between frequency and component reactance leads to a capacitive and inductive region along the frequency spectrum as illustrated in Figure 5. When designing high speed digital circuitry the effect of this behaviour must be taken into account. The fundamental frequency of the signal in question is chosen to be at the resonance point of the series L-C-R circuit, ensuring minimal attenuation as a result of the parasitic component properties.

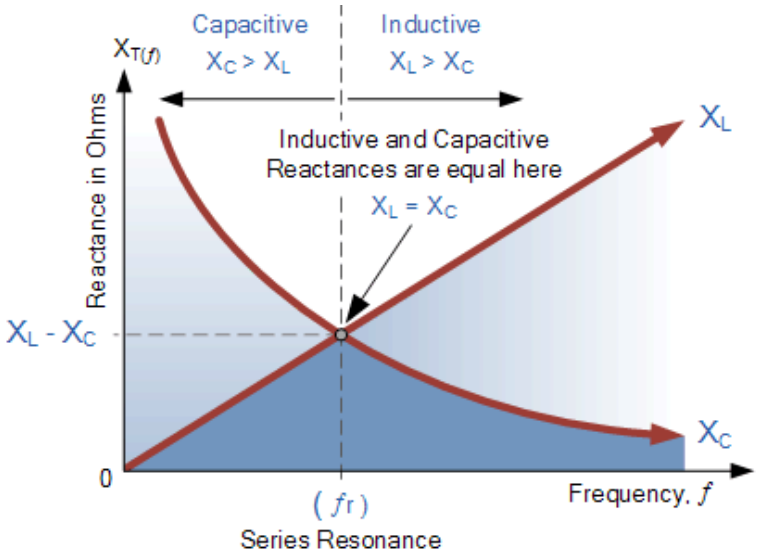


Figure 5: L-C-R Frequency Response [9]

The rounding of the signals transitional edges stem from the attenuation of the harmonics of the signal being used. The increasing frequency of the harmonics present means that the inductive reactance that they encounter is increasing linearly with frequency. Some potential impacts from this attenuation is that the hardware receiving the data may not be able to sufficiently sample the signals being received leading to timing issues and data loss.

1.2 Historical Review of EMC Studies of Integrated Circuits

Earlier studies into the EMC performance of integrated circuits were aimed towards the immunity of components in harsh Electromagnetic environments. The evolution of integrated circuits meant that the power consumption and frequency of transmitters were increasing adding to the severity of the EM environment. Research into the immunity of ICs within circuit operation became a vital part of academic research. Whalen [10] studied the effect of EMI on devices such as the 7400 series NAND gates and showed that the output varied with incident power. From the effects noticed during immunity testing, Larson *et al* proposed modifications to the transistor model to account for the unusual conditions of RFI [11]. The new Ebers-Moll model allows for the RF behaviour of a transistor to be predicted when the interference conditions are theoretically deduced rather than observed. The introduction of CMOS technology began to replace the existing bipolar technologies (TTL) due to the vast improvement to the power dissipation, and comparisons of their susceptibility to EMI began. Kenneally *et al* [12] reported that the new CMOS technologies were less susceptible to EMI at frequencies above 5 – 10 MHz, and virtually insensitive to EMI at frequencies above 100 MHz. Laurin *et al* [13] investigated the effect of EMI on the 6809 microprocessor from Motorola and recorded function loss in oscillator circuits when placed near a current loop. The advancement of CMOS technologies allowed for larger and denser devices; and calls for low-emissive, high-immunity ICs within the frequency band 1MHz – 1GHz began to rise [3]. Research into investigating and controlling the emissions from ICs began in an attempt to investigate their contribution to the EM environment [3]. It was not until the 1990s that the impact of emissions from embedded components was considered [3]. The origins of IC emission measurements stem from a phenomenon identified as simultaneous switching noise (SSN), where studies showed that the noise amplitude was influenced by the number of switching output drivers and grounding techniques [14]. Research into the effect of logic families and circuit design techniques was published by Robinson *et al* [1] in 1998 who discovered that emissions in the near and far field were dependent upon a combination of the component choice and circuit design. Component choice in this case is relating to the variation of logic inverters from the CMOS & TTL families, and the circuit design was the inclusion of a ground plane to reduce the loop size of the traces on the PCB. Peak emission measurements were taken in an open area test site and the greatest improvement to emissions was observed when technologies with slower switching frequencies and EMC design techniques were combined, delivering a reduction to emissions by over 30dB. Considering the component technology - independent of any circuit design techniques - the 74ACT technology delivered the highest peak emissions in comparison to the 74LS devices with a mean difference of 8dB. This established that the rise and fall times can have a

substantial impact on the amplitude of harmonic content observed - irrelevant of any circuit design techniques applied.

The parasitic emissions from an IC are attributable to the I/O and the digital synchronous cores. Work by Takashima *et al* [15] proposed that the number of I/O used directly influenced the parasitic emissions from ICs. Van Wershoven [16], using the Taguchi method in an attempt to build a picture of the EMC performance of ICs, discovered that controlling attributes such as the slew rate of the I/O drivers reduced the impact on supply and ground bounce present within a system. With an increase to the number of I/O affecting emissions, combining this with a faster slew rate could produce an exponential rise to EMI in the near and far field. Should a device with variable slew rate be used within a system - where it is supply voltage critical - then variations on the supply and ground rails could potentially cause a malfunction to the system operation. In addition to the number of I/O used and the technology chosen, the software or firmware implemented within a programmable device will affect the overall emissions [17]. Fioro *et al* [17] conclude that emissions produced are influenced by the embedded software within an 8-bit microcontroller. Often within digital circuits, there are multiple ways of implementing a design to achieve the same function, so care should be applied when utilising a device such as a microprocessor. Methods of reducing these parasitic emissions from ICs came to the forefront of research as calls for low emissive devices were growing rapidly. The most popular and effective methods of controlling the levels of radiated EMI was the inclusion of on-board and on-chip decoupling capacitors [3], and a technique known as spread spectrum clock generation (SSCG). Hardin *et al* [18] proposed this method of SSCG which intentionally spreads the energy of a narrowband signal to wideband reducing the amplitude of the harmonics. An attenuation as high as 13dB was recorded from this testing and can be applied to emissions produced by the digital synchronous core and I/O to similar effect.

Power supply noise is another consideration when analysing the EMC performance of integrated circuits (ICs). Research has delved into not only practically testing the ICs but developing methods into the prediction of how the power supply noise may present itself based on IC operation and implementation. Modern devices containing millions of gates all switching state simultaneously causes substantial current to be drawn from the power distribution network (PDN) [19]. Laurent [20] found that power supply noise was likely to cause timing issues before any other failures within the IC occurred. Laurent [20] also found that the measured peak noise is largely irrelevant and the average noise during switching is a greater factor when determining the EMC performance of an IC. Ren [19] *et al,* found that once the PDN has been established the power supply noise can be estimated from the impedance network. The simulated and measured values were relatable in both the time and frequency domain [19]. The designer must be aware of all potential sources of EMI and the implications of using a device or technology within a design. Having this quantitative knowledge in the earlier stages of a design process will allow for EMC measures, such as effective shielding and grounding, to be implemented. From this, an optimised design can be achieved that satisfies both EMC compliance and signal integrity.

1.3 FPGA Overview

Section 1.3 gives an overview of the architecture of an FPGA and examines the circuitry relating to the I/O buffer standards. More specifically an overview into the two standards that form the basis of this research, Low Voltage CMOS (LVCMOS) and Low Voltage TTL (LVTTL).

1.3.1 FPGA Basic Architecture

The architecture of an FPGA illustrated in Figure 6, consists of configurable logic blocks (CLBs), I/O Blocks and Routing Channels; all interconnected by Connection Boxes (CB) and Switch Boxes (SB). The vertical and horizontal routing channels are linked through switch boxes and the CLBs are connected to the routing channels through connection boxes [21]. The routing channels allow connections among the internal logic blocks to implement any user defined digital circuit.

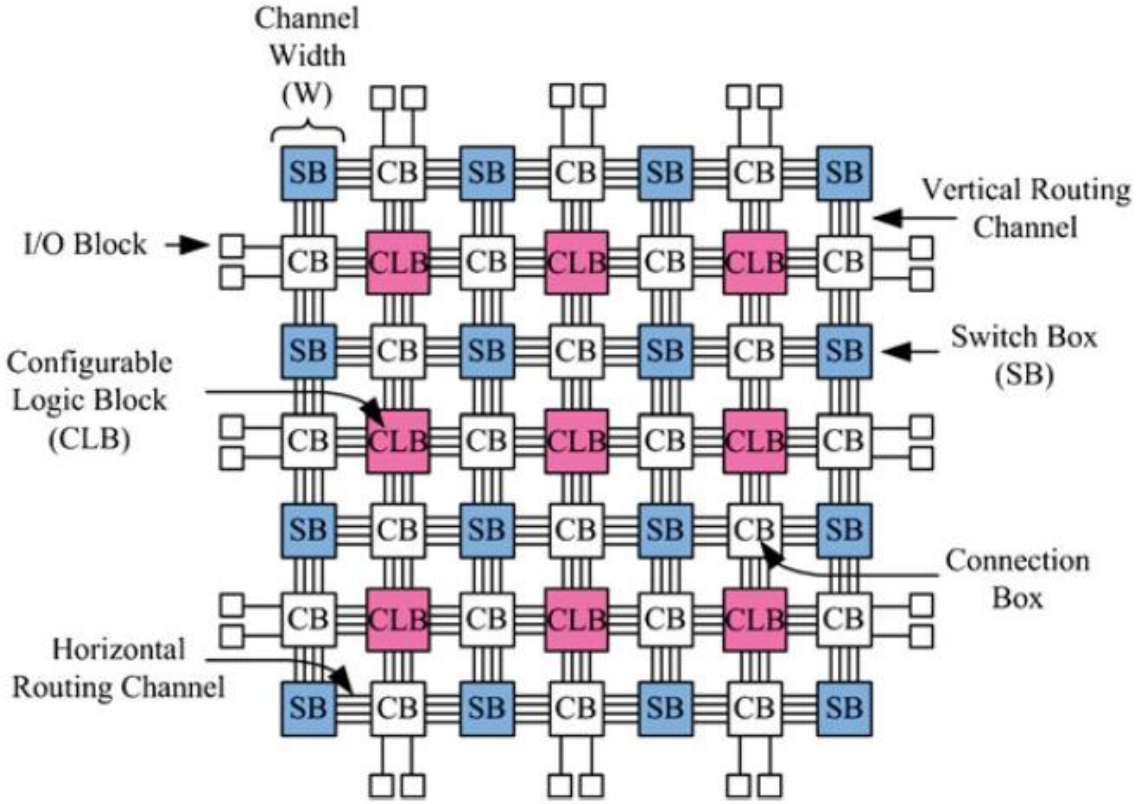


Figure 6: FPGA Architecture Overview [21]

1.3.1.1 Configurable Logic Block

The configurable logic block is the component of an FPGA that provides basic logic and storage functionality for digital circuit designs. Each of the configurable logic blocks consist of an array of Basic Logic Elements (BLEs) varying from 4 to 10 - depending upon the manufacturer [21]. The basic logic elements are made up of an n-bit look-up table (LUT), a D-Type Flip-Flop, and a 2x1 multiplexer (MUX), as shown in Figure 7.

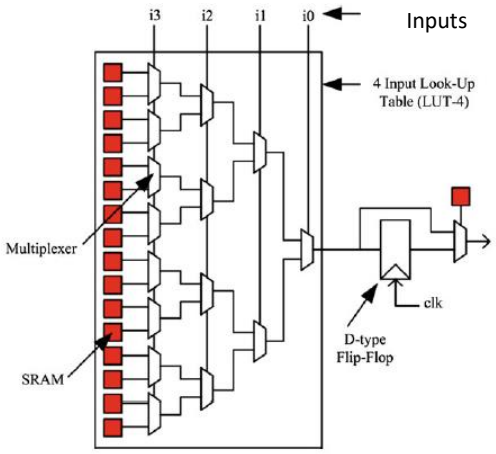


Figure 7: Basic Logic Element [21]

The Static RAM (SRAM) cells of an LUT are used for routing the interconnections and programing the Configurable Logic Blocks that implement the logical functions of a design [21]. The D-type flip-flop allows the user to synchronise the output with the internal clock or act as a storage element. The multiplexer gives the designer the choice between the output of the D Type Flip-Flop or the LUT.

1.3.1.2 FPGA I/O Block

The FPGA I/O block (IOB), shown below in Figure 8, connects the internal logic to the outside world allowing the designer to communicate with peripherals within the circuit or system. The buffering stage of the IOB consists of the input and output buffers. The input and output buffers have the ability to apply a passive pull up or pull down to provide a known state to the connecting PCB traces. The array of D-Type Flip Flops and Multiplexers form the input logic and output logic circuitry. A Spartan 6 FPGA I/O block contains two IOBs, two ILOGICs, two OLOGICs and two IODELAYs shown in Figure 9 [22].

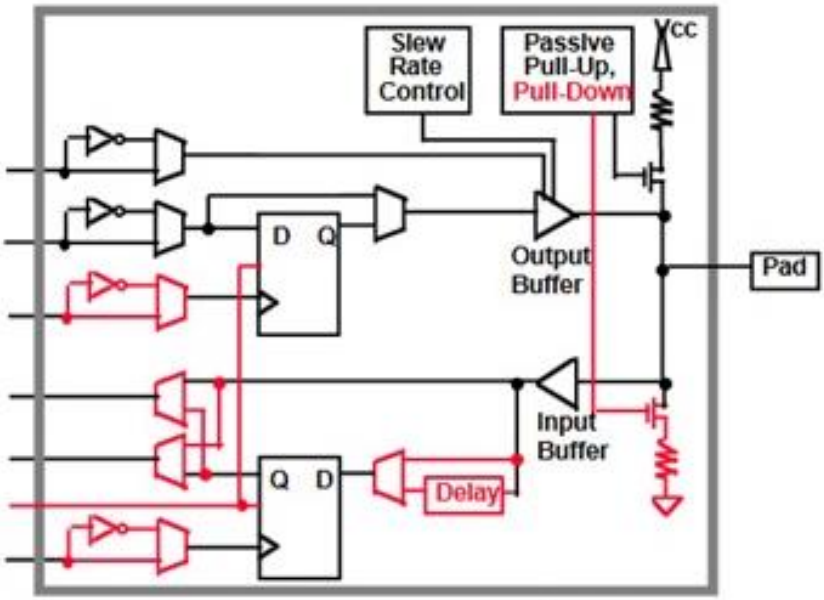


Figure 8: FPGA I/O Block Overview [23]

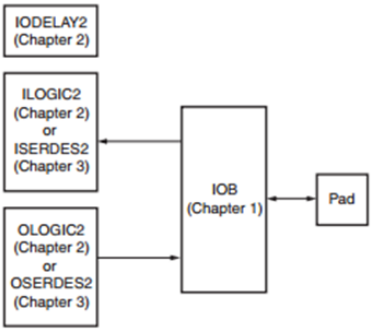


Figure 9: SPARTAN-6 FPGA I/O Block [22]

The I/O Blocks fall into two categories either single-ended standards or differential standards. The focus of this research is limited to following standards - LVCMOS (1.2V, 1.5V, 1.8V, 2.5V and 3.3V) and LVTTL (3.3V) single-ended I/O standards.

1.3.2 FPGA LVCMOS & LVTTL Logic Standards

The properties of the two I/O logic standards are well documented throughout established literature [24], [25], [26]. The more notable differences being switching speed, power dissipation, output drive capabilities, and logic levels [24]. Each of the I/O buffers within the Spartan-6 FPGA have the ability to configure the logic standard, drive strength and slew rate of the respective drivers. The slew rate setting within the FPGA controls the rate at which the output of the buffer can change. Varying the drive strength introduces additional transistors in parallel to change the current delivered to the load. A combination of an excessive drive strength and a fast slew rate can introduce phenomena such as ringing (overshoot and undershoot) and rounding of the transitional edges. It is likely that because of these phenomena, issues such as timing, component oscillations and an increase to the overall emissions produced will occur.

1.3.3 FPGA Output Buffer Circuit Overview

The FPGA I/O buffers hold the configuration illustrated in Figure 10, consisting of two P-channel and two N-channel MOSFET devices. This buffer configuration is used to meet the LVCMOS (Low Voltage Complimentary-Metal-Oxide-Semiconductor) and the LVTTL (Low Voltage Transistor-Transistor-Logic) Standards.

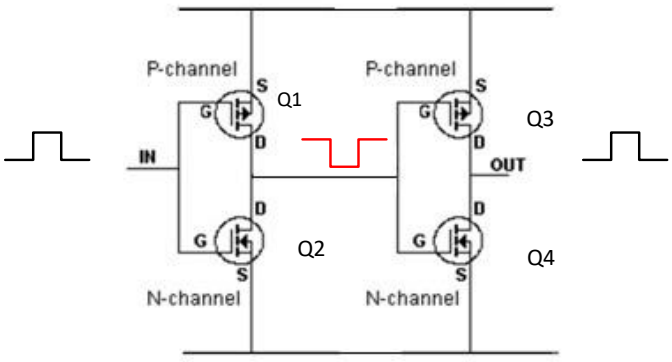


Figure 10: Output Buffer Circuit [27]

When source of Q1 is more positive than the gate, the channel is turned on and providing that the threshold voltage (V_{TH}) is positive enough current flows between the source and the drain. As the input signal transitions to logic '1' Q1 turns off and as it returns again to logic '0' Q1 turns on again. The N-Channel Q2 transistor having zero voltage between the gate and the source remains in the OFF state. The second parallel combination of Q3 and Q4 performs the same function as described with Q1 and Q2 and inverts the signal back again to its original state.

1.3.4 Logic Family Comparison

The evolution of logic families has seen CMOS technologies dominate and the bipolar TTL family become an almost extinct logic family except for demonstrations and academia. Figure 11 illustrates a timeline for the progression of logic families since the 1960s.

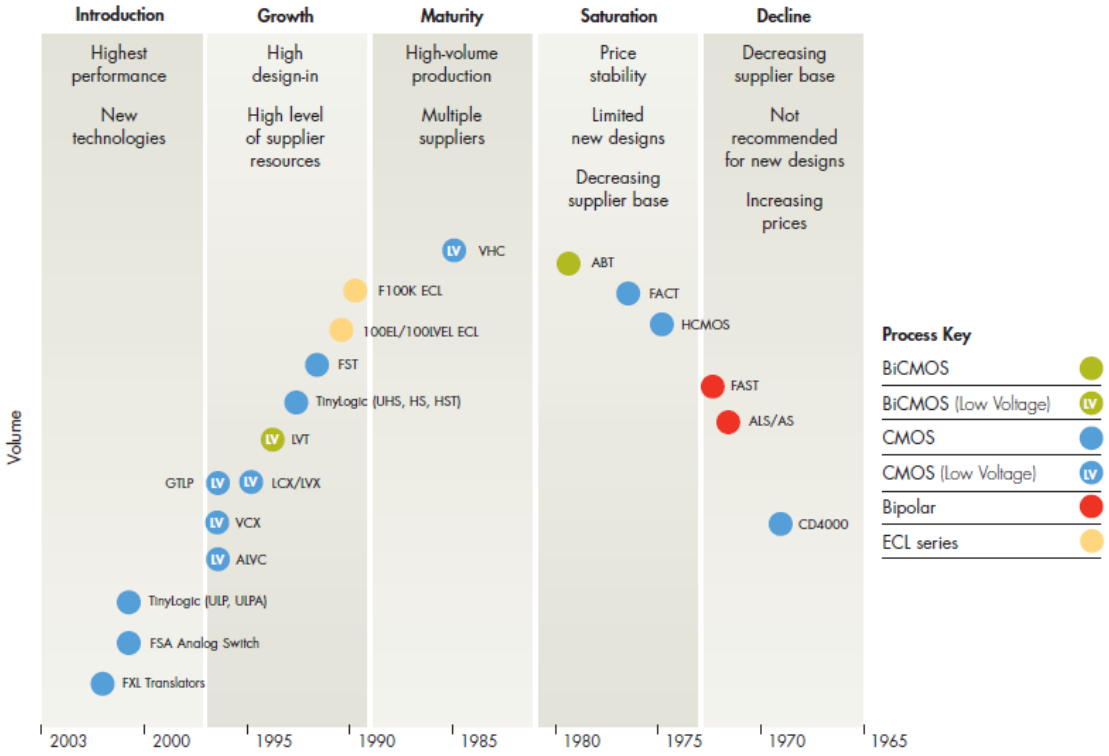


Figure 11: Logic Family Timeline [26]

The bipolar TTL logic family was the most commonly used logic family in industry and academia in the 1960s to 1970s. The introduction of CMOS technologies in the late 1970s began to displace TTL due to its superior performance and improved susceptibility to EMI. The two logic families that dominated the 1980s and 1990s were the CMOS and BiCMOS. The BiCMOS logic family addressed the need of interfacing with CMOS components requiring TTL logic levels yet keeping the improved performance of CMOS. The low voltage derivatives of the CMOS and BiCMOS were becoming more and more available throughout the 1990s to 2000s as the demand for low power consumption and denser devices were growing. The TTL logic family is not used within new designs today, instead CMOS technology can provide an output that is compatible with the TTL standard and it is this reason the Spartan 6 contains the functionality to provide a TTL output without the drawbacks of using TTL architecture.

Comparing the characteristics from a selection of bipolar and CMOS logic families, it is possible to anticipate which family will produce the greater magnitude of EMI during radiated emissions testing. Paying particular attention to propagation delay and supply current, it becomes clear to predict which family will produce the higher level of emissions.

Logic Family	Type	Propagation Delay (ns)	Supply Current (mA) @ Max Spec and Max Vcc
CMOS	LCX	6.5	0.01
	LVX	12.0	0.04
	HC	25.0	0.08
	AC	7.5	0.08
Bipolar (TTL)	FASTr	3.9	75
	FAST	6.5	90
	AS	6.2	90
	ALS	10.0	27

Table 1: A Comparison of Logic Families [26]

The figures detailed in Table 1 indicate that the bipolar families are capable of much faster switching speeds and higher current consumption than the equivalent CMOS families. The FASTr technology records a propagation delay of 3.9ns whereas the CMOS technologies record a delay of 6.5ns - almost half of that of the bipolar family. Comparing the supply current of the LVX and ALS logic type, both exhibiting similar propagation delays, the LVX supply current drawn is at approximately 40µA, whereas the ALS records a supply current of 27mA. From these figures in Table 1, it becomes clear that the TTL family has a higher switching speed than the CMOS equivalent yet it comes with greater power consumption as a result. From this behaviour it is reasonable to expect the higher level of emissions to be produced from the LVTTL logic family than the CMOS equivalents. The ability to control any unnecessary emissions from the overall system will not only reduce the EMI produced it will also deliver a more cost effective system. Reducing characteristics such as the switching speed and power consumption will not only reduce the emissions it will require a smaller power supply.

1.4 Overview of Thesis

The following sections of this thesis detail the research carried out into the radiated emissions produced by the chosen Xilinx Spartan-6 FPGA and the design of the hardware used for testing. Section 2 gives an overview of the PCB hardware specifically designed for this research project and the VHDL code implemented to produce the required signals for testing. An overview of the key hardware blocks, justification for their inclusion and how they potentially impact upon any results gained is included. An overview of the VHDL code used for testing is included to allow for repeatability and to account for the behaviour of the FPGA. The description of the VHDL code covers the key aims of the code and the cores and primitives used for this testing.

Section 3 establishes and validates a test plan, which will ultimately be used to examine the time and frequency domain behaviour the signals produced by the FPGA. Firstly, to validate the test plan a calibrated or 'known' source in the form of a signal generator has been used to illustrate how the edge rate of signals impact the harmonic content recorded. This establishes a practical understanding of how the harmonic content varies from the theoretical expectations. The time and frequency domain measurements are taken through a 50Ω coaxial cable from the measurement instrumentation to the 50Ω output of the signal generator. Section 4 is a theoretical and practical analysis of the harmonic content produced by the signals from the FPGA. This is intended to illustrate and examine the behaviour of the signals and account for any discrepancies or phenomena that occur within the signals produced. The time and frequency domain measurements are taken through a 50Ω coaxial cable from the measurement instrumentation to a SMa connector that is part of the PCB architecture.

Section 5 examines the emissions produced from each of the FPGA I/O driver settings individually. Logic Standard, Drive Strength and Edge Rate are varied one by one to quantify how these settings impact the peak level of harmonics recorded. The measurements are taken through an H-field probe in the near field and record the voltage on the coil of the probe.

Section 6 gives a full overview of all of the radiated emissions measurements taken for each I/O driver settings. The results within section 6 are organised by logic I/O standard, and within each of the standards, a baseline has been stated to quantify the increase or decrease to the peak level emissions produced by the FPGA.

Section 7 delivers the concluding comments on the research project and gives suggestions on further research beyond this project.

Section 0, contains the additional information relating to this project. This is inclusive of the schematics for the PCB designed for this project, the GERBER files used to manufacture the PCB, the VHDL code to program the FPGA and finally the plots of emissions produced from each I/O driver setting.

2 Circuit for Testing - Architecture & Design

Section 2 describes the hardware designed and manufactured for this research project and the VHDL code used for testing. Included within this section is a description of the circuitry designed to obtain the required measurements and the circuitry implemented to make the FPGA functional. The schematic, GERBER files and VHDL are located in the Appendix 1, Appendix 2 and Appendix 3 respectively.

2.1 Hardware Design Overview

The PCB shown in Figure 13, has been designed with the overall aim of obtaining radiated emissions measurements when varying the I/O driver settings and standards. The hardware present on the board has been kept to a minimum to restrict any emissions from surrounding circuitry.

Figure 12, illustrates a conceptual overview for the PCB hereinafter referred to as the MSCR-001 PCB stating the architecture of the board.

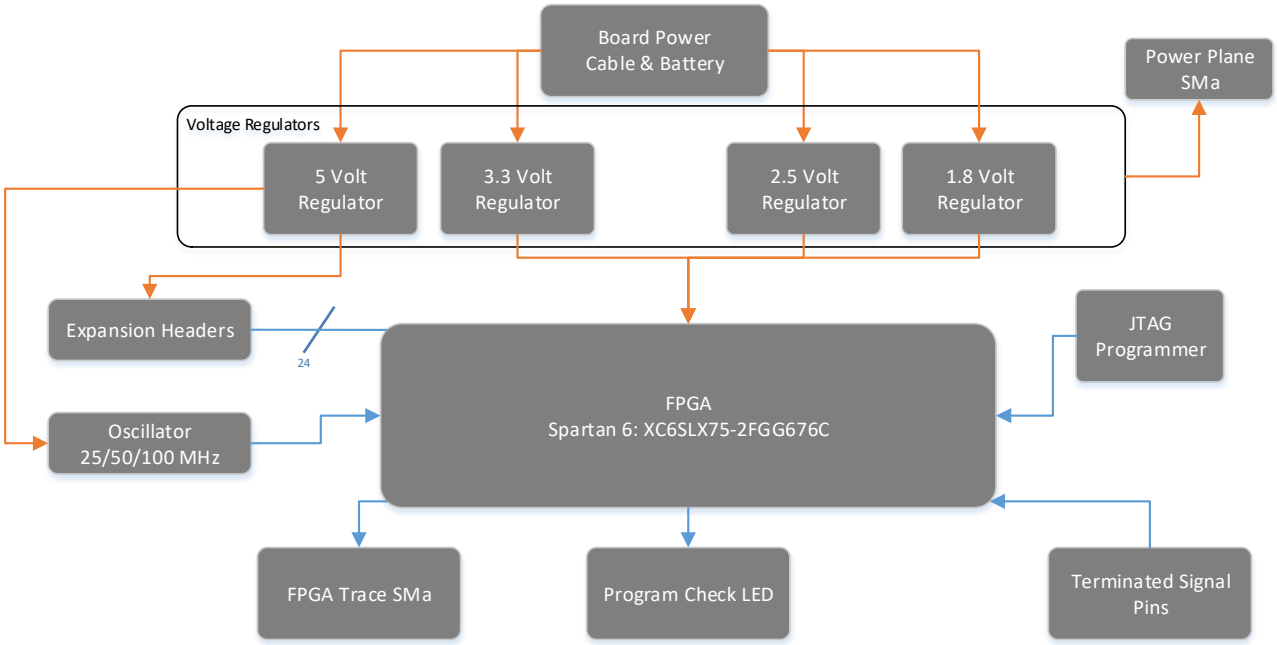


Figure 12: MSCR-001 Hardware Architecture

The chosen FPGA for this research is the Spartan 6: XC6SLX75-2FGG676C from Xilinx. The device is a 676 pin Ball Grid Array (BGA) package device and is widely used within the engineering industry for such applications as Audio and Digital Signal Processing, meaning any results gained would be pertinent to current digital system designs. Xilinx have a substantial array of devices available that can be used with readily available design tools such as the Xilinx ISE Design Suite and excellent implementation support through their online datasheets.

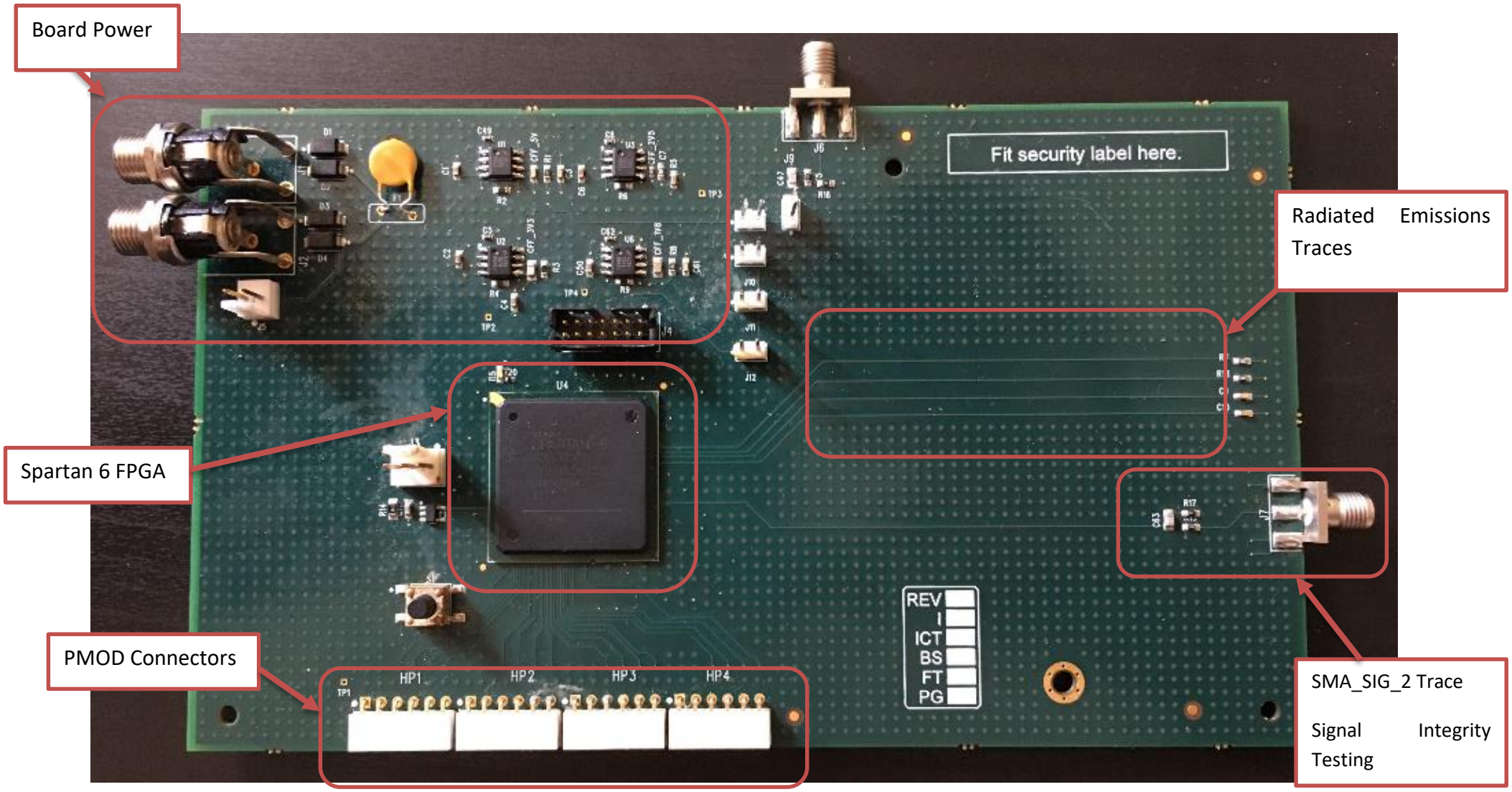


Figure 13: MSCR-001 PCB Overview

2.1.1 Board Power

The input voltage to the PCB is designed to be +12 Volts DC allowing the board to be battery powered (J5) or powered from an AC/DC mains supply (J1 & J2) shown in Figure 14. The option to power the PCB by AC/DC mains supply allows for constant supply during development testing and the option to power the PCB via battery will allow the mains cables to be removed during radiated emissions testing. Mains and I/O cables have been identified as one of the potential antenna for radiating Electromagnetic Interference [28], [29], this functionality ensures that if the mains cables conduct EMI or act as an antenna to radiate emissions they can be removed entirely and the PCB powered via a battery.

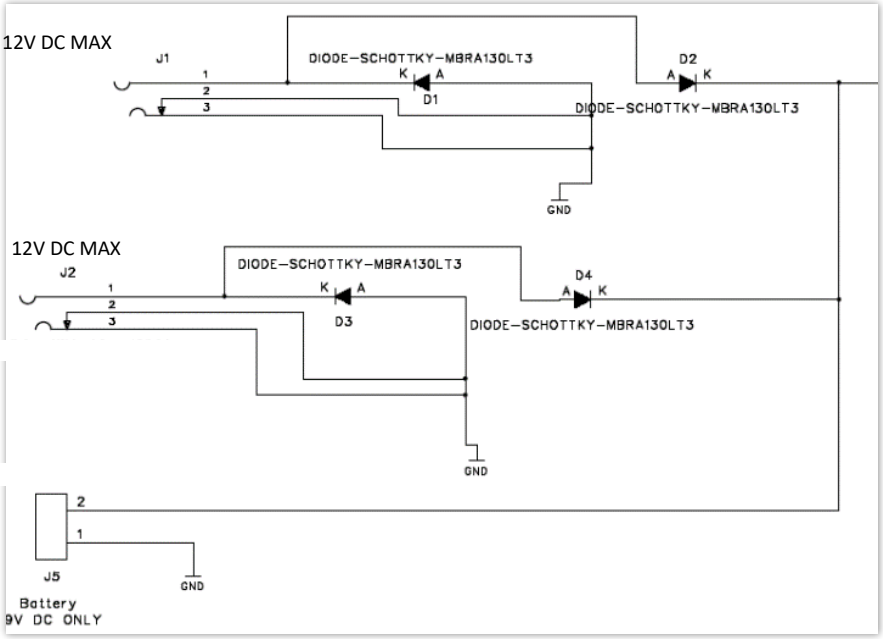


Figure 14: MSCR-001 Board Power

2.1.2 Voltage Regulators

As with many systems containing integrated circuits of this nature, an array of voltages are required for the functionality of the FPGA. The use of other ICs within the circuit that could produce additional EMI needs to be avoided wherever possible. Ouyang *et al* [30] identify switching regulators as a potential source of EMI with the high and low side power MOSFTETs being one of the major sources of EMI. So with the goal of minimising EMI from the surrounding hardware, a linear voltage regulator has been chosen to achieve the voltage derivations required. Linear regulators could be considered an inefficient way to achieve voltage derivations in larger systems. However, for the purpose of this research achieving the required voltages without compromising the emissions results taken is paramount. The on-board linear regulators provide 5 volts, 3.3 volts, 2.5 volts and 1.8 volts. The 5 volts regulator is used to supply the Peripheral Module (PMOD) connectors to allow expansion beyond the MSCR-001 PCB and the oscillator IC. The remaining three voltage regulators are used to supply the FPGA - with the 3.3 volts powering the I/O banks, the 2.5 volts powering the programming interface and the remaining 1.8 volts is used to power the core of the FPGA.

2.1.3 Expansion Headers

A potential for expansion beyond the hardware committed to the PCB is present in the form of four PMOD connectors. This expansion approach is used extensively throughout demonstration boards and may prove to be useful for any additional circuitry that may be required. Each PMOD connector has two pins allocated to supply +5 volts and 0 volts return generated on the MSCR-001 PCB. This will allow further expansion past this board without the need for additional external power supplies.

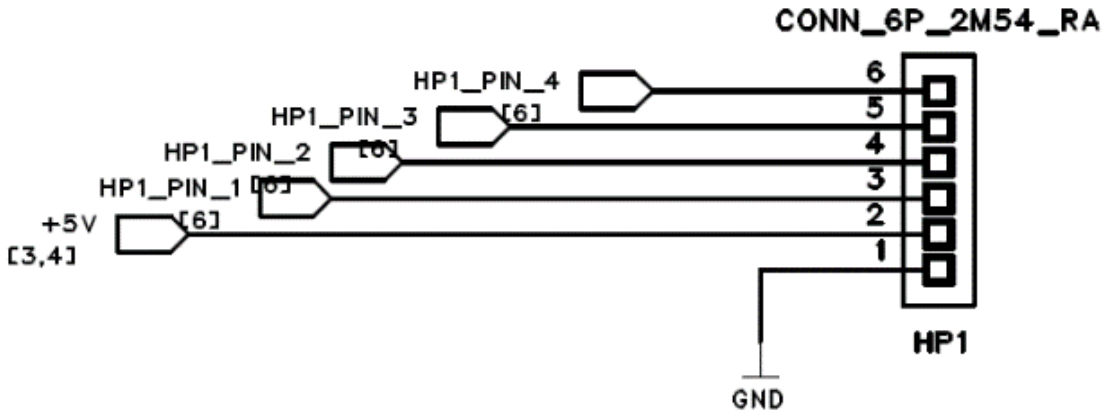


Figure 15: MSCR-001 Expansion Header

Referring to Figure 15, the remaining four pins on the PMOD connector have been allocated to I/O pins on the FPGA. The PMOD connectors have been labelled HP1, HP2, HP3 and HP4 the individual pins HP1_PIN_1 to HP4_PIN_4. They provide access to 16 I/O pins located in bank 2 on the FPGA as illustrated in Figure 16.

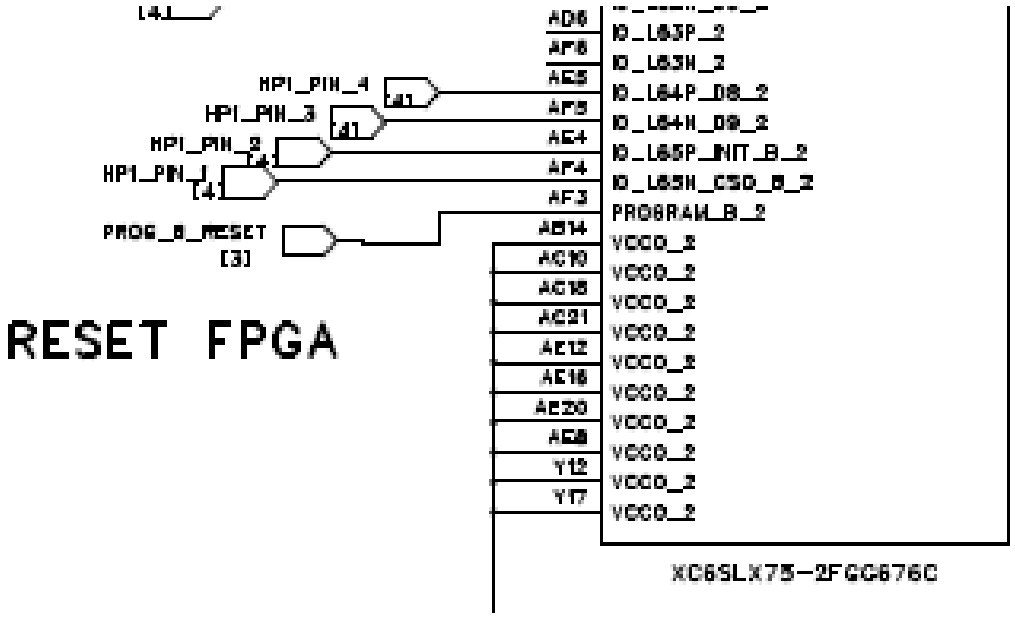


Figure 16: FPGA Expansion Port Nets

2.2 Measurement Architecture

The measurement architecture on the PCB has been designed to allow measurements to be taken without the need for additional circuitry and to allow the FPGA to drive circuitry, which will not interfere with any emissions measurements gained. All measurement traces have been routed to have an impedance of 50Ω by controlling the track widths on the PCB.

The key elements of circuitry used for measurements on the MSCR-001 PCB are:

- Signal Integrity Measurement Traces
- Radiated Emissions Traces

2.2.1 Signal Integrity Measurement Traces

The first of the measurement traces shown in Figure 17, and connects to I/O pin V26 of the FPGA for examination of the signals under the various I/O driver settings. The trace includes a DC blocking capacitor (C1), L-attenuator (R1 & R2) and finally terminates with an SMA connector to allow connection to the measurement instrumentation.

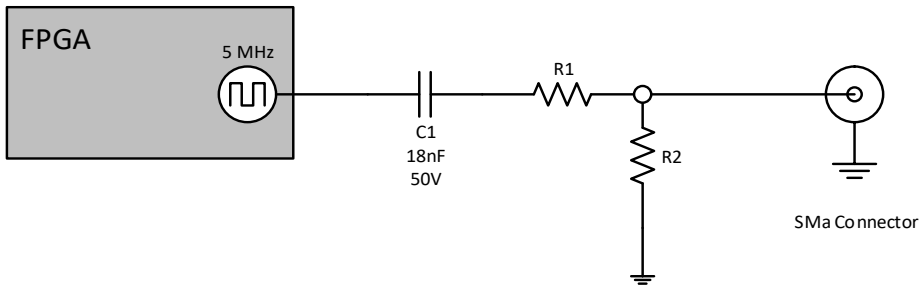


Figure 17: SMA FPGA I/O Connection

The second of the measurement traces shown in Figure 18 provides access to the power planes on the PCB to monitor noise as a result of the I/O settings within the FPGA. Power supply switching noise can be attributable to such phenomena as clock jitter [19]. Jumpers J8 – J12 allow selection of connection to each of the power planes, and the SMa connector is designed to interface with either the oscilloscope or spectrum analyser.

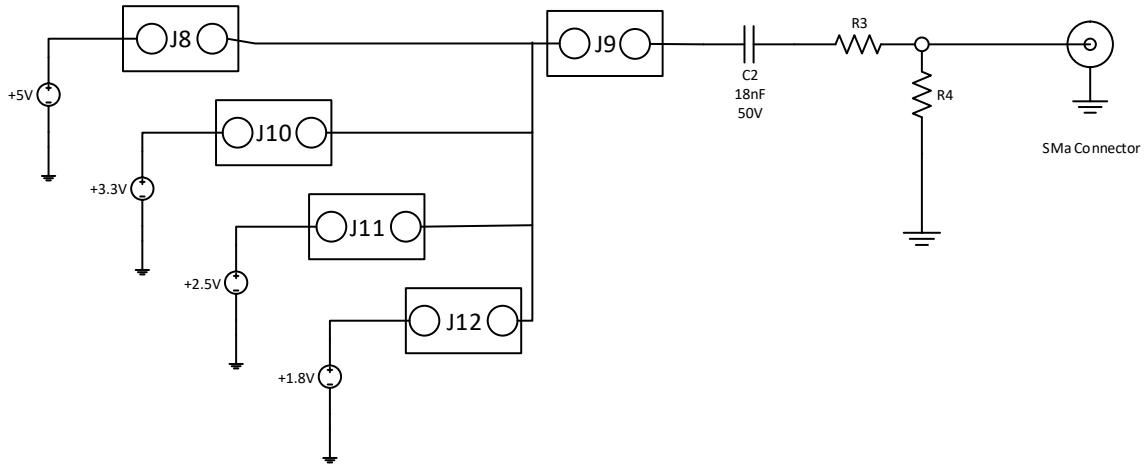


Figure 18: SMA Power Plane Connection

2.2.2 Measurement Instrument Protection

The instrumentation protection is firstly in the form of a DC blocking capacitor, which will prevent any DC voltages damaging the front end of the measurement instruments. The second is a 10:1 attenuator which has been added to lower the potential of any voltages or transients to the front end of the instruments should they be able to bypass the DC blocking capacitor.

2.2.3 DC Blocking Capacitor

Using Equation 4, the DC blocking capacitor has been chosen to have a low reactance value at the 5MHz source signal frequency. A capacitor behaves like a short at higher frequencies and open circuit at lower frequencies.

$$X_c = \frac{1}{2\pi f C}$$

Equation 4: Capacitor Reactance Formula [24]

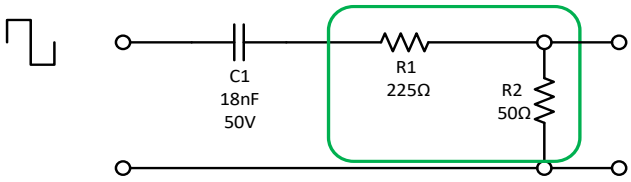


Figure 19: DC Blocking Capacitor

2.2.3.1 Capacitor Reactance

The reactance value X_c has been chosen to be less than 2 Ohms at the source signal frequency. Rearranging the Equation 5 to make C the subject:

$$C = \frac{1}{2\pi \times 2 \times (5 \times 10^6)} = 15.9\ _{nF}$$

Equation 5: Transposed Capcitor Reactance Equation

A value of 18nF has been used, as this is the nearest possible value of commonly available capacitors.

2.2.3.2 Capacitor ESR & ESL

Including a DC blocking capacitor introduces along with it Equivalent Series Resistance (ESR) and Equivalent Series Inductance (ESL). These properties of the capacitor will have an impact on the signals recorded by the spectrum analyser. The ESR is dependent upon the technology of the capacitor used. Capacitors such as wet tantalum can have ESR values in the order of 5Ω. This additional series resistance will cause attenuation to the peak levels of the harmonics recorded as the resistance will cause a voltage drop across it. To minimise this effect, the technology of the DC blocking capacitor is ceramic, as this technology possesses one of the lowest ESR values for capacitors.

The ESL opposes the reactance of a capacitor and varies with frequency. As the frequency increases, so does the ESL value and ultimately the impedance of the capacitor, as shown in Figure 20. The harmonics of the 5MHz clock signal used will experience a higher ESL and impedance value than the fundamental frequency. This increasing impedance will attenuate the peak value of emissions recorded at these harmonic frequencies.

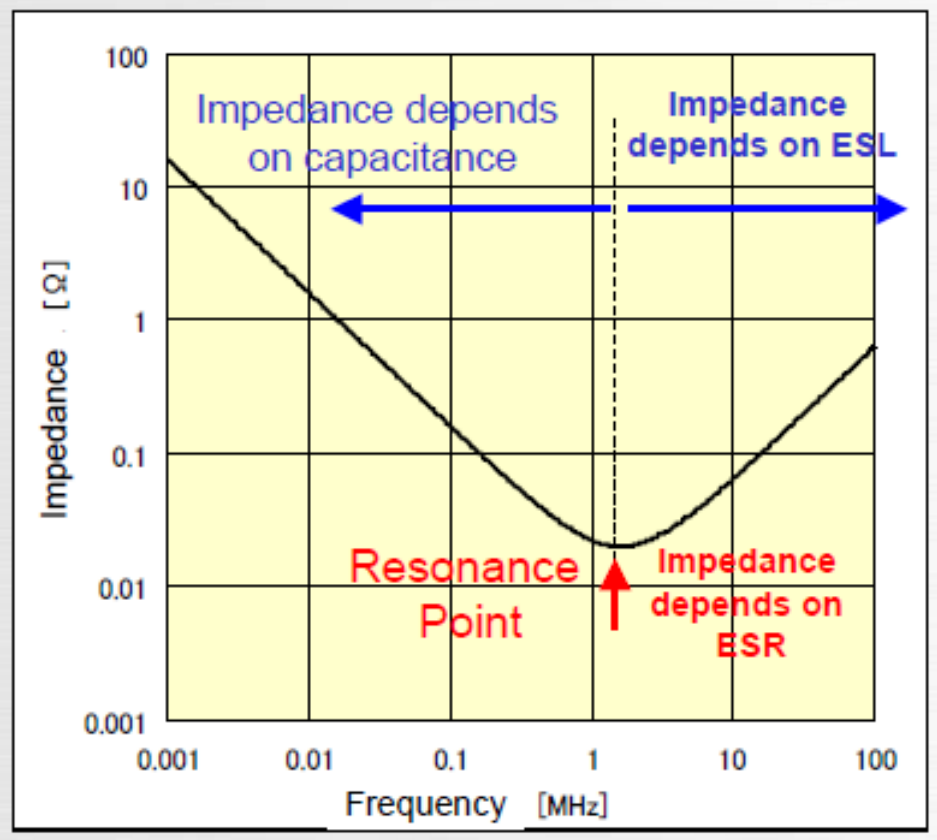


Figure 20: DC Blocking Capacitor Impedance [31]

2.2.4 Attenuator

The attenuator is designed to reduce the signal potential by a ratio of 10:1. The chosen configuration is an L- attenuator, as illustrated below, which acts as a voltage divider. The components values have been calculated using Equation 6.

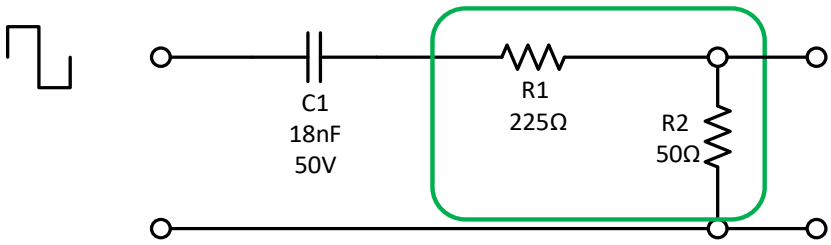


Figure 21: Attenuator Circuit

The values of the resistors have been calculated to take into account that when the PCB trace is terminated with the 50Ω measurement instrument, the attenuation that occurs is 10:1.

$$V_{out} = V_{in} \frac{R_2}{R_1 + R_2}$$

Equation 6: Voltage Divider Equation [24]

2.2.5 Capacitor Attenuation

As identified within section 2.2.3, including the DC blocking capacitor in series with the PCB trace will cause some attenuation of the signal produced by the FPGA. The magnitude of the attenuation will be predominantly influenced by the attenuator included within the circuitry however the capacitor will introduce additional attenuation to the signal that is being produced by the FPGA. When calculating the additional attenuation that the capacitor introduces into the signal path the reactive elements such as the parasitic inductance and capacitance must be taken into account. These values replace the capacitor with a series RLC circuit with the values shown in Figure 22.

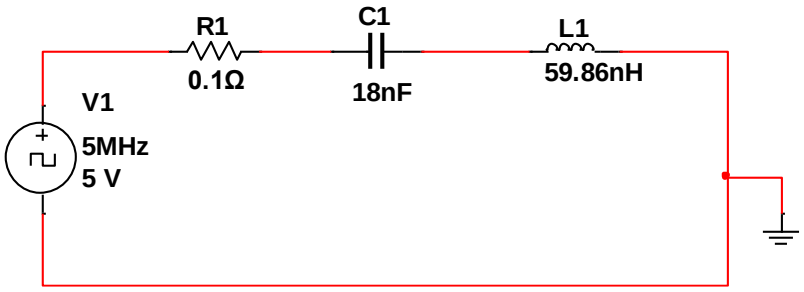


Figure 22: Capacitor Equivalent Circuit

The total impedance of the capacitor is takes into account the reactance of the capacitor (X_C) and inductor (X_L) and the equivalent series resistance (ESR) of the capacitor.

$$|Z| = \sqrt{(Req^2) + (|X_L - X_C|^2)}$$

Equation 7: Capacitor Series Impedance

From the datasheet the value of R_{EQ} = 0.1Ω so negligible for the purpose of this calculation. The capacitive and inductive reactance is calculated as follows. The capacitive reactance of the 18nF capacitor is obtained using Equation 4. With a fundamental frequency of 5MHz and a capacitance value of 18nF the capacitive reactance is;

$$X_c = \frac{1}{2\pi \times (5 \times 10^6) \times (18 \times 10^{-9})} = 1.768\ \Omega$$

Equation 8: Capacitive Reactance Formula

The inductive reactance obtained from the point where $X_C = X_L$, this transposes to give an inductance L of 59.86 x10^{-9}.

$$X_L = 2 \times \pi \times f \times L = \ 1.768\ \Omega$$

Equation 9: Inductive Reactance Formula

As observed from the Equation 8 & 10 detailed above the overall impedance of the capacitor varies with frequency, as the frequency increases the capacitive reactance reduces and the inductive reactance increases. This will add to the series resistance R_1 in Figure 21 that forms part of the voltage divider attenuator as shown in Figure 23.

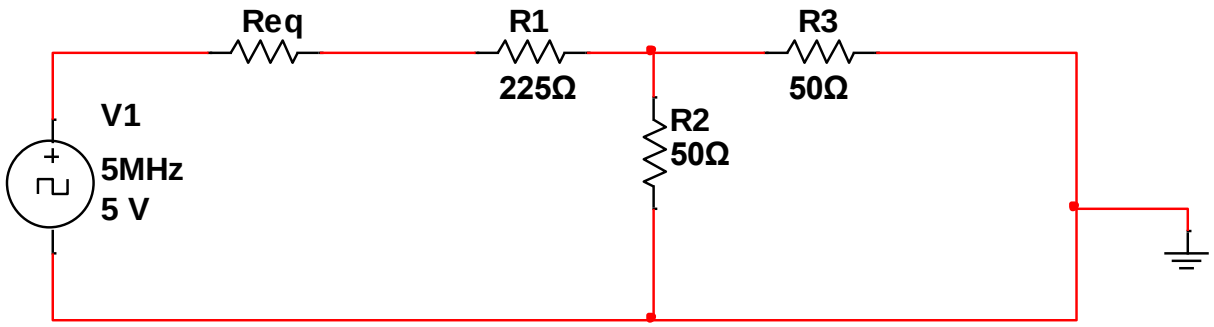


Figure 23: Attenuator Equivalent Circuit

As the frequency of the harmonics increases the value of R_{eq} increases along with it. The voltage response of the circuit is shown in Figure 23. The graph predicts the input voltage to the spectrum analyser of a square wave of 5V and a frequency range of 5MHz to 1GHz. This will impact the signals that are produced by the FPGA by attenuating harmonics of the periodic square wave increase.

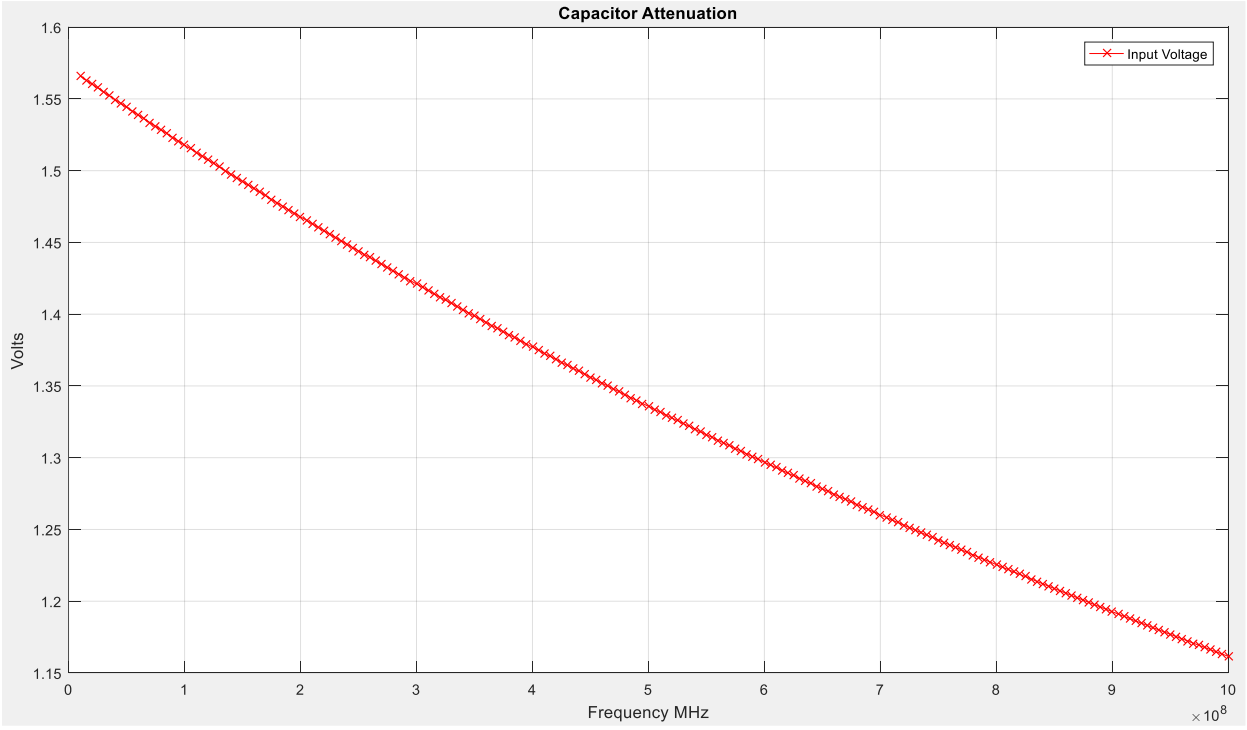


Figure 24: Capacitor Attenuation

2.2.6 Emissions Traces

Finally, for the measurement architecture, four resistive loads can be driven from individual FPGA I/O pins. The configuration illustrated in Figure 25 will be used for the radiated emissions testing, giving a repeatable testing arrangement. The traces are designed to be a transmission line with a characteristic and termination impedance of 50Ω to prohibit reflections on the line. The termination impedance has been calculated using Equation 10 - Z_{TERM} is the 50Ω termination resistance and Z_0 is the 50Ω characteristic impedance of the transmission line. Any reflections on the transmission line will introduce additional EMI into the spectrum giving results that will not be solely representative of EMI produced by the FPGA I/O drivers.

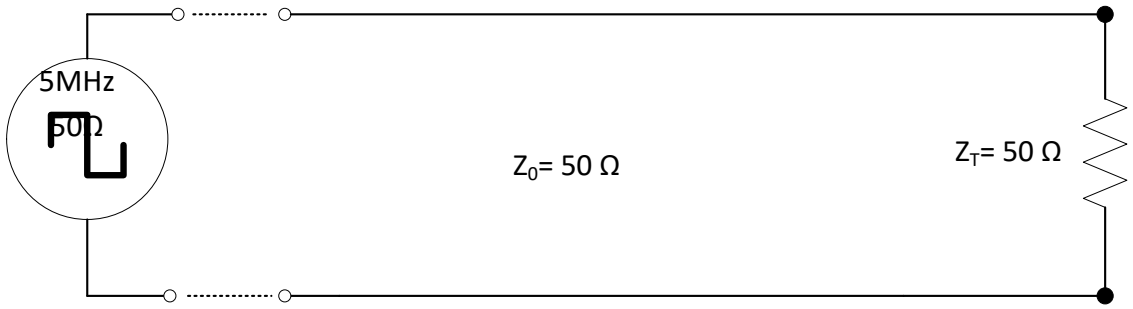


Figure 25: Terminated I/O Signal pins

$$\rho = \frac{Z_{TERM} - Z_0}{Z_{TERM} + Z_0}$$

Equation 10: Transmissions Line Reflection Coefficient Formula [32]

2.3 VHDL Code Design

The testing of the MSCR-001 PCB has been divided into two sections - an analysis of a selection of signals produced by the FPGA, and the peak level emissions produced under the various I/O driver settings. The VHDL code written for this project has been designed to produce the required signals for this testing and with as much commonality of code between the two testing phases as possible. The FPGA is required to produce a 5MHz clock signal, and output this to drive the circuitry shown in Figure 17 and Figure 25. To achieve this the FPGA receives a 10MHz clock signal (MCLK) from an external on board oscillator and produces a 5MHz clock output. This is achieved by using functional blocks of code that Xilinx provide in the form of cores and primitives. This will ensure that the VHDL code used is repeatable and utilises minimal resources within the FPGA. The VHDL code is intended to be representative of an implementation that would be used in a real world application using these primitives and IP (intellectual property) that is readily available within the Spartan-6 device. The VHDL code written for this project is located in Appendix 3.

Xilinx FPGAs contain many cores and primitives to assist with the digital design process such as the digital clock manager and dual data rate flip-flops. These cores and primitives can be used as functional blocks to provide an operation within the design and will provide a repeatable set of VHDL code for this testing. The intent of the code is to utilise minimal logic tiles of the FPGA so that the emissions recorded will be representative of the I/O standards and settings, and not the additional internal workings of the FPGA that have come about from inefficient design.

2.3.1 MSCR-001 VHDL Cores & Primitives

To provide the functionality required for the testing the following key cores and primitives have been used;

- DCM – Digital Clock Manager
- BUFGMUX (Clock Multiplexer)
- ODDR (Dual data rate peripheral)

2.3.2 DCM – Digital Clock Manager (FREQ_CHANGE)

The digital clock manager (DCM) is a primitive in Xilinx FPGAs and is used to implement such functions as delay locked loops, digital frequency synthesis or a digital clock spread spectrum. The main benefit to using this primitive within the FPGA is that it will provide a repeatable means of generating the required clock frequency for testing. DCMs are fundamentally used within digital designs to handle the clock management as they have the added benefit of removing such timing issues as clock skew. For the application of this code, the DCM has been implemented to receive an external clock signal of 10MHz (MCLK) and generate two clock frequencies of 5MHz and 100 MHz for radiated emissions testing. Figure 26 illustrates the high level block overview of the DCM available within the Spartan-6 FPGA.

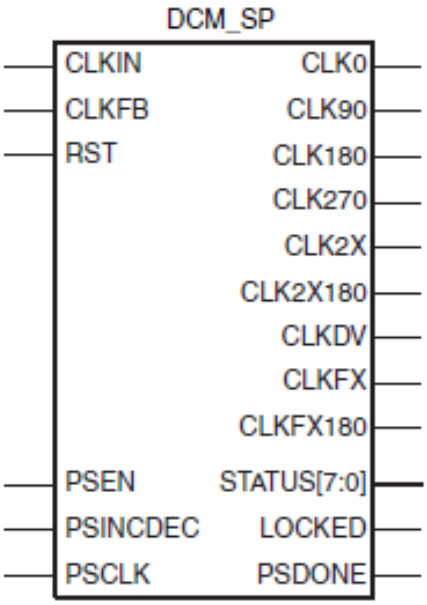


Figure 26: DCM Primitive [33]

2.3.3 BUFGMUX (CLOCK_MUX)

The BUFGMUX is a 2 to 1 multiplexer, shown in Figure 27, the select line 'S' allows a glitch less transition between different clocks present within the system [33]. This primitive will allow for the selection of which clock signal will be used for the radiated emissions testing.

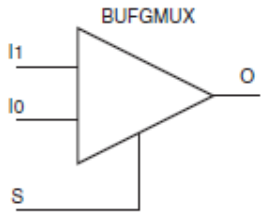


Figure 27: BUFGMUX Primitive[33]

2.3.4 ODDR2 (HP2_PIN_2 & SMA_SIG2)

The Output Dual Data Rate (ODDR) shown in Figure 28 is an element within the FPGA designed for communication with peripherals. The ODDR2 allows a clock signal to be output from the FPGA with no noise or timing issues and is often used for source-synchronous communication. Source-synchronous communication is used for various applications within engineering such as the transmission of digital audio where a clock signal is sent along with data. Due to the internal workings of the FPGA, the clock distribution network is physically separate from the data network and connecting this to the I/O pins would cause significant noise issues, something that needs to be actively avoided as this could interfere with results gained with additional EMI. The ODDR2 primitive within the FPGA allows the clock network to be connected to the I/O eliminating these noise issues, which for the purpose of this research allows the signals to be outputted for testing without compromising results.

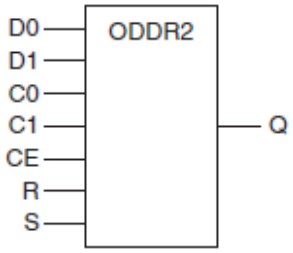


Figure 28: ODDR2 Primitive [22]

2.4 VHDL Code Overview

Figure 29 illustrates the overview of the RTL (Register-Transfer Level) schematic of the VHDL code written to produce the required signals for testing. To the left of the RTL schematic it shows the master clock being received by the FPGA and inputting to the DCM. The two outputs of the DCM are the 5MHz and 100MHz clock signals that input to the BUFGMUX. The select line is connected to HP1_PIN_1 of the PMOD connectors so allows for selection between the two clock signals, the default signal is the 5MHz clock. The 5 MHz clock signal is then outputted to the SMA_SIG_2 and TRACE_1 pin for signal integrity analysis and radiated emissions testing. During the radiated emissions testing the output to SMA_SIG_2 has been removed to ensure that additional EMI is not recorded from this trace.

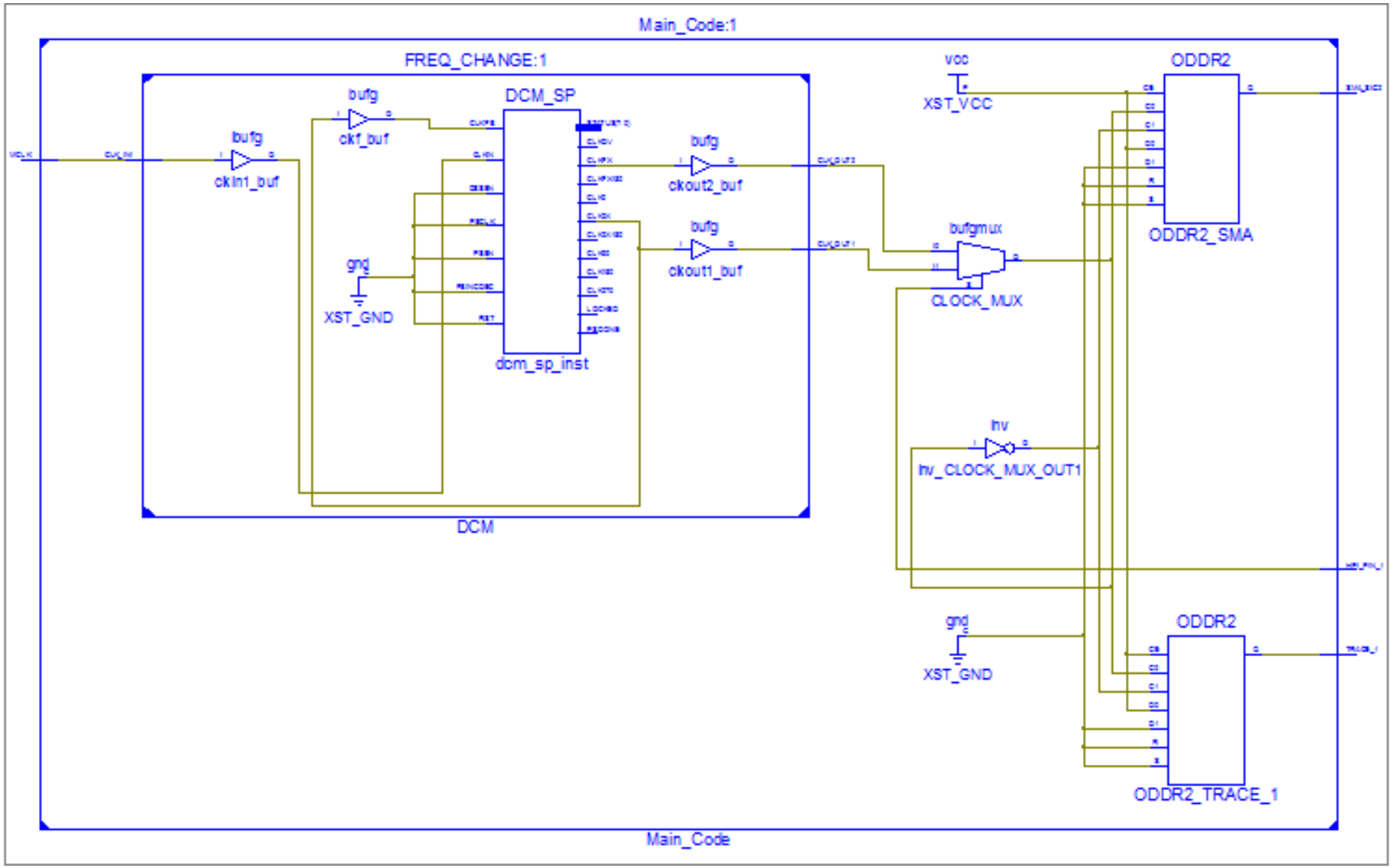


Figure 29: VHDL Code RTL Schematic

3 Signal Testing – Signal Generator

Section 3 examines the behaviour of periodic signals in both the time and frequency domain and introduces the method of analysing and assessing the results gained. The signals used within this section are from a signal generator to examine the harmonic content of signals with varying edge rates.

The test plan outlined is what will be used to examine the signals from the MSCR-001 FPGA board. Initially testing with a signal generator gives a greater degree of confidence in any results gained from the FPGA, if an understanding of the expected performance in the time and frequency domain is gained. This testing is split between two sets of signals, firstly two signals having a very large difference between their edge rates and secondly four signals, which closely represent those that will be produced by the FPGA.

3.1 Testing Overview

The purpose of this testing is to illustrate how the harmonic content observed within the frequency spectrum changes between signals that possess differences in their edge rates. Using a calibrated source such as a signal generator to provide the signals, it will give a greater confidence in any results recorded.

The signal generator testing will produce results that closer represent the Fourier theory than is likely to be produced from the FPGA board due to the component properties present on the PCB. The testing is split into both an analysis of the time and frequency domain and will give an overview of how the harmonic content presents itself within the frequency domain from properties of the signal obtained within the time domain. The time domain analysis identifies the properties of the clock signal that contribute to the amplitude of the harmonics. The practical frequency domain analysis has been carried out using a spectrum analyser to identify the harmonic content of the signals produced by the signal generator. From this data, the peak level of harmonic content has been recorded to allow for comparison between signals. Finally, the theoretical calculations of the frequency domain behaviour have been obtained to allow for comparison to the practically obtained data.

The signals that will be used for this testing are detailed in Table 2 and the order of testing will be to examine and compare the harmonic content of signals 1 and 2, and then signals 3 to 6. Comparing signals 1 & 2 will give an illustration to what extent the edge rate of a signal can impact the amplitude of the harmonics between two signals with a drastically different rise times. Signals 3 – 6 give a more realistic depiction of the signals that will be produced by the FPGA through their array of I/O driver settings.

3.1.1 Source Signals

Signal Number	Signal Type	Frequency	Amplitude	Duty Cycle	Rise Time
1	Square Wave	1 MHz	5 V	50%	10 ns
2	Triangle Wave	1 MHz	5 V	50%	400 ns
3	Square Wave	1 MHz	8 V	50%	10 ns
4	Square Wave	1 MHz	8 V	50%	20 ns
5	Square Wave	1 MHz	8 V	50%	40 ns
6	Square Wave	1 MHz	8 V	50%	80 ns

Table 2: Signal Generator Source Signals

3.1.2 Time Domain Analysis Test Setup

The time domain analysis of the source signals will provide the signal properties required to carry out a theoretical Fourier analysis using

Equation 1. This testing will also be used as a visual inspection to examine whether the waveform is exhibiting any interference such as ringing or reflections that could hinder any of the results gained. The time domain results will be obtained using an oscilloscope through the testing arrangement shown in Figure 30 and Figure 31.

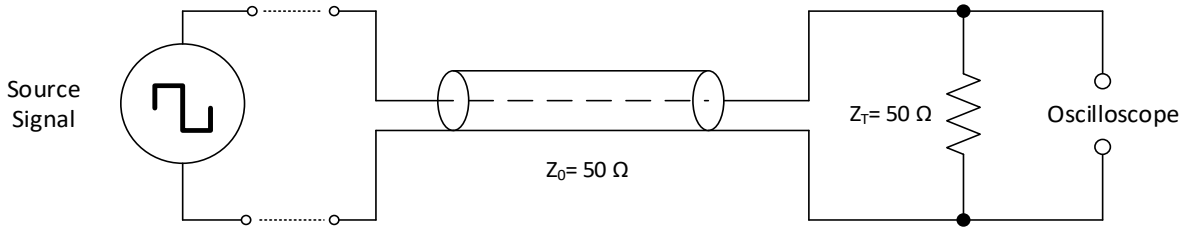


Figure 30: Time Domain Test Setup - Signal Integrity Testing

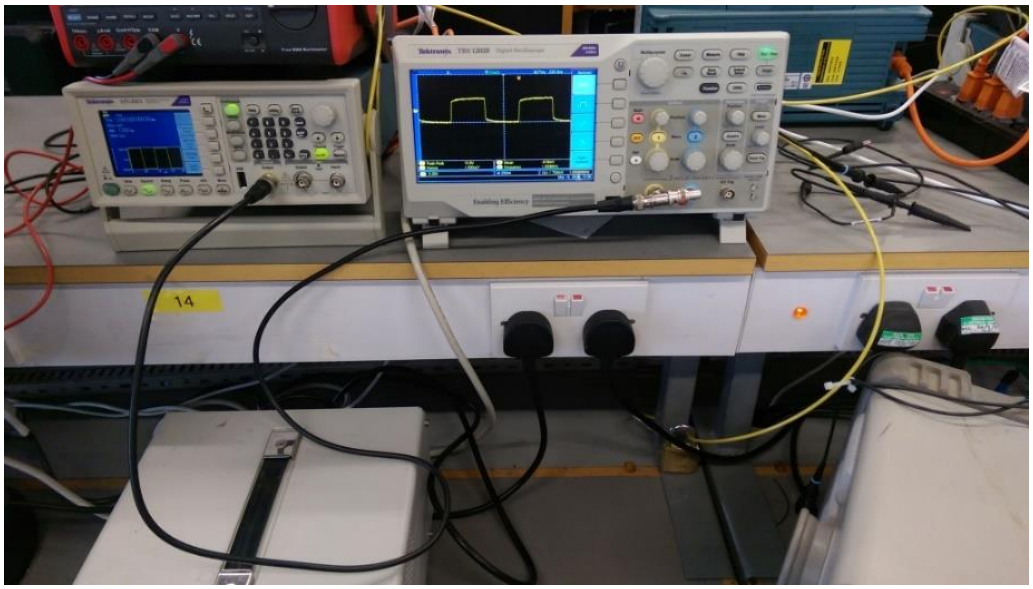


Figure 31: Time Domain Testing Photograph - Signal Generator

A signal generator provides the source signal, the transmission medium to the oscilloscope is via a 50 Ω coaxial cable with a BNC Connector either side. The transmission line is terminated with a 50 Ω termination resistor to prohibit any reflections. The theory for this design is based on the reflection coefficient formula for transmission lines as detailed in Equation 10. The specification of the oscilloscope has been chosen as be able to record any overshoot or ringing on the peaks and troughs of the signal. An oscilloscope with a bandwidth or sample rate too low and the signals will appear rounded and more sinusoidal than the expected square wave hiding any phenomena that could introduce additional harmonics to the spectrum. All testing has been carried out using the calibrated equipment in the University of York 4th Floor teaching laboratory.

3.1.2.1 Time Domain Testing Equipment

The test equipment used for the time domain analysis is specified below in Table 3, with a photograph of the testing arrangement shown in Figure 31.

Equipment	Specification/Details
PC with ARB express software	ARB express software is used to generate the required signals for analysis
USB B – USB A Cable 1M	USB B to USB A cable.
Tektronix AFG 2021 Signal Generator	1 uHz-20 MHz Range 50 Ohm Output Impedance
50 R Coax Cable	BNC to BNC Cable
BNC T-Piece Connector	N/A
50 Ohm Termination	BNC Connector 50 Ohm 4 GHz Max Frequency
Oscilloscope: Tektronix TBS1202B	2.5 GS/s 400 MHz

Table 3: Signal Generator Time Domain Analysis Test Equipment

3.1.3 Frequency Domain Analysis

The frequency domain analysis will obtain the practical measurements for the harmonic content of the signals listed in Table 2 using a spectrum analyser and the configuration shown in Figure 32.

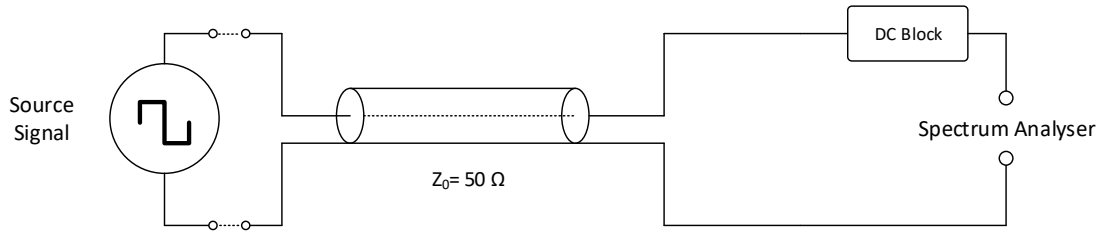


Figure 32: Frequency Domain Test Setup Signal Integrity Testing

The same signal source and transmission medium has been used in the form of a 50Ω coaxial cable. The 50Ω termination has been removed due to the input impedance of the analyser being 50 Ω. The DC block illustrated in Figure 32 is used to offer some level of protection to the front-end of the spectrum analyser.

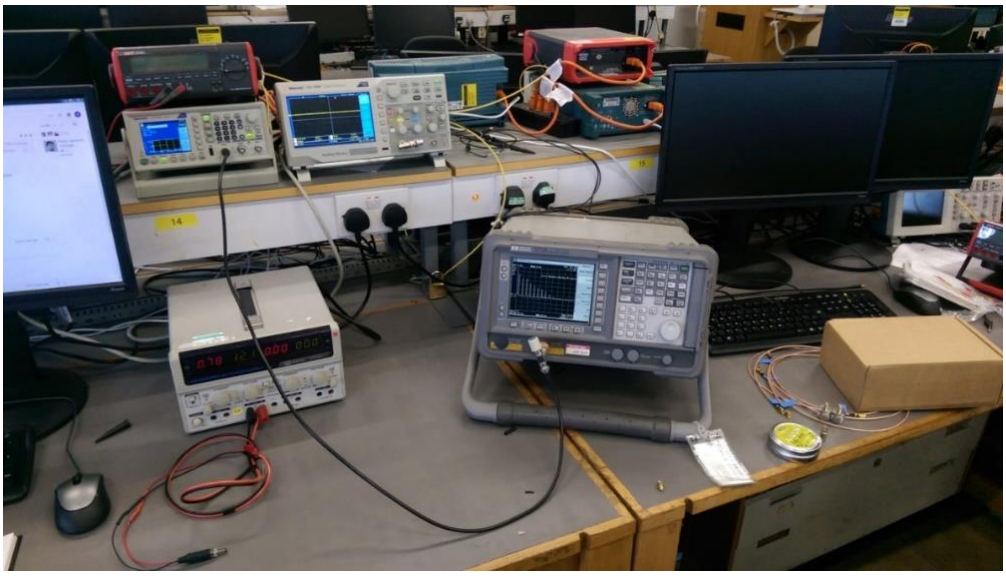


Figure 33: Frequency Domain Testing Photograph - Signal Generator

3.1.4 Results Processing MATLAB

The frequency domain results obtained from the spectrum analyser have been processed using MATLAB, to establish a 'peak level' of harmonic content or peak emissions produced. The same method has been used for identifying the peak levels of radiated emissions and harmonic content produced by the MSCR-001 PCB. The MATLAB code has been split into three individual scripts to process the results in an organised and controlled manner.

The first of the MATLAB scripts shown in Appendix 4 originally written by Tom McMurray and modified by Dr John Dawson is used to validate the input signal to ensure that the data is in a format that the code can read and process correctly. Once the data has been read in the code then identifies the maxima and minima of the data based on the positive and negative slopes before and after a data point.

The second script written by John Dawson shown in appendix 5 analyses all of the maxima and minima recorded and removes the minima from the data array by setting including the condition for a minimum gap between maxima and a minimum fall between maxima. It is the remaining maxima that is being used as the 'peaks' to compare the harmonic content or emissions recorded between signals and I/O driver settings.

Finally the third script given in Appendix 6 process the data for comparison and plots this comparatively to allow an analysis of the recorded data obtained from the different driver settings.

3.1.4.1 Test Equipment & Setup

The test equipment used for the time domain analysis is specified below in Table 4, with a photograph of the testing arrangement shown in Figure 33.

Equipment	Specification
PC with ARB express software	ARB express software is used to generate the required signals for analysis
USB B – USB A Cable 1M	USB B to USB A cable.
Tektronix AFG 2021 Signal Generator	1 uHz-20 MHz Range 50 Ohm Output Impedance
50 R Coax Cable	BNC to BNC Cable
BNC T-Piece Connector	50 Ohm
50 Ohm Terminator	BNC Connector 50 Ohm 4 GHz Max Frequency
Spectrum Analyser: HP E411B	Frequency Range: 9KHz – 1.5 GHz Max Voltage: 100V DC

Table 4: Signal Generator Frequency Domain Test Equipment

3.2 Signal 1 & 2 Time and Frequency Domain Results

Signals 1 & 2 offer the greatest difference to their rise times, so this will give an exaggerated example of how the edge rates of a signal can affect the harmonic content. The time domain results of signals 1 & 2 are illustrated below in Figure 34 & Figure 35 respectively, with the properties of those signals detailed in Table 5.

3.2.1 Time Domain Analysis

Figure 34: Sig Gen Signal 1 (Square Wave)

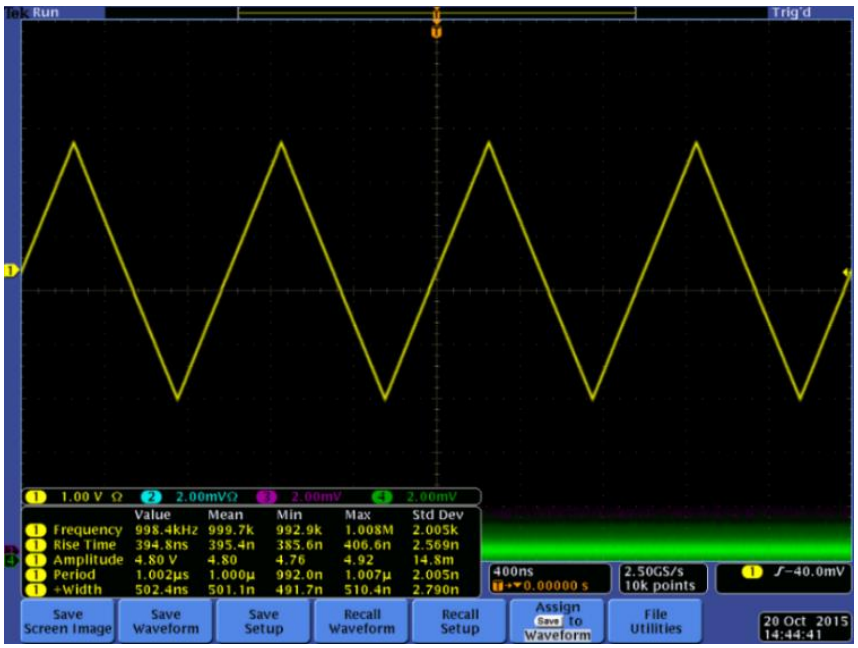


Figure 35: Sign Gen Signal 2 (Triangle Wave)

Measured Attribute	Symbol	Signal 1	Signal 2	Prefix
Rise Time	tr	10.66	394.8	nS
Pulse Period	T	1000	1000	nS
Pulse Width	pw	500	502.4	nS
Amplitude	A	4.8	4.8	V
Frequency Breakpoint	N/A	29.86	0.8	MHz

Table 5: Sig Gen Signals 1 & 2 Results

Observing the time domain representations of signals 1 and 2 shows that there is no visible interference to the signals such as reflections or ringing. The rise time of Signal 1 is approximately 10ns, when in comparison the rise time of Signal 2 is approximately 400ns almost 40 times slower. The two frequency domain behaviours of these signals should be significantly different and the disparity between the harmonic content visible without much detailed analysis.

3.2.2 Frequency Domain Analysis

The harmonic content of Signal 1 shown in

Figure 36 has harmonic peaks past the observed frequency range carrying on past the 100MHz region. The frequency domain behaviour of Signal 2 shown in Figure 37 is drastically different in terms of the harmonic content. The amplitude of the harmonic peaks has decayed to a level that is below the noise floor and no longer observable around the 40MHz region. This drastic reduction to the harmonic amplitude means that a signal with a slower edge rate will have less harmonics at an amplitude that is likely to interfere with surrounding circuitry or cause failures to radiated emissions testing. From the Fourier series, a square wave signal has an

infinite number of harmonics it is just the amplitude of those harmonics that is determined by the signal properties as detailed in Equation 1.

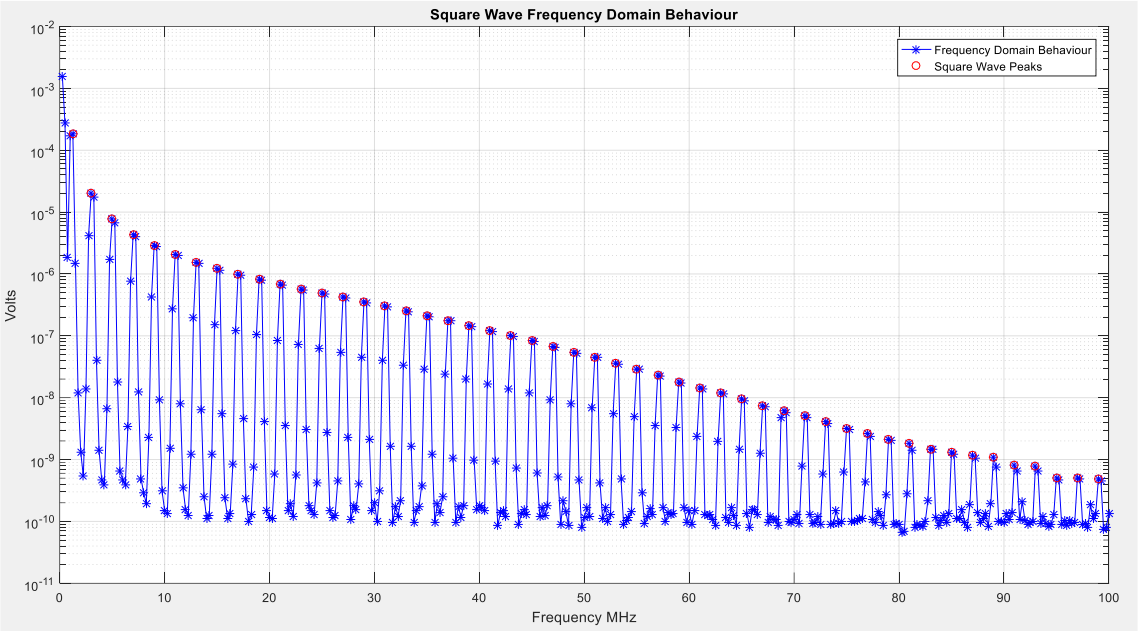


Figure 36: Signal 1 (Square Wave) - Frequency Domain Response

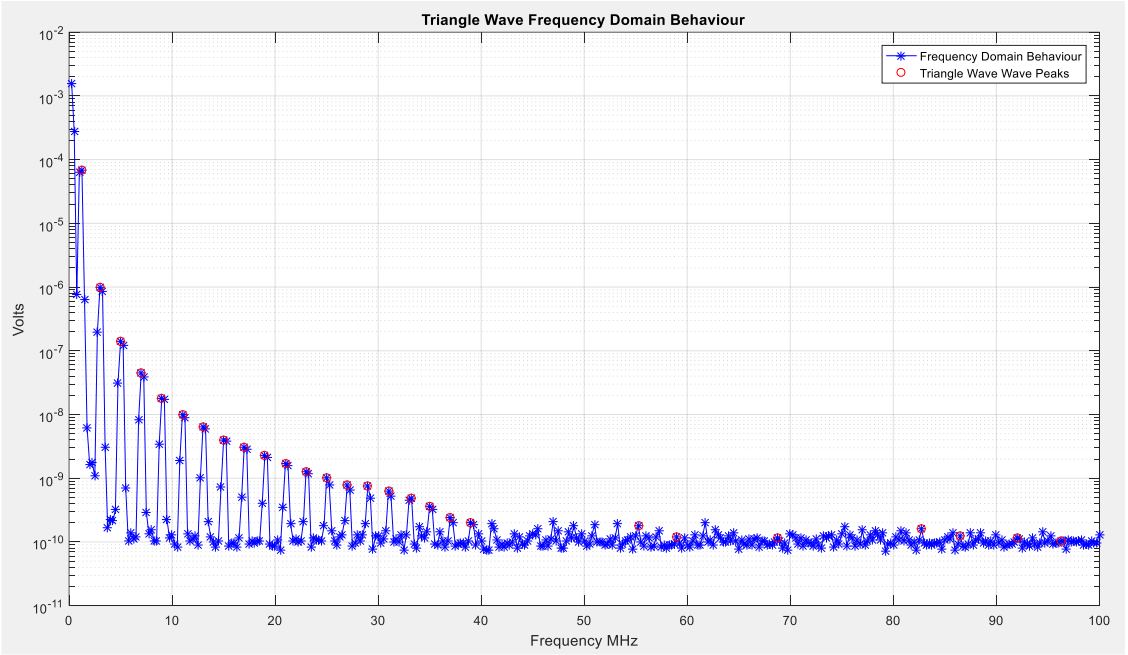


Figure 37: Signal 2 (Triangle Wave) - Frequency Domain Response

3.2.2.1 Signal 1 & 2 Peak Harmonics Comparison

From identifying the peaks harmonics recorded of each frequency domain plots it is clear to see that the traces are drastically different in their peak harmonic levels. The comparative plot of Signal 1 (blue trace) and Signal 2 (red trace) is shown in Figure 38 and it is clear to see the extent of difference between the harmonic content of the two signals. With the frequency break points occurring at around 30 MHz for Signal 1 and 800 kHz for Signal 2 the decay rate

of 40dB/decade occurs much earlier into the frequency spectrum for the triangle wave meaning that the remaining harmonics beyond this point fall quicker towards the noise floor.

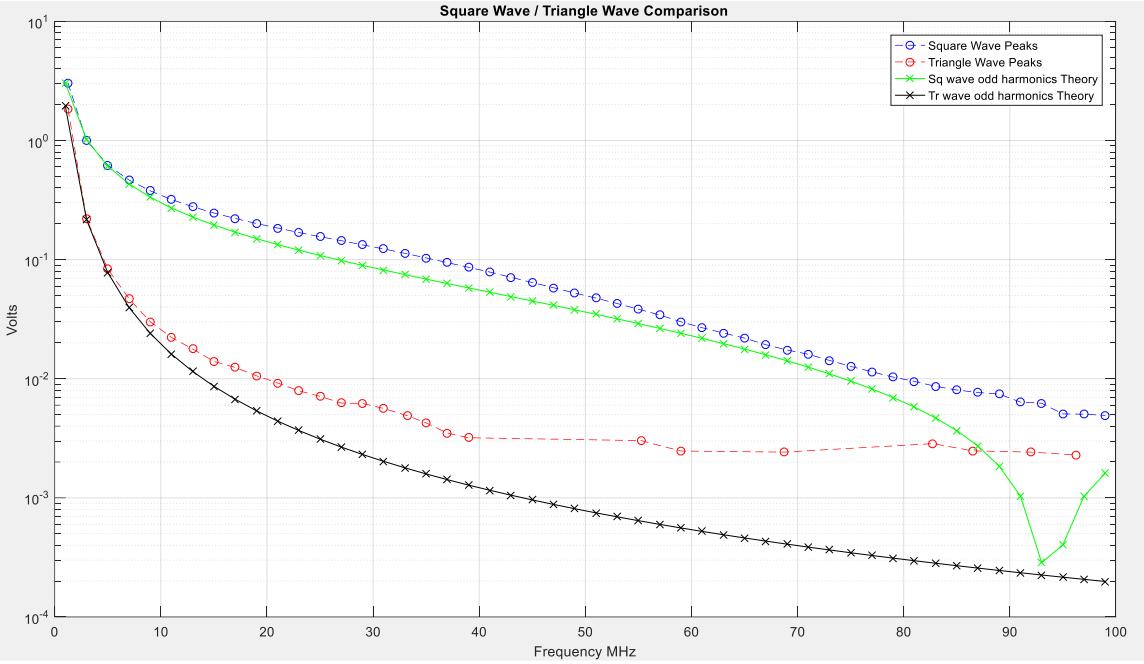


Figure 38: Square Wave and Triangle Wave (Practical & Theory)

For another level of comparison, taking the mean value of the peak levels recorded gives an indication of how vastly the two peak level plots vary with Signal 1 having a mean level of approximately -13dBµV in comparison to Signal 2, which is approximately -27dBµV. These give and overall mean difference between the harmonic content with the two signals of -14dB.

3.2.3 Theory v Practical Curve Comparison

Figure 38 illustrates the practical and theoretical frequency domain behaviours of the square and triangle wave signals used for this testing. The blue and green traces represent the practical and theoretical curves respectively for the square wave, and the red and black traces represent the practical and theoretical curves respectively for the triangle wave. As can be seen from the curves for each signal although they are very close yet there are still some differences between the practical and theoretical approximations of the signals detailed in Table 2.

Firstly analysing the practical and theoretical traces from the square wave, the amplitude of the harmonics recorded are greater along the observed spectrum past the 5th harmonic than the theoretical results present themselves to be. The reasoning for this is that the practical frequency domain behaviour will not contain solely odd harmonics due to the asymmetry of the edges of the signal and the even harmonics have raised the peak level recorded above the amplitude of the theoretical trace. This is supported by the absence of the concave presented by the square wave theoretical trace between 80 – 100MHz, the even harmonics present

within the practical frequency domain behaviour present the peak level as a straight line through this frequency range of the spectrum.

The practical and theoretical traces plotted for the triangle wave again are very similar, with the practical trace having a greater peak amplitude across the observed spectrum. With the addition of even harmonics from the asymmetry of the edges of the triangle wave the amplitude of the peak level harmonics does not decay as quickly as the theoretical trace. The peaks recorded past the 40MHz frequency are not recorded practically as they have fallen below the noise floor.

3.3 Signal 3 - 6 Time and Frequency Domain Results

The difference between the harmonic content of the signals produced by the MSCR-001 PCB will not be as great as those shown in Figure 34 & Figure 35. The rise times of the signals that are produced by the FPGA are likely to be much closer. The analysis in this section is intended to serve as a more accurate depiction of the signals that will be produced by the FPGA.

The testing strategy applied to Signals 1 & 2 will be applied to the Signals 3 – 6 from

Table 2. The time and frequency domain representations have been obtained practically and plotted comparatively for the four of the signals. The observed range of the frequency spectrum has been extended up to a stop frequency of 150 MHz as the signals will be operating with similar edge rates to Signal 1 and this is will ensure that the harmonics further along the spectrum are recorded. As seen with Signal 1 the harmonic amplitude continued past the 100MHz upper limit of the observed spectrum. Signals 3, 4, 5 & 6 are illustrated in Figure 39, Figure 40, Figure 41 and Figure 42 respectively and are four square waves with a rise time starting 10ns and doubling to reach a final rise time of 80ns.

3.3.1 Time Domain Analysis

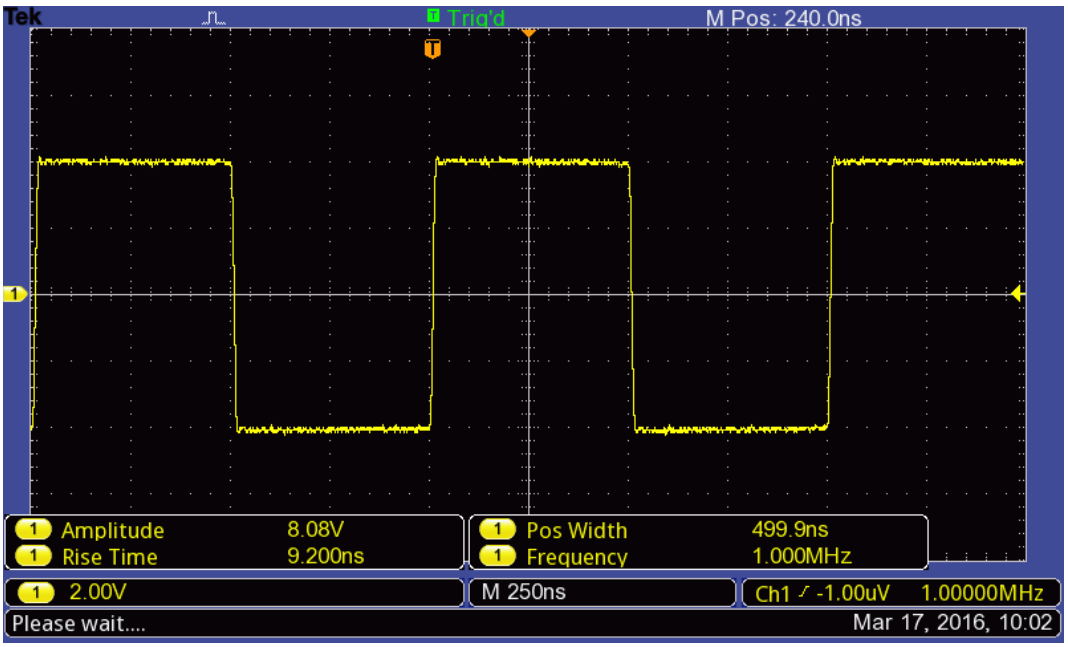


Figure 39: Signal Generator Square Wave 10nS Rise Time

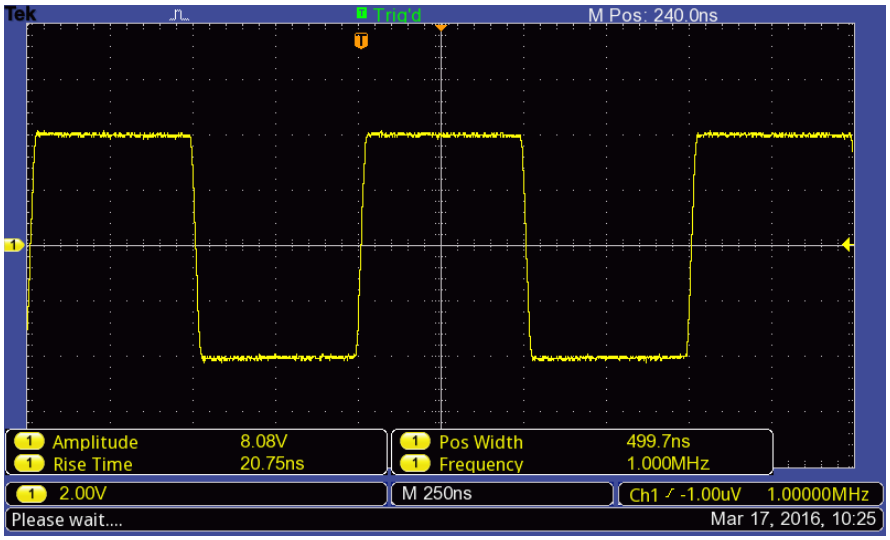


Figure 40: Signal Generator Square Wave 20nS Rise Time

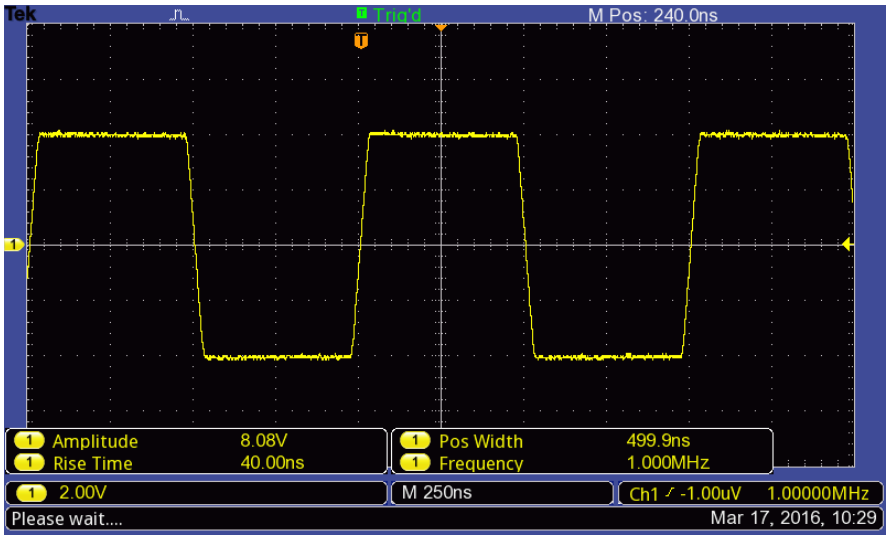
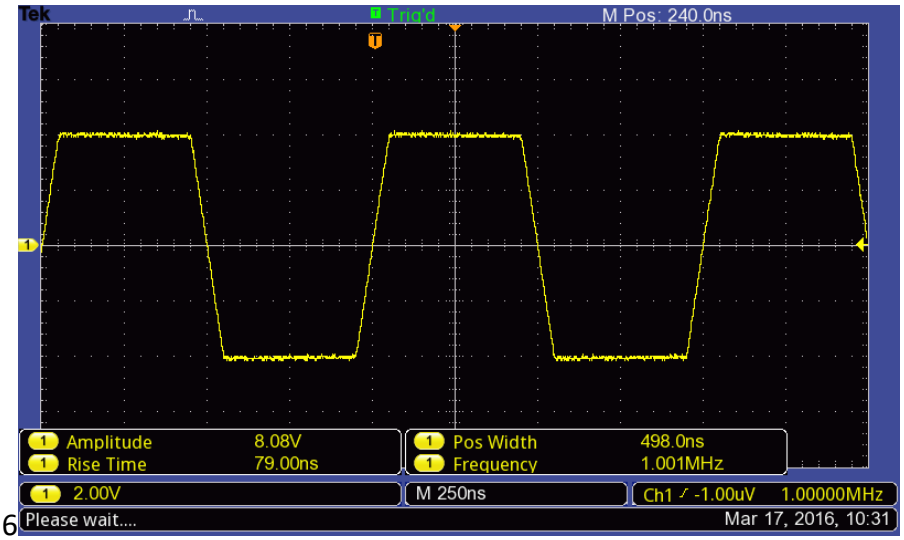


Figure 41: Signal Generator Square Wave 40nS Rise Time



6

Figure 42: Signal Generator Square Wave 80nS Rise Time

Measured Attribute	Signal 1	Signal 2	Signal 3	Signal 4	Prefix
Rise Time	9.2	20.75	40.00	79.00	ns
Pulse Period	1000	1000	1000	1000	ns
Pulse Width	500	500	500	500	ns
Amplitude	8	8	8	8	V
Frequency Breakpoint	34.5	15.34	7.95	4	MHz

Table 6: Sig Gen Signals 3 - 6 Signal Properties

As the edge rate of the signals increases it can be seen that the signal shape is becoming more representative of a trapezoidal waveform approximation. Secondly to this it can also be seen in Table 6 that the harmonic amplitude decay break point from 20dB/decade to 40dB/decade is approximately halving as the rise time of the signals doubles. From this, a clear difference of harmonic amplitude should be observable from the frequency domain results. The harmonic amplitude will be decaying faster at different points along into the spectrum for each signal.

3.3.2 Frequency Domain Analysis

From the harmonic content of Signals 3 – 6 it can be seen that the higher the edge rate the more representative of a comb like spectrum it becomes. Signal 3 with the fastest edge rate has harmonics with a high enough amplitude to be recorded past the observed spectrum of 150MHz. Whereas the amplitude of harmonics in Signals 4 – 6 have dissipated into the noise floor around the 70 – 100 MHz range.

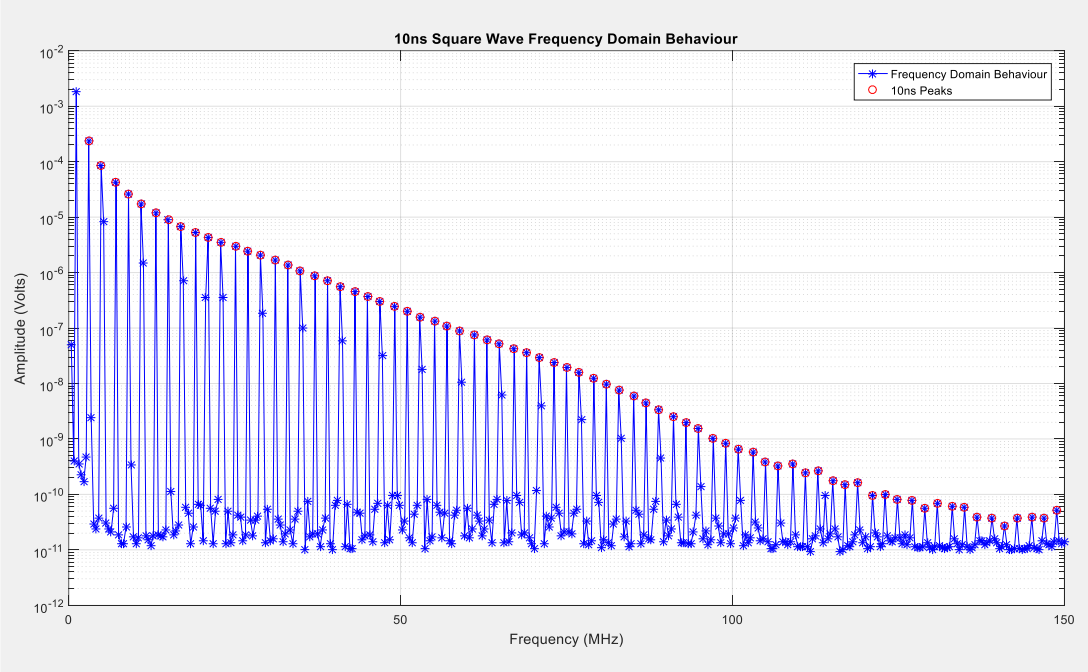


Figure 43: Signal Generator Square Wave 10nS Rise Time Frequency Domain Behaviour

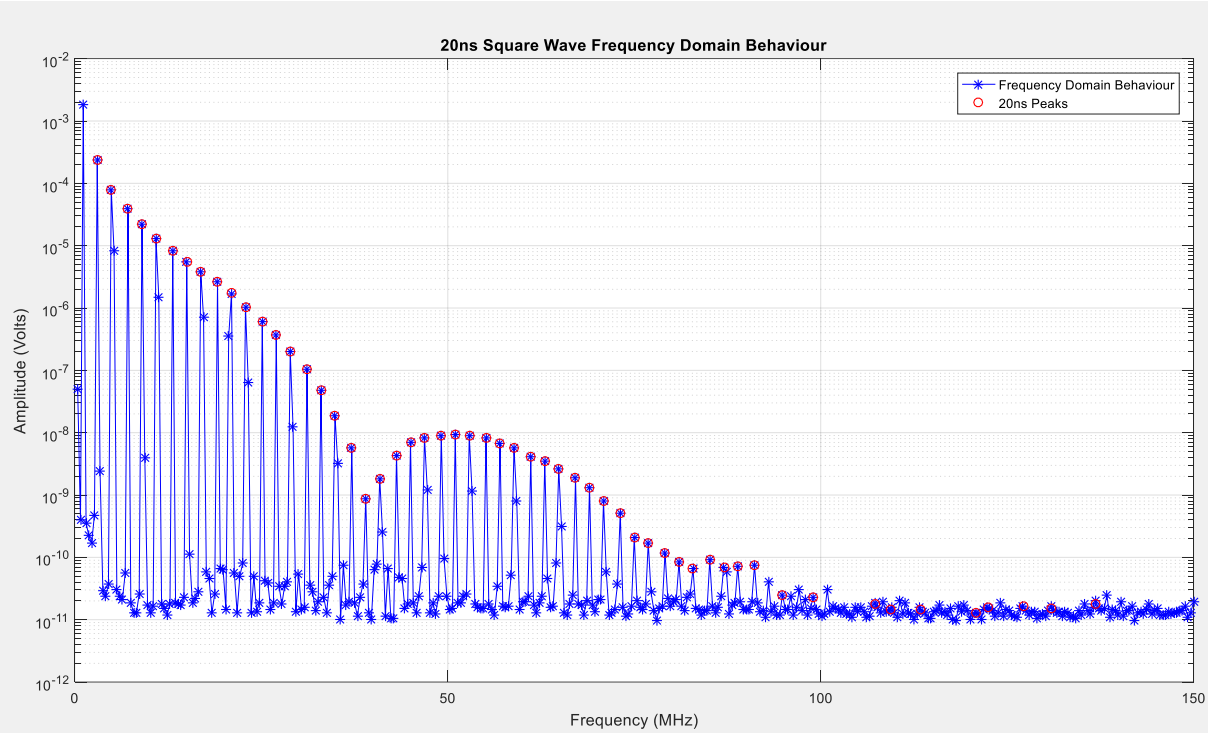


Figure 44: Signal Generator Square Wave 20nS Rise Time Frequency Domain Behaviour

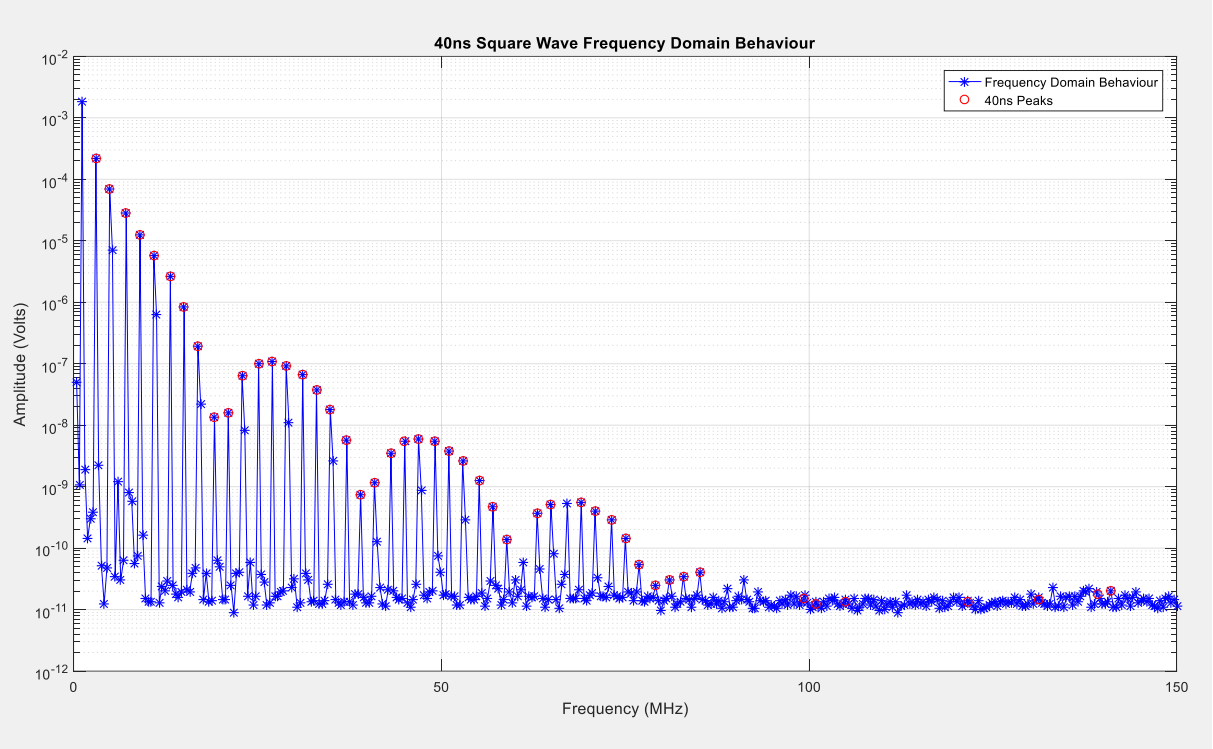


Figure 45: Signal Generator Square Wave 40nS Rise Time Frequency Domain Behaviour

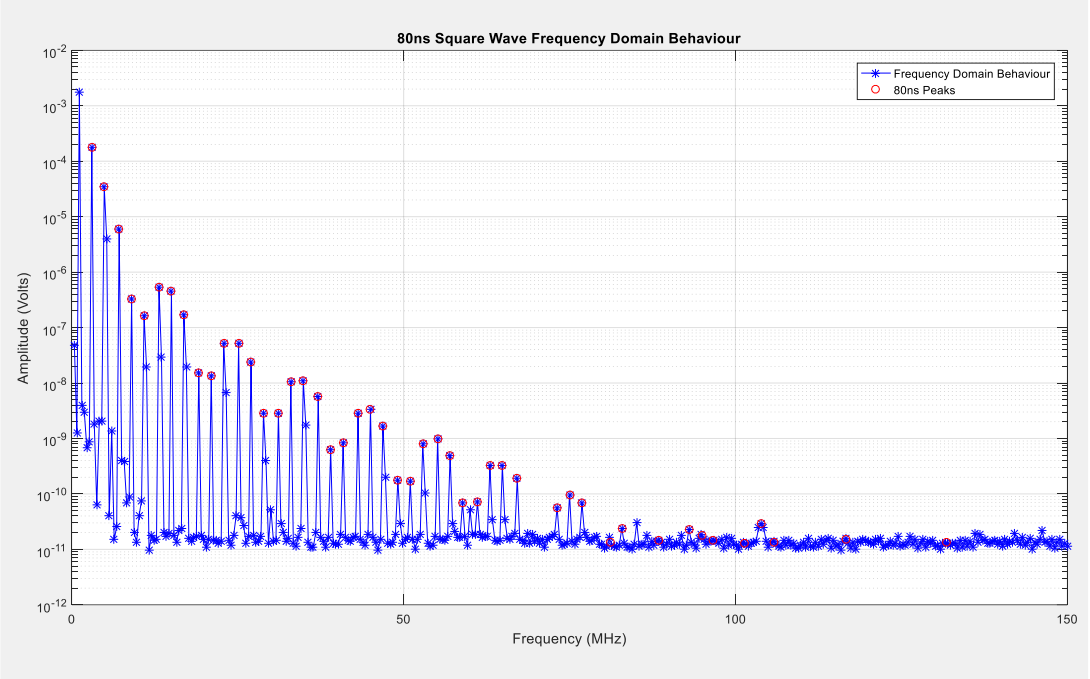


Figure 46: Signal Generator Square Wave 80nS Rise Time Frequency Domain Behaviour

3.3.2.1 Signal 3 – 6 Peak Level Harmonics Comparison

When plotting the peak levels of harmonics comparatively shown in Figure 47, the decay rate and spectral envelopes becomes more apparent. Signal 3 due to its faster edge rate doesn't exhibit the comb pattern within the observed spectrum, potentially altering the reference level on the spectrum analyser would illustrate this and if a higher stop frequency was used. Signal 4 begins to illustrate the comb spectrum envelope with the number of concaves in the envelop doubling as the edge rate doubles across Signals 4 – 6.

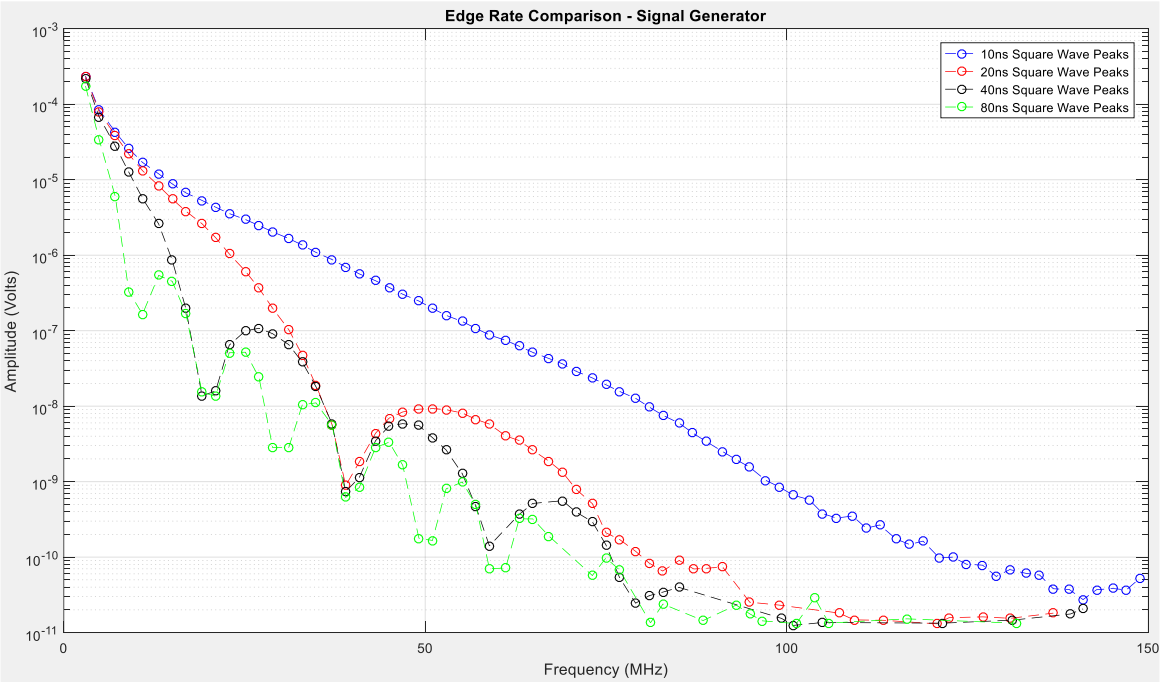


Figure 47: Signal Generator Square Wave Peak Harmonic Level Comparison

From the peak level of the harmonics obtained for the four signals, a clear difference between the peak level harmonic content can be observed from the graph across the spectrum. Analysing the average amplitude of the peak harmonics recorded across the observed spectrum as detailed in Table 7 gives a greater indication of the levels of EMI that could potentially radiate from a digital system due to an edge rate of a signal.

Signal Number	Average Level of Harmonic Amplitude	Prefix
Signal 3	-17.7	dBµV
Signal 4	-22.6	dBµV
Signal 5	-24.0	dBµV
Signal 6	-28.0	dBµV

Table 7: Average Level of Peak Harmonics Signal 3 – 6

Comparing the opposite extremes of the signal rise times used a reduction to harmonic amplitude on average across the observed spectrum of 11dB. Signal 3 with a 10ns rise time has an average peak level of harmonics of -17.7dBµV when compared to the Signal 6 with a rise time of 80ns this records an average level of -28dBµV recording. The greatest difference seen between by doubling the rise time is between 10ns and 20ns and this shows a reduction to harmonic amplitude of 5.1dB. This shows that considering the rise time of a signal within a design can drastically reduce the amplitude of the harmonics.

3.3.3 Theory v Practical Curve Comparison

Figure 48 to Figure 51 illustrates the practical v theoretical domain plots of Signals 3 – 6 detailed in Table 2, the spectrum analyser is recording in dBm terminated with 50Ω.

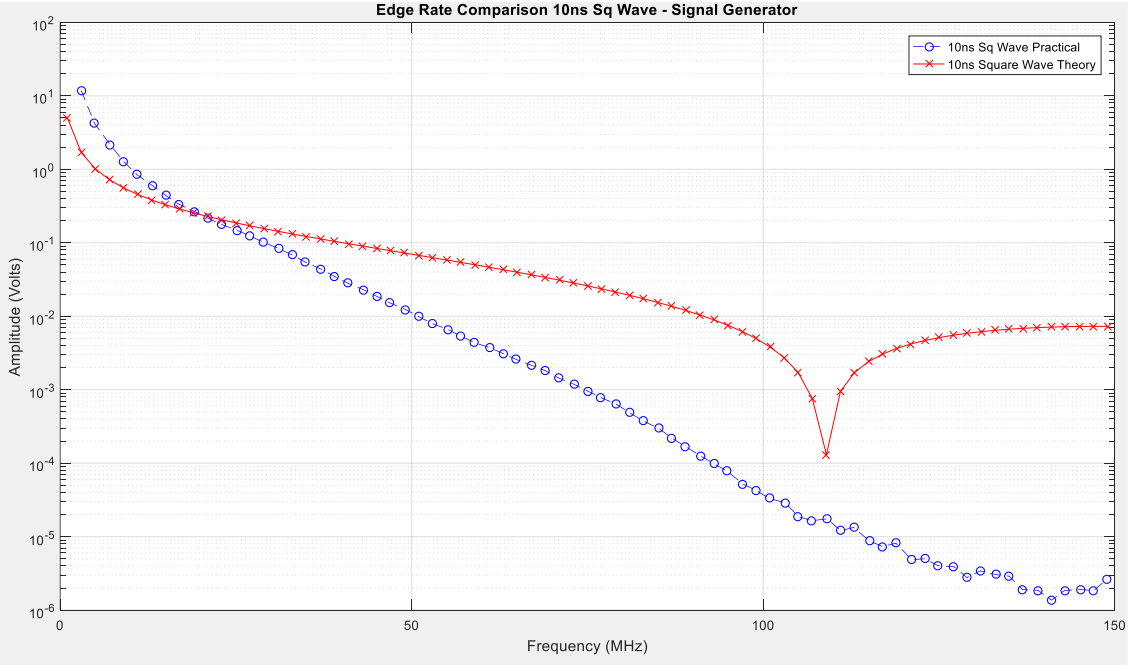


Figure 48: 10ns Square Wave Practical & Theoretical Curves

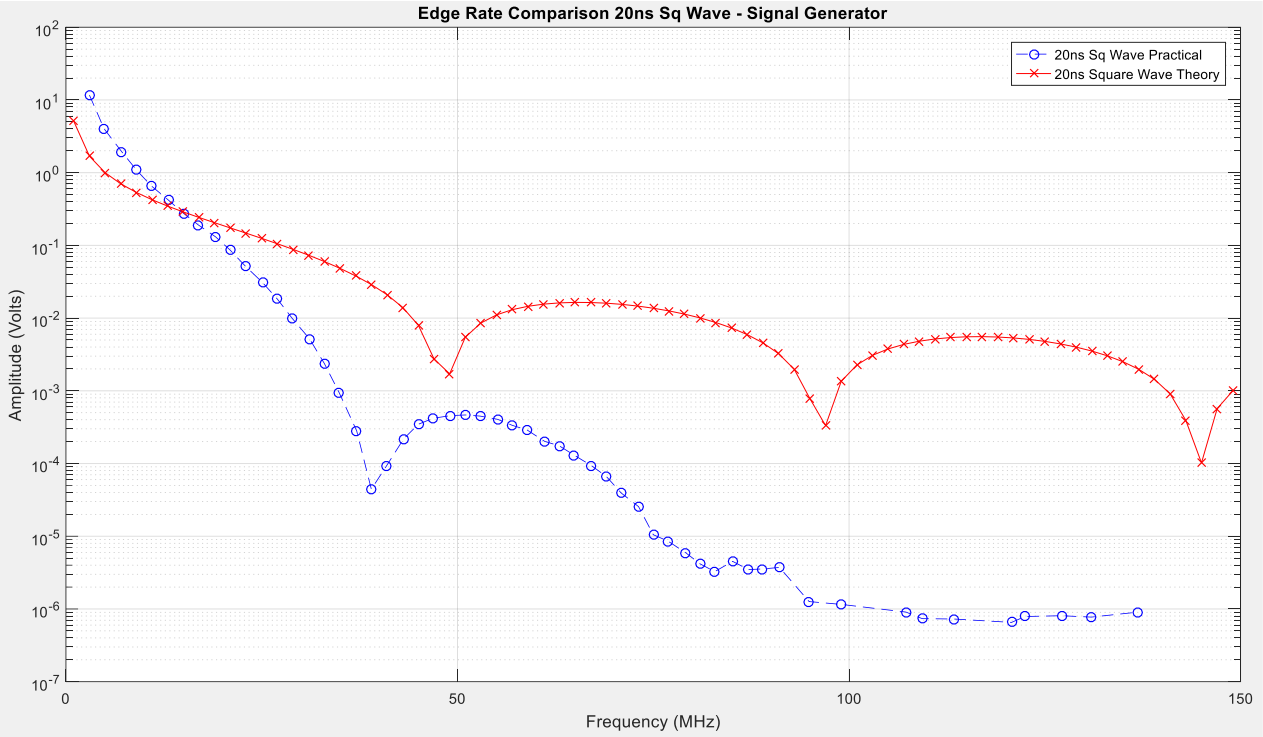


Figure 49: 20ns Square Wave Practical & Theoretical Curves

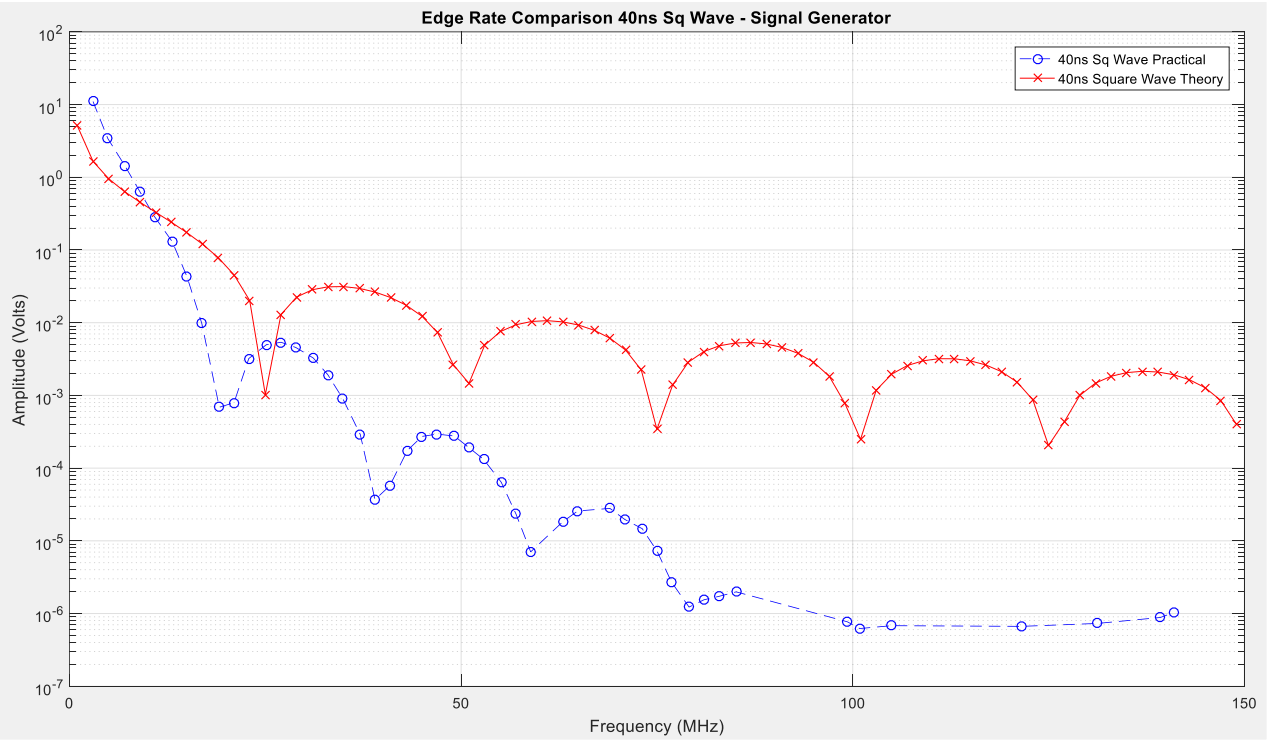


Figure 50: 40ns Square Wave Practical & Theoretical Curves

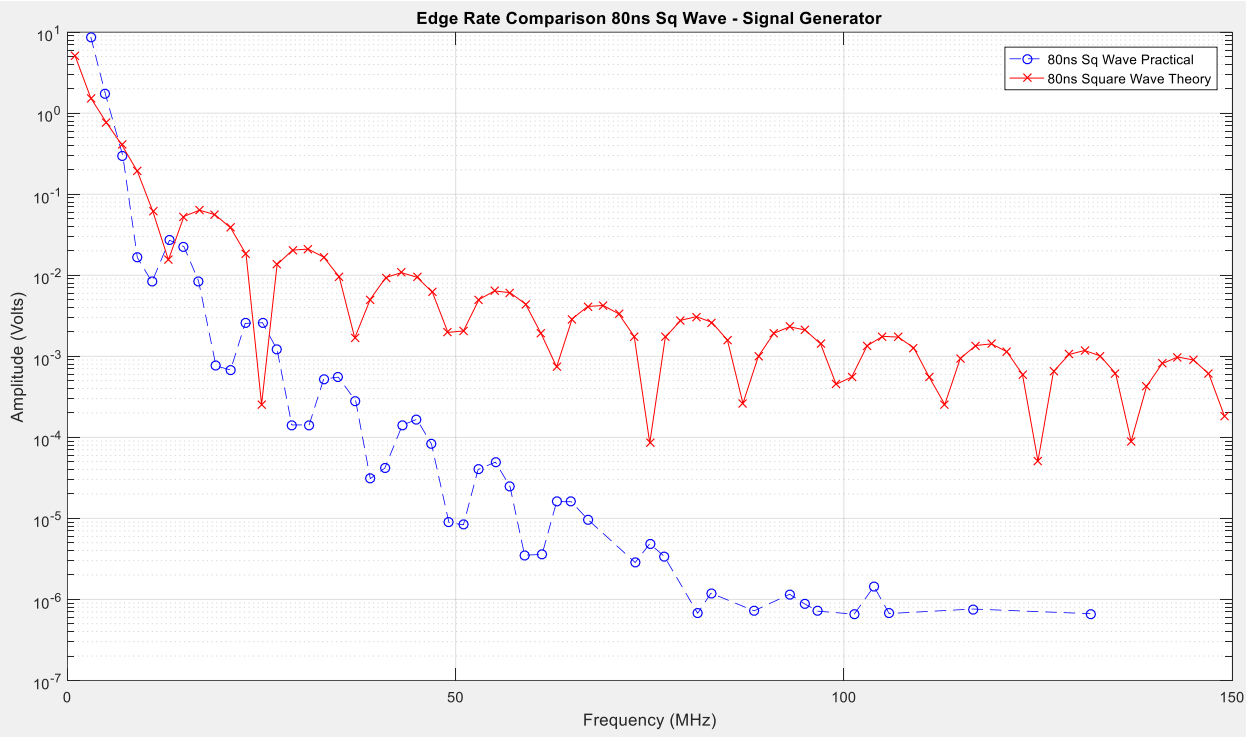


Figure 51: 80ns Square Wave Practical & Theoretical Curves

Examining the comparison plots in Figure 48 to Figure 51 it can be seen how the practical results can drastically vary from what is expected from the theory. Firstly, the amplitude of the harmonics is higher for the practical traces than the theoretical curves on each of the plots around the fundamental frequency.

This is down to the even harmonics present within the frequency spectrum increasing the magnitude of the peak level harmonics recorded around the fundamental frequency. The practical trace decays at a faster rate than the theoretical trace causing the peaks to fall below the noise floor around the 150MHz region for signal 3 (Figure 48) and 80 – 100MHz region for signal 4 - 6 (Figure 49 to Figure 51). The cause of this fast decay to harmonic amplitude is due to the finite rise time of the signals meaning that the break point at $F_2 = \frac{1}{\pi t_r}$ occurs increasing the decay from 20dB/decade to 40dB/decade of the harmonics until they fall below the noise floor.

3.4 Signal Generator Testing Conclusion

From the testing and analysis carried out in section 3, it is illustrative of what to expect when analysing the harmonic content of digital clock signals in 'ideal' practical conditions. The relationship between the amplitude of harmonics recorded and the edge rate of signals has been established by comparing Signals 1 – 6 from Table 2. The comb spectral envelope has been illustrated in Figure 48 to Figure 51 showing both the practical and theoretical signal curves and has shown the progression of harmonic amplitude decay as the edge rate increases by a factor of two each time. Throughout this analysis, ideal practical conditions have been used with a transmission line of 50Ω and termination impedance of 50Ω. The

source used is as accurate as can be achieved practically and has recorded close results between the practical and theoretical frequency domain behaviours in Figure 38. This has formed a basis of understanding and comparison to the signals from the FPGA. There is some misalignment between the theoretical and practical traces on each of the figures, most noticeably the fundamental frequencies on Figure 48 to Figure 51 is not aligned. This is down to the MATLAB code missing the fundamental frequency harmonic as the points recorded prior to this peak are minimal, which does not allow for the peak to be correctly identified. Secondly the minima is misaligned between the theoretical and practical traces, this is down to an error within the MATLAB code producing the incorrect spectral behaviour. The amplitude is incorrect due to the harmonic decay of the theoretical trace not experiencing the second frequency break point of F_2 leading to an error within the plots.

In reality, the testing of the FPGA signals will vary as the transmission medium will not be a shielded coaxial cable terminating at the measurement instrument, it will be a PCB trace exposed to EMI. The signals will be subjected to components with parasitic characteristics and tolerances, which will alter the amplitude of the harmonics recorded. The advantages of the testing carried out in section 3 has given a representation of the characteristics of harmonics from clock signals over a variety of edge rates and will allow for any abnormalities from the FPGA time and frequency domain testing to be identified.

4 Signal Integrity Testing - MSCR-001 PCB

Following on from the testing carried out in Section 3, Section 4 examines the harmonic content and the signal integrity of a selection of signals produced by the FPGA. This is intended to examine and validate the signals produced by MSCR-001 PCB before subjecting it to radiated emissions testing, and to ensure that results gained are emissions levels of the attributes intended to be measured.

4.1 Spartan 6 I/O Attributes

The I/O driver attributes available within the Spartan-6 FPGA are detailed in Table 8 and allow variation through their drive strength, edge rate, and logic standards. For the purpose of this research, the logic standards will be restricted to LVCMOS and LVTTL.

Attribute	Variable Settings						
Drive Strength (mA)	24	16	12	8	6	4	2
Edge Rate	FAST				SLOW		
Logic Standard	LVCMOS				LVTTL		
Voltage Level CMOS	LVCMOS33 (3.3V)		LVCMOS25 (2.5V)		LVCMOS18 (1.8V)	LVCMOS15 (1.5V)	LVCMOS12 (1.2V)
Voltage Level TTL	LVTTL (3.3V)						

Table 8: I/O Properties for Spartan 6

As can be seen from the array of variable attributes, it is possible to have a multitude of I/O driver settings, which will influence the signals produced by the FPGA. Each setting will alter the properties of the signal produced and ultimately the circuits EMC performance.

4.2 Test Plan & Setup

To gain an appreciation of how much of an influence the I/O driver attributes have on the signals produced by the FPGA, eight signals have been chosen for analysis. This testing is to examine whether any change is identifiable between the time and frequency domain representations at each driver setting. The chosen signals identified in Table 9, are taken from the two logic standards LVTTL and LVCMOS33. The testing examines signals from the greater extremes on what is possible from their drive strengths and edge rate settings. This will ensure that any changes to the amplitude of the harmonics can be attributed to one I/O driver property changing and not a combination of them.

Signal Number	I/O Standard	Drive (mA)	Slew	Clock Frequency
1	LVTTL	24	Fast	5 MHz
2	LVTTL	24	Slow	5 MHz
3	LVTTL	2	Fast	5MHz
4	LVTTL	2	Slow	5 MHz
5	LVCMOS33	24	Fast	5 MHz
6	LVCMOS33	24	Slow	5 MHz
7	LVCMOS33	2	Fast	5 MHz
8	LVCMOS33	2	Slow	5 MHz

Table 9: MSCR-001 Output Driver Attributes

If a change to the harmonic content of signals cannot be identified when making a large change to the drive strength and edge rates settings then it is highly improbable that any difference can be identified with signals sharing similar settings. Figure 52 and Figure 53 gives an overview of the testing setup for the signal integrity measurements to be taken from the MSCR-001 PCB.

4.2.1 Time & Frequency Domain Set-Ups

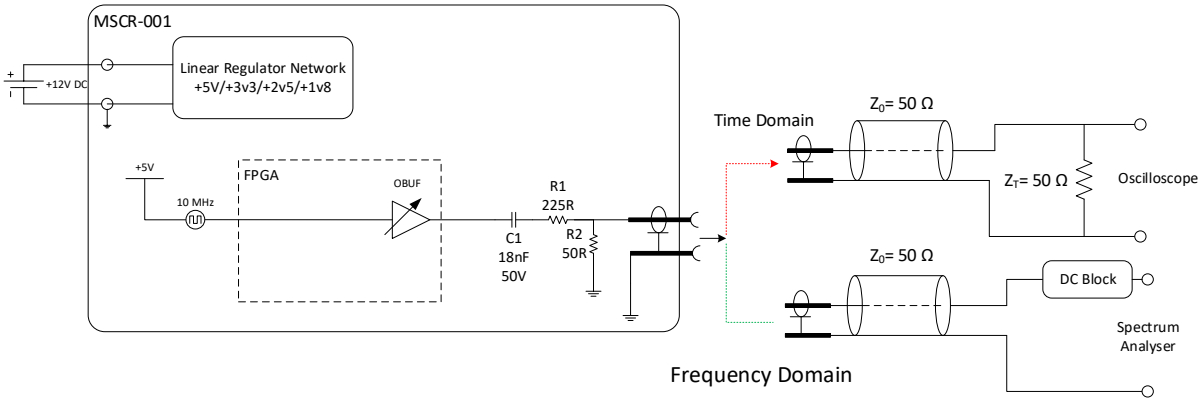


Figure 52: Time & Frequency Domain Test Setup MSCR-001

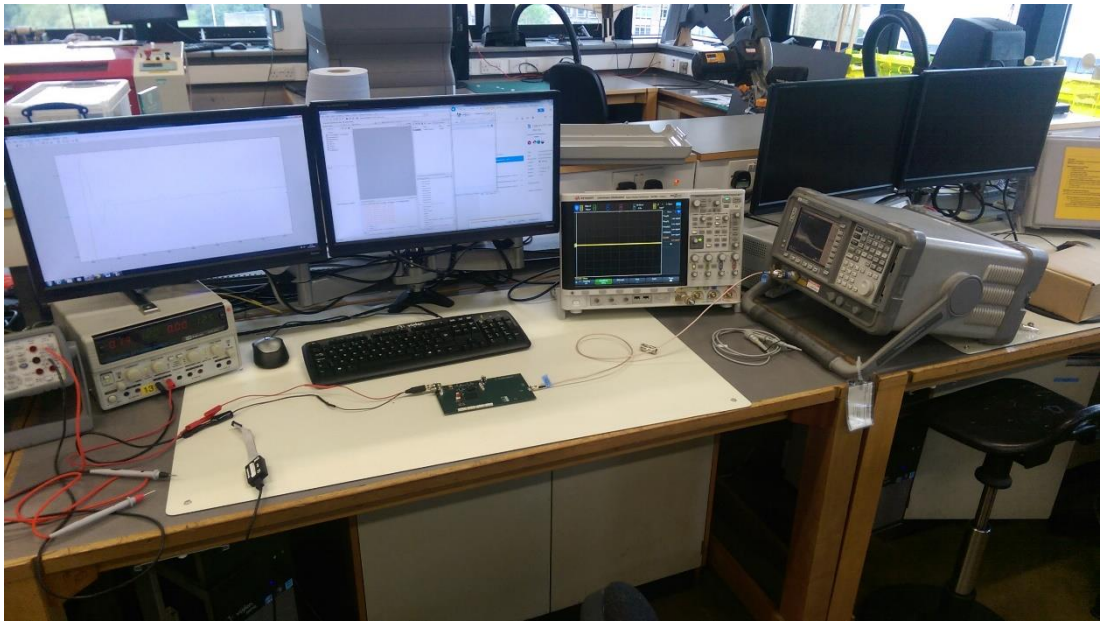


Figure 53: Time & Frequency Domain Test Setup Photograph

The test setup consists of a variable bench top power supply outputting +12V DC to the PCB. The FPGA provides an output signal to the on board SMA Connector, which connects to a 50Ω RF cable. The interface to the oscilloscope contains a 50Ω termination to inhibit reflections on the line. The interface to the spectrum analyser contains a DC block as another layer of protection to the spectrum analyser. The 50Ω termination on the input to the spectrum analyser is not required due to the input impedance to the analyser being 50Ω. For time domain testing the cable will terminate at the oscilloscope and for the frequency domain testing the cable will terminate at the spectrum analyser.

The equipment used for the testing of this hardware is listed below;

4.2.2 Time Domain Test Equipment

Item	Manufacturer	Model	Specification
Variable PSU	GW Instek	K1 Module PL310	Voltage Range: 0 – 30V Maximum Current: 3A
DUT	N/A	MSCR-001	Voltages: 12V/5V/3.3V/2.5V/1.8V Current Drawn: 0.2A
Oscilloscope Probe	Tektronix	TBS1202B	Bandwidth : 200 MHz Sample Rate: 2 GS/s
BNC T-Piece	Amphenol	B9073D1-ND3G-50	Impedance: 50 Ohm
50R Termination	Amphenol	B1004A1-ND3G-50R-0.01-1W	Impedance: 50 Ohm
Oscilloscope	Keysight	InfiiVision DSOX4024A	Bandwidth: 200 MHz Sample Rate: 5GS/s

Table 10: Time Domain Testing Equipment

4.2.3 Frequency Domain Test Equipment

Item	Manufacturer	Model	Specification
Variable PSU	GW Instek	K1 Module PL310	Voltage Range: 0 – 30V Maximum Current: 2A
DUT	N/A	MSCR-001	Voltages: 12V/5V/3.3V/2.5V/1.8V Current Drawn: 0.2A
Attenuator	N/A	N/A	On board attenuator giving a 10:1 Attenuation. Resistive T-Attenuator
DC Blocking Capacitor	N/A	N/A	Capacitance Value :
SMa Connector	Emerson		Frequency Range: 0 – 18 GHz
RF Cable	Harbour Industries	M17/152-00001 MIL-DTL-27478	
SMa to BNC Connector	N/A	N/A	N/A
50R Coax			
BNC T-Piece	Amphenol	B9073D1-ND3G-50	Impedance: 50 Ohm
50R Termination	Amphenol	B1004A1-ND3G-50R-0.01-1W	Impedance: 50 Ohm
BNC – N-Type Connector	Multi-Comp	11-32 TGN	
Spectrum Analyser	Hewlett Packard		Frequency Range: 9KHz – 1.5 GHz Max Voltage: 100V DC

Table 11: Frequency Domain Testing equipment

Taking into consideration the data recorded in Figure 43, the harmonic content of the signal has an amplitude above the noise floor past the upper limit of the observed spectrum. To ensure that all harmonics are recorded all along the spectrum the frequency range has been increased to 0 – 800MHz. This is to give a more detailed depiction of how far the harmonics of signals can present themselves along the spectrum under the various I/O driver settings of the FPGA.

4.3 Overview of Testing - MSCR-001 PCB

Using the signals detailed in Table 9, this testing is to analyse the time and frequency domain representations of the signals produced by the FPGA before subjecting the hardware to radiated emissions testing. If the larger differences of driver settings do not deliver a change in harmonic content then it is very unlikely that two drivers exhibiting similar properties will show a noticeable difference to either the amplitude of harmonic content or the emissions they produce using the current testing method.

4.3.1 LVTTL Testing

Figure 54 to Figure 57 shows the time domain representations of Signals 1 - 4 from the FPGA respectively. With Signals 1 & 2 having the highest drive strength settings yet Signal 1 having a fast edge rate and Signal 2 having a slow edge rate setting respectively. A signal having the maximum drive strength and 'fast' edge rate most likely deliver the oscillations to the time domain signals as described in 1.1.1. The FPGA is driving a signal trace routed to 50Ω, an attenuator and an 18nF capacitor which possess and ESL value. It can be seen that both signals are exhibiting overshoot, undershoot and ringing on the transitional edges. This effect will cause additional harmonic peaks to be introduced into the spectrum at the frequency the oscillations occur.

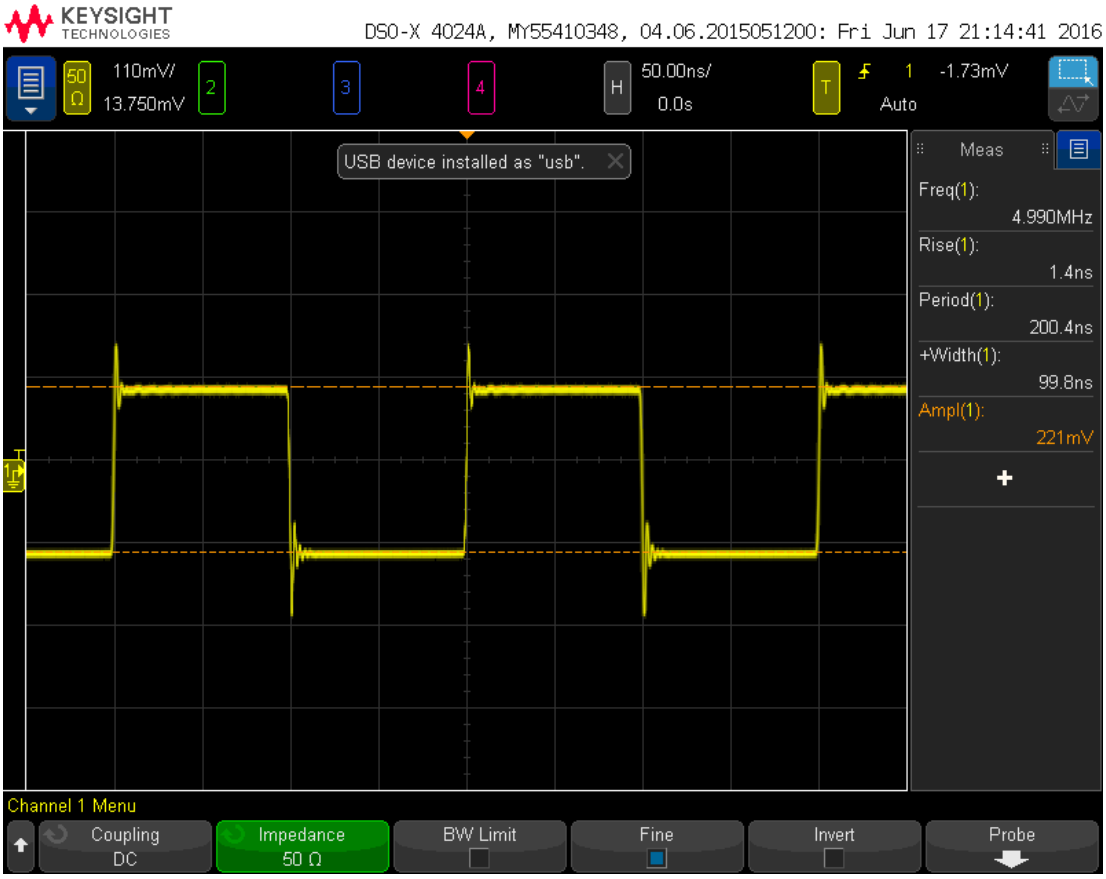


Figure 54: LVTTL-24mA-Fast Time Domain Behaviour

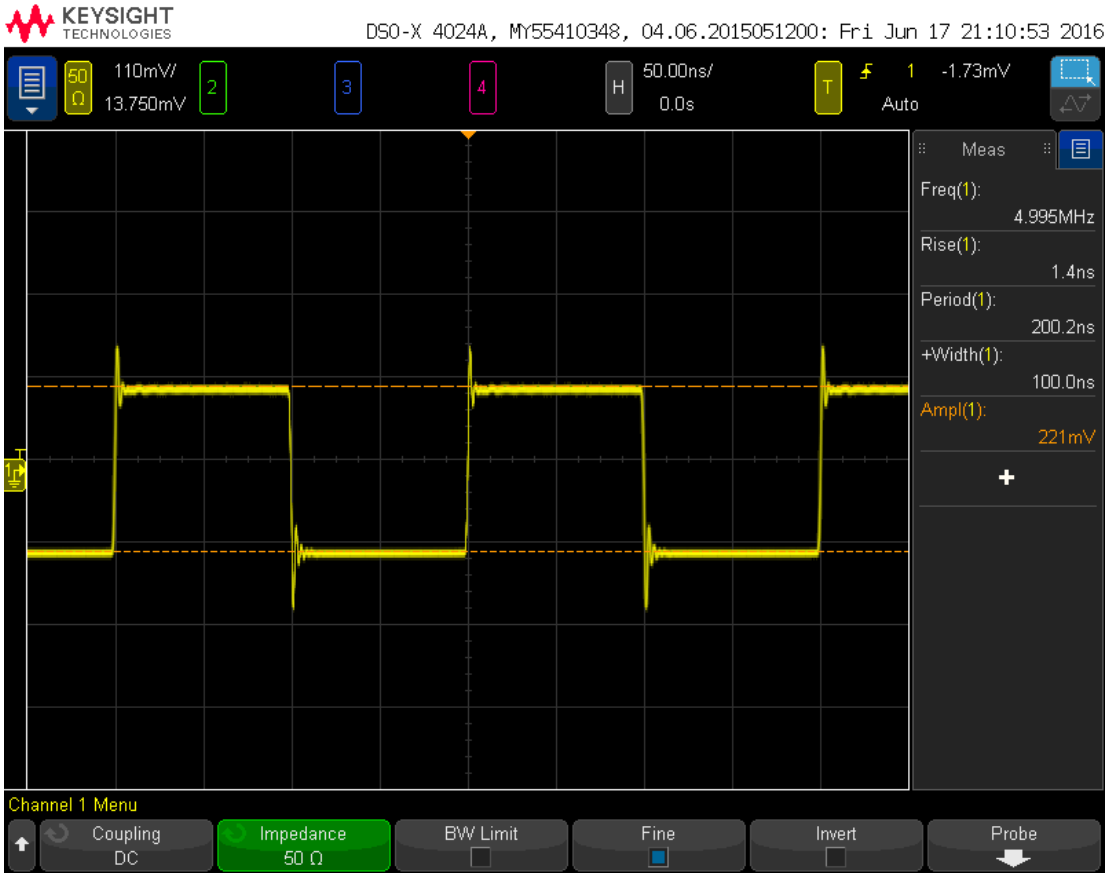


Figure 55: LVTTL/24mA/Slow Time Domain Behaviour

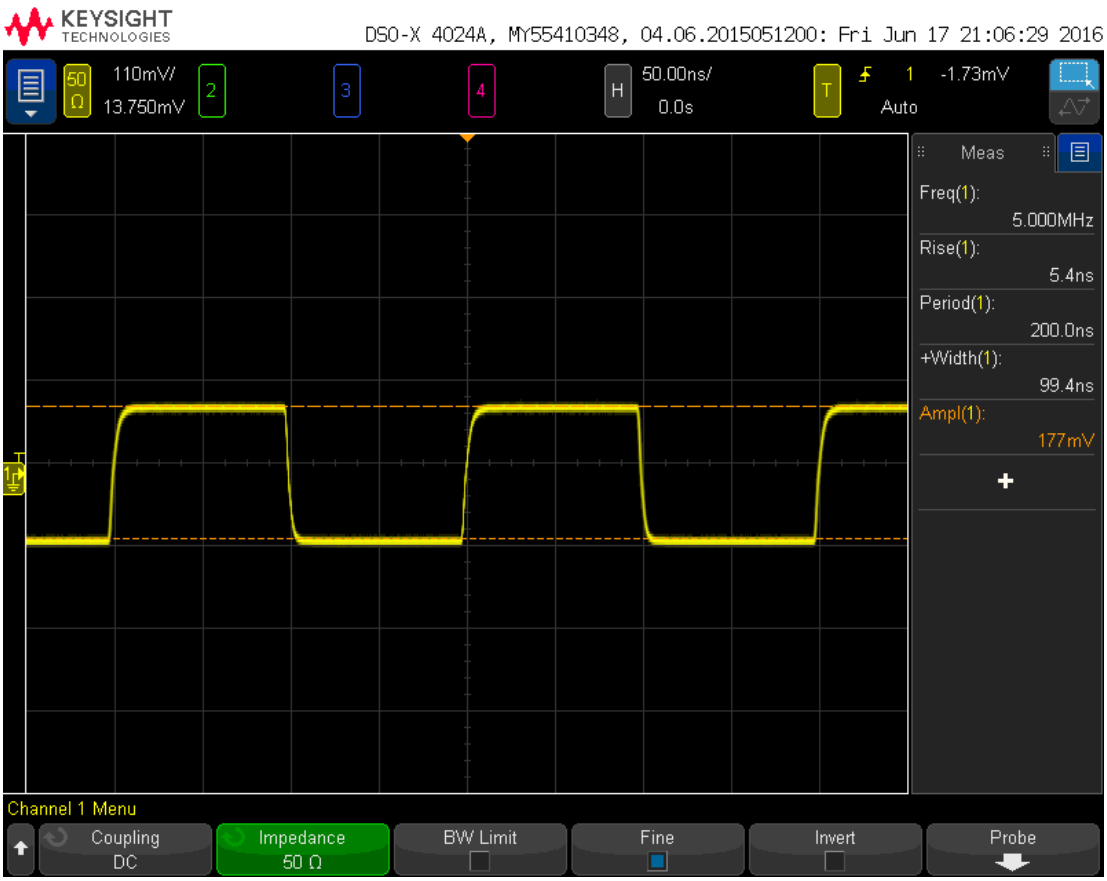


Figure 56: LVTTL/2mA/Fast Time Domain Behaviour

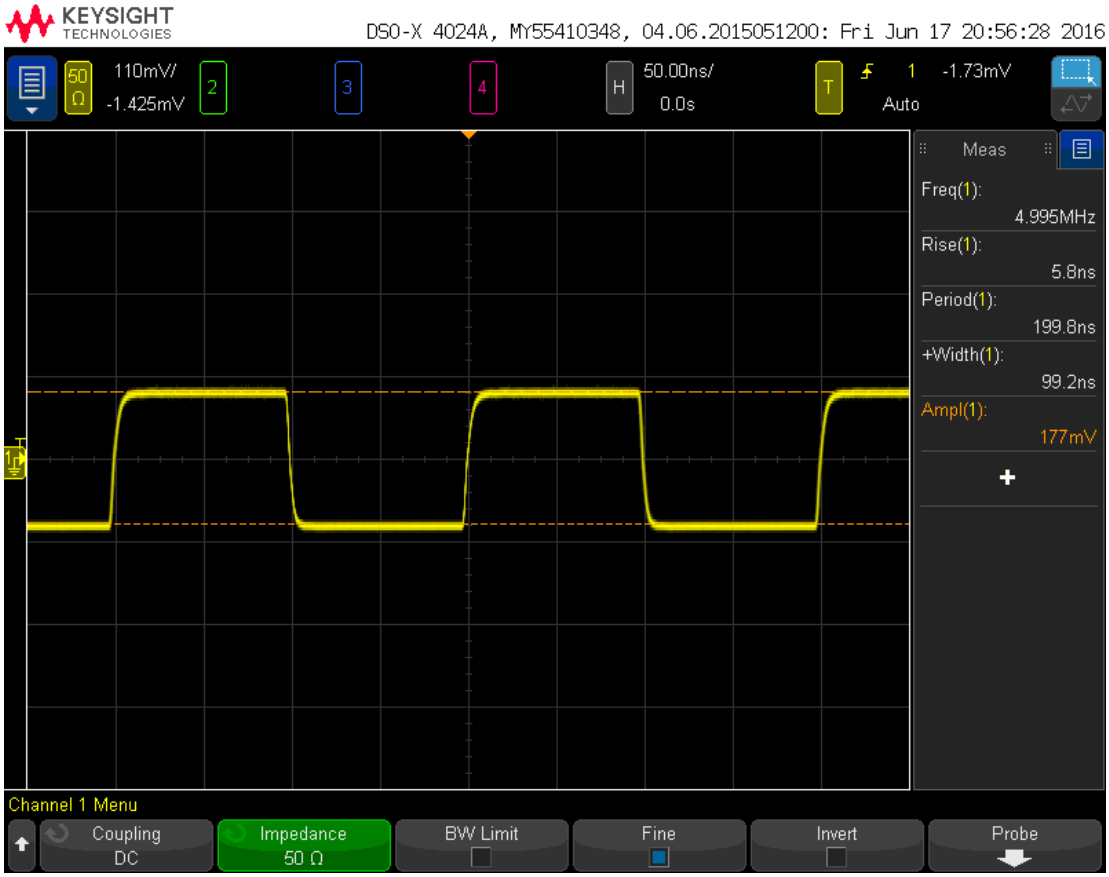


Figure 57: LVTTL-2mA-Slow Time Domain Behaviour

Signals 3 & 4 having the lowest drive strength settings it can be seen that the signals are closely representative of an RC circuit response with the slower rise times rounding off the transitional edges of signals. The rounding of the signal edges occurs due L-C-R response of the PCB trace and measurement protection components. The harmonic content on this signal will be less as the rounding of the transitional edges will attenuate the harmonic peaks as this effect has increased the rise time.

The measured characteristics of the signals are detailed in Table 12.

Measured Attribute	LVTTL-24mA- Fast	LVTTL-24mA-Slow	LVTT-2mA-Fast	LVTTL-2mA-Slow	Prefix
Rise Time	1.4	1.4	5.4	5.8	ns
Pulse Period	200.4	200.2	200	199.8	ns
Pulse Width	99.8	100	99.4	99.2	Ns
Amplitude	2.2	2.2	1.7	1.7	V
Frequency Breakpoint	227.36	227.36	58.94	54.88	MHz

Table 12: LVTTL Signal Characteristics

4.3.1.1 LVTTL Signal Comparison

It can be observed that from changing the drive strength of the I/O buffers it visibly alters the time domain representations of the signals. The 24mA drive strength signals have clear over and undershoot on the transitional edges, whereas the 2mA drive strength signals have rounded edges and overall a reduction of 4.4ns to the rise time of the signals occurs. From this slower rise time and less aggressive transition between states the amplitude of the harmonics should reduce significantly along with it. Plotting the comparative peak level of harmonics recorded in Figure 58 it can be seen that the difference between the two drive strength settings are significant. It is less clear however to see from the graph the difference that changing the edge rate has on the peak level of harmonics. From the 400MHz onwards region it can be seen that the faster edge rate records harmonic peaks above that of the signals with the slower edge rates. Taking the average of the peak level of harmonics recorded for each signal gives an indication of how much the settings vary over the observed spectrum. The LVTTL-24mA-Fast and the LVTTL-24mA-Slow signals recorded an average peak level of -47.53dBµV and -48.03dBµV respectively identifying a reduction to emissions levels of approximately 0.5dB through altering the edge rate of the buffer. The LVTTL-2mA-Fast and LVTTL-2mA-Slow recorded an average level of -57.81dBµV and -58.92dBµV again identifying a reduction to the peak level of emissions however by approximately over 1dBµV. Comparing the two drive strength settings of 24mA to 2mA a reduction to the peak level of emissions of approximately 10dBµV has been recorded. From these figures it can be seen that a difference in the level of peak emissions produced does reduce and can be identified when selecting a reduced drive strength and edge rate setting with the user constraints file.

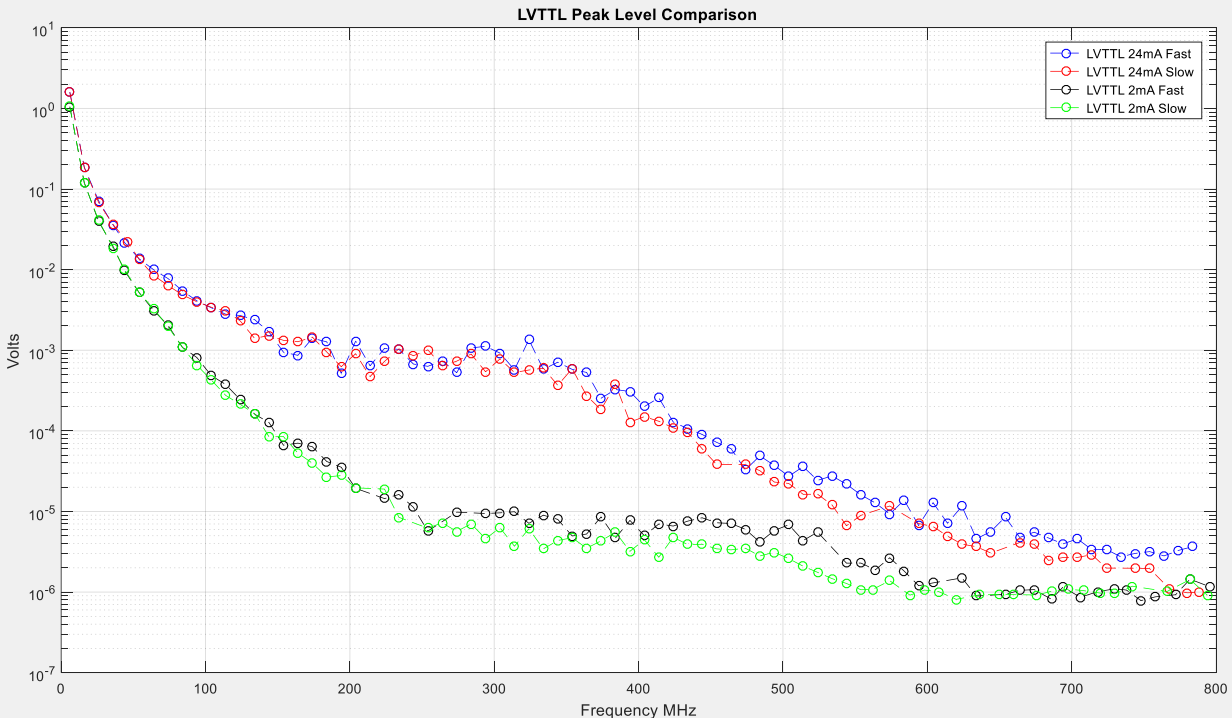


Figure 58: Peak Level Comparison FPGA LVTTL Signals

Observing the graph in Figure 58 it can be seen that the greatest reduction of peak level of harmonic content is between the 200MHz to 400MHz region. A circuit or system containing harmonics with this amplitude could prove to be troublesome during normal operation or radiated emissions testing. This give an insight to the level of reduction that can be achieved to EMI by controlling the selection of the signals communicating with peripherals.

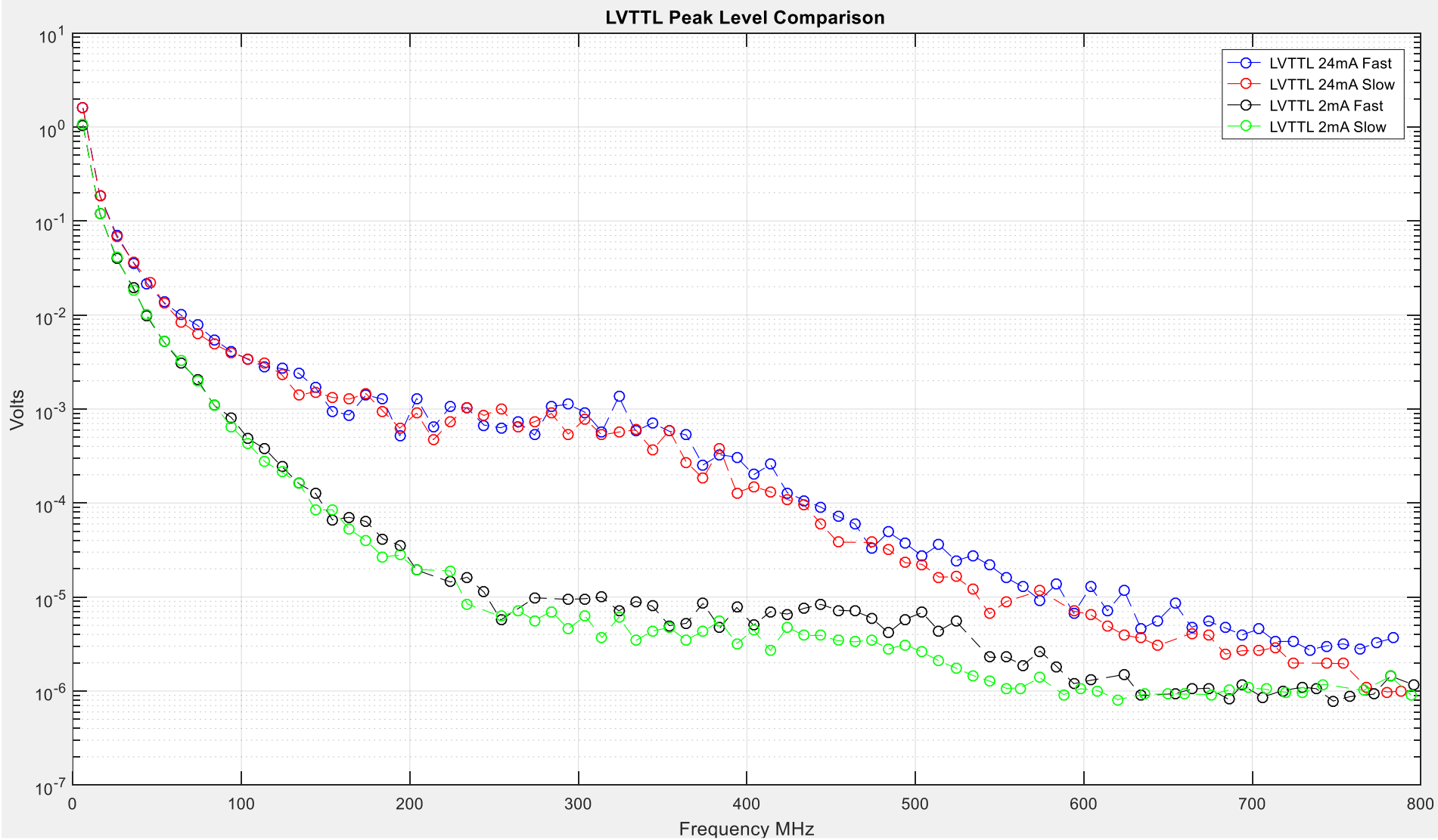


Figure 59: Peak Level Harmonic Comparison FPGA LVTTL Signals

4.3.2 LVTTL Theory v Practical Analysis

The LVTTL-24mA-Fast and LVTTL-2mA-Slow I/O driver settings have been chosen for comparison against the theoretical curve as illustrated in Figure 60 and Figure 61 respectively.

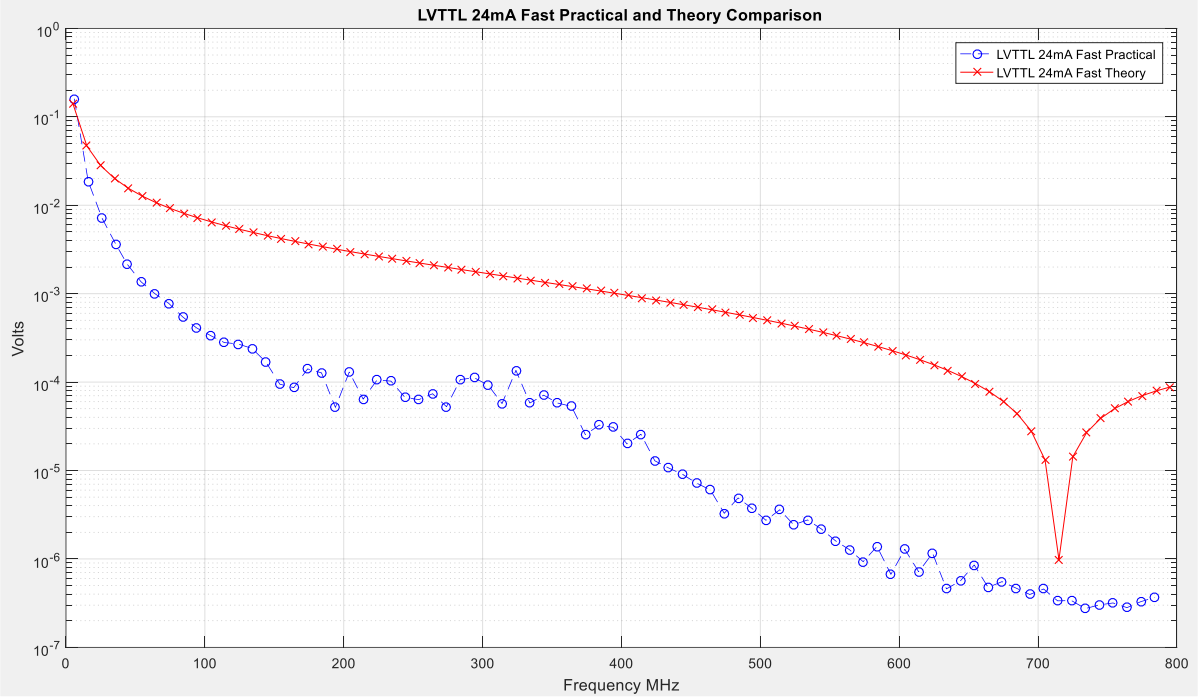


Figure 60: LVTTL-24mA-Fast Practical v Theory Comparison

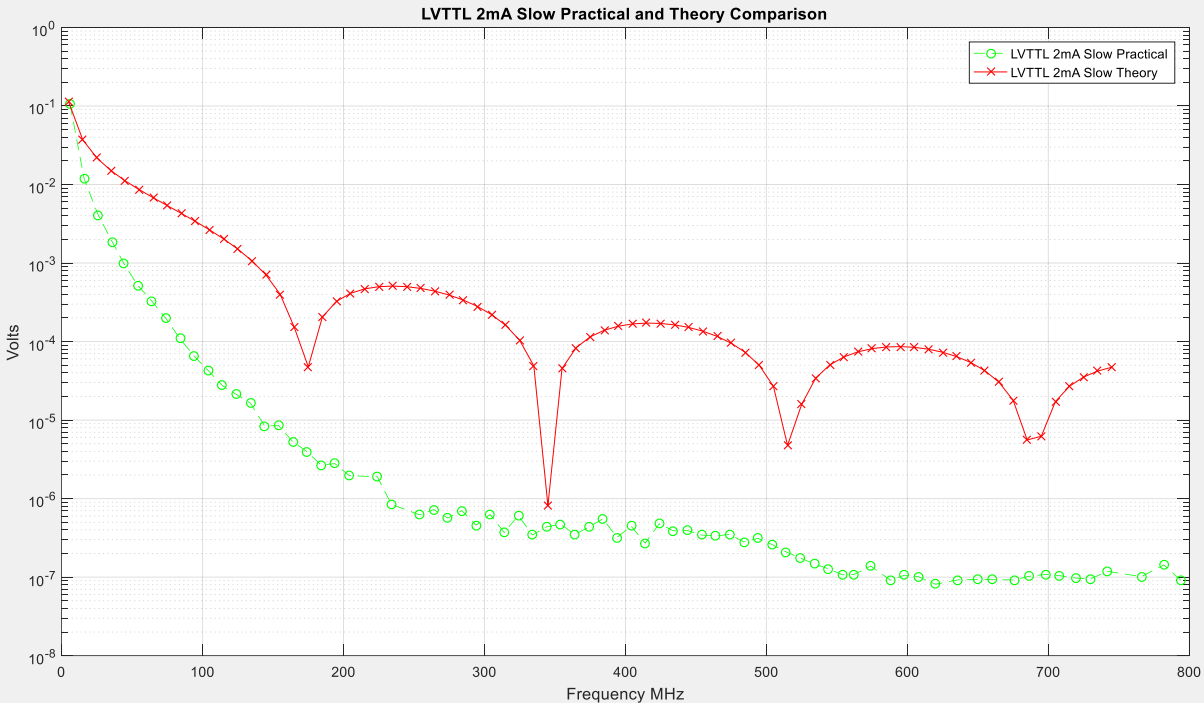


Figure 61: LVTTL-2mA-Slow Practical v Theory Comparison

Analysing the LVTTL practical traces in comparison to the theoretical, it is showing a faster significant decay rate to the amplitude of the harmonics for the practical signal than it is the theoretical. The results show that the fundamental frequency harmonic for the practical signal is slightly less in amplitude than the theory. As the frequency of the harmonics increase the disparity between the theoretical and practical signals becomes greater. This attenuation is due to the attenuation of the practical signals as identified within section 1.1 when applying periodic signals to practical circuitry. Secondly, the attenuation is attributable to the second frequency decay point F_2 leading to a decay rate of 40dB/decade that is not seen with the theoretical representation.

4.3.3 LVCMOS33 Testing

The second set of signals to be assessed from the FPGA is Signals 5 – 8 from Table 9. They are from the LVCMOS 3.3V logic family represented below by Figure 62 to Figure 65 respectively. Again the signals with the highest drive strength are exhibiting over and undershoot on the transitional edges. From this it is to be expected that the harmonic content will not present itself as illustrated in Section 3 with a comb like spectral envelope. The ringing of the signals will introduce additional harmonics to the spectrum leading to variations in the spectral envelope recorded. From the time domain representations change in edge rate setting between signals does deliver a change in the rise time of the signal of 200µs between the LVCMOS33-24mA-Fast and the LVCMOS33-24mA-Slow also the same occurs for the LVCMOS33-2mA-Fast and LVCMOS33-2mA-Slow.

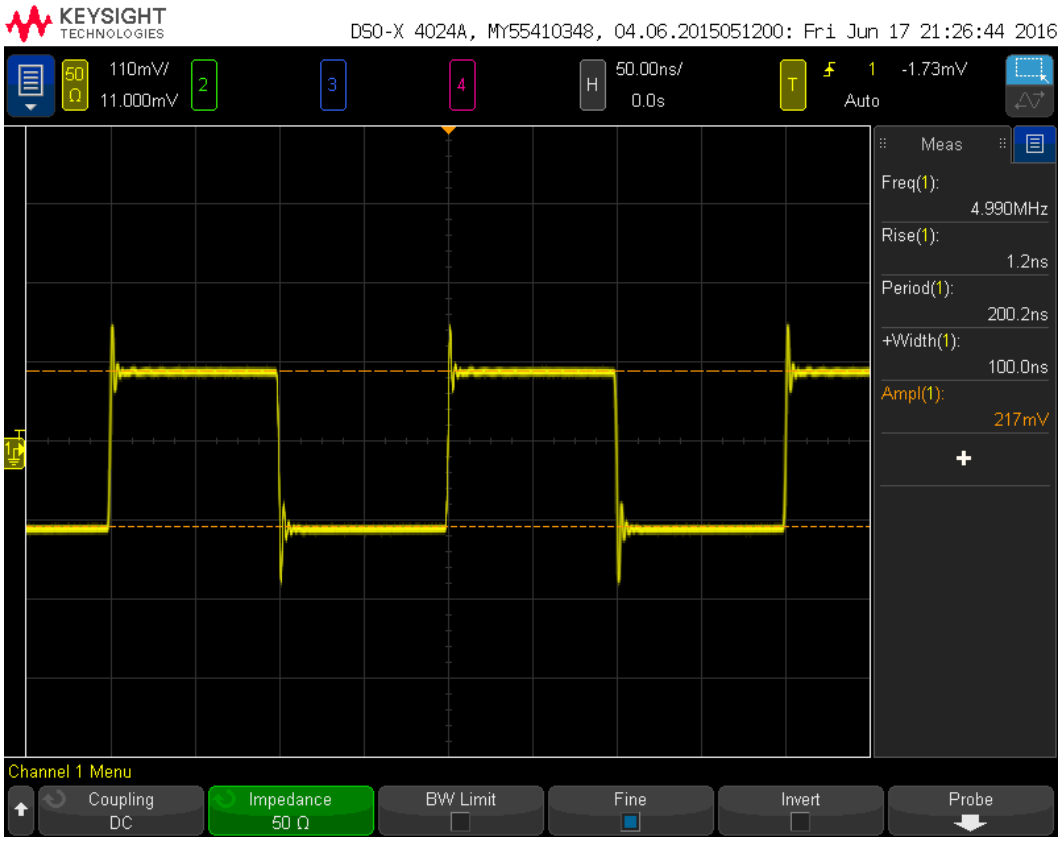


Figure 62: LVCMOS33-24mA-Fast Time Domain Behaviour

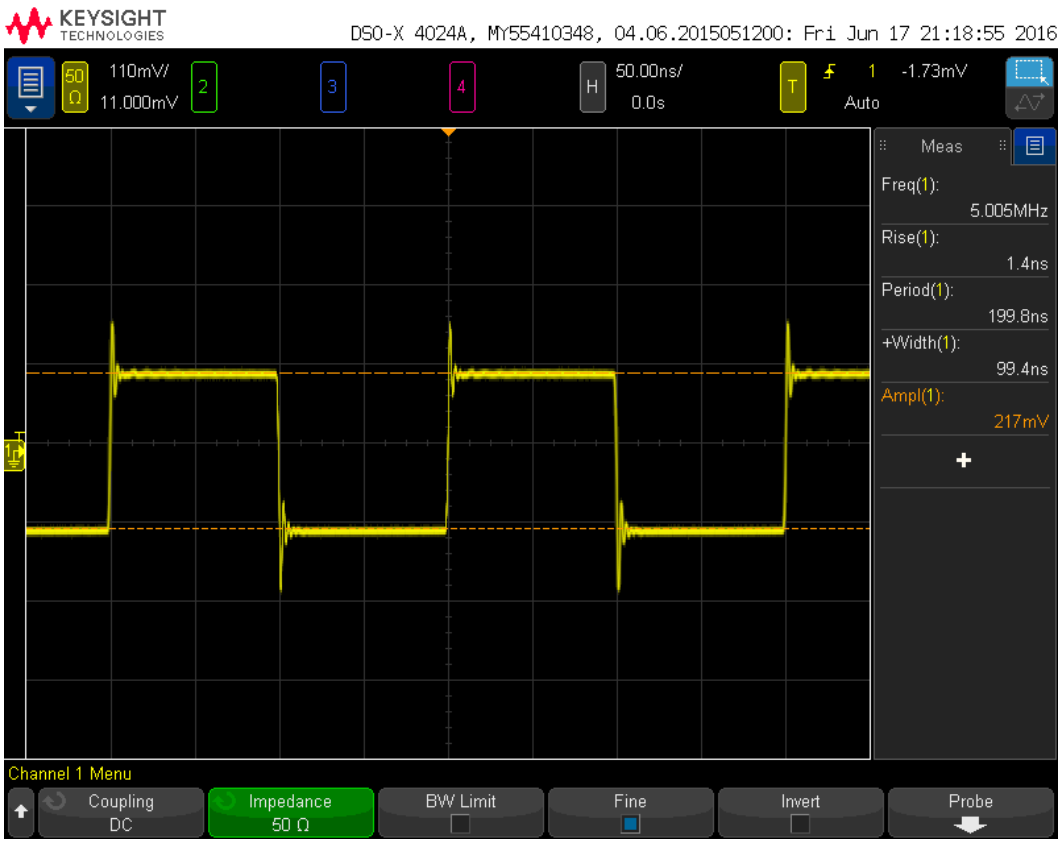


Figure 63: LVCMOS33-24mA-Slow Time Domain Behaviour

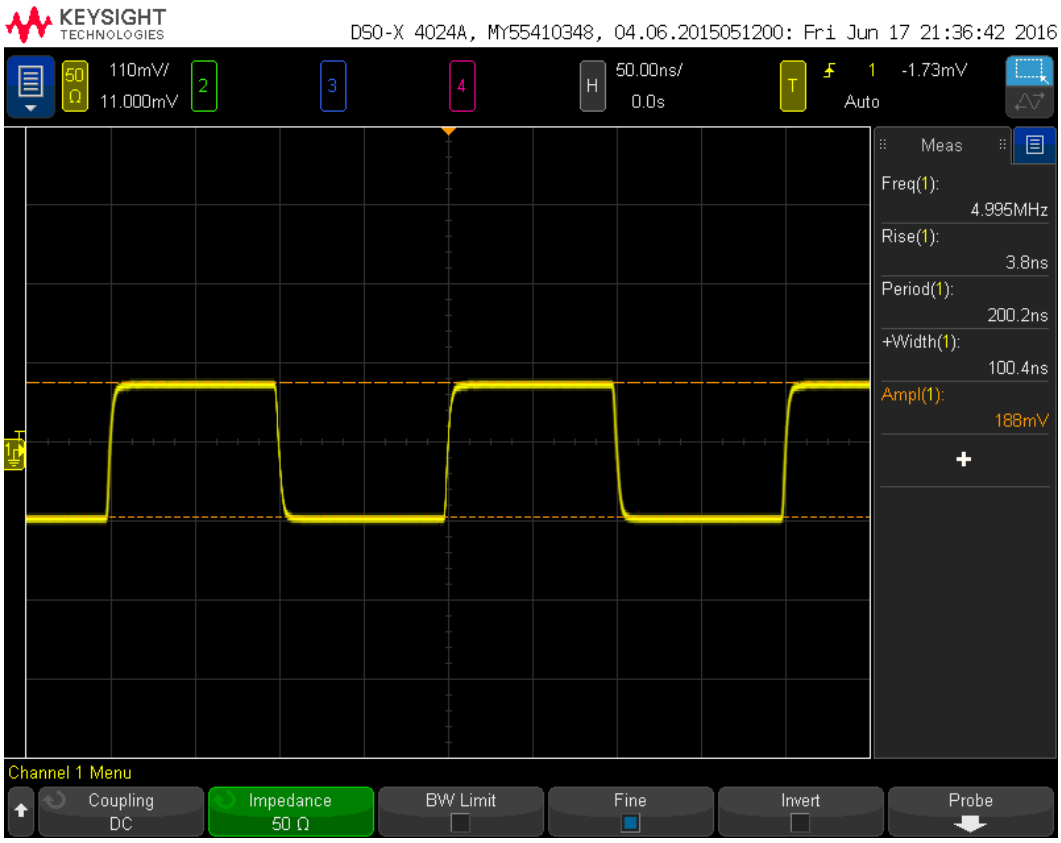


Figure 64: LVCMOS33-2mA-Fast Time Domain Behaviour

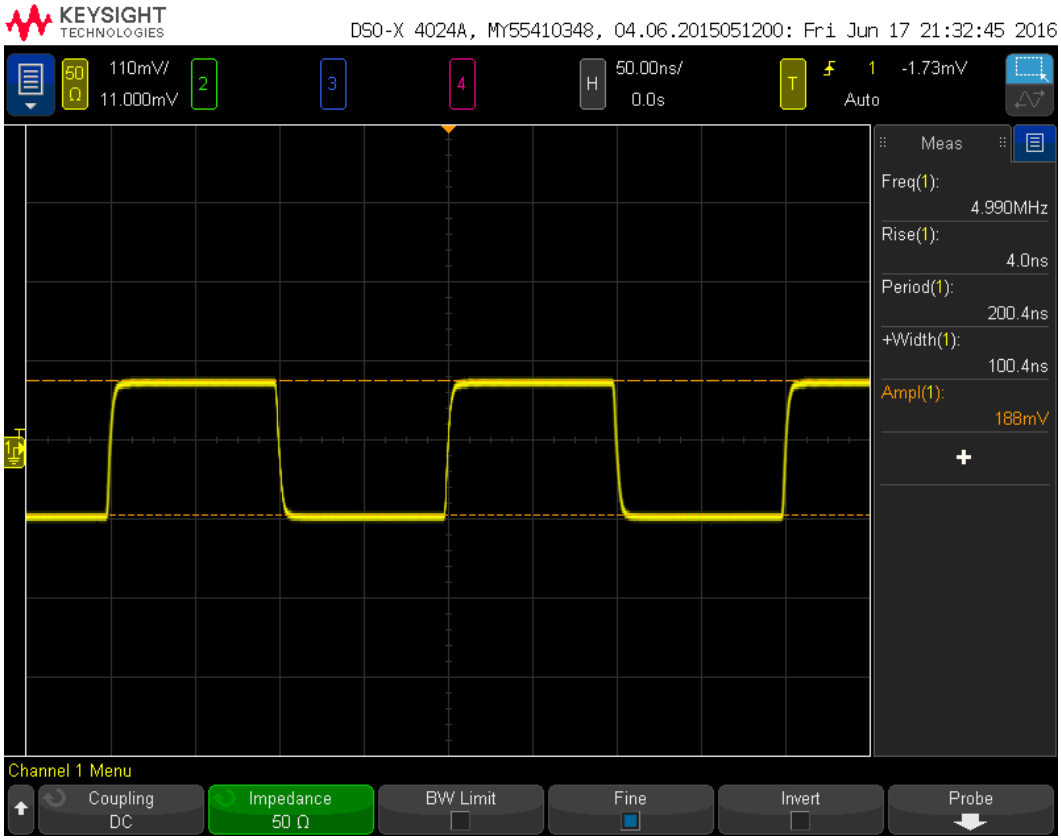


Figure 65: LVCMOS33-2mA-Slow Time Domain Behaviour

Signals 7 and 8 having the lowest drive strength settings, it can be seen that the signal waveform are closely representative of an RC circuit behaviour with the slower rise times and rounding of the edges of signals. The measured characteristics of the signals are detailed in Table 13.

Measured Attribute	LVCMOS33-24mA-Fast	LVCMOS33-24mA-Slow	LVCMOS33-2mA-Fast	LVCMOS33-2mA-Slow	Prefix
Rise Time	1.2	1.4	3.8	4	ns
Pulse Period	200.2	199.8	200	200.4	ns
Pulse Width	100	100	99.4	100.4	ns
Amplitude	217	217	188	188	mV
Frequency Breakpoint	265.36	227.36	83.76	79.5	MHz

Table 13: LVTTL Signal Characteristics

4.3.3.1 MSCR-001 – LVCMOS33 Signal Comparison

The four LVCMOS33 signals recorded in Figure 62 to Figure 65 all show a variation to the rise time of the signals based upon the attribute changed whether this be drive strength or edge rate. Altering the drive strength to the respective ends of their capabilities delivers a maximum variation of 3.6ns while the edge rate delivering 0.2ns.

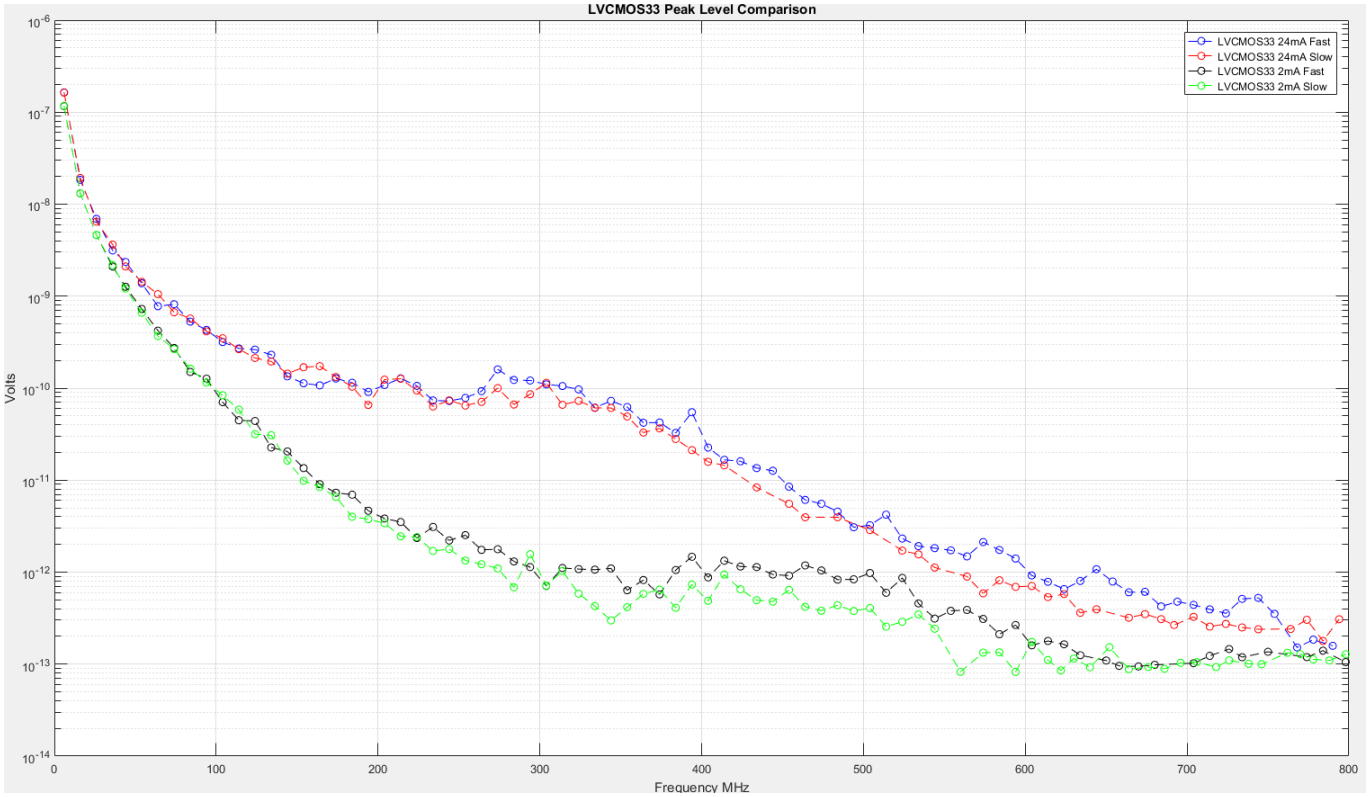


Figure 66: Peak Level Harmonic Comparison FPGA LVCMOS33 Signals

Plotting the peak level of harmonics of these signals shows a very similar result to that of the LVTTL comparative plot. The greater changes to amplitude of the harmonics again are attributable to the vast difference in drive strength setting of 24mA to 2mA, yet with a change in edge rate it can be seen that this influences the harmonic content more prominently towards the latter end of the observed spectrum shown in Figure 66 and Figure 24. The average level of the peak harmonic amplitudes support the initial observations, the average levels recorded for the LVCMOS33-24mA-Fast signal and the LVCMOS33-24mA-Slow signal are -47.18dBµV and -47.54dBµV respectively identifying a reduction of approximately 0.4dB between the fast and slow edge rates at the maximum drive strength setting. At the opposite end of the drive strength capabilities the LVCMOS33-2mA-Fast and LVCMOS33-2mA-Slow have an average peak harmonic level of -56.287dBµV and -58.23dBµV respectively. From the plots observed in Figure 58 and Figure 24 and the average level of the harmonic peaks it has been established that a difference between the peak harmonic levels can be identified through this method of analysis. It is reasonable from these results to predict that the level of emissions produced by the PCB under the array of I/O driver settings will be distinguishable and the results establishing a level of emissions produced by the FPGA I/O driver setting.

4.3.4 LVCMOS33 Theory v Practical Analysis

The LVCMOS33-24mA-Fast and LVCMOS33-2mA-Slow I/O driver settings have been chosen for comparison against the theoretical curve as illustrated in Figure 67 and Figure 68 respectively.

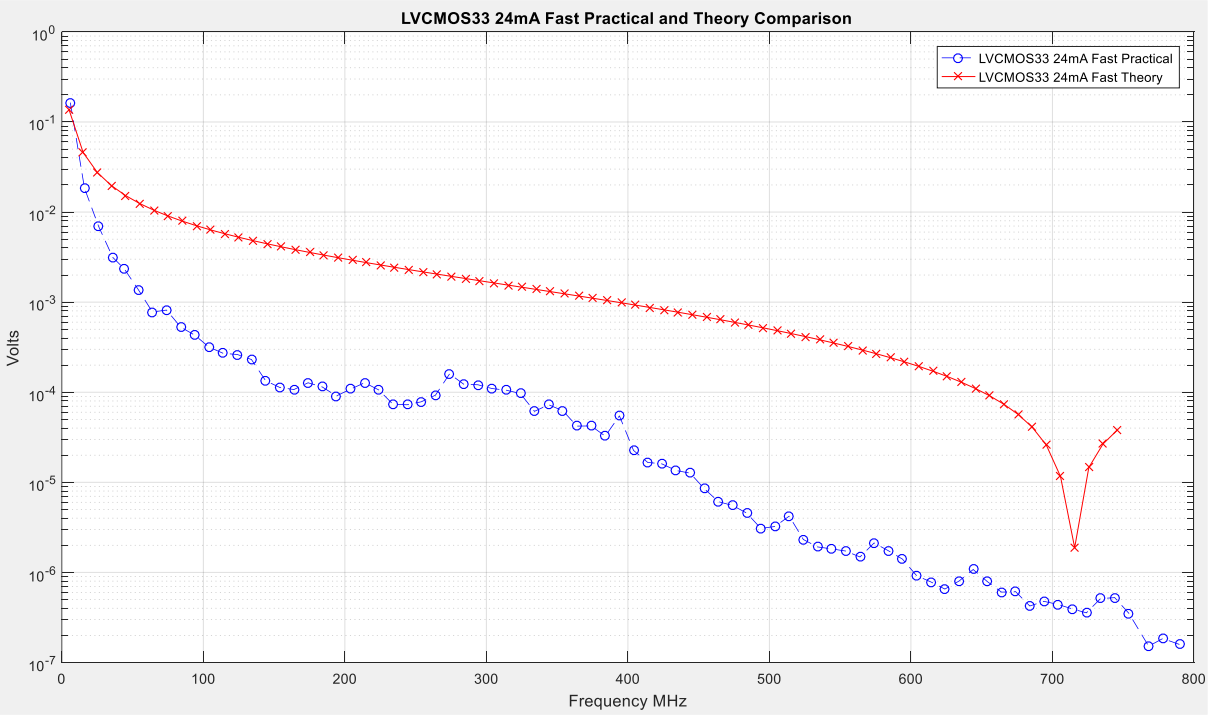


Figure 67: LVCMOS33-24mA-Fast Practical v Theory Comparison

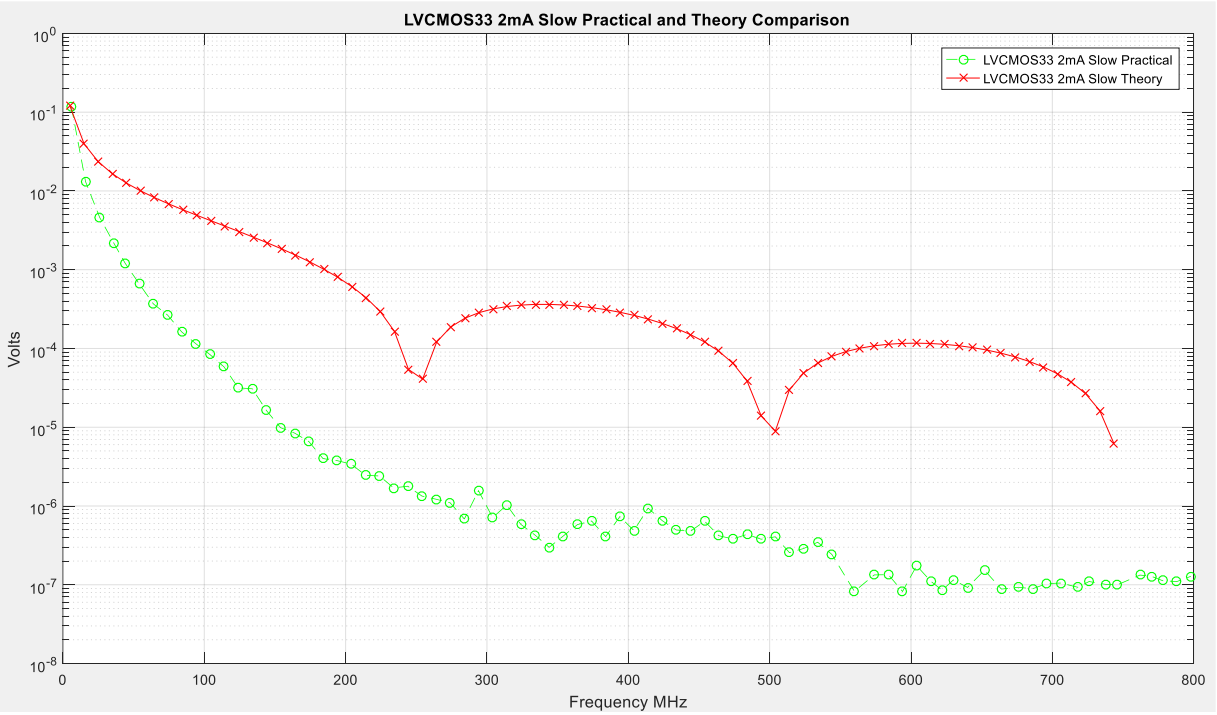


Figure 68: LVCMOS33-2mA-Slow Practical v Theory Comparison

Analysing the LVCMOS33 practical traces in comparison to the theoretical, it is showing a faster significant decay rate to the amplitude of the harmonics for the practical signal than it is the theoretical. The results show that the fundamental frequency harmonic for the practical signal is slightly less in amplitude than the theory. As the frequency of the harmonics increase the disparity between the theoretical and practical signals becomes greater. This attenuation is due to the attenuation of the practical signals as identified within section 1.1 when applying periodic signals to practical circuitry. Secondly, the attenuation is attributable to the second frequency decay point F_2 leading to a decay rate of 40dB/decade that is not seen with the theoretical representation.

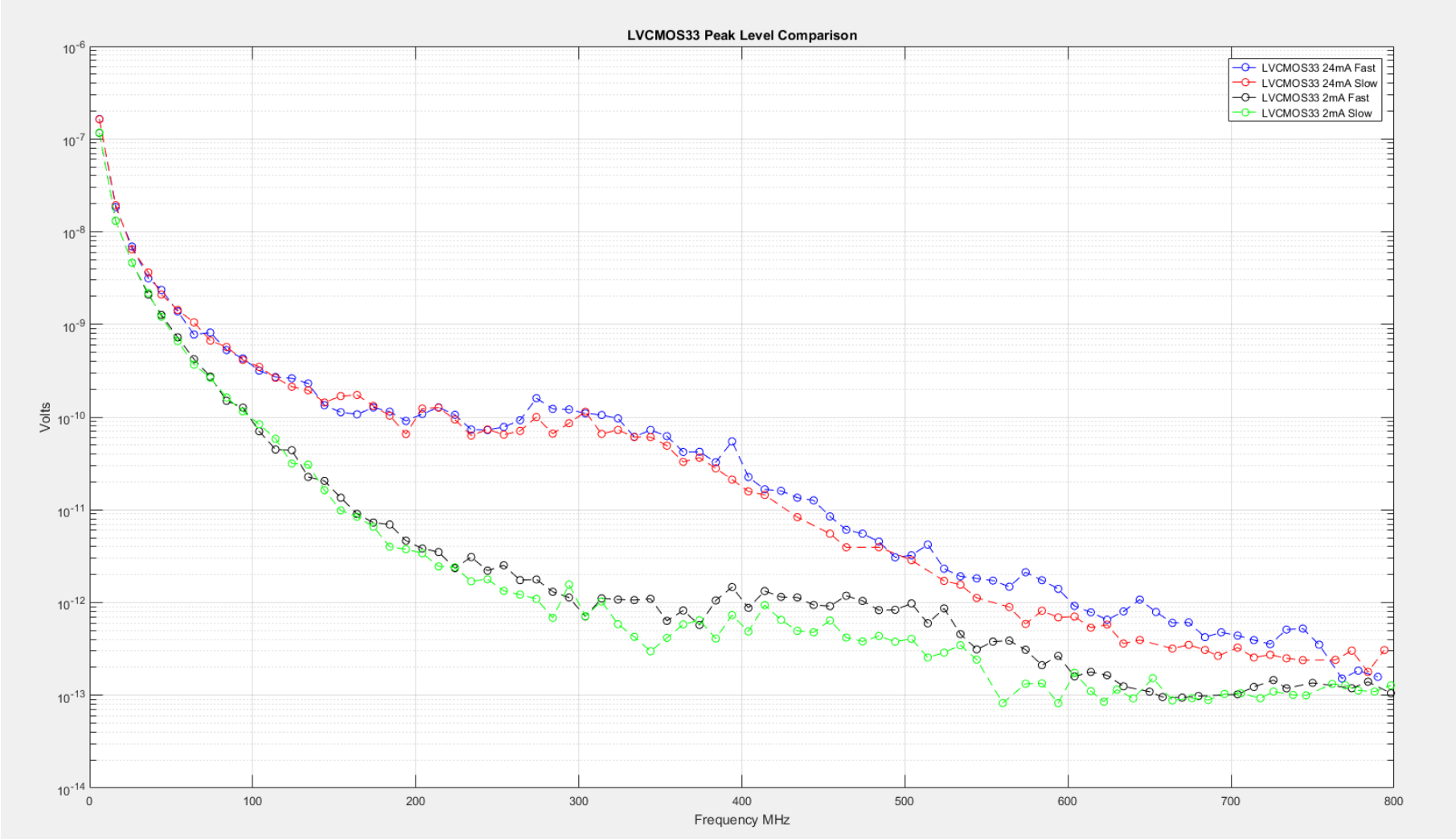


Figure 69: Peak Level Harmonics Comparison FPGA LVCMOS33 Signals

5 MSCR-001 – Radiated Emissions Testing

Section 5 details the radiated emissions testing of the MSCR-001 PCB inclusive of the testing setup, testing procedure and analysis of the results recorded. This testing span through the full range of the LVCMOS and LVTTL I/O settings that are available within the FPGA and the peak emissions produced have been recorded by a spectrum analyser and processed in MATLAB. The results have then been graphically and numerically assessed to reach a conclusion to the level of emissions a driver setting could introduce into the frequency spectrum and a reference guide to allow the designer to either reduce EMI during testing or control emissions during the design phase.

5.1 Test Setup

The setup used for the near field, radiated emissions testing is illustrated below in Figure 70 and Figure 71. The variables in terms of test equipment setup have been considered to record the highest levels of emissions from the PCB. These variables have been identified to be the four items listed below.

1. PCB Location
2. Antenna Location
3. Antenna Height
4. Antenna Orientation

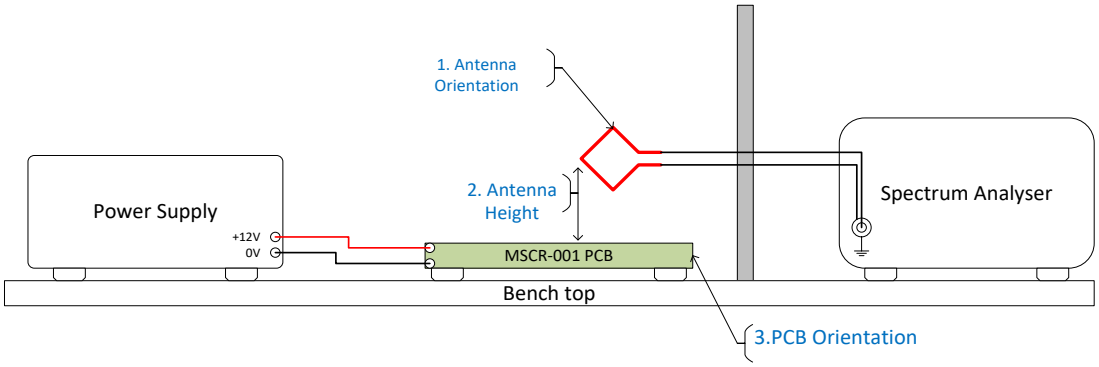


Figure 70: Radiated Emissions Test Setup

Figure 71: Radiated Emissions Testing Photograph

The location of the MSCR-001 PCB has been placed onto the bench top surface and fixed into place to prevent movement during testing. To establish the remaining variables, the antenna height, antenna location and antenna orientation have been established by programming the FPGA and adjusting them until the highest level of emissions was observed. The antenna height has been established to be 50mm above the PCB surface and fixed in place. The orientation and location of the antenna are set as shown in Figure 71. Restricting any movement from the PCB and recording the variables of the test setup will ensure that the measurements are repeatable.

5.1.1 Test Equipment

The test equipment used for the radiated emissions measurements is detailed below in Table 14.

Item	Manufacturer	Model	Specification
Variable PSU	GW Instek	K1 Module PL310	Voltage Range: 0 – 30V Maximum Current: 2A
DUT	N/A	MSCR-001	Voltages: 12V/5V/3.3V/2.5V/1.8V Current Drawn: 0.2A
DC Blocking Capacitor	N/A	N/A	Capacitance Value : 18nF
N-Type to SMa Connector	Emerson		Frequency Range: 0 – 18 GHz
RF Cable	Harbour Industries	M17/152-00001 MIL-DTL-27478	N/A
SMa to BNC Connector	N/A	N/A	N/A
H-Field Probe	R-A-M Test	H-Field Probe	Frequency Range 1Hz – 9GHz Nominal Impedance: 50Ω
Spectrum Analyser	Hewlett Packard		Frequency Range: 9KHz – 1.5 GHz Max Voltage: 100V DC

Table 14: Radiated Emissions Test Equipment

5.1.2 Spectrum Analyser Settings

The radiated emissions' testing has been carried out over a frequency range of 0-800 MHz, a reference level of 25dBµV and a resolution bandwidth of 300 kHz.

The unit that is usually applied to radiated emissions is dBµV/m, which pertains to the magnetic or electric field that is being measured. For the results displayed here the unit of dBµV has been used as this is for the purpose of a peak level comparison between different driver settings and not the overall field that they produce. This is valid for the purposes of this comparison if the dB ratio is kept consistent for all of the measurements obtained.

5.1.3 Test Procedure

The radiated emissions' testing identifies the emissions produced by the FPGA under the array of I/O driver settings within the LVCMOS and LVTTL standards.

Attribute	Variable Settings						
Drive Strength (mA)	24	16	12	8	6	4	2
Edge Rate	FAST			SLOW			
Logic Standard	LVCMOS			LVTTL			
Voltage Level CMOS	LVCMOS33 (3.3V)	LVCMOS25 (2.5V)		LVCMOS18 (1.8V)		LVCMOS15 (1.5V)	LVCMOS12 (1.2V)
Voltage Level TTL	LVTTL (3.3V)						

Table 15: I/O Properties for Spartan 6

The I/O settings listed above in Table 15 form the criteria for the radiated emissions testing; each of the settings has been tested and only changing one property at a time between measurements. This ensures that any changes to the level of emissions produced are attributable to the I/O properties that have changed and not a combined effect of multiple settings changing at the same time.

5.1.4 Radiated Emissions PCB Configuration

For the radiated emission testing, the FPGA will be driving an on board PCB trace with a characteristic impedance of 50 Ω with a 5MHz clock signal shown in Figure 72. The PCB track impedance has been controlled using the AppCAD tool to ensure that the PCB traces are 50Ω. The trace is terminated with a 50Ω resistor to inhibit reflections. A terminated PCB track has been chosen for the radiated emissions testing as this is representative of how designs would be implemented in a real world application.

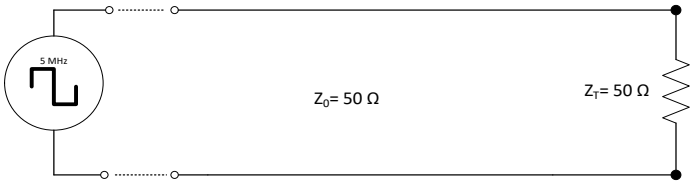


Figure 72: Radiated Emissions Cicuitry

5.1.5 Order of Testing

The radiated emissions' testing is split into three sections; giving an overview of how each of the variable attributes influences the level of emissions. The three sections analyse each of the variables that can be changed; logic standard, drive strength and edge rate. Assessing each of the attributes individually will give an indication of the magnitude of change to the level of emissions produced. A quantifiable level of emissions has been established by obtaining the peak levels of harmonics recorded from each driver setting, plotting them comparatively and then taking an average level to establish which setting produces the greatest EMI across the observed spectrum. The following comparisons will establish a quantifiable overview of EMI produced by this FPGA through the array of driver settings identified in Table 15:

1. Logic Standard Emissions Testing
2. Driver Strength Emissions Testing
3. Edge Rate Emissions Testing

This testing provides a design engineer with a point of reference to approach a design from the conceptual stage; having some knowledge of how the design choices will affect the level of emissions produced. The results seen below are reflective of the voltage seen on the coil of the H-field probe and it is used to provide a comparative measurement on how the logic standards and settings stack up against each other in terms of the emissions produced.

5.2 Results Anomalies and Equipment Limitations

Throughout the results obtained from the logic standard, drive strength and edge rate radiated emissions testing. There are certain frequencies where the peak levels recorded shift between the two subjects i.e. the CMOS technology providing a higher level of emissions than the TTL and vice versa. This can be attributed to the driver themselves producing a higher level of emissions or limitations of the equipment that has been used. In terms of the drivers causing an increase to the emissions produced the particular standards are required to produce a fixed propagation delay and switching speed to interface with the respective logic. It is from this additional functionality of switching speed that causes an increase to the overall radiated emissions produced by the driver settings. As for the unforeseen increases to emissions, i.e. the TTL standard producing lower emissions than the CMOS, this can be attributed to the physical hardware and the measurement equipment used. Due to the fact that this is physical hardware and the inclusion of even harmonics into the spectrum there are more frequencies that radiating from the PCB trace. The characteristics of the PCB trace have the potential to influence the reflection coefficient and the reflections add to the level of emissions produced. Finally the measurement equipment used has some impact on the 'peak level' of emissions recorded. The chosen spectrum analyser has the capability of recording a maximum of 401 points per measurement. When recording the peaks of the harmonics or emissions present and the limitation of the measurement equipment the true peak is not recorded but a point approaching this on the adjacent positive and negative slopes. As a result there may be peaks that appear within the plots that are actually higher than what has been recorded, leading to the results that may appear incorrectly that the CMOS technology produces a peak level in a certain frequency range that emissions are higher than the TTL.

5.3 Logic Standard Testing

The logic standard testing compares the levels of EMI across the LVTTL, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15 and LVCMOS12 I/O standards that are available within the FPGA. To establish a more accurate understanding of how the peak level of emissions varies between I/O driver settings three comparisons have been made. These three comparisons set the drive strength and edge rate at fixed values throughout their capabilities to give a broad range of how the emissions vary within the I/O logic standard setting.

5.3.1 Comparison One – Maximum Settings

The first comparison is with the maximum drive strength setting of '24mA' and an edge rate set to 'Fast' and fixed across the available technologies. The LVCMOS15 & LVCMOS12 technologies have been omitted from this testing comparison due to the restrictions of the FPGA not allowing the drive strength setting of '24mA' for these two logic standards. The signals that have been plotted for this comparison are detailed below in Table 16.

Trace No.	Technology	Drive Strength	Edge Rate	Average Noise Level dBµV
1	LVTTL	24mA	Fast	-59.99
2	LVCMOS33	24mA	Fast	-63.75
3	LVCMOS25	24mA	Fast	-63.47
4	LVCMOS18	24mA	Fast	-62.92

Table 16: Logic Standard Testing – Maximum I/O Setting Results

5.3.1.1 Results

From the traces plotted in Figure 73, it can be observed that the peak level of emissions produced from the LVTTL I/O standard is at a higher level along the observed spectrum. From each of the peak levels of emissions recorded at each driver setting an average has been taken to identify which I/O logic standard produces the highest average level of emissions in the frequency domain.

The average level of emissions has identified that the LVTTL driver setting produces the highest level on average across the observed spectrum. The LVTTL I/O logic standard setting averages approximately -60dBµV almost +3dB higher than that of the LVCMOS standards. The LVCMOS standards average at between -62.9dBµV to -63.75dBµV showings a variation to the peak level emissions of 0.85dB. Figure 73 has a 50dB range on its Y-axis which makes identifying any accurate understanding of the variation to emissions very difficult. To have a more accurate illustration of how much the peak level of emissions increases or decreases between I/O logic standards, the peak values are stored within a one dimensional array and these peak values will be compared to the LVTTL logic standard setting to determine just how much variation occurs.

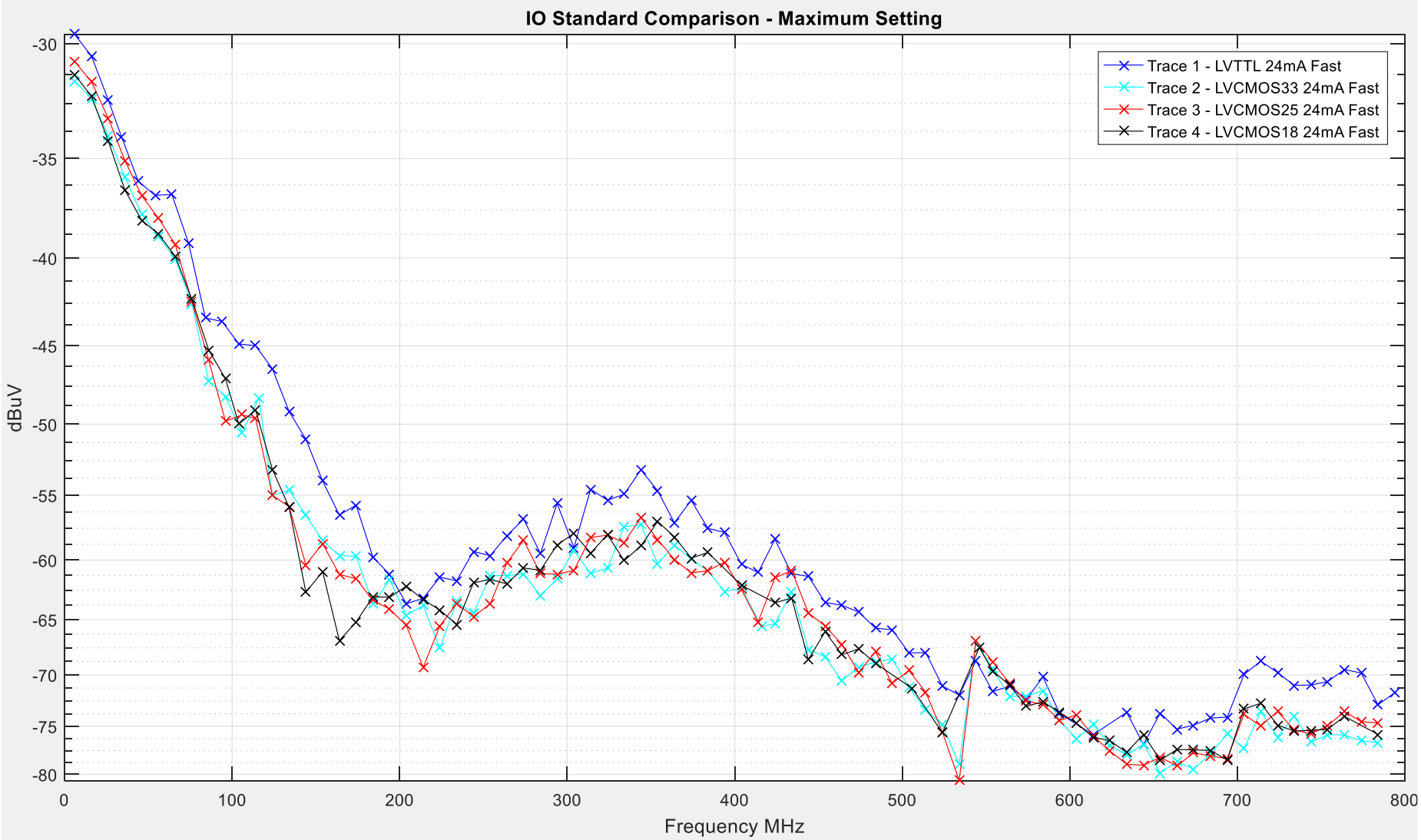


Figure 73: Logic Standard Testing - Maximum Setting Radiated Emissions Comparison

5.3.1.2 Logic Standard Testing - Delta in Harmonic Peak Levels (Max Setting)

Examining the difference between the traces shown in Figure 73 the following relationships have been calculated. The vectors that hold the peak levels for the emissions are identified by A_n, and each comparison is between the traces is identified by Δ_n then;

- A_{LVTTL} = Peak harmonics vector LVTTL
- $A_{LVCMOS33}$ = Peak harmonics vector LVCMOS33
- $A_{LVCMOS25}$ = Peak harmonics vector LVCMOS25
- $A_{LVCMOS18}$ = Peak harmonics vector LVCMOS18

Using the LVTTL logic standard as the baseline for the testing Δ1, Δ2 and Δ3 shows the difference in peak emissions recorded for comparison 1.

Δ1 illustrated below in Figure 74 shows;

$$\Delta_1 = \boldsymbol{A_{LVTTL} - A_{LVCMOS33}}$$

Equation 11: Delta between LVTTL and LVCMOS33 (Comparison 1)

The maxima seen within this data plot is seen at around 120MHz, and has an amplitude of 8.6dB. This translates that the LVTTL I/O standard contains a peak harmonic that is +8.6B higher than the LVCMOS33 standard with the same drive strength and edge rate. The LVCMOS33 I/O standard does contain harmonics that are higher than the LVTTL I/O standard, between 500 – 600MHz three harmonic peaks were recorded to be greater than the LVTTL standard and a minima of -2.11dB was recorded at approximately 540MHz in Figure 74.

Δ2 illustrated below in Figure 75 shows;

$$\Delta_2 = \boldsymbol{A_{LVTTL} - A_{LVCMOS25}}$$

Equation 12: Delta between LVTTL and LVCMOS25 (Comparison 1)

The maxima seen within this data plot is seen at around the 120MHz frequency and has an amplitude of 9.63dB. This translates that the LVTTL I/O standard contains a peak harmonic that is +9.63dB higher than the LVCMOS25 standard with the same drive strength and edge rate. The LVCMOS25 I/O standard does contain harmonics that are higher than the LVTTL I/O standard, between 500 – 600MHz three harmonic peaks were recorded to be greater than the LVTTL standard with a minima of -2.8dB was recorded at approximately 540MHz in Figure 75.

Δ3 illustrated below in Figure 76 shows;

$$\Delta_3 = \boldsymbol{A_{LVTTL} - A_{LVCMOS18}}$$

Equation 13: Delta between LVTTL and LVCMOS18 (Comparison 1)

The maxima seen within this data plot is seen at around the 120MHz frequency and has an amplitude of 11.6dB. This shows that the LVTTL I/O standard contains a peak harmonic that is +11.6dB greater than the LVCMOS18 standard with the same drive strength and edge rate. The LVCMOS25 I/O standard does contain harmonics that are higher than the LVTTL I/O standard, between 180 – 300MHz and 500 – 600MHz harmonic peaks were recorded to be below the LVTTL standard with a minima of -1.6dB was recorded at approximately 540MHz in Figure 76.

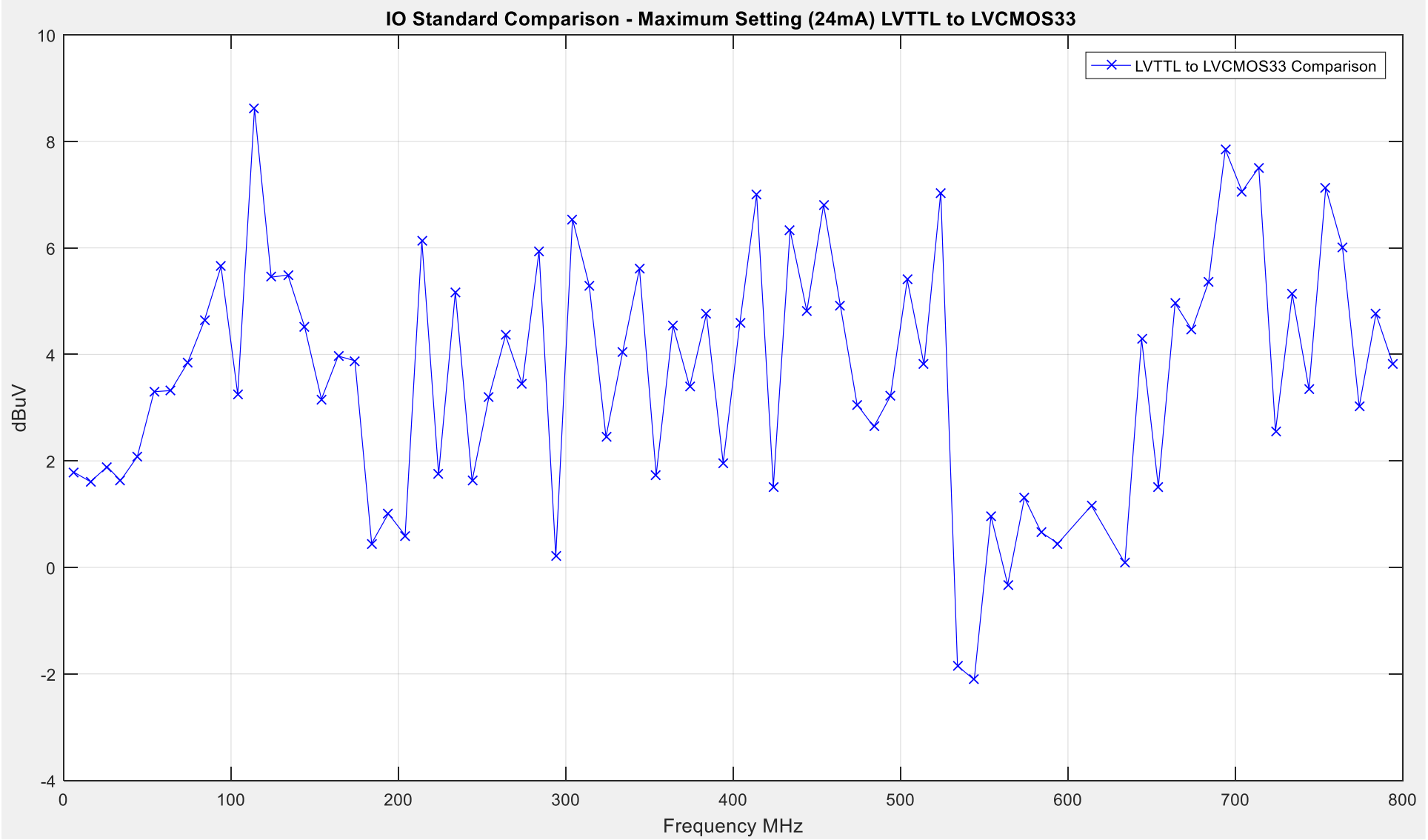


Figure 74: Logic Standard Comparison (Max Setting) - Peak Harmonic Difference I/O (LVTTL to LVCMOS33)

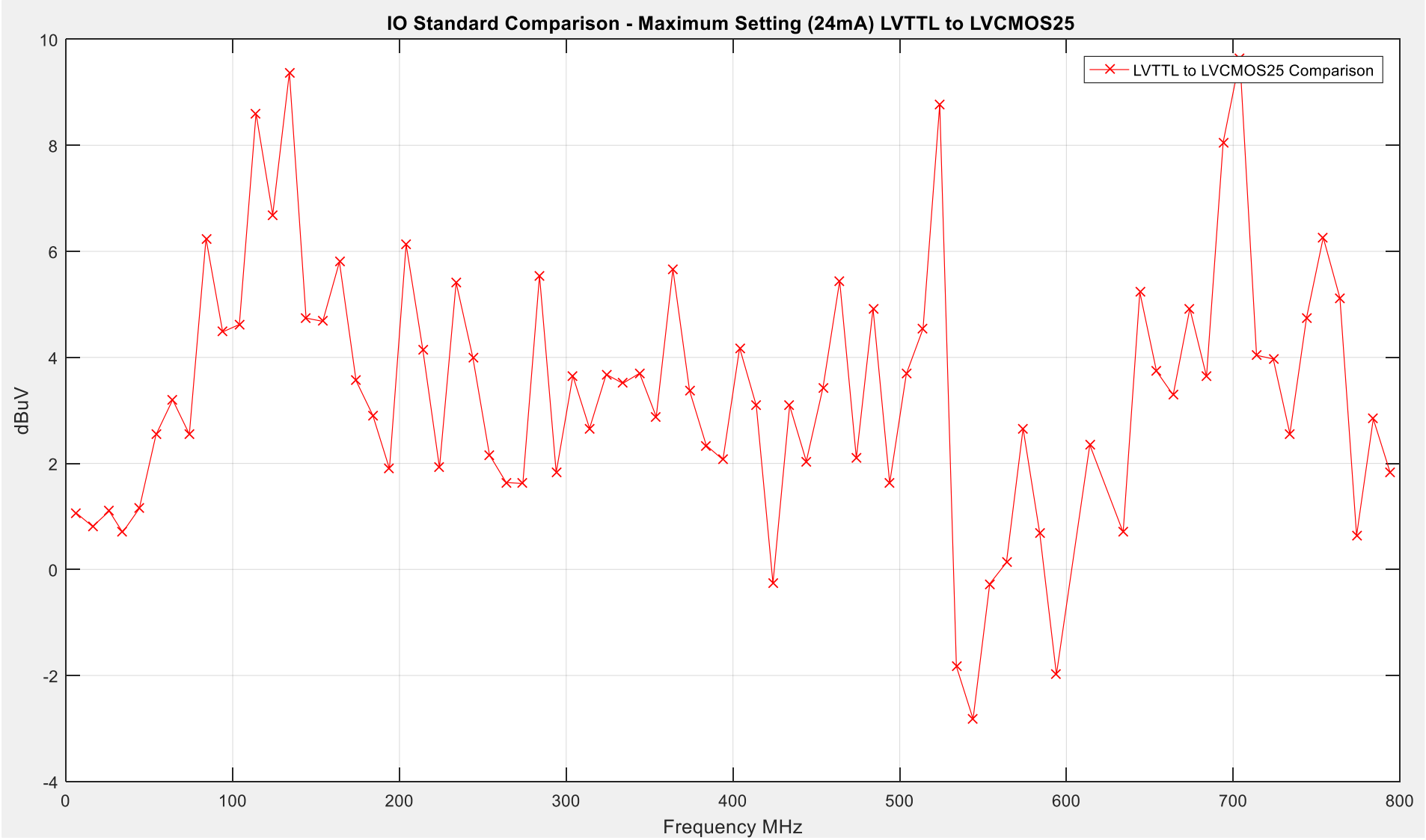


Figure 75: Logic Standard Comparison (Max Setting) - Peak Harmonic Difference I/O (LVTTL to LVCMO25)

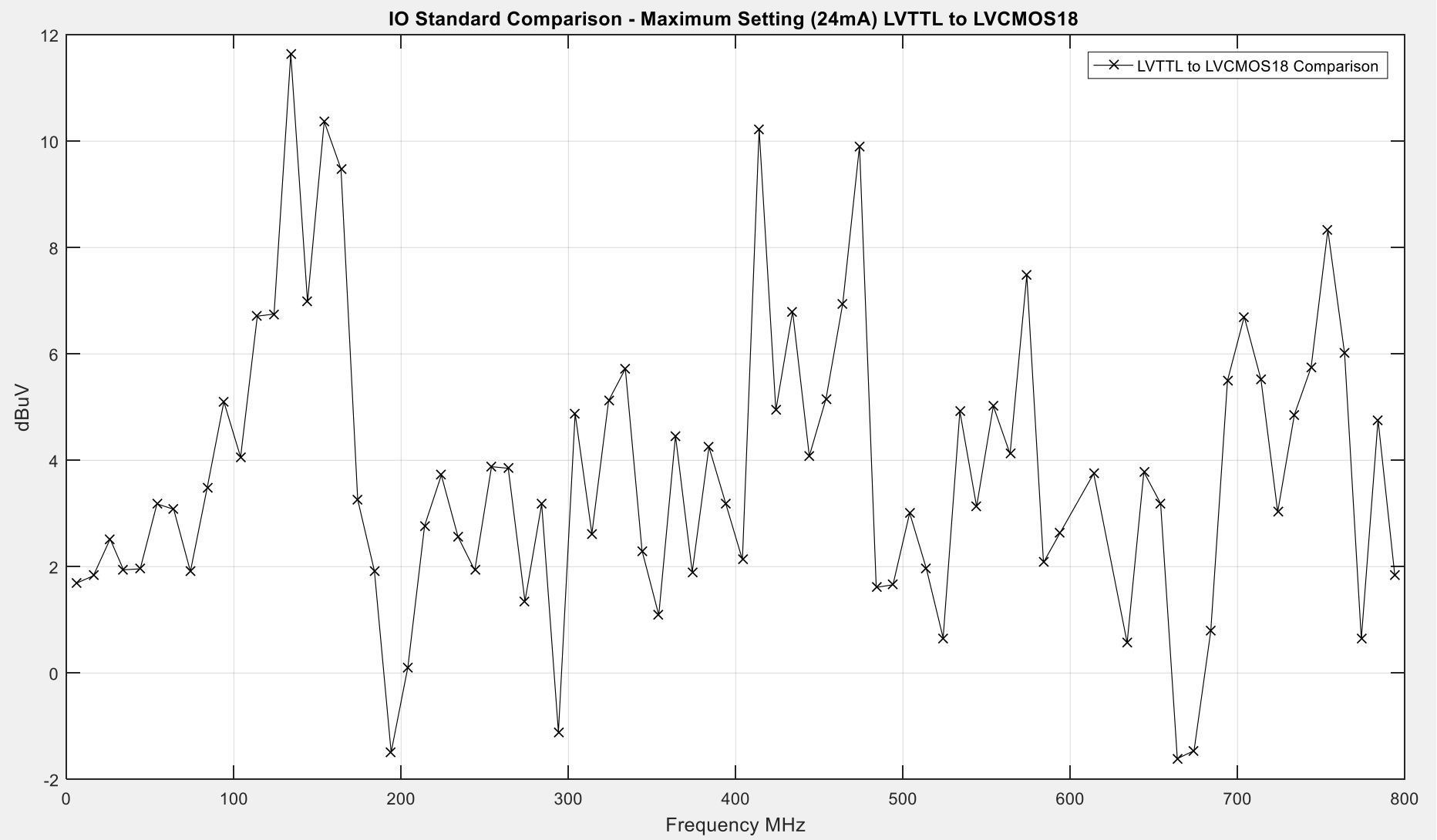


Figure 76: Logic Standard Comparison (Max Setting) - Peak Harmonic Difference I/O (LVTTL to LVCMOS18)

5.3.2 Comparison Two – Default Settings

The second of the emissions measurement comparisons is with the default setting that is applied to the FPGA I/O if the user constraints file is not customised to a certain configuration. This default setting of the I/O output buffers within the Spartan 6 FPGA is LVCMOS25 with'12mA' drive strength and 'Fast' edge rate.

Trace No.	Technology	Drive Strength	Edge Rate	Average Noise Level dB
1	LVTTL	12mA	Fast	-61.47
2	LVCMOS33	12mA	Fast	-65.16
3	LVCMOS25	12mA	Fast	-65.05
4	LVCMOS18	12mA	Fast	-64.48
5	LVCMOS15	12mA	Fast	-65.94
6	LVCMOS12	12mA	Fast	-65.35

Table 17: Logic Standard Testing – Default I/O Setting Results

5.3.2.1 Results

The traces displayed in Figure 77, show the peak levels of emissions from the driver settings identified in Table 17. Again observing the plots it can be seen the emissions produced from the LVTTL standard produces the highest level of emissions across the spectrum and the average level of emissions produced supports this observation with approximately 61.5dBµV. The LVCMOS technologies range vary by 1.5dBµV, with the LVCMOS15 having the lowest average at 64.5dBµV and the LVCMOS18 has the highest at 65.94dBµV. The difference again between the LVCMOS and LVTTL technologies averaging at +3dBµV identifies the LVTTL standard as significantly in terms of emissions produced.

As before the range of 50dB on the Y-axis in Figure 77 makes identifying the magnitude of any delta between the traces very difficult so a comparison between each of the driver settings is shown below.

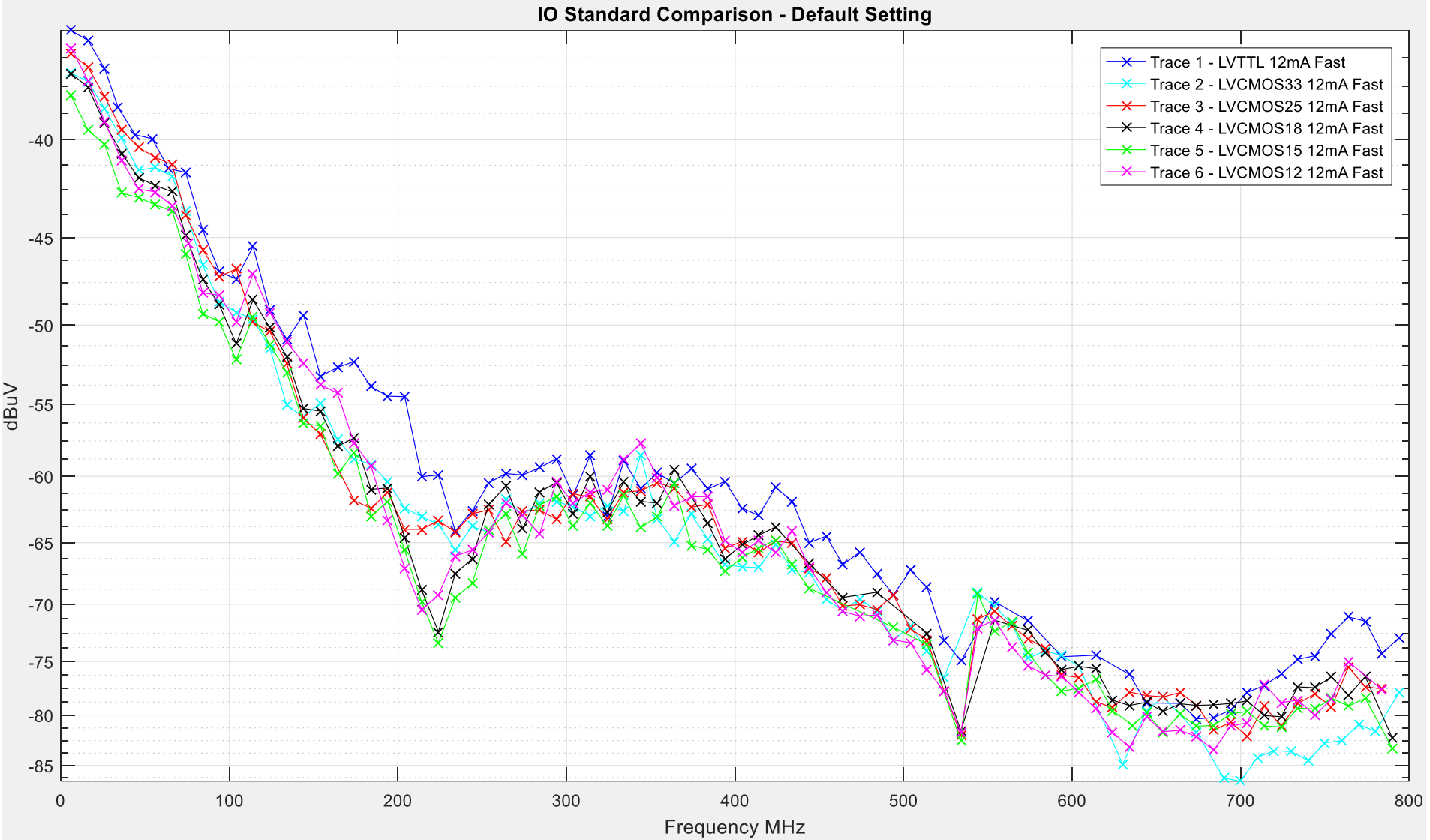


Figure 77: Logic Standard Testing - Default Setting Radiated Emissions Comparison

5.3.2.2 Logic Standard Testing Delta in Harmonic Peak Levels (Default Setting)

If the vectors that hold the peak levels for the harmonics are identified by A_n and each comparison is between the traces is identified by Δ_n then;

- A_{LVTTL} = Peak harmonics vector LVTTL
- $A_{LVCMOS33}$ = Peak harmonics vector LVCMOS33
- $A_{LVCMOS25}$ = Peak harmonics vector LVCMOS25
- $A_{LVCMOS18}$ = Peak harmonics vector LVCMOS18
- $A_{LVCMOS15}$ = Peak harmonics vector LVCMOS15
- $A_{LVCMOS12}$ = Peak harmonics vector LVCMOS12

Using the LVTTL logic standard as the baseline for the testing Δ4, Δ5, Δ6, Δ7 and Δ8 shows the difference in peak emissions recorded for comparison 2.

Δ4 illustrated below in Figure 78 shows;

$$\Delta_4 = A_{LVTTL} - A_{LVCMOS33}$$

Equation 14: Delta between LVTTL and LVCMOS33 (Comparison 2)

The maxima seen within Figure 78 is seen at around 700 MHz, and has an amplitude of 11.99dB. This translates that the LVTTL I/O standard contains a peak harmonic that is +11.99B higher than the LVCMOS33 standard with the same drive strength and edge rate. None of the emissions recorded for the LVCMOS33 setting is higher than the LVTTL logic standard.

Δ5 illustrated below in Figure 79 shows;

$$\Delta_5 = A_{LVTTL} - A_{LVCMOS25}$$

Equation 15: Delta between LVTTL and LVCMOS25 (Comparison 2)

The maxima recorded in Figure 79 is seen at around 170 MHz, and has an amplitude of 10.12dB. This translates that the LVTTL I/O standard contains a peak harmonic that is +10.12dB higher than the LVCMOS25 standard with the same drive strength and edge rate. None of the emissions recorded for the LVCMOS25 setting is higher than the LVTTL logic standard.

Δ6 illustrated below in Figure 80 shows;

$$\Delta_6 = A_{LVTTL} - A_{LVCMOS18}$$

Equation 16: Delta between LVTTL and LVCMOS18 (Comparison 2)

The maxima recorded in Figure 80, is seen at around 450 MHz, and has an amplitude of 14.8dB. This translates that the LVTTL I/O standard contains a peak harmonic that is +14.8dB higher than the LVCMOS18 standard with the same drive strength and edge rate. None of the emissions recorded for the LVCMOS18 setting is higher than the LVTTL logic standard.

Δ7 illustrated below in

Figure 81 shows

$$\Delta_7 = A_{LVTTL} - A_{LVCMOS15}$$

Equation 17: Delta between LVTTL and LVCMOS15 (Comparison 2)

The maxima seen in

Figure 81 is seen at around 450 MHz, and has an amplitude of 16.8dB. This translates that the LVTTL I/O standard contains a peak harmonic that is +16.8dB higher than the LVCMOS15 standard with the same drive strength and edge rate. None of the emissions recorded for the LVCMOS15 setting is higher than the LVTTL logic standard.

Δ8 illustrated below in Figure 82 shows

$$\Delta_8 = A_{LVTTL} - A_{LVCMOS12}$$

Equation 18: Delta between LVTTL and LVCMOS12 (Comparison 2)

The maxima seen in Figure 82 is seen at around 190 MHz, and has an amplitude of 12.5dB. This translates that the LVTTL I/O standard contains a peak harmonic that is +12.5dB higher than the LVCMOS18 standard with the same drive strength and edge rate. The minima for this plot is -3.21dB, this translates to the LVCMOS12 logic standard having a peak level of emissions that is 3.21dB higher than the LVTTL at 190MHz.

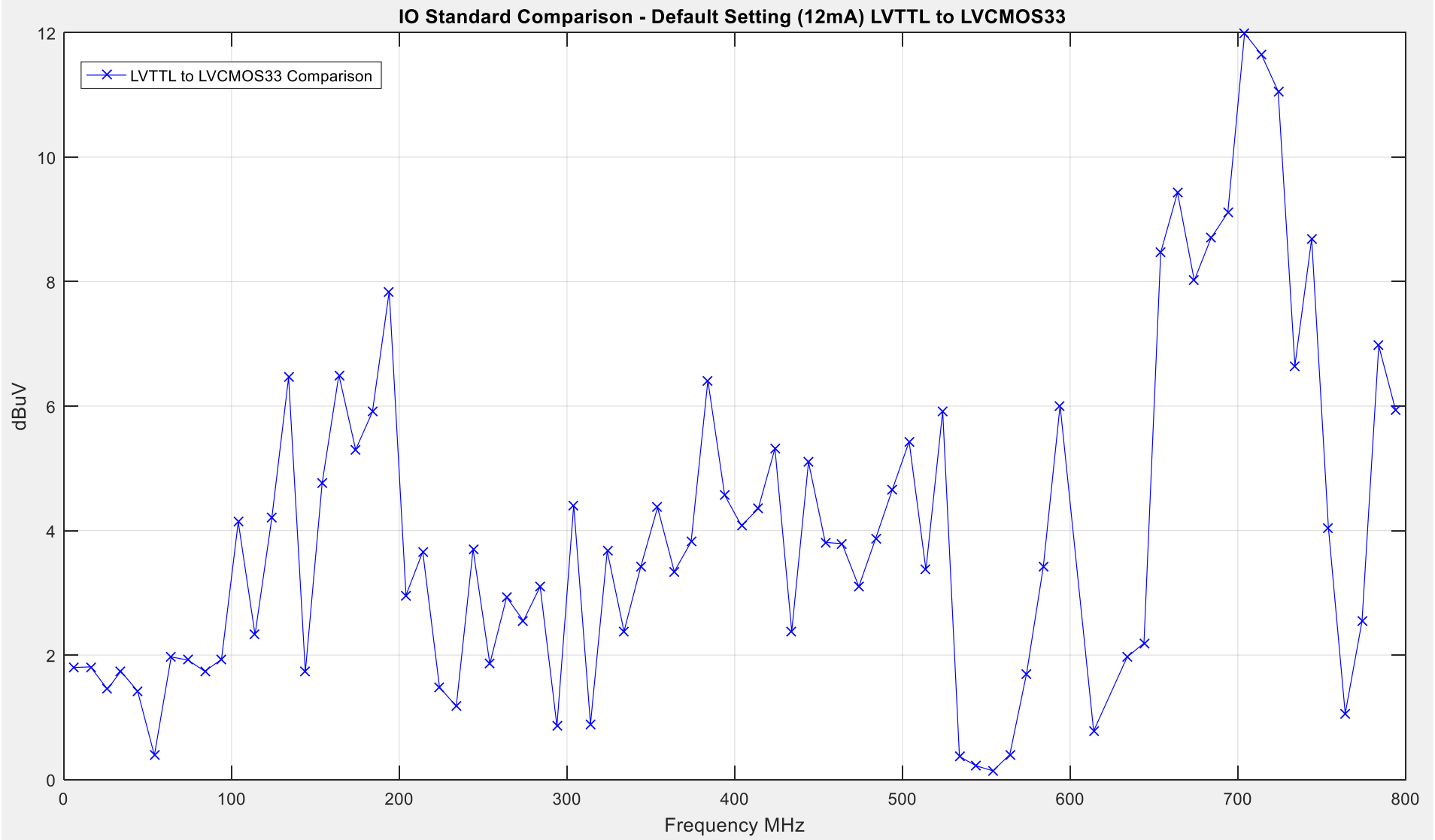


Figure 78: Peak Harmonic Difference (LVTTL to LVCMOS33)

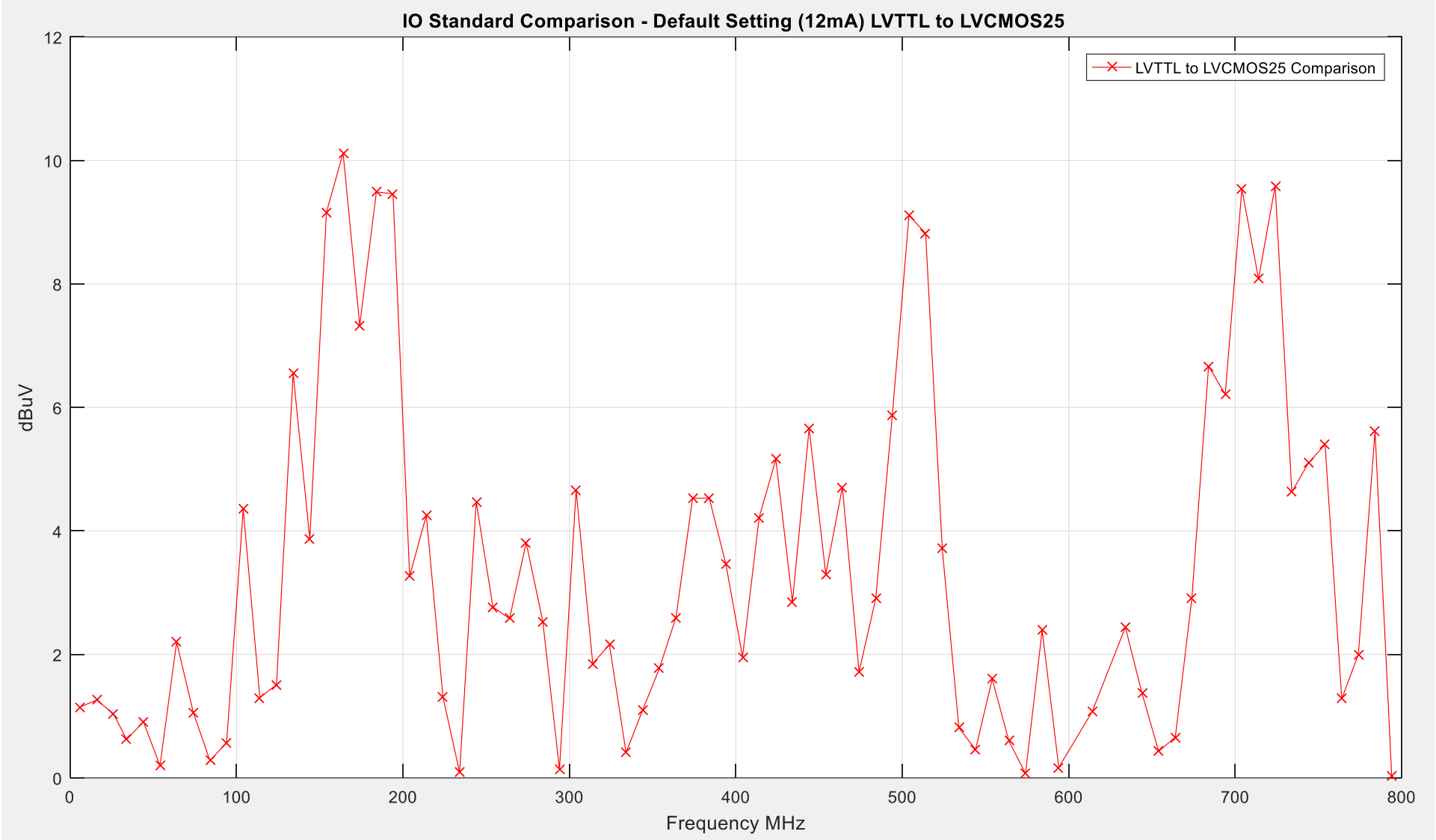


Figure 79: Peak Harmonic Difference (LVTTL to LVCMOS25)

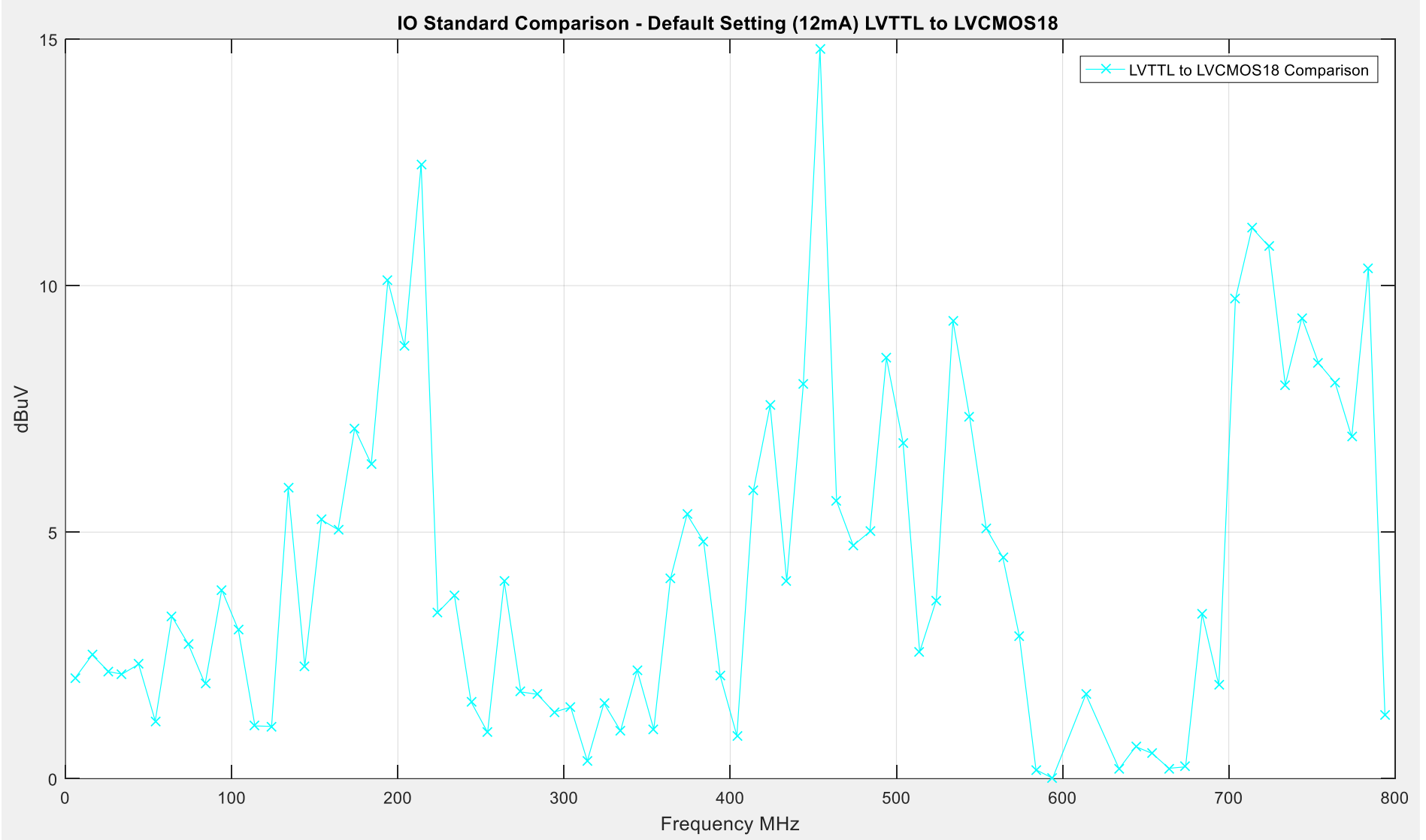


Figure 80: Peak Harmonic Difference (LVTTL to LVCMOS18)

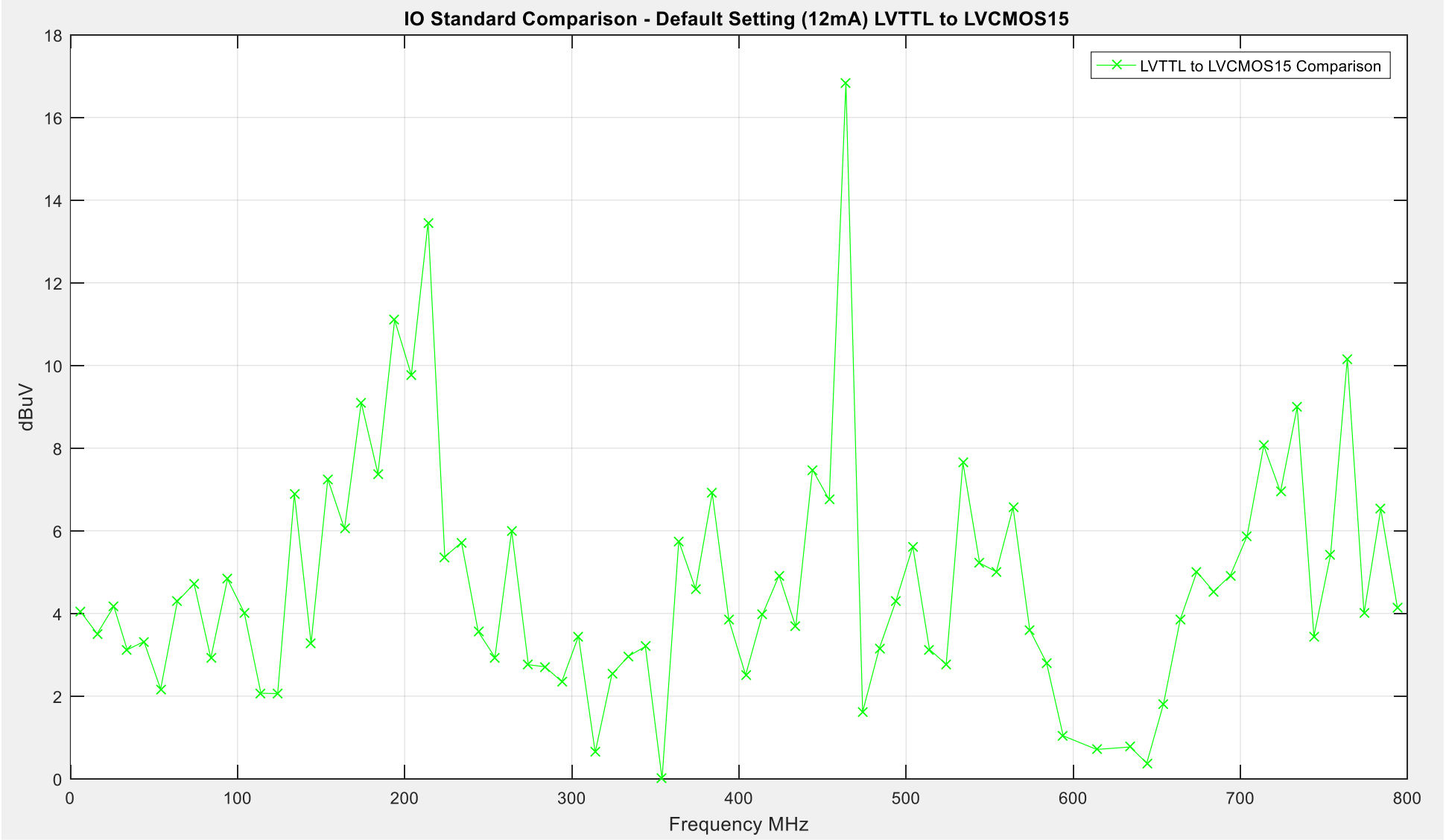


Figure 81: Peak Harmonic Difference (LVTTL to LVCMOS15)

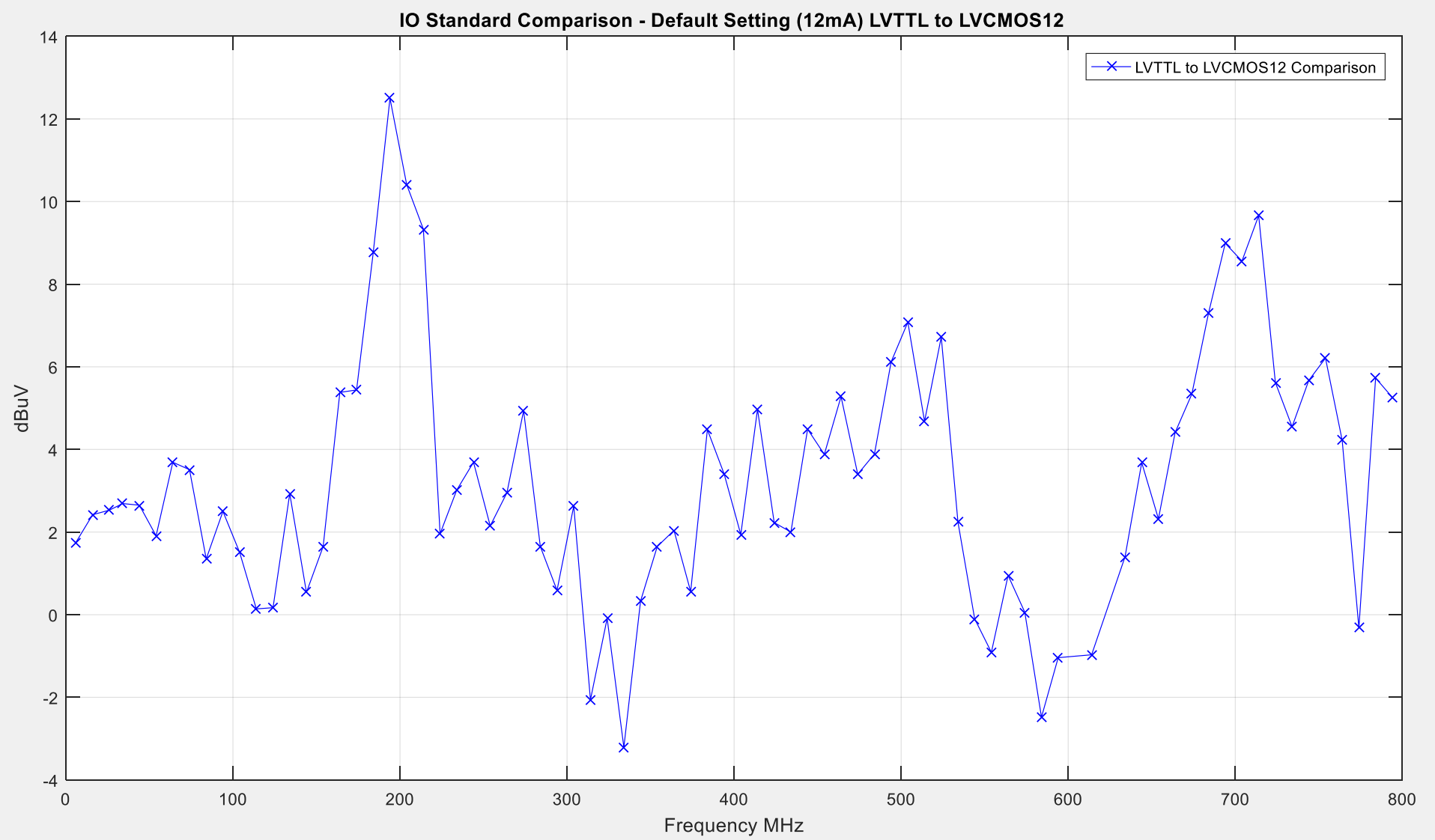


Figure 82: Peak Harmonic Difference (LVTTL to LVCMOS12)

5.3.3 Comparison Three – Minimum Settings

The third of the logic standard emissions measurements is with the minimum drive strength '2mA' and 'slow' edge rate setting that can be applied to the FPGA. The details of these settings are listed below in Table 18 inclusive of the average level taken from the peak harmonic vector.

Trace No.	I/O Standard	Drive Strength	Edge Rate	Average Noise Level dB
1	LVTTL	2mA	Slow	-73.8976
2	LVCMOS33	2mA	Slow	-73.3359
3	LVCMOS25	2mA	Slow	-72.6679
4	LVCMOS18	2mA	Slow	-73.7525
5	LVCMOS15	2mA	Slow	-74.6304
6	LVCMOS12	2mA	Slow	-73.2297

Table 18: Logic Standard Testing – Minimum I/O Setting

5.3.3.1 Results

The emissions produced by the I/O standards at the minimum drive strength and edge rate are shown in Figure 83. The variation between the peak levels of emissions is predominantly different to what was seen in comparison 1 and comparison 2. The most notable difference is that at the lower frequency range up to approximately 110MHz the LVTTL logic standard produces the lowest level of emissions of all the logic standards with approximately -73.9dBµV. From the average level taken from each of the peak harmonic vectors, the variation is much closer than the other comparisons with a difference of approximately 1.2dBµV. The highest average level of emissions recorded was shown to be from the LVCMOS25 standard with -72.66dBµV and the lowest was from the LVCMOS15 standard recording approximately -74.63dBµV. Giving a variation of 2dBµV. Again due to the range on the Y-axis identifying any difference between the peak levels is difficult, as a result a closer inspection of the delta between each peak levels has been done. The peak levels of emissions obtained from the LVTTL logic standard have been used a baseline to identify the disparity between the emissions produced.

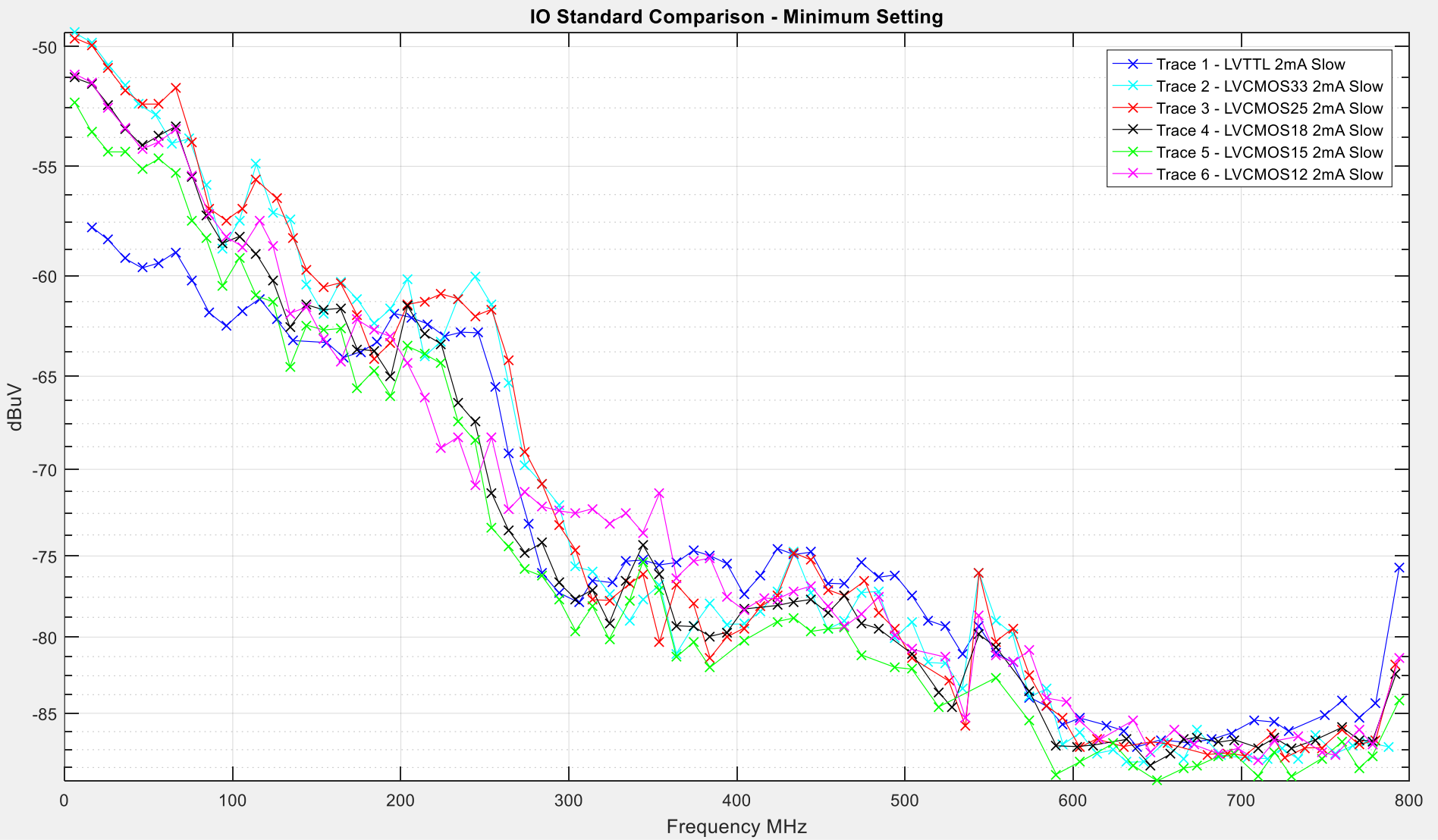


Figure 83: Logic Standard Testing - Minimum Setting Radiated Emissions Comparison

5.3.3.2 Delta in Harmonic Peak Levels (Default Setting)

Figure 83 illustrates the differences between the I/O logic standard settings with a drive strength fixed at a setting of '2mA' and the edge rate setting fixed to 'Slow'. As before the range of 50dB makes identifying the amplitude of this delta very difficult so a comparison between each of the driver settings is shown below.

If the vectors that hold the peak levels for the harmonics are identified by A_n and the difference between the peak levels is identified by Δ_n then;

- A_{LVTTL} = Peak harmonics vector LVTTL
- $A_{LVCMOS33}$ = Peak harmonics vector LVCMOS33
- $A_{LVCMOS25}$ = Peak harmonics vector LVCMOS25
- $A_{LVCMOS18}$ = Peak harmonics vector LVCMOS18
- $A_{LVCMOS15}$ = Peak harmonics vector LVCMOS15
- $A_{LVCMOS12}$ = Peak harmonics vector LVCMOS12

Δ4 illustrated below in Figure 84 shows;

$$\Delta_9 = A_{LVTTL} - A_{LVCMOS33}$$

Equation 19: Delta between LVTTL and LVCMOS33 (Comparison 3)

From Figure 84, the LVTTL logic standard produces emissions that are less than the LVCMOS33 logic standard. The minima recorded at this frequency -11.71dB at 240MHz, translating that the LVCMOS33 standard contains a peak emissions that is 11.71dB greater than the LVTTL logic standard. The maxima recorded for the plot in Figure 84 is 10.76dB at 740MHz meaning that the LVTTL logic standard contain an emission peak of 10.76dB at this particular frequency.

Δ5 illustrated below in Figure 85 shows;

$$\Delta_{10} = A_{LVTTL} - A_{LVCMOS25}$$

Equation 20: Delta between LVTTL and LVCMOS25 (Comparison 3)

From Figure 85, the LVTTL logic standard produces emissions that are less than the LVCMOS25 standard up to the 300MHz region, with the exception of 3 emission peaks around the 170MHz region. The minima recorded in the 0 - 300MHz region is -11.8dB, which translates to the LVTTL logic standard being 11.8dB lower than the LVCMOS25 standard at this point. The maxima within this comparison is 11.15dB at approximately 740MHz, which translates to the LVTTL logic standard containing emissions peaks that are 11.5dB higher than the LVCMOS25 logic standard.

Δ6 illustrated below in Figure 86 shows

$$\Delta_{11} = A_{LVTTL} - A_{LVCMOS18}$$

Equation 21: Delta between LVTTL and LVCMOS18 (Comparison 3)

From Figure 86, the LVTTL logic standard produces emissions that are less than the LVCMOS18 standard up to the 300MHz region, with the exception of a handful of emission peaks around the 170 – 220MHz region. The minima recorded within 0-300MHz region is -6.94dB, which translates to the LVTTL logic standard being 6.94dB lower than the LVCMOS18 standard at this point. The maxima within this comparison is 12.58dB at approximately 740MHz, which translates to the LVTTL logic standard containing emissions peaks that are 12.58dB higher than the LVCMOS18 logic standard.

Δ7 illustrated below in Figure 87 shows

$$\Delta_{12} = A_{LVTTL} - A_{LVCMOS15}$$

Equation 22: Delta between LVTTL and LVCMOS15 (Comparison 3)

From Figure 87, the LVTTL logic standard produces emissions that are less than the LVCMOS15 standard sporadically throughout the observed spectrum. The minima recorded within plot at approximately 30MHz is -5.26dB, which translates to the LVTTL logic standard being 5.26dB lower than the LVCMOS15 standard at this point. The maxima within this comparison is 11.13dB at approximately 740MHz, which translates to the LVTTL logic standard containing emissions peaks that are 11.13dB higher than the LVCMOS15 logic standard.

Δ8 illustrated below in Figure 88 shows

$$\Delta_{13} = A_{LVTTL} - A_{LVCMOS12}$$

Equation 23: Delta between LVTTL and LVCMOS12 (Comparison 3)

From Figure 88, the LVTTL logic standard produces emissions that are less than the LVCMOS12 standard sporadically throughout the observed spectrum. The minima recorded within plot at approximately 60MHz is -6.87dB, which translates to the LVTTL logic standard being 6.87dB lower than the LVCMOS12 standard at this point. The maxima within this comparison is 11.42dB at approximately 740MHz, which translates to the LVTTL logic standard containing emissions peaks that are 11.42dB higher than the LVCMOS15 logic standard at this particular frequency.

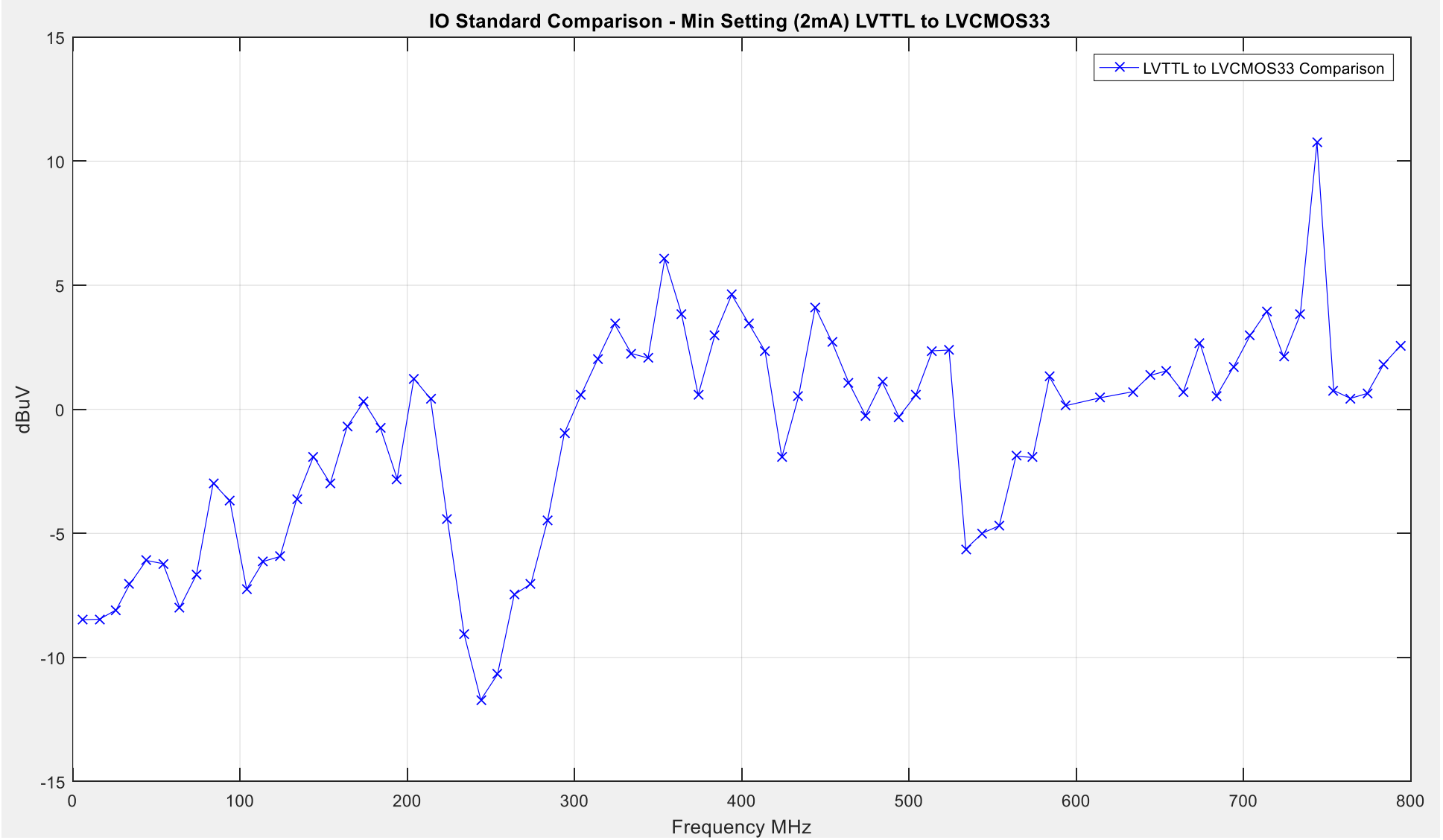


Figure 84: Peak Harmonic Difference (LVTTL to LVCMOS33)

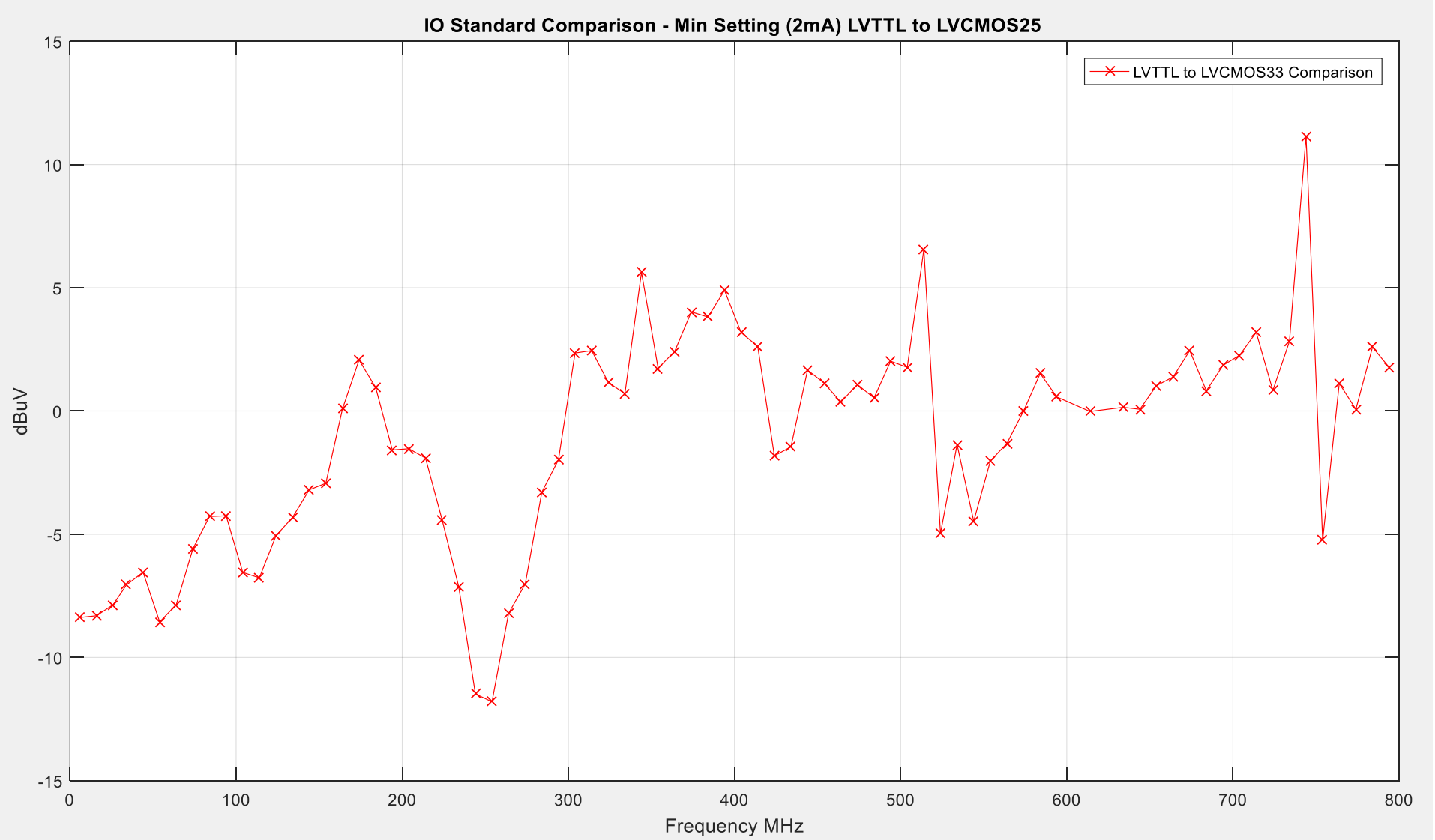


Figure 85: Peak Harmonic Difference (LVTTL to LVCMOS25)

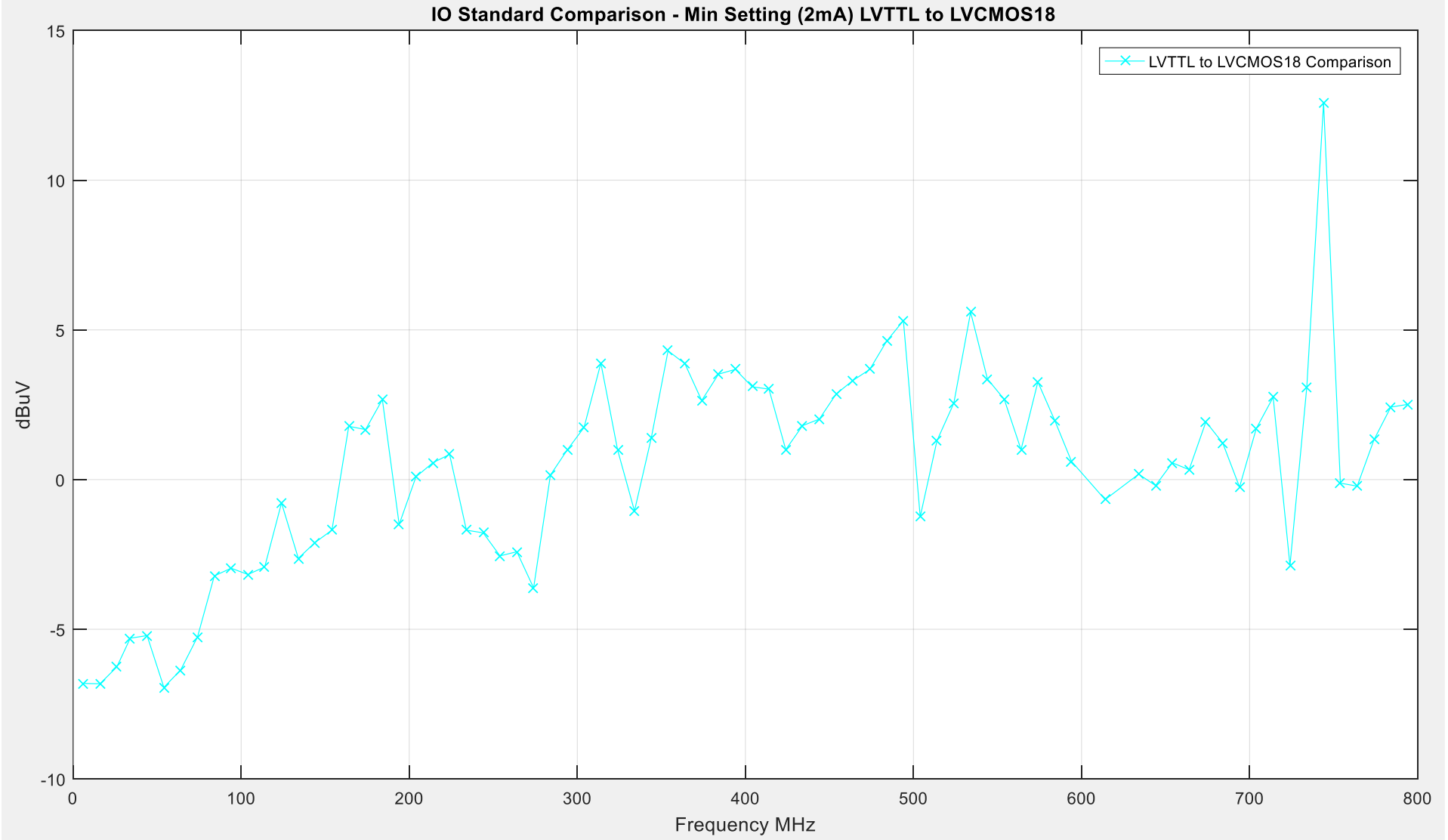


Figure 86: Peak Harmonic Difference (LVTTL to LVCMOS18)

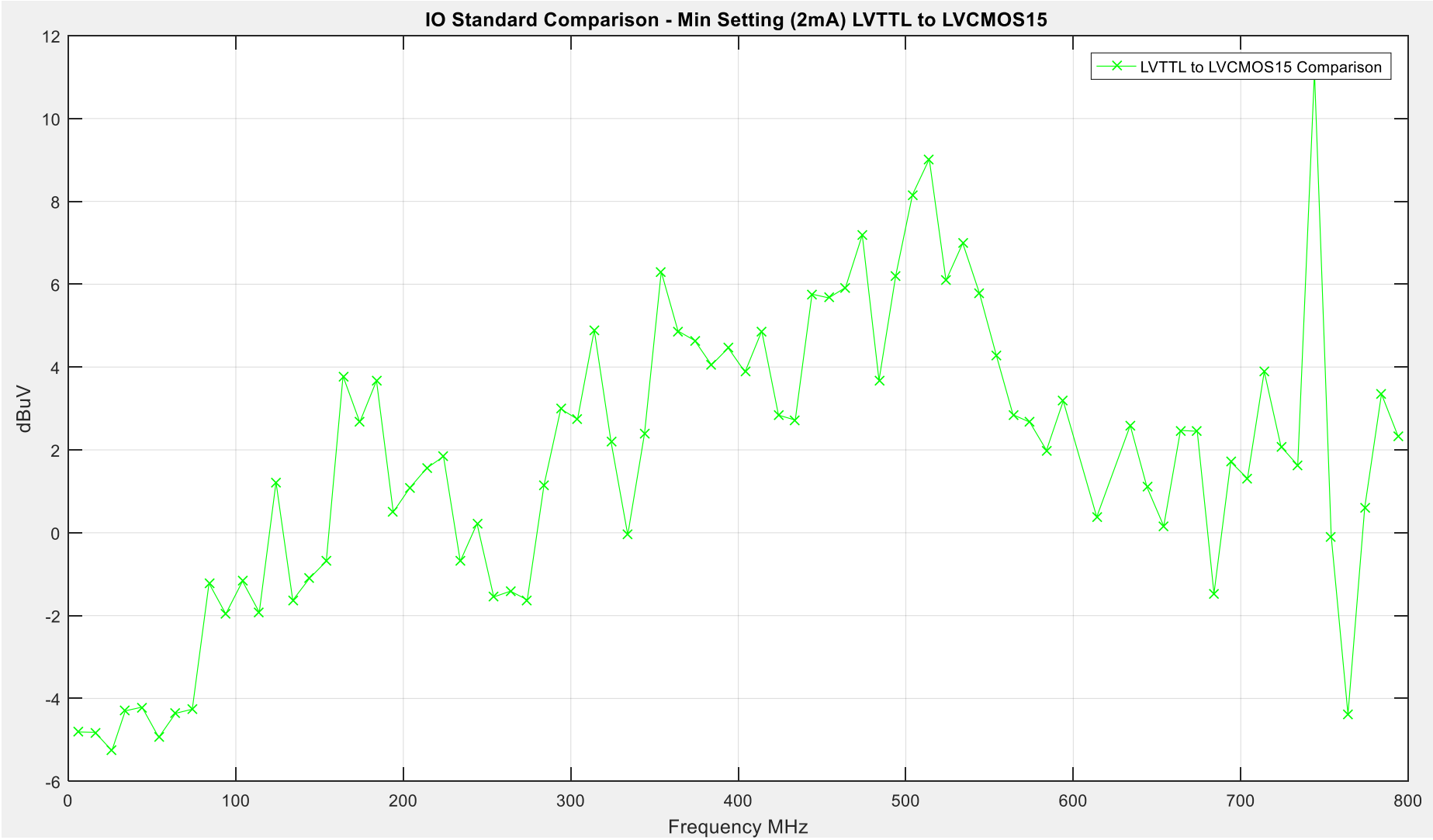


Figure 87: Peak Harmonic Difference (LVTTL to LVCMOS15)

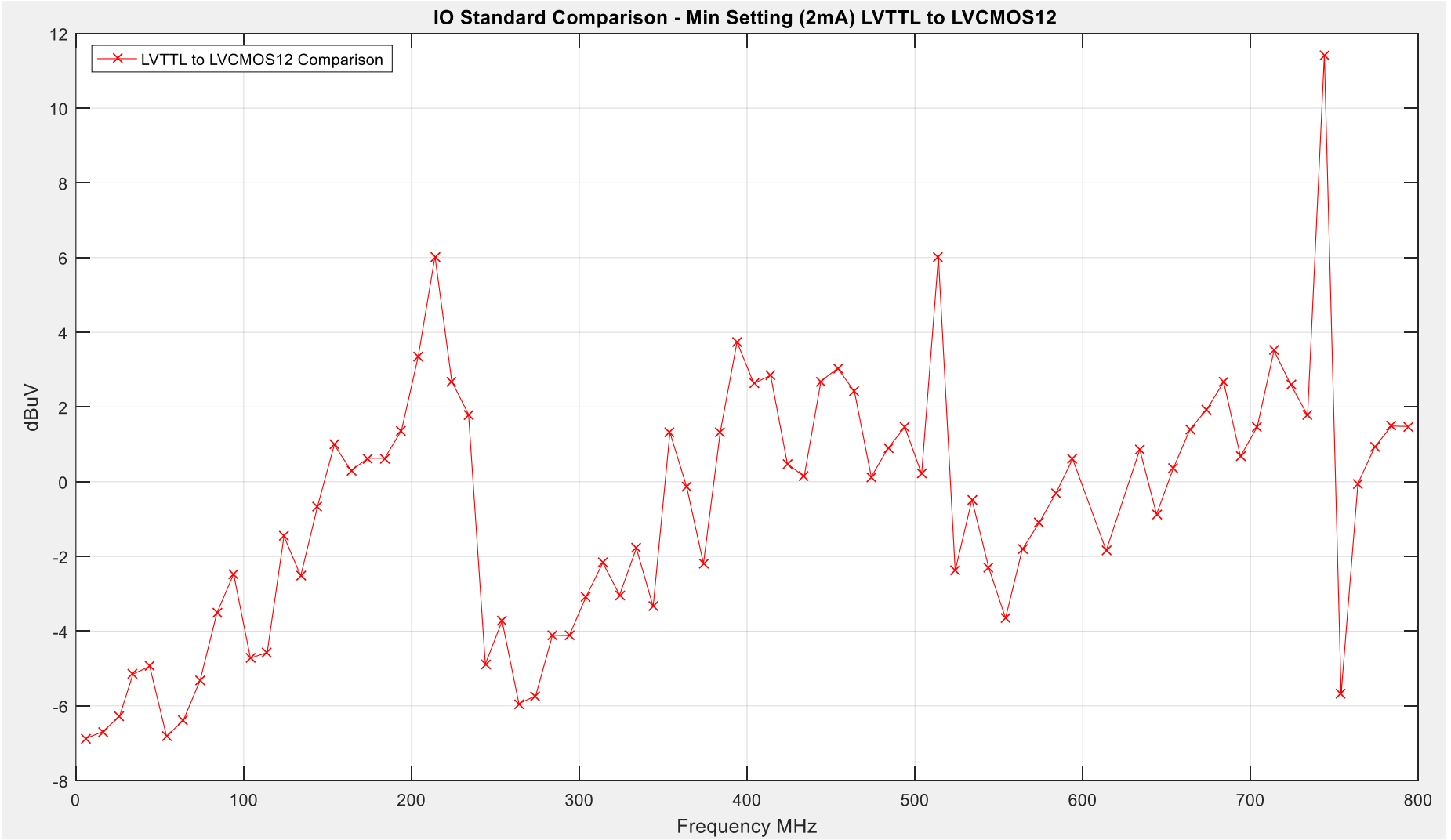


Figure 88: Peak Harmonic Difference (LVTTL to LVCMOS12)

5.3.4 I/O Standard Testing Conclusion

From the three measurement comparisons it can be concluded that the logic standard chosen significantly influences the peak level of emissions produced by the Spartan-6 FPGA. Changing no other variables than the logic standard, the peak level of emissions have been compared across three separate driver settings and edge rates to identify the logic standard with the highest level of emissions. Table 19, gives an overview of the average of the peak level of emissions obtained from the peak emissions recorded during testing.

Comparison 1 – Maximum Setting Average Noise Level dB	Comparison 2 – Default Setting Average Noise Level dB	Comparison 3 – Minimum Setting Average Noise Level dB
-59.99	-61.47	-73.8976
-63.75	-65.16	-73.3359
-63.47	-65.05	-72.6679
-62.92	-64.48	-73.7525
-	-65.94	-74.6304
-	-65.35	-73.2297

Table 19: I/O Standard Testing Overview - Average Emission Levels

The first of the three measurement comparisons observes the peak level of emissions produced by the logic standards with a drive strength of '24mA' and an edge rate of 'Fast'. The highest average level of emissions was recorded from the LVTTL I/O standard of approximately -60dBµV. The corresponding LVCMOS standards recorded a highest average of approximately 63.75dBµV showing an increase of more than +3.5dBµV by selecting the LVTTL IO standard. The greatest difference recorded between the LVCMOS standards is approximately 0.8dBµV. From the closer delta plots in Figure 74 to Figure 76 the greatest difference seen between the LVTTL and LVCMOS standards emissions traces is 11.6dB when comparing the LVTTL logic standard to the LVCMOS18 logic standard. Also the minima is seen where the LVTTL produces emissions that are -2.6dB lower than the LVCMOS25 logic standard.

The second of the measurement comparisons, entitled the default setting varies the logic standard across driver settings with a '12mA' drive strength and a fast edge rate. The emissions recorded were again higher from the LVTTL I/O standard with an average of approximately -61.5dBµV, +3dB greater than the LVCMOS standards. The LVCMOS standards recorded a highest average of -64.5dBµV across the 6 driver settings. From the closer delta plots in Figure 78 to Figure 82 the maxima of 16.8dB is seen when the LVTTL logic standard peak emissions is compared with the LVCMOS15 standard. The minima of -3.2dB is seen when comparing the LVTTL logic standard to the LVCMOS12 standard.

Finally the minimum driver settings comparison of the driver logic standards shows that the largest difference seen on average between the LVTTL and LVCMOS standards has reduced significantly to be less than 1 dB below the highest average recorded. The logic standard with

the highest average level of peak emissions is LVCMO25 with -72.6dBµV. The difference between any two of the logic standards on average is approximately 1.2dBµV. From these results it can be concluded that between the available logic standards, LVTTL produces the highest increase in emissions on average with an increase of approximately +3dBµV. Relating this to signal voltage levels an increase of +3dB is equivalent to doubling the amplitude of the noise source. From the closer delta plots in Figure 84 to Figure 88, it has been seen that the LVTTL is not the greatest contributor to peak level emissions along the observed frequency spectrum. Observing the frequency range 0-300MHz the LVTTL standard often produces peak level emissions that are lower than all of the LVCMOS standards. The greatest maxima of 12.58dB are seen when comparing the LVTTL to the LVCMOS18 standard, which translates to the LVTTL standard producing emissions that are 12.58dB higher than the LVCMOS18 standard. The greatest minima of -11.8dB is seen when comparing the LVTTL standard to the LVCMOS25 standard, which translates to the LVCMOS25 having emissions 11.8dB higher than the LVTTL standard.

By choosing to the implement a design around the LVCMOS I/O standard in favour of the LVTTL the reduction to average peak emissions has been shown to as high as -3dBµV. A reduction to emissions this significant is halving the amplitude of the emissions produced. From the closer delta comparisons it has been found that the peak levels of emissions fluctuate between logic standards, and that the LVTTL standard does contain peaks that are lower than the LVCMOS standards. When selecting the logic standard to be used in a design then careful consideration must also be applied by taking into account the required drive strength and edge rate for the design also. Greater variation between levels was seen when using the lowest drive strength setting ‘2mA’ and ‘slow’ edge rate. Overall the emissions produced from the LVTTL standard at the higher drive strength setting (24mA) and the default setting drive strength setting (12mA) has shown to be greater than that of the LVCMOS standard.

5.4 Drive Strength Testing

This section compares and analyses the emissions recorded when changing the drive strength settings across all available logic families within the Spartan-6 FPGA. The peak level of emissions has been recorded and an average level of these peaks taken to give a view of how vastly the level of emissions varies on average when changing the drive strength within each logic standard. Secondly to this a comparison between each plot has been taken to illustrate graphically the change to the peak level of emissions from each I/O driver setting. Table 20 to Table 25 contains the results obtained from the drive strength testing for the LVTTL, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15 and the LVCMOS12 logic standards respectively. From the peak level of emissions that has been recorded for each of the I/O driver strength settings a closer comparison of the change has been taken to illustrate the extent of change to emissions between the LVTTL drive strength settings.

5.4.1 LVTTL Drive Strength Testing Results

The traces illustrated in Figure 89 show the peak level of emissions recorded for the LVTTL I/O buffer drive strength settings detailed in Table 20 below.

LVTTL Setting	Average Noise Level dBµV	Delta Comparison dB
LVTTL-24mA-Fast	-59.9919	0
LVTTL-16mA-Fast	-60.5901	-0.7023
LVTTL-12mA-Fast	-61.4738	-2.376
LVTTL-8mA-Fast	-62.7774	-3.87
LVTTL-6mA-Fast	-68.2449	-7.92
LVTTL-4mA-Fast	-69.5009	-9.48
LVTTL-2mA-Fast	-72.6039	-13.19

Table 20: LVTTL Drive Strength Emissions Levels Overview

From these results obtained it gives an indication of how much variation occurs on average across the peak levels but does not give an indication of how this variation is distributed across the emissions spectrum. To achieve a more detailed comparison between the I/O driver settings, closer comparisons have been done to illustrate how the level of emissions varies across the observed spectrum. The 'LVTTL-24mA-Fast' I/O driver setting has been used as the baseline for the following 6 comparisons, for reference this trace is illustrated in Figure 90. The range of driver strength settings within the LVTTL logic standard reduces the peak level of emissions by 13.19dB from the 24mA setting to the 2mA setting.

5.4.1.1 Delta 1 – LVTTL-24mA-Fast to LVTTL-16mA-Fast Comparison

Delta 1 examines the variation to peak level emissions between the 'LVTTL-24mA-Fast' and the 'LVTTL-16mA-Fast' driver settings. Ultimately quantifying the change to emissions between 24mA to 16mA drive strength when using the LVTTL technology using Equation 24.

$$\Delta_1 = A_{LVTTL(24mA)} - A_{LVTTL(16mA)}$$

Equation 24: Drive Strength Testing: Delta 1 – LVTTL 24mA to 16mA Comparison

Where A_n is the vector that holds the peak level of emissions and Δ_n is the comparison equation.

The maxima of +4.73dB is recorded at approximately 640MHz, this is the highest point where the 24mA setting is greater than the 16mA setting in terms of the peak level of emissions. The minima of -4.53dB is recorded at approximately 170MHz, with the minima depicting the point where the 16mA setting is higher than the 24mA setting again in terms of the peak level of emissions recorded. The average level of change across the observed spectrum between the 24mA and 16mA drive strength settings is 0.7023dB. Figure 91 illustrates the plot for this comparison.

5.4.1.2 Delta 2 – LVTTL-24mA-Fast to LVTTL-12mA-Fast Comparison

Delta 2 examines the variation to peak level emissions between the 'LVTTL-24mA-Fast' and the 'LVTTL-12mA-Fast' driver settings. Ultimately quantifying the change to emissions between 24mA to 12mA drive strength when using the LVTTL technology using Equation 25.

$$\Delta_2 = A_{LVTTL(24mA)} - A_{LVTTL(12mA)}$$

Equation 25: Drive Strength Testing: Delta 2 – LVTTL 24mA to 12mA Comparison

Where A_n is the vector that holds the peak level of emissions and Δ_n is the comparison equation.

The maxima of +10.75dB is recorded at approximately 750MHz, this is the highest point where the 24mA setting is greater than the 12mA setting in terms of the peak level of emissions. The minima of -9.12dB is recorded at approximately 190MHz, with the minima depicting the point where the 12mA setting is higher than the 24mA setting again in terms of the peak level of emissions recorded. The average level of change across the observed spectrum between the 24mA and 12mA drive strength settings is 2.376dB.Figure 92 illustrates the plot for this comparison.

5.4.1.3 Delta 3 – LVTTL-24mA-Fast to LVTTL-8mA-Fast Comparison

Delta 3 examines the variation to peak level emissions between the 'LVTTL-24mA-Fast' and the 'LVTTL-8mA-Fast' driver settings. Ultimately quantifying the change to emissions between 24mA to 8mA drive strength when using the LVTTL technology using Equation 26.

$$\Delta_3 = A_{LVTTL(24mA)} - A_{LVTTL(8mA)}$$

Equation 26: Drive Strength Testing: Delta 3 – LVTTL 24mA to 8mA Comparison

Where A_n is the vector that holds the peak level of emissions and Δ_n is the comparison equation.

The maxima of +11.64dB is recorded at approximately 570MHz, this is the highest point where the 24mA setting is greater than the 8mA setting in terms of the peak level of emissions. The

minima of -10.04dB is recorded at approximately 190MHz, with the minima depicting the point where the 8mA setting is higher than the 24mA setting again in terms of the peak level of emissions recorded. The average level of change across the observed spectrum between the 24mA and 8mA drive strength settings is 3.87dB. Figure 93 illustrates the plot for this comparison.

5.4.1.4 Delta 4 – LVTTL-24mA-Fast to LVTTL-6mA-Fast Comparison

Delta 4 examines the variation to peak level emissions between the 'LVTTL-24mA-Fast' and the 'LVTTL-6mA-Fast' driver settings. Ultimately quantifying the change to emissions between 24mA to 6mA drive strength when using the LVTTL technology using Equation 27.

$$\Delta_4 = A_{LVTTL(24mA)} - A_{LVTTL(6mA)}$$

Equation 27: Drive Strength Testing: Delta 4 – LVTTL 24mA to 6mA Comparison

Where A_n is the vector that holds the peak level of emissions and Δ_n is the comparison equation.

The maxima of +20.32dB is recorded at approximately 10MHz, this is the highest point where the 24mA setting is greater than the 6mA setting in terms of the peak level of emissions. The minima of -10.04dB is recorded at approximately 190MHz, with the minima depicting the point where the 6mA setting is higher than the 24mA setting again in terms of the peak level of emissions recorded. The average level of change across the observed spectrum between the 24mA and 6mA drive strength settings is 7.92dB. Figure 94 illustrates the plot for this comparison.

5.4.1.5 Delta 5 – LVTTL-24mA-Fast to LVTTL-4mA-Fast Comparison

Delta 5 examines the variation to peak level emissions between the 'LVTTL-24mA-Fast' and the 'LVTTL-4mA-Fast' driver settings. Ultimately quantifying the change to emissions between 24mA to 4mA drive strength when using the LVTTL technology using Equation 28.

$$\Delta_5 = A_{LVTTL(24mA)} - A_{LVTTL(4mA)}$$

Equation 28: Drive Strength Testing: Delta 5 – LVTTL 24mA to 4mA Comparison

Where A_n is the vector that holds the peak level of emissions and Δ_n is the comparison equation.

The maxima of +22.93dB is recorded at approximately 10MHz, this is the highest point where the 24mA setting is greater than the 4mA setting in terms of the peak level of emissions. The minima of -3.6dB is recorded at approximately 190MHz, with the minima depicting the point where the 4mA setting is higher than the 24mA setting again in terms of the peak level of emissions recorded. The average level of change across the observed spectrum between the

24mA and 4mA drive strength settings is +9.48dB. Figure 95 illustrates the plot for this comparison.

5.4.1.6 Delta 6 – LVTTL-24mA-Fast to LVTTL-4mA-Fast Comparison

Delta 6 examines the variation to peak level emissions between the 'LVTTL-24mA-Fast' and the 'LVTTL-2mA-Fast' driver settings. Ultimately quantifying the change to emissions between 24mA to 2mA drive strength when using the LVTTL technology using Equation 29.

$$\Delta_6 = A_{LVTTL(24mA)} - A_{LVTTL(2mA)}$$

Equation 29: Drive Strength Testing: Delta 6 – LVTTL 24mA to 2mA Comparison

Where A_n is the vector that holds the peak level of emissions and Δ_n is the comparison equation.

The maxima of +27.91dB is recorded at approximately 10MHz, this is the highest point where the 24mA setting is greater than the 2mA setting in terms of the peak level of emissions. The minima of -1.9dB is recorded at approximately 190MHz, with the minima depicting the point where the 2mA setting is higher than the 24mA setting again in terms of the peak level of emissions recorded. The average level of change across the observed spectrum between the 24mA and 2mA drive strength settings is +13.19dB. Figure 96 illustrates the plot for this comparison.

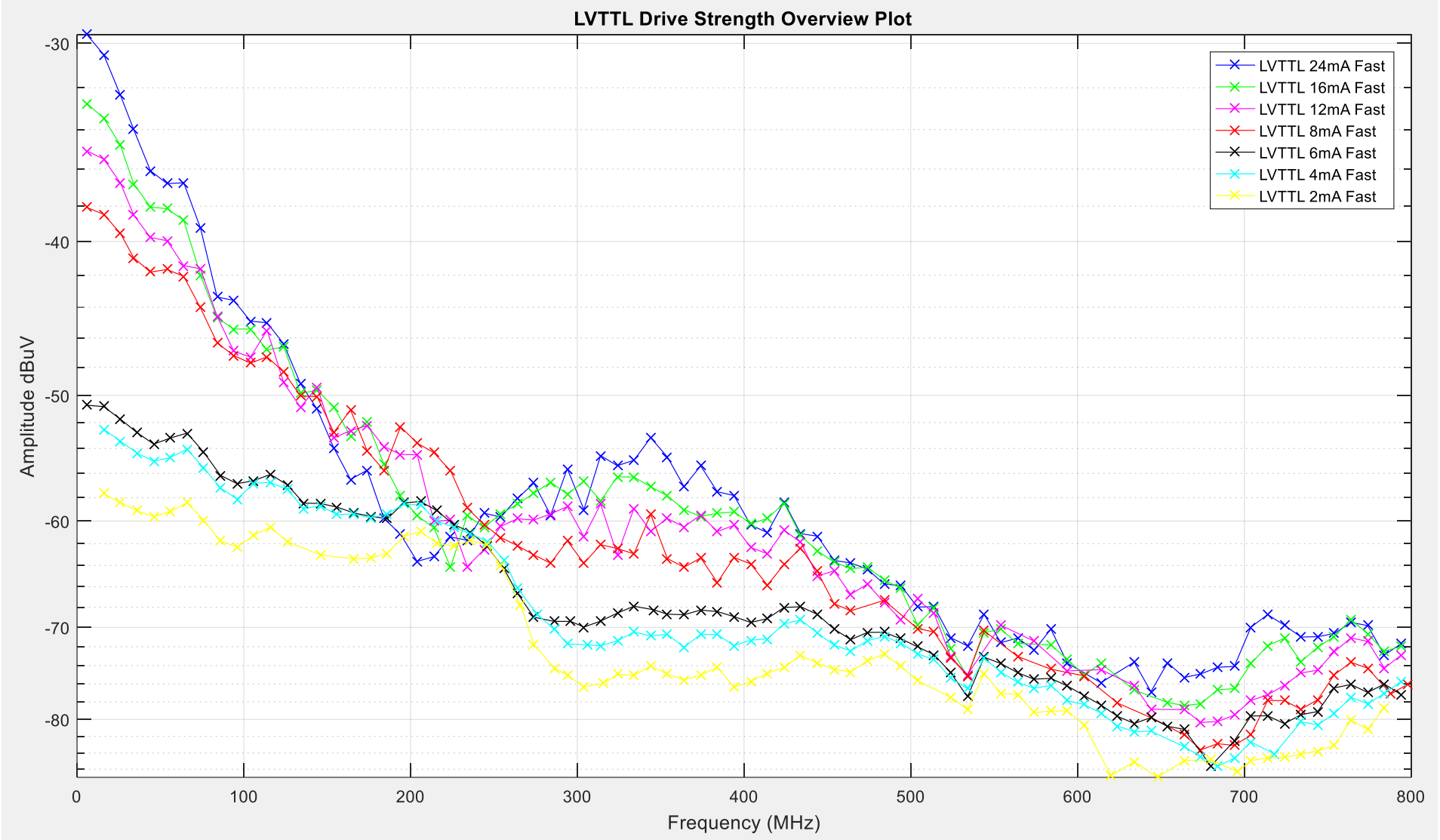


Figure 89: LVTTL Drive Strength Overview Plot

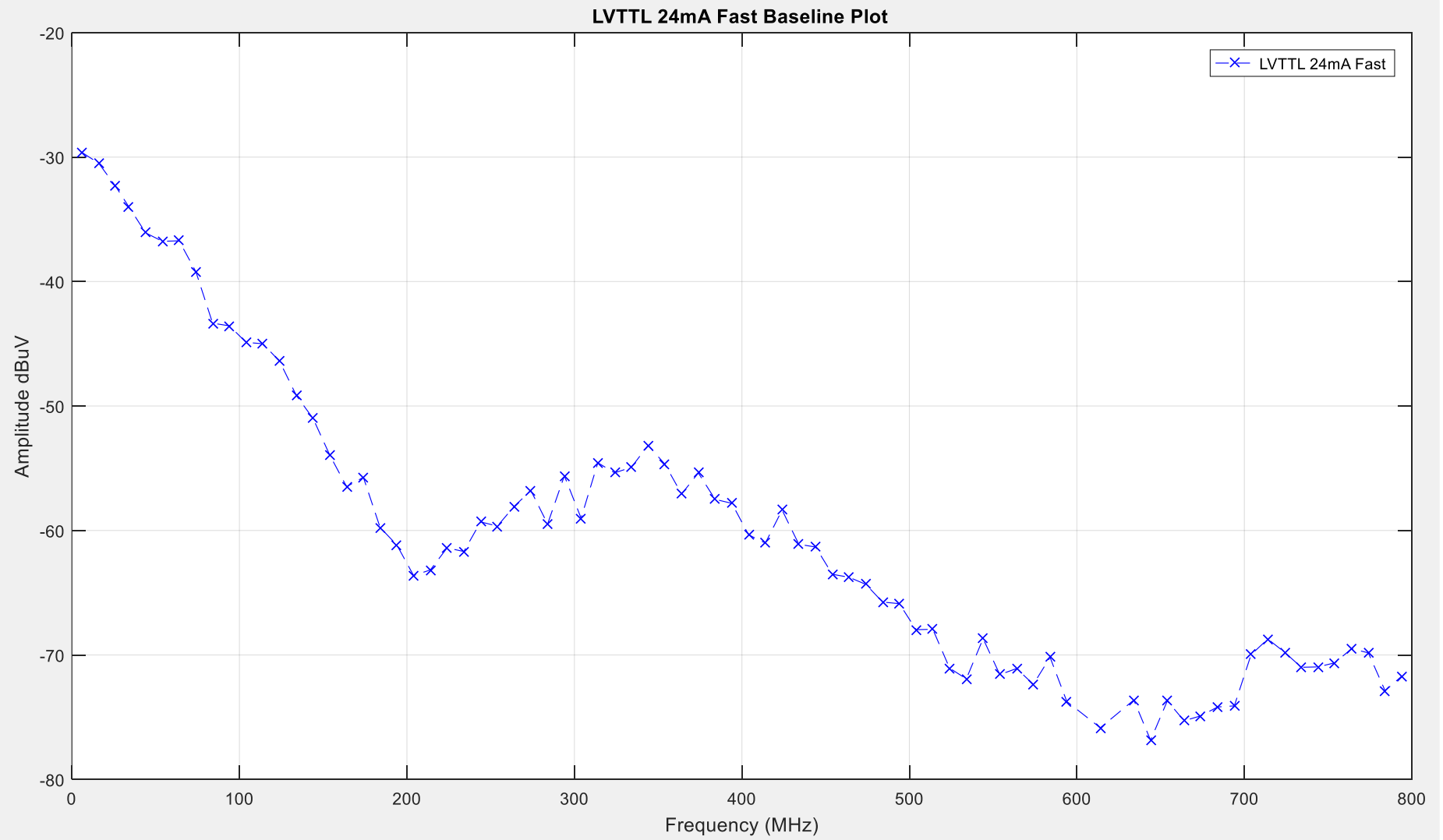


Figure 90: LVTTL-24mA-Fast Drive Strength Baseline Plot

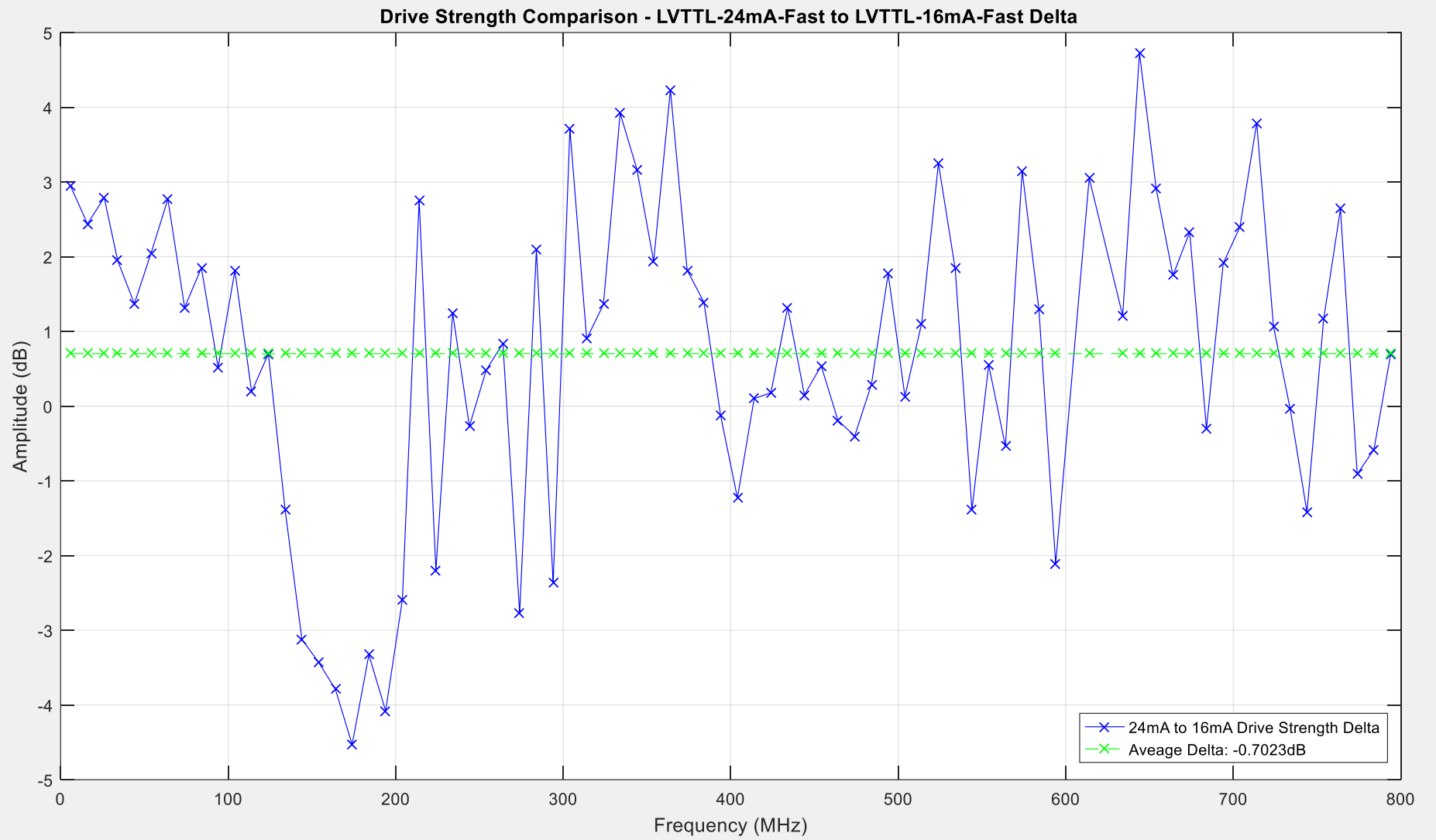


Figure 91: LVTTL-24mA-Fast to LVTTL-16mA-Fast Drive Strength Comparison

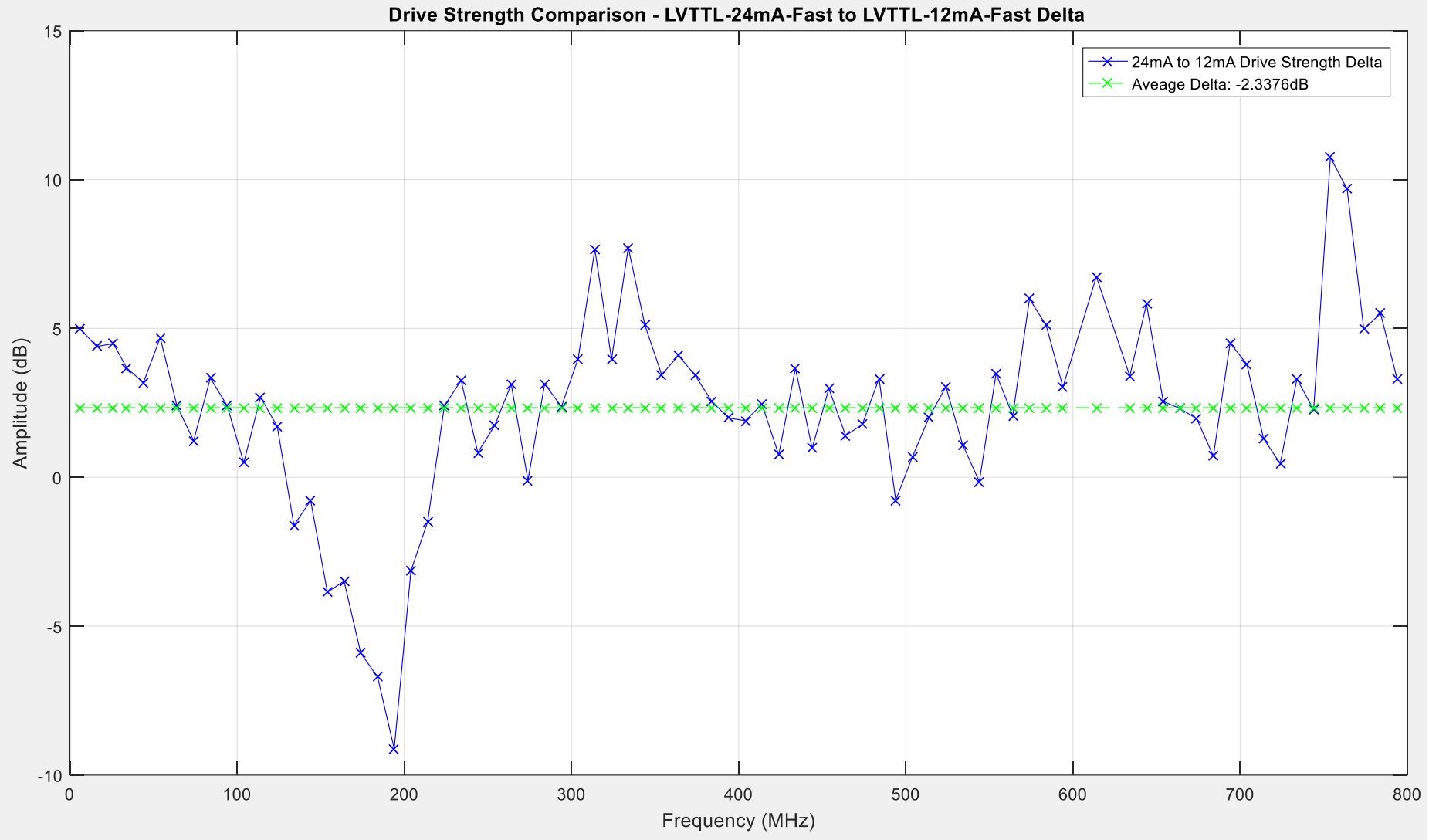


Figure 92: LVTTL-24mA-Fast to LVTTL-12mA-Fast Drive Strength Comparison

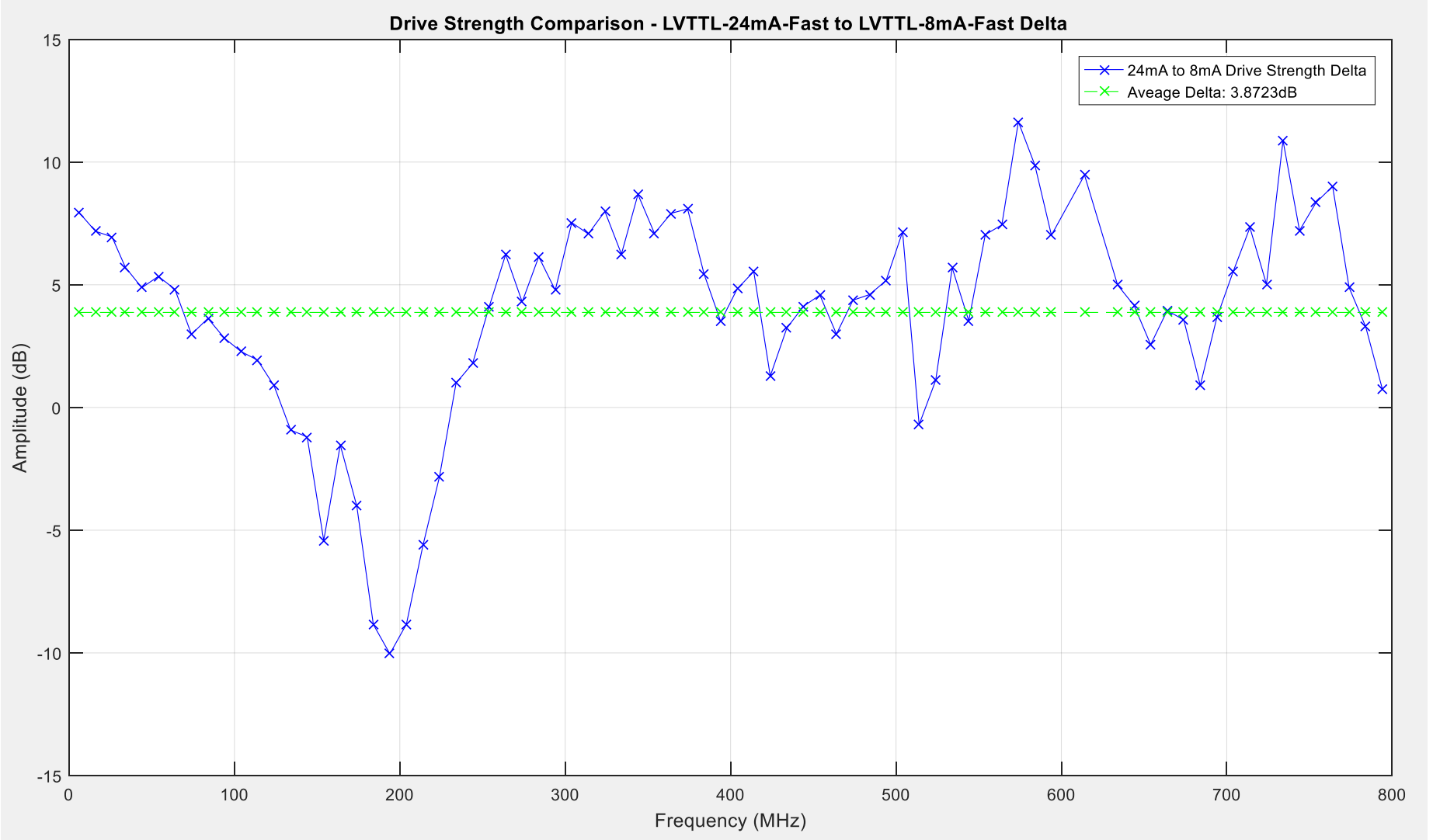


Figure 93: LVTTL-24mA-Fast to LVTTL-8mA-Fast Drive Strength Comparison

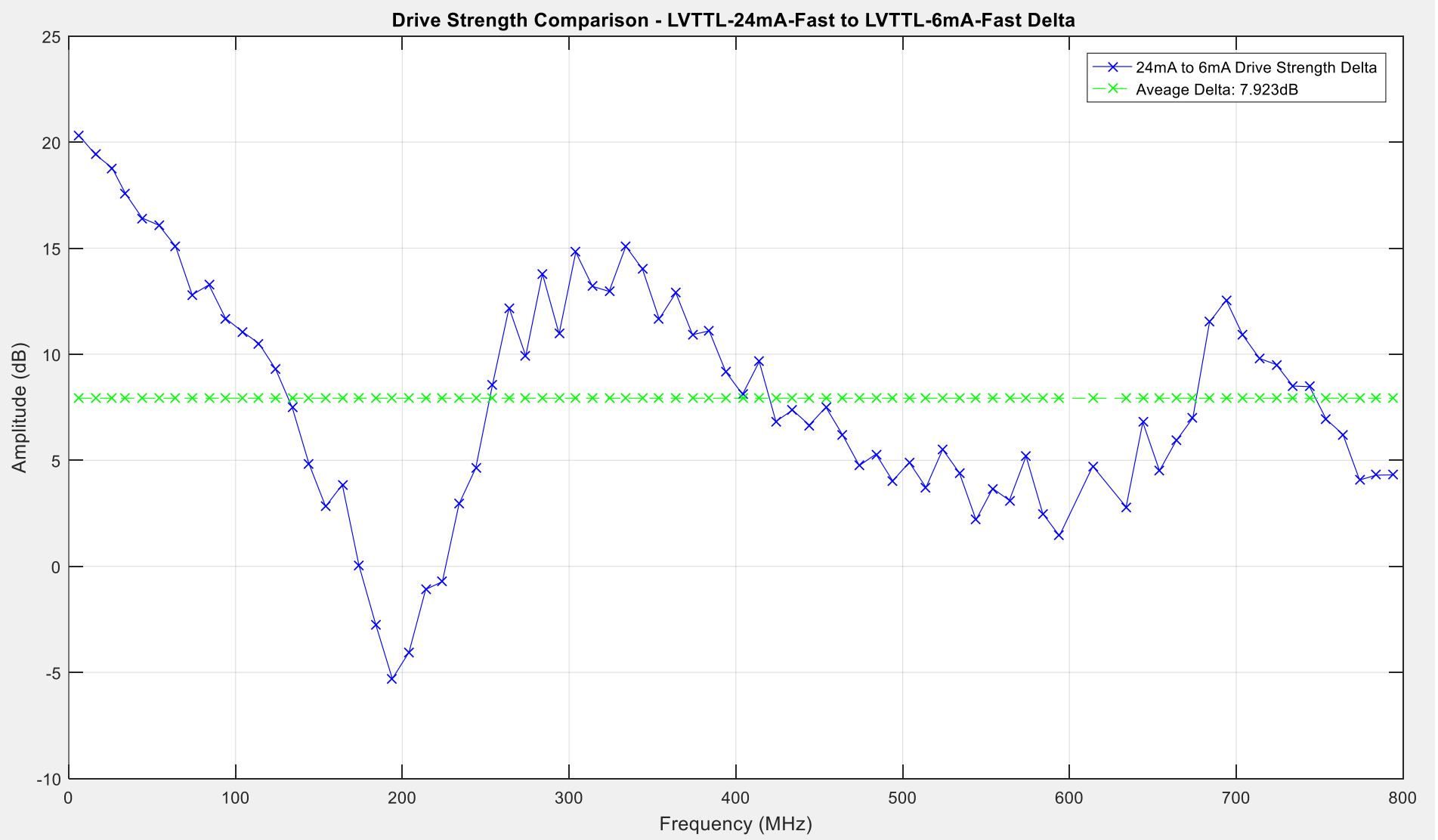


Figure 94: LVTTL-24mA-Fast to LVTTL-6mA-Fast Drive Strength Comparison

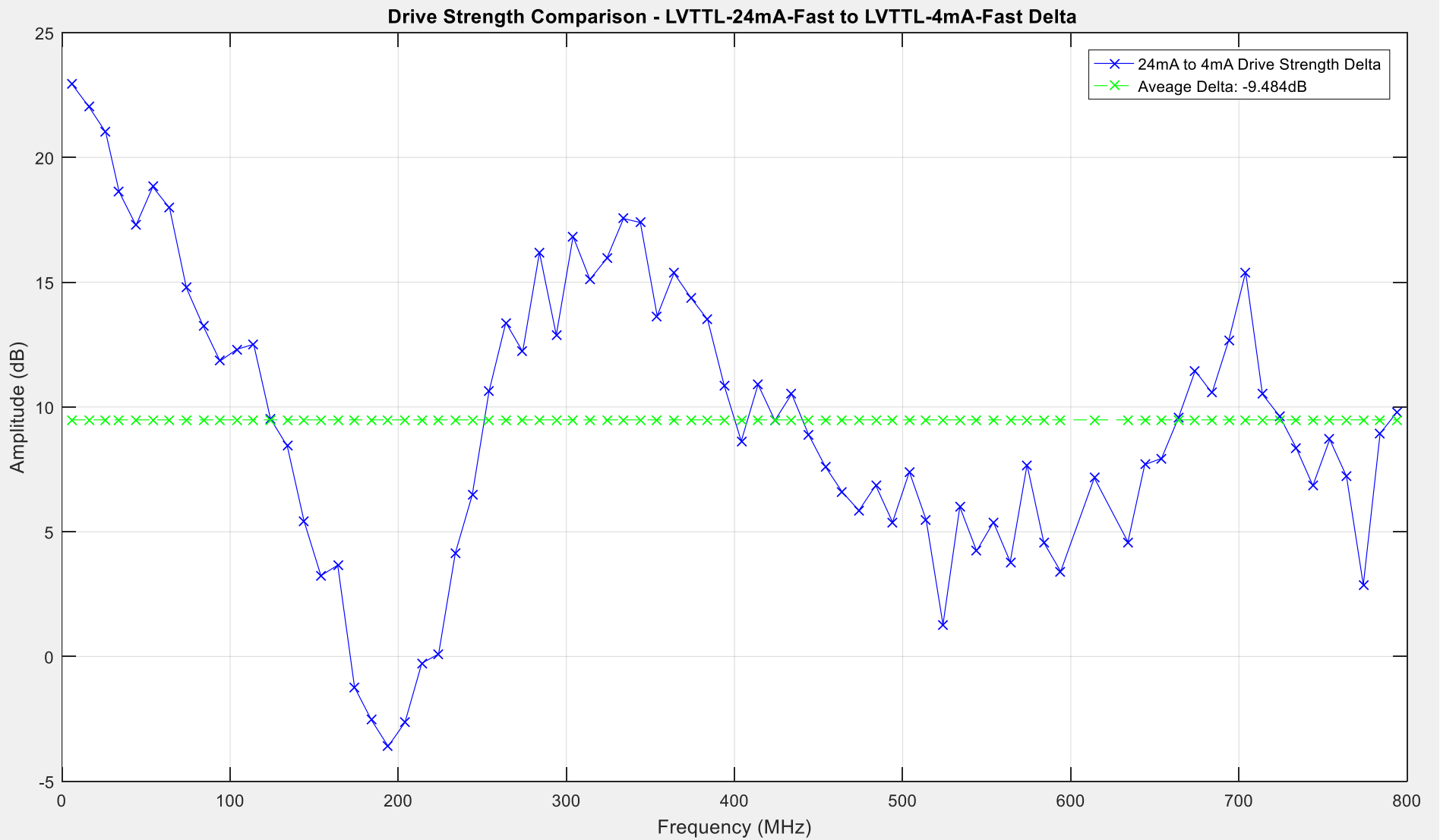


Figure 95: LVTTL-24mA-Fast to LVTTL-4mA-Fast Drive Strength Comparison

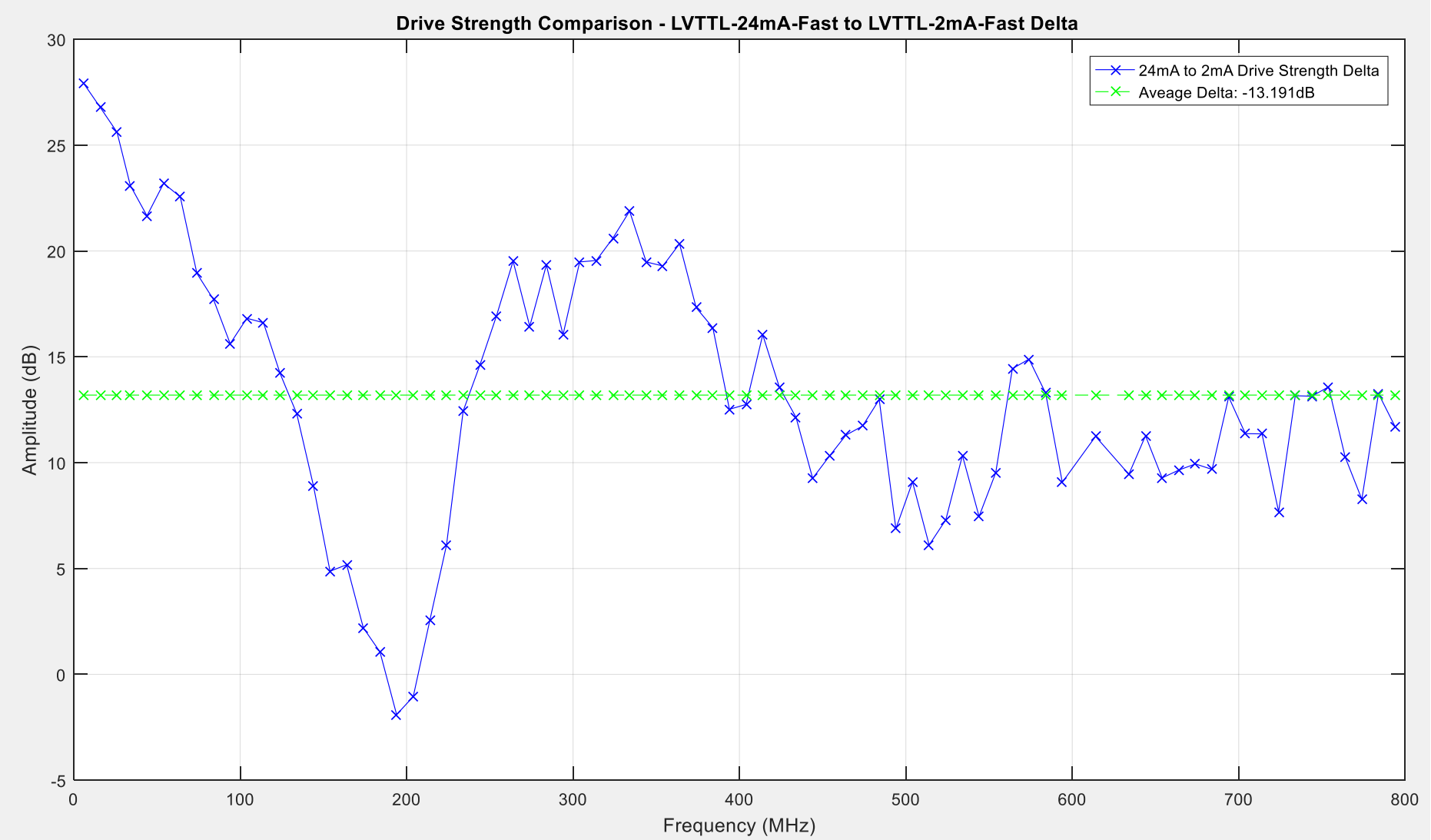


Figure 96: LVTTL-24mA-Fast to LVTTL-2mA-Fast Drive Strength Comparison

5.4.2 LVCMOS33 Drive Strength Results

The traces illustrated in Figure 97 shows the peak level of emissions recorded for the LVTTL I/O buffer drive strength settings detailed in Table 21 below.

LVCMOS33 Setting	Average Noise Level dBµV	Delta Comparison dB
LVCMOS33-24mA-Fast	-63.7553	0
LVCMOS33-16mA-Fast	-64.4566	-0.6723
LVCMOS33-12mA-Fast	-65.1585	-2.3608
LVCMOS33-8mA-Fast	-66.3082	3.2362
LVCMOS33-6mA-Fast	-68.6833	-4.3013
LVCMOS33-4mA-Fast	-69.5231	-6.095
LVCMOS33-2mA-Fast	-72.0851	-8.37

Table 21: LVCMOS33 Drive Strength Emissions Levels Overview

From these results obtained it gives an indication of how much variation occurs on average across the peak levels but does not give an indication of how this variation is distributed across the emissions spectrum. To achieve a more detailed comparison between the I/O driver settings, closer comparisons have been done to illustrate how the level of emissions varies across the observed spectrum. The 'LVCMOS33-24mA-Fast' I/O driver setting has been used as the baseline for the following 6 comparisons, for reference this trace is illustrated in Figure 98. The LVCMOS33-24mA-Fast drive strength testing has an average level of peak emissions of 63.75dBµV.

5.4.2.1 Delta 7 – LVCMOS33-24mA-Fast to LVCMOS33-16mA-Fast Comparison

Delta 7 examines the variation to peak level emissions between the 'LVCMOS33-24mA-Fast' and the 'LVCMOS33-16mA-Fast' driver settings. Ultimately quantifying the change to emissions between 24mA to 16mA drive strength when using the LVCMOS33 technology using Equation 30.

$$\Delta_7 = A_{LVCMOS33(24mA)} - A_{LVCMOS33(16mA)}$$

Equation 30: Drive Strength Testing: Delta 7 – LVCMOS33 24mA to 16mA Comparison

Where A_n is the vector that holds the peak level of emissions and Δ_n is the comparison equation.

The maxima of +4.57dB is recorded at approximately 710MHz, this is the highest point where the 24mA setting is greater than the 16mA setting in terms of the peak level of emissions. The minima of -3.95dB is recorded at approximately 180MHz, with the minima depicting the point where the 16mA setting is higher than the 24mA setting again in terms of the peak level of emissions recorded. The average level of change across the observed spectrum between the 24mA and 16mA drive strength settings is -0.6732dB. Figure 99 illustrates the plot for this comparison.

5.4.2.2 Delta 8 – LVCMOS33-24mA-Fast to LVCMOS33-12mA-Fast Comparison

Delta 8 examines the variation to peak level emissions between the 'LVCMOS33-24mA-Fast' and the 'LVCMOS33-12mA-Fast' driver settings. Ultimately quantifying the change to emissions between 24mA to 12mA drive strength when using the LVCMOS33 technology using Equation 31.

$$\Delta_8 = A_{LVCMOS33(24mA)} - A_{LVCMOS33(12mA)}$$

Equation 31: Drive Strength Testing: Delta 8 – LVCMOS33 24mA to 12mA Comparison

Where A_n is the vector that holds the peak level of emissions and Δ_n is the comparison equation.

The maxima of +11.28dB is recorded at approximately 770MHz, this is the highest point where the 24mA setting is greater than the 12mA setting in terms of the peak level of emissions. The minima of -9.92dB is recorded at approximately 510MHz, with the minima depicting the point where the 12mA setting is higher than the 24mA setting again in terms of the peak level of emissions recorded. The average level of change across the observed spectrum between the 24mA and 12mA drive strength settings is -2.3608dB. Figure 100 illustrates the plot for this comparison.

5.4.2.3 Delta 9 – LVCMOS33-24mA-Fast to LVCMOS33-8mA-Fast Comparison

Delta 9 examines the variation to peak level emissions between the 'LVCMOS33-24mA-Fast' and the 'LVCMOS33-8mA-Fast' driver settings. Ultimately quantifying the change to emissions between 24mA to 8mA drive strength when using the LVCMOS33 technology using Equation 32.

$$\Delta_9 = A_{LVCMOS33(24mA)} - A_{LVCMOS33(8mA)}$$

Equation 32: Drive Strength Testing: Delta 9 – LVCMOS33 24mA to 8mA Comparison

Where A_n is the vector that holds the peak level of emissions and Δ_n is the comparison equation.

The maxima of +9.95dB is recorded at approximately 790MHz, this is the highest point where the 24mA setting is greater than the 8mA setting in terms of the peak level of emissions. The minima of –11.9dB is recorded at approximately 510MHz, with the minima depicting the point where the 8mA setting is higher than the 24mA setting again in terms of the peak level of emissions recorded. The average level of change across the observed spectrum between the 24mA and 8mA drive strength settings is -3.2362dB. Figure 101 illustrates the plot for this comparison.

5.4.2.4 Delta 10 – LVCMOS33-24mA-Fast to LVCMOS33-6mA-Fast Comparison

Delta 10 examines the variation to peak level emissions between the 'LVCMOS33-24mA-Fast' and the 'LVCMOS33-6mA-Fast' driver settings. Ultimately quantifying the change to emissions between 24mA to 6mA drive strength when using the LVCMOS33 technology using Equation 33.

$$\Delta_{10} = A_{LVCMOS33(24mA)} - A_{LVCMOS33(6mA)}$$

Equation 33: Drive Strength Testing: Delta 10 – LVCMOS33 24mA to 6mA Comparison

Where A_n is the vector that holds the peak level of emissions and Δ_n is the comparison equation.

The maxima of +18.53dB is recorded at approximately 5MHz, this is the highest point where the 24mA setting is greater than the 6mA setting in terms of the peak level of emissions. The minima of –7.22dB is recorded at approximately 220MHz, with the minima depicting the point where the 6mA setting is higher than the 24mA setting again in terms of the peak level of emissions recorded. The average level of change across the observed spectrum between the 24mA and 6mA drive strength settings is -4.3013dB. Figure 102 illustrates the plot for this comparison.

5.4.2.5 Delta 11 – LVCMOS33-24mA-Fast to LVCMOS33-4mA-Fast Comparison

Delta 11 examines the variation to peak level emissions between the 'LVCMOS33-24mA-Fast' and the 'LVCMOS33-4mA-Fast' driver settings. Ultimately quantifying the change to emissions between 24mA to 4mA drive strength when using the LVCMOS33 technology using Equation 34.

$$\Delta_{11} = A_{LVCMOS33(24mA)} - A_{LVCMOS33(4mA)}$$

Equation 34: Drive Strength Testing: Delta 11 – LVCMOS33 24mA to 4mA Comparison

Where A_n is the vector that holds the peak level of emissions and Δ_n is the comparison equation.

The maxima of 16.57dB is recorded at approximately 330MHz, this is the highest point where the 24mA setting is greater than the 4mA setting in terms of the peak level of emissions. The minima of –10.94dB is recorded at approximately 520MHz, with the minima depicting the point where the 4mA setting is higher than the 24mA setting again in terms of the peak level of emissions recorded. The average level of change across the observed spectrum between the 24mA and 4mA drive strength settings is -6.0954dB. Figure 103 illustrates the plot for this comparison.

5.4.2.6 Delta 12 – LVCMOS33-24mA-Fast to LVCMOS33-2mA-Fast Comparison

Delta 12 examines the variation to peak level emissions between the 'LVCMOS33-24mA-Fast' and the 'LVCMOS33-2mA-Fast' driver settings. Ultimately quantifying the change to emissions between 24mA to 2mA drive strength when using the LVCMOS33 technology using Equation 35.

$$\Delta_{12} = A_{LVCMOS33(24mA)} - A_{LVCMOS33(2mA)}$$

Equation 35: Drive Strength Testing: Delta 12 – LVCMOS33 24mA to 2mA Comparison

Where A_n is the vector that holds the peak level of emissions and Δ_n is the comparison equation.

The maxima of 21.58dB is recorded at approximately 350MHz, this is the highest point where the 24mA setting is greater than the 2mA setting in terms of the peak level of emissions. The minima of –5.33dB is recorded at approximately 520MHz, with the minima depicting the point where the 2mA setting is higher than the 24mA setting again in terms of the peak level of emissions recorded. The average level of change across the observed spectrum between the 24mA and 2mA drive strength settings is -8.37dB. Figure 104 illustrates the plot for this comparison.

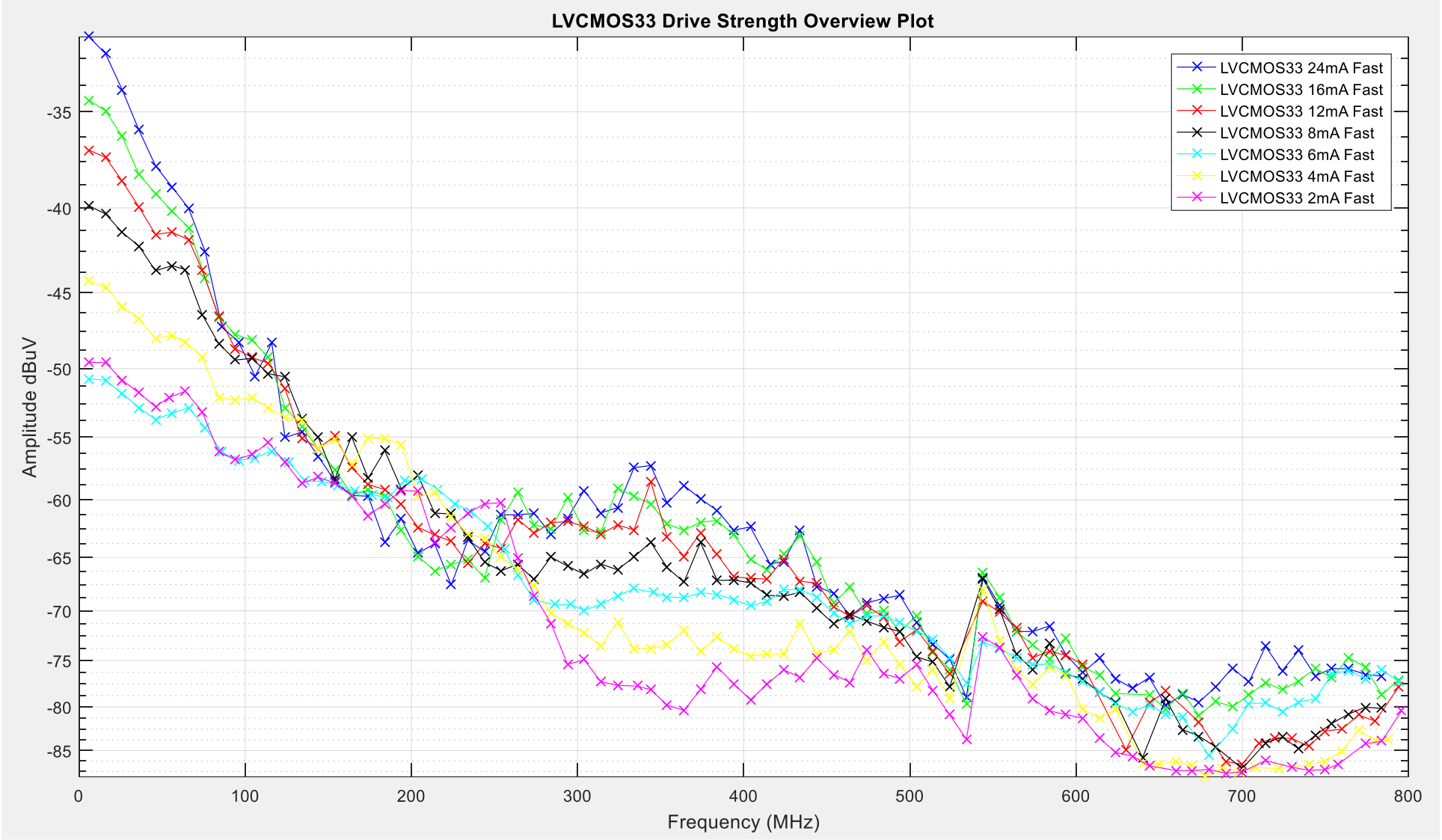


Figure 97: LVCMOS33 Drive Strength Overview Plot

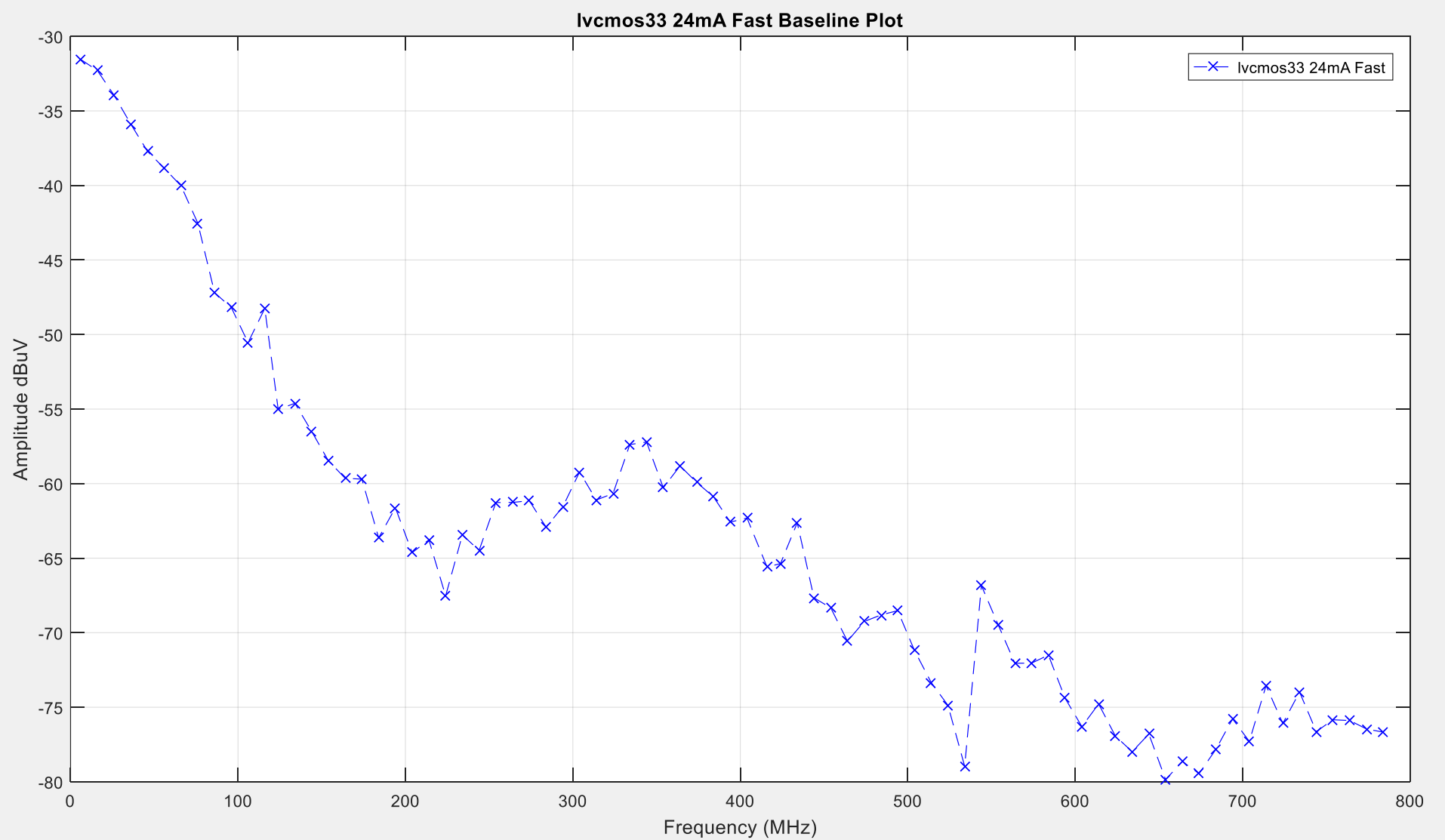


Figure 98: LVCMOS33 Drive Strength Overview Plot

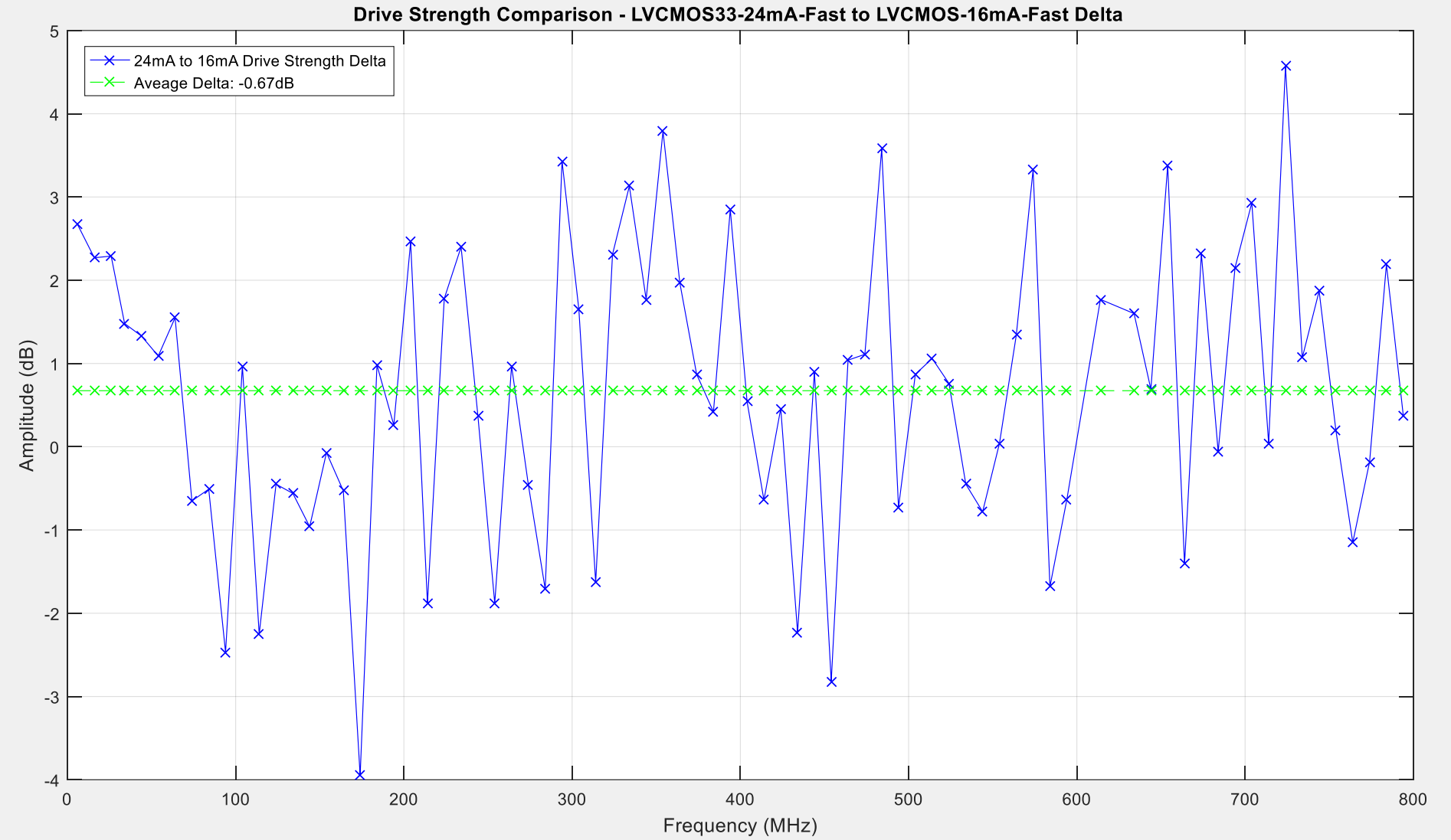


Figure 99: LVCMOS33-24mA-Fast to LVCMOS33-16mA-Fast Drive Strength Comparison

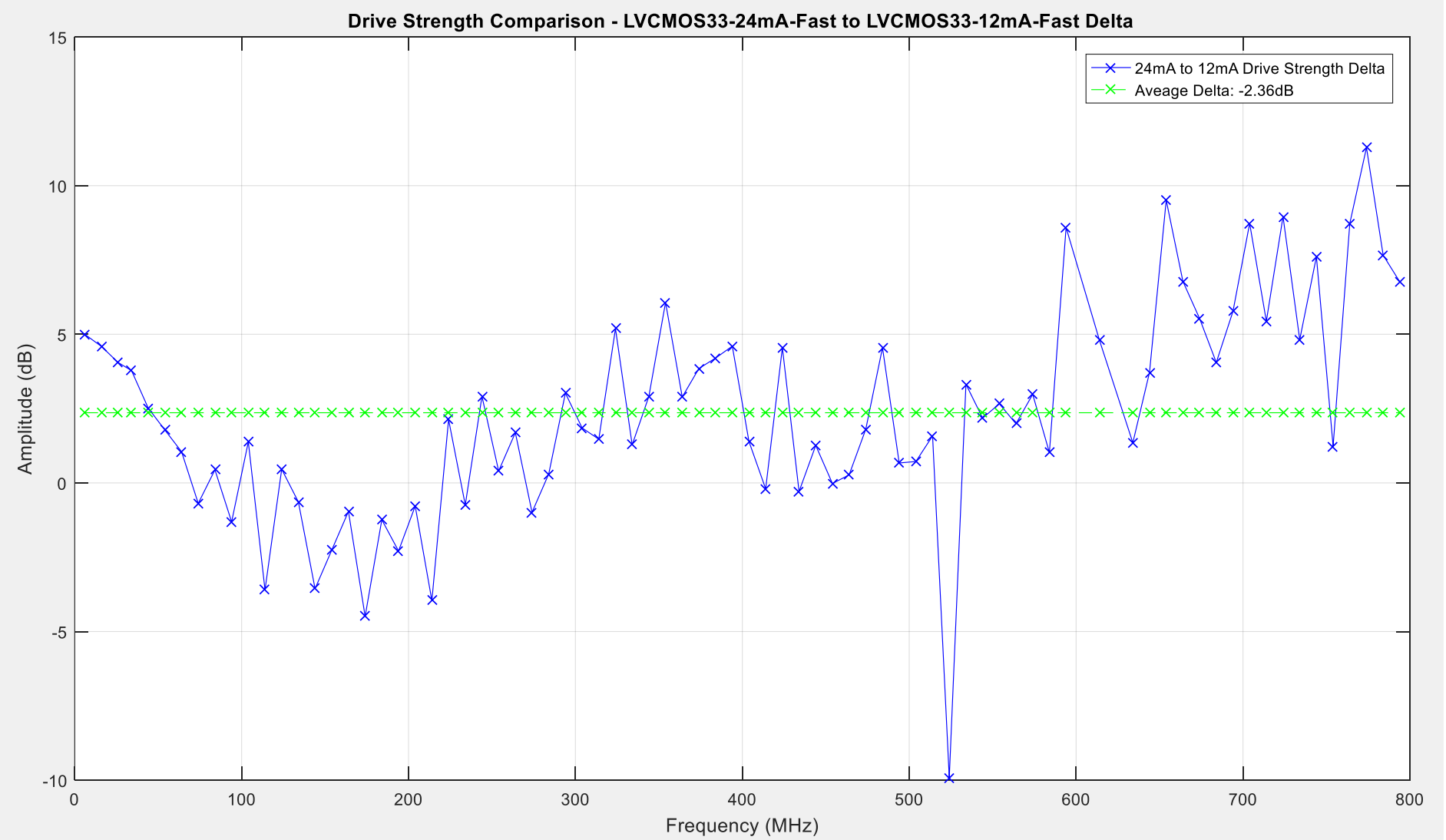


Figure 100: LVCMOS33-24mA-Fast to LVCMOS33-12mA-Fast Drive Strength Comparison

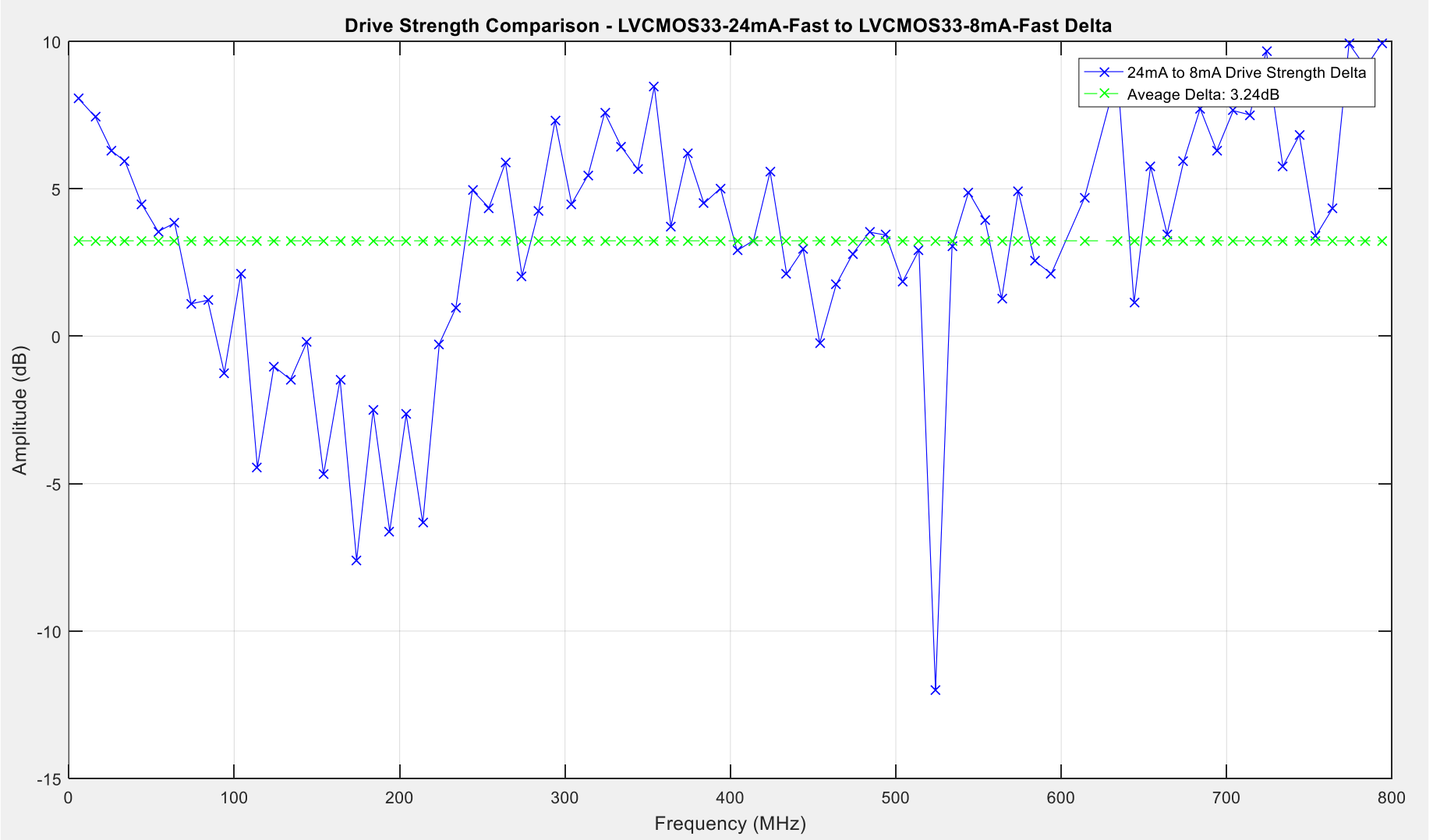


Figure 101: LVCMOS33-24mA-Fast to LVCMOS33-8mA-Fast Drive Strength Comparison

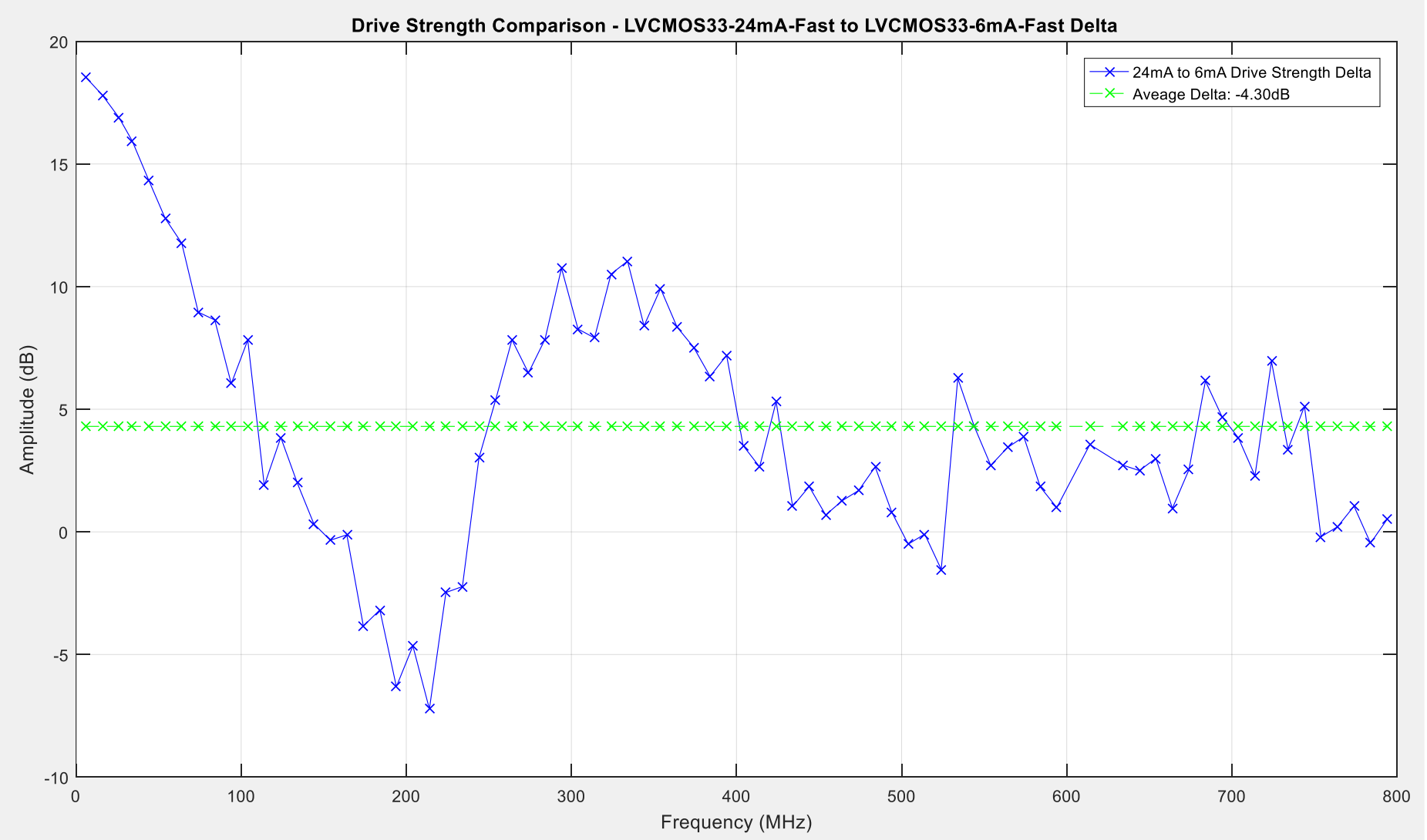


Figure 102: LVCMOS33-24mA-Fast to LVCMOS33-6mA-Fast Drive Strength Comparison

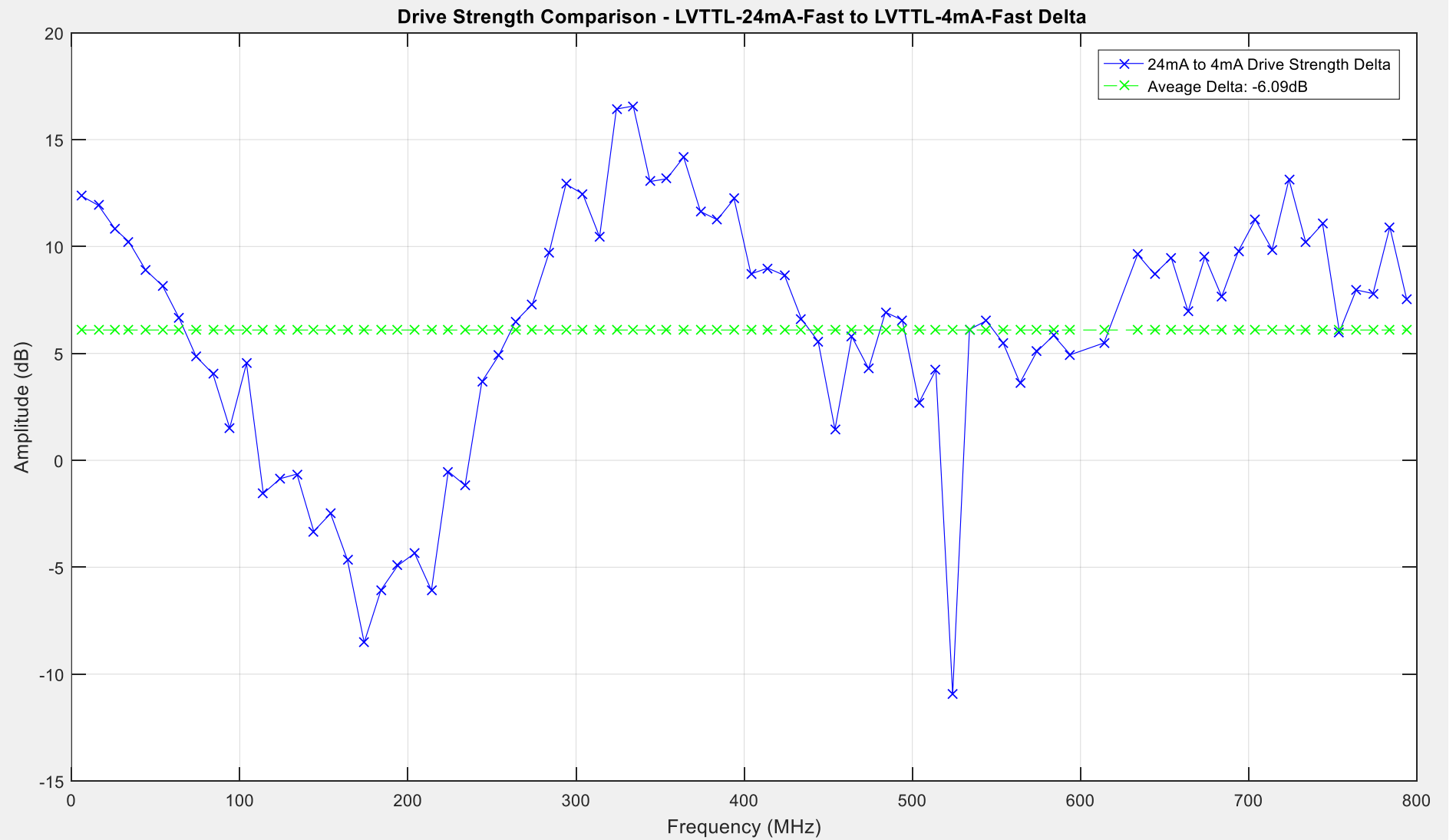


Figure 103: LVCMOS33-24mA-Fast to LVCMOS33-4mA-Fast Drive Strength Comparison

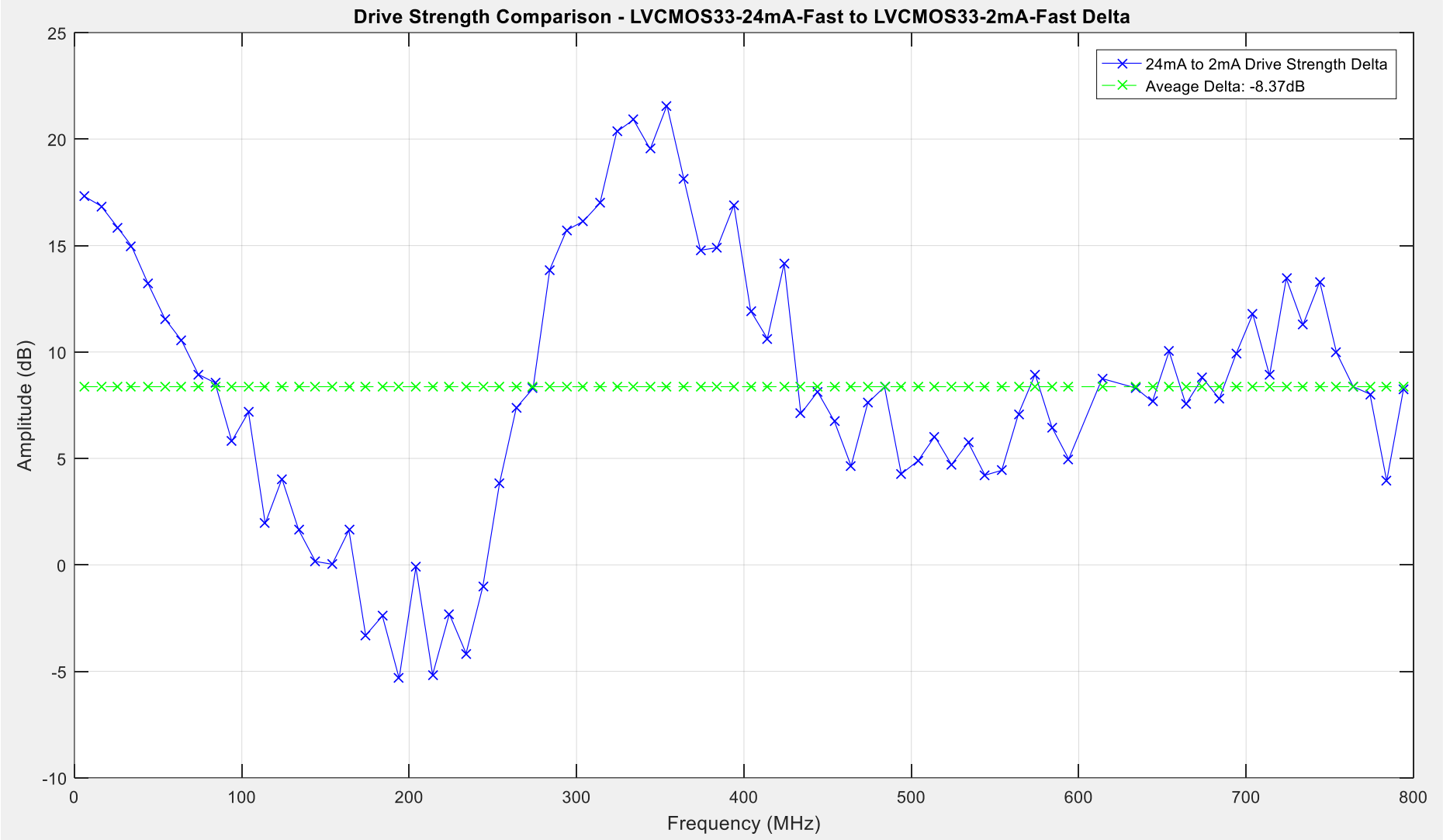


Figure 104: LVCMOS33-24mA-Fast to LVCMOS33-2mA-Fast Drive Strength Comparison

5.4.3 LVCMOS25 Drive Strength Results

The traces illustrated in Figure 105 shows the peak level of emissions recorded for the LVCMOS25 I/O buffer drive strength settings detailed in Table 22 below.

LVCMOS25 Setting	Average Noise Level dBµV	Delta Comparison dB
LVCMOS25-24mA-Fast	-63.4778	0
LVCMOS25-16mA-Fast	-65.1675	-2.169
LVCMOS25-12mA-Fast	-65.0459	-1.678
LVCMOS25-8mA-Fast	-66.2582	-3.18
LVCMOS25-6mA-Fast	-67.3227	-3.75
LVCMOS25-4mA-Fast	-69.0062	-4.64
LVCMOS25-2mA-Fast	-72.0572	-9.16

Table 22: LVCMOS25 Drive Strength Emissions Levels Overview

From these results obtained it gives an indication of how much variation occurs on average across the peak levels but does not give an indication of how this variation is distributed across the emissions spectrum. To achieve a more detailed comparison between the I/O driver settings, closer comparisons have been done to illustrate how the level of emissions varies across the observed spectrum. The 'LVCMOS25-24mA-Fast' I/O driver setting has been used as the baseline for the following 6 comparisons, for reference this trace is illustrated in Figure 105. The LVCMOS25-24mA-Fast drive strength testing has an average level of peak emissions of 63.4778dBµV.

5.4.3.1 Delta 13 – LVCMOS25-24mA-Fast to LVCMOS25-16mA-Fast Comparison

Delta 13 examines the variation to peak level emissions between the 'LVCMOS25-24mA-Fast' and the 'LVCMOS25-16mA-Fast' driver settings. Ultimately quantifying the change to emissions between 24mA to 16mA drive strength when using the LVCMOS25 technology using Equation 36.

$$\Delta_{13} = A_{LVCMOS25(24mA)} - A_{LVCMOS25(16mA)}$$

Equation 36: Drive Strength Testing: Delta 13 – LVCMOS25 24mA to 16mA Comparison

Where A_n is the vector that holds the peak level of emissions and Δ_n is the comparison equation.

The maxima of 10.68dB is recorded at approximately 505MHz, this is the highest point where the 24mA setting is greater than the 16mA setting in terms of the peak level of emissions. The minima of –10.99dB is recorded at approximately 520MHz, with the minima depicting the point where the 16mA setting is higher than the 24mA setting again in terms of the peak level of emissions recorded. The average level of change across the observed spectrum between the 24mA and 16mA drive strength settings is -2.169dB. Figure 107 illustrates the plot for this comparison.

5.4.3.2 Delta 14 – LVCMOS25-24mA-Fast to LVCMOS25-12mA-Fast Comparison

Delta 14 examines the variation to peak level emissions between the 'LVCMOS25-24mA-Fast' and the 'LVCMOS25-12mA-Fast' driver settings. Ultimately quantifying the change to emissions between 24mA to 12mA drive strength when using the LVCMOS25 technology using Equation 37.

$$\Delta_{14} = A_{LVCMOS25(24mA)} - A_{LVCMOS25(12mA)}$$

Equation 37: Drive Strength Testing: Delta 14 – LVCMOS25 24mA to 12mA Comparison

Where A_n is the vector that holds the peak level of emissions and Δ_n is the comparison equation.

The maxima of 6.3dB is recorded at approximately 505MHz, this is the highest point where the 24mA setting is greater than the 12mA setting in terms of the peak level of emissions. The minima of –9.44dB is recorded at approximately 510MHz, with the minima depicting the point where the 12mA setting is higher than the 24mA setting again in terms of the peak level of emissions recorded. The average level of change across the observed spectrum between the 24mA and 12mA drive strength settings is -1.678dB. Figure 108 illustrates the plot for this comparison.

5.4.3.3 Delta 15 – LVCMOS25-24mA-Fast to LVCMOS25-8mA-Fast Comparison

Delta 15 examines the variation to peak level emissions between the 'LVCMOS25-24mA-Fast' and the 'LVCMOS25-8mA-Fast' driver settings. Ultimately quantifying the change to emissions between 24mA to 8mA drive strength when using the LVCMOS25 technology using Equation 38.

$$\Delta_{15} = A_{LVCMOS25(24mA)} - A_{LVCMOS25(8mA)}$$

Equation 38: Drive Strength Testing: Delta 15 – LVCMOS25 24mA to 8mA Comparison

Where A_n is the vector that holds the peak level of emissions and Δ_n is the comparison equation.

The maxima of 10.51dB is recorded at approximately 505MHz, this is the highest point where the 24mA setting is greater than the 8mA setting in terms of the peak level of emissions. The minima of –9.14dB is recorded at approximately 510MHz, with the minima depicting the point where the 8mA setting is higher than the 24mA setting again in terms of the peak level of emissions recorded. The average level of change across the observed spectrum between the 24mA and 8mA drive strength settings is -3.18dB. Figure 109 illustrates the plot for this comparison.

5.4.3.4 Delta 16 – LVCMOS25-24mA-Fast to LVCMOS25-6mA-Fast Comparison

Delta 16 examines the variation to peak level emissions between the 'LVCMOS25-24mA-Fast' and the 'LVCMOS25-6mA-Fast' driver settings. Ultimately quantifying the change to emissions between 24mA to 6mA drive strength when using the LVCMOS25 technology using Equation 39.

$$\Delta_{16} = A_{LVCMOS25(24mA)} - A_{LVCMOS25(6mA)}$$

Equation 39: Drive Strength Testing: Delta 16 – LVCMOS25 24mA to 6mA Comparison

Where A_n is the vector that holds the peak level of emissions and Δ_n is the comparison equation.

The maxima of 10.74dB is recorded at approximately 330MHz, this is the highest point where the 24mA setting is greater than the 6mA setting in terms of the peak level of emissions. The minima of –7.61dB is recorded at approximately 205MHz, with the minima depicting the point where the 6mA setting is higher than the 24mA setting again in terms of the peak level of emissions recorded. The average level of change across the observed spectrum between the 24mA and 6mA drive strength settings is -3.75dB. Figure 110 illustrates the plot for this comparison.

5.4.3.5 Delta 17 – LVCMOS25-24mA-Fast to LVCMOS25-4mA-Fast Comparison

Delta 17 examines the variation to peak level emissions between the 'LVCMOS25-24mA-Fast' and the 'LVCMOS25-4mA-Fast' driver settings. Ultimately quantifying the change to emissions between 24mA to 4mA drive strength when using the LVCMOS25 technology using Equation 40.

$$\Delta_{17} = A_{LVCMOS25(24mA)} - A_{LVCMOS25(4mA)}$$

Equation 40: Drive Strength Testing: Delta 17 – LVCMOS25 24mA to 4mA Comparison

Where A_n is the vector that holds the peak level of emissions and Δ_n is the comparison equation.

The maxima of 14.89dB is recorded at approximately 310MHz, this is the highest point where the 24mA setting is greater than the 4mA setting in terms of the peak level of emissions. The minima of –-14.2dB is recorded at approximately 550MHz, with the minima depicting the point where the 4mA setting is higher than the 24mA setting again in terms of the peak level of emissions recorded. The average level of change across the observed spectrum between the 24mA and 4mA drive strength settings is -4.64dB. Figure 111 illustrates the plot for this comparison.

5.4.3.6 Delta 18 – LVCMOS25-24mA-Fast to LVCMOS25-2mA-Fast Comparison

Delta 18 examines the variation to peak level emissions between the 'LVCMOS25-24mA-Fast' and the 'LVCMOS25-2mA-Fast' driver settings. Ultimately quantifying the change to emissions between 24mA to 2mA drive strength when using the LVCMOS25 technology using Equation 41.

$$\Delta_{18} = A_{LVCMOS25(24mA)} - A_{LVCMOS25(2mA)}$$

Equation 41: Drive Strength Testing: Delta 18 – LVCMOS25 24mA to 2mA Comparison

Where A_n is the vector that holds the peak level of emissions and Δ_n is the comparison equation.

The maxima of 23.2dB is recorded at approximately 330MHz, this is the highest point where the 24mA setting is greater than the 2mA setting in terms of the peak level of emissions. The minima of –-9.05dB is recorded at approximately 520MHz, with the minima depicting the point where the 2mA setting is higher than the 24mA setting again in terms of the peak level of emissions recorded. The average level of change across the observed spectrum between the 24mA and 2mA drive strength settings is -9.16dB. Figure 112 illustrates the plot for this comparison.

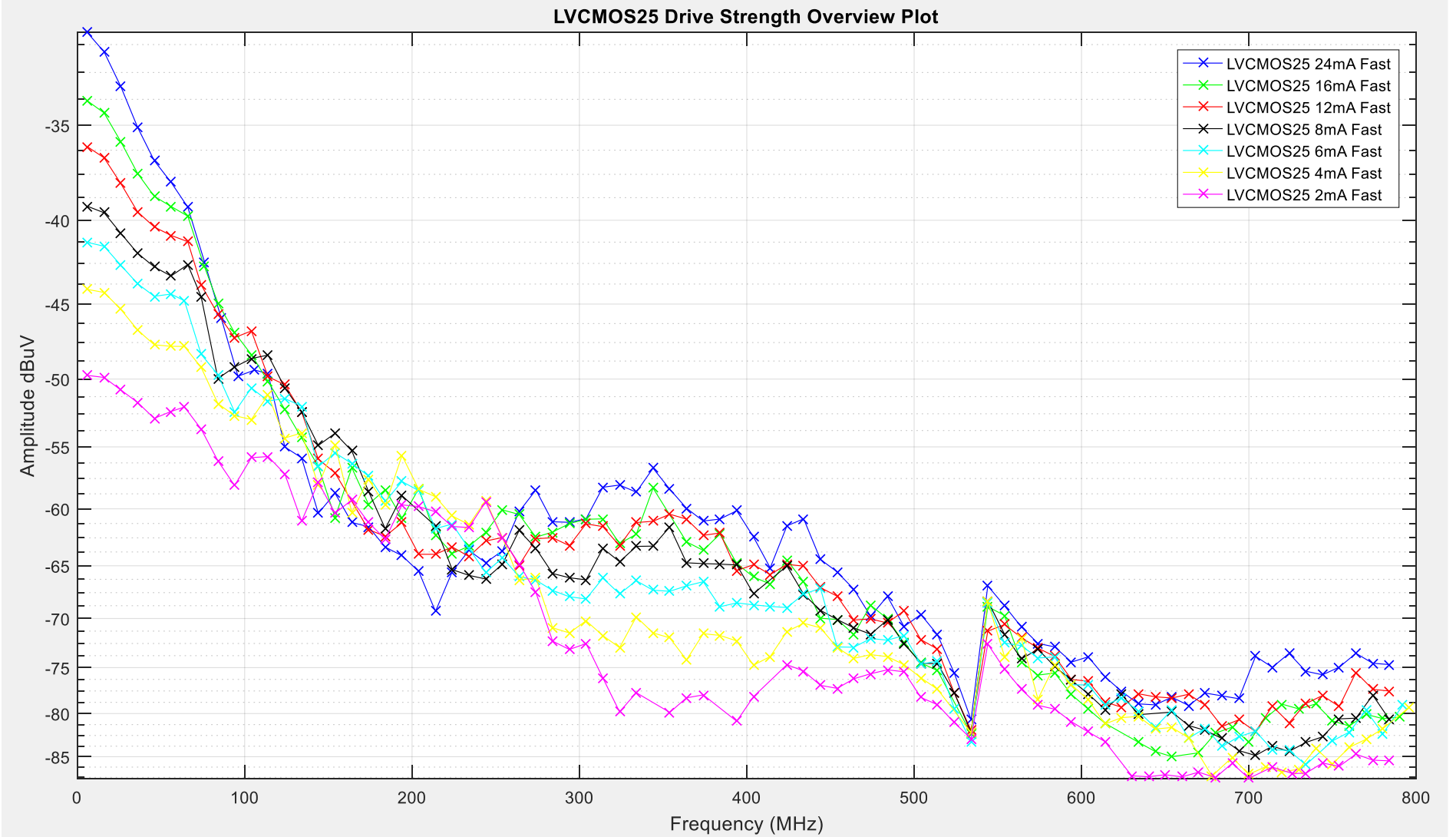


Figure 105: LVCMOS25 Drive Strength Overview Plot

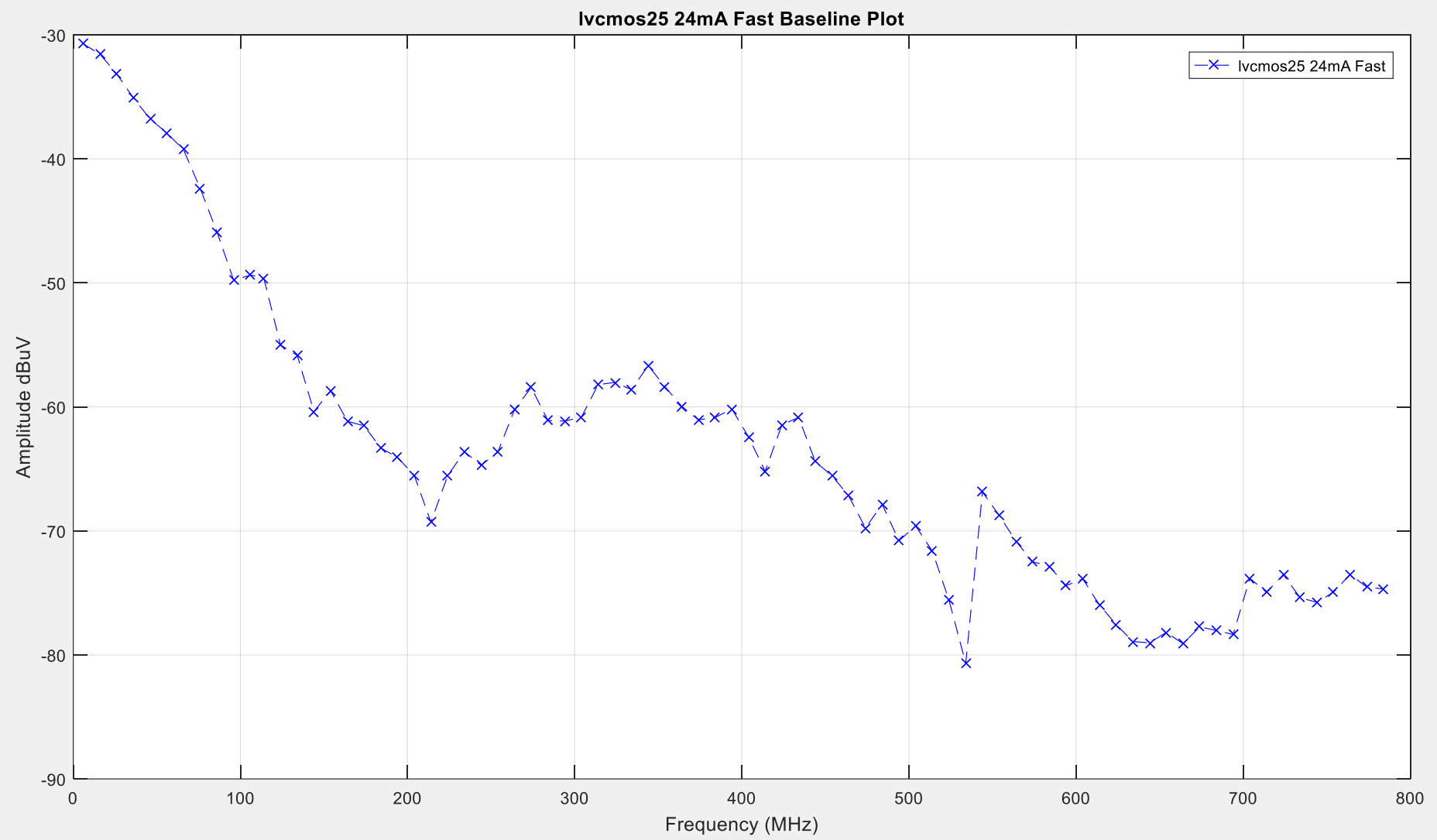


Figure 106: LVCMOS25 Drive Strength Baseline Plot

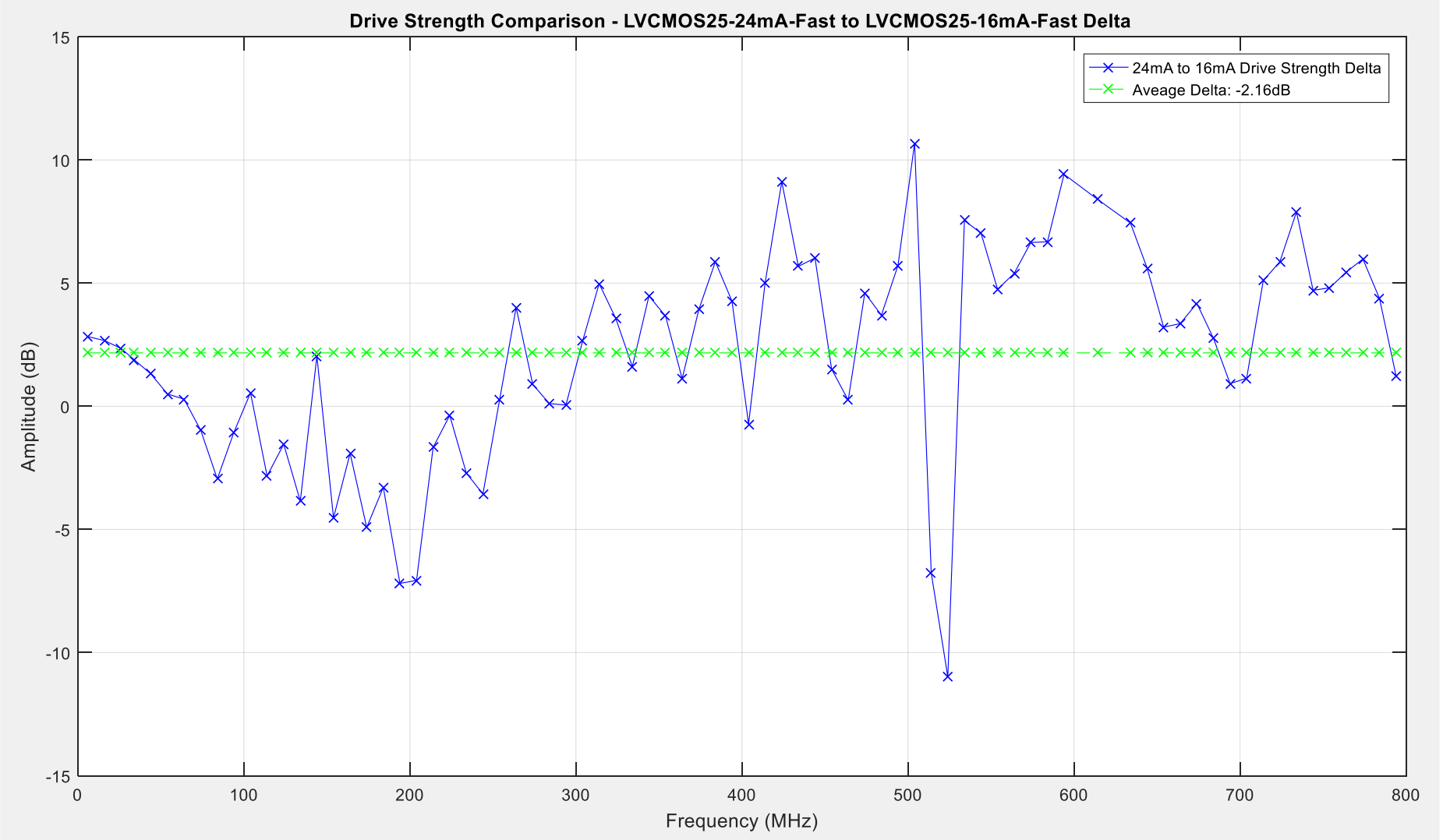


Figure 107: LVCMOS25-24mA-Fast to LVCMOS25-16mA-Fast Drive Strength Comparison

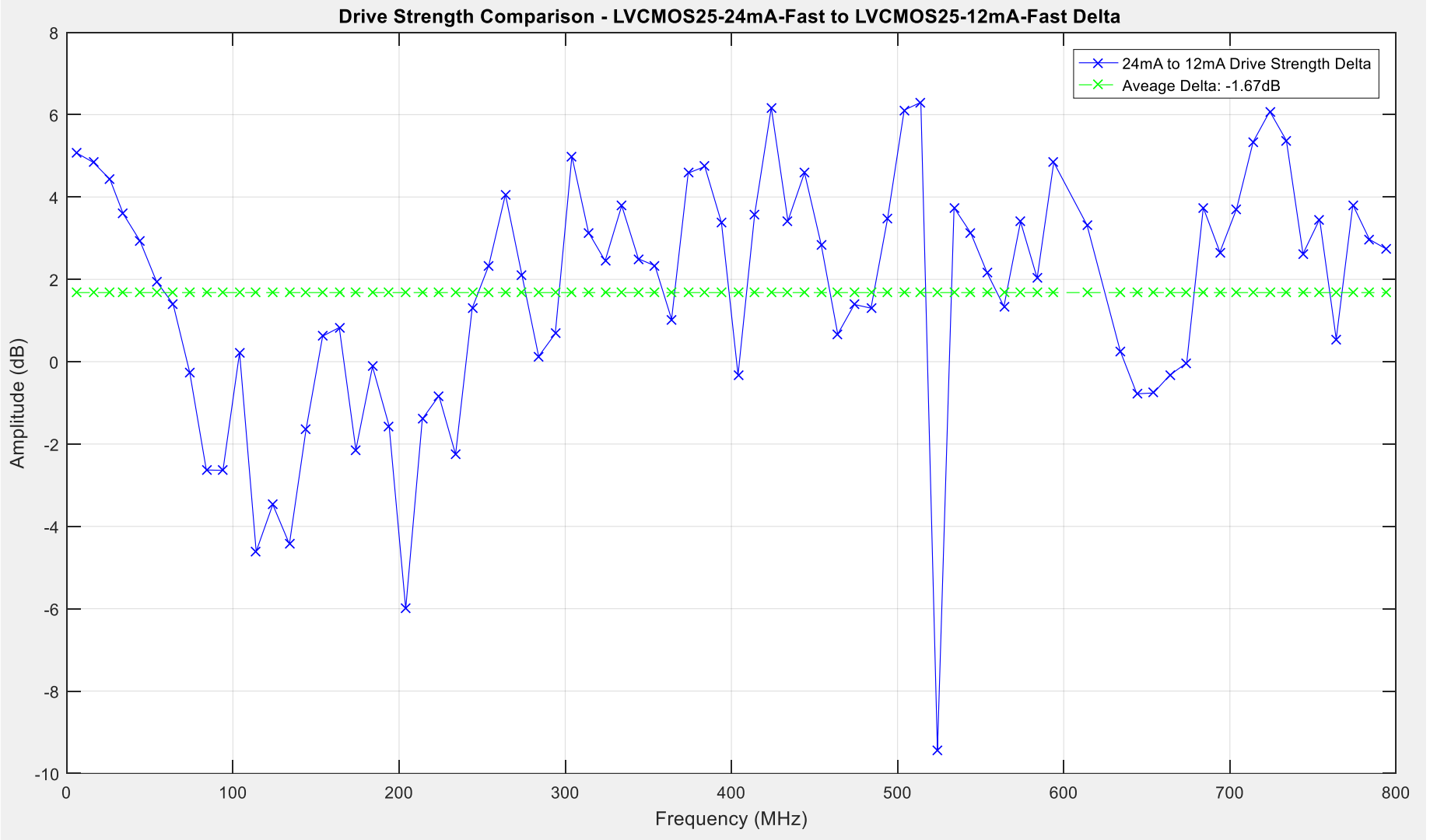


Figure 108: LVCMOS25-24mA-Fast to LVCMOS25-12mA-Fast Drive Strength Comparison

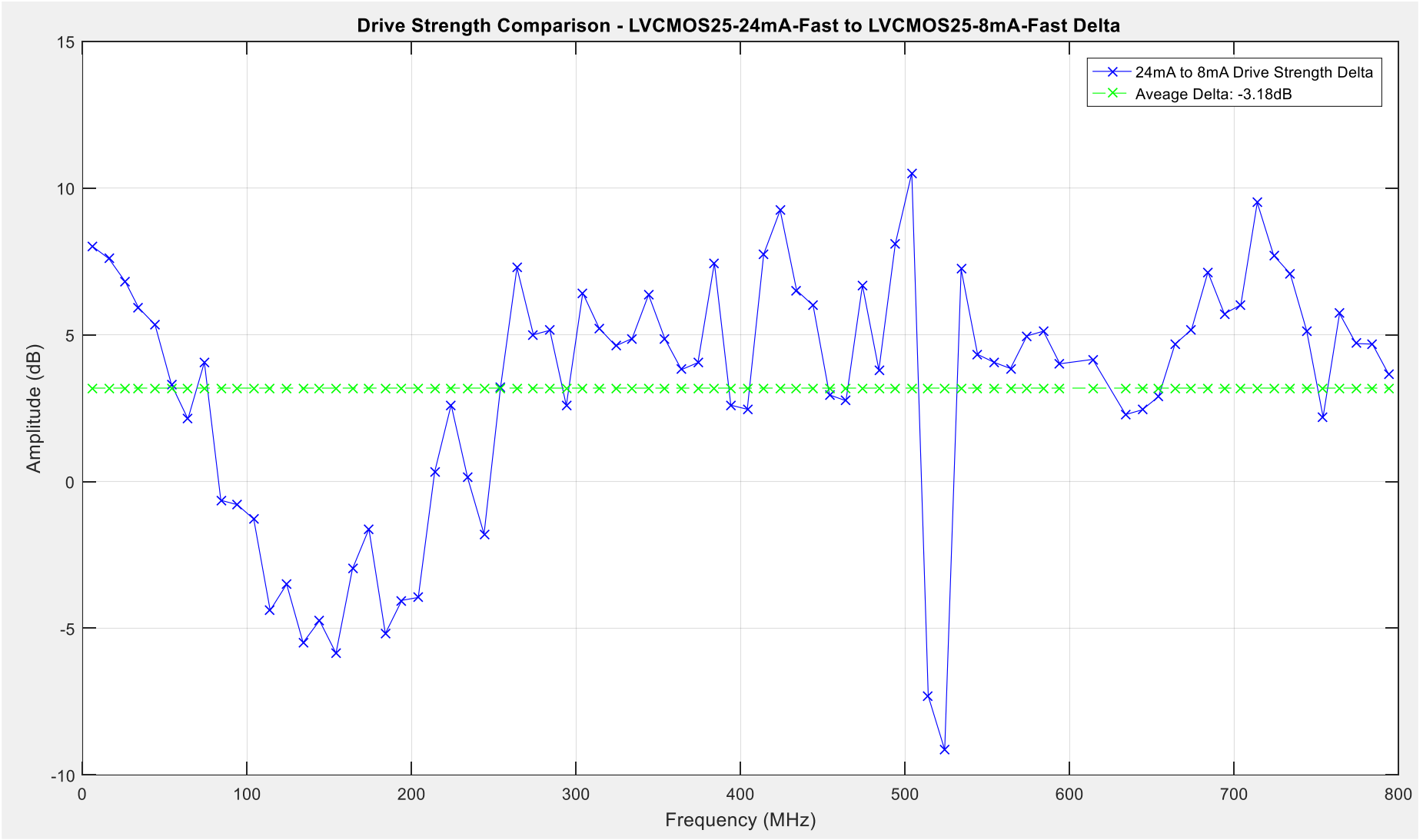


Figure 109: LVCMOS25-24mA-Fast to LVCMOS25-8mA-Fast Drive Strength Comparison

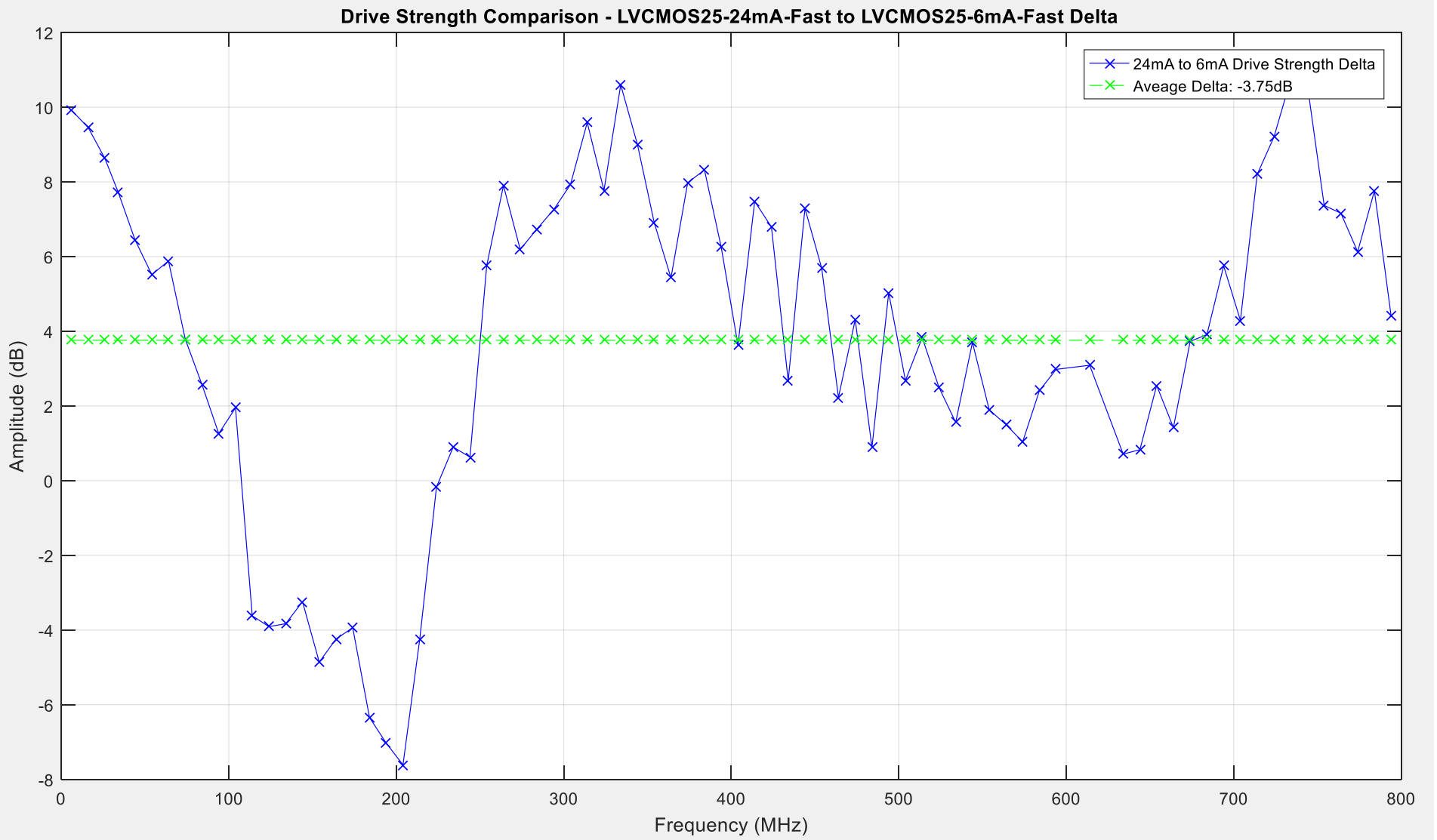


Figure 110: LVCMOS25-24mA-Fast to LVCMOS25-6mA-Fast Drive Strength Comparison

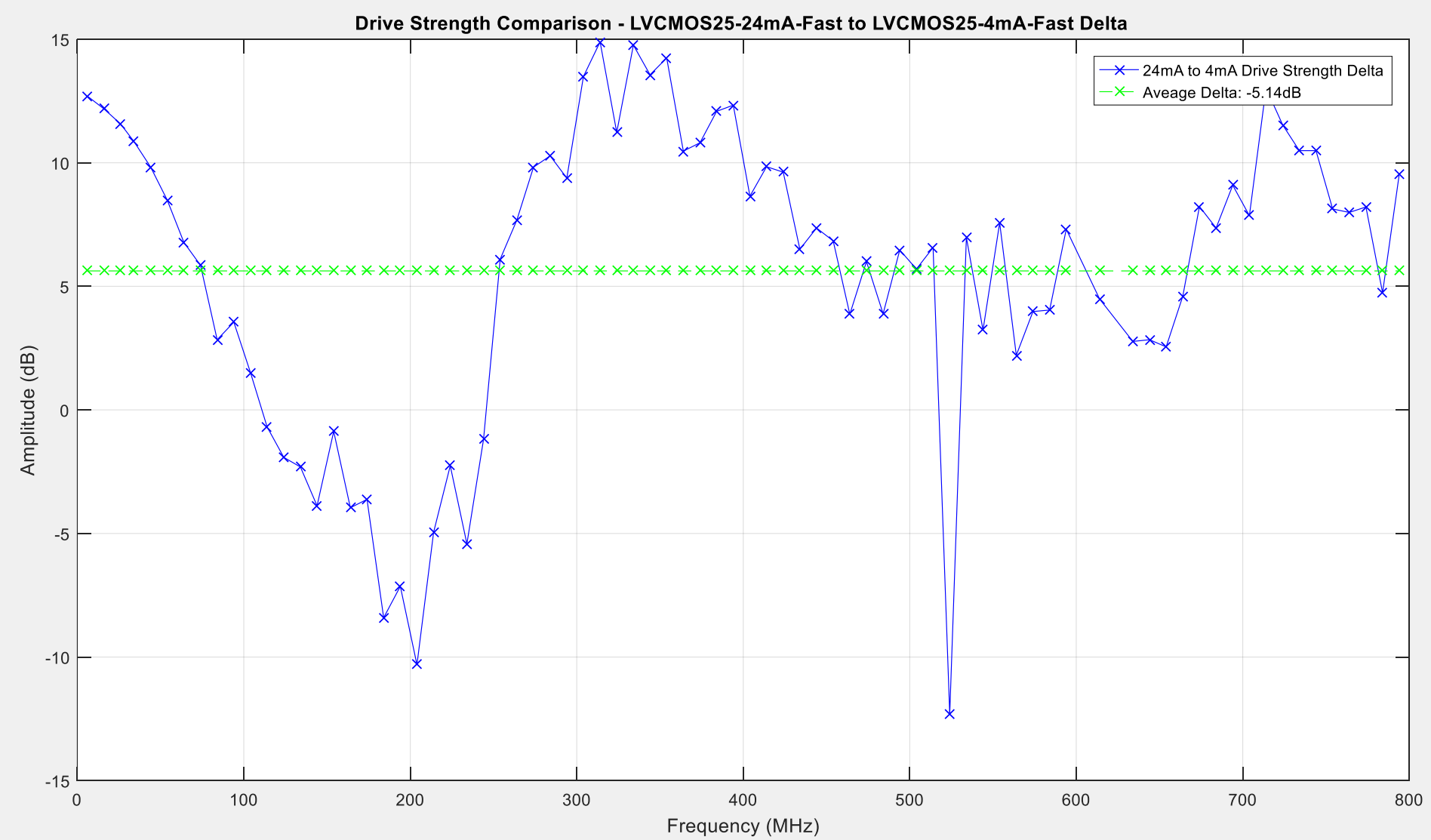


Figure 111: LVCMOS25-24mA-Fast to LVCMOS25-4mA-Fast Drive Strength Comparison

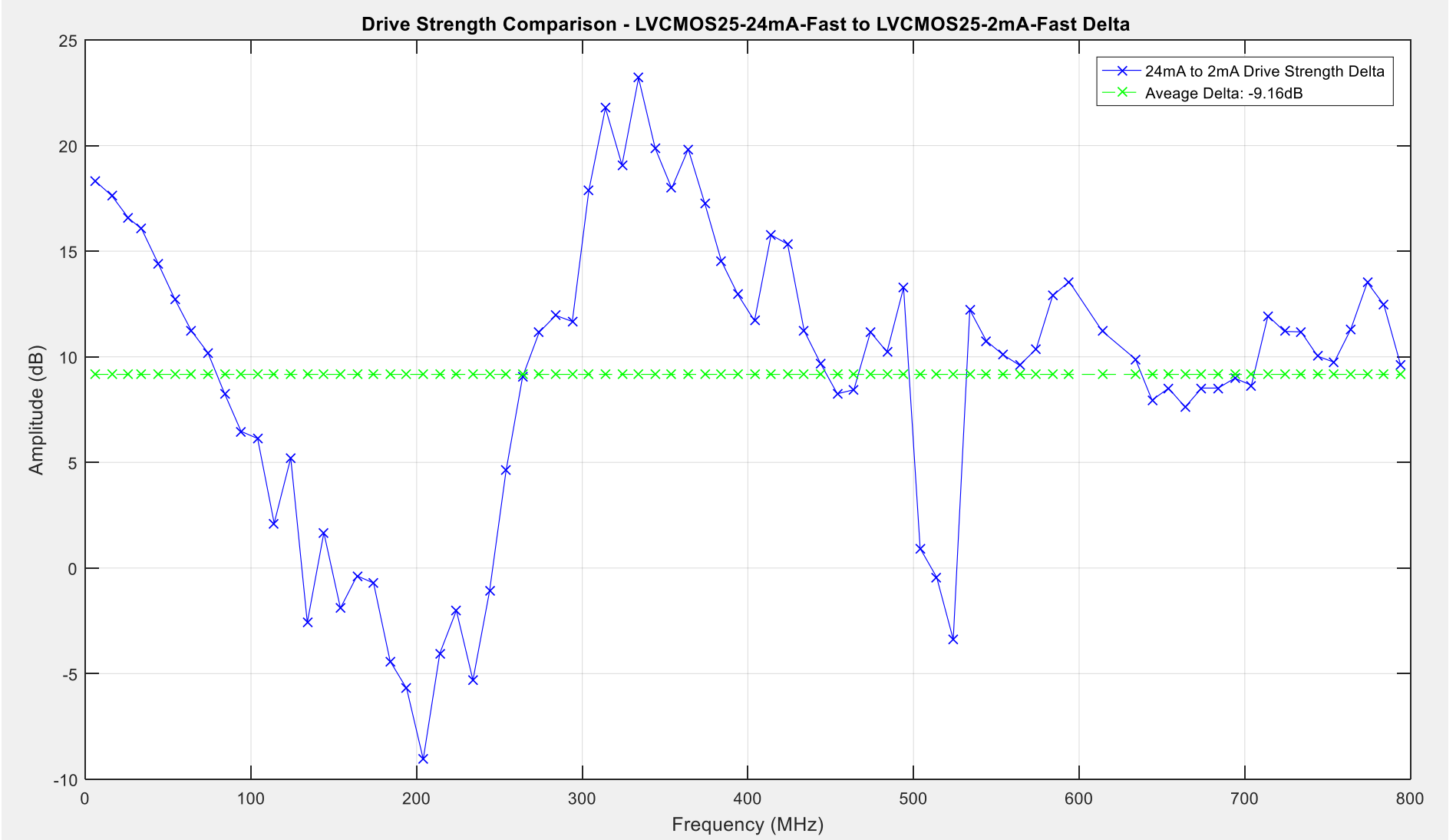


Figure 112: LVCMOS25-24mA-Fast to LVCMOS25-2mA-Fast Drive Strength Comparison

5.4.4 LVCMOS18 Drive Strength Results

The traces illustrated in Figure 113 shows the peak level of emissions recorded for the LVCMOS18 I/O buffer drive strength settings detailed in Table 23 below.

LVCMOS18 Setting	Average Noise Level dBµV	Delta Comparison dB
LVCMOS18-24mA-Fast	-62.9278	0
LVCMOS18-16mA-Fast	-63.8729	0.6919
LVCMOS18-12mA-Fast	-64.4889	2.0722
LVCMOS18-8mA-Fast	-66.2304	2.7736
LVCMOS18-6mA-Fast	-67.583	3.6155
LVCMOS18-4mA-Fast	-69.1953	5.5682
LVCMOS18-2mA-Fast	-72.7413	9.2812

Table 23: LVCMOS18 Drive Strength Emissions Levels Overview

From these results obtained it gives an indication of how much variation occurs on average across the peak levels but does not give an indication of how this variation is distributed across the emissions spectrum. To achieve a more detailed comparison between the I/O driver settings, closer comparisons have been done to illustrate how the level of emissions varies across the observed spectrum. The 'LVCMOS18-24mA-Fast' I/O driver setting has been used as the baseline for the following 6 comparisons, for reference this trace is illustrated in Figure 114. The LVCMOS18-24mA-Fast drive strength testing has an average level of peak emissions of 62.9278dBµV.

5.4.4.1 Delta 19 – LVCMOS18-24mA-Fast to LVCMOS18-16mA-Fast Comparison

Delta 19 examines the variation to peak level emissions between the 'LVCMOS18-24mA-Fast' and the 'LVCMOS18-16mA-Fast' driver settings. Ultimately quantifying the change to emissions between 24mA to 16mA drive strength when using the LVCMOS18 technology using Equation 42.

$$\Delta_{19} = A_{LVCMOS25(24mA)} - A_{LVCMOS25(16mA)}$$

Equation 42: Drive Strength Testing: Delta 19 – LVCMOS18 24mA to 16mA Comparison

Where A_n is the vector that holds the peak level of emissions and Δ_n is the comparison equation.

The maxima of 10.79dB is recorded at approximately 150MHz, this is the highest point where the 24mA setting is greater than the 16mA setting in terms of the peak level of emissions. The minima of –9.61dB is recorded at approximately 520MHz, with the minima depicting the point where the 16mA setting is higher than the 24mA setting again in terms of the peak level of emissions recorded. The average level of change across the observed spectrum between the 24mA and 16mA drive strength settings is -0.6919dB. Figure 115 illustrates the plot for this comparison.

5.4.4.2 Delta 20 – LVCMOS18-24mA-Fast to LVCMOS18-12mA-Fast Comparison

Delta 20 examines the variation to peak level emissions between the 'LVCMOS18-24mA-Fast' and the 'LVCMOS18-12mA-Fast' driver settings. Ultimately quantifying the change to emissions between 24mA to 12mA drive strength when using the LVCMOS18 technology using Equation 43.

$$\Delta_{20} = A_{LVCMOS25(24mA)} - A_{LVCMOS25(12mA)}$$

Equation 43: Drive Strength Testing: Delta 20 – LVCMOS18 24mA to 12mA Comparison

Where A_n is the vector that holds the peak level of emissions and Δ_n is the comparison equation.

The maxima of 16.63dB is recorded at approximately 450MHz, this is the highest point where the 24mA setting is greater than the 12mA setting in terms of the peak level of emissions. The minima of –8.98dB is recorded at approximately 160MHz, with the minima depicting the point where the 12mA setting is higher than the 24mA setting again in terms of the peak level of emissions recorded. The average level of change across the observed spectrum between the 24mA and 12mA drive strength settings is -2.0722dB. Figure 116 illustrates the plot for this comparison.

5.4.4.3 Delta 21 – LVCMOS18-24mA-Fast to LVCMOS18-8mA-Fast Comparison

Delta 21 examines the variation to peak level emissions between the 'LVCMOS18-24mA-Fast' and the 'LVCMOS18-8mA-Fast' driver settings. Ultimately quantifying the change to emissions between 24mA to 8mA drive strength when using the LVCMOS18 technology using Equation 44.

$$\Delta_{21} = A_{LVCMOS25(24mA)} - A_{LVCMOS25(8mA)}$$

Equation 44: Drive Strength Testing: Delta 21 – LVCMOS18 24mA to 8mA Comparison

Where A_n is the vector that holds the peak level of emissions and Δ_n is the comparison equation.

The maxima of 9.99dB is recorded at approximately 295MHz, this is the highest point where the 24mA setting is greater than the 8mA setting in terms of the peak level of emissions. The minima of –9.18dB is recorded at approximately 160MHz, with the minima depicting the point where the 8mA setting is higher than the 24mA setting again in terms of the peak level of emissions recorded. The average level of change across the observed spectrum between the 24mA and 8mA drive strength settings is -2.7736dB. Figure 117 illustrates the plot for this comparison.

5.4.4.4 Delta 22 – LVCMOS18-24mA-Fast to LVCMOS18-6mA-Fast Comparison

Delta 22 examines the variation to peak level emissions between the 'LVCMOS18-24mA-Fast' and the 'LVCMOS18-6mA-Fast' driver settings. Ultimately quantifying the change to emissions between 24mA to 6mA drive strength when using the LVCMOS18 technology using Equation 45.

$$\Delta_{22} = A_{LVCMOS25(24mA)} - A_{LVCMOS25(6mA)}$$

Equation 45: Drive Strength Testing: Delta 22 – LVCMOS18 24mA to 6mA Comparison

Where A_n is the vector that holds the peak level of emissions and Δ_n is the comparison equation.

The maxima of 10.94dB is recorded at approximately 350MHz, this is the highest point where the 24mA setting is greater than the 6mA setting in terms of the peak level of emissions. The minima of –11.02dB is recorded at approximately 150MHz, with the minima depicting the point where the 6mA setting is higher than the 24mA setting again in terms of the peak level of emissions recorded. The average level of change across the observed spectrum between the 24mA and 6mA drive strength settings is -3.6155dB. Figure 118 illustrates the plot for this comparison.

5.4.4.5 Delta 23 – LVCMOS18-24mA-Fast to LVCMOS18-4mA-Fast Comparison

Delta 23 examines the variation to peak level emissions between the 'LVCMOS18-24mA-Fast' and the 'LVCMOS18-4mA-Fast' driver settings. Ultimately quantifying the change to emissions between 24mA to 4mA drive strength when using the LVCMOS18 technology using Equation 46.

$$\Delta_{23} = A_{LVCMOS25(24mA)} - A_{LVCMOS25(4mA)}$$

Equation 46: Drive Strength Testing: Delta 23 – LVCMOS18 24mA to 4mA Comparison

Where A_n is the vector that holds the peak level of emissions and Δ_n is the comparison equation.

The maxima of 14.23dB is recorded at approximately 350MHz, this is the highest point where the 24mA setting is greater than the 4mA setting in terms of the peak level of emissions. The minima of –-7.9dB is recorded at approximately 150MHz, with the minima depicting the point where the 4mA setting is higher than the 24mA setting again in terms of the peak level of emissions recorded. The average level of change across the observed spectrum between the 24mA and 4mA drive strength settings is -5.5682dB. Figure 119 illustrates the plot for this comparison.

5.4.4.6 Delta 24 – LVCMOS18-24mA-Fast to LVCMOS18-2mA-Fast Comparison

Delta 24 examines the variation to peak level emissions between the 'LVCMOS18-24mA-Fast' and the 'LVCMOS18-2mA-Fast' driver settings. Ultimately quantifying the change to emissions between 24mA to 2mA drive strength when using the LVCMOS18 technology using Equation 47.

$$\Delta_{24} = A_{LVCMOS25(24mA)} - A_{LVCMOS25(2mA)}$$

Equation 47: Drive Strength Testing: Delta 24 – LVCMOS18 24mA to 2mA Comparison

Where A_n is the vector that holds the peak level of emissions and Δ_n is the comparison equation.

The maxima of 19.57dB is recorded at approximately 350MHz, this is the highest point where the 24mA setting is greater than the 2mA setting in terms of the peak level of emissions. The minima of –-5.95dB is recorded at approximately 150MHz, with the minima depicting the point where the 2mA setting is higher than the 24mA setting again in terms of the peak level of emissions recorded. The average level of change across the observed spectrum between the 24mA and 2mA drive strength settings is -9.28dB. Figure 120 illustrates the plot for this comparison.

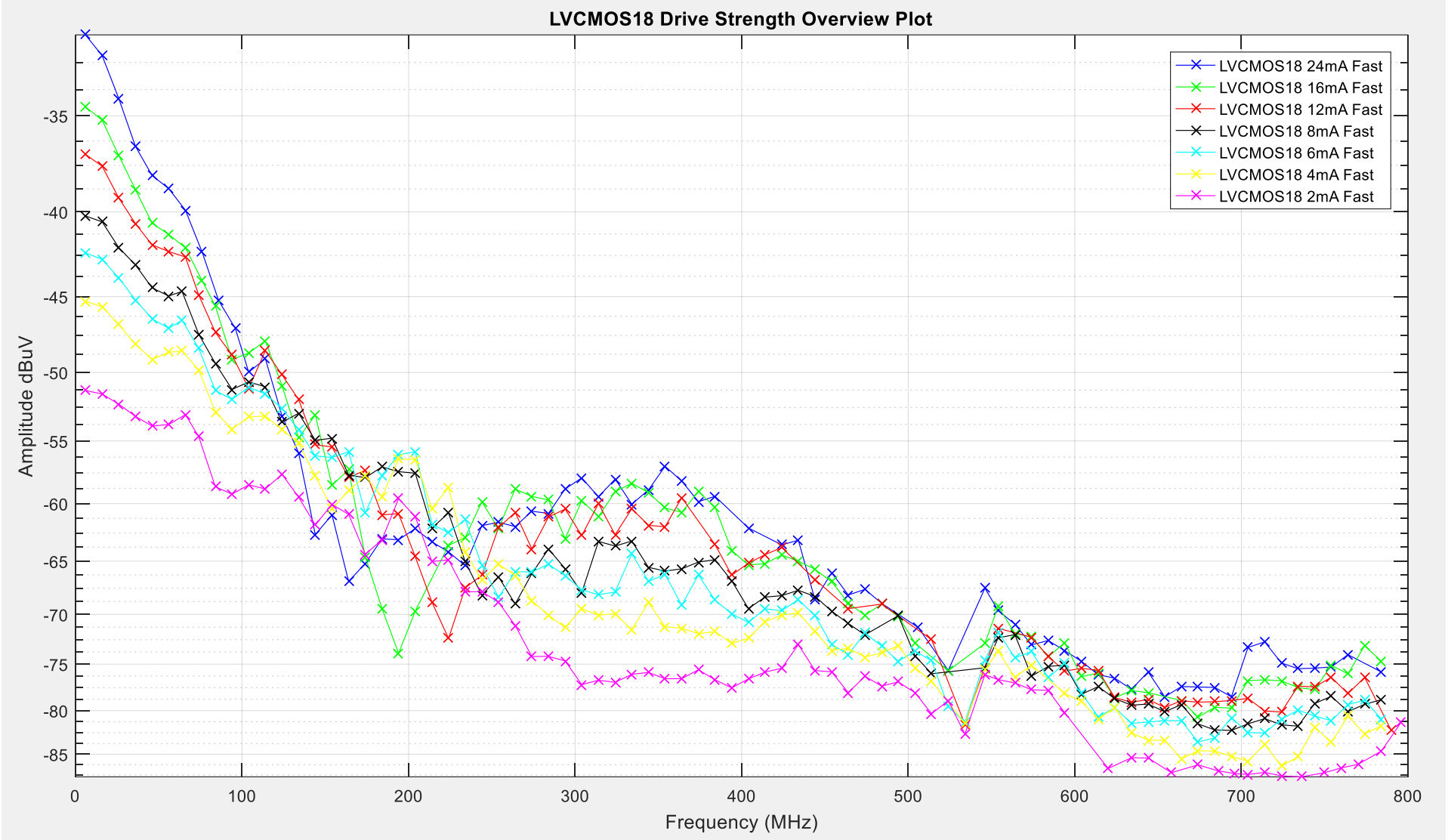


Figure 113: LVCMOS18 Drive Strength Overview Plot

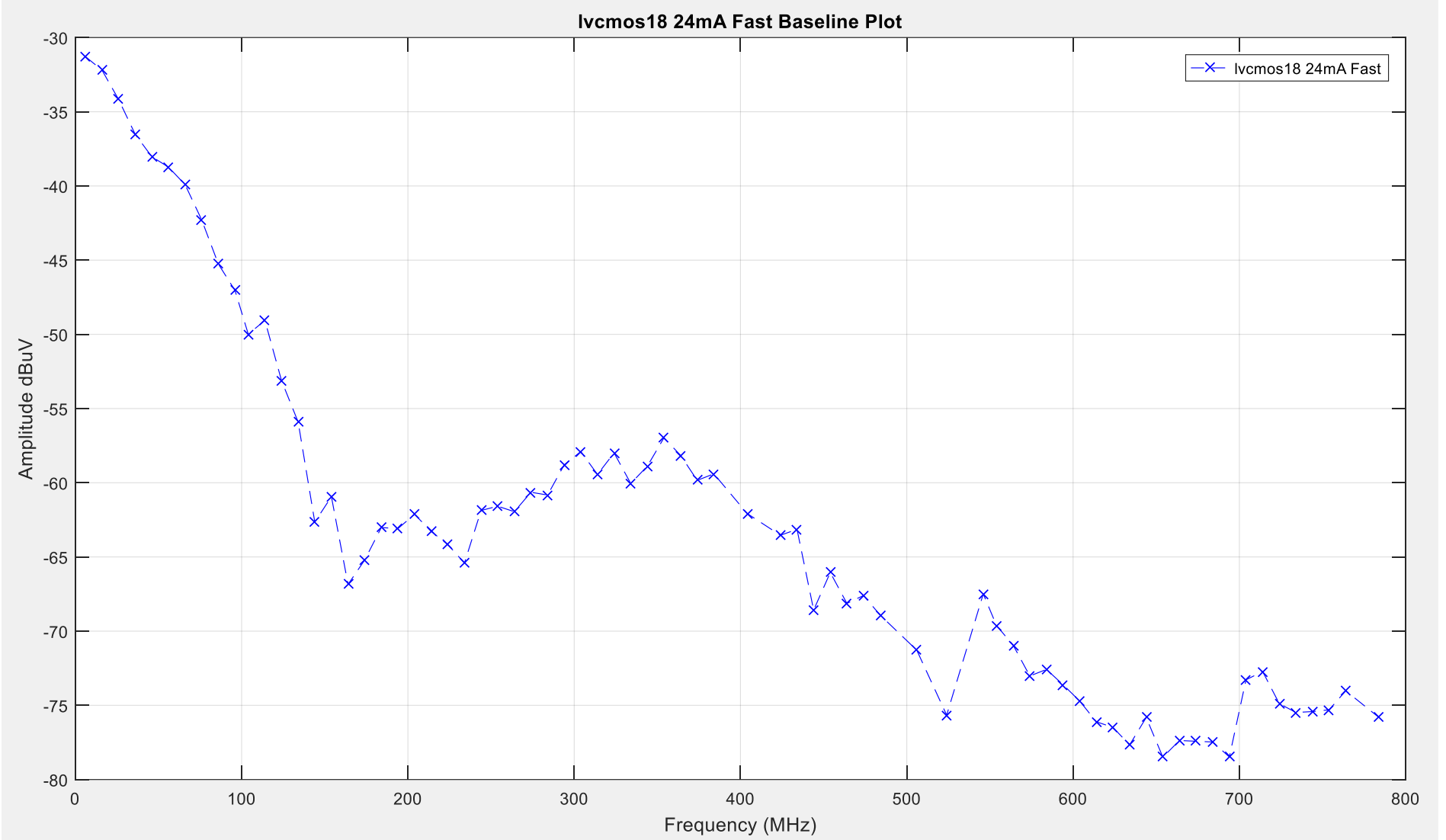


Figure 114: LVCMOS18 Drive Strength Baseline Plot

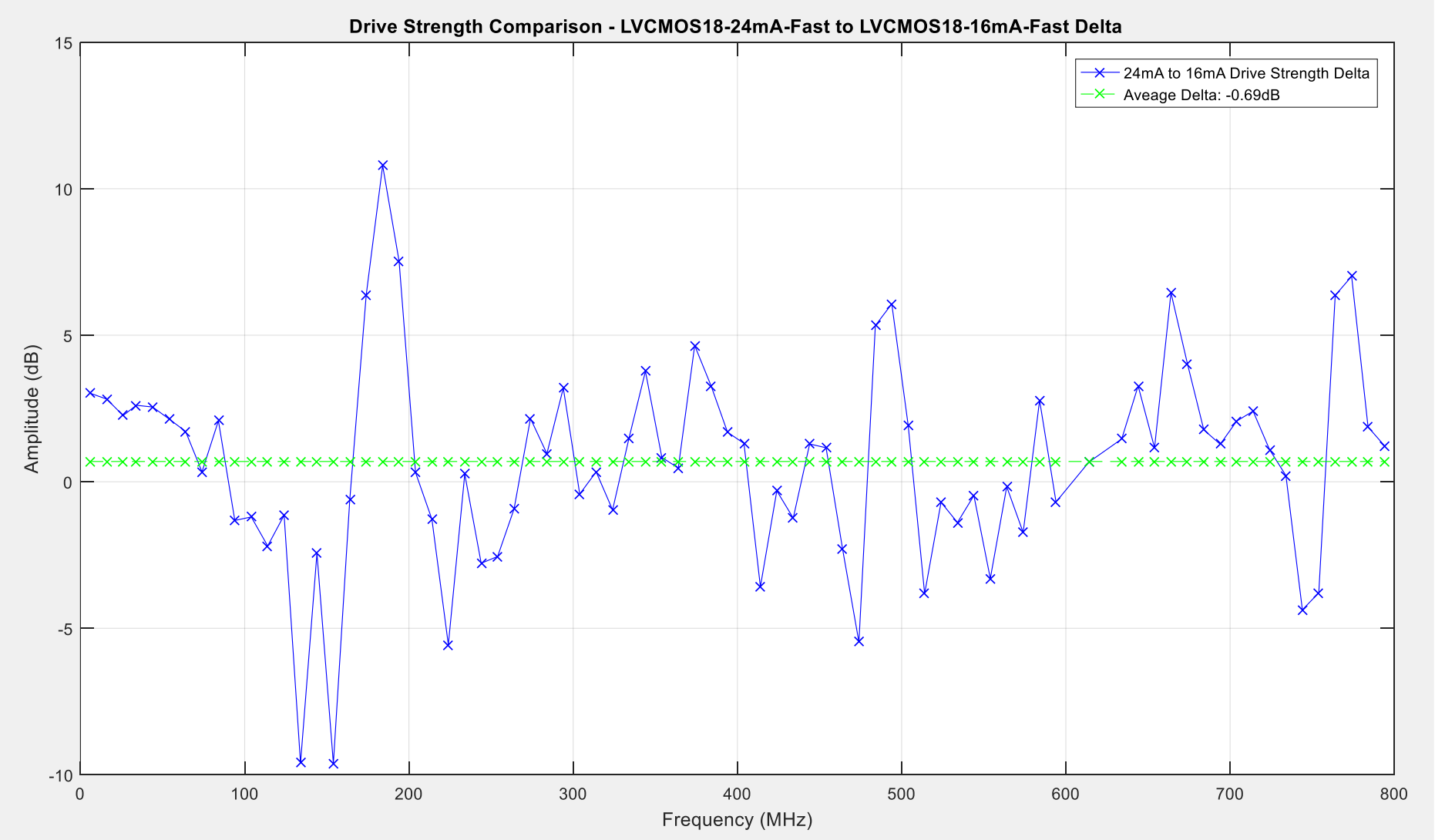


Figure 115: LVCMOS18-24mA-Fast to LVCMOS18-16mA-Fast Drive Strength Comparison

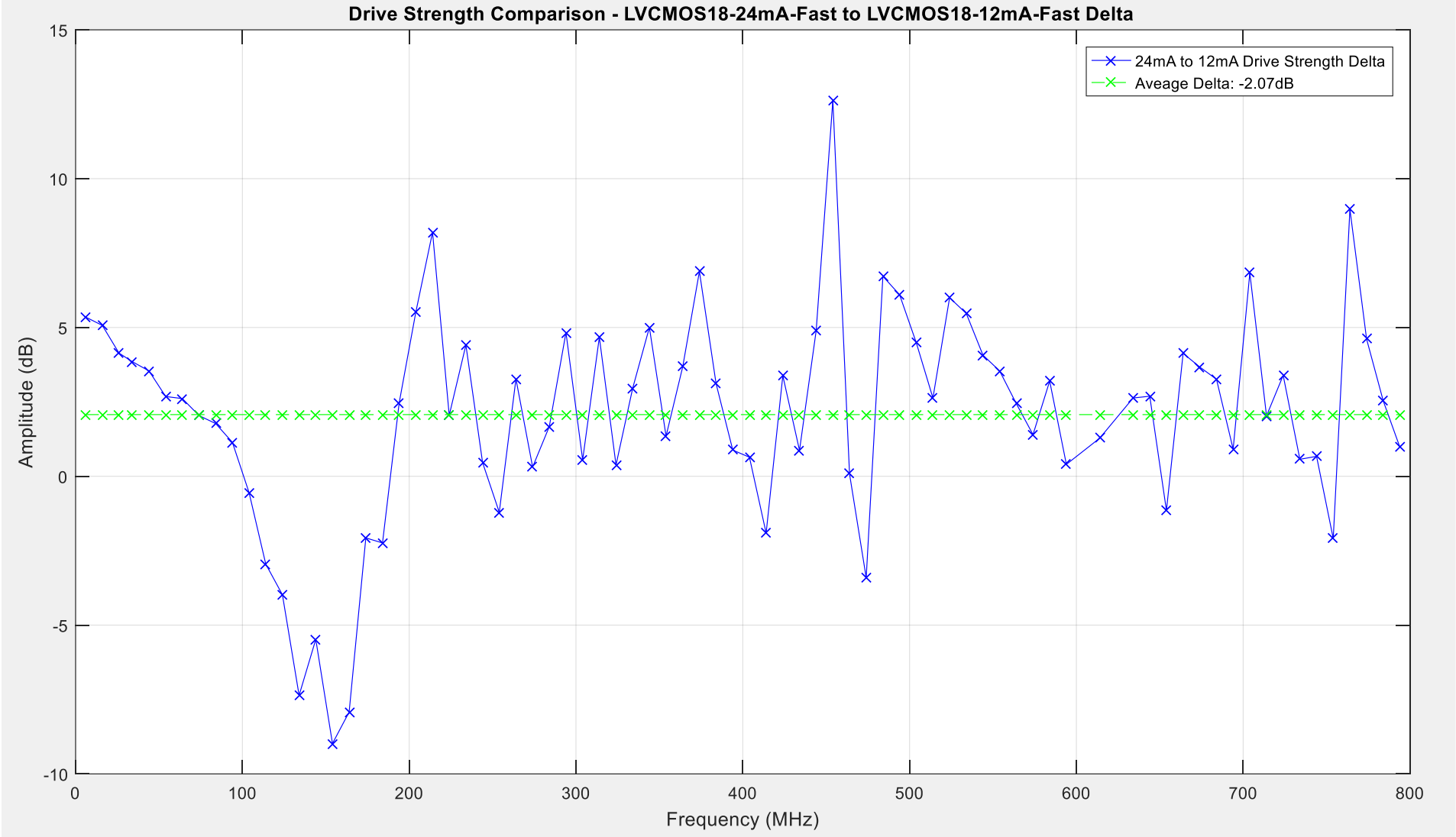


Figure 116: LVCMOS18-24mA-Fast to LVCMOS18-12mA-Fast Drive Strength Comparison

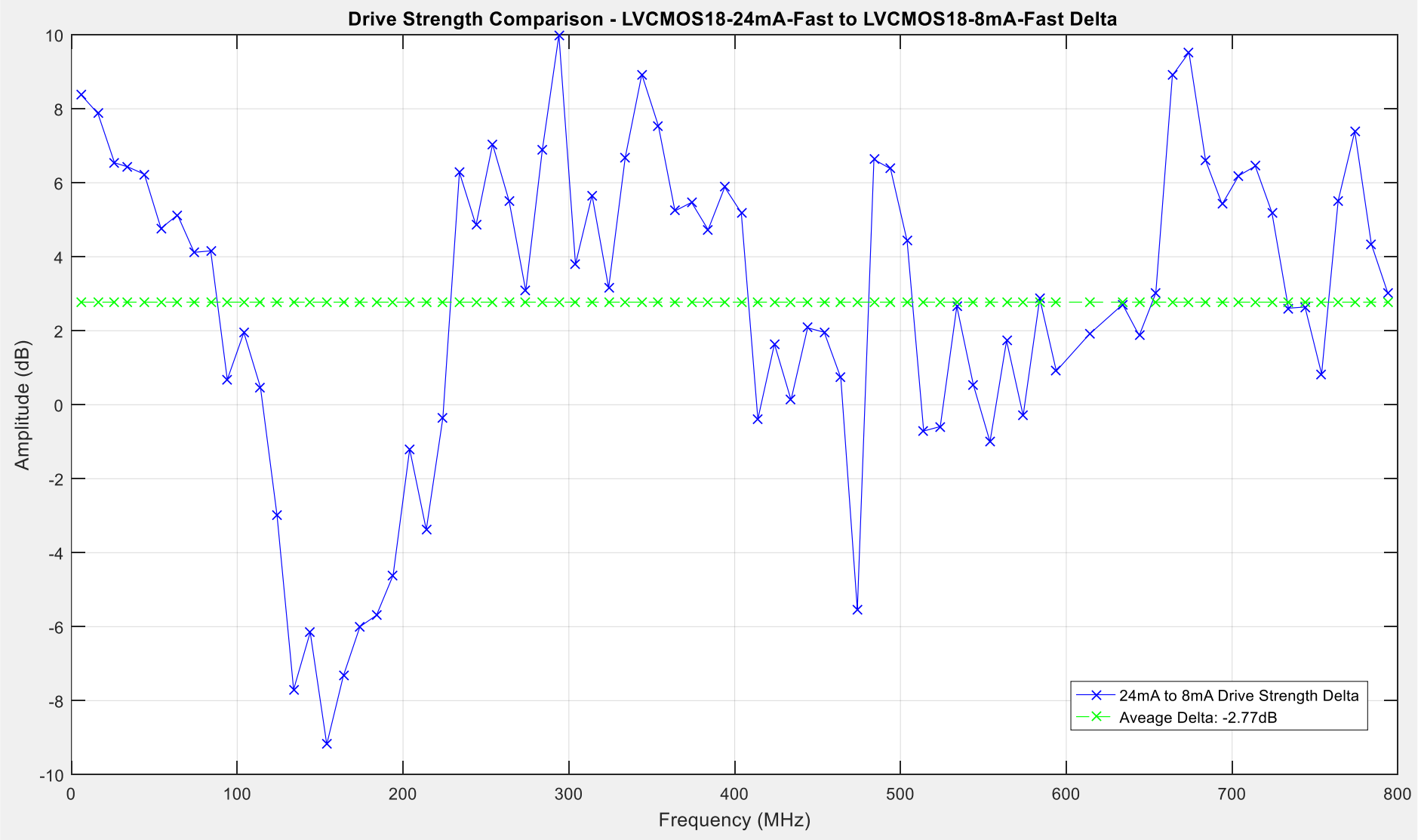


Figure 117: LVCMOS18-24mA-Fast to LVCMOS18-8mA-Fast Drive Strength Comparison

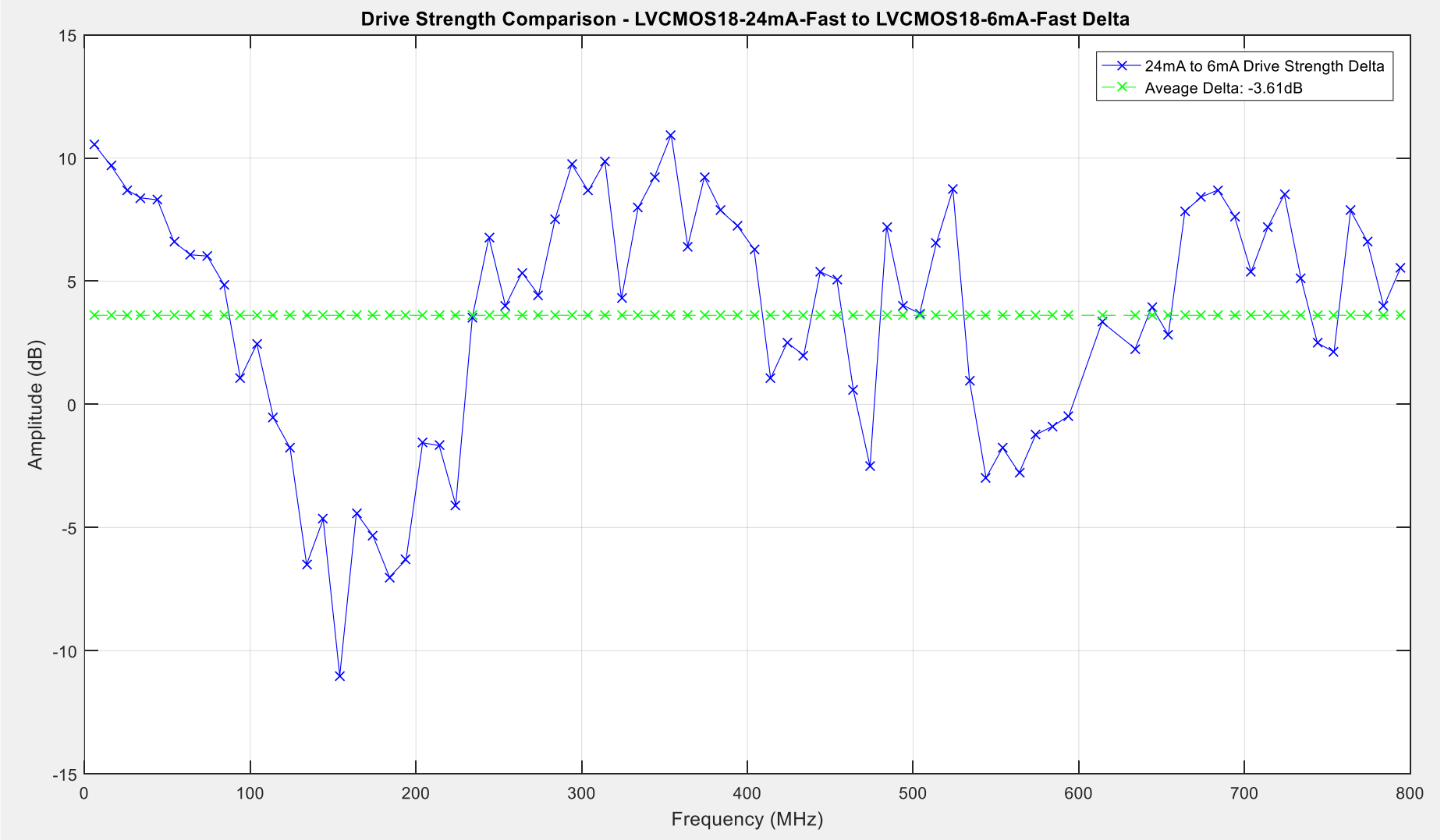


Figure 118: LVCMOS18-24mA-Fast to LVCMOS18-6mA-Fast Drive Strength Comparison

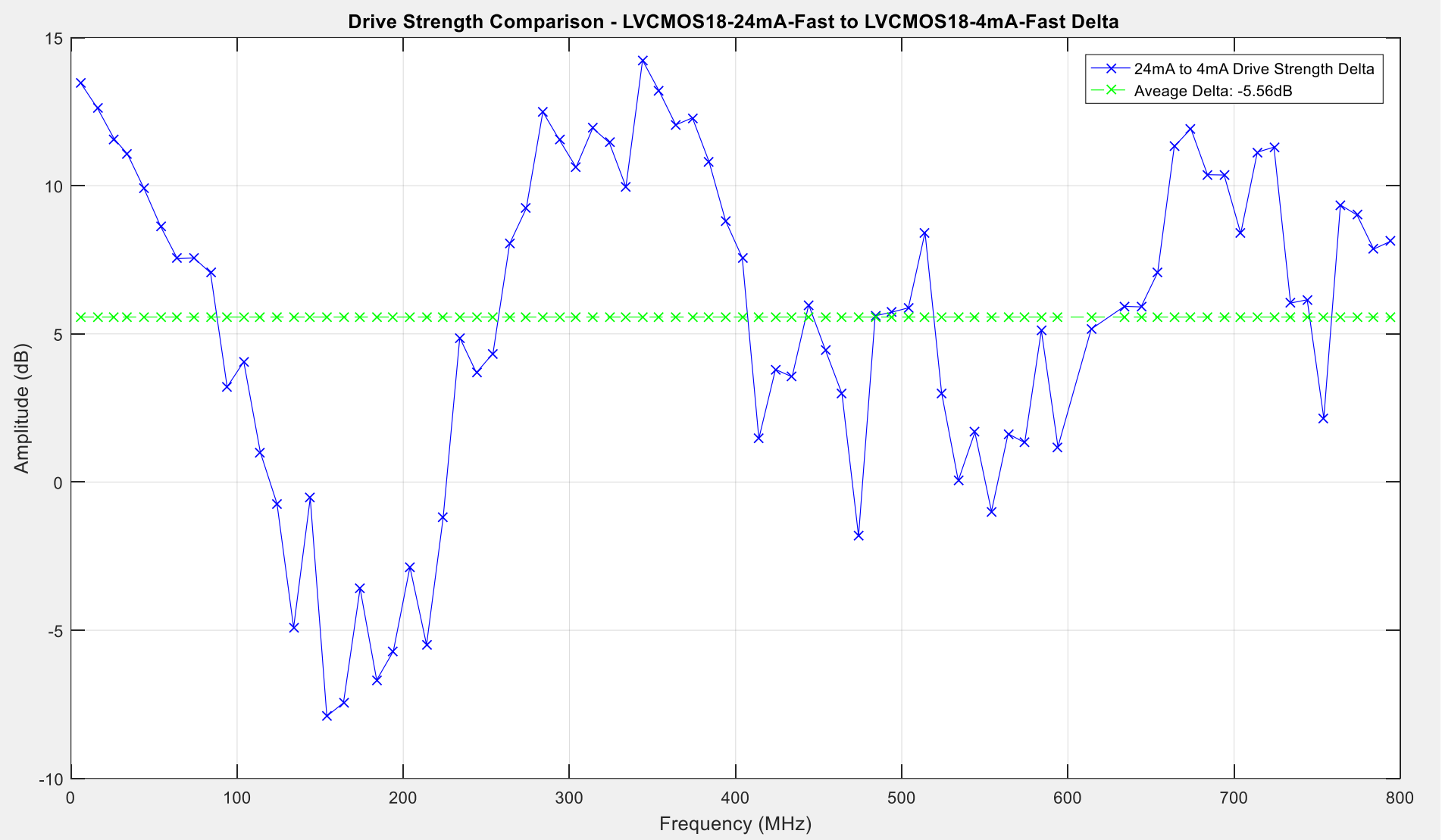


Figure 119: LVCMOS18-24mA-Fast to LVCMOS18-4mA-Fast Drive Strength Comparison

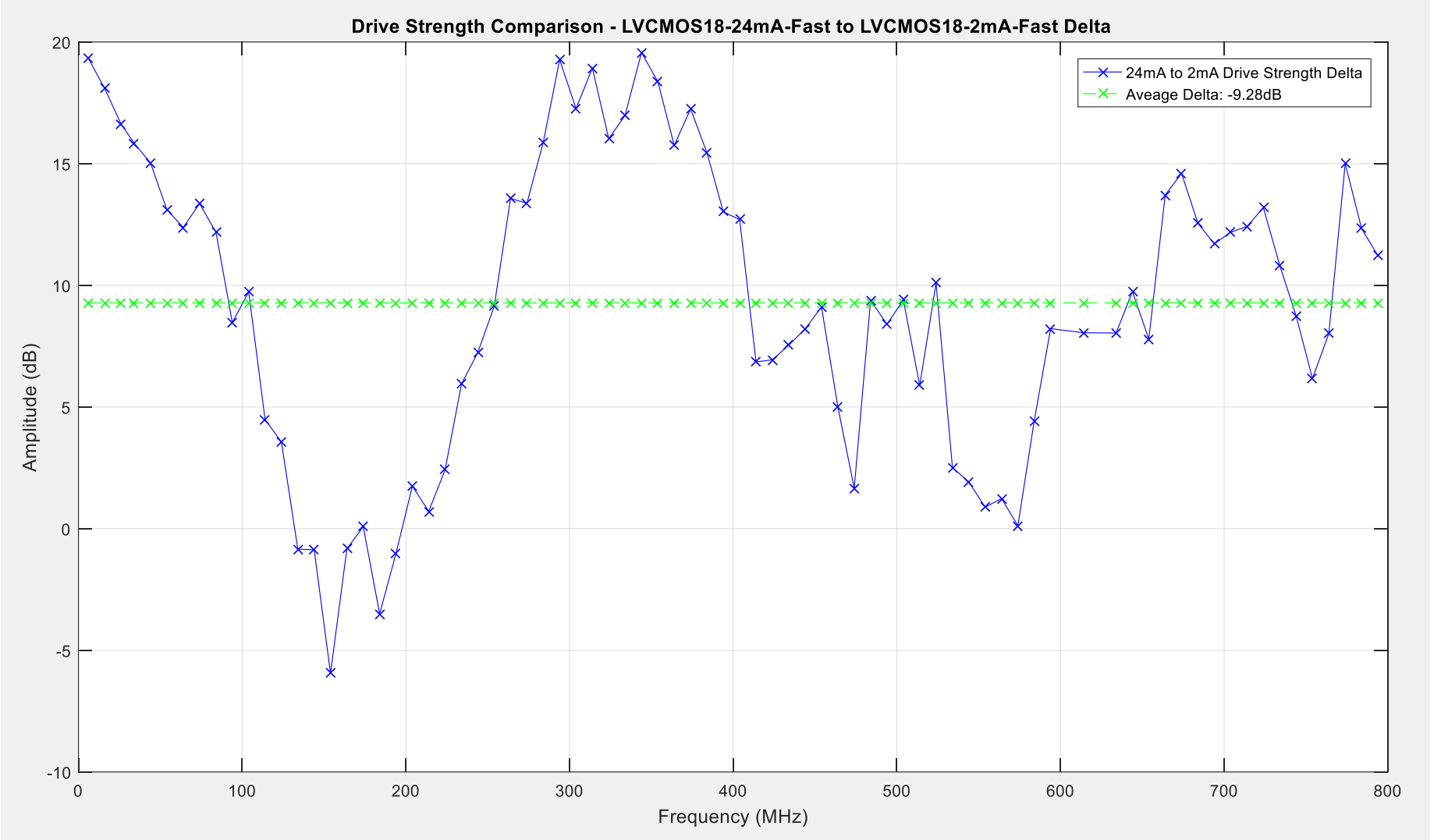


Figure 120: LVCMOS18-24mA-Fast to LVCMOS18-2mA-Fast Drive Strength Comparison

5.4.5 LVCMOS15 Drive Strength Results

The traces illustrated in Figure 121 shows the peak level of emissions recorded for the LVCMOS15 I/O buffer drive strength settings detailed in Table 24 below.

LVCMOS15 Setting	Average Noise Level dBµV	Delta Comparison dB
LVCMOS15-16mA-Fast	-65.7494	0
LVCMOS15-12mA-Fast	-65.9496	1.1727
LVCMOS15-8mA-Fast	-68.0284	2.0817
LVCMOS15-6mA-Fast	-68.9168	3.1346
LVCMOS15-4mA-Fast	-70.2876	5.0136
LVCMOS15-2mA-Fast	-74.4882	8.6740

Table 24: LVCMOS15 Drive Strength Emissions Levels Overview

From these results obtained it gives an indication of how much variation occurs on average across the peak levels but does not give an indication of how this variation is distributed across the emissions spectrum. To achieve a more detailed comparison between the I/O driver settings, closer comparisons have been done to illustrate how the level of emissions varies across the observed spectrum. The 'LVCMOS15-16mA-Fast' I/O driver setting has been used as the baseline for the following 5 comparisons, for reference this trace is illustrated in Figure 122. The LVCMOS15-16mA-Fast drive strength testing has an average level of peak emissions of 65.75dBµV.

5.4.5.1 Delta 25 – LVCMOS15-16mA-Fast to LVCMOS15-12mA-Fast Comparison

Delta 25 examines the variation to peak level emissions between the 'LVCMOS15-16mA-Fast' and the 'LVCMOS15-12mA-Fast' driver settings. Ultimately quantifying the change to emissions between 16mA to 12mA drive strength when using the LVCMOS15 technology using Equation 48.

$$\Delta_{25} = A_{LVCMOS15(16mA)} - A_{LVCMOS15(12mA)}$$

Equation 48: Drive Strength Testing: Delta 25 – LVCMOS15 16mA to 12mA Comparison

Where A_n is the vector that holds the peak level of emissions and Δ_n is the comparison equation.

The maxima of 11.47dB is recorded at approximately 450MHz, this is the highest point where the 16mA setting is greater than the 12mA setting in terms of the peak level of emissions. The minima of –-13.03dB is recorded at approximately 180MHz, with the minima depicting the point where the 12mA setting is higher than the 16mA setting again in terms of the peak level of emissions recorded. The average level of change across the observed spectrum between the 16mA and 12mA drive strength settings is -1.17dB. Figure 123 illustrates the plot for this comparison.

5.4.5.2 Delta 26 – LVCMOS15-16mA-Fast to LVCMOS15-8mA-Fast Comparison

Delta 26 examines the variation to peak level emissions between the 'LVCMOS15-16mA-Fast' and the 'LVCMOS15-8mA-Fast' driver settings. Ultimately quantifying the change to emissions between 16mA to 8mA drive strength when using the LVCMOS15 technology using Equation 49.

$$\Delta_{26} = A_{LVCMOS15(16mA)} - A_{LVCMOS15(8mA)}$$

Equation 49: Drive Strength Testing: Delta 26 – LVCMOS15 16mA to 8mA Comparison

Where A_n is the vector that holds the peak level of emissions and Δ_n is the comparison equation.

The maxima of 9.19dB is recorded at approximately 250MHz, this is the highest point where the 16mA setting is greater than the 8mA setting in terms of the peak level of emissions. The minima of –-16.48dB is recorded at approximately 190MHz, with the minima depicting the point where the 8mA setting is higher than the 16mA setting again in terms of the peak level of emissions recorded. The average level of change across the observed spectrum between the 16mA and 8mA drive strength settings is -2.08dB. Figure 124 illustrates the plot for this comparison.

5.4.5.3 Delta 27 – LVCMOS15-16mA-Fast to LVCMOS15-6mA-Fast Comparison

Delta 27 examines the variation to peak level emissions between the 'LVCMOS15-16mA-Fast' and the 'LVCMOS15-6mA-Fast' driver settings. Ultimately quantifying the change to emissions between 16mA to 6mA drive strength when using the LVCMOS15 technology using Equation 50.

$$\Delta_{27} = A_{LVCMOS15(16mA)} - A_{LVCMOS15(6mA)}$$

Equation 50: Drive Strength Testing: Delta 27 – LVCMOS15 16mA to 6mA Comparison

Where A_n is the vector that holds the peak level of emissions and Δ_n is the comparison equation.

The maxima of 9.31dB is recorded at approximately 380MHz, this is the highest point where the 16mA setting is greater than the 6mA setting in terms of the peak level of emissions. The minima of –-16.8dB is recorded at approximately 190MHz, with the minima depicting the point where the 6mA setting is higher than the 16mA setting again in terms of the peak level of emissions recorded. The average level of change across the observed spectrum between the 16mA and 6mA drive strength settings is -3.13dB. Figure 125 illustrates the plot for this comparison.

5.4.5.4 Delta 28 – LVCMOS15-16mA-Fast to LVCMOS15-4mA-Fast Comparison

Delta 28 examines the variation to peak level emissions between the 'LVCMOS15-16mA-Fast' and the 'LVCMOS15-4mA-Fast' driver settings. Ultimately quantifying the change to emissions between 16mA to 4mA drive strength when using the LVCMOS15 technology using Equation 51.

$$\Delta_{28} = A_{LVCMOS15(16mA)} - A_{LVCMOS15(4mA)}$$

Equation 51: Drive Strength Testing: Delta 28 – LVCMOS15 16mA to 4mA Comparison

Where A_n is the vector that holds the peak level of emissions and Δ_n is the comparison equation.

The maxima of 12.9dB is recorded at approximately 360MHz, this is the highest point where the 16mA setting is greater than the 4mA setting in terms of the peak level of emissions. The minima of –-17.47dB is recorded at approximately 190MHz, with the minima depicting the point where the 4mA setting is higher than the 16mA setting again in terms of the peak level of emissions recorded. The average level of change across the observed spectrum between the 16mA and 4mA drive strength settings is -5.013dB. Figure 126 illustrates the plot for this comparison.

5.4.5.5 Delta 29 – LVCMOS15-16mA-Fast to LVCMOS15-2mA-Fast Comparison

Delta 29 examines the variation to peak level emissions between the 'LVCMOS15-16mA-Fast' and the 'LVCMOS15-2mA-Fast' driver settings. Ultimately quantifying the change to emissions between 16mA to 2mA drive strength when using the LVCMOS15 technology using Equation 52.

$$\Delta_{29} = A_{LVCMOS15(16mA)} - A_{LVCMOS15(2mA)}$$

Equation 52: Drive Strength Testing: Delta 29– LVCMOS15 16mA to 2mA Comparison

Where A_n is the vector that holds the peak level of emissions and Δ_n is the comparison equation.

The maxima of 18.9dB is recorded at approximately 310MHz, this is the highest point where the 16mA setting is greater than the 2mA setting in terms of the peak level of emissions. The minima of –-13.29dB is recorded at approximately 190MHz, with the minima depicting the point where the 2mA setting is higher than the 16mA setting again in terms of the peak level of emissions recorded. The average level of change across the observed spectrum between the 16mA and 2mA drive strength settings is -8.674dB. Figure 127 illustrates the plot for this comparison.

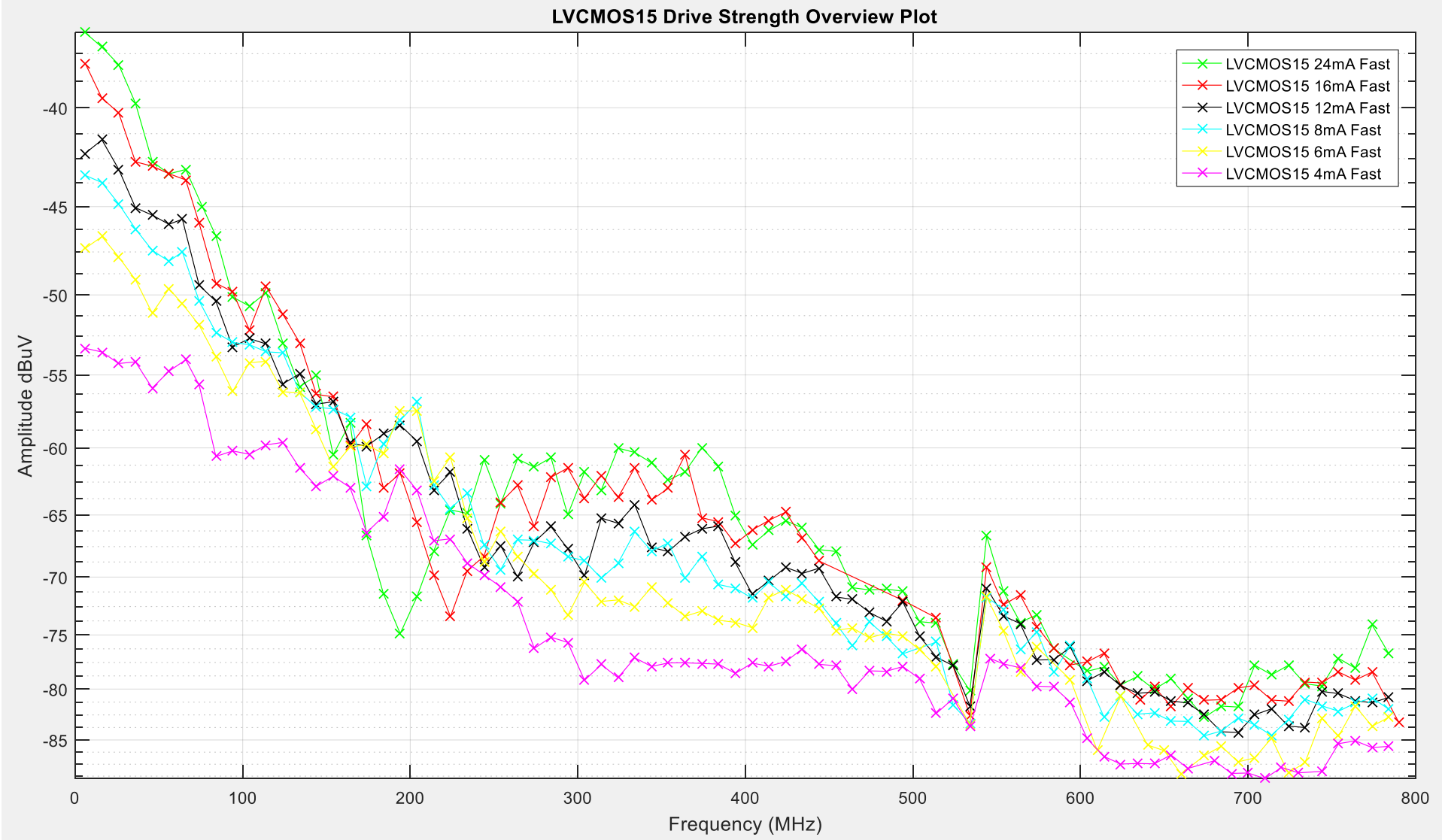


Figure 121: LVCMOS15 Drive Strength Overview Plot

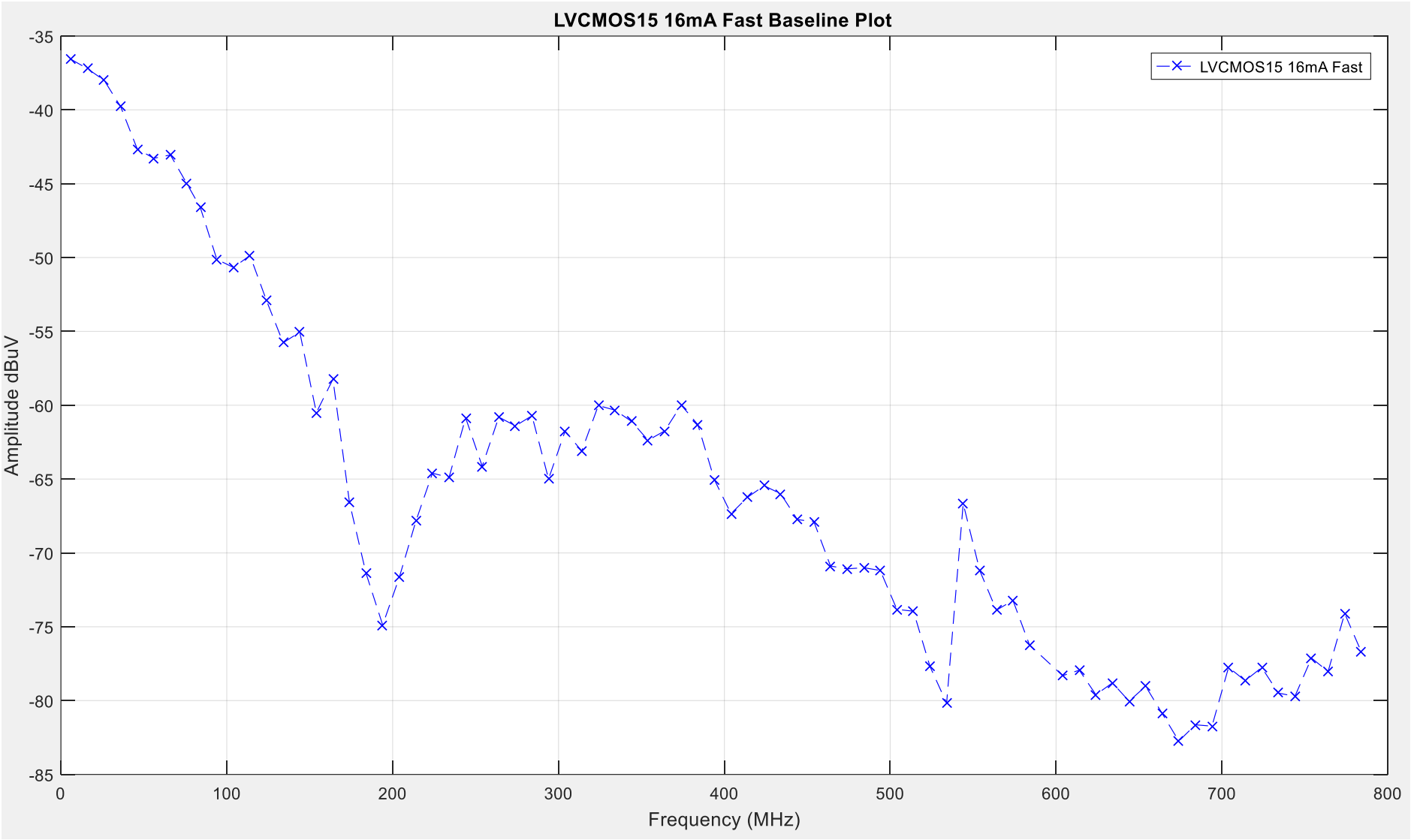


Figure 122: LVCMOS15 Drive Strength Baseline Plot

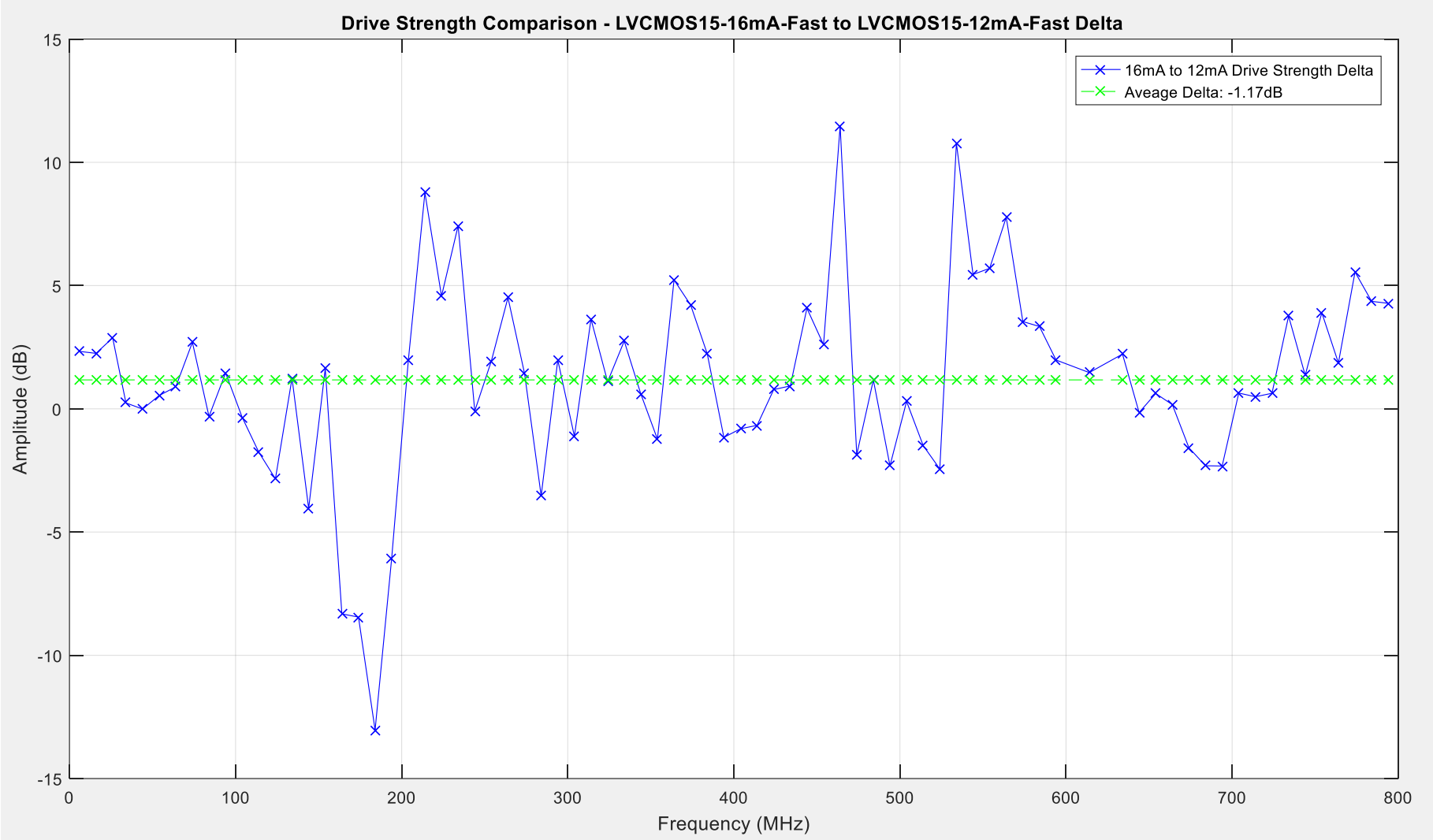


Figure 123: LVCMOS15-16mA-Fast to LVCMOS15-12mA-Fast Drive Strength Comparison

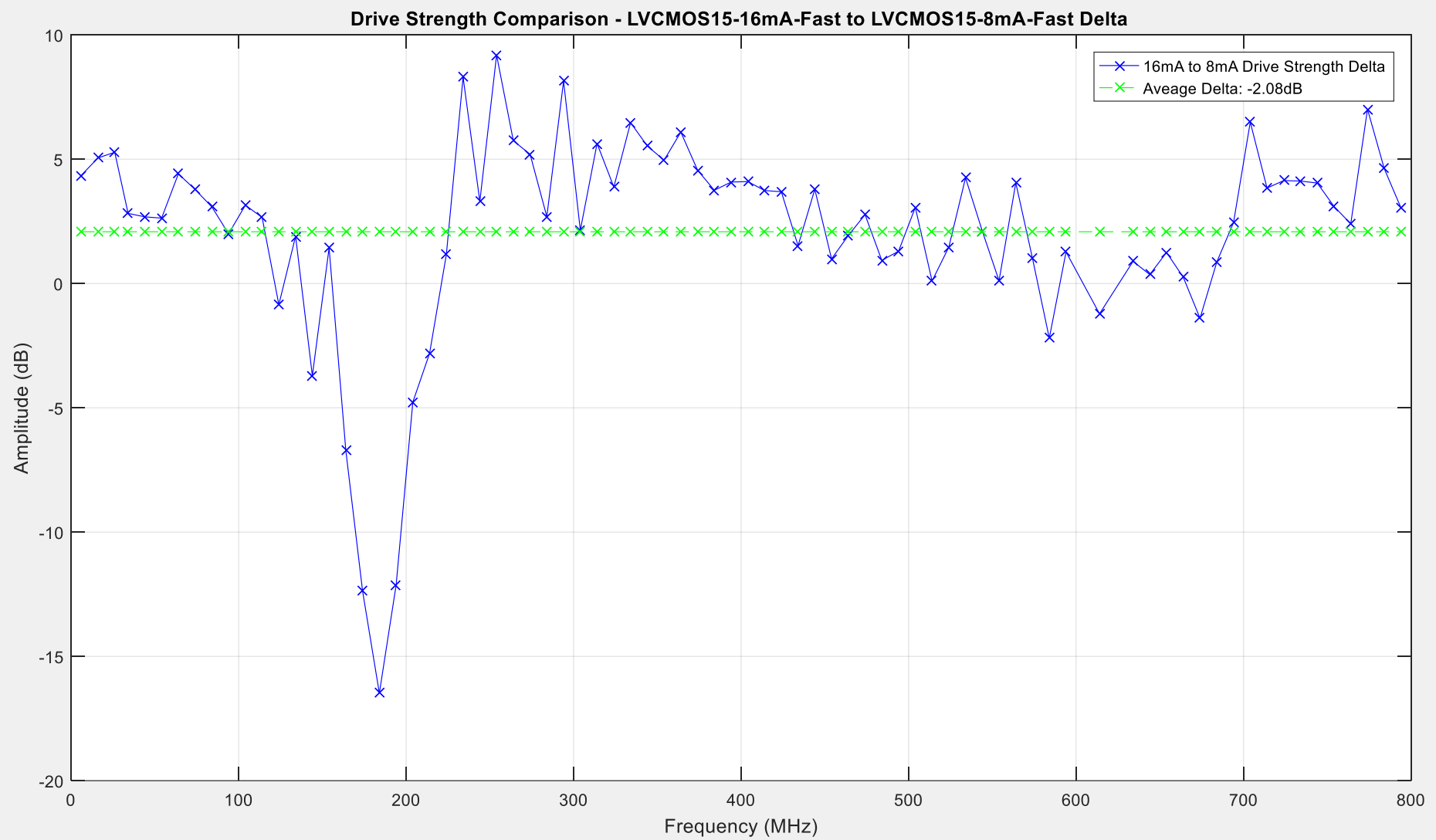


Figure 124: LVCMOS15-16mA-Fast to LVCMOS15-8mA-Fast Drive Strength Comparison

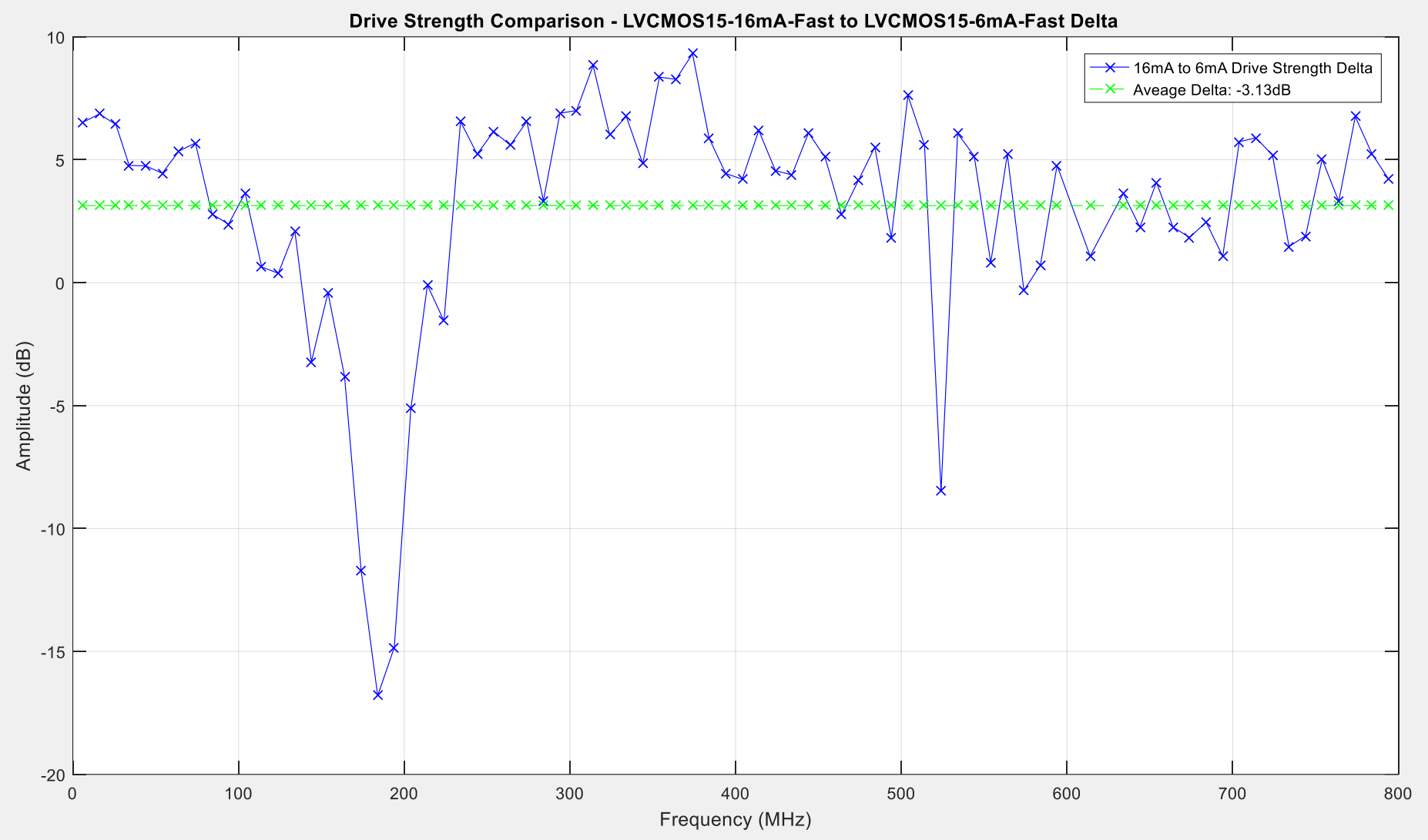


Figure 125: LVCMOS15-16mA-Fast to LVCMOS15-6mA-Fast Drive Strength Comparison

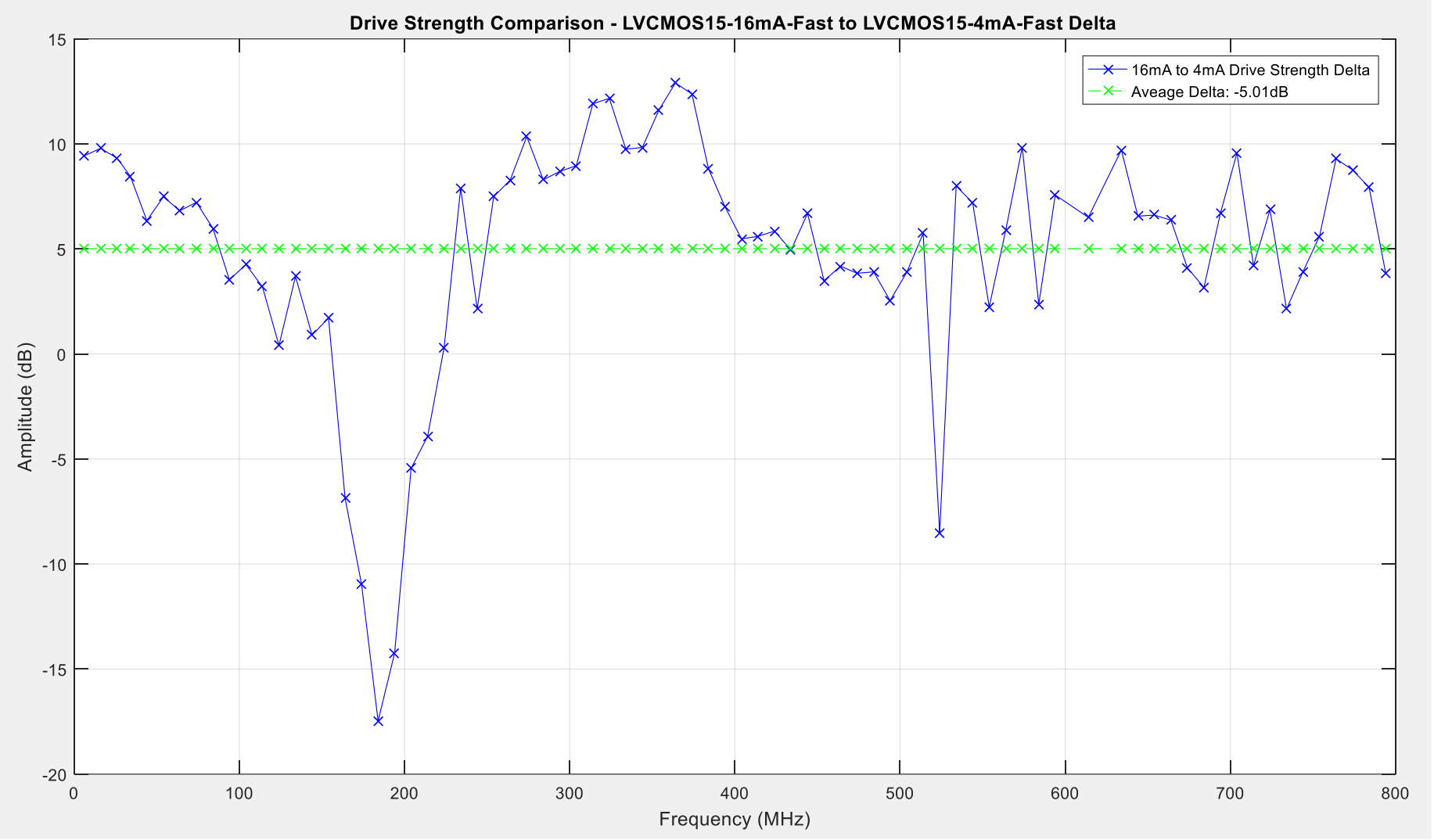


Figure 126: LVCMOS15-16mA-Fast to LVCMOS15-4mA-Fast Drive Strength Comparison

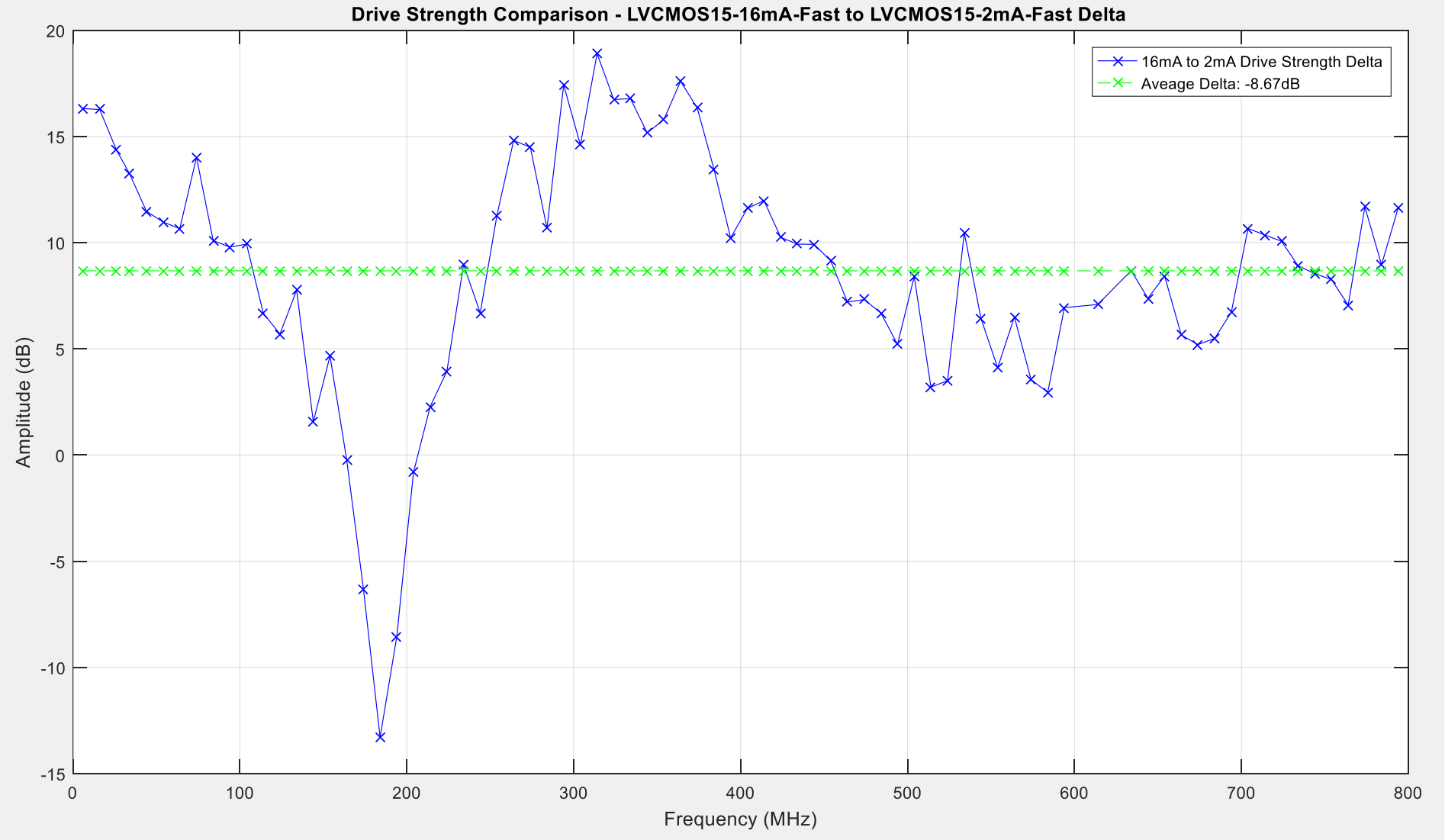


Figure 127: LVCMOS15-16mA-Fast to LVCMOS15-2mA-Fast Drive Strength Comparison

5.4.6 LVCMOS12 Drive Strength Results

The traces illustrated in Figure 128 shows the peak level of emissions recorded for the LVCMOS12 I/O buffer drive strength settings detailed in Table 25 below.

LVCMOS12 Setting	Average Noise Level dBµV	Delta Comparison dB
LVCMOS12-12mA-Fast	-65.3499	0
LVCMOS12-8mA-Fast	-65.3281	0.0528
LVCMOS12-6mA-Fast	-66.1517	0.8994
LVCMOS12-4mA-Fast	-68.27	2.8641
LVCMOS12-2mA-Fast	-72.0559	6.4858

Table 25: LVCMOS12 Drive Strength Emissions Levels Overview

From these results obtained it gives an indication of how much variation occurs on average across the peak levels but does not give an indication of how this variation is distributed across the emissions spectrum. To achieve a more detailed comparison between the I/O driver settings, closer comparisons have been done to illustrate how the level of emissions varies across the observed spectrum. The 'LVCMOS12-12mA-Fast' I/O driver setting has been used as the baseline for the following 4 comparisons, for reference this trace is illustrated in Figure 129. The LVCMOS12-12mA-Fast drive strength testing has an average level of peak emissions of 65.34dBµV.

5.4.6.1 Delta 30 – LVCMOS12-12mA-Fast to LVCMOS12-8mA-Fast Comparison

Delta 30 examines the variation to peak level emissions between the 'LVCMOS12-12mA-Fast' and the 'LVCMOS12-8mA-Fast' driver settings. Ultimately quantifying the change to emissions between 12mA to 8mA drive strength when using the LVCMOS12 technology using Equation 53.

$$\Delta_{30} = A_{LVCMOS12(12mA)} - A_{LVCMOS12(8mA)}$$

Equation 53: Drive Strength Testing: Delta 30– LVCMOS12 12mA to 8mA Comparison

Where A_n is the vector that holds the peak level of emissions and Δ_n is the comparison equation.

The maxima of 4.65dB is recorded at approximately 105MHz, this is the highest point where the 12mA setting is greater than the 8mA setting in terms of the peak level of emissions. The minima of -6.58dB is recorded at approximately 190MHz, with the minima depicting the point where the 8mA setting is higher than the 12mA setting again in terms of the peak level of emissions recorded. The average level of change across the observed spectrum between the 12mA and 8mA drive strength settings is -0.0528dB. Figure 130 illustrates the plot for this comparison.

5.4.6.2 Delta 31 – LVCMOS12-12mA-Fast to LVCMOS12-6mA-Fast Comparison

Delta 31 examines the variation to peak level emissions between the 'LVCMOS12-12mA-Fast' and the 'LVCMOS12-6mA-Fast' driver settings. Ultimately quantifying the change to emissions between 12mA to 6mA drive strength when using the LVCMOS12 technology using Equation 54.

$$\Delta_{31} = A_{LVCMOS12(12mA)} - A_{LVCMOS12(6mA)}$$

Equation 54: Drive Strength Testing: Delta 31– LVCMOS12 12mA to 6mA Comparison

Where A_n is the vector that holds the peak level of emissions and Δ_n is the comparison equation.

The maxima of 6.95dB is recorded at approximately 80MHz, this is the highest point where the 12mA setting is greater than the 6mA setting in terms of the peak level of emissions. The minima of –14.54dB is recorded at approximately 520MHz, with the minima depicting the point where the 6mA setting is higher than the 12mA setting again in terms of the peak level of emissions recorded. The average level of change across the observed spectrum between the 12mA and 6mA drive strength settings is -0.899dB. Figure 131 illustrates the plot for this comparison.

5.4.6.3 Delta 32 – LVCMOS12-12mA-Fast to LVCMOS12-4mA-Fast Comparison

Delta 32 examines the variation to peak level emissions between the 'LVCMOS12-12mA-Fast' and the 'LVCMOS12-4mA-Fast' driver settings. Ultimately quantifying the change to emissions between 12mA to 4mA drive strength when using the LVCMOS12 technology using Equation 55.

$$\Delta_{32} = A_{LVCMOS12(12mA)} - A_{LVCMOS12(4mA)}$$

Equation 55: Drive Strength Testing: Delta 32– LVCMOS12 12mA to 4mA Comparison

Where A_n is the vector that holds the peak level of emissions and Δ_n is the comparison equation.

The maxima of 7.86dB is recorded at approximately 340MHz, this is the highest point where the 12mA setting is greater than the 4mA setting in terms of the peak level of emissions. The minima of –11.55dB is recorded at approximately 520MHz, with the minima depicting the point where the 4mA setting is higher than the 12mA setting again in terms of the peak level of emissions recorded. The average level of change across the observed spectrum between the 12mA and 4mA drive strength settings is -2.8641dB. Figure 132 illustrates the plot for this comparison.

5.4.6.4 Delta 33 – LVCMOS12-12mA-Fast to LVCMOS12-2mA-Fast Comparison

Delta 33 examines the variation to peak level emissions between the 'LVCMOS12-12mA-Fast' and the 'LVCMOS12-2mA-Fast' driver settings. Ultimately quantifying the change to emissions between 12mA to 2mA drive strength when using the LVCMOS12 technology using Equation 56.

$$\Delta_{33} = A_{LVCMOS12(12mA)} - A_{LVCMOS12(2mA)}$$

Equation 56: Drive Strength Testing: Delta 33– LVCMOS12 12mA to 2mA Comparison

Where A_n is the vector that holds the peak level of emissions and Δ_n is the comparison equation.

The maxima of 14.14dB is recorded at approximately 340MHz, this is the highest point where the 12mA setting is greater than the 2mA setting in terms of the peak level of emissions. The minima of –4.55dB is recorded at approximately 520MHz, with the minima depicting the point where the 2mA setting is higher than the 12mA setting again in terms of the peak level of emissions recorded. The average level of change across the observed spectrum between the 12mA and 2mA drive strength settings is -6.485dB. Figure 133 illustrates the plot for this comparison.

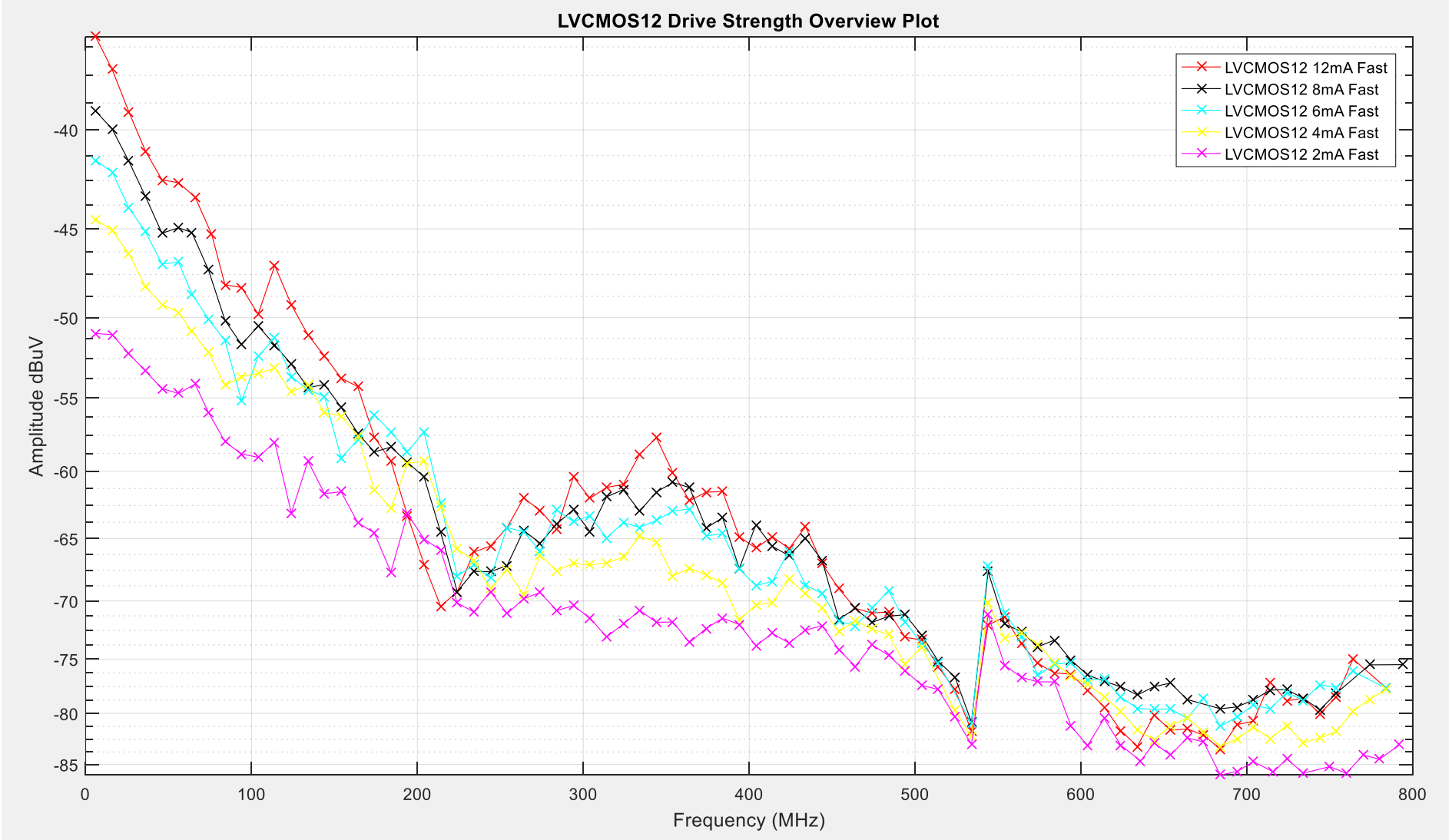


Figure 128: LVCMOS12 Drive Strength Overview Plot

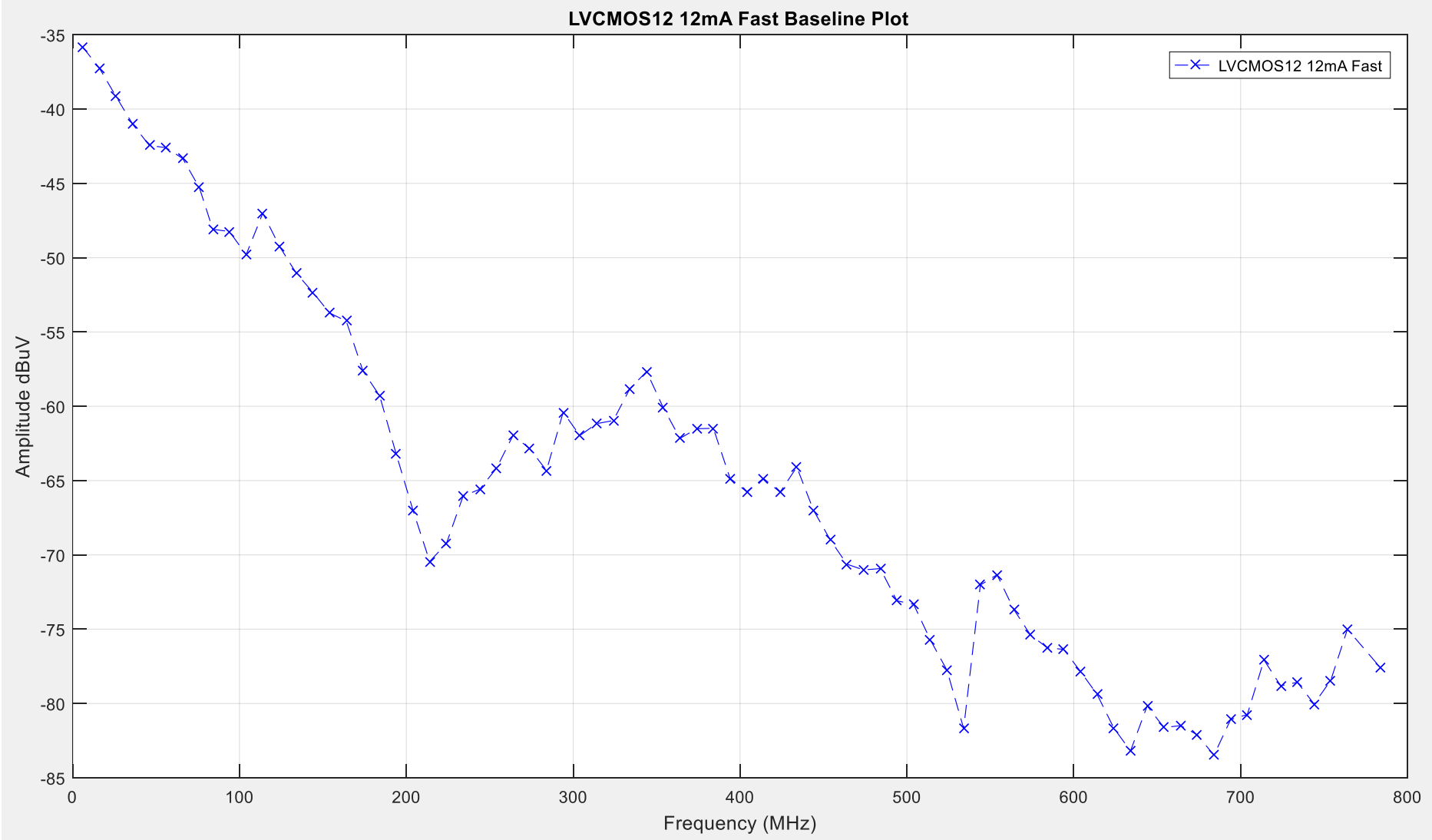


Figure 129: LVCMOS12 Drive Strength Baseline Plot

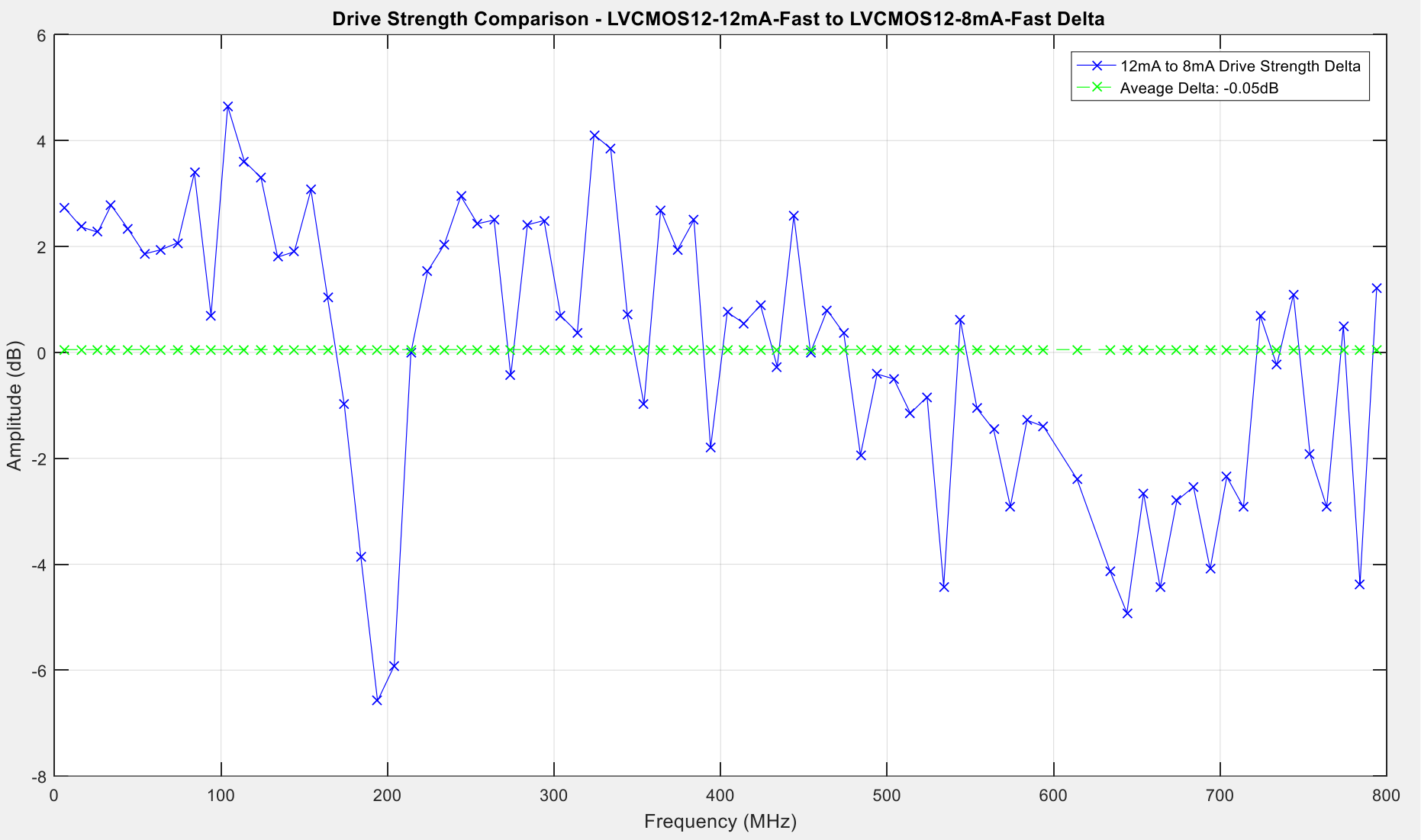


Figure 130: LVCMOS12-12mA-Fast to LVCMOS12-8mA-Fast Drive Strength Comparison

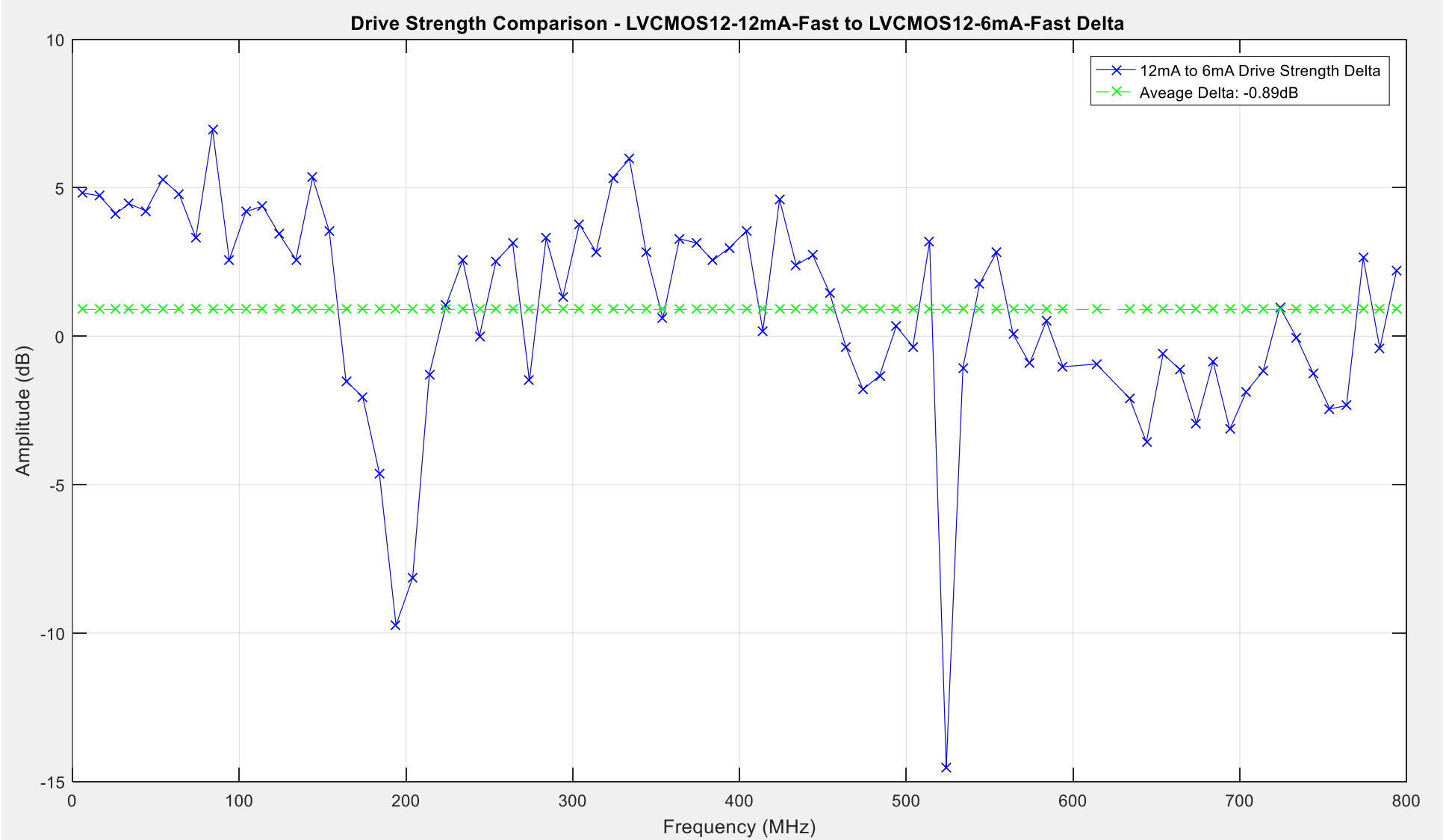


Figure 131: LVCMOS12-12mA-Fast to LVCMOS12-6mA-Fast Drive Strength Comparison

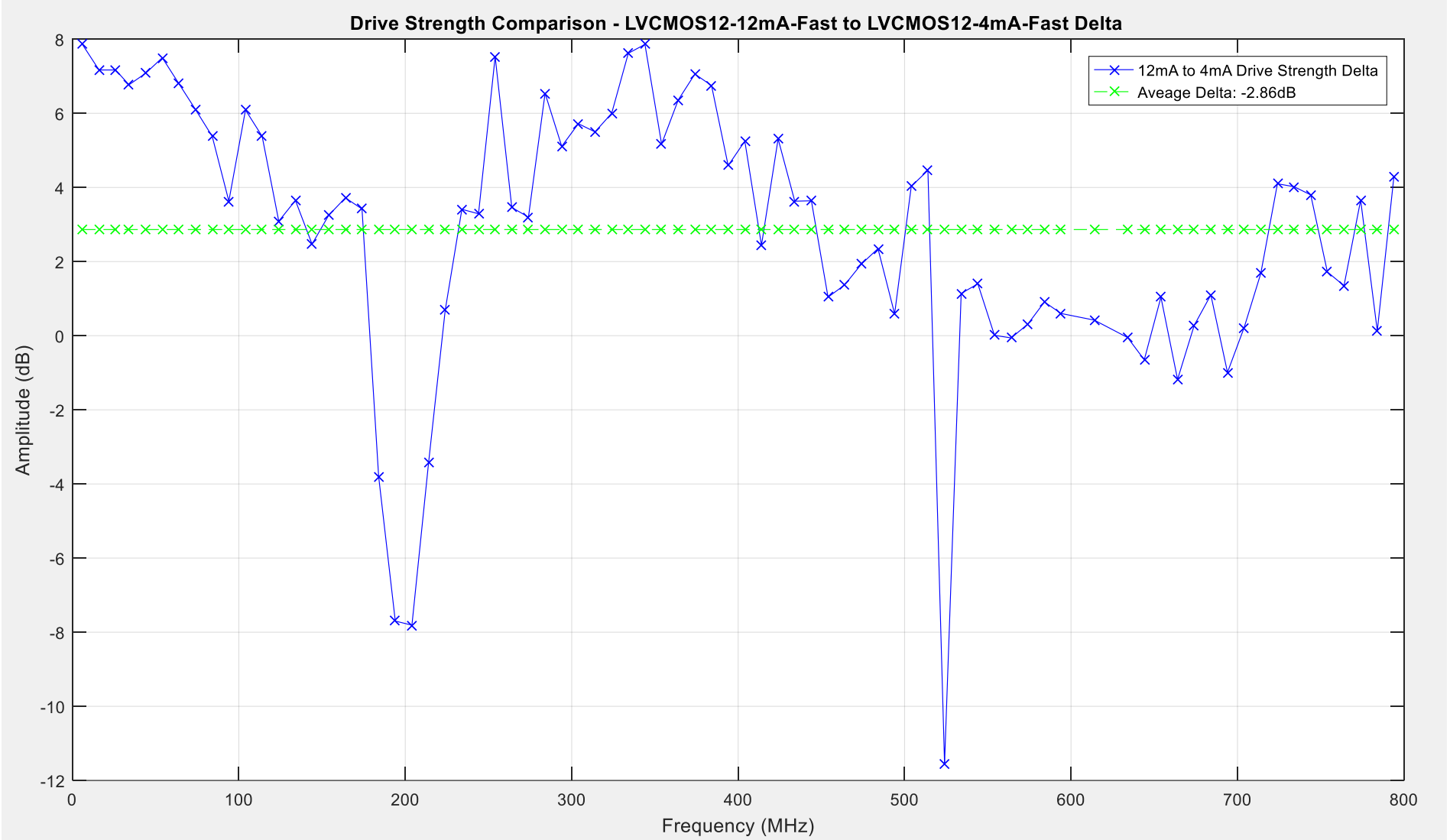


Figure 132: LVCMOS12-12mA-Fast to LVCMOS12-4mA-Fast Drive Strength Comparison

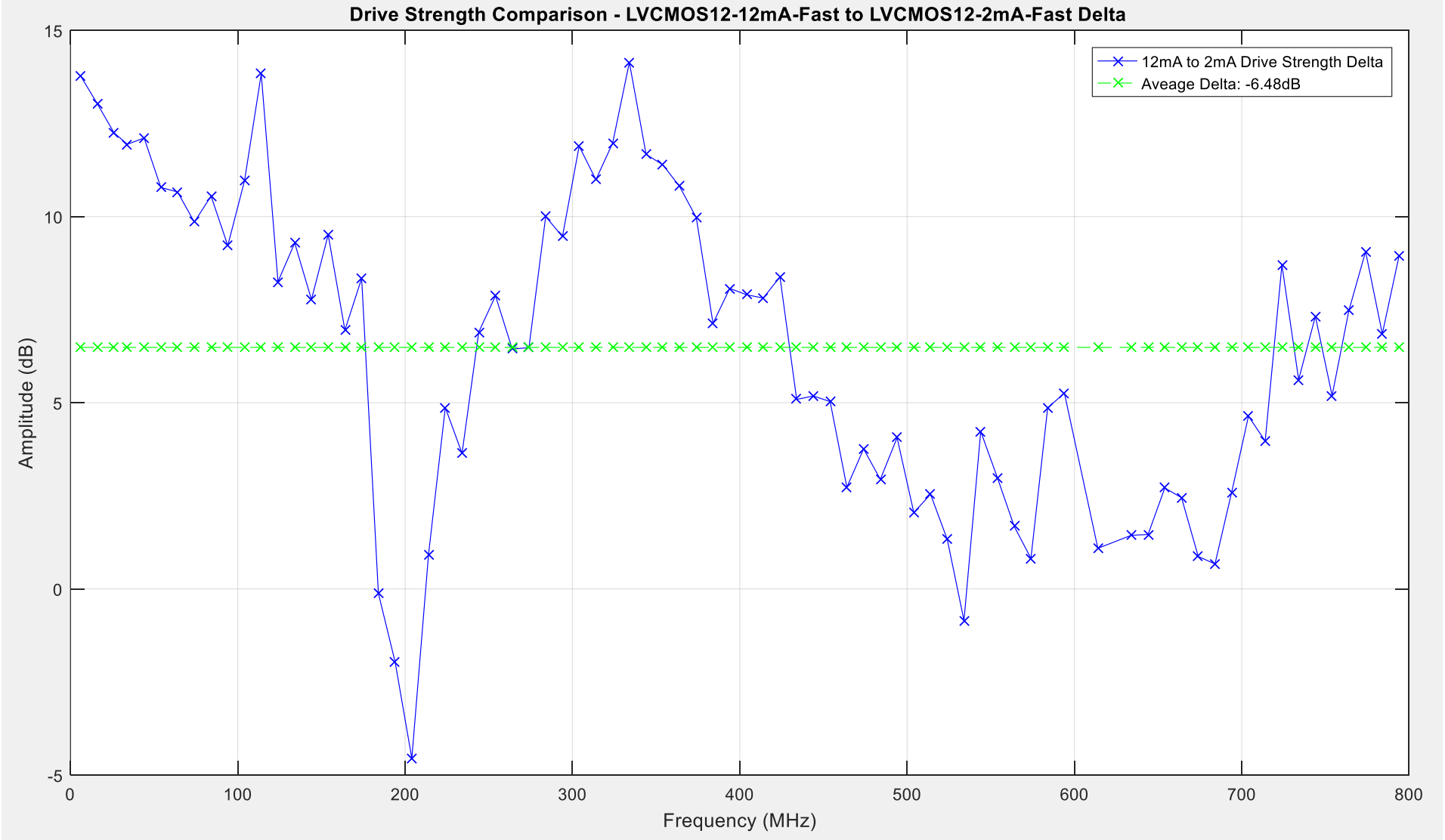


Figure 133: LVCMOS12-12mA-Fast to LVCMOS12-2mA-Fast Drive Strength Comparison

5.4.7 Drive Strength Testing Conclusion

The selection of drive strength settings of an FPGA I/O buffer is chosen based on the load that the particular pin is driving. Selection of this setting is fundamental when meeting the timing requirements of digital circuitry such as an RS-485 communications line or the current required by the load such as a relay or solid state switch. The results have shown that the emissions between the maximum and minimum drive strength settings are certainly significant when designing for EMC compliance. Comparing the full range of drive strength settings has recorded a significant reduction to emissions across all technologies.

The highest average level of change to peak emissions recorded from the LVTTL I/O standard with a reduction of more than 13.19dB from the maximum setting of '24mA' to the minimum setting of '2mA'. The greatest maxima seen from the comparison plots throughout this drive strength testing for the LVTTL logic standard is approximately an increase to the peak level of emissions of +29dB. This is seen when comparing the 'LVTTL-24mA-Fast' to the 'LVTTL-2mA-Fast' in delta 6.

The highest average level of change to peak emissions recorded from the LVCMOS33 I/O standard with a reduction of more than 8.37dB was from the maximum setting of '24mA' to the minimum setting of '2mA'. The greatest maxima seen from the comparison plots throughout this drive strength testing for the LVCMOS33 logic standard is approximately an increase to the peak level of emissions of +21.58dB. This is seen when comparing the 'LVCMOS33-24mA-Fast' to the 'LVCMOS33-2mA-Fast' in delta 12.

The highest average level of change to peak emissions recorded from the LVCMOS25 I/O standard with a reduction of more than 9.16dB was from the maximum setting of '24mA' to the minimum setting of '2mA'. The greatest maxima seen from the comparison plots throughout this drive strength testing for the LVCMOS25 logic standard is approximately an increase to the peak level of emissions of +23.2dB. This is seen when comparing the 'LVCMOS25-24mA-Fast' to the 'LVCMOS25-2mA-Fast' in delta 18.

The highest average level of change to peak emissions recorded from the LVCMOS18 I/O standard with a reduction of more than 9.28dB was from the maximum setting of '24mA' to the minimum setting of '2mA'. The greatest maxima seen from the comparison plots throughout this drive strength testing for the LVCMOS18 logic standard is approximately an increase to the peak level of emissions of +19.57dB. This is seen when comparing the 'LVCMOS18-24mA-Fast' to the 'LVCMOS18-2mA-Fast' in delta 24.

The highest average level of change to peak emissions was recorded from the LVCMOS15 I/O standard with a reduction of more than 8.67dB was from the maximum setting of '16mA' to the minimum setting of '2mA'. The greatest maxima seen from the comparison plots throughout this drive strength testing for the LVCMOS15 logic standard is approximately an increase to the peak level of emissions of +18.9dB. This is seen when comparing the 'LVCMOS15-16mA-Fast' to the 'LVCMOS15-2mA-Fast' in delta 29.

The highest average level of change to peak emissions recorded from the LVCMOS12 I/O standard with a reduction of more than 6.48dB was from the maximum setting of '12mA' to the minimum setting of '2mA'. The greatest maxima seen from the comparison plots throughout this drive strength testing for the LVCMOS12 logic standard is approximately an increase to the peak level of emissions of +14.14dB. This is seen when comparing the 'LVCMOS12-16mA-Fast' to the 'LVCMOS12-2mA-Fast' in delta 33.

As can be seen from the drive strength testing overview above, the significance of utilising the required drive strength and not implementing an efficient design can reduce peak emissions by as much as almost 30dB at particular a particular frequency. In terms of the average level of peak emissions, this is dependent upon the logic standard chosen. It can be concluded that the I/O driver settings that possess a 24mA drive strength and Fast edge rate will always produce the higher average of peak emissions. As the voltage level of the LVCMOS standard reduces so does the delta of peak level emissions. From this it can be concluded that when selecting the drive strength for the I/O buffers it is equally dependent upon the logic standard the design is built around. Careful consideration should be given to the selection of drive strength within any design to ensure that the product has the best chance for EMC compliance.

5.5 Edge Rate Comparison

The edge rate comparison for the radiated emissions testing is intended to assess how the edge rate setting of 'Fast' or 'Slow' affects the level of EMI produced. The edge rate has been varied between its two states across all of the I/O Standards and with the drive strength at the maximum and the minimum of their respective capabilities. The LVTTL, LVCMOS33 LVCMOS25 and LVCMOS18 have a maximum drive strength capability of 24mA and a minimum setting of 2mA. The LVCMOS15 has a maximum drive strength setting capability of 16mA and a minimum setting of 2mA and the LVCMOS12 has a maximum driver strength setting of 12mA and a minimum setting of 2mA.

5.5.1 Edge Rate Testing Overview & Results

To obtain a quantifiable level of emissions produced from the edge rate testing results, the delta between the chosen traces has been calculated and an average of the change to the level of emissions has been taken. This will allow a designer to understand a rough order of magnitude to the changes between the 'Fast' and 'Slow' edge rate settings.

5.5.2 LVTTL Edge Rate Results

The traces illustrated in Figure 134 show the peak level of emissions recorded for the LVTTL I/O buffer edge rate settings detailed in Table 26 below.

Driver Setting	LVTTL Average of Peak Harmonic Level dB	Delta dB
LVTTL-24mA-Fast	-59.9919	-0.44
LVTTL-24mA-Slow	-60.4249	
LVTTL-2mA-Fast	-72.6039	-1.05
LVTTL-2mA-Slow	-73.8976	

Table 26: LVTTL Edge Rate Emissions Results

From these results obtained it gives an indication of how much variation occurs on average across the peak levels, but does not give an indication of how this variation is distributed across the emissions spectrum. To achieve a more detailed comparison between the edge rate settings, closer comparisons have been done to illustrate how the level of emissions varies across the observed spectrum. Two comparisons have taken place at opposite ends of the respective drive strength capabilities to illustrate how the edge rate can influence the peak level of emissions produced. The 'LVTTL-24mA-Fast' I/O driver setting has been used as the baseline for the first comparison against the 'LVTTL-24mA-Slow', for reference this trace is illustrated in Figure 135. The 'LVTTL-2mA-Fast' I/O driver setting has been used as the baseline for the second comparison against the 'LVTTL-2mA-Slow', for reference this trace is illustrated in Figure 136.

5.5.2.1 Delta 1 – LVTTL-24mA-Fast to LVTTL-24mA-Slow Comparison

Delta 1 examines the variation to peak level emissions between the 'LVTTL-24mA-Fast' and the 'LVTTL-24mA-Slow' driver settings. Ultimately quantifying the change to peak level emissions between the 'Fast' and 'Slow' edge rate settings when using the LVTTL technology using Equation 57.

$$\Delta_1 = A_{LVTTL-24mA-Fast} - A_{LVTTL-24mA-Slow}$$

Equation 57: Edge Rate Testing: Delta 1 – LVTTL-24mA-Fast to LVTTL-24mA-Slow Comparison

Where A_n is the vector that holds the peak level of emissions and Δ_n is the comparison equation.

The maxima of +8.14dB is recorded at approximately 640MHz, this is the highest point where the 'Fast' setting is greater than the 'Slow' setting in terms of the peak level of emissions. The minima of -5.64dB is recorded at approximately 205MHz, with the minima depicting the point where the 'Slow' setting is higher than the 'Fast' setting again in terms of the peak level of emissions recorded. The average level of change across the observed spectrum between the 'Fast' and 'Slow' edge rate settings is -0.444dB. Figure 137 illustrates the plot for this comparison.

5.5.2.2 Delta 2 – LVTTL-2mA-Fast to LVTTL-2mA-Slow Comparison

Delta 2 examines the variation to peak level emissions between the 'LVTTL-2mA-Fast' and the 'LVTTL-2mA-Slow' driver settings. Ultimately quantifying the change to peak level emissions between the 'Fast' and 'Slow' edge rate settings when using the LVTTL technology using Equation 58.

$$\Delta_2 = A_{LVTTL-2mA-Fast} - A_{LVTTL-2mA-Slow}$$

Equation 58: Edge Rate Testing: Delta 2 – LVTTL-2mA-Fast to LVTTL-2mA-Slow Comparison

Where A_n is the vector that holds the peak level of emissions and Δ_n is the comparison equation.

The maxima of +6.6dB is recorded at approximately 720MHz, this is the highest point where the 'Fast' setting is greater than the 'Slow' setting in terms of the peak level of emissions. The minima of -8.8dB is recorded at approximately 740MHz, with the minima depicting the point where the 'Slow' setting is higher than the 'Fast' setting again in terms of the peak level of emissions recorded. The average level of change across the observed spectrum between the 'Fast' and 'Slow' edge rate settings is 1.055dB. Figure 138 illustrates the plot for this comparison.

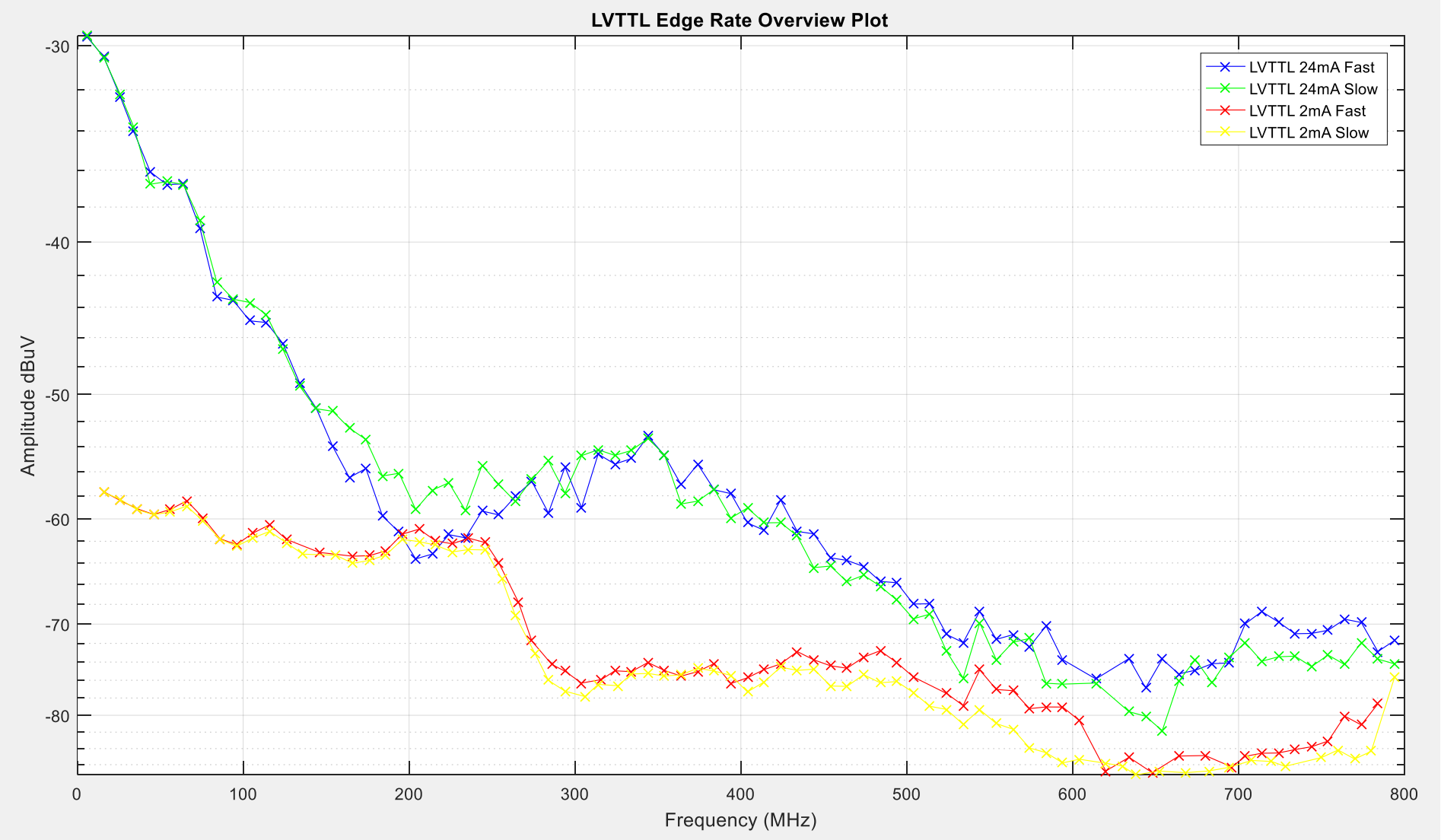


Figure 134: LVTTL Edge Rate Comparison Overview

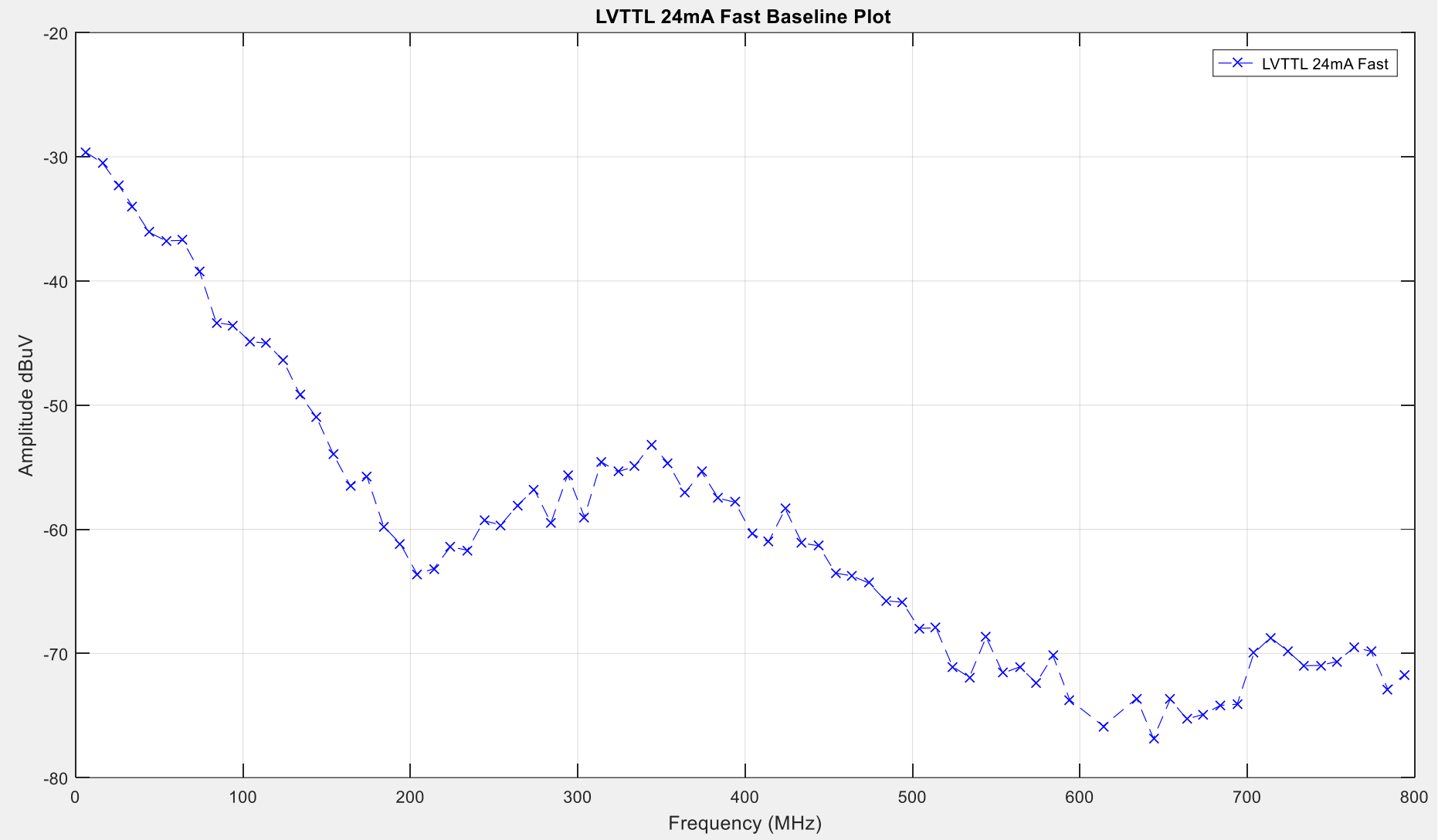


Figure 135: LVTTL-24mA-Fast Baseline Plot

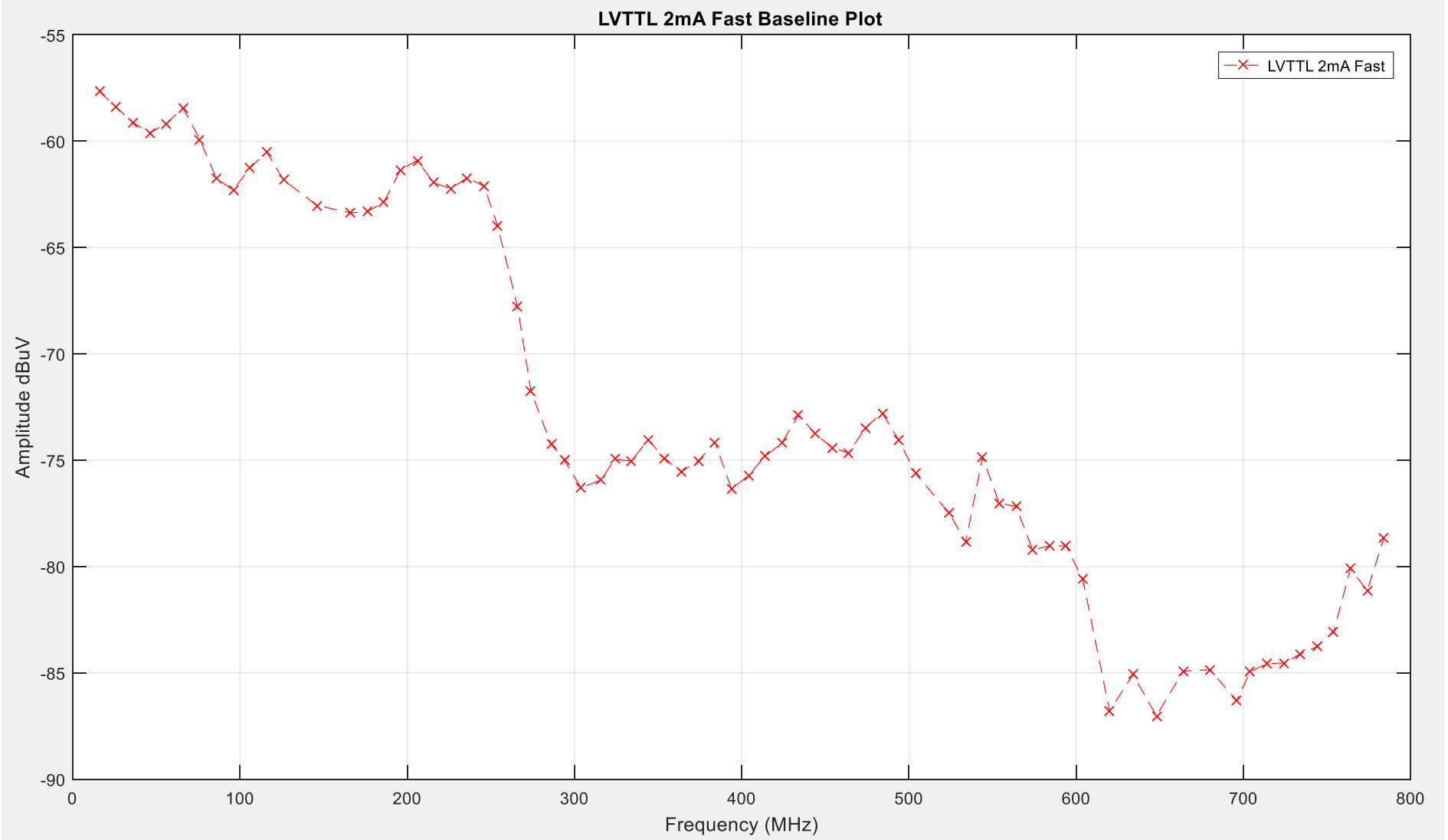


Figure 136: LVTTL-2mA-Fast Baseline Plot

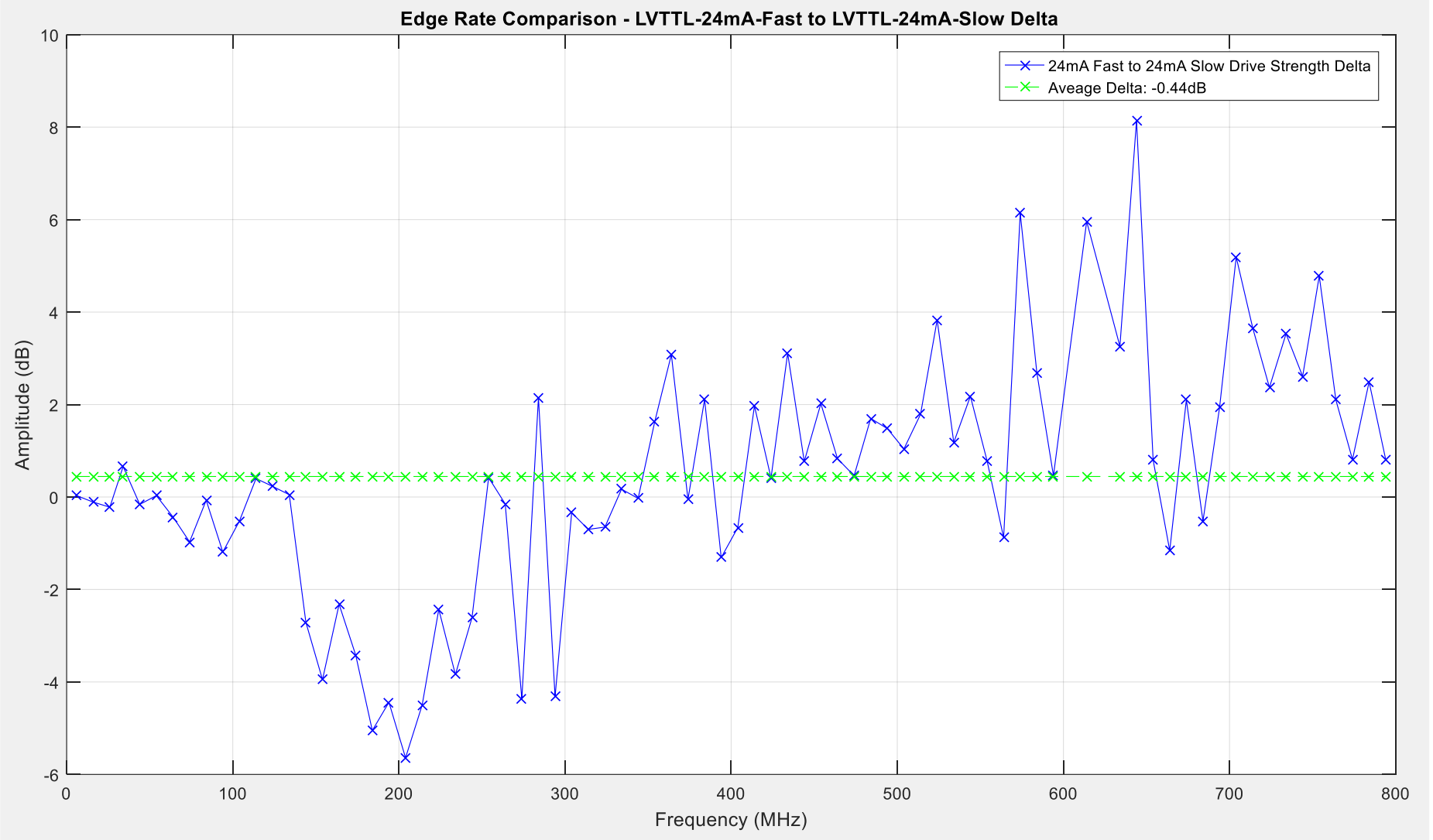


Figure 137: LVTTL-24mA-Fast to LVTTL-24mA-Slow Edge Rate Comparison

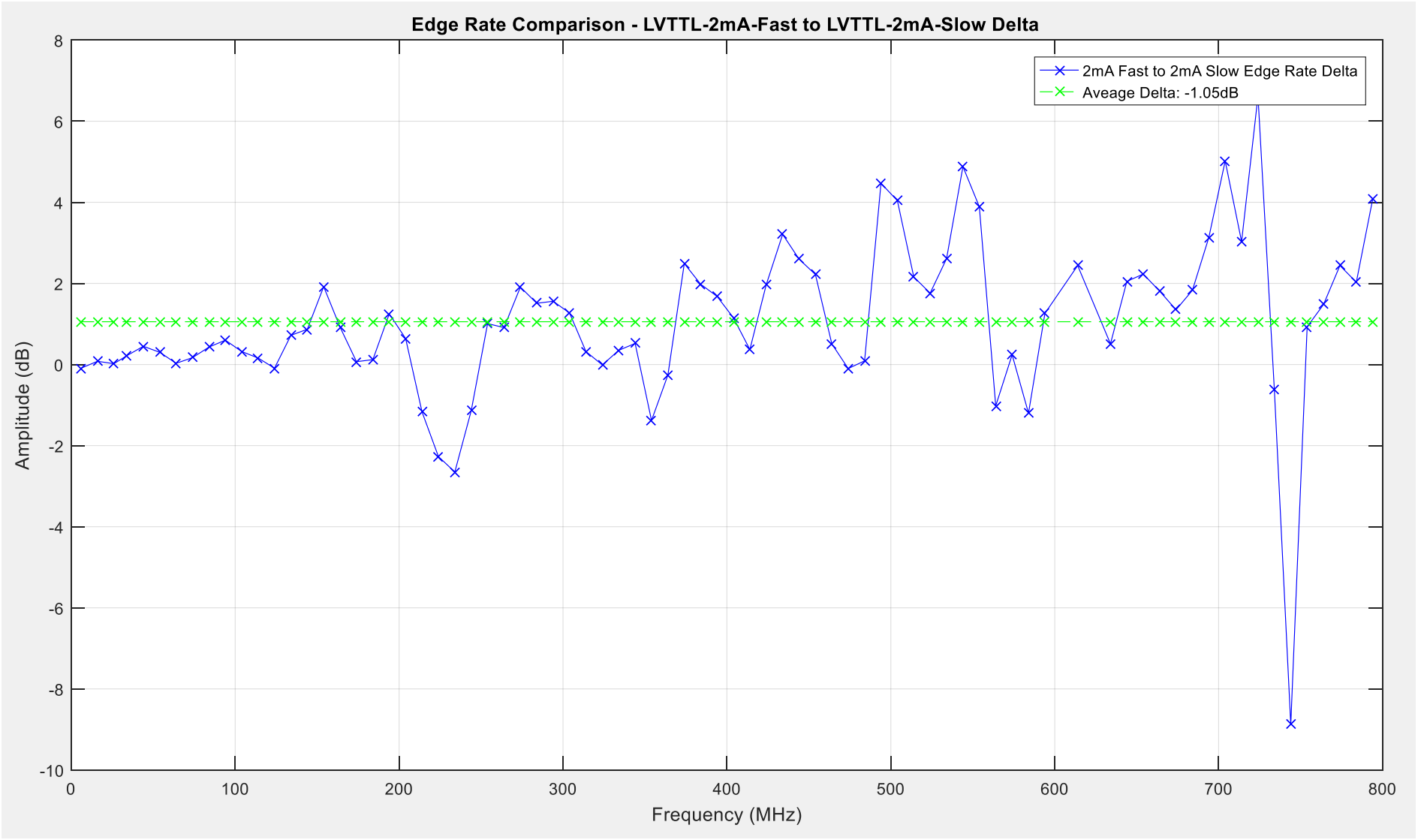


Figure 138: LVTTL-2mA-Fast to LVTTL-2mA-Slow Edge Rate Comparison

5.5.3 LVCMOS33 Edge Rate Results

The traces illustrated in Figure 139 show the peak level of emissions recorded for the LVCMOS33 I/O buffer edge rate settings detailed in Table 27 below.

Driver Setting	LVCMOS33 Average of Peak Harmonic Level dBµV	Delta dB
LVCMOS33-24mA-Fast	-63.7553	-0.5023
LVCMOS33-24mA-Slow	-64.8541	
LVCMOS33-2mA-Fast	-72.1851	-0.845
LVCMOS33-2mA-Slow	-73.3359	

Table 27: LVCMOS33 Edge Rate Emissions Results

From these results obtained it gives an indication of how much variation occurs on average across the peak levels, but does not give an indication of how this variation is distributed across the emissions spectrum. To achieve a more detailed comparison between the edge rate settings, closer comparisons have been done to illustrate how the level of emissions varies across the observed spectrum. Two comparisons have taken place at opposite ends of the respective drive strength capabilities to illustrate how the edge rate can influence the peak level of emissions produced. The 'LVCMOS33-24mA-Fast' I/O driver setting has been used as the baseline for the first comparison against the 'LVCMOS33-24mA-Slow', for reference this trace is illustrated in Figure 140. The 'LVCMOS33-2mA-Fast' I/O driver setting has been used as the baseline for the second comparison against the 'LVCMOS33-2mA-Slow', for reference this trace is illustrated in Figure 141.

5.5.3.1 Delta 3 – LVCMOS33-24mA-Fast to LVCMOS33-24mA-Slow Comparison

Delta 3 examines the variation to peak level emissions between the 'LVCMOS33-24mA-Fast' and the 'LVCMOS33-24mA-Slow' driver settings. Ultimately quantifying the change to peak level emissions between the 'Fast' and 'Slow' edge rate settings when using the LVCMOS33 technology using Equation 59.

$$\Delta_3 = A_{LVCMOS33-24mA-Fast} - A_{LVCMOS33-24mA-Slow}$$

Equation 59: Edge Rate Testing: Delta 3 – LVCMOS33-24mA-Fast to LVCMOS33-24mA-Slow Comparison

Where A_n is the vector that holds the peak level of emissions and Δ_n is the comparison equation.

The maxima of +13.51dB is recorded at approximately 560MHz, this is the highest point where the 'Fast' setting is greater than the 'Slow' setting in terms of the peak level of emissions. The minima of -6.6dB is recorded at approximately 170MHz, with the minima depicting the point where the 'Slow' setting is higher than the 'Fast' setting again in terms of the peak level of emissions recorded. The average level of change across the observed spectrum between the 'Fast' and 'Slow' edge rate settings is -0.5023dB. Figure 142 illustrates the plot for this comparison.

5.5.3.2 Delta 4 – LVCMOS33-2mA-Fast to LVCMOS33-2mA-Slow Comparison

Delta 4 examines the variation to peak level emissions between the 'LVCMOS33-2mA-Fast' and the 'LVCMOS33-2mA-Slow' driver settings. Ultimately quantifying the change to peak level emissions between the 'Fast' and 'Slow' edge rate settings when using the LVCMOS33 technology using Equation 60.

$$\Delta_4 = A_{LVCMOS33-2mA-Fast} - A_{LVCMOS33-2mA-Slow}$$

Equation 60: Edge Rate Testing: Delta 4 – LVCMOS33-2mA-Fast to LVCMOS33-2mA-Slow Comparison

Where A_n is the vector that holds the peak level of emissions and Δ_n is the comparison equation.

The maxima of +6.9dB is recorded at approximately 790MHz, this is the highest point where the 'Fast' setting is greater than the 'Slow' setting in terms of the peak level of emissions. The minima of -3.42dB is recorded at approximately 290MHz, with the minima depicting the point where the 'Slow' setting is higher than the 'Fast' setting again in terms of the peak level of emissions recorded. The average level of change across the observed spectrum between the 'Fast' and 'Slow' edge rate settings is 0.845dB. Figure 143 illustrates the plot for this comparison.

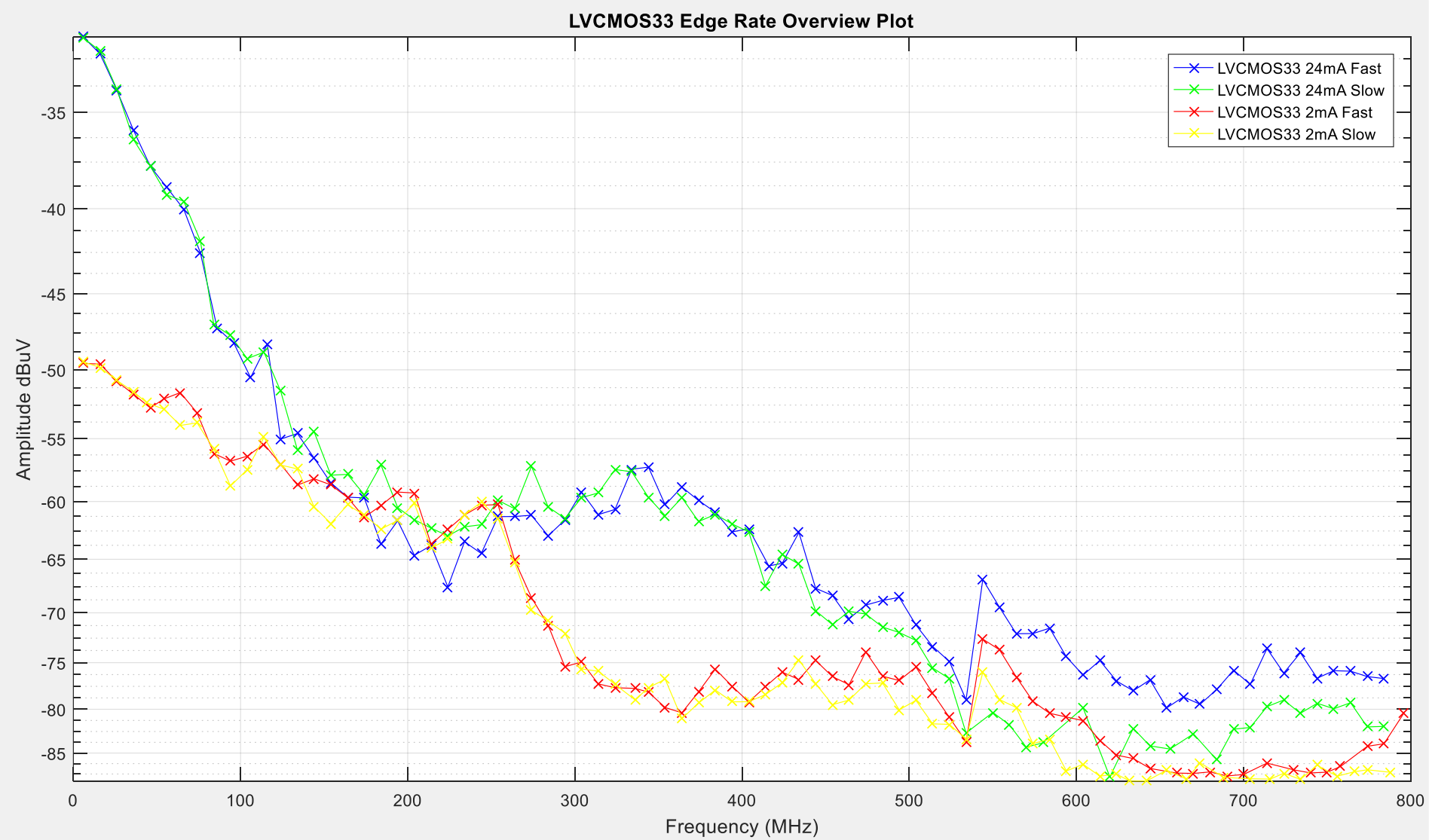


Figure 139: LVCMOS33 Edge Rate Comparison Overview

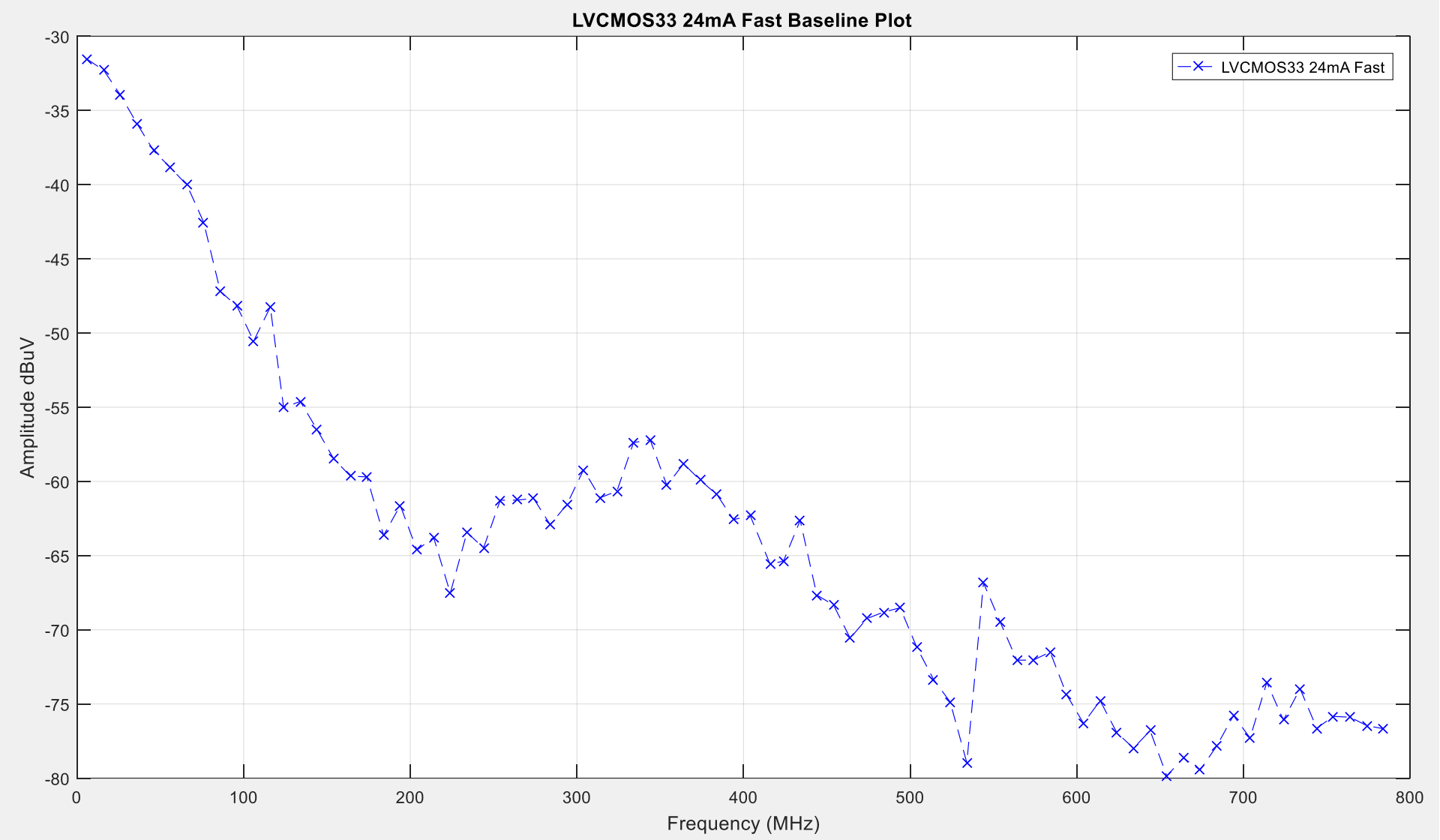


Figure 140: LVCMOS33 Edge Rate 24mA Baseline Plot

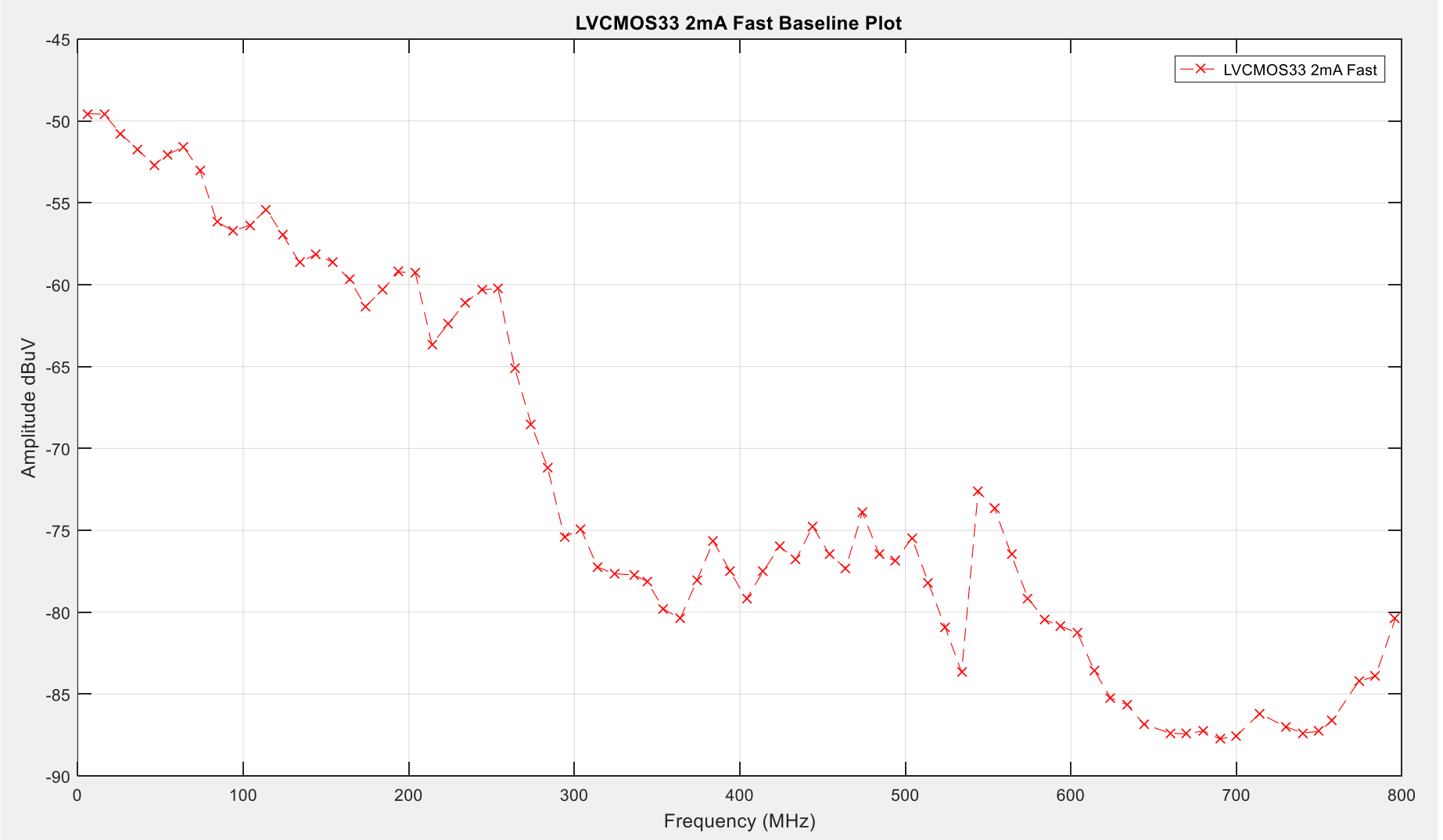


Figure 141: LVCMOS33 Edge Rate 24mA Baseline Plot

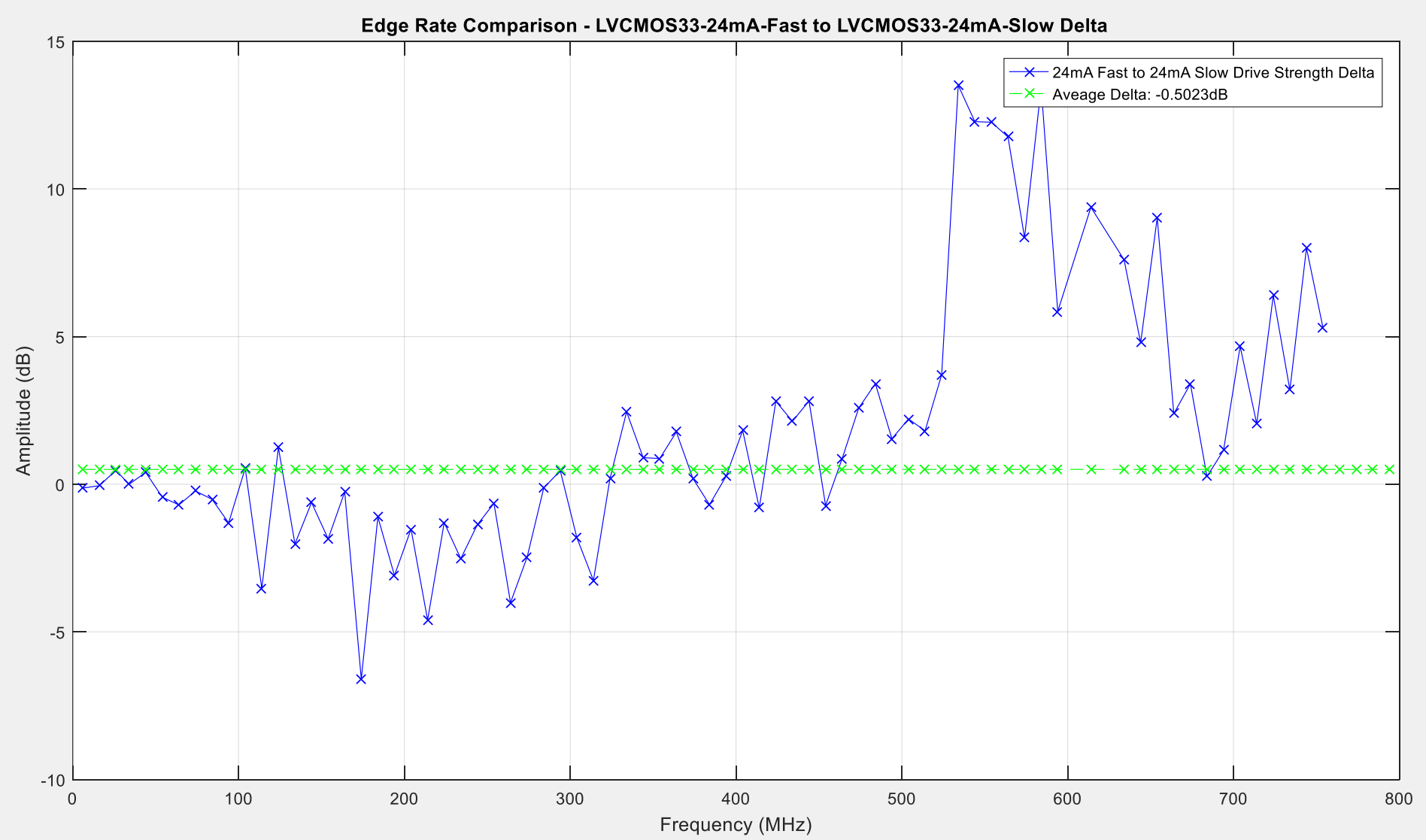


Figure 142: LVCMOS33-24mA-Fast to LVCCMOS33-24mA-Slow Edge Rate Comparison

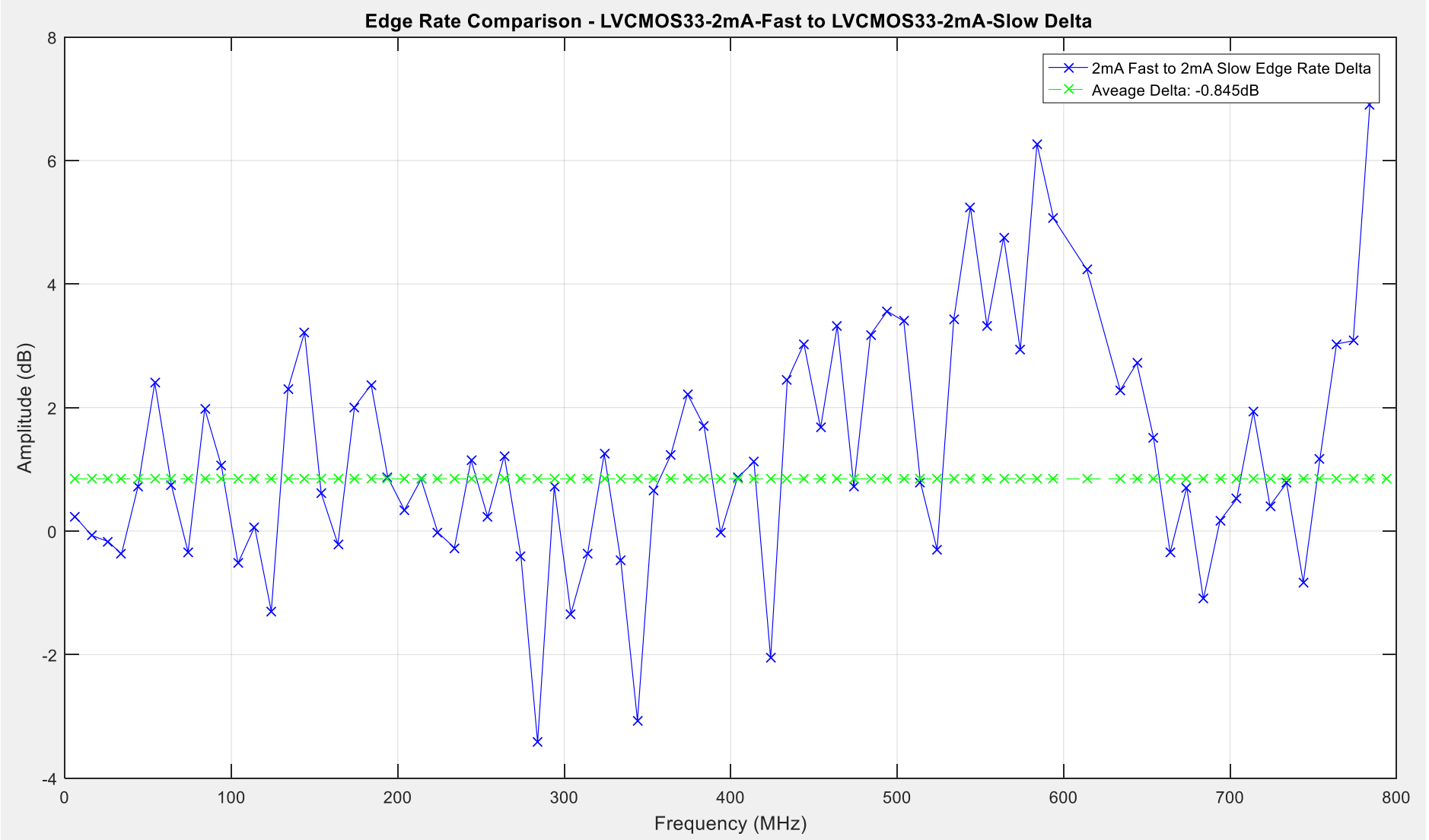


Figure 143: LVCMOS33-2mA-Fast to LVCCMOS33-2mA-Slow Edge Rate Comparison

5.5.4 LVCMOS25 Edge Rate Results

The traces illustrated in Figure 144 show the peak level of emissions recorded for the LVCMOS25 I/O buffer edge rate settings detailed in Table 28 below.

Driver Setting	LVCMOS25 Average of Peak Harmonic Level dBµV	Delta dB
LVCMOS25-24mA-Fast	-63.4778	1.2004
LVCMOS25-24mA-Slow	-64.6782	
LVCMOS25-4mA-Slow	-70.7144	
LVCMOS25-2mA-Fast	-72.0572	0.6107
LVCMOS25-2mA-Slow	-72.6679	

Table 28: LVCMOS25 Edge Rate Emissions Results

From these results obtained it gives an indication of how much variation occurs on average across the peak levels, but does not give an indication of how this variation is distributed across the emissions spectrum. To achieve a more detailed comparison between the edge rate settings, closer comparisons have been done to illustrate how the level of emissions varies across the observed spectrum. Two comparisons have taken place at opposite ends of the respective drive strength capabilities to illustrate how the edge rate can influence the peak level of emissions produced. The 'LVCMOS25-24mA-Fast' I/O driver setting has been used as the baseline for the first comparison against the 'LVCMOS25-24mA-Slow', for reference this trace is illustrated in Figure 145. The 'LVCMOS25-2mA-Fast' I/O driver setting has been used as the baseline for the second comparison against the 'LVCMOS25-2mA-Slow', for reference this trace is illustrated in Figure 146.

5.5.4.1 Delta 5 – LVCMOS25-24mA-Fast to LVCMOS25-24mA-Slow Comparison

Delta 5 examines the variation to peak level emissions between the 'LVCMOS25-24mA-Fast' and the 'LVCMOS25-24mA-Slow' driver settings. Ultimately quantifying the change to peak level emissions between the 'Fast' and 'Slow' edge rate settings when using the LVCMOS25 technology using Equation 61.

$$\Delta_5 = A_{LVCMOS25-24mA-Fast} - A_{LVCMOS25-24mA-Slow}$$

Equation 61: Edge Rate Testing: Delta 5 – LVCMOS25-24mA-Fast to LVCMOS25-24mA-Slow Comparison

Where A_n is the vector that holds the peak level of emissions and Δ_n is the comparison equation.

The maxima of +7.7dB is recorded at approximately 110MHz, this is the highest point where the 'Fast' setting is greater than the 'Slow' setting in terms of the peak level of emissions. The minima of -10.91dB is recorded at approximately 520MHz, with the minima depicting the point where the 'Slow' setting is higher than the 'Fast' setting again in terms of the peak level of emissions recorded. The average level of change across the observed spectrum between the 'Fast' and 'Slow' edge rate settings is -1.3327dB. Figure 147 illustrates the plot for this comparison.

5.5.4.2 Delta 6 – LVCMOS25-2mA-Fast to LVCMOS25-2mA-Slow Comparison

Delta 6 examines the variation to peak level emissions between the 'LVCMOS25-2mA-Fast' and the 'LVCMOS25-2mA-Slow' driver settings. Ultimately quantifying the change to peak level emissions between the 'Fast' and 'Slow' edge rate settings when using the LVCMOS25 technology using Equation 62.

$$\Delta_6 = A_{LVCMOS25-2mA-Fast} - A_{LVCMOS25-2mA-Slow}$$

Equation 62: Edge Rate Testing: Delta 6 – LVCMOS25-2mA-Fast to LVCMOS25-2mA-Slow Comparison

Where A_n is the vector that holds the peak level of emissions and Δ_n is the comparison equation.

The maxima of +10.73dB is recorded at approximately 790MHz, this is the highest point where the 'Fast' setting is greater than the 'Slow' setting in terms of the peak level of emissions. The minima of -3.78dB is recorded at approximately 290MHz, with the minima depicting the point where the 'Slow' setting is higher than the 'Fast' setting again in terms of the peak level of emissions recorded. The average level of change across the observed spectrum between the 'Fast' and 'Slow' edge rate settings is 0.605dB. Figure 148 illustrates the plot for this comparison.

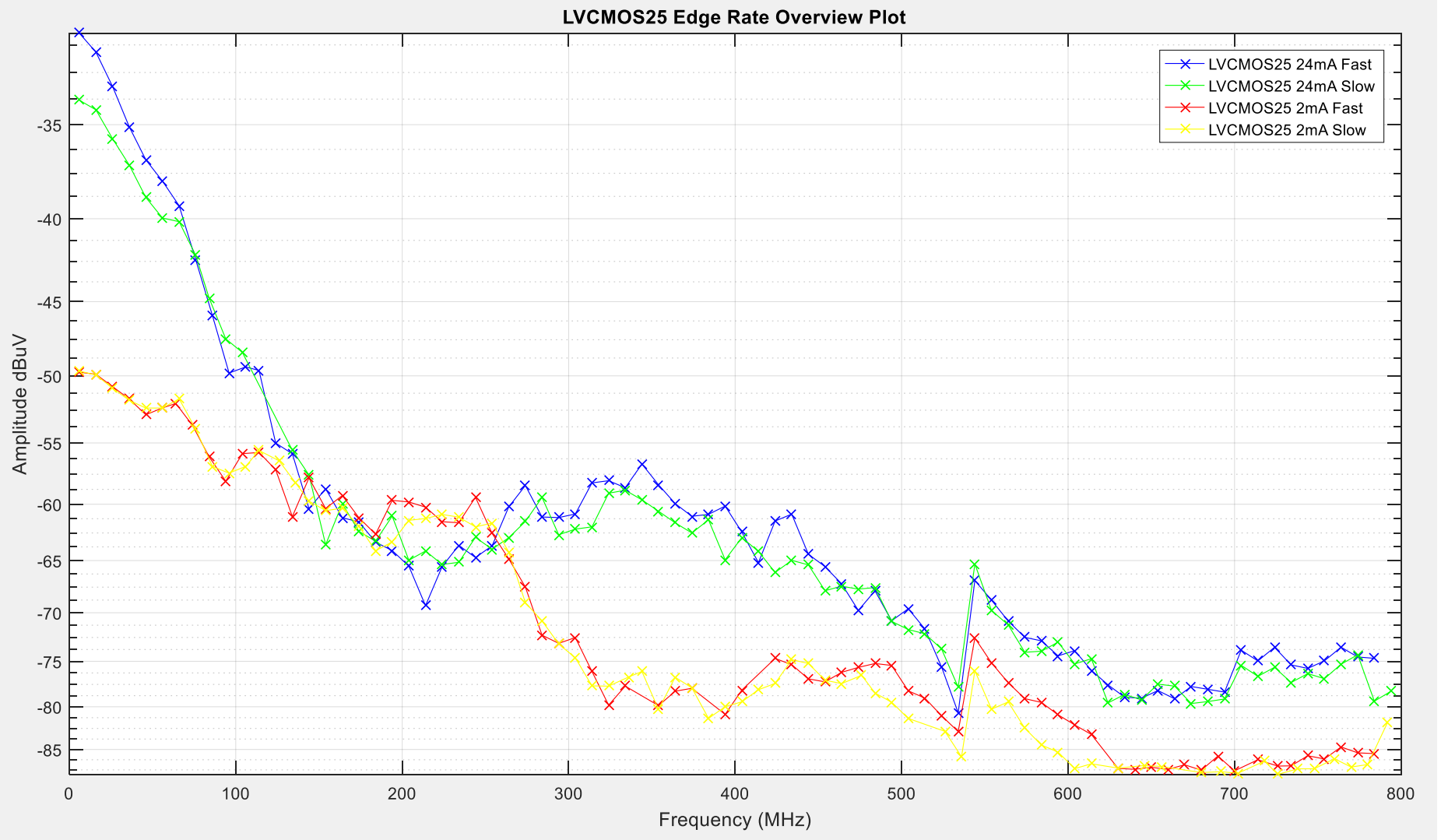


Figure 144: LVCMOS25 Edge Rate Comparison Overview

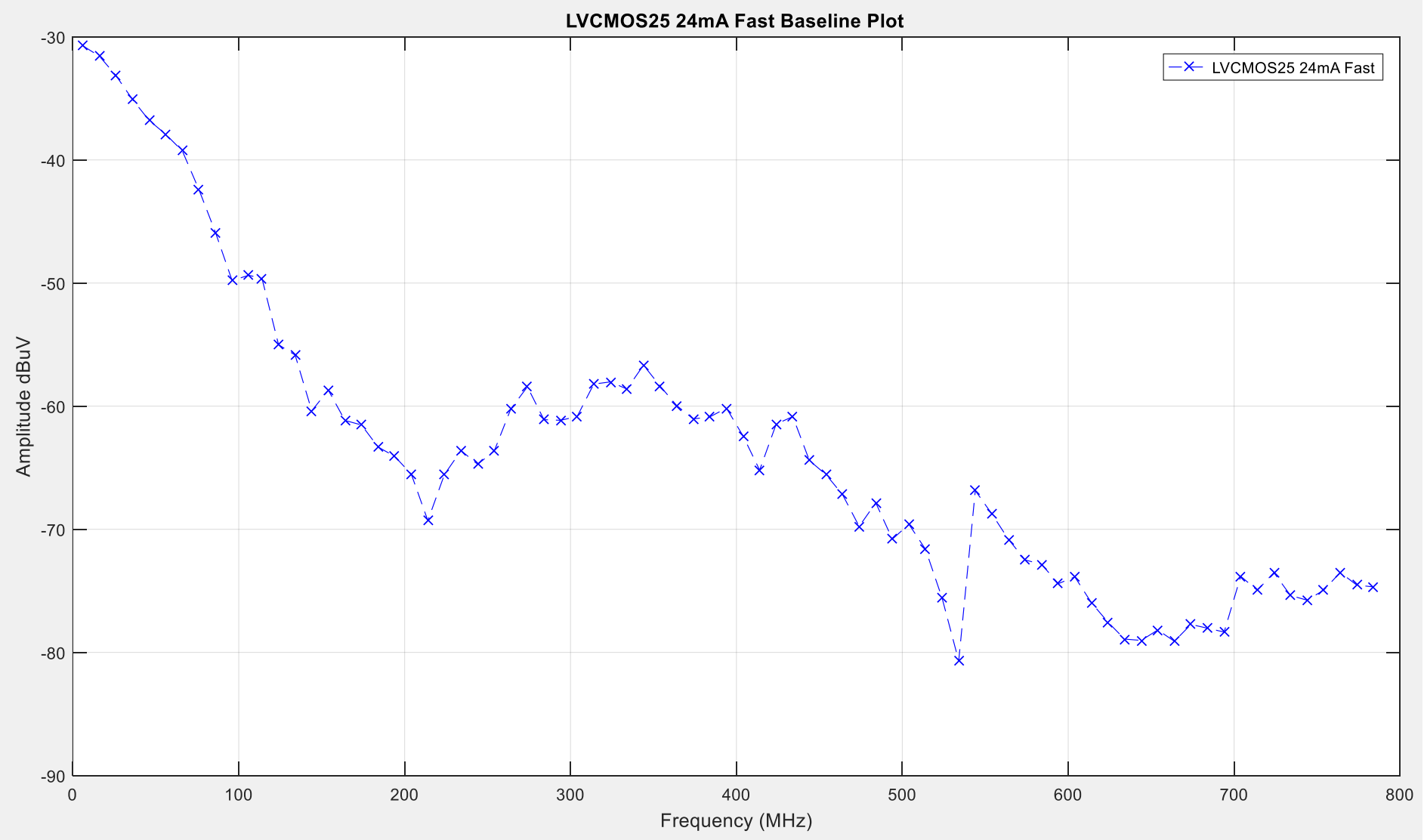


Figure 145: LVCMOS25-24mA-Fast Baseline Plot

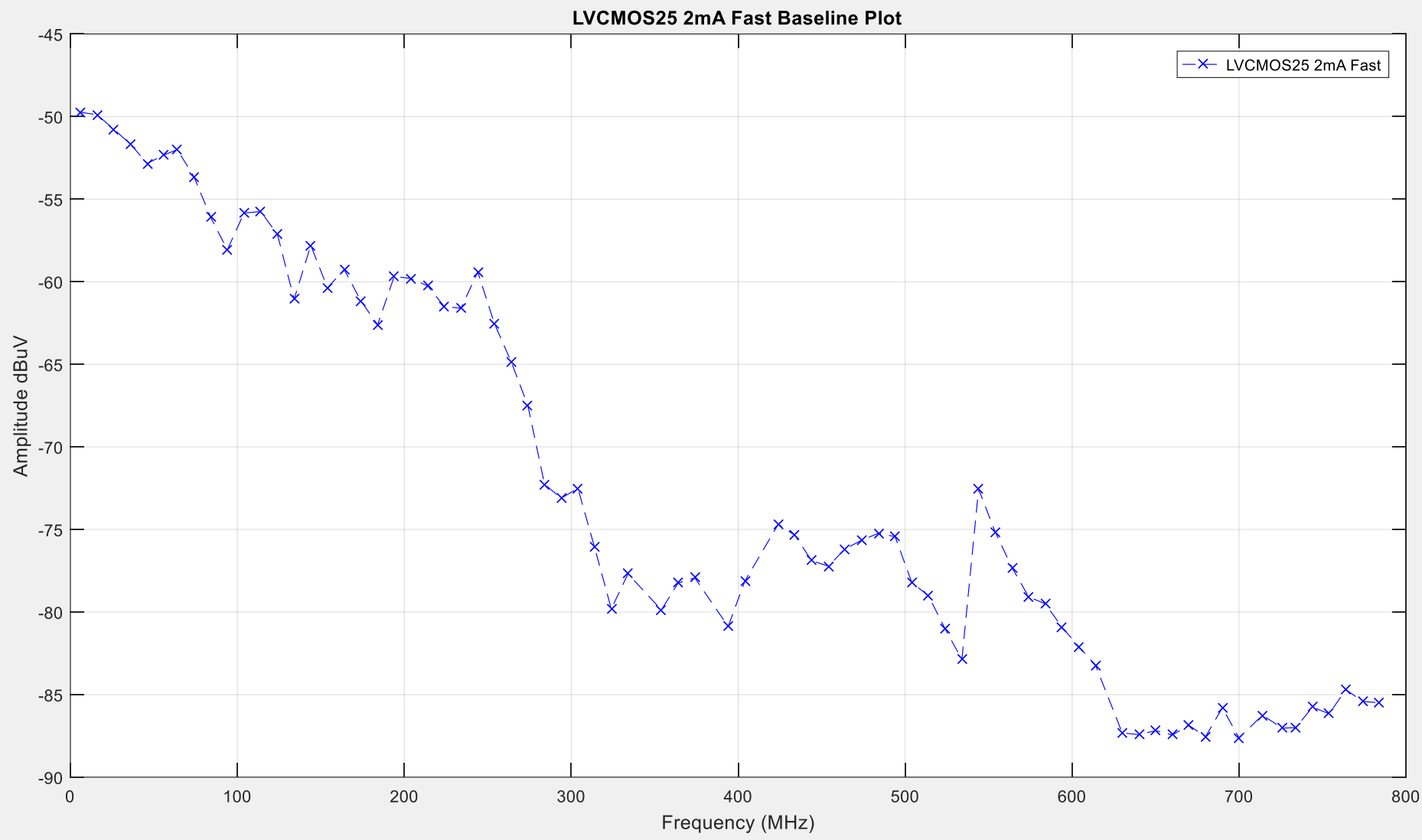


Figure 146: LVCMOS25-2mA-Fast Baseline Plot

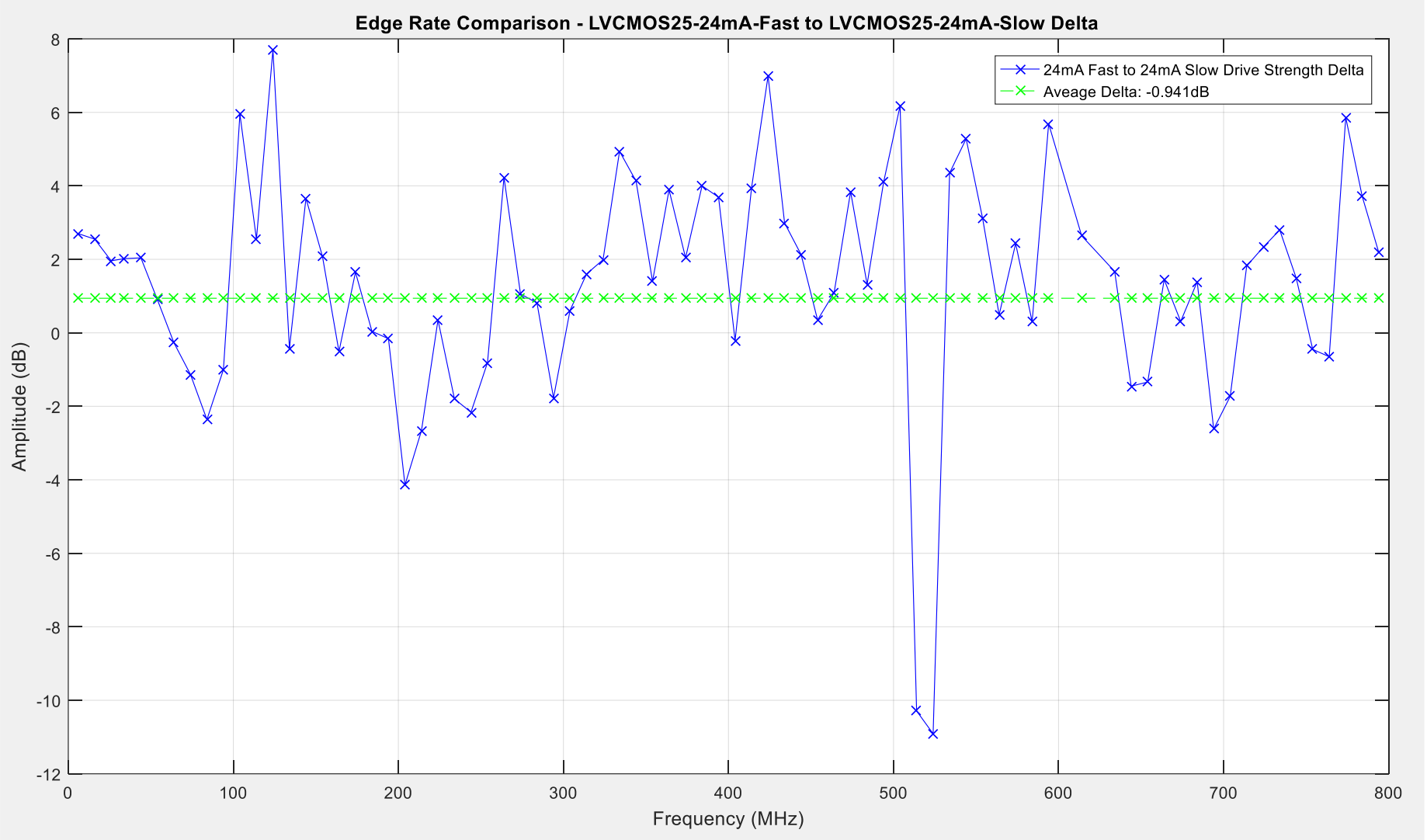


Figure 147: LVCMOS25-24mA-Fast to LVCMOS25-24mA-Slow Edge Rate Comparison

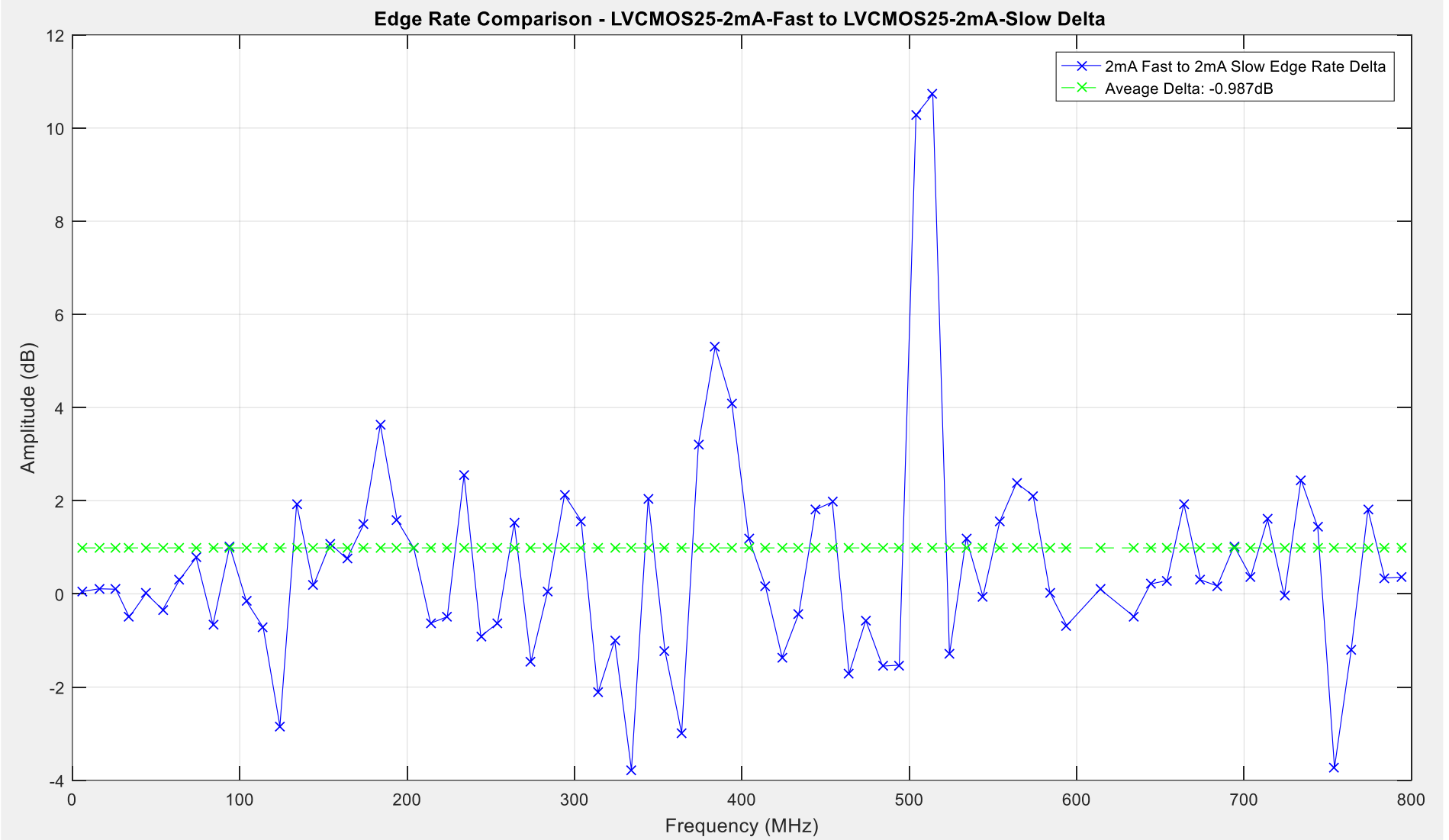


Figure 148: LVCMOS25-2mA-Fast to LVCCMOS33-2mA-Slow Edge Rate Comparison

5.5.5 LVCMOS18 Edge Rate Results

The traces illustrated in Figure 144 show the peak level of emissions recorded for the LVCMOS18 I/O buffer edge rate settings detailed in Table 29 below.

Driver Setting	LVCMOS18 Average of Peak Harmonic Level dBµV	Delta dB
LVCMOS18-24mA-Fast	-62.9278	-0.8301
LVCMOS18-24mA-Slow	-64.1558	
LVCMOS18-2mA-Fast	-72.7413	-1.6354
LVCMOS18-2mA-Slow	-73.7525	

Table 29: LVCMOS18 Edge Rate Emissions Results

From these results obtained it gives an indication of how much variation occurs on average across the peak levels, but does not give an indication of how this variation is distributed across the emissions spectrum. To achieve a more detailed comparison between the edge rate settings, closer comparisons have been done to illustrate how the level of emissions varies across the observed spectrum. Two comparisons have taken place at opposite ends of the respective drive strength capabilities to illustrate how the edge rate can influence the peak level of emissions produced. The 'LVCMOS18-24mA-Fast' I/O driver setting has been used as the baseline for the first comparison against the 'LVCMOS18-24mA-Slow', for reference this trace is illustrated in Figure 149. The 'LVCMOS18-2mA-Fast' I/O driver setting has been used as the baseline for the second comparison against the 'LVCMOS18-2mA-Slow', for reference this trace is illustrated in Figure 150.

5.5.5.1 Delta 7 – LVCMOS18-24mA-Fast to LVCMOS18-24mA-Slow Comparison

Delta 7 examines the variation to peak level emissions between the 'LVCMOS18-24mA-Fast' and the 'LVCMOS18-24mA-Slow' driver settings. Ultimately quantifying the change to peak level emissions between the 'Fast' and 'Slow' edge rate settings when using the LVCMOS18 technology using Equation 63.

$$\Delta_7 = A_{LVCMOS18-24mA-Fast} - A_{LVCMOS18-24mA-Slow}$$

Equation 63: Edge Rate Testing: Delta 7 – LVCMOS18-24mA-Fast to LVCMOS18-24mA-Slow Comparison

Where A_n is the vector that holds the peak level of emissions and Δ_n is the comparison equation.

The maxima of +14.17dB is recorded at approximately 660MHz, this is the highest point where the 'Fast' setting is greater than the 'Slow' setting in terms of the peak level of emissions. The minima of -6.29dB is recorded at approximately 150MHz, with the minima depicting the point where the 'Slow' setting is higher than the 'Fast' setting again in terms of the peak level of emissions recorded. The average level of change across the observed spectrum between the 'Fast' and 'Slow' edge rate settings is -0.83dB. Figure 151 illustrates the plot for this comparison.

5.5.5.2 Delta 8 – LVCMOS18-2mA-Fast to LVCMOS18-2mA-Slow Comparison

Delta 8 examines the variation to peak level emissions between the 'LVCMOS18-2mA-Fast' and the 'LVCMOS18-2mA-Slow' driver settings. Ultimately quantifying the change to peak level emissions between the 'Fast' and 'Slow' edge rate settings when using the LVCMOS18 technology using Equation 64.

$$\Delta_8 = A_{LVCMOS18-2mA-Fast} - A_{LVCMOS18-2mA-Slow}$$

Equation 64: Edge Rate Testing: Delta 8 – LVCMOS18-2mA-Fast to LVCMOS18-2mA-Slow Comparison

Where A_n is the vector that holds the peak level of emissions and Δ_n is the comparison equation.

The maxima of +11.11dB is recorded at approximately 520MHz, this is the highest point where the 'Fast' setting is greater than the 'Slow' setting in terms of the peak level of emissions. The minima of -4.79dB is recorded at approximately 710MHz, with the minima depicting the point where the 'Slow' setting is higher than the 'Fast' setting again in terms of the peak level of emissions recorded. The average level of change across the observed spectrum between the 'Fast' and 'Slow' edge rate settings is 1.657dB. Figure 153 illustrates the plot for this comparison.

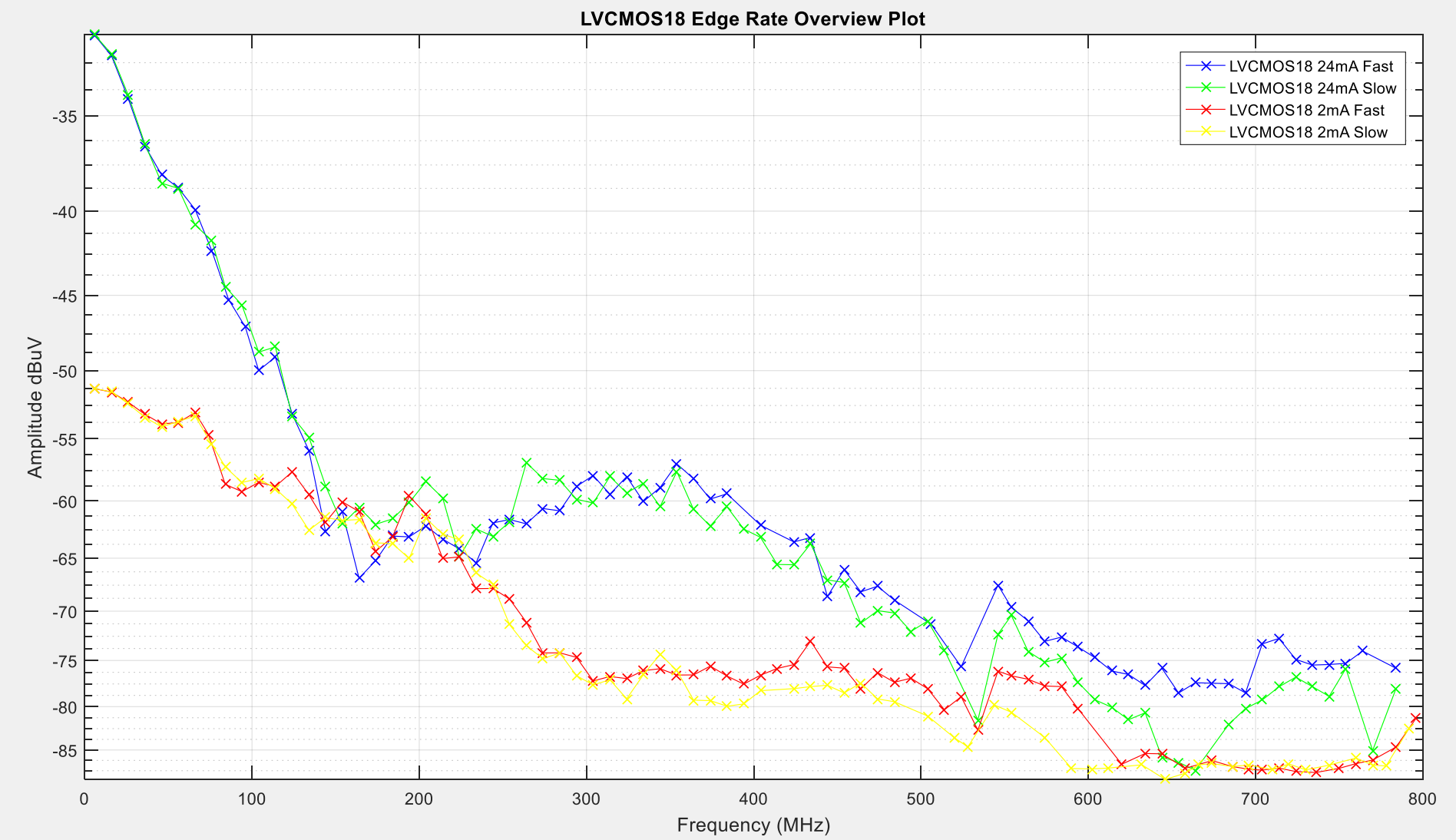


Figure 149: LVCMOS18 Edge Rate Comparison Overview

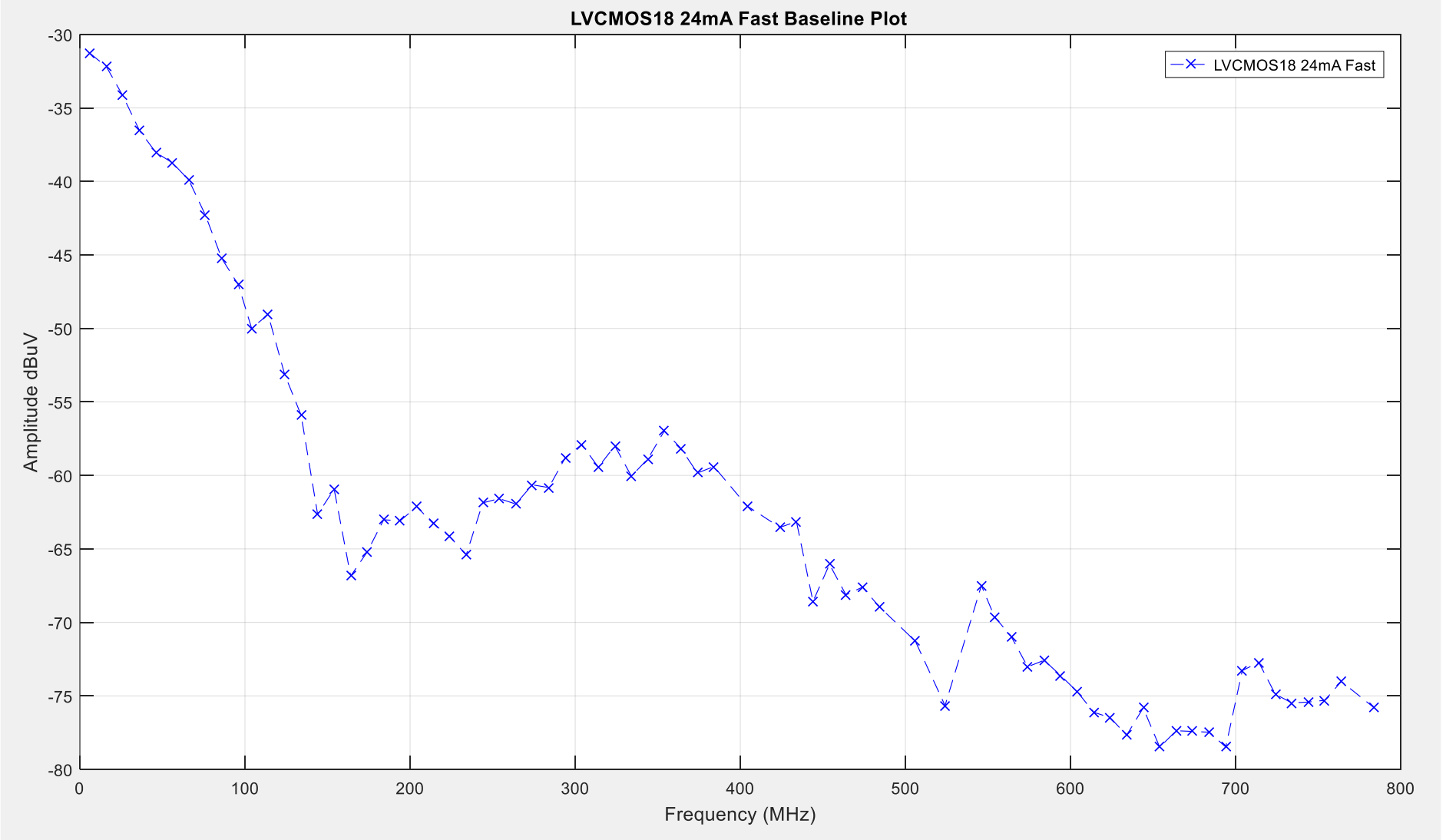


Figure 150: LVCMOS18-24mA-Fast Baseline Plot

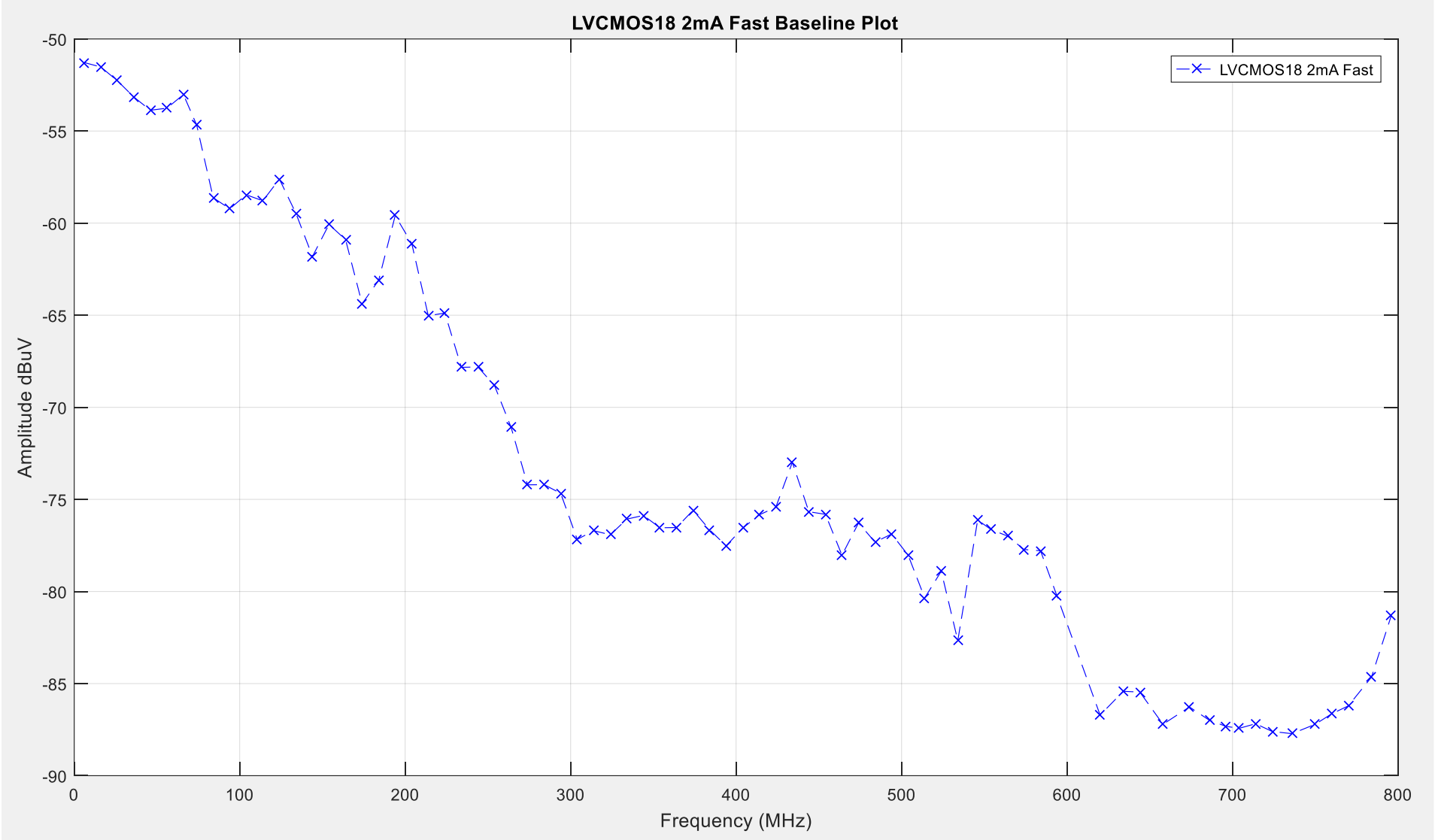


Figure 151: LVCMOS18-2mA-Fast Baseline Plot

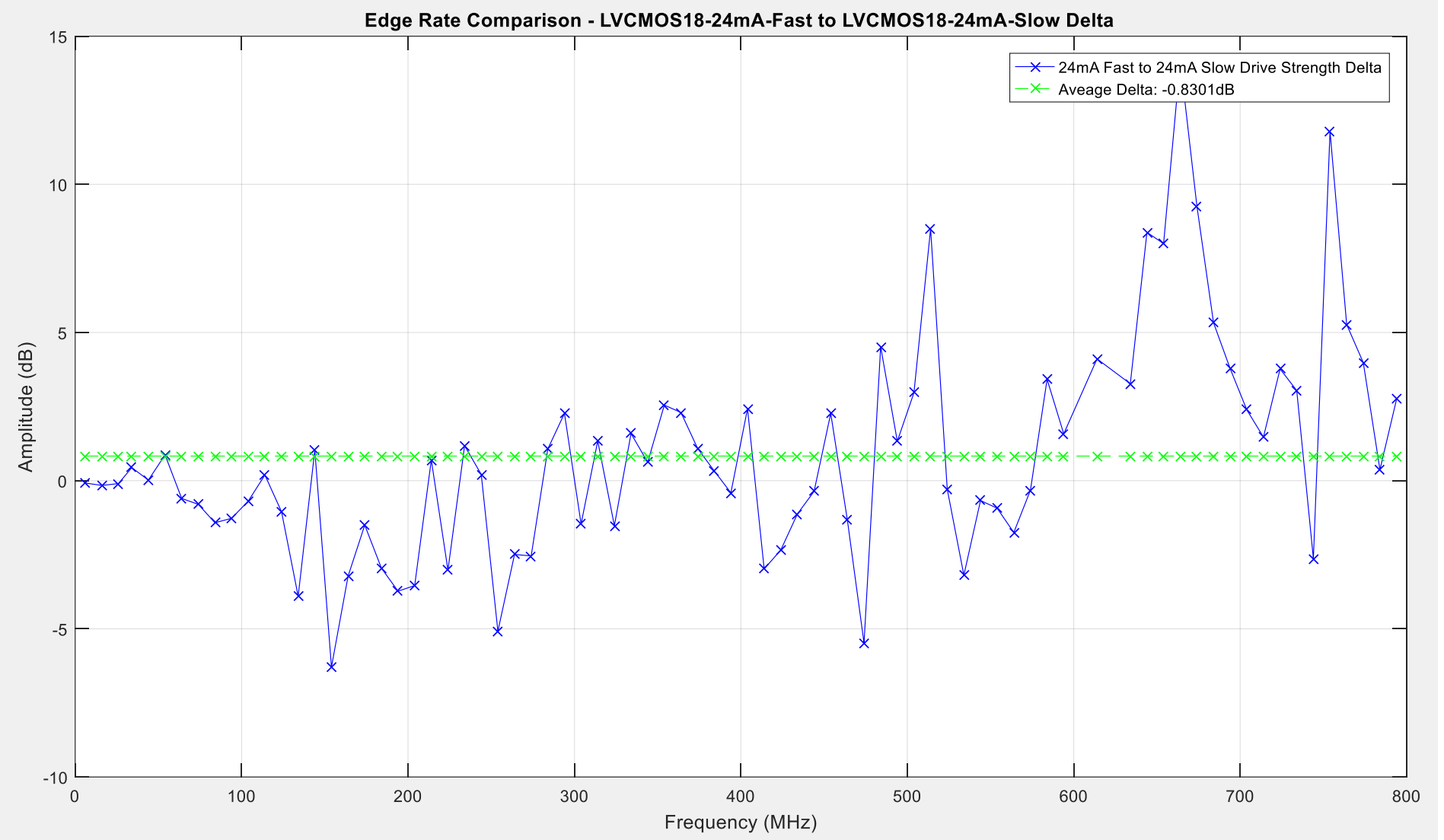


Figure 152: LVCMOS18-24mA-Fast to LVCMOS18-24mA-Slow Edge Rate Comparison

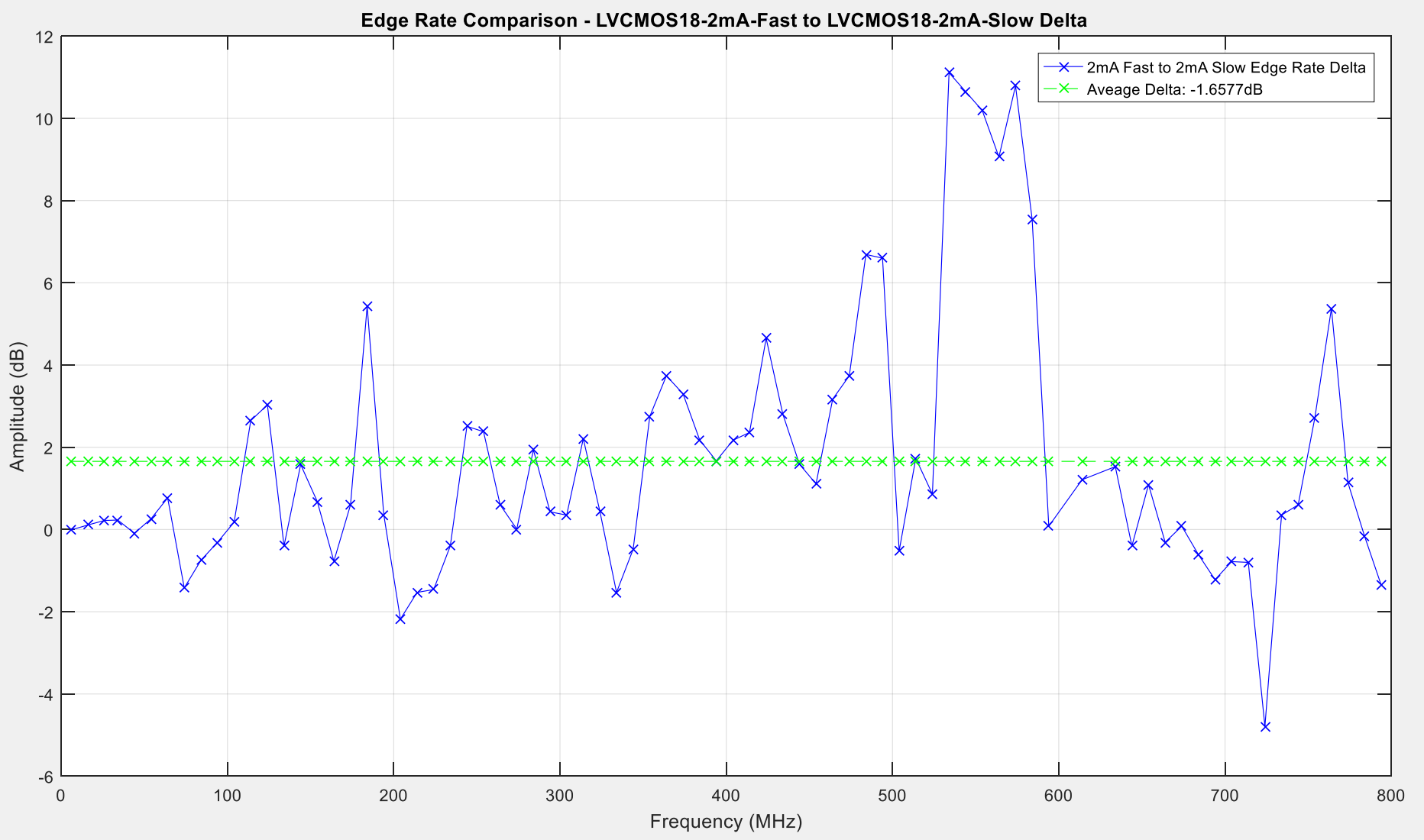


Figure 153: LVCMOS18-24mA-Fast to LVCMOS18-24mA-Slow Edge Rate Comparison

5.5.6 LVCMOS15 Edge Rate Results

The traces illustrated in Figure 154 show the peak level of emissions recorded for the LVCMOS15 I/O buffer edge rate settings detailed in Table 30 below.

Driver Setting	LVCMOS15 Average of Peak Harmonic Level dBµV	Delta dB
LVCMOS15-16mA-Fast	-65.9496	1.7
LVCMOS15-16mA-Slow	-67.6404	
LVCMOS15-2mA-Fast	-74.4882	1.9973
LVCMOS15-2mA-Slow	-76.4704	

Table 30: LVCMOS15 Edge Rate Emissions Results

From these results obtained it gives an indication of how much variation occurs on average across the peak levels, but does not give an indication of how this variation is distributed across the emissions spectrum. To achieve a more detailed comparison between the edge rate settings, closer comparisons have been done to illustrate how the level of emissions varies across the observed spectrum. Two comparisons have taken place at opposite ends of the respective drive strength capabilities to illustrate how the edge rate can influence the peak level of emissions produced. The 'LVCMOS15-16mA-Fast' I/O driver setting has been used as the baseline for the first comparison against the 'LVCMOS18-16mA-Slow', for reference this trace is illustrated in Figure 155. The 'LVCMOS15-2mA-Fast' I/O driver setting has been used as the baseline for the second comparison against the 'LVCMOS15-2mA-Slow', for reference this trace is illustrated in Figure 156.

5.5.6.1 Delta 9 – LVCMOS15-16mA-Fast to LVCMOS15-16mA-Slow Comparison

Delta 9 examines the variation to peak level emissions between the 'LVCMOS15-16mA-Fast' and the 'LVCMOS15-16mA-Slow' driver settings. Ultimately quantifying the change to peak level emissions between the 'Fast' and 'Slow' edge rate settings when using the LVCMOS18 technology using Equation 65.

$$\Delta_9 = A_{LVCMOS15-16mA-Fast} - A_{LVCMOS15-16mA-Slow}$$

Equation 65: Edge Rate Testing: Delta 9 – LVCMOS15-16mA-Fast to LVCMOS18-16mA-Slow Comparison

Where A_n is the vector that holds the peak level of emissions and Δ_n is the comparison equation.

The maxima of +12.36dB is recorded at approximately 505MHz, this is the highest point where the 'Fast' setting is greater than the 'Slow' setting in terms of the peak level of emissions. The minima of -11.39dB is recorded at approximately 520MHz, with the minima depicting the point where the 'Slow' setting is higher than the 'Fast' setting again in terms of the peak level of emissions recorded. The average level of change across the observed spectrum between the 'Fast' and 'Slow' edge rate settings is -1.7dB. Figure 157 illustrates the plot for this comparison.

5.5.6.2 Delta 10 – LVCMOS15-2mA-Fast to LVCMOS15-2mA-Slow Comparison

Delta 10 examines the variation to peak level emissions between the 'LVCMOS15-2mA-Fast' and the 'LVCMOS15-2mA-Slow' driver settings. Ultimately quantifying the change to peak level emissions between the 'Fast' and 'Slow' edge rate settings when using the LVCMOS15 technology using Equation 66.

$$\Delta_{10} = A_{LVCMOS15-2mA-Fast} - A_{LVCMOS15-2mA-Slow}$$

Equation 66: Edge Rate Testing: Delta 10 – LVCMOS15-2mA-Fast to LVCMOS15-2mA-Slow Comparison

Where A_n is the vector that holds the peak level of emissions and Δ_n is the comparison equation.

The maxima of +12.07dB is recorded at approximately 540MHz, this is the highest point where the 'Fast' setting is greater than the 'Slow' setting in terms of the peak level of emissions. The minima of -4.79dB is recorded at approximately 205MHz, with the minima depicting the point where the 'Slow' setting is higher than the 'Fast' setting again in terms of the peak level of emissions recorded. The average level of change across the observed spectrum between the 'Fast' and 'Slow' edge rate settings is 1.9773dB. Figure 158 illustrates the plot for this comparison.

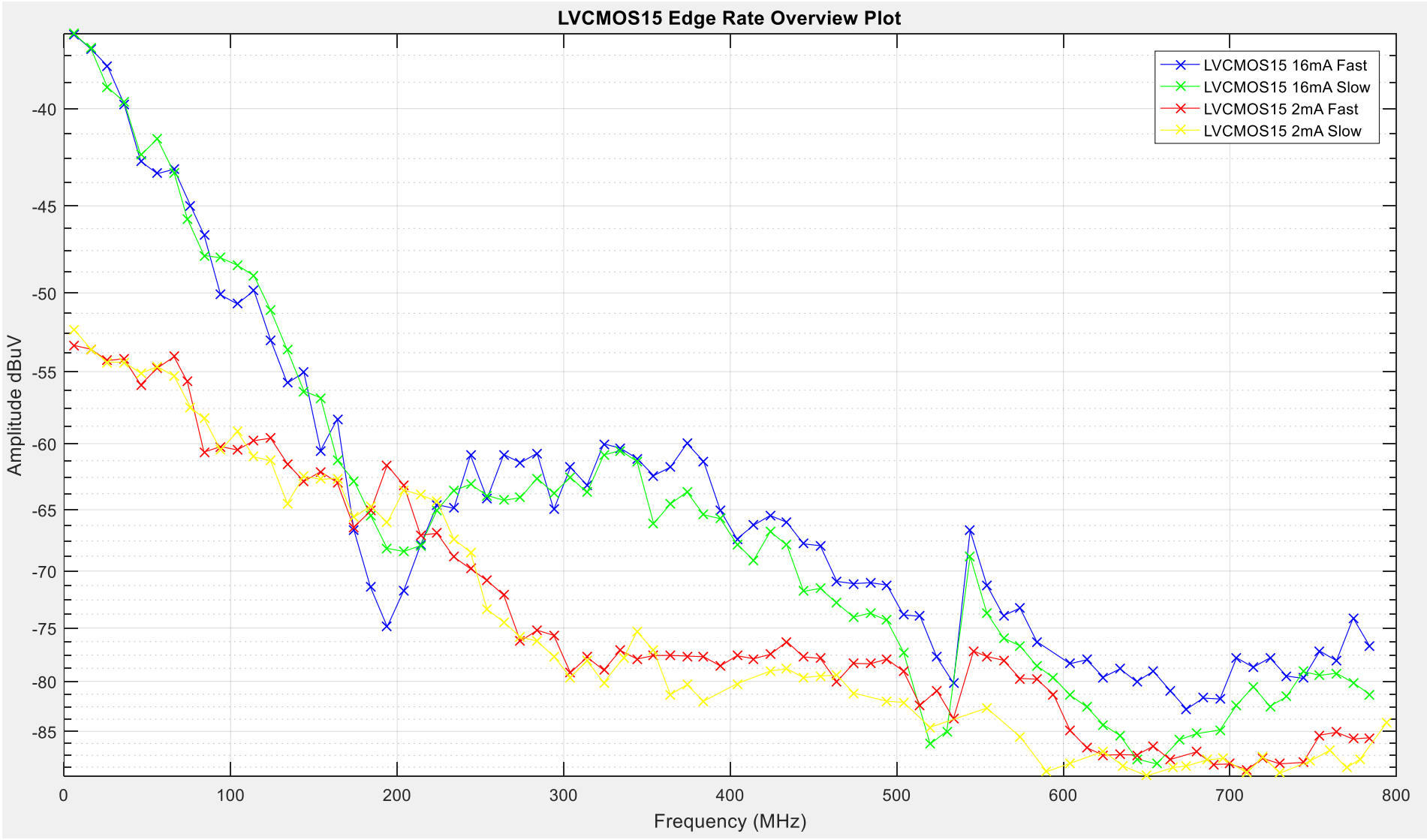


Figure 154: LVCMOS15 Edge Rate Comparison Overview

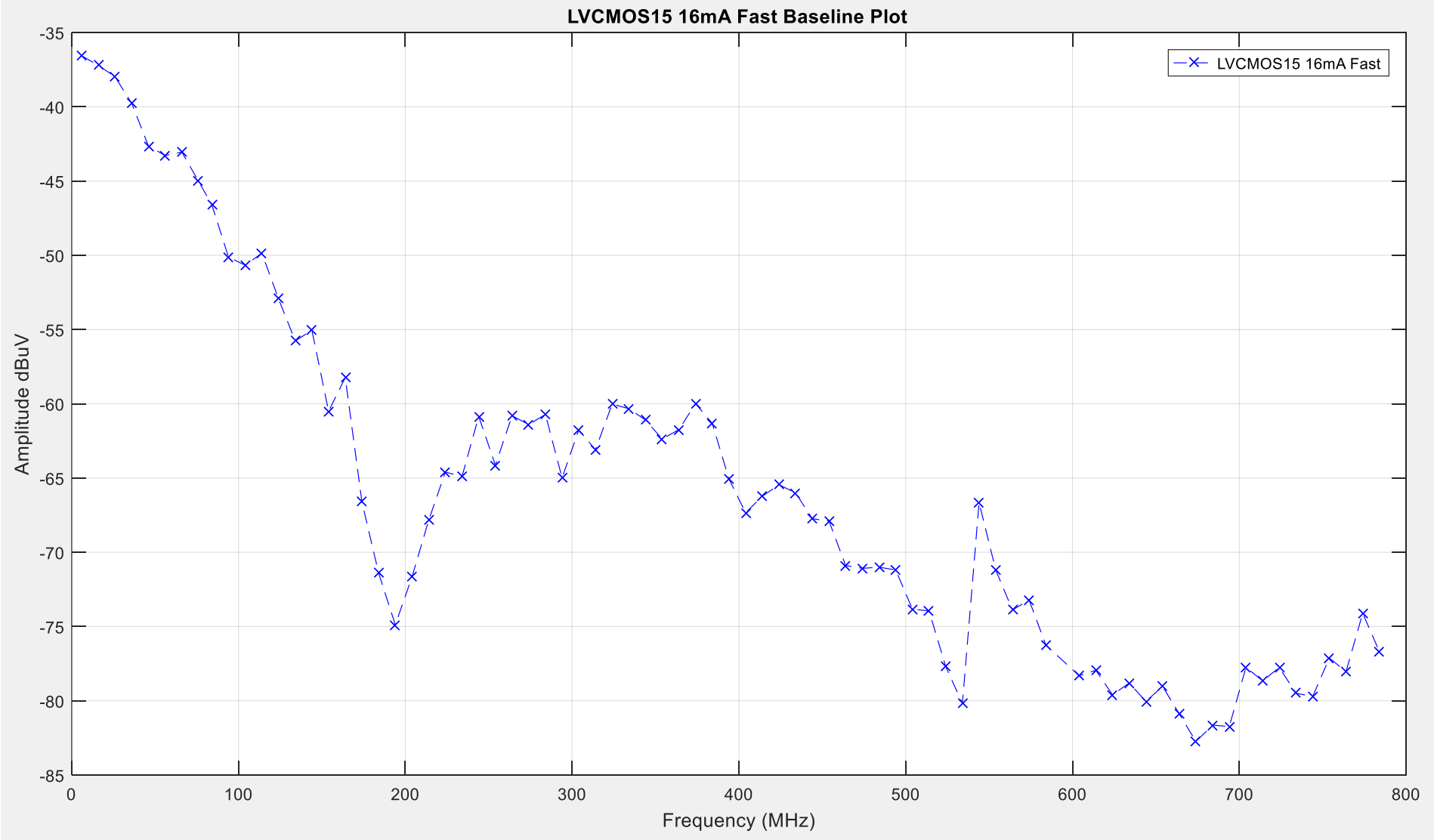


Figure 155: LVCMOS15-16mA-Fast Baseline Plot

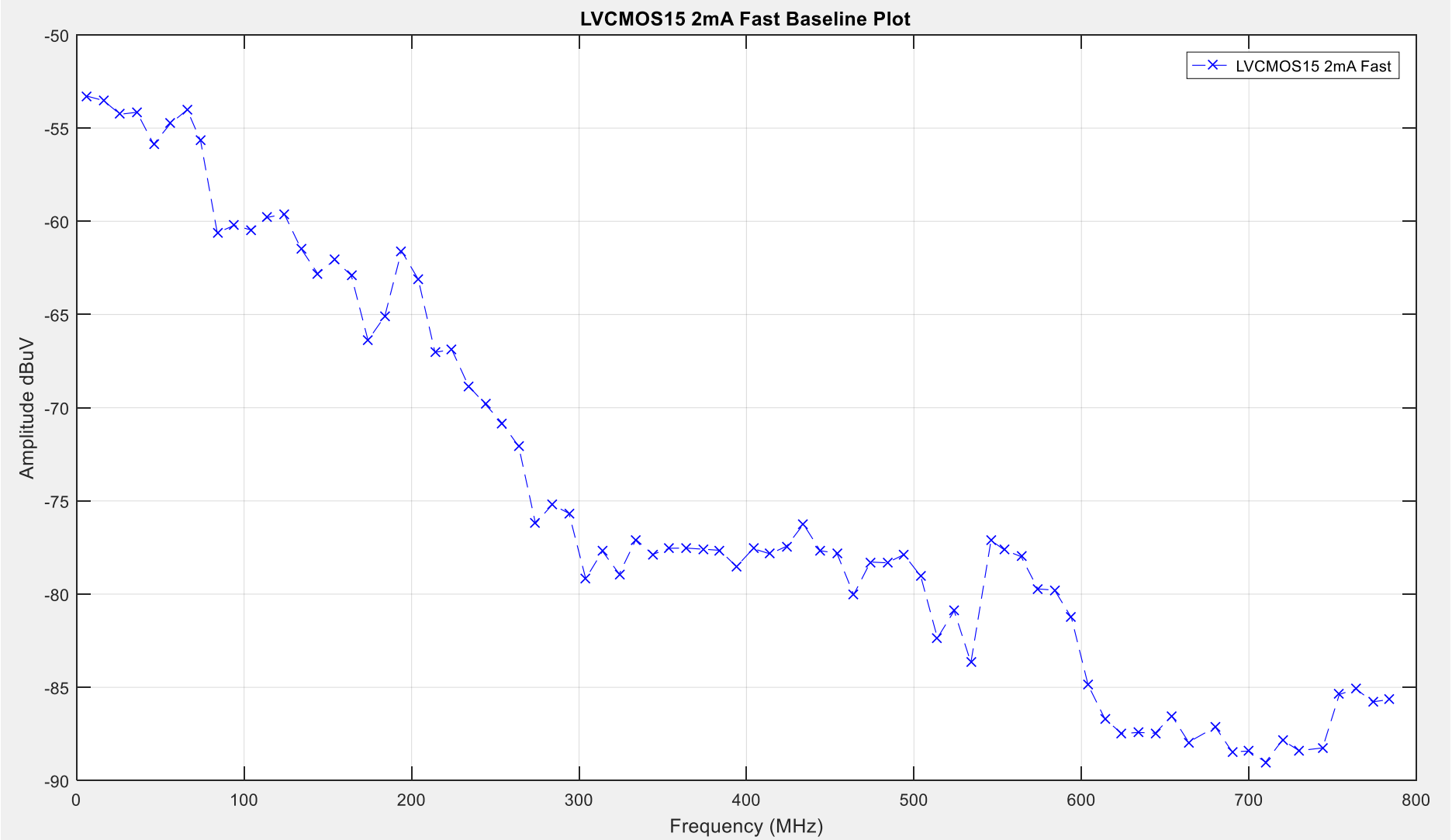


Figure 156: LVCMOS15-2mA-Fast Baseline Plot

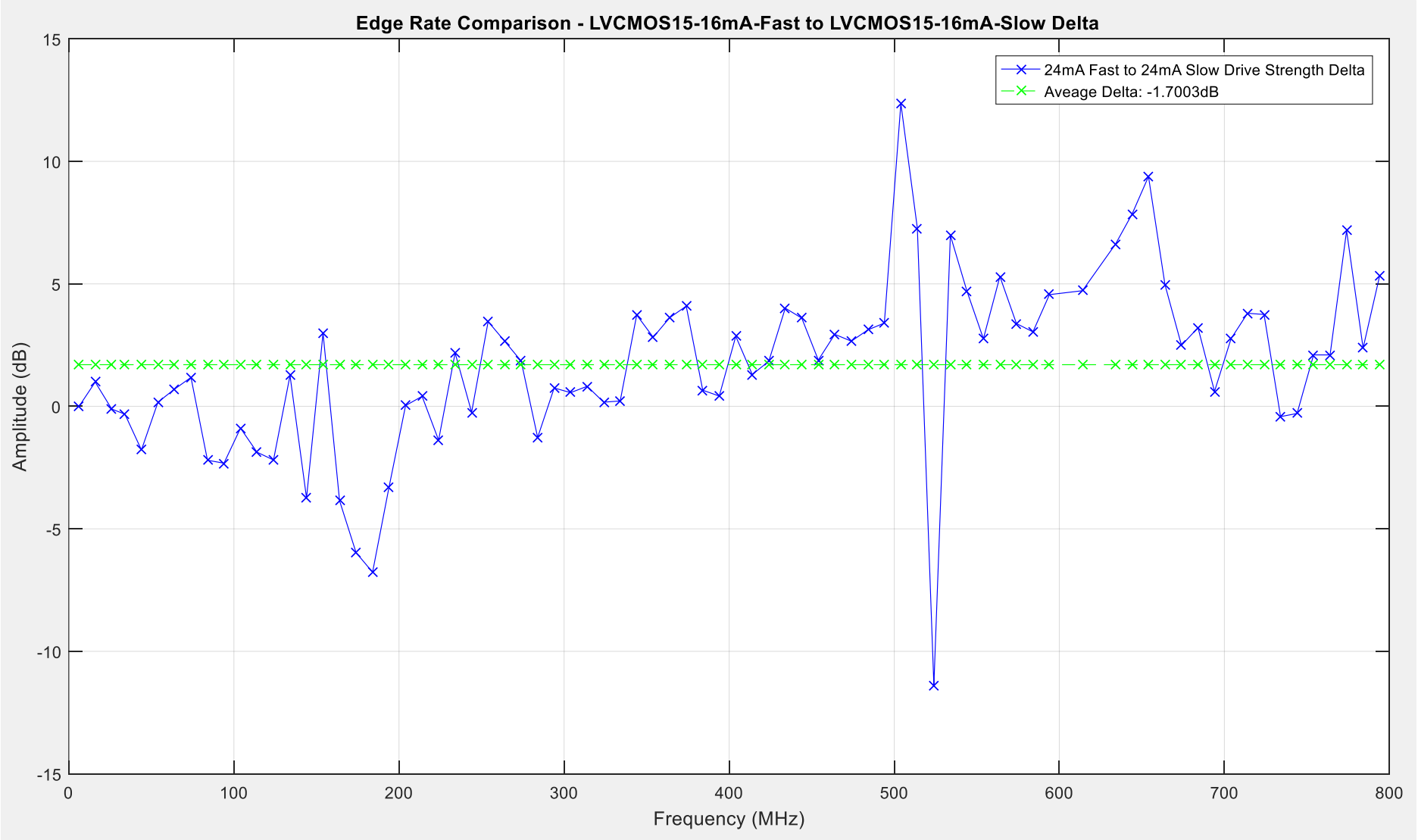


Figure 157: LVCMOS15-16mA-Fast to LVCMOS15-16mA-Slow Edge Rate Comparison

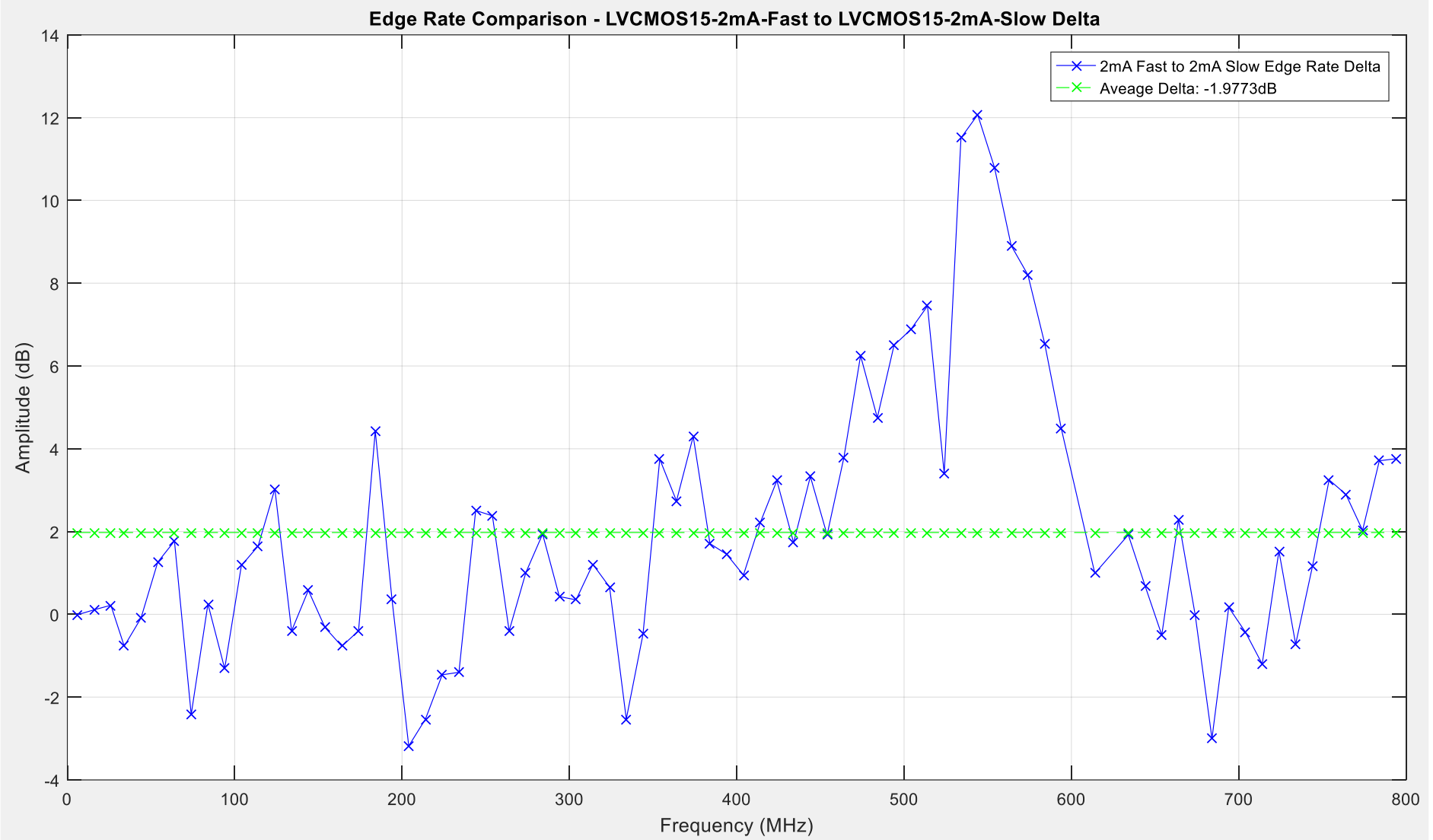


Figure 158: LVCMOS15-2mA-Fast to LVCMOS15-2mA-Slow Edge Rate Comparison

5.5.7 LVCMOS12 Edge Rate Results

The traces illustrated in Figure 159 show the peak level of emissions recorded for the LVCMOS12 I/O buffer edge rate settings detailed in Table 31 below.

Driver Setting	LVCMOS12 Average of Peak Harmonic Level dBµV	Delta dB
LVCMOS12-12mA-Fast	-65.3499	2.306
LVCMOS12-12mA-Slow	-67.6404	
LVCMOS12-2mA-Fast	-72.0559	1.83
LVCMOS12-2mA-Slow	-73.2297	

Table 31: LVCMOS12 Edge Rate Emissions Results

From these results obtained it gives an indication of how much variation occurs on average across the peak levels, but does not give an indication of how this variation is distributed across the emissions spectrum. To achieve a more detailed comparison between the edge rate settings, closer comparisons have been done to illustrate how the level of emissions varies across the observed spectrum. Two comparisons have taken place at opposite ends of the respective drive strength capabilities to illustrate how the edge rate can influence the peak level of emissions produced. The 'LVCMOS12-12mA-Fast' I/O driver setting has been used as the baseline for the first comparison against the 'LVCMOS12-12mA-Slow', for reference this trace is illustrated in Figure 160. The 'LVCMOS12-2mA-Fast' I/O driver setting has been used as the baseline for the second comparison against the 'LVCMOS12-2mA-Slow', for reference this trace is illustrated in Figure 161.

5.5.7.1 Delta 11 – LVCMOS12-12mA-Fast to LVCMOS12-12mA-Slow Comparison

Delta 11 examines the variation to peak level emissions between the 'LVCMOS12-12mA-Fast' and the 'LVCMOS12-12mA-Slow' driver settings. Ultimately quantifying the change to peak level emissions between the 'Fast' and 'Slow' edge rate settings when using the LVCMOS12 technology using Equation 67.

$$\Delta_9 = A_{LVCMOS12-16mA-Fast} - A_{LVCMOS12-12mA-Slow}$$

Equation 67: Edge Rate Testing: Delta 11 – LVCMOS12-12mA-Fast to LVCMOS12-12mA-Slow Comparison

Where A_n is the vector that holds the peak level of emissions and Δ_n is the comparison equation.

The maxima of +7.94dB is recorded at approximately 505MHz, this is the highest point where the 'Fast' setting is greater than the 'Slow' setting in terms of the peak level of emissions. The minima of -7.54dB is recorded at approximately 520MHz, with the minima depicting the point where the 'Slow' setting is higher than the 'Fast' setting again in terms of the peak level of emissions recorded. The average level of change across the observed spectrum between the 'Fast' and 'Slow' edge rate settings is -2.3028dB. Figure 162 illustrates the plot for this comparison.

5.5.7.2 Delta 12 – LVCMOS12-2mA-Fast to LVCMOS12-2mA-Slow Comparison

Delta 12 examines the variation to peak level emissions between the 'LVCMOS12-2mA-Fast' and the 'LVCMOS12-2mA-Slow' driver settings. Ultimately quantifying the change to peak level emissions between the 'Fast' and 'Slow' edge rate settings when using the LVCMOS12 technology using Equation 68.

$$\Delta_{10} = A_{LVCMOS12-2mA-Fast} - A_{LVCMOS12-2mA-Slow}$$

Equation 68: Edge Rate Testing: Delta 12 – LVCMOS12-2mA-Fast to LVCMOS12-2mA-Slow Comparison

Where A_n is the vector that holds the peak level of emissions and Δ_n is the comparison equation.

The maxima of +9.98dB is recorded at approximately 650MHz, this is the highest point where the 'Fast' setting is greater than the 'Slow' setting in terms of the peak level of emissions. The minima of -4.79dB is recorded at approximately 520MHz, with the minima depicting the point where the 'Slow' setting is higher than the 'Fast' setting again in terms of the peak level of emissions recorded. The average level of change across the observed spectrum between the 'Fast' and 'Slow' edge rate settings is 1.8314dB. Figure 163 illustrates the plot for this comparison.

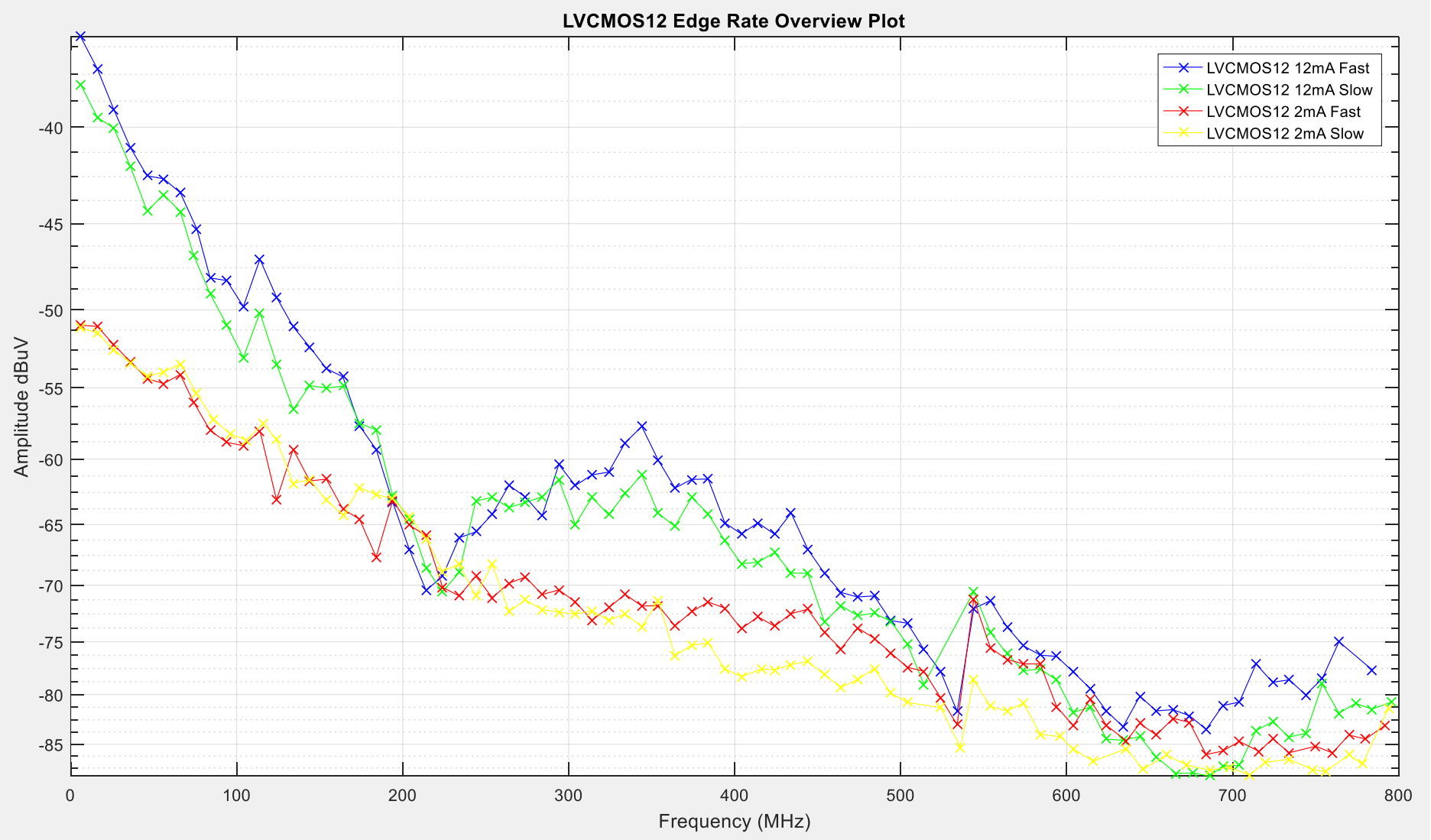


Figure 159: LVCMOS12 Edge Rate Comparison Overview

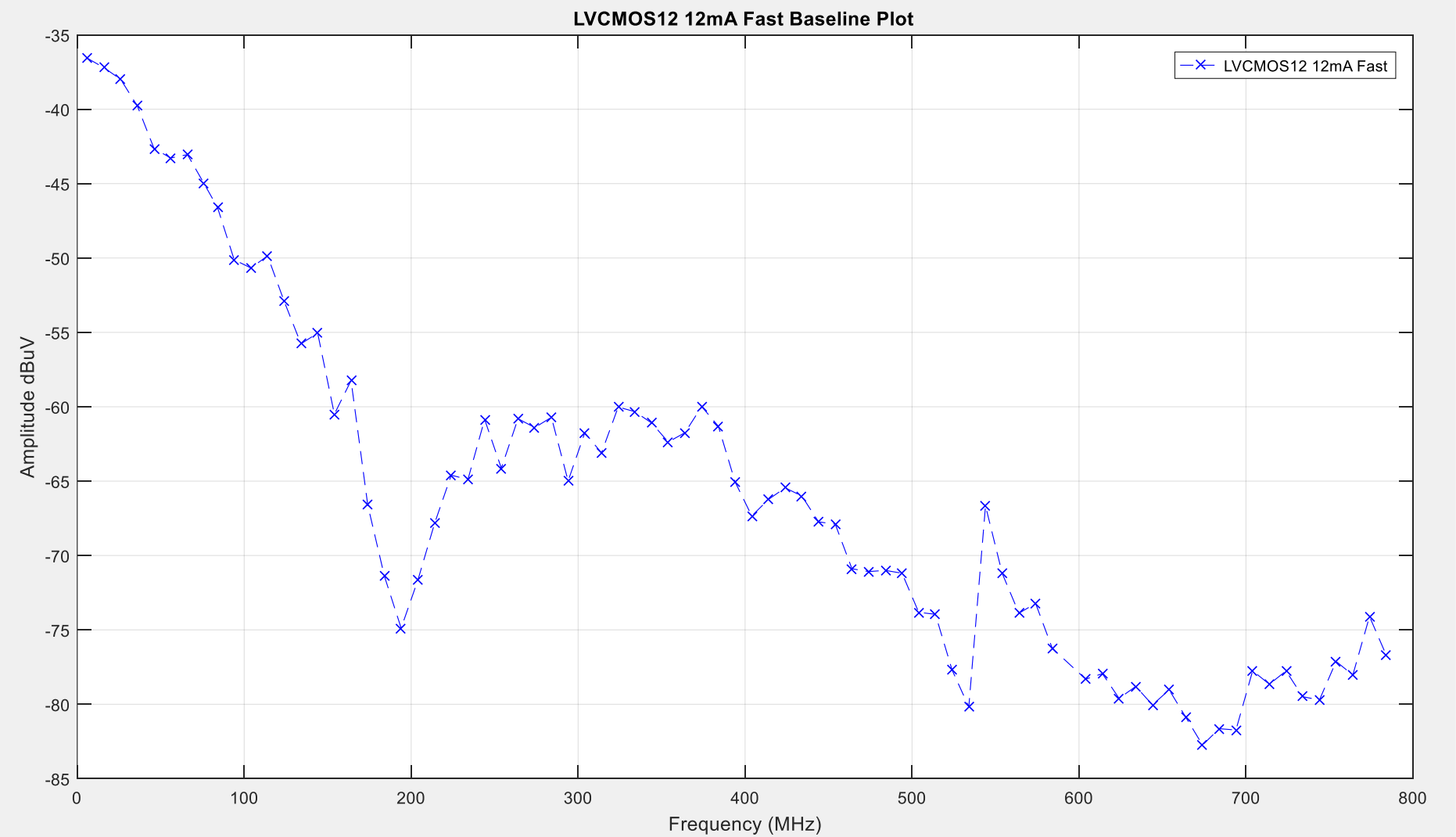


Figure 160: LVCMOS12 12mA Baseline Comparison

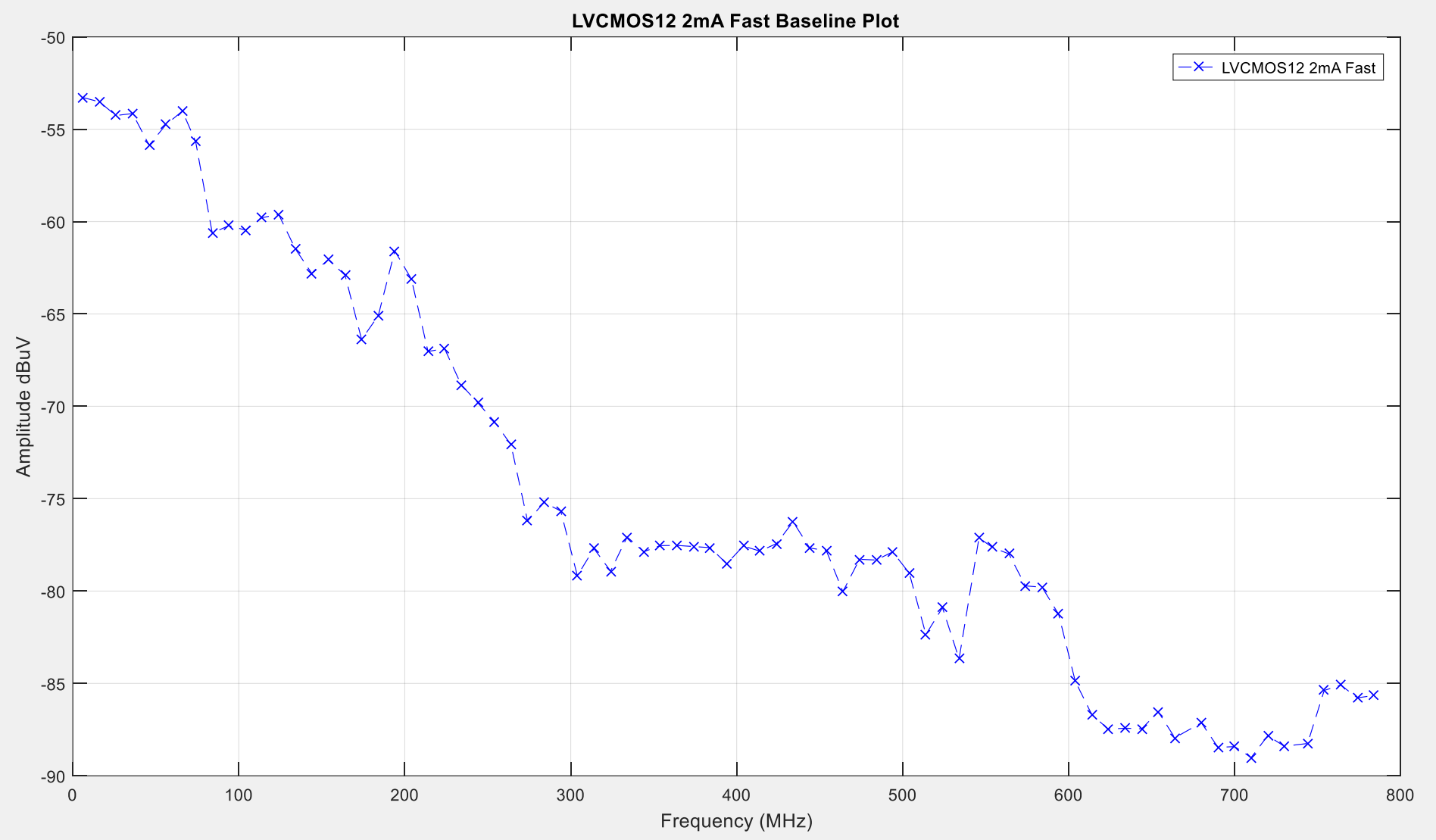


Figure 161: LVCMOS12 2mA Baseline Comparison

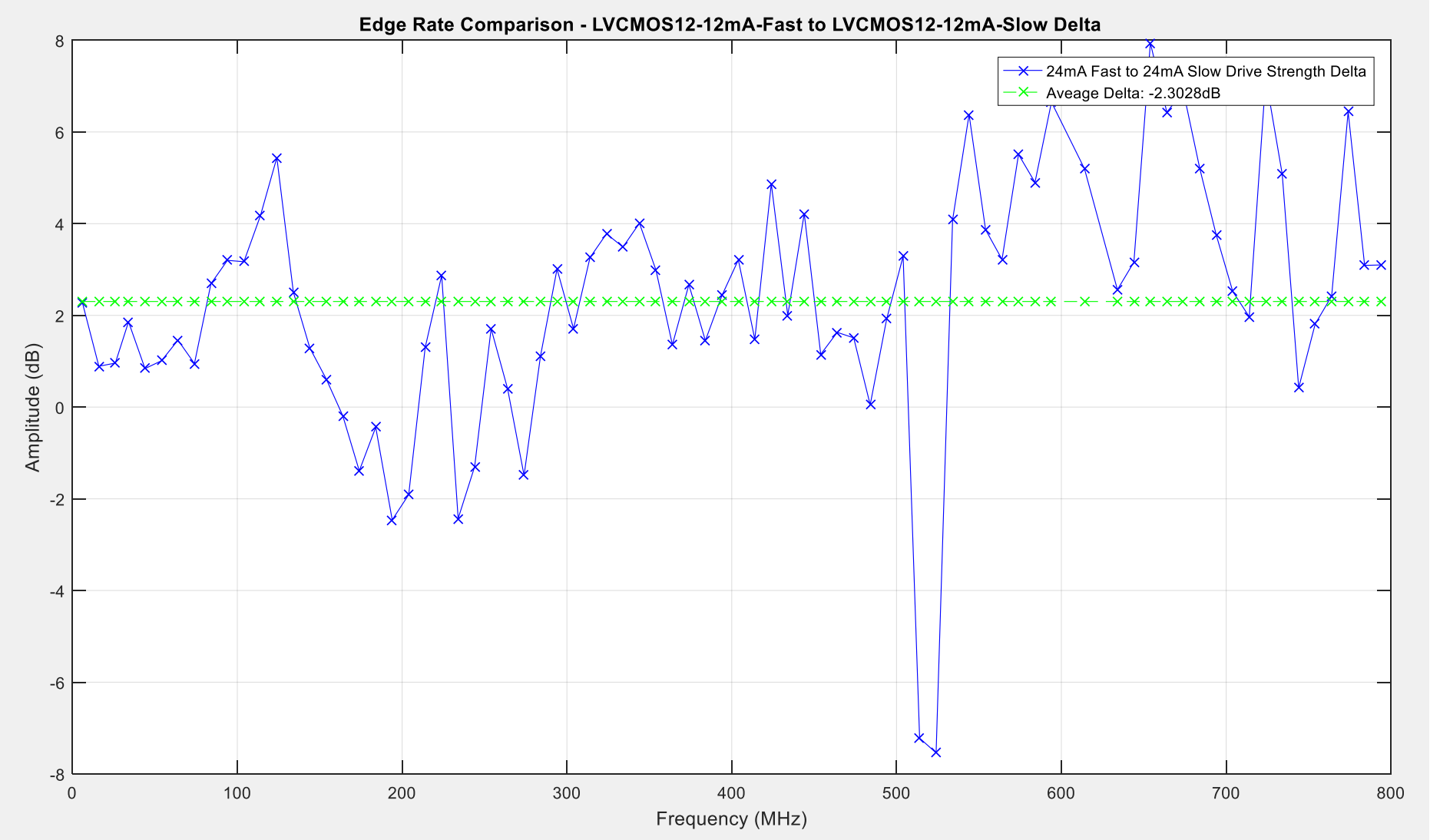


Figure 162: LVCMOS12-12mA-Fast to LVCMOS12-12mA-Slow Edge Rate Comparison

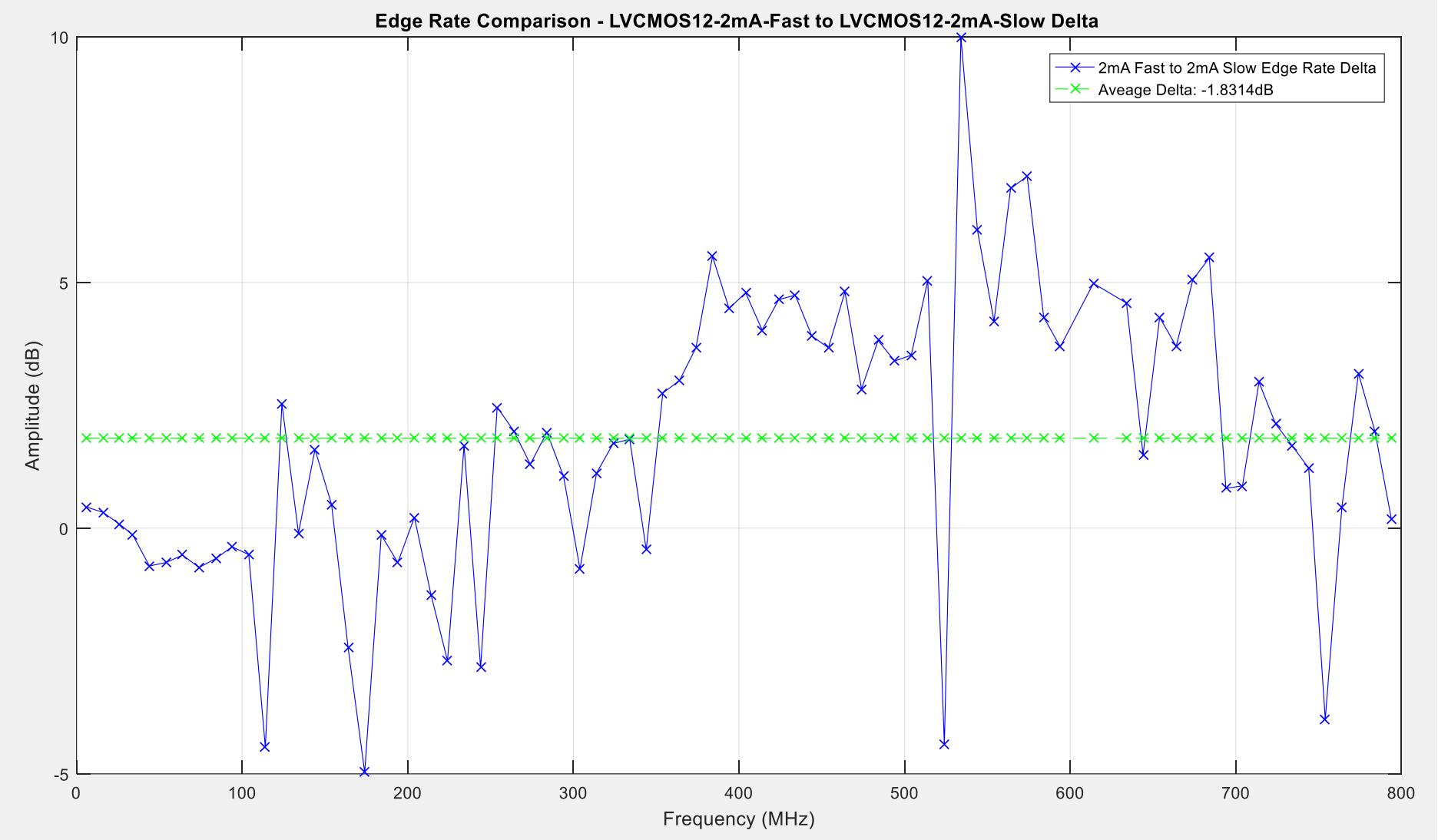


Figure 163: LVCMOS12-2mA-Fast to LVCMOS12-2mA-Slow Edge Rate Comparison

5.5.8 Edge Rate Testing Conclusion

The changes to the average level of peak emissions recorded through changing the edge rate setting varies across each of the I/O standards and drive strength settings detailed in Table 26 to Table 31. The magnitude of change to peak level emissions is dependent on the drive strength and I/O standard chosen. The variation to emissions recorded is significant enough to warrant careful consideration when selecting the edge rate setting within design process with the greatest recorded variation of emissions being approximately 2.3dB within the LVCMOS12 I/O standard.

Through changing the edge rate from 'Fast' to 'Slow' at a drive strength setting of '24mA' and '2mA', the highest average level of change to peak emissions recorded from the LVTTL I/O standard with a reduction of more than -1.05dB with a minimum drive strength setting of '2mA'. The greatest maxima seen from the comparison plots within the LVTTL standard is approximately 8.14dB, with a drive strength setting of 24mA. This translates as the point where emissions produced from the 'Fast' edge rate setting are higher than the 'Slow' edge rate setting.

Through changing the edge rate from 'Fast' to 'Slow' at a drive strength setting of '24mA' and '2mA', the highest average level of change to peak emissions recorded from the LVCMOS33 I/O standard with a reduction of more than -0.845dB with a minimum drive strength setting of '2mA'. The greatest maxima seen from the comparison plots within the LVCMOS33 standard is approximately 13.51dB, with a drive strength setting of 24mA. This translates as the point where emissions produced from the 'Fast' edge rate setting are higher than the 'Slow' edge rate setting.

Through changing the edge rate from 'Fast' to 'Slow at a drive strength setting of '24mA' and '2mA', the highest average level of change to peak emissions recorded from the LVCMOS25 I/O standard with a reduction of more than -1.2004dB with a maximum drive strength setting of '24mA'. The greatest maxima seen from the comparison plots within the LVCMOS25 standard is approximately 10.73dB, with a drive strength setting of 2mA. This translates as the point where emissions produced from the 'Fast' edge rate setting are higher than the 'Slow' edge rate setting.

Through changing the edge rate from 'Fast' to 'Slow at a drive strength setting of '24mA' and '2mA', the highest average level of change to peak emissions recorded from the LVCMOS18 I/O standard with a reduction of more than -1.6354dB with a maximum drive strength setting of '2mA'. The greatest maxima seen from the comparison plots within the LVCMOS18 standard is approximately 14.17dB, with a drive strength setting of 24mA. This translates as the point where emissions produced from the 'Fast' edge rate setting are higher than the 'Slow' edge rate setting.

Through changing the edge rate from ‘Fast’ to ‘Slow at a drive strength setting of ‘16mA’ and ‘2mA’, the highest average level of change to peak emissions recorded from the LVCMOS15 I/O standard with a reduction of more than -1.9973dB with a maximum drive strength setting of ‘2mA’. The greatest maxima seen from the comparison plots within the LVCMOS15 standard is approximately 12.36dB, with a drive strength setting of 16mA. This translates as the point where emissions produced from the ‘Fast’ edge rate setting are higher than the ‘Slow’ edge rate setting.

Through changing the edge rate from ‘Fast’ to ‘Slow at a drive strength setting of ‘12mA’ and ‘2mA’, the highest average level of change to peak emissions recorded from the LVCMOS12 I/O standard with a reduction of more than -2.306dB with a maximum drive strength setting of ‘2mA’. The greatest maxima seen from the comparison plots within the LVCMOS12 standard is approximately 9.98dB, with a drive strength setting of 2mA. This translates as the point where emissions produced from the ‘Fast’ edge rate setting are higher than the ‘Slow’ edge rate setting.

Whilst this testing has not returned a rule of thumb for the change to the level of emissions that varying the edge rate will produce, it has identified through changing the edge rate the maximum increase to emissions between settings is a maxima of 14.17dB between particular frequencies. The greatest average delta is seen with the LVCMOS12 logic standard setting and a drive strength of 2mA. The edge rate does appear to have more of an impact when using drive strengths at the lower end of their respective capabilities. As a result of this it can been concluded that the peak level of emissions produced is influenced by the changing of the edge rate setting and that the magnitude of this change is heavily influenced by the drive strength setting of the respective I/O buffer.

6 Radiated Emissions Reference Levels

Section 6 contains an overview of the average peak harmonic levels recorded throughout the radiated emissions testing for each of the I/O driver settings grouped by their logic standard. From the peak harmonics recorded for each I/O driver setting the mean has been taken to give a quantifiable level of emissions for a particular I/O driver setting. All emissions traces obtained for this testing are located in appendix 4.

6.1 Testing Overview

The radiated emissions for each of the driver settings has been recorded and the peaks of each harmonics obtained. In order to identify a quantifiable increase or reduction to the level of emissions produced from a particular I/O driver setting the average of the peaks for each level has been calculated and this is what has been used for this comparison. To establish a baseline for this testing to quantify an increase or in each I/O standard the drive strength setting of 12mA and an edge rate of 'Fast' has been set as the point to compare against within each logic standard.

6.1.1 LVTTL Emissions Overview

Driver Setting	LVTTL Average of Peak Harmonic Level dBµV	Delta dB
LVTTL-24mA-Fast	-59.9919	1.4819
LVTTL-24mA-Slow	-60.4249	1.0489
LVTTL-16mA-Fast	-60.5901	0.8837
LVTTL-16mA-Slow	-62.7485	-1.2747
LVTTL-12mA-Fast	-61.4738	0
LVTTL-12mA-Slow	-64.2944	-2.8206
LVTTL-8mA-Fast	-62.7774	-1.3036
LVTTL-8mA-Slow	-65.7867	-4.3129
LVTTL-6mA-Fast	-68.2449	-6.7711
LVTTL-6mA-Slow	-70.2474	-8.7736
LVTTL-4mA-Fast	-69.5009	-8.0271
LVTTL-4mA-Slow	-71.6628	-10.189
LVTTL-2mA-Fast	-72.6039	-11.1301
LVTTL-2mA-Slow	-73.8976	-12.4238

Table 32: LVTTL Emissions Overview

From the baseline average of -61.47dBµV obtained from the LVTTL-12mA-Fast driver setting it is possible to cause an increase of approximately 1.5dBµV to the peak level of emissions produced or reduce this by approximately -12.5dBµV.

6.1.2 LVCMOS33 Emissions Overview

Driver Setting	LVCMOS33 Average of Peak Harmonic Level dBµV	Delta dB
LVCMOS33-24mA-Fast	-63.7553	1.4032
LVCMOS33-24mA-Slow	-64.8541	0.3044
LVCMOS33-16mA-Fast	-64.4566	0.7019
LVCMOS33-16mA-Slow	-65.3392	-0.1807
LVCMOS33-12mA-Fast	-65.1585	0
LVCMOS33-12mA-Slow	-67.4423	-2.2838
LVCMOS33-8mA-Fast	-66.3082	-1.1497
LVCMOS33-8mA-Slow	-68.9713	-3.8128
LVCMOS33-6mA-Fast	-68.6833	-3.5248
LVCMOS33-6mA-Slow	-69.2096	-4.0511
LVCMOS33-4mA-Fast	-69.5231	-4.3646
LVCMOS33-4mA-Slow	-70.5716	-5.4131
LVCMOS33-2mA-Fast	-72.0851	-6.9266
LVCMOS33-2mA-Slow	-73.3359	-8.1774

Table 33: LVCMOS33 Emissions Overview

From the baseline average of -65.15dBµV obtained from the LVCMOS33-12mA-Fast driver setting it is possible to cause an increase of approximately 1.4dBµV to the peak level of emissions produced or reduce this by approximately -8.17dBµV.

6.1.3 LVCMOS25 Emissions Overview

Driver Setting	LVCMOS25 Average of Peak Harmonic Level dBµV	Delta dB
LVCMOS25-24mA-Fast	-63.4778	1.5681
LVCMOS25-24mA-Slow	-64.6782	0.3677
LVCMOS25-16mA-Fast	-65.1675	-0.1216
LVCMOS25-16mA-Slow	-65.2962	-0.2503
LVCMOS25-12mA-Fast	-65.0459	0
LVCMOS25-12mA-Slow	-66.1547	-1.1088
LVCMOS25-8mA-Fast	-66.2582	-1.2123
LVCMOS25-8mA-Slow	-68.5519	-3.506
LVCMOS25-6mA-Fast	-67.3227	-2.2768
LVCMOS25-6mA-Slow	-68.9214	-3.8755
LVCMOS25-4mA-Fast	-69.0062	-3.9603
LVCMOS25-4mA-Slow	-70.7144	-5.6685
LVCMOS25-2mA-Fast	-72.0572	-7.0113
LVCMOS25-2mA-Slow	-72.6679	-7.622

Table 34: LVCMOS25 Emissions Overview

From the baseline average of -65.04dBµV obtained from the LVCMOS25-12mA-Fast driver setting it is possible to cause an increase of approximately 1.56dBµV to the peak level of emissions produced or reduce this by approximately -7.62dBµV.

6.1.4 LVCMOS18 Emissions Overview

Driver Setting	LVCMOS18 Average of Peak Harmonic Level dBµV	Delta dB
LVCMOS18-24mA-Fast	-62.9278	1.5611
LVCMOS18-24mA-Slow	-64.1558	0.3331
LVCMOS18-16mA-Fast	-63.8729	0.616
LVCMOS18-16mA-Slow	-66.5671	-2.0782
LVCMOS18-12mA-Fast	-64.4889	0
LVCMOS18-12mA-Slow	-66.2571	-1.7682
LVCMOS18-8mA-Fast	-66.2304	-1.7415
LVCMOS18-8mA-Slow	-68.0241	-3.5352
LVCMOS18-6mA-Fast	-67.583	-3.0941
LVCMOS18-6mA-Slow	-68.9543	-4.4654
LVCMOS18-4mA-Fast	-69.1953	-4.7064
LVCMOS18-4mA-Slow	-70.4473	-5.9584
LVCMOS18-2mA-Fast	-72.7413	-8.2524
LVCMOS18-2mA-Slow	-73.7525	-9.2636

Table 35: LVCMOS18 Emissions Overview

From the baseline average of -64.48dBµV obtained from the LVCMOS18-12mA-Fast driver setting it is possible to cause an increase of approximately 1.56dBµV to the peak level of emissions produced, or reduce this by approximately -9.26dBµV.

6.1.5 LVCMOS15 Emissions Overview

Driver Setting	LVCMOS15 Average of Peak Harmonic Level dBµV	Delta dB
LVCMOS15-12mA-Fast	-65.9496	0
LVCMOS15-12mA-Slow	-67.6404	-1.6908
LVCMOS15-8mA-Fast	-68.0284	-2.0788
LVCMOS15-8mA-Slow	-68.9592	-3.0096
LVCMOS15-6mA-Fast	-68.9168	-2.9672
LVCMOS15-6mA-Slow	-70.3969	-4.4473
LVCMOS15-4mA-Fast	-70.2876	-4.338
LVCMOS15-4mA-Slow	-72.0614	-6.1118
LVCMOS15-2mA-Fast	-74.4882	-8.5386
LVCMOS15-2mA-Slow	-74.6304	-8.6808

Table 36: LVCMOS15 Emissions Overview

From the baseline average of -65.94dBµV obtained from the LVCMOS15-12mA-Fast driver setting it is only possible to lower the drive strength setting as the maximum drive strength available is 12mA for this logic standard. The maximum reduction to emissions possible within the LVCMOS12 standard is approximately -8.68dBµV.

6.1.6 LVCMOS12 Emissions Overview

Driver Setting	LVCMOS12 Average of Peak Harmonic Level dBµV	Delta dB
LVCMOS12-12mA-Fast	-65.3499	0
LVCMOS12-12mA-Slow	-67.6404	-2.2905
LVCMOS12-8mA-Fast	-65.3281	0.0218
LVCMOS12-8mA-Slow	-67.0799	-1.73
LVCMOS12-6mA-Fast	-66.1517	-0.8018
LVCMOS12-6mA-Slow	-67.691	-2.3411
LVCMOS12-4mA-Fast	-68.27	-2.9201
LVCMOS12-4mA-Slow	-69.3286	-3.9787
LVCMOS12-2mA-Fast	-72.0559	-6.706
LVCMOS12-2mA-Slow	-73.2297	-7.8798

Table 37: LVCMOS15 Emissions Overview

From the baseline average of -65.94dBµV obtained from the LVCMOS15-12mA-Fast driver setting it is only possible to lower the drive strength setting as the maximum drive strength available is 12mA for this logic standard. The maximum reduction to emissions possible within the LVCMOS12 standard is approximately -8.68dBµV.

7 Conclusions

This research projects asks the question of how varying the I/O standards and attributes within a Spartan-6 FPGA impacts the radiated emissions spectrum. The results recorded within this research provide a quantifiable reference to the level of EMI produced under the various I/O driver settings available within the Spartan-6 FPGA. Of the logic standards and driver settings tested the LVTTL has proven to be the biggest contributor to the level EMI produced throughout the project. The results gained from the Spartan-6 FPGA are comparable to the wide variety of FPGAs that are available on the market as they all contain I/O drivers of the same standard and have similar drive strength and edge rate capabilities that have been covered within this research.

The frequency domain behaviour of the practical and theoretical traces recorded within section 3.2.3 gives an accurate indication of how the theoretical behaviour deviates from the practically obtained results. The results gained from section 3.3.3 deviate significantly due to errors within the MATLAB code and the theoretical signals produced for the comparison. The same deviations occur within sections 4.3.2 and 4.3.4, a more accurate method of analysis is required to incorporate the behaviour of such effects as a filer circuit in series with the signal path. Solely relying on Equation 1 is not an accurate enough method to predict how the behaviour of a periodic signal will present itself within the frequency domain.

Comparing the level of EMI produced across the individual I/O driver settings, the results have delivered an overview of how they can impact the levels of emissions produced. The logic standard testing has shown that the increase to emissions is approximately 3dB when implementing a design around the LVTTL logic standard. When comparing the plots individually a maxima of 16.8dB was observed between two logic standard settings when comparing the LVTTL standard to the LVCMOS15 standard. The LVCMOS standards produced a similar level of emissions during testing and the only immediate drawback would be implementing a design around the LVTTL standard. The results gained from the drive strength testing has shown that again the LVTTL standard produces the peak level of emissions and a reduction of approximately 13.19dB from the maximum to minimum drive strength setting. The LVCMOS standards all produced a similar level of peak level emissions, with the exception of the LVCMOS12 standard that has a limitation to its drive strength of 12mA. The highest range seen from the LVCMOS standards throughout the maximum to minim drive strength settings was 9.16dB, recorded from the LVCMOS25 logic standard. From this it is reasonable to conclude that the LVTTL produces a higher average of peak emissions and basing a design around the LVCMOS standard will reduce the peak emissions on average by 4dB across the observed spectrum. The results gained from the edge rate testing has shown that in more cases the highest average reduction to peak level emissions was seen when varying the edge rate with a 2mA drive setting and the lower logic levels. The highest average reduction to peak level emissions of -2.306dB was seen when varying the edge from ‘fast’ to ‘slow’ with a drive strength of 2mA and the LVCMOS12 logic standard.

Considering the results detailed within section 6, it is hoped that this will provide a reference to any designer as to the average levels of emissions produced by the FPGA under the various I/O driver settings. The LVTTL standard shows a reduction of peak level emissions on average of 13.9dB from the 'LVTTL-24-Fast' to 'LVTTL-2-Slow' I/O driver settings. The LVCMOS33 logic standard shows a reduction of peak level emissions on average of 12.2dB from the 'LVCMOS33-24-Fast' to 'LVCMOS33-2-Slow' I/O driver settings. From all of the logic standards examined these two are the only 3.3 volt logic standard used and are the more comparable, this shows that a reduction of almost 2dB is seen by electing to use the LVCMOS33 over the LVTTL standard. The LVCMOS25 shows a reduction of peak level emissions on average of 9.19dB from the 'LVCMOS25-24-Fast' to 'LVCMOS25-2-Slow' I/O driver settings. The LVCMOS18 shows a reduction of peak level emissions on average of 10.7dB from the 'LVCMOS18-24-Fast' to 'LVCMOS18-2-Slow' I/O driver settings. The LVCMOS15 shows a reduction of peak level emissions on average of 8.6dB from the 'LVCMOS15-24-Fast' to 'LVCMOS15-2-Slow' I/O driver settings. The LVCMOS12 shows a reduction of peak level emissions on average of 7.8dB from the 'LVCMOS12-24-Fast' to 'LVCMOS12-2-Slow' I/O driver settings. These average levels combined with the plots included within appendix 4 will hopefully serve as a useful tool when designing any new circuit or system that includes a device of this nature.

It was informative to see how the practical signals produced by the FPGA vary from what is expected from theoretical analysis and how component values impact the time and frequency domain representations of a signal. This further supports the notion that an accurate L-C-R model is a vital component of high speed circuit design. The introduction of oscillations were observed within the driver settings using the upper limit of drive strength and fast edge rates which introduces additional harmonics to the frequency spectrum. Contrasting this to the signals produced from drivers that had a drive strength at the lower end of their capabilities, i.e. 2mA, illustrated significant rounding of the transitional edges of the signal. From this it would be feasible to expect timing issues from the variations to these signals based entirely on the buffer setting.

The research detailed within this thesis focusses on near field emissions measurements to determine the level of EMI in dBµV under the various I/O driver settings. It would be pertinent in further research to examine emissions with the far field either in an anechoic chamber or an open area test site to look at the potential emissions to surrounding circuits and systems. Secondly using a near field probe and based on the emissions results gained within this research it would be possible to calculate and plot the near field in A/m^2 (amperes per square metre). This would allow for the characteristics of the magnetic field to be simulated and used during the design phases and within future research projects. Furthermore it would be possible to map out all of the noise sources present on the MSCR-001 PCB and extrapolate this to reflect the far field measurements to give an indication of the far field behaviour of the FPGA. What this research has shown is the potential impact that changing any of the I/O driver attributes can potentially have on a circuit or system and it is the hope that this research can be another step towards quantifying the EMC performance of ICs.

7.1 Further Research

The possibilities for further research based on the findings within this thesis would be to establish a wider picture of how the I/O standards and attributes can impact the radiated emissions spectrum, and other influences that an FPGA has on the EMC performance of the circuits and system that they are included within. The intention behind this research was to contribute towards the road map of the EMC performance of integrated circuits.

Initially, should this project be expanded upon then it would be pertinent to extrapolate the results obtained within the near field and establish how this translates to the electric field that would be obtained in far field measurements. This project focuses on the peak levels of emissions that have been recorded at a given fixed point and not the surrounding field. This would give the designer the opportunity to model what the electric field would be and the potential impact that the FPGA has on surrounding circuits and systems and not just the surrounding circuitry on the PCB.

Although the CMOS & bipolar I/O standards found in the Spartan-6 FPGA are common across the FPGAs that are available on the market, the drive strength and logic levels of the respective I/O standards does vary. It would be pertinent to investigate the behaviour of FPGAs of different models and different manufactures such as Altera, Atmel, Microsemi etc. This would either confirm that the I/O standards under a fixed configuration will produce a similar 'peak level' of emissions or whether this varies between FPGA models and manufacturers.

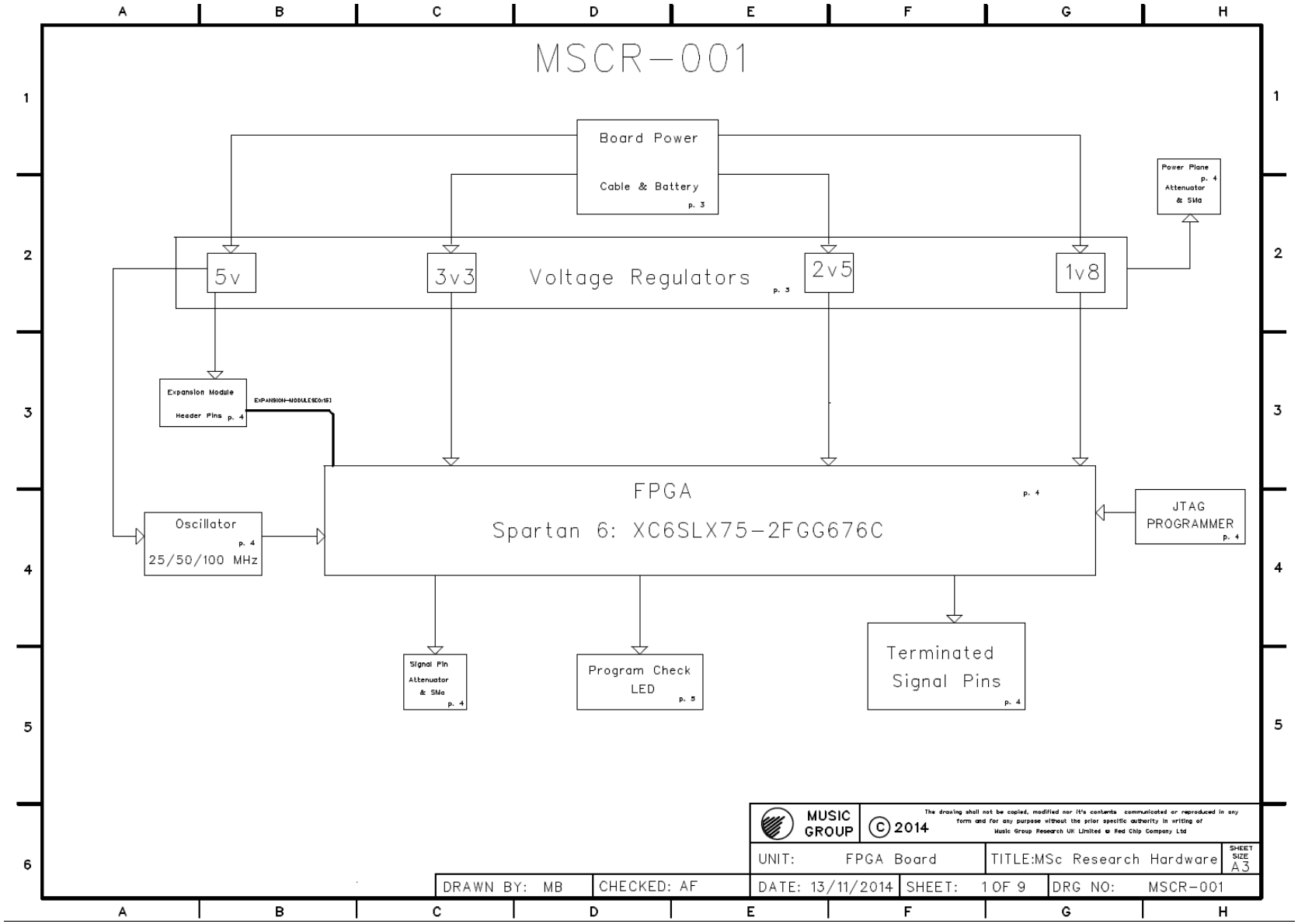
Another area for further research would be to investigate the noise produced on the power and ground planes as a result of utilising a particular I/O standard, drive strength or edge rate. In applications such as professional audio the integrity of the power and ground planes are seen as being vital to producing acceptable audio. If utilising a particular I/O standard, drive strength or edge rate of a FPGAs I/O introduces additional noise into a circuit or system then a designer needs to be aware of this. Noise on the power and ground planes can corrupt on board memory or make cause fluctuations on power rails.

Appendix

Below outlines the contents of the appendix in support of this thesis.

- Appendix A1 – MSCR-001 Schematics
- Appendix A2 – MSCR-001 GERBER files
- Appendix A3 – VHDL Code
- Appendix A4 – Peak Detect MATLAB Code
- Appendix A5 – Q-Fit MATLAB Code
- Appendix A6 – Results Processing MATLAB Code
- Appendix A7 – UCF File

Appendix A1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Power Plane
p. 4
Attenuator
& SMa
5v
3v3
Voltage Regulators
p. 3
2v5
1v8
Expansion Module
Header Pins p. 4
EXPANSION-MODULESCON1
FPGA
p. 4
Spartan 6: XC6SLX75-2FGG676C
JTAG
PROGRAMMER
p. 4
Oscillator
p. 4
25/50/100 MHz
Signal Pin
Attenuator
& SMa
p. 4
Program Check
LED
p. 5
Terminated
Signal Pins
p. 4
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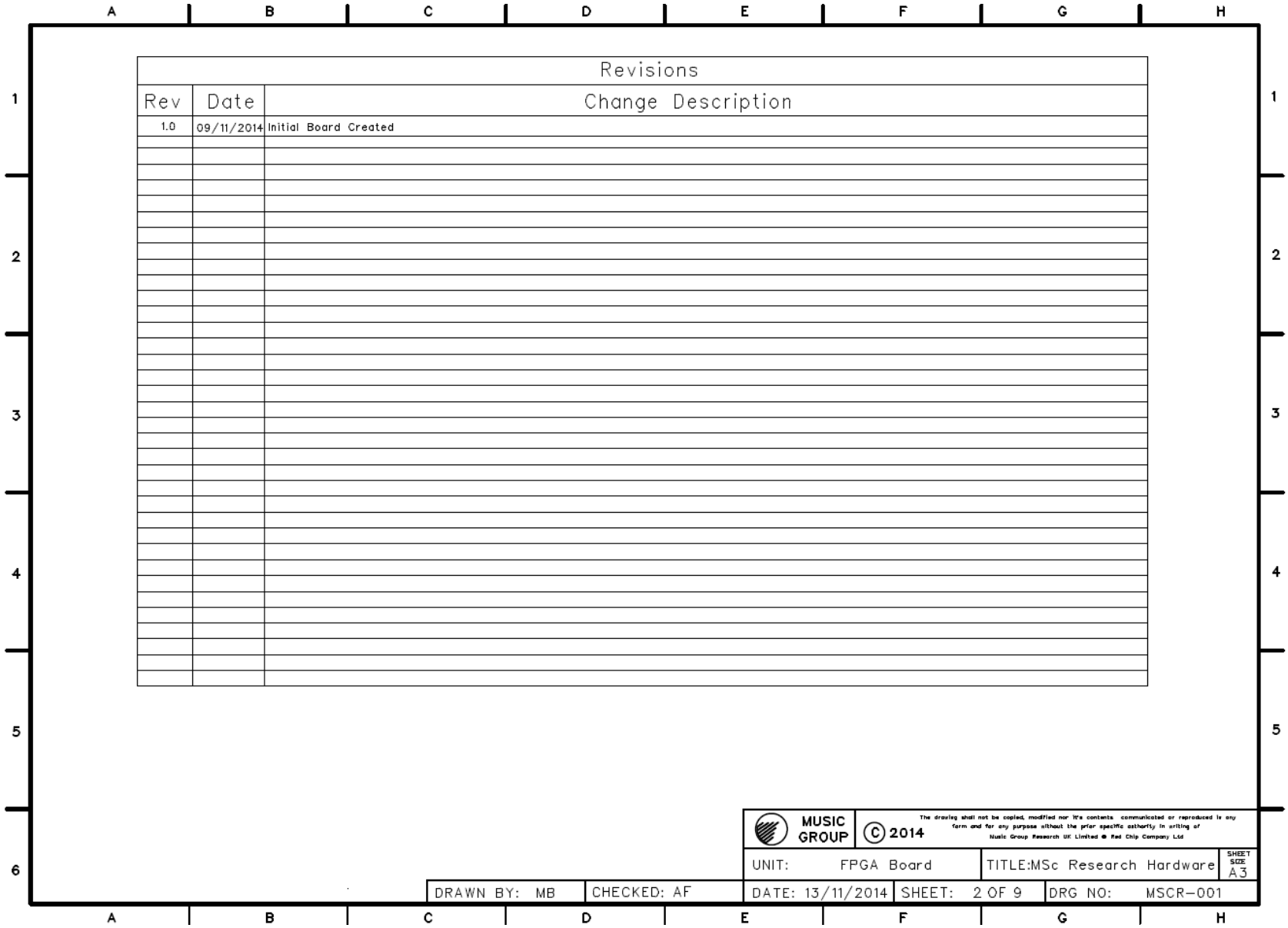
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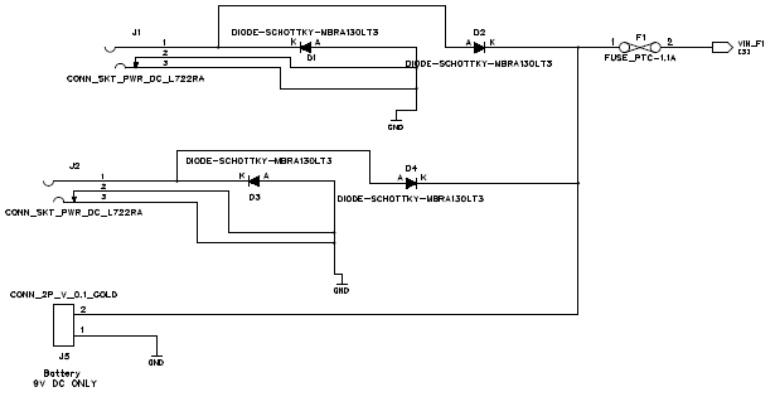
External Supply

External +12V Power Supply



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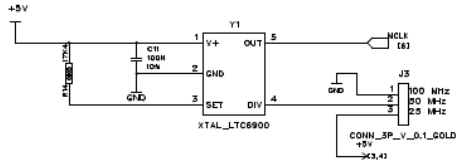

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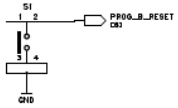

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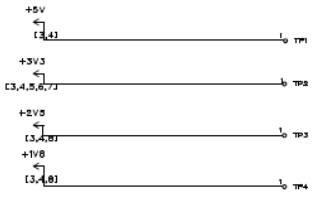

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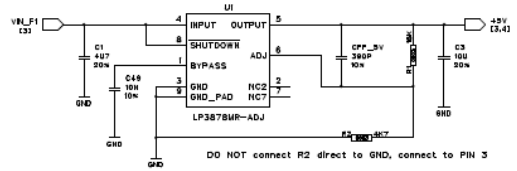

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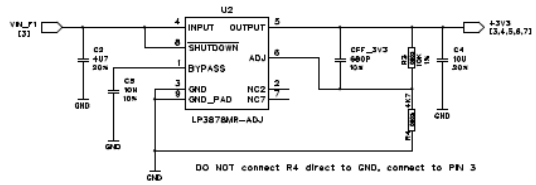

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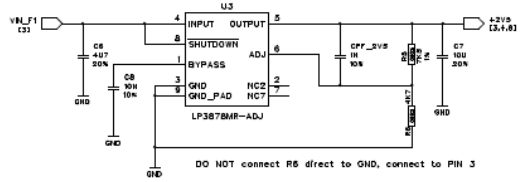

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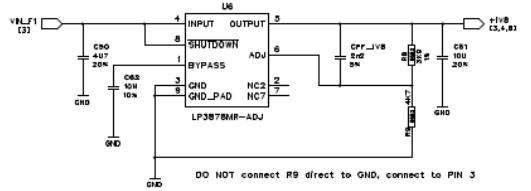

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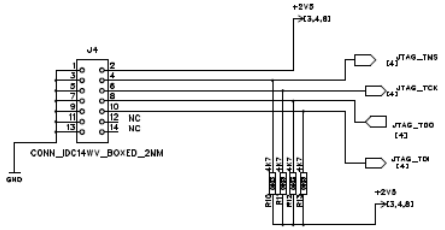

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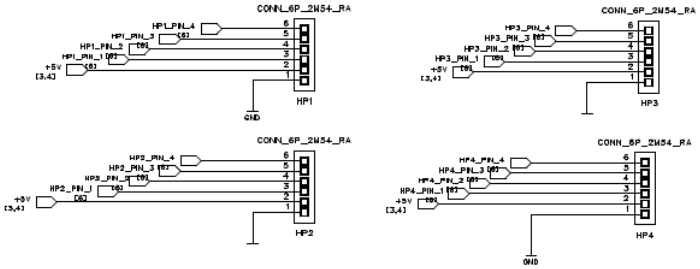

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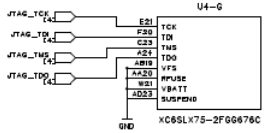

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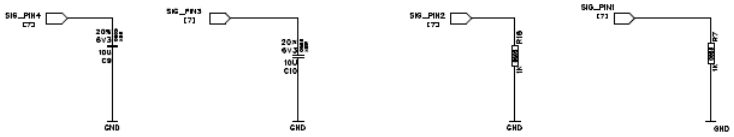

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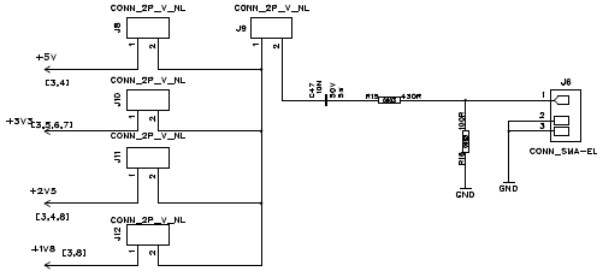

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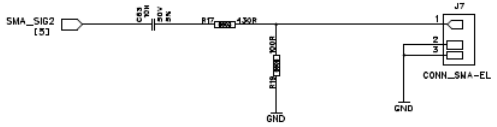

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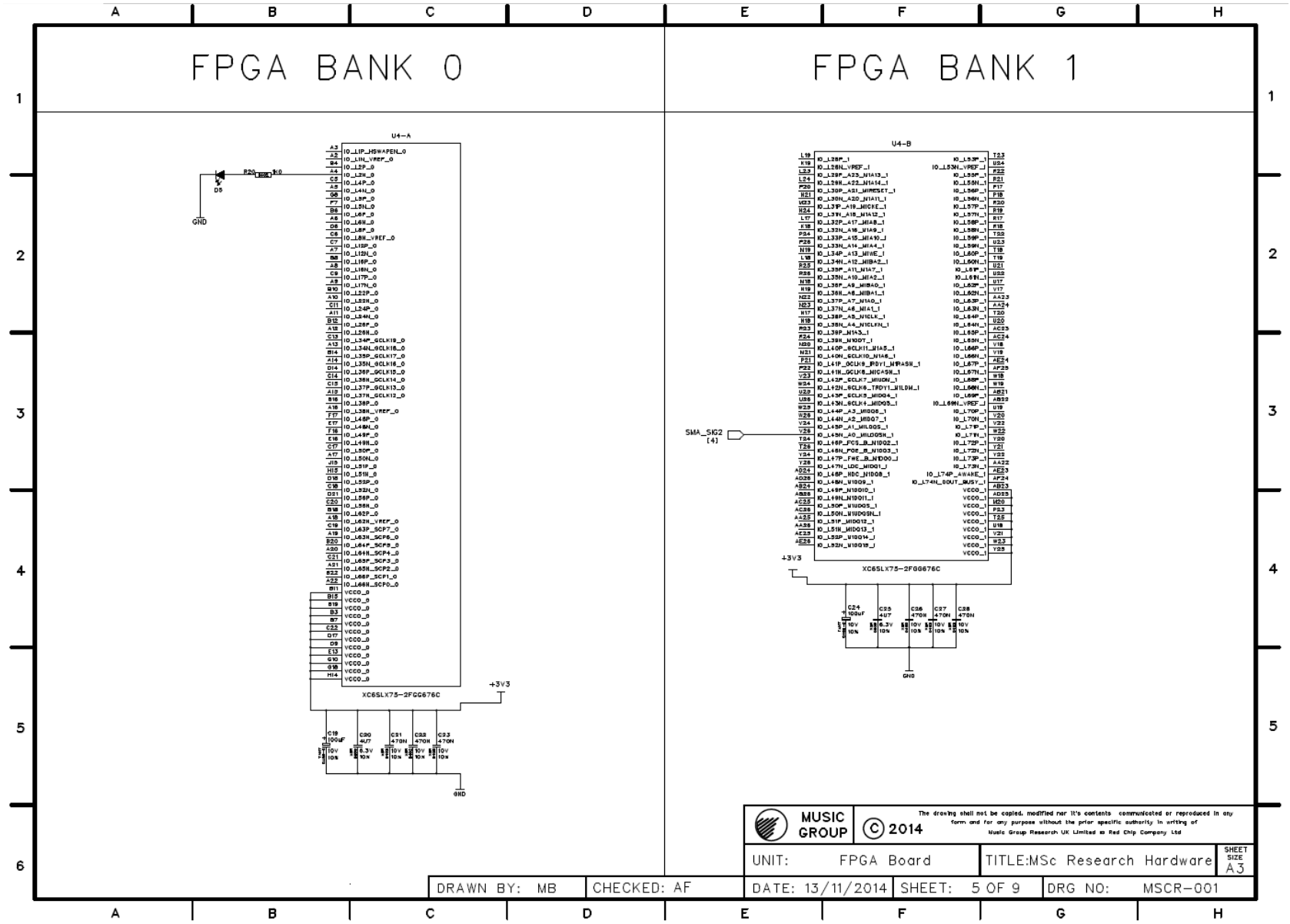
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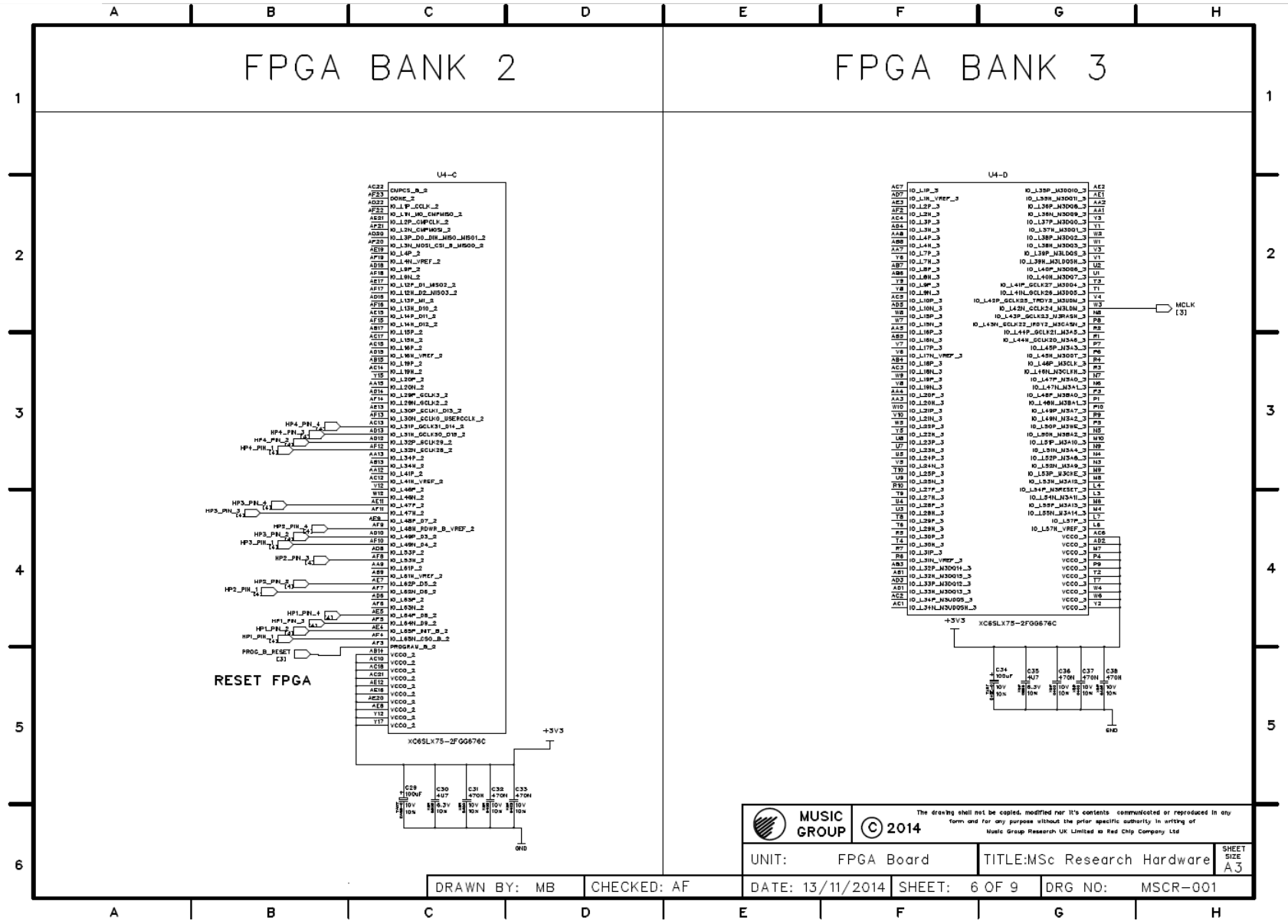
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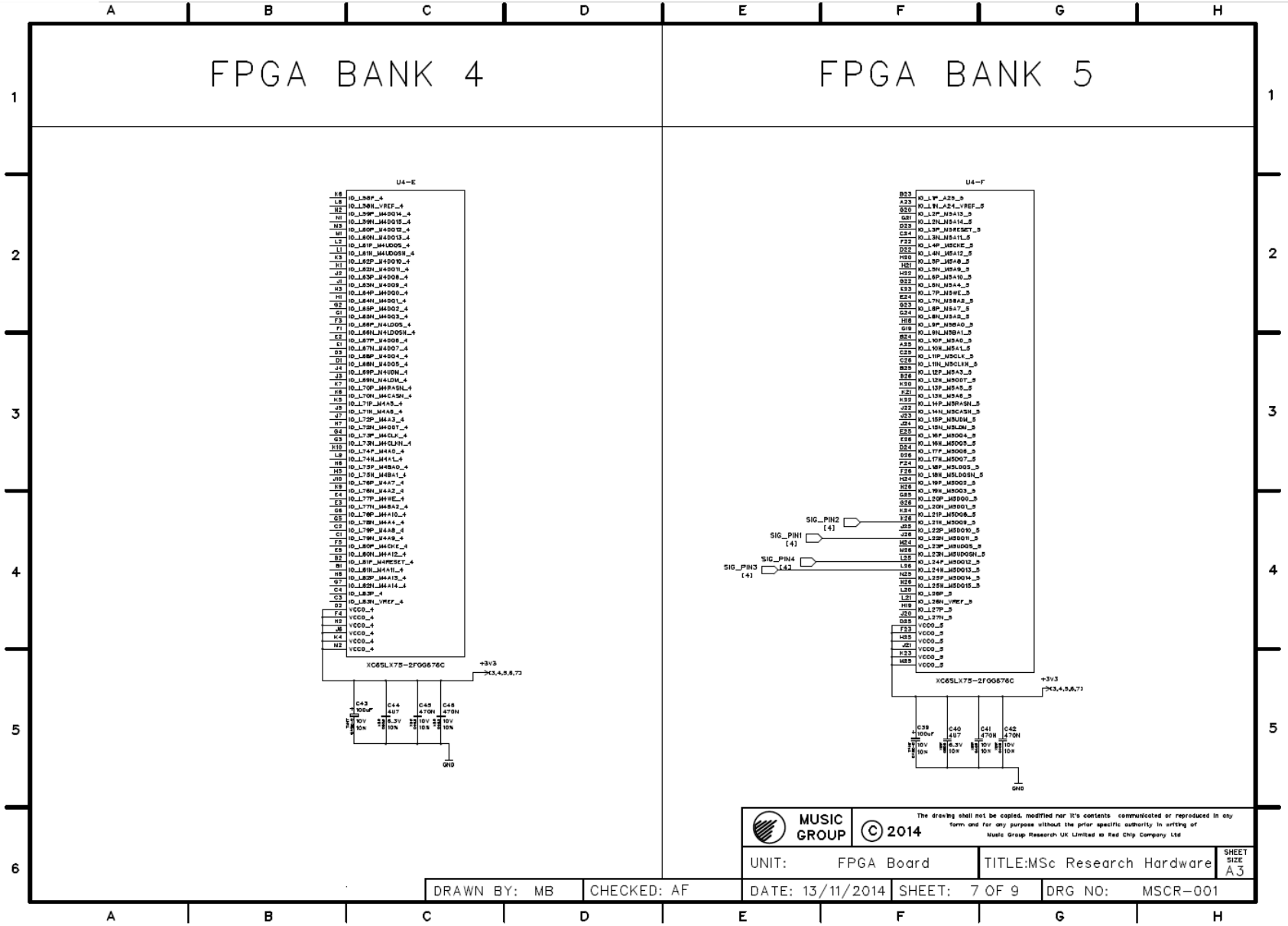
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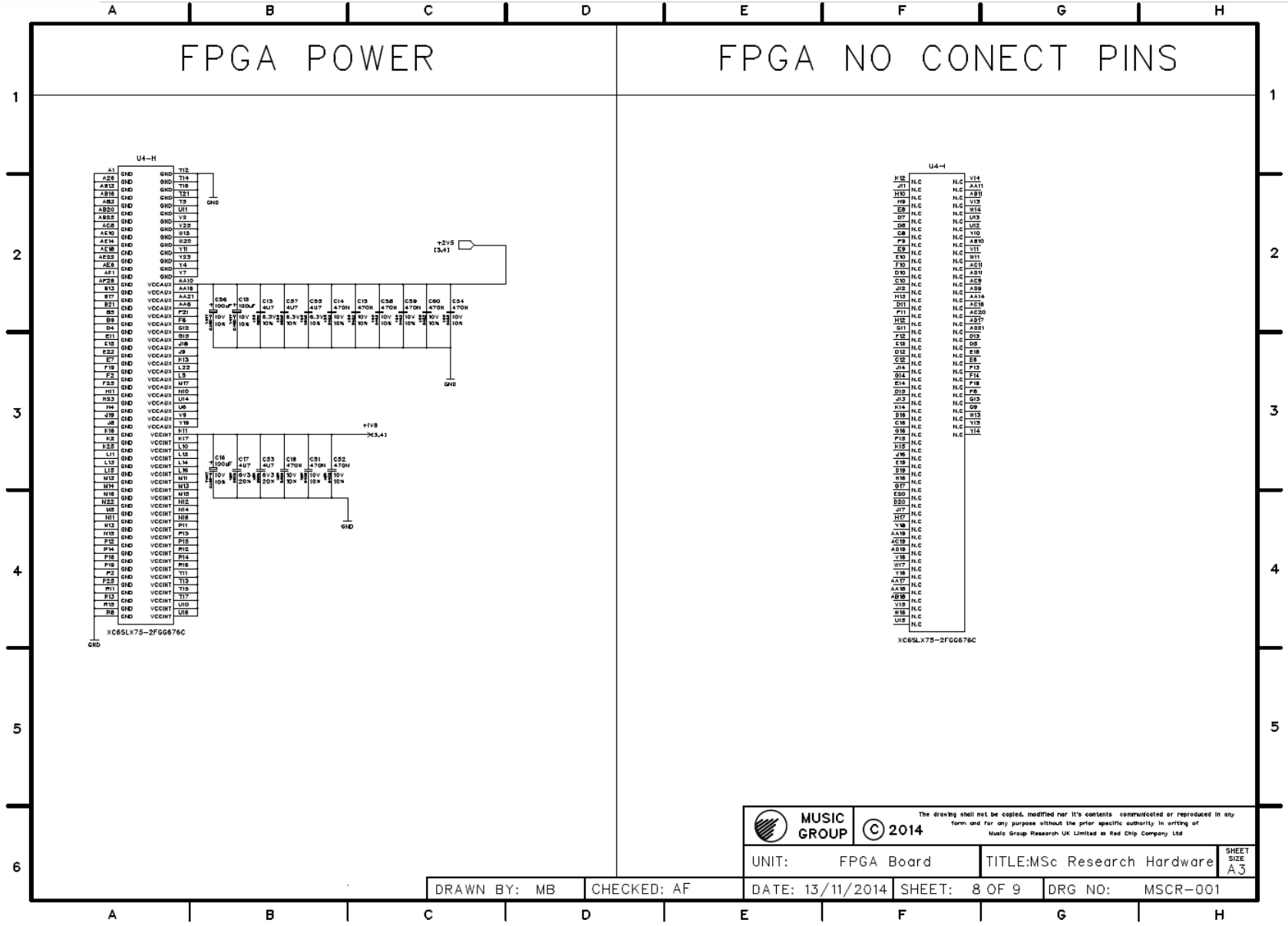
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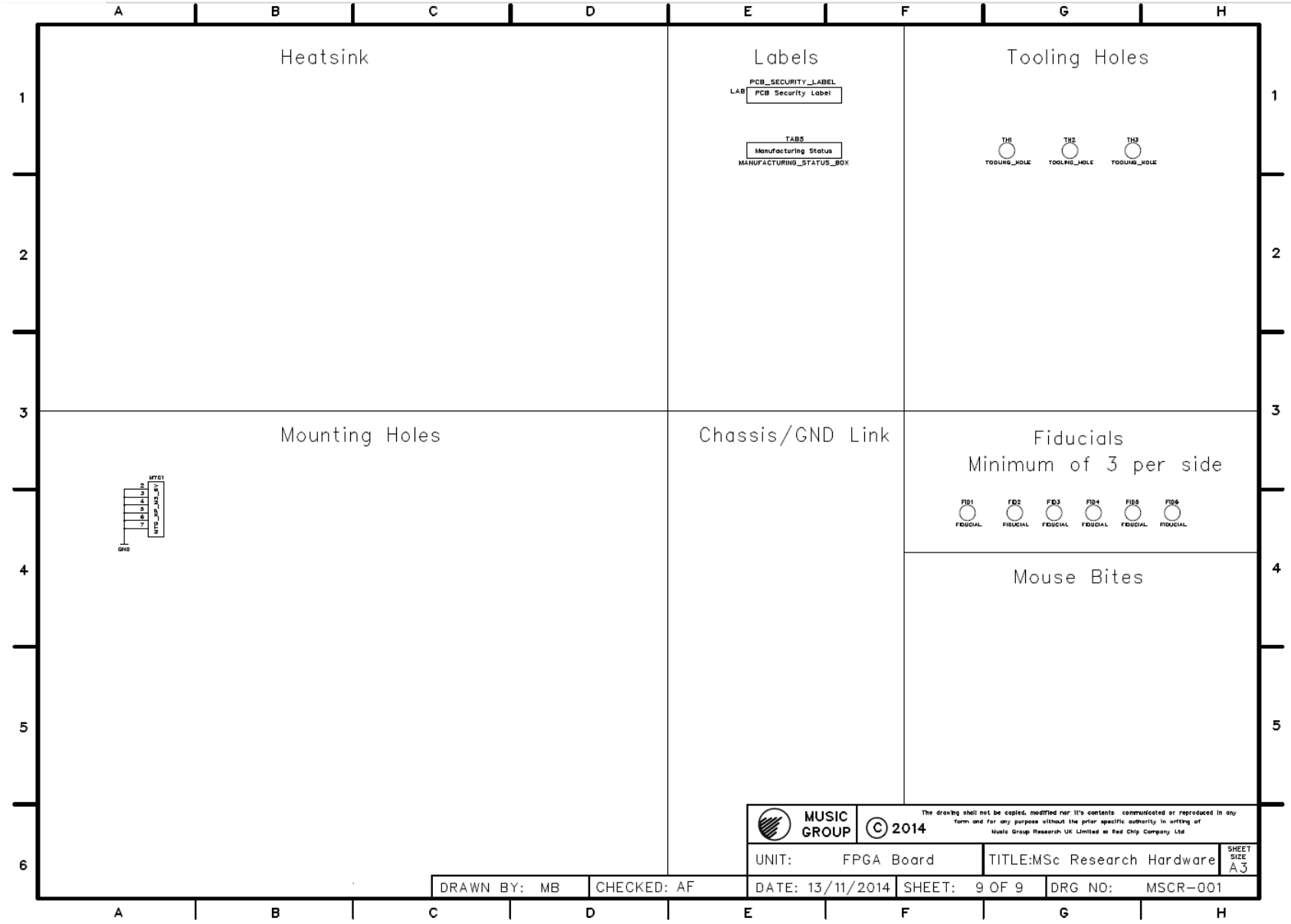
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Chassis/GND Link
Fiducials
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FID1
FIDUCIAL
FID2
FIDUCIAL
FID3
FIDUCIAL
FID4
FIDUCIAL
FID5
FIDUCIAL
FID6
FIDUCIAL
Mouse Bites
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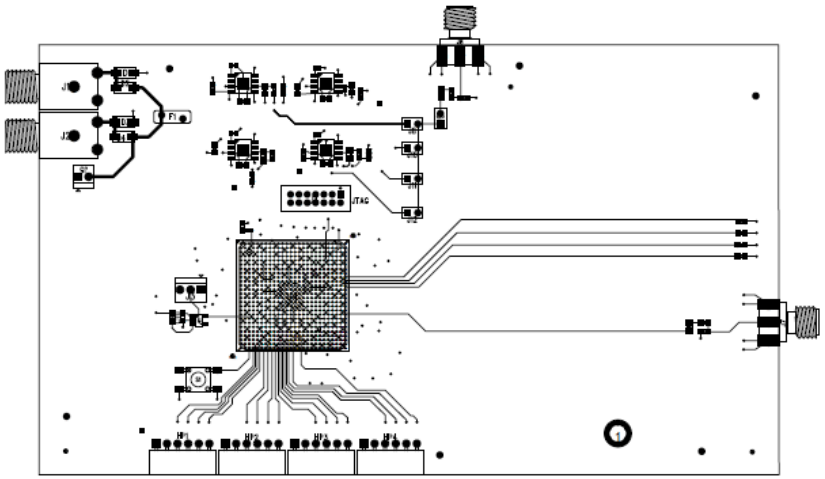
UNIT: FPGA Board
TITLE:MSc Research Hardware
SHEET SIZE A3
DRAWN BY: MB
CHECKED: AF
DATE: 13/11/2014
SHEET: 9 OF 9
DRG NO: MSCR-001

Appendix A2

A3



Component Side			
UNIT: DN9610			
TITLE: AES50 REPEATER	DRAWN: SW	DATE: 02-05-12	CAD LAYER 1
BOARD No. 3190 BOARD Iss. B	CHECKED:	SHEET Iss: B	DRG No. PCK9610-3190-B.PCB

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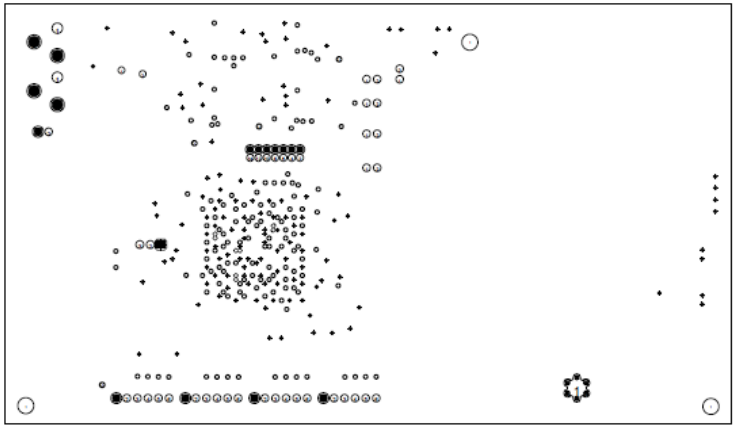
A3



UNIT: DN9610				
TITLE: AES50 REPEATER		DRAWN: SW	DATE: 02-05-12	CAD LAYER 2
BOARD No. 3190	BOARD Iss. B	CHECKED:	SHEET Iss: B	DRG No.PCK9610-3190-B.PCB

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UNIT: DN9610			
TITLE: AES50 REPEATER	DRAWN: SW	DATE: 02-05-12	CAD LAYER
BOARD No. 3190 BOARD Iss. B	CHECKED:	SHEET Iss: B	DRG No.PCK9610-3190-B.PCB

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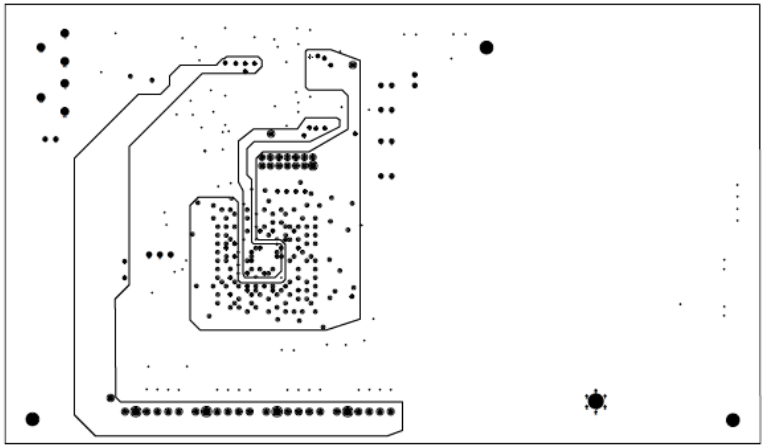

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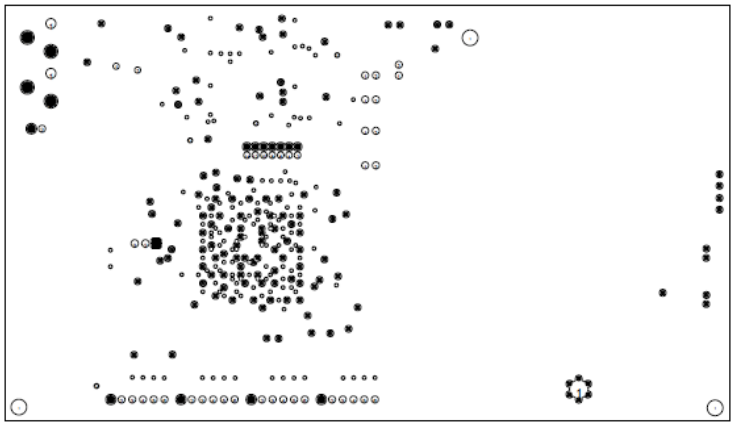
TITLE: AES50 REPEATER	DRAWN: SW	DATE: 02-05-12	CAD LAYER
BOARD No. 3190 BOARD Iss. B	CHECKED:	SHEET Iss: B	DRG No.PCK9610-3190-B.PCB

A3



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BOARD No. 3190	BOARD Iss. B	CHECKED:	SHEET Iss: B	DRG No. PCK9610-3190-B.PCB

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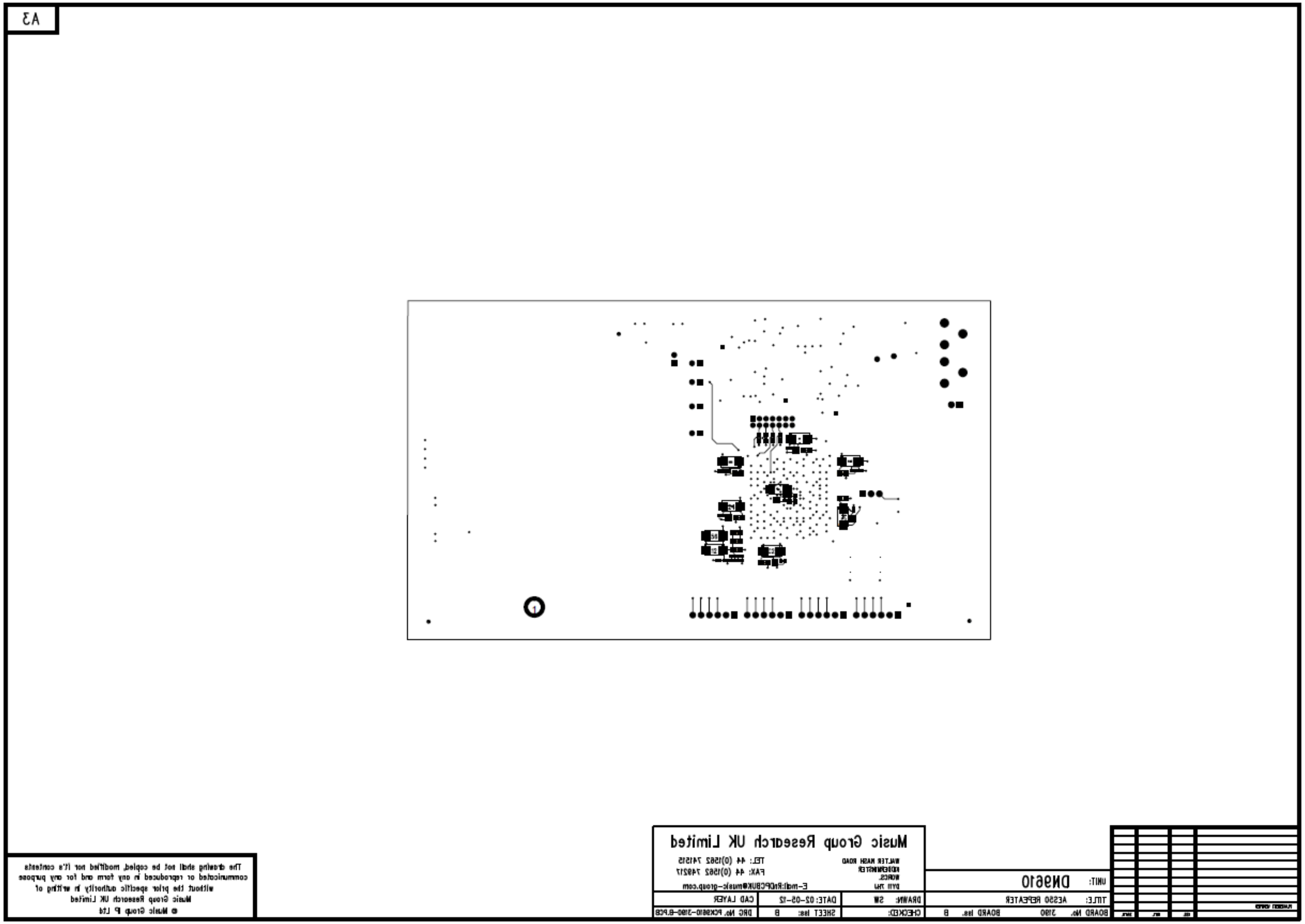
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Music Group Research UK Limited
E-mail:RnDPCBUK@music-group.com
UNIT: DN9610
TITLE: AES50 REPEATER
DRAWN: SW
DATE: 02-05-12
CAD LAYER
BOARD No. 3190
BOARD Iss. B
CHECKED:
SHEET Iss: B
DRG No. PCK9610-3190-B.PCB
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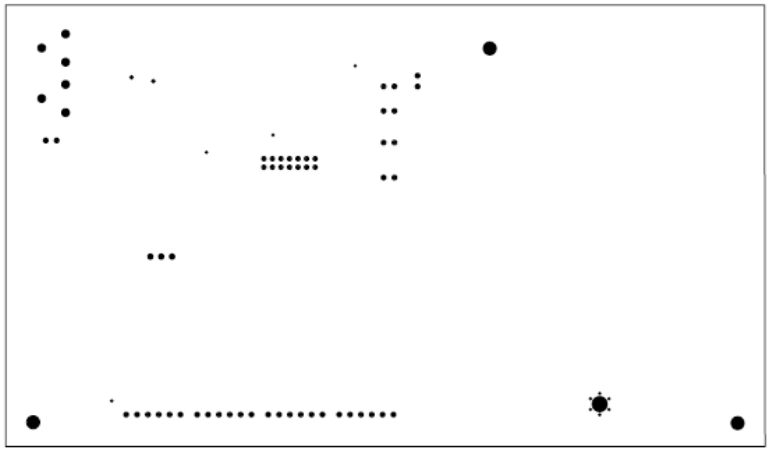

Drill Drawing

UNIT: DN9610

TITLE: AES50 REPEATER

BOARD No. 3190 BOARD Iss. B

CHECKED:

DRAWN: SW | DATE: 02-05-12 | CAD LAYER 24

SHEET Iss: B | DRG No.PCK9610-3190-B.PCB

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Appendix A3

```
1 ----------------------------------------------------------------------------------
2 -- Company:
3 -- Engineer: Mark Boden
4 --
5 -- Create Date: 13:00:10 07/20/2015
6 -- Design Name: MSCR-001 PCB Code
7 -- Module Name: Main_Code - Behavioral
8 -- Project Name: Master of Sceience (Research)
9 -- Target Devices: Spartan 6 FPGA
10 -- Tool versions:
11 -- Description:
12 --
13 -- Dependencies:
14 --
15 -- Revision:
16 -- Revision 0.01 - File Created
17 -- Additional Comments:
18 --
19 ----------------------------------------------------------------------------------
20 library IEEE;
21 use IEEE.STD_LOGIC_1164.ALL;
22 use IEEE.NUMERIC_STD.ALL;
23 library UNISIM;
24 use UNISIM.VComponents.all;
25
26 entity Main_Code is
27 Port ( MCLK : in std_logic; -- MCLK Input from External Oscillator
28 HP1_PIN_1 : inout std_logic; -- Header Socket 1 (Pin 1)
29 -- HP2_PIN_1 : out std_logic; -- Header Socket 2 (Pin 2)
30 -- HP2_PIN_2 : out std_logic; -- Header Socket 3 (Pin 3)
31 -- HP2_PIN_3 : out std_logic; -- Header Socket 4 (Pin 4)
32 -- HP2_PIN_4 : out std_logic; -- Header Pin 2 (1-4)
33 SMA_SIG2 : out std_logic; -- SMA Output
34 TRACE_1 : out std_logic); -- PCB Trace 1 with 50R Termination.
35 -- TRACE_2 : out std_logic; -- PCB Trace 2 with 50R Termination.
36 -- TRACE_3 : out std_logic; -- PCB Trace 3 with Capacitive Termination.
37 -- TRACE_4 : out std_logic); -- PCB Trace 4 with Capacitive Termination.
38 end Main_Code;
39
40 architecture Behavioral of Main_Code is
41
42 component FREQ_CHANGE
43 port
44 (-- Clock in ports
45 CLK_IN1 : in std_logic;
46 -- Clock out ports
47 CLK_OUT1 : out std_logic;
48 CLK_OUT2 : out std_logic);
49 end component;
50
51 --Signal Declarations
52
53 signal FIVE_MHz_CLK : std_logic;
54 signal HUNDRED_MHz_CLK : std_logic;
55 signal CLOCK_MUX_OUT : std_logic;
56 signal inv_CLOCK_MUX_OUT : std_logic;
57 signal DDR_OUT : std_logic;
58 signal OBUFT_SMA : std_logic;
59
60 begin
61
62 -- Digital Clock Manager
```

```
63 DCM : FREQ_CHANGE
64 port map
65 (-- Clock in ports
66 CLK_IN1 => MCLK,
67 -- Clock out ports
68 CLK_OUT1 => HUNDRED_MHz_CLK,
69 CLK_OUT2 => FIVE_MHz_CLK);
70
71 -- Clock Multiplexer
72 CLOCK_MUX : BUFGMUX
73 generic map
74 (
75 CLK_SEL_TYPE=> "SYNC" --Glitchles ("SYNC") or fast ("ASYNC")
clock switch-over
76 )
77 port map (
78 O => CLOCK_MUX_OUT, -- 1-bit output: Clock buffer output
79 I0 => FIVE_MHz_CLK, -- 1-bit input: clock buffer input (S=0)
80 I1 => HUNDRED_MHz_CLK, -- 1-bit input: clock buffer input (S=1)
81 S => HP1_PIN_1 -- 1-bit input: clock buffer select
82 );
83 -- Inverted Clock Pulse
84 inv_clock_mux_out <= (NOT CLOCK_MUX_OUT);
85
86 -- Dual Edge Flip-Flop
87 ODDR2_SMA : ODDR2
88 generic map(
89 DDR_ALIGNMENT => "NONE", -- Sets output alignment to "NONE", "C0", "C1"
90 INIT => '0', -- Sets initial state of the Q output to '0' or '1'
91 SRTYPE => "ASYNC") -- Specifies "SYNC" or "ASYNC" set/reset
92 port map (
93 Q => SMA_SIG2, -- 1-bit output data
94 C0 => CLOCK_MUX_OUT, -- 1-bit clock input
95 C1 => (inv_CLOCK_MUX_OUT), -- 1-bit clock input
96 CE => '1', -- 1-bit clock enable input
97 D0 => '1', -- 1-bit data input (associated with C0)
98 D1 => '0' -- 1-bit data input (associated with C1)
99 );
100
101 ---- Dual Edge Flip-Flop
102 --ODDR2_HP2_PIN_1 : ODDR2
103 -- generic map(
104 -- DDR_ALIGNMENT => "NONE", -- Sets output alignment to "NONE", "C0", "C1"
105 -- INIT => '0', -- Sets initial state of the Q output to '0' or '1'
106 -- SRTYPE => "ASYNC") -- Specifies "SYNC" or "ASYNC" set/reset
107 -- port map (
108 -- Q => HP2_PIN_1, -- 1-bit output data
109 -- C0 => CLOCK_MUX_OUT, -- 1-bit clock input
110 -- C1 => (inv_CLOCK_MUX_OUT), -- 1-bit clock input
111 -- CE => '1', -- 1-bit clock enable input
112 -- D0 => '1', -- 1-bit data input (associated with C0)
113 -- D1 => '0' -- 1-bit data input (associated with C1)
114 --);
115 --
116 ---- Dual Edge Flip-Flop
117 --ODDR2_HP2_PIN_2 : ODDR2
118 -- generic map(
119 -- DDR_ALIGNMENT => "NONE", -- Sets output alignment to "NONE", "C0", "C1"
120 -- INIT => '0', -- Sets initial state of the Q output to '0' or '1'
121 -- SRTYPE => "ASYNC") -- Specifies "SYNC" or "ASYNC" set/reset
122 -- port map (
123 -- Q => HP2_PIN_2, -- 1-bit output data
```

```
124 -- C0 => CLOCK_MUX_OUT, -- 1-bit clock input
125 -- C1 => (inv_CLOCK_MUX_OUT), -- 1-bit clock input
126 -- CE => '1', -- 1-bit clock enable input
127 -- D0 => '1', -- 1-bit data input (associated with C0)
128 -- D1 => '0' -- 1-bit data input (associated with C1)
129 --);
130
131 ---- Dual Edge Flip-Flop
132 ODDR2_TRACE_1 : ODDR2
133 generic map(
134 DDR_ALIGNMENT => "NONE", -- Sets output alignment to "NONE", "C0", "C1"
135 INIT => '0', -- Sets initial state of the Q output to '0' or '1'
136 SRTYPE => "ASYNC") -- Specifies "SYNC" or "ASYNC" set/reset
137 port map (
138 Q => TRACE_1, -- 1-bit output data
139 C0 => CLOCK_MUX_OUT, -- 1-bit clock input
140 C1 => (inv_CLOCK_MUX_OUT), -- 1-bit clock input
141 CE => '1', -- 1-bit clock enable input
142 D0 => '1', -- 1-bit data input (associated with C0)
143 D1 => '0' -- 1-bit data input (associated with C1)
144 );
145
146 ---- Dual Edge Flip-Flop
147 --ODDR2_TRACE_2 : ODDR2
148 -- generic map(
149 -- DDR_ALIGNMENT => "NONE", -- Sets output alignment to "NONE", "C0", "C1"
150 -- INIT => '0', -- Sets initial state of the Q output to '0' or '1'
151 -- SRTYPE => "ASYNC") -- Specifies "SYNC" or "ASYNC" set/reset
152 -- port map (
153 -- Q => TRACE_2, -- 1-bit output data
154 -- C0 => CLOCK_MUX_OUT, -- 1-bit clock input
155 -- C1 => (inv_CLOCK_MUX_OUT), -- 1-bit clock input
156 -- CE => '1', -- 1-bit clock enable input
157 -- D0 => '1', -- 1-bit data input (associated with C0)
158 -- D1 => '0' -- 1-bit data input (associated with C1)
159 --);
160 --
161 ---- Dual Edge Flip-Flop
162 --ODDR2_TRACE_3 : ODDR2
163 -- generic map(
164 -- DDR_ALIGNMENT => "NONE", -- Sets output alignment to "NONE", "C0", "C1"
165 -- INIT => '0', -- Sets initial state of the Q output to '0' or '1'
166 -- SRTYPE => "ASYNC") -- Specifies "SYNC" or "ASYNC" set/reset
167 -- port map (
168 -- Q => TRACE_3, -- 1-bit output data
169 -- C0 => CLOCK_MUX_OUT, -- 1-bit clock input
170 -- C1 => (inv_CLOCK_MUX_OUT), -- 1-bit clock input
171 -- CE => '1', -- 1-bit clock enable input
172 -- D0 => '1', -- 1-bit data input (associated with C0)
173 -- D1 => '0' -- 1-bit data input (associated with C1)
174 --);
175 --
176 --
177 ---- Dual Edge Flip-Flop
178 --ODDR2_TRACE_4 : ODDR2
179 -- generic map(
180 -- DDR_ALIGNMENT => "NONE", -- Sets output alignment to "NONE", "C0", "C1"
181 -- INIT => '0', -- Sets initial state of the Q output to '0' or '1'
182 -- SRTYPE => "ASYNC") -- Specifies "SYNC" or "ASYNC" set/reset
183 -- port map (
184 -- Q => TRACE_4, -- 1-bit output data
185 -- C0 => CLOCK_MUX_OUT, -- 1-bit clock input
```

```
186 -- C1 => (inv_CLOCK_MUX_OUT), -- 1-bit clock input
187 -- CE => '1', -- 1-bit clock enable input
188 -- D0 => '1', -- 1-bit data input (associated with C0)
189 -- D1 => '0' -- 1-bit data input (associated with C1)
190 --);
191
192 end Behavioral;
193
194
```

Appendix A4

```
function [pospeakind,negpeakind]=peakdetect(signal)
%% PEAKDETECT peak detection
%
% [pospeakind,negpeakind]=peakdetect(signal)
%
% The positive and negative polarity (concave down and up) peak index vectors are
% generated from the signal vector. Positive and negative
% polarity peaks occur at points of positive to negative and negative to positive
% slope adjacency, respectively. The typically rare contingencies of peaks
% occurring at the lagging edges of constant intervals are supported. Complex
% signals are modified to the modulus of the elements. If unspecified, the signal
% vector is entered after the prompt from the keyboard.
% Implemented using MATLAB 6.0.0
%
% Examples:
%
% » [p,n]=peakdetect([-1 -1 0 1 0 1 0 -1 -1])
%
% p =
%
% 4 6
%
% n =
%
% 1 5 8
%
% » [p,n]=peakdetect(cos(2*pi*(0:999999)/500000))
%
% p =
%
% 1 500001 1000000
%
% n =
%
% 250001 750001
%
% Copyright (c) 2001
% Tom McMurray
% mcmurray@teamcmi.com
% Modified by J F Dawson APr 2006 - plot line changed for octave then disabled
% The function seems to find every peak - too sensitive for noisy data - JFD
%% if signal is not input, enter signal or return for empty outputs
if ~nargin
signal=input('enter signal vector or return for empty outputs\n');
if isempty(signal)
pospeakind=[];
negpeakind=[];
return
end
end
sizsig=size(signal);
%% while signal is unsupported, enter supported signal or return for empty outputs
while isempty(signal)|~isnumeric(signal)|~all(all(isfinite(signal)).)..
|length(sizsig)>2|min(sizsig)~=1
signal=input(['signal is empty, nonnumeric, nonfinite, or nonvector:\nenter .'..
'finite vector or return for empty outputs\n']);
if isempty(signal)
pospeakind=[];
negpeakind=[];
return
end
sizsig=size(signal);
```

```
end
%% if signal is complex, modify to modulus of the elements
if ~isreal(signal)
signal=abs(signal);
end
%% if signal is constant, return empty outputs
if ~any(signal-signal(1))
pospeakind=[];
negpeakind=[];
disp('constant signal graph suppressed')
return
end
sizsig1=sizsig(1);
lensig=sizsig1;
%% if signal is a row vector, modify to a column vector
if lensig==1
signal=signal(:);
lensig=sizsig(2);
end
lensig1=lensig-1;
lensig2=lensig1-1;
%% if signal length is 2, return max/min as positive/negative polarity peaks
if ~lensig2
[sig,pospeakind]=max(signal);
[sig,negpeakind]=min(signal);
disp('2 element signal graph suppressed')
return
end
%% generate difference signal
difsig=diff(signal);
%% generate vectors corresponding to positive slope indices
dsgt0=difsig>0;
dsgt00=dsgt0(1:lensig2);
dsgt01=dsgt0(2:lensig1);
%% generate vectors corresponding to negative slope indices
dslt0=difsig<0;
dslt00=dslt0(1:lensig2);
dslt01=dslt0(2:lensig1);
%% generate vectors corresponding to constant intervals
dseq0=difsig==0;
dseq01=dseq0(2:lensig1);
clear difsig
%% positive to negative slope adjacencies define positive polarity peaks
pospeakind=find(dsgt00&dslt01)+1;
%% negative to positive slope adjacencies define negative polarity peaks
negpeakind=find(dsgt01&dslt00)+1;
%% positive slope to constant interval adjacencies initiate positive polarity peaks
peakind=find(dsgt00&dseq01)+1;
lenpeakind=length(peakind);
%% determine positive polarity peak terminations
for k=1:lenpeakind
peakindk=peakind(k);
l=peakindk+1;
% if end constant interval occurs, positive polarity peak exists
if l==lensig
pospeakind=[pospeakind;peakindk];
% else l<lensig, determine next nonzero slope index
else
dseq0l=dseq0(l);
while dseq0l&l<lensig1
l=l+1;
dseq0l=dseq0(l);
```

```
end
% if negative slope or end constant interval occurs, positive polarity peaks exist
if dslt0(l)|dseq0l;
pospeakind=[pospeakind;peakindk];
end
end
end
%% negative slope to constant interval adjacencies initiate negative polarity peaks
peakind=find(dslt00&dseq01)+1;
lenpeakind=length(peakind);
clear dseq01
%% determine negative polarity peak terminations
for k=1:lenpeakind
peakindk=peakind(k);
l=peakindk+1;
% if end constant interval occurs, negative polarity peak exists
if l==lensig
negpeakind=[negpeakind;peakindk];
% else l<lensig, determine next nonzero slope index
else
dseq0l=dseq0(l);
while dseq0l&l<lensig1
l=l+1;
dseq0l=dseq0(l);
end
% if positive slope or end constant interval occurs, negative polarity peaks exist
if dsgt0(l)|dseq0l;
negpeakind=[negpeakind;peakindk];
end
end
end
clear dsgt0 peakind
%% if initial negative slope occurs, initial positive polarity peak exists
if dslt00(1)
pospeakind=[1;pospeakind];
% elseif initial positive slope occurs, initial negative polarity peak exists
elseif dsgt00(1)
negpeakind=[1;negpeakind];
% else initial constant interval occurs, determine next nonzero slope index
else
k=2;
dseq0k=dseq0(2);
while dseq0k
k=k+1;
dseq0k=dseq0(k);
end
% if negative slope occurs, initial positive polarity peak exists
if dslt0(k)
pospeakind=[1;pospeakind];
% else positive slope occurs, initial negative polarity peak exists
else
negpeakind=[1;negpeakind];
end
end
clear dsgt00 dslt0 dslt00 dseq0
%% if final positive slope occurs, final positive polarity peak exists
if dsgt01(lensig2)
pospeakind=[pospeakind;lensig];
% elseif final negative slope occurs, final negative polarity peak exists
elseif dslt01(lensig2)
negpeakind=[negpeakind;lensig];
end
```

```
clear dsgt01 dslt01
%% if peak indices are not ascending, order peak indices
if any(diff(pospeakind)<0)
pospeakind=sort(pospeakind);
end
if any(diff(negpeakind)<0)
negpeakind=sort(negpeakind);
end
%% if signal is a row vector, modify peak indices to row vectors
if sizsig1==1
pospeakind=pospeakind.';
negpeakind=negpeakind.';
end
% plot signal peaks
% JFD I really don't want it to splat a plot on the screen....
% semilogy(0:lensig1,signal,'k-x',pospeakind-1,signal(pospeakind),'rs',negpeakind-1,
signal(negpeakind),'bo')
% xlabel('Sample')
% ylabel('Signal')
```

Appendix A5

```
function [f0,Q,A0]=qfit2(f,A)
% [f0,Q, A0]=qfit(f,Sxx)
% Determine Q-factors of peaks using Robinson fitting algorithm
% Robinson...
% Input
% f = frequency vector (real)
% A = Amplitude vector (can be complex)
% Outputs
% f0 = resonant frequency
% Q = Q-factor
% A0 = Amplitude at resonance
%
% uses:
% peakdetect - for initial peak search
% J F Dawson 7 APril 2006
%% Amplitude only no imaginary part
A=abs(A);
%% find index of all maxima and minima
[ppi,npi]=peakdetect(A);
%% find the distance between maxima and minima
% should be a minima between maxima and vice-versa except at the ends
if ppi(1)<npi(1) % a peak before first minima - remove it we can't deal with it
ppi=ppi(2:length(ppi));
end
%[ppi(length(ppi)-10:length(ppi)),npi(length(npi)-10:length(npi))]
if ppi(length(ppi))>npi(length(npi)) % a peak after last minima - remove it
ppi=ppi(1:length(ppi)-1);
end
%[length(ppi),length(npi)] % ppi should be one shorter than npi
if length(npi)-length(ppi) ~= 1
disp('Warning number of maxima should be one less than number of minima!)';
[length(ppi),length(npi)]
end
%% bracket each positive peak by adjacent minima
lppi=[npi(1:length(npi)-1)]; %minima which are lower bracket for each peak
uppi=[npi(2:length(npi))]; %minima which are upper bracket for each peak
% prune out noise and maxima unlikely to be useful for Q estimate
% At least mingap points either side separating from the next minima
mingap=1; %5;
%find all peaks separated from minima by at least mingap
clrpk=find((ppi-lppi>mingap) & (uppi-ppi>mingap)); % indices into list of clear peaks
% generate list of bracketed "clear" peaks: centre ; lower bracket ; upper bracket
cppi = ppi(clrpk);clppi = lppi(clrpk);cuppi = uppi(clrpk);
% A fall of minfall (ratio) from the peak so that we can resolve it
minfall=0.3; %~10dB
%find all peaks which have a fall > minfall to the nearest minima
hipk=find(((A(cppi)./A(clppi))>minfall) & ((A(cppi)./A(cuppi))>minfall));
%list of bracketed "high" peaks: centre ; lower bracket ; upper bracket
hppi=cppi(hipk);hlppi=clppi(hipk);huppi=cuppi(hipk);
% Get part of each peak to fit -
% go down fitfall
fitfall=0.7; % ratio: must be >= minfall
for i=1:length(hppi) % each peak
for j=hppi(i)-1:-1:hlppi(i) % low side
if (A(j)/A(hppi(i)))<fitfall
break;
end
end
hflppi(i,1)=j; % set the low limit to point near fitfall
for j=hppi(i)+1:+1:huppi(i) % high side
if (A(j)/A(hppi(i)))<fitfall
```

```
break;
end
end
hfuppi(i,1)=j; % set the low limit to point near fitfall
end % each peak
%% Fit to get Q-factor using MPRs method
f0=[]; Q=[]; A0=[];
f0=f(hppi);
A0=A(hppi);
```

Appendix A6

```
%% read data and format
clear all;
close all;
% Import Excel file into array
data1 = xlsread('Combined sq v tr');
% Run the Theoretical Matlab FFT Script
Theoretical_fft_analysis;
% Variables
f = data1(2:end,1); % Frequency in Hz
uV = 1E-6;
Volts = 1E6;
Vsq = 10.^(data1(2:end,2)./10)*uV; % Square Wave amplitude in volts.
Vtr = 10.^(data1(2:end,3)./10)*uV; % Triangle Wave amplitude in volts.
MHz = 1E6;
%% Square Wave & Triangle Wave Peaks
% Process peakks of the square wave
clf
[f0sq,Qsq,A0sq]=qfit3(f/MHz,Vsq);
% Process peaks of the triangle wave
clf
[f0tr,Qtr,A0tr]=qfit3(f/MHz,Vtr);
%% Plot data
% Square Wave
figure(1);
clf
semilogy(f/MHz, Vsq, 'b-*');
hold on
semilogy(f0sq,abs(A0sq),'ro');
hold on
grid on
% title ('Square Wave Frequency Domain Behaviour');
% xlabel('Frequency MHz');
% ylabel('Volts');
% legend ('Frequency Domain Behaviour', 'Square Wave Peaks');
% Triangle Wave
figure(2);
clf
semilogy(f/MHz, Vtr, 'b-*');
hold on
semilogy(f0tr,abs(A0tr),'ro');
grid on
title ('Triangle Wave Frequency Domain Behaviour');
xlabel('Frequency MHz');
ylabel('Volts');
legend ('Frequency Domain Behaviour', 'Triangle Wave Wave Peaks');
%% Plot Data for comparison
figure(3)
semilogy (f0sq, abs(A0sq),'b--o',f0tr,abs(A0tr),'r--o',f/MHz, In,'g-x') ;
grid on
title ('Square Wave / Triangle Wave Comparison');
xlabel('Frequency MHz');
ylabel('Volts');
legend('Square Wave Peaks', 'Triangle Wave Peaks')
%% Average Noise Levels of the emissions
A0_sq_dB = 10*log10(A0sq*Volts);
Ave_A0_sq_dB = mean(A0_sq_dB);
disp(Ave_A0_sq_dB);
A0_tr_dB = 10*log10(A0tr*Volts);
Ave_A0_tr_dB = mean(A0_tr_dB);
disp(Ave_A0_tr_dB);
```

Appendix A7

```
# NET LOCATIONS

NET "MCLK" LOC = W3;
NET "SMA_SIG2" LOC = V26;
NET "HP1_PIN_1" LOC = AF4;
NET "HP2_PIN_1" LOC = AF7;
NET "HP2_PIN_2" LOC = AE7;
NET "TRACE_1" LOC = J26;
NET "TRACE_2" LOC = K26;
NET "TRACE_3" LOC = L26;
NET "TRACE_4" LOC = L25;

# I/O Properties

#SMA_SIG2 - SMa OUTPUT FOR SPECTRUM ANALYSER

NET "SMA_SIG2" DRIVE = 12;
NET "SMA_SIG2" SLEW = FAST;
NET "SMA_SIG2" IOSTANDARD = LVCMOS25;

#HP2_PIN_1 - OUTPUT FOR OSCILLOSCOPE MEASUREMENTS

NET "HP2_PIN_1" DRIVE = 2;
NET "HP2_PIN_1" SLEW = slow;
NET "HP2_PIN_1" IOSTANDARD = LVCMOS25;

NET "HP2_PIN_2" DRIVE = 2;
NET "HP2_PIN_2" SLEW = SLOW;
NET "HP2_PIN_2" IOSTANDARD = LVCMOS25;

# Radiated Emissions Traces

NET "TRACE_1" DRIVE = 16;
NET "TRACE_1" SLEW = fast;
NET "TRACE_1" IOSTANDARD = LVCMOS12;

NET "TRACE_2" DRIVE = 16;
NET "TRACE_2" SLEW = fast;
NET "TRACE_2" IOSTANDARD = LVCMOS12;

NET "TRACE_3" DRIVE = 16;
NET "TRACE_3" SLEW = fast;
NET "TRACE_3" IOSTANDARD = LVCMOS12;

NET "TRACE_4" DRIVE = 16;
NET "TRACE_4" SLEW = fast;
NET "TRACE_4" IOSTANDARD = LVCMOS12;

```

Acronyms

Acronym	Definition
BGA	Ball Grid Array
BiCMOS	Bipolar CMOS
BLE	Basic Logic Element
C	Capacitance
CB	Connection Box
CD	Critically Damped
CLB	Configurable Logic Block
CMOS	Complementary Metal Oxide Semiconductor
dB	Decibels
dBµV	dB Microvolt
DC	Direct Current
DUT	Device under Test
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
FPGA	Field Programmable Gate Array
GHz	Gigahertz
GND	Ground
I/O	Input / Output
IC	Integrated Circuit
IOB	Input/Output Block
IP	Intellectual Property
L	Inductance
L-C-R	Inductor, Capacitor, Resistor
LUT	Look-up table
LVCMOS	Low Voltage CMOS
LVTTL	Low Voltage TTL
MATLAB	Matrix Laboratory
MHz	Megahertz
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MSCR	Master of Science Research
MUX	Multiplexer
OD	Overdamped
PCB	Printed Circuit Board
PDN	Power Delivery Network
PMOD	Peripheral Module
R	Resistance
RAM	Random Access Memory
SB	Switch Box
SRAM	Static Random Access Memory
SSCG	Spread Spectrum Clock Generation
SSN	Simultaneous Switching Noise
TTL	Transistor Transistor Logic
UD	Underdamped
VHDL	VHSIC Hardware Descriptive Language
VHSIC	Very High Speed Integrated Circuit

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