Novel GaN-based Vertical Field Effect Transistors for Power Switching

by

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Dedicated to my family

Abstract

Novel GaN-based vertical structures are investigated to exploit the high voltage and high power capability of GaN. Two distinctive structures – vertical high electron mobility transistor (VHEMT) and vertical junction field effect transistor (VJFET) are studied. The trade-off between on-state resistance (R_{on}), threshold voltage (V_{th}) and breakdown voltage are modelled using technology computer aided design (TACD) simulation and real devices are fabricated and characterized.

In the VHEMT structure. A novel crystallographic wet etching technique is developed to obtain a c-plane sidewall in a V-shape groove (V-groove). Based on this technique, a V-groove metal-oxide-semiconductor (VMOS) structure is established. The threshold voltage shifts from 2 to 6 V after multiple sweeps which indicates presence of interfacial traps. In addition, an AlGaN/GaN heterostructure is successfully regrown by molecular beam epitaxy (MBE) on the V-groove surface which forms the platform for the two dimensional electron gas.

Subsequently, the design of VJFET structures are discussed. Contrary to the published result in the literature, the simulation suggests that a higher V_{th} can be achieved without compromising R_{on}. As a preparation for the VJFET structure, p-type GaN and $GaN_{1-x}As_x$ based diodes grown by MBE are characterized. A hole concentration of as high as 8.5×10^{19} cm^{-3} is achieved in the $GaN_{1-x}As_x$ structure which improves the conductivity and contact resistivity. Trench regrowth VJFET structures using p-GaN and p-$GaN_{1-x}As_x$ are characterized. A high leakage current is observed which is thought to be caused by defects at the regrowth interface. The regrowth structures are further studied in detail by transmission electron microscopy (TEM).

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List of publications

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Chapter 1 Introduction

1.1 Overview

Gallium Nitride (GaN) is a binary III-V compound which is a fast emerging wide bandgap material in high power, high voltage and high frequency applications. The potential of GaN was brought into people's sights in the 1990s by M. A. Khan et. al. where a sheet of carrier with unusually high electron density and mobility known as two dimensional electron gas (2DEG) was observed at an AlGaN/GaN hetero-interface [1-3]. Based on this advantage, GaN heterostructure field effect transistors (HFETs), also known as high electron mobility transistors (HEMTs) with very high switching speed and low resistance were developed which has become the main platform for modern GaN-based HEMT devices.

With the recent technology advancement, GaN HEMTs are attracting more interests in power switching applications. The key requirements for power switching applications are: (1) high breakdown voltage (V_{br}) with low on-state resistance (R_{on}) to reduce conduction loss, (2) high switching speed and (3) enhancement-mode (E-mode) operation (i.e. the device is off when no gate voltage is applied) for system fail-safe considerations. GaN shows its potential due to the wide bandgap (E_g), high critical field (E_{cr}), high electron mobility (μ_n) and saturation velocity (V_{sat}).

The overall material properties of GaN and its major rivals, Silicon (Si) and Silicon Carbide (SiC), are shown in Table 1.1 [4]. Although the thermal conductivity of GaN is slightly lower than Si, the E_g of GaN is more than three times higher. As a result, the intrinsic carriers are greatly reduced which enables GaN to work more reliably under high temperature. The high E_{cr} allows a smaller device size to sustain the high voltage, together with high electron mobility and high saturation velocity enable GaN-based devices to be more compact and work at lower loss and higher efficiency than Silicon devices. The E_g and E_{cr} are similar for GaN and SiC. However, due to the existence of the high mobility 2DEG, GaN-based devices are

expected to achieve lower R_{on} and higher switching speed hence increasing the overall efficiency.

Table 1.1 Comparison of material properties of Si, GaN and 4H-SiC [4].

	Si	GaN	4H-SiC
Bandgap (eV)	**1.12**	**3.39**	**3.26**
Critical field (MV/cm)	**0.3**	**3.3**	**2.0**
Electron mobility (cm^2/V-s)	**1350**	**1000 (bulk) 2000 (2DEG)**	**650**
Dielectric constant	**11.8**	**9.9**	**10**
Electron saturation velocity (10^7 cm/s)	**1.0**	**2.5**	**2.0**
Thermal conductivity (W/cm-K)	**1.5**	**1.3**	**4.5**
BFOM	**1**	**827**	**330**

For power electronics, Baliga's Figure of Merit (BFOM) is the most commonly used standard to evaluate the potential of vertical devices based on the physical properties of the semiconductor. This is described by Eq. 1.1.1 [5,6].

$$BFOM(vertical) = \varepsilon_s \, \mu_n \, E_c^3 = \frac{4 \, V_{br}^2}{R_{on}} \qquad [1.1.1]$$

where ε_s is the permittivity of the semiconductor. Using Si as a reference, the normalized BFOM of GaN and SiC are shown in table 1.1. GaN shows the greatest potential among the three materials.

At the moment, GaN HEMTs have found their place in the medium voltage market sector. 600/650 V rated devices are commercially available from several manufacturers. Evaluation boards using commercial GaN devices were built to assess GaN device performance [7]. For example, a 5 kW DC-DC boost converter was designed to operate at 1 MHz switching frequency which achieved over 98% efficiency and much reduced system weight [8]. A 4 kW three-phase inverter was built with 600 V GaN HEMTs to operate at 100 kHz as a motor drive unit. The inverter was able to produce spike-free sine wave output and showed a significant improvement in efficiency over the Si IGBT counterpart [9,10]. A 600 V/29 mΩ power factor

correction (PFC) unit designed for 750 kHz switching frequency, also showed significant improvement in power conversion efficiency over the Si power MOSFETs [11,12]. Overall, GaN is a very promising material to boost the performance of power electronic devices and the GaN power market is expected to expand very quickly in the coming years.

Despite the excellent material properties, the performance of GaN-based devices is yet to match the theoretical limits. There is a range of obstacles to be tackled to realise the true potential. For instance, the high cost of bulk substrate has prevented wide adoption of natively grown GaN devices. In fact, most of the products today are grown on Si substrates to reduce cost. However, Due to the large lattice mismatch (17%) and thermal expansion coefficient (56%), GaN-on-Si suffers from high dislocation densities typically in the range of 10^9 cm^{-2} which can result in leakage currents and early device breakdown [13-15]. In addition, GaN-based devices are susceptible to trapping effects, both at the semiconductor surface and in the bulk region. The trapped electrons act as negative charges which can reduce the number of carriers in the channel, hence reducing the conductivity and give rise to current collapse. Due to these reasons, SiC devices are dominating the high voltage (>1200 V) applications [4,16].

On another aspect, improving the quality of p-type GaN is another important task. As a building block of many devices, a reliable p-GaN not only enables a variety of device topologies, including many vertical ones, but also greatly improves device performance and reliability. At the moment, p-type ion-implantation is not readily available due to severe lattice damage and low activation efficiency [17-19]. Therefore, the production of most p-GaN layers are limited to epitaxial growth. Magnesium (Mg) is the most widely used p-type dopant. However, due to the high activation energy (170 meV) of Mg acceptors, the formation of Mg-H complexes and the self-compensation effect, the maximum effective hole concentration achieve is typically in the lower 10^{18} cm^{-3} range

[20-22]. In addition, there are also other issues such as dislocations, interfacial defects and bulk trapping effects which pose threats to device performance and reliability.

1.2 Motivations for developing vertical devices

For power electronics, many applications require high voltage (> 1000 V) blocking capability. Taking the application in electric vehicles for example. A low-loss high voltage switching unit is required to drive the motor. While the maximum motor source voltage is 650 V, a higher breakdown rating of 1.2 kV is required to take account for the voltage overshoot caused by parasitic components in the system [23,24]. Currently, the main stream of GaN HEMTs adopt a lateral topology where the current flows laterally in the device as shown in Fig. 1.1 (a).

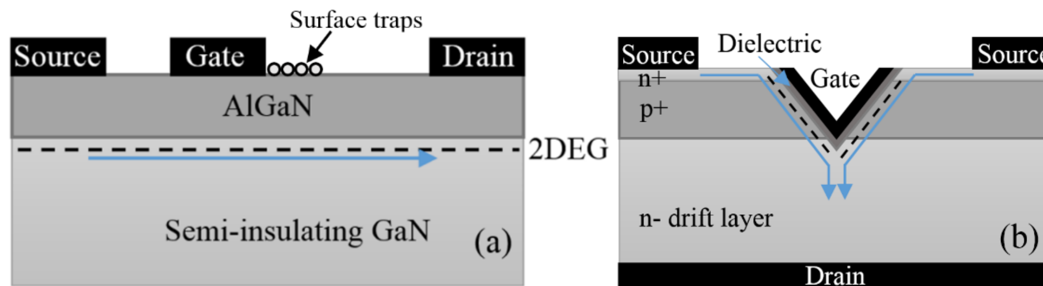

Fig. 1.1 Schematic device structures of (a) HEMT and (b) VMOSFET.

These devices can work comfortably within the 650 V requirement. To further increase V_{br} to 1200 V, the distance between the gate and drain contacts needs to be nearly doubled which would result in an increased device footprint. In comparison, vertical structures are not restricted by the device area. Fig. 1.1 (b) shows the schematic structure of a vertical metal-oxide-semiconductor field effect transistor (VMOSFET) where the current flows vertically. Only an increased thickness is needed to accommodate the high voltage. Hence, higher current capacity and power density are expected for vertical devices for applications above 1000 V.

An additional benefit from vertical structures is the mitigation of surface related instabilities as seen in lateral HEMTs. In lateral HEMTs, the peak electric field usually occurs at the gate edge on the drain side. The high field promotes electrons to tunnel through the barrier causing surface leakage current [25]. In addition, electrons are more likely to be trapped by the surface

traps, forming a negatively charged region which acts as a "virtual gate" causing a current collapse phenomenon during a switching transient, which is known as DC-RF dispersion [26,27]. Although these issues can be alleviated by proper surface passivation and multiple field plate designs, they remain problematic at high voltages. In vertical structures, the peak electric field is held in the bulk of the semiconductor, typically by a reverse biased P-N junction, hence the surface related issues could be eliminated.

1.3 Background of GaN-based vertical devices

The first structure being investigated is the vertical P-N diode as shown in Fig. 1.2(a), which is the building block of many vertical transistors. Due to the large difference in lattice constant, GaN grown on foreign substrates, such as sapphire and Si, suffers from high background doping and high dislocation density (10^9 cm^{-2}) which poses a challenge to the V_{br} of the device. Yet, tremendous improvements have been achieved in the recent years. By carefully controlling the background doping and dislocation density, GaN-on-sapphire quasi-vertical diodes with V_{br} of 800-1000 V have been achieved [28,29]. Meanwhile, the blocking capability of GaN-on-Si diodes has been increased to more than 500 V and provides the possibility to achieve fully-vertical structures [30,31].

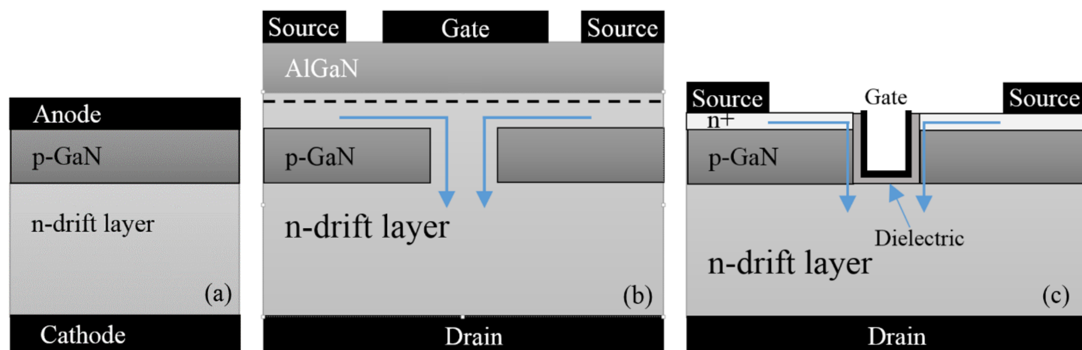

Fig. 1.2 Schematic device structures of GaN-based (a) P-N diode, (b) CAVET and (c) UMOSFET.

However, the breakdown field observed in these devices is typically less than 1.9 MV/cm which is still far away from the theoretical value (3.3 MV/cm) which suggests the breakdown is still dominated by the imperfections in the material. However, using these substrates can effectively reduce cost and could be adopted by the medium voltage range sector.

The real potential of GaN diodes was not brought to realization until recently when low dislocation density (10^4 to 10^6 cm^{-2}) bulk GaN substrates became commonly available. GaN diodes with V_{br} ranging from 1.4 to 4.7 kV have been reported [32-38]. Thanks to the lattice matched substrate, the drift region can be grown much thicker (up to 40 μm reported) while maintaining low n-type doping densities (~10^{15} cm^{-3}). Meanwhile, avalanche breakdown with more than 3 MV/cm breakdown field has been observed by many groups [33-36,39] and the forward bias ideality factor near unity has been observed with 8 μm thick drift region and >1400 kV breakdown voltage [35]. These remarkable results illustrate the importance of achieving good crystal quality and demonstrate the potential of GaN devices.

In comparison to P-N diodes, GaN-based vertical transistors are still at the early stage of development. So far, one of the most widely studied vertical structures is the current aperture vertical electron transistor (CAVET) which was first demonstrate in early 2000s for dispersion-free performance [40,41]. Later on, the structure was re-designed to exploit the high breakdown voltage advantage. The device structure is shown in Fig. 1.2 (b). In principle, the device utilises an AlGaN/GaN structure to control the current flow along the 2DEG. Because of the p-GaN current blocking layer (CBL), current can only flow vertically through the aperture and to the drain. It combines the advantage of high speed HEMT and the high voltage capability with a thick drift layer. However, the main difficulty is the formation of the channel (aperture) region. Various fabrication techniques have been attempted by UCSB, including aperture regrowth by MOCVD [40], Mg-implanted CBL [42], and regrown CBL by both MBE and MOCVD [43]. The best achieved V_{br} in these structures was 250 V with R_{on} of 2.2 mΩ-cm^2 [42]. By optimizing the regrowth process, a record low R_{on} of 0.4 mΩ-cm^2 was achieved with dispersion-free operation using 200 ns pulses, however, at a much reduced V_{br}

of 20 V [43]. In 2014, H. Nie et. al. reported a 1.5 kV 2.2 mΩ-cm^2 CAVET structure on a bulk GaN substrate which is so far the best V_{br}/R_{on} FOM reported in CAVET structures [44]. This device also features an E-mode operation achieved using a p-GaN gate structure which is very promising for power switching applications. There were also some creative structures [45,46] which were variations of the CAVET.

Another promising structure is the U-shape metal-oxide-semiconductor FET (UMOSFET) which is shown in Fig. 1.2 (c). The current conduction is supported by the inversion layer at the vertical sidewall of the U-shape trench and the off-state leakage is blocked by the p-GaN CBL. This structure benefits from a simpler device structure and inherent E-mode operation. The best reported R_{on} was 1.8 mΩ-cm^2 for a 1.2 kV device [47], and a higher blocking voltage of up to 1.6 kV has been demonstrated at the expense of increased R_{on} [48]. The downside of this structure is the low inversion channel mobility, hence lower transconductance, which could slow down the switching speed of the device. Based on the same principle, there was development of static induction transistors (SITs) which is a simpler version of MOSFET, however, the V_{br} is limited below 450 V for the SITs even with a bulk GaN substrate [49,50].

As an overview, the BFOM of the vertical devices are compared in Fig. 1.3. The material limits are calculated using eq. 1.1.1 based on the theoretical values shown in table 1.1. It can be seen that P-N diodes using bulk GaN substrates are approaching the theoretical limit of GaN. In the meanwhile, despite being at the early stage of development, GaN vertical transistors are already close to the SiC limit and great progress are expected in the coming years.

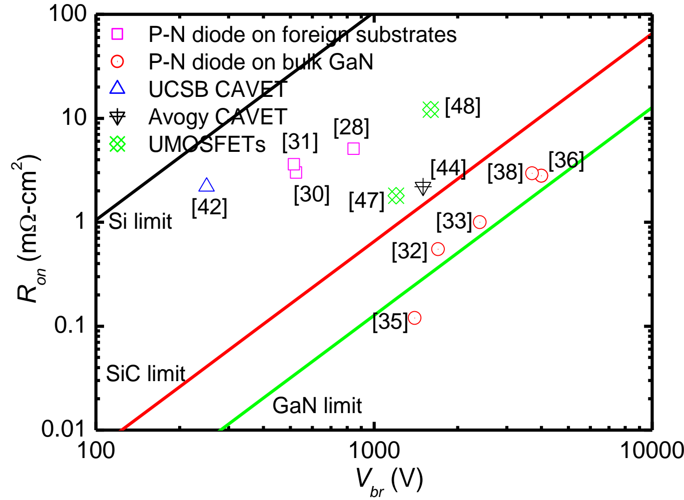

Fig. 1.3 Benchmark of recent GaN-based vertical diodes and vertical transistors.

1.4 Synopsis of the thesis

Due to the demands for high power, high voltage power electronic devices, there is an increasing interest in developing vertical devices. This work focuses on the development of novel vertical transistors using GaN-based materials. The research covers the device design & modelling, material growth, device fabrication and characterizations of two distinctive structures: VHEMT and VJFET.

Chapter 2 describes the fundamentals of GaN, including material properties, the polarisation effect and formation of 2DEG in the AlGaN/GaN heterostructure. The operation of a basic GaN HEMT and a threshold voltage model are discussed. Next, utilising the unique polarisation effect, a novel vertical HEMT structure is introduced with a TCAD simulation-based modelling of various design parameters.

Chapter 3 presents the fabrication of the VHEMT structure. A novel crystallographic KOH wet etching technique is developed to form a c-plane sidewall. After etching, an AlGaN/GaN channel regrowth is performed by two epitaxial growth methods, MBE and MOCVD. The respective structures are studied both structurally and electrically. In addition, a VMOSFET structure is demonstrated with effective transistor behaviour.

In chapter 4, GaN_xAs_{1-x}-GaN P-N diodes are fabricated and characterized as a preparation for the VJFET structure. The conductivity and crystallinity of the GaN_xAs_{1-x} layers are found to vary with the growth conditions. The current conduction mechanism in the diodes is also studied in forward and reverse bias conditions.

Chapter 5 starts with a discussion in design and modelling through TCAD simulation in terms of the device threshold voltage, on-state resistance and breakdown voltage. Secondly, the VJFET structure is fabricated in two routes - the p-type regrowth and the n-type regrowth. The regrown structures are thoroughly studied.

Lastly, Chapter 6 concludes the thesis and presents recommendations for the future work.

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Chapter 2 Device Physics, Simulation and Modelling

In preparation for device fabrication, simulation work is performed to predict the electrical behaviour. The simulation work was performed using Sentaurus TCAD (version G2012.06), provided by Synopsis [1]. Computer aided simulation is a very useful tool in designing semiconductor devices, not only for reproducing measured results and predicting device performance, but also providing a path towards understanding of the device physics behind the electrical behaviour. In this chapter, the operation of TCAD is explained with an example of conventional AlGaN/GaN HEMT structure, followed by analyses of specific device structures of VHEMTs.

2.1 Introduction to TCAD

Overall, the simulator represent a continuous region by discretizing it onto a grid of nodes. This process is known as meshing. The device is approximated by solving numerical equations in each node. Fig. 2.1 illustrates the process of a simulation. The simulation begins with building the device, including defining materials, adding doping, adding contacts and meshing. Here, applying appropriate meshing is the most critical process to achieve better convergence. Then appropriate material parameters (e.g. bandgap and carrier mobility) and physical models (e.g. polarisation and carrier transport mechanisms) are assigned to each region. Thirdly, the test conditions (e.g. ramping voltage across contacts) are defined and the transport equations are solved. Lastly, the current-voltage (I-V) results are extracted and the profile of the device can be viewed.

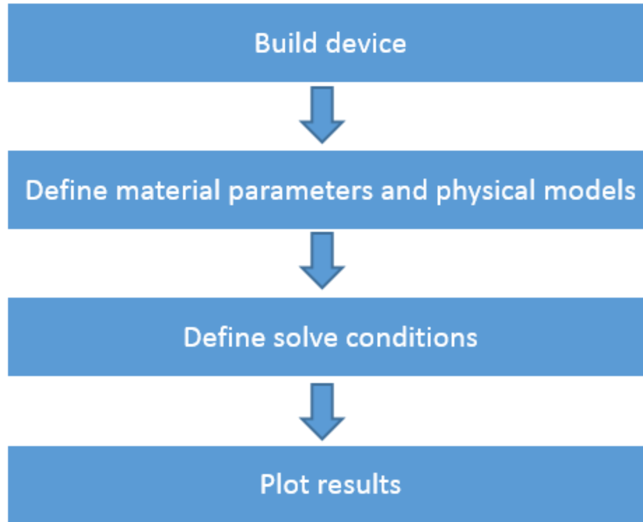

Fig. 2.1 Illustration of the flow of TCAD simulation.

In the scope of this work, simulation is performed by solving Poisson's equation coupled with the 2D drift-diffusion (DD) carrier transport equations and current continuity equations. For instance, the electrostatic potential is the solution of Poisson's equation,

$$\varepsilon\nabla^2\phi = -e(p - n + N_D - N_A) - \rho_{trap} \qquad [2.1.1]$$

where ε is the electrical permittivity, e is the elementary charge, n and p are the electron and hole densities, N_D and N_A are the ionized donor and acceptor charge densities and ρ_{trap} is the charge density contributed by traps and fixed charges. The electron and hole current continuity equations are given by,

$$\nabla \cdot J_n = e\frac{\partial n}{\partial t} + eR_{net} \qquad [2.1.2]$$

$$-\nabla \cdot J_p = e\frac{\partial p}{\partial t} + eR_{net} \qquad [2.1.3]$$

where J_n and J_p are the electron and hole current densities and R_{net} is net recombination rates. The generation-recombination (GR) process is normally modelled by Shockley-Read-Hall (SRH) process. The Direct band-to-band generation is neglected due to the large bandgap of GaN and extremely low intrinsic carrier densities at room temperature. The electron and hole currents described by the 2D drift-diffusion equations are given by,

$$J_n = -en\mu_n E + eD_n \nabla n \quad [2.1.4]$$

$$J_p = -ep\mu_p E - eD_p \nabla p \quad [2.1.5]$$

where μ_n and μ_p are electron and hole mobilities, D_n and D_p are the electron and hold diffusivities and E is the electric field. The first term describes the drift current which is dependent on the carrier density and mobility. For GaN-based HEMTs the electron mobility in the 2DEG channel is much higher than the bulk region hence it must be treated separately in order to obtain the correct simulation results.

In addition to these fundamental semiconductor equations, specific physical models are applied to different device structures which will be discussed separately in the following sections.

2.2 Models for AlGaN/GaN HEMTs

2.2.1 Spontaneous and piezoelectric polarisations

In comparison to the classic Si-based devices, the GaN-based devices feature unique polarisation effects that have significant influence over the device performance. For instance, GaN devices are usually grown in a Wurtzite structure which is formed with hexagonal unit cells where Ga atoms and N atoms form an intercepting close packed sub-lattices as shown in Fig. 2.2. Due to the different electronegativity of Ga and N atoms, the electrons tend to move towards one atom [2]. This asymmetric distribution of electrons results in a net positive charge at one end and a net negative charge at the other end, known as a dipole moment, exists along the c-axis or the [0001] direction which is known as spontaneous polarisation (P_{SP}).

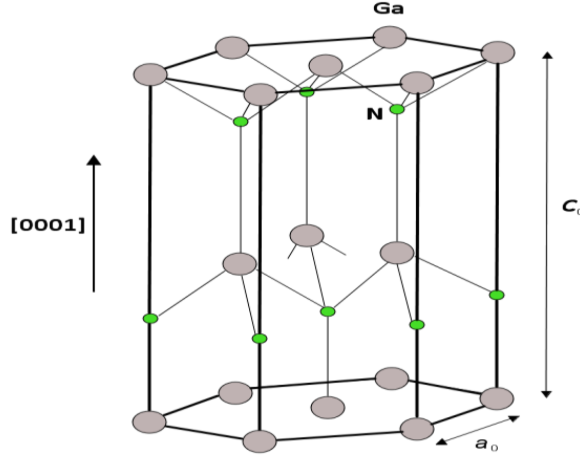

Fig. 2.2 Lattice structure of Ga-face Wurtzite GaN unit cell.

The spontaneous polarisation coefficients for GaN and AlN are -2.9×10^{-6} and -8.1×10^{-6} C/cm^2, respectively. The negative sign indicates the direction of the field is in the [000-1] direction. For Ga-face devices, the field is pointing towards the substrate and the direction reverses for N-face devices. For ternary compounds (i.e. $Al_xGa_{1-x}N$), the spontaneous polarisation is modelled by a mole fraction dependent linear interpolation,

$$P_{SP(Al_xGa_{1-x}N)} = P_{SP(AlN)}x + P_{SP(GaN)}(1-x) \qquad [2.2.1]$$

Another important contribution is the piezoelectric polarisation (P_{PZ}) in the AlGaN barrier. Due to the difference in lattice constant, when an AlGaN layer is grown on a GaN buffer, the lattice mismatch creates a tensile strain in the AlGaN layer causing a distortion in the AlGaN lattice which results in a strain-induced piezoelectric polarisation field. The computation of piezoelectric component follows the expression [3],

$$P_{PZ} = 2\frac{a_{GaN}-a_{AlGaN}}{a_{AlGaN}}(1-relax)(e_{31}-e_{33}\frac{c_{13}}{c_{33}}) \qquad [2.2.2]$$

where e_{ij} are piezoelectric coefficients and c_{ij} are stiffness constants, a_{GaN} and a_{AlGaN} are the lattice constants of GaN and AlGaN respectively. A linear interpolation between GaN and AlN is used for calculating a_{AlGaN}. The term *relax* describes a strain relaxation effect when

the AlGaN layer exceeds a critical thickness. For the scope of this work, the AlGaN thickness is always kept below the critical value hence *relax* is assumed to be small (0.1 by default). The values of the parameters used in the simulation is summarized in table 2.1 below [4].

Table 2.1 Parameters used in the polarisation model [4].

Symbol	Unit	GaN	AlN
P_{SP}	C/cm^2	-2.9×10^{-6}	-8.1×10^{-6}
e_{31}	C/cm^2	-3.5×10^{-5}	-5×10^{-5}
e_{33}	C/cm^2	1.27×10^{-4}	1.79×10^{-4}
c_{13}	GPa	106	108
c_{33}	GPa	398	373
a	Å	3.189	3.112
relax		0.1	0.1

As the value of $(e_{31} - e_{33}\frac{c_{13}}{c_{33}})$ is always negative, the value of P_{PZ} and P_{SP} are both negative and in the same direction. Thus the net polarisation at the AlGaN/GaN interface is simply the sum of all components,

$$\rho_{Pol} = P_{PZ(AlGaN)} + P_{SP(AlGaN)} - P_{SP(GaN)} \quad [2.2.3]$$

As a result, a net positive sheet charge presents at the AlGaN/GaN interface and a negative sheet charge presents at the AlGaN surface, as shown in Fig. 2.3. These charges will result in an electric field that drives free electrons towards the AlGaN/GaN interface. Sentaurus has a built-in polarisation model to calculate the polarisation charge based on the above equations. For instance, the number of polarization charge depends on the AlGaN layer composition and thickness. In addition, the direction of the polarisation field is also defined in the parameter file so that the full polarization only exists on the (0001) direction. Alternatively, the corresponding polarisation charge can also be specified manually at each interface.

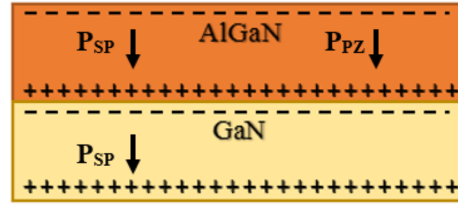

Fig. 2.3 Polarisation charges and polarisation fields in an AlGaN/GaN heterojunction.

2.2.2 Surface states and 2DEG

One of the advantages of GaN-based HEMTs is the existence of a high electron density and mobility channel, known as two dimensional electron gas (2DEG), where a sheet electron charges are confined in a triangular quantum well at the AlGaN/GaN interface. Unlike AlGaAs/GaAs heterostructures, AlGaN/GaN devices do not require any intentional doping in the barrier to achieve a 2DEG. As the AlGaN/GaN channel layers are un-doped (or unintentionally doped), the electrons do not suffer from impurity scattering. In addition, an AlN spacer layer is usually inserted between AlGaN and GaN to further reduce the alloy scattering whereby a very high electron mobility ~2000 $cm^2V^{-1}s^{-1}$ can be achieved which improves the device on-resistance (R_{on}) and switching speed.

In addition to the polarisation charges, surface states play an important role in determining the 2DEG. The atoms at surface of the semiconductor are missing adjacent atoms leading to broken covalent bonds, known as dangling bonds [5]. These bonds do not possess minimum energy configuration therefore behave like traps to capture/emit electrons. In addition, surface contaminants, crystal defects or damage can also form traps. There are two types of traps – donor-like traps and acceptor-like traps. Donor-like traps are neutral when occupied by electrons (below Fermi-level or E_F) and positively charged when empty (above E_F). Whereas Acceptor-like traps are negatively charged when occupied (below E_F) and neutral when empty (above E_F). The trap occupation and charge states are shown in Fig. 2.4.

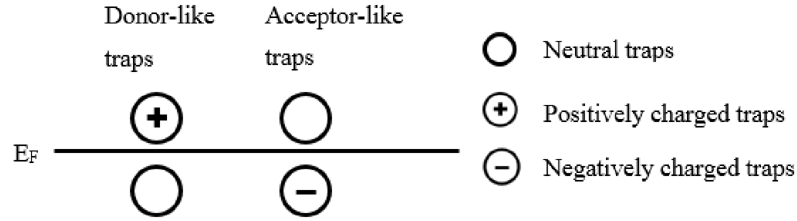

Fig. 2.4 Charge states of donor-like and acceptor-like traps with respect to the fermi-level

The source of the 2DEG is to-date inconclusive [6]. The most widely accepted explanation, proposed by Ibbetson et al. [7], is that the electrons from the surface donor-like traps are driven into the channel by the polarisation field forming the 2DEG channel. The 2DEG charges are balanced by positively charged surface traps to satisfy charge neutrality principle as shown in Fig. 2.5(a). Notice that this is under the assumption that the AlGaN layer has exceeded a critical thickness for the 2DEG to form. To illustrate this effect, a simulation is carried out.

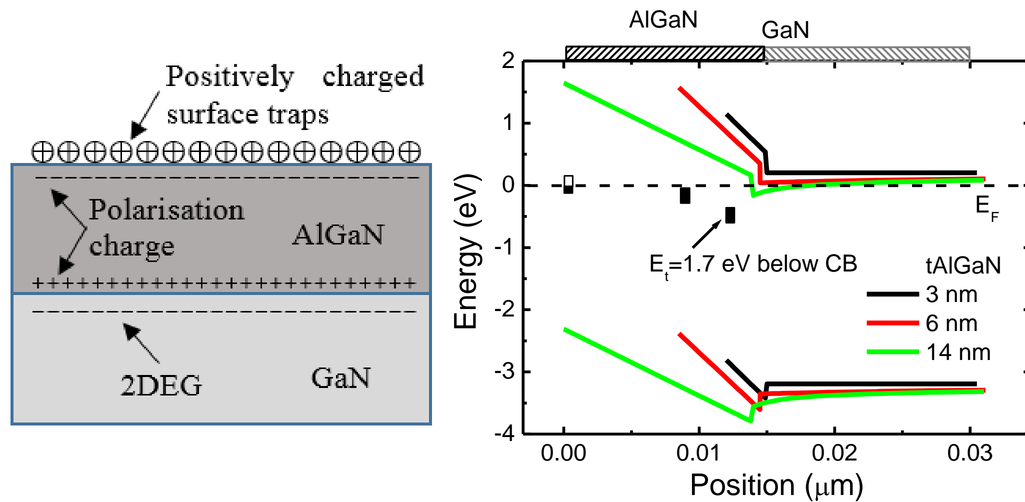

Fig. 2.5 (a) Charge distribution in an AlGaN/GaN structure. (b) Band diagram of AlGaN/GaN structures with different AlGaN thicknesses. The position of curves was moved horizontally for a better view.

The simulated energy band diagram and surface charge state is shown in Fig. 2.5(b). In the simulation, the Al mole fraction is kept constant at 20% (corresponding to a polarisation charge density of ~1.1×10^{13} cm^{-2}) and the thickness of the AlGaN layer is varied. The distribution of the energy of surface donor-traps is represented by an effective single energy

level E_t = 1.7 eV below conduction band (*CB*) [8]. It can be seen that for AlGaN thickness (*tAlGaN*) less than critical thickness (t_{cr}) (i.e. *tAlGaN* = 3 nm), the surface donor traps are below E_F and occupied by electrons, hence there is no 2DEG in the channel. As *tAlGaN* increases, the voltage drop across the AlGaN barrier increases and the donor traps approach the E_F and start to pass electrons into the channel. For *tAlGaN* > t_{cr}, the electrons are emptied from the donor traps and transferred into the channel forming a 2DEG. When this happens, the negative 2DEG charges and positive surface charges negate the polarisation charges, reducing the electric field in the AlGaN barrier which is reflected by a reduced slope as shown in the band diagram. It is noteworthy that both the energy level and the number of traps are important to determine the 2DEG density. For an ideal surface (i.e. no surface traps), there would be no 2DEG unless the valence band (VB) starts to cross the E_F which provides electrons from the states in the VB and forms a two dimensional hole gas (2DHG) at the surface to balance the 2DEG.

2.2.3 Derivation of threshold voltage

Fig. 2.6 illustrates the structure of a basic HEMT device which has three terminals including two ohmic contacts named source and drain and a terminal named gate. Usually a positive voltage is applied to the drain (V_d) to induce a current flow between the source and drain contacts. A gate voltage (V_g) (with respect to the source voltage) is applied to modulate the current flow in the 2DEG channel. A negative V_g repels electrons in the 2DEG, reducing the current in the channel. When V_g is large enough to deplete the 2DEG completely, the channel is pinched off and this voltage is defined as the threshold voltage (V_{th}) of the device.

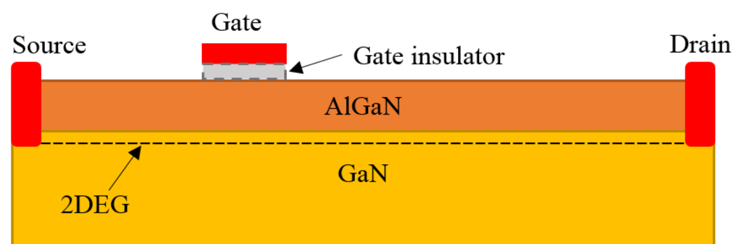

Fig. 2.6 Schematic structure of a basic HEMT device.

The gate can be formed by a Schottky metal contact (such as Ni/Au or Pt/Au) or a metal-insulator-semiconductor (MIS) structure. Generally a Schottky contact offers simpler structure and faster switching speed but is associated with higher leakage current and limited positive gate voltage range. In comparison, a MIS structure has an insulating layer (such as SiO_2, Al_2O_3 and SiN_x) between the gate metal and semiconductor to prevent gate leakage current and to increase the useful V_g range. However, adding an insulator layer also reduces the gate capacitance causing a shift in V_{th} and reduction in transconductance (g_m). In this section, a theoretical model of V_{th} of Schottky gate and MIS gate devices is derived with the aid of a band diagram.

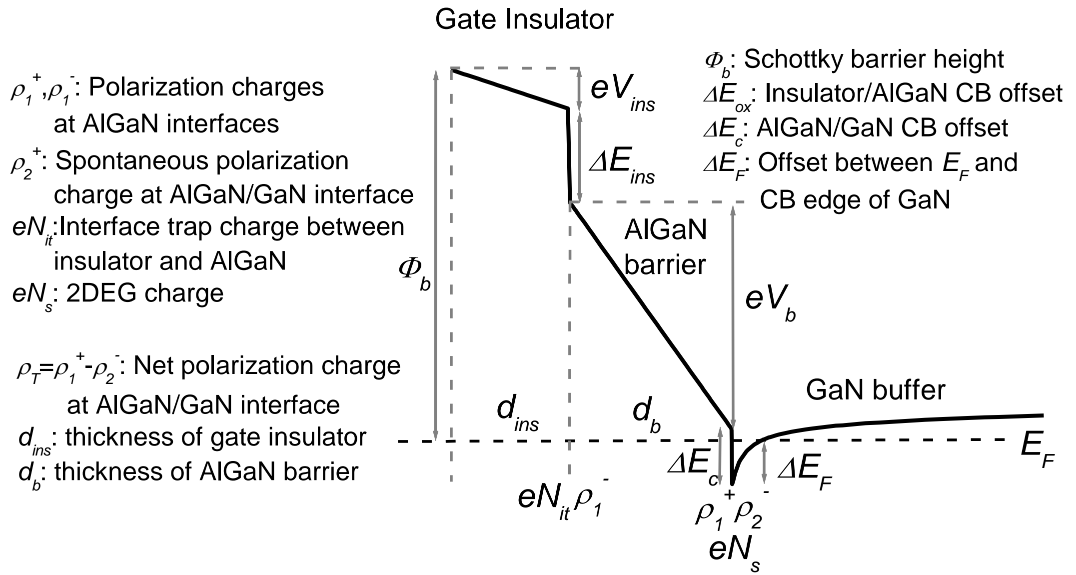

Fig. 2.7 Simulated conduction band diagram of AlGaN/GaN HFET with gate insulator layer showing band offsets and charge distribution.

The band diagram under the gate and charge distribution is shown in Fig. 2.7. Applying Gauss's Law to each interface,

$$\varepsilon_{ins}\, E_{ins} - \varepsilon_b\, E_b \;=\; eN_{it} - \rho_1^- \qquad [2.2.4]$$

$$\varepsilon_b\, E_b - \varepsilon_{bu}\, E_{bu} \;=\; \rho_T - en_s \qquad [2.2.5]$$

where ε_{ox}, ε_b *and* ε_{bu} are the permittivity of gate insulator, AlGaN barrier and GaN buffer, respectively, E_{ox}, E_b and E_{bu} are the electric fields perpendicular to the interface in the gate

insulator, AlGaN barrier and GaN buffer, respectively. N_{it} is the density of charge present at the insulator/semiconductor interface. Converting the electric fields used in expression 2.2.4 and 2.2.5 to the respective voltage drops across each region, assuming no space charge away from the interfaces,

$$\varepsilon_{ins}\,\frac{V_{ins}}{d_{ins}} - \varepsilon_b\,\frac{V_b}{d_b} = eN_{it} - \rho_1^- \qquad [2.2.6]$$

$$\varepsilon_b\,\frac{V_b}{d_b} - \varepsilon_{bu}\,\frac{V_{bu}}{d_{bu}} = \rho_T - en_s \qquad [2.2.7]$$

where d_{ins}, d_b and d_{bu} are the thickness of gate insulator, AlGaN barrier and GaN buffer, respectively. Since the field in the buffer away from the 2DEG is small, the second term on the LHS of Eq. [2.2.7] can be neglected. Substituting [2.2.7] into [2.2.6] gives the voltage developed across the gate insulator and AlGaN barrier layer,

$$V_{ins} = \frac{d_{ins}}{\varepsilon_{ins}}\,(eN_{it} - en_s - \rho_2^-) \qquad [2.2.8]$$

$$V_b = \frac{d_b}{\varepsilon_b}(\rho_T - en_s) \qquad [2.2.9]$$

where $\rho_T = (\rho_1^+ - \rho_2^-)$ is the net polarisation charge at the AlGaN/GaN interface. From inspection of Fig. 2.7,

$$(\Phi_b - eV_{ins} - \Delta E_{ins} - eV_b - \Delta E_c + \Delta E_F) = 0 \qquad [2.2.10]$$

Substituting Eq. [2.2.8] and [2.2.9] and solving for en_s,

$$en_s = \frac{C_b}{C_{ins}+C_b}(eN_{it} - \rho_2^-) + \frac{C_{ins}}{C_{ins}+C_b}(\rho_T) - \frac{C_{ins}\,C_b}{C_{ins}+C_b}\frac{1}{e}(\Phi_b - \Delta E_{ins} - \Delta E_c + \Delta E_F)$$

[2.2.11]

where, $C_b = \frac{\varepsilon_b}{d_b}$ and $C_{ins} = \frac{\varepsilon_{ins}}{d_{ins}}$ are the barrier and insulator capacitance per unit area, respectively. For a Schottky gate, $d_{ins} = 0$, $C_{ins} = \infty$ and $\Delta E_{ins} = 0$, Eq. [2.2.11] is simplified to,

$$en_s = \rho_T - \frac{C_b}{e}\,(\Phi_b - \Delta E_c + \Delta E_F) \qquad [2.2.12]$$

Adding a gate bias (V_g) to the system, $\Phi_b = \Phi_b - eV_g$ (conduction band is raised up with negative V_g). It can be seen that the effectiveness of V_g scales with the total capacitance. The V_{th} is defined when the conduction band edge reaches the Fermi level (i.e. $\Delta E_F = 0$). Setting $V_{th} = V_g$ and $en_s = 0$, solving for V_{th} gives the expression,

$$V_{th} = \frac{1}{e}\left(\Phi_b - \Delta E_{ins} - \Delta E_c\right) - \frac{d_{ins}}{\varepsilon_{ins}}\left(eN_{it} - \rho_2^-\right) - \frac{d_b}{\varepsilon_b}\left(\rho_T\right) \qquad [2.2.13]$$

In the absence of the gate insulator Eq. [2.2.13] is simplified to,

$$V_{th} = \frac{1}{e}\left(\Phi_b - \Delta E_c\right) - \frac{d_b}{\varepsilon_b}\left(\rho_T\right) \qquad [2.2.14]$$

In Eq. [2.2.13], N_{it} is the total net interface charge density, including the positive donor-like traps (with the same amount as the 2DEG) and other (either positive or negative) ionized charges. Increasing d_{ins} could shift the V_{th} to positive or negative direction depending on the relative magnitudes of eN_{it} and ρ_2^-. One way to achieve E-mode operation is by decreasing d_b (i.e. recessed gate structures) [9]. It not only reduces the voltage drop across the barrier, but also moves the surface donor states below the Fermi-level which reduces eN_{it}, hence V_{th} shifts towards the positive direction. Other ways to achieve E-mode operation could be increasing Φ_b by adding a p-type (Al)GaN layer at the gate [10,11] or introducing negative charges (such as fluorine implantation) to make N_{it} more negative [12-14].

2.3 Design of novel vertical HEMTs

In chapter 1, we have introduced the existing vertical structures which are all based on (0001) c-plane GaN. This section discusses the design of a novel vertical HEMT (VHEMT) which is grown on a (11-22) semi-polar substrate which is ~58° from the c-plane [15]. The main reason for using this orientation is to obtain a V-shape groove (V-groove) with a sloping c-plane sidewall by a crystallographic KOH-based wet etching process. The detailed fabrication process will be discussed in the following chapter.

The schematic device structure is shown in Fig. 2.8 which resembles a Si VMOS structure. The difference is that the VHEMT structure utilizes a 2DEG channel instead of an inversion layer on the sidewall. From the substrate, the device consists of a heavily doped n+ current spreading layer, a lightly doped n^- drift layer, a p^+ current blocking layer (CBL) and a top n^+ contact layer. After the V-groove etching, an AlGaN/GaN channel layer is over-grown on the V-groove surface, where a 2DEG is formed on the c-plane sidewall. The other sloping side wall is made up of two neighbouring m-planes from the m-plane family forming a "saw tooth" profile. It should be noted that the m-plane cannot form a 2DEG as it is a non-polar plane.

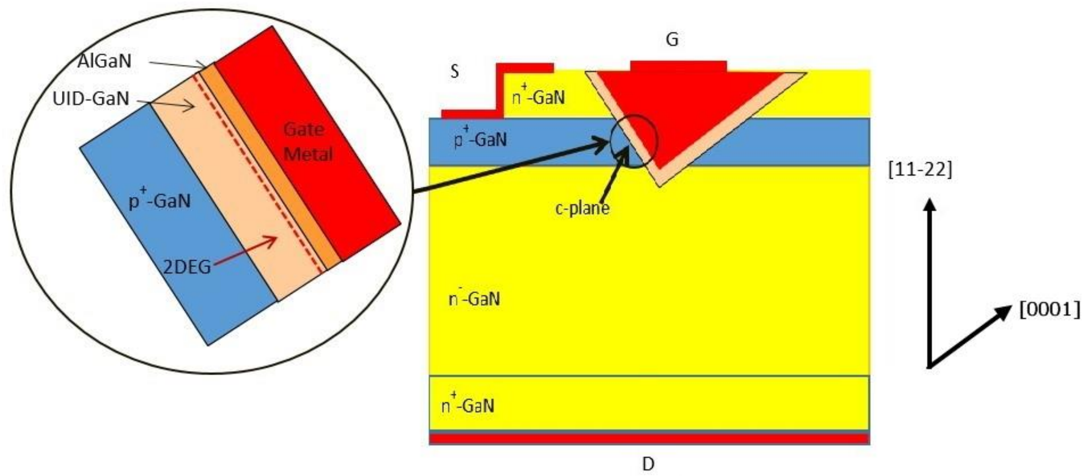

Fig. 2.8 Schematic structure of a VHEMT device

Instead of an inversion layer as in an MOS structure, a 2DEG on the c-plane side wall forms the conduction channel which allows for a lower R_{on} and higher transconductance (g_m). The device operates in the same way as in an HFET where the conductance of the 2DEG channel is controlled by the gate voltage and the V_{th} can be controlled by optimizing the composition and thickness of the AlGaN barrier. The off-state source-to-drain leakage is blocked by the p-type GaN current blocking layer (CBL). It should be emphasized that the p-GaN CBL must be conductive and grounded to allow charging and discharging of the P-N junction which is necessary for realizing high blocking voltage. A less conductive p-GaN can limit the charging/discharging current which could hinder the switching speed of the device.

2.3.1 Design parameters

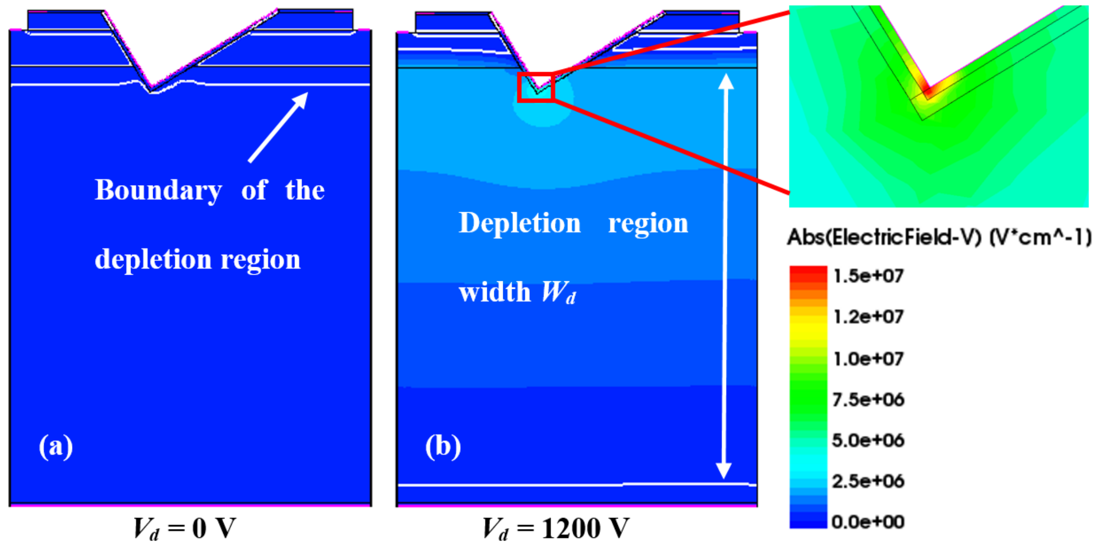

Fig. 2.9 Simulated electric field and depletion region with drain bias of (a) 0 V and (b) 1200 V. The enlarged region shows the peak electric field at the gate corner. The source and gate terminals are grounded.

The primary application of vertical structures would be in the high breakdown voltage (V_{br} > 1200 V) regime due to its area-effectiveness. The high voltage is sustained by a thick and lightly doped drift region. As shown in Fig. 2.9, when a P-N junction is reverse biased in the off-state, the depletion region will extend into the drift region towards the drain to sustain the electric field. The peak electric field in a P-N junction is described by,

$$|E_{peak}| = \frac{eN_D W_d}{\varepsilon_s} \quad [2.3.1]$$

where e is the elementary charge, N_D is the effective donor concentration in the drift region and ε_s is the permittivity of the semiconductor. In a one-sided junction, the depletion width (W_d) in the lightly doped drift region can be approximated by,

$$W_d = \left[\frac{2\varepsilon_s}{e}\frac{1}{N_D}(V_{bi} - V_{in})\right]^{\frac{1}{2}} \quad [2.3.2]$$

where V_{in} is the applied voltage and V_{bi} is the built-in voltage which is approximately equal to the bandgap (E_g) of the material, given by,

$$V_{bi} = \frac{E_g}{e} + \frac{kT}{e} ln\left(\frac{N_A N_D}{N_C N_V}\right) \quad [2.3.3]$$

where N_C and N_V are the density of states in the conduction band and valence band, respectively. The relationship between E_{peak} and V_{in} can be found by substituting Eq. [2.3.2] into [2.3.1] which gives,

$$|E_{peak}| = \sqrt{\frac{2eN_D(V_{bi} - V_{in})}{\varepsilon_s}} \quad [2.3.4]$$

For high voltage applications, V_{bi} (~3 V) can be ignored and the theoretical V_{br}, based on an avalanche breakdown process, can be calculated by substituting the critical electrical field (E_{cr}) and Eq. [2.3.4] is reduced to,

$$V_{br} = \frac{\varepsilon_s E_{cr}^2}{2eN_d} \quad [2.3.5]$$

Here E_{cr} represents the peak electric field at which the impact ionization integral reaches unity. It can be seen that V_{br} varies as a function of N_d.

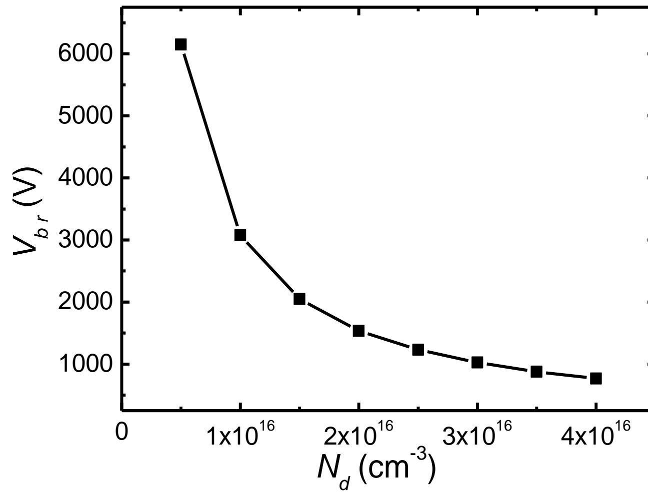

Fig. 2.10 Theoretical calculation of V_{br} as a function of N_d using a critical field of 3.35 MV/cm.

Using the theoretical E_{cr} value of 3.35 MV/cm, the V_{br} is plotted as a function of N_d in Fig. 2.10. From the plot, it can be seen that the N_d must be no more than 2.5×10^{16} cm^{-3} in order to sustain 1200 V. In practice, due to the defects and dislocations, the breakdown field is usually

less than the theoretical value. Hence, it is recommended to use lower N_d to give more safety margin. However, due to the impurities (Si, O, etc.) incorporated during GaN growth, the lowest doping level in UID GaN is typically about 1×10^{16} cm^{-3}, and the typical p-type doping can be achieved is about 2×10^{17} cm^{-3}. Taking these values into Eq. [2.3.1], the depletion width under 1200 V drain bias is about 11.5 μm. Therefore, a 12 μm drift layer is adopted in this study similar to other works in the literature [16,17]. On the other hand, the depletion into the p-GaN CBL is calculated to be about 0.55 μm. Considering the depletion at the upper P-N junction, a minimum thickness of 1 μm for the p-GaN CBL should be used to avoid punch-through under high reverse bias. Having the layer thicknesses set, the design parameters include (1) the penetration depth of the V-groove into the drift region (*t_penetration*), (2) AlGaN barrier thickness (*t_AlGaN*) and (3) gate dielectric thickness (*t_SiN$_x$*). The overall dimensions of the device is shown in Fig. 2.11.

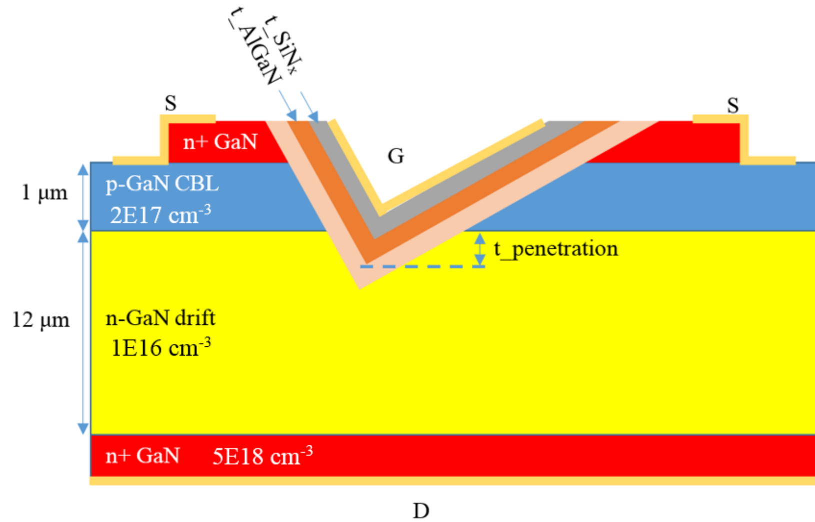

Fig. 2.11 Schematic VHEMT structure showing critical design parameters.

2.3.2 Transfer characteristics

An initial simulation is performed to calibrate the simulation using a lateral HEMT device with a 27 nm $Al_{0.2}Ga_{0.8}N$ barrier with a Schottky gate (i.e. *t_SiN$_x$* = 0 nm). The 2DEG concentration (~9×10^{12} cm^{-2}), electron mobility (~1750 cm^{-2}V^{-1}s^{-1}) and contact resistance (0.75 Ω-mm) are set as determined by Hall and transmission line model (TLM) measurements.

Fig. 2.12 (a) shows the calibration of transfer characteristics of a simulated device against a real device fabricated by our team at Sheffield. The *I-V* characteristics were obtained by quasi-static measurement (i.e. not in pulse mode) by two source measure units (SMUs). Good agreement is obtained except for a small discrepancy due to the self-heating effect which is typically seen at higher current levels (> 400 mA/mm) [18] which was not included in the simulation. Using the same 2DEG parameters, the simulated transfer characteristics of the VHEMT are shown in Fig. 2.12 (b). The V_{th} is -4.4 V as expected from the 2DEG concentration. Interestingly, a significant roll-off is observed at higher gate biases. For instance, for $V_g > -2$ V, the slope (g_m) is significantly reduced. This is in contrary to the operation of lateral HEMT as shown in Fig. 2.12 (a) which indicates that the conduction is dominated by another region rather than the 2DEG.

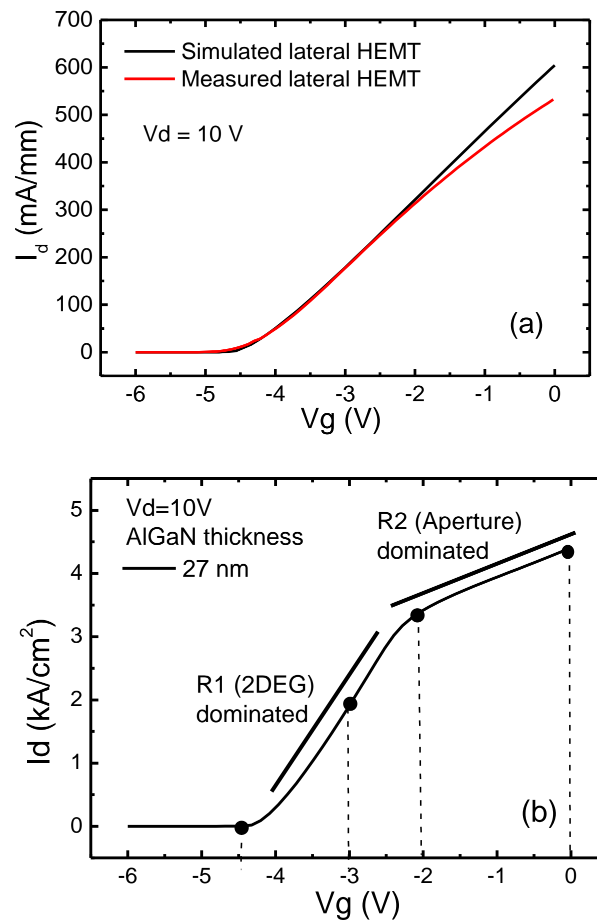

Fig. 2.12 Transfer characteristics of (a) simulated and measured lateral HEMTs used to calibrate the simulation, and (b) simulated VHEMT structure with a Schottky gate.

This behaviour can be explained by introducing an aperture resistance as shown in Fig. 2.13. The colour contour shows the electron density in the top region of the device. R1 and R2 represents the resistance of the 2DEG and the aperture region, respectively. The aperture resistance is formed due to the depletion region. In Fig. 2.12 (b), at $V_g = 0$ V, 2DEG channel is highly conductive hence R2 dominates. At $V_g = -2$ V, R1 is increased due to the reverse gate bias. As a consequence, the voltage drop across R1 is increased which effectively reverse biases the CBL/channel P-N junction, leading to an increased depletion region, hence R2 increases. At this moment, the conduction is still dominated by R2. At $V_g = -3$ V, R1 is much greater than R2 and conduction becomes 2DEG dominated. Finally, the channel is completely pinched off at $V_g < -4$ V.

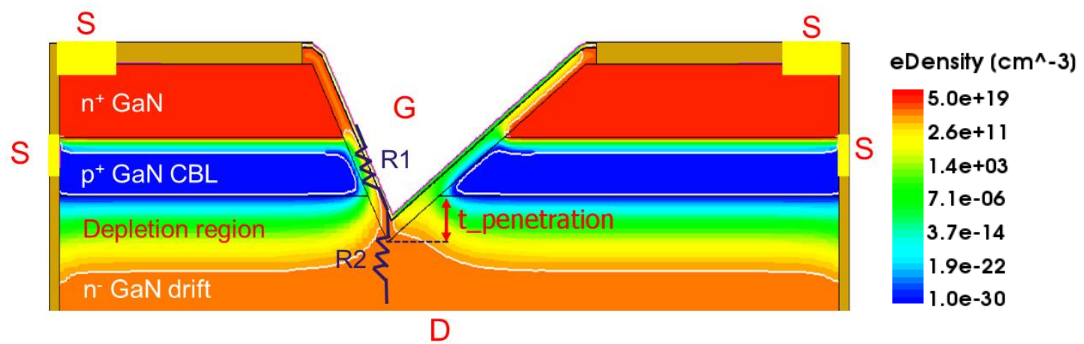

Fig. 2.13 Illustration of the dominant resistance paths. The colour contour shows the electron density in the on state.

One way to reduce the roll-off is by increasing *t_penetration* whereby the trench corner is moved away from the depletion region hence reducing R2. Fig. 2.14 illustrates the effects of varying *t_penetration*. With the trench corner moving away from the depletion region, the roll-off effect is deferred to a higher V_g and the current level at $V_g = 0$ V is increased from 2.5 to 5 kA/cm^2.

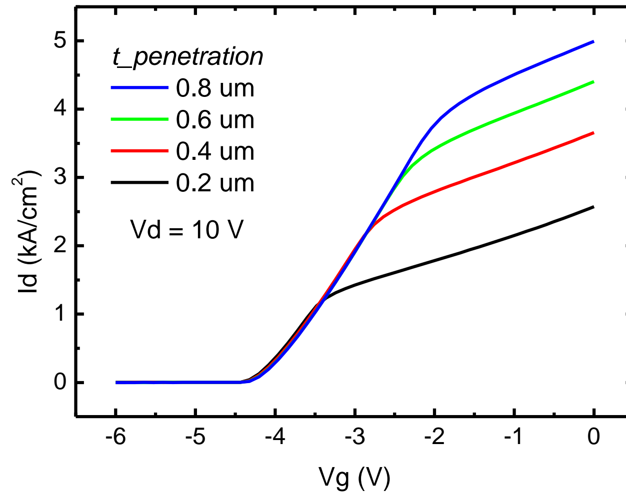

Fig. 2.14 Simulated transfer characteristics of VHEMTs showing the effects of different penetration depth.

This concept can also be explained by a cascode structure where R1 and R2 can be viewed as two transistors connected in a cascode configuration as shown in Fig. 2.15 (a) where R1 is the 2DEG channel with V_{th} = -4 V and R2 is effectively a JFET whose V_{th} depends on *t_penetration*. R_{drift} and R_{CBL} are the resistance of the drift region and p-GaN CBL, respectively. To validate this concept, this model was applied into a SPICE modelling where two transistors (R1 and R2) are connected in a cascode configuration as shown in Fig. 2.15 (a). The V_{th} of R1 is fixed at -4 V and the V_{th} of R2 is varied between -15 to -3 V to mimic the change in *t_penetration*. R_{drift} and R_{CBL} are set to small values as they are not the major factors in this model.

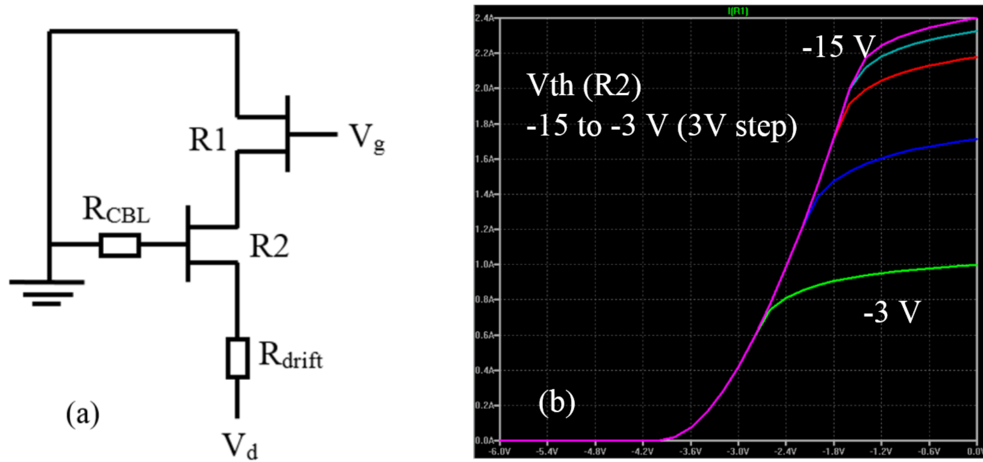

Fig. 2.15 (a) the cascode configuration used in the SPICE model. (b) SPICE modelling results of transfer characteristics with the V_{th} of R2 varied from -15 V (purple) to -3 V (green).

The simulated result is shown in Fig. 2.15 (b). Higher current level is achieved when $V_{th\,(R2)}$ is more negative, corresponding to larger *t_penetration* (i.e. deeper trench). Therefore, the same effect was reproduced which validates the proposed model. This concept is applicable for many vertical structures that consist of a channel through the p-GaN CBL region, such as CAVET and UMOS structures to certain extent. However, as the trench corner moves closer to the drain, higher electric field is subjected to the gate. So the trade-off between the R_{on} and V_{br} must be considered which will be discussed in the following sections.

2.3.3 Threshold voltage and electric field in MIS gate structures

As discussed in section 2.2.3 as well as published by several authors [7-9,19,20], one way to achieve E-mode operation is by reducing the barrier thickness to a sub-critical thickness. As shown in Fig. 2.16 (a), a V_{th} of 0.5 V is achieved with *t_AlGaN* = 3 nm. However, the maximum gate voltage that can be applied is ~1.5 V as a large current will flow through the Schottky gate for higher gate biases. This limits the useful range of V_g and the output current. Besides, such a low V_{th} may have safety issues as any noise in the gate voltage can falsely turn on the device. Therefore, a higher V_{th} (> 3 V) is preferred which can be achieved by inserting a gate dielectric/insulator.

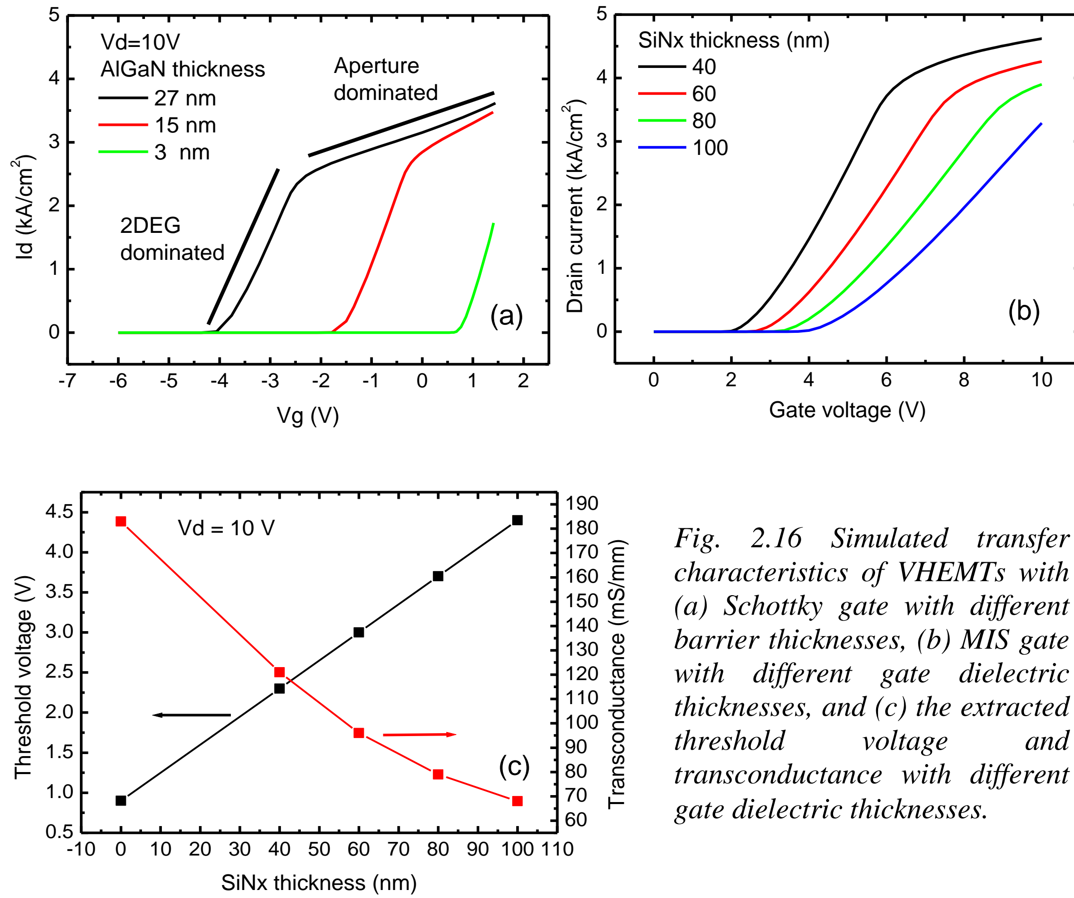

Fig. 2.16 Simulated transfer characteristics of VHEMTs with (a) Schottky gate with different barrier thicknesses, (b) MIS gate with different gate dielectric thicknesses, and (c) the extracted threshold voltage and transconductance with different gate dielectric thicknesses.

The results are shown in Fig. 2.16 (b). In the simulation, a silicon nitride (SiN_x) layer with varying thickness is used as the gate dielectric. It is worth mentioning that as the donor-like traps at the SiN_x/AlGaN interface are now below the fermi-level, the net interfacial trap density (N_{it}) is zero (assuming no other charge components). It can be seen that the V_{th} is increased with increasing SiN_x thickness which is due to the reduction in gate capacitance. However, it comes with the cost of reduced transconductance (g_m). The values of V_{th} and g_m are extracted with respect to SiN_x thickness in Fig. 2.16(c) where a clear trade-off is observed.

Another important aspect for power applications is the breakdown voltage (V_{br}) of the device. From the experience in Si VMOS devices, the major challenge is the crowding of electric field lines at the sharp trench corner, therefore the VMOS structure was soon replaced by UMOS and double-diffused MOS (DMOS) structures [21]. However, in the VHEMT, a V-groove is necessary for the high mobility 2DEG on the c-plane. One way to reduce the electric field is by rounding the trench corner. This can be achieve during the regrowth process as the GaN

atoms tend to accumulate at the bottom of the trench. A rounded corner is observed which will be discussed in the following Chapter.

Due to the presence of a high density of dislocations and defects, the breakdown of GaN-based devices is predominantly affected by the leakage current through dislocations and defects, instead of the classic avalanche breakdown. In addition, the impact ionization coefficients of GaN and SiN_x are not well established. Therefore, in the simulation, the V_{br} of the device is correlated to the electric field in the device. To compare the difference in the electric field, sharp corner (limited by mesh size ~1 nm) and rounded corner (with 20 nm radius) structures are simulated. The drain bias is ramped to 1200 V and the gate is held at 0 V as the device operates in the E-mode (*t_AlGaN* = 3 nm). The SiN_x thickness and *t_penetraion* are set to 40 nm and 0.6 μm, respectively. Fig. 2.17(a) and (b) depict the electric field distribution in the MIS gate structure with a sharp corner and rounded corner, respectively. It can be observed that the electric field peaks at the SiN_x surface at the trench corner with the magnitude reduced from 13 to 10.8 MV/cm by rounding the corner.

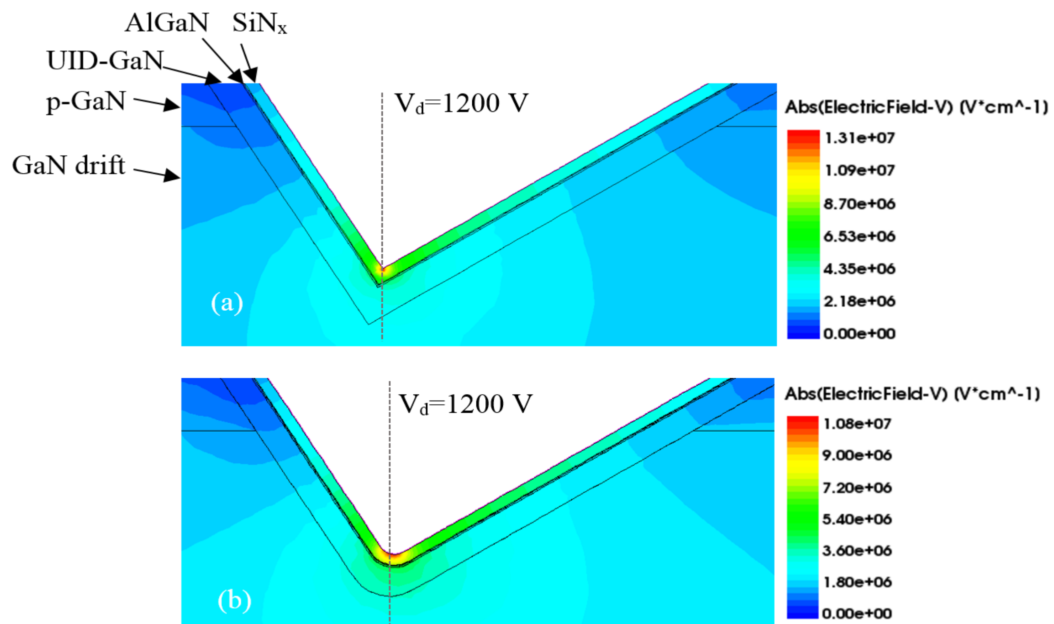

Fig. 2.17 Simulated electric field distribution at drain bias of 1200 V in the VHEMT structures with a (a) sharp corner and (b) rounded corner. The colour represents the electric field distribution. The dotted lines illustrate the position of the cut lines where the electric field is plotted in Fig 2.18.

Although the field is reduced, the value of the field is still enormous. Experimental work in the literature shows that the breakdown field of PECVD SiN_x can vary between 3 – 11 MV/cm, depending on the quality of the film [22-24]. The fields in the VHEMTs are at the upper limit of the breakdown field even with a rounded corner. To further reduce the electric field, the SiN_x thickness is increased using the rounded corner structure.

Fig. 2.18 shows the field distribution along the trench corner. The peak electric field is reduced to ~9 MV/cm with 100 nm SiN_x. In addition to the peak field in the gate dielectric, it can be observed that the electric field in the semiconductor layer is also reduced with increasing SiN_x which is obvious since thicker SiN_x leads to more voltage drop across the gate dielectric hence reducing the electric field in the semiconductor. It is important to keep the electric field below the critical field of semiconductor as well.

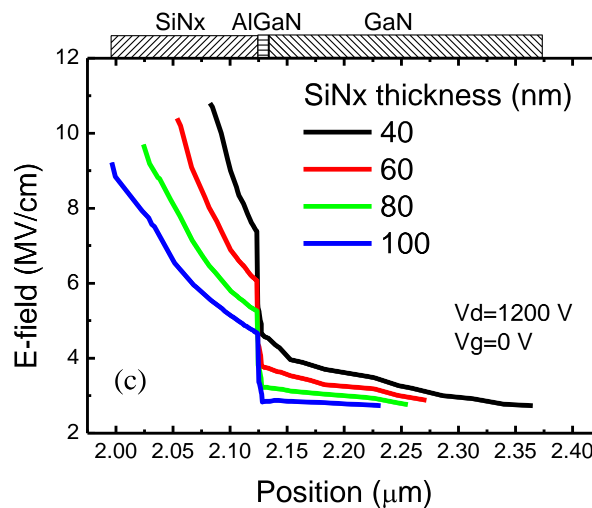

Fig. 2.18 Simulated electric field plotted along the cutline in the rounded corner structure with different SiN_x thicknesses.

To see the trend of the electric field in both layers, the peak field in the SiN_x and GaN layers with different SiN_x thickness are extracted with respect to the applied drain voltage, as shown in Fig. 2.19 (a) and (b). The field in the sharp corner is generally higher than that in the rounded corner as expected. Since the breakdown field of SiN_x is not well defined, we can instead use the breakdown field of GaN (3 MV/cm) to define the V_{br} rating of the device.

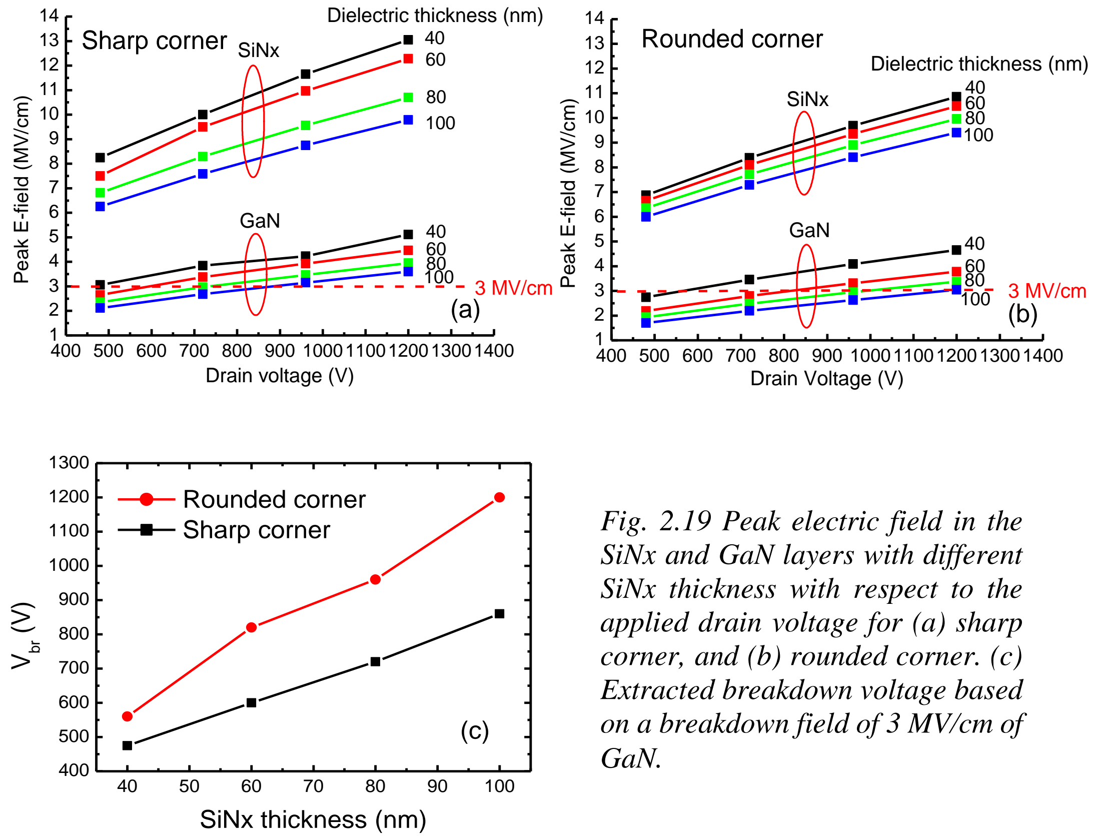

Fig. 2.19 Peak electric field in the SiNx and GaN layers with different SiNx thickness with respect to the applied drain voltage for (a) sharp corner, and (b) rounded corner. (c) Extracted breakdown voltage based on a breakdown field of 3 MV/cm of GaN.

Note that the 3 MV/cm criteria is only a crude estimation of the breakdown field which may not reflect the real impact ionization process described by $M = \frac{1}{1-\int_0^x \alpha dx}$ as the ionization multiplication factor M depends on the integral of ionization coefficient α over a distance, thus the avalanche breakdown cannot be directly translated from the electric field of a single point. Whilst the theoretical critical electric field is estimated about 3.35 MV/cm, the actual breakdown field reported in the literature is about 2.7–3.1 MV/cm using bulk GaN substrates [25,26]. The deterioration is caused by leakage either through the bulk defects or through the edge termination [27]. Therefore, a breakdown field of 3 MV/cm is assumed to extract V_{br}. Fig. 2.19 (c) compares the V_{br} in sharp and rounded corner structures with respect to the SiN_x thickness. A V_{br} of 1200 V is estimated for the rounded corner structure with 100 nm SiN_x whereas the V_{br} is limited below 850 V for the sharp corner structure. Further increasing SiN_x thickness is undesirable as it will result in poor g_m (Fig. 2.15).

Lastly, changing *t_penetration* is also observed to have a great impact on the peak electric field. As shown in Fig. 2.20, the electric field is reduced by moving the corner towards the p-GaN CBL layer. One apparent reason is the increased distance between the gate and drain. More importantly, it is also affected by the depletion region of the P-N junction, the same region that reduces the on-state current as discussed in section 2.3.2. The depletion region around the corner can reduce the electric field and protect the gate. Hence the trade-off of V_{br} and R_{on} is a key design issue to be considered.

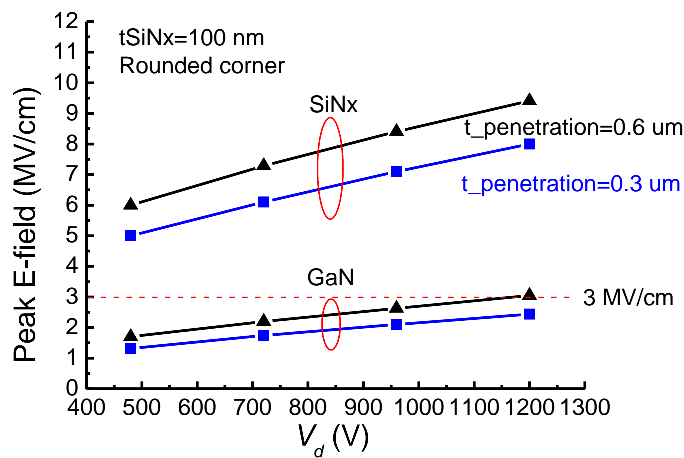

Fig. 2.20 Peak electric field in the SiN_x and GaN layers with different penetration depth with respect to the applied drain voltage for a rounded corner with 100 nm SiN_x gate dielectric.

2.4 Summary

The basic models for AlGaN/GaN (MIS)HEMTs such as the 2DEG formation mechanism and derivation of V_{th} is discussed with the aid of a band diagram. Based on the understanding, a novel VHETM structure is proposed using a (11-22) semi-polar GaN substrate. TCAD simulation discovered a sudden decrease of g_m and increase of on-state resistance which is caused by the aperture resistance which can be modelled by a cascode structure. It is found that moving the trench away from the depletion region can alleviate the issue but can result in an increased electric field at the trench corner. The breakdown voltage of the device is

monitored as a function of electric field. The breakdown voltage can be increased by (1) rounding the trench corner, (2) increasing the gate dielectric thickness or (3) moving the trench corner towards the p-GaN CBL. A breakdown voltage of 1200 V is achievable by optimizing the device, however, the trade-off between V_{br} and R_{on} is a key design issue to be considered.

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Chapter 3 Fabrication and Characterization of VMOSFETs and VHEMTs $(11\bar{2}\bar{2})$ Using Semi-polar GaN

In this chapter, the detailed fabrication process and the characterization results of VMOSFETs and VHEMTs are presented. To avoid the plasma damage which is usually seen in dry etching process, wet etching is preferred. However, due to the atomic bond configuration, (0001) c-plane GaN is almost immune to any chemical etching unless a photo-enhanced chemical (PEC) etching method is used [1]. Alternatively, GaN layer grown in semi-polar or non-polar directions can be etched by KOH solution without the aid of UV light. Among the various wafer orientations, the (11-22) semi-polar GaN was chosen for the study because of the relative orientation with respect to the c-plane. The (11-22) plane is ~58.3° from the c-plane as shown in Fig. 3.1 and is widely used in LED research to alleviate the quantum-confined stark effect caused by the strong polarisation field. These efforts have made bulk substrates with low dislocation density ($<5\times10^{6}$ cm^{-2}) available which is essential for realizing high blocking voltages.

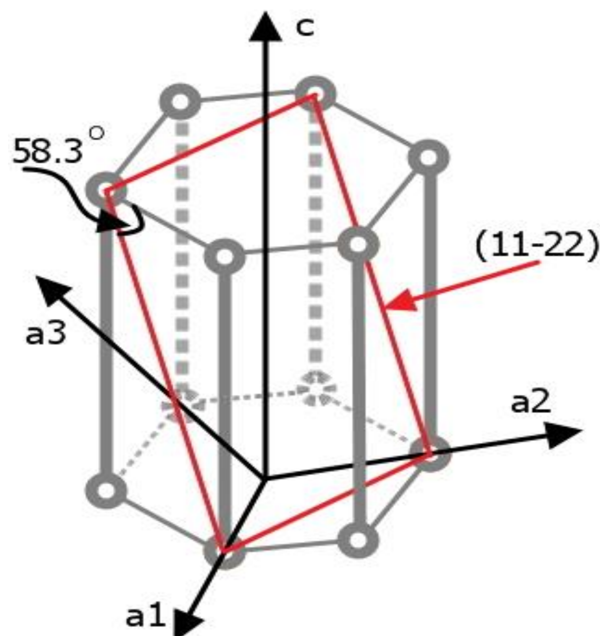


Fig. 3.1 Schematic structure of GaN unit cell showing the (11-22) plane.

Due to the novelty of the design, the materials under investigation are grown on a more commonly available (10-10) m-plane sapphire substrate by metal-organic chemical vapour deposition (MOCVD) with the help from colleagues at University of Cambridge. The wafers were subject to an initial V-groove etching and sent to University of Cambridge for MOCVD regrowth or University of Nottingham for MBE regrowth. MBE is the preferred regrowth method due to its relatively lower growth temperature to avoid mass transport effect which will be covered in the next section. The regrown samples are studied by scanning electron microscopy (SEM), transmission electron microscopy (TEM) and energy dispersive X-ray spectroscopy (EDS). Finally, a full device fabrication is carried out followed by electrical measurements.

3.1 Crystallographic KOH Etching and Overgrowth

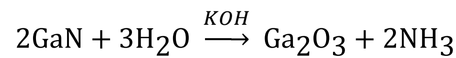
3.1.1 KOH etching of (11-22) GaN

In order to establish the etching process, a simplified structure with 3 µm semi-insulating (SI) GaN was grown on (10-10) m-plane sapphire by MOCVD. GaN grown on sapphire typically suffers from poor crystal quality due to the lattice mismatch between (11-22) GaN and m-plane sapphire substrate [2-5]. In order to improve the crystal quality, an AlN interlayer technique was employed as described in [6]. First the sample was pre-cleaned in the reactor in a H_2 ambient. Next, a pulsed nucleation layer of 25 nm GaN was grown at 800 ˚C, followed by a continuous growth of 700 nm GaN at 1080 ˚C. A 15 nm AlN interlayer was subsequently grown at 1080 ˚C, followed by approximately 2.3 um of GaN. The purpose of the AlN interlayer was to act as a dislocation reduction layer, as well as a getter for unintentional oxygen incorporation in semi-polar crystals. The wafers typically contain a threading dislocation density about 10^9 cm^{-2} and a basal plane stacking fault density in the 10^5 cm^{-1} regime.

Prior to wet etching, 200 nm SiN_x was deposited by PECVD as a hard mask. The sample was patterned by standard photolithography with the long edge orientated along the [1-100] axes

(Fig. 3.2) to obtain the c-plane sidewall. Reactive ion etching was performed to open the windows on the SiN_x for wet etching. Subsequently, the sample was etched in 4 M KOH solution at 90 °C for 20 minutes with an etch rate of ~98 nm/min. Lastly, the SiN_x mask was removed by hydrofluoric acid.

The KOH etching of (11-22) GaN has been widely investigated in LED applications and the chemical reaction mechanism and the resulting surface morphology are well understood in the literature [7-10].The hydroxide ions (OH^-) react with surface GaN atoms following the reaction:



$$2GaN + 3H_2O \xrightarrow{KOH} Ga_2O_3 + 2NH_3$$

where KOH acts as a catalyst as well as a solvent for the resulting gallium oxide. However, due to the presence of three negatively charged dangling bonds of nitrogen (N) atom at the surface of c-plane GaN, the surface is completely screened and OH^- ions are prevented from accessing the surface. Therefore, Ga-face c-plane GaN is almost immune to KOH and etching is only observed along defects and dislocations [11]. Semi-polar and non-polar planes can be etched by KOH but the etch rate can vary according the atom configurations. For example, the (1-100) m-plane is more stable than the (11-22) plane as more negative dangling bonds are presenting at the m-plane surface [10].

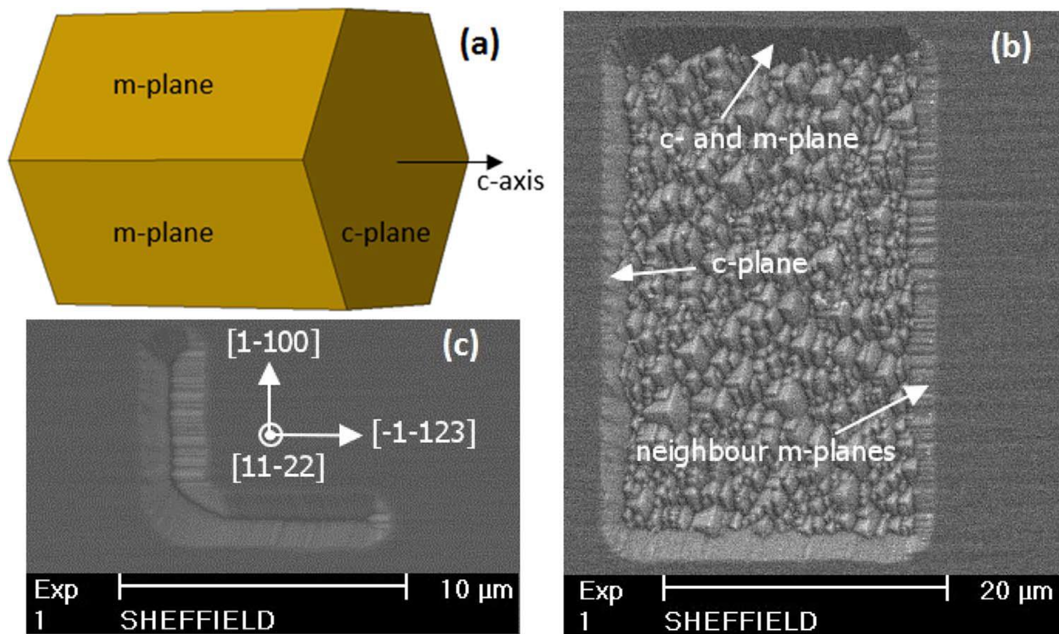


Fig. 3.2 (a) The schematic structure of a unit cell of wurtzite GaN oriented in [11–22] direction showing the crystallographic planes of the facets. The SEM images of the etched sample in the (b) 22 µm opening region and (c) 2 µm opening region. All figures are aligned in the same orientation.

Fig. 3.2 (a) illustrates the top view of a unit cell of wurtzite GaN orientated in [11-22] direction. Fig. 3.2 (b) shows the SEM images of the etched region with an opening length of 22 µm which can be used to identify the crystal planes of the facets revealed by the wet etching. Typical trigonal prism cells consisting of a c-plane and two m-plane facets from the m-plane family are observed in the central region. The crystallographic planes of the sidewalls can be identified from the prism-shaped features in Fig. 3.2 (b) as well as that illustrated in Fig. 3.2 (a). In detail, a c-plane facet is obtained on the left sidewall. The top and bottom sidewalls consist of c- and m-plane facets are arranged in a step-like manner, whilst two m-plane facets are found on the right sidewall.

In comparison, the etching revealed a V-groove with a reduced opening width of ~2 µm shown in Fig. 3.2 (c). The samples in Fig. 3.2(b) and (c) are in the same orientation, but due to the reduced opening width, the (11-22) plane is fully masked by the slow etching c- and m- planes where an etch-stop is achieved. In this way, as the slopes of both sidewalls are fixed, the etch depth can be controlled by the opening width, which is more reliable compared to a time-

based etching. In addition, another V-groove is formed in the perpendicular direction due to a similar mechanism. However, when the sample is significantly over-etched, the resulting feature size can become larger than the as-patterned size due to a further lateral etching (most likely in the m-plane) but at a significantly reduced etch rate compared to the (11-22) plane. After dipping in a buffered HF solution, the samples are ready for regrowth.

3.1.2 MOCVD regrown

After the V-groove etching, the channel regrowth was initially performed by MOCVD. The wafer was first heated up to 1030 ˚C in NH_3. Then 100 nm of GaN was grown followed by 25nm of AlGaN. The wafer was then cooled down in NH_3. The V/III ratio used was reasonably low (~900) to promote lateral overgrowth. The top-view SEM image is shown in Fig. 3.3 (a). Unexpectedly, an “etching” effect is observed resulting in a cavity in the c-plane sidewall. In the meantime, the top/bottom and right sidewalls are planarized which are thought to be the intersections of the two facets before regrowth. It is believed that the high temperature during heating up results in de-composition of GaN and a possible mass transport effect [12,13] which causes the “etching” effect. A cross-sectional TEM image was taken on the right sidewall as shown in Fig. 3.3 (b). No AlGaN was observed even after switching on the source gases.

In order to alleviate the “etching” effect, another regrowth was performed with growth temperature lowered to 950 ˚C with other growth conditions kept the same. The SEM and TEM images are shown in Fig. 3.3 (c) and (d), respectively. This time, the “etching” effect is greatly reduced but the c-plane sidewall remains rough. An AlGaN layer with an Al fraction ~20% and a thickness of ~50 nm is observed by TEM-EDX (not shown). Clearly, the “etching” effect needs to be improved further. However, further lowering the growth temperature could result in un-controlled carbon incorporation and poor crystal quality in the regrowth structure. Hence the MOCVD regrowth was not pursued further.

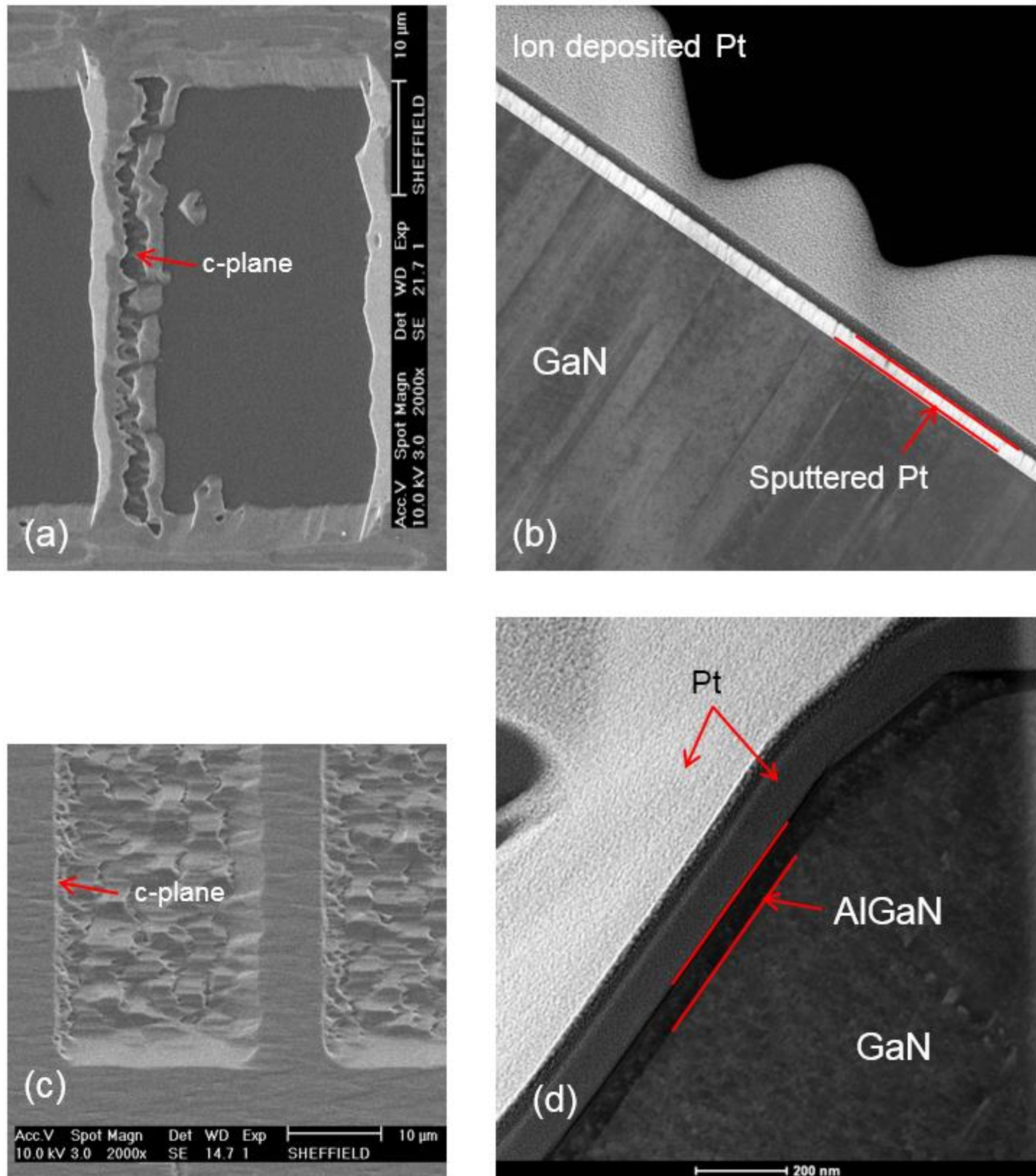


Fig. 3.3 (a) SEM image and (b) cross-sectional TEM image of sample regrown at 1030 ˚C. (c) SEM image and (d) cross-sectional TEM image of sample regrown at 950 ˚C.

3.1.3 MBE regrowth

MBE was chosen for the regrowth due to its relatively low growth temperature to avoid mass transport at the high temperatures (~1000 ˚C) during MOCVD growth. In addition, it prevents the Mg from diffusing from p-GaN CBL into the regrown UID-GaN channel region which may upset the 2DEG mobility. Also, the hydrogen-free environment of the MBE growth prevents passivation of the exposed CBL during regrowth. In order to verify the feasibility of

MBE regrowth, the sample was transferred (in air) to a plasma-assisted molecular beam epitaxy (PA-MBE) chamber for the regrowth of 100 nm UID-GaN and 20 nm AlGaN at approximately 750 °C with N_2 flow of 1 sccm and RF power of 200 W. The growth was under Ga-rich conditions with a Ga beam equivalent pressure of 2.1×10^{-7} Torr to ensure a smooth growth. The Al/Ga ratio during AlGaN growth was approximately 1:4 aiming for 20% Al fraction.

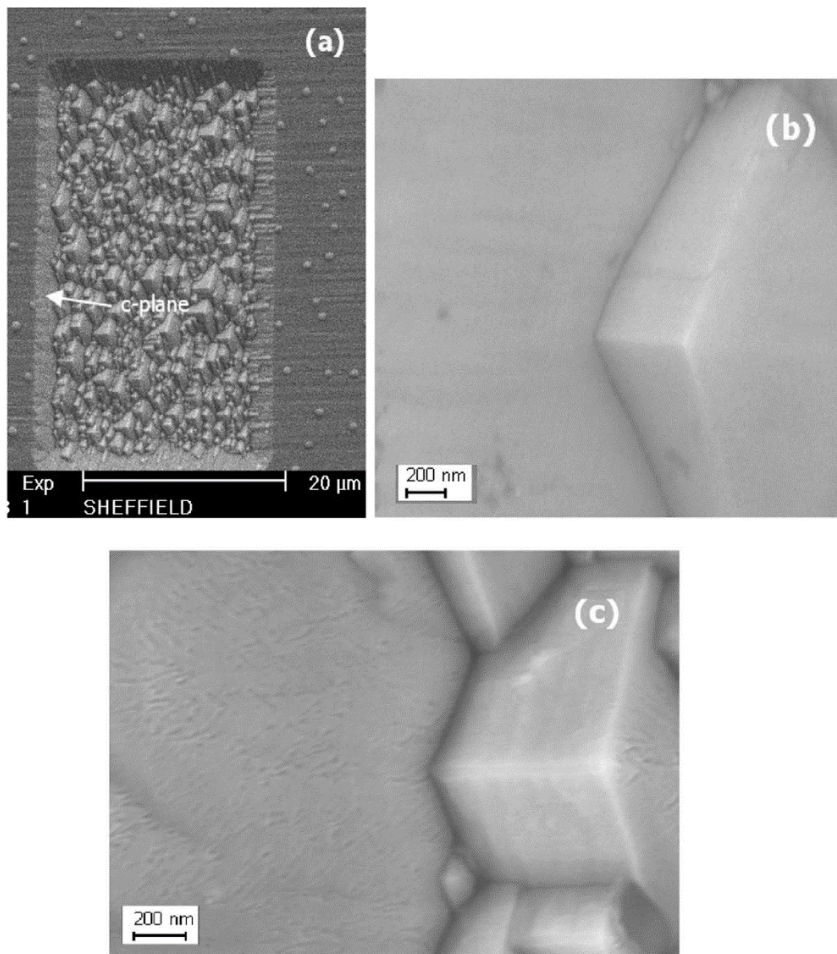


Fig. 3.4 (a) The SEM images of etched (11-22) GaN after MBE regrowth under Ga-rich conditions. The high resolution SEM image of the c-plane sidewall (b) before regrowth, and (c) after regrowth.

The SEM image after the regrowth is shown in Fig. 3.4 (a). In contrast to the MOCVD regrowth, the surface morphology is less modified (i.e. no material decomposition or mass transport occurred). In comparison to the surface before regrowth (Fig. 3.2), the formation of

Ga droplets can be observed which is expected from the Ga-rich growth conditions. Fig. 3.4 (b) and (c) present high magnification SEM images of the c-plane sidewall before and after regrowth, respectively. Small fissures can be observed on the c-plane surface after regrowth which are thought to be caused by the stress in the AlGaN layers.

Fig. 3.5 shows the cross-sectional TEM image of the c-plane sidewall with EDS mapping showing the fraction of the Ga and Al atoms. No discernible interface is observed at the interface between underlying GaN and regrown GaN which is an indication of the good quality of the etched surface achieved by wet etching. A uniformly grown 20 nm AlGaN layer with a smooth interface with the underlying GaN is observed which is essential for the formation of high mobility 2DEG.

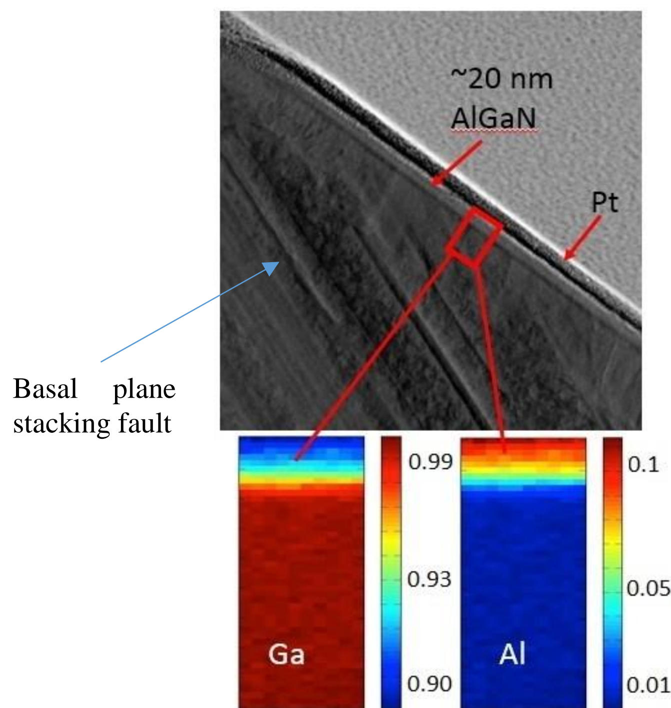


Fig. 3.5 The cross-sectional TEM image of the regrown c-plane sidewall with EDS mapping showing success growth of $Al_{0.1}Ga_{0.9}N$.

The aluminium mole fraction in the AlGaN layer is 10(±2)% determined by EDS which is less than the target composition of 20 %. This could be due to the local flux variation and different material incorporation within the trench compared to a planar growth. The thickness and Al

fraction in the AlGaN layer are important in controlling the 2DEG and hence the V_{th} of the device. It provides the opportunity for enhancement-mode operation by optimizing the regrowth conditions. Although the 10% Al in AlGaN is somewhat lower than our expected value, it serves as a clear evidence of successful regrowth of AlGaN layer. These results are very encouraging and suggest that MBE is a suitable method for the regrowth process.

3.1.4 Discussion

Whilst the KOH etching results are consistent with many published results [8-10], it is noticed that the slope of the c-plane facet is actually shallower than the predicted 58˚ slope. This can be inferred from the horizontal lengths of the sidewalls (Fig. 3.2). For an ideal c-plane, a ratio of ~1:3 is expected from the slopes of the c-plane and m-plane sidewalls. However, the actual ratio is 1:1.3 which indicates a shallower angle than a c-plane sidewall. In addition, it is clear from Fig. 3.5 that the slope is different from the basal plane stacking faults which are known to be 58˚ (i.e. follow the c-planes). Fig. 3.6 shows the atomic force microscopy (AFM) scan image on the sidewall. A slope of ~35.7˚ is extracted from the line profile which runs perpendicular to the edge as indicated by the blue line. The opposite m-plane sidewall is ~32˚ (not shown) which agrees with the expected value.

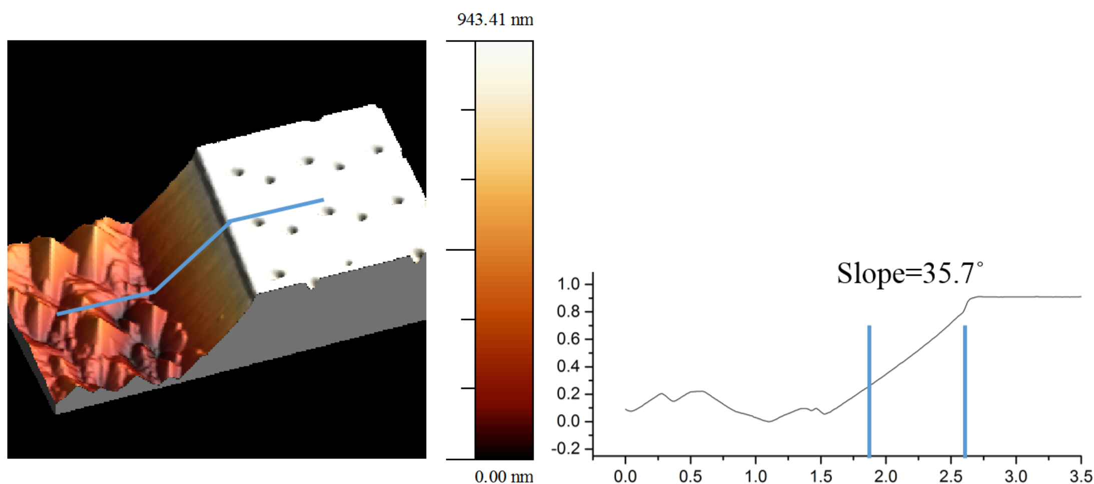


Fig. 3.6 AFM image of the c-plane sidewall with the sidewall sloped extracted from the line profile as indicated by the blue line.

In addition to the sidewall, the "c-plane" facet of the prism features at the bottom of the trench is also shallow at ~42˚. A tilted SEM view of the prism features shows a curved profile on the "c-plane" facets, as shown in Fig 3.7 (a). This curving was also observed in [9,10] but it was not discussed in detail.

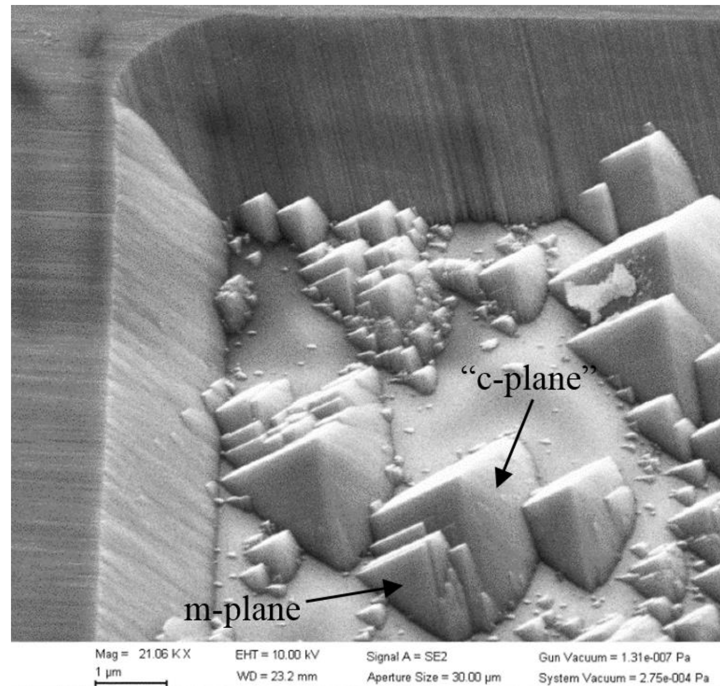


Fig. 3.7 Tilted SEM image of KOH etched (11-22) GaN which is partly etched down to sapphire substrate.

In order to interpret the origin of the shallower slope, it is necessary to understand the progression of the etching process. Fig. 3.8 depicts the schematic cross-sectional structure during etching. At stage 1, a few monolayers of the top surface is removed, exposing the prism hillocks. At this stage, since the c- and m-plane facets are slow etching, there must be a fast etching point which allows an etch rate of 90 nm/min. It can be deduced that the apex of the hillocks is the most vulnerable point to OH^- since it is in the transition between c- and m-plane, and is surrounded by OH^- from a wide direction. Removing the apex tends to expose the fast etching semi-polar plane which is immediately etched and progresses to the next available c- and m-plane facets (stage 2). Subsequently, as the apex moves into close proximity to the c-plane facet, the negative electric field from the surface charge counter-balances the diffusion

force of OH^- and the apex is preserved (stage 3). Lastly, a "staircase" structure is formed on the sidewall (stage 4). While each c-plane step is of an angle of 58˚, the overall slope is reduced depending on the ratio between the c- and m- steps.

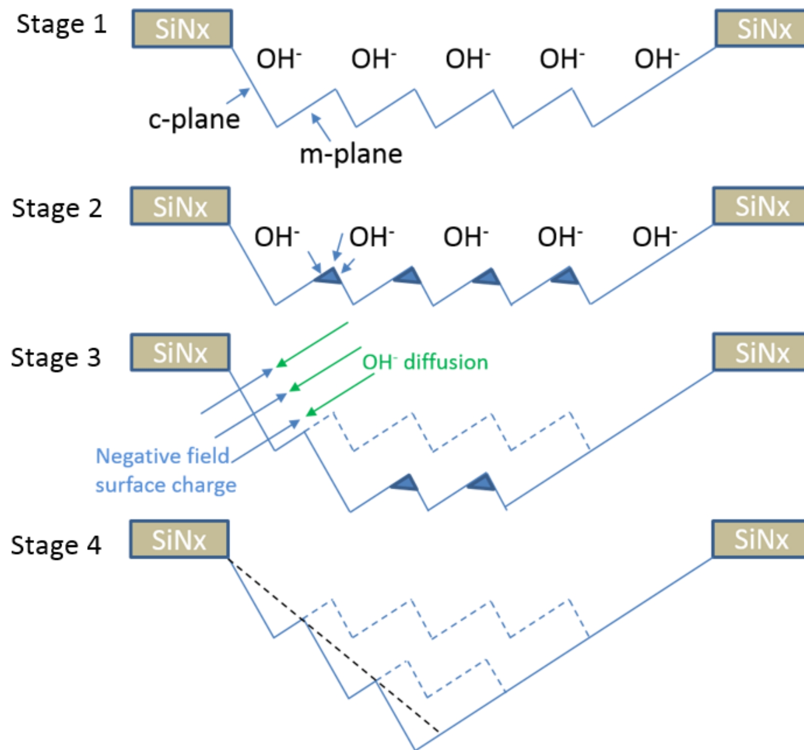


Fig. 3.8 (a) Schematic representation of the etching process of (11-22) GaN to illustrate the mechanism of the shallower sidewall.

One way to achieve the correct slope is by increasing the OH^- concentration. The increased concentration gradient will result in higher diffusion force hence reducing the size of the m-step. In agreement with the above analysis, the sidewall slope was increased to 41˚ when the KOH solution was increased to 30 M which is about the maximum concentration for KOH at 90˚. It is clear that the OH^- concentration need further increase. This can be achieved by using NaOH as an etchant since the solubility of NaOH in water is about twice of that of KOH. In our latest experiment, the correct slope of 58˚ was achieved in the sample etched in 60 M NaOH solution at 90 ˚C.

3.2 Fabrication of VHEMT Structures

After establishing the regrowth process, a complete VHEMT device is fabricated. In detail, the structure is grown on m-plane sapphire substrate by MOCVD. The structure starts with a 1 μm heavily doped (Si: ~10^{18} cm^{-3}) n^+ GaN spreading layer followed by 3 μm lightly doped (Si: ~10^{16} cm^{-3}) n^- GaN drift layer and 0.5 μm p-GaN CBL. The growth is interrupted at the p-GaN and an activation annealing is performed at 800 ˚C for 20 minutes in the MOCVD chamber as an attempt to break the Mg-H bonds and drive out the H_2 to achieve higher hole concentration in the p-GaN layer. Subsequently, a 0.5 μm top n^+ GaN (Si: ~10^{18} cm^{-3}) contact layer is grown in-situ.

An initial KOH etching experiment (4M KOH at 90 °C) revealed that the etch rate of p-GaN is less than 10 nm/min which is approximately 6 times slower than the n-type GaN. Park and Lee [14] observed a similar dopant dependent etching phenomena where the wet etching activation energy was found to be the highest for Mg-doped (11-22) GaN (compared to Si-doped and UID layers) which was attributed to the downward band banding and negative charge accumulation at the surface region causing a repulsion to the OH^- ions. This behaviour has prevented us from using a simple one step wet etching since an extended etching time (>30 min) would cause the KOH diffuse into the SiN_x/GaN interface and create an undercut at the surface region. Therefore, a dry followed by wet etching process was adopted in all VHEMT structures.

The fabrication process flow is shown in Fig. 3.9 (a)-(f). Firstly, a 200 nm SiN_x hard mask deposited by PECVD (a). The opening is patterned along the (1-100) direction using standard lithography. Prior to the wet etching, the top n^+ GaN and p-GaN CBL are completely etched away using ICP (b). The sample is then dipped into 4M KOH at 90 °C for 10 minutes to form the V-groove and the SiN_x is removed by buffered HF (c). The sample is then transferred to MBE chamber for an AlGaN/GaN (25/100 nm) channel regrowth (d). After a number of ICP etching to access the respective layers (e), Ti/Al/Ni/Au (20/100/25/45 nm), Ni/Au (20/20 nm)

and Ni/Au (20/200 nm) metal stacks are thermally evaporated to form the contacts to n-GaN, p-GaN and gate, respectively (f). Lastly, the device is passivated with 200 nm SiO_2 deposited by PECVD and finished with bond pad metallization (not shown). The source and p-GaN are connected together and grounded to provide a charging/discharging path in the p-GaN.

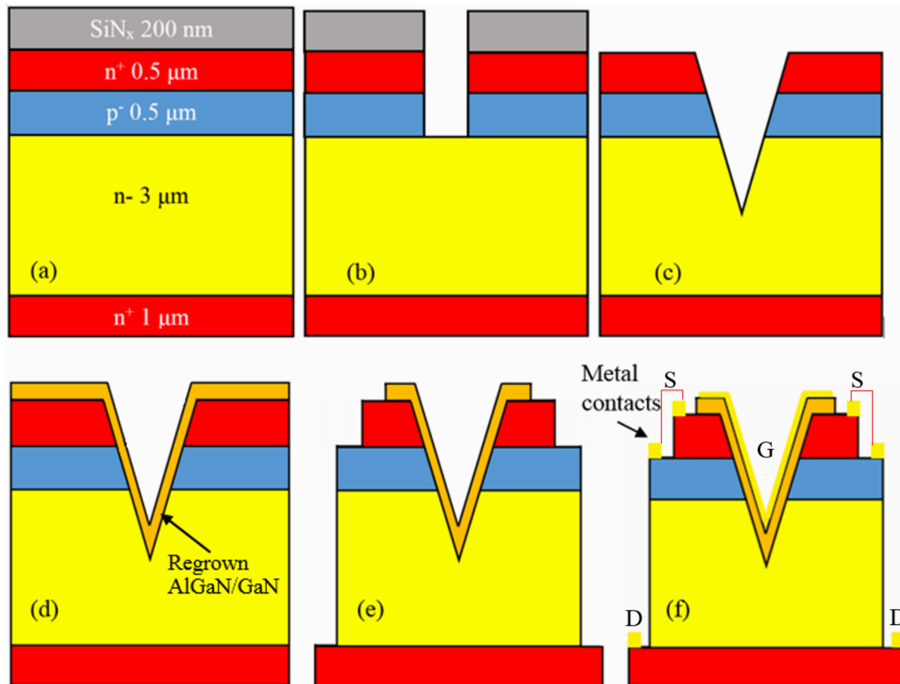


Fig. 3.9 Processing steps of a VHEMT device.

3.2.1 Structural analyses

Prior to the electrical measurement, SEM and TEM images are taken after the regrowth (stage d) to characterize the device structure. The top view SEM image is shown in Fig. 3.10 (a) which consists a V-groove in the centre surrounded by rough edges. The rough edge is caused by an undercut when KOH gets into the GaN/SiN_x interface during the etching process. The enlarged image reveals some fissuring on the regrown surface and formation of Ga droplets.

A surprising result is observed by TEM as shown in Fig. 3.10 (b). The slopes of the sidewalls are significantly sharper than the expected c- and m-plane although the sidewalls are relatively smooth. Moreover, the slope persists even after a prolonged etching time which indicates the formation of other chemically stable planes. The diagonal lines that extend all the way from

the sapphire substrate to the surface are the basal plane stacking faults which are ~58° from the surface (i.e. parallel to the c-plane). From the stacking faults, it is clear that the right sidewall has deviated from the c-plane by ~16°. The deviation from c-plane can result in a reduced polarisation field and 2DEG and it is still unclear how much influence it may have. M. Okada, etc. [15,16] reported a vertical HFET structure where a 2DEG is formed on a sloping surface with an angle of about 16° from c-plane which suggests that it is possible to form a 2DEG on the sidewall. However, a one-step wet etching would be preferable to achieve the correct slope. A photo-enhanced chemical (PEC) etching technique may be used to accelerate the etching of p-GaN.

The enlarged image in Fig. 3.10 (b) shows the magnified trench corner region where shallower angles are obtained. With respect to the stacking faults, the left sidewall is perpendicular and the right sidewall is parallel which conform to the expected m- and c-plane, respectively. In addition, instead of a sharp corner, a rounded curvature with a diameter of ~80 nm is observed which is beneficial for reducing electric field. Fig. 3.10 (c) shows the compositional mapping of the corner area by EDS. The Al mole fraction is measured to be ~10 at% with a thickness of ~25 nm, similar to the results in section 3.1.3.

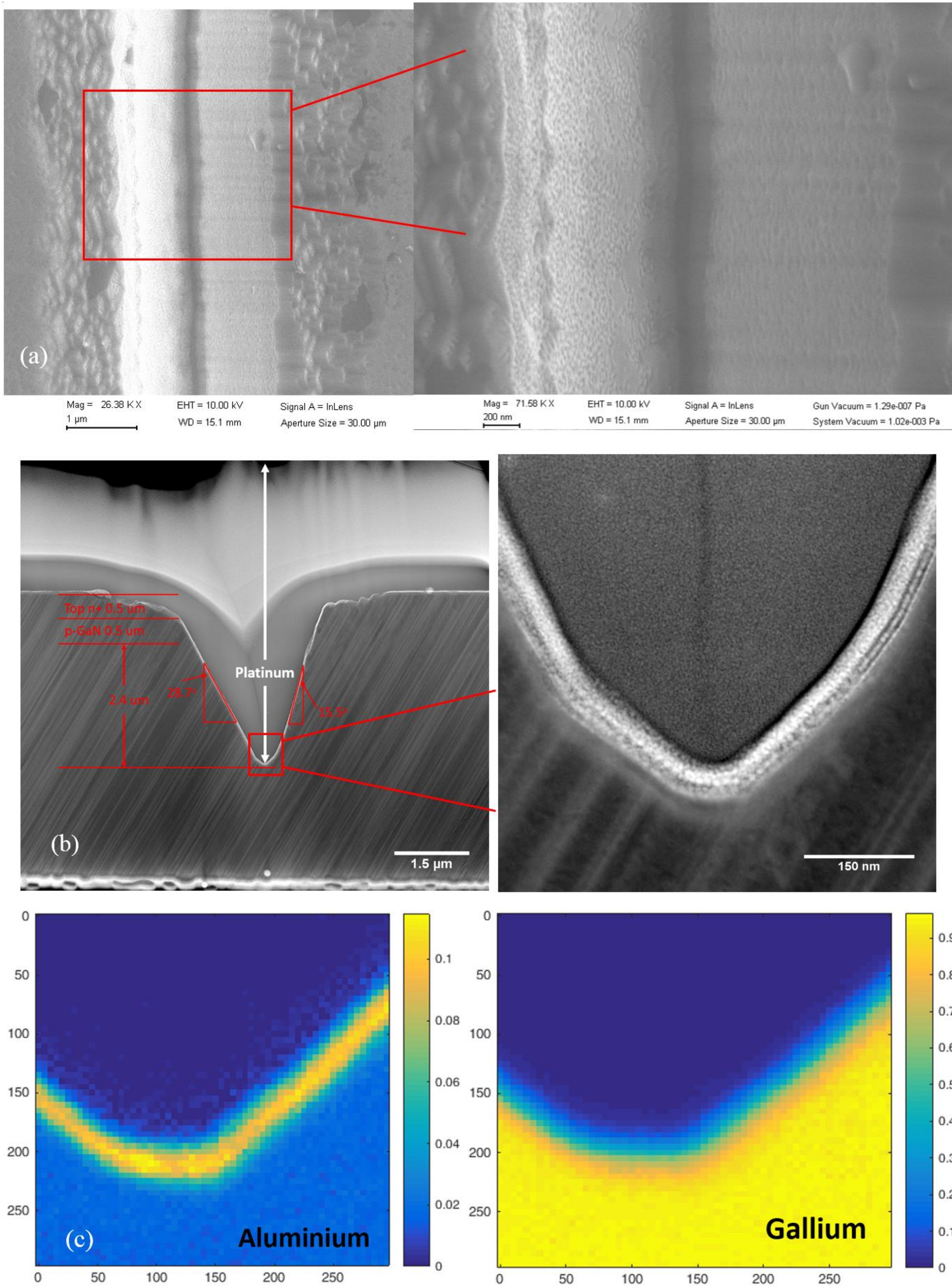


Fig. 3.10 (a) Top view SEM image with an enlarged central region of the V-groove after regrowth, (b) cross-sectional TEM image with an enlarged view of the corner after regrowth and (c) EDS mapping showing the Al and Ga fraction in the regrown structure.

3.2.2 Electrical characterization

To gain a better understanding of the device, each layer of the structure is characterized by a circular transmission line model (CTLM) structure. As shown in Fig. 3.11 (a) and (b), the top and bottom n^+ GaN layers are highly conductive with contact resistances (R_C) between 0.8 and 1.0 Ω-mm and sheet resistances (R_{sh}) of 40 and 120 Ω/sq, respectively. However, a non-ohmic behaviour is observed in the drift layer, as shown in Fig. 3.11 (c), which could be due to the low doping concentration in the layer. Due to the non-ohmic nature of the contacts, it is difficult to obtain a reliable R_{sh} value but it is estimated to be around the level of 70 kΩ/sq. The reason for the high resistance value is still under investigation but could be solved by simply increasing the SiH_4 gas flow during the growth conditions.

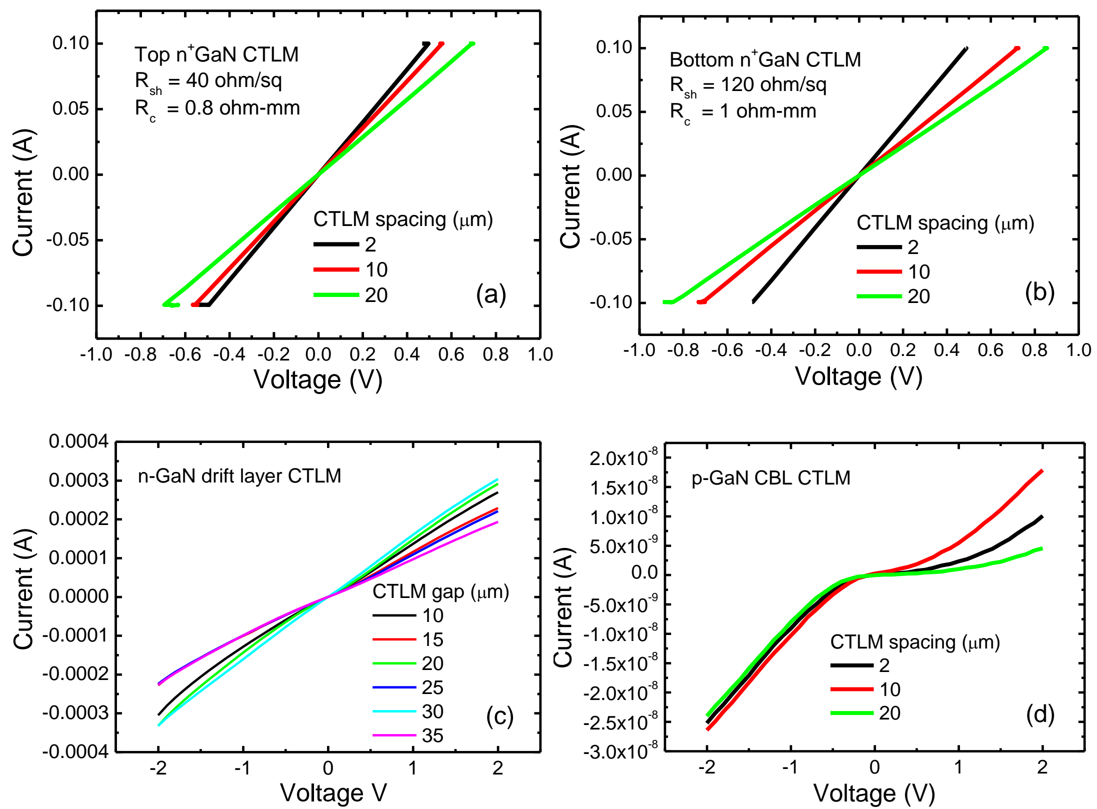


Fig. 3.11 CTLM measurement results of (a) top n^+ GaN contact layer, (b) bottom n^+ GaN spreading layer, (c) n^- GaN drift layer, and (d) p-GaN CBL.

Fig 3.11 (d) reveals the current through the p-GaN CBL in the CTLM structure. A rectifying behaviour together with a low current level (in nano-Amperes) is observed. The poor electrical

conductivity can be due to poor p-type ohmic contacts in addition to a high sheet resistance as a result of low effective hole concentration. Several groups reported a lower Mg incorporation efficiency in (11-22) GaN compared to the c-plane GaN [17-19]. Moreover, although the p-GaN is activated using an interrupted growth technique, it is impossible to avoid H_2 incorporation (either from H_2 carrier gas or NH_3) during the top n^+ GaN growth which can serve to passivate some of the Mg. The p-GaN layer not only acts as a current blocking layer, but also provides a charging/discharging path for the P-N junction which is essential for realizing high blocking voltages. Therefore, more work is needed in the future to improve the electrical performance of p-GaN and the p-type ohmic contacts.

In the vertical structure, the large drain voltage is mostly sustained by the P-N junction. Therefore, it is important to understand the P-N junction characteristics of the VHEMT device, especially the reverse bias leakage characteristics. The *I-V* characteristics of the P-N junction is measured by probing the p-GaN CBL and the bottom n^+ GaN as shown in Fig. 3.12 (a). Despite the low conductivity in the p-GaN, diode behaviour is observed. In the reverse bias, the leakage current is insignificant (< 5 nA) up to -5 V. However, the reverse leakage current increases rapidly with reverse biases larger than 5 V as shown in Fig. 3.12 (b). There are two possible leakage in the structure. Firstly, the mesa sidewall is subjected to plasma damage during the dry-etching process resulting in a leakage path. Another possibility is punch-through effect in the bulk p-GaN due to the low hole concentration. The detailed characterization of leakage current will be studied in section 3.3.2.

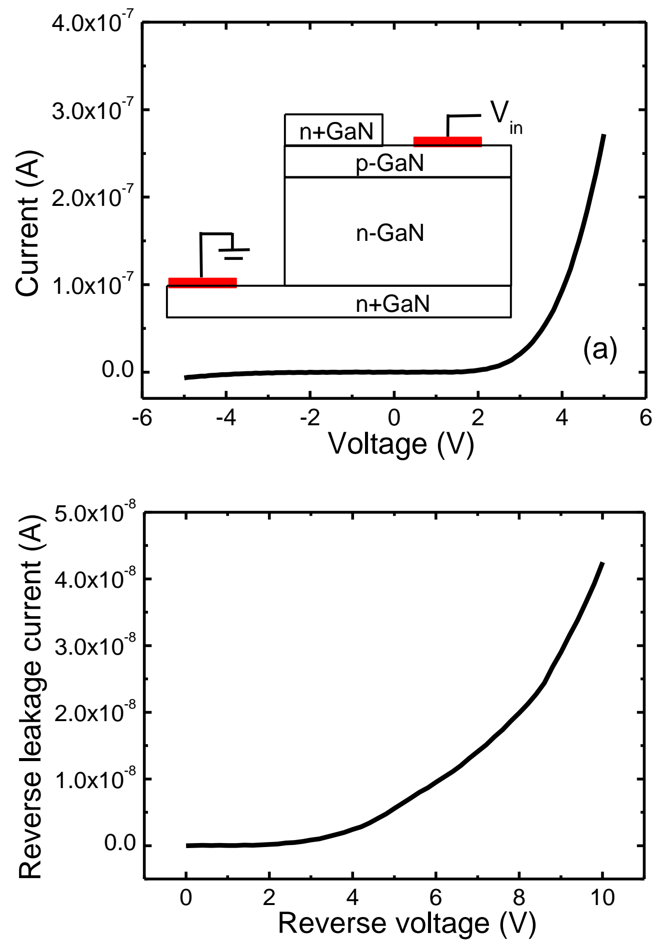


Fig. 3.12 (a) Current voltage characteristics of the P-N junction. The inset shows the overall device structure. (b) Reverse leakage characteristics on a linear scale.

By far, one of the biggest challenges in characterizing the VHEMT is to establish the 2DEG property. Since the 2DEG only exist on the c-plane sidewall whose size is only 1-2 μm, it is very difficult to make measurements using the traditional methods, such as Vann Der Pauw Hall structure and TLM since it is difficult to rule out the contribution from other regions. To study the property of the regrown layers, the vertical conductivity (between drain and source) of the structures with and without the regrown layers is compared. In the measurement, the gate is left floating to avoid any leakage current from the gate. As shown in Fig. 3.13, the current remains low before regrowth and the current is increased by 3 order of magnitude after regrowth. It should be emphasized that the leakage current through the p-GaN CBL remains low after regrowth which indicates that the conduction path is provided by the regrown layers.

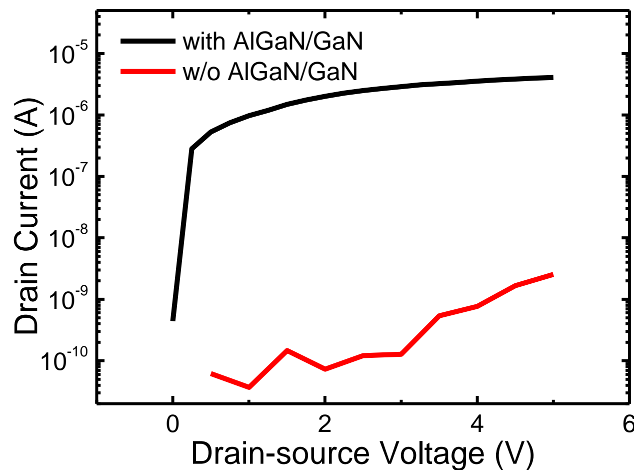


Fig. 3.13 Comparison of drain current in structures with (black) and without (red) the regrown AlGaN/GaN layers with the gate is floated.

However, there are two possible sources of conduction - the 2DEG and/or background doping. In this case, it is likely that the conduction is dominated by the background doping for two reasons. Firstly, the Al fraction in the AlGaN barrier is only 10% and the sidewall is 16˚ off the c-plane, therefore, it is unlikely to achieve the level of polarisation field as one would expect in a HEMT device. Secondly, a Hall effect measurement was performed on a calibration GaN layer (without an AlGaN or 2DEG) grown on sapphire by MBE. The sample shows n-type doping with an electron concentration between $2 - 5\times10^{17}$ cm^{-3} from the background doping. It is believed that the regrown layers in the VHEMT are doped to a similar level to form a major source of conduction.

To further characterize the transistor behaviour, a gate sweep is applied to obtain the device transfer characteristics. However, a high reverse gate leakage current is observed as shown in Fig. 3.14. Because of the leakage, there is no gate modulation on the channel conductivity. The high reverse leakage current may be caused by tunnelling through a thinner Schottky barrier due to the high level of n-type doping in the regrown layers. Another possibility may be the leakage through defects at the metal/semiconductor interface, such as the pits and fissures, as well as dislocations which can act as recombination centres or intermediate states facilitating the trap-assisted tunnelling process [20].

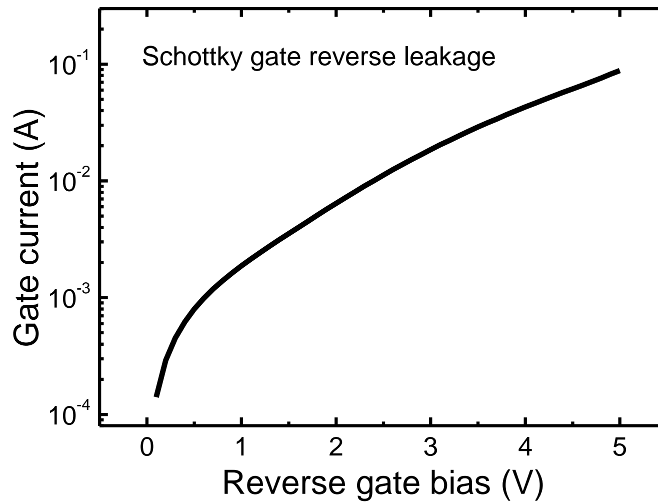


Fig. 3.14 Typical gate reverse leakage current on a semi-log scale with a gate length of 1.5 μm and gate width of 50 μm

3.3 Demonstration of VMOSFETs

At the same time as evaluating the VHEMT structures, a simpler structure – VMOSFET was fabricated to establish a transistor behaviour. The Si VMOSFET was first proposed in the 1970s which features many advantages such as simple processing, high packaging density and short channel (thus smaller gate capacitance) with higher breakdown voltage than conventional (lateral) MOSFETs [21,22]. This work is the first demonstration of VMOSFET using the semi-polar (11-22) GaN.

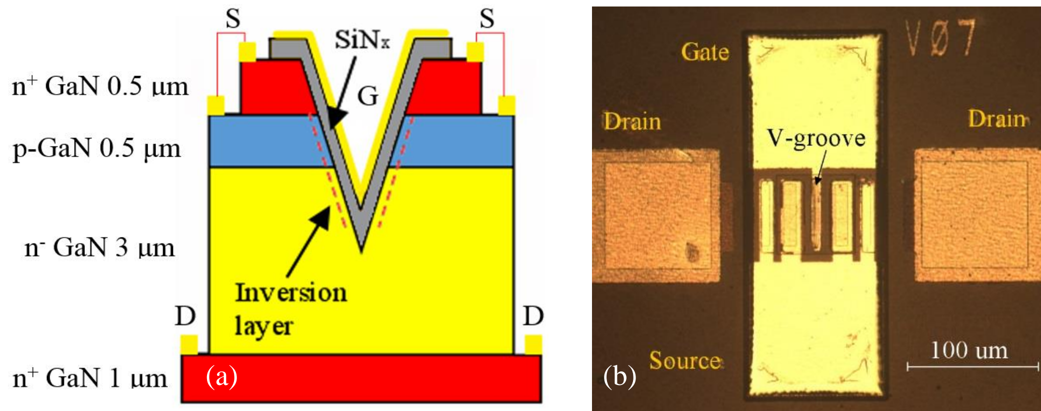


Fig. 3.15 (a) Schematic structure of the VMOSFET. (b) Optical image of the device.

The schematic device structure and the optical image of the fabricate device are shown in Fig. 3.15 (a) and (b), respectively. The concept is the same as the classical Si VMOSFET such that an inversion layer is induced by a gate bias to support the conduction along the sidewall. The device fabrication process is very similar to that of the VHEMT which is described earlier in section 3.2, except that a 20 nm SiN_x gate dielectric is deposited by PECVD on the V-groove (instead of the AlGaN/GaN channel) after the V-groove etching. Here SiN_x is chosen for the first demonstration of transistor. Other choices of gate dielectric materials, such as HfO_2, SiO_2, Al_2O_3, etc., can be explored to achieve better performance in the future.

3.3.1 Initial characterization

Fig. 3.16 depicts the typical transfer characteristics of 20 devices. Starting from a fresh device, the gate voltage is swept from 0 to 8 V for three consecutive sweeps with the drain bias (V_d) kept at 3 V to avoid leakage through the p-GaN CBL. Based on the V_{th} of the first sweep (2.8 V), a hole concentration of about 3×10^{17} cm^{-3} is calculated under the assumption that no traps/fixed charges exist at the SiN_x/GaN interface. However, given the low conductivity of the p-GaN as observed in section 3.2.2, the hole concentration is unlikely to reach this level. Thus it is likely that net negative charges exist in the gate region which gives rise to the measured V_{th}.

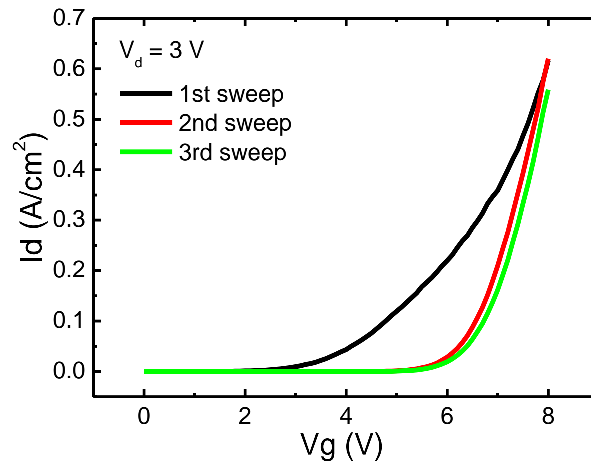


Fig. 3.16 Three consecutive sweeps of transfer characteristics on a linear scale.

It also can be seen that there is a pronounced positive shift in V_{th} from 2.8 to 6.0 V between the first and second sweeps. The V_{th} then saturates at about 6.2 V after the third. The positive V_{th} shift can be attributed to the electrons getting trapped at localized states at the SiN_x/GaN interface or within the bulk SiN_x under a forward gate bias. In addition, the shift is fully recoverable after rest for several hours in room temperature and faster de-trapping under elevated temperature. A similar trapping effect is widely observed in GaN-based MIS-HEMTs [23-27]. It is well known that the GaN surface is susceptible to traps (energy states within the bandgap) which can be due to the presence of poor quality native oxide layer, nitrogen vacancies, dangling bonds or surface impurities such as oxygen and carbon. When a sufficient forward bias is applied to the gate, the conduction band at the semiconductor surface is pulled down below the Fermi-level and a quantum well filled with electrons is formed at the insulator/semiconductor interface. When the forward bias is removed, for an ideal surface without any traps, these electrons would go away instantaneously. However, with the traps, the electrons can get trapped. The trapped electrons are slow to emit thus behave as negative charges, therefore more positive gate bias is required to induce the same amount of channel carriers, giving rise to the positive shift in V_{th}.

In addition to the interfacial traps, electrons can get into bulk traps within the gate dielectric which can also contribute to the shift in V_{th}. So far, there is not a reliable way to quantitatively

distinguish between the two types of traps. Therefore, the total shift in V_{th} could be the result of the combination of the interfacial and bulk traps. However, for traps in the bulk dielectric, the trapping and de-trapping processes tend to be much slower due to the deeper trap energies associated with the tunnelling transport process (e.g. Poole-Frenckel or Fowler–Nordheim tunnelling). Thus, it is believed that the interfacial traps dominates the shift of V_{th}.

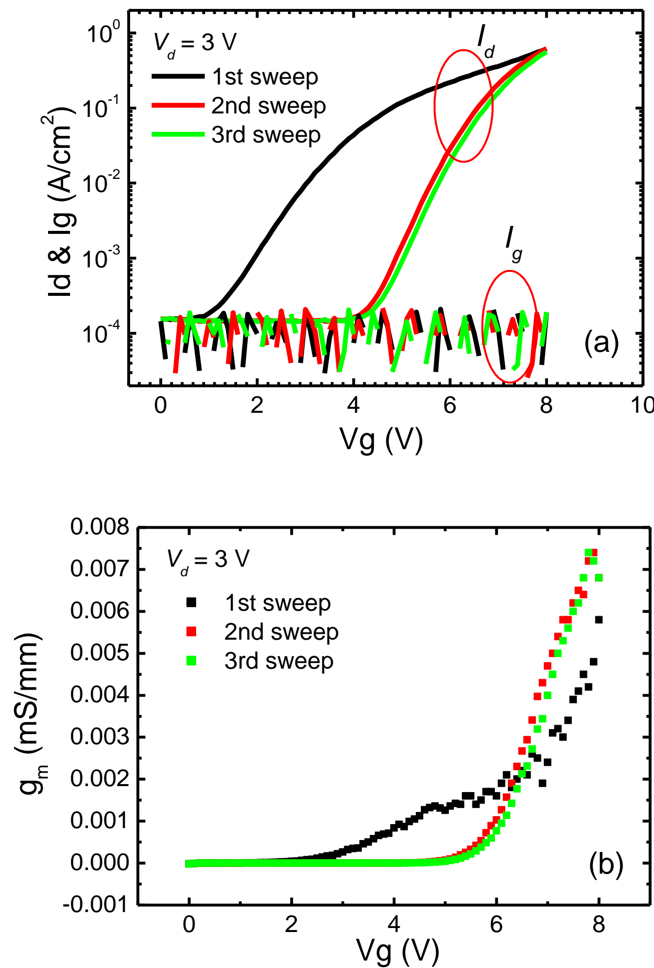


Fig. 3.17 Three consecutive sweeps of (A) transfer characteristics on a log scale showing the gate currents and (b) transconductance (g_m).

The typical transfer characteristics and the gate currents are plotted on a semi-log scale as shown in Fig. 3.17 (a). It can be observed that the device off-state gate leakage current remains below the detection limit of the SMU within the applied gate voltage range. The device transconductance (g_m) is plotted in Fig. 3.17 (b). Interestingly, it is observed that the overall g_m is increased in the second and third sweeps. The g_m of a MOSFET is described by [28],

$$g_m \cong \frac{W}{L}\mu_n C_{ins} V_d \qquad [3.3.1]$$

where W and L are the gate width and length, respectively, μ_n is the electron mobility and C_{ins} is the capacitance of the gate insulator. Since the device geometry is fixed and V_d is kept constant, it can be deduced that the g_m enhancement comes from the increase in electron mobility in the inversion channel. This kind of mobility enhancement is rarely observed in HEMTs since the trapped charges are away from the channel (i.e. at the surface of AlGaN barrier) and the 2DEG mobility tends to be unaffected [29]. Whereas in a MOSFET, the trapped charge is in the vicinity of the inversion channel, therefore it is speculated to have an influence over the channel mobility.

The typical device *I-V* characteristics are shown in Fig. 3.18. Note that the device has been previously measured during the transfer measurement, therefore the V_{th} is about 6 V. The area-specific on-resistance ($R_{on\text{-}sp}$) measured at $V_g = 8$ V is about 10 Ω-cm^2 determined with a device active area of 7.5×10^{-7} cm^{-2} defined by the trench opening size (1.5 μm × 50 μm). It is also observed that I_d has a second increase after saturation which is an indication of a possible punch-through effect which is also observed in Si MOSFETs [30,31]. The *I-V characteristics* clearly demonstrates the transistor behaviour and verifies feasibility of the design.

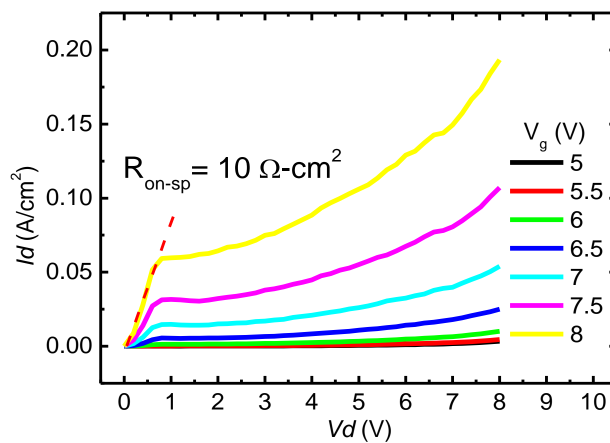


Fig. 3.18 The I-V characteristics of a GaN VMOSFET.

3.3.2 Leakage current analysis

The study of GaN-based vertical structures has lasted for more than a decade. However, there is still no commercial product available. One of the major obstacles is the high leakage current that prevents the realization of high blocking voltage. Therefore, it is important to understand the device leakage paths. As shown in Fig. 3.19, the total leakage current consists of three components in the structure: (1) gate leakage through gate dielectric, (2) electrons travelling through the bulk p-GaN CBL, and (3) leakage current along the mesa sidewall. Within these leakages, component (1) can be measured by monitoring the gate current whereas the source current is the sum of components (2) and (3).

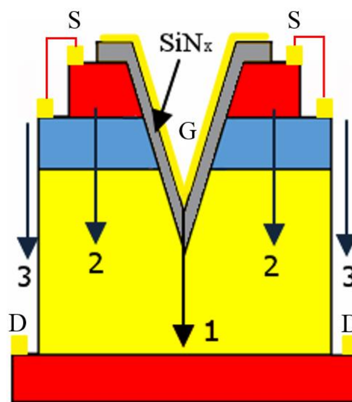


Fig. 3.19 Schematic diagram of leakage paths: (1) gate leakage, (2) bulk CBL leakage, and (3) mesa sidewall leakage.

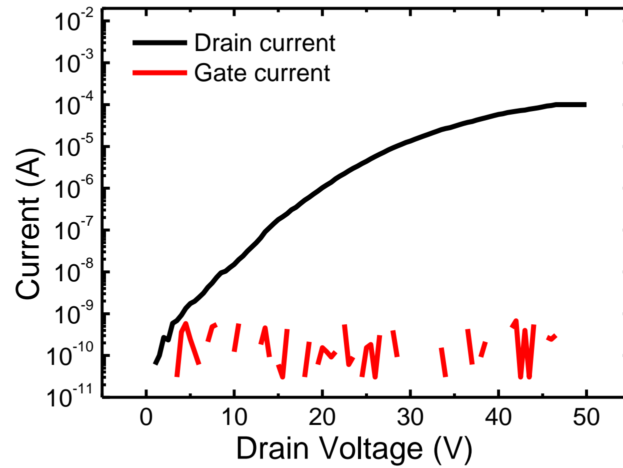


Fig. 3.20 Three-terminal breakdown characteristics of the VMOSFET.

Fig. 3.20 shows the typical off-state three-terminal breakdown characteristics. During the measurement, the gate is held at 0 V as it is an E-mode device. It can be seen that the gate current remains in noise level within the measured range which suggests all leakage is from the source.

There are two components in the drain-to-source leakage, namely the bulk CBL leakage and the mesa sidewall leakage. To differentiate the leakage path, circular diode structures with diameters (d) ranging from 60 to 200 μm are used to characterize the source leakage current. Since the diode circumference is proportional to d and diode area is proportional to d^2, the dominant leakage path can be determined based on the relationship between d and leakage current.

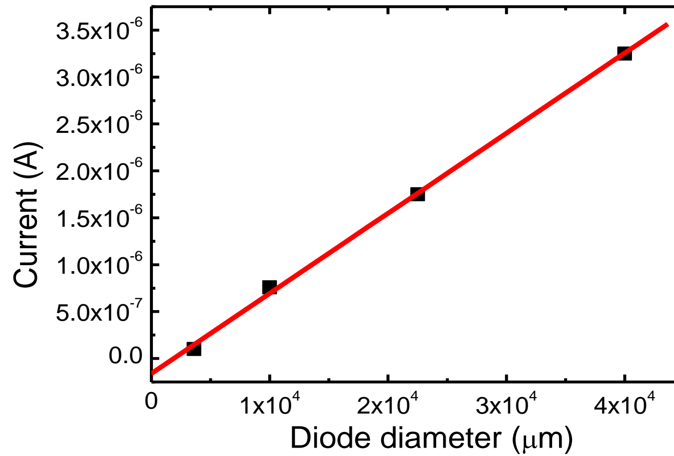


Fig. 3.21 The leakage current of circular diodes plotted as a function of device area (d^2). Data presented is the average of 4 sets of devices.

The average leakage current of 4 sets of the diode structures is plotted in Fig. 3.21. A linear dependence is found between the leakage current and device area which indicates the leakage current mainly comes from the bulk CBL. The leakage could originate from interfacial states at the P-N junction which is evidenced by the early turn-on in the forward bias which will be discussed in the following section. The interfacial states can act as tunnelling sites or recombination centres which give rise to the leakage current. Additionally, the punch-through effect should also be considered due to the low hole concentration in the CBL which could be fully depleted under reverse bias.

The gate blocking capability is further characterized by applying a gate-source voltage until a breakdown is observed in a VMOS structure. Because the gate dielectric overlaps the source n^+ region, the measured breakdown field reflects the true characteristics of the SiN_x without any voltage drop over the GaN layers. It can be seen from Fig. 3.22 that the leakage current is below 15 nA before a hard breakdown happens at about 14 V which corresponds to a breakdown field of 7 MV/cm which is within the expected value for SiN_x (3-11 MV/cm) as discussed in chapter 2.

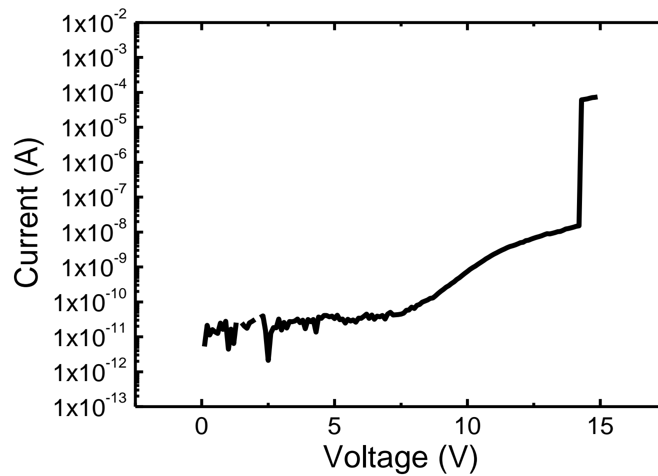


Fig. 3.22 Gate breakdown characteristics in a VMOSFET.

3.4 Summary

The fabrication process and initial characterization results of VMOSFET and VHEMT structures are described. A self-limiting KOH wet etching technique was developed to enable the fabrication of the devices. Channel regrowth is performed by both MOCVD and MBE on the KOH etched samples. It was found that the high temperature in MOCVD can cause an "etching" effect in the c-plane sidewall due to the mass transport effect. Whereas the lower temperature MBE growth produced a uniform $Al_{0.1}Ga_{0.9}N$ barrier with a smooth interface with the underlying GaN layer.

Simpler VMOS structure with proper gate modulation was successfully demonstrated as a precursor to the VHEMT structure. In the transfer characteristics, a positive shift in V_{th} is observed during multiple sweep which is caused by charge trapping at the SiN_x/GaN interface under a forward gate bias. The three-terminal breakdown analysis revealed that the leakage current is dominated by the bulk leakage through the p-GaN CBL. The results signify the importance of the p-GaN layer in preventing the leakage currents to achieve high breakdown voltages.

Based on the characterization of the VHEMT structure, further optimization is needed to demonstrate a working VHEMT. In detail, it is important to establish the correct c-plane

sidewall slope together with a correct Al fraction to obtain the 2DEG. Furthermore, it is essential to obtain a low background doping in the regrown layers with a smooth surface in the regrowth process to remove unwanted leakage paths. Lastly, low resistivity and high hole concentration in the p-GaN CBL is the key to the realization of high blocking voltage and high switching speed. Therefore, an effective Mg activation process, especially when encapsulated by the top n^+ GaN, needs to be developed.

3.5 Reference

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Chapter 4 Characterization of GaN-based P-N diodes

P-N junction is the most important building block in a VJFET. Therefore, as a precursor to the VJFET structure, regrown P-N diodes are first studied. Due to the lack of a reliable p-type implantation technique, forming VJFET structures requires epitaxial regrowth in an etched structure which poses a challenge. In fact, very few studies on GaN-based VJFETs are reported so far because of the difficulties in growing of p-GaN in a trenched structure. In detail, due to the high activation energy of magnesium (Mg) in p-GaN, the hole concentration in p-GaN is limited to 10^{18} cm^{-3}. Additionally, regrown p-GaN faces more issues such as defects and contamination at the regrown interface [1], impurity incorporation and non-planar grown [2] which could be detrimental to the device. P-GaN plays a major role in sustaining the high blocking voltage in vertical structures, as well as in affecting the device V_{th}, V_{br} and the switching speed. Therefore, it is essential to understand the characteristics of regrown p-GaN.

4.1 Choices of p-type material

Mg is the most common dopant to achieve p-type doping in GaN grown by both metal-organic chemical vapour deposition (MOCVD) and molecular beam epitaxy (MBE). However, achieving high hole concentration has been a challenging task due to (a) the low solubility of Mg atoms, (b) the formation of defects and Mg self-compensation effect at high doping level and (c) the large activation energy of Mg (~170 meV) [3-5]. In addition, the formation of Mg-H bonds which is commonly seen in MOCVD grown p-GaN can further reduce the effective hole concentration.

In contrast to MOCVD, MBE growth uses solid Mg source as p-type dopant source thus does not require activation process (to break the Mg-H bonds) and a hole concentration up to $\sim 3\times10^{18}$ cm^{-3} can be achieved [6]. In addition, MBE growth is farther away from thermodynamic equilibrium which allows the growth of thermodynamically forbidden materials. Professor Sergei V. Novikov at the University of Nottingham has developed a

diluted material $GaN_{1-x}As_x$ whose bandgap can be varied between 0.7 to 3.4 eV depending on the Arsenide (As) composition. In addition, the $GaN_{1-x}As_x$ alloy becomes amorphous when $0.17<x<0.8$ and can provide a hole concentration up to 1×10^{20} cm^{-3} [7-9]. Therefore, in this study, MBE was chosen for the growth process and both p-GaN and p-$GaN_{1-x}As_x$ are characterized and compared.

4.1.1 Comparison between p-GaN and p-$GaN_{1-x}As_x$

As an initial characterization step, both p-GaN and p-$GaN_{1-x}As_x$ samples were grown on sapphire substrates to evaluate the electrical properties. The p-GaN sample (SN834) was grown to 0.5 µm at ~760 ˚C under Ga-rich condition. The p-$GaN_{1-x}As_x$ sample (SN838) was grown to a thickness of 1 µm at much lower temperature of ~245 ˚C in order to achieve amorphous growth and to promote Mg solubility. The detailed growth conditions are described in the following sections. Hall Effect and CTLM samples were prepared to extract the carrier and contact properties. Ni/Au (20/20 nm) was thermally evaporated followed by a lift-off process to form ohmic contact. In order to achieve good ohmic contact on p-GaN, SN834 was annealed at 500 ˚C in a N_2/O_2 mixed gases environment for 5 minutes whereas SN838 was not annealed since high temperature annealing (above growth temperature) may damage the p-$GaN_{1-x}As_x$ layer.

In SN834, the hole concentration is about 1.9×10^{18} cm^{-3} and hole mobility is 0.73 $cm^2V^{-1}s^{-1}$ measured by Hall effect measurement. The sheet resistance, depicted in Fig. 4.1(a), varies from 35 to 400 kΩ/sq from the edge to the centre of the wafer. This variation is thought to be caused by the non-uniform heat distribution in the MBE system. In comparison, SN838 shows a reduction in both magnitude and variation in R_{sh} from 13 to 32 kΩ/sq as shown in Fig. 4.1(b). A hole concentration in the 2×10^{19} range is measured by Hall measurement.

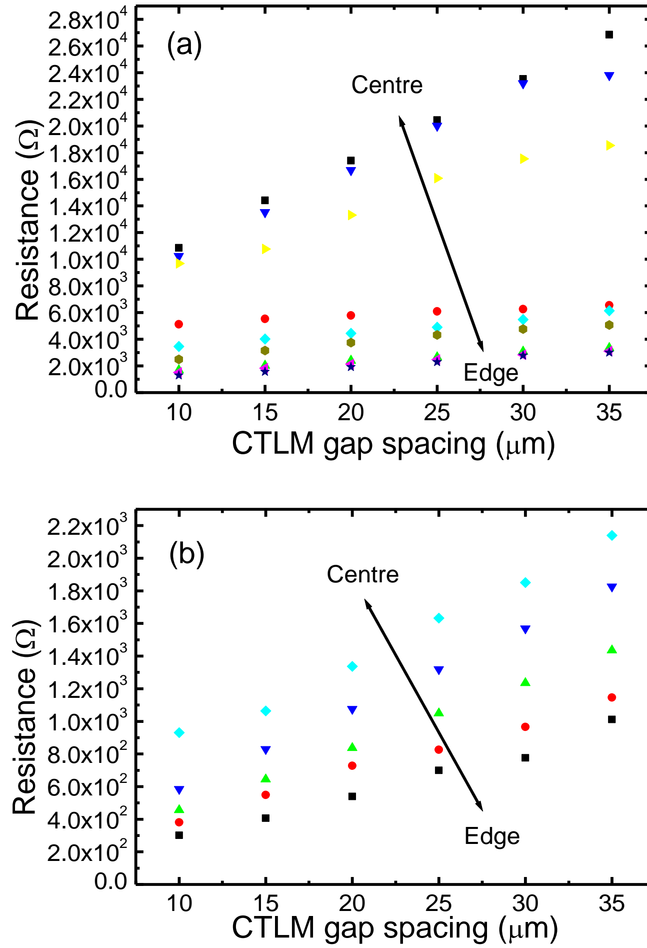

Fig. 4.1 CTLM results of (a) crystalline p-GaN (SN836) and (b) p-$GaN_{1-x}As_x$ showing a variation of resistance across the wafer.

From the Hall and CTLM results, it is clear that p-$GaN_{1-x}As_x$ can provide a much higher hole concentration and better conductivity than p-GaN. The high hole concentration and low resistance can improve the performance of electronic devices. Therefore, more p-$GaN_{1-x}As_x$ samples were prepared to explore the possibility of using this material in electronic devices.

4.2 Characterization of p-$GaN_{1-x}As_x$/n-GaN diodes

In the previous section, we have shown that a high hole concentration together with lower resistance can be achieved using p-$GaN_{1-x}As_x$. However, reports on the characteristics of the material in electronic devices are still lacking. In this section, a study of the electrical characteristics of p-$GaN_{1-x}As_x$/n-GaN junction diodes is presented, including the structural properties and transport mechanisms.

4.2.1 P-N diode fabrication details

The diode structure is shown in Fig. 4.2. Firstly, n-GaN templates with a 500 nm n+GaN contact layer with a Si concentration of ~5×10^{18} cm^{-3} and 3 μm GaN drift layer with Si concentration of ~2×10^{16} cm^{-3} were grown using MOCVD on sapphire substrates. Subsequently, the sample was transferred (in air ambient) into a plasma assisted molecular beam epitaxy (MBE) chamber for 1 μm $GaN_{1-x}As_x$ regrowth. Two samples (samples 1 and 2) were grown at different Ga beam equivalent pressures (BEPs) of 2.3×10^{-7} and 2.1×10^{-7} Torr, respectively. These Ga BEPs were chosen to enable growth with the lowest resistivity which, as will be discussed later, is also close to the conditions where a transition between amorphous and polycrystalline is possible. The As and Mg BEPs were kept at 6.6×10^{-6} and 6×10^{-9} Torr and the substrate temperature was held at 245 °C during growth for both samples. The detailed growth mechanisms can be found elsewhere [7,8]. In addition, a set of $GaN_{1-x}As_x$ calibration layers were grown to study the dependence of resistivity and contact resistance on Ga BEP which was specified between 1.3×10^{-7} and 2.2×10^{-7} Torr.

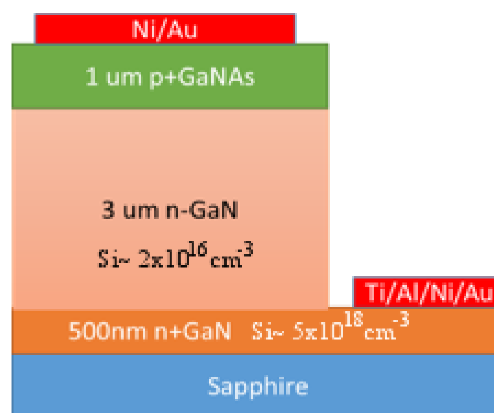

Fig. 4.2 Device structure of $GaN/GaN_{1-x}As_x$ P-N junction

The mesa diode was patterned by standard lithography with an active area of 1.2×10^{-3} cm^2 and dry-etched in an inductively coupled plasma system with Cl_2-based gases to access the n+GaN current spreading layer. Ti/Al/Ni/Au and Ni/Au contacts were deposited using a thermal evaporator as the cathode and anode, respectively. It is worth mentioning that most

Ni-based ohmic contacts formed on p-GaN in the literature required a post-deposition annealing in O_2 ambient to achieve a good ohmic contact [10,11]. However, in our samples, post-deposition annealing was not required due to the high carrier concentration in the p-type material.

4.2.2 Properties of $GaN_{1-x}As_x$ layer

Room temperature Hall-effect measurements were carried out on a calibration sample grown on sapphire which is to eliminate any possible leakage through the n-GaN layer. With a Ga BEP of 2.3×10^{-7} Torr, hole concentration of 8.5×10^{19} cm^{-3} and mobility of 0.15 $cm^2V^{-1}s^{-1}$ were extracted. CTLM structures were used to study the dependence of specific contact resistance (ρ_c) and resistivity on the Ga BEP. As shown in Fig. 4.3, a clear reduction of ρ_c and resistivity are observed with increased Ga BEP. With Ga BEP increased to 2.2×10^{-7} Torr, ρ_c and the resistivity reduced to 1.3×10^{-4} Ωcm^2 and 0.5 Ωcm, respectively, which are lower than those typically achieved in conventional p-GaN [12-15].

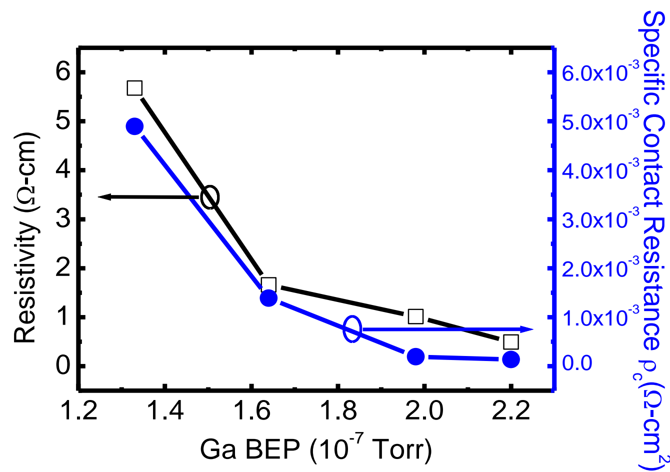

Fig. 4.3 Dependence of $GaN_{1-x}As_x$ resistivity (black) and specific contact resistance (blue) on Ga flux during growth.

However, it has been observed before that an increased Ga BEP can result in the formation of polycrystalline clusters embedded in the amorphous matrix [9]. In addition to the grain boundaries, the polycrystalline region contains a high density of defects in the crystallites

which can lead to high leakage current, and therefore is undesirable. The aim was to grow the highest possible conductivity layers while avoiding the formation of polycrystalline structures. Fig. 4.4(a) shows the transmission electron microscopy images of the P-N diode samples. An all-polycrystalline structure was observed in sample 1 (Ga BEP 2.3×10^{-7} Torr).

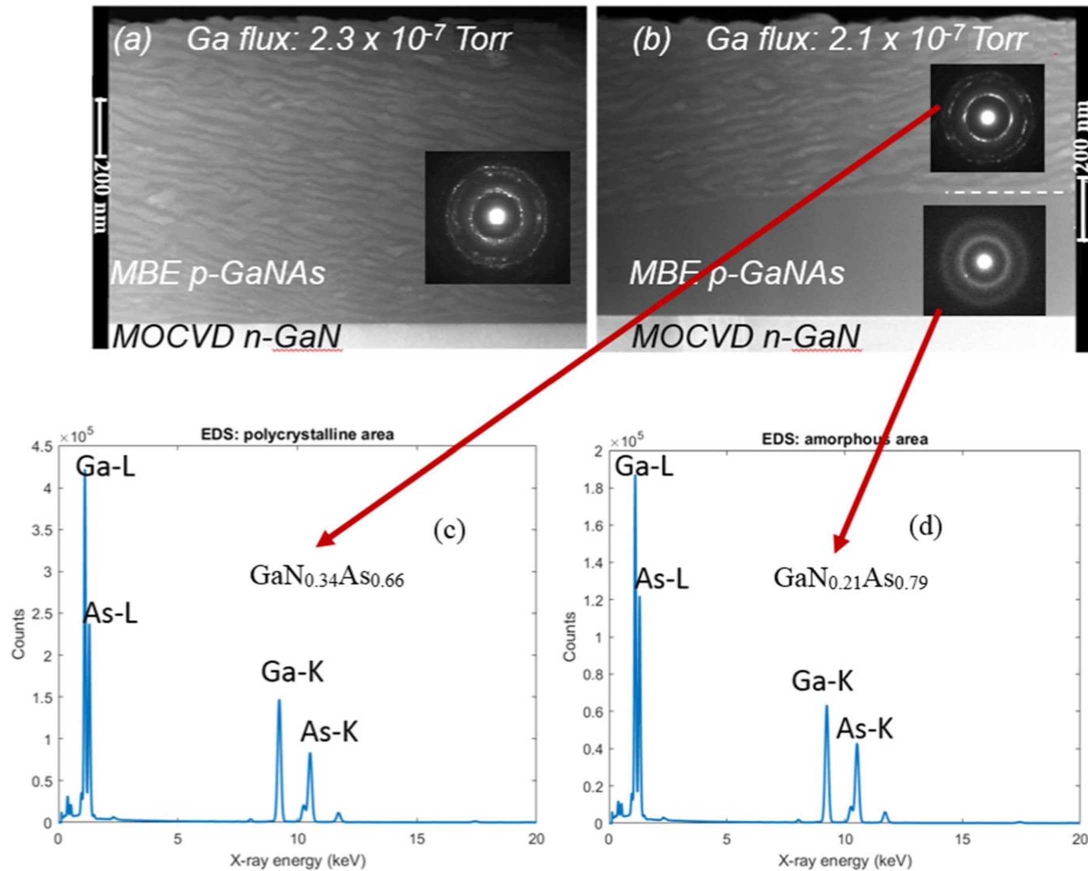

Fig. 4.4 TEM images with electron diffraction patterns of $GaN_{1-x}As_x$ layers showing (a) sample 1 (all-polycrystalline structure), and (b) sample 2 (amorphous/polycrystalline structure); EDS results showing the composition of (c) polycrystalline region, and (d) amorphous region.

In comparison, when the Ga BEP was reduced to 2.1×10^{-7} Torr in sample 2, as shown in Fig. 4.4(b), the growth started with an amorphous layer (~350 nm) followed by a polycrystalline layer which can be identified by the TEM images and electron diffraction patterns. It is thought that the transition occurred as a result of Ga accumulation during growth which increased the effective Ga BEP.

Effort was given to determine the bandgap of the material. However, we were unable to detect any photoluminescence (PL) or cathodoluminescence (CL) signal from $GaN_{1-x}As_x$ layers, similar to what was observed in previous studies [7,8]. Instead, an energy dispersive x-ray spectroscopy (EDS) analysis was carried out on sample 2 to determine the average composition of each region. As shown in Fig. 4.4(c) and (d), $GaN_{0.34}As_{0.66}$ and $GaN_{0.21}As_{0.79}$ compositions were measured in the polycrystalline and amorphous regions, respectively. According to the band anti-crossing model and previously published results, the bandgap values of both samples are estimated to be about 1 eV [7,8].

4.2.3 Current conduction mechanisms in the P-N junctions

The room temperature turn-on voltage (defined at 10 mA/cm^2) for samples 1 and 2 are 1.29 and 1.07 V, respectively. The higher turn-on voltage in sample 1 agrees with the high bandgap estimated by EDS. Fig. 4.5(a) and (b) show the temperature dependent current–voltage (*I–V–T*) characteristics for samples 1 and 2 measured over the temperature range of 305–430 K on a semi-log scale. The forward currents increase exponentially at low bias (<0.35 V) and non-exponentially at higher bias voltage due to series resistance. In order to identify the dominant current conduction mechanism at low bias regime, the reverse saturation current I_0 and ideality factor n is extracted by fitting to the Shockley model described by [16]:

$$I = I_0[\exp\left[\frac{q(V-IR_s)}{nkT}\right] - 1] \qquad 4.1$$

where R_s is the series resistance, k the Boltzmann constant and T the temperature. In the classical generation-recombination (G-R) model, n lies between 1 and 2 and is independent of temperature and I_0 is characterized by:

$$I_0 \propto \exp[-\frac{E_{ac}}{2kT}] \qquad 4.2$$

where E_{ac} is the activation energy that describes the energy of the recombination site. It is worth mentioning that n is equal to 1 when diffusion dominates the current transport process and n is equal to 2 when the transport is dominated by G-R process which takes place in the

mid-gap states. On the other hand, n is found to be inversely proportional to T in a tunnelling dominated process. Therefore, the relationship of n and T is widely used to determine the dominant transport process.

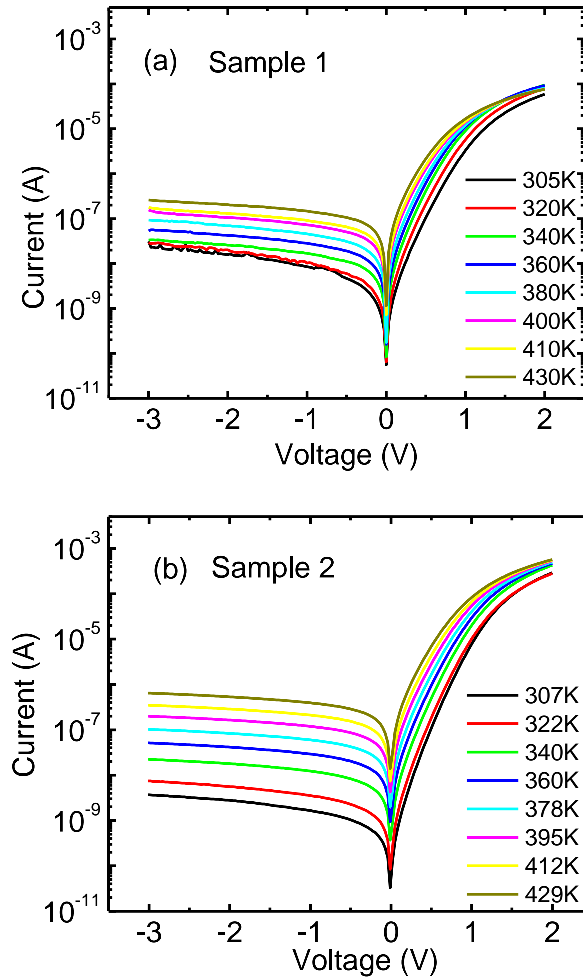

Fig. 4.5 Temperature dependent I–V characteristics on semi-log scale of (a) sample 1 (all-polycrystalline) and (b) sample 2 (amorphous/polycrystalline).

Fig. 4.6 (a) and (b) depict the curve fittings which were used to extract I_0 and n for sample 1 and sample 2, respectively. Good curve fitting was obtained at the low bias regime (<0.35 V) where series resistance and high injection effect are insignificant. The n extracted at room temperature from samples 1 and 2 are 4.3 and 3.5, respectively. Several groups have reported n greater than two in GaN P-N junctions which contradicts the G-R model. Shah et. al. [17] attributed this behaviour to the summation of n of each rectifying junction within the structure, including the contacts. In our case, there is only one junction and the contacts are ohmic as confirmed by CTLM measurements. However, at low currents the n+/n-GaN junction could contribute to additional n due to the abrupt change in doping profile. Another possibility is due to the high density of interfacial defects, dislocations and non-uniformity of the doping [1,15].

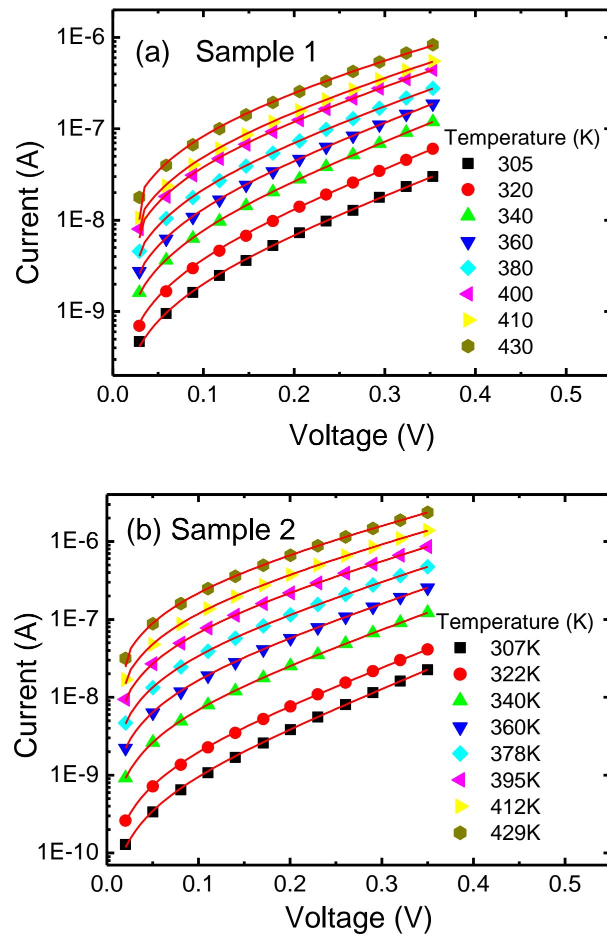

Fig. 4.6 Curve fitting of temperature dependent I-V characteristics at low bias regime (<0.35 V) of (a) sample 1and (b) sample 2. The red lines are the fitted curves.

On the other hand, a tunnelling current in the junction may also result in $n > 2$ which can be identified when n is inversely proportional to T [18-21]. The plot of n versus T is given in Fig. 4.7. In sample 1, n reduces to 3.8 when T increases to 340 K which is a signature of a tunnelling mechanism. Within this temperature range, $\ln(I_0)$ is observed to be proportional to T which can be described by a multi-step tunnelling mechanism similar to amorphous silicon P-N junctions [19] and GaN LEDs [22].

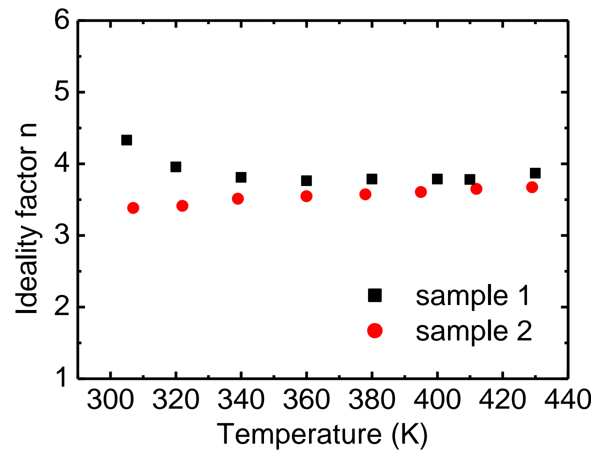

Fig. 4.7 Temperature dependent of ideality factor n.

As a polycrystalline structure, tunnelling is expected at the grain boundaries between the crystallites [23]. In addition, the high density of defects within the crystallites may also act as mid-gap states and lead to defect-assisted tunnelling. Above 340 K, n becomes independent of T indicating a possible transition to the G-R process. A similar transition process was also observed in wafer fused GaN/GaAs diodes [24].

Fig. 4.8 shows the Arrhenius plot of I_0 to determine the energies of the recombination sites. However, a nonlinear fit was observed for sample 1 whereas one would expect a straight line in the case of recombination dominated conduction. A similar nonlinearity has been observed in polysilicon P-N diodes [23] where two activation energies were obtained, indicating the presence of two energy levels within the bandgap. In our case, the activation energy gradually increases from 0.32 to 0.48 eV as the temperature increases, which may indicate multiple energy levels distributed within the bandgap. It is speculated that the recombination process occurs at the lower energy tunnelling sites at low temperature and, as temperature increases, higher energy levels are involved which moves the activation energy towards higher values. In sample 2, on the other hand, n remains almost constant throughout the temperature range. $\ln(I_0)$ is observed to have a linear dependence on $1/kT$ which is consistent with equation [4.2]. $E_{ac} = 0.56$ eV is extracted from Arrhenius plot which is in agreement with the estimated half bandgap value for $GaN_{0.21}As_{0.79}$. This is an indication that recombination in the amorphous $GaN_{0.21}As_{0.79}$ part of the depletion region dominates the conduction.

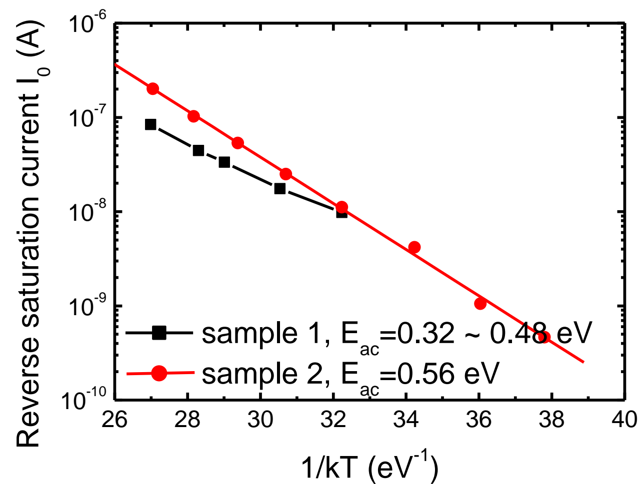

Fig. 4.8 Arrhenius plot of I_0. Sample 1 is tunnelling dominated at temperatures below 340 K therefore not shown in the Arrhenius plot.

Fig. 4.9 shows the forward current characteristics on a log–log scale. At bias greater than 0.35 V, the currents follow a power law (V^m) dependence in both samples. The value of m is greater than two which indicates that the current is space charge limited [21]. This is understandable as the electron concentration of the drift layer is more than three orders of magnitude lower than the hole concentration in the p-type region. The electrons in the drift region recombine with the holes injected and forms an additional space charge region. The reduced m at higher bias indicates a transition towards series resistance limited region.

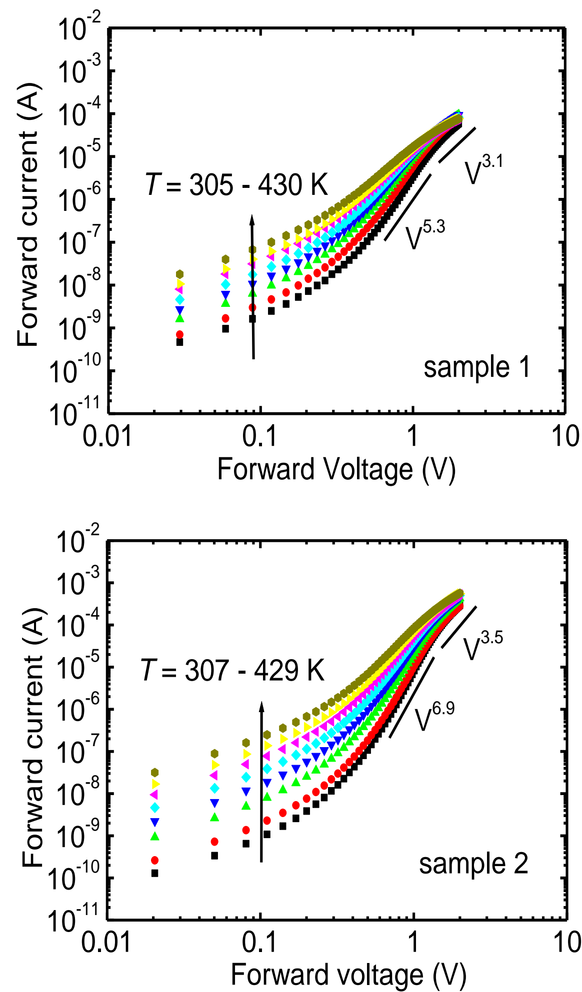

Fig. 4.9 Forward current characteristics on a log–log scale of (a) sample 1, and (b) sample 2.

Fig. 4.10 shows the temperature dependent reverse currents plotted against reverse voltage V_r on a log–log scale. Two distinctive regions can be seen in both samples. At $V_r > 0.3$ V (except T<340 K regime in sample 1), the reverse currents follow a $V^{0.5}$ dependence which is known to be the generation current within the depletion region [21]. The Arrhenius plots of the reverse currents at 0.5 V yield activation energies of 0.28–0.37 eV for sample 1 and 0.52 eV for sample 2. The increase of activation energy of sample 1 is believed to be due to a similar behaviour as in the low forward bias regime which involves multiple energy levels. At $V_r < 0.3$ V, the reverse currents do not follow the $V^{0.5}$ relationship but are found to have a similar T dependence as in the multi-step tunnelling case. Additionally, a similar trend is observed in sample 1 for all applied voltages at $T < 340$ K. This behaviour is in agreement with the transition from tunnelling to recombination under forward bias in sample 1.

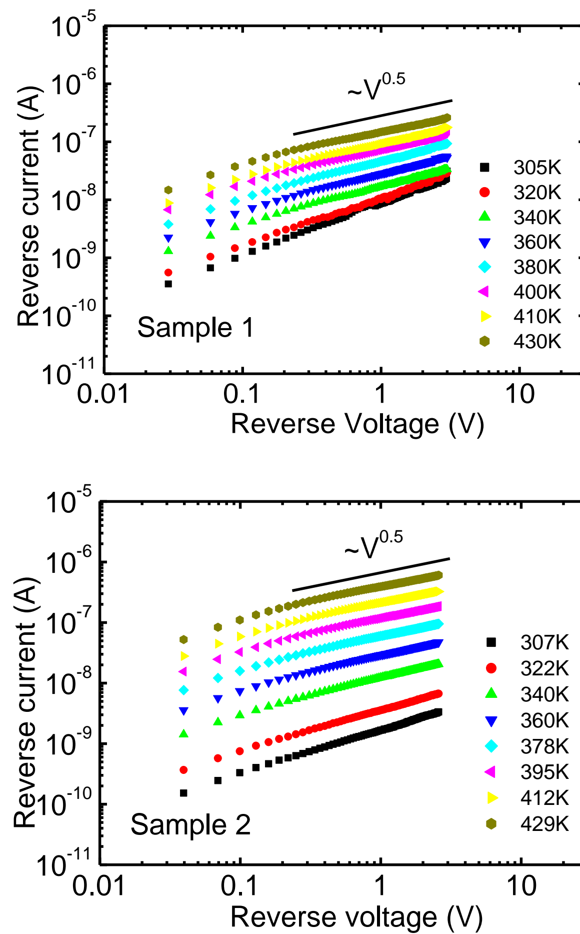

Fig. 4.10 Reverse current characteristics on a log–log scale of (a) sample 1, and (b) sample 2.

4.2.4 Discussion

Several groups observed a reduced turn-on voltage in regrown GaN diode structures which was attributed to tunnelling current through interfacial defect states [1,24–26]. In other words, the diode characteristics were dominated by the interfacial states instead of the band discontinuity and junction built-in potential. In our case, an early turn-on is very likely to happen as a tunnelling current is observed in the sample as revealed by the I–V–T experiment. However, from the *I–V* measurement, the turn-on voltages (1.29 and 1.07 V) are close to the estimated bandgap values of the respective $GaN_{1-x}As_x$ layers. So the turn-on voltage in our case cannot be as heavily dominated by interfacial states as in [24].

In addition, the 'non-physical' ideality factor ($n > 2$) presented in both samples is likely to be caused by the existence of tunnelling currents associated with the defects within the structure. In our samples, the dangling bonds at the GaN surface and the impurities incorporated during the transfer before MBE regrowth can contribute mid-gap states presents at the $GaN/GaN_{1-x}As_x$ interface leading to the non-ideal behaviours.

4.3 Summary

We have studied the structural and electrical characteristics of p-$GaN_{1-x}As_x$ layer and P-N diodes formed by p-$GaN_{1-x}As_x$ and n-GaN. A comparative study suggests that $GaN_{1-x}As_x$ can achieve much higher hole concentration and lower resistivity than conventional p-GaN. The material resistivity and crystallinity depends on Ga BEP during growth. The resistivity decreases with increased Ga BEP, however, an increased BEP can result in formation of poor quality polycrystalline structure. A transition from amorphous into polycrystalline is also observed which is thought to be due to Ga accumulation in the MBE chamber. The formation of an amorphous layer with low resistivity requires careful control of the Ga BEP during growth. The transport mechanism is also influenced by material crystallinity. At low forward bias, G-R process is the possible dominating mechanism in the amorphous structure whereas a possible transition from tunnelling to recombination is observed in the polycrystalline

structure. At high forward bias, the currents show space charge limited characteristics due the low carrier density in the n-type region. In reverse bias, tunnelling current dominates at low voltage and becomes recombination dominated at higher reverse bias. Overall, the high hole concentration is beneficial for good ohmic contacts and shows promise for low-loss GaN-based power diodes and JFETs. Practical diodes designed to withstand high reverse breakdown voltage will likely require less As concentration in order to increase the bandgap so that the carrier generation and tunnelling are limited.

4.4 Reference

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Chapter 5 GaN Vertical junction Field Effect Transistors

5.1 Introduction

Vertical junction field effect transistors (VJFETs) are very promising for power switching applications with many merits such as high breakdown voltage, low on-state resistance, low switching loss and better reliability in high temperature operation due to the mitigation of gate dielectric problems such as in MOSFETs. For example, SiC VJFET-based converter modules with a blocking voltage of 4.5 kV and converter efficiency up to 97% has been demonstrated [1]. In addition, owing to the wide bandgap of SiC, normally-off operation can be achieved without gate current injection [2]. Based on this, integrated cascode structures are proposed to further improve the switching speed at high drain voltages by reducing the effective Miller capacitance [3]. Being a wide bandgap material with excellent material properties, GaN VJFETs are expected to have an outstanding performance. Therefore, it is of interest to investigate the VJFET structure using GaN.

Compared with Si and SiC, GaN-based JFETs are not widely studied. A few groups demonstrated GaN lateral JFETs [4-6] in the early 2000s. But it was less favourable compared to HEMTs which can reach an electron mobility of nearly 2000 $cm^2V^{-1}s^{-1}$. Recently, increasing interests were expressed in developing VJFETs for its simplicity in device structure and potential high voltage handling capability. Kizilyalli and Aktas [7] demonstrated a lateral channel VJFET (LC-VJFET) which is similar to the CAVET structure with the 2DEG replaced by an n-GaN channel. A simulation work based on the LC-VJFET suggests a promising device performance [8]. However, in the lateral channel configuration, the device active area will inevitably be increased to allow for effective gate control, leading to a reduced current density. Hence, in this study, conventional vertical channel JFETs (VC-JFETs) are explored to reveal their high current and high voltage potential. Design considerations, trench regrowth processes and device characterization results of the VJFETs are presented.

5.2 Design of VJFET

In this section, the design of VJFET is discussed with the aid of TCAD simulations. For VJFETs, the channel is the most critical region which determines the V_{th}, R_{on} and even the breakdown voltage of the device. Although the practical device properties are expected to deviate from the ideal case, the simulation can serve as a guideline for practical device design. In addition, the switching speed of the device could be hindered by a low quality p-GaN layer. A transient simulation is also performed to investigate the effects of p-GaN resistance over the switching speed.

5.2.1 Threshold voltage design

The schematic device structure of a typical VJFET is shown in Fig. 5.1. Current flows from the drain to the source through the n-GaN channel which is surrounded by the p-GaN gate. The p-GaN is usually heavily doped to form a one-sided PN junction. A depletion region is formed in the channel region to block current flow.

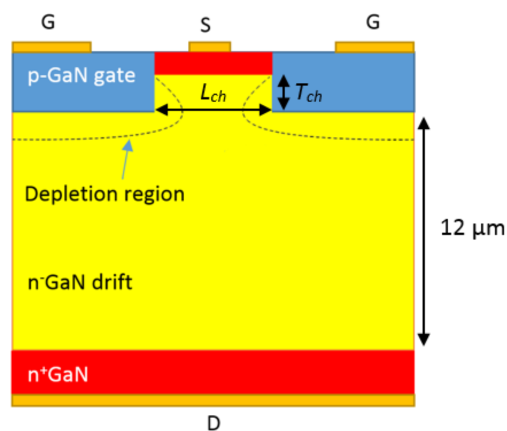

Fig. 5.1 Schematic diagram of a typical VJFET structure.

For a depletion-mode (D-mode) device, a negative gate bias is applied to widen the depletion region and the channel is pinched off when the depletion regions overlap. If the depletion regions overlap when no gate bias is applied, the device is in the enhancement-mode (E-mode) and a forward gate bias is needed to turn on the device. The maximum gate voltage can be

applied without gate current injection is equivalent to the built-in voltage (V_{bi}) of the gate-source PN diode. In the off-state, the p-GaN also serves as a current blocking layer by forming a reverse biased junction between p-GaN and drift n⁻GaN layer. The drift layer is 12 μm thick and lightly n-type doped to 1×10^{16} cm^{-3} designed to sustain a 1200 V off-state voltage. The top and bottom n$^+$GaN layers are to facilitate the formation of ohmic contacts.

For power electronics, a normally-off operation is preferred which can be achieved when the depletion region overlaps at zero gate bias. Assuming the P-GaN is heavily doped to form a one-sided junction, the V_{th} of a VJFET is given by [3],

$$V_{th} = V_{bi} - \frac{eN_{ch}\left(\frac{L_{ch}}{2}\right)^2}{2\varepsilon_0\varepsilon_r} \quad [5.2.1]$$

where V_{bi} is approximately equal to the bandgap (3 V), N_{ch} is the channel doping and L_{ch} is the channel width. It can be seen that smaller N_{ch} and L_{ch} are preferred for higher V_{th}. However, As discussed in Chapter 3, the background n-type doping is typically about 1×10^{16} cm^{-3} and, therefore, L_{ch} is the most critical parameter in controlling the V_{th} of a VJFET.

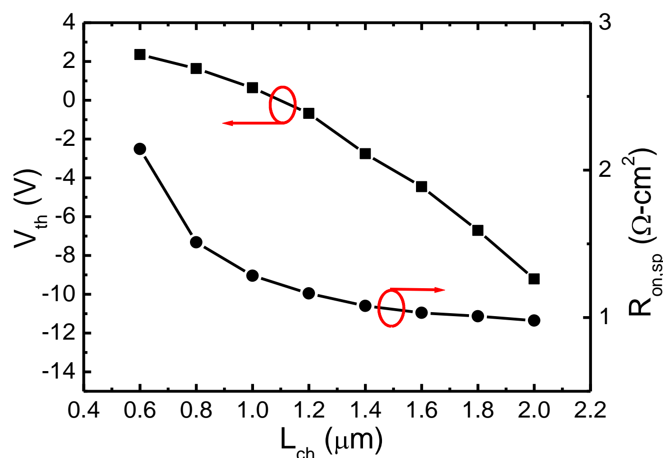

Fig. 5.2 Simulated V_{th} and R_{on} as a function of channel length L_{ch}.

Fig. 5.2 shows the simulated V_{th} plotted as a function of L_{ch}. It can be seen that the E-mode operation can be achieved by using a sub-micro channel length. To give a better margin for gate signal noise from harsh EMI conditions, more positive V_{th} can be achieved by further

reducing L_{ch}. However, the small opening size can lead to an increased channel resistance. The area-specific on-state resistance ($R_{on,sp}$) extracted at V_g = 3 V is also plotted for the corresponding L_{ch}. The device active area is defined by L_{ch} plus a margin of 1 μm on each side of the channel to account for the alignment margin between the source and gate contacts. It is observed that R_{on-sp} rapidly increases when L_{ch} is reduced below 1 μm which is due to the narrower channel and the restricted gate voltage swing since the gate turn-on voltage is limited below 3 V. Additionally, the narrow channel length also poses a threat to the device fabrication process, such as the alignment and regrowth processes.

5.2.2 Drain induced barrier lowering (DIBL) effect

The DIBL, also referred as short channel effect, is a very common problem in FETs. It is the effect that the barrier is effectively lowered by the applied drain voltage (V_d). The so-called punch-through effect happens when the barrier is not sufficient to block the current when V_d exceeds the punch-through voltage V_{pt} and the device is turned on without forward biasing the gate which leads to faulty operation. To better understand the effect, the DIBL effect is simulated using an E-mode device (L_{ch} = 0.6 μm) with a channel thickness of 1 μm. The drain voltage is swept until a punch-through is reached while the gate voltage is held at 0 V. The DIBL effect is illustrated in Fig. 5.3 (a) with the aid of a simulated conduction band diagram of the channel region of the device. It can be seen that the barrier is reduced when the drain voltage increases.

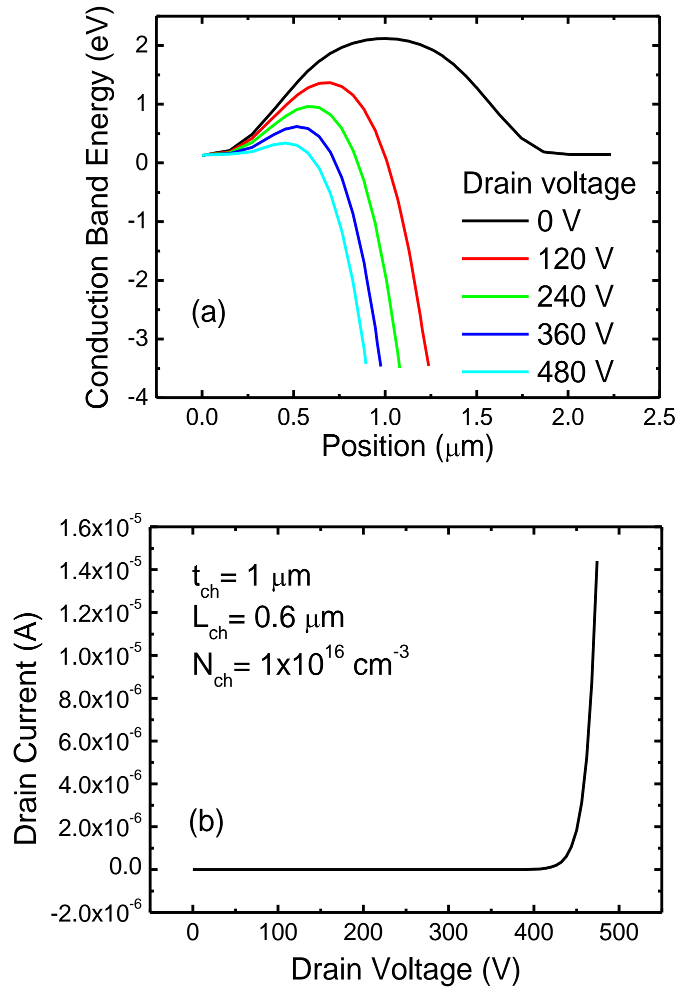

Fig. 5.3 (a) Simulated conduction band energy at various drain voltages. (b) Simulated punch-through voltage of an E-mode VJFET with gate voltage held at 0 V.

Fig. 5.3 (b) shows the corresponding punch through current. In this case, the DIBL induced breakdown happens at 430 V which is much less than the designed 1200 V avalanche breakdown capability. This suggests the V_{pt} needs to be further improved.

There are several ways to increase the V_{pt}, such as applying a negative gate bias to enhance the barrier. However, this is not applicable for E-mode devices as the gate voltage is preferred to be held at 0 V in the off-state. Alternatively, the channel thickness (T_{ch}) can be increased, similar to reducing the short channel effect in MOSFETs.

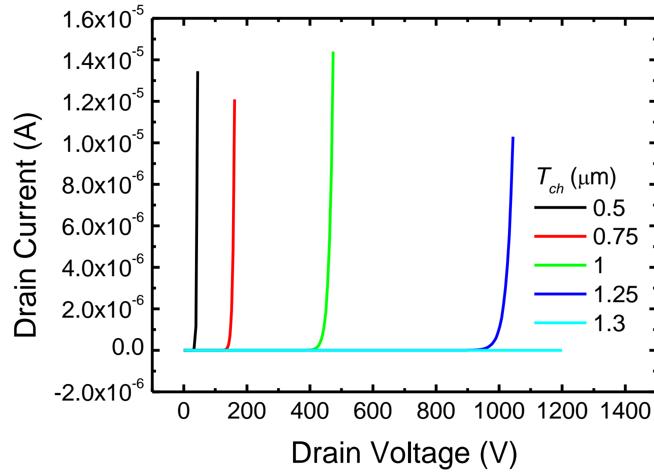

Fig. 5.4 Simulated V_{pt} as a function of channel thickness T_{ch}.

Fig. 5.4 shows the simulated V_{pt} of the 0.6 μm device with different T_{ch} where a systematic increase in V_{pt} with increasing T_{ch} is observed. The punch-through is increased to more than 1200 V with a 1.3 μm channel thickness.

5.2.3 Optimization of channel resistance

Although the relationship between $R_{on\text{-}sp}$ and V_{th} has been previously studied in section 5.2.1 as well as in [8], the design is not optimized since the channel design is over simplified where only a fixed T_{ch} is used. By observing the channel configuration, it is intuitive that both L_{ch} and T_{ch} have an influence over the channel resistance. For instance, for a given V_{pt}, narrower channel requires less T_{ch} to hold the voltage therefore reducing the channel resistance. In other words, for an optimized channel design, T_{ch} should be kept minimal to reduce $R_{on\text{-}sp}$ while maintaining the V_{pt} to the required level.

Fig. 5.5 shows the *I-V* curves at a gate voltage of 3 V with L_{ch} ranging between 0.6 to 0.8 μm. The corresponding T_{ch} is the minimum thickness required to achieve 1200 V V_{pt}. It can be observed that, despite the difference in saturation current, the $R_{on\text{-}sp}$ values of the three curves are similar. This finding is contrary to the published work [8] and it suggests that by carefully designing the channel region, a more positive V_{th} can be achieved without too much penalty of $R_{on\text{-}sp}$.

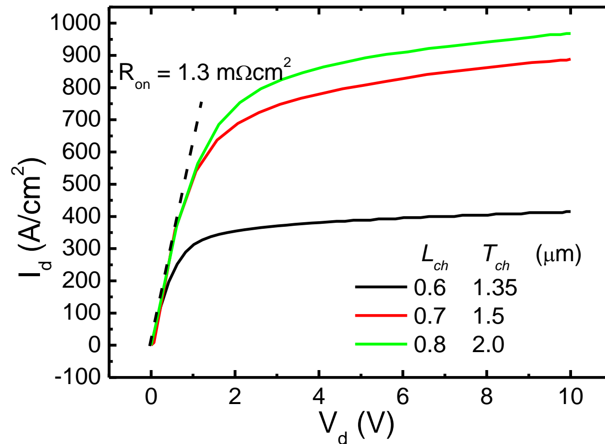

Fig. 5.5 Simulated I-V curves at V_g=3 V of VJFETs with different L_{ch}. The corresponding T_{ch} are the minimum values required to achieve 1200 V V_{pt}.

5.2.4 The effects of p-GaN conductance on switching performance

Due to the relatively large activation energy of Mg (~170 meV), it is difficult to achieve a high conductivity in a p-GaN layer, especially in a buried p-GaN structure as there is no free surface to facilitate the H out diffusion [9]. In a VJFET, as well as any vertical structures that uses p-GaN as a CBL, the p-GaN conductivity is important in determining the switching speed. Taking VJFET as an example, when a VJFET is switching between on/off states, carrier transport is required to charge/discharge the depletion regions, both in the channel and in the drift region. To verify the effect of p-GaN resistance over the switching performance, the device turn-on transient is modelled using TCAD simulation in mixed-mode with the circuit configuration as shown in Fig. 5.6. The mixed-mode simulation is similar to a SPICE modelling, but it takes the device parameters directly from the device simulator which allows us to monitor the influence of each individual physical parameter, such as gate length, carrier mobility, bandgap, etc., which is impossible in the SPICE modelling.

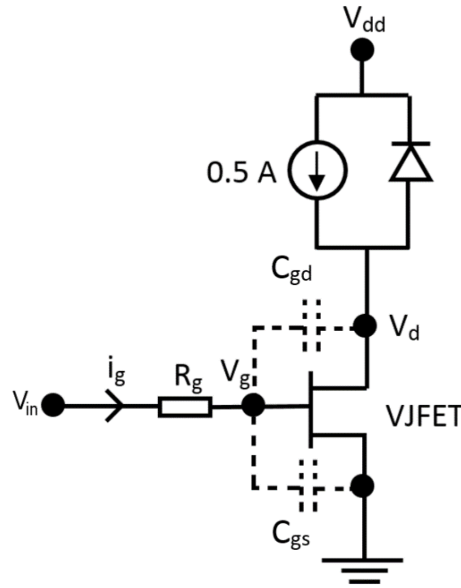

Fig. 5.6 Circuit diagram used in TCAD simulation for switching speed measurement.

An E-mode VJFET with a V_{th} of ~2.3 V is used in the simulation. The gate input voltage (V_{in}) is switched from 0 to 3 V to turn-on the device and the device turn-on speed is measured under 600 V. A current source is used to supply a constant 0.5 A load current and an external gate resistor (R_g) of 1 Ω is used to slow down the switching speed slightly for a better comparison [10]. The gate-drain capacitor (C_{gd}) and gate-source capacitor (C_{gs}) represent the depletion regions in the drift region and channel region, respectively, which are charged/discharged by the gate current (i_g). In a power transistor, the switching speed is mostly limited by the gate charge stored in C_{gd} which is calculated by,

$$Q_{gd} = C_{gd} \times V_d \qquad [5.2.2]$$

Due to the large applied V_d (typically 600-1200 V), the effective Q_{gd} is greatly enhanced which is referred to as the Miller effect. Also for this reason, other vertical structures that use p-GaN CBL will be subjected to the same effect. The time required to charge C_{gd} is determined by,

$$t = \frac{dQ_{gd}}{di_g} \qquad [5.2.3]$$

where i_g represents the average gate current during the charging period. The switching speed could be slowed down if i_g is small as a result of high resistance of the p-GaN. The resistivity of p-GaN is described by,

$$R = \frac{1}{pe\mu_h} \qquad [5.2.4]$$

where p and μ_h are the hole concentration and mobility in the p-GaN, e is the elementary charge. To test the concept, different p-GaN resistance is applied to the device by varying μ_h in the p-GaN layer. In the meanwhile, p is kept unchanged (2×10^{17} cm^{-3}) to avoid any change in other variables in the device (such as V_{th} and depletion width).

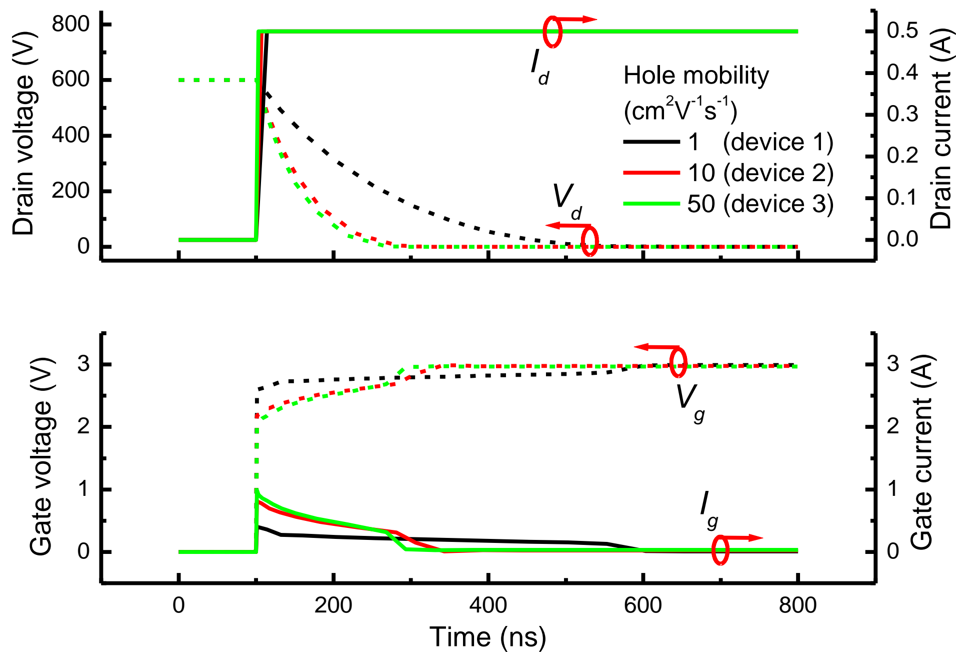

Fig. 5.7 The switch-on waveforms of VJFETs at a drain voltage of 600 V with varying hole mobility in the p-GaN layer.

The switching speeds of three devices with hole mobilities of 1, 10 and 50 $cm^2V^{-1}s^{-1}$ are simulated with V_g switched from 0 to 3 V at a V_d of 600 V. The switching waveforms are shown in Fig. 5.7. It can be seen that V_g first rises to a plateau voltage within a nano-second. During this period, the channel region is charged up to provide the required load current (i.e. 0.5 A) and the drain current rise time (t_{r_I}) can be extracted. Subsequently, V_g enters the Miller plateau during which the depletion region in the drift layer is charged. At the same time, V_d

reduces since the device is turned on and the drain voltage fall time (t_{f_V}) can be extracted. After the depletion region is fully charged up, V_g rises again to the same level as V_{in} to complete the turn-on process. The equivalent gate charge Q_{gd} is found to be 89 nC by integrating i_g over the plateau period. Using Eq. 5.2.2, the corresponding effective C_{gd} is calculated to be 148 pF.

Table 5.1 Simulated switching characteristics of three devices at 600 V with different hole mobility in the p-GaN layer.

	t_{r_I} (ns)	t_{f_V} (ns)	E_{loss} (µJ)
Device 1	14	275	38.2
Device 2	7	116	15.6
Device 3	3	102	14.2

The simulated switching speed and the energy loss (E_{loss}) of the three devices are summarized in table 5.1. It is clear that the switching speeds of device 2 and device 3 are much faster than device 1 as a result of higher i_g (Fig. 5.7) during the charging period. On the other hand, there is only a marginal difference between device 2 and device 3. In this case, the total gate resistance is dominated by R_g (1 Ω) in the gate loop. The results illustrate the importance of obtaining a good conductivity in the p-GaN layer. In an optimized device, the p-GaN resistance should be kept below the value of the external gate resistor in the gate loop to increase the switching speed and minimise the switching loss.

In summary, several design aspects of a VJFET is discussed and modelled using TCAD simulation. The combination of channel thickness and channel length determines the V_{th}, R_{on} and V_{pt} of the device. By optimizing the channel aspect ratio, the V_{th} of an E-mode device can be increased while maintaining the low R_{on} advantage. In the turn-on transient simulation, it is also shown that the p-GaN resistance can influence the switching speed and energy loss. To optimize the device performance, the p-GaN resistance should be kept at least smaller than

the series resistance in the gate loop. Using the simulation results as a guideline, practical devices are fabricated and two possible fabrication routes are explored – (1) p-GaN gate regrowth and (2) n-GaN channel regrowth which will be discussed in the following sections.

5.3 VJFET by p-type regrowth

In SiC VJFETs, the p-GaN region is typically formed by ion implantation. However, the p-type ion implantation will create too much damage to the GaN crystal hence the technique is not readily available for GaN. Consequently, the fabrication process involves a trench etching step to define the channel followed by an epitaxial regrowth process.

5.3.1 Device fabrication

The first version of VJFET is following the p-type regrowth route using two materials, namely the p-GaN and the p-$GaN_{1-x}As_x$. The substrate template and fabrication procedures are identical for both materials.

Fig. 5.8 (a)-(d) depicts the fabrication process. The template consist of a 500 nm heavily doped n^+ GaN current spreading layer, a 3 μm thick lightly doped n-GaN drift region and a 0.3 μm thick n^+GaN cap layer is grown on c-plane sapphire substrate by MOCVD (a). A 200 nm SiO_2 is deposited by MOCVD which acts as the etching mask to etch ~1 μm trench by ICP (b). Subsequently, using the SiO_2 as a regrowth mask, either 0.5 μm p-GaN or 1 μm p-$GaN_{1-x}As_x$ is regrown by MBE (c). The growth conditions are similar as described in chapter 5. Hall effect measurements on separate calibration samples on sapphire substrates show effective hole concentrations about 1×10^{18} and 5×10^{19} cm^{-3} for p-GaN and p-$GaN_{1-x}As_x$, respectively. Finally, ICP etching is performed to access the n^+GaN layers followed by the formation metal contacts (d).

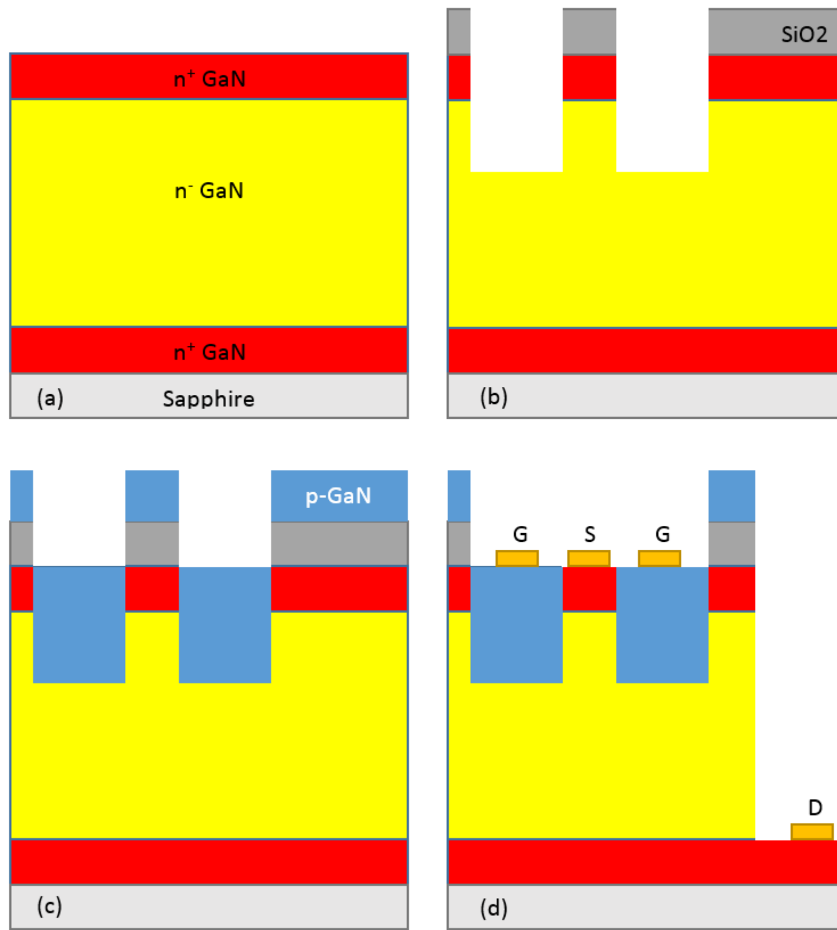

Fig. 5.8 Fabrication steps for p-type regrowth VJFET.

5.3.2 Comparison between p-GaN and p-$GaN_{1-x}As_x$ regrown structures

Fig. 5.9 (a) shows the cross-sectional TEM image of the p-GaN regrowth sample. It can be seen that p-GaN is grown on both surfaces of the GaN and SiO_2 which reflects the low selectivity nature of the growth. Similar non-selective growth has been observed in the literature for growth temperatures less than 800 ˚C [11-14]. In this structure, the growth inside the trench is the most critical which will act as the gate of the device. However, the first ~200 nm from the regrown interface of the regrown p-GaN in the trench region is very defective which could be due to the defects or contamination at the regrown interface after dry etching. On the sidewall of the trench, there is a continuous growth which bulges over the SiO_2 mask. Voids are observed at the interface between the sidewall and the bottom of the trench as the result of the simultaneous growth. Similar growth results are obtained in the p-$GaN_{1-x}As_x$

regrown sample as shown in the cross-sectional SEM images in Fig 5.9 (b) and (c). As the growth temperature is only ~245 ˚C, the growth becomes non-selective hence is comparably more uniform.

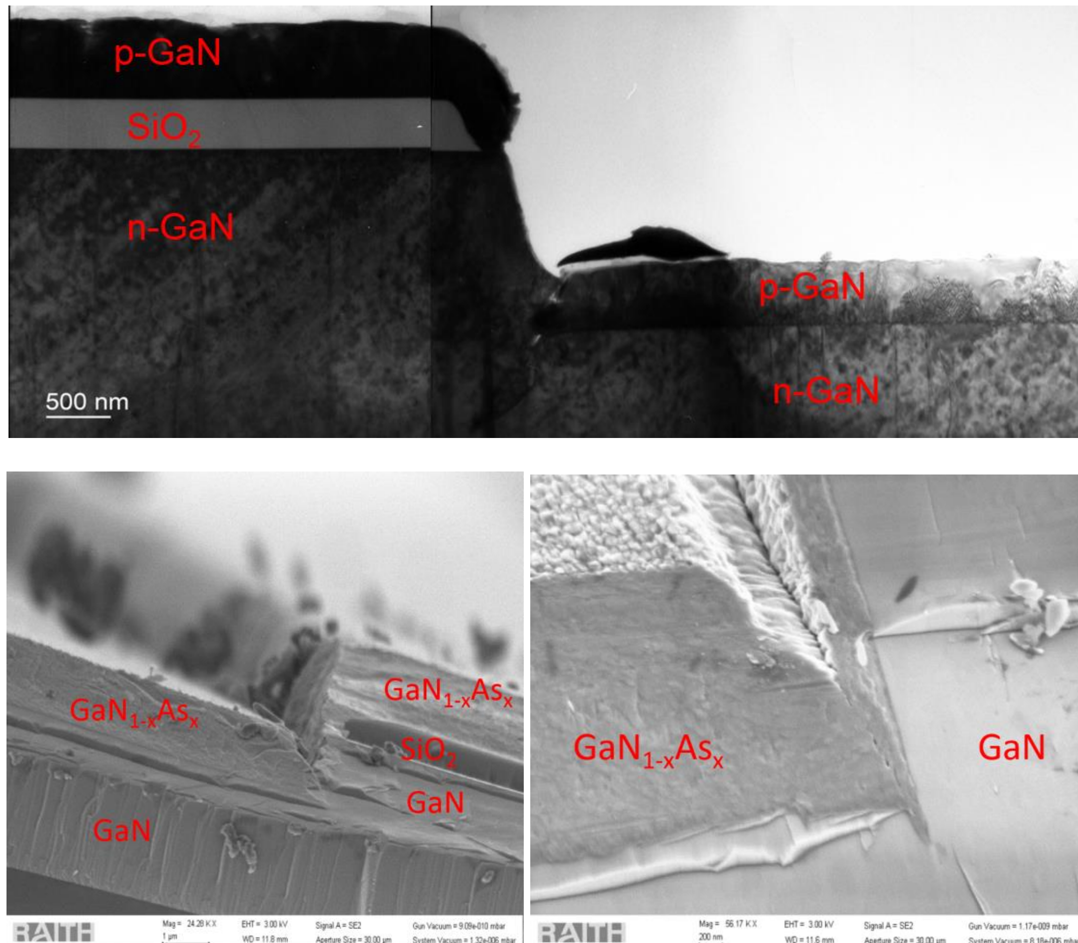

Fig. 5.9 The cross-sectional view of (a) TEM image of p-GaN regrown structure, (b) and (c) SEM images of $GaN_{1-x}As_x$ regrown sample.

Since the operation of VJFET is based on the PN junction at the channel region, the gate-source PN junction is first examined as illustrated in Fig. 5.10 (a). High leakage currents are observed in both forward and reverse biases since the theoretical turn-on voltage of GaN PN diodes should be around 3 V determined by its bandgap. The leakage currents could be related to the defective layer close to the regrowth interface. In addition, the continuous growth on the sidewall also creates a heavily doped PN junction at the top n^+ region which could enhance the tunnelling current.

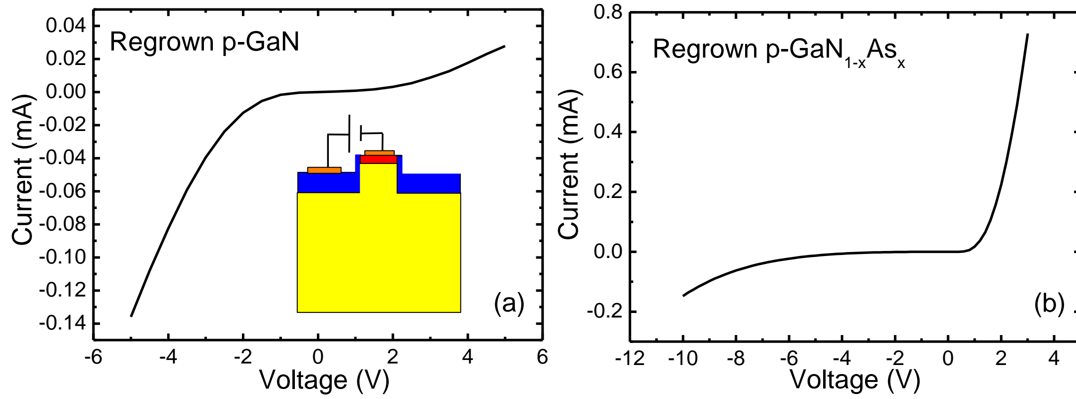

Fig. 5.10 The I-V characteristics of the PN junction with (a) p-GaN regrown structure and (b) $GaN_{1-x}As_x$ regrown structure. The inset shows the connection of the PN junction.

In comparison, the p-$GaN_{1-x}As_x$ sample shows a rectifying behaviour, as shown in Fig. 5.10 (b), with a turn-on voltage about 1 V which is similar to the results from the planar diodes in Chapter 5. However, the reverse leakage current is also pronounced which could be due to tunnelling at the grain boundaries in the amorphous material and possible defects at the regrowth interface. These leakage currents have prevented a meaningful measurement of the transfer characteristics as no gate modulation can be observed.

In summary, VJFET structures are attempted by regrowth of p-GaN or p-$GaN_{1-x}As_x$ in a trench region by MBE. Both regrown materials have shown non-selective behaviour and a continuous growth over the sidewall. The regrown p-GaN is very defective close to the interface and is unable to form a PN junction. The regrown p-$GaN_{1-x}As_x$ shows more promising results and better diode behaviour, but still suffers from high reverse leakage. These results reflect the difficulty in growing p-GaN in a trench region. To avoid these issues, an n-GaN regrowth process is developed which could offer more benefits which is described in the next section.

5.4 VJFET by n-GaN regrowth

Owing to the difficulties in obtaining good quality p-type material into the trench, an alternative method of n-GaN regrowth is adopted. There are several advantages by using this

method. For example, the p-GaN is a part of the MOCVD pre-grown template which contains less number of defects and better interface quality compared to a regrown structure. In addition, the process offers better flexibility for the fabrication process which will be explained in the following section.

5.4.1 Device fabrication

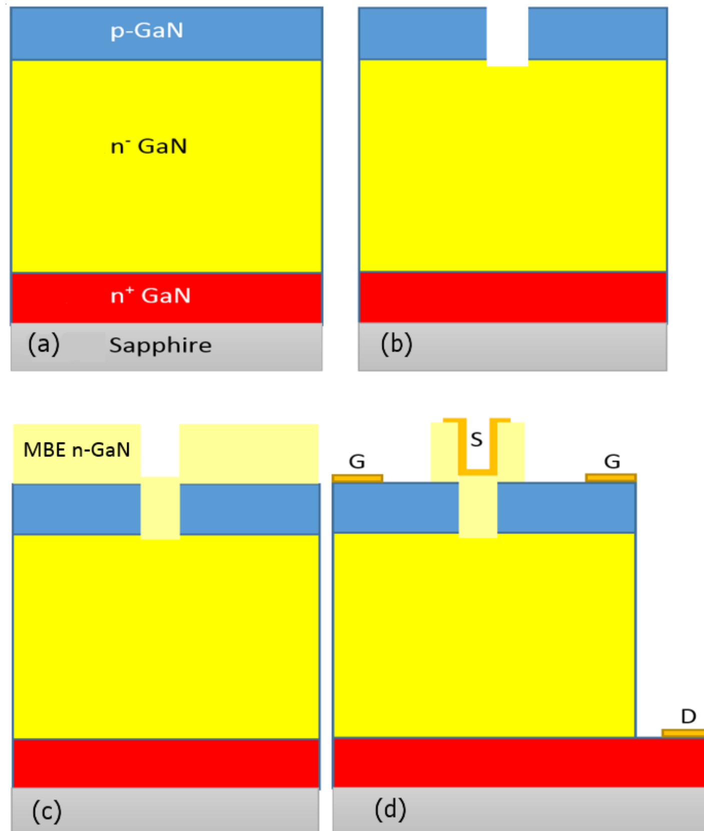

Fig. 5.11 Fabrication steps of n-GaN regrowth VJFET.

The template consists of a P-I-N structure is grown on m-plane sapphire substrate by MOCVD and the fabrication process is shown in Fig. 5.11 (a)-(d). The template consists of a 1 μm heavily doped (Si: ~10^{18} cm^{-3}) n^+ GaN spreading layer followed by 2 μm lightly doped (mid-10^{16} cm^{-3}) n^- GaN drift layer and 1 μm p-GaN CBL (a). The sample is annealed by an RTA at 800 ˚C for 10 min to activate the holes in the p-GaN by breaking the Mg-H bond. Using photo-resist as an etching mask, a ~1 μm deep trench is etched by ICP to access the n^- GaN drift layer and the photoresist is removed (b). The sample is then transferred into an MBE chamber

aiming to grow a lightly doped channel region (c). Lastly, ICP etching is performed to access the p-GaN and bottom n+ GaN layers and metal contacts are formed to the respective layers to form a quasi-vertical structure (d).

5.4.2 Structural analysis

The regrown sample is first characterized by SEM. Fig. 5.12 (a) shows a birds-eye view of a SEM image at a trench region after regrowth. A clear difference is observed between the trench surface and top surface. In detail, the top surface is relatively smoother despite the existence of pits. The reason of the formation of the pits is unclear but could be attributed to defects or contamination at the regrowth interface. On the other hand, the trench surface is rougher which could be due to several reasons, including defects generated by the dry-etching process, oxidation or contamination during the transfer, and possible change in temperature and source gas ratio within the trench region which leads to an incomplete coalescence. There also appears to be a growth on the sidewall which is of a similar roughness as the trench region.

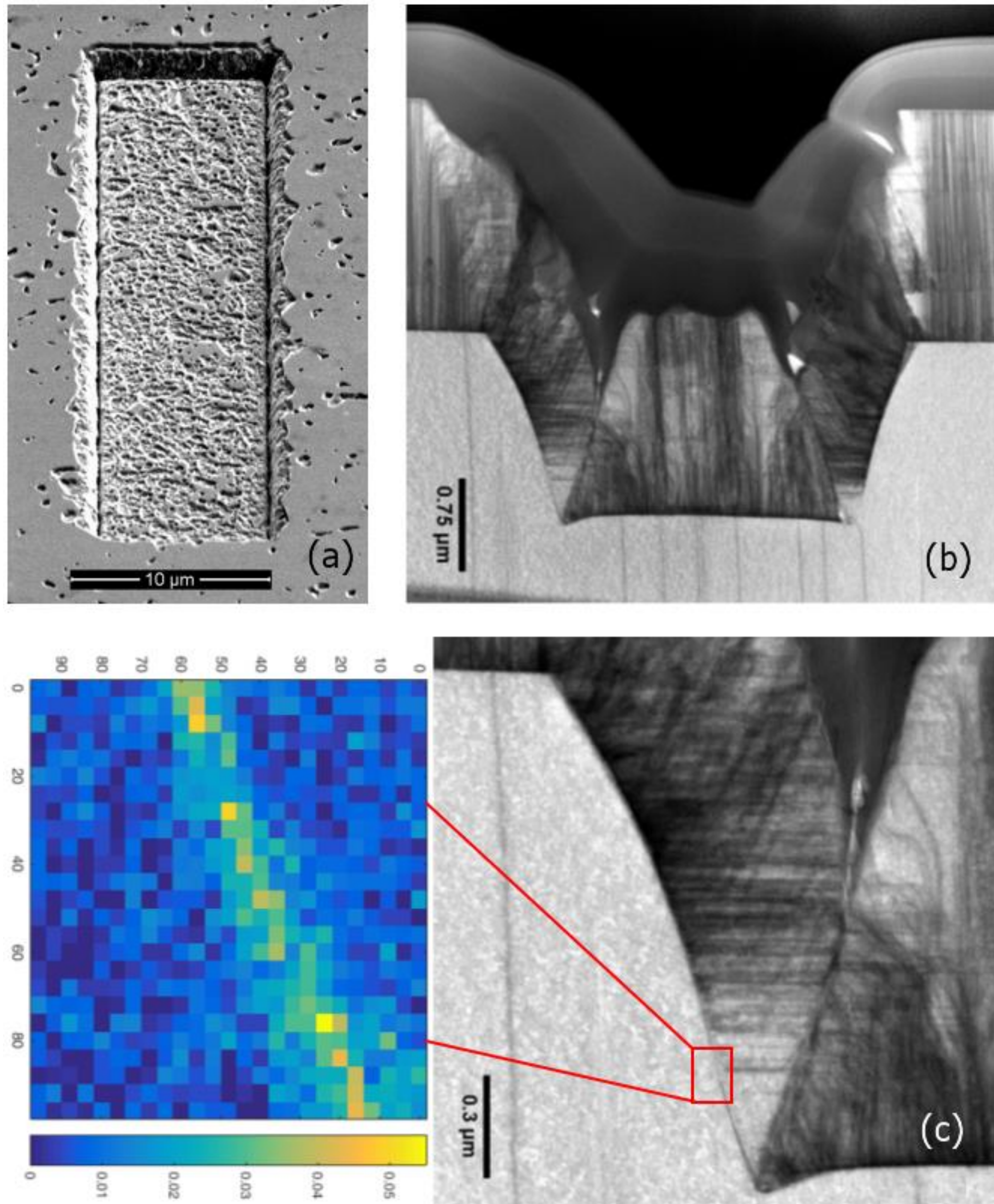

Fig. 5.12 (a) SEM image of the n-GaN regrown sample. (b) Cross-sectional TEM image of a trench region. (c) Enlarged image at the trench corner with an EDS mapping showing an oxygen signal at the regrowth interface.

To better understand the regrown material, the sample is studied using TEM which is shown in Fig. 5.12 (b). It can be seen that the growth initiates from the horizontal surface and the sidewall at the same time, forming a clear interface at the boundaries between the meeting growth fronts. The dislocations (dark lines) on the sidewall propagates along multiple directions which is an indication of formation of polycrystalline structure. The regrowth

thicknesses at the top surface and trench bottom surface are 1.86 and 1.60 μm, respectively. The slower growth rate indicates that less source gases are supplied into the trench.

Fig. 5.12 (c) shows an enlarged image at the trench corner with an EDS mapping. The regrown layer is particularly defective close to the regrowth interface which is an indication of defective and possibly contaminated interface. The EDS revealed a high oxygen content of about 5 at.% at the regrowth interface. This large amount of oxygen could come from the oxidation of the surface during the transfer process, especially after the dry-etching process, the etched surface maybe more defective and picks up oxygen more easily. It emphasizes the importance of the growth surface quality and surface treatment before regrowth may be necessary to remove the defects/contamination.

5.4.3 Electrical characterization

The regrown n-GaN layer is characterized by Hall measurement and TLM measurement. It has a sheet resistance of 24 kΩ/sq, an electron concentration of 5×10^{17} cm^{-3} and an electron mobility of 5.5 $cm^2V^{-1}s^{-1}$. Unexpectedly, the electron concentration is much higher than the expected value (1×10^{16} cm^{-3}) and is likely caused by un-intentional doping, such as Oxygen, which could migrate from the regrowth interface (Fig. 5.12), or due to an enhanced incorporated during the non-planar growth [9].

The device transfer characteristics are shown in Fig. 5.13. The drain voltage is kept at 1 V to avoid leakage current through the gate. I_d is observed to increase, only slightly, with V_g at forward gate bias. However, the channel could not be pinched off for several reasons. Firstly, the high gate leakage at reverse bias which could be due to the defects at the P-N junction. In addition, the channel has a net electron concentration at mid-10^{17} cm^{-3} regime which too high to be pinched off.

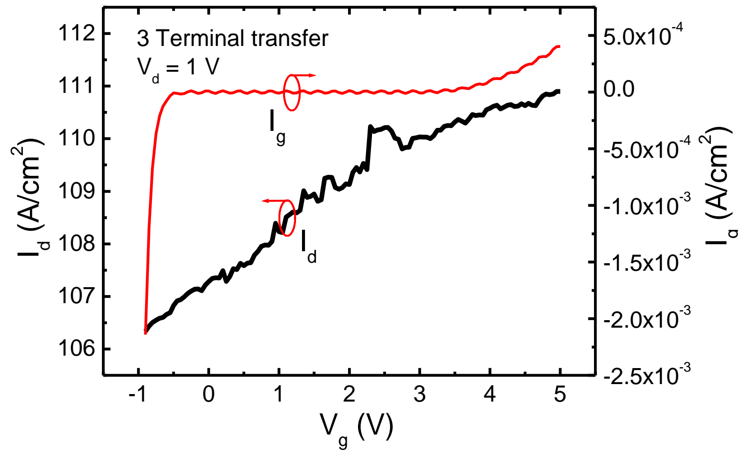

Fig. 5.13 Transfer characteristics of the n-GaN regrowth VJFET showing the drain current (black) and gate current (red).

5.4.4 Off-state leakage current analysis

In a VJFET, the blocking capability is predominantly determined by the reverse biased P-N diode. To characterize the reverse leakage current, circular P-I-N diodes with diameters ranging between 60 to 250 µm were fabricated using the same MOCVD grown template (i.e. without regrowth). The vertical leakage consists two parts: (1) bulk leakage due to the high dislocation density (~10^9 cm^{-2}) found in GaN layers grown on sapphire substrates [15] and (2) mesa sidewall leakage due to the plasma induced damage during dry-etching [16,17]. Several methods were found effective in removing of the mesa plasma damage, including N_2 plasma treatment [18], thermal annealing [19,20], NaOH and KOH wet treatments [20]. The KOH treatment was adopted in this study to evaluate the effects of sidewall leakage.

Fig. 5.14 shows the schematic structure of the fabricated diode. The wafer structures are the same as templates before regrowth as described in section 5.4.1. The fabrication starts with an activation annealing at 800 ˚C in N_2 ambient to activate the hole in the p-GaN. The mesa sidewall is etched down to the bottom n+ access layer using ICP with Cl_2-based gases under an RF power of 100 W which gives an etch rate of about 100 nm/min. To remove the plasma damage, sample 2 underwent a 1M KOH etching at 90 ˚C for 30 minutes whereas sample 1 (a

reference sample) was not treated. This is followed by the formation of p- and n- contacts using Ni/Au and Ti/Au, respectively.

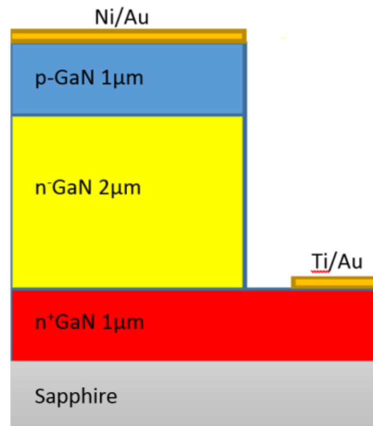

Fig. 5.14 The schematic structure of the P-I-N diode.

Fig. 5.15 (a) and (b) shows the typical reverse bias leakage currents in the reference sample and KOH treated sample, respectively. There is an overall improvement in the treated sample, particularly in the voltage range below 40 V. The leakage current in the reference sample rises quickly and does not scale with diode size. In comparison, the leakage currents in the treated sample shows a better dependence over the device area. It is believed that high energy plasma during dry-etching can create N vacancies which act as shallow donors to create a leakage path at the etched surface [18-20]. The improvement can be attributed to the removal of the defective layer at the mesa sidewall by KOH treatment.

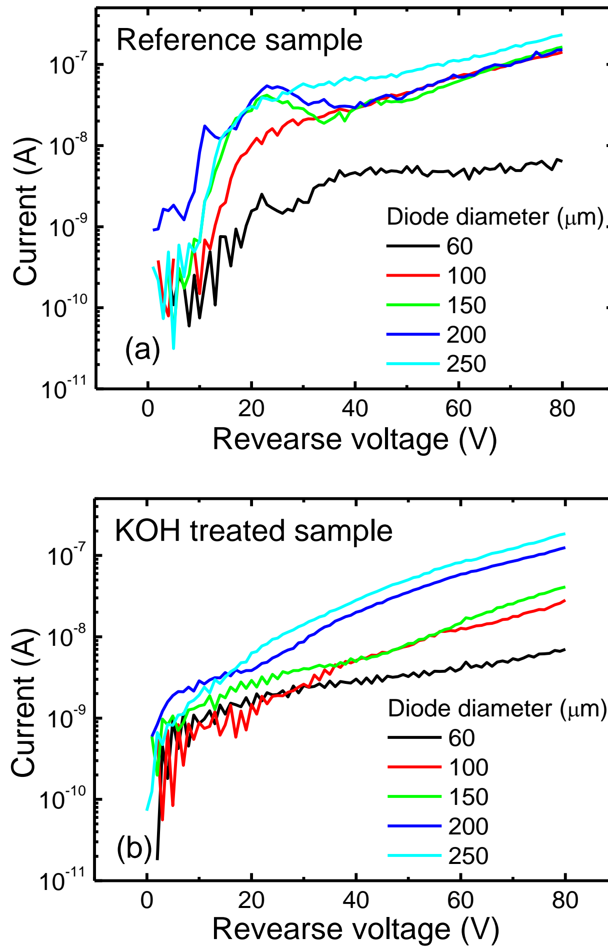

Fig. 5.15 Reverse leakage currents in (a) reference sample and (b) KOH treated sample with different diode diameters.

To further verify the suppression of sidewall leakage in the KOH treated sample, the leakage current at 80 V is plotted as a function of device area, as shown in Fig. 5.16. A linear dependence is observed which indicates the leakage is dominated by the bulk region, possibly through the dislocations [21]. It is evident that the KOH treatment is effective in suppressing the plasma damage-induced sidewall leakage.

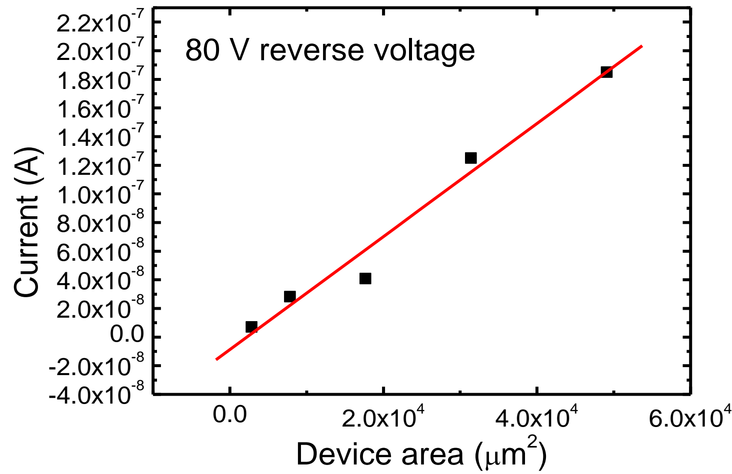

Fig. 5.16 Reverse leakage currents of the KOH treated sample at 80 V plotted as a function of device area.

5.5 Summary

Being a promising high voltage power device, as well as a building block of other vertical structures, GaN VJFET is explored in this study. The design of VJFETs is discussed in both static and transient aspects with the aid of TCAD simulation. In addition to the knowledge that already exists in the literature, it is found that the channel aspect ratio is important in determining the breakdown induced by DIBL effect. With optimized channel design, the V_{th} can be increased without compromising R_{on}. In addition, the role of p-GaN during the switching transient is presented which is rarely discussed in the literature. In power devices, a large amount of charge transfer takes place during switching due to the Miller effect. The switching speed is determined by the gate current which is limited by the p-GaN resistance. This effect is also applicable to other vertical structures that use p-GaN as a CBL.

Due to the difficulty in ion-implantation, the fabrication of VJFETs requires an epitaxial regrowth process in the trenched region. Two fabrication routes are explored – by regrowth of p-GaN or n-GaN. However, both methods show high leakage currents between the regrowth P-N junctions. TEM and EDS analyses reveal a high density of defects and contamination at the regrowth interface. As a result, the fabricated VJFETs cannot be pinched off. Wet chemical treatment using KOH proved to be effective in removing the dry-etching damage. Performing

a KOH surface pre-treatment before regrowth is advisable to improve the interface quality which could be the key to a successful device demonstration. As a pioneering work, this study provides useful insight and can form the foundation of the future development of VJFETs.

5.6 Reference

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Chapter 6 Conclusions and Recommendations for future work

6.1 Conclusions

Due to the intrinsic material properties, GaN-based devices are favourable for high voltage, high power applications. Currently, the main stream of development is focusing on lateral HEMTs which covers the medium voltage range (650 V). For higher voltage, especially for >1000 V application, vertical structures are more advantageous due to the area effectiveness. Due to the novelty of the study, the research covers the most fundamental aspects, including device design and modelling, material growth, device fabrication and characterization, both structural and electrical. Two vertical transistor structures were studied and summarized below.

6.1.1 VHEMT structure

One of the unique advantage of GaN is the ability to form the 2DEG which allows a low-loss, fast switching operation. Therefore, the VHEMT is built on the idea of utilising the 2DEG. The device was initially modelled using a TCAD simulation. It was found that V_{th} of the device can be adjusted to an E-mode by changing the thickness of AlGaN barrier and gate dielectric. The simulation also discovered an increased aperture resistance which can be explained by an equivalent cascode operation mode which is unique in this vertical structure. It was found that moving the trench away from the depletion region can alleviate the issue but can result in an increased electric field at the trench corner. The breakdown voltage of the device was also studied. Several ways were found effective in reducing the peak E-field in the structure, such as rounding the trench corner, increasing the gate dielectric thickness or moving the trench corner towards the p-GaN CBL. The results indicate that the trade-off between R_{on} and V_{br} is a key design issue to be considered in this device.

The device is based on a semi-polar (11-22) GaN template grown on m-plain sapphire substrate for two purposes: (1) to enable a plasma damage-free wet etching process in order

to achieve a good interface quality, and (2) to obtain the c-plane on a sloping sidewall to form the conduction path. A self-limiting KOH based wet etching technique was developed to obtain a V-groove. Based on the etched structure, a simpler VMOS structure was first fabricated as a precursor for the later VHEMT structure. Gate modulation was successfully demonstrated where a positive shift of V_{th} from +2 to +6 V was observed which is caused by the charged trapping at the SiN_x/GaN interface. However, the p-GaN layer in the structure showed high resistivity, possibly due to the insufficient Mg activation caused by the top encapsulation. In addition, a high leakage current through the p-GaN CBL was observed. The results indicate the importance of a good p-type layer quality.

For a full VHEMT fabrication, the AlGaN/GaN Channel regrowth was performed by both MOCVD and MBE on the patterned sample. It was found that the high temperature in MOCVD (~1000 ˚C) can lead to a mass transport of material and modifies the surface significantly. Whereas the lower temperature MBE growth (~760 ˚C) produced a uniform AlGaN/GaN structure. The regrown structure showed high background doping concentration (up to mid-10^{17} cm^{-3}) which caused a high gate leakage. Future optimizations on the regrowth process is required to obtain the correct Al mole fraction and minimize background doping.

6.1.2 VJFET structure

On the other hand, VJFET is promising for high voltage (1200 V), low loss switching applications [1]. In addition, it is the most important building block of many other vertical structures. Therefore, the VJFET structure was chosen for the study. As a preparation work, regrown P-N diode using a novel p-GaN_xAs_{1-x} was characterized. The GaN_xAs_{1-x} layer can be polycrystalline or fully amorphous depending on the Ga flux during growth. Both forward and reverse conduction showed tunnelling current dominated behaviour which is possibly due to the high hole concentration (5×10^{19} cm^{-3}) and high interfacial defect density.

The design of VJFETs is discussed in both static and transient aspects with the aid of TCAD simulation. In addition to the knowledge that already exists in the literature, it was found that

the channel aspect ratio is an important parameter. With optimized channel design, the V_{th} can be increased without compromising R_{on}. In addition, the role of p-GaN during the switching transient is presented which is rarely discussed in the literature. In power devices, large amount of charge transfer takes place during switching is to the Miller effect. The switching speed is determined by the gate current which is limited by the p-GaN resistance.

Due to the difficulty in ion-implantation, the fabrication of VJFETs requires an epitaxial regrowth process in the trenched region. Two fabrication routes are explored – by regrowth of p-GaN or n-GaN. However, both methods show high leakage currents between the regrowth P-N junctions. TEM and EDS analyses reveal a high density of defects and contamination at the regrowth interface. As a result, the fabricated VJFETs cannot be pinched off. Wet chemical treatment using KOH is proved to be effective in removing the dry-etching damage which reduced the mesa leakage significantly. As a pioneering work, this study provides useful insights and can form the foundation of the future development of VJFETs.

6.2 Recommendations for future work

The research on GaN-based vertical structure is at early stage. This work provides some alternative routes towards the realization of high performance vertical transistors. Despite the successful demonstration and fabrication of several device structures, the performance of the device requires improvement. Therefore, the following recommendations are suggested.

(1) Similar as most of the published work in the literature, the device simulation performed in this work was assuming ideal material properties. However, it is well known that GaN is susceptible to defects and trapping effects both in the bulk and at the surface of the semiconductor. The trapped charge can cause instability in V_{th} and various current collapse phenomena. Therefore, developing a model that contains the trapping effects would be helpful in understanding the device physics. In addition, performing transient and AC analyses would be interesting to estimate the device properties, such as switching loss, capacitances, and possible trapping effects.

(2) One of the difficulties in both of the VFETs is the high off-state leakage current. This is partly due to the poor crystal quality and the inability to grow thick layers on sapphire substrate. Furthermore, the quasi-vertical structure will also lead to current crowding effect as well as more complicated fabrication process. Therefore, it would be advisable to grow on bulk GaN substrates to achieve the best performance.

(3) The n-p-i-n structure described in Chapter 4 required a dry followed by wet etching process due to the slow etch rate of the p-GaN layer. This etching method was unable to produce c-plane as required for the full polarisation fields. A one-step wet etching is required which could be achieved by a PEC method to accelerate the etching in the p-GaN layer. Besides, there was no precise angular alignment tool for the photolithography to find the specific directions. For accurate alignment, proper tools, such as electron-beam lithography (EBL) are recommended.

(4) Achieving a high hole concentration in p-type GaN has always been a challenge. Especially for the MOCVD grown n-p-i-n structure, there is no free surface for the out diffusion of H atoms to prevent Mg being passivated. Consequently, the hole concentration and breakdown voltage are poor in the structure. To tackle that, MBE grown p-GaN layer may be used since it uses solid Mg as dopant source which does not require activation annealing.

(5) The regrowth on a patterned wafer is always challenging. For instance, the substrate temperature and gas ratio can vary at different height leading to non-uniform growth. In addition, defects or contaminations can be formed at regrowth surface, either during dry-etching or/and during transfer in air ambient. It is advisable to perform a surface treatment/cleaning, such as KOH and TMAH treatment, immediately prior to the regrowth process. Optimization of the growth conditions are required to bring down the background doping to the 10^{16} cm^{-3} regime.

(6) The MBE regrowth of the VJFET structure showed non-selectivity behaviour over the SiO_2 mask, GaN trench sidewall and the bottom of trench. This resulted in a formation of

polycrystalline structure, as well as thin gaps between the growth fronts. In contrast, MOCVD growth is expected to have a higher selectivity between the mask and semiconductor. And the high growth temperature is more favourable for coalescence. Therefore, MOCVD regrowth maybe promising for the VJFET structure. Yet, the mass transport and unintentional doping are the issues which need to be considered [2].

6.3 References

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Appendix A. Code for Sentaurus Input Files

Section 1: Code for VHEMT

1.1 Structure definition

```
;--------------------------------------------------------------
; Some control parameters
;--------------------------------------------------------------
(define tgate_dielectric  @tgate_dielectric@)
(define tGaN_cap          0.00)
(define NGaN_cap          1E16)
(define tAlGaN_barrier  @tAlGaN_barrier@)
(define xAlGaN          0.24)
(define NAlGaN_barrier          1E14)
(define tGaN_channel          @tGaN_channel@)
(define NGaN_channel  @NGaN_channel@)
(define tGaN_source          0.5)
(define NGaN_source          5E18)
(define tpGaN_CBL          @tpGaN_CBL@)
(define NpGaN_CBL          2E17)
(define tpenetration          (+ tGaN_channel @tpenetration@))
(define tGaN_drift          12)
(define NGaN_drift          1E16)
(define tGaN_substrate  0.1)
(define NGaN_substrate          5E18)
(define thickness1          (+ tGaN_source tpGaN_CBL tpenetration))
(define Lg1          (/ thickness1 1.6236))
(define Lg2          (/ thickness1 0.6159))
(define Ls          1)
(define Lg          (+ Lg1 Lg2))
(define Lsg          1.5)
;------------------------------------------------------------------------
; Derived parameters
;------------------------------------------------------------------------
;Vertical coordinates
(define Ytop          0)
(define Y0_AlGaN_barrier          Ytop)
(define Y0_GaN_channel          (+ Y0_AlGaN_barrier tAlGaN_barrier))
(define Y0_GaN_source          (+ Y0_GaN_channel tGaN_channel))
(define Y0_pGaN_CBL          (+ Y0_GaN_source tGaN_source))
(define Y0_GaN_drift          (+ Y0_pGaN_CBL tpGaN_CBL))
(define Y0_penetration          (+ Y0_GaN_drift tpenetration))
(define Y0_mp_GaN_channel    (- Y0_penetration (* tGaN_channel 1.375884256)))
(define Y0_mp_GaN_channel_1(- Y0_mp_GaN_channel (* (+ tAlGaN_barrier tGaN_cap)
0.85145246)))
(define Y0_mp_GaN_channel_hm          (+ Y0_mp_GaN_channel_1 (* 0.005 0.5244318)))
(define Y0_mp_GaN_channel_lm          (- Y0_penetration (* (- tGaN_channel 0.005)
1.375884256)))
(define Y0_mp_AlGaN_barrier (- Y0_penetration (* (+ tGaN_channel tAlGaN_barrier)
1.375884256)))
```

```
(define Y0_mp_GaN_cap (- Y0_penetration (* (+ tGaN_channel tAlGaN_barrier tGaN_cap) 1.375884256)))
(define Y0_mp_GaN_cap_2 (- Y0_mp_AlGaN_barrier (* tGaN_cap 0.85145246)))
(define Y0_mp_gate_dielectric (- Y0_penetration (* (+ tGaN_channel tAlGaN_barrier tGaN_cap tgate_dielectric) 1.375884256)))
(define Y0_mp_gate_dielectric_2 (- Y0_mp_GaN_cap (* tgate_dielectric 0.85145246)))
(define Y0_GaN_substrate (+ Y0_GaN_drift tGaN_drift))
(define Ybottom (+ Y0_GaN_substrate tGaN_substrate))
(define Y0_GaN_channel_1 (- Y0_GaN_source (* 0.5244318 tGaN_channel)))
(define Y0_GaN_channel_hm1 (- Y0_GaN_source (* 0.5244318 (- tGaN_channel 0.005))))
(define Y0_GaN_channel_2 (- Y0_GaN_source (* 0.85145246 tGaN_channel)))
(define Y0_GaN_channel_lm2 (- Y0_GaN_source (* 0.85145246 (- tGaN_channel 0.005))))
(define Y0_AlGaN_barrier_1 (- Y0_GaN_source (* 0.5244318 (+ tGaN_channel tAlGaN_barrier))))
(define Y0_AlGaN_barrier_2 (- Y0_GaN_source (* 0.85145246 (+ tGaN_channel tAlGaN_barrier))))
(define Y0_GaN_cap_1 (- Y0_GaN_source (* 0.5244318 (+ tGaN_channel tAlGaN_barrier tGaN_cap))))
(define Y0_GaN_cap_2 (- Y0_GaN_source (* 0.85145246 (+ tGaN_channel tAlGaN_barrier tGaN_cap))))
(define Y0_gate_dielectric_1 (- Y0_GaN_source (* 0.5244318 (+ tGaN_channel tAlGaN_barrier tGaN_cap tgate_dielectric))))
(define Y0_gate_dielectric_2 (- Y0_GaN_source (* 0.85145246 (+ tGaN_channel tAlGaN_barrier tGaN_cap tgate_dielectric))))

;Horizontal coordinates
(define Xmin 0)
(define Xsource_left1 Xmin)
(define Xsource_left2 (+ Xmin Ls))
(define Xgt.l (+ Xsource_left2 Lsg))
(define Xgt.lc (+ Xgt.l (* 0.85145246 tGaN_channel)))
(define Xgt.lchm (+ Xgt.l (* 0.85145246 (- tGaN_channel 0.005))))
(define Xgt.lb (+ Xgt.l (* 0.85145246 (+ tGaN_channel tAlGaN_barrier))))
(define Xgt.lcap(+ Xgt.l (* 0.85145246 (+ tGaN_channel tAlGaN_barrier tGaN_cap))))
(define Xgt.lgate_dielectric (+ Xgt.l (* 0.85145246 (+ tGaN_channel tAlGaN_barrier tGaN_cap tgate_dielectric))))
(define Xgt.m (+ Xgt.l Lg1))
(define Xgt.mc (+ Xgt.m (* tGaN_channel 0.3270206617)))
(define Xgt.mc_1 (- Xgt.mc (* (+ tAlGaN_barrier tGaN_cap) 0.5244318)))
(define Xgt.mc_hm (- Xgt.mc_1 (* 0.005 0.85145246)))
(define Xgt.mc_lm (+ Xgt.m (* (- tGaN_channel 0.005) 0.3270206617)))
(define Xgt.mb (+ Xgt.m (* (+ tGaN_channel tAlGaN_barrier) 0.3270206617)))
(define Xgt.mcap (+ Xgt.m (* (+ tGaN_channel tAlGaN_barrier tGaN_cap) 0.3270206617)))
(define Xgt.mcap_2 (- Xgt.mb (* tGaN_cap 0.5244318)))
(define Xgt.mdielectric (+ Xgt.m (* (+ tGaN_channel tAlGaN_barrier tGaN_cap tgate_dielectric) 0.3270206617)))
(define Xgt.mdielectric_2 (- Xgt.mdielectric (* tgate_dielectric 0.85145246)))
(define Xgt.r (+ Xgt.m Lg2))
(define Xgt.rc (- Xgt.r (* 0.5244318 tGaN_channel)))
(define Xgt.rclm (- Xgt.r (* 0.5244318 (- tGaN_channel 0.005))))
(define Xgt.rb (- Xgt.r (* 0.5244318 (+ tGaN_channel tAlGaN_barrier))))
(define Xgt.rcap (- Xgt.r (* 0.5244318 (+ tGaN_channel tAlGaN_barrier tGaN_cap))))
```

```
(define Xgt.rgate_dielectric       (- Xgt.r (* 0.5244318 (+ tGaN_channel tAlGaN_barrier tGaN_cap tgate_dielectric))))
(define Xsource_right1  (+ Xgt.r Lsg))
(define Xsource_right2  (+ Xsource_right1 Ls))
(define Xmax             Xsource_right2)
;-----------------------------------------------------------------------
; Build epi structure
;-----------------------------------------------------------------------
(sdegeo:set-default-boolean "ABA")

; sidewall passivation left
(sdegeo:create-rectangle (position (- Xmin 0.02) Y0_pGaN_CBL 0) (position Xmin Ybottom 0)  "SiO2" "sidewall_left" )
; sidewall passivation right
(sdegeo:create-rectangle (position (+ Xmax 0.02) Y0_pGaN_CBL 0) (position Xmax Ybottom 0)  "SiO2" "sidewall_right" )

;top passivation left
(sdegeo:create-polygon (list (position (+ Xmin (/ Ls 2)) Y0_gate_dielectric_1 0)  (position Xgt.lgate_dielectric Y0_gate_dielectric_1 0)(position Xgt.l Y0_GaN_source 0)(position (+ Xmin (/ Ls 2)) Y0_GaN_source 0)(position (+ Xmin (/ Ls 2)) Y0_gate_dielectric_1 0)) "SiO2" "top_passivation_left" )

;top passivation right
(sdegeo:create-polygon (list (position (- Xmax (/ Ls 2)) Y0_gate_dielectric_2 0) (position Xgt.rgate_dielectric Y0_gate_dielectric_2 0)(position Xgt.r Y0_GaN_source 0)(position (- Xmax (/ Ls 2)) Y0_GaN_source 0)(position (- Xmax (/ Ls 2)) Y0_gate_dielectric_2 0)) "SiO2" "top_passivation_right" )

; Substrate
(sdegeo:create-rectangle (position Xmin Y0_GaN_substrate 0) (position Xmax Ybottom 0)
  "GaN" "GaN_substrate" )
(sdedr:define-constant-profile "GaN_substrate_const" "ArsenicActiveConcentration" NGaN_substrate)
(sdedr:define-constant-profile-region "GaN_substrate_const" "GaN_substrate_const" "GaN_substrate")

; GaN_drift
(sdegeo:create-rectangle (position Xmin Y0_GaN_drift 0) (position Xmax Y0_GaN_substrate 0)  "GaN" "GaN_drift" )
(sdedr:define-constant-profile "GaN_drift_const" "ArsenicActiveConcentration" NGaN_drift)
(sdedr:define-constant-profile-region "GaN_drift_const" "GaN_drift_const" "GaN_drift")
(sdedr:define-refinement-size "Ref.GaN_drift" 99 0.5 66 0.3)
(sdedr:define-refinement-region "Ref.GaN_drift" "Ref.GaN_drift" "GaN_drift")
(sdedr:define-refinement-function "Ref.GaN_drift" "DopingConcentration" "MaxTransDiff" 1)

; pGaN_CBL
(sdegeo:create-rectangle (position Xmin Y0_pGaN_CBL 0) (position Xmax Y0_GaN_drift 0)
  "GaN" "pGaN_CBL" )
(sdedr:define-constant-profile "pGaN_CBL_const" "BoronActiveConcentration" NpGaN_CBL)
(sdedr:define-constant-profile-region "pGaN_CBL_const" "pGaN_CBL_const" "pGaN_CBL")
(sdedr:define-refinement-size "Ref.pGaN_CBL" 99 0.1 66 0.05)
```

```
(sdedr:define-refinement-region "Ref.pGaN_CBL_lump_1" "Ref.pGaN_CBL" "pGaN_CBL_lump_1")
(sdedr:define-refinement-region "Ref.pGaN_CBL_lump_2" "Ref.pGaN_CBL" "pGaN_CBL_lump_2")

; GaN_source
(sdegeo:create-rectangle (position (+ Xmin (/ Ls 2)) Y0_GaN_source 0) (position (- Xmax (/ Ls 2)) Y0_pGaN_CBL 0) "GaN" "GaN_source" )
(sdedr:define-constant-profile "GaN_source_const" "ArsenicActiveConcentration" NGaN_source)
(sdedr:define-constant-profile-region "GaN_source_const" "GaN_source_const" "GaN_source")
(sdedr:define-refinement-size "Ref.GaN_source" 99 0.1 66 0.05)
(sdedr:define-refinement-region "Ref.GaN_source_lump_1" "Ref.GaN_source" "GaN_source_lump_1")
(sdedr:define-refinement-region "Ref.GaN_source_lump_2" "Ref.GaN_source" "GaN_source_lump_2")

; GaN_channel
(sdegeo:create-polygon (list (position Xgt.lc Y0_GaN_channel_1 0) (position Xgt.mc_1 Y0_mp_GaN_channel_1 0) (position Xgt.mc Y0_mp_GaN_channel 0) (position Xgt.rc Y0_GaN_channel_2 0) (position Xgt.r Y0_GaN_source 0) (position Xgt.m Y0_penetration 0) (position Xgt.l Y0_GaN_source 0) (position Xgt.lc Y0_GaN_channel_1 0)) "GaN" "GaN_channel" )
(sdedr:define-constant-profile "GaN_channel_const" "ArsenicActiveConcentration" NGaN_channel)
(sdedr:define-constant-profile-region "GaN_channel_const" "GaN_channel_const" "GaN_channel")

; GaN_channel_high_mobility
(sdegeo:create-polygon (list (position Xgt.lc Y0_GaN_channel_1 0) (position Xgt.mc_1 Y0_mp_GaN_channel_1 0)(position Xgt.mc_hm Y0_mp_GaN_channel_hm 0) (position Xgt.lchm Y0_GaN_channel_hm1 0) (position Xgt.lc Y0_GaN_channel_1 0)) "GaN" "GaN_channel_hm" )
(sdedr:define-constant-profile "GaN_channel_hm_const" "ArsenicActiveConcentration" NGaN_channel)
(sdedr:define-constant-profile-region "GaN_channel_hm_const" "GaN_channel_hm_const" "GaN_channel_hm")

; GaN_channel_low_mobility
(sdegeo:create-polygon (list (position Xgt.rc Y0_GaN_channel_2 0) (position Xgt.mc Y0_mp_GaN_channel 0) (position Xgt.mc_1 Y0_mp_GaN_channel_1 0)(position Xgt.mc_hm Y0_mp_GaN_channel_hm 0) (position Xgt.mc_lm Y0_mp_GaN_channel_lm 0)(position Xgt.rclm Y0_GaN_channel_lm2 0) (position Xgt.rc Y0_GaN_channel_2 0)) "GaN" "GaN_channel_lm" )
(sdedr:define-constant-profile "GaN_channel_lm_const" "ArsenicActiveConcentration" NGaN_channel)
(sdedr:define-constant-profile-region "GaN_channel_lm_const" "GaN_channel_lm_const" "GaN_channel_lm")

;AlGaN_barrier_left
(sdegeo:create-polygon (list (position Xgt.lc Y0_GaN_channel_1 0) (position Xgt.mc_1 Y0_mp_GaN_channel_1 0) (position Xgt.mb Y0_mp_AlGaN_barrier 0) (position Xgt.lb Y0_AlGaN_barrier_1 0)(position Xgt.lc Y0_GaN_channel_1 0)) "AlGaN" "AlGaN_barrier_left" )
```

```
(sdedr:define-constant-profile "AlGaN_barrier_left_const" "ArsenicActiveConcentration"
NAlGaN_barrier)
(sdedr:define-constant-profile-region "AlGaN_barrier_left_const"
"AlGaN_barrier_left_const" "AlGaN_barrier_left")
(sdedr:define-constant-profile "xmole_AlGaN_barrier_left_const" "xMoleFraction" xAlGaN)
(sdedr:define-constant-profile-region "xmole_AlGaN_barrier_left_const"
"xmole_AlGaN_barrier_left_const" "AlGaN_barrier_left")

;AlGaN_barrier_right
(sdegeo:create-polygon (list (position Xgt.mc_1 Y0_mp_GaN_channel_1 0) (position
Xgt.mc Y0_mp_GaN_channel 0)(position Xgt.rc Y0_GaN_channel_2 0) (position Xgt.rb
Y0_AlGaN_barrier_2 0)(position Xgt.mb Y0_mp_AlGaN_barrier 0)(position Xgt.mc_1
Y0_mp_GaN_channel_1 0)) "AlGaN" "AlGaN_barrier_right" )
(sdedr:define-constant-profile "AlGaN_barrier_right_const" "ArsenicActiveConcentration"
NAlGaN_barrier)
(sdedr:define-constant-profile-region "AlGaN_barrier_right_const"
"AlGaN_barrier_right_const" "AlGaN_barrier_right")
(sdedr:define-constant-profile "xmole_AlGaN_barrier_right_const" "xMoleFraction"
xAlGaN)
(sdedr:define-constant-profile-region "xmole_AlGaN_barrier_right_const"
"xmole_AlGaN_barrier_right_const" "AlGaN_barrier_right")
;gate dielectric
(sdegeo:create-polygon (list
(position Xgt.lcap Y0_GaN_cap_1 0)(position Xgt.mcap Y0_mp_GaN_cap 0)(position
Xgt.rcap Y0_GaN_cap_2 0)(position Xgt.rgate_dielectric Y0_gate_dielectric_2 0)(position
Xgt.mdielectric Y0_mp_gate_dielectric 0)(position Xgt.lgate_dielectric
Y0_gate_dielectric_1 0)(position Xgt.lcap Y0_GaN_cap_1 0))
 "Nitride" "gate_dielectric")
;-------------------------------------------------------------------------
; Define electrodes
;-------------------------------------------------------------------------
;gate-------------------------------------------------------------------------------------
(define gt.metal.top (sdegeo:create-polygon (list (position Xgt.lgate_dielectric
Y0_gate_dielectric_1 0) (position Xgt.mdielectric Y0_mp_gate_dielectric 0) (position
Xgt.rgate_dielectric Y0_gate_dielectric_2 0) (position Xgt.lgate_dielectric
Y0_gate_dielectric_1 0)) "Metal" "tmp.gate.top" ))
(sdegeo:define-contact-set "gate")
(sdegeo:set-current-contact-set "gate")
(sdegeo:set-contact-boundary-edges gt.metal.top)
(sdegeo:delete-region gt.metal.top)
;source & drain-------------------------------------------------------------------
(sdegeo:insert-vertex (position Xsource_left2 Y0_GaN_source 0.0))
(sdegeo:insert-vertex (position Xsource_right1 Y0_GaN_source 0.0))
(sdegeo:insert-vertex (position (+ Xsource_left1 (/ Ls 3)) Y0_pGaN_CBL 0.0))
(sdegeo:insert-vertex (position (- Xsource_right2 (/ Ls 3)) Y0_pGaN_CBL 0.0))
(sdegeo:define-contact-set "source_left")
(sdegeo:set-current-contact-set "source_left")
(sdegeo:define-2d-contact (find-edge-id (position (- Xsource_left2 0.05) Y0_GaN_source 0))
"source_left")
(sdegeo:define-contact-set "source_right")
(sdegeo:set-current-contact-set "source_right")
(sdegeo:define-2d-contact (find-edge-id (position (+ Xsource_right1 0.05) Y0_GaN_source
0)) "source_right")
(sdegeo:define-contact-set "source_CBL")
(sdegeo:set-current-contact-set "source_CBL")
```

```
(sdegeo:define-2d-contact (find-edge-id (position (+ Xsource_left1 0.05) Y0_pGaN_CBL 0.0)) "source_CBL")
(sdegeo:define-2d-contact (find-edge-id (position (- Xsource_right2 0.05) Y0_pGaN_CBL 0.0)) "source_CBL")
(sdegeo:define-contact-set "drain")
(sdegeo:set-current-contact-set "drain")
(sdegeo:define-2d-contact (find-edge-id (position  (+ Xmin 0.5) Ybottom 0)) "drain")

;-----------------------------------------------------------------------------------------------------
;Meshing
;-----------------------------------------------------------------------------------------------------

; Global
(sdedr:define-refinement-window "pl.Globle" "Rectangle" (position Xmin Ytop 0) (position Xmax Ybottom 0))
(sdedr:define-refinement-size "Ref.Globle" 0.5   1 0 0.25 0.5 0)
(sdedr:define-refinement-placement "Ref.Globle" "Ref.Globle" "pl.Globle")
;;(sdedr:define-refinement-function "Ref.Globle" "MaxLenInt" "GaN" "AlGaN" 0.005 2 "DoubleSide")
(sdedr:define-refinement-function "Ref.Globle" "MaxLenInt" "GaN_source_lump_1" "pGaN_CBL_lump_1" 0.005 1.6 "DoubleSide" "UseRegionNames")
(sdedr:define-refinement-function "Ref.Globle" "MaxLenInt" "GaN_source_lump_2" "pGaN_CBL_lump_2" 0.005 1.6 "DoubleSide" "UseRegionNames")
(sdedr:define-refinement-function "Ref.Globle" "MaxLenInt" "GaN_source_lump_1" "GaN_channel" 0.01 3 "UseRegionNames")
(sdedr:define-refinement-function "Ref.Globle" "MaxLenInt" "GaN_source_lump_2" "GaN_channel" 0.01 3 "UseRegionNames")
(sdedr:define-refinement-function "Ref.Globle" "MaxLenInt" "GaN_drift" "pGaN_CBL_lump_1" 0.005 1.6 "UseRegionNames")
(sdedr:define-refinement-function "Ref.Globle" "MaxLenInt" "GaN_drift" "pGaN_CBL_lump_2" 0.005 1.6 "UseRegionNames")
(sdedr:define-refinement-function "Ref.Globle" "MaxLenInt" "pGaN_CBL_lump_1" "GaN_drift" 0.005 1.6 "UseRegionNames")
(sdedr:define-refinement-function "Ref.Globle" "MaxLenInt" "pGaN_CBL_lump_2" "GaN_drift" 0.005 1.6 "UseRegionNames")
(sdedr:define-refinement-function "Ref.Globle" "MaxLenInt" "pGaN_CBL_lump_1" "GaN_channel" 0.01 3 "DoubleSide" "UseRegionNames")
(sdedr:define-refinement-function "Ref.Globle" "MaxLenInt" "pGaN_CBL_lump_2" "GaN_channel" 0.01 3 "DoubleSide" "UseRegionNames")
(sdedr:define-refinement-function "Ref.Globle" "MaxLenInt" "GaN_drift" "GaN_channel" 0.04 2 "UseRegionNames")
(sdedr:define-refinement-function "Ref.Globle" "MaxLenInt" "GaN_drift" "GaN_substrate" 0.02 3 "DoubleSide" "UseRegionNames")
(sdedr:define-refinement-function "Ref.Globle" "MaxLenInt" "GaN" "SiO2" 0.01 2 "DoubleSide")
;drift depletion region
(sdedr:define-refinement-window "pl.drift_depletion" "Rectangle" (position Xmin Y0_GaN_drift 0) (position Xmax (+ Y0_GaN_drift 0.6) 0))
(sdedr:define-refinement-size "Ref.drift_depletion" 99 0.1 0 66 0.05 0)
(sdedr:define-refinement-placement "Ref.drift_depletion" "Ref.drift_depletion" "pl.drift_depletion")
; Left source
(sdedr:define-refinement-window "pl.source_left" "Rectangle" (position (- Xsource_left2 0.1) Y0_GaN_source 0) (position (+ Xsource_left2 0.1) (+ Y0_GaN_source 0.03) 0))
(sdedr:define-refinement-size "Ref.source_left" 0.04 0.01 0 0.02 0.005 0)
```

```
(sdedr:define-refinement-placement "Ref.source_left" "Ref.source_left" "pl.source_left")
; Right source
(sdedr:define-refinement-window "pl.source_right" "Rectangle" (position (- Xsource_right1
0.1) Y0_GaN_source 0) (position (+ Xsource_right1 0.1) (+ Y0_GaN_source 0.03) 0))
(sdedr:define-refinement-size "Ref.source_right" 0.04 0.01 0 0.02 0.005 0)
(sdedr:define-refinement-placement "Ref.source_right" "Ref.source_right" "pl.source_right")
;------------------------------------------------------------------
; Meshing Offseting
;------------------------------------------------------------------;
(sdenoffset:create-global
 "usebox" 2
 "maxangle" 60)
(sdenoffset:create-noffset-interface "Material" "AlGaN" "Nitride"
 "hlocal" 0.001
 "factor" 2)
(sdenoffset:create-noffset-interface "Material" "Nitride" "AlGaN"
 "hlocal" 0.001
 "factor" 1.3)
(sdenoffset:create-noffset-interface "material" "AlGaN" "GaN"
 "hlocal" 0.001
 "factor" 2)
(sdenoffset:create-noffset-interface "material" "GaN" "AlGaN"
 "hlocal" 0.001
 "factor" 2)
(sdenoffset:create-noffset-interface "region" "GaN_channel" "GaN_channel_hm"
"hlocal" 0.008
 "factor" 1.4)
(sdenoffset:create-noffset-interface "region" "GaN_channel" "GaN_channel_lm"
"hlocal" 0.008
 "factor" 1.4)
(sdenoffset:create-noffset-interface "region" "GaN_channel" "pGaN_CBL_lump_1"
 "hlocal" 0.01
 "factor" 2)
(sdenoffset:create-noffset-interface "region" "GaN_channel" "pGaN_CBL_lump_2"
 "hlocal" 0.01
 "factor" 2)
(sdenoffset:create-noffset-interface "region" "GaN_channel" "GaN_source_lump_1"
 "hlocal" 0.01
 "factor" 2)
(sdenoffset:create-noffset-interface "region" "GaN_channel" "GaN_source_lump_2"
 "hlocal" 0.01
 "factor" 2)
(sdenoffset:create-noffset-interface "region" "GaN_channel" "GaN_drift"
 "hlocal" 0.02
 "factor" 2)
;----------------------------------------------------------------------
(sde:build-mesh "snmesh" "-offset" "n@node@") ;
;----------------------------------------------------------------------
```

1.2 Sdevice file

```
Electrode {
	{ Name="gate"   Voltage= 0 Schottky Workfunction= 4.7 }
```

```
	{ Name="source_left" Voltage= 0 DistResist=12E-6 }
	{ Name="source_right" Voltage= 0 DistResist=12E-6 }
	{ Name="source_CBL" Voltage= 0 DistResist=1E-3 }
	{ Name="drain"  Voltage= 0 DistResist=12E-6 }
}

File {
	Grid= "@tdr@"
	Parameter= "@parameter@"
	Current= "@plot@"
	Plot= "@tdrdat@"
	Output= "@log@"
}

Physics {
	AreaFactor= 1000			* So that currents are given in A/mm
	Mobility (
		DopingDependence
		Highfieldsaturation
	)
	EffectiveIntrinsicDensity (Nobandgapnarrowing)
	Fermi
	Recombination (SRH)

	Thermionic

	DefaultParametersFromFile	* Use parameter files within the MaterialDB
directory to determine defaults.
}


Physics (RegionInterface="AlGaN_barrier_left/gate_dielectric") {
	Traps (
		(Fixedcharge Conc=-@pol_charge@)
		(Donor Level Conc= @N_surf@ EnergyMid= 1.6 FromCondBand)
	)
}

Physics (RegionInterface="GaN_channel_hm/AlGaN_barrier_left") {
	Traps (
Fixedcharge Conc=@pol_charge@)
}

Plot {
	Electricfield/Vector
	eCurrent/Vector hCurrent/Vector TotalCurrent/Vector
	SRH
	eMobility hMobility
	eGradQuasiFermi hGradQuasiFermi
	eEparallel hEparallel
	eVelocity hVelocity
	DonorConcentration Acceptorconcentration
	Doping SpaceCharge
	ConductionBand ValenceBand eQuasiFermiEnergy hQuasiFermiEnergy
	BandGap Affinity
```

```
        xMoleFraction
        eBarrierTunneling
        eTrappedCharge hTrappedCharge
}

Math {
        Extrapolate
        Iterations= 12
        DirectCurrentComputation
        ExtendedPrecision
        Digits= 8
        RHSMin= 1e-15
        eDrForceRefDens= 1e8
        hDrForceRefDens= 1e8

        CNormPrint
        NewtonPlot (
          Error MinError
          Residual
        )
  eMobilityAveraging= ElementEdge
  * uses edge mobility instead of element one for electron mobility
  hMobilityAveraging= ElementEdge
  * uses edge mobility instead of element one for hole mobility
  GeometricDistances
  * when needed, compute distance to the interface instead of closest point on the interface
  ParameterInheritance= Flatten
  * regions inherit parameters from materials
  }

Solve {
        Coupled (Iterations= 10000 LinesearchDamping= 1e-5) {Poisson}
        Coupled (Iterations= 10000 LinesearchDamping= 1e-5) {Poisson Electron Hole}
        Plot(FilePrefix="n@node@_zero")

        NewCurrentFile="n@node@_Vd_ramp_"
        Quasistationary (
                InitialStep= 0.01 Minstep= 1e-4 MaxStep= 0.1
                Goal{Name="drain" Voltage= 10}
        ) {
                Coupled {Poisson Electron Hole}
                Plot(FilePrefix="n@node@_Vd10V" Time=(1))
        }

        NewCurrentFile="n@node@_Vg_positive_"
        Load(FilePrefix="n@node@_Vd10V")
        Quasistationary (
                InitialStep= 0.005 Minstep= 1e-4 MaxStep= 0.03
                Goal{Name="gate" Voltage= 10}
        ) {
                Coupled {Poisson Electron Hole}
                Plot(FilePrefix="n@node@_Vg2V" Time=(0.2))
                Plot(FilePrefix="n@node@_Vg4V" Time=(0.4))
                Plot(FilePrefix="n@node@_Vg6V" Time=(0.6))
                Plot(FilePrefix="n@node@_Vg8V" Time=(0.8))
```

```
        Plot(FilePrefix="n@node@_Vg10V" Time=(0.1))
    }
```

1.3 Parameter file

```
#define ParFileDir .
Material="GaN" {
#includeext "ParFileDir/sdevice_GaN.par"}
Material= "GaN" {
    ConstantMobility:
    { * mu_const = mumax (T/T0)^(-Exponent)
        mumax = 900 ,  150              # [cm2/(Vs)]
        Exponent      = 1 ,     2.1              # [1]
    }

    Epsilon
    { * Ratio of the permittivities of material and vacuum
      * epsilon() = epsilon
        epsilon  = 10.4   # [1]
    }

    Epsilon_Aniso
    { * Ratio of the permittivities of material and vacuum
      * epsilon() = epsilon
        epsilon  = 10.4   # [1]
    }

    # Adjust velocity saturation temperature dependence
    HighFieldDependence:
    {
        Vsat_Formula   = 2 ,     2              # [1]
        * Formula2 for saturation velocity:
        *       vsat = A_vsat - B_vsat*(T/T0)
        * A_vsat        = 1.8e7 ,        1.0000e+07          # [1]
        * B_vsat        = 0 ,     0                  # [1] (default in F-
2011.09)

        A_vsat  = 2.5e7 ,         1.0000e+07
        B_vsat  = 2.3e6 ,         0
        # Approximation to match results shown in figure 3 of Benbakhti et al, IEEE
Trans Electron Dev., 56-10, p.2178 (2009)

}

    # Tunneling masses are made very small in this example. The objective of this setup
is
    # to obtain near zero contact resistance. Tunneling masses mt can also be calibrated
to
    # render experimentally observed contact resistances
    BarrierTunneling {
        mt      = 0.05, 0.05     # [1]
        g       = 1,    1            # [1]
```

```
		}
}
Material= "AlN" {
	Epsilon
	{ * Ratio of the permittivities of material and vacuum
	  * epsilon() = epsilon
		epsilon  = 9.14   # [1]
	}

	Epsilon_Aniso
	{ * Ratio of the permittivities of material and vacuum
	  * epsilon() = epsilon
		epsilon  = 10.7   # [1]
	}

	BarrierTunneling {
		mt	= 0.05, 0.05	# [1]
		g	= 1,	1		# [1]
	}
}

Region= "GaN_channel_hm" {

	* Higher value for constant mobility in the 2DEG channel
	ConstantMobility:
	{ * mu_const = mumax (T/T0)^(-Exponent)
		mumax = 1750 ,		150		# [cm2/(Vs)]
		Exponent	= 1 ,	2.1			# [1]
	}
}

Region= "GaN_channel_lm" {

	*  Lower value for constant mobility in the inversion channel
	ConstantMobility:
	{ * mu_const = mumax (T/T0)^(-Exponent)
		mumax = 100 ,  50		# [cm2/(Vs)]
		Exponent	= 1 ,	2.1			# [1]
	}
}
```

Section 2: Code for VJFET

2.1 Structure definition

```
;-----------------------------------------------------------------------------------------------------
; control parameters
;-----------------------------------------------------------------------------------------------------
(define		tGaN_drift	12)
(define		xGaN_drift	@xGaN_drift@)
(define		tpGaN		@tpGaN@)
```

```
(define        xpGaN          @xpGaN@) ;2E17
(define        tGaN_channel   (+ tpGaN 0.5))
(define        xGaN_channel   @xGaN_channel@)
(define        tGaN_top       0.2)
(define        tGaN_drain     1)
(define        xsourcenGaN    5e18)
(define        xdrainnGaN     5e18)
(define        tpenetration   0)
(define        tSiN           0.1)
(define        lGaN_channel   @lGaN_channel@)
(define        lGaN_drift     (+ lGaN_channel 78))
(define        lGaN_drain     (+ lGaN_drift 20))
(define        lpGaN          39)
(define        lgate          15)
(define        ldrain         10)

;device parameters
(define        Ysource_top    0)
(define        Ysource_bot    (+ Ysource_top tpGaN))
(define        YnGaN_top      (+ Ysource_top tGaN_top))
(define        YnGaN_bot      (+ Ysource_bot tGaN_top))
(define        YpGaN          (+ YnGaN_top tGaN_channel))
(define        YGaN_drift     (+ YpGaN tpGaN))
(define        YGaN_drain     (+ YGaN_drift tGaN_drift))
(define        Ybottom                (+ YGaN_drain tGaN_drain))
(define        YSiN_pGaN      (- YpGaN tSiN))
(define        YSiN_nGaN      (- YGaN_drain tSiN))

(define        Xleft          0)
(define        XpGaN_left1    0)
(define        XpGaN_left2    (+ Xleft lpGaN))
(define        XpGaN_right1   (+ XpGaN_left2 lGaN_channel))
(define        XpGaN_right2   (+ XpGaN_right1 lpGaN))
(define        XnGaN_drain1   0)
(define        XnGaN_drain2   (+ XpGaN_right2 20))
(define        XnGaN_source1          (- XpGaN_left2 6))
(define        XnGaN_source2          (+ XpGaN_right1 6))
(define        Xmid           (/ XpGaN_right2 2))
(define        Xmax           XnGaN_drain2)

;--------------------------------------------------------------------------------------------------------
;Build epi structure
;--------------------------------------------------------------------------------------------------------

(sdegeo:set-default-boolean "ABA")

;Source n+GaN_top1
(sdegeo:create-rectangle (position XnGaN_source1 Ysource_top 0) (position XpGaN_left2
YnGaN_top 0)  "GaN" "sourcenGaN_top1"   )
(sdedr:define-constant-profile                              "ndop_sourcenGaN_top1_const"
"ArsenicActiveConcentration" xsourcenGaN)
(sdedr:define-constant-profile-region                       "ndop_sourcenGaN_top1_const"
"ndop_sourcenGaN_top1_const" "sourcenGaN_top1")
;Source n+GaN_top2
```

```
(sdegeo:create-rectangle (position XpGaN_right1 Ysource_top 0) (position XnGaN_source2 YnGaN_top 0)   "GaN" "sourcenGaN_top2"   )
(sdedr:define-constant-profile "ndop_sourcenGaN_top2_const" "ArsenicActiveConcentration" xsourcenGaN)
(sdedr:define-constant-profile-region "ndop_sourcenGaN_top2_const" "ndop_sourcenGaN_top2_const" "sourcenGaN_top2")
;Source n+GaN_bot
(sdegeo:create-rectangle   (position XpGaN_left2 Ysource_bot 0) (position XpGaN_right1 YnGaN_bot 0)   "GaN" "sourcenGaN_bot"  )
(sdedr:define-constant-profile "ndop_sourcenGaN_bot_const" "ArsenicActiveConcentration" xsourcenGaN)
(sdedr:define-constant-profile-region "ndop_sourcenGaN_bot_const" "ndop_sourcenGaN_bot_const" "sourcenGaN_bot")
;n-GaN top at source left
(sdegeo:create-rectangle   (position XnGaN_source1 YnGaN_top 0) (position XpGaN_left2 YpGaN 0)
  "GaN" "sourceGaN_top1"  )
(sdedr:define-constant-profile "ndop_sourceGaN_top1_const" "ArsenicActiveConcentration" xGaN_channel)
(sdedr:define-constant-profile-region "ndop_sourceGaN_top1_const" "ndop_sourceGaN_top1_const" "sourceGaN_top1")
;n-GaN top at source right
(sdegeo:create-rectangle   (position XpGaN_right1 YnGaN_top 0) (position XnGaN_source2 YpGaN 0)   "GaN" "sourceGaN_top2"   )
(sdedr:define-constant-profile "ndop_sourceGaN_top2_const" "ArsenicActiveConcentration" xGaN_channel)
(sdedr:define-constant-profile-region "ndop_sourceGaN_top2_const" "ndop_sourceGaN_top2_const" "sourceGaN_top2")
;p-GaN left
(sdegeo:create-rectangle   (position XpGaN_left1 YpGaN 0) (position XpGaN_left2 YGaN_drift 0)
  "GaN" "pGaN_left"   )
(sdedr:define-constant-profile "pdop_pGaN_left_const" "BoronActiveConcentration" xpGaN)
(sdedr:define-constant-profile-region "pdop_pGaN_left_const" "pdop_pGaN_left_const" "pGaN_left")
;p-GaN right
(sdegeo:create-rectangle   (position XpGaN_right1 YpGaN 0) (position XpGaN_right2 YGaN_drift 0)
  "GaN" "pGaN_right"   )
(sdedr:define-constant-profile "pdop_pGaN_right_const" "BoronActiveConcentration" xpGaN)
(sdedr:define-constant-profile-region "pdop_pGaN_right_const" "pdop_pGaN_right_const" "pGaN_right")
;n-GaN drift
(sdegeo:create-rectangle   (position Xleft YGaN_drift 0) (position XpGaN_right2 YGaN_drain 0)
  "GaN" "GaN_drift"   )
(sdedr:define-constant-profile "ndop_GaN_drift_const" "ArsenicActiveConcentration" xGaN_drift)
(sdedr:define-constant-profile-region "ndop_GaN_drift_const" "ndop_GaN_drift_const" "GaN_drift")
;n-GaN channel
(sdegeo:create-rectangle   (position XpGaN_left2 YnGaN_bot 0) (position XpGaN_right1 (+ YGaN_drift tpenetration) 0)   "GaN" "nGaN_channel"   )
```

```
(sdedr:define-constant-profile "ndop_nGaN_channel_const" "ArsenicActiveConcentration" xGaN_channel)
(sdedr:define-constant-profile-region "ndop_nGaN_channel_const" "ndop_nGaN_channel_const" "nGaN_channel")
;Drain n+GaN
(sdegeo:create-rectangle
 (position XnGaN_drain1 YGaN_drain 0) (position XnGaN_drain2 Ybottom 0) "GaN" "drainnGaN" )
(sdedr:define-constant-profile "ndop_drainnGaN_const" "ArsenicActiveConcentration" xdrainnGaN)
(sdedr:define-constant-profile-region "ndop_drainnGaN_const" "ndop_drainnGaN_const" "drainnGaN")
;SiN_nGaN_drain
(sdegeo:create-rectangle (position XpGaN_right2 YGaN_drain 0) (position XnGaN_drain2 YSiN_nGaN 0) "Nitride" "SiN_nGaN" )
;SiN_pGaN_left
(sdegeo:create-rectangle
 (position XpGaN_left1 YpGaN 0) (position XnGaN_source1 YSiN_pGaN 0) "Nitride" "SiN_pGaN_left" )
;SiN_pGaN_right
(sdegeo:create-rectangle (position XpGaN_right2 YpGaN 0) (position XnGaN_source2 YSiN_pGaN 0) "Nitride" "SiN_pGaN_right" )
;-----------------------------------------------------------------------------------------------------
;Define contacts
;-----------------------------------------------------------------------------------------------------
(sdegeo:insert-vertex (position (+ XpGaN_left1 13) YpGaN 0.0))
(sdegeo:insert-vertex (position (+ XpGaN_left1 28) YpGaN 0.0))
(sdegeo:insert-vertex (position (- XpGaN_right2 13) YpGaN 0.0))
(sdegeo:insert-vertex (position (- XpGaN_right2 28) YpGaN 0.0))
(sdegeo:insert-vertex (position (- XnGaN_drain2 10) YGaN_drain 0.0))
(sdegeo:insert-vertex (position (- XpGaN_left2 3) Ysource_top 0.0))
(sdegeo:insert-vertex (position (+ XpGaN_right1 3) Ysource_top 0.0))
(sdegeo:define-contact-set "drain" 4.0 (color:rgb 1.0 0.0 0.0) "##")
(sdegeo:define-contact-set "source" 4.0 (color:rgb 1.0 0.0 0.0) "##")
(sdegeo:define-contact-set "gate" 4.0 (color:rgb 1.0 0.0 0.0) "##")
;drain contact
(sdegeo:define-2d-contact (find-edge-id (position (- XnGaN_drain2 2) YGaN_drain 0)) "drain")
;Source contact
(sdegeo:define-2d-contact (find-edge-id (position (+ XnGaN_source1 4) 0 0)) "source")
(sdegeo:define-2d-contact (find-edge-id (position (- XnGaN_source2 4) 0 0)) "source")
(sdegeo:define-2d-contact (find-edge-id (position (+ XpGaN_left2 0.5) Ysource_bot 0)) "source")
;Gate contact left
(sdegeo:define-2d-contact (find-edge-id (position (+ XpGaN_left1 14) YpGaN 0)) "gate")
;Gate contact right
(sdegeo:define-2d-contact (find-edge-id (position (- XpGaN_right2 14) YpGaN 0)) "gate")
;-----------------------------------------------------------------------------------------------------
;Meshing
;-----------------------------------------------------------------------------------------------------
; Global
(sdedr:define-refinement-window "Pl.global" "Rectangle"
(position 0 0 0) (position XnGaN_drain2 Ybottom 0))
(sdedr:define-refinement-size "Ref.global" (/ Xmax 10) (/ Ybottom 50) 0 (/ Xmax 20) (/ Ybottom 100) 0)
```

```
(sdedr:define-refinement-placement "Ref.global" "Ref.global" "Pl.global")
(sdedr:define-refinement-function "Ref.global" "DopingConcentration" "MaxTransDiff" 1)
(sdedr:define-refinement-function "Ref.global" "MaxLenInt" "GaN_drift" "drainnGaN"
0.001 6 "DoubleSide" "UseRegionNames")
(sdedr:define-refinement-function "Ref.global" "MaxLenInt" "pGaN_left" "GaN_drift" 0.01
1.4 "DoubleSide" "UseRegionNames")
(sdedr:define-refinement-function "Ref.global" "MaxLenInt" "pGaN_right" "GaN_drift" 0.01
1.4 "DoubleSide" "UseRegionNames")
(sdedr:define-refinement-function "Ref.global" "MaxLenInt" "pGaN_left" "nGaN_channel"
0.008 1.4 "DoubleSide" "UseRegionNames")
(sdedr:define-refinement-function "Ref.global" "MaxLenInt" "pGaN_right" "nGaN_channel"
0.008 1.4 "DoubleSide""UseRegionNames")
(sdedr:define-refinement-function "Ref.global" "MaxLenInt" "sourceGaN_top1"
"pGaN_left" 0.008 1.4 "DoubleSide" "UseRegionNames")
(sdedr:define-refinement-function "Ref.global" "MaxLenInt" "sourceGaN_top2"
"pGaN_right" 0.008 1.4 "DoubleSide" "UseRegionNames")
;channel
(sdedr:define-refinement-window "pl.channel" "Rectangle" (position (- Xmid 0.02) (- YpGaN
0.1) 0) (position (+ Xmid 0.02) (+ YGaN_drift 0.5) 0))
(sdedr:define-refinement-size "Ref.channel" 0.02 0.2 0 0.01 0.1 0)
(sdedr:define-refinement-placement "Ref.channel" "Ref.channel" "pl.channel")
(sdedr:define-refinement-size "Ref.nGaN_channel" 0.05 0.2 0.25 0.1 )
(sdedr:define-refinement-region "Ref.nGaN_channel" "Ref.nGaN_channel"
"nGaN_channel" )
;p-GaN depletion left
(sdedr:define-refinement-size "Ref.pGaN_left" 99 0.1 66 0.05 )
(sdedr:define-refinement-region "Ref.pGaN_left" "Ref.pGaN_left" "pGaN_left" )
;p-GaN depletion right
(sdedr:define-refinement-size "Ref.pGaN_right" 99 0.1 66 0.05 )
(sdedr:define-refinement-region "Ref.pGaN_right" "Ref.pGaN_right" "pGaN_right" )
;below channel
;p-GaN/source_nGaN interface
(sdedr:define-refinement-window "pl.interface2" "Rectangle"
(position XnGaN_source1 (- YpGaN 0.8) 0) (position XnGaN_source2 (+ YpGaN 0.2) 0))
(sdedr:define-refinement-size "Ref.interface2" 2 0.03 0 1 0.015 0)
(sdedr:define-refinement-placement "Ref.interface2" "Ref.interface2" "pl.interface2")
(sdedr:define-refinement-function "Ref.interface2" "DopingConcentration" "MaxTransDiff"
1)
;drain cornor1
(sdedr:define-refinement-window "pl.drain_cornor1" "Rectangle" (position (- Xmax 10.15)
YGaN_drain 0) (position (- Xmax 9.95) (+ YGaN_drain 0.1) 0))
(sdedr:define-refinement-size "Ref.drain_cornor1" 0.01 0.01 0 0.005 0.005 0)
(sdedr:define-refinement-placement "Ref.drain_cornor1" "Ref.drain_cornor1"
"pl.drain_cornor1")
;------------------------------------------------------------------------
(sde:build-mesh "snmesh" "" "n@node@")
;------------------------------------------------------------------------
```

2.2 Sdevice file

```
Device JFET {
File {
	Grid= "@tdr@"
```

```
        Parameter= "@parameter@"
        Current= "@plot@"
        Plot= "@tdrdat@"
}
Electrode {
     { Name="gate"   Voltage= 0 }
     { Name="source" Voltage= 0  0 DistResist=12E-6 }
     { Name="drain"  Voltage= 0  0 DistResist=12E-6 }
}
Physics {
        AreaFactor= 1e5
        Mobility (
                DopingDependence
                Highfieldsaturation
        )
        EffectiveIntrinsicDensity (Nobandgapnarrowing)
        Fermi
        Recombination( SRH )
        DefaultParametersFromFile
}}
File {
  Output= "@log@"
}
Plot {
        Electricfield/Vector
        eCurrent/Vector hCurrent/Vector TotalCurrent/Vector
        SRH eAvalanche hAvalanche Auger
        eDensity hDensity
        eMobility hMobility
        eGradQuasiFermi hGradQuasiFermi
        eEparallel hEparallel
        eVelocity hVelocity
        DonorConcentration Acceptorconcentration
        Doping SpaceCharge
        ConductionBand ValenceBand eQuasiFermiEnergy hQuasiFermiEnergy
        BandGap Affinity
        }
Math {
        Extrapolate
        Iterations= 40
        DirectCurrentComputation
        ExtendedPrecision
        Digits= 8
        RHSMin= 1e-15
        eDrForceRefDens= 1e8
        hDrForceRefDens= 1e8
        CNormPrint
        eMobilityAveraging= ElementEdge
        * uses edge mobility instead of element one for electron mobility
        hMobilityAveraging= ElementEdge
        * uses edge mobility instead of element one for hole mobility
        GeometricDistances
        * when needed, compute distance to the interface instead of closest
        * point on the interface
        ParameterInheritance= Flatten
```

```
            * regions inherit parameters from materials
}
System {
  JFET (source=0 gate=2 drain=3)
  Vsource_pset vd  (4 0) { dc= 0 }
  Vsource_pset vg  (5 0) { pwl= (0 0 1e-7 0 1.01e-7 3 8e-7 3)}
  Resistor_pset rg (5 2) { resistance= @Rg@ }
  Resistor_pset rd (6 3) { resistance= 0.001 }
  Isource_pset isource (4 6) { dc= 0.5 }
#   Inductor_pset Ld (4 3) { inductance = 500e-6 }
  Diode_pset     dioded  (6 4) { }
  Plot "n@node@_1" (time() v(2) v(3) v(4) v(5) i(rd 3) i(rg 2))
}

Solve {
            Poisson
            Coupled (Iterations= 10000 LinesearchDamping= 1e-4) {Poisson}
            Coupled (Iterations= 10000 LinesearchDamping= 1e-4) {Poisson Electron Hole}
            Plot(FilePrefix="n@node@_zero")
#drain ramp
            NewCurrentFile="n@node@_Vd_ramp_"
            Quasistationary (
                        InitialStep= 0.01 Minstep= 1e-4 MaxStep= 0.1
                        Goal{Parameter=vd.dc Value= 600}
            ) {         Coupled {Poisson Electron Hole}
                        Plot(FilePrefix="n@node@_Vd=10V" Time=(1))}
  NewCurrentPrefix="Transient"
  Transient (
    InitialTime= 0 FinalTime= 8e-7
    InitialStep= 1e-9 Increment= 1.5 Decrement= 2
    MinStep=5e-10 MaxStep= 5e-8
  ){ Coupled { Poisson Electron hole}
}
}
```

2.3 Parameter file

```
#define ParFileDir .
Material="GaN" {
#  #includeext "ParFileDir/sdevice_GaN.par"
}
Region="pGaN_left" {
            * changing hole mobility
            ConstantMobility:
            { * mu_const = mumax (T/T0)^(-Exponent)
                        mumax = 900 ,  @h_mobility@ #150                # [cm2/(Vs)]
                        Exponent          = 1 ,      1 #2.1             # [1]
            }}
Region="pGaN_right" {

            * changing hole mobility
            ConstantMobility:
            { * mu_const = mumax (T/T0)^(-Exponent)
```

```
                mumax = 900 ,  @h_mobility@ #150                 # [cm2/(Vs)]
                Exponent        = 1 ,      1 #2.1                # [1]
        }}
#Material="Nitride" {
#  #includeext "ParFileDir/Nitride.par"
#}
```

Appendix B. Key Fabrication Processes

1. Photolithography

Photolithography is used to transfer the patterns from a mask onto a sample using UV light and a UV light-sensitive photoresist (PR). The procedures are summarized below.

(1) Standard 3-step cleaning in n-butyl, acetone and IPA

(2) Pre-bake on a 100 ˚C hotplate for 1 min

(3) Spin at 4000 rpm using corresponding photoresist for the correct thickness (SPR350 = 1 μm, BPRS200 = 2.2 μm, SPR350 = 4.7 μm) and bake on a 100 ˚C hotplate for 1 min

(4) Expose the edge to remove edge bead and develop in MF26A developer for 30 sec

(5) Expose using aligner (UV300) for the correct exposure time (SPR350 =11 sec, BPRS200 = 25 sec, SPR350 = 53 sec)

(6) Develop in MF26A developer (MF26A:H2O 1:0.7 for BPRS200) for 1 min

(7) Rinse in DI water

2. Inductively coupled plasma (ICP) etching

ICP is a very widely used dry etching process which gives anisotropic etching profile and accurate control over the etch depth using a laser endpoint interferometry. It is used in multiple steps in the fabrication of VHEMT and VJFET structures. The processing steps are summarized below.

(1) Load the sample and target the laser onto the region to be etched

(2) The gases flow of 15 and 4 standard cubic centimetre per minute (sccm) for Cl_2 and Ar, respectively. An ICP power of 450 W and RF power 150 W gives a etch rate ~120 nm/min

(3) Monitor the interference signal until the correct thickness is achieved

(4) Remove the sample and clean the photoresist using EKC-830 positive photoresist striper on a 100 ˚C hotplate. Use the ultrasonic bath if necessary. Rinse in DI water

(5) Detect the etch depth using Dektak surface profiler

3. Metal deposition

Metal contact is formed by Edwards coating system E306A thermal evaporator. Electricity is passed through a coil which generates heat to evaporate the metal. A maximum of 4 different metals can be used in one evaporation. A precision up to 0.1 nm can be achieved with a crystal monitor. The procedures are,

(1) Clean sample surface with an O_2 plasma asher for 3 min to remove residue photoresist

(2) Dip the sample in $HCl:H_20$ (1:1) solution for 1 min to remove surface oxide

(3) Immediately transfer the sample into the evaporator chamber, load the coils with the corresponding metal scheme

(3.1) n-type ohmic: Ti/Al/Ni/Au 20/120/25/45 nm, anneal at 850 ˚C for 30 sec in N_2

(3.2) p-type ohmic: Ni/Au 20/20 nm, anneal at 500 ˚C for 5 min in mixed N_2/O_2

(3.3) Schottky: Ni/Au 20/200 nm, no annealing required

(4) Pump the chamber to 2-4$\times 10^{-6}$ Torr and evaporate the metal

(5) Soak the sample in acetone for 1-2 hours and lift-off the metal with a jet of acetone or using ultrasonic bath

(6) Anneal the sample using rapid thermal annealing

4. KOH etching

The KOH etching is a wet etching technique used for VHEMT and VMOSFET fabrication in this study. The alignment of the opening is the key to achieving the correct sidewall. SiN_x is

used as a hard mask in this study since photoresist can be dissolved in KOH. SiO_2 can also be used as hard mask, but the removal of SiO_2 in RIE/ICP is more difficult compared to SiN_x.

(1) Clean the sample using 3-step cleaning and dip in HCl for 10 min to remove surface oxide. This step is important, otherwise, a poor interface quality can lead to an undercut between SiN_x and GaN

(2) Deposit 150 nm SiN_x using PECVD

(3) Pattern the sample using photolithography or EBL with the sidewall in the [1-100] direction (perpendicular to the surface striations) to obtain c-plane

(4) Etch the sample in RIE/ICP with O_2/CHF_3 5/35 sccm, 150 W for 4 min 30 sec to open up the etch window. Remove residue photoresist using EKC-830

(5) Dip in 4 M KOH solution (2.7 g KOH in 12.5 mL DI water) at 90 ˚C (measured by a thermocouple) for 20 min. Rinse in DI water

(6) Remove the SiN_x mask by a buffered HF etching for 5 min.