

**MODULAR MULTILEVEL CASCADED FLYING CAPACITOR  
STATCOM FOR BALANCED AND UNBALANCED LOAD  
COMPENSATION**

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The candidate confirms that the work submitted is his/her own, except where work which has formed part of jointly-authored publications has been included. The contribution of the candidate and the other authors to this work has been explicitly indicated below. The candidate confirms that appropriate credit has been given within the thesis where reference has been made to the work of others. Most materials contained in the chapters of this thesis have been previously published in research articles written by the author of this research (Oghenewogaga Oghorada).

The research has been supervised and guided by Dr. Li Zhang, who appears as co-author on these articles. All the materials included in this document is the author's entire intellectual ownership.

A.) Details of the publications which have been used are given below;

In chapter 3:

Oghorada, OJK, Zhang, L and CJ Nwobu "Performance Evaluation of Pulse Width Modulation Techniques for Losses Reduction in Modular Multilevel Flying Capacitor Converter". Published in 2016 Proceedings of the IET 2016 – 8<sup>th</sup> International Conference on Power Electronics, Machines and Drives (PEMD 2016), IET, **DOI:** 10.1049/cp.2016.0376.

In chapter 5:

Nwobu, CJ, OJK Oghorada, Zhang, L and I. B. Efika "A modular multilevel flying capacitor converter-based STATCOM for reactive power control in distribution systems". Published in 2015 Proceedings of the EPE 2015 – 17<sup>th</sup> European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe), **DOI:** 10.1109/EPE.2015.7309085.

In Chapter 6:

Oghorada, OJK and Zhang, L "Control of a Modular Multi-level Converter STATCOM for Low Voltage Ride-Through Condition". Published in 2016 Proceedings of the IECON 2016 - 42<sup>nd</sup> Annual Conference of the IEEE Industrial Electronics Society, IEEE, **DOI:** 10.1109/IECON.2016.7794143.

Oghorada, OJK, and Zhang, L "Control of a Single-Star Flying Capacitor Converter Modular Multi-level Cascaded Converter (SSFCC-MMCC) STATCOM for Unbalanced Load Compensation". Published in 2016 Proceedings of the IET 2016 – 8<sup>th</sup> International Conference on Power Electronics, Machines and Drives (PEMD 2016), IET, **DOI:** 10.1049/cp.2016.0375.

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Oghorada, OJK and Zhang, L “*Analysis of Star and Delta Connected Modular Multilevel Cascaded Converter-Based STATCOM for Load Unbalanced Compensation*”, Published in International Journal of Electrical Power and Energy Systems, Elsevier, DOI: <https://doi.org/10.1016/j.ijepes.2017.08.034>.

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B.) Details of the research contained within these publication which are directly attributed to Oghenewogaga Oghorada with the exception detailed in C,

The published research is entirely attributed to Oghenewogaga Oghorada: the introduction section, the novel ideals in the papers, the pulse width modulation FC-MMCC analysis, overlapping hexagon space vector modulation using three and two-level hexagon, derivations and implementation of various zero sequence components under unbalance load and low voltage ride through and all the editing process of the manuscripts.

C.) Details of the contributions of other authors to the research.

Dr. Li Zhang is the co-author for all the publications listed above. These have all been written under her supervision, benefiting from excellent technical advice, guidance and valuable feedback.

C.J Nwobu performed proofreading and carried out voltage regulation for FC-MMCC based STATCOM.

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## **Abstract**

Voltage and current unbalance are major problems in distribution networks, particularly with the integration of distributed generation systems. One way of mitigating these issues is by injecting negative sequence current into the distribution network using a Static Synchronous Compensator (STATCOM) which normally also regulates the voltage and power factor. The benefits of modularity and scalability offered by Modular Multilevel Cascaded Converters (MMCC) make them suitable for STATCOM application.

A number of different types of MMCC may be used, classified according to the sub-module circuit topology used. Their performance features and operational ranges for unbalanced load compensation are evaluated and quantified in this research.

This thesis investigates the use of both single star and single delta configured five-level Flying Capacitor (FC) converter MMCC based STATCOMs for unbalanced load compensation. A detailed study is carried out to compare this type of sub-module with several other types namely: half bridge, 3-L H-bridge and 3-L FC half bridge, and reveals the one best suited to STATCOM operation. With the choice of 5-L FC H-bridge as the sub-module for STATCOM operation, a detailed investigation is also performed to decide which pulse width modulation technique is the best. This was based on the assessment of total harmonic distortion, power loss, sub-module switch utilization and natural balancing of inner flying capacitors. Two new modulation techniques of swapped-carrier PWM (SC-PWM) along with phase disposed and phase shifted PWM (PS-PWM) are analyzed under these four performance metrics.

A novel contribution of this research is the development of a new space vector modulation technique using an overlapping hexagon technique. This space vector strategy offers benefits of eliminating control complexity and improving waveform quality, unlike the case of multilevel space vector technique. The simulation and experimental results show that this method provides superior performance and is applicable for other MMCC sub-modules.

Another contribution is the analysis and quantification of operating ranges of both single star and delta MMCCs in rating the cluster dc-link voltage (star) and current (delta) for unbalanced load compensation. A novel method of extending the operating capabilities of both configurations uses a third harmonic injection method. An experimental investigation validates the operating range extension compared to the pure sinusoidal zero sequence

voltage and current injection. Also, the superiority of the single delta configured MMCC for unbalanced loading compensation is validated.

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## List of Abbreviations

AC	Alternating Current
DC	Direct Current
PCC	Point of Common Coupling
TCSC	Thyristor Controlled Series Capacitor
SVC	Static VAR Compensator
SSSC	Static Synchronous Series Compensator
STATCOM	Static Synchronous Compensator
UPFC	Unified Power Flow Controller
PLL	Phase Locked Loop
DDSRF	Decoupled Double Synchronisation Reference Frame PLL
CDSC-PLL	Cascaded Delay Signal Cancellation PLL
EO-PLL	Energy Operator PLL
SRF-PLL	Synchronisation Reference Frame PLL
NPC	Neutral Point Clamped Converter
FC, FCC	Flying Capacitor Converter
MMCC	Modular Multilevel Cascaded Converter
FC-MMCC	Flying Capacitor Modular Multilevel Cascaded Converter
PS-PWM	Phase-Shifting Pulse-Width Modulation
PD-PWM	Phase Deposition Pulse Width Modulation
SC-PWM	Swapped Carrier Pulse Width Modulation
FACTS	Flexible AC Transmission Systems
HVDC	High Voltage DC Transmission
SSBC	Single Star Bridge Cells
SDBC	Single Delta Bridge Cells
DGS	Distributed Generated System
3L	Three-level
5L	Five-level

## Symbols

$v_o, i_o$	Zero sequence voltage and current
$\varphi_o$	Zero sequence phase angle
$I_p, I_n$	positive and negative sequence currents
$\varphi_{ip}, \varphi_{in}$	positive and negative sequence current phase angles
$V_p, V_n$	positive and negative sequence voltages
$\varphi_{vp}, \varphi_{vn}$	positive and negative sequence voltage phase angles
$k_{ir}$	degree of Load unbalance, $I_n/I_p$
$I_{q\_ref}$	reference converter positive sequence active current
$V_{dc\_avg}$	average value of three phase sub-module capacitor voltages
$V_{dc\_i}$	average value of phase sub-module capacitor voltages,
$n_{mp}$	number of sub-modules per phase
$K_{p\_dc}, K_{i\_dc}$	Active Current proportional and integral controller gains
$K_{p\_c}, K_{i\_c}$	Cluster voltage balancing proportional and integral controller gains per phases
$K_{io}$	Circulating current proportional controller gain
$V_s$	Maximum Supply side voltage
$V_{dc\_sm(i)}$	Sub-module capacitor voltage where $i=a, b, c$ or $ab, bc, ca$
$i_s$	Supply side current
$v_{ci}$	Converter cluster reference voltages where $i=a, b, c$ or $ab, bc, ca$
$i_{ci}$	Converter cluster currents where $i=a, b, c$ or $ab, bc, ca$
$m_a, M_a$	<i>Amplitude</i> modulation index
$m_f$	<i>Frequency</i> modulation index
$f$	Frequency
$f_s$	Switching frequency
$T_s$	Sampling period
$s$	Second



## **Chapter 1 Introduction**

### **1.1 Background Literature**

Recent decades have seen a tremendous growth in usage of electrical power mainly resulting from industrialization and high population growth rate, especially in developing countries. This has led to more installation of conventional generating units utilizing fossil fuels and in turn increases emission of greenhouse gases especially carbon dioxide, methane, and nitrous oxide. These gases cause an increase in atmospheric temperature which results in global warming and climate change. With the urgent need of reducing these gases, clean and sustainable means of generating electricity using renewable natural sources like wind and solar are now integrated into distributed grid network as distributed generation systems (DGS). Also, the integration of these DGS into the distribution network is encouraged by the market de-regulation. These DGS provide benefits of reduced carbon emission and increase total power capacity.

However, integrating these DGS results in the power network becoming more complex and subject to disturbances. The latter is due to the fact that these DGS are subject to weather conditions, unlike conventional generating sources. With the utilization of electric vehicles and interconnection of several electric grids, there is also the need for integrating AC grids with DC grids, making the distribution network requiring bi-directional flow of power.

An important issue in a distribution network is the current imbalance and voltage unbalance. The unbalanced load connected across the phases results in current imbalance whilst unbalanced voltage is caused by fault conditions across a distribution line and connection of large single phase loads such as single phase traction drives and arc furnaces. These conditions cause undesired effects of equipment malfunction, low power factor and increased line losses. All these challenges pose a serious concern about how the aging existing electrical grid will cope with these issues.

A cost-effective solution is to establish a more efficient distribution network with communication facilities which improve the control of power flow within the distribution network (i.e. efficient management of electrical power distribution and consumption). Therefore, power electronic devices are the

electrical infrastructure required in achieving the efficient control of power flow. Presently active research has been carried out on the use of Flexible AC Transmission System (FACTS) [1-13] and High Voltage DC Systems [14-25] in power flow control.

## **1.2 Flexible AC Transmission Systems**

The growth of distributed generation systems increases the need for flexible control of power flow in distribution networks, and may introduce transient stability issues. Reactive power flow causing extra losses in distribution line conductors is a long-standing problem that worsens as existing lines are pushed to their capacity limits by increasing loading. Consequently, controllable network devices known as Flexible AC Transmission Systems (FACTS) are being increasingly installed at critical points to regulate the flow of active and reactive powers in distribution networks. These controllable network devices were initially phase-shifting transformers, fixed or mechanical switched capacitors and inductors. With the demand for higher flexibility, the first proposed devices were using series or parallel connected capacitors [26, 27] with Thyristors as the switching devices.

FACTS devices are generally classified into three groups namely;

1. First generation
  - Thyristor Controlled Series Capacitor (TCSC)
  - Static VAR Compensator (SVC)
2. Second generation
  - Static Synchronous Series Compensator (SSSC)
  - Static Compensator (STATCOM)
3. Third generation
  - Unified power flow controller (UPFC)

It is important to note that both 1<sup>st</sup> and 2<sup>nd</sup> generation devices are either shunt or series connected while the 3<sup>rd</sup> generation combines both series and shunt devices together.

### **1.2.1 Thyristor Controlled Series Capacitor (TCSC)**

This is a series connected device which regulates active power flow by varying reactance of the transmission line impedance. These thyristor controlled series reactors combine both capacitors and inductors as seen in Figure 1.1 (a).

This has been installed commercially at Kanawa River substation on a 345 kV transmission line [28], Kayentta substation on a 230 kV transmission line. Siemens and ABB still have these devices available for customers [29, 30].

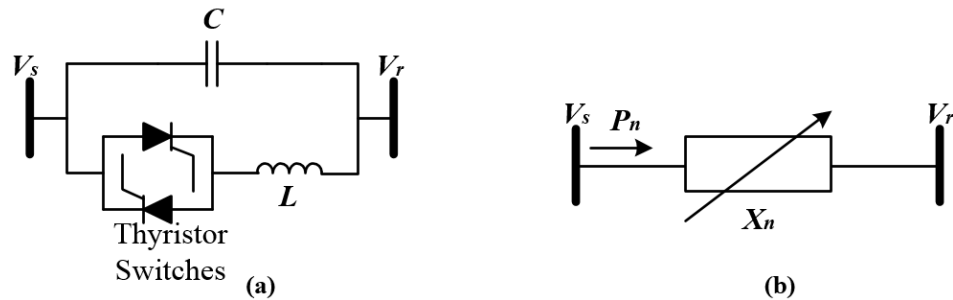


Figure 1.0.1: Thyristor controlled series capacitor: (a) Thyristor controlled reactor with fixed capacitors, (b) Variable reactance representation.

### 1.2.2 Static VAR Compensator (SVC)

This type of device is connected parallel to the grid lines. This generates or absorbs reactive power to the line either to increase or decrease line voltage. This is achieved either using thyristor controlled capacitor banks (TSCs) or reactor banks (TCRs). The circuit representation of an SVC using thyristor controlled reactors and a model representation using susceptance  $B_n$  to represent reactance  $X_n$  are shown in Figure 1.2 (a) and (b). The reactive power on the line can be controlled by varying the susceptance  $B_n$  assuming the line resistance is negligible. This is also used for reactive power compensation and oscillation damping.

The drawback of this technology is the calculation required in determining the number of capacitors and inductors switched in or out at every time instant. This was first commercially installed in 1970's for stability improvement and voltage control [31]. This device is still commercially provided by Siemens, ABB and GE Grid [32-34].

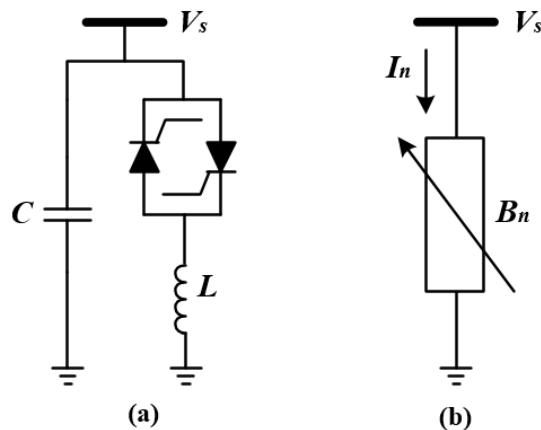


Figure 1.0.2: Static VAR Compensator: (a) TCR with fixed capacitors, (b) Variable susceptance representation [35].

### 1.2.3 Static Synchronous Series Compensator (SSSC)

Voltage Source Converters have replaced Thyristor switched devices forming the second generation FACTS devices. The SSSC uses power converter and reactive elements in controlling the impedance of a transmission line. Similar to TCSC, an SSSC is series connected to the transmission lines and regulates active and reactive powers by varying the line impedance. The equivalent model of SSSC, as shown in Figure 1.3, is a series connected VSC having variable magnitude  $V_c$  and phase angle  $\theta_c$ . Their variations adjust the active and reactive power flows through the line. The only practical applications of SSSC are a laboratory investigation highlighting its various control schemes [36-38]. Commercial applications are found as parts of UPFCs installed at Inez substation [39] and Kangjin substation [40].

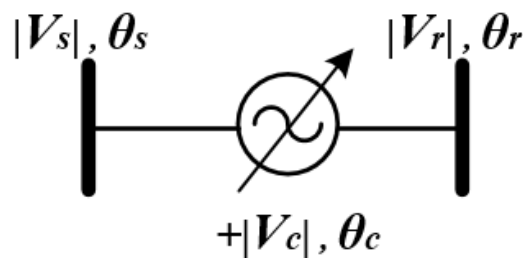


Figure 1.0.3: Static Synchronous Series Compensator equivalent circuit model

### 1.2.4 Static Synchronous Compensator (STATCOM)

The STATCOM is a shunt connected type of the SSSC. This controls the flow of reactive power to and from the line by regulating the converter voltage magnitude and angle. This is applied in voltage regulation and power factor correction. Figure 1.4 shows the equivalent circuit model of the STATCOM.

The first commercial STATCOM was installed by Kansai Electric power Co. Inc. (KEPCO) and Mitsubishi Motors, Inverters in 1980 [41] which was using force commutated thyristors and rated at 20 MVAR. Others are  $\pm 80$  MVAR STATCOM in Japan (1991) [42];  $\pm 100$  MVAR STATCOM at Sullivan substation (1996) [43]; 8 MVA STATCOM at Rejsby Hede wind farm (1997) [44]. Many more recent installations by different manufacturers are listed in [45]. Since STATCOM device is the theme of the thesis, detailed discussions will be given in section 1.4.



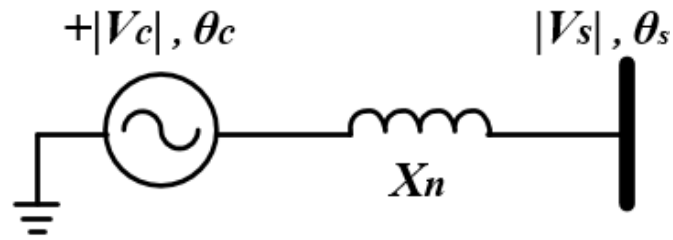


Figure 1.0.4: STATCOM equivalent power circuit model.

### 1.2.5 Unified Power Flow Controller (UPFC)

This third generation FACTS device combines both shunt and series connected devices in the second generation. The series connected controller regulates the active or reactive power flows through the lines whilst the shunt connected controller controls the reactive power flow of the line and maintains the dc bus capacitor voltage to its nominal value [46-48]. The circuit diagram of the UPFC is shown in Figure 1.5.

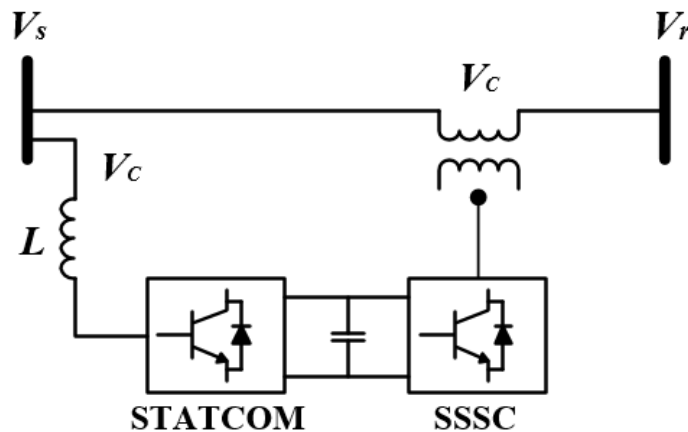


Figure 1.0.5: Unified Power Flow Controller [35].

### 1.3 Multilevel Converters

Multilevel converters offer an alternative means of realizing medium power converters for STATCOM applications. This concept dates back to the mid 1970's [49]. The multiple voltage levels from this type of converters are formed by stacking extra switches through capacitors, clamping diodes or cascading converter cells together. Considering a converter with a DC source voltage  $V_{DC}$  consisting of  $n$  stacked cells, each cell synthesizes only  $n$ th fraction of  $V_{DC}$ , which significantly reduces the voltage stress on the switches within each cell. The synthesized output voltage waveform being multiple voltage levels of the source voltage contains less harmonics and lower THD at a low switching frequency. This results in little or no filter requirements. Although with their benefits, multilevel converter still poses challenges of cost and control complexity [50]. A brief review of the well-known types of multilevel

converters namely Neutral point clamped (NPC) and the Flying Capacitor Converter (FCC) has been presented in the literature [49-58] and a brief summary is given below.

### 1.3.1 Neutral Point Converter (NPC)

This was proposed by Nabae et al in 1981 [59]. The NPC is also known as multipoint clamped converter [60]. NPC has various types and are classified based on the voltage clamping methods, these include diode clamped, switch clamped, bi-directional switch clamped [61], asymmetrical multi-point clamped [62], diode capacitor clamped and mutual diode multi-point clamped [63]. The most basic and used of NPCs is the five-level H-bridge diode clamped configuration which synthesizes an output voltage having five distinctive voltage levels:  $0$ ;  $+V_{DC}/2$ ;  $-V_{DC}/2$ ;  $+V_{DC}$ ; and  $-V_{DC}$ . A five-level NPC converter is shown in Figure 1.6.

Each leg of the converter consists of two complementary power switches ( $S_{a1}:S_{a3}$ ,  $S_{a2}:S_{a4}$ ,  $S_{b1}:S_{b3}$ ,  $S_{b2}:S_{b4}$ ) which are clamped with diodes ( $D_{a1}-D_{a2}$ ,  $D_{b1}-D_{b2}$ ). These diodes prevent voltage in one level from interfering with other levels. It is important to note that switches  $S_1$  and  $S_4$  cannot be switched on simultaneously to avoid over voltage. The capacitors  $C_1$  and  $C_2$  provide the converter neutral point, hence the voltage across both capacitor must be kept balanced to prevent distorted levels appearing in the converter output voltage. Three operating states (1100, 0110, and 0011) and nine switch states exist for this NPC.

Extending this converter for higher voltage levels, higher and uneven power loss distribution appear across power devices especially clamping diodes. Also, the DC link capacitor voltage balancing becomes difficult to meet [64-66].

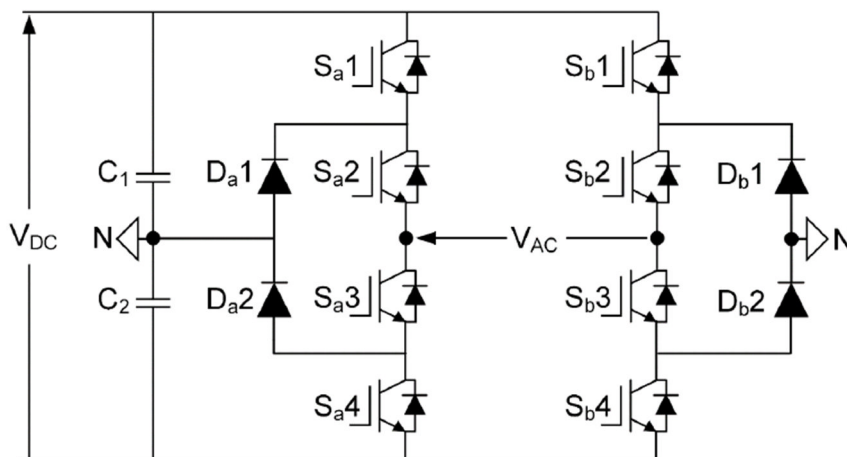


Figure 1.0.6: 5-level H-bridge Neutral Point Clamped Converter [35].

### 1.3.2 Flying Capacitor Converter

Meynard and Foch in 1992 proposed the Flying Capacitor (FC) multilevel Converter [54]. This is also known as the capacitor clamped or floating Capacitor Converter. This topology is comparable to NPC with the exception of clamping diodes replaced by capacitors. The application of the floating capacitor converter is well known [51, 52]. This topology is less applicable in industrial application because;

- Higher switching frequencies greater than 1 kHz is required for its capacitor voltages to be maintained at their rated value.
- The circuit is bulky and more expensive due to the high number of capacitors required.

However, this converter offers more redundant switch states compared to NPC. This aids switching stress to be shared among the devices.

Figure 1.7 shows a full bridge 5-level FC converter. This synthesizes five distinct voltage levels of  $0$ ;  $+V_{DC}/2$ ;  $-V_{DC}/2$ ;  $+V_{DC}$ ; and  $-V_{DC}$ . The flying capacitors ( $C_a$  and  $C_b$ ) are rated  $V_{DC}/2$ . Each leg of the converter has two complementary switching pair  $S_1:S_4$ ,  $S_2:S_3$ . There are four operating states (1100, 1010, 0101, and 0011) with 16 switch states in total for this converter.

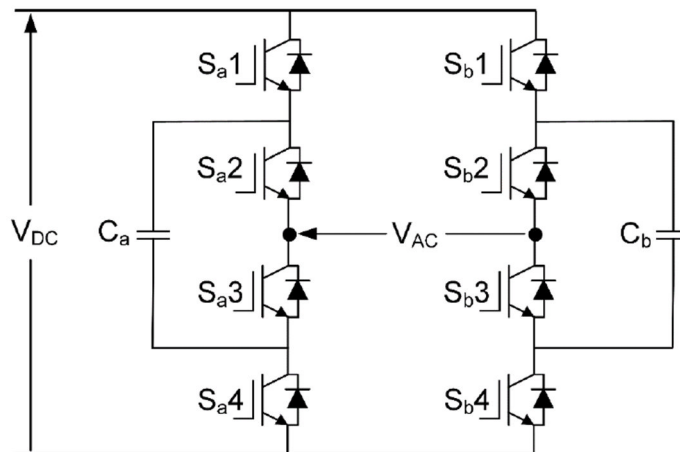


Figure 1.0.7: 5-level full bridge Flying Capacitor Converter[35].

### 1.3.3 Modular Multilevel Cascaded Converters

One challenge of the multilevel converter topology is the complex control technique required when the converter is configured for higher voltage levels and this, in turn, makes it bulky. Also, failure of a particular part either switch or clamping device could lead to total shut-down of its operation. Whereby in practice, this down time is costly to power system providers.

With a modular concept, converters can easily be extended to any required voltage levels, where the converter total output voltage is the summation of all sub-module output voltages. Also, a faulty sub-module can be removed and replaced without affecting the operation of other sub-modules.

The concept of the modular multilevel converter was introduced in the 1960's through the cascaded H-bridge topology [67]. This was first practically implemented by Robicon Corporation in the 1990's for drive application [68]. This implementation involved a cascade of three H-bridges per phase, a complex phase shifting transformer setup to supply the DC power requirements of each isolated H-bridge. The cost of the phase shifting transformer made it less attractive for high power applications. Nevertheless, the benefit of its modular nature inspired researchers to further explore this cascaded converter topology.

In 2002, Lenisacar and Marquart proposed the concept of the modular multilevel converter [69, 70] which improved the functionality of the multilevel converter for high power applications. This was based on half bridge converter serially connected to build up to higher voltages. Two major benefits of this topology are naturally its modularity and scalability. The converter can easily scale up its voltage/power rating to meet the application need without a step-up transformer. This attribute of scalability makes the output voltage waveform having reduced harmonics and hence lower filtering requirements. This topology provides fault tolerant capability as it can bypass a faulty module and reprogrammed to generate a reduced voltage. The switching and clamping devices used for this topology are rated at module level enabling the use of reduced voltage stressed devices. Thus, this enhances ease of manufacturing, maintenance, cost, reliability, and efficiency of this topology. This topology over the years has been applied for reactive power compensation [71-73].

#### **1.4 MMCC-Based Static Synchronous Compensator (STATCOM)**

Voltage source converter based Static Compensator (STATCOM) provides a smaller footprint, faster dynamics in reactive power response than the Static Var Compensator using thyristor switch control. In 1996 Lia and Peng [74], applied the cascaded H-bridge converter as a static Synchronous Compensator (STATCOM) for reactive power control. This implementation eliminated the need for complex phase shifting transformer recommended by Robicon Corporation thus leading to the idea of modular converters for

STATCOM. The Modular multilevel cascaded converters, in star connection, has been applied for voltage regulation and power factor correction in balanced grid systems [75-77]. This topology provides benefits of modularity, good waveform performance, efficiency, and with the number of sub-modules being proportional according to the point of connection ac voltage level, it can be scaled-up to any desired voltage levels without using step-up transformers [78, 79]. Likewise, MMCC converters in delta connection has been used as STATCOM in regulating negative sequence reactive power [80].

In this sub-section, the principles of using STATCOM for voltage regulation and power factor correction are reviewed using phasor analysis. This is followed by describing briefly two grid synchronization schemes and current control method commonly applied for STATCOM for either balanced or unbalance operations. This is necessary since these schemes are used in the control of the MMCC-STATCOM. Finally a review on the current applications of MMCC-based STATCOM, the problems and technical challenges are highlighted.

#### 1.4.1 Principles of Voltage and Power Factor Control by STATCOM

This analysis is performed on a simplified power network with its one line diagram shown in Figure 1.8. This represents a balanced three phase system made up of a voltage source  $V_s$ , line impedance  $Z_s=R_s+jX_s$  and an inductive load with impedance  $Z_L=R_L+jX_L$  and total power  $P_L+jQ_L$ . A STATCOM functioning as the voltage compensator,  $V_c$ , with variable voltage is connected to the PCC of the system via its filter with impedance  $Z_c=R_c+jX_c$  and supplies the reactive power  $Q_C$  required by the system.

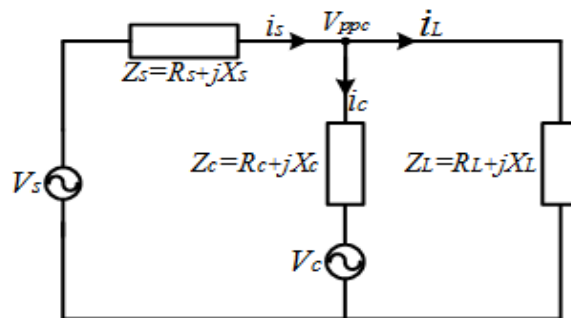


Figure 1.0.8: Single phase circuit representation.

Without STATCOM, the current at the source and load sides should be equal ( $i_s = i_L$ ), and the voltage difference between the supply and PCC is  $\Delta V = V_s - V_{PCC}$ . Assuming supplying an inductive load and taking PCC voltage as the reference, ( $V_{PCC} = V \angle 0^\circ$ ) the current supplied is expressed as:

$$\vec{i}_s = \frac{P_s - jQ_s}{V_{PCC}} \quad (1.1)$$

The voltage drop due to the line impedance is given as:

$$\Delta V = \Delta V_{Real} + j\Delta V_{imag} = \frac{P_s R_s + Q_s X_s}{V_{PCC}} + j \frac{P_s X_s - Q_s R_s}{V_{PCC}} \quad (1.2)$$

This shows that the voltage drop between  $V_s$  and  $V_{PCC}$  is mainly due to the power requirements of the load and line impedance. The phasor diagram expressing the relationship between  $V_s$ ,  $V_{PCC}$  and current phasors are given in Figure 1.9.

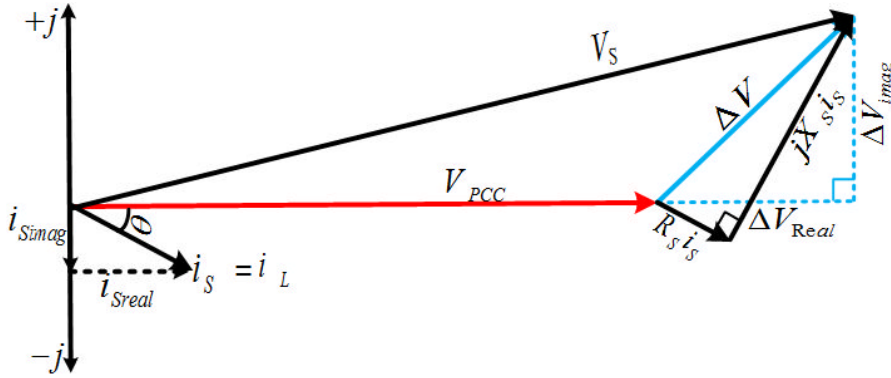


Figure 1.0.9: Phasor diagram between supply and PCC voltages.

#### 1.4.1.1 Voltage Regulation

According to the above analysis, to achieve  $|V_{PCC}|=|V_s|$ , the STATCOM is required to supply the correct amount of reactive power. The condition of achieving this is analysed below. The supply voltage magnitude can be expressed in terms of the voltage drop  $\Delta V$  and  $V_{PCC}$  as:

$$V_s = \Delta V + V_{PCC} = \left( V_{PCC} + \frac{P_s R_s + Q_s X_s}{V_{PCC}} \right) + j \frac{P_s X_s - Q_s R_s}{V_{PCC}} \quad (1.3)$$

Simplifying (1.3) gives,

$$|V_s|^2 = \left( V_{PCC} + \frac{P_s R_s + Q_s X_s}{V_{PCC}} \right)^2 + \left( \frac{P_s X_s - Q_s R_s}{V_{PCC}} \right)^2 \quad (1.4)$$

The above expression can be simplified using the supply current equal to the load current as:

$$i_{sreal} + j i_{simag} = \frac{P_s}{V_{PCC}} - j \frac{Q_s}{V_{PCC}} \quad (1.5)$$

Equation (1.6) is simplified as:

$$|V_s|^2 = (V_{PCC} + R_s i_{Sreal} - X_s i_{Simag})^2 + (X_s i_{Sreal} - R_s i_{Simag})^2. \quad (1.6)$$

Assuming  $R_s$  is negligible and the phase angle between  $V_{PCC}$  and current is  $\theta$  (figure 1.9), Equation (1.6) is simplified as:

$$\begin{aligned} |V_s|^2 &= (V_{PCC} + (X_s i_s \sin \theta))^2 + (X_s i_s \cos \theta)^2 \\ &= V_{PCC}^2 + 2V_{PCC} X_s i_s \sin \theta + |X_s i_s|^2 \end{aligned} \quad (1.7)$$

Therefore to achieve  $|V_s|=|V_{PCC}|$ , we set  $|2V_{PCC} X_s i_s \sin \theta| + |X_s i_s|^2 = 0$ , the  $\theta$  becomes:

$$\theta = -\sin^{-1}\left(\frac{X_s i_s}{2V_{PCC}}\right). \quad (1.8)$$

The expression in (1.7) shows that for  $|V_s|=|V_{PCC}|$ , the current injected by the STATCOM when added to the original load current will make the current flowing through  $Z_s$  to lead  $V_{PCC}$  by  $\theta$  as seen in Figure 1.10.

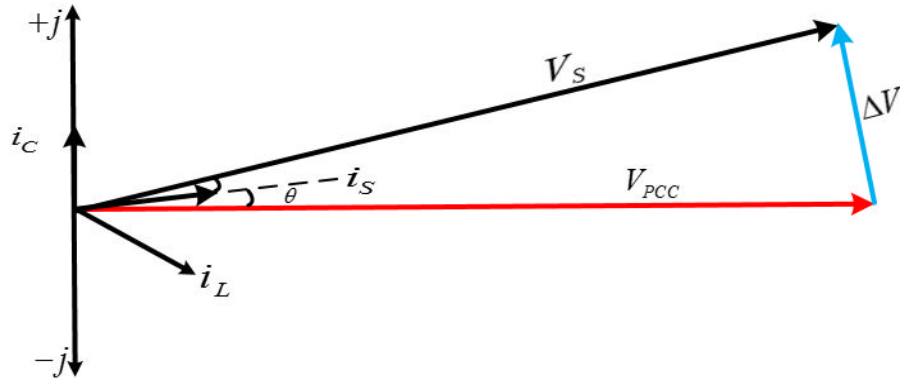


Figure 1.0.10: Phasor diagram illustrating  $|V_s|=|V_{PCC}|$ .

#### 1.4.1.2 Power Factor Correction

To achieve maximum active power transfer in a power distribution system, the load reactive power  $Q_L$  is compensated by the compensator  $Q_C$  such that the supply end reactive power becomes zero, i.e.:

$$Q_s = Q_L + Q_C = 0, \text{ where } Q_C = -Q_L. \quad (1.9)$$

Therefore, the voltage drop across the line impedance becomes:

$$\Delta V = (R_s + jX_s) \frac{P_s - j0}{V_{PCC}} = \frac{P_s R_s}{V_{PCC}} + j \frac{P_s X_s}{V_{PCC}}. \quad (1.10)$$

The above expression shows that the voltage drop across distribution line is solely due to  $P_s$ . This further implies that both unity power factor correction and voltage regulation cannot be achieved at the same time. The phasor relationship between  $V_s$  and  $V_{PCC}$  is shown in Figure 1.11.

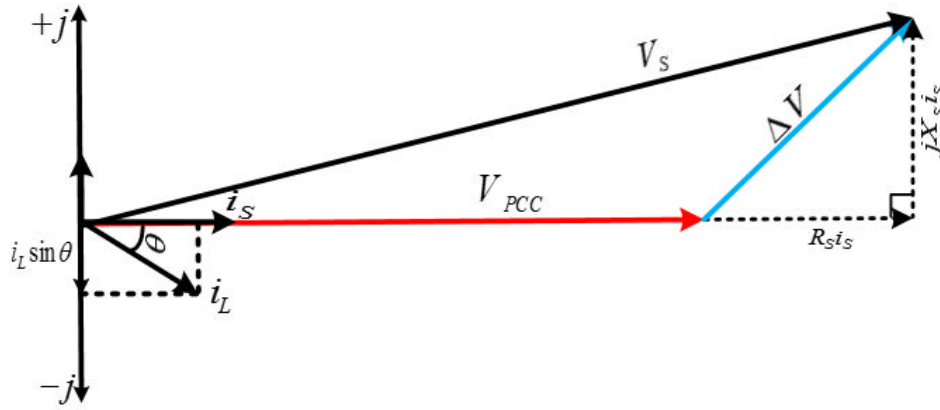


Figure 1.0.11: Phasor diagram showing unity power factor correction.

### 1.4.2 Grid Voltage Synchronization Techniques

For effective control of active and reactive power flow in distribution systems through power electronic converters connected to the grid, the reference signal generated by these converters must be in unison with the fundamental component of the grid voltage (i.e. its voltage magnitude and phase angle). This should be achieved regardless of the conditions of grid voltages being unbalance and containing harmonics. A good synchronization technique is determined by the following criteria;

- Ability to stay synchronized under unbalance voltage conditions like voltage sags and swells.
- Ability to accurately and quickly respond to transient changes.
- Ability to track frequency and phase variations when they deviate from their real values.

Various grid voltage synchronization schemes have been discussed extensively in the literature, and these can be grouped either as open loop or closed loop schemes. Open loop synchronization schemes estimate the grid voltage frequency and phase angle directly by instantaneously sampling the grid voltage as shown in Figure 1.12. The major limitation of the open loop method is its sensitivity to noise, and this can only be addressed by filtering out distorted signals. Example of open loop schemes include Low pass filter [81, 82], space vector filter [83], Kalman filter [84-87], weighted least square estimation [88], energy operator [89] and discrete Fourier transform [90-92]. The closed loop schemes operate by aligning the phase angle of its internal oscillator with that of the fundamental grid voltage component.



The loop consists of three parts namely; a phase detector, loop filter, and voltage controlled oscillator as seen in Figure 1.13. The phase detector generates the difference between the actual voltage signal and the one synthesized by the internal oscillator. The high-frequency AC signals are attenuated by the loop filter. This is either implemented using a low pass filter or PI regulator. Examples include SRF-PLL, DDSRF-PLL and CDSC-PLL. For the purpose of this study, the SRF-PLL and DDSRF-PLL are discussed below since they are used in the STATCOM control in Chapter 5 and 6.

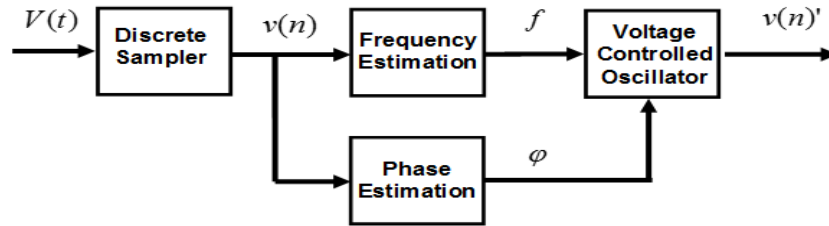


Figure 1.0.12: Open loop synchronization technique block diagram [35].

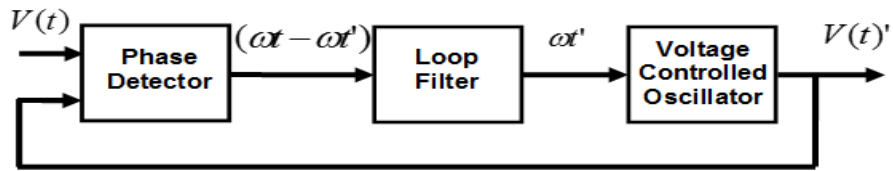


Figure 1.0.13: Closed loop synchronization technique block diagram.

#### 1.4.2.1 Synchronous Reference Frame- Phase Lock Loop (SRF-PLL)

This technique is applicable for balanced grid voltages. The phase detector comprises of both Clarke's and Park's transformation matrices, which transforms three phase voltages into  $dq$  rotating reference frame components based on Equation (1.11).

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos \theta & \cos(\theta - 2\pi/3) & \cos(\theta + 2\pi/3) \\ \sin \theta & \sin(\theta - 2\pi/3) & \sin(\theta + 2\pi/3) \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix}. \quad (1.11)$$

Figure 1.14 shows the SRF-PLL structure. The loop filter and the voltage controlled oscillator forms a closed loop feedback control that forces the  $d$ -component to be zero through eliminating the phase angle error. Under balanced grid voltage conditions, the bandwidth is set to a high value, thus resulting in a fast and precise response in detecting the phase angle.

For the condition when three-phase voltages are unbalanced, the presence of the negative sequence component introduces second order harmonic component on the *dq*-components. By reducing the bandwidth of the loop filter, the effect of the second order harmonic component is reduced but comes with a consequence of increased delay. From the closed loop transfer function, the bandwidth of the loop filter can be determined. The transfer function of the PLL [93] is:

$$G(s) = \frac{sK_p + K_i}{s^2 + sK_p + K_i} = \frac{s2\zeta\omega_n + \omega_n^2}{s^2 + s2\zeta\omega_n + \omega_n^2} \quad (1.12)$$

where  $K_p = 2\zeta\omega_n$ ,  $K_i = \omega_n^2$  and  $K_p$  is the proportional gain,  $K_i$  is the integral gain,  $\zeta$  is the damping ratio and  $\omega_n$  is the undamped natural frequency.

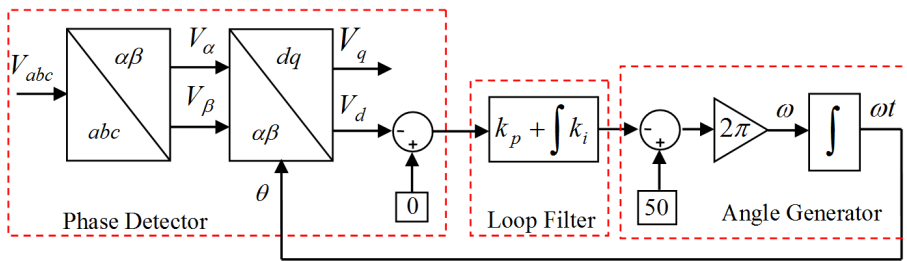


Figure 1.0.14: Synchronous Reference Frame (SRF-PLL).

With the limitation pose by the PLL bandwidth in extracting positive sequence component from the unbalanced grid three phase voltages with asymmetrical fault, filters can be used.

This filter is usually placed before the loop filter as seen in Figure 1.15. The better the choice of this filter, the more accurate the phase angle identified by the PLL. The filters used include low pass filter (LPF) [94], moving average filter (MAF) [95-97], resonant filters [98] and notch filters [94]. All these introduce additional delays, resulting in slower response speed. A better synchronization method of decoupling the effects of the positive and negative sequence components has been used in this research and is discussed below.

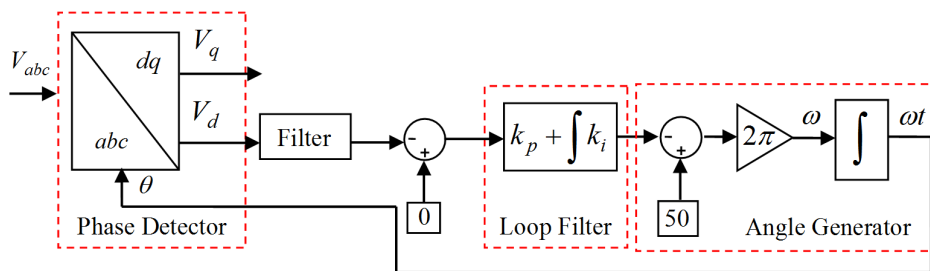


Figure 1.0.15: SRF-PLL + Filter.

### 1.4.2.2 Decoupled Double Synchronous Reference Frame- Phase Lock Loop (DDSRF-PLL)

This PLL technique uses two synchronous reference frames, i.e. the double synchronisation reference frame (DSRF) with  $dq^{+1}$  and  $dq^{-1}$  rotates with positive angular velocity  $\omega$  and  $dq^{-1}$  is rotating with negative velocity  $-\omega$ . The positive and negative sequence components of the unbalance voltages with a DSRF are shown in Figure 1.16.

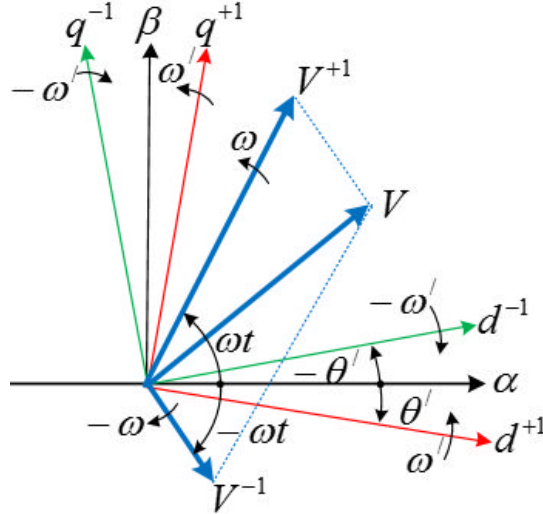


Figure 1.0.16: Double Synchronous Reference Frame structure.

The unbalance voltage vector expressed in the DSRF, yields:

$$v_{dq}^{+1} = \begin{bmatrix} v_d^{+1} \\ v_q^{+1} \end{bmatrix} = [T_{dq}^{+1}] v_{\alpha\beta} = V^{+1} \begin{bmatrix} 0 \\ 1 \end{bmatrix} + V^{-1} \begin{bmatrix} \sin(-2\omega t) \\ \cos(-2\omega t) \end{bmatrix} \quad (1.13)$$

$$v_{dq}^{-1} = \begin{bmatrix} v_d^{-1} \\ v_q^{-1} \end{bmatrix} = [T_{dq}^{-1}] v_{\alpha\beta} = V^{+1} \begin{bmatrix} \sin(2\omega t) \\ \cos(2\omega t) \end{bmatrix} + V^{-1} \begin{bmatrix} 0 \\ 1 \end{bmatrix} \quad (1.14)$$

$$\text{where } [T_{dq}^{+1}] = [T_{dq}^{-1}]^T = \begin{bmatrix} \cos \omega t & -\sin \omega t \\ \sin \omega t & \cos \omega t \end{bmatrix}.$$

Equations (1.13) and (1.14) show that the  $dq^{+1}$  and  $dq^{-1}$  terms comprise DC terms and oscillatory terms at  $2\omega$  which both correspond to the magnitude of positive, negative sequence voltage signals and coupling between both sequences which results from both voltage vectors rotating in opposite direction.

The oscillatory terms can be cancelled out using a decoupling network as analysed in **Appendix A.1**.

As shown in Figure 1.17, the DDSRF-PLL is an extension of the SRF-PLL. The only difference is the presence of the decoupling network used in cancelling out the  $2\omega$  oscillatory terms shown in equations (1.13)-(1.14). Therefore the need of reducing the PLL bandwidth is totally avoided.

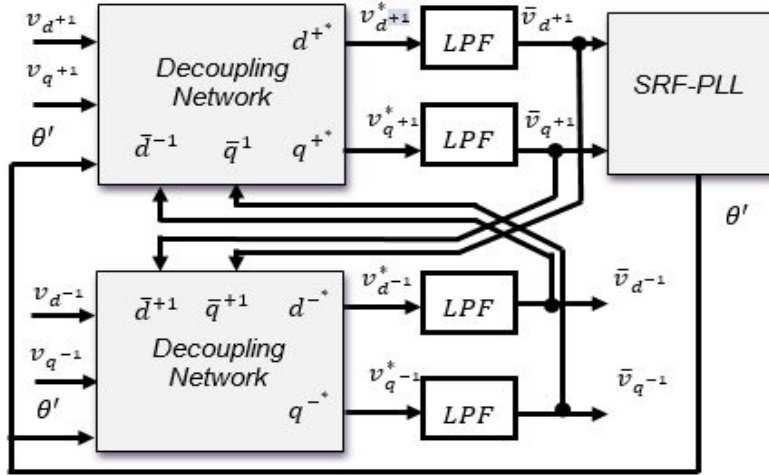


Figure 1.0.17: Block diagram of the DDSRF-PLL.

### 1.4.3 STATCOM Current Control Method

Once the grid voltage fundamental frequency is properly identified through PLL, another important aspect is the effective current controller capable of injecting required currents into the grid. The current injected into the grid by the STATCOM must maintain a relationship with the voltage at the point of coupling to deliver the desired reactive power. Various current control methods have been extensively discussed in the literature [99-104]. Two current control methods using either SFR or DDSRF are PI and deadbeat controllers which can be applied STATCOM operating under either balanced or unbalanced conditions.

#### 1.4.3.1 Synchronous Reference Frame Current Controller

This is the most widely applied solution for the control of current injection for STATCOM applications. These controllers are either implemented using PI controllers or predictive deadbeat control when operated in the  $dq$  frame when balanced currents are injected into the grid. This controller achieves a good performance. However, under unbalance conditions, the behaviour of this controller is inadequate, since there is no control loop for negative sequence component control. Figure 1.18 shows the structure of this controller.

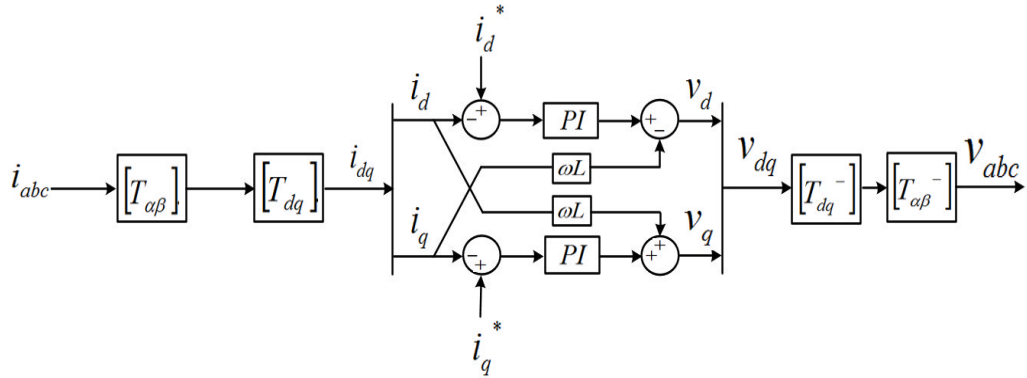


Figure 1.0.18: Synchronous reference frame current controller.

### 1.4.3.2 Decoupled Double Synchronous Reference Frame Current Controller

To effectively control a current vector having both positive and negative sequence components, two synchronous reference frames both rotating in the positive and negative direction at the fundamental grid frequency current controller is applied along with a decoupling network in attenuating the oscillatory signal at twice the fundamental frequency in the  $dq$  signals obtained through park transform. The DDSRF discussed in the synchronization section is similar except with the inclusion of the PI or deadbeat regulators used in controlling the injected currents. Figure 1.19 shows the structure of the DDSRF current controller. In this Figure, note that the decoupling term ( $\omega L$ ) on both positive and negative sequence have their signs inverted because of their opposite directions of rotation.

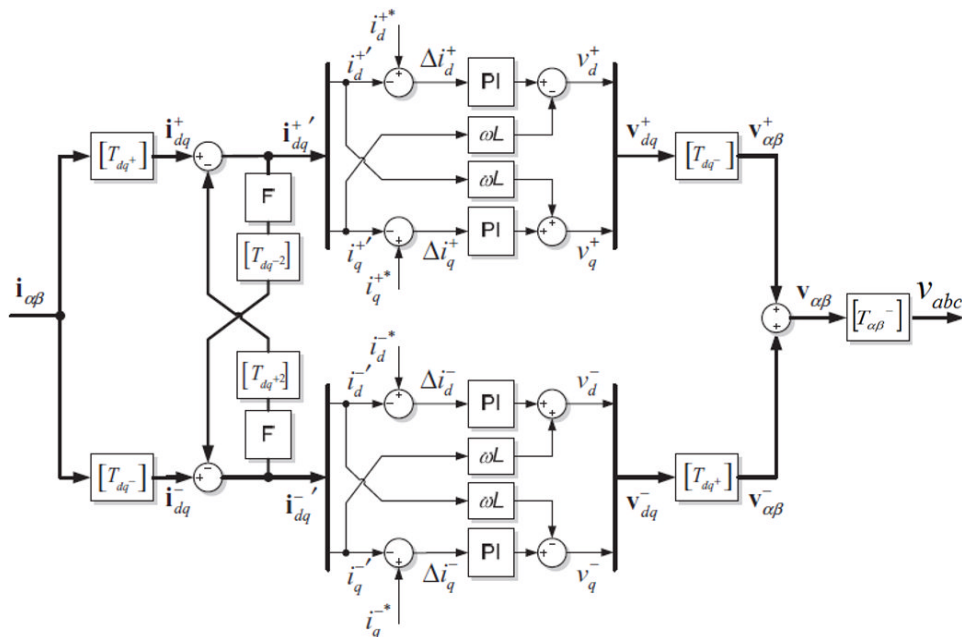


Figure 1.0.19: Decouple double synchronous reference frame current controller [105].

#### 1.4.4 MMCC STATCOM Applications and Challenges

Alstom in 2001 [106] installed its first commercial MMCC based STATCOM with 175 MVAR capacity. Other commercial installations include a three-voltage level  $\pm 100$  MVAR STATCOM (2002) [107] and six MMCC STATCOM stations known as the SVC light by ABB in Sweden, Germany, France, Finland and USA [108, 109]. All these have been installed to operate under balanced grid conditions.

However, the control of this topology introduced challenges of inter and intra-cluster balancing control of sub-module capacitors which at the moment is a subject of active research [110-113].

The main limitation of an MMCC based STATCOM is the lack of a common dc link which results in the difficulty of exchanging energy between phase limb sub-modules. One of the methods applied is by selecting appropriate redundant switching vectors [114]. This provides fast control of all sub-module voltages but it is limited in flexibility as the number of switching vector increases with the number of voltage levels. This situation of capacitor voltage balancing is more difficult when the grid is unbalanced (i.e. voltage unbalance or load current unbalance) especially with the growth of distributed power generation systems. Consequently, the sub-module voltages drift away from their rated levels, thus resulting in STATCOM malfunction leading to distorted current injected into the grid, and overstressing or even damaging the switching devices.

To overcome this problem the approach used for SSBC-MMCC is to inject a sinusoidal zero sequence voltage in the converter neutral point [72, 115-118]. For SDBC-MMCC a zero sequence current is injected in the delta configured three phase limbs [80, 117, 119]. However, such a scheme causes serious problems; in the former case, the injected zero sequence voltage can cause the converter phase voltages to exceed their rated level, resulting in the SSBC operating in over-modulation mode or even becoming uncontrollable. In the SDBC-MMCC, it can lead to current exceeding the rated limit. Researchers have investigated the unbalanced cases in [120-122], but only for real power supply (i.e. application in PV power generation); detailed analysis is not given, the rating quantification is not analysed clearly, and the improvement method is not clearly investigated. Another recent publication [123] highlighted the compensation limitations for star connection under unbalanced current compensation, and delta connection under unbalanced voltage compensation, i.e. the singularity issue, without analysing the delta case for a load unbalance condition. However, there is no research giving a clear

quantitative relation between the level of load current unbalance and the phase limb voltage rating in a star connection, nor to the phase current rating in delta connection. Furthermore, it is necessary to explore new methods to effectively mitigate such limitations, and hence extend the MMCC-STATCOM's operating ranges under unbalanced load compensation which is the major interest of this research work.

### **1.5 Aims, Objectives and Thesis Structure**

The aim of this research is to investigate the use of a Flying Capacitor Modular Multilevel Cascaded Converter as a STATCOM (FC-MMCC) for reactive power and unbalanced load current compensation in a distribution system. The objectives in achieving this research aim are:

- Investigating and assessing different MMCC configurations and sub-module types that best suits STATCOM applications in terms of footprint, cost, control complexity and redundancy.
- Investigating multi-level pulse width modulation schemes that best suits the control of an MMCC using five-level H-bridge flying capacitor converters as sub-modules, under metrics of power loss, THD, natural balancing capability of flying capacitors and sub-module switch utilization.
- Developing novel space vector modulation schemes using overlapping hexagon techniques that offer better THD and reduced complexity for MMCC's using any sub-module types.
- Analyse, simulate and experimentally validate the operational characteristics of FC-MMCC based STATCOM for reactive power compensation.
- Analyse, simulate and experimentally validate the use of third order harmonic zero sequence components in extending the operating capability of single star and delta FC-MMCC based STATCOMs for reactive power and negative sequence current compensation under unbalance load compensation.

The structure of the thesis is as follows;

Chapter 2 presents a detailed analysis and comparison of the various MMCC configurations using different sub-module types for STATCOM applications. The benchmark for this assessment is based on footprint, cost, redundancies and control complexity. This comprehensively compares the various MMCC configurations and explains the choice of the five-level H-bridge flying capacitor converter as the sub-module for this research.

Chapter 3 discusses the use of carrier modulation control schemes for FC-MMCC. These pulse width modulation techniques include phase disposed PWM (PD-PWM), swapped carrier PWM (SC-PWM) and phase shifted PWM (PS-PWM). The performance of each modulation technique is evaluated in terms of natural capacitor voltage balancing, converter power losses, waveform harmonics and switch utilization.

Chapter 4 presents a novel overlapping hexagon space vector modulation (OH-SVM) technique for MMCC, which offers flexibility and simplicity of control compared to multilevel space vector modulation techniques. It discusses the principle of this new method and compares it with conventional multilevel SVM.

Chapter 5 presents simulation and experimental validation of the FC-MMCC as a STATCOM for power factor correction in power distribution systems. The sub-module dc-capacitor voltage rating, the voltage ripple, and converter filter requirements are discussed. The experimental system is described and the simulation and experimental results of the FC-MMCC STATCOM for power factor correction are analysed.

Chapter 6 explores the FC-MMCC STATCOM for compensating load reactive power and unbalanced load current in a power distribution system. Two non-sinusoidal zero sequence components are applied for the inter-cluster balancing control of both star and delta configurations. The MMCC compensation operating range and required ratings are quantified and compared with those for sinusoidal injection. Experimental validation is included.

A summary of the findings made during this research is provided in chapter 7 with recommendations for future research.



## **Chapter 2**

### **ASSESSMENT of MODULAR MULTI-LEVEL CASCADED CONVERTERS IN STATCOM APPLICATIONS**

One major constituent of an MMCC is its sub-module unit. Among the various types, the 2-level half-bridge and 3-level H-bridge cells are the most widely applied. Others that have been used include the 3-level flying capacitor (FC) half-bridge, 3-level Neutral Point Clamped (NPC) half-bridge [124, 125], 5-level flying capacitor H-bridge and the hybrid cell types formed by, for example, the combination of half bridge FC and 2-level half bridge [126]. These various sub-module types, when applied in an MMCC-STATCOM, offer different cost, operating behaviour, control and footprint requirements.

This chapter presents a detailed analysis and comparison of various MMCC-configurations using four sub-module types, namely the 2-level half-bridge, 3-level FC half bridge, 3-level H-bridge and 5-level FC H-bridge for an 11kV STATCOM. The different sub-module concepts are described through a quadrant system concept, highlighting their features and degrees of freedom. Afterward, a review of the general classifications of MMCC is presented. This chapter is concluded with a comprehensive comparison of various MMCC configurations and sub-module types that best suit STATCOM operation. The benchmark for this assessment is based on footprint, cost, switching state redundancies as discussed in [35, 127] and control complexity. Note that the terms cell, sub-module, and module are used interchangeably in this thesis.

#### **2.1 Sub-module Circuits of Modular Multilevel Cascaded Converters**

Those discussed here include the 2-level Half bridge, 3-level FC Half bridge, 3-level H-bridge and 5-level FC H-bridge. A quadrant system is used to show their inverting and rectifying states.

##### **2.1.1 Half-bridge cells**

Two types, the two-level and three-level FC half-bridge sub-modules, are considered.

### 2.1.1.1 Two-level Half bridge cell

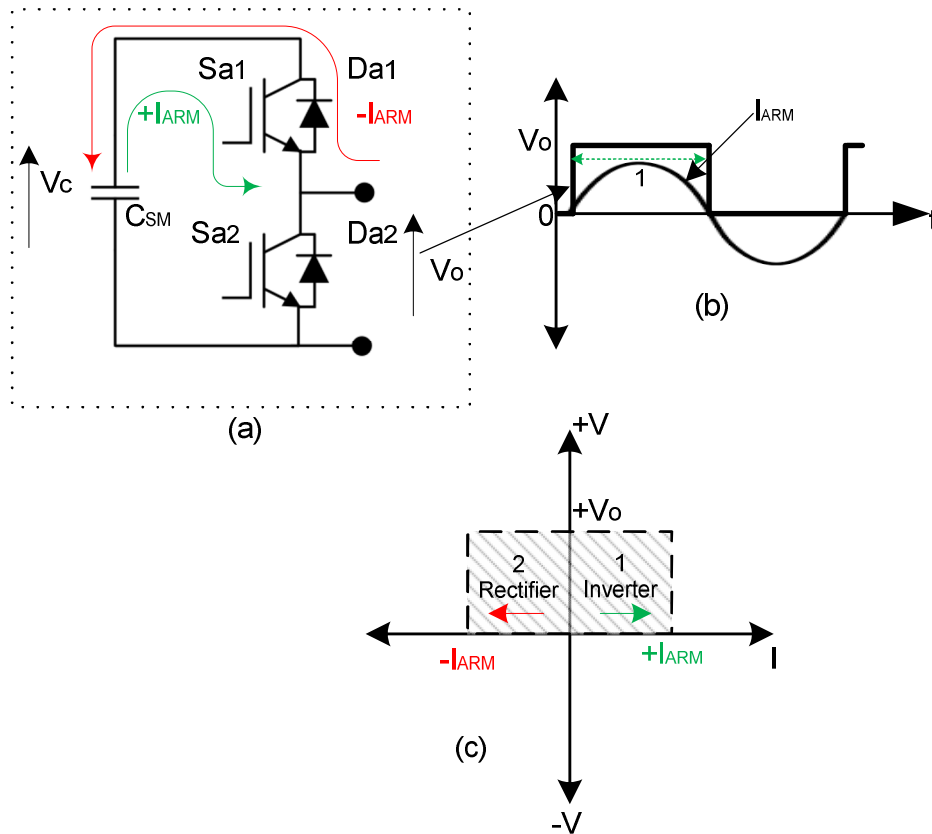


Figure 2.1: Two-level half bridge sub-module: (a) Power Circuit; (b) sub-module output voltage and current; (c) Two quadrant operation modes current.

The circuit configuration of this type is shown in Figure 2.1(a). It comprises two complementary switches ( $S_{a1}$ ,  $S_{a2}$ ), with anti-parallel diodes, ( $D_{a1}$ ,  $D_{a2}$ ) connected in parallel with a dc storage element normally a capacitor. It has only two switch states  $S_{a1}:1$ ,  $S_{a2}:0$  and  $S_{a1}:0$ ,  $S_{a2}:1$  which make it capable of synthesizing two distinct output voltage levels  $+V_o$  and 0 respectively as seen in Figure 2.1(b). A bi-directional current flows through this sub-module, allowing two quadrant operation as shown in Figure 2.1(c). The operational states of this sub-module result in its capacitor being charged or discharged are shown in Table 2.1.

Table 2.1: Two-level half bridge sub-module operating states

Quadrant State	Switch state		Diode state		$V_o$	$I_{ARM}$	Rectifier Mode	Inverter Mode
	$S_{a1}$	$S_{a2}$	$D_{a1}$	$D_{a2}$			$I_{ARM}\uparrow$	$I_{ARM}\downarrow$
1	1	0	0	0	$V_C$	+1	-	$C_{SM}\downarrow$
2	0	0	1	0		-1	$C_{SM}\uparrow$	-
-	0	1	0	0	0	-1	NC	-
-	0	0	0	1		+1	-	NC

$V_o$  – sub-module output voltage;  $I_{ARM}$  – converter arm current; and  $V_C$  - sub-module capacitor voltage states ( $\downarrow$  = Discharging,  $\uparrow$  = Charging, NC= No change).

**2.1.1.2 Flying Capacitor half-bridge cell**

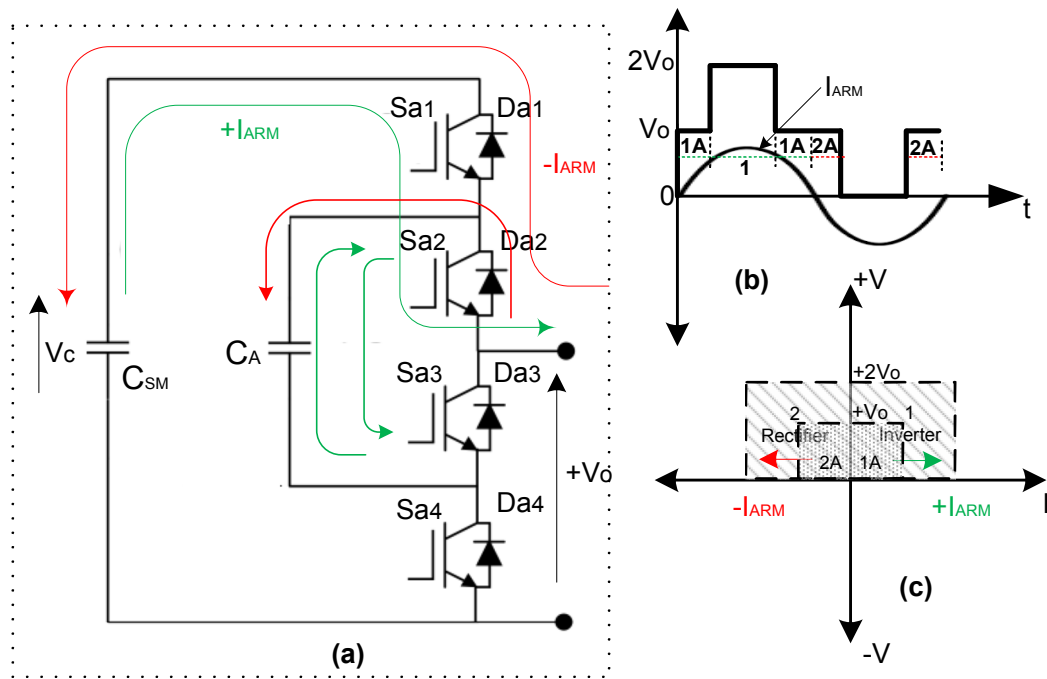


Figure 2.2: Three-level FC half bridge sub-module: (a) Power Circuit; (b) sub-module output voltage and current; (c) and  $i$ - $v$  two quadrant operation modes.

The circuit configuration for this cell is shown in Figure 2.2 (a). This comprises two complementary switching pairs ( $S_{a1}, S_{a4}$ ), ( $S_{a2}, S_{a3}$ ) with their corresponding antiparallel diodes ( $D_{a1}, D_{a4}$ ), ( $D_{a2}, D_{a3}$ ) connected in parallel across the inner flying capacitor ( $C_A$ ) and sub-module capacitor ( $C_{SM}$ ). The inner flying capacitor voltage rating is half the module capacitor voltage (i.e.  $V_A=0.5V_C$ ). This sub-module has four switch states that result in sub-module

capacitor being charged and discharged as shown in Table 2.2. Three distinct unipolar output voltages are generated by this sub-module (0,  $+V_o$  and  $+2V_o$ ) (see Figure 2.2(b)). Figure 2.2 (c) shows the two quadrant operation modes of this sub-module with quadrant 1 and 2 operating in inverting and rectifying modes respectively.

Table 2.2: Three-level FC half bridge sub-module operating states

Quad r ant State	Switch state				Diode state				$V_o$	$I_{ARM}$	Rectifie	Inverte
	$S_{a1}$	$S_{a2}$	$S_{a3}$	$S_{a4}$	$D_{a1}$	$D_{a2}$	$D_{a3}$	$D_{a4}$			r Mode	r Mode
											$I_{ARM}\uparrow$	$I_{ARM}\downarrow$
-	0	0	1	1	0	0	0	0	0	-1	-	NC
-	0	0	0	0	0	0	1	1	0	+1	NC	-
1A	0	1	0	0	0	0	0	1	0.5	+1	-	$C_A\downarrow$
2A	0	0	0	1	0	1	0	0	$V_C$	-1	$C_A\uparrow$	-
1A	1	0	0	0	0	0	1	0	0.5	+1	-	$C_{SM}\downarrow C_A\uparrow$
2A	0	0	1	0	1	0	0	0	$V_C$	-1	$C_{SM}\uparrow C_A\downarrow$	-
1	1	1	0	0	0	0	0	0	$V_C$	+1	-	$C_{SM}\downarrow$
2	0	0	0	0	1	1	0	0	$V_C$	-1	$C_{SM}\uparrow$	-

## 2.1.2 H-bridge cells

### 2.1.2.1 Three-level H-bridge cell

This type of sub-module has been mostly investigated for the single star and single delta MMCC STATCOM [71, 78]. The power circuit configuration is shown in Figure 2.3 (a). This comprises two pairs of complementary switches ( $S_{a1}$ ,  $S_{a2}$ ), ( $S_{a3}$ ,  $S_{a4}$ ) with their corresponding antiparallel diodes ( $D_{a1}$ ,  $D_{a2}$ ), ( $D_{a3}$ ,  $D_{a4}$ ) connected in parallel across the cell capacitor  $C_{SM}$ . This sub-module synthesizes three distinct output voltage levels (0,  $+V_o$  and  $-V_o$ ) as seen in Figure 2.3(b).

The sub-module allows four quadrant-operation as illustrated in Figure 2.3 (c). Quadrants 1, 3 and 2, 4 refer to the inverting and rectifying modes. Capacitor  $C_{SM}$  discharges under the inverting mode because the polarities of both the output voltage and converter arm current are in the same direction while the reverse is the case for the rectifying mode. The four switch states are illustrated in Table 2.3.

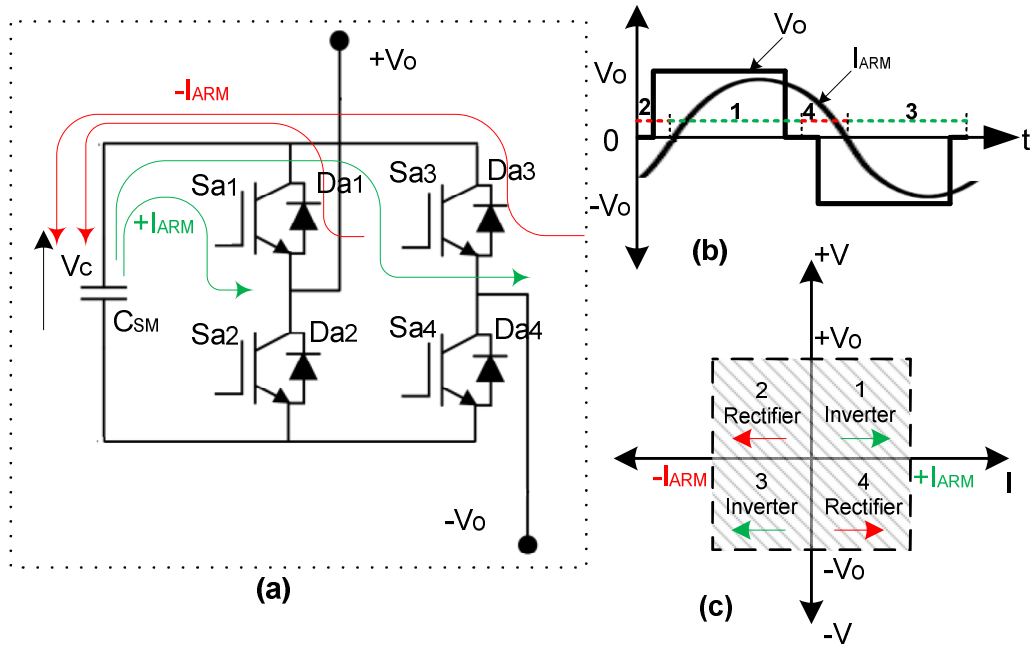


Figure 2.3: Three-level H-bridge sub-module: (a) Power Circuit; (b) sub-module output voltage and current; (c) and *i-v* four quadrant operation modes.

Table 2.3: Three-level H-bridge sub-module operating states

Quad rant State	Switch state				Diode state				$V_o$	$I_{ARM}$	Rectifie	Inverte
	$S_{a1}$	$S_{a2}$	$S_{a3}$	$S_{a4}$	$D_{a1}$	$D_{a2}$	$D_{a3}$	$D_{a4}$			r Mode	r Mode
											$I_{ARM}\uparrow$	$I_{ARM}\downarrow$
1	1	0	0	1	0	0	0	0	$V_c$	+1	-	$C_{SM}\downarrow$
2	0	0	0	0	1	0	0	1		-1	$C_{SM}\uparrow$	-
3	0	1	1	0	0	0	0	0	$-V_c$	-1	-	$C_{SM}\downarrow$
4	0	0	0	0	0	1	1	0		+1	$C_{SM}\uparrow$	-
-	1	0	0	0	0	0	1	0	0	+1	-	NC
-	0	0	1	0	1	0	0	0		-1	NC	-
-	0	1	0	0	0	0	0	1		-1	-	NC
-	0	0	0	1	0	1	0	0		+1	NC	-

### 2.1.2.2 Five-level Flying Capacitor bridge cell

The circuit configuration for this cell is shown in Figure 2.4 (a). It is formed by parallel connection of two 3-level FC half bridge converters along with one common sub-module capacitor  $C_{SM}$ . Consequently, there are two flying

capacitors ( $C_A$  and  $C_B$ ) each for its own half-bridge leg. This synthesizes five bipolar voltage levels ( $0, +V_o, +2V_o, -V_o$  and  $-2V_o$ ) as illustrated in Figure 2.4(b). The two inner flying capacitors have their voltages rated half of  $C_{SM}$  (i.e.  $V_A = V_B = 0.5V_C$ ). There are altogether 16 switch states that result in the sub-module capacitor  $C_{SM}$  and the two flying capacitors charging or discharging as shown in Table 2.4. The bipolar voltage nature of this sub-module ensures four quadrant operation which allow power flow in both directions as illustrated in Figure 2.4 (c).

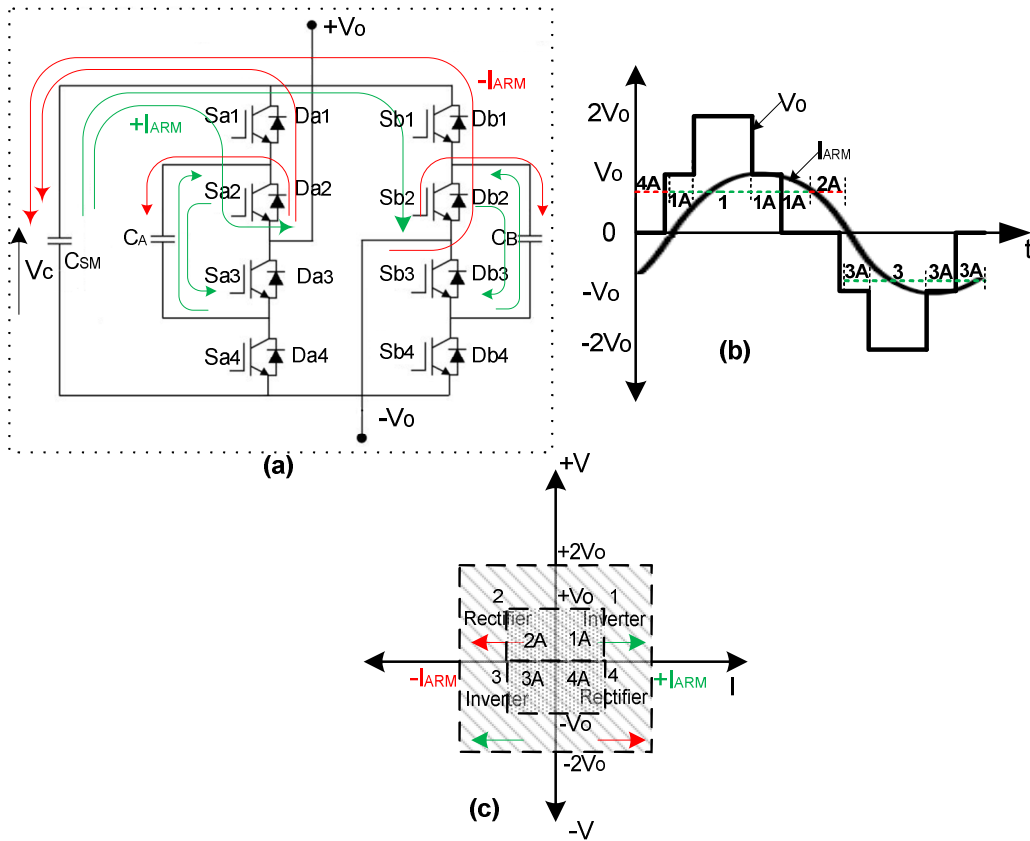


Figure 2.4: Five-level FC H-bridge sub-module: (a) Power Circuit; (b) sub-module output voltage and current; (c) and  $i$ - $v$  four quadrant operation modes.

Table 2.4: Five-level FC H-bridge sub-module operating states

Quadrant State	Switch state				Diode state				$V_o$	$I_{ARM}$	Rectifier	Inverter
	$S_{a1}$	$S_{a2}$	$S_{a3}$	$S_{a4}$	$D_{a1}$	$D_{a2}$	$D_{a3}$	$D_{a4}$			Mode	Mode
	$S_{b1}$	$S_{b2}$	$S_{b3}$	$S_{b4}$	$D_{b1}$	$D_{b2}$	$D_{b3}$	$D_{b4}$			$I_{ARM}\uparrow$	$I_{ARM}\downarrow$
1	1	1	0	0	0	0	0	0	$V_C$	+1	-	$C_{SM}\downarrow$
	0	0	1	1	0	0	0	0		-1	$C_{SM}\uparrow$	-
2	0	0	0	0	1	1	0	0	$V_C$	-1	$C_{SM}\uparrow$	-
	0	0	0	0	0	0	1	1		-	-	$C_{SM}\downarrow$
3	0	0	1	1	0	0	0	0	$V_C$	-1	-	$C_{SM}\downarrow$
	1	1	0	0	0	0	0	0		+1	$C_{SM}\uparrow$	-
4	0	0	0	0	0	0	1	1	$V_C$	+1	$C_{SM}\uparrow$	-
	0	0	0	0	1	1	0	0		-	-	$C_{SM}\downarrow$
1A	1	1	0	0	0	0	0	0	$0.5 V_C$	+1	-	$C_b\downarrow$
	0	0	1	0	1	0	0	0		-1	$C_b\uparrow$	-
2A	0	0	0	0	1	1	0	0	$0.5 V_C$	-1	$C_{SM}\uparrow$	-
	1	0	0	0	0	0	1	0		$C_b\downarrow$	$C_b\downarrow$	-
1A	1	1	0	0	0	0	0	0	$0.5 V_C$	+1	-	$C_{SM}\downarrow$
	0	0	0	1	0	1	0	0		-1	$C_b\uparrow$	$C_b\uparrow$
2A	0	0	0	0	1	1	0	0	$0.5 V_C$	-1	$C_{SM}\uparrow$	-
	0	1	0	0	0	0	0	1		$C_b\downarrow$	$C_b\downarrow$	-
1A	1	0	0	0	0	0	1	0	$0.5 V_C$	+1	-	$C_{SM}\downarrow$
	0	0	1	1	0	0	0	0		-1	$C_a\uparrow$	$C_a\uparrow$
2A	0	0	1	0	1	0	0	0	$0.5 V_C$	-1	$C_{SM}\uparrow$	-
	0	0	0	0	0	0	1	1		$C_a\downarrow$	$C_a\downarrow$	-
1A	0	1	0	0	0	0	0	1	$0.5 V_C$	+1	-	$C_a\downarrow$
	0	0	1	1	0	0	0	0		-1	$C_a\uparrow$	$C_a\uparrow$
2A	0	0	0	1	0	1	0	0	$0.5 V_C$	-1	$C_a\uparrow$	-
	0	0	0	0	0	0	1	1		-	-	$C_a\downarrow$
-	1	1	0	0	0	0	0	0	0	+1	-	NC
	0	0	0	0	1	1	0	0		-1	NC	-
-	0	0	0	0	1	1	0	0	0	-1	-	NC
	1	1	0	0	0	0	0	0		+1	NC	-
-	0	0	1	1	0	0	0	0	0	-1	-	NC
	0	0	0	0	0	0	1	1		+1	NC	-
-	0	0	0	0	0	0	1	1	0	+1	NC	-
	0	0	1	1	0	0	0	0		-1	NC	-

Quadrant State	Switch state				Diode state				$V_o$	$I_{ARM}$	Rectifier	Inverter
	$S_{a1}$	$S_{a2}$	$S_{a3}$	$S_{a4}$	$D_{a1}$	$D_{a2}$	$D_{a3}$	$D_{a4}$			Mode	Mode
	$S_{b1}$	$S_{b2}$	$S_{b3}$	$S_{b4}$	$D_{b1}$	$D_{b2}$	$D_{b3}$	$D_{b4}$			$I_{ARM\uparrow}$	$I_{ARM\downarrow}$
-	0	0	1	0	1	0	0	0	0	-1	-	$C_a\downarrow C_b\uparrow$
	1	0	0	0	0	0	1	0			+1	$C_a\uparrow C_b\downarrow$
-	1	0	0	0	0	0	1	0	0	+1	$C_a\downarrow C_b\uparrow$	-
	0	0	1	0	1	0	0	0			-1	-
-	0	1	0	0	0	0	0	1	0	+1	$C_a\downarrow C_b\uparrow$	-
	0	0	0	1	0	1	0	0			-1	-
1	1	0	0	0	0	0	1	0	0	+1	-	$C_{SM}\downarrow$ $C_a\uparrow C_b\uparrow$
	0	0	0	1	0	1	0	0			-1	$C_{SM}\uparrow$ $C_a\downarrow C_b\downarrow$
2	0	0	1	0	1	0	0	0	0	-1	$C_{SM}\uparrow$ $C_a\downarrow C_b\downarrow$	-
	0	1	0	0	0	0	0	1			-	-
2	0	0	0	1	0	1	0	0	0	-1	$C_{SM}\uparrow$ $C_a\downarrow C_b\downarrow$	-
	1	0	0	0	0	0	1	0			+1	-
3A	0	0	1	0	1	0	0	0	-0.5	-1	-	$C_a\downarrow$
	0	0	1	1	0	0	0	0			$V_C$	+1
4A	1	0	0	0	0	0	1	0	$V_C$	+1	$C_{SM}\uparrow$ $C_a\downarrow$	-
	0	0	0	0	0	0	1	1			-	-1
3A	0	0	0	1	0	1	0	0	-0.5	-1	-	$C_{SM}\downarrow$ $C_b\uparrow$
	1	1	0	0	0	0	0	0			$V_C$	+1
4A	0	0	0	0	0	0	1	1	$V_C$	+1	$C_{SM}\uparrow$ $C_b\downarrow$	-
	0	0	1	0	1	0	0	0			-	-1
3A	0	0	1	1	0	0	0	0	-0.5	-1	-	$C_b\downarrow$
	0	1	0	0	0	0	0	1			$V_C$	+1
4A	0	0	0	0	0	0	1	1	$V_C$	+1	$C_b\uparrow$	-
	0	0	0	1	0	1	0	0			-	-1



## 2.2 Classification of Modular Multilevel Converters

Various names have been used in the literature describing the modular multilevel converter topology such as  $M^2C$ ,  $M2C$ , Cascaded multilevel converter and Chain-link converter. In 2010, Akagi [75] presented a classification and terminology for this topology. This was done to establish consistency in the naming and classification of various types and differences in circuit structure. The name Modular Multilevel Cascaded Converter (MMCC) was adopted with four groups namely [75];

- Single Star Bridge Cells (MMCC-SSBC)
- Single Delta Bridge Cells (MMCC-SDBC)
- Double Star Chopper Cells (MMCC-DSCC)
- Double Star Bridge Cells (MMCC-DSBC)

Each of these groups has its distinct characteristics which make it suitable for certain applications. For consistency, the terms arm and limb are used interchangeably in this literature. This refers to a serial connection of cells that generate the same output voltage in an MMCC. In this discussion, capacitors are used to represent the storage elements. The above topologies can be further categorized into two groups, namely; those having no common dc-link being single cell types, normally used for STATCOM applications and those having a common dc-link being double star type, and typically used in HVDC systems. These are discussed below.

### 2.2.1 Single Cell types

This MMCC topology is built from H-bridge modules, which are either three-level or five-level flying capacitor full bridge. Multiples of such modules are stacked-up to form a phase limb and there is no common dc-link required. Half bridge cells cannot be used to build this type of converter because of their unipolar output voltage. Applications of this topology include flexible AC Transmission devices, such as STATCOM, Battery Energy Storage System (BESS) [78, 128-130], and grid connection inverters for distributed energy sources [131].

#### 2.2.1.1 Single Star Bridge Cells (MMCC-SSBC)

The configuration of the MMCC-SSBC is illustrated in Figure 2.5 using either three-level or five-level FC H-bridges. Each phase arm of this topology comprises  $N$  cells stacked-up. The ac terminals of the three converter arms ( $A_1$ ,  $B_1$  and  $C_1$ ) are connected to the ac mains ( $A_2$ ,  $B_2$  and  $C_2$ ) through the arm impedances ( $R_{CABC}$  and  $L_{CABC}$ ) which are used for converter current filtering. The other ends of the converter arm terminals are connected together forming

the neutral point which is either floating or grounded depending on the application requirements.

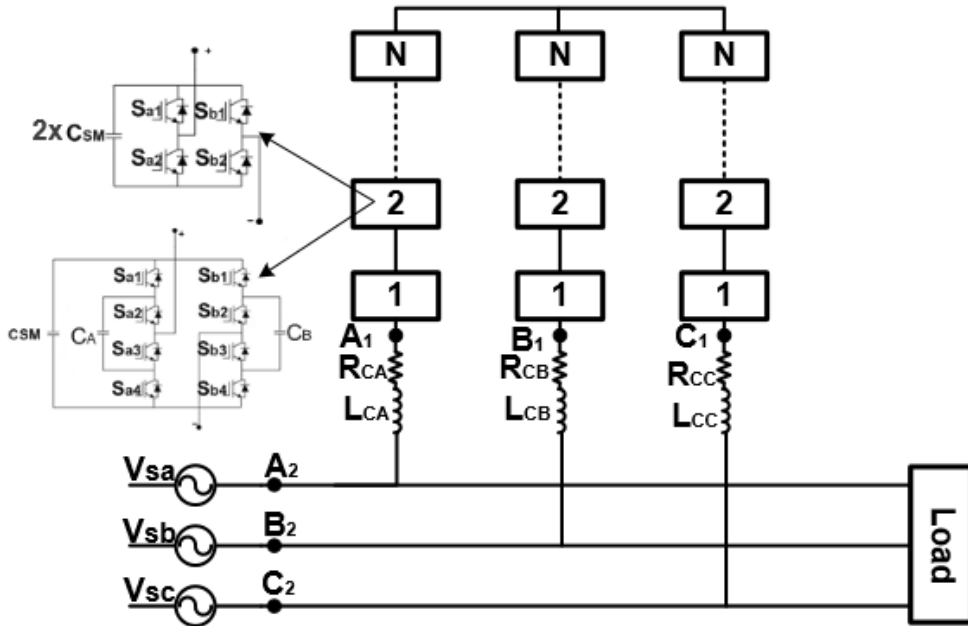


Figure 2.5: MMCC single star structure.

The terminal voltage of each phase arm is dependent on the number of sub-modules switched into the current flow path and their respective dc voltages, and is expressed as:

$$v_{ci} = m_a N_j V_{dc\_sm} \sin(\omega t + \phi_{vc}) \quad (2.1)$$

where  $m_a$ ,  $N_j$  and  $V_{dc\_sm}$  are the converter modulation index, number of sub-modules switching into the conduction path, and sub-module dc capacitor voltage;  $i$  represents phases  $a$ ,  $b$  or  $c$  with phase angles  $\phi_{vc} = [0, 2\pi/3, 4\pi/3]$  respectively.

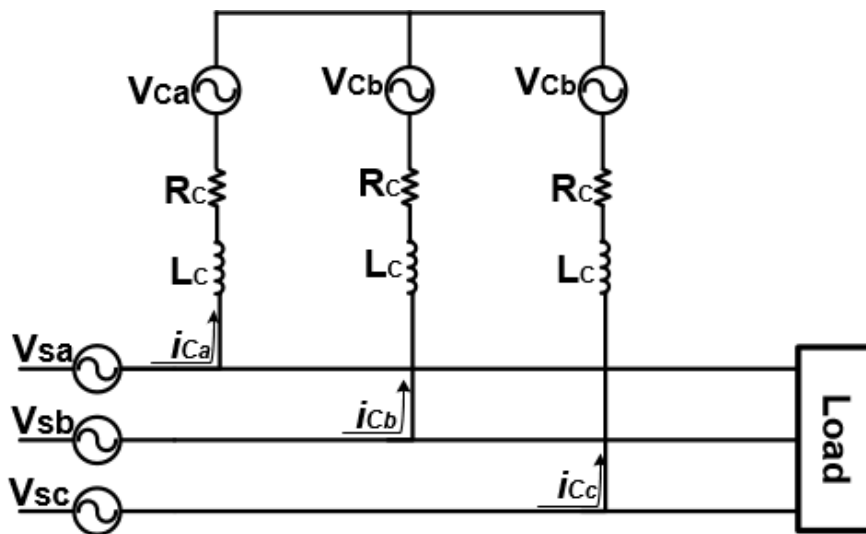


Figure 2.6: MMCC single star equivalent circuit.

The direction of the phase current and the switch states of each sub-module decide how the sub-module capacitor voltages being charged and discharged. With reference to the equivalent circuit illustrated in Figure 2.6 the current in each phase, is expressed as:

$$i_{ci} = I_c \sin(\omega t + \varphi_{vc} + \varphi_{ic}) \quad (2.2)$$

where  $\varphi_{ic}$  is the current phase angle with respect to its terminal voltage and  $I_c$  the maximum phase current. The fundamental frequency component of  $i_{ci}$  defines the active and reactive power exchange between the ac grid and converter side.

The voltage equation of the SSBC-MMCC per phase leg as seen in Figure 2.6 is:

$$v_{si} - v_{ci} = R_c i_{ci} + L_c \frac{di_{ci}}{dt}. \quad (2.3)$$

Substituting (2.1) into (2.3) and expressing (2.3) with respect to the converter current derivative, we have:

$$\frac{di_{ci}}{dt} = \frac{v_{si}}{L_c} - \frac{m_a N_j V_{dc\_sm} \sin(\omega t + \varphi_{vc})}{L_c} - \frac{R_c}{L_c} i_{ci}. \quad (2.4)$$

Assuming switching losses are negligible, power on both ac and dc sides of the SSBC per phase cluster should be equal, thus:

$$N_j V_{dc\_sm} I_{dc\_sm} = v_{ci} i_{ci} \quad (2.5)$$

where  $I_{dc\_sm}$  is the current flowing through the sub-module capacitor. This current can be expressed in terms of sub-module capacitance and ac power as:

$$I_{dc\_sm} = \frac{v_{ci} i_{ci}}{N_j V_{dc\_sm}} = C_{sm} \frac{dV_{dc\_sm}}{dt}. \quad (2.6)$$

From this the dc voltage derivative term can be expressed as;

$$\frac{dV_{dc\_sm}}{dt} = \frac{v_{ci} i_{ci}}{N_j C_{sm} V_{dc\_sm}} = \frac{m_a i_{ci} \sin(\omega t + \varphi_{vc})}{C_{sm}}. \quad (2.7)$$

According to Equations (2.4) and (2.7), the state–space model of the single star MMCC can be written as:

$$\dot{x} = Ax + Bu \quad (2.8)$$

$$\text{where } x = \begin{bmatrix} i_{ci} \\ V_{dc\_sm} \end{bmatrix}; A = \begin{bmatrix} -\frac{R_c}{L_c} & -m_a N_j \sin(\omega t + \varphi_{vc}) \\ \frac{m_a \sin(\omega t + \varphi_{vc})}{C_{sm}} & 0 \end{bmatrix}, u = \begin{bmatrix} v_{si} \\ 0 \end{bmatrix},$$

$$B = \begin{bmatrix} \frac{1}{L_c} & 0 \\ 0 & 0 \end{bmatrix}.$$

Under balanced operation there is no circulating current flowing between phase arms. With unbalanced condition, both positive and negative sequence symmetrical components interact, zero sequence voltage may be injected to the converter neutral point [116].

### 2.2.1.2 Single Delta Bridge Cells

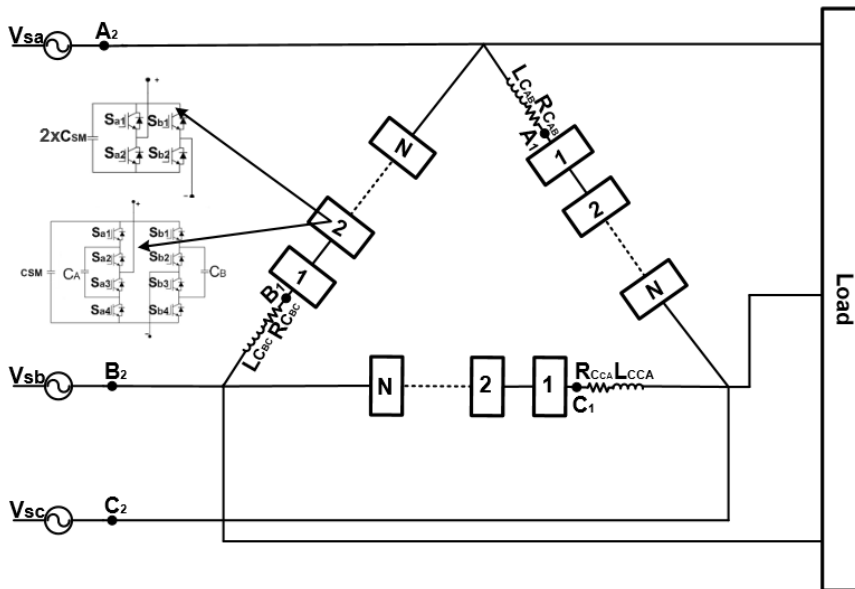


Figure 2.7: MMCC single delta structure.

The configuration of the MMCC-SDBC is illustrated in Figure 2.7. The individual converter arms (AB, BC and CA) consist of  $N$  serially connected modules and they are connected in a delta form. This configuration neither provides a common dc-link nor common neutral point. If the converter arm voltage rating is lower than that of ac supply mains, a transformer having either floating star or delta configurations at the converter end is required.

The state-space model of this converter is the same as that of the SSBC and is expressed as:

$$\begin{bmatrix} \dot{i}_{ci} \\ V_{dc\_sm} \end{bmatrix} = \begin{bmatrix} -\frac{R_c}{L_c} & -m_a N_j \sin(\omega t + \pi/6 + \varphi_{vc}) \\ \frac{m_a \sin(\omega t + \pi/6 + \varphi_{vc})}{C_{sm}} & 0 \end{bmatrix} \begin{bmatrix} i_{ci} \\ V_{dc\_sm} \end{bmatrix} + \begin{bmatrix} 1 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} v_{si} \\ 0 \end{bmatrix} \quad (2.9)$$

where  $v_{si}$  and  $i_{ci}$  are the ac grid line voltages ( $v_{sab}$ ,  $v_{sbc}$  and  $v_{sca}$ ) and converter phase currents ( $i_{cab}$ ,  $i_{cbc}$  and  $i_{cca}$ ).

Circulating current flows within the SDBC phase arms when any form of unbalance occurs as seen in Figure 2.8. This current is expressed as:

$$i_z = \frac{1}{3}(i_{cab} + i_{cbc} + i_{cca}) = I_z \sin(\omega t + \varphi_{iz}) . \quad (2.10)$$

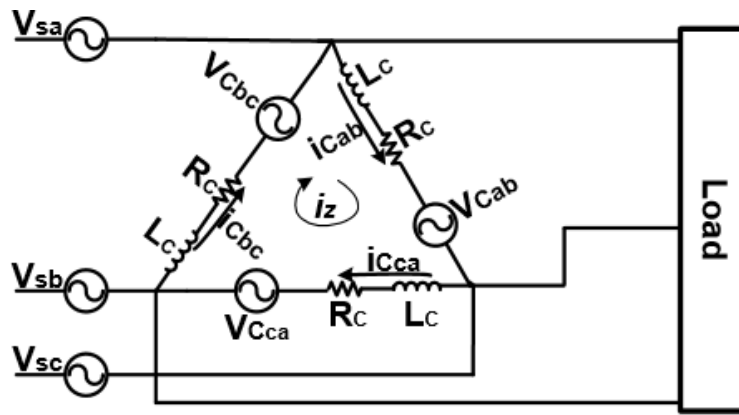


Figure 2.8: Circulating Current flow in MMCC single delta structure.

This current aids the arm voltage balance in this configuration via interacting with both positive and negative sequence symmetrical components of the converter, but imposes limitations on this converter's current rating.

### 2.2.2 Double Cell types

This can be implemented using either half-bridge (chopper) or H-bridge cells as sub-modules, depending on the application requirement. This MMCC topology is an extension of the single star cell. The double star topology aids applications which require a common dc-link in particular the HVDC systems. The double delta MMCC has neither received industrial interest nor analysed in any academic literature because no additional benefit has been seen by using this topology. Hence it is not considered.

The double star topology can be implemented either with chopper cells (i.e. two-level half bridge and three-level FC half bridge) or H-bridge cells (i.e. three-level H-bridge and five-level FC H-bridge). Figure 2.9 shows the MMCC double star configuration. When implemented with the chopper cell, it is known as double star chopper cell (DSCC), while with H-bridge it is known as double

star bridge cell (DSBC). Ideally, this configuration is formed by phase-parallel connection of two single-star MMCC. Each phase of this topology consist of two arms per phase namely; the top and bottom arms. These top and bottom arms of each phase are connected by the converter arm reactors ( $L_{Cat}$ ,  $L_{Cab}$ ,  $L_{Cbt}$ ,  $L_{Cbb}$ ,  $L_{Cct}$ , and  $L_{Ccb}$ ) to form the AC phase terminals ( $A_2$ ,  $B_2$  and  $C_2$ ). The top and bottom arms are joined together to form a common dc bus with the positive terminal formed by the three top arms ( $+0.5V_{dc}$ ) while the negative terminal formed by the bottom arms ( $-0.5V_{dc}$ ).

### 2.2.2.1 Double Star Cells

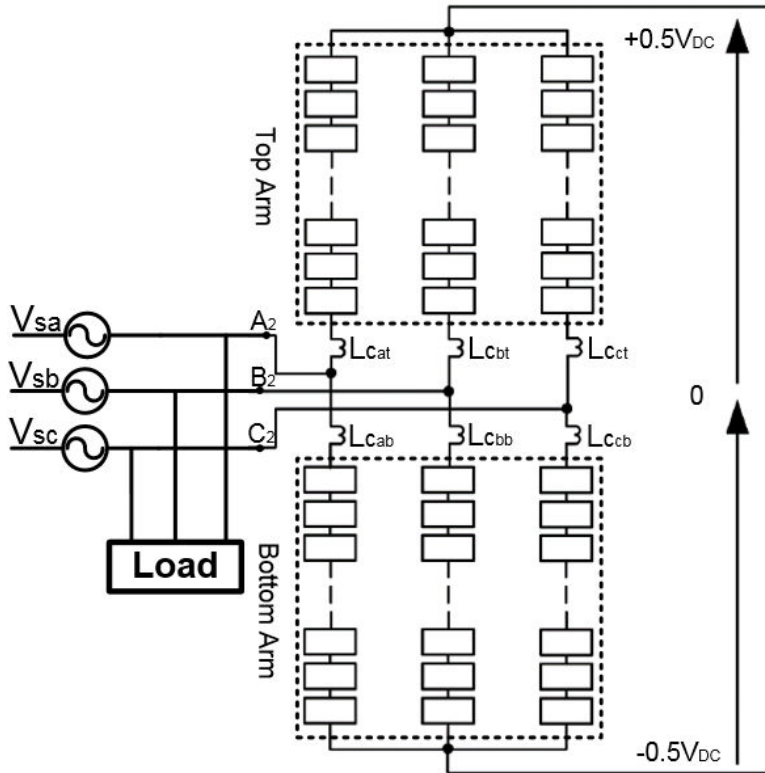


Figure 2.9: MMCC double star cell structure.

Both top and bottom arms conduct simultaneously, thus the voltage across both top and bottom arms is expressed as:

$$\begin{aligned} v_{ti} &= 0.5V_{dc} (1 - m_a \sin(\omega t + \varphi_{vc})) \\ v_{bi} &= 0.5V_{dc} (1 + m_a \sin(\omega t + \varphi_{vc})) \end{aligned} \quad (2.11)$$

where  $v_{ti}$ ,  $v_{bi}$  and  $V_{dc}$  are the top arm, bottom arm and dc-link voltage of the converter. The arm currents across each phase is a summation of both ac and dc component. Based on the MMCC equivalent circuit shown in Figure 2.10, the waveforms of the top arm, bottom arm and phase voltages when both H-bridge and half bridge cells are used, are shown in Figure 2.11. For both bridge and chopper cells, the top and bottom arm voltages satisfy the following as shown in Table 2.5.

Table 2.5: Top and bottom arm voltages of double star cells

Arm voltages	DSBC	DSCC
Top	$-V_{C_{ti}} \leq v_{ti} \leq V_{C_{ti}}$	$0 \leq v_{ti} \leq V_{C_{ti}}$
Bottom	$-V_{C_{bi}} \leq v_{bi} \leq V_{C_{bi}}$	$0 \leq v_{bi} \leq V_{C_{bi}}$

where  $V_{C_{ti}}$  and  $V_{C_{bi}}$  are the top and bottom arm cell dc voltages. From Figure 2.11, the phase voltage waveform generated by DSBC is twice the magnitude synthesized by the DSCC counterpart, where both cells are equally rated.

The top and bottom arm currents per phase are expressed as:

$$\begin{aligned} i_{ti} &= 0.5i_{si} + i_{zi} \\ i_{bi} &= i_{zi} - 0.5i_{si} \end{aligned} \quad (2.12)$$

where  $i_{si}$  is the phase current and  $i_{zi}$  represents the circulating current component or common mode current which shows the power exchange relationship between the dc side and converter side. The summation of the circulating current across the phases equals zero. This means that the circulating current only flows within the converter circuit. The MMCC phase leg equation for Figure 2.10 are:

$$\begin{aligned} 0.5V_{dc} &= v_{si} + v_{ti} + R_c i_{ti} + L_c \frac{di_{ti}}{dt} \\ 0.5V_{dc} &= -v_{si} + v_{bi} + R_c i_{bi} + L_c \frac{di_{bi}}{dt} \end{aligned} \quad (2.13)$$

Summing up both top and bottom arm voltages is expressed as:

$$V_{dc} = v_{ti} + v_{bi} + R_c (i_{ti} + i_{bi}) + L_c \frac{d(i_{ti} + i_{bi})}{dt} \quad (2.14)$$

Adding up the top and bottom arm currents yield:

$$i_{ti} + i_{bi} = 2i_{zi} \quad (2.15)$$

Substituting (2.15) into (2.14) gives:

$$\frac{di_{iz}}{dt} = \frac{1}{2L_c} [V_{dc} - (v_{ti} + v_{bi})] - \frac{R_c}{L_c} i_{zi} \quad (2.16)$$

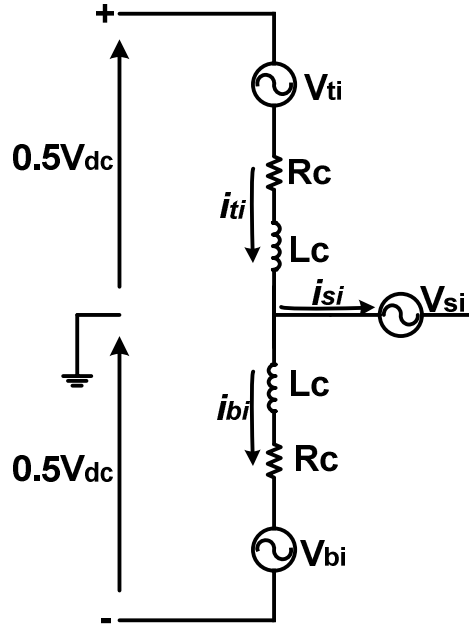


Figure 2.10: double star MMCC single phase equivalent circuit.

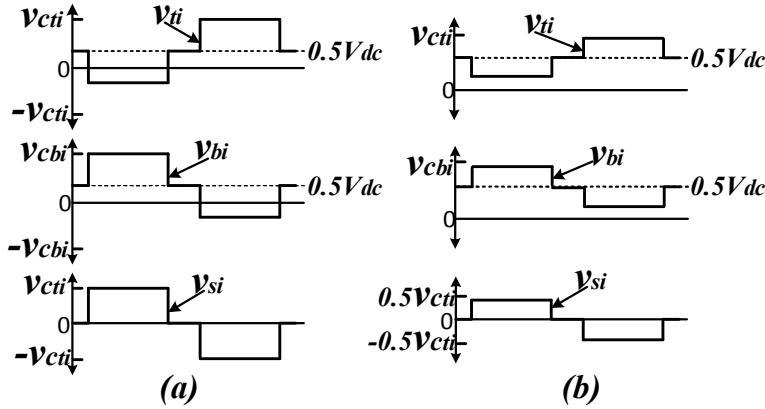


Figure 2.11: Waveforms of top, bottom arms and phase voltage (a) DSBC and (b) DSCC.

The current flowing in both top and bottom arms can be expressed in terms of the arm capacitors per phase as:

$$i_{ti} = \frac{N_{ti}}{N} C \frac{dv_{ti}}{dt}, i_{bi} = \frac{N_{bi}}{N} C \frac{dv_{bi}}{dt} . \quad (2.17)$$

Putting (2.12) into (2.17) gives;

$$\begin{aligned} \frac{dv_{ti}}{dt} &= \frac{N_{zi}}{N_i C} + \frac{N_{si}}{2N_i C} \\ \frac{dv_{bi}}{dt} &= \frac{N_{zi}}{N_i C} - \frac{N_{si}}{2N_i C} \end{aligned} \quad (2.18)$$

The state-space model of the double star MMCC topology is given as:



$$\begin{bmatrix} \dot{i}_{zi} \\ v_{ti} \\ v_{bi} \end{bmatrix} = \begin{bmatrix} -\frac{R_c}{L_c} & -\frac{1}{2L_c} & -\frac{1}{2L_c} \\ \frac{N}{N_{ti}C} & 0 & 0 \\ \frac{N}{N_{bi}C} & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{zi} \\ v_{ti} \\ v_{bi} \end{bmatrix} + \begin{bmatrix} \frac{1}{2L_c} & 0 & 0 \\ 0 & \frac{N}{2N_{ti}C} & 0 \\ 0 & -\frac{N}{2N_{bi}C} & 0 \end{bmatrix} \begin{bmatrix} V_{dc} \\ i_{si} \\ 0 \end{bmatrix}. \quad (2.19)$$

Equation (2.19) can be used in designing controllers for the MMCC. The Similar modulation techniques can be applied to control both the single and double cell structures. However, the current control strategies may be more complex. [132-135].

### 2.2.3 Emerging MMCC Topologies

The emergence of new MMCC circuit structures is driven by the need to improve efficiency, cost, functionality (i.e. fault blocking capability) and footprint. Academic and industrial researchers are suggesting new MMCC configurations for HVDC applications. These emerging topologies are classified either as parallel-hybrid or series-hybrid configuration. This describes the way the converter arms between the ac and dc terminals are connected. An example of the parallel-hybrid type is the alternate arm converter (ACC). Each arm comprises a series connection of director switches and a string of H-bridge sub-modules. Three phase arms are connected in parallel to the two dc terminals. The use of H-bridge sub-modules inherently limit dc-side short-circuit faults. The use of the director switches reduces the number of sub-modules, hence the conduction losses per converter arm by 40% [136-138] when compared with MMCC-DSBC for the same rating. This has the ability of ride through ac faults [139]. An example of the series-hybrid is the series bridge converter. Each arm comprises a parallel connection between an H-bridge circuit and a series string of modules. Each arms are connected in series to either absorb or supply power to the dc-link. Both the ACC [140, 141] and SBC [142, 143] are subject of intensive research.

## 2.3 Analysis of MMCC Configurations for STATCOM

The various MMCC configurations and sub-module types discussed in the previous section will be analysed and compared for STATCOM application, based on the following metrics of footprint, cost, control capability, and control complexity.

### 2.3.1 Sub-module Components

For this investigation, the MMCC-based STATCOMs are applied to a distribution grid system rated at 11kV for either voltage regulation or unity

power factor correction. The fundamental components used in any of the four sub-modules for implementing the various MMCC configurations are [35];

- Power semiconductor switch comprising two complementary IGBT switches with anti-parallel diode connected across each IGBT.
- Heat sink
- Electrolytic capacitor (for convenience)
- Gate drive electronic module (GEM) which comprises field programmable gate array (FPGA) and transducers (LEM).

The various components used for all the different sub-modules are shown in Table 2.6. All specifications for the components are obtained from their manufacturers' datasheets.

### 2.3.2 Sub-module Number Requirement Based on MMCC Configuration

The cell count/phase ratio and number of sub-modules required per phase for different MMCC configurations is shown in Table 2.7.

Table 2.6: Components used for sub-module analysis

Component	Part Number	Rating
IGBT switch module	Infineon IKW30N60T	600V, 30A
Heat sink	Fisher electronics SK105/105SA	$R_{th}=2K/W$
Capacitor	EETED2G561EA (Panasonic)	400V, 560 $\mu$ F
Gate electronics module	Actel ProASIC3 FPGA Board	Only key parts are considered
	Gate drive circuits	
	LEM LV 25-P (Voltage transducer)	

### 2.3.3 Metrics Analysis

The metrics of footprint, cost, redundancy and control complexity are applied in the following analysis.

#### 2.3.3.1 Footprint

A converter layout similar to that used by ABB and Alstom [144, 145] in a high voltage transmission grid system is assumed in this analysis. Both the sub-module layout and a single phase platform layout is as shown in Figure 2.12.

Table 2.7: Number of sub-modules required per phase limb

Cell count/phase	No. of sub-modules/phase	2-L half bridge	3-L FC half bridge	3-L H-bridge	5-L FC H-bridge
1	Single star	-	-	27.5≈28	13.75≈14
√3	Single delta	-	-	47.63≈48	23.82≈24
4	DSCC	112	56	-	-
2	DSBC	-	-	56	28

A sub-module layout consists of cell capacitors, a switch module (heat sink included) and the gate electronics module. Each sub-module is kept in an enclosure which is suspended from the earthing plane, i.e. the ceiling of the building housing of the converter. This is done to make sure protection against natural disaster [145-147]. The platform shelter height is determined by both the number of sub-modules and the unified specific creepage distance (USCD) between adjacent tiers of sub-modules. The IEC60815 [145] specifies the USCD as 3.5cm/kV.

The converter footprint calculation is based on the USCD and the number of sub-modules needed to reach the required voltage rating and is basically a function of the width (X) and height (Y) of the converter platform. The expression for the footprint is:

$$F = (n_t Y_{sm} + (n_t + 1) Y_{cd}) n_{smt} X_{sm} \quad (2.20)$$

where  $n_t$  = Required number of sub-modules tiers,  $n_{smt}$  = Required number of sub-modules per tiers,  $Y_{sm}$  = Sub-modules height,  $Y_{cd}$  = Inter-tier insulation clearance gap and  $X_{sm}$  = sub-modules width

The value of their inter-tier insulation clearance gap is expressed as

$$Y_{cd} = USCD \frac{\text{voltage rating of converter}}{\text{required number of sub - moduletiers}} \quad (2.21)$$

Where  $USCD = 3.5 \text{ cm/kV}$

In this analysis, 7 and 6 tiers are used for all the sub-module types' layout for single star, double star and single delta. This is because the height of the building for an onshore application is limited by the local planning regulations[148]. Therefore, the insulation clearance gap of each inter-tier is evaluated as:

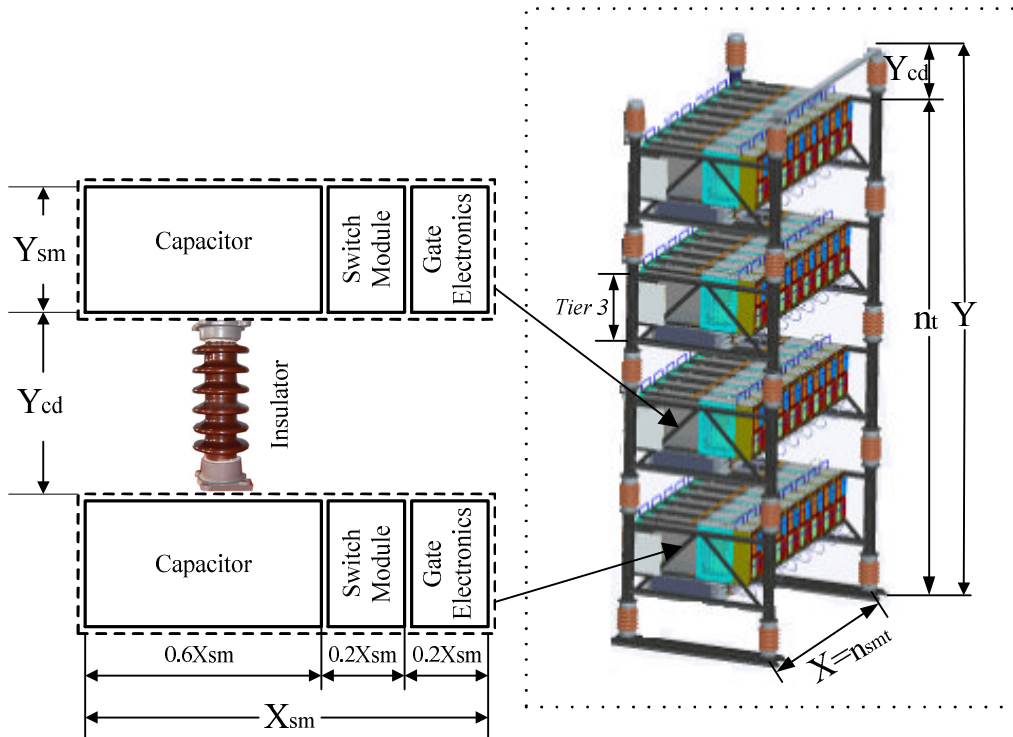


Figure 2.12: Guideline for footprint assessment (a) sub-module layout showing clearance distance (i.e. insulation between two sub-modules); (b) single platform layout with sub-modules [35, 148].

$$Y_{cd} = \frac{3.5cm}{kV} \times \frac{11kV}{7} = 5.5cm$$

for both single star and double star configurations while for single delta configuration it is calculated as:

$$Y_{cd} = \frac{3.5cm}{kV} \times \frac{11kV}{6} = 6.416cm .$$

Table 2.8 shows the per-unit size for a sub-module.

Table 2.8: Per-unitised sizes for sub-module width

Component	Quantity	Comments
<b>IGBT Switch Module</b>	$X_s = 20\%$ of $X_{SM}=0.2$	
<b>Capacitor</b>	$X_c = 60\%$ of $X_{SM}=0.6$	Normally around 50-60% of sub-module width[144]
<b>Gate electronics module</b>	$X_{GEM} = 20\%$ of $X_{SM}=0.2$	

The height  $Y_{sm}$  is based on a heat sink having the largest height of 20cm and total width  $X_{sm}$  is assumed three times of  $Y_{sm}$  i.e. 60 cm, which gives a dimension of 20 cm x 60 cm.

Table 2.9 shows the relationship between the numbers of tiers and the number of sub-modules per tier for all the different sub-module types.

Table 2.9:  $n_t$  and  $n_{smt}$  for sub-module types based on different MMCC configurations

Sub-module types		Two-level half bridge	Three-level FC half bridge	Three-level H-bridge	Five-level FC H-bridge
Single star	$n_t$	-	-	7	7
	$n_{smt}$	-	-	4	2
Single delta	$n_t$	-	-	6	6
	$n_{smt}$	-	-	8	4
double star	$n_t$	7	7	7	7
	$n_{smt}$	16	8	8	4

The analysis of the different MMCC configurations and sub-module types under footprint metrics is discussed below.

Table 2.10: Sub-module per unit width and MMCC configuration Footprint calculation

Component	2L-half bridge		3L-FC half bridge		3L-H-bridge		5L-FC H-bridge	
	Qty	Width (pu)	Qty	Width (pu)	Qty	Width (pu)	Qty	Width (pu)
$X_s$	1	0.2	2	0.4	2	0.4	4	0.8
$X_c$	1	0.6	3	1.8	1	0.6	4	2.4
$X_{GEM}$	1	0.2	1	0.2	1	0.2	1	0.2
$X_{sm}$ (pu)		1		2.4		1.2		3.4
<b>Footprint (m<sup>2</sup>)</b>								
Single star		-		-		5.2992		7.5072
Single delta		-		-		9.4985		13.456
Double star		17.664		21.1968		10.5984		15.0144

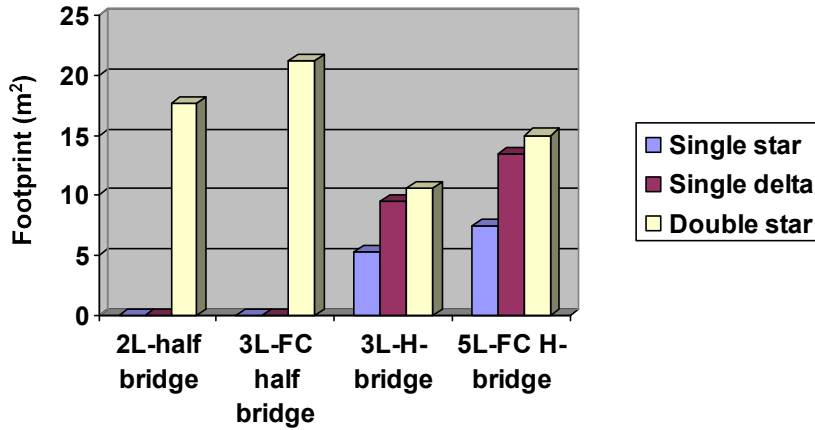


Figure 2.13: MMCC-STATCOM footprint assessment.

From the platform calculation plot shown in Figure 2.13, it is seen that for STATCOM application (i.e. balance system compensation) the single star configuration provides the best footprint among the other MMCC configurations. This is because the number of sub-modules required for this application is the lowest. On the other hand when half-bridge sub-modules are used for double star STATCOM applications the resultant footprint is the highest. Among the sub-module types, the 3-level H-bridge provides the lowest footprint followed by the 5-level FC H-bridge, where both are for single star configuration.

### 2.3.3.2 Cost

The cost is evaluated according to the prices of the components required in building each sub-module type for different MMCC configurations. For a practical MMC converter, the real prices of components are not disclosed by the converter manufacturer. In this analysis, the cost metrics of a sub-module are based instead on the prices of the key components which are obtainable from the Farnell website. The component prices for a sub-module unit are shown in Table 2.11, only the unit cost of a component is considered.

The unit (i.e. sub-module) and total cost of implementing the different MMCC configurations are shown in Table 2.12.

From the cost metric plot in Figure 2.14, the single star configuration provides the lowest cost among all the MMCC configurations considered here, followed by single delta and double star using 3-level H-bridge. This is because the cost has a direct relationship with the number of components required per configuration. From the cost analysis, double star MMCC especially the 3L-FC half bridge sub-module types cost the most.

Table 2.11: Prices of components for one sub-module unit

Component	Part Number	Unit cost (£)
IGBT switch module	IKW30N60T (1 pair)	9.14
Heat sink	SK105	6.58
Capacitor	EETED2G561EA (Panasonic)	8.64
Gate electronics module	Actel ProASIC3 FPGA Board	6.75
	Gate drive +Isolation (ACPL-332J; MEV1S0515SC)	12.85
	LEM LV 25-P (Voltage transducer)	52.69

Table 2.12: sub-module and MMCC configuration cost calculation

Component	2L-half bridge		3L-FC half bridge		2L-H-bridge		3L-FC H-bridge		
	Qty	cost (£)	Qty	cost (£)	Qty	cost (£)	Qty	cost (£)	
<b>IGBT switch</b>	1	9.14	2	18.28	2	18.28	4	36.56	
<b>Heat sink</b>	1	6.58	2	13.16	2	13.16	4	26.32	
<b>Capacitor</b>	1	8.64	3	25.92	1	8.64	4	34.56	
<b>GEM</b>	<b>FPGA</b>	1	6.75	1	6.75	1	6.75	1	6.75
	<b>Gate driver</b>	2	25.7	4	51.40	4	51.40	8	102.80
	<b>LEM LV25</b>	1	52.69	2	105.4	1	52.69	3	158.07
<b>Unit cost (£)</b>		109.5		220.89		150.92		365.06	
<b>Total cost (£)</b>									
<b>Single star</b>		-		-		4225.76		5110.84	
<b>Single delta</b>		-		-		7244.16		8761.44	
<b>Double star</b>		12264		12369.84		8451.52		10221.68	

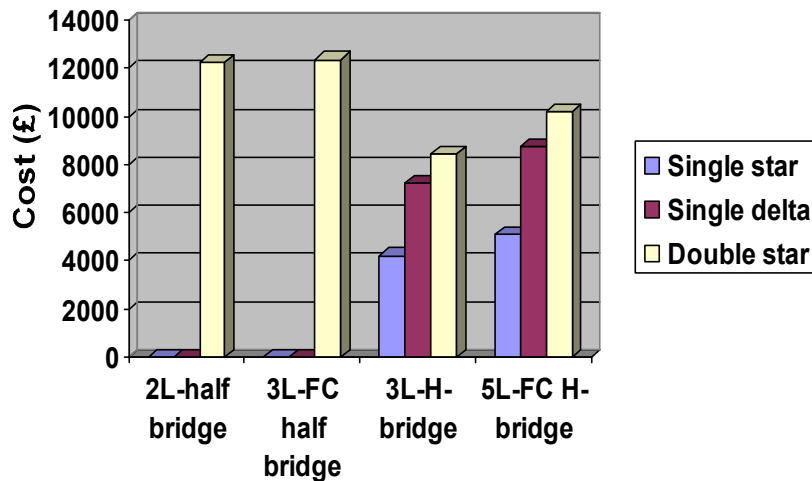


Figure 2.14: MMCC-STATCOM cost assessment.

### 2.3.3.3 Redundancy

Redundancy here is the number of distinct combinations of switch states which gives rise to the same sub-module output voltage. For example, the 3L-FC half bridge module has one redundancy since the switch states for charging its inner capacitor and that for discharging it give the same sub-module output voltage.

The state in which a sub-module operates as an uncontrolled rectifier (i.e. no switching pulse is applied) is not considered as an operating state, but rather as a start-up strategy for charging up capacitors of sub-modules in an MMCC. This is done before normal operation of the MMCC.

The various ways of charging and discharging each sub-module capacitors and the different MMCC configurations are listed in both Table 2.13 and 2.14 respectively.

From Table 2.13, it can be seen that the FC H-bridge sub-module provides more redundant states than the rest of the sub-module types. This is considered an advantage for using FC topology. It is seen that both FC sub-module inner capacitors are effectively charged and discharged during the inverter mode by using the necessary switch states without implementing any feedback control.

From Table 2.14, it can be also seen that the 5-level FC H-bridge implemented in double star configuration has the highest number of charging and discharging combinations compared to other configurations. This benefit is at the detriment of cost and footprint.



Table 2.13: Possible charging and discharging sub-module and inner capacitor combinations for different sub-modules

<b>Sub-module type/Mode of operation</b>		<b>Sub-module charge/discharge combination</b>						<b>Unit Total</b>
		<b>Charging</b>			<b>Discharging</b>			
		<b>C<sub>SM</sub></b>	<b>C<sub>A</sub></b>	<b>C<sub>B</sub></b>	<b>C<sub>SM</sub></b>	<b>C<sub>A</sub></b>	<b>C<sub>B</sub></b>	
<b>2L-half bridge</b>	<i>Inverting</i>	-	-	-	1	-	-	2
	<i>Rectifying</i>	1	-	-	-	-	-	
	<i>No. of ways</i>	1	-	-	1	-	-	
<b>3L-FC half bridge</b>	<i>Inverting</i>	-	1	-	2	1	-	6
	<i>Rectifying</i>	2	1	-	-	1	-	
	<i>No. of ways</i>	2	2	-	2	2	-	
<b>3L-H-bridge</b>	<i>Inverting</i>	-	-	-	2	-	-	4
	<i>Rectifying</i>	2	-	-	-	-	-	
	<i>No. of ways</i>	2	-	-	2	-	-	
<b>5L-FC H-bridge</b>	<i>Inverting</i>	-	4	4	6	4	4	28
	<i>Rectifying</i>	6	4	4	-	4	4	
	<i>No. of ways</i>	6	8	8	6	8	8	

Table 2.14: Possible redundant combinations of sub-module types across different MMCC configurations

<b>MMCC Configurations</b>	<b>Two-level half bridge</b>	<b>Three-level FC half bridge</b>	<b>Three-level H-bridge</b>	<b>Five-level FC H-bridge</b>
<b>Single star</b>	-	-	112	392
<b>Single delta</b>	-	-	192	672
<b>Double star</b>	224	336	224	784

### 2.3.3.4 Control complexity

The complexity of control required to do STATCOM operation varies with different MMCC configurations and sub-module type. This metric will be based on the number of control variables required to meet correct operation of the MMCC-STATCOM. The control variables of each configuration are highlighted in Table 2.15. Control complexity can also be assessed for the different sub-module types to identify which components need to be controlled to achieve adequate operation. Table 2.16 shows the required number of components per sub-module.

The double star topology requires the highest complexity of control when compared to the other two configurations as seen in Table 2.15. It requires regulation of the common dc-link voltage, top and bottom arm voltages and currents, and suppression of the circulating current flowing between phase arms. It is important to state that circulating current control is only required in single delta MMCC's when an unbalanced condition occurs. This will be discussed in detail in Chapters 6.

Table 2.15: Control complexity assessment for each MMCC-configuration

<i>MMCC configuration</i>	<i>Common dc-link control</i>	<i>Phase cluster arm control</i>	<i>Sub-module control</i>	<i>Circulating current control</i>	<i>Total</i>
<i>Single star</i>	-	1	1	-	2
<i>Single delta</i>	-	1	1	-	2
<i>Double star</i>	1	2	1	1	5

Table 2.16: Control complexity assessment for each sub-module type

<i>Sub-module types</i>	<i>Two-level half bridge</i>	<i>Three-level FC half bridge</i>	<i>Three-level H-bridge</i>	<i>Five-level FC H-bridge</i>
<i>Sub-module capacitor</i>	1	1	1	1
<i>Inner capacitor</i>	-	1	-	2
<i>Total control</i>	1	2	1	3

The 5L-FC H-bridge requires 1 and 2 more levels of control with respect to both 3L-FC half bridge, 2L-half bridge, 3L H-bridge respectively. This higher control complexity limits its operation for STATCOM application. However, control complexity of the 5L-FC H-bridge is reduced to 1 by applying advanced modulation techniques that ensure adequate natural balancing of the inner capacitors without needing extra control loops. This will be discussed in detail in Chapters 3 and 4.

### 2.3.4 Comparison of Sub-module Concepts for an 11kV MMCC-STATCOM

Table 2.17, summarises the metrics of the various MMCC configurations using different sub-module types. The following conclusions can be drawn:

Table 2.17: Comparison of MMCC types based on 11kV STATCOM

<b>MMCC configuration</b>	<b>Footprint (m<sup>2</sup>)</b>	<b>Cost (£)</b>	<b>Redundancy</b>	<b>Control complexity</b>
<b>Single star</b>				
<b>3L-H-bridge</b>	5.30	4226	112	56
<b>5L-FC H-bridge</b>	7.51	5111	392	84
<b>Single delta</b>				
<b>3L-H-bridge</b>	9.50	7244	192	96
<b>5L-FC H-bridge</b>	13.46	8761	672	144
<b>Double star</b>				
<b>2L-half bridge</b>	17.66	12264	224	560
<b>3L-FC half bridge</b>	21.2	12370	336	560
<b>3L-H-bridge</b>	10.6	8451	224	280
<b>5L-FC H-bridge</b>	15.01	10222	784	420

- **Single star MMCC:** this can be implemented with either 3L-H-bridge or 5L-FC-H-bridge sub-module types. This configuration requires the smallest footprint, lowest cost and lowest control complexity compared to the other MMCC types. However it provides the fewest redundant states available for charging and discharging sub-module capacitors, particularly for the 3L-H-bridge. From these considerations, in single star configuration, the 3L-H-bridge sub-module is the best choice for the STATCOM.
- **Single delta MMCC:** this configuration, using 3-level H-bridge, offers smaller footprint and lower control complexity when compared to the double star MMCC with the same type of sub-module. The 3-level H-bridge provides fewer redundant states compared to the 5-level FC H-bridge. It also offers benefits of lower cost, size and control complexity compared to the latter. The 5-level FC H-bridge double star configuration offers more redundancy than its single delta counterpart.
- **Double star MMCC:** This configuration if built with H-bridge sub-modules offers the lowest cost, smallest footprint and lowest control complexity compared to those using the two other types of sub-modules as shown in Table 2.17. Also in comparison with the 5-level FC H-bridge single delta configuration, it requires a smaller footprint and benefits from lower cost. Among the MMCC configurations, the double star using the half bridge is the least attractive for STATCOM application because of its high footprint, cost, and control complexity.

A graphical representation has been designed to show the ranking of MMCCs using different sub-modules in terms of meeting the metrics of assessment. The ranking order is from 8 (best) down to 1 (worst), as shown in the following Table 2.18.

From Figure 2.15, the single star configurations using 3-level H-bridge and 5-level FC H-bridge offer the lowest cost, size, and control complexity among all the MMCC configurations. The reduction in platform size for both sub-module types further reduces the total cost of MMCC-STATCOM. This assessment shows that the choice of a double star configured half bridge sub-modules for STATCOM does not offer any cost benefit.

Table 2.18: Comparison of MMCC types based on 11kV STATCOM

<b>MMCC configuration</b>	<b>Footprint (m<sup>2</sup>)</b>	<b>Cost (£)</b>	<b>Redundancy</b>	<b>Control complexity</b>	<b>Total score</b>
<b>Single star</b>					
<b>3L-H-bridge</b>	8	8	1	8	25
<b>5L-FC H-bridge</b>	7	7	6	7	27
<b>Double star</b>					
<b>3L-H-bridge</b>	6	6	2	6	20
<b>5L-FC H-bridge</b>	4	4	7	5	20
<b>Double star</b>					
<b>2L-half bridge</b>	2	2	4	1	9
<b>3L-FC half bridge</b>	1	1	5	1	8
<b>3L-H-bridge</b>	5	5	4	4	18
<b>5L-FC H-bridge</b>	3	3	8	3	17

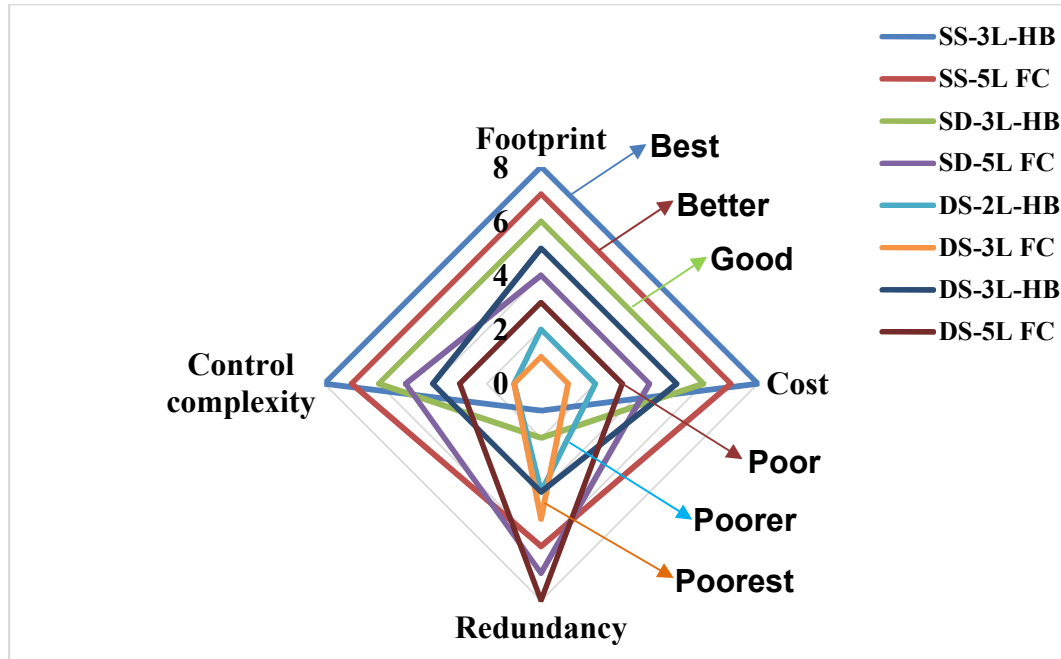


Figure 2.15: MMCC configuration ranking.

## 2.4 Summary

This chapter has presented a detailed analysis and comparison of the various MMCC configurations using four sub-module types, namely the 2-level half bridge, 3-level flying capacitor half bridge, 3-level H-bridge and 5-level flying capacitor H-bridge as applied to a STATCOM. The different sub-module concepts have been described through a quadrant system highlighting their various degrees of freedom. A review of the general classifications of MMCCs namely SSBC-MMCC, SDBC-MMCC, DSBC-MMCC and DSCC-MMCC was given with the various sub-module types applicable to them. For the single cell types, only the H-bridge sub-module types are applicable, while for the double star cell types both half and H-bridge types are applicable for a STATCOM.

The MMCC configurations have been assessed under the metrics of footprint, cost, control complexity and redundancy. The 3-level H-bridge under the single star MMCC provides the lowest footprint, cost, and control complexity, thus making it the best configuration choice for a STATCOM and this shows why it is the preferred choice in the industry. Also, the analysis has shown that the 5-level flying capacitor sub-module single star configuration has better levels of control complexity, size, and cost when compared to the other MMCC configurations. This provides more redundant states, and fewer control feedback loops for capacitor management, than the configurations of the single star, single delta and double star using 3-level H-bridge submodule.

## Chapter 3

### Carrier-Based Sinusoidal PWM Techniques for Flying Capacitor Modular Multi-level Cascaded Converter

PWM techniques are most widely used for voltage source converters including the modular multilevel cascaded converter family. Detailed research has been carried out on various ways of implementing PWM control of the modular multilevel cascaded converters, and several methods have been established; these are phase disposed PWM (PD-PWM), swapped carrier PWM (SC-PWM) and phase shifted PWM (PS-PWM). This chapter investigates the application of these PWM techniques to a three-phase Flying Capacitor Modular Multilevel Cascaded Converter. This comprises two serially connected five-level flying capacitor converter modules, giving nine voltage levels per phase. The fundamental principles and implementation schemes of these PWM schemes are discussed. A contribution of this research is the evaluation of the performance of each PWM method, in terms of natural capacitor voltage balancing, converter power loss, waveform harmonics, and switch utilisation. This has not before been reported and is now discussed in this chapter.

#### 3.1 Performance Metrics for FC-MMCC Modulation Techniques

The circuit diagram of the flying capacitor MMCC used for evaluating the PWM techniques is shown in Figure 3.1. It uses a five-level flying capacitor H-bridge as the basic sub-module, which is formed by connecting two three-level FC half bridges sharing one capacitor  $C_{SM}$ . Further splitting this FC sub-module, there are 4 switch cells; cells 1A and 1B consist of complementary switch pairs  $S_{a1}:S_{a4}$  and  $S_{b1}:S_{b4}$  having  $C_{SM}$  connected across them, while 2A consists of switch pairs  $S_{a2}:S_{a3}$  with inner capacitor  $C_A$  and 2B has switch pair  $S_{b2}:S_{b3}$  and inner capacitor  $C_B$  connected across them. Six such FC sub-modules are used to form a three phase bridge; two are cascaded per phase and the three phase - limbs are connected in a single star configuration.

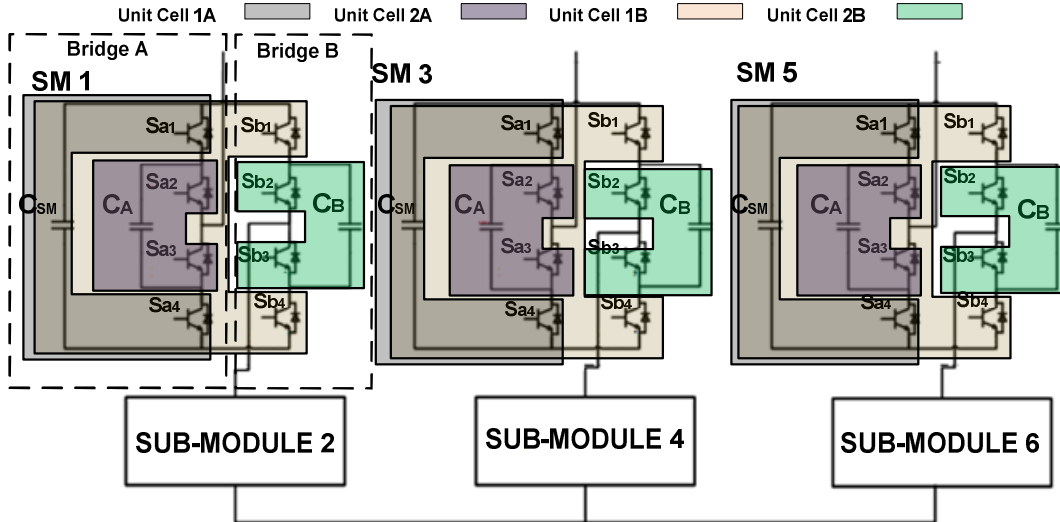


Figure 3.1: FC-MMCC circuit structure [35].

For ease of explanation, the nomenclature described below is applied

- **Unit cell:** this refers to a pair of complementary switches having a capacitor connected across them, such as 1A, 1B, 2A and 2B above.
- **Switching frequency ( $f_s$ ):** this refers to the number of switching transitions per unit cell in a fundamental cycle.
- **Sub-module switching frequency ( $f_{sm}$ ):** this is the number of switching transitions experienced by a sub-module within a fundamental cycle.
- **Equivalent switching frequency:** this is the number of switching steps observed over the multi-level output voltage within a fundamental cycle.
- **Frequency modulation index ( $m_f$ ):** this is the ratio of the switching frequency to the fundamental frequency  $f_o$ :

$$m_f = \frac{f_s}{f_o}. \quad (3.1)$$

- **Amplitude modulation index ( $m_a$ ):** this is the ratio of the desired voltage amplitude to the sum of all sub-module capacitor voltages.

### 3.1.1 Natural Voltage Self-Balancing Ability

Ideally, under steady-state conditions by PWM control, the inner capacitor voltages of the FC-MMCC should be self-balanced. This is achieved by having the converter cell capacitors exchange zero net active power with the ac side over one or several fundamental cycles. However, the net charges of the inner flying capacitor voltages may not be zero over one or several cycles of operation, causing voltage deviations or drift, which is rephrase as follows:



- **Capacitor voltage drift:** this phenomenon occurs when the current magnitudes and durations of charging and discharging of the inner capacitor are unequal, resulting in the real capacitor voltage moving systematically away from its nominal value over a number of fundamental cycles.
- **Capacitor voltage deviation:** this more rapid voltage cycling is due to the inner flying capacitor balanced charging and discharging within one fundamental period. Its magnitude depends on the inner flying capacitance and the switching pulses synthesized by the modulation scheme.

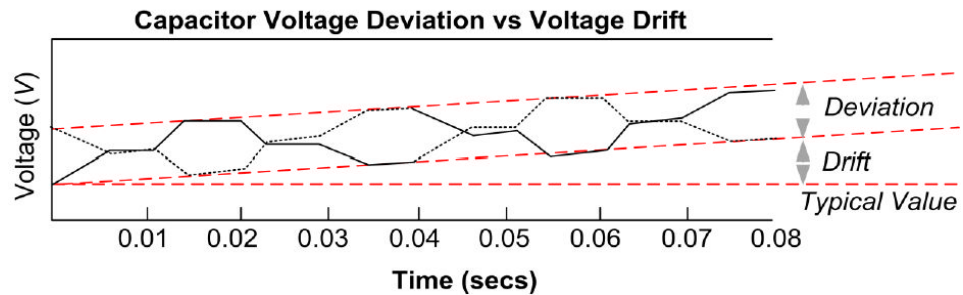


Figure 3.2: Graphical illustration of capacitor voltage drift and variation [35].

Natural voltage balancing of inner flying capacitors, i.e.  $C_A$  and  $C_B$ , is an important attribute for evaluating PWM schemes for FC-MMCC. An ideal PWM technique should enable inner flying capacitor voltages to be self-balanced under open-loop mode with no capacitor voltage measurement. This means that the mean current flowing in all capacitors is zero under steady-state conditions, giving zero voltage drift. Inner capacitor voltage with minimum deviation and zero drift minimises harmonic distortion of the inverter output voltage and reduces capacitance.

### 3.1.2 Power Loss

Power losses of an MMCC are mainly due to the conduction and switching losses of the switching devices (power transistors and diodes). Two methods have been applied for calculating them. One uses a mathematical model of the current waveform in each switch [149] and the other an average model based on piecewise linear characteristics of semiconductor devices obtained from the manufacturer's datasheet. In this research, the losses are evaluated as not only depending on the instantaneous current through the switches and but also on the instantaneous junction temperature of each device. Losses due to flying capacitor equivalent series resistance (ESR) are also included.

### 3.1.2.1 Conduction loss

This is the loss due to the on-state voltage drop of a semiconductor switching device when current flows through it (i.e. during its conduction period) [150, 151]. Conduction losses can either be evaluated through simulations which are fed with precise curve-fit data for the device on-state voltage as a function of current [149, 152] or by an analytical method using a piecewise linear approximation to the same current-voltage characteristics to compute average conduction losses [153, 154]. Using the analytical method, the on-state voltage drop is expressed as:

$$V_{cond}(i_{cond}) = V_o + R_{ON} \cdot i_{cond} \quad (3.2)$$

where  $V_{cond}$  is the forward voltage drop,  $R_{ON}$  is either the IGBT ( $R_{ON\_CE}$ ) collector emitter on-state resistance or diode ( $R_{ON\_D}$ ) on-state resistance,  $V_o$  denotes either the IGBT ( $V_{CEO}$ ) zero current collector-emitter voltage or diode ( $V_{FO}$ ) zero current forward voltage and  $i_{cond}$  is the instantaneous value of converter phase current through the device and it is denoted  $i_c$  for an IGBT and  $i_f$  for a diode. This method only considers the semiconductor device characteristics through a linear relationship without taking into consideration their junction temperature. For this analysis (3.2) is simplified as a function of current and device junction temperature which is expressed as [155]:

$$V_{cond}(t) = f_{cond}(i_{cond}(t), T_j(t)). \quad (3.3)$$

The conduction energy loss,  $E_{cond}$ , for either an IGBT or a diode within a switching period  $t_o$ - $t$  is expressed as;

$$E_{cond} = \int_{t_0}^t i_{cond}(t) \cdot V_{cond}(t) dt. \quad (3.4)$$

The average conduction power losses across a semiconductor device is a function of both switching frequency  $f_s$  and  $E_{cond}$  and is expressed as:

$$P_{avg\_cond} = f_s \cdot E_{cond} \quad (3.5)$$

where  $P_{avg\_cond}$  can be written as either  $P_{avg\_condT}$  (IGBT) or  $P_{avg\_condD}$  (diode) respectively.

Thus the total conduction loss across a switch is expressed as:

$$P_{cond} = P_{avg\_condT} + P_{avg\_condD} . \quad (3.6)$$

### 3.1.2.2 Switching loss

The switching power losses are due to the finite time taken for a semiconductor device to change from on to off states and vice versa. These power losses are dependent on the load current, the voltage across the switch, and the switching frequency [151, 156-162]. It is impractical to evaluate switching power losses using sampled data over such a short switching interval which normally ranges from a few nanoseconds to fractions of a microsecond. In this research, the switching losses are accounted for by evaluating an energy impulses after each turn on and turn off events, and they depend mainly on the current through the IGBT and diode and their respective junction temperatures. Thus, the switching loss  $P_S$  is calculated as:

$$P_S = f_S (E_{s\_ON} + E_{s\_OFF}) \quad (3.7)$$

where  $E_{S\_ON}$  is the IGBT turn on energy loss,  $E_{S\_OFF}$  is the IGBT turn off energy and reverse recovery diode loss. And are defined as:

$$E_{s\_ON} = f_{S\_ON}(i_c(t), T_{j-T}) \cdot \left( \frac{V_{CE}}{V_{CE\_Ref}} \right) \quad (3.8)$$

$$E_{s\_OFF} = f_{S\_OFF}(i_c(t), T_{j-T}(t)) \cdot \left( \frac{V_{CE}}{V_{CE\_Ref}} \right) + f_{S\_OFF}(i_F(t), T_{j-D}(t)) \cdot \left( \frac{V_F}{V_{F\_Ref}} \right) \quad (3.9)$$

where  $f_{S\_ON}$  and  $f_{S\_OFF}$  are the switching energy functions for turn-on and turn-off energies.

$T_{j-T}$  and  $T_{j-D}$  are respectively the junction temperatures of IGBT and diode  $V_{CE\_Ref}$ ,  $V_{F\_Ref}$  are the reference voltages for IGBT and diode switching losses derived from their respective data sheets.

### 3.1.2.3 Flying capacitor loss

Losses in the flying capacitors of the FC-MMCC are accounted for by the products of their internal equivalent series resistance (E.S.R)  $R_{Cap}$  and the current flowing through them during both charging and discharging periods [155]. The capacitor energy loss  $E_{cap}$  is expressed as:

$$E_{cap} = \int_{t_0}^t C^2 \left( \frac{dv}{dt} \right)^2 \cdot R_{Cap} dt \quad (3.10)$$

For the FC sub-module flying capacitors, such as  $C_A$  and  $C_B$  in Figure 3.1, either a charge or discharge transition occurs between a time interval  $t_0 - t$ . The average power loss within this time interval is expressed as:

$$P_{avg\_cap} = f_S \cdot E_{cap} \quad (3.11)$$

### 3.1.2.4 A Power Loss Estimation Algorithm

The total power loss for a switching device can be estimated by combining the conduction and switching losses evaluated separately using the equations already described in the previous subsections. However, in this research, a more accurate loss estimation algorithm is applied. This uses the IGBT characteristic curves between  $I_C$ ,  $T_{j-T}$  and  $V_{CE}$ , as shown in Figure 3.3(a), which is given in the device data sheet [29]. According to device measured current and temperature values these curves, embedded in the power loss calculation model as a look-up table, give the device on-state voltages  $V_{CE}$ . Likewise, the characteristic curves for diode forward voltage  $V_F$  are also embedded as a look-up table in the model. As illustrated in Figure 3.3(a), these tables enable  $V_{CE}$  and  $V_F$  evaluations at two different device junction temperatures ( $125^{\circ}\text{C}$  and  $150^{\circ}\text{C}$ ). Voltage values which are not given in these tables are estimated by interpolation. These obtained values are then used to evaluate device conduction losses using equations (3.4)-(3.6). For switching power loss calculation characteristics curves of IGBT switching energy losses, shown in Figure 3.3(b), is used. Applying different values of device current and voltage, these curves give  $E_S$  for IGBT at the same two junction temperatures as that for conduction loss. These curves are also embedded as a set of look-up tables. The next procedure following  $E_S$  evaluation calculates switching loss using equation (3.7).

A thermal circuit model is used for evaluating the device instantaneous temperature  $T_j$ . This applies the average power loss values obtained for each device, and the device thermal impedance. According to device data sheet, the device thermal impedance values considered include a junction to case ( $R_{thJC}$ ), case to heat sink ( $R_{thCH}$ ), and heat sink to ambient ( $R_{thH}$ ) impedance as seen in Appendix B1. Figure. 3.4(a) shows the structure of the thermal circuit model for a device pack consisting of a diode and an IGBT.

Based on the above-described procedure, a power loss evaluation algorithm is derived aggregating both conduction and switching losses over a fundamental cycle for each IGBT and diode. Using measured device current this algorithm works iteratively in evaluating converter total power loss in real time operation. The procedure of this evaluation algorithm is listed below;

- The device junction temperature is initially set to the measured ambient temperature value.
- Individual device on state voltage  $V_{CE}$  or diode forward voltage  $V_F$  are estimated using their current (either  $I_C$  or  $I_F$ ) and junction temperatures.
- Device switching energies are calculated using their look-up table.

- Both on state voltage and switching energies are applied in calculating either diode  $P_{Total D}$  or IGBT power losses  $P_{Total T}$ .
- Device power losses are fed into the thermal circuit model in evaluating their corresponding device junction temperature.

With the newly evaluated temperature values, the iteration process completes and returns to the beginning to calculate the new power loss values. This process repeats until the device junction temperature and power loss values settle to constants. The algorithm has been applied to assess the efficiencies of an MMCC under different PWM schemes and will be described in the preceding subsections. Figure 3.4 (b) shows the algorithm which is applied to a simulated FC-MMCC.

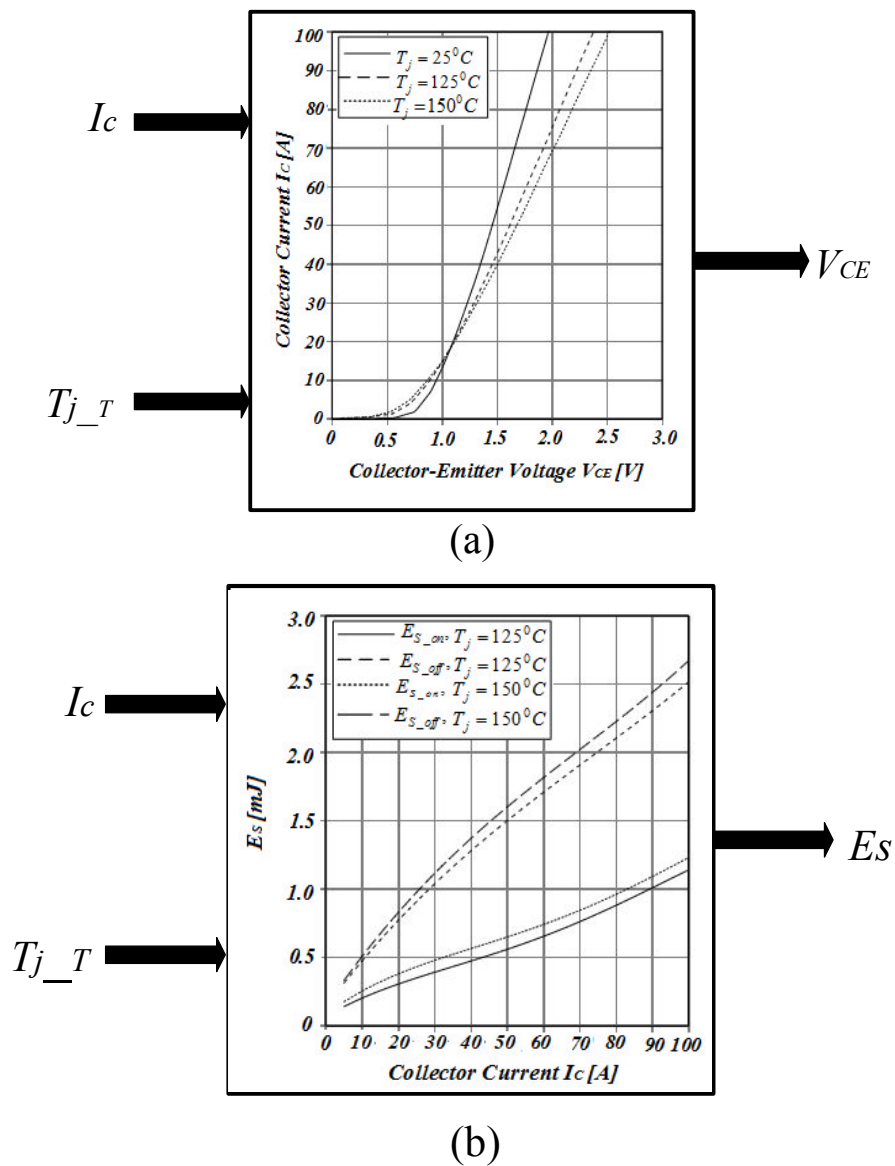
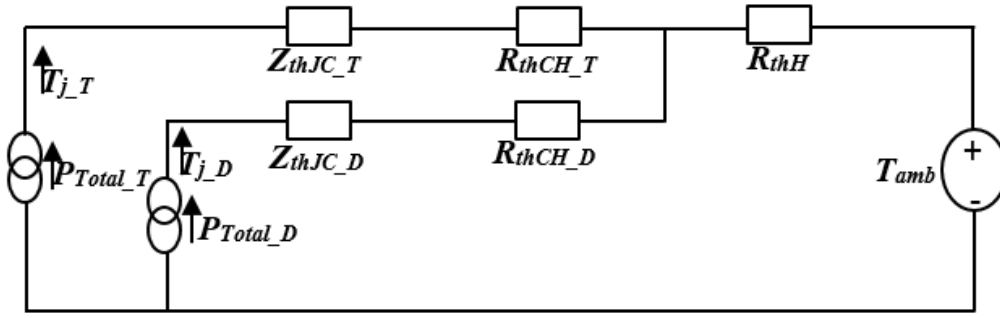
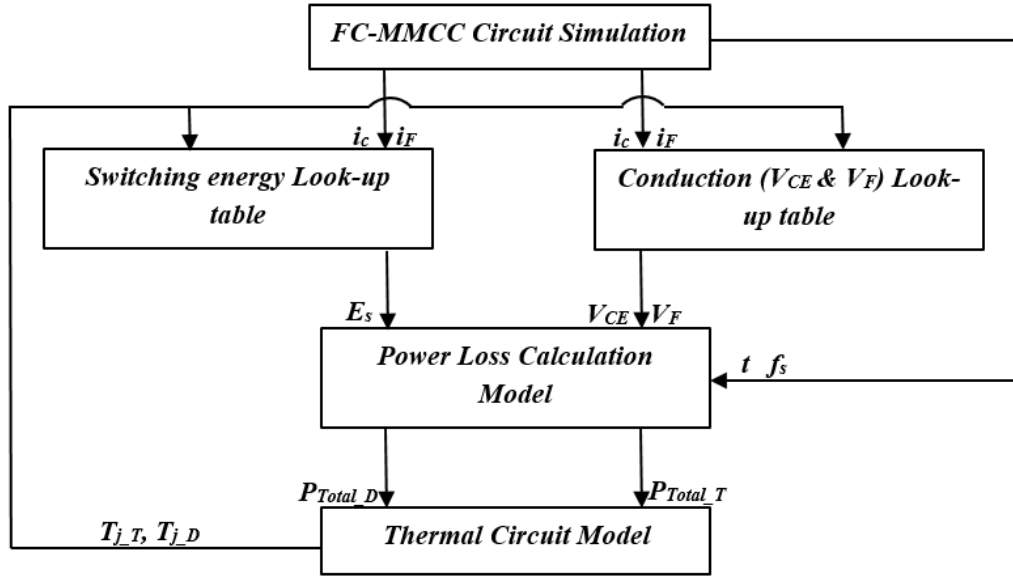


Figure 3.3: Characteristic curves for (a)  $i_c$  and  $T_{j\_T}$  vs  $V_{CE}$  and (b)  $i_c$  and  $T_{j\_T}$  vs  $E_s$ .



(a)



(b)

Figure 3.4: (a) Thermal and (b) loss evaluation model for an FC-MMCC.

### 3.1.3 Total Harmonic Distortion (THD)

This metric is used to assess the output voltage waveform performance. The THD of a voltage waveform primarily depends on the PWM methods used and switching frequency and is defined as:

$$THD = \sqrt{\sum_{n=2,3,\dots} \left(\frac{V_n}{V_1}\right)^2} \quad (3.12)$$

where  $V_1$ , and  $V_n$  refer to the *rms* values of the fundamental and *n*th harmonic component present in the converter output voltage. For this analysis, the unipolar switching method is applied to all PWM methods tested.

### 3.1.4 Sub-module Switch Utilization

This metric is used to investigate the switches within a sub-module that are evenly or unequally stressed/utilized over a fundamental period. This implies

that if some switches are more stressed within a sub-module, these switches will be more prone to failure.

### 3.2 Carrier Placement PWM Techniques

Detailed research has been carried out over the years on the carrier placement-based pulse width modulation techniques for multilevel converters [51, 163-169]. In principle, this compares triangular carrier signals with sinusoidal reference signals, the obtained switching pulses which synthesize the reference signals are applied to control the converter switches [164].

The choice of a carrier placement strategy depends on the requirement of the application. These carrier placement modulation techniques can broadly be grouped into two namely; the vertical and horizontal placement techniques. The former has multiple triangular carrier waves displaced along the voltage axis at different voltage levels, each relates to a complementary switch pair. There are in general three such methods; phase disposition PWM (PD-PWM), phase opposition disposition PWM (POD-PWM) and alternative phase opposition disposition PWM (APOD-PWM). For the horizontal carrier placement schemes, multiple triangular carrier waves are displaced along the horizontal (time or phase angle) axis from each other with equal phase shifts. All these techniques have been discussed in detail by Holmes et al [165].

In this section, the PD-PWM, swapped carrier PWM, and PS-PWM applied to control the FC-MMCC are discussed and compared below.

#### 3.2.1 Phase Disposed PWM (PD-PWM)

This also called the level shift PWM, involves displacing the triangular carriers vertically according to the voltage levels. The number of the triangular carriers used is determined by the number of distinct voltage levels minus 1 and for the five level FC-MMCC example used in this research, four triangular carrier signals are used. The four level-shifted carriers are all in phase and equally spaced from -1 to +1. They are compared with two reference signals which are phase shifted by  $180^\circ$  and with the same magnitudes and frequency. The PD-PWM scheme implemented for phase A of the FC-MMCC is illustrated in Figure 3.5. The four carrier signals are compared with two sinusoidal reference signals with their respective magnitudes  $+V_{ref}$  and  $-V_{ref}$ . Frequency modulation index  $m_f=15$ , and amplitude modulation index  $m_a=0.8$  are applied. The resultant pulse signals, as shown in Figure 3.5, are applied to control eight complementary switch pairs in the two chained FC sub-modules. The first two (red and orange) are for two left limb switch pairs  $S_{a1}:S_{a4}$  and  $S_{a2}:S_{a3}$  in sub-module 1. The second two (green and blue) are to fire the same left-limb

switch pairs in sub-module 2. The third pair and fourth pair of pulse signals fire switch pairs.  $S_{b1}:S_{b4}$  and  $S_{b2}:S_{b3}$  on the right-hand-side limbs of sub-modules 1 and 2.

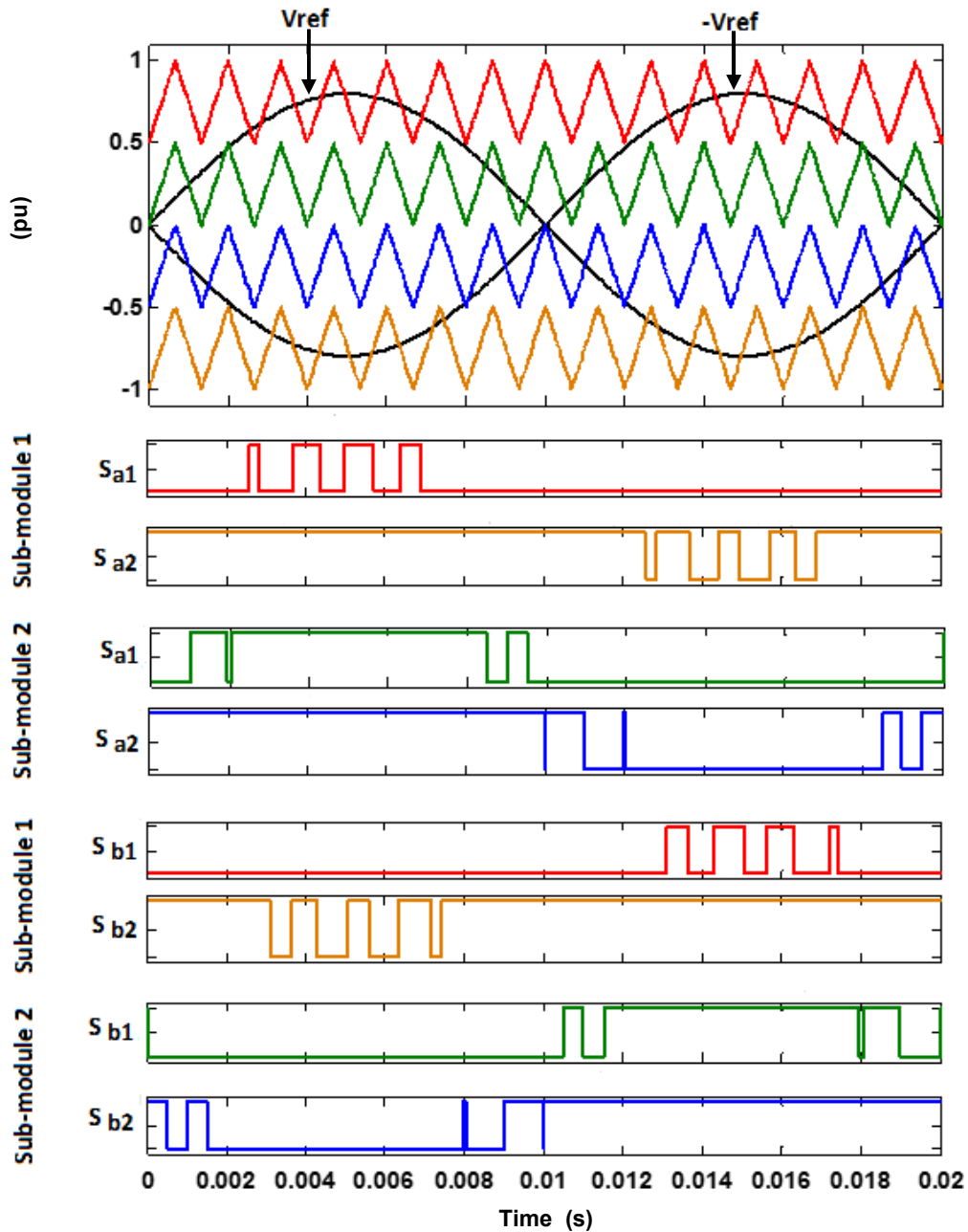


Figure 3.5: Phase disposed PWM for FC-MMCC at  $m_f = 15$ .

### 3.2.1.1 Natural Voltage balancing ability

The inner flying capacitor voltage natural balancing ability of the FC-MMCC under steady-state is investigated when controlled by the above PD-PWM switching signals. The voltage waveforms of these capacitors in sub-modules 1 and 2 and their corresponding switching signals as illustrated in Figure 3.6 are used for this analysis.



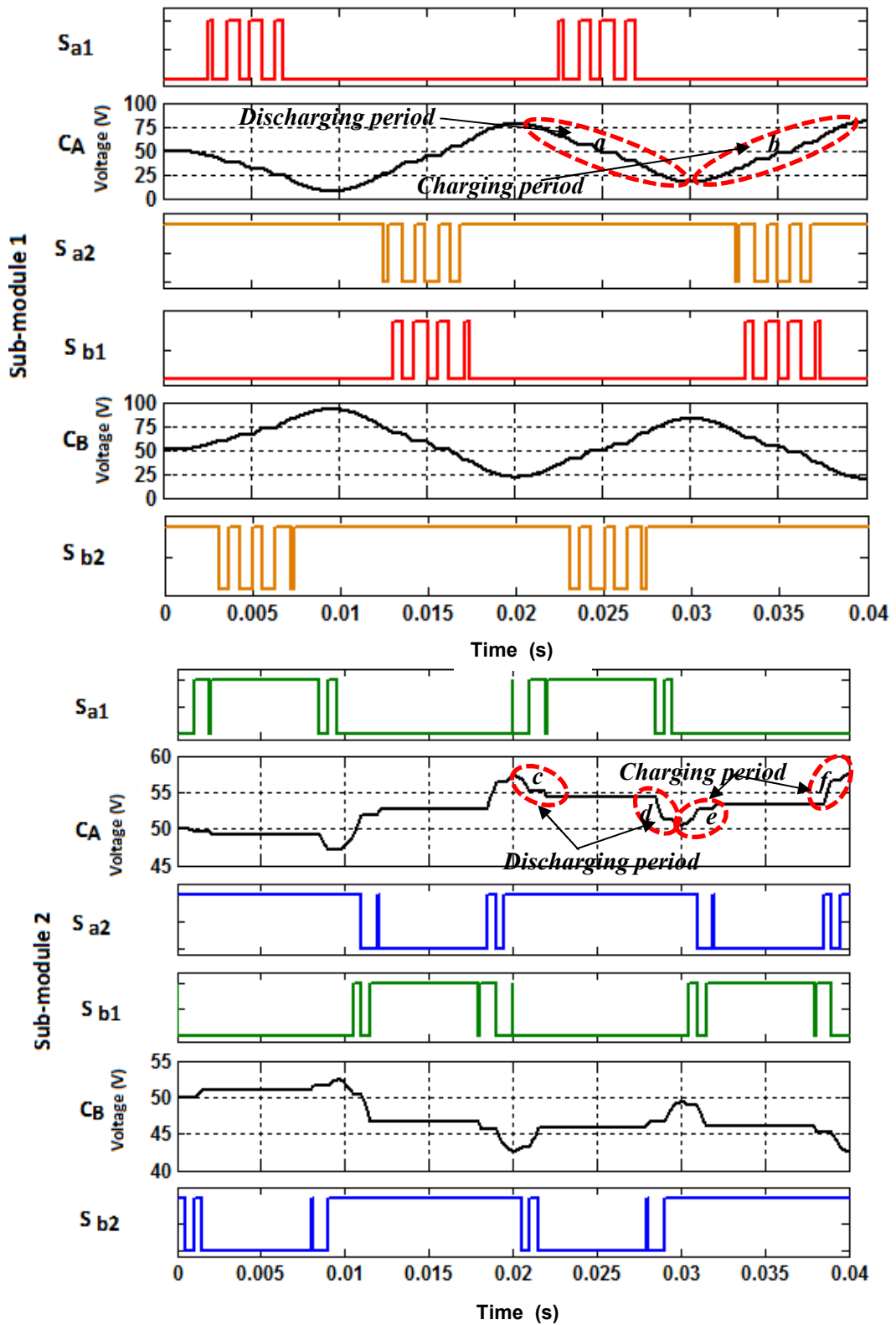


Figure 3.6: PD-PWM switching actions for investigating sub-module flying capacitor variation.

As observed from waveforms in this figure, starting from voltage = 50V, the inner flying capacitors in both sub-modules experience equal charging and discharging durations, For example for sub-module 1, voltage falling interval *a* equals voltage rising duration *b*, while for sub-module 2, voltage falling

interval  $c$  and  $d$  equals voltage rising period  $e$  and  $f$ . Thus resulting in zero voltage drift over every fundamental cycle. However, the voltage deviation across each FC sub-module differs. This is accounted for by the switching actions of ( $S_{a1}:S_{a2}$  and  $S_{b1}:S_{b2}$ ) switches in each sub-module. For sub-module 1, the mean voltage deviation is about  $\pm 70\%$  because over each half fundamental cycle, the pulses applied across  $S_{a1}=0$ ,  $S_{a2}=1$  has longer durations which discharges and charges  $C_A$  in each half of the fundamental cycle. Whilst for sub-module 2, both  $C_A$  and  $C_B$  experience mean voltage deviation of about  $\pm 8\%$ , which is attributed by ( $S_{a1}:S_{a2}$  and  $S_{b1}:S_{b2}$ ) switches having shorter durations of charging and discharging states compared to longer periods when both switches are high (i.e.  $C_A$  and  $C_B$  are bypassed) over each fundamental cycle.

As a result of the large Flying capacitor voltage variation in sub-module 1, the spectral quality of the output voltage waveform will be adversely affected. The performance of natural voltage balancing of the flying capacitors makes this PWM method undesirable for some applications.

### **3.2.1.2 Power losses**

#### ***Conduction loss***

As observed from Figure 3.7, modulation index affects both IGBT and diode conduction losses in different ways, i.e. when  $m_a$  increases, the conduction periods of the IGBTs increase, while those of the diodes reduce (see Figure 3.8(a)). Therefore, the ratio of the diode to IGBT conduction losses decreases as  $m_a$  increases (see appendix B2). It is also observed that, for the same reference magnitude, increasing the switching frequency has no impact on the conduction loss occurring in the IGBTs and diodes. As illustrated in Figure 3.8(b), the conduction losses for the same  $m_a$  at carrier frequencies  $f_s=0.75$  kHz, 1.5 kHz and 3.0 kHz are the same.

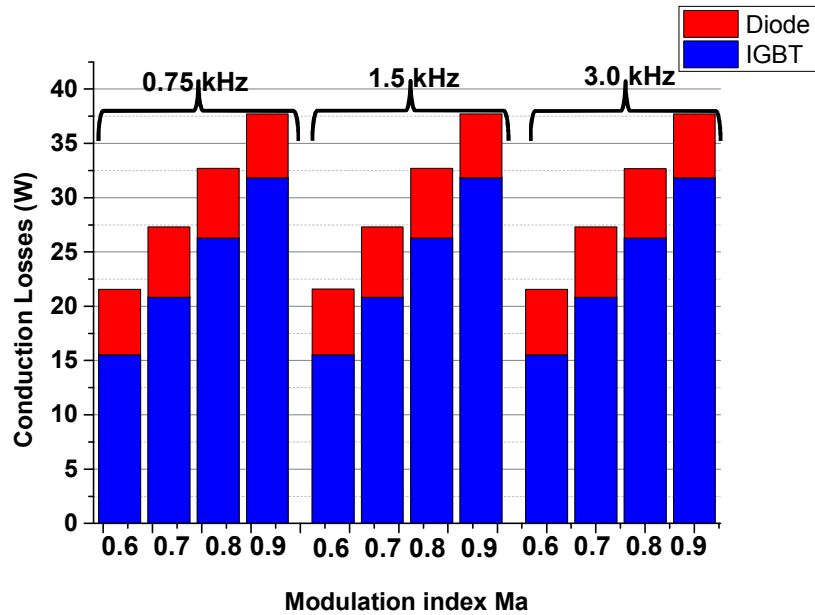


Figure 3.7: IGBT and Diode conduction losses.

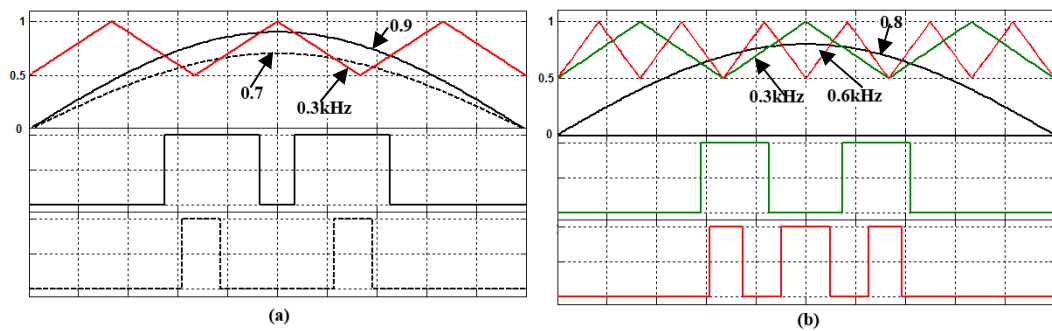


Figure 3.8: (a) variation in reference signal  $m_a$ ; (b) variation in carrier signal frequency.

**Switching loss**

As observed in Figure 3.9, FC-MMCC switching loss increases as switching frequency increases. The number of switching transitions increases by a factor of 2 as the switching frequency increases from 0.75 kHz to 1.50 kHz (see Figure 3.8(b)). Also, as modulation index increases for a fixed switching frequency, the number of switching transitions remains the same, see Figure 3.8(a). The diode switching loss is nearly about 25% of the IGBT switching loss as seen in Figure 3.9.

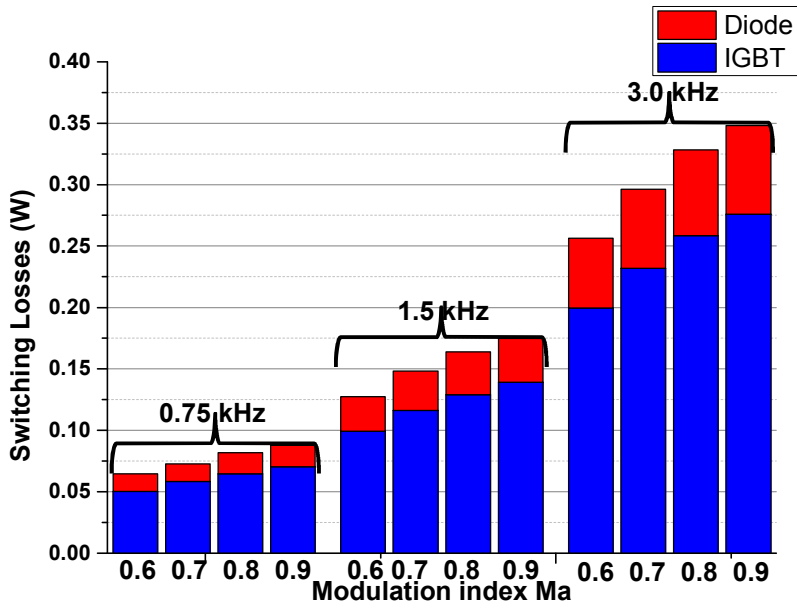


Figure 3.9: IGBT and Diode switching loss.

### ***Flying Capacitor losses***

Due to the difference in voltage deviations between the inner flying capacitors of sub-modules 1 and 2, the power dissipations in both are unequal as seen in Figure 3.10. It can be seen that the area of the charge/discharge region of each sub-module inner capacitor (see Figure 3.6) has a direct relationship with the power loss shown (see appendix B4).

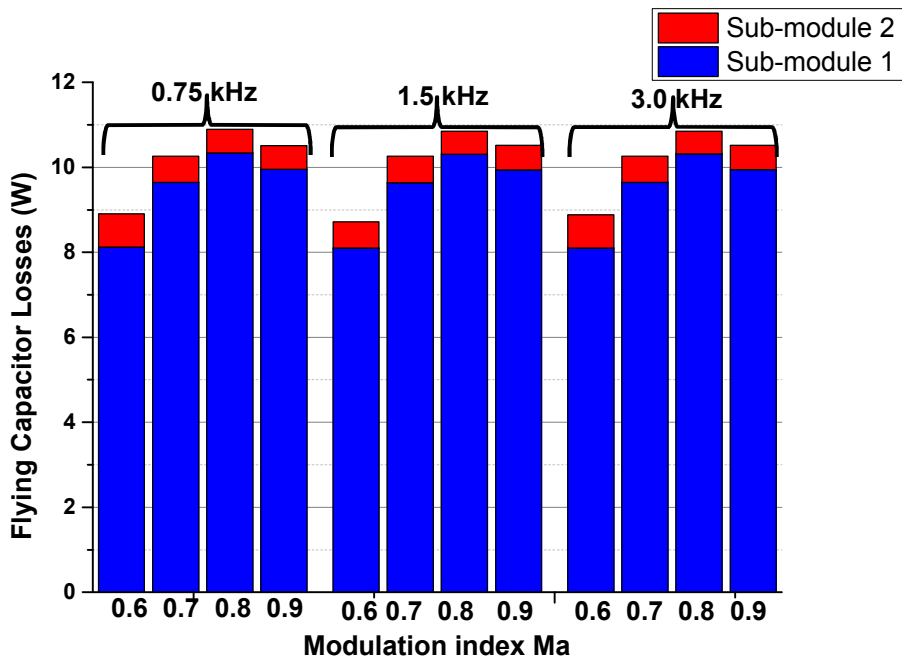


Figure 3.10: Flying capacitor loss.

### Total loss

As observed from Figure 3.11, as  $m_a$  increases, the total power loss increases, which is mainly contributed by IGBT conduction losses. Likewise, increase in total loss is only accounted for by the IGBT and diode switching losses as switching frequency increases. In addition, the power loss contribution of the IGBTs, diodes and inner floating capacitors with respect to the total loss are 60%, 15% and 25% respectively.

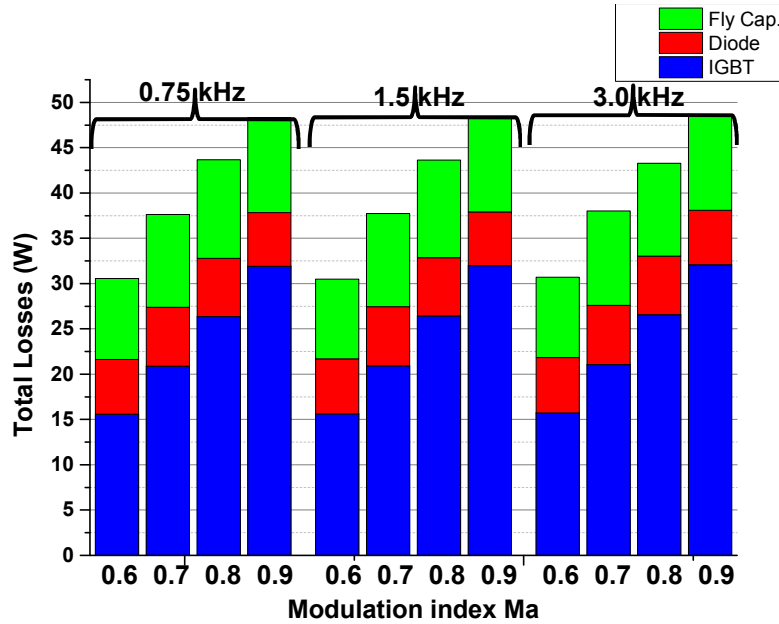


Figure 3.11: Total Losses.

#### 3.2.1.3 Total harmonic distortion (THD) analysis

In analysing the spectrum quality of the FC-MMCC output voltage, the Fourier series of the instantaneous voltage signal  $v(t)$  generated by the carrier placement scheme is used [165]. This is expressed as:

$$\begin{aligned}
 v(t) = & \underbrace{\frac{a_{00}}{2}}_{1^{st} \text{ Term (DC offset)}} + \underbrace{\sum_{n=1}^{\infty} [a_{0n} \cos(n(\omega_0 t + \phi_0)) + b_{0n} \sin(n(\omega_0 t + \phi_0))]}_{2^{nd} \text{ Term (Fundamental + Baseband harmonics)}} \\
 & + \underbrace{\sum_{m=1}^{\infty} [a_{m0} \cos(m(\omega_c t + \phi_c)) + b_{m0} \sin(m(\omega_c t + \phi_c))]}_{3^{rd} \text{ Term (Carrier harmonics)}} \\
 & + \underbrace{\sum_m \sum_n \left[ \begin{aligned} & a_{mn} \cos(m(\omega_c t + \phi_c) + n(\omega_0 t + \phi_0)) \\ & + b_{mn} \sin(m(\omega_c t + \phi_c) + n(\omega_0 t + \phi_0)) \end{aligned} \right]}_{4^{th} \text{ Term (Sideband harmonics)}}
 \end{aligned} \tag{3.13}$$

where  $a_{00}$  represents the amplitude of the DC offset and should always be zero for all modulation strategies investigated in this chapter.

$a_{0n}$  and  $b_{0n}$ , are for reference fundamental component and its harmonics with index  $n$ , and often refer as the baseband harmonics.  $a_{m0}$ ,  $b_{m0}$  and  $a_{mn}$ ,  $b_{mn}$  represent the amplitudes of carrier and sideband harmonic components, where  $n$  and  $m$  represent the index variables for the baseband and carrier harmonics.

$\omega_0 = 2\pi/T$  and  $\omega_c = 2\pi/T_c$  are the reference and carrier signal angular frequencies,  $\phi_0$  and  $\phi_c$  phase shifts of the reference and carrier signals.

According to (3.13), the first DC offset term is zero, the second term represents the fundamental component surrounded by baseband harmonics. For the carrier placement method, all baseband harmonics before the equivalent carrier switching frequency are totally suppressed except the fundamental signal. The third term is the harmonic element at carrier signal frequency and its multiples. The fourth term represents the sideband harmonics resulting from the difference between the carrier and baseband harmonic components.

For this modulation method, it ideally gives good harmonic performance when three-level H-bridge sub-modules are used. However if using the five-level FC H-bridge sub-modules, the flying capacitor voltages deviate too far from their nominal values causing poor spectral quality of the output voltage waveform. Figure 3.12 shows the ideal phase and line-line voltage waveforms with  $m_a=0.8$  and  $m_f=15$ . From the harmonic spectrum of the phase voltage shown in Figure 3.13(a), it can be seen that all baseband harmonics and harmonics at twice the switching or carrier frequency and its multiples are suppressed except the fundamental and sideband harmonics due to the unipolar switching. These sideband harmonics frequencies are expressed as:

$$f_h = h \times f_o = ((j2m_f) \pm k) f_o \quad (3.14)$$

where  $j=1, 2, 3, \dots$   $k=1, 3, 5, \dots$  odd number,

The total harmonic distortion of the phase voltage waveform is 12.10%. From the Figure 3.13, the first sidebands before and after the  $2m_f$  are evaluated using (3.14) as:

$$f_{29} = (2 \times 15 - 1) \times 50 = 1450 \text{ Hz}, \quad f_{31} = (2 \times 15 + 1) \times 50 = 1550 \text{ Hz} \quad (3.15)$$

Likewise, for the line voltage spectrum, all the 3<sup>rd</sup> order harmonics are suppressed and the sideband harmonics appear around the even multiples of  $m_f$ . The total harmonic distortion for the line voltage waveform is 9.25% as illustrated in Figure 3.13 (b).

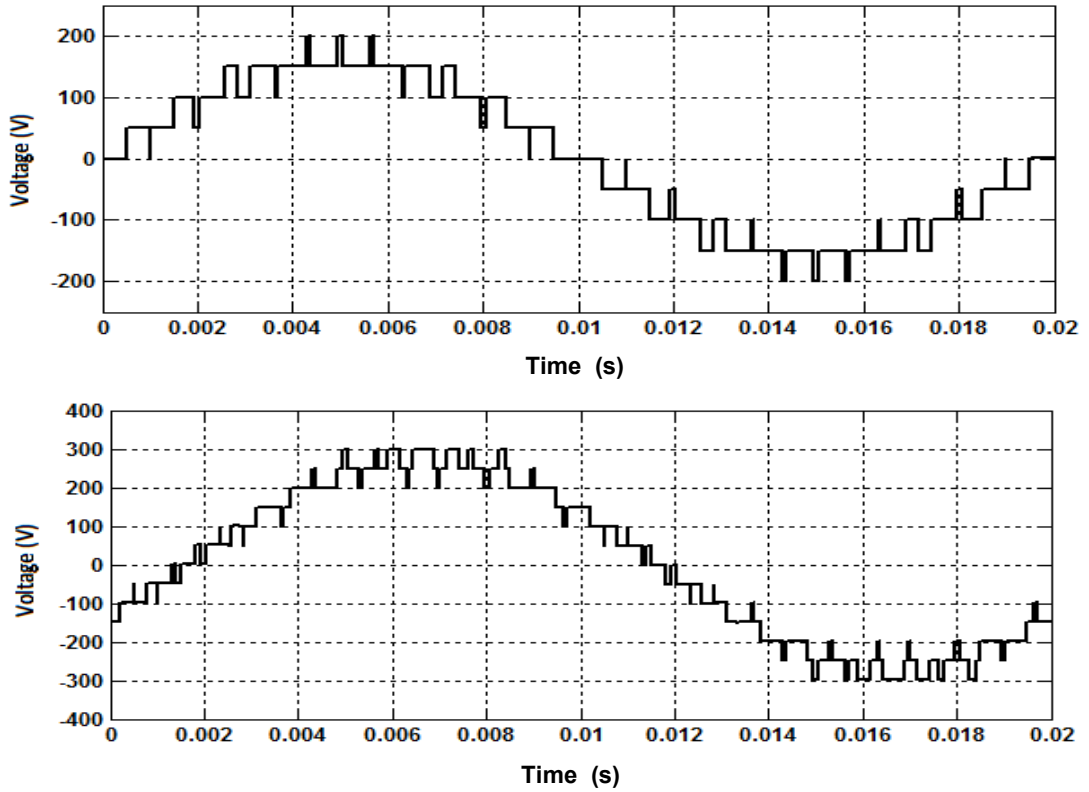


Figure 3.12: (a) Phase voltage waveform, (b) Line-line voltage waveform.

The harmonic order for the line voltage spectrum can be expressed using 3.13 but with  $j=1, 2, 3 \dots k=1, 5, 7 \dots$  odd numbers excluding multiples of 3.

However using PD-PWM to control a nine-level FC-MMCC, the phase and line voltage spectra as shown in Figure 3.15 (a) and (b), has some baseband harmonics around the fundamental. These are introduced by the large voltage deviation of the flying capacitors  $C_A$  and  $C_B$  of sub-module 1, hence creating distortions on the output voltage waveform having a THD of 17.86%. The sideband harmonics (i.e. for both phase and line voltage spectra) appear around the carrier frequency as shown in Figure 3.15. Figure 3.16 illustrates a 3-D plot of phase voltage THD as a function of modulation frequency and amplitude modulation index. As expected, THD reduces drastically as  $m_a$  increases, while it reduces slightly when  $m_f$  increases.

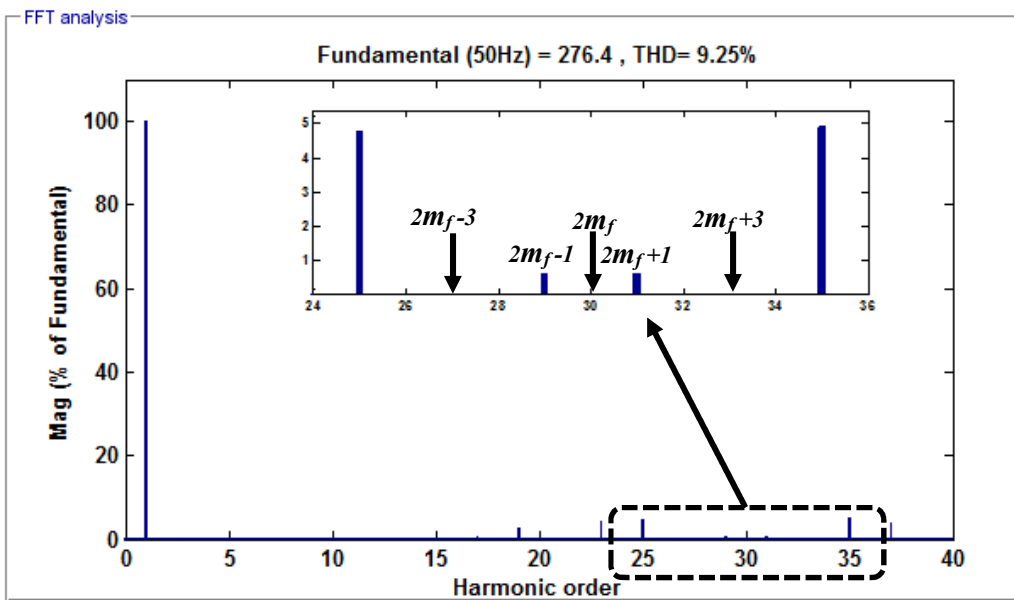
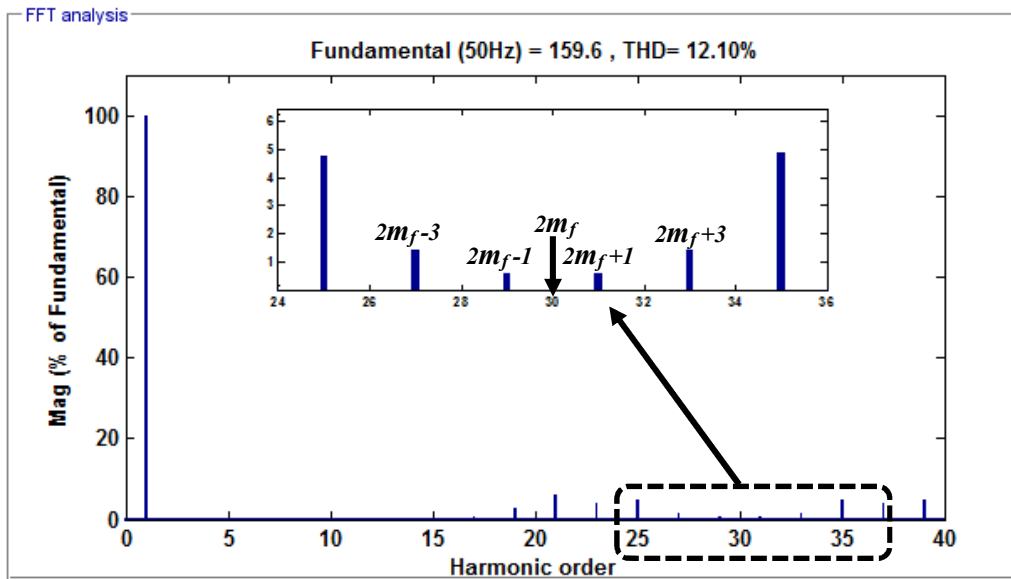


Figure 3.13: (a) Phase voltage spectrum, (b) Line voltage spectrum.



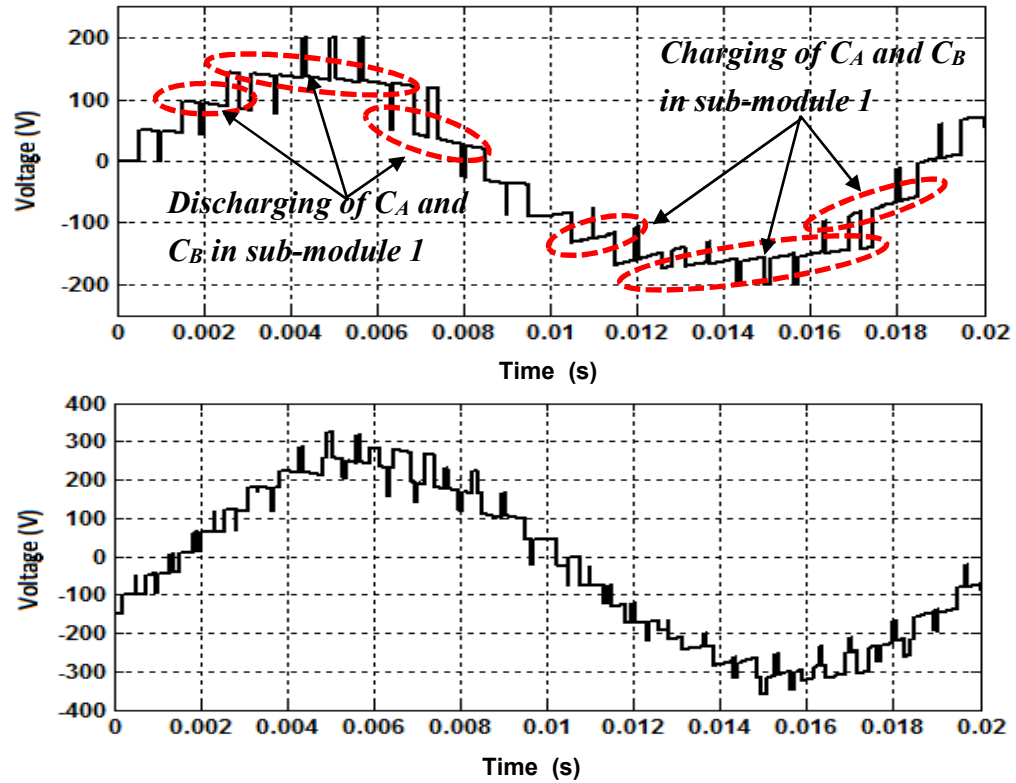


Figure 3.14: (a) Phase voltage of the FC-MMCC (highlighting the intermediate voltage levels that are contributing to the distortion of voltage waveform) and (b) Line voltage.

### 3.2.1.4 Sub-module switch utilization

It is seen from Figure 3.5, that the conduction periods are different for each sub-module switch, and hence the conduction losses are different for different switches. From Figure 3.17, switches  $S_{a1}$ ,  $S_{a3}$  show less conduction loss than  $S_{a2}$ ,  $S_{a4}$ . This uneven switch utilization across the five-level FC sub-module affects the charging and discharging of the sub-module capacitors, making this topology unattractive for active power filtering and FACTS application. The unequal utilization also results in uneven heat distribution across sub-module switches.

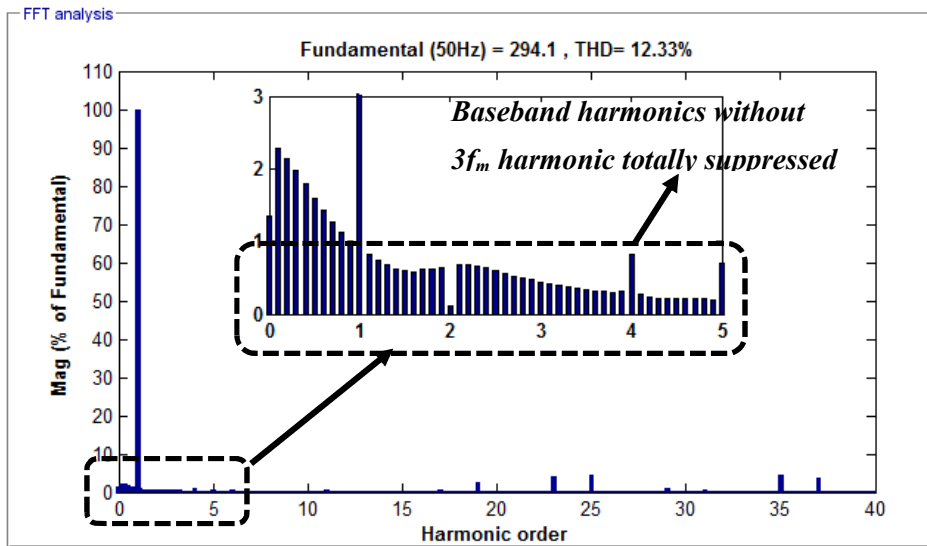
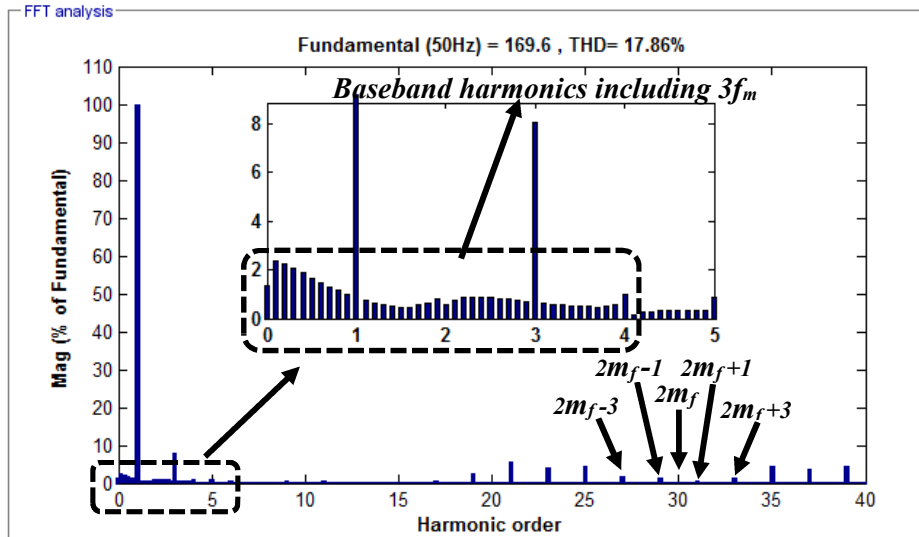


Figure 3.15: (a) Phase and (b) line voltage spectra.

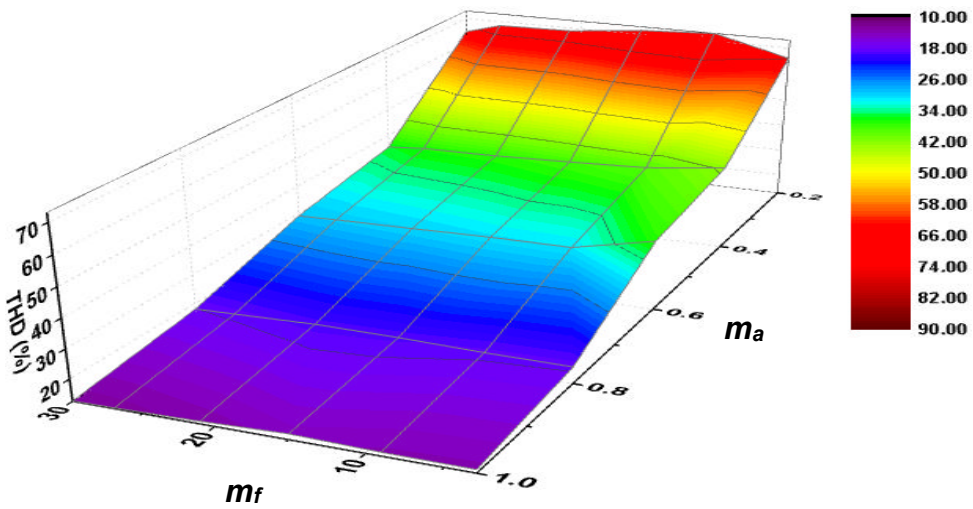


Figure 3.16:3-D plot of Total harmonic distortion as a function of  $m_a$  and  $m_f$ .

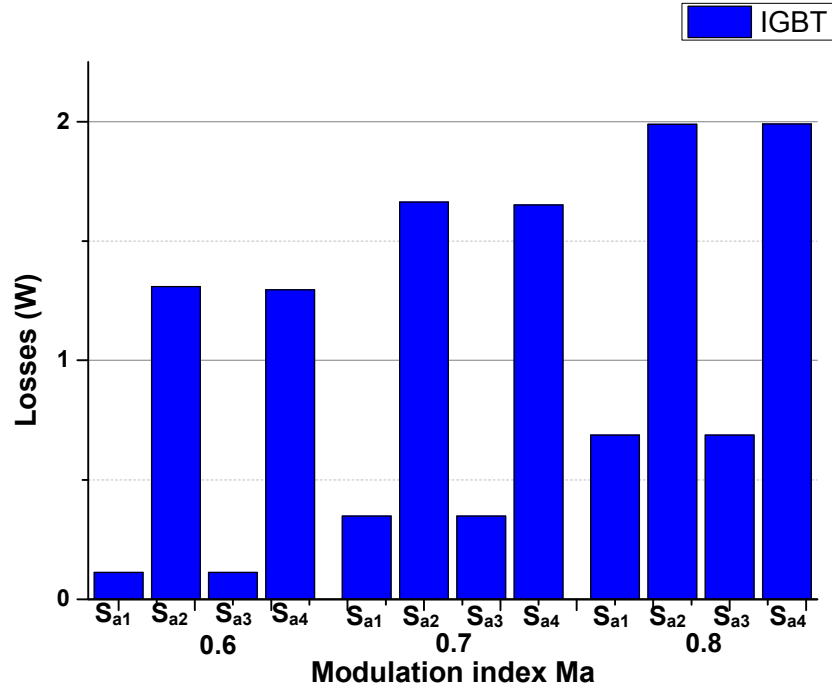


Figure 3.17: Sub-module Switch utilization conduction losses.

### 3.2.2 Swapped Carrier PWM (SC-PWM)

To handle the shortcomings of the PD-PWM technique when applied to FC-MMCC, a new modulation technique known as swapped or rotational carrier PWM was developed. In this method, the level of the carrier signals are rotated in an orderly manner either at the end of each quarter fundamental cycle or at the end of each carrier wave cycle. These distinct swapping patterns are referred to as method 1 and method 2.

With the two anti-phase modulating signals compared with four carrier signals, carrier signals 1 and 2 control complementary pair ( $S_{a1}:S_{a4}$ ,  $S_{b1}:S_{b4}$ ) and ( $S_{a2}:S_{a3}$ ,  $S_{b2}:S_{b3}$ ) and in sub-module 1 while carrier signals 3 and 4 are for switches in sub-module 2. A modulation frequency index  $m_f=15$  is applied.

#### 3.2.2.1 Method 1 - Quarter fundamental cycle rotation

Figure 3.18 shows this method. The colour code in Figure 3.5 (PD-PWM) is maintained for reference. Here the two carriers, (Red and Green) that lie above x – axis and intersect with the positive reference  $+V_{ref}$ , are dedicated for sub-module 1 Left-Hand-Side (LHS) switches  $S_{a1}:S_{a4}$  and  $S_{a2}:S_{a3}$ . They interchange their vertical positions after every quarter of the reference signal cycle ( $T_m/4$ ). The other two carriers (Blue and Brown) lying below the x – axis, and also intersecting with  $+V_{ref}$ , are for sub-module 2 LHS switches  $S_{a1}$  and  $S_{a2}$  and change positions at the same quarter cycle instants. This procedure

is also applied to control sub-modules 1 and 2 RHS switches,  $S_{b1}:S_{b4}$  and  $S_{b2}:S_{b3}$ .

This sequence of alternating positions is repeated for the other two carriers in the second (i.e. negative) half cycle. After the first fundamental cycle  $T_m$ , the two carrier signals, either above or below the x-axis are transposed, i.e. red (signal-1) shifts to level 2, green (signal-2) up to level 1, blue (signal-3) down to level 4 and brown (signal-4) up to level 3. Then the quarter cycle swapping procedure applied during the first fundamental cycle is repeated. This two carrier rotational sequences (i.e. for signal-1, level 1 to level 2 first fundamental cycle and level 2 to level 1 second fundamental cycle) are repeated for every two fundamental cycles. The effect of this quarter cycle swapping is that it brings a phase shift equal to the duration  $T_m/4$  between the two resultant adjacent pulse signals during each positive and negative half of the modulating signals.

### **3.2.2.2 Method 2- Carrier cycle rotation method**

Figure 3.19 shows this method. The two carriers across the positive and negative of the reference signals swap their positions after each carrier cycle ( $T_C$ ), namely the Red (carrier signal -1) and the green (carrier signal-2) swap their positions every carrier cycle. The same applies to blue (carrier signal -3) and brown (carrier signal-4). This sequence of swapping positions is repeated for a fundamental cycle period  $T_m$ . At the beginning of the second fundamental cycle, the swapping sequence is transposed such that carrier signal-1 occupies the former position of carrier signal-2, carrier signal-2 occupies the former position of carrier signal-1. Likewise, carrier signal-3 and carrier signal-4 swap their previous positions at the first carrier cycle. These two carrier rotational sequences are repeated for every two modulating cycles. This method creates a phase shift equivalent to the duration  $T_C$  between the two adjacent carrier signals in controlling sub-module 1 and 2.

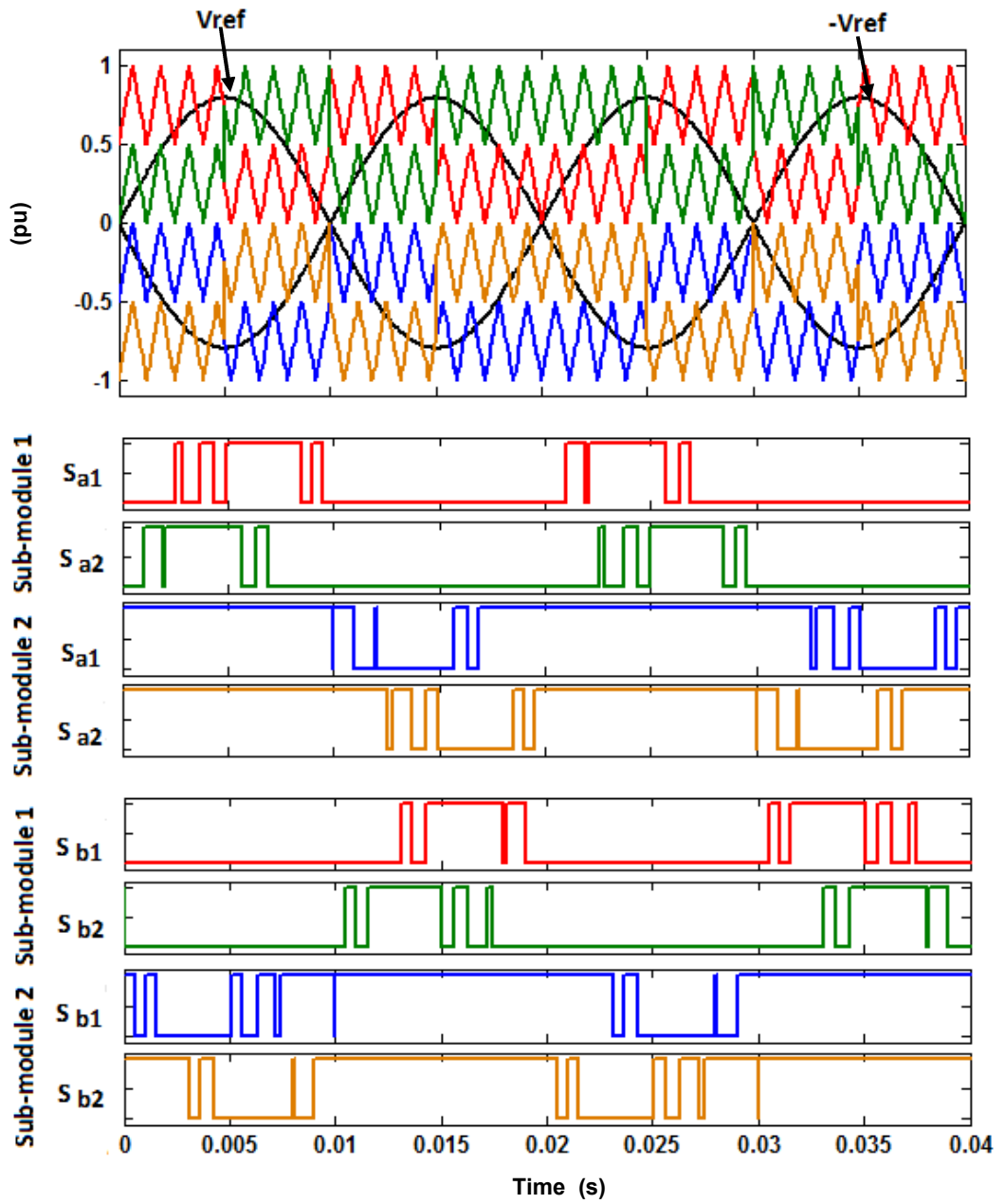


Figure 3.18: Quarter fundamental cycle rotation method for FC-MMCC.

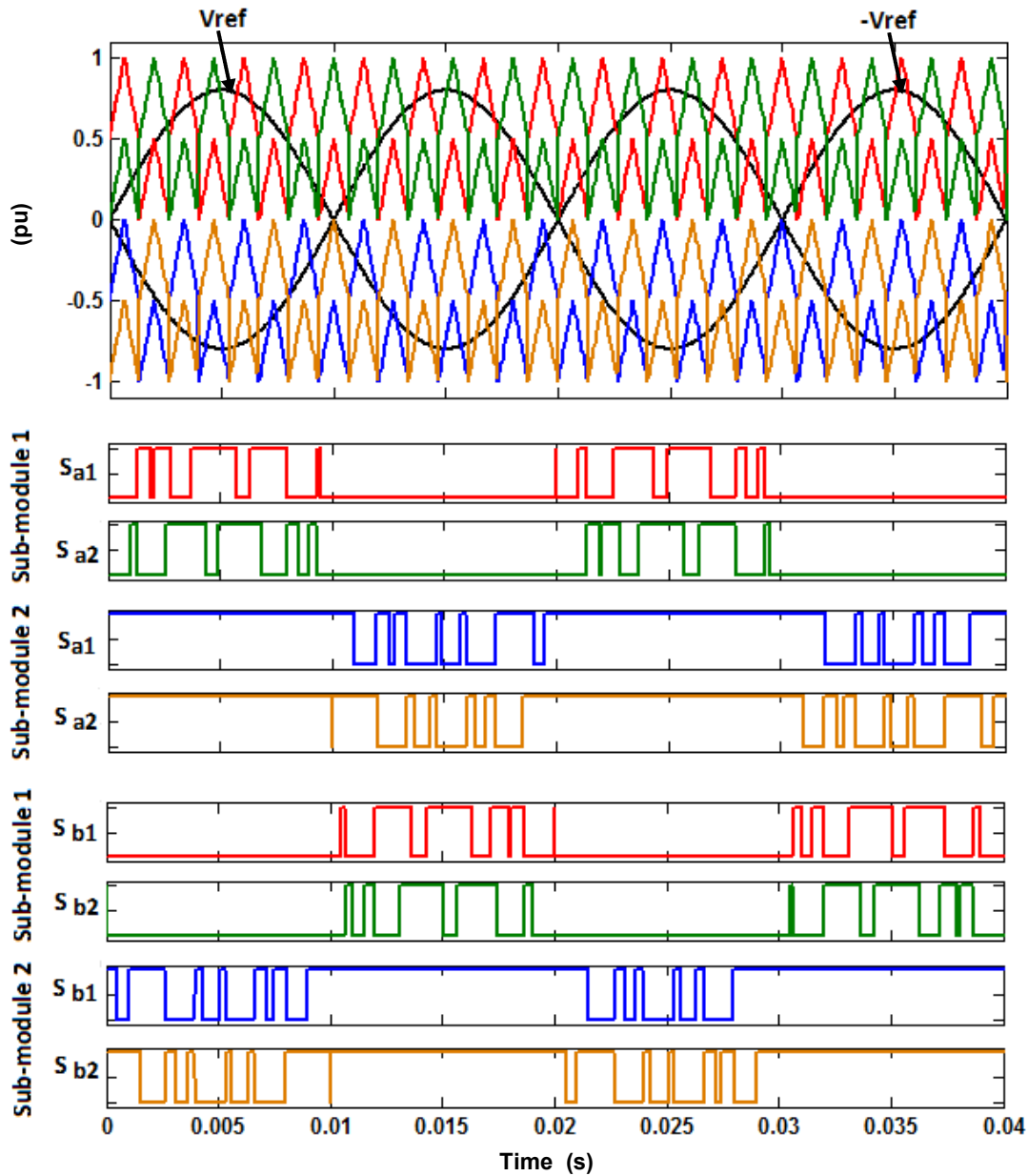


Figure 3.19: Carrier cycle rotation method for FC-MMCC.

### 3.2.2.3 Natural balancing ability

Using the switching signals generated by the above two carrier swapping PWM techniques, the natural voltage balancing ability of the FC-MMCC's inner flying capacitors is assessed over two modulation cycles. Figure 3.20 shows the switching signals for  $S_{a1}$  and  $S_{a2}$ , and those for  $S_{b1}$  and  $S_{b2}$ , together with the voltage waveforms of their corresponding inner capacitors,  $C_A$  and  $C_B$ , when Method 1 is used. In Figure 3.21 the switching signals for the same pairs of devices and voltage waveforms of the same inner capacitors under Method 2 are displayed.

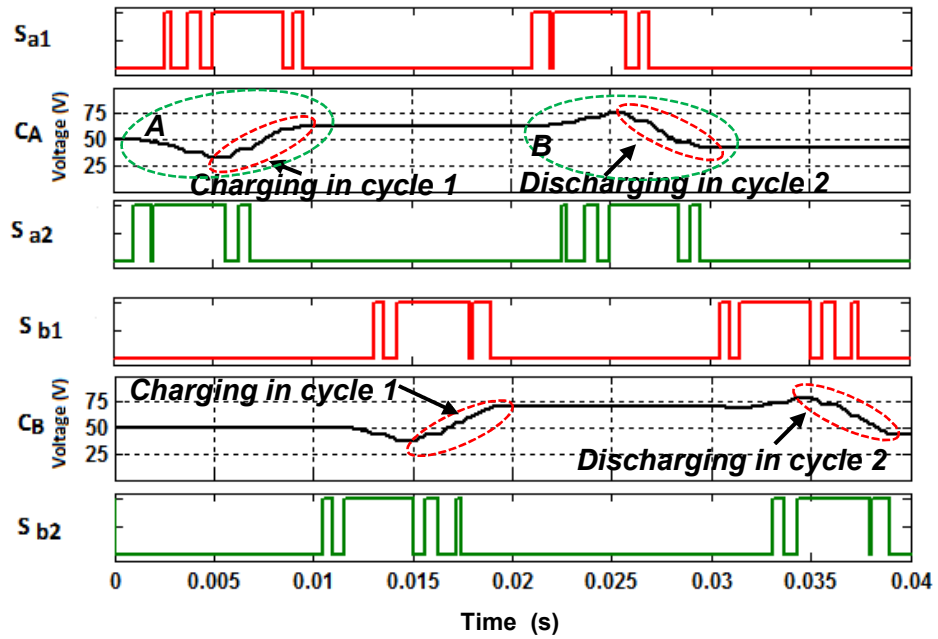


Figure 3.20: Quarter cycle rotation PWM switching actions for investigating sub-module flying capacitor variation

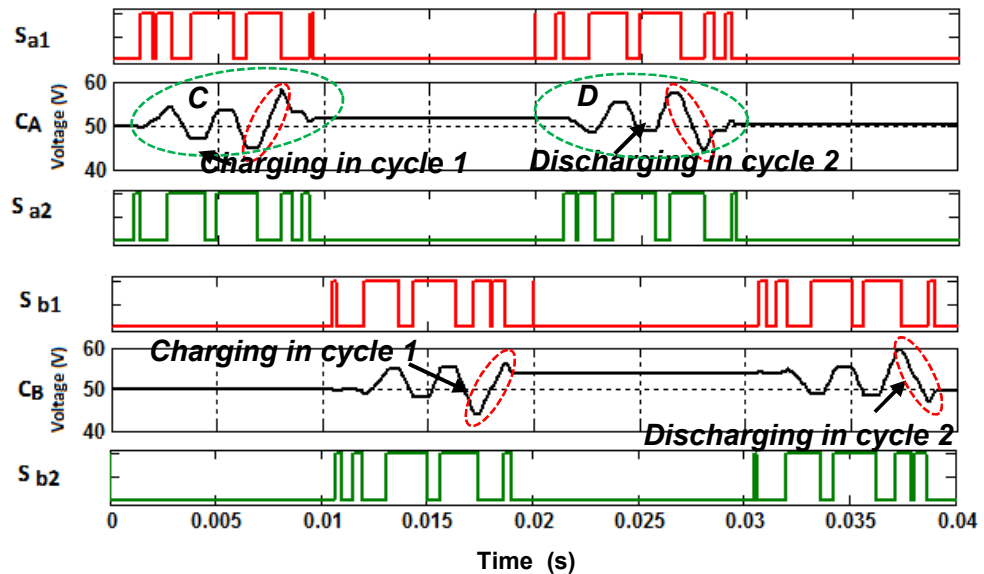


Figure 3.21: Carrier cycle rotation PWM switching actions for investigating sub-module flying capacitor variation.

As observed from both sets of diagrams, the patterns of switching pulses for LHS  $S_{a1}$  and  $S_{a2}$  and those for RHS  $S_{b1}$  and  $S_{b2}$  are symmetrical except for the phase shifts over two fundamental cycles. Consequently if, during the first fundamental cycle, the switching signals cause the inner flying capacitors to discharge, they would result in the same capacitors being charged during the second cycle, and vice versa. Also the ampere-time products for charging and discharging intervals would be equal, making the voltage drift to be zero.

For the quarter cycle rotational method as shown in Figure 3.20, it is observed that due to spreading the carrier swapping sequence over half a cycle of the modulating signal, the inner flying capacitors voltages vary by  $\pm 35\%$  during the first and second fundamental cycle. This same swapping sequence is implemented with two carrier cycles (i.e. carrier cycle rotation method) causing the inner capacitors to deviate by  $\pm 10\%$  under both fundamental cycles. The difference in capacitor voltage deviation between both methods lies with the duration if the switches when  $C_A$  and  $C_B$  are bypassed. In contrast, the PD-PWM scheme experiences longer durations of charging and discharging switch operating states compared to the SC-PWM. Thus, the swapped carrier PWM can achieve natural balancing with less voltage deviation compared to the phase disposed PWM.

### 3.2.2.4 Power loss

#### Conduction loss

Similar relationships between conduction losses and  $m_a$ ,  $m_f$  discussed for PD-PWM exist for both swapped carrier PWM methods, as can be seen in Figure 3.22 and Figure 3.23 respectively. As observed across Figure 3.24(a) and Figure 3.24(b), the carrier Method 2 experiences more conduction periods than the Method 1 quarter cycle PWM corresponding to conduction losses of 27.90W and 29.65W respectively at  $f_s=0.75$  kHz and  $m_a=0.8$  (see appendix B7-B8).

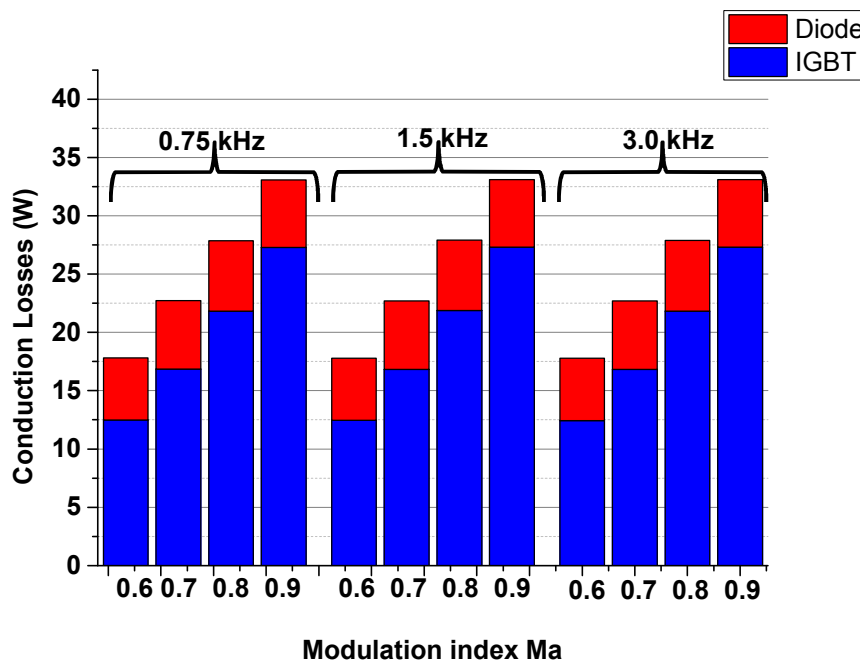


Figure 3.22: Quarter cycle rotation PWM IGBT and Diode conduction loss.



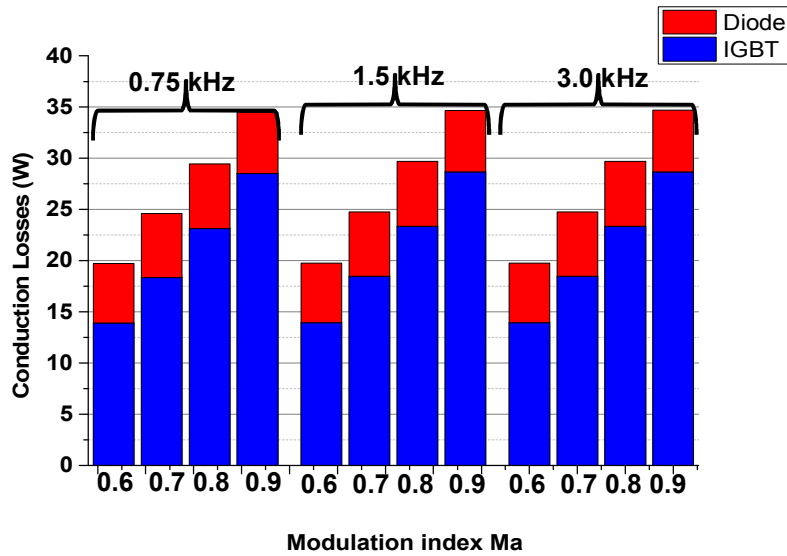


Figure 3.23: Carrier cycle rotation PWM IGBT and Diode conduction loss.

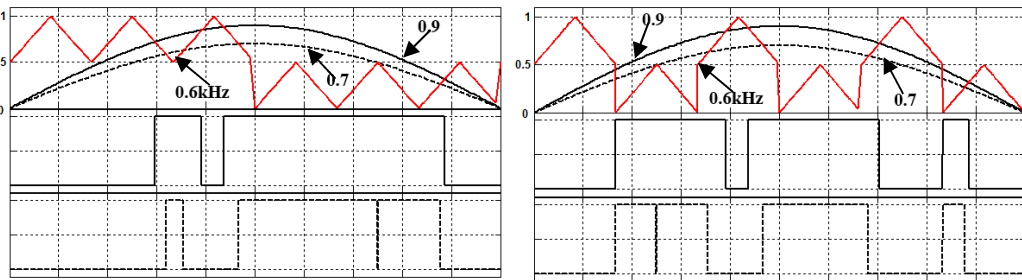


Figure 3.24: Variation in reference signal  $m_a$  (a) Quarter cycle rotation PWM; (b) Carrier cycle rotation PWM.

### Switching loss

Under both swapped carrier methods, the switching losses increase by a factor of two as switching frequency increases from 0.75 kHz and 1.5 kHz respectively as seen in Figure 3.25 and Figure 3.26. The difference in switching losses between both methods is solely accounted for by their number of switching transitions over half a fundamental cycle (see Figure 3.24). The diode switching loss is nearly about 25% of the IGBT switching loss as seen in Figures 3.25 and 3.26.

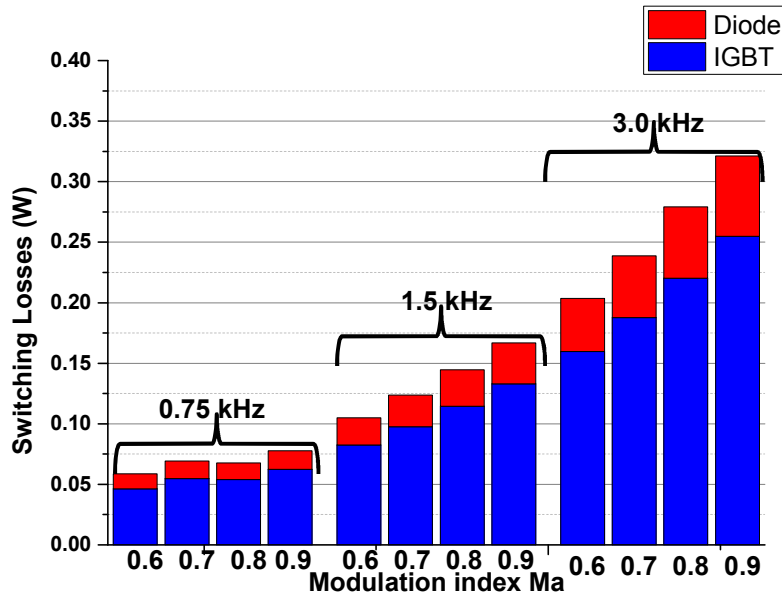


Figure 3.25: Quarter cycle rotation PWM IGBT and Diode switching loss.

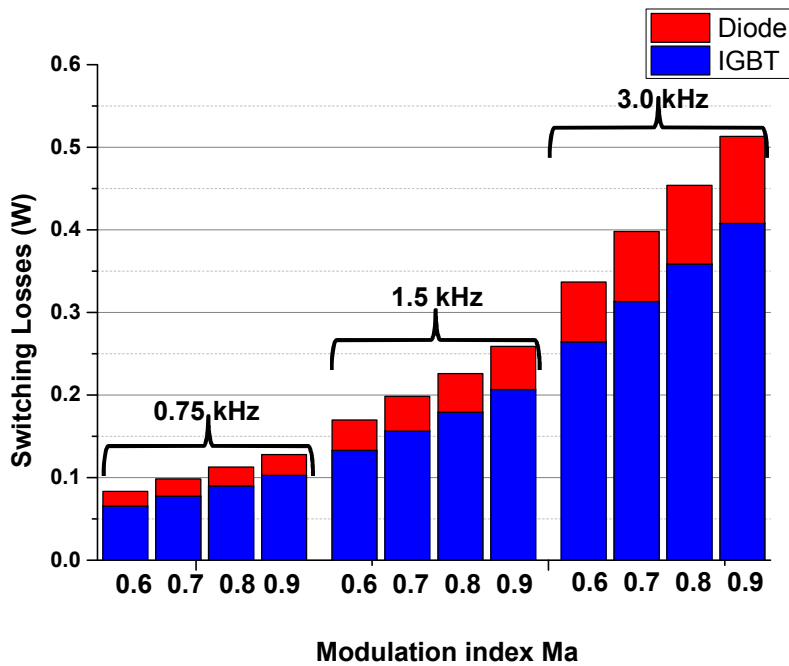


Figure 3.26: Carrier cycle rotation PWM IGBT and Diode switching loss.

**Flying Capacitor losses**

The power losses across both sub-module inner flying capacitors of both methods are equal (see Figure 3.27 and Figure 3.28). This is because the area of charge/discharge region of each inner capacitors (see Figure 3.20 and Figure 3.21) are equal.

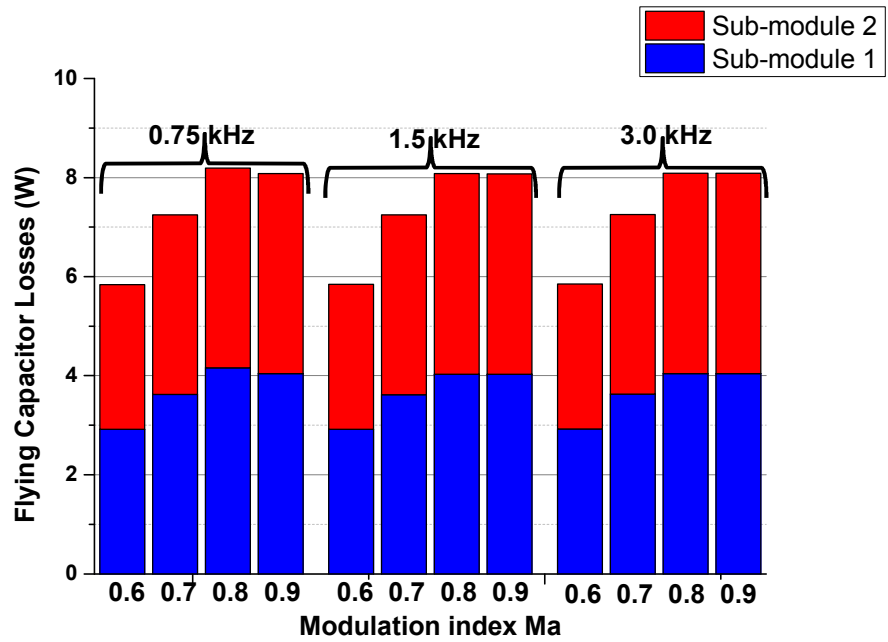


Figure 3.27: Quarter cycle rotation PWM Flying capacitor loss.

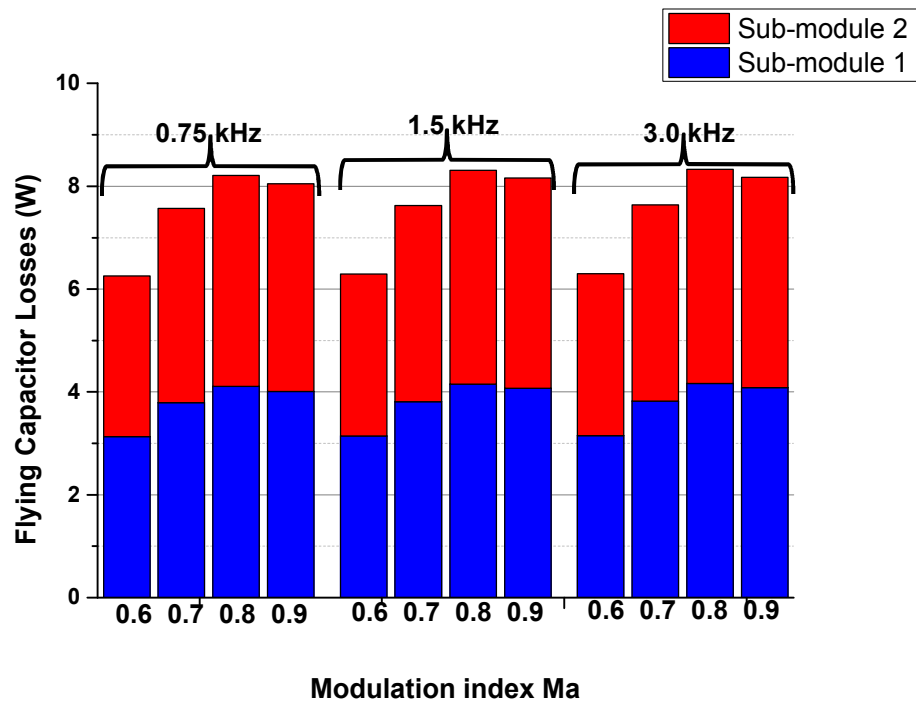


Figure 3.28: Carrier cycle rotation PWM Flying capacitor loss.

**Total loss**

The relationship expressed under PD-PWM scheme between total losses with  $m_a$  and  $m_f$  is similar under these methods. In contrast, the Carrier cycle rotation PWM incurs higher total losses compared to the Quarter cycle rotation PWM.

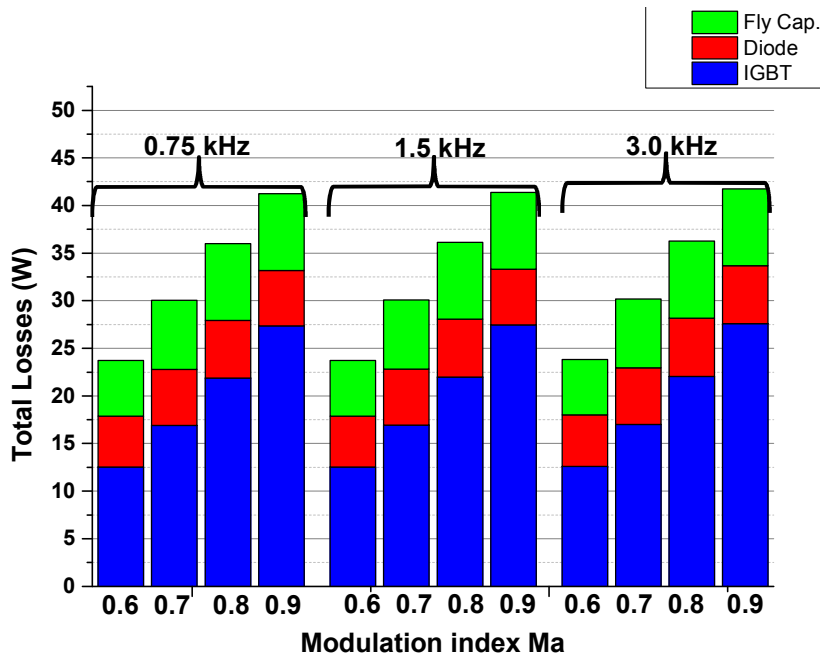


Figure 3.29: Quarter cycle rotation PWM total loss.

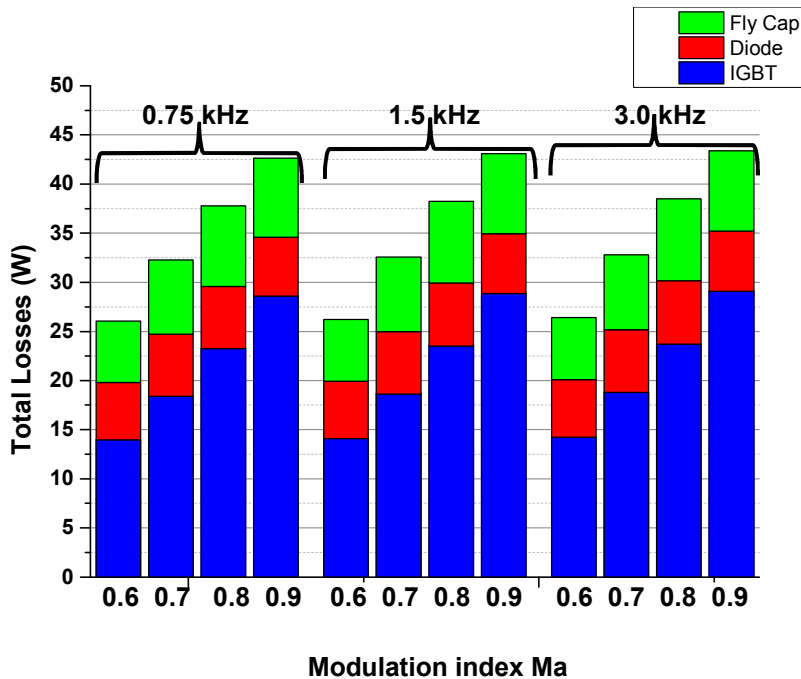


Figure 3.30: Carrier cycle rotation PWM total loss.

### 3.2.2.5 Total harmonic distortion (THD) analysis

The phase voltage and line-to-line voltage waveforms, and their frequency spectra, for the two swapped carrier PWM methods are shown in Figures 3.31- 3.34. The harmonic orders in the spectra of the phase and line output voltage waveforms are expressed below using unipolar switching:

$$\text{Phase voltage: } f_h = h \times f_o = (j(2m_f) \pm k)f_o \quad (3.16)$$

where  $j=1, 2, 3 \dots k=1, 3, 5 \dots$  odd number for phase voltage while for line voltage  $j=1, 2, 3 \dots k=1, 5, 7 \dots$  odd number, excluding odd multiples of 3.

The THDs for the phase and line output voltage waveforms are 16.92%, 15.55% for Method 1 and 12.68%, 9.74% for Method 2. The difference in spectrum quality for both methods lies in the fact that for the quarter cycle method, some baseband harmonics are present around the fundamental frequency while for the carrier cycle method, the baseband harmonics are suppressed up to sidebands found around  $2m_f$ . These baseband harmonics are introduced by the large voltage deviations experienced by the inner flying capacitors. These variations in the flying capacitor voltages create distortion in the output voltage waveforms as seen in Figure 3.31 (phase voltage waveform for quarter cycle method). Figures 3.35 and 3.36 show the 3-D plot of phase voltage THD as a function of  $m_f$  and  $m_a$  for both methods. As can be seen, the carrier rotational method provides better THD performance compared to the quarter cycle method.

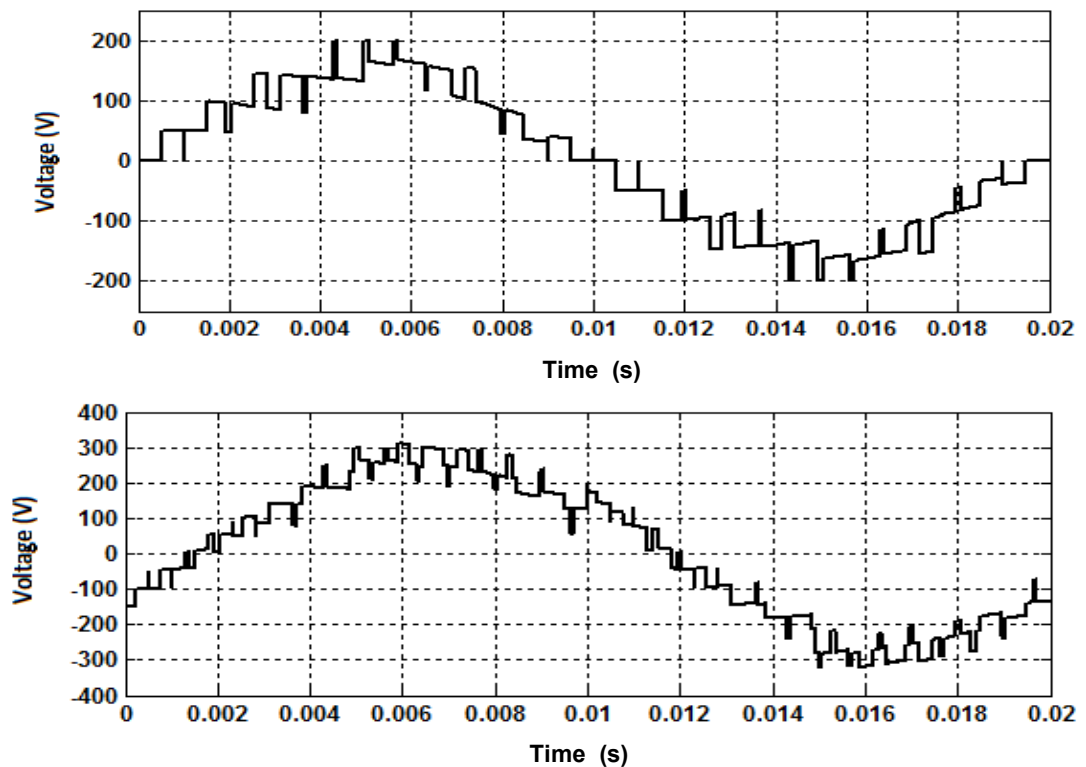


Figure 3.31: Quarter cycle method (a) Phase, (b) line voltage waveforms.

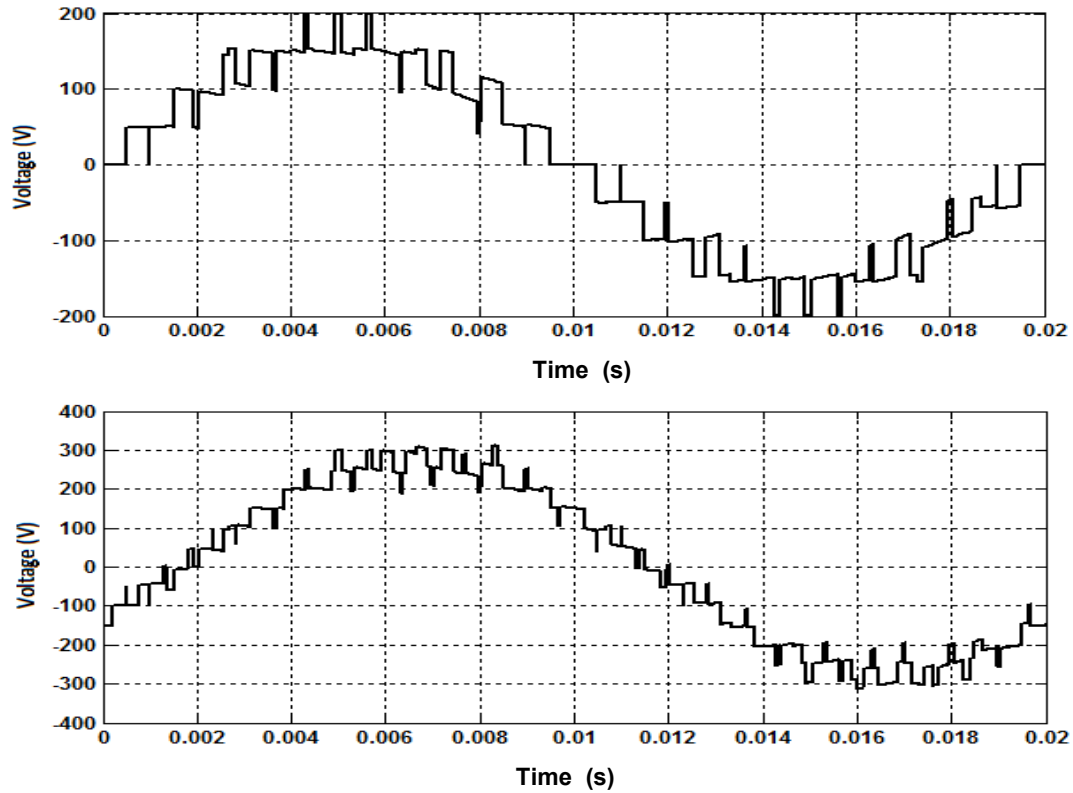


Figure 3.32: Carrier cycle method (a) Phase, (b) line voltage waveforms.

### 3.2.2.6 Sub-module switch utilization

From Figures 3.37 – 3.38, switches  $S_{a1}$ ,  $S_{a2}$  exhibit less conduction loss than  $S_{a3}$ ,  $S_{a4}$ . But the variation in sub-module switch utilization is lower compared to the PD-PWM scheme.

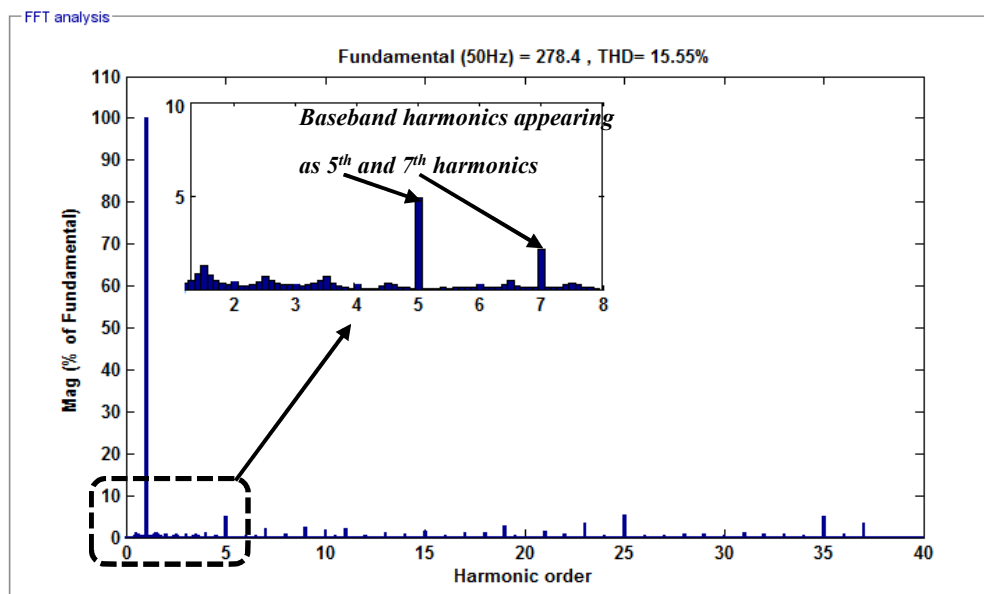
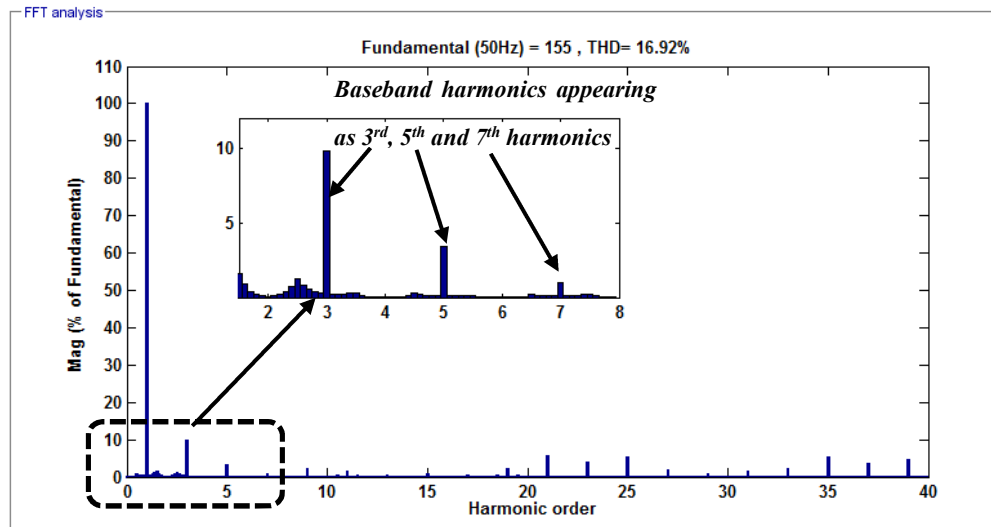
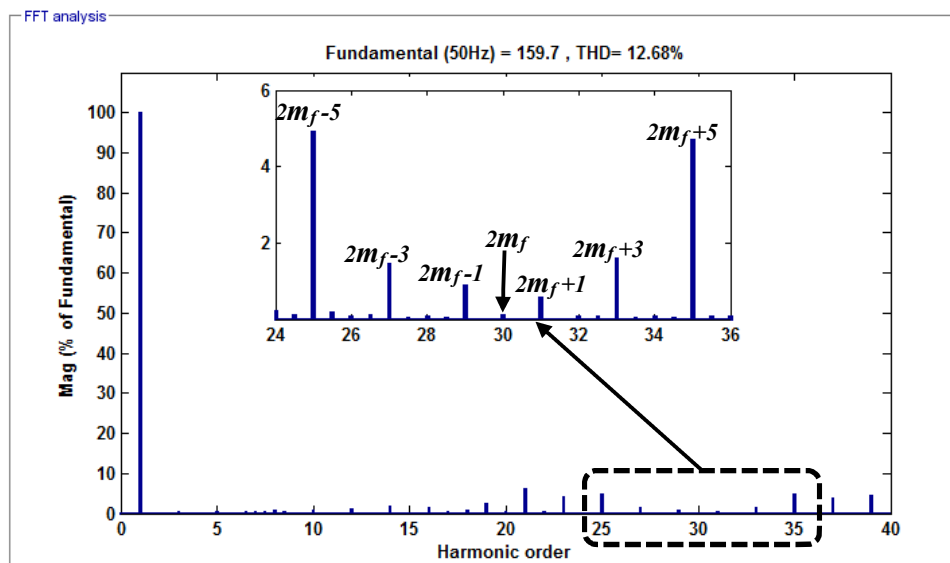


Figure 3.33: Quarter cycle method highlighting (a) phase and (b) line voltage spectra.



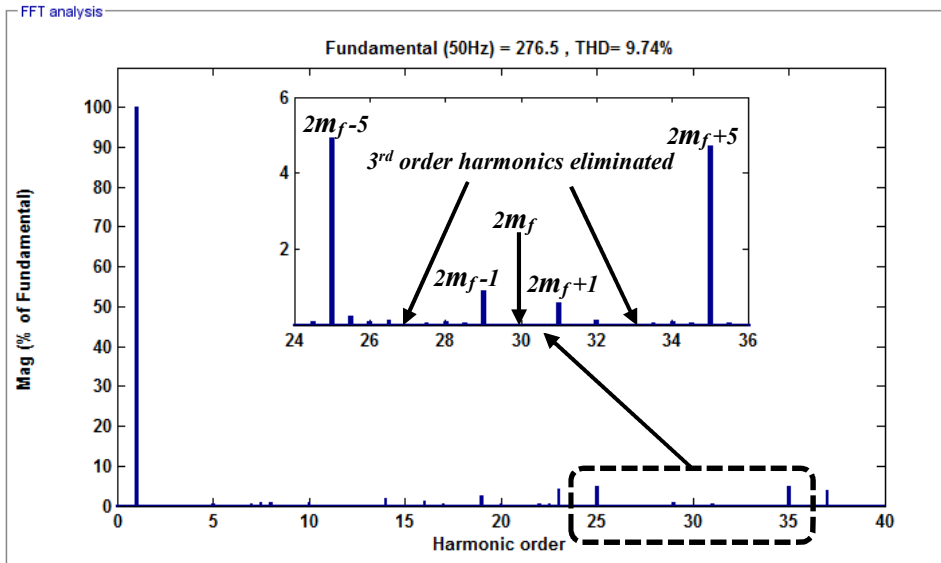


Figure 3.34: Carrier cycle method highlighting (a) phase and (b) line voltage spectra.

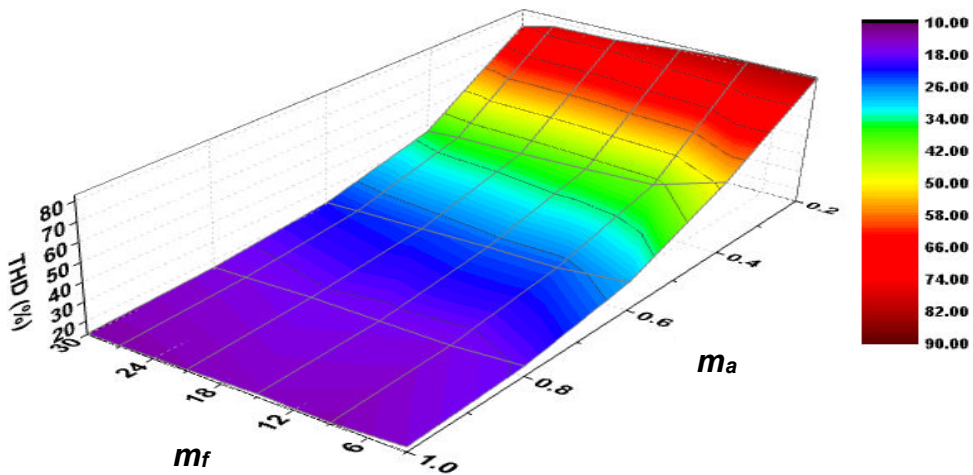


Figure 3.35: Quarter cycle PWM 3-D plot of Total Harmonic Distortion as a function of  $m_a$  and  $m_f$ .

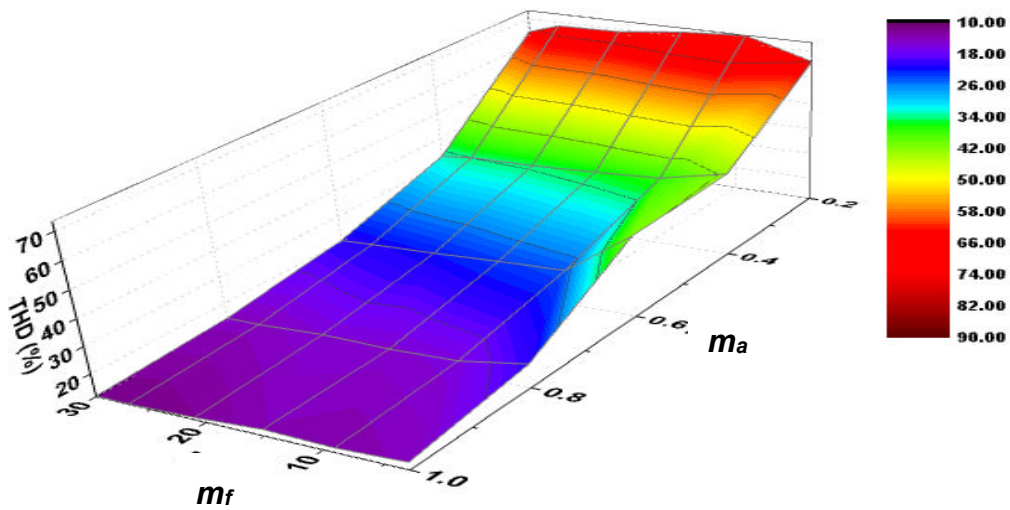


Figure 3.36: Carrier cycle PWM 3-D plot of Total Harmonic Distortion as a function of  $m_a$  and  $m_f$ .



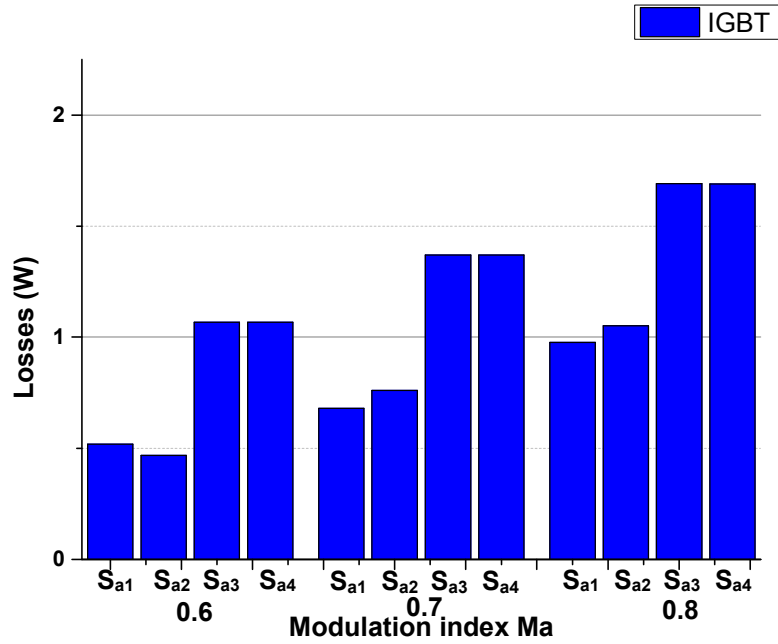


Figure 3.37: Quarter cycle PWM sub-module switch utilization conduction losses.

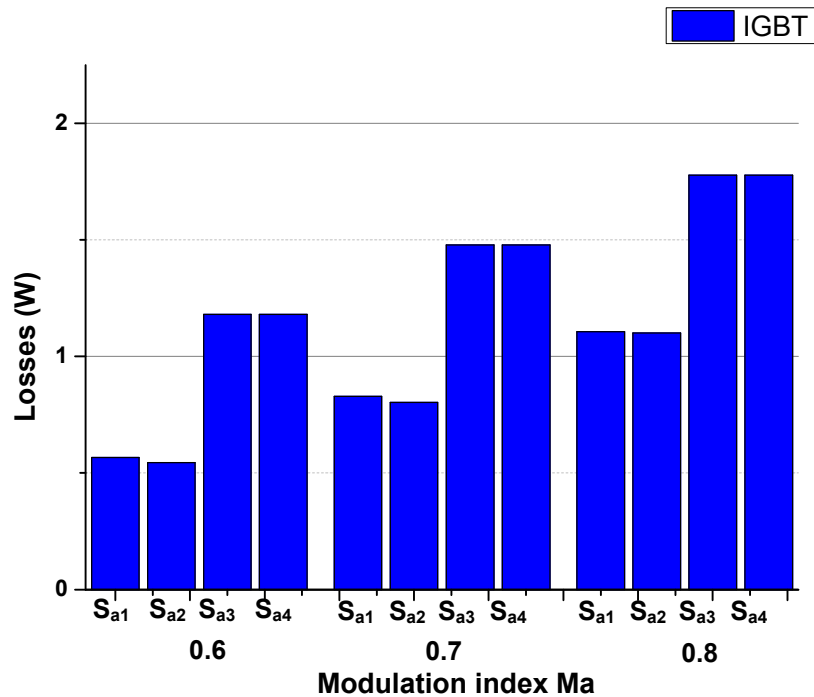


Figure 3.38: Quarter cycle PWM sub-module switch utilization conduction losses.

### 3.2.3 Phase Shifted PWM (PS-PWM)

This is also known as horizontal displacement PWM. This involves the use of multiple triangular carriers which are equally phase or time shifted from each other along the horizontal axis. The number of carriers  $N_T$  required by this

technique is given by the number of voltage levels  $m$ , minus 1. For the two sub-module cascaded FC-MMCC, four triangular carrier signals are required in total; two for each sub-module (i.e. for unipolar switching). The constant phase angle delay  $\alpha_c$  between carriers is expressed as:

$$\alpha_c = \frac{180^\circ}{N_T} \quad (3.17)$$

where  $N_T$  is the total number of triangular carriers and in this case it is 4, so  $\alpha_c = 45^\circ$ .

The PS-PWM scheme implemented for the FC-MMCC and the resultant pulse trains for the switches of two cascaded FC modules in one phase limb are illustrated in Figure 3.40. The four phase-shifted carrier signals are compared with the two anti-phased reference signals  $V_{ref}$  and  $-V_{ref}$  to synthesize switching signals.

For sub-module 1,  $V_{ref}$  compared to triangular carriers 1 (Red) and 2 (Green) generates switching pulses to drive the complementary switches  $S_{a1}:S_{a4}$  and  $S_{a2}:S_{a3}$  and whilst  $-V_{ref}$  compared with the same carriers leads to signals to drive switching pairs  $S_{b1}:S_{b4}$  and  $S_{b2}:S_{b3}$ . In this case, the modulation frequency index  $m_f = 5$  is used and  $m_a = 0.8$ . The switching signals for sub-module 2 are also shown in Figure 3.40.

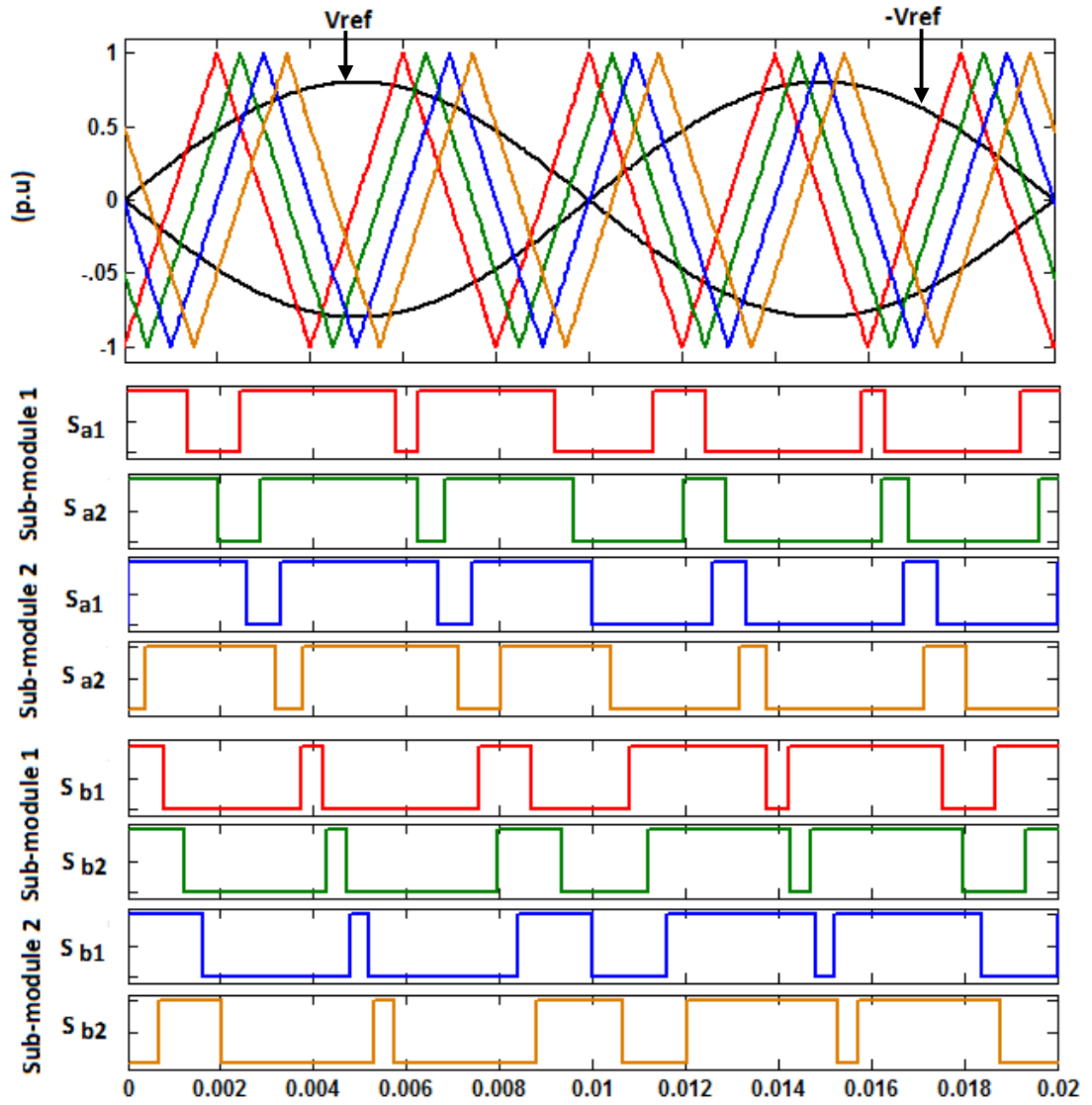


Figure 3.39: Phase shifted PWM for FC-MMCC at  $m_f=5$ .

### 3.2.3.1 Natural balancing ability

The balancing ability of the PS-PWM scheme for the inner flying capacitors is investigated using sub-module switching signals shown in Figure 3.40 for one reference cycle operation.

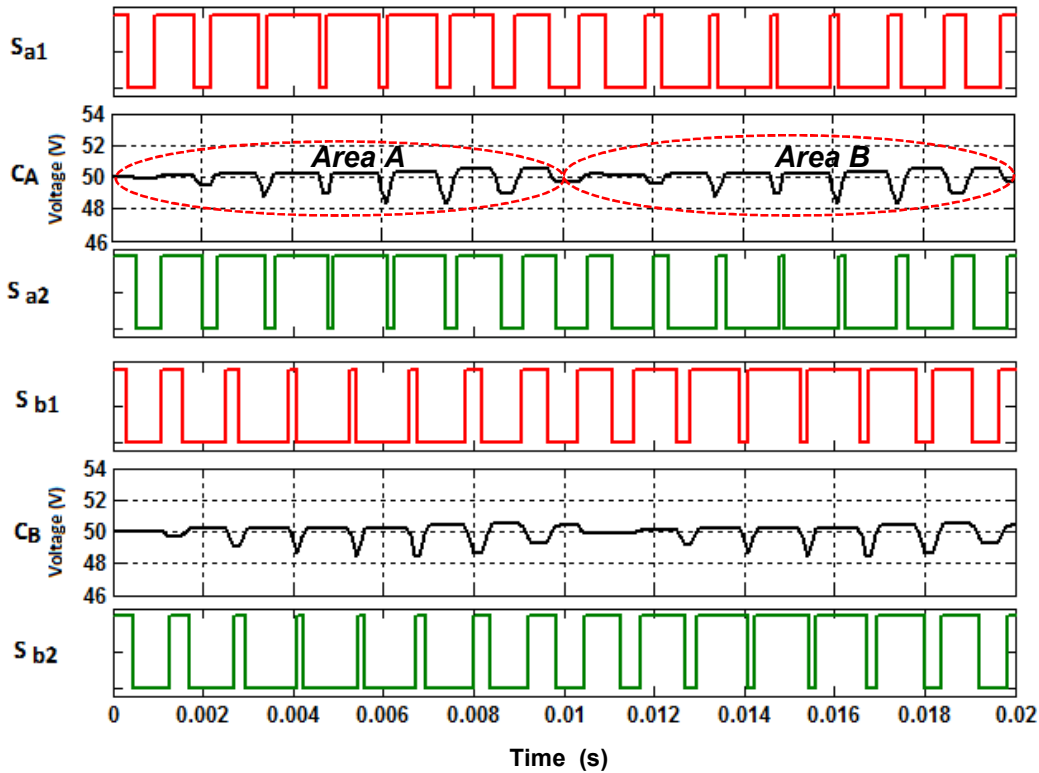


Figure 3.40: Phase shifted PWM switching actions for investigating sub-module flying capacitor variation.

As observed from Figure 3.40, the switching patterns are symmetrical over a fundamental half cycle. This symmetry results from the repetitive nature of the switching signals over a fundamental cycle, thus resulting in the charging/discharging durations in each half modulating cycle to be equal having a zero voltage drift (*i.e. charge/discharge under area A = area B*). Balance is assessed by considering whether the net charge transferred over one cycle is zero. In this example, the inner flying capacitor voltages deviate from their nominal values by  $\pm 1.5\%$  per cycle. This small deviation is accounted by the bypass states of  $C_A$  and  $C_B$  far exceeding their charge/discharge operating switch states.

### 3.2.3.2 Power loss

#### **Conduction loss**

Similar relationships between conduction losses and  $m_a$ ,  $m_f$  discussed for PD-PWM exist for the PS-PWM scheme, as seen in Figure 3.41.

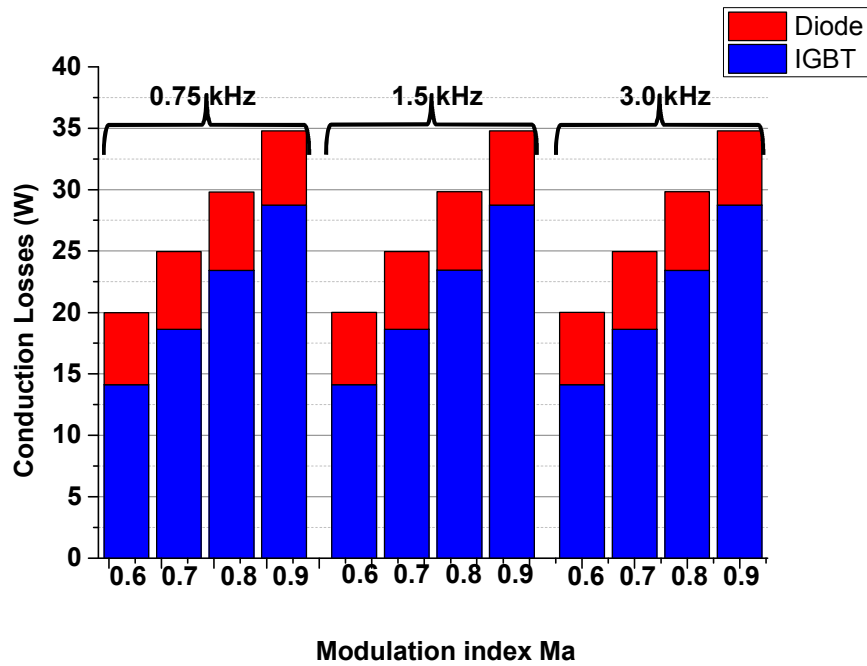


Figure 3.41: IGBT and Diode conduction loss.

### Switching loss

The switching loss of IGBT and diode increases by a factor of two as switching frequency increases by 2 as illustrated in Figure 3.42. In comparing with other carrier PWM techniques, the PS-PWM switching losses is higher than the other carrier types. This is attributed to the horizontal displacement of carriers such that when compared to the modulating signal, the number of switching transition is more compared to vertically displaced carriers.

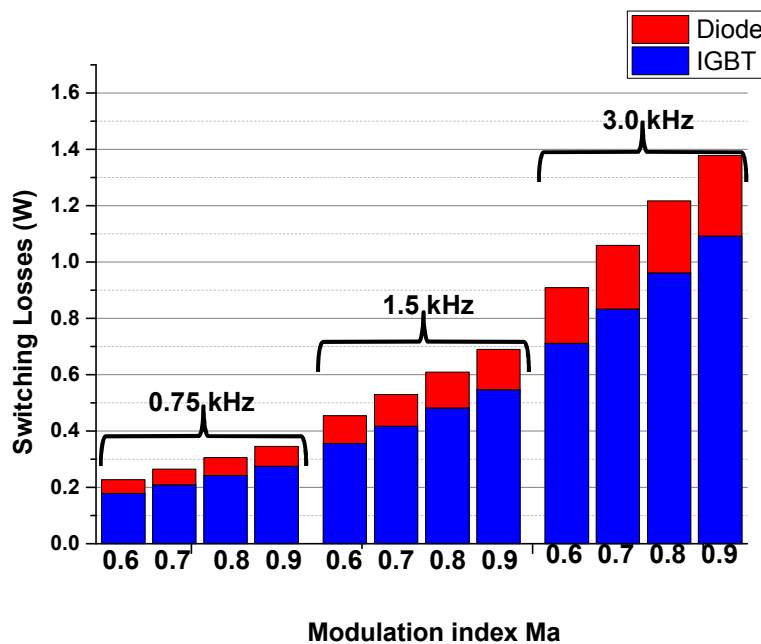


Figure 3.42: IGBT and Diode switching loss.

### Flying Capacitor losses

The equal area of charge/discharge of each inner flying capacitor as shown in Figure 3.40 validates each sub-module flying capacitor experiencing equal power loss (see Figure 3.43).

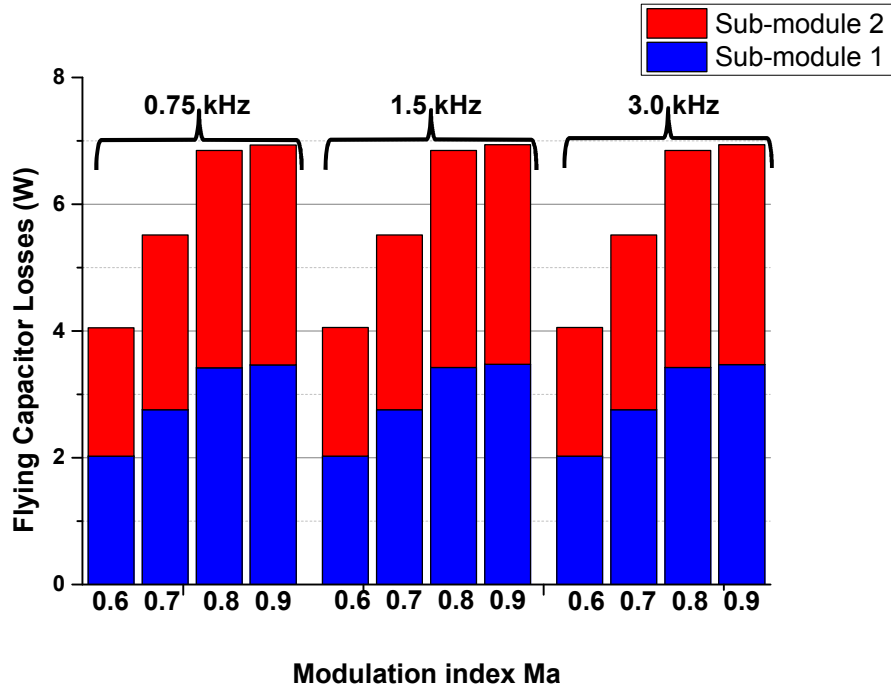


Figure 3.43: Flying capacitor loss.

### Total loss

The power loss contributions of IGBT, diode and inner floating capacitor with respect to the total loss are 64%, 17.8% and 18.2% see Figure 3.44.

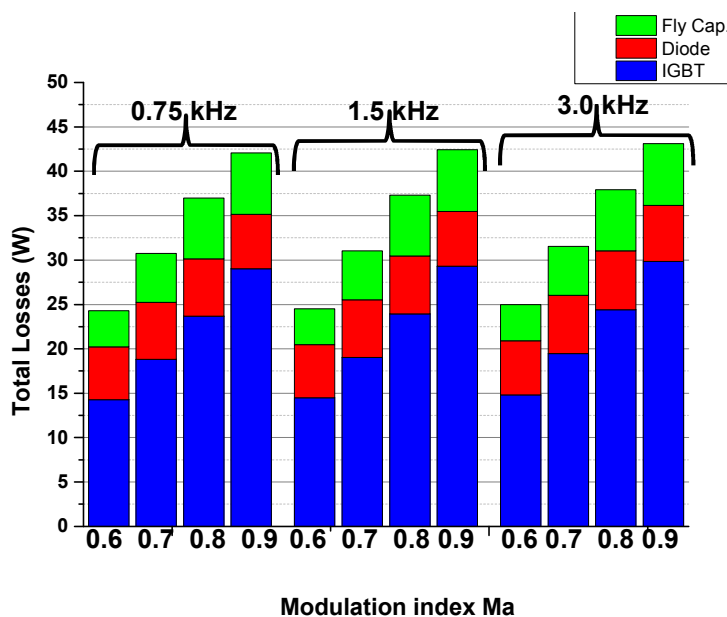


Figure 3.44: Total Losses.

### 3.2.3.3 Total harmonic distortion (THD) analysis

The FC-MMCC phase and line voltage waveforms and frequency spectra are shown in Figure 3.45 and Figure 3.46. For this analysis,  $m_f=15$ . The harmonic orders in the spectra of the phase and line output voltage are expressed below as:

$$\text{Phase voltage: } f_h = h \times f_o = (j8m_f \pm k)f_o \quad (3.18)$$

where  $j=1, 2, 3 \dots$   $k=1, 3, 5 \dots$  odd number for phase voltage while for line voltage  $j=1, 2, 3 \dots$   $k=1, 5, 7 \dots$  odd number, excluding odd multiples of 3.

As observed from both Figure 3.46 (a) and Figure 3.46 (b), all the baseband, and sideband around carrier harmonics are suppressed until the 8<sup>th</sup> multiple of the carrier frequency. This is because the four phase-shifted carriers and the two anti-phase reference signals make the equivalent switching frequency of the FC-MMCC to be eight times the cell switching frequency (i.e.  $f_{sw}=8 \times f_s$ ).

The THD for both the phase and line voltages are 12.92% and 9.70% respectively. For the phase voltage spectrum, all even harmonics are eliminated with sideband harmonics appearing around  $8m_f$  and its multiples, whilst for line frequency spectrum, all 3<sup>rd</sup> order harmonics appearing around  $8m_f$  and its multiples are eliminated. Figure 3.47 shows the 3-D plot of phase voltage THD as a function of both frequency and amplitude modulation indexes for both methods.

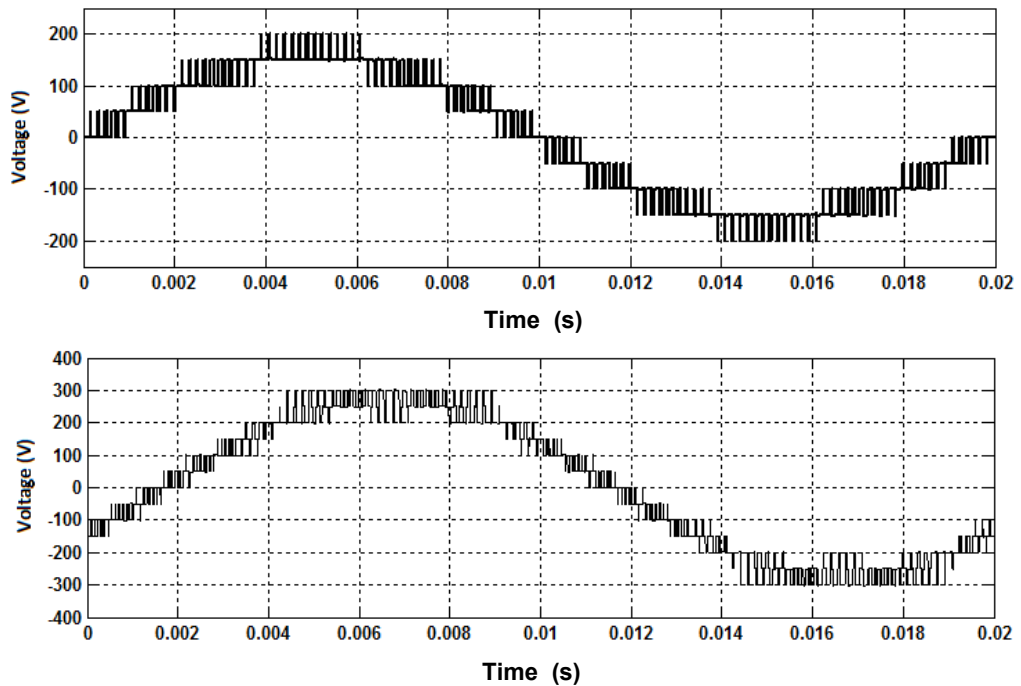


Figure 3.45: (a) phase and (b) line voltage waveforms of the FC-MMCC.

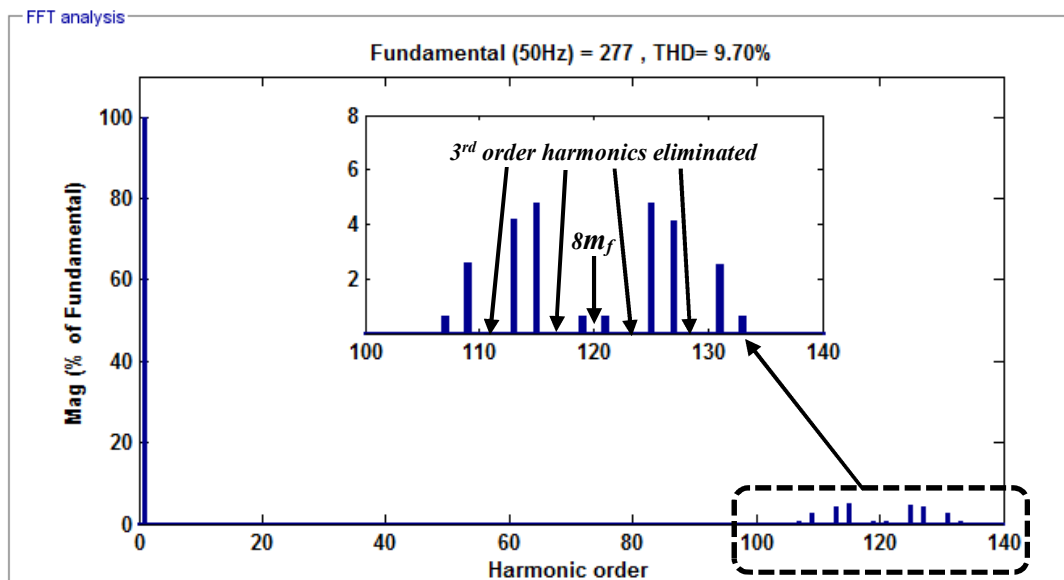
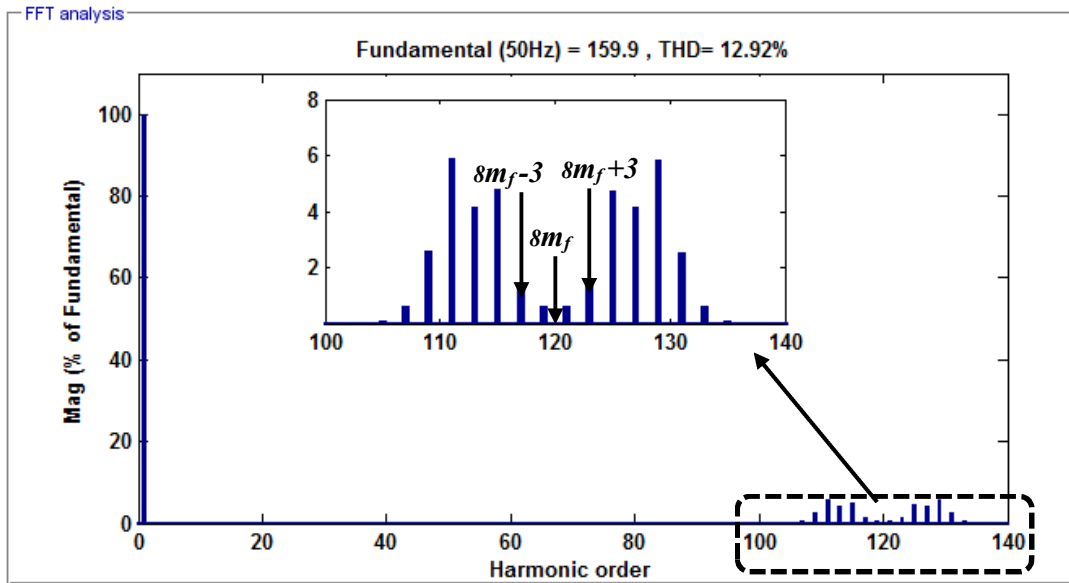


Figure 3.46: (a) phase and; (b) voltage spectra (PS-PWM).

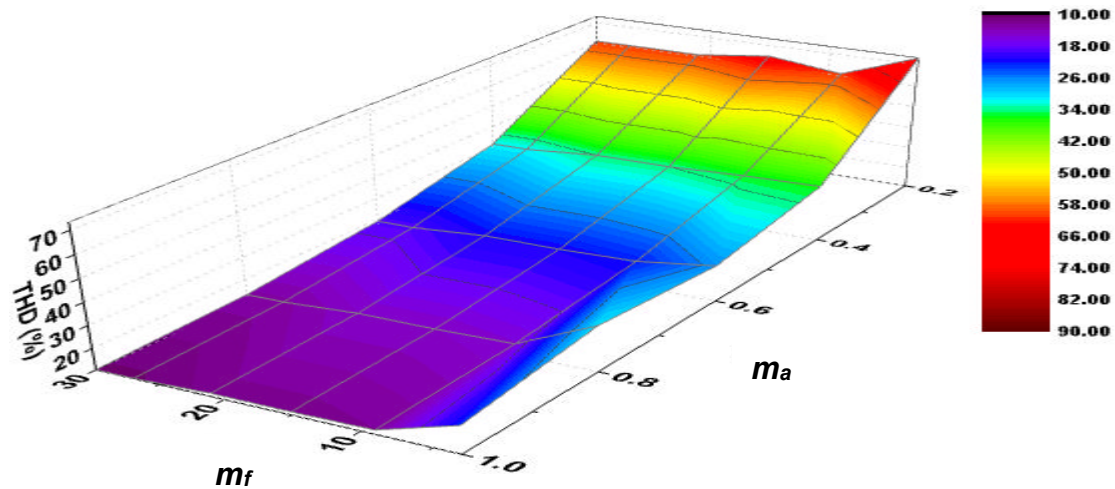


Figure 3.47: PS-PWM 3-D plot of Total harmonic distortion as a function of  $m_a$  and  $m_f$ .



### 3.2.3.4 Sub-module switch utilization

From Figure 3.48, it is observed that the sub-module switches are equally utilized over every fundamental cycle. This is because the pulses applied in controlling the sub-module switches are identical. From appendix B.21, the switches  $S_{a1}$ ,  $S_{a2}$  and  $S_{b1}$ ,  $S_{b2}$  across a sub-module experience equal conduction losses.

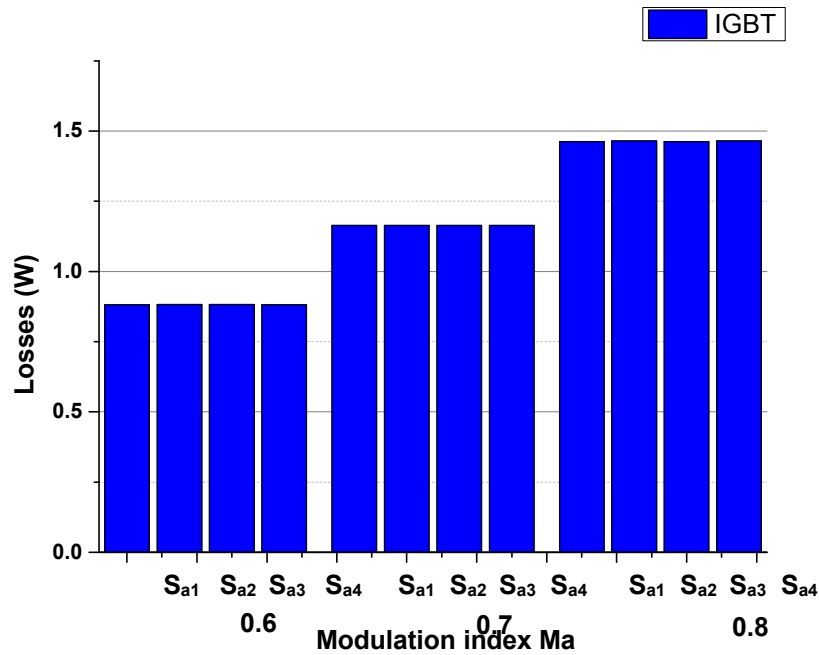


Figure 3.48: PS-PWM sub-module switch utilization conduction losses.

## 3.3 Discussion and Comparison of different Carrier PWM Techniques

### 3.3.1 Natural Balancing Ability

This is achievable under all the PWM schemes discussed but the amount of voltage deviation varies between them. This is as observed in Figure 3.49, which shows the relationship between  $m_f$  and inner capacitor voltage variation (i.e. actual voltage deviation/nominal capacitor voltage) for all PWM techniques. The PS-PWM followed by the carrier-swapped PWM offers the best voltage deviation compared to the others. This is due to the high number of switching transitions provided by these schemes.

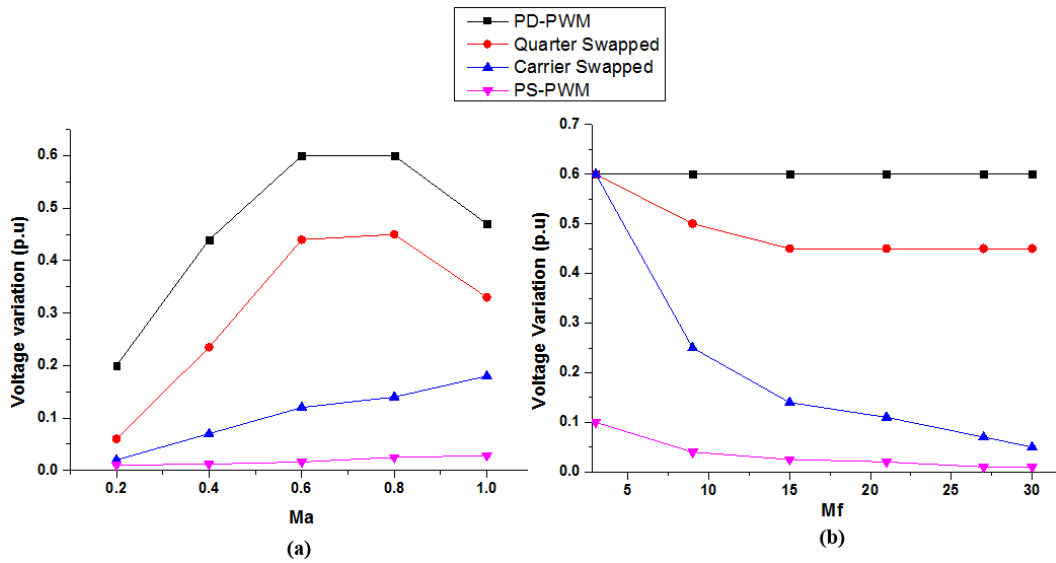
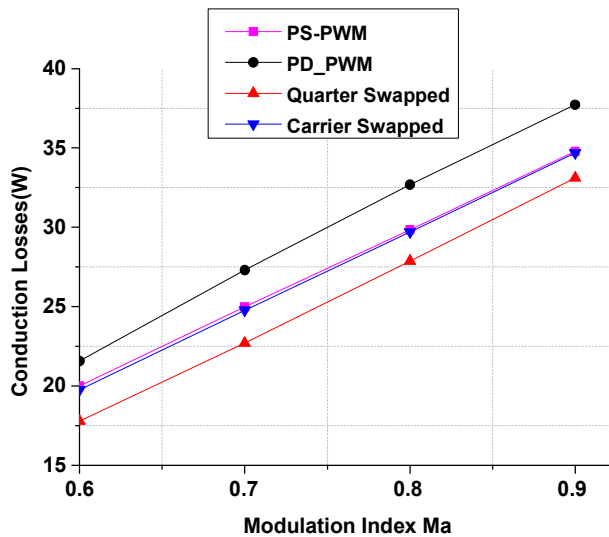


Figure 3.49: Inner flying capacitor voltage with respect to (a) modulation index and (b) modulation frequency.

### 3.3.2 Power loss

As seen in Figure 3.50(b), the PD-PWM and quarter cycle PWM give the highest and lowest conduction losses compared to the other PWM schemes. This is accounted for by their conduction periods. Figure 3.50(a) shows that the PS-PWM incurs more switching losses compared to other PWM methods. This is due to the phase shifting effect of its carrier signals which result in an equivalent switching frequency of  $8m_f$  compared to the  $2m_f$  offered by the vertically displaced methods.



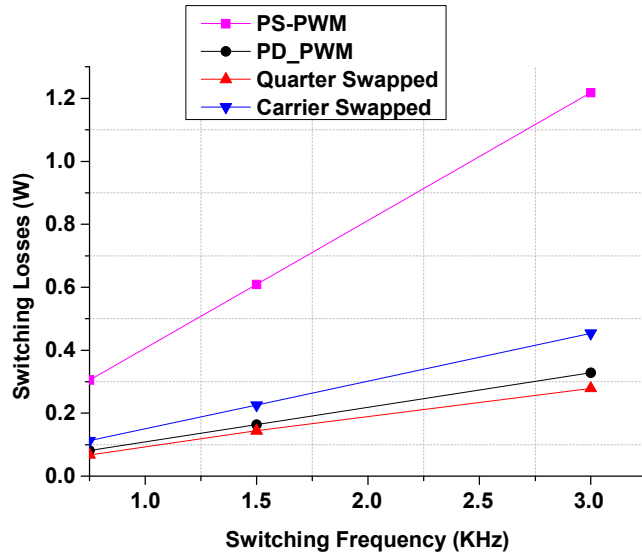
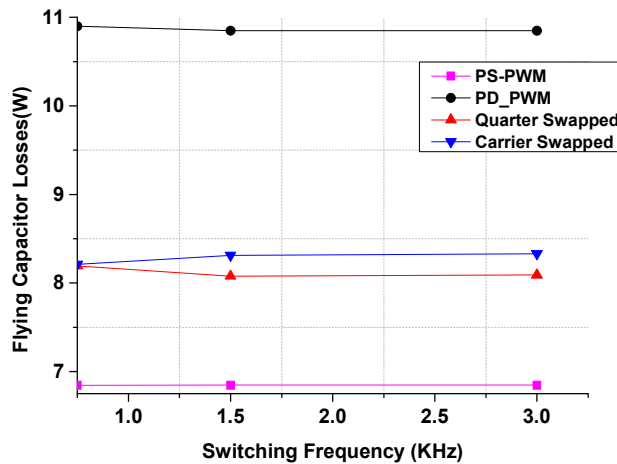


Figure 3.50: Power losses (a) conduction and (b) switching losses.

The PS-PWM and PD-PWM produce the lowest and highest inner flying capacitor power losses as seen in Figure 3.51(a). This is because the rate of charge and discharge has a direct relationship with power dissipated across the equivalent series resistance of each inner flying capacitor. In addition, the summation of each device power losses shows that the PD-PWM results in the highest while the quarter cycle method offers the lowest, see Figure 3.51(b).



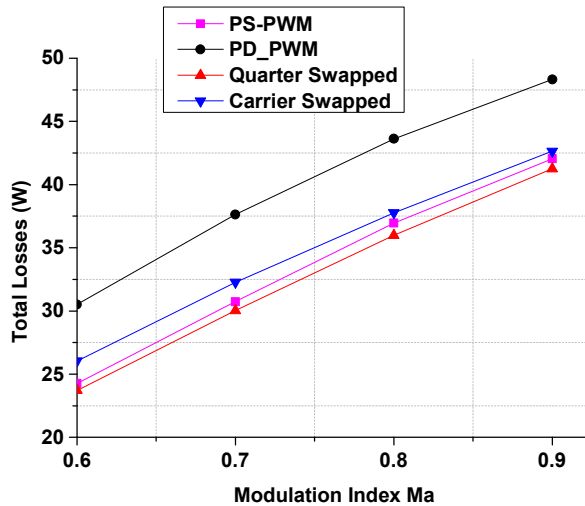


Figure 3.51: Power losses (a) Flying capacitor and (b) total losses.

### 3.3.3 Total harmonic distortion

The PS-PWM and PD-PWM generate the best and worst THDs compared to the two carrier swapped methods as seen in Figure 3.52. The PS-PWM is superior because it offers less voltage deviation for its inner flying capacitors which build-up the intermediate states of the converter output voltage.

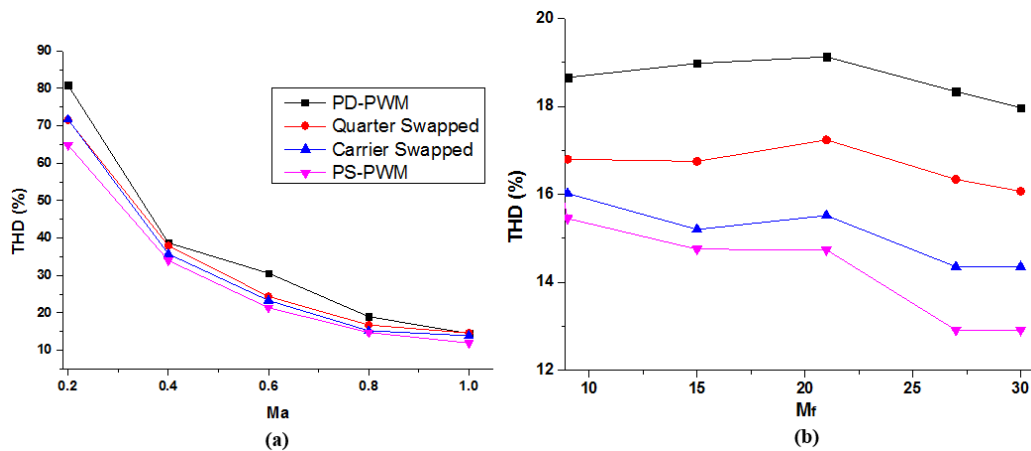


Figure 3.52: Total harmonic distortion with respect to (a) modulation index and (b) modulation frequency.

### 3.3.4 Sub-module switch utilization

From Figure 3.53, it is seen that in comparing between  $S_{a1}$  and  $S_{a2}$  switches for effective inner flying capacitor balancing, these switches are equally used for both PS-PWM and carrier – swapped methods, and slightly utilized for the quarter cycle method while the PD-PWM give the worst utilization.

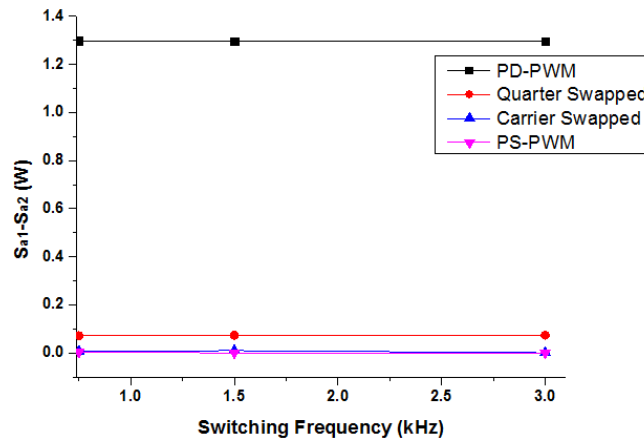


Figure 3.53: Sub-module switch utilization.

To graphically analyse these PWM methods for FC-MMCC application, a scoring system allocating values for each PWM schemes is used. These values range from 1-4, where first-4 and down to fourth-1. From Figure 3.54, the PS-PWM scheme offers the best performances followed by the rotational carrier method.

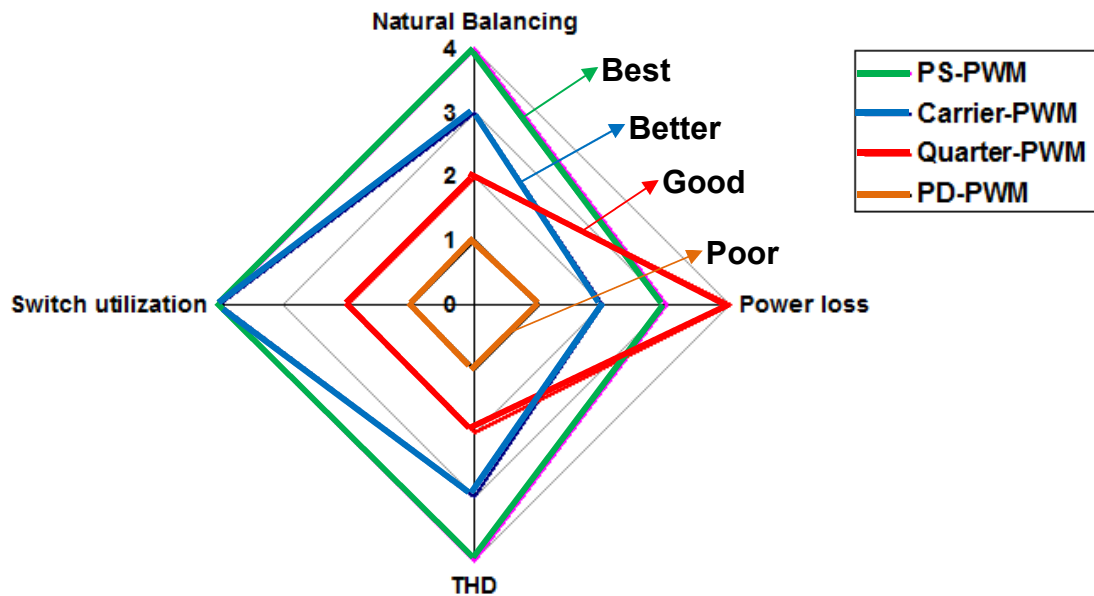


Figure 3.54: Carrier placement PWM ranking.

### 3.4 Summary

This chapter has presented four carrier-based PWM schemes for the FC-MMCC. All schemes were analysed in terms of natural voltage balancing ability of their inner flying capacitors, power losses, THD and sub-module switch utilization. In comparison with other three schemes, the PS-PWM stands out to be the best in all four criteria.

## Chapter 4

### Overlapping Hexagon Space Vector Modulation Strategy

Space vector modulation technique is a well-known and preferred PWM scheme for voltage source converters of all voltage levels since it offers an extra 15.5% dc bus voltage utilization [170], and reduced current ripples. This method cannot be applicable when a phase angle unbalanced exist between voltage phases. For its control of the basic three-phase two-level converter the SVM technique uses the three-phase stationary reference frame voltages to represent each inverter switch state. These states are mapped to the complex two-phase orthogonal  $\alpha\text{-}\beta$  plane, hence forming a hexagon. The reference voltage is represented as a vector in this plane and duty-cycles are computed for the selected switching state vectors in proximity to the reference.

For multilevel converters, conventional and MMCC, implementation of space vector modulation technique, though widely known and popular [170-175], is complicated. In particular, for an MMCC having many modules per phase, the number of switch states can be large and increases with the voltage levels, hence the on-line selection of switch states and calculation of duty cycle at different voltage levels become tedious. In addition, it is difficult to choose switch states and sequences to simultaneously obtain capacitor voltage balancing, minimum switching loss and harmonic reductions.

This chapter presents a novel overlapping hexagon space vector modulation (OH-SVM) technique developed by the author for the control of modular multilevel cascaded converters. The rationale of the proposed method is simple; instead of using a single hexagon with multiple regions in the six sectors to cover multiple levels of voltages, it uses either multiple two-level hexagons or multiple three-level hexagons which are overlapped on each other. The number of such hexagons is dependent on the number of cascaded modules in an MMCC, and switching state selection and duty ratio calculation can be performed per hexagon and per module without involving complicated procedures when using a single multilevel hexagon. This scheme offers flexibility and simplicity for controlling an MMCC with any number of chained modules.

This chapter starts by reviewing the basic SVM technique for two-level and multilevel converters. It then describes the new OH-SVM which uses both 2-level and 3-level hexagons. Comparison between this new SVM and the conventional multi-level SVM method for controlling an FC-MMCC with two cascaded modules is performed by simulation studies of these methods. The

OH-SVM technique using a 2-level hexagon method for two cascaded 3-level H-bridge converters per phase is experimentally validated.

#### 4.1 Review of the Basic SVM Method

Using the basic SVM technique for controlling a three-phase 2-level VSC with dc-bus voltage  $\pm V_{dc}/2$ , the three phase  $abc$  coordinates are projected into  $\alpha$ - $\beta$  coordinates see Figure 4.1, and the three phase voltages are transformed to their equivalent  $\alpha$ - $\beta$  representation using Clarke transformation matrix as expressed in (4.1) below:

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix}. \quad (4.1)$$

For a 2-level VSC, there are eight switch states used to synthesize the reference voltage vector  $\vec{V}_{ref}$ . Its  $\alpha$ - $\beta$  and  $abc$  coordinate forms are expressed below:

$$\vec{V}_{ref} = v_\alpha + jv_\beta = \frac{2}{3} \left( V_a + V_b e^{-j\frac{2\pi}{3}} + V_c e^{j\frac{2\pi}{3}} \right). \quad (4.2)$$

Using  $\alpha$ - $\beta$  components the magnitude and angular value  $\theta$  of reference voltage vector can be expressed as:

$$V_{ref} = \sqrt{V_\alpha^2 + V_\beta^2} \quad (4.3)$$

$$\theta = \tan^{-1} \left( \frac{V_\beta}{V_\alpha} \right) = 2\pi f_s t \quad (4.4)$$

where  $f_s$  is the sampling frequency.

Amongst the eight voltage vectors, six are active ( $\vec{V}_1 - \vec{V}_6$ ) and two zero ( $\vec{V}_0$  and  $\vec{V}_7$ ) states voltage vectors. These are mapped in a two-phase orthogonal  $\alpha$ - $\beta$  plane, hence forming a hexagon constellation pattern in the complex plane as shown in Figure 4.1. The three-phase reference voltage also mapped in this plane can be approximated by the selected sequence of the switching vectors and their corresponding duty-cycles. The magnitude of each switching state vector is  $2V_{dc}/3$ . The magnitude of a vector to the mid-point of the line between each switching state vector vertex is  $V_{dc}/\sqrt{3}$ . The amplitude modulation index,  $m_a$ , is defined as the ratio of the peak output voltage sinusoid to the maximum positive available voltage  $V_{dc}/2$ . Therefore, the maximum possible modulation depth for SVM is 1.155 and so it can operate

with modulation depths above unity, in the same way as sine-triangle PWM with the 3<sup>rd</sup> order harmonic injection.

The location of  $\vec{V}_{ref}$  determines the voltage vectors involved in active switching. The volt-second principle is applied in determining the duty cycle of each voltage vectors when used [174, 176]. This principle states that the product of the reference voltage vector  $\vec{V}_{ref}$  and its sampling period  $T_s$  must be equal to the sum of the product of each three voltage vectors and their dwell times closest to  $\vec{V}_{ref}$ . Using the example when the reference vector  $\vec{V}_{ref}$  is in sector 1 of the hexagon in Figure 4.2,  $\vec{V}_{ref}$  is expressed as [165]:

$$\vec{V}_{ref} T_s = \vec{V}_1 T_1 + \vec{V}_2 T_2 + \vec{V}_0 T_0 \quad (4.5)$$

where  $T_1$ ,  $T_2$  and  $T_0$  are dwell times of voltage vectors  $\vec{V}_1$ ,  $\vec{V}_2$  and  $\vec{V}_0$  respectively. Considering  $\vec{V}_{ref}$  in sector 1, the reference voltage vector and the three voltage vectors are expressed as:

$$\begin{aligned} \vec{V}_{ref} &= V_{ref} (\cos \theta + j \sin \theta); \vec{V}_1 = V_{dc}; \\ \vec{V}_2 &= V_{dc} (\cos \pi/3 + j \sin \pi/3); \vec{V}_0 = \vec{V}_7 = 0 \end{aligned} \quad (4.6)$$

Substituting (4.6) into (4.5) gives:

$$V_{ref} (\cos \theta + j \sin \theta) T_s = T_1 V_{dc} + T_2 V_{dc} (\cos \pi/3 + j \sin \pi/3). \quad (4.7)$$

$$\text{Real components: } \frac{V_{ref}}{V_{dc}} T_s \cos \theta = T_1 + T_2 \cos \pi/3. \quad (4.8)$$

$$\text{Imaginary components: } \frac{V_{ref}}{V_{dc}} T_s \sin \theta = T_2 \sin \pi/3. \quad (4.9)$$

Substituting the solution of  $T_2$  into (4.7),  $T_1$  is evaluated as:

$$T_1 = \frac{2T_s V_{ref}}{\sqrt{3} V_{dc}} \sin(\pi/3 - \theta); \text{ and } T_2 = \frac{2T_s V_{ref}}{\sqrt{3} V_{dc}} \sin \theta. \quad (4.10)$$

The dwell time for the zero switching state vector is expressed as:

$$\begin{aligned} T_0 &= T_s - T_1 - T_2 \\ &= T_s \left( 1 - \frac{2V_{ref}}{\sqrt{3} V_{dc}} \sin(\pi/3 + \theta) \right). \end{aligned} \quad (4.11)$$



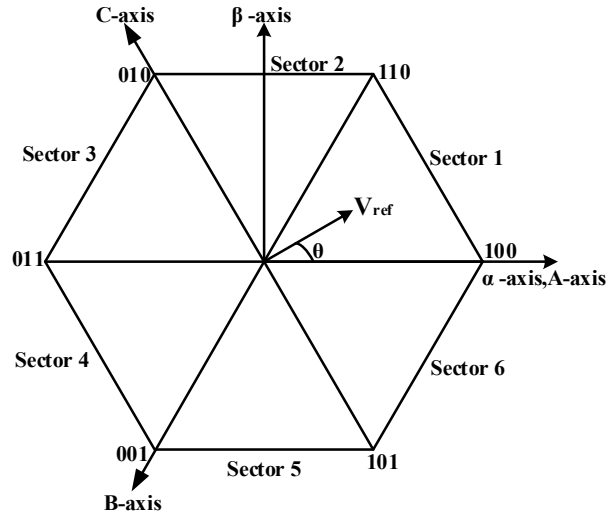


Figure 4.1: Two-level SVM scheme showing voltage vectors.

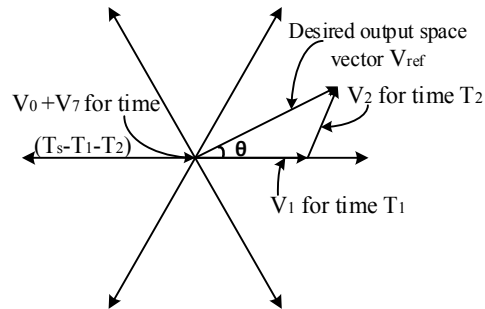


Figure 4.2: Creation of the desired output space vector with nearest three switching vectors.

To implement the Space vector modulation technique either a symmetrical method or a two-phase method is used. For the two-phase method, two zero switching vectors,  $\vec{V}_0$  and  $\vec{V}_7$  are applied either at the beginning or the end of each  $T_s/2$  switching period. In particular, if  $\vec{V}_7$  is applied at the end for all odd sectors and for even sectors,  $\vec{V}_0$  is applied at the beginning. Using the symmetrical method, both zero vectors are used at the beginning or at the end of a half switching period alternatively, e.g. if  $\vec{V}_0$  is used at the beginning of  $T_s/2$  then  $\vec{V}_7$  is applied at the end. In the second half cycle  $\vec{V}_7$  is applied first and  $\vec{V}_0$  is used at the end as shown in Figure 4.3(b). Figure 4.3 shows the space vector modulation vector patterns for the first sextant under both two-phase and symmetrical methods. It is claimed that the symmetrical method offers better output waveform quality while the two-phase method provides reduced switching losses [177-179].

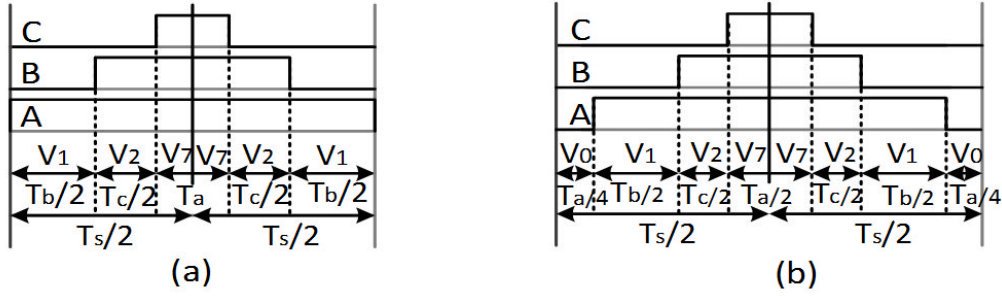


Figure 4.3: Vector sequence for the (a) Two-phase and (b) symmetrical method in the first sextant.

## 4.2 Space Vector Modulation for Multilevel Converters

Extending the two-level hexagon approach for controlling the multilevel inverters [173] leads to an increased number of switching state vectors and hence the increase in control complexity [171-173, 180-182]. For example, considering a three-phase FC-MMCC formed by two cascaded full-bridge FCC modules per phase leg, so regarding as two voltage tiers. Each leg's left-hand-side (LHS) half-bridge FCs A<sub>1</sub>, B<sub>1</sub> and C<sub>1</sub> forms a three-phase 5-level converter which has 125 switching state vectors hexagon constellation as shown in Figure 4.5(a). The same applies to the RHS A<sub>2</sub>, B<sub>2</sub> and C<sub>2</sub>. For either LHS or RHS converters, the overall vector boundary still has a hexagonal form, with vertices being the full voltage in each phase. For choosing the switch states to control the converter and calculating their corresponding duty ratios, the angular position of reference voltage  $\vec{V}_{ref}$  at every sample time instant has to be identified. This can be difficult due to the extended hexagon. One method is to divide each of the six hexagon sectors into multiple equal triangles, and check which triangle encircles the vertex of  $\vec{V}_{ref}$ . Naturally as the number of voltage levels increases, the numbers of both the switching vectors and triangle sections increases. The 5-level hexagon has 96 triangular regions over six sectors with 16 small triangles per sector as shown in Figure 4.5(a) and (b). In general, if  $n$  is the number of voltage levels (from 0 to +V<sub>max</sub> or -V<sub>max</sub> to 0) per phase limb, the total numbers of triangular regions,  $n_T$ , is:

$$n_T = 6(n - 1)^2 \quad (4.12)$$

and the number of switch states,  $n_V$ , required to synthesize a reference voltage for an  $n$ -level converter structure is:

$$n_V = n^3. \quad (4.13)$$

Consequently, the modulation process, involving reference vector region determination, switch states selection, and later duty cycle calculation,

becomes complicated and time-consuming. Also, it is difficult to determine the sequence of switch states to simultaneously obtain capacitor voltage balancing (i.e. inner flying capacitors for 5L-FCC), minimum switching loss and harmonic reductions at a low switching frequency.

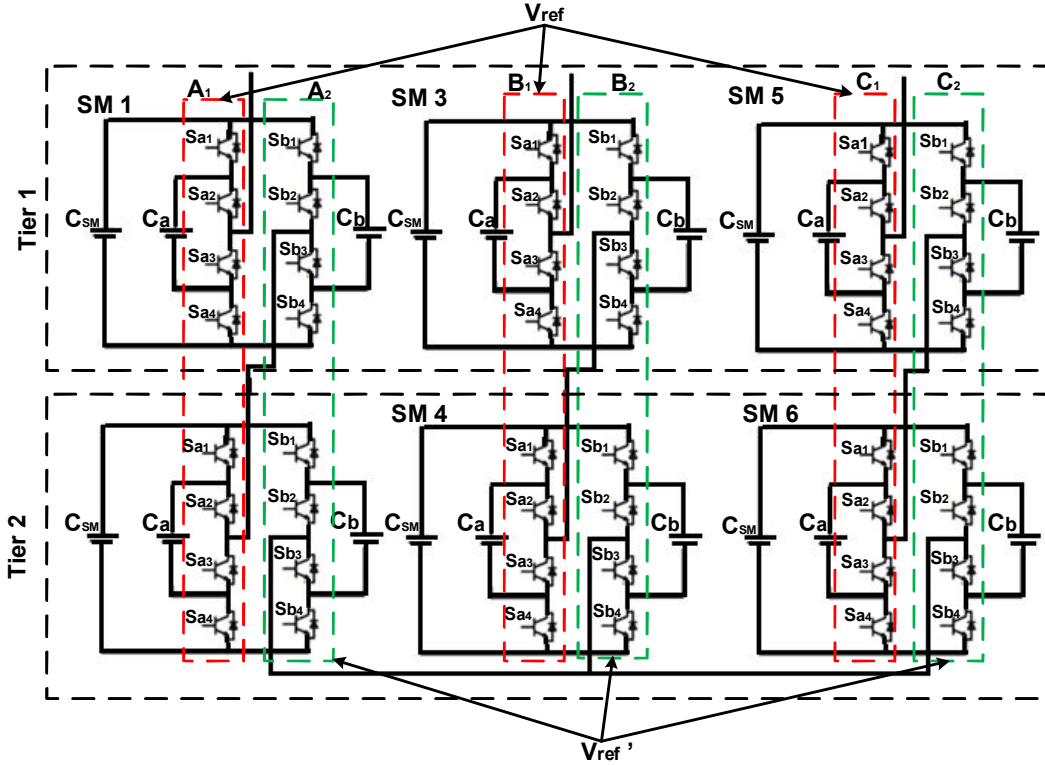


Figure 4.4: 5-level hexagon SVM implementation on two cascaded 5-Level FCC.

Also like the carrier-based PWM method in Chapter 3, unipolar switching technique may be applied, so two reference voltage vectors are identified across the sectors during every switching instant. For the two cascaded 5-level FCC shown in Figure 4.5, 9-level hexagon will be required to control the cascaded 9-level FC-MMCC, to reduce the ease of implementation a 5-level hexagon having two reference voltage vectors  $\vec{V}_{ref}$  and  $\vec{V}_{ref}'$  that are antiphase to each other are applied as shown in Figure 4.6, where each reference voltage vectors commences in sector 5 and 2. Table 4.1 shows the regions corresponding to each modulation index range. Table 4.2 highlights the complex conditions used in selecting each region based on the reference voltage decompose into its  $\alpha$ - $\beta$  vector magnitude as defined in equations (4.18)-(4.19). Figure 4.7 shows how the triangular regions within each sector is determined using a reference voltage vector  $\vec{V}_{ref}$  having a modulation index ranging within  $0.75 \leq m_a \leq 1$ .

Table 4.1: Region selection based on  $m_a = V_{ref}/V_{dc}$

Modulation index $m_a$	Regions
$0.75 \leq m_a \leq 1$	$R_1 \rightarrow R_7$
$0.5 < m_a \leq 0.75$	$R_8 \rightarrow R_{12}$
$0.25 < m_a \leq 0.5$	$R_{13} \rightarrow R_{15}$
$0 < m_a \leq 0.25$	$R_{16}$

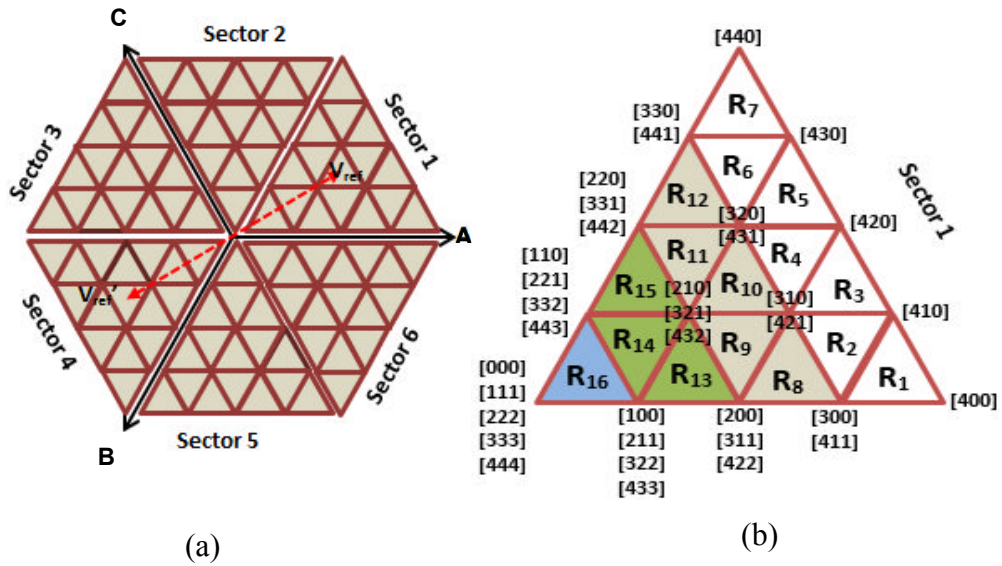


Figure 4.5: Conventional Multilevel-SVM (a) Hexagon for a 5-level SVM and (b) Sector 1 of the 5-level hexagon.

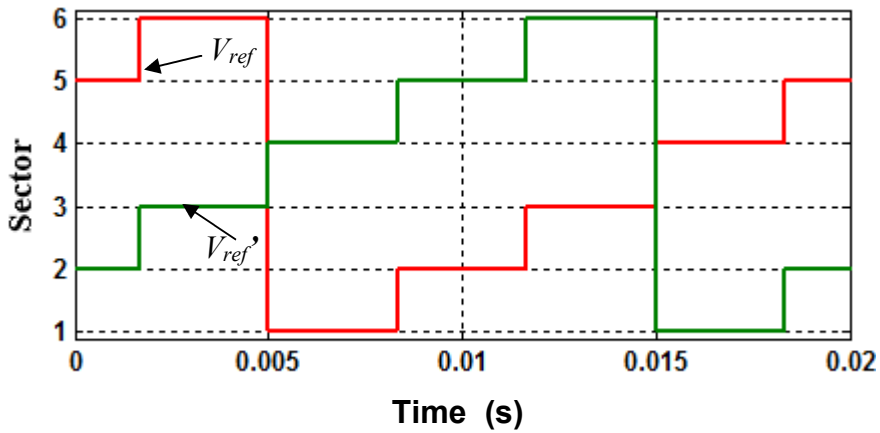


Figure 4.6: Sector identification for 5-level hexagon reference vectors.

Table 4.2: Selection criteria for regions  $R_1 \rightarrow R_7$

Criteria	Regions
$V_{s\alpha} > 0.75, V_{s\beta} < 0.25$	$R_1$
$0.5 < V_{s\alpha} < 0.75, V_{s\beta} < 0.25, V_{s\alpha} + V_{s\beta} > 0.75$	$R_2$
$0.5 < V_{s\alpha} < 0.75, 0.25 < V_{s\beta} < 0.5$	$R_3$
$0.25 < V_{s\alpha} < 0.5, 0.25 < V_{s\beta} < 0.5$	$R_4$
$0.25 < V_{s\alpha} < 0.5, 0.5 < V_{s\beta} < 0.75$	$R_5$
$V_{s\alpha} < 0.25, 0.5 < V_{s\beta} < 0.75, V_{s\alpha} + V_{s\beta} < 0.75$	$R_6$
$V_{s\alpha} < 0.25, V_{s\beta} > 0.75$	$R_7$

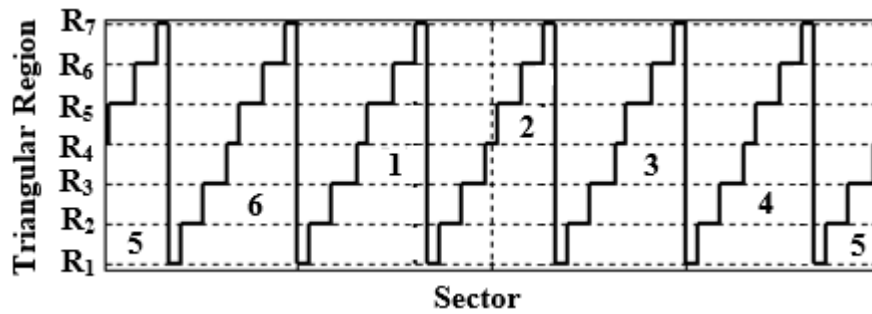


Figure 4.7: Region selection for  $m_a > 0.75$ .

### 4.3 Overlapping Hexagon Space Vector Modulation

This new space vector modulation scheme developed by the author simplifies the modulation procedure greatly for multilevel converters. There are two methods of implementation depending on the type of hexagons used.

#### 4.3.1 Using Two-level Hexagon

This is particularly suitable for MMCCs comprising 3-L H-bridge sub-modules. It uses multiple two-level hexagons as shown in Figure 4.1. Each of them defines the switch states of 3-L H-bridge sub-modules in one tier as seen in Figure 4.8. As mentioned each H-bridge sub-module consists of two 2-level half-bridges, there are six of them in a tier, forming two three-phase two-level inverters, LHS and RHS ones. While the LHS one synthesizes a reference voltage vector  $\vec{V}_{ref}$  the RHS one synthesizes its  $180^\circ$  counterpart  $\vec{V}_{ref}'$ , both are in one two-level hexagon for determining the switch states of all switches

in one tier. For an MMCC of 3-L H-bridge having four cascaded tiers and generating 9-level voltage, a total of 4 hexagons are required which are projected on one pair of  $\alpha$ - $\beta$  axes as shown in Figure 4.9.

The two-level hexagons can also be used for MMCC with 5-L FC modules as shown in Figure 4.4. Though in this case there are only two tiers, each uses two hexagons and in total four hexagons are needed. These hexagons are all on the same  $\alpha$ - $\beta$  axes and are phase shifted from each other by an angle  $\alpha_{SH}$  determined by the fundamental reference signal period  $T$ , and sample period,  $T_s$ , and the number of complementary switches per phase limb  $n_{mp}$ , as [183]:

$$\alpha_{SH} = \frac{\left( \frac{T_s}{2n_{mp}} \right)}{T} \times 360^\circ . \quad (4.14)$$

Assuming the ratio of the sampling period to the fundamental period is 1/5, (4.14) gives the phase shift between each overlapping hexagons  $(360^\circ/8)/5=9^\circ$ , resulting in a 2-D representation that contains four interleaved hexagons. It is worth noting that each sub-module consists of two 2-level or two 3-level half-bridges, there been six of them in a tier.

Because of the phase shift between hexagons, the angular positions of both  $\vec{V}_{ref}$  and  $\vec{V}_{ref}'$  in each hexagon are also different. Taking the hexagon for the lowest tier as the reference with angular value  $\theta$ , that for the  $m^{th}$  tier is given as:

$$\theta_m = (\theta - (m - 1)\alpha_{SH}) \text{ rad} , \quad (4.15)$$

while  $\vec{V}_{ref}'$  is displaced by  $180^\circ$  from  $\theta_m$ .

#### 4.3.1.1 Sector identification

Implementation of OH-SVM involves, firstly, determination of exact locations of the reference voltage vectors, hence the switch states to be applied for each tier. This requires identifying the sector number, according to the reference voltage vector phase angle  $\theta_m$ , at every sample time instant in a 2-level hexagon. With multiple overlapped hexagons the sector numbers of the reference voltage vector for each hexagon may be different at certain sample instants. This can be obtained from the expression in (4.16) which shows the Euclidean division of the perceived angle ( $\theta_m$ ) by the sector angle ( $60^\circ$  or  $\pi/3$ ), where  $S_N$  represents the current sector number. Figure 4.10 shows the phase shift between reference voltage vectors for each 2-level hexagons, where each four of the hexagons have 4 reference voltage vectors ( $V_{ref}$ ,  $V_{ref1}$ ,  $V_{ref2}$  and  $V_{ref3}$ ) and anti-phase ( $V_{ref}'$ ,  $V_{ref1}'$ ,  $V_{ref2}'$  and  $V_{ref3}'$ ) for controlling its LHS and RHS switches.

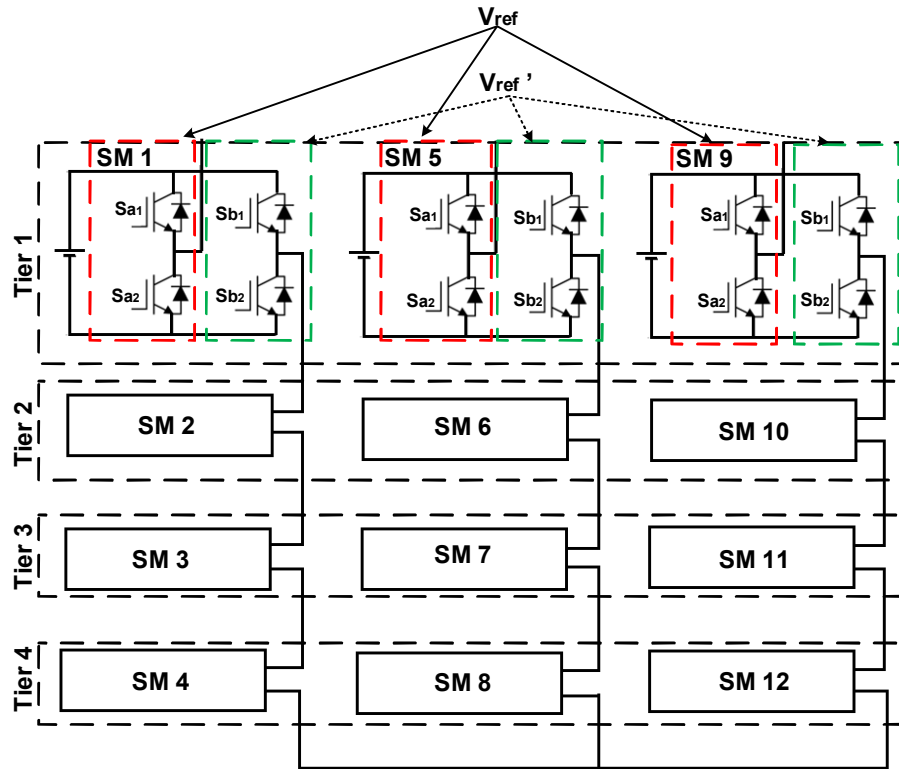


Figure 4.8: Schematic diagram of a MMCC with four cascaded 3-L H-bridges.

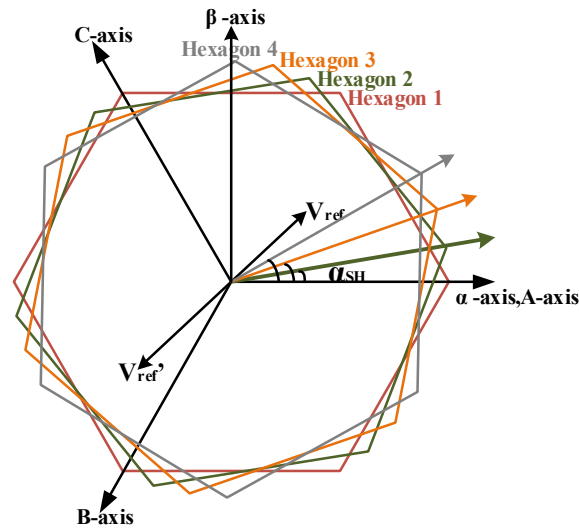


Figure 4.9: Two-level hexagon for OH-SVM highlighting phase shift between each hexagons.

$$\theta_m / (\pi / 3) = (S_N - 1) \pi / 3 + \theta_m \bmod \pi / 3 . \quad (4.16)$$

According to magnitudes and angles of  $\vec{V}_{ref}$  and  $\vec{V}_{ref}'$  the switching vectors for these modules and their respective duty ratios at each sample instant can be calculated by applying the well-known two-level SVM technique as discussed in section 4.1. Clearly using the two-level hexagons it simplifies the modulation algorithm as compared to using five-level hexagons; since the former

comprises only 8 switch states, there are no multiple triangular regions per sector, hence no need to find which one of the sixteen triangles containing the reference vectors of  $\vec{V}_{ref}$  and  $\vec{V}_{ref}'$ .

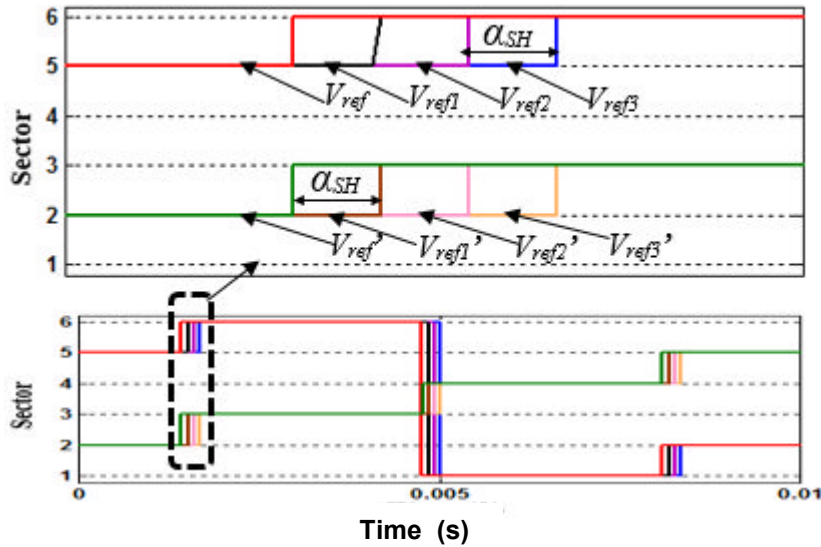


Figure 4.10: Sector identification for 2-level hexagon reference vector.

Figure 4.11 shows the flowchart for implementing the OH-SVM using 2-level hexagons. The control variables are initialized by first computing the overlapping angle between the hexagons. The  $\alpha_{SH}$  aids in the determination of the sectors in which the reference voltage vectors lie in each hexagon. Once the sector is identified, the dwell times of the three closest voltage vectors are calculated and applied to control the converter switches.

### 4.3.2 Using Three-level Hexagons

For FC-MMCC modulation, three-level hexagon can also be used. In this case, one tier comprises six FC half-bridge, hence having two three-phase FCCs, as shown in Figure 4.4. For a three-level hexagon there are 27 switching state vectors as shown in Figure 4.12(a). And sector one is given in Figure 4.12(b). Naturally, for MMCC in Figure 4.4 with only two tiers, two such hexagons are needed, both are projected on a pair of  $\alpha$ - $\beta$  axes as shown in Figure 4.12(c). The phase shifts between these overlapping 3-level hexagons are evaluated using the same formula (4.14) from each other by an angle  $\alpha_{SH}$  determined by the fundamental reference signal period  $T$ , and sample period,  $T_s$ , and the number of two complementary switching pair per phase are referred as  $n_{mp}$ , where as in the 2-level hexagon one complementary switching pair per phase is used [183].

Again if the ratio of the sampling period to the fundamental period is 1/5, according to (4.14)  $\alpha_{SH} = (360^\circ/4)/5 = 18^\circ$ , resulting in a 2-D representation that contains two interleaved 3-level hexagons. This shows that the overlapping



angle for the 3-level hexagon is twice the 2-level hexagon case. Due to the phase shift between hexagons, the angular positions of both reference voltage vectors in each hexagon are also different and are evaluated using (4.15).

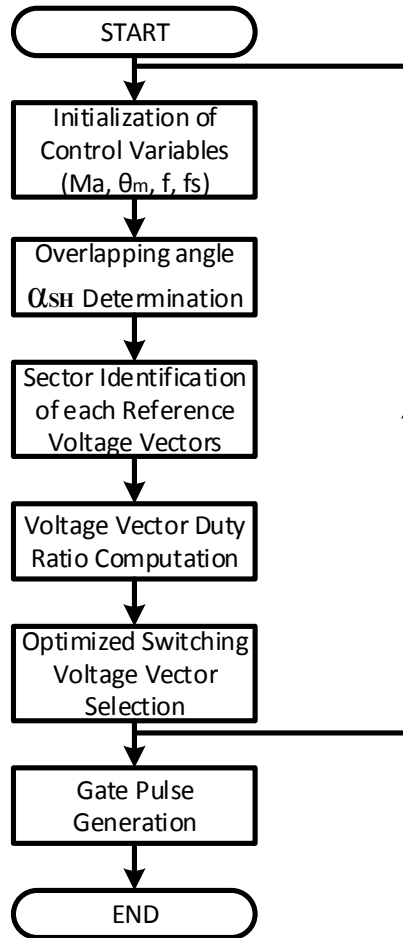


Figure 4.11: Flowchart for 2-level hexagon implementation.

#### 4.3.2.1 Sector identification

Compared to the case when using two-level hexagon in subsection 4.3.1, this is more complicated. Firstly, it still requires determining exact locations of the reference voltage vectors, hence the switch states to be applied to switches in each tier. However, this involves identifying the sector number and also locating its vertex in one of the four triangles within the sectors at every time instant. Identification of sector where each reference voltage vector lies can be determined using (4.16). Figure 4.13 shows the phase shift between reference voltage vectors between ( $V_{ref}$  and  $V_{ref1}$ ) and anti-phase reference voltage vector ( $V_{ref}'$  and  $V_{ref1}'$ ) to be  $2\alpha_{SH}$  between each 3-level hexagons.

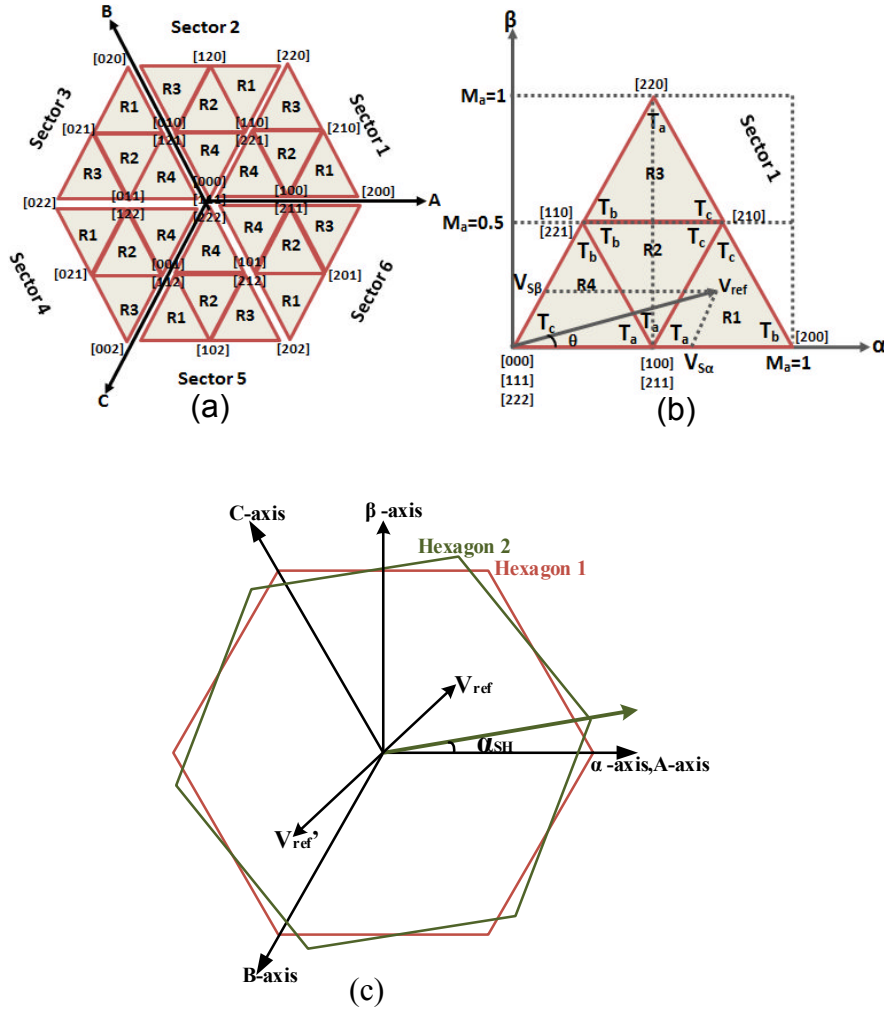


Figure 4.12: 3-level hexagon for OH-SVM (a) all sectors and reference voltages (b) region detection in sector 1 (c) phase shift between two hexagons.

#### 4.3.2.2 Region selection

To find which triangular region in the chosen sector has the reference voltage vectors, considering  $\vec{V}_{ref}$ , this is resolved into sector edge components ( $V_{S\alpha}$ ,  $V_{S\beta}$ ) which are shown in Figure 4.12(b) and expressed in (4.17) and (4.18) below.

$$V_{S\alpha} = \frac{V_{ref}}{2V_{DC}} \left[ \cos \theta_m - \frac{\sin \theta_m}{\sqrt{3}} \right]. \quad (4.17)$$

$$V_{S\beta} = \frac{V_{ref}}{V_{DC}} \frac{\sin \theta_m}{\sqrt{3}}. \quad (4.18)$$

The values estimated above are then used to identify the relevant triangle according to rules given in Table 4.3. For  $m_a > 0.5$  the regions are seen to be selected between 1, 2 and 3 see Figure 4.14.

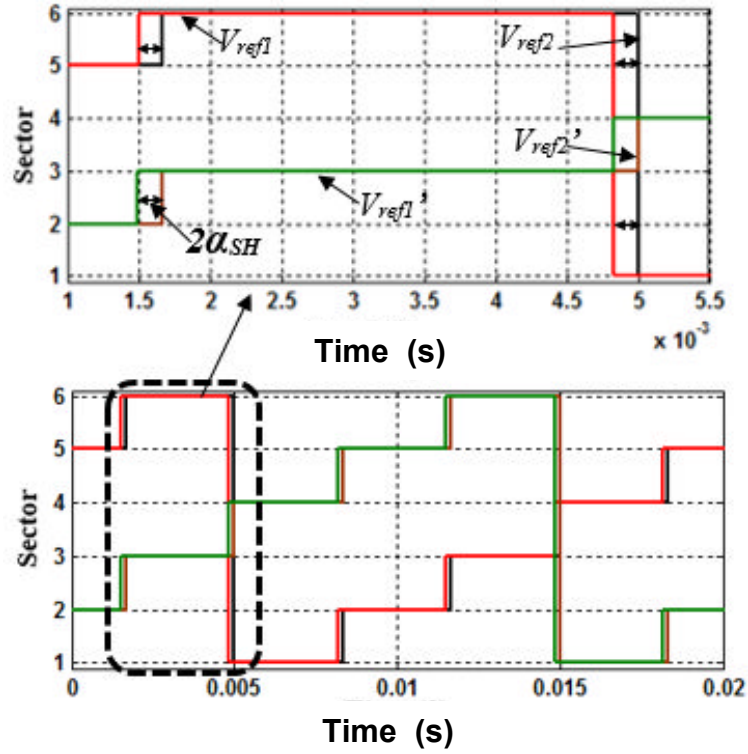


Figure 4.13: Sector identification of reference voltage vectors in a 3-level hexagon.

Table 4.3: Region selection Criteria ( $M_a = V_{ref} / V_{DC}$ )

Region1	Region 2	Region3	Region 4
$V_{S\alpha} > 0.5M_a$	$V_{S\alpha} < 0.5M_a$ $V_{S\beta} < 0.5M_a$ $ V_{S\alpha} + V_{S\beta}  > 0.5M_a$	$V_{S\beta} > 0.5M_a$	$V_{S\alpha} < 0.5M_a$ $V_{S\beta} < 0.5M_a$ $ V_{S\alpha} + V_{S\beta}  < 0.5M_a$

Once the correct triangle region is identified, the switch states suitable for synthesizing  $\vec{V}_{ref}$  can be determined as the three vectors located closest to the vertices of the chosen region. However for an MMCC with 5L-FC sub-modules, each location corresponds to four switch states; two of these are independent but the other two give the same voltage level with different switch states, due to the inner floating capacitors in the module. For example, the switching vectors for sector 1, region 1 are 200, 210, 100 and 211 shown in Figure 4.12(b). The latter two create redundancy and only one is chosen to re-balance the floating capacitor voltage. The corresponding three duty cycles,  $T_a$ ,  $T_b$  and  $T_c$  are calculated using formulae in Table 4.4 for every sample instant of duration  $T_s$  and must satisfy the condition:

$$T_s = T_a + T_b + T_c. \quad (4.19)$$

### 4.3.2.3 Optimal switching state/voltage vector selection

The sequence of implementing the switch states requires careful consideration, particularly for a 5L-FC module. The requirements are to make sure a good output waveform, keep up natural balancing of the floating capacitor voltages and have the least number of switches changing states per sample.

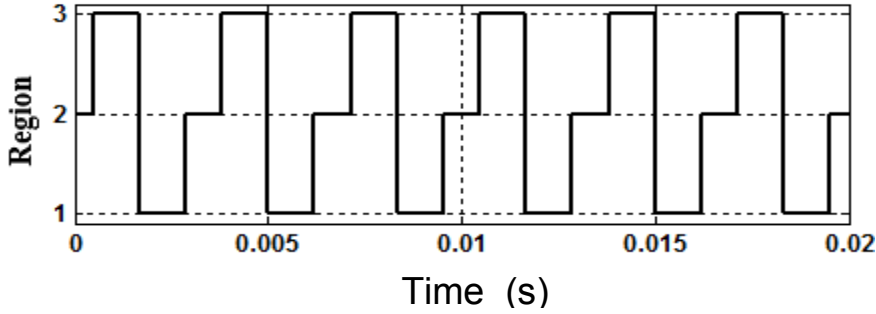


Figure 4.14: Region selection for  $m_a > 0.5$ .

Table 4.4: Duty Cycle calculation formulae

Region 1	Region 2
$T_a = 2T_s \left( 1 - \frac{V_{ref}}{\sqrt{3}V_{DC}} \sin \left( \frac{\pi}{3} + \theta_m \right) \right)$	$T_a = T_s \left( 1 - \frac{2V_{ref}}{\sqrt{3}V_{DC}} \sin \theta_m \right)$
$T_b = T_s \left( \frac{2V_{ref}}{\sqrt{3}V_{DC}} \sin \left( \frac{\pi}{3} + \theta_m \right) - 1 \right)$	$T_b = 2T_s \left( 1 - \frac{V_{ref}}{\sqrt{3}V_{DC}} \sin \left( \frac{\pi}{3} + \theta_m \right) \right)$
$T_c = T_s \left( \frac{2V_{ref}}{\sqrt{3}V_{DC}} \sin \theta_m \right)$	$T_c = T_s \left( \frac{2V_{ref}}{\sqrt{3}V_{DC}} \sin \left( \frac{\pi}{3} - \theta_m \right) - 1 \right)$
Region 3	Region 4
$T_a = T_s \left( \frac{2V_{ref}}{\sqrt{3}V_{DC}} \sin \theta_m - 1 \right)$	$T_a = T_s \left( \frac{2V_{ref}}{\sqrt{3}V_{DC}} \sin \left( \frac{\pi}{3} - \theta_m \right) \right)$
$T_b = 2T_s \left( 1 - \frac{V_{ref}}{\sqrt{3}V_{DC}} \sin \left( \frac{\pi}{3} + \theta_m \right) \right)$	$T_b = T_s \left( \frac{2V_{ref}}{\sqrt{3}V_{DC}} \sin \theta_m \right)$
$T_c = T_s \left( \frac{2V_{ref}}{\sqrt{3}V_{DC}} \sin \left( \frac{\pi}{3} - \theta_m \right) \right)$	$T_c = T_s \left( 1 - \frac{2V_{ref}}{\sqrt{3}V_{DC}} \sin \left( \frac{\pi}{3} + \theta_m \right) \right)$

Table 4.5 shows the switching state vector sequence table for implementing the 3-level hexagon SVM where  $L=V_{ref}$  and  $R=V_{ref}'$  denote the vectors used for the LHS and RHS limbs of the full bridge FC converter in a tier over one switching period  $T_s$ . Here  $\vec{V}_{ref}$  is located in sector 1, region 1 and  $\vec{V}_{ref}'$  is

located in sector 4, region 1 of the 3-level hexagon. By convention in SVM,  $T_s$  and calculated switching vector times,  $T_a$ ,  $T_b$ , and  $T_c$  are split in half and arranged as shown in Table 4.5. It can be observed that all floating capacitors of LHS and RHS FC modules are being charged and discharged and vice versa, for an equal number of times within a  $T_s$  cycle. With this approach implemented for all the 24 triangle regions of the 3-level hexagons, optimal natural voltage balancing of the 5L-FC modules can be achieved.

Figure 4.15 shows the flowchart for implementing the 3-level hexagon technique which is similar to that when using the 2-level hexagons as shown in Figure 4.11 except it has an additional part for the region selection.

Table 4.5: Vector combination chart showing optimized selection of switch states for LHS and RHS switches when  $V_{ref}$  in region 1 sector 1 and  $V_{ref}'$  in region 1 and sector 4

where Green=charging state and Red= discharging state

phase		$T_a/4$		$T_b/2$		$T_c/2$		$T_a/4$		$T_a/4$		$T_c/2$		$T_b/2$		$T_a/4$	
		L	R	L	R	L	R	L	R	L	R	L	R	L	R	L	R
Region 1	A	1	0	1	0	1	0	1	1	1	0	1	0	1	0	0	0
		0	0	1	0	1	0	1	0	1	1	1	0	1	0	1	0
	B	0	1	0	1	1	1	1	1	0	1	0	1	0	1	0	0
		0	0	0	1	0	1	0	1	1	1	1	1	0	1	0	1
	C	0	1	0	1	0	1	1	1	0	1	0	0	0	1	0	0
		0	0	0	1	0	0	0	1	1	1	0	1	0	1	0	1
		$T_s/2$						$T_s/2$									
		$T_s$															

#### 4.4 Simulation Studies: Comparison of the Different Space vector Modulation Schemes

To validate the overlapping hexagon SVM for both 2-level and 3-level hexagon methods, the conventional method is compared with the novel schemes in terms of waveform quality, switching losses, natural balancing ability of the inner flying capacitor and computational complexity. In addition, the 2-level hexagon SVM is applied to control four cascaded H-bridges and results are compared with two cascaded FC-MMCC. The 5L-FC and 3L-HB MMCC parameters are shown in Table 4.6.

Figure 4.16 (a)-(g) to Figure 4.17 (a)-(g) show the voltage and current waveforms using 2, 3 OH-SVM schemes and Figure 4.17 (a)-(g) using

classical multilevel SVM. As can be seen, all the schemes lead to the converter generating 9-level (peak to peak) output phase voltages with good harmonic performance. However, the voltage and current waveforms from the 2-level and 3-level OH-SVM show better performance than those from the classical 5-level hexagon, as shown by its phase and line-line voltage waveforms. This is also clear from its phase and line-line voltage THD values which are all lower than the ones from both 3-level and 5-level method as listed in Table 4.7.

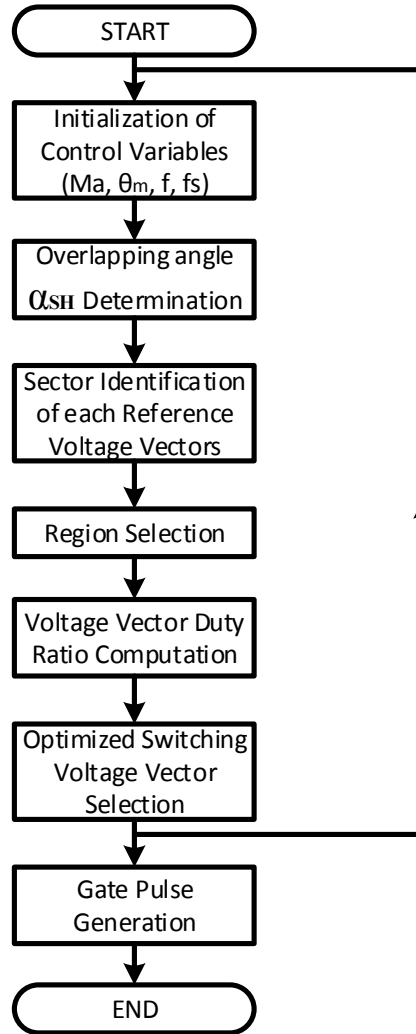


Figure 4.15: Flowchart for 3-level hexagon implementation.

For the phase limb output voltage, the harmonics appear as sidebands around 8, 4 and 2 times the actual switching frequency for 2, 3 OH-SVM and classical multilevel SVM. The harmonic frequency  $f_h$  for the three algorithms are;

Phase voltage using 2-level hexagon:  $f_h = hx f_o = (j8m_f \pm k)f_o$

Phase voltage using 3-level hexagon:  $f_h = hx f_o = (j4m_f \pm k)f_o$

Phase voltage using 5-level hexagon:  $f_h = hx f_o = (j2m_f \pm k)f_o$

where harmonic position,  $j=1, 2, 3\dots$  and sideband index,  $k=1, 3, 5 \dots$  odd number

For line voltage sideband index,  $k=1, 5, 7 \dots$  odd numbers excluding odd multiples of 3.

Table 4.6: 5L-FC and 3L-HB MMCC parameters

Modulation index $m_a$	0.85
Switching frequency $f_s$	1500
Sub-module dc voltage 5L-FC	100V
Sub-module dc voltage 3L-HB	50V
Sub-module inner capacitor dc voltage	50V
Capacitance of inner capacitor	560 $\mu$ F
Resistive load $R$	20 $\Omega$
Inductive load $L$	20mH

The followings are observed from THDs of the three methods,

- 3<sup>rd</sup> order harmonics appear as baseband around the fundamental harmonic in the phase voltage spectrum but are eliminated in the line voltage spectrum.
- Sideband harmonics first appear around the 4<sup>th</sup> and 8<sup>th</sup> multiple of the sampling frequency for both the three-level and two-level hexagons respectively. This is because the two 3-level and four 2-level hexagons are overlapped (i.e. phase shifted) having two anti-phase voltage reference vectors thus making the equivalent sampling frequency of the FC-MMCC to be four and eight times the sampling frequency (i.e. for three-level hexagon:  $f_{sw}=4xf_s$  and for two-level hexagon:  $f_{sw}=8xf_s$ ).

The total harmonic distortion for the phase and line output voltage waveforms are 28.22%, 12.7% for three-level hexagon and 22.89%, 8.47% for the two-level hexagon. The difference in spectra quality for both methods lies in the fact that the three-level hexagon more harmonics which appear as sideband around the 4<sup>th</sup> multiple of the sampling frequency, whilst for the two-level hexagon these harmonics are fewer and only appear as sidebands found around  $8m_f$ .

With the equivalent switching frequency of the 2-level hexagon OH-SVM being 2 and 4 times higher than the 3-level hexagon OH-SVM and classical multilevel SVM respectively, the switching losses incurred by the former is greater. Also, this equivalent switching frequency effect ensures operating at lower switching frequencies and still achieving the good waveform quality.

With an adequate selection of the sequences of voltage vectors, both the 3-level hexagon OH-SVM and classical multilevel SVM ensure natural voltage balancing of inner floating capacitors. But the capacitor voltage fluctuations when using the 2-level hexagon are seen to be lowest, followed by the 3-level hexagon and 5-level hexagon with values being  $\pm 1.2\%$ ,  $\pm 3\%$  and  $\pm 20\%$  respectively. This is attributed to the overlapping nature of both 2 and 3-level OH-SVM.

The nature of the conventional multilevel SVM, proper selection of the switch state vectors in balancing inner capacitor voltage of the 5L-FC results in switch state transition exceeding one voltage level. The solution is to use either the 2-level or 3-level OH-SVM. The results of Figure 4.16(a) and 4.17(a) confirm this.

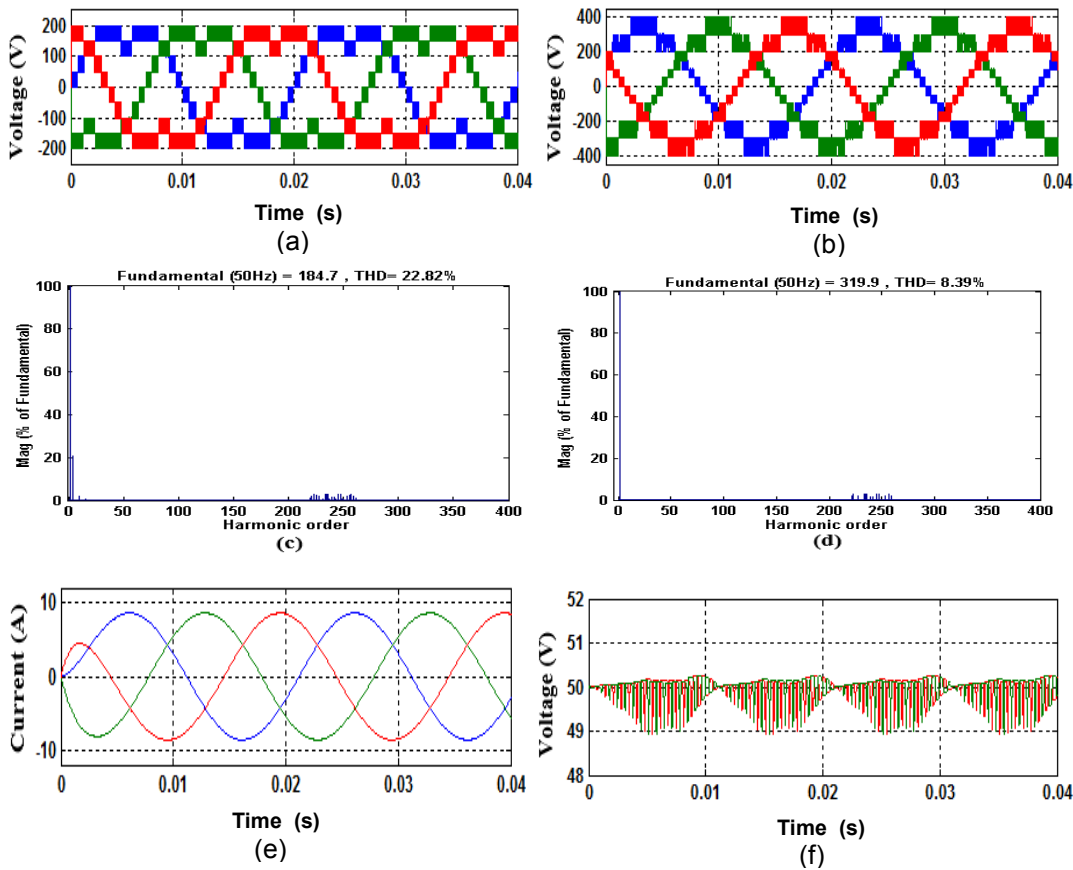


Figure 4.16: 2-level OH-SVM for MMCC with 5L-FCC; (a) Phase voltage, (b) Line voltage, (c) Phase voltage THD, (d) Line voltage THD(e) Load current(f) Inner flying capacitor voltage.



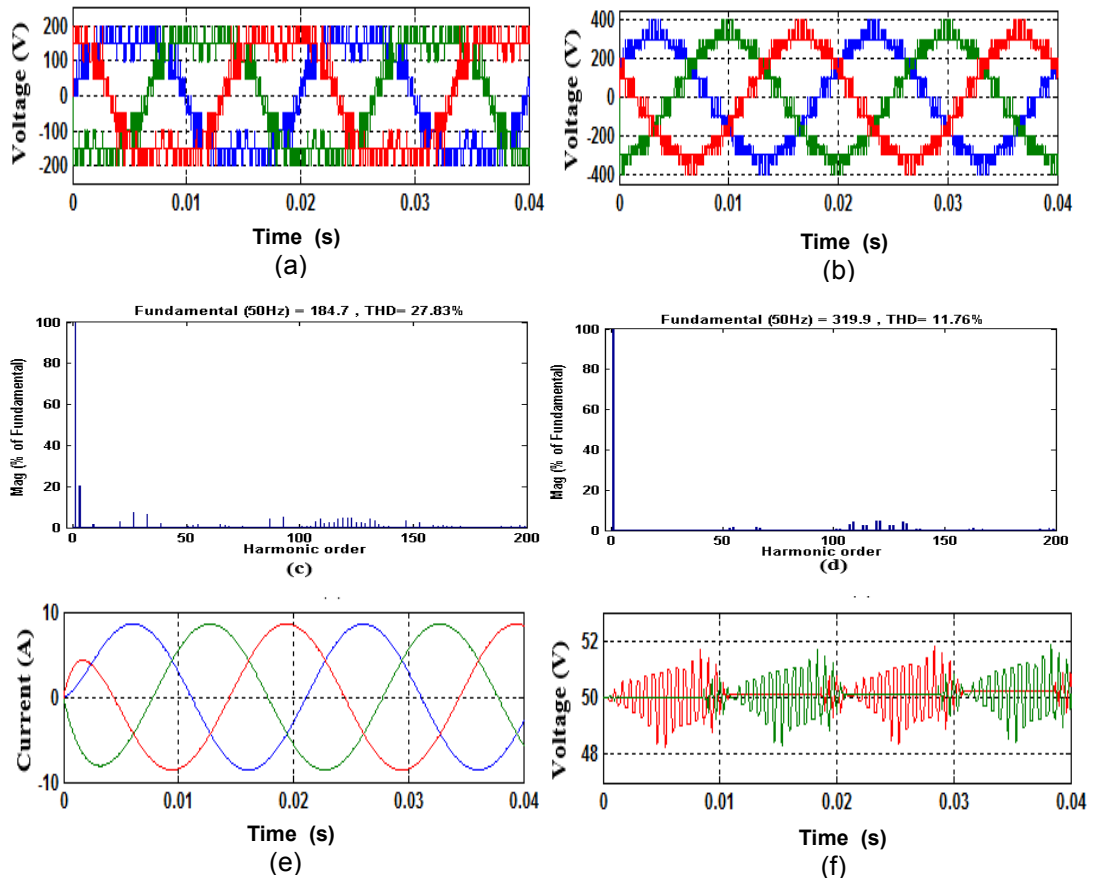


Figure 4.17: 3-level OH-SVM for MMCC with 5L-FCC; (a) Phase voltage, (b) Line voltage, (c) Phase voltage THD, (d) Line voltage THD (e) Load current (f) Inner flying capacitor voltage.

Based on the SIMULINK models, the computational load for each SVM algorithm is compared and listed in Table 4.8. According to the sum of arithmetic operations, such as addition, subtraction, division, multiplication and trigonometric functions, the classical multilevel SVM requires the highest computational burden amongst three, the 2-level OH-SVM is the most computationally efficient method.

Table 4.7: Comparison of OH-SVM Schemes

Phase shifted-SVM schemes	2-level hexagon	3-level hexagon	Conventional SVM
Phase voltage THD (%)	22.82	27.83	37.04
Line voltage THD (%)	8.39	11.76	16.39
Phase Current THD (%)	2.35	2.50	3.79
FC voltage Variation (%)	±1.2	±3	±20

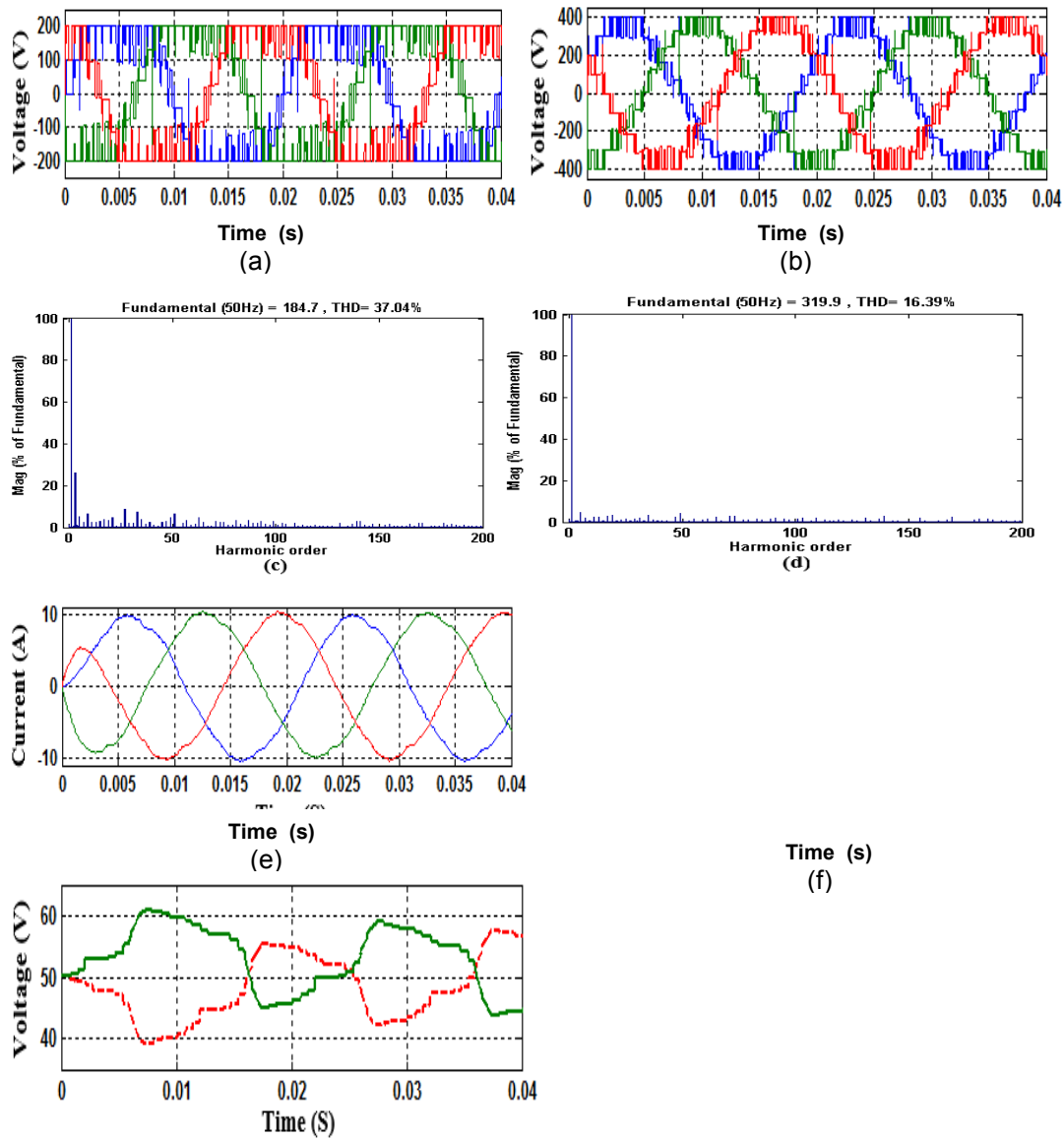


Figure 4.18: Conventional SVM for MMCC with 5L-FCC; (a) Phase voltage, (b) Line voltage, (c) Phase voltage THD, (d) Line voltage THD (e) Load current and (f) Inner flying capacitor voltage.

Table 4.8: Computational Comparison of SVM schemes

Computational Task in each section	2-level hexagon	3-level hexagon	Conventional SVM
$V_{ref}$ & $V_{ref}$ ' angle	8	4	2
Sector Selection	8	4	2
Region Selection	-	96	384
Duty Ratio	144	288	576

Total	160	392	964
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Comparisons of MMCCs built using either 3L-HB or 5L-FC while controlled by the same 2-level OH-SVM scheme are carried out. Figure 4.19 (a)-(e) shows results from the 3L-HB modules and compared with that in Figure 4.16 for 5L-FC sub-modules, they show similar performance in terms of waveform quality.

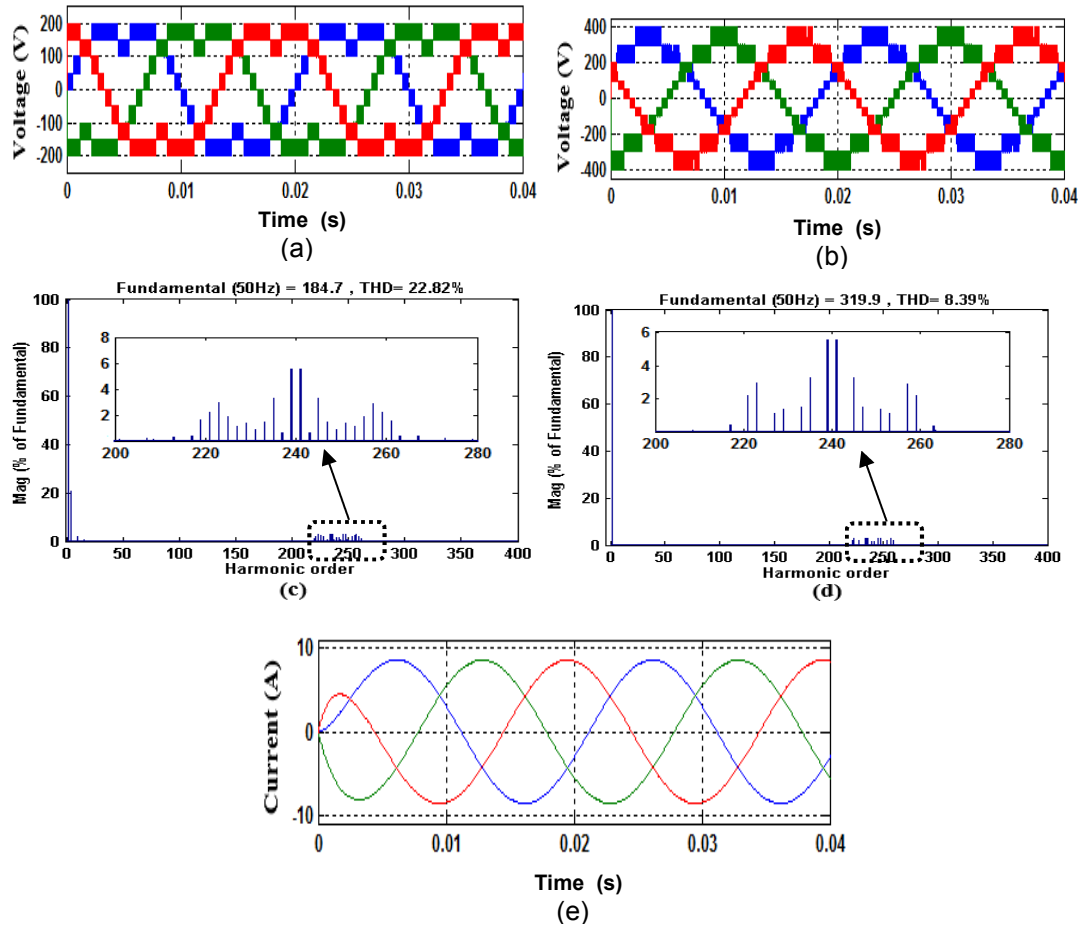


Figure 4.19: 2-level OH-SVM for MMCC with 3L-HB; (a) Phase voltage, (b) Line voltage, (c) Phase voltage THD (d) Line voltage THD and (e) current waveform.

### 4.5 Experimental Validation of 2-level Overlapping Hexagon Space Vector Modulation

An experimental MMCC with 3L H-bridge modules is used in verifying the 2 level hexagon OM-SVM scheme. This consists of eZdspF28335 board from Spectrum Digital which synthesizes the PWM signals and fed through gate drivers to drive two cascaded 3-L H-bridges. The two cascaded 3-L H-bridge making up this topology uses the IFR740IGBT switches, each rated at 400V, 10A and IGBT bypass diodes rated 45V, 10A. Experimental setup of the MMCC is illustrated in Figure 4.20. The converter was supplied from isolated dc sources obtained from laboratory power supplies.

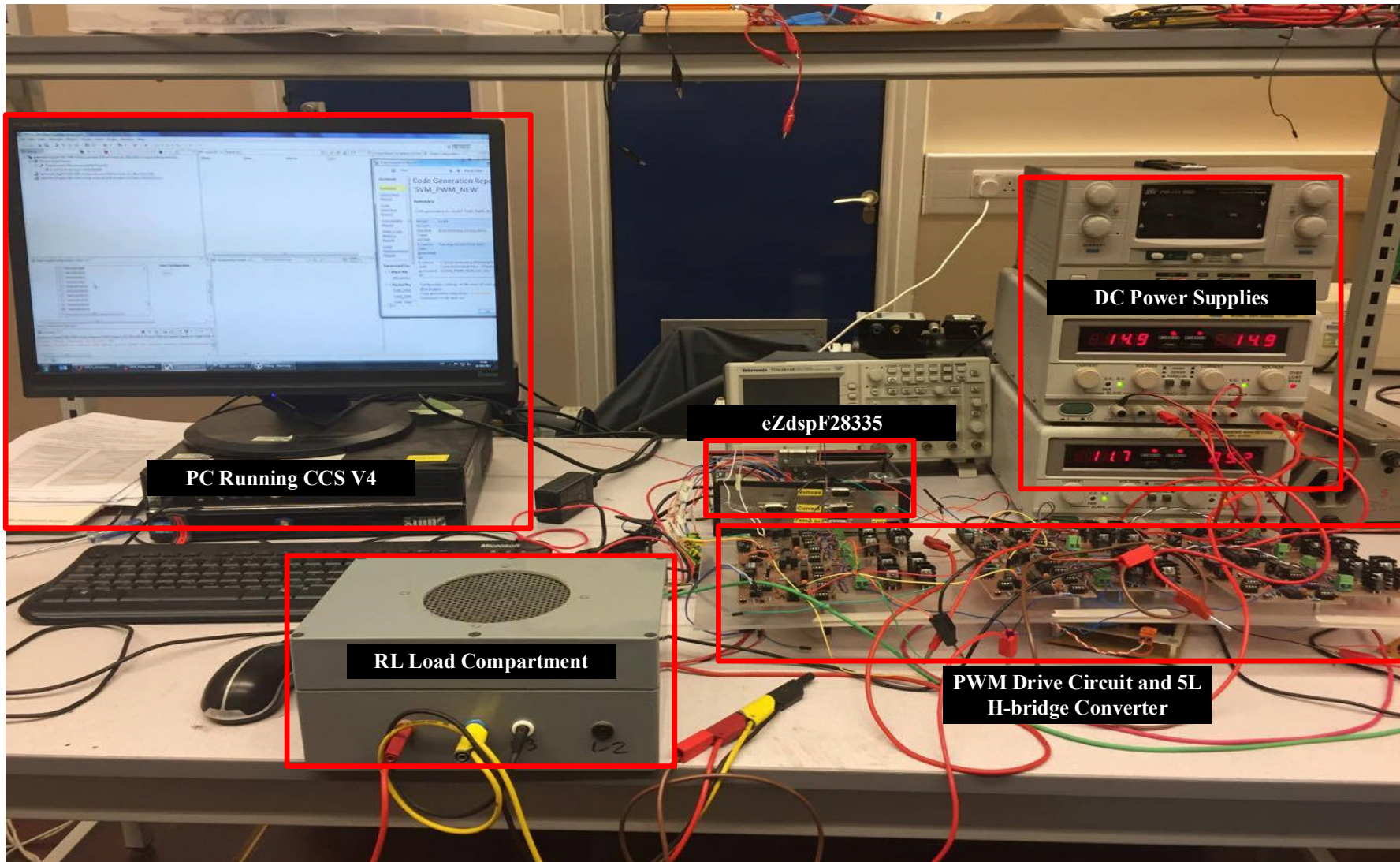


Figure 4.20: MMCC experimental setup.

### 4.5.1 PWM Generation

The eZdspF28335 board Spectrum digital is a DSP controller chosen to generate the PWM signals to control the cascaded H-bridges. The eZdspF28335 board features include [184]; 32-bit floating point unit, 68 kB RAM, 512 kB Flash Memory, 150 MHz operating frequency, 12-bit ADC having 16 input channels, Embedded USB JTAG and 18-channel enhanced PWM output (ePWM). This board was chosen because of its fast processing speed and Rapid Control Prototyping (RCP) capability [184]. The latter enables the developer to write control algorithm in function blocks which are graphically structured using Matlab SIMULINK, hence avoiding the slow and tedious process of coding the algorithms in computer languages. The integrated development environment (IDE), i.e. the Code Composer Studio, then, converts the graphically coded algorithm into machine code which can be executed by the DSP controller. This speeds up the development process significantly [185]. A snap shot of eZdspF28335 board is shown in Figure 4.21.

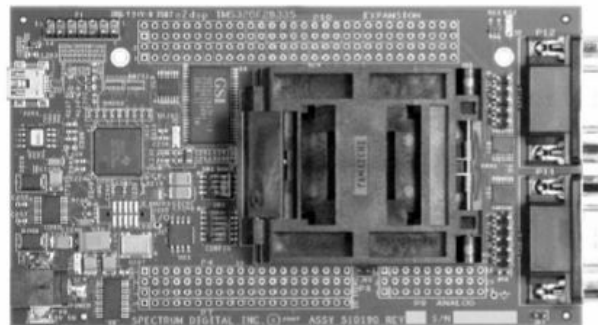


Figure 4.21: Spectrum Digital eZdspF28335 board [184].

With RCP the Matlab SIMULINK PWM algorithm in graphical form can be dedicated to the specific DSP device, i.e. TMS320F28335.

This is by using support packages, the Embedded Coder package, which is added to SIMULINK to utilise the Texas Instrument C2000 toolbox which has the building blocks for simulating the TMS320F28335 on eZdspF28335 board. Once the PWM controller is designed in SIMULINK, it can be compiled using the Embedded Coder Package, and the output file is loaded on the DSP through the CCS and PWM signal can be generated. eZdspF28335 board can be used for implementing many functions but in this case, it is utilized only for generating the pulse width modulated signals. Further information of the eZdspF28335 is found in [184].

### 4.5.2 Experimental Results

The proposed OH-SVM scheme was implemented using the eZdspF28335 board, with a sampling frequency of 400 Hz and modulation index 0.8. The experimental set-up is similar to Figure 4.8 with the exception of two 3L H-bridge sub-modules cascaded per phase. Each module is connected to 20V dc power source. Connected across the three phase of cascaded H-bridge is a balanced R-L load of  $7.5\Omega$  and 10mH. Figure 4.22(a)-(c) show, respectively, the plots of the output phase, and line-to-line voltage waveforms and phase currents.

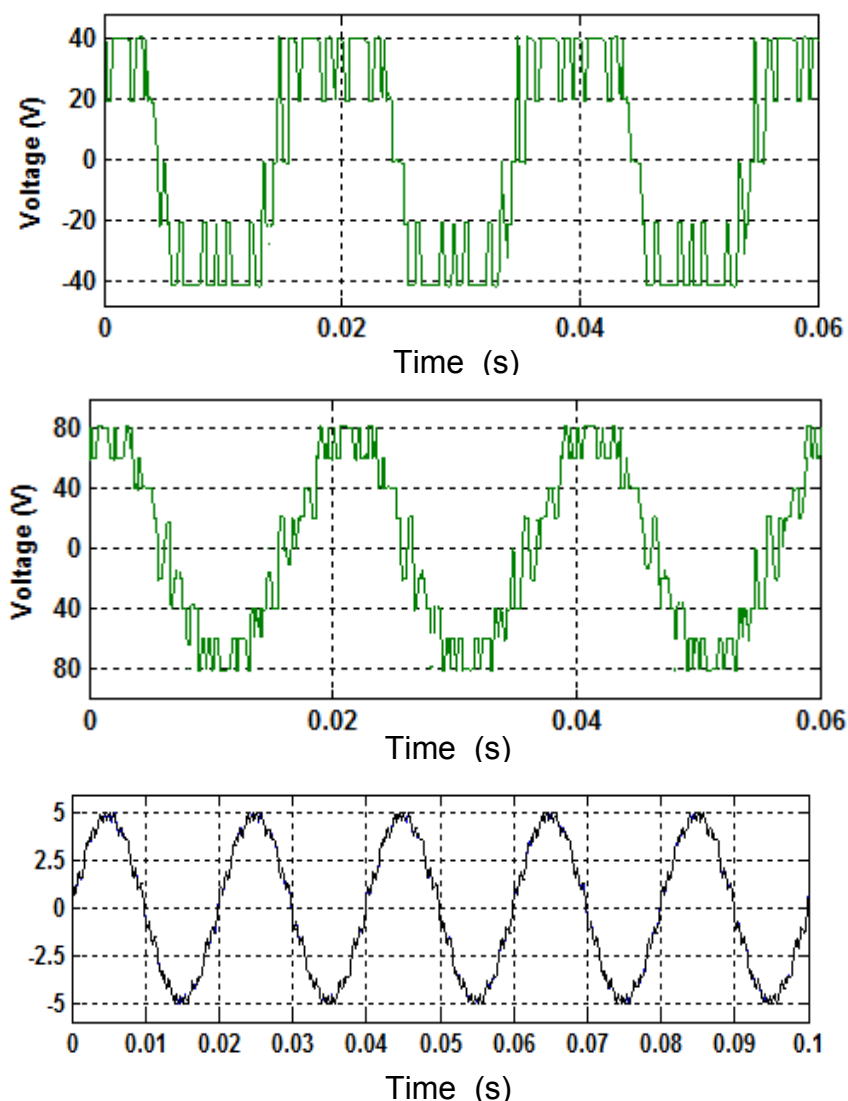


Figure 4.22: Experimental results (a) Two cascaded H-bridge output Phase voltage, (b) Line voltage and (c) phase current waveform.

## 4.6 Summary

This chapter presented a new space vector modulation technique for the control of MMCCs, called overlapping hexagon space vector modulation. The operating principles and implementation procedures of this scheme were described in detail for overlapping multiples of either two-level or three-level hexagons. Comparison of this new scheme with the classical multilevel SVM method has shown its benefits. These include improved voltage and current waveform quality, the ability to maintain inner flying capacitor voltage balancing, particularly for the FC-MMCC, and reduced computation complexity. Considering the application of this OH-SVM with 2-level hexagons to two MMCCs having the same voltage levels, but with one using 5L-FC as the basic module and the other using the 3L H-bridge, the resultant voltage and current waveforms show similar features. Their THD values are comparable. The experimental results of the two cascaded 3L H-bridge sub-modules using the proposed 2L OH-SVM technique validate the simulated results for MMCCs.

## Chapter 5

### FC-MMC Based STATCOM for Power Factor Correction

This chapter explores the FC-MMCC as a STATCOM for power factor correction in power distribution systems. The power flow analysis showing the relationships between voltage sources, namely the sending side voltage, PCC side voltage, a voltage source converter acting as STATCOM, an R-L load and a distribution line impedance, and the condition of achieving zero phase shift between voltage and current at the PCC have been discussed in chapter one. In this chapter, the dc capacitor voltage rating, the sub-module capacitor voltage ripple and the converter filter requirements are also analysed. Also, the use of an FC-MMCC as a STATCOM in single star configuration for a balanced three phase power system is investigated via simulation. Thereafter, power factor correction is experimentally validated using an FC-MMCC based STATCOM. This experimental system is described and the simulation and experimental results are compared.

#### 5.1 Converter Voltage and DC Capacitor Voltage Requirements

The difference between the FC-MMCC output voltage and PCC voltage determines the amount of current flowing between them. For a STATCOM, its power rating is determined by the maximum power it is meant to compensate, this is usually set about 20%-30% of the maximum load power [186, 187]. Since the minimum voltage is restricted by the PCC phase voltage, the current rating of the converter can be determined. The phasor relationship between the STATCOM terminal voltage and PCC voltage and current is shown in Figure 5.1 and 5.2 respectively. The STATCOM converter current relates its terminal voltage and PCC voltage by:

$$\vec{i}_c = \frac{\vec{v}_{PCC} - \vec{v}_c}{R_c + jX_c} \quad (5.1)$$

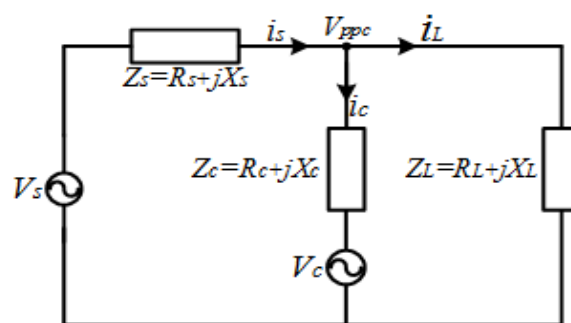


Figure 5.1: Single phase circuit representation.



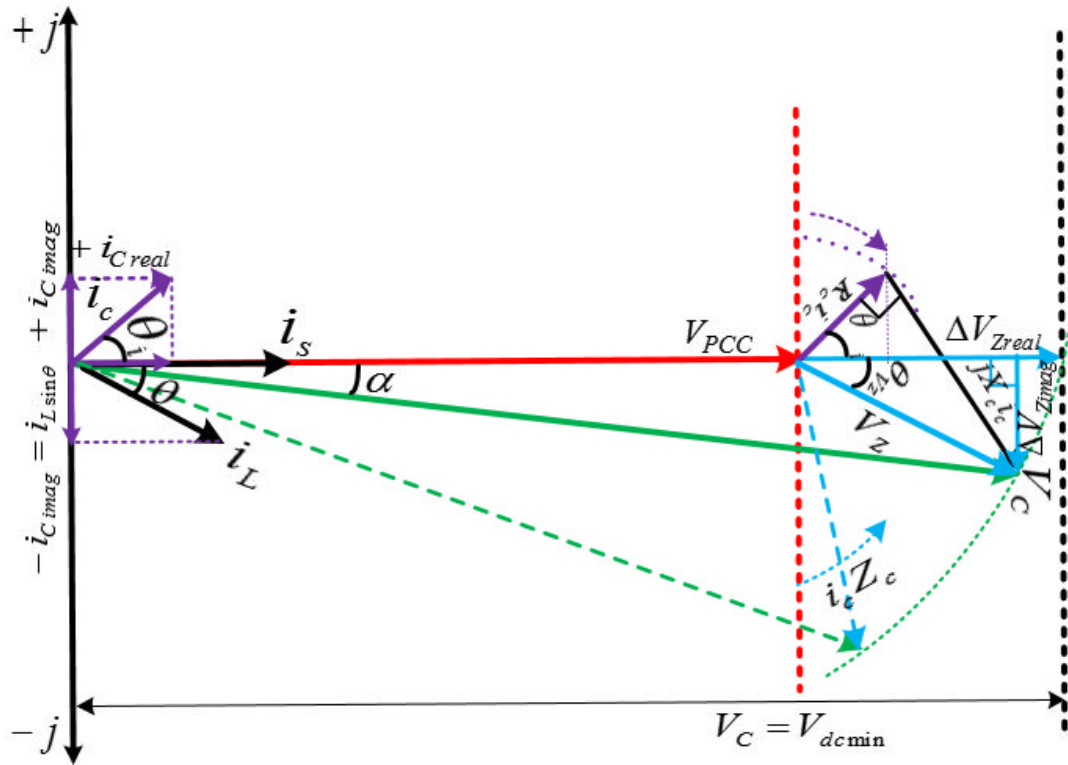


Figure 5.2: Diagram showing phasor relationship between converter, PCC voltages and currents.

Also, the converter dc voltage is related to converter output voltage  $v_c$  by the modulation ratio  $m_a$  as:

$$m_a = \frac{V_{Cpeak}}{V_{dc}} = \frac{NV_{CSM}}{NV_{dcSM}} = \frac{V_{CSM}}{V_{dcSM}} \tag{5.2}$$

where,  $V_{Cpeak}$  = peak value of converter output voltage,

$V_{CSM}$  = peak voltage value per sub-module,

$V_{dcSM}$  = dc voltage per sub-module

$N$  = total number of sub-modules per phase cluster

The relationship between the various parameters in Figure 5.1 is explained below.

For unity power factor correction operation, ignoring converter real current drawn, the maximum compensating current supplied by the FC-MMCC is determined by the load reactive current  $i_L \sin \theta$ . This means that no reactive current is supplied from PCC source side hence:

$$i_{Simag} = i_{Limag} + i_{Cimag} = 0. \tag{5.3}$$

From the figure above, the load power factor determines directly the current injected by the FC-MMCC STATCOM.

The phase angle of the converter current with respect to the PCC voltage is determined according to the amount reactive power is supplied or absorbed, and active power it absorbs. If it supplies more reactive power than the active power absorbed its current angle is in the range of  $45^\circ \leq \theta_i \leq 90^\circ$  or if more active power is absorbed than the reactive power injected it is  $0^\circ \leq \theta_i \leq 45^\circ$ . Also, the converter filter impedance has a significant influence on the converter output voltage since the product of  $\vec{i}_c$  and  $\vec{Z}_c$  determines the voltage difference between  $\vec{v}_c$  and  $\vec{v}_{PCC}$ .

For voltage regulation, the power rating of the FC-MMCC is determined by the amount of reactive current required to compensate the voltage drop across the distribution line impedance.

The maximum energy in the dc capacitors of the FC-MMCC also determines the maximum reactive power it can compensate. Since it uses low voltage capacitor per sub-module the total energy stored in the three phase limbs of an FC-MMCC is determined by the sub-module capacitance  $C_{SM}$  and phase cluster dc voltage  $V_{dc}$  and is expressed as:

$$E_{MMCC} = \frac{3}{2N} C_{SM} V_{dc}^2. \quad (5.4)$$

Expressing the total energy in the FC-MMCC in terms of the specific energy. (i.e. the amount of stored kJ of energy per MVA of the MMCC ratings) is given as:

$$E_S = \frac{3}{2NS_{MMCC}} C_{SM} V_{dc}^2. \quad (5.5)$$

The cell capacitance is therefore expressed as:

$$C_{SM} = \frac{2E_S S_{MMCC}}{3N V_{dcSM}^2}. \quad (5.6)$$

[188] evaluated that to restrict the capacitor voltage ripple to the maximum 10% of its nominal level, an energy value of 30-40kJ/MVA is required. So, for an MMCC of 1059MVA,  $\pm 320$ kV with 400 sub-modules per arm, according to [189], the estimated cell capacitance to achieve the specified energy is 10mF at a nominal cell voltage of 1.6kV with IGBT rated at 4.5 kV, 1200A.

To determine the magnitude, the phase angle of FC-MMCC voltage and hence the dc cluster voltage, the phasor diagram of STATCOM current and consequent voltage drop across its terminal filter for the case of unity power factor as shown in Figure 5.3 is used.

The magnitude of the converter output voltage is expressed based on triangle (1) as:

$$V_C^2 = (V_{PCC} + \Delta V_{Zreal})^2 + (\Delta V_{Zimag})^2. \quad (5.7)$$

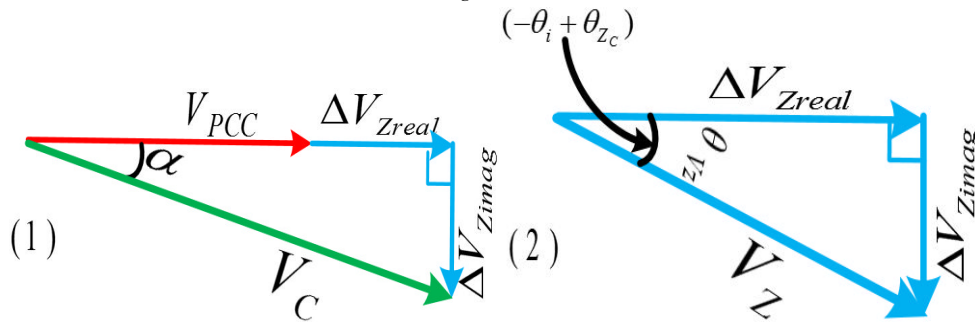


Figure 5.3: Diagram showing phasor relationship between converter and PCC voltages.

From triangle (2):

$$\Delta V_{Zreal} = V_Z \cos \theta_{VZ} \quad (5.8)$$

$$\Delta V_{Zimag} = V_Z \sin \theta_{VZ} \quad (5.9)$$

where the voltage drop across converter filter impedance is given as:

$$V_Z \angle \theta_{VZ} = |i_C Z_C| \angle (-\theta_i + \theta_{ZC}) \quad (5.10)$$

where  $\theta_{VZ}$  = angle of  $V_Z$  with respect to  $V_{PCC}$

$\theta_i$  = angle of  $i_C$  with respect to  $V_{PCC}$

$\theta_{ZC}$  = phase angle of filter impedance

Substituting  $\Delta V_{Zreal}$  and  $\Delta V_{Zimag}$  into (5.7), gives:

$$\begin{aligned} V_C^2 &= (V_{PCC} + V_Z \cos \theta_{VZ})^2 + (V_Z \sin \theta_{VZ})^2 \\ &= V_{PCC}^2 + 2V_{PCC}V_Z \cos \theta_{VZ} + V_Z^2 \\ V_C &= \sqrt{V_{PCC}^2 + 2V_{PCC}i_C Z_C \cos(-\theta_i + \theta_{ZC}) + |i_C Z_C|^2} \end{aligned}$$

The angle of the converter voltage with respect to  $V_{PCC}$  is:

$$\alpha = \tan^{-1} \left( \frac{i_C Z_C \sin(-\theta_i + \theta_{ZC})}{V_{PCC} + i_C Z_C \cos(-\theta_i + \theta_{ZC})} \right). \quad (5.11)$$

A percentage factor  $k_f$  can be used in relating the filter impedance  $Z_C$  to the load impedance  $Z_L$ , which is given as:

$$|Z_C| = k_f |Z_L|. \quad (5.12)$$

Substituting  $Z_c$  by  $k_f Z_L$ , the converter voltage magnitude and angle is written as:

$$V_c = \sqrt{V_{PCC}^2 + 2k_f i_c Z_L V_{PCC} \cos(-\theta_i + \theta_{ZC}) + (k_f i_c Z_L)^2} \quad (5.13)$$

$$\alpha = \tan^{-1} \left( \frac{i_c k_f Z_L \sin(-\theta_i + \theta_{ZC})}{1 + i_c k_f Z_L \cos(-\theta_i + \theta_{ZC})} \right) \quad (5.14)$$

And since converter voltage magnitude  $V_c$  cannot exceed  $V_{dc}$ , the required cluster dc voltage should be expressed as:

$$V_{dc \min} = \sqrt{V_{PCC}^2 + 2k_f i_c Z_L V_{PCC} \cos(-\theta_i + \theta_{ZC}) + (k_f i_c Z_L)^2} \quad (5.15)$$

From the above two equations, the  $V_{dc}$  value and converter voltage phase angle depend on the  $V_{PCC}$ , percentage factor  $k_f$  and the compensating current and filter impedance.

### 5.1.1 Variation of Converter Cell DC-bus voltage

To investigate this; a simple  $R$ - $L$  filter is connected between the converter and PCC. The converter filter angle  $\theta_{ZC}$  is expressed in terms of its cut-off frequency as:

$$\theta_{ZC} = \tan^{-1} \left( \frac{f_0}{f_{cut}} \right) = \tan^{-1} \left( \frac{2\pi f_0 L_C}{R_C} \right) = \tan^{-1} \left( \frac{X_C}{R_C} \right) = \tan^{-1}(k_c). \quad (5.16)$$

The converter filter cut-off frequency will be used instead of its impedance to the dc-bus voltage analysis.

Equations (5.12) - (5.14) are evaluated using a MATLAB program (see *Appendix C.1*) in determining the converter dc-bus voltage.

For this analysis, the STATCOM is set to compensate the whole reactive current drawn by the load. Also, the converter current angle is varied between  $60^\circ \leq \theta_i \leq 90^\circ$  because the active current drawn by the STATCOM cannot exceed the reactive current compensated.

Figure 5.4 and Figure 5.5 show the required cluster dc voltage under two different  $k_f$  values for converter current phase angle in the range of  $60^\circ \leq \theta_i \leq 90^\circ$  at different converter filter cut-off frequencies between  $100\text{Hz} \leq f_{cut} \leq 1000\text{Hz}$ . The converter current angle is varied between  $60^\circ \leq \theta_i \leq 90^\circ$  because for a practical STATCOM, the active current drawn by the STATCOM should not exceed the reactive current compensated. This current phase angle variation range shows the ratio of reactive current required from the STATCOM to the active current absorbed by the converter from the grid in compensating for its

power losses. Also for this analysis, the STATCOM is set to compensate the whole reactive current drawn by the load.

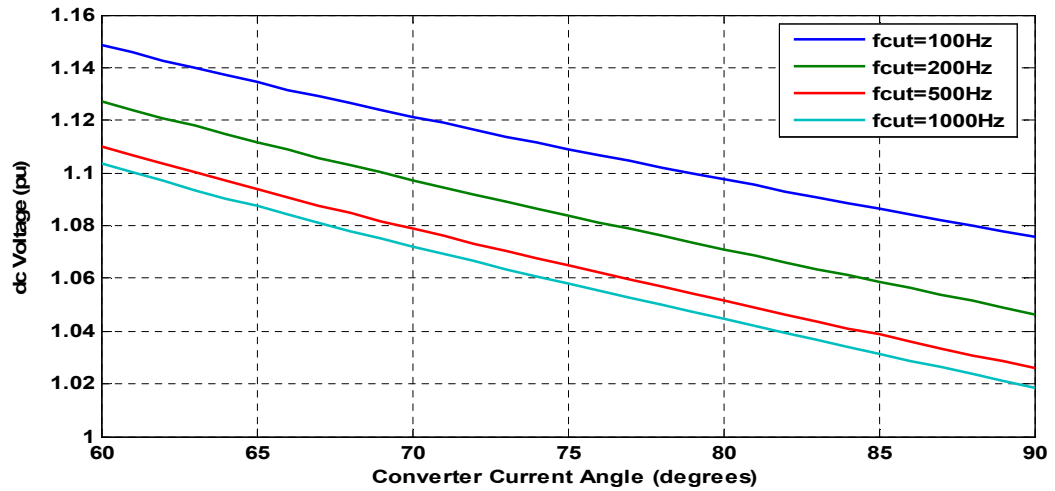


Figure 5.4: Changes in converter current phase angle against minimum required converter dc-bus voltage when  $k_f=0.3$  for  $f_{cut}$  between 100Hz to 1 kHz.

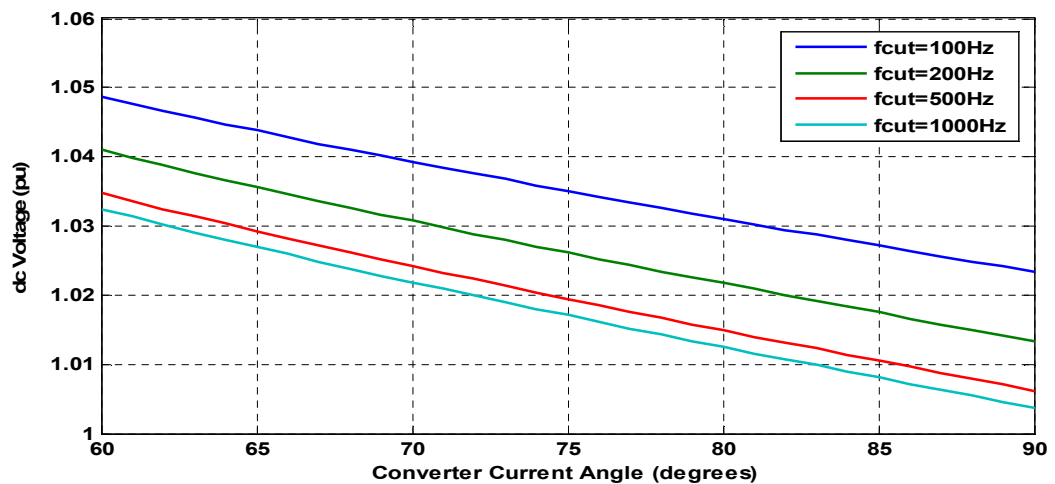


Figure 5.5: Changes in converter current phase angle against minimum required converter dc-bus voltage when  $k_f=0.1$  for  $f_{cut}$  between 100Hz to 1 kHz.

Figure 5.4 shows the case when the converter filter  $k_f$  is 30% of the load impedance. The minimum converter dc-bus voltage is seen to be between  $1.15pu$  to  $1.12pu$  when current phase angle is between  $60^\circ \leq \theta_i \leq 70^\circ$  for  $f_{cut}=100Hz$  which is higher than the PCC voltage by  $0.15pu$  to  $0.12pu$ . At  $\theta_i=60^\circ$ , the STATCOM compensation reactive current is  $0.366pu$  greater than the real current required to compensate converter losses. Between  $80^\circ \leq \theta_i \leq 90^\circ$ , the required  $i_{Creal}$  is lower compared to the compensated reactive current, this then makes the required converter cell dc-bus voltage to be between  $1.095pu$  to  $1.075pu$ .

Figure 5.5 illustrates a similar condition as that in Figure 5.4 but for  $k_f = 10\%$  of load impedance. It is seen that for a lower  $k_f$ , the minimum converter dc-bus voltage is seen to be between  $1.048pu$  to  $1.025pu$ , which is higher than PCC voltage by only  $0.048pu$  to  $0.025pu$  for  $60^\circ \leq \theta_f \leq 90^\circ$  at  $f_{cut} = 100\text{Hz}$ . Because of the high voltage levels synthesized by FC-MMCC, lower filter impedance can be applicable and still can achieve full reactive power compensation.

The analysis has shown that the choice of the MMCC filter influences the converter dc bus voltage rating under reactive power compensation. The results of this analysis can be summarized as follows;

- The required minimum dc converter voltage increases as the real current required for converter power loss compensation increases.
- The required minimum dc converter voltage increases as the converter filter impedance size increases while the reverse is the case when the converter filter cut-off frequency increases.

## 5.2 Determination of Sub-module capacitor voltage ripple of FC-MMCC STATCOM

The voltage ripple in each sub-module capacitor show the energy exchange between the MMCC and the grid. This comprises of mainly second order harmonic component and higher order ones due to switching, they shorten capacitor life span [190]. If its magnitude is higher than 10% of the nominal DC-voltage, it has an adverse effect on the MMCC control system and current fed into the grid [191-194]. In this section, an expression of the sub-module capacitor voltages as a function of converter voltage and current is derived and, hence the converter current angle, filter size and cut-off frequencies on capacitor voltage ripple are analysed.

Taking the PCC voltage as reference, the relationship of the converter ac side voltage with the PCC voltage can be written as:

$$\sum_{i=1}^N v_{C-i} - v_{PCC} - R_C i_C - L_C \frac{di_C}{dt} = 0 \quad (5.17)$$

where  $v_{C-i}$  is the ac voltage generated by the  $i^{th}$  sub-module,  $L_C$  and  $R_C$  represent converter filter parameters,  $v_{pcc}$  and  $i_C$  are the PCC voltage and converter current.

On the dc side, the sub-module voltage  $V_{sm-i}$  is related to the current  $I_{sm-i}$  flowing into the capacitor as:

$$I_{sm-i} = C_{SM} \frac{dv_{sm-i}}{dt} \quad (5.18)$$

where  $C_{sm}$  represent the capacitance of sub-module capacitors. Assuming the losses due to switching action is neglected, the powers on both the ac side and the dc side are equal and can be expressed as:

$$\begin{aligned} V_{sm-i} I_{sm-i} &= v_{C-i} i_C \\ I_{sm-i} &= \frac{v_{C-i} i_C}{V_{sm-i}} \end{aligned} \quad (5.19)$$

Substituting (5.18) into (5.19) gives:

$$\frac{v_{C-i} i_C}{V_{sm-i}} = C_{SM} \frac{dV_{sm-i}}{dt} \quad (5.20)$$

An expression of sub-module energy is derived by solving the differential equation (5.20) as:

$$\frac{C_{sm} V_{sm-i}^2(t)}{2} = E_{sm-i}(t_o) + \int_{t_o}^t v_{C-i} i_C dt \quad (5.21)$$

where  $E_{sm-i}(t_o)$  is the energy stored in the  $i^{th}$  sub-module capacitor at  $t = t_o$ . Replacing  $v_{C-i} = V_{C-i} \sin(\omega t + \alpha_{V-i})$  and  $i_C = I_C \sin(\omega t + \theta_i)$  in (5.21), which means all other harmonics in the PCC voltage and converter current are neglected. Therefore, (5.21) is simplified to:

$$\frac{C_{sm} V_{sm-i}^2(t)}{2} = E_{sm-i}(t_o) + V_{C-i} I_C \int_{t_o}^t \sin(\omega t + \alpha_{V-i}) \sin(\omega t + \theta_i) dt \quad (5.22)$$

Simplifying (5.22),

$$\begin{aligned} \frac{C_{sm} V_{sm-i}^2(t)}{2} &= E_{sm-i}(t_o) + \frac{V_{C-i} I_C}{2} \int_{t_o}^t [\cos(\alpha_{V-i} - \theta_i) - \cos(2\omega t + \alpha_{V-i} + \theta_i)] dt \\ &= E_{sm-i}(t_o) + \frac{V_{C-i} I_C}{2} \int_{t_o}^t \left[ \cos(\alpha_{V-i} - \theta_i) - \cos 2\omega t \cos(\alpha_{V-i} + \theta_i) \right. \\ &\quad \left. + \sin 2\omega t \sin(\alpha_{V-i} + \theta_i) \right] dt \\ &= E_{sm-i}(t_o) + \frac{V_{C-i} I_C}{2} \left[ \cos(\alpha_{V-i} - \theta_i)(t - t_o) - \frac{1}{2\omega} \left[ \sin(2\omega t + \alpha_{V-i} + \theta_i) \right. \right. \\ &\quad \left. \left. - \sin(2\omega t_o + \alpha_{V-i} + \theta_i) \right] \right] \end{aligned} \quad (5.23)$$

The time varying equation for sub-module capacitor voltage is expressed as:

$$V_{sm-i} = \sqrt{V_{sm-i}^2(t_0) + \underbrace{\frac{V_{C-i} I_C}{C_{sm}} \left( \cos(\alpha_{V-i} - \theta_i)(t - t_0) - \frac{1}{2\omega} \left[ \begin{array}{l} \sin(2\omega t + \alpha_{V-i} + \theta_i) \\ -\sin(2\omega t_0 + \alpha_{V-i} + \theta_i) \end{array} \right] \right)}_{\text{voltage ripple}}}} \quad (5.24)$$

where  $\omega$  is the angular frequency of the grid voltage,  $V_{C-i}$  and  $\alpha_{V-i}$  are the converter voltage maximum value and phase angle.  $I_C$  and  $\theta_i$  are the converter current maximum value and phase angle.

$V_{sm-i}(t_0)$  is the nominal voltage of  $i^{th}$  sub-module capacitor.

The converter voltage and current phase angles are expressed as:

$$\alpha_{V-i} = \tan^{-1} \left( \frac{i_C Z_C \sin(-\theta_i + \theta_{ZC})}{V_{PCC} + i_C Z_C \cos(-\theta_i + \theta_{ZC})} \right) \quad (5.25)$$

$$\theta_i = \tan^{-1} \left( \frac{i_{Cimag}}{i_{Creal}} \right). \quad (5.26)$$

From equation (5.25), the converter voltage phase angle is influenced by the converter filter impedance parameters.

### 5.2.1 Variation of Sub-module capacitor voltage ripple

In this section, the influence of converter filter impedance hence its cut-off frequency, compensation current phase angle and sub-module capacitance to the capacitor voltage ripple is analysed. A MATLAB program (see Appendix C.2) using Equations (5.24)-(5.26) is used in determining the peak capacitor voltage ripple. Figures 5.6 to 5.8 show the capacitor voltage ripple magnitude under converter current phase angle operating range  $60^\circ \leq \theta_i \leq 90^\circ$  at different converter filter ratios  $k_C$ ,  $k_f$  and sub-module capacitance  $C_{sm}$ .

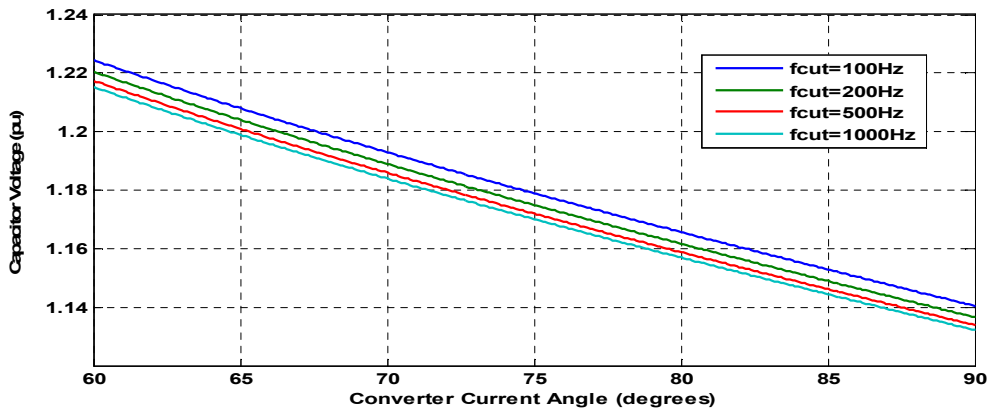


Figure 5.6: Changes in converter current phase angle against capacitor voltage when  $k_f=0.3$  for  $f_{cut}$  between 100Hz to 1 kHz and a fixed capacitance of  $C_{sm}=0.56\text{mF}$ .



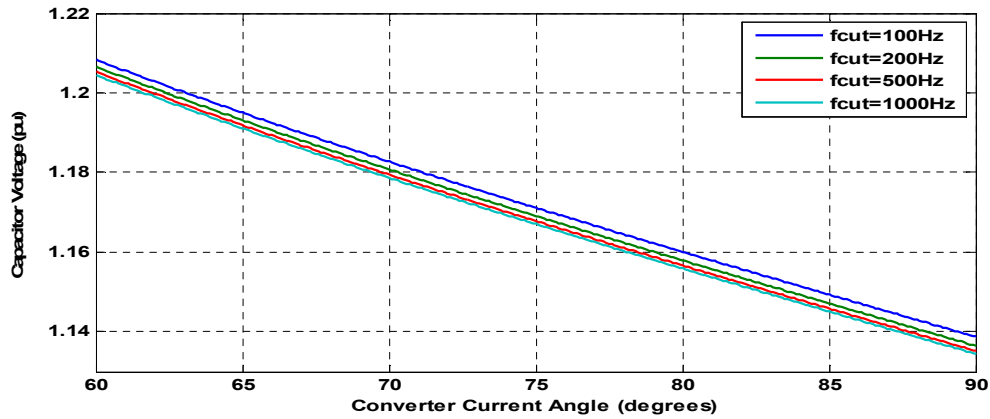


Figure 5.7: Changes in converter current phase angle against capacitor voltage when  $k_f=0.1$  for  $f_{cut}$  between 100Hz to 1 kHz and a fixed capacitance value  $C_{sm}=0.56\text{mF}$ .

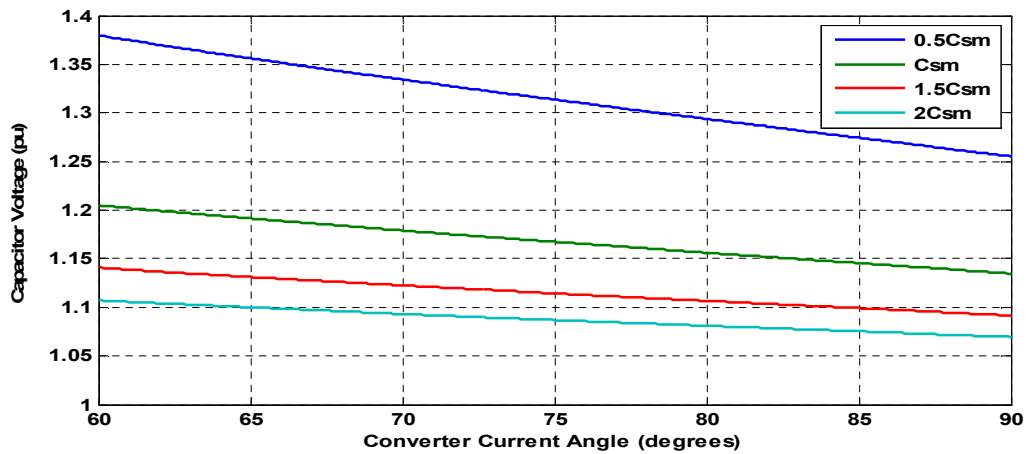


Figure 5.8: Changes in converter current phase angle against capacitor voltage when  $k_f=0.1$  for  $f_{cut}=1$  kHz and varying capacitance value.

Figure 5.6 shows the case when the converter filter  $k_f$  is 30% of the load impedance. The converter sub-module capacitor voltage decreases from 1.22pu to 1.135pu for  $f_{cut}=200\text{Hz}$  corresponding to  $60^\circ \leq \theta_i \leq 90^\circ$ . This increase in the capacitor voltage is due to the effect of its voltage ripple. As seen in Figure 5.5 for  $f_{cut}$  values of 100Hz, 200Hz, 500Hz and 1000Hz at converter current phase angle  $\theta_i=90^\circ$ , the voltage ripples are 0.14pu, 0.137pu, 0.134pu and 0.132pu.

Figure 5.7 illustrates a similar condition as Figure 5.5 but for  $k_f=10\%$  of load impedance. It is seen that for a low  $k_f$ , the converter voltage ripple is seen to be 0.208pu and 0.138pu, corresponding to  $\theta_i=60$  and  $90^\circ$  respectively at  $f_{cut}=100\text{Hz}$ . As seen in Figure 5.8, as the sub-module capacitance increases the voltage ripple decreases.

The analysis above has shown that the choice of the MMCC filter, sub-module capacitance, and converter current phase angle has an influence on the

converter sub-module capacitor voltage ripple. These analysis results are summarized in the following;

- The sub-module capacitor voltage ripple decreases as the converter power losses are negligible.
- The sub-module capacitor voltage ripple increases as the converter filter impedance size increases.
- The sub-module capacitor voltage ripple decreases as its capacitance value increases.
- The sub-module capacitor voltage ripple decreases as the ratio of reactive power injected to the grid and active power absorbed by the converter increases.

### 5.3 FC-MMCC STATCOM Simulation Studies

In this section, the simulation study of using the FC-MMCC as a STATCOM in single star configuration for unity power factor correction of a small power system is presented.

#### 5.3.1 Power System Configuration

Figure 5.9 shows a power system rated at 100V, 3.0kVA and 50Hz supplying an inductive load and using an FC-MMCC STATCOM for reactive power compensation. Each of the converter phase legs has two cascaded 5-L FCC modules, hence synthesizing a total of 9 voltage levels per phase. The FC-MMCC STATCOM is connected to the PCC via an  $R-L$  filter and an inductive load with a power factor of 0.83 is connected to the same PCC.

The converter filter parameters, converter dc-bus voltages and sub-module capacitance values are selected based on the analysis given in the earlier sections. The filter cut-off frequency  $f_{cut}$  of 176.8Hz and  $k_f$  factor of 0.11 are selected giving filter parameters of  $2.5\Omega$  and 2.25mH and converter minimum dc voltage is set to be 20% higher than  $V_{PCC}$ . Thus the converter voltage of 120V is equally shared between the two FCC-sub-modules of each phase cluster. The parameters of the power network are listed in Table 5.1.

Table 5.1: FC-MMCC power system parameters

Rating	Value
PCC Side	3.0 kVA (110V, 10A)
Distribution Line	Aluminium PI TX line (d= 10mm, s= 1m, l=1.1 km) L =2mH, R = 0.4 $\Omega$ , X= 0.6283 $\Omega$ , Short circuit current = 137 A
Load Side	1.5 kVA (100V, 5 A) Load: 22 $\Omega$ , 47mH Power factor = 0.83 lagging
Converter Side	1.8 kVA (120V, 5A) Filter: 2.5 $\Omega$ , 2.25 mH DC Capacitor rating (per sub-module): 400 V, 1.12 mF (utilized at 60 V) Module Flying Capacitor: 400V, 0.56mF (utilized at 30 V)
Switching frequency	750 Hz

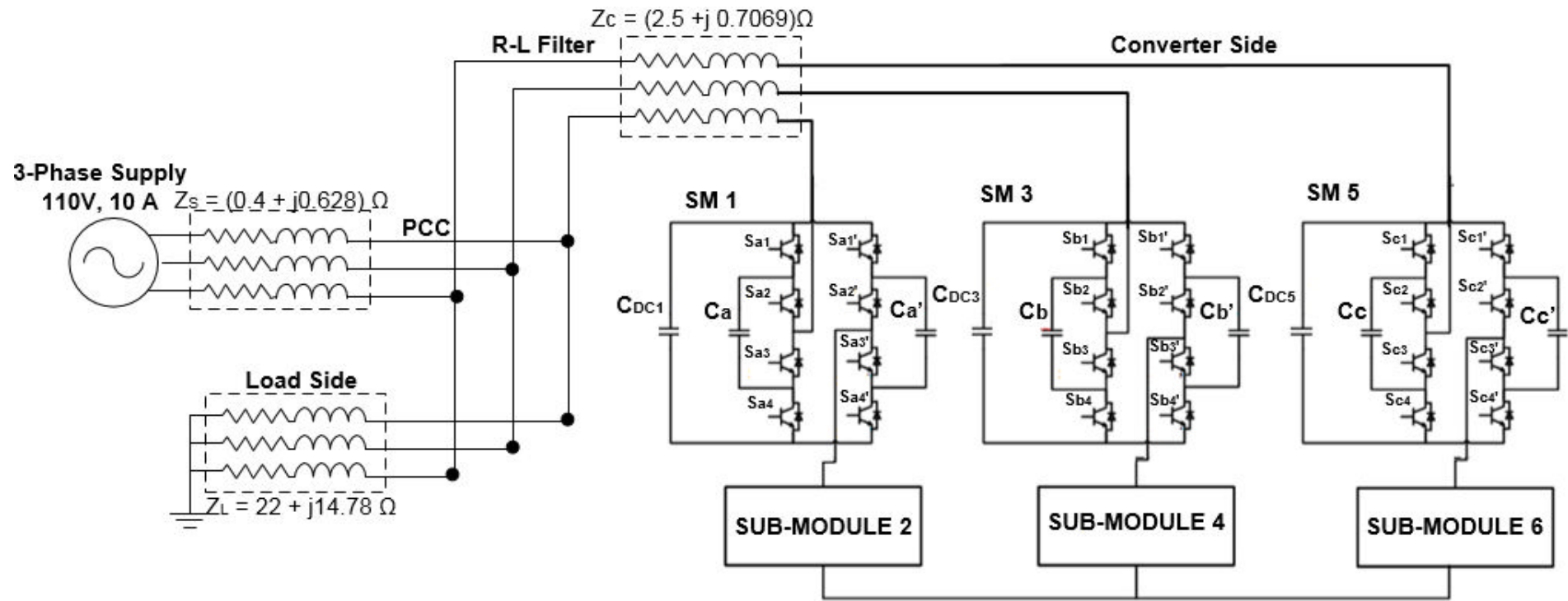


Figure 5.9: Simulated Power System Configuration.

### 5.3.2 FC-MMCC STATCOM Control Scheme

To achieve unity power factor correction regulation through quadrature power compensation, STATCOM controller must meet the following criteria;

1. It must remain in synchronisation with the PCC voltage under all operating conditions (steady or transient states) and on the event of a fault, it should quickly re-gain synchronisation upon fault clearance.
2. It should be able to regulate both the ac-side and converter dc-side voltages to the required levels, hence to dictate the flow of quadrature power and compensate the converter losses.

To achieve the above criteria, the STATCOM controller was developed to comprise the following parts;

1. A synchronous reference frame phase locked loop (SRF-PLL) for synchronizing the converter output voltage with the PCC voltage.
2. Measurement system for the acquisition of the voltages and currents as well as converting such values to their equivalent synchronous reference  $d$ - $q$  frame as required.

The STATCOM controller is divided into three parts

1. DC bus voltage balancing control
2. Reactive current extraction, and
3. Current control.

The vector current control method has been applied for this research since it provides independent control of real and reactive power through the use of rotating synchronous reference frame decoupling technique.

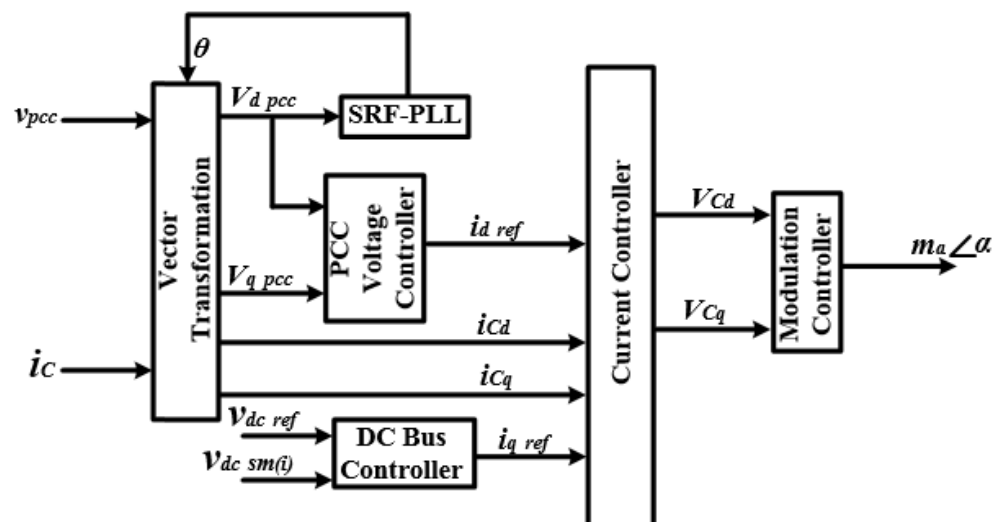


Figure 5.10: Block diagram of STATCOM controller.

Figure 5.10 shows the block diagram of FC-MMCC STATCOM controller which comprises three parts as mentioned above. All the measured voltage and current signals from PCC bus, converter bus, and sub-module dc-voltages are filtered using low pass filter filters. The filtered ac signals are transformed to their  $d$ - $q$  components using grid voltage as the reference frame with its phase angle derived from the phase locked loop discussed in chapter one. A sampling frequency of 12 kHz is applied for grid voltage synchronization. The dc-bus voltage controller maintains the sub-module dc voltages of the FC-MMCC to their nominal values. The output of this controller generates the required  $q$ -axis current component for STATCOM (converter losses) and is used as the reference current value to the current controller. The  $d$ -axis reference current value for STATCOM is evaluated by measuring reactive current absorbed by the inductive load bus by supplying an equivalent capacitive current for power factor compensation. Using the evaluated  $d$ - $q$  currents as references and measured STATCOM ac currents as feedback, a current controller is applied to determine the STATCOM ac terminal voltage vector reference  $V_{dq}$ . These are converted to converter modulation index and angle and are applied to the PWM controller to generate switching signals for the FC-MMCC STATCOM.

### 5.3.3 Overall dc-bus voltage balancing control

The dc-bus voltage per sub-module should be ideally maintained at its required level by its module capacitor, but due to load, switching pattern changes and converter switches losses, the voltage may vary. A controller is therefore used to maintain the dc voltage across each sub-module to its required value. The controller uses the average value of the three phase limb voltages as the feedback signal, namely:

$$V_{dc(avg)} = \frac{\sum_{i=1}^6 V_{dc\_sm(i)}}{3} \quad (5.27)$$

where  $i$  = number of sub-modules,  $V_{dc\_sm(i)}$  = dc voltage across each individual sub-modules. This is compared with the reference dc bus voltage,  $V_{dc\_ref}$  and the error signal is applied to a  $P+I$  controller to generate the  $q$ -component of the current control vector. Since  $PS$ - $PWM$  scheme enables natural balancing of inner floating capacitors, this thereby eliminates the need for feedback control of their voltages. The block diagram of the dc bus controller is shown in Figure 5.11.

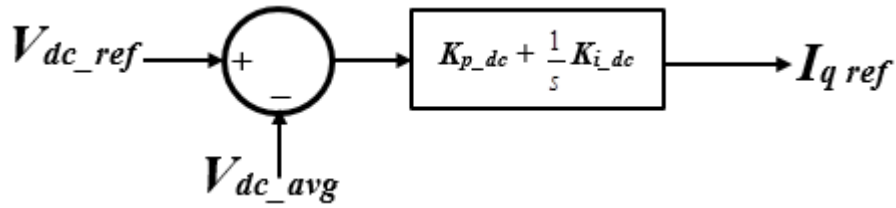


Figure 5.11: Overall dc-voltage controller.

### 5.3.4 Current Controller

The current controller evaluates the converter reference voltage vector which can generate the compensating current for obtaining unity power factor power flow. The controller is designed based on the well-known relationship between FC-MMCC and PCC voltage vectors as:

$$v_{C(abc)} = v_{PCC(abc)} + R_C i_{C(abc)} + L_C \frac{di_{C(abc)}}{dt} \quad (5.28)$$

where  $R_C$  and  $L_C$  are the converter filter impedance parameters.

Transforming equation (5.28) from stationary  $abc$  frame to  $d-q$  rotating reference frame (given in appendix C.4), the converter voltages in  $d-q$  reference form are expressed as:

$$v_{Cd} = v_{d\ pcc} + R_C i_{Cd} + L_C \frac{di_{Cd}}{dt} + \omega L_C i_{Cq} \quad (5.29)$$

$$v_{Cq} = v_{q\ pcc} + R_C i_{Cq} + L_C \frac{di_{Cq}}{dt} - \omega L_C i_{Cd}. \quad (5.30)$$

It is obvious that under steady state condition, the differential terms in above two equations are zero and the voltage  $d-q$  terms are therefore constants. Applying deadbeat predictive control scheme, for a sufficiently small sampling period  $T_s$ , the derivative term of (5.28) can be expressed as:

$$\frac{di_C}{dt} = \frac{\Delta i_C}{T_s} = \frac{i_{C(K+1)} - i_{ref(K+1)}}{T_s} \quad (5.31)$$

At the end of a sampling period, the controller aims to equate the compensating current  $i_{C(K+1)}$  to the reference current  $i_{ref(K+1)}$ . Since  $i_{ref(K+1)}$  is not known in advance, its present current value  $i_{C\ ref(K)}$  is used. Thus the compensating current  $i_{C(K)}$  and the reference current  $i_{C\ ref(K)}$  are represented as  $(i_{Cd(K)}, i_{Cq(K)})$  and  $(i_{d\ ref(K)}, i_{q\ ref(K)})$ .

The deadbeat control equation for calculating the required reference voltage for the next sampling period is:

$$\begin{bmatrix} v_{Cd(k+1)} \\ v_{Cq(k+1)} \end{bmatrix} = \begin{bmatrix} v_{d\ pcc(k)} \\ v_{q\ pcc(k)} \end{bmatrix} + \begin{bmatrix} (R_C - \frac{L_C}{T_S}) & \omega L_C \\ -\omega L_C & (R_C - \frac{L_C}{T_S}) \end{bmatrix} \begin{bmatrix} i_{Cd(k)} \\ i_{Cq(k)} \end{bmatrix} + \begin{bmatrix} \frac{L_C}{T_S} & 0 \\ 0 & \frac{L_C}{T_S} \end{bmatrix} \begin{bmatrix} i_{d\ ref(k)} \\ i_{q\ ref(k)} \end{bmatrix} \quad (5.32)$$

The output voltages calculated from the above control scheme are transformed into *abc* voltages to control the converter operation via PS-PWM scheme discussed in chapter three.

## 5.4 Simulation Results and Discussions

Investigating reactive power compensation for the power system network shown in Figure 5.9, unity power factor correction at PCC when an inductive load draws reactive power is studied.

### 5.4.1 Unity Power Factor Correction

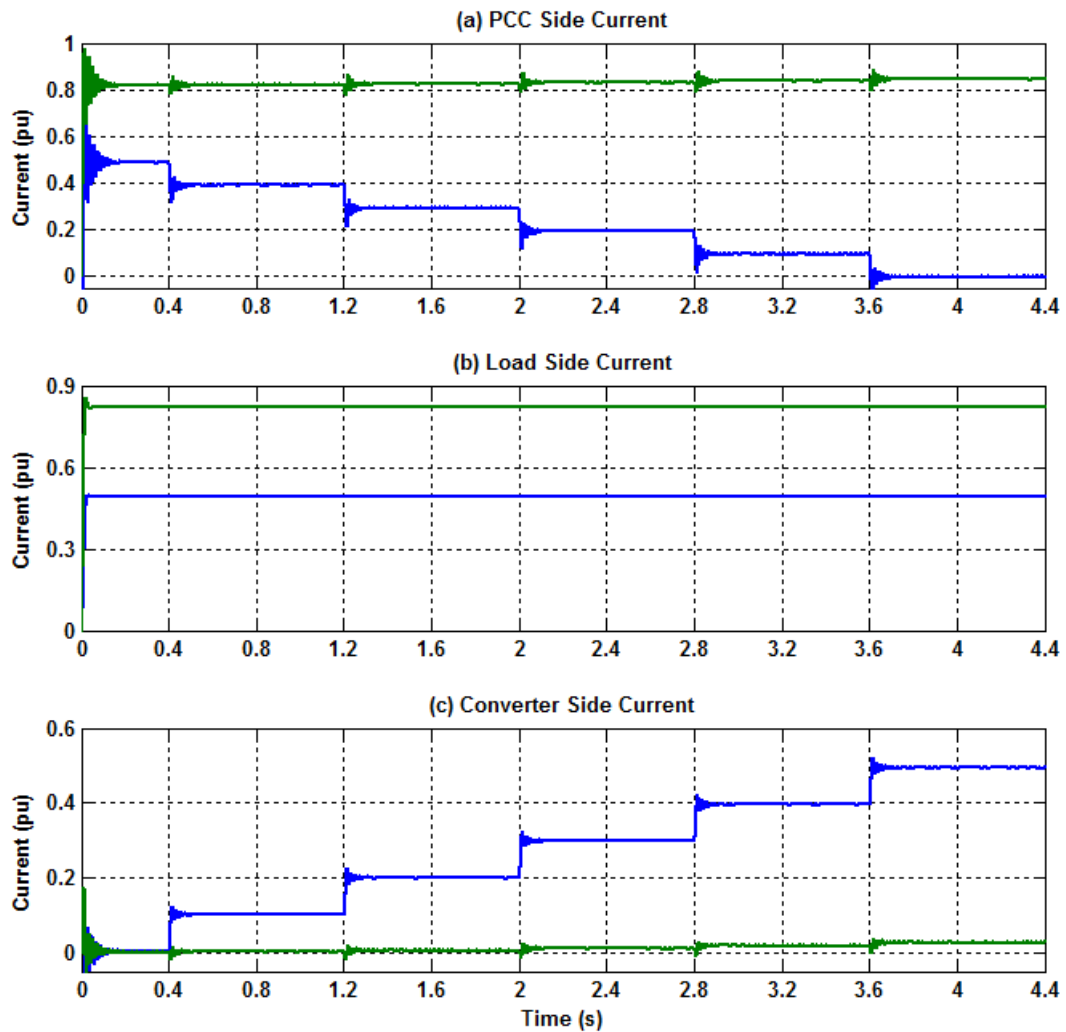
MATLAB SIMULINK was used in this study to obtain unity power factor correction for the power network shown in Figure 5.9 with parameters listed in Table 5.1. The inductive load supplied which absorbs a reactive power of 900VAr. At the first stage during time interval  $0s < t \leq 0.4s$  the converter sub-module capacitors are pre-charged to the required level. At  $t = 0.4s$  the load is connected and the compensation of reactive power starts from 20% of its rated level. This is increased at the step of 20% for every 0.8 s, thus, we have intervals of  $0.4s < t \leq 1.2s$ ,  $1.2s < t \leq 2s$ ,  $2s < t \leq 2.8s$ ,  $2.8s < t \leq 3.6s$  and  $3.6s < t \leq 4.4s$  corresponding to 20%, 40%, 60%, 80% and 100% reactive power compensation. The voltage proportional and integral controller gains for the dc capacitor controller are set as  $K_{p\_dc} = 0.5$   $K_{i\_dc} = 10$  respectively.

#### 5.4.1.1 Active and Reactive Current Responses

The responses of active and reactive currents at PCC, load, and STATCOM buses are shown in Figure 5.12 (a)-(c).

As the reactive current level of STATCOM compensation increases from 0A to 2.4A, the PCC reactive current decreases from 0.48pu (2.4A) to 0A. The load absorbed active and reactive currents are unchanged. The PCC active current is observed to be slightly increasing as the compensated current increases from 0.82pu (4.1A) to 0.85pu (4.25A). This increment is attributed to the active current required to balance the STATCOM sub-module capacitor and filter resistance.



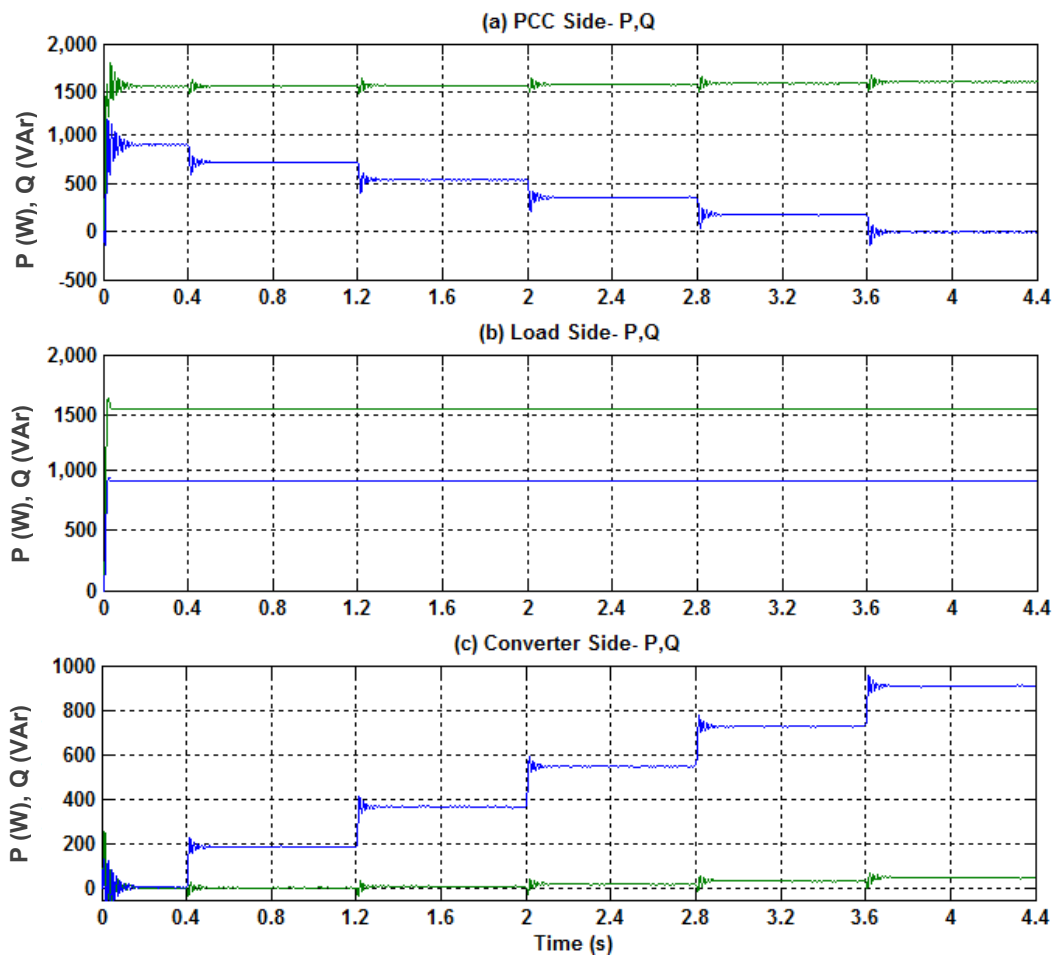


Blue-Reactive current and Green-Active current component

Figure 5.12:  $d$ - $q$  current control, (a) PCC, (b) Load and (c) STATCOM.

#### 5.4.1.2 Active and Reactive power

Figure 5.13 (a)-(c) shows the PCC, Load, and converter active and reactive powers. As expected these are similar to their current responses. At time intervals  $0 < t \leq 0.4$  to  $3.6 < t \leq 4.4$  corresponding to 0% to 100% reactive power compensation, the PCC reactive power decreases from 900 VAR to 0 VAR and active power increases from 1600 W to 1650 W. The decrease in PCC reactive power results from converter reactive power injection whilst the PCC active power increases results from maintaining converter sub-module capacitor voltages and converter resistance filter power consumption compensation.



Blue-Reactive power and Green-Active power

Figure 5.13: Active and reactive power across (a) PCC, (b) Load and (c) converter sides.

#### 5.4.1.3 PCC Voltage and current Responses

The PCC current magnitudes and angles at different compensation levels are shown in Figure 5.14 (a)-(b). While the PCC voltage and current waveforms are shown in Figure 5.15.

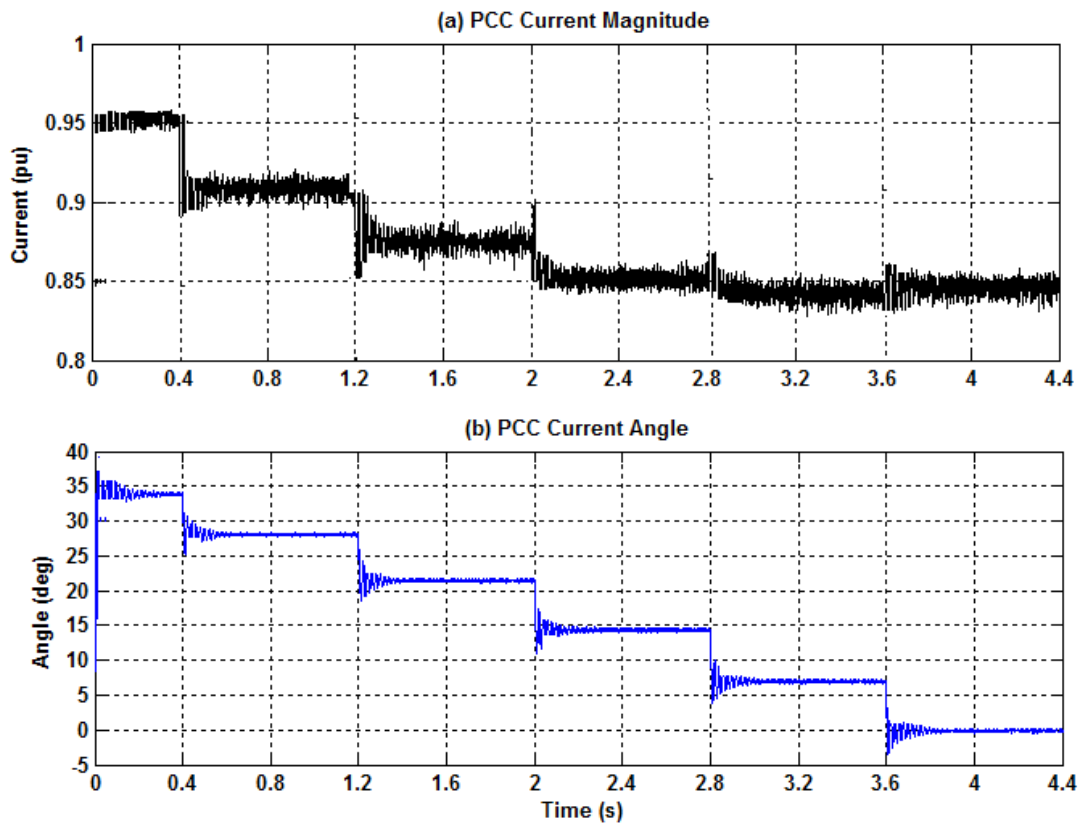


Figure 5.14: (a) PCC Current magnitude and (b) PCC Current angle.

At  $t=0$ , the PCC current magnitude and phase angles are initially higher due to charging converter sub-module capacitors. Once the compensation starts PCC current values reduces gradually corresponding to each compensation current increment and are,  $0.95 \angle 34^\circ pu$ ,  $0.91 \angle 28^\circ pu$ ,  $0.84 \angle 7^\circ pu$  and  $0.85 \angle 0^\circ pu$  for 0%, 20%, 80% and 100% test intervals. This shows that the reactive power draw from the PCC by the load gradually reduces to zero.

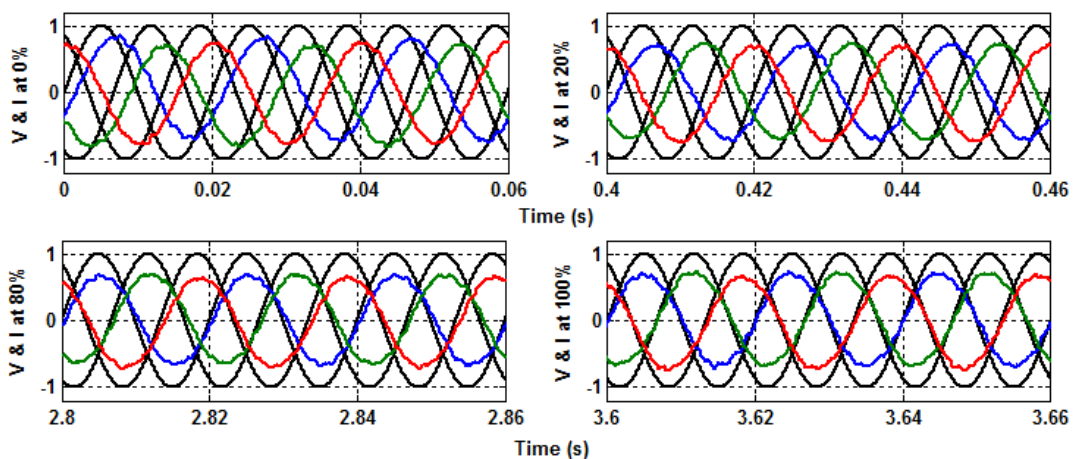


Figure 5.15: PCC voltage and current waveforms.

#### 5.4.1.4 STATCOM Waveforms

Figures 5.16 show the voltage and current waveforms measured at the STATCOM terminal, while the STATCOM voltage and current magnitude and angle are shown in Figures 5.17 and 5.18 respectively. In contrast to the PCC current, the STATCOM current magnitude and phase angle with respect to compensation levels, increase gradually, they are,  $0.09 \angle 88.8^\circ pu$ ,  $0.39 \angle 87.3^\circ pu$  and  $0.485 \angle 86.8^\circ pu$  corresponding to 20%, 80%, and 100% compensation levels. Corresponding to this compensation pattern the converter terminal voltages are adjusted by the controller to meet current requirement. The modulation index and converter voltage angles are,  $0.834 \angle -0.5^\circ pu$ ,  $0.833 \angle -1^\circ pu$ ,  $0.832 \angle -1.5^\circ pu$ ,  $0.831 \angle -2^\circ pu$  and  $0.832 \angle -2.5^\circ pu$ . Figure 5.19 shows the converter three-phase voltage waveforms having 9 distinct voltage levels.

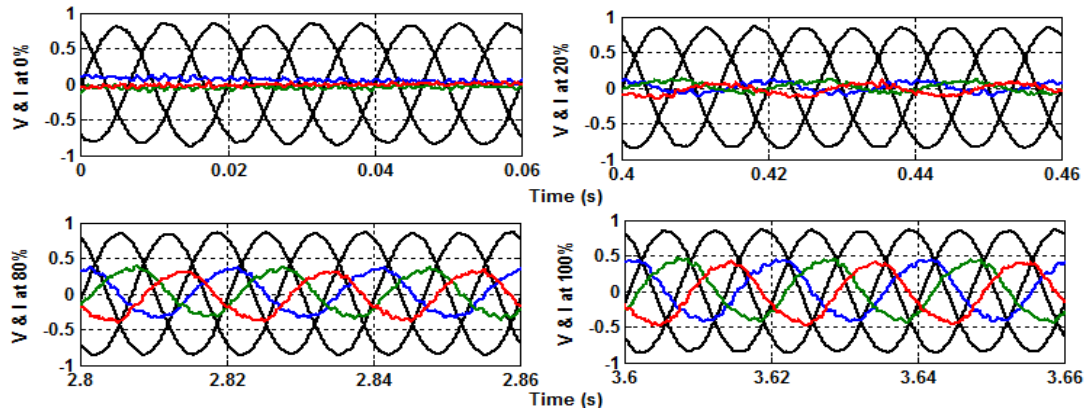


Figure 5.16: STATCOM voltage and current waveforms.

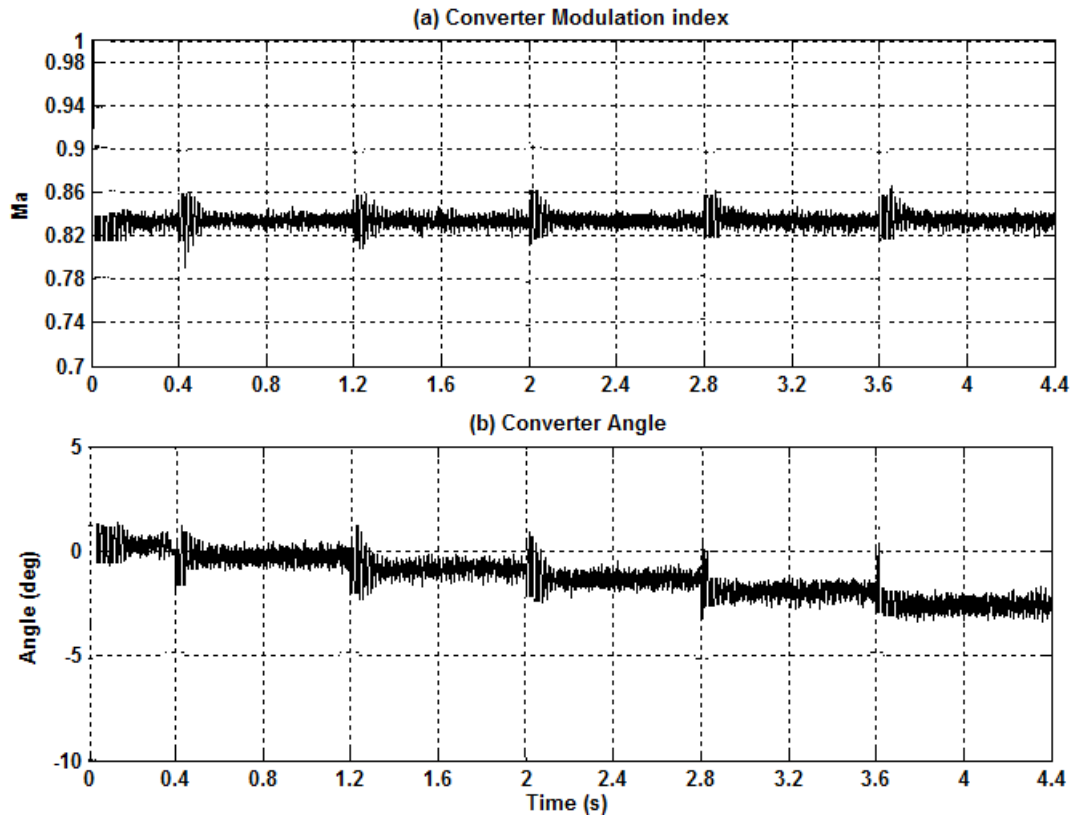


Figure 5.17: (a) Converter voltage magnitude and (b) angle at zero compensation, 20%, 40%, 60%, 80% and 100%.

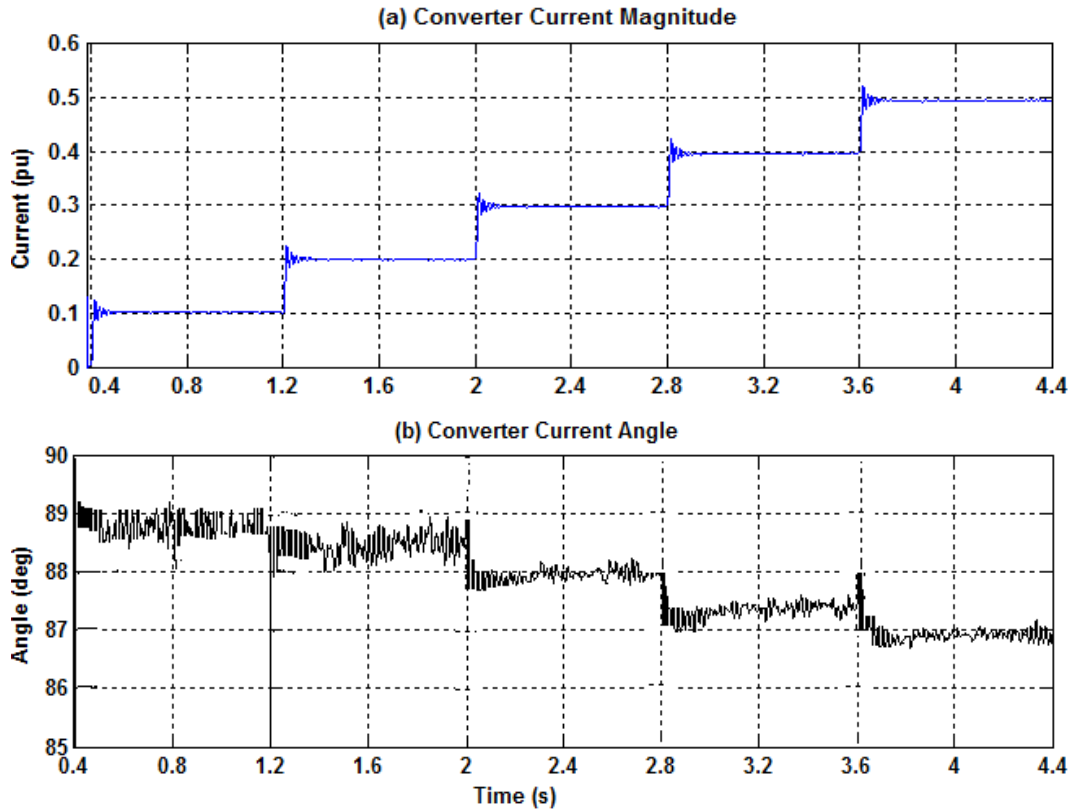


Figure 5.18: (a) Converter Current magnitude and (b) angle at zero compensation, 20%, 40%, 60%, 80% and 100%.

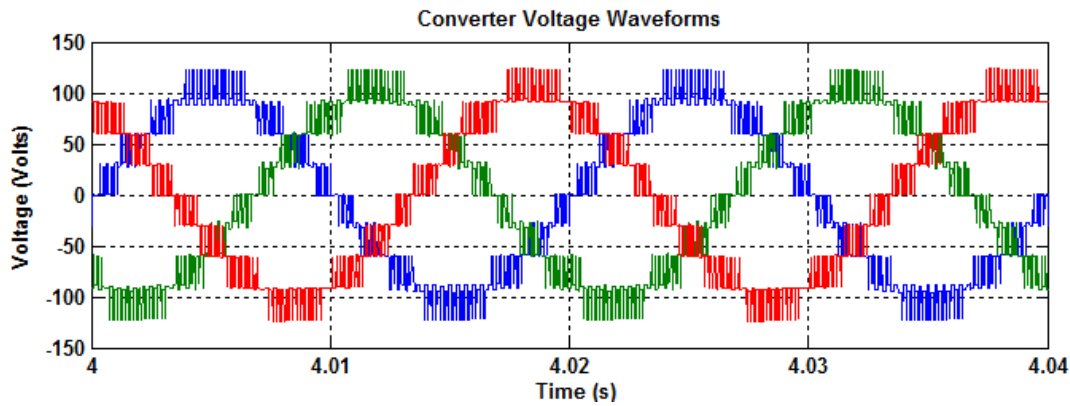


Figure 5.19: (a) converter Voltage waveforms.

#### 5.4.1.5 DC Converter Capacitor Voltage

Figure 5.20 (a)-(c) and Figure 5.21 (a)-(c) show the converter sub-module capacitor and inner flying capacitor voltage waveforms. The dc sub-module capacitor and inner flying capacitor voltages are controlled to maintain a nominal value of 60V and 30V corresponding to 1pu respectively. At time interval  $0 < t \leq 4.4s$ , the sub-module capacitor voltages and inner flying capacitors are well balanced. But as compensation level increases (i.e. current magnitude increases), the capacitor voltage ripple across both sub-module and inner capacitors increases but is well within  $\pm 10\%$ .

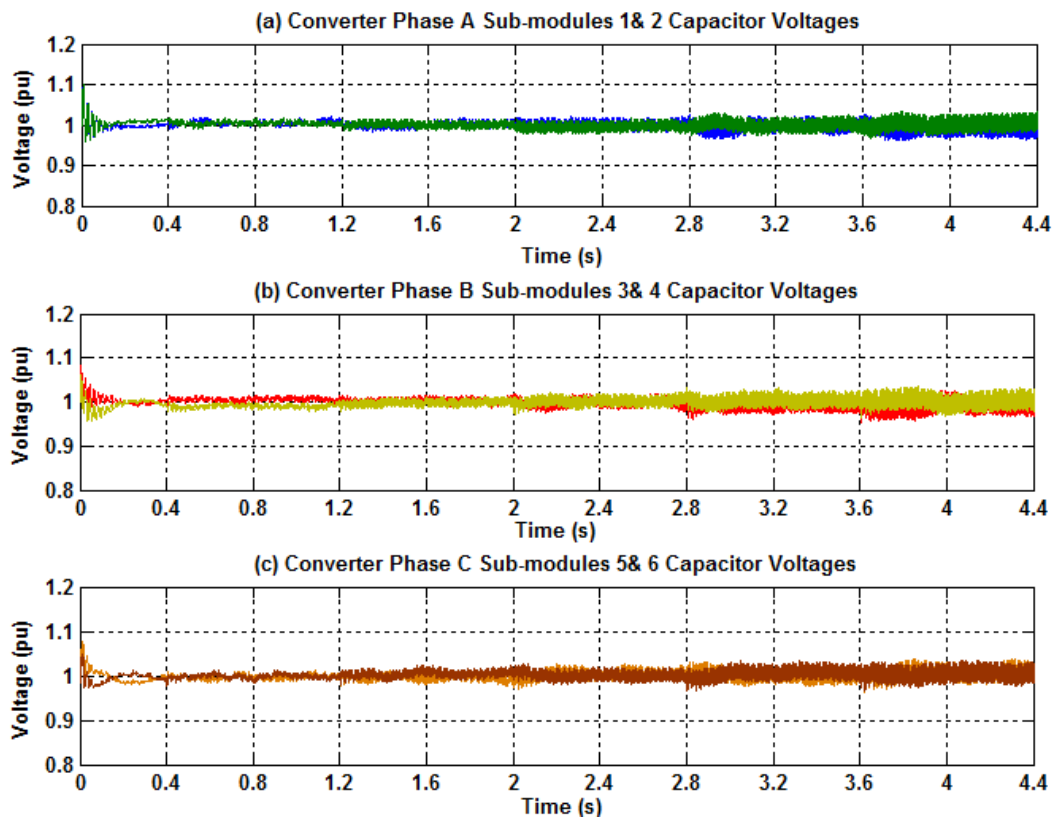


Figure 5.20: Converter Sub-module capacitor voltages across (a) phase A, (b) phase B and (c) Phase C.

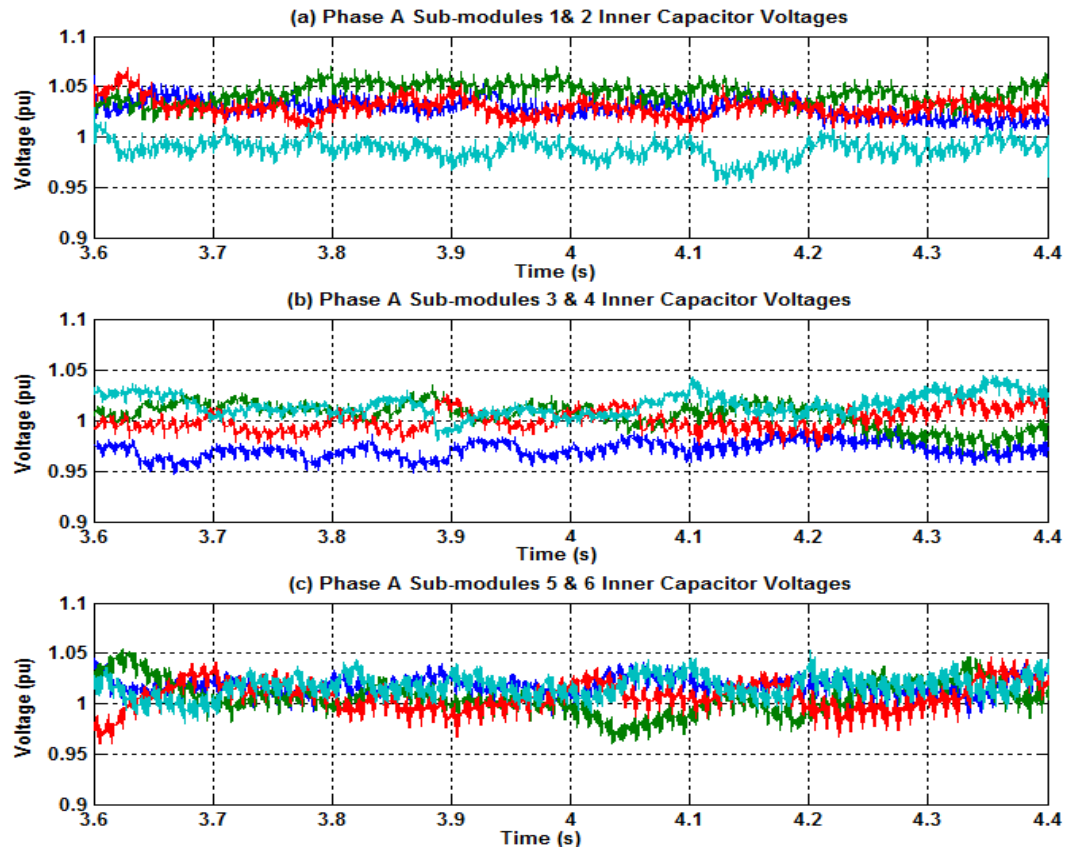


Figure 5.21: Converter Sub-module inner flying capacitor voltages across (a) phase A, (b) phase B and (c) Phase C.

## 5.5 Experimental System and Validation

The control strategy presented in the previous section for the FC-MMCC functioning as a STATCOM is practically verified. An experimental FC-MMCC designed, and implemented by previous researchers in the School of Electronic and Electrical Engineering, University of Leeds was used for this validation. The author developed the DSP software program code for implementing the FC-MMCC as a STATCOM. A simplified block diagram of the hardware system is shown in Figure 5.22. This consists of FC-MMCC, Load, a digital control part, and measurement part.

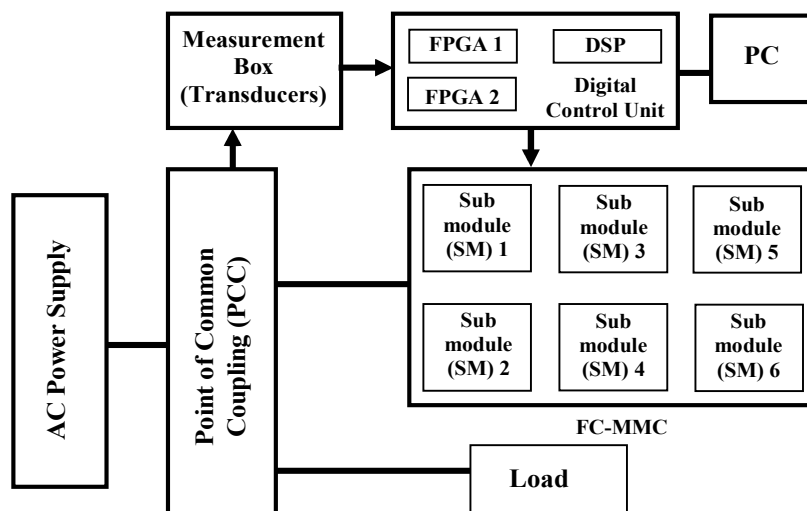


Figure 5.22: FC-MMCC STATCOM block diagram.

The FC-MMCC has six FCC sub-modules, two per phase limb. For total modularity and scalability, these sub-modules are constructed by assembling four half-bridge cells which basically has a flying-capacitor and a complementary pair of semiconductor switches as shown in Figure 5.23. The measurement unit consists of voltage and current transducers for measuring FC-MMCC capacitor voltages for feedback control and Power system voltage and currents for proper control of STATCOM operation. The digital control unit consists of the Digital Signal Processor (DSP) and Field Programmable Gate Array (FPGA) which perform functions of processing data from the transducers and further generating control functions for driving the FC-MMCC switches.



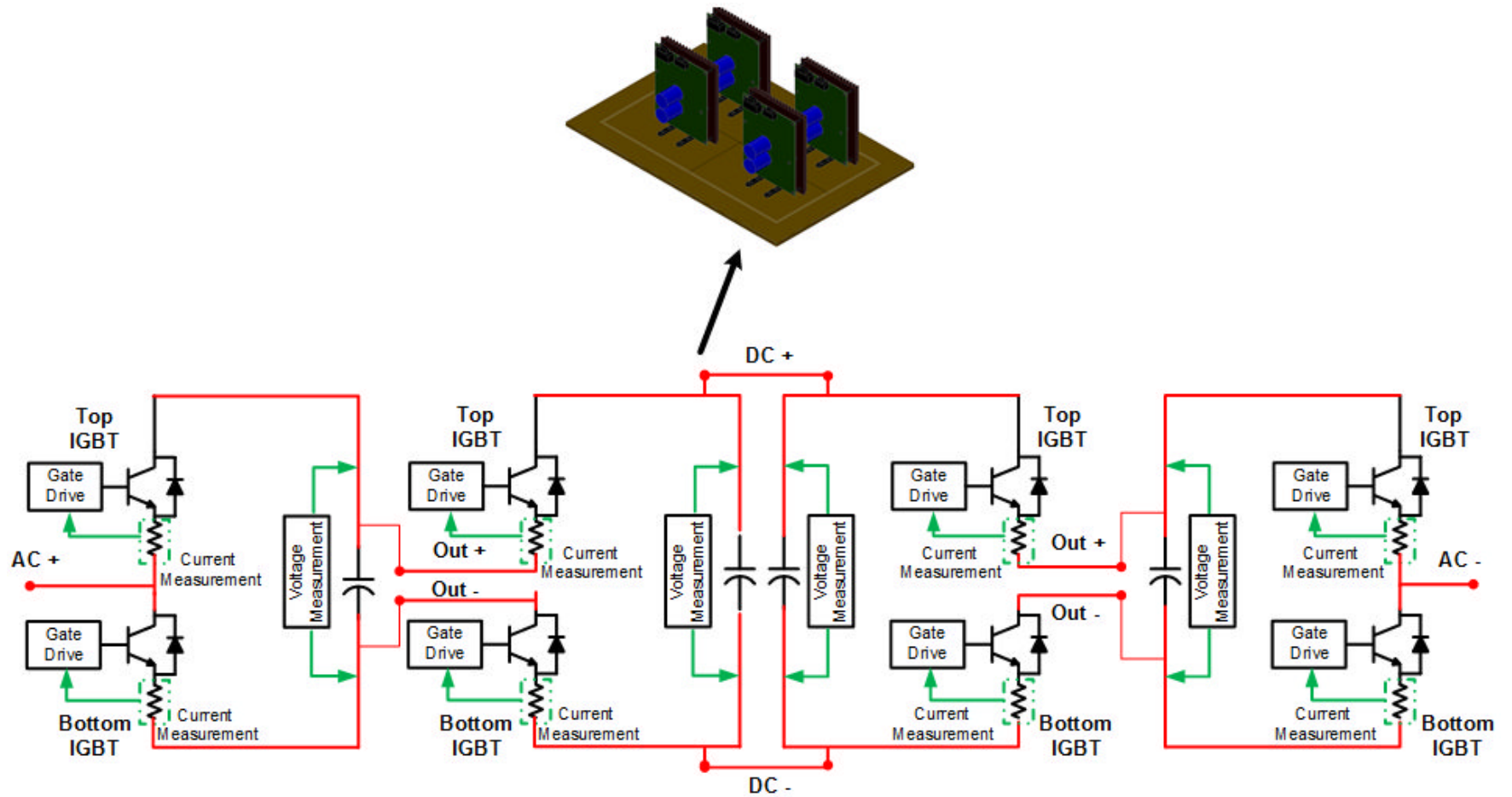


Figure 5.23: 5-level full bridge flying capacitor.

### 5.5.1 Cell card power circuit

The power cell card layout is a design of the control and power Applications Group at Leeds University [195] see Figure 5.24. This consist of a electrolytic capacitor, pair of complementary semiconductor switches, an isolated DC-DC 15V converter for powering gate drive circuits, over current protection, voltage and current sensor circuits and a fibre optic transmitter-receiver circuits for transferring switching pulses to the gate drive circuit. The power cell card PCB design and manufactured PCB power cell cards are shown in *Appendix C.5*. The protection circuit on the power cell cards is reset using S-R latch circuits when over current and voltage fault occurs.

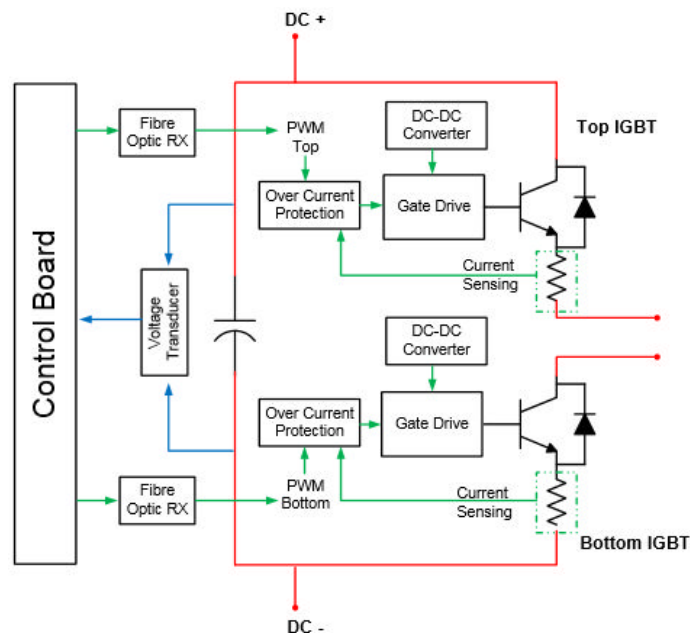


Figure 5.24: Power cell card circuit diagram.

The fibre optic Transmitter/Receiver circuit provides galvanic isolation between the digital and analogue control signals. These are based on Avago's technologies HBFR-1521 transmitter and HBFR-2351 receivers [196]. These are powered by 5V power supply. The output of this unit is fed into the gate drive circuit which provides the necessary voltage to drive the IGBT switches. This also provides galvanic isolation and are powered by 15V DC-DC converter. The power cell card power supply layout is shown in Figure 5.25. These power supplies include 3.3V, 5V, 15V and  $\pm 15V$  where the 5V is the main supply source on the cell cards. The linear voltage regulator generates the 3.3V power supply that powers the protection circuitry, while the  $\pm 15V$  power supply powers the voltage transducers for capacitor voltage measurement.

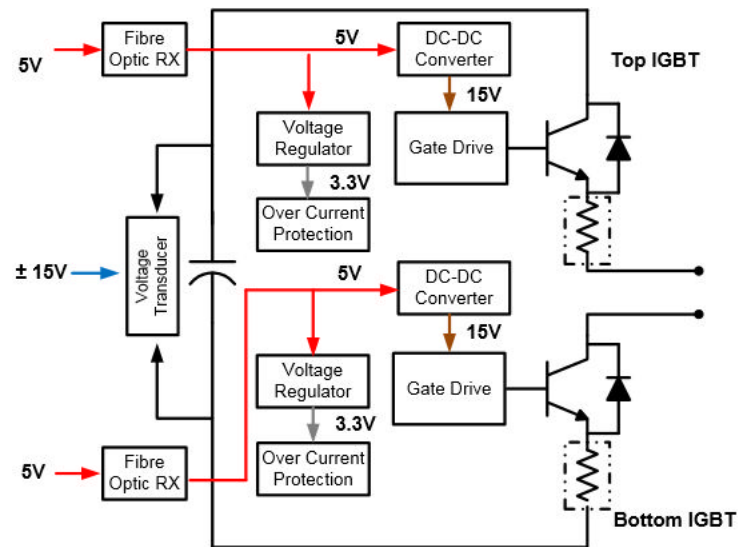


Figure 5.25: Power cell card power supply layout.

The switching device and capacitor characteristics are summarized in Appendix C.6.

### 5.5.2 Data Acquisition Unit

This comprises of transducers required for the measurement of voltage and current values of AC and DC quantities of FC-MMCC and Power system. The analogue signals are fed to the digital control unit and are applied for control signal calculation. For voltage measurement, the LEM LV 25-P is used [197] because of its linearity error of  $\pm 0.2\%$ , which gives an accuracy of  $\pm 0.8\%$ , having a conversion ratio of 1:2.5. This transducer has good resolution, high bandwidth and high immunity to noise and external interference. These were used for AC voltages measurement at the source, load and converter side and for DC voltages of the FC-MMCC capacitor voltages. The peak voltage rating of this transducer is 500V. Likewise, for current measurement, the LEM LA 55-P which uses Hall Effect is applied in capturing the current at the PCC, load and converter sides [198]. This has excellent resolution because it has a linearity error less than 0.15% and conversion ratio of 1:1000, and immunity to external interference. This has a conversion ratio of 1:1000 and has a peak current rating of 50A. The power circuit of both voltage and current transducers are shown in Appendix C.8. The measurement box is shown in Figure 5.26 consist of 9 LEM LV 25-P voltage and 9 LEM LA 55-P current transducers for measuring voltage and currents at the PCC, load and converter sides.

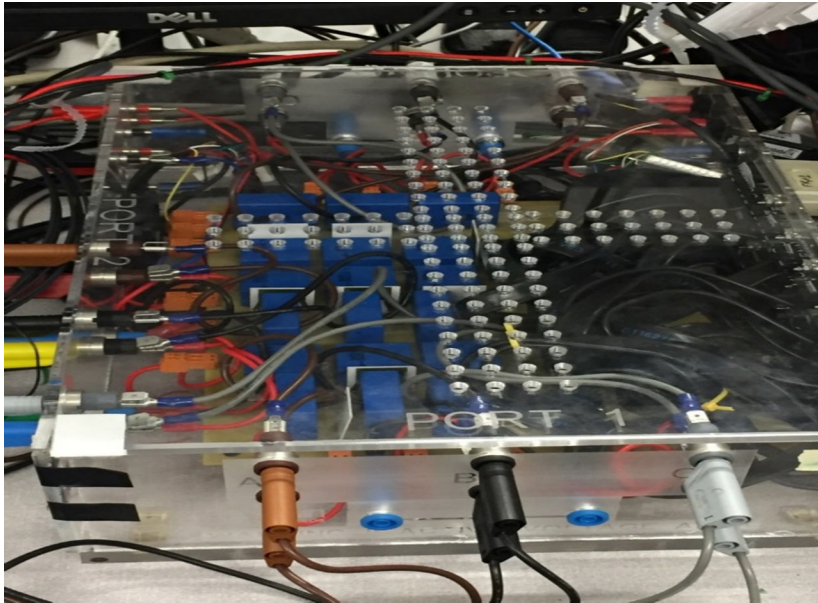


Figure 5.26: Measurement Box.

### 5.5.3 Digital Control unit

The control unit comprises of the digital signal processor and ProASIC FPGA module. The data acquired from the voltage and current transducers are converted into digital form in order to carry out the STATCOM control actions. The Host port interface (HPI) daughter card monitors the external memory interface (EMIF) which acts as a communication channel between DSP and FPGA. The code composer studio and Libero Soc are used in programming the DSP and FPGA.

#### 5.5.3.1 FPGA Cards

This sits on the 32 bit EMIF and communicates through a 7-bit address and 32-bit data buses with DSP. This performs functions of; (a) sampling/transmitting measured signals from transducers to DSP via an interrupt routine and (b) synthesizing switching pulses from control signals received from DSP. The interrupt service routine is triggered by the FPGA module which acts as the Master. This aids transferring the synthesized PWM switching pulses through fibre optic breakout boards to the fibre optic transmitter as shown in Figure 5.27. The Actel ProASIC FPGA layout its components are shown in *Appendix C.9*.

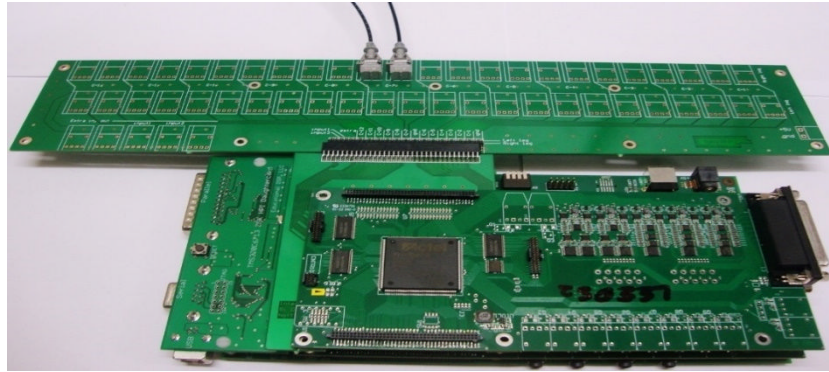


Figure 5.27: FPGA connected with Fibre Optic Break out Board.

### 5.5.3.2 Digital Signal Processor

The TMS320C6713 is a high-speed floating point processor having a clock frequency of 225MHz. This performs eight operation per instruction cycle due to its Harvard architecture. The HPI provides an interface for PC connection. The DSP LLCDSK6713HPI daughter card ensures real time access to data variables to the external memory while DSP is in operation. The DSP function as the main control centre as;

- (a) Receiving A/D measured signals from FPGA for STATCOM control.
- (b) Transferring reference control signals to FPGA for pulse signal generation.

A/D signals from FPGA are calibrated and converted back to their original values inside the DSP for proper implementation of STATCOM operation. This is done using (5.33)-(5.35).

$$S_{norm} = (S - S_{mid}) / S_{mid} \quad (5.33)$$

$$S_{mid} = (S_{Pk-Pk} / 2) - S_{Pk} \quad (5.34)$$

$$S_{actual} = S_{norm} \times C_f \quad (5.35)$$

where  $S$  = 16-bit signal from FPGA A/D converter,  $S_{mid}$  = mid-point,  $S_{norm}$  = normalised signal and  $C_f$  = transducers conversion factor.

### 5.5.4 Program Overview

The main program routine is mainly an initialisation routine which sets the external memory interface and initial control variables. The main program consists of two sub-routines namely the FPGA initialisation and PWM sub-routines.

**FPGA initialisation sub-routine**: this set-up the external interrupt service routine and clears the FPGA counters when its default state is activated.

Thereafter, the PWM dead time is set when the watchdog timer is enabled. In addition, the up-down counters that generate the triangular carriers are allocated with their initial values. This routine is in the active state only when the external interrupt has been triggered.

**PWM sub-routine:** this routine is only triggered when the FPGA triggers the external interrupt. This reads all the A/D signals from the FPGA and calibrate these digital signals to their original analogue form before performing control actions of PLL synchronisation, vector transformation, dc bus capacitor voltage control, Current reference control and predictive current controller that generates the sinusoidal modulation index reference waveforms which is fed back to the FPGA to synthesize gate signals to drive the FC-MMCC switches.

Figure 5.28 shows the flow chart of the main, FPGA initialisation and PWM sub-routines on how the software program works.

## 5.6 Experimental Validation

The experimental setup for validating the FC-MMCC functioning as a STATCOM is like that of the simulation study. Figure 5.29 shows the power system experimental circuit diagram and values of the components are listed in Table 5.2. Figure 5.30 shows the photograph of the experimental rig.

Table 5.2: Power system Characteristics

Rating	Value
PCC Side	3.0 kVA (110V, 10A)
Distribution Line	Aluminium PI TX line (d= 10mm, s= 1m, l=1.1 km) L =2mH, R = 0.4 $\Omega$ , X= 0.6283 $\Omega$ , Short circuit current = 137 A
Load Side	1.5 kVA (100V, 5 A) Load: 22 $\Omega$ , 47mH Power factor = 0.83 lagging
Converter Side	1.8 kVA (120V, 5A) Filter: 2.5 $\Omega$ , 2.25 mH DC Capacitor rating (per sub-module): 400 V, 1.12 mF (utilized at 60 V) Module Flying Capacitor: 400V, 0.56mF (utilized at 30 V)
Switching frequency	750 Hz

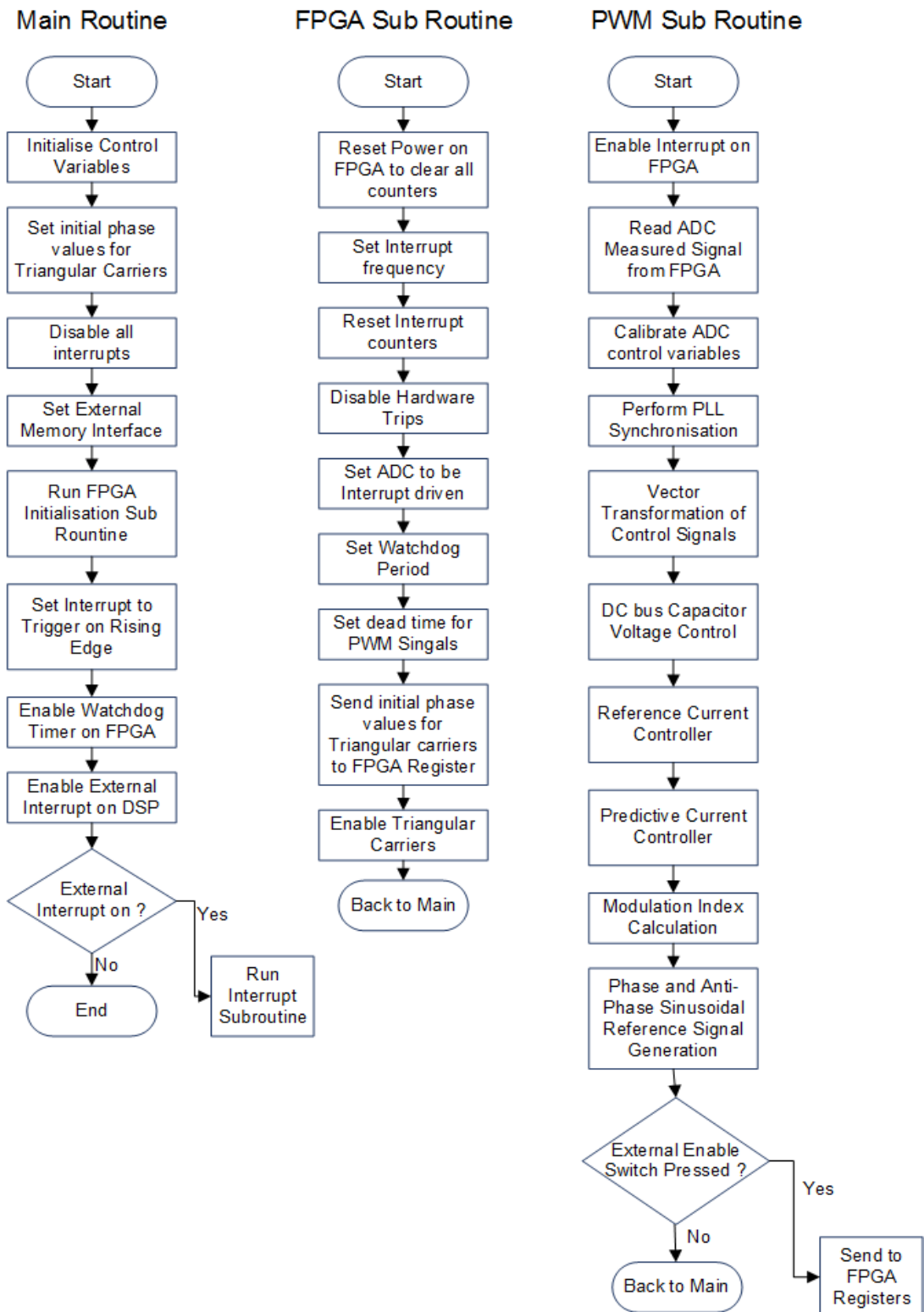


Figure 5.28: Program Flow Chart for Program Main, FPGA and PWM Routines.

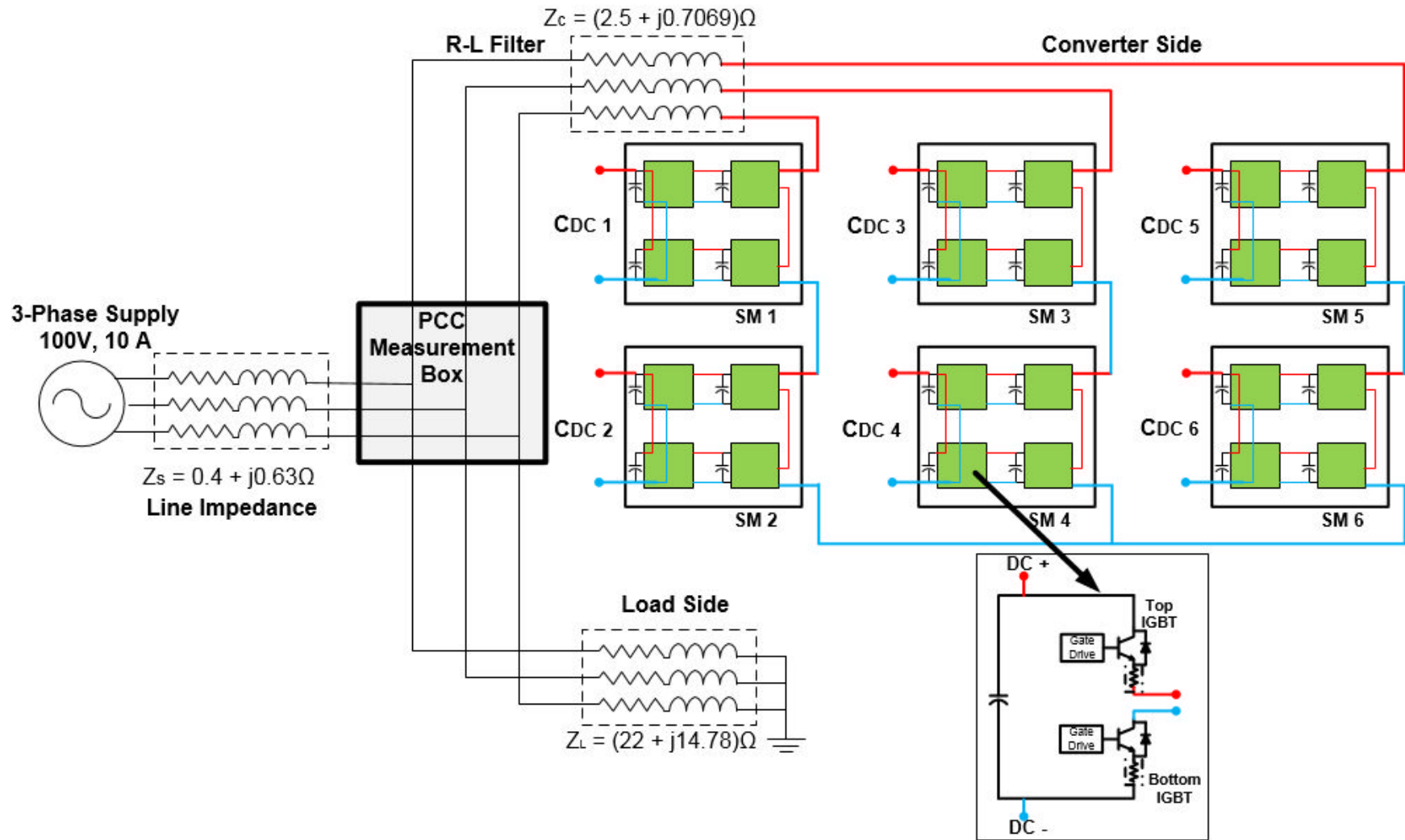


Figure 5.29: Experimental power system configuration.



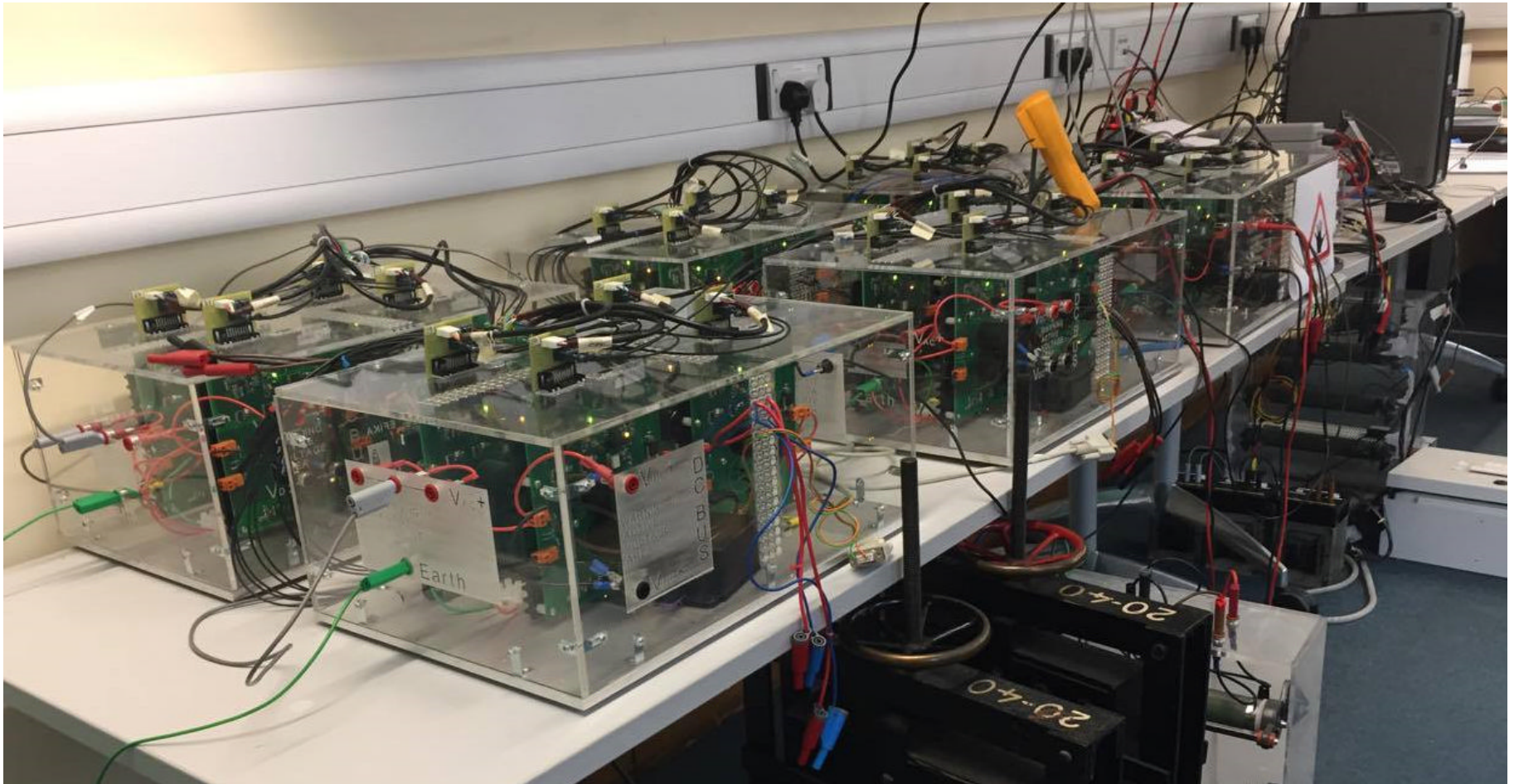


Figure 5.30: Experimental setup.

### 5.6.1 Control System Implementation

The real-time control scheme for the experimental rig is implemented using the DSP and FPGA as described in the previous section. The block diagram showing the implementation procedure as illustrated in Figure 5.31 is implemented in the DSP. The overall dc sub-module voltage is controlled using discrete time PI controller while the current control based on discrete time dead-beat predictive controller.

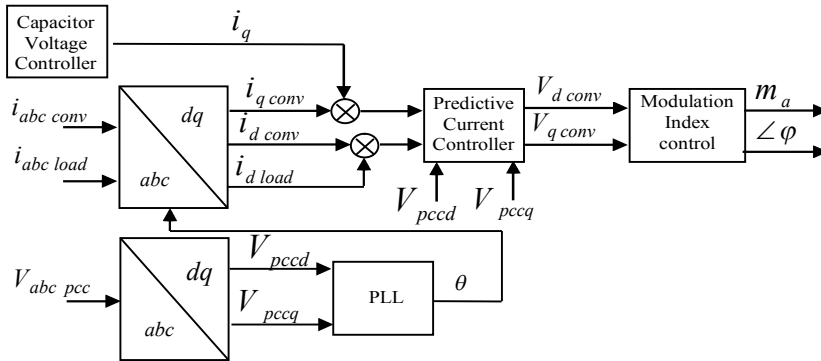


Figure 5.31: Block diagram of control system.

#### 5.6.1.1 Grid Synchronization

In this implementation, the synchronous reference frame phase lock loop technique has been implemented since the three phase voltages are balanced. Figure 5.32 shows the measured grid phase voltages, frequency and the phase angle from PLL for grid voltage synchronization.

#### 5.6.1.2 Discrete time PI Controller for sub-module DC voltage

The PI controller is implemented in controlling dc capacitor voltages. In order to implement the PI controller during the interrupt routine, digitized PI controller is designed and the equations describing its implementation is derived below.

$$V_{error} = V_{ref} - V_{actual} \quad (5.36)$$

$$V_{errori} = (V_{error} + V_{error\_prev})T_s \quad (5.37)$$

$$V = K_P(V_{error} + \frac{V_{errori}}{T_i})T_s \quad (5.38)$$

where  $V$  is generated PI control signal,  $V_{error}$  is the proportional error,  $V_{errori}$  is the integral error,  $T_i$  the integration time constant and  $T_s$  is the sampling or interrupt period which is set at 10 kHz. The proportional control gain and integration time constant for is controller are set to  $K_P=0.5$  and  $T_i=0.1$  in order

to attain minimum overshoot, fast settling time and minimum steady state error.

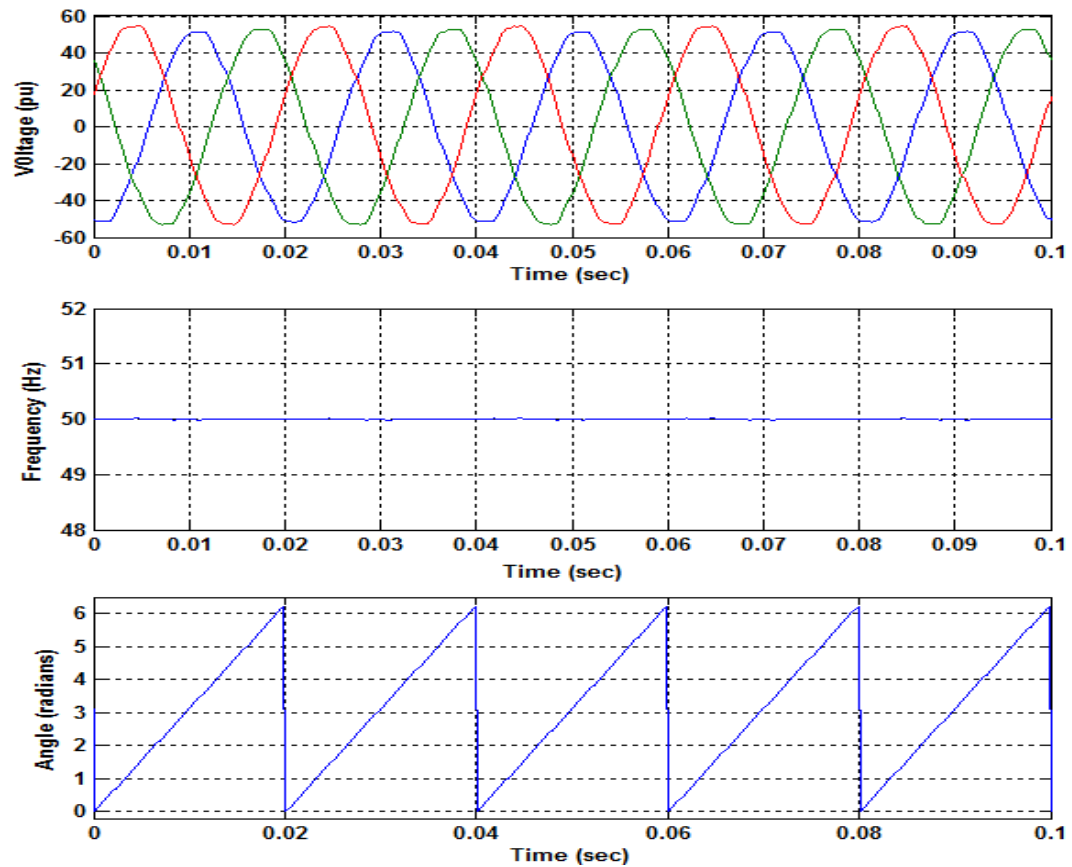


Figure 5.32: Synchronised grid voltage (a) PCC voltage (b) frequency and (c) Angle.

Also, the sample time of this controller is made to be 5 times the sampling time of the predictive current controller since the latter is required to be faster for stability. The predictive dead beat current controller implemented for the experimental setup is similar to the case discussed under the simulation studies.

### 5.6.1.3 Capacitor Pre-charge Control

Capacitor pre-charge operation ensures sub-module capacitor voltages to be at the desired voltage levels before converter compensation operation starts. This is achieved by regulating the sub-module dc capacitor voltages with the  $i_{q\ conv}$  component while  $i_{d\ conv}$  is set to zero. Figure 5.33 show the block diagram of pre-charge controller.

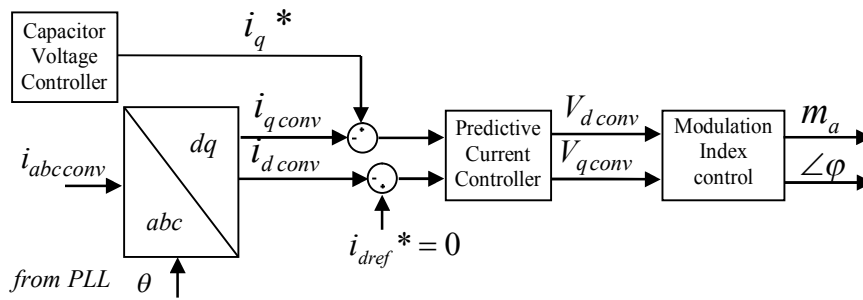


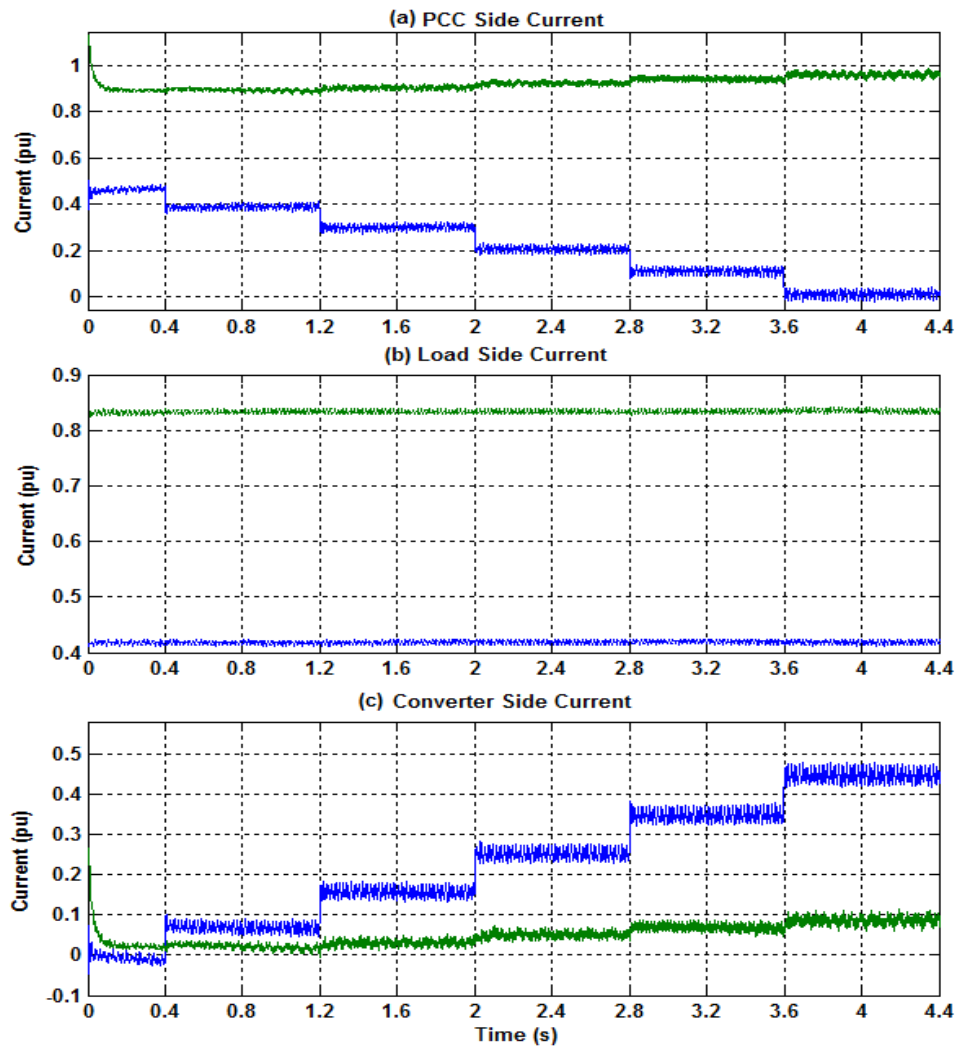
Figure 5.33: Block diagram for pre-charge controller.

## 5.6.2 Result and Discussion

Figure 5.29 shows the experimental setup with the converter switching frequency set to 750 Hz. At the start of the experiment, an inductive load is connected to absorb the reactive power of 900 VAR. During the time interval  $0s < t \leq 0.4s$  the converter sub-module capacitors are charged to the desired voltage level. At time intervals  $0.4s < t \leq 1.2s$ ,  $1.2s < t \leq 2.4s$ ,  $2s < t \leq 2.8s$ ,  $2.8s < t \leq 3.6s$  and  $3.6s < t \leq 4.4s$  the STATCOM controller is active to compensate 20%, 40%, 60%, 80% and 100% of load reactive power.

### 5.6.2.1 Active and Reactive Current responses

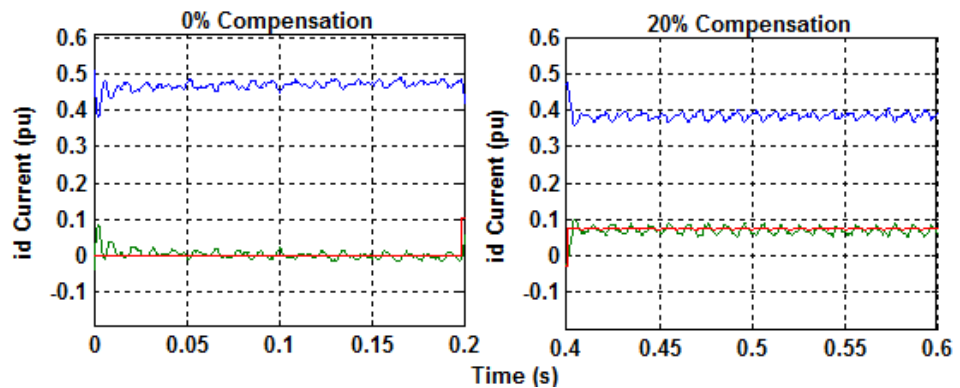
Figure 5.34 (a)-(c) shows the PCC, Load, and converter side real and reactive currents. At time intervals  $0 < t \leq 0.4$ ,  $0.4 < t \leq 1.2$ ,  $1.2 < t \leq 2.4$ ,  $2 < t \leq 2.8$ ,  $2.8 < t \leq 3.6$  and  $3.6 < t \leq 4.4$ , it is seen that the reactive current at PCC reduces from 2.4A (0.48pu) to 0A, corresponding to compensation modes of 0% to 100%. While the converter reactive currents increases from 0A to 2.4A (0.48pu). On the load side, the reactive current is unchanged. The PCC real current is seen to increase as the level of compensation increases due to the active power absorbed by the converter to maintain capacitor voltages. The PCC active current increases from 4.15A (0.83pu) to 4.625A (0.925pu) corresponding to 0% to 100% reactive power compensation.



Blue-Reactive current and Green-Active current component

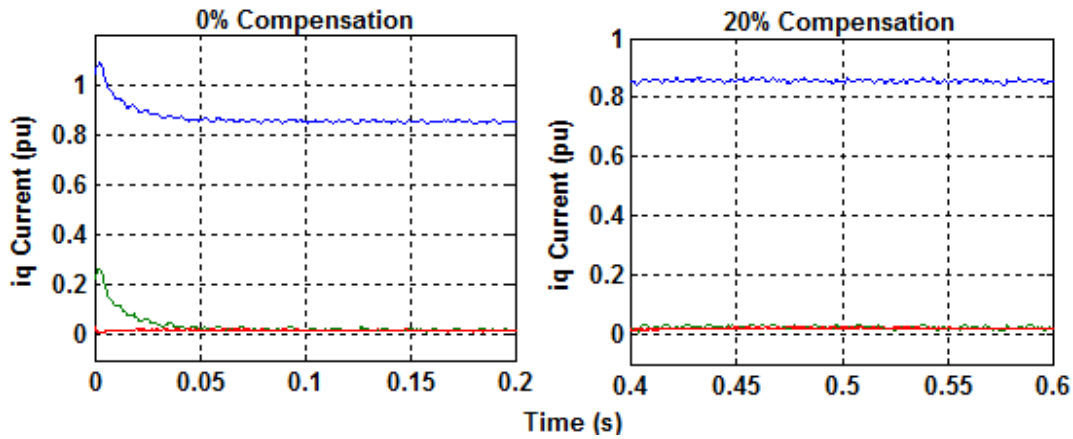
Figure 5.34: d-q current control, (a) PCC, (b) Load and (c) converter.

Figure 5.35 and Figure 5.36 show the STATCOM current step response at different compensation levels. It is seen that the STATCOM controller attains steady state within 40ms for both reactive ( $i_d$ ) and active currents ( $i_q$ ).



Blue- PCC current, Green- converter current, Red- current reference

Figure 5.35: Response time of STATCOM reactive current under each load condition Signals.

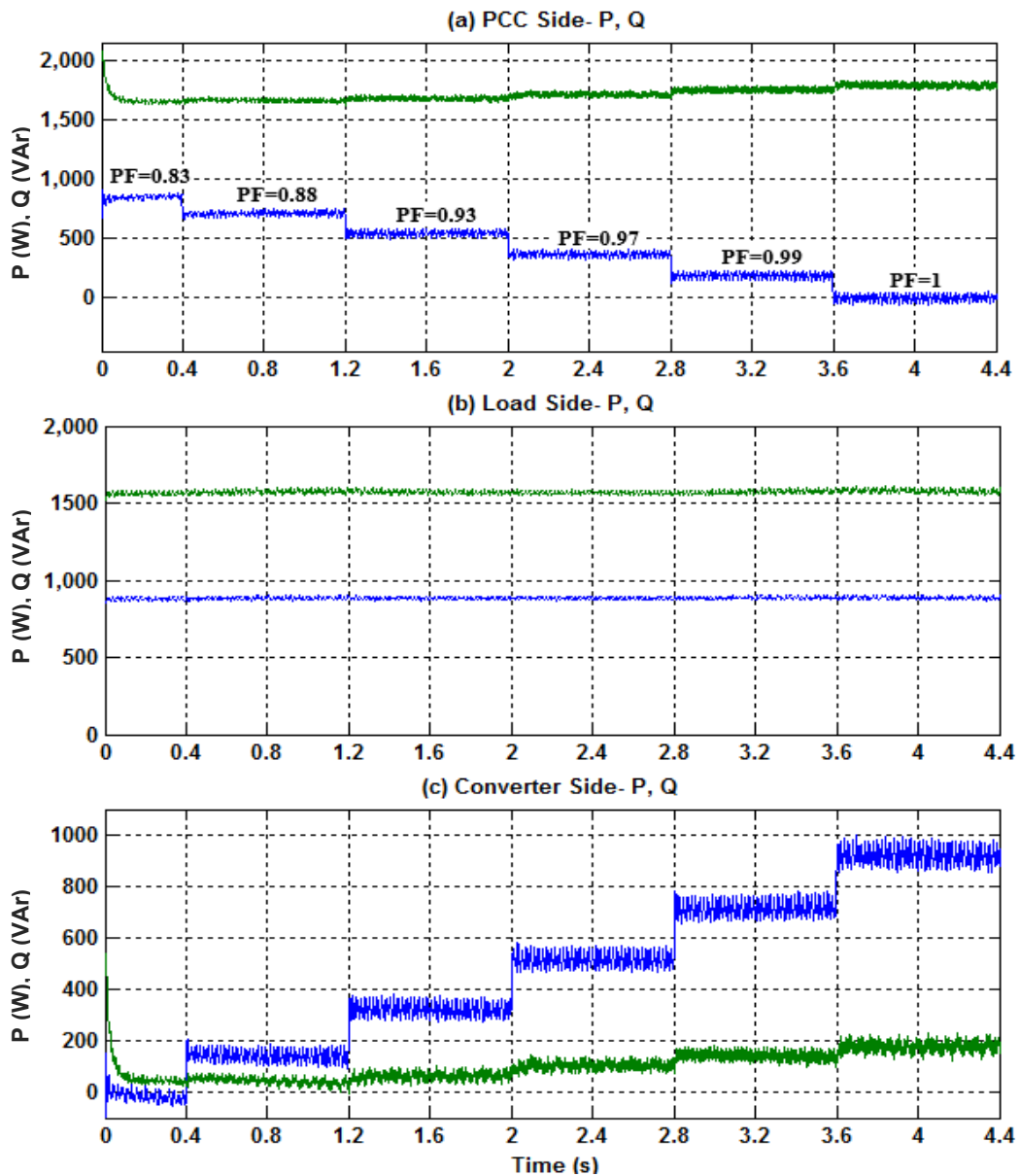


Blue- PCC current, Green- converter current, Red- current reference

Figure 5.36: Response time of STATCOM active current under each load condition Signals.

### 5.6.2.2 Active and Reactive power

Figures 5.37 (a)-(c) show the PCC, Load and converter active and reactive power. The active and reactive power responses across the PCC, load and converter sides are similar to their current responses. At time intervals  $0 < t \leq 0.4$  to  $3.6 < t \leq 4.4$  corresponding to 0% to 100% reactive power compensation, the PCC reactive and active powers decreases and increases from 900 VAR to 0 VAR and 1600 W to 1800 W respectively. The decrease in PCC reactive power results from converter reactive power injection whilst the PCC active power increases results from maintaining converter sub-module capacitor voltages and converter resistance filter power consumption compensation.



Blue-Reactive power and Green-Active power

Figure 5.37: Active and reactive power across (a) PCC, (b) Load and (c) converter sides.

### 5.6.2.3 PCC Voltage and current Responses

The PCC current magnitudes and angles at different compensation levels are shown in Figure 5.38 (a)-(b). While the PCC voltage and current waveforms are shown in Figure 5.39.

At  $t = 0$ , the PCC current magnitude and power factor angles increase initially depicting the current absorbed in charging converter sub-module capacitors. The PCC current values corresponding to each compensator increment of 0%, 20%, 40%, 60%, 80% and 100% are  $0.955 \angle 34^\circ pu$ ,  $0.93 \angle 28^\circ pu$ ,  $0.91 \angle 21.6^\circ pu$ ,  $0.915 \angle 14^\circ pu$  and  $0.925 \angle 0^\circ pu$ . This shows that the reactive power at PCC gradually reduces to zero as seen in Figure 5.38 (b).

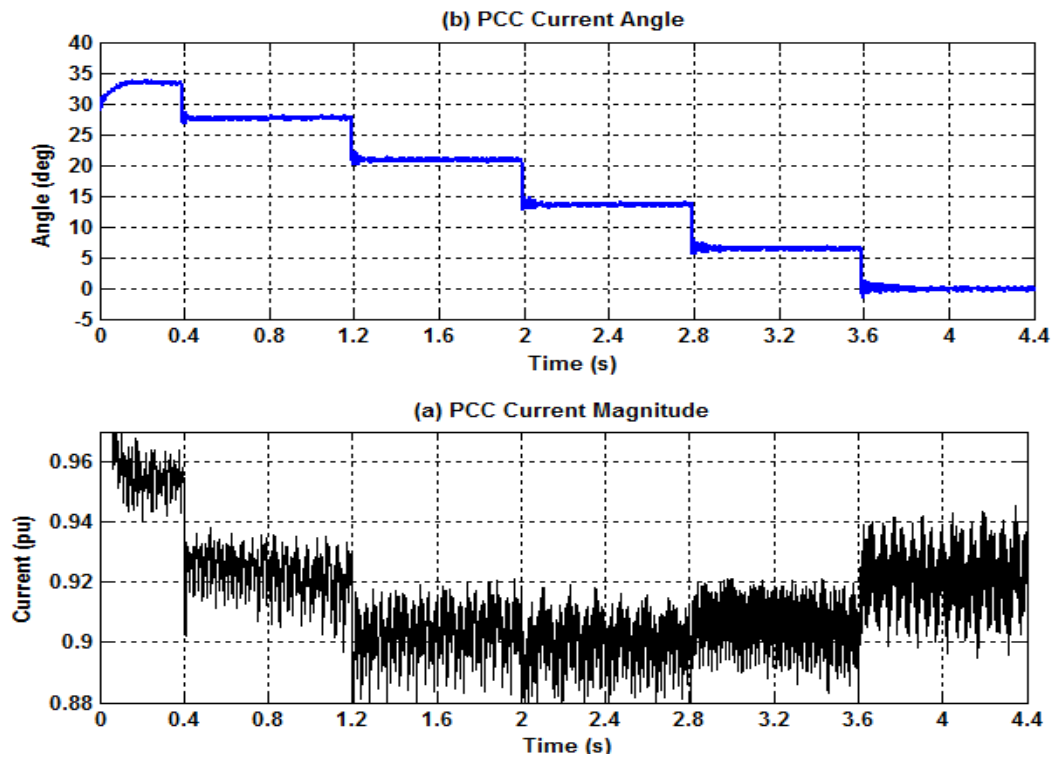


Figure 5.38: (a) PCC Current magnitude and (b) PCC Current angle.

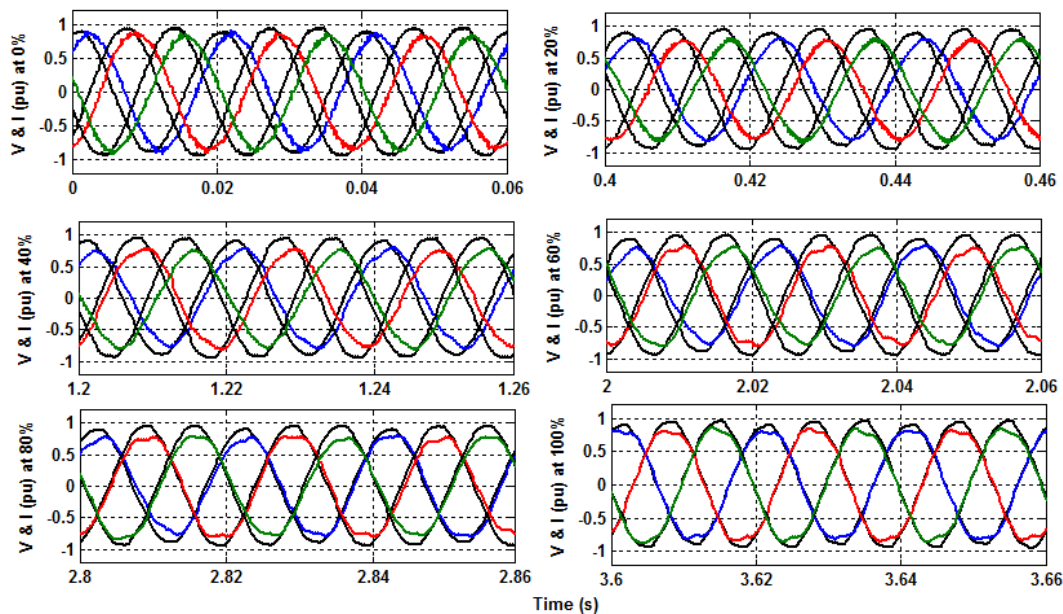


Figure 5.39: PCC voltage and current waveforms.

#### 5.6.2.4 Converter side waveforms

Figure 5.40 shows the voltage and current waveforms while the converter voltage and current magnitude and angle are shown in Figure 5.41 and 5.42 respectively. The converter current magnitude and phase angle with respect to compensation levels are,  $0.085 \angle 86^\circ pu$ ,  $0.185 \angle 84^\circ pu$ ,  $0.285 \angle 82^\circ pu$ ,



$0.385 \angle 81.5^\circ pu$  and  $0.485 \angle 80.5^\circ pu$  corresponding to 20%, 40%, 60%, 80% and 100% compensation mode respectively.

At compensation mode of 20%, 40%, 60%, 80% and 100% the converter terminal voltages are adjusted by the STATCOM controller to meet current requirement. The modulation index and converter angles are  $0.81 \angle -1^\circ pu$ ,  $0.81 \angle -4^\circ pu$ ,  $0.815 \angle -8^\circ pu$ ,  $0.8075 \angle -11^\circ pu$  and  $0.805 \angle -15^\circ pu$ . Figure 5.43 shows the converter voltage three-phase voltage waveforms having 9 distinct voltage levels.

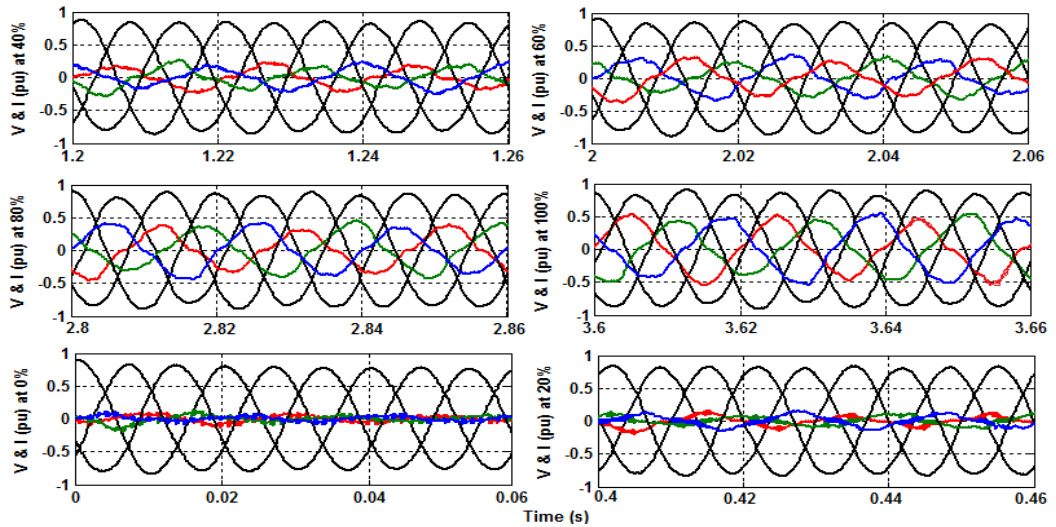


Figure 5.40: Converter voltage and current waveforms.

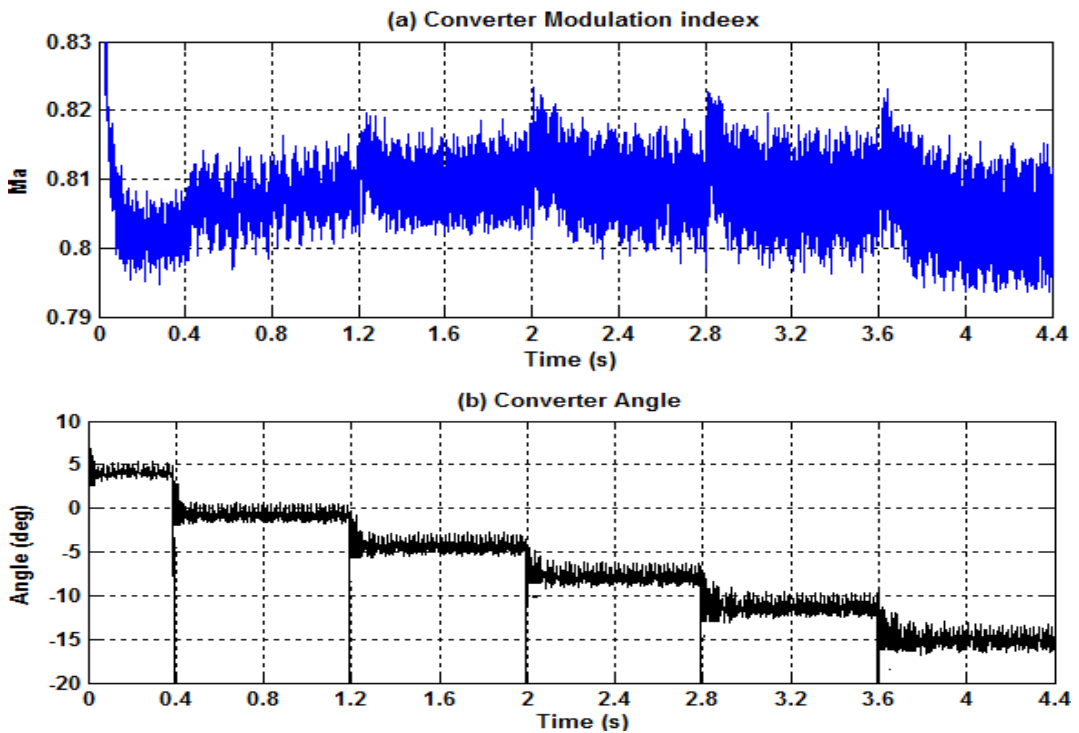


Figure 5.41: (a) Converter voltage magnitude and (b) angle at zero compensation, 20%, 40%, 60%, 80% and 100%.

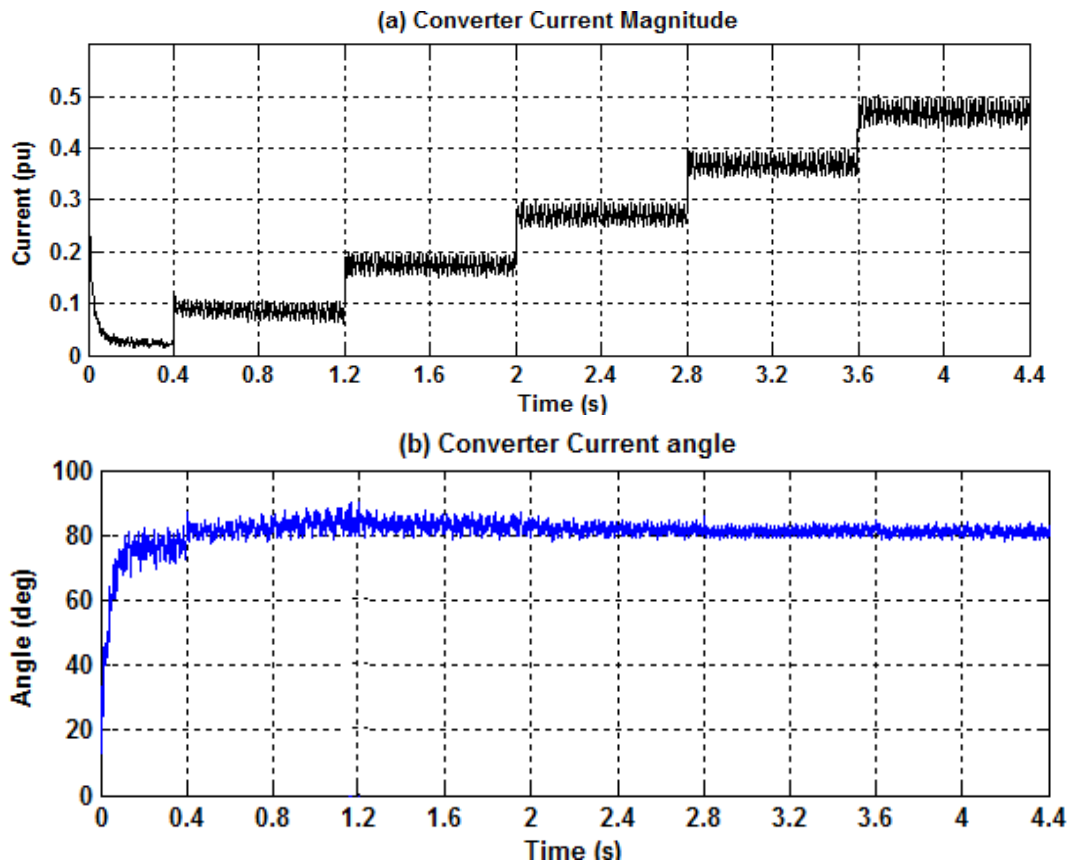


Figure 5.42: (a) Converter Current magnitude and (b) angle at zero compensation, 20%, 40%, 60%, 80% and 100%.

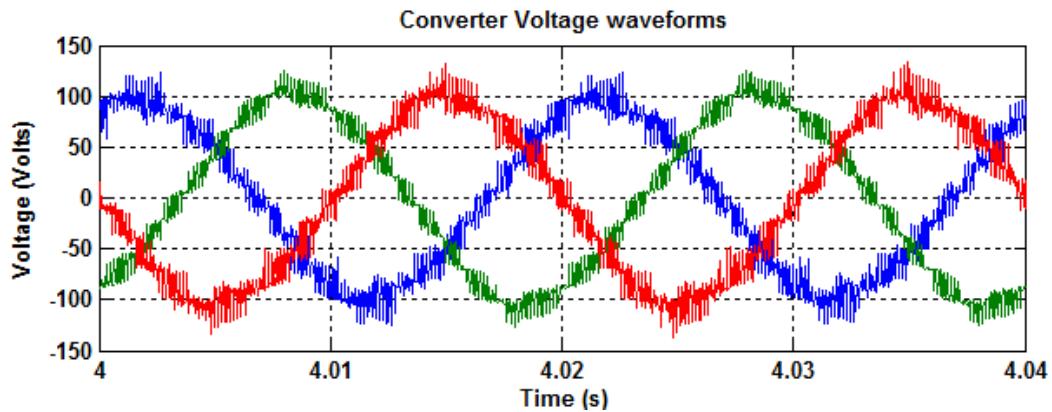


Figure 5.43: (a) converter Voltage waveforms.

### 5.6.2.5 DC capacitor voltages of converter

Figure 5.44 (a)-(c) shows sub-module capacitors while Figure 5.45 (a)-(c) shows the inner flying capacitor voltage waveforms. The sub-module and inner flying capacitors are seen to be maintained within 10% of their nominal rated values as seen in Figure 5.44 and 5.45 respectively. But the voltage ripples across each sub-module and inner flying capacitors increases as the current flowing through the converter increases due to the compensation level

increment. The sub-module and inner capacitor voltage ripples are seen to be  $\pm 5\%$  and  $\pm 2\%$  during 100% of converter compensation.

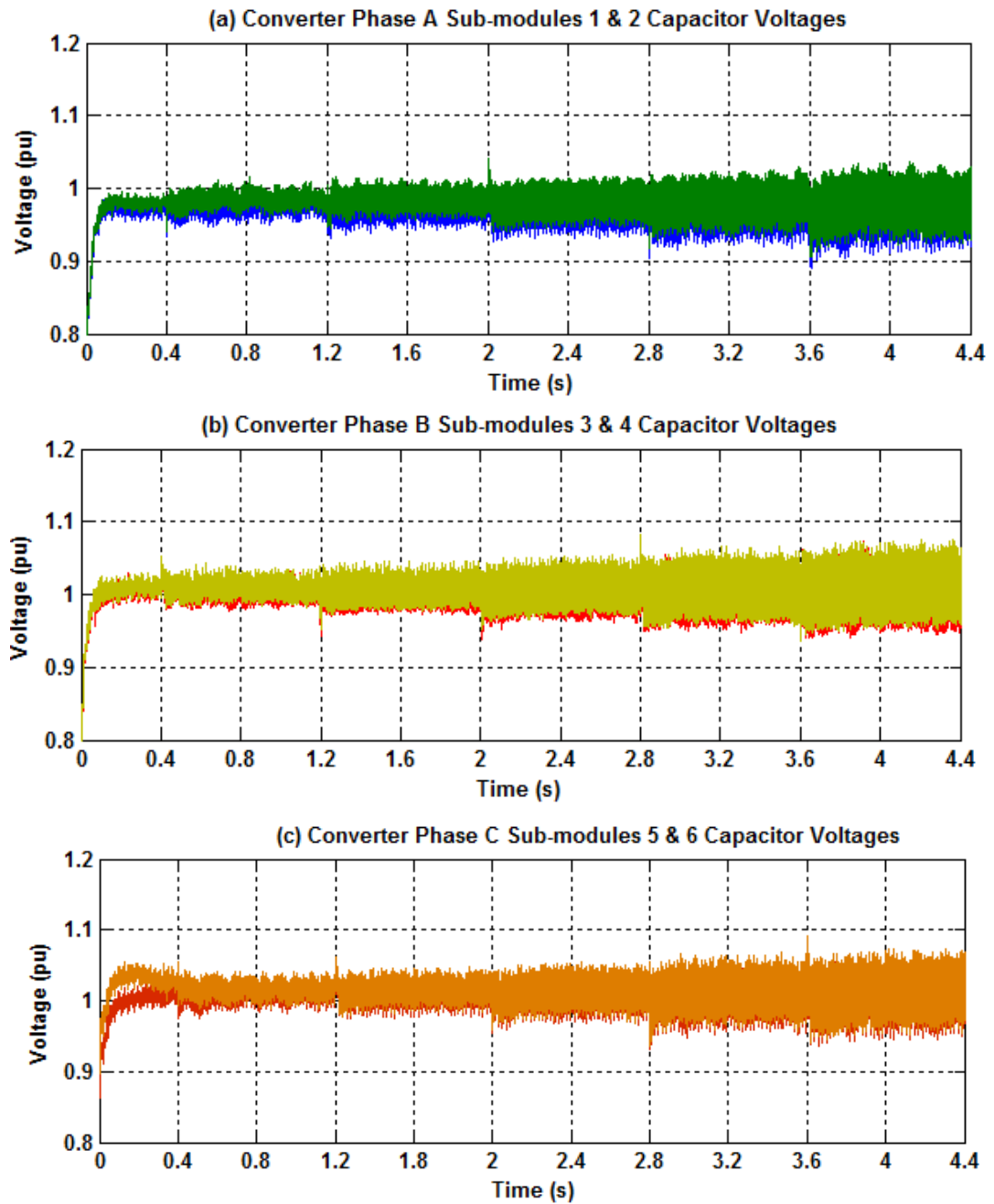


Figure 5.44: Converter Sub-module capacitor voltages across (a) phase A, (b) phase B and (c) Phase C.

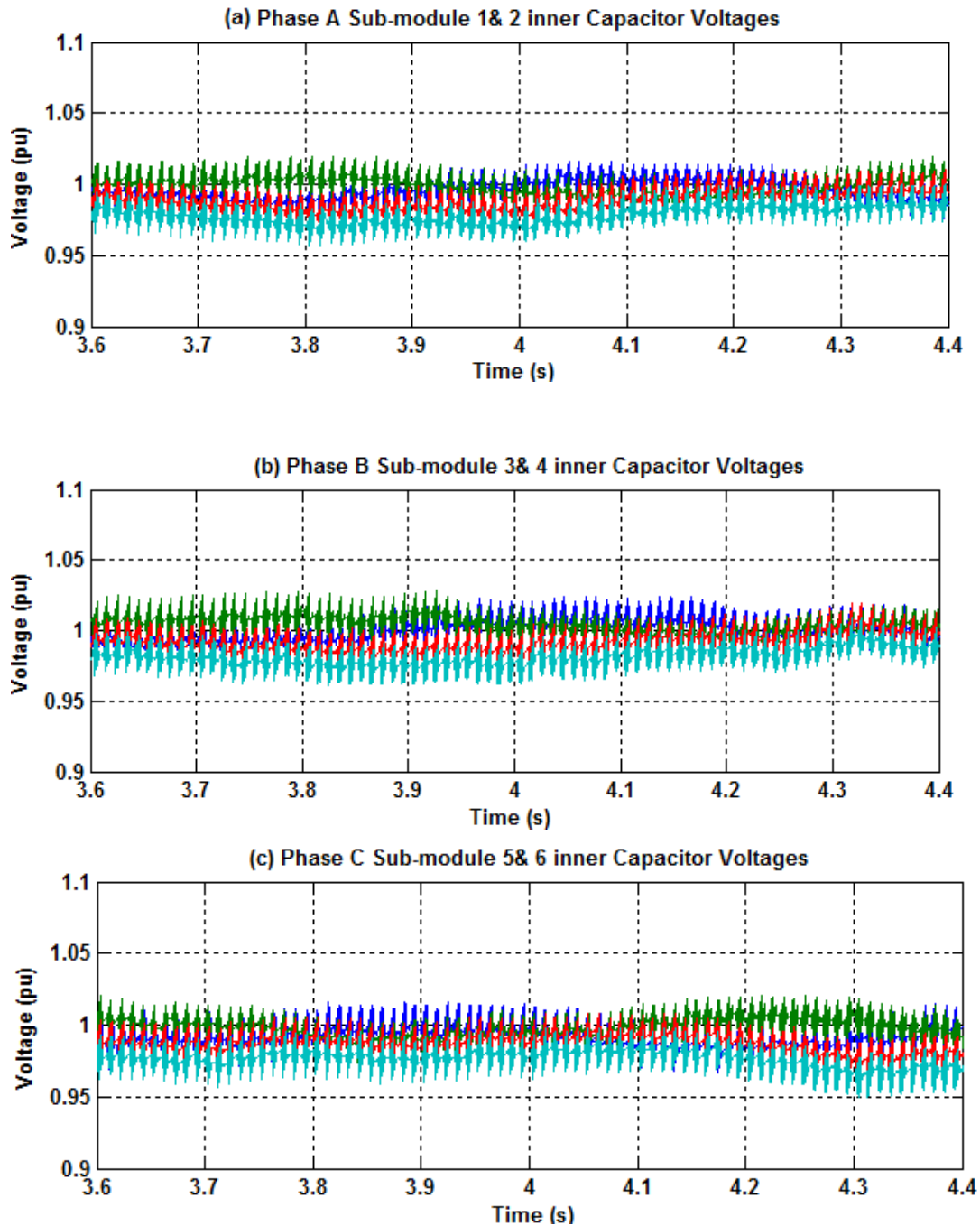


Figure 5.45: Converter Sub-module inner flying capacitor voltages across (a) phase A, (b) phase B and (c) Phase C.

The three phase voltage waveform of the supply source is shown in Figure 5.46, it is seen to be slightly unbalance. From the spectrum analysis of the voltage waveform, it is seen to contain odd harmonics of 3<sup>rd</sup>, 5<sup>th</sup>, 7<sup>th</sup> and 9<sup>th</sup> but all are less than 1% of the fundamental component.

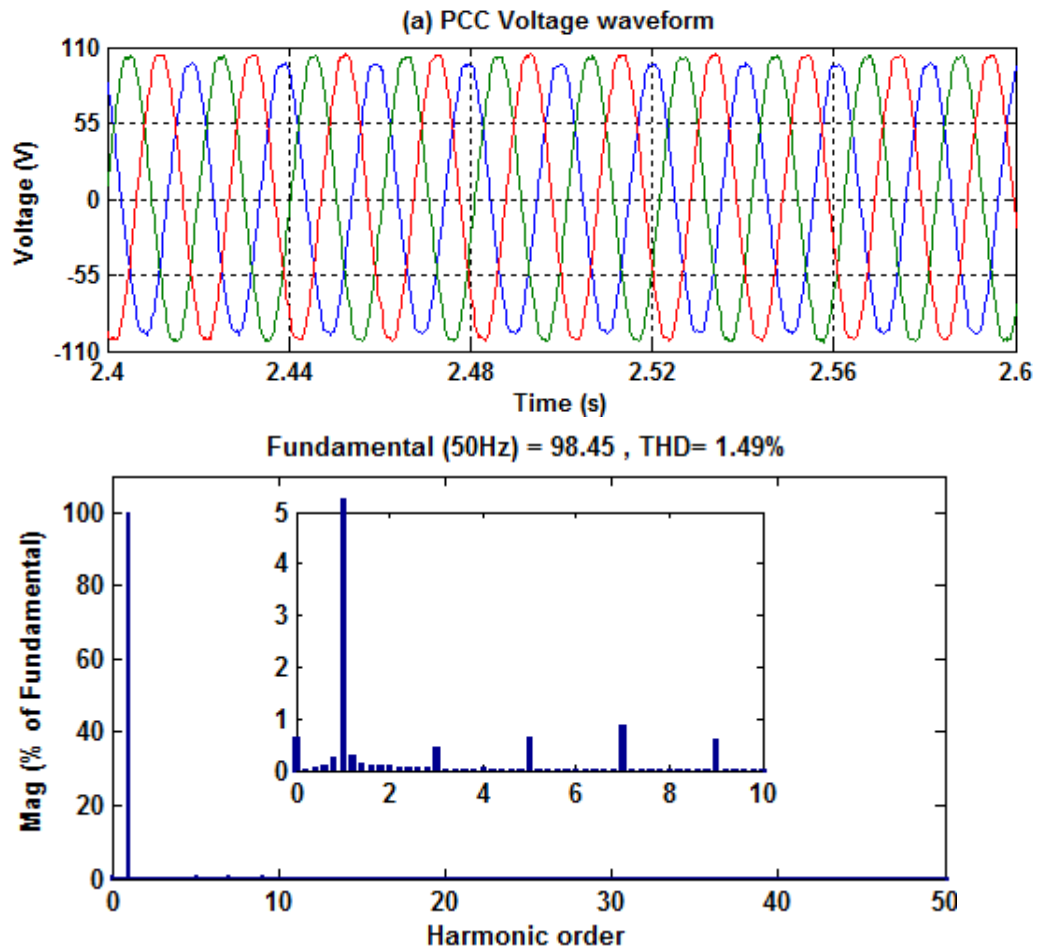


Figure 5.46: PCC voltage (a) three phase waveforms, and (b) phase A voltage Spectrum.

## 5.7 Conclusion

This chapter presented the operation principle and control scheme for making an MMCC to function as a STATCOM for reactive power compensation in a balanced power system. Equations for determining the required converter voltage and sub-module capacitor voltage ripple for reactive power compensation were derived. The control scheme consisting of an outer  $PI$  voltage control loop for the overall sub-module dc voltage and an inner dead-beat current controller has been explained in detail. Its application to an FC-MMCC with six sub-modules for reactive power compensation has been described and desired results were shown. Validation of the control scheme on an experimental FC-MMCC rig connected on a simple network were carried out, and results presented showing that unity power factor correction has been achieved under various operation conditions.

## **Chapter 6**

### **FC-MMCC Based STATCOM for Unbalanced Load Compensation**

This chapter examines the FC-MMCC STATCOM for compensating not only the load reactive power but also unbalanced load current in power distribution systems. As discussed in Chapter 1, three-phase current unbalance in a distribution network is common. The conditions are exacerbated by the widespread use distributed generators which are often single phase though they appear as unbalanced generators, rather than loads. A STATCOM can be effective in compensating the unbalanced load current, hence re-balance the current at PCC source end. With its advantages highlighted in chapter two, the H-bridge based MMCC STATCOM is considered the most suitable. However, because DC link capacitors per phase are separated, the MMCC has the problem of phase cluster DC voltages drifting away from their nominal value when working under unbalanced load. Consequently, it causes STATCOM malfunctioning, leading to distorted currents being injected into the grid, and possibly overstressing or even damaging the switching devices.

A method to address the balance problem is developed and presented in this chapter. The principle is to inject a non-sinusoidal zero sequence voltage/current composed of a fundamental plus its third harmonic component, which allows power sharing between the clusters but does not corrupt the current waveform injected into the grid. Applications of this approach to MMCC STATCOMs in both star and delta configurations are considered.

In this chapter the control technique for using MMCC- STATCOMs, in either star or delta configuration, to compensate the unbalanced load current, as well as reactive power, is presented. The phase cluster power imbalances due to such compensation are analysed, hence formulae for estimating zero sequence voltage/current to combat this imbalance are derived and presented in detail. The chapter then quantifies the operating ranges and required ratings due to the zero sequence and combined zero and third harmonic injection. Results are compared and discussed in detail.

#### **6.1 Circuit Configurations of an MMCC STATCOM**

Like the case discussed in Chapter 5, the MMCC STATCOM used for unbalanced operation also uses 5-L FC H-bridges as sub-modules and have N such modules cascaded per phase. Three phase limbs may be in either

star (SSBC) or delta connections (SDBC) as illustrated in Figure 6.1(a) and (b), they show different characteristics under unbalanced operation. For SSBC, the neutral points of the grid and converter sides are not connected together. As usual terminals of phase limbs are connected through reactive filters. For SDBC, the head and tail of two phase limbs are tied through a filter reactor to limit the current harmonics and handle their voltage differences between phase clusters. Here the grid is assumed having voltages at PCC noted as  $v_{Sm}$ , (where  $m=a, b, c$ ) and phase output currents from the converter  $i_m$ , which are unbalanced, hence have positive and negative sequence components. They are represented by the equations given as below.

$$v_{Sm} = V_p \sin(\omega t + \varphi_{vp} - k \frac{2\pi}{3}) + V_n \sin(-\omega t + \varphi_{vn} - k \frac{2\pi}{3}) \quad (6.1)$$

$$i_m = I_p \sin(\omega t + \varphi_{ip} - k \frac{2\pi}{3}) + I_n \sin(-\omega t + \varphi_{in} - k \frac{2\pi}{3}) \quad (6.2)$$

where subscripts  $p$  and  $n$  define the coefficients for the positive and negative components.  $k$  takes values  $k=0, 1, 2$  and  $\varphi_{vp}$ ,  $\varphi_{vn}$ ,  $\varphi_{ip}$  and  $\varphi_{in}$  are the phase angles of the positive and negative sequence voltages and currents.

In Figure 6.1 the dc capacitor voltages are  $V_{dcn}$ , (where  $m=a, b, c$  for star connection and  $m=ab, bc, ca$  for delta);  $n=1, 2, N$ ) for all the converter modules.

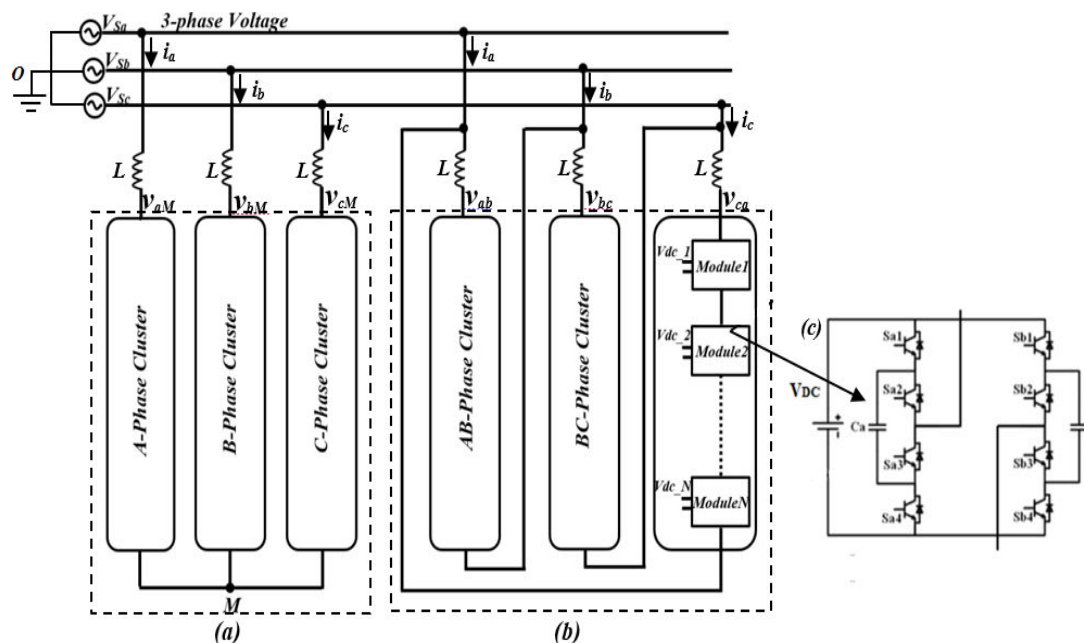


Figure 6.1: Configurations of Two MMCC STATCOMs namely (a) SSBC, (b) SDBC, with (c) 5L-FC as sub-module.

## 6.2 Inter-Cluster DC Voltage Balancing Control Based on Zero Sequence Components

### 6.2.1 Current Re-balance Control and Problem Caused

For a power system having load drawing three-phase unbalanced current, the MMCC-STATCOM in this system can be effective in overcoming the problem by enabling the current at the PCC to be re-balanced. This requires the MMCC-STATCOM supplying current having the negative sequence elements as expressed by equation (6.2). However the consequence of performing load current re-balance control result in the power per phase limb of MMCC, evaluated by multiplying (6.1) and (6.2), becomes unbalanced. These unbalanced active powers, flowing through the converter phases, causes converter inter-cluster dc capacitor voltage imbalance, in turn the MMCC will not work as required.

### 6.2.2 Analysis of Unbalance Phase Power and Zero Sequence Elements

To overcome the above problem the unbalanced power elements must be cancelled hence achieving equal active power flow through phase clusters. This can be obtained by injecting zero sequence and third harmonic components, Evaluations of the required zero sequence components are summarized below for both star and delta configured MMCCs.

For star connection the scheme injects zero sequence voltage, hence the converter phase voltage can be written as following while the current is given by equation (6.2):

$$v_{mM} = v_{Sm} + v_o = V_p \sin(\omega t + \varphi_{vp} - k \frac{2\pi}{3}) + V_n \sin(-\omega t + \varphi_{vn} - k \frac{2\pi}{3}) + V_o \sin(\omega t + \varphi_o). \quad (6.3)$$

For delta connection, zero sequence current is injected so we have converter voltages and currents expressions given as:

$$v_m = \sqrt{3}(V_p \sin(\omega t + \varphi_{vp} - k \frac{2\pi}{3} + \frac{\pi}{6}) + V_n \sin(-\omega t + \varphi_{vn} - k \frac{2\pi}{3} + \frac{\pi}{6})). \quad (6.4)$$

$$i_{mo} = i_m + i_o = \frac{1}{\sqrt{3}}(I_p \sin(\omega t + \varphi_{ip} - k \frac{2\pi}{3} + \frac{\pi}{6}) + I_n \sin(-\omega t + \varphi_{in} - k \frac{2\pi}{3} + \frac{\pi}{6})) + I_o \sin(\omega t + \varphi_o) \quad (6.5)$$

Figure 6.2 shows the definitions of both voltage and current variables for both MMCC configurations in a simplified circuit representation.



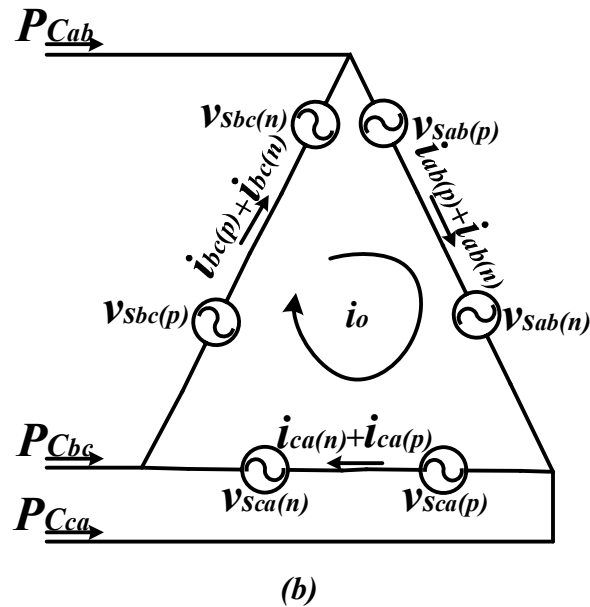
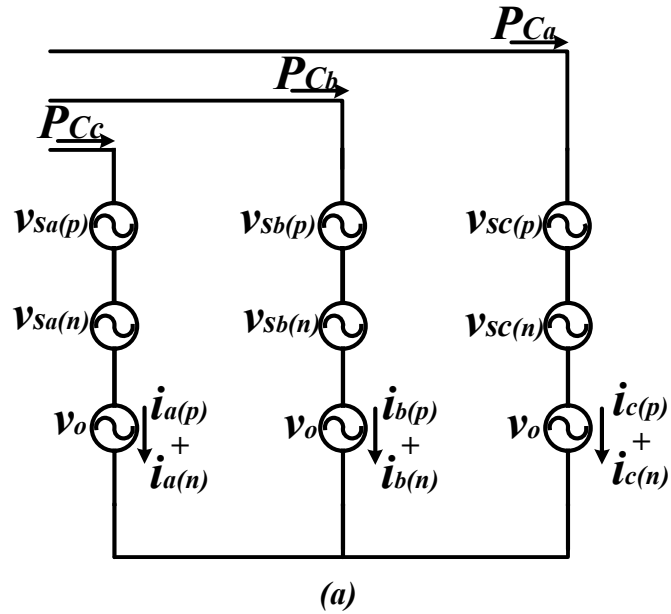
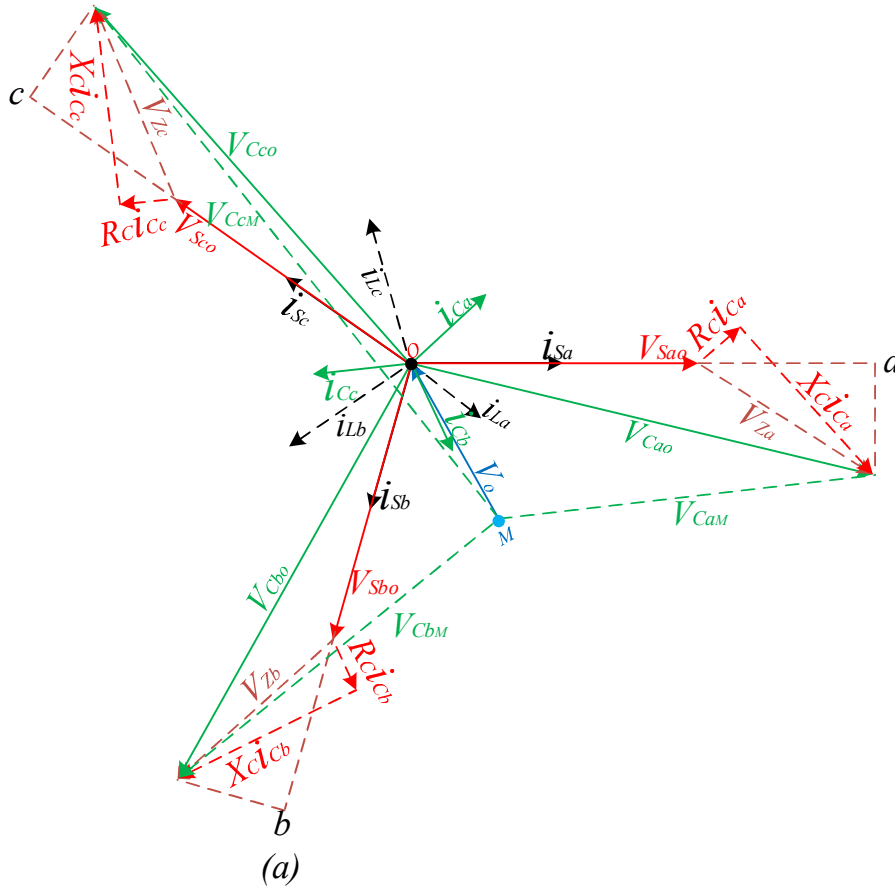


Figure 6.2: Circuits and variables in (a) MMCC-SSBC and (b) MMCC-SDBC.

The phasor diagram shown in Figure 6.3 (a) and (b) depicts situations where the STATCOM supplies both positive and negative sequence currents into the grid while injecting either zero sequence voltage (in Figure 6.3(a)) or current (in Figure 6.3 (b)). The unbalanced phase currents from the MMCC-STATCOMs are for compensating the load unbalance currents  $i_{Labc}$  by hence ensuring the grid currents to be balanced and in phase with the grid voltages  $v_{sabc}$  as shown in Figure 6.3.

The grid  $i_{sm}$  and load  $i_{Lm}$  currents are represented by black lines while the converter currents used in compensating the unbalanced load currents are represented by green lines. The converter voltages phasor are represented

by green lines. The initial converter voltages  $V_{cmo}$  neutral point  $\mathbf{o}$  are shifted to point  $\mathbf{M}$  by the addition of zero sequence voltage  $V_o$  represented by blue line in controlling the inter-cluster dc voltage imbalance, particularly for the SSBC-MMCC as shown in Figure 6.3 (a). While for the SDBC-MMCC, a zero sequence current  $i_o$  represented by blue line circulates around the converter for its inter-cluster dc voltage control.



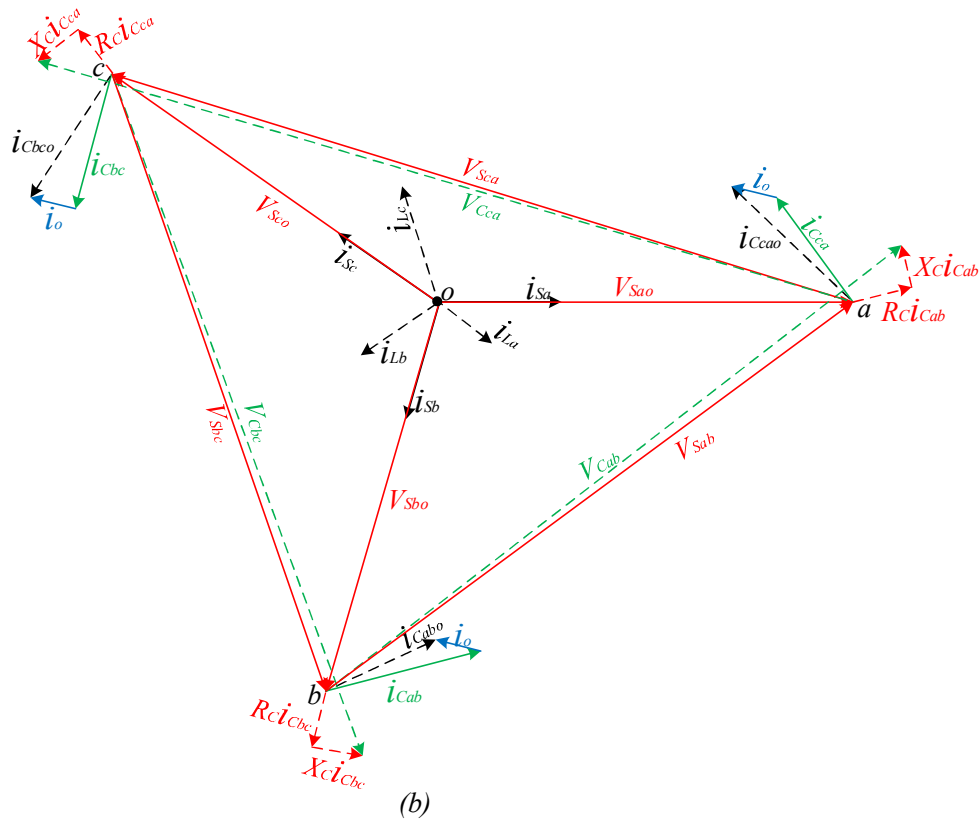


Figure 6.3: Voltage and Current phasor diagram for (a) SSBC and (b) SDBC-MMCC.

The subsequent instantaneous powers per phase cluster are evaluated according to [199] as:

$$\begin{aligned} p_m &= v_{m_o} \cdot i_m, m = a, b, c \text{ for star configuration, and} \\ p_m &= v_m \cdot i_{m_o}, m = ab, bc, ca \text{ delta configuration.} \end{aligned} \quad (6.6)$$

The average active power at each phase is calculated as:

$$P_m = \frac{\omega}{2\pi} \int_0^{\frac{2\pi}{\omega}} p_m dt \quad (6.7)$$

For SSBC-MMCC the average phase active power is obtained by multiplying (6.3) and (6.2) and averaging the product over time, is given by:

$$P_m = \frac{1}{2} \left( \begin{array}{l} V_p I_p \cos(\varphi_{vp} - \varphi_{ip}) + q \frac{1}{2} V_p I_n \cos(\varphi_{vp} + \varphi_{in}) + q \frac{1}{2} V_n I_p \cos(\varphi_{vn} + \varphi_{ip}) \\ + \underbrace{V_n I_n \cos(\varphi_{vn} - \varphi_{in})}_{P_{Cm}^{++} \text{ and } P_{Cm}^{--}} + r \frac{\sqrt{3}}{2} V_p I_n \sin(\varphi_{vp} + \varphi_{in}) + r \frac{\sqrt{3}}{2} V_n I_p \sin(\varphi_{vn} + \varphi_{ip}) \\ - q \frac{1}{2} V_o I_p \cos(\varphi_o - \varphi_{ip}) + q \frac{1}{2} V_o I_n \cos(\varphi_o + \varphi_{in}) \\ - r \frac{\sqrt{3}}{2} V_o I_p \sin(\varphi_o - \varphi_{ip}) - r \frac{\sqrt{3}}{2} V_o I_n \sin(\varphi_o + \varphi_{in}) \end{array} \right) \quad (6.8)$$

where,  $q$  and  $r$  take values  $q = -2, 1, 1$  and  $r = 0, +1, -1$  for  $m = a, b, c$ .

Likewise for SDBC-MMCC the average power per phase, given by multiplying (6.5) and (6.6) and time averaging the product, is expressed as:

$$P_m = \frac{1}{2} \left( \begin{array}{l} V_p I_p \cos(\varphi_{vp} - \varphi_{ip}) - q \frac{1}{2} V_p I_n \cos(\varphi_{vp} + \varphi_{in}) - q \frac{1}{2} V_n I_p \cos(\varphi_{vn} + \varphi_{ip}) \\ + \underbrace{V_n I_n \cos(\varphi_{vn} - \varphi_{in})}_{P_{Cm}^{++} \text{ and } P_{Cm}^{--}} + r \frac{\sqrt{3}}{2} V_p I_n \sin(\varphi_{vp} + \varphi_{in}) + r \frac{\sqrt{3}}{2} V_n I_p \sin(\varphi_{vn} + \varphi_{ip}) \\ + r \frac{3}{2} V_p I_o \cos(\varphi_{vp} - \varphi_o) - r \frac{3}{2} V_n I_o \cos(\varphi_{vn} + \varphi_o) \\ - q \frac{\sqrt{3}}{2} V_p I_o \sin(\varphi_{vp} - \varphi_o) + q \frac{\sqrt{3}}{2} V_n I_o \sin(\varphi_{vn} + \varphi_o) \end{array} \right) \quad (6.9)$$

where,  $q$  and  $r$  take values  $q = 1, -2, 1$  and  $r = +1, 0, -1$  for  $m = ab, bc, ca$  (delta) respectively.

As can be seen the first two terms in both power equations (6.9) and (6.10) are the products of positive sequence voltage and current (i.e.  $P_{Cm}^{++}$ ), and negative sequence voltage and current (i.e.  $P_{Cm}^{--}$ ); these active powers are provided by the grid to compensate for power losses within the converter. The remaining eight terms can be grouped into two equal sets; the first four are the cross products of both positive sequence voltage and negative sequence current (i.e.  $P_{Cm}^{+-}$ ), and negative voltage and positive sequence current (i.e.  $P_{Cm}^{-+}$ ). The second set is due to zero sequence elements; for star connection, these are the products of zero sequence voltage and positive current or negative sequence current (i.e.  $P_{Cm}^{o+}$  and  $P_{Cm}^{o-}$ ). For delta connection, they are zero sequence current multiplying respectively positive or negative sequence voltages (i.e.  $P_{Cm}^{+o}$  and  $P_{Cm}^{-o}$ ). The sum of these terms are written as:

$$P_{Cm} = \frac{1}{2} (P_{Cm}^{+-} + P_{Cm}^{-+} + P_{Cm}^{o+} + P_{Cm}^{o-}) \quad (6.10)$$

It is clear that non-zero  $P_{cm}$  causes phase cluster dc voltages drifting suppressing it requires exact estimation of the unknown zero sequence voltage  $v_o$  for the star topology and the single zero sequence current  $i_o$  for the Delta case.

### 6.2.3 Estimation of Zero Sequence Components

This can only be done via feedback control of per phase cluster dc-voltages. A method is proposed here as shown in Figure 6.4. The scheme consists of three voltage feedback loops one per phase, they all use the same reference voltage which is the average of all three phase cluster dc-voltages,  $V_{dc\_avg}$ . This compares each phase cluster's measured average voltage  $v_{dcn}$  and a PI controller is then used to generate the compensating current. Multiplying this with the measured  $v_{dcn}$  gives the required power to regulate the three phase cluster dc-voltages to the same nominal level. Furthermore the unbalanced active powers,  $P_{Cm}^{+-}$  and  $P_{Cm}^{+}$  can be applied to compare with the control loop output power. These powers are estimated through real-time measurement of PCC phase voltages and converter reference currents. The differences give per phase zero sequence average active powers ( $P_{Cm}^o$ ) as:

$$P_{Cm}^o = \underbrace{P_{Cm}}_{P_{CmFB}} - \underbrace{(P_{Cm}^{+-} + P_{Cm}^{+})}_{P_{CmFF}}, \text{ where } m = a, b, c \text{ for star, } ab, bc, ca \text{ for delta.} \quad (6.11)$$

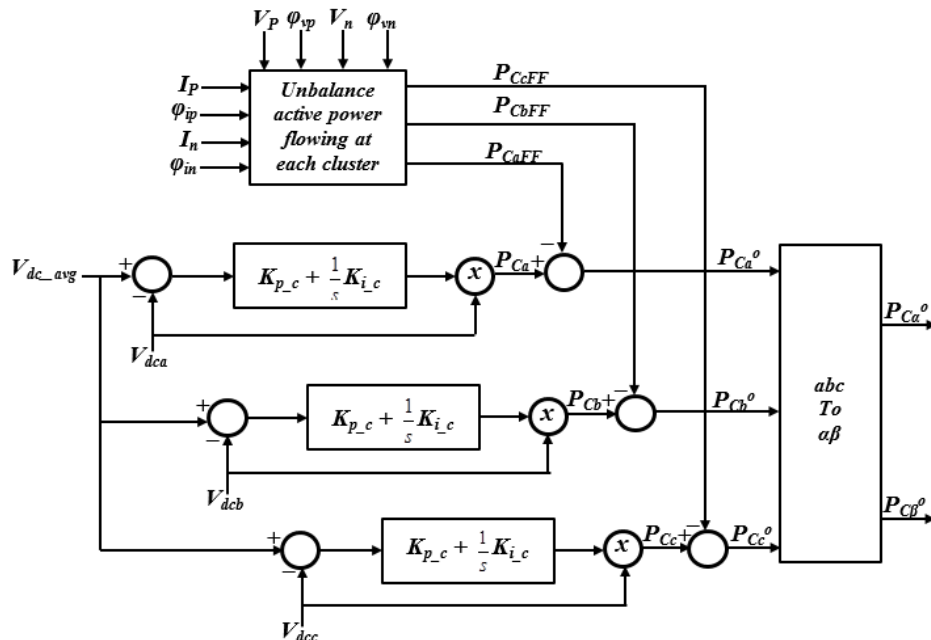


Figure 6.4: Diagram of cluster voltage balancing control.

The three-phase active power obtained is then transformed into  $\alpha$ - $\beta$  form, and can be written as functions of zero sequence voltage as:

$$\begin{bmatrix} P_{C\alpha}^o \\ P_{C\beta}^o \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} P_{Ca}^o \\ P_{Cb}^o \\ P_{Cc}^o \end{bmatrix} = \frac{1}{2} \begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{bmatrix} \begin{bmatrix} V_o \cos \phi_o \\ V_o \sin \phi_o \end{bmatrix} \quad (6.12)$$

where:

$$\begin{aligned} A_{11} &= (I_p \cos \phi_{ip} - I_n \cos \phi_{in}) \\ A_{12} &= (I_p \sin \phi_{ip} + I_n \sin \phi_{in}) \\ A_{21} &= (-I_p \sin \phi_{ip} + I_n \sin \phi_{in}) \\ A_{22} &= (I_p \cos \phi_{ip} + I_n \cos \phi_{in}) \end{aligned} \quad (6.13)$$

Likewise the zero sequence current is given by:

$$\begin{bmatrix} P_{Ca}^o \\ P_{C\beta}^o \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} P_{Cab}^o \\ P_{Cbc}^o \\ P_{Cca}^o \end{bmatrix} = \frac{\sqrt{3}}{4} \begin{bmatrix} B_{11} & B_{12} \\ B_{21} & B_{22} \end{bmatrix} \begin{bmatrix} I_o \cos \phi_o \\ I_o \sin \phi_o \end{bmatrix} \quad (6.14)$$

$$\begin{aligned} B_{11} &= \sqrt{3}(V_p \cos \phi_{vp} - V_n \cos \phi_{vn}) + (-V_p \sin \phi_{vp} + V_n \sin \phi_{vn}) \\ B_{12} &= (V_p \cos \phi_{vp} + V_n \cos \phi_{vn}) + \sqrt{3}(V_p \sin \phi_{vp} + V_n \sin \phi_{vn}) \\ B_{21} &= (-V_p \cos \phi_{vp} + V_n \cos \phi_{vn}) + \sqrt{3}(-V_p \sin \phi_{vp} + V_n \sin \phi_{vn}) \\ B_{22} &= \sqrt{3}(V_p \cos \phi_{vp} + V_n \cos \phi_{vn}) - (V_p \sin \phi_{vp} + V_n \sin \phi_{vn}) \end{aligned} \quad (6.15)$$

The zero sequence voltage and current can then be expressed as:

$$\begin{bmatrix} V_o \cos \phi_o \\ V_o \sin \phi_o \end{bmatrix} = \frac{2}{I_p^2 - I_n^2} \begin{bmatrix} A_{22} & -A_{12} \\ -A_{21} & A_{11} \end{bmatrix} \begin{bmatrix} P_{Ca}^o \\ P_{C\beta}^o \end{bmatrix} \quad (6.16)$$

$$\begin{bmatrix} I_o \cos \phi_o \\ I_o \sin \phi_o \end{bmatrix} = \frac{1}{\sqrt{3}(V_p^2 - V_n^2)} \begin{bmatrix} B_{22} & -B_{12} \\ -B_{21} & B_{11} \end{bmatrix} \begin{bmatrix} P_{Ca}^o \\ P_{C\beta}^o \end{bmatrix} \quad (6.17)$$

where the magnitude and phase angle of the zero sequence voltage and current are given as:

$$\begin{aligned} m_o &= \sqrt{(m_o \cos \phi_o)^2 + (m_o \sin \phi_o)^2} \\ \phi_o &= \arctan \left( \frac{m_o \sin \phi_o}{m_o \cos \phi_o} \right), \text{ where } m = V \text{ and } I \end{aligned} \quad (6.18)$$

The detailed derivation procedure of the zero sequence component is given in appendix D1. It can be seen from (6.17) that for the SSBC-MMCC, the zero sequence voltage becomes infinite large (i.e.  $v_o \rightarrow \infty$ ) when,  $I_n \approx I_p$ , consequently resulting in one or two converter phase voltages requiring unlimited high cluster dc-link voltage which is not realisable. Thus the capability of a SSBC-MMCC STATCOM for unbalanced load compensation is limited by the rating of its phase cluster voltages. However, this is not the case for the delta connection. From (6.18), the zero sequence current circulating between the phases increases with the magnitude of  $I_p$  and  $I_n$ , but does not tend to infinity when  $I_n \approx I_p$ .

### 6.3 Control of MMCC STATCOMs for Unbalance Load Compensation

The control system for an MMCC STATCOM for unbalanced load compensation consists of mainly three parts as shown in Figure 6.5; these are the phase cluster dc-voltage control due to unbalanced power and that due to balanced converter power losses, and the converter current control loop. The synchronous rotating  $dq$  reference frame is used for this control system (the derivation is shown in appendix D2). The DDSRF phase locked loop discussed in Chapter one is used to synchronize all MMCC variables to the grid voltage, i.e. transforming the stationary quantities into  $dq$  rotating frame using grid voltage as the reference synchronization angle  $\theta$ .

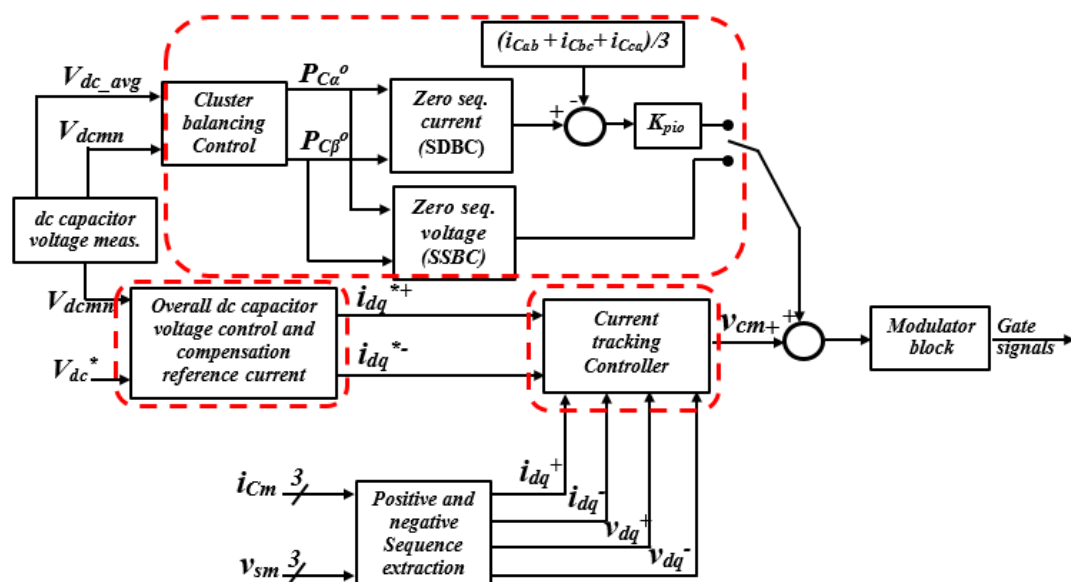


Figure 6.5: Overall unbalance Load compensation block diagram.

#### 6.3.1 DC-link voltage control

The dc-link voltage control is divided into two parts namely;

1. Overall dc-link voltage control
2. Inter phase cluster voltage balancing control

The overall dc-link voltage control provides the active power required to maintain each dc capacitors to their required/desired values in all three phases. This active power required by all the dc capacitors are determined through a *PI* regulator as shown in Figure 6.6. The direct component of the positive sequence current is:

$$i_q^{+*} = (K_{p\_dc} + K_{i\_dc}/s)(V_{dc}^* - V_{dc\_avg}) \quad (6.19)$$

where  $k_{p\_dc}$  and  $k_{i\_dc}$  are the proportional and integral gain of *PI* regulator,  $V_{dc}^*$  is the desired reference value of the dc-link and  $V_{dc\_avg}$  is the average value of all three phase sub-module dc-voltages.

The inter-cluster voltage control evaluates the zero sequence voltage or current for either star or delta-based MMCC. The zero sequence voltage calculated for the SSBC-MMCC is directly summed to the converter output reference voltages from the predictive current controller (see Figure 6.6); while for the SDBC-MMCC, the zero sequence current is converted into a voltage command through a proportional controller as:

$$V_A = K_{io} \left( -\frac{(i_{ab} + i_{bc} + i_{ca})}{3} + I_o \sin(\omega t + \phi_o) \right) \cdot \quad (6.20)$$

This voltage command is also added to the output of the predictive current controller.

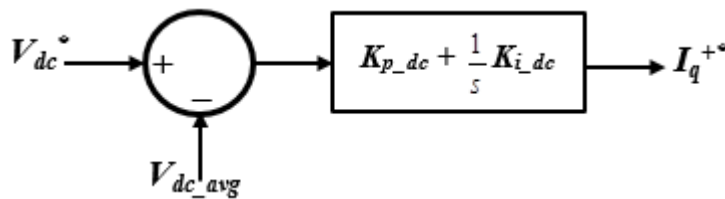


Figure 6.6: Overall dc capacitor voltage control.

Figure 6.7 shows the flowchart of the control algorithm for both SSBC and SDBC STATCOMs for performing reactive power and unbalanced load compensations. Firstly the negative sequence and positive sequence reactive currents are extracted from the measured load current, leaving only the positive sequence active currents which will be supplied by the source at PCC. Meanwhile, the required active current due for the overall sub-module dc capacitor voltage balancing is computed. Both these current elements are combined to form the STATCOM reference value for its current control. The next step involves evaluating the magnitude and angle of zero sequence



components ( $v_o$  for SSBC and  $i_o$  for SDBC). These use the currents evaluated from the first step, PCC voltages and the inter-cluster active powers and apply equation (6.18). The calculated zero sequence components are then combined with the reference converter voltages obtained from the current control loop, forming the reference voltage signals required by the PWM scheme for the converter switching control.

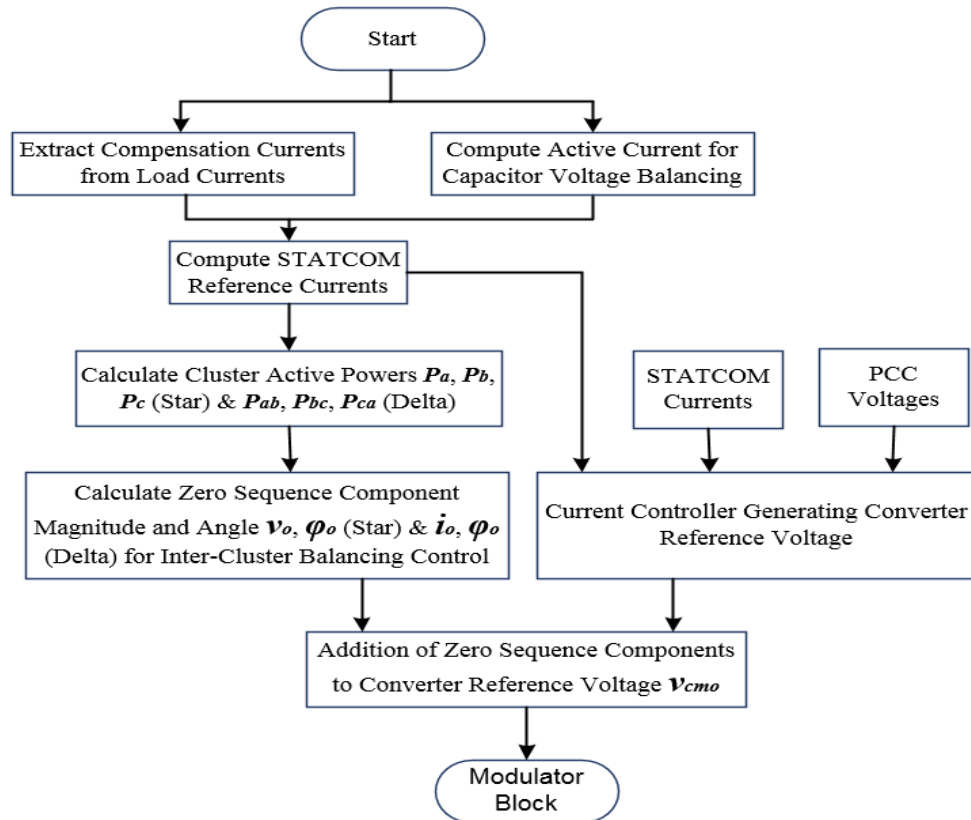


Figure 6.7: Flowchart of Single cell MMCC for unbalanced load compensation

### 6.3.2 Current Control using Dual vector predictive control

This is implemented using two predictive current controllers in positive and negative sequence synchronous reference frame as illustrated in Figure 6.8. PCC voltages and converter currents are transformed into positive and negative sequence components with the current controller tracking the converter reference currents generated from voltage control loops the outputs of the predictive current controller i.e. the reference output voltages are given below as:

$$\begin{bmatrix} v_{Cd}^+(k+1) \\ v_{Cq}^+(k+1) \end{bmatrix} = \begin{bmatrix} v_{PCCd}^+(k) \\ v_{PCCq}^+(k) \end{bmatrix} + \begin{bmatrix} (R_C - \frac{L_C}{T_S}) & \omega L_C \\ -\omega L_C & (R_C - \frac{L_C}{T_S}) \end{bmatrix} \begin{bmatrix} i_{Cd}^+(k) \\ i_{Cq}^+(k) \end{bmatrix} + \begin{bmatrix} \frac{L_C}{T_S} & 0 \\ 0 & \frac{L_C}{T_S} \end{bmatrix} \begin{bmatrix} i_{Cd}^{+*}(k) \\ i_{Cq}^{+*}(k) \end{bmatrix} \quad (6.21)$$

$$\begin{bmatrix} v_{Cd(k+1)}^- \\ v_{Cq(k+1)}^- \end{bmatrix} = \begin{bmatrix} v_{PCCd(k)}^- \\ v_{PCCq(k)}^- \end{bmatrix} + \begin{bmatrix} (R_c - \frac{L_c}{T_s}) & -\omega L_c \\ \omega L_c & (R_c - \frac{L_c}{T_s}) \end{bmatrix} \begin{bmatrix} i_{Cd(k)}^- \\ i_{Cq(k)}^- \end{bmatrix} + \begin{bmatrix} \frac{L_c}{T_s} & 0 \\ 0 & \frac{L_c}{T_s} \end{bmatrix} \begin{bmatrix} i_{Cd(k)}^{-*} \\ i_{Cq(k)}^{-*} \end{bmatrix} \quad (6.22)$$

where  $v_{Cdq}^+$ ,  $v_{Cdq}^-$  and  $v_{pccdq}^+$ ,  $v_{pccdq}^-$  are the converter reference and PCC positive and negative sequence voltage, while  $i_{Cdq}^+$ ,  $i_{Cdq}^-$  and  $i_{Cdq}^{*+}$ ,  $i_{Cdq}^{*-}$  are the positive and negative sequence converter and reference currents.  $R_f$  and  $L_f$  are the converter resistive and inductive filter parameters,  $\omega$  is the angular frequency of PCC voltage. For delta connection,  $R_f$  and  $L_f$  are replaced by  $R_f/3$  and  $L_f/3$  in (6.21) and (6.22) respectively. The reference  $dq$  voltages are transformed into three stationary reference frame which is fed into the modulation block (PS-PWM) to generate the converter switching pattern.

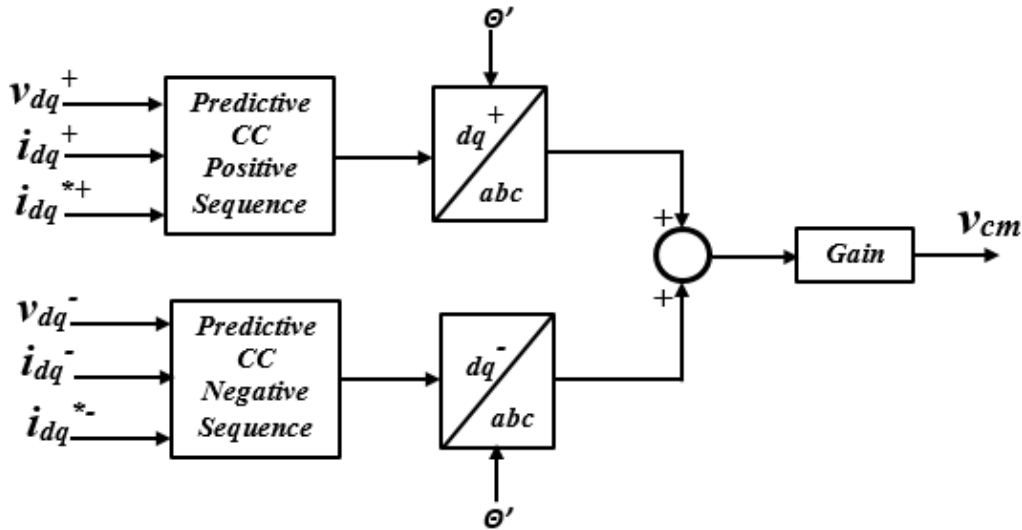


Figure 6.8: Predictive current control (CC) block. For star MMCC  $\theta' = \theta$  and  $Gain = 1$  while for delta MMCC  $\theta' = \theta + \pi/6$  and  $Gain = \sqrt{3}$ .

### 6.3.3 Evaluation of the zero sequence voltage and current to the degree of load unbalance

In this section, the zero sequence voltage and current applied in ensuring inter-cluster capacitor voltage balancing are analysed under different degree of load unbalance. This is to show how their magnitude and phase angles are influenced by the compensation current magnitude and phase angles to the grid voltage. In these analyses, the power losses in the converter will be neglected thus resulting in the positive sequence compensation current  $I_p$  phase angle relative to  $V_p$  being  $+\pi/2$  (i.e. capacitive operation). The magnitudes of the zero sequence components required to prevent cluster voltage unbalance vary not only with  $I_n$  magnitude change but also with its phase angle relative to  $V_p$ . The simplified expressions for zero sequence voltage magnitude and phase angle are given as:

$$V_o = \frac{V_p I_n}{I_p^2 - I_n^2} \sqrt{(I_p^2 + I_n^2 + 2I_p I_n \cos(\varphi_{ip} + 3\varphi_{in}))} \quad (6.23)$$

$$\varphi_o = \arctan \left( \frac{I_p \sin(\varphi_{ip} + \varphi_{in}) - I_n \sin 2\varphi_{in}}{I_p \cos(\varphi_{ip} + \varphi_{in}) + I_n \cos 2\varphi_{in}} \right) \quad (6.24)$$

From (6.23), it is seen that the magnitude of the zero sequence voltage depends on the magnitudes and phase angles of both positive and negative sequence currents to be compensated. Two examples are given below to verify this.

### Case 1

$I_p = 1pu$ ,  $I_n = 0.5pu$ , and both these currents are in phase hence i.e.  $\varphi_{ip} = \varphi_{in} = +\pi/2$ , and  $V_p = 1pu$ , thus:

$$V_o = \frac{0.5}{1 - 0.5^2} \sqrt{(1^2 + 0.5^2 + 1 \cos(2\pi))} = \frac{0.5}{0.75} \sqrt{2.25} = 1pu$$

$$\varphi_o = \arctan \left( \frac{\sin(\pi) - 0.5 \sin \pi}{\cos(\pi) + 0.5 \cos \pi} \right) = \arctan \left( \frac{0}{-1.5} \right) = 180^\circ$$

### Case 2

$I_p = 1pu$ ,  $I_n = 0.5pu$ , and the two currents are anti-phased to each other i.e.  $\varphi_{ip} = +\pi/2$ ,  $\varphi_{in} = -\pi/2$ , and  $V_p = 1pu$ . Then:

$$V_o = \frac{0.5}{1 - 0.5^2} \sqrt{(1^2 + 0.5^2 + \cos(-\pi))} = \frac{0.5}{0.75} \sqrt{0.25} = 0.33pu$$

$$\varphi_o = \arctan \left( \frac{\sin(0) - 0.5 \sin(-\pi)}{\cos(0) + 0.5 \cos(-\pi)} \right) = \arctan \left( \frac{0}{0.5} \right) = 0^\circ$$

These examples show that with the same magnitudes for  $I_p$  and  $I_n$  if there phase angles are different the resultant  $V_o$  magnitudes are different. The 3-D plot in Figure 6.9 shows the variation of  $V_o$  with respect to both  $\varphi_{in}$  and the degree of unbalance defined as  $K_{ir} = I_n/I_p$  which further validates the above analysis. The plot shows that the maximum  $V_o$  value not only occurs at  $\varphi_{in} = \pi/2$  but also at  $\varphi_{in} = -\pi/6$  and  $-2\pi/3$ , likewise the minimum occurs at  $\varphi_{in} = -\pi/2$ ,  $\pi/6$  and  $2\pi/3$ .

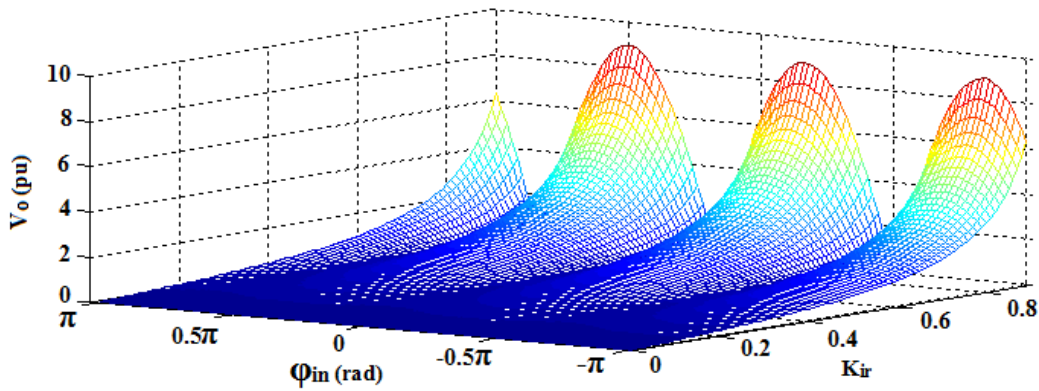


Figure 6.9: Relationship between the zero sequence voltage magnitude  $V_o$ , degree of unbalance  $K_{ir}=I_n/I_p$ , and the phase angle of the negative sequence current  $\varphi_{in}$  at the maximum PCC voltage 230V.

For SDBC, the zero sequence current magnitude and angle can be simplified as:

$$I_o = \frac{I_n}{\sqrt{3}} \quad (6.25)$$

$$\begin{aligned} \varphi_o &= \arctan(-\cot \varphi_{in}) \\ &= 90^\circ + \varphi_{in} \end{aligned} \quad (6.26)$$

Thus above shows that the magnitude of the zero sequence current  $I_o$  is proportional to  $I_n$  and independent of its relative phase (see Figure 6.10). The whole derivations are given in appendix D4.

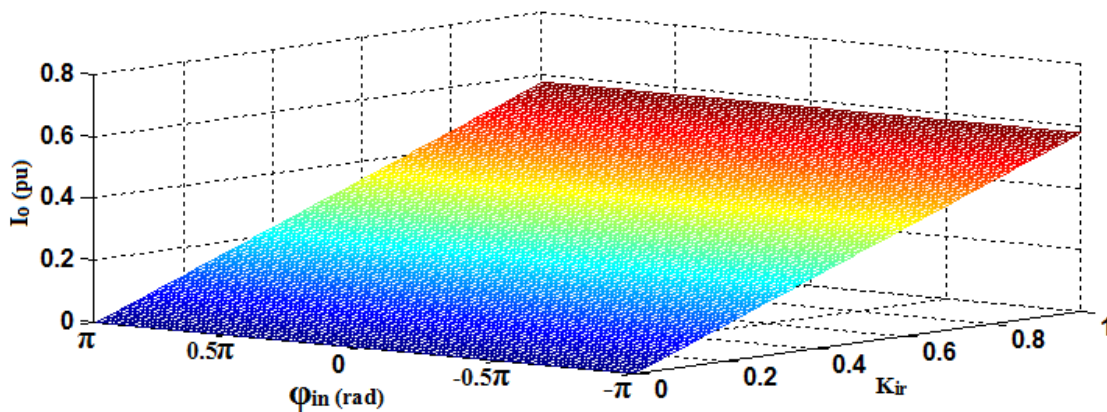


Figure 6.10: Relationship between the zero sequence current  $I_o$ , degree of unbalance  $K_{ir}=I_n/I_p$ , and the phase angle of the negative sequence current  $\varphi_{in}$  at maximum cluster current  $(2/\sqrt{3})$  A.

## 6.4 Derivation of Required Third Harmonic Component

As has been analysed and shown in Figures 6.9 and 6.10, when compensating unbalanced load current the operating range of SSBC is limited in comparison to that of SDBC. With the increase of  $K_{ir}$ , zero sequence voltage can grow excessively high, pushing one of the phase cluster voltages well above its rated level. This, in turn, leads to its DC-link voltage collapsing, making the converter not able to operate. One way to extend the SSBC's operating range is to inject zero sequence voltage plus its third harmonic, thus reducing the peak value of injected voltage.

To find the third harmonic component in SSBC MMCC case, we take the zero sequence voltage magnitude and angle, evaluated by (6.18), as the fundamental element and add its third harmonic component and the third harmonic of the PCC voltage, so the new injection term for balancing inter cluster voltage is expressed as:

$$\begin{aligned} v_o &= V_o \sin(\omega t + \varphi_o) \\ v_{o3} &= V_o (\sin(\omega t + \varphi_o) + \frac{1}{6} \sin(3\omega t + 3\varphi_o)) + \frac{V_p}{6} \sin(3\omega t + 3\varphi_{VP}) \end{aligned} \quad (6.27)$$

Likewise for SDBC MMCC the injection current term is given as:

$$\begin{aligned} i_o &= I_o \sin(\omega t + \varphi_o) \\ i_{o3} &= I_o (\sin(\omega t + \varphi_o) + \frac{1}{6} \sin(3\omega t + 3\varphi_o)) \end{aligned} \quad (6.28)$$

Waveforms of the converter phase cluster reference quantities (i.e. voltage for SSBC and current for SDBC respectively) with zero sequence components injection only and zero sequence plus third harmonics are shown in Figure 6.11. For SSBC the phase voltages shown in Figure 6.11 (a) and (b) are obtained when the ratio of negative to positive sequence currents, defined as  $K_{ir} = I_n/I_p$ , is set to 0.3 and they are in phase. It can be seen clearly that the magnitudes of the three phase cluster voltages are different. Comparing both injection techniques the maximum phase voltage corresponding to the third harmonic injection is 1.2 pu, while the zero sequence injection is 1.3 pu which is about 10% higher. In the SDBC case, the current waveforms are derived with  $K_{ir} = 0.55$ . The maximum phase current magnitude for the combined zero sequence current and its third harmonic is only 88% of that when only zero sequence current is injected.

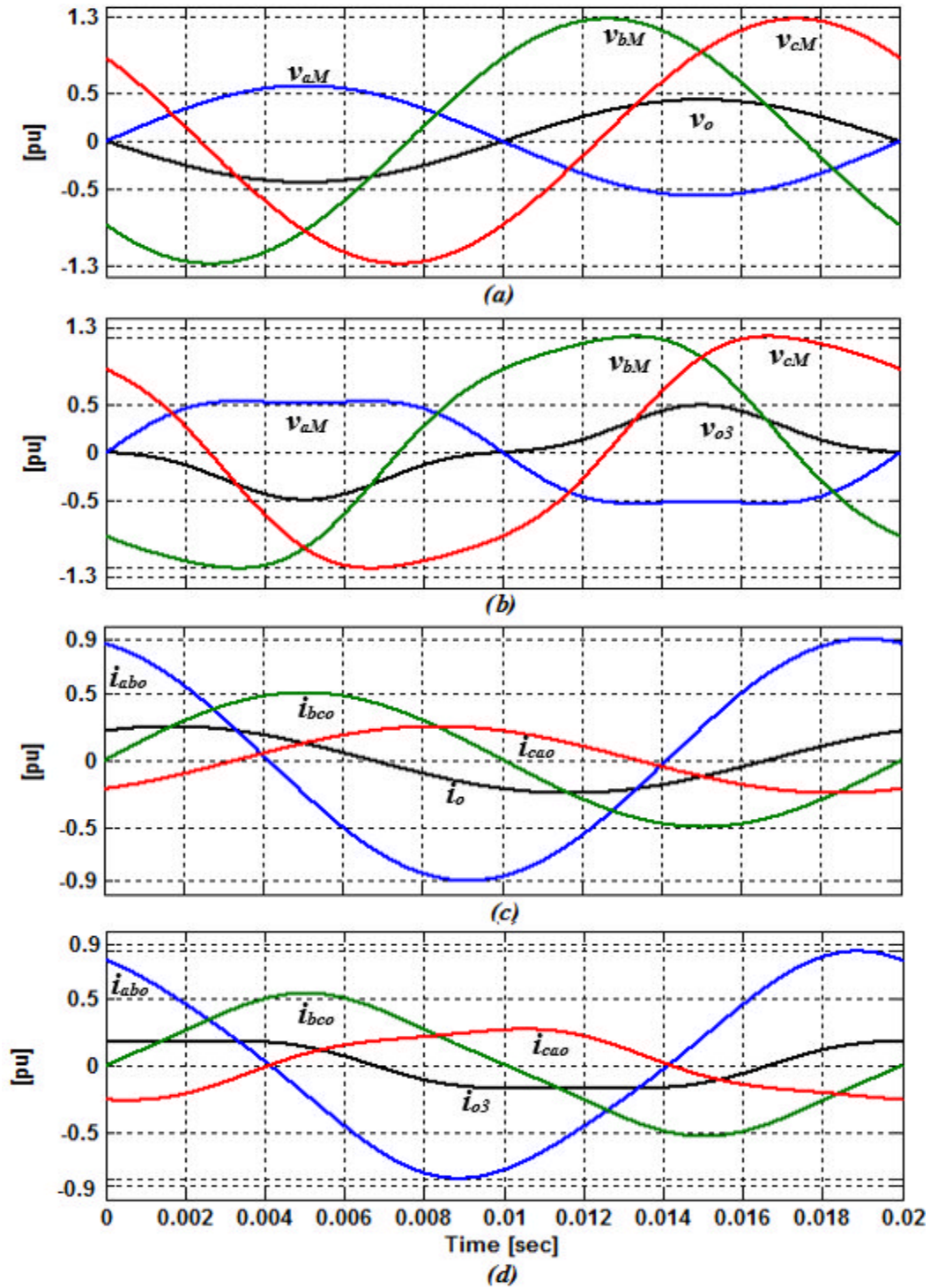


Figure 6.11: SSBC and SDBC converter cluster voltage and current reference waveforms (a) injecting zero sequence voltage, (b) zero sequence voltage + its third harmonic for  $I_n/I_p = 0.3pu$ , (c) injecting zero sequence current and (d) zero sequence current + its third harmonic injection with  $I_n/I_p = 0.55pu$ .

## 6.5 Operating Range Extensions and Ratings of MMCC under Various Unbalanced Load conditions

The operating ranges and ratings of both SSBC and SDBC-MMCC are analysed under load unbalanced conditions. This analysis is based on the zero sequence component method of inter cluster balancing control. Under this condition, the influence of the zero sequence components on the operating capabilities and rating of the MMCC are analysed. The degree of load current imbalance  $K_{ir}$  is used in this investigation.

### 6.5.1 SSBC MMCC

The differences between the magnitudes of injected voltage when using zero sequence voltage  $v_o$  and the third harmonic injection method as discussed in section 6.4, are shown in Figure 6.12 for  $K_{ir}$  varying from 0 to 0.9 with phase angle  $\varphi_m = \varphi_{ip}$  (worst condition). It can be seen that in the range  $0 \leq K_{ir} \leq 0.5$ , the magnitudes when using  $v_{o3}$  which includes PCC voltage third harmonic components are always higher than that of using  $v_o$  only while the reverse is the case in the range  $0.5 \leq K_{ir} \leq 0.9$ . It is seen in Figure 6.12 that at  $K_{ir} = 0.5$ , the magnitude of  $v_o$  and  $v_{o3}$  are equal because the two third harmonic components of  $v_{o3}$  are equal and opposite, thereby cancelling out each other (see the analysis in 6.3.3).

In determining the phase cluster dc-capacitor voltage required by the SSBC-MMCC for load unbalance compensation, the voltages of each phase are dependent on their cluster individual module dc-link voltages  $V_{dc}$ , and their total value  $\Sigma V_{dc} = n_{mp} \cdot V_{dc}$ , where  $n_{mp}$  is the number of modules per phase. The three phase voltages may be different and the peak values of the maximum phase voltages can be defined as:

$$V_{dc\_rated} = \text{Max} (|V_{mM}|) \leq n_{mp} V_{dc} \quad (6.29),$$

where the converter output voltage is given as:

$$v_{mM} = v_m + v_o + \underbrace{L \frac{di_m}{dt} + Ri_m}_{v_f} = V_{mM} \sin(\omega t + \phi_m) \quad (6.30)$$

and  $V_f$  defines the voltage drop across the MMCC filter;  $m = a, b, c$ .

Figure 6.13 shows a logarithmic plot of the  $V_{dc\_rated}$  varying according to  $K_{ir}$ , when injecting both zero sequence voltage fundamental plus the third harmonic component. It is seen that by injecting  $v_{o3}$  for inter cluster voltage balancing, the maximum cluster dc-link voltage,  $V_{dc\_rated}$ , is clearly lower than when injecting only  $v_o$  for  $0 \leq K_{ir} \leq 0.45$  and  $0.55 \leq K_{ir} \leq 0.9$ . Within the range  $0.45 \leq K_{ir} \leq 0.55$  a dead zone exists, meaning that the  $V_{dc\_rated}$  values of both  $v_o$  and  $v_{o3}$  injection techniques are almost equal. This results from the fact that within  $0.45 \leq K_{ir} \leq 0.55$  both  $v_o$  and  $v_{o3}$  are almost equal as illustrated in Figure 6.13. Since it is practically not feasible to rate an MMCC-SSBC STATCOM more than twice its nominal PCC voltage, the  $v_{o3}$  techniques provide better and reduced  $V_{dc\_rated}$  voltage utilization compared to the  $v_o$  counterpart. For example, for  $K_{ir}=0.2$ , the normalized peak  $V_{dc\_rated} / V_p$  under  $v_o$  injection is about 1.18pu whereas for  $v_{o3}$  it is only 1.07pu. This implies that for an 11 kV distribution system compensating  $K_{ir}=0.2$  of load unbalance where each converter module is rated 400V, 33 and 30 modules will be required for both  $v_o$  and  $v_{o3}$  injection techniques respectively. It is therefore seen that the use of the zero sequence voltage fundamental plus its third harmonic components reduces the number of sub-modules required per phase for the SSBC-STATCOM. It is important to note that this dead zone phenomenon only occurs for the worst case condition ( $\varphi_{in} = \varphi_{ip}$ ).

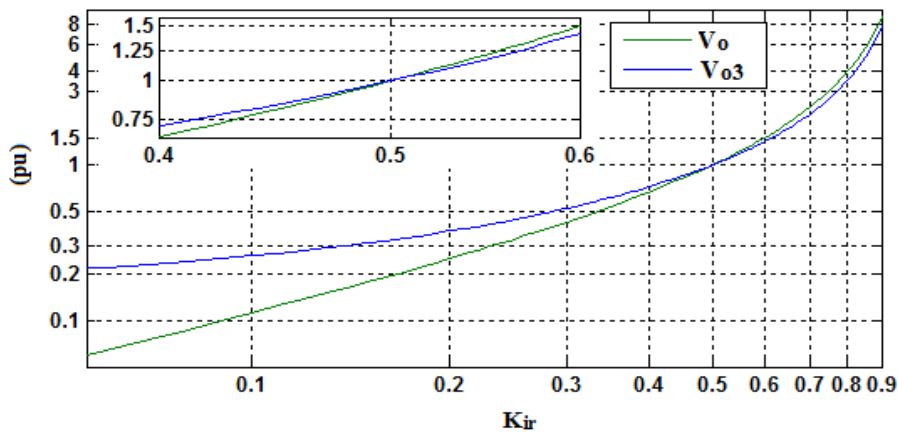


Figure 6.12: Comparison between sinusoidal and third harmonic zero sequence injection with respect to  $K_{ir}$ .



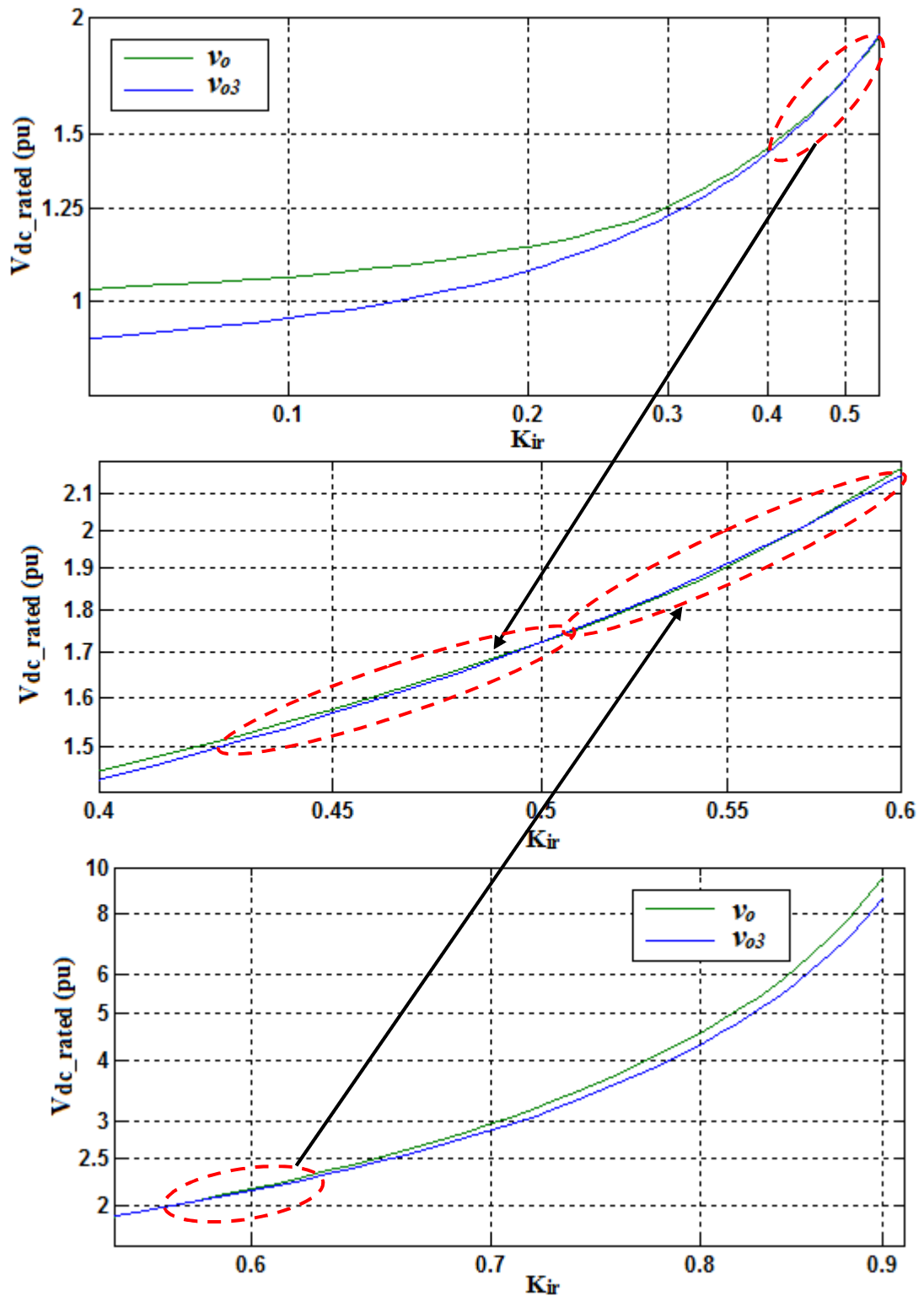


Figure 6.13: Comparison between sinusoidal and third harmonic zero sequence injection with respect to estimated DC-link cluster voltage.

### 6.5.2 SDBC MMCC

Comparing the current magnitudes of injecting  $i_0$  and  $i_{03}$  as a function of  $K_{ir}$ , the one under  $i_{03}$  is lower than that when injecting its fundamental frequency counterpart as  $K_{ir}$  varies from 0 to 1 as seen in Figure 6.14.

The phase cluster currents in the SDBC are expressed as;

$$i_m = i_{mp} + i_{mn} + i_o \text{ where } m = ab, bc, ca \quad (6.31)$$

The current rating  $I_{rated}$  of the SDBC is determined by the maximum phase current given as;

$$I_{rated} = \text{Max}(|I_m|) \quad (6.32)$$

The maximum phase current of the SDBC only occurs when the zero sequence current is in phase with any of the phase cluster currents. Based on equation (6.32), this occurs at  $\varphi_{in} = -\pi/3, -\pi$  and  $\pi/3$ .

Figure 6.15, shows the relationship between the maximum cluster current and the degree of unbalance  $K_{ir}$  for both the  $i_o$  and  $i_{o3}$  injections at  $\varphi_{in} = -\pi/3$ . It is seen that by injecting  $i_{o3}$  for inter cluster voltage balancing, the required cluster current rating,  $I_{rated}$ , is lower than when injecting just a fundamental component of the zero sequence current ( $i_o$ ). For example when  $K_{ir} = 1$  the rated cluster current required for both  $i_o$  and  $i_{o3}$  injection techniques are 1.39 pu and 1.29 pu respectively.

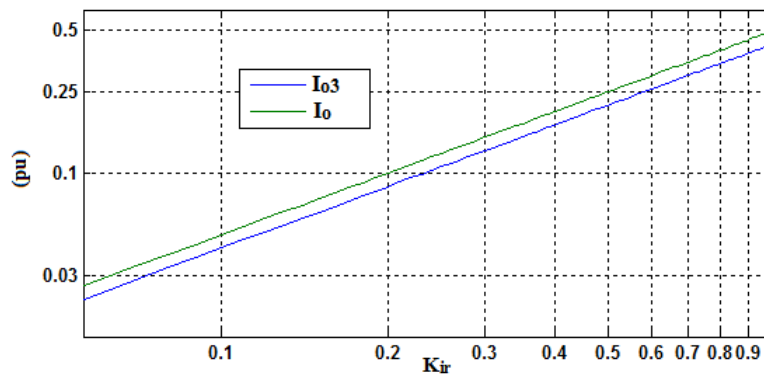


Figure 6.14: Comparison between sinusoidal and third harmonic zero sequence injection with respect to  $K_{ir}$ .

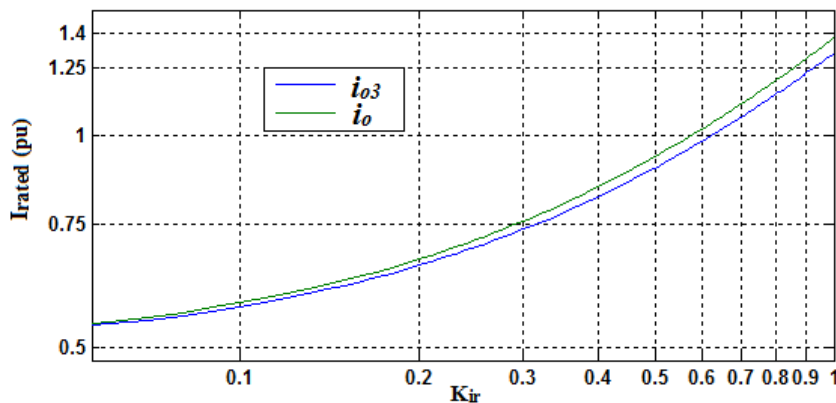


Figure 6.15: Comparison between sinusoidal and third harmonic zero sequence injection with respect to estimated cluster current.

Figure 6.16 contrasts the increases of  $v_o$  and  $i_o$  as  $K_{ir}$  raises from 0 to 0.9. Note that the vertical axes on the right and left-hand sides represent the magnitudes of  $i_o$  and  $v_o$ . At the level of unbalance when  $K_{ir}=0.9$ , one can see that  $i_o$  is only  $0.5 \text{ pu}$ , hence 50% of the phase nominal value, however,  $v_o$  is  $9 \text{ pu}$ , 9 times of the nominal voltage value. From this plot, it is clear that the required magnitude of zero sequence current for balancing the inter-cluster capacitor voltage of the SDBC is far lower than the zero sequence voltage required for SSBC.

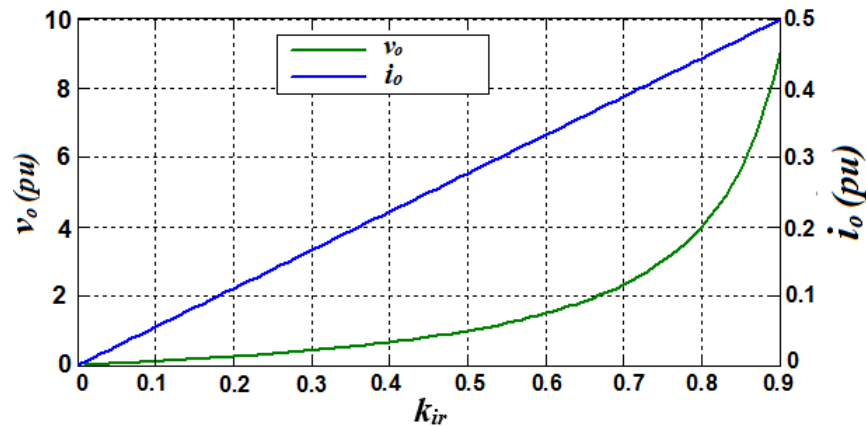


Figure 6.16: Comparison between Zero sequence current and voltage for the same  $K_{ir}=I_n/I_p$  condition at their maximum limits.

## 6.6 Simulation Results and Discussion

The theoretical analysis presented in the earlier sections has been verified via simulation tests for both star and delta configured MMCC using both fundamental and third harmonic injection of zero sequence components. The parameters of the MMCC circuits and control gains are listed in Table 6.1 and 6.2 respectively.

For these tests, the load was set to have a degree of unbalance,  $K_{ir}=0.7$ , Figures 6.17 and 6.18 show the results obtained for SSBC-MMCC, whilst Figures 6.19 and 6.20 are for SDBC-MMCC. Each figure displays ten variables at different nodes of the system, these are (a) degree of load unbalance  $K_{ir}$  variation, (b) and (c) are the supply voltages and currents, (d) converter phase reference voltages, (e) converter phase voltages, (f) converter cluster currents, (g) inter-cluster sub-module capacitor voltages, (h) sub-module capacitor voltages, (i) sub-module inner flying capacitor voltages, (j) zero sequence components either voltage (star) or current (delta).

Table 6.1: MMCC power system parameters

Configuration	SSBC	SDBC
PCC Side	1.8 kVA (60V, 10A)	
Distribution Line	Aluminium PI TX line (d= 10mm, s= 1m, l=1.1 km) L =2mH, R = 0.4 $\Omega$ , X= 0.6283 $\Omega$ , Short circuit current = 137 A	
Load Side	1.8 kVA (60V, 10A) Load A: 22 $\Omega$ , 42mH Load B: 20.5 $\Omega$ , 42mH Load C: 10 $\Omega$ , 1.64mH	
Converter Side	1.5 kVA (100V, 5A) Filter:10 $\Omega$ , 10mH DC Capacitor rating (per sub-module): 400 V, 1.12 mF (utilized at 50 V) Module Flying Capacitor: 400V, 0.56mF (utilized at 25 V)	1.26 kVA (140V, 3A) Filter: 10 $\Omega$ ,10mH DC Capacitor rating (per sub-module): 400 V, 1.12 mF (utilized at 70 V) Module Flying Capacitor: 400V, 0.56mF (utilized at 35 V)

Table 6.2: Control gain parameters

Gain parameters	SSBC	SDBC
Overall dc capacitor proportional gain $K_{p-dc}$	0.1	0.1
Overall dc capacitor integral gain $K_{i-dc}$	20	10
Cluster dc capacitor proportional gain $K_{p-c}$	0.1	0.01
Cluster dc capacitor integral gain $K_{i-c}$	30	30
Circulating current proportional gain $K_{pio}$	-	30

Figure 6.17 shows the waveforms for SSBC-based STATCOM using sinusoidal zero sequence voltage injection. Figure 6.18 gives the corresponding waveforms under the same operating conditions but using third harmonic zero sequence voltage  $v_{o3}$  for inter-cluster dc-voltage balancing.

As seen from both figures, during the time interval  $0 < t < 0.1s$ , the STATCOM operates under unbalanced load conditions but only reactive power compensation is carried out. From  $t=0.1s$ , the STATCOM controller compensates load unbalance by increasing  $K_{ir}$  in steps of 0.21, 0.105, 0.075

and 0.05 in Figure 6.17(a) and in steps of 0.21, 0.14, 0.09 and 0.05 in Figure 6.18(a).

It can be seen clearly that when using sinusoidal zero sequence voltage injection, adequate compensation of negative sequence current is achieved for  $K_{ir}$  up to 0.6 ( $0.1s < t < 0.5s$ ) and sub-module dc capacitor voltages are operating within their nominal rating (see Figure 6.17(g)-(h)). However, further increasing the degree of unbalance, when  $K_{ir}=0.65$  ( $0.5s < t < 0.6s$ ), phase C converter voltage exceeds its nominal value as seen in Figure 6.17(d)-(e) due to high zero sequence voltage (reaching 60 V) (see Figure 6.17(j)). The dc-link voltage become uncontrollable see Figure 6.17(h)-(i) which result in distorted currents injected in the grid as seen in Figure 6.17(c), (f).

In contrast, the operating range can be observed when third harmonic zero sequence voltage injection is used as shown in Figure 6.18. Within the time interval  $0.4s < t < 0.5s$  at  $K_{ir}=0.65$ , the converter phase C voltage is still within the rated limit (see Figure 6.18(d)-(e)) and the inter-cluster and sub-module capacitor dc voltages are still been maintained balanced. Thus, it is clear that using the third harmonic voltage injection for inter-cluster dc-link voltage balance in contrast with the fundamental zero sequence voltage, the magnitude of the third harmonic injected zero sequence voltage is lesser than the other for the same  $K_{ir}$  value. Thus, the working range of the SSBC-MMCC is extended compared to that when only zero sequence voltage is used.

The operating behaviour of SDBC STATCOM under unbalanced load compensation is seen in Figures 6.19 and 6.20. Comparing with SSBC STATCOM, the SDBC offers much higher capability. The superiority of the SDBC over SSBC is mostly evident at a high degree of load unbalance, at  $K_{ir}=0.7$ , the SDBC compensates the unbalanced current completely as seen in Figures 6.19(c) and 6.20(c). The inter-cluster and sub-module dc capacitor voltages are maintained within  $\pm 10\%$  of their nominal rated values (see Figures 6.19(g)-(h) and Figures 6.20(g)-(h)). Comparing the results of using third order harmonic with the fundamental zero sequence current injections, the magnitude of the zero sequence current with third harmonics at  $K_{ir}=0.7$  is 0.1A lower than to that of fundamental zero sequence current which is 0.6A ( see Figure 6.19(j) and Figure 6.20(j)).

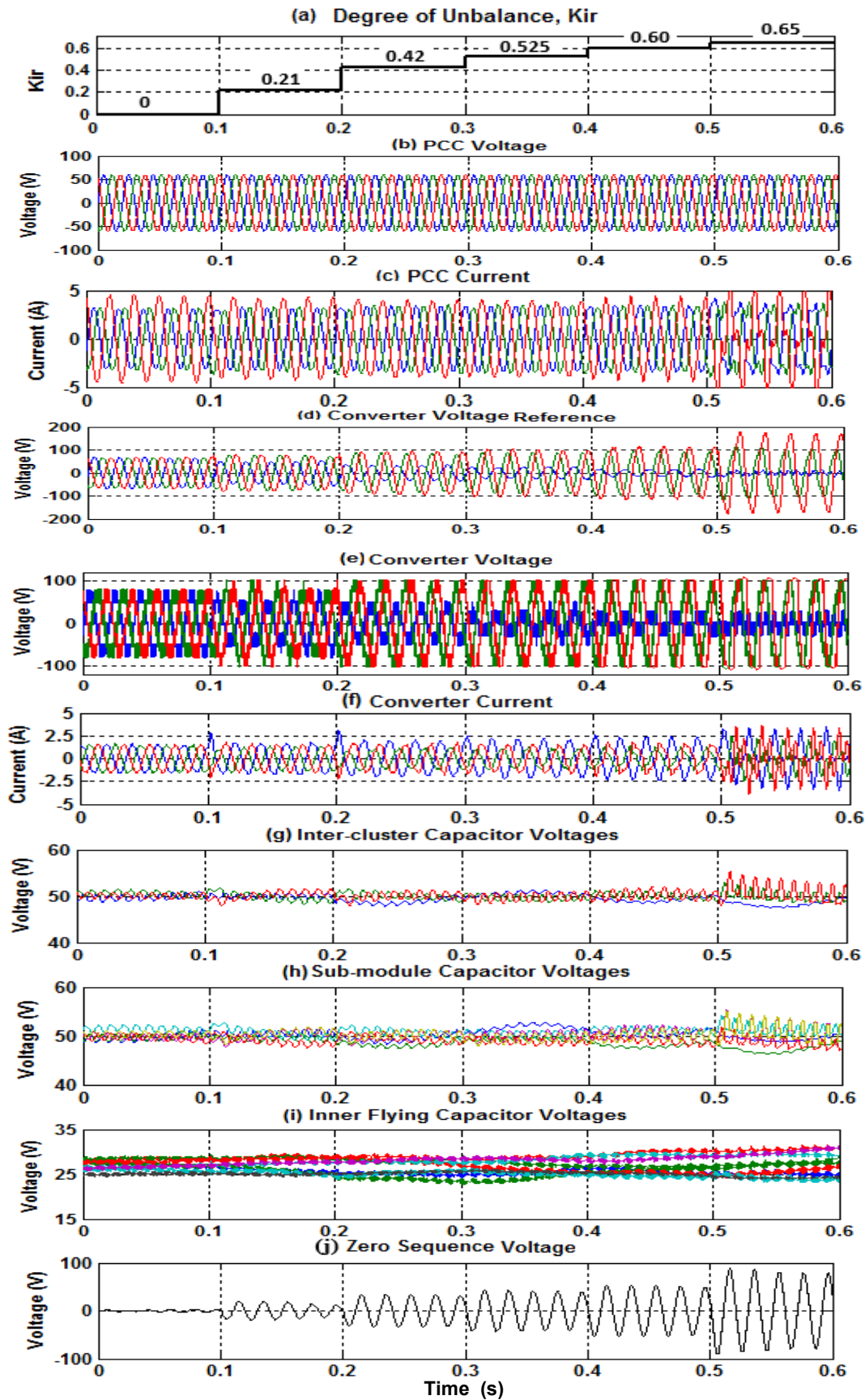


Figure 6.17: Operating behaviour of SSBC under unbalance load using sinusoidal zero sequence voltage injection.

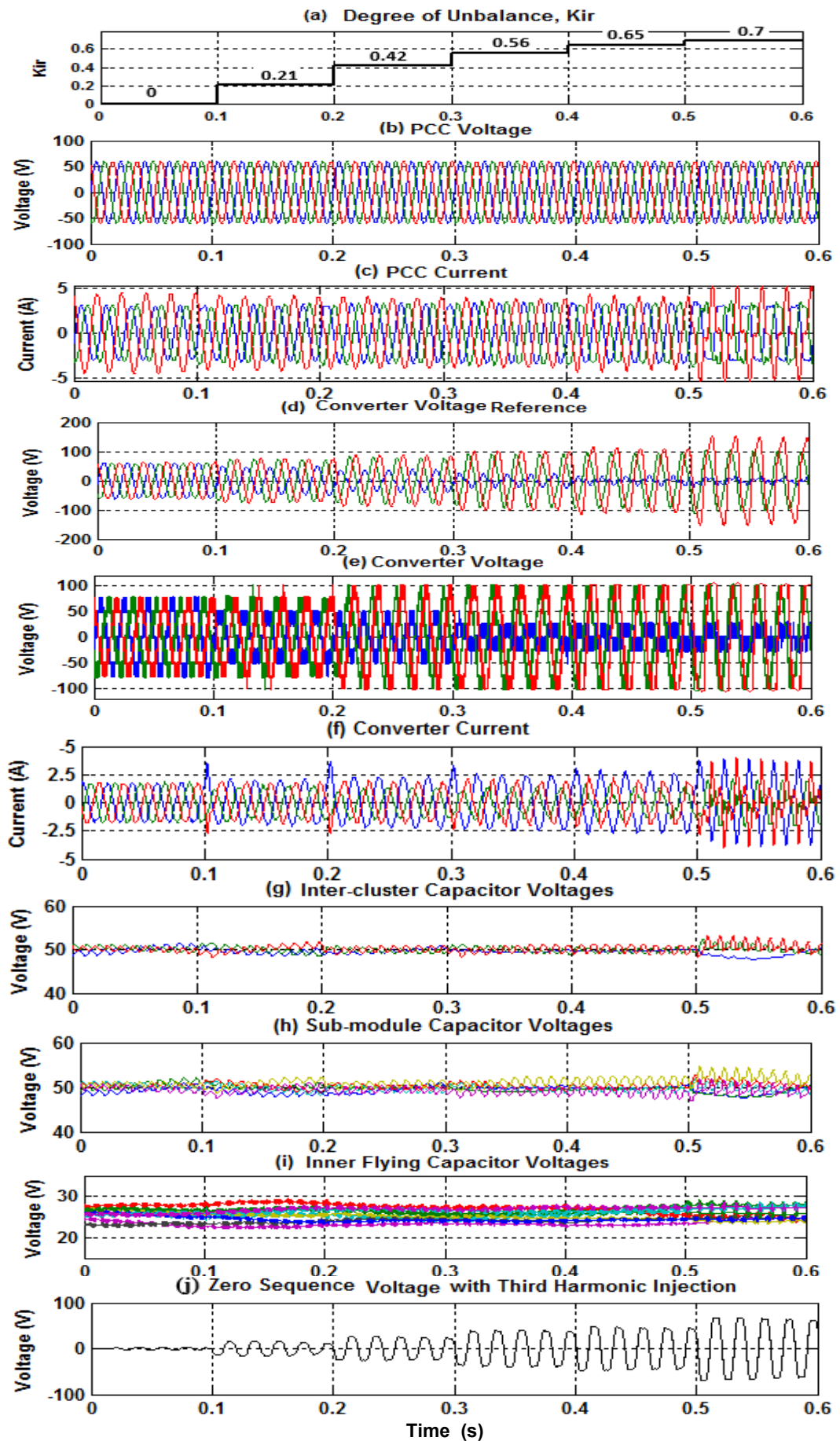


Figure 6.18: Operating behaviour of SSBC under unbalance load compensation using third harmonic zero sequence voltage injection.

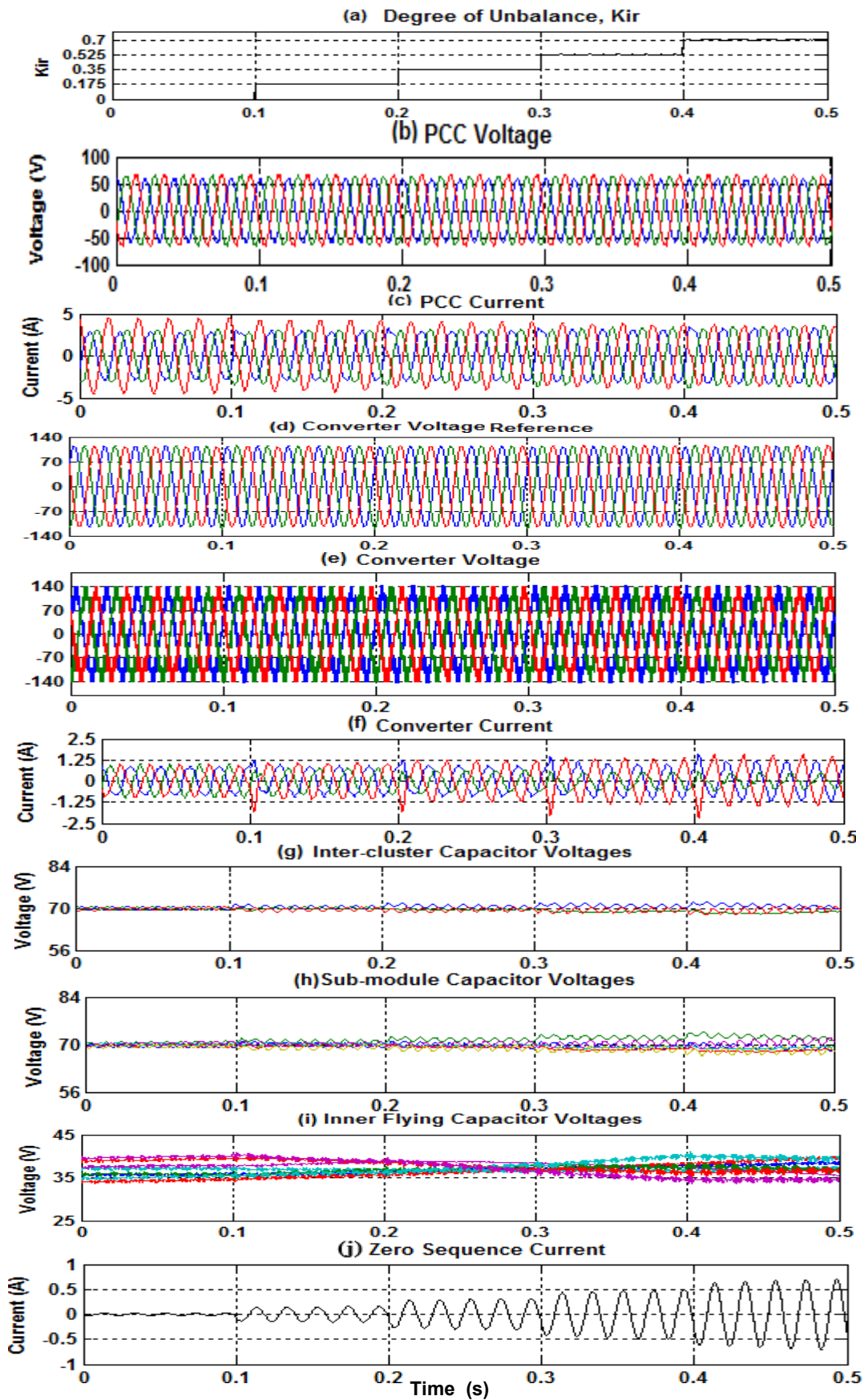


Figure 6.19: Operating behaviour of SDBC under unbalance load using sinusoidal zero sequence current injection.



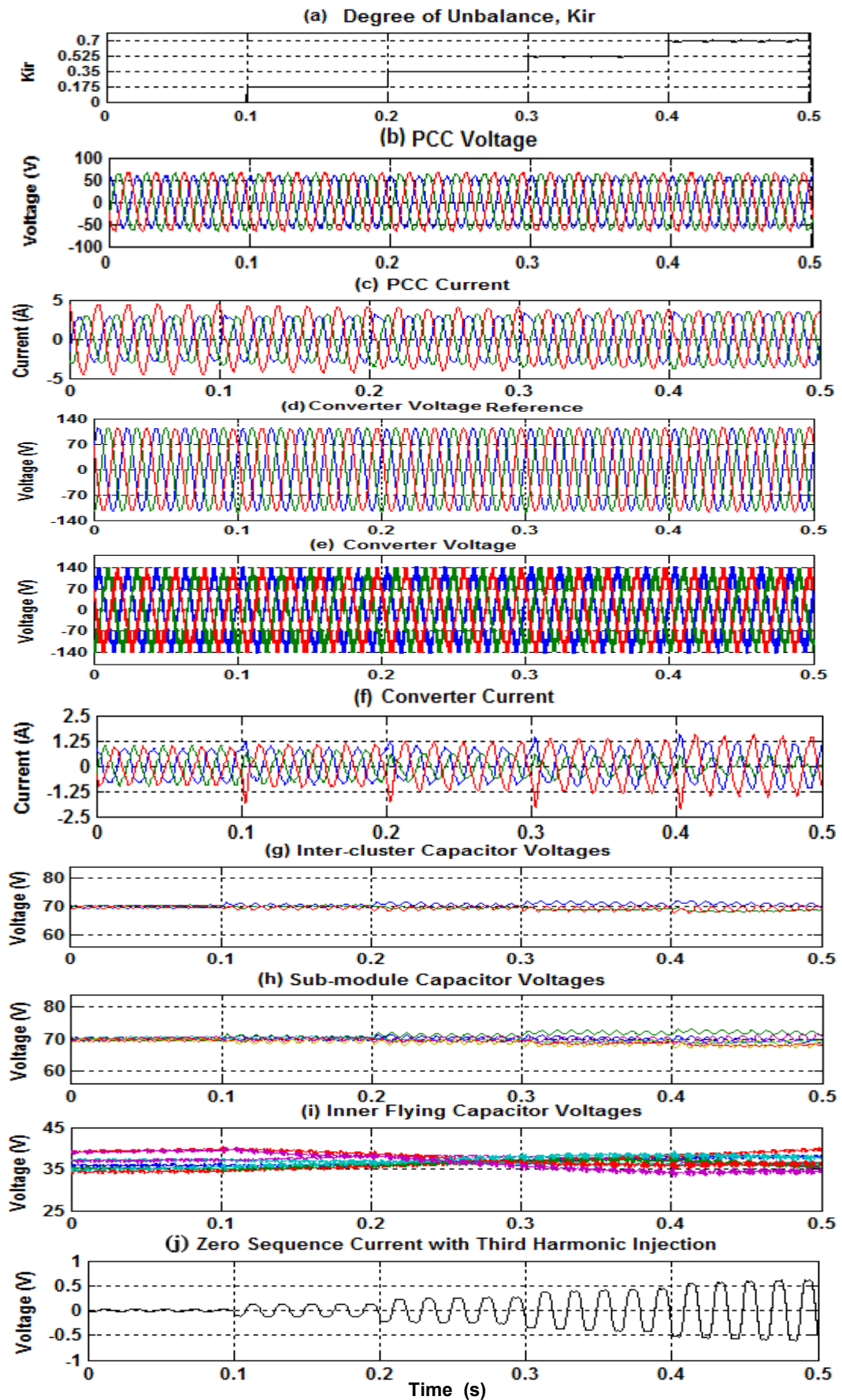


Figure 6.20: Operating behaviour of SDBC under unbalance load compensation using third harmonic zero sequence current injection.

## 6.7 Experimental Validations

### 6.7.1 Experimental set-up

The power system for testing the STATCOM capability in compensating reactive power and negative sequence current at a single feeder bus point of a distribution system is shown in Figure 6.21. Only the star configured MMCC is shown since both configurations have been schematically shown in Figure 6.1. This is further divided into three parts namely the PCC side, load side and converter side; these are discussed below.

- The PCC side comprises of the 415V 3-phase power supply connected via an auto transformer which is set to 60V and transmission line impedance.
- The load side is modelled to represent an unbalance load which consumes reactive power and introduces current imbalance at the point of common coupling. This consists of rheostats and inductors modelled across each phase. The load impedance across each phase is shown in Table 6.3.
- The converter side consists of the built prototype 9-level MMCC consisting of two cascaded 5-level FC sub-modules which are connected to the PCC through and R-L filter. The converter is configured in both star and delta configurations for this research.

Table 6.3: Power system Characteristics

Configuration	SSBC	SDBC
PCC Side	1.8 kVA (60V, 10A)	
Distribution Line	Aluminium PI TX line (d= 10mm, s= 1m, l=1.1 km) L =2mH, R = 0.4 $\Omega$ , X= 0.6283 $\Omega$ , Short circuit current = 137 A	
Load Side	1.8 kVA (60V, 10A), Load A: 22 $\Omega$ , 42mH Load B: 20.5 $\Omega$ , 42mH, Load C: 10 $\Omega$ , 1.64mH	
Converter Side	1.5 kVA (100V, 5A) Filter: 10 $\Omega$ , 10mH DC Capacitor rating (per sub-module): (utilized at 50 V) Module Flying Capacitor: (utilized at 25 V)	1.26 kVA (140V, 3A) Filter: 10 $\Omega$ , 10mH DC Capacitor rating (per sub-module): (utilized at 70 V) Module Flying (utilized at 35 V)

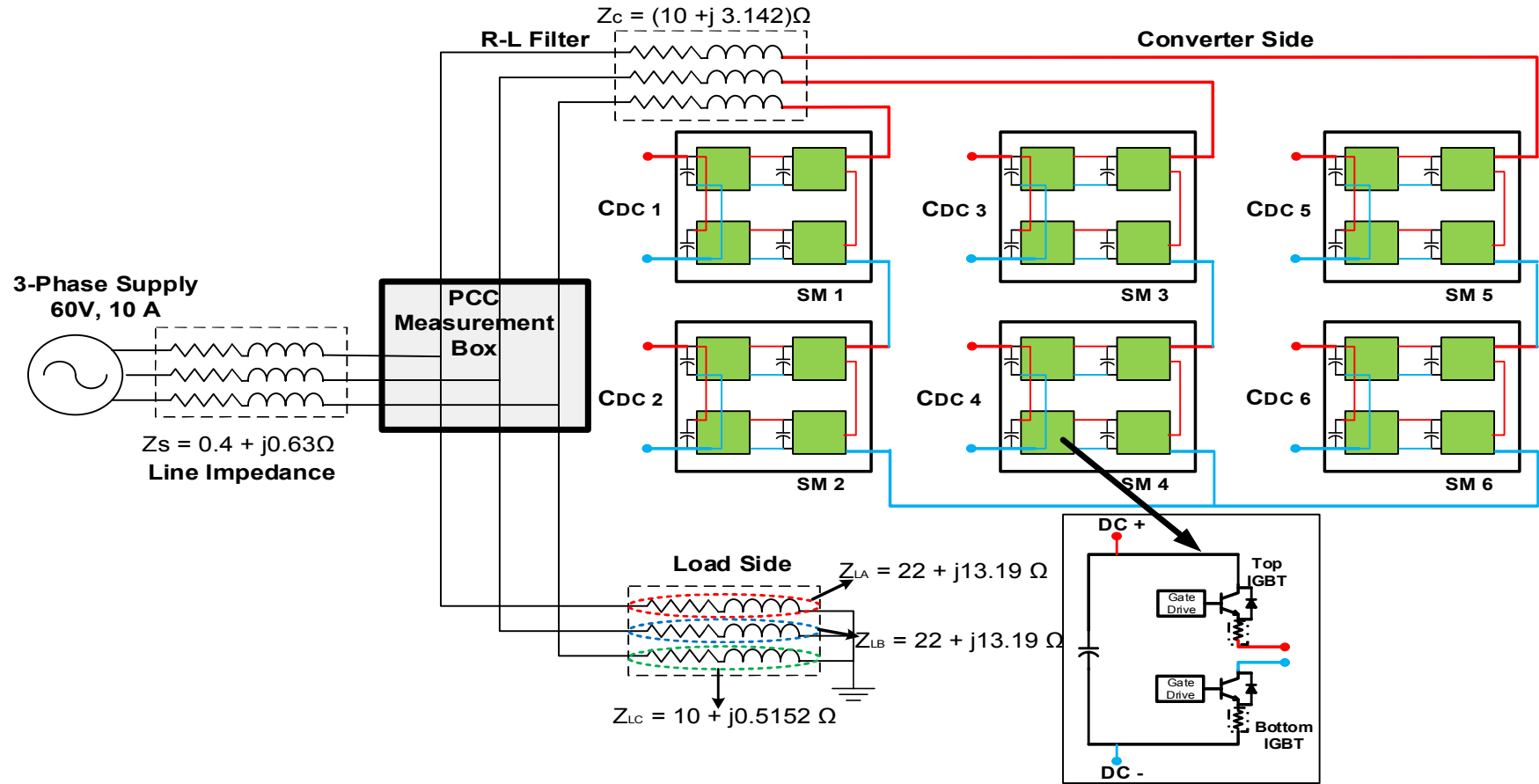


Figure 6.21: Experimental power system configuration for MMCC in star configuration.

### 6.7.2 Results and Discussion

The simulation results presented in the previous section been validated experimentally for both star and delta configured MMCCs using both fundamental and third harmonic injection of zero sequence components under similar test conditions as the simulation tests. The controller parameters are listed in Table 6.4.

Table 6.4: Control gain parameters

Gain parameters	SSBC	SDBC
Overall dc capacitor proportional gain $K_{p-dc}$	0.1	0.1
Overall dc capacitor integral gain $K_{i-dc}$	20	10
Cluster dc capacitor proportional gain $K_{p-c}$	0.1	0.01
Cluster dc capacitor integral gain $K_{i-c}$	30	30
Circulating current proportional gain $K_{pio}$	-	30

For these tests, the load was set to have a degree of load unbalance,  $K_{ir}=0.7$ , Figures 6.22 and 6.23 show the results obtained for the SSBC-MMCC, whilst Figures 6.24 and 6.25 are for the SDBC-MMCC.

Figure 6.22 shows the waveforms obtained for SSBC-based STATCOM with a sinusoidal zero sequence voltage injection. Figure 6.23 gives the corresponding waveforms under the same operating conditions but using third harmonic zero sequence voltage  $v_{o3}$  for inter-cluster dc-voltage balancing.

As can be seen from both figures, during the time interval  $0 < t < 0.1s$ , the STATCOM operates under unbalanced load conditions but only compensating reactive power. From  $t=0.1s$ , the STATCOM controller compensates load unbalance by increasing  $K_{ir}$  in steps of 0.21, 0.105, 0.075 and 0.05 in Figure 6.22(a) and in steps of 0.21, 0.14, 0.09 and 0.05 in Figure 6.23(a).

It can be seen clearly that when using sinusoidal zero sequence voltage injection, adequate compensation of negative sequence current is achieved for  $K_{ir}$  up to 0.6 ( $0.1s < t < 0.5s$ ) and sub-module dc capacitor voltages are operating within their nominal rating (see Figure 6.22 (g)-(h)). However, further increasing the degree of current unbalance, when  $K_{ir}=0.65$  ( $0.5s < t < 0.6s$ ), phase C converter voltage exceeds its nominal value as seen in Figure 6.22 (d)-(e) due to high zero sequence voltage (reaching 60V) (see Figure 6.22 (j)). The dc-link voltage becomes uncontrollable (see Figure 6.22 (h)-(i)) which

result in distorted currents being injected into the grid as seen in Figures 6.22 (c), (f).

In contrast, the converter operating range, when the third harmonic zero sequence voltage injection is used, can be observed as shown in Figure 6.23. Within the time interval  $0.4s < t < 0.5s$  at  $K_{ir}=0.65$ , the converter phase C voltage is still within the rated limit (see Figures 6.23 (d)-(e)) and the inter-cluster and sub-module capacitor dc voltages are still been maintained balanced. Thus, it is clear that when using the third harmonic voltage injection for inter-cluster dc-link voltage balance, the magnitude of the injected voltage is lower than the fundamental zero sequence voltage for the same  $K_{ir}$  value. Thus, the operating range of the SSBC-MMCC is extended.

The operating behaviour of the SDBC STATCOM under unbalanced load compensation has also been tested and results can be seen in Figures 6.24 and 6.25. In comparison with SSBC STATCOM, the SDBC offers much better capability. The superiority of the SDBC over SSBC is most evident at a higher degree of load unbalance, at  $K_{ir}=0.7$ , the SDBC compensates the unbalanced current completely as seen in Figures 6.24 (c) and 6.25 (c). The inter-cluster and sub-module dc capacitor voltages are maintained within  $\pm 10\%$  of their nominal rated values (see Figure 6.26 (g)-(h) and Figure 6.25 (g)-(h)). In contrast using the third order harmonic with the fundamental zero sequence current injection, the magnitude of the injected current at  $K_{ir}=0.7$  is 0.1A lower compared to its fundamental zero sequence counterpart which is 0.6A (see Figure 6.24 (j) and Figure 6.25 (j)). The inner flying capacitors of the delta configured MMCC are seen to be balanced within  $\pm 10\%$  of their nominal rated values (see Figure 6.26 (a)-(c)) for  $K_{ir}=0.7$ . Figure 6.26 (d) shows converter terminal voltage using PS-PWM scheme which has 9 distinctive levels.

Though the carrier frequency per module is 750 Hz, the PS-PWM results in the harmonics in the MMCC phase voltage waveform being eight times of the carrier frequency and its sidebands, hence the most significant harmonic frequency is  $750 \times 8 = 6000\text{Hz}$  and those of its sidebands. Two plots showing the converter voltage waveform and its harmonic spectra with THD of 10.39% are presented in Figure 6.26 (e). The converter phase voltage spectra diagram shows clearly the harmonic frequencies at the specified frequency values.

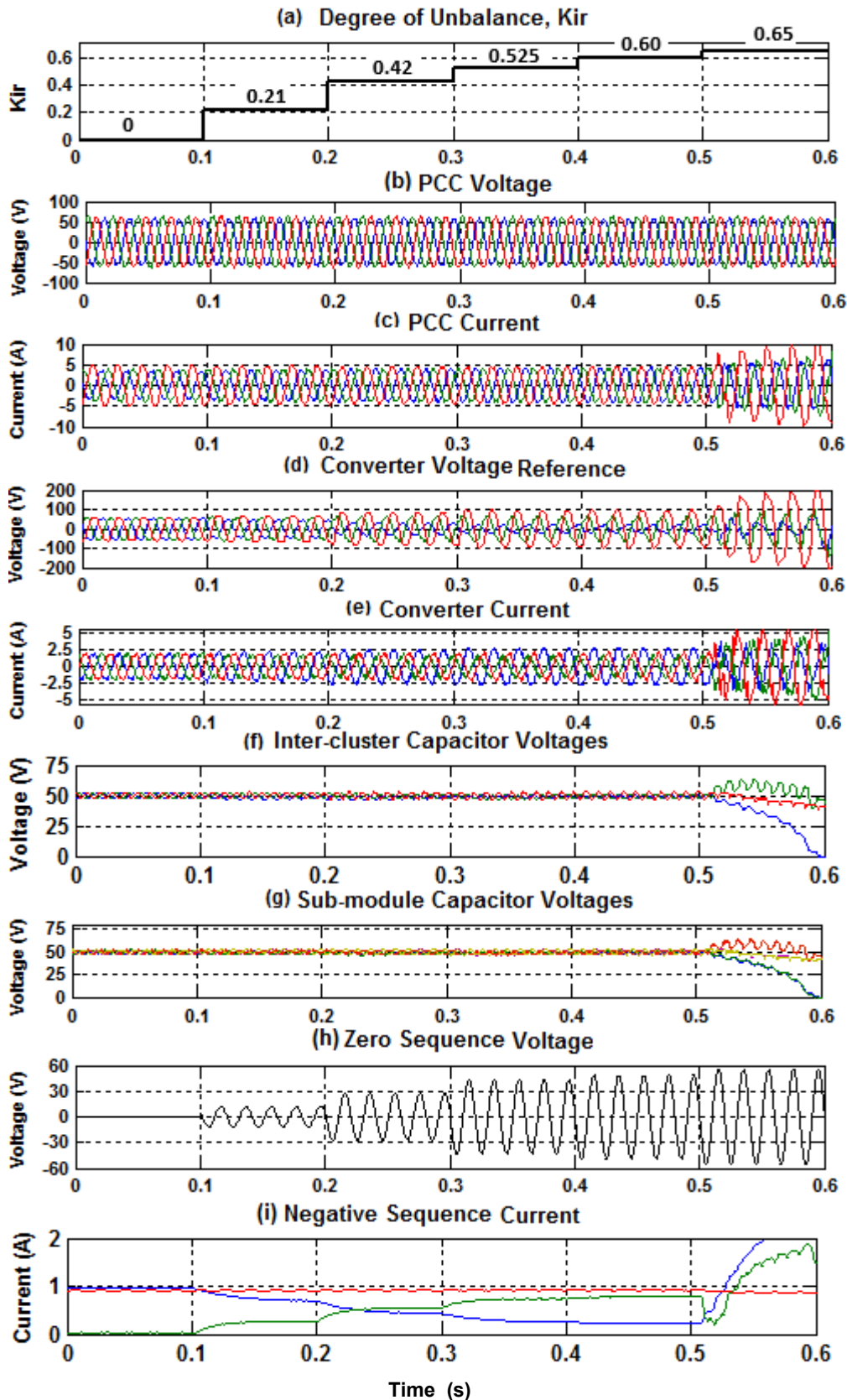


Figure 6.22: Operating behaviour of SSBC under unbalance load using sinusoidal zero sequence voltage injection.

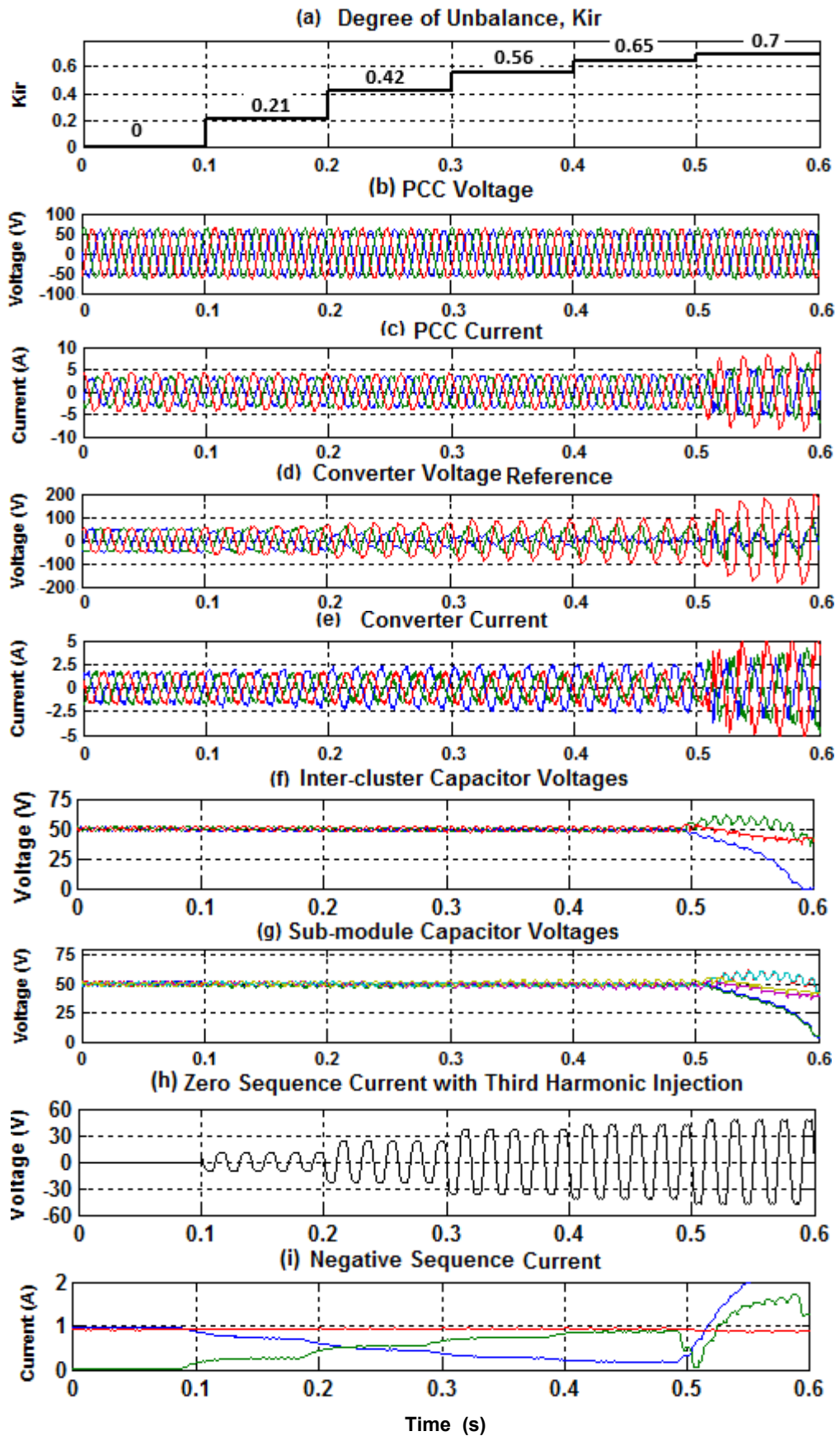


Figure 6.23: Operating behaviour of SSBC under unbalance load compensation using third harmonic zero sequence voltage injection.

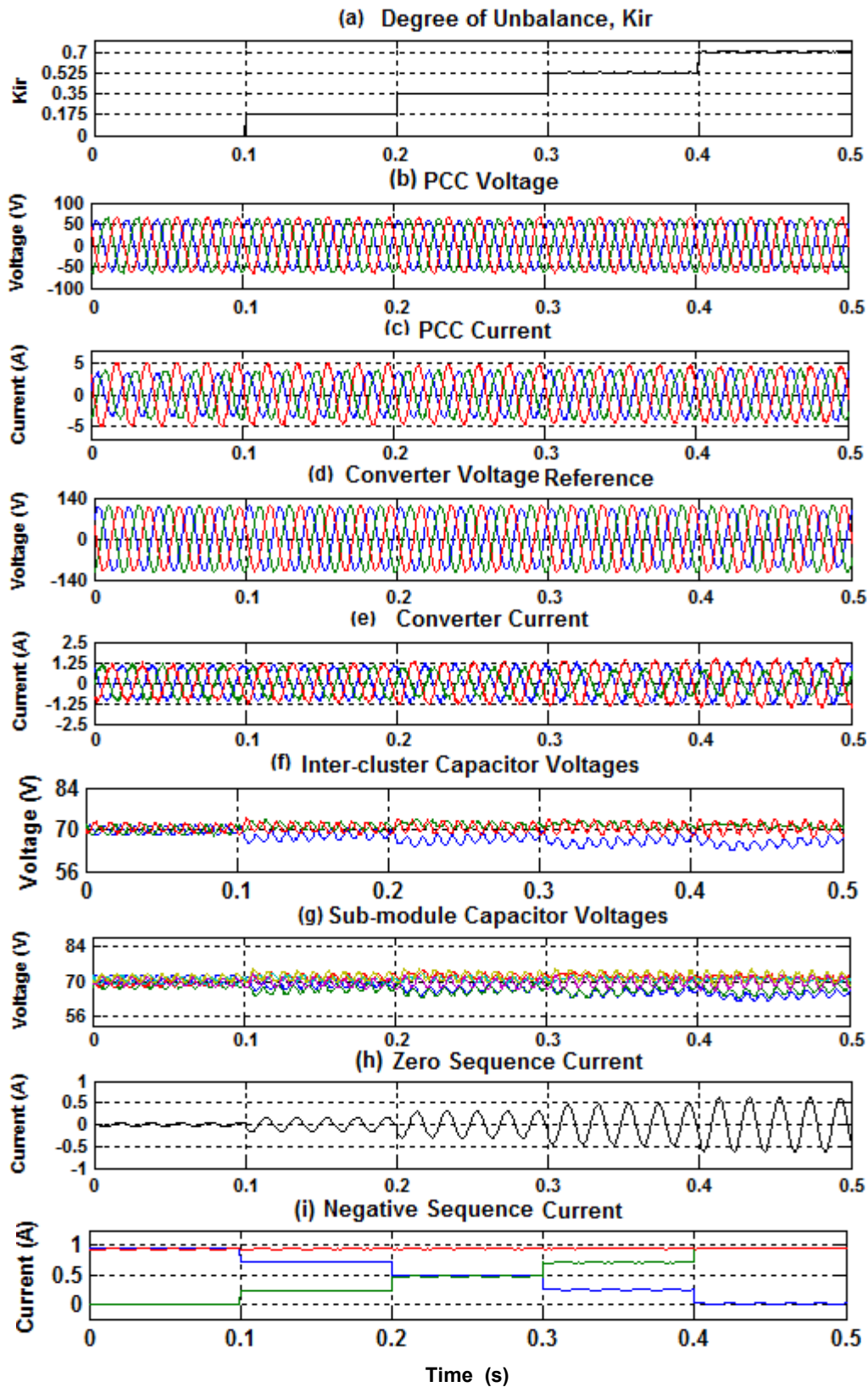


Figure 6.24: Operating behaviour of SDBC under unbalance load using sinusoidal zero sequence current injection.



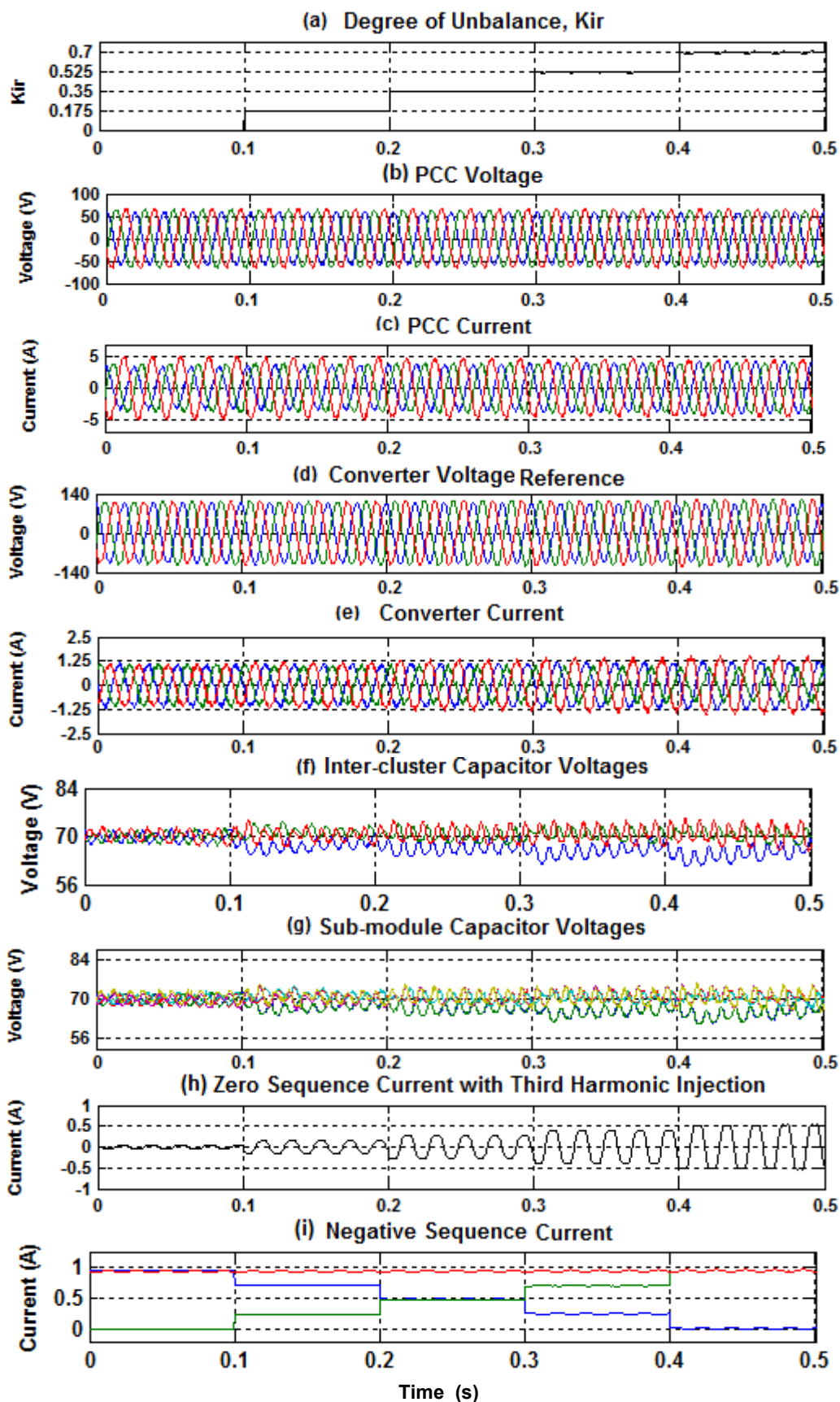


Figure 6.25: Operating behaviour of SDBC under unbalance load compensation using third harmonic zero sequence current injection.

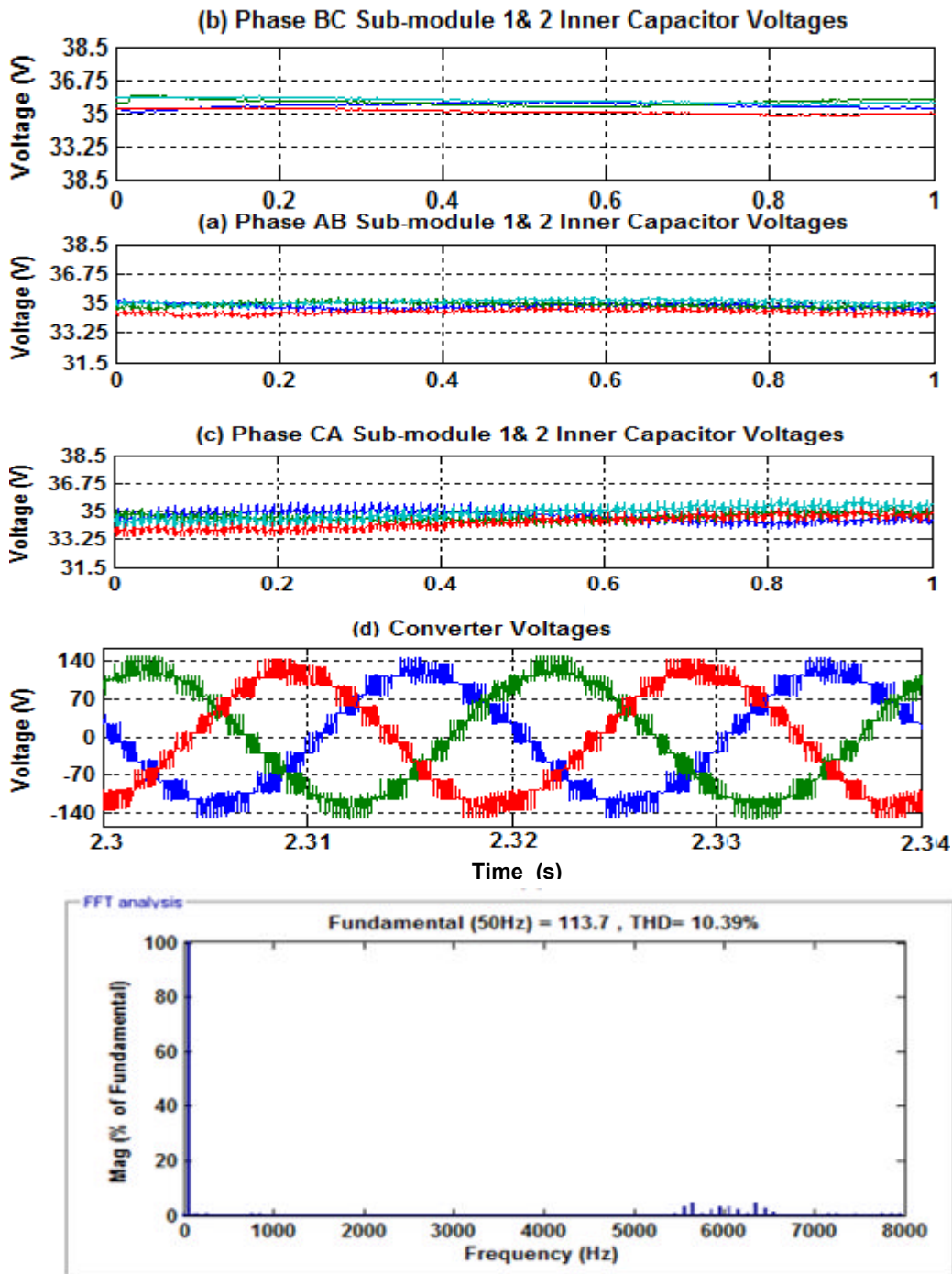


Figure 6.26: Operating behaviour of SDBC under unbalance load compensation using third harmonic zero sequence current injection.

To highlight the effectiveness of the STATCOM controller in compensating the positive sequence reactive current and negative sequence current at PCC, the power quality performance is shown through spectrum plot of the supply end current when using SDBC STATCOM. Figure 6.27 shows that at the full compensation the current THD is a low 4.13%. This gives a clear indication of good power quality performance since the voltage at PCC is assumed well-balanced and harmonic free. The SSBC case is not displayed because its

capability is limited, thus resulting in injected distorted current when its sub-module capacitor voltages are unstable.

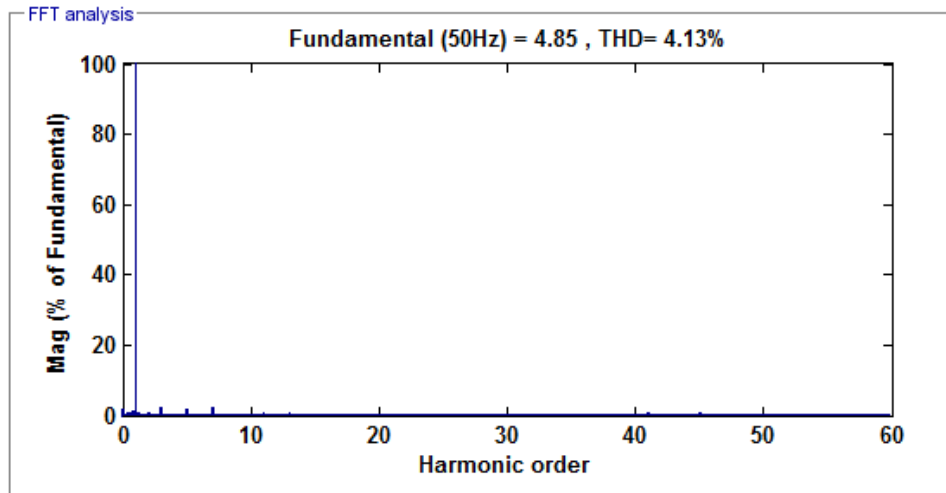


Figure 6.27: Supply end phase current THD during full compensation of SDBC

## 6.8 Comparison between Simulation and Experimental Results

Both experimental and simulation studies were performed under the same conditions and results obtained are seen to be similar. The positive sequence reactive power and negative sequence current at the point of common coupling is shown to be fully compensated by the SDBC STATCOM controller under both simulation and experimental tests. While for the single star configured MMCC, the sub-module dc capacitors become uncontrollable as  $K_{ir}=0.65$  and  $K_{ir}=0.7$  for the fundamental and third harmonic injection methods under both simulation and experimental test.

The significant differences between both cases are;

1. Once the converter voltage exceeds 100V, the sub-module capacitor voltages become uncontrollable, thus resulting in the sub-module capacitor voltages drastically dropping below or above  $\pm 50\%$  their nominal values in the experimental test while for the simulation test, it does not drop below  $\pm 20\%$ .
2. In both test conditions using the SSBC-MMCC, once the converter voltage exceeds its maximum value, the current injected into the grid becomes distorted.
3. The converter waveforms of the experimental results appear to be less ideal because of the switching devices were not ideal.

## 6.9 Summary

The chapter investigated the MMCC STATCOM for compensating simultaneously unbalanced load current and reactive power. It has shown that the voltage/current operating ranges of both the star and delta configured MMCC STATCOMs are limited, due to the zero sequence voltage or current injection necessary to balance inter cluster dc-link voltages. This chapter proposed the addition of a third harmonic component to its fundamental zero sequence voltage/current components to extend their operating ranges. The effect of such addition has been shown to reduce the voltage and current requirements of SSBC and SDBC respectively. Neither the third harmonic nor zero sequence components are added to the grid since they only flow within the three phase clusters. A detailed analysis of the operating ranges of both star and delta configured MMCC in rating the dc-link voltage (star) and cluster current (delta) has been discussed. This has shown that the third harmonic zero sequence component injection technique offers an extension of the operating range at a given dc-link voltage (SSBC) and cluster current (SDBC), and also lower dc-link voltage and current rating, at a given degree of unbalance for both star and delta configured MMCC respectively except for the dead zone which occurs at the worst condition of the zero sequence voltage.

Experimental validations of the analysis confirmed that, with the newly proposed scheme, the capability of the SSBC MMCC-based STATCOM for unbalanced load compensation can be much improved. The extended voltage operating range allows it to operate normally for a degree of load unbalance 5% higher than the case when only the sinusoidal zero sequence voltage is used. For the same unbalance, the converter voltage can be reduced by 12%. In conclusion, regardless of the superior capability provided by SDBC, the zero sequence current injected using the third harmonic component technique requires less current compared to the fundamental zero sequence current counterpart.

## **Chapter 7**

### **Conclusion and Recommendations for Future Research**

#### **7.1 Conclusion**

This research has focused on investigating Modular Multilevel Cascaded Converters in STATCOM applications, using the flying Capacitor H-bridge converter as sub-modules. To the author's knowledge, no study has investigated the use of such MMCCs for unbalanced STATCOM applications. The simulation and experimental studies have shown the capability of such converters for both reactive power and negative sequence current compensation. This research has helped to fill a knowledge gap regarding sub-module concepts for MMCC STATCOM applications in unbalanced load conditions.

The main contributions and achievements of this study are summarised below;

1. A study was carried out to assess which sub-module and MMCC configurations best suit STATCOM applications. These were based on the metrics of footprint, cost, control complexity and redundancy. From the assessment, it was established that the H-bridge sub-module is the most feasible for STATCOM applications, followed by FC H-bridge sub-modules when applied as a single star MMCC. The half bridge and FC half bridge sub-modules were seen to offer the least benefits for STATCOM applications along with the double star configurations.
2. A study was carried out to decide which pulse width modulation techniques best suit the operation of the FC-MMCC for STATCOM applications. This was based on the assessment of total harmonic distortion, sub-module switch utilization, natural balancing of inner flying capacitors and power losses. Two new modulation techniques of carrier-swapped PWM along with phase disposed and PS-PWM, were analysed under the four performance metrics. In comparison with the other three schemes, the PS-PWM stands out as the best in terms of natural balancing capability for the inner flying capacitors, total

harmonic distortion, and sub-module switch utilization, because the bypass states of the FC-MMCC inner capacitors far exceed in number their charge/discharge operating switch states. Also, among all the PWM schemes investigated, the quarter cycle swapped carrier PWM provides the lowest power losses because of its conduction and switch transition periods.

3. One of the significant contributions of this research work is the development of a novel space vector modulation technique, the overlapping hexagon space vector modulation method. Unlike the conventional multilevel SVM scheme, this uses either multiple two-level or three-level hexagons which are overlapped with each other. By dividing the MMCC into multiple voltage tiers, it performs switching state selection and duty ratio calculation per hexagon and per tier in the same ways as when controlling a two-level three-phase H-bridge or a three-level FC converter. The method avoids complicated procedures when using a single multilevel hexagon and offers flexibility and simplicity for controlling an MMCC with any number of chained modules. The simulation and experimental test show that the overlapping hexagon SVM provides superior performance and is applicable for all MMCC sub-modules.
4. For the FC-MMCC STATCOM, the author developed a method for determining the rated value of the MMCC dc capacitor voltage through phasor analysis and equations. This relationship highlighted the influence of the filter size and cut-off frequencies on the rating of the MMCC cluster dc voltage. An experimental closed loop system for validating the use of FC-MMCC in reactive power compensation has been developed, taking into consideration the choice of filter size, voltage rating, and sub-module capacitors. The experimental and simulation results agreed well.
5. Another important contribution of the work is the analysis and quantification of the operating ranges of both single star and delta configured MMCCs for unbalanced load compensation. For the star-connected case, an analytical expression has been derived showing clearly the relationship between the zero sequence voltage magnitude

and the level of load unbalance expressed in terms of negative to positive sequence current. This shows that the level of unbalanced current the SSBC can compensate without overloading its phase voltage is around 0.6. Likewise, for the delta connection, an expression for the zero sequence current with respect to the level of load unbalance has also been derived, and shows that  $i_o$  does not equal infinity when  $k_{ir}=1$  but rather has a finite value unlike for  $v_o$  under SSBC case. Test results confirm that the influence of a high load unbalance  $k_{ir}=0.7$  is completely compensated.

6. To extend the operating capabilities of both configurations, the research further investigated the application of third harmonic injection technique. Simulation and experiment confirmed that the third harmonic injection can allow a significant operating range extension and reduced zero sequence current magnitude by 7.69% and 16.6% compared to the sinusoidal zero sequence voltage and current.

At the time of writing, five published conference papers have been derived from the work based on Chapters 3, 5 and 6. Three journal publications are under considerations based on Chapters 3, 4 and 6.

## 7.2 Future Recommendation

The current research can be extended in further research which as suggested below;

1. Investigation in this research was for unbalanced load operation using both fundamental and third harmonic zero sequence components for inter-cluster voltage balancing control. The use of square wave, third harmonic square wave and optimum injection techniques for extending the capability of the SSBC may further enhance the viability of this converter topology.
2. Proportional resonant controllers can be implemented for both inter-cluster balancing and current control loops in order to reduce control complexity.
3. The FC-MMCC can also be validated for active filtering and reactive power compensation under unbalanced load conditions.

4. The overlapping hexagon SVM can be further implemented on the FC-MMCC experimental rig to give a detailed comparison with MMCC H-bridge sub-modules.
5. The overlapping hexagon SVM can further be modified to implement the FC-MMCC STATCOM for unbalanced load compensation.
6. Finally, two inter-cluster voltage balancing methods using zero sequence components and negative sequence currents can be applied to both configurations of star and delta MMCC operating under unbalanced voltage condition. The two inter-cluster voltage balancing control methods can be validated experimentally on the FC-MMCC rig under this condition.



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## Appendix A

The unbalance voltage vectors are given as;

$$v_{\alpha\beta} = \begin{bmatrix} v_{\alpha} \\ v_{\beta} \end{bmatrix} = v_{\alpha\beta}^{+1} + v_{\alpha\beta}^{-1} = V^{+1} \begin{bmatrix} \sin(\omega t + \phi^{+1}) \\ \cos(\omega t + \phi^{+1}) \end{bmatrix} + V^{-1} \begin{bmatrix} \sin(-\omega t + \phi^{-1}) \\ \cos(-\omega t + \phi^{-1}) \end{bmatrix} \quad (\text{A.1})$$

Two rotating reference frames  $dq^{+1}$  and  $dq^{-1}$  having angular positions  $\theta$  and  $-\theta$  are considered where  $\theta = \omega t$  occurs when the angle is perfectly detected by the PLL. Equation (A.1) can be expressed in  $dq^{+1}$  and  $dq^{-1}$  frames as;

$$v_{dq}^{+1} = \begin{bmatrix} v_d^{+1} \\ v_q^{+1} \end{bmatrix} = \begin{bmatrix} \bar{v}_d^{+1} \\ \bar{v}_q^{+1} \end{bmatrix} + \begin{bmatrix} \tilde{v}_d^{+1} \\ \tilde{v}_q^{+1} \end{bmatrix} = \underbrace{V^{+1} \begin{bmatrix} \sin\phi^{+1} \\ \cos\phi^{+1} \end{bmatrix}}_{DC\text{terms}} + \underbrace{V^{-1} \begin{bmatrix} \cos 2\omega t & -\sin 2\omega t \\ \sin 2\omega t & \cos 2\omega t \end{bmatrix} \begin{bmatrix} \sin\phi^{-1} \\ \cos\phi^{-1} \end{bmatrix}}_{AC\text{terms}} \quad (\text{A.2})$$

$$v_{dq}^{-1} = \begin{bmatrix} v_d^{-1} \\ v_q^{-1} \end{bmatrix} = \begin{bmatrix} \bar{v}_d^{-1} \\ \bar{v}_q^{-1} \end{bmatrix} + \begin{bmatrix} \tilde{v}_d^{-1} \\ \tilde{v}_q^{-1} \end{bmatrix} = \underbrace{V^{-1} \begin{bmatrix} \sin\phi^{-1} \\ \cos\phi^{-1} \end{bmatrix}}_{DC\text{terms}} + \underbrace{V^{+1} \begin{bmatrix} \cos 2\omega t & \sin 2\omega t \\ -\sin 2\omega t & \cos 2\omega t \end{bmatrix} \begin{bmatrix} \sin\phi^{+1} \\ \cos\phi^{+1} \end{bmatrix}}_{AC\text{terms}} \quad (\text{A.3})$$

Both equations clearly show that the AC terms in  $dq^{+1}$  and  $dq^{-1}$  axes result from the DC terms in  $dq^{-1}$  and  $dq^{+1}$  axes respectively. These  $2\omega$  transformation matrices are represented as;

$$[T_{dq}^{+2}] = [T_{dq}^{-2}]^T = \begin{bmatrix} \cos 2\omega t & -\sin 2\omega t \\ \sin 2\omega t & \cos 2\omega t \end{bmatrix} \quad (\text{A.4})$$

Therefore, (1.19) and (1.20) can be written as;

$$\begin{aligned} v_{dq}^{+1} &= \bar{v}_{dq}^{+1} + [T_{dq}^{+2}] \bar{v}_{dq}^{-1} \\ v_{dq}^{-1} &= \bar{v}_{dq}^{-1} + [T_{dq}^{-2}] \bar{v}_{dq}^{+1} \end{aligned} \quad (\text{A.5})$$

The estimated values at the DDSRF outputs are;

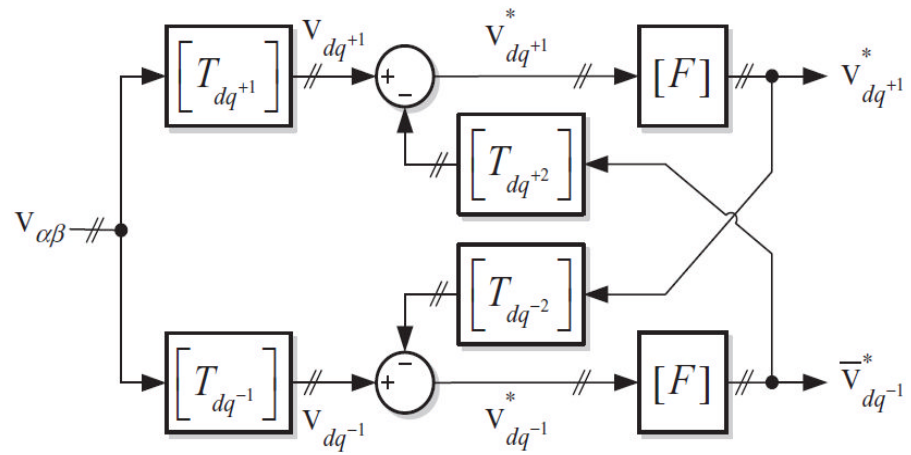
$$\begin{aligned} \bar{v}_{dq}^{+1} &= [F] \left\{ v_{dq}^{+1} - [T_{dq}^{+2}] \bar{v}_{dq}^{-1} \right\} \\ \bar{v}_{dq}^{-1} &= [F] \left\{ v_{dq}^{-1} + [T_{dq}^{-2}] \bar{v}_{dq}^{+1} \right\} \end{aligned} \quad (\text{A.6})$$

$$[F] = \begin{bmatrix} LPF(s) & 0 \\ 0 & LPF(s) \end{bmatrix}$$

where

$$LPF(s) = \frac{\omega_f}{s + \omega_f}$$

The block diagram of the DDSRF is shown below.



Block diagram of the DDSRF [93]

## Appendix B

### B.1: IGBT and diode thermal characteristics

Device	Thermal resistance	K/W
IGBT	Junction to case $R_{thJC}$	0.66
	Case to heatsink $R_{thCH}$	0.7
Diode	Junction to case $R_{thJC}$	0.9
	Case to heatsink $R_{thCH}$	0.7
Heatsink $R_{thH}$		2

### B.2: PD-PWM IGBT and diode Conduction loss

Carrier frequency (Hz)	Total IGBT conduction losses (W)				Total Diode conduction losses (W)			
	Modulation index ( $m_a$ )							
	0.6	0.7	0.8	0.9	0.6	0.7	0.8	0.9
750	15.52	20.83	26.29	31.82	6.05	6.48	6.40	5.91
1500	15.52	20.82	26.29	31.82	6.05	6.48	6.40	5.91
3000	15.52	20.82	26.28	31.82	6.05	6.48	6.40	5.91

### B3: PD-PWM IGBT and diode switching loss

Carrier frequency (Hz)	Total IGBT switching losses (W)				Total Diode switching losses (W)			
	Modulation index ( $m_a$ )							
	0.6	0.7	0.8	0.9	0.6	0.7	0.8	0.9
750	0.050	0.058	0.065	0.070	0.014	0.016	0.02	0.018
1500	0.099	0.116	0.129	0.139	0.028	0.032	0.04	0.036
3000	0.2	0.232	0.258	0.276	0.057	0.064	0.07	0.072



**B4: PD-PWM Inner flying capacitor power losses**

Carrier frequency(Hz)	Flying Capacitor	Modulation Index ( $m_a$ )			
		0.6	0.7	0.8	0.9
750	C <sub>a1</sub>	4.075	4.821	5.172	4.998
	C <sub>a2</sub>	4.049	4.821	5.163	4.956
	C <sub>b1</sub>	0.392	0.314	0.278	0.301
	C <sub>b2</sub>	0.389	0.302	0.280	0.257
1500	C <sub>a1</sub>	4.050	4.818	5.152	4.970
	C <sub>a2</sub>	4.050	4.818	5.152	4.97
	C <sub>b1</sub>	0.391	0.313	0.273	0.288
	C <sub>b2</sub>	0.391	0.313	0.273	0.288
3000	C <sub>a1</sub>	4.051	4.820	5.155	4.973
	C <sub>a2</sub>	4.051	4.820	5.155	4.973
	C <sub>b1</sub>	0.390	0.311	0.270	0.285
	C <sub>b2</sub>	0.390	0.311	0.270	0.285

**B5: PD-PWM Total Losses**

Carrier frequency (Hz)	Modulation index ( $m_a$ )			
	0.6	0.7	0.8	0.9
750	30.52	37.64	43.62	48.33
1500	30.58	37.71	43.70	48.41
3000	30.71	37.85	43.87	48.59

**B6: PD-PWM Sub-module Switch utilization**

Carrier frequency(Hz)	switches	Modulation Index ( $m_a$ )			
		0.6	0.7	0.8	0.9
750	S <sub>a1</sub>	0.112	0.348	0.687	1.129
	S <sub>a2</sub>	1.310	1.663	1.988	2.306
	S <sub>a3</sub>	0.112	0.348	0.688	1.113
	S <sub>a4</sub>	1.296	1.651	1.990	2.310
1500	S <sub>a1</sub>	0.112	0.347	0.688	1.131
	S <sub>a2</sub>	1.296	1.650	1.988	2.306
	S <sub>a3</sub>	0.112	0.349	0.689	1.120
	S <sub>a4</sub>	1.296	1.651	1.990	2.310
3000	S <sub>a1</sub>	0.112	0.348	0.688	1.115
	S <sub>a2</sub>	1.296	1.650	1.988	2.306
	S <sub>a3</sub>	0.111	0.347	0.687	1.116
	S <sub>a4</sub>	1.296	1.651	1.990	2.311

**B7: Quarter cycle rotation PWM IGBT and diode Conduction loss**

Carrier frequency (Hz)	Total IGBT conduction losses (W)				Total Diode conduction losses (W)			
	Modulation index ( $m_a$ )				Modulation index ( $m_a$ )			
	0.6	0.7	0.8	0.9	0.6	0.7	0.8	0.9
750	12.48	16.85	21.82	27.30	5.34	5.87	6.04	5.79
1500	12.45	16.83	21.86	27.32	5.34	5.87	6.04	5.79
3000	12.45	16.83	21.83	27.32	5.34	5.87	6.04	5.80

**B8: Carrier cycle rotation PWM Conduction loss**

Carrier frequency (Hz)	Total IGBT conduction losses (W)				Total Diode conduction losses (W)			
	Modulation index ( $m_a$ )				Modulation index ( $m_a$ )			
	0.6	0.7	0.8	0.9	0.6	0.7	0.8	0.9
750	13.91	18.34	23.14	28.45	5.81	6.26	6.30	5.97
1500	13.95	18.47	23.34	28.66	5.81	6.29	6.38	6.02
3000	13.95	18.48	23.35	28.67	5.81	6.30	6.36	6.02

**B9: Quarter cycle rotation PWM Switching loss**

Carrier frequency (Hz)	Total IGBT switching losses (W)				Total Diode switching losses (W)			
	Modulation index ( $m_a$ )				Modulation index ( $m_a$ )			
	0.6	0.7	0.8	0.9	0.6	0.7	0.8	0.9
750	0.046	0.055	0.054	0.062	0.012	0.015	0.014	0.015
1500	0.083	0.098	0.114	0.133	0.023	0.026	0.030	0.030
3000	0.160	0.188	0.220	0.255	0.044	0.051	0.059	0.067

**B10: Carrier cycle rotation PWM Switching loss**

Carrier frequency (Hz)	Total IGBT switching losses (W)				Total Diode switching losses (W)			
	Modulation index ( $m_a$ )				Modulation index ( $m_a$ )			
	0.6	0.7	0.8	0.9	0.6	0.7	0.8	0.9
750	0.065	0.078	0.09	0.102	0.018	0.021	0.023	0.025
1500	0.133	0.156	0.179	0.206	0.037	0.042	0.047	0.053
3000	0.264	0.313	0.359	0.408	0.072	0.085	0.096	0.106

**B11: Quarter cycle rotation PWM Flying Capacitor losses**

Carrier frequency(Hz)	Flying Capacitor	Modulation Index ( $m_a$ )			
		0.6	0.7	0.8	0.9
750	C <sub>a1</sub>	1.459	1.812	2.020	2.024
	C <sub>a2</sub>	1.462	1.812	2.014	2.017
	C <sub>b1</sub>	1.459	1.809	2.014	2.016
	C <sub>b2</sub>	1.461	1.816	2.020	2.025
1500	C <sub>a1</sub>	1.460	1.810	2.019	2.019
	C <sub>a2</sub>	1.458	1.807	2.013	2.011
	C <sub>b1</sub>	1.462	1.814	2.021	2.019
	C <sub>b2</sub>	1.464	1.817	2.026	2.027
3000	C <sub>a1</sub>	1.463	1.816	2.026	2.025
	C <sub>a2</sub>	1.461	1.812	2.020	2.017
	C <sub>b1</sub>	1.461	1.812	2.020	2.019
	C <sub>b2</sub>	1.463	1.815	2.026	2.027

**B12: Carrier cycle rotation PWM Flying Capacitor losses**

Carrier frequency(Hz)	Flying Capacitor	Modulation Index ( $m_a$ )			
		0.6	0.7	0.8	0.9
750	C <sub>a1</sub>	1.564	1.8879	2.0542	2.024
	C <sub>a2</sub>	1.567	1.9025	2.0533	1.9863
	C <sub>b1</sub>	1.561	1.8869	2.0517	2.0177
	C <sub>b2</sub>	1.564	1.8904	2.0519	2.0181
1500	C <sub>a1</sub>	1.572	1.905	2.076	2.036
	C <sub>a2</sub>	1.572	1.906	2.076	2.036
	C <sub>b1</sub>	1.573	1.907	2.080	2.042
	C <sub>b2</sub>	1.573	1.907	2.080	2.042
	C <sub>a1</sub>	1.575	1.909	2.0824	2.043
	C <sub>a2</sub>	1.575	1.909	2.082	2.043

3000	C <sub>b1</sub>	1.575	1.910	2.083	2.045
	C <sub>b2</sub>	1.575	1.910	2.083	2.045

### B13: Quarter cycle rotation PWM Total loss

Carrier frequency (Hz)	Modulation index (m <sub>a</sub> )			
	0.6	0.7	0.8	0.9
750	23.72	30.04	35.99	41.25
1500	23.74	30.07	36.11	41.36
3000	23.84	30.19	36.25	41.53

### B14: Carrier cycle rotation PWM Total loss

Carrier frequency (Hz)	Modulation index (m <sub>a</sub> )			
	0.6	0.7	0.8	0.9
750	26.05	32.26	37.77	42.64
1500	26.22	32.58	38.23	43.10
3000	26.40	32.80	38.49	43.38

### B15: Quarter fundamental cycle rotation method Sub-module Switch utilization

Carrier frequency(Hz)	switches	Modulation Index (m <sub>a</sub> )			
		0.6	0.7	0.8	0.9
750	S <sub>a1</sub>	0.518	0.680	0.976	1.328
	S <sub>a2</sub>	0.467	0.761	1.051	1.407
	S <sub>a3</sub>	1.067	1.370	1.691	2.021
	S <sub>a4</sub>	1.067	1.370	1.690	2.020
1500	S <sub>a1</sub>	0.441	0.677	0.980	1.335
	S <sub>a2</sub>	0.508	0.755	1.060	1.415
	S <sub>a3</sub>	1.065	1.368	1.691	2.021



750	14.12	18.61	23.42	28.75	5.88	6.35	6.39	6.05
1500	14.12	18.62	23.44	28.75	5.89	6.35	6.40	6.05
3000	14.12	18.62	23.44	28.75	5.89	6.35	6.40	6.05

### B18: Phase shifted PWM Switching loss

Carrier frequency (Hz)	Total IGBT switching losses (W)				Total Diode switching losses (W)			
	Modulation index ( $m_a$ )				Modulation index ( $m_a$ )			
	0.6	0.7	0.8	0.9	0.6	0.7	0.8	0.9
750	0.179	0.209	0.242	0.274	0.049	0.056	0.064	0.071
1500	0.356	0.417	0.481	0.547	0.098	0.113	0.128	0.143
3000	0.712	0.833	0.961	1.093	0.197	0.227	0.257	0.286

### B19: Phase shifted PWM Flying Capacitor losses

Carrier frequency (Hz)	Flying Capacitor	Modulation Index ( $m_a$ )			
		0.6	0.7	0.8	0.9
750	C <sub>a1</sub>	1.013	1.379	1.719	1.713
	C <sub>a2</sub>	1.013	1.379	1.700	1.753
	C <sub>b1</sub>	1.013	1.379	1.722	1.718
	C <sub>b2</sub>	1.013	1.379	1.705	1.751
1500	C <sub>a1</sub>	1.014	1.380	1.712	1.737
	C <sub>a2</sub>	1.014	1.380	1.712	1.737
	C <sub>b1</sub>	1.014	1.380	1.711	1.733
	C <sub>b2</sub>	1.045	1.380	1.711	1.733
3000	C <sub>a1</sub>	1.014	1.380	1.712	1.735
	C <sub>a2</sub>	1.014	1.380	1.712	1.735
	C <sub>b1</sub>	1.014	1.380	1.712	1.735
	C <sub>b2</sub>	1.014	1.380	1.712	1.735

**B20: Phase shifted PWM Total loss**

Carrier frequency (Hz)	Modulation index ( $m_a$ )			
	0.6	0.7	0.8	0.9
750	24.28	30.74	36.96	42.06
1500	24.51	31.01	37.29	42.42
3000	24.97	31.55	37.90	43.11

**B21: Phase shifted PWM Sub-module Switch utilization**

Carrier frequency(Hz )	switches	Modulation Index ( $m_a$ )			
		0.6	0.7	0.8	0.9
750	S <sub>a1</sub>	0.881	1.164	1.462	1.793
	S <sub>a2</sub>	0.882	1.164	1.465	1.794
	S <sub>a3</sub>	0.882	1.164	1.462	1.793
	S <sub>a4</sub>	0.881	1.164	1.465	1.794
1500	S <sub>a1</sub>	0.883	1.164	1.466	1.796
	S <sub>a2</sub>	0.883	1.163	1.465	1.796
	S <sub>a3</sub>	0.883	1.163	1.466	1.796
	S <sub>a4</sub>	0.883	1.164	1.465	1.796
3000	S <sub>a1</sub>	0.883	1.164	1.465	1.796
	S <sub>a2</sub>	0.883	1.163	1.465	1.796
	S <sub>a3</sub>	0.883	1.164	1.465	1.796
	S <sub>a4</sub>	0.883	1.164	1.465	1.796



**B22: Comparison of PWM Schemes**

<i>PWM Schemes</i>	<i>Natural bal. capability/voltage deviation</i>	<i>Power losses</i>	<i>THD</i>	<i>Sub-module switch utilization</i>
<i>PS-PWM</i>	4	3	4	4
<i>Carrier PWM</i>	3	2	3	4
<i>Quarter PWM</i>	2	4	2	2
<i>PD-PWM</i>	1	1	1	1

## Appendix C

### C.1 Matlab Code for Case Study

```
thetai = 60:1:90;
thetai_rad = (thetai/180)*pi;
theta = (30/180)*pi;
Vpcc = 1;
Isreal = 1*cos(-theta);
Isimag = 1*sin(-theta);
Icimag = -Isimag;
Icreal = Icimag./tan(thetai_rad);
Icmag = sqrt(Icreal.^2+Icimag^2);
Zmag = 0.1;
for kc = 0.5 %limited to 10 max
thetaz = atan(kc);
thetaz_deg = (thetaz/pi)*180;
Vzmag = Icmag*Zmag;
thetavz = -thetai_rad+thetaz;
thetavz_deg = (thetavz/pi)*180;
b = Vzmag.*cos(thetavz);
Vdc1 = sqrt(Vpcc.^2+2*Vpcc.*Vzmag.*cos(thetavz)+Vzmag.^2);
con_angle =
atan((Icmag.*Zmag.*sin(thetavz))/(1+Icmag.*Zmag.*sin(thetavz)));
con_angle_deg = (con_angle/pi)*180;
Rconv = (Vpcc.*Icmag.*sin(thetai_rad));
Pconv = (Vpcc.*Icmag.*cos(thetai_rad));
end
figure(1);
plot(thetai,Vdc1,thetai,Vdc2,thetai,Vdc3,thetai,Vdc4);
```

### C.2 Matlab Code for Case Study Capacitor Voltage Ripple

```
thetai = 60:0.1:90;
thetai_radian = (thetai/180)*pi;
angle_Vpp = 0;
theta = (30/180)*pi;
Vpcc = 230;
```

```
Isreal =10*cos(-theta);
Isimag =10*sin(-theta);

Icimag = -Isimag;
Icreal = Icimag./tan(thetai_radian);

Icmag = sqrt(Icreal.^2+Icimag^2);
% Icmag = 1;
for kc = 0.05 %limited to 10 max

    w=2*pi*50;
    thetavz = atan(kc);
    kk=23;
    Zmag = 0.1*kk;

    Csm=0.25*1.12e-3;

    Vzmag = Icmag*Zmag;
    thetavz= -thetai_radian+thetaz;
    thetavz_deg = (thetavz/pi)*180;
    time=[];
    con_ang=[];
    Vsssi= [];
    thetasss=[];
    Rc= sqrt((Zmag.^2)./(1+ (kc)^2));
    t0=0;
    Lc=(kc*Rc)/w;
    N=1;
    Vdc= sqrt(Vpcc.^2+2*Vpcc.*Vzmag.*cos(thetavz)+Vzmag.^2);
    Vc_i=0.85*Vdc;
    con_angle= atan((Icmag.*Zmag.*sin(-
    thetai_radian+thetaz))/(1+Icmag.*Zmag.*sin(-thetai_radian+thetaz)));
    con_angledeg=(con_angle/pi)*180;
    con_ang=[con_ang con_angle];
    t=0.02;
```

```

q= cos(con_angle - thetai_radian).*(t);
y=(1/(2*w)).*(sin(2*w*t +con_angle + thetai_radian ) - sin(con_angle +
thetai_radian));
r=(Vc_i.*Icmag)./Csm;
rr=r.*(q - y);
Vsm_i =sqrt((300).^2 + rr);
Vssm=Vsm_i./(300);
Vzz=-r.*(q - y);
time=[time t];
thetasss=[thetasss thetai];
Vsssi= [Vsssi Vssm];
end

```

```

figure(2);
plot(thetasss,Vsssi,thetasss,Vsssi1 ,thetasss,Vsssi2,thetasss,Vsssi3);

```

### C.3 Clarke's and Park's Transformation

For three-phase symmetrical and balanced quantities like voltage  $v$ , having magnitude  $V$ , frequency  $f$ , angular velocity  $\omega=2\pi f$  and phase angle  $\theta=0$ . When defined in its stationary 3-phase **abc** reference frames:

$$v_a(t) = V \sin(\omega t + \theta), v_b(t) = V \sin(\omega t + \theta - \frac{2\pi}{3}), v_c(t) = V \sin(\omega t + \theta + \frac{2\pi}{3})$$

Clarke's transformation gives a representation of three-phase voltage vector in a stationary two-dimensional ( $\alpha$ - $\beta$ ) reference frame. The matrix representation for the power invariant Clarke's transformation is defined by equations (C3.1)-(C3.3)

$$\begin{bmatrix} \vec{V}_\alpha \\ \vec{V}_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} \vec{V}_a \\ \vec{V}_b \\ \vec{V}_c \end{bmatrix} \quad \text{where} \quad (C3.1)$$

$$\vec{V}_\alpha = \sqrt{\frac{2}{3}} \left( \vec{V}_a - \frac{1}{2} \vec{V}_b - \frac{1}{2} \vec{V}_c \right) \quad \text{and} \quad (C3.2)$$

$$\vec{V}_\beta = \sqrt{\frac{2}{3}} \left( -\frac{\sqrt{3}}{2} \vec{V}_b + \frac{\sqrt{3}}{2} \vec{V}_c \right) \quad (C3.3)$$

The inverse matrix representation for the power invariant Clarke's transformation is shown as;

$$\begin{bmatrix} \vec{V}_a \\ \vec{V}_b \\ \vec{V}_c \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} \vec{V}_\alpha \\ \vec{V}_\beta \end{bmatrix} \quad (\text{C3.4})$$

The  $\frac{2}{3}$  factor is a normalising factor that ensures the Clarke's transformation is a unit circle (i.e. 1.5 to 1 p.u.) and the square root  $\sqrt{\frac{2}{3}}$  ensures that this is kept when power is considered (power circle normalised to 1 pu) i.e.  $\sqrt{\frac{2}{3}} V \times \sqrt{\frac{2}{3}} I = \frac{2}{3} P$ .

The stationary  $\alpha$ - $\beta$  reference frame is further transformed into a  $d$ - $q$  frame rotating synchronous with a chosen reference frame at the angular frequency  $\omega$ . The matrix for transforming  $\alpha$ - $\beta$  to  $d$ - $q$  using the power invariant form of Park's transformation is given below as;

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} \vec{V}_\alpha \\ \vec{V}_\beta \end{bmatrix} \quad (\text{C3.5})$$

$$V_d = \sqrt{\frac{2}{3}} (\vec{V}_\alpha \cos\theta - \vec{V}_\beta \sin\theta) \quad (\text{C3.6})$$

$$V_q = \sqrt{\frac{2}{3}} (\vec{V}_\alpha \sin\theta + \vec{V}_\beta \cos\theta) \quad (\text{C3.7})$$

where  $\theta = \omega t$

The inverse matrix for the power invariant Park's transformation is given as;

$$\begin{bmatrix} \vec{V}_\alpha \\ \vec{V}_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} V_d \\ V_q \end{bmatrix} \quad (\text{C3.8})$$

Equation (C3.5) can further be simplified using (C3.1) having a direct  $abc$  to  $d$ - $q$  transformation as;

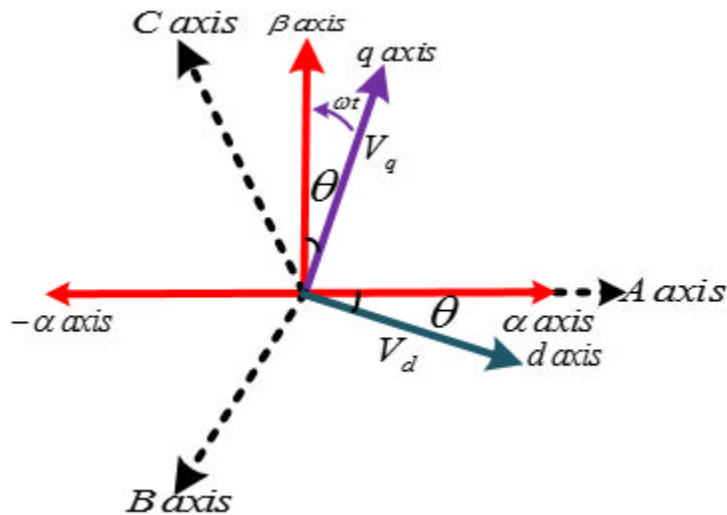
$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos\theta & \left(-\frac{1}{2}\cos\theta + \frac{\sqrt{3}}{2}\sin\theta\right) & -\left(\frac{1}{2}\cos\theta + \frac{\sqrt{3}}{2}\sin\theta\right) \\ \sin\theta & -\left(\frac{1}{2}\sin\theta + \frac{\sqrt{3}}{2}\cos\theta\right) & \left(-\frac{1}{2}\sin\theta + \frac{\sqrt{3}}{2}\cos\theta\right) \end{bmatrix} \begin{bmatrix} \vec{V}_a \\ \vec{V}_b \\ \vec{V}_c \end{bmatrix} \quad (\text{C3.9})$$

$$\begin{aligned} \sin\left(\theta \pm \frac{2\pi}{3}\right) &= -\frac{1}{2}\sin\theta \pm \frac{\sqrt{3}}{2}\cos\theta \\ \cos\left(\theta \pm \frac{2\pi}{3}\right) &= -\frac{1}{2}\cos\theta \mp \frac{\sqrt{3}}{2}\sin\theta \end{aligned} \tag{C3.10}$$

Substituting (C1.10) into (C1.9) results in;

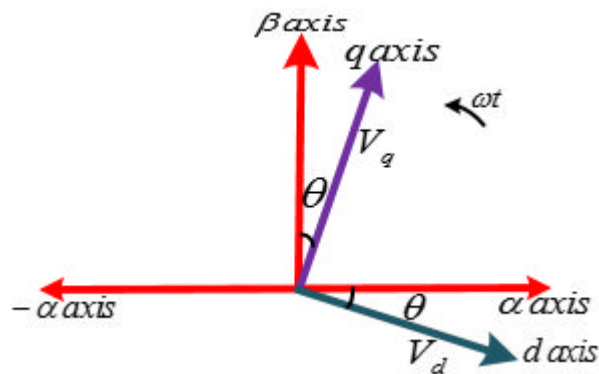
$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ \sin\theta & \sin\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta + \frac{2\pi}{3}\right) \end{bmatrix} \begin{bmatrix} \vec{V}_a \\ \vec{V}_b \\ \vec{V}_c \end{bmatrix} \tag{C3.11}$$

Figure below shows the stationary three-phase voltage and its representations in  $\alpha$ - $\beta$  and  $d$ - $q$  reference frames through Park's and Clarke's Transformation.



**Park's and Clarke's Transformation**

### Derivation of Decoupling Operator ( $e^{j\theta}$ )



**Park's Transformation**

Figure 2.3 shows a voltage vector in  $d$ - $q$  reference frame. The phase angle  $\theta$  is the displacement or phase shift between this voltage vector and the

synchronous reference frame and based on the arrow indicated direction of rotation it is a lagging phase angle. The voltage vector in  $\alpha\text{-}\beta$  and  $d\text{-}q$  forms could be written as complex quantities  $V_\alpha + jV_\beta$  and  $V_d + jV_q$  respectively.

Assuming unity magnitude we have

$\vec{V}_\alpha = \sin \omega t$  and  $\vec{V}_\beta = \cos \omega t$  then Park's transformation matrix can be re-written as;

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \sin \theta & \cos \theta \\ -\cos \theta & \sin \theta \end{bmatrix} \begin{bmatrix} \sin \omega t \\ \cos \omega t \end{bmatrix} \quad (\text{C3.12})$$

Neglecting the  $\sqrt{\frac{2}{3}}$  normalising factor

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} \sin \theta & \cos \theta \\ -\cos \theta & \sin \theta \end{bmatrix} \begin{bmatrix} \sin \omega t \\ \cos \omega t \end{bmatrix} = \begin{bmatrix} \sin(\omega t - \theta) \\ \cos(\omega t - \theta) \end{bmatrix} \quad (\text{C3.13})$$

The park's transformation can be expressed in term of an operator  $e^{j\theta}$

$$V_d + jV_q = [\text{operator}] \times (V_\alpha + jV_\beta) \quad (\text{C3.14})$$

Solving for [operator] in (C1.14) yields;

$$\begin{aligned} [\text{operator}] &= \frac{V_d + jV_q}{V_\alpha + jV_\beta} = \frac{\sin(\omega t - \theta) + j \cos(\omega t - \theta)}{\sin \omega t + j \cos \omega t} \\ &= (\sin(\omega t - \theta) + j \cos(\omega t - \theta))(\sin \omega t - j \cos \omega t) \\ &= \cos \theta + j \sin \theta = e^{j\theta} \end{aligned} \quad (\text{C3.15})$$

Therefore, the relationship between  $d\text{-}q$  and  $\alpha\text{-}\beta$  can be expressed as;

$$V_d + jV_q = e^{j\theta} \times (V_\alpha + jV_\beta) \quad (\text{C3.16})$$

#### C.4 Converter Voltage transformation from abc to d-q

The relationship between the converter STATCOM and PCC is defined as;

$$V_{PCC(abc)} = V_{C(abc)} + i_{C(abc)} R_f + L_f \frac{di_{C(abc)}}{dt} \quad (\text{C4.1})$$

Where  $R_f$  and  $L_f$  are the filtering resistance and inductance coupling the converter to PCC.

Transforming from stationary  $abc$  into  $\alpha\text{-}\beta$  reference frame, the voltage drop across the filter is a function of the converter current. The voltage across the filter can be calculated in  $\alpha\text{-}\beta$  reference frame using conventional circuit theory along with the equations for the drop across resistors and inductors as function of the current flowing through them as;

$$V_{f(\alpha\beta)} = i_{C(\alpha\beta)} R_f + L_f \frac{di_{C(\alpha\beta)}}{dt} \quad (C4.2)$$

Transforming from  $\alpha$ - $\beta$  voltage and current vectors into rotating  $d$ - $q$  reference frame vectors;

$$e^{-j\theta} V_{f(dq)} = e^{-j\theta} i_{C(dq)} R_f + L_f \frac{de^{-j\theta} i_{C(dq)}}{dt} \quad (C4.3)$$

$$V_{f(dq)} = i_{C(dq)} R_f + e^{j\theta} L_f \frac{de^{-j\theta} i_{C(dq)}}{dt}$$

The derivative term  $e^{j\theta} L_f \frac{de^{-j\theta} i_{C(dq)}}{dt}$  can be simplified using product rule,

Recall  $\frac{d}{dt}(v.u) = v \frac{du}{dt} + u \frac{dv}{dt}$  and  $\theta = \omega t$

$$\text{where } v = i_{cdq}, u = e^{-j\omega t}, \frac{dv}{dt} = \frac{di_{cdq}}{dt}, \frac{du}{dt} = -j\omega e^{-j\omega t} \quad (C4.4)$$

$$\frac{de^{-j\omega t} i_{cdq}}{dt} = -j\omega e^{-j\omega t} i_{cdq} + e^{-j\omega t} \frac{di_{cdq}}{dt} \quad (C4.5)$$

Substituting (C4.5) into (C4.3) gives;

$$V_{Cdq} = i_{Cdq} R_f + L_f \frac{di_{Cdq}}{dt} - j\omega L_f i_{Cdq} \quad (C4.6)$$

The definition of voltage and current vectors are given as;

$$v_{fdq} = v_{fd} + v_{fq}; i_{fdq} = i_{Cd} + i_{Cq} \quad (C4.7)$$

The converter voltage is expressed in terms of both PCC voltage and voltage drop across converter filter in  $d$ - $q$  frame as;

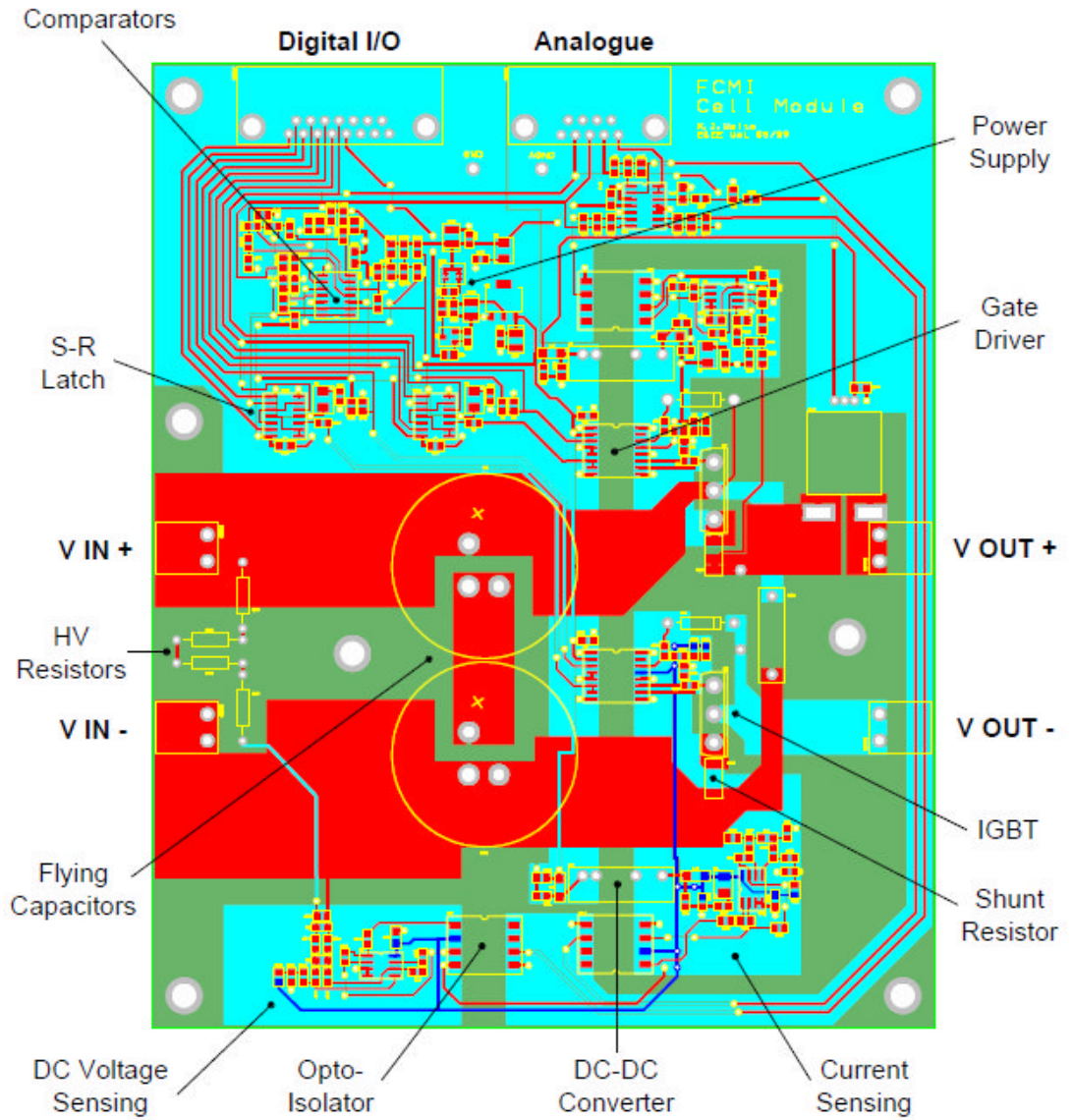
$$V_{Cd} = V_{dPCC} - i_{Cd} R_f - L_f \frac{di_{Cd}}{dt} - \omega L_f i_{Cq} \quad (C4.8)$$

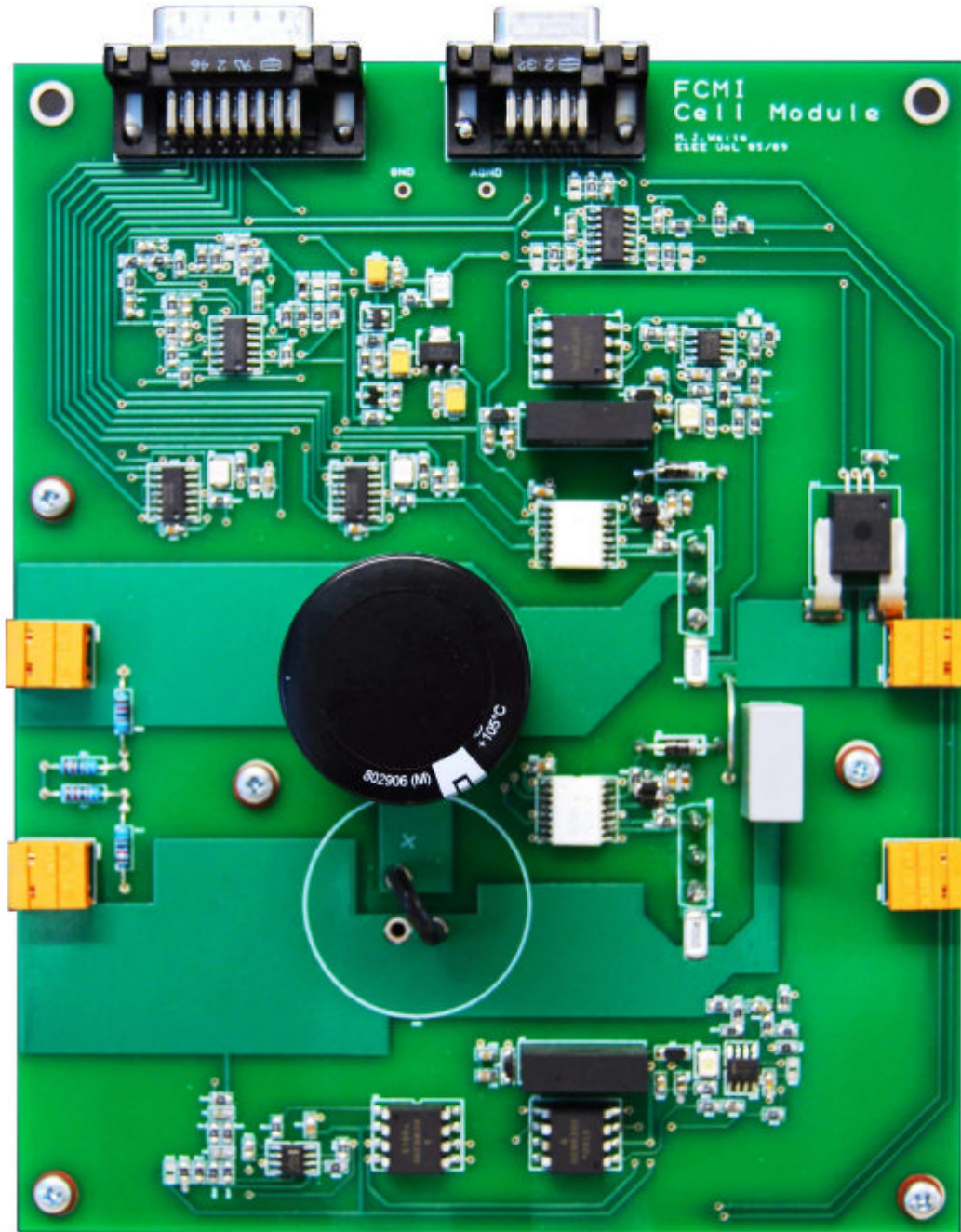
$$V_{Cq} = V_{qPCC} - i_{Cq} R_f - L_f \frac{di_{Cq}}{dt} + \omega L_f i_{Cd}$$

The equation above is used in calculating the appropriate inverter voltage to generate the desired compensation currents.



### C.5: Unit power cell card PCB design and Manufactured PCB [35]





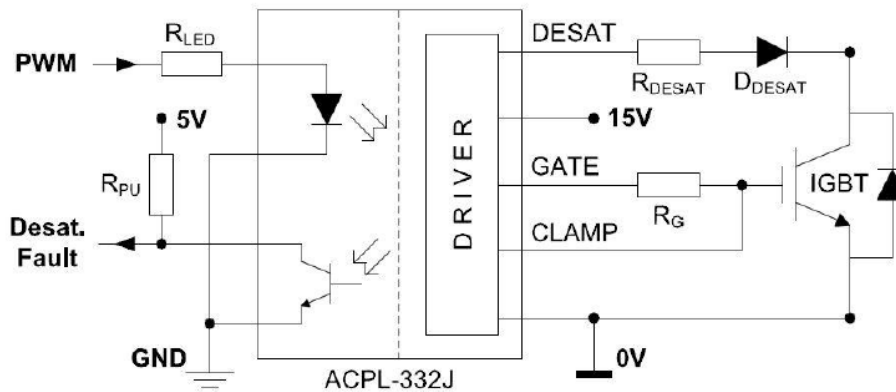
### C.6: IGBT characteristics and Capacitor characteristics

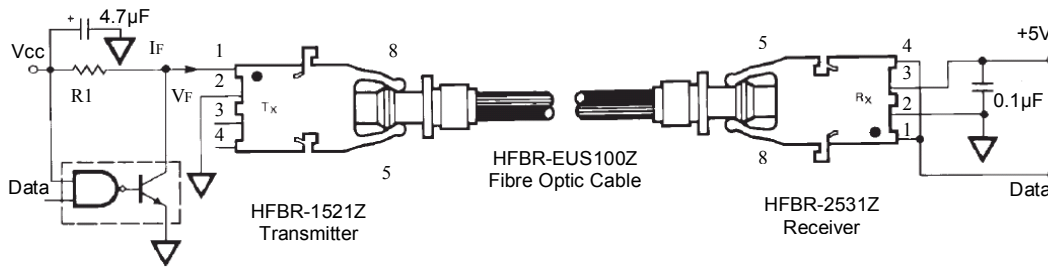
Parameter	Value
Maximum collector-emitter voltage $V_{CE}$	600 V
Maximum DC collector current $I_C$	30 A
Short-circuit collector $I_{C(SC)}$	275 A
Short-circuit withstand time $t_{SC}$	5 $\mu$ s

Collector-emitter saturation voltage $V_{CE(sat)}$	1.5 – 1.9 V
Gate-emitter threshold voltage $V_{GE(Th)}$	4.1 – 5.7 V
Total turn-on time $t_{on}$	44 – 50 ns
Total turn-off time $t_{off}$	300 – 382 ns

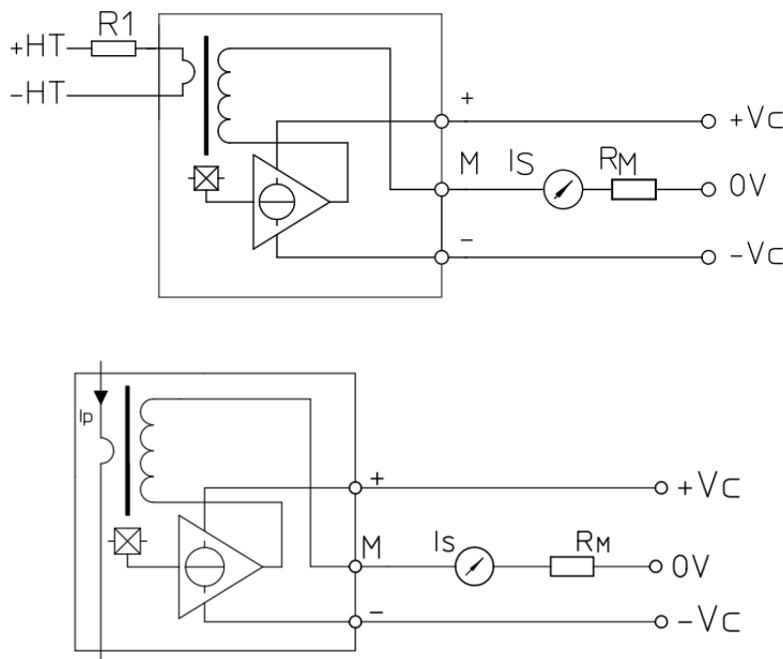
Parameter	Value
Capacitance	560 $\mu\text{F} \pm 20\%$
Maximum working voltage	400 V <sub>DC</sub>
Maximum surge voltage	450 V <sub>DC</sub>
Maximum RMS ripple current (120 Hz)	5.52A
Maximum RMS ripple current (10 kHz)	7.70 A
Lifetime	3000h

### C.7: Gate Drive Circuit and Fibre Optic Transmitter, Receiver Circuit Diagram [35]



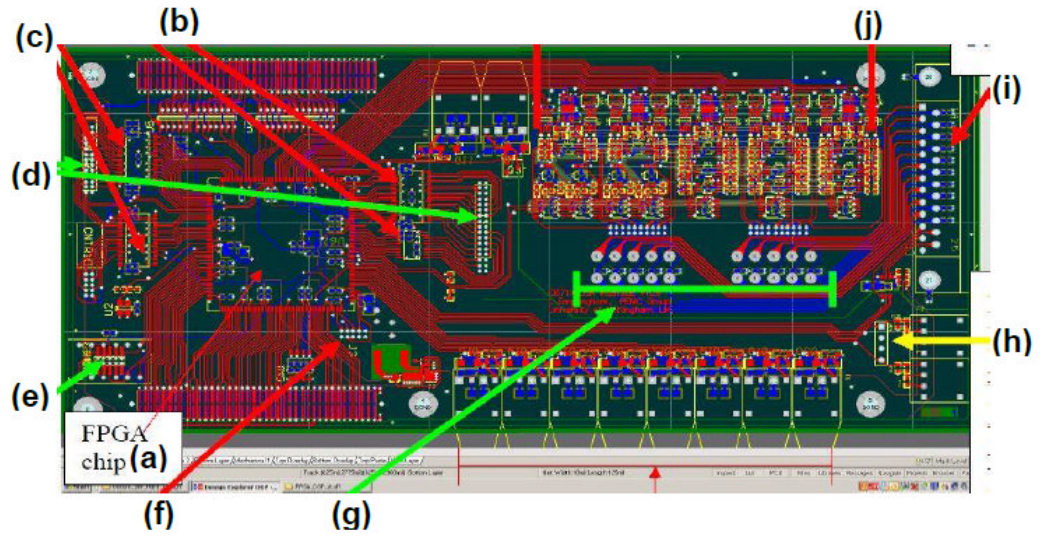


### C.8: Voltage and Current Transducer Circuit [35]



### C.9: Actel ProASIC FPGA board layout [35]

- (a) Actel ProASIC III FPGA Chip for data processing
- (b) Three Phillips LVC16245A bidirectional buffers
- (c) One Phillips 74LVC245A bidirectional buffers
- (d) 26 pin I/O Header connectors
- (e) Fault monitor display LED
- (f) 10-way programming connector for Flash Pro 4
- (g) Burden resistors for A/D converter at  $\pm 5V$  voltage range
- (h) 4-way header connector for Set/Reset Enable under faults
- (i) 25-way D-Sub connector for input A/D signals
- (j) 10 LTC 1407A-1 Analogue to Digital converters.



## Appendix D

### D1:Zero sequence Component derivation

The three phase zero sequence active powers across each cluster of the SSBC-MMCC based on (6.10) is expressed as;

$$\begin{aligned}
 P_{Ca}^o &= \frac{1}{4} \left( 2V_o I_p \cos(\varphi_o - \varphi_{ip}) - 2V_o I_n \cos(\varphi_o + \varphi_{in}) \right) \\
 P_{Cb}^o &= \frac{1}{4} \left( \begin{aligned} &-V_o I_p \cos(\varphi_o - \varphi_{ip}) - \sqrt{3}V_o I_p \sin(\varphi_o - \varphi_{ip}) + V_o I_n \cos(\varphi_o + \varphi_{in}) \\ &\quad - \sqrt{3}V_o I_n \sin(\varphi_o + \varphi_{in}) \end{aligned} \right) \quad (D1.1) \\
 P_{Cc}^o &= \frac{1}{4} \left( \begin{aligned} &-V_o I_p \cos(\varphi_o - \varphi_{ip}) + \sqrt{3}V_o I_p \sin(\varphi_o - \varphi_{ip}) + V_o I_n \cos(\varphi_o + \varphi_{in}) \\ &\quad + \sqrt{3}V_o I_n \sin(\varphi_o + \varphi_{in}) \end{aligned} \right)
 \end{aligned}$$

The three phase zero sequence active powers across each cluster of the SDBC-MMCC based on (6.11) is expressed as;

$$\begin{aligned}
 P_m &= \frac{1}{4} \left( \begin{aligned} &3V_p I_o \cos(\varphi_{vp} - \varphi_o) - \sqrt{3}V_p I_o \sin(\varphi_{vp} - \varphi_o) - 3V_n I_o \cos(\varphi_{vn} + \varphi_o) \\ &\quad + \sqrt{3}V_n I_o \sin(\varphi_{vn} + \varphi_o) \end{aligned} \right) \\
 P_m &= \frac{1}{4} \left( 2\sqrt{3}V_p I_o \sin(\varphi_{vp} - \varphi_o) - 2\sqrt{3}V_n I_o \sin(\varphi_{vn} + \varphi_o) \right) \quad (D1.2) \\
 P_m &= \frac{1}{4} \left( \begin{aligned} &-3V_p I_o \cos(\varphi_{vp} - \varphi_o) - \sqrt{3}V_p I_o \sin(\varphi_{vp} - \varphi_o) + 3V_n I_o \cos(\varphi_{vn} + \varphi_o) \\ &\quad + \sqrt{3}V_n I_o \sin(\varphi_{vn} + \varphi_o) \end{aligned} \right)
 \end{aligned}$$

Both (D1.1) and (D1.2) are simplified as;

$$\begin{aligned}
 \begin{bmatrix} P_{Ca}^o \\ P_{Cb}^o \\ P_{Cc}^o \end{bmatrix} &= \frac{1}{4} \left( \begin{aligned} &\left[ \begin{array}{cc} 2I_p \cos \varphi_{ip} & 2I_p \sin \varphi_{ip} \\ I_p (-\cos \varphi_{ip} + \sqrt{3} \sin \varphi_{ip}) & I_p (-\sin \varphi_{ip} - \sqrt{3} \cos \varphi_{ip}) \\ I_p (-\cos \varphi_{ip} - \sqrt{3} \sin \varphi_{ip}) & I_p (-\sin \varphi_{ip} + \sqrt{3} \cos \varphi_{ip}) \end{array} \right] \begin{bmatrix} V_o \cos \varphi_o \\ V_o \sin \varphi_o \end{bmatrix} \\ &+ \left[ \begin{array}{cc} -2I_n \cos \varphi_{in} & 2I_n \sin \varphi_{in} \\ I_n (\cos \varphi_{in} - \sqrt{3} \sin \varphi_{in}) & I_n (-\sin \varphi_{in} - \sqrt{3} \cos \varphi_{in}) \\ I_n (\cos \varphi_{in} + \sqrt{3} \sin \varphi_{in}) & I_n (-\sin \varphi_{in} + \sqrt{3} \cos \varphi_{in}) \end{array} \right] \begin{bmatrix} V_o \cos \varphi_o \\ V_o \sin \varphi_o \end{bmatrix} \end{aligned} \right) \quad (D1.3)
 \end{aligned}$$

$$\begin{bmatrix} P_{Cab}^o \\ P_{Cbc}^o \\ P_{Cca}^o \end{bmatrix} = \frac{1}{4} \left( \begin{bmatrix} V_p(\sqrt{3} \cos \varphi_{vp} - \sin \varphi_{vp}) & V_p(\sqrt{3} \sin \varphi_{vp} + \cos \varphi_{vp}) \\ 2V_p \sin \varphi_{vp} & -2V_p \cos \varphi_{vp} \\ V_p(-\sqrt{3} \cos \varphi_{vp} - \sin \varphi_{vp}) & V_p(-\sqrt{3} \sin \varphi_{vp} + \cos \varphi_{vp}) \end{bmatrix} \begin{bmatrix} I_o \cos \varphi_o \\ I_o \sin \varphi_o \end{bmatrix} \right. \\ \left. + \begin{bmatrix} V_n(-\sqrt{3} \cos \varphi_{vn} + \sin \varphi_{vn}) & V_n(\sqrt{3} \sin \varphi_{vn} + \cos \varphi_{vn}) \\ -2V_n \sin \varphi_{vn} & -2V_n \cos \varphi_{vn} \\ V_n(-\sqrt{3} \cos \varphi_{vn} + \sin \varphi_{vn}) & V_n(-\sqrt{3} \sin \varphi_{vn} + \cos \varphi_{vn}) \end{bmatrix} \begin{bmatrix} I_o \cos \varphi_o \\ I_o \sin \varphi_o \end{bmatrix} \right) \quad (D1.4)$$

(D1.3) and (D1.4) are transformed into  $\alpha$ - $\beta$  cluster power forms as;

$$\begin{bmatrix} P_{Ca}^o \\ P_{Cb}^o \\ P_{Cc}^o \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} P_{Ca}^o \\ P_{Cb}^o \\ P_{Cc}^o \end{bmatrix} \\ = \frac{1}{6} \left( \begin{bmatrix} 3I_p \cos \varphi_{ip} & 3I_p \sin \varphi_{ip} \\ -3I_p \sin \varphi_{ip} & 3I_p \cos \varphi_{ip} \end{bmatrix} + \begin{bmatrix} -3I_n \cos \varphi_{in} & 3I_n \sin \varphi_{in} \\ 3I_n \sin \varphi_{in} & 3I_n \cos \varphi_{in} \end{bmatrix} \right) \begin{bmatrix} V_o \cos \varphi_o \\ V_o \sin \varphi_o \end{bmatrix} \\ = \frac{1}{2} \begin{bmatrix} I_p \cos \varphi_{ip} - I_n \cos \varphi_{in} & I_p \sin \varphi_{ip} + I_n \sin \varphi_{in} \\ -I_p \sin \varphi_{ip} + I_n \sin \varphi_{in} & I_p \cos \varphi_{ip} + I_n \cos \varphi_{in} \end{bmatrix} \begin{bmatrix} V_o \cos \varphi_o \\ V_o \sin \varphi_o \end{bmatrix} \\ = \frac{1}{2} \begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{bmatrix} \begin{bmatrix} V_o \cos \varphi_o \\ V_o \sin \varphi_o \end{bmatrix} \quad (D1.5)$$

where:

$$\begin{aligned} A_{11} &= (I_p \cos \varphi_{ip} - I_n \cos \varphi_{in}) \\ A_{12} &= (I_p \sin \varphi_{ip} + I_n \sin \varphi_{in}) \\ A_{21} &= (-I_p \sin \varphi_{ip} + I_n \sin \varphi_{in}) \\ A_{22} &= (I_p \cos \varphi_{ip} + I_n \cos \varphi_{in}) \end{aligned} \quad (D1.6)$$

Likewise the zero sequence current is given by:

$$\begin{aligned}
 \begin{bmatrix} P_{Ca}^o \\ P_{Cb}^o \\ P_{Cc}^o \end{bmatrix} &= \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} P_{Cab}^o \\ P_{Cbc}^o \\ P_{Cca}^o \end{bmatrix} \\
 &= \frac{\sqrt{3}}{4} \left( \begin{bmatrix} V_p(\sqrt{3} \cos \varphi_{vp} - \sin \varphi_{vp}) & V_p(\sqrt{3} \sin \varphi_{vp} + \cos \varphi_{vp}) \\ V_p(-\sqrt{3} \sin \varphi_{vp} - \cos \varphi_{vp}) & V_p(\sqrt{3} \cos \varphi_{vp} - \sin \varphi_{vp}) \end{bmatrix} \right. \\
 &\quad \left. + \begin{bmatrix} V_n(-\sqrt{3} \cos \varphi_{vn} + \sin \varphi_{vn}) & V_n(\sqrt{3} \sin \varphi_{vn} + \cos \varphi_{vn}) \\ V_n(\sqrt{3} \sin \varphi_{vn} + \cos \varphi_{vn}) & V_n(\sqrt{3} \cos \varphi_{vn} - \sin \varphi_{vn}) \end{bmatrix} \right) \begin{bmatrix} I_o \cos \varphi_o \\ I_o \sin \varphi_o \end{bmatrix} \\
 &= \frac{\sqrt{3}}{4} \left( \begin{bmatrix} (\sqrt{3}(V_p \cos \varphi_{vp} - V_n \cos \varphi_{vn}) & (V_p \cos \varphi_{vp} + V_n \cos \varphi_{vn}) \\ + (-V_p \sin \varphi_{vp} + V_n \sin \varphi_{vn}) & + \sqrt{3}(V_p \sin \varphi_{vp} + V_n \sin \varphi_{vn}) \end{bmatrix} \right. \\
 &\quad \left. \begin{bmatrix} (-V_p \cos \varphi_{vp} + V_n \cos \varphi_{vn}) & (\sqrt{3}(V_p \cos \varphi_{vp} + V_n \cos \varphi_{vn}) \\ + \sqrt{3}(-V_p \sin \varphi_{vp} + V_n \sin \varphi_{vn}) & -(V_p \sin \varphi_{vp} + V_n \sin \varphi_{vn}) \end{bmatrix} \right) \begin{bmatrix} I_o \cos \varphi_o \\ I_o \sin \varphi_o \end{bmatrix} \\
 &= \frac{\sqrt{3}}{4} \begin{bmatrix} B_{11} & B_{12} \\ B_{21} & B_{22} \end{bmatrix} \begin{bmatrix} I_o \cos \varphi_o \\ I_o \sin \varphi_o \end{bmatrix}
 \end{aligned} \tag{D1.7}$$

$$\begin{aligned}
 B_{11} &= \sqrt{3}(V_p \cos \varphi_{vp} - V_n \cos \varphi_{vn}) + (-V_p \sin \varphi_{vp} + V_n \sin \varphi_{vn}) \\
 B_{12} &= (V_p \cos \varphi_{vp} + V_n \cos \varphi_{vn}) + \sqrt{3}(V_p \sin \varphi_{vp} + V_n \sin \varphi_{vn}) \\
 B_{21} &= (-V_p \cos \varphi_{vp} + V_n \cos \varphi_{vn}) + \sqrt{3}(-V_p \sin \varphi_{vp} + V_n \sin \varphi_{vn}) \\
 B_{22} &= \sqrt{3}(V_p \cos \varphi_{vp} + V_n \cos \varphi_{vn}) - (V_p \sin \varphi_{vp} + V_n \sin \varphi_{vn})
 \end{aligned} \tag{D1.8}$$

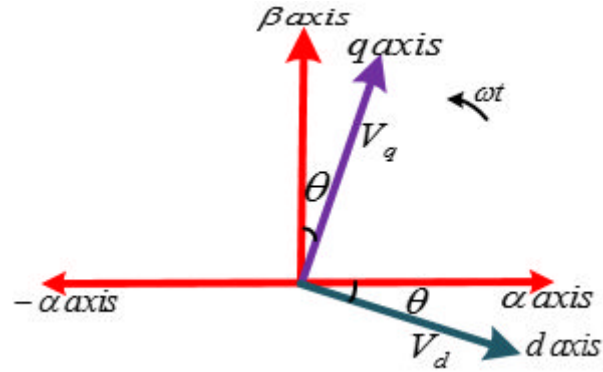
The zero sequence voltage and current can then be expressed as:

$$\begin{bmatrix} V_o \cos \varphi_o \\ V_o \sin \varphi_o \end{bmatrix} = \frac{2}{I_p^2 - I_n^2} \begin{bmatrix} A_{22} & -A_{12} \\ -A_{21} & A_{11} \end{bmatrix} \begin{bmatrix} P_{Ca}^o \\ P_{Cb}^o \end{bmatrix} \tag{D1.9}$$

$$\begin{bmatrix} I_o \cos \varphi_o \\ I_o \sin \varphi_o \end{bmatrix} = \frac{1}{\sqrt{3}(V_p^2 - V_n^2)} \begin{bmatrix} B_{22} & -B_{12} \\ -B_{21} & B_{11} \end{bmatrix} \begin{bmatrix} P_{Ca}^o \\ P_{Cb}^o \end{bmatrix} \tag{D1.10}$$



## D2: Positive and Negative Sequence Decoupling Operator Derivation



### Park's Transformation

Figure above shows a voltage vector in **d-q** reference frame. The phase angle  $\theta$  is the displacement or phase shift between this voltage vector and the synchronous reference frame and based on the arrow indicated direction of rotation it is a lagging phase angle. The voltage vector in  **$\alpha$ - $\beta$**  and  **$d$ - $q$**  forms could be written as complex quantities  $V_\alpha + jV_\beta$  and  $V_d + jV_q$  respectively.

Assuming unity magnitude we have;

$\vec{V}_\alpha^+ = \sin \omega t$  and  $\vec{V}_\beta^+ = \cos \omega t$  then Park's transformation matrix for positive sequence voltage components can be re-written as;

$$\begin{bmatrix} V_d^+ \\ V_q^+ \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos \theta & -\sin \theta \\ \sin \theta & \cos \theta \end{bmatrix} \begin{bmatrix} \sin \omega t \\ \cos \omega t \end{bmatrix} \quad (D2.1)$$

Neglecting the  $\sqrt{\frac{2}{3}}$  normalising factor

$$\begin{bmatrix} V_d^+ \\ V_q^+ \end{bmatrix} = \begin{bmatrix} \cos \theta & -\sin \theta \\ \sin \theta & \cos \theta \end{bmatrix} \begin{bmatrix} \sin \omega t \\ \cos \omega t \end{bmatrix} = \begin{bmatrix} \sin(\omega t - \theta) \\ \cos(\omega t - \theta) \end{bmatrix} \quad (D2.2)$$

The park's transformation can be expressed in term of an operator  $e^{j\theta}$

$$V_d^+ + jV_q^+ = [\text{operator}] \times (V_\alpha^+ + jV_\beta^+) \quad (D2.3)$$

Solving for [operator] in (D.3) yields;

$$\begin{aligned} [\text{operator}] &= \frac{V_d^+ + jV_q^+}{V_\alpha^+ + jV_\beta^+} = \frac{\sin(\omega t - \theta) + j \cos(\omega t - \theta)}{\sin \omega t + j \cos \omega t} \\ &= (\sin(\omega t - \theta) + j \cos(\omega t - \theta))(\sin \omega t - j \cos \omega t) \\ &= \cos \theta + j \sin \theta = e^{j\theta} \end{aligned} \quad (D2.4)$$

Therefore, the relationship between positive sequence  **$d$ - $q$**  and  **$\alpha$ - $\beta$**  can be expressed as;

$$V_d^+ + jV_q^+ = e^{j\theta} \times (V_\alpha^+ + jV_\beta^+) \quad (D2.5)$$

This is only valid for positive sequence component of the **d-q** vector. The negative sequence component of the **d-q** vector rotates in the opposite direction to the positive sequence components. For this reason, the direction of the park's transformation must be reversed.

$$\begin{bmatrix} V_d^- \\ V_q^- \end{bmatrix} = \begin{bmatrix} \cos \theta & \sin \theta \\ -\sin \theta & \cos \theta \end{bmatrix} \begin{bmatrix} \sin(-\omega t) \\ \cos(-\omega t) \end{bmatrix} = \begin{bmatrix} \sin(-\omega t + \theta) \\ \cos(-\omega t + \theta) \end{bmatrix} \quad (D2.6)$$

The park's transformation can be expressed in term of an operator  $e^{j\theta}$

$$V_d^- + jV_q^- = [\text{operator}] \times (V_\alpha^- + jV_\beta^-) \quad (D2.7)$$

Solving for [operator] in (D.7) yields;

$$\begin{aligned} [\text{operator}] &= \frac{V_d^- + jV_q^-}{V_\alpha^- + jV_\beta^-} = \frac{\sin(-\omega t + \theta) + j \cos(-\omega t + \theta)}{\sin(-\omega t) + j \cos(-\omega t)} \\ &= (\sin(-\omega t + \theta) + j \cos(-\omega t + \theta))(\sin(-\omega t) - j \cos(-\omega t)) \\ &= \cos \theta - j \sin \theta = e^{-j\theta} \end{aligned} \quad (D2.8)$$

Therefore, the relationship between negative sequence **d-q** and  **$\alpha$ - $\beta$**  can be expressed as;

$$V_d^- + jV_q^- = e^{-j\theta} \times (V_\alpha^- + jV_\beta^-) \quad (D2.9)$$

### D3: Converter Voltage transformation from abc to d-q

The relationship between the converter STATCOM and PCC is defined as;

$$V_{PCC(abc)} = V_{C(abc)} + i_{C(abc)} R_f + L_f \frac{di_{C(abc)}}{dt} \quad (D3.1)$$

Where  $R_f$  and  $L_f$  are the filtering resistance and inductance coupling the converter to PCC.

Transforming from stationary **abc** into  **$\alpha$ - $\beta$**  positive and negative sequence reference frames, the voltage drop across the filter is a function of the converter current. The voltage across the filter can be calculated in  **$\alpha$ - $\beta$**  reference frame using conventional circuit theory along with the equations for the drop across resistors and inductors as function of the current flowing through them as;

$$\begin{aligned} V_{f(\alpha\beta)}^+ &= i_{C(\alpha\beta)}^+ R_f + L_f \frac{di_{C(\alpha\beta)}^+}{dt} \\ V_{f(\alpha\beta)}^- &= i_{C(\alpha\beta)}^- R_f + L_f \frac{di_{C(\alpha\beta)}^-}{dt} \end{aligned} \quad (D3.2)$$

Transforming from  **$\alpha$ - $\beta$**  voltage and current vectors into rotating **d-q** reference frame vectors;

$$e^{-j\theta} V_{f(dq)}^+ = e^{-j\theta} i_{C(dq)}^+ R_f + L_f \frac{de^{-j\theta} i_{C(dq)}^+}{dt} \quad (D3.3)$$

$$V_{f(dq)}^+ = i_{C(dq)}^+ R_f + e^{j\theta} L_f \frac{de^{-j\theta} i_{C(dq)}^+}{dt}$$

$$e^{j\theta} V_{f(dq)}^- = e^{j\theta} i_{C(dq)}^- R_f + L_f \frac{de^{j\theta} i_{C(dq)}^-}{dt} \quad (D3.4)$$

$$V_{f(dq)}^- = i_{C(dq)}^- R_f + e^{-j\theta} L_f \frac{de^{j\theta} i_{C(dq)}^-}{dt}$$

The derivative terms  $e^{j\theta} L_f \frac{de^{-j\theta} i_{C(dq)}^+}{dt}$  and  $e^{-j\theta} L_f \frac{de^{j\theta} i_{C(dq)}^-}{dt}$  can be simplified using product rule,

Recall  $\frac{d}{dt}(v.u) = v \frac{du}{dt} + u \frac{dv}{dt}$  and  $\theta = \omega t$

for positive sequence  $v = i_{cdq}^+$ ,  $u = e^{-j\omega t}$ ,  $\frac{dv}{dt} = \frac{di_{cdq}^+}{dt}$ ,  $\frac{du}{dt} = -j\omega e^{-j\omega t}$

$$(D3.5)$$

therefore,  $\frac{de^{-j\omega t} i_{cdq}^+}{dt} = -j\omega e^{-j\omega t} i_{cdq}^+ + e^{-j\omega t} \frac{di_{cdq}^+}{dt}$

for negative sequence  $v = i_{cdq}^-$ ,  $u = e^{j\omega t}$ ,  $\frac{dv}{dt} = \frac{di_{cdq}^-}{dt}$ ,  $\frac{du}{dt} = j\omega e^{j\omega t}$

$$(D3.6)$$

therefore,  $\frac{de^{j\omega t} i_{cdq}^-}{dt} = j\omega e^{j\omega t} i_{cdq}^- + e^{j\omega t} \frac{di_{cdq}^-}{dt}$

Substituting (D3.5) and (D3.6) into (D3.3) and (D3.4) respectively, gives;

$$V_{Cdq}^+ = i_{Cdq}^+ R_f + L_f \frac{di_{Cdq}^+}{dt} - j\omega L_f i_{Cdq}^+ \quad (D3.7)$$

$$V_{Cdq}^- = i_{Cdq}^- R_f + L_f \frac{di_{Cdq}^-}{dt} + j\omega L_f i_{Cdq}^-$$

The definition of voltage and current vectors are given as;

$$v_{fdq}^+ = v_{fd}^+ + v_{fq}^+; i_{fdq}^+ = i_{cd}^+ + i_{cq}^+; v_{fdq}^- = v_{fd}^- + v_{fq}^-; i_{fdq}^- = i_{cd}^- + i_{cq}^- \quad (D3.8)$$

The converter voltage is expressed in terms of both PCC voltage and voltage drop across converter filter in **d-q** frames as;

$$\begin{aligned}
 V_{Cd}^+ &= V_{dPCC}^+ - i_{Cd}^+ R_f - L_f \frac{di_{Cd}^+}{dt} - \omega L_f i_{Cq}^+ \\
 V_{Cq}^+ &= V_{qPCC}^+ - i_{Cq}^+ R_f - L_f \frac{di_{Cq}^+}{dt} + \omega L_f i_{Cd}^+ \\
 V_{Cd}^- &= V_{dPCC}^- - i_{Cd}^- R_f - L_f \frac{di_{Cd}^-}{dt} + \omega L_f i_{Cq}^- \\
 V_{Cq}^- &= V_{qPCC}^- - i_{Cq}^- R_f - L_f \frac{di_{Cq}^-}{dt} - \omega L_f i_{Cd}^-
 \end{aligned} \tag{D3.9}$$

The equation above is used in calculating the appropriate converter voltages to generate the desired compensation currents.

#### D4:Zero sequence Component Simplification for Unbalanced Load Analysis

The three phase zero sequence active powers across each cluster of the SSBC and SDBC-MMCC are expressed as;

$$\begin{aligned}
 P_{Ca}^o &= P_{Ca} + \frac{1}{4} (2V_p I_n \cos(\varphi_{vp} + \varphi_{in})) \\
 P_{Cb}^o &= P_{Cb} - \frac{1}{4} (V_p I_n \cos(\varphi_{vp} + \varphi_{in}) + \sqrt{3} V_p I_n \sin(\varphi_{vp} + \varphi_{in})) \\
 P_{Cc}^o &= P_{Cc} - \frac{1}{4} (V_p I_n \cos(\varphi_{vp} + \varphi_{in}) - \sqrt{3} V_p I_n \sin(\varphi_{vp} + \varphi_{in}))
 \end{aligned} \tag{D4.1}$$

$$\begin{aligned}
 P_{Cab}^o &= P_{Cab} - \frac{1}{4} (-V_p I_n \cos(\varphi_{vp} + \varphi_{in}) + \sqrt{3} V_p I_n \sin(\varphi_{vp} + \varphi_{in})) \\
 P_{Cbc}^o &= P_{Cbc} - \frac{1}{4} (2V_p I_n \cos(\varphi_{vp} + \varphi_{in})) \\
 P_{Cca}^o &= P_{Cca} - \frac{1}{4} (-V_p I_n \cos(\varphi_{vp} + \varphi_{in}) - \sqrt{3} V_p I_n \sin(\varphi_{vp} + \varphi_{in}))
 \end{aligned} \tag{D4.2}$$

The positive sequence PCC voltage phase angle is set as reference; therefore  $\varphi_{vp}=0$ . Equation (D4.1) and (D4.2) are simplified as;

$$\begin{aligned}
 P_{Ca}^o &= P_{Ca} + \frac{1}{4} (2V_p I_n \cos(\varphi_{in})) \\
 P_{Cb}^o &= P_{Cb} - \frac{1}{4} (V_p I_n \cos(\varphi_{in}) + \sqrt{3} V_p I_n \sin(\varphi_{in})) \\
 P_{Cc}^o &= P_{Cc} - \frac{1}{4} (V_p I_n \cos(\varphi_{in}) - \sqrt{3} V_p I_n \sin(\varphi_{in}))
 \end{aligned} \tag{D4.3}$$

$$\begin{aligned}
 P_{Cab}^o &= P_{Cab} - \frac{1}{4} \left( -V_p I_n \cos(\varphi_{in}) + \sqrt{3} V_p I_n \sin(\varphi_{in}) \right) \\
 P_{Cbc}^o &= P_{Cbc} - \frac{1}{4} \left( 2V_p I_n \cos(\varphi_{in}) \right) \\
 P_{Cca}^o &= P_{Cca} - \frac{1}{4} \left( -V_p I_n \cos(\varphi_{in}) - \sqrt{3} V_p I_n \sin(\varphi_{in}) \right)
 \end{aligned} \tag{D4.4}$$

(D4.3) and (D4.4) are transformed into  $\alpha$ - $\beta$  cluster power forms as;

$$\begin{aligned}
 \begin{bmatrix} P_{C\alpha}^o \\ P_{C\beta}^o \end{bmatrix} &= \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} P_{Ca}^o \\ P_{Cb}^o \\ P_{Cc}^o \end{bmatrix} \\
 &= \frac{2}{3} \begin{bmatrix} P_{Ca} - \frac{1}{2}(P_{Cb} + P_{Cc}) + \frac{3}{4}V_p I_n \cos(\varphi_{in}) \\ \frac{\sqrt{3}}{2}(P_{Cc} - P_{Cb}) + \frac{3}{4}V_p I_n \sin(\varphi_{in}) \end{bmatrix}
 \end{aligned} \tag{D4.5}$$

$$\begin{aligned}
 \begin{bmatrix} P_{C\alpha}^o \\ P_{C\beta}^o \end{bmatrix} &= \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} P_{Cab}^o \\ P_{Cbc}^o \\ P_{Cca}^o \end{bmatrix} \\
 &= \frac{2}{3} \begin{bmatrix} P_{Cab} - \frac{1}{2}(P_{Cbc} + P_{Cca}) + \frac{3}{8}V_p I_n \cos(\varphi_{in}) - \frac{3\sqrt{3}}{8}V_p I_n \sin(\varphi_{in}) \\ \frac{\sqrt{3}}{2}(P_{Cca} - P_{Cbc}) + \frac{3\sqrt{3}}{8}V_p I_n \cos(\varphi_{in}) + \frac{3}{8}V_p I_n \sin(\varphi_{in}) \end{bmatrix}
 \end{aligned} \tag{D4.6}$$

Assuming there are no losses in the converters,  $P_{Ca} = P_{Cb} = P_{Cc}$   $P_{Cab} = P_{Cbc} = P_{Cca} = 0$ , (D4.5) and (D4.6) become;

$$\begin{bmatrix} P_{C\alpha}^o \\ P_{C\beta}^o \end{bmatrix} = \frac{1}{2} \begin{bmatrix} V_p I_n \cos(\varphi_{in}) \\ V_p I_n \sin(\varphi_{in}) \end{bmatrix} \tag{D4.7}$$

$$\begin{bmatrix} P_{C\alpha}^o \\ P_{C\beta}^o \end{bmatrix} = \frac{1}{4} \begin{bmatrix} V_p I_n (\cos \varphi_{in} - \sqrt{3} \sin \varphi_{in}) \\ V_p I_n (\sqrt{3} \cos \varphi_{in} + \sin \varphi_{in}) \end{bmatrix} \tag{D4.8}$$

Putting (D4.7) into (D1.5) and (D4.8) into (D1.6);

$$\begin{aligned}
 \frac{1}{2} \begin{bmatrix} V_p I_n \cos(\varphi_{in}) \\ V_p I_n \sin(\varphi_{in}) \end{bmatrix} &= \frac{1}{2} \begin{bmatrix} I_p \cos \varphi_{ip} - I_n \cos \varphi_{in} & I_p \sin \varphi_{ip} + I_n \sin \varphi_{in} \\ -I_p \sin \varphi_{ip} + I_n \sin \varphi_{in} & I_p \cos \varphi_{ip} + I_n \cos \varphi_{in} \end{bmatrix} \begin{bmatrix} V_o \cos \varphi_o \\ V_o \sin \varphi_o \end{bmatrix} \\
 \begin{bmatrix} V_o \cos \varphi_o \\ V_o \sin \varphi_o \end{bmatrix} &= \frac{1}{4} \begin{bmatrix} V_p I_n \cos(\varphi_{in}) \\ V_p I_n \sin(\varphi_{in}) \end{bmatrix} \begin{bmatrix} I_p \cos \varphi_{ip} - I_n \cos \varphi_{in} & I_p \sin \varphi_{ip} + I_n \sin \varphi_{in} \\ -I_p \sin \varphi_{ip} + I_n \sin \varphi_{in} & I_p \cos \varphi_{ip} + I_n \cos \varphi_{in} \end{bmatrix}^{-1} \\
 &= \frac{V_p I_n}{I_p^2 - I_n^2} \begin{bmatrix} I_p (\cos \varphi_{ip} \cos \varphi_{in} - \sin \varphi_{ip} \sin \varphi_{in}) + I_n (\cos^2 \varphi_{in} - \sin^2 \varphi_{in}) \\ I_p (\sin \varphi_{ip} \cos \varphi_{in} + \cos \varphi_{ip} \sin \varphi_{in}) - 2I_n \sin \varphi_{in} \cos \varphi_{in} \end{bmatrix} \\
 &= \frac{V_p I_n}{I_p^2 - I_n^2} \begin{bmatrix} I_p \cos(\varphi_{ip} + \varphi_{in}) + I_n \cos 2\varphi_{in} \\ I_p \sin(\varphi_{ip} + \varphi_{in}) - I_n \sin 2\varphi_{in} \end{bmatrix}
 \end{aligned} \tag{D4.9}$$

$$\begin{aligned}
 \frac{1}{4} \begin{bmatrix} V_p I_n (\cos \varphi_{in} - \sqrt{3} \sin \varphi_{in}) \\ V_p I_n (\sqrt{3} \cos \varphi_{in} + \sin \varphi_{in}) \end{bmatrix} &= \frac{\sqrt{3}}{4} \begin{bmatrix} \sqrt{3} V_p \cos \varphi_{vp} & V_p \cos \varphi_{vp} \\ -V_p \cos \varphi_{vp} & \sqrt{3} V_p \cos \varphi_{vp} \end{bmatrix} \begin{bmatrix} I_o \cos \varphi_o \\ I_o \sin \varphi_o \end{bmatrix} \\
 \begin{bmatrix} I_o \cos \varphi_o \\ I_o \sin \varphi_o \end{bmatrix} &= \frac{1}{\sqrt{3}} \begin{bmatrix} \sqrt{3} V_p & V_p \\ -V_p & \sqrt{3} V_p \end{bmatrix}^{-1} \begin{bmatrix} V_p I_n (\cos \varphi_{in} - \sqrt{3} \sin \varphi_{in}) \\ V_p I_n (\sqrt{3} \cos \varphi_{in} + \sin \varphi_{in}) \end{bmatrix} \\
 &= \frac{V_p^2 I_n}{4\sqrt{3} V_p^2} \begin{bmatrix} (\sqrt{3} \cos \varphi_{in} - 3 \sin \varphi_{in} - \sqrt{3} \cos \varphi_{in} - \sin \varphi_{in}) \\ (\cos \varphi_{in} - \sqrt{3} \sin \varphi_{in} + 3 \cos \varphi_{in} + \sqrt{3} \sin \varphi_{in}) \end{bmatrix} \\
 &= \frac{I_n}{\sqrt{3}} \begin{bmatrix} -\sin \varphi_{in} \\ \cos \varphi_{in} \end{bmatrix}
 \end{aligned} \tag{D4.10}$$

The zero sequence voltage and current magnitudes and phase angles are:

$$\begin{aligned}
 V_o &= \frac{V_p I_n}{I_p^2 - I_n^2} \sqrt{\left( I_p^2 (\cos^2(\varphi_{ip} + \varphi_{in}) + \sin^2(\varphi_{ip} + \varphi_{in})) + I_n^2 (\cos^2(2\varphi_{in}) + \sin^2(2\varphi_{in})) \right. \\
 &\quad \left. + 2I_p I_n (\cos(\varphi_{ip} + \varphi_{in}) \cos 2\varphi_{in} - \sin(\varphi_{ip} + \varphi_{in}) \sin 2\varphi_{in}) \right)} \\
 &= \frac{V_p I_n}{I_p^2 - I_n^2} \sqrt{(I_p^2 + I_n^2 + 2I_p I_n \cos(\varphi_{ip} + 3\varphi_{in}))} \\
 \varphi_o &= \arctan \left( \frac{I_p \sin(\varphi_{ip} + \varphi_{in}) - I_n \sin 2\varphi_{in}}{I_p \cos(\varphi_{ip} + \varphi_{in}) + I_n \cos 2\varphi_{in}} \right)
 \end{aligned} \tag{D4.11}$$

$$\begin{aligned}
 I_o &= \frac{I_n}{\sqrt{3}} \sqrt{\cos^2 \varphi_{in} + \sin^2 \varphi_{in}} \\
 &= \frac{I_n}{\sqrt{3}} \\
 \varphi_o &= \arctan \left( -\frac{\cos \varphi_{in}}{\sin \varphi_{in}} \right) \\
 &= \arctan(-\cot \varphi_{in}) \\
 &= 90^\circ + \varphi_{in}
 \end{aligned} \tag{D4.12}$$