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Contributing Towards Improved Communication Systems for Future Cellular Networks

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Abstract

The rapid growth of wireless communications and upcoming requirements of 5G networks are driving interest in the areas from wireless transceivers to sensor nodes. One of the most vital components of the wireless transmitter is the radio frequency power amplifier. A large-signal device model of the transistor is an essential part of the power amplifier design process. Despite the significant developments in large-signal modelling, the models for commercially available devices from the manufacturers are still under continuous development and often lack accuracy.

One of the main objectives of this thesis is the validation and extension of an analytic approach as an alternative to conventional large-signal modelling for power amplifier designing.

The first contribution is the derivation of new analytical expressions based on the equivalent circuit model, including the extrinsic parasitic elements introduced by the package, to calculate the optimum source and load impedances and to predict the performance of a radio frequency power amplifier. These expressions allow to evaluate the effects of a package on the optimum impedance values and performance.

The second contribution is establishing the accuracy of the analytic approach. Harmonic balance simulation is used as the first benchmark to evaluate the method at various bias points and frequencies. The validity of the analytic approach is demonstrated at a frequency of 3.25 GHz for gallium nitride based high power devices with measurement of prototype radio frequency power amplifier designed for the impedance values obtained from the analytic expressions.

The third contribution is extending the analytic approach to determine the optimum impedance values for different criteria of maximum gain, linearity and efficiency. The analytic expressions are utilized to gain an understanding of the relationship among the device performance, the elements of devices and package models and I-V characteristics.

The wireless sensor networks are essential elements for the realization of the Internet of Things. Sensor nodes, which are the fundamental building blocks of these networks, have to be energy efficient and able to produce energy to reduce the maintenance cost and to prolong their lifetime. The second main aim of the thesis is designing and

implementing an ultra-low power autonomous wireless sensor node that harvests the indoor light energy.

The forth contribution of this thesis includes a comprehensive comparison of six different solar cell technologies under a controlled light intensity, carried out to determine the best option for indoor light energy harvesting. The power consumption of the node is reduced by selecting the appropriate hardware and implementing a wake-up receiver to reduce the active and idle mode currents. The low power consumption coupled with light energy harvesting significantly prolong the operating lifetime of the node.

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Chapter 1

Introduction

1.1 Background

Human history has come a long way since the oldest forms of wireless communications like shouts, jungle drums or smoke signals. However, the wireless communication as we know today started with the prediction of the existence of electromagnetic waves by James Clerk Maxwell in 1865. In 1887, Heinrich Rudolf Hertz proved this theory by transmitting and receiving radio signal pulses. Soon after their revolutionary work, Nikola Tesla successfully demonstrated transmission of radio waves wirelessly in 1893. In 1898, Guglielmo Marconi made his demonstration of wireless communication from a boat in the English Channel and later in 1901, he successfully transmitted radio signal across the Atlantic Ocean. Although, Tesla was the first to be successful in this venture, Marconi is generally cited as the inventor of radio and was awarded a Nobel Prize in Physics in 1909.

The popularity of radio and television all around the world in the following years led to a wide network of unidirectional wireless communication by 1930s. Eventually, the demand for bidirectional wireless communication emerged. Military applications accelerated the research in the field of mobile wireless communications during and shortly after, the Second World War. In 1946, American Telephone and Telegraph Company's (AT&T) Bell Laboratories installed and commercialized Mobile Telephone Service (MTS) in St. Louis, USA. There was also interesting progress in the area of satellite communications. In 1957, The Union of Soviet Socialist Republics (USSR) put Sputnik 1, the first artificial satellite, into Earth's orbit. It had two radio-transmitters on board working at 20.005 and 40.002 MHz. The United States of America (U.S.A) soon followed USSR by launching their satellite Explorer 1 in 1958. This encouraged the development of satellite communications, which is to this day an important area of wireless communications.

The cellular communications experienced a revitalized interest in the 1970s with the paramount contributions from pioneering companies like Motorola and AT&T. Motorola produced the first handheld phone in 1973. AT&T Bell Labs implemented the idea of hexagonal cells in cellular communications with detailed system plans. These helped in the growth of mobile wireless communication and in the 1980s, the era of cellular communication begun. Since then mobile wireless communications has seen tremendous growth and development. The evolution of global wireless

communications technology can be categorized into different generations as shown in Figure 1.1.

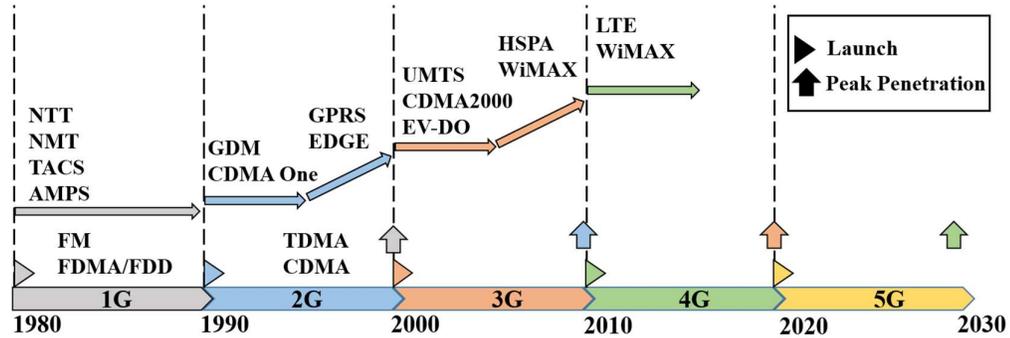


Figure 1.1: Evolution of Wireless Telecommunication/Cellular Network Systems

Nippon Telephone and Telegraph (NTT) installed the first commercial cellular system in Tokyo in 1979, followed by Europe and U.S.A. These first generation (1G) systems provided voice communication through analog radio transmission. To overcome the bad spectral efficiency of analog transmission and to meet the growth of the market, the second-generation (2G) mobile systems with digital networks and modulations schemes were introduced in the early 1990s. The availability of new technologies and the ever-increasing number of mobile users and their demand for more bandwidth and greater speed triggered the industries and researchers to devise the next generation of mobile communication system. In addition, there was a necessity for global network standards. Therefore, the International Telecommunication Union (ITU) was formed to specify the standard for next generation mobile networks with the International Mobile Telecommunications (IMT) requirements. The 3rd and 4th generations of mobile communication systems can accommodate higher user numbers and provide high speed and more bandwidth for high-quality multimedia applications with a remarkable enhancement in performance and Quality of Service (QoS) with the aim of omnipresent access at low cost. Long Term Evolution (LTE)-Advanced standardized by the 3rd Generation Partnership Project (3GPP) and IEEE standard 802.16m (i.e. Wireless MAN-Advanced) are currently the main technologies for 4G. Higher data speed is achieved through secure all-IP based internet protocol and Orthogonal Frequency Division Multiplexing (OFDM) is used as the multiple access technology.

It can be seen from Figure 1.1 that there has been one new technology every 10 years since 1980, however it took nearly 20 years for a technology to reach peak penetration

from its launch. The first commercial LTE networks were launched in 2009, and based on the historical facts it will not reach its peak until around 2030. According to GSMA Intelligence, 60% of world's population will be under LTE coverage by 2020. In addition, as a technology LTE still has a lot of room for development. This raises the question about the necessity of another new generation of mobile technology by 2020. However, the anticipated traffic growth in 2020 and beyond indicates that it will be necessary to adopt new technology with enhanced capabilities with higher bit-rates and wider bandwidth.

According to ITU-R Report M.2370-0 [1.1], there will be a tremendous growth in services such as audio-visual media streaming with new contents like virtual reality and augmented reality, video calls and conference, autonomous driving, cloud computing and storage. The subscriber behaviour is also another driver behind this prediction. From 2007 to 2014, the global subscription numbers of mobile broadband users went up by 764% and in the developing countries the growth was a staggering rate of 3000% due to increasing number of smartphone users. In developing countries, the infrastructure for the fixed internet is poor and improving the conditions is challenging. Therefore, the mobile broadband internet is popular. In addition, it is estimated that by 2050 another 2.5 billion people will be added to urban population and 64% of people will live in cities [1.2]. Currently, majority of the mobile data traffic is generated by the urban population, so it can be safely said that in coming years there will be a need of more upgrade in telecommunication infrastructure and technology to cope with the expected urban population.

Internet of Things (IoT) is presently one of the most talked about ideas in the media and industry. Internet is one of the most significant, dynamic and dominant inventions in all of human history. It has already made an incredible impact on communication, education, business, science, government, and humanity. Although we have observed extraordinary growth of the World Wide Web, but in a sense IoT is essentially the first real evolution of the internet. The IoT is about smart machines not only interacting and communicating with other machines, but also with objects, infrastructures and the environment. In 1999, a group of researchers from seven universities in four continents working in the area of networked Radio Frequency Identification (RFID) at the Auto-ID Labs of Massachusetts Institute of Technology (MIT) with Kevin Ashton first conceived the term "Internet of Things" [1.3]. According to Cisco Internet Business

Solutions Group (ISBG) [1.4], the IoT refers to a situation when more machines are connected to the internet than people. The IoT is predicted to grow to 50 billion devices connected to the internet by 2020. From approximately 0.4 billion machine-to-machine connections in the world right now, the number will be near 7 billion in 2020 and by 2030, it will reach a staggering 97 billion [1.1]. Implementation of technologies such as the RFID tag, short-range wireless communications, real-time localization, mobile internet, ad hoc and wireless sensor networks will make the IoT into a reality. The IoT will allow us to collect more data, and coupled with the ability to process these into information, it is expected to enable people to gather more knowledge and advance even further.

Therefore, the next generation of mobile network systems should be able to handle massive connectivity not only in terms of total number but also performance and efficiency. To meet the demand for increased user number and data traffic; advanced modulation, coding and multiple access schemes, new network architectures and technologies are being explored as some of the potential solutions which may improve the spectral efficiency of future wireless communication systems. All the cellular technologies up to 4G work in the frequency range of 300 MHz to 3 GHz. Popular wireless communication technology Wi-Fi works at 2.4 and 5 GHz. A range of commercial systems for satellite systems, fixed wireless networks and radars is already available above 6 GHz. The wide range of new services and applications and the rapid growth in wireless data traffic in future will require broader and adjacent channel bandwidth. This cannot be fully addressed by currently available bands. This suggests the necessity to study spectrum resources at higher frequency ranges. Continuous academic and industry research and development are ongoing to evaluate the technical feasibility of frequency bands above up to 100 GHz for wireless transmitters and receivers. Commercial 60 GHz multiple gigabit wireless systems (MGWS) products are already available and prototyping more products at various frequencies such as 11, 15, 28, 44, 70 and 80 GHz are in progress. It has to be noted that no single frequency range fulfils all conditions required to install IMT systems particularly in areas with diverse geographic and population density. Therefore, to meet the capacity and coverage requirements of the future, multiple frequency ranges at both low and high bands would be needed.

The device technology used in the wireless communication systems plays a vital role in its performance. Gallium arsenide (GaAs) heterojunction bipolar transistor (HBT) and high electron mobility transistor (HEMT), silicon metal–oxide–semiconductor field-effect transistor (MOSFET) and complementary metal-oxide semiconductor (CMOS), and silicon germanium (SiGe) HBT BiCMOS are technologies for the RF front-end of mobile handsets. GaAs Monolithic Microwave Integrated Circuit (MMIC) technologies currently are leading the industry due to their maturity and advantages over others. However, advance technology like Ultra CMOS Global 1 shows the potential to match the performance of GaAs technology at much lower cost. Indium Phosphide (InP) based HBT and HEMT also show improved performance over GaAs technology and has significant prospect to be used in communication applications up to more than 140 GHz. Silicon LDMOS has been the most commonly used technology in base stations for a long time and now is being replaced by the GaN HEMT devices for 4G. GaN HEMT technology has the potential to dominate the 5G network applications due to its high frequency ability as well as higher power density. Therefore, it has the clear advantage of smaller size. Due to its smaller size, the impedances of these devices are higher and hence designing the matching circuits is simpler which makes them an ideal choice for broadband applications. As a consequence, GaN HEMT technology is bound to be used in mobile devices as well.

1.2 Motivation, Previous Work and Aim of this Thesis

One of the most vital components of the wireless transmitter is the power amplifier (PA). As shown in Figure 1.2, in a typical wireless transmitter, the PA is the last stage before the antenna. It amplifies and produces radio signals with necessary power at the antenna for transmission.

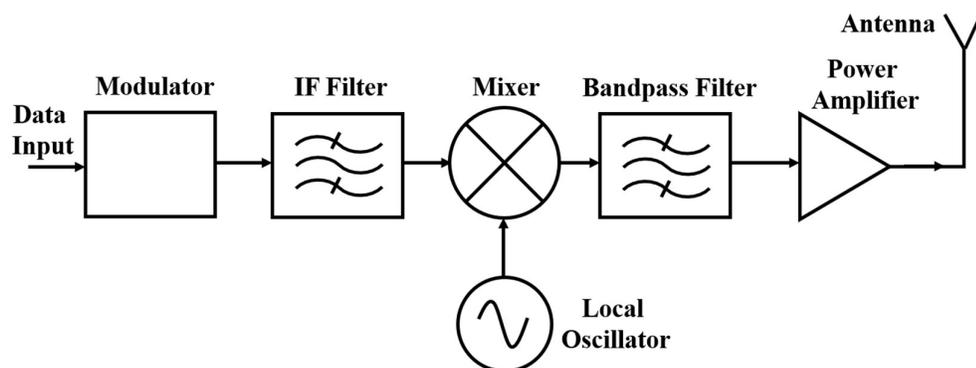


Figure 1.2: A typical wireless transmitter

Since the PA consumes most of the power in a wireless transmitter, its efficiency is the most dominant factor in the total power dissipation in the system which is particularly important for wireless communication systems. At the same time, advanced modulation schemes require PAs to meet strict specification of linearity. Therefore, these systems demand not only substantial power at high frequencies but also linearity and efficiency. The use of the right device and appropriate circuitry is a precondition of designing a power amplifier. The choice of a technology is related to both technical and economic constraints of the PA to be designed. The datasheets, applicable only to a vendor test board design, usually do not specify the device performance under any other bias condition or frequency except that of the specific test board. This makes it difficult to predict the performance from datasheet alone. Conventionally load-pull and source-pull measurement systems or more popularly harmonic balance simulations with the large-signal models of the transistors are used to assess the performance of the devices being considered for the power amplifier. However, the load tuner systems are very expensive, and on the other hand, in a lot of cases the large-signal models for commercially available devices supplied by the vendors are not accurate and sometimes have convergence problems. A lot of times, the choice of device depends upon the experience of the designer and prototyping the amplifier becomes the most reliable approach. However, this trial and error method leads to several iterations in the design cycle which is costly in terms of both time and money. Therefore, a reliable, fast and cost-effective method to predict device performance is useful for PA design.

As an alternative to conventional methods, assessment of RF performance of a transistor for power amplifiers using an analytical approach has been developed. In 1983, Cripps [1.5] first analytically showed the impact of load impedance on load-pull contours and also demonstrated that simple equations could lead to good agreement with experiment. This was further extended by Walker [1.6] to a transistor having input, output and feedback capacitance and source inductance. However, the expressions in [1.6] yielded inaccurate results since it neglected gate resistance and drain conductance for Si RF power MOSFETs. It also considered a linear current generator which limited its accuracy predicting the large-signal performance. Fioravanti et al. [1.7] mainly extended the work in [1.6] to obtain the optimum impedance values by adding more elements in the equivalent model and also included

them in the calculation of gain compression by considering a non-linear current generator for the first time. These analytic expressions were proposed for silicon RF power MOSFETs, and were extended to include the effects of parasitic inductances and pad capacitances by Chevaux et al. [1.8] using a 14-element model for GaN HEMT devices.

The main achievement of this thesis is the experimental validation of this analytical approach to calculate the optimum impedance values and to predict RF performance for high power GaN HEMT devices in a radio frequency power amplifier with considerably good accuracy at frequencies up to 3.25 GHz. The accuracy has been extended to include different bias conditions cross-verified via harmonic balance simulations using exactly the same equivalent model of the transistor. Another extension of novel output of this thesis is the extension of the analytical approach to optimize impedance values for the various criteria of maximum gain, linearity and efficiency, which are most widely used by PA designers. Our results show that the GaN HEMT is relatively immune to different optimization criteria compared to the silicon LDMOS. Using analytic approach, the response can be attributed to higher values of feedback capacitance and output conductance in the GaN HEMT. The effects of nonlinear input capacitance and package parasitic are also taken into account in the analysis. The impacts of uncertainty and errors involved with extraction and measurement are examined in detail.

Another area of wireless communications explored in this thesis is the wireless sensor node. Wireless sensor networks, which are already being used in numerous applications including environment, medical, military, transportation, crisis management, and smart homes. The most fundamental building blocks of a wireless sensor network are sensing nodes with data processing and communication capabilities. Although individual nodes consume a very small amount of power, a large number of nodes need a lot of power to operate. A battery powered wireless sensor node (WSN) is the most feasible, effective and popular solution. However, the WSN is often installed in a hard-to-reach location, so changing the battery regularly can be expensive and problematic. Therefore, in order for the IoT to reach its full potential, research is required to make these sensors and processors to be highly energy efficient and self-sustaining. This means that in addition to very low power

consumption, it must also have the ability to generate electricity by ambient energy harvesting.

Selecting an appropriate microcontroller unit (MCU) and transceiver is crucial in minimizing the power consumption in a WSN. A lot of these WSNs could be deployed indoors where the availability of ambient light might be limited. For example: typically, in an office there is an average of eight hours of light available for five days a week. In order to be operational over an extensive period of time the WSN should manage to harvest enough energy with limited resources. This makes the choice of solar cell and the power management system, which can efficiently acquire and manage the microwatts to milliwatts of power produced by the solar cell, significant. In addition, a wake-up receiver (WuR) can considerably reduce the unnecessary energy consumption in a WSN by allowing to turn off the transceiver during idle time. However, today's commercially available wireless sensor nodes usually do not include any wake-up receiver in the designs. A successful design of autonomous WSN involves careful execution of equally important tasks of choosing the most suitable MCU and transceiver, using the right solar cell for indoor condition, designing an efficient power management system and implementing a WuR.

The second focus of this thesis is therefore an ultra-low power autonomous wireless sensor node with a wake-up receiver to minimize the total power consumption by reducing the idle time current in the WSN. Although at present silicon-based solar cell technologies capture more than 80% market of the total commercially produced solar cells [1.9], technologies such as dye-sensitised and perovskite solar cells offer promising performance for indoor application. Six different solar cells technologies are studied under a controlled light intensity. The results show that considering both performance and cost, the DSSC is the best possible solution for indoor energy harvesting.

1.3 Outline

The thesis is organized into seven chapters.

In **Chapter 2**, the device structures and operating principles of the GaN HEMT and Si LDMOS devices are briefly described and a brief summary of the state-of-the-art commercial RF transistors is present. This chapter then explores some of the basic concepts of a radio frequency power amplifier such as important figures of merit,

classes of operation and optimum impedance values for matching network. Finally, various amplifier architectures to improve the performance are also discussed.

Chapter 3 presents a brief introduction to the types of device modelling. It then briefly compares some of the existing empirical models and describes the state-of-the-art in device modelling reported in the literature.

Chapter 4 primarily focuses on the extraction procedure of the parameter values of the small-signal equivalent circuit model of an RF power transistor. It first describes the methods to measure commercial devices in non-coaxial packages with coaxial equipment. It also explains different calibration methods and approaches to remove the effects of test fixtures from measured S-parameters. New models for two GaN HEMT devices with inaccurate large-signal models are proposed in this chapter. Finally, the relationship between extracted parameter values and device technology is studied.

In **Chapter 5**, new analytical expressions are derived based on a 19-parameter lumped element model that includes the parasitic elements of the package. The accuracy of the analytic approach at different bias conditions and frequencies are first validated via harmonic balance simulation. Prototype amplifiers using the impedance values from analytical approach and vendor model are built and measured to establish the validity and accuracy of our method via experiment. The method is then extended to optimise the impedance values for the different criteria and results are compared for two devices for Si and GaN HEMT and explained in terms of device technologies. The effects of package parasitic on the optimum impedance values and performance are studied using the analytic approach. The influence of nonlinear input capacitance is also analysed. The impacts of extracted parameter values and I-V characteristic on the impedance values and RF performance are studied using the analytic approach. This chapter demonstrates the strength of the analytical approach to be applied for the optimization of the device at both device and amplifier design levels.

In **Chapter 6**, major issues and challenges in wireless sensor technology are discussed. Then the design and implementation of an autonomous WSN, which addresses the issue of limited energy, is described accompanied by a survey of state-of-the-art commercial products for each component. Different solar cell technologies are characterized in a controlled light intensity similar to indoor condition at room

temperature in order to determine the best possible solution for indoor energy harvesting. The charging characteristic of a rechargeable battery is also studied as a function of the open circuit voltage, short-circuit current and harvested power from the solar cells. Finally, the design and implementation of a wake-up receiver is presented.

Finally, the work in this thesis is summarized in **Chapter 7**. Possible continuation of the studies and future work are also recommended.

References

- [1.1] International Telecommunication Union, “IMT traffic estimates for the years 2020 to 2030,” Geneva, Report ITU-R M.2370-0, July, 2015.
- [1.2] United Nations, “World Urbanization Prospects: The 2014 Revision, Highlights”, New York, ST/ESA/SER.A/352, 2014.
- [1.3] M. Friedemann and C. Floerkemeir, “From the Internet of Computers to the Internet of Things,” *From Active Data Management to Event-Based Systems and More*, Springer-Verlag, Berlin, 2010, pp. 242–259.
- [1.4] D. Evans, “The Internet of Things - How the Next Evolution of the Internet is Changing Everything,” CISCO White Paper, April, 2011, pp. 1–11.
- [1.5] S. C. Cripps, “A Theory for the Prediction of GaAs FET Load-Pull Power Contours,” *1983 IEEE MTT-S International Microwave Symposium Digest*, Boston, MA, USA, 1983, pp. 221-223.
- [1.6] J. Walker, “Analytic expressions for the optimum source & load impedance and associated large-signal gain of an RF power transistor,” *2003 IEEE MTT-S International Microwave Symposium Digest*, Philadelphia, PA, USA, 2003, pp. 1725-1728 vol.3.
- [1.7] P. Fioravanti, O. Spulber and M. M. De Souza, “Analytic Large-Signal Modeling of Silicon RF Power MOSFETs,” in *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, no. 5, pp. 829-837, May 2007.
- [1.8] N. Chevaux and M. M. De Souza, “New analytical expressions for the design of linear power amplifier using GaN HEMTs,” *2009 Asia Pacific Microwave Conference*, Singapore, 2009, pp. 1112-1115.

Chapter 1

[1.9] T.M. Razykov, C.S. Ferekides, D. Morel, E. Stefanakos, H.S. Ullal, H.M. Upadhyaya, "Solar photovoltaic electricity: Current status and future prospects," *Solar Energy*, Volume 85, Issue 8, August 2011, Pages 1580-1608.

Chapter 2

Basic Concepts of Radio Frequency Power Amplifier

Abstract

In this chapter, the device structures of silicon-based laterally diffused metal–oxide–semiconductor field-effect transistor (Si LDMOSFET) and gallium nitride based high electron mobility transistor (GaN HEMT), particularly the devices studied in this thesis are described. A brief comparison of state-of-the-art commercial RF transistors shows that Si LDMOS and GaN HEMT are competitive in the frequency range of 2 to 3.5 GHz with transistors from both technologies offering similar output power. Although GaN HEMTs show higher efficiency compared to Si LDMOS devices, the power gain from the latter is higher than the former. Finally, some important figures of merit and different classes of operation and architectures of radio frequency power amplifiers (RF PAs) are discussed.

2.1 Introduction

The radio frequency power amplifier (RF PA), one of the fundamental components of any communication system, is used to amplify an RF signal using DC power before transmission. Many receivers also have a stage of RF amplification to amplify the received signal from the antenna. The most expensive and power consuming component of an RF PA is the transistor.

Currently, a range of RF transistors from various technologies is implemented in wireless communications systems and each technology has its own advantages and limitations. The semiconductor transistor technologies are usually categorized in terms of materials or operation principles. Table 2.1 displays the material properties of some commonly used semiconductors. These materials properties determine the device characteristics and set the fundamental limitation of a technology.

Table 2.1: Material properties of popular semiconductors [2.1], [2.2]

Material Property	Silicon	Gallium Arsenide	4H-Silicon Carbide	Gallium Nitride	Diamond
Bandgap, E_g (EV)	1.12	1.43	3.26	3.45	5.45
Electron Breakdown Field E_{br} (kV/cm)	300	400	2200	2000	10000
Dielectric Constant, ϵ	11.9	13.1	10.1	9	5.5
Electron Mobility, μ ($\text{cm}^2/\text{V}\cdot\text{s}$)	1500	8500	1000	1250	2200
Saturated Electron Drift Velocity, v_{sat} ($\times 10^7$ cm/s)	1	1	2	2.5	2.7
Thermal Conductivity, λ (W/cm.K)	1.5	0.46	4.9	1.3	22
BFOM/BFOM (Si)	1.0	9.6	3.1	24.6	-
JFOM/JFOM (Si)	1.0	2.7	20	27.5	50

Baliga's figure of merit (BFOM) [2.3] is a measure of the on-resistance of a device ($R_{ON} \propto 1/\mu \cdot E_{br}^3$) which indicates the power handling capability.

Johnson's figure of merit (JFOM) [2.4] is a measure of the ultimate high frequency capability or cut-off frequency of the material ($f_T \propto E_{br} \cdot v_{sat} / 2\pi$).

Silicon LDMOS has the advantage of extensive research and incremental development, which lead to low cost and reliable performance which have made it the transistor of choice for a wide variety of RF applications since the late 90's. However, due to low electron mobility and drift velocity, the operation of silicon-based transistors is mostly limited to frequencies below 3 GHz. Gallium arsenide or GaAs transistors are capable of operating at frequencies up to 250 GHz because of the high electron mobility. However, these devices cannot tolerate high voltages, currents and temperature. Therefore, GaAs devices are most widely used for low power applications such as RFPAs for cell phones.

Both gallium nitride (GaN) and silicon carbide (SiC) have similar material properties that indicates comparable performance. The higher thermal conductivity of SiC gives it an advantage of better heat dissipation which is an important property for high power, high temperature performance. Although SiC MESFETs show promising performance for high power microwave devices; GaN HEMTs display higher power densities and higher frequency capabilities [2.5], [2.6]. Diamond clearly exhibits the best theoretical performance, as its figure of merit values are much higher than any other semiconductor. However due to the very high cost involved, it would not be commercially feasible to manufacture diamond-based transistors yet. Therefore, GaN is the ideal choice for high power microwave device [2.1], [2.2], [2.7], [2.8].

Due to their high power capabilities, silicon-based laterally diffused metal–oxide–semiconductor field-effect transistor (Si LDMOSFET) and gallium nitride based high electron mobility transistor (GaN HEMT) device technologies currently are the primary choices for wireless communication infrastructures. Continuous research and improvement have extended the frequency of operation for Si LDMOS up to 4 GHz. For example, the output capacitance, which greatly influences the frequency-dependent RF performance, has been reduced by a factor of two for LDMOS in the last decade by scaling down the physical size of the device [2.9]. As result, there is a competition between these two technologies in the frequency range of 2 to 3.5 GHz, particularly because reliability of GaN devices is still under development.

In this chapter, the basic operation and device structures of SI LDMOS and GaN HEMT are described first and a brief comparison of state-of-the-art commercial RF transistors is presented. The basic concepts and some important figures of merit that

are necessary for designing RF power amplifier are discussed. Finally, classes of operation and architectures of RF PAs are discussed.

2.2 RF Power Transistors

2.2.1 Silicon LDMOS

2.2.1.1 Basic Operation of a MOSFET

The basic operation of an n-type MOSFET is based on the variation of charge concentration of a metal–oxide–semiconductor (MOS) capacitor between the gate contact and in the semiconductor, which are separated by an insulator such as silicon dioxide (SiO_2). As seen in Figure 2.1, there is also an ohmic contact for semiconductor substrate. If a positive voltage (V_{GS}) is applied at the gate (G), for a p-type semiconductor holes are expelled from the oxide–semiconductor interface.

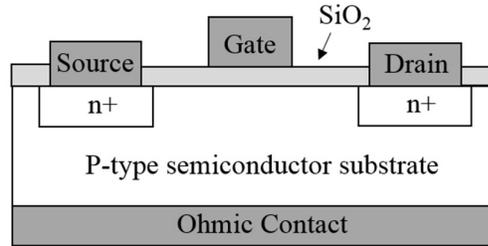


Figure 2.1: Schematic of the cross-section of an n-channel MOSFET.

At a certain applied gate voltage called the threshold voltage (V_{th}), the electron concentration at the SiO_2/Si interface becomes equal to the hole concentration in bulk of p-type semiconductor and an inversion layer is created at the surface of the p-body region and the silicon dioxide layer. The positive voltage at the gate also attracts more electrons from the highly doped n+ diffusion regions. When $V_{GS} > V_{th}$, there is an excess of electrons in the channel and with increasing V_{GS} the carrier concentration in the channel gets higher.

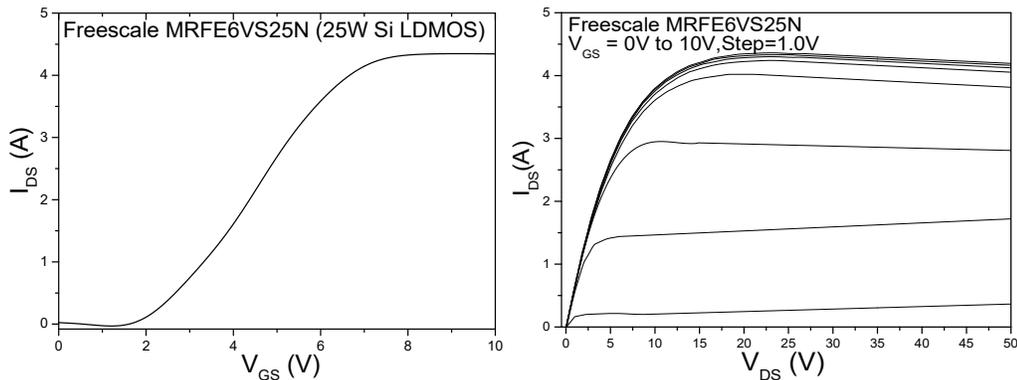


Figure 2.2: Measured I-V characteristic of Freescale MRFE6VS25N, a 25 W silicon LDMOS.

However, the current only starts to flow when a voltage applied between the drain (D) and the source (S) terminals ($V_{GS} > V_{th}$ and $V_{DS} > 0$). From the measured I-V characteristics for Freescale MRFE6VS25N, a 25W silicon LDMOS, in Figure 2.2; it can be noted that the threshold voltage $V_{th} = 1.4$ V. At a certain drain-source voltage, the channel width near drain becomes zero due to the charge depletion near drain contact and after this point, the current fundamentally remains the same and is called saturation current.

2.2.1.2 Device Structure of an LDMOSFET

Figure 2.3 (a) shows the schematic of the device cross-section of a typical n-channel RF LDMOS transistor from Freescale Semiconductor [2.10]. Its simplified form can be seen in Figure 2.3 (b). The Si LDMOS studied in this thesis is Freescale's MRFE6VS25N which a 25 W Si LDMOS transistor.

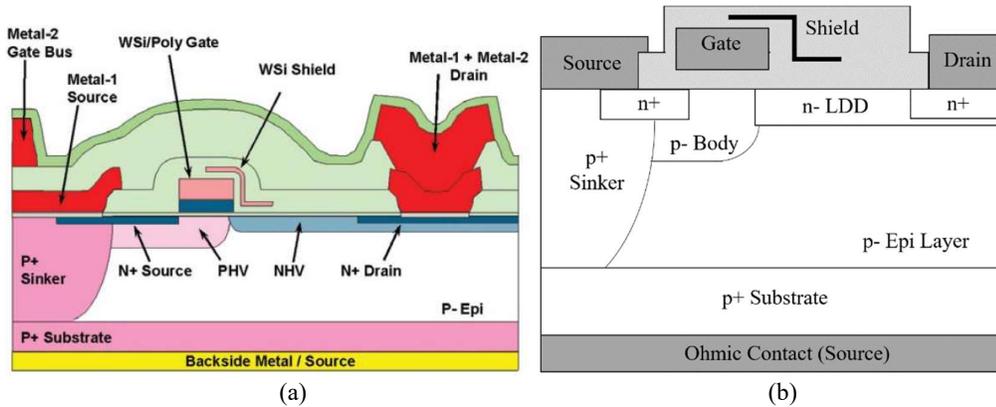


Figure 2.3: (a) Schematic of the cross section of the n-channel LDMOS from Freescale Semiconductor [2.10] and (b) its simplified form.

The n-channel LDMOS transistor is built on a highly doped p+ silicon substrate. A low doped p- epitaxial layer is grown upon the substrate which reduces the drain-to-substrate capacitance and thus helps to increase the efficiency. The gate is made out of a conductor which is insulated from the channel below by layer of silicon dioxide. Tungsten silicide/polysilicon (WSi/Poly) gate is implemented to achieve a low gate access resistance. The WSi shield over the gate is employed to reduce the gate-to-drain feedback capacitance and also to control surface electric fields that allows to achieve improved device performance without compromising the breakdown voltage. Two highly doped n+ diffusion regions, which are opposite type to the body region, form the source and drain of the transistor. The channel length is defined by the low doped p-type body, referred to p-type high voltage (PHV) region, below the gate and the

source regions. The threshold voltage and drain current saturation depend on the dimension on the p-body region and the lateral diffusion of the dopants. At the drain side of the gate, a lightly doped drain (LDD) n- region, also known as n-type high voltage (NHV), is implemented to obtain high breakdown voltage. The stacked drain metal (Metal-1 + Metal-2 Drain in Figure 2.3) is designed to reduce electromigration and thus improve the reliability. The parallel gate bus (Metal-2 Gate Bus in Figure 2.3) is used to reduce the gate resistance. The top metal (Metal-1 Source in Figure 2.3) electrically connects the top source to the bottom source metal via the highly doped p+ sinker and p+ substrate to create a source connected ground plane. This reduces the source inductance and resistance [2.10] in the device which enables high power gain at high frequencies and high on-state breakdown voltages. In addition, it also allows the die to be directly attached onto a thermally and electrically conductive package flange.

2.2.2 AlGaN/GaN HEMT

2.2.2.1 Basic HEMT Operation

The principles of operation in a HEMT are based on the properties of a heterojunction. The heterojunction is formed when a wide band-gap semiconductor material is grown on a relatively narrow band-gap semiconductor material or vice-versa. Due to the difference in their band gaps, also known as band-offsets, band-bending takes place at the interface as shown in Figure 2.4.

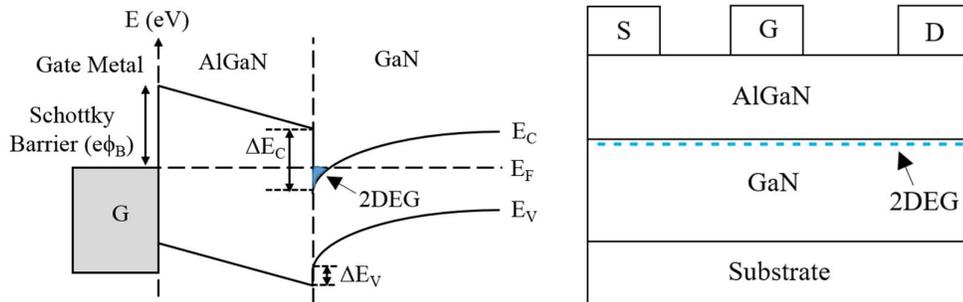


Figure 2.4: AlGaN/GaN band diagram and simplified AlGaN/GaN HEMT Structure.

Near the heterojunction in the upper part of the narrow bandgap semiconductor layer, a triangular quantum well is formed because of the presence of polarization charge at the interface and discontinuity in the conduction band. This quantum well acts as the conducting channel for the HEMT. A lower channel resistance, which improves the device performance, could be attained by increasing the electron mobility and density of the electrons in 2DEG in a HEMT.

The HEMT is a three-terminal device where the current between the drain (D) and source (S) flows through the 2DEG conducting channel and is controlled by the space charge which changes according to the applied voltage at the gate (G) terminal. If the gate voltage is increased in the negative value, the space charge underneath the gate starts to spread and deplete the channel. At some point the channel is totally pinched-off leading to the off state.

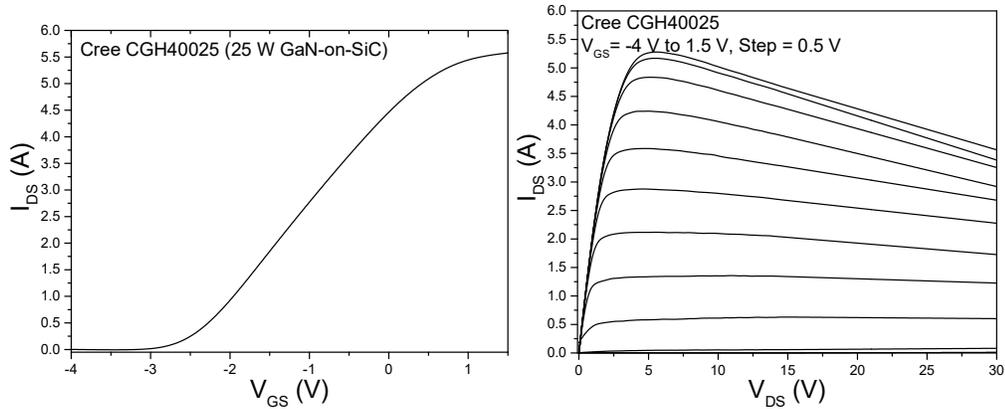


Figure 2.5: Measured I-V characteristics of Cree CGH40025, a 25 W GaN HEMT.

Figure 2.5 shows the measured I-V characteristics of Cree CGH40025, a 25 W GaN HEMT. The pinch-off voltage $V_{\text{pinch-off}}$, often called the threshold voltage V_{th} for HEMT devices, is -3.14 V. The decrease in drain current at high drain and gate voltages is the result of self-heating which has been discussed later.

2.2.2.2 Polarization Effects

The 2DEG in a AlGa_N/Ga_N heterostructure arises due to strong spontaneous and piezoelectric polarization in the crystal. The Ga_N crystal lacks symmetry due to its wurtzite structure and this results in high polarity as the electron charge cloud shifts toward one side of the atom. Therefore, there is a built-in electric field in the crystal which leads to spontaneous polarization (P_{SP}). The electric field and sheet charges in both AlGa_N and Ga_N crystals due to P_{SP} can be seen in Figure 2.6.

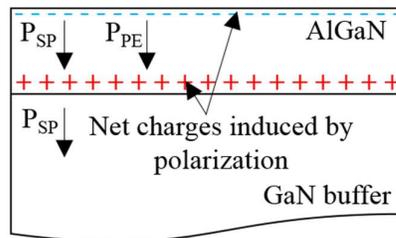


Figure 2.6: Spontaneous (AlGa_N and Ga_N) and piezoelectric (AlGa_N) polarization induced electric field and sheet charges and combined polarization effect in AlGa_N/Ga_N structure.

The AlGaN layer when grown on a GaN buffer layer is strained because of the difference in lattice constant between the two materials. This leads to deformation in the crystal lattice structure and a resulting polarization field. Since these materials have large values of piezoelectric coefficients, the piezoelectric polarization (P_{PE}) is very strong in an AlGaN/GaN heterostructure. Figure 2.6 shows the resulting sheet charge at both faces of the AlGaN layer.

Now if the orientation of the GaN crystal can be arranged in such a way during growth so that the spontaneous and piezoelectric polarizations are in the same direction [2.11], then the polarization field in AlGaN will be higher than that in the GaN buffer layer and due to this disruption in polarization field, there will be large positive sheet charge at the AlGaN/GaN interface. This electric field will increase as the AlGaN layer thickness is increased during the growth process, and after a critical thickness the electric field will be strong enough to create ionized donor states at the surface of the AlGaN layer as electrons move to the AlGaN/GaN interface and accumulate on the side of the lower bandgap GaN buffer layer.

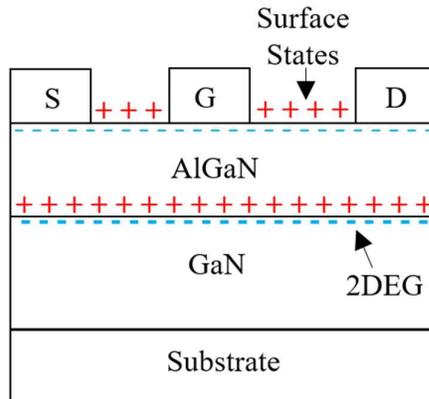


Figure 2.7: Polarization induced surface states and 2DEG in AlGaN/GaN HEMT.

There will be a 2DEG at the interface and positive states due to ionized donors at the surface. These effects allow the AlGaN/GaN heterostructure to form the 2DEG without any intentional doping in the AlGaN layer. The electron concentration in the 2DEG in the hetero-interface can be increased further by inducing more strain which can be accomplished by controlling the fraction of Al mole in the AlGaN barrier layer.

Higher Al fraction in the AlGaN layer increases the piezoelectric polarization and results in higher carrier concentration in the 2DEG. However, when the carrier concentration is higher, the usual low temperature scattering mechanism like alloy disorder scattering in AlGaN/GaN heterostructure becomes prominent even at room

temperature. This along with the interface roughness scattering leads to the decrease in electron mobility in the 2DEG. Both of these issues can be addressed by an AlN spacer layer between the AlGaN and GaN layers [2.12].

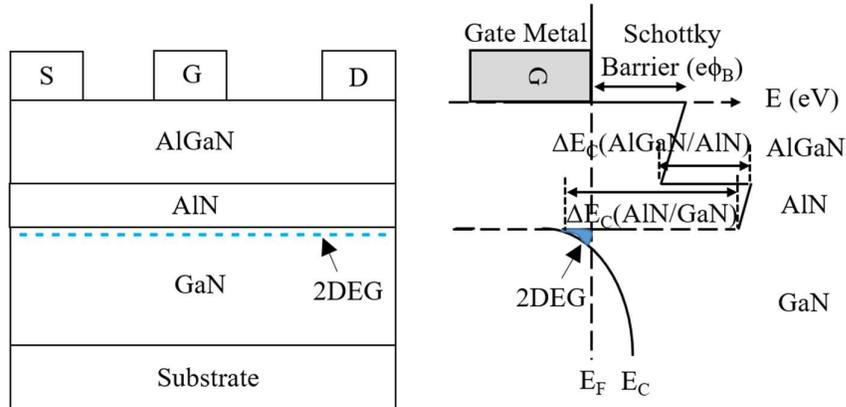


Figure 2.8: Simplified device structure and the band diagram of AlGaN/GaN HEMT with AlN spacer layer.

Higher bandgap of the AlN layer elevates the height of the potential barrier as seen in Figure 2.8; and consequently, the penetration of electron wave function into the AlGaN layer is significantly decreased and so are the interface roughness scatterings. Since AlN is a binary material, there is no alloy scattering. The polarization-induced charge at the AlN/GaN interface due to AlN spacer layer also increases the carrier concentration in 2DEG. As a consequence, this AlN spacer layer greatly increases the conductivity of the 2DEG.

2.2.2.3 Choice of Substrate

Many of the material properties of a device, and consequently its performance and reliability depend on the substrate used and therefore the selection of an appropriate substrate is very important. The major criteria for choosing a substrate are material properties such as lattice constant, thermal expansion coefficient (TEC), surface chemistry, temperature stability, thermal and electrical conductivity. The availability and most importantly the cost of the substrate have to be taken in to account for the commercialization of the device.

The process to grow bulk GaN crystal growth is still in very early stage and there are material properties and economic challenges to overcome before GaN substrates could be used for GaN HEMTs. Therefore, the inaccessibility of GaN substrate has led to the use of different materials as the substrate of choice for the GaN HEMTs.

AlGaIn/GaN heterostructure has been grown on silicon (Si), aluminium nitride (AlN), sapphire, silicon carbide (SiC), diamond substrates. Growth of AlGaIn/GaN on GaN templates [2.13] and ‘SopSiC’ composite substrate of silicon, silicon carbide and silicon dioxide [2.14] have also been reported. It is well known that the high power devices suffer from self-heating at large drain-to-source voltages which is detrimental for device performance and long-term reliability. Therefore, in order to maintain device performance, the generated heat has to be transferred from junction. GaN HEMT on sapphire substrate shows poorer performance compared to silicon substrate [2.15], [2.16] due to almost five times lower thermal conductivity which makes it a poor choice as a substrate for high power GaN HEMT devices for RF application. Diamond, due to its large thermal conductivity, currently has drawn a lot of attention as a substrate for GaN HEMT devices. It has been reported [2.17] that the drain current and transconductance of HEMTs on diamond are much higher than that of GaN HEMTs grown on any other substrate and the rise in temperature with increasing drain-to-source voltage is also lower when compared to any other substrate. At present, all the commercially available GaN HEMTs are grown on either silicon carbide or silicon substrates. A brief comparison of these two substrates is presented in the following section.

Comparison of SiC and Si substrates

Silicon carbide or SiC is presently the primary substrate of choice for GaN HEMTs due its high thermal conductivity and high breakdown voltage. Semi-insulating SiC substrates have very high resistivity which in combination with other material properties makes it an excellent substrate for high power and high frequency devices. However, SiC is produced in small-size wafer such as 50 mm-150 mm in diameter and the usual cost of a 50 mm wafer in 2016 is £314 - £402 [2.18]. As a result, GaN-on-SiC HEMTs are comparatively more expensive.

Silicon substrates on the other hand are low cost. The typical cost of a standard wafer size of 300 mm is £100 - £161 [2.18], which makes it good for commercialization. However due to the lower thermal conductivity of 1.5 W/cm/K in silicon, the resultant heat transfer rate from the device channel in these high power devices is low. As a result, these devices suffer from prominent self-heating compared to the GaN HEMTs on SiC substrate. However, according to Nitronex [2.19], the difference between the thermal conductivity of SiC and Si starts to decrease as the operating temperature starts

to increase and at an operating temperature of 175°C, it is 0.6 W/cm/K. The thermal resistance can be reduced even further by reducing the Si die thickness. By reducing the thickness from 4mil to 2mil, Nitronex has managed to decrease the thermal resistance by 15%.

Table 2.2: Material properties of SiC and Si substrates

Property	SiC	Si
Bandgap (eV)	3.26	1.12
Electric Breakdown Field (kV/cm)	2200	300
Thermal Conductivity (W/cm ² K)	4.9	1.5
Lattice Mismatch with GaN (%)	4	17
Thermal Expansion Coefficient Mismatch (%)	3.2	54

Another major issue with Si substrate is the difficulty to grow good quality GaN on it. As can be seen in Table 2.2, the lattice mismatch of silicon with GaN is 17%, and this leads to a high dislocation density in the GaN layer grown on the Si substrate. This situation is deteriorated further by the 54% mismatch in thermal expansion coefficient (TEC) between GaN and Si. As a result, it is difficult to grow crack-free GaN layers for the HEMT fabrication. In addition, low resistivity silicon substrates result in higher losses at high frequency [2.20]. For example, below 10 GHz, the attenuation loss in 100 Ω-cm silicon substrate is 0.49 dB/mm compared to 0.15 dB/mm in 10000 Ω-cm silicon substrate. The coupling of RF signal with the lossy low resistivity substrate results in lower performance for the device.

By depositing an aluminium nitride (AlN) transition layer on high-resistivity Si substrates, both lattice mismatch and TEC mismatch have been addressed [2.19], [2.21] - [2.23]. The high resistivity silicon substrate overcomes the substrate-induced loss by the low resistivity silicon substrate. Figure 2.9 shows the schematic for the cross-section of the epi layers structure of Nitronex NPTB00025, the 25W GaN HEMT on 10,000 Ω-cm Si substrate [2.19].

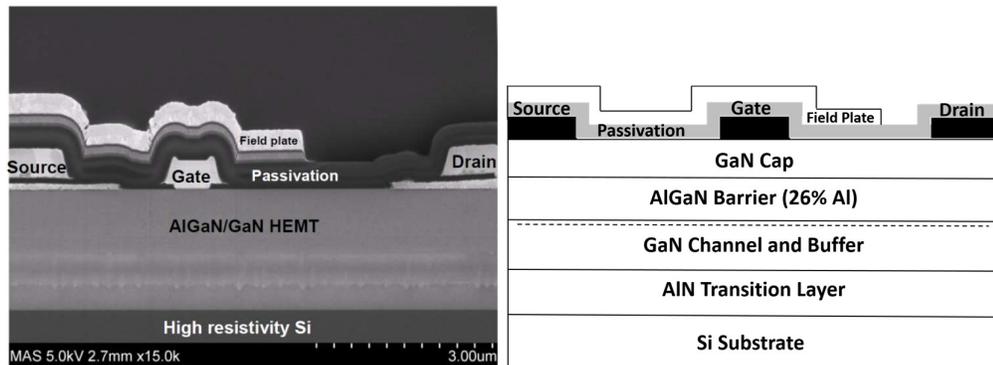


Figure 2.9: Cross-section and simplified schematic of the epi layer structure for 25 W GaN HEMT on Si [2.19].

The stress caused by the lattice mismatch is absorbed by the AlN/Si interface, while the AlN/GaN transition layer reduces the stress due to the TEC mismatch. The AlN layer also provides a highly resistive substrate which allows high frequency operation [2.22].

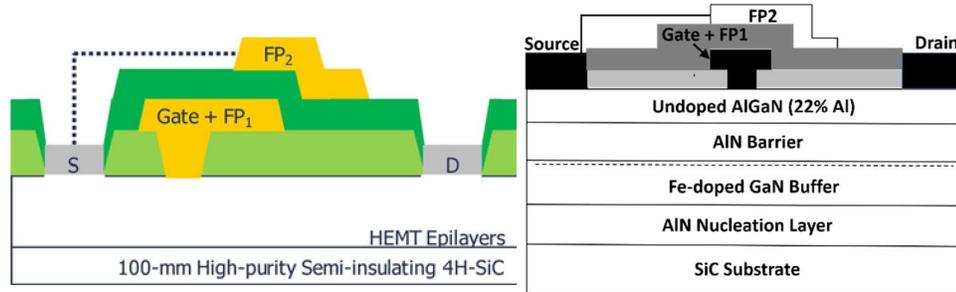


Figure 2.10: Cross-section and simplified schematic of the epi layer structure for 25 W GaN HEMT on SiC [2.24].

Figure 2.10 shows the schematic of the epi layers for Cree CGH40025, the 25 W GaN HEMT on SiC [2.24]. The passivation layers and field plates in both devices help to reduce the impact of surface and buffer traps and increase the breakdown voltage. Other significant differences between these two structures are the Fe-doped GaN buffer layer and the presence of an AlN barrier layer in the Cree CGH40025 structure. The iron-doped GaN buffer layer helps to achieve more stability and higher breakdown voltage as well as high power and high frequency operation [2.25], [2.26]. The Al fraction in the AlGaN barrier of Nitronex NPTB0025 is 26% which is higher than that (22%) of Cree CGH40025.

2.3 State-of-the-art Commercial RF Transistors

Figure 2.11 shows a brief comparison of current state-of-the-art commercially available RF transistors in silicon LDMOS and GaN HEMT technologies. The data have been collected from the product datasheets of six leading manufacturers in 2016.

It can be seen from Figure 2.11 that currently above 3.5 GHz, the GaN HEMT is the only available option for high power RF amplifiers. However, in the frequency range of 2 GHz to 3.5 GHz, silicon LDMOS and GaN HEMT technologies are highly competitive with a lot of transistors available in the market. The transistors from both technologies display similar output power up to 125 Watts.

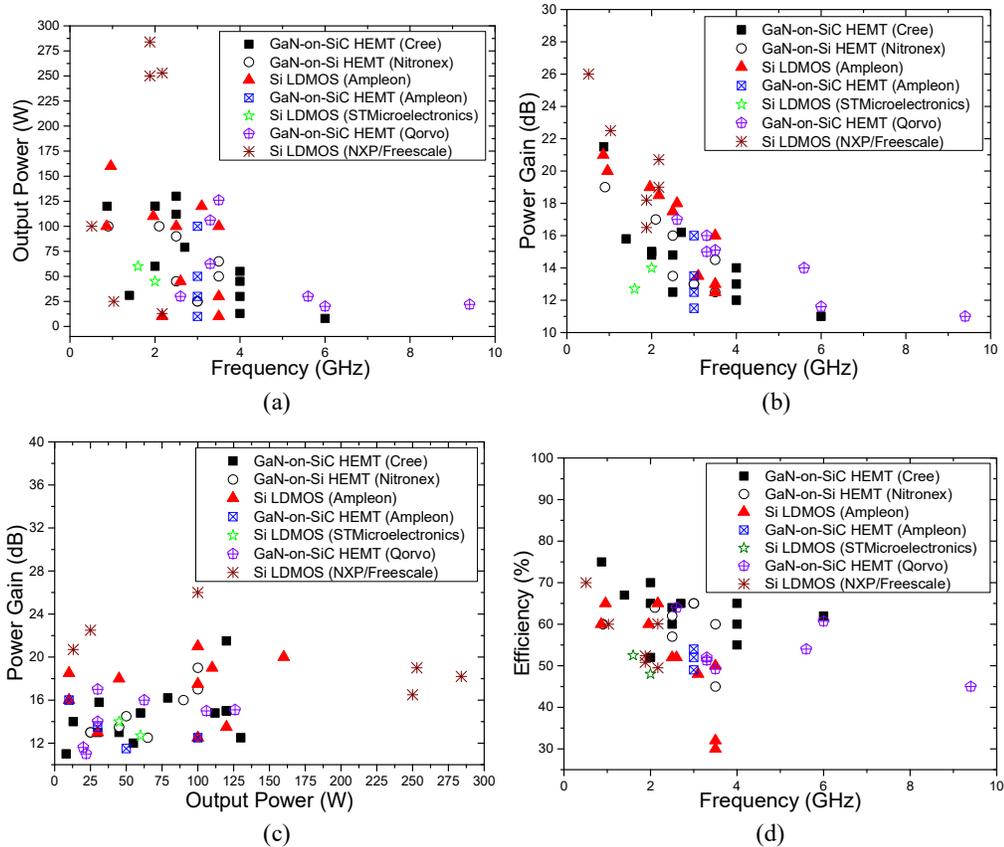


Figure 2.11: A comparison of performance of commercial RF transistors.

Interestingly, it can be observed in Figure 2.11 (b) that power gain from silicon LDMOS devices are higher than GaN HEMT transistor. The GaN HEMT devices still have not achieved the potential power gain based on its material properties, which confirms the lack of maturity of this technology and scope for improvement. Although the values of efficiency of these transistors in RF PAs are not directly comparable in Figure 2.11 (d) because the bias currents are different; however, it can be said that GaN HEMT shows higher efficiency compared to Si LDMOS. Besides specified RF performance, the cost involved is an important criterion in the amplifier design process. The GaN HEMT devices are roughly three to four times more expensive than a silicon LDMOS with the same output power. For example, the unit prices for 25 W transistors from Cree, Nitronex and Freescale are £90.73, £128.55 and £27.65 respectively.

The large output capacitance of the silicon LDMOS reduces the output impedance, and consequently, designing an output matching circuit to standard 50Ω load becomes challenging. High power silicon LDMOS devices operating at higher frequencies (3-4 GHz) are commonly internally matched for a range of frequencies to elevate the low

impedance of the die to a higher value at the package leads. Even the unmatched silicon LDMOS with more than 200 Watts output power LDMOS in Figure 2.11 (a) are optimized for an operating frequency range of 100 MHz. Due to lower dielectric constant and smaller gate periphery than silicon LDMOS, GaN devices have lower output capacitance. As a result, designing the matching networks for GaN GEMTs is more convenient. This also makes GaN HEMT an excellent choice for broadband amplifiers.

Therefore, a designer often faces the challenging task of choosing the most suitable RF transistor considering performance, design challenges and cost. As mentioned in Chapter 1, making a decision based on the information in datasheet is not always possible because in most cases, the RF performance provided in the datasheets by the manufacturers is very limited to particular conditions, which might not be compatible with the intended application. Therefore, an accurate method to predict the device performance is not only essential to reduce the time and cost involved in an RF PA design, but also helpful to a designer for selecting the best transistor for an application within the constraints.

2.4 Power Amplifier

A simplified RF power amplifier circuitry can be seen in Figure 2.12.

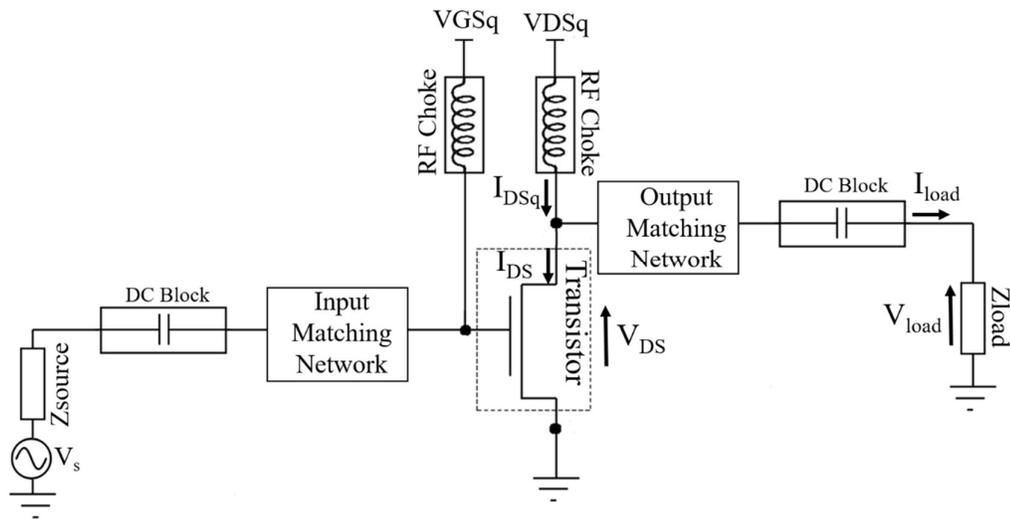


Figure 2.12: Simplified block diagram of a RFPA.

The active device, in this case a FET, is biased at a quiescent drain voltage (V_{DSq}) and quiescent current drain current (I_{DSq}) through RF choke and DC block. A RF choke prevents the RF signals from interfering in the DC biasing network and a DC block

removes the DC components of the RF signal. The input and output matching networks are designed to present the optimum source and load impedances to the transistor to optimize power transfer from the source to the input of the transistor and from the output of the transistor to the load.

The DC bias condition and the design of matching networks depend on the desired performance of the intended application of the amplifier.

2.4.1 Load-line Match and Conjugate Match

In the configuration of a power amplifier shown in Figure 2.12, the relationship between voltages at the output of the transistor is as following:

$$V_{DS} = V_{DSq} + V_{load} \quad (2.1)$$

Here, V_{DS} and V_{load} are the total voltages across the active device and the load, and V_{DSq} is the supply voltage. The total voltages in (2.1) include the DC and AC components. If only the AC or incremental quantities are considered, then it can be observed that $v_{load} = v_{ds}$. This means that by maximizing the RF voltage swing across the device, the voltage swing across the load can also be maximized. However, the output matching network modifies the voltage across the load (V_{load}); therefore, depending on the matching network, the AC voltage v_{load} would be different for the same RF voltage swing v_{ds} across the device. Similarly, the relationship between the currents can be presented as:

$$I_{DS} = I_{DSq} + I_{load} \quad (2.2)$$

Again, the relationship between the incremental quantities $i_{load} = -i_{ds}$ shows that by maximizing the RF drain current, the current in the load can also be maximized. By maximizing both voltage and current swings across the load, the maximum output power from the transistor in an amplifier can be obtained. Since the load impedance is:

$$Z_{load} = \frac{V_{load}}{I_{load}} \quad (2.3)$$

Equation (2.2) can be re-written as:

$$I_{DS} = I_{DSq} - \frac{(V_{DS} - V_{DSq})}{Z_{load}} \quad (2.4)$$

Equation 2.4 is the fundamental equation which describes the relationship between the drain current (I_{DS}) and drain voltage (V_{DS}) of the transistor.

Now the point where $V_{DS} = V_{DSq}$ and $I_{DS} = I_{DSq}$ is called the bias point of the amplifier. The current and voltage of the transistor follows a trajectory which is centred at this point. This trajectory is called the “load line”. When the load impedance Z_{load} is equal to a pure resistance (R_{load}), then the slope of the load line is equal to $-1/R_{load}$.

It is common practice to superimpose the load line on the I_{DS} - V_{DS} curves of the transistor. The ultimate limits on the load line are imposed by the device constraints since exceeding them is detrimental for the device. For instance, the maximum value of the voltage (V_{MAX}) is limited by the breakdown voltage of the device and the maximum drain current (I_{MAX}) is limited by carrier density and saturation velocity of electrons in the material. On the other hand, the minimum value of drain current is zero as it cannot go negative and the minimum voltage defining load line is the knee voltage (V_{knee}) which is the drain voltage where $I_{DS} = I_{MAX}$.

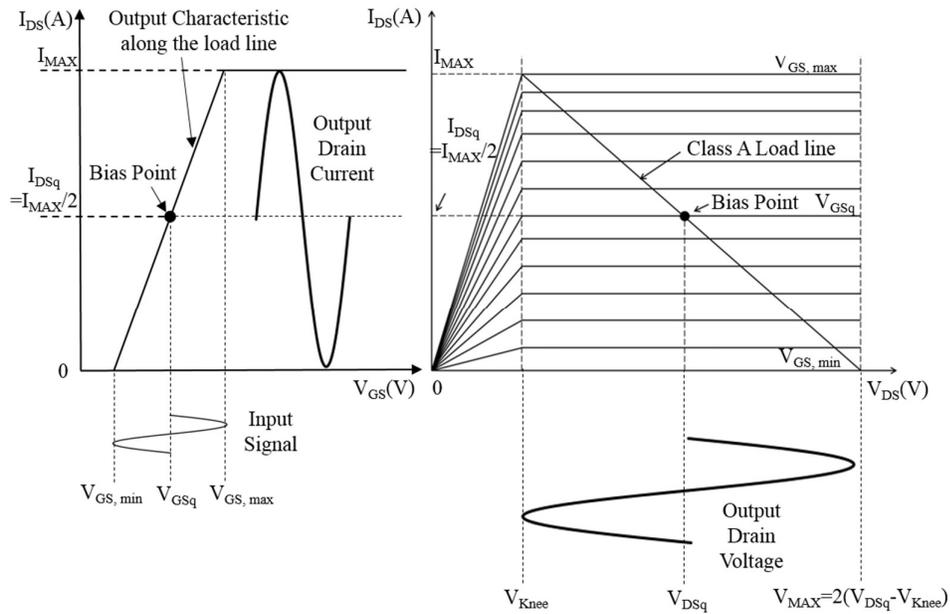


Figure 2.13: Load line superimposed on the I_{DS} - V_{DS} characteristics.

In Figure 2.13, the gate quiescent voltage V_{GSq} is in the middle of minimum ($V_{GS,min}$) and maximum ($V_{GS,max}$) gate voltages which corresponds to the threshold or pinch-off voltage and saturation voltage respectively. Therefore, the quiescent current here is $I_{MAX}/2$. If a sinusoidal input signal is applied at the gate, then as its amplitude swing

from $V_{GS,q}$ to $V_{GS,min}$ and $V_{GS,q}$ to $V_{GS,max}$, the corresponding sinusoidal output drain current swings from $I_{MAX}/2$ to zero and $I_{MAX}/2$ to I_{MAX} respectively. Similarly, the output voltage has a peak-to-peak amplitude of $(V_{DSq} - V_{knee})$ to $2(V_{DSq} - V_{knee})$. In a load line match, the value of the optimum load resistance presented to the transistor current generator is determined to ensure these maximum voltage and current swings to obtain maximum power. In this example, it is given by:

$$R_{load} = V_{MAX} / I_{MAX} \quad (2.5)$$

On the other hand, in a conjugate match, the maximum power is delivered into an external load by a generator when the load resistance value is equal to the real part of the current generator impedance (R_{gen}) and the reactive part is resonated out. In an amplifier design, the source and load impedances, Z_{source} and Z_{load} , can be conjugate matched to the input and output impedances, Z_{in} and Z_{out} , of the generator, as in

$$Z_{source} = Z_{in}^* = Z_0 \left(\frac{1 + \Gamma_{source}}{1 - \Gamma_{source}} \right) = Z_0 \left(\frac{1 + \Gamma_{in}^*}{1 - \Gamma_{in}^*} \right) \quad (2.6)$$

$$Z_{load} = Z_{out}^* = Z_0 \left(\frac{1 + \Gamma_{load}}{1 - \Gamma_{load}} \right) = Z_0 \left(\frac{1 + \Gamma_{out}^*}{1 - \Gamma_{out}^*} \right) \quad (2.7)$$

Here Γ are the reflection coefficients and can be obtained from measured S-parameters [2.27]. A device gives higher output power for small input signal than when it is conjugate matched since $R_{gen} > R_{load}$. The conjugate match however does not take the physical constraints of the device due to material properties such as maximum current and breakdown voltage into account.

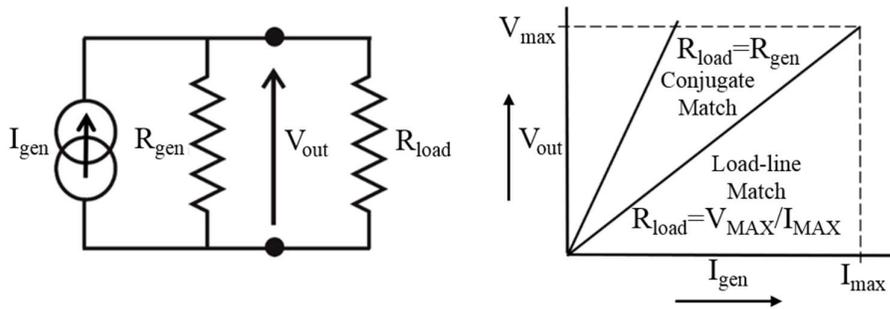


Figure 2.14: Conjugate match and load line match [2.28].

Therefore, when an amplifier is optimised for power gain, conjugate match, which is also called small-signal gain match, is applied. On the other hand, when maximum

output power is the design requirement, load-line match, which is also called power match, is the ideal choice.

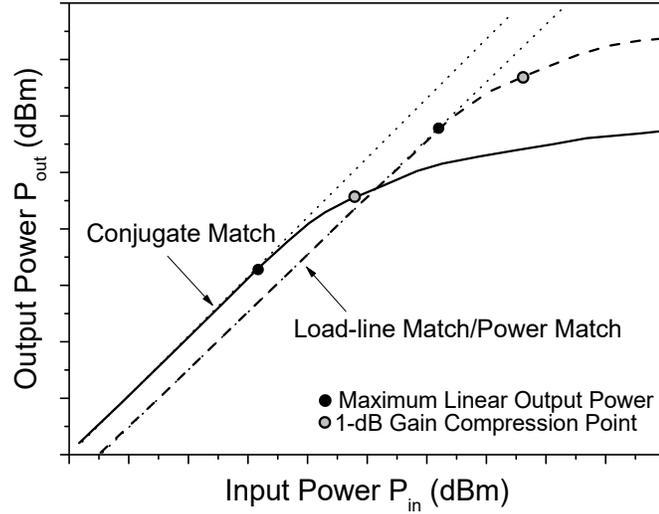


Figure 2.15: Input power versus output power and gain compression characteristics for conjugate match and load line match impedance matching.

Figure 2.15 shows the output power and gain compression characteristics of an RFPA for conjugate and load-line impedance matching. The load-line match leads to higher maximum linear output power as the gain compressions starts at higher output power.

2.5 Figure of Merits

2.5.1 Power Gain

The power gain (PG) of an amplifier is the ratio of the power delivered at the load (P_{load}) to the input power (P_{in}) delivered by the generator and given by the following expression:

$$Power\ Gain\ (PG) = \frac{P_{load}}{P_{in}} \quad (2.8)$$

Commonly the power gain is expressed in dB:

$$PG\ (dB) = P_{load}\ (dBm) - P_{in}\ (dBm) \quad (2.9)$$

2.5.2 Gain Compression

Ideally, as the input power is increased, the output power of the device should also increase given by the relationship in (2.8). However, in a real amplifier this is not the case. At one point, the output power does not increase proportionally with input signal. The point, as shown in Figure 2.16, where the amplifier displays a reduction of 1dB

in the power gain is called the 1dB compression point, and the corresponding output power is the P1dB output power.

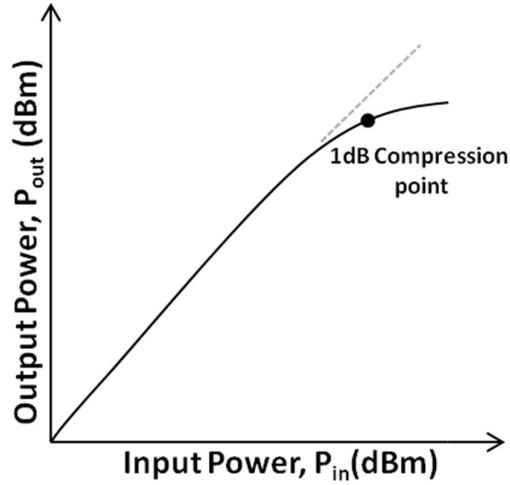


Figure 2.16: Compression characteristic for an RF power amplifier.

The P1dB is widely used as an indication of the linearity of an RF PA as it represents the maximum linear output power.

2.5.3 Efficiency

The drain efficiency (η) or simply called efficiency is defined as the ratio of RF output power to DC input power from the supply and given by the following equation:

$$\eta = \frac{P_{out}}{P_{DC}} \quad (2.10)$$

It describes the efficiency of an amplifier to convert DC supply power into output power. Therefore, it is also called DC-to-RF efficiency. The output power is the RF power at the load at the fundamental frequency and it given by:

$$P_{out} = P_{load} = \frac{I_{load} V_{load}}{2} = \frac{I_{load}^2 R_{load}}{2} \quad (2.11)$$

Where I_{load} and V_{load} are respectively the values of output current and voltage at the fundamental frequency, and R_{load} is the load resistance. The DC power is expressed as:

$$P_{DC} = V_{DSq} I_{DC} \quad (2.12)$$

Where V_{DSq} is drain quiescent voltage and I_{DC} is the mean or DC component of the output current.

The measure of the efficiency of the device with more importance is the power added efficiency (PAE) which describes the incremental RF power added by the amplifier. It takes into account the input power required to achieve an output power. As a result, PAE depends on the power gain of the device since $P_{out} = PG \cdot P_{in}$. Power added efficiency (PAE) is defined as:

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} = \frac{P_{in} (PG - 1)}{P_{DC}} = \eta \left(1 - \frac{1}{PG} \right) \quad (2.13)$$

2.5.4 Linearity

Gain compression, as explained earlier, represents nonlinearity in an amplifier. In fact, 1-dB gain compression point is the first indication of nonlinearity before the device goes into hard-saturation. Figure 2.17 shows the transfer characteristic curve of an ideal FET in comparison to that of a real device. Below the pinch-off voltage and from the saturation point, a device is said to be strongly nonlinear. In other words, these two voltage points set the boundary for the range of linear operation. In practice, even the linear region has some nonlinear characteristics which are termed as weakly nonlinear effects. Therefore, in a real-life situation, a transistor would have a transfer curve displayed in Figure 2.17 by the solid black curve, which combines both weak and strong nonlinear effects and gradually changes from cut-off to linear and from linear to saturation.

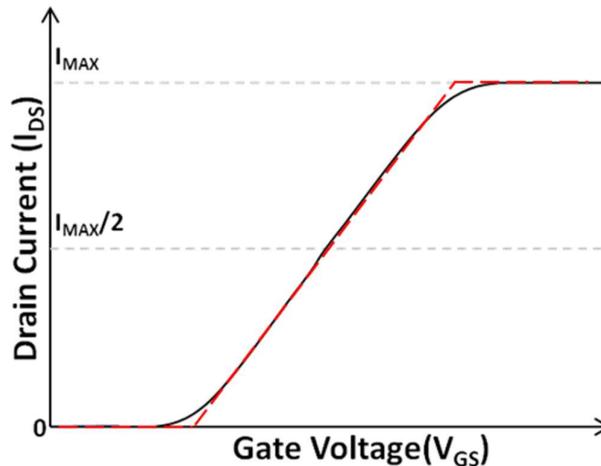


Figure 2.17: Transfer characteristic curve of FET in ideal case (red) and in real device combining weak and strong non-linearity (black).

When presented mathematically, the output current waveform can be expressed by the following equation [2.27]:

$$I_{out} = I_{DSq} + g_m V_{in} + g_{m2} V_{in}^2 + g_{m3} V_{in}^3 + \dots \quad (2.14)$$

Where

$$V_{in} = V_{GSq} + V_s \cos(\omega_0 t) \quad (2.15)$$

Where V_{GSq} is the gate quiescent current and V_s is the amplitude of the signal at the gate.

For simplicity, it can be assumed that $V_{in} = A \cos(\omega_0 t)$. Therefore, equation (2.14) can be written as:

$$I_{out} = I_{DSq} + g_m A \cos(\omega_0 t) + g_{m2} A^2 \cos^2(\omega_0 t) + g_{m3} A^3 \cos^3(\omega_0 t) + \dots \quad (2.16)$$

The first term on the right-hand side of (2.16) is the quiescent bias current. The second term is the linear output term at the fundamental frequency. The third term is the output term for second harmonic and so on.

By using the following relationship:

$$\cos^2(\omega_0 t) = \frac{1}{2}(\cos(2\omega_0 t) + 1) \quad (2.17)$$

Equation (2.16) can be written as:

$$I_{out} = \left(I_{DSq} + \frac{g_{m2} A^2}{2} \right) + g_m A \cos(\omega_0 t) + \frac{g_{m2} A^2}{2} \cos(2\omega_0 t) + \dots \quad (2.18)$$

For low levels of input power, the harmonic components are negligible and a good approximation can be achieved even after ignoring the terms where the powers of A are greater than 2. As the input power increases beyond a certain value, the harmonic components also start to increase, first the second harmonic, followed by the third- and fourth- harmonic components. As the gain of the amplifier begins to compress, these harmonics increase more rapidly with input power. Ultimately, the amplifier is in its strongly nonlinear region, and the output power saturates when any further increase in input power results in no further increase in the output power at the fundamental frequency.

For a two-tone signal, the linearity of RF PA is commonly described in terms of intermodulation distortion. The two-tone signal as in (2.19) have same amplitude (A), but different frequencies ω_1 and ω_2 .

$$V_{in} = A(\cos(\omega_1 t) + \cos(\omega_2 t)) \quad (2.19)$$

If the V_{in} from (2.19) is put into (2.14), then along with DC and harmonic terms, other terms are produced at frequencies at the sum and difference of ω_1 and ω_2 . In particular, there are two terms at frequencies $(2\omega_2 - \omega_1)$ and at $(2\omega_1 - \omega_2)$ which are very close to the outputs of two fundamental tones and have the following form:

$$i_{IMD3} = \frac{3}{4} g_{m3} A^3 [\cos(2\omega_1 - \omega_2)t + \cos(2\omega_2 - \omega_1)t] \quad (2.20)$$

As indicated from the presence of the cubic term in equation (2.20), these tones are known as “third-order intermodulation” and of great importance in the assessment of RF PA linearity as the frequency of this component is close to the frequencies of the input signal. A two-tone input signal with different amplitude shows non-linear behaviour as small-signal gain suppression and cross-modulation.

It is desired that this non-linear product is as small as possible. It has been observed that at a certain gate voltage and a particular input power, the IMD3 has a very low value. These points are called IMD3-null or sweet spots. Biasing the amplifier at these points leads to higher signal to IMD ratio and as a result, the amplifier shows better linearity.

2.5.4.1 AM/AM and AM/PM distortion

The amplitude-to-amplitude or AM/AM distortion in nonlinear system such as an RF PA shows the change in output signal amplitude with respect to the input signal amplitude. The AM/AM distortion is dominated by the nonlinear transconductance (g_m) of the device and therefore shows similar characteristic as the gain compression. The amplitude-to-phase or AM/PM distortion is the unwanted change in the phase of the output signal with respect to the change in the amplitude of the input signal. The AM/PM distortion has been attributed to nonlinear capacitances in the device [2.29].

2.6 Classification of Power Amplifiers

An RF PA designer always has to negotiate a trade-off between power gain, linearity and efficiency. However, the importance of each criterion is different for various

applications. For example: linearity is important for a base station, whereas efficiency is vital for handsets on battery operated amplifiers used in broadcasting. These specific performances can be achieved by choosing appropriate class of operation and architecture of RF PA. There are primarily two groups of PAs: linear PAs and switch-mode PAs.

In the typical linear PA, the transistor works as a current source controlled by the input RF signal at the gate. Linear PAs are usually suitable in applications where linearity or bandwidth is important; however, these PAs have low efficiency. In switch-mode PAs, the transistor operates as a switch. In an ideal switch-mode amplifier, the transistor is either open to allow current flowing through the device but with no voltage across it, or closed, with voltage across the device but allowing no current flowing through it. This allows the PAs to achieve 100% efficiency. However, this high efficiency is achieved at the expense of decreased linearity and bandwidth.

2.6.1 Linear Power Amplifiers

2.6.1.1 Class-A Amplifier

It can be observed in Figure 2.18 that the device is biased in the exact middle of its active region where $I_{DSq} = I_{MAX}/2$ and $V_{GSq} = (V_{GS,MAX} - V_{th})/2$; and at all times of the input cycle, it operates in the active region. This biasing condition creates a Class-A amplifier.

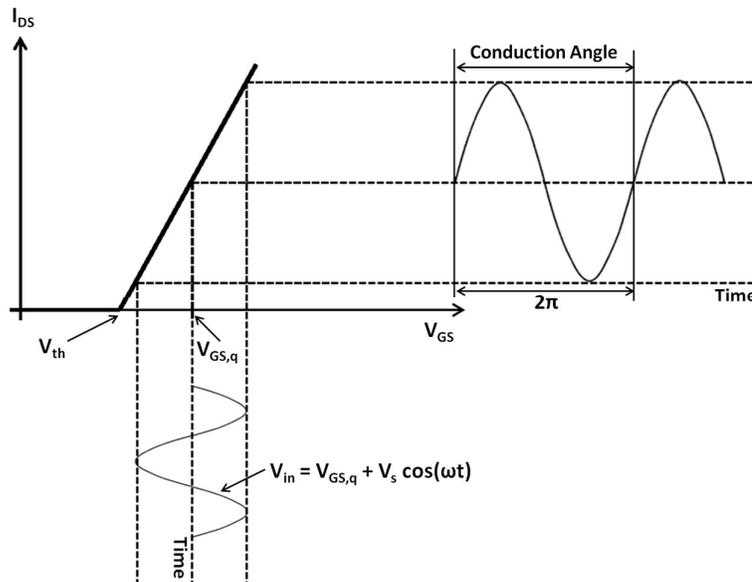


Figure 2.18: Input and output waveforms of class-A amplifier.

In [2.30], the conduction angle is defined as “the angle measured in degrees or radians over one period for which the device remains conducting”. For a class-A amplifier it is equal to 360 degree or 2π radians. The RF voltage waveform or the maximum value of the voltage swing across R_{load} is $(V_{DS,q} - V_{knee})$ and the current waveform has a maximum amplitude of $I_{MAX}/2$. For a class-A amplifier, $I_{DS,total}$ can reach to a maximum value of I_{MAX} .

The DC power consumption is given by equation 2.22:

$$P_{DC} = I_{DSq} \times V_{DSq} \quad (2.22)$$

And the RF power can be calculated using:

$$P_{RF} = (I_{load} \times V_{load}) / 2 \quad (2.23)$$

Therefore, the maximum RF output power, where the current and voltage swings have the maximum values, is:

$$P_{RF,MAX} = \frac{(I_{MAX}/2) \times (V_{DSq} - V_{knee})}{2} = \frac{I_{DSq} \times (V_{DSq} - V_{knee})}{2} \quad (2.24)$$

The maximum drain efficiency of a Class-A amplifier is given by:

$$\eta_{MAX} = \frac{P_{RF,MAX}}{P_{DC}} = \frac{V_{DSq} - V_{knee}}{2V_{DSq}} \quad (2.25)$$

The maximum efficiency of a Class-A amplifier can be 50%, if only given that $V_{knee} = 0$ V. The calculated V_{knee} for the GaN HEMT devices studied in this thesis is the range of 3 V to 4.7 V. As the V_{knee} is more than 0 V, the efficiency is reduced even further in practice. Since the device is on for the whole time, the output of Class-A amplifier can totally resemble the input signal, only amplified and thus this amplifier shows very good linearity. However, even the Class-A amplifiers display some weak nonlinearity such as intermodulation distortion even at lower levels [2.28].

2.6.2 Class-B Amplifier

In a Class-B amplifier, the transistor is biased at the threshold voltage. If a sinusoidal RF input signal with a peak value of V_s is applied to the transistor biased at V_{th} , then the input voltage can be written as:

$$V_{in} = V_{GSq} + V_s \cos(\omega t) \quad (2.26)$$

The output current at the drain which is given by:

$$I_{out} = I_{DSq} + g_m (V_{in} - V_{th}) \quad (2.27)$$

Now when $V_{in} < V_{th}$, there is no current as the device does not conduct any longer. The Class-B amplifier has a conduction angle of 180 degrees or π radians. Since the device conducts for 180 degrees compared to 360 degrees in Class-A amplifiers, the DC power consumed is reduced and as a result, efficiency in a Class-B amplifier is higher than that of Class-A amplifier. As the device conducts for half cycle of the input signal, the output current resembles a half-wave rectified sinusoid signal. The drain voltage swings from $V_{DS,q}$ down to V_{Knee} and up to $2(V_{DS,q} - V_{Knee})$, so the zero-to-peak amplitude is $(V_{DS,q} - V_{Knee})$. The maximum value of current across the load (I_{load}) is I_{MAX} . The DC component of the drain current in Class-B amplifier is given by I_{MAX}/π .

The maximum efficiency of a Class-B amplifier [2.30] is given by:

$$\eta_{MAX} = \left(\frac{I_{load}}{I_{MAX}} \right) \left(\frac{V_{DSq} - V_{knee}}{V_{DSq}} \right) \frac{\pi}{4} \quad (2.30)$$

When $V_{knee} = 0$ V and $I_{load} = I_{MAX}$, the maximum value of drain efficiency of a Class-B amplifier is close to $\frac{\pi}{4}$ or 78%.

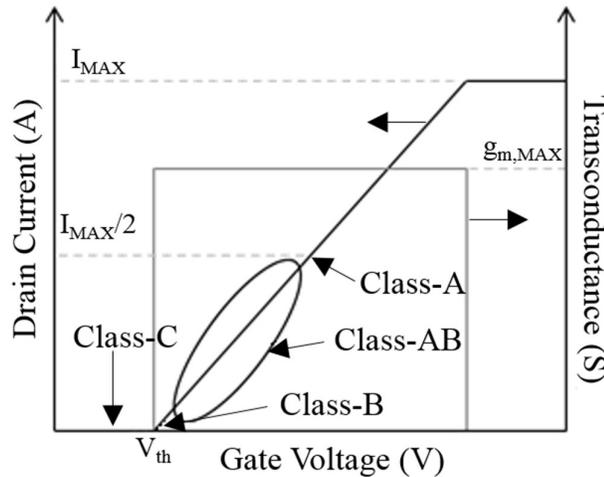


Figure 2.19: Transfer characteristic and forward transconductance of an ideal amplifier. Bias conditions for class-A, B, AB and C amplifiers are also shown.

Although Class-B amplifier is clearly more efficient than Class-A amplifier, it shows poor linearity. A Class-B amplifier could be linear if the transconductance (g_m) was constant throughout the conduction angle as shown in Figure 2.19. However, unlike

the ideal case, in real devices the forward transconductance (g_m) gradually starts to decrease and falls to zero around the threshold and saturation voltages and therefore if the transistor is biased at its threshold voltage, the output suffers from distortion. Therefore, in practice the device is biased slightly above the threshold voltage for a Class-B amplifier.

2.6.3 Class-AB Amplifier

A Class-A amplifier is used when linearity is the main priority. However, it suffers from very low efficiency of maximum of 25% to 30%. On the other hand, in applications where higher efficiency is important, Class-B amplifier is suitable, but it suffers from poor non-linearity due to its bias-point near threshold voltage. Therefore, in an application where both linearity and efficiency are crucial, a Class-AB amplifier can be employed. A Class-AB amplifier is biased somewhere in between the bias points of Class-A and B operations. When the input voltage swings below the threshold voltage, the device does not conduct for that portion of the cycle. It overcomes the gain loss at low gate voltages around threshold voltage in Class-B amplifier and at the same time, since the quiescent current is lower, it has better efficiency than a Class-A amplifier. Depending on the bias point, the conduction angle of a Class-AB amplifier has a value in between 180 and 360 degrees and it has efficiency between 50% and 78%.

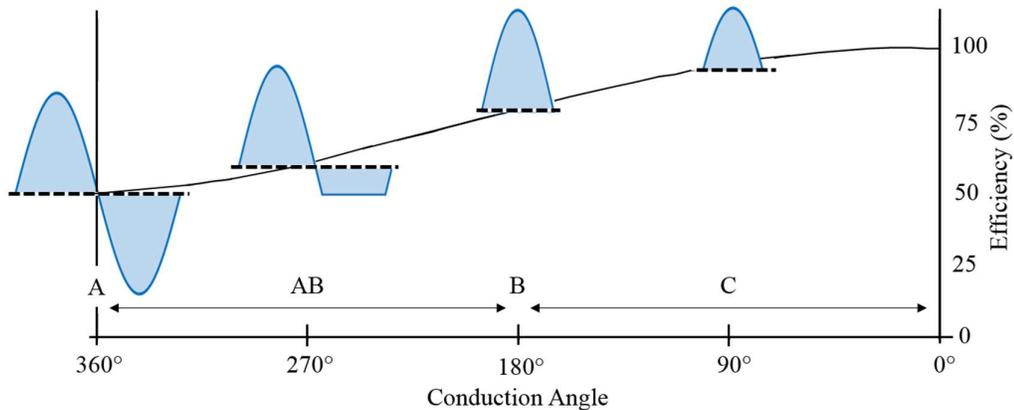


Figure 2.20: Output waveforms and conduction angles of Class-A, AB, B and C amplifiers.

2.6.4 Class-C Amplifier

The transistor is biased below its threshold voltage in a Class-C amplifier, and as a result, the device is active for less than half of the input RF signal and the conduction angle is between 180 and 0 degrees. The Class-C PA achieves high efficiency by

compromising linearity. As it can be seen in Figure 2.20, the efficiency can be increased further by reducing the conduction angle. However, this results in a decline of output power toward zero [2.28]. The common trade-off is an ideal efficiency of 85% at a conduction angle of 150 degrees.

2.7 Power Amplifier Architectures

Modern modulation schemes use complex waveforms to high speed data transmission. In order to maintain both the amplitude and phase information of the modulated signal, it is crucial that the PA is highly linear. On the other hand, the high peak-to-average power ratio (PAPR) in these complex modulation schemes requires the linear RF PAs to be operated in back-off condition where the efficiency is reduced. With the increase in usage of portable voice and data communication systems; it has become essential that the PA, which consumes most of the energy in communication system, should be highly efficient since it helps to reduce the power consumption, extend the battery lifetime, reduce the cost of heat management system, increase the overall reliability of the system and also reduce the environmental pollution. There are few PA architecture and techniques that can be implemented to improve the linearity or efficiency or both.

2.7.1 Balanced Amplifier

A single transistor amplifier sometimes does not have sufficient power capability to meet the required output power. In such case, a balanced amplifier configuration, shown in Figure 2.21, can be implemented, which comprises two identical amplifiers and two 3dB hybrid quadrature couplers.

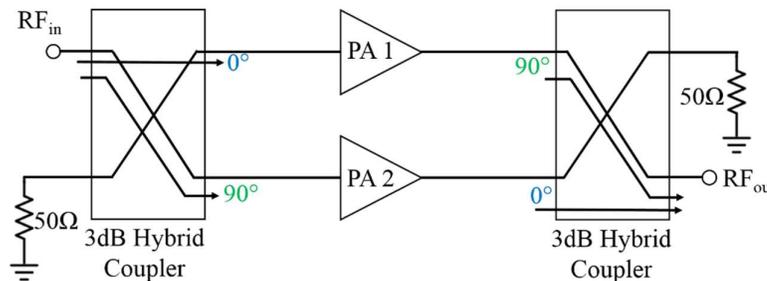


Figure 2.21: Simplified Balanced PA architecture.

The 3dB hybrid coupler splits the input signal equally with 90° phase difference and feeds the signals to the individual amplifiers. At the output coupler, the output signals from the PAs get 90° and 0° phase shifts. Thus the signal from the amplifiers are in phase and as a result, this configuration can achieve twice the output power of a single-

ended amplifier. The isolated ports of the couplers in the balanced PA are typically terminated by 50Ω . The reflected signals at the input and output from the individual PAs are 180° out of phase and cancel each other out. As a result, a balanced amplifier has low return loss and better stability compared to a single-ended amplifier. However, the cost and size of the balanced amplifier will be more than double compared to a single-ended amplifier due to the hybrid coupler.

2.7.2 Multiple Stage Amplifier

In RF PA design, often a single transistor amplifier cannot meet the specified gain requirement of the system. A multiple stage amplifier, where two or more amplifiers are connected in cascade, can be the solution. Figure 2.22 shows the basic architecture of a two-stage amplifier. The output from the first PA is the input to second amplifier.

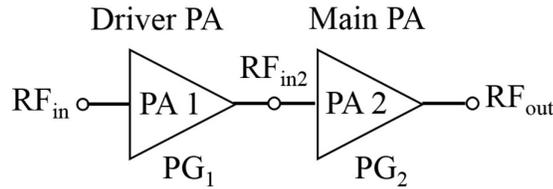


Figure 2.22: Simplified Multistage PA architecture.

The total power gain of this two-stage amplifier can be calculated as following:

$$RF_{out} = PG_2 \times RF_{in2} = PG_2 \times PG_1 \times RF_{in} = PG_{total} \times RF_{in} \quad (2.30)$$

$$PG_{total} (dBm) = PG_1 (dBm) + PG_2 (dBm) \quad (2.31)$$

In a multiple stage amplifier, the amplifiers do not have to have the same power. Therefore, usually a low power amplifier is used in the first stage as the driver amplifier and the second amplifier is a high power amplifier, which acts as the main power amplifier. A combination of balanced power amplifier with a driver amplifier in cascade can be implemented to achieve the required gain and output power.

2.7.3 Doherty

The Doherty amplifier, first proposed in 1936 by W.H. Doherty [2.31], offers a solution to the degradation of average efficiency for signals with amplitude modulation. A Doherty architecture is designed with a combination of two individual PAs called the main or carrier amplifier and the auxiliary or peaking amplifier which are typically biased at Class-AB/B and Class-C respectively. Up to a certain level of

the input power, the main amplifier alone produces the output power and the peaking amplifier is biased off. The peaking amplifier starts to produce output at a point when the main amplifier starts to show gain compression as shown in Figure 2.23. As a result, the combined output power is linear up the compression point of the peaking power amplifier.

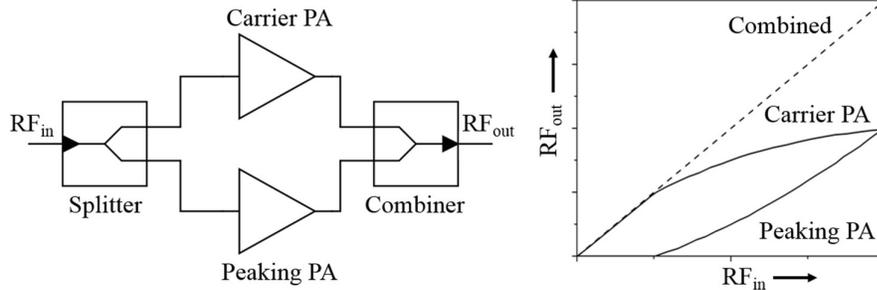


Figure 2.23: Simplified Doherty PA architecture and performance.

Typically, the point where the peaking amplifier becomes active is 6dB power backed-off from the peak combined output power. This allow to maintain the maximum efficiency of the main PA for a significant range of input power.

2.7.4 Envelope Elimination and Restoration (EER)

Kahn originally proposed the envelope elimination and restoration (EER) PA technique in 1952 [2.32]. The block diagram of the conventional EER can be seen in Figure 2.24.

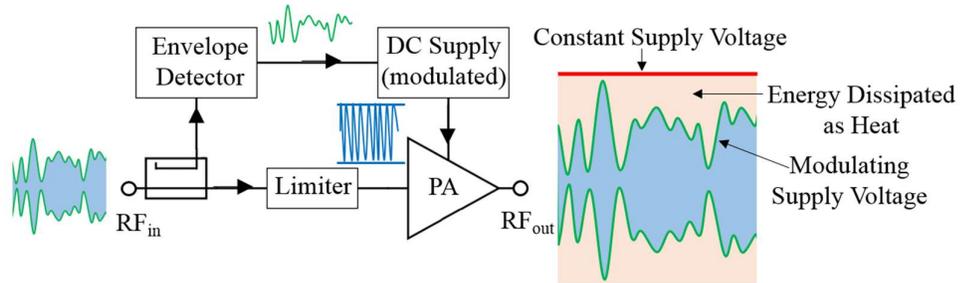


Figure 2.24: Block diagram of the EER transmitter.

The limiter removes the envelope of the input signal to allow a constant-amplitude amplified signal at the switch-mode PA output that conserves the phase modulation of the original input signal. The envelope information of the amplified signal at the output can be reinstated by modulating the DC supply voltage by the output signal from the coupled envelop detector after amplifying it up to a suitable condition. The efficiency

of EER architecture is higher compared to the constant supply voltage where the power consumption is higher.

2.7.5 Envelope Tracking (ET)

This technique is based on the principle of operating the amplifier in compression as much as possible to obtain higher efficiency. Since both the maximum power added efficiency and output power are functions of supply voltage, the basic idea is to map the instantaneous output power to an optimal supply voltage. The Envelope tracking (ET) system almost similar to EER except few major differences described as follows:

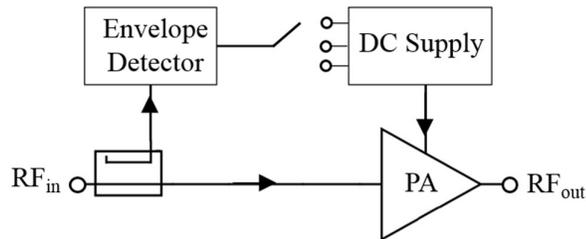


Figure 2.25: Block diagram of the ET transmitter.

From the ET architecture shown in Figure 2.25, the absence of a limiter can be noticed compared to that of EER in Figure 2.24. The second difference is that the modulating signal of the DC supply voltage does not fully replicate the envelope of the input signal. Based on the level of the input signal, the power supply, which is usually a DC-DC converter, acts like a switch with two or more discrete output voltage levels to optimize the efficiency. Finally, the RF PA operates in a linear mode.

2.7.6 Predistortion

In predistortion linearization technique a nonlinear element, which has a transfer characteristic complementary to the distortion from the amplifier, is placed in the path of input signal before amplification so that the resulting output is linear (Figure 2.26).

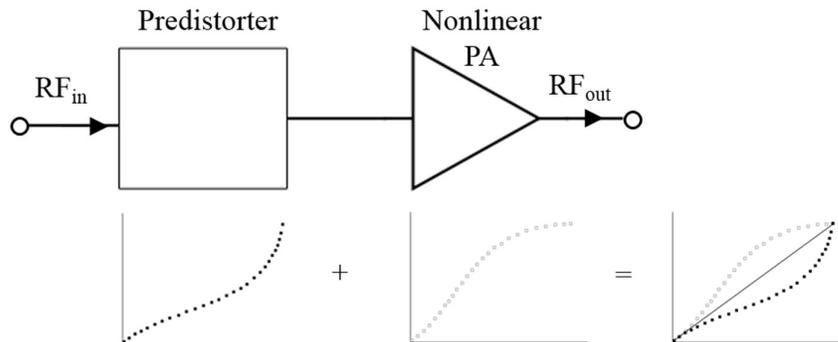


Figure 2.26: Block diagram of a transmitter implementing predistortion technique.

This allows the power amplifier to operate closer to its saturation output. As a result, both linearity and efficiency of the system are improved.

References

- [2.1] U. K. Mishra, P. Parikh, and Y. F. Wu, "AlGaIn/GaN HEMTs: An overview of device operation and applications," in *Proceedings of the IEEE*, vol. 90, pp. 1022–1031, 2002.
- [2.2] U. K. Mishra, L. Shen, T. E. Kazior and Y. F. Wu, "GaN-Based RF Power Devices and Amplifiers," in *Proceedings of the IEEE*, vol. 96, no. 2, pp. 287-305, February 2008.
- [2.3] B. J. Baliga, "Semiconductors for high-voltage, vertical channel field-effect transistors," *Journal of Applied Physics*, vol. 53, no. 3, pp. 1759–1764, 1982.
- [2.4] E. Johnson, "Physical limitations on frequency and power parameters of transistors," *1958 IRE International Convention Record*, New York, NY, USA, 1965, pp. 27-34.
- [2.5] R. J. Trew, "SiC and GaN transistors - is there one winner for microwave power applications?" in *Proceedings of the IEEE*, vol. 90, no. 6, pp. 1032-1047, Jun 2002.
- [2.6] S. E. Saddow and A. Agarwal, Eds., *Advances in Silicon Carbide Processing and Applications*. Artech House, INC, 2004.
- [2.7] G. J. Sullivan, M. Y. Chen, J. A. Higgins, J. W. Yang, Q. Chen, R. L. Pierson, and B. T. McDermott, "High-power 10-GHz operation of AlGaIn HFET's on insulating SiC," in *IEEE Electron Device Letters*, vol. 19, no. 6, pp. 198–200, 1998.
- [2.8] S. T. Sheppard, K. Doverspike, W. L. Pribble, S. T. Allen, J. W. Palmour, L. T. Kehias, and T. J. Jenkins, "High-Power Microwave GaN / AlGaIn HEMT 's on Semi-Insulating Silicon Carbide Substrates," in *IEEE Electron Device Letters*, vol. 20, no. 4, pp. 161–163, 1999.
- [2.9] S. J. C. H. Theeuwens and J. H. Qureshi, "LDMOS technology for RF power amplifiers," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 6, pp. 1755–1763, 2012.

- [2.10] Freescale Semiconductor, “50V RF LDMOS An ideal RF power technology for ISM ,broadcast and commercial aerospace applications.”, White paper. [Online]. Available: https://www.nxp.com/files/rf_if/doc/white_paper/50VRFLDMOSWP.pdf
- [2.11] O. Ambacher, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy, W. J. Schaff, L. F. Eastman, R. Dimitrov, L. Wittmer, M. Stutzmann, W. Rieger, and J. Hilsenbeck, “Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face AlGaN/GaN heterostructures,” *Journal of Applied Physics*, vol. 85, no. 6, p. 3222, 1999.
- [2.12] M. Wosko, B. Paszkiewicz, R. Paszkiewicz, and M. Tłaczała, “Influence of AlN spacer on the properties of AlGaN/AlN/GaN heterostructures,” *Optica Applicata*, vol. 43, no. 1, pp. 61–66, 2013.
- [2.13] J. M. Bethoux, P. Vennéguès, F. Natali, E. Feltin, O. Tottereau, G. Nataf, P. De Mierry, and F. Semond, “Growth of high quality crack-free AlGaN films on GaN templates using plastic relaxation through buried cracks,” *Journal of Applied Physics*, vol. 94, no. 10, pp. 6499–6507, 2003.
- [2.14] V. Hoel, N. Defrance, J. C. De Jaeger, H. Gerard, C. Gaquiere, H. Lahreche, R. Langer, A. Wilk, M. Lijadi, and S. Delage, “First microwave power performance of AlGaN/GaN HEMTs on SopSiC composite substrate,” *Electronics Letters*, vol. 44, no. 3, pp. 238–239, 2008.
- [2.15] P. Javorka, A. Alam, M. Marso, M. Wolter, J. Kuzmik, A. Fox, M. Heuken, and P. Kordoš, “Material and device issues of AlGaN/GaN HEMTs on silicon substrates,” *Microelectronics Journal*, vol. 34, no. 5–8, pp. 435–437, 2003.
- [2.16] J. Kuzmik, R. Javorka, A. Alam, M. Marso, M. Heuken and P. Kordos, "Determination of channel temperature in AlGaN/GaN HEMTs grown on sapphire and silicon substrates using DC characterization method," in *IEEE Transactions on Electron Devices*, vol. 49, no. 8, pp. 1496-1498, Aug 2002.
- [2.17] B. C. Joshi, C. Dhanavantri, and D. Kumar, “Sapphire, SiC, AlN, Si and diamond-substrate material for GaN HEMT and LED,” *Journal of Optoelectronics and Advanced Materials*, vol. 11, no. 8, pp. 1111–1116, August, 2009.
- [2.18] University Wafer (2016). *Your Leading Supplier of Silicon Wafers and other Substrates/Services* [Online]. Available: <http://www.universitywafer.com/>

- [2.19] Nitronex Corporation, “Substrates for GaN RF Devices,” [Online]. Available:http://www.richardsonrfpd.com/resources/RelDocuments/SYS_16/Nitronex_Substrates_for_GaN_RF_Devices_App_Notes.pdf, Application Note AN-011, June, 2008.
- [2.20] R.-Y. Yang, M.-H. Weng, and H.-W. Wu, “Loss Characteristics of Silicon Substrate with Different Resistivities,” *Microwave and Optical Technology Letters*, vol. 48, no. 9, pp. 1773–1776, 2006.
- [2.21] T. Warren Weeks, M. D. Bremser, K. S. Ailey, E. Carlson, W. G. Perry, and R. F. Davis, “GaN thin films deposited via organometallic vapor phase epitaxy on $\alpha(6H)$ -SiC(0001) using high-temperature monocrystalline AlN buffer layers,” *Applied Physics Letters*, vol. 67, no. 1, p. 401, 1995.
- [2.22] J. D. Brown, R. Borges, E. Piner, A. Vescan, S. Singhal, and R. Therrien, “AlGaIn/GaN HFETs fabricated on 100-mm GaN on silicon (111) substrates,” *Solid-State Electronics*, vol. 46, no. 10, pp. 1535–1539, 2002.
- [2.23] A. Krost and A. Dadgar, “GaN-based optoelectronics on silicon substrates,” *Materials Science and Engineering: B*, vol. 93, no. 1–3, pp. 77–84, 2002.
- [2.24] S. Lee, T. Kennedy, C. Hallin, H. Antunes, B. Fetzer, S. T. Sheppard, A. Burk, D. A. Gajewski, R. Mcfarland, J. Milligan, and J. Palmour, “Performance and reliability of AlGaIn/GaN HEMT on 100-mm SiC substrate with improved epitaxial growth uniformity,” *2013 International Conference on Compound Semiconductor Manufacturing Technology (CS MANTECH) 2013*, no. 919, pp. 117–120, 2013.
- [2.25] Y. C. Choi, L. F. Eastman and M. Pophristic, “Effects of an Fe-doped GaN Buffer in AlGaIn/GaN Power HEMTs on Si Substrate,” *2006 European Solid-State Device Research Conference*, Montreux, 2006, pp. 282-285.
- [2.26] H.-Y. Wang, K.-D. Mai, L.-Y. Peng, Y.-H. Cheng, and H.-C. Chiu, “Effects of the Fe-doped GaN buffer in AlGaIn-GaN HEMT on SiC substrate,” in *Proceedings of the 2015 IEEE International Conference on Electron Devices and Solid-State Circuits, EDSSC 2015*, vol. 7, pp. 645–648, 2015.
- [2.27] L. Besser and R. Gilmore, *Practical RF Circuit Design for Modern Wireless Systems (Volume I)*, Norwood, MA 02062: Artech House, INC, 2003.

- [2.28] S. Cripps, *RF Power Amplifiers for Wireless Communications*, Second Ed., Norwood, MA 02062, Artech House, INC, 2006.
- [2.29] L. C. Nunes, P. M. Cabral and J. C. Pedro, “AM/AM and AM/PM Distortion Generation Mechanisms in Si LDMOS and GaN HEMT Based RF Power Amplifiers,” in *IEEE Transactions on Microwave Theory and Techniques*, vol. 62, no. 4, pp. 799-809, April 2014.
- [2.30] L. Besser and R. Gilmore, *Practical RF Circuit Design for Modern Wireless Systems (Volume II)*, Norwood, MA 02062: Artech House, INC, 2003.
- [2.31] W. H. Doherty, “A New High Efficiency Power Amplifier for Modulated Waves,” in *Proceedings of the Institute of Radio Engineers*, vol. 24, no. 9, pp. 1163-1182, Sept. 1936.
- [2.32] L. R. Kahn, “Single-Sideband Transmission by Envelope Elimination and Restoration,” in *Proceedings of the IRE*, vol. 40, no. 7, pp. 803-806, July 1952.

Chapter 3

Device Modelling

Abstract

In this chapter, the primary types of device modelling suitable for RF PA design are briefly described first. The equivalent circuit large-signal model is the most popular choice for circuit simulation considering accuracy, complexity and computation time. Although various equivalent circuit models exist, the reported results show that no single model is capable of accurately representing the device characteristics across a range of frequencies, gate and drain voltages. Recent development in nonlinear device modelling is also explored

3.1 Introduction

An accurate large-signal device model can enable a “first-pass” success, thus save considerable cost and time in designing an RF PA. In 1952 [3.1], William Shockley presented the first FET model using partial differential equations to describe the time-dependent characteristics of the device. Since then, in the last 60 years, lots of advances have been made in the area of device modelling. As in [3.1], most of the earlier models reported in the literature are physics based [3.2], [3.3] with the aim to explain device behaviour and improve performance and fabrication process. Simulation programs to analyse nonlinear circuits started being developed in the late 1960s and early 1970s to evaluate contemporary circuits offered by the growing field of Integrated Circuits. One of the most distinguishable outcome of this developments was SPICE (Simulation Program with Integrated Circuit Emphasis), released in 1972, by University of California, Berkeley. The model proposed by Shichman and Hodges [3.4] is considered as the first MOSFET model for the SPICE circuit simulator. In 1974, Van Tuyl and Liechti proposed the first nonlinear computer model for gallium arsenide (GaAs) MESFET [3.5], [3.6] which was later simplified and applied by Curtice in his model [3.7] presented in 1980. A few more models for MESFET were developed over the next 10 years. The development of HEMT technology also influenced the nonlinear modelling research in the 1990s. The Angelov-Chalmers model [3.8], proposed in 1992, is the most popular empirical model for HEMT devices. Existing or improved MESFET models were also applied to model HEMT devices. The EEHEMT model, initially designed for GaAs HEMT by Keysight Technologies (formerly Agilent Technologies) for Advanced Design System (ADS) software, is an extension of Curtice model [3.9].

As presented in [3.10], Figure 3.1 shows a simple survey of published articles in IEEE transaction on microwave theory and technique (MTT) including the term “nonlinear model” or “large-signal model”.

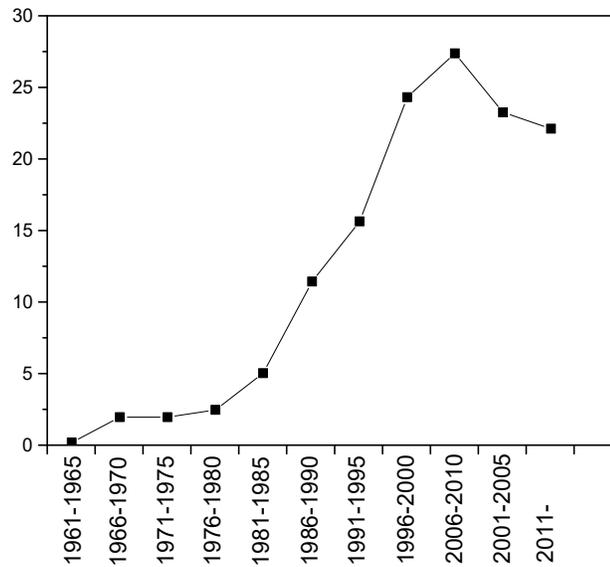


Figure 3.1: Average number of published articles in IEEE transaction on microwave theory and technique (MTT) including the term “nonlinear model” or “large-signal model” [3.10].

It can be noticed that activities in nonlinear modelling of RF transistors really started in 1980s and sped up in the 1990s, peaked in the 2000s and started to saturate in recent years.

In addition to the extensive research, the device characterization and modelling have also become more sophisticated and accurate with the technological advancement of measurement equipment and availability of powerful simulation tools. Modern vector network analysers combined with the pulsed testing equipment allows pulsed S-parameter and pulsed I-V measurements which significantly improved the accuracy of device characterization which is fundamental for modelling. The large-signal models have made their way from research lab to engineering and the manufacturing industry.

The organization of the chapter is as follows: the primary types of device models are briefly described first. Then a comparison of various compact models, which are the most popular choices for circuit simulation, are presented. In the end, the recent development in nonlinear device modelling is explored.

3.2 Types of Large-Signal Device Models:

Large-signal models for transistors can be generally categorized into two groups [3.11]: physics-based models and measurement-based or empirical models. The

empirical models can be further divided into behavioural models and equivalent circuit models as follows:

1. Physics-based Models
2. Measurement-Based or Empirical Models
 - I. Behavioural Models or “Black-box” models
 - A. Table-based Models
 - B. Artificial Neural Network Models
 - C. Harmonic Distortion Models (using X-parameters)
 - II. Equivalent circuit Models

3.2.1 Physics-based Models

Physic-based models usually describe the behaviour of the device by solving complex equations; it requires considerable amounts of simulation time and computer memory. Therefore, the analysis could be very lengthy and thus majority of those physics-based models would not be suitable for circuit design.

In last decade, physics-based models [3.12] – [3.19] which can be used in computer aided design (CAD) tools have been reported. These are constructed upon fundamental equations as well as derived equations to calculate the electric field, carrier density and transport properties based up on the material properties and device structural geometry. Some of these quasi-two-dimensional physics-based models [3.12], [3.13] assume that the electric field in the undepleted active channel is essentially one-dimensional, while still considering the conducting channel to be two-dimensional. In some physics-based models, a device is divided into regions and then by applying simplified linearized approximations with the right boundary conditions, a comprehensive device model can be derived. A physics-based model can be very accurate since the parameters have physical significance or origin. The models can be simply adjusted to take account of a wide range of phenomena that influence device performance. As a result, this model can accurately describe the device for any operating range.

However, materials and physical properties of the device must be known which can be difficult to obtain by the end user and sometimes requires sophisticated measurement systems. Since at the fabrication stage of the device all the information is available, implementation of this model is easier and more useful for device

engineers. A device with new materials or a new structure can be thoroughly characterised before fabrication using a physics-based model.

3.2.2 Measurement-based or Empirical Models

3.2.2.1 Behavioural Models or Black-Box Models

In behavioural or the “black-box” modelling technique, the internal operation or details of the device under test (DUT) is not required to be known. All the information required to construct such models is acquired by applying voltages or signals to the DUT and measuring its responses. As a result, these models are totally technology independent. However, one major drawback of this approach is the reduction in accuracy if the model is not simulated close to the measured data points. Therefore, in order to make these models highly accurate for a wide range of input signals and bias points, the responses from the DUT also have to be measured under a wide range of conditions. This can be very time-consuming and can increase the complexity of the model. Some of the commonly used black-box models such as table-based models, artificial neural network models and harmonic distortion models are briefly described in the following section.

3.2.2.1.1 Table-based Models

The table-based model can reproduce a device behaviour from measured data saved in a look-up table. Table 3.1 can be considered as a simplified data sample for a table-based model to describe the I-V characteristics of a device.

Table 3.1 A simplified data sample for a table-based model to describe the device I-V characteristics Cree CGH40025, a 25W GaN-on-SiC HEMT

$V_{GS} \backslash V_{DS}$	0	1	2	3	4	5
-4.0	0	1×10^{-6}	2×10^{-6}	3×10^{-6}	4×10^{-6}	5×10^{-6}
-3.75	0	1×10^{-6}	2×10^{-6}	3×10^{-6}	4×10^{-6}	5×10^{-6}
-3.50	0	1×10^{-6}	2×10^{-6}	3×10^{-6}	4×10^{-6}	5×10^{-6}
-3.25	0	0.8×10^{-3}	1.6×10^{-3}	2.2×10^{-3}	2.6×10^{-3}	3.0×10^{-3}
-3.0	0	31.57×10^{-3}	56.44×10^{-3}	72.49×10^{-3}	81.90×10^{-3}	87.49×10^{-3}
-2.75	0	116.8×10^{-3}	207.9×10^{-3}	265.7×10^{-3}	298.1×10^{-3}	315.7×10^{-3}

The measured values of dependent variables such as drain and gate currents are tabulated for each corresponding point of independent variables like V_{GS} and V_{DS} which are measured as well.

The value of the drain current at any voltage between the measured points can be interpolated from these measured data.

$$I_{DS,Model}(V_{GS}, V_{DS}) = \text{interpolate} \left(I_{DS,Measured}(V_{GS}, V_{DS}) \right) \quad (3.1)$$

Table-based large-signal models [3.20] – [3.27] have been developed for microwave transistors to reproduce the nonlinear behaviour in circuit design simulation tools. Multidimensional spline functions are implemented for fitting, interpolation and extrapolation of the measured data. The Root model [3.20], which can be considered as the first widely-used table-based model, uses eight state functions to describe intrinsic device characteristics. In [3.20], one of the state functions to describe the drain current in the frequency domain in the large-signal model, is expressed as:

$$I_D = H(\omega)I_{DC}(V_{GS}, V_{DS}) + j\Omega Q_D(V_{GS}, V_{DS}) + (1 - H(\omega))I_{high}(V_{GS}, V_{DS}) \quad (3.2)$$

In (3.2), I_{DC} is the directly tabulated values of measured DC I-V characteristics, while Q_D and I_{high} are computed from the measured s-parameters. During simulation, two-dimensional spline functions are used to interpolate the tabulated state functions. In some table-based models, only the fitting coefficients are stored.

Using small-signal data to generate nonlinear functions to describe the large-signal behaviour of the device is an indirect extraction method. With the progress of nonlinear vector network analyser systems, nonlinear characteristics of the FET can be obtained directly from time-domain large-signal measurements [3.28] – [3.30]. With the integration of active harmonic load-pull, advanced measurement systems allow to create look-up tables [3.31], [3.32] for a range of independent variables such as bias conditions, input power and load impedances. Compared to the indirect method like the Root model [3.20] which uses DC and S-parameters over 1000 bias points, the direct extraction in [3.31] requires only 121 data points. This reduces computation time and memory size of the model.

The selection of appropriate interpolation and extrapolation techniques in terms of accuracy, speed and memory requirements is essential for the model implementation in the simulator. This is also important to avoid convergence problems. A poor

interpolation technique may result in oscillation data; therefore, a good technique is required to ensure smooth data fitting to retain the continuity and monotonicity of the data and thus able to produce higher order derivatives of the data for better harmonics and intermodulation distortion simulation. Poor extrapolation techniques may lead to inaccuracy in data that are out of the measured data range.

3.2.2.1.2 Artificial Neural Network Models

Motivated by the capability of the human brain to gain an understanding from observation and derive a conclusion from presumption, the artificial neural networks (ANNs) are systems designed to process information in a similar way [3.33]. The building blocks of an ANN are neurons and links or synapses. A neuron receives data, processes them and yields an output. The neurons that receive external data are the input neurons and the neurons whose outputs are the system or model outputs are the output neurons. All the neurons in between these two stages, which are not connected externally, are called hidden neurons.

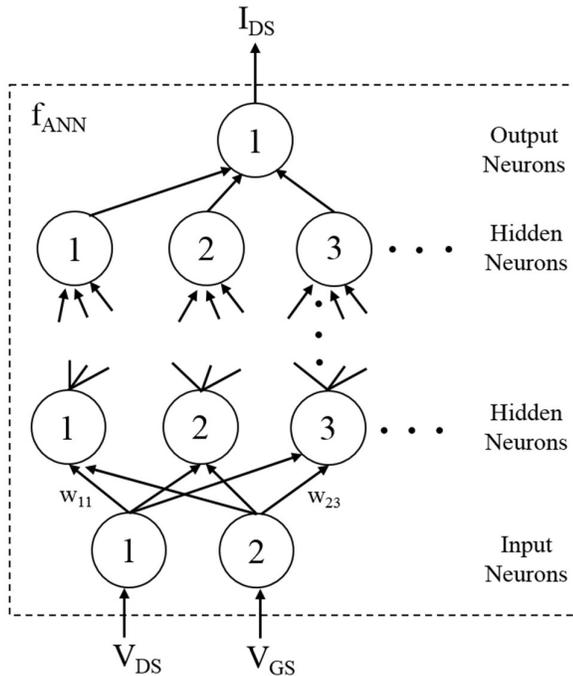


Figure 3.2: Architecture of an artificial neural network.

Assuming an ANN with two inputs and one output neurons as seen in Figure 3.2, the input-output relationship can be expressed as:

$$I_{DS} = f_{ANN}(V_{DS}, V_{GS}, w) \quad (3.3)$$

In (3.3), “w” is the weight parameter of an interconnection link between two neurons. The values of these weight parameters are optimized in the training phase in order to model the device characteristics.

The training of the ANN is the most important stage of the model development where it learns the input-output relationship of the transistor from data generated from physics-based model or measurement.

The initial values of the weight parameters depend on the ANN model used. The most popular neural network structure, which is multilayer perception (MLP) neural network [3.33], commonly uses initialization by random-weights. Choosing a suitable neural network structure and training algorithm is important while training a neural network. The selection of an ANN structure for a specific application depends on the relationship between the inputs and outputs. Radial basis function (RBF) networks, wavelet networks, recurrent networks and knowledge-based neural network (KBNN) are some of the other neural network structures, beside MLP, used for microwave modelling [3.34]. Different optimization-based training algorithms such as backpropagation (BP), conjugate-gradient, quasi-Newton, Levenberg-Marquardt, Huber quasi-Newton are commonly used for ANN training [3.34].

Once trained, ANN models can be very fast and accurate behavioural models that can be used in advanced simulation software such as ADS or Microwave Office. Nonlinear device modelling and RF power amplifier design have been demonstrated using neural network approach [3.35] - [3.45]. For a new technology where the device theory or equations are unavailable or very complex, the ANN models can be a great solution.

3.2.2.1.3 Polyharmonic Distortion Modelling Using X-parameters

Polyharmonic distortion (PHD) modelling [3.46] - [3.48] by Dr. Jan Verspecht and Dr. David Root is a frequency-domain black-box modelling approach. The fundamental idea of the PHD modelling is extending S-parameter measurements from small-signal to large-signal conditions. In this method, the DUT is simulated by a set of discrete tones which are harmonically related and the responses are measured using a large-signal network analyser (LSNA). The measured data contain all the nonlinear characteristics of the device such as compression characteristics, AM-PM distortion, amplitude dependency of the input and output match, amplitude and phase of the fundamental and harmonics, spectral regrowth. As a result, the extracted PHD model

from these data can be very accurate. The X-parameters [3.49], a trademark of Keysight Technologies, are based on the PHD modelling. These X-parameters are supersets of S-parameters measured with their nonlinear vector network analyser (NVNA) and are applicable to linear and nonlinear components under both small-signal and large-signal conditions. The measured X-parameters can include bias points, power and frequency as the independent sweep variable and can be used for large-signal modelling [3.50], [3.51] in ADS. The NVNA can be used in combination with a load-pull tuner to measure impedance-dependent X-parameters [3.52] - [3.55] that can generate extremely accurate black-box models.

3.2.2.2 Equivalent Circuit Models

The equivalent circuit large-signal model is an empirical model based on a small-signal equivalent circuit that describes the behaviour of the device over a range of frequencies at a specific bias point. The equivalent circuit is constructed with lumped elements that also have some physical aspects related to the device operation and technology.

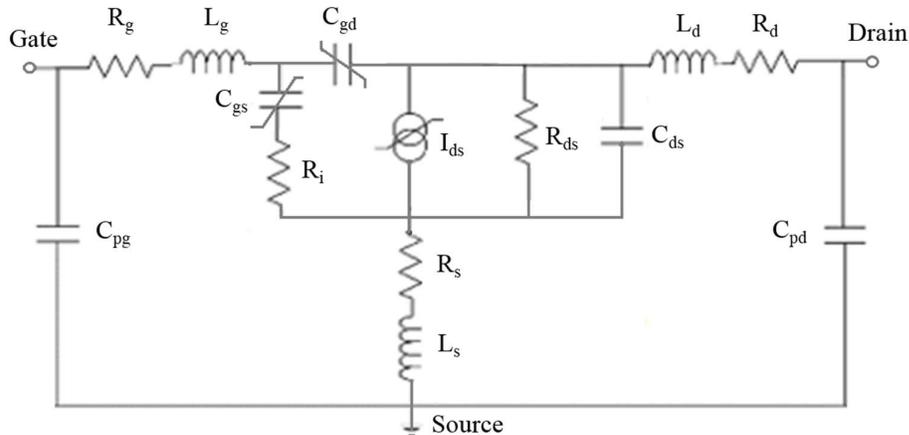


Figure 3.3: A large-signal equivalent circuit model of FET [3.56].

Figure 3.3 shows a simplified large-signal equivalent circuit model of a FET [3.56]. The topology of the network and number of elements in the equivalent circuit mainly depend on the requirement and frequency range of the target application.

The drain-source current generator represents the conduction current, which is obtained from I-V measurements. The capacitances are attributed to the additional displacement currents in the device originated by charge variations due to the time-varying voltage when an RF signal is applied. The nonlinear characteristics of these

capacitances are obtained from multi-bias S-parameter measurements. These behaviours of the device are then emulated mathematically with analytical functions that fit the sets of measured data over the range of voltage and frequency. When the model is simulated at a bias condition or frequency outside the range of measured data, it uses extrapolation to simulate the data. The primary advantage of the equivalent circuit model is the fast computational time which makes it very suitable for nonlinear circuit design in a simulator.

One of the disadvantages of the large-signal equivalent circuit modelling is that often additional parameters and fitting coefficients are used in the equations for better fit to measured data which have no physical significance. This can make the model more empirical and less physical. According to [3.57], the Curtice [3.58], EEHEMT [3.9] and Angelov GaN HEMT [3.59] models have 59, 71 and 90 parameters in the analytical equations respectively. As the number of parameters increases, the extraction procedure can be more difficult and time-consuming. This also increases uncertainty in parameter values that can lead to poor convergence.

Another major disadvantage of the large-signal equivalent circuit modelling is that the functions cannot fit the measured data for large range of bias points and frequency. Some of the most commonly used or at least the basis of the most proposed large-signal equivalent circuit models for the MESFET and HEMT are: Curtice quadratic [3.7], Curtice cubic [3.60], Statz [3.61], Materka [3.62], Advanced Materka, Rodriguez [3.63] and Angelov [3.64] models. The Materka, Statz and Rodriguez models are essentially improved Curtice Model. In the studies presented in [3.65] - [3.69], these large-signals models have been compared in terms of their DC and RF performances and the results are briefly summarised here.

For MESFET devices, the Curtice cubic model works best to predict the drain current (I_{DS}) as a function of V_{GS} , whereas the Rodriguez model is most accurate to predict I_{DS} as a function of V_{DS} . The Statz model shows good fitting at higher V_{GS} , but suffers from inaccuracy at lower V_{GS} . The Advanced Materka model shows good overall fitting for I-V characteristics. However, models proposed for MESFET do not work very well for HEMT because of the significant distinctions between their electrical behaviours [3.70]. Unlike MESFETs, HEMTs turn on more sharply after threshold voltage and show prominent peak transconductance well before the maximum gate voltage. In addition, the input capacitance in HEMT devices decreases very quickly at

lower gate voltages and shows a peak value, whereas in MESFETs it changes slowly. Some of the early models for the HEMT devices are basically the MESFET models or in some cases their modified or improved variations with additional parameters. For example, Miller et al. [3.65] used additional parameters to the Curtice and Materka models to improve the models for HEMT devices. This dependency and the relationships of some other parameters with V_{DS} are correctly modelled by Chalmers. The Angelov model [3.64], which is an extension of the Chalmers model [3.8], provides the best fitting for the HEMT for functions of the V_{GS} and V_{DS} . It can be used for both MESFET and HEMT devices, although it fails to show good fitting near cut-off for MESFET devices.

The most important part of large-signal modelling is accurately predicting the RF performance of a device over a range of frequencies and bias points. The study in [3.69] shows that Advanced Materka model can achieve best overall prediction of output power across a range of frequencies and bias conditions; whereas according to [3.67], best fitting for output power is achieved by the Statz model. While the Curtice cubic model predicts the 1-dB and 3dB gain compression points more accurately, the Statz model more accurately predicts the third-order intermodulation distortion or IMD_3 . The Angelov model does not show any significant advantage over other models in terms of IMD_3 prediction [3.67].

The results in the above studies confirmed that no single model is capable of accurately representing the device characteristics across a range of frequencies, gate and drain voltages. In addition, the different conclusion in different studies also show that the overall accuracy of the models depends on the accuracy of parameters and coefficients extraction. There is also a trade-off between accuracy and complexity. Therefore, the selection of appropriate model always depends on the application.

3.3 Developments in Large-Signal Device Modelling

Self-heating and trapping induced dispersion influences the GaN HEMT performance, and therefore these effects have to be incorporated into a large-signal model in order to accurately represent a real GaN device in simulation.

Self-heating arises from the power dissipation in GaN HEMT devices. The power dissipation (P_{diss}) can be calculated from (3.4):

$$P_{diss}(W) = P_{DC}(W) + P_{in}(W) - P_{out}(W) \quad (3.4)$$

Here, P_{in} , P_{out} and P_{DC} are the input, output and consumed DC power respectively. Typically, GaN HEMT based RF PAs are biased at high drain voltage and high current. The power dissipation in the GaN device at these bias conditions is high, and consequently the internal temperature of the device rises during operation. The DC power consumption increases even further as a function of RF input signal at the gate. Due to the power dissipation, the channel temperature can reach several hundred degrees above the ambient temperature. The phonon scattering in the crystal is increased because of this increased temperature and as a result, the electron mobility (μ) is decreased. Therefore, as displayed in Figure 3.4, the drain current decreases at high power level and results in a negative differential output conductance.

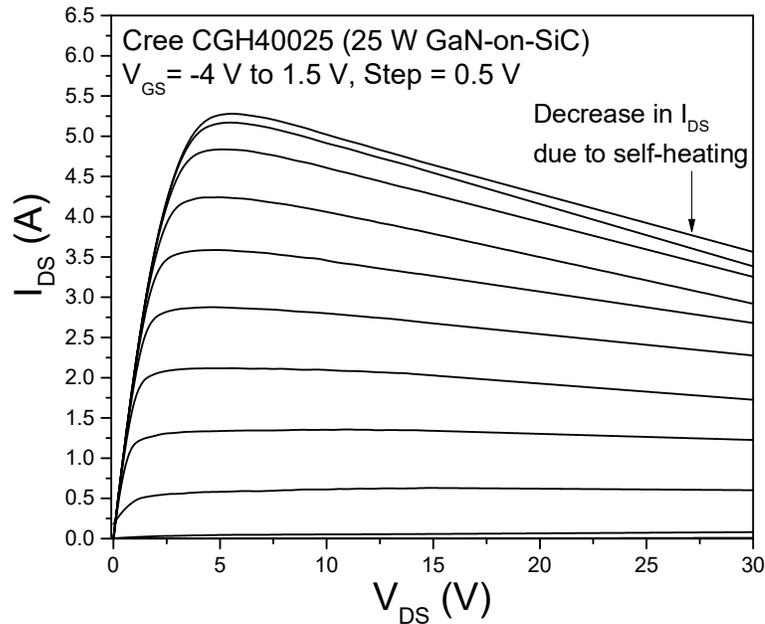


Figure 3.4: Measured I-V characteristic of Cree CGH40025, a 25 W GaN-on-SiC HEMT with self-heating effect. The drain current (I_{DS}) decreases at high power level and results in a negative differential output conductance

It can be observed that this effect is not so strong at low drain voltages. Sometimes, this can also be represented with the nonlinear characteristics of source (R_s) and drain (R_d) resistances with increasing temperature. These effects are known as the self-heating effects in GaN HEMTs and significantly influences the device I_{DS} - V_{DS} characteristic and performance. Severe self-heating reduces device lifetime and can even cause device failures which greatly affect overall reliability.

The RF output power measured at microwave frequencies for GaN HEMTs has been reported to be lower than the expected value based on the DC I-V characteristics. This degradation of the device performance can be attributed to reduction in drain current and an increase in the knee voltage. This occurrence has been termed as the “knee walkout”, “current collapse”, “current slump” or “DC-to-RF” dispersion. This behaviour is related to the existence of two kinds of traps in device structure: surface traps and buffer or substrate traps.

In surface trapping, electrons, as shown in Figure 3.5, are confined into the surface states in the AlGa_N barrier layer of the AlGa_N/Ga_N devices. These electrons act like a negatively biased metal gate that gives rise to the concept of ‘virtual gate’ [3.71] which depletes the 2DEG of electrons and thus increases the parasitic resistances of the devices.

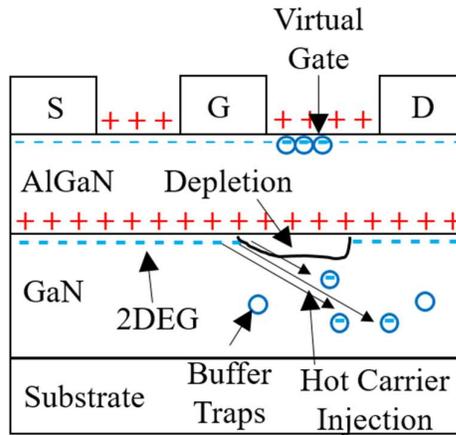


Figure 3.5: Locations of surface and buffer traps.

The traps in the buffer or substrate are generally the result of impurities or defects in the crystalline. Electrons get trapped into these energy states due to hot-electron injection at high drain voltage. These trapped electrons cannot take part in the conduction and as a result, the drain current is reduced. When a RF input signal is applied to a device, it changes the gate and drain voltages. Since the capture time is very short compared to the relatively long emission time of the electrons from the traps, for a RF signal at microwave frequency, the drain current cannot keep up with the change in gate and drain voltages. Hence, these mechanisms are also called “gate-lag” and “drain-lag”. The current collapse and gate-lag due to the surface states can be minimized by appropriate surface passivation such as silicon nitride, although the exact mechanism of this is not clearly known yet. It has been suggested that passivation

stabilizes the charge at the surface and the interface [3.72], increases the positive charge at the Si₃N₄/AlGaN interface [3.73], modifies donor states at the surface [3.71] or reduces the surface trap density [3.74]. Implementation of a field-plate in the device structure lessens the electric field at the drain edge of the gate which reduces the hot-electron injection into the buffer layer [3.75] and this can reduce the drain-lag. Most of the recent large-signal models such as in [3.27], [3.76] - [3.86] use either analytical functions, temperature-dependent parameters or sub-circuits to include the trapping and self-heating effects.

Using frequency and temperature dependent parameters in the expressions, Angelov et al. extended [3.64] the Chalmers model to include the temperature effects and frequency dispersion. The temperature dependency of main parameters is obtained by extracting the values in the temperature range of 17- 400 K and the frequency dispersion are taken into account by additional parameters whose values are obtained from DC and pulsed I-V and S-parameter measurements. Angelov et al. expressed the drain current as:

$$I_{ds,RF} [V_{gs}(t), V_{ds}(t)] = I_{ds,DC} [V_{gs}(t), V_{ds}(t)] + \Delta I_{ds} [V_{gs}(t), V_{ds}(t)] + \Delta \bar{I}_{ds} [V_{gs}(t), V_{ds}(t)] \quad (3.5)$$

The second and third terms on the right-hand side of (3.5) incorporates the dispersion effects into the drain current with frequency dependent parameters in the expressions for ΔI_{ds} and $\Delta \bar{I}_{ds}$.

The temperature effects are implemented to the model using linear function:

$$R_s(T) = R_{s0} + A_{Rs} \Delta T \quad (3.6)$$

Here, the function $R_s(T)$ represents the temperature dependency of the source resistance R_s , where R_{s0} is the value at room temperature, A_{Rs} is the linear temperature coefficient and ΔT is the difference between temperatures.

The second approach to incorporate self-heating and trapping induced dispersion in the equivalent circuit models is introducing sub-circuits. Curtice et al. extended [3.87] the Curtice model to include the gate-lag, drain-lag and self-heating effects by adding sub-circuits for each phenomenon as shown in Figure 3.6.

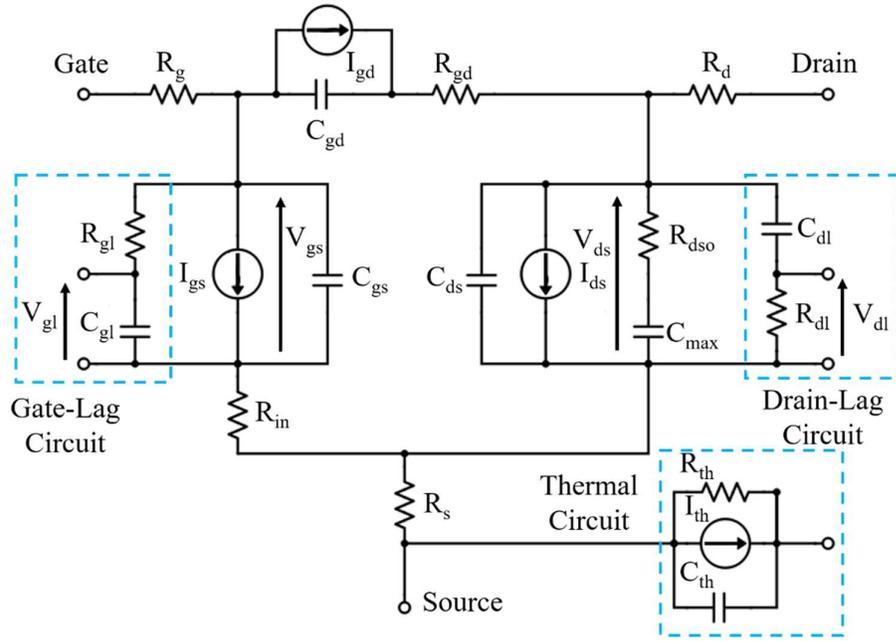


Figure 3.6: Curtice et al. [3.87] added sub-circuits in the FET model to incorporate the gate-lag, drain-lags and temperature effects.

The gate-lag and drain-lag circuits in the model in Figure 3.6 sample the gate and drain voltages and feed fractions of these voltages back to the gate. These feedback factors and the time constant of the RC circuit are the lag parameters. The thermal sub-circuit consists the device thermal resistance (R_{th}) and thermal capacitance (C_{th}). The values of the parameters can be extracted from measurements [3.80] or physics-based simulation [3.86]. In [3.78], a transistor in series with the main transistor has been used as the virtual gate to account the DC-to-RF dispersion. In [3.79], the sub-circuits add transients to gate voltage based on the capture and emission time of the charges from the traps. In the other models, a four-terminal circuit topology is used to characterize the trapping dispersion. In this approach, the current is described as a function of DC and RF gate and drain voltages as in (3.7):

$$I_{DS} = f(V_{DSq,DC}, V_{GSq,DC}, v_{ds,RF}, v_{gs,RF}) \quad (3.7)$$

The static and dynamic components are separated by RC filter networks at gate and drain terminals.

Most of these models also include the nonlinear characteristics of other parameters such as C_{gs} and C_{gd} which are extracted from pulsed S-parameter measurement at multi-bias points.

3.4 Analytic Approach for Large-signal Modelling

The analytic approach, which is described in detail in chapter 5, is an excellent alternative to conventional large-signal models. It is an equivalent circuit model using analytic method for mathematical computation. The basis of this method is a set of expressions derived from an equivalent circuit model whose parameter values are extracted from measured S-parameters. The measured IV characteristics are stored in table and used directly. In Angelov model [3.8], the equation for drain current is:

$$I_{ds} = I_{pk} (1 + \tanh(\psi)) \tan(\alpha V_{ds}) (1 + \lambda V_{ds}) \quad (3.8)$$

In (3.8), ψ is a power series function expressed as:

$$\psi = P_1 (V_{gs} - V_{pk}) + P_2 (V_{gs} - V_{pk})^2 + P_3 (V_{gs} - V_{pk})^3 \dots \quad (3.9)$$

In (3.8) - (3.9), I_{pk} is the drain current and V_{pk} is the gate voltage where $g_m = g_{m,max}$, α is the saturation voltage parameter and λ is the channel length modulation parameter. The coefficients P_1 , P_2 and P_3 influence the maximum value and shape the modelled transconductance curve. Initial values of most parameters are extracted from measured I-V characteristics and then optimization techniques are applied.

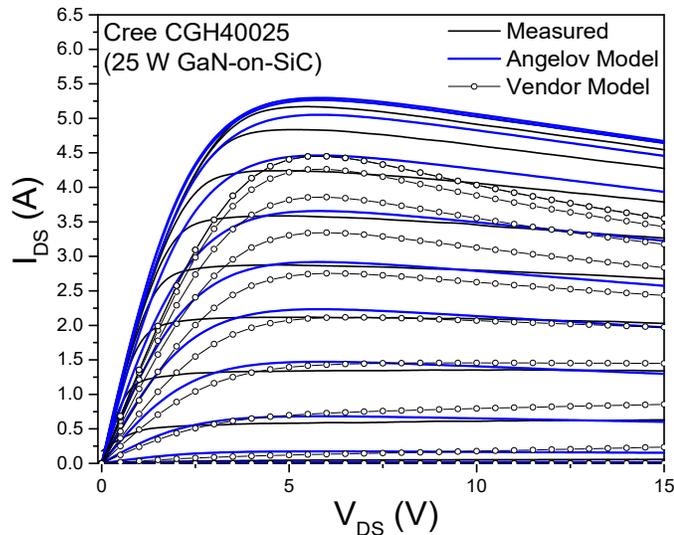


Figure 3.7: Measured and modelled I-V characteristics of Cree CGH40025, a 25 W GaN-on-SiC HEMT.

Figure 3.7 shows measured and modelled I-V characteristics of Cree CGH40025, a 25 W GaN-on-SiC HEMT. The lack of agreement between modelled and measured I-V characteristics in the linear region can be observed, and this is quite challenging. Figure 3.7 also displays the simulated I-V characteristics using the vendor model,

which shows disagreement with measurement. By implementing the analytic approach, the difficulty and inaccuracy of reproducing the device characteristics can be avoided. Besides, the analytic approach has only 19 parameters in the expressions. Thus, extracting a large number of parameter values or optimizing a lot fitting coefficients can also be avoided. As a result, this method is a simple and fast way to obtain the optimum impedance values and predict the RF performance with considerable accuracy.

References

- [3.1] W. Shockley, "A unipolar 'field-effect' transistor," *Proc. IRE*, vol. 40, no. 11, pp. 1365–1376, November 1952.
- [3.2] J. R. Hauser, "Small signal properties of field effect devices," in *IEEE Transactions on Electron Devices*, vol. 12, no. 12, pp. 605-618, December 1965.
- [3.3] K. Lehovec and R. Zuleeg, "Voltage-Current Characteristics of GaAs J-FETs in the Hot Electron Range," *Solid-State Electronics*, vol. 13, issue 10, October 1970, pp. 1415-1424.
- [3.4] H. Shichman and D. A. Hodges, "Modeling and simulation of insulated-gate field-effect transistor switching circuits," in *IEEE Journal of Solid-State Circuits*, vol. sc-3, pp. 285–289, September 1968.
- [3.5] R. L. Van Tuyl, "The Early Days of GaAs ICs," *Technical Digest - IEEE Compound Semiconductor Integrated Circuit Symposium CSICS 2010*, Monterey, California, USA , October 2010.
- [3.6] R. L. Van Tuyl and C. A. Leichti, "Technical Report AFAL-TR-74-40, Air Force Avionics Lab., Contract No. F33615-73-C-1242," March 1974.
- [3.7] W. R. Curtice, "A MESFET Model for Use in the Design of GaAs Integrated Circuits," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 28, no. 5, pp. 448-456, May 1980.
- [3.8] I. Angelov, H. Zirath and N. Rosman, "A new empirical nonlinear model for HEMT and MESFET devices," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 40, no. 12, pp. 2258-2266, December 1992.

- [3.9] Keysight Technologies (formerly Agilent Technologies), “Agilent 85190A IC-CAP Reference,” Palo Alto, California, USA, 2006. [Online]. Available: <http://cp.literature.agilent.com/litweb/pdf/iccap2006/pdf/icref.pdf>.
- [3.10] M. Golio, L. Dunleavy and T. Gneiting, “History and state-of-the-art in large signal modeling for RF/microwave power amplifier development,” *2015 IEEE MTT-S International Microwave Symposium*, Phoenix, AZ, 2015, pp. 1-4.
- [3.11] M. Golio and J. Golio, *RF and Microwave Circuits, Measurements, and Modelling*, Second Edition, Boca Raton, Florida, CRC Press, Taylor & Francis Group, 2008.
- [3.12] P. A. Sandborn, J. R. East and G. I. Haddad, “Quasi-two-dimensional modeling of GaAs MESFET's,” in *IEEE Transactions on Electron Devices*, vol. 34, no. 5, pp. 985-991, May 1987.
- [3.13] C. M. Snowden and R. R. Pantoja, “Quasi-two-dimensional MESFET simulations for CAD,” in *IEEE Transactions on Electron Devices*, vol. 36, no. 9, pp. 1564-1574, September 1989.
- [3.14] X. Cheng, M. Li and Y. Wang, “Physics-Based Compact Model for AlGaIn/GaN MODFETs With Close-Formed I - V and C - V Characteristics,” in *IEEE Transactions on Electron Devices*, vol. 56, no. 12, pp. 2881-2887, Dec. 2009.
- [3.15] D. Hou, G. L. Bilbro, and R. J. Trew, “Analytic model for conduction current in AlGaIn/GaN HFETs/HEMTs,” *Active and Passive Electronic Components*, vol. 2012, Article ID 806253, 11 pages, 2012.
- [3.16] D. Hou, G. L. Bilbro, and R. J. Trew, “A compact physical AlGaIn/GaN HFET model,” in *IEEE Transactions on Electron Devices*, vol. 60, no. 2, pp. 639–645, February 2013.
- [3.17] S. Khandelwal and T. A. Fjeldly, “A physics based compact model of I-V and C-V characteristics in AlGaIn/GaN HEMT devices,” *Solid-State. Electronics*, vol. 76, pp. 60–66, 2012.
- [3.18] R. J. Trew, “AlGaIn/GaN HFET models and the prospects for physics-based compact models,” *Technical Digest - IEEE Compound Semiconductor Integrated Circuit Symposium CSICS 2010*, Monterey, California, USA, October 2010, pp. 7 - 10.

- [3.19] H. Yin, G. L. Bilbro and R. J. Trew, "A new physics-based compact model for AlGaN/GaN HFETs," *2007 IEEE/MTT-S International Microwave Symposium*, Honolulu, HI, 2007, pp. 787-790.
- [3.20] D. E. Root, S. Fan, and J. Meyer, "Technology Independent Large Signal Non Quasi-Static FET Models by Direct Construction from Automatically Characterized Device Data," in *Proceedings of 21st European Microwave Conference 1991*, vol. 2, no. 1, pp. 927–932, 1991.
- [3.21] G. Werthof, A.; Kompa, "A Unified Consistent DC To RF Large Signal Fet Model Covering the Strong Dispersion Effects of HEMT Devices," in *Proceedings of 22nd European Microwave Conference 1992*, pp. 1091–1096, 1992.
- [3.22] R. R. Daniles, A. T. Yang, and J. P. Harrang, "A Universal Large/Small Signal 3-Terminal FET Model Using a Nonquasi-Static Charge-Based Approach," in *IEEE Transactions on Electron Devices*, vol. 40, no. 10, pp. 1723–1729, 1993.
- [3.23] A. Rofougaran and A. A. Abidi, "A table lookup FET model for accurate analog circuit simulation," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 12, no. 2, pp. 324-335, February 1993.
- [3.24] I. Schmale and G. Kompa, "Integration of thermal effects into a table-based large-signal FET model," *Microwave Conference, 1998. 28th European*, Amsterdam, Netherlands, 1998, pp. 102-107.
- [3.25] I. Angelov, "An Empirical Table-Based FET Model," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 47, no. 12, pp. 2350–2357, 1999.
- [3.26] M. Fernández-Barciela, P. J. Tasker, Y. Campos-Roca, M. Demmler, H. Massler, E. Sánchez, M. Carmen Currás-Francos, and M. Schlechtweg, "A simplified broad-band large-signal nonquasi-static table-based fet model," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 48, no. 3, pp. 395–405, 2000.
- [3.27] A. Jarndal and G. Kompa, "Large-signal model for AlGaN/GaN HEMTs accurately predicts trapping- and self-heating-induced dispersion and intermodulation distortion," in *IEEE Transactions on Electron Devices*, vol. 54, no. 11, pp. 2830–2836, 2007.
- [3.28] M. C. Curras-Francos, P. J. Tasker, M. Fernandez-Barciela, S. S. O'Keefe, Y. Campos-Roca and E. Sanchez, "Direct extraction of nonlinear FET I-V functions from

time domain large signal measurements,” in *Electronics Letters*, vol. 34, no. 21, pp. 1993-1994, 15 Oct 1998.

[3.29] M. C. Currás-Francos, P. J. Tasker, M. Fernandez-Barciela, Y. Campos-Roca and E. Sanchez, “Direct extraction of nonlinear FET Q-V functions from time domain large signal measurements,” in *IEEE Microwave and Guided Wave Letters*, vol. 10, no. 12, pp. 531-533, Dec 2000.

[3.30] J. Benedikt, R. Gaddi, P. J. Tasker, and M. Goss, “High-power time-domain measurement system with active harmonic load-pull for high-efficiency base-station amplifier design,” in *IEEE Transactions on Microwave Theory and Techniques*, vol. 48, no. 12, pp. 2617–2624, 2000.

[3.31] H. Qi, J. Benedikt and P. Tasker, “Direct extraction of large-signal table-based behavioural models from time-domain voltage and current waveforms,” *High Frequency Postgraduate Student Colloquium*, 2005, 2005, pp. 25-28.

[3.32] M. C. Currás-Francos, “Table-based nonlinear HEMT model extracted from time-domain large-signal measurements,” in *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 5, pp. 1593–1600, 2005.

[3.33] Q.-J. Zhang, K. C. Gupta, and V. K. Devabhaktuni, “Artificial Neural Networks for RF and Microwave Design-From Theory to Practice,” in *IEEE Transactions on Microwave Theory and Techniques*, vol. 51, no. 4, pp. 1339–1350, 2003.

[3.34] V. Devabhaktuni, M. Yagoub, Y. Fang, J. Xu, and Q.-J. Zhang, “Neural networks for microwave modeling: Model development issues and nonlinear modeling techniques,” *International Journal of RF and Microwave Computer-Aided Engineering*, vol. 11, issue 1, pp. 4–21, January 2001.

[3.35] A. H. Zaabab, Qi-Jun Zhang and M. Nakhla, “Application of neural networks in circuit analysis,” in *Proceedings., IEEE International Conference on Neural Networks*, 1995., Perth, WA, 1995, pp. 423-426 vol.1.

[3.36] A. H. Zaabab, Q. J. Zhang and M. Nakhla, “Analysis and optimization of microwave circuits and devices using neural network models,” *Microwave Symposium Digest, 1994., IEEE MTT-S International*, San Diego, CA, USA, 1994, pp. 393-396 vol.1.

- [3.37] A. H. Zaabab and M. Nakhla, "A neural network modeling approach to circuit optimization and statistical design," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 43, no. 6, pp. 1349–1358, 1995.
- [3.38] K. Shirakawa, M. Shimiz, N. Okubo, and Y. Daido, "A Large-Signal Characterization of an HEMT Using a Multilayered Neural Network," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 45, no. 9, pp. 1630–1633, 1997.
- [3.39] J. Rousset, Y. Harkouss, J. M. Collantes and M. Campovecchio, "An accurate neural network model of FET for intermodulation and power analysis," in *Proceedings of 26th European Microwave Conference*, pp. 16-19, Sept. 1996.
- [3.40] A. Zarate-de Landa, P. Roblin, J. A. Reynoso-Hernandez and J. R. Loo-Yau, "Modeling the I-V Curves and Its Derivatives of Microwave Transistors Using Neural Networks," in *IEEE Microwave and Wireless Components Letters*, vol. 22, no. 9, pp. 468-470, Sept. 2012.
- [3.41] J. Xu, D. Gunyan, M. Iwamoto, A. Cognata and D. E. Root, "Measurement-Based Non-Quasi-Static Large-Signal FET Model Using Artificial Neural Networks," *2006 IEEE MTT-S International Microwave Symposium Digest*, San Francisco, CA, 2006, pp. 469-472.
- [3.42] J. Gao, L. Shen and D. Luo, "High frequency HEMT modeling using artificial neural network technique," *2015 IEEE MTT-S International Conference on Numerical Electromagnetic and Multiphysics Modeling and Optimization (NEMO)*, Ottawa, ON, 2015, pp. 1-3.
- [3.43] H. Kabir, L. Zhang, M. Yu, P. H. Aaen, J. Wood and Q. J. Zhang, "Smart Modeling of Microwave Devices," in *IEEE Microwave Magazine*, vol. 11, no. 3, pp. 105-118, May 2010.
- [3.44] A. H. Jarndal, O. A. Alhammedi and R. H. Al-Ali, "GaN power amplifiers design using genetic neural network model," *Communications, Signal Processing, and their Applications (ICCSPA), 2015 International Conference on*, Sharjah, 2015, pp. 1-6.
- [3.45] A. D. Huang, Z. Zhong, W. Wu and Y. X. Guo, "An Artificial Neural Network-Based Electrothermal Model for GaN HEMTs With Dynamic Trapping Effects

Consideration,” in *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 8, pp. 2519-2528, August 2016.

[3.46] D. E. Root, J. Verspecht, D. Sharrit, J. Wood, and A. Cognata, “Broad-band Poly-Harmonic Distortion (PHD) behavioral models from fast automated simulations and large-signal vectorial network measurements,” in *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 11, pp. 3656–3664, 2005.

[3.47] J. Verspecht and D. E. Root, “Polyharmonic distortion modeling,” in *IEEE Microwave Magazine*, vol. 7, no. 3, pp. 44-57, June 2006.

[3.48] J. Verspecht, D. Gunyan, J. Horn, J. Xu, A. Cognata and D. E. Root, “Multi-tone, Multi-port, and Dynamic Memory Enhancements to PHD Nonlinear Behavioral Models from Large-signal Measurements and Simulations,” *2007 IEEE/MTT-S International Microwave Symposium*, Honolulu, HI, 2007, pp. 969-972.

[3.49] D. E. Root, J. Horn, L. Betts, C. Gillease, and J. Verspecht, “X-parameters: The new paradigm for measurement, modeling, and design of nonlinear RF and microwave components,” *Microwave Engineering Europe*, December 2008 pp 16-21.

[3.50] J. Horn, D. Gunyan, L. Betts, C. Gillease, J. Verspecht and D. E. Root, “Measurement-based large-signal simulation of active components from automated nonlinear vector network analyzer data via X-parameters,” *Microwaves, Communications, Antennas and Electronic Systems, 2008. COMCAS 2008. IEEE International Conference on*, Tel-Aviv, 2008, pp. 1-6.

[3.51] C. S. Chiu, K. M. Chen, G. W. Huang, C. H. Hsiao, K. H. Liao, W. L. Chen, S. C. Wang, M. Y. Chen, Y. C. Yang, K. L. Wang, and L. K. Wu, “Characterization of annular-structure RF LDMOS transistors using polyharmonic distortion model,” *Microwave Symposium Digest, 2009. MTT '09. IEEE MTT-S International*, Boston, MA, 2009, pp. 977-980.

[3.52] G. Simpson, J. Horn, D. Gunyan and D. E. Root, “Load-pull + NVNA = enhanced X-parameters for PA designs with high mismatch and technology-independent large-signal device models,” *Microwave Measurement Symposium, 2008 72nd ARFTG*, Portland, OR, 2008, pp. 88-91.

- [3.53] D. E. Root, J. Xu, J. Horn, M. Iwamoto and G. Simpson, "Device modeling with NVNAs and X-parameters," *Integrated Nonlinear Microwave and Millimeter-Wave Circuits (INMMIC), 2010 Workshop on*, Goteborg, 2010, pp. 12-15.
- [3.54] J. Horn, D. E. Root and G. Simpson, "GaN Device Modeling with X-Parameters," *2010 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, Monterey, CA, 2010, pp. 1-4.
- [3.55] D. Gunyan, J. Horn, J. Xu and D. E. Root, "Nonlinear validation of arbitrary load X-parameter and measurement-based device models," *Microwave Measurement Conference, 2009 73rd ARFTG*, Boston, MA, 2009, pp. 1-4.
- [3.56] L. Sang, Y. Xu, Y. Chen, Y. Guo, and R. Xu, "Large signal equivalent circuit model for package ALGaN/GaN HEMT," *Progress In Electromagnetics Research Letters*, vol. 20, no. January, pp. 27–36, 2011.
- [3.57] L. Dunleavy, C. Baylis, W. Curtice and R. Connick, "Modeling GaN: Powerful but Challenging," in *IEEE Microwave Magazine*, vol. 11, no. 6, pp. 82-96, Oct. 2010.
- [3.58] W. R. Curtice and M. Ettenberg, "A Nonlinear GaAs FET Model for Use in the Design of Output Circuits for Power Amplifiers," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 33, no. 12, pp. 1383–1394, 1985.
- [3.59] I. Angelov, K. Andersson, D. Schreurs, D. Xiao, N. Rorsman, V. Desmaris, M. Sudow, and H. Zirath, "Large-signal modelling and comparison of AlGaIn/GaN HEMTs and SiC MESFETs," *2006 Asia-Pacific Microwave Conference*, Yokohama, 2006, pp. 279-282.
- [3.60] W. R. Curtice, "GaAs MESFET modeling and nonlinear CAD," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 36, no. 2, pp. 220-230, Feb 1988.
- [3.61] H. Statz, P. Newman, I. W. Smith, R. A. Pucel and H. A. Haus, "GaAs FET device and circuit simulation in SPICE," in *IEEE Transactions on Electron Devices*, vol. 34, no. 2, pp. 160-169, Feb 1987.
- [3.62] T. Kacprzak and A. Materka, "Compact DC Model of GaAs FET's for Large-Signal Computer Calculation," in *IEEE Journal of Solid-State Circuits*, vol. 18, no. 2, pp. 211–213, 1983.

- [3.63] J. Rodriguez-Tellez and P. J. England, "Five-parameter DC GaAs MESFET model for nonlinear circuit design," in *IEE Proceedings G - Circuits, Devices and Systems*, vol. 139, no. 3, pp. 325-332, June 1992.
- [3.64] I. Angelov, L. Bengtsson and M. Garcia, "Extensions of the Chalmers nonlinear HEMT and MESFET model," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 44, no. 10, pp. 1664-1674, Oct 1996.
- [3.65] M. Miller, M. Golio, B. Beckwith, E. Arnold, D. Halchin, S. Ageno, and S. Dorn, "Choosing an optimum large signal model for GaAs MESFETs and HEMTs," *Microwave Symposium Digest, 1990., IEEE MTT-S International*, Dallas, TX, 1990, pp. 1279-1282 vol.3.
- [3.66] R. Touhami, M. C. E. Yagoub, and H. Baudrand, "Comparing the MESFET and HEMT models for efficient circuit design," in *International Journal of Numerical Modeling Electronic Networks, Devices and Fields*, vol. 20, issue. 3, pp. 149-161, March 2007.
- [3.67] J. Castelino, P. Wong, E. Sijercic, B. Pejcinovic and A. Baric, "Comparison of non-linear MESFET models over 1-12 GHz frequency range," in *Proceedings of the 2003 10th IEEE International Conference on Electronics, Circuits and Systems, 2003. ICECS 2003.*, 2003, pp. 487-490 Vol.2.
- [3.68] J. R. Tellez, M. Al-Daas, and K. A. Mezher, "Comparison of Nonlinear MESFET Models for Wideband Circuit Design," in *IEEE Transactions on Electron Devices*, vol. 41, no. 3, pp. 288-293, 1994.
- [3.69] E. Sijercic and B. Pejcinovic, "Comparison of non-linear MESFET models," *9th International Conference on Electronics, Circuits and Systems*, 2002, pp. 1187-1190 vol.3.
- [3.70] S. A. Maas, *Nonlinear Microwave and RF Circuits*. Artech House, INC, 2003.
- [3.71] R. Vetry, N. Q. Zhang, S. Keller, and U. K. Mishra, "The impact of surface states on the DC and RF characteristics of AlGaIn/GaN HFETs," in *IEEE Transactions on Electron Devices*, vol. 48, no. 3, pp. 560-566, 2001.
- [3.72] G. Koley, V. Tilak, L. F. Eastman, and M. G. Spencer, "Slow transients observed in AlGaIn/GaN HFETs: Effects of SiNx passivation and UV illumination," in *IEEE Transactions on Electron Devices*, vol. 50, no. 4, pp. 886-893, 2003.

- [3.73] B. M. Green, K. K. Chu, E. M. Chumbes, J. A. Smart, J. R. Shealy and L. F. Eastman, "The effect of surface passivation on the microwave characteristics of undoped AlGaIn/GaN HEMTs," in *IEEE Electron Device Letters*, vol. 21, no. 6, pp. 268-270, June 2000.
- [3.74] A. Vertiatchikh, L. F. Eastman, W. J. Schaff and I. Prunty, "Effect of surface passivation of AlGaIn/GaN heterostructure field-effect transistor," in *Electronics Letters*, vol. 38, no. 8, pp. 388-389, 11 Apr 2002.
- [3.75] K. Horio, A. Nakajima, and K. Itagaki, "Analysis of field-plate effects on buffer-related lag phenomena and current collapse in GaN MESFETs and AlGaIn/GaN HEMTs," *Semiconductor Science and Technology*, vol. 24, no. 8, p. 85022 (1-7), July 2009.
- [3.76] K. Koh, H. M. Park, and S. Hong, "A spline large-signal FET model based on bias-dependent pulsed I-V measurement," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 11, pp. 2598-2603, November 2002.
- [3.77] R. G. Brady, G. Rafael-Valdivia and T. J. Brazil, "Large-Signal FET Modeling based on Pulsed Measurements," *2007 IEEE/MTT-S International Microwave Symposium*, Honolulu, HI, 2007, pp. 593-596.
- [3.78] A. M. Conway and P. M. Asbeck, "Virtual Gate Large Signal Model of GaN HFETs," *2007 IEEE/MTT-S International Microwave Symposium*, Honolulu, HI, 2007, pp. 605-608.
- [3.79] O. Jardel, F. De Groote, T. Reveyrand, J. C. Jacquet, C. Charbonniaud, J. P. Teyssier, D. Floriot, and R. Quéré, "An electrothermal model for AlGaIn/GaN power HEMTs including trapping effects to improve large-signal simulation results on high VSWR," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, no. 12, pp. 2660-2669, 2007.
- [3.80] L. S. Liu, J. G. Ma, and G. I. Ng, "Electrothermal large-signal model of III-V FETs accounting for frequency dispersion and charge conservation," *IEEE MTT-S International Microwave Symposium Digest*, vol. 57, no. 12, pp. 749-752, 2009.
- [3.81] I. Angelov, M. Thorsell, K. Andersson, N. Rorsman, E. Kuwata, H. Ohtsuka, and K. Yamanaka, "On the large-signal modeling of High Power AlGaIn/GaN

HEMTs,” *2012 IEEE MTT-S International Microwave Symposium Digest (MTT)*, Montreal, QC, Canada, 2012, pp. 1-3.

[3.82] A. Jarndal, S. Pillai, H. Abdulqader, and G. Kompa, “On the large-signal modeling of AlGaN/GaN devices using genetic neural networks,” in *the Proceedings of 2012 7th European Microwave Integrated Circuits Conference, EuMIC 2012*, Amsterdam, 2012, pp. 60–63.

[3.83] G. Torregrosa, J. Grajal, M. Peroni, A. Serino, A. Nanni and A. Cetronio, “Large-Signal modeling of power GaN HEMTs including thermal effects,” *2007 European Microwave Integrated Circuit Conference, EuMIC 2007*, Munich, 2007, pp. 36-39.

[3.84] Y. Liu and E. Reese, “AlGaN/GaN HEMT Large Signal Nonlinear Compact Model Accounting for Thermal Effects and Trapping Dispersion,” *2013 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, Monterey, CA, 2013, pp. 1-5.

[3.85] A. Santarelli, D. Niessen, R. Cignani, G. P. Gibiino, P. A. Traverso, C. Florian, D. Schreurs, and F. Filicori, “Large-signal GaN transistor characterization and modeling including charge trapping nonlinear dynamics,” *2014 IEEE MTT-S International Microwave Symposium (IMS2014)*, Tampa, FL, 2014, pp. 1-3.

[3.86] C. Wang, Y. Xu, X. Yu, C. Ren, Z. Wang, H. Lu, T. Chen, B. Zhang, and R. Xu, “An Electrothermal Model for Empirical Large- Signal Modeling of AlGaN / GaN HEMTs Including Self-Heating and Ambient Temperature Effects,” in *IEEE Transactions on Microwave Theory and Techniques*, vol. 62, no. 12, pp. 2878–2887, 2014.

[3.87] W. R. Curtice, J. R. Bennett, D. Suda and B. A. Syrett, “Modeling of current lag in GaAs IC's,” *1998 IEEE MTT-S International Microwave Symposium Digest*, Baltimore, MD, USA, 1998, pp. 603-606 vol.2.

Chapter 4

S-Parameter Measurements, Extraction and Small-Signal Modelling of Packaged Radio Frequency Power Transistors

Abstract

This chapter primarily focuses on the extraction of the small-signal equivalent circuit model parameters for GaN HEMT and Si LDMOS RF transistors rating from 2 W to 25 W over a range of frequencies from 200 MHz to 8 GHz. The methodology refers to several extraction processes reported in the literature and is found to be the best approach. It also describes the methods to measure radio frequency power transistors packaged in surface mount technology with coaxial measurement equipment, as well as approaches to remove the effects of measurement errors and test fixture from measured S-parameters. This chapter proposes new models for two GaN HEMT devices which otherwise lack accuracy or do not have any large-signal model supplied by their vendors. The obtained parameter values are validated for the RF devices via a comparison of measured and simulated s-parameters of the small-signal model. The relationships between the device process technology and the extracted parameter values are examined with respect to output power.

4.1 Introduction

Nowadays, many manufacturers offer nonlinear large-signal models for their RF power devices to aid PA designers to prototype amplifiers. These models are still under continuous development, and most of them may often fail to represent the DC and RF characteristics of the device with reasonable accuracy or worst still, wrongly predict the device impedances and their performance in simulation. Examples of such device models explored in the duration of this thesis work include the Mitsubishi MGF0843G, or Nitronex NPTB00025. In the case of the RFHIC RT233, no nonlinear model is available. This thesis has been motivated at a time when GaN technology for RFPA applications is still in the process of making inroads into the market, and therefore requires a need for a sound characterisation and modelling capability. It is always an important and equally difficult task to decide on a part number for a given amplifier application, since the accuracy of the model is not easy to ascertain a priori.

In this chapter the correlation between the device cross-section and the equivalent circuit model is highlighted. In order to characterize and extract the parameter values to construct an accurate model of a device, accurate measurement is imperative. However, the measurement can be affected by various errors. The sources of these errors and different correction procedures to remove them are discussed. Numerous parameter extraction procedures have been proposed in the literature. The method implemented in this thesis is a combination of several techniques and found to be the best approach. The obtained parameter values are then validated for commercial RF devices via a comparison of measured and simulated s-parameters of the small-signal model.

4.2 Small-Signal Equivalent Circuit Model

Figure 4.1 shows a lumped element small-signal equivalent circuit model [4.1], [4.2] used in this thesis for modelling RF power devices.

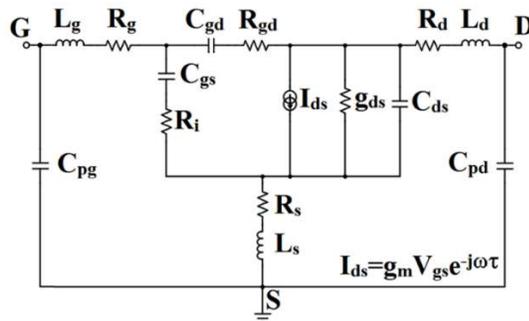


Figure 4.1: A small-signal equivalent model [4.1], [4.2].

The equivalent small-signal model can be divided into two parts:

1. Intrinsic elements, which include forward transconductance (g_m) of the nonlinear current generator, output conductance (g_{ds}), intrinsic capacitances C_{gs} , C_{gd} , C_{ds} , access resistances R_i and R_{gd} , are bias-dependent and therefore their values are extracted from measurements at bias conditions of interest. The resistances R_i and R_{gd} are relevant only for a GaN HEMT, but not an LDMOS.
2. Extrinsic elements are the series inductances (L_s , L_d , L_g) and resistances (R_s , R_d , R_g) and parasitic pad capacitances (C_{pg} , C_{pd}). These elements are independent of biasing condition.

At higher frequency, the device displays more parasitic effects. The state of the art in small-signal modelling proposed by Jing et al. [4.2] and Anwar et al. [4.3] are considered additional lumped elements in their models to accurately describe the device behaviour up to 50 GHz. Since the improvement from these additional elements is observable way beyond the target frequency of this work, a simpler 15-element model [4.2] is considered in this thesis.

4.3 Correlation between Device Structure and Small-Signal Model

The lumped elements in the equivalent circuit model are superimposed on the cross-section of a GaN HEMT device as shown in Figure 4.2.

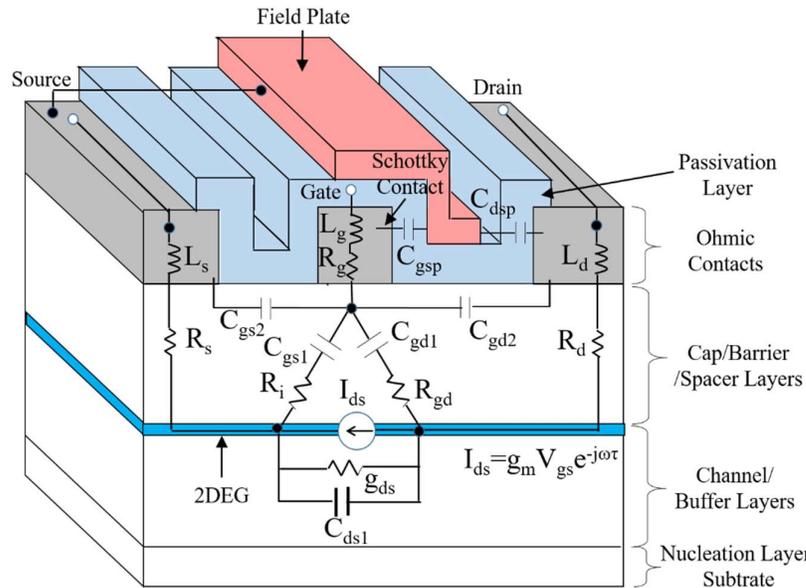


Figure 4.2: Basic device structure and physical correlation of the parameters in the small-signal equivalent circuit for a GaN HEMT.

Pad Capacitance: The capacitances C_{pg} and C_{pd} (not in Figure 4.2) are the capacitance between the contacting bond pads at the gate and drain terminals respectively.

Extrinsic Resistances: The source-to-channel (R_s) and drain-to-channel (R_d) resistances are the accumulation of the resistance due to ohmic contacts, resistance between the metal electrodes and cap layer and also the bulk drift region resistance between the drain contact and the end of the channel. The gate resistance (R_g) is the gate-metal resistance due to the Schottky contact at the gate.

Extrinsic Inductances: The metallization of the gate, drain and source contacts of the device surface respectively give rise to the gate (L_g), drain (L_d) and source (L_s) inductances.

Intrinsic Capacitances: The gate-to-source capacitance (C_{gs}), also known as the input capacitance, depends on the gate-to-channel capacitance through the barrier layer at the gate side (C_{gs1}), the fringing capacitance between gate and source electrodes (C_{gs2}), and the parasitic capacitance between gate and source-terminated field plate (C_{gsp}). The total gate-to-source capacitance is as follows:

$$C_{gs} = C_{gs1} + C_{gs2} + C_{gsp} \quad (4.1)$$

The gate-to-drain capacitance (C_{gd}) depends on the gate-to-channel capacitance through the barrier layer at the drain side (C_{gd1}) and the fringing capacitance between gate and drain electrodes (C_{gd2}) and given by:

$$C_{gd} = C_{gd1} + C_{gd2} \quad (4.2)$$

The capacitance C_{gd} provides a feedback path between the input and output of the device. Therefore, C_{gd} is also called the feedback capacitance. The drain-to-source capacitance (C_{ds1}) is the geometric capacitance between the drain and source electrodes in the buffer layer as shown in Figure 4.2. The parasitic capacitance between drain and source-terminated field plate (C_{dsp}) also contributes to the total value of C_{ds} which is given by:

$$C_{ds} = C_{ds1} + C_{dsp} \quad (4.3)$$

Intrinsic Resistances: The origin of resistances R_i and R_{gd} is related to the resistances from the gate to source and drain respectively, because in a GaN HEMT, the quantum well of charge carriers is separated from the gate by an AlGaIn cap layer. The R_i and

R_{gd} are the intrinsic charging resistances associated with the finite time required by the capacitances C_{gs} and C_{gd} to setup and the time constants are expressed by $R_i C_{gs}$ and $R_{gd} C_{gd}$ respectively. These resistances are also known as access resistance and feedback resistance respectively.

Transconductance Delay: The transconductance delay (τ) is the time taken for g_m to change in response to a change in gate voltage (V_{GS}). In other words, it is the time taken by the channel charge to re-arrange itself when the gate voltage changes.

Transconductance: When the FET is in the saturation region, the drain current I_{DS} is primarily controlled by the gate voltage (V_{GS}). The forward transconductance is determined by differentiating the saturated drain current with respect to the gate voltage for a constant drain voltage and given by.

$$g_m = \frac{\delta I_{DS}}{\delta V_{GS}} \text{ at constant } V_{DS} \quad (4.4)$$

It is a measure of how well the FET can control its drain current by changing the gate voltage. From (4.4), it can be seen that the transconductance, g_m is the slope of the transfer curve or output characteristic curve of a FET and is a measure of its dc gain. It is always desired to be constant over a wide range of V_{GS} since this implies better linearity.

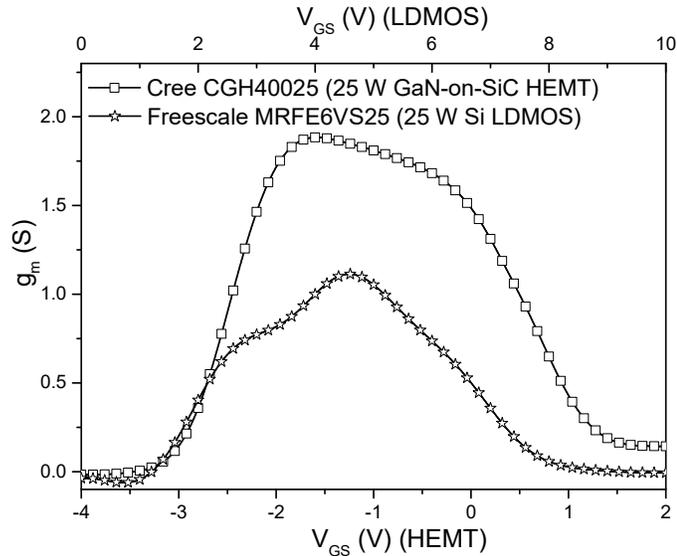


Figure 4.3: Transconductance (g_m) of a 25 W GaN-on-SiC HEMT and a 25 W Si LDMOS as function of gate voltage (V_{GS}).

Figure 4.3 shows the values of g_m from measurement for a 25 W silicon LDMOS (Freescale MRFE6VS25) and a 25 W GaN-on-SiC HEMT (Cree CGH40025). The

nearly constant and higher value of transconductance for the 25 W GaN HEMT over wider range of gate voltages than the 25 W Si LDMOS indicates higher linear output power and gain as would be expected from the material properties.

Output Conductance: Drain or output conductance (g_{ds}) describes how the drain current changes with respect to the change in drain-to-source voltage and given by following equation:

$$g_{ds} = \frac{\delta I_{DS}}{\delta V_{DS}} \quad (4.5)$$

The drain to source resistance (R_{ds}) is the reciprocal of output conductance (g_{ds}). It can be seen from Figure 4.4 that above a drain voltage of 5 V, the g_{ds} has fairly constant value of 0.015 S for the 25W GaN-on-SiC HEMT and 0.003 S for the 25 W Si LDMOS. This is the saturation region where the change in drain current in respect to drain voltage is insignificant.

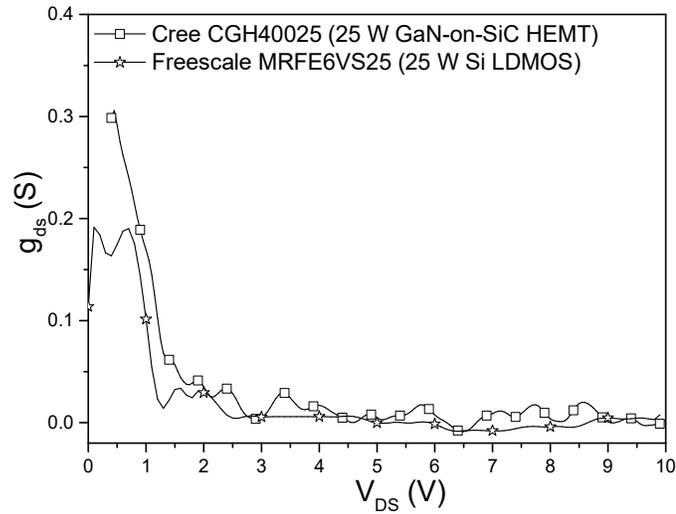


Figure 4.4: Output conductance (g_{ds}) of a 25 W GaN-on-SiC HEMT and a 25 W Si LDMOS as function of drain voltage (V_{DS}).

The output conductance has a strong influence on the intrinsic voltage gain (A_{vi}) of a transistor which is given by:

$$A_{vi} = \frac{g_m}{g_{ds}} = g_m R_{ds} \quad (4.6)$$

The corresponding lower value of R_{ds} in a device with high g_{ds} value results in lower voltage swing at the output and reduces the intrinsic voltage gain. Therefore, the lower value of g_{ds} in 25 W Si LDMOS would allow it to achieve higher intrinsic voltage gain than the 25 W GaN HEMT.

In Figure 4.4, one can notice the ripple in the measured value of output conductance, which can be attributed to measurement errors. The primary sources of errors in I-V measurements are internal system noise, noise due to external electrostatic interference, insufficient settling time between test signal and measurement, resolution of the analog to digital converters, unwanted currents, poor connections and cables, and environmental conditions such as temperature, humidity and light. Although these errors cannot be eliminated completely, the measurement accuracy can be improved by using low noise connections and cables, allowing sufficient settling time, and implementing techniques such as shielding, guarding and proper grounding. The measurement accuracy can also be improved by taking the average of multiple measurements.

In the design process, yield analysis allows to consider these random variations from the nominal value of any parameter and to measure the effects on the performance specifications. The design can be then modified to minimize these effects through yield optimization [4.4].

4.4 Measurement of a Packaged Device

Measurement equipment like a vector network analyser (VNA) has coaxial connectors. However, the circuits used in today's RF and wireless communication systems which are primarily realized via microstrip transmission lines require the devices to be packaged in smaller and integrated ways; this inevitably leads to non-coaxial connectors. Practically all the RF power devices nowadays are packaged using the surface-mount technology (SMT). As a result, a test fixture is required as an interface between the measurement equipment and the device under test (DUT) and also to provide good electrical and mechanical connections. Since the size of these packages varies greatly depending on the device technology and power-rating as well as heat-dissipation and environmental conditions, no single standard fixture is available. This makes designing high quality RF fixtures equally important to accurately measure the device characteristics.

4.4.1 Designing a Test Fixture

An ideal fixture should have a perfect match between the VNA and DUT so that there is no reflection. It should also have flat frequency response with no electrical length and loss in order to avoid distortion of the signal. For consistent data, it should also

have simple and quick connections that are repeatable. Therefore, the goal is to keep the effects of the fixture on measurement at minimum.

4.4.2 Measurement Errors

There are three types of measurement errors.

Drift errors are mainly caused by a change in temperature and can be eliminated by recalibrating the VNA. However, by establishing a steady ambient temperature during calibration and measurement, the drift errors can be reduced or even avoided.

Random errors are unpredictable and can be caused by anything from the quality of the connectors to noise in the equipment and cannot be removed by calibration. The impact of these errors can be minimized by taking average measurements over multiple sweeps, or by reducing the intermediate frequency (IF) bandwidth.

Systematic errors are the primary source of measurement errors which are connected to signal leakage, reflection and frequency response of the system. The six types of system errors, as described in [4.5], are as follows:

- Directivity (E_D) and crosstalk (E_X) errors related to signal leakage.
- Source (E_S) and load (E_L) impedance mismatches relating to reflections.
- Frequency response errors caused by reflection (E_R) and transmission (E_T) tracking with the test receivers.

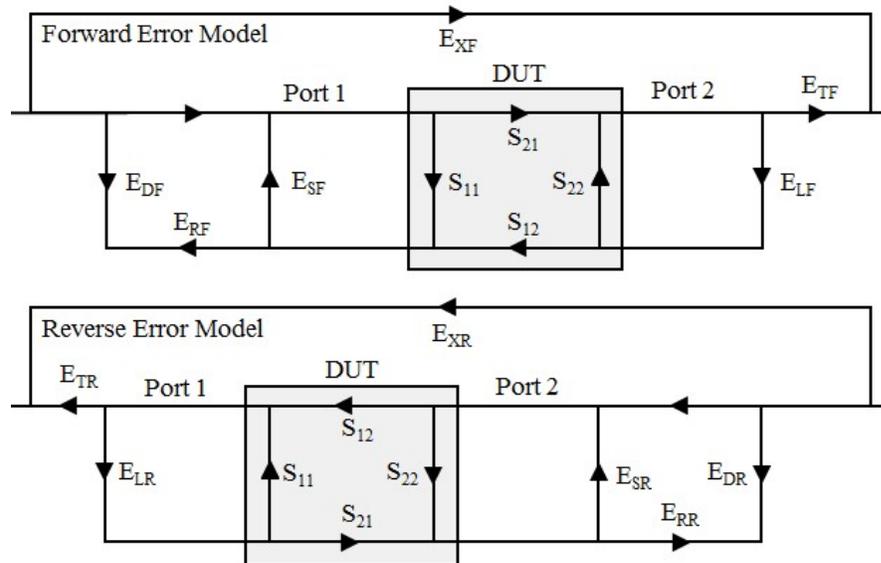


Figure 4.5: 12-term error model for a two-port system.

In two port systems, six errors in forward (F) direction and another six in reverse (R) direction, as shown in Figure 4.5, give rise to a total of 12 error terms.

4.4.3 Calibration

Calibration is a process to remove systematic errors from measurements. There are basically two types of error correction procedures: response calibration and vector error calibration [4.5]. In the response calibration, a reference trace of a calibration standard is stored in system memory and later measured data is divided by the trace for normalization. This is a simple method, but unfortunately it just corrects the frequency response errors out of all the 12 system errors. The vector error correction is a more in-depth method that requires more calibration standards with precisely known electrical characteristics. The VNA then compares the measured data with the standard stored in its memory and calculates the error model. This allows the removal of major systematic errors in measurements.

This pre-measurement process eliminates the errors from the network analyser and any impact from the cables or adapters. Since it does not take the effects of the fixture into account, adding a fixture in the measurement set-up after the calibration introduces errors due to loss, phase shift, and mismatch [4.6] as shown in Figure 4.6. Moreover, the measured data now consists the responses of both DUT and fixture. Therefore, any effect of the fixture must be removed in order to obtain the response of the DUT only.

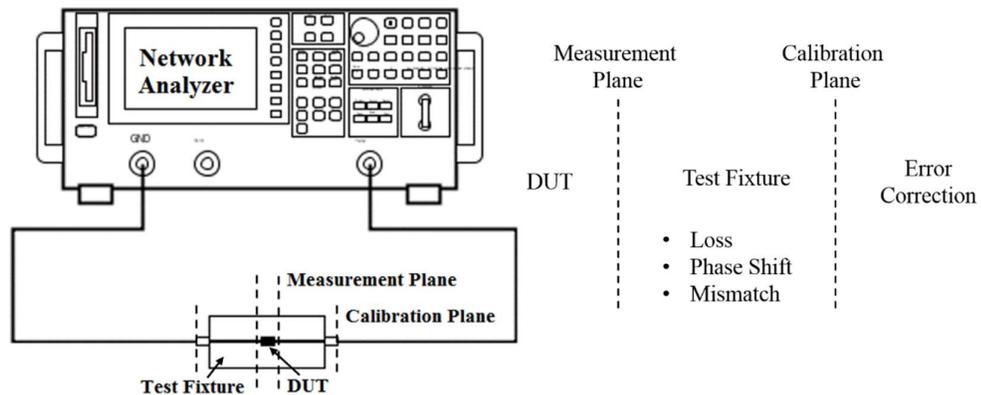


Figure 4.6: Error introduced by the test fixture after calibration

4.4.4 Removing Fixture Errors

The three primary approaches to remove the errors and effects of the fixture are as follows:

4.4.4.1 Modelling

This method requires very good knowledge of fixture characteristics. Usually the fixture is measured in order to obtain a precise model of it. The vector network analyser then applies a mathematical correction based on the model.

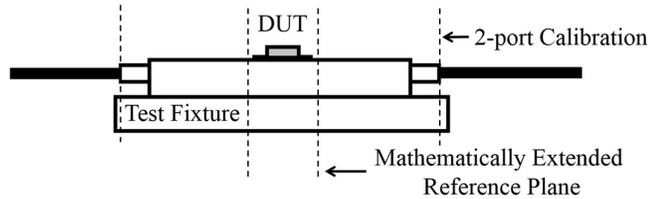


Figure 4.7: Removing fixture errors by mathematically extending the reference plane via modelling. An example of this method is the port extension feature on the VNA. As depicted in Figure 4.7, at first a full 2-port calibration is performed at the end of the coaxial cables. After connecting the fixture, the reference plane is then shifted to the DUT mathematically. This method is based on the assumptions that the fixture has flat magnitude, linear phase, constant impedance and no loss. Therefore, if the quality of the fixture is significantly better than the requirements of the DUT, then this method might be adequate.

4.4.4.2 De-embedding

De-embedding is a process that requires the S-parameters of the fixture (Figure 4.8). Once the S-parameter matrix of the fixture is available, the performance of the DUT can be extracted mathematically from the combined measurement by de-embedding the fixture.

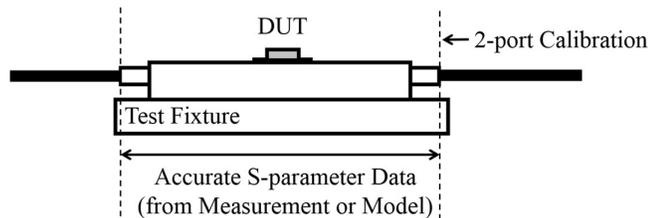


Figure 4.8: Removing fixture errors by de-embedding the fixture.

The two most common ways to acquire these data is from direct measurement or equivalent model of the fixture. The standard practice is to construct a faithful linear model of the fixture in a software like ADS and match it with measured s-parameter data. The de-embedding process involves these following steps [4.7]:

1. First the combined S-parameters of the DUT and fixture are measured.

- The test fixture and the DUT in Figure 4.9 (a) can be considered as a cascaded system of three separate two-port networks as shown in Figure 4.9 (b).

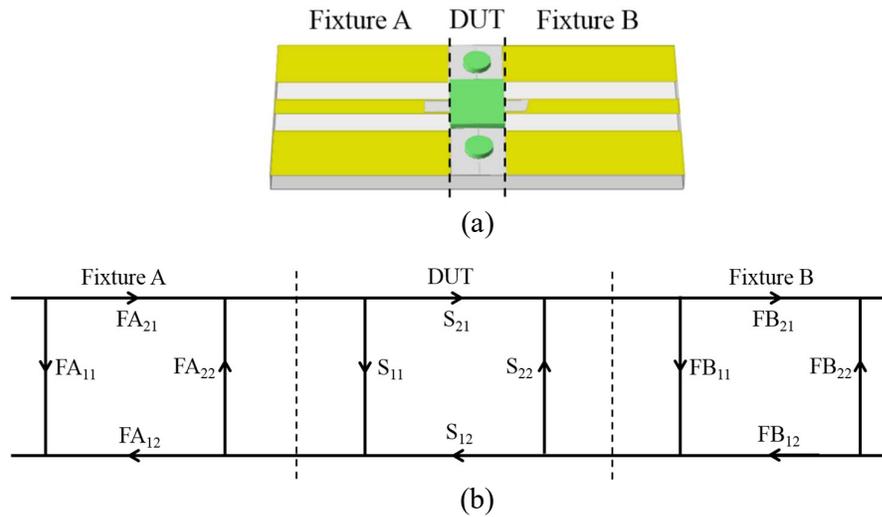


Figure 4.9: Both sides of the test fixture and DUT can be imagined as a cascaded system of three separate two-port networks.

Since each half of the fixture, represented as Fixture A and B, is identical in terms of electrical and mechanical characteristics, the measured data of only one half is sufficient to construct the model of the full fixture. Therefore, half the fixture, designed using a thru line of same length as Fixture A and B, is fabricated and measured as shown in Figure 4.10. A model is constructed in ADS with a coax component for the SMA connector, and a series inductor and a shunt capacitor are used to model the coaxial-to-microstrip transition. Based on the fixture, a microstrip or coplanar waveguide line is used to represent the thru line.

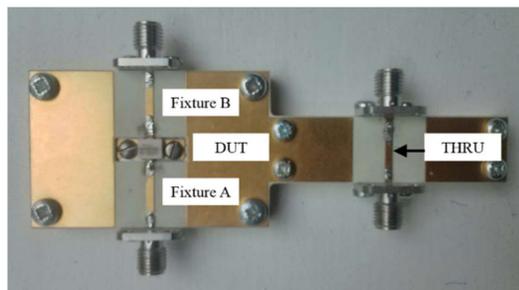


Figure 4.10: Fabricated test fixture.

It is important to include accurate values of thickness, dielectric constant and loss tangent of the substrate material in order to model the transmission line accurately. Table 4.1 shows the physical characteristics of the substrate and SMA connectors and dimension of the coplanar waveguide for the test fixture.

Table 4.1: Physical characteristics of the substrate and SMA connectors and dimension of the coplanar waveguide for the test fixture

Substrate (Rogers 4350B)				
H (mm)	ϵ_r	T (mm)	TanD	
0.508	3.66	0.035	0.0037	
Coplanar Waveguide				
W (mm)	G (mm)	L (mm)		
2.6	6.7	14		
SMA Connector				
Di (mm)	Do (mm)	L (mm)	ϵ_r	TanD
1.275	4.15	7.6	2.1	0.001

Figure 4.11 shows the schematic of the modelled test fixture in ADS. The values of inductance and capacitance are optimized until a match is obtained between the measured and simulated S-parameters of the fixture.

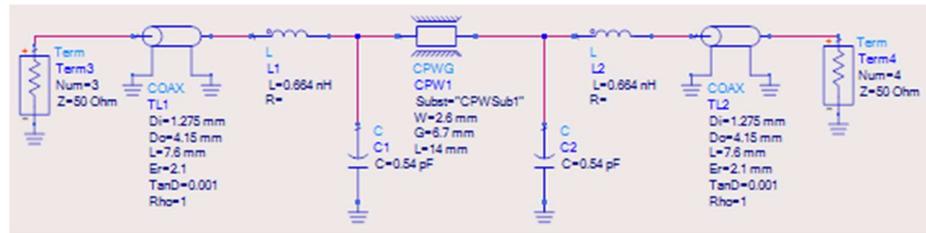


Figure 4.11: Schematic diagram of the designed test fixture in ADS.

Figure 4.12 shows the measured and modelled return and insertion losses of the test fixture from 200 MHz to 4 GHz. This agreement ensures the accuracy of the model for this range of frequency.

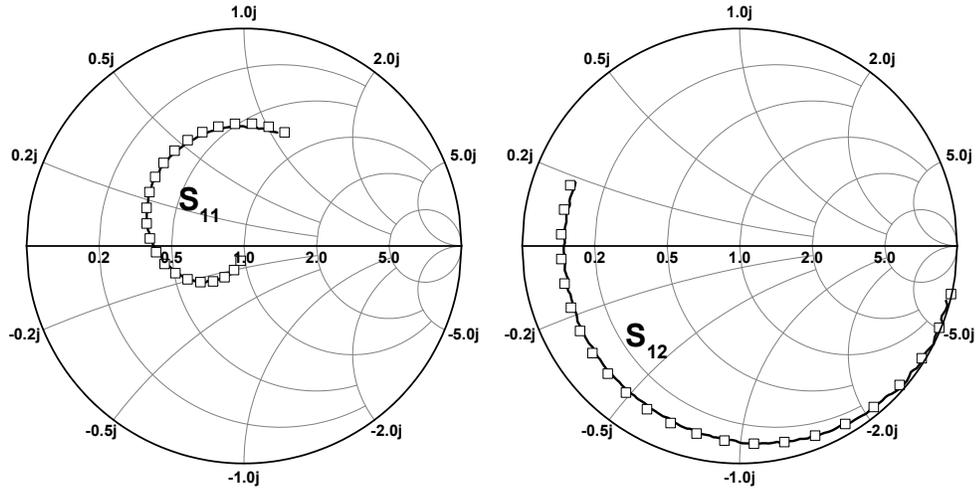


Figure 4.12: Comparison of measured (line) and modelled (symbol) return (S_{11}) and insertion losses (S_{12}) of the test fixture from 200 MHz to 4 GHz.

3. For convenience, the S-parameters are converted into T-parameters.

$$[T_{measured}] = [T_{FA}] [T_{DUT}] [T_{FB}] \quad (4.7)$$

Both sides of (4.7) are then multiplied by the inverse T-parameter matrix of half the fixture to obtain the T-parameter for the DUT only.

$$[T_{FA}][T_{FA}]^{-1}[T_{DUT}][T_{FB}][T_{FB}]^{-1} = [T_{DUT}] \quad (4.8)$$

4. The de-embedded T-parameters of the DUT are now reconverted into S-parameters.

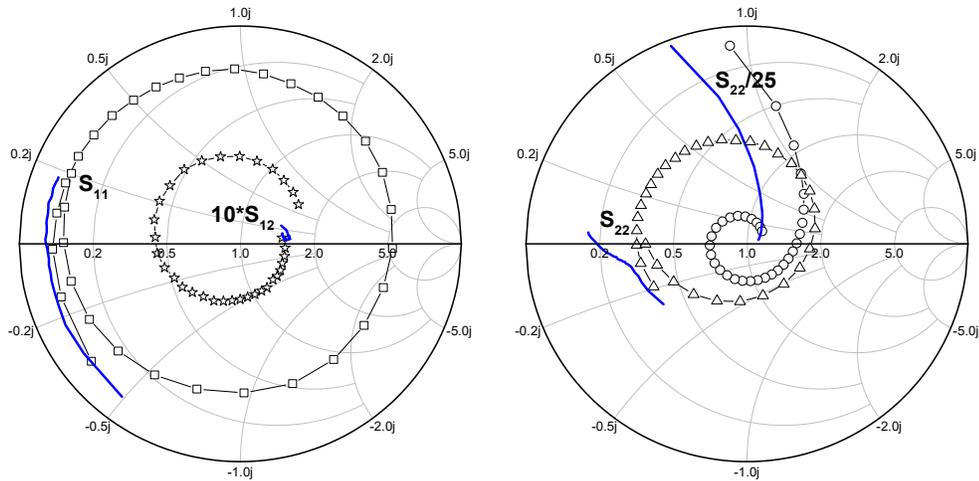


Figure 4.13: Measured S-parameters before (symbol) and after (line) de-embedding of the test fixture.

Figure 4.13 shows measured S-parameters before and after de-embedding. The overall accuracy of the de-embedding process strongly depends on the accuracy of the fixture model. A simplified lumped element based model such as this does not take nonlinear effects into account, and is therefore effective for a limited frequency range, such as 200 MHz to 4 GHz in this case, but not for broadband S-parameter measurements [4.8] over a frequency range of 200 MHz to 8 GHz.

4.4.4.3 Direct Measurement Technique

The direct measurement technique involves in-fixture calibration, which means calibration standards are measured in place of the DUT and errors terms are calculated. As a result, the measurement plane and the calibration plane are same as shown in Figure 4.14. This allows to directly measure the response of the DUT. The accuracy of this method relies on the quality of the calibration standards and precise knowledge of their characteristics.

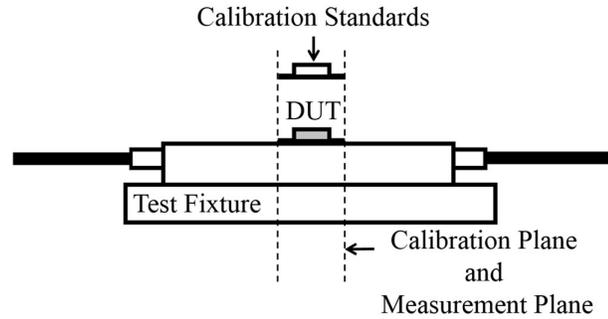


Figure 4.14: In direct measurement approach the calibration plane is same as the measurement plane. This allows to perform the calibration at the end of test fixture.

The most commonly used in-fixture calibrations are full 2-port SOLT (short, open, load, thru) and TRL (thru, reflect, line) calibration techniques. A full 2-port calibration removes all the twelve error terms and allows maximum possible accuracy in measurements. The choice of calibration depends on both accuracy and ease-of-use. A comparison of measurement uncertainty for various calibration kits in [4.9] shows that TRL calibration technique provides better quality of calibration than SOLT calibration technique. In addition, realizing high-quality SOLT standards becomes challenging as the frequency increases [4.10]. In particular, it is difficult to fabricate a purely resistive load standard with excellent quality [4.11]. On the other hand, TRL calibration techniques has only three standards which have less stringent requirements and can be easily fabricated [4.11]. In this thesis, SOLT calibration and de-embedding method are used up to 4 GHz and direct measurement technique using TRL calibration are used above 4 GHz and up to 8 GHz to obtain the device S-parameters.

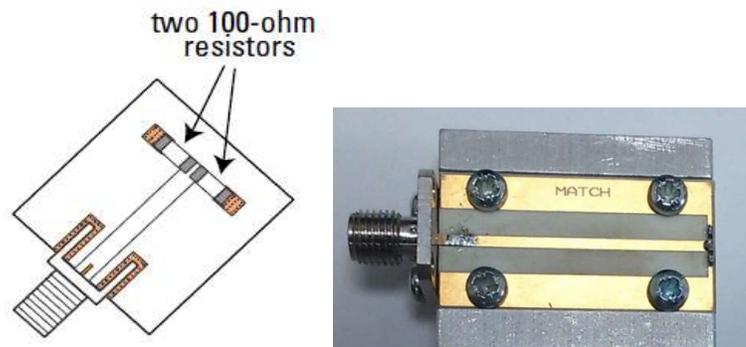
4.4.4.3.1 Designing TRL Calibration Standards

The design of TRL calibration standards should satisfy specific requirements as mentioned in Table 4.2 [4.10]. In addition, the usable bandwidth of this method for a thru/line pair is only 8:1 (frequency span: start frequency). Therefore, sometimes it is necessary to use multiple lines to extend the bandwidth. In addition, it is difficult to design the line standard for low frequency range since the physical length of the standard becomes very long. Therefore, in the low frequency range a match standard is used instead. So this particular calibration technique is basically a combination of “TRM (THRU, REFLECT, MATCH)” and “TRL (THRU, REFLECT, LINE)” calibration techniques for frequency range of 0 - 2 GHz and 2 GHz – 18 GHz respectively.

Table 4.2: Requirements for the thru-reflect-line (TRL) calibration standards

Standard	Requirements
THRU (Zero Length)	No loss and no characteristic impedance. $S_{21}=S_{12}=1$ at 0° and $S_{11}=S_{22}=0$.
REFLECT	Reflection coefficient (Γ) must be identical on both ports. Its magnitude is optimally 1, but does not need to be known. On the other hand, the phase of Γ must be known within $\frac{1}{4}$ wavelength or 90° .
LINE	Characteristic impedance (Z_0) on the line establishes the reference impedance of the measurement, and ideally should be same as the Z_0 (50Ω) of the system. The insertion phase of the line must not be the same as the thru and the difference between the line and the thru must be between 20° and $160^\circ \pm n \times 180^\circ$ where n is an integer.

MATCH: The MATCH standard is designed by adding two $100\ \Omega$ resistors in parallel at the end of a $50\ \Omega$ transmission line as shown in Figure 4.15. The transmission line has the same length as the REFLECT standard.

**Figure 4.15:** Fabricated MATCH standard.

THRU: Although the characteristic impedance of the thru is not needed to be known, in order to reduce any reflection during coaxial to transmission line transition, this standard is designed to have an impedance of $50\ \Omega$. It is easily done using the “LineCalc” tool in Advanced Design System (ADS) [4.12]. The fabricated thru standard can be seen in Figure 4.16. Table 4.3 shows the physical characteristics of the substrate and dimension of the coplanar waveguide for thru standard.

Table 4.3: THRU standard

Substrate (Rogers 4350B)				
H (mm)	ϵ_r	T (mm)	TanD	
0.508	3.66	0.035	0.0037	
Coplanar Waveguide				
W (mm)	G (mm)	L (mm)		
1.3	3.1	63.5		

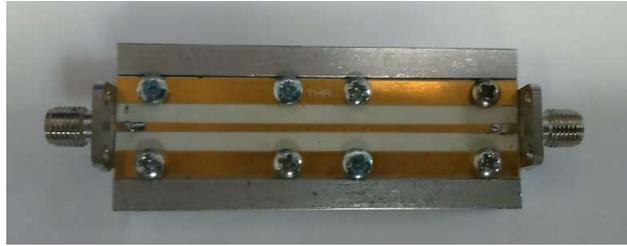


Figure 4.16: Fabricated thru standard.

REFLECT: Since zero length thru is used to set the reference plane, the reflect standard has half the length of the thru standard. A reflection standard can be realized via an open or a short; and in this case, an “open” is used. The fabricated open standard can be seen in Figure 4.17. This standard should have high reflection coefficient. For TRL calibration, the reflection coefficient does not have to be known. Table 4.4 shows the physical characteristics of the substrate and dimension of the coplanar waveguide for reflect standard

Table 4.4: REFLECT standard

Substrate (Rogers 4350B)				
H (mm)	ϵ_r	T (mm)	TanD	
0.508	3.66	0.035	0.0037	
Coplanar Waveguide				
W (mm)	G (mm)	L (mm)		
1.3	3.1	31.75		

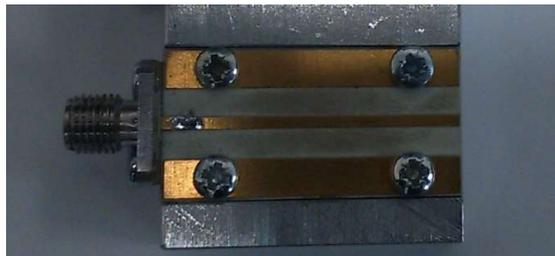


Figure 4.17: Fabricated reflect standard. An open is used as reflect.

LINE: The intended bandwidth for this TRL calibration standards is up to 18 GHz, which requires multiple line standards. The optimal break frequency is determined by $\sqrt{f_1 \times f_2}$, where f_1 and f_2 are the start and stop frequencies. For example:

$$\text{Optimal break frequency} = \sqrt{(2000 \times 18000)} \text{ MHz} = 6000 \text{ MHz} \quad (4.8)$$

A thru and line standard have the same physical characteristics, but differ in electrical characteristic. The difference in electrical length (ΔL) between the thru and line standards can be calculated with (4.9):

$$\text{Electrical length } \Delta L(\text{cm}) = \frac{15000 \times VF}{\text{Start Frequency}(\text{MHz}) + \text{Stop Frequency}(\text{MHz})} \quad (4.9)$$

Where velocity factor, $VF = 1/\sqrt{\epsilon_r}$ and ϵ_r is the dielectric constant of the laminate. The insertion phase of a transmission line at a particular frequency is given by (4.10):

$$\text{Insertion Phase} = \frac{0.012 \times \text{Frequency}(\text{MHz}) \times \text{length}(\text{cm})}{VF} \quad (4.10)$$

LINE1

$$\Delta L_1 = \frac{15000 \times VF}{2000 + 6000} = 1.0051 \text{ cm} = 10 \text{ mm} \quad (4.11)$$

$$\text{Length of LINE 1} = (\text{THRU} + 10) \text{ mm} = 73.5 \text{ mm} \quad (4.12)$$

$$\text{Insertion Phase}_{2000 \text{ MHz}} = (0.012 \times 2000 \times 1.0051) / VF = 44.77^\circ \quad (4.13)$$

$$\text{Insertion Phase}_{6000 \text{ MHz}} = (0.012 \times 6000 \times 1.0051) / VF = 134.31^\circ \quad (4.14)$$

LINE2

$$\Delta L_2 = \frac{15000 \times VF}{6000 + 18000} = 0.3350 \text{ cm} = 3.35 \text{ mm} \quad (4.15)$$

$$\text{Length of LINE 2} = (\text{THRU} + 3.35) \text{ mm} = 66.85 \text{ mm} \quad (4.16)$$

$$\text{Insertion Phase}_{6000 \text{ MHz}} = (0.012 \times 6000 \times 0.3350) / VF = 44.99^\circ \quad (4.17)$$

$$\text{Insertion Phase}_{18000 \text{ MHz}} = (0.012 \times 18000 \times 0.3350) / VF = 134.98^\circ \quad (4.18)$$

In both cases, the insertion phase is in between 20 and 160 degrees which satisfies the requirement for a line standard in TRL calibration. The fabricated LINE1 and LINE2 standards are depicted in Figure 4.18. It also needs to be noted that the impedance of the line standards is 50Ω . Table 4.5 shows the physical characteristics of the substrate and dimension of the coplanar waveguide for line standards.

Table 4.5: LINE standards

Substrate (Rogers 4350B)				
H (mm)	ϵ_r	T (mm)	TanD	
0.508	3.66	0.035	0.0037	
Coplanar Waveguide				
W (mm)	G (mm)	L1 (mm)	L2 (mm)	
1.3	3.1	73.5	66.85	



Figure 4.18: LINE1 and LINE 2 standards after fabrication.

4.4.4.3.2 Characterizing and Defining the TRL standards in VNA

The calibration standards must be defined correctly in the VNA. If the standards are defined incorrectly, the calibration will not be accurate, and it can result in poor measurements. Unlike ideal standards, the fabricated standards are never perfect; therefore, they have to be measured and characterized first before being defined in the VNA.

REFLECT: Unlike an ideal REFLECT, the OPEN does not have a reflection coefficient equal to 1. Unless it is included in the definition of the standard, the network analyser assumes that it is perfect, and this leads to error during calibration. This imperfection or source of error can be modelled with a resistor and nonlinear capacitance as shown in Fig. 4.19.

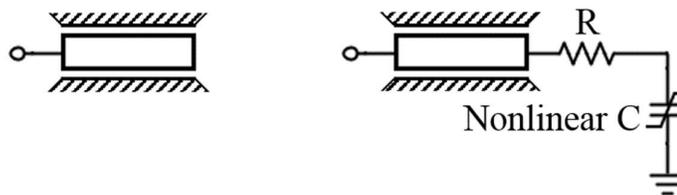


Figure 4.19: Model of the REFLECT standard in ADS with and without the error model. The values of resistance (R) and nonlinear capacitance (Nonlinear C) are obtained via optimization in ADS where a match between measurement and model of the REFLECT standard is achieved.

In order to obtain the values of the resistance and capacitance, the REFLECT standard is modelled in ADS following the model in [4.13].

Table 4.6: Error model for the REFLECT standard

R (Ω)	1.26			
Coefficients for Nonlinear C	C0	C1	C2	C3
	1.12e-12	2.6e-24	1.37e-48	3.0e-42

The values of the resistance and coefficients for the nonlinear capacitance in Table 4.6 are obtained through optimization until a fit between the measured and modelled response of the reflect standard is achieved as shown in Figure 4.20.

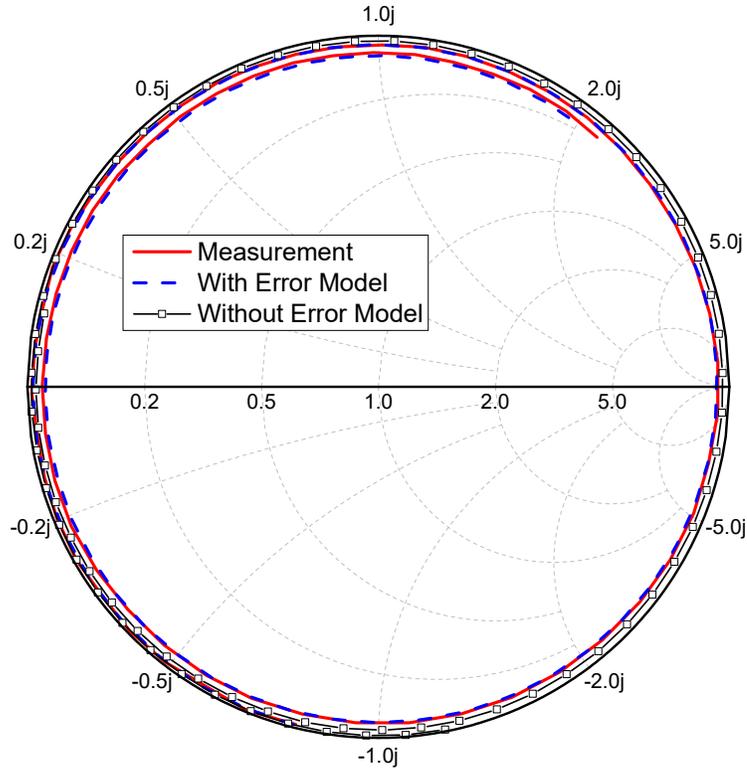


Figure 4.20: A comparison of measured (—solid line) and simulated response of the REFLECT standard, with (---dashed line) and without (-·-·) the error model shown in Figure 4.18. Measurement and simulation are in closer agreement after the introduction of the error model.

LINE: While defining the LINE standards in VNA, the delay of each line with respect to the THRU standard has to be known. Delay of a transmission line is given by:

$$Delay = \frac{length \times \sqrt{\epsilon_r}}{speed\ of\ light} \quad (4.19)$$

The calculated delays for both transmission line are given by (4.20) and (4.21):

$$Delay\ of\ LINE1 = \frac{10\ mm \times \sqrt{3.48}}{299792458\ m/s} = 62.52\ ps \quad (4.20)$$

$$Delay\ of\ LINE2 = \frac{3.35\ mm \times \sqrt{3.48}}{299792458\ m/s} = 20.85\ ps \quad (4.21)$$

However, in case of a transmission line such as coplanar waveguide, all the electric field of the signal is not contained within the dielectric material. A portion of the

electric field is in the air above the substrate and a portion of it is in the dielectric material. Therefore, in practice the dielectric constant is in fact the effective dielectric constant ϵ_{eff} , which is a function of the relative dielectric constant of the substrate, the width and thickness of the transmission line. The effective dielectric constant ϵ_{eff} can be calculated using the “LineCalc” tool in Advanced Design System (ADS) [4.12] and its value is 3.033 for the substrate characteristics and dimension of the line standards given in Table 4.5. Therefore, the actual delays of the line standards can be calculated from (4.22) and (4.23):

$$\text{Delay of LINE1} = \frac{10 \text{ mm} \times \sqrt{3.033}}{299792458 \text{ m/s}} = 58.09 \text{ ps} \quad (4.22)$$

$$\text{Delay of LINE2} = \frac{3.35 \text{ mm} \times \sqrt{3.033}}{299792458 \text{ m/s}} = 19.46 \text{ ps} \quad (4.23)$$

The delays of the line standards are also measured using the VNA and the values for LINE1 and LINE2 standards are 57.4255 ps and 20.4348 ps respectively. The incorrect values of delay for line standards calculated using relative dielectric constant ϵ_r instead of effective dielectric constant ϵ_{eff} causes error in calibration and consequently in the measurement. Figure 4.21 shows the measured s-parameters before and after error correction in standard definition is applied in the VNA. Without the correction, the extracted parameter value would be over-estimated.

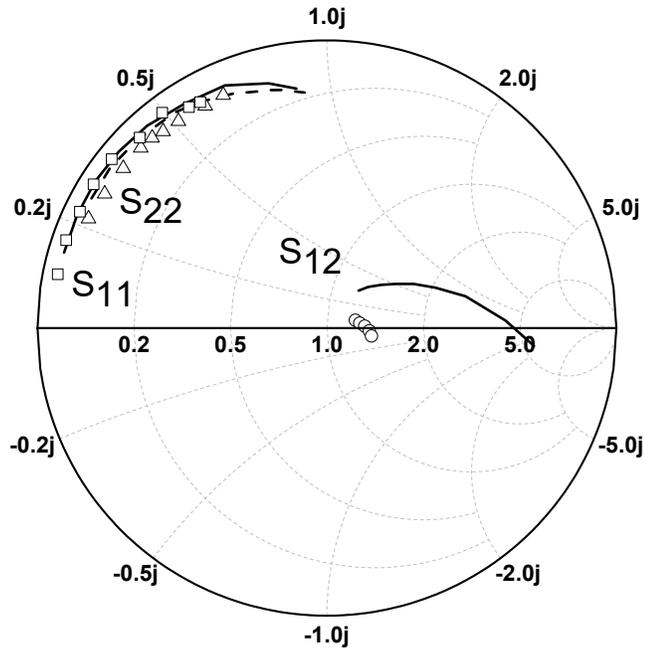


Figure 4.21: Measured S-parameters before (line) and after (symbol) error correction model applied.

4.5 Parameter Extraction

4.5.1 Package Model and its Equivalent Lumped Element Model

The 10W GaN-on-SiC HEMT, CGH40010, from Cree, Inc. is an unmatched transistor. The package model is supplied by the manufacturer in [4.14]. As shown in Figure 4.22, the model is constructed with lumped elements and microstrip lines. Table 4.7 shows the material properties of the substrate which are provided by the manufacturer.

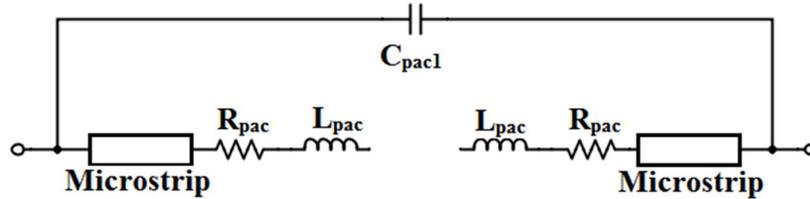


Figure 4.22: Model for the 440166 package type used in CGH40010 from Cree, Inc.

Table 4.7: Lumped element values and physical characteristics of the substrate and dimension of the coplanar waveguide for the 440166 package model

Substrate		
H (mil)	ϵ_r	T (mil)
20	9.6	1.4
Microstrip Line		
W (mil)	L (mm)	
100	30	
Lumped Elements		
C_{cap1} (pF)	R_{pac} (Ω)	L_{pac} (nH)
0.002	0.01	0.55

The small-signal equivalent circuit model consists only of lumped elements which makes it easier for mathematical manipulation. To extract the device parameters, the package parasitic elements must be de-embedded first. Therefore, for convenience, the microstrip lines in the package model are replaced by a shunt capacitor [4.15] as shown in Figure 4.23.

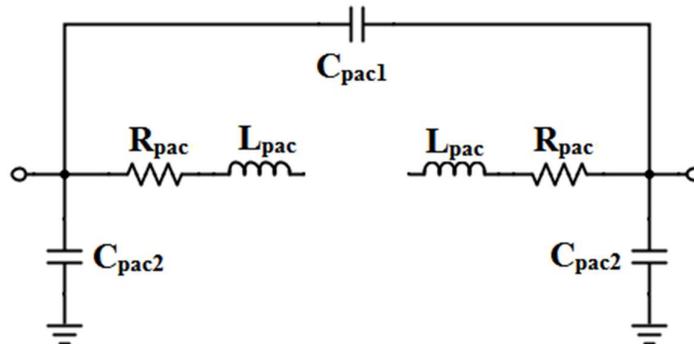


Figure 4.23: Equivalent lumped element circuit of the package model in Figure 4.16.

The value of the shunt capacitor (C_{pac2}) is determined through optimization until a match between the simulated S-parameters of the package model in Figure 4.21 and its equivalent lumped element circuit model in Figure 4.23 is achieved. It can be obtained as seen in Figure 4.24 for $C_{pac2} = 0.41079$ pF.

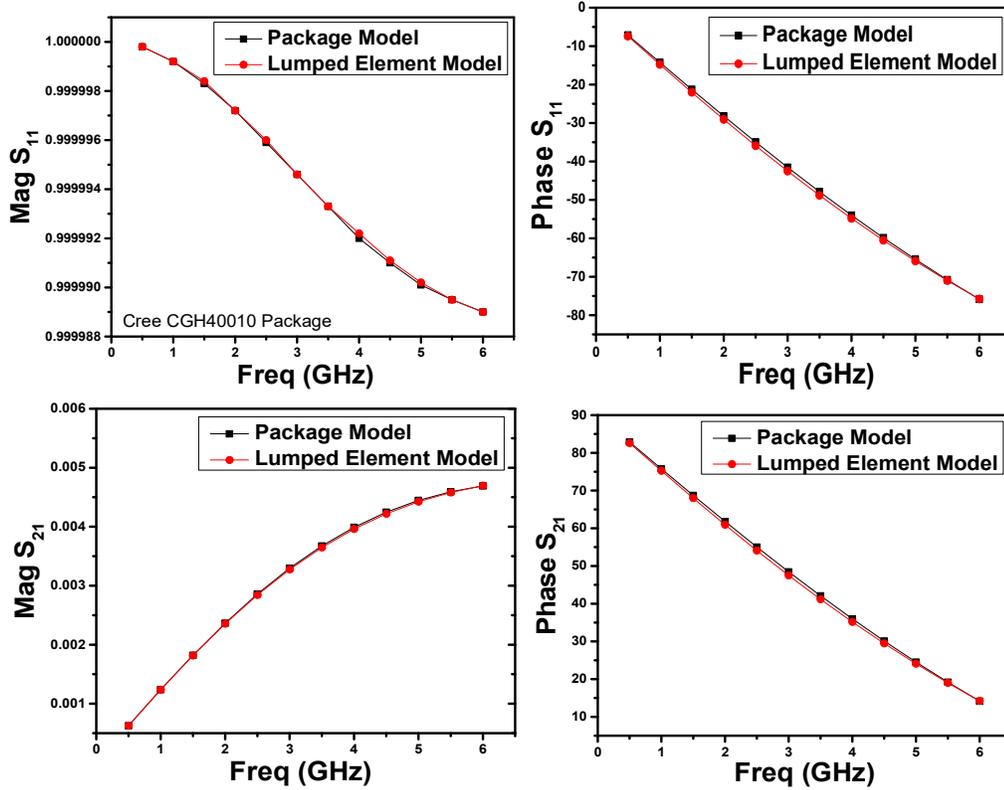


Figure 4.24: A comparison of S-parameters of the package model for the Cree CGH40010 (10 W GaN-on-SiC HEMT) and its equivalent lumped element circuit model for $C_{pac2} = 0.41079$ pF. For this equivalent circuit model $S_{11} = S_{22}$ and $S_{12} = S_{21}$.

4.5.2 De-embedding Package Parasitic and Extracting Equivalent Lumped Element Model of a GaN HEMT

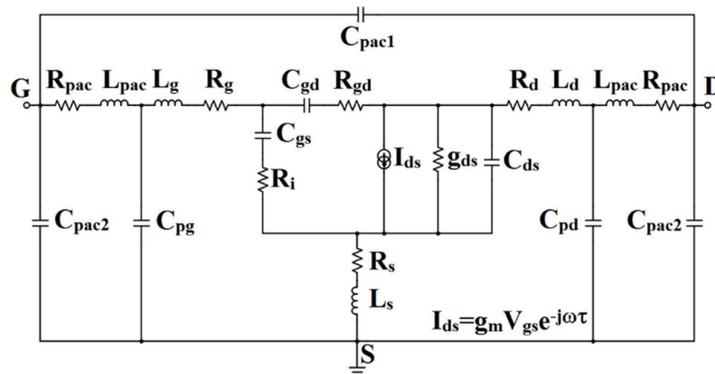


Figure 4.25: Equivalent circuit model considering the package model.

Figure 4.25 shows the equivalent lumped element model of GaN HEMT including the parasitic elements of the package. It is essentially the same small-signal model in Figure 4.1, including the package parasitic elements. The package parasitic elements are first removed from measured S-parameters following the de-embedding process described in Section 4.4.4.2 to acquire the device model.

4.5.3 Extraction of extrinsic parameters

In [4.16], the authors showed that in order to extract the values of intrinsic parameters the extrinsic elements have to be de-embedded first. Therefore, the extraction procedure of a small-signal model begins with the extraction of extrinsic elements from two sets of measurement under “cold condition”.

4.5.3.1 Extraction of pad capacitance:

In the cold modelling procedure, the device is first biased at below-pinch off where $V_{DS} = 0$ V and $V_{GS} < V_{th}$ in order to suppress the channel conductivity to extract the parasitic pad capacitances.

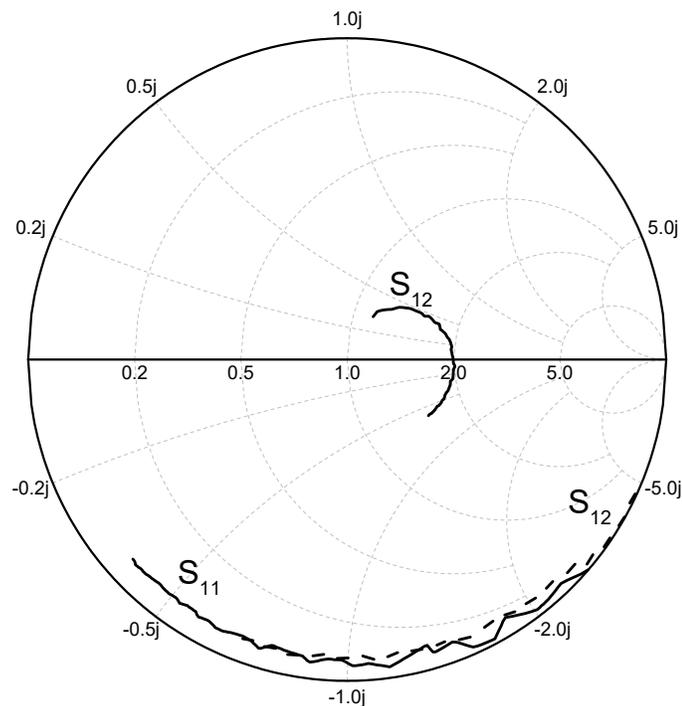


Figure 4.26: Measured S_{11} , S_{12} and S_{22} parameter for the Cree CGH40010 (10 W GaN-on-SiC HEMT) at below pinch-off condition ($V_{DS} = 0$ V and $V_{GS} < V_{pinch-off}$).

Figure 4.26 shows the measured S-parameters for the 10 W GaN-on-SiC HEMT after de-embedding of the test fixture from measured data. The equivalent circuit at this condition can be seen in Figure 4.27.

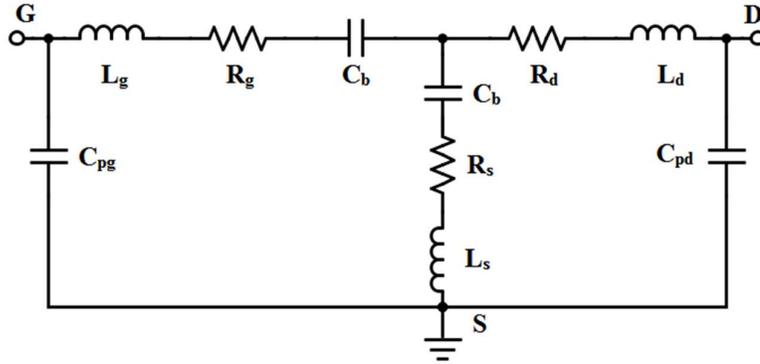


Figure 4.27: Equivalent circuit at below pinch-off condition.

Under this condition, the resistances have no influence on the imaginary parts of the Y-parameters and the effect of inductances can be ignored for lower frequency range. As a result, the “passive” device shows purely capacitive behaviour [4.16] from low to medium frequencies. Based on these assumptions, the circuit in Figure 4.27 can be represented as the one in Figure 4.28.

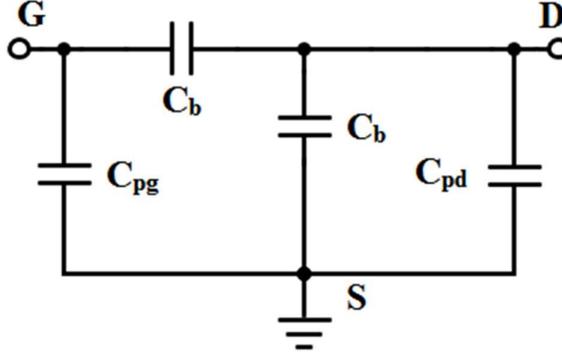


Figure 4.28: Equivalent circuit at below pinch-off condition at lower frequency.

The capacitance C_b is the fringing capacitance which arises from the depletion layer on both sides under the gate. Since the circuit looks like a pi-network, the s-parameters are converted to Y-parameters. The imaginary parts of the Y-parameters can be expressed as:

$$\text{Im}(Y_{11}) = j\omega(C_{pg} + 2C_b) \quad (4.24)$$

$$\text{Im}(Y_{12}) = \text{Im}(Y_{21}) = -j\omega C_b \quad (4.25)$$

$$\text{Im}(Y_{22}) = j\omega(C_{pd} + C_b) \quad (4.26)$$

The imaginary parts are found to be linearly dependent with frequency when plotted. The values of C_b , C_{pg} , C_{pd} are obtained from the slopes of these lines. The extracted pad capacitance value is 2.135 pF.

The extracted pad capacitance value in this method is overestimated as the values of other parasitic capacitances are not separated. Figure 4.29 shows the equivalent circuit of a GaN HEMT at below pinch-off condition at lower frequency according to [4.2].

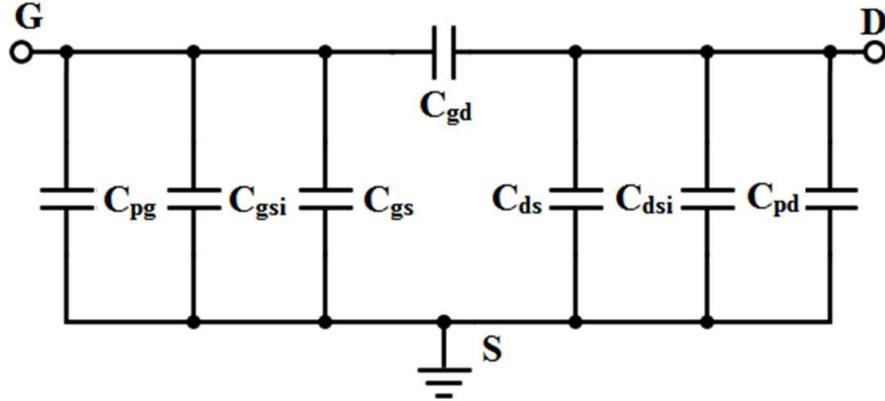


Figure 4.29: Equivalent circuit under below pinch-off condition ($V_{DS} = 0$ V, $V_{GS} < V_{pinch-off}$).

In Figure 4.29, C_{gs} , C_{gd} and C_{ds} are the intrinsic part of the total capacitances at below pinch-off condition, and C_{gsi} and C_{dsi} are the inter-electrode capacitances between gate, source and drain. In the method [4.2] followed in this thesis, the pad capacitances are extracted from below pinch-off condition as before. The imaginary parts of the Y-parameters of the equivalent circuit in Figure 4.29 can be expressed as:

$$\text{Im}(Y_{11}) = j\omega(C_{pg} + C_{gsi} + C_{gs} + C_{gd}) \quad (4.27)$$

$$\text{Im}(Y_{12}) = \text{Im}(Y_{21}) = -j\omega C_{gd} \quad (4.28)$$

$$\text{Im}(Y_{22}) = j\omega(C_{pd} + C_{dsi} + C_{ds} + C_{gd}) \quad (4.29)$$

The total capacitances of gate-to-source, drain-to-source and gate-to-drain are extracted from the slopes of these curves plotted in Figure 4.30. Now, the individual capacitance values are separated from the total capacitances using the assumptions [4.2] below:

$$C_{gs} = C_{gd} \quad (4.30)$$

$$C_{dsi} = 3C_{pd} \quad (4.31)$$

$$C_{ds} = 12C_{pd} \quad (4.32)$$

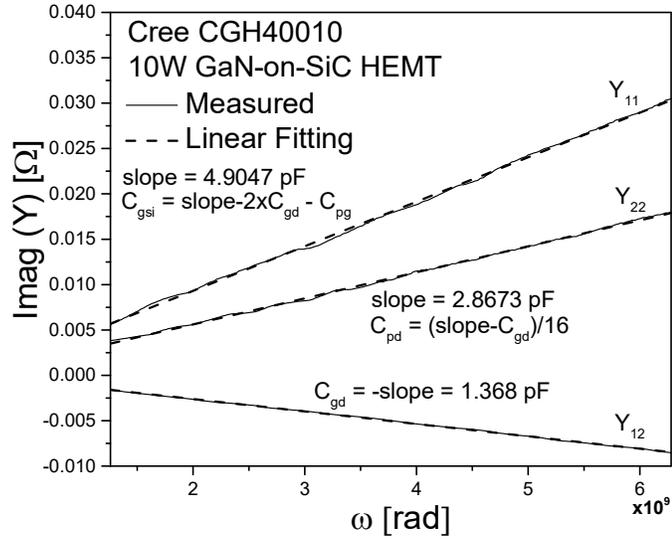


Figure 4.30: Extraction of pad capacitance values from the slope of the imaginary part of the Y-parameters under below pinch-off condition ($V_{DS} = 0$ V, $V_{GS} < V_{pinch-off}$) for the Cree CGH40010 (10 W GaN-on-SiC HEMT).

4.5.3.2 Extraction of parasitic Inductance and Resistance

In [4.16], Dambrine et al. demonstrated a method to determine the parasitic inductance and resistance by reducing the impact of the capacitive effect at the gate by driving sufficient gate current (I_g) through the drain at a bias condition where $V_{DS} = 0$ V and $V_{GS} > V_{pinch-off}$.

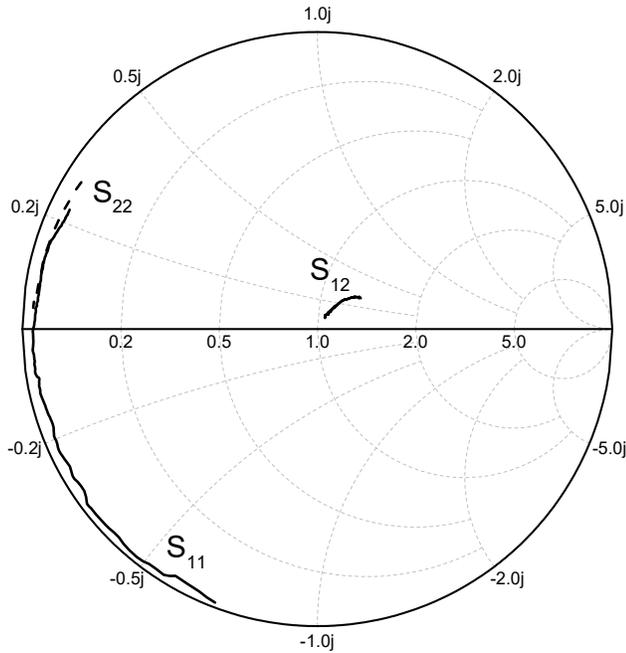


Figure 4.31: Measured S_{11} , S_{12} and S_{22} parameter for the Cree CGH40010 (10 W GaN-on-SiC HEMT) at above pinch-off condition ($V_{DS} = 0$ V and $V_{GS} > V_{pinch-off}$).

According to this procedure, high gate current I_g is required to make the capacitive behaviour of S_{11} , as depicted in Figure 4.31, disappear. Therefore, a high positive gate voltage ($V_{GS} > 0$ V) needs to be applied to AlGaN/GaN HEMT to follow this procedure. Since these devices show very high gate resistance, and this can cause detrimental effects or can even destroy the Schottky gate [4.1]. In this thesis, the procedure proposed by Chen et al [4.1] under zero drain voltage and low gate bias voltage ($V_{pinch-off} < V_{GS} < 0$) has been followed. For the GaN HEMT devices extracted in this thesis, the voltage is within the range of -2 V to -1 V.

After de-embedding the extrinsic parasitic capacitances, the intrinsic device under this condition shows a Π configuration in series with the parasitic resistances and inductances (Figure 4.32). Under this circumstance, the values of all the lumped elements cannot be extracted directly. The Wye-Delta transformation is applied to the intrinsic device to turn it from a Π configuration into a T configuration.

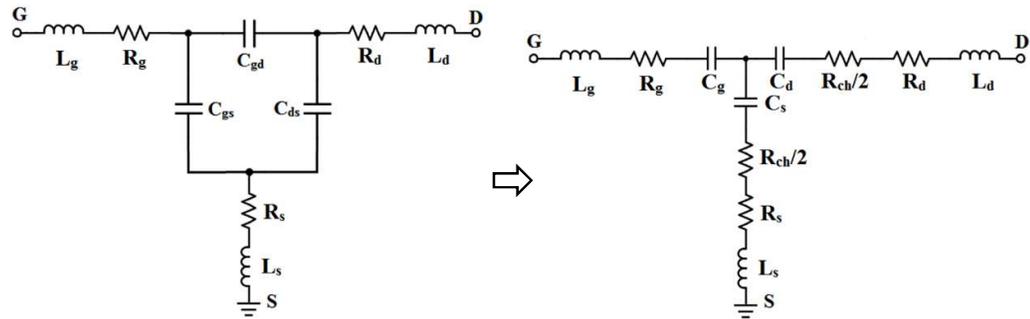


Figure 4.32: Equivalent circuit at above pinch-off condition ($V_{DS} = 0$ V, $V_{GS} > V_{pinch-off}$) before (a) and after (b) the Wye-Delta transformation.

This transformation allows to express the device using Z-parameters as given by (4.33) - (4.35) [4.1]:

$$Z_{11} = R_s + R_g + j \left(\omega L_s + \omega L_g - \frac{1}{\omega C_g} - \frac{1}{\omega C_s} \right) \quad (4.33)$$

$$Z_{12} = R_s + \frac{R_{ch}}{2} + j \left(\omega L_s - \frac{1}{\omega C_s} \right) \quad (4.34)$$

$$Z_{22} = R_s + R_d + R_{ch} + j \left(\omega L_s + \omega L_d - \frac{1}{\omega C_s} - \frac{1}{\omega C_d} \right) \quad (4.35)$$

The imaginary parts of (4.33) – (4.35) can be rewritten as:

$$\omega^2 (L_g + L_s) = \omega \text{Im} (Z_{11}) \quad (4.36)$$

$$\omega \operatorname{Im}(Z_{12}) = \omega^2 L_s \quad (4.37)$$

$$\omega^2 (L_d + L_s) = \omega \operatorname{Im}(Z_{22}) \quad (4.38)$$

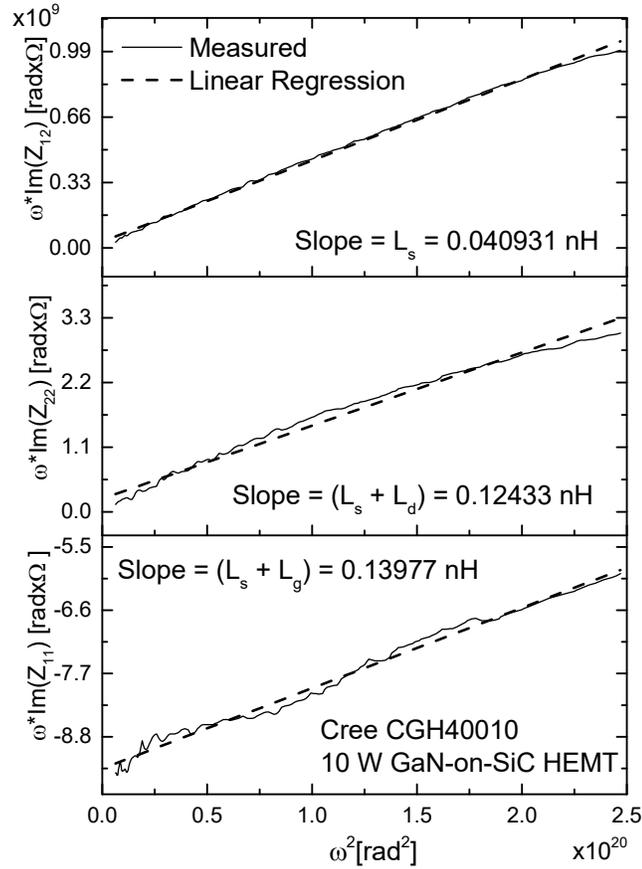


Figure 4.33: Extraction of L_s , L_g and L_d at above pinch-off condition ($V_{DS} = 0$ V and $V_{GSq} > V_{pinch-off}$) for the Cree CGH40010 (10 W GaN-on-SiC HEMT).

The source inductance (L_s) is first determined from the slope of $\omega \times \operatorname{Im}(Z_{12})$ versus ω^2 curve. Then the values of the terms $(L_g + L_s)$ and $(L_d + L_s)$ are extracted respectively from the slopes of $\omega \times \operatorname{Im}(Z_{11})$ versus ω^2 and $\omega \times \operatorname{Im}(Z_{22})$ versus ω^2 curves. Finally, the values of gate inductance (L_g) and drain inductance (L_d) are determined by subtracting the source inductance.

There are only three equations (4.33 - 4.35) and four resistance values to be determined. This would require an additional measurement. In [4.17], a method termed as cold reverse is described where all the values of extrinsic parasitic resistance R_s , R_d and R_g can be obtained from measured S-parameters at the condition where $V_{DS} = 0$ V and $V_{pinch-off} < V_{GS} < 0$ V.

First the package parasitic elements and the extrinsic capacitances and inductances are subtracted from the measured data. The remaining device effects can be presented by the real and imaginary parts of the Z-parameters as expressed by the following equations:

$$\operatorname{Re}(Z_{11}) = R_g + R_s + \alpha \frac{R_{ch}}{1 + \omega^2 C_{ch}^2 R_{ch}^2} \quad (4.39)$$

$$\operatorname{Im}(Z_{11}) = -\frac{1}{\omega C_{gg}} - \alpha \frac{\omega C_{ch} R_{ch}^2}{1 + \omega^2 C_{ch}^2 R_{ch}^2} \quad (4.40)$$

$$\operatorname{Re}(Z_{12}) = R_s + \beta \frac{R_{ch}}{1 + \omega^2 C_{ch}^2 R_{ch}^2} \quad (4.41)$$

$$\operatorname{Im}(Z_{12}) = -\beta \frac{\omega C_{ch} R_{ch}^2}{1 + \omega^2 C_{ch}^2 R_{ch}^2} \quad (4.42)$$

$$\operatorname{Re}(Z_{22}) = R_d + R_s + \frac{R_{ch}}{1 + \omega^2 C_{ch}^2 R_{ch}^2} \quad (4.43)$$

$$\operatorname{Im}(Z_{22}) = -\frac{\omega C_{ch} R_{ch}^2}{1 + \omega^2 C_{ch}^2 R_{ch}^2} \quad (4.44)$$

Here, R_{ch} and C_{ch} are the resistance and capacitance of the conduction channel impedance, α and β are channel impedance parameters and C_{gg} is the capacitance of the Schottky-gate impedance.

Now, (4.43) can be written in terms of (4.44) as follows:

$$\operatorname{Re}(Z_{22}) = R_d + R_s + \frac{-\operatorname{Im}(Z_{22})}{\omega} \frac{1}{C_{ch} R_{ch}} \quad (4.45)$$

Multiplying both sides by $\omega/\operatorname{Im}(Z_{22})$, (4.45) can be expressed as:

$$\frac{\operatorname{Re}(Z_{22})}{\operatorname{Im}(Z_{22})} \omega = -\frac{1}{C_{ch} R_{ch}} + \frac{\omega}{\operatorname{Im}(Z_{22})} (R_d + R_s) \quad (4.46)$$

By plotting $\omega \times \operatorname{Re}(Z_{22})/\operatorname{Im}(Z_{22})$ versus $\omega/\operatorname{Im}(Z_{22})$ as shown in Figure 4.34, the value of $(R_d + R_s)$ can be obtained from the slope of the curve.

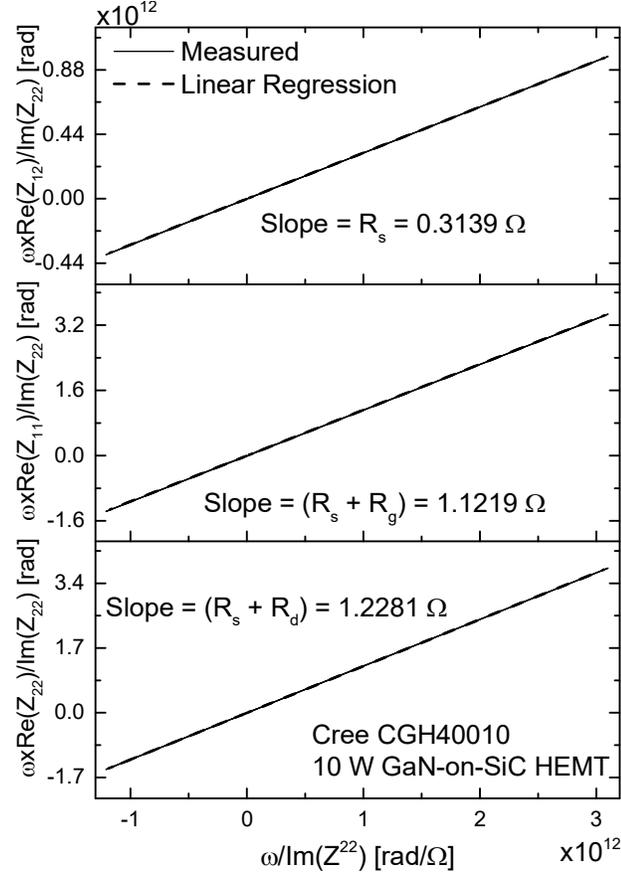


Figure 4.34: Extraction of R_s , R_g and R_d at above pinch-off condition ($V_{DS} = 0$ V and $V_{GSq} > V_{pinch-off}$) for the Cree CGH40010 (10 W GaN-on-SiC HEMT).

Now rewriting (4.39) and (4.41) in terms of $Im(Z_{22})$ as in (4.47) and (4.48), the values of R_s and $(R_g + R_s)$ can be determined respectively.

$$\frac{Re(Z_{11})}{Im(Z_{22})} \omega = -\frac{\alpha}{C_{ch} R_{ch}} + \frac{\omega}{Im(Z_{22})} (R_g + R_s) \quad (4.47)$$

$$\frac{Re(Z_{12})}{Im(Z_{22})} \omega = -\frac{\beta}{C_{ch} R_{ch}} + \frac{\omega}{Im(Z_{22})} (R_s) \quad (4.48)$$

4.5.3.3 Extraction of Intrinsic Parameters

The intrinsic parameters of the small-signal model are bias-dependent. Therefore, these are extracted from the measured data at the bias condition of interest. First of all, the extrinsic parameters obtained in previous section are de-embedded to get the intrinsic Y-parameters. According to Dambrine et al. [4.16], the intrinsic parameters can be extracted from the following equations:

$$Y_{11} = (R_i C_{gs}^2 \omega^2 / D) + j\omega(C_{gs} / D + C_{gd}) \quad (4.49)$$

$$Y_{12} = -j\omega C_{gd} \quad (4.50)$$

$$Y_{21} = \left[g_m e^{-j\omega\tau} / (1 + j\omega R_i C_{gs}) \right] - j\omega C_{gd} \quad (4.51)$$

$$Y_{22} = g_{ds} + j\omega (C_{ds} + C_{gd}) \quad (4.52)$$

$$\text{Where: } D = 1 + \omega^2 C_{gs}^2 R_i^2 \quad (4.53)$$

Dambrine et al. considered the value of $D = 1$ at low frequency. Berroth and Bosche [4.18] observed that this assumption gives an excellent match up to 5 GHz but displays notable errors at higher frequencies. The authors proposed an improved method to analytically extract the values of the intrinsic parameters by using expressions separating the real and imaginary parts of the above equations without assuming the value of D equal to 1 which overcomes the limitations at higher frequency. Similar to [4.18], J. Lu et al. [4.2] used the following formulations to obtain the values of intrinsic parameters:

$$\omega C_{gd} = -\text{Im}(Y_{12}) \left(1 + \left(\frac{\text{Re}(Y_{12})}{\text{Im}(Y_{12})} \right)^2 \right) \quad (4.54)$$

$$\omega C_{ds} = \text{Im}(Y_{22}) + \text{Im}(Y_{12}) \quad (4.55)$$

$$\omega C_{gs} = (\text{Im}(Y_{11}) + \text{Im}(Y_{12})) \left(1 + \frac{(\text{Re}(Y_{11}) + \text{Re}(Y_{12}))^2}{(\text{Im}(Y_{11}) + \text{Im}(Y_{12}))^2} \right) \quad (4.56)$$

After plotting these equations against angular frequency (ω) as in Figure 4.35, the value of each parameter is extracted from the slope of the corresponding curve.

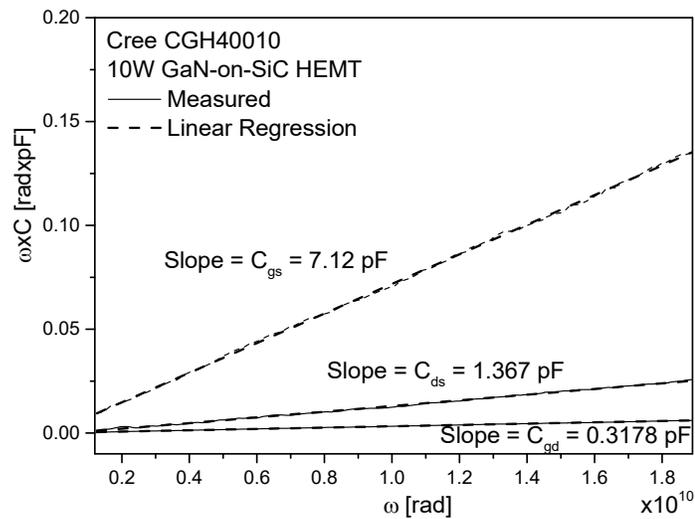


Figure 4.35: Extraction of intrinsic capacitance values for the Cree CGH40010 (10 W GaN-on-SiC HEMT) at $V_{DS} = 28$ V and $I_{DSq} = 340$ mA.

Transconductance (g_m), output conductance (g_{ds}) and resistance R_i and R_{gd} are extracted from the mean values of g_m , g_{ds} , R_i and R_{gd} curves plotted against frequency as shown in Figure 4.36.

$$g_m = \text{Re}(Y_{21}) \quad (4.57)$$

$$g_{ds} = \text{Re}(Y_{22}) \quad (4.58)$$

$$R_i = \text{Re}(Y_{11}) \quad (4.59)$$

$$R_{gd} = \text{Re}(Y_{12}) \quad (4.60)$$

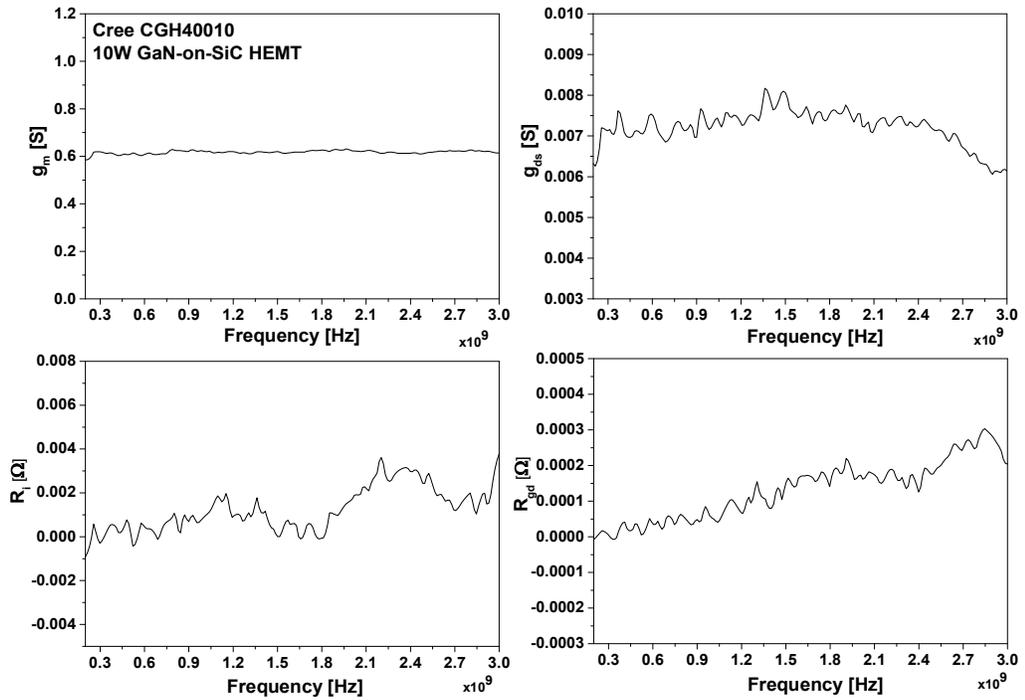


Figure 4.36: Extraction of g_m , g_{ds} , R_i and R_{gd} for the Cree CGH40010 (10 W GaN-on-SiC HEMT) at $V_{DS} = 28$ V and $I_{DSq} = 340$ mA.

It can be mentioned that the value of transconductance extracted from S-parameters or the dynamic transconductance $g_{m,dynamic}$ and the value obtained from DC measurement or static transconductance $g_{m,static}$ are 0.623 S and 0.728 S respectively. Current collapse, due to trapping effects, reduces the dynamic saturation current compared to the DC current and as a result, $g_{m,dynamic}$ is less than the static $g_{m,static}$. The effects of DC-to-RF dispersion on the RF performance are explored in detail in Chapter 5.

After the parameters are extracted, a small-signal model is built in ADS and the S-parameters are simulated. The parameter values are optimized using the ADS optimization blocks to obtain good match between the measurement and model. Table

4.8 shows the parameter values for Cree CGH40010 (10 W GaN-on-SiC HEMT) before and after optimization.

Table 4.8 Extracted parameter values of Cree CGH40010 before and after optimization at $V_{DS} = 28$ V, $I_{DSq} = 340$ mA, Frequency = 0.4 - 3.5 GHz

		Before	After Optimization	% of Change
Package Parasitic Elements	C_{pac1} (pF)	0.002	0.002	0
	C_{pac2} (pF)	0.41079	0.41079	0
	L_{pac} (nH)	0.55	0.55	0
	R_{pac} (Ω)	0.01	0.01	0
Extrinsic Parameters	C_{pg} (pF)	0.0937	0.0891	-4.91
	C_{pd} (pF)	0.0937	0.0891	-4.91
	L_s (nH)	0.04093	0.0412	+0.66
	L_d (nH)	0.07502	0.03435	-54.21
	L_g (nH)	0.0988	0.0674	-31.78
	R_s (Ω)	0.391	0.01435	-96.33
	R_d (Ω)	1.107	1.279	+15.54
Intrinsic Parameters	R_g (Ω)	1.213	1.2073	-0.47
	C_{gd} (pF)	0.3178	0.341	+7.3
	C_{ds} (pF)	1.367	1.589	+16.24
	C_{gs} (pF)	7.12	6.71661	-5.67
	g_m (S)	0.617	0.641	+3.89
	g_{ds} (S)	0.007	0.007	0
	R_i (nΩ)	0.0012	0.0012	0
	R_{gd} (nΩ)	0.00013	0.00013	0

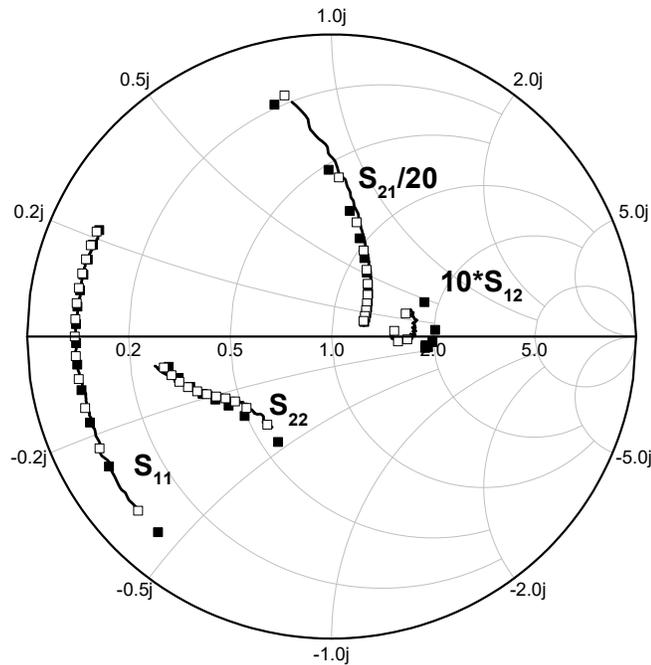


Figure 4.37: Comparison of measured (line) and modelled S-parameters before (■) and after (□) optimization for the 10 W GaN-on-SiC HEMT (Cree CGH40010) at $V_{DS} = 28$ V, $I_{DSq} = 340$ mA, Frequency = 0.4 - 3.5 GHz. The S-parameters are obtained after de-embedding the test fixture from measured data using SOLT calibration.

It can be seen from Table 4.8 that the R_s shows the highest difference before and after optimization. Therefore, the extraction procedure falls short to extract the value of source resistance. This can be observed in simulated S_{12} parameter as well in Figure 4.37. The R_s is obtained from the real part of S_{12} .

4.5.4 Extracting Equivalent Lumped Element Model of Si LDMOS

4.5.4.1 Extraction of Extrinsic Parameters

The extrinsic parameter values for a silicon LDMOS are extracted following the method proposed by Gaddi in [4.19]. The equivalent circuit under this condition shows a T topology and can be expressed in terms of Z-parameters as:

$$Z_{12} = R_s + j\omega L_s - \frac{1}{j\omega C_s} \quad (4.61)$$

$$Z_{22} = R_d + R_s + j\omega(L_d + L_s) - \left(\frac{1}{j\omega C_d} + \frac{1}{j\omega C_s} \right) \quad (4.62)$$

$$Z_{11} = R_g + R_s + j\omega(L_g + L_s) - \left(\frac{1}{j\omega C_g} + \frac{1}{j\omega C_s} \right) \quad (4.63)$$

The imaginary parts of equations (4.61) - (4.63) can be rewritten as:

$$\frac{\text{Im}(Z_{12})}{\omega} = L_s - \frac{1}{\omega^2 C_s} \quad (4.64)$$

$$\frac{\text{Im}(Z_{22})}{\omega} = (L_d + L_s) - \left(\frac{1}{\omega^2 C_d} + \frac{1}{\omega^2 C_s} \right) \quad (4.65)$$

$$\frac{\text{Im}(Z_{11})}{\omega} = (L_g + L_s) - \left(\frac{1}{\omega^2 C_g} + \frac{1}{\omega^2 C_s} \right) \quad (4.66)$$

After plotting $\text{Im}(Z_{12})/\omega$ against $1/\omega^2$, the value of L_s can be obtained from the intersection of the line and the y-axis. Similarly, the values of $L_d + L_s$ and $L_g + L_s$ are obtained by plotting $\text{Im}(Z_{22})/\omega$ and $\text{Im}(Z_{11})/\omega$ against $1/\omega^2$ respectively. As shown in Figure 4.38, the values of R_s , $R_d + R_s$, $R_g + R_s$ are determined directly from the real part of the equations (4.61) - (4.63) respectively.

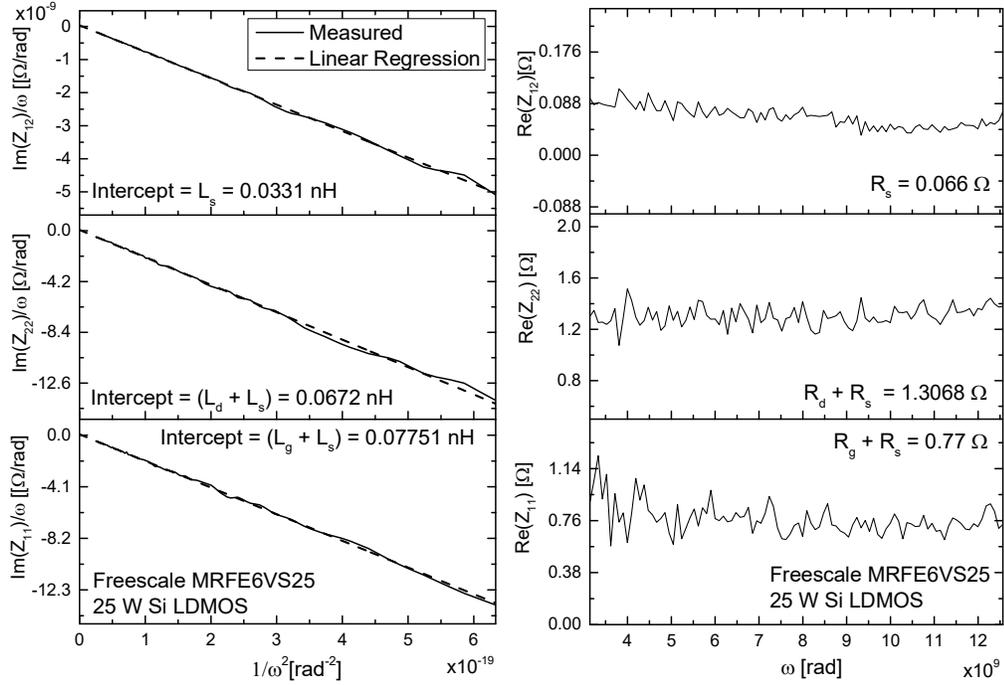


Figure 4.38: Extraction of extrinsic inductances L_s , L_g and L_d and resistances R_s , R_g and R_d at $V_{DSq} = 0$ V and $V_{GSq} = 0$ V for the Freescale MRFE6VS25 (25 W Si LDMOS).

4.5.4.2 Extraction of Intrinsic Parameters

The intrinsic parameters of the silicon LDMOS are extracted following the method by Dambrine et al [4.16]. Since the MRFE6VS25 operates up to 2 GHz, it can be assumed that $D = 1$ and for a silicon LDMOS equations (4.49) - (4.52) can be written as:

$$Y_{11} = C_{gs}^2 \omega^2 + j\omega (C_{gs} + C_{gd}) \quad (4.67)$$

$$Y_{12} = -j\omega C_{gd} \quad (4.68)$$

$$Y_{21} = g_m - j\omega (C_{gd} + g_m (C_{gs} + \tau)) \quad (4.69)$$

$$Y_{22} = g_{ds} + j\omega (C_{ds} + C_{gd}) \quad (4.70)$$

The imaginary parts of Y_{12} , Y_{11} and Y_{22} are plotted against the angular frequency ω as shown in Figure 4.39 and the values C_{gd} , $C_{gs} + C_{gd}$ and $C_{ds} + C_{gd}$ are obtained from the slopes of these lines.

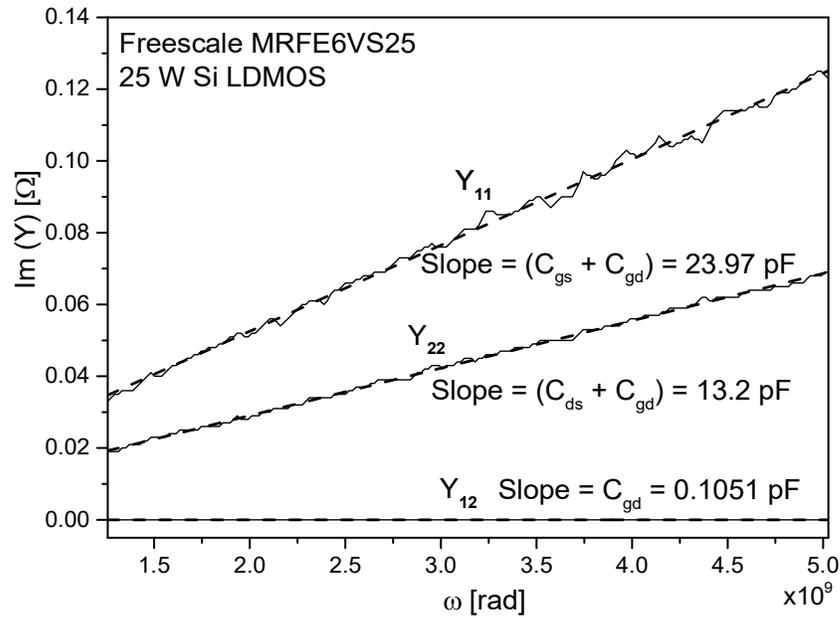


Figure 4.39: Extraction of intrinsic capacitance values for the Freescale MRFE6VS25 (25 W Si LDMOS) at $V_{DS} = 50 \text{ V}$ and $I_{DSq} = 450 \text{ mA}$.

The values of transconductance g_m and output conductance g_{ds} are extracted from the real parts of Y_{21} and Y_{22} respectively (Figure 4.40).

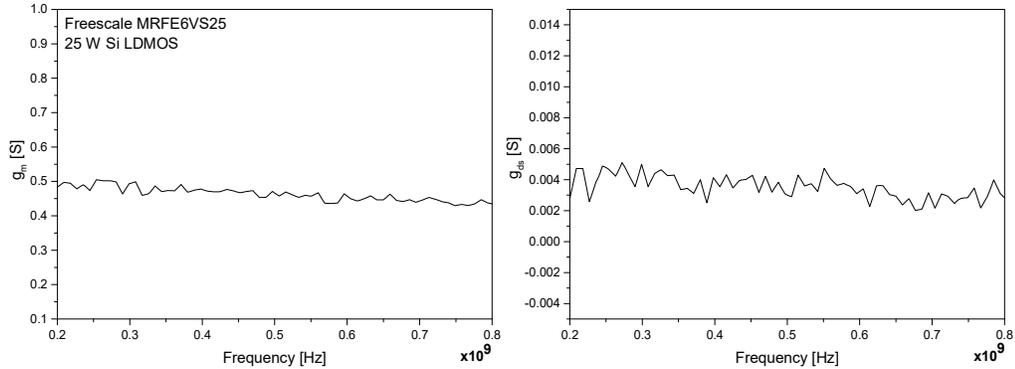


Figure 4.40: Extraction of g_m and g_{ds} for the Freescale MRFE6VS25 (25 W Si LDMOS) at $V_{DS} = 50 \text{ V}$ and $I_{DSq} = 450 \text{ mA}$.

Like the GaN HEMT, the extracted parameter values are optimized using ADS optimization blocks to obtain good match between the measured and modelled data. Table 4.9 shows the parameter values for Freescale MRFE6VS25 before and after optimization.

Table 4.9 Extracted parameter values of Freescale MRFE6VS25 before and after optimization at $V_{DS} = 50$ V, $I_{DSq} = 450$ mA, Frequency = 0.2 – 2 GHz

		Before	After Optimization	% of Change
Extrinsic Parameters	L_s (nH)	0.0331	0.03001	-9.3%
	L_d (nH)	0.03719	0.03719	0
	L_g (nH)	0.0475	0.0475	0
	R_s (Ω)	0.066	0.045	-31.82
	R_d (Ω)	1.3068	1.497	+14.55
	R_g (Ω)	0.77	0.646	-16.10
Intrinsic Parameters	C_{gd} (pF)	0.1051	0.1069	+1.71
	C_{ds} (pF)	13.09	14.38	+9.85
	C_{gs} (pF)	23.8649	24.68	+3.41
	g_m (S)	0.477	0.486	+1.89
	g_{ds} (S)	0.003	0.003	0

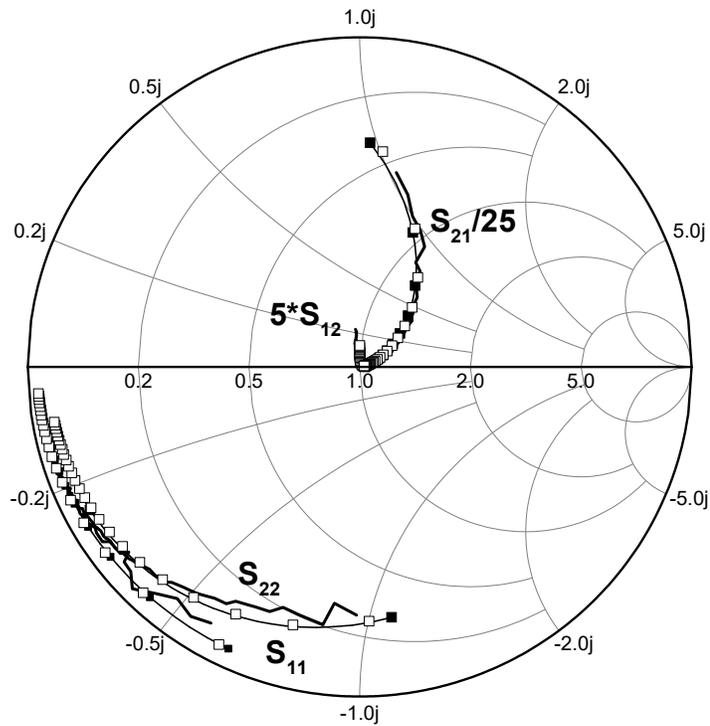


Figure 4.41: Comparison of measured (line) and modelled S-parameters before (■) and after (□) optimization for the 25 W Si LDMOS Freescale MRFE6VS25 at $V_{DS} = 50$ V, $I_{DSq} = 450$ mA, Frequency = 0.2 - 2 GHz. The S-parameters are obtained after de-embedding the test fixture from measured data using SOLT calibration.

It can be seen from Table 4.9 and Figure 4.41 that the extracted parameter values of the silicon LDMOS require minimum optimization after extraction to obtain a good match between measured and simulated S-parameters using the model.

4.6 Validation

The values of the extracted lumped elements are summarized in Table 4.10 – Table 4.16 for GaN HEMT and Si LDMOS devices rating from 2 W to 25 W over a range of frequencies from 200 MHz to 8 GHz. The small-signal models are built in ADS and the S-parameters from simulation and measurement are compared to validate the obtained parameter values after extraction and optimization. The measured drain current and corresponding transconductance characteristics are also presented in the following sections.

4.6.1 Cree CGH40010 (10 W GaN-on-SiC HEMT)

The Cree CGH40010 from Cree is a 10 W GaN-on-SiC HEMT. It has been chosen to show the effects of parasitic introduced by the package since the package model is available from the manufacturer. Table 4.10 shows the extracted parameter values with and with considering the package parasitic separately.

Table 4.10 Extracted parameter values of Cree CGH40010 at $V_{DS} = 28$ V, $I_{DSq} = 340$ mA, Frequency = 0.4 - 3.5 GHz

		Considering Package Separately	Without Considering Package Separately
Package Parasitic Elements	C_{pac1} (pF)	0.002	-
	C_{pac2} (pF)	0.41079	-
	L_{pac} (nH)	0.55	-
	R_{pac} (Ω)	0.01	-
Extrinsic Parameters	C_{pg} (pF)	0.0891	0.1145
	C_{pd} (pF)	0.0891	0.1145
	L_s (nH)	0.0412	0.039
	L_d (nH)	0.0289	0.6215
	L_g (nH)	0.0674	0.6505
	R_s (Ω)	0.01435	0.01435
	R_d (Ω)	1.279	1.43
	R_g (Ω)	1.2073	1.33
Intrinsic Parameters	C_{gd} (pF)	0.341	0.3339
	C_{ds} (pF)	1.589	1.570
	C_{gs} (pF)	6.71661	7.190
	g_m (S)	0.641	0.623
	g_{ds} (S)	0.007	0.007
	R_i (n Ω)	0.0012	0.006
	R_{gd} (n Ω)	0.00013	0.00012

It can be observed in Table 4.10 that intrinsic parameters are nearly identical in both cases whether or not the package is considered separately. The bond wires in the package mainly introduce additional inductance and resistance to the extrinsic parameters. The influence of these parasitic elements on the optimum impedance values and device performance are explored in Chapter 5.

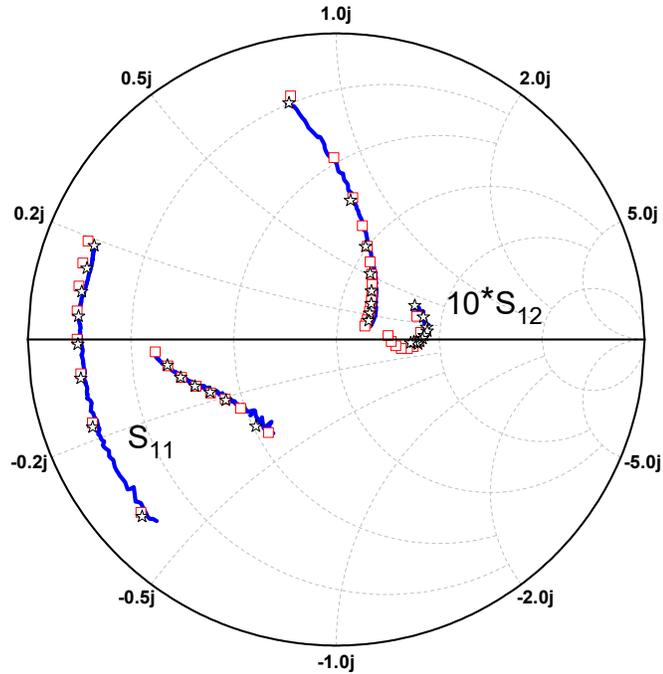


Figure 4.42: Comparison of measured (line) and modelled S-parameters with (□) and without (☆) package parasitic for the 10 W GaN-on-SiC HEMT (Cree CGH40010) at $V_{DS} = 28$ V, $I_{DSq} = 340$ mA, Frequency = 0.4 - 3.5 GHz. The S-parameters are obtained after de-embedding the test fixture from measured data using SOLT calibration.

The good agreement between the simulated and measured data in Figure 4.42 ensures the validation of the values of extrinsic and intrinsic parameters obtained via direct extraction procedure, followed by optimization.

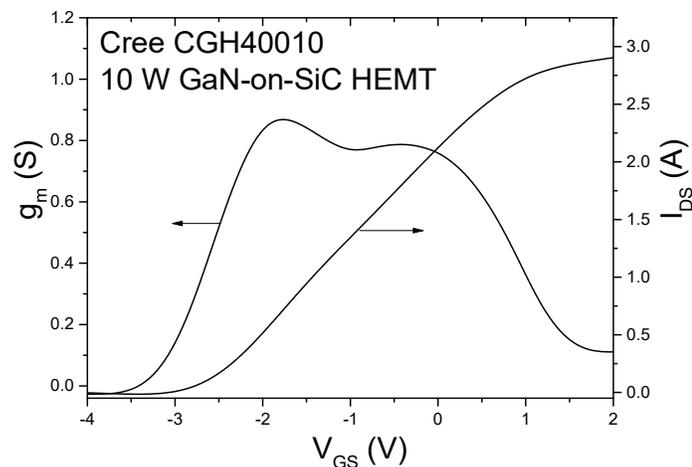


Figure 4.43: Measured drain current (I_{DS}) versus gate-to-source voltage (V_{GS}) and corresponding transconductance (g_m) for the Cree CGH40010 (10 W GaN-on-SiC HEMT).

Figure 4.43 shows the measured drain current and corresponding transconductance for the 10W GaN-on-SiC HEMT.

4.6.2 Cree CGH40025 (25 W GaN-on-SiC HEMT)

As shown in Table 4.11, the parameter values for the Cree CGH40025, a 25 W GaN-on-SiC HEMT are extracted for various bias points of $I_{DSq} = 90$ mA, 150 mA, 250 mA, 350 mA and 450 mA at $V_{DS} = 28$ V.

Table 4.11 Extracted parameter values of Cree CGH40025 at $V_{DS} = 28$ V, $I_{DSq} = 90$ mA, 150 mA, 250 mA, 350 mA and 450 mA, Frequency = 0.2 - 3.5 GHz

Extrinsic Parameters	C_{pg} (pF)	0.1861					
	C_{pd} (pF)	0.1861					
	L_s (nH)	0.03422					
	L_d (nH)	0.4640					
	L_g (nH)	0.4958					
	R_s (Ω)	0.0017					
	R_d (Ω)	1.1358					
	R_g (Ω)	0.8041					
	I_{DSq}	90mA	150mA	250mA	350mA	450mA	Change from 90mA to 450mA
Intrinsic Parameters	C_{gd} (pF)	0.5287	0.5318	0.5542	0.5714	0.588	11.22 %
	C_{ds} (pF)	2.398	2.482	2.515	2.545	2.692	12.26 %
	C_{gs} (pF)	11.75	12.67	13.31	13.85	14.17	20.60 %
	g_m (S)	0.785	0.985	1.182	1.283	1.332	69.68 %
	g_{ds} (S)	0.007	0.009	0.011	0.013	0.015	114.29 %

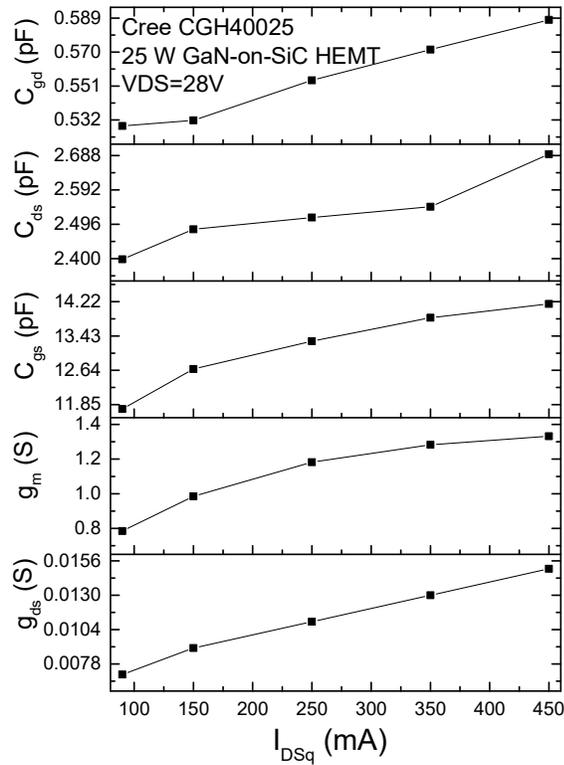


Figure 4.44: Comparison of intrinsic parameter values for the 25 W GaN-on-SiC HEMT (Cree CGH40025) at $V_{DS} = 28$ V, Freq = 0.4 - 4 GHz, $I_{DSq} = 90$ mA, 150 mA, 250 mA, 350 mA and 450 mA.

Figure 4.44 shows the intrinsic parameters values of the Cree CGH40025 plotted against the quiescent current I_{DSq} . It can be seen that the values of these bias dependent intrinsic parameters increase with the increase in quiescent current. The values of transconductance and output conductance, which depends on the conducting channel, show large variation as the number of carrier electrons in the 2DEG increases with the gate voltage.

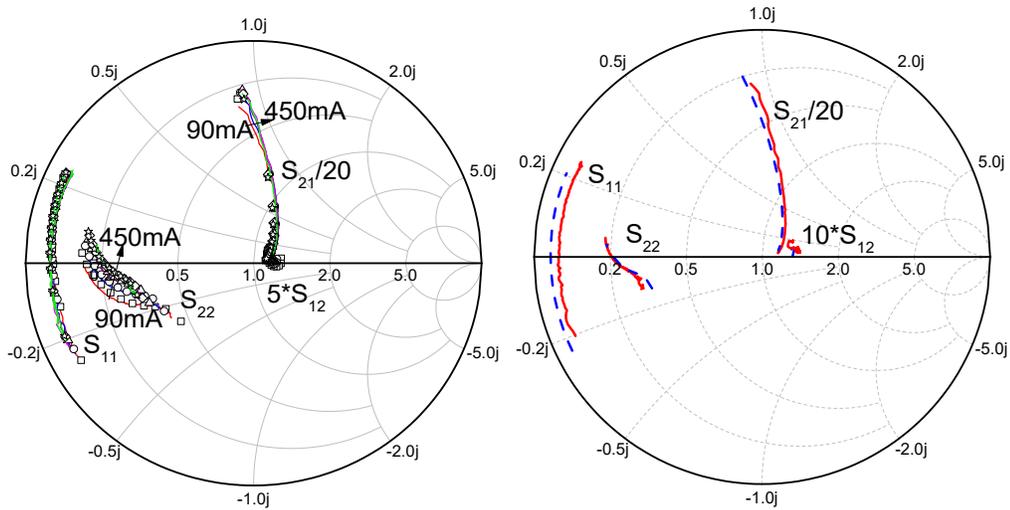


Figure 4.45: (Left) Comparison of measured (line) and modelled (symbol) S-parameters for the 25 W GaN-on-SiC HEMT (Cree CGH40025) at $V_{DS} = 28$ V, Freq = 0.4 – 4 GHz, $I_{DSq} = 90$ mA, 150 mA, 250 mA, 350 mA and 450 mA. The S-parameters are obtained after de-embedding the test fixture from measured data using SOLT calibration. (Right) Comparison of measured (solid) and simulated (dash) S-parameters using the vendor model at $V_{DS} = 28$ V, Freq = 0.4 – 4 GHz, $I_{DSq} = 450$ mA.

Figure 4.45 displays a good agreement between the modelled and measured S-parameters for the Cree CGH40025 to ensure the validation of the extracted parameter values at various bias points. Figure 4.45 also shows a comparison of the measured and simulated S-parameters using the large-signal model provided by the vendor at the bias condition of $V_{DS} = 28$ V and $I_{DSq} = 450$ mA. In our experience, and as the good agreement between the S-parameters suggests, the large-signal model for Cree CGH40025 can be considered as an example of an excellent vendor model. This can be clearly observed in the comparison of the simulated impedance values and RF performance with analytically calculated and experimentally measured results for a Class-AB RF PA presented in Chapter 5.

The measured drain current and corresponding transconductance characteristic are presented in Figure 4.46 and compared with the Cree CGH40010, a 10 W GaN-on-SiC HEMT from the same manufacturer

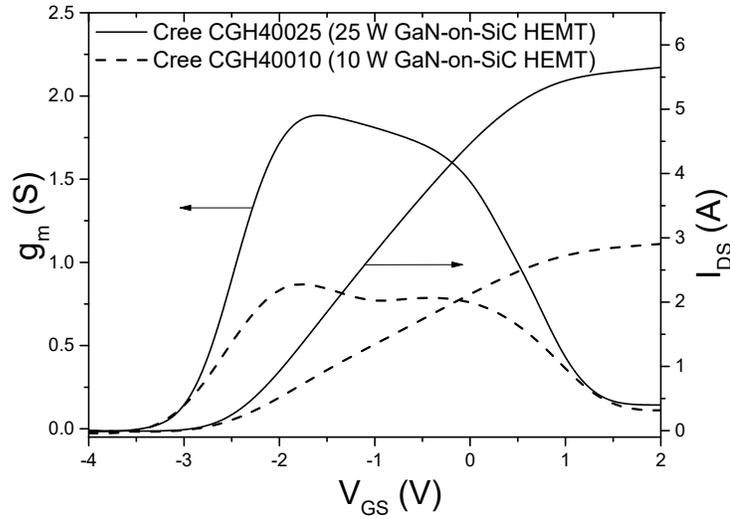


Figure 4.46: Measured drain current (I_{DS}) versus gate-to-source voltage (V_{GS}) and corresponding transconductance (g_m) for the Cree CGH40025 (25 W GaN-on-SiC HEMT) and Cree CGH40010 (10 W GaN-on-SiC HEMT).

The maximum values of I_{DS} and g_m are 5.65 A and 1.884 S for the 25 W HEMT compared to 2.90 A and 0.868 S for the 10W HEMT which shows the effect of scaling.

4.6.3 Nitronex NPTB00025 (25 W GaN-on-Si HEMT)

The NPTB00025, a 25 W GaN-on-Si HEMT from Nitronex has been chosen in this thesis to demonstrate the usefulness of the analytic approach in designing an RF power amplifier compared to using the vendor supplied large-signal model in harmonic balance simulation. The extracted values of the small-signal model parameters from measured and simulated S-parameters at $V_{DS} = 28V$ and $I_{DSq} = 450$ mA are presented in Table 4.13. The package model shown in Figure 4.47 for the Nitronex NPTB00025 has been provided by the vendor.

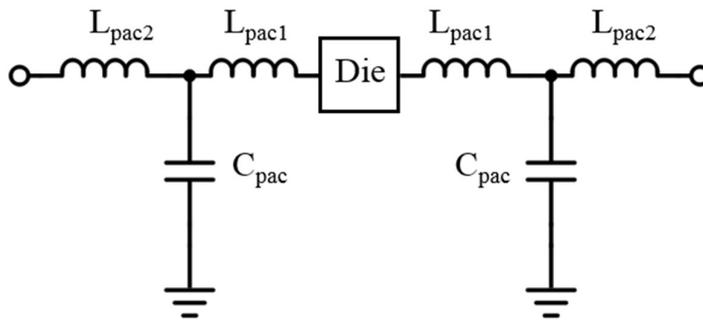


Figure 4.47: Vendor provided package model for Nitronex NPTB00025.

Table 4.12: Lumped element values of the package model for Nitronex NPTB00025.

C_{cap} (pF)	L_{pac1} (Ω)	L_{pac2} (nH)
0.46	0.1	0.1

Compared to the package model for the Cree CGH40010, this model does not take parasitic feedback capacitance and resistance due to the package into consideration. However, the values of these two parameters in Cree package model are 0.002 pF and 0.01 respectively which are negligible. A further difference is the value of parasitic inductance introduced by the packed is less compared to Cree package mode. The impact of parasitic elements introduced by the package on the impedance value and RF performance are later explored in Chapter 5.

Table 4.13 shows the parameters values for the Nitornex NPTB00025, a 25 W GaN-on-Si HEMT, extracted at the bias point of 450 mA at $V_{DS} = 28$ V from measured and simulated S-parameters using the large-signal model provided by the vendor.

Table 4.13 Extracted parameter values of Nitronex NPTB00025 at $V_{DS} = 28$ V, $I_{DSq} = 450$ mA, Frequency = 0.4 - 3.5 GHz

		Measured Data		Simulated Data
		Considering Package Separately	Without Considering Package Separately	
Package Parasitic	L_{pac1} (nH)	0.1	-	-
	L_{pac2} (nH)	0.1	-	-
	C_{pac} (pF)	0.46	-	-
Extrinsic Parameters	C_{pg} (pF)	0.2389	0.2534	0.2008
	C_{pd} (pF)	0.2389	0.2534	0.2008
	L_s (nH)	0.07696	0.0759	0.06240
	L_d (nH)	0.34829	0.5273	0.7212
	L_g (nH)	0.26645	0.5926	0.8273
	R_s (Ω)	0.01	0.01	0.191
	R_d (Ω)	0.846	0.761	1.62
	R_g (Ω)	0.609	0.569	0.195
Intrinsic Parameters	C_{gd} (pF)	0.7744	0.7541	0.620
	C_{ds} (pF)	3.055	3.005	2.54
	C_{gs} (pF)	12.80	12.38	11.23
	g_m (S)	1.012	1.005	1.078
	g_{ds} (S)	0.017	0.015	0.010

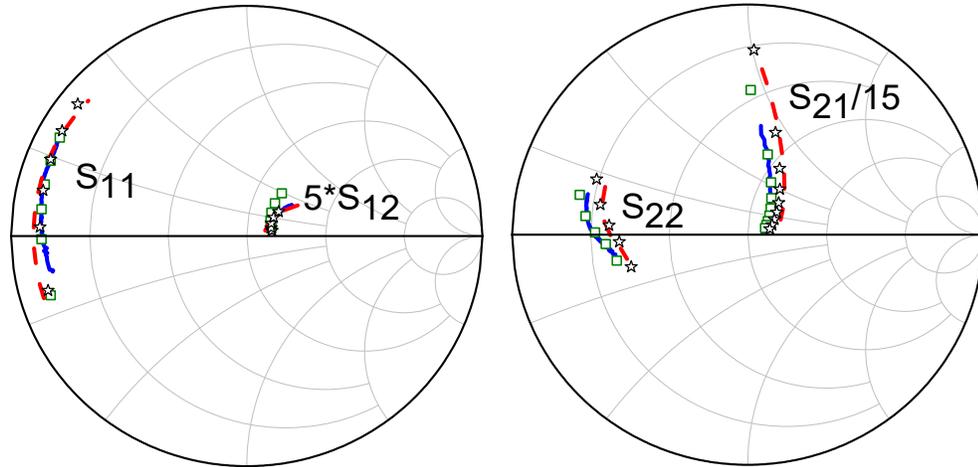


Figure 4.48: Measured (solid) and modelled (\square) S-parameters for the 25 W GaN-on-Si HEMT (Nitronex NPTB00025) at $V_{DS} = 28$ V, $I_{DSq} = 450$ mA, Freq = 0.4 - 3.5 GHz. It also shows the vendor model (dash) and modelled (\star) S-parameters from simulation. The S-parameters are obtained after de-embedding the test fixture from measured data using SOLT calibration.

Figure 4.48 shows measured and modelled S-parameters for the Nitronex 25 W GaN-on-Si HEMT. It also shows the simulated and modelled S-parameters using the large-signal model provided by the vendor. Good agreement of the modelled S-parameters in both cases shows the validation the obtain parameter values via extraction and optimization. Significant differences in S_{21} and S_{22} parameters from measurement and simulation using vendor model can be noted. The impact of the different between measurement and large-signal model provided by the vendor is explored in Chapter 5.

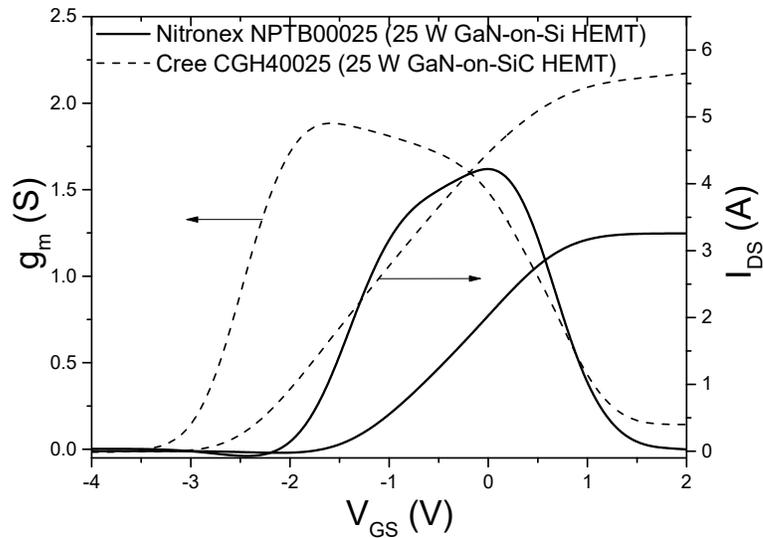


Figure 4.49: Measured drain current (I_{DS}) versus gate-to-source voltage (V_{GS}) and corresponding transconductance (g_m) for the Nitronex NPTB00025 (25 W GaN-on-Si HEMT) and Cree CGH40025 (25 W GaN-on-SiC HEMT).

Figure 4.49 shows the measured drain current and corresponding transconductance for the 25 W GaN-on-Si HEMT and the 25 W GaN-on-SiC HEMT. The lower value of drain current and narrower g_m - V_{GS} curve in GaN-on-Si HEMT indicate that the maximum output power and linearity would be less compared to the GaN-on-SiC HEMT.

4.6.4 RFHIC RT233 (2 W GaN-on-SiC HEMT)

The RT233, a 2 W GaN-on-SiC HEMT from RFHIC, does not have any large-signal vendor model to our knowledge. Therefore, one of the objectives in this thesis is to contribute to the large-signal modelling of this device using analytic approach. Secondly, the low power rating of this device allowed to experimentally extract the values input capacitance for a range of gate voltages from -3 V to 2 V to study its influence on optimum impedance values and RF performance. Table 4.14 shows the extracted parameter values for RT233 at $V_{DS} = 28$ V and $I_{DSq} = 140$ mA.

Table 4.14 Extracted parameter values of RFHIC RT233 at $V_{DS} = 28$ V, $I_{DSq} = 140$ mA, Frequency = 0.2 - 3.5 GHz

Extrinsic Parameters	C_{pg} (pF)	0.1507
	C_{pd} (pF)	0.1507
	L_s (nH)	0.06975
	L_d (nH)	0.911
	L_g (nH)	1.147
	R_s (Ω)	0.05
	R_d (Ω)	3.04
	R_g (Ω)	2.86
Intrinsic Parameters	C_{gd} (pF)	0.2008
	C_{ds} (pF)	0.9
	C_{gs} (pF)	6.94
	g_m (S)	0.294
	g_{ds} (S)	0.007
	R_i (nΩ)	0.003
	R_{gd} (nΩ)	0.0001

Figure 4.50 shows the simulated and measured S-parameters for the RT233 at $V_{DS} = 28$ V and $I_{DSq} = 140$ mA from 0.2 – 3.5 GHz.

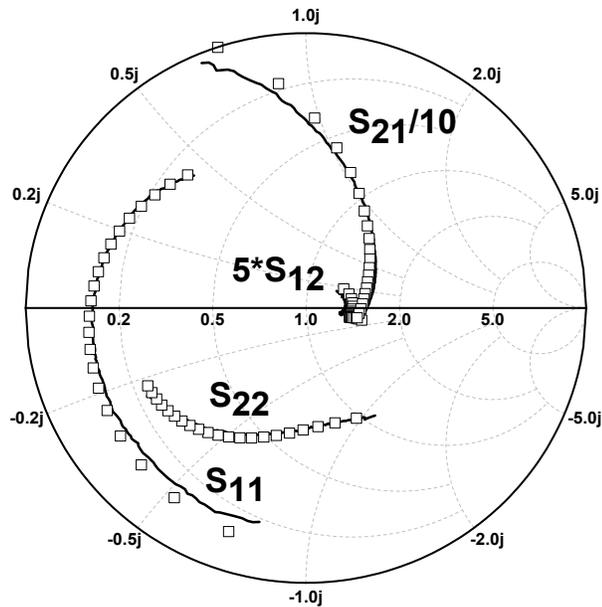


Figure 4.50: Comparison of measured (line) and modelled (symbol) S-parameters for the 2 W GaN-on-SiC HEMT (RFHIC RT233) at $V_{DS} = 28$ V, $I_{DSq} = 140$ mA, Freq = 0.2 - 3.5 GHz. The S-parameters are obtained after de-embedding the test fixture from measured data using SOLT calibration.

The good agreement between the simulated and measured S-parameters in Figure 4.50 ensures the validation of the extracted parameter values. The measured drain current and corresponding transconductance characteristic are presented in Figure 4.51.

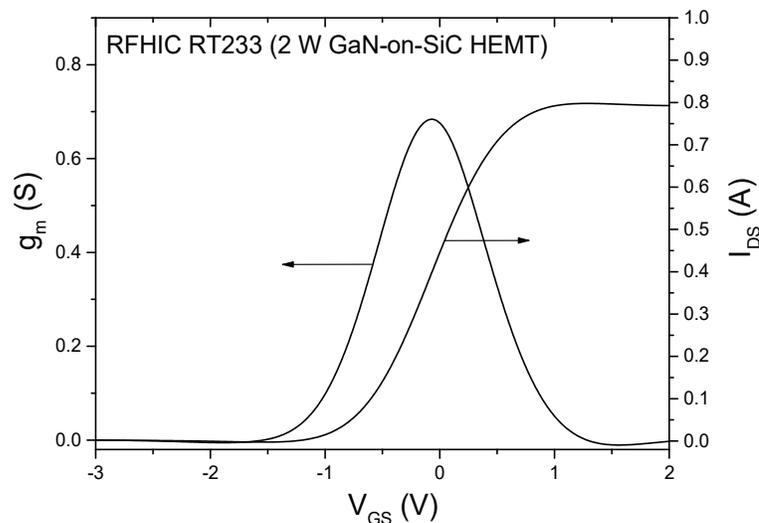


Figure 4.51: Measured drain current (I_{DS}) versus gate-to-source voltage (V_{GS}) and corresponding transconductance (g_m) for the 2 W GaN-on-SiC HEMT (RFHIC RT233).

It can be seen from Figure 4.51 that the RT233 lacks flatness in the transconductance characteristics and displays more of a peak; therefore, RT233 is expected to show poor linearity in a RF power amplifier.

4.6.5 Mitsubishi MGF0843G (20 W GaN-on-SiC HEMT)

Figure 4.52 shows the S-parameters for the MGF0843G, a 20 W GaN-on-SiC HEMT from Mitsubishi Electric, from 750 MHz to 8 GHz at $V_{DS} = 47$ V and $I_{DSq} = 180$ mA obtained from the datasheet, our measurement and simulation using the vendor provided model. The measured and simulated I-V characteristics are depicted in Figure 4.53.

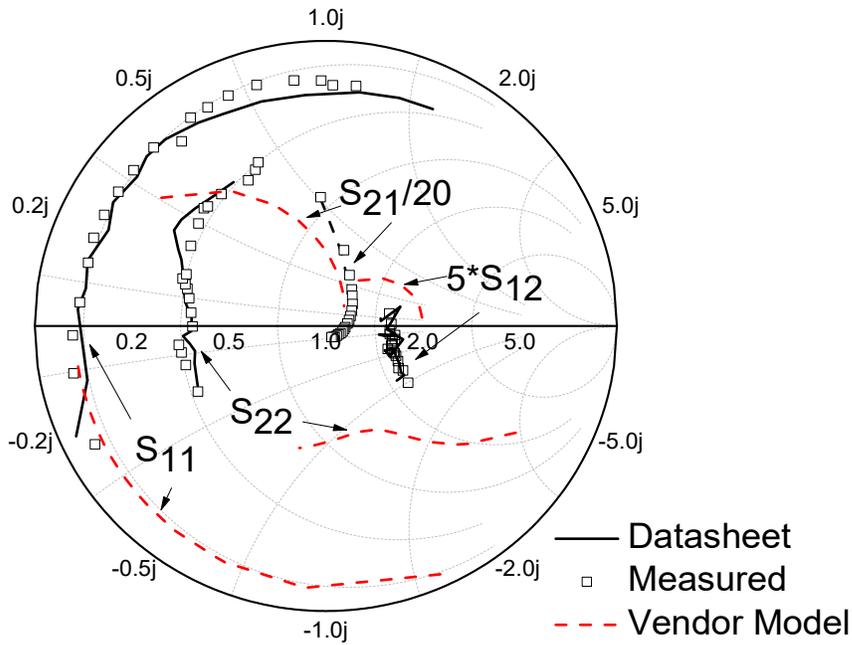


Figure 4.52: Comparison of S-parameters obtained from measurement (symbol), datasheet (solid line) and simulation using large-signal model provided by the vendor (dashed line) for the Mitsubishi MGF0843G (20W GaN-on-SiC HEMT) at $V_{DS} = 47$ V, $I_{DSq} = 180$ mA, Freq = 0.75 - 8 GHz. The S-parameters are obtained via direct measurement approach using TRL calibration.

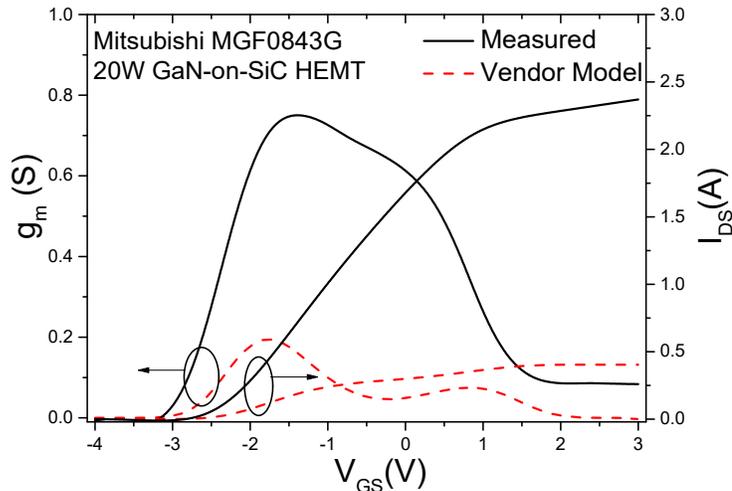


Figure 4.53: Measured and simulated (using vendor supplied large-signal model) drain current (I_{DS}) versus gate-to-source voltage (V_{GS}) and corresponding transconductance (g_m) for the Mitsubishi MGF0843G (20 W GaN-on-SiC HEMT).

It is evident that the large-signal vendor model lacks the accuracy to describe the RF and DC characteristic of the device. Therefore, an accurate model is necessary in order to design a RF power amplifier using this transistor. This thesis contributes to the construction of such a new model for Mitsubishi MGF0843G that can facilities prototyping. Compared to present cellular technologies that work up to 3 GHz, 5G applications will potentially utilize the higher frequency spectrum. A novel contribution of this work is extending the analytic approach up to 8 GHz. By implementing the TRL calibration kit described in section 4.4.4.3, the S-parameters are measured and a model is constructed up to 8 GHz. Table 4.15 shows the extracted parameter values at $V_{DS} = 47$ V and $I_{DSq} = 180$ mA.

Table 4.15 Extracted parameter values of Mitsubishi MGF0843G $V_{DS} = 47$ V, $I_{DSq} = 180$ mA, Frequency = 0.75 - 8 GHz

Extrinsic Parameters	C_{pg} (pF)	0.095
	C_{pd} (pF)	0.095
	L_s (nH)	0.05384
	L_d (nH)	0.7038
	L_g (nH)	0.6644
	R_s (Ω)	0.002
	R_d (Ω)	1.641
	R_g (Ω)	0.874
Intrinsic Parameters	C_{gd} (pF)	0.596
	C_{ds} (pF)	1.14
	C_{gs} (pF)	6.75
	g_m (S)	0.537
	g_{ds} (S)	0.005
	R_i (n Ω)	0.001
	R_{gd} (n Ω)	0.0007

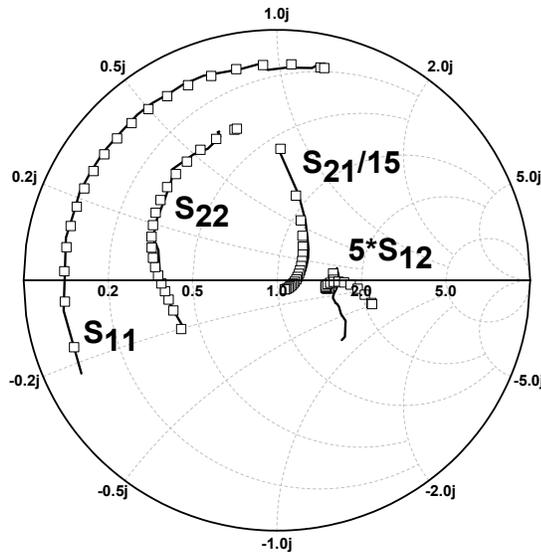


Figure 4.54: Comparison of measured (line) and modelled (symbol) S-parameters for the 20 W GaN-on-SiC HEMT (Mitsubishi MGF0843G) at $V_{DS} = 47$ V, $I_{DSq} = 180$ mA, Freq = 0.75 - 8 GHz. The S-parameters are measured via direct measurement approach using TRL calibration.

Figure 4.54 shows a good agreement between the simulated and measured S-parameters to ensure the validation of the extraction procedure and parameter values.

4.6.6 Freescale MRFE6VS25 (25 W Si LDMOS)

Table 4.16 shows the extracted parameter values for MRFE6VS25 at $V_{DS} = 50$ V and $I_{DSq} = 450$ mA.

Table 4.16 Extracted parameter values of Freescale MRFE6VS25 at $V_{DS} = 50$ V, $I_{DSq} = 450$ mA, Frequency = 0.2 - 2 GHz

Extrinsic Parameters	L_s (nH)	0.03001
	L_d (nH)	0.03719
	L_g (nH)	0.0475
	R_s (Ω)	0.045
	R_d (Ω)	1.497
	R_g (Ω)	0.646
Intrinsic Parameters	C_{gd} (pF)	0.1069
	C_{ds} (pF)	14.38
	C_{gs} (pF)	24.68
	g_m (S)	0.486
	g_{ds} (S)	0.003

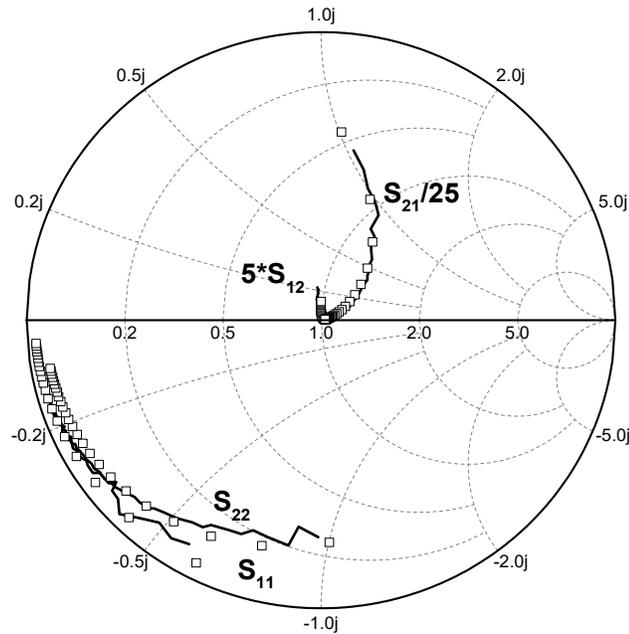


Figure 4.55: Comparison of measured (line) and modelled (symbol) S-parameters for the Freescale MRFE6VS25 (25W Si LDMOS) at $V_{DS} = 50$ V, $I_{DSq} = 450$ mA, Freq = 0.2 - 2 GHz. The S-parameters are obtained after de-embedding the test fixture from measured data using SOLT calibration.

Figure 4.55 shows a good agreement between the simulated and measured S-parameters using the procedure implemented earlier. Figure 4.56 shows the measured drain current and corresponding transconductance for MRFE6VS25 along with Cree

CGH40025 (25 W GaN-on-SiC HEMT) and Nitronex NPTB00025 (25 W GaN-on-Si HEMT)

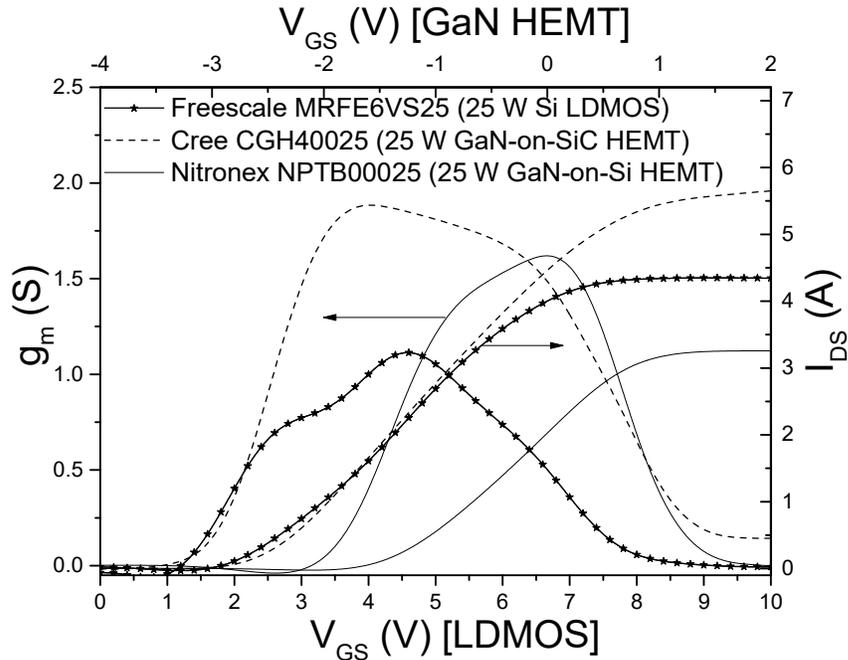


Figure 4.56: Measured drain current (I_{DS}) versus gate-to-source voltage (V_{GS}) and corresponding transconductance (g_m) for the Freescale MRFE6VS25 (25 W Si LDMOS), Cree CGH40025 (25 W GaN-on-SiC HEMT) and Nitronex NPTB00025 (25 W GaN-on-Si HEMT).

It can be seen from Figure 4.56 that CGH40025, the 25 W GaN-on-SiC HEMT from Cree has the highest saturation drain current and a broad and relatively flat transconductance curve. Therefore, the maximum output power and highest linearity are expected from CGH40025. Freescale MRFE6VS25, the 25 W silicon LDMOS has higher drain current and broader transconductance than the Nitronex NPTB00025, the 25 W GaN-on-Si HEMT. However, NPTB00025 has higher transconductance value compared to MRFE6VS25. The RF performance of these 25 W Si LDMOS and GaN-on-Si are compared in detail in chapter 5.

4.7 A Comparison of Parameter Values

Table 4.17 shows the extracted parameter values for the GaN HEMT and Si LDMOS devices rating from 2 W to 25 W over the range of frequencies from 200 MHz to 8 GHz presented in Section 4.6. The extracted extrinsic and intrinsic parameter values for all six devices are plotted against the device output power in Figures 4.57 - 4.62.

Table 4.17 Extracted parameter values for GaN HEMT and Si LDMOS devices rating from 2 W to 25 W over a range of frequencies from 200 MHz to 8 GHz.

	2W GaN-on-SiC	10W GaN-on-SiC	20W GaN-on-SiC	25W GaN-on-SiC	25W GaN-on-Si	25 Si LDMOS
Bias Condition	$V_{DS}=28\text{ V}$, $I_{DSq}=140\text{mA}$	$V_{DS}=28\text{ V}$, $I_{DSq}=340\text{mA}$	$V_{DS}=47\text{ V}$, $I_{DSq}=180\text{mA}$	$V_{DS}=28\text{ V}$, $I_{DSq}=450\text{mA}$	$V_{DS}=28\text{ V}$, $I_{DSq}=450\text{mA}$	$V_{DS}=50\text{ V}$, $I_{DSq}=450\text{mA}$
Cpg (pF)	0.1507	0.1145	0.095	0.1861	0.2534	-
Cpd (pF)	0.1507	0.1145	0.095	0.1861	0.2534	-
Ls (nH)	0.06975	0.039	0.05384	0.03422	0.0759	0.03001
Ld (nH)	0.911	0.6215	0.7038	0.4640	0.5273	0.03719
Lg (nH)	1.147	0.6505	0.6644	0.4958	0.5926	0.0475
Rs (Ω)	0.05	0.01435	0.002	0.0017	0.01	0.045
Rd (Ω)	3.04	1.43	1.641	1.1358	0.761	1.497
Rg (Ω)	2.86	1.33	0.874	0.8041	0.569	0.646
Cgd (pF)	0.2008	0.3339	0.596	0.588	0.7541	0.1069
Cds (pF)	0.9	1.570	1.14	2.692	3.005	14.38
Cgs (pF)	6.94	7.190	6.75	14.17	12.38	24.68
gm (S)	0.294	0.623	0.537	1.332	1.005	0.486
gds (S)	0.007	0.007	0.005	0.015	0.015	0.003
Ri	0.003	0.006	0.001	0.0042	0.03	-
Rgd	0.0001	0.00012	0.0007	0.0004	0.0017	-

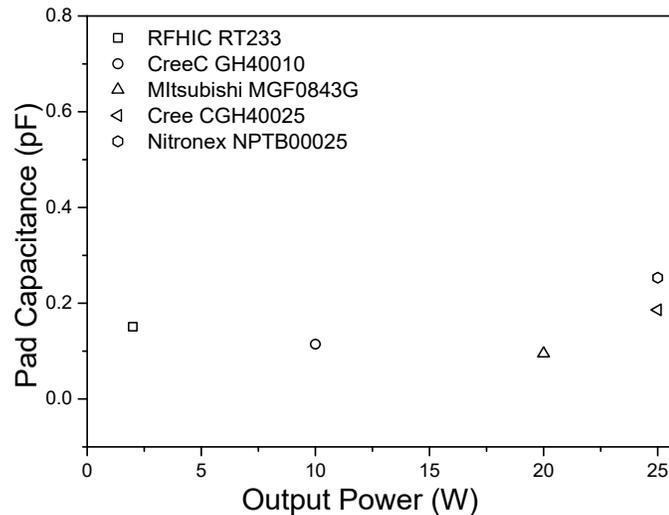


Figure 4.57: Comparison of extracted pad capacitance values for RFHIC RT233, Cree CGH40010, Mitsubishi MGF0843G, Cree CGH40025, and Nitronex NPTB00025.

It can be seen from Table 4.17 and Figure 4.57 that, except the devices from the same manufacturer, the pad capacitance values do not show any clear relationship with the output power. This can be attributed to the fact the different manufacturers implement different layouts for the bond pads.

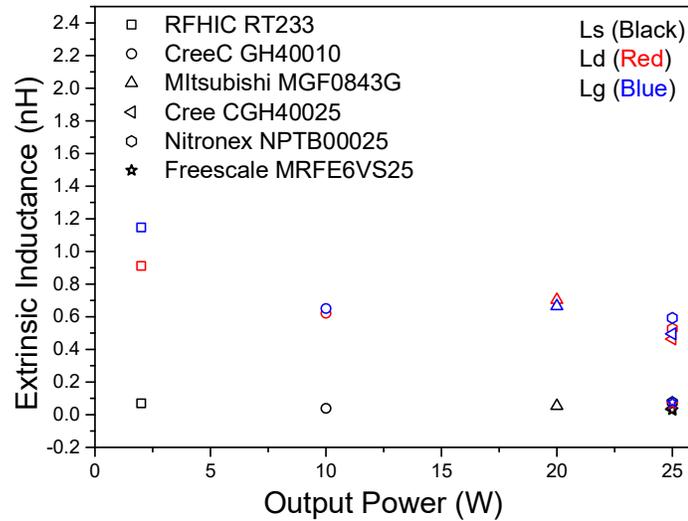


Figure 4.58: Comparison of extracted inductance values for RFHIC RT233, Cree CGH40010, Mitsubishi MGF0843G, Cree CGH40025, Nitronex NPTB00025 and Freescale MRFE6VS25

Figure 4.58 shows the extrinsic inductance values of all six devices. The package of the device as described in Section 4.6.1 and mutual inductance greatly influence the parasitic drain and gate inductance values. The source inductance depends on the connection to the back side of the die. The connection is established using through-via in GaN HEMT and source sinker diffusion in LDMOS. Therefore, the inductance values do not show any strong relationship with the output power as the devices use different packages.

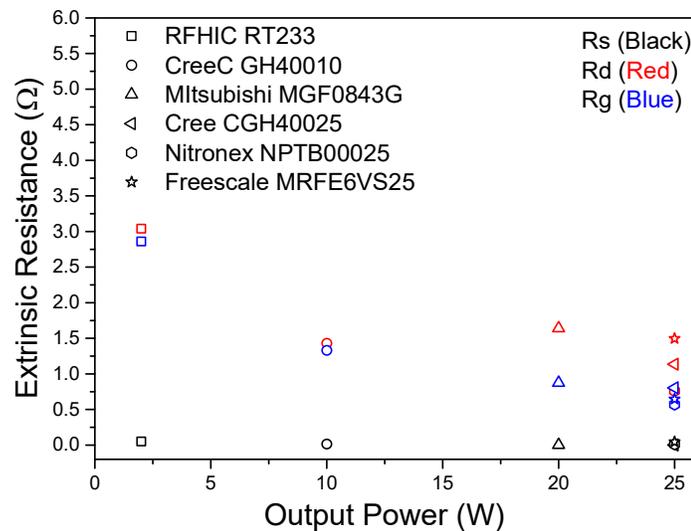


Figure 4.59: Comparison of extracted resistance values for RFHIC RT233, Cree CGH40010, Mitsubishi MGF0843G, Cree CGH40025, Nitronex NPTB00025 and Freescale MRFE6VS25.

Figure 4.59 shows the extrinsic resistance values of all six devices. The gate periphery, which is the total size of the FET, is larger in high output power devices and values of many parameters are directly influenced by it. The drain (R_d) and source (R_s) resistances or the access resistance generally display an inverse relationship with the gate periphery. The gate resistance due to Schottky contact depends on the number of gate fingers since $R_g \propto 1/\text{number of fingers}$.

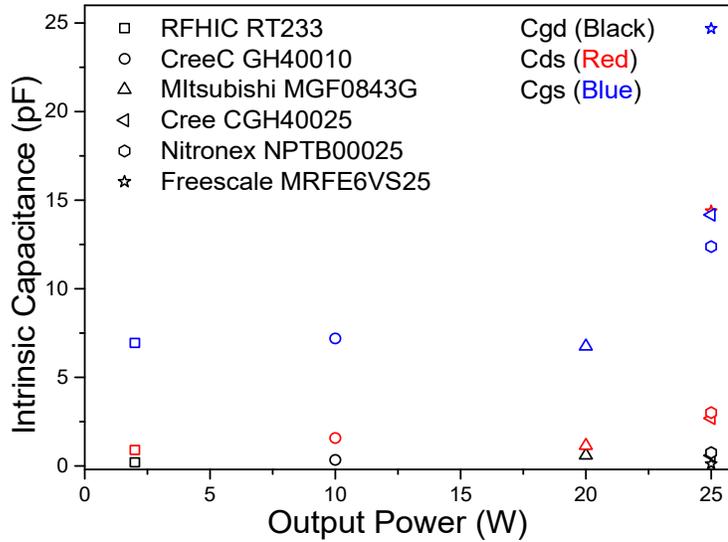


Figure 4.60: Comparison of extracted intrinsic capacitance values for RFHIC RT233, Cree CGH40010, Mitsubishi MGF0843G, Cree CGH40025, Nitronex NPTB00025 and Freescale MRFE6VS25.

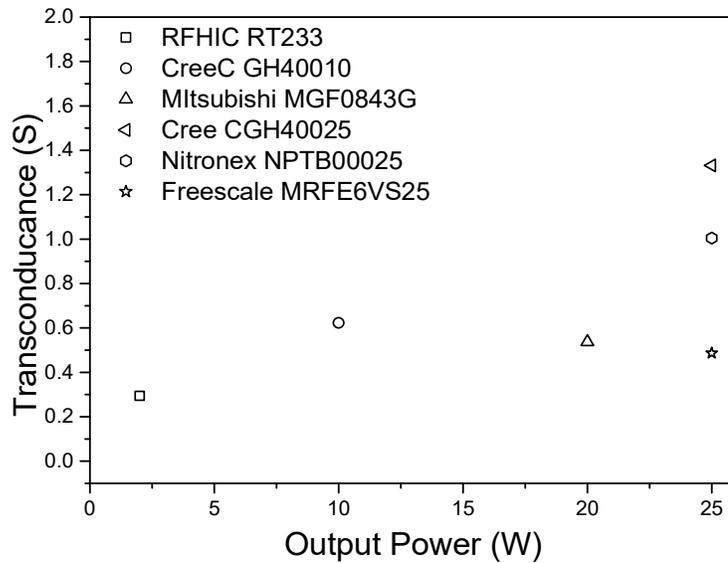


Figure 4.61: Comparison of extracted transconductance values for RFHIC RT233, Cree CGH40010, Mitsubishi MGF0843G, Cree CGH40025, Nitronex NPTB00025 and Freescale MRFE6VS25. Not just the peak but the width is also important for the linearity.

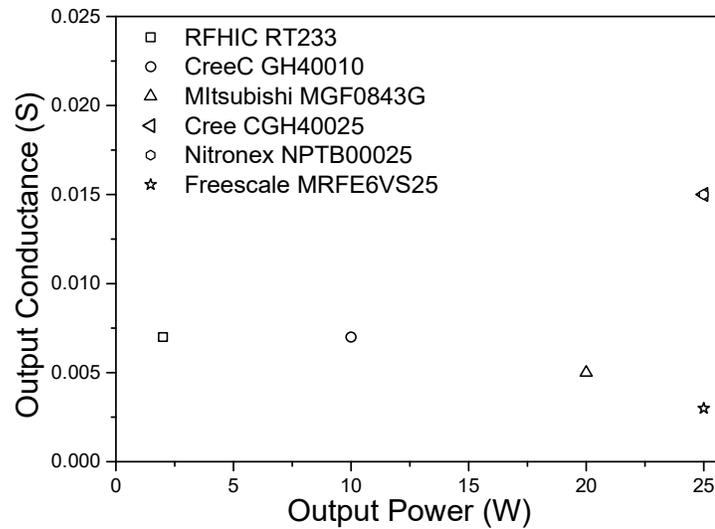


Figure 4.62: Comparison of extracted output conductance values for RFHIC RT233, Cree CGH40010, Mitsubishi MGF0843G, Cree CGH40025, Nitronex NPTB00025 and Freescale MRFE6VS25.

It can be seen from Figures 4.60 - 4.61 that for the GaN HEMT devices the intrinsic parameters in general exhibit an increasing trend as the output power increases. Since capacitance is proportional to the area, its value increases with gate periphery which is larger for device with higher output power. The total charge in the 2DEG also increases with device width. Due to a larger number of charge accumulation, a high power GaN HEMT has a low drain-to-source on-resistance (R_{ds}). Therefore, the output conductance (g_{ds}), which is the reciprocal of the drain-to-source on-resistance ($g_{ds} = 1/R_{ds}$), increases as the output power increases. The relationship between transconductance, a measure of how well the drain current is controlled by the gate voltage, and the output power is not so straight forward. The transconductance value of 25W HEMT from Cree is 1.332 S; this is twice of 0.623 S, the value of g_m in 10W HEMT from the same manufacturer. However, the 25 W transistors exhibit different transconductance values at the same quiescent current of 450 mA. The 25 W GaN-on-SiC HEMT has the highest current and transconductance values. The 25 W Si LDMOS shows higher drain current than the 25 W GaN-on-Si HEMT, but a lower value of transconductance. These results show that the device technology highly influences the extent to which the gate voltage can control the drain current. The effects of scaling can be observed clearly in the 10 W and 25 W GaN-on-SiC HEMTs since these two devices are from the same manufacturer. The GaN devices have much smaller on-resistance which results in higher output conductance compared to Si LDMOS and thus have higher output conductance.

Compared to the GaN devices with similar output power, the 25W Si LDMOS has higher values of C_{gs} and C_{ds} and lower value of C_{gd} . The capacitances in the GaN HEMT have been described in Section 4.3. Figure 4.62 shows the capacitances in a silicon LDMOS as described by G. Cao et al. [4.20].

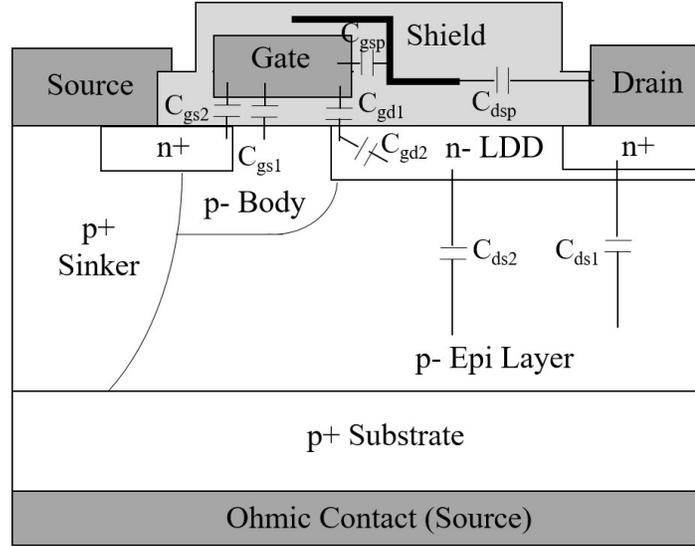


Figure 4.62: Capacitances in a silicon LDMOS.

The gate-to-source capacitance depends on the gate-to-channel capacitance between the gate and source (C_{gs1}), the overlap capacitance between gate and source diffusion (C_{gs2}), and the parasitic capacitance between gate and field plate (C_{gsp} .)

$$C_{gs} = C_{gs1} + C_{gs2} + C_{gsp} \quad (4.73)$$

The C_{gs} in the Si LDMOS is strongly influenced by the silicon dioxide and spacer technology at the gate. The large overlap of gate and source diffusion contributes to the large value of the C_{gs} in Si LDMOS. The drain-to-source capacitance C_{ds} in Si LDMOS can be primarily attributed to the junction capacitances between the p- epi layer and the heavily doped drain and light doped drift region. It also has a parasitic capacitance between drain and field plate (C_{gsp} .)

$$C_{ds} = C_{ds1} + C_{ds2} + C_{dsp} \quad (4.74)$$

The capacitances C_{ds1} and C_{ds2} are absent in GaN HEMT and this results in the lower value of C_{ds} compared to Si LDMOS. The feedback capacitance, C_{gd} , in LDMOS is defined by the oxide capacitance of gate-LDD overlap (C_{gd1}) and the capacitance between gate and drift region (C_{gd2}) which depends on the doping of the drift region

and bias condition [4.20], [4.21]. Since these capacitances are in series, the total feedback capacitance in Si LDMOS is given by:

$$C_{gd} = \frac{C_{gd1} \times C_{gd2}}{C_{gd1} + C_{gd2}} \quad (4.75)$$

Reduction of gate and LDD overlap and light doping in the drift region leads to small values of C_{gd2} and C_{gd3} and the feedback capacitance is decreased [4.21]. The shield over the gate prevents interaction between the gate and the drain and helps to keep the feedback capacitance low. It can be mentioned that most of the commercially available GaN HEMT devices now use SiN_x for passivation which has high dielectric constant that can further increase the parasitic capacitance [4.22], [4.23] in these devices. However, the source-terminated field-plate prevents the interaction between gate and drain/source and eliminates such parasitic capacitance.

The parameters values are first extracted and then optimized to achieve a good fit of the simulated S-parameter to measured data. Although the optimization algorithm always aims to minimize the total error, the maximum obtainable accuracy is limited by the numerical calculation. Therefore, errors can be introduced by the extraction procedure and optimization algorithm, and can affect the accuracy of the analytic approach. The effects of parameter values on the calculated optimum impedance values and RF performance are studied using analytic expressions and are presented in Chapter 5.

4.8 Summary

In this chapter, the errors involved in the measurements and various correction procedures are discussed. A TRL calibration kit is designed and implemented to measure the S-parameters up to 8 GHz. A parameter extraction method, which is a combination of several techniques, is presented to construct a small-signal model. The obtained parameter values are then validated for commercial RF devices via a comparison of measured and simulated s-parameters of the small-signal models. In this chapter, new models for the Mitsubishi MGF0843G and RFHIC RT233 are proposed due to lack of accuracy and unavailability of the models respectively. The relationships among the device technology, output power and the parameter values of the equivalent circuit model are also studied by comparing the extracted values for the GaN HEMT and Si LDMOS devices rating from 2 W to 25 W. Peculiar scaling trends

are evident from described characteristics. This is a first comprehensive comparison such parts and technologies to our knowledge.

References

- [4.1] G. Chen, V. Kumar, R. S. Schwindt, and I. Adesida, “A low gate bias model extraction technique for AlGa_N/Ga_N HEMTs,” in *IEEE Transactions on Microwave Theory and Technique*, vol. 54, no. 7, pp. 2949–2952, 2006.
- [4.2] J. Lu, Y. Wang, L. Ma, and Z. Yu, “A new small-signal modeling and extraction method in AlGa_N/Ga_N HEMTs,” *Solid-State Electronics*, vol. 52, no. 1, pp. 115–120, 2008.
- [4.3] A. Jarndal and G. Kompa, "A new small signal model parameter extraction method applied to GaN devices," *IEEE MTT-S International Microwave Symposium Digest*, pp. 1423–1426, 2005.
- [4.4] Keysight Technologies (formerly Agilent Technologies), “Tuning, Optimization and Statistical Design”, 2016 [Online]. Available: <http://edadocs.software.keysight.com/display/ads201601/Tuning,+Optimization,+and+Statistical+Design>
- [4.5] Keysight Technologies, “Applying Error Correction to Network Analyzer Measurements.”, USA, Application Note AN 1287-3, 2002.
- [4.6] Keysight Technologies, “Accurate Measurement of Packaged RF Devices,” USA, White Paper, 1995.
- [4.7] Keysight Technologies, “Signal Integrity Analysis Series. Part 3: The ABCs of De-Embedding.”, USA, Application Note, 2007.
- [4.8] Keysight Technologies, “De-embedding and Embedding S-Parameter Networks Using a Vector Network Analyzer,” USA, Application Note 1364-1, 2004.
- [4.9] J. P. Dunsmore, *Handbook Microwave Component Measurements with Advanced VNA Techniques*, Chichester, UK, John Wiley & Sons, Ltd., 2012.
- [4.10] Keysight Technologies, “In-fixture Microstrip Device Measurements Using TRL * Calibration,” USA, Product Note PN 8720-2 , 2000.
- [4.11] Keysight Technologies, “In-Fixture Measurements Using Vector Network Analyzers,” USA, Application Note AN 1287-9, 2006.

- [4.12] Keysight Technologies, “Advanced Design System” *Website*: <http://www.keysight.com/en/pc-1297113/advanced-design-system-ads?cc=US&lc=eng>.
- [4.13] B. J. Fleury and O. Bernard, “Designing and Characterizing TRL Fixture Calibration Standards for Device Modeling,” *Applied Microwave and Wireless*, pp. 26–42, 2001.
- [4.14] R. Pengelly, “Large Signal Modeling of GaN HEMT based Circuits,” May, 2010.
- [4.15] R. Rhea, “The Yin-Yang of Matching Part 1- Basic Matching Concepts,” High Frequency Electronics, 2006. [Online] Available: http://highfrequelec.summittechmedia.com/Mar06/HFE0306_Rhea.pdf.
- [4.16] G. Dambrine, A. Cappy, F. Heliodore, and E. Playez, “A New Method for Determining the FET Small-Signal Equivalent Circuit,” in *IEEE Transactions on Microwave Theory and Technique*, vol. 36, no. 7, pp. 1151–1159, 1988.
- [4.17] J. A. Zaudio Flores, “Device Characterization and Modeling of Large-Signal GaN HEMTs,” PhD Dissertation, Faculty of Electrical Engineering and Computer Science, The University of Kassel, Kassel, Hesse, Germany, 2012.
- [4.18] M. Berroth and R. Bosch, “High-frequency equivalent circuit of GaAs FET’s for large-signal applications,” in *IEEE Transactions on Microwave Theory and Technique*, vol. 39, no. 2, pp. 224–229, 1991.
- [4.19] R. Gaddi, P. J. Tasker, and J. A. Pla, “Direct extraction of LDMOS small signal parameters from off-state measurements,” *Electronics Letters*, vol. 36, no. 23, pp. 1964–1966, 2000.
- [4.20] G. Cao, S. K. Manhas, E. M. S. Narayanan, M. M. De Souza, and D. Hinchley, “Comparative study of drift region designs in RF LDMOSFETs,” in *IEEE Transactions on Electron Devices*, vol. 51, no. 8, pp. 1296–1303, 2004.
- [4.21] S. Xu, P. Foo, J. Wen, Y. Liu, F. Lin and C. Ren, "RF LDMOS with extreme low parasitic feedback capacitance and high hot-carrier immunity," Electron Devices Meeting, 1999. IEDM '99. Technical Digest. International, Washington, DC, USA, 1999, pp. 201-204.

[4.22] S. Rajan, Y. Pei, Z. Cheng, S. P. DenBaars and U. K. Mishra, "Surface Passivation of AlGa_N/Ga_N HEMTs," *Device Research Conference, 2008*, Santa Barbara, CA, 2008, pp. 131-132.

[4.23] W. Lu, V. Kumar, R. Schwindt, E. Piner, and I. Adesida, "A comparative study of surface passivation on AlGa_N/Ga_N HEMTs," *Solid-State Electronics*, vol. 46, no. 9, pp. 1441–1444, 2002.

Chapter 5

New Analytical Approach to Large-Signal Modelling of Class AB RF Power Amplifier Considering Elements of Package and Validation of Analytic Approach via Measurements

Abstract

New analytical expressions are derived from the equivalent circuit lumped element model considering package parasitic in chapter 4. This chapter focuses on establishing the accuracy and validity of the analytic approach in obtaining the optimum impedance values to design linear radio frequency power amplifiers (RF PAs) and analysing the RF performance. The accuracy of the method at different bias conditions, optimization criteria and high frequency is first validated via HB simulation. The accuracy is then evaluated for 25 W GaN HEMT based linear RF PAs at the frequency of 3.25 GHz for the first time with experimental results. The RF PA built using the calculated impedance values from the analytic approach demonstrates an average of 2 dB higher power gain, 1.3-1.8 dB higher output power at P1dB and 8-13% higher efficiency in comparison to the amplifier designed using impedances predicted by the vendor model. The error margin for measured results for power gain, P1dB and PAE compared to prediction are reduced to -2.7%, -8.2% and 10.5% from -34%, -12.8% and -54% respectively in comparison to results from HB simulation using the vendor model. The effects of nonlinear input capacitance and package parasitic along with equivalent circuit parameter values and I-V characteristics on the analytically calculated impedance values and RF performance are examined.

5.1 Introduction

An RFPA is designed by realizing input and output matching networks to present optimum source and load impedances to the transistor to ensure the maximum power transfer from the source to the input of the transistor and from the output of the transistor to the load. Therefore, choosing the optimum impedance values is significant for the performance of RF power amplifiers. Designers often use various optimization criteria of maximum linearity, power gain or power added efficiency, in order to meet required specifications. Conventionally load-pull/source-pull with impedance tuners or large-signal models in harmonic balance (HB) simulation are used to obtain the optimum impedance values. As a simple and quick alternative to these methods, the analytical approach was developed [5.1] – [5.3] to design the RFPA and to predict the RF performance. In this method, analytical expressions are derived from the equivalent circuit model of the transistor and used for the calculation of optimum load and source impedances, output and input power, power gain and linearity.

In this chapter, validation of the analytical approach to calculate the optimum impedance values and to predict RF performance is demonstrated. Harmonic balance (HB) technique and analytic approach are described first. Since commercial RF transistors are available in different packages and the parasitic elements introduced by the package affects device performance, new analytical expressions are derived based on a 19-element model considering the package parasitic as shown in Figure 4.25 in Chapter 4. The analytic approach is then extended by proposing a method to optimize the impedance values for different criteria popularly used by designers, viz. maximum power gain, linearity and efficiency. The accuracy of the analytic approach is first verified via HB simulations. Then the measured results for three prototype RF power amplifiers designed at a high frequency of 3.25 GHz using 25 W GaN HEMT devices are used as another benchmark to evaluate the validity of analytic approach. The unique advantage of the analytical approach is to directly link the device performance to its extrinsic and intrinsic elements of the equivalent circuit model and thus to its physical structure. The uncertainty and error introduced from measurement, characterization and assumptions can introduce errors and inaccuracy in the calculated results. Using the analytic approach, the effects of various sources of error are studied.

5.2 Harmonic Balance Technique

Prototyping an RFPA is an expensive affair. Therefore, designers require the support of simulation tools to minimize errors, reduce costs and accelerate the design process. In the early days of nonlinear circuit analysis, time-domain simulation tools such as SPICE were the primary choice for nonlinear circuit simulation. However, this method becomes inefficient for highly nonlinear circuits at high frequency. In order to find a solution, the unknown voltages at nodes and branch currents in a circuit are often sampled thousands of times which requires a lot of computer memory and time. Designers use capacitors to block the DC at the RF input and output ports and inductors to choke the RF signal off from the DC bias networks. Such components usually have high quality factor. In order to obtain the transient response of these elements, the simulation must run for thousands of cycles. Simulating distributed circuit elements in time-domain is also ineffective and unreliable. In RF and microwave applications, multi-tone simulation is a very common practice, and this has been proven to be troublesome to manage in time-domain simulators. In addition, the nonlinearity leads to the creation of components at harmonic frequencies and intermodulation distortion. Therefore, the simulator should have a time step appropriate for the highest frequency and at the same time, also for the lowest frequency. All these short-comings can be overcome by harmonic balance (HB) simulations.

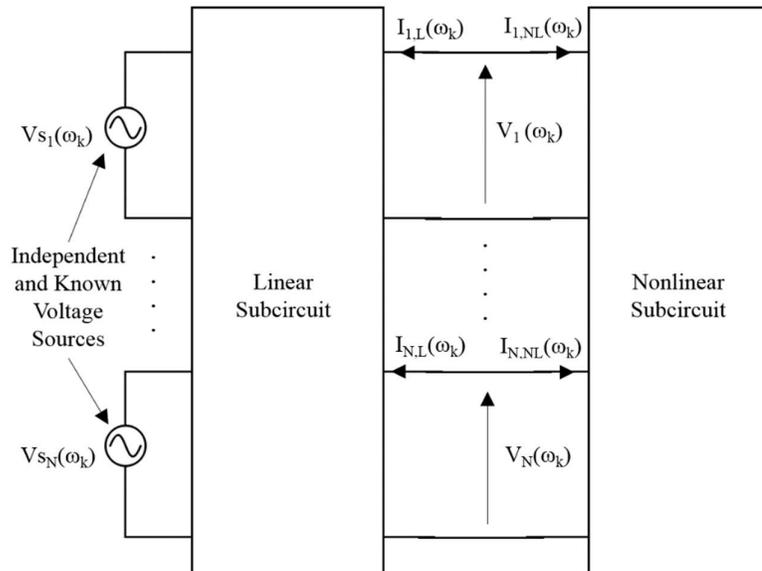


Figure 5.1: The principle of HB simulation.

The harmonic balance (HB) approach is a powerful frequency-domain technique that uses numerical mathematics to analyse a high frequency nonlinear system and obtain its steady-state response directly. The principle behind HB simulation is to partition the circuit into two interconnecting subcircuits as illustrated in Figure 5.1. One subcircuit contains the linear elements and the second incorporates nonlinear components. Here, ω_k is the set of frequencies being considered in the analysis.

The HB approach is an application of Kirchhoff's current law (KCL) which states that the sum of current at all nodes should be zero. The currents of the linear subnetwork are obtained from the relationships of the signal voltages ($V_{S1}(\omega_k), V_{S2}(\omega_k), \dots, V_{SN}(\omega_k)$) and the admittances or Y-parameters. In a HB simulator these voltages are known, and hence the current for the linear subcircuit ($I_{1,L}(\omega_k), I_{2,L}(\omega_k), \dots, I_{N,L}(\omega_k)$) can be easily computed. In the frequency domain formulation of the circuit equations, the unknown voltage waveforms of the interconnecting ports ($V_1(\omega_k), V_2(\omega_k), \dots, V_N(\omega_k)$) are represented in their phasor forms at each of the frequency. Using inverse Fourier transform, the voltage waveforms are then converted from the frequency-domain into time-domain. The nonlinear network currents are calculated in the time-domain and converted back to frequency-domain using Fourier transform. The sum of linear and nonlinear currents is checked to satisfy the KCL. Therefore, the goal of the analysis in HB simulation is finding a set of voltage phasors so that Kirchhoff's laws satisfied at each of the interconnecting ports, i.e.:

$$\text{Find: } V_1(\omega_k), V_2(\omega_k), \dots, V_N(\omega_k) \quad (5.1)$$

$$\text{So that: } |I_L(\omega_k)| = |I_{NL}(\omega_k)| \quad (5.2)$$

A solution is found if the currents for the linear and nonlinear sub-circuits are same or in other words, balanced at each harmonic frequency. This is why this method is called harmonic balance technique. The goal is usually never met at the first attempt, and therefore several iterations and an optimization method is employed to adjust the voltages and currents. An error function (ϵ) is used to calculate the margin of error in KCL. Typically, in HB simulation, a solution is obtained when the value of this error function becomes very small for each interconnecting port.

$$|I_L(\omega_k)| = |I_{NL}(\omega_k)| < \epsilon_{desired} \quad (5.3)$$

At this point the simulation is considered to be converged and the corresponding voltages and currents are the steady-state solution of the nonlinear system.

Although an infinite number of harmonics can be considered in HB, for practical purpose a limited number of harmonics are considered taking computation time and power into account. However, insufficient number of harmonic components, especially for highly nonlinear circuit such as an RFPA operating in gain compression, affects the accuracy of the solution. In addition, this can lead to convergence problem. Typically, the designers consider up to 7th to 9th harmonic components as a trade-off between accuracy, computation time and resources. The optimization method used can be another source of inaccuracy and convergence problem in HB simulation.

It has to be mentioned that the nonlinear device models used for RF PA design are a very common source of convergence problem in HB simulation. Generally, this difficulty arises from the discontinuities in the model equations and their derivatives, incorrectly entered or extracted parameter or coefficient values.

5.2.1 Load-pull and Source-pull Simulations and Designing RFPAs for Different Criteria

The optimum impedance values to design an RF PA using a transistor can be determined from load-pull and source-pull simulations in a HB simulator such as ADS using the large-signal model of the device.

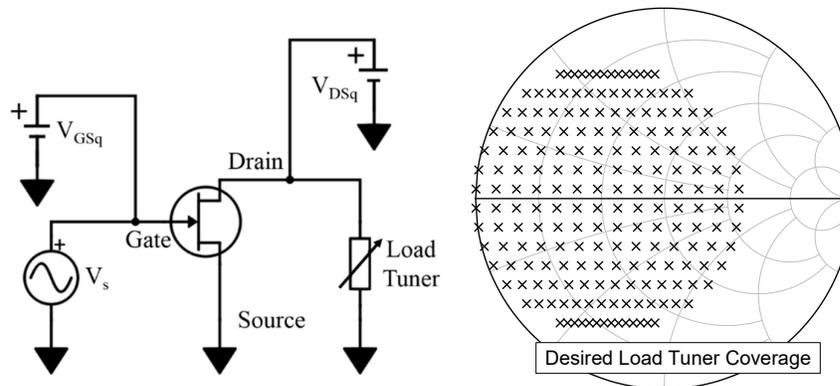


Figure 5.2: Schematic diagram of a load-pull simulation in ADS.

In a load-pull simulation, the impedance at the output is tuned by sweeping the load reflection coefficients in a desired region in the Smith chart, as displayed in Figure 5.2, at a constant available source power for defined frequency and bias voltages. The

contours of equal delivered power and power-added-efficiency are generated on the Smith chart as shown in Figure 5.3.

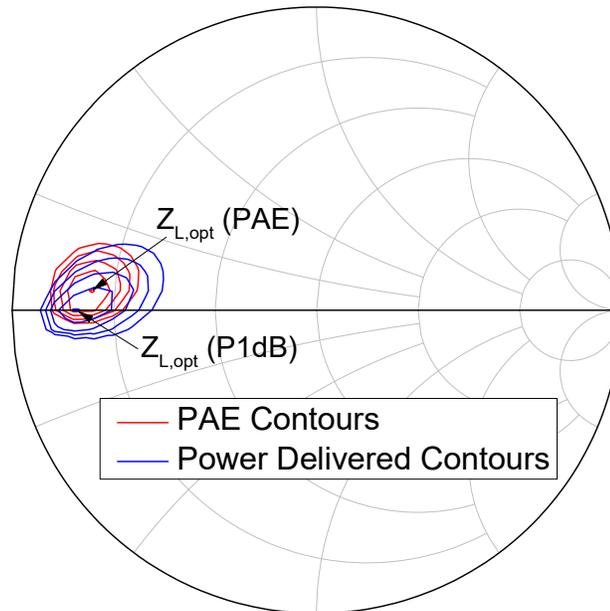


Figure 5.3: Power-added-efficiency (PAE) and power delivered contours obtained from load-pull simulation in ADS.

Since the input power remains constant, this means that the variations of the delivered power or PAE are due to the variations of just the load impedance. An impedance is considered as optimal when the delivered output power or the power-added-efficiency is maximum. It can be observed that the maximum delivered power and maximum PAE are obtained at different impedance values. The optimum load impedance value, $Z_{L,opt}$, for maximum linearity and PAE can be obtained from the power delivered or PAE contours respectively. The optimum load impedance value for maximum gain is obtained from the delivered power contour with the source power set to the small-signal power level which is typically less than 10 dBm. In the next step, the optimum source impedance, $Z_{S,opt}$, is determined in a similar procedure where the value of the source impedance is tuned while the optimum load impedance determined in the previous step is set at the load termination.

Once the optimum impedance values are obtained, the matching network circuits are designed in ADS and the RFPA is simulated to predict the gain, output power and power-added-efficiency.

5.3 Analytic Approach

In 1983, Cripps [5.4] first analytically showed the impact of load impedance on load-pull contours and also demonstrated that simple equations could lead to good agreement with experiment. As described in Chapter 2, the load line match is a practical solution to obtain the maximum power from an amplifier by selecting a value of load resistance that allows maximum voltage and current swing within the limit of the transistor.

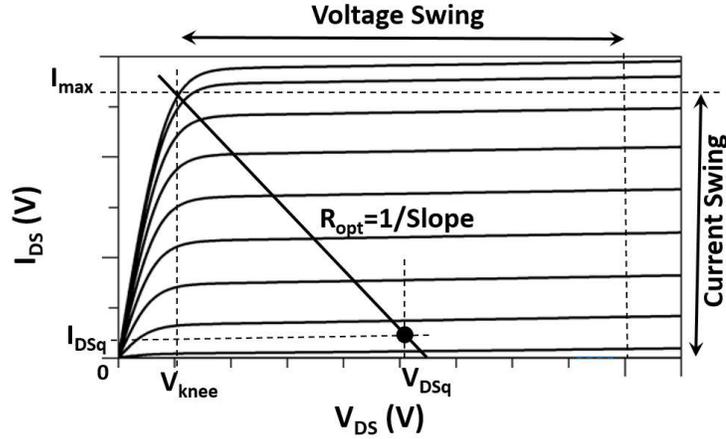


Figure 5.4: Load line for a Class-AB amplifier.

Figure 5.4 shows the load line corresponding to maximum linear power for a class-AB amplifier. This value of optimum load resistance (R_{opt}) can be calculated from the following equation:

$$R_{opt} = \frac{V_{max}}{I_{max}} \frac{\pi(1 - \cos(\alpha/2))}{\alpha - \sin(\alpha)} \quad (5.4)$$

Where α is the conduction angle and can be determined from:

$$\alpha = 2 \cos^{-1} \left(\frac{I_{DSq}}{I_{DSq} - I_{max}} \right) \quad (5.5)$$

Here, I_{DSq} is the drain quiescent current and I_{max} is the amplitude of the drain current at $V_{GS} = V_{GS,max}$ and $V_{DS} = V_{knee}$, where $V_{GS,max}$ is the maximum gate voltage allowed for the device and V_{knee} is the knee voltage. The term V_{max} is the maximum voltage swing and is defined as the following:

$$V_{max} = 2(V_{DSq} - V_{knee}) \quad (5.6)$$

Here V_{DSq} is the drain quiescent voltage. It can be seen from (5.6) that the maximum voltage swing is primarily limited by the knee voltage and not by the breakdown voltage (V_{Br}) of the device since V_{Br} is typically more than twice the V_{DSq} . Therefore, the value of V_{knee} has to be obtained first in order to determine the load line and the optimum value of R_{opt} . It is defined as the drain-to-source voltage at which the device delivers the maximum linear output power. As shown in [5.2], it can be calculated numerically from (5.7):

$$P_{LIN,max} = \frac{1}{8} V_{max} I_{max} = \frac{1}{4} (V_{DSq} - V_{knee}) f(V_{GS,max}, V_{knee}) \quad (5.7)$$

Utilizing this load line concept, the authors in [5.1] – [5.3] derived analytical expressions based on a lumped element model of the device to obtain the optimum impedance values and RF performance. The basis of this method are a set of derived expressions describing the input and output voltages and currents of small-signal equivalent circuit model extracted from measured S-parameters and the Fourier transform of these waveforms.

According to the load line concept, the optimum load resistance R_{opt} is imposed on the intrinsic current generator. However, the measured I-V characteristics is always at the external terminals of the device. This extrinsic drain current $I_{DS,ext}$ is different from the intrinsic current $I_{DS,int}$ since it includes the effect of resistances R_g , R_d , R_s and R_{ds} . In analytic approach, the measured I-V curves are used directly in the analysis to obtain the load line.

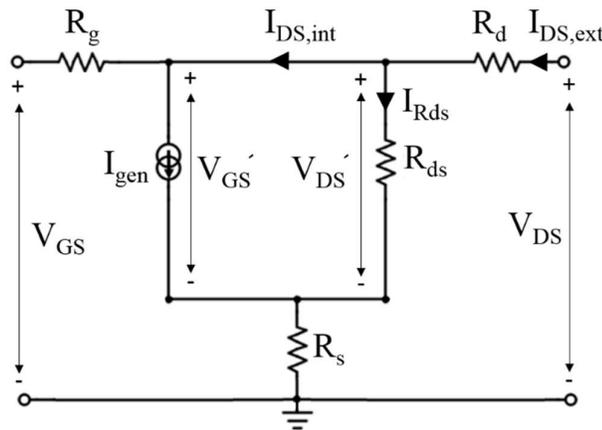


Figure 5.5: Equivalent circuit model to extract the intrinsic I-V characteristics from the measured I-V curves at the extrinsic plain.

$$I_{DS,int} = I_{DS,ext} - I_{R_{ds}} = I_{DS,ext} - \frac{V_{DS}'}{R_{ds}} = I_{DS,ext} - \frac{V_{DS} - I_{DS,ext}(R_d + R_s)}{R_{ds}} \quad (5.8)$$

Equation (5.8) derived from the circuit in Figure 5.5 allows to obtain the intrinsic I-V characteristics from the extrinsic measured I-V curves.

Figure 5.6 shows the drain-to-source current of Cree CGH40025, a 25 W GaN-on-SiC HEMT, at the intrinsic current generator after the extrinsic and intrinsic resistors are de-embedded using (5.8) from the output drain current measured at the extrinsic device plain.

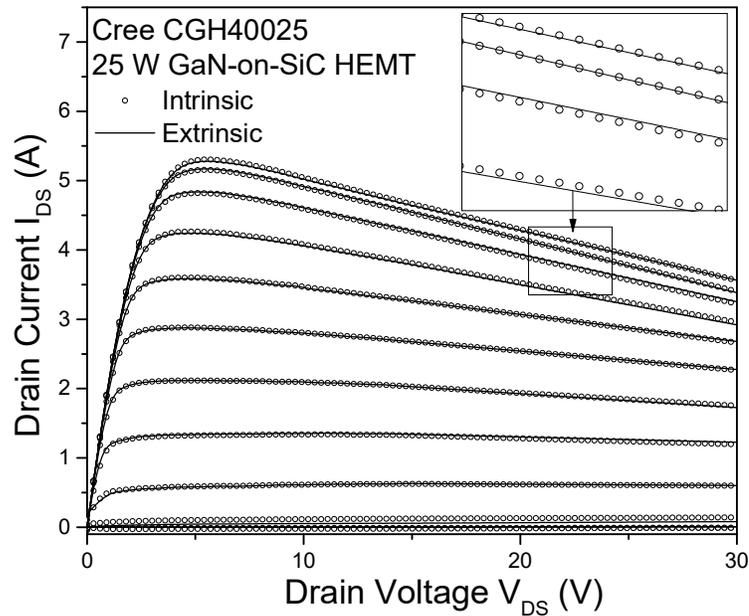


Figure 5.6: Extrinsic and intrinsic output drain current of the 25 W GaN-on-SiC HEMT (Cree CGH40025).

It can be observed from Figure 5.6 that the difference between the output current at the intrinsic current generator and extrinsic measurement plain is not significant.

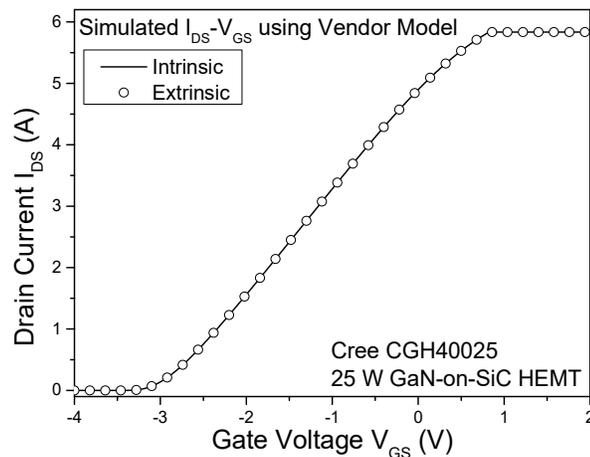


Figure 5.7: Simulated extrinsic and intrinsic output drain current of the 25 W GaN-on-SiC HEMT (Cree CGH40025) using the vendor model.

These simulated extrinsic and intrinsic I-V characteristics using the large-signal model provided by the vendor also do not show any difference as displayed in Figure 5.7. This validates the assumption of imposing optimum load (R_{opt}) on the current generator using the measured I-V characteristics in the analytic approach.

The difficulty and inaccuracy of reproducing the device characteristics with complex equations or a large number of parameter values or optimizing a lot of fitting coefficients is also avoided. Although this can be considered simplistic, in practice, it is proven to be very effective in predicting the optimum impedance values and the RF performance up to 7.5 GHz as demonstrated in this chapter. In addition, the unique approach for correlating device or process technology to actual RF performance allowed by this method is a feature which is not possible via HB simulation.

5.3.1 Optimization of Source and Load Impedances and Calculating RF Performance for Different Criteria

The work so far has only been done to obtain the optimum impedance values and predict the RF performance for maximum linear output power. In this chapter, a method to determine the optimum load and source impedance values of a RF transistor for the criteria of maximum gain and maximum efficiency is proposed by extending the analytic approach.

Maximum linearity and efficiency cannot be achieved at the same time because the optimum load resistance values for maximum efficiency and maximum linear output power are different. This trade-off can be attributed to the voltage and current swings at these different load resistances and corresponding output power and efficiency [5.4]. The voltage swing increases as the load resistance increases. On the other hand, the current swing decreases with increasing load resistance and becomes more and more bifurcated which leads to relatively low DC component. As a result, the amplifiers deliver higher output power at lower efficiency when the value of the load resistance is lower. At higher load resistance, the amplifier produces lower output power at higher efficiency. The optimization technique presented here is based on this principle.

As shown in Figure 5.4, the load line connects the bias point (V_{DSq} , I_{DSq}) and (V_{knee} , I_{max}) point. The values of the (I_{max} , V_{knee}) point are swept while I_{DSq} and V_{DSq} are kept constant. This results in different values of R_{opt} calculated using (5.4). The maximum

values of voltage and current swings also change accordingly. The corresponding impedance values and RF performance are calculated analytically for each value of R_{opt} . Traditionally in order to achieve the maximum gain, the source and load impedance values are conjugate matched. In this work the load line theory has also been applied to determine the impedance values optimized for maximum power gain.

5.3.2 New Analytic Expressions

Figure 5.8 shows a small signal equivalent model of an RF power transistor including the package parasitic. The values of the lumped elements have been extracted and presented in Chapter 4. C_{p1} , C_{p2g} and C_{p2d} are the package parasitic capacitances. R_{pg} and R_{pd} and L_{pg} and L_{pd} are the package parasitic resistances and inductances respectively. C_{pg} and C_{pd} are the extrinsic gate and drain pad capacitances. Resistors R_g , R_d and R_s are the extrinsic gate, drain and source resistances. Inductors L_g , L_d and L_s are the extrinsic gate, drain and source inductances. The input, feedback and output capacitances are represented by C_{gs} , C_{gd} and C_{ds} respectively. The forward transconductance and output conductance are represented by g_m and g_{ds} .

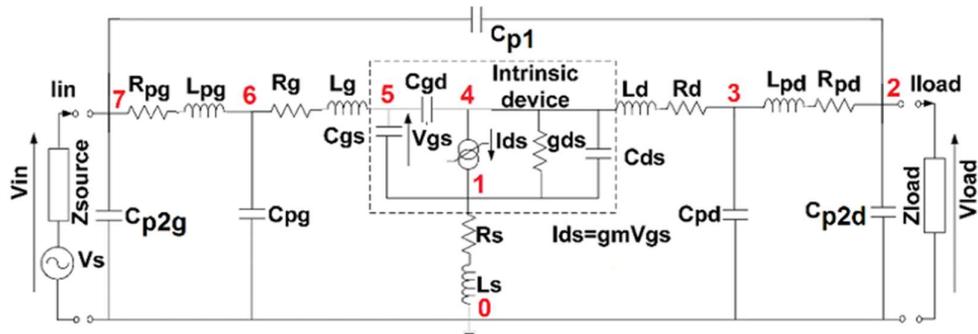


Figure 5.8: Equivalent circuit model for a GaN HEMT including matching impedances.

Equations (5.9) - (5.12) are derived by analyzing the circuit in Figure 5.8.

$$V_{in} = V_{70} = V_{76} + V_{60} = V_{76} + V_{65} + V_{51} + V_{10} \quad (5.9)$$

$$I_{in} = I_{70} + I_{72} + I_{76} \quad (5.10)$$

$$V_{load} = V_{20} = V_{23} + V_{30} \quad (5.11)$$

$$I_{load} = I_{32} + I_{72} + I_{20} \quad (5.12)$$

As in [5.1] – [5.3], the optimum load impedance is obtained by presenting the optimum load line resistance (R_{opt}) to the current generator, which provides the following relationship:

$$V_{41} = -g_m V_{gs} R_{opt} \quad (5.13)$$

Therefore, the input and load voltages and currents in (5.9) - (5.12) can be calculated as following:

$$\begin{aligned} V_{in} = & Z_{pgs} [Y_{Cgd} (V_{gs} + g_m V_{gs} R_{opt}) + Y_{Cgs} V_{gs} + Y_{Cgs} \{Z_g ((Y_{Cgd} (V_{gs} + g_m V_{gs} R_{opt}) + Y_{Cgs} V_{gs})) + V_{gs} + Z_s (Y_{Cgs} V_{gs} \\ & + g_m V_{gs} - g_m V_{gs} g_{ds} R_{opt} - Y_{Cds} g_m V_{gs} R_{opt})\}] + Z_g \{Y_{Cgd} (V_{gs} + g_m V_{gs} R_{opt})\} + Y_{Cgs} V_{gs} + V_{gs} + Z_s (Y_{Cgs} V_{gs} + g_m V_{gs} \\ & - g_m V_{gs} g_{ds} R_{opt} - Y_{Cds} g_m V_{gs} R_{opt}) \end{aligned} \quad (5.14)$$

$$\begin{aligned} I_{in} = & Y_{pgs} (Z_{pgs} [Y_{Cgd} (V_{gs} + g_m V_{gs} R_{opt}) + Y_{Cgs} V_{gs} + Y_{Cgs} \{Z_g ((Y_{Cgd} (V_{gs} + g_m V_{gs} R_{opt}) + Y_{Cgs} V_{gs})) + V_{gs} + Z_s (Y_{Cgs} V_{gs} \\ & + g_m V_{gs} - g_m V_{gs} g_{ds} R_{opt} - Y_{Cds} g_m V_{gs} R_{opt})\}] + Z_g \{Y_{Cgd} (V_{gs} + g_m V_{gs} R_{opt})\} + Y_{Cgs} V_{gs} + V_{gs} + Z_s (Y_{Cgs} V_{gs} + g_m V_{gs} \\ & - g_m V_{gs} g_{ds} R_{opt} - Y_{Cds} g_m V_{gs} R_{opt})) + Y_{pd} [Z_{pgd} \{Y_{Cgd} (V_{gs} + g_m V_{gs} R_{opt}) + Y_{Cgs} V_{gs} + Y_{Cgs} (Z_g (Y_{Cgd} (V_{gs} + g_m V_{gs} R_{opt}) \\ & + V_{gs} + Z_s (Y_{Cgs} V_{gs} + g_m V_{gs} - g_m V_{gs} g_{ds} R_{opt} - Y_{Cds} g_m V_{gs} R_{opt}))\}] + Z_g (Y_{Cgd} (V_{gs} + g_m V_{gs} R_{opt})) + Y_{Cgs} V_{gs} + V_{gs} \\ & + g_m V_{gs} R_{opt} + Z_d (Y_{Cgd} (V_{gs} + g_m V_{gs} R_{opt}) + Y_{Cgs} V_{gs} - g_m V_{gs} + g_m V_{gs} g_{ds} R_{opt} + Y_{Cds} g_m V_{gs} R_{opt}) + Z_{pd} \{Y_{Cgs} (V_{gs} + \\ & g_m V_{gs} R_{opt}) + Y_{Cgs} V_{gs} - g_m V_{gs} + g_m V_{gs} g_{ds} R_{opt} + Y_{Cds} g_m V_{gs} R_{opt} - Y_{Cpd} (Z_s (Y_{Cgs} V_{gs} + g_m V_{gs} - g_m V_{gs} g_{ds} R_{opt} \\ & - Y_{Cds} g_m V_{gs} R_{opt}) - Z_d (Y_{Cgd} (V_{gs} + g_m V_{gs} R_{opt}) + Y_{Cgs} V_{gs}) - g_m V_{gs} + g_m V_{gs} g_{ds} R_{opt} + Y_{Cds} g_m V_{gs} R_{opt} - g_m V_{gs} R_{opt}\}] \\ & + Y_{Cgs} (V_{gs} + g_m V_{gs} R_{opt}) + Y_{Cgs} V_{gs} + Y_{Cpgs} \{Z_g \{Y_{Cgd} (V_{gs} + g_m V_{gs} R_{opt})\} + Y_{Cgs} V_{gs} + V_{gs} + Z_s (Y_{Cgs} V_{gs} + g_m V_{gs} \\ & - g_m V_{gs} g_{ds} R_{opt} - Y_{Cds} g_m V_{gs} R_{opt})\}] \end{aligned} \quad (5.15)$$

$$\begin{aligned} V_{load} = & Z_s (Y_{Cgs} V_{gs} + g_m V_{gs} - g_m V_{gs} g_{ds} R_{opt} - Y_{Cds} g_m V_{gs} R_{opt}) - Z_d \{Y_{Cds} (V_{gs} + g_m V_{gs} R_{opt}) + Y_{Cgs} V_{gs} - g_m V_{gs} \\ & + g_m V_{gs} g_{ds} R_{opt} + Y_{Cds} g_m V_{gs} R_{opt}\} - g_m V_{gs} R_{opt} - Z_{pd} [Y_{Cgd} (V_{gs} + g_m V_{gs} R_{opt}) + Y_{Cgs} V_{gs} - g_m V_{gs} + g_m V_{gs} g_{ds} R_{opt} \\ & + Y_{Cds} g_m V_{gs} R_{opt} - Y_{Cpd} \{Z_s (Y_{Cgs} V_{gs} + g_m V_{gs} - g_m V_{gs} g_{ds} R_{opt} - Y_{Cds} g_m V_{gs} R_{opt}) - Z_d (Y_{Cgd} (V_{gs} + g_m V_{gs} R_{opt}) \\ & + Y_{Cgs} V_{gs} - g_m V_{gs} + g_m V_{gs} g_{ds} R_{opt} + Y_{Cds} g_m V_{gs} R_{opt}) - g_m V_{gs} R_{opt}\}] \end{aligned} \quad (5.16)$$

$$\begin{aligned} I_{load} = & Y_{pd} (Z_s (Y_{Cgs} V_{gs} + g_m V_{gs} - g_m V_{gs} g_{ds} R_{opt} - Y_{Cds} g_m V_{gs} R_{opt}) - Z_d \{Y_{Cds} (V_{gs} + g_m V_{gs} R_{opt}) + Y_{Cgs} V_{gs} - g_m V_{gs} \\ & + g_m V_{gs} g_{ds} R_{opt} + Y_{Cds} g_m V_{gs} R_{opt}\} - g_m V_{gs} R_{opt} - Z_{pd} [Y_{Cgd} (V_{gs} + g_m V_{gs} R_{opt}) + Y_{Cgs} V_{gs} - g_m V_{gs} + g_m V_{gs} g_{ds} R_{opt} \\ & + Y_{Cds} g_m V_{gs} R_{opt} - Y_{Cpd} \{Z_s (Y_{Cgs} V_{gs} + g_m V_{gs} - g_m V_{gs} g_{ds} R_{opt} - Y_{Cds} g_m V_{gs} R_{opt}) - Z_d (Y_{Cgd} (V_{gs} + g_m V_{gs} R_{opt}) \\ & + Y_{Cgs} V_{gs} - g_m V_{gs} + g_m V_{gs} g_{ds} R_{opt} + Y_{Cds} g_m V_{gs} R_{opt}) - g_m V_{gs} R_{opt}\}]) \end{aligned} \quad (5.17)$$

Where: $Y_{Cgs} = j\omega C_{gs}$, $Y_{Cgd} = j\omega C_{gd}$, $Y_{Cds} = j\omega C_{ds}$, $Y_{Cp1} = j\omega C_{p1}$, $Y_{Cp2g} = j\omega C_{p2g}$, $Y_{Cp2d} = j\omega C_{p2d}$, $Y_{Cpg} = j\omega C_{pg}$ and $Y_{Cpd} = j\omega C_{pd}$ respectively and $Z_{pg} = R_{pg} + j\omega L_{pg}$, $Z_{pd} = R_{pd} + j\omega L_{pd}$, $Z_s = R_s + j\omega L_s$, $Z_g = R_g + j\omega L_g$ and $Z_d = R_d + j\omega L_d$.

The values of optimum source and load impedances are obtained by (5.18) and (5.19):

$$Z_{source} = \text{conj} \left(\frac{V_{in}}{I_{in}} \right) \quad (5.18)$$

$$Z_{load} = \frac{V_{load}}{I_{load}} \quad (5.19)$$

The input and output powers are calculated using the following equations:

$$P_{in} = \frac{1}{2} \text{Re}\{V_{in} \times \text{conj}(I_{in})\} \quad (5.20)$$

$$P_{out} = \frac{1}{2} \text{Re}\{V_{load} \times \text{conj}(I_{load})\} \quad (5.21)$$

The power gain is then calculated from the ratio between P_{out} and P_{in} .

Analytic Expressions Without Package Parasitic

Although the RF transistors are commonly available in three-terminal packages; however, in case of most commercial transistors, the package models are not easily available. Therefore, another set of expressions (5.22) - (5.25) are derived without considering the package parasitic in the equivalent circuit model.

$$V_{in} = Z_g \{ Y_{Cgd} (V_{gs} + g_m V_{gs} R_{opt}) \} + Y_{Cgs} V_{gs} + V_{gs} + Z_s \{ Y_{Cgs} V_{gs} + g_m V_{gs} - g_m V_{gs} g_{ds} R_{opt} - Y_{Cds} g_m V_{gs} R_{opt} \} \quad (5.22)$$

$$I_{in} = Y_{Cgd} (V_{gs} + g_m V_{gs} R_{opt}) + Y_{Cgs} V_{gs} + Y_{Cps} [Z_g \{ Y_{Cgd} (V_{gs} + g_m V_{gs} R_{opt}) \} + Y_{Cgs} V_{gs} + V_{gs} + Z_s \{ Y_{Cgs} V_{gs} + g_m V_{gs} - g_m V_{gs} g_{ds} R_{opt} - Y_{Cds} g_m V_{gs} R_{opt} \}] \quad (5.23)$$

$$V_{load} = Z_l \{ -Y_{Cgd} (V_{gs} + g_m V_{gs} R_{opt}) + g_m V_{gs} - g_m V_{gs} g_{ds} R_{opt} - Y_{Cds} g_m V_{gs} R_{opt} \} - g_m V_{gs} R_{opt} \} + Z_s \{ Y_{Cgs} V_{gs} + g_m V_{gs} - g_m V_{gs} g_{ds} R_{opt} - Y_{Cds} g_m V_{gs} R_{opt} \} \quad (5.24)$$

$$I_{load} = Y_{Cgd} (V_{gs} + g_m V_{gs} R_{opt}) - g_m V_{gs} + g_m V_{gs} g_{ds} R_{opt} + Y_{Cds} g_m V_{gs} R_{opt} + Y_{Cpd} [Z_d \{ -Y_{Cgd} (V_{gs} + g_m V_{gs} R_{opt}) + g_m V_{gs} - g_m V_{gs} g_{ds} R_{opt} - Y_{Cds} g_m V_{gs} R_{opt} \} + Z_s \{ Y_{Cgs} V_{gs} + g_m V_{gs} - g_m V_{gs} g_{ds} R_{opt} - Y_{Cds} g_m V_{gs} R_{opt} \}] \quad (5.25)$$

5.3.3 Non-linear case

The device output current (I_{ds}) can be described as:

$$I_{ds} = g_m V_{gs} \quad (5.26)$$

However, in practice, neither is transconductance a constant, nor the drain current has a linear relationship with the input signal at the gate for a real transistor as seen in Figure 5.9 from the measurements of the 25 W GaN-on-SiC HEMT (Cree CGH40025).

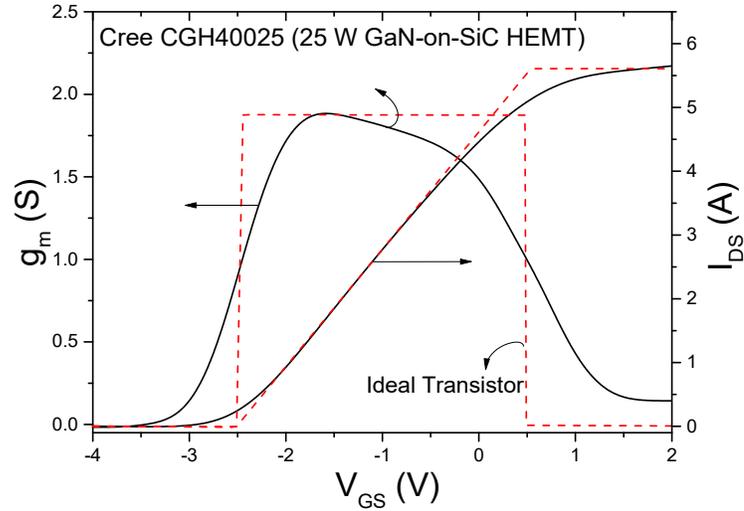


Figure 5.9: Drain-to-source current and transconductance in cases of an ideal transistor and the 25 W GaN-on-SiC HEMT (Cree CGH40025).

Therefore, based on the relationship in (5.26), the expressions in (5.14) - (5.17) and (5.22) – (5.25) are only valid at small-signal. To determine the power gain at large signals, the nonlinear characteristic of the output current needs to be taken into account. Following the method developed by Fioravanti et al. in [5.2], the fundamental component of the current I_{gen} is determined by the Fourier transform of the output current waveform ($I_{gen,wave}$). The output current waveform $I_{gen,wave}$ is defined as:

$$I_{gen,wave} = I_{out} (V_{GSq} + V_{gs}(t)) \quad (5.27)$$

Where I_{out} is the device output characteristic along the load line, V_{GSq} is the gate bias voltage and $V_{gs}(t)$ is the input RF signal at the gate. The term $g_m V_{gs}$ is then replaced by I_{gen} in (5.14) - (5.17) and (5.22) - (5.25).

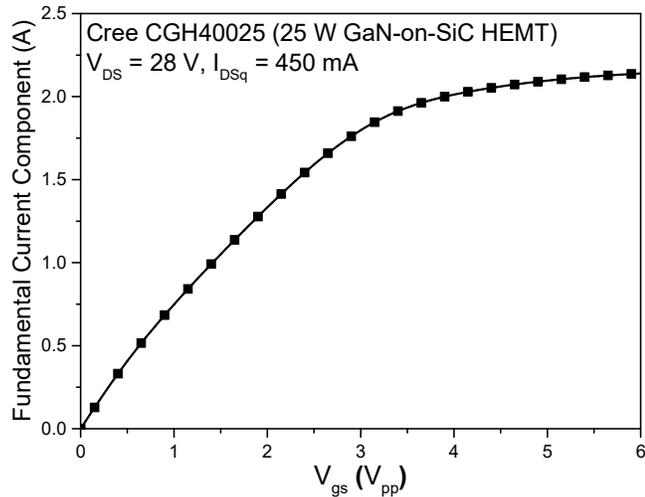


Figure 5.10: Calculated fundamental component of the current generator as a function of input signal.

When the input signal power increases, the value of the current component at the fundamental frequency starts to saturate as shown in Figure 5.10. This allows to predict the device performance at large-signal operation.

5.3.4 Calculating the Efficiency

The DC component of the current can also be determined from the RF current waveform at the load using Fourier analysis as described by Cripps in [5.4]. By following that concept, the DC component (I_{DC}) is determined by using the following equation:

$$I_{DC} = \frac{I_{gen,wave}}{2\pi} \frac{2\sin(\alpha/2) - \cos(\alpha/2)}{1 - \cos(\alpha/2)} \quad (5.28)$$

The DC power is then calculated using (5.29):

$$P_{DC} = V_{DSq} I_{DC} \quad (5.29)$$

The power-added efficiency (PAE) is then calculated by using the following equation:

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \quad (5.30)$$

5.4 Methods of Validation of Analytic Approach

Statistician George Box once said “essentially, all models are wrong, but some are useful” [5.5]. The validity of a model depends on its usefulness within the range of intended application. The validation of any model or technique need to be performed to determine the degree of accuracy with which it depicts the real device in a specified application. From the perspective of a modelling engineer, it helps to establish confidence in measurement, characterisation, extraction and any assumption made during the construction of the model. It can also help to make further necessary improvements of the model. From the perspective of an RFPA designer, the validation gives confidence in the credibility of the model in calculating the optimum impedance values and predicting the performance at a desired condition.

The results obtained from any method depends on the implemented technique; and the inherent limits of the procedure always introduce errors to the solution. The analytic approach uses DC or static load line in the analysis which assumes pure resistive load is presented to the current generator and calculates the optimum impedance values and the small-signal and large-signal RF performances.

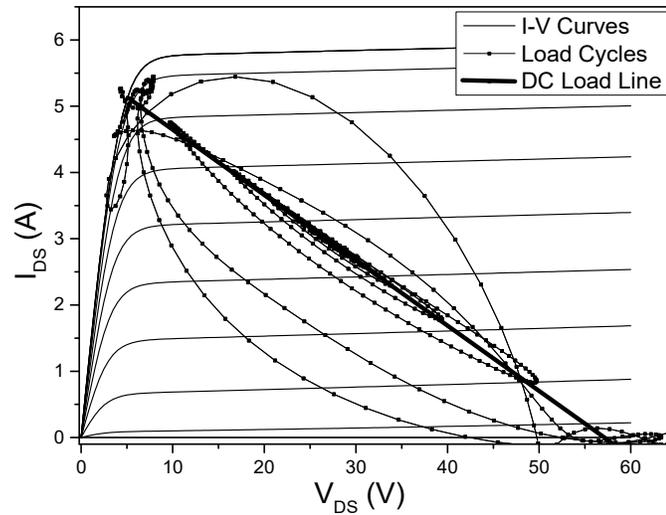


Figure 5.11: DC load line and load cycles of an RFPA as a function of input RF signal when the load and source impedance values are optimized for maximum linearity.

However, for an RF input signal, the drain current and voltage deviate from this ideal load line and a dynamic load line or more precisely, a load cycle is the realistic situation. At small-signal power level, the load cycle is elliptical along the DC load line around the bias or quiescent point of the amplifier. As the input power increases, the dynamic load line deviates more and more from the DC load line. At large-signal, the load cycle starts to clip severely due to the current limitation of the transistor as shown in Figure 5.11. This can affect the accuracy of the analytic approach in predicting the large-signal performance.

The small-signal s-parameters verification of the extracted equivalent circuit models have already been presented in Chapter 4. In this chapter, the accuracy of analytic approach based on the model to obtain the optimum impedance values and to predict the large-signal performance are evaluated via HB simulation and experimental results.

5.4.1 Harmonic Balance Simulation

Harmonic balance simulations in ADS are used as the first benchmark to validate the calculated optimum impedance values and RF performance using the new analytic expressions. The accuracy of the method is evaluated at different bias conditions, at different optimization criteria and frequencies.

In order to perform HB simulations using the equivalent circuit lumped element model, the nonlinear current generator has been modelled using a 2-port symbolically-

defined device (SDD) in ADS as shown in Figure 5.12. The SDD is an equation-based component that allows defining non-linear components such as the current generator by describing the relationship between the gate and drain voltages and the drain current. The measured I_{DS} - V_{GS} extracted along the load line is fitted using a polynomial equation of 11th order.

$$I_{DS} = C_0 + C_1V_{GS} + C_2V_{GS}^2 + \dots + C_{11}V_{GS}^{11} \quad (5.31)$$

The coefficients (C_0, C_1, \dots, C_{11}) can be easily determined using polynomial curve fitting. The range of gate voltages is divided into two regions and corresponding coefficients are applied in order to achieve excellent match between measurement and model. The implementation of this nonlinear current generator model has been done in collaboration with Nagaditiya Poluri.

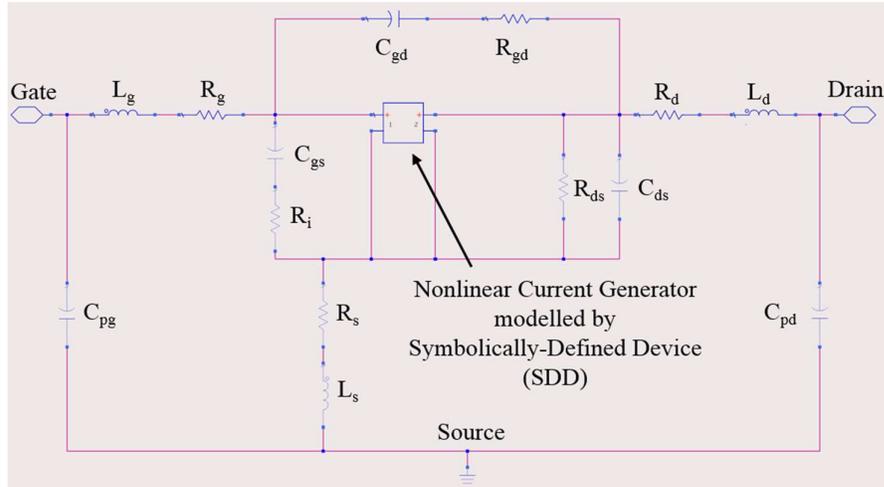


Figure 5.12: Schematic diagram of the large-signal model used in harmonic balance simulation in ADS.

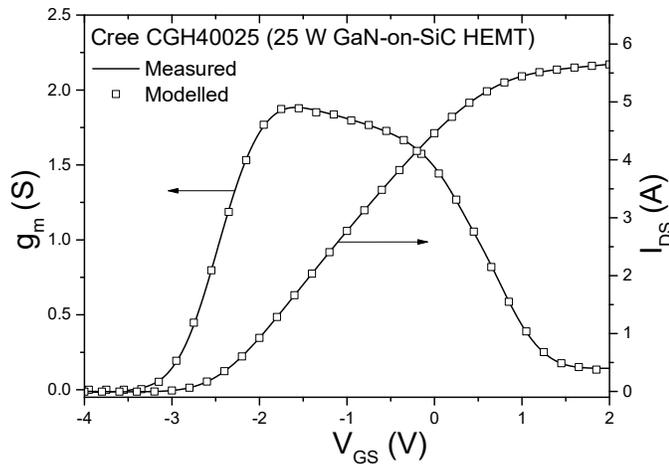


Figure 5.13: I_{DS} - V_{GS} and g_m - V_{GS} curves for Cree CGH40025 obtained from measurement (line) and simulation (symbol) using the model in Figure 5.12.

Figure 5.13 shows the measured and simulated $I_{DS}-V_{GS}$ and g_m-V_{GS} curves for the Cree CGH40025. The optimum load and source impedances are first obtained from HB simulation and analytic approach using the methods described in Sections 5.2.1 and 5.3.2 respectively. In order to evaluate the accuracy of the analytic approach in predicting the RF performance, RF PAs are simulated in ADS and the performance is compared with analytically calculated results using identical values of the extracted parameters and nonlinear current generator in both approaches.

5.4.2 Measurement of Prototype RF Power Amplifiers

As the second benchmark to evaluate the accuracy of analytic approach, experimental results of three prototype RFPAs, designed using the 25 W Cree and Nitronex 25 W GaN HEMT devices, are used. A Class AB power amplifier is designed with the Cree CGH40025, a 25 W GaN-on-SiC HEMT, using the optimum impedance values obtained from the analytical expressions. The 25 W GaN-on-Si based Class-AB RFPAs are designed using two different sets of impedance values: one calculated using the analytic expressions, and the second obtained from HB simulations using the vendor supplied model. The layouts for the input and output matching networks are designed on a Rogers RO4350 hydrocarbon ceramic laminate. The low dielectric loss of 0.0031 and 0.0037 at high frequencies such as 2.5 GHz and 10 GHz respectively makes this material suitable for designing RF PAs at the operating frequency of 3.25 GHz. Figure 5.14 shows two prototype power amplifiers designed using the 25 W Cree and Nitronex GaN HEMTs.

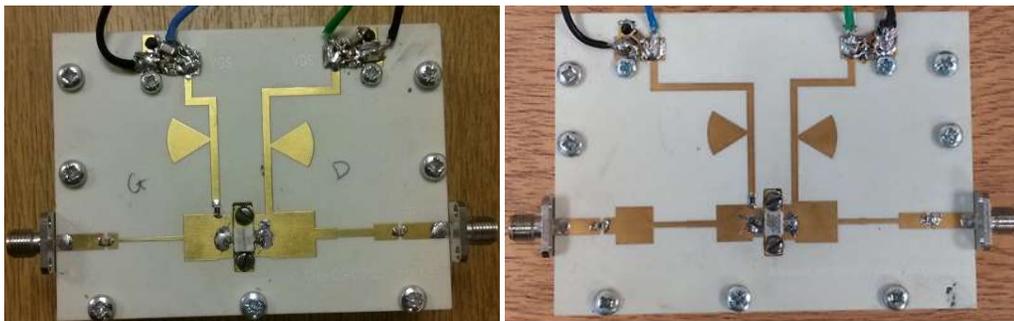


Figure 5.14: Photographs of prototype amplifiers using Cree CGH40025 (left) and Nitronex NPTB00025 (right).

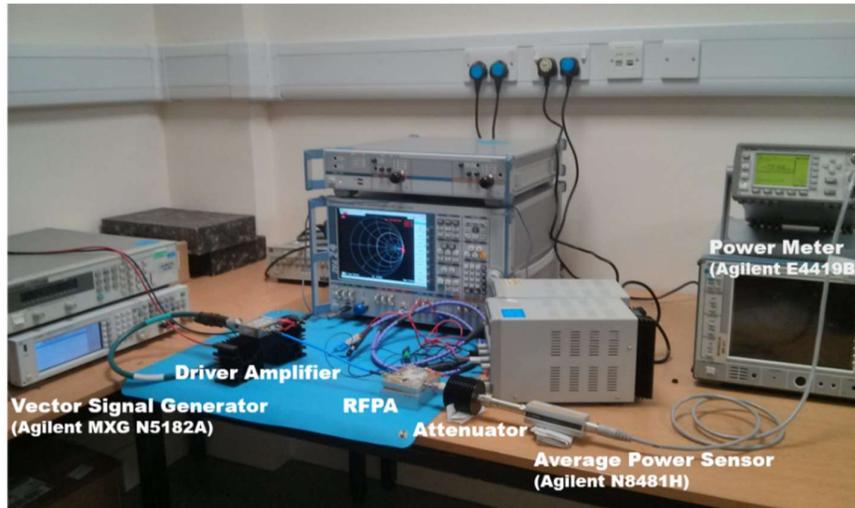


Figure 5.15: The set-up for large-signal measurement of the prototype amplifiers.

Figure 5.15 shows the setup for large-signal measurement of the prototype amplifiers. Since the signal generator can produce a maximum output power of 17 dBm, a driver amplifier is used to push the prototype RFPA into compression to measure the output power at 1-dB gain compression and maximum efficiency. The driver amplifier is HMC1086 from Hittite Microwave Corporation, a 25 W GaN-based PA with a small-signal gain of 22 dB in the frequency range of 2 – 3.5 GHz. The output from the RFPA is reduced with a 30 dB attenuator before measuring with the power sensor and power meter to protect the instruments.

5.5 Validation of Analytic Approach via HB Simulation

5.5.1 At Different Bias Points

The verification of the analytic approach is carried out to evaluate its accuracy by comparing the calculated results from analytical approach with the HB simulation in ADS for the Cree CGH40025 at different biases varying from mid Class-AB ($I_{DSq} = 450$ mA) to deep Class-AB (90 mA). The $I_{DS}-V_{GS}$ characteristic is extracted along the load line for each bias points from the $I_{DS}-V_{DS}$ characteristics. A small step size of 0.1 V for the gate voltage is used to obtain the output characteristics as accurately as possible near the threshold voltage where very small currents are involved.

Figure 5.16 shows the delivered power contours from the load-pull and source-pull simulations in ADS and a comparison of analytically calculated and simulated optimum impedance values for maximum P1dB for the Cree CGH40025 as the quiescent bias current is changed from 90 mA to 450 mA.

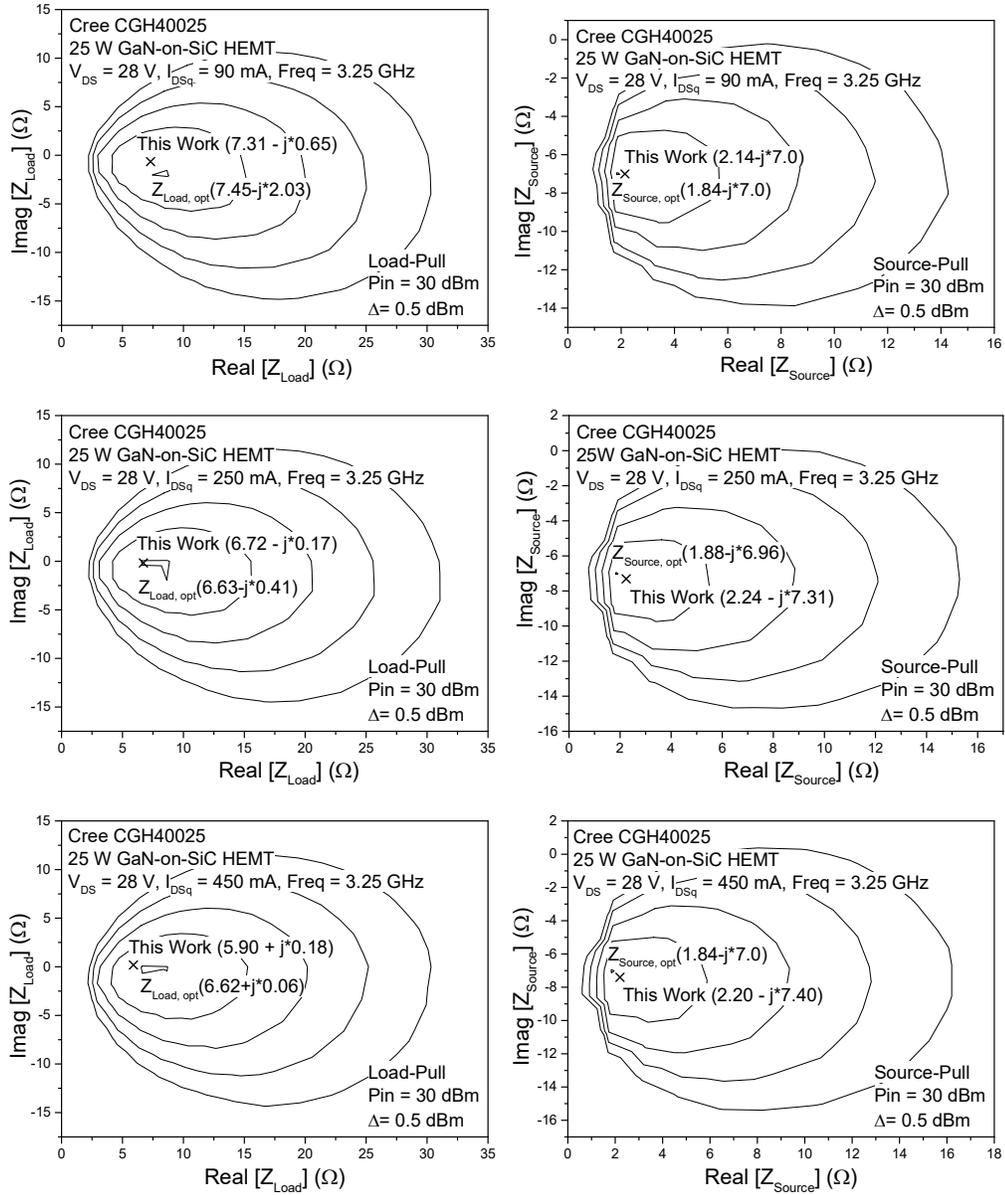


Figure 5.16: Delivered power contours from the load-pull and source-pull simulations in ADS and comparison of analytically calculated and simulated optimum impedance values for maximum P_{1dB} for the Cree CGH40025 at $V_{DS} = 28$ V and $I_{DSq} = 90$ mA, 250 mA and 450 mA.

Figure 5.16 shows that the optimum impedance values calculated using the analytic expressions in all three bias points are on contours which are less than 0.5 dBm lower than the maximum delivered output. It can be seen that the analytic expressions allow to calculate optimum impedance values with good precision.

In order to evaluate the accuracy of analytic approach in predicting the RF performance, RF PAs are simulated in ADS and the performance is compared with analytically calculated results. The values of impedances and RF performance are summarised in Figure 5.17 and Table 5.1.

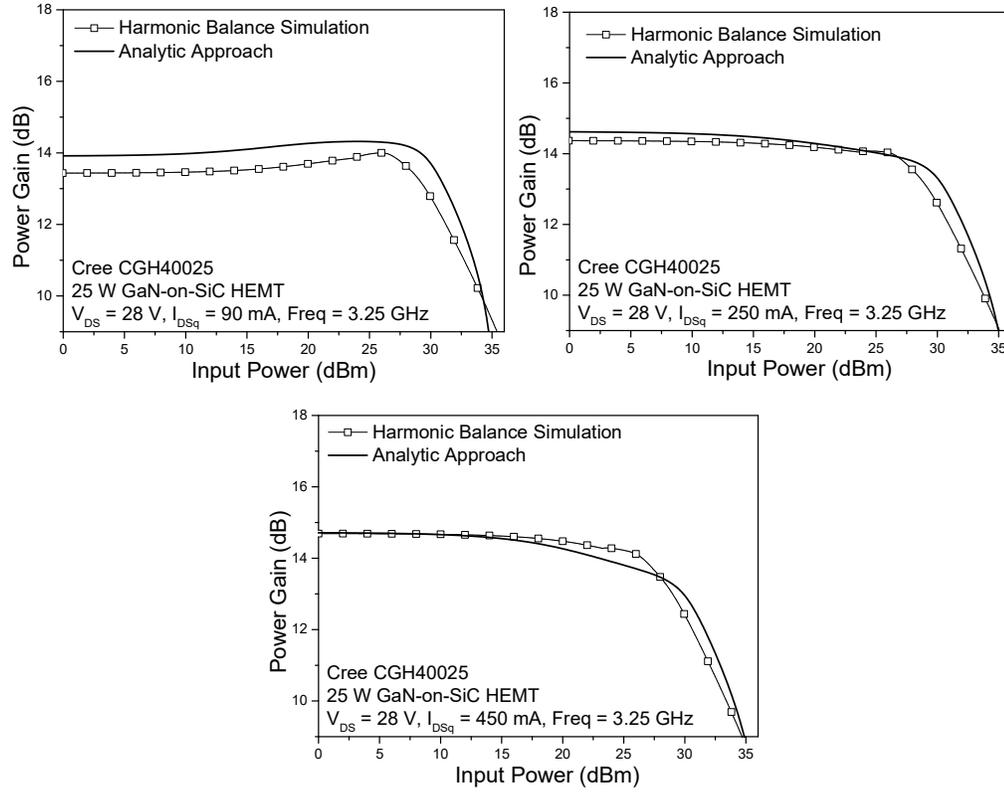


Figure 5.17: Comparison of simulated and calculated power gain and output power versus input power using (5.22) – (5.25) for Cree CGH40025 at $V_{DS} = 28$ V, Frequency = 3.25 GHz and at different bias points of $I_{DSq} = 90$ mA, 250 mA and 450 mA when source and load impedances are optimized for maximum linearity.

Table 5.1 Comparison of analytically calculated and HB simulated impedance values and RF performance of Cree CGH40025 at $V_{DS} = 28$ V, Frequency = 3.25 GHz and at different bias points of $I_{DSq} = 90$ mA, 250 mA and 450 mA.

	HB Simulation	Analytic Approach
90 mA		
Z_{source} (Ω)	$1.84 - j*7.0$	$2.14 - j*7.00$
Z_{load} (Ω)	$7.45 - j*2.03$	$7.31 - j*0.65$
Gain (dB)	13.44	13.92
P1dB (dBm)	43.05	44.22
PAE (%)	49.61	46.91
250 mA		
Z_{source} (Ω)	$1.88 - j*6.96$	$2.24 - j*7.31$
Z_{load} (Ω)	$6.63 - j*0.41$	$6.72 - j*0.17$
Gain (dB)	14.37	14.63
P1dB (dBm)	41.82	42.57
PAE (%)	48.02	44.04
450 mA		
Z_{source} (Ω)	$1.84 - j*7.0$	$2.20 - j*7.40$
Z_{load} (Ω)	$6.62 + j*0.06$	$5.90 + j*0.18$
Gain (dB)	14.69	14.72
P1dB (dBm)	41.09	41.23
PAE (%)	45.90	40.52

The results show that the maximum errors for analytic approach in predicting the power gain and P1dB compared to the results from HB approach using identical parameters (as opposed to the predictions from the vendor model) are 3.5%, 1.81%, 0.20% and 2.7%, 1.79%, 0.34% respectively for 90 mA, 250 mA and 450 mA. The accuracy at 90 mA in predicting the power gain and P1dB is lower than 250 mA and 450 mA. The maximum error in the calculated power-added-efficiency is 5.44%, 8.29% and 11.72% respectively for 90 mA, 250 mA and 450 mA.

The results show that analytic approach can accurately calculate the optimum impedance values for all bias conditions. However, the prediction of RF performance shows higher percentage of error as the gate bias voltage moves towards the threshold voltage. In most cases, the large-signal model provided by the vendors shows higher percentage of error between simulation and measurement, especially for power gain and efficiency. Therefore, considering the value of maximum error in prediction, it can be said that the analytical expression can yield reasonably accurate prediction of performance from Class-AB to deep Class-AB.

5.5.2 For Different Optimization Criteria

In this section, the validity of analytic approach to calculate the optimum impedance values and RF performance at different criteria of maximum gain, maximum linearity and maximum efficiency are evaluated. The results are calculated analytically using the method presented in Section 5.3. Figure 5.18 shows the analytically calculated power gain, output power at 1-dB compression point (P1dB) and PAE as functions of load resistance for the MRFE6VS25, a 25 W Si LDMOS from Freescale.

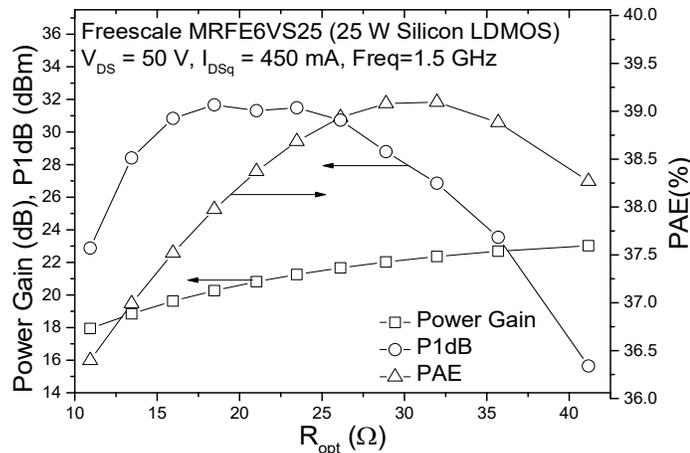


Figure 5.18: Analytically calculated power gain, P1dB and PAE as functions of load resistance for the Si LDMOS at $V_{DS} = 50 \text{ V}$, $I_{DSq} = 450 \text{ mA}$ and Frequency = 1.5 GHz.

It can be noted that the maximum value in each case can be obtained for one particular value of load resistance. By using the corresponding value of R_{opt} in (5.22-5.25), the optimum load and source impedance values for each criteria and RF performance (Figure 5.19) are calculated. The optimum impedance values from load-pull and source-pull simulations and RF performance are also obtained in HB simulation using the large-signal model provided by the vendor. The results are summarised in Table 5.2.

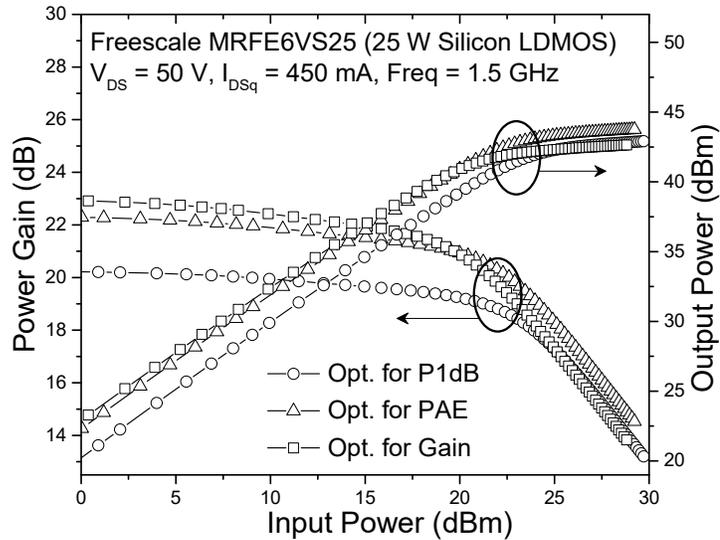


Figure 5.19: Analytically calculated RF performances for the criteria of maximum power gain, maximum linearity and maximum efficiency for the Si LDMOS at $V_{DS} = 50$ V, $I_{DSq} = 450$ mA and Frequency = 1.5 GHz.

Table 5.2 Calculated and HB simulated power gain, P1dB, PAE and optimum source and load impedance values for 25 W Si LDMOS (Freescale MRFE6VS25)

	Optimized for Gain (dB)	Optimized for P1dB (dBm)	Optimized for PAE (%)	Variation from maximum to minimum value (%)
Analytic Approach				
R_{opt} (Ω)	41.17	18.47	30.35	
Z_{source} (Ω)	0.54+j*5.74	1.02+j*4.58	0.72+j*5.30	
Z_{load} (Ω)	0.59+j*6.82	2.18+j*5.62	1.03+j*6.59	
Gain (dB)	23.74	20.71	22.74	12.76
P1dB (dBm)	35.67	38.86	37.97	8.21
PAE (%)	26.54	24.64	31.47	15.67
HB Simulation (Vendor Model)				
Z_{source} (Ω)	0.25+j*1.62	0.25+j*1.62	0.25+j*1.80	
Z_{load} (Ω)	1.87+j*5.22	2.00+j*4.51	1.89+j*3.47	
Gain (dB)	27.11	25.40	23.17	14.53
P1dB (dBm)	43.50	44.65	44.11	2.58
PAE (%)	51.17	59.20	61.56	16.88

Figure 5.20 shows the analytically calculated RF performance for Nitronex NPTB00025, the 25 W GaN-on-Si HEMT, for the three different criteria of maximum gain, maximum linearity and maximum PAE. The optimum impedance values and RF performance at different criteria are also obtained from HB simulations. The results are summarised in Table 5.3.

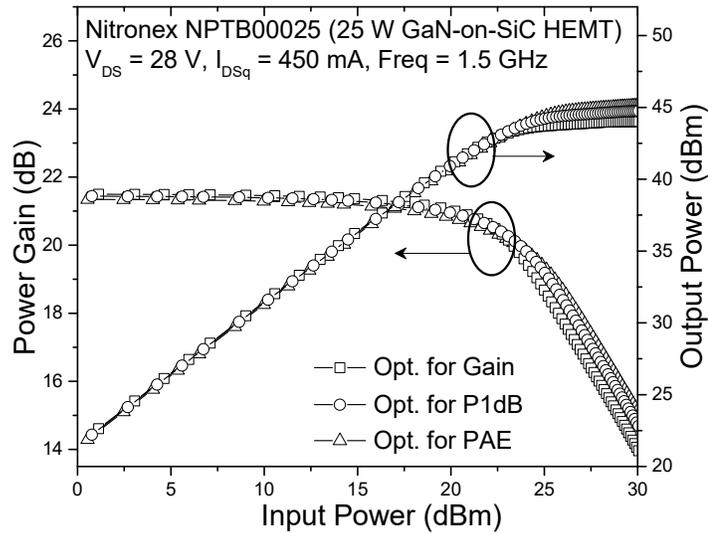


Figure 5.20: Analytically calculated RF performances for the criteria of maximum power gain, maximum linearity and maximum efficiency for the GaN-on-Si HEMT at $V_{DS} = 28 \text{ V}$, $I_{DSq} = 450 \text{ mA}$ and Frequency = 1.5 GHz.

Table 5.3 Calculated and HB simulated power gain, P1dB, PAE and optimum source and load impedance values for 25 W GaN-on-Si HEMT (Nitronex NPTB00025)

	Optimized for Gain (dB)	Optimized for P1dB (dBm)	Optimized for PAE (%)	Variation from maximum to minimum value (%)
Analytic Approach				
$R_{opt} (\Omega)$	28.17	24.17	23.00	
$Z_{source} (\Omega)$	1.85-j*1.02	2.12-j*0.83	2.21-j*0.78	
$Z_{load} (\Omega)$	10.6+j*15.3	12.0+j*12.6	12.3+j*11.6	
Gain (dB)	19.14	19.11	19.09	0.26
P1dB (dBm)	42.14	42.75	42.69	1.42
PAE (%)	51.78	55.45	55.74	7.10
HB Simulation (Vendor Model)				
$Z_{source} (\Omega)$	2.10-j*1.88	2.10-j*1.87	2.10-j*1.87	
$Z_{load} (\Omega)$	10.42+j*5.36	9.82+j*2.47	9.70+j*4.67	
Gain (dB)	21.99	21.35	21.91	2.9
P1dB (dBm)	40.75	41.45	41.04	1.69
PAE (%)	68.25	67.36	68.97	1.04

The value of load resistance for which the maximum value for a given criterion can be achieved is highlighted in bold in Tables 5.2 and 5.3.

It can be seen that for the Si LDMOS the power gain, linearity and PAE are much higher when the impedance values are optimized for that particular criterion. The Si LDMOS also shows better small signal gain at lower frequencies, due to its lower feedback capacitance, source inductance, output conductance and higher optimum load resistance. In comparison, the response from GaN HEMT to optimization is minimal. This behaviour has also been observed in HB simulation using corresponding large-signal model from the vendor as depicted in Table 5.3. The unique advantage of the analytical approach reveals that the response is due to the close value of the optimum load resistance (R_{opt}) in case of the GaN HEMT, especially for P1dB and PAE which are 24.17Ω and 23Ω respectively. On the other hand, a strong contrast in the load resistance values for different conditions in Si LDMOS explains the well optimized RF performance in this case.

Furthermore, contrary to the load line theory which states that the device efficiency increases with increasing load resistance; the maximum PAE is observed at a lower value of load resistance for the GaN HEMT. In order to investigate these peculiarities, the RF performance of the GaN-on-Si HEMT is analytically calculated again where the value of each parameter in (5.22) – (5.25) is replaced one at a time by the corresponding value from Si LDMOS to observe its effect.

Table 5.4. Influence of parameters on the optimisation

Parameters	Variation from maximum to minimum (%)		
	PG	P1Db	PAE
Initial Value	0.26	1.42	7.10
C_{pg}, C_{pd}, L_d, L_g	0.26	1.38	7.08
L_s	0.17	0.65	2.39
R_s	0.71	1.49	7.02
R_d	0.17	0.53	4.49
R_g	0.17	0.55	2.76
C_{gd}	4.18	3.02	14.4
C_{ds}	0.39	0.60	2.91
C_{gs}	0.62	1.35	7.93
g_{ds}	2.06	2.27	3.36

It can be observed from Table 5.4 that among all the parameters that affect the RF performance, the higher values of feedback capacitance (C_{gd}) and output conductance (g_{ds}) in GaN HEMT are mostly responsible for the immunity of GaN HEMT to optimization.

As discussed in Chapter 4, the value of feedback capacitance C_{gd} is higher in GaN HEMT compared to Si LDMOS. Higher value of feedback capacitance reduces the

power gain and consequently influences the efficiency since $PAE = \text{drain efficiency} \times (1 - 1/\text{Gain})$.

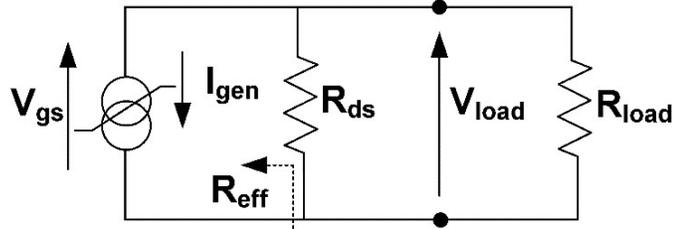


Figure 5.21: Effective resistance presented to the device output.

The output conductance (g_{ds}) is the reciprocal of the drain-to-source on-resistance (R_{ds}) as seen in Figure 5.21. GaN HEMT devices have high electron mobility in 2DEG and consequently a smaller on-resistance that results in a higher output conductance compared to Si LDMOS. This smaller value of R_{ds} , however, acts in parallel to the load resistance to reduce the effective resistance presented to the current generator of the device. Hence this causes reduction in power gain and efficiency and results in a minimal response to optimization.

5.5.3 At High Frequency

In this section, the validity of the analytic approach at a high frequency of 7.5 GHz is demonstrated using the MGF0843G, a 20 W GaN HEMT from Mitsubishi. The available large-signal model from Mitsubishi shows large mismatch between the simulated and measured S-parameters as shown in Section 4.6.5. The RF performance obtained from HB simulation using the vendor model also displays large error as shown in Figure 5.22. Therefore, a new model has been proposed for this device.

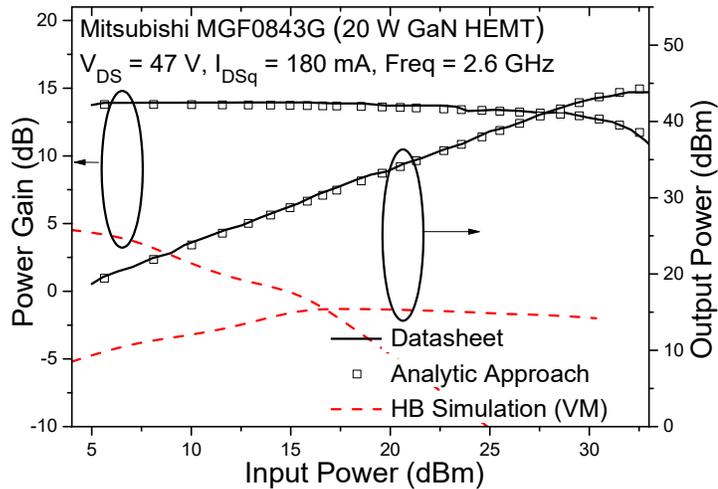


Figure 5.22: Analytically calculated RF performance for the 20 W GaN-on-SiC HEMT at 2.6 GHz and $V_{DS} = 47 \text{ V}$, $I_{DSq} = 180 \text{ mA}$.

In Figure 5.22, the good match between analytically calculated results with the measured results provided in the datasheet ensure the accuracy of the extracted model at 2.6 GHz. To validate the model and analytically calculated results at the frequency of 7.5 GHz, harmonic balance simulation results using ADS are used as benchmark.

Figure 5.23 shows the load-pull and source-pull contours obtained from ADS simulations using the large-signal modelling technique described in Section 5.4.1. The calculated optimum impedance values using the analytic expressions are also shown. The values of optimum impedances are summarised in Table 5.5.

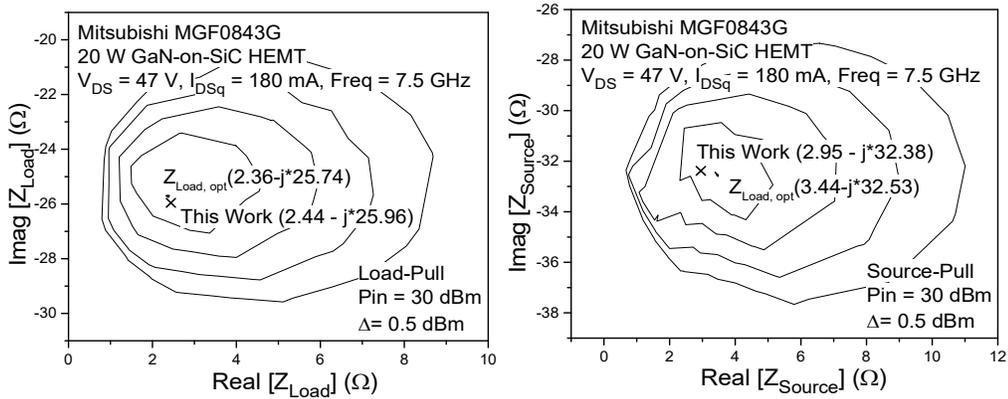


Figure 5.23: Comparison of simulated and calculated optimum impedance values for Mitsubishi MGF0843G at $V_{DS} = 47$ V, $I_{DSq} = 180$ mA and Frequency = 7.5 GHz.

The impedance values from analytic approach correspond to powers within 0.5 dB of the maximum deliverable power determined by the source/load-pull simulations. One can observe that the analytic expressions allow to determine the optimum impedances with good accuracy even at a high frequency of 7.5 GHz. A Class AB linear amplifier is simulated in ADS using these impedance values to design the matching networks.

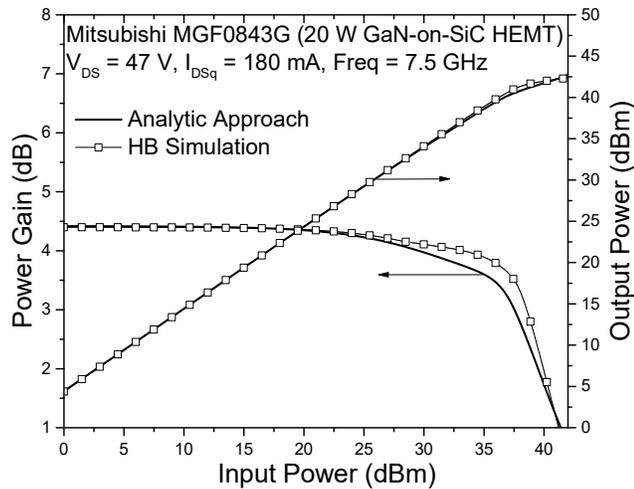


Figure 5.24: Comparison of simulated and calculated power gain and output power versus input power for Mitsubishi MGF0843G at $V_{DS} = 47$ V, $I_{DSq} = 180$ mA and Frequency = 7.5 GHz.

Table 5.5 Simulated and analytically calculated optimum source and load impedances and RF performance of Mitsubishi MGF0843G at $V_{DS} = 47$ V, $I_{DSq} = 180$ mA and Frequency = 7.5 GHz

	Source/Load-Pull Simulations	Analytic Expression
Z_{source} (Ω)	3.44-j*32.53	2.95-j*32.38
Z_{load} (Ω)	2.36-j*25.74	2.44-j*25.96
Power Gain (dB)	4.39	4.42
P1dB (dBm)	41.23	39.64
PAE (%)	18.62	15.91

The good agreement between the simulated and calculated power gain can be noted. This confirms that the analytic approach can be implemented at higher frequencies to design power amplifiers.

5.6 Effects of Package Parasitic

At high frequency, the parasitic and heat transfer properties of the package can have significant impact on the device RF performance. Therefore, it is important to understand the effects of the package. In case of most commercial transistors, the package models are not easily available, and in such situation, it is assumed that the package parasitic effects are included in the extracted values of the rest of the parameters. The error introduced by the assumption has to be evaluated to gain confidence in analytic approach. The analysis of temperature effect of the package on the internal temperature and performance of the device is a complex issue and usually performed in three-dimensional finite element analysis. The effects of the parasitic elements of the package are studied here. As the package model for Cree CGH40010, a 10 W GaN-on-SiC HEMT, is available from the manufacturer, the optimum impedance values and RF performance of this device are calculated with and without considering the package parasitic separately. The parameter values have already been presented in Chapter 4. The influence of each parasitic elements of the package is also studied. The methodology of this analysis is to start with the die and then recalculating the source and load impedance values and the RF performance by gradually modifying the value of one package parasitic element at a time. This helps to attribute any change to that specific parameter alone.

The optimum impedance values and RF performance for the 10 W GaN-on-SiC HEMT (Cree CGH40010) are calculated using the new expressions (5.14) - (5.17). The results are shown in Figure 5.25 and summarized in Table 5.6.

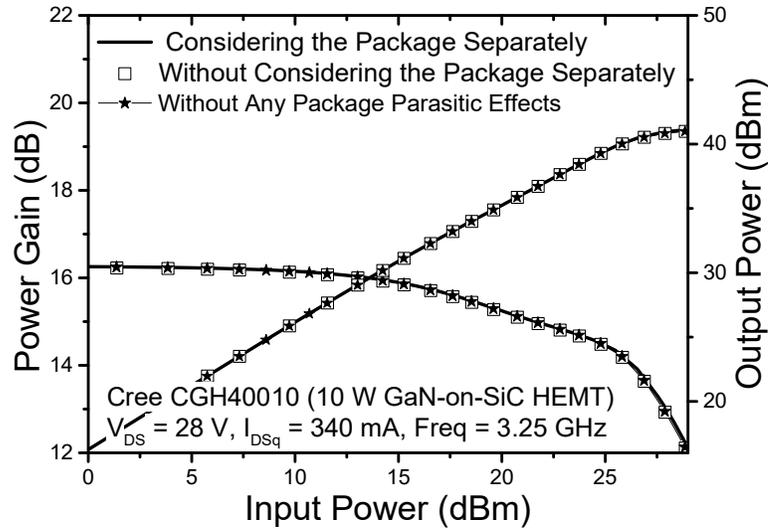


Figure 5.25: Analytically calculated RF performance for the 10 W GaN-on-SiC HEMT at 3.25 GHz and $V_{DS} = 28$ V, $I_{DSq} = 340$ mA.

Table 5.6 Analytically calculated power gain, P1dB, PAE and optimum source and load impedance for the 10 W GaN-on-SiC HEMT (Cree CGH40010) at $V_{DS} = 28$ V, $I_{DSq} = 340$ mA, Frequency = 3.25 GHz

	Without any package parasitic effects (only die)	Considering the package separately.	Without considering the package separately
Z_{source} (Ω)	$2.69+j*3.67$	$3.10-j*8.06$	$2.52-j*8.56$
Z_{load} (Ω)	$7.56+j*15.61$	$7.00+j*4.65$	$7.10+j*3.43$
Gain (dB)	16.27	16.27	16.46
P1dB (dBm)	34.68	34.68	34.90
PAE (%)	37.73	37.66	39.26

The calculated impedance values and predicted RF performance with and without considering package parasitic separately are very close. This can be attributed to the fact that when the package is not considered separately in the small-signal equivalent circuit, the extracted extrinsic parameter values also include these parasitic, though de-embedding helps delineate these contributions specifically. Table 5.6 also shows the calculated optimum impedance values and RF performance of the device die without any package parasitic. The impact of package parasitic on the impedance values and RF performance are studied in the following section with the analytic approach.

The values marked by the solid symbols are the corresponding values for the package parasitic for the Cree CGH40010.

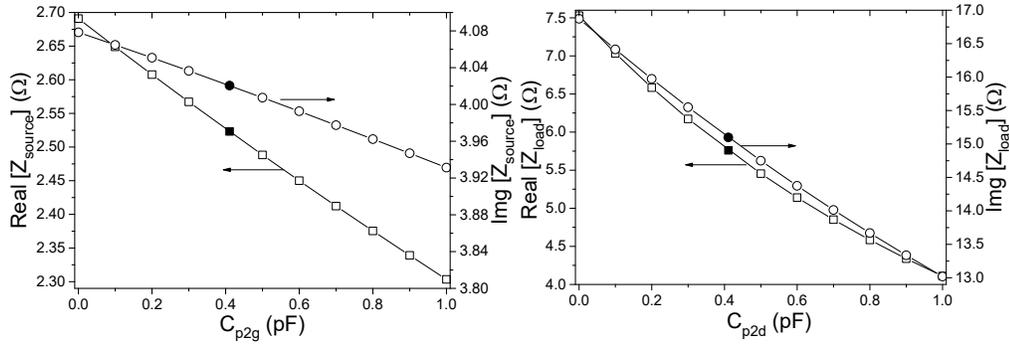


Figure 5.26: Effects of package parasitic capacitance on the source (left) and load (right) impedance values for the 10 W GaN-on-SiC HEMT at 3.25 GHz and $V_{DS} = 28$ V, $I_{DSq} = 340$ mA. The values marked by the solid symbols are the corresponding values of the package parasitic for the Cree CGH40010.

Figure 5.26 shows the impact of the shunt capacitance introduced by the package parasitic on the source and load impedance values. The results show that due to package parasitic capacitance both the source and load impedances come down compared to the unpackaged die. Therefore, although the parasitic capacitance does not have any detrimental effect of the device performance, higher values of C_{p2g} and C_{p2d} can make designing the matching networks difficult as the impedances are reduced.

Figure 5.27 shows the impact of the inductance introduced by the package parasitic on the source and load impedance values. The results show that the parasitic inductances at the gate and the drain due to package parasitic do not affect the real part of the impedance values. The reactive part of both the source and load impedances changes quite significantly with the increasing parasitic inductance values.

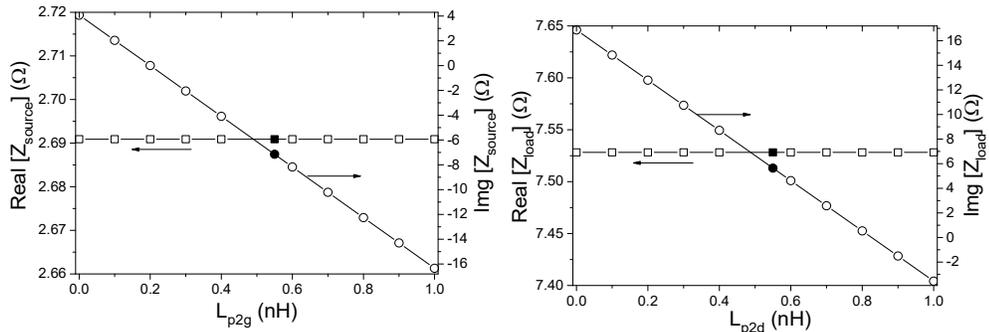


Figure 5.27: Effects of package parasitic inductance on the source (left) and load (right) impedance values for the 10 W GaN-on-SiC HEMT at 3.25 GHz and $V_{DS} = 28$ V, $I_{DSq} = 340$ mA.

The impact of the parasitic resistance introduced by the package on the source and load impedance values can be seen in Figure 5.28. The results show that the parasitic resistances at the gate and the drain have no effect on the imaginary part of the

impedance values. However, these resistances affect the real part of the source and load impedance values differently. While the real part of source impedance increases, the load impedance decreases with increasing value of the parasitic resistance.

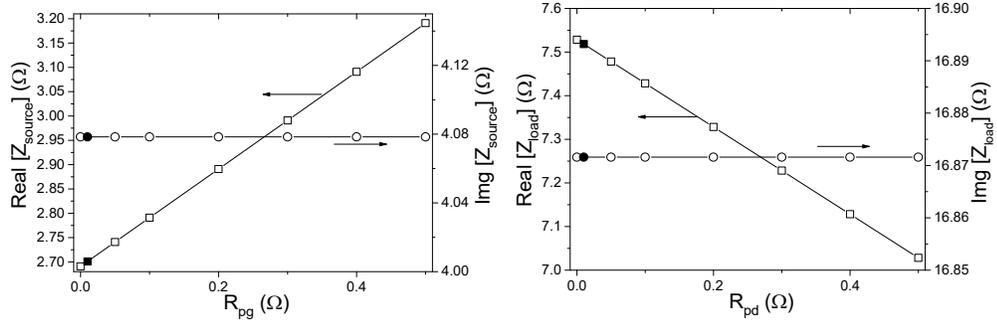


Figure 5.28: Effects of package parasitic resistance on the source (left) and load (right) impedance values for the 10 W GaN-on-SiC HEMT at 3.25 GHz and $V_{DS} = 28$ V, $I_{DSq} = 340$ mA.

Any resistance introduced by the package would cause loss and have detrimental effect on the device RF performance. When the resistance values in the package model are increased, the reduction in power gain, P1dB and PAE can be observed in Figure 5.29.

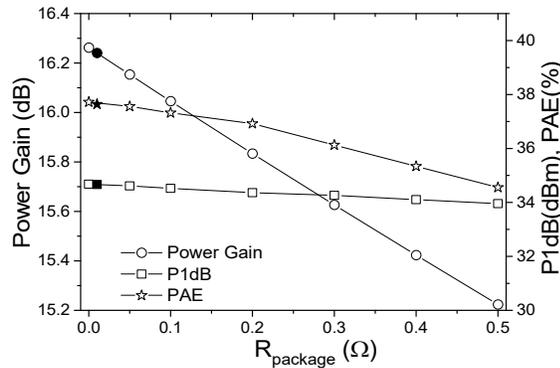


Figure 5.29: Effects of package parasitic resistance on the RF performance of the 10 W GaN-on-SiC HEMT at 3.25 GHz and $V_{DS} = 28$ V, $I_{DSq} = 340$ mA.

The package also introduces capacitance C_{p1} as a parasitic feedback capacitance between the drain and the gate. Its impact on the source and load impedance values can be seen in Figure 5.30.

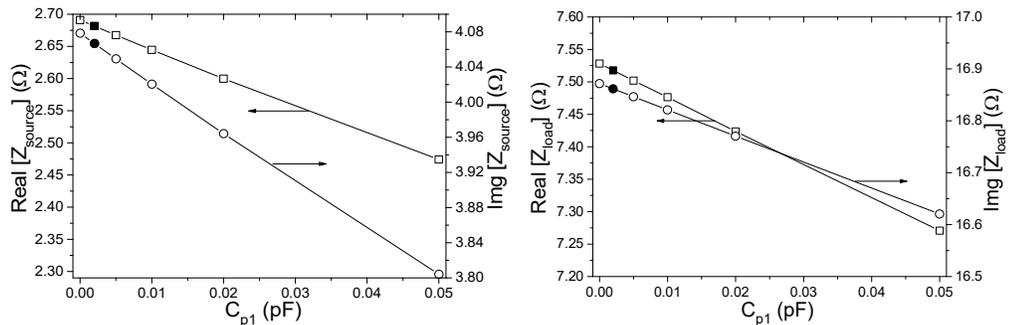


Figure 5.30: Effects of package parasitic feedback capacitance on the source (left) and load (right) impedance values for the 10 W GaN-on-SiC HEMT at 3.25 GHz and $V_{DS} = 28$ V, $I_{DSq} = 340$ mA.

It can be noted that the parasitic capacitance has stronger influence on the source impedance than the load impedance. Figure 5.31 shows the effect of the parasitic capacitance C_{p1} in the RF performance of the device. As the value of C_{p1} increases, the power gain of the device decreases due to higher feedback capacitance.

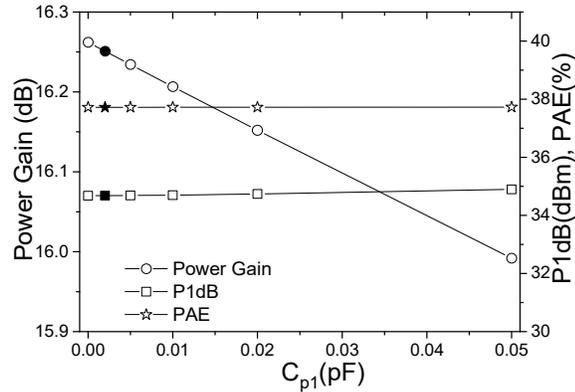


Figure 5.31: Effects of package parasitic feedback capacitance on the RF performance of the 10 W GaN-on-SiC HEMT at 3.25 GHz and $V_{DS} = 28$ V, $I_{DSq} = 340$ mA.

Therefore, when a die is considered for packaging, the goal should be to keep the values of the parasitic elements which have detrimental effect on the device performance at their minimum. The results show that package induced parasitic elements such as C_{p1} and $R_{package}$ can significantly reduce device performance and therefore, their values should be as low as possible. The package for Cree CGH40010 has low values for the parameters C_{p1} and $R_{package}$ (0.002 pF and 0.01 respectively) and does not introduce any source inductance. As a result, the package has minimal effect on the device RF performance before and after packaging. Higher values of parameters such as C_{p2g} and C_{p2d} can change the source and load impedances to lower values and make designing the matching network difficult and therefore, their values should be low as well.

It can be concluded that the new expressions allow to evaluate the RF performance of a device die in a package if the package and device models are available. This can be especially useful to predict the performance of the same active device in packages with different size or mounting technology as sometimes an alternative package is necessary due to application requirements. Since the device would exhibit different impedance values and performance as results of the additional parasitic effects introduced by the use of a different package, the new analytical expressions can be utilized for the optimization of devices packages. The results also ensure that for commercially available packaged RF transistors where the package model is not

always available; the simpler expressions, without considering the package parasitic effects separately, are sufficiently adequate to calculate the optimum impedances and to predict the device performance using the analytic approach.

5.7 Validation of Analytic Approach via Measurement and Comparison with Vendor Model

The power gain and output power against input power obtained from analytical calculation, HB simulation using the vendor model and our model and experimental measurements for the Cree CGH40025, a 25 W GaN-on-SiC, are presented in Figure 5.32 and Table 5.7.

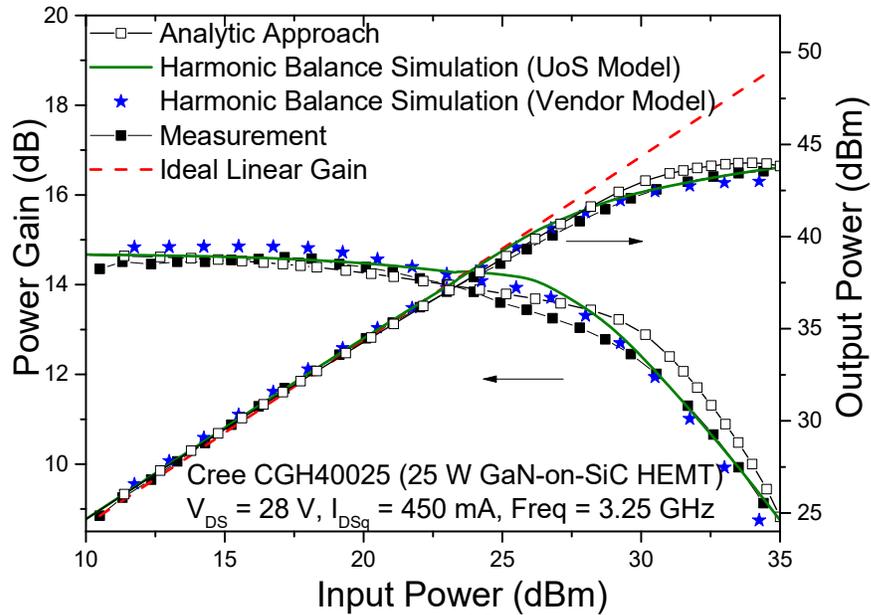


Figure 5.32: Comparison of analytically calculated, measured and simulated (using vendor model in ADS) power gain and output power versus input power for Cree CGH40025 at $V_{DS} = 28$ V, $I_{DSq} = 450$ mA and Frequency = 3.25 GHz.

Table 5.7 Analytically calculated, simulated (internal model and vendor model) and measured power gain, P1dB, PAE and optimum source and load impedance for Cree CGH40025, a 25 W GaN-on-SiC HEMT at $V_{DS} = 28$ V, $I_{DSq} = 450$ mA, Frequency = 3.25 GHz

Method	Z_{source}	Z_{load}	Gain (dB)	P1dB (dBm)	PAE (%)
Analytic Approach (measured I-V)	$2.20-j*7.40$	$5.90+j*0.18$	14.72	41.23	40.52
Harmonic Balance Simulation (Vendor Model)	$1.85-j*7.00$	$5.47+j*1.39$	14.81	40.07	50.20
Harmonic Balance Simulation (Large-signal model by our group)	$1.84-j*7.0$	$6.62+j*0.06$	14.69	41.09	45.09
Measurement	-	-	14.51	39.70	68.04

It can be seen from Table 5.7 that the obtained impedance values in all three cases show good agreement. Figure 5.32 shows that the calculated and simulated power gain are in good agreement with the measurement with a maximum of 2% error. As it can be seen from Table 5.7, the output power in 1-dB gain compression point is overestimated by 1.53 dBm and 1.39 dBm in analytic approach and our internal large-signal model respectively with 3.71% and 3.38% errors in prediction compared to 0.37 dBm in HB simulation using large-signal model provided by the vendor from the measured results. The harmonic balance simulated results using the vendor model, which takes both trapping and self-heating into account, shows good match with the experimental results with just 0.92% error in prediction. The measured power gain starts to show compression at lower input power. This phenomenon is called the “soft-gain compression” and it severely affects the linearity of the GaN HEMT based RF PAs.

The performance of Nitronex NPTB0025, the 25 W GaN-on-Si HEMT based amplifiers prototyped using the vendor model and the analytic approach are compared in Figure 5.33 and Table 5.8. The results demonstrate the validity and accuracy of the analytic approach in absence of a good large-signal model from the vendor.

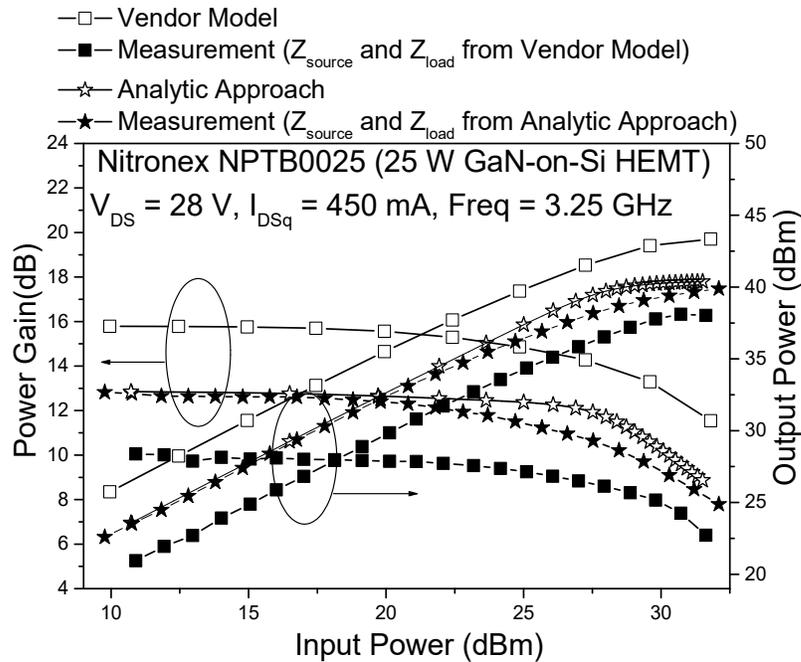


Figure 5.33: Comparison of performance of RF PAs designed using the vendor model in HB simulation versus analytic approach using the extraction in Chapter 4 at 3.25 GHz and 450mA for the 25 W GaN-on-Si HEMT.

Table 5.8 Analytically calculated, vendor model simulated and measured power gain, P1dB, PAE and optimum source and load impedance for the 25 W GaN-on-Si HEMT (Nitronex NPTB00025) at $V_{DSq} = 28$ V, $I_{DSq} = 450$ mA, Frequency = 3.25 GHz

	Analytic Approach (AA)	Vendor Model (VM)	Measured (Analytic Approach)	Measured (Vendor Model)	% of error in prediction (AA/VM)
$Z_{source}(\Omega)$	2.51-j*7.79	1.91-j*11.55	-	-	-
$Z_{load}(\Omega)$	3.77- j*0.54	9.71-j*4.51	-	-	-
Gain(dB)	12.89	15.79	12.54	10.42	-2.71/-34.01
P1dB(dBm)	39.51	40.02	36.27	34.91	-8.20/-12.77
PAE (%)	31.10	56.28	34.37	25.83	+10.51/-54.10

The results shown in Table 5.8 and Figure 5.33 confirm the enhanced performance of the amplifier using analytically calculated impedance values in terms of small-signal power gain, linearity and efficiency by as much as 2 dB, 1.3-1.8 dBm and 8-13.61% respectively. Table 5.8 also shows the percentage error in measured and predicted results of these three parameters of -2.71%, -8.20%, 10.51% and -34.01%, -12.77%, -54.10% for analytic approach and vendor model respectively. This data is the average of measured results for each prototype amplifier across three different device chips.

Figure 5.34 shows the output return loss for both the prototype amplifiers. The values and corresponding voltage standing wave ratio (VSWR) are summarised in Table 5.9.

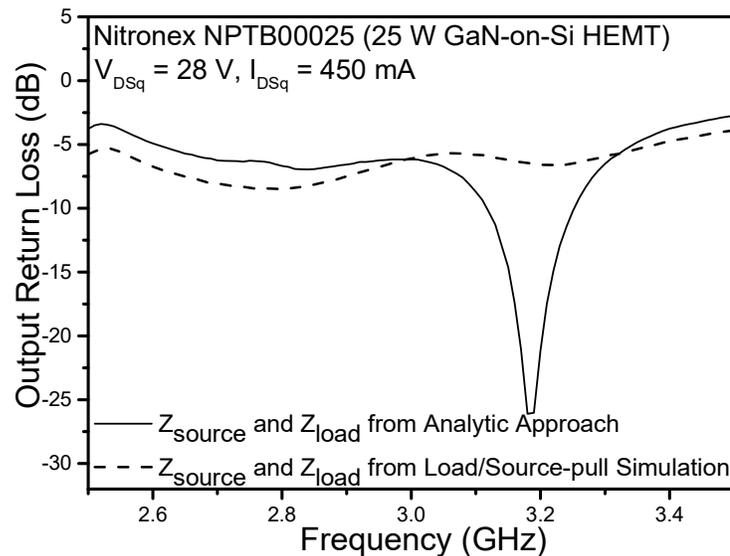


Figure 5.34: Comparison of return loss at the output for amplifiers using vendor model and analytic approach impedance values at 450mA for the 25 W GaN-on-Si HEMT.

Table 5.9 A comparison of return loss and corresponding VSWR at the input and output of the 25 W GaN-on-Si HEMT amplifiers

	Vendor Model		Analytic Approach	
	Return Loss	VSWR	Return Loss	VSWR
Input	21.86	1.18:1	11.88	1.68:1
Output	5.80	3.11:1	26.11	1.10:1

When the load impedance does not match with the output impedance of the device, reflections occur at the load resulting in higher return loss and voltage standing wave is created depending on the phase of the incident and reflected voltage waveforms. The output return loss using the vendor model impedance values is 5.80 dB which results in a VSWR of 3.11:1 compared to the output return loss of 26.11 dB and corresponding VSWR of 1.10:1 for the analytically calculated impedance values. Higher value of return loss causes output power loss [5.6], [5.7] and degradation in efficiency [5.8] due to load mismatch. Therefore, the difference in performance of the prototype amplifiers can be attributed to accuracy of the impedance values as the effect of the mismatch is reflected in poorer RF performance. Beside performance degradation, the excessive reflected power can affect the stability of the amplifier and cause it to oscillate [5.9] and severely damage the device [5.7]. Higher voltage standing wave ratio (VSWR) can also cause heat dissipation [5.6], [5.9], and consequently an increase in the junction temperature [5.8], [5.9] which affects the performance and long-term reliability of the device.

5.8 Impact of Various Sources of Errors

5.8.1 Measurement and Characterisation

The accuracy of the results obtained from any model or method depends on the accuracy of the used data. Although calibration is performed before measurements to eliminate system errors, uncertainty and errors in the measurements, characterisation and extraction can still introduce errors in the calculated results.

5.8.1.1 Effects of Parameter Values

In Figure 5.33 and Table 5.8, a difference of nearly 3 dB in power gain is evident between calculated results using the analytic approach and the simulated results using the vendor model for the GaN-on-Si HEMT. A further insight is available from the examination of the L_s , R_g , C_{gd} , and g_{ds} as these parameters affect the RF performance [5.10]. The values of these parameters obtained from measurement are higher than the

values extracted from the large-signal model provided by the vendor. A higher source inductance, L_s results in higher input power in order to oppose the voltage drop induced, thus decreasing the power gain whereas the gate resistance R_g increases the resistive loss at the input of the device. Higher values of the feedback capacitance, C_{gd} restrain the high frequency gain.

Figure 5.35 shows the measured and modelled S-parameters of the 25 W GaN-on-Si HEMT. A comparison between measured and vendor model S-parameters shows prominent difference between the S_{21} and S_{22} parameters which correspond to the gain and output impedance of the device. The higher value of S_{21} leads to overestimation of power gain. The RF performance of the power amplifiers strongly depends on the load impedance, Z_{load} which is mainly influenced by parameters L_d , C_{ds} , g_{ds} and C_{gd} . Except C_{gd} , the parameters L_d , C_{ds} and g_{ds} are extracted from S_{22} . Hence, the value of load impedance can be primarily attributed to S_{22} . Therefore, the different load impedance values from the vendor model and analytic approach in Table 5.8 are expected due to the difference in simulated and measured s-parameters for the device.

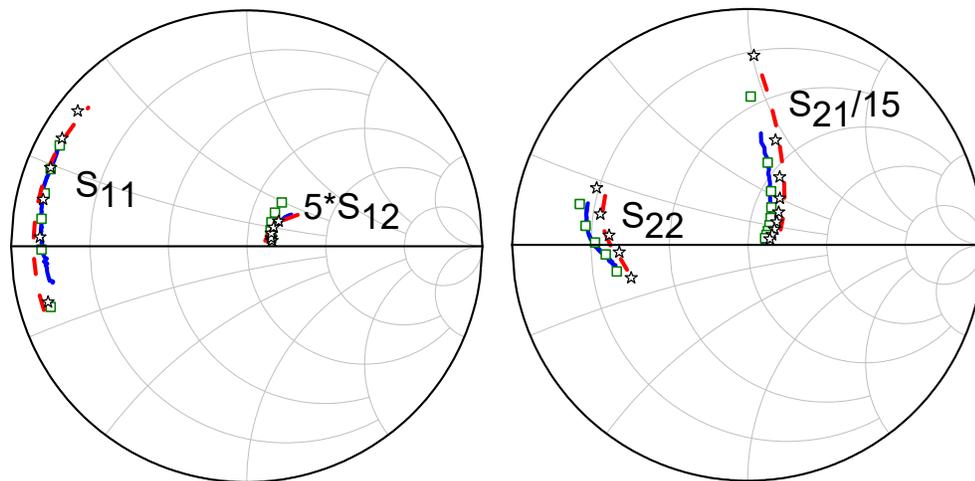


Figure 5.35: Measured (solid) and modelled (\square) S-parameters for the 25 W GaN-on-Si HEMT (Nitronex NPTB00025) at $V_{DS} = 28$ V, $I_{DSq} = 450$ mA, Freq = 0.4 - 3.5 GHz. It also shows the vendor model (dash) and modelled (\star) S-parameters from simulation.

The influence of each of the parameter on the power gain is examined by replacing its value to the same value as the vendor model one at a time in (5.22) - (5.25). The RF performance is re-calculated and the difference can be attributed to the value of the specific lumped element as shown in Table 5.10.

Table 5.10 The influence of parameters on the RF performance for the 25 W GaN-on-Si HEMT (Nitronex NPTB00025)

	Power Gain (dB)	P1dB (dBm)
Initial Values	12.89	39.51
Replacing L_s	13.49	39.41
Replacing R_s	13.47	39.25
Replacing R_g	13.65	39.70
Replacing C_{gd}	13.53	39.41
Replacing g_{ds}	13.11	40.30
Replacing $L_s, R_s, R_g, C_{gd}, C_{ds}$ and g_{ds}	15.21	40.42

Influence of different parameters on impedance values can be seen in Table 5.11. The difference in Z_{source} and Z_{load} can be primarily attributed to L_g and L_d respectively. The parameters C_{gd} , C_{ds} and g_{ds} also affects the impedance values.

Table 5.11 Influence of parameters on the source and load impedance values for the 25 W GaN-on-Si HEMT (Nitronex NPTB00025)

	$Z_{source} (\Omega)$	$Z_{load} (\Omega)$
Initial Values	$2.51-j*7.79$	$3.77-j*0.54$
Replacing L_g	$2.98-j*13.12$	$4.31-j*1.05$
Replacing L_d	$2.83-j*7.78$	$4.50-j*5.13$
Replacing R_s	$2.12-j*7.58$	$3.64-j*0.57$
Replacing C_{ds}, C_{gd} and g_{ds}	$2.75-j*7.87$	$5.22+j*0.98$
Replacing $L_g, L_d, R_s, C_{ds}, C_{gd}$ and g_{ds}	$2.89-j*12.88$	$5.97-j*3.83$

5.8.1.2 Effects of I-V Characteristics: DC-to-RF Dispersion

Frequency dispersion of the I-V characteristics due to trapping and self-heating effects in GaN HEMTs influences the large-signal performance at microwave frequencies. Under the RF signal, the dynamic or ac components of the gate and drain voltages change according to the frequency of the applied signal. Electrons are captured by the surface and buffers traps and released due to change in voltages. In AlGaIn/GaN devices, these capture and emission time constants of the traps are asymmetric as the capture time is faster compared to emission time. As a result, these electrons cannot be part of the output current straightaway and the output current under this condition is lower than the DC current. The amount of current dispersion due to trapping depends on the rate of change of the dynamic voltage components or the RF components. Trapping induced DC-to-RF dispersion, also known as current collapse, is responsible

for limiting the output power predicted from the DC I-V by compressing the RF current swing [5.11] in GaN HEMT devices due to less current available in the active channel [5.12]. The reduction of the average output current due to the trapping effects with increasing power influences the gain compression characteristics [5.13]. Implementation of silicon nitride passivation layer [5.14], GaN cap layer [5.15], and field plates [5.16] which reduce the effect of surface traps. Buffer traps due to intrinsic material characteristics like lattice mismatch are more difficult to avoid. Therefore, current dispersion due to trapping effects still cannot be totally avoided.

In order to characterize the gate-lag and drain-lag effects, pulsed I-V measurements with typical pulse widths of 100 ns to 10 μ s are performed [5.17]. The narrow pulse width allows to avoid the self-heating effect to distinguish between the impacts of both phenomena individually. If the electron emission time from any of the traps in these devices are in few micro-second range, then the measured I-V would not be able to account for these traps which would normally affect the device performance under high frequency RF operation. However, such pulsed I-V measurement systems for high power devices with more than 1 A drain current are very expensive and not easily available. The lack of measurement equipment often restrains a designer to acquire appropriate I-V curves. The B1505 from Keysight Technologies used for the I-V characteristics measurement allows a minimum pulse width of 500 μ s. As a result, the measured IV characteristics of these devices under this condition might not represent the trapping effects under high frequency operation in total accuracy.

Self-heating due to power dissipation in high power devices increases the junction temperature which reduces electron saturation velocity and low-field mobility, and consequently drain current and output power are degraded [5.18]. GaN HEMTs suffer more from self-heating effect compared to Si or GaAs FETs because of higher power densities. Hassan et al. [5.19] showed that the soft gain compression in GaN HEMT based PAs are only observable under static conditions like continuous-wave (CW) signals, but not under dynamic conditions such as modulated signal. The authors suggested that, unlike the modulated signals where the device temperature depends on the average power, the measured RF performance at each input power level is at different device temperatures under CW signal. The effective thermal resistance increases with increasing pulse width and the differences in effective thermal resistance under CW and short pulses conditions can be factors of four or more [5.20].

The increased effective thermal resistance under CW condition would cause increased self-heating in the device.

In order to observe the effects of trapping and self-heating, the RF performance of the 25 W GaN-on-SiC HEMT is re-calculated with different sets of simulated IV from the vendor model which from our experience is an excellent model. The trapping effect can be observed under pulsed conditions. The self-heating effect can be disabled which allows to evaluate the RF performance with and without its impact. The simulated I-V characteristics are obtained using 200 ns pulse width with 10% duty cycle.

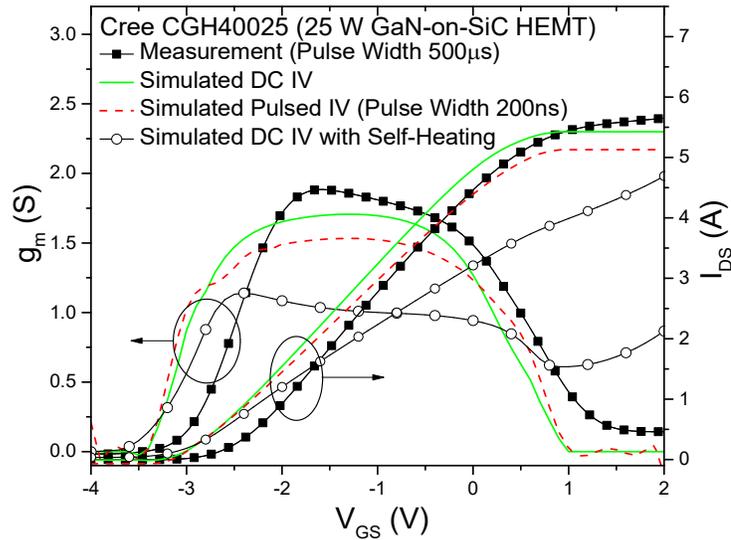


Figure 5.36: Comparison of measured (—■—) and simulated I-V curves under DC, with (—○—) and without self-heating (—), and pulsed (---) conditions for Cree CGH40025. The simulated I-V characteristics show current collapse due to dispersion effects under self-heating and pulse conditions.

Figure 5.36 shows the measured and simulated I-V characteristics and corresponding transconductance values for the Cree CGH40025. It can be seen that the values of maximum current from measurement under a pulse width of 500 μs match closely with simulated DC I-V without any self-heating effect. The value of maximum drain current simulated under a pulse width of 200 ns and DC condition with self-heating effect is less than the simulated DC I-V characteristic without any self-heating. The decrease in drain current can be attributed to current collapse due to traps and self-heating induced dispersion effects. The corresponding transconductance values at 450 mA for measured and simulated IV characteristics under DC and pulsed are 1.26 S, 1.29 S and 1.21 S respectively. The transconductance value from the simulated DC I-V with self-heating effect is 1.01 S. The optimum impedance values and RF performance are calculated by the analytic expressions using these different sets of I-

V characteristics. Since in these analyses, all the other parameters in (5.22) -(5.25) are unchanged except the I-V characteristic, any alteration in the device performance can be attributed to a specific set of I-V curves.

Figure 5.37 shows the power gain and output power against input power obtained from analytical calculation, HB simulation using the vendor model and UoS model and experimental measurements for the Cree CGH40025. The results are summarised in Table 5.12. In this analysis, the difference in the analytically calculated results can be attributed to the different I-V curves in Figure 5.36.

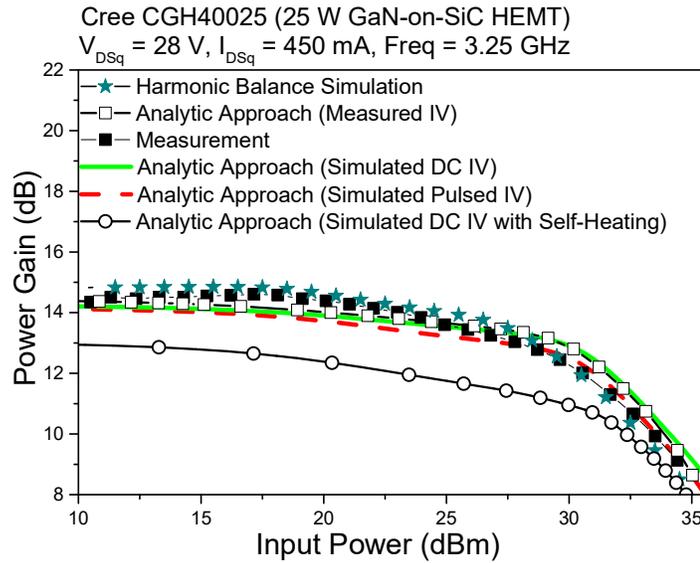


Figure 5.37: Comparison of HB simulated, analytically calculated and measured results for the 25 W GaN-on-SiC HEMT RFPA at 3.25 GHz and $V_{DS} = 28$ V and $I_{DSq} = 450$ mA using different sets of IV characteristics.

Table 5.12: The Influence of device I-V characteristics on the performance

Condition	Gain (dB)	P1dB (dBm)
Harmonic Balance Simulation (using vendor model)	14.81	40.07
Analytic Approach (using measured I-V – 500 μ s)	14.72	41.23
Measurement	14.51	39.70
Analytic Approach (using simulated DC I-V)	14.24	41.52
Analytic Approach (using simulated DC I-V with self-heating)	13.02	34.86
Analytic Approach (using simulated pulsed I-V – 200ns)	14.17	39.88

The results show that when DC I-V curves with self-heating are considered in the analysis, the predicted device performance is worse than experimental result due to the lower value of drain current and transconductance value. In high frequency operation on the RF PA, the simulating signal does not evidently increase the internal temperature of the device and the self-heating effect is not prominent as observed in

DC or static IV curves. Therefore, the DC I-V curves with self-heating gives worst-case performance the device under RF operation where the input signal is slow enough to heat up the device. In case of the measured, simulated DC and pulsed (200 ns) I-V curves, the small signal gain is similar because of the comparable values of g_m at the bias condition of 450 mA. Since the measured and simulated DC I-V curves display similar values of maximum output current, the values of output power at 1-dB compression point in both cases are close. When the simulated pulsed I-V curves are considered, the output power at 1-dB compression point is reduced to 39.88 dBm from 41.52 dBm as seen in Table 5.12 due to the reduced output current at higher gate voltages. The power gain curve starts to show compression at lower input power which is similar to the behaviour observed in measurement. Therefore, based on the results it can be suggested that the soft gain compression can be induced by the electron trap-related phenomena in the device. The results also demonstrated that the prediction of linearity by analytical approach can be improved with more accurate measurement of device I-V characterization.

The measured results for CGH40025 and NPTB00025 show that the GaN-on-SiC HEMT displays better performance than the GaN-on-Si HEMT despite both devices having the same power rating of 25 W. This can be attributed to superior device characteristics of the CGH40025. Figure 5.39 displays the I_{DS} - V_{GS} characteristics and corresponding transconductance for the 25 W GaN HEMTs.

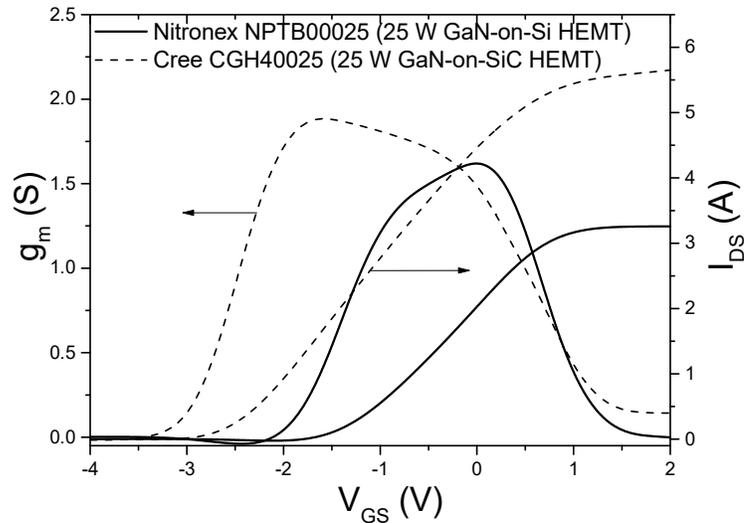


Figure 5.38: Measured drain current (I_{DS}) versus gate-to-source voltage (V_{GS}) and corresponding transconductance (g_m) for the Nitronex NPTB00025 (25 W GaN-on-Si HEMT) and Cree CGH40025 (25 W GaN-on-SiC HEMT)

It can be seen from Figure 5.38 that the maximum drain currents are 5.65 A and 3.25 A respectively for the 25 W GaN-on-SiC HEMT (Cree CGH40025) and GaN-on-Si HEMT (Nitronex NPTB00025) devices. The higher drain current leads to a greater value of maximum current swing and thus higher output power for the CGH40025 than the NPTB0025. From Figure 5.38 it can also be noted that the value of transconductance of CGH40025 at the bias point of $V_{DSq} = 28$ V and $I_{DSq} = 450$ mA is 1.26 S compared to 1.12 S for NPTB0025 and remains fairly constant for a wide range of gate voltages. These result in higher power gain and linearity in the GaN-on-SiC HEMT. In addition, compared to the GaN-on-SiC HEMT, GaN-on-Si HEMT has larger values of source inductance, feedback capacitance and output capacitance which also cause the inferior performance. Figure 5.39 shows that the analytically calculated and measured power gain and output power for the 25 W GaN-based RFPAs with CGH40025 and NPTB00025.

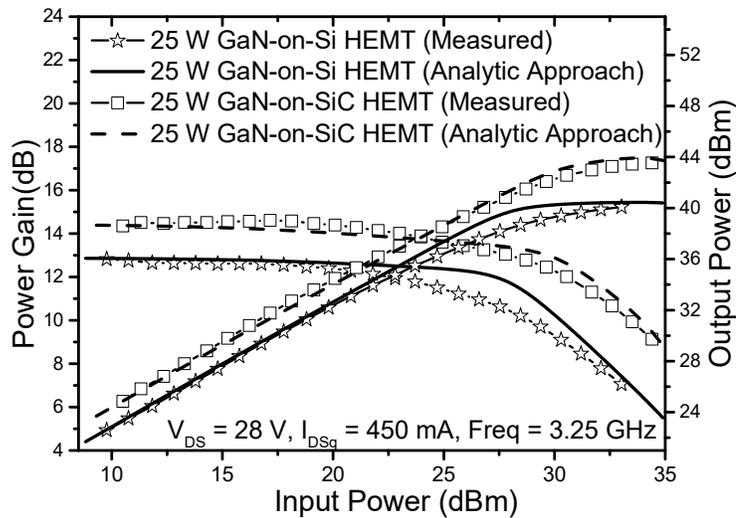


Figure 5.39: Comparison of analytically calculated and measured results for the 25 W GaN-on-Si and GaN-on-SiC HEMT RFPAs at 3.25 GHz and $V_{DS} = 28$ V and $I_{DSq} = 450$ mA.

The analytically calculated (41.23 dBm) and measured (39.70 dBm) output power at 1-dB gain compression point for the Cree CGH40025 are in close agreement with an error of -3.7% in P1dB prediction compared to Nitronex NPTB00025, in which has an error of -8.2% in prediction.

It has been already demonstrated that the current collapse due to trapping effects can be responsible for the DC-to-RF dispersion in GaN HEMT based RF PAs. The lattice mismatch between GaN and silicon is 17%, which is much higher than the 4% mismatch between GaN and SiC. In addition, the thermal expansion coefficient

mismatch between GaN and silicon is 54% compared to 3.2% between GaN and SiC. These effects can lead to higher density of dislocation in the GaN buffer layer in GaN-on-Si during the fabrication process. Therefore, the GaN-on-Si HEMT may have larger number of traps compared to GaN-on-SiC HEMT and as a result, the DC-to-RF dispersion is higher in the NPTB00025 based prototype amplifier than the CGH40025 based amplifier.

5.8.2 Assumption

In principle, models are always simplified representation of device physics and operation in real world. The extent of simplification varies from model to model. The assumptions made to derive a model can often be sources of error since it is a trade-off between complexity and accuracy. One such assumption in the analytic approach is considering a constant value of the input capacitance. Therefore, it is important to determine the consequences of this assumption on the calculated impedance values and predicted RF performance.

5.8.2.1 Effects of Nonlinear Input Capacitance

The gate-to-source capacitance (C_{gs}) plays an important role in the performance of an RF power amplifier and is therefore an essential component in large-signal modelling. Its nonlinear characteristic changes the phase response of an input matching network designed for a particular impedance and causes amplitude-to-phase distortion (AM/PM) [5.21].

The AM/PM distortion is the alteration in the phase of the output signal relating to the variation in the amplitude of the input signal. The analytic approach assumes that a known signal V_{gs} is directly imposed on the current generator. In real case, V_{gs} has to be determined from the input signal of the amplifier. Considering the device nonlinearities, the analysis would be beyond the scope of analytic approach and the harmonic balance is required. Therefore, in order to observe the influence of the nonlinear input capacitance, a large-signal model of the RT233, a 2 W GaN-on-SiC HEMT, is constructed in ADS. The low power of this device allowed the extraction of input capacitance at multi-bias points within the limitation of available measurement equipment. When an input signal is applied, the capacitance value changes accordingly to the signal amplitude resulting in an effective input capacitance which is a function of input power. The effective capacitance values at 2.5 GHz and

$V_{DS} = 28$ V, $I_{DSq} = 140$ mA are obtained from HB simulation in ADS and implemented via a look-up table as a function of input power in the analytic approach.

Figure 5.40 shows the values of input capacitance (C_{gs}) extracted experimentally for a range of gate-to-source voltage (V_{GS}) from -4 V to 3 V for RT233, the 2W GaN HEMT from RFHIC Corporation. The nonlinear current generator and the nonlinear capacitance are modeled as nonlinear polynomial functions of the order of 11 (Figure 5.40).

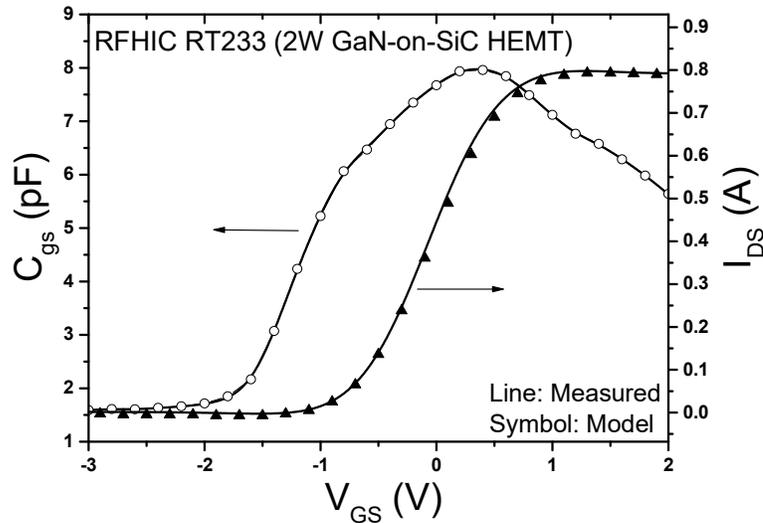


Figure 5.40: Measured and modelled input capacitance values and I_{DS} - V_{GS} curve for the 2 W GaN-on-SiC HEMT.

The effective capacitance values at 2.5 GHz and $V_{DS} = 28$ V, $I_{DSq} = 140$ mA as shown in Figure 5.41 are obtained from HB simulation in ADS and implemented via a look-up table as a function of input power in the analytic approach

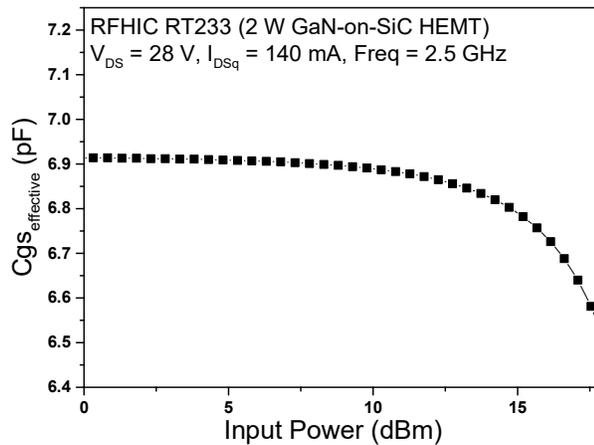


Figure 5.41: The effective capacitance of the 2 W GaN-on-SiC HEMT as a function of input power at 2.5 GHz and $V_{DS} = 28$ V, $I_{DSq} = 140$ mA.

Another large-signal model is constructed where the input capacitance (C_{gs}) is set to a constant value of pF which corresponds to the bias condition of $V_{DS} = 28$ V and $I_{DSq} = 140$ mA. Two Class AB amplifiers are designed and simulated in ADS using both models.

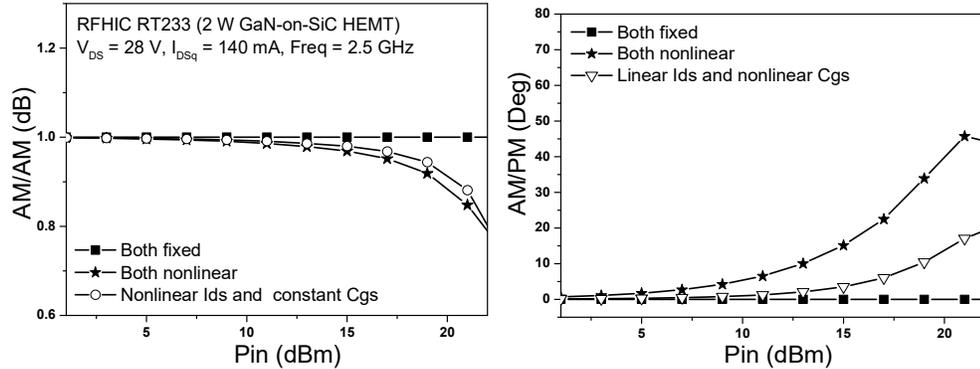


Figure 5.42: Influence of nonlinear current source and input capacitance on the AM/AM and AM/PM distortions for the RFHIC RT233, a 2 W GaN-on-SiC HEMT.

Figure 5.42 shows the phase and amplitude distortions obtained from HB simulations for both the large-signal models for RT233. It can be seen that the nonlinear C_{gs} has little to no impact on the amplitude-to-amplitude (AM/AM) distortion and the main source of AM/AM distortion is the nonlinear current generator. The nonlinear characteristics of both the input capacitance C_{gs} and drain current I_{ds} contribute to the AM/PM distortion in the RF PA.

Now the optimum impedance values and the RF performance are calculated using the analytic expressions by considering fixed and nonlinear C_{gs} values and the results are presented in Figure 5.43 and Table 5.13.

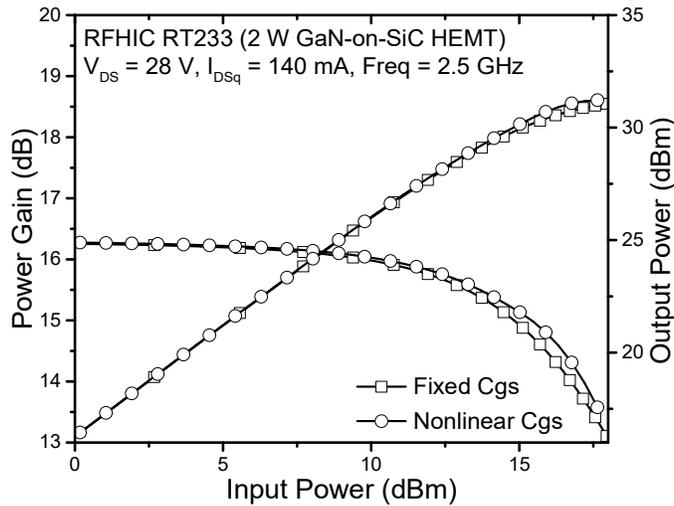


Figure 5.43: Analytically calculated RF performance for RFHIC RT233, a 2 W GaN-on-SiC HEMT, at 2.5 GHz and $V_{DS} = 28$ V, $I_{DSq} = 140$ mA.

Table 5.13 Analytically calculated power gain, P1dB, PAE and optimum source and load impedance for the 2 W GaN-on-SiC HEMT (RFHIC RT233) at $V_{DS} = 28$ V, $I_{DSq} = 140$ mA, Frequency = 2.5 GHz

	Constant C_{gs}	Nonlinear C_{gs}
Z_{source} (Ω)	$2.65-j*11.30$	$2.65-j*11.33$
Z_{load} (Ω)	$10.61+j*34.79$	$10.61+j*34.79$
Gain (dB)	16.29	16.29
P1dB (dBm)	29.37	29.81
PAE@P1dB (%)	12.60	13.40

It can be observed that the characteristics of C_{gs} has minimal impact in the calculated impedance values, power gain and output power. Therefore, the consideration of linear input capacitance in the analytical approach does not cause any error in the prediction of output power at 1-dB compression point.

5.9 Summary

In this chapter, new analytic expressions are derived based on a 19-element equivalent circuit model considering the package parasitic. The analytic approach is extended to optimize the impedance values and calculate the RF performance for different criteria popularly used by RF PA designers, viz. maximum power gain, linearity and efficiency. Harmonic balance simulation using large-signal model, the most popular method to design RF PAs, is described and used as the first benchmark to evaluate the accuracy of analytic approach at different bias points, different criteria and high frequency by comparing the analytically calculated results with HB simulation. The results show that the analytic approach can calculate the impedance values in all cases with excellent precision. It can also predict the RF performance with good accuracy. A comparison of two identically rated commercially available 25 W RF power transistors in silicon LDMOS and GaN-on-Si HEMT technologies in terms of their respond to optimization showed that the GaN HEMT is comparatively immune to optimization than Si LDMOS due to higher values of feedback capacitance and output conductance. Prototype Class-AB RF power amplifiers using GaN-on-Si and SiC HEMTs are fabricated and measured for the first time at a high output power up of 25 W at a high frequency of 3.25 GHz to evaluate the accuracy and validity of the analytic approach in calculating the optimum impedance values and predicting the performance via measurements. Based on the experimental results, the analytic approach is established as a simple yet effective alternative to conventional method

such as harmonic balance (HB) technique to design and predict the RF performance of RF PAs with fair accuracy. Results from HB simulation using the corresponding vendor models are also compared to show that in absence of a good large-signal model, the analytically calculated impedance values helps to achieve better performance. The impacts of various sources of error in calculation are also studied. The results show that assumptions made to simplify the calculation does not compromise the overall accuracy of the analytic approach. However, the accuracy of the method in predicting large-signal performance can be improved by using I-V characteristics that represents current collapse responsible for DC-to-RF dispersion in a device.

References

- [5.1] J. Walker, "Analytic expressions for the optimum source & load impedance and associated large-signal gain of an RF power transistor," *2003 IEEE MTT-S International Microwave Symposium Digest*, Philadelphia, PA, USA, 2003, pp. 1725-1728 vol.3.
- [5.2] P. Fioravanti, O. Spulber and M. M. De Souza, "Analytic Large-Signal Modeling of Silicon RF Power MOSFETs," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, no. 5, pp. 829-837, May 2007.
- [5.3] N. Chevaux and M. M. De Souza, "New analytical expressions for the design of linear power amplifier using GaN HEMTs," *2009 Asia Pacific Microwave Conference*, Singapore, 2009, pp. 1112-1115.
- [5.4] S. Cripps, *RF Power Amplifiers for Wireless Communications*, Second Edition, Norwood, Artech House INC, 2006.
- [5.5] G. E. P. Box and N. R. Draper, *Empirical Model-Building and Response Surfaces*, New York, John Wiley & Sons, 1976.
- [5.6] RF Micro Devices, "Amplifier RF Voltage and Current Calculations for Different Loading Conditions," Greensboro, North Carolina, USA, Application Note AN120131, 2012.
- [5.7] Keysight Technologies, "Understanding RF / Microwave Solid State Switches and their Applications," USA, Application Note, May 2010.
- [5.8] C. Luetzelschwab, "The Impact of Load SWR on the Efficiency of Power Amplifiers," *QEX*, October 2005.

- [5.9] R. W. Brounley, “Mismatched Load Characterization for High-Power RF Amplifiers,” *High Frequency Electronics*, pp. 30–38, April 2004.
- [5.10] N. Chevaux and M. M. De Souza, “Comparative Analysis of VDMOS / LDMOS Power Transistors for RF Amplifiers,” in *IEEE Transactions on Microwave Theory and Technique*, vol. 57, no. 11, pp. 2643–2651, November, 2009.
- [5.11] C. Roff, J. Benedikt, P.J. Tasker, D.J. Wallis, K.P. Hilton, J.O. Maclean, D.G. Hayes, J. Powell, M.J. Uren and T. Martin, “Applications of Waveform Engineering for Analysing New Device Technologies,” *Automated RF & Microwave Measurement Society (ARMMS) Conference*.
- [5.12] C. Roff, J. Benedikt, P. J. Tasker, D. J. Wallis, K. P. Hilton, J. O. Maclean, D. G. Hayes, M. J. Uren, and T. Martin, “Analysis of DC – RF Dispersion in AlGa_N / Ga_N HFETs Using RF Waveform Engineering,” in *IEEE Transactions on Electron Devices*, vol. 56, no. 1, pp. 13–19, 2009.
- [5.13] O. Jardel, F. De Groote, T. Reveyrand, J. C. Jacquet, C. Charbonniaud, J. P. Teyssier, D. Floriot, and R. Quéré, “An electrothermal model for AlGa_N/Ga_N power HEMTs including trapping effects to improve large-signal simulation results on high VSWR,” in *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, no. 12, pp. 2660–2669, 2007.
- [5.14] P. McGovern, J. Benedikt, P. J. Tasker, J. Powell, K. P. Hilton, J. L. Glasper, R. S. Balmer, T. Martin, and M. J. Uren, “Analysis of DC-RF dispersion in AlGa_N/Ga_N HFETs using pulsed I-V and time-domain waveform measurements,” *IEEE MTT-S International Microwave Symposium Digest*, June, 2005, pp. 503-506.
- [5.15] L. Shen, R. Coffie, D. Buttari, S. Heikman, a. Chakraborty, a. Chini, S. Keller, S. P. DenBaars, and U. K. Mishra, “High-power polarization-engineered Ga_N/AlGa_N/Ga_N HEMTs without surface passivation,” in *IEEE Electron Device Letters*, vol. 25, no. 1, pp. 7-9, January 2004.
- [5.16] Y. F. Wu, A. Saxler, M. Moore, R. P. Smith, S. Sheppard, P. M. Chavarkar, T. Wisleder, U. K. Mishra, and P. Parikh, “30-W/mm Ga_N HEMTs by field plate optimization,” in *IEEE Electron Device Letters*, vol. 25, no. 3, pp. 117-119, March 2004.

- [5.17] D. E. Root, "Future Device Modeling Trends," in *IEEE Microwave Magazine*, vol. 13, no. 7, pp. 45-59, November-December 2012.
- [5.18] A. P. Zhang, L. B. Rowland, E. B. Kaminsky, V. Tilak, A. F. Allen and B. J. Edward, "Self-heating effects in AlGaIn/GaN high-power HEMTs," *Device Research Conference, 2003*, Salt Lake City, UT, USA, 2003, pp. 15-16.
- [5.19] H. Sarbishaei, D. Y. T. Wu and S. Boumaiza, "Linearity of GaN HEMT RF power amplifiers - a circuit perspective," *2012 IEEE MTT-S International Microwave Symposium Digest (MTT)*, Montreal, QC, Canada, 2012, pp. 1-3.
- [5.20] R. Pengelly, "Large Signal Modeling of GaN HEMT based Circuits," May, 2010.
- [5.21] T. Rahkonen, S. Hietakangas and J. Aikio, "AM-PM distortion caused by transistor's signal-dependent input impedance," *2011 20th European Conference on Circuit Theory and Design (ECCTD)*, Linkoping, 2011, pp. 833-836.

Chapter 6

Design and Implementation of an Ultra-Low Power Wireless Sensor Node

Abstract

Major issues and challenges present in wireless sensor technology are discussed. State-of-the-art micro-controllers, transceivers, power management integrated circuits and storage elements are compared to determine the best solutions to design an ultra-low power autonomous wireless sensor node. The performances of six solar cell technologies for indoor energy harvesting are assessed under a controlled light intensity of $77.40 \mu\text{W}/\text{cm}^2$. A comparison of the measured efficiencies of crystalline (c-Si), polycrystalline (poly-Si), amorphous silicon (a-Si), perovskite, gallium arsenide (GaAs) and dye-sensitized solar cells (DSSC) shows that both DSSC and GaAs solar cells exhibit an efficiency of $\sim 28\%$, whereas the efficiencies of perovskite and a-Si solar cells are 20.4% and 15.59% respectively. Considering both performance and cost, DSSC is the best choice for indoor light energy harvesting. Due to its high power density of $22.0 \mu\text{W}/\text{cm}^2$, the DSSC requires an area of 15 cm^2 to charge a 3.4 mAh rechargeable battery from a nominal voltage of 2.8 to 3.0 V in 60 minutes. A wake-up receiver is designed and implemented to reduce the power consumption of the wireless sensor node.

6.1 Introduction

The wireless sensor network was initially developed for military applications. The sound surveillance system (SOSUS) deployed by the United States Military in the 1950s can be considered as the first wireless network [6.1] which had any actual similarity to today's wireless sensor networks. This network used hydrophones connected with cables to monitor the movement of Soviet Union submarines in the ocean. The advancement of semiconductor and sensor technologies, networking topologies and protocols, energy harvesting and storage technologies and finally the convergence of these technologies reduced the cost and size of Wireless Sensor Nodes (WSNs). This has enabled the technology to be used in large-scale applications and become an integral part in our daily lives. Today, the applications of wireless sensor networks have extended from surveillance and enemy tracking to environment monitoring such as pollution, forest fire and flood detection. The WSNs are used in agriculture to monitor the condition of soil, crop and change in the climate or number of weeds or pests and thus help farmers to respond appropriately and increase the productivity. In healthcare, range of applications have emerged which can extensively expand and significantly improve the quality of services in hospitals and care centres. The WSN technology is already widely used in industrial automation, disaster management, structure monitoring, traffic control and transportation. In recent times, smart homes and cities are drawing a lot of attention as the key areas of application of WSN. Home automation allows an end user to control the lighting, heating and cooling systems with convenience. Hive from British Gas and Nest from Google are smart thermostats that are already being used at homes to monitor and control the heating and hot water. In addition to convenience, these smart meters help to save energy and ensure safety. The application of the WSN in this work is to sense the ambient temperature.

The organization of this chapter is as follows: some of the major issues and challenges present in wireless sensor technology are discussed first. The design and implementation of the wireless sensor node in this work addresses one of these challenges, which is limited energy source. Choosing the appropriate component is vital to a successful design process. Therefore, the latest commercially available off-the-shelf components such as micro-controllers, transceivers, power management

integrated circuits and storage elements are compared to determine the best option. Next, a brief description of six solar cell technologies is presented. The measurement setup and experimental details to determine the efficiency of solar cells in an indoor condition is presented and crystalline silicon (c-Si), polycrystalline silicon (poly-Si), amorphous silicon (a-Si) solar cells and dye-sensitized solar cell (DSSC) are characterized in a controlled light intensity of $77.40 \mu\text{W}/\text{cm}^2$ at room temperature. Their performances are then compared with the perovskite and gallium arsenide (GaAs) solar cell results reported in [6.2], [6.3] respectively. The charging characteristic of a rechargeable battery is also studied as a function of the open-circuit voltage (V_{OC}), short-circuit current (I_{SC}) and harvested power from the solar cells ($P_{Harvested}$). Finally, a wake-up receiver is designed and implemented to reduce the power consumption of the wireless sensor node.

6.2 Challenges in Wireless Sensor Nodes and Networks

A wireless sensor node is a small device that combines the sensing, processing, storage, communication and power supply in it. It collects information about the surroundings and environment and sends it to a base station or sink node directly or via other nodes. At least one sink node and a number of sensor nodes form a wireless sensor network. Sometimes, these nodes are deployed in remote and difficult to reach areas. Once deployed, these sensor nodes are usually unattended and expected to work autonomously. However, there are various challenges faced by the researchers and engineers while designing and implementing a wireless sensor network. Therefore, it is essential to understand the existing challenges in this technology. Some of the major challenges are briefly described below:

Limited Resources: A sensor node typically has low processing capability and limited amount of memory. As a result, the data processing, storage and information transferring capability of an individual sensor node is very limited. Therefore, the algorithms and protocols should be designed to make the best use of the limited resources. In addition, a wireless sensor network can consist of thousands of nodes. Therefore, it is desirable that an individual node is cheap.

Limited Energy: A sensor node needs energy for data sensing, processing and communicating. Most of the wireless sensor nodes are powered by batteries that have finite energy. Once the energy is consumed, they have to be changed or recharged which

can be difficult, expensive and cumbersome. This limited energy of the storage poses a significant challenge in the design process of a WSN. It is crucial that both the hardware design and software protocols are energy efficient.

Lifespan: The lifespan of a node is mainly restricted by limited energy. The lifespan of a sensor node can be shortened by the lifespan of the energy storage element. Ambient energy harvesting with a rechargeable storage element is the most popular solution for a wireless sensor node. However, a rechargeable energy storage element can go through a finite number of charging-discharging cycles before it can no longer meet the expected quality of service. This process can be delayed with reduced energy consumption. Therefore, the overall power consumption of a sensor node needs to be minimized in order to extend the lifespan.

Lack of Common Standards: Currently there are different solutions such as ZigBee, Z-Wave, Insteon and Wavenis for implementing a wireless sensor network. This presents a challenge to large-scale deployment, as there is no direct communication between these various standards without using gateway or proxies.

However, with the implementation of Internet Protocol (IP) based standard, it would be possible to connect all smart objects and sensors via the Internet. This is vital to make the Internet of Things into a reality. The ZigBee Alliance has already embraced this solution with ZigBee IP, which is an IPv6 based solution.

Data Management: Data collection is the primary objective of a sensor node. With the ever-increasing number of devices connected to a wireless sensor network, handling of the large volume of generated data would be one of the main challenges in near future. It will be necessary to increase the memory storage and processing capability of each sensor node in the network.

Security and Interference: Data integrity, confidentiality and authenticity has to be maintained to ensure the target node receives the exact data send by the source node and the data has not been intercepted or altered by anyone in middle. It is also essential to verify that a trusted sender has sent the data. With increasing number of treats and various kinds of attacks, security is a very challenging and complex issue in a wireless sensor networks.

6.2.1 Focus of this Work

The focus of the design and implementation of the WSN in this thesis is addressing the issue of limited energy. The work involves reduction of power consumption as well as using energy harvesting and storage to achieve autonomous operation.

There has been extensive research to make the wireless sensor nodes to be highly energy efficient and self-sustaining. The issue with power consumption has been primarily addressed in the literature in two ways. The first is implementing energy-efficient communication protocols medium access control [6.4], routing [6.5], data gathering [6.6] and topology management [6.7].

The second approach is by managing power consumption to avoid wasteful and inefficient activities. The work in this thesis adapts the latter approach by reducing the power consumption during idle time by implementing a wake-up receiver (WuR). The process is described in Section 6.3.4. Besides reduced power consumption, energy harvesting and storage are equally important to address the limited available energy in a WSN. The ability of a WSN to generate electricity by ambient energy harvesting has drawn particular attention. A “direct-use” energy harvesting architecture [6.8] must generate more power than the minimum requirement at all times which is inconvenient in most situations. A WSN powered by a rechargeable battery using the harvested power from ambient energy resources is the most effective and viable solution to achieve long lifetime and low maintenance cost. This is also one of the vital features for an autonomous WSN. Several energy sources such as mechanical vibration [6.9] - [6.12], thermal [6.13], [6.14], radio frequency [6.15] - [6.18], wind [6.19] - [6.21] and light [6.22], [6.23] have been explored.

Table 6.1: A comparison of various ambient energy sources in terms of available and harvested powers [6.24]

Source		Available Power	Harvested Power	Efficiency
Ambient Light	Indoor	0.1 mW/cm ²	10 μW/cm ²	5-30% [6.25]
	Outdoor	100 mW/cm ²	10 mW/cm ²	
Vibration /Motion	Human	0.5 m@1Hz 1 m/s ² @50Hz	4 μW/cm ²	1-10% [6.25]
	Industrial	1 m@5Hz 10 m/s ² @1kHz	100 μW/cm ²	
Thermal Energy	Human	20 mW/cm ²	30 μW/cm ²	0.15%
	Industrial	100 mW/cm ²	1-10 mW/cm ²	1-10%
Radio Frequency	Cell Phone	0.3 μW/cm ²	0.1 μW/cm ²	33.33%

Table 6.1 shows a comparison of various ambient energy sources reported in literature for WSNs in terms of available and harvested power. Amongst these various sources, outdoor light is the best energy source with highest power density. It is evident from Table 6.1 that under indoor conditions, light is the best energy source considering both power density and efficiency. However, the power available is typically less than $100 \mu\text{W}$, therefore micro-scale energy harvesting systems [6.26], [6.27] with ultra-low power circuits with maximum power point tracking (MPPT) have been proposed. Light energy harvesters have the disadvantage of being able to produce energy only in the presence of adequate light. Hybrid combination of energy sources [6.28] has been proposed to overcome this limitation. Wireless sensor nodes such as the one in this work can also solely depend on the storage element to operate in the dark or poor light conditions.

6.3 Structure of an Autonomous Wireless Sensor Node

Figure 6.1 displays the basic diagram of a typical autonomous ultra-low power WSN.

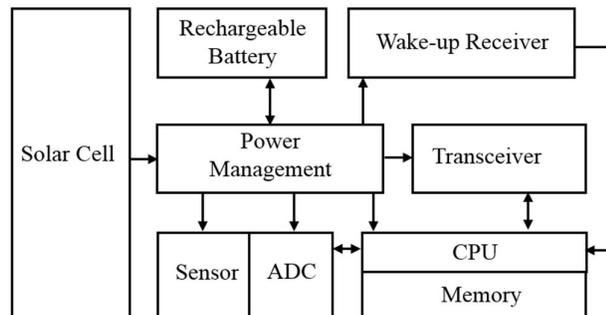


Figure 6.1: Block diagram of an autonomous wireless sensor node with rechargeable battery and power management with energy harvesting.

A sensor unit gathers data such as temperature, pressure or humidity from the surroundings and produces electrical or optical signals. An analog-to-digital converter or ADC in the microcontroller unit (MCU) converts the analog signals produced by the sensor and sends to the central processing unit or CPU. The CPU performs computation and processing the data, controls all the functionalities by the node. The MCU has memory storage to store the received data, processed information and instructions or code. The transceiver, which is the radio unit of the node, is controlled by the MCU to send and receive data. A power management unit (PMU) controls, allocates and supplies the required energy to each of these components. The PMU in

an autonomous wireless sensor node also consists a power boost converter with batter management to harvest the energy from ambient source like light using a solar cell to charge the rechargeable battery. Choosing the appropriate component is vital to successfully design a low power autonomous wireless sensor node. Therefore, in the following sections, state-of-the-art commercially available off-the-shelf components for the sensor node such as MCU, transceivers, PMU and storage elements are compared in order to determine the best solution.

6.3.1 Microcontroller Unit (MCU) and Radio Unit (Transceiver)

A microcontroller unit processes the data collected by the sensors, drives a radio unit for connectivity and performs all other tasks in a node. The selection of the MCU and radio unit totally depends on the specific application and system requirements. A MCU is evaluated based on key features such as bit, flash, memory, operating voltage, power consumption and response time. The selection of a radio unit or a transceiver depends on important features such as transmitter power, current consumption in receive (RX) and transmit (TX) modes, receiver sensitivity, throughput, types of modulation and carrier frequency. There are number of commercially available devices that integrate MCU and transceiver on a single chip. This significantly simplifies the design process.

Table 6.2: A comparison of various Micro-Controller Units (MCU)

MCU						
Model	Si1062	CC1310	MC12311	AX8052F151	PMA71x	nRF9E5
CPU	8051	ARM Cortex – M3	HCS08	AX8052 (Semi RISC Core)	8051	8051 compatible
Bit	8	32	8	8	8	8
Flash	64 KB	128 KB	32 KB	64 KB	6 KB	32 KB
RAM/ SRAM	4 KB	8KB and 20KB	2 KB	8.25 KB	256 bytes	4 KB and 256 bytes
ADC	10-bit	12-bit	12-bit	10-bit	10-bit	10-bit
Operating Voltage	1.8-3.6V	1.8-3.8V	1.8-3.6V	2.2-3.6V	1.9-3.6V	1.9-3.6V
Active Current	160 μ A/MHz	51 μ A/MHz	~500 μ A/MHz	150 μ A/MHz	155.8 μ A/MHz	250 μ A/MHz
Sensor Supply Current	35 μ A	400 μ A + 8.2 μ A/MHz	-	-	-	-
Current in Power Down Mode	120 nA	185 nA	450 nA	500 nA	590 nA	2500 nA
Response Time from Power Down Mode	2-50 μ s	1097 μ s	~595 μ s	3000 μ s	1410 μ s	1000 μ s

Table 6.2 shows a comparison of MCUs with integrated sub-1GHz transceivers: Silicon Labs' Si1062 [6.29], Texas Instruments' CC1310 [6.30], Freescale's MC12311 [6.31], ON Semiconductor's AX8052F15 [6.32], Infineon's PMA71xx [6.33] and Nordic Semiconductor's nRF9E5 [6.34]. It can be seen from Table 6.2 that the CC1310 from Texas Instruments has the best features among all the wireless MCUs. It has a 32-bit CPU and larger memory as well as lowest active mode current of 51 μ A per MHz. The Si1062 from Silicon Labs, on the other hand, has the lowest current consumption in low power down or sleep mode. If the data traffic in a network is low, then the WSN remains inactive for a long period. Therefore, the current consumption in this mode would be vital for the overall power consumption of the WSN. In addition, the CC13010 deploys a sensor controller that can run autonomously from the rest of the system. The supply current required for the sensor is significantly higher than that of the simpler sensor in Si1062. Most importantly, the response times from the power down mode for the CC1310 and Si1062 are 1097 μ s and 2-50 μ s respectively. The other four devices have considerably higher current consumption in power down mode as well as in active mode and high response times.

Table 6.3 shows a comparison of sub-1 GHz transceivers, which are integrated with the MCUs presented in Table 6.2.

Table 6.3: A comparison of the sub-1 GHz transceivers integrated with the MCUs in Table 6.2

Radio Transceiver						
Model	Si1062	CC1310	MC12311	AX8052F15	PMA71xx	nRF9E5
Max. Transmitter Power	+20 dBm	+14 dBm	+17 dBm	+15 dBm	+10 dBm	+10 dBm
Current RX	10/13 mA	5.5 mA	16 mA	17 mA	Not available	12.5 mA
Current TX (mA) @ +10 dBm	18 mA	12.9 mA	33 mA	22 mA	16.9 mA	30 mA
Receiver Sensitivity	-126/-110 dBm @500bps/40k bps, GFSK	-124 dBm @ 50kbps, GFSK	-115 dBm @ 4.5kbps, FSK	-98 dBm @ 100kbps, FSK	-70 dBm @ 32kbps, FSK	-100 dBm @ 50kbps, GFSK
Max. Throughput	1 Mbps	5 Mbps	300 kbps	600 kbps	32 kbps	50 kbps
Modulation Type	OOK, (G)FSK, 4(G)FSK	(G)FSK, MSK, OOK	FSK, GFSK, MSK, OOK	ASK, PSK, MSK, FSK	ASK, FSK	GFSK
Carrier Frequency (MHz)	142-1050	315,433,470,500,779,868,915,920	315, 433, 470, 500, 779, 868, 915, 920	400-470, 800-940	315, 433, 868, 915	433, 868, 915

It can be seen that the CC1310 from Texas Instruments has the minimum receive (RX) and transmit (TX) mode currents, and highest sensitivity. It also has the highest throughput. However, its maximum transmitter power is less than that of Si1062 from Silicon Labs. In addition, for a minimum order quantity of less than 2500 devices, the unit price of CC1310 is GBP 6.11; which is higher than that of GBP 4.11 for Si1062. The sensor nodes are deployed in hundreds and thousands in a wireless sensor network, therefore the price is also an important factor. Therefore, considering current consumption, response time, transmission power, sensitivity and price, Si1062 from Silicon Labs has been chosen as the best option for the processing unit with the integrated transceiver in designing this particular WSN application.

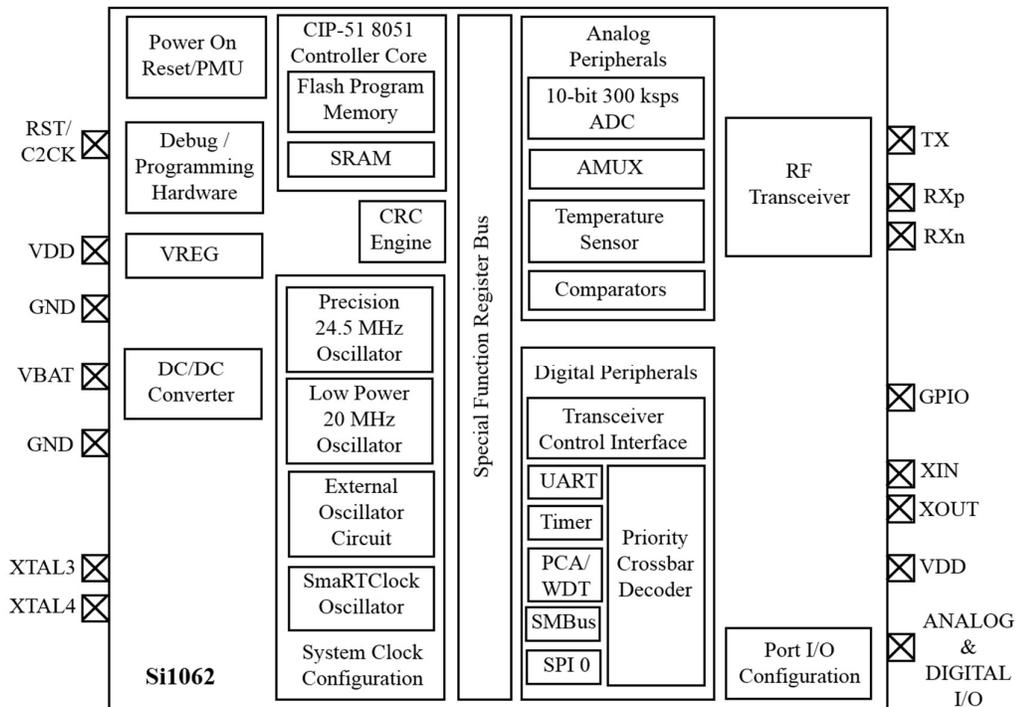


Figure 6.2: Block diagram of the ultra-low power MCU with integrated high-performance sub-1 GHz transceiver Si1062 from Silicon Laboratories [6.29].

Figure 6.2 shows the block diagram of Si1062. It uses a CIP-51 microcontroller core with a maximum system clock at 25 MHz; and it is totally compatible with the MCS-51 instruction set. The system clock can be configured using any of its four oscillators. The Si1062 has a set of analog and digital peripherals including a 10-bit, 300 ksp/s analog-to-digital converter (ADC), a 16-bit accumulator, dual comparators, an analog multiplexer (AMUX), temperature sensor, timer and general purpose input/output

(GPIO) pins. The Si0162 allows a designer the total control to assign analog and digital functions to specific port pins. While in sleep mode, the digital peripherals do not consume any power. Analog peripheral like the radio unit needs to be shut down before going to any low power mode to reduce the power consumption.

The Si1062 transceiver uses time division duplexing (TDD), which means it transmits and receives data packets by turns. It supports five different modulations schemes such as On-off keying (OOK), Gaussian frequency shift keying (GFSK), four-level GFSK (4GFSK), frequency-shift keying (FSK), and 4FSK. The Si1062 datasheet recommends GFSK modulation schemes for best performance and cleanest modulation spectrum. The transceiver in Si1062 has a Class-E power amplifier (PA) which is optimized to consume lowest current possible and thus provide very high efficiency. The PA is designed in single-ended configuration for simple antenna matching and lower budget.

6.3.1.1 Temperature Sensor

Access to the on-chip temperature sensor on Si1062 can be directly gained through the ADC multiplexer. The ADC mux channel have to select the temperature sensor to measure the temperature.

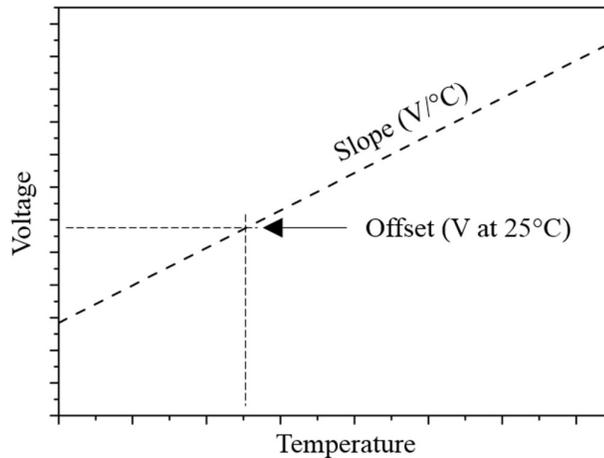


Figure 6.3: Transfer function of the temperature sensor.

The voltage measured (V_{Temp}) by the temperature sensor is converted to temperature, Temp ($^{\circ}C$), by using (6.1) by the transfer function shown in Figure 6.3.

$$Temp (^{\circ}C) = 25 + (V_{Temp} - Offset) / slope \quad (6.1)$$

The values of slope and offset in (6.1) and other electrical characteristics of the temperature sensor are given in Table 6.3.

Table 6.4: Electrical characteristics of the on-chip temperature sensor on Si1062 [6.29]

Parameter	Test Condition	Min.	Typ.	Max.
Linearity		-	± 1 °C	
Slope		-	3.40 mV/°C	
Slope Error		-	40 μ V/°C	
Offset	Temp = 25 °C	-	1025 mV	
Offset Error	Temp = 25 °C	-	18 mV	
Temperature Sensor Settling Time	Initial Voltage = 0V	-	-	3.0 μ s
Supply Current		-	35 μ A	-

6.3.1.2 External Reset as Wake-up Source

The power management unit (PMU) on Si1062 allows normal, idle, sleep, suspend and sleep mode. Amongst these five power modes, the sleep mode is the lowest power consumption state. While in sleep mode, the smart clock, port match, comparator or the reset pin can be used as a wake-up source. The system can also be put into a predefined default condition using one of the reset sources in Si1062. The external reset (RST) pin allows a circuit to put the MCU into a reset state. The device exits the sleep mode at any falling edge on RST. However, in order to force a system reset, the active low on the RST pin has to be more than 15 μ s. The wake-up receiver designed for the WSN utilizes this feature to wake-up the MCU in Si1062 from sleep mode.

6.3.1.3 Antenna Selection

An antenna is fundamental component for designing any wireless communication system. It converts electrical signals in electromagnetic waves and vice versa and radiates into free space so that they can travel the maximum distance possible. The most important criteria to select an antenna for RF applications are performance, size and cost. Table 6.5 shows the advantages and disadvantages of some commonly used antenna types.

Table 6.5: A comparison of various antenna types.

Type	Advantages	Disadvantages
Whip Antenna	+ good performance	- Expensive - Large size
PCB Antenna	+ low manufacturing cost	- Difficult to design - Large size at low frequency
Chip Antenna	+ small size + less influenced by interference	- Medium performance - Medium cost

As it can be seen from Table 6.5 that a whip antenna is the best solution if performance is the only priority. However, this type antenna is relatively expensive and larger in size. The wavelength λ at the frequency of operation determines the length of a whip antenna. The most commonly used whip antenna is an omni-directional quarter-wavelength or half-wavelength monopole antenna. This antenna consists one metal conductor of the length of $\lambda/4$ or $\lambda/2$ and radiates in all directions. The frequency of operation for this WSN has been chosen to be 868 MHz in order to comply with European ZigBee recommendations [6.35]. It is also compatible with smart meters for homes in UK [6.36] to ensure a better management of energy within in the building. The length of the whip antenna in the wireless MCU development kit from Silicon Labs [6.37] is 19.5 cm. This large size would prevent the designed WSN from achieving the desired small size and compactness.

Microstrip or PCB antenna is another type of antenna that is frequently used in RF applications. However, designing a PCB antenna is not straightforward. In addition, these antennas suffer from low power and efficiency. Chip or ceramic antenna offers a solution that is a compromise between all the required criteria of an antenna. A chip antenna consists a conductor with in a high dielectric material like ceramic, which results in slower velocity of propagation. Thus, the antenna is small at the frequency of operation. At the same time, these antennas are less influenced by any interference, which makes them ideal for compact design or three-dimensional structure. Therefore, an 868 MHz ultra-compact omni-directional chip antenna in a surface-mount package with a characteristic impedance of 50Ω from LinX Technologies [6.38] has been chosen for the WSN.

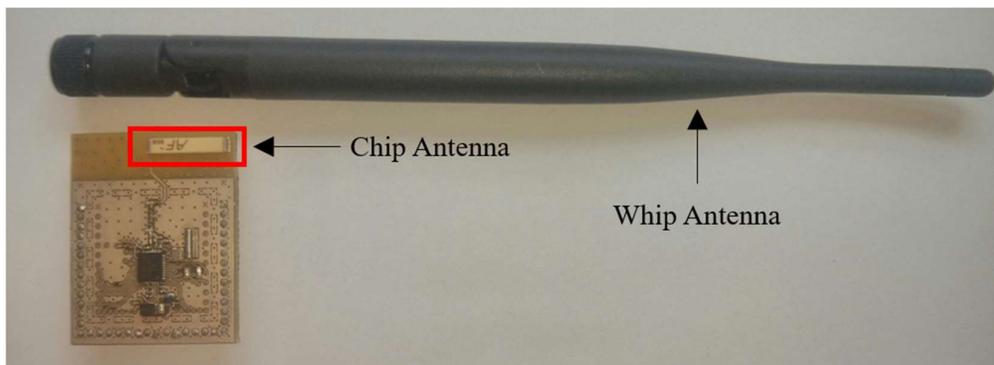


Figure 6.4: Photograph of the whip antenna and the chip antenna.

Figure 6.4 shows a size comparison of the chip antenna, just 1.6 cm in length, and the whip antenna, which is 19.5 cm in length. However, there is a trade-off between

compactness and performance. This chip antenna has a maximum gain is +0.5 dB compared to +2 dB of the whip antenna. Therefore, it has a shorter range of 2 meters than the whip antenna, which has a range of more than 4 meters.

6.3.2 Power Management

Since the WSNs are expected to operate autonomously when the availability of ambient light might be limited, the functions of a power management unit or PMU is crucial. Firstly, it must manage and allocate the limited energy to each component in the node. Secondly, it must efficiently acquire the low output power produced by the solar cells in indoor condition which is in the range of microwatts. The selection of the PMU is usually done on the basis of its quiescent current, voltage range, efficiency, low voltage operation and capability to extract the maximum power from a solar cell. A variety of commercial integrated circuit (IC) already exist for energy harvesting. Table 6.6 compares Texas Instruments' BQ25504 [6.39], Analog Device's ADP5090 [6.40], Linear Technology's LTC3105 [6.41], Maxim Integrated's MAX17710 [6.42], ST Microelectronics' SPV1050 [6.43] and Silicon Labs' TS3300 [6.44] power management ICs (PMICs).

Table 6.6: A comparison of various power management integrated circuits.

PMIC	BQ25504	ADP5090	LTC3105	MAX17710	SPV1050	TS3300
Input Voltage Range	0.13 – 3V	0.08-3.3V	0.225-5V	0.75 – 5.3V	0.15-18V	0.6-3V
V_{IN} (Cold Start)	330mV	380 mV	250 mV	750 mV	550 mV	600 mV
Quiescent Current	<330 nA	320 nA	24 μ A	635 nA (linear charging), 1 μ A (boost charging)	1.7-2.6 μ A	10.8 μ A
Maximum Efficiency	93%	93%	91%	N.A.	92%	84%
Output Voltage	2.5-5.25V	2.2-5.2V	1.6-5.25V	4.15-5.3V	2.2-5.3V	1.8-3.6V
MPPT	yes	yes	Yes	No	yes	no

It can be seen from Table 6.6 that BQ25504 and ADP5090 have the best performances considering input and output voltage range, cold start voltage, quiescent current and efficiency. Both implement the maximum power point tracking (MPPT) to ensure the maximum efficiency in energy harvesting from the solar cell itself. Any

of these two ICs could be chosen for the energy harvester. The PMU designed for the prototype WSN is based on the Texas Instruments BQ25504.

6.3.2.1 Theory of Operation and Design of the Power Management Unit

Figure 6.5 shows the schematic diagram of the power management unit designed based on the suggested application circuit by Texas Instrument for typical solar energy harvesting [6.39]. The pin configuration of the BQ25504 IC is also depicted in Figure 6.5 and the function of each pin is briefly described in Table 6.7.

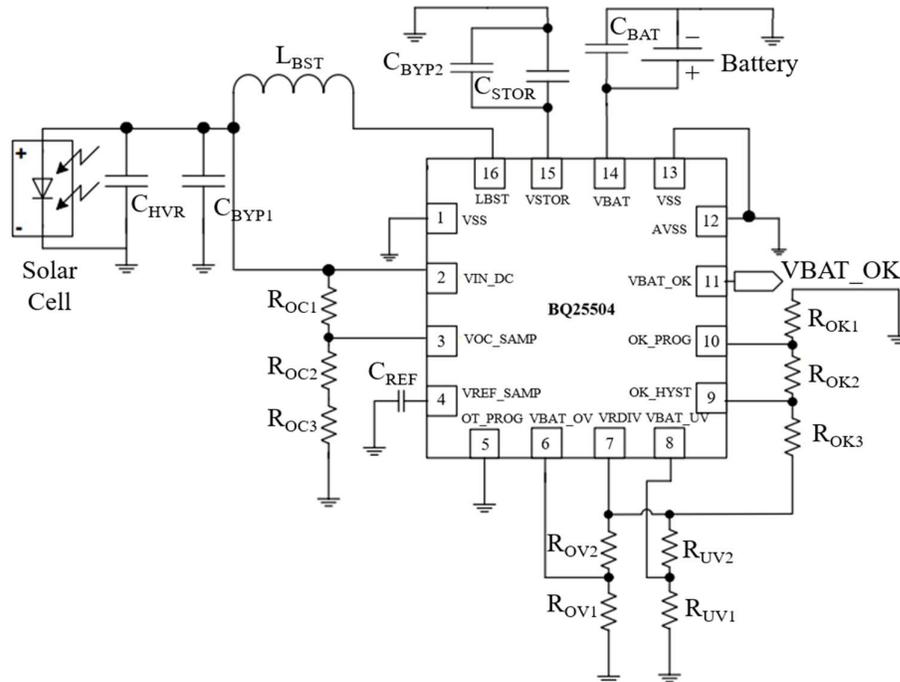


Figure 6.5: Schematic diagram of the power management unit (PMU) circuit using BQ25504 IC.

Table 6.7: Pin functions of the BQ25504 IC [6.39]

PIN		I/O	Description
No.	Name		
1	VSS	Input	General ground connection.
2	VIN_DC	Input	DC voltage input from the solar cell.
3	VOC_SAMP	Input	Sampling input voltage for the MPPT circuit.
4	VREF_SAMP	Input	Voltage provided by the MPPT circuit.
5	OT_PROG	Input	IC over-temperature threshold pin.
6	VBAT_OV	Input	Battery overvoltage threshold.
7	VRDIV	Output	Voltage divider biasing voltage.
8	VBAT_UV	Input	Battery undervoltage threshold.
9	OK_HYST	Input	Battery okay voltage hysteresis threshold.
10	OK_PROG	Input	Digital input for IC over temperature threshold.

11	VBAT_OK	Output	Digital output for indicating battery is okay.
12	AVSS	Supply	General ground connection.
13	VSS	Supply	General ground connection.
14	VBAT	I/O	Connected to the rechargeable battery.
15	VSTOR	Output	Connection for the boost charger output, typically connected to the load.
16	LBST	Input	Inductor connection for boost charger switching node.

Cold-Start and Boost Charging

If the V_{STOR} voltage is above the threshold voltage called V_{STOR_CHGEN} which is of typically 1.8 V, then the main boost charger can efficiently harvest the energy from the solar cell with an output voltage as low as 130 mV. However, if $V_{STOR} < V_{STOR_CHGEN}$, then cold-start (CS) circuit is activated instead of main boost charger. The CS circuit requires a minimum input voltage, $V_{IN(CS)}$, of 330 mV and a minimum input power, $P_{IN(CS)}$, of 15 μ W to operate. It is important that this minimum required input voltage and power for the power management IC is small enough that it can harvest the microwatts of power produced by the solar cells in indoor condition. This circuit has very low efficiency and its only objective is to charge V_{STOR} above V_{STOR_CHGEN} so that the main booster can operate. During this time, all the others features are turned off.

Maximum Power Point Tracking

Figure 6.6 shows the measured I-V characteristics and the corresponding power produced by a dye-sensitized solar cell panel in indoor condition.

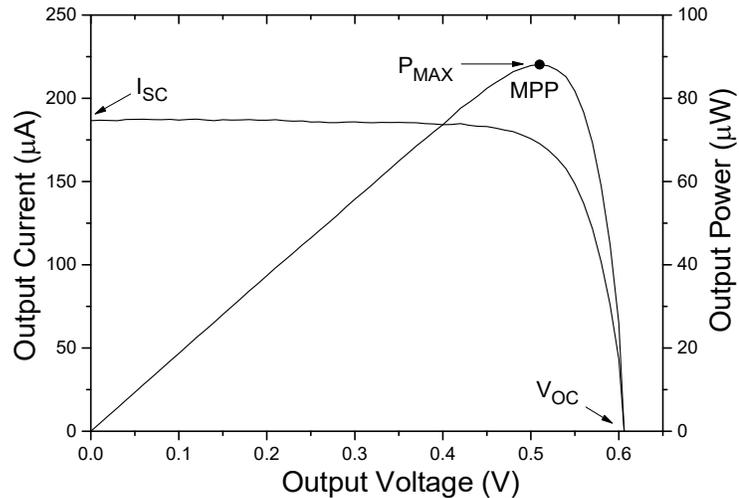


Figure 6.6: Measured I-V and P-V characteristics of a dye-sensitized solar cell panel displaying short-circuit current (I_{SC}), open-circuit voltage (V_{OC}) and maximum power point (MPP).

The open-circuit voltage (V_{OC}), the short-circuit current (I_{SC}), the maximum power point (MPP) and solar cell power conversion efficiency ($\eta_{\text{Solar Cell}}$) are the most important parameters to characterise a solar cell. The I_{SC} is the maximum output current from the solar cell when there is no load or short-circuit condition. In Figure 6.6, I_{SC} = current at $V = 0$ V. The V_{OC} is the maximum voltage capacity of the solar cell in the absence of current. In Figure 6.6, V_{OC} = voltage at $I = 0$ A. The power $P = IV$ is zero at both of these points and the maximum power from a solar cell is produced at a point, known as the MPP, between the two points. The voltage and current at MPP are $V_{MP, \text{Solar Cell}}$ and $I_{MP, \text{Solar Cell}}$ respectively. The ratio of $V_{MP, \text{Solar Cell}}$ and V_{OC} is 85%.

To maximize the power extracted from the solar cell or panel, BQ25504 implements a MPPT controller circuit. It acquires a new reference voltage every 16 s by occasionally deactivating the charger for 256 ms and sampling a fraction of the solar cell's open-circuit voltage ($V_{OC, \text{Solar Cell}}$) at V_{IN_DC} pin. For most of the solar cells, the maximum power point (MPP) is typically at 70-85% of their V_{OC} . The ratio of MPPT is set to 78% by using a simple external circuit with resistors R_{OC1} , R_{OC2} and R_{OC3} which work as a voltage divider between V_{IN_DC} and ground with mid-point at V_{OC_SAMP} .

$$V_{REF_SAMP} = V_{IN_DC}(V_{OC, \text{Solar Cell}}) \left(\frac{R_{OC1}}{R_{OC1} + R_{OC2} + R_{OC3}} \right) \quad (6.2)$$

The sample voltage is stored in the external capacitor C_{REF} connected to the V_{REF_SAMP} pin. The boost converter regulates the input voltage (V_{IN_DC}) to this reference voltage to extract the maximum power from the solar cell.

The inductor, resistors and capacitors are selected by following the guideline of recommended values by Texas Instruments [6.39] are seen in Table 6.8:

Table 6.8: Values for the inductor, resistors and capacitors for the PMU circuit

Component	Description	Min.	Nom.	Max.
C_{HVR}	Input Capacitance	4.23 μF	4.7 μF	5.17 μF
C_{STOR}	Storage Capacitance	4.23 μF	4.7 μF	5.17 μF
C_{BAT}	Equivalent Battery Capacitance	100 μF		
C_{REF}	Sampled Reference Storage Capacitance	9 nF	10 nF	11 nF
C_{BYP1}, C_{BYP2}	Bypass Capacitance		0.1 μF	
R_{OC_SUM}	Total Resistance for setting MPPT Reference	18 M Ω	20 Ω	22 Ω

R_{OK_SUM}	Total Resistance for setting VBAT_OK Reference	9 Ω	10 Ω	11 Ω
R_{UV_SUM}	Total Resistance for setting VBAT_UV Reference	9 Ω	10 Ω	11 Ω
R_{OV_SUM}	Total Resistance for setting VBAT_OV Reference	9 Ω	10 Ω	11 Ω
L_{BST}	Input Inductance	19.8 μH	22 μH	24.2 μH

Since the total resistance value for setting the MPPT reference is 20 M Ω , the values for R_{OC1} , R_{OC2} and R_{OC3} can be determined by rewriting (6.2) as (6.3) and (6.4).

$$R_{OC1} = R_{OC_SUM} \times \left(1 - \frac{V_{REF_SAMP}}{V_{IN_DC(VOC, Solar Cell)}} \right) = 20 \text{ M}\Omega (1 - 0.78) = 4.4 \text{ M}\Omega \quad (6.3)$$

$$R_{OC2} + R_{OC3} = R_{OC_SUM} \times \left(\frac{V_{REF_SAMP}}{V_{IN_DC(VOC, Solar Cell)}} \right) = 20 \text{ M}\Omega \times 0.78 = 15.6 \text{ M}\Omega \quad (6.4)$$

The values of R_{OC1} , R_{OC2} and R_{OC3} used in this design are 10 M Ω , 4.42 M Ω and 5.6 M Ω respectively.

Battery Overcharging and Discharging Protection

In order to protect the 3.0 V rechargeable battery from excessive charging voltages, the overvoltage (V_{BAT_OV}) threshold is set to 3.15 V using external resistors R_{OV1} and R_{OV2} and its value, when the battery voltage is increasing, is given by (6.5):

$$V_{BAT_OV} = \frac{3}{2} V_{BIAS} \left(1 + \frac{R_{OV2}}{R_{OV1}} \right) \quad (6.5)$$

The voltage V_{BIAS} is a reference voltage. The values of resistors R_{OV1} and R_{OV2} are calculated by (6.6) and (6.7) respectively.

$$R_{OV1} = \frac{3}{2} \frac{R_{OV_SUM} \times V_{BIAS}}{V_{BAT_OV}} = \frac{3}{2} \frac{10 \text{ M}\Omega \times 1.25 \text{ V}}{3.15 \text{ V}} = 5.95 \text{ M}\Omega \quad (6.6)$$

$$R_{OV2} = R_{OV_SUM} - R_{OV1} = 10 \text{ M}\Omega - 5.95 \text{ M}\Omega = 4.05 \text{ M}\Omega \quad (6.7)$$

The boost charger is disabled if the battery voltage reaches V_{BAT_OV} threshold. The boost charger starts working again when the battery voltage is below the threshold of ($V_{BAT_OV} - V_{BAT_OV_HYST}$) where $V_{BAT_OV_HYST}$ is an internal hysteresis voltage.

To save the battery from being deeply discharged and damaged, an undervoltage threshold voltage (V_{BAT_UV}) of 2.20 V is determined by using external resistors R_{UV1} and R_{UV2} . The value of V_{BAT_UV} when the batter voltage is decreasing is given by:

$$V_{BAT_UV} = V_{BIAS} \left(1 + \frac{R_{UV2}}{R_{UV1}} \right) \quad (6.8)$$

The values of resistors R_{UV1} and R_{UV2} are calculated by (6.9) and (6.10) respectively.

$$R_{UV1} = \frac{R_{UV_SUM} \times V_{BIAS}}{V_{BAT_UV}} = \frac{10 \text{ M}\Omega \times 1.25 \text{ V}}{2.2 \text{ V}} = 5.68 \text{ M}\Omega \quad (6.9)$$

$$R_{UV2} = R_{UV_SUM} - R_{UV1} = 10 \text{ M}\Omega - 5.60 \text{ M}\Omega = 4.4 \text{ M}\Omega \quad (6.10)$$

In order to V_{BAT_UV} feature to be functional, the load and battery must be connected to V_{STOR} and V_{BAT} pins respectively. When the V_{STOR} is above V_{BAT_UV} plus an internal hysteresis voltage $V_{BAT_UV_HYST}$, the V_{STOR} and V_{BAT} pins are effectively shorted via an internal PMOS FET. When the $V_{STOR} < V_{BAT_UV}$, the V_{STOR} and V_{BAT} pins are disconnected.

Battery Voltage in Operating Range (V_{BAT_OK})

To determine if the battery voltage is at the acceptable level of 2.44 V to turn on the system load, external resistors are used to set the threshold voltage V_{BAT_OK} . When battery voltage is decreasing, the threshold is given by (6.11):

$$V_{BAT_OK_PROG} = V_{BIAS} \left(1 + \frac{R_{OK2}}{R_{OK1}} \right) \quad (6.11)$$

When the battery voltage is increasing, the threshold is given by (6.12):

$$V_{BAT_OK_HYST} = V_{BIAS} \left(1 + \frac{R_{OK2} + R_{OK3}}{R_{OK1}} \right) \quad (6.12)$$

The logic high and low levels of this signal is equal to V_{STOR} and ground respectively. The $V_{BAT_OK_PROG}$ threshold has to be equal and greater than V_{BAT_UV} threshold. The values of the resistors R_{OK1} , R_{OK2} and R_{OK3} can be determined from (6.13) - (6.15) respectively.

$$R_{OK1} = \frac{V_{BIAS} \times R_{OK_SUM}}{V_{BAT_OK_HYST}} = \frac{1.25 \text{ V} \times 10 \text{ M}\Omega}{2.8 \text{ V}} = 4.46 \text{ M}\Omega \quad (6.13)$$

$$R_{OK2} = \left(\frac{V_{BAT_OK_PROG}}{V_{BLAS}} - 1 \right) \times R_{OK1} = \left(\frac{2.45V}{1.25V} - 1 \right) \times 4.46 M\Omega = 4.28 M\Omega \quad (6.14)$$

$$R_{OK3} = R_{OK_SUM} - R_{OK1} - R_{OK2} = 1.26 M\Omega \quad (6.15)$$

Thermal Shutdown

In order to protect the rechargeable battery from being damaged at high temperature, the BQ25504 utilizes an integrated temperature sensor to scan the junction temperature of the device. When the OT_PROG pin is connected to low, the temperature threshold is typically 65°C with a hysteresis of 5°C. If the temperature threshold is passed, then the boost charger is deactivated and charging stops until the temperature goes back to below the threshold.

6.3.2.2 Layout

In order to avoid unstable operation and electromagnetic interference problems in the power management circuit, the printer circuit board layout needs to be designed carefully.

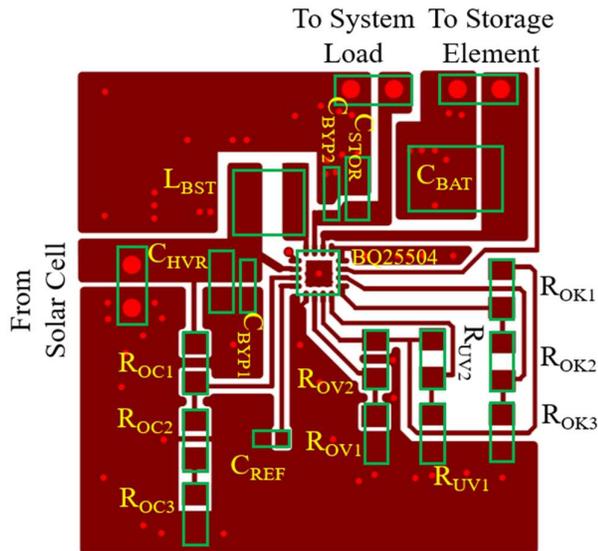


Figure 6.7: Layout of the designed power management unit (PMU) using BQ25504 IC.

All the input and output capacitors and inductors are placed as close as possible to the respective pins of the IC as seen in Figure 6.7. To reduce the impact of any noise on the voltage setting nodes with high impedance, the external resistors are also placed as close as possible to corresponding pins so that the shortest trace could be realized between the pin and the midpoint of the voltage divider. For the main current and

power ground paths, the traces are designed to be short and wide. Short traces are used for non-power ground paths as well. Figure 6.7 shows the designed layout of the PMU.

6.3.2.3 Selection of Storage Element

There are two major commercially available energy storage solutions for wireless energy harvesting sensors: batteries and supercapacitors. In a lot of cases, the lifetime of a sensor node depends on the storage element lifetime, therefore, it is important to choose the appropriate storage element.

A battery stores electrical energy in chemical form. In a battery, positive and negative terminals or electrodes are separated by the electrolyte. When a battery is connected to an electric circuit, the chemical reactions in the electrolyte cause a build-up of electrons at the negative electrode which then flow through the external circuit to the positive electrode. This process is reversible in a rechargeable battery. There can be various combinations of materials used for electrodes and electrolytes. Table 6.9 compares the characteristics of four most commonly used rechargeable batteries: lead acid, nickel-cadmium, nickel-metal, hydride and lithium-ion, in this case lithium manganese, batteries.

Table 6.9 A comparison of commonly used rechargeable batteries

Specifications	Lead Acid	Nickel-Cadmium	Nickel-metal-hydride	Lithium-Manganese
Specific Energy (Wh/kg)	30-50	45-80	62-120	100-150
Charge Time (hour)	8-16	1-2	2-4	1 or less
Cycle Life (80% discharge)	200-300	1000	300-500	500-1000
Self-Discharge/Month	5-15%	20%	30%	< 5%
Cell Voltage (V)	2	1.2	1.2	3-3.7
Discharge Cutoff Voltage	1.75	1	1	2.5-3
Internal Resistance (mΩ/V)	< 8.3	17-33	33-50	6.6-20
Coulombic Efficiency	~90 %	~70-90%	~70-90%	99%
Toxicity	High	High	Low	Low

The charge storage capability of a battery is called “battery capacity” and expressed as the product of time and current it can constantly supply during that duration. The specific energy is the essentially the battery capacity per unit mass. The lithium manganese battery has comparatively high specific energy of 100-150 Wh/kg which makes it ideal as a small-sized rechargeable storage element for a wireless sensor node. The internal resistance of a battery depends on the chemical and physical properties of the battery. A battery can be made of one or more cells. Therefore, a combination of cells is required in a battery with lower cell voltages. This can further increase the

internal resistance of the battery. Higher values of internal resistance in nickel-cadmium and nickel-metal-hydride batteries opposes the flow of current and reduce the coulombic efficiency, which indicates the ratio of output and input charges in a battery during discharging and charging. Due to low internal resistance of 6.6-20 m Ω /V, the lithium-manganese battery has the highest efficiency of 99%. This puts less stress on the battery and prolongs its cycle life which is determined by the numbers of charge-discharge cycles a battery can go through before it can no longer meet the required performance criteria. Table 6.9 shows that the nickel-cadmium and lithium-manganese batteries have the longest cycle life of 1000 times.

Due to electrochemical process in the battery even when it is not being used, it loses stored energy. This self-discharge depends on battery chemistry and temperature. Lithium-manganese batteries also have the advantage of low self-discharge rate of less than 5% per month. Therefore, considering all the characteristics, lithium ion battery is the best option from the available rechargeable batteries.

Capacitors are also being used as storage element in wireless sensor nodes. A capacitor consists two conductors separated by a dielectric material. When voltage is applied, an electric field is created between the conductors and positive and negative charges are collected on them and thus the capacitor stores energy using these static charges. A supercapacitor has conductors with bigger surface area and thinner electrolyte dielectric materials than a conventional capacitor and as a result, it can achieve greater capacitance value. Table 6.10 shows a comparison of typical supercapacitor and li-ion battery.

Table 6.10 A comparison of supercapacitor and battery

Specifications	Supercapacitor	Li-ion Battery
Voltage	2.3-2.7 V	3.-3.7 V
Charging Time	1-10 seconds	60 minutes or less
Discharge Time	Seconds	Hours
Discharge Characteristics	Linear: Reaches voltage threshold quickly, prevents full use of energy spectrum	Exponential: Steady voltage, 90-95% energy is delivered before reaching threshold voltage
Self-Discharge	50% in 30-40 days	Less than 5% in 30 days
Cycle Life	>500, 000	500-1000
Service Life	10-15 years	5-10 years
Specific Energy	1-10 Wh/kg	100-150 Wh/kg
Specific Power	1000-10,000 Wh/kg	1000-3000 Wh/kg
Charge Temperature	-40 to 65°C	0 to 45°C
Discharge Temperature	-40 to 65°C	-20 to 60°C
Cost per kWh	\$ 10,000	\$ 250 - \$ 1000

It can be seen from Table 6.10 that a supercapacitor has higher specific power of 1000-10000 Wh/kg compared to 1000-3000 Wh/kg of a li-ion battery. This makes it an ideal choice for burst-mode power delivery where high power is required within microseconds to minutes. It can also be charged 300 times faster than a li-ion battery and can go through approximately 500 times more charging-discharging cycles; and as a result, it has longer service life. However, it has lower specific energy of 1-10 Wh/kg compared to 100-150 Wh/kg in a battery. As the specification of an autonomous wireless sensor node requires long operation time, a rechargeable battery is more suitable due to its higher energy density. In addition, due to exponential discharge characteristics, a battery can retain the voltage steadily and delivers 90-95% of its stored charge before reaching the threshold voltage. On the other hand, a supercapacitor exhibits a linear discharge characteristic and therefore, quickly reaches the threshold voltage before delivering the stored energy. The higher self-discharge rate in a supercapacitor also makes it unsuitable for an autonomous operation of a wireless sensor node.

Thin-film battery is one of the emerging technologies for energy storage. Thin-film batteries can operate over a wide range of temperature and can also be charged faster than the li-ion batteries [6.45], [6.46]. These batteries are capable of supplying high continuous and pulsed currents, have low self-discharge rate of less than 5%, can go through 1,000-10,000 charging and discharging cycles and have long life-time of more than 10 years [6.45]. However, thin-film batteries suffer from low specific energy of 13-34 Wh/kg. The overall capacity of a battery is limited by the mass of electrolyte material [6.46]. Since the layer thickness cannot not be more than few micrometres [6.45], the total capacity is low. In addition, the thin-film batteries are still expensive. A number of companies have been commercializing solid-state thin film rechargeable batteries and the market is predicted to grow even more. With the capacity increased and price reduced, in future thin-film batteries will eventually be the best solution for storage elements in energy harvesting.

Considering the characteristics, a lithium-ion coin cell battery has been chosen as the storage element in the WSN. The rechargeable battery of choice is ML-614S/FN, a 3.0 V Manganese Lithium battery with a capacity of 3.4 mAh from Panasonic [6.47]. The battery has sufficient capacity for the specified operation and at the same time can

be charged with the solar cells under indoor light in a short period, which is very important for an autonomous WSN.

During reception and transmission, the transceiver requires 13-18 mA of current within 15 μ S causing a large and fast system load transient. This might cause the C_{STOR} capacitor to briefly discharge below the V_{BAT_UV} threshold. This results in BQ25504 switching off the PFET between V_{STOR} and V_{BAT} and turning off the booster charger. In some cases, the C_{STOR} capacitors may possibly discharge further and drop below the V_{STOR_CHGEN} threshold. This would cause BQ25504 to go in cold start. The battery has a 10 μ A discharge current which is not sufficient to meet this surge current requirements of the Si4440 radio transceiver in Si1062. Therefore, an external capacitance of 2000 μ F is used in parallel with the storage element to provide the necessary short-term, high power bursts for the transceiver. This solution can also be achieved by increasing C_{STOR} , but this would increase cold-start time.

6.3.3 A Study of the Performance of Solar Cells for Indoor Autonomous Wireless Sensor Node

6.3.3.1 Solar Cell Basic

A photovoltaic cell or solar cell is a device that converts light energy of a photon directly into electricity by the photovoltaic effect.

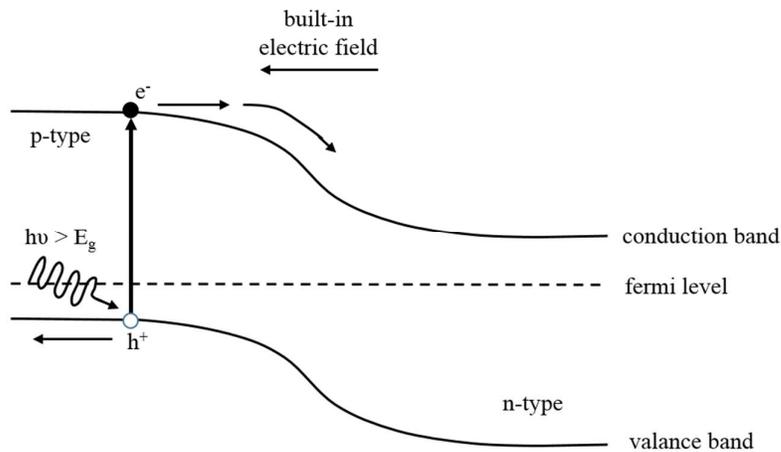


Figure 6.8: Band diagram of a p-n junction solar cell and the photovoltaic effect.

When light shines on a solar cell, the material which is usually semiconductor p-n junction absorbs some of the photons if the energy of the photon is equal or higher than its bandgap as shown in Figure 6.8. This raises electrons from valance band to higher energy state conduction band. If the electron-hole pairs are generated on the p-

type silicon of the solar cell and the electrons are diffused in the depletion region before recombining, then they are moved across to the n-type by the built-in electric field and kept it there. The presence of light and charge separation process creates excess electrons and holes on the n-type and p-type sides respectively which results in charge separation.

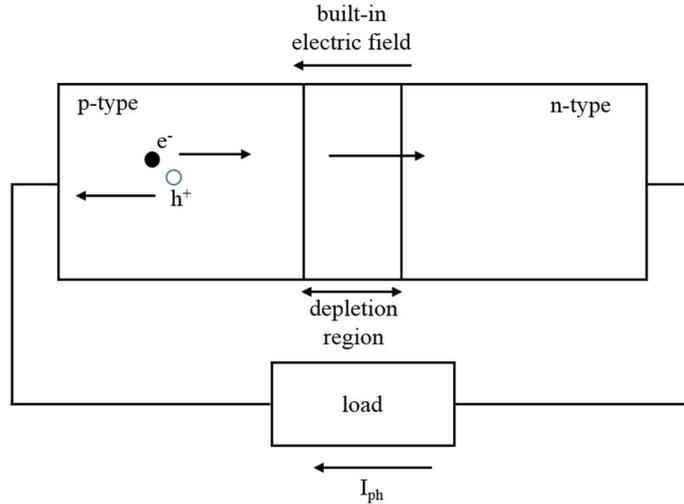


Figure 6.9: Conventional p-n junction solar cell.

Now if the p-type and n-type sides of the solar cell are connected via an external circuit as shown in Figure 6.9, then electrons travel through the circuit and power a load and reach the p-type semiconductor to recombine with holes. The generated current is called photo current (I_{ph}) and the light energy absorbed by the electron is used in powering the load.

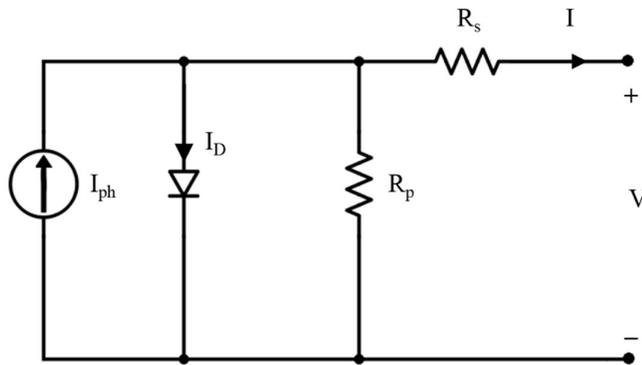


Figure 6.10: Equivalent circuit of a solar cell.

Figure 6.10 shows an equivalent electrical circuit of a solar cell represented by a current source connected in parallel with a diode, a series resistance (R_s) because of solar cells internal and contacts resistances and a parallel resistance (R_p) to represent the leakage of current in the solar cell.

The output current (I) can be defined by the Shockley solar cell equation (6.16):

$$I = I_{ph} - I_0 \left(e^{\frac{q(V+R_s I)}{nk_B T}} - 1 \right) - \frac{V + R_s I}{R_p} \quad (6.16)$$

In (6.16), the second term is the reverse diode current where I_0 is the saturation current of the diode in the dark, q is the electron charge (1.60×10^{-19} coulomb), V is the output voltage of the cell at the terminals, n is the diode ideality factor, k_B is the Boltzmann constant (1.38×10^{-23} m² kg s⁻² K⁻¹) and T is the ambient temperature in kelvin (K). In an ideal solar cell, $n = 1$, $R_s = 0$ and $R_p = \infty$.

The efficiency of a solar cell is the ratio of its electrical output power to its input power, which is the power of the incident light on the active area of the cell. The maximum efficiency of the solar cell ($\eta_{MAX, Solar Cell}$) can be obtained using (6.17):

$$\eta_{MAX, Solar Cell} = P_{MAX} / P_{IN} \quad (6.17)$$

In an energy harvester, the overall efficiency of the system depends on the solar cell and the power management unit. The efficiency of the power management unit (η_{PMU}) is obtained from the datasheet of the BQ25504 [6.39] and depends on its input voltage ($V_{IN, PMU}$) and current ($I_{IN, PMU}$) which corresponds to the $V_{MP, Solar Cell}$ and $I_{MP, Solar Cell}$ from the solar cell at its MPP. The overall system efficiency (η_{System}) is then calculated using (6.18):

$$\eta_{System} = \eta_{MAX, Solar Cell} \times \eta_{PMU} \quad (6.18)$$

6.3.3.2 Types of Solar Cells

Based on the materials used, solar cells can primarily be classified into two categories: silicon and non-silicon based technologies. Currently, silicon-based solar cell technology is accounted for more than 80% of the total production of commercial solar cells [6.48]. The remaining market is shared by technologies based on materials such as copper indium diselenide (CIS), copper indium gallium diselenide (CIGS) and cadmium telluride (CdTe). Emerging technologies such as organic, dye-sensitized, perovskite and group III-V solar cells are still under development. The following section briefly describes monocrystalline silicon, polycrystalline silicon, amorphous silicon, gallium arsenide, dye-sensitized and perovskite solar cell technologies that are studied for indoor energy harvesting for the designed wireless sensor node.

Crystalline Silicon Solar Cells

The majority of commercial silicon solar cells are single-crystal silicon wafers fabricated by the Czochralski method. The single crystal of silicon is usually very pure. In the monocrystalline or just crystalline silicon (c-Si) solar cell p-n junction is formed by boron doped p-type and phosphorous doped n-type regions. The lower installation cost, durability and longevity are the primary advantages of c-Si solar cells.

Polycrystalline Silicon Solar Cells

Large wafers with multiple silicon crystals or polycrystalline silicon (poly-Si) are fabricated using plasma-enhanced chemical vapour deposition where silicon is melted and then poured into a large mould. Compared to c-Si, poly-Si manufacturing process is less expensive, and has higher throughput. Like c-Si, poly-Si solar cells also have less impurities, but often defects are introduced by grain boundaries. Like c-Si, poly-Si solar cells also have the advantage of durability and longevity.

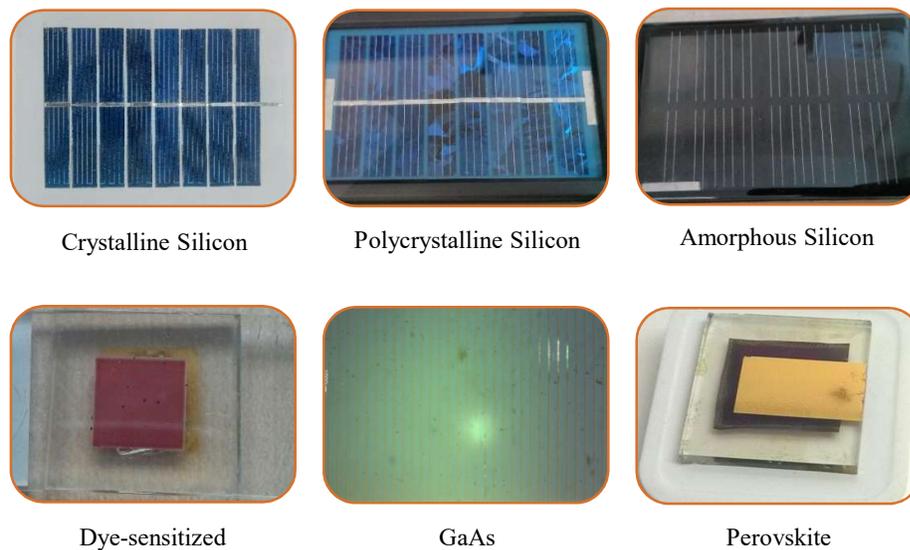


Figure 6.11: Photograph of six types of solar cell.

Amorphous Silicon Solar Cells

Amorphous silicon (a-Si) solar cell is one of the thin-film technologies. In a-Si, the silicon atoms do not follow a pattern and are randomly arranged. Many of the silicon atoms remain unpaired and as a result, they have dangling bonds. The a-Si has increased light absorption coefficient due to the disorder, but also suffers from high density of defects because of the dangling bonds. As a solution, Hydrogen atoms are

introduced in order to passivate these dangling bonds. Therefore, a-Si is basically an compound of silicon and hydrogen which is produced using chemical vapour deposition of gases containing silane (SiH_4). Another advantage is the relatively cheap mass production cost compared to crystalline silicon cells.

Gallium Arsenide Solar Cells

Gallium arsenide (GaAs) is a group III-V compound semiconductor material with a direct energy bandgap, excellent electron mobility and high light absorption coefficient. As a result, GaAs solar cells are highly efficient. Liquid encapsulated Czochralski or Bridgmann method is used to grow single crystals of GaAs. The high cost of raw materials and manufacturing is the major disadvantage of this technology.

Dye-Sensitized Solar Cells

The dye-sensitized solar cell (DSSC) is a non-silicon based emerging solar cell technology that offers a technically and economically reliable substitute to current p-n junction solar cells based on silicon due to its good efficiency and low manufacturing cost. A DSSC consists a light-absorbing dye with broad absorption band, typically based on ruthenium or osmium, on a wide band semiconductor material like titanium dioxide (TiO_2) nanoparticles. The charges are separated and injected from the dye into the conduction band of TiO_2 at the interface.

Perovskite Solar Cells

Perovskite solar cell is another emerging photovoltaic technology that showed very fast and significant improvement in efficiency over a very short period of time. It replaces the liquid in a DSSC with perovskite. The material and manufacturing costs are also cheap. A perovskite is a compound material that has the same crystallographic structure as the mineral named perovskite. The most effective perovskite solar cells produced so far have the following combination of materials in the generic perovskite form ABX_3 :

A: A positively charged organic atom such as methylammonium (CH_3NH_3^+)

B: A positively charged inorganic atoms such as lead (II) (Pb^{2+}) or tin (Sn^{2+}).

X_3 : A negatively charged smaller halogen atom such as chloride (Cl^-), boron (Br^-) or iodine (I^-).

The structure of the perovskite solar cell is same as that of DSSC.

6.3.3.3 Comparison of the Different Solar Cells Studied

The manufacturers only specify the solar cell efficiencies at outdoor condition and there has been very little study of these different solar cell technologies in indoor conditions. Figure 6.12 shows the external quantum efficiency (E.Q.E) for different solar cells under standard test condition (STC) with AM 1.5 or 1 sun spectrum and an intensity of 1000 W/m².

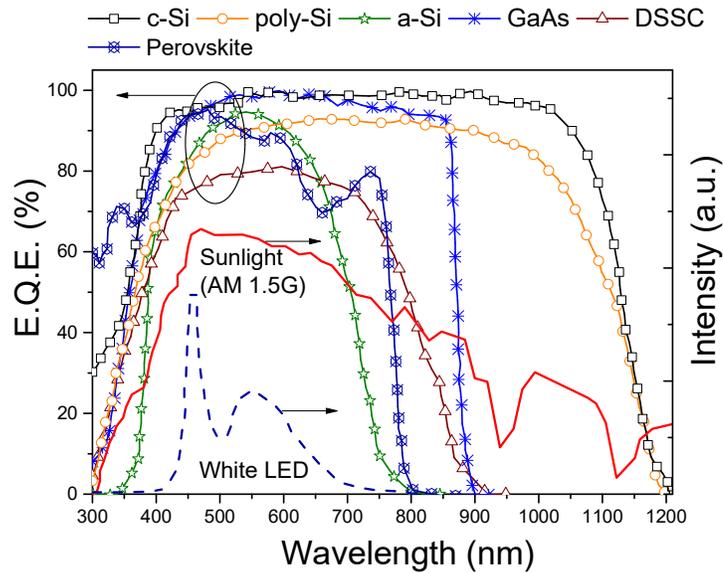


Figure 6.12: The external quantum efficiency of the six solar cells under outdoor solar spectrum (AM 1.5G) and illumination spectrum of the sun and white LED.

The E.Q.E. is the ratio of the number of electrons collected by the solar cell to the number of incident photons of a given energy on the solar cell. If the energy of the incident photon E_{ph} is less than the energy band gap E_g of the material ($E_{ph} < E_g$), then the photon is not collected by the solar cell and this results in non-absorption loss and the E.Q.E becomes zero. The entire spectrum of sunlight covers a range of electromagnetic radiation from 250 nanometres (nm) to 3200 nm and the corresponding photons have energy varying from 5 electron-volts (eV) to 0.4 electron-volts (eV). Since the energy band gap E_g of crystalline and polycrystalline solar cell is 1.1 eV [6.49], they absorb most of the photons in outdoor condition. Therefore, the E.Q.E of c-Si and poly-Si solar cells are close to maximum for a broad range of wavelengths.

As discussed in Section 6.3.3.1, the photons with energy E_{ph} larger than the bandgap E_g are absorbed by the solar cell and electron-hole pairs are generated. However, the extra energy $E_{ph}-E_g$ is lost by the excited electrons to the lattice atoms via a process called thermalization [6.50]. Therefore, in such cases, only a fraction of the total energy of the collected photons is converted into electricity. The cell efficiency, which can also be called as conversion efficiency, is given by the ratio of the electrical output power to the power of incident light. The cell efficiency is affected by this thermalization loss. This loss can be reduced if the emission spectrum of the light source and the absorption spectrum of the material of the solar cell, which depends on the energy band gap, match closely.

The human eye is sensitive to the electromagnetic radiation in the range of wavelengths from 390 nm to 700 nm and is typically most sensitive at 555 nm. The specific emission spectra of artificial light sources such as incandescent, compact fluorescent light bulbs and light emitting diode (LED) typically range from 400 nm to 700 nm and peak at different wavelengths. The cool white LED lamp has illumination wavelengths ranging from 400 nm to 750 nm and peaks at around 475 nm, which corresponds to the photons with the energy of 3.54 - 1.65 eV and 2.6 eV respectively. The cool white LED light is considered a very efficient artificial light source since its emission spectrum matches closely with the visible light spectrum.

The energy band gaps of GaAs, Perovskite and a-Si are 1.424 eV [6.49], 1.9 eV [6.2] and 1.55 eV [6.51] respectively. The spectral sensitivity or spectral response of these solar cells to cool white LED is more suitable since their absorption spectra match closely to the emission spectrum of this light compared to c-Si and poly-Si solar cells. Therefore, these solar cells would suffer less from thermalization loss under this light.

Beside external quantum efficiency and thermalization loss, the cell efficiency also strongly depends on the intensity of the light source. In standard test condition (STC), the solar cells are characterized under an intensity of 1000 W/m² or 100 mW/cm², whereas the typical intensity of indoor light sources is usually less than 0.1 mW/cm². The studies in [6.52], [6.53] show that the efficiency does not have a linear relationship with light intensity. The results demonstrate that the efficiency of crystalline silicon solar cells under the light intensity of 200-1000 W/m² differs very less from the maximum value. However, below the light intensity of 100 W/m², the efficiency decreases linearly. On the other hand, the efficiencies of GaAs, a-Si [6.53] and DSSC

[6.52] solar cells change only slightly for the whole range of intensity. Interestingly, the results in [6.52] in fact show that the efficiency of a-Si solar cells increases under lower intensity. According to the Shockley solar cell equation (6.16), lower value of series resistance R_s and higher value of parallel resistance R_p (Figure 6.10) result in higher output current from the solar cell, and consequently improve the efficiency. The authors in [6.50], [6.52] reported that under high light intensity, the series resistance R_s and at low light intensity, the parallel resistance have strong influence on the efficiency of the solar cells. These parameter values strongly depend on solar cell technologies and even manufactures. The a-Si solar cell naturally has high parallel resistance R_p [6.53], and therefore displays lowest decreases in efficiency under lower light intensity.

The solar cell efficiency clearly depends on the external quantum efficiency, thermalization loss, and emission spectrum and intensity of the light source. However, all the commercially available solar cells are characterized under standard test condition (STC) of AM 1.5 or 1 sun spectrum and 1000 W/m^2 light intensity; and unfortunately, no standard test condition exists for indoor condition since the emission spectrum and light intensity varies greatly depending on the light source and environment. The efficiency of a solar cell also varies with temperature. However, in indoor condition the temperature variation is typically small and its influence can be ignored. Therefore, the cell efficiency can be measured at room temperature. Amongst the various solar cell technologies, a comparison of commercially available solar panels of amorphous silicon (a-Si) and crystalline silicon (c-Si) technologies showed that a-Si solar panel has higher power density of $15 \mu\text{W/cm}^2$, outperforming its c-Si counterpart which has a power density of $9 \mu\text{W/cm}^2$ under indoor condition of 300 lux [6.54]. A comparison in [6.55] showed that a-Si solar cells have higher power density and efficiency than even early prototypes of dye-sensitized solar cells (DSSC) at low illuminance level of less than 300 lux. At 300 lux, both technologies showed a power density of $10 \mu\text{W/cm}^2$. Perovskite solar cells have the advantage of low cost compared to GaAs and Si technologies. The performance of perovskite solar cells evaluated in [6.2] shows that small-area cells (5.1 mm^2) display a maximum efficiency of 22.55 - 27.4% compared to 18.6 - 20.4% efficiency for large-area cells (5.4 cm^2) under 100-1000 lux. A comparison of DSSC and GaAs solar cells in [6.3] showed the latter to have higher power density of $25 \mu\text{W/cm}^2$ compared to DSSC ($5 \mu\text{W/cm}^2$) in indoor

conditions of 300 lux. Since the efficiency of a solar cell depends on the emission spectrum and intensity of the artificial light source, it is crucial that the solar cells are characterised in an environment similar to its intended application.

6.3.3.3.1 Experiment Setup

The wavelength of illumination from LED and fluorescent lamps ranges from 350 nm to 750 nm. The average of measured illuminance, using lux and power meters, in an indoor condition (i.e. an office) is about 330 lux or $60.79 \mu\text{W}$ respectively. The corresponding light intensity is calculated to be $77.40 \mu\text{W}/\text{cm}^2$.

Figure 6.13 shows the measurement setup designed to maintain a stable and constant light intensity of $77.40 \mu\text{W}/\text{cm}^2$ throughout the duration of the study. Inside the Brackenheath I1010W, a 10 W cool white LED, is used as the light source. Multiple black light filters are used to reduce the light intensity to the desired level of $77.40 \mu\text{W}/\text{cm}^2$ while the white wall of the cube reflects the light which allows to achieve uniformity.



Figure 6.13: Designed measurement setup with a controlled environment of $77.40 \mu\text{W}/\text{cm}^2$ light intensity using a 10 W cool white LED and light filters. The solar cell is located at the top centre.

The I-V characteristics of each of the solar cell panels are measured using a Keithley 4200-SCS under this controlled light intensity at room temperature, and corresponding current and power density are calculated.

6.3.3.3.2 Characteristics of the Solar Cells

Figure 6.14 shows the measured characteristics of the solar cells studied. The performance of the perovskite solar cell corresponding to light intensity of 330 lux is interpolated from the results in [6.2] under various light intensities ranging from 200 to 1000 lux.

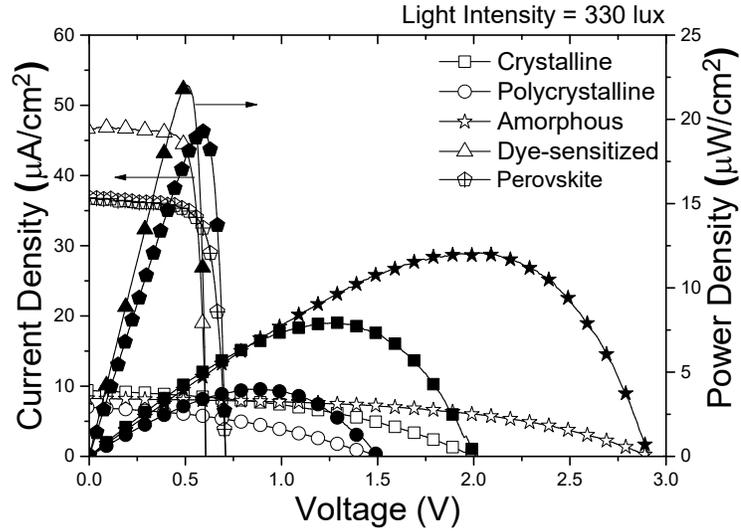


Figure 6.14: Measured solar cell characteristics under the controlled light intensity of $77.40 \mu\text{W}/\text{cm}^2$. The number of solar cells and total area of each panel are different and further described in Table 6.10.

Table 6.11 A comparison of properties and characteristics of the six solar cells studied.

Type of Solar Cell	No. of Cells in Panel	V_{oc} (V)	I_{sc} (μA)	Dimension (cm)		Area of Unit Cell (cm^2)	Total Area of Panel (cm^2)	Power Density at MPP ($\mu\text{W}/\text{cm}^2$)	Unit Efficiency (%)	System Efficiency (%)
c-Si	8	2.0	699.56	7.7	1.2	9.24	73.12	7.91	10.22	9.10
Poly-Si	8	1.5	319.07	5.6	1	5.6	44.8	3.99	5.16	4.54
a-Si	9	2.89	233.35	5.2	0.61	3.18	28.62	12.07	15.59	14.03
DSSC	4 (parallel)	0.6	194.41	1	1	1	4	22.0	28.42	22.74
GaAs [6.3]	1	0.90	-	-	-	8.55	8.55	26.07	28.03	24.10
Perovskite [6.2]	1	0.71	200.08	-	-	5.44	5.44	19.32	20.4	17.34

Table 6.11 summarizes the properties and measured results for the solar cells. It also compares the reported performances of perovskite and GaAs solar cells. The performance of DSSC is calculated from small area cells of 1 cm^2 each and since they

do not display the higher value of internal resistance observed in large-area cells, the efficiency is expected to be overestimated by about 10 - 15% compared to large-area cells. It can be observed that under the light intensity of $77.40 \mu\text{W}/\text{cm}^2$, the GaAs solar cell has the highest power density of $26.07 \mu\text{W}/\text{cm}^2$, followed by DSSC and perovskite and then a-Si. The c-Si and poly-Si solar cells, although show the highest values of external quantum efficiencies under outdoor solar spectrum (Figure 6.12), display the poorest performance in indoor condition due to thermalization loss, spectral mismatch with white LED and decrease in efficiency under low light intensity as discussed in section 6.3.3.3.

The results show that in indoor condition, DSSC and GaAs solar cells are comparable and are currently the best technologies to achieve desired harvested power required for the operation of an autonomous wireless sensor node utilizing minimum area due to their high-power densities. The material and manufacturing cost of GaAs solar cell is significantly higher than DSSCs and perovskite solar cells. The range of power densities of DSSC in different studies indicate that as a technology DSSC still has not matured yet. The perovskite solar cell technology is also developing at a very fast rate. Therefore, it can be concluded that considering performance and cost, DSSC and perovskite solar cells are the best choice for indoor light energy harvesting.

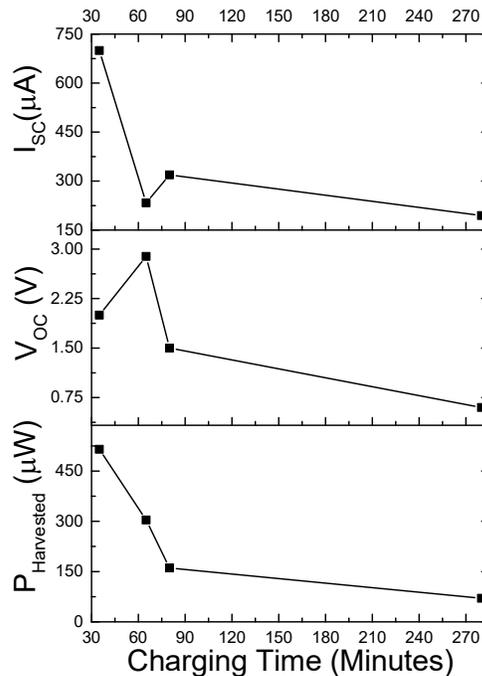


Figure 6.15: The relationships between battery charging time and open circuit voltage, short-circuit current and harvested power by the power management system from the solar cells. As expected the charging time strongly depends on the harvested power.

Figure 6.15 shows the charging characteristics of the rechargeable battery as function of open-circuit voltage (V_{OC}), short-circuit current (I_{SC}) and harvested power ($P_{Harvested}$). As expected, the solar cell panel which has the maximum harvested power charges the battery fastest from a nominal voltage of 2.8 V to 3.0 V. However, the voltage and current at the MPP are also relevant since the efficiency of the power management system depends on $V_{IN, PMU}$ and $I_{IN, PMU}$. For the power management system in this WSN, the efficiency is nearly independent above $V_{IN, PMU} = 1.8$ V and $I_{IN, PMU} = 200$ μ A.

It can be noted from Figure 6.15 that for a reasonable charging time of 60 minutes, an average harvested power of 300 μ W is required. Considering a power management unit efficiency (η_{PMU}) of 90%, the power from the solar cell at its input needs to be 333 μ W. The total active area required for the solar cell panel using DSSC, which is the best choice in indoor condition, is 333 μ W / (22 μ W/cm²) or 15 cm². In order to achieve a system efficiency of 90%, the possible best arrangement is achieved when three DSSCs of 5 cm \times 1 cm area are connected in series to obtain I_{SC} of 243 μ A and V_{OC} of 1.8 V.

6.3.4 Wake-up Receiver

In a WSN, the transceiver or radio unit consumes the highest amount of power in operation. If the data traffic is low, then the power consumed by this unused hardware during the idle time can become significant. Table 6.12 shows the current consumption of the transceiver in Si1062 in various modes of operation.

Table 6.12 Current Consumption and Duration of Various Operation Modes in

Operation Mode	Current	Duration
Transmit	13 mA	15 msec
Receive	18 mA	10 msec
Ready state	1.8 mA	3599.9 sec
Shut down	30 nA	3599.9 sec

Considering the supply voltage of 3 V and three transmission and reception per hour, the energy consumption per day for each of these operation modes can be calculated.

$$Tx \text{ energy per day} = 13mA \times 3V \times 15ms \times 3 \times 24 = 0.04212J \quad (6.19)$$

$$Rx \text{ energy per day} = 18mA \times 3V \times 15ms \times 3 \times 24 = 0.0583J \quad (6.20)$$

$$Ready \text{ mode energy per day} = 1.8mA \times 3V \times 3599.9s \times 24 = 466.5J \quad (6.21)$$

$$Shutdown \text{ mode energy per day} = 30nA \times 3V \times 3599.9s \times 24 = 0.0078J \quad (6.22)$$

It is observed that if the radio unit is in a ready state at all times, then the transceiver in Si1062 requires 1.8 mA current compared to shut down mode current of just 30 nA [6.29]. In such a case, while idle, the radio unit consumes 466.5 Ws or joules in one day. This is even higher than the combined energy consumption for transmission and reception. Such high energy consumption would prevent the WSN to operate autonomously with limited energy; and for this reason, the development kit supplied by Silicon Labs [6.37] uses two 1.5 V AA batteries with 2300 mAh - 2850 mAh capacity, mini USB connector or an external power supply to operate. Since the power consuming components are only required to be active for a short period, the average power consumption of the transceiver, and consequently the WSN can be reduced significantly if they are put into sleep mode during idle time.

Duty cycling has been a popular and energy efficient choice to utilize this low activity rate compared to always-on mode. The WSN periodically changes its state between active and sleep modes. Once in active mode, the MCU executes the commands and performs its task, sends the data and subsequently goes back to low power sleep mode and the radio unit is completely shut down. For example: the smart clock (RTC) in Si1062 can be used as a timer to wake-up the MCU in a particular interval. In duty-cycling technique if the neighbouring nodes in the network are not properly synchronized, then the receiver node might still be in sleep mode when the sender node is ready. In such a case, the sender node should wait until the receiver node wakes up to forward the data packet. In high duty-cycle, this might create the problem of increased latency in data transmission.

Implementing a wake-up receiver (WuR) can resolve this problem. The WuR is an asynchronous method that uses a dedicated circuit that constantly listens to the wireless channel. If a wake-up signal is detected by the WuR, then it quickly wakes the MCU up from sleep mode which then powers up the radio unit for data reception and transmission. This helps to overcome the problem of latency in duty cycle. Since the WuR is always on while the rest of the WSN is in sleep mode, its power consumption should be extremely low so that overall power consumption of the WSN does not increase significantly with the inclusion of a WUR.

There are mainly two categories of WuR: passive and active wake-up receivers. As the names suggest, an active wake-up receiver has some active components such as low-noise amplifier (LNA), local oscillator (LO) in the circuit. It has the advantage of

longer operating range, but at the same time consumes more power than a passive wake-up receiver which suffers from shorter operating range of less than two meters.

The reported wake-up receivers use either Frequency Shift Keying (FSK) [6.56] or On-Off Keying (OOK) [6.57] modulation schemes as they can be easily demodulated. However, the WuR receivers designed for FSK signal suffers from the disadvantage of high power consumption since they use frequency synthesizer such as a local oscillator compared to the envelope detectors in WuR designed for OOK signal. The power consumption of the WuR in [6.56] is 126 μW , whereas it is just 51 μW [6.57] for a WUR using OOK signal. It must be mentioned that the WuR in [6.57] uses a low-noise amplifier (LNA) to improve the sensitivity of the WuR. The power consumption can be reduced even further by using only passive elements. Therefore, in order to design a low power autonomous WSN, a passive wake-up receiver using OOK modulation scheme is implemented in this work.

6.3.4.1 Design and Implementation

The WuR is designed primarily based on the designs described in [6.58], [6.59]. There are mainly two differences between this design and the one presented in [6.58]. Firstly, this design implements a two-stage voltage multiplier instead of a four-stage voltage multiplier. Secondly, in place of a voltage divider consisting two resistors to determine the threshold voltage of the comparator, the WuR in this work incorporated the adaptive threshold generator from the design presented in [6.59]. The major difference between WuR design in this work and the one in [6.59] is that the latter has the capability to process Media Access Control (MAC) data communication protocol which is an addressing mechanism. This feature enables a wake-up signal to wake up a particular node in a wireless sensor network with multiple nodes. It can considerably reduce the interruption from other communications.

The WuR uses mostly passive elements to achieve low power consumption. Figure 6.16 shows the three blocks of the designed WuR: the matching network, 2-stage voltage multiplier that acts as an envelope detector, an adaptive threshold generator and a digital comparator.

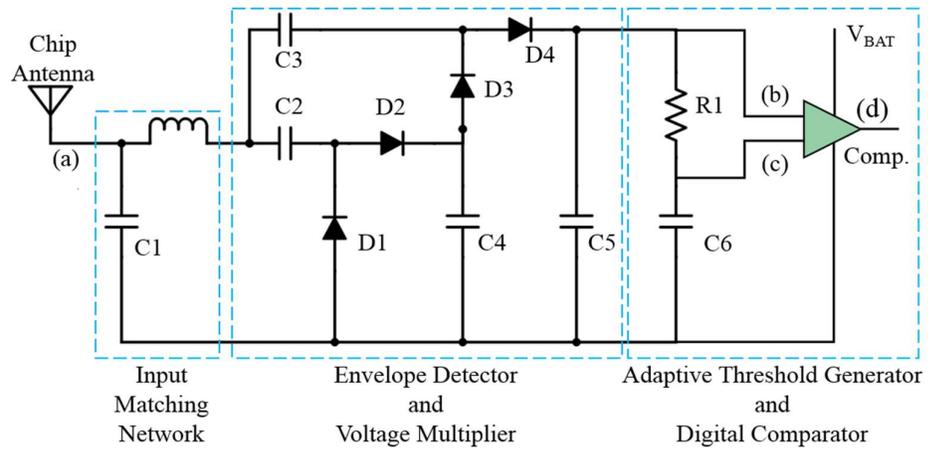


Figure 6.16: The schematic diagram and block diagram of the wake-up receiver.

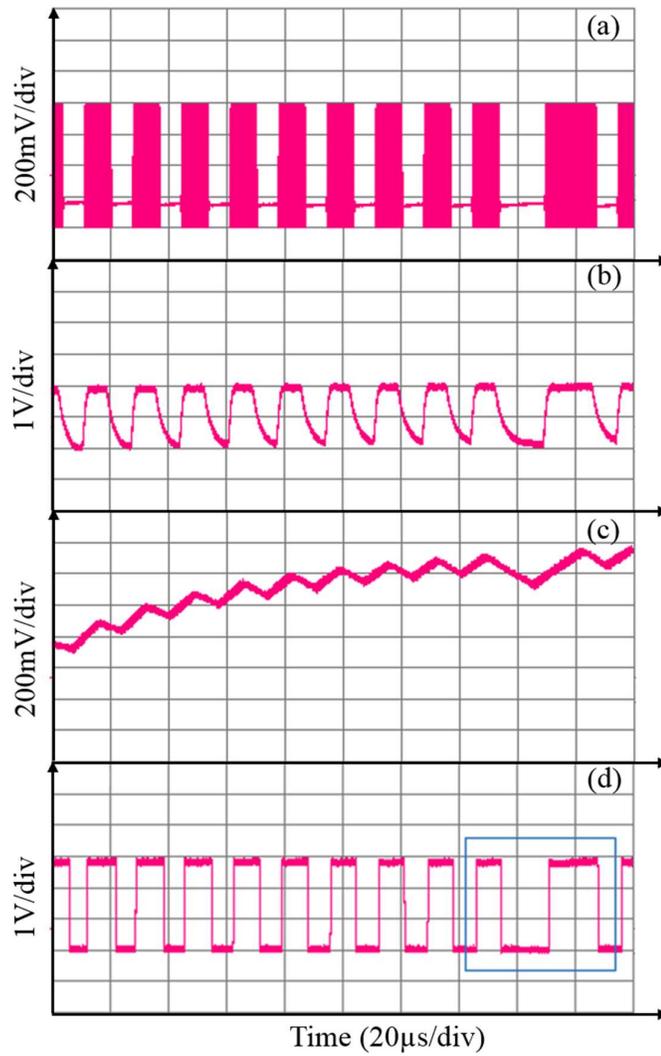


Figure 6.17: Measured (a) Input OOK signal. (b) Output from the envelop detector. (c) Adaptive threshold voltage. (d) PWM output from the comparator captured in oscilloscope.

Input Matching Network

The wake-up signal in on-off keying (OOK) modulation received by the antenna is shown in Figure 6.17 (a). The first part of the WuR circuit after the antenna is the input matching network. It matches the impedance of the rest of the circuit to the 50 Ω chip antenna to transfer maximum power of the received signal to the next stage of the WuR. The matching network is designed using two reactive elements: a series inductor (L1) and a parallel capacitor (C1).

Envelope Detector and Voltage Multiplier

The strength of the received signal is usually very weak because of the path loss during radio wave transmission. Therefore, the next part of the WuR is a two-stage voltage multiplier consisting the capacitors C2-C5 and the diodes D1-D4. It also acts as an envelope detector to extract the low frequency envelope from the received high frequency OOK signal. The RF Schottky diodes HSMS-2852 from Avago Technologies [6.60] are used as these have very low threshold voltage and are able to operate at high frequencies. The output of this part of the circuit can be seen in Figure 6.17 (b).

Adaptive Threshold Generator and Digital Comparator

The last part of the circuit consists an adaptive threshold generator (R1 and C6) and a digital comparator. The implementation of adaptive threshold technique has two benefits:

1. Rather than being fixed, the value of the threshold voltage for the comparator changes based on the strength of the signal received at (a). This increases the dynamic range of the WuR.
2. It uses the energy from the antenna for its operation which reduces the power consumption.

The output from the adaptive threshold generator is shown in Figure 6.17 (c). The maximum value is 50% of the signal level at (b). The comparator converts the analog signal into a digital signal with appropriate voltage levels corresponding to the “high” and “low” logical levels of the MCU. The output from the comparator which is the final output from the WuR is a pulse width modulated (PWM) signal as shown in Figure 6.17 (d). The nano-power comparator TS881 from ST Microelectronics [6.61]

is the only active component in the WuR circuit and it typically requires 210 nA current to operate.

The wake-up signal is an OOK modulated signal with a data rate of 120 kbps. The PWM signal from the comparator output has a period of 8.33 μs . When there is an active low at the reset pin on the transceiver for more than 15 μs as it can be seen in Figure 6.18, the WSN wakes up from its sleep.

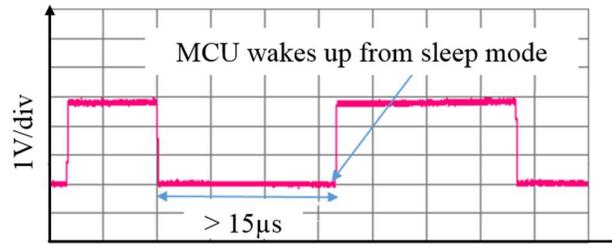


Figure 6.18: Measured PWM output from the comparator captured in oscilloscope.

6.3.4.2 Energy Consumption of the WSN

Figure 6.19 shows a measured current pulse profile of the MCU and radio transceiver in the WSN during its operation. The current consumption for each step is calculated by multiplying current and time interval. After waking-up (A), the MCU “active mode” is initialized to execute the commands (B). After that the radio goes in to “ready state” (C) and then transmits the packet (D). Finally, the MCU shuts down the peripherals (E) and goes back to sleep.

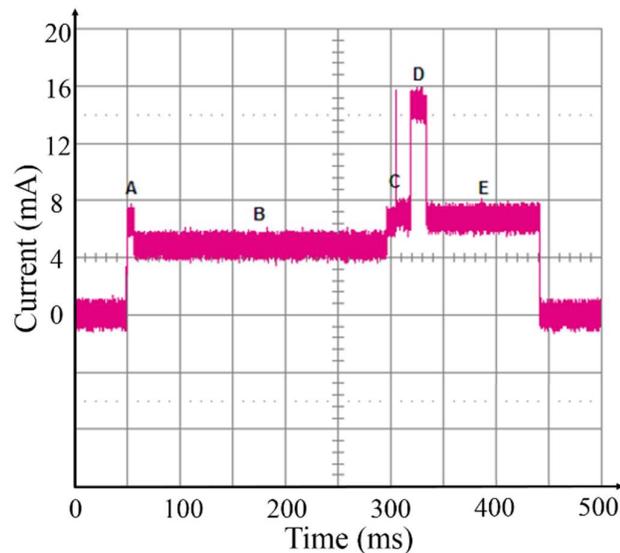


Figure 6.19: Measured current consumption of the MCU and radio transceiver in the autonomous WSN captured in oscilloscope.

The total current consumption ($I_{\text{Execution}}$) during application execution time ($T_{\text{Execution}}$) of 386 ms is 2.25 mAs. If a wake-up signal is sent after a time period (T_{period}), the total current consumption in sleep mode ($I_{\text{Total Sleep Mode Current}}$) can be calculated using (6.23) where $I_{\text{Sleep Mode}}$ is the combined sleep mode current for MCU and WuR:

$$I_{\text{Total Sleep Mode}} = I_{\text{Sleep Mode}} \times (T_{\text{Period}} - T_{\text{Execution}}) \quad (6.23)$$

For a period of 20 minutes, the total current consumption in sleep mode is 1.21 mAs. Now the average current consumption for WSN can be calculated using (6.24).

$$I_{\text{Average}} = (I_{\text{Total Sleep Mode}} + I_{\text{Execution}}) / T_{\text{Period}} \quad (6.24)$$

The power management system disconnects the battery from the load when the nominal voltages drops to 2.6 V which corresponds to 0.8 mAh of the battery capacity. For an average current consumption of 2.88 μA , the hours of operation without any energy harvesting can be estimated using (6.25).

$$\text{Hours of operation} = \text{Battery Capacity} / I_{\text{Average}} \quad (6.25)$$

Without any input from the solar cell, the WSN can operate for 277 hours or can complete 833 transmissions.

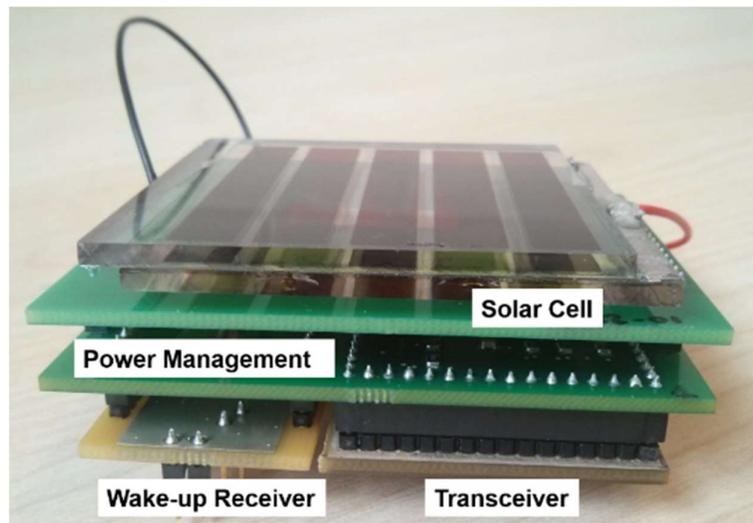


Figure 6.20: Photograph of the prototype wireless sensor node.

The performance of the WSN on this work is summarized in Table 6.13 and compared with commercial WSN from Cymbet Corporation [6.62]. The WSN in this design has lower current consumption in both active and sleep modes. In addition, it also has longer range and wider bandwidth.

Table 6.13 A summary of autonomous wireless sensor node performance

	Cymbet	This Work
Sleep Mode Current	1100 nA	800 nA
Sleep Mode Current with Wake-Up Receiver	No Wake-Up Receiver	1010 nA
Active Mode Current	270 μ A / MHz	160 μ A / MHz
Maximum Output Power	+1 dBm	+20 dBm
Sensitivity	-104 dBm	-126 dBm
Range	<1 meter	>2 meters
Bandwidth	83.5 MHz	908 MHz
Battery Capacity	100 μ Ah	3.4 mAh
Area of Solar Cell	32.94 cm ²	15 cm ²
Operation without Solar Cell Input	Total 25 transmissions before reaching battery cut-off voltage of 3.3 V (3.8 V Battery)	Total 833 transmissions before reaching battery cut-off voltage of 2.6 V (3.0 V Battery)

However, it can be noted in Table 6.13 that the operational range of the wireless sensor node is around 2 meters, which is significantly less than the range that would be achieved considering the transmitted power of +20 dBm and receiver sensitivity of -126 dBm. The receiver sensitivity $P_{\text{sensitivity}}$ is the lowest signal power level at which the receiver can detect an RF signal and demodulate the data to obtain the useful information. Therefore, the received power should be always greater than the receiver sensitivity. The Friis Transmission Formula [6.63] which describes the relationship between the transmitted and received power in free space can be written as [6.64]:

$$P_r = P_t G_t G_r \left(\frac{\lambda}{4\pi R} \right)^2 \quad (6.26)$$

In (6.26), P_r is the received power, P_t is the transmitted power, and G_t and G_r are transmitter and receiver antenna gains respectively. The term $(\lambda/4\pi R)^2$ represents the path loss, where λ is the wavelength of the signal and R is the range or distance between the transmitter and receiver. The path loss is caused by the free space loss. As the transmitted signal propagates, it attenuates or becomes weaker with increasing distance between transmitter and receiver, and consequently it becomes more difficult for a receiver to detect the signal.

However, the free space loss alone cannot represent a realistic situation. In real-world, there are system losses at the transmitter and receiver due to insertion loss in the transmission line and any loss due to an impedance mismatch with the antenna. In addition, losses are also introduced by the interaction between the electromagnetic signal and environment and there might not be a clear line-of-sight path for

propagation. The range can also be degraded by other unpredictable factors. Therefore, designers usually consider additional and temporary path losses or signal fading called fade margin which can be tolerated before system performance is impacted. Therefore, taking total system loss L_{sys} and fade margin F_M into account for a realistic situation [6.65], (6.26) can be written as:

$$P_r = \frac{P_t G_t G_r}{F_M L_{\text{sys}}} \left(\frac{\lambda}{4\pi R} \right)^2 \quad (6.27)$$

The maximum range can be calculated by rewriting (6.27) as the following equation by considering the receiver sensitivity:

$$R_{\text{max}} = \sqrt{\frac{P_t G_t G_r \lambda^2}{P_{\text{sensitivity}} F_M L_{\text{sys}} (4\pi)^2}} \quad (6.28)$$

Since, $\lambda = c/f$ where c is the speed of light and f is the frequency of the signal, (6.28) can be expressed as:

$$R_{\text{max}} (\text{meters}) = 10^{\frac{P_t(\text{dBm}) + G_t(\text{dBi}) + G_r(\text{dBi}) - P_{\text{sensitivity}}(\text{dBm}) - F_M(\text{dBm}) - L_{\text{sys}}(\text{dBm}) - 27.55 + 20 \log_{10}(f)}{20}} \quad (6.29)$$

It can be seen from (6.29) that the maximum range can be improved by increasing the transmitted power, transmitter and receiver antenna gains and receiver sensitivity; and also by reducing fade margin and losses. For given transmitted power, antenna gains, receiver sensitivity, path loss and no fade margin considered; the maximum range depends on the system loss which is generally associated with losses at the transmitter and receiver due to insertion loss in the transmission line and any loss due to an impedance mismatch with the antenna. Figure 6.21 shows the measured return loss of the impedance matching circuit of the wake-up receiver.

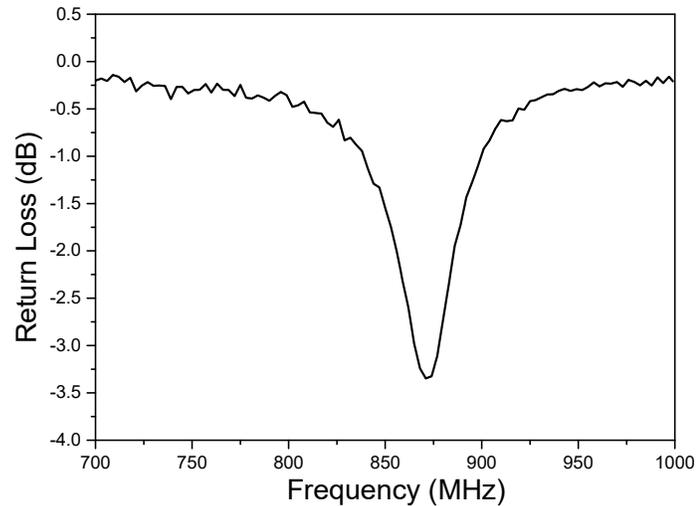


Figure 6.21: Measured input return loss of the impedance matching circuit of the wake-up receiver.

The high return loss of 3.24 dB at the frequency of 868 MHz indicates a mismatch of impedances between the 50 Ω chip antenna and the wake-up receiver which has an impedance of $(2.54 - j*40.22) \Omega$. This impedance mismatch leads to mismatch loss. The most commonly stated indicator of impedance mismatch in the datasheet of an antenna is the voltage standing wave ratio (VSWR). A perfect match, although never obtainable, would have a VSWR of 1:1. While a VSWR of less than 1.5:1 is desirable, a VSWR of 2:1 is usually the standard for an antenna to display acceptable performance [6.38]. For the designed wake-up receiver, the corresponding VSWR for the return loss of 3.24 dB is 5.424:1, and this high return loss or VSWR leads to significant mismatch loss. The value of reflected power due to mismatch can be calculated using the following equation:

$$\text{Reflected Power (\%)} = 100 \times \Gamma^2 \quad (6.30)$$

$$\text{Where, Reflection Coefficient } \Gamma = 10^{(-\text{Return Loss} / 20)} \quad (6.31)$$

For the return loss of 3.24 dB, 45.47% power of the incident signal is reflected and 54.53% is transferred from the antenna to the wake-up receiver. This inefficiency causes high system loss, and consequently, the maximum range is decreased. In other words, since the received power can be expressed as:

$$P_r(\text{dBm}) = P_t(\text{dBm}) + G_t(\text{dBi}) + G_r(\text{dBi}) - F_M(\text{dBm}) - L_{\text{path}}(\text{dBm}) - L_{\text{sys}}(\text{dBm}) \quad (6.32)$$

Therefore, the received power decreases when the losses increase. However, the condition $P_r > P_{\text{sensitivity}}$ must be satisfied for the wake-up receiver to produce useful output signal. Hence, to increase the received power, the distance between transmitter and receiver is reduced to decrease the path loss to compensate for the higher system loss.

Therefore, to improve the range of the wireless sensor node, the input matching network of the wake-up receiver should be improved to reduce the return loss to less than 9.54 dB to achieve a VSWR of 2:1 or less. The matching network is designed using transmission lines and discrete components such as series inductor and shunt capacitor. The wake-up receiver also consists components such as diodes, capacitors, resistors, comparator and transmission lines which are within proximity due to the compact design. This might lead to unintended electromagnetic coupling between the circuit elements and thus introduce coupling induced mismatch. Therefore, three-

dimensional (3D) electromagnetic (EM) simulations should be performed to design and optimize the matching network, as well as the physical layout of the wake-up receiver if necessary. Although manufacturer models for the discrete components have been used in ADS for designing the matching network, the impact of component tolerances on the performance has not been evaluated. In future design, this effect should also be considered. In addition, designing the matching network using transmission lines by replacing the inductor and capacitor can also be considered to avoid the loss and parasitic effects associated with the discrete components. Future designs should also include a fade margin to avoid the effects of unpredicted and temporary losses and allow the wireless sensor node to maintain the desired range through its operation.

6.4 Summary

In this chapter, a comprehensive comparison of six different solar cell technologies for indoor light energy harvesting under a controlled light intensity of 330 lux, which corresponds to typical office illumination, is presented. The results show that DSSC and GaAs solar cells exhibit similar performances in indoor condition. However, considering the material and manufacturing cost DSSC and perovskite solar cells are the best options for designing an autonomous wireless sensor node. A 3.0 V Magnesium Lithium rechargeable battery with a capacity of 3.4 mAh and an external capacitor of 2000 μF in parallel are used as the energy storage elements. The design and implementation of an autonomous WSN, which has an average power consumption of 8.64 μW for a period of 20 minutes is described. Without any input from the solar cell, the WSN can transmit 833 times before reaching the battery cut-off voltage of 2.6 V. A DSSC solar cell panel with the area requirement of 15 cm^2 and the power management system can harvest adequate energy with excellent efficiency for the autonomous operation of the WSN from under indoor light intensity of 77.40 $\mu\text{W}/\text{cm}^2$. The area of the WSN can be further reduced in future prototypes by designing the MCU and WuR on the same printed circuit board and by using single chip antenna for the transceiver and the WuR. The range of the wireless sensor node can also be extended by improving the matching network of the wake-up receiver.

References

- [6.1] Silicon. Laboratories, Inc., “The Evolution of Wireless Sensor Networks,” White Paper, 2013.
- [6.2] C. Y. Chen, J. H. Chang, K. M. Chiang, H. L. Lin, S. Y. Hsiao, and H. W. Lin, “Perovskite Photovoltaics for Dim-Light Applications,” *Advanced Functional Materials*, pp. 7064–7070, 2015.
- [6.3] I. Mathews, G. Kelly, P. J. King and R. Frizzell, “GaAs solar cells for Indoor Light Harvesting,” *2014 IEEE 40th Photovoltaic Specialist Conference (PVSC)*, Denver, CO, 2014, pp. 0510-0513.
- [6.4] V. Rajendran, K. Obraczka and J. Garcia-Luna-Aceves, “Energy-efficient collision-free medium access control for wireless sensor networks”, in *Proceedings of the first ACM Conference on Embedded Networked Sensor Systems (SenSys)*, 2003.
- [6.5] C. Schurgers and M.B. Srivastava, “Energy efficient routing in wireless sensor networks”, in *Proceedings of IEEE Military Communications Conference (MILCOM)*, vol. 1, pp. 357-361, 2001.
- [6.6] S. Lindsey and C. S. Raghavendra, “PEGASIS: Power-efficient gathering in sensor information systems,” *2002 IEEE Aerospace Conference Proceedings*, 2002, pp. 3-1125-3-1130 vol.3.
- [6.7] C. Schurgers, V. Tsiatsis and M. B. Srivastava, “STEM: Topology management for energy efficient sensor networks,” *2002 IEEE Aerospace Conference Proceedings*, 2002, pp. 3-1099-3-1108 vol.3.
- [6.8] S. Sudevalayam and P. Kulkarni, “Energy Harvesting Sensor Nodes: Survey and Implications,” in *IEEE Communications Surveys & Tutorials*, vol. 13, no. 3, pp. 443-461, Third Quarter 2011.
- [6.9] S. Roundy, P. K. Wright, and J. Rabaey, “A study of low level vibrations as a power source for wireless sensor nodes,” *Computer Communications*, vol. 26, no. 11, pp. 1131–1144, 2003.
- [6.10] C. B. Williams and R. B. Yates, “Analysis Of A Micro-electric Generator For Microsystems,” in *Proceedings of the 8th International Conference on Solid-State Sensors and Actuators Eurosensors IX, Sensors and Actuators A: Physical*, Volume 52, Issues 1–3, March–April 1996, Pages 8-11.

- [6.11] R. N. Torah, M. J. Tudor, K. Patel, I. N. Garcia and S. P. Beeby, "Autonomous Low Power Microsystem Powered by Vibration Energy Harvesting," *2007 IEEE Sensors*, Atlanta, GA, 2007, pp. 264-267.
- [6.12] R. Amirtharajah and A. P. Chandrakasan, "Self-powered signal processing using vibration-based power generation," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 5, pp. 687–695, 1998.
- [6.13] H. Bottner, J. Nurnus, A. Gavrikov, G. Kuhner, M. Jagle, C. Kunzel, D. Eberhard, G. Plescher, A. Schubert, and K.-H. Schlereth, "New thermoelectric components using microsystem technologies," in *Journal of Microelectromechanical Systems*, vol. 13, no. 3, pp. 414-420, June 2004.
- [6.14] J. P. Carmo, L. M. Goncalves, and J. H. Correia, "Thermoelectric microconverter for energy harvesting systems," in *IEEE Transactions on Industrial Electronics*, vol. 57, no. 3, pp. 861–867, March 2010.
- [6.15] M. Piñuela, P. D. Mitcheson and S. Lucyszyn, "Ambient RF Energy Harvesting in Urban and Semi-Urban Environments," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 7, pp. 2715-2726, July 2013.
- [6.16] P. Nintanavongsa, U. Muncuk, D. R. Lewis and K. R. Chowdhury, "Design Optimization and Implementation for RF Energy Harvesting Circuits," in *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 2, no. 1, pp. 24-33, March 2012.
- [6.17] T. Le, K. Mayaram and T. Fiez, "Efficient Far-Field Radio Frequency Energy Harvesting for Passively Powered Sensor Networks," in *IEEE Journal of Solid-State Circuits*, vol. 43, no. 5, pp. 1287-1302, May 2008.
- [6.18] H. Jabbar, Y. S. Song and T. T. Jeong, "RF energy harvesting system and circuits for charging of mobile devices," in *IEEE Transactions on Consumer Electronics*, vol. 56, no. 1, pp. 247-253, February 2010.
- [6.19] D. Carli, D. Brunelli, D. Bertozzi, and L. Benini, "A high-efficiency wind-flow energy harvester using micro turbine," *2010 International Symposium on Power Electronics Electrical Drives Automation and Motion (SPEEDAM)*, pp. 778–783, June 2010.

- [6.20] C. Park and P. Chou, “AmbiMax: Autonomous Energy Harvesting Platform for Multi-Supply Wireless Sensor Nodes”, *3rd Annual IEEE Communications Society on Sensor and Ad Hoc Communications and Networks*, vol. 1, pp. 168-177, Sept. 2006.
- [6.21] M. Weimer, T. Paing and R. Zane, “Remote Area Wind Energy Harvesting for Low-power Autonomous Sensors”, *37th IEEE Power Electronics Specialists Conference*, pp. 1-5, 2006.
- [6.22] D. Brunelli, L. Benini, C. Moser and L. Thiele, “An Efficient Solar Energy Harvester for Wireless Sensor Nodes,” *2008 Design, Automation and Test in Europe*, Munich, 2008, pp. 104-109.
- [6.23] V. Raghunathan, A. Kansal, J. Hsu, J. Friedman, and M. Srivastava, “Design considerations for solar energy harvesting wireless embedded systems,” in *the Proceedings of the Fourth International Symposium on Information Processing in Sensor Networks*, 2005 (IPSN'05), pp. 457–462, 2005.
- [6.24] R. J. M. Vullers, R. van Schaijk, I. Doms, C. Van Hoof, and R. Mertens, “Micropower energy harvesting,” *Solid-State. Electronics*, vol. 53, no. 7, pp. 684–693, 2009.
- [6.25] L. Huang, V. Pop, R. de Francisco, R. Vullers, G. Dolmans, H. de Groot, and K. Imamura, “Ultra low power wireless and energy harvesting technologies — An ideal combination,” *2010 IEEE International Conference on Communication Systems (ICCS)*, Singapore, 2010, pp. 295-300.
- [6.26] H. Yu and Q. Yue, “Indoor Light Energy Harvesting System for Energy-aware Wireless Sensor Node,” *2012 International Conference on Future Energy, Environment, and Materials, Energy Procedia*, vol. 16, pp. 1027–1032, 2012.
- [6.27] A. S. Weddell, N. R. Harris, and N. M. White, “An Efficient Indoor Photovoltaic Power Harvesting System for Energy-Aware Wireless Sensor Nodes,” *Euroensors 2008*, Dresden, 2008.
- [6.28] Y. K. Tan and S. K. Panda, “Energy Harvesting From Hybrid Indoor Ambient Light and Thermal Energy Sources for Enhanced Performance of Wireless Sensor Nodes,” in *IEEE Transactions on Industrial Electronics*, vol. 58, no. 9, pp. 4424-4435, Sept. 2011.

- [6.29] Silicon Laboratories, Inc., “Si106x/108x Ultra-Low Power MCU with Integrated High-Performance Sub-1 GHz Transceiver,” 2014.
- [6.30] Texas Instruments, “CC1310 SimpleLink™ Ultralow Power Sub-1-GHz Wireless MCU,” 2015.
- [6.31] Freescale Semiconductor, “MC12311 Highly-integrated, cost-effective single-package solution for the sub-1 GHz, Wireless MBUS Standard,” 2011.
- [6.32] ON Semiconductor, “AX8052F151 SoC Ultra-Low Power RF-Microcontroller for the 400 - 470 MHz and 800 - 940 MHz Bands”, 2016.
- [6.33] Infineon Technologies, “Smart Low Energy Wireless Systems with a Microcontroller Unit PMA71xx,” 2010.
- [6.34] Nordic Semiconductor, “nRF9E5 433/868/915MHz RF Transceiver with Embedded 8051 Compatible Microcontroller and 4 Input, 10 Bit ADC,” 2011.
- [6.35] ZigBee Alliance, Inc., “ZigBee Specification,” San Ramon, California ,2012.
- [6.36] Office of Communications (Ofcom), “Short Range Devices operating in the 863 - 870 MHz frequency band,” Final Report, 2210/SRDMR/R/3, August 2010.
- [6.37] Silicon Laboratories, Inc., “Si106x Development Kits Users’ Guide,” 2013.
- [6.38] Linx Technologies, “Ultra Compact Chip Antenna Data Guide,” 2012.
- [6.39] Texas Instruments Inc., “BQ25504 Ultra Low-Power Boost Converter With Battery Management for Energy,” 2014.
- [6.40] Analog Devices Inc., “ADP5090 Ultralow Power Boost Regulator with MPPT and Charge Management,” 2015.
- [6.41] Linear Technology Corporation, “LTC3105 400mA Step-Up DC/DC Converter with Maximum Power Point Control and 250mV Start-Up” 2010.
- [6.42] Maxim Integrated, “MAX17710 Energy-Harvesting Charger and Protector,” 2012.
- [6.43] STMicroelectronics, “SPV1050: Ultralow power energy harvester and battery charger with embedded MPPT and LDOs,” 2015.
- [6.44] Silicon Laboratories, Inc., "TS3300 0.6-3V_{IN}, 1.8-3.6V_{OUT}, 3.5μA, High-Efficiency Boost + Output Load Switch", 2014.

- [6.45] P. Spies, L. Mateu, and M. Pollak, Eds., *Handbook of Energy Harvesting Power Supplies and Applications*, Boca Raton, Taylor & Francis Group, 2013.
- [6.46] N. J. Dudney, W. C. West, and J. Nanda, Eds., *Handbook of Solid State Batteries*, Second Edition, Singapore, World Scientific Publishing Co. Pte. Ltd, 2016.
- [6.47] Panasonic Corporation, “Manganese Lithium Coin Batteries (ML series): Individual Specifications,” 2005.
- [6.48] T. M. Razykov, C. S. Ferekides, D. Morel, E. Stefanakos, H. S. Ullal, and H. M. Upadhyaya, “Solar photovoltaic electricity: Current status and future prospects,” *Solar Energy*, vol. 85, no. 8, pp. 1580–1608, 2011.
- [6.49] J. L. Gray, “The Physics of the Solar Cell,” in *Handbook of Photovoltaic Science and Engineering*, A. Luque and S. Hegedus, Eds., John Wiley & Sons, Ltd, Chichester, UK, 2003.
- [6.50] M. Kasemann, K. Rühle, and L. M. Reindl, “Photovoltaic Energy Harvesting under Low Lighting Conditions,” in *Proceedings of AMA Conference 2013*, September, pp. 483–485, 2013.
- [6.51] D. E. Carlson and C. R. Wronski, “Amorphous silicon solar cell,” *Applied Physics Letters*, vol. 28, no. 11, pp. 671–673, 1976.
- [6.52] J. F. Randall and J. Jacot, “Is AM1.5 applicable in practice? Modelling eight photovoltaic materials with respect to light intensity and two spectra,” *Renewable Energy*, vol. 28, no. 12, pp. 1851–1864, 2003.
- [6.53] N. H. Reich, W. Van Sark, E. a Alsema, S. Y. Kan, S. Silvester, A. Van Der Heide, R. W. Lof, and R. Schropp, “Weak Light Performance and Spectral Response of Different Solar Cell Types,” in *the Proceedings of the 20th European Photovoltaic Solar Energy Conference and Exhibition*, no. 1, pp. 4–7, 2005.
- [6.54] C. Carvalho and N. Paulino, “On the feasibility of indoor light energy harvesting for wireless sensor networks,” *Conference on Electronics, Telecommunications and Computers – CETC 2013, Procedia Technol.*, vol. 17, pp. 343–350, 2014.
- [6.55] S. Vignati, “Solutions for Indoor Light Energy Harvesting,” M.S. thesis, Communication Systems Department, School of Information and Communication

Technology, Kungliga Tekniska Högskolan (KTH), SE-164 40 Kista, Stockholm, Sweden, November 2012.

[6.56] M. Lont, D. Milosevic, A. H. M. van Roermund and G. Dolmans, “Ultra-low power FSK Wake-up Receiver front-end for body area networks,” *2011 IEEE Radio Frequency Integrated Circuits Symposium*, Baltimore, MD, 2011, pp. 1-4.

[6.57] X. Huang, S. Rampu, X. Wang, G. Dolmans, and H. de Groot, “A 2.4GHz/915MHz 51 μ W Wake-Up Receiver with Offset and Noise Suppression,” in *IEEE International Solid-State Circuit Conference*, 2010, pp. 222–223.

[6.58] J. Ansari, D. Pankin, and P. Mähönen, “Radio-triggered wake-ups with addressing capabilities for extremely low power sensor network applications,” *International Journal of Wireless Information Networks*, vol. 16, no. 3, pp. 118–130, 2009.

[6.59] S. J. Marinkovic and E. M. Popovici, “Nano-Power Wireless Wake-Up Receiver With Serial Peripheral Interface,” in *IEEE Journal on Selected Areas in Communications*, vol. 29, no. 8, pp. 1641-1647, September 2011.

[6.60] Avago Technologies, “HSMS-285x Series Surface Mount Zero Bias Microwave Schottky Detector Diodes,” 2009.

[6.61] STMicroelectronics, “TS881: Rail-to-rail 0.9V nanopower comparator,” 2013.

[6.62] Cymbet Corporation, “CBC-EVAL-08 EnerChip™ EH Solar Energy Harvester Evaluation Kit,” 2014.

[6.63] H. T. Friis, "A Note on a Simple Transmission Formula," in *Proceedings of the Institute of Radio Engineers (IRE)*, vol. 34, no. 5, pp. 254-256, May 1946.

[6.64] T. S. Rappaport, *Wireless Communications: Principles and Practice*, 2nd Ed. Prentice Hall, Upper Saddle River, NJ, 2002.

[6.65] Campbell Scientific, Inc., “The Link Budget and Fade Margin”, Utah, USA, Application Note 3RF-F, 2016.

Chapter 7

Conclusion

This thesis describes the implementation and extension of an analytic approach that facilitates the design of RF power transistors and amplifiers. It has been verified that the analytic approach, using expressions derived from an equivalent circuit model, yields optimum impedance values and reasonably accurate predictions of the RF performance of power amplifier before the fabrication of prototypes. This proved to be effective and helpful for designing RF PAs using commercially available RF transistors since the large-signal models provided by most vendors generally lack the required accuracy. The analytic approach is utilized to gain an understanding of the relationship between the device performance, the elements of devices and package models, S-parameters and I-V characteristics. This can be easily applied from the design stage to commercially available devices to reduce time and costs related to amplifier design and also the development and optimization of devices and packages for RF applications.

This thesis describes the design and implementation of an autonomous wireless sensor node. The power consumption of a WSN has been reduced by choosing the appropriate hardware and employing a wake-up receiver to reduce the active and idle mode currents. The low power consumption together with ambient energy harvesting can allow a wireless sensor node to be autonomous and considerably extend its operating lifetime. A study is carried out to evaluate and compare the performance of six solar cell technologies under indoor light condition. The results and observations can be useful for future research using this technology.

7.1 Main Achievements

The main results that have been presented in the thesis are summarised here.

New Analytic Expressions

New expressions are derived to calculate the optimum source and load impedances and to predict the performance of a radio frequency power amplifier. The expressions include additional extrinsic elements for the parasitic introduced by the package which allow to evaluate the effects of a package on the optimum impedance values and performance.

Validation of Analytic Approach for High Power Amplifiers

For the first time, the validity and accuracy of the analytic approach are demonstrated at a high frequency of 3.25 GHz for high power GaN based devices with measured results of prototype amplifiers designed for the impedance values obtained from the analytic expressions.

Optimization of Impedance Values for Different Criteria

The analytic approach is extended to determine the optimum impedance values and predict the RF performance for different criteria of maximum gain, linearity and efficiency. A study of the responses of silicon LDMOS and GaN HEMT using this approach demonstrated that the latter is relatively immune to optimization due to higher value of feedback capacitance and output conductance.

A Comparison of Six Solar Cell Technologies for Indoor Energy Harvesting and Design of an Autonomous Wireless Sensor Node

A comprehensive comparison of six different solar cell technologies for indoor light energy harvesting under a controlled light intensity of 330 lux, which corresponds to typical office illumination, is carried out. The dye-sensitized and perovskite solar cells are found to be the best options considering both performance and cost. The design and implementation of an autonomous wireless sensor node using commercially available components is presented. By including a wake-up receiver in the design, the overall power consumption has been reduced significantly.

7.2 Future Work

The work in this thesis can be improved and extended to obtain a more complete set of tools that will help researchers and engineers to design and optimize radio frequency transistors, amplifiers, and wireless sensor nodes and network. Few potential directions of future research are suggested below.

Design of Broadband Power Amplifiers

All the present cellular technologies up to 4G work in the frequency range of 300 MHz to 3 GHz; and therefore, there are many different frequency bands in use around the world. In addition, the wide range of new services and applications and the rapid

growth in wireless data traffic will require broader and adjacent channel bandwidth for communication systems for future 5G cellular network. Traditional RF systems require separate amplifiers and support components for each band. A broadband amplifier can provide a single front end that can handle a wide range of frequencies with desired performance across the whole band. This can significantly reduce the cost and complexity of RF design. The work in this thesis focused on amplifiers designed at one frequency. The analytic approach can be extended to design broadband power amplifiers. By calculating the RF performance of the device at a range of frequencies and load resistance values, an optimum load resistance can be chosen that gives the best trade-off between RF performance and broadband operation.

Evaluation of Analytic Approach at Higher Frequency

The requirement for broader and adjacent channel bandwidth for communication systems for future 5G cellular network cannot be totally addressed by current available bands. Therefore, it will be necessity to use spectrum resources at higher frequency range. In this thesis, the analytic approach to design linear amplifiers is extended up to a high frequency of 7.5 GHz and the accuracy of the calculated results has been validated by comparing with harmonic balance simulation results. The validity and accuracy of analytic approach is demonstrated with measurement of prototype amplifiers at a frequency of 3.25 GHz. In accordance with this work, the validity and accuracy of analytic approach should be evaluated at higher frequency with experimental results of prototype amplifiers. The equivalent circuit model and analytic expressions should be improved as necessary.

Study of Dispersion Effects on the Extrinsic and Intrinsic Parameter Values

The frequency-dependent dispersion effects on the RF performance have been studied in thesis using the I-V characteristics under DC and pulsed conditions. The values of intrinsic and extrinsic parameters in the equivalent circuit model are extracted from S-parameters measurements under continuous wave conditions. Since the behaviour of RF transistors differs between continuous wave and pulsed stimulus, the work in this thesis can be extended by extracting the parameter values from pulsed S-parameter measurements and then using the analytic approach to the study the impact of dispersion effects on the intrinsic and extrinsic parameters and the RF performance by

comparing the calculated results using the parameter values obtained from CW and pulsed S-parameter measurements.

Improvement of the Range of the Wireless Sensor Node

The range of the wireless sensor node in this work is limited by the high return loss at the input due to impedance mismatch between the wake-up receiver and the antenna. Therefore, the input matching network should be improved to reduce the return loss and thus increase the range of the wireless sensor node. The wake-up receiver and the matching network consist of discrete components and transmission lines in close proximity due to the compact design. This might lead to unintended electromagnetic coupling between the circuit elements and coupling-induced mismatch. Three-dimensional electromagnetic simulations can be performed to design and optimize the matching network, as well as the physical layout of the wake-up receiver if necessary. The impact of component tolerances on the performance should also be considered. In addition, a fade margin should be considered to avoid the effects of unpredictable and temporary losses and allow the wireless sensor node to maintain the desired range through its operation.

Design and Implementation of an Autonomous Wireless Sensor Network

The work in this thesis only considered two nodes communicating with each other, whereas in an actual application, a wireless sensor network would consist of more nodes. Therefore, the wake-up receivers should be designed to make sure only the target node wakes up from sleep mode.

In a wireless sensor network with multiple nodes, the data traffic for an individual node is expected to be higher than the considered scenario in this work as the nodes often have to relay the packets from other nodes. Therefore, the total number of receive and transmit operations and consequently the power consumption of an individual node would also increase. Therefore, the required power to be generated from energy harvesting and the corresponding size of the solar cell panels should be determined from further study based on the network.

List of Publications/Conferences

1. M. Rasheduzzaman, N. Chevaux, M.M. De Souza, N. McEwan, R. Rayit, and J. Brunning, "Understanding the Response of GaN HEMT to Optimization Criteria in RF Power Amplifiers Using the Analytic Approach", *IET Active and Passive RF Devices Seminar*, London, 2016.
2. M. Rasheduzzaman, N. Poluri, and M.M. De Souza, "Evaluation of Analytic Approach for design of Deep Class-AB Power Amplifiers in GaN", *Poster Presentation in UK Semiconductors 2016*, Sheffield, July 2016.
3. M. Rasheduzzaman, P. Balakrishna Pillai, A.N.C. Mendoza, and M.M. De Souza, "A Study of the Performance of Solar Cells for Indoor Autonomous Wireless Sensors", *10th International Symposium on Communication Systems, Networks and Digital Signal Processing CSNDSP 2016*, Prague, July 2016.
4. M. Rasheduzzaman, N. Chevaux, M.M. De Souza, "A study of the mechanism of the nonlinear input capacitance on the RF performance in GaN HEMT devices", *33rd Automated RF and Microwave Measurement Society (ARMMS) Conference*, Wyboston, 09 Nov 2015 - 10 Nov 2015.
5. M. M. De Souza, M. Rasheduzzaman, S.N. Kumar, "Designing high power RF amplifiers: An analytic approach", in *Proceedings, of 2014 International Caribbean Conference on Devices, Circuits and Systems, ICCDCS 2014 Conference*, Mexico, April 2014.
6. N. Chevaux, M. Rasheduzzaman and M.M. De Souza, "Progress of power devices in RF applications", in *Proceedings of 11th International Seminar on Power Semiconductors*, Prague, 2012.
7. M.M. De Souza, N. Chevaux, M. Rasheduzzaman, "RF Power Amplifier: Pushing the Boundaries of Performance versus Cost", in *Proceedings of SPIE 8549, 16th International Workshop on Physics of Semiconductor Devices*, October 2012.

Glossary

Adapter	A two-sided coaxial component that enables connection between two dissimilar connectors or cables.
Admittance	A measure of the ease with which alternating current flows in a circuit; it is the reciprocal of the impedance of an electric circuit
Ambient Temperature	Temperature of the air surrounding any electrical component or device.
Amplifier	An active device that takes an input signal and produces an output signal of the same frequency with higher power level.
Analog-to-Digital Converter (ADC)	A device that changes an analog signal to a digital signal of corresponding magnitude.
Antenna	An RF component or device used to transform electric power traveling through a conductor, such as transmission line, into electromagnetic wave in free space and vice versa.
Antenna Gain	The maximum ratio of an antenna's maximum radiation intensity, the ability to focus or receive power, in a given direction relative to a standard; the standard is usually an isotropic radiator or a dipole.
Attenuation	The decrease in the power of an electric signal with distance in the direction of propagation due to the losses in the transmission medium.
Attenuator	A device or network that absorbs part of an input signal and transmits the remainder with minimal distortion.
Back-off	A technique used to reduce the intermodulation products for multiple carriers to avoid distortion in amplifiers when operated near saturation. A 6 dB back-off is defined by a 6 dBm difference between the input signal power required for saturation and that applied.
Band Gap	The energy difference between the top of the valence band and bottom of the conduction band of a material.
Base Station	A transceiver in radio communication system that is permanently positioned in a specific geographical location. A mobile radio transceiver establishes connection with a base station to gain access to the telephone network.

Bias Network	In an RF power amplifier, the bias network is a circuit designed to apply the proper DC bias to the appropriate terminals of the transistor and to isolate the DC voltages and currents from interfering with the RF operation of the circuit and vice versa.
Bit	The fundamental unit of data in a computer, short for “binary digit”, that has a single binary value of either “0” or “1.”
Bit rate	The number of bits transmitted per second.
Characteristic Impedance	An intrinsic property of a transmission line defines the frequency-dependent measure of opposition to an alternating current travelling through it. For a uniform line, it is not dependent on its length and can be calculated based on the physical dimensions and dielectric properties of the transmission line structure. Most RF and microwave systems and components have a characteristic impedance of 50 Ohms.
Continuous Wave (CW)	Periodic and usually sinusoidal wave of constant amplitude, in contrast to a pulsed or modulated wave.
Coaxial	A transmission line formed by two concentric conductors separated by a dielectric designed to confine the fields and their energy in the medium between the two conductors. For example: in a coaxial cable the core which transmits the signal and the metallic shield have a dielectric insulator in between, and everything protected by plastic jacket.
Conductor	A material that presents very little resistance to electrically charged carriers, usually electrons, and allows them to move easily with the application of voltage; and thus, allows the flow of electrical current.
Decibel (dB)	In RF, decibel is a unit of measure equal to ten times the logarithm to the base 10 of a power ratio between two electrical signals.
dBm	Decibels referenced to 1 milliwatt. This is the standard unit of power level used in RF or microwave work. For example: 0 dBm = 1 mW.
dB<i>i</i>	Decibels related to isotropic. dB <i>i</i> relates the gain of an antenna relative to an isotropic (perfectly spherical pattern) antenna.
DC Block	An electrical component, often a capacitor in series, used to prevent low frequencies or direct current (DC) components in

RF circuits without affecting the RF signal along a transmission line.

Die	An uncased discrete device or integrated circuit obtained from a semiconductor wafer.
Dielectric	A medium that acts as an electrical insulator due to its negligible or poor electrical conductivity.
Dielectric Constant (ϵ_r)	An electric property of an insulator or semiconducting material, which describes how differently electric fields will behave inside of the material as compared to air. For example: gallium nitride has a dielectric constant $\epsilon_r = 9$ as compared to $\epsilon_r = 1$ for air.
Dielectric Loss	Loss in power due to the transformation of electromagnetic energy into heat within the dielectric material.
Electromagnetic Waves	An electromagnetic (EM) wave is a combination of electric and magnetic fields moving through space carrying energy. In an EM wave, the fields oscillate perpendicular to each other and to the direction of propagation.
Effective Dielectric Constant (ϵ_{eff})	The resulting effect of having two dielectric materials in a transmission medium. For example, in a microstrip transmission line, the electric field supported by the signal traveling through the conductor flow through both air and the substrate; and thus, it has an effective dielectric constant ϵ_{eff} .
Electromagnetic Interference (EMI)	Any unwanted electromagnetic signal or disturbance, usually can be generated by electronic circuits switching at high frequencies, that interrupts and often degrades or limits the performance of an electronic or electrical equipment.
Envelope	The waveform generated by connecting the peak values of a modulated carrier wave.
Equivalent Circuit	A combination of electric circuit elements chosen to represent the operation of a device by establishing the same relationships for voltage, current, and power.
Fourier Analysis	The process in which a complex waveform is decomposed into component waves, each having a certain frequency, amplitude and phase.
Fourier Transform	A mathematical technique to convert a time domain signal to a frequency domain signal and vice versa.

Frequency	The repetition rate of a periodic signal. The unit of frequency is hertz (Hz) which represents one cycle per second.
Frequency Domain	Representation of a signal by its frequency components
Frequency Range	The minimum and maximum frequencies between which a particular component will function properly as per its specification.
Gain	The ratio of the output power to the input power of an amplifier, usually expressed in dB.
GHz	A unit of frequency measure equal to 1000 MHz or a billion hertz.
Ground	The electrical “zero” state, used as the reference point to measure voltages in a circuit.
Grounding	A safety measure where a wire is intentionally connected to earth to carry electrical current under short circuit or other conditions that would be potentially dangerous. The grounding wire does not carry electricity under normal circuit operations.
Harmonic	Sinusoidal component of a periodic waveform that has a frequency equal to an integer multiple of the fundamental frequency.
Hertz	International standard term for cycles per second. For example: 60 cycles per second is equal to 60 hertz or 60 Hz.
I-V Characteristics	A set of graphical curves that describes the current through a device as a function of applied voltages across its terminals.
Impedance (Z)	Electrical property of a network that defines the frequency-dependent measure of opposition to an alternating current travelling through it. Impedance is defined in Ohms (Ω) as the ratio of the AC voltage to the AC current at a given point in the network and usually represented in complex notation as $Z = R + jX$, where R is the ohmic resistance and X is the reactance. In case of DC voltage and current, impedance and resistance are the same.
Insertion loss	The loss due to the insertion of a component in a signal path.

Intermediate frequency (IF)	The frequency produced when two signals are combined in a mixer circuit.
Lattice Constant	The length of the sides of the three-dimensional unit cell in a crystal.
Light Emitting Diode (LED)	An optical semiconductor device that emits light through spontaneous emission by a phenomenon termed as electroluminescence. When voltage is applied across an LED, which is essentially a forward-biased p-n junction, electric current passes through it. The electrons recombine with holes and release energy in the form of photons.
Line of Sight	The shortest possible straight line that can be imagined between a transmitter and a receiver. The strongest signal will be received if there are no obstacles in the line of sight.
Matching Network	A matching network is an electric circuit, connected between a source and its load, designed to maximise the power transfer from the source to the load. Its input impedance is the complex conjugate of the source output impedance, while its output impedance is the complex conjugate of the load impedance. Thus, it matches the source to the load and ensures maximum transfer of power.
MHz	A unit of frequency measure equal to 1000 kHz or a million hertz.
Metallization	The technique of depositing thin metallic coating layer on a semiconductor to form contacts and conductive paths for interconnection.
Microstrip	A transmission line consisting of a conductive strip and a ground plane separated by a dielectric.
Microwave	Electromagnetic waves with frequencies between 300 MHz and 300 GHz in electromagnetic spectrum.
Noise	Random fluctuations of electrical signals generated by natural disturbances or circuit components.
Ohmic Contact	A metal-semiconductor junction formed between a metal and a semiconductor that provides current conduction from metal to semiconductor and vice versa, and thus creating a low resistance, non-rectifying contact.

On-Off Keying (OOK)	A binary form of amplitude modulation where the “on” state is represented by the presence of energy in the modulated wave and the “off” state is the absence of energy in the keying interval.
Optimization	The process or methodology of determining the values of a set of parameters that maximizes or minimizes an objective function to achieve the highest achievable performance of a design or system under the given constraints.
Output Power	The RF power delivered to the load.
Package	A die must be packaged to be useful. The die is connected within the package with bond wires connecting from pads on the die to lead pins on the package. The package protects the die from the environment and allows easy connection of the die with other components in the system.
Pad	A metallized area on the surface of a semiconductor die that allows the connection of bond wires or test probes the die.
Passivation	The process of forming an insulating dielectric layer directly over the surface of a die to protect it from contaminants, moisture or particles.
PCB	A PCB or printed circuit board is a flat sheet of insulating material with traces and pads of a conducting material such as copper printed or etched on it. Active and passive electronic components as well as integrated circuits are mounted on the pads and the traces connect the components together to form a working circuit.
Power Amplifier	An amplifier at the final stage of a system, operating at either audio or radio frequency range, that raises the signal power to the required level and delivers the power to a termination such as speaker, antenna, or resistive load.
Power Supply	An electronic device that converts one form of power from a source into a form which is needed by the equipment to which power is being supplied. For example: a bench top power supply unit converts mains electricity, which is alternating current, into direct current.
Prototype	A preliminary model of a product or system proves that the concept works and exhibits full or partial functionality of the final product.

Pulse	A sudden change in the level of a signal over a relatively short period of time and a quick return to its original value which is normally constant.
Pulse Width	The length of time over which the value of the pulsed signal is at the transient level. It is measured by the elapsed time between the rising and falling edges of a single pulse
Quality Factor (Q-factor)	<p>The quality factor (Q) a measure of the relationship between stored energy and rate of energy dissipation in an electrical component or a circuit. It can be obtained by:</p> $Q = 2 \pi * (\text{Energy stored} / \text{Energy dissipated per cycle})$ <p>A "high-Q" circuit has mostly reactive components as such inductor and capacitor, with low resistance. Hence the rate of energy loss is low and oscillations reduce more slowly.</p>
Radio Frequency	Any of the electromagnetic wave in the general frequency range from 3 kHz to 300 GHz. It is also often used generically and interchangeably with the term microwave (300 MHz to 300 GHz) for the high frequency circuit or signal.
Return Loss	A measure of reflected power on a transmission line due to impedance mismatch when it is terminated or connected to any passive or active device. Return loss, usually expressed in dB, is the ratio of reflected power to incident power.
RF Power Amplifier	A power amplifier capable of providing gain at radio frequencies.
RF Choke	A component, usually an inductor, that allows low frequency or DC to pass through, but blocks RF signals by presenting a very high impedance at radio frequencies.
RF Power	The RF power (P_{RF}) is the maximum amount of mean or average power (P_{avg}) of an RF signal, expressed in watts, delivered to the load by an RF power amplifier over a complete period of time (T).

$$P_{RF} = P_{avg} = \frac{1}{T} \int_0^T p(t) \cdot dt$$

Here, $p(t)$ is the instantaneous power, which is the power given at any instant of the time (t) over the duration of the RF signal. The average RF power delivered to the load R can also be written as:

$$P_{RF} = \frac{1}{T} \int_0^T \frac{v(t)^2}{R} \cdot dt = \frac{1}{T} \int_0^T i(t)^2 R \cdot dt$$

Here, $v(t)$ and $i(t)$ are the instantaneous voltage and current. In RF circuits, the average currents and voltages are generally stated as root mean square or rms values. Therefore, the P_{RF} is also known as rms power and expressed as:

$$P_{RF} = \frac{V_{rms}^2}{R} = I_{rms}^2 R = V_{rms} \cdot I_{rms}$$

$$\text{Where, } V_{rms} = \sqrt{\frac{1}{T} \int_0^T v(t)^2 \cdot dt} \text{ and } I_{rms} = \sqrt{\frac{1}{T} \int_0^T i(t)^2 \cdot dt}$$

For a continuous wave, the P_{RF} can be calculated as:

$$P_{RF} = I_{rms}^2 R = R \left(\sqrt{\frac{1}{T} \int_0^T (I_{peak} \sin(\omega t))^2 dt} \right)^2$$

$$= \frac{RI_{peak}^2}{2T} \int_0^T 2 \sin^2(\omega t) \cdot dt = \frac{RI_{peak}^2}{2} \frac{1}{T} \int_0^T (1 - \cos(2\omega t)) \cdot dt$$

Since the sinusoidal term averages to zero over any number of complete cycles, the RF power for continuous wave RF signal can be expressed as:

$$P_{RF} = \frac{RI_{peak}^2}{2} = \frac{1}{2} V_{peak} I_{peak}$$

Here, V_{peak} and I_{peak} are the peak value of RF voltage and current.

Resolution	The smallest amount of change in the input signal that the device or instrument can detect reliably.
Sampling	The process used to convert a continuous-time signal into a discrete-time signal.
Schematic	An illustration that depicts how an electronic device is constructed.
Schematic Diagram	A diagram that shows the components and signal flow paths of an electronic circuit.
Schottky Contact	A metal-semiconductor junction formed between a metal and a semiconductor where the energy band forms a potential barrier known as the Schottky barrier to align the Fermi levels on both sides of the junction. The electrons must overcome the Schottky barrier in order to flow from the semiconductor into the metal and thus creates a rectifying contact.
Schottky Diode	A diode formed by the Schottky barrier junction, often chosen for its high switching speed and low forward voltage drop.

Semiconductor	A material that can act as an electrical conductor or insulator depending on chemical alterations or external conditions. Examples are silicon and gallium arsenide.
Settling Time	The time required for a measurement system to stabilize to a specified accuracy limit.
Shield	(1) A conducting structure in an RF device that greatly reduces the effect of electric fields coming from one side onto the other side. It is also known as field plate. (2) The metallic layer placed around the conductors in a cable or the metallic enclosure in measurement system, that prevents electromagnetic or electrostatic interference between the external fields and enclosed conductors or device under test.
SMA Connector	SubMiniature version A or SMA connector is a coaxial RF connector with both male and female versions with a typical frequency range of DC - 18 GHz.
Spectrum	A term usually used to describe the range of frequencies or wavelengths of electromagnetic radiation for any specific application. For example: the visible light spectrum refers to the electromagnetic radiation with wavelengths in the range of 390 nm to 700 nm. All the known spectrums are collectively termed as electromagnetic spectrum.
Substrate	A thin slice of dielectric or semiconductor material over which transmission lines, circuit components and active devices are fabricated. A substrate can be a printed circuit board, a ceramic, or a semiconductor wafer.
Termination	A circuit element or device placed at the end of a transmission line that absorbs the signal energy, ideally with little to no reflection.
Throughput	The amount of information flow per unit time.
Thin Film	A thin layer of material, usually few nanometres to micrometres in thickness, deposited onto a substrate.
Time Domain	The specification of a signal as a function of time.
Tolerance	The total amount by which a quantity can vary. In other words, the tolerance is the difference between the maximum and minimum limits.

Transceiver	A device in a communication system that can serve as both transmitter and receiver.
Transmission Line	A conductive connection, made of conductors and dielectric material, with known electrical characteristics designed to carry electromagnetic energy from one point to another.
Transient	Any signal or condition that exists only for a short time.
Vector Network Analyser (VNA)	A microwave instrument designed to measure and process the magnitude and phase of transmitted and reflected waves from the linear network or device under test.
Velocity of Propagation	Velocity of propagation, also known as velocity factor, is a measure of the speed of a signal in a transmission medium in comparison to the speed of light in free space or vacuum.
Voltage Standing Wave Ratio (VSWR)	A way of expressing impedance mismatch in RF circuits, resulting in signal reflection which causes voltage standing waves. The VSWR is defined as the ratio of the maximum voltage to the minimum voltage in the standing wave. A perfect impedance match would cause no voltage standing wave, so the VSWR would be 1:1. The larger the impedance mismatch, the larger the value of VSWR.
Wafer	Wafer, also called slice or substrate, is a thin slice of semiconductor material on which semiconductor devices are made.
Y-parameters	The input and output admittances that are used to characterize a two-port device or network.
Z-parameters	The input and output impedances that are used to characterize a two-port device or network.
ZigBee	A standard for short-distance, low-data-rate communications based on the IEEE 802.15.4 specification. ZigBee is created and maintained by the ZIGBEE Alliance Group.