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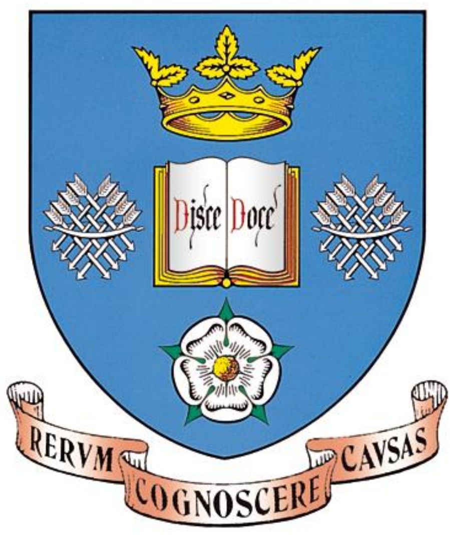

EVALUATION OF THERMAL MANAGEMENT SOLUTIONS FOR POWER SEMICONDUCTORS

By

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ABSTRACT

This thesis addresses the thermal management and reliability concerns of power semiconductor devices from die to system level packaging design. Power electronics is a continuously evolving and challenging field. Systems continue to evolve, demanding increasing functionality within decreasing packaging volume, whilst maintaining stringent reliability requirements. This typically means higher volumetric and gravimetric power densities, which require effective thermal management solutions, to maintain junction temperatures of devices below their maximum and to limit thermally induced stress for the packaging medium.

A comparison of thermal performance of Silicon and Silicon Carbide power semiconductor devices mounted on Polycrystalline Diamond (PCD) and Aluminum Nitride (AlN) substrates has been carried out. Detailed simulation and experimental analysis techniques show a 74% reduction in junction to case thermal resistance ($R_{th\ (j\text{-}c)}$) can be achieved by replacing the AlN insulating layer with PCD substrate. In order to improve the thermal performance and power density of polycrystalline diamond substrates further at the system level, direct liquid cooling technique of Direct Bonded Copper (DBC) substrates were performed.

An empirical model was used to analyse the geometric and thermo-hydraulic dependency upon thermal performance of circular micro pins fins. Results show that micro pin fin direct cooling of DBC can reduce the number of thermal layers in the system, and reduce the thermal resistance by 59% when compared to conventional DBC cooling without a base plate.

Thermal management and packaging solutions for the wide band gap semiconductors, such as GaN, is also described in detail. Comparisons of face up and flip chip thermal performance of GaN on Sapphire, Silicon and 6H-SiC substrates in a T0-220 package system is presented. Detailed thermal simulation results analysed using ANSYS® show that a flip chip mounted GaN on sapphire substrate can reduce junction to case thermal resistance by 28% when compared against the face up mounted technique.

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LIST OF ACRONYMS

Si	Silicon
SiC	Silicon carbide
GaN	Gallium nitride
Beo	Beryllium oxide
AlN	Aluminium nitride
PCD	Polycrystalline diamond
DBC	Direct Bonded Copper
PGA	Pin grid array
QFP	Quad flat pack
SOT	Small outline package
SnAg	Lead free solder
Al_2O_3	Aluminium oxide
MCM	Multichip modules
FOM	Figure of Merit
HEMT	High Electron Mobility Transistor
LIGA	Lithographie, Galvanik and Abformung

NOMENCLATURE

Symbol	Definition	Unit
V	Voltage	(V)Volt
I	Current	(A)Ampere
R	Resistance	(Ω)Ohm
L	Inductance	(H)Henry
C	Capacitance	(F)Farad
ΔT	Temperature difference	°C
P_D	Power dissipated	W
R_{th}	Thermal resistance	°C/W
k	Thermal conductivity	W/mK
A	Cross sectional area	m^2
C_{th}	Thermal capacitance	J/°C
c_p	Specific heat capacity	J/Kg.K
ρ	Density	Kg/m^3
V	Volume	m^3
F_{sw}	Switching frequency	Hz
E_{on}	Turn on energy loss	J
E_{off}	Turn off energy loss	J
A_c	Contact area	m^2
A_v	Void area	m^2
α	Coefficient of thermal expansion	C^{-1}
σ_e	Equivalent stress	Pa
$\Delta\varepsilon$	Strain amplitude	-
ε_f	Fracture strain	-
c	Empirical fatigue ductility exponent	-
T_j	Junction temperature	°C
T_c	Case temperature	°C
$R_{th(j-c)}$	Thermal resistance junction to case	°C/W
$R_{th(c-HS)}$	Thermal resistance case to heat sink	°C/W

Symbol	Definition	Unit
$R_{th(Hs-a)}$	Thermal resistance heat sink to ambient	°C/W
$R_{th(j-a)}$	Thermal resistance junction to ambient	°C/W
$Z_{th(j-c)}$	Thermal impedance junction to case	°C/W
L	Tile length	m
b	Tile breadth	m
W_L	Wetting area length	m
W_b	Wetting area breadth	m
H	Fin height	m
D	Fin diameter	m
ΔP	Pressure drop	Pa
m_f	Mass flow rate	Kg/s
R_e	Reynolds number	-
μ	Viscocity	Kg/(s.m)
p_r	Prandtl number of water	-
p_{rs}	Prandtl number of air	-
k_{fluid}	Thermal conductivity of fluid	W/mK
k_{fluid}	Thermal conductivity of fin	W/mK

CHAPTER 1: INTRODUCTION

1.1 Introduction

Power electronics is a continuously evolving and challenging field as power systems continue to demand increasing functionality within a decreasing packaging volume whilst maintaining stringent reliability requirements. This typically results in higher volumetric and power densities, which require effective thermal management solutions to maintain junction temperatures below their maximum rating. The thermal design of a semiconductor package depends upon the semiconductor die size, power dissipation, junction and ambient temperatures as well as cost constraints. The focus of semiconductor engineering to increase die current densities makes the thermal design more challenging due to its associated increase of heat flux[1]. Moreover, over the next decade, the advancements in the power density is expected because of the increase in power dissipation and reduction in the size, which is illustrated in Figure 1.1. The advancements in power density highlight the importance of thermal management solutions in determining the future semiconductor device technology.

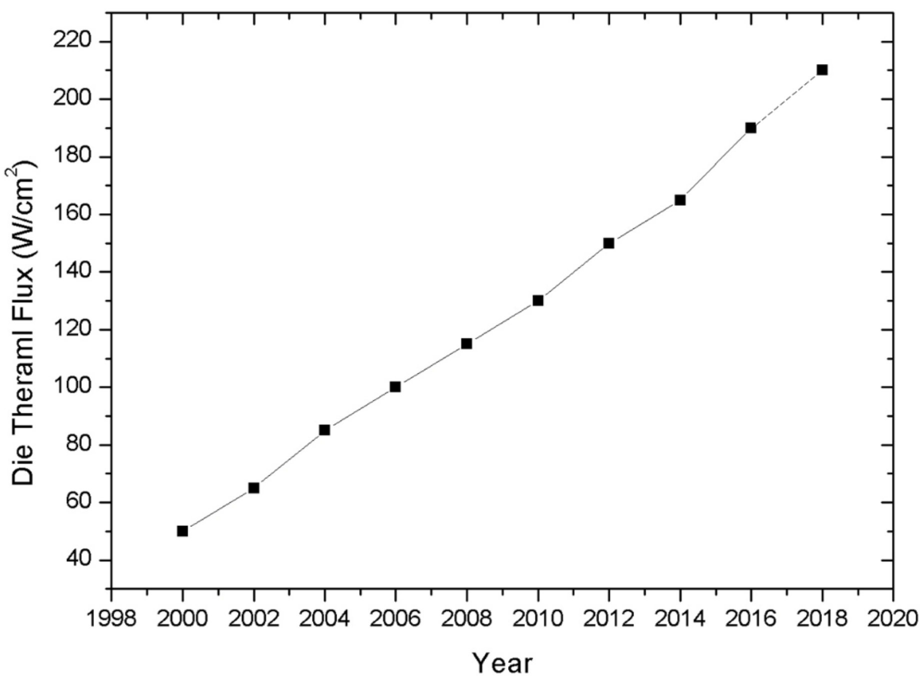


Figure 1.1: Thermal flux trend[1]

1.2 What is Thermal management?

The flow of electrical current through the leads and Silicon layers of a power semiconductor device, effects in substantial internal heat generation within an operating environment. The heat generated internally has to be removed appropriately using adequate cooling techniques. In the absence of cooling—the junction temperature of the semiconductor device would rise at

a constant rate to its maximum value at which semiconductor device fails catastrophically[2]. In order to maintain the junction temperature of the semiconductor device below its maximum allowable limit, the device should be placed in contact with a medium at a lower temperature, which assists heat flow away from the device as heat flows from a hot to a cold medium. Due to the cooling effect, the junction temperature rise is restrained as it approaches thermal equilibrium. Under steady-state conditions, all the heat generated by the component is transferred to the ambient. Thus by implementing forced cooling technique, such as liquid cooling or forced impingement cooling instead of natural convection, the junction temperature rise above the ambient can be reduced. Conduction, convection and radiation are the three modes of heat transfer which plays a vital role in electronics cooling. Effective power semiconductor thermal packaging relies on careful combination of materials and heat transfer mechanisms to maintain the device junction temperature well below its maximum limit.

1.3 Why Thermal management?

Advancement in the field of power electronics has led to substantial increase in power density integration and reduction in component size. This leads to high heat flux dissipation at the chip level. In order to keep the junction temperature well below the maximum allowable limit with respect to device performance and reliability, enhancements in cooling techniques are required; therefore thermal management solutions are increasingly important in determining the future of the power electronics industry. The significant challenge lies in maintaining the junction temperature below the maximum allowable limit by dissipating the heat flux from the power semiconductor device. The key factors influencing the thermal design of the system are chip size, power dissipation, material layer properties, junction temperature and ambient temperature. Power semiconductor manufacturers aim at reducing the chip size over the years which in turn increases the thermal design challenges, due to the increased levels of heat flux. The growth in power density is estimated to increase significantly over the next few decades due to smaller chip size and high power dissipation. The increasing power density and challenges in thermal design indicates the need for thermal management and its significance in determining the future of power semiconductor devices[3].

1.4 Electrical and thermal parameters

A correlation between the electrical and thermal parameters is shown in Figure 1.2[4]. In the electrical domain, according to Ohm's law, a linear relationship exist between current flowing through a resistor causing a voltage drop across it.

$$V = I.R \qquad (1.1)$$

In the thermal domain, the voltage and current relationship is defined as the temperature difference is equal to product of the power dissipated and the thermal resistance of the object.

$$\Delta T = P_D.R_{th} \qquad (1.2)$$

Where, electrical resistance in electrical domain corresponds to thermal resistance in thermal domain. Current (I) in electrical domain corresponds to power dissipated (P_D) in thermal domain, while voltage difference in electrical domain corresponds to temperature difference (ΔT) in thermal domain as described in Figure 1.2.

Figure 1.2: Electrical and thermal domain (a) Electrical and (b) Thermal domain

1.5 Heat transfer modes

Heat transfer in a power module occurs in three modes conduction, convection and radiation[5]. Figure 1.3 shows the cross sectional heat transfer path for a convectional wire bonded power module. Radiative heat transfer occurs in the active region of the semiconductor die due to power dissipation. Whereas, conductional heat transfer occurs in the board level mainly through the die attach medium, DBC substrate, base plate and thermal interface material. Convectional heat transfer occurs in the heat sink level either through natural or forced convection.

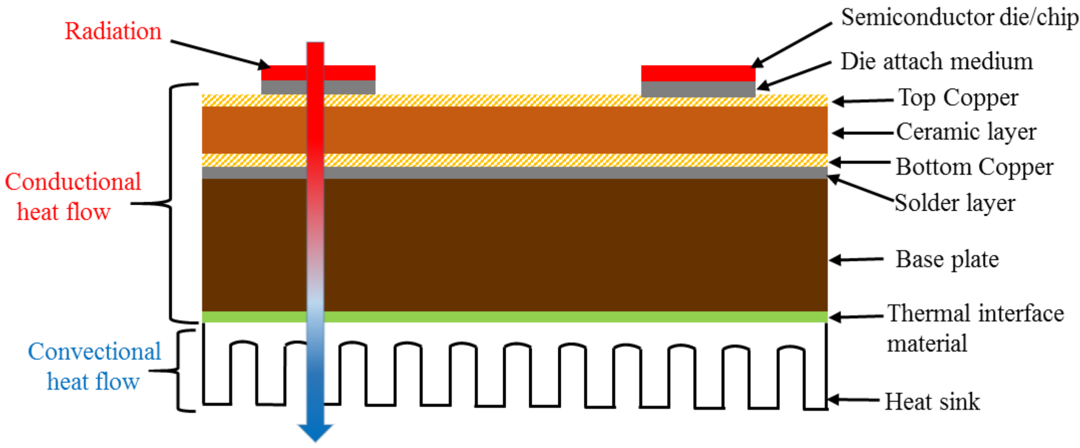


Figure 1.3: Heat flow in a wire bonded power module

1.5.1 Radiation

Radiative heat transfer is due to the electromagnetic waves propagating through empty space. Heat radiation occurs in all bodies when the temperature reaches above absolute zero. Radiation in the power semiconductor devices is due to the movement of electrons in the atom which are observed as electromagnetic radiation. The radiated electromagnetic waves transmit heat energy away from the active area of the semiconductor die. Equation (1.3) describes the radiative heat transfer.

$$P_r = \sigma \,.\, \varepsilon \,.\, A \,.\, (T_1 - T_2) \qquad (1.3)$$

Where, σ, ε, A and T are the Stefan-Boltzman constant (5.66×10^{-8} W/m^{2}K^4), emissivity, surface area of the body and temperature difference respectively.

1.5.2 Conduction

Conduction heat transfer occurs due to temperature gradient in a body. Heat energy is transferred from a hot surface to a cold surface, the conductional heat flow can be represented as one dimensional heat flow as shown in Figure 1.4. Heat flows into Face1 and out from Face 2, assuming no heat loss distributed through sides of the object. According to the one-dimensional thermal conduction equation, when the two faces are held at identical temperature, temperature of the object mainly depends on the distance (L) between the Face 1 and Face 2 and its thermal conductivity.

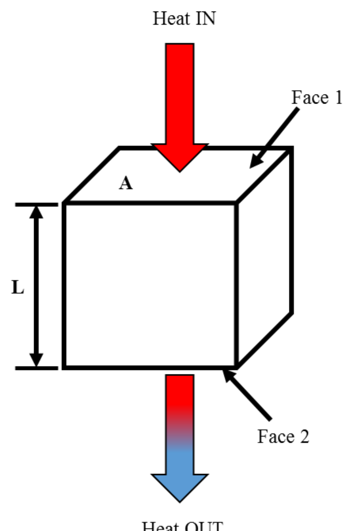


Figure 1.4: Conductional heat flow in a body

Heat transfer rate by conduction through the object in Figure 1.4 can be expressed as,

$$\frac{Q}{t} = \frac{kA}{L}\Delta T_{12} \qquad (1.4)$$

Where,

A – Cross-sectional area of the object

L – Wall thickness

ΔT_{12} – Temperature difference between two surfaces ($\Delta T_{12} = T_1 - T_2$)

k – Thermal conductivity of the material (W/mK)

The thermal resistance for conductional heat flow depends upon the thermal conductivity of the material, material thickness and area. Theoretically the thermal resistance for conductional heat flow can be represented using equation (1.5).

$$R_{Conduction} = \frac{L}{kA} \qquad (1.5)$$

Where L , k and A are the thickness of the material, thermal conductivity and cross sectional area respectively. Thermal resistance can be decreased by either increasing the cross sectional area, thermal conductivity or decreasing the thickness of the material. Table 1.1 compares the thermal conductivity of the common materials at 25°C used in electronics packaging.

Table 1.1: Common materials used in packaging

Material	Thermal conductivity 'k' (W/mK) at 25°C
Si	140
SiC	360
Solder (SnAg)	57
Silver thin film sintering	200
Copper	390
BeO	300
Alumina	35
AlN	170

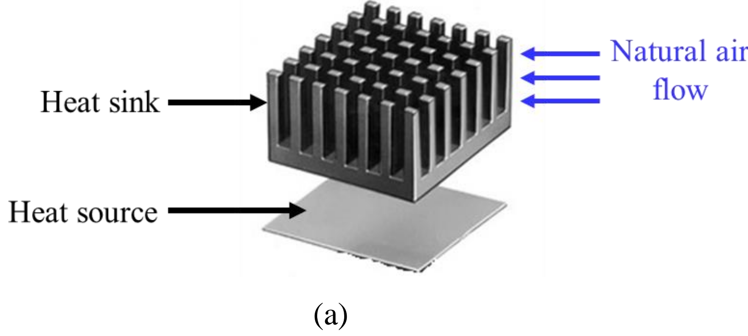
The thermal resistance for conductional heat flow can be calculated using equation (1.6), the ratio of the temperature difference to the corresponding power dissipation.

$$R_{Conduction} = \frac{T_1 - T_2}{P_d} \qquad (1.6)$$

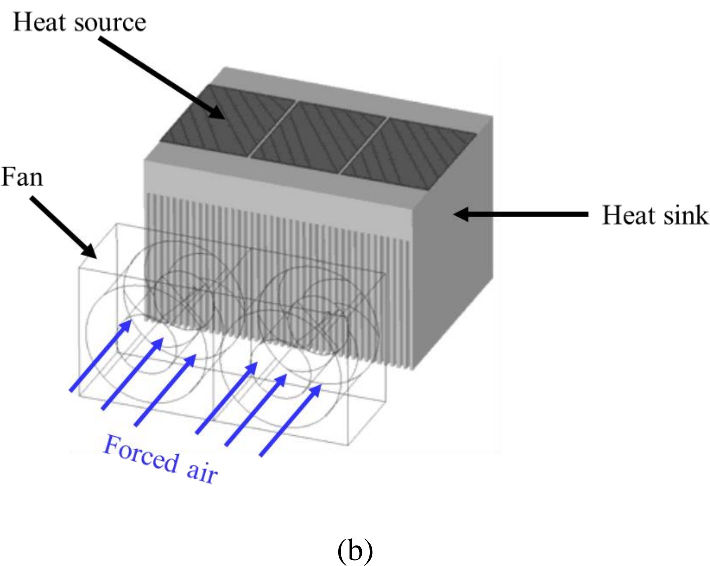
Where P_d is power dissipation and T_1 - T_2 are temperature difference between the two surfaces.

1.5.3 Convection

Convectional flow is due to the transfer of heat energy in ambient temperature via air or liquid mediums. Convectional heat transfer can be classified into natural convection and forced convection; natural convection occurs due to buoyancy force arising from density differences caused by temperature variations in the fluids. Natural convection does not require any external source like a pump or fan to push the air or fluid through it. Forced convection occurs due to the air/fluid motion generated due to external medium like a fan or pump as shown in Figure 1.5. A significant amount of heat energy can be transported efficiently using forced convection. Convectional heat transfer occurs at the system level in which the heat from the power device through different thermal layers is transported to the ambient effectively through air cooled or liquid cooled heatsinks.



(a)



(b)

Figure 1.5:Convectional heat flow (a) Natural convection; (b) Forced convection[5]

1.6 Thermal Modelling Techniques

Power electronics design involves careful consideration of the electrical and thermal domains. For instance, overdesigning the system will increase the cost and weight whereas, under designing the system may cause early failure of the power electronic components. An optimised design solution is therefore essential for perfect operation of power electronic components, which involves a good understanding and accurate prediction of semiconductor die junction temperatures and transferring the heat efficiently to the ambient. No sole thermal analysis tool works best in all circumstances[6]. A good thermal evaluation requires a combination of empirical calculations based upon thermal specifications and thermal modelling. The art of thermal analysis involves utilising one or more existing thermal tools to validate each other. Some of the existing thermal models available and widely used are

- Electro-thermal modelling
- Finite element analysis

1.6.1 Electro-thermal modelling

Physics based electro-thermal modelling would provide a more theoretical representation of thermal behaviour. Thermal model uses the material properties of the thermal layers to determine the thermal behaviour of the system. Commonly used electro thermal models are Cauer and Foster networks.

1.6.1.1 Foster thermal network

Figure 1.6 shows the Foster thermal network with parallel R/C pairs connected in a series sequence for a single chip module. The RC parameters are extrapolated from the measured thermal impedance data using curve fitting methods to determine the finite exponential terms (1.7) [7]

$$Z_{th} = \sum_{i=1}^{n} R_i \left(1 - e^{-\frac{t}{\tau_i}}\right) \qquad (1.7)$$

Where i is the index term, R_i and τ_i represent thermal resistance and time constant respectively. Thermal capacitance C_i can be calculated from equation (1.8)

$$\tau_i = R_i C_i \qquad (1.8)$$

Time constant τ_i and thermal resistance R_i values are generally provided by manufacturer data sheets which eases in calculating the remaining index term and thermal capacitance C_i. The main advantage of Foster model is it provides a quick and easier estimation of thermal resistances and capacitances for each index terms respectively. On the other hand, the disadvantages of the Foster thermal network is that it represents only the behaviour characteristics of the model, and is not associate with the physical parameters of the thermal layer materials and geometries involved. Moreover, the Foster network does not relate to physical thermal response of the overall system where the heat flow from junction to case are governed by the heat capacity and thermal resistance of various layers which accounts thermal delays in the system. With the transient curve representing junction temperature against time, exponential terms comprising of a time constant and amplitudes could be fit to the transient curve to represent the Foster RC model.

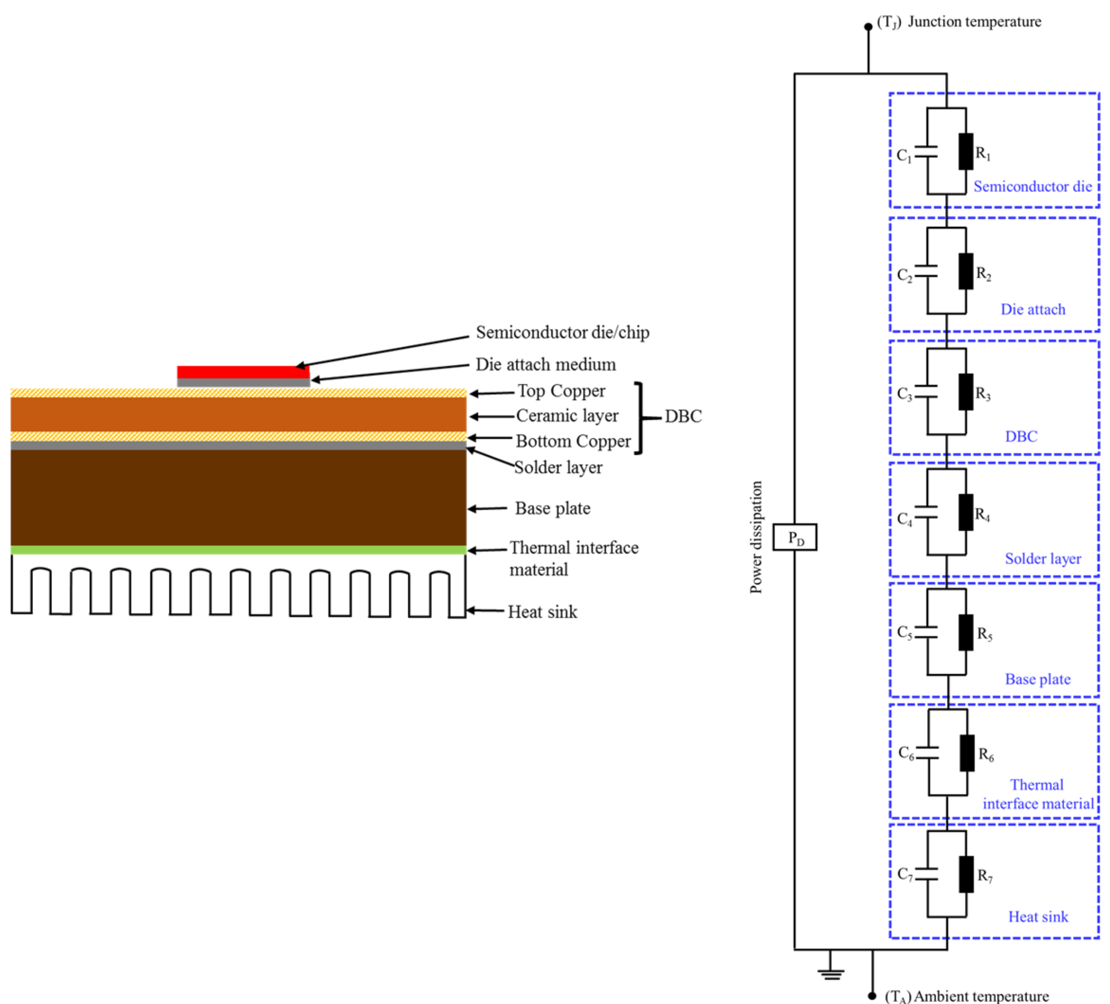


Figure 1.6: Foster thermal network of a single chip module

1.6.1.2 Cauer thermal network

Cauer thermal network utilises thermal capacitors connected to a thermal ground, referred at absolute zero, allowing the network to store heat energy. The Cauer thermal network provides more realistic physical representation of the system transient behaviour by accounting for time delays using material properties[7]. Figure 1.7 shows the Cauer thermal network with thermal resistance and capacitance path for a single chip module. Thermal resistance and capacitance values for each node or layers can be obtained from the geometric and its material parameters such as thermal conductivity, density and specific heat capacity values[7].

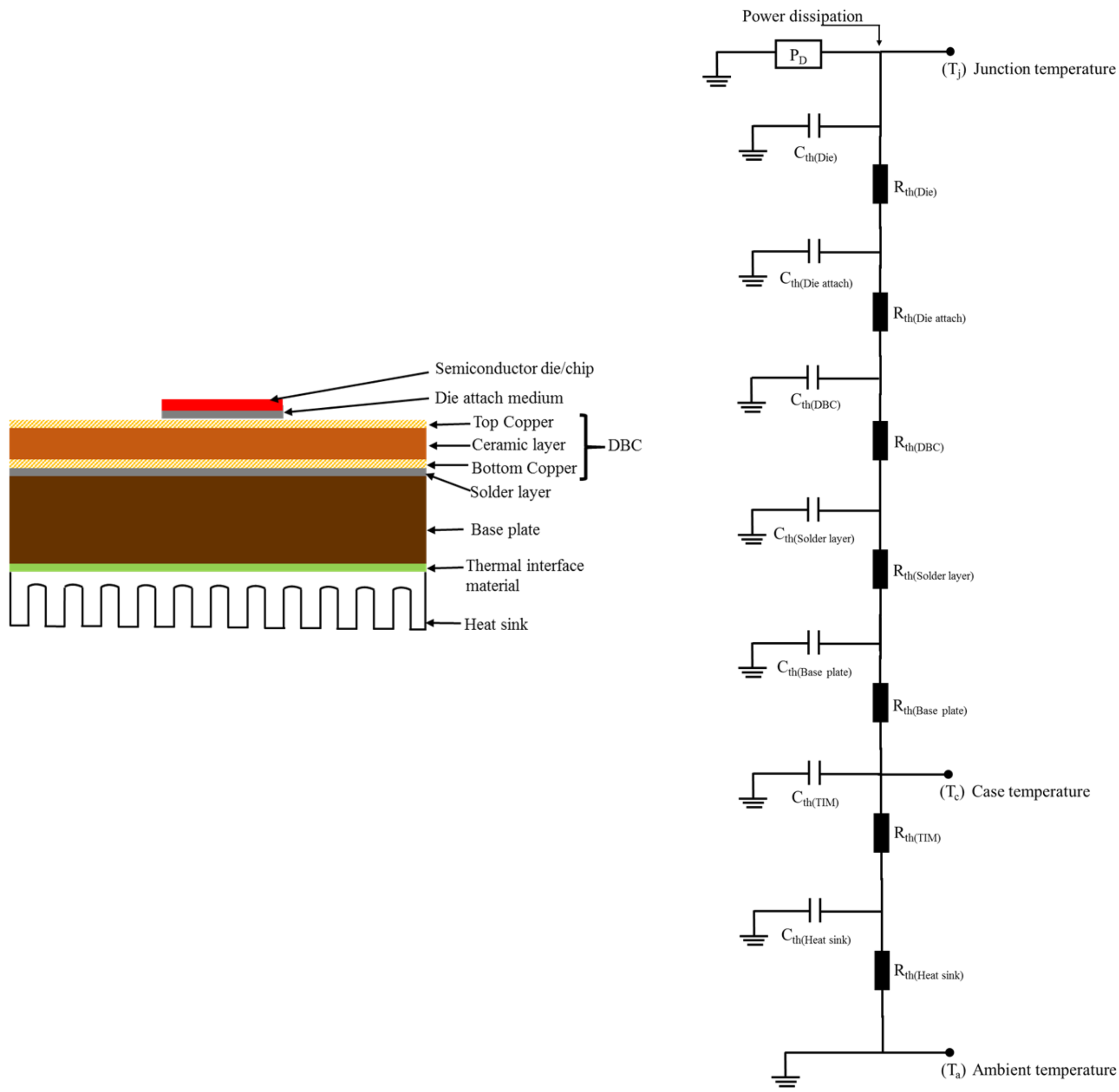


Figure 1.7: Cauer thermal network

This approach of thermal modelling provides accurate simulations as it utilises material layer properties unlike the Foster thermal model. Thermal resistance is calculated as shown in equation (1.5), whereas thermal capacitance is calculated using equation (1.9) where c_p, ρ & V are specific heat capacity, density and volume of each layer.

$$C = c_p.\rho.V \qquad (1.9)$$

1.6.1.3 Comparison between Foster and Cauer thermal network

Cauer thermal network provides a physical representation of the system; However, to utilise the best of the Cauer thermal model circuit certain simulation tools are required. When Cauer thermal network is used along with the circuit simulation tools for thermal calculation, it provides accurate results for any complex thermal model with time varying, multiple heat

sources with arbitrary power inputs. Foster network is mathematically easier to perform thermal calculations. Even though only junction temperature has physical representativeness in the Foster network, if transient response curves are measured under certain ambient environmental conditions, then it could be transferred onto Foster model to predict the temperatures under varying power level. Even complex thermal models can be constructed using Foster model. Cauer thermal network does not require measured data to calculate the thermal resistance of the system as it uses material layer properties. Whereas, Foster network require measured data and it does not interpret the layer material properties for calculating the thermal resistance.

1.6.2 Finite element analysis

The finite element method (FEM) is a numerical technique for finding approximate solutions to boundary value problems for partial differential equations. It is also referred to as finite element analysis (FEA). It subdivides a large problem into smaller, simpler parts that are called finite elements. The simple equations that model these finite elements are then assembled into a larger system of equations that models the entire problem. Three dimensional (3D) approach in finite element analysis predicts more accurate results close to the experimental values. Finite element analysis involves dividing a body or a system into smaller elements allowing equations governing the system physics to be solved. The biggest challenge in using the FEM thermal simulation tools lies in constructing appropriate geometry and finding thermal parameters to predict results accurately. Thermal parameters required for the simulations are Density, Specific Heat Capacity and Thermal conductivity. These parameters are temperature dependent and it exhibits significant variation over temperature ranges from 25°C to 250°C and it’s important to include these parameters for predicting accurate results[8]. Advantages of FEM thermal simulation tool are summarised below,

- 3D finite element analysis provides a three dimensional thermal approach in solving thermal models unlike, Cauer or Foster thermal model which uses one dimensional thermal approach.
- Complex thermal model with multiple heat sources are easy to be modelled using finite element analysis.
- Temperature dependent parameters such as density, specific heat capacity and thermal conductivity can be used with the thermal modelling simulation in a tabular form for varying temperature ranges.

- Thermal contours and temperature distributions results with hotspots can be performed using finite element modelling and moreover, temperature differences between each individual thermal layers can be identified using temperature probes for thermal calculations.

1.7 Reliability

The main aim of thermal management in power electronics packaging is to ensure the reliability of a system. Reliability can be defined as a probability measurement of adequate system performance, in which the system must function without failure when subjected to certain operating conditions. The reliability of power electronics devices is widely characterised using a bath-tub curve[1] with three distinct phases as shown in Figure 1.8. The first phase in a bath-tub curve corresponds to burn in-time phase in which the failures are caused due to the component malfunction, manufacturing defects, etc.

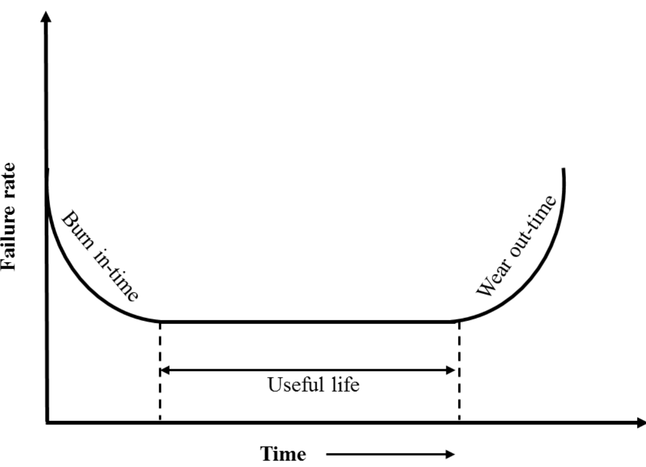


Figure 1.8: Bath tub curve[1]

The subsequent phase is the useful life or normal life period since the failure rate throughout this phase is much lower compared to the infant mortality. Wear-out time period is the final phase in which the failure rate is higher due to aging and fatigue of the components.

1.7.1 Failure mode

The main failure rate in electronics are due to overheating[9], occuring when the electronic component is operated constantly above the maximum junction temperature limit. Device junction temperature has high influence on the reliability and semiconductor device operation[1]. The materials with different co-efficient of thermal expansions are bonded together in electronic packages, they expand with respect to temperature variation and result in

thermal strain and stress between the layers. The induced thermo-mechanical stress leads to failure of the electronic component; wire bond lift off and solder layer degradation, crack generation and propagation are some of the common thermo- mechanical failures[10-12].

1.8 Semiconductor Power loss

Ideal power semiconductor switch should turn on and off instantly, should have infinite impedance in the off state and exhibit zero resistance whilst operating in the on state. However, these ideal characteristic are not achievable in semiconductor devices. The semiconductor power loss can be divided into three sections conduction loss, switching (Turn ON and Turn OFF) loss and off state loss. When the semiconductor switch is turned off the off state losses are very low due to the negligible small leakage current and is generally neglected under normal operating temperature conditions. Conduction loss occur when the semiconductor device is fully turned on, Figure 1.9 shows the IV characteristic of an 25A 1200V IGBT[13] (see Appendix 1). The conduction loss is calculated using (1.10)

$$P_{conduction} = V_{ce} \times I_c \qquad (1.10)$$

Where, V_{ce} is corresponding onstate voltage drop and I_c is the collector current.

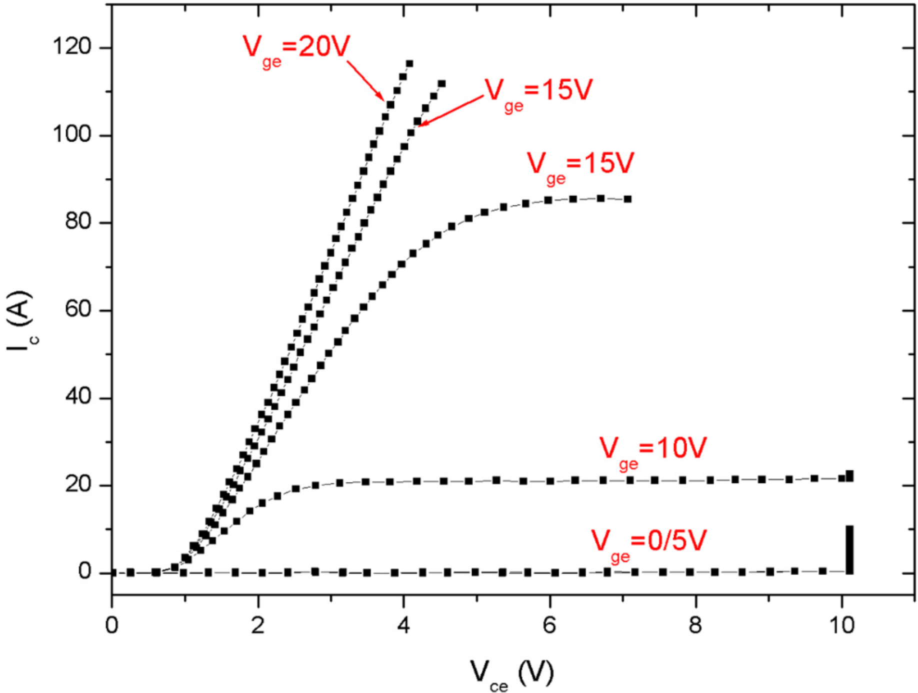


Figure 1.9: IGBT I-V characteristics

Figure 1.9 represents I-V characteristic of IGBT power semiconductor switch representing the voltage and current relationship during the ON state of the semiconductor switch. Power dissipation during conduction mode is calculated by multiplying the on-state voltage (V_{ce}) to its corresponding on-state current. Switching losses occur during the turn on and turn off switching events. In order to examine the switching and conduction losses in a semiconductor die, a DC-DC converter with IGBT as switching device is considered. Figure 1.10 shows a DC-DC converter operating at 50% duty cycle, the corresponding voltage and current wave form during turn on and turn off are illustrated in Figure 1.11. Red line indicates the current wave form and black line indicates the voltage of an IGBT.

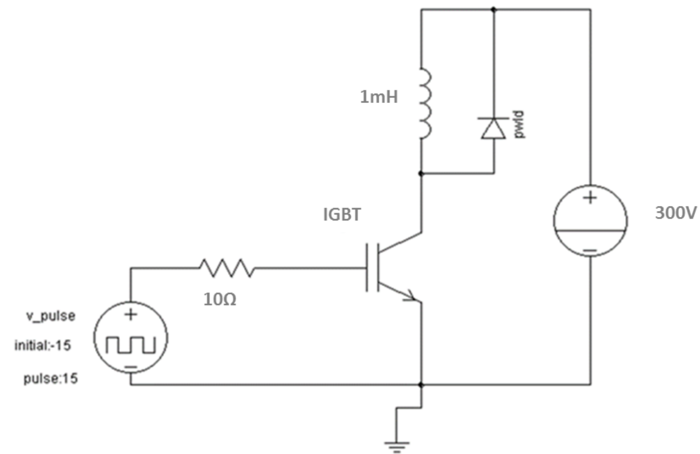


Figure 1.10: DC-DC converter

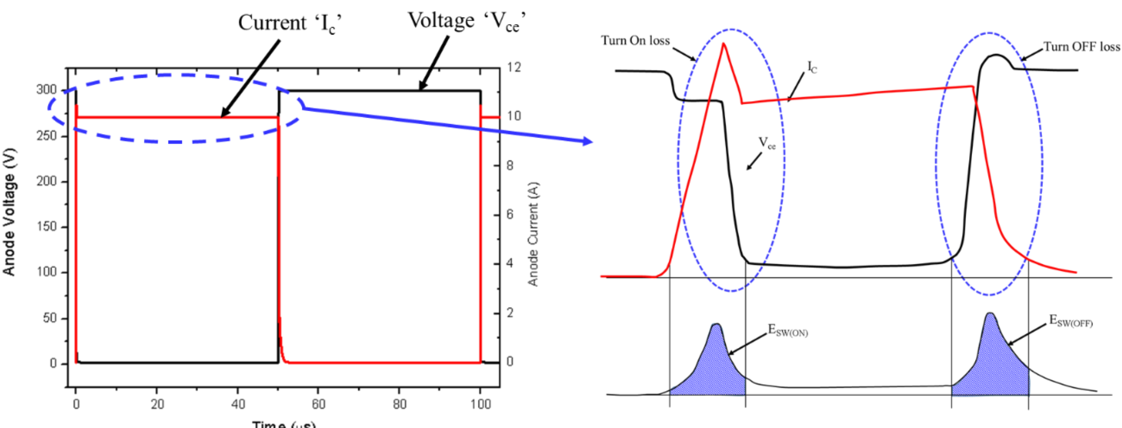


Figure 1.11: Voltage and current waveforms of IGBT

Switching losses are further classified into turn on and turn off losses and they are represented in terms of turn on energy loss (E_{on}) and turn off energy loss (E_{off}) which is represented as power loss integrated over a switching time. Turn on losses occur when the semiconductor

device is switched from its OFF state to ON state. Whereas, the turn off loss occur when the semiconductor devices is switched from its ON state to OFF state. Switching losses are frequency dependent. When the current and voltage are constant the $E_{sw(ON)}$ and $E_{sw(OFF)}$ are identical for each turn on and turn off event, the average switching loss can be calculated by summing the $E_{sw(ON)}$ and $E_{sw(OFF)}$ and multiplying it over the frequency as shown in equation (1.11)

$$P_{SW} = F_{sw}(E_{sw(ON)} + E_{sw(OFF)}) \qquad (1.11)$$

Where, Fsw is the switching frequency; total power loss is the sum of conduction loss and switching loss times the percentage of duty cycle.

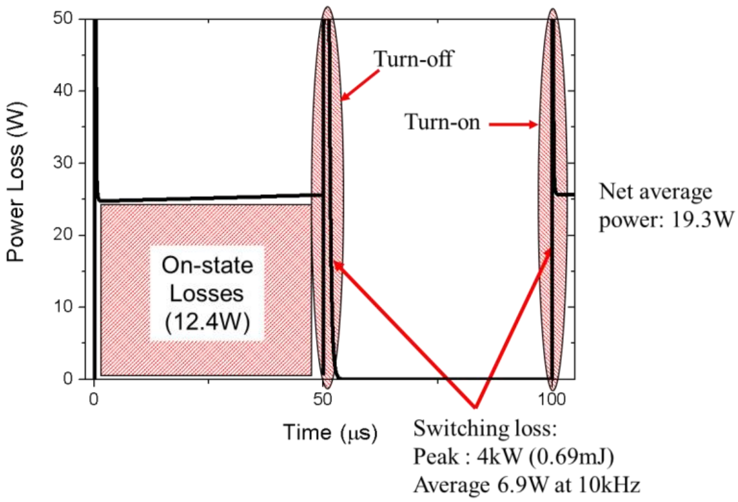


Figure 1.12: Instantaneous power loss per cycle

Figure 1.12 shows the instantaneous power loss per cycle at 10kHz switching frequency for a DC-DC convertor using an IGBT device as depicted in Figure 1.10, these power loss are observed as thermal energy and they must be dissipated whilst maintain the junction temperature below its maximum value.

1.9 Thermal energy and power density

The power loss from the semiconductor die are observed as thermal energy. Power density is directly influenced by the power loss, for example, considering an 25A 1200V IGBT[14](see Appendix 2) the total power loss at different switching frequency is shown in Figure 1.13 for a DC-DC converter at a fixed duty cycle.

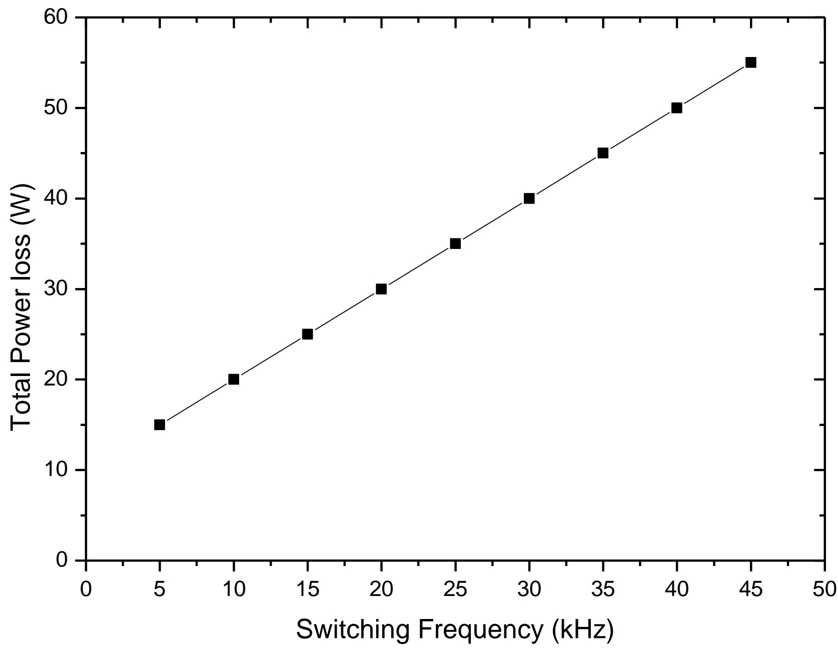


Figure 1.13: Switching power loss

The power loss increases with switching frequency. The required heat sink thermal resistance at power losses of 17, 23 and 30W were calculated using equation (1.6) for worst case condition with maximum junction temperature (T_j) 150°C and a 60° ambient temperature (T_a). Figure 1.14 shows the calculated heat sink thermal resistance and the corresponding heatsink length. The heat sink thermal resistance required decreases with increase in power loss whereas, the heat sink size increases with power loss.

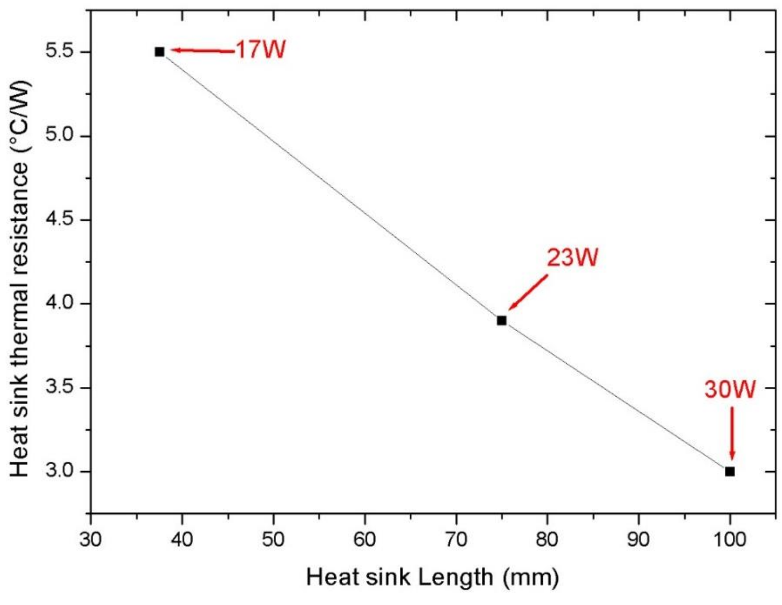


Figure 1.14: Heat sink thermal resistance and heat sink length

1.10 Thesis structure

This thesis addresses the thermal management and reliability concerns of power semiconductor device technologies like Silicon and wide band gap semiconductors (SiC and GaN) right from die level to system level packaging designs for discrete and power module packages. The evolution of electronics packaging with different mounting and interconnect techniques available for conventional for discrete and power module packaging are summarised and discussed in Chapter 2. Moreover, summary of different interconnect technologies with its advantages and disadvantages are also detailed. Comparison of thermal performance of Silicon and Silicon Carbide power semiconductor dies mounted on Polycrystalline Diamond (PCD) and Aluminum Nitride (AlN) substrates for a traditional wire bond are shown. Detailed simulation and experimental analysis techniques were performed to measure the junction to case thermal resistance ($R_{th\ (j\text{-}c)}$) under steady state and transient conditions. The thermo-mechanical reliability of PCD and AlN substrates were analysed using thermal cycling test using ANSYS structural tool to examine the stress, strain, safety factor and life cycle fatigue. The thermal performance of PCD substrates were further analysed for next generation semiconductor technologies and silver sintering die attach. Polycrystalline diamond has shown improved thermal performance over the conventional insulators in DBC substrates from Chapter 3. Thermal performance of PCD insulator on DBC substrate was further enhanced by using direct liquid cooling technique, micro fins were embedded on to the bottom copper of the DBC substrate with PCD as ceramic layer. This reduces the number of thermal layers in the system compared to the conventional one and in turn increase the thermal performance of the overall system. Moreover, the high thermal conductivity of PCD can be utilised efficiently by using direct cooling technique. An Empirical model was used to analyse the thermal performance of micro pin fins geometries and thermo-hydraulic parameters were varied accordingly to find the optimal circular micro pin fin diameter and length. Thermal management and packaging solutions for the next generation wide band gap semiconductors such as GaN is described in Chapter 5. Comparison of face up and flip chip thermal performance of GaN on Sapphire, Silicon and 6H-SiC substrates in a T0-220 package system is presented. Detailed thermal simulation results were analysed using ANSYS® thermal tool moreover, the effect of package parasitic for flip chip and face up mounted on T0-220 package were observed. Finally, a summary of all chapters with concluding remarks and suggestion for future work are described in Chapter 6.

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CHAPTER 2:   SEMICONDUCTOR PACKAGING

2.1 Introduction

Essentially, power electronics packages deliver device protection, mechanical support, cooling, electrical connection and electrical isolation for electronic components. Packaging technology is an important field next to power devices in determining the overall performance of single chip or multichip power packages. Power-semiconductor manufacturers have been focusing on electronic power conversion research effort by moving towards high-frequency operation, which results in improved converter performance, higher power density and decrease of system weight and cost. This typically results in pushing the limits of present packaging technologies, which in turn indicates packaging as the dominant technology limiting the rapid growth of power electronics applications. The main drives for semiconductor development are on-state resistance reduction, miniaturisation of semiconductor die, increased thermal performance and thermo-mechanical reliability. Power density can be identified in terms of Silicon to foot print ratio[1], which is semiconductor die (Silicon) divided by total foot print ratio.

In this chapter an overview of the evolution of semiconductor packaging with different mounting and interconnect technologies are discussed. Further, the advantages and disadvantages of various mounting and interconnect technologies are analysed and discussed.

2.2 Single chip/Discrete packages:

Through hole and surface mount packages are the two main classifications of discrete power semiconductor packaging. Some of the through-hole packages available commercially are:

- Dual-In-Line Package
- Transistor Outline Package (T0)
- Pin Grid Array (PGA)

Whereas, surface mount packages are:

- Small Outline Package
- Quad Flat pack (QFP)
- Small Outline Transistor (SOT)
- Plastic Leaded Chip Carrier (PLCC)

Figure 2.1 shows a selection of through-hole packages whereas, Figure 2.2 shows surface mount packages for power devices.

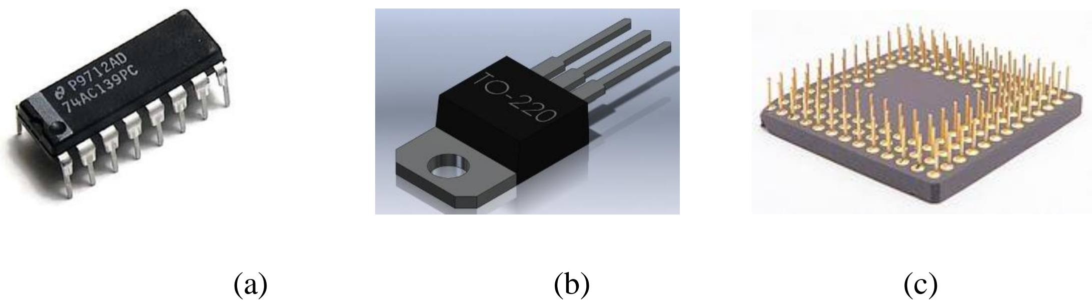


Figure 2.1: Through hole power packages[2] (a) Dual inline package (b) Transistor outline T0-220 (c) Pin grid array

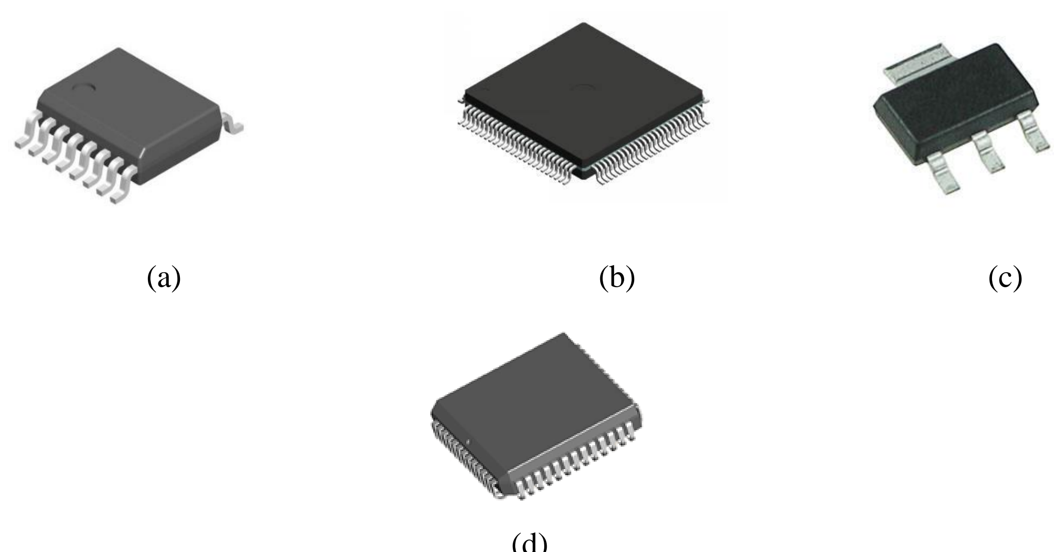
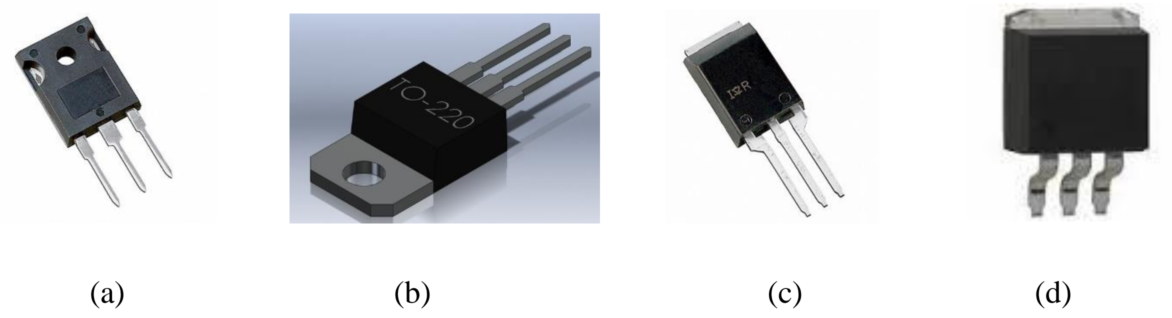


Figure 2.2: Surface mount packages[2] (a) Small Outline Package; (b) Quad flat pack (QFP); (c) small outline transistor (SOT); (d) Plastic leaded chip carrier (PLCC)

2.2.1 Through hole and surface mount packages

Some of the widely used through-hole type packages are T0. T0-247 packages are commonly used for high power level applications, whereas T0-220 packages are used for applications requiring power levels of within 50W. The commercial TO packages are shown in Figure 2.3. The advantages of TO-220 over TO-247 packages are very low thermal resistance, small in size and low cost, these advantages have made TO-220 packages to be widely used in all industrial/commercial applications. The super TO-220 / super TO-247 have higher power densities as it removes the heat sink mounting hole, extending the plastic epoxy to the outer package compared to standard equivalents. This allows twice the available die space in the same foot print area, increasing the die to footprint area ratio to approximately 30 percent. Moreover, current handling capacity of super TO-220/TO-247 are much higher when

compared over TO-220 and TO-247 packages due to its increased Silicon to foot print ratio. The main disadvantage of supper T0-220 is that it requires efficient heat sink mounting methods for attaching the device to the heat sink. TO-263 or D^2Pak is a modified version of TO-220 for high current conversion and surface mount adaptability. The TO-263 or D^2Pak provides very low on-state resistance, high power and high current handling capacity due to its low inner connection resistance and reduced package leads. The main disadvantage of TO-263 or D^2Pak is its high cost and large package area.



(a) (b) (c) (d)

Figure 2.3: TO Packages [3] (a)T0-247; (b)T0-220; (c)SuperT0-220/superT0-247; (d)T0-263/D^2PAK

Surface mount packages have been recently advancing in the semiconductor market and conventionally available is SO-8 package with Silicon MOSFET rated up to current level of 10A. Figure 2.4 shows the commercial surface mount S0 packages. The advantage of SO-8 package is ease of handling and small in size. The main disadvantage is high package thermal resistance as most of the heat flows via the cross-sectional area of anode (drain/collector) leads to the heat sink. Thin Shrink Small Outline Package -8 (TSSOP) occupies very small foot print area with less than 40% than the conventional SO-8 package. The main application of TSSOP-8 are in portable electronics due to its small in size. SOT-223 was developed to improve the thermal performance in TSSOP-8 packages. TSOP-6 and SOT-23 packages are used for low power and high power density application, the only disadvantage is its plastic moulded injection as the package occupies three times the foot print area of die.

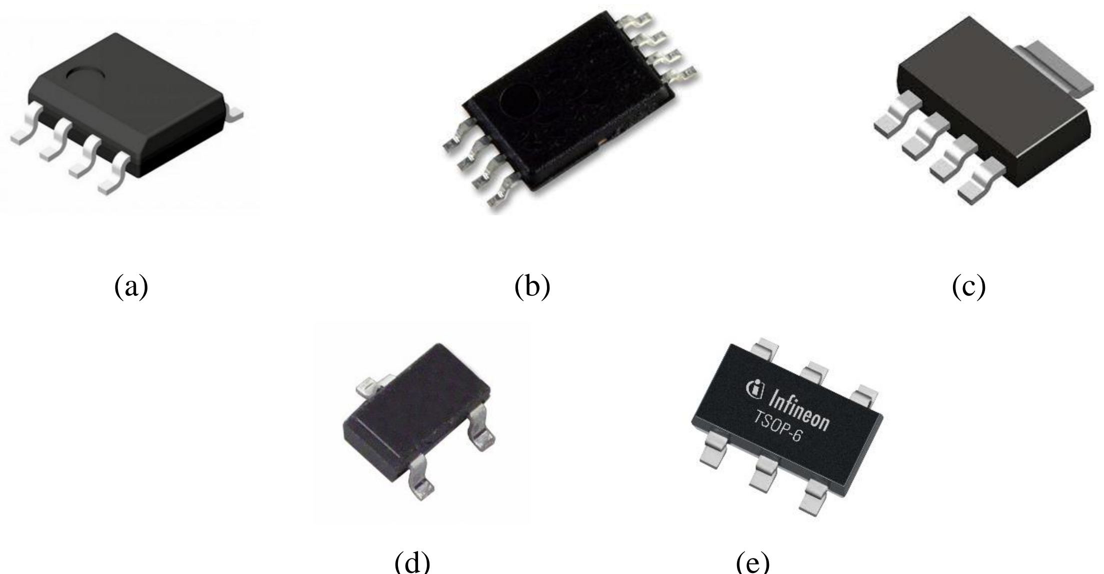


Figure 2.4: Surface mount SO package [3];(a)S0-8; (b)TSSOP-8; (c)SOT-223; (d)SOT-23; (e)TSOP-6

Leadless packaging is an advance packaging technology which reduces the overall package size by 44% when compared to TSOP-6 by eliminating the leads along the sides of the package and enhanced anode contact connection. Flip chip and ball grid array packaging are another step change in packaging technology benefiting reduced foot print with the same size as the semiconductor die. Flip chip has been emerging recently, FlipFET by International Rectifier uses true chip scale packaging and 100% Silicon-to-footprint ratio in which the semiconductor die is flipped and bumped to make the electrical interconnections. Figure 2.5 shows the Silicon-to-footprint ratio percentage for surface mount and through hole packages with respect to years. Through hole packages had higher silicon-to-foot print ratio till year 1995 and from year 1995 surface mount packages started to dominate enabling up to 100% silicon to foot print ratio.

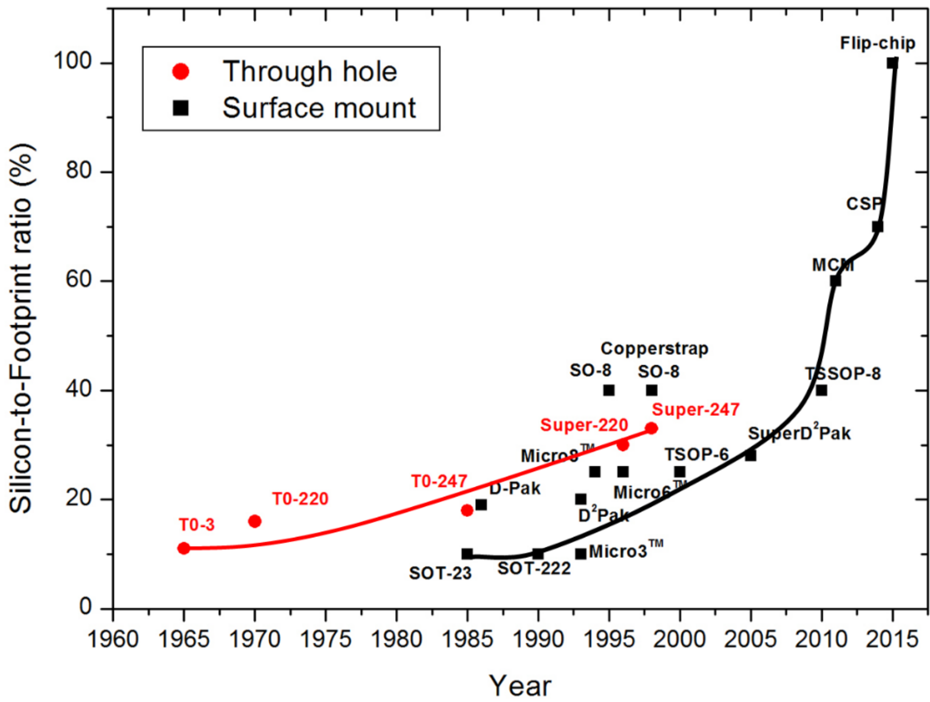


Figure 2.5: Silicon to foot print ratio for surface mount package[4]

Surface mount technologies offer high component density and high Silicon to footprint ratio at low cost when compared to through hole technologies. Surface mount technologies requires few drilling holes when used on PCB (Printed Circuit Board) and allowing both sides of the PCB to be used for efficient production. The mounting and assembling process for surface mount is significantly faster as the components are placed at the rate of 10,000 of placement per hour whereas, the placement rate for through hole technologies are less than 1000 placements per hour. Even though surface mount technique offers many advantages over through hole packages; through hole packages are widely used in many applications due to its robust bond making it more suitable in high mechanical stress environments. Through hole packages has better thermal performance, as the heat sink can be mounted directly on the back substrate of the die and bigger package size. Whereas, in surface mount packages the thermal management is quite challenging due to the smaller package size.

2.2.2 Interconnection medium

2.2.2.1 Wire bonding interconnect

Wire bonding is one of the leading interconnect technology that has been extensively used for electronic power packaging applications. Wire bonding creates an electrical connection between semiconductor die and substrate. Figure 2.6 demonstrates the conventional wire bond

package used for packing applications. On the other hand, although wire bonding technology is highly used in the electronic power technology, wire bonding technology has following few disadvantages:

- High thermal and electrical losses due to heavy and thin wires making electrical connections between the semiconductor die and the I/O leads contributing 90% of package resistance[5];
- Substantial parasitic inductance is observed at high frequencies;
- Wire bond interconnect has very poor thermo-mechanical reliability leading to device failure[6] .

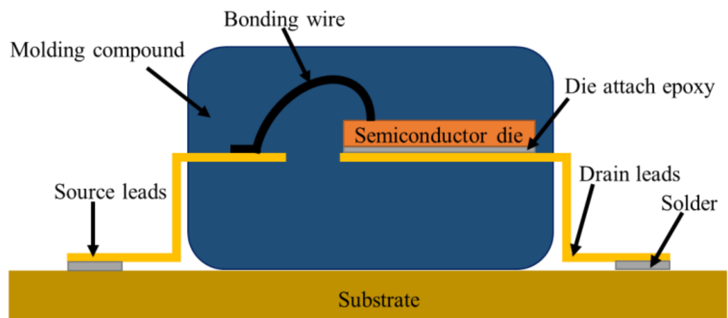


Figure 2.6: Conventional wire bond package

2.2.2.2 Power connect technology

The conventional wire bond interconnect technology was replaced by connecting the die directly with the copper lead frame[7]. Figure 2.7 shows the power connect technology, in order to achieve direct connection, the top and bottom metallisation layers of the semiconductor die was made using solderable metal to attach the lead frame. This can been accomplished using a nickel-based metallisation method above the aluminium metal pad. Few advantages of power connect technologies are the miniaturisation of package size to 50%, low package resistance of less than 1 mΩ and increased current capability. The only drawback of power connect technology is poor thermo-mechanical reliability because of the discrepancy in the coefficient of thermal expansion (CTE) between copper lead frame and Si die, which resulted in high thermal stress at the interfaces.

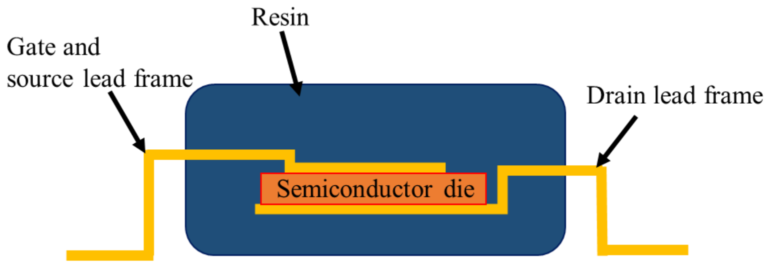
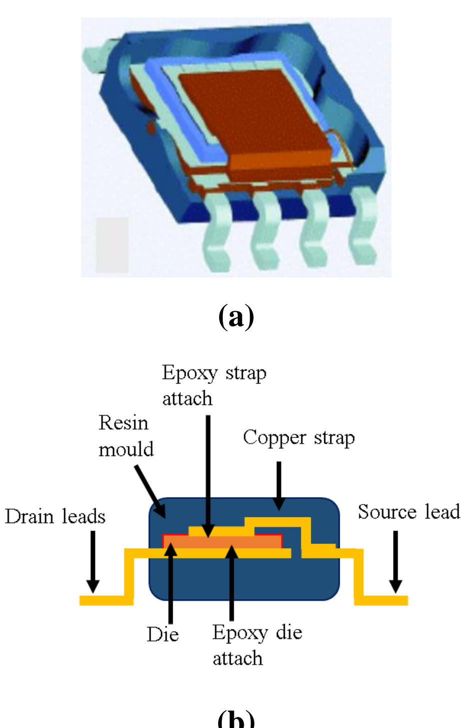


Figure 2.7: Power connect technology[7]

2.2.2.3 Copper strap technology

Copper strap technologies was developed in 1999[8] to replace wire bond interconnects. Figure 2.8 shows the cross section and schematic outline of copper strap technology. Through the copper strap technology, the junction to case thermal resistance ($R_{th(j-c)}$) can be reduced by approximate of 20% and the total package resistance can be reduced by the approximate of 61% from 1.1mΩ to 0.11mΩ when compared to the conventional wire bond technology. This is a direct result of the copper strap providing an improved thermal and electrical conduction path from die to ambient [8]. The only disadvantage of copper strap technology is reliability issues due to the CTE mismatch of copper and Silicon die which induces stress in to the epoxy layer resulting in failure.[8]



(a)

(b)

Figure 2.8: Copper strap technology (a) Outline view[8] (b) cross sectional schematic view

2.2.2.4 SO-8 Wireless package

SO-8 wireless package uses solder bump interconnect technology to connect the die to the leads as shown in Figure 2.9. The solder balls are deposited on the source and gate pads of the semiconductor die; the gate and source leads are aligned to the solder bumps. As a final process the solder bumps are reflowed to attach on to the leads. The main advantage of solder bump interconnect technology is better thermal performance as it provides a heat transfer path via source to leads due to the solder bump acting as an interface between semiconductor die and leads. The SO-8 wireless package has low package inductance and occupies less package area when compared to the conventional wire bond package. The disadvantage is SO-8 wireless package has high contact resistance and low mechanical reliability due to the high CTE mismatch between the solder bumps and the leads.

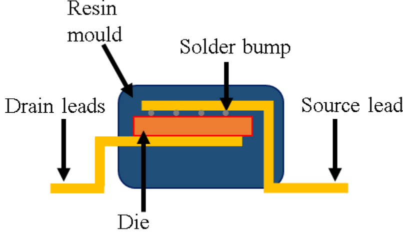
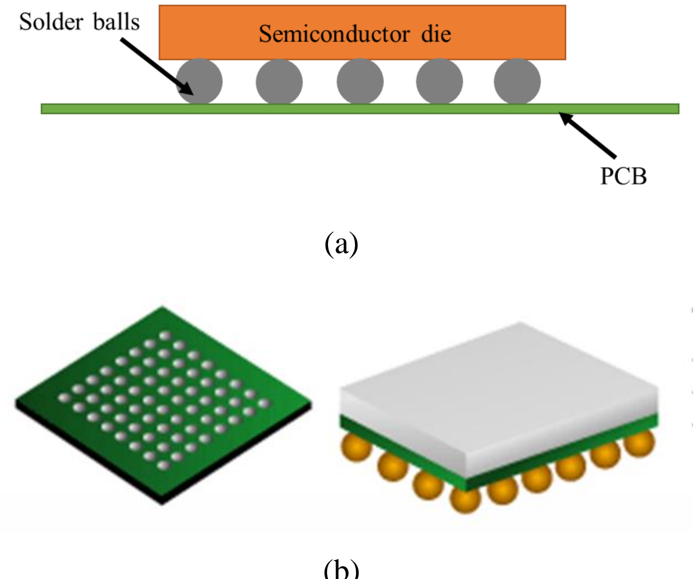


Figure 2.9: SO-8 Wireless package

2.2.2.5 Flip chip BGA MOSFET

Flip chip BGA MOSFET was introduced in the year 1999[9, 10] which benefited from low drain to source resistance ($R_{DS(ON)}$) and overcomes the drawbacks of conventional packages such as wire bond and copper straps. The package typically uses fine pitch of ball grid array interconnect mechanism which replaces the wire bond and package leads. Figure 2.10 illustrates the structure of BGA MOSFET package. The solder ball along the edges are for drain interconnection whereas the remaining solder balls are for source and gate connections. The main advantages of BGA package are:

- The BGA package contributes to a total package thickness of only 0.7mm[9] and occupies less than 50% space in the PCB area when compared to the conventional MOSFET packages with similar current and voltage ratings.
- BGA MOSFETs have reduced on-state resistance ($R_{DS(ON)}$) of 35% when compared to the SO-8 package which in turn increases the current and power handling capability.
- Due to the flip chip techniques and distinctive design it provides an efficient heat transfer path from the die junction to the case of the package via the solder balls.



(a)

(b)

Figure 2.10: BGA MOSFET package (a) cross sectional view; (b) outline view[9]

2.2.2.6 Bottomless package

Bottomless package was developed by in 2000 which was an improved version of wireless SO-8 package. The main advantage of wireless SO-8 package was its low package resistance but it has significant impact on its thermal performance. The Bottomless package was developed to overcome the drawback of the SO-8 package. Thermal performance was achieved by attaching the backside of the semiconductor die directly on to the heat sink. Figure 2.11 shows the bottomless package. The drain leads have been eliminated in bottomless package as the drain region of semiconductor die is directly contacted with bottom of package. The source and gate connection are formed using lead frame via solder ball interconnection. This unique packaging approach provides very low on-state resistance which in turn increases current handling capability upto 60% compared to similar rated semiconductor die in conventional SO-8 packages. The $R_{th(J\text{-}C)}$ (Thermal resistance junction to case) was significantly reduced from 25ºC/W [11](S0-8 package) to less than 1ºC/W, as the heat transfer path from drain to heat sink is thermally coupled by reducing the number of thermal layers from drain to heatsink.

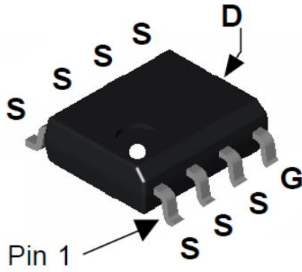


Figure 2.11: Bottomless package[11]

2.2.2.7 FlipFET

FlipFET technology was introduced in 2000 which utilises a true chip scale package by which the terminals are positioned at same side of semiconductor die in the design of solder bumps [2, 12] providing the smallest package footprint ratio. Figure 2.12 shows the FlipFET power MOSFET. As the package is same size as the semiconductor die the FlipFET technology reduces Silicon to foot print ratio by approximately 70% when compared to S0-8 packages. Moreover, the package parasitic effect and other losses associated are minimised with improved thermal performance and low on-state resistance. Another advantage of FlipFET is that it could be used with existing surface mount technology processes with standard reflow profiles.

Figure 2.12: FlipFET power MOSFET[12]

2.3 Power Electronics Module packaging

Power converter modules are implemented extensively for power conversion and motor drive applications. Figure 2.13 shows the conventional IGBT module, the vertical IGBT device structure allows the emitter and gate to be on the topside with collector on the bottom side of the die. However, for the diode the anode is on the top side and cathode is on the bottom side of the die allowing the diode to be connected in anti-parallel with respect to the IGBT. The semiconductor dies are attached on to the DBC substrate using a suitable die attach medium. DBC is a three layer structure with centre ceramic layer, Al_2O_3 or AlN, sandwiched between top and bottom copper layers. The top copper layer is etched and patterned to accommodate IGBT and diodes, wire bond interconnect is conventionally used to make electrical connections between the diode, IGBT and substrate.

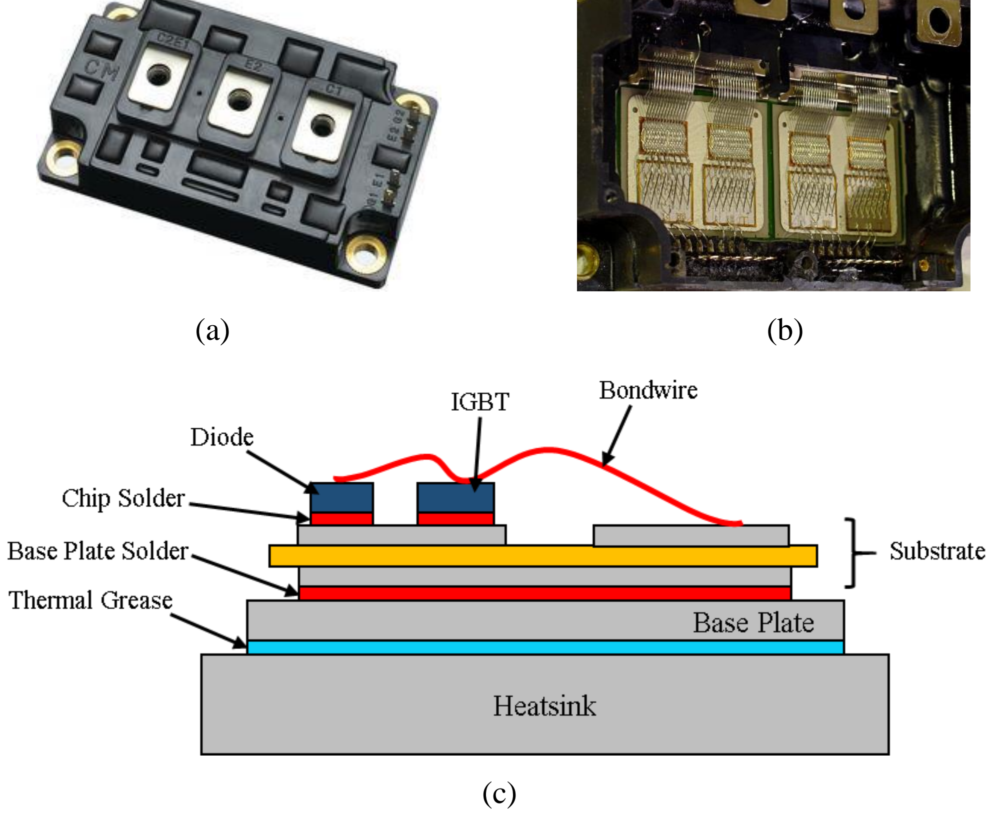


Figure 2.13: Conventional IGBT module (a) & (b) outline and detailed view [13]; (c) Schematic cross sectional view

The current handling capability of the module is increased by connecting dies in parallel, significantly increasing the wire bonds within the module resulting in high parasitic resistance and inductance. For a conventional power electronic system the power module is mounted directly on the heat sink and the control drive board is placed in adjacent to the power module, the main drawback of this kind of arrangement is high manufacturing cost, poor reliability and occupies more space due to the number of thermal layers involved. Power semiconductor manufacturers have been researching over years to improve the power density of power modules by reducing the number of thermal layers and integrating the heatsink within the power modules. There are still some boundaries associated with this kind of packaging approach as wire bond interconnection is not reliable and shows poor thermal management due to the number of thermal layers involved in transferring heat from semiconductor die to the heat sink. A system level approach of integrated power electronics module has been implemented by many semiconductor manufacturers [14-16] to enable greater integration within power modules. Hybrid packaging is a next step in power module packaging with power devices assembled in planar structure [17-20] with gate controls and protection circuits in a separate assembly and combined into a single module.

2.3.1 3D packaging of power modules

3D integration of package was developed to overcome the effect of parasitic in wire bonds and to improve the thermal efficiency by adapting multichip modules (MCM). 3D packaging is a next generation breakthrough in power modules enabling stacking the semiconductor dies on top of one another enabling high power density. The 3D packaging are primarily divided into three categories such as solder, pressure contact and thin film approaches[21]. The development of 3D power modules are still in research study due to the level of complexity involved in packaging and reliability concerns.

2.3.2 Metal Post Interconnect Parallel Plate Structure packaging technique

Metal Post Interconnect Parallel Plate Structure (MPIPPS) [22, 23] is a low cost approach using metal posts as interconnecting medium. Figure 2.14 shows the MPIPPS structure.

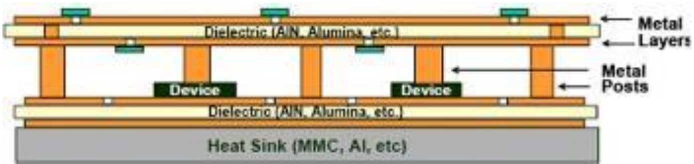


Figure 2.14: MPIPPS structure [23]

The semiconductor device is placed in between the two DBC substrates in which the copper layers are etched and patterned, semiconductor dies where attached using solder paste. Copper metal posts are used as interconnections between top and bottom DBC substrates and the semiconductor dies, eliminating wire bond interconnects. The MPIPPS package structure has many advantages

- The metal posts reduces the parasitic effect to minimum value which in turn enables large current carrying capability. Moreover, metals posts provide an enhanced thermal path for heat transfer from the die junction to the ambient: The MPIPPS packaging approach also enables double sided cooling technique for convective heat transfer which further reduces the junction to ambient thermal resistance.
- The control circuitry can be easily integrated onto the module package due to the stacking arrangement.
- The main disadvantage is high thermal stress due to two DBC substrates when compared to the conventional package, which in turn decreases the thermomechanical reliability.

2.3.3 Flip chip power module package:

Flip chip power module [24, 25] package was developed in 2000, in which the semiconductor dies were flipped and die-attached onto a high thermal conductive substrate. Figure 2.15 shows the schematic cross section of flip chip power module. The semiconductor dies are flipped and die attached on to the top copper layer which are etched and patterned to form electrical connections, a ceramic layer is used to isolate the top copper and bottom copper layers which acts a base heat sink. However, the passive components are directly soldered on to the top copper layer and the whole assembly is epoxy moulded leaving the bottom copper heat sink exposed. This packaging approach enables double sided cooling which in turn reduces thermal resistance form junction to ambient. The main disadvantage is thermo-mechanical reliability of solder bumps with difference in CTE mismatch with the semiconductor die[25].

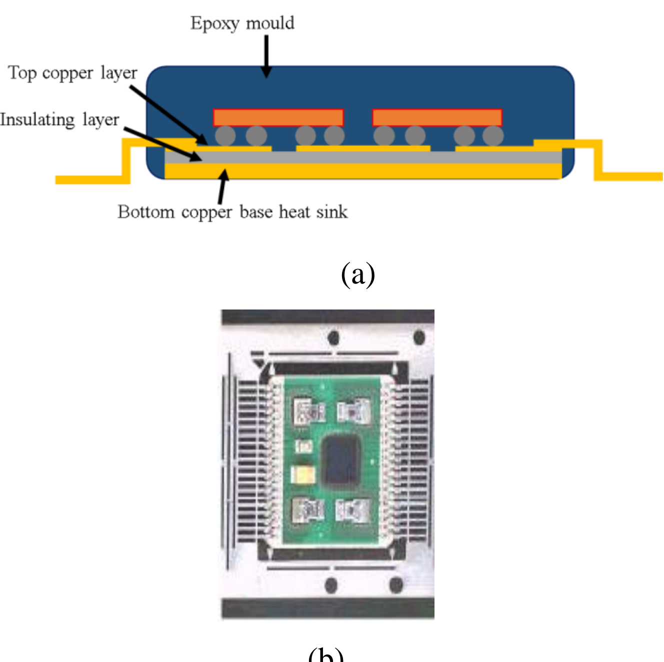


Figure 2.15: Flip chip power module(a) cross sectional schematic view (b) Detailed view[25]

2.3.4 Power overlay technology:

Power overlay (POL) technology was established in 1995 as a high density interconnect technique for multichip modules [26]. The power overlay technology uses an interconnect layer above the die and base plates. Figure 2.16 shows the schematic cross section of power overlay interconnect technology.

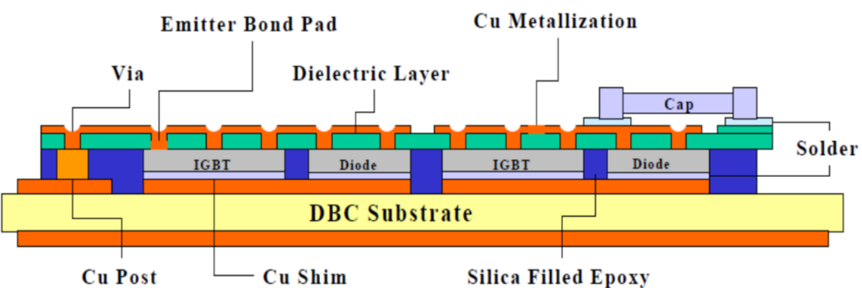


Figure 2.16: Schematic cross section of power overlay interconnect technology [26]

Kapton tape is positioned on the top surface of semiconductor devices using an adhesive. The Kapton tape is pre-etched with metallised vias which acts as an electrical path for the gate and cathode pads. The bottom side the semiconductor device are die attached on to DBC substrates using solder paste. This kind of arrangement allows to have multi-layered interconnection structure with embedded passive components and gate drive circuitry. The main pros and cons of POL interconnect technology are:

- Low parasitic effect due to the elimination of wire bond thus improving the electrical performance.
- Improved thermal performance due to the reduction in number of thermal interfaces and double sided cooling.
- High flexible options in integrating drive circuits and passives within the module package.
- Thermo-mechanical stress is high on the device interconnection layer because of the mismatch in CTE between Kapton and copper layers that results in poor reliability.

2.3.5 Pressure contact interconnect technology:

Pressure contact interconnect or press pack for IGBTs is an interconnect technology developed in 2008[27]. Figure 2.17 shows Semikron's SkiiPPack pressure contact interconnect technology, the electrical contacts between the PCB board and DBC substrate are made via C-shaped spring which provides necessary pressure. The copper alloy is used as a material in spring contact which provides good electrical conductivity. Moreover, the internal bus bar construction does not require any mechanical support as they are replaced with a plastic pressure spreader. Pressure contact is widely used in many application due to its reduced junction to case thermal resistance when compared to conventional power module (with copper base plate), as the DBC substrates are attached directly on to the heat sink.

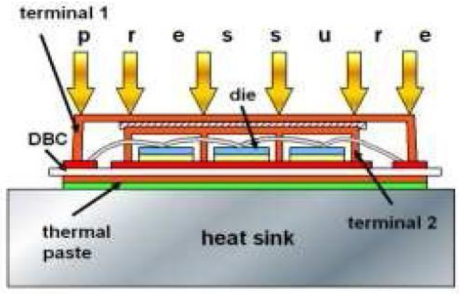


Figure 2.17: Semikron's SkiiPPack pressure contact interconnect technology[27]

2.3.6 Pressure assisted/pressure less silver sintering

Silver paste sintering is now been used widely due to its high electrical and thermal conductivity (~250 W/mK) which replaces the conventional solder paste die attach. Silver sintering requires very high temperature of >500ºC, way beyond the semiconductor device operating temperature. However, the sintering temperature profile can be reduced by applying external pressure [28-31]. Schematic setup for silver sintering process is illustrated in Figure 2.18.

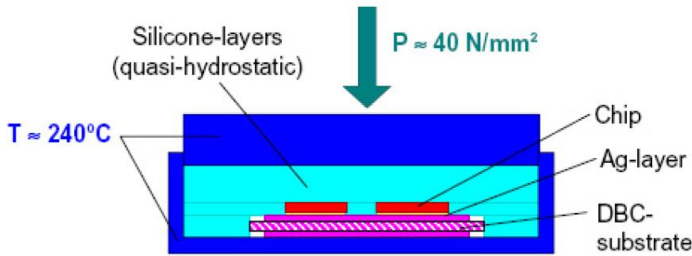


Figure 2.18: Schematic setup for silver sintering[31]

Due to advancement in technologies, pressure less silver sintering is now been used in power semiconductor die attach with the melting point of higher than 300 °C. Pressure less silver sintering has similar electrical and thermal performance when compared to pressure assisted silver sintering material, except the pressure setup needed to cure the silver sintering paste is not needed in turn minimises the process of applying pressure to the semiconductor die. Pressure less and pressure assisted silver sintering are more suitable for SiC power semiconductor devices with maximum junction temperature of 250°C and high temperature electronics.

2.3.6.1 Flexible interconnect

Flexible interconnect is a potential breakthrough in advance interconnects for power module packaging. Figure 2.19 shows the Semikron Skin technology [32], the electrical interconnections between the power device and the DBC substrate are made through a micro

via flexible PCB which is silver sintered on to the top of the die and DBC substrate. This kind of arrangement facilitates low parasitic inductance than the conventional wire bond module. Moreover, silver sintering attach on the top and bottom of the die provides a very low junction to case to thermal resistance when compared to the wire bond modules.

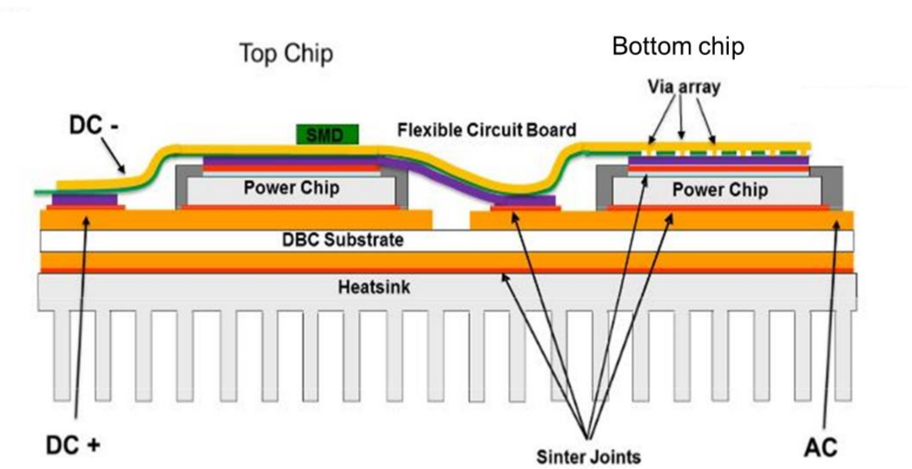


Figure 2.19: Semikron Skin technology with flexible interconnect[32]

2.4 Summary of various interconnect technologies

In discrete packaging, wire bond technology is conventionally used as an interconnection medium for surface mount and TO packages. Wire bond technology were replaced by solder bump interconnects which uses solder bump to connect the leads of the package. This in turn improved the thermal performance significantly and reduced the package resistance. The main disadvantage of solder bump technology is that the package leads act as a degrading factor subsidising to the overall resistance and power loss. More over the current handling capacity, thermal performance and over all reliability are also affected by the package leads. In order to overcome the drawbacks in solder bumps interconnections flip chip technology was developed. In Flip chip technology the semiconductor dies were flipped and solder bumped directly on to the substrate which in turn reduced the package resistance and improved the thermal performance compared to the other interconnect methods. Commercially, wire bond interconnect is still widely used in discrete packages and seems to dominate due to its low packaging cost and less complexity. Flip chip as an alternative for wire bond interconnect has emerged recently and been used commercially on surface mount and through hole packages. The flip chip interconnect has attracted the next generation wide band gap semiconductor technologies such as SiC and GaN were high power density and high efficiency are of a major concern.

In power module packaging, wire bond interconnect with copper base plate is used conventionally in wide range of applications due to its low cost and less complexity. The 3D, flip chip and power overlay interconnects in power modules are still under study level and are not available commercially yet. The pressure contact and silver sintered interconnects are an alternative for conventional power module and are available commercially for many applications. Improved thermal performance by removing the base plate layer and replacing solder die attach with silver paste, high power density, high efficiency are the main advantages of pressure assisted/pressure less silver sintered when compared over the conventional power module interconnect. Every chip level interconnect technology has its own advantages and disadvantages, it's impossible to achieve a unique interconnect technology which fits for all applications. Table 2.1 shows the advantages and disadvantages of various chip level interconnect technologies.

Table 2.1: Summary of various interconnection medium

Parameter	Material used	Advantages	Disadvantages	Application
Wire bond	Al wire or Au wire	Low cost; Ease of interconnection	High package parasitic; Poor thermal management; Difficult for Integration	Commercially used in most of the applications
Metal Deposition	Ti, Ni, Cr, Cu, Ag, Mo, Au, etc	Good electrical and thermal performance; 3D integration of structure	High manufacturing cost due to precession; Low thermo-mechanical reliability; High parasitic capacitance	Multi chip power modules
Flip-chip	SnPb or SnAg(lead free) solders;Au-stud bumps	Good electrical and thermal performance; 3D integration of structure; High density	Low reliability due to CTE mismatch; Potential lead contamination	FlipFET's; BGA; Bottom less; Power connect
Conductive epoxy curing	Ag or Au filled epoxies	Good reliability; 3D integration of structure;	Not suitable for high temperature packaging; Poor electrical and thermal performance	DirectFET; CoperStrap
Press pack	N/A	Good overall performance	High cost	High power application
Pressure-assisted/pressure less silver sintering	Micro/nano silver paste	Good overall performance	Technology is at its initial stages; High cost	Used in large area die attachment applications

The thesis focus on improving the thermal performance, thermos-mechanical and electrical reliabilities of different power semiconductor device technologies like Si and wide band gap semiconductors (SiC and GaN) on commercial discrete and power module packages; with different mounting and interconnect techniques. Next chapter discusses the possible techniques to improve the thermal performance and thermo-mechanical reliability on commercial power module packages.

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CHAPTER 3: THERMAL PERFORMANCE OF ALN AND PCD SUBSTRATES

3.1 Introduction

In this chapter, a comparison of steady state and transient thermal performance of Silicon power semiconductor dies mounted on Polycrystalline Diamond (PCD) and Aluminium Nitride (AlN) substrates are presented. The requirement for this work comes from increasing the thermal performance in a conventional wire bond packaging which uses aluminium nitride as an electrical insulating layer. The overall thermal resistance reduction will be an improvement on the conventional wire bond packaging design by changing the ceramic layer material from aluminium nitride to polycrystalline diamond due to the higher thermal conductivity of PCD (2000W/mK) than AlN (170W/mK).

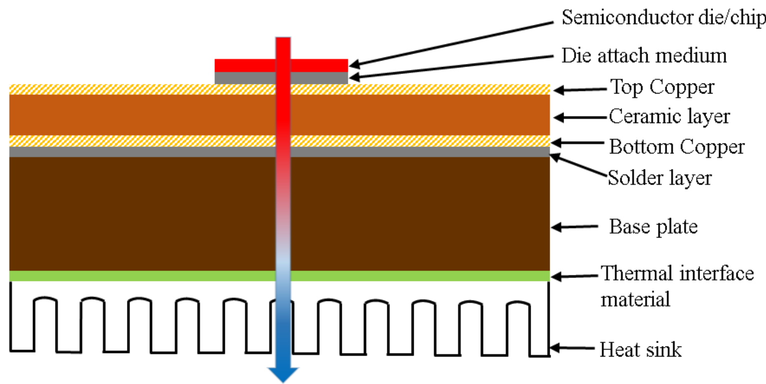

Figure 3.1: Typical cross-section of a conventional wire bond package

Power electronics is a continuously evolving and challenging field. Systems continue to demand increasing functionality within a decreasing packaging volume whilst maintaining stringent reliability requirements. This typically results in higher volumetric and gravimetric power densities, which requires an effective thermal management solutions to maintain the junction temperature below its maximum rating. The thermal design of a package depends upon the semiconductor die size, power dissipation, junction and ambient temperatures as well as cost constraints. With the focus of semiconductor engineering to increase die current densities, this makes the thermal design more challenging, due to its associated increase of heat flux. With the increase in power dissipation and reduction in the size, the growth in power density is expected to increase further over the next decade[1, 2]. The increasing power density underlines the importance of thermal management solutions in determining the future semiconductor device technology.

A typical cross-section of a conventional packaging system is shown in Figure 3.1. Corresponding layers from die junction to heat sink ambient helps in thermal dissipation and getting the heat effectively out from the semiconductor die. The die attach medium should be both electrically and thermally conductive and helps in attaching the semiconductor die on to the top copper of the DBC substrates. DBC is a three layer structure with ceramic layer sandwiched between the top and bottom copper layers. Top copper layer is both electrically and thermally conductive. Ceramic layer acts as an electrical insulating and thermally conductive. Bottom copper layer is used to neutralise the co-efficient of thermal expansion (CTE) mismatch between the top and bottom copper layers. The DBC is attached on to the baseplate using a solder layer. Base plate acts as a heat spreader for efficient thermal dissipation, the base plate is attached on to the heat sink ambient using a thermal interface material of good thermal conductivity. Figure 3.2 shows the thermal resistance contribution of each layer.

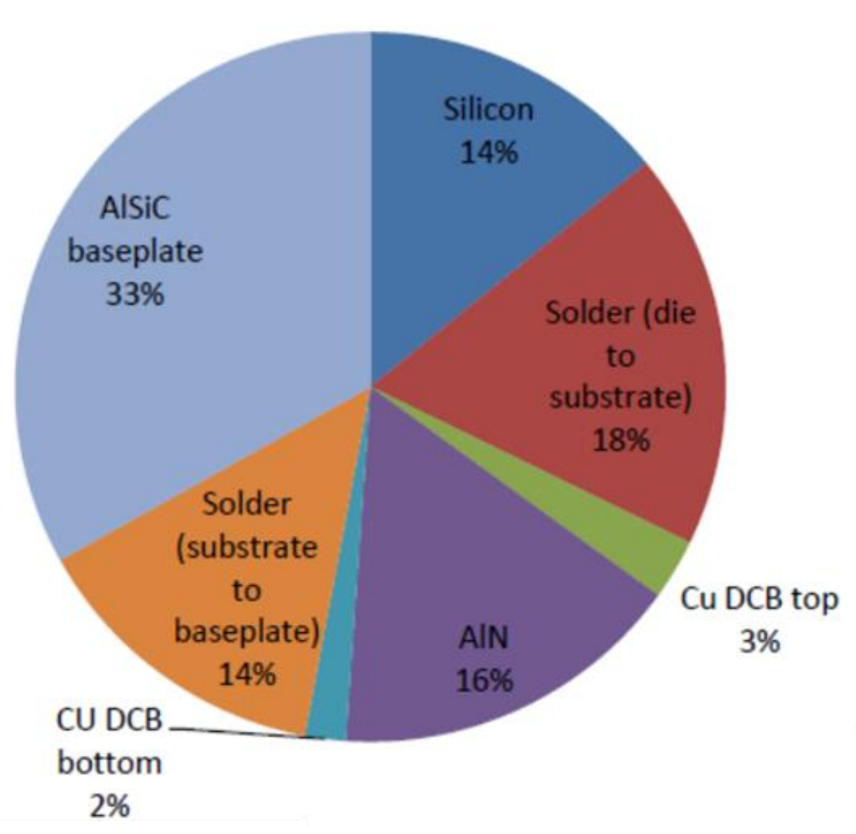

Figure 3.2: The thermal resistance distribution in a conventional power module

The base plate contributes approximately 33% of the total thermal resistance, due to the advancement in high power density packaging the base plate layer can be removed and the Direct Bonded Copper (DBC) is attached directly on to the heat sink using pressure contact technology [3] which reduces the number of thermal layers and overall thermal resistance. Figure 3.3 shows the schematic cross section of high power density packaging module, dies are arranged on the top metallisation layer of a DBC substrate.

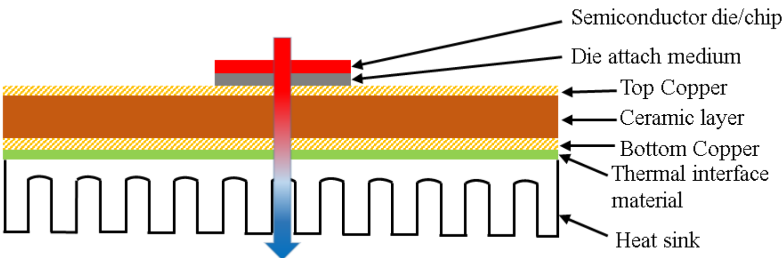

Figure 3.3: Schematic cross section of high power density module without the base plate

During operation thermal losses within the semiconductor need to be removed from the system through the substrate to the heat-sinking medium. The ceramic layer contributes high thermal resistance about 16% next to the solder layer as shown in Figure 3.2. Therefore moving towards a material with a higher thermal conductivity, significant advantages in terms of power density can be achieved [2]. Within the power electronic module, materials with different mechanical properties are attached together. These materials have dissimilar Coefficients of Thermal Expansion (CTE) which induce thermal stress on the structures and leads to thermal fatigue and ultimately failure of the packaging [4-7]. A precise assessment of thermal stresses on the structures plays a significant role in the design and reliability of power semiconductor packaging.

Table 3.1: Mechanical and thermal properties of the common materials at 25°C used in power electronics packaging[5, 6, 8]

Parameter	Poly-crystalline diamond	AlN	Copper	SnAg	Si
Thermal conductivity (W/mK)	2000	170	390	53	140
CTE (ppm/K)	1	4.5	18	23	4
Dielectric strength (kv/mm)	100	17	-	-	-
Specific Heat capacity (J/Kg.K)	516	740	390	218.9	710
Density ($g.cm^{-3}$)	3.5	3.26	8.96	7.39	2.32
Youngs modulus (Pa)	1.22e+12	3.3e+11	1.1e+11	4.59e+10	1.3e+11
Poisson ratio	0.2	0.24	0.34	0.4	0.064
Bulk modulus (Pa)	4.42e+11	2.1e+11	1.4e+11	5.61e+10	9.76e+10
Shear modulus (Pa)	4.78e+11	1.31e+11	4.8e+10	2.02+10	5.1e+10
Tensile yield strength (Pa)	6e+10	2.7e+08	2.8e+08	2.78e+07	7e+11
Compressive yield strength (Pa)	1.65e+10	2.7e+09	2.8e+08	3.12e+07	7e+11

Table 3.1 compares the mechanical and thermal properties of the common materials at 25°C used in power electronics packaging [5, 6, 8]. Common materials used for the DBC electrical isolation layer are Aluminium Nitride and Alumina. In terms of thermal conductivity, hardness, dielectric strength, tensile strength, density and CTE Polycrystalline Diamond seems to be the potential material for DBC substrates.

The Cauer Model is a realistic physical representation of the transient thermal behaviour[9]. With the appropriate knowledge of the material properties of the layers and the module construction it is possible to create such a model though the assumption of heat-spread is critical and thicker layers might need to be divided into several R/C terms. Figure 3.4(a) shows the Cauer thermal model of power module from junction to ambient. The dashed lines represent the thermal resistance (junction-case) $R_{th(j-c)}$ (Figure 3.4 (b)) containing semiconductor die, solder layer, top copper layer, ceramic layer and bottom copper layer.

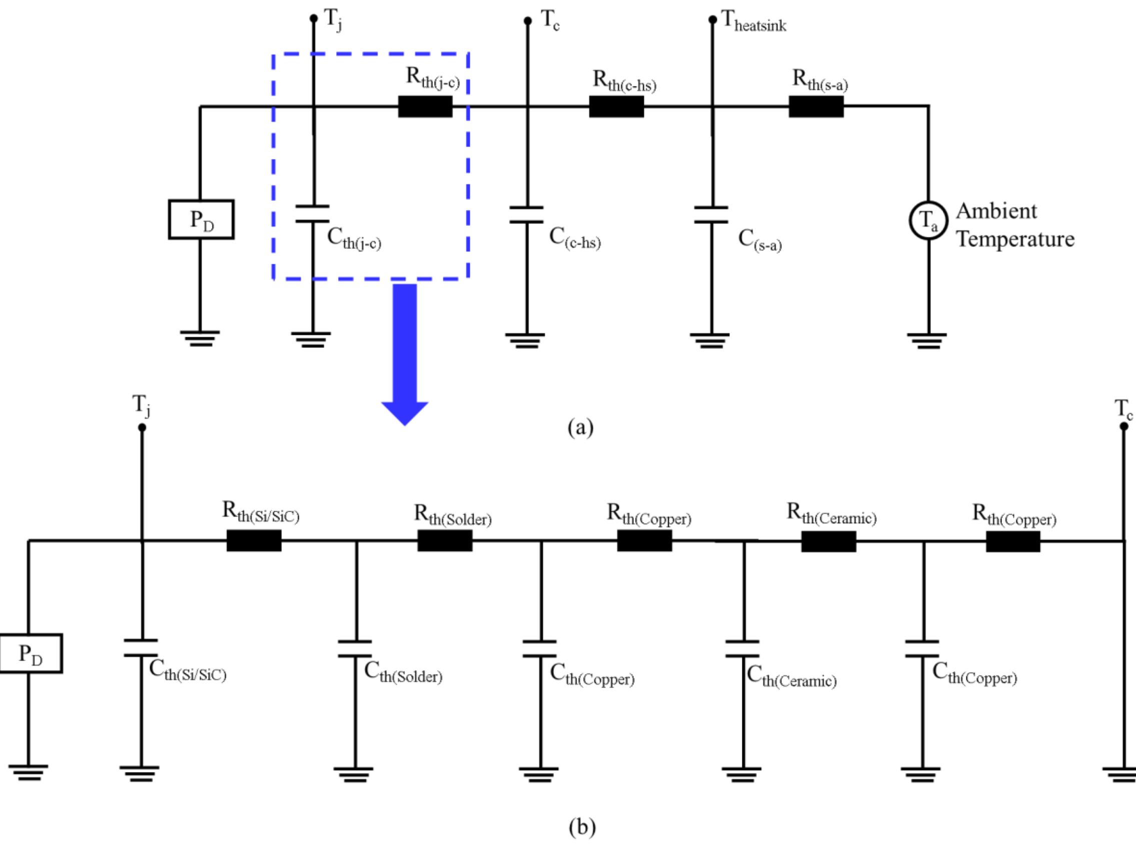

Figure 3.4: Cauer thermal model of a power module cross section

Numerical analysis of AlN and PCD substrates were presented in [10] which demonstrated that PCD substrate shows improved thermal performance. This chapter presents experimental results for Silicon dies attached to PCD and AlN substrates. Section 3.2, 3.3 and 3.4 discusses the selection of material and details the test rig used to obtain the experimental results. Section 3.5 presents measurement results for the material under steady state, transient conditions and thermal cycling reliability of PCD and AlN tiles whereas, Section 3.6 studies the next generation device technologies performance over PCD substrates. Finally conclusion are presented in Section 3.7.

3.2 Selection of materials

3.2.1 Power semiconductor Device

Semiconductor device technology used is Silicon, 25A 1200V rated Infineon IGBT4 [11] dies were selected as the power devices for this work (see Appendix 1). The die size of 5mm x 5.5mm with Nickel Silver metallisation on the backside and Aluminium on the top with a maximum junction temperature of 150°C, Figure 3.5 shows the IGBT die.

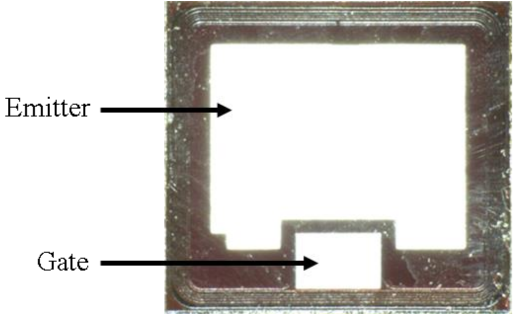

Figure 3.5: IGBT die

3.2.2 Die attach medium

The die attach medium acts as an interconnect material between the semiconductor die and the substrate. Conventionally lead free solder paste is used as the die attach medium, by moving towards silver sintering would increase the thermal performance because of the higher thermal conductivity in comparison with the conventional lead free solder. The main disadvantage of silver sintering is its high curing temperature and pressure sintering required for die attachment process and high cost. SnAg (lead free) from SynTECH-LF(see Appendix 4) [12] was used as a die attach medium. Combination is Sn (96.5)/Ag(3.0)/Cu(0.5), the temperature profile used for die attach is shown in Figure 3.6.

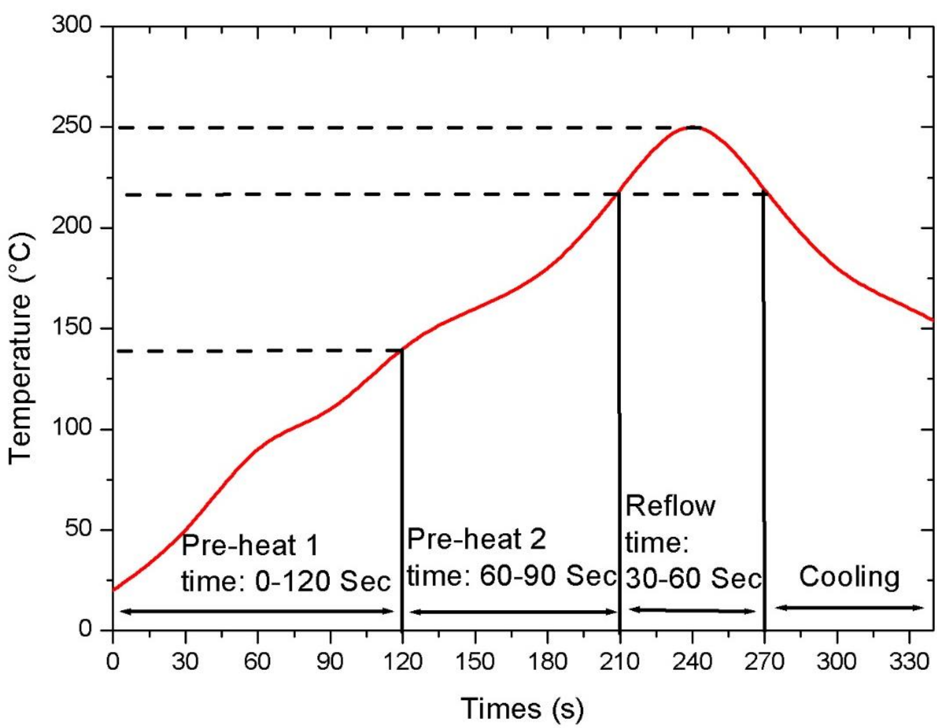

Figure 3.6: Temperature profile for lead free solder[12]

3.2.3 DBC Substrates

DBC is a three-layer structure in which two copper conductors are electrically isolated from each other by a ceramic [13], as shown in Figure 3.7.

Figure 3.7: Schematic cross section of DBC

Commercially Alumina (Al_2O_3), Beryllium oxide (BeO) and Aluminium nitride (AlN) are used as ceramic layers; for a majority of applications beryllium oxide is avoided due to its toxicity. From these materials alumina is generally used for cost sensitive products whereas aluminium nitride is targeted towards high performance and high reliability applications due to their superior thermal properties. Polycrystalline diamond is also an attractive substrate option due to its superior thermal conductivity, dielectric strength and hardness. Dielectric strength refers to the maximum voltage that can be applied to a given material without causing it to break down, usually expressed in volts or kilovolts per unit of thickness.

The main advantage of DBC substrates are,

- DBC is a conventional substrate widely used in power modules due to its low cost. The copper and alumina bonding acts as one piece of material through a coefficient of thermal expansion (CTE). The corresponding CTE is lesser compared to the CTE of pure copper and equivalent to the CTE of alumina (ceramic) [13].
- The thick copper layer enables an effective heat distribution for the power devices. 100nm gold is flashed on the top and bottom copper layers to make corrosive resistant and Ni layer of 100nm thickness is used for strengthening the wire bond pads.

The DBC substrates are designed to accommodate one switching device along with an anti-parallel diode. AlN DBC were manufactured by Curamik® Electronics and PCD manufactured by Element Six are used as a substrate comparison. The AlN tile measures 60mmx22mm whereas the PCD was 29mmx25mm. The top copper layer is etched to isolate the gate, collector and emitter terminals. Figure 3.8 and 3.9 shows the PCD and AlN substrates. The thicknesses of the two DBC substrate systems with Cu/PCD/Cu of 100/500/100 μm for PCD whereas Cu/AlN/Cu of 200/630/200 was used for AlN.

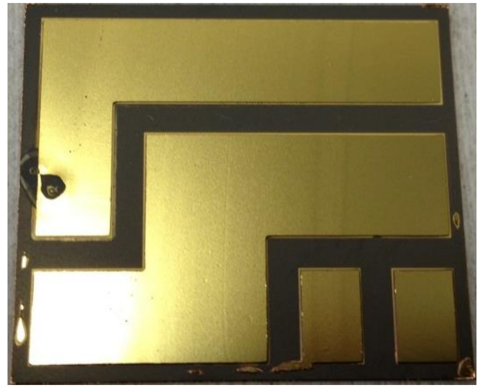

Figure 3.8: PCD substrates

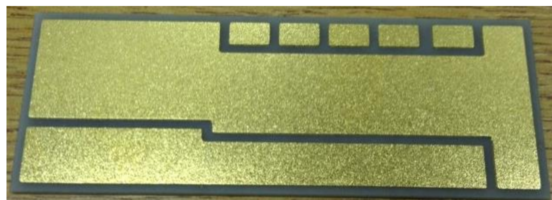

Figure 3.9: AlN substrates

3.2.4 Heat sink

Custom made aluminium liquid cooled heat sink was designed and manufactured at University of Sheffield. More details on the heat sink design is attached in the Appendix 3. Liquid cooled heat sink thermal resistance was calibrated and measured against water flow rate. Liquid cooled heat sink was used to achieve a low a thermal resistance path to make sure the heat flow is towards the heat sink. Thermal resistance of the water cooled heat sink was measured at different flow rates from 3 lpm to 15 lpm, as shown in Figure 3.10. A flow rate of 11 lpm was used in these experiments obtaining a thermal resistance of 10 °C/kW. Figure 3.10 shows the measured performance of the liquid cooled heat sink with respect to flow rate.

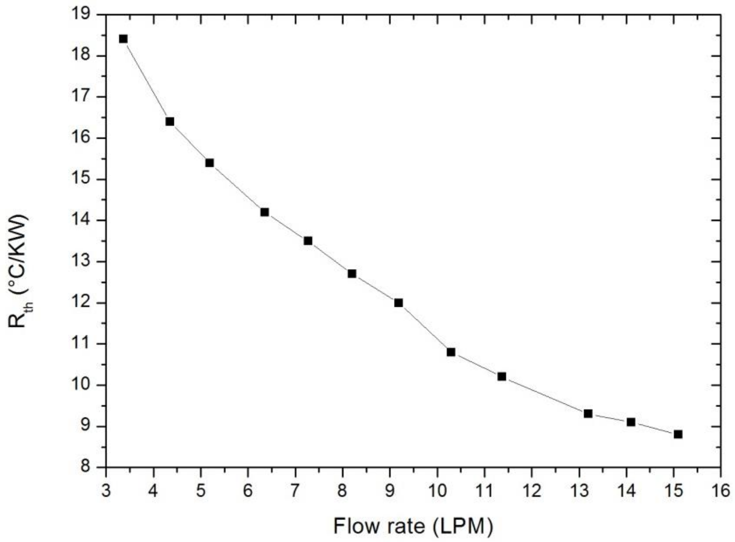

Figure 3.10: Thermal resistance Vs Flow rate

3.2.5 Wire bonding

Wire bonding is a major interconnect technology which is widely used in the electronic packaging industry. The die is first attached to the top copper of DBC substrate using solder, and then the source and gate aluminium pads on the IGBT die are wire-bonded to a metallised top copper track pads. The wire bonding was done at University of Sheffield using a wedge wire bonder. Four aluminium wires of 200µm thick were ultrasonically bonded from IGBT emitter pad to surrounding conductive trace. Fuse current for each 200µm Al wire was 9.5A [14](see Appendix 5), as a rule of thumb enabling ~2x current carrying capability of the device rated current. 100µm thick Al wire was used for the gate wire and emitter sense as shown in Figure 3.11.

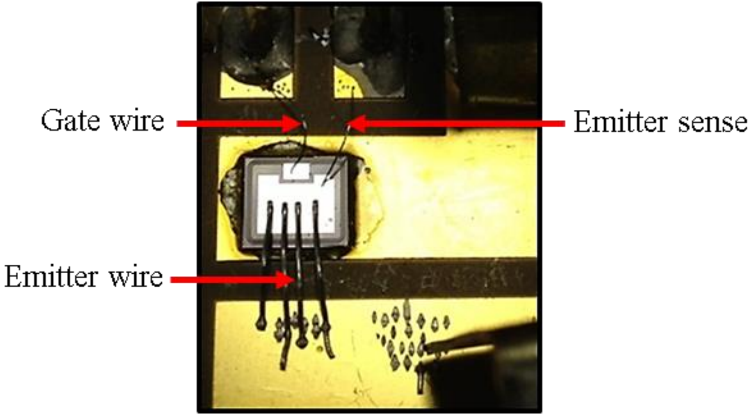

Figure 3.11: PCD substrate die attached and wire bonded

3.3 Experimental setup

3.3.1 Junction temperature measurement

The junction temperature defines the temperature inside the chip, which is significant for the safe operations of semiconductor devices. Since the chip temperature is not homogenous, the term virtual junction temperature is used (T_j). The virtual junction temperature is an average chip temperature assuming homogenous cooling of the device. $T_{j(max)}$ describes the maximum allowed dynamic junction temperature in the device on-state. Even under dynamic overload conditions i.e, at high power level and at different duty cycle operation the device is not allowed to exceed the $T_{j(max)}$ value, for the Silicon die used, the maximum operating junction temperature is 175°C.

Junction temperatures measurements are vital for estimating the thermal performance of semiconductor packages. Measuring the junction temperature in a semiconductor die using electrical method is extensively used in semiconductor packaging industry[15]. Electrical method of measuring the junction temperature is a direct, non-invasive technique as it utilises semiconductor die junction as the temperature sensor. Even though infrared and liquid crystal sensing techniques can also be used to measure the semiconductor die junction temperatures, these methods are restricted to the directly visible junctions on the semiconductor die. On the other hand, junction temperature measurement using electrical method can be achieved using temperature sensitive parameters of semiconductor die.

3.3.1.1 Electrical method

The electrical method uses temperature sensitive parameter, which is the forward voltage drop of the semiconductor die. The forward voltage drop also known as the "collector-emitter

voltage $V_{ce(sat)}$" [16-18] changes with respect to junction temperatures. The I-V characteristics of the IGBT die are measured at junction temperatures ranging from 10°C to 150°C, temperature step of 10°C, using a thermo stream. Thermo stream uses hot and cold air to control the temperatures from -55°C to 250°C and it's interfaced to a sealed chamber. The device to be tested is placed inside the sealed chamber and the temperature of the device is monitored using a K type thermocouple. At each temperature step the device is made to soak for 20 seconds so that the junction temperature in the device equals the desired temperature. The sealed chamber is interfaced with curve tracer to measure the I-V characteristics. The 'V_{ce}' forward voltage increases with junction temperature which could be observed in Figure 3.12, showing the I-V characteristics of the IGBT die measured at junction temperature of 25°C and 150°C.

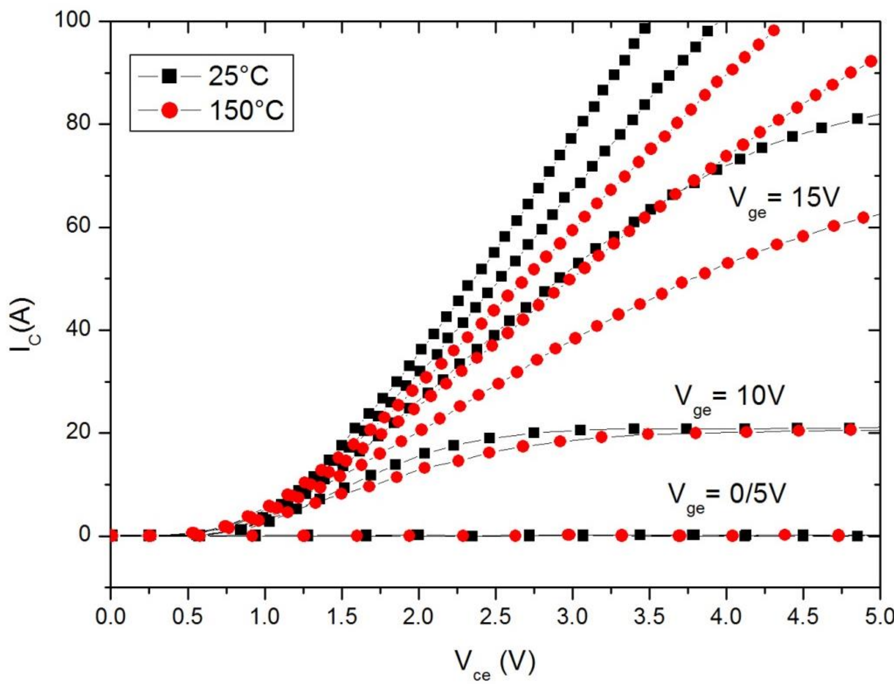

Figure 3.12: I-V characteristics of IGBT measured at junction temperatures of 25°C and 150°C

Figure 3.13 shows measured on-state voltage drop 'V_{ce}' at collector currents 'I_c' 10, 12.5 and 15A at gate voltage V_{ge} =10V with different junction temperatures from 25°C to 150°C. The on-state voltage drop 'V_{ce}' is directly proportional to junction temperature and increases with collector current 'I_c'.

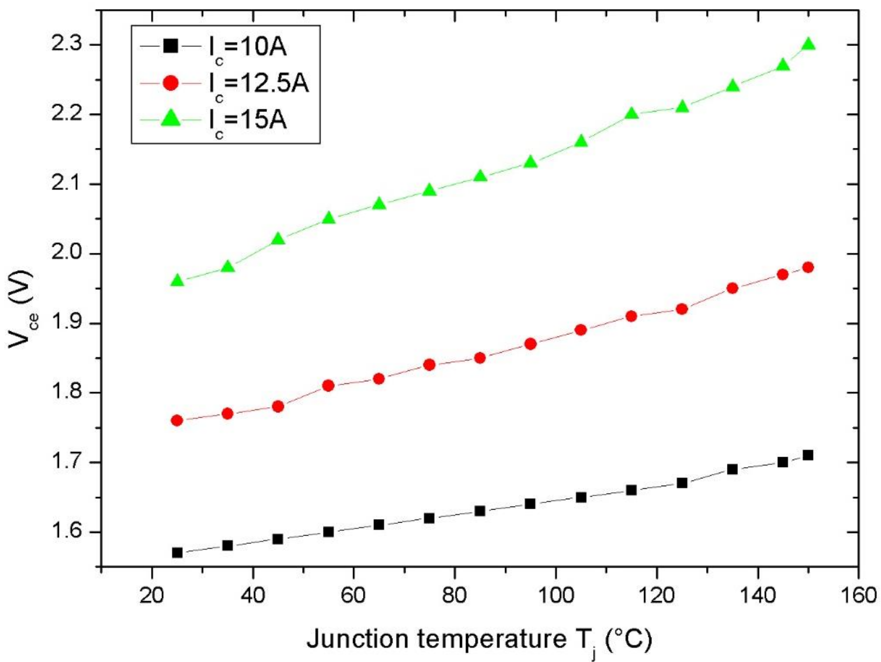

Figure 3.13: V_{ce} Vs T_j at gate voltage V_{gs}=10V

Figure 3.14 summarises the shift in V_{ce} at different junction temperatures for IGBT dies mounted over AlN and PCD substrates at V_{ge} = 10V and I_c = 15A. The V_{ce} versus T_j curve for IGBT dies mounted on AlN and PCD tiles shows less than 5% error, which gives confidence in the measured data.

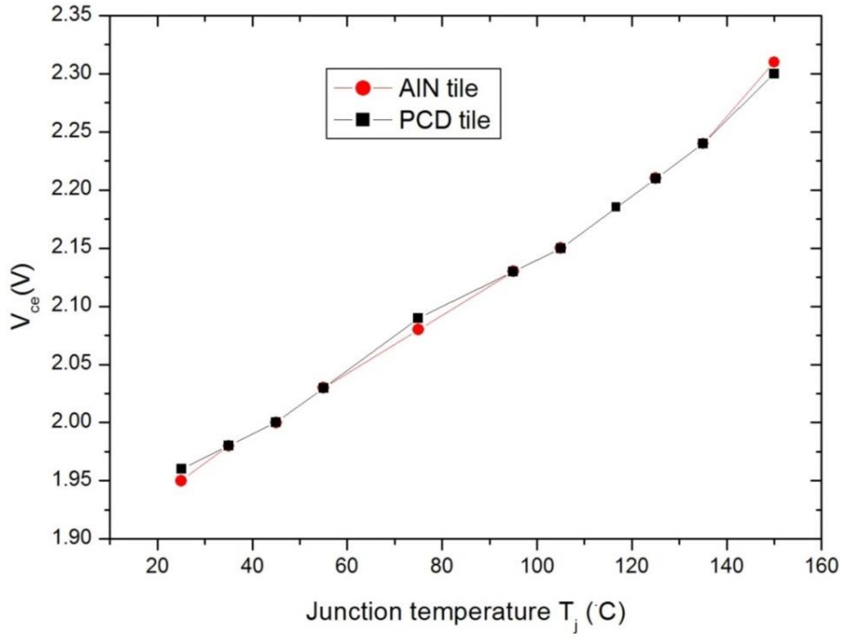

Figure 3.14: V_{ce} Vs T_j at V_{ge} = 10V and I_c = 15A for PCD and AlN substrate

3.4 Overview of experimental setup

Figure 3.15 shows the schematic cross section of the experimental structure. The IGBT dies mounted on AlN and PCD tiles were placed on a copper block, which was used as an interface between the DBC substrates and liquid cooled heat sink. Case temperature thermocouple was buried within a copper block and placed right underneath the die to observe the maximum case temperature. The heat sink thermocouple was placed on top of the heat sink and was sealed using kapton polyimide tape. In order to minimise the air gap between the DBC substrate and copper block; and to hold the system firmly together a spring force was used. Figure 3.16 shows the photographic view of the experimental structure.

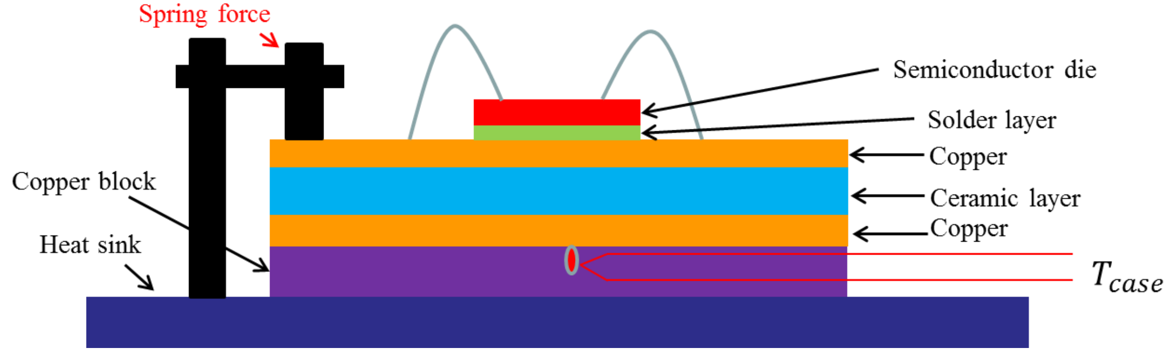

Figure 3.15: Schematic cross section of the experimental structure

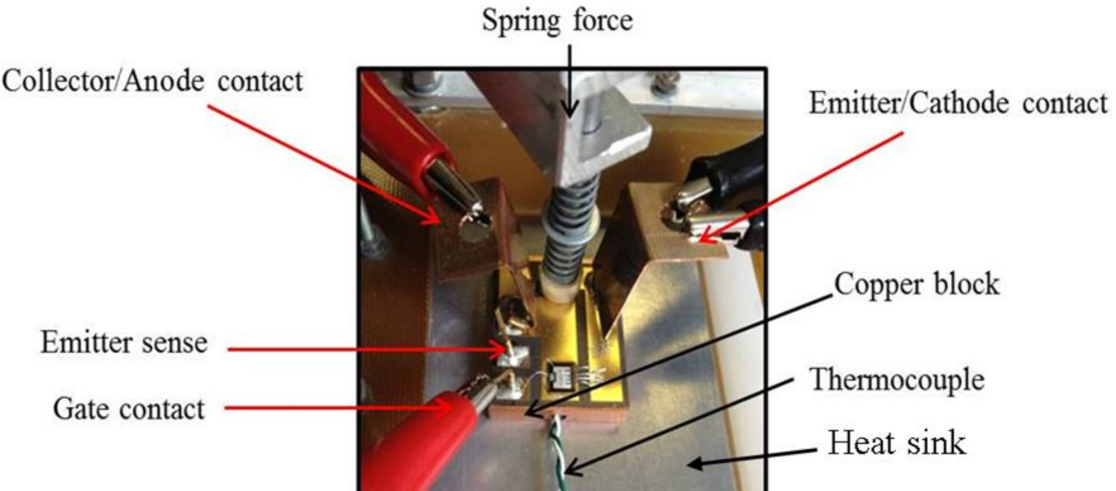

Figure 3.16: Photographic view of the experimental structure

The case and heat sink temperature were monitored using K-type thermocouples which was interfaced to a PICO data logger. Figure 3.17 shows the case and heat sink temperature response logged for a 27 minute test period to make sure the thermal equilibrium conditions.

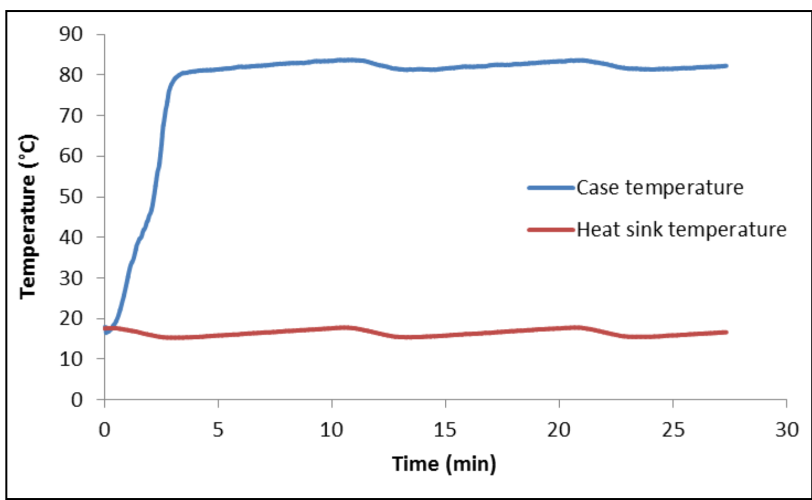

Figure 3.17: Data log of case and heat sink temperature

3.5 Experimental measurement of thermal resistance of PCD and AlN substrates

3.5.1 Thermal resistance (junction-case) $R_{th(j-c)}$

Thermal Resistance is defined as the difference in temperature between two closed isothermal surfaces divided by the total heat flow between them[15]. Defining T_J and T_C as the junction & case temperatures respectively, and the total heat flow rate between them as P, the thermal resistance between them is represented in equation (3.1),

$$R_{th} = \frac{T_J - T_C}{P} \tag{3.1}$$

Where,

T_j = Junction temperature

T_c = Case temperature

P = Power applied

The unit of thermal resistance is °C/W.

Prior to equilibrium, the component is considered to be in thermal transition or a transient thermal state. At thermal equilibrium, time becomes an irrelevant parameter. It took 5 to 10 minutes for the system to reach the equilibrium conditions. Once equilibrium has been reached, the duration of previous heating is not needed to predict the temperature of the component.

The IGBT dies mounted on AlN and PCD tiles were tested at two different power levels; at each power level eight tests were taken to gain confidence in result stability.

Thermal resistance was measured at a power level of ~32W, as shown in Figure 3.18, under gate emitter voltage V_{GE}=10V and a collector current I_C of 15A. The potential voltage difference across the collector and emitter terminal V_{CE} was noted and monitored using digital oscilloscope. From Figure 3.13 the junction temperature (T_j) was referred from the measured collector-emitter voltage (V_{CE}). The power level (P) was calculated by the collector-emitter voltage V_{CE} and collector current I_C. The case and heat sink temperatures were measured using embedded thermocouples and monitored using picco data logger for ~20minutes in order to achieve thermal equilibrium conditions. Moreover, V_{ce} voltage was measured between the collector terminal and emitter sense to eliminate the heavy wire bonding resistance. A second test was repeated increasing the power level to 40W by increasing the gate-emitter voltage to 15V and collector current to 20A. These results are shown in Figure 3.19.

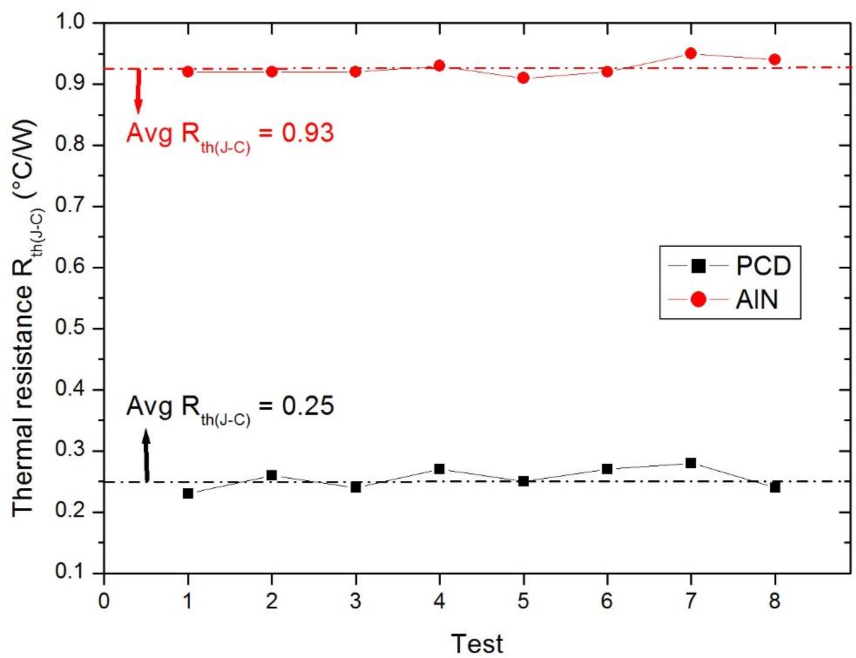

Figure 3.18: Thermal Resistance (Junction – Case) $R_{th(j-c)}$ at ~32w For PCD and ALN Substrates

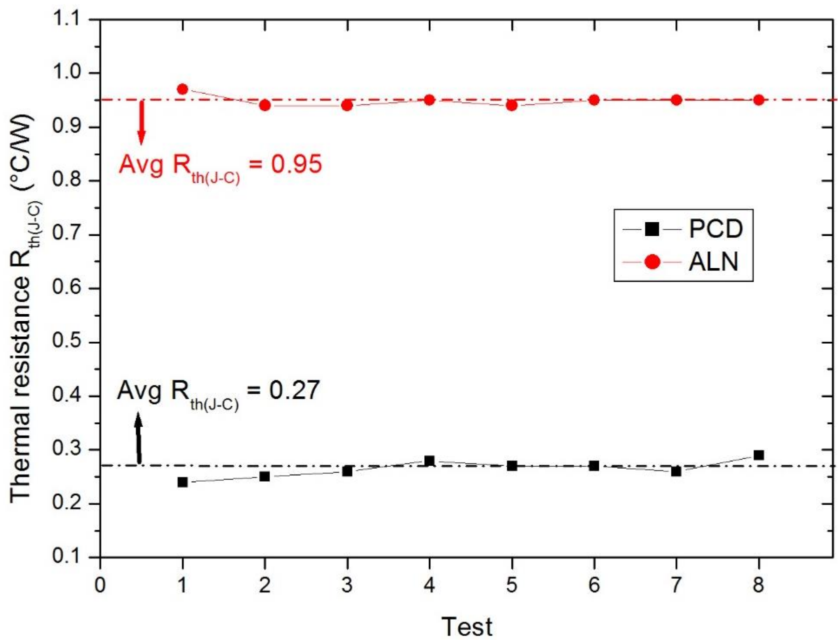

Figure 3.19: Thermal Resistance (junction – case) $R_{th(j\text{-}c)}$ at ~40W for PCD And AlN Substrates

From Figures 3.18 and 3.19 the measured junction-to-case thermal resistance $R_{th(j\text{-}c)}$ varies by approximately 5% for each test point accounts to thermal and electrical measurement errors and changes in contact resistance [19] when the test assembly is mantled at the commencement of each tests. As shown, compared to the AlN benchmark a 74 % reduction in junction-to-case thermal resistance $R_{th(j\text{-}c)}$ was achieved using polycrystalline diamond.

3.5.2 Thermal Impedance (junction to case) $Z_{th(j\text{-}c)}$

When the power devices are subjected to transient loading condition, the temperatures within the component package changes towards a new thermal equilibrium level. Thermal impedance measurements were performed using the same experimental setup as described in Section 3.4 apart from the 15V volt pulse applied to the gate –emitter voltage (V_{GE}) via an arbitrary function generator. For these measurements 'I_c =15A' and continuous pulse width ranging from 1µs to 1s was used to calculate thermal impedance with duty cycle set to 10-50%. Figure 3.20 shows the schematic wave form for thermal impedance (Z_{th}) for PCD tile measured at 100µs (50% duty cycle).

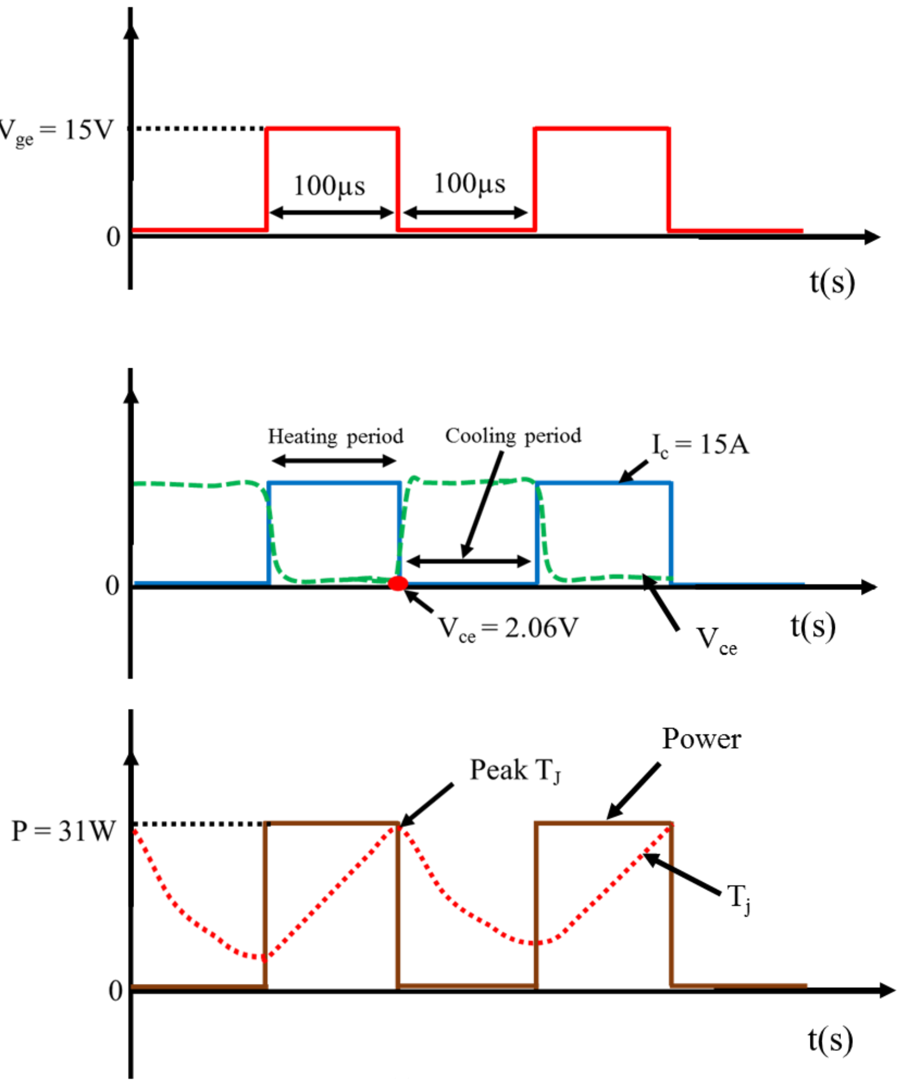

Figure 3.20: Schematic wave form for thermal impedance (Z_{th}) for PCD tile measured at 100µs (50% duty cycle).

Junction temperature starts to increases for the first pulse and at the end of the first pulse termination the junction temperature starts to cools until the second power pulse is applied. This represents heating period which is ON time of the pulse and cooling period, OFF time of the pulse. The peak junction temperature is calculated using Figure 3.13 by measuring the corresponding temperature sensitive parameter 'V_{ce}' at the end of heating period whereas, the case temperature was measured using the thermocouple. The resultant thermal impedance junction to case was calculated using equation (3.2),

$$Z_{th} = \frac{T_{peak\,J} - T_C}{V_{ce} * I_C} \qquad (3.2)$$

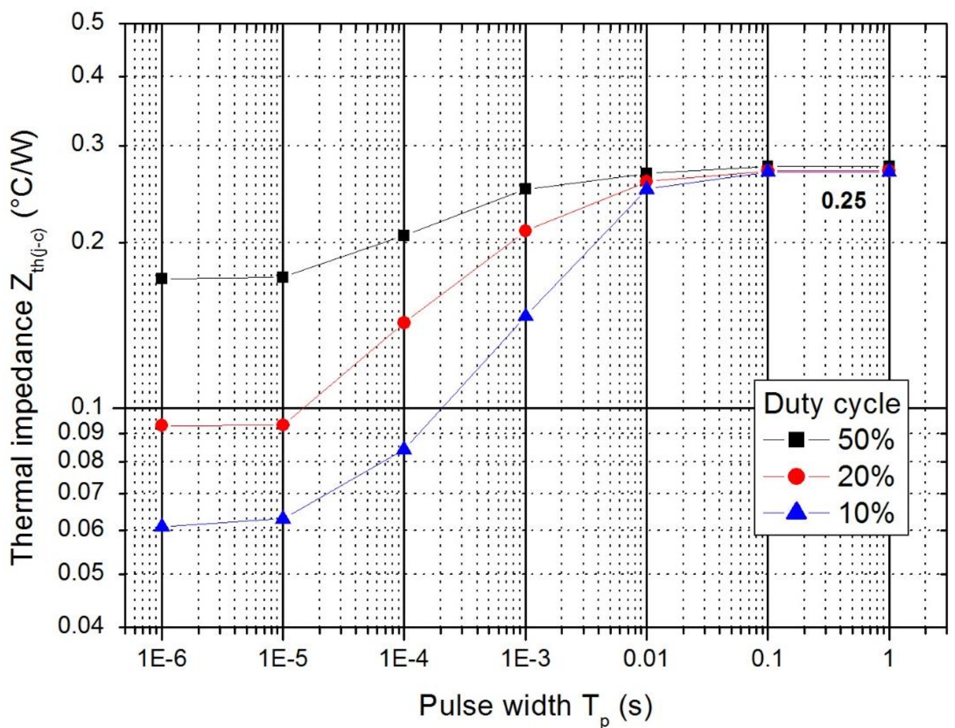

Figure 3.21: Thermal impedance (junction to case) $Z_{th(j-c)}$ for PCD substrate

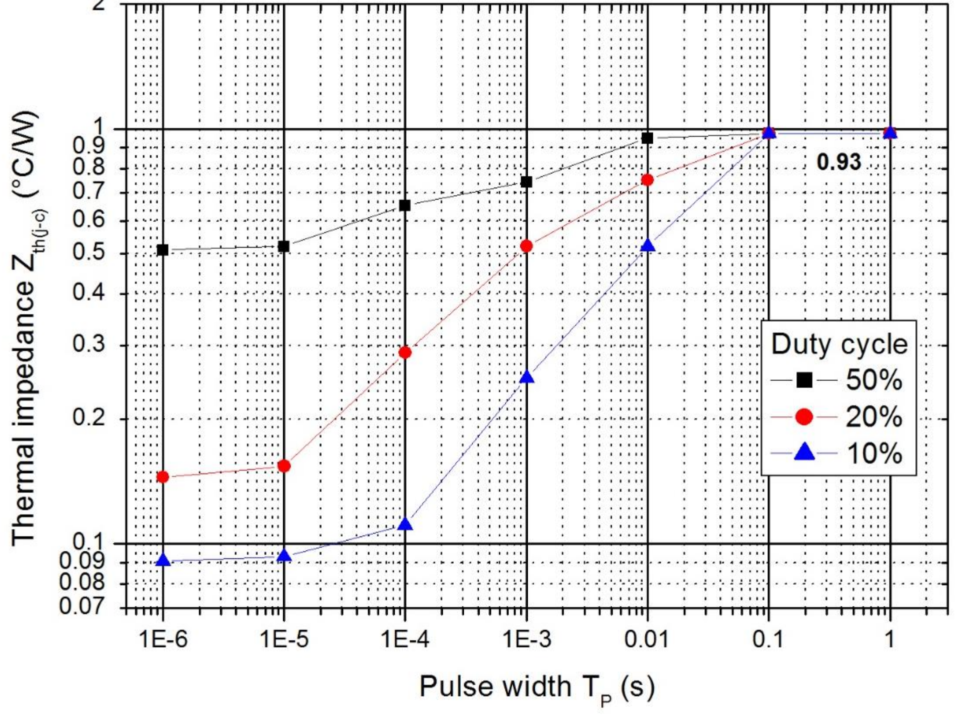

Figure 3.22: Thermal impedance (junction to case) $Z_{th(j-c)}$ for AlN substrate

Thermal impedance measurements for the PCD and AlN tiles are shown in Figure 3.21 and 3.22 respectively. Thermal impedance increases with the length of the pulse width, for example, a short pulse width of 1µs at 10% duty cycle a very low thermal impedance of 0.09ºC/W was measured. This is due to the fact that the junction temperature increase is small for a very short pulse width as a result of the thermal capacitor charging. At longer pulse width of >0.1s the thermal capacitors has charged to its maximum energy, resulting the thermal impedance to saturates at its DC thermal resistance. Figure 3.22 compares the thermal impedance for PCD and AlN tiles at 50% duty cycle. The PCD tiles show reduced thermal impedance compared to the AlN substrate at higher (500 kHz) and lower (5 Hz) frequencies as a direct result of its overall lower thermal impedance.

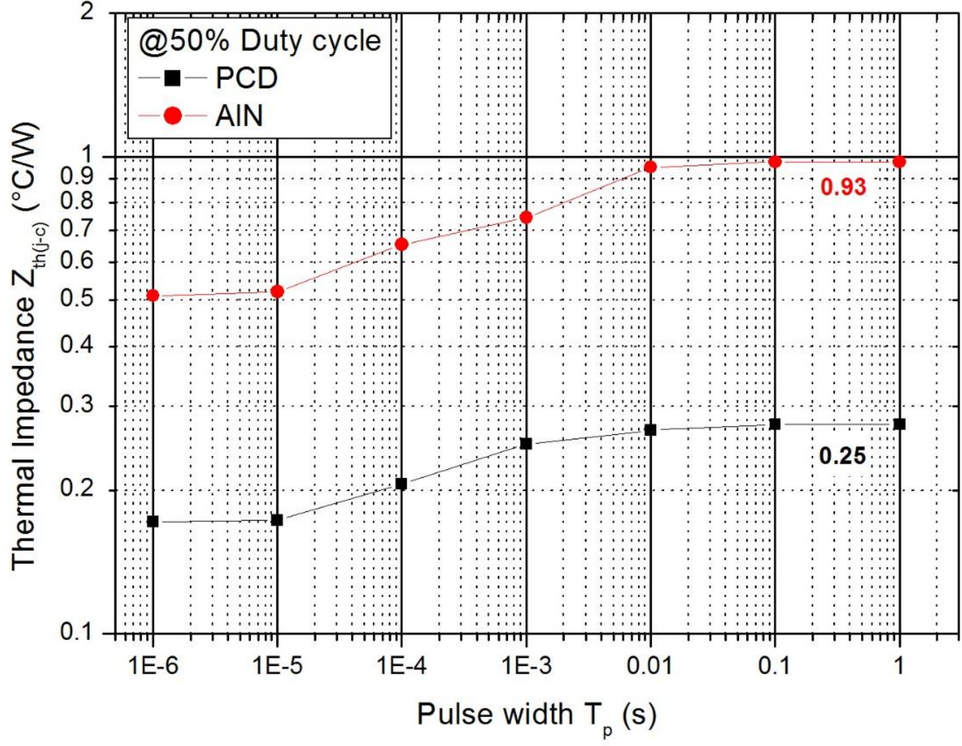

Figure 3.23: Thermal impedance (junction to case) Zth(j-c) for PCD and AlN substrates at 50% duty cycle

3.5.3 Void influence and contact thermal resistance

To determine the thickness of the solder layer and to understand the influence of solder voids upon thermal resistivity, five AlN substrate samples were cross sectioned through the centre of the die and analysed. Cross sectional analysis was done at University of Sheffield, as part of sample preparation the sample is sectioned using a slow diamond cutter. The sectioned sample is mounted and plotted using epoxy plotting resin. The sample is grinded and polished to be

observed on the digital microscope, a typical cross-section is shown in Figure 3.24. The solder, copper and ceramic layers were scanned in both horizontal and vertical directions for voids, as shown in Figure 3.25. The net average voids and the influence of thermal resistance on solder layers and copper layers are summarised in Table 3.2. The void influence at Si and ceramic layers were insignificant, as there were in nanometre scale range as expected.

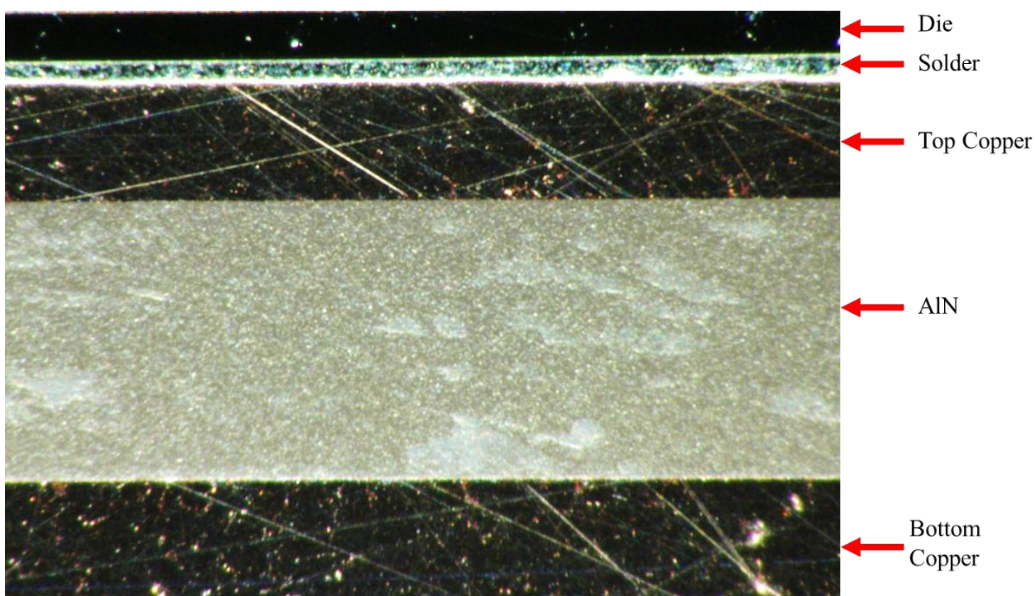

Figure 3.24: Cross-section of AlN DBC tile

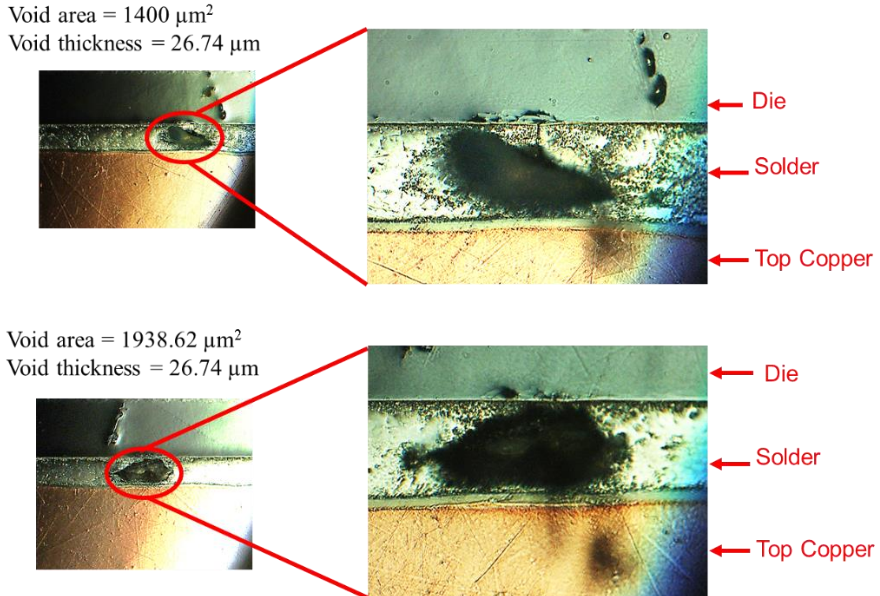

Figure 3.25: Detailed view of Solder voids

Table 3.2: Summary of voids in solder and copper layers

Parameter	Thickness	Length	Average Void area over 5 samples	Average Void thickness	Void percentage across the entire die
Solder layer	43µm	5mm	1836.07 μm^2	15.6 µm	0.77 %
Copper layer	200µm	22mm	290.18 μm^2	19 µm	0.04 %

The void thermal resistance can be calculated using equation (3.3)[20]. Table 3.3 shows the void thermal resistance for solder and copper layers:

$$Void\ thermal\ resistance = \frac{1}{h_c} \tag{3.3}$$

$$h_c = \frac{1}{L_g}\left(\frac{A_c}{A}k_A + \frac{A_v}{A}k_f\right)$$

Where,

h_c = Contact coefficient

L_g = thickness of the void

A_c = contact area

A = total cross sectional area

A_v = void area

k_A = thermal conductivity of void material

k_f = thermal conductivity of air which fills the void space

Table 3.3: Void thermal resistance in solder and copper layers

Parameter	Void thermal resistance (m^2 °C/W)
Solder layer	2.53E-9
Copper layer	1.62E-10

3.5.4 Simulation structure and specifications

To observe the influence of material thicknesses upon thermal resistance for both AlN and PCD tiles both systems were analysed using ANSYS®. ANSYS® is a finite element analysis simulation tool. The geometry structure was constructed using ANSYS® DesignModeler using the same dimensions and parameters used in the experimental analysis. The constructed geometry was simulated using ANSYS® TransientThermal to predict the temperature variation. A 40W thermal load was applied to the topside of the die. A die and solder thickness of 150µm and 43µm was used in this simulation. Physical parameters, listed in Table 3.1 and similar setup as described in Section 3.4 were used to develop the simulation. The backside of the tile was attached to the copper base and on to the liquid cooled heat sink of thermal resistance 10ºC/kW. It is assumed that a perfect thermal boundary exists between the backside metal and the heat sink. Figure 3.26 shows the 3D thermal contours of PCD tile mounted on to copper block and the heat sink.

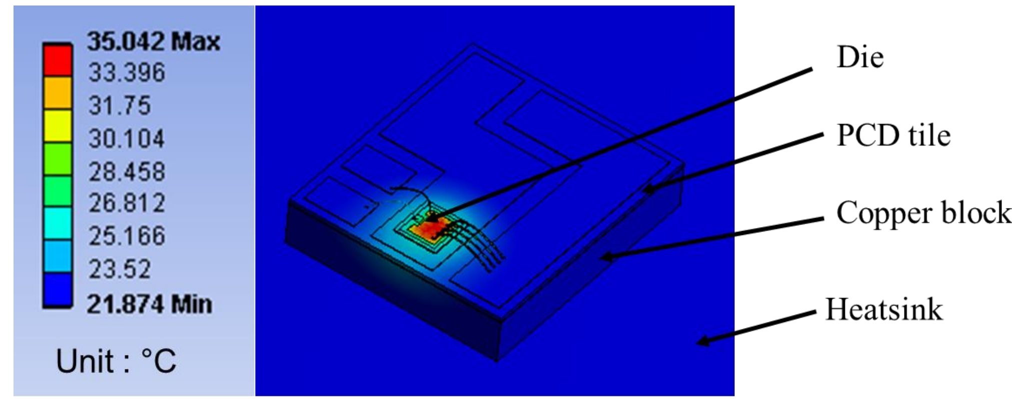

Figure 3.26: 3D view of PCD tile mounted on a copper block and heatsink

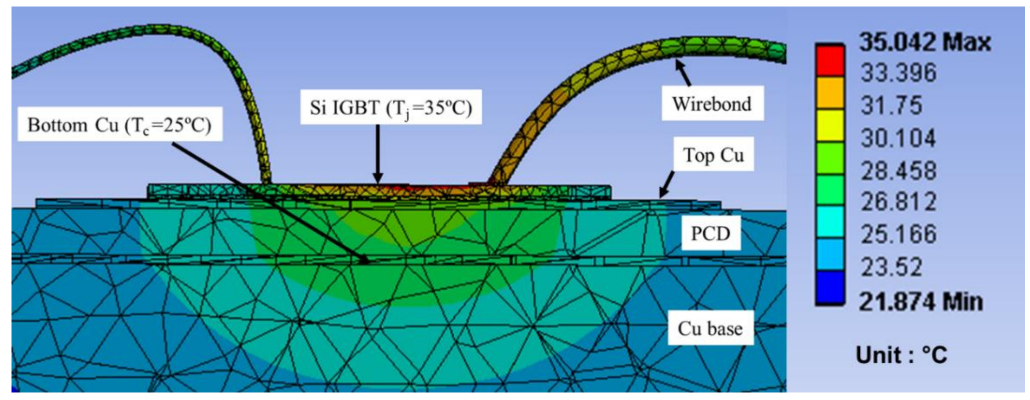

Figure 3.27: Cross-sectional thermal contours for PCD tile (Thermal loading = 40W, Ambient = 22ºC)

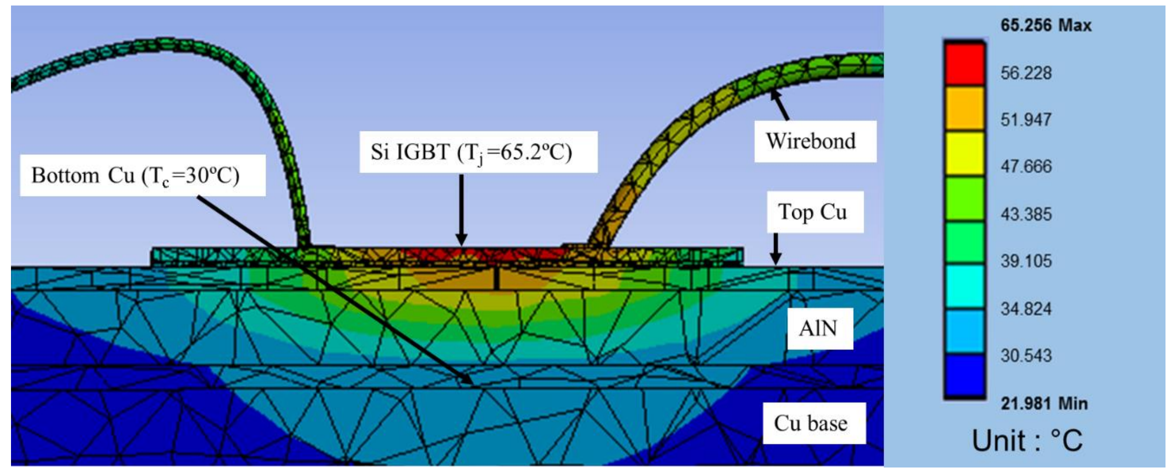

Figure 3.28: Cross-sectional thermal contours for AlN tile (Thermal loading = 40W, Ambient = 22ºC)

Figure 3.27 and 3.28 shows cross sectional thermal distribution for Silicon power devices attached to the PCD and AlN tiles respectively. As shown, due to the higher thermal conductivity of the PCD the thermal gradient within this layer is significantly reduced in comparison to the AlN counterpart. This has reduced the IGBT junction temperature from 65.2˚C to 35˚C. Table 3.4 compares the measured thermal resistance of the AlN and PCD tiles obtained through both simulation and experimental measurements. As shown the difference between simulated and measured thermal resistance (junction to case) for PCD and AlN substrates lies within ~11%.

Table 3.4: Measured and Simulated Thermal Resistance (junction – case) $R_{th(j-c)}$

Parameter	Simulated $R_{th(j-c)}$ (˚C/W)	Measured $R_{th(j-c)}$ (˚C/W)
PCD substrate	0.25	0.27
AlN substrate	0.88	0.95

Figure 3.29 shows the influence of insulating layer thicknesses upon the junction-to-case thermal resistivity for silicon dies attached to AlN and PCD tiles with 100µm and 200µm top/bottom side copper metallisation thickness. Compared to the AlN system, thermal

resistance is less-sensitive to layer thickness for the PCD substrate where metallisation thicknesses plays a more significant role.

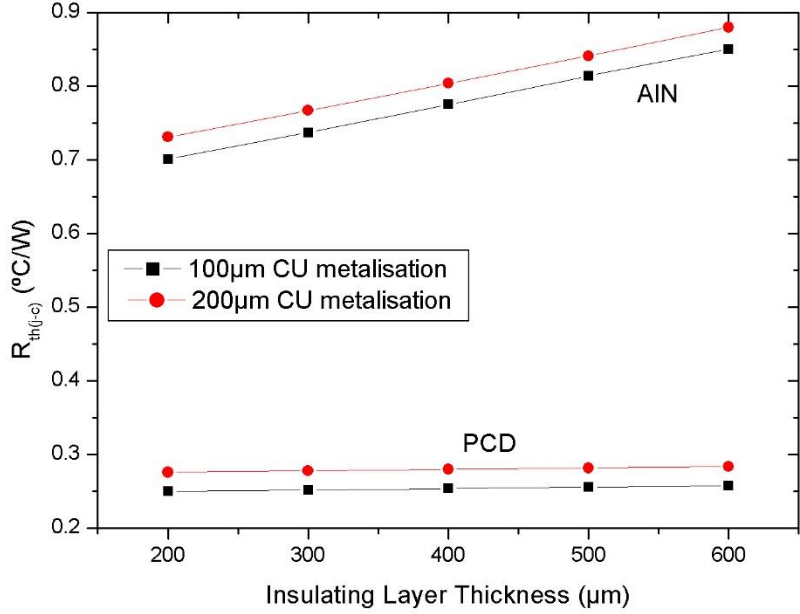

Figure 3.29: Variation in the thermal resistance with thicknesses for Si dies on AlN and Diamond tiles

3.5.5 Thermal Cycle Reliability for PCD & AlN substrates

Reliability of the Aluminium Nitride and Polycrystalline Diamond tiles were evaluated using thermal cycling test. Thermal stress due to thermal cycling was numerically modelled in ANSYS® Static structural tool. The tiles were exposed to a temperature range from -55°C to 150°C at a ramp rate of 1°C/s with dwell time of 15 minutes at each temperatures, total of four cycles [21, 22] as shown in Figure 3.30. The structure is constructed using ANSYS® DesignModeler and simulated using Structural Analysis[23, 24]. The ANSYS® Structural Analysis calculates the strain and stress in X and Y axis co-ordinates, the strain and stress in Z axis is very low and is negligible due to the micro structure geometry. The mechanical properties used in the simulation were same as from Table 3.1.

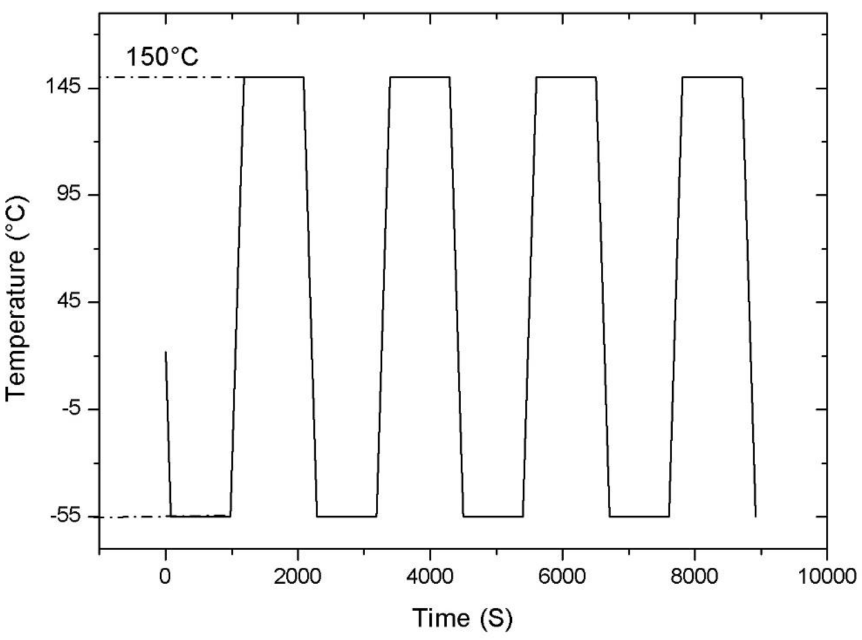

Figure 3.30: Thermal loading

3.5.5.1 Equivalent strain

Thermal strain is deformation of material caused by temperature change as represented in equation (3.4)[25].

$$\varepsilon_t = \propto \Delta T \tag{3.4}$$

Where,

$\propto$ = Coefficient of thermal expansion (CTE) (C^{-1})

ΔT = Change in temperature (°C)

ε_t = Thermal strain

Figure 3.31 and 3.32 shows 3D thermal strain contours for a Silicon die mounted on a PCD or AlN substrate during the 150ºC dwell period. As shown the resultant thermal strain causes the tile to exhibit a concave shape, as a result of the top copper metallisation pattern and mismatch in Coefficient of Thermal Expansion (CTE) of the PCD/AlN tile compared to the Silicon die.

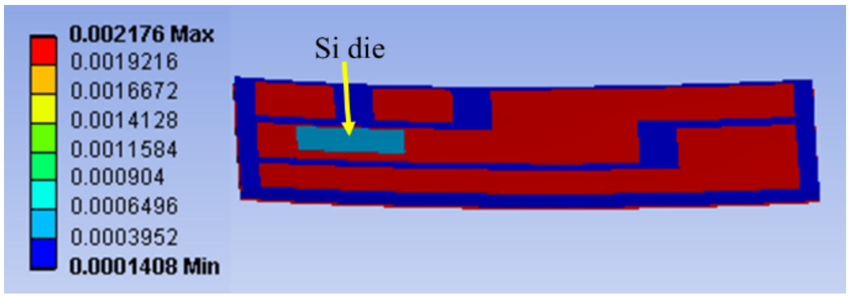

Figure 3.31: Thermal strain contours for Si die mounted over polycrystalline diamond tile at 150°C

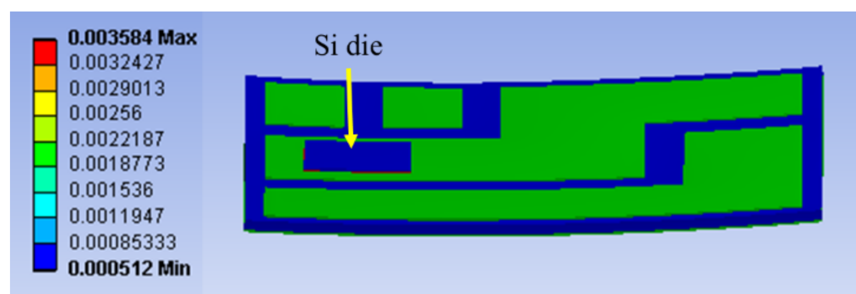

Figure 3.32: Thermal strain contours for Si die mounted over Aluminium nitride tile 150°C

Maximum strain was found in the solder (SnAg) and top/bottom copper layers as they have a very high coefficient of thermal expansion [8] than PCD, AlN and silicon materials.

3.5.5.2 Equivalent stress(Von-Mises)

Mechanical stress is developed due to thermal strain in the system. A common way to express these multidirectional stresses is to summarise them into an equivalent stress, also known as the von-Mises stress. The unit of equivalent stress is 'Pa' represented using equation (3.5)[25].

$$f = \propto \, . \, \Delta T . \, \Upsilon \qquad (3.5)$$

Where,

f = Equivalent stress

∝ = Coefficient of thermal expansion CTE (°C^{-1})

ΔT = change in temperature (°C)

Y = young's modulus or Elastic modulus (Pa)

Figures 3.33 and 3.34 shows three-dimensional thermal stress contours for the Silicon die mounted on to the PCD and AlN substrates observed at 150°C. A maximum thermal stress of 390MPa is observed for the PCD and 283MPa for AlN systems located at the top and bottom copper layers.

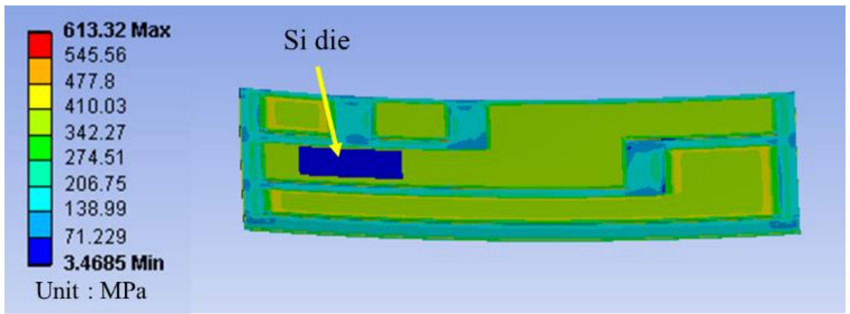

Figure 3.33: Thermal stress contours for Si die mounted over polycrystalline diamond tile 150°C.

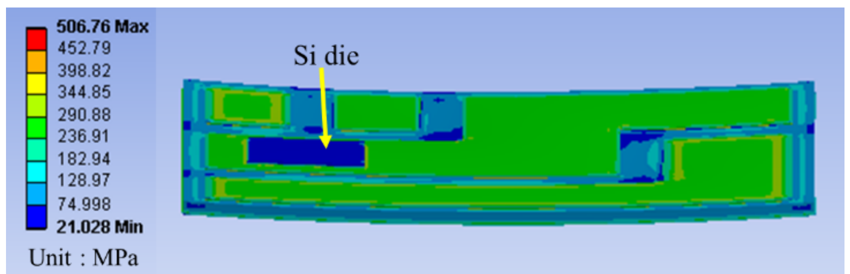

Figure 3.34: Thermal stress contours for Si die mounted over aluminium nitrite tile 150°C

3.5.5.3 Safety factor

Safety factor is the ratio of the material yield strength of the material to equivalent stress developed. Safety factor determines how much the designed structure actually will be able to withstand the induced thermal stress, the higher the safety factor the less likely the system will fail; therefore a safety factor <1 is reflected as untrustworthy [26]. Using (3.6) safety factor is described as

$$Safety\ factor = \frac{S_{limit}}{\sigma_e} \tag{3.6}$$

Where,

S_{limit} = Yield strength of the material (MPa)

σ_e = Equivalent stress (MPa)

Table 3.5 shows the comparison of thermal stress and safety factors for PCD and AlN substrates. PCD system exhibits similar safety factor when compared over the conventional AlN system.

Table 3.5: Thermal stress and safety factor in silicon device mounted on polycrystalline diamond and aluminium nitride substrates

	PCD system		**AlN system**	
Parameter	**Equivalent stress (MPa)**	**Safety factor**	**Equivalent stress (MPa)**	**Safety factor**
Silicon	34	15	48	15
Solder(SnAg)	130	0.3	211	0.2
Top/Bottom copper	390	0.3	283	0.4
Ceramic	136	9	156	10

3.5.5.4 Life cycle fatigue

Life cycle fatigue determines the reliability of DBC substrate, fatigue failure may occur in DBC substrates due to thermal cycling. When DBC substrates are subjected to extreme thermal loading conditions and due to the different Cu/AlN/Cu material sandwiches failures such as fracture and brittle are observed on the DBC substrates. In order to predict the life cycle fatigues of DBC materials. The life cycle fatigue can be predicted using Mason and Coffin law [27, 28]. Mason and coffin law is classified in to two types, (i) low life cycle fatigue for materials/structures which have low life cycles such as semiconductors and electronics packaging materials. (ii) High life cycle fatigue for materials which have high life cycles such as steel and titanium materials. Manson and coffin law for low cycle fatigue prediction as described in equation (3.7),

$$N = \frac{\left(\frac{\Delta\varepsilon/2}{\varepsilon_f}\right)^{\frac{1}{c}}}{2} \qquad (3.7)$$

Where 'N' is the number of cycles to failure , $\Delta\varepsilon$, ε_f and c are equivalent strain amplitude, fractured strain and empirical fatigue ductility exponent. Thermal cycling profile as shown in Figure 3.30 was performed for PCD and AlN substrates without the Si and the die attach medium, as the fracture strain and empirical fatigue ductility exponent for Solder and Si layer require intensive tests to calculate and not available in literature. 3D equivalent stress for PCD substrate (Top Cu/PCD/Bottom Cu) is shown in Figure 3.35.

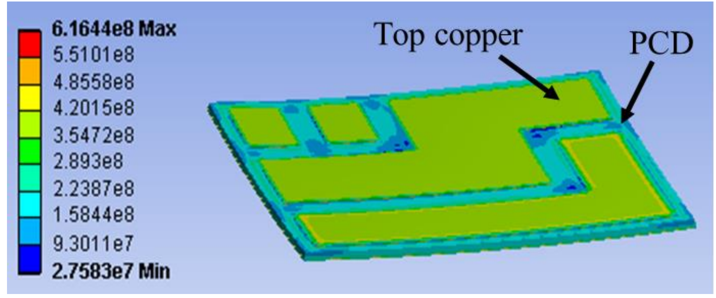

Figure 3.35: Equivalent stress contours for PCD substrate

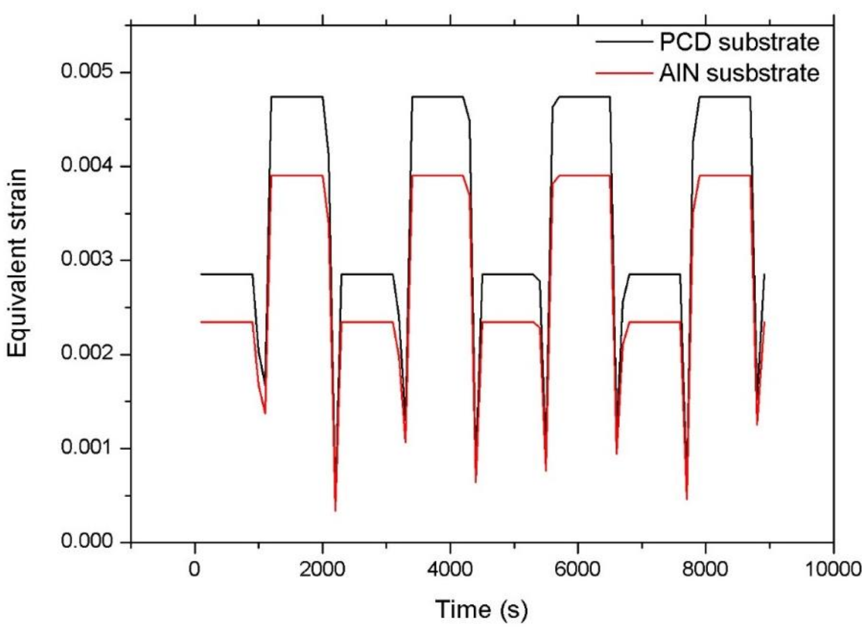

Figure 3.36: Maximum equivalent strain for PCD and AlN substrates

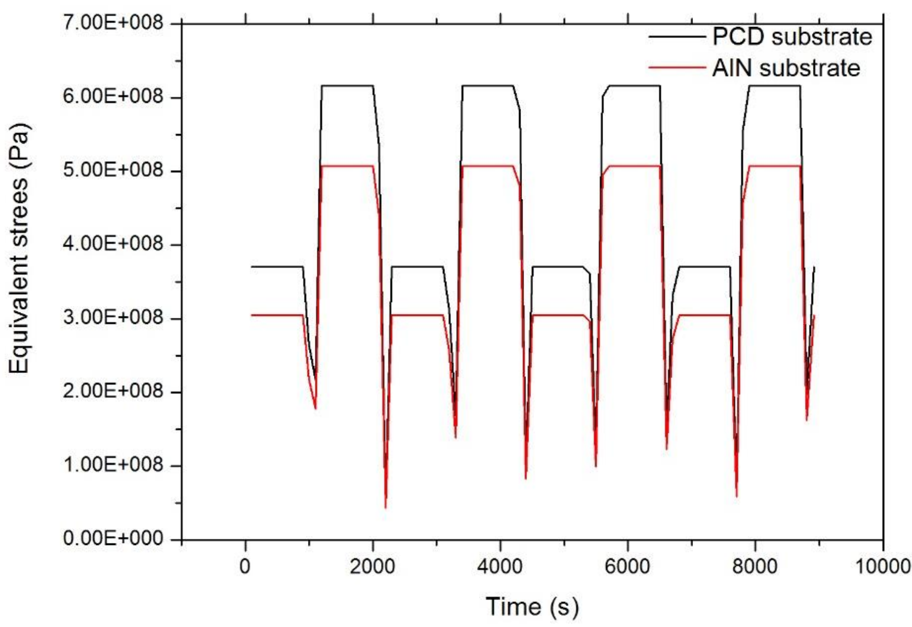

Figure 3.37: Maximum equivalent stress for PCD and AlN substrates

Figure 3.36 and 3.37 shows the maximum equivalent strain and stress for PCD and AlN substrates, the maximum strain and stress was observed in the copper layers. The fracture strain 'ε_f' 0.3[29] and 'c' -0.66[30] for copper the life cycle can be calculated using equation (3.7). The copper layer has the maximum stress and strain compared to the PCD/AlN layer and the life cycle is predicted based on the material properties of copper. Figure 3.38 shows the life cycle fatigue for PCD and AlN substrates, AlN has extended fatigue life cycle when compared over PCD substrates.

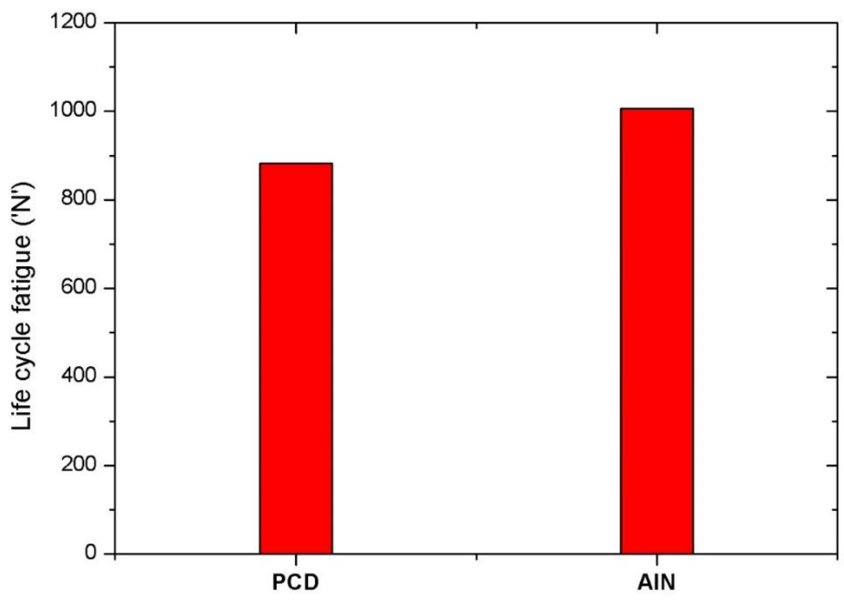

Figure 3.38: Life cycle fatigue for PCD and AlN substrates

3.5.6 Rated current and switching frequency improvement

As power rating is proportional to thermal resistance, the PCD tile can benefit from increased current rating or switching frequencies. Considering a worst case operating condition at a 100°C ambient temperature, maximum junction temperature of 150^{0}C and air cooled heat-sink with a heat-sink-to-ambient thermal resistance of 0.1^{O}C/W [31](see Appendix 6) gives a total junction-to-ambient thermal resistance of 0.37°C/W and 1.05°C/W for the PCD and AlN tiles respectively; using thermal network in Figure 3.39 and equations (3.8) and (3.9). Neglecting the interface thermal resistance, Figure 3.40 shows the DC current rating of the IGBT die for the AlN and PCD substrates. The PCD tile increases the power rating by a factor of 2.8 from 47W to 135W; resulting in a ~2 x increase in the current rating.

$$R_{th(j-a)} = \frac{T_j - T_a}{P} \tag{3.8}$$

Rewriting equation (3.8) for power dissipation (P) ,

$$P = \frac{T_j - T_a}{R_{th(j-a)}} \tag{3.9}$$

Where,

$R_{th(j-a)}$ = 0.37°C/W (for PCD) and 1.05 °C/W (for AlN)

T_j = Junction temperature (150°C)

T_a = Ambient temperature (60°C)

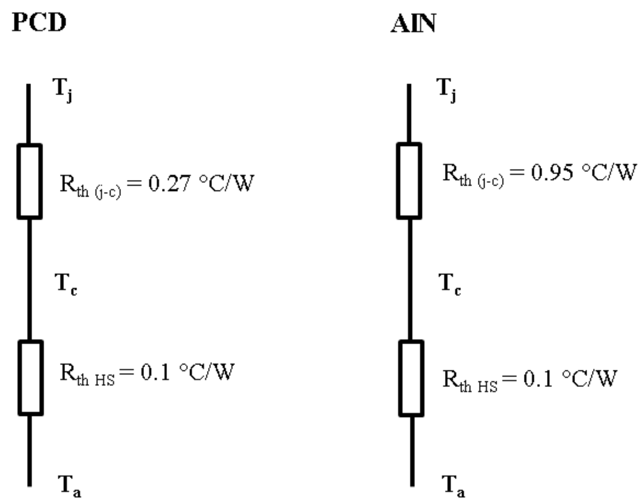

Figure 3.39: Thermal resistance junction to ambient ($R_{th(j-a)}$) network path

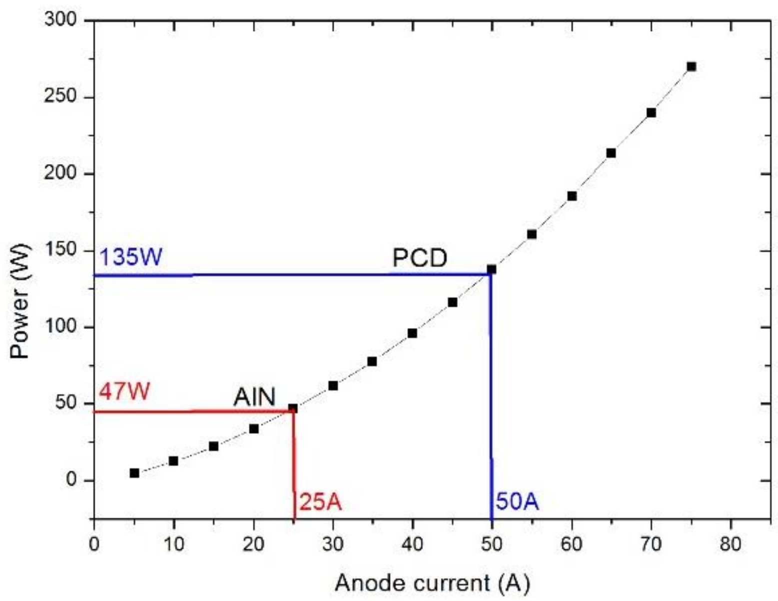

Figure 3.40: IGBT current rating at 100ºC ambient temperature

In terms of switching frequency improvement, considering a 600V DC-DC converter application as shown in Figure 3.41, at 50 % duty cycle with an ambient temperature of T_a = 100°C and maximum junction temperature of T_{jmax} = 150°C the total energy loss at T_{jmax} =150°C was found to be 4 mJ from the datasheet of similar 25A rated IGBT [32](datasheet attached in the appendix) device as the present IGBT [11] datasheet does not provide information about switching characteristic. As shown in Figure 3.42 by taking the increased power rating as increased switching losses the PCD tile can increase switching frequency by a factor of ~5.7. This would help increase converter power density by reduced passive filtering components as a result of the increased frequency and increase power density.

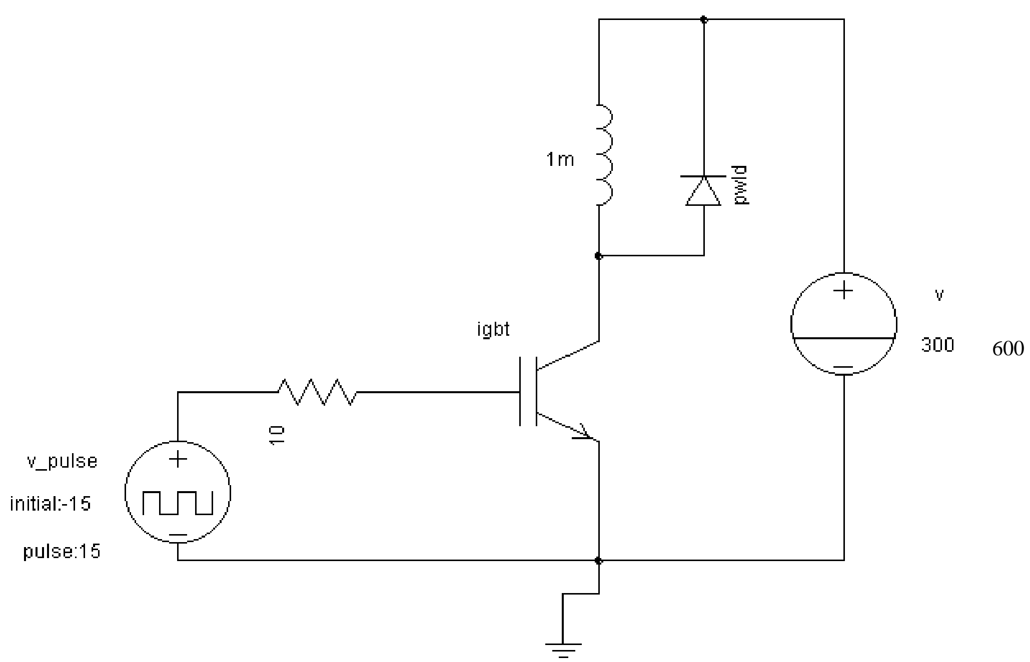

Figure 3.41: DC-DC converter

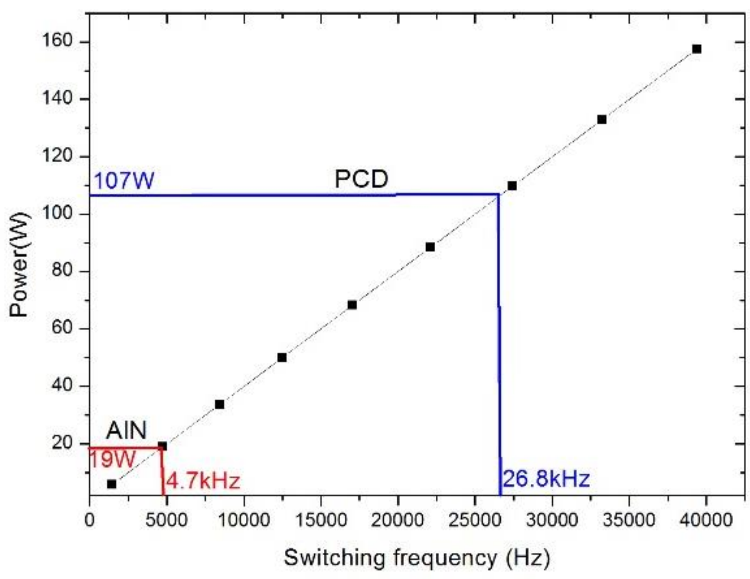

Figure 3.42: Maximum switching frequency for the AlN and PCD tiles operated at 25A.

3.6 Next generation technologies

Polycrystalline diamond has shown improved thermal performance over the conventional AlN substrates, this could be benefited in next generation technologies like wide band gap semiconductors such as SiC and GaN. SiC power devices with their superior characteristics offer greater performance in high temperature operating environment. SiC semiconductor power device has many advantages [33] when compared over the Si power devices

- SiC power devices possess lower on-resistances R_{on} which means lower conduction losses
- High break down voltage capability due to higher electric breakdown field, for example Si Schotty diodes commercially available are typically rated at lower than 300V whereas commercially rated SiC schottky diode have a break down voltage of 600V.
- SiC power devices have a high thermal conductivity of 490 W/mK whereas Si power devices have thermal conductivity of 150 W/mK. Therefore, the heat from the device could be transferred out efficiently due to the slow increase in device temperature which could benefit from lower junction to case thermal resistance $R_{th(j-c)}$.
- SiC power devices can operate at high junction temperatures in the range of 250ºC whereas, Si power devices have a maximum operating junction of 150ºC.
- Temperature dependent onstate and reverse breakdown voltages for SiC power devices vary only slightly due to temperature changes.
- Reverse recovery characteristics for SiC power devices are excellent which in turn reduces the switching losses and eliminates the use of snubber circuit.
- SiC power devices can operate at high switching frequency of greater than 20 kHz whereas, it's not possible in Si power devices.

As SiC power device can operate at high operating junction of 250ºC the conventional lead free solder(SnAg) cannot be used as a die attach medium as the melting point of solder is ~215ºC. Silver sintering is an alternative technology for high temperature packaging which replaces lead free solder as silver melting temperature is about 960°C. Silver sintering technology uses temperature profile in the range of 190ºC to 300ºC with sintered pressure of 5- 10 MPa, silver sintering has high thermal conductivity of 200-300W/mK when compared to solder paste of thermal conductivity 53W/mK.

3.6.1 Simulation structure and specification

To understand the thermal performance of next generation technology, ANSYS® thermal simulation was performed with SiC dies attached using silver sintering on to the PCD substrates. Figure 3.43 is shown a simplified cross-section of the thermal system considered. Silicon carbide die is attached onto a DBC substrate using Silver sinterd paste as a die attach compound. The structure is built using Design modeller and simulated using Ansys Steady-

State Thermal. For the analysis identical PCD tile specification of thickness of 500µm, top and bottom side copper thicknesses of 100µm were used.

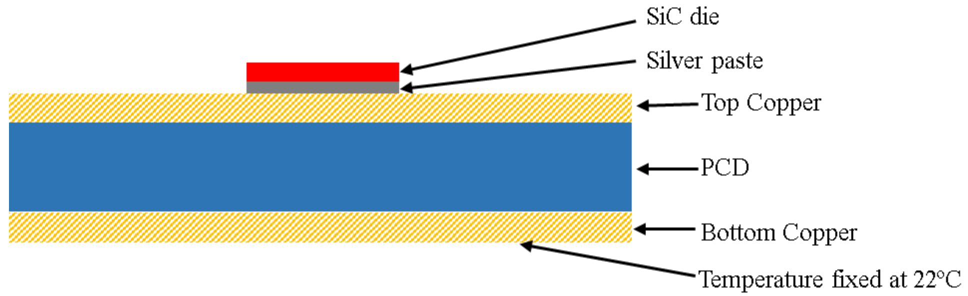

Figure 3.43: Simplified cross-section of the simulation thermal system

The Table 3.6 shows the material thicknesses used along with the thermal conductivity [34] (see Appendix 7 for silver sintered paste). For thermal simulations, SiC die size of 2.1x2.1mm [35](see Appendix 8) were arranged onto a 29.32x25.41mm PCD substrate. Thermal loading of 40W was applied to the active area of the die. The backside of the tile, which is bottom copper is kept at a constant temperature of 22°C.

Table 3.6: Material Thicknesses for the polycrystalline diamond substrate

Material	Thickness (µm)	Thermal conductivity (W/m.K)
SiC	300	360
Silver sintered paste	43	200
Topside Copper	100	390
Insulator (PCD)	500	2000
Bottom side Copper	100	390

3.6.2 Simulation results

Figure 3.44 shows a typical three-dimensional simulation of the silicon carbide dies attached to PCD tile whist dissipating 40W of losses. As shown, there is no thermal cross-talk between die and the edge of top copper and there is sufficient spacing so that the physical boundary of the system has not influenced the thermal heat flux.

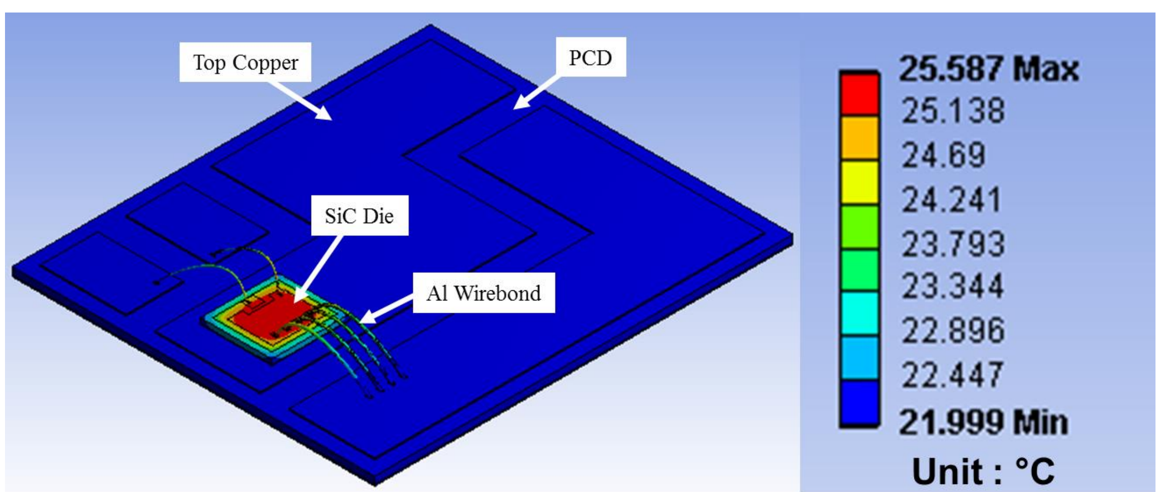

Figure 3.44: Three-dimensional simulation of the silicon carbide dies attached to a PCD tile

Figure 3.45 show the thermal distribution for SiC power device die attached using silver sinterd paste on a poly crystalline diamond substrate. These cut lines are taken through the center of the substrate through SiC die. As shown, due to the higher thermal conductivity of the polycrystalline diamond, the thermal gradient within this layer is significantly reduced compared to the Si and solder dieattach. The maximum junction temperature(T_j) was observed to be 25.5ºC, with a bottom copper fixed at conatant temperature of 22ºC. The thermal resistance junction to case ($R_{th(j-c)}$) of SiC dies mounted over PCD substrate using silver sinterd paste was calculated to be 0.08ºC/W using equation (3.1).

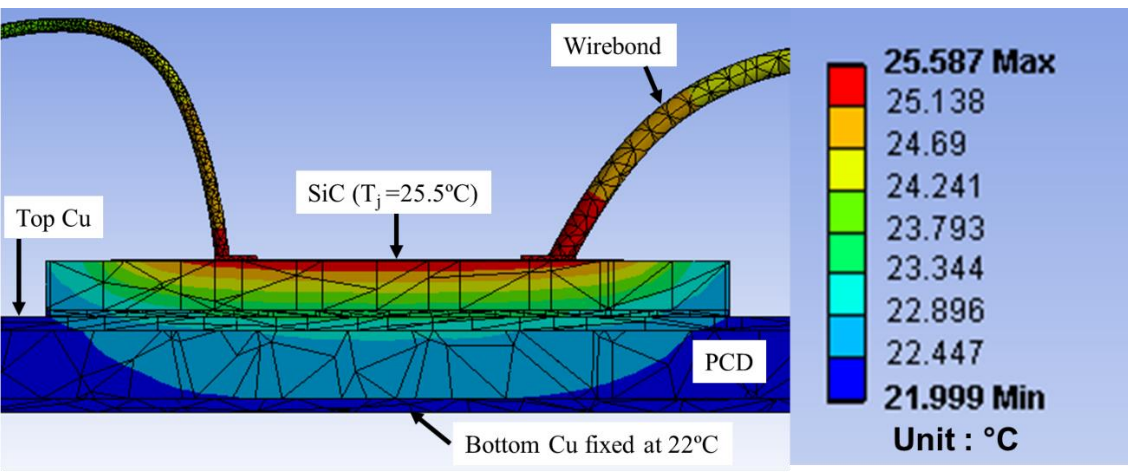

Figure 3.45: Cross-sectional Thermal contours of SiC dies on PCD tile using silver paste die attach

Table 3.7 compares the thermal resistance juction to case ($R_{th(j-c)}$) for Si solder dieattach and SiC silver-sintered die attach mounted over polycrystalline diamond substrates. Thermal reisitance junction to case ($R_{th(j-c)}$) results for Si power devices mounted over polycrystalline diamond substrates using solder paste were discussed in section 3.5.4. As shown in Figure 3.46, next generation technology SiC and silver sinterd die attach reduces the thermal resistance juction to case ($R_{th(j-c)}$) from 0.25 to 0.08ºC/W due to better thermal conductivity of SiC and silver sinterd paste when compared over converntional Si and solder(SnAg) paste.

Table 3.7: Si-SnAG & SiC-Silver sintered paste comparison

PCD tile	T_j	ΔT	$R_{th(j-c)}$
Si-SnAg die attach	35ºC	10ºC	0.25 ºC/W
SiC- Silver sinterd paste	25.5ºC	3.5ºC	0.08 ºC/W

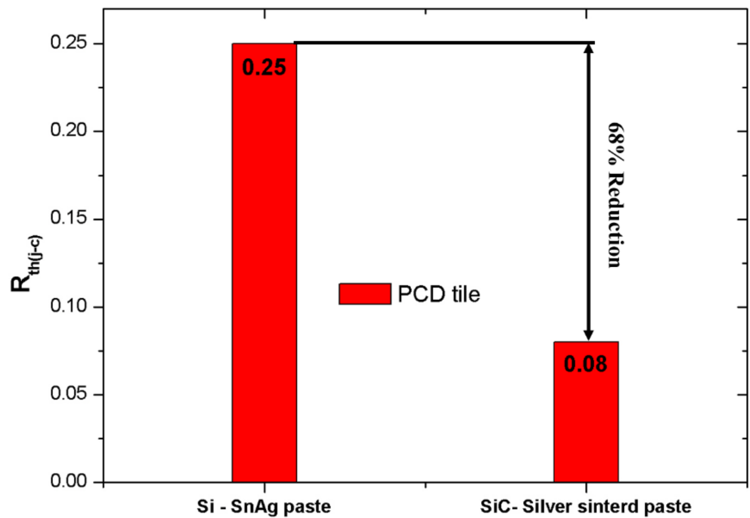

Figure 3.46: Thermal resistance reduction in percentage

3.6.3 Thermal cycling reliability

Thermal cycling of SiC silver sinterd paste die attach on PCD tiles were analysed using ANSYS® static structural analysis. Similar thermal loading condition were used as shown in Fig 3.30. Equivalent strain contours for SiC silver sinterd paste die attach on PCD tiles observed at 150ºC is shown in Figure 3.47.

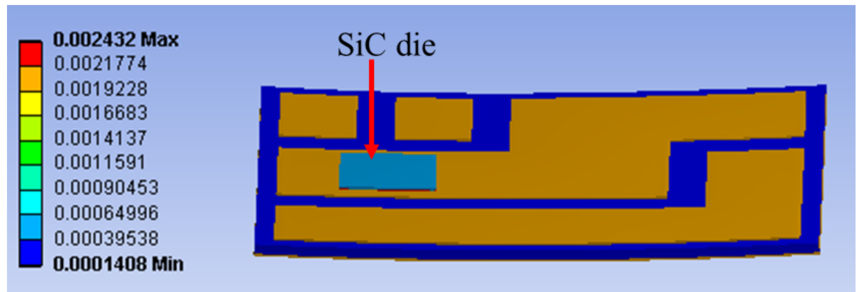

Figure 3.47: Thermal strain contours for SiC die mounted over polycrystalline diamond tile using silver sinterd die attach at 150°C

Equivalent stress contours for SiC silver sintered paste die attach on PCD tiles observed at 150ºC is shown in Figure 3.48.

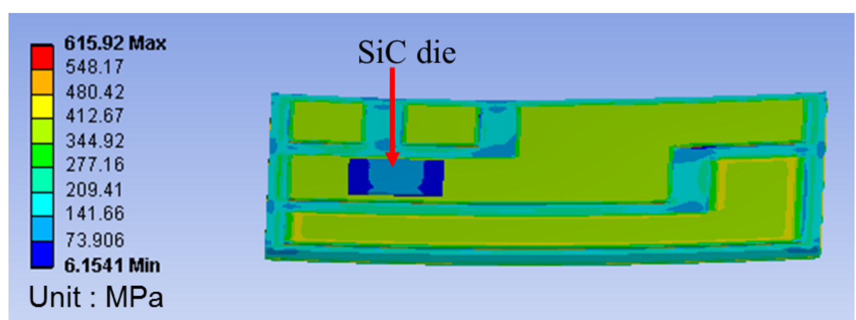

Figure 3.48: Thermal stress contours for SiC die mounted over polycrystalline diamond tile using silver sinterd die attach at 150°C

Table 3.8 shows the comparison of thermal stress and safety factors for Si - SnAg and SiC – silver sintered mounted over PCD substrates. As shown SiC- silver sintered die attach improves the safety factor from 0.3 to 1.3 on the die attach layer when compared over the conventional Si – SnAg die attach, which is ~3x better reliable.

Table 3.8: Comparison of thermal stress and safety factors for Si - SnAg and SiC – silver sintered mounted over PCD substrates

	PCD tile			
	Si - SnAg		SiC - silver sinterd	
Parameter	**Equivalent stress (MPa)**	**Safety factor**	**Equivalent stress (MPa)**	**Safety factor**
Si/SiC	34	15	88.6	15
Die attach	130	0.3	33.7	1.3
Top/Bottom copper	390	0.3	391	0.3
Ceramic	136	9	145	8.7

3.7 Conclusion

In this chapter, an assessment of thermal performance of PCD and AlN substrates under steady state and transient condition, based on experimental measurements is presented. Extensive experimental results has proven that replacing the AlN insulating layer with a PCD substrate can result in 74% reduction in junction-to-case thermal resistance $R_{th(j-c)}$. In terms of thermal cycling reliability, polycrystalline diamond system exhibits similar reliability aspect when compared over the conventional AlN system with respect to safety factor and life cycle fatigue. Thermal simulation results performed using Ansys predict that the ploy crystalline diamond thermal resistance is less sensitive to layer thicknesses. The voids in the solder and copper layers does not play a significant contribution in terms of thermal contact resistance as the void percentage remains less than 1% of the solder and copper layer area. The increased thermal performance of PCD can benefit from a ~2 x increase in the current rating and switching frequency by a factor of ~5.7 when compared over AlN tile for a 600V DC-DC converter application. PCD when used in power module it could significantly increase the power density of the system. PCD has shown low thermal resistance, better thermal performance than conventional AlN which could be benefited from increase in converter power density by reducing passive filtering components as a result of the increased frequency and increase power density. Due to poly crystalline diamond reduced thermal resistance junction to case ($R_{th(j-c)}$), could offer significant advantages over next generation high power density devices like wide

bandgap semiconductors, such as SiC power devices. When SiC power device mounted over PCD substrate using silver sintered paste die attach reduces thermal resistance junction to case ($R_{th(j-c)}$) by 63% when compared over the conventional Si - solder (SnAg) paste die attach. PCD has shown low thermal resistance, better thermal performance than conventional AlN substrate but however PCD is limited in terms of cost factor as it is five times greater than conventional AlN substrates.

PCD has shown improved thermal performance than the conventional AlN substrates. In the next Chapter, a discussion on further enhancing the thermal performance of PCD insulator on DBC substrate by using direct liquid cooling technique.

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CHAPTER 4 : DIRECT COOLING OF POLYCRYSTALLINE DIAMOND SUBSTRATES

4.1 Introduction

Recent advancements in power electronic systems has resulted in decreasing the die size and increasing the power density, this in turn steadily increases the heat dissipation. High power density modules are widely used in many applications and require effective thermal management solutions for a reliable operation. Lack of appropriate cooling system would result in increased die junction temperature and possible failure of the power module, due to the dependency of die junction temperature and reliability. Power module packages in general consist of power semiconductor dies attached on to a DBC substrate using die attach material. The DBC substrates are then soldered on a base plate which acts as a mechanical support and a heat spreader when the module is attached to the heat sink. A thermal interface material is used between the heat sink and the base plate to achieve a good thermal contact. The Figure 4.1 shows a typical cross section of a conventional power module.

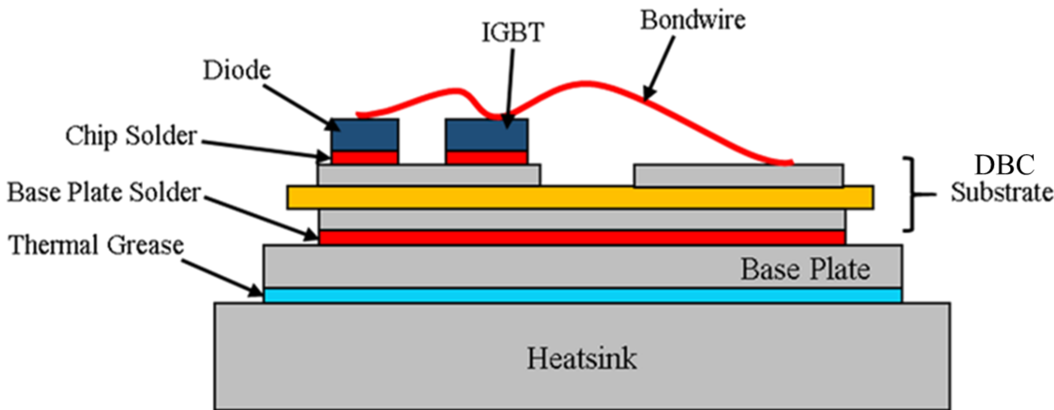


Figure 4.1: Cross sectional view of a power module

A pie chart as shown in Figure 4.2 represents junction to case thermal resistance contribution for a power module (as depicted in Figure 4.1) with AlN as ceramic layer. The majority of the thermal resistance is contributed by the copper base plate and the thermal interface material due to the poor conductivity of thermal interface material and the bulk thickness of copper base plate.

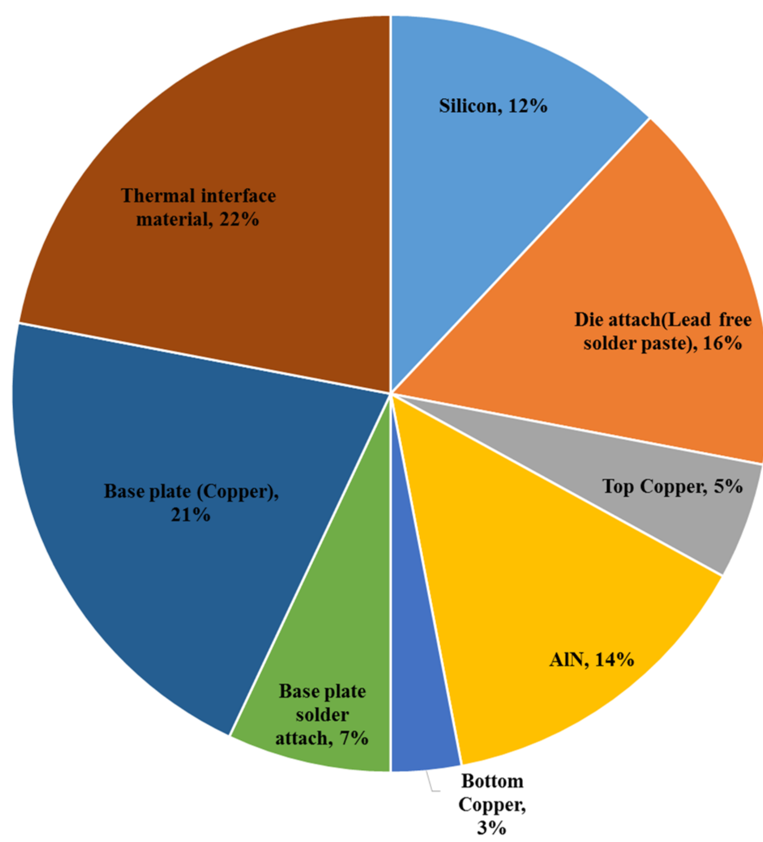


Figure 4.2: Percentage of thermal resistance contribution [1]

In this chapter, the thermal performance of PCD isolation layer on a DBC substrate was further enhanced by using a direct liquid cooling technique. Micro fins were embedded on to the bottom copper of the DBC substrate with PCD as insulation layer. This reduces the number of thermal layers in the system and in turn will increase the thermal performance. Moreover, the high thermal conductivity of PCD can be utilised efficiently by using direct cooling technique. Different micro pin fin geometries and its thermo-hydraulic parameters were varied to find the optimum thermal performance.

4.1.1 Direct cooling of base plate

In order to increase the thermal performance and to reduce the number of thermal layers many advancement were made for direct liquid cooling of power module. Chun-Kai[2] proposed direct cooling of IGBT power modules using micro channel structures embedded on to the copper base plate as shown in Figure 4.3. This eliminates the need for thermal interface material which has a very poor thermal conductivity and constitutes to the majority of the overall thermal resistance as shown in Figure 4.2.

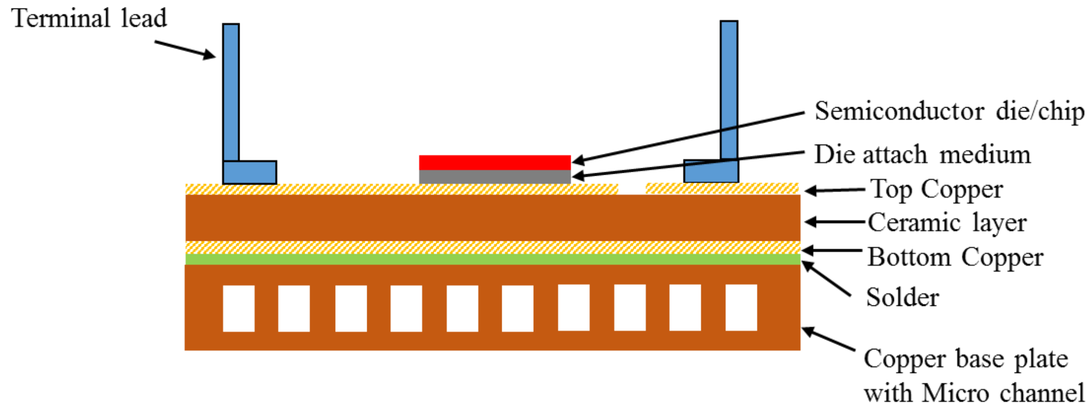


Figure 4.3: Micro channel structure for direct cooling of base plate[2]

The micro channel structure resulted in direct liquid cooling on the base plate and has shown a reduction of thermal resistance by 25% when compared to the conventional liquid cooled module. Figure 4.4 shows the photographic view of the micro channelled base plate.

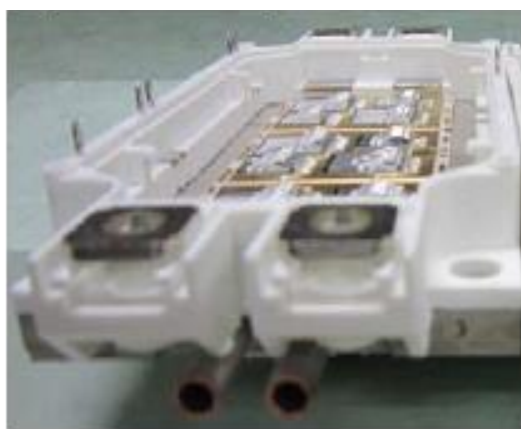


Figure 4.4: Photographic view of Micro channelled base plate[2]

4.1.2 Double sided cooling

Double sided cooling was developed for embedded power module packaging enabling improved thermal performance for non-wire bonded modules. Figure 4.5 shows the embedded power module package with top and bottom side cooling. The semiconductor devices are die attached on to the DBC substrates and on the top side of the semiconductor device the electrical connections were made via a solder mask and etched copper metallisation enabling non wire bond interconnections. This kind of arrangement enables cooling on the top side of the semiconductor die as well and reducing the number of thermal layers without the base plate heat spreader. This results in simultaneously cooling the top and bottom sides of the power

module and improving the heat transfer efficiently out to the ambient from the semiconductor die. The heat transfer rate was further improved by forced jet impingement cooling techniques, on both the top and bottom sides of the power module. However, the double sided cooling techniques are still within research level as it imposes difficulties in terms of electrical connections.

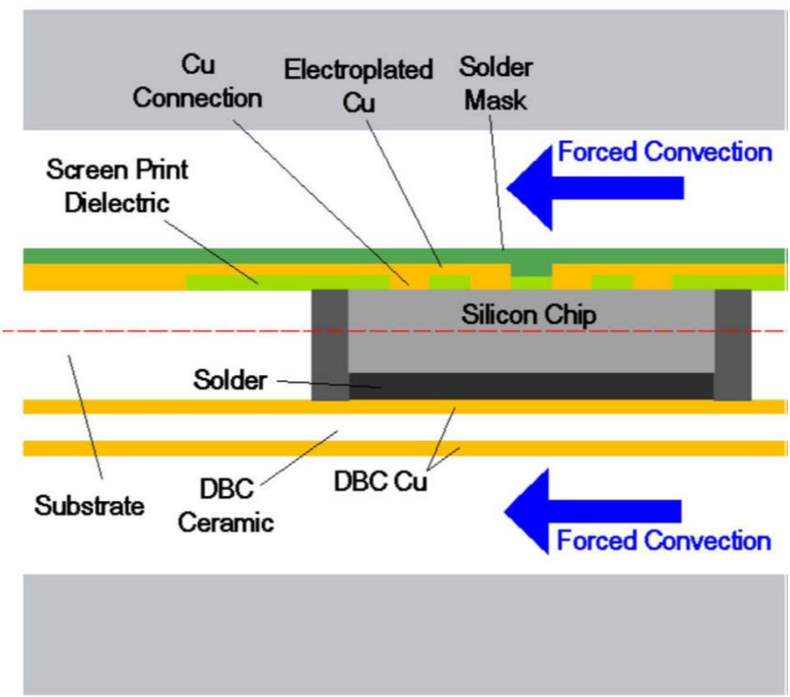


Figure 4.5: Double sided cooling for embedded power module [3]

4.1.3 Direct cooling of power modules (without base plate)

The pressure contact modules[4] which are next step in cooling the power modules, pressure contacts were used to replace the bonded interfaces by reducing the thermal bonded interfaces. Electrical spring connectors were used to apply the pressure evenly over the DBC tiles, to improving the thermal, thermomechanical reliability and electrical performance. Figure 4.6 shows the Semikron power module without the base plate and the pressure contacts. The module developed benefits from both improved thermal performance by eliminating the copper base plate and increasing the thermal cycling reliability as the thermal stress form the base plate is removed.

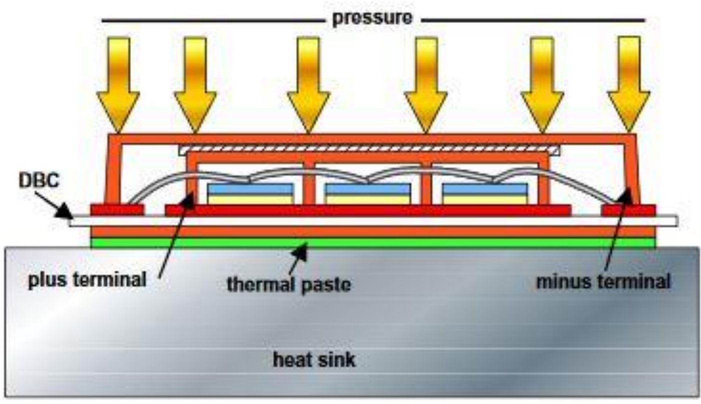
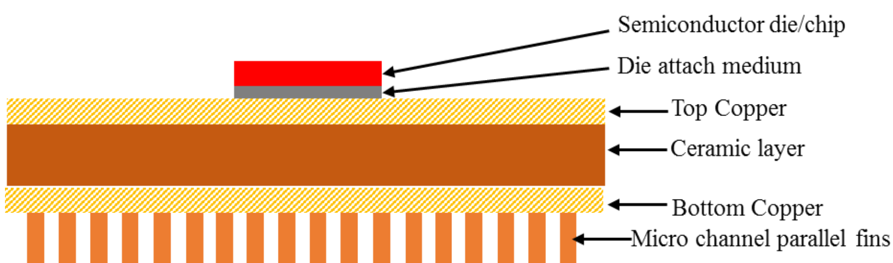


Figure 4.6: Semikron power module[4]

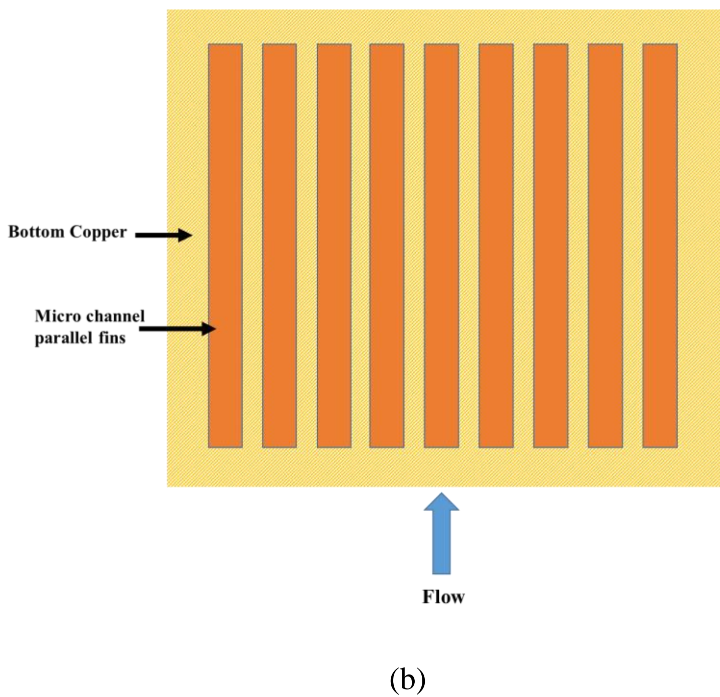
Even though the semikron's base plate less technology has shown improved thermal performance form junction to case and thermo mechanical reliability by removing the base plate and solder joints compared to conventional module as shown in Figure 4.1. However, the amount of heat transferred to the ambient is limited by the thermal interface material (which has high thermal resistance) between the heat sink and the DBC substrate.

4.1.3.1 Micro channel structures

Micro channel structures enables direct cooling DBC substrates by eliminating the thermal interface material. Liquid cooled micro structures with high heat transfer coefficients have proven to be a potential solution in the next generation thermal management challenges. Micro channel parallel fins have shown improved thermal performance when compared over other micro structures [5-8], Figure 4.7 shows micro channel parallel fins on a DBC structure as a cross sectional (a) and top view (b). The advantages of micro channel fins are very low thermal resistance for high heat flux, extracting heat efficiently to the outside ambient and high heat transfer co-efficient; for a small volume and reduced size [9]. The main disadvantage of this structure is the micro channel parallel pins are arranged in inline resulting in laminar flow between the channels. Therefore, the cross flow action (turbulent flow) cannot not be achieved which could increase the heat transfer efficiently when compared to the laminar structures[10].



(a)



(b)

Figure 4.7: (a) Cross sectional schematic of micro channel parallel fins in a DBC substrate; (b) Top view

4.1.3.2 Micro pin fin structures

Advancement in micro-fabrication technology has led to investigate the performance of more complex structures, such as micro pin fins. Micro pin fins can be fabricated to the bottom copper of the substrates using LIGA (Lithographie, Galvanik and Abformung) fabrication or other electroforming process techniques, enabling structures with high heat transfer co-efficient. Figure 4.8 shows a thermal resistance comparison for micro channel fin [10] and micro pin fin structures with respect to fin heights at a fixed flow rate of water at 1 lpm with identical wetting area and material. The Micro pin fins structures shows reduced thermal resistance when compared to micro channel structures due to the enhanced cross flow action (turbulent flow).

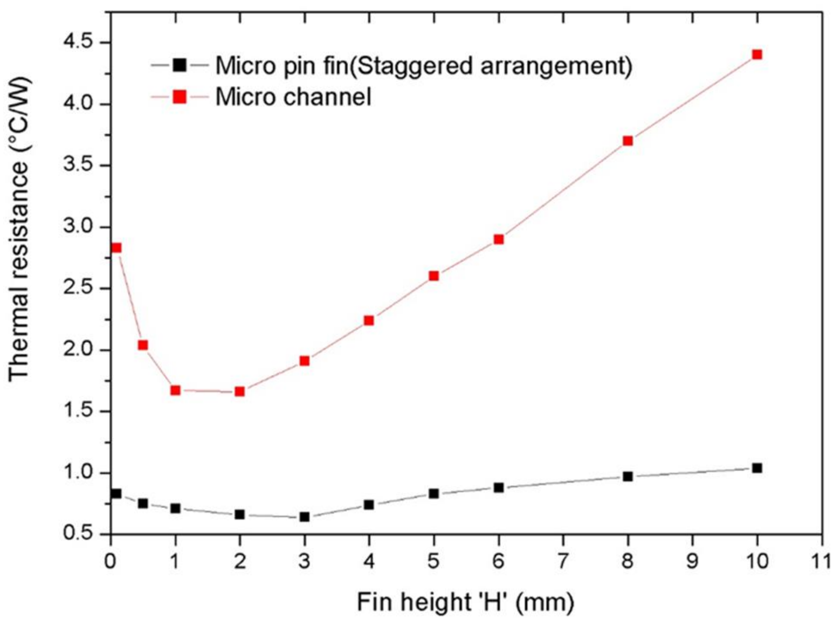
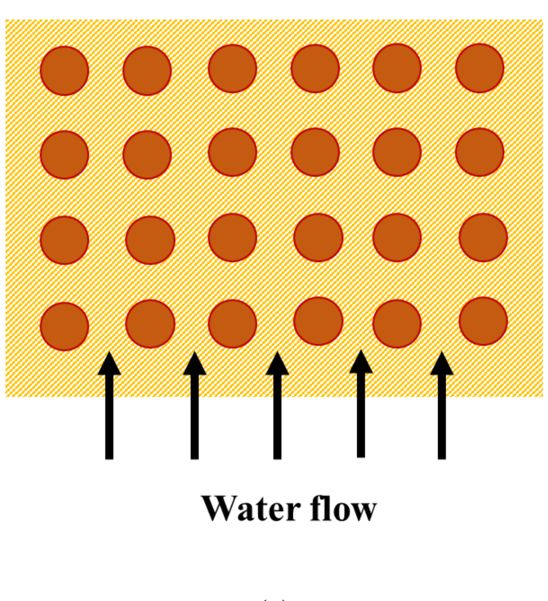
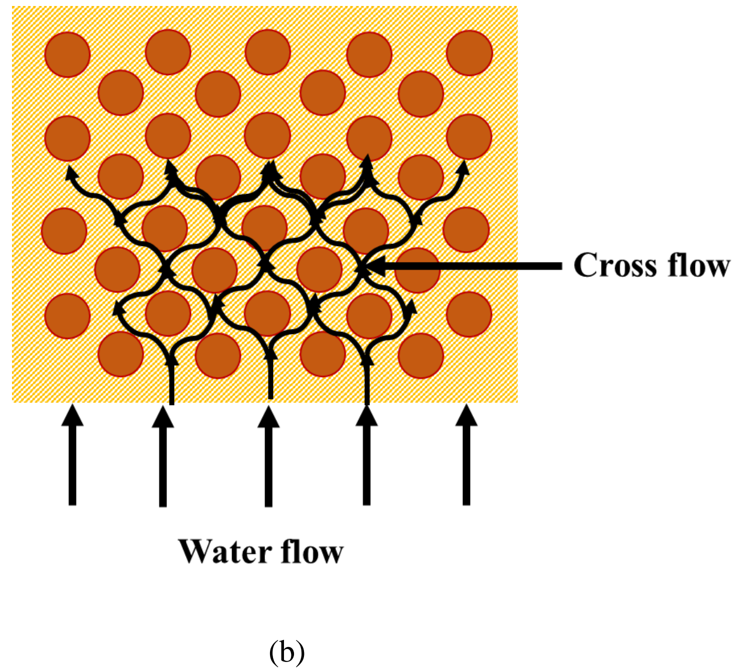


Figure 4.8: Thermal resistance comparison between micro channel fin and micro pin fin structures[10]

Staggered micro pin fin arrangement seems to be a promising structure in terms of removing high heat flux form the semiconductor device for a given die, tile volume and liquid flow rate [11-14], due to the cross flow action enabling turbulent flow across the pin fin structures. Figure 4.9 shows the flow action on an in-line and staggered micro pin fin.



(a)



(b)

Figure 4.9: (a) Micro pin fin in-line arrangement (b) Micro pin fin staggered arrangement

Many studies have been practised on influence of micro pin fin structure shapes upon thermal performance, starting from rectangular, circular and cone shaped structures. Ali Kosar and Yoav Peles [15] has compared the thermal performance of five different micro pin fin structures keeping the wetting area and fin heights constant as shown in Figure 4.10.

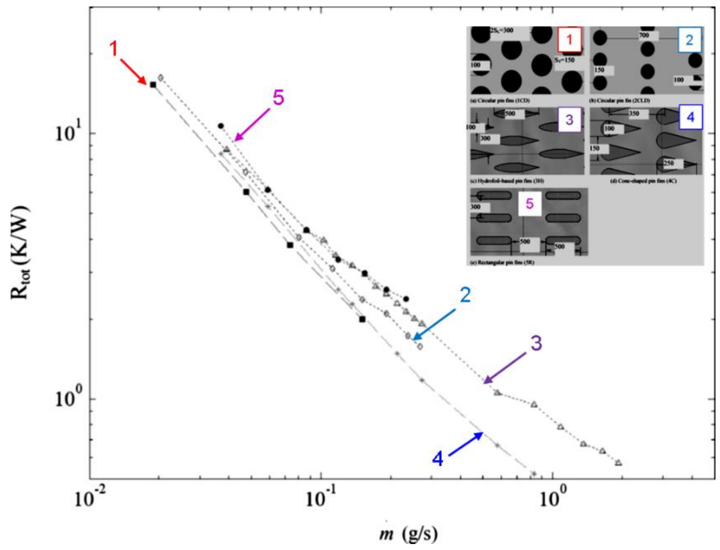


Figure 4.10: Thermal resistance comparison of circular, hydrofoil, cone and rectangular shaped micro pin fin structures[15].

Circular and cone shaped micro pin fin structure has shown reduced thermal resistance when compared to the rectangular and hydro foil shaped structures due to its enhanced micro pin fin

shape structure enabling more turbulent flow for the circular and cone shaped micro pin fins. For this work circular and micro pin fin structures were considered for embedding on to the bottom copper of the DBC substrate with PCD as ceramic layer.

4.2 Empirical model

Due to the complexity of liquid flow and heat transfer rate in the micro pin fins no accurate analytical or numerical method is available to predict the thermal performance of micro pin fins. Present studies on thermal performance of micro pin fin are based upon empirical methods, for this analysis a simplified empirical[13] based expression for estimating thermal resistance for a circular micro pin fin structures was used. The empirical equations from [13] were modelled in Matlab Simulink to calculate the circular fin pin thermal resistance and pressure drop based upon pin geometries, liquid flow rate and thermo-hydraulic conditions. Figure 4.11 shows the empirical based Simulink model for determining thermal resistance and pressure drop in circular micro pin fin. The model is divided into five blocks including input, pressure drop, Reynolds number, thermal resistance and output blocks.

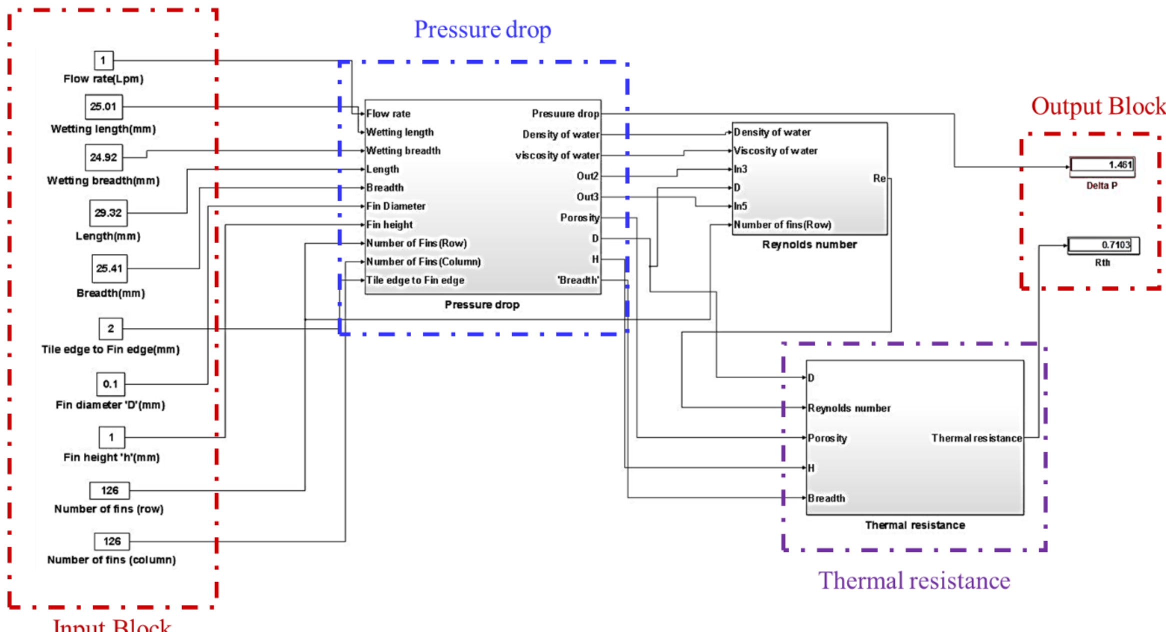


Figure 4.11: Simulink model for determining Thermal resistance and pressure drop on a circular micro pin fin.

4.2.1 Input block

The empirical model uses the circular micro pin fin shape geometries, liquid flow rate and its thermos-hydraulic parameters to determine the pressure drop and thermal resistance. Figure 4.20 shows the geometric parameters required for estimating the thermal resistance and pressure drop.

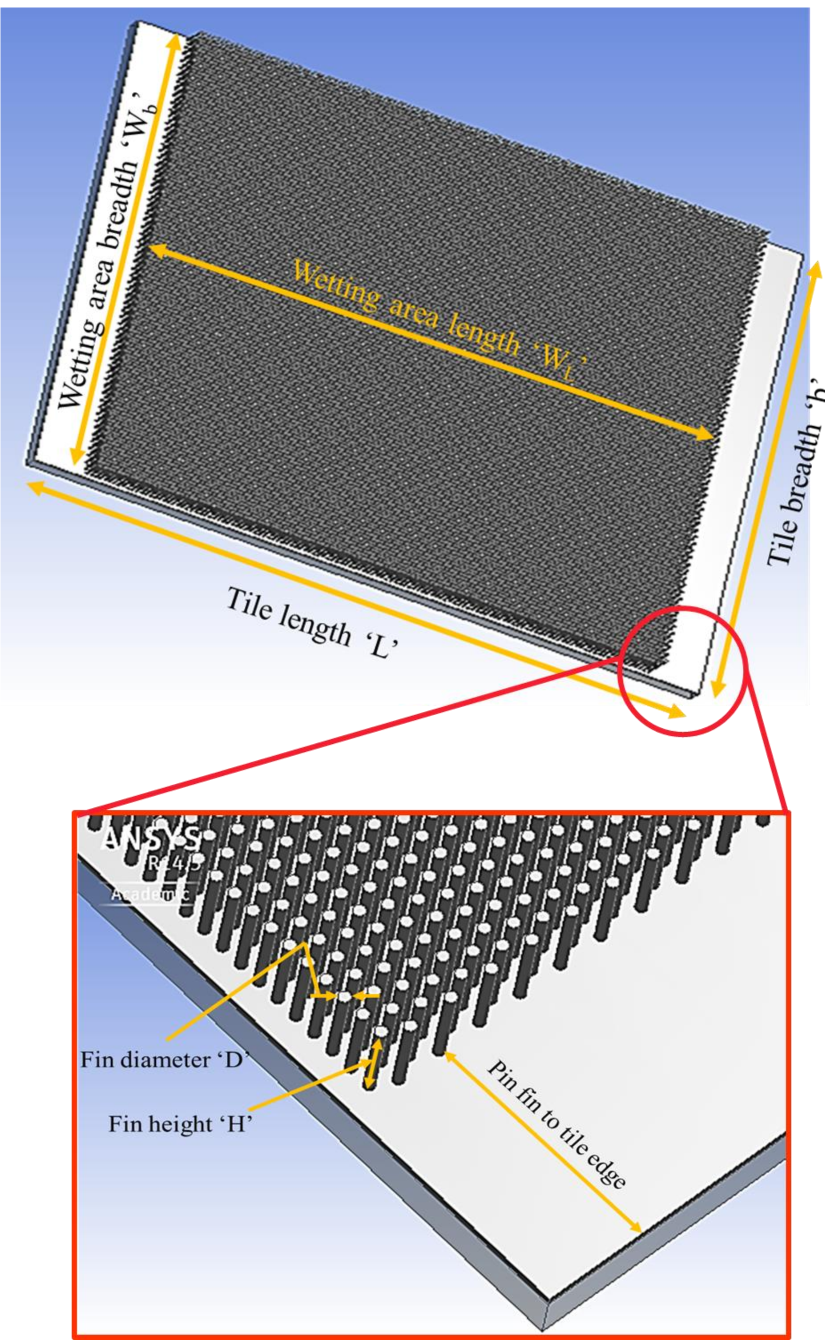


Figure 4.12: Pin fin geometry parameters

The PCD tile area of 29.32mm x 25.41mm with 100/500/100 µm of Cu/PCD/Cu thicknesses as detailed in Chapter 2 was considered for this work. Water cooling with a 2mm spacing was

used between the tile to the micro pin fin edge for enclosure and mounting considerations. Parameters such as fin height, diameter and water flow rate were varied to find the optimum thermal performance. Table 4.1 summarises the geometric parameters used in the empirical model. The number of pin fins in a row and column are calculated based upon the wetting area length ‘W_L’, wetting area breadth ‘W_B’ and pin fin diameter used.

Table 4.1: Geometric parameters considered

Parameter	Values considered
Water Flow rate	Varied from 0.5 to 4 lpm
Tile length ‘L’	29.32 mm
Tile breadth ‘B’	25.41 mm
Wetting area length ‘W_L’	25.01 mm
Wetting area breadth ‘W_B’	24.92 mm
Pin fin to Tile edge spacing	2 mm
Pin fin diameter ‘D’	Varied from 0.1 to 0.4 mm
Pin fin height ‘H’	Varied from 0.5 to 3 mm

4.2.2 Pressure drop

The pressure drop is an important parameter directly influencing the performance of micro pin fin structures as it is directly proprtional to the flow rate and inversly proportinal to the micro fin height. The over all pressure drop of overall is calculated based upon the mass flow rate, pin fin height, diameter, number of pin fins (N) and water viscosity, as shown in equation (4.1).

$$\Delta P = \frac{m_f}{\left(\frac{\rho D^3}{90\mu}\right)\left(\frac{N_{row}}{N_{column}}\right)\left(\frac{H}{D}\right)\left(\frac{1-\varepsilon}{\varepsilon}\right)^{0.4}\left(\sqrt{\frac{\pi}{4(1-\varepsilon)}}-1\right)} \quad (4.1)$$

m_f,μ and ρ represents mass flow rate, vicosity and density of water. Where as N, D, H and ε are number of fins, fin diameter,fin height and porosity respectively. Porosity ‘ε’ is calculated based on the wetting area and micro pin fin density. Pressure drop has a direct relation to mass flow rate and the number of pin fins. The pressure drop is expected to be lower than the standard atmospheric pressure drop(1atm) due to its inverse relation with respect to micro pin fin height.

4.2.3 Reynolds number

Reynolds number, calculated by equation (4.2), is used to determine laminar or turbulent flow in a system. Reynolds number is calculated based upon the fin diameter, number of fins, porosity and pressure drop. The mass flow rate is directly related with pressure as represented by equation (4.1). If the system has Reynolds number <2300 the flow is laminar, if this number is >2300 it is in said to be in turbulent flow [10].

$$R_e = \frac{\rho D^2}{90\, \mu^2\, N_{row}} \left(\frac{1-\varepsilon}{\varepsilon}\right)^{0.4} \Delta P \qquad (4.2)$$

For flow rates from 0.5 to 4 lpm and based upon the circular pin fin geometric structure, system has a Reynolds number <2300 i.e, in the laminar flow region. The empirical model considers inlet flow rate of the overall system and doesn't include the flow pattern on the circular fins due to the complex process used to predict the flow around the fins[16].

4.2.4 Thermal resistance

Thermal resistance determines the thermal performance in the fin pins and is a function of geometric parameters involving fin height'H', fin diameter 'D', wetting area length 'W_L' and porosity 'ε'; and thermo-hydraulic parameters; Reynolds number 'Re', Prandtl number 'Pr', thermal conductivity of the fluid 'K_{fluid}' and thermal conductivity of pin fin material 'K_{fin}'. The overall thermal resistance of micro pin fin can be expressed using equation (4.3),

$$R_{th} = 1 + \frac{(Re)^{1-0.4}\, Pr^{0.64}}{\frac{\varepsilon}{\left(1-\sqrt{4(1-\frac{\varepsilon}{\pi}}\right)}\, 0.9 \left(\frac{W_L}{H}\right)\left(\frac{Pr}{Pr_s}\right)^{0.25} \left\{1 + 2\left(\frac{1-\varepsilon}{\varepsilon}\right) \frac{tanh\left[2\left(\frac{H}{D}\right)\sqrt{0.9\,(Re)^{0.4}\, Pr^{0.36}\left(\frac{Pr}{Pr_s}\right)^{0.25}\left(\frac{k_{fluid}}{k_{fin}}\right)}\right]}{\sqrt{0.9\,(Re)^{0.4}\, Pr^{0.36}\left(\frac{Pr}{Pr_s}\right)^{0.25}\left(\frac{k_{fluid}}{k_{fin}}\right)}}\right\}}$$

(4.3)

Table 4.2 summarises the values of thermos-hydraulic parameters considered in the empirical model for a water cooled copper pin fin micro channel. Prandtl (Pr) number gives the information about the type of fluid. Also it provides the information about the thickness of thermal and hydrodynamic boundary layer.

Table 4.2: Thermo-hydraulic parameters

Parameter	Value used
Prandtl number 'Pr' of water @ 25°C	7.01
Prandtl number 'Pr_s' of air @ 25°C	0.71
Thermal conductivity of water 'K_{fluid}' @ 25°C	0.56 (W/mK)
Thermal conductivity of copper fin material 'K_{fin}' (W/mK)	401 (W/mK)

From Equation (4.3) it can be evident that the thermal resistance is purely dependent on geometric parameters, Reynolds number (Re), Pressure drop (ΔP) and Prandtl number (P_r); not the heat flow. The obtained thermal resistance from the empirical model can be used to predict the temperature difference (ΔT) for a given heat flux subject to geometric and thermo-hydraulics parameters.

4.3 Empirical results

The pin fin diameter, pin fin height and flow rate were varied to find the optimum design value for circular pin fins. Thermal resistance and pressure drop are inversely proportional to each other and there is a trade-off between these two parameters. In order to predict the optimum pin fin dimensions, the water flow rate was fixed at 1 lpm and the pin fin geometries are varied. The pin fin diameter were varied from 0.1 mm to 0.4 mm and the pin fin height were varied from 0.5 mm to 3 mm. Figure 4.13 shows the thermal resistance at varying pin fin diameter and height. The thermal resistance increases with fin diameter thicknesses from 0.1 to 0.4 mm whereas, thermal resistance decreases with fin height variation form 0.5 to 3 mm.

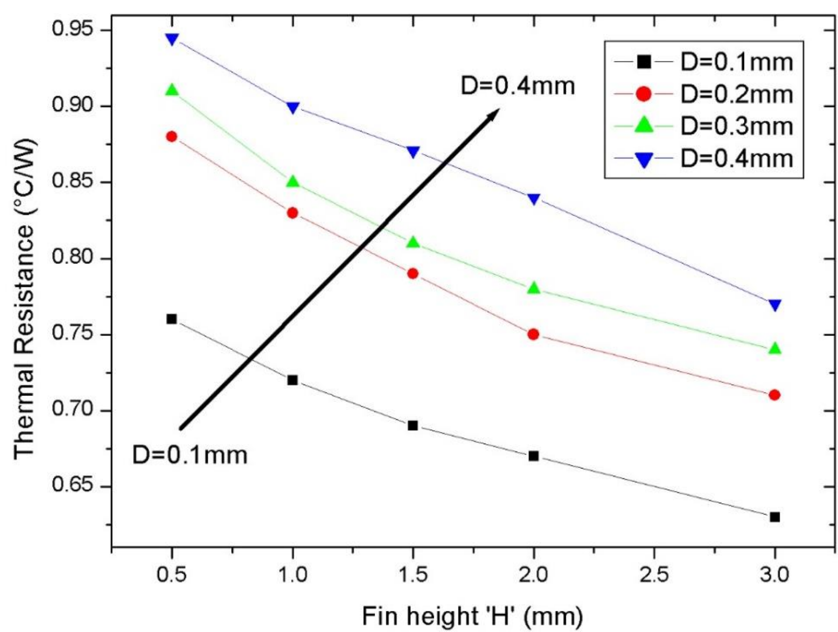


Figure 4.13: Thermal resistance for varying pin fin diameter and height at a fixed flow rate of 1 lpm

Figure 4.14 shows the pressure drop for varying pin fin diameter and height, the pressure drop increases with decrease in fin diameter as its evident the fin density increase would increase the pressure drop. Moreover, the pressure drop decreases with increase in fin height.

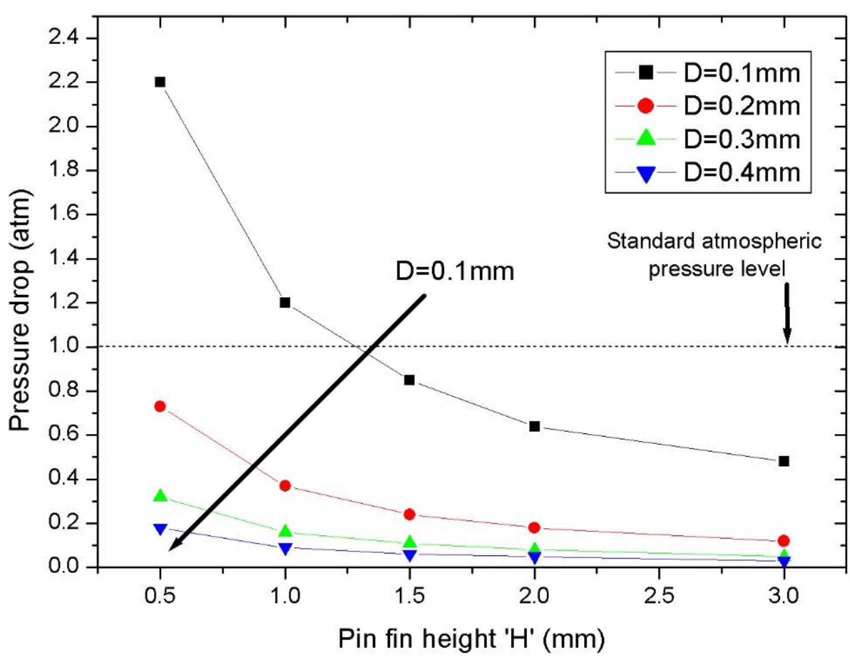


Figure 4.14: Pressure drop for varying pin fin diameter and height at a fixed flow rate of 1 lpm

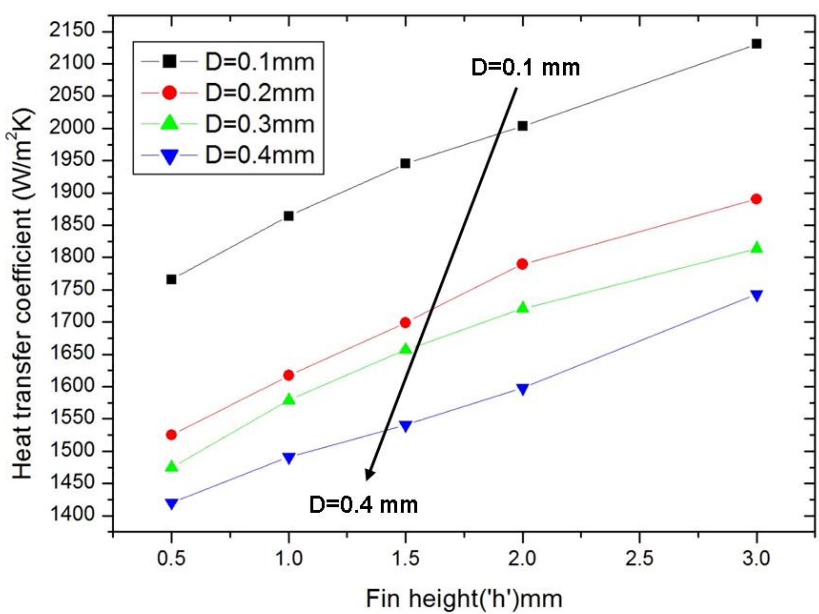


Figure 4.15: Heat transfer co efficient for varying pin fin diameter and height at a fixed flow rate of 1 lpm

Figure 4.15 shows the heat transfer co-efficient for pin fin diameters form 0.1 mm to 0.4 mm with pin fin height from 0.5 mm to 3 mm. Fin diameter D=0.1mm has high heat transfer co efficient due to its reduced thermal resistance when compared to other fin diameters. Fin diameter of D = 0.1mm seems to have the lowest thermal resistance and pressure drop at a standard atmospheric pressure level (1 atm). In order to see the thermal dependency with

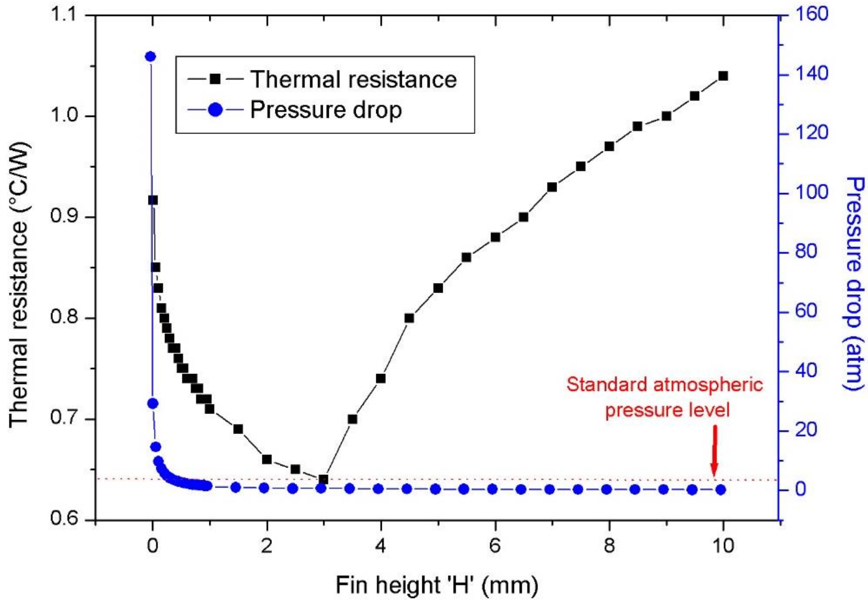


Figure 4.16: Thermal resistance and pressure drop for pin fin D=0.1mm at fixed flow of 1 lpm

respect to fin height, Fin diameter D = 0.1 mm was fixed and its respective height was varied from 0.5 mm to 10 mm. Figure 4.16 shows the thermal resistance and pressure drop for fin diameter D =0.1mm with varying fin height from 0.5 to 10 mm. Thermal resistance starts to decrease from 0.5 mm to 2.5 mm fin height and the thermal resistance increases after 2.5 mm to 10 mm fin height. The pressure drop decreases as fin height increases up to 1 mm and starts to saturate after 1 mm fin height. The potential fin height with improved thermal performance lies between 1 mm to 3 mm fin height as evident from Figure 4.16.

Due to the limitation and complexity in LIGA fabrication technology with high aspect ratio (fin diameter/fin height) structures from external manufacturers, two circular pin fin geometric design were chosen as shown in Table 4.3.

Table 4.3: Circular pin fin designs

Parameter	Fin diameter 'D' (mm)	Fin height 'H' (mm)
Design 1	0.1	1
Design 2	0.2	2

The influence of flow rate upon thermal resistance and pressure drop was analysed for two circular pin fin designs. Figure 4.17 shows the thermal resistance and pressure drop for circular pin fin Design 1(D=0.1mm; H=1mm) with flow rate varying from 0.5 to 4 lpm.

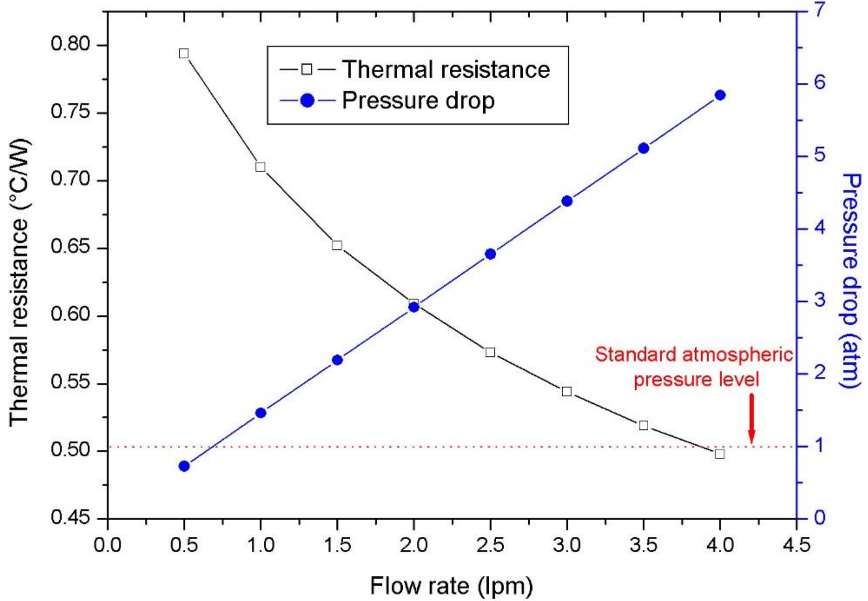


Figure 4.17: Thermal resistance and pressure drop for circular Design 1 (D=0.1mm; H=1mm)

There is a trade -off between thermal resistance and pressure drop with respect to flow rate. Pressure drop is direct relation to flow rate whereas thermal resistance is inversely proportional to the flow rate. The optimum flow rate lies between the 0.5 to 1 lpm, with respect to a pressure drop of 1atm. Figure 4.18 shows the thermal resistance and pressure drop for circular pin fin Design 2 (D=0.2mm; H=2mm) with flow rate varying from 0.5 to 4 lpm. The optimum flow rate for circular pin fin Design 2 lies between 0.5 to 1.5 lpm in consideration with respect to standard atmospheric pressure drop (1 atm). Due to the decrease in pin fin density in Design 2 when compared over Design 1, it is evident that the thermal resistance for Design 2 would be higher than the Design 1.

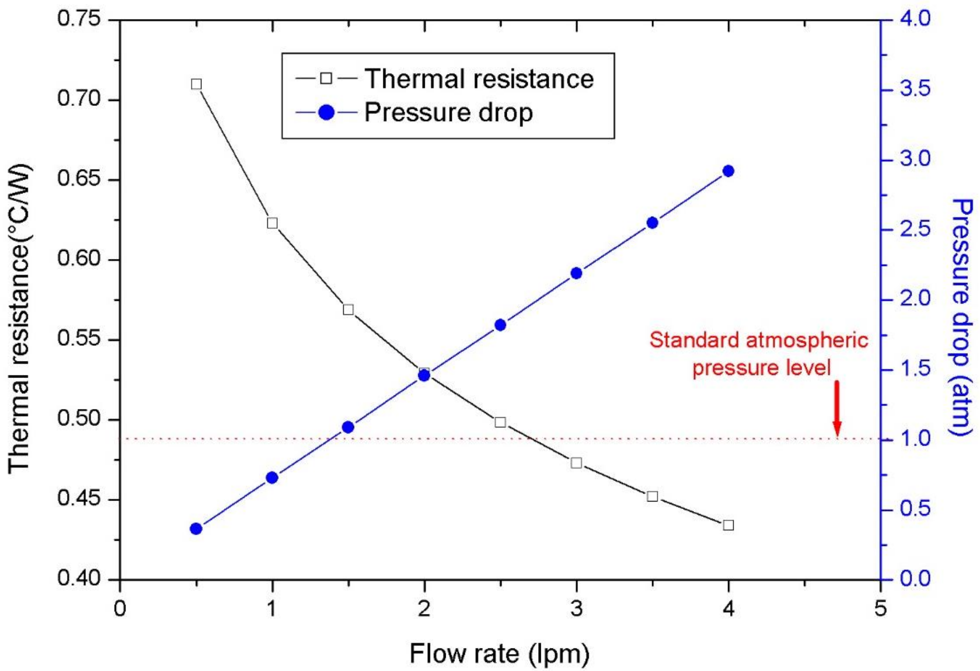


Figure 4.18: Thermal resistance and pressure drop for circular Design 2 (D=0.2mm; H=2mm)

4.4 Comparison between conventional and micro pin fin cooling

Figure 4.19 shows the schematic cross section of a power module without the base plate metal. The DBC substrate is attached to the liquid cooled heatsink using a thermal interface material (TIM), heatsink compound or thermal pad to improve the thermal contact. Commercially used thermal interface material[17] (see Appendix 9) with a thermal resistance of 1.8°C/W based upon the DBC area (29.32mm x 25.41mm), thicknesses of 0.25mm. A liquid cooled heatsink with thermal resistance of 0.30°C/W at a flow rate of 8 lpm as described in Figure 3.10 Chapter 3 was considered for comparative purposes.

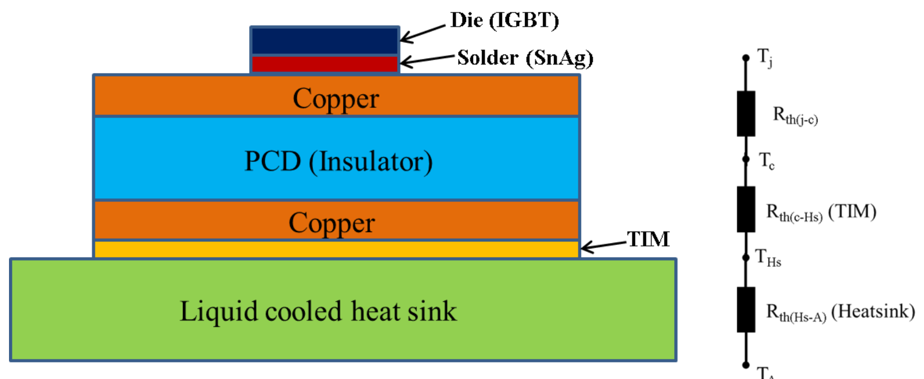


Figure 4.19: Cooling of power module without baseplate

Figure 4.20 shows the cross section of direct cooling of DBC substrate using micro pin fin structures. Circular micro pin fins with thermal resistance of 0.70°C/W at a flow rate of 1 lpm with circular pin fin of diameter (D=0.1mm) and height (H=1mm) was used to compare against a conventional cooling technique.

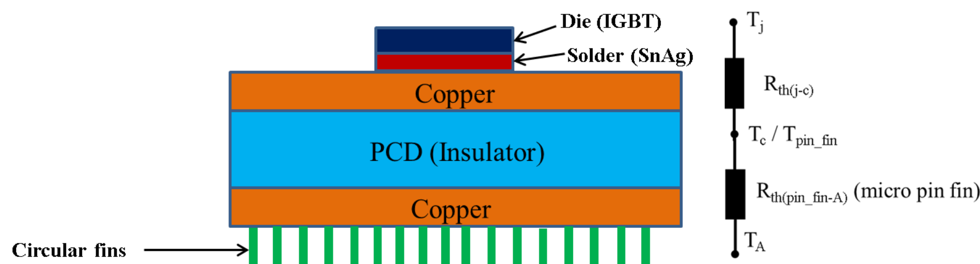


Figure 4.20: Micro pin fin direct cooling of DBC substrate

Figure 4.21shows comparison between the conventional and micro pin fin direct cooling from junction to ambient. The junction to case thermal resistance '$R_{th(j-c)}$' of 0.27°C/W was used, as measured in Chapter 2. Direct cooling of DBC using micro pin fin heat sink has thermal resistance '$R_{th(j-a)}$' (junction to ambient) of 0.97 °C/W which is a 59% reduction when compared to the conventional cooling of DBC substrate without baseplates, which has a thermal resistance '$R_{th(j-a)}$' (junction to ambient) of 2.37 °C/W. The number of thermal layers are reduced in this case by moving towards micro pin fin direct cooling of DBC substrates.

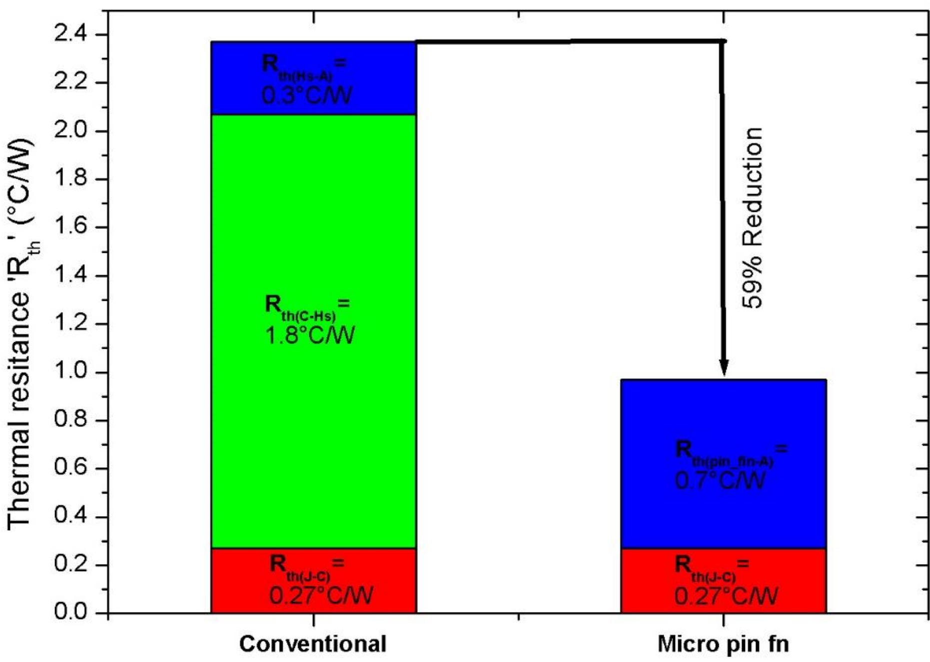


Figure 4.21: Comparison between conventional and micro pin fin direct cooling of DBC substrates

4.5 LIGA fabrication technology

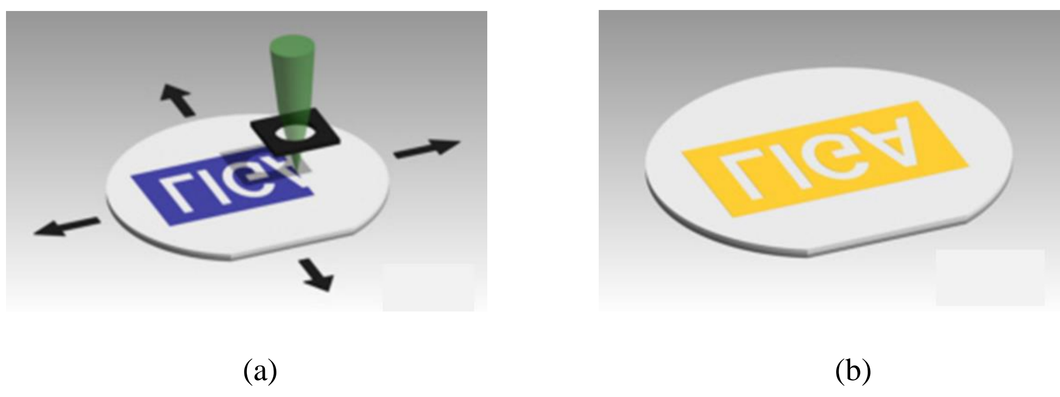
Main advantages of Lithographie, Galvanik and Abformung (LIGA) fabrication is that micro structures can be fabricated with high aspect ratios, high precision, excellent reproducibility, smooth side walls, inclined structures are possible with finest details[18]. X-Ray LIGA fabrication uses X-Rays to create high precession structures and has many advantages over the UV LIGA process as high aspect ratios structures can be fabricated with different kind of materials such as metals, ceramics and plastics. UV LIGA is commonly used in low cost applications where precision and high aspect ratio are not essential. For this work X-Ray LIGA fabrication technique was used to design micro pin fins on the bottom copper of the DBC substrate.

Main fabrication steps in X-Ray LIGA process includes:

4.5.1 Fabrication (Intermediate mask)

The micro pin fin structures were designed on to the CAD system. A resist layer is deposited on top of the substrate and the drawings are transferred on the resist layer using an electron beam, as shown in Figure 4.22 (a). The electron beam writer has high accuracy and moves within close proximity limits of the substrate. The substrate with a resist layer acts as the intermediate mask membrane and is spin-coated with transparent thermoplastic (PMMA) also

known as acrylic glass. The lithography process is initiated on the resist layer which replaces the long chained molecules with short chained as it's important for the wet chemical development process. An absorber material (usually gold) is deposited on to the substrate using electroplating, as it is intensely absorbent to X-Rays, as shown in Figure 4.22 (b). Dry etching processes is used to remove the non-irradiated part of the resist layer.

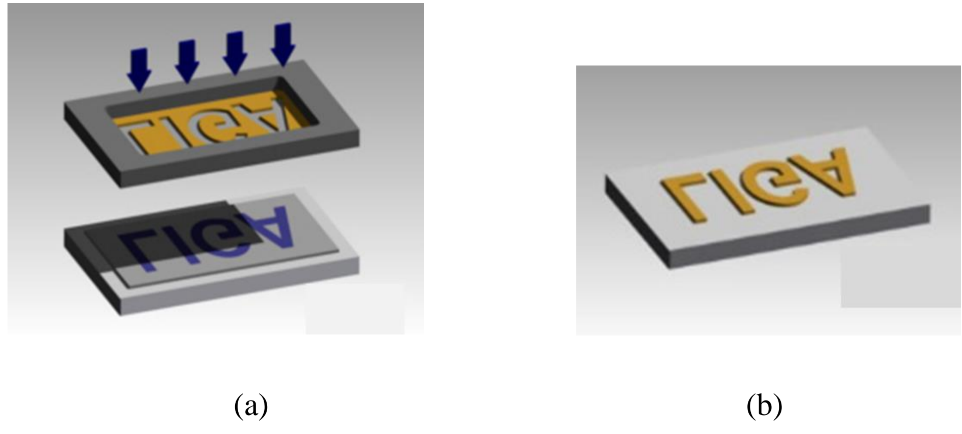


(a) (b)

Figure 4.22:Fabrication[18] (a) Electron beam lithography; (b) Gold electroplating

4.5.2 Fabrication (Working mask)

A working mask is fabricated from the intermediate mask by replicating the gold structures on the working mask via X-Ray lithography using a transparent thermoplastic resist layer as shown in Figure 4.23 (a). The absorber layer (gold) is deposited on to the resist layer using electroplating and is made to expose with X-Rays and the remaining non-irradiated resist layer is removed as represented in Figure 4.23 (b).

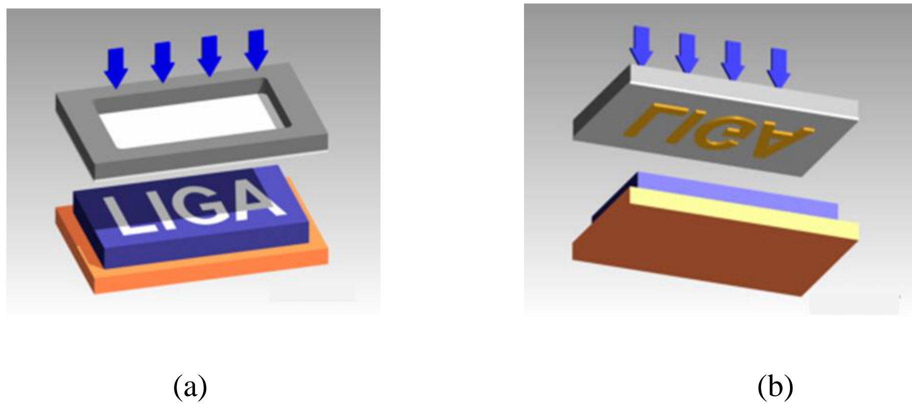


(a) (b)

Figure 4.23: Working mask[18] (a) X-Ray lithography; (b) Gold deposition on resist layer

4.5.3 Microstructure fabrication

The fabricated working mask is used as a tool to for implementing deep X-ray lithography structures on to a separate transparent thermoplastic resist layer as shown in Figure 4.24. The transparent thermoplastic are bonded on to the substrate as foils and later wet chemical development process is done on the irradiated parts of the PMMA resist layer which is shown in Figure 4.25.



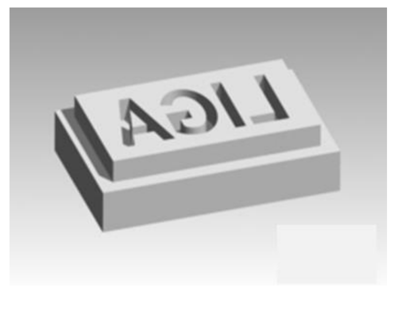
(a) (b)

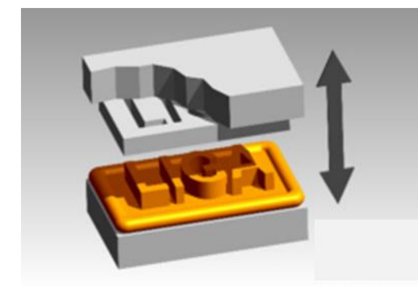
Figure 4.24: X-ray lithography process [18](a) Top isometric view; (b) Bottom isometric view

Figure 4.25: Fabricated microstructures[18]

4.5.4 Electroforming

The fabricated micro structures are submerged on to the electrolytic bath and the desired metal material, copper for this work, is deposited on to the irradiated parts of the microstructures. The electroplating process can also be sustained further to make a mould with the fabricated microstructures as shown in Figure 4.26 (a). Conventionally nickel or gold is used as metal material, but due to the advancement in technologies copper is also used in the electroforming process. The electroplated microstructures moulds are transferred on to a base material via hot embossing or injection moulding as represented in Figure 4.26 (b).





(a) (b)

Figure 4.26: Electroplating [18](a) Electroplated micro structures; (b) Final structure Injection moulded on to base material.

4.6 Micro structure geometric designs for LIGA process

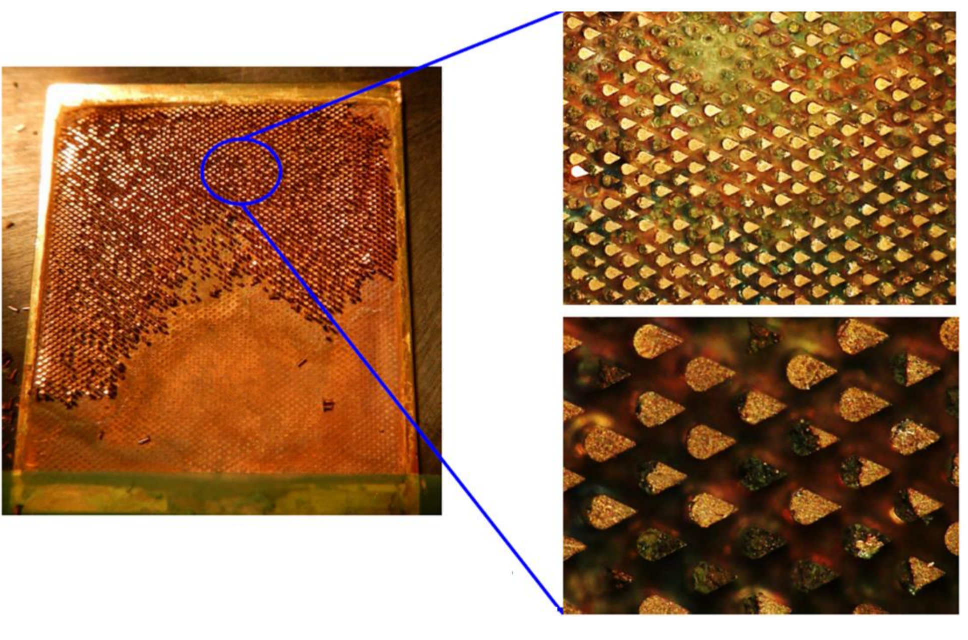
Table 4.4 shows the circular and cone shaped micro pin fins used for LIGA fabrication. There are no empirical model to predict the thermal performance of a cone shaped micro pin fins due to their complex micro structures arrangement. The geometric dimensions for cone shaped pins were approximated based upon the performance of circular pin fin diameters and height. This kind of approach would give a good comparison between the circular and cone shaped micro pin fins with varying geometric parameters. The micro structures were outsourced to get manufactured using LIGA technology at Mircroworks precision structures in Germany.

Table 4.4: Circular and Cone shaped Micro pin fins for LIGA fabrication

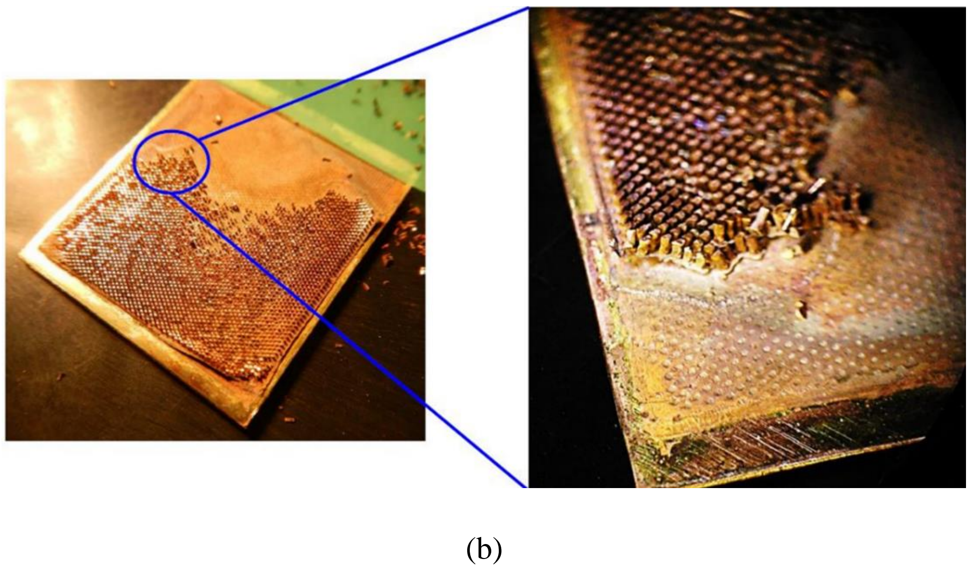
Parameter	Fin diameter 'D' (mm)	Fin height 'H' (mm)	Fin length 'L' (mm)	Micro pin fin shape
Design 1	0.1	1	-	Circular
Design 2	0.2	2	-	
Design 3	0.1	1	0.25	Cone
Design 4	0.2	2	0.3	

4.7 Fabricated micro structures using LIGA technology

The micro structure design geometries as shown in Table 4.4 were fabricated using LIGA technology on to the bottom copper of polycrystalline diamond DBC substrates. The initial LIGA fabricated sample for Design 3 (Cone shaped, D=0.1mm, H=1mm & L=1mm) is shown in Figure 4.27. As shown the micro pin fin cone shaped structures were lifted off in many areas due to the poor adhesion on to the bottom copper of the DBC substrates. The bottom and top copper in DBC substrates are flashed with 4µm of gold for corrosive resistance. The presence of 4µm gold layer in the bottom copper led to poor adhesion. In order to overcome the adhesion issue, the bottom copper gold layer can be removed via chemical etching and sputter deposit 2 µm titanium layer on to the bottom copper layer. Further the titanium layer is etched to obtain a rough topography for good adhesion of resist and the plated layers.



(a)



(b)

Figure 4.27: LIGA fabricated Cone shaped micro pin fin structures (a) detailed view of cone shaped structures; (b) pin fin structure lift off due to poor adhesion

4.8 Conclusion

In this Chapter, an empirical model was used to analyse the thermal performance of circular micro pins fins, geometric and thermo-hydraulic parameters were varied accordingly to find the optimal circular micro pin fin diameter and length. Increase in circular micro pin fin diameter (varied from 0.1mm to 0.4mm) decreases the thermal resistance whereas, thermal resistance decreases with increase in pin fin height (varied from 0.5 mm to 10 mm) up to 2.5mm. Moreover, pressure drop increases with decrease in fin diameter and fin height. There is a trade -off between thermal resistance and pressure drop with respect to flow rate as pressure drop is a direct relation of flow rate, whereas thermal resistance is inversely proportional to the flow rate.

Micro pin fin direct cooling of DBC reduces the number of thermal layers in the system which in turn reduces the thermal resistance by 59% when compared to conventional DBC cooling without base plates. Moreover, the high thermal conductivity of PCD can be utilised efficiently by using direct cooling technique. Four micro pin fin designs (two circular and two cone shaped micro pin fin) were chosen for fabrication using LIGA technology. Initial fabrication have suffered from adhesive issues between the bottom copper and micro pin fins due to the gold layer in bottom copper. Therefore, an alternative solution is being applied to rectify the problem by removing the gold layer via chemical etching and sputter deposit 2 µm titanium layer on to the bottom copper layer. Further the titanium layer is etched to obtain a rough topography for good adhesion of resist and the plated layers.

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CHAPTER 5 : THERMAL PERFORMANCE OF GAN FACE UP AND FLIP CHIP PACKAGING IN T0-220

5.1 Introduction

In this Chapter, numerical comparisons of the thermal performance of face up and flip chip Gallium Nitride (GaN) semiconductor devices grown on Sapphire, Silicon and 6H-Silicon carbide substrates mounted on T0-220 package system; under steady state and transient conditions is presented. GaN semiconductors devices are being emerged and widely used in high power density and higher voltage operational applications due to its increased electric field strength, higher efficiency and smaller foot print. However, heat removal from GaN devices and electronic packages seems to be more challenging due to higher heat flux and smaller device foot print. For years, work on wide band gap materials and devices has promised substantial improvements over the conventional Si based counterparts with their capability to operate at high temperature, high power density, high voltage and high frequencies to make it more attractive for future of electronics. SiC and GaN are two important wide band gap semiconductors showing better future in high frequency and high power density applications.

5.1.1 Material Properties

The material property of the wideband gap semiconductor relates to the energy essential for an electron to be transferred from the top of the valence band to the bottom of the conduction band. The materials with this essential energy of more than one or two electron volts (eV) are stated to be wide bandgap materials. Figure 5.1 compares the specific on state resistance and breakdown voltage for different semiconductor device technologies (see Appendix 10). GaN has low on-state resistance and high breakdown voltage when compared to SiC and conventional Si semiconductor device technologies.

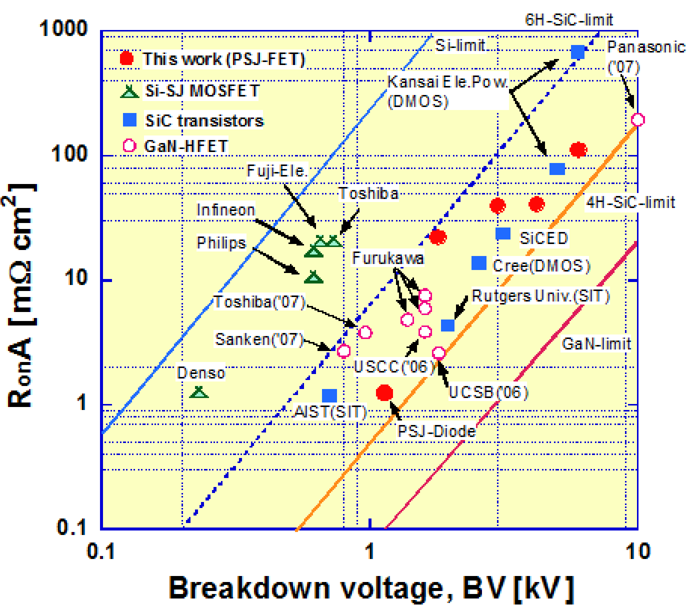


Figure 5.1: On state resistance and breakdown voltage for various semiconductor device technologies [1, 2]

Table 5.1 compares the material properties of Si, 4H-SiC and GaN semiconductors. Typically SiC and GaN are referred to as compound semiconductors as they compose of multiple elements in the periodic table.

Table 5.1: Material properties of Si, 4H-SiC & GaN[3]

Materials Property	Si	4H -SiC	GaN
Band Gap (eV)	1.1	3.2	3.4
Dielectric strength 10^6 V/cm	0.3	3	3.5
Electron Mobility (cm^2/V-sec)	1450	900	2000
Electron Saturation Velocity (10^6 cm/sec)	10	22	25
Thermal Conductivity (W/m K)	150	370	130

The material properties, listed in Table 5.1, have major influence in the fundamental design and performance characteristics of semiconductors, among which SiC and GaN have superior material properties making more suitable for high power density and high frequency applications. The dielectric strength is the maximum electric field that a material can withstand under ideal conditions without breaking down. The dielectric strength material property of SiC and GaN are very high when compared to Si which makes the device capable to operate at higher voltages at low leakage currents. Due to high electron mobility and electron saturation velocity of GaN makes it substantially the best suitable device for very high frequency

operations. The relatively poor thermal conductivity of GaN signifies the requirement of efficient thermal management solutions and mounting techniques in order to remove the heat efficiently from the device.

5.1.2 GaN substrate options

GaN wafers can be processed via homoepitaxial or heteroepitaxy approachs. Homoepitaxial can be advantageous over heteroepitaxy due to its process of growing GaN on native substrates (growing GaN wafers on bulk GaN substrates). This would reduce the need for buffer layers and eliminates the lattice miss match between the materials, moreover the cost of growing GaN wafers on GaN substrate is expensive due to the high cost of GaN material. However, homoepitaxial process approach is in the very early stages of the production and exhibit many challenge issues in the growth of bulk single crystal GaN substrate[4]. Heteroepitaxial is a more suitable approach in processing GaN on a non-native substrates. Some of the non-native substrates used in heteroepitaxial approaches are GaN on sapphire, GaN on Si and GaN on SiC [5]. GaN on diamond and GaN on GaN are in the very early stages of production and involves many challenging issues in terms of fabrication. Figure 5.2 shows the cross sectional schematic view of GaN heteroepitaxial structure for a FET device.

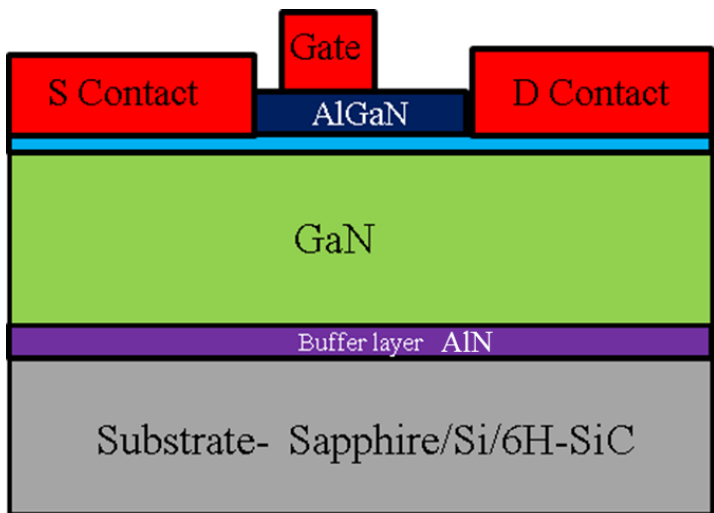


Figure 5.2: Cross sectional schematic view of GaN heteroepitaxial structure for a FET device[6].

The buffer layer is used in between the substrate and GaN to neutralise the crystal lattice mismatch. AlN is widely used as buffer layer which provides a good material match to neutralise the lattice miss match effect between GaN and the substrate[7]. Table 5.2 shows the thermal conductivity parameter for Sapphire, Silicon and 6H-SiC substrates. Each substrate

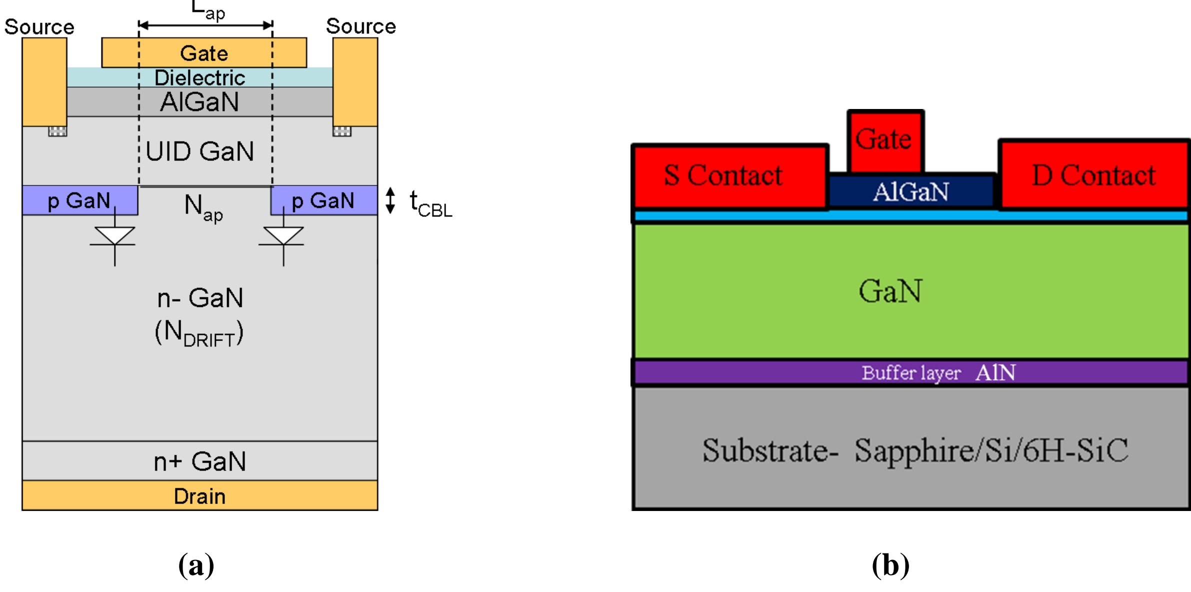
has its own advantages and disadvantages. For example, sapphire has a very low thermal conductivity and low cost when compared to Silicon and 6H-SIC substrates, but has very low crystal lattice mismatch between the GaN and Sapphire.

Table 5.2: Substrates thermal conductivity

Parameter	Thermal conductivity (W/mK)
Sapphire	45
Silicon	149
6H-SiC	490

5.1.3 Device Topology

Device topology in general can be classified into vertical and lateral devices. Figure 5.3 shows the vertical and lateral GaN device structures. In lateral devices the Gate, Drain and Source contacts are located on the top side of the device having current flow across the surface of the die. Whereas, in the vertical device topology the gate and source contacts are located on the top and drain contact on the bottom of the device providing current flow from top to bottom. The heteroepitaxial approach of GaN on Sapphire/Si/SiC substrates are limited to lateral device topology due to the buffer layer essential to neutralise the lattice miss match between the materials.



(a) **(b)**

Figure 5.3: (a) Vertical GaN device (b) Lateral GaN device[8]

Commonly used lateral device structure, regardless to applications, is HEMT (High Electron Mobility Transistor), as shown in Figure 5.2. The main applications of HEMT GaN devices are towards high frequency applications, for example wireless communications and defence systems. Another promising application being researched and pursued is with GaN on Sapphire/Si/SiC HEMTS for lower voltage switching power electronics applications, where manufacturers and industry are focusing towards developments.

5.1.4 GaN Packaging options and mounting techniques

Power semiconductor devices require a package which meets robust, flexible heat sink mount and wire bonds/lead frame size to meet the thermal management and current carrying capability. Discreet GaN packaging options are through hole such as TO-220/247/257 and surface mount packages, such as QFN. GaN power devices can be either face up and flip chip mounted on to the conventional TO-220/247/257 packages, for this work, conventional TO-220 package was chosen for thermal and parasitic element analysis of GaN on Sapphire/Si/SiC substrates. Face up mounting structure used for Ansys thermal simulation and Ansys Q3D in estimating parasitic elements along with the results is discussed in Section 5.3. Section 5.4 details the flip chip mounting structure along with the thermal and parasitic elements; whereas, comparison of the two mounting system results is discussed in Section 5.5.

5.2 Electrical Package Parasitic

Parasitic is a circuit element possessed by any electrical component which is not required for its intended purpose. For example, resistor is designed to have resistance, but it will also retain unwanted capacitance and inductance. All current carrying conductors possess parasitic resistance, inductance, capacitance and these parasitic elements are unavoidable. These parasitic components can be minimised but cannot be completely removed from the electronic package. The parasitic elements of a package is typically represented in terms of Resistance (R), Inductance (L) and Capacitance (C).

Resistance is mainly due to the voltage drop in the package. At DC resistance the current is distributed equally along the entire cross section of the conductor whereas, at AC resistance the current is mainly concentrated on the surface of the conductor due to the skin effect. AC resistance increases with respect to frequency, because at high frequency the skin depth decreases which in turn decreases current flow along the cross sectional area. Resistance is directly proportional to the length of the conductor and its cross sectional area.

Inductance in a closed loop system is represented by Equations (5.1) or (5.2)[9]

$$L = \frac{\lambda}{i} \qquad (5.1)$$

$$V = L\frac{d_i}{d_t} \qquad (5.2)$$

Where, λ, i and V are flux linkage, current flow and change in induced voltage. In a package the signals propagate through drain or gate leads and returns through source or ground leads. The parasitic inductance can be calculated for open circuit path or just a part of the closed loop single lead. This concept could be used to calculate the inductance contributions of various elements in the package and can be separated into various inductance elements. Figure 5.4 shows the self and mutual inductance of a single loop. Mutual inductance 'M' in two leads is defined as the magnitude of the secondary voltage induced by the changes in the primary current. Self-inductance is created in a lead having a change in magnetic flux, which in turn induces an opposing voltage within the same lead.

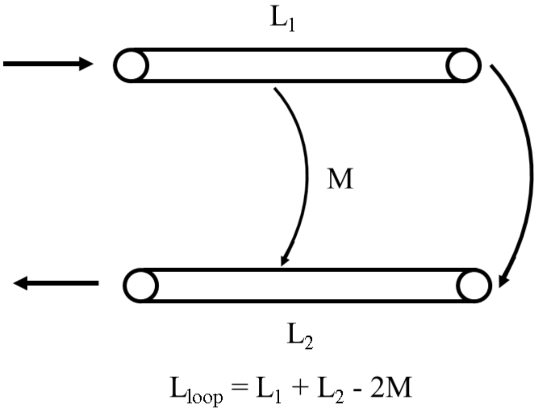


Figure 5.4: Self and mutual inductance of a single loop

DC inductance is calculated based on the assumption that the current flows through the entire cross sectional area of the conductor. Whereas, AC inductance is calculated based on the assumption that the current flows only on the surface of the conductors as the skin depth is small compared to the cross sectional area of the conductor.

Self-capacitance is due to the capacitance of any element in the package to ground. Mutual capacitance is the capacitance between any two elements for example, the capacitance from drain lead to source lead.

5.2.1 Equivalent circuit model of package lead

Figure 5.5 represents the T-equivalent[9] circuit model with package parasitic elements for TO- standard package. Each Gate/Drain/Source lead has a 'source' and a 'sink' signifying its two ends. The resistance and inductance is divided into two parts and placed in between the self-capacitance.

Mutual inductance exists between gate to source, drain to source and gate to drain. The mutual parasitic elements has to be as low as possible for a perfect system, and is usually represented in terms of coupling co-efficient. The coupling coefficient 'k' for inductance is represented using equations 5.3.

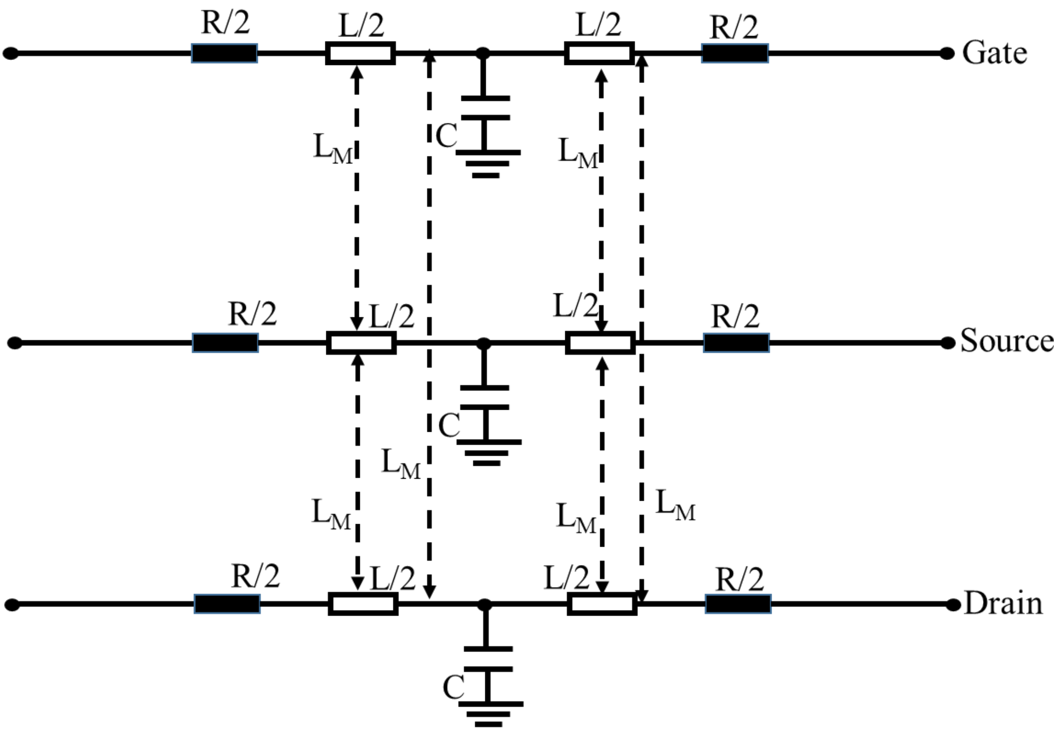


Figure 5.5: T-equivalent circuit

$$K_L = \frac{L_M}{\sqrt{L_1 L_2}} \qquad (5.3)$$

The coupling coefficient 'k' is expressed between 0 and 1 value, where 0 represents zero or no inductive coupling and 1 represents maximum coupling. For example, if k=1 the two leads are perfectly coupled, if k > 0.5 the two leads are closely coupled and if k < 0.5 the two leads are lightly coupled.

5.3 Face up mounting

5.3.1 Structure definition

Thermal performance of GaN on Sapphire, Si and 6H-SiC substrates for a face up mounting system were analysed using ANSYS® thermal tool under steady state and transient conditions. Figure 5.6 shows the schematic 3D view of GaN face up structure. The current rating of the device was 2.5A with a breakdown voltage of 1200V. Figure 5.7 shows the detailed cross-section schematic view along the channel region of GaN face up structure.

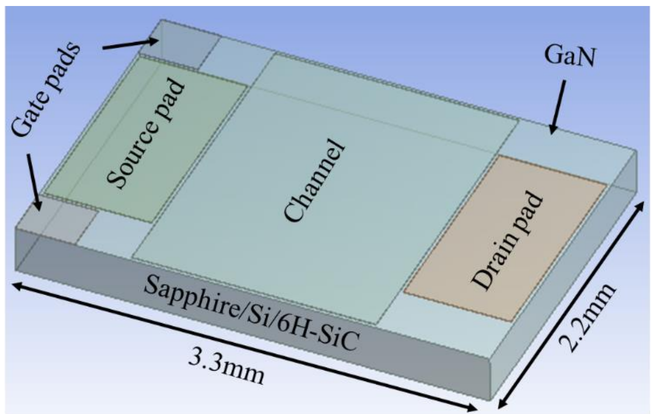


Figure 5.6: Schematic 3D view of GaN face up structure

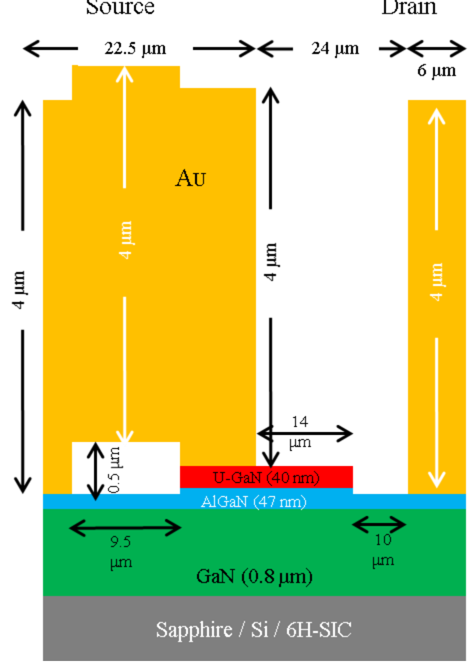


Figure 5.7: Detailed cross-section schematic view along the channel region of GaN face up structure.

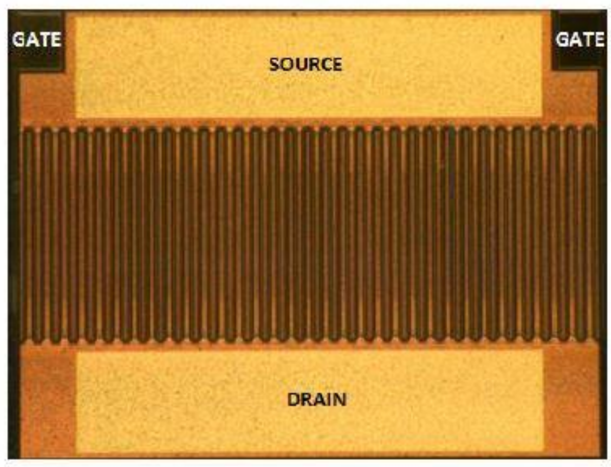


Figure 5.8: Fabricated GaN on SiC serpentine Gate PSJ HFET[10]

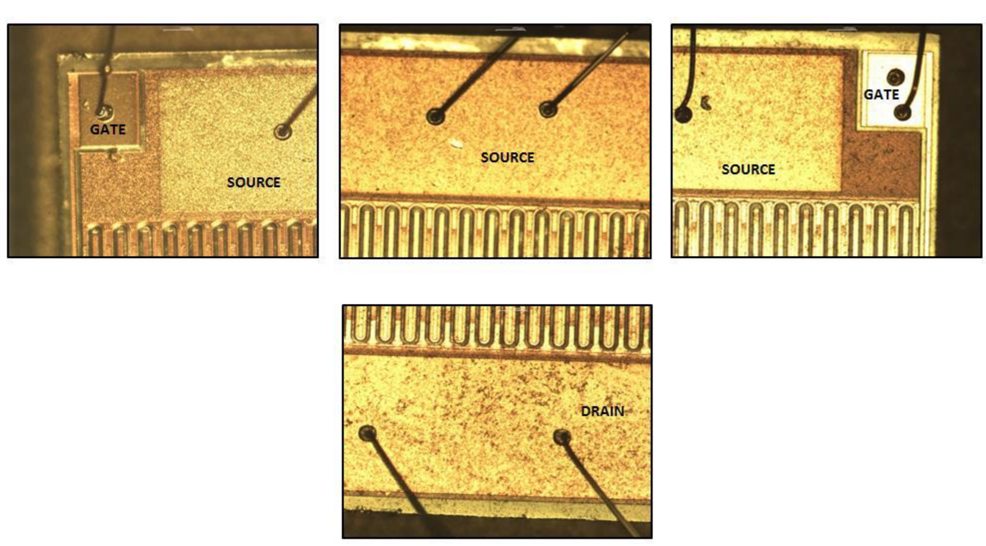


Figure 5.9: Wire-bonded PSJ HFET[10]

Figure 5.8 & 5.9 shows the fabricated GaN on SiC serpentine Gate PSJ (Polarisation Superjunction) HFET (Heterojuction field-effect transistor) and wire-bonded image fabricated and presented in previous study [10]. The detailed serpentine and multi finger design structures and electrical performances can be found in [10]. Serpentine design structure was considered for face up mounting (wire-bonded) and multi finger design arrangement for flip chip mounting systems. The design structure for multi finger arrangement on flip chip mounting system is discussed in Section 5.4.1.

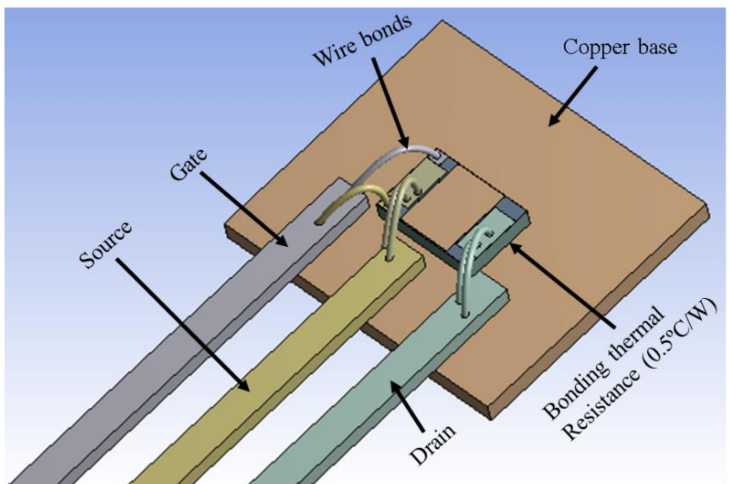


Figure 5.10: 3D schematic view of GaN face up on TO-220 package without the epoxy resin

For the thermal simulation the face up structure was soldered on to the TO-220 copper base of 500µm thick with a bonding thermal resistance of 0.5ºC/W as shown in Figure 5.10. The gate, source and drain pads are connected to the TO-220 lead frames using 100µm thick aluminium wire bonds, the fusing current for 100µm thick Au wire was observed to be 4A[11] (see Appendix 5). Two 100µm thick aluminium wires with a total current carrying capability of 8A were used between the pads and the lead frame, as a rule of thumb enabling ~2x current carrying capability of the device rated current with wire bond loop length of <10mm with a loop height of <1mm.

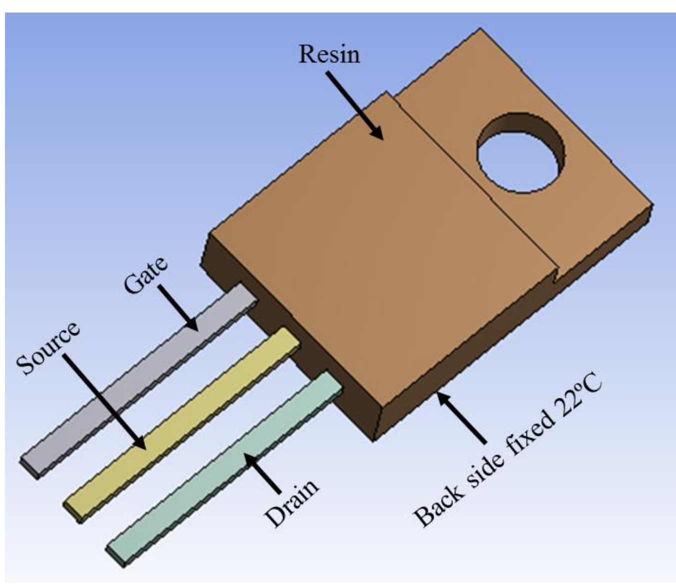


Figure 5.11: 3D view of GaN on sapphire/silicon/6H-SiC with face up mounting in a T0-220 package system

Figure 5.11 shows the 3D view of GaN on Sapphire/Silicon/6H-SiC with face up mounting in a T0-220 package system. In order to understand the thermal dependency upon substrate layer thickness, the Sapphire, Silicon and 6H-SiC substrate thicknesses as shown in Table 5.3 are used. The back side of the T0-220 package was held at a constant temperature of 22℃. Thermal loading of 5 to 20 W with a step of 5W was considered to be applied on the channel region of the GaN semiconductor device. Table 5.4[12-14] shows the thermal conductivity values for different materials used in the simulation. The model was simulated using ANSYS steady state and transient thermal analysis tool.

Table 5.3: Substrate thicknesses

Parameters	Thickness(µm)
Sapphire	150
	200
	550
Si	375
	675
	1000
6H-SiC	200
	370
	675

Table 5.4: Thermal conductivity values at 25˚C used in simulation

Material	Thermal conductivity (W/mK)
GaN	150
Au	318
Cu	400
Resin	2.4
Sapphire	45
Si	149
6H-SiC	490

5.3.2 Face up mounting results

5.3.2.1 Steady state analysis

Figure 5.12 shows the 3D thermal contour distribution for GaN on Sapphire (550µm) in a T0-220 package with a thermal loading of 20W whereas, Figure 5.13 shows the detailed view of thermal contours and hotspot region without resin body. The maximum junction temperature of the device was found to be 157ºC.

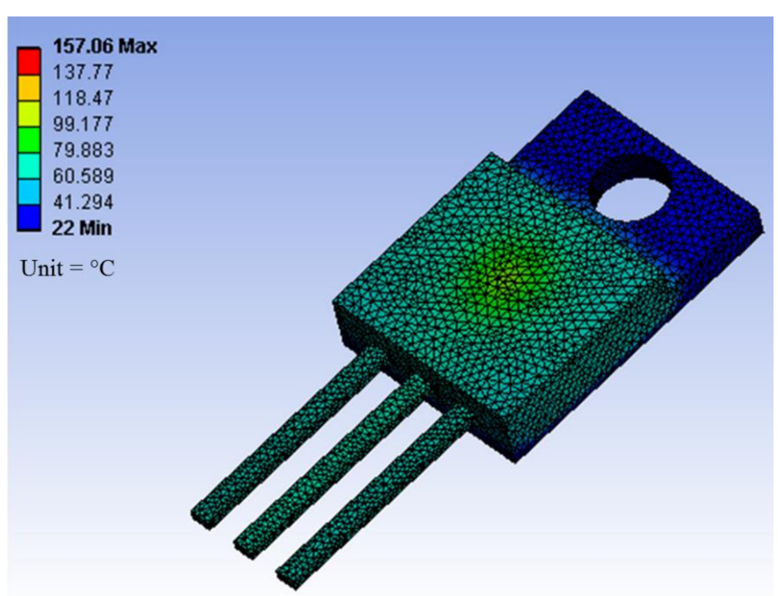


Figure 5.12: 3D thermal contours for GaN on sapphire (550µm) in a T0-220 package with a thermal loading of 20W

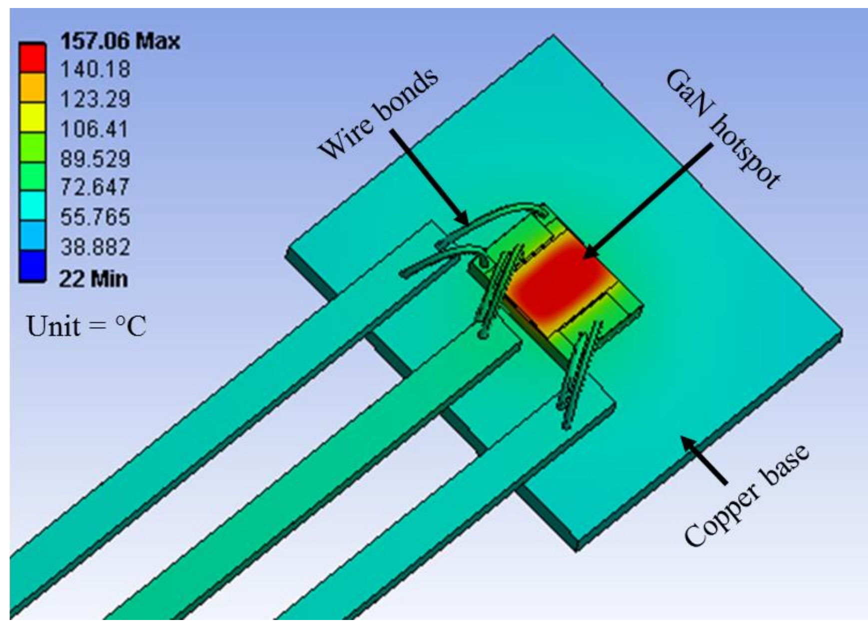


Figure 5.13: Detailed view representing hotspot region without the resin body

The cross-sectional view of GaN on Sapphire (550µm) with temperature distribution is shown in Figure 5.14. The junction to case thermal resistance ($R_{th(j-c)}$) was found to be 6.75ºC/W using (5.4)

$$R_{th(j-c)} = \frac{T_j - T_c}{P} \qquad (5.4)$$

Where,

T_j = Junction temperature (157ºC)

T_c = Case temperature (22ºC)

Power = 20W

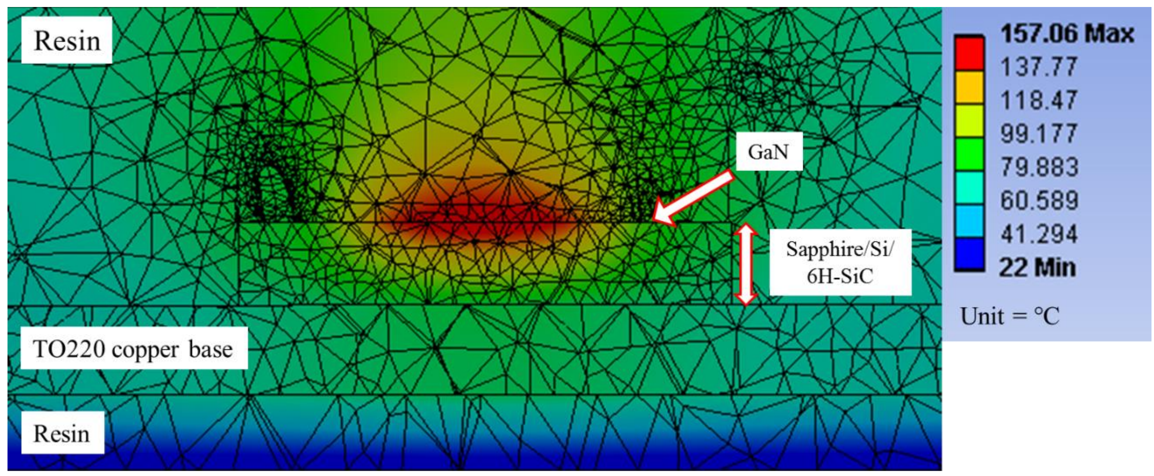


Figure 5.14: Cross-sectional view of GaN on Sapphire (550µm) with thermal contour distribution

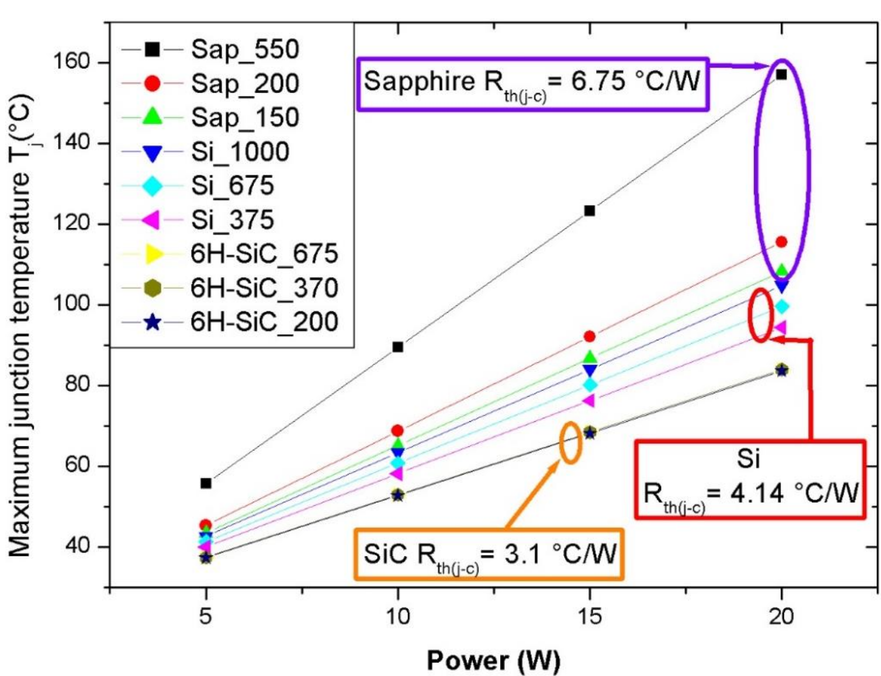


Figure 5.15: Maximum junction temperature (T_j) with respect to variation in substrate layer thicknesses for face up GaN

In order to understand the thermal dependency upon substrate layer thicknesses, the Sapphire, Silicon and 6H-SiC thicknesses as shown in Table 5.4 were analysed. Thermal loading conditions were varied from 5 to 20W with a step of 5W. The maximum junction temperature (T_j) with respect to variation in sapphire, silicon and 6H-SiC substrate layer thicknesses for face up GaN is shown in Figure 5.15.

In face up mounting system the junction temperature increses with increase in substrate layer thicknesses. The thermal resistance junction to case ($R_{th(j-c)}$) for GaN on sapphire (550µm) was observed to be 6.75ºC/W whereas, thermal resistance decreases to 4.14ºC/W and 3.1ºC/W for GaN on Si(1000µm) and GaN on 6H-SiC(675µm) due to the better thermal conductivity and heatflow in Si and 6H-SiC compared to sapphire substrates. Table 5.5 shows the temperature difference and thermal resistance junction to case at 20W power level for GaN devices mounted on to sapphire/Si/6H-SiC substrates in a T0-220 package.

Table 5.5: Thermal resistance junction to case at 20W power level for GaN devices mounted on a T0-220 package.

Substrate	$\Delta T_{(j-c)}$ (ºC)	$R_{th(j-c)}$ (ºC/W)
Sapphire 550µm	135.06	6.75
Sapphire 200µm	93.57	4.67
Sapphire 150µm	86.37	4.31
Si 1000µm	82.82	4.14
Si 675µm	77.67	3.88
Si 375µm	72.44	3.62
6H-SiC 675µm	62.03	3.10
6H-SiC 370µm	62.01	3.10
6H-SiC 200µm	61.64	3.08

5.3.2.2 Transient analysis

Many GaN devices operate in high frequency operation, it is vital to understand the pulsed transient response of GaN devices. An effective graph representing thermal impedance and pulse width is important[15]. ANSYS® transient thermal analysis tool was used to predict thermal impedance at different pulse width under 50% duty cycle condition. Table 5.6 show the density and specific heat capacity values used in the simulation for time constant calculation[15, 16].

Table 5.6: Density and specific heat capacity values used in the simulation

Material	Density (g/cm^3)	Specific heat capacity (J/Kg ºC)
GaN	6.15	490
Au	19.3	129.1
Cu	8.92	387
Resin	1.79	1000
Sapphire	3.98	753.6
Si	2.32	710
6H-SiC	3.21	690

Transient thermal analysis was performed under 50% duty cycle condition for GaN on Sapphire, Silicon and 6H-SiC substrate thicknesses as shown in Table 5.3. Thermal impedance junction to case was plotted for different pulse width ranging from 1µs to 10s. Figure 5.16 shows the transient response for GaN on Sapphire substrates whereas, Figure 5.17 & 5.18 shows the thermal response for Si and 6H-SiC substrates.

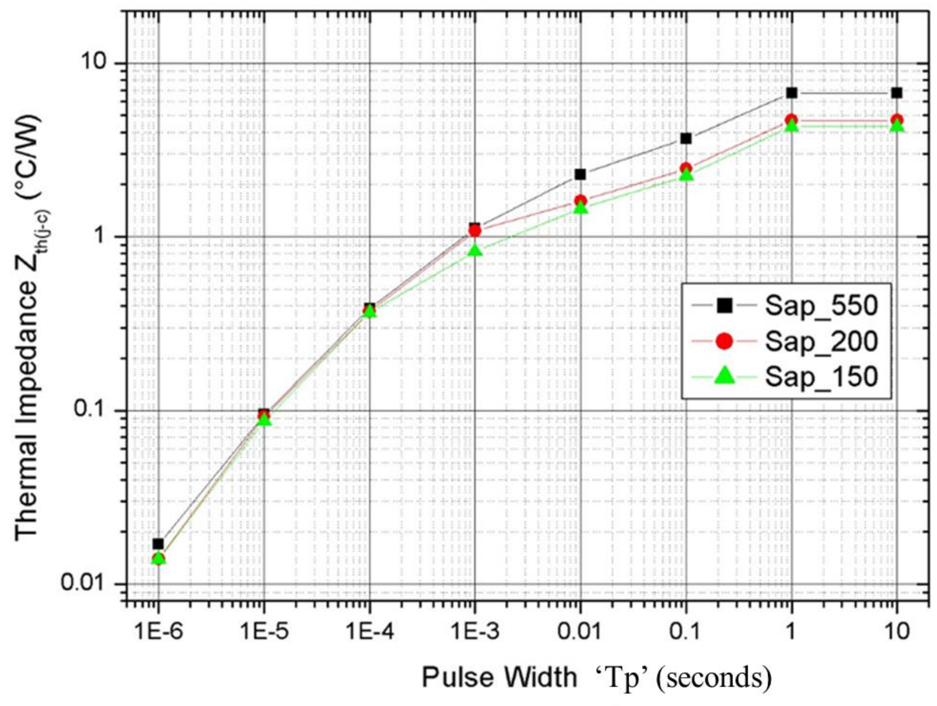


Figure 5.16: Transient response for GaN on Sapphire substrates

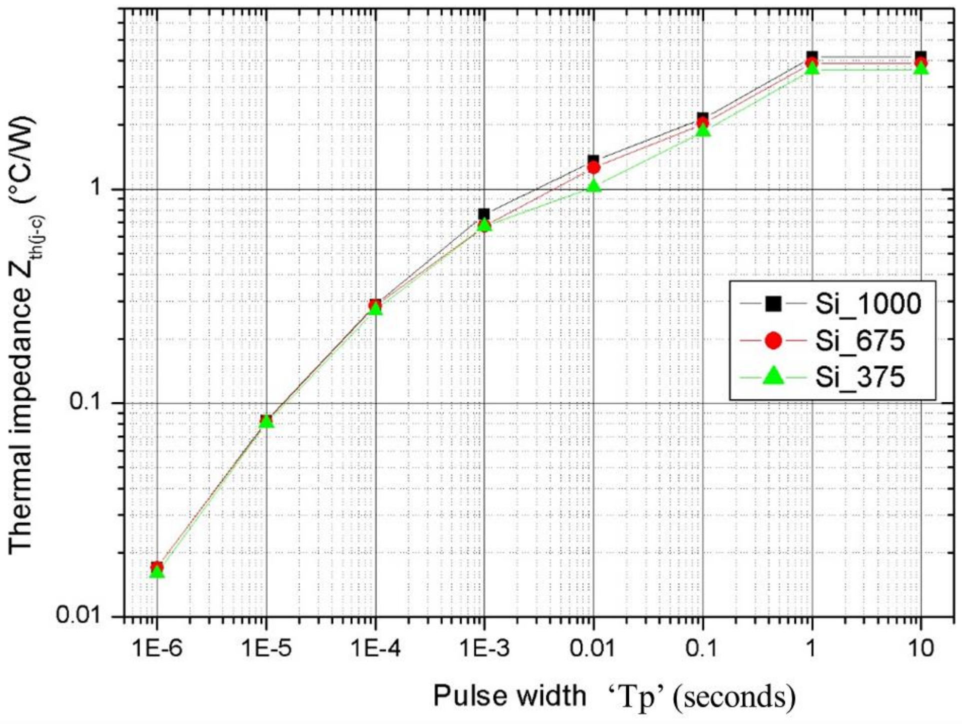


Figure 5.17: Transient response for GaN on Silicon substrates

For these measurements the 20W power pulse was applied to the thermal system and continuous pulse width ranging from 1µs to 10s was applied at 50% duty cycle condition. As shown thermal impedance reduces with pulse width as a direct result of the energy absorbed by the system.

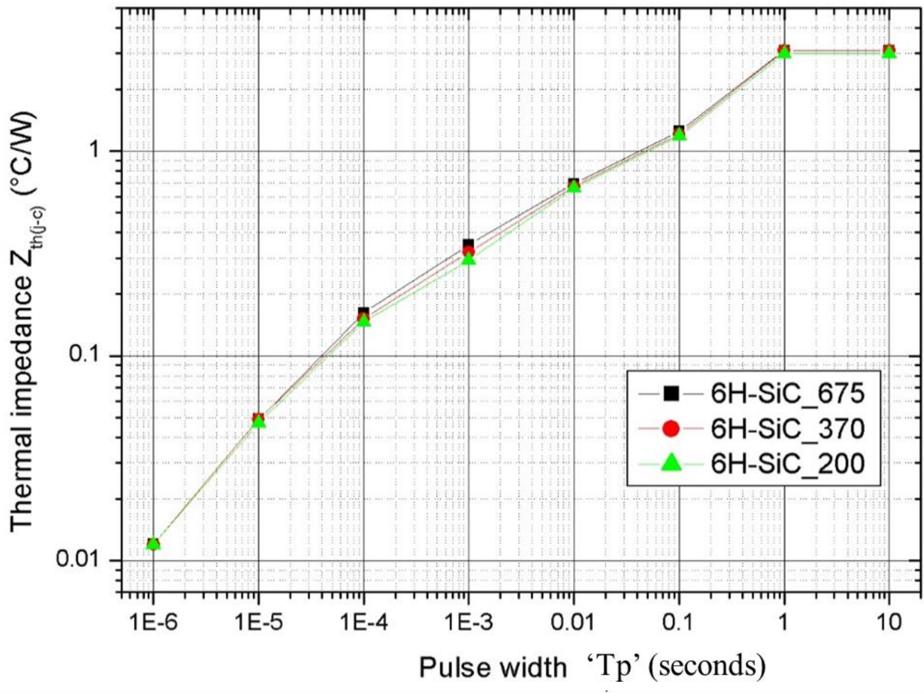


Figure 5.18: Transient response for GaN on 6H-SiC substrates

The variation in substrate layer thicknesses shows same thermal response for first 100µs, but varies after this point with respect to sapphire substrate layer thicknesses until full thermal saturation is reached. Thermal impedance rise is higher after 100µs which can be explained by slower thermal response of the system attributed by layer thicknesses, specific heat capacity and thermal conductivity of the materials. Table 5.7 shows the like to like comparison of thermal impedance junction to case for different substrates at 10µs pulse width, as thermal impedance does not vary significant with respect to layer thicknesses variation at 10µs pulse width.

Table 5.7: Thermal impedance junction to case for different substrates at 10 micro-second pulse width

Parameter	$Z_{th(j\text{-}c)}$ @ 10µs pulse width
GaN on Sapphire	0.1
GaN on Si	0.08
GaN on 6H-SiC	0.05

Thermal impedance junction to case ($Z_{th(j\text{-}c)}$) is higher for GaN on sapphire because of its high specific heat capacity and thermal conductivity property when compared over Si and 6H-SiC substrates.

5.3.2.3 Package Parasitic elements

The parasitic elements for face up mounted for GaN on Sapphire/Si/6H-SiC in a T0-220 package is analysed using ANSYS Q3D extractor. The ANSYS Q3D Extractor uses electromagnetic field simulation to extract parasitic resistance, inductance and capacitance. Two 100µm wire bonds were used to interconnect the gate, source and drain pads with the leads of the package. 500 kHz frequency was used to analyse the parasitic elements under AC condition, Figure 5.19 shows the 'source' and 'sink' points used in simulation for analysing the parasitic elements.

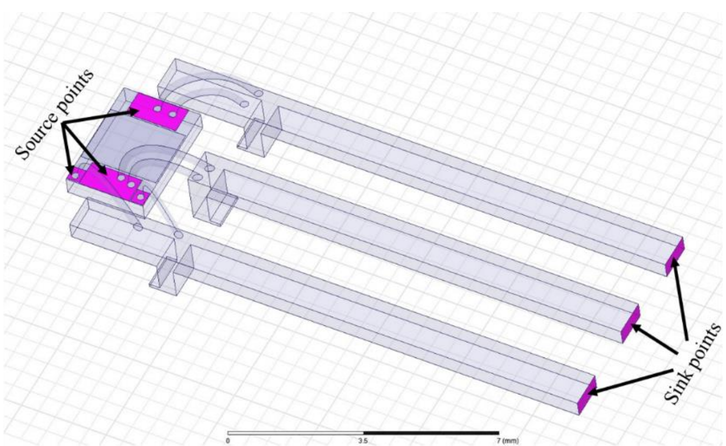


Figure 5.19: 'Source' and 'sink' points used in Q3D for analysing the parasitic elements.

Table 5.8: Self-resistance, inductance and capacitance

Parameter	Gate	Source	Drain
Resistance (mΩ)	3.23	2.88	2.65
Inductance (nH)	9.28	9.14	9.37
Capacitance (pF)	0.64	0.97	0.70

Table 5.9: Mutual inductance and resistance

Parameter	Gate - Source	Gate – Drain	Drain - Source
Inductance (nH)	4.04	2.61	4

Table 5.10: Coupling Co-efficient 'k' between the leads

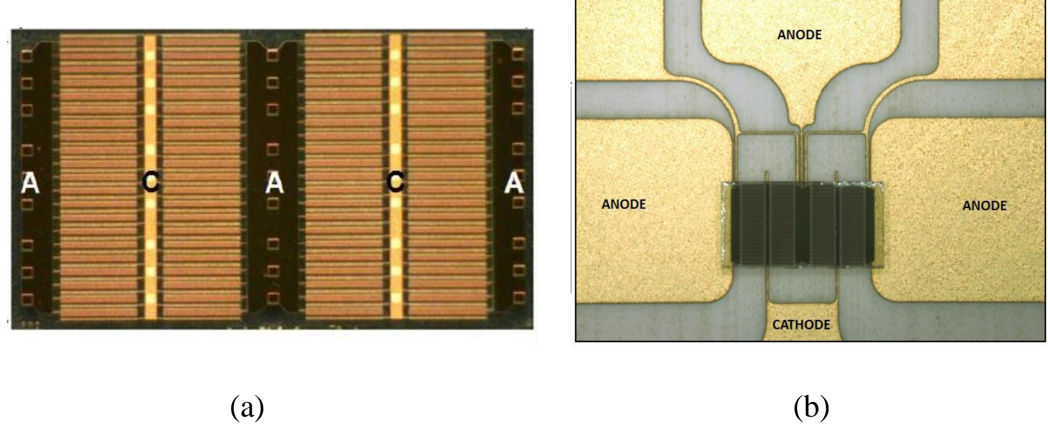
Parameter	Coupling Co-efficient 'k'	
	Resistance	Inductance
Gate -Gate	1	1
Gate - Source	0.20	0.43
Gate – Drain	0.13	0.27
Source-Source	1	1
Drain - Source	0.24	0.43
Drain-Drain	1	1

Table 5.8 shows the AC R-L-C parasitic element analysed under 500kHz frequency, whereas Table 5.9 shows the parasitic mutual inductance and Table 5.10 shows coupling coefficient 'k' between the gate, source and drain leads. The coupling co-efficient between gate –gate, source-source and drain-drain is '1' signifying perfectly coupled condition which is the perfect case condition as detailed in Section 5.2.1

5.4 Flip chip mounting

5.4.1 Structure definition

Thermal performance of GaN on Sapphire, Si and 6H-SiC substrates for flip chip mounting system were analysed using ANSYS® thermal tool under steady state and transient conditions.



(a) (b)

Figure 5.20: (a) Fabricated PN diode of GaN on SiC with multi finger design structure; (b) Image after flip chip process[10]

Figure 5.20 shows the fabricated PN diode of GaN on SiC with multi finger design arrangement whereas, Figure 5.21 shows an X-ray image of flip chipped device. As mention in Section 5.3.1 serpentine and multi finger design structures and electrical performances were completed as a part of previous study and described in [10]. Serpentine design structure was considered for face up mounting (wire-bonded) and multi finger design arrangement for flip chip mounting systems.

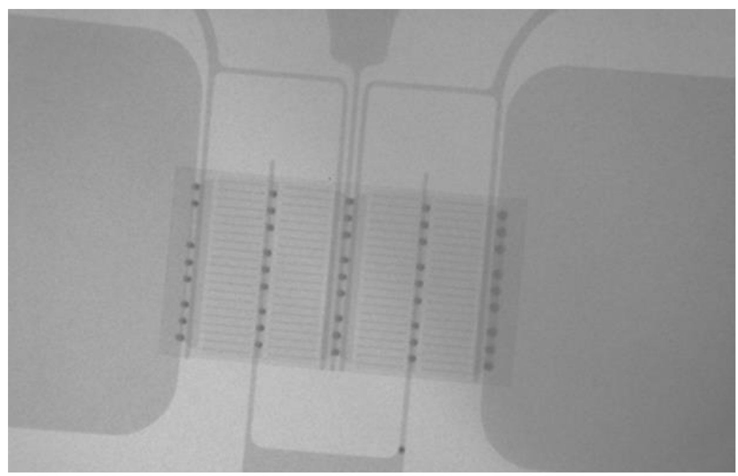


Figure 5.21: X-ray image of flip chipped device

For thermal simulation GaN HFET transistors with multi finger design arrangement was considered, Figure 5.22 shows the schematic 3D view of GaN flip chip structure. The current rating of the device was 2.5A with a break down voltage of 1200V similar to GaN device on face up mounted system discussed in Section 5.3.1.

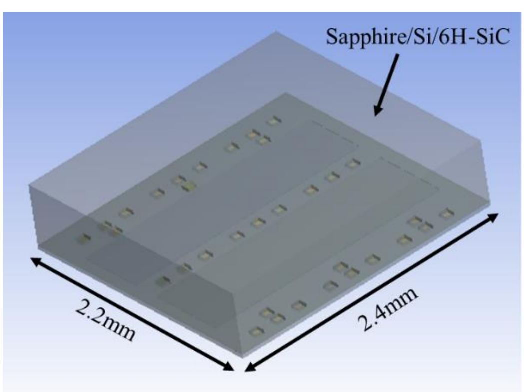


Figure 5.22: Schematic 3D view of GaN flip chip structure

Figure 5.23 shows the cross-section schematic view of flip chip interconnection along with gold stud bump and other interconnection layers. The structure replaces the conventional flip chip solder bump with gold stud bump interconnection technology. Gold stud bump flip chip interconnection offers wide advantages than the conventional solder bump interconnection in terms of better thermal conductivity and mechanical reliability; with low co efficient of thermal expansion[17]. The only disadvantage of using gold stud bumps inter-connection is it uses thermocompression bonding which requires high processing temperature and pressure. Thermocompression bonding requires coupling layers[18] and additional metal layers to achieve a perfect flip chip interconnection layer. The Au layer thicknesses of 4µm and 1µm are used as a mating layers for the gold stud bump whereas; Ni, Cu and Ag are used as metal layers to enhance the bonding strength at reduced functional pressure and bonding temperature.

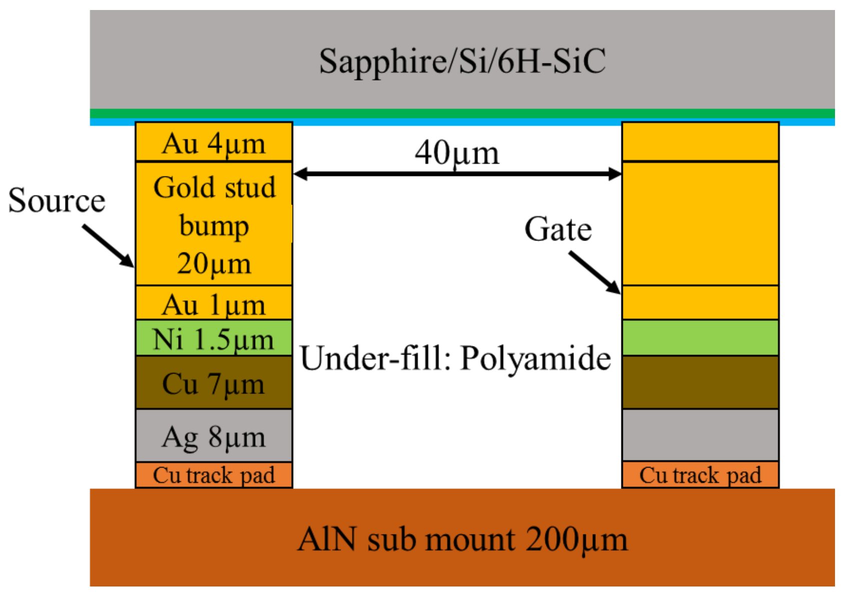


Figure 5.23: Schematic cross-section of flip chip interconnection

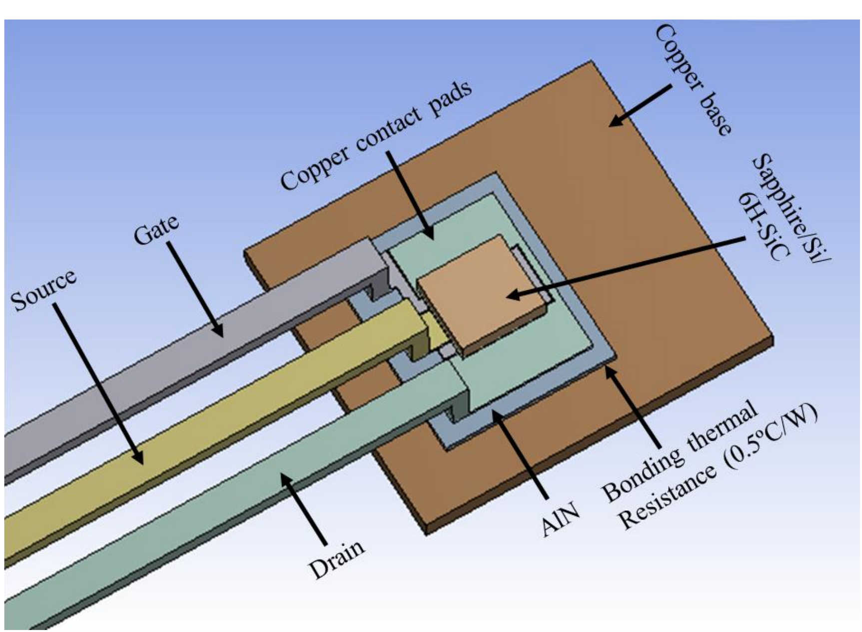


Figure 5.24: 3D schematic view of GaN flip chip on TO-220 package without the epoxy resin

The AlN sub mount was soldered on to the TO-220 copper base with a bonding thermal resistance of 0.5ºC/W as shown in Figure 5.24. The gate, source and drain pads are connected to the TO-220 lead frames via gold stud bump interconnection layers as shown in Figure 5.23 and 100µm thick copper track pads. Polyamide under fill is used to fill the gap between GaN device and the AlN sub mount, which acts as an electrical-insulator and provides mechanical strength. The polyamide under fill neutralises the CTE miss match between the GaN device

and the sub mount, avoiding stress deliberation in the stud bump interconnection region which would cause early failure.

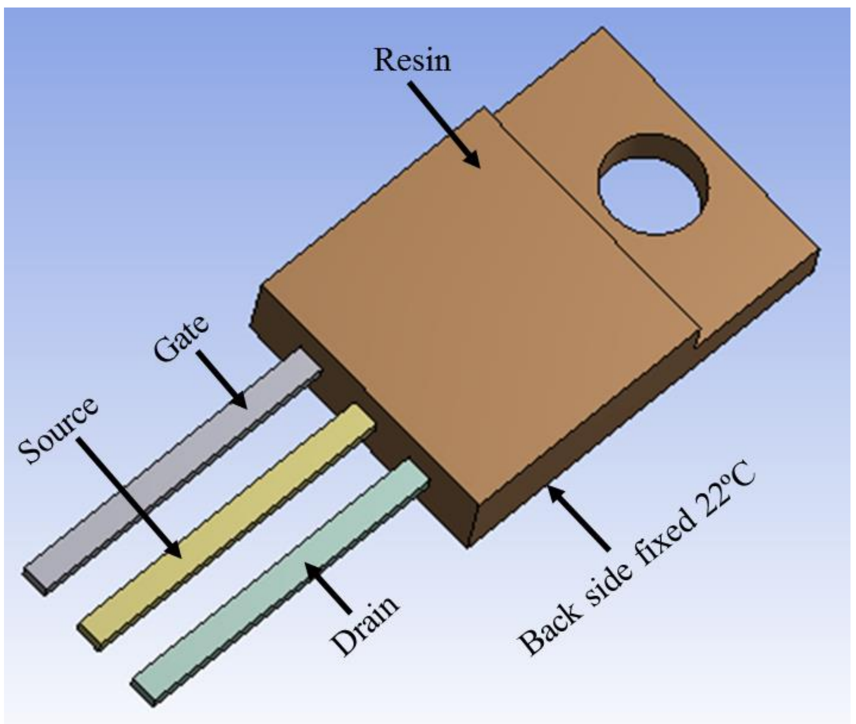


Figure 5.25: 3D view of GaN on sapphire/silicon/6H-SiC with flip chip mounting in a T0-220 package system

Figure 5.25 shows the 3D view of GaN on Sapphire/Silicon/6H-SiC with flip chip mounting in a T0-220 package system. In order to understand the thermal dependency upon substrate layer thickness, the Sapphire, Silicon and 6H-SiC substrates thicknesses as shown in Table 5.4 were used. The back side of the T0-220 package was held at a constant temperature of 22ºC. Thermal loading of 5 to 20 W with a step of 5W was considered to be applied to the channel region of the GaN semiconductor device. Table 5.11[12-14] below shows the thermal conductivity values for different materials used in the simulation. The model was simulated using ANSYS® steady state and transient thermal analysis tool.

Table 5.11: Thermal conductivity values at 25°C used in simulation

Material	Thermal conductivity (W/mK)
GaN	150
Au	318
Cu	400
Ag	429
Ni	90.9
Polyamide	0.24
Resin	2.4
Sapphire	45
Si	149
6H-SiC	490

5.4.2 Flip chip mounting results

5.4.2.1 Steady state analysis

Figure 5.26 shows the 3D thermal contours for GaN on sapphire (550µm) in a T0-220 package with a thermal loading of 20W whereas, Figure 5.27 shows the detailed view of thermal contours and hotspot region without resin body. The maximum junction temperature of the device were found to be 80.53ºC

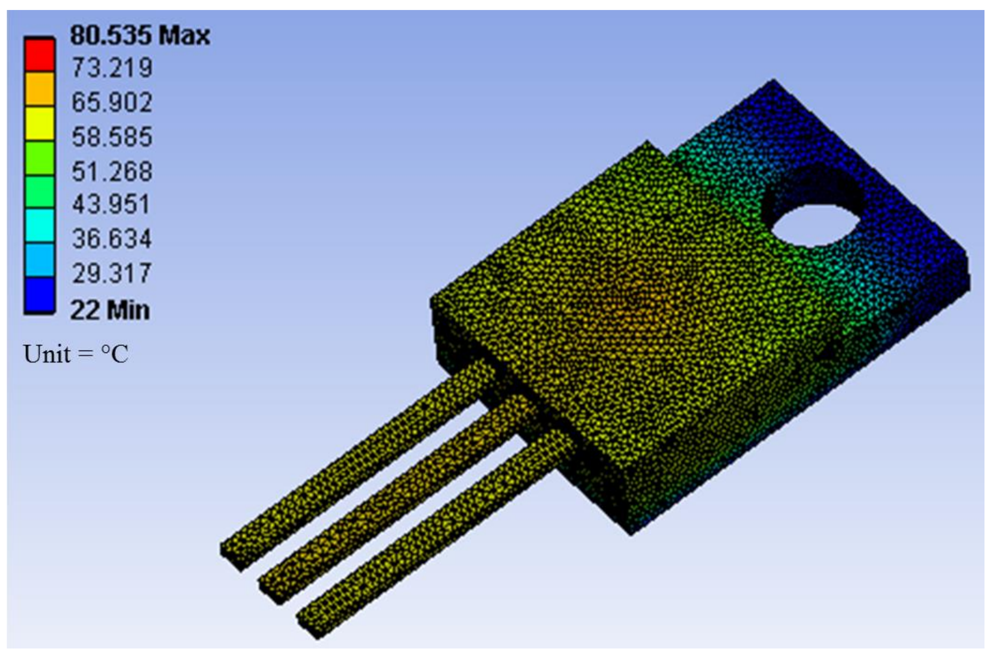


Figure 5.26: 3D thermal contours for GaN on sapphire (550µm) in a T0-220 package with a thermal loading of 20W

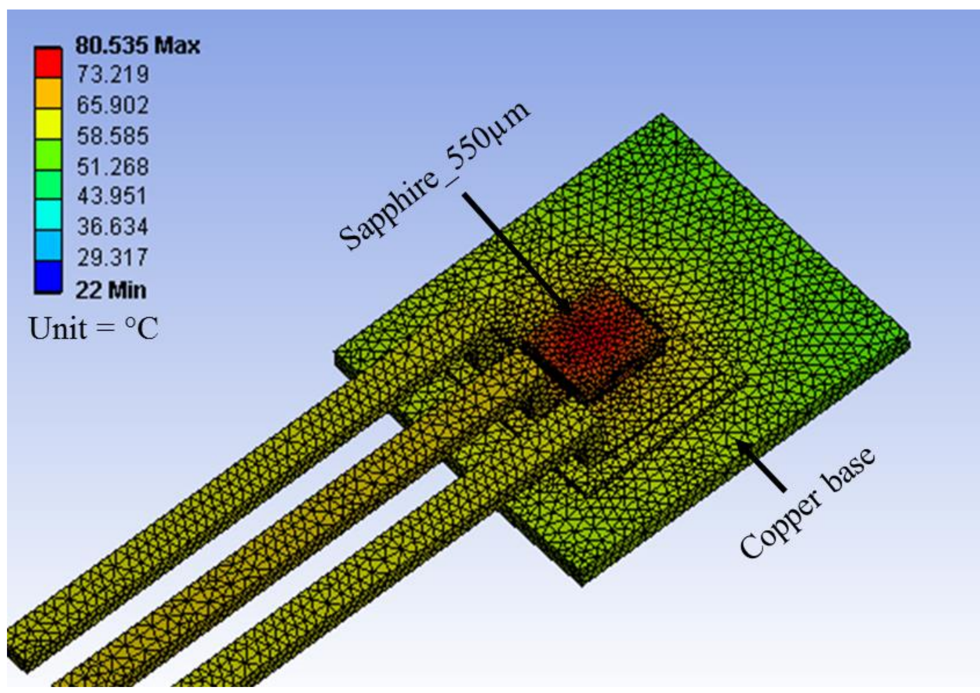


Figure 5.27: Detailed view representing hotspot region without the resin body

The cross-sectional view of GaN on Sapphire (550µm) with temperature distribution is shown in Figure 5.28. The junction to case thermal resistance ($R_{th(j-c)}$) was found to be 2.92ºC/W using equation (5.4) Where, T_j = 80.53ºC; T_c = 22ºC; P = 20W. Thermal loading conditions were varied from 5 to 20W with a step of 5W. The maximum junction temperature (T_j) with respect to variation in sapphire, silicon and 6H-SiC substrate layer thicknesses for face up GaN is shown in Figure 5.29.

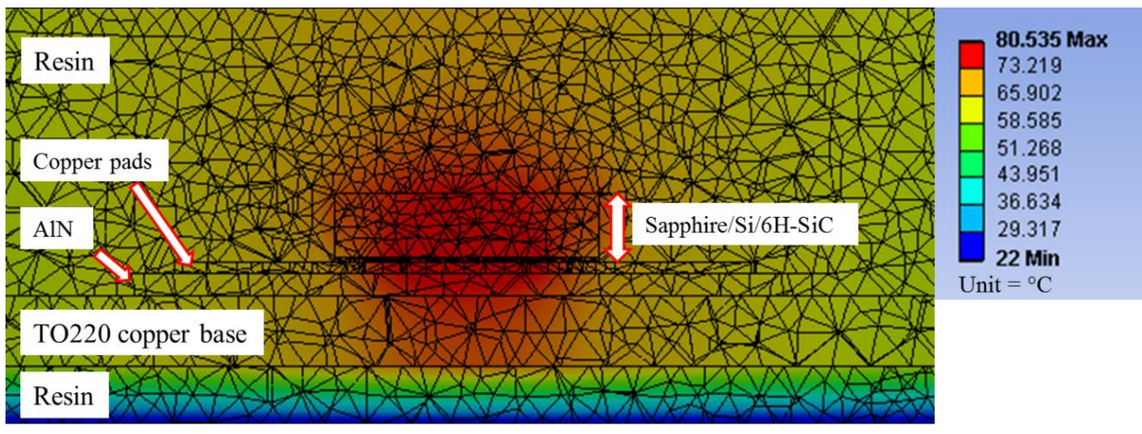


Figure 5.28: Cross-sectional view of GaN on Sapphire (550µm) with thermal contour distribution

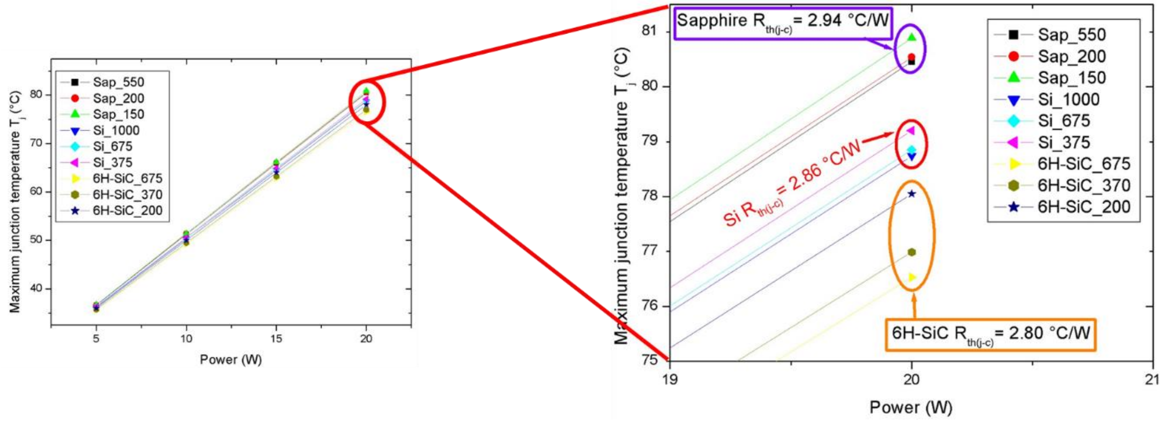


Figure 5.29: Maximum junction temperature (T_j) with respect to variation in substrate layer thicknesses for flip chip GaN

The thermal resistance junction to case ($R_{th(j-c)}$) for GaN on sapphire (150µm) was predicted to be 2.94ºC/W whereas, thermal resistance decreases to 2.86ºC/W and 2.80ºC/W for GaN on Si(375µm) and GaN on 6H-SiC(200µm) due to the better thermal conductivity of Si and 6H-SiC compared to Sapphire substrates. Table 5.12 shows the temperature difference and thermal resistance junction to case at 20W power level for GaN devices mounted on to different

substrates in a T0-220 package. In flip chip mounting system the junction temperature increses with decrease in substrate layer thicknesses and more over, the junction temperature variation is smaller with respect to substrate layer thicknesses.

Table 5.12: Thermal resistance junction to case at 20W power level for GaN devices mounted on a T0-220 package.

Substrate	$\Delta T_{(j-c)}$ (ºC)	$R_{th(j-c)}$ (ºC/W)
Sapphire 550µm	58.46	2.92
Sapphire 200µm	58.54	2.92
Sapphire 150µm	58.89	2.94
Si 1000µm	56.74	2.83
Si 675µm	56.85	2.84
Si 375µm	57.2	2.86
6H-SiC 675µm	54.53	2.72
6H-SiC 370µm	54.99	2.74
6H-SiC 200µm	56.05	2.80

5.4.2.2 Transient analysis

Thermal impedance at different pulse width under 50% duty cycle condition was analysed using Ansys transient thermal. Table 5.13[15, 16] shows the density and specfic heat capacity values used in the simulation for time constant calculation.

Table 5.13: Density and specific heat capacity values used in the simulation

Material	Density (g/cm^3)	Specific heat capacity (J/Kg °C)
GaN	6.15	490
Au	19.3	129.1
Cu	8.92	387
Resin	1.79	1000
Polyamide	1.13	1700
Ag	10.5	230
Ni	8.90	445
AlN	3.26	740
Sapphire	3.98	753.6
Si	2.32	710
6H-SiC	3.21	690

Transient thermal analysis was performed under 50% duty cycle condition for GaN on sapphire thicknesses of 150, 200 & 550 µm, GaN on silicon thicknesses of 375,675 & 1000 µm and GaN on 6H-SiC thicknesses of 200, 370 & 675 µm. Figure 5.30 shows the transient response for GaN on sapphire substrates whereas, Figure 5.31 & 5.32 shows the thermal response for Si and 6H-SiC substrates. Thermal impedance junction to case was plotted for different pulse width ranging from 1µs to 10s.

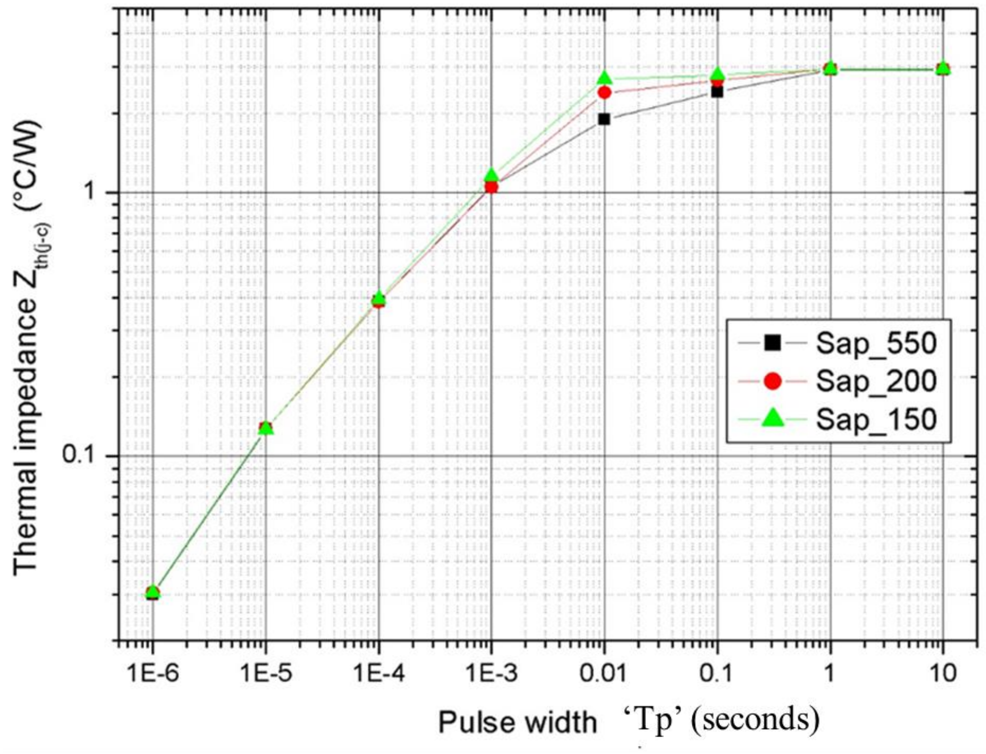


Figure 5.30: Transient response for GaN on sapphire substrates

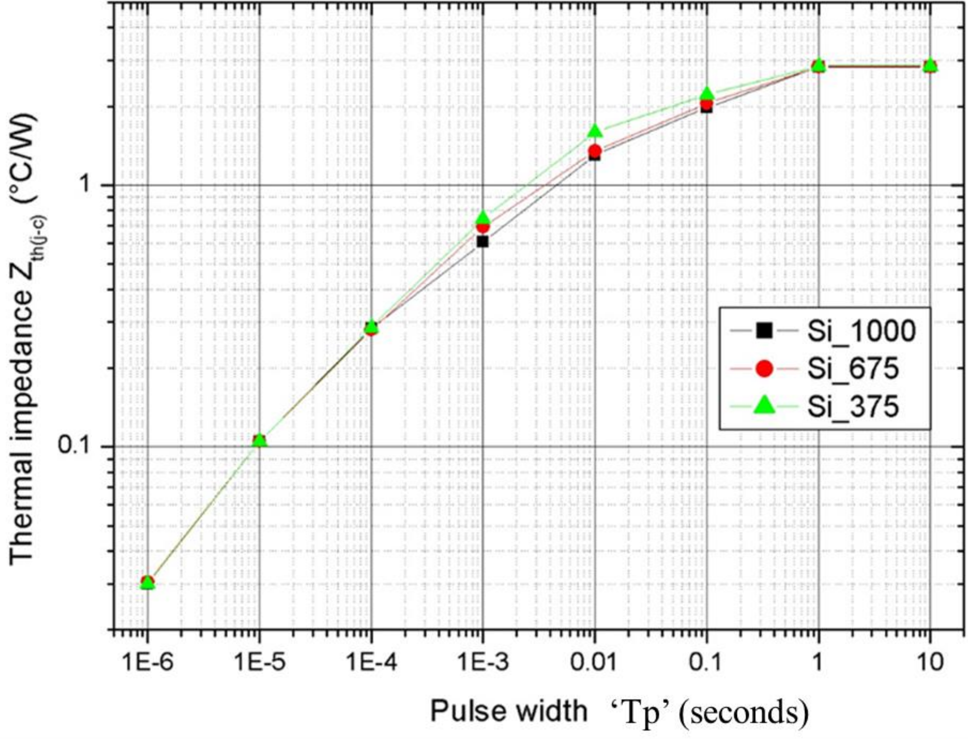


Figure 5.31: Transient response for GaN on Si substrates

For these measurements the 20W power pulse was applied to the thermal system and a continuous pulse was applied of width ranging from 1µs to 10s at 50% duty cycle. As shown thermal impedance reduces with pulse width as a direct result of the energy absorbed by the system.

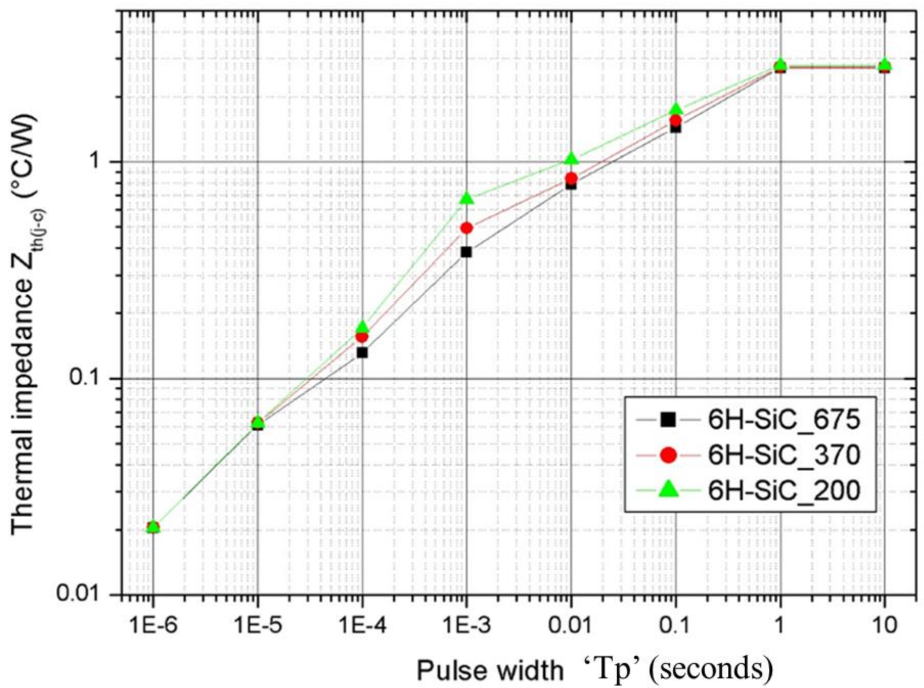


Figure 5.32: Transient response for GaN on 6H-SiC substrates

The variation in substrate layer thicknesses shows same thermal response for first 100 micro-seconds, but varies after this point with respect to sapphire substrate layer thicknesses until full thermal saturation is reached at ~1 second. Thermal impedance decreases with increase in substrate layer thicknesses due to the flip chip arrangement enabling efficient heat transfer through the flip chip interconnection and the AlN sub mount. Thermal impedance rise is higher after 100 micro-seconds which can be explained by slower thermal response of the system attributed by layer thicknesses, specific heat capacity and thermal conductivity of the materials. Table 5.14 shows the like to like comparison of thermal impedance junction to case for different substrates at 10µs pulse width, as thermal impedance does not vary significant with respect to layer thickness variations at 10µs pulse width.

Table 5.14: Thermal impedance junction to case for different substrates at 10 micro-second pulse width

Parameter	$Z_{th(j-c)}$ @ 10µs pulse width
GaN on Sapphire	0.12
GaN on Si	0.10
GaN on 6H-SiC	0.061

Thermal impedance junction to case ($Z_{th(j-c)}$) is higher for GaN on sapphire because of its high specific heat capacity and low thermal conductivity when compared over Si and 6H-SiC substrates, which in turn increases the thermal time constant and slows the thermal response of the overall system.

5.4.2.3 Package Parasitic elements

The parasitic elements for GaN flipchip mounted systems on T0-220 package with different substrates were analysed using ANSYS Q3D extractor. 500 kHz frequency was used to analyse the parasitic elements under AC condition, Figure 5.33 shows the 'source' and 'sink' points used in simulation for analysing the parasitic elements. 100µm thick copper track pad is used to connect the gate, source and drain leads with the GaN device.

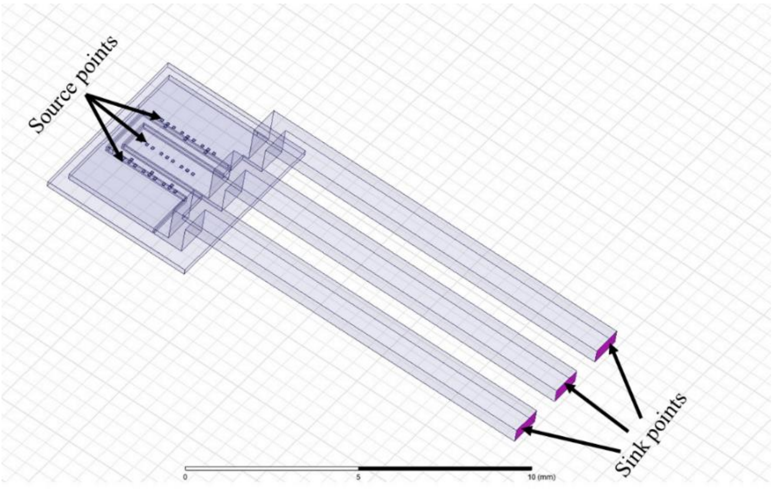


Figure 5.33: 'Source' and 'sink' points used in Q3D for analysing the parasitic elements.

Table 5.15: Self-resistance, inductance and capacitance

Parameter	Gate	Source	Drain
Resistance (mΩ)	1.9	1.7	1.88
Inductance (nH)	8.22	8.11	7.74
Capacitance (pF)	2.11	2.09	1.11

Table 5.16: Mutual resistance and inductance

Parameter	Gate - Source	Gate – Drain	Drain - Source
Inductance (nH)	2.89	4.23	4.2

Table 5.17: Coupling Co-efficient ‘k’ between the leads

Parameter	Coupling Co-efficient ‘k’	
	Resistance	Inductance
Gate -Gate	1	1
Gate - Source	0.09	0.35
Gate – Drain	0.23	0.53
Source-Source	1	1
Drain - Source	0.22	0.53
Drain-Drain	1	1

Table 5.15 shows the AC R-L-C parasitic element analysed under 500kHz frequency, whereas Table 5.16 shows the parasitic mutual inductance and Table 5.17 shows coupling coefficient ‘k’ between the gate, source and drain leads. The coupling co efficient between gate –gate, source-source and drain-drain is ‘1’ signifying perfectly coupled condition which has to be the ideal case; which gives confidence in the analysed simulation results.

5.5 Comparison between Face up and Flip chip mounted system

In this section, thermal performance and parasitic elements comparison of face up and flip chip mounted GaN on sapphire (550µm) T0-220 package is presented under steady state and transient conditions. The comparison was performed for the extreme worst case condition with greater substrate thicknesses for GaN on sapphire (550µm)/Silicon (1000µm)/6H-SiC (675µm) substrates, as the influence of substrate layer thickness in thermal resistance is significant in face up mounted system.

5.5.1 Steady state thermal resistance

Figure 5.34 shows the steady state thermal comparison of GaN on sapphire (550µm) for face up and flip chip mounted systems. Flip chip mounted GaN on sapphire shows 56% reduced thermal resistance when compared to GaN on sapphire face up mounting system.

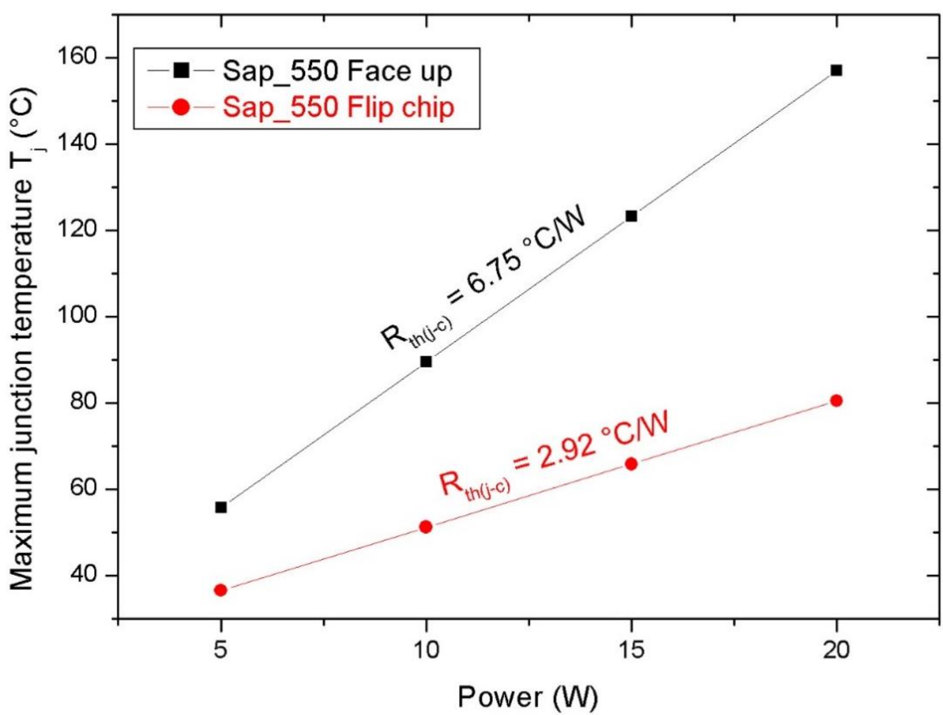


Figure 5.34: Steady state thermal comparison of GaN on sapphire (550µm) for face up and flip chip mounted systems

Flip chip mounting system has enhanced heat transfer path, allowing efficient heat conducting path from GaN device hot spot (channel region) through the gold stud bump layers and to the AlN sub mount. Moreover, the thicknesses of the substrate layer doesn’t influence the thermal performance directly in flip chip mounting system which enables use of thicker substrates in ease for mechanical handling. Table 5.18 shows the like to like comparison of flip chip and

face up mounted system for GaN on Sapphire/Si/6H-SiC substrates with respect to thickness variations at 20W power level.

Table 5.18: Comparison of flip chip and face up mounted system for GaN on Sapphire/Si/6H-SiC substrates

GaN on Sapphire @Power =20W			
Parameter	**Face up $R_{th(j-c)}$ (°C/W)**	**Flip chip $R_{th(j-c)}$ (°C/W)**	**$R_{th(j-c)}$ Reduction**
Sapphire 550µm	6.75	2.92	56%
Sapphire 200µm	4.67	2.92	37%
Sapphire 150µm	4.31	2.94	31%
GaN on Si @Power = 20W			
Parameter	**Face up $R_{th(j-c)}$ (°C/W)**	**Flip chip $R_{th(j-c)}$ (°C/W)**	**$R_{th(j-c)}$ Reduction**
Si 1000µm	4.14	2.83	31%
Si 675µm	3.88	2.84	26%
Si 375µm	3.62	2.86	20%
GaN on 6H-SiC @Power = 20W			
Parameter	**Face up $R_{th(j-c)}$ (°C/W)**	**Flip chip $R_{th(j-c)}$ (°C/W)**	**$R_{th(j-c)}$ Reduction**
6H-SiC 675µm	3.10	2.72	12%
6H-SiC 370µm	3.10	2.74	11%
6H-SiC 200µm	3.08	2.80	9%

Thermal resistance for GaN on Sapphire/Si/6H-SiC increases slightly with substrate thicknesses for face up mounting system whereas, opposite trend is observed for flip chip mounting system.

5.5.2 Transient thermal impedance

Figure 5.35 shows the transient thermal impedance comparison of GaN on sapphire (550µm) for face up and flip chip mounted systems at 50% duty cycle condition. Flip chip mounted system shows high thermal impedance for pulse width ranging from 1µs to 100µs and reduces after 100µs until thermal equilibrium is achieved. The similar trend is seen for the GaN on Si and GaN on 6HSiC substrates as shown in Figures 5.36 & 5.37 respectively.

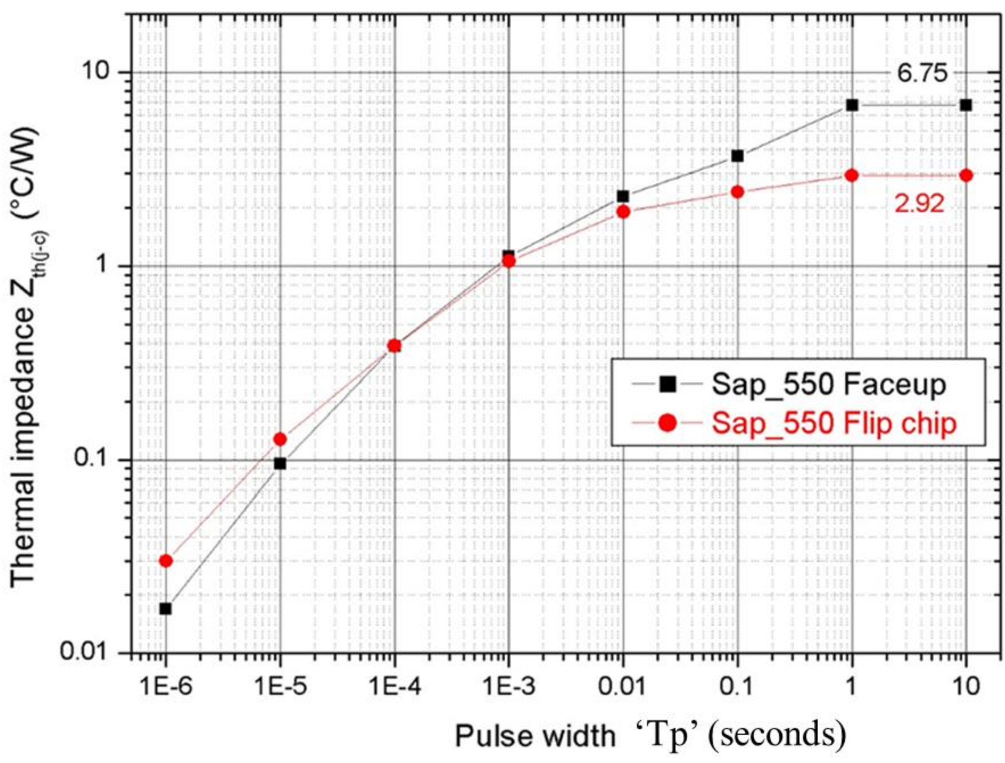


Figure 5.35: Transient thermal impedance comparison of GaN on sapphire (550µm) for face up and flip chip mounted systems at 50% duty cycle

The face up mounted system shows reduced thermal impedance at high frequencies (>50 kHz) when compared to flip chip system whereas, at low frequencies (<5 kHz) flip chip system shows reduced thermal impedance over the face up system until thermal equilibrium condition is reached.

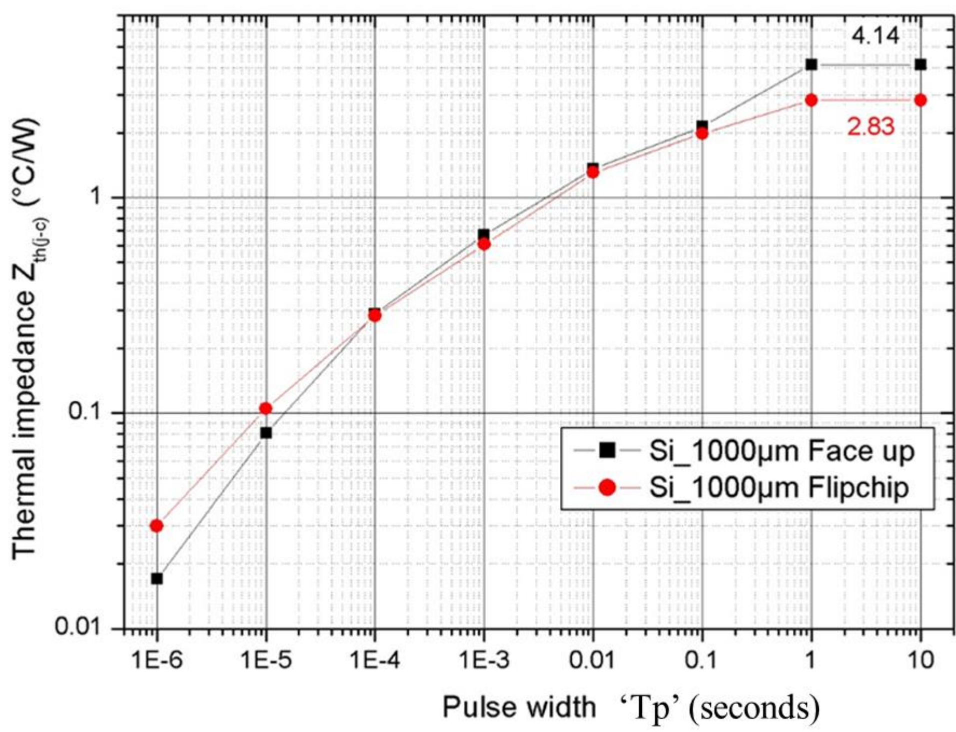


Figure 5.36: Transient thermal impedance comparison of GaN on Si (1000µm) for face up and flip chip mounted systems at 50% duty cycle

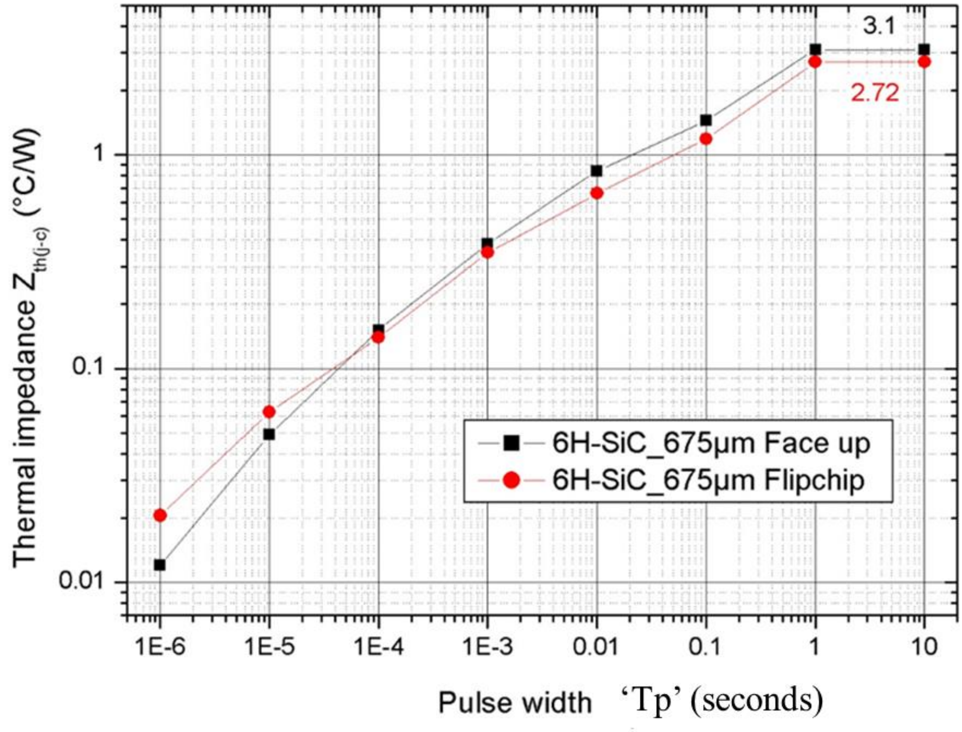


Figure 5.37: Transient thermal impedance comparison of GaN on 6H-SiC (675µm) for face up and flip chip mounted systems at 50% duty cycle

5.5.3 Parasitic elements

Figures 5.38 & 5.39 shows the self/mutual parasitic resistance and inductance comparison for face up and flip chip system observed at 500 kHz frequency condition. L_m represents the mutual inductance between the T0-220 leads. Flip chip system shows reduced parasitic resistance and inductance when compared over the face up mounted system due to the interconnection material and copper track path from the GaN contact pads to T0-220 lead lengths. Mutual parasitic inductance is observed to be high in flip chip system, as the copper track pad paths for gate/drain/source are located very close to each other enabling a high coupling effect when compared to face up system.

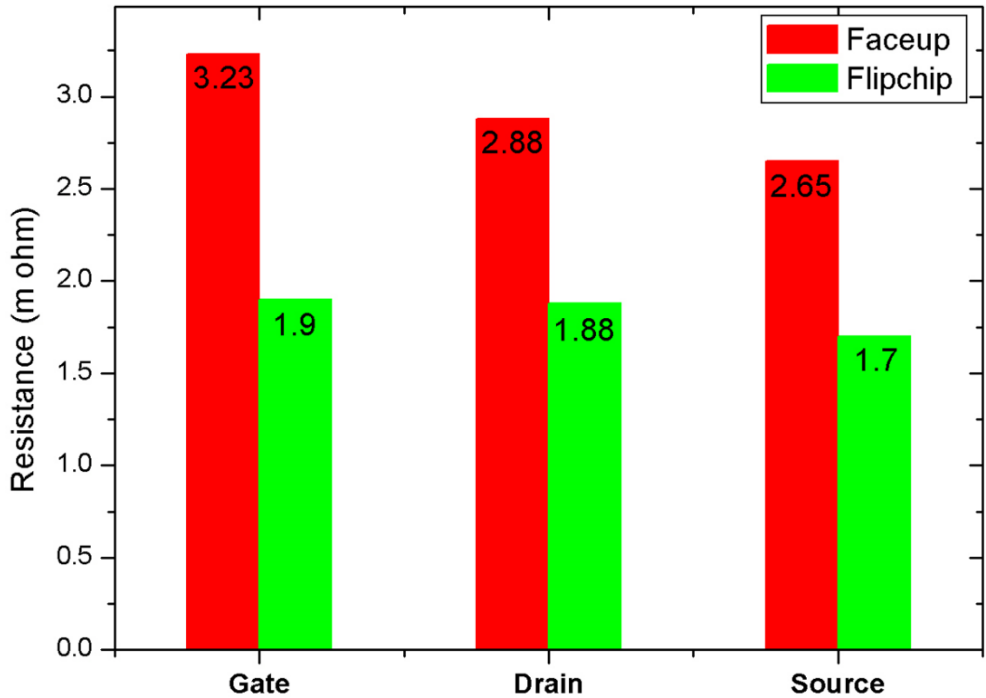


Figure 5.38: Self-resistance parasitic comparison for face up and flip chip system observed at 500 kHz frequency

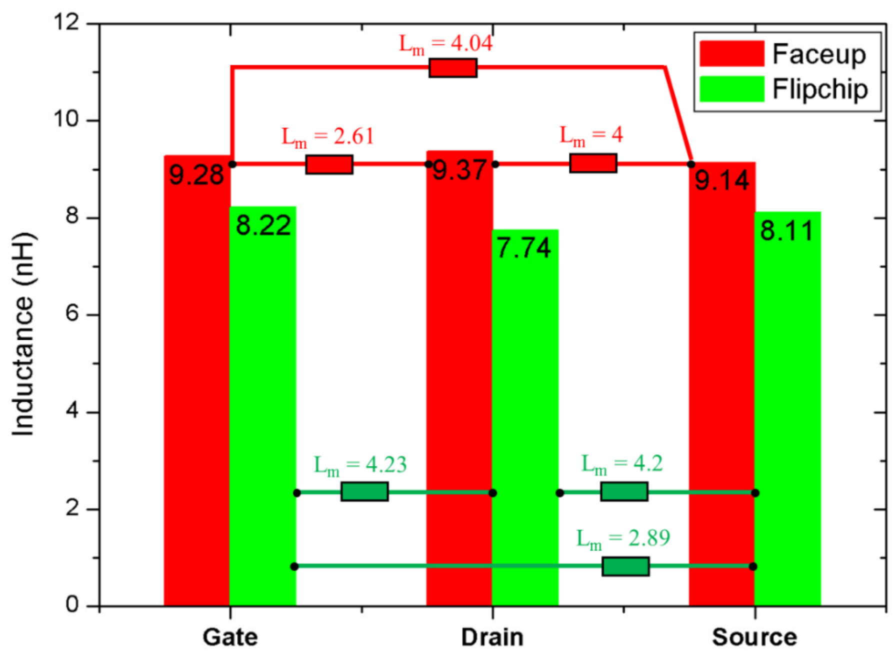


Figure 5.39: Self/mutual parasitic inductance comparison for face up and flip chip system observed at 500 kHz frequency

Figure 5.40 shows the self-capacitance for face up and flip chip mounted system at 500kHz, flip chip system shows high parasitic capacitance due to the various interconnection layers thicknesses and material properties.

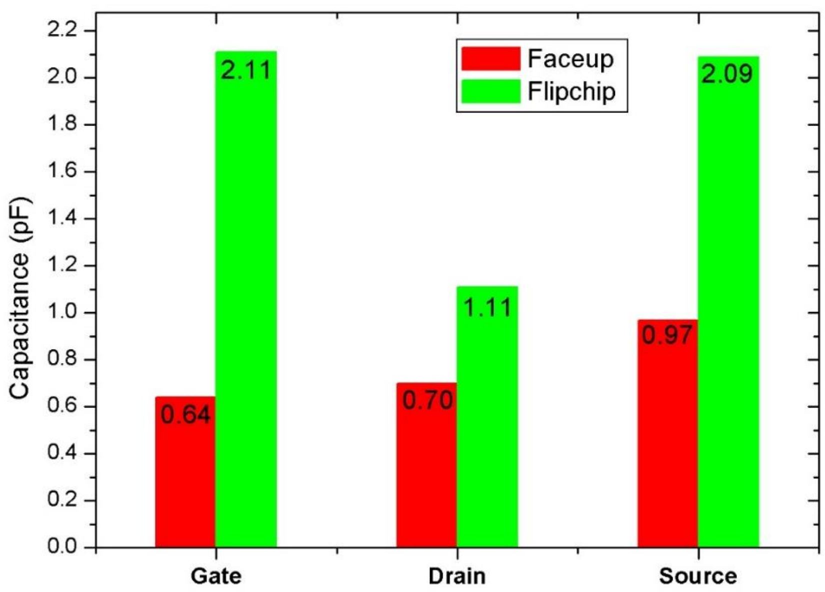


Figure 5.40 : Self-capacitance for face up and flip chip mounted system at 500 kHz frequency

5.6 Conclusion

In this Chapter, an numerical assessment of steady state and transient thermal performance of face up and flip chip GaN on Sapphire/Si/6H-SiC with respect to substrate layer thicknesses variation in a T0-220 package is presented. Extensive simulation results has proven that GaN on 6H-SiC substrates shows 54% reduction in thermal resistance when compared over GaN on sapphire substrates for face up mounted system. Further, 56% reduction in thermal resistance can be achieved by moving form face up to flip chip mounted system. In face up mounted system the substrate layer thicknesses directly influence the thermal resistance junction to case $R_{th\ (j-c)}$ whereas, in flip chip mounted system the inverse occurs. Further, extensive simulation results predicts that the maximum junction temperature rise (T_J) can be decreased by moving towards silicon/6H-SiC substrates. Under transient condition the flip chip system shows low thermal resistance at frequencies ranging <5 kHz. However, at high frequencies ranging from 5 kHz to 500 kHz the flip chip shows increased thermal resistance over the face up system. The influence of parasitic elements can be reduced further by moving towards flip chip system which reduces the self-resistance and inductance elements by 41% and 17% respectively. Mutual inductance is observed to be high for flip chip system as the copper track pad paths for drain/source/gate are placed very close to each other enabling high coupling coefficient. The parasitic capacitance for flip chip system is greater when compared over the face up system due to the various flip chip interconnection layer thicknesses and the material properties.

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CHAPTER 6 : CONCLUSIONS

This thesis has addressed the research contributions in the field of thermal management and reliability of power semiconductor packages from on-chip to package level. The thesis has described the methods to overcome challenges in power module and discrete packages, particularly in thermal management and reliability issues for Si and Wide band gap semiconductors device technologies. Some of the key results and recommendation for future work are described in this chapter.

An assessment of thermal performance of PCD and conventional AlN electrical isolating layers on DBC substrates under steady state and transient conditions for power module packaging was presented in Chapter 3. The key outcomes are

- Extensive experimental results has proven that replacing the AlN insulating layer with a PCD substrate has resulted in 74% reduction in junction-to-case thermal resistance $R_{th(j-c)}$.

- Thermal cycling reliability has demonstrated, polycrystalline diamond system exhibits similar reliability aspect when compared over the conventional AlN system with respect to safety factor and life cycle fatigue.

- Thermal simulation results performed using Ansys predict that the ploy crystalline diamond thermal resistance is less sensitive to layer thicknesses.

- The voids in the solder and copper layers does not play a significant contribution in terms of thermal contact resistance as the void percentage remains less than 1% of the solder and copper layer area.

- The increased thermal performance of PCD can benefit from a ~2 x increase in the current rating and switching frequency by a factor of ~5.7 when compared over AlN tile for a 600V DC-DC converter application.

- The use of PCD in power module could significantly increase the power density of the system. PCD has shown low thermal resistance, better thermal performance than conventional AlN which could be benefited from increase in converter power density by reducing passive filtering components as a result of the increased frequency and increase power density.

- Due to poly crystalline diamond reduced thermal resistance junction to case ($R_{th(j-c)}$), could offer significant advantages over next generation high power density devices like Wide bandgap semiconductors such as SiC power devices. When SiC power devices are mounted on polycrystalline diamond substrate using silver sintered paste die attach reduces thermal resistance junction to case ($R_{th(j-c)}$) by 63% compared to conventional Si - solder (SnAg) paste die attach.

- PCD has shown low thermal resistance, better thermal performance than conventional AlN substrate, however PCD is limited in terms of cost factor as it is five times greater than conventional AlN substrates.

- The life cycle fatigue can be performed with semiconductor dies attached on to the PCD and AlN DBC substrates using solder or silver sintered paste. The fracture strain needs to be calculated experimentally for each layers involved which could be used to calculate the fatigue life cycle from die to the bottom copper of DBC substrate.

Thermal performance of PCD on a DBC substrate was further enhanced by using direct liquid cooling technique as detailed in Chapter 4. Key findings are:

- Empirical model was used to analyse the thermal performance of circular micro pins fins, geometric and thermo-hydraulic parameters were varied accordingly to find the optimal circular micro pin fin diameter and length.

- Increase in circular micro pin fin diameter decreases thermal resistance whereas, thermal resistance decreases with increase in pin fin height up to 2.5mm. Moreover, pressure drop increases with decrease in fin diameter and fin height. There is a trade - off between thermal resistance and pressure drop with respect to flow rate as pressure drop is a direct relation of flow rate, whereas thermal resistance is inversely proportional to the flow rate.

- Micro pin fin direct cooling of DBC reduces the number of thermal layers in the system which in turn reduces the thermal resistance by 59% compared to conventional DBC cooling without base plate.

- Moreover, the high thermal conductivity of PCD can be utilised efficiently by using direct cooling technique. Four micro pin fin designs (two circular and two cone shaped micro pin fin) were chosen for fabrication using LIGA technology.

- Initial fabrication of ‘Design 3’ had adhesive issue between the bottom Copper and micro pin fins an alternative solution was used to rectify the problem. The LIGA fabrication process for rest of the ‘Designs’ are under manufacturing process.

- The empirical model has to be validated with the experimental results for ‘Design 2 and 3’ which is a recommendation for future work.

A numerical assessment of steady state and transient thermal performance of face up and flip chip GaN on Sapphire/Si/6H-SiC with respect to substrate layer thicknesses variation in a T0-220 package is detailed in Chapter 5. Flip chip system offers many advantages over face up system which are summarised below,

- Extensive simulation results has proven that GaN on 6H-SiC substrates shows 54% reduction in thermal resistance compared over GaN on sapphire substrates for face up mounted system. Further, 56% reduction in thermal resistance can be achieved by moving form face up to flip chip mounted system.

- In face up mounted system the substrate layer thicknesses directly influence the thermal resistance junction to case $R_{th\ (j-c)}$ whereas, in flip chip mounted system the inverse occurs. Further, extensive simulation results predicts that the maximum junction temperature rise (T_j) can be decreased by moving towards silicon/6H-SiC substrates.

- Under transient condition the flip chip system shows low thermal resistance at frequencies ranging <5 kHz. However, at high frequencies ranging from 5 kHz to 500 kHz the flip chip shows increased thermal resistance over the face up system.

- The influence of parasitic elements can be reduced further by moving towards flip chip system which reduces the self-resistance and inductance elements by 41% and 17% respectively. Mutual inductance is observed to be high for flip chip system as the copper track pad paths for drain/source/gate are placed very close to each other

enabling high coupling coefficient. The parasitic capacitance for flip chip system is greater when compared over the face up system due to the various flip chip interconnection layer thicknesses and the material properties.

In summary, PCD as insulator in DBC substrate has shown improved thermal performance compared over the conventional AlN DBC substrates used in power module. The improved thermal performance of PCD can be advantages by using direct liquid cooling technique. Advance wide band gap semiconductor device technology such as GaN heteroepitaxial approach on flip chip mounting technique has shown significant improved thermal performance and less package parasitic inductance compared over the face up mounting technique.

6.1 Future work

PCD as an insulator layer has shown improved thermal performance compared over the conventional insulator materials. Further, the thermal and electrical performance of PCD substrates can be evaluated on a single phase full bridge or a three phase converter module. Impact on converter weight, size and power density using PCD and conventional substrates can be evaluated and compared. The reliability fatigue life cycle prediction for PCD substrates from semiconductor Si/SiC die to bottom copper of the substrate requires extensive detailed experimental analysis to obtain the fracture strain data. Initial fabrication of micro pin fins using LIGA technology had adhesion issue between the micro pin fins and the bottom copper of the substrate. Therefore, an alternative solution to overcome the adhesion issue as discussed in Chapter 4 has being employed. The empirical model for micro pin fins has to be verified experimentally. The thermal performance of flip chip and face up mounting for GaN semiconductor device on a T0-220 package has been evaluated and compared. Further, the thermal and parasitic inductance performance of flip chip and face up mounting for GaN can be evaluated for surface mount packages such as S0-8, SOT-23 and QFN (Quad-flat no-leads). The impact of GaN face up and flip chip mounting technique on a converter thermal and parasitic inductance performance can be evaluated.

6.2 Publications

- Submitted technical report for diamond demonstrator work to Rolls Royce regarding thermal packaging of semiconductor device, document no: RR-USH DIAMONDDEMO-TR-2013-001.

- M. Balakrishnan, M. R. Sweet, and E. M. Sankara Narayanan, "Comparison of the thermal properties of polycrystalline diamond and aluminium nitride substrates," in *Industrial Electronics Society, IECON 2013 - 39th Annual Conference of the IEEE*, 2013, pp. 544-548.

- Balakrishnan, Manoj; Sweet, M.R.; Narayanan, E.M.Sankara, "Thermal cycling reliability of polycrystalline diamond and aluminium nitride substrates," *Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM), 2014 International Symposium on* , vol., no., pp.128,132, 18-20 June 2014.

- M. Balakrishnan, M. R. Sweet, and E. M. Sankara Narayanan, "Comparison of the thermal performance of polycrystalline diamond and aluminium nitride substrates," in IEEE transaction on Power Electronics (Submitted for review).

APPENDICES

1. Infineon's IGBT4 Low Power Chip," IGC27T120T6L

IGC27T120T6L

IGBT4 Low Power Chip

FEATURES:

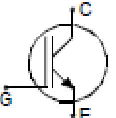
- 1200V Trench + Field Stop technology
- low switching losses
- positive temperature coefficient
- easy paralleling

This chip is used for:

- low / medium power modules

Applications:

- low / medium power drives



Chip Type	V_{CE}	I_{Cn}	Die Size	Package
IGC27T120T6L	1200V	25A	4.99 x 5.45 mm^2	sawn on foil

MECHANICAL PARAMETER		
Raster size	4.99 x 5.45	mm^2
Emitter pad size	3.182 x 3.962	mm^2
Gate pad size	0.826 x 1.31	mm^2
Area total / active	27.2 / 17.3	mm^2
Thickness	115	µm
Wafer size	150	mm
Flat position	90	grd
Max.possible chips per wafer	537	
Passivation frontside	Photoimide	
Pad metal	3200 nm AlSiCu	
Backside metal	Ni Ag –system suitable for epoxy and soft solder die bonding	
Die bond	Electrically conductive glue or solder	
Wire bond	Al, <500µm	
Reject ink dot size	∅ 0.65mm ; max 1.2mm	
Recommended storage environment	Store in original container, in dry nitrogen, < 6 month at an ambient temperature of 23°C	

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IGC27T120T6L

MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Collector-Emitter voltage, T_j=25 °C	V_{CE}	1200	V
DC collector current, limited by T_{jmax}	I_C	[1]	A
Pulsed collector current, t_p limited by T_{jmax}	I_{cpuls}	75	A
Gate-Emitter voltage	V_{GE}	±20	V
Operating junction temperature	T_j	-40 ... +175	°C
Short circuit data [2] V_{GE} = 15V, V_{CC} = 800V, Tvj = 150°C	tp	10	µs
Reverse bias safe operating area [2] (RBSOA)	$I_{C\,max}$ = 50A, $V_{CE\,max}$ = 1200V, Tvj max= 150°C		

[1] depending on thermal properties of assembly

[2] not subject to production test - verified by design/characterization

STATIC CHARACTERISTICS (tested on wafer), T_j=25 °C

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Collector-Emitter breakdown voltage	$V_{(BR)CES}$	V_{GE}=0V , I_C= 0.85 mA	1200			V
Collector-Emitter saturation voltage	$V_{CE(sat)}$	V_{GE}=15V, I_C=25 A	1.6	1.85	2.1	V
Gate-Emitter threshold voltage	$V_{GE(th)}$	I_C=0.85m A , V_{GE}=V_{CE}	5.0	5.8	6.5	V
Zero gate voltage collector current	I_{CES}	V_{CE}=1200V , V_{GE}=0V			2.4	µA
Gate-Emitter leakage current	I_{GES}	V_{CE}=0V , V_{GE}=20V			120	nA
Integrated gate resistor	R_{Gint}			-		Ω

ELECTRICAL CHARACTERISTICS (not subject to production test - verified by design/characterization)

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Input capacitance	C_{iss}	V_{CE}=25V, V_{GE}=0V, f=1MHz		1430		pF
Output capacitance	C_{oss}			115		pF
Reverse transfer capacitance	C_{rss}			85		pF

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IGC27T120T6L

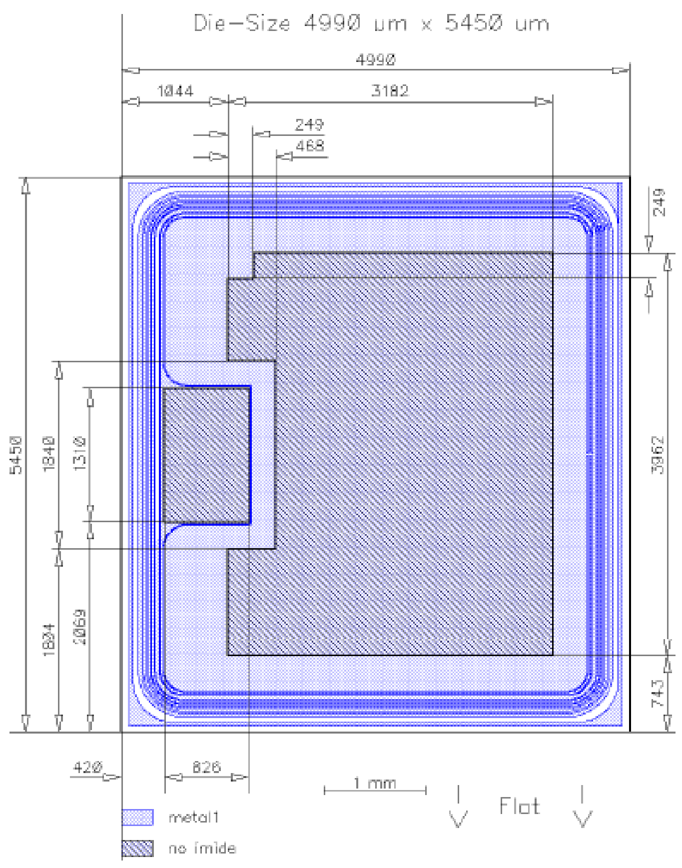
SWITCHING CHARACTERISTICS inductive load (not subject to production test - verified by design /characterization)

Parameter	Symbol	Conditions [1]	Value			Unit
			min.	typ.	max.	
Turn-on delay time	$t_{d(on)}$	T_j=125°C V_{CC}=600V, I_C=25A, V_{GE}=-15/15V, R_G= ---Ω		tbd		ns
Rise time	t_r			tbd		
Turn-off delay time	$t_{d(off)}$			tbd		
Fall time	t_f			tbd		

[1] values also influenced by parasitic L- and C- in measurement and package.

IGC27T120T6L

CHIP DRAWING



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IGC27T120T6L

FURTHER ELECTRICAL CHARACTERISTICS

This chip data sheet refers to the device data sheet	tbd	

DESCRIPTION

AQL 0,65 for visual inspection according to failure catalogue
Electrostatic Discharge Sensitive Device according to MIL-STD 883
Test-Normen Villach/Prüffeld

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2. Infineon's TRENCHSTOP IGBT technology," IGW25N120H3 datasheet

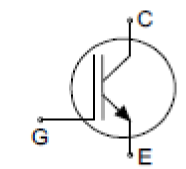
IGW25N120H3

High speed switching series third generation

High speed IGBT in Trench and Fieldstop technology
recommended in combination with SiC Diode IDH15S120

Features:

TRENCHSTOP™ technology offering
- best in class switching performance: less than 500µJ total switching losses achievable
- very low V_{CEsat}
- low EMI
- maximum junction temperature 175°C
- qualified according to JEDEC for target applications
- Pb-free lead plating; RoHS compliant
- complete product spectrum and PSpice Models: http://www.infineon.com/igbt/



Applications:

- solar inverters
- uninterruptible power supplies
- welding converters
- converters with high switching frequency

Package pin definition:

- Pin 1 - gate
- Pin 2 & backside - collector
- Pin 3 - emitter

Green

Key Performance and Package Parameters

Type	V_{CE}	I_C	V_{CEsat}, T_{vj}=25°C	T_{vjmax}	Marking	Package
IGW25N120H3	1200V	25A	2.05V	175°C	G25H1203	PG-TO247-3

IGW25N120H3

High speed switching series third generation

Maximum ratings

Parameter	Symbol	Value	Unit
Collector-emitter voltage	V_{CE}	1200	V
DC collector current, limited by T_{vjmax} T_C = 25°C T_C = 100°C	I_C	50.0 25.0	A
Pulsed collector current, t_p limited by T_{vjmax}	I_{Cpuls}	100.0	A
Turn off safe operating area $V_{CE} \leq$ 1200V, $T_{vj} \leq$ 175°C	-	100.0	A
Gate-emitter voltage	V_{GE}	±20	V
Short circuit withstand time V_{GE} = 15.0V, $V_{CC} \leq$ 600V Allowed number of short circuits < 1000 Time between short circuits: ≥ 1.0s T_{vj} = 175°C	t_{SC}	10	µs
Power dissipation T_C = 25°C Power dissipation T_C = 100°C	P_{tot}	326.0 156.0	W
Operating junction temperature	T_{vj}	-40...+175	°C
Storage temperature	T_{stg}	-55...+150	°C
Soldering temperature, wave soldering 1.6 mm (0.063 in.) from case for 10s		260	°C
Mounting torque, M3 screw Maximum of mounting processes: 3	M	0.6	Nm

Thermal Resistance

Parameter	Symbol	Conditions	Max. Value	Unit
Characteristic				
IGBT thermal resistance, junction - case	$R_{th(j-c)}$		0.46	K/W
Thermal resistance junction - ambient	$R_{th(j-a)}$		40	K/W

Electrical Characteristic, at T_{vj} = 25°C, unless otherwise specified

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Static Characteristic						
Collector-emitter breakdown voltage	$V_{(BR)CES}$	V_{GE} = 0V, I_C = 0.50mA	1200	-	-	V
Collector-emitter saturation voltage	V_{CEsat}	V_{GE} = 15.0V, I_C = 25.0A T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 175°C	- - -	2.05 2.50 2.70	2.40 - -	V
Gate-emitter threshold voltage	$V_{GE(th)}$	I_C = 0.85mA, V_{CE} = V_{GE}	5.0	5.8	6.5	V
Zero gate voltage collector current	I_{CES}	V_{CE} = 1200V, V_{GE} = 0V T_{vj} = 25°C T_{vj} = 175°C	- -	- -	250.0 2500.0	µA
Gate-emitter leakage current	I_{GES}	V_{CE} = 0V, V_{GE} = 20V	-	-	600	nA
Transconductance	g_{fs}	V_{CE} = 20V, I_C = 25.0A	-	13.0	-	S

IGW25N120H3

High speed switching series third generation

Electrical Characteristic, at T_{vj} = 25°C, unless otherwise specified

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Dynamic Characteristic						
Input capacitance	C_{ies}	V_{CE} = 25V, V_{GE} = 0V, f = 1MHz	-	1430	-	pF
Output capacitance	C_{oes}		-	95	-	
Reverse transfer capacitance	C_{res}		-	75	-	
Gate charge	Q_G	V_{CC} = 960V, I_C = 25.0A, V_{GE} = 15V	-	115.0	-	nC
Short circuit collector current Max. 1000 short circuits Time between short circuits: ≥ 1.0s	$I_{C(SC)}$	V_{GE} = 15.0V, V_{CC} ≤ 600V, t_{SC} ≤ 10μs T_{vj} = 175°C	-	87	-	A

Switching Characteristic, Inductive Load

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
IGBT Characteristic, at T_{vj} = 25°C						
Turn-on delay time	$t_{d(on)}$	T_{vj} = 25°C, V_{CC} = 600V, I_C = 25.0A, V_{GE} = 0.0/15.0V, r_G = 23.0Ω, $L\sigma$ = 80nH, $C\sigma$ = 67pF $L\sigma$, $C\sigma$ from Fig. E Energy losses include "tail" and diode (IKW25N120H3) reverse recovery.	-	27	-	ns
Rise time	t_r		-	41	-	ns
Turn-off delay time	$t_{d(off)}$		-	277	-	ns
Fall time	t_f		-	17	-	ns
Turn-on energy	E_{on}		-	1.80	-	mJ
Turn-off energy	E_{off}		-	0.85	-	mJ
Total switching energy	E_{ts}		-	2.65	-	mJ
Turn-on energy	E_{on}	T_{vj} = 25°C, V_{CC} = 800V, I_C = 10.0A, V_{GE} = 0.0/15.0V, r_G = 3.0Ω, $L\sigma$ = 80nH, $C\sigma$ = 67pF $L\sigma$, $C\sigma$ from Fig. E Energy losses include "tail" and diode (IDH15S120) reverse recovery.	-	0.08	-	mJ
Turn-off energy	E_{off}		-	0.27	-	mJ
Total switching energy	E_{ts}		-	0.35	-	mJ

IGW25N120H3

High speed switching series third generation

Switching Characteristic, Inductive Load

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
IGBT Characteristic, at T_{vj} = 175°C						
Turn-on delay time	$t_{d(on)}$	T_{vj} = 175°C, V_{CC} = 600V, I_C = 25.0A, V_{GE} = 0.0/15.0V, r_G = 23.0Ω, $L\sigma$ = 80nH, $C\sigma$ = 67pF $L\sigma$, $C\sigma$ from Fig. E Energy losses include "tail" and diode (IKW25N120H3) reverse recovery.	-	26	-	ns
Rise time	t_r		-	35	-	ns
Turn-off delay time	$t_{d(off)}$		-	347	-	ns
Fall time	t_f		-	50	-	ns
Turn-on energy	E_{on}		-	2.60	-	mJ
Turn-off energy	E_{off}		-	1.70	-	mJ
Total switching energy	E_{ts}		-	4.30	-	mJ
Turn-on energy	E_{on}	T_{vj} = 175°C, V_{CC} = 800V, I_C = 10.0A, V_{GE} = 0.0/15.0V, r_G = 3.0Ω, $L\sigma$ = 80nH, $C\sigma$ = 67pF $L\sigma$, $C\sigma$ from Fig. E Energy losses include "tail" and diode (IDH15S120) reverse recovery.	-	0.10	-	mJ
Turn-off energy	E_{off}		-	0.62	-	mJ
Total switching energy	E_{ts}		-	0.72	-	mJ

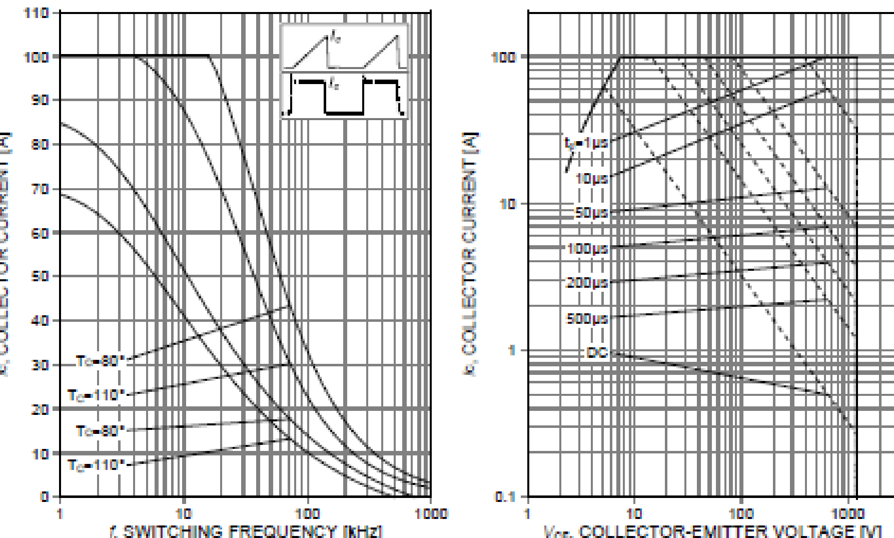


Figure 1. **Collector current as a function of switching frequency**
(T_j≤175°C, D=0.5, V_{CE}=600V, V_{GE}=15/0V, r_G=23Ω)

Figure 2. **Forward bias safe operating area**
(D=0, T_C=25°C, T_j≤175°C; V_{GE}=15V)

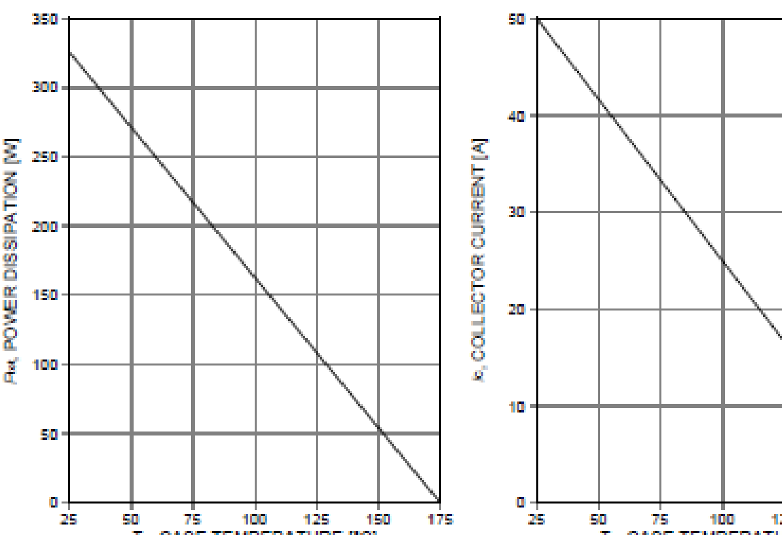


Figure 3. **Power dissipation as a function of case temperature**
(T_j≤175°C)

Figure 4. **Collector current as a function of case temperature**
(V_{GE}≥15V, T_j≤175°C)

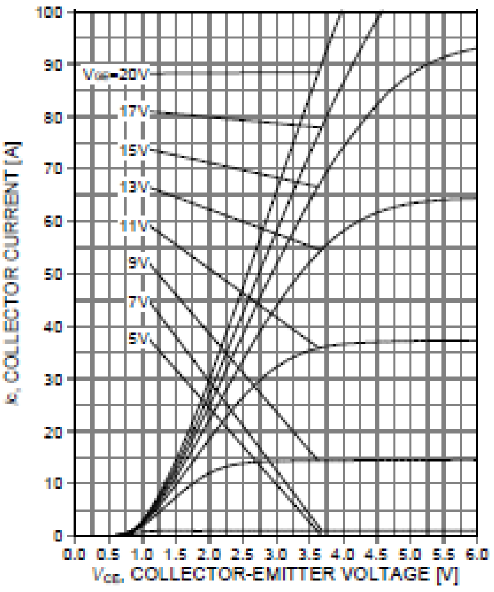


Figure 5. **Typical output characteristic**
(T_j=25°C)

Figure 6. **Typical output characteristic**
(T_j=175°C)

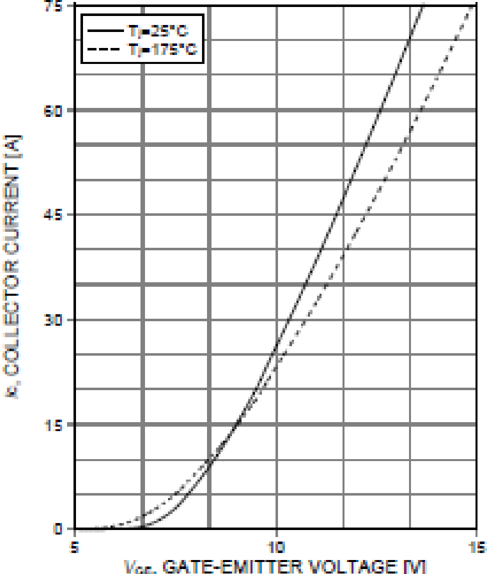


Figure 7. **Typical transfer characteristic**
(V_{CE}=20V)

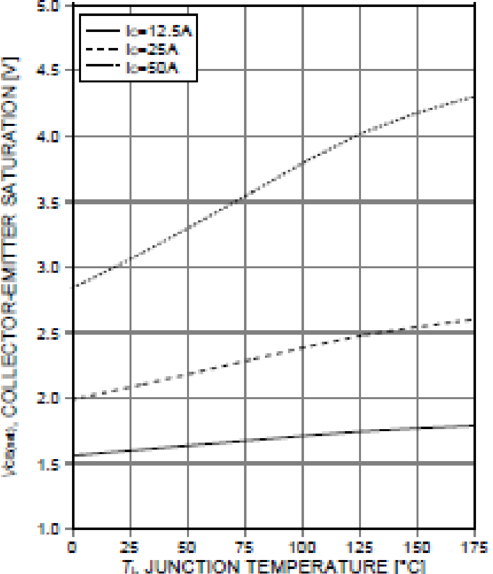


Figure 8. **Typical collector-emitter saturation voltage as a function of junction temperature**
(V_{GE}=15V)

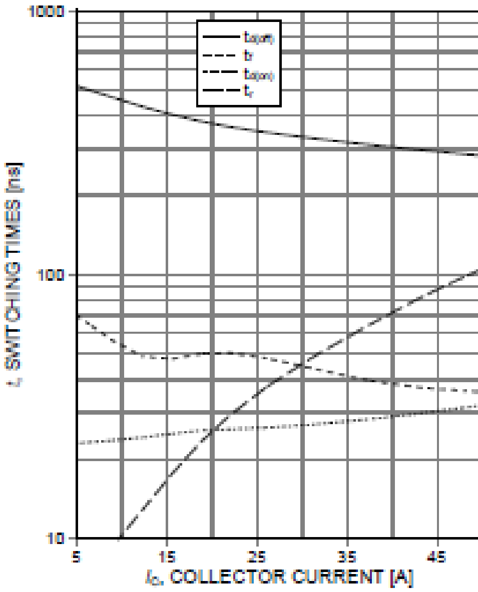


Figure 9. Typical switching times as a function of collector current
(ind. load, T_j=175°C, V_{CE}=600V, V_{GE}=15/0V, r_G=23Ω, test circuit in Fig. E)

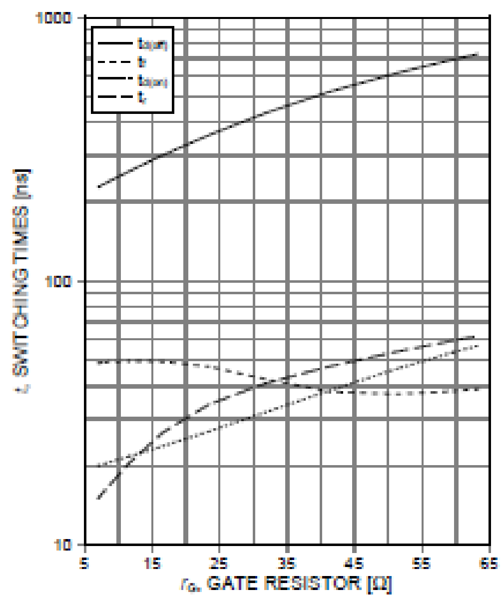


Figure 10. Typical switching times as a function of gate resistor
(ind. load, T_j=175°C, V_{CE}=600V, V_{GE}=15/0V, I_C=25A, test circuit in Fig. E)

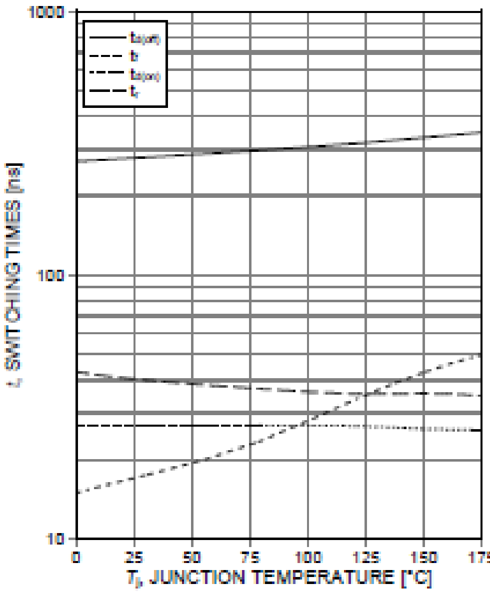


Figure 11. Typical switching times as a function of junction temperature
(ind. load, V_{CE}=600V, V_{GE}=15/0V, I_C=25A, r_G=23Ω, test circuit in Fig. E)

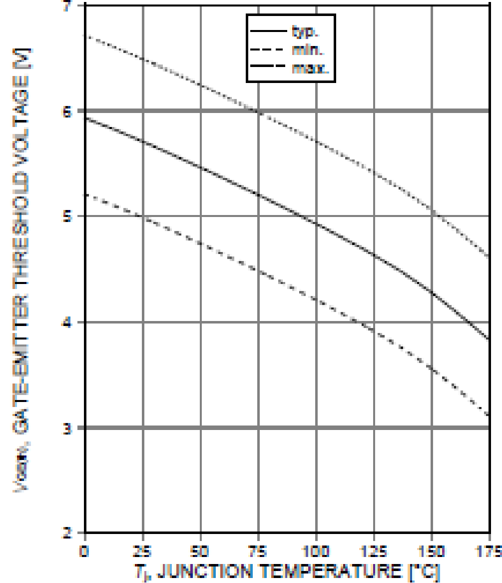


Figure 12. Gate-emitter threshold voltage as a function of junction temperature
(I_C=0.85mA)

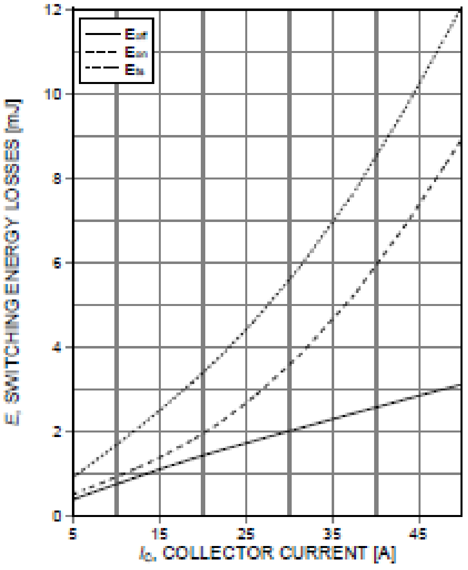


Figure 13. **Typical switching energy losses as a function of collector current**
(ind. load, T_j=175°C, V_{CE}=600V, V_{GE}=15/0V, r_G=23Ω, test circuit in Fig. E)

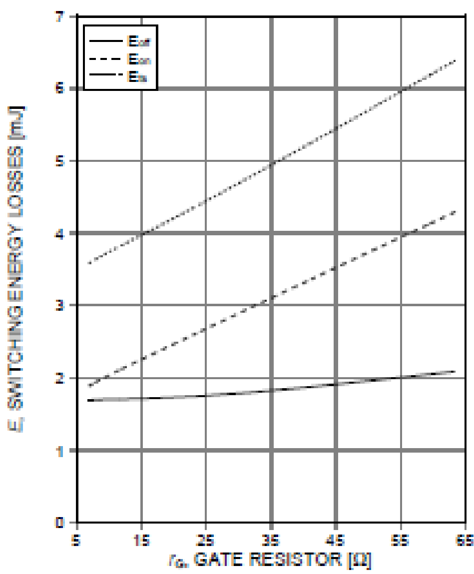


Figure 14. **Typical switching energy losses as a function of gate resistor**
(ind. load, T_j=175°C, V_{CE}=600V, V_{GE}=15/0V, I_C=25A, test circuit in Fig. E)

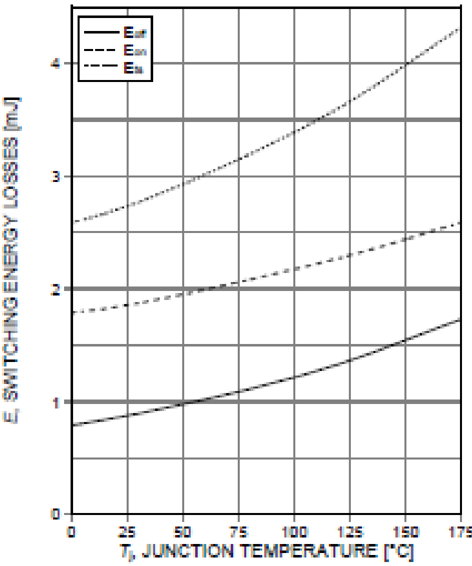


Figure 15. **Typical switching energy losses as a function of junction temperature**
(ind load, V_{CE}=600V, V_{GE}=15/0V, I_C=25A, r_G=23Ω, test circuit in Fig. E)

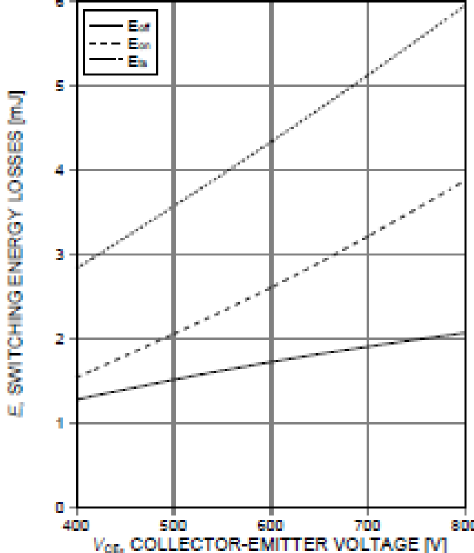


Figure 16. **Typical switching energy losses as a function of collector emitter voltage**
(ind. load, T_j=175°C, V_{GE}=15/0V, I_C=25A, r_G=23Ω, test circuit in Fig. E)

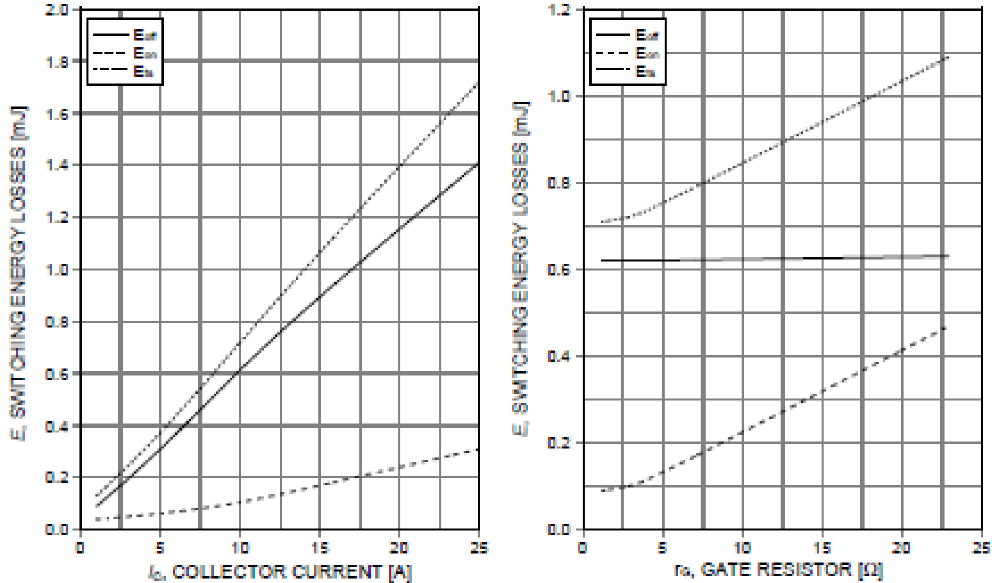


Figure 1. Typical switching energy losses as a function of collector current
(ind. load, T_j=125°C, V_{CE}=800V, V_{GE}=15/0V, r_G=3Ω, Diode IDH15S120)

Figure 2. Typical switching energy losses as a function of gate resistor
(ind. load, T_j=125°C, V_{CE}=800V, V_{GE}=15/0V, I_C=10A, Diode IDH15S120)

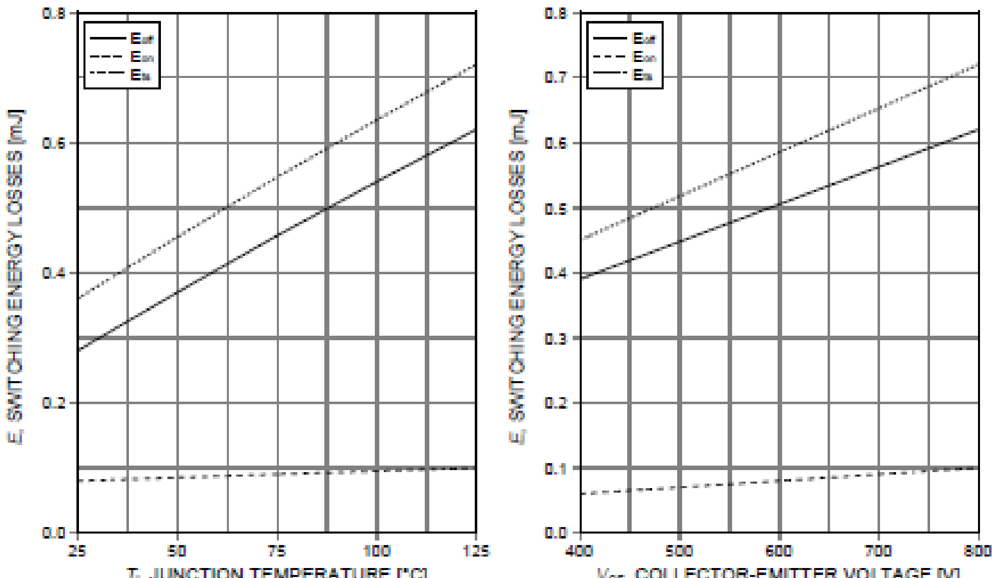


Figure 3. Typical switching energy losses as a function of junction temperature
(ind load, V_{CE}=800V, V_{GE}=15/0V, I_C=10A, r_G=3Ω, Diode IDH15S120)

Figure 4. Typical switching energy losses as a function of collector emitter voltage
(ind. load, T_j=125°C, V_{GE}=15/0V, I_C=10A, r_G=3Ω, Diode IDH15S120)

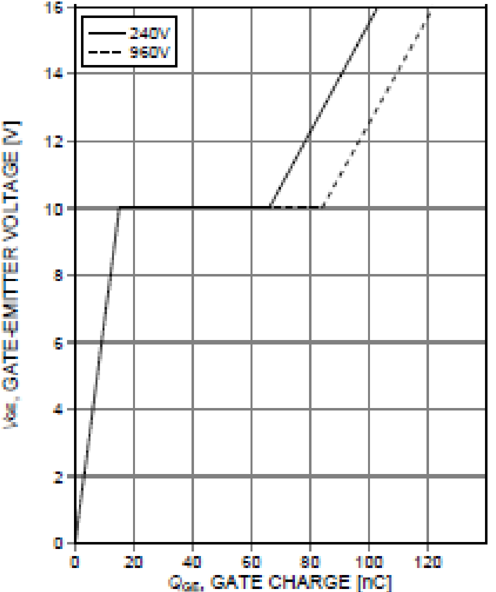


Figure 17. Typical gate charge
(I_C=25A)

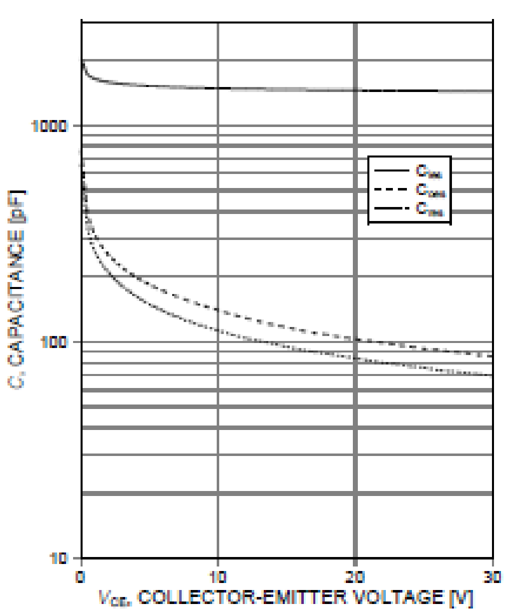


Figure 18. Typical capacitance as a function of collector-emitter voltage
(V_{GE}=0V, f=1MHz)

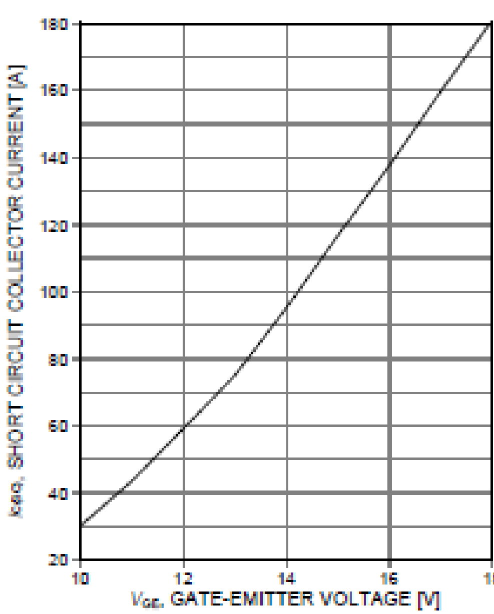


Figure 19. Typical short circuit collector current as a function of gate-emitter voltage
(V_{CE}≤600V, start at T_j=25°C)

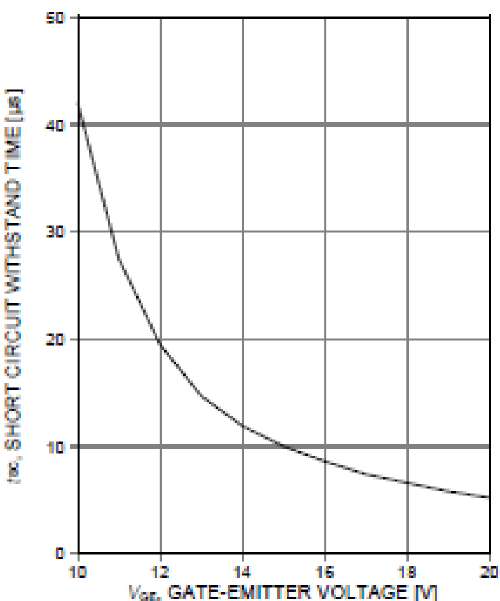


Figure 20. Short circuit withstand time as a function of gate-emitter voltage
(V_{CE}≤600V, start at T_j≤150°C)

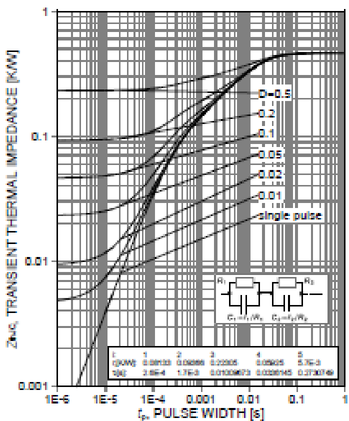
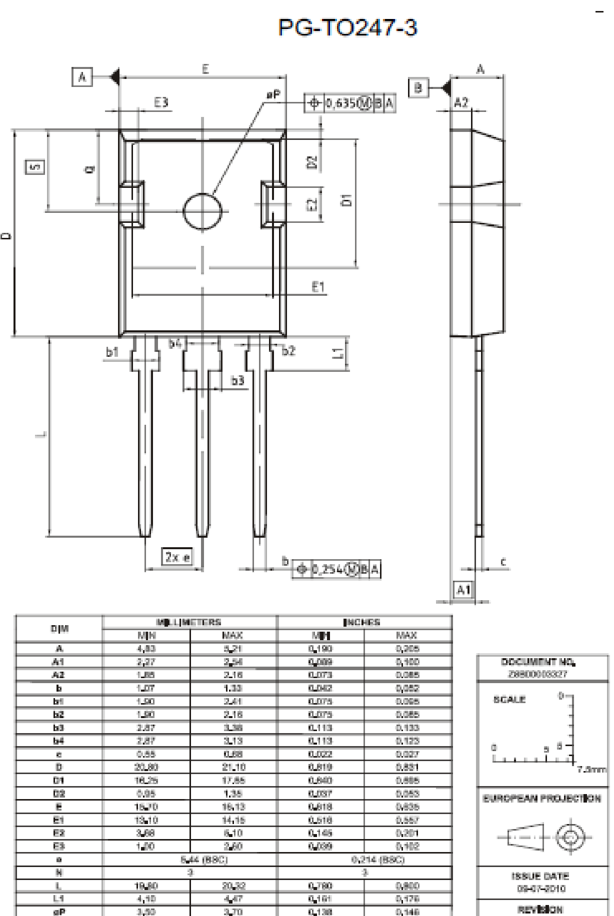


Figure 21. IGBT transient thermal impedance ($D=t_p/T$)

IGW25N120H3

High speed switching series third generation

PG-TO247-3



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4,83	5,21	0,190	0,205
A1	2,27	2,54	0,089	0,100
A2	1,85	2,16	0,073	0,085
b	1,07	1,33	0,042	0,052
b1	1,90	2,41	0,075	0,095
b2	1,90	2,16	0,075	0,085
b3	2,87	3,38	0,113	0,133
b4	2,87	3,13	0,113	0,123
c	0,55	0,68	0,022	0,027
D	20,80	21,10	0,819	0,831
D1	16,25	17,65	0,640	0,695
D2	0,95	1,35	0,037	0,053
E	15,70	16,13	0,618	0,635
E1	13,10	14,15	0,516	0,557
E2	3,68	5,10	0,145	0,201
E3	1,00	2,60	0,039	0,102
e	5,44 (BSC)		0,214 (BSC)	
N	3		3	
L	19,80	20,32	0,780	0,800
L1	4,10	4,47	0,161	0,176
øP	3,50	3,70	0,138	0,146
Q	5,49	6,00	0,216	0,236
S	6,04	6,30	0,238	0,248

DOCUMENT NO. Z8B00003327

SCALE

EUROPEAN PROJECTION

ISSUE DATE 09-07-2010

REVISION 05

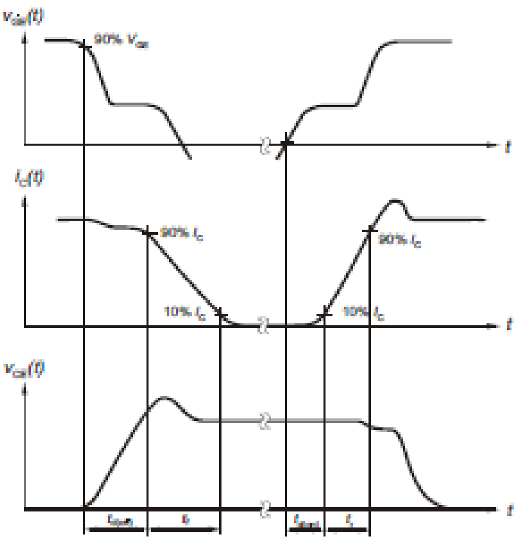


Figure A. Definition of switching times

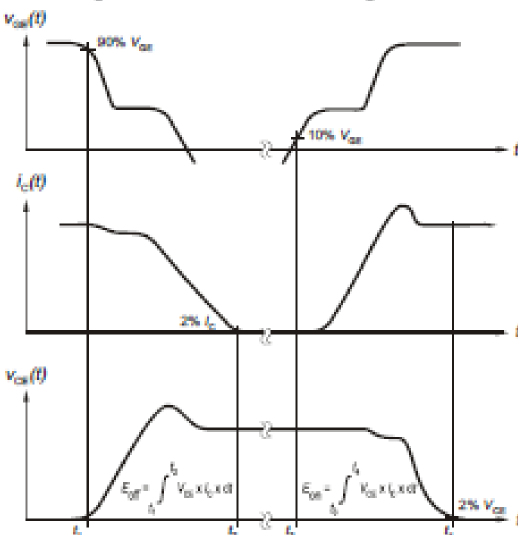


Figure B. Definition of switching losses

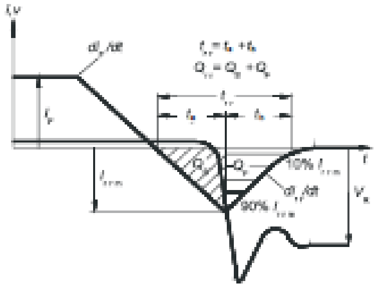


Figure C. Definition of diodes switching characteristics

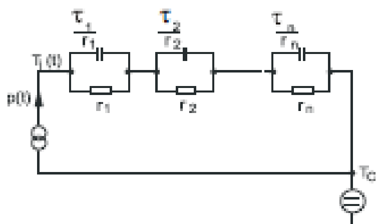


Figure D. Thermal equivalent circuit

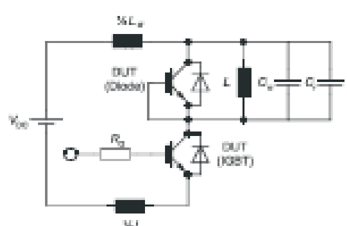


Figure E. Dynamic test circuit
Parasitic inductance L_σ,
Parasitic capacitor C_σ,
Relief capacitor C_r
(only for ZVT switching)

Revision History

IGW25N120H3

Revision: 2014-02-27, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
1.1	2011-12-12	Preliminary data sheet
2.1	2014-02-27	Final data sheet

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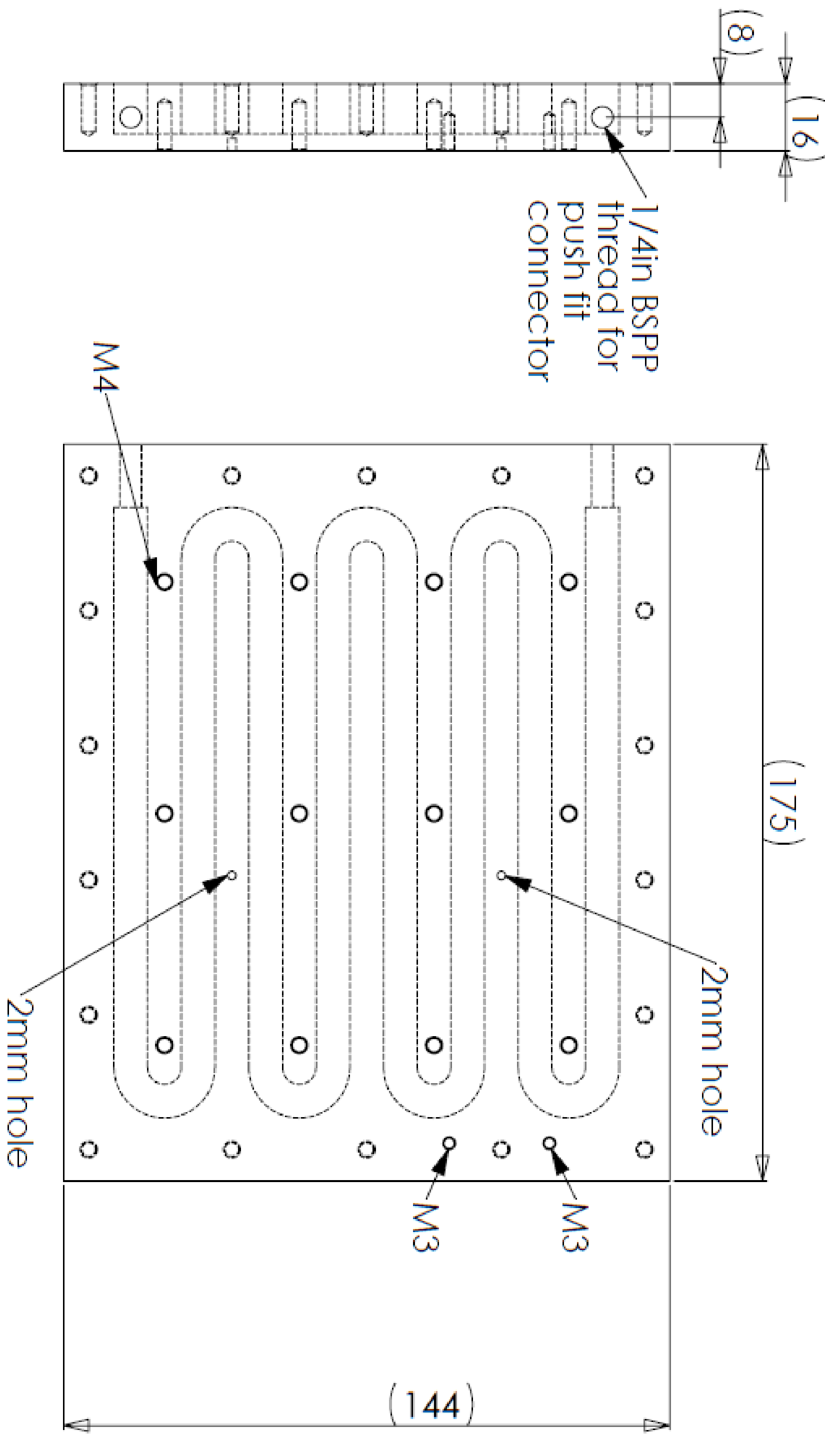
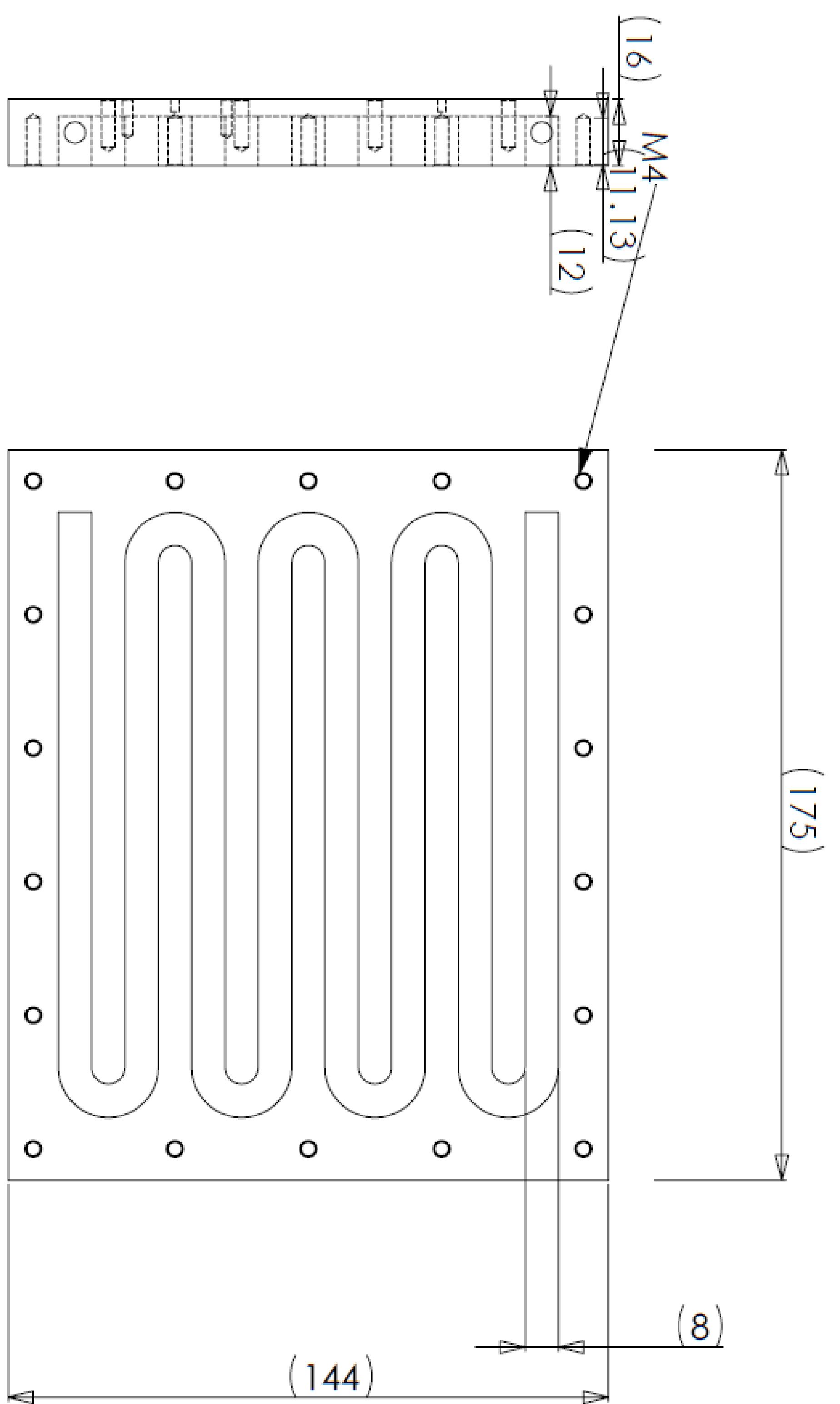
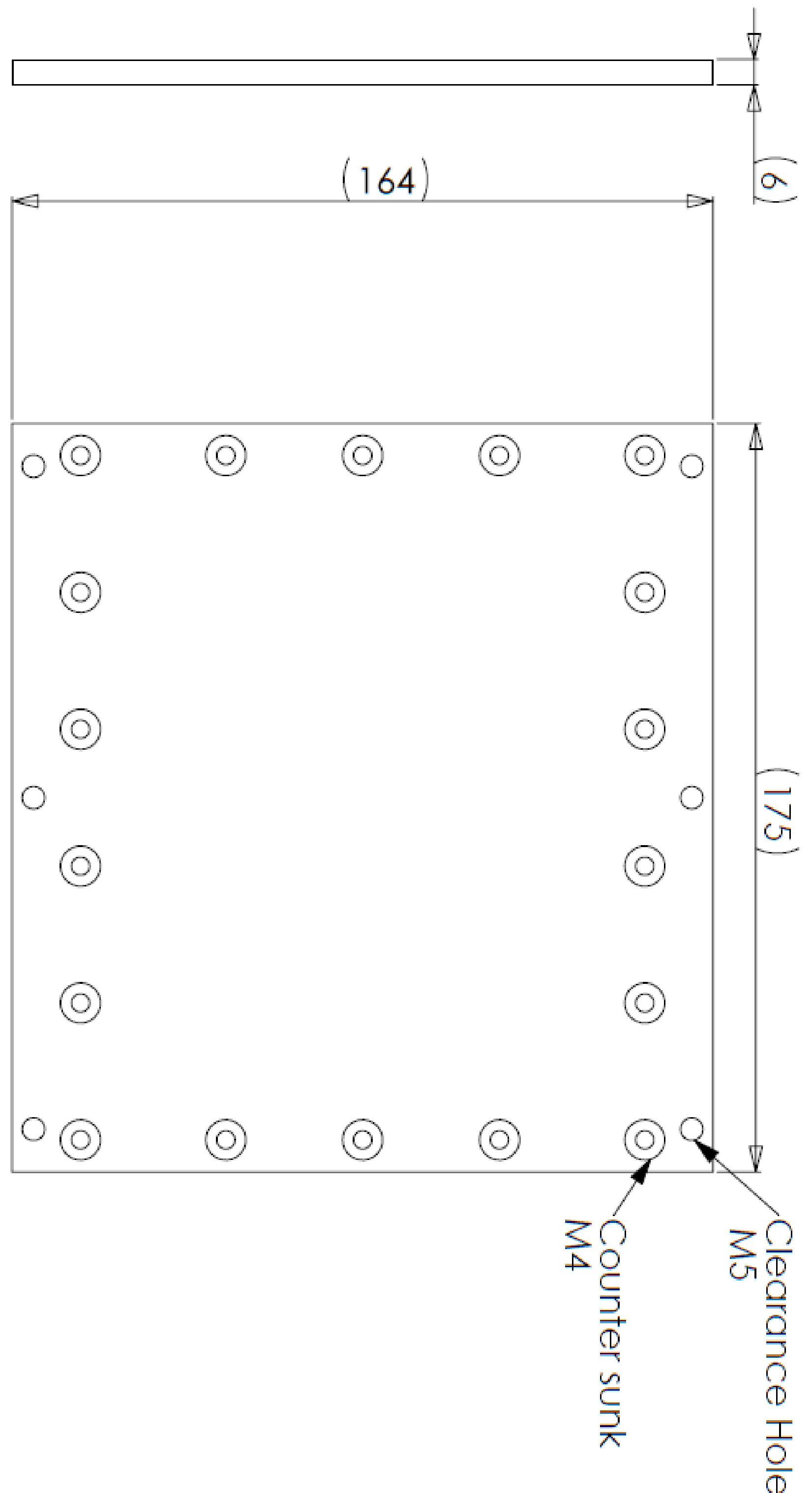
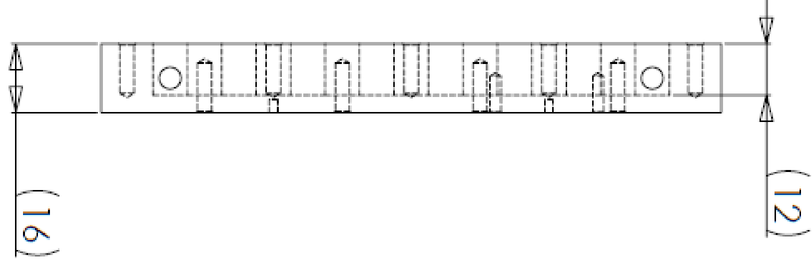
3. Liquid coold heat sink design




(16)
M4
11.13
(12)
(175)
(8)
(144)



(164)
(6)
(175)
Counter sunk M4
Clearance Hole M5


(16)
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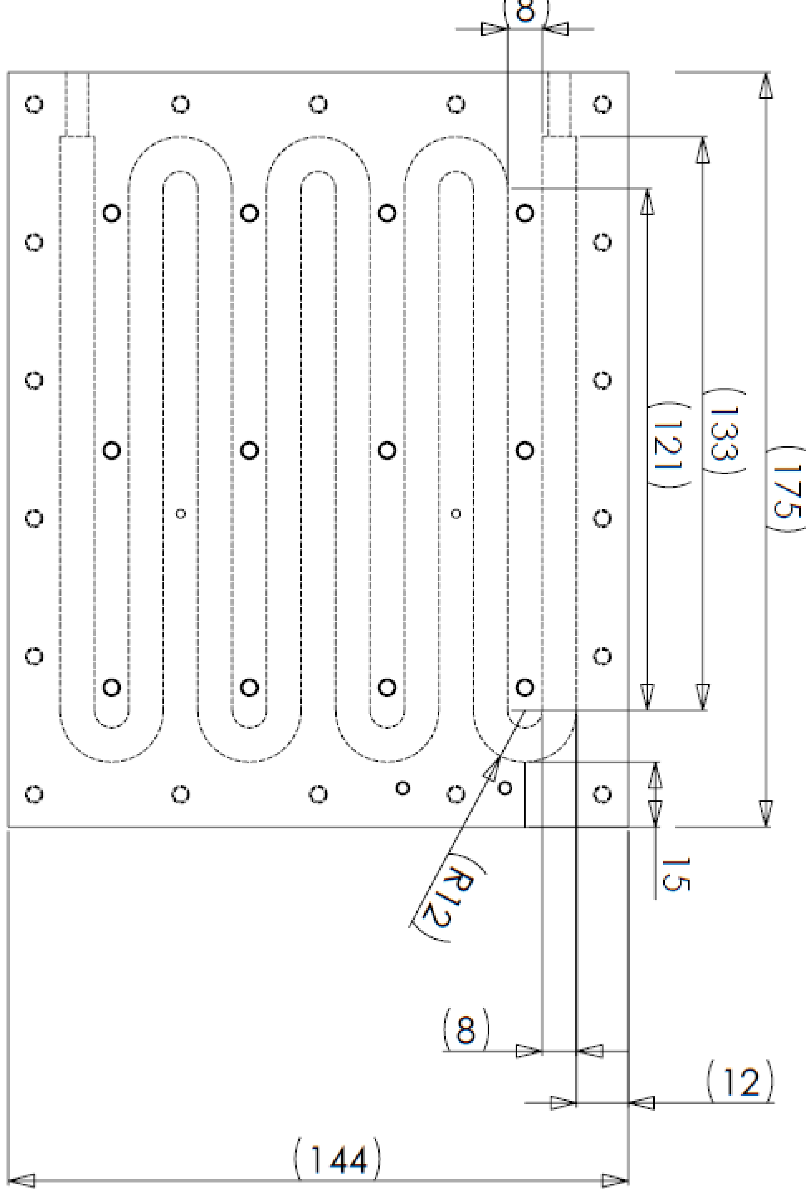

(8)
(133)
(121)
(175)
15
(R12)
(8)
(12)
(144)

4. Lead free solder paste – SynTECH-LF 96.5Sn/3.0Ag/0.5Cu

500 Main Street, Suite 18
PO Box 989
Deep River, CT 06417 USA
Toll Free: 800.435.0317
Phone: 860.526.8300
Fax: 860.526.8243
www.amtechsolder.com

SMD291SNL,SMD291SNL10,SMD291SNL10T5,
SMD291SNL250T3, SMD291SNL250T5

SynTECH-LF Lead Free Solder Paste

Product Data Sheet

Product Highlights

- ROL0 flux classification
- Higher viscosity solder paste for better print definition
- Clear residue
- Low voiding
- RoHS II and REACH compliant
- Compatible with enclosed printing heads
- Print & Dispense grade solder paste available
- Passes BONO Test @ 1.56%

Available Alloys

Alloy	Temp °C	Temp °F
42Sn/58Bi	138	280
42Sn/57Bi/1Ag	138	280
96.5Sn/3.0Ag/0.5Cu	217-220	423-428
99.0Sn/0.3Ag/0.7Cu	217-221	423-430
96.5Sn/3.5Ag	221	430
99.3Sn/0.7Cu	227	441
95Sn/5Sb	235-240	455-464
95Sn/5Ag	221-245	430-473

Packaging

500 gram jars, 500gram cartridges
35 or 100 gram syringes ProFlow cassettes

Test Results

Test J-STD-004 or other requirements (as stated)	Test Requirement	Result
Copper Mirror	IPC-TM-650: 2.3.32	L: No breakthrough
Corrosion	IPC-TM-650: 2.6.15	L: No Corrosion
Quantitative Halides	IPC-TM-650: 2.3.28.1	L: <0.5%
Electrochemical Migration	IPC-TM-650: 2.6.14.1	L: <1 decade drop (No-clean)
Surface Insulation Resistance 85 °C, 85% RH @ 168 Hours	IPC-TM-650: 2.6.3.7	L: ≥100 MΩ (No Clean)
Tack Value	IPC-TM-650: 2.4.44	64g
Viscosity - Malcom @ 10 RPM/25 °C ($x10^3$mPa/s)-SAC305 T3/T4	IIPC-TM-650: 2.4.34.4	Print: 155-215 Dispensing: 125-170
Visual	IPC-TM-650: 3.4.2.5	Clear and free from precipitation
Conflict Minerals Compliance	Electronic Industry Citizenship Coalition (EICC)	Compliant
REACH Compliance	Articles 33 and 67 of Regulation (EC) No 1907/2006	Contains no substance >0.1% w/w that is listed as a SVHC or restricted for use in solder materials

SynTECH-LF Lead Free Solder Paste

Printer Operation

TThe following are general guidelines for stencil printer optimization with SynTECH-LF. Some adjustments may be necessary based on your process requirements.

Print Speed: 25-100 mm/sec
Squeegee Pressure: 70-250g/cm of blade
Under Stencil Wipe: Once every 10-25 prints, or as necessary

Stencil Life

>12 hours @ 30-45% RH and 20-25 °C
~ 4 hours @ 45-75% RH and 20-25 °C

Cleaning

SynTECH-LF is a no-clean solder paste that does not require cleaning for most SMT assemblies. For applications requiring cleaning, SynTECH-LF can be cleaned using commercially available flux residue removers such as Kyzen Aquanox A4241, A4520, A4625 and A4625B (Batch Cleaners). Kyzen brand cleaners are available from Amtech.

Amtech Low Oxide Powder Distribution

Micon Size	Type	Pitch Requirements
45 - 75µ	Type-2	24 mil and above
25 - 45µ	Type-3	16 - 24 mil
20 - 38µ	Type-4	12 - 16 mil
15 - 25µ	Type-5	8 - 12 mil
5 - 15µ	Type-6	5 - 8 mil
2 - 11µ	Type-7	< 5 mil

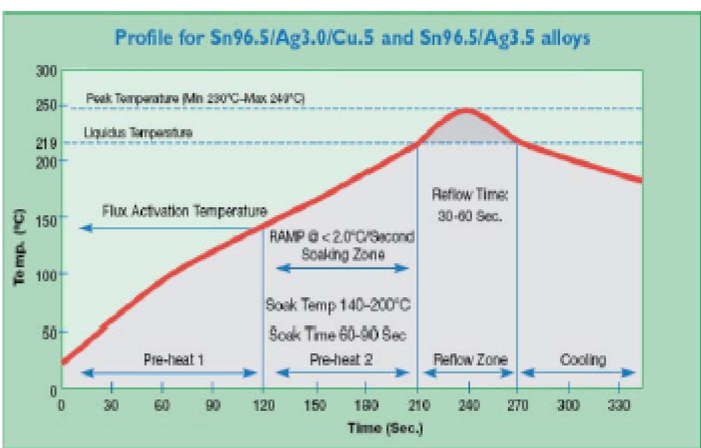
Note: Type-6 and Type-7 may not be available in certain alloys.
Other powder distributions are available on request.

Storage

Solder paste should be stored between 3-8 °C (37-46 °F) to obtain the maximum refrigerated shelf life of six months. Unopened solder paste stored at room temperature, 25 °C (77 °F) will have a one month shelf life. Syringes and cartridges should be stored vertically in the refrigerator with the dispensing tip down. Allow 4-8 hours for solder paste to reach an operating temperature of 20-25 °C (68-77 °F). Keep the solder paste container sealed while warming the solder paste to operating temperature. **NEVER FREEZE SOLDER PASTE.**

Recommended Profile

This profile is designed to serve as a starting point for process optimization using SynTECH-LF. To achieve better results with voiding or to reduce tombstoning, consider using a longer soaking zone, (170-220 °C) for 60-90 seconds, with a rapid pre-heat stage. If there is evidence of solder de-wetting, consider lowering the peak reflow temperature, or reduce the time above liquidus to <60 seconds.



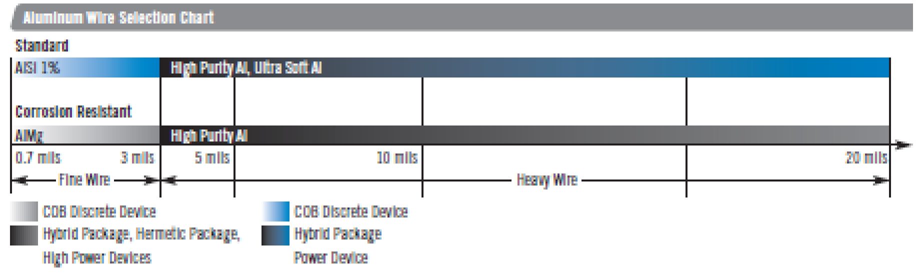
AMTECH Part Numbers

SynTECH-LF 96.5Sn/3.0Ag/0.5Cu, Type 3, 500 gram jar: Part Number: 13680
SynTECH-LF 96.5Sn/3.0Ag/0.5Cu, Type 4, 500 gram jar: Part Number: 13689
SynTECH-LF 96.5Sn/3.0Ag/0.5Cu, Type 3, 35 gram syringe: Part Number: 13650
Other alloy and packaging combinations available upon request.

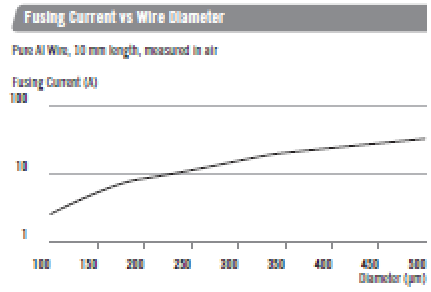
Revised February 3, 2014

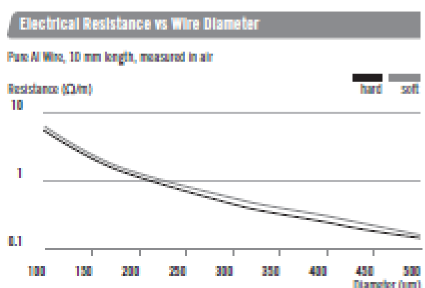
5. Fuse current for Al heavy and fine wires

Aluminum Bonding Wires

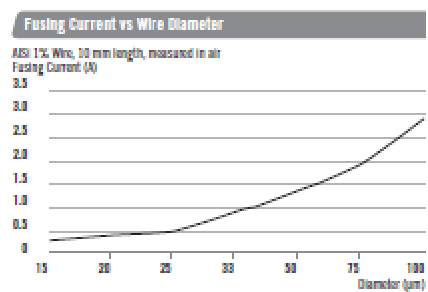


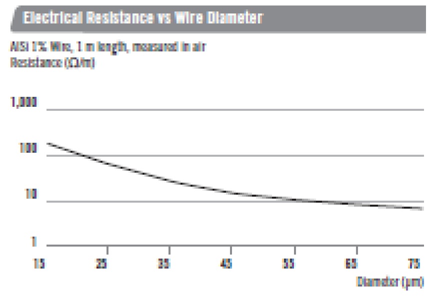
Electrical Properties of Heavy Aluminum Wires



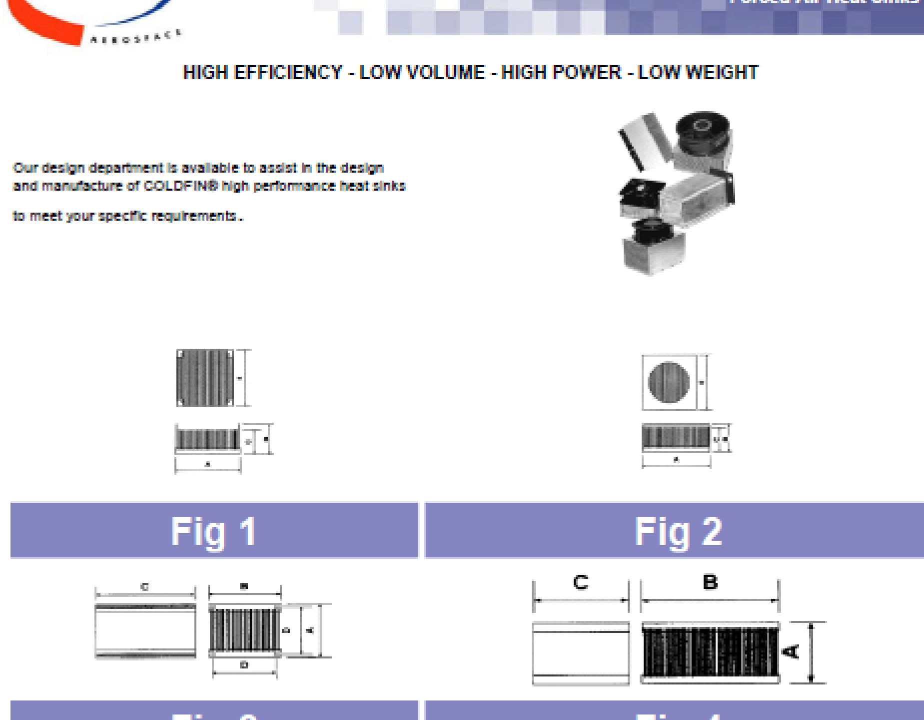


Electrical Properties of Fine Aluminum Wires





6. COLDFIN® high performance heat sinks, CF2-0816-0805-1500A datasheet



Catalog Number	fig.	dim'n A	dim'n B	dim'n C	dim'n D	dim'n E	Weight (Kg)	Thermal Resistance
CF1-0816-0375-0816A	1	81.6	40.75	37.5	71.5	81.6	0.4	0.20° C/Watt *
CF1-1250-0470-1250A	1	125.0	51.5	47.0	113.5	125.0	1.1	0.07° C/Watt **
CF1-1500-1250-2000A	2	153.0	130.0	125.0	–	200.0	4.7	0.05° C/Watt †
CF1-2500-1250-2500A	2	253.0	130.0	125.0	–	250.0	9.44	0.03° C/Watt ††
CF2-0816-0805-1000A	3	80.5	81.6	100.0	71.5	–	1.01	0.15° C/Watt *
CF2-0816-0805-1500A	3	80.5	81.6	150.0	71.5	–	1.52	0.13° C/Watt *
CF2-2500-1200-1250A	4	120.0	250.0	125.0	–	–	5.0	0.05° C/Watt ‡

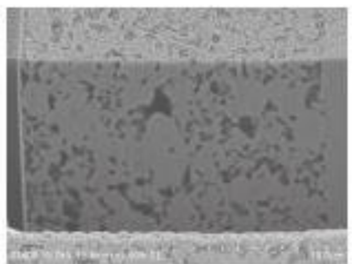
Notes:
1) Base plates are nominal 12 mm thick.
2) If heat sinks shown in fig.2 are required without the fan cowling then the overall width should be reduced by 3 mm.

Test results were obtained using the fans listed below:

HS MARSTON AEROSPACE LTD, WOBASTON ROAD, FORDHOUSES, WOLVERHAMPTON, WV10 6QJ
TEL: +44 (0)1902 623500   FAX: + 44 (0)1902 623519

7. Kyocera CT2700 Silver sintering paste

Pressure-less Silver Sintering Paste

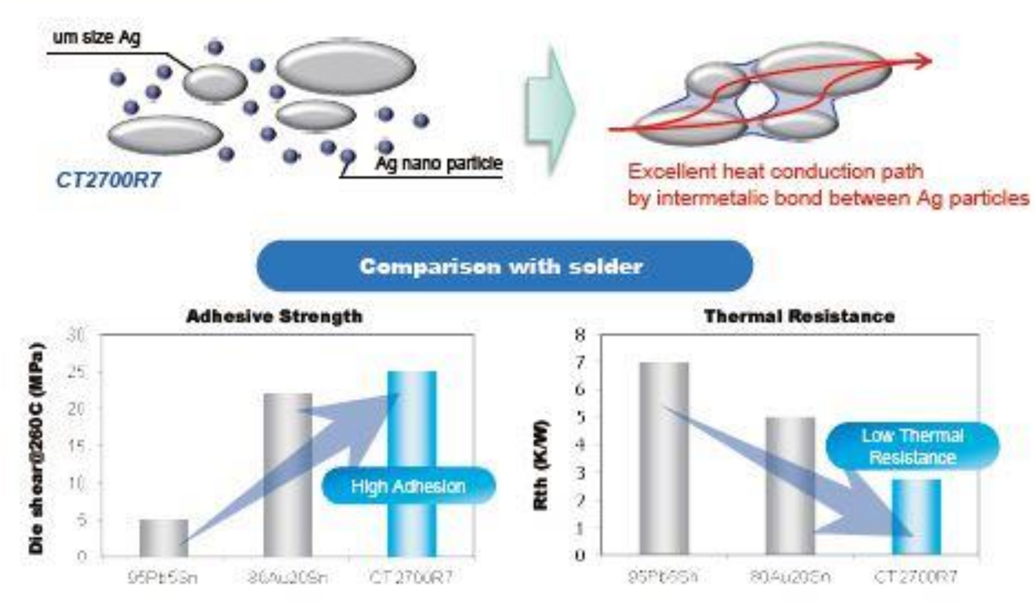


Recently, power devices such as IGBTs, LED power and automotive modules need more strict critical quality and are reaching their performance limit with resin-based DA pastes, so a new solution is needed to overcome technical hurdles. In addition, for environmental and health endangerment from lead, the semiconductor industry is making every effort to eliminate high-lead solder, when feasible. However, even now there is no single identified lead-free solution for all applications. The unique properties, such as the high melting point and thermal conductivity of these high-lead alloys are necessary for the level of reliability required for these products. Therefore, in order to achieve their requirement, we have developed pressure-less silver sintering paste based on nano-Ag technology. Our paste demonstrates a thermal conductivity of more than 200W/mK and excellent die shear adhesion to bare Cu as well as noble plating like gold and silver. Moreover, this paste shows excellent interface reliability in not only general automotive requirements but also in SiC applications with high Tj by adoption of an original resin dispersion system.

Pressure-less Silver Sintering Paste

Name	Viscosity (Pa·s)	Elastic modulus (GPa)	Thermal conductivity (W/m·k)	Volume Resistivity (Ω·cm)	Adhesive strength (N/4mm^2)		Cure condition (Nitrogen)	Applied chip size	Characteristic
					25℃	260℃			
CT2700R6	60	17.6	200	6x10^{4}	>400	>400	200deg.Cx1.5h (250deg.Cx1.5h)	2 ~ 6mm^2	Standard High thermal conductivity
CT2700R7	55	26.2	200	4x10^{4}	>400	>400	200deg.Cx1.5h (250deg.Cx1.5h)	1 ~ 10mm^2	For Bare Cu application Excellent interface reliability
CT2700R7S	100	21.6	200	4x10^{4}	>400	>400	200deg.Cx1.5h (250deg.Cx1.5h)	0.3 ~ 12mm^2	Printable Wide die size window

Sintering Mechanism



8. Normally-OFF Silicon Carbide Junction Transistor," GA10JT12-CAL datasheet

GeneSiC SEMICONDUCTOR — **Die Datasheet** — **GA10JT12-CAL**

Normally – OFF Silicon Carbide Junction Transistor

V_{DS}	=	1200 V
$R_{DS(ON)}$	=	100 mΩ
I_D @ 25 °C	=	25 A
h_{FE}	=	80

Features

- 210 °C Maximum Operating Temperature
- Gate Oxide Free SiC Switch
- Exceptional Safe Operating Area
- Excellent Gain Linearity
- Temperature Independent Switching Performance
- Low Output Capacitance
- Positive Temperature Coefficient of $R_{DS,ON}$
- Suitable for Connecting an Anti-parallel Diode

G D S

Die Size = 2.10 mm x 2.10 mm

Advantages

- Compatible with Si MOSFET/IGBT Gate Drive ICs
- > 20 µs Short-Circuit Withstand Capability
- Lowest-in-class Conduction Losses
- High Circuit Efficiency
- Minimal Input Signal Distortion
- High Amplifier Bandwidth

Applications

- Down Hole Oil Drilling, Geothermal Instrumentation
- Hybrid Electric Vehicles (HEV)
- Solar Inverters
- Switched-Mode Power Supply (SMPS)
- Power Factor Correction (PFC)
- Induction Heating
- Uninterruptible Power Supply (UPS)
- Motor Drives

Table of Contents

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Section II: Static Electrical Characteristics 2
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Section VI: Mechanical Parameters 10
Section VII: Chip Dimensions 10
Section VIII: SPICE Model Parameters 12

Section I: Absolute Maximum Ratings

(T_C = 25 °C unless otherwise specified)

Parameter	Symbol	Conditions	Value	Unit	Notes
Drain – Source Voltage	V_{DS}	V_{GS} = 0 V	1200	V	
Continuous Drain Current	I_D	T_C = 25°C	25	A	
Continuous Drain Current	I_D	T_C > 125°C, assumes R_{thJC} < 0.88 °C/W	10	A	
Continuous Gate Current	I_G		1.3	A	
Turn-Off Safe Operating Area	RBSOA	T_{VJ} = 210 °C, Clamped Inductive Load	$I_{D,max}$ = 10 @ $V_{DS} \le V_{DSmax}$	A	Fig. 16
Short Circuit Safe Operating Area	SCSOA	T_{VJ} = 210 °C, I_G = 1 A, V_{DS} = 800 V, Non Repetitive	>20	µs	
Reverse Gate – Source Voltage	V_{SG}		30	V	
Reverse Drain – Source Voltage	V_{SD}		25	V	
Operating Junction and Storage Temperature	T_j, T_{stg}		-55 to 210	°C	
Maximum Processing Temperature	T_{Proc}	10 min. maximum	325	°C	

Section II: Static Electrical Characteristics

Parameter	Symbol	Conditions	Value Min.	Value Typical	Value Max.	Unit	Notes
A: On State							
Drain – Source On Resistance	$R_{DS(ON)}$	I_D = 10 A, T_j = 25 °C I_D = 10 A, T_j = 150 °C I_D = 10 A, T_j = 175 °C		100 160 180		mΩ	Fig. 4
Gate – Source Saturation Voltage	$V_{GS,SAT}$	I_D = 10 A, I_D/I_G = 40, T_j = 25 °C I_D = 10 A, I_D/I_G = 30, T_j = 175 °C		3.50 3.27		V	Fig. 7
DC Current Gain	h_{FE}	V_{DS} = 8 V, I_D = 10 A, T_j = 25 °C V_{DS} = 8 V, I_D = 10 A, T_j = 125 °C V_{DS} = 8 V, I_D = 10 A, T_j = 175 °C		80 55 50		–	Fig. 5
B: Off State							
Drain Leakage Current	I_{DSS}	V_{DS} = 1200 V, V_{GS} = 0 V, T_j = 25 °C V_{DS} = 1200 V, V_{GS} = 0 V, T_j = 150 °C V_{DS} = 1200 V, V_{GS} = 0 V, T_j = 175 °C		1 1 2		μA	Fig. 8
Gate Leakage Current	I_{SG}	V_{SG} = 20 V, T_j = 25 °C		20		nA	

Section III: Dynamic Electrical Characteristics

Parameter	Symbol	Conditions	Value Min.	Value Typical	Value Max.	Unit	Notes
A: Capacitance and Gate Charge							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 800 V, f = 1 MHz		1275		pF	Fig. 9
Reverse Transfer/Output Capacitance	C_{rss}/C_{oss}	V_{DS} = 800 V, f = 1 MHz		30		pF	Fig. 9
Output Capacitance Stored Energy	E_{OSS}	V_{GS} = 0 V, V_{DS} = 800 V, f = 1 MHz		12		μJ	Fig. 10
Effective Output Capacitance, time related	$C_{o(tr)}$	I_D = constant, V_{GS} = 0 V, V_{DS} = 0…800 V		55		pF	
Effective Output Capacitance, energy related	$C_{o(er)}$	V_{GS} = 0 V, V_{DS} = 0…800 V		40		pF	
Gate-Source Charge	Q_{GS}	V_{GS} = -5…3 V		11		nC	
Gate-Drain Charge	Q_{GD}	V_{GS} = 0 V, V_{DS} = 0…800 V		55		nC	
Gate Charge - Total	Q_g			66		nC	
B: Switching[1]							
Internal Gate Resistance – ON	$R_{G(INT-ON)}$	V_{GS} > 2.5 V, V_{DS} = 0 V, T_j = 175 °C		0.19		Ω	
Turn On Delay Time	$t_{d(on)}$	T_j = 25 °C, V_{DS} = 800 V, I_D = 10 A, Resistive Load Refer to Section V for additional driving information.		10		ns	
Fall Time, V_{DS}	t_f			10		ns	Fig. 11, 13
Turn Off Delay Time	$t_{d(off)}$			22		ns	
Rise Time, V_{DS}	t_r			10		ns	Fig. 12, 14
Turn On Delay Time	$t_{d(on)}$	T_j = 175 °C, V_{DS} = 800 V, I_D = 10 A, Resistive Load		10		ns	
Fall Time, V_{DS}	t_f			10		ns	Fig. 11
Turn Off Delay Time	$t_{d(off)}$			35		ns	
Rise Time, V_{DS}	t_r			10		ns	Fig. 12
Turn-On Energy Per Pulse	E_{on}	T_j = 25 °C, V_{DS} = 800 V, I_D = 10 A, Inductive Load Refer to Section V.		140		μJ	Fig. 11, 13
Turn-Off Energy Per Pulse	E_{off}			10		μJ	Fig. 12, 14
Total Switching Energy	E_{ts}			150		μJ	
Turn-On Energy Per Pulse	E_{on}	T_j = 175 °C, V_{DS} = 800 V, I_D = 10 A, Inductive Load		140		μJ	Fig. 11
Turn-Off Energy Per Pulse	E_{off}			100		μJ	Fig. 12
Total Switching Energy	E_{ts}			150		μJ	

[1] – All times are relative to the Drain-Source Voltage V_{DS}

Section IV: Figures

A: Static Characteristics

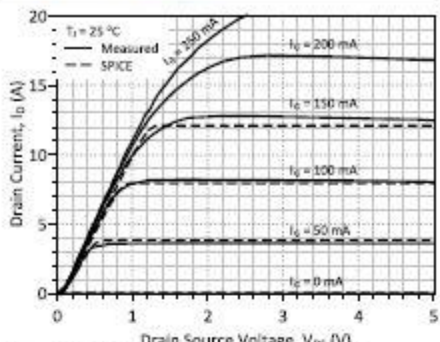


Figure 1: Typical Output Characteristics at 25 °C

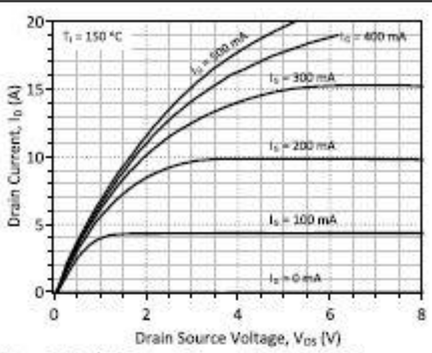


Figure 2: Typical Output Characteristics at 150 °C

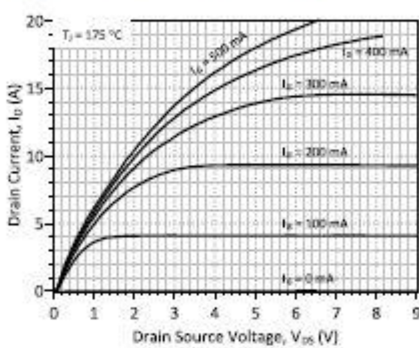


Figure 3: Typical Output Characteristics at 175 °C

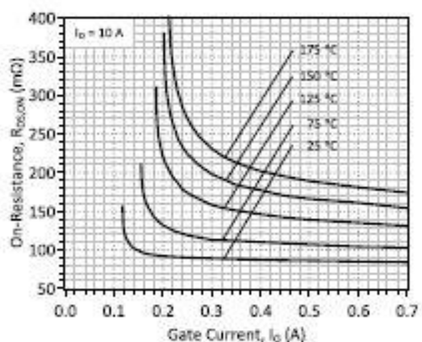


Figure 4: On-Resistance vs. Gate Current

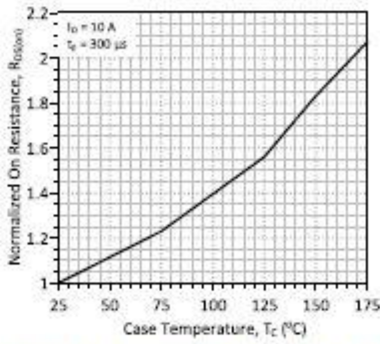


Figure 5: Normalized On-Resistance vs. Temperature

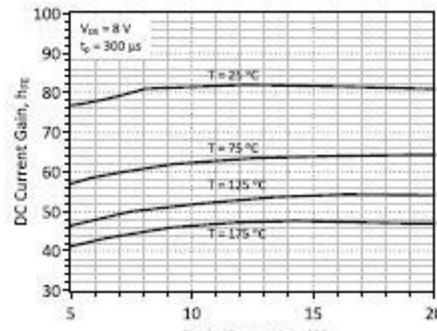


Figure 6: DC Current Gain vs. Drain Current

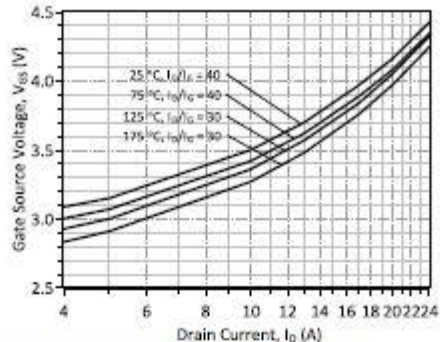


Figure 7: Typical Gate – Source Saturation Voltage

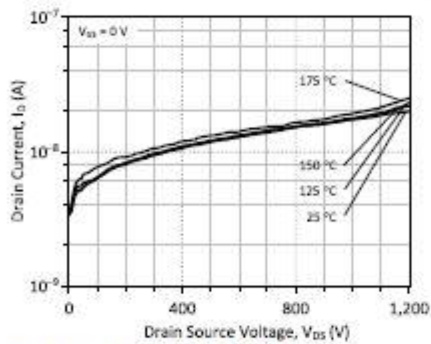


Figure 8: Typical Blocking Characteristics

B: Dynamic Characteristics

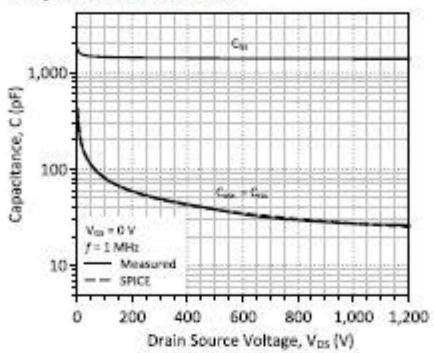


Figure 9: Input, Output, and Reverse Transfer Capacitance

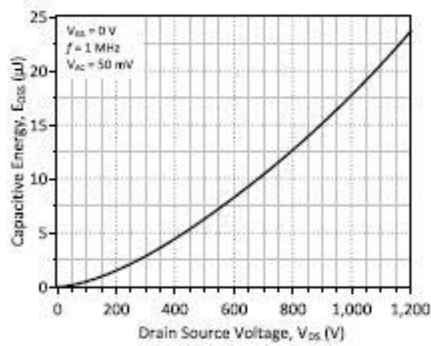


Figure 10: Energy Stored in Output Capacitance

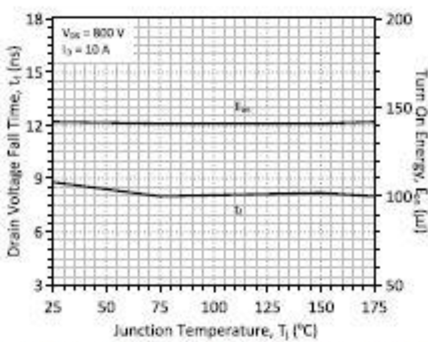


Figure 11: Typical Switching Times and Turn On Energy Losses vs. Temperature

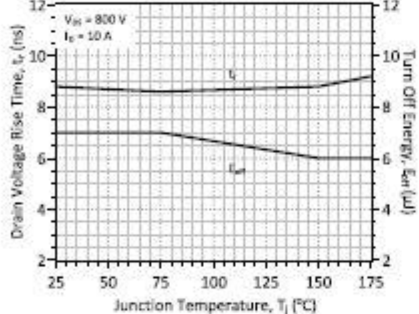


Figure 12: Typical Switching Times and Turn Off Energy Losses vs. Temperature

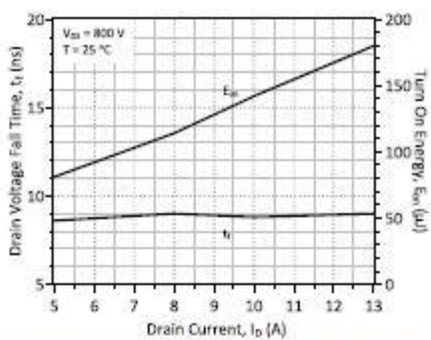


Figure 13: Typical Switching Times and Turn On Energy Losses vs. Drain Current

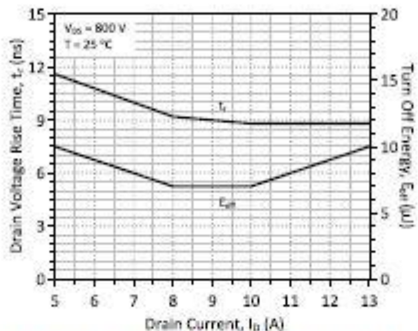


Figure 14: Typical Switching Times and Turn Off Energy Losses vs. Drain Current

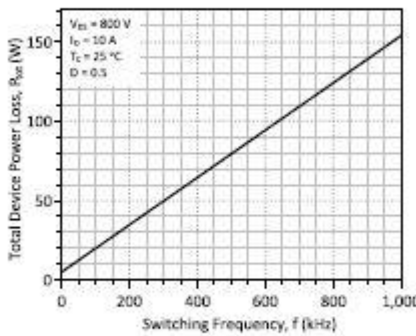


Figure 15: Typical Hard Switched Device Power Loss vs. Switching Frequency [3]

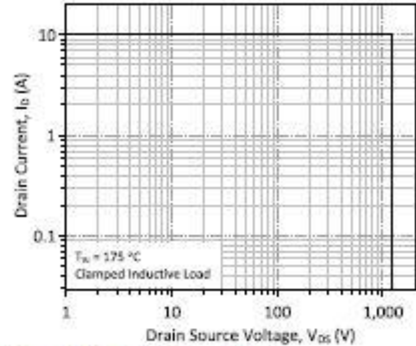


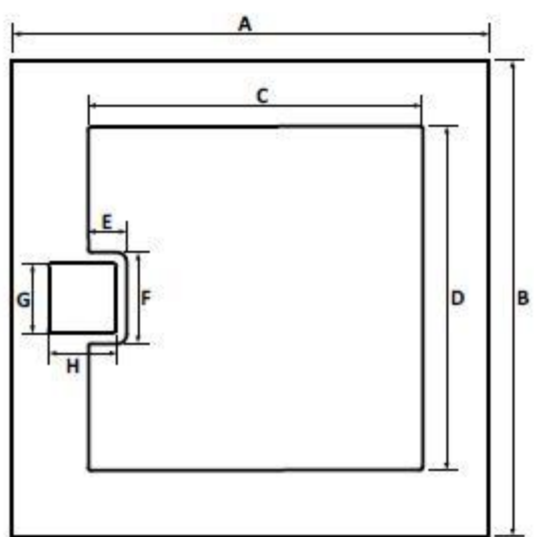
Figure 16: Turn-Off Safe Operating Area

[3] – Representative values based on device conduction and switching loss. Actual losses will depend on gate drive conditions, device load, and circuit topology.

Section VI: Mechanical Parameters

Die Dimensions	2.10 x 2.10	mm²	83 x 83	mil²
Die Area total / active	4.41/3.31	mm²	6836/5134	mil²
Die Thickness	360	µm	14	mil
Wafer Size	100	mm	3937	mil
Flat Position	0	deg	0	deg
Die Frontside Passivation	Polyimide			
Gate/Source Pad Metallization	4000 nm Al			
Bottom Drain Pad Metallization	400 nm Ni + 200 nm Au			
Die Attach	Electrically conductive glue or solder			
Wire Bond	Al ≤ 10 mil (Source) Al ≤ 3 mil (Gate)			
Reject ink dot size	Φ ≥ 0.3 mm			
Recommended storage environment	Store in original container, in dry nitrogen, < 6 months at an ambient temperature of 23 °C			

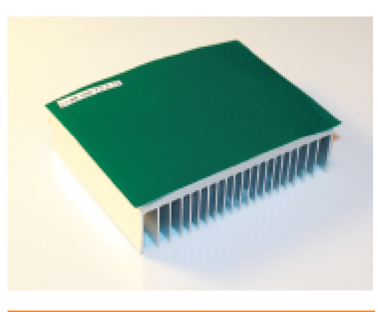
Section VII: Chip Dimensions



		mm	mil
DIE	A	2.10	83
	B	2.10	83
SOURCE WIREBONDABLE	C	1.47	58
	D	1.52	60
	E	0.17	7
	F	0.40	16
GATE WIREBONDABLE	G	0.30	12
	H	0.30	12

9. Thermal interface material Li-98

Li-98
Thermal Tape



Features

Good adhesion
Very good thermal conductivity
Highly compressible
Easy to assemble

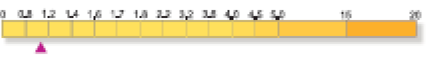
Applications

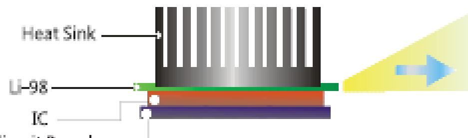
Electronic components: IC / CPU / MOS
LED / M/B / P/S / Heat Sink / LCD-TV / Notebook PC / PC / Telecom Device / Wireless Hub etc....
DDR II Module / DVD Applications / Hand-Set applications etc...

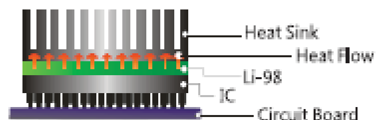
Properties

REACH Compliant
RoHS Compliant

Thermal Conductivity: 0.95 W/mK
(W/mK - Z Axis)







Property	Li-98		Li-98C	Li98CN	Unit	Test Method
Thickness	0.15	0.25	0.2	0.18		ASTM D374
Colour	White	White	White	White		Visual
Reinforcement Carrier	Fibreglass mesh					
Density	1.85	1.85	1.9	1.8	g/cm^3	ASTM D792
Tensile Strength	200	400	200	50	psi	ASTM D412
Glass Transition Temperature	-30	-30	-27	-30	°C	
Short Time Use Temperature (30sec)	200	200	200	200	°C	
Continuous Working Temperature	-30 to 120	-30 to 120	-30 to 120	-30 to 120	°C	
Thermal Conductivity	0.95	0.95	1.8	2	W/mK	ASTM D5470
Thermal Impedance @ <1psi	1.0	1.8	0.7	0.6	C in 2/W	ASTM D5470
Thermal Impedance @ 50psi	0.9	1.5	0.5	0.3	C in 2/W	ASTM D5470
Initial Tack	11	10	14	15	cm	PSTC-6
Lap Shear Strength	61	61	65	55	N/cm^2	ASTM D1002
Die Shear Strength @ 25 °C	120	120	118	100	N/cm^2	-
Die Shear Strength @ 80 °C	69	69	68	55	N/cm^2	-
Holding Power 1000g @ 25 °C using 1 in^2	>10000	>10000	>10000	>10000	min	PSTC-7
Holding Power 1000g @ 80 °C using 1 in^2	>10000	>10000	>10000	>10000	min	PSTC-7
180° Peeling Strength (aluminium)	4	5	4	3	N/cm	ASTM D3330
Dielectric Breakdown Voltage (Vac)	>2	>3	>3	>5	kV	ASTM D149
Dielectric Breakdown Voltage (Vdc)	>3	>4	>4	>6	kV	ASTM D149

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10. Polarization super junction a new concept for GaN high voltage devices

http://www.powdec.co.jp/business/tutorial/file/IWWPE2012%20powdec%20slide.pdf

Polarization Super-junction

A New Concept for GaN High-Voltage Devices

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-- Discussion --

◆ Comparison of on-resistance