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Characterisation of charge carrier defects in high-dielectric-metal-gate and thin film transistor devices

by

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Abstract

Metal oxide semiconductor (MOS) transistors find application either as a switch or amplifier in high and low power electronic devices. In both sectors, devices rely on the availability of a good insulator layer for achieving desirable performance. The traditional CMOS transistors with Silicon (Si) semiconductor and SiO_2 gate insulator has reached its limits with regards to supporting the need for faster and smaller devices. In low power CMOS technology high-dielectric (high-*k*) materials are being used to replace SiO_2 insulator to minimise gate leakage current that arises as a result of device scaling. Another emerging field of application of electronic devices is the field of flat panel displays that aims to make use of transparent thin film MOS transistors. Alternate materials to amorphous silicon (a-Si:H) and poly-silicon (poly-Si) are being researched, to fabricate thin film transistors (TFTs), in favour of traditional materials that have limited optical transparency and mobility. Again, these TFTs are surely in need of good insulators to achieve stable operation against threshold voltage shifts. Performance of MOS transistors is highly dependent on the density of defects in the device. Defects in a transistor could be due to the inherent charge traps in the device materials or the traps formed during fabrication. These charge traps can affect the performance of a transistor such as causing shift in threshold voltage and degrading device mobility and also affect the reliability and stability of the device. Hence it becomes necessary to determine the cause, quantity and impact of defects so that better materials and/or better fabrication processes could be devised to obtain efficient devices.

In this work the aim is to investigate the different defects/traps that impact MOS transistors employed in CMOS and transparent TFT technologies and also to study the impact of these defects on device mobility. Electrical current and capacitance measurements are carried out along with analytical modelling to quantify and understand the nature of the defects in the devices. Charge trap generation and distribution due to post-metallisation annealing of HfO_2 based MOS transistor is studied. The density of defects in a ZnO based TFT with Ta_2O_5 gate insulator is also investigated in this study.

List of Figures and Tables

List of Acronyms/Abbreviations

CMOS	Complementary Metal oxide semiconductor
a-Si:H	Hydrogenated amorphous silicon
TTFT	Transparent thin film transistor
ZnO	Zinc Oxide
HfO_2	Hafnium dioxide
Ta_2O_5	Tantalum pentoxide
MOSFET	Metal oxide semiconductor field effect transistor
PMA	Post metallisation anneal
CV	Capacitance-Voltage
CP	Charge pumping
EOT	Equivalent oxide thickness
FGR	Fermi golden rule
BTE	Boltzmann transport equation
RTA	Relaxation time approach
TCO	Transparent conductive oxide
IGZO	Indium Gallium Zinc Oxide
ITO	Indium tin oxide
RTN	Random telegraph noise
LFN	Low frequency noise
SILC	Stress induced leakage current
HKMG	High *k (dielectric constant/permittivity)* metal gate
EWF	Effective work function
IPE	Internal photoemission

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Chapter 1

Introduction

1.1 Motivation and background of the thesis

Silicon has been the most widely used material in the semiconductor industry. Silicon has good physical, electrical and optical properties, forms a stable oxide and is widely available and cost effective compared to other semiconductor materials. Since its invention in the 1960s, MOSFETs (Metal Oxide Semiconductor Field Effect Transistors) have found widespread application in high and low power electronic devices, particularly as a key component in ICs (Integrated circuits). Traditionally, MOS transistors for low power application such as in CMOS technology have been made on Si substrates with SiO_2 as gate insulator. The need to have smaller, faster, less power consuming ICs has resulted in the size of the MOS transistors decreasing over time. This trend has been termed as Moore's law, an observation put forward by Gordon Moore, that the density of devices on IC chips will double every two years [1] [2]. With MOS technology nodes now being scaled beyond 45nm, the thickness of the gate insulator needs to be only about 1nm. At such thickness, the possibility of high leakage current through the SiO_2 insulator layer is high due to quantum tunneling. An ideal MOS transistor would have high on-current at low operating voltages which can be achieved with high gate capacitance. One alternative to achieve high gate capacitance without decreasing insulator thickness is by using materials with a high dielectric constant (*k*).Among the many materials considered for gate insulator for CMOS transistors, Hafnium dioxide (HfO_2) has emerged as a suitable high-*k* dielectric candidate. In 2007, Intel manufactured the first high-*k* based MOS transistor with HfO_2 gate insulator [3].

One other technology being considered in this study is that of transparent thin film transistors (TTFT), which find application in flat panel displays. Thin film transistor technology was also introduced around the same time as the MOSFETs. Although first demonstrated in 1973 [4], popularity of TFTs as potential candidates with application in display technology industry only grew after the invention of hydrogenated amorphous Silicon (a-Si:H) in 1979 [5]. Even though a-Si:H was widely researched and put into production of flat panel displays, it suffered from low mobility and less transparency. Advanced research into materials and fabrication processes of TFTs has resulted in semiconductor materials, gate oxide and electrodes with high optical transparency in the visible region of electromagnetic spectrum and thus making 'transparent electronics' a reality. Conductive oxide semiconductors such as IGZO (Indium-Gallium-Zinc

Oxide) and ZnO are the most widely researched active layer materials for TTFTs. Similar to that in MOSFETs, high-*k* dielectric gate insulators are the preferred choice for TFTs as well [6-9]. Insulators such as SiO_2 can be used on TFTs but for TTFT technology the processing temperature is very low (<150℃) and fabrication of good quality SiO_2 is not possible at such low temperature. Also, to obtain a good gate capacitance, to ensure a TFT with low operating voltage and less leakage current, high-*k* materials are the preferred choice for gate insulator.

In conventional MOS devices, with the natural oxide layer of Si, i.e.SiO_2, grown on Si substrate, the semiconductor/oxide interface layer and bulk oxide is of good quality and can be considered electrically neutral. No gate interface and gate oxide is electrically neutral in reality because of charge traps at the interface and/or mobile ionic charges and oxide charges in the oxide bulk. The newer semiconductor materials and high-*k* insulators exhibit higher density of interface and oxide defects. Charge defects in a device are generated due to inherent impurities of the material or due to the fabrication processes. These defects cause mobility degradation, threshold voltage shifts, gate leakage and other issues related to device performance and reliability. This study aims to extract the quantity and distribution of defects in high-*k* MOSFETs and ZnO TFTs.

1.2 Organisation of the thesis

Further to the brief introduction, Chapter 2 gives more details on the basics of the structure and operation related to MOSFETs and TFTs. Quantum Mechanical effects in MOS devices and the physics behind scattering and its influence on device mobility are reviewed. The conduction mechanism in oxide semiconductors and the importance of DOS calculation is also presented. In Chapter 3, the study carried out so far to characterize the charge defect density and its influence on device mobility due to two different fabrication processes of high-*k* metal gate MOS transistors is presented. In Chapter 4, electrical performance characteristics of bottom-gated pC-ZnO TFT, fabricated at the University of Sheffield is studied. Field effect methods to calculate the DOS profile in the transistor is also presented. Chapter 5 concludes this thesis with the indications on further experimental work and analysis.

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Chapter 2

Technical Background and Literature Review

2.1 Introduction to device structure

Fig.2.1 shows a generic schematic of a MOSFET (Metal Oxide Semiconductor Field Effect Transistor) and a bottom-gated TFT (thin film transistor) respectively. A MOS structure forms the basis of both MOSFETs and TFTs. The basic structure of a MOS or in general a MIS (Metal Insulator Semiconductor) device technology is a semiconductor substrate and a metal electrode separated by an insulating layer (an oxide in the case of MOS). MOSFETs, although a four terminal device with source (S), drain (D), gate and substrate terminals, are considered as three terminal devices with a grounded substrate terminal. TFTs are three terminal devices with gate, source (S) and drain (D) terminals. MOSFETs and TFTs are field effect devices where the conduction i.e. flow of charge carriers, is controlled by the electric field, resulting from the externally applied gate bias, near the semiconductor-insulator interface.

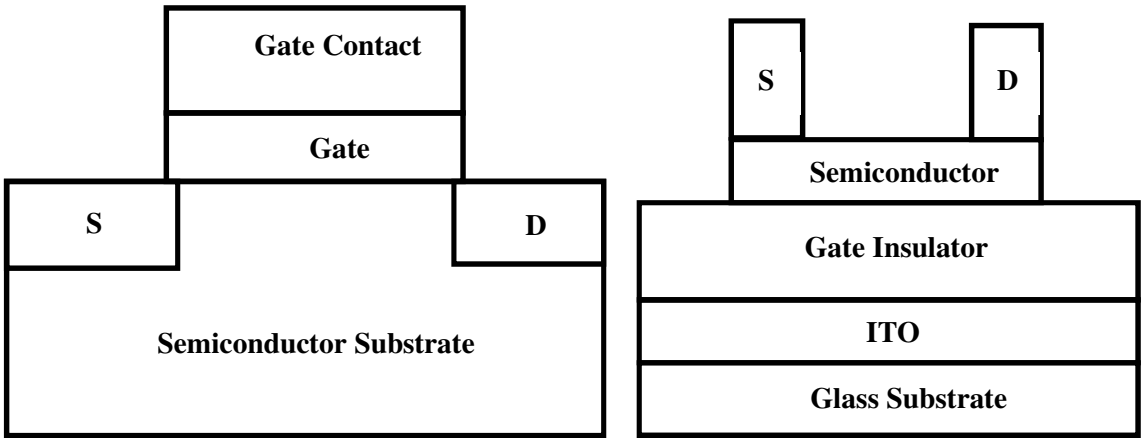

Figure 2.1: Schematic of (a) MOSFET and (b) bottom gated TFT.

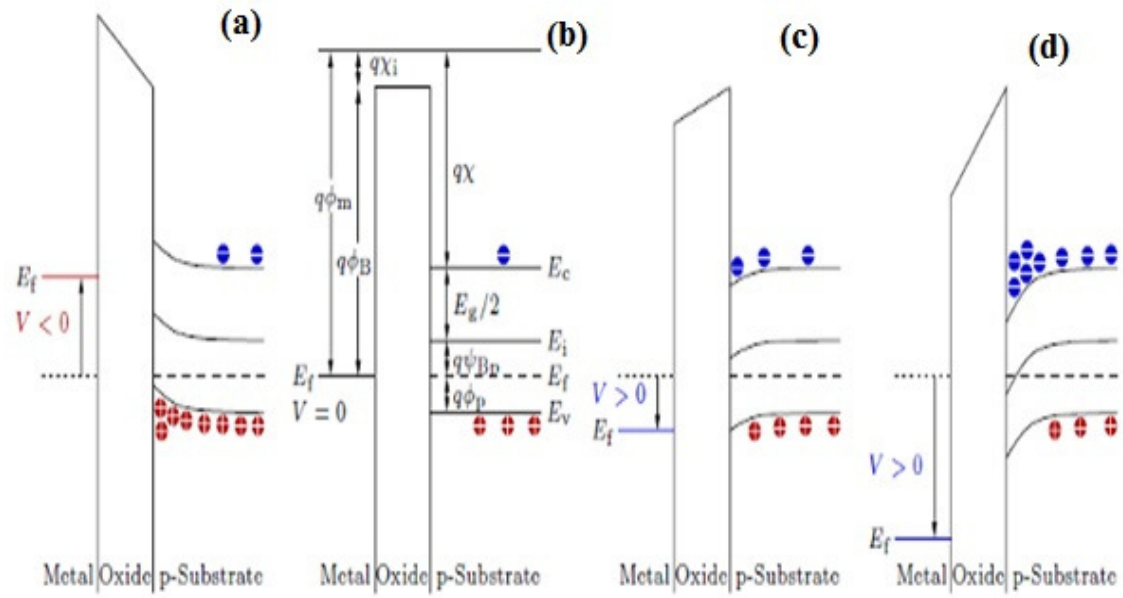

Figure 2.2: Schematic energy diagram of an ideal MOS structure showing the band bending in the substrate under ideal conditions (a) in accumulation (b) flat band (c) depletion (d) inversion conditions [taken from [1]].

Working regimes of an ideal MOS device, illustrated in Fig.2.2, is explained here considering a simpler MOS capacitor with p-type substrate. The operating conditions of a MOS structure depends on the applied voltage ***V*** on the metal contact with respect to the Fermi level (i.e. electron energy) of the grounded semiconductor. Under ideal conditions, (i) the semiconductor is considered to be uniformly doped (ii) the oxide is free of charges i.e. under all bias conditions no current flows through the oxide layer and thus the resistivity of the oxide layer is infinite (iii) work function difference between the metal and the semiconductor (ϕ_{ms}) is zero i.e. the Fermi levels of the metal and semiconductor substrate are in alignment. The term E_C represents the energy at the bottom of the conduction band, E_V stands for the energy at the top of the valence band and E_i is the intrinsic energy level. The Fermi level, E_f , of the semiconductor depends on the doping of the substrate.

1) Under no applied voltage, the Fermi levels of the metal and semiconductor are at the same level and the energy bands throughout the substrate is flat. This is termed as the **flat band** condition. With no applied voltage no field exists in the oxide and the substrate and the charge carrier concentration in the substrate is in equilibrium.

2) Consider a negative voltage **V** applied to the gate. This potential increase the Fermi level of the metal with respect to the Fermi level of the substrate and induces an electric field across the

oxide layer. The induced electric field attract the positively charged holes from the interior of the substrate towards the substrate/oxide interface while electrons are repelled away from the interface into the semiconductor bulk. This accumulation of holes near the interface causes band bending and the valence band edge in the substrate moves closer to the Fermi level. The device is then said to operate in **accumulation** region. The potential at the substrate surface is termed as surface potential.

3) Similarly, if a positive voltage is applied at the gate, an electric field is induced at the substrate surface through the oxide which attracts electrons towards the interface. This field causes the bands near the substrate surface to bend downwards. The valence band near the surface moves away from the Fermi level because of the surface getting depleted of majority carriers, here, holes. This is known as **depletion** condition. Due to depletion the net charge at the surface is negative because of the acceptor ions.

4) Increasing the gate voltage further, more electrons get accumulated at the interface increasing the band bending and the negative charge at the region. At some very high applied voltage, the intrinsic potential band near the surface bends below the Fermi potential. At this condition the surface region is fully depleted of holes and has a high concentration of minority carriers i.e. electrons. This condition is called **inversion**. The negative charge at the surface, in inversion, consists of ionized acceptor ions and thermally generated electrons.

In a MOSFET, the heavily doped source and drain regions act as reservoir of charge carriers. Under sufficiently high positive gate voltage, the *p*-type semiconductor region near the insulator gets populated by electrons, forming a conduction channel between the source and drain regions and thus initiating current flow.

Although optional, TFTs generally do not have source and drain implants. Consider a TFT with *n*-type semiconductor and zero gate-electrode-semiconductor work function difference. When a positive voltage is applied at the gate, majority carriers i.e. electrons, accumulate at the semiconductor-insulator interface forming a conduction channel. Now if a positive voltage is applied at the drain terminal, an electric current is established in the semiconductor from source (S) to drain (D) terminals corresponding to the 'on-state' of the TFT. Now if a negative potential is applied at the gate, regardless of the drain terminal potential, a very low drain current will flow in the device which corresponds to the 'off-state' of the TFT. Since the constituent materials of TFTs have large band gap compared to the conventional Si based transistors, a high surface potential is needed to form a conduction channel of minority carriers and hence inversion region is not generally achieved in TFTs.

2.2 Poisson's Equation

As discussed above, applying an external voltage at the gate terminal of the MOS structure induces an electric field across the oxide layer at the substrate surface. This electric field causes band bending and increased carrier concentration at the surface. The relation between the electric field, surface potential and charge density at the surface can be understood using Poisson's equation. Poisson equation relates the electrostatic potential (**Φ**) to the charge density (**ρ**).

Consider 'x' as the distance measured along the depth of the semiconductor from the semiconductor/oxide interface, the extent of band bending, $\phi(x)$ at position x can be expressed [2] as

$$\phi(x) = \phi_i(x) - \phi_i(x = \infty) \quad \text{..... (2.1)}$$

where $\phi_i(x)$ is the electrostatic potential and is equal to the surface potential, ϕ_S, at the semiconductor/oxide interface and zero in the bulk of the semiconductor. If E is the electric field at the surface due to the applied gate voltage (V_g), $\phi(x)$ is the electrostatic potential at a position x (in eV) and $\rho(x)$ is the carrier density per unit volume at x, then the Poisson relation can be expressed as

$$d^2\phi(x)/dx^2 = -dE/dx = -\rho(x)/\varepsilon_s \quad \text{..... (2.2)}$$

where ε_S is the permittivity of the substrate and q is charge of electron. The charge density $\rho(x)$ (in m^{-3}) is the sum of the ionized acceptors (N_a) and donors (N_d) and of charge carriers concentration ***n*** and ***p*** for electrons and holes respectively in the space charge region and can be written as

$$\rho(x) = q\left[p(x) - n(x) + N_d - N_a\right] \quad \text{..... (2.3)}$$

Thus Eqn. (2.2) becomes

$$d^2\phi(x)/dx^2 = -(q/\varepsilon_s)\left[p(x) - n(x) + N_d - N_a\right] \quad \text{..... (2.4)}$$

Integrating the total charge density in the substrate, from the bulk towards the surface, gives the electric field (E) which is related to the total charge density per unit area (Q_S) of the semiconductor by Gauss's law as:

$$E = \int (1/\varepsilon_S)\rho(x)\,dx = Q_S/\varepsilon_S \quad \text{..... (2.5)}$$

From Eqn. (2.5) the total charge in the semiconductor substrate can be expressed as:

$$Q_s = \int q\left[p(x) - n(x) + N_d - N_a \right] dx \qquad \text{..... (2.6)}$$

From Eqn. (2.6) and Eqn. (2.4) relation between surface potential (ϕ_S) and total charge in the substrate can be established. By numerically solving the above equation, the variation of charge density along the substrate with respect to the variation in surface potential which in turn, is related to the electric field due to the external applied voltage at the gate, can be calculated.

The relation between the voltage applied at the gate terminal (V_g) and the resulting surface potential can be expressed as

$$V_g = \phi_s + V_{ox} = Q_s / C_{ox} + \phi_s \qquad \text{..... (2.7)}$$

where V_{ox} is the potential drop across the oxide layer and C_{ox} is the capacitance per unit area of the oxide layer.

2.3 Quantum Mechanics

Along with the wave function, each electron has a wave vector (k) associated with it. The wave vector (k) of an electron is defined in reciprocal lattice. The relation between the energy $E(k)$ and k in the k-space or momentum space is termed the energy dispersion relation. This relation reveals information about the band structure of materials.

When two atoms interact the energy levels of the atoms split into several discrete energy bands. The higher energy level split into two separate bands of energies. The upper energy band, termed as conduction band, is mostly partly filled meaning, some of the energy states of the band is occupied by very few electrons with high energy level whereas the lower energy band, termed the **valence band**, is mostly filled. The separation between the two allowed energy bands i.e. the conduction and valence bands, is known as forbidden gap or forbidden band. The forbidden gap represents the energy states that cannot be occupied by electrons. The energy gap $(E_g \ in \ eV)$ in a solid is measured as difference in energy between the lower edge of conduction band (E_c) and upper edge of valence band (E_v) i.e. $E_g = E_c - E_v$

Electrons that occupy the conduction band are called free electrons and they define the conductivity of a solid. Through thermal excitation, for example, applying an electric field, it is possible to increase the energy level of electrons in the valence band to overcome the energy gap and move in to the conduction band. The number of electrons moving into the conduction band

depends on the availability of empty energy states in the band. When a valence electron gains energy and moves into conduction band, a vacancy, termed as a hole is created in the valence band. Holes are considered positively charged and movement of holes in a crystal is in opposite direction to that of electrons.

The band gap of a solid can be used to categorise a material as metal, insulator or semiconductor. At absolute zero temperature (0K), Metals usually have overlapping or partially filled energy bands meaning availability of free electrons and ease of excitation of valence electrons. This abundance of free electrons makes metals good conductors. In insulators, the conduction band is empty and the valence band is completely filled with electrons. The band gap in insulators is very large and the absence of electrons in the conduction band makes conduction impossible in insulators. The energy states in semiconductors at absolute zero is the same as that in insulators but energy gap in semiconductors is less than that in insulators. This makes it possible to excite electrons into the conduction band and makes conduction possible in semiconductors.

The structure of the conduction and the valence band, as well as the band gap energy is fundamental to the electronic properties of a semiconductor material. The band structure and effective mass of a solid are defined in reciprocal lattice explained with respect to Brillouin zone (BZ). Kittel [3] defines the first Brillouin zone as "the smallest volume entirely enclosed by planes that are the perpendicular bisectors of the reciprocal lattice vectors drawn from the origin". Brillouin zones form an essential part of the electron energy-band structure analysis of crystals. Band structure explains various properties of materials such as conductivity, electrical resistivity, and optical absorption.

Quantum mechanics treats materials at the microscopic level to be made up of atoms. Atomic level treatment of solids help to explain many electrical and optical properties of the solids such as transport mechanism which is primarily governed by the movement of valence electrons associated with the atoms. The charge carriers in a system (here, electrons) are experimentally known to occupy only certain energy states. The behaviour of electrons under the influence of potential energy that could be, either external applied potential or internal potential due to lattice vibrations, define the electronic properties of any semiconductor material. Analogous to the Newton's laws of motion in classical physics, the behaviour of electrons in crystal structure can be studied using quantum mechanics. The dynamics of electron i.e. the probability of finding an electron, at a particular time and at a particular position in the solid system, can be studied with the help of Schrödinger equation. The solution of Schrödinger equation is a wave function ($\mathbf{\Psi}$) of a particle that corresponds to the energy of that particle. The wave function is a complex term and the squared magnitude of the wave function of an electron gives the probability of finding an

electron in space x at an instant t. Solution of the Schrodinger equation provides the forbidden or allowed states of charge carriers in the quantised state.

For an electron moving along the direction ***x*** in a system under the influence of potential **V(*x*)**, the Schrödinger equation can be given as:

$$-h^2 / 2m^* \left[\left(d^2 / dx^2 \right) + V(x) \right] \Psi_k(x) = E \Psi_k(x) \qquad \text{..... (2.8)}$$

where $\psi_k(x)$ is the wave function of the k^{th} electronic state, E is the energy Eigen value, $\hbar$ is the reduced Planck's constant. The term m^*, given by Eqn. (2.9), is the effective mass of electron which takes into consideration the effect of ions and periodic potential in the crystal lattice on the carriers. If the wave vector associated with an electron is k, then $E(k)$ gives the momentum-energy dispersion relation. The $E(k) - k$ relation is important to understand the band structure of a material which is fundamental information regarding material properties like band gap and conductivity.

$$m^* = \hbar^2 / \left[\partial^2 E(k) / \partial k^2 \right] \qquad \text{..... (2.9)}$$

The kinetic energy E of a particle with mass m^* is related to the wavenumber, k by:

$$E(k) = \frac{\hbar^2 k^2}{2m^*} \qquad \text{..... (2.10)}$$

2.4 1D Schrodinger- Poisson Equation

In order to understand the quantum mechanical changes brought about by the external applied potential in ultra-thin oxides with charge traps, the one dimensional Schrodinger equation needs to be extended to include the total charge density of the system and hence needs to be solved in combination with the electrostatics of the system described by the Poisson equation.

The total electron distribution function $n(x)$ can be related to the Schrodinger equation as

$$n(x) = \sum_{(k=1)}^{m} |\psi_k(x)|^2 \, n_k \qquad \text{..... (2.11)}$$

where n_k is the average occupation number of state k, m is the number of bound states. In the classical treatment of the system, the occupation of the electronic state k is given by the Fermi-Dirac distribution:

$$n_k = \frac{(m^*)}{\pi h^2} \int_{E_k}^{\infty} \frac{1}{1+e^{(E-E_F)/k_B T}}\, dE \qquad \text{..... (2.12)}$$

where E_F is the Fermi level energy, k_B is the Boltzmann constant and T is the temperature. In quantum mechanical treatment, the density of states of electrons and holes in each sub-band need to be known to calculate the total density of carriers. From [2] the density of carriers in each sub band (denoted by i) can be given as:

$$N_i(x) = \frac{n_v m_D^* k_B T}{2\pi\hbar^2} \ln\left[1+e^{\frac{E_c - E_i}{k_B T}}\right] |\psi_i(x)|^2 \quad \text{(for electrons)} \qquad \text{..... (2.13)}$$

$$N_i(x) = \frac{n_v m_D^* k_B T}{2\pi\hbar^2} \ln\left[1+e^{\frac{E_i - E_v}{k_B T}}\right] |\psi_i(x)|^2 \quad \text{(for holes)} \qquad \text{..... (2.14)}$$

Where n_v is the degeneracy factor, m_D^* is the effective mass of density of state. The total density of carriers in the semiconductor can then be expressed as the sum of the density of carriers in each sub-band and the total carriers outside of the quantum well region. With the help of the above equations and the Poisson equation, the eigenvalues and wave-functions in a sub-band can be calculated. Following steps are followed to solve the Schrodinger-Poisson system self-consistently:

1- a starting potential $\phi(x)$ is assumed to solve the Schrödinger's equation.

2- The resulting wave-function and Eigen energy is used to calculate the electron charge density, $n(x)$

3- Poisson equation is again solved to obtain new $\phi(x)$ using $n(x)$.

4- The new value of potential is again used to solve the Schrodinger equation to obtain updated wave-functions and Eigen energies.

5- The above steps are iterated until a certain error criteria is satisfied which is given as $|\phi_i(x) - \phi_{i-1}(x)| < z$, a constant.

2.5 High-*k* Metal gate (HKMG) MOS transistors

Titanium nitride (TiN)/HfO_2 HKMG is a promising candidate to replace poly-Si/SiO_2 gate stack in MOS processes [4]. Good thermal stability and tunable work function makes TiN a good option for metal gate whereas HfO_2 offers merits of large bandgap, good integration with Si and high dielectric permittivity [5][6]. Even though TiN/HfO_2 HKMG provides low EOT and high mobility, issues of threshold voltage (V_T) instabilities and mobility degradation at high

temperature processing due to charged oxygen vacancies is a matter of concern. Post metallization anneal (PMA) has been reported as a good way to diffuse oxygen into the metal/high-*k* stack to overcome V_T instability using work function engineering [7] [8]. However this process introduces additional oxide defects in the gate stack and the limited knowledge of the spatial distribution of these defects makes it difficult to relate the trap generation phenomenon to gate process variables.

Ultra-thin HKMG devices are often plagued by leaky gate and other anomalies like frequency dispersion which affect interpretation of measured data for trap parameter extraction. Conventional experimental techniques to characterize charge defects in the gate stack mainly follow the principles applicable to SiO_2 gated devices and hence corrections need to be made to adapt these methods for high-*k* MOS devices [9]. For example, low frequency quasi-static CV (capacitance–voltage) method [10] that is used to determine interface trap density, conductance technique [11] that is used to determine the trap parameter such as trap density, energy and capture cross-section and Berglund technique [12] that is used to determine flat band voltage are affected by issues related to thin gate oxides such as large leakage current, parasitic impedances, series resistance and so on [13-16]. Charge Pumping (CP) is one of the most widely used methods to characterize traps in the gate stack but, inaccurate assumptions in the values of trap location and capture cross-section could result in erroneous charge density determination [17-19]. Also the distance to which CP can probe is limited [19-20]. Similarly Stress induced leakage current (SILC) is limited by the gate leakage in the device and the depth to which it can probe accurately [21]. Low frequency noise (LFN) and Random telegraph noise (RTN) methods are also being commonly used to locate trap defects in the gate stack [22-23]. Even though these methods provide good understanding of trap energy and location through capture and emission times of defects, they do not provide quantity of traps in the stack and also errors in estimating the trapping energy could result in incorrect trap defect locations [24]. Fixed charge at the interfaces and/or in the bulk of gate dielectric has a direct impact on the inversion charge mobility interacting with inversion channel carriers in the MOS device via Coulomb Scattering [25] [26].

2.5.1 Scattering in CMOS

Unlike carriers travelling in vacuum, electrons travelling in a semiconductor are interrupted i.e. scattered by collisions with impurity atoms, other carriers, phonons and crystal defects of the material, which can be collectively called as scattering centres. Scattering is one of the factors that affect the carrier mobility in a device. Scattering mechanism in a MOS transistor can be mainly categorised as:

1- Phonon Scattering : due to lattice vibrations of the semiconductor material

2- Coulomb Scattering: due to defects/impurities in the semiconductor and gate insulator. Coulomb scattering could be due to the presence of oxide traps in the gate oxide and/or near the semiconductor- insulator interface. It could also be due to the dopants in the channel.
3- Surface roughness scattering: due to irregularity at semiconductor/ insulator interface.

Scattering of a charge carrier takes place due to the interaction of the potentials associated with the carrier and the impurities. This scattering potential can be evaluated with the help of Fermi golden rule (FGR) which can be expressed as in Eqn. (2.15) [27]. Consider a particle with initial state of crystal momentum *k* being scattered to a final momentum state of *k'*. The transition rate of this event can be expressed as:

$$S(k',k) = \frac{2\pi}{\hbar}\left|\langle k'|V(s)|k\rangle\right|^2 \delta(E_{k'} - E_k) \quad \text{..... (2.15)}$$

where V(s) is the scattering potential. The delta function indicates energy conservation during scattering and $\hbar$ is the reduced Planck's constant.

Movement of carriers in a semiconductor system under the influence of electric potential can be understood with the help of Boltzmann transport equation (BTE) [28]. In the presence of scattering, the total rate of change of the distribution function, $f(x,k,t)$ of an electron at position ***x*** at time ***t*** and with momentum ***k*** equals the rate of scattering which can be expressed as in Eqn. (2.16) and is known as the BTE [29].

$$\frac{\partial f}{\partial t} + \dot{x}\cdot\nabla_x f + \dot{k}\cdot\nabla_k f = \left(\frac{\partial f}{\partial t}\right)_{coll} \quad \text{..... (2.16)}$$

where $\dot{k}$ is the rate of change of momentum, $\dot{x}$ is the rate of change of distance which is the group velocity (v_g) of the electrons moving under the influence of the periodic lattice potential i.e. Bloch electrons [30] and the RHS term is known as collision integral. According to Lorentz law, $\dot{k} = qE$ where q is the elementary electron charge and *E* is applied electric field. Eqn. (2.16) then becomes

$$\frac{\partial f}{\partial t} + v_g\cdot\nabla_x f + qE\cdot\nabla_k f = \left(\frac{\partial f}{\partial t}\right)_{coll} \quad \text{..... (2.17)}$$

Considering the scattering event mentioned above, the net effect of scattering can be expressed as

$$\left(\frac{\partial f}{\partial t}\right)_{coll} = \sum_{k'} f(k')\, S(k',k)[1-f(k)] \; - \; \sum_{k} f(k)\, S(k,k')[1-f(k')] \qquad \text{…….. (2.18)}$$

where $f(k)$ is the distribution of electrons in the final state k and $S(k,k')$ is the transition rate when an electron is scattered from initial state of k to a final state of k' (*in-scattering*) and $S(k',k)$ is the transition rate when an electron is scattered from initial state of k' to a final state of k (*out-scattering*). Converting the summation over ***k*** space to integration in ***k*** space, Eqn. (2.18) can be written as

$$\left(\frac{\partial f}{\partial t}\right)_{coll} = \frac{V}{8\pi^3}\int\left\{S(k',k)\,f(k')[1-f(k)] - S(k,k')\,f(k)[1-f(k')]\right\}dk' \qquad \text{…..…... (2.19)}$$

where V is the volume of the crystal and $\frac{V}{8\pi^3}$ is the density of states in '***k***' space.

The BTE can be solved using a Relaxation time approximation (RTA) method which gives the collision integral expression as:

$$\left(\frac{\partial f}{\partial t}\right)_{coll} = -\frac{f(x,k,t) - f_0(x,k,t)}{\tau(k)} \qquad \text{…….. (2.20)}$$

where $\tau(k)$ is the relaxation time which represents the characteristic time a system takes to go back to the equilibrium state once the excitation is removed and $f(x,k,t)$ is the distribution to be calculated. The equilibrium distribution function $f_0(x,k,t)$ can be written as $f_0(x,k,t) = \frac{1}{e^{(E_k-\mu)/k_BT}+1}$. The term in the numerator is the deviation of the distribution function from equilibrium.

The non-equilibrium distribution function can be expressed as the sum of a symmetrical component (f_s) and an asymmetrical component (f_a) of momentum as

$$f = f_s + f_a \qquad \text{…….. (2.21)}$$

The symmetric component assumes equal amount of carriers flowing in opposite directions and hence its contribution to the current flow is zero. The collision integral can also be written as a summation of symmetric and asymmetric components as

$$\left(\frac{\partial f}{\partial t}\right)_{coll} = \left(\frac{\partial f}{\partial t}\right)_{symm} + \left(\frac{\partial f}{\partial t}\right)_{asymm} \qquad \text{…….. (2.22)}$$

The approach of RTA holds true only under certain conditions [29] [31-32] where we assume

1- a non-degenerate semiconductor, which implies f<<1 and the term [1-f] reduces to unity
2- low applied fields, which implies deviation of distribution function from equilibrium to be small
3- collision is elastic in nature

and this allows the collision integral to be written as

$$\left(\frac{\partial f}{\partial t}\right)_{coll} = -\frac{f_a(k)}{\tau(k)} \qquad \text{..... (2.23)}$$

Eqn. (2.17) then becomes

$$\frac{\partial f}{\partial t} + v_g \cdot \nabla_x f + qE \cdot \nabla_k f = -\frac{f_a(k)}{\tau(k)} \qquad \text{..... (2.24)}$$

Knowing the distribution function makes it possible to calculate the macroscopic properties like mobility and conductivity of the semiconductor. Current density due to flow of carriers can be expressed as

$$J = qn < v(x) > \qquad \text{..... (2.25)}$$

where $< v(x) >$ is the average velocity vector at point $\boldsymbol{x}$. $\boldsymbol{J}$ can be written in terms of the distribution function as

$$J = 2\frac{q}{(2\pi)^3}\int v f_a(x,k,t)dk \qquad \text{..... (2.26)}$$

From Eqn. (2.24), assuming steady state condition ($\frac{\partial f}{\partial t} = 0$) and spatially homogenous semiconductor $\left(\nabla_x f = 0\right)$,

$$f_a(k) = -\tau(k)\frac{qE}{\hbar}\nabla_k f \qquad \text{..... (2.27)}$$

Replacing f by f_0, as deviation from equilibrium is assumed to be small, and with change of variables,

$$\nabla_k f \approx \nabla_k f_0 = \frac{\partial f_0}{\partial \varepsilon} \cdot \nabla_k \varepsilon(k) = \hbar \frac{\partial f_0}{\partial \varepsilon} v \qquad \text{..... (2.28)}$$

where $\varepsilon = \frac{(\hbar k)^2}{2m^*}$ is the electron energy.

Eqn. (2.27) then becomes,

$$f_a(k) = -q\tau(k)\frac{\partial f_0}{\partial \varepsilon}(v \cdot E) \quad \text{..... (2.29)}$$

Substituting Eqn. (2.29) in Eqn. (2.26) yields,

$$J = -\frac{q}{4\pi^3}\int \tau(k)\frac{\partial f_0}{\partial \varepsilon}\, v\, (v \cdot E)dk \quad \text{..... (2.30)}$$

According to Ohm's law,

$$J = \sigma E \quad \text{..... (2.31)}$$

where σ is the conductivity and E is the electric field.

From Eqn. (2.31) and Eqn. (2.30)

$$\sigma = -\frac{q}{4\pi^3}\int \tau(k)\frac{\partial f_0}{\partial \varepsilon} v^2 dk \quad \text{..... (2.32)}$$

Also

$$\sigma = qn\mu \quad \text{..... (2.33)}$$

where μ is the mobility and n is the electron concentration given as

$$n = \frac{1}{4\pi^3}\int f_0 dk \quad \text{..... (2.34)}$$

From Eqn. (2.31) and Eqn. (2.33), mobility (μ) can be derived as

$$\mu = \frac{q\int \tau(k)\frac{\partial f_0}{\partial \varepsilon}\, v^2 dk}{\int f_0 dk} \quad \text{..... (2.35)}$$

Calculations explained in Section 2.5.1 forms the basis of the in-house simulator, SCATTER, used in this study to understand the spatial distribution and quantification of charge traps in the gate stack influencing the carrier mobility in HKMG devices.

2.5.2 Materials and properties

One of the major application area for thin film devices is as the select transistor in flat panel displays [33]. Fabricating efficient thin film devices require conductor, semiconductor and insulator materials that would exhibit good uniform performance characteristics when deposited on a large area. Along with cost of fabrication, for transistors in display applications, transparency is also a driving factor and materials that would allow fabrication at lower temperature and are transparent in the visible region of the electromagnetic spectrum are favoured. The area of thin film transistors (TFTs) has gained much attention fairly recently with the discovery of oxide semiconductors that allow fabrication of TFTs with better electrical performance than a-Si or pc-

Si. Transparent Conducting Oxides (TCO) such as IGZO, SnO_2, IZO and ZnO are among the most widely investigated materials that satisfy the 'transparency' criteria and also exhibit high electrical conductivity [34-38]. Additionally, to realise a fully flexible transparent TFT, transparent gate electrode and gate insulator, that are compatible with low temperature processing are essential. HfO_2, Ta_2O_5, SiN are among the gate insulator materials that are currently explored [39-41]. For rigid transparent applications a glass substrate is widely used whereas plastic and paper find use as substrate for flexible devices [42-43]. These substrates are usually coated with a transparent conducting material such as Indium tin oxide (ITO) to form the gate electrode of the TFT devices [44]. In this study, ZnO is employed as the semiconducting material. ZnO is a II-VI direct bandgap semiconducting material with a band gap energy of about 3.4eV [45].

Unlike in conventional MOS transistors where the device is grown on a bulk semiconducting substrate, semiconducting layer of oxide devices are often deposited leading to low crystal quality or in other words, amorphous or polycrystalline semiconducting channel layer. Low temperature deposition of ZnO results in the oxide semiconductor in a polycrystalline atomic structure.

Generally, the increased structural randomness/disorderliness of the amorphous semiconductors result in increased collisions among the carriers and thus in degraded carrier mobility in comparison with polycrystalline and crystalline materials. The initial TFT devices, which were based on a-Si, thus exhibited mobilities in the range of $1cm^2/Vs$ [46] whereas single crystalline Si gives a typical mobility of over 500 cm^2/Vs. Devices with improved mobility were made possible by using pc-Si, however, this required higher temperature deposition which is a barrier for realising TFT devices on cheaper plastic substrates. However, in 2004 Nomura et al [46], reported a high mobility TFT device using a-IGZO semiconductor channel, which gave a field-effect mobility of ~10 cm^2/Vs, despite the amorphous nature of the oxide semiconductor. Reason for this improved performance in ionic IGZO semiconductor is suggested due to the *s* orbital of the heavy metal cations that form a highly dispersed conduction band minima resulting in small electron effective mass [47]. Even though pc-ZnO is an ionic oxide and is a strong contender for TTFT applications, ZnO TFTs are believed to exhibit low mobility due to grain boundary scattering [48][49]. However recent work by Brox-Nilsen et al. [50] and Zhang et al. [51] have reported ZnO TFTs with mobilities $>50cm^2/Vs$. This brings up the question of whether grain boundary scattering is dominant in pc-ZnO TFTs or if the carrier conduction in ZnO is similar to that in a-IGZO and this forms the hypothesis for this study.

2.5.3 Carrier transport in thin film devices

As discussed earlier, lattice of the disordered amorphous and polycrystalline materials have aperiodic lattice structure which gives rise to increased scattering and hence lower device mobility. The electrical performance of the oxide semiconductor TFTs is dependent on the

fabrication processes and can be better understood with the knowledge of carrier transport in the devices. The density of states (DOS) represent the measure of disorder in a material and can be used to study the carrier transport mechanism of the material [52].

In non-crystalline materials, the states/ traps are localised near the edges of conduction band (E_c) and valence band (E_V) and these traps have some 'activation energy' associated with them. In the conduction band of a non-crystalline semiconductor the localised states are separated from the non-localised states by an energy, E_{CM} ,termed as mobility edge [53]. The activation energy (E_a) is the minimum energy needed by the electrons to escape the localised state and is defined as the energy difference between the Fermi level and the conduction band edge. E_a is maximum at the flat band condition. Fig.2.3 shows a schematic of the concept of localised and delocalised states in non-crystalline semiconductors.

Carrier transport in amorphous materials is mainly governed by mechanisms such as Variable range hopping (VRH), Percolation and Trap limited conduction (TLC) which are temperature and applied bias dependent. Fig.2.4 shows a two dimensional schematic of the three conduction mechanisms.

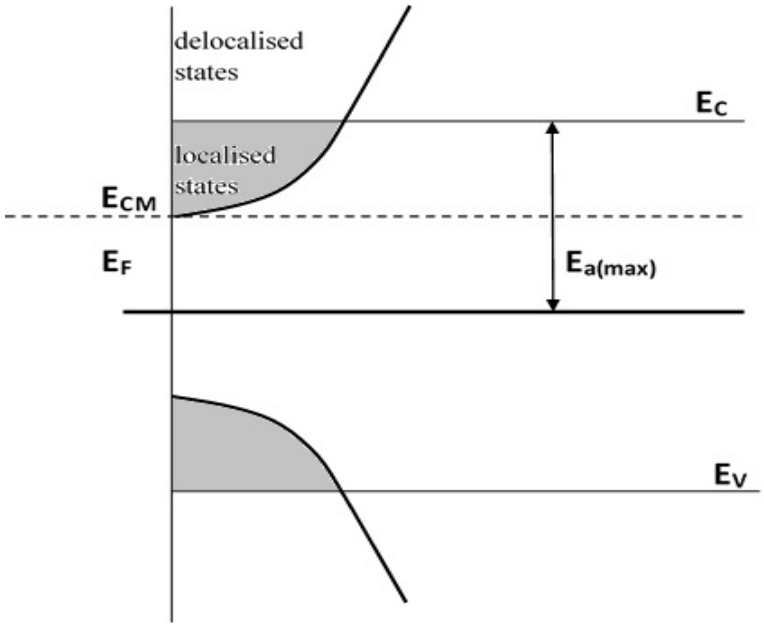

Figure 2.3: Schematic energy band diagram showing the existence of localised and delocalised states in non-crystalline semiconductors.

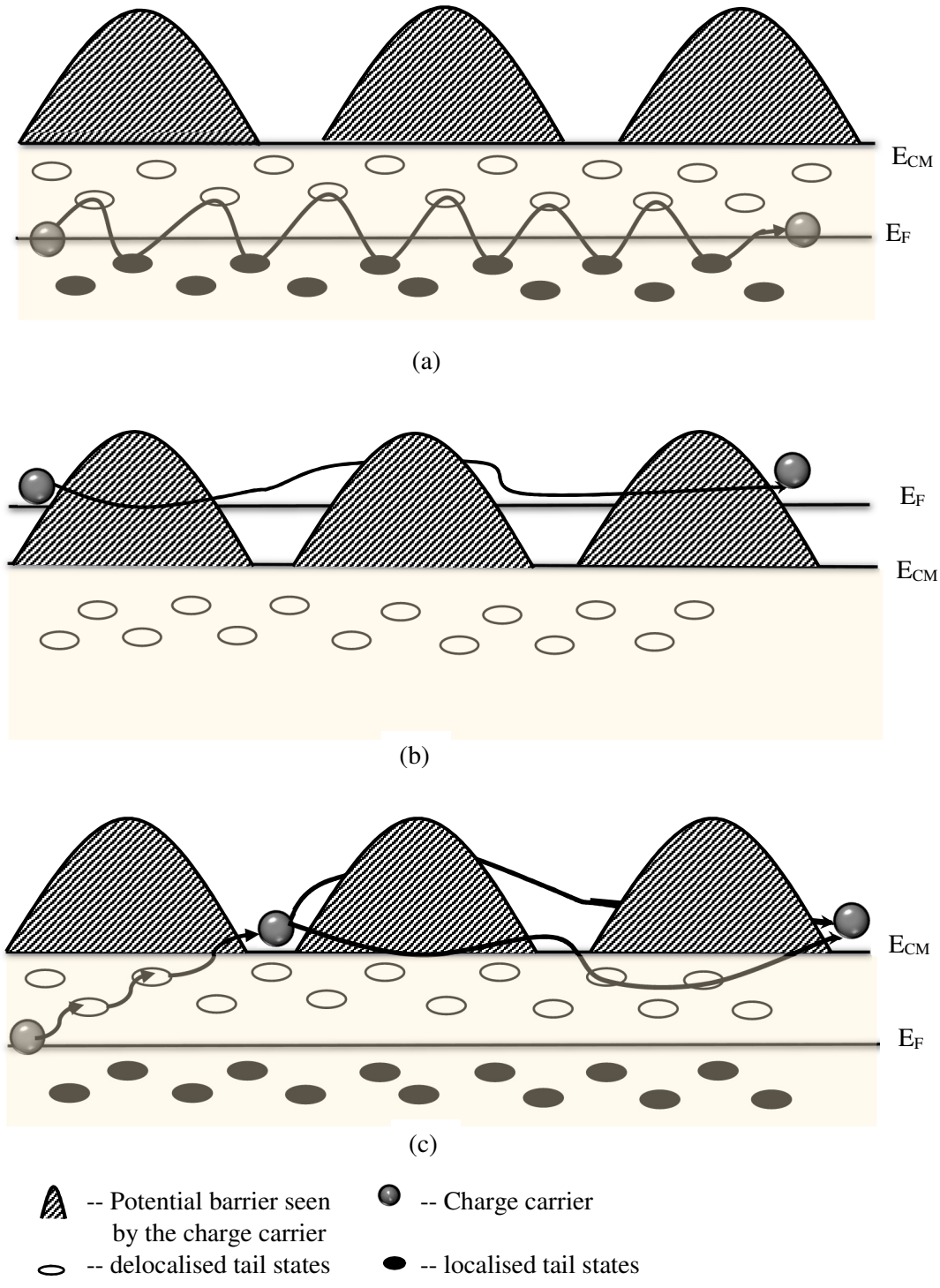

Figure 2.4: Two dimensional schematic showing (a) Variable range hopping (b) Percolation (c) Trap limited conduction mechanism.

In VRH, the fermi level is below the mobility edge and the charge transport occurs with the charge carrier hopping between the localised states. This conduction is dominant at low temperatures. In Percolation conduction, known to be prevalent at higher applied bias regions and independent of the temperature considered, Fermi level moves into the conduction band and carrier transport

takes place with the charge carriers moving around/through (i.e. percolating) the potential barrier. Similar to VRH, TLC is characterised by the presence of Fermi level of the semiconductor within the localised tail states. But unlike VRH, TLC governs carrier transport at high temperatures and low effective fields when the carriers are released into the conduction band by thermal generation [54-56]. Carrier conduction in poly-crystalline semiconductors is considered to be grain-boundary limited and is often explained with the help of Seto's model [57].

2.6 Simulators- SP-Scatter and SCATTER

This section gives a brief description of the in-house Schrodinger-Poisson solver *SP-Scatter* [58] simulator and device mobility simulator *SCATTER* [59] used in this study. *SP-Scatter* is a one dimensional (1D) Schrodinger-Poisson solver and some of the main features of the simulator are:

1- It incorporates an arbitrary number of gate stack layers and material orientations. Also allows for a variation in band gap and dielectric constant along the gate stack.
2- Includes a non – parabolic band structure
3- Considers wave penetration in the oxide
4- Considers exchange-correlation and image potential
5- Can calculate both interface state density (D_{it}) and fixed charge density (N_{fix}).

For a given semiconductor/gate stack structure *SP- Scatter* defines a grid to represent the quantised energy well and to calculate the wave function of each quantised sub-band. Eigen energy values and electron occupation of each sub-band is calculated for the range of gate bias values specified in the input file. Also charge density and effective field is calculated for the entire input voltage range. For a given gate work function value, the fixed charge density in the device can be determined using *SP-Scatter*.

Results of Schrödinger- Poisson solver serves as the input for the device mobility simulator *SCATTER*. Values of charge density, Eigen wave function, Eigen energy values and electron occupation are input to *SCATTER* to calculate device mobility while taking into consideration the scattering mechanism in the device. *SCATTER* allows to vary the magnitude and position of charge defects in the gate stack to allow study the impact of Coulomb scattering on device mobility. *SCATTER* employs Poisson equation based on Green's function to calculate coulomb scattering limited device mobility [59] [60].

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Chapter 3

Effect of Post-metallisation anneal in the charge trap distribution in TiN/HfO_2/SiO_2/Si MOS device

In this study we aim to quantify and identify the spatial distribution profile of the charge traps in the gate stack of high-k metal gate (HKMG) samples, resulting from the two different gate stack annealing processes they are subjected to. The samples used in this study have been supplied by the University of Texas (Dallas). Details of the fabrication process can be found in [1]. One of the samples have been subjected to Post metallization anneal (PMA) in O_2 ambient in addition to Forming gas anneal (FGA). The PMA process is assumed to introduce additional oxide trap defects in the gate stack. Fixed oxide charge at the interfaces and/or in the bulk of gate dielectric has a direct impact on the inversion charge mobility interacting with inversion channel carriers in the MOS device via Coulomb Scattering [2-3]. In this study we make use of this concept to extract the spatial distribution profile of the fixed oxide charge in the gate stack resulting due to PMA. A device with only Forming Gas anneal (FGA) is used for comparison. The QM mobility model, *SCATTER*, allows the trap defects to be placed anywhere along the gate stack. The interface states are determined experimentally via conductance technique [4].

Section 3.1 discusses the electrical measurement set-up and electrical device parameter analysis and extraction of the two samples. Section 3.2 discusses the experimental methodology and results of charge density calculations. Section 3.3 discusses the device mobility and charge distribution results followed by discussion of the findings in Section 3.4.

3.1 Measurement Setup and Electrical device parameter extraction

The samples have a gate stack comprising of SiO_2 (1nm)/ HfO_2 (2nm) /TiN (10nm) /Al (300nm) on p-type Si wafer. The HKMG sample with only Forming gas anneal , henceforth referred to as ***Sample P1***, has a 700 ^oC anneal in N_2 for 60 sec post HfO_2 deposition and the HKMG sample with FGA and PMA, henceforth referred to as ***Sample P2***, has an additional 30 sec O_2 anneal post TiN deposition. The effective gate work function (EWF) of Sample P1 and Sample P2 has been determined through Internal PhotoEmission (IPE) [20].

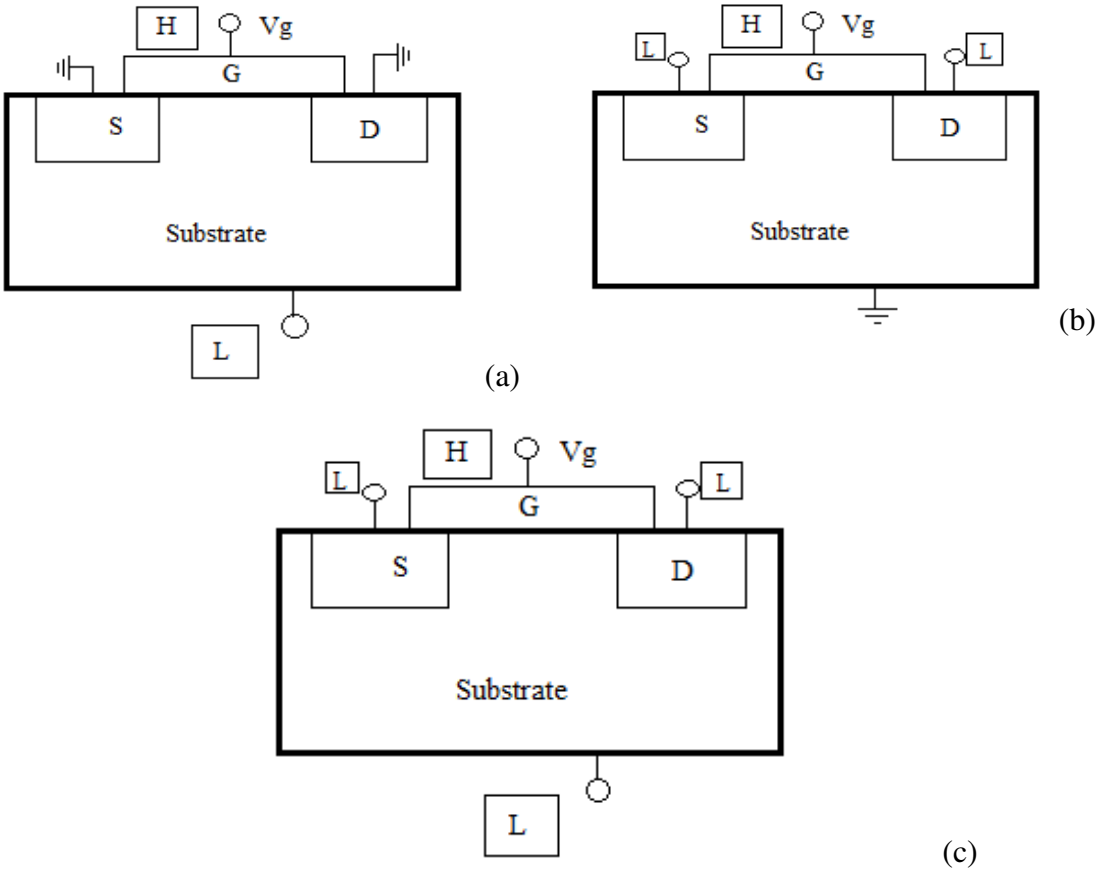
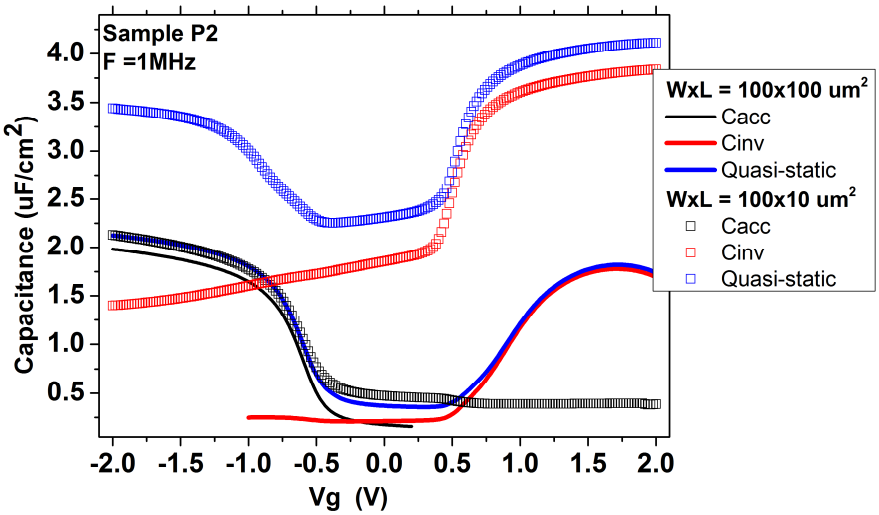


Figure 3.1: Schematic connection diagram for (a) Gate to bulk (Accumulation) capacitance (b) Gate to Source-Drain (Inversion) capacitance (c) Quasi-static capacitance (H : High Potential High Current; L: Low Potential Low Current terminals of the LCR meter.)

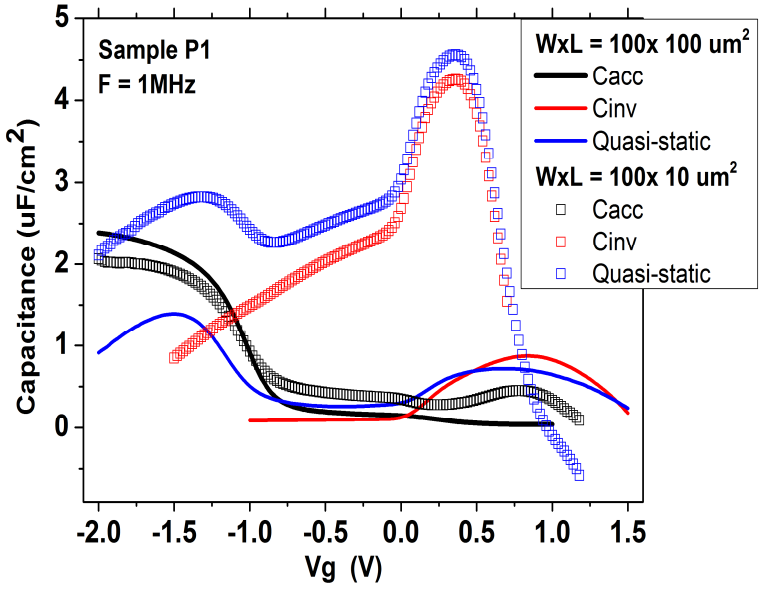
Fig. 3.1 shows the electrical split-CV measurement setup of the MOS devices carried out using Agilent E4980A LCR meter with open/short corrections to take into account parasitic impedances of cables, connectors and adaptors. Quantum mechanical simulations are carried out using in-house Schrödinger-Poisson solver, *SP-Scatter* [21], to match the measured and experimental CV characteristics and mobility code *SCATTER* [22], to calculate Coulomb Scattering.

3.1.1 Gate Leakage and Dissipation Factor

Fig. 3.2(a) and 3.2(b) compares the Split CV and Quasi-static CV characteristics obtained from short channel and long channel devices of sample P1 and sample P2. It can be seen that the measured split CV and Quasi-static CVs of the devices, for short channel and long channel, and for both Samples, sample P1 and P2, do not coincide. Assuming this mismatch behaviour in CV plots could be due to the parasitic effects induced by the chuck of the probe station, measurements were repeated by isolating the wafer from the chuck [5]. The samples were placed on a copper plate and then mounted on a glass plate to ensure isolation from the chuck of the probe station.



(a)



(b)

Figure 3.2: Comparison of Split CV and Quasi-static CV curves from short channel and long channel devices of (a) Sample P2 (b) Sample P1.

The copper plate provided connection to the substrate of the device while the glass plate ensured isolation of the device from the chuck. Schematic of the set-up is shown in Fig. 3.3.

A comparison of the measurements obtained, with and without the copper plate connection, for short channel device, W x L = 100x5 um^2 , of Samples P1 and P2 is shown in Fig.3.4. The measurements did not show any significant improvements with relation to the Split CV curves although the capacitance roll-off of Sample P1 at higher gate voltages was improved by the isolation process.

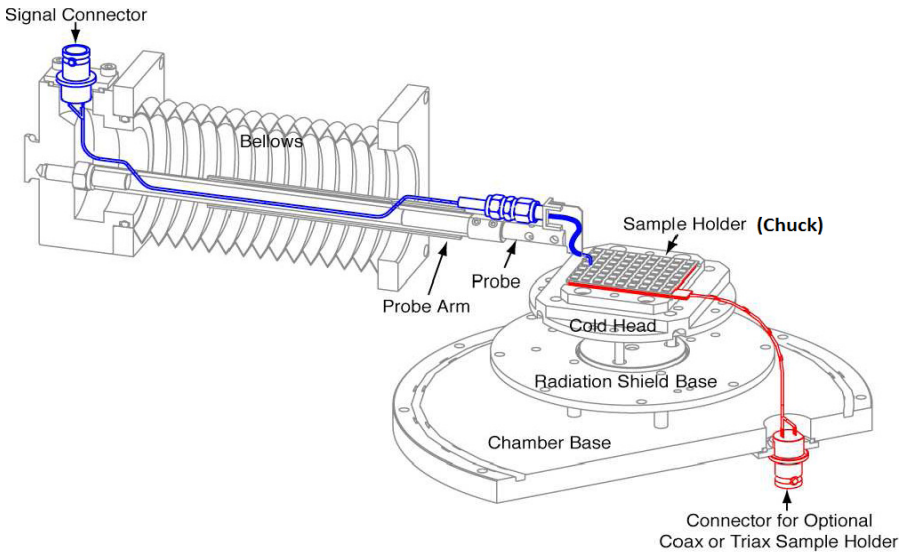
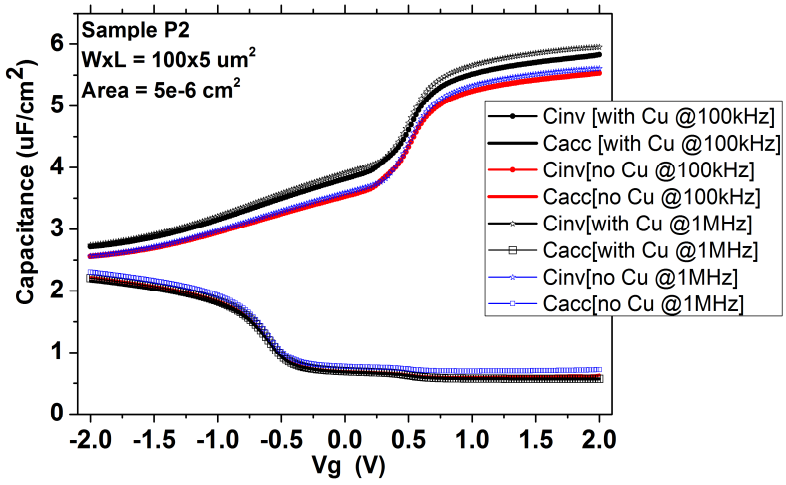
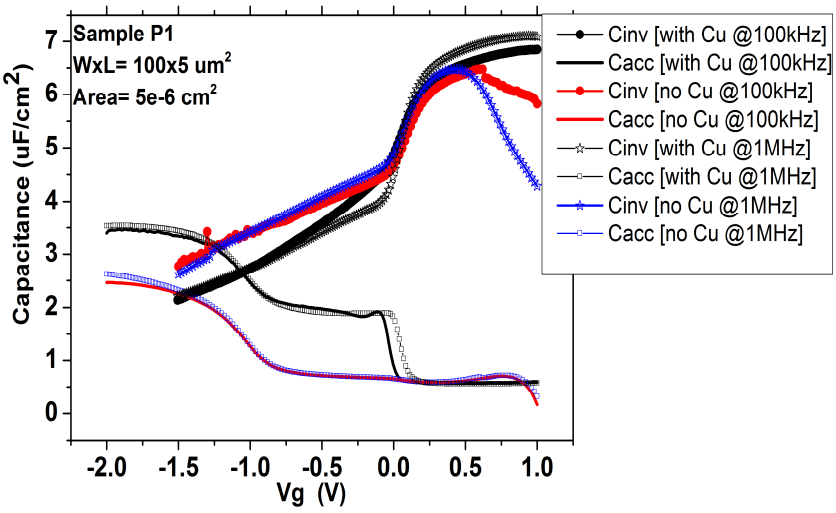


Figure 3.3: Schematic cross-section of connection from probe-arm to the base of the chuck. The connector shown in red forms the chuck (base) connection during measurement. [6]



(a)



(b)

Figure 3.4: Measured Split CV curves from short channel device (W x L = 100x5 um^2) of Sample P1 and P2 showing the effect of chuck capacitance (*with/no Cu* indicates presence/absence of the copper plate).

Due to the decreasing thickness of the gate oxide in the modern CMOS devices, the gate capacitor becomes very lossy due to direct tunnelling current. The lossy nature of the gate capacitor is represented in the CV measurements by the Dissipation factor (D) which is dependent on frequency and which, for gate oxide thickness < 2nm, is preferable to be within D<10 [7].

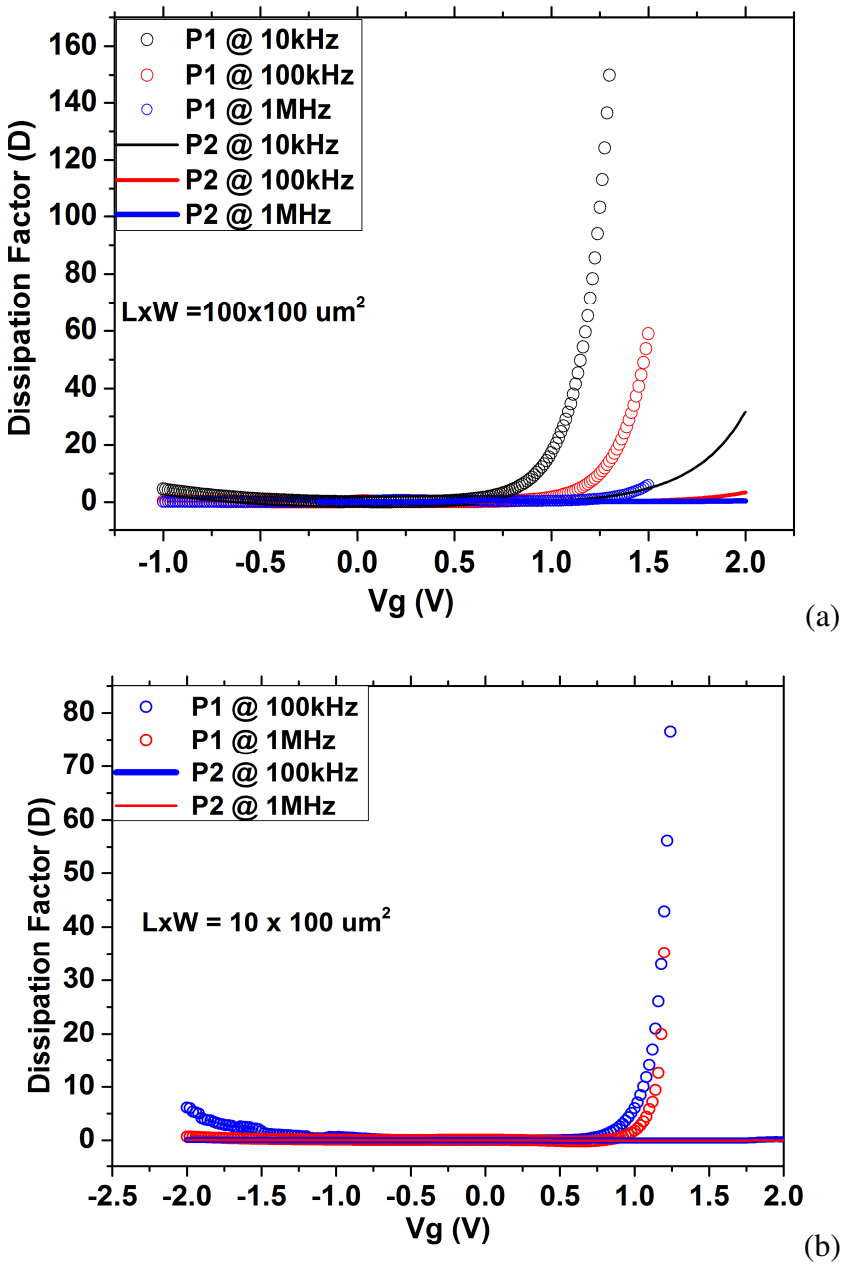


Figure 3.5: Dissipation Factor obtained from (a) long channel and (b) short channel length device.

The variation of dissipation factor with respect to frequency obtained from a typical long channel and short channel device, of Samples P1 and P2 is shown in Fig. 3.5(a) and Fig.3.5 (b) respectively. Large leakage i.e. large ***D*** is reflected in the CV characteristics as roll-off in the

accumulation and inversion capacitances and/or negative capacitance values at high gate voltages. The dissipation factor decreases with increase in frequency. The gate leakage for Sample P1 is higher compared to Sample P2. For ultra-thin high-*k* gate MOS structures, along with the gate oxide leakage current, the resistance drop across the channel is also an important factor and can contribute to the capacitance roll-off at high gate voltages. To keep the leakage to a minimum, capacitance measurements from short channel length devices are preferred but, since large area devices are required to obtain sufficient capacitance, CV measurements are usually carried out on devices with large W/L ratio[7]. The gate leakage problem of the MOS structures can also be overcome by measuring the capacitance at high frequencies so that the capacitive current becomes dominant. In order to keep the channel resistance and the gate leakage at minimum, measurements were considered at 1MHz. High frequency measurements are also preferred to avoid charge trapping effects in the MOS Sample.

3.1.2 Gate oxide thickness and oxide capacitance

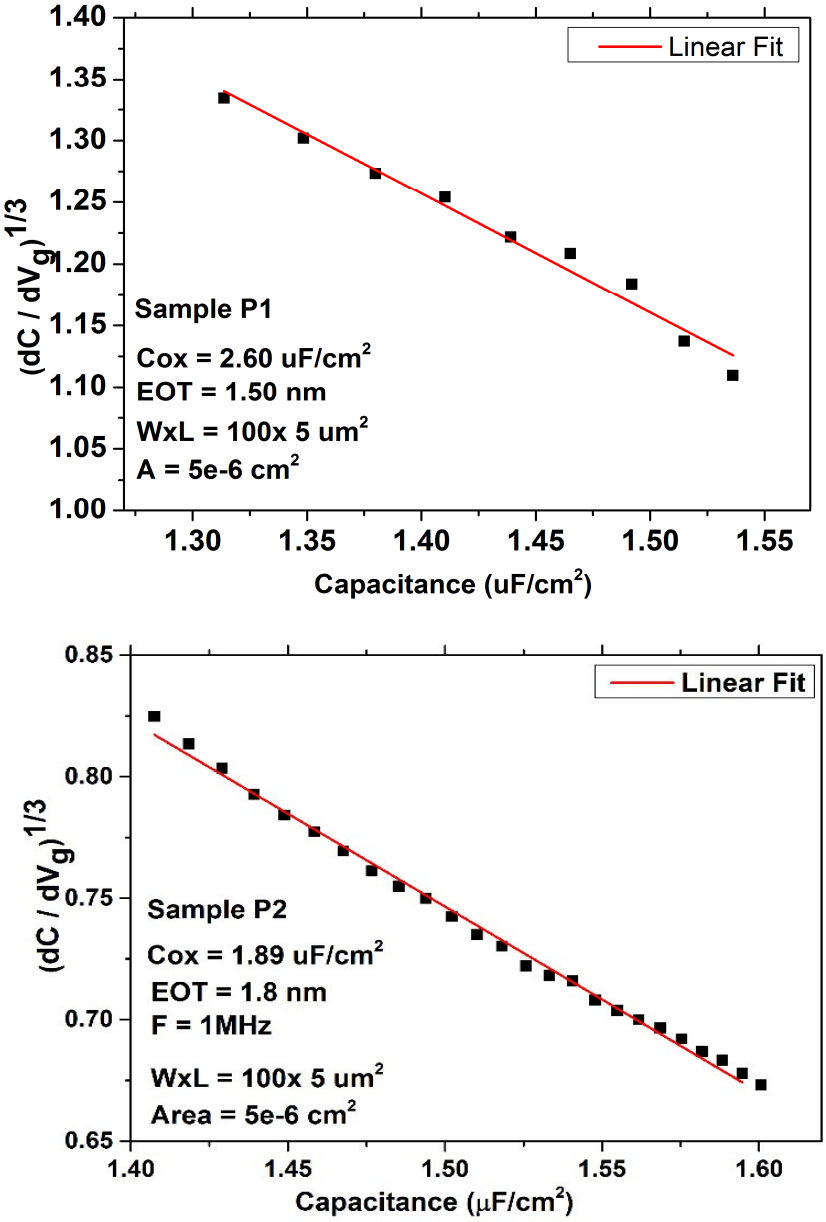
In traditional Si-MOS devices with SiO2 insulator, the thickness of the gate insulator is the same as the thickness of the SiO2 layer. However, in MOS devices with high-*k* gate insulator layer, the thickness of the gate oxide is expressed in terms of 'Equivalent Oxide Thickness' (EOT). EOT, given by Eqn.3.1, indicates the thickness of the high-k layer in terms of the thickness of SiO_2 layer. The gate oxide stack of the Samples P1 and P2 consists of 2nm of HfO_2 and 1nm of SiO_2 which gives an EOT of 1.35nm. The oxide capacitance ($\boldsymbol{C_{ox}}$) of the samples, calculated numerically using Eqn.3.2, yields a value of 2.88 μF/cm^2.

$$EOT \ \ (in\ nm) \ = \ \varepsilon_{SiO_2} \ * \ \left(t/\varepsilon\right)_{higk\text{-}k} \qquad \text{..... (3.1)}$$

$$C_{ox} = \varepsilon_{SiO_2} * A / t_{ox} \qquad \text{..... (3.2)}$$

where $\left(t/\varepsilon\right)_{higk\text{-}k}$ is the thickness/dielectric constant of the high-*k* insulator layer, ε_{SiO_2} is the dielectric constant of SiO_2 (~ 3.9), *A* is the gate area and t_{ox} is the oxide thickness.

Islam's technique [8] provides an analytical alternative to determine the oxide capacitance and oxide thickness values. Islam's model for the accumulation gate capacitance of MOS structure with high-k dielectric gate takes into account the Quantum mechanical effects in the structure. Islam's model assumes linear approximation of the relationship between the accumulation capacitance and Silicon surface potential in moderate accumulation as



(a) (b)

Figure 3.6: EOT and oxide capacitance values obtained for Samples P1 and P2.

$$C_{acc} = a + b * \phi_S \qquad \text{..... (3.3)}$$

C_{acc} is the accumulation capacitance, a and b are constants and ϕ_S is the surface potential. Using the relation between the surface potential and gate voltage (V_g), in Eqn.3.4, established by [9]

$$\frac{d\phi_S}{dV_g} = 1 - \frac{C_g}{C_{ox}} \qquad \text{..... (3.4)}$$

and considering the total capacitance in moderate and strong accumulation to be equal to C_{acc}, Eqn.3.5 is derived as

$$\left|\frac{dC_g}{dV_g}\right|^{1/3} = b^{1/3}\ (1\ -\ \frac{C_g}{C_{ox}}) \qquad \text{…….. (3.5)}$$

where C_g is the gate capacitance. Oxide capacitance is obtained from the linear intercept of $\left(dC_g/dV_g\right)^{1/3}$ versus the gate capacitance in the strong accumulation region. Fig. 3.6 shows the results obtained from Islam's technique for Samples P1 and P2. The higher EOT obtained for Sample P2 could be due to the additional O_2 anneal of the gate stack of Sample P2.

3.1.3 Flat band voltage and Substrate doping density

Maserjian's *Y function* method [10] allows analytical estimation of flat band voltage and substrate doping density in Si-MOS. Eqn. 3.6 gives the expression to determine the device parameters from the measured CV data.

$$Y = (1/C)^3\left(\frac{dC}{dV_g}\right)$$

$$= (1/C_{Si})\left(\frac{dC_{Si}}{d\Phi_S}\right) \qquad \text{…….. (3.6)}$$

where C and C_{Si} are, respectively, the measured and semiconductor capacitances and Φ_S is the surface potential.

Maserjian's function is independent of the oxide capacitance and considers the total capacitance as a series combination of oxide capacitance and substrate capacitance. Using *Y*-function, the flat band voltage is determined as the gate voltage (V_g) at which Y is 1/3 of the minimum value of Y in depletion and is given as

$$Y_{\min} = \frac{-1}{q\ \varepsilon_{Si} N_{dop}} \quad \text{and} \qquad \text{…….. (3.7)}$$

$$Y_{fb} = Y_{\min}/3 \qquad \text{…….. (3.8)}$$

Fig.3.7 shows the parameters estimated for Samples P1 and P2.

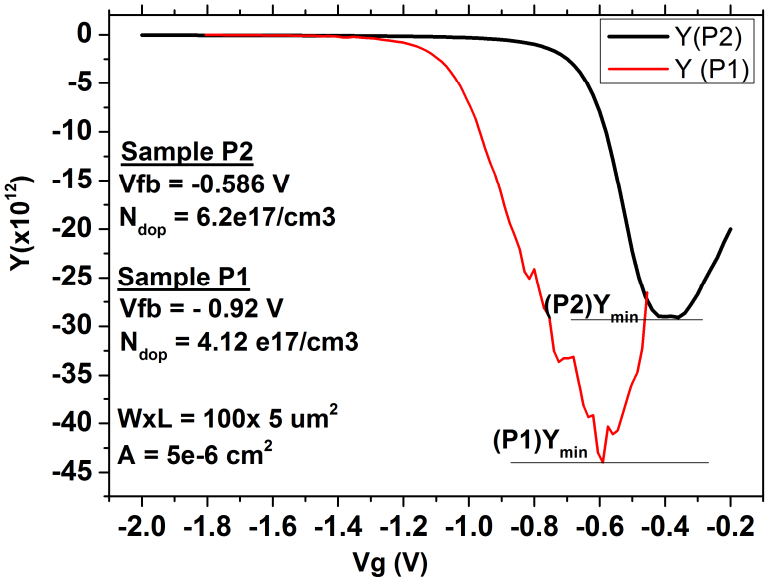


Figure 3.7: Substrate doping density calculation using Y-function method.

3.1.4 Fixed oxide charge density

Fig.3.8 shows the plot of flat band voltage (V_{FB}) versus Equivalent Oxide Thicknesses (EOT) to determine effective gate work function (EWF) of the samples [20] [23]. For an EOT of 1.35nm, EWF obtained for Sample P1 and P2 are 4.1eV and 4.45eV, respectively [11]. Introduction of oxygen into the TiN metal gate yields a higher EWF.

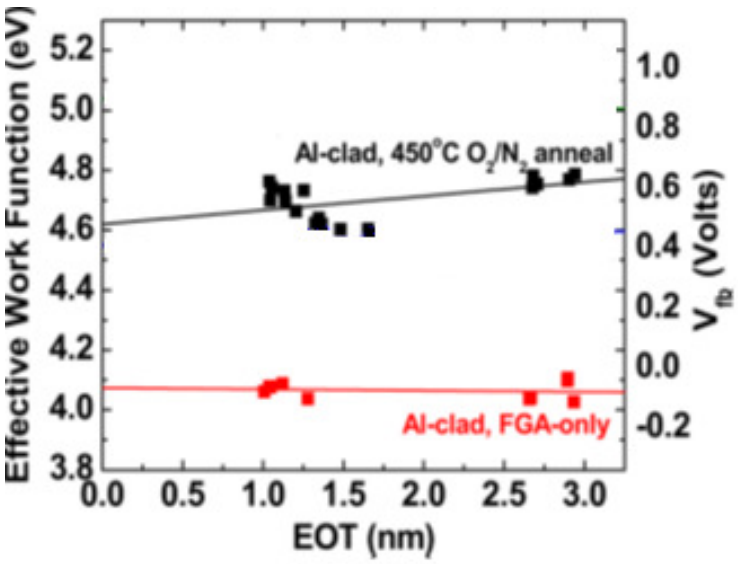


Figure 3.8: EWF extraction from EOT and $V_{FB.}$ (data from University of Texas(Dallas)).

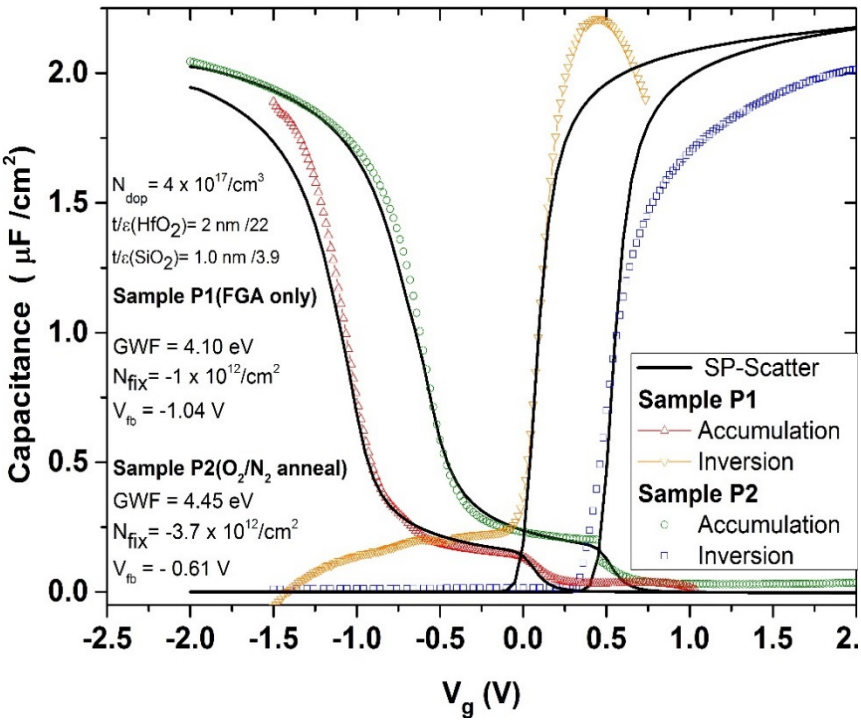


Figure 3.9: Experimental (shown in symbols) and simulated (shown in black lines) Split CV characteristics for Sample P1 and P2. Device parameters estimated from SP-Scatter for samples P1 and P2 is shown in the plot. EWF from IPE has been used.

Fig.3.9 shows the experimental split CV characteristics of the samples measured at a frequency of 1MHz. A shift towards more positive values of flat band and threshold voltages can be observed for the sample with O_2/N_2 PMA indicating the presence of negatively charged fixed charge defects in the gate oxide layer. This shift in V_{FB} has been previously suggested to be due to the introduction of higher applied bias to align the Fermi levels of the gate stack and the substrate [12]. Once the EWF is determined independently, the fixed charge density is ascertained by matching the experimental CV with *SP-SCATTER*. A charge density of 1.0×10^{12} cm^{-2} and 3.7×10^{12} cm^{-2} is estimated for Sample P1 and P2, respectively. SP simulations consider the fixed charge density to be located at the Si/SiO_2 interface.

3.1.5 Experimental Mobility calculation from Split CV characteristics

Experimental mobility of the Sample P2 devices is calculated using the Split CV method. The channel mobility is calculated as

$$\mu_{eff} = (W / L) * g_d / Q_i \quad \text{..... (3.9)}$$

$$g_d = \left.\frac{dI_d}{dV_d}\right|_{V_g = cons\tan t} \qquad \text{…….. (3.10)}$$

$$Q_i = \int_{-\infty}^{V_g} C_{gc}(V_g)\, dV_g \qquad \text{……. (3.11)}$$

The Effective field is then calculated as

$$E_{eff} = \left(\eta * Q_i + Q_b\right) / \varepsilon_S \qquad \text{…….. (3.12)}$$

where η = ½ for electrons (averaging of the electric field over the electron distribution in the inversion layer) [13]

$Q_b = \int_{V_{fb}}^{\infty} C_{gb}\, dV_g$ is the depletion charge

ε_S = semiconductor dielectric permittivity

and a universal mobility [14] plot is obtained by plotting mobility against effective field.

3.3 Conductance Technique to determine interface state density (D_{it})

The conductance Technique [4] is an efficient method to determine the density of interface states in MOS devices. This method is based on the principle that the energy loss/gain during the capture/emission of electrons by traps in response to applied bias and frequency is reflected in the parallel conductance and capacitance measured from the MOS device. The conductance technique can be employed either as a function of voltage [15] or as a function of frequency [16]. Here, conductance-frequency method is employed to extract the density of interface state across the band gap of Si. Conductance of the MOSFET in accumulation, depletion and inversion regimes are performed as a function of frequency at constant gate potentials. Conductance due to traps/interface states attain a maximum at a frequency that corresponds to the time constant of the trap. D_{it} extraction technique proposed in [17] and [18] employ a modified conductance-frequency method that take the effects of the parasitics in ultra-thin gate devices into account and extract the parallel conductance and capacitance of the Si bulk from the measured data.

Considering a parallel connection mode, the electrical equivalent of the MOS structure when measured between gate and substrate terminals can be shown as in Fig. 3.10.

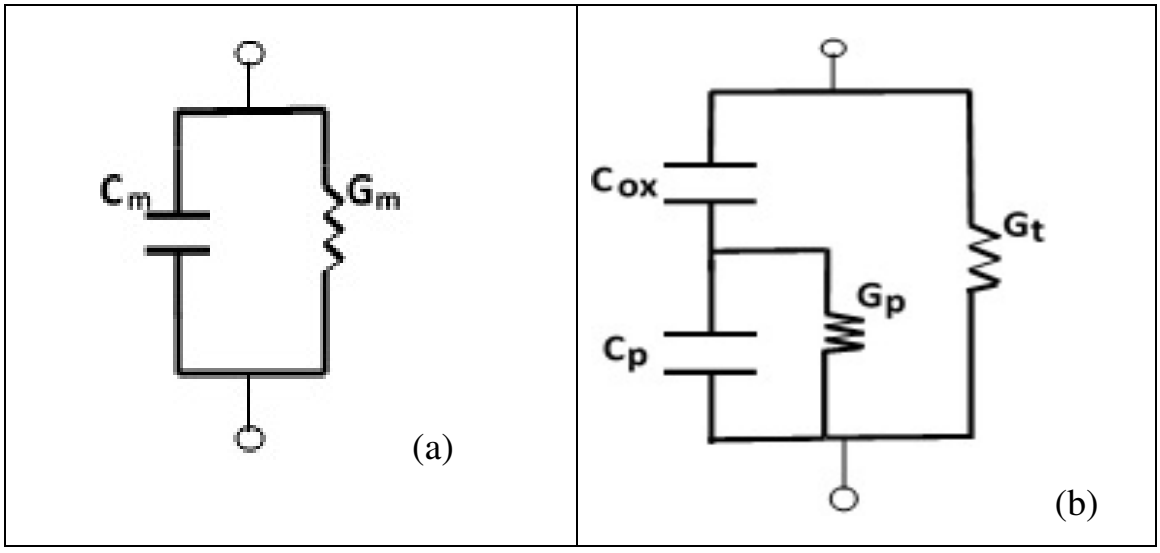


Figure 3.10: Electrical equivalent circuit of MOS structure. a) Measured capacitance (C_m) and conductance (G_m) between gate and substrate in accumulation and depletion mode. b) Oxide capacitance (C_{ox}), parallel capacitance (C_p) and conductance (G_p) of the substrate and tunnelling conductance (G_t) between gate and substrate terminals [17] .

C_{ox}, C_m and C_P are the oxide, measured and corrected parallel capacitances respectively. G_t G_m and G_P are, respectively, the tunnelling conductance due to gate leakage, measured and parallel conductance of the substrate. In strong accumulation, magnitude of the measured capacitance is almost same as that of the capacitance due to gate oxide. From the measured conductance (G_m) and capacitance (C_m), the parallel conductance (G_P) of the device can be written as

$$G_p = \frac{G_m - G_t}{\left(\frac{G_m - G_t}{\omega C_{ox}}\right)^2 + \left(1 + \frac{C_m}{C_{ox}}\right)^2} \quad \text{..... (3.13)}$$

where $\omega = 2\pi f$ is the frequency.

Interface state density is extracted by fitting the normalised parallel conductance, G_p / ω, vs. ω curve from measurement using an appropriate model for the interface trap energy. Assuming a single time constant model where interface traps are assumed to be on the same energy level, the parallel conductance can be expressed as

$$G_p / \omega = \frac{q\omega D_{it}\tau_{it}}{1 + \omega^2 \tau_{it}^2} \quad \text{..... (3.14)}$$

where τ_{it} is the interface state time constant and q is electron charge.

If a continuum of states is assumed, i.e. if the interface states are assumed to be continuously distributed throughout the Si band gap, G_p / ω can be written as

$$G_p / \omega = \frac{q \cdot D_{it}}{2 \cdot \omega \cdot \tau_{it}} \ln\left((1 + (\omega \cdot \tau_{it})^2\right) \quad \text{..... (3.15)}$$

and assuming surface potential fluctuations in the substrate due to non-uniformities in doping density, oxide and interface charges, the normalised conductance can be written as

$$G_p / \omega = \frac{q}{2} \int_{-\infty}^{+\infty} \left[\frac{D_{it}}{\omega\tau_{it}} \ln(1 + (\omega\tau_{it})^2) \frac{1}{\sqrt{2\pi\sigma^2}} \exp\left(- \frac{\Psi_s - \overline{\Psi_s}}{2\sigma^2} \right) \right] d\Psi_s \quad \text{..... (3.16)}$$

where σ is the standard deviation of the surface potential fluctuations, Ψ_s is the surface potential and $\overline{\Psi_s}$ is the mean surface potential [26]. Berglund integral [9], given in Eqn. (3.17), makes it possible to calculate the surface potential which can then be employed to determine the distribution of interface states in the band gap.

$$\Psi_S = \int_{V_{FB}}^{V} 1 - \frac{C_c}{C_{ox}} dV_g \qquad \text{..... (3.17)}$$

where V_{FB} is the flatband voltage, V_g is the applied gate potential and C_c is the corrected capacitance.

In inversion mode of operation the interface state response is modelled using a transmission line model proposed in [18]. This model considers the effect of parasitics such as gate leakage, channel resistance and depletion capacitance and models the channel response assuming single trap model for interface states.

Fig. 3.11 shows the measured and modelled G_m / ω as a function of ω in weak inversion for Sample P2. A fit to the measured G_m / ω curve is obtained by iterating D_{it} and τ_{it}. Fig. 3.12 shows the D_{it} distribution in the upper band gap of sample P2. Conductance and capacitance measured in depletion and inversion mode for Sample P1 (not shown) and in the depletion mode in Sample P2 (not shown) does not show any features/ peaks and needs further investigation and modelling to extract interface state density values.

Total interface state density (N_{it}) is calculated by integrating D_{it} over the entire band gap. A total N_{it} ~ 1.0x10^{12} cm^{-2} is obtained in the upper band gap of Sample P2.

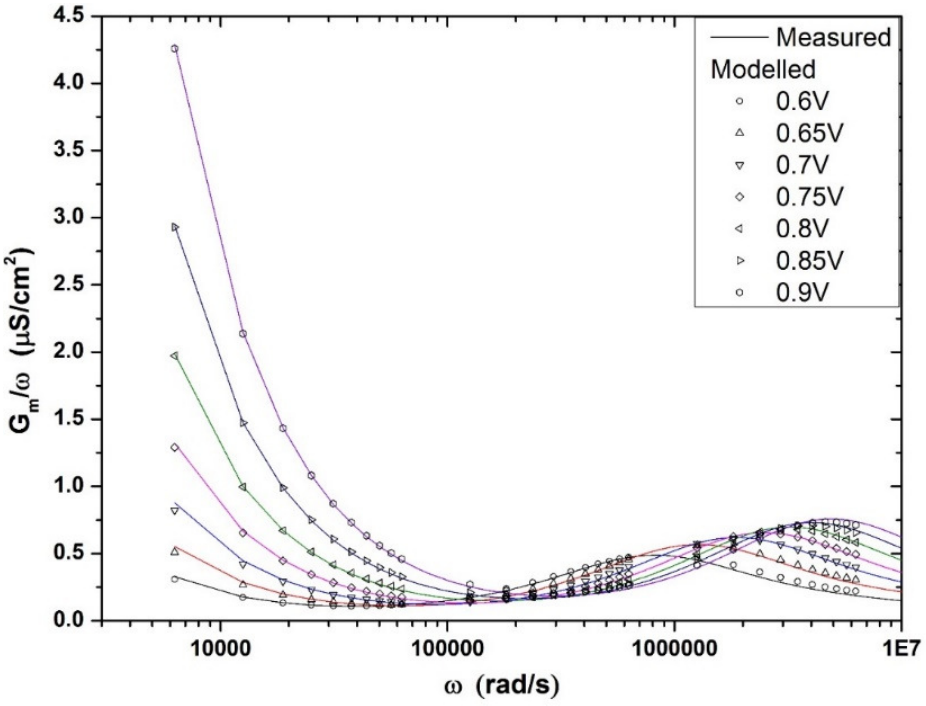


Figure 3.11: Modelled and measured Gm/w vs. w curve in inversion for sample P2.

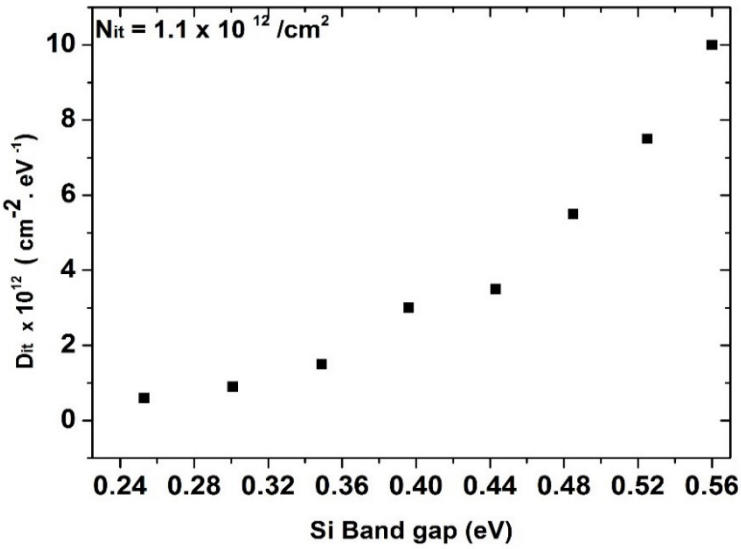


Figure 3.12: D_{it} in the upper band gap of Sample P2. Interface charge density is calculated by integrating D_{it} over the entire Si band gap. Single time constant model has been used.

3.4 Device Mobility and charge distribution profile

Experimental inversion charge mobility of the samples at room temperature, shown in Fig.3.13, is calculated from the measured drain current (I_d) vs. gate voltage (V_g) characteristics, shown in the inset of Fig.3.13, and the experimental split CV characteristics.

Peak mobilities of ~250 cm^2/ Vs and ~195 cm^2/Vs are obtained for Sample P1 and Sample P2 respectively. The mobility values for the samples appear flat at high effective field indicating the presence of high defect density at the Si/SiO_2 interface. In order to model the inversion mobility using *SCATTER*, the interface charge density in the samples is determined independently using the conductance method. Corrections for parasitic effects such as leakage current, frequency dispersion and channel resistance have been applied to the measured conductance-frequency data [17] [18].

Fig.3.14 shows the comparison of experimental and modelled inversion mobility for Samples P2. To obtain a match with the experimental device mobility different possibilities of charge distribution profile along the gate dielectric are simulated in *SCATTER* (not shown here). Distribution profile of N_{it} and N_{fix} for best-fit mobility curve for the sample is shown in inset. Si/SiO_2 interface is set as 0.0nm distance. Interface density distribution is considered to about 0.5nm into SiO_2 layer. Fixed charge defects are considered distributed at the HfO_2/SiO_2 and TiN/HfO_2 interfaces. For Sample P2, mobility modelling yields a fixed charge density of $1x10^{12}$ cm^{-2} at the HfO_2/ SiO_2 interface and $2.7x10^{12}$ cm^{-2} at the TiN/HfO_2 interface.

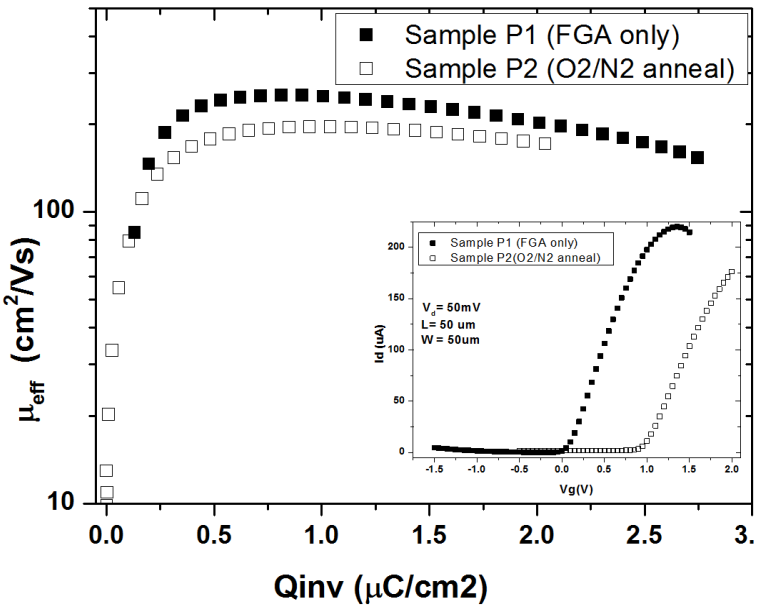


Figure 3.13: Experimental inversion charge mobility of Sample P1 and P2. Drain current (I_d) vs. Gate voltage (Vg) characteristics used in the calculation is shown in inset.

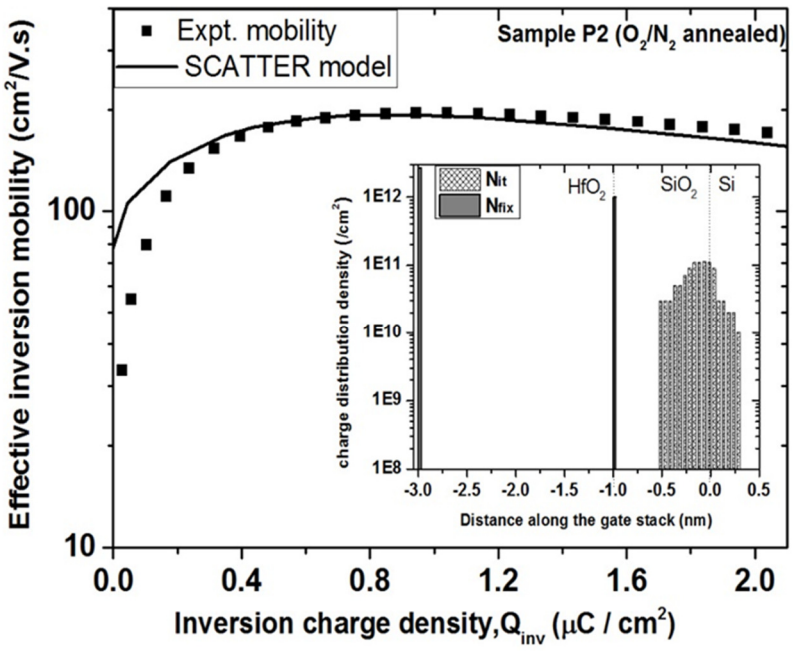


Figure 3.14: Modelled inversion mobility for Sample P2. Charge distribution profile employed for mobility modelling in SCATTER is shown in inset.

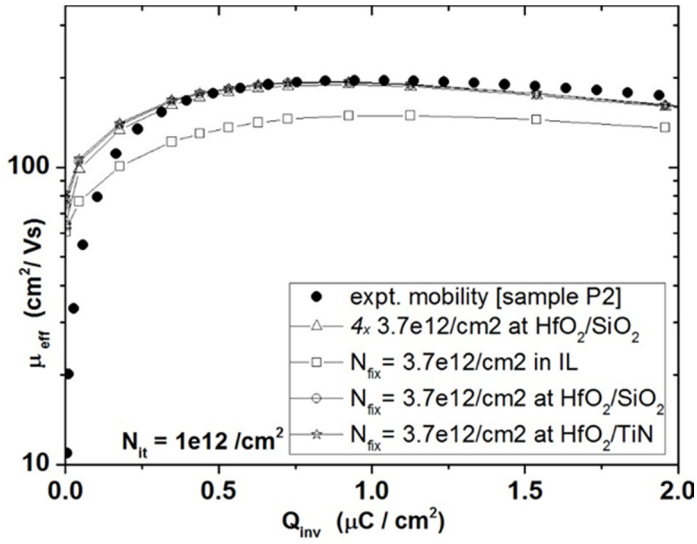


Figure 3.15: Variation in device mobility with respect to charge density positioning in the gate stack. Total N_{it} of 1x10^{12} cm^{-2} considered at substrate/SiO2 interface.

3.5 Discussion

Fig.3.15 evaluates how the position and quantity of charge traps along the depth of the gate dielectric from the substrate/IL interface affects the magnitude and shape of the mobility curve. Case of Sample P2 is examined. An interface defect density of 1x10^{12} cm^{-2} is considered at the Si/SiO_2 interface which is reflected in the flatness of the curve. Considering a total fixed charge density of 3.7x10^{12} cm^{-2} to be located within the SiO_2 IL (at -0.5nm) results in an underestimated mobility curve. This suggests that the defects are either located away from SiO_2 IL or is present in the IL with relatively low magnitude. The match obtained for the experimental mobility, shown in Fig.3.15 was possible with a trap density of 1x10^{12} cm^{-2} at the HfO_2/SiO_2 interface (at -1.0nm) suggesting a fixed charge density less than 1x10^{12} cm^{-2} to be present in the IL. This points to the charge defects being located in the HfO_2 bulk and/or at the TiN/HfO_2 interface. Influence of the fixed charge traps on inversion mobility is inversely proportional to its location from the Si channel. For a trap density 4 times the total fixed charge density considered at the HfO_2/SiO_2 interface yields only 2% degradation in peak mobility. From these results, the additional fixed charge density observed in Sample P2 is concluded to be distributed mainly in the HfO_2 and beyond towards TiN layer. Previous works have reported Post metallization anneal in oxygen ambient to result in increased oxide charge density and have suggested to be located within high-*k* bulk and/or at TiN/HfO_2 interface using first principle calculations [1] and RTN [19].

In summary, with the help of quantum mechanical mobility modelling we determined the density and distribution of fixed oxide defects in the TiN/HfO_2/SiO_2 gate stack subjected to post-metallization anneal. Subjecting the TiN/HfO_2 gate stack to O_2/N_2 PMA is shown to introduce

fixed oxide charge defects in the gate stack, concentrated mainly at the HfO_2/SiO_2 and beyond. Inversion mobility of device with PMA is seen to reduce to 78% mobility of FGA-only process due to oxygen diffusion.

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Chapter 4

ZnO Transparent Thin Film Transistors

As mentioned in the earlier chapter, carrier conduction and hence the electrical performance of TFTs, similar to that in traditional Si devices, is highly dependent on the density of localised gap states (DOS). Various methods have been developed to calculate the trap densities in TFT including Capacitance-Voltage (CV) methods [1], Field effect (FE) methods [2] [3] deep level transient spectroscopy (DLTS) [4] and photocurrent method [5]. CV method on TFTs is difficult due the thin channel layer and requires special gap-cell structures for measurement. In this chapter, to begin with, the electrical performance of the TFTs, fabricated at the University of Sheffield, UK, is characterised. In the latter part of the chapter the numerical methods and the results from the DOS calculation is explained.

4.1 Electrical device parameter extraction

The bottom-gated ZnO/Ta_2O_5 Transparent Thin Film Transistors considered in this study have a channel (ZnO) thickness of 20nm and insulator (Ta_2O_5) thickness of 90nm. The gate electrode is glass substrate coated with ITO. Aluminium (Al) is used to form the metal contacts. Electrical measurements were made with the help of Keithley 4200 semiconductor characterisation system and a cryogenic probe station.

The electrical performance parameters of the TFTs such as mobility, threshold voltage, on/off ratio and sub-threshold slope are calculated from the transfer characteristics ($I_d - V_g$) measured under ambient conditions. Fig.4.1 shows the measured transfer characteristics which is expressed in per unit area to compare the performance of transistors of different device dimensions. Comparison of drain current as a function of Over-drive voltage ($V_g - V_t$), gives a more realistic view of the ON region performance of the transistors. The dielectric constant of the gate insulator is calculated from the measured oxide capacitance (C_{ox}) which results in a dielectric permittivity value (ε_{ox}) of 19.03. From Fig.4.1, the best characteristics is obtained for the device with WxL= 300 µm x 4 µm and hence the electrical device parameter extraction for this device is explained below. The transfer characteristics of the TFT is measured at a low drain bias voltage (V_d) of about 0.1V. Low drain voltage is preferred to ensure a uniform distribution of effective field in the device.

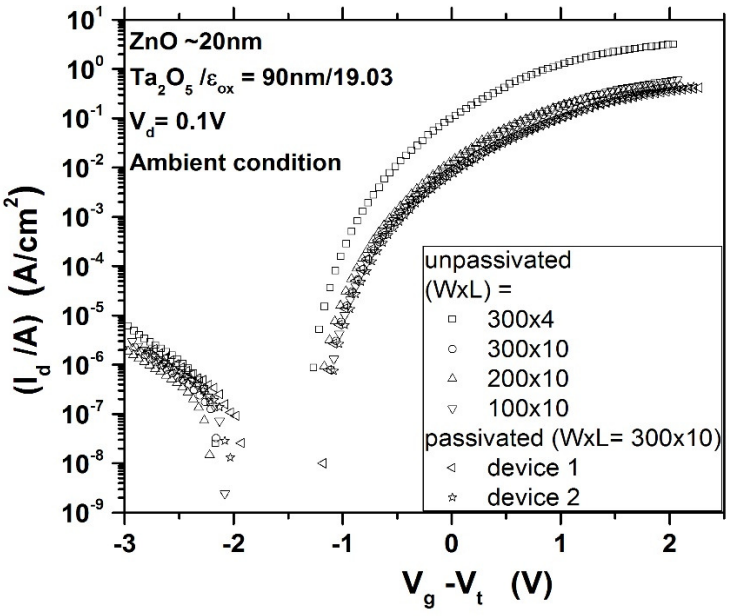


Figure 4.1: Transfer characteristics per unit area measured on transistors as a function of overdrive voltage.

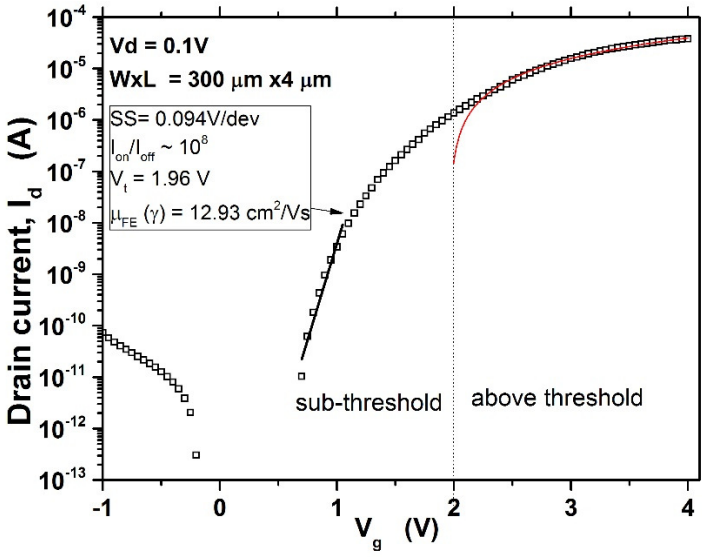


Figure 4.2: Log (I_d)-V_g characteristics and the calculated electrical device parameters. Threshold voltage (V_t) and field-effect mobility is calculated using 'gamma' method.

An on-off ratio (I_{on} / I_{off}) of ~10^8 and sub-threshold slope (SS) of 94mV/dec is calculated from the log (I_d) - V_g plot in Fig.4.2. An off current (I_{off}) in the range of 10^{-13}A is estimated for the device. I_{off} denotes the amount of drain current flowing in the device when it is in the off condition. A low I_{off} value and high on/off ratio indicate a good device. SS is defined as the amount of gate bias needed to increase the drain current by a factor of 10 and is an indicator of the switching speed of the device.

Using the MOSFET equation for drain current given in Eqn.4.1, which assumes a linear relation between the drain current and the applied gate bias, device mobility (μ_{lin}) of 14.87 cm^2/Vs is extracted from a linear fit to the $I_d - V_g$ curve (Fig.4.3). Also a threshold voltage (V_t) of 2.24V is extracted from the interpolation of the linear fit to the x-axis.

$$I_d = \frac{W}{L} C_{ox} \mu_{lin} (V_g - V_t) V_d \quad \text{..... (4.1)}$$

where C_{ox} is the capacitance per unit area of the gate insulator, and *W* and *L* are the width and length of the channel respectively.

The linear I-V relation does not hold true for TFTs and hence a more appropriate relation that considers a gate voltage dependence of device mobility i.e. field effect mobility as expressed in Eqn.4.2 is considered.

$$\mu_{FE} = \frac{\partial I_d / \partial V_g}{C_{ox} (W/L) V_d} \quad \text{..... (4.2)}$$

The V_g dependence of μ_{FE} can be explained by the energy dependent density-of-localized-states near the Fermi level [5]. As V_g increases, most localized states are filled, and more induced charges can contribute to the free carriers. The transconductance ($\partial I_d / \partial V_g$) method of mobility calculation is suggested to over-estimate the device mobility and Kishida et. al [5] suggested a 'gamma (γ)' relation between the drain current and V_g as expressed in Eqn.4.3.

$$I_d = \frac{W}{L} C_{ox} \mu_0 (V_g - V_t)^{(1+\gamma)} V_d \quad \text{..... (4.3)}$$

where μ_0 is the fitting parameter associated with the field effect mobility (μ_{FE}) and γ is related to the characteristic temperature (T_g) of the tail state distribution and is given as

$$\gamma = 2\left[\frac{T_g}{T} - 1\right] \quad \text{..... (4.4)}$$

Field effect mobility is then calculated using the relation

$$\mu_{FE} = \mu_0 (V_g - V_t)^{\gamma} \quad \text{..... (4.5)}$$

Device mobility calculated using Eqns.4.1, 4.2 & 4.5 are compared in Fig. 4.5.

The saturation mobility (μ_{sat}) of the device is calculated from the linear fitting of $I_d^{1/2} - V_g$ plot, shown in Fig.4.3, and using the relation given in Eqn. 4.6.

$$I_d = \frac{C_{ox}\mu_{sat}W}{2L}(V_g - V_t)^2 \text{ for } V_d > V_g - V_t \quad \text{..... (4.6)}$$

The maximum density of states (N_{ss}) at the substrate-insulator interface states can be estimated from the sub-threshold slope using Eqn. (4.7). The N_{ss} calculated is about 3.2e12 /cm^2.

$$N_{ss} = \left[\frac{SS\,(\log e)}{(kT/q)} - 1\right]\frac{C_{ox}}{q} \quad \text{..... (4.7)}$$

where k is the Boltzmann's constant, T is the ambient temperature (here T= 298K) and q is the electronic charge.

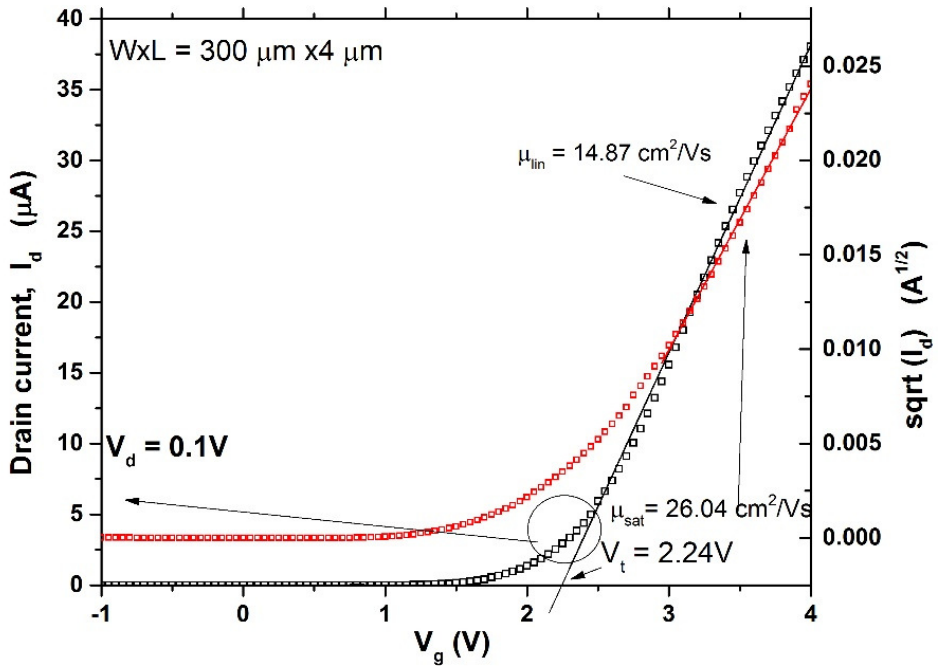


Figure 4.3: Calculation of Saturation and linear mobilities calculated from the experimental transfer characteristics. Threshold voltage (V_t) from the linear fit is also shown.

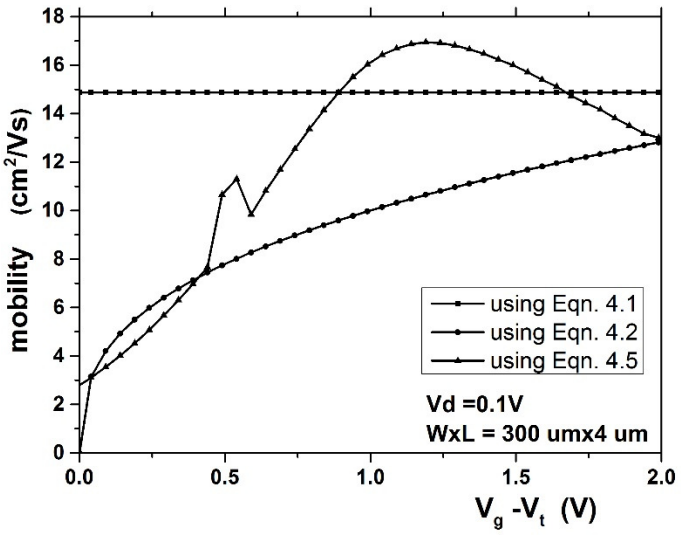


Figure 4.4: Device mobility calculated from Eqns. (4.1), (4.2) and (4.5). The kink in the transconductance curve calculated using Eqn.4.5 is because of the small kink in the I_d-V_g data that is being exaggerated during differentiation of the values.

4.2 Extraction of the Density of states (DOS) in ZnO TFT

Field effect (FE) methods employed in this study to determine the density of states is explained in the following sections.

4.2.1 DOS from Temperature dependent FE measurement

The conductivity of certain semiconductor materials are observed to be temperature dependent. This temperature dependence of conductivity is due to the movement of carriers in to the conduction band with increase in temperature which increases the density of free carriers i.e. thermal generation/activation of carriers. Based on this phenomenon of thermal activation of carriers, Schropp et al [6] developed a temperature dependent FE method to extract the distribution of gap states.

Fig.4.5 shows the measured temperature dependent transfer characteristics. A typical drain current vs. gate bias curve can be considered to be consisting of 3 sections: the above-threshold region, the sub-threshold region and the gate leakage region. All the three regions of the experimental transfer characteristics is seen to be thermally activated. Thermal activation of gate leakage current could be because of the charge trapping property of the gate insulator. A similar observation was made by Takechi et.al [7]. The positive shift in threshold voltage with decrease

in temperature is because a higher bias i.e. a higher effective field is needed to induce conduction in the device at lower temperatures.

The thermal activation energy of the drain current, i.e. the energy needed by the carriers to move from the localised tail states into conduction band, and temperature usually follow an Arrhenius relation which can be given as

$$I_d\left(V_g\right) = I_{d0} e^{\left(-E_a\left(V_g\right)/kT\right)} \quad \text{..... (4.8)}$$

where I_{d0} is the prefactor, $E_a(V_g)$ is the activation energy, *k* is the Boltzmann constant and T is temperature.

Plotting $\ln(I_d)$ vs. $1/kT$ yields the activation energy ($E_a(V_g)$) and pre-factor (I_{d0}) from the slope and intercept respectively. Activation energy, in simple terms is the energy difference between the Fermi level and the edge of the conduction band. Fig.4.6 shows the distribution of the activation energy and pre-factor values calculated from the experimental data as a function of applied gate bias. It can be observed that the activation energy drops-off fast in the lower Vg region, eventually levelling-off in the higher Vg region. It is suggested that this behaviour is because as the gate voltage is increased, the Fermi level moves closer to the conduction band edge and is pinned in the tail states due to the high density of states in band tail [7]. Thus the activation energy in the higher gate voltage region corresponds to the trap density in the tail states. In certain polycrystalline and amorphous materials the activation energy and the pre-factor is seen to follow a relation known as Meyer-Neldel (MN) rule [8] as expressed in Eqn.4.9.

$$I_{d0}\left(V_g\right) = I_{d00}\, e^{\left(A_{app} E_a\left(V_g\right)\right)} \quad \text{..... (4.9)}$$

A_{app} is the apparent MN parameter. The MN parameter is an intrinsic property of a material. Its origin is related to the energy dependence of the electron-phonon coupling of lattice to the localised states in disordered materials [9] [10]. Fig.4.7 shows the experimental E_a vs. $\ln(I_{d0})$ plot. The MN parameter value is obtained from a linear fit to the graph. From Fig.4.7 it is observed that the value of the MN parameter is different for different region of Ea and the linear fit is possible only in the higher Ea region. The A value obtained from the linear fitting of the graph that the value of the MN parameter is different for different regions of E_a and the linear fit is pos using Eqn.4.9 yields an apparent value of the MN parameter which is usually higher than the MN value of the material [6].

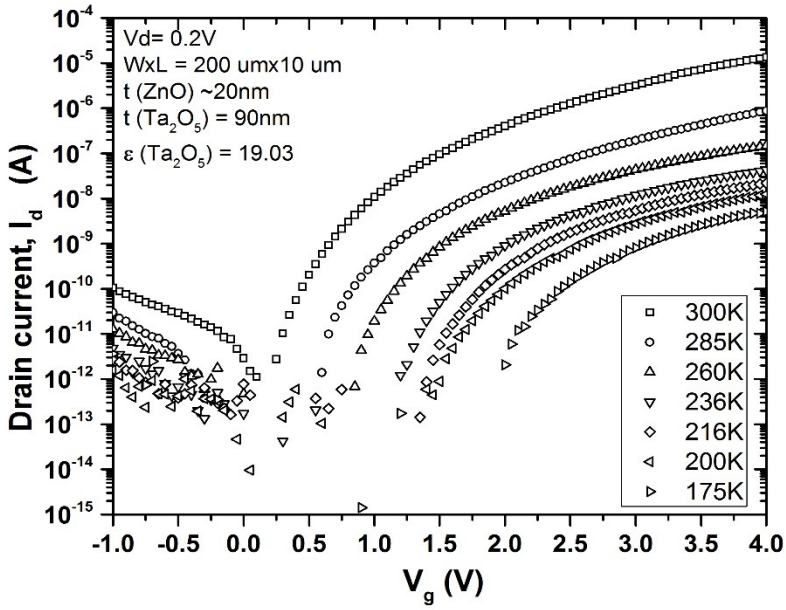


Figure 4.5: Temperature dependent transfer characteristics.

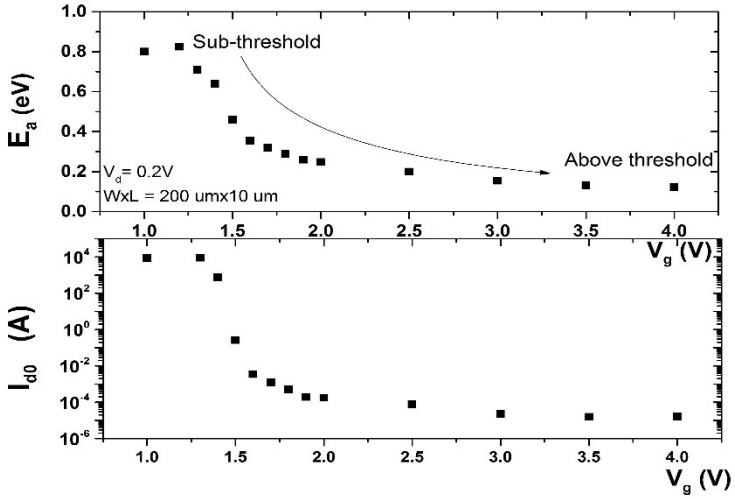


Figure 4.6: Activation energy and prefactor vs. applied gate voltage (Vg).

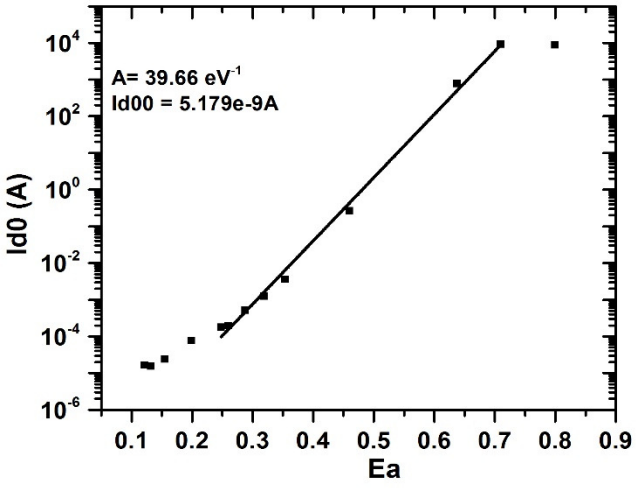


Figure 4.7: Prefactor (I_{d0}) vs Activation energy (Ea) to calculate MN parameter.

The distribution of density of states in the energy band gap is calculated using Poisson's equation by determining the band bending at the interface with respect to the externally applied gate bias. An initial potential is needed to equalise the bands and the range of applied bias that cause the band bending is expressed by the term Field voltage (V_F) given as

$$V_F = V_g - V_{FB} \quad \text{..... (4.10)}$$

The temperature dependent DOS calculation method proposed by Schropp et al [6] solves the Poisson's relation by considering the band bending as a function of field voltage at a point near to the insulator-semiconductor interface instead of calculating the band bending along the depth of the semiconductor. This solution requires less computational power to solve the Poisson equation [11] [12]. The band bending $\left(y_s\left(V_F\right)\right)$ and charge density $\left(n\left(y_s\right)\right)$ near the interface is then calculated using Eqns 4.11 - 4.13 [13].

$$\exp(\beta - A)\times y_s(V_F) - (\beta - A)\, y_s(V_F) - 1 = \frac{(\beta - A)\, t_s\, \varepsilon_{ox}}{I_{FB}\, t_{ox}\, \varepsilon_s}\left(V_F \times I_d(V_F) - \int_0^{V_F} I_d(V_F')\, dV_F'\right) \quad \text{..... (4.11)}$$

where $\beta = 1/kT$, t_s is the semiconductor thickness, ε_s is the permittivity of the semiconductor, t_{ox} is the thickness of the gate oxide and ε_{ox} is the permittivity of the gate oxide. I_{FB} is the drain current at flat band condition given as

$$I_{FB} = I_{00} \cdot \exp[(A - \beta) \cdot E_{aFB}] \quad \text{..... (4.12)}$$

E_{aFB} is the activation energy at flat bands.

The resultant charge density $n\left[y_s\left(\mathrm{V}_F\right)\right]$ is calculated using Eqn.4.13

$$n(y_s) = \frac{\varepsilon_0\, \varepsilon_{ox}}{q\, t_{ox}\, t_s} \frac{I_{FB}\{\exp[(\beta - A) \cdot y_s] - 1\}}{\partial I_d(V_F)/\partial V_F} \quad \text{..... (4.13)}$$

Fig.4.8 shows the calculated band bending, as a function of field voltage, and charge density as a function of band bending at the interface. The DOS is then calculated using Eqn.4.14.

$$DOS(E) = \left|\frac{dn(y_s)}{dy_s}\right|_{y_s = E} \quad \text{..... (4.14)}$$

Fig. 4.9 shows the calculated tail state density distribution. The DOS values from this study is compared with the DOS reported for an a-IGZO/SiO2 device [13] and for an a-Si:H TFT. Device mobilities reported for the devices compared are about 9-11cm^2/Vs for a-IGZO TFT and ~1cm^2/Vs for the a-Si:H TFT. Mobility of 3.56 cm^2/Vs (at T=300K) is calculated for our (UoS)

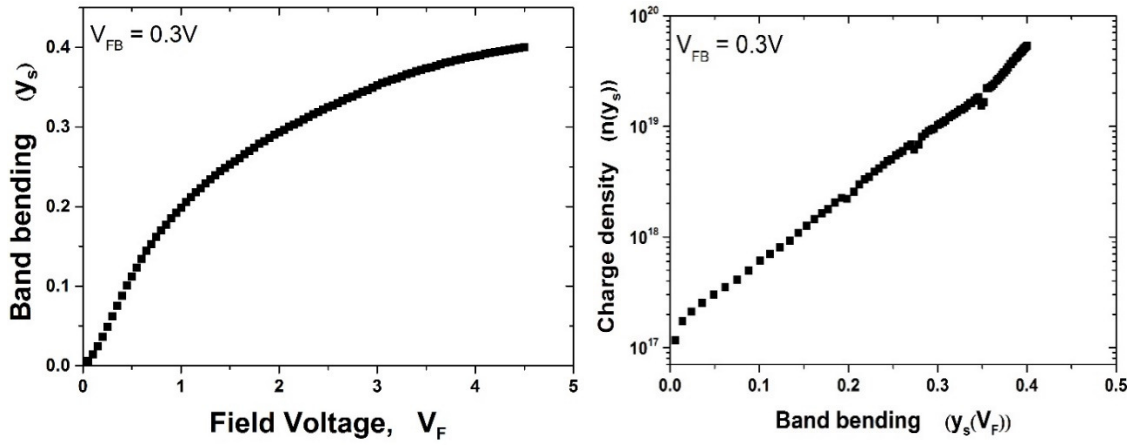


Figure 4.8: Calculated (a) band bending at the semiconductor- insulator interface as a function of field voltage and (b) charge density as a function of band bending

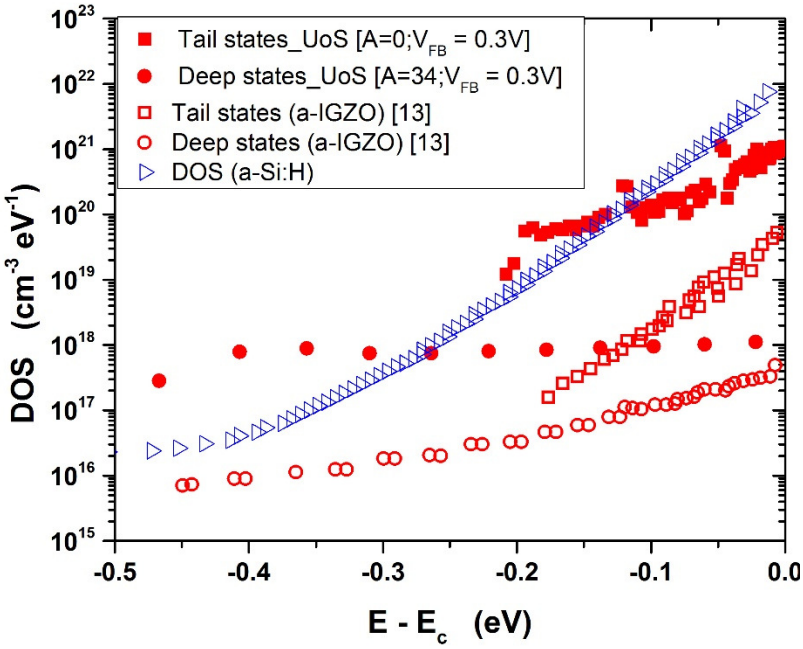


Figure 4.9: DOS in the band tail and deep level calculated using the temperature dependent FE measurement method. Calculated DOS values are compared with the values reported for a-IGZO [13] and a-Si:H.

ZnO TFT. The tail state density for the ZnO TFT falls in between that for the a-IGZO and a-Si:H devices. Accurate determination of DOS depends on the accuracy of V_{FB} determination. To calculate the flat band voltage, an initial gate bias voltage is assumed and activation energy as a function of gate bias is calculated using Eqn. 4.15. The voltage value which gives a close match

between the calculated and the experimental $E_a(V_g)$ determines the flat band voltage. Fig.4.10 shows the comparison of the calculated and experimental activation energy as a function of gate bias.

$$E_a(V_g) = E_{aFB} - \frac{I_{FB}}{I_d(V_g)\, t_s}\left(\frac{\varepsilon_s \varepsilon_0}{q}\right)^{1/2} \int_0^{y_s(V_F)} \frac{y\ \exp[(\beta - A)\, y]}{\sqrt{2\int_0^y n(y')dy'}}\, dy \qquad \text{..... (4.15)}$$

DOS calculated in the higher $E_a(V_g)$ region corresponds to the deep level defect density whereas the DOS in the lower $E_a(V_g)$ corresponds to the tail state density. The match for the experimental curve is obtained for a MN parameter (*A*) of 34eV^{-1} and V_{FB} of 0.3V. DOS in the tail state density was possible for MN parameter value of 0eV^{-1}.

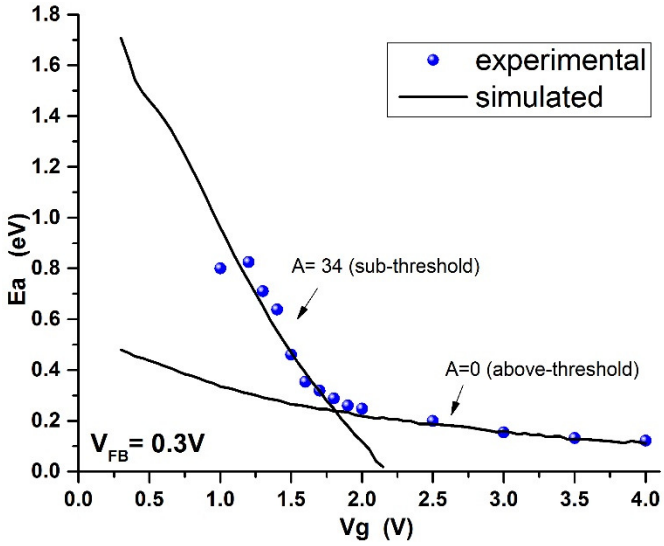


Figure 4.10: Comparison of calculated and measured E_a vs. V_g values. The flat band voltage and MN parameter for the calculated $E_a\left(V_g\right)$ is shown.

Device mobility obtained at room temperature from the temperature dependent IV measurement is only about 4cm^2/Vs which is very low as compared to the ambient condition measurement. The DOS calculation, even though it yields result that is consistent with the theory and the experimental data, it does not help to prove the reason behind the high device mobility observed for ZnO TFTs.

4.2.2 Localised tail state distribution from transfer characteristics of the TFT

Lee et. al. [14] proposed an alternate analytical method to calculate sub-gap DOS from the transfer characteristics of the TFT. In this method the electric field in the channel layer due to the applied drain and gate biases is considered and a closed form relation between the applied bias and the surface potential at the semiconductor/insulator interface is derived. Fig.4.11 shows the schematic of the bottom gated TFT being considered. n_{free} and n_{trap} are the free carrier and trap carrier densities in the semiconductor respectively. ε_s is the permittivity of the semiconductor, t_S is the thickness of the channel layer and *L* is the length of the channel.

Considering line integral form of the electric field, the 2D Poisson's equation in the channel layer can be written as

$$\oint_C \vec{E} \cdot \vec{dl} = \int_0^x E_y dx - \int_0^y E_x dy \qquad \text{..... (4.16)}$$

$$= -\frac{q}{\varepsilon_S} \int_0^x \int_0^y [n_{free} + n_{trap}] dy dx \qquad \text{..... (4.17)}$$

Assuming the conditions,

$E_x = 0 \quad at\ (x = 0)\ \ and\ E_y = 0 \quad at\ (y = t_S)$ and

$\left|E_y\right| >> \left|E_x\right|\ for\ \ V_g >> V_d$,

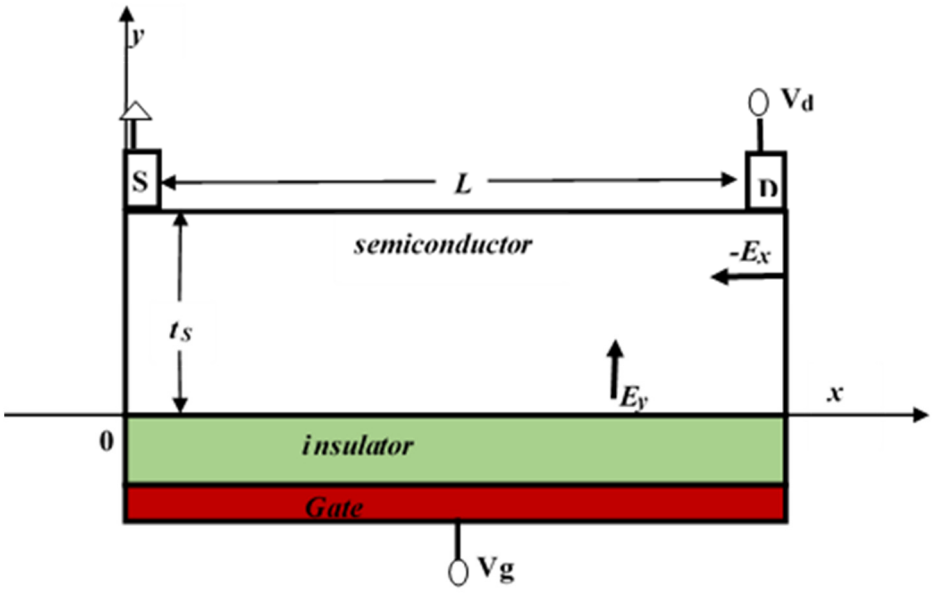


Figure 4.11: Schematic showing the direction of electric fields and parameter constants for DOS calculation.

electric field at the semiconductor-insulator interface i.e. the surface electric field (E_s) is expressed as a function of the surface potential at the interface as

$$E_y(y=0) = -\frac{\partial \varphi}{\partial y}$$

$$= \sqrt{\frac{2q}{\varepsilon_S}\int_0^{\varphi_S}[n_{free}(\varphi)+n_{trap}(\varphi)]\,d\varphi} = E_S \qquad \text{..... (4.18)}$$

Again, using Gauss's law, E_S is defined as

$$E_S = \frac{Q_{free}+Q_{trap}}{\varepsilon_S} \qquad \text{..... (4.19)}$$

where Q_{free} and Q_{trap} are the free charge and trapped charge densities at the localised states [15]. Now, the charge neutrality condition at the interface is expressed as

$$C_{ox}(\mathrm{V_g} - \mathrm{V_{FB}} - \varphi_\mathrm{S}) = \varepsilon_S E_S + Q_{it} \qquad \text{..... (4.20)}$$

where V_{FB} is the flat band voltage and $Q_{it}\,(=C_{it}\varphi_S)$ is the interface charge density. C_{it} is the interface capacitance calculated from the sub-threshold slope of the transfer characteristics. From Eqns 4.19 and 4.20:

$$Q_{free}+Q_{trap} = C_{ox}[V_g - V_{FB} - (1+\frac{C_{it}}{C_{ox}})\,\varphi_S] \qquad \text{..... (4.21)}$$

Assuming the band mobility (μ_0) value as the maximum calculated field effect mobility, the free charge density (Q_{free}) is calculated as a function of the applied bias (V_g) using Eqn.(4.22) as [16],

$$Q_{free}(V_g) = \frac{I_d(V_g)}{V_d \mu_0 (W/L)} \qquad \text{..... (4.22)}$$

And the free carrier density is then approximated as a function of V_g using

$$n_{free}(V_g) \approx \frac{Q_{free}^2(V_g)}{\varepsilon_S kT} \qquad \text{..... (4.23)}$$

Distribution of the φ_S as a function of V_g is then computed from the expression for free carrier density as a function of φ_S using the relation

$$n_{free}(\varphi_s) = N_C \exp[(E_{F0} - E_c + q\varphi_s)/kT] \qquad \text{..... (4.24)}$$

where N_C is the density of states for free carriers, E_C is the conduction band edge, E_{F0} is the Fermi energy at flat band. Using the condition that at flat band, there is no band bending at the interface i.e. $\varphi_s = 0$,

$$E_{F0} - E_C \approx kT \ln[n_{free}(\varphi_s = 0) / N_C] \quad \text{..... (4.25)}$$

Thus, using Eqns 4.24 & 4.25, variation of surface potential with respect to V_g can be computed as

$$\varphi_S = \frac{2kT}{q} \ln[\frac{Q_{free}(V_g)}{\sqrt{N_C \varepsilon_S kT}}] + \frac{(E_C - E_{F0})}{q} \quad \text{..... (4.26)}$$

Fig.4.12 shows the transfer characteristics of the TFT being considered. Calculated free carrier density as a function of V_g is shown in Fig.4.13. Fig.4.14 shows the calculated φ_S and $E_F - E_C$ as a function of V_g.

Using the surface potential distribution and free carrier density, the trap carrier density as a function of surface potential is calculated using

$$n_{trap}(\varphi_S) = \frac{\varepsilon_S}{2q} \frac{\partial E_S^2}{\partial \varphi_S} - n_{free}(\varphi_S) \quad \text{..... (4.27)}$$

Subsequently, the effective subgap trap density $N_{subgap}(\varphi_S)$ is calculated using

$$N_{subgap}(\varphi_S) \approx \frac{\partial n_{trap}(\varphi_S)}{\partial \varphi_S} \quad \text{..... (4.28)}$$

And as shown in Fig.4.16, the density of tail states and its characteristics energy is calculated using

$$N_{tail}(E_F) = N_{tc} \exp[(E_F - E_C) / kT_t] \quad \text{..... (4.29)}$$

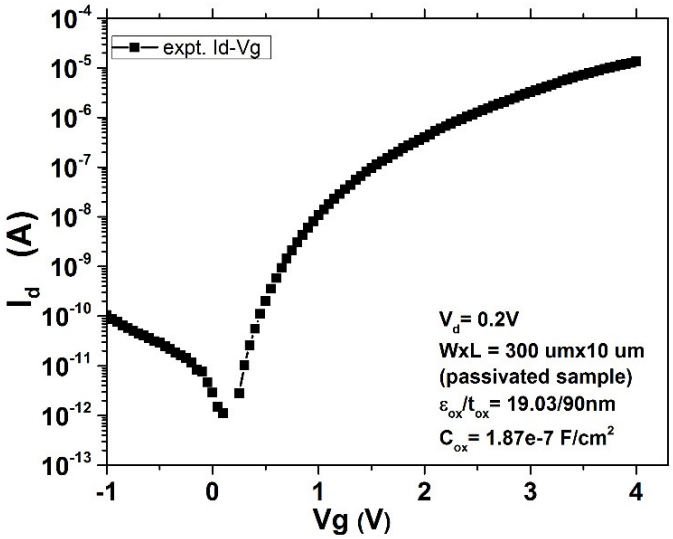
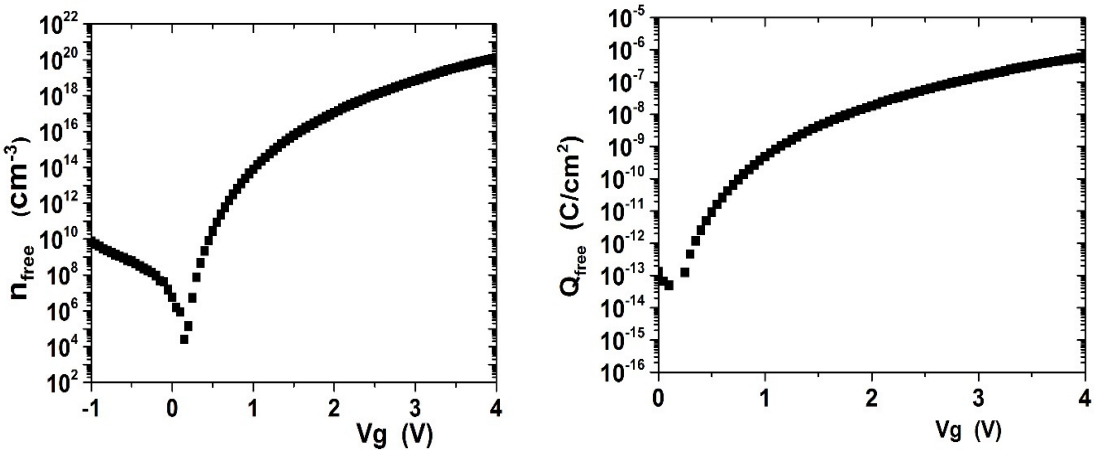


Figure 4.12: Transfer characteristics measured at 300K as part of the low temperature IV measurement. The maximum field effect mobility (at Vg = 4V) is calculated as 3.71cm2/Vs.



(a) (b)

Figure 4.13: Calculated (a) free carrier density and (b) charge density vs. Vg.

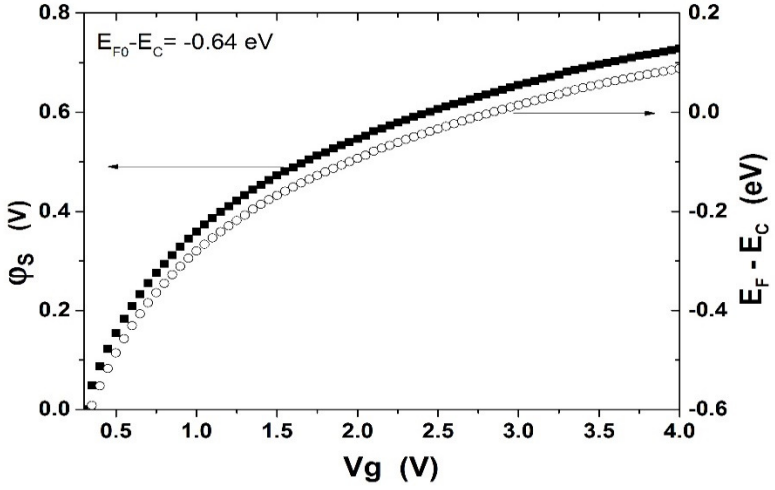


Figure 4.14: Correspondence of surface potential (ϕ_S) and $(E_F - E_C)$ with V_g .
$E_F = E_{F0}(at\ \varphi_S = 0)$

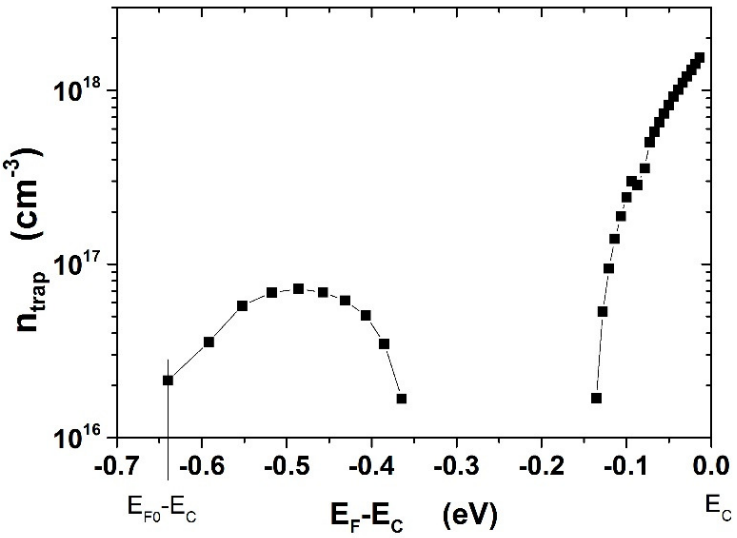


Figure 4.15: Calculated trap density distribution in the energy gap.

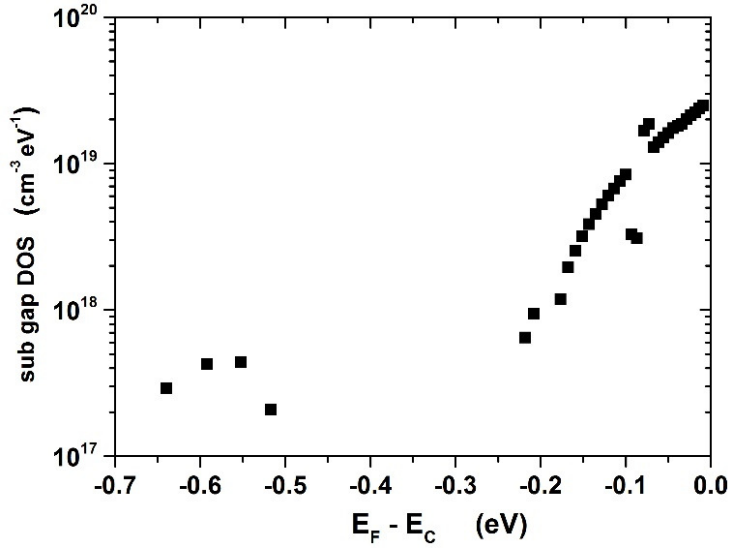


Figure 4.16: Calculated sub gap DOS as a function of $(E_F - E_C)$

From the above calculations, the value obtained for tail state density, N_{tc}, is ~2.5e19, from the intercept of the DOS distribution, and from the slope of the DOS distribution a value of 5.77meV is calculated for the characteristic energy of tail states, kT_t. Table 4.1 summarises the key parameter values obtained from calculations.

Parameter		Value	Units
Band Mobility, μ_0 (at Vg= 4V)		3.71	cm^2/Vs
Free carrier density, n_{free} (at Vg= 4V)		1.2×10^{20}	cm^{-3}
Free charge density, Q_{free} (at Vg= 4V)		6×10^{-7}	C/cm^2
Surface Potential, φ_S $(at\ E_F = E_C)$		0.64	V
Trap carrier density, n_{trap}	$(at\ \varphi_S = 0)$	2.1×10^{16}	cm^{-3}
	$(at\ E_F = E_C)$	1.9×10^{18}	
Sub-gap density of state (DOS) $(at\ E_F = E_C)$		2.75×10^{19}	$cm^{-3}eV^{-1}$

Table 4.1: Summary of the parameter values obtained from calculations using the Localised tail state distribution method.

From literature, for a typical a-Si TFT device with $\mu_{FE} \sim$ 1.2 cm^2/Vs, the kT_t value from analytical calculations is ~29meV and, for an a-IGZO TFT with $\mu_{FE} \sim 10$ cm^2/Vs the value for the characteristic tail state energy is ~20meV [18-19]. For the ZnO device reported above, the field effect mobility is about 3.7 cm^2/Vs, which falls in between the mobility values of the a-Si and a-IGZO devices. Based on the analytical results gathered from literature, the characteristic tail state energy value of the ZnO TFT is thus expected to be between 20 and 30meV. Also, the temperature of operation considered in order to satisfy the condition that the tail state energy is higher than thermal energy ($kT_t > kT$) so that the free carrier density is less than the density of carriers in the tail states $(n_{free} < n_{trap})$, is different for a-Si and the disordered oxide semiconductor TFTs. In order to determine the information on gap states accurately, the above condition needs to be true. From literature, where the tail state distribution parameters have been retrieved using the transfer characteristics method, the measured data considered for analytical calculations has been chosen keeping this condition in mind. For DOS calculation in a-Si TFTs the transfer-characteristic data at 300K is chosen [14] whereas in the case of a-IGZO TFT, this method is applied to the data at 77K [17]. Thus to employ this analytical method of DOS calculation, it is essential to know beforehand the temperature at which the condition $kT_t > kT$ is satisfied. In this study the temperature at which the above condition is satisfied is not known

previously and as shown in Table 4.1, for the IV data considered here, the $n_{free} < n_{trap}$ condition is not satisfied. This method can be adopted to validate the DOS calculated using an alternative method, given that the conditions of temperature and free carrier density are satisfied, but otherwise the calculation would result in incorrect DOS parameter values.

4.3 Conclusion

The electrical device parameters of the ZnO device fabricated in-house has been extracted. However, the density of states calculations did not yield good results. The device is seen to have a large variation in transfer characteristics in temperature dependent measurements. Since the FE methods used is highly sensitive to the variation in temperature, this behaviour affects the density of states determination through inaccurate flat band voltage and surface potential profiles. The inaccuracy undoubtedly will affect further calculations and that is evident in the results obtained. Also, in this study, the temperature at which the condition $kT_t > kT$ is satisfied is not known beforehand and it has not been possible to obtain the measurement of the ZnO devices at lower temperatures. Hence the method of DOS from transfer characteristics has not helped to retrieve the DOS parameters accurately either.

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Chapter 5

Conclusion and Future Work

In this thesis, the basic physics regarding the trap density characterisation and its effect on device mobility in high-*k* meal gate (HKMG) MOSFETs and ZnO TFTs and the results on some initial characterisation exercises carried out are presented.

The electrical parameters extracted for the HKMG samples agree with the values from literature. However, conductance measurement results of these devices indicate the presence of parasitic elements which has affected further analysis to extract the interface density distribution. However, with the help of the in-house simulators and the experimentally retrieved parameter values, this study has attempted to identify the spatial distribution of the charge traps and explain the degradation in mobility in HKMG device with post-metallisation anneal. In-line with literature, greater influence on the inversion charge carriers is noted from the presence of fixed oxide traps near the TiN/HfO2 interface, presumably from the oxygen anneal process subjected on the device.

In the study on ZnO TTFT device, the electrical parameters have been extracted successfully. The large shift/swing observed in the temperature dependent transfer characteristics have a detrimental effect on the density of states calculations. For this study, which mainly aims to understand the conduction mechanism responsible for the high device mobility, it is crucial to have devices that are stable under bias conditions. Also, during the experiment stage, degradation in the devices in the short span of few days was noted. This would point to inferior quality of the constituent materials which could be a reason behind the poor performance when measured under varying temperature values.

In terms of future work,

- For the HKMG study, in order to ascertain the validity of the fixed oxide charge density value from simulations, obtaining accurate values for the other variables particularly, the interface density is important. Alternate experimental methods such as Charge pumping could be tried to determine this parameter or modelling the gate capacitance and conductance might prove useful.
- Further, this work does not consider the influence of bulk oxide traps in high-*k* MOS. It is assumed that the influence of these trap charges is negligible on the inversion carriers but to provide an exhaustive study it will be beneficial to study this element of the charge trap as well.

- Also, at this stage of the work, to extract the electrical parameters, the fixed oxide charges are assumed to be located near the substrate/gate oxide interface. This could be further extended to include a charge distribution profile in SP-Scatter.
- For the ZnO TFT study, in order to determine accurate density of states profile, alternate methods could be employed but that in turn will require special device structures and/or biasing under light/current stress. More importantly, success of this study depends heavily on the stability and reliability of the devices. Thus it is imperative to fabricate devices that will be stable under the various biasing conditions.
- Also, exploring the presence and influence of oxide traps in Ta_2O_5 will help to rule out the cause for large swing in the measurements.
- Another important point to note in the ZnO TTFT study is that the current methods available to calculate DOS is predominantly adapted to Si-based devices. The composition and behaviour of composite materials like ZnO is different from Si and hence needs appropriate methodology and assumptions that fit the properties of these materials.