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Planar InAs avalanche photodiodes for infrared sensing: Towards a true solid state photomultiplier

By:

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A thesis submitted in partial fulfilment of the requirements for the degree of
Doctor of Philosophy

The University of Sheffield
Faculty of Engineering
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Submission Date

5th August 2016

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Acknowledgements

I would like to express my sincere gratitude to Prof. Chee Hing Tan for his continuous support throughout my PhD. For your patience, inspiration, guidance, and financial support I am truly grateful. I am fortunate to have met Dr. Jon Willmott whose guidance over the last 4 years has greatly enriched my experience. I would like to thank Prof. John David for many enjoyable discussions, and finding time to share his knowledge. I am in debt to Dr. Ian Sandall for teaching me the art of fabrication and characterisation. I would like to thank Dr. Jo Shien Ng, and past and present members of the Impact Ionisation Group for the useful discussions, support and friendship most notably from Drs, Zhou, Meng, Dimler, Kerr, Hobbs, Richards, Gomez, Green, J. Xie, S. Xie, Cheong and Auckloo.

I would like to express gratitude to Dr. Ken McEwan from DSTL and LAND Instruments for funding this project and providing industrial relevance.

This work would not have been possible without the National III-V Centre, with a special thanks to Dr. Andrey Krysa for growing InAs wafers, and also Dr. Ken Kennedy, Dr. Rob Airy and Saurabh Kumar for fabrication advice. I would like to thank Prof. Russell Gwilliam for many useful discussions and for enabling access to the Ion Beam Centre at the University of Surrey. I would like to thank all the EEE staff, particularly Ian Wraith and Stephen Dorward, for enabling this work to be carried out, and keeping the department running smoothly.

The last four years have been particularly enjoyable as it has been my good fortune to share them with Gemma, who has balanced my academic work with many fond memories of Sheffield. Finally, I would like to thank my family and friends for their unwavering support throughout this time.

Abstract

Planar InAs avalanche photodiodes (APDs) are reported as low noise, high gain photon detectors operating across the electromagnetic spectrum from 1.5 to 3.5 μm . This work includes a study of post-growth selective area doping techniques in InAs required for forming planar junctions, through to developing the first planar and lateral InAs APDs to realise high gain.

Be ion implantation and annealing are developed for selective area P-type doping InAs. An implantation and annealing procedure was optimised to maximise Be activation and recovery, whilst minimising Be diffusion. A planar fabrication procedure was developed and InAs planar photodiodes were characterised with high uniformity and low surface leakage achieving a detectivity of $6.08 \times 10^8 \text{ cmHz}^{-1/2}\text{W}^{-1}$ at room temperature.

InAs APDs were fabricated using a planar fabrication process. The activation energy of the bulk and surface leakage components of the dark current were analysed to determine the dominant leakage mechanisms. Utilising an optimised structure to minimise tunnelling current, a record high gain in excess of 300 was achieved at -26 V at 200 K. The maximum gain was limited by breakdown, and the breakdown mechanism was found to be due to an unusual thermal runaway effect within an electric field hotspot at the planar junction edge. To mitigate the formation of electric field hotspots, planar APDs with guard rings were designed and characterised. Planar APDs with optimised guard ring placements were characterised with lower dark current near breakdown, and an increased breakdown voltage at 200 K compared to unguarded APDs.

The gain limitations of InAs APDs utilising a conventional structure are discussed. To overcome such limitations a novel lateral APD structure was proposed. A range of lateral APD structures were simulated to evaluate the evolution of a lateral electric field that may lead to enhanced lateral gain. N-type selective area doping using Si implantation and annealing were developed, and a range of lateral APD structures were fabricated utilising Be and Si implantation and annealing. Lateral APDs were characterised and an optimised structure was identified. Finally a discussion of the recommended work to be carried out on InAs APDs is presented.

Publications

Journal papers:

X. Zhou, M. J. Hobbs, **B. S. White**, J. P. R. David, J. R. Willmott, and C. H. Tan, "An InGaAlAs-InGaAs Two-Color Photodetector for Ratio Thermometry," *IEEE Transactions on Electron Devices*, vol. 61, pp. 838-843, 2014.

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C. H. Tan, I. Sandall, X. Zhou, **B. S. White**, M. Hobbs, S. Zhang, A. B. Krysa and J. P. David, "Mid-IR detectors at Sheffield," *UK compound semiconductors conference*, Sheffield, UK, July 2013.

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X. Zhou, I. Sandall, **B. S. White**, A. B. Krysa, J. R. Willmott and C. H. Tan, "InAs photodiode for 3.43 μm radiation thermometer," *41th International Symposium on Compound Semiconductors (ISCS)*, Montpellier, France, May 2014.

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B. S. White, X. Zhou, I. Sandall, C. H. Tan and J. R. Willmott "Remote temperature sensing using InAs photodiodes" in *2014 IEEE Photonics Conference (IPC)*, San Diego, California, USA, October, 2014.

B. S. White and C. H. Tan “Novel lateral cascaded InAs avalanche photodiodes for infrared sensing: Towards a true solid state photomultiplier” Defence and Security symposium, Defence Academy of the United Kingdom, Shrivenham, UK, November, 2016.

List of symbols

A	Area	MWIR	Mid-wavelength infrared
a	Tunnelling current fitting parameter	n	Ideality factor
APD	Avalanche photodiode	N_A	Acceptor concentration
AR	Anti-reflective	N_D	Donor concentration
b	Recombination constant	NEP	Noise equivalent power
BIB	Blocked impurity band	n_i	Intrinsic carrier concentration
C-V	Capacitance-voltage	N_i	Unintentional doping concentration
D^*	Detectivity	N_{ii}	Impact ionisation frequency
d_{arc}	Thickness of the anti-reflective coating	NIR	Near-infrared
d_e	Dead space	PDF	Probability density function
d_{eff}	Effective device thickness	PMF	Probability mass function
D_n	Diffusion coefficient of electrons	PMT	Photomultiplier tube
D_p	Diffusion coefficient of holes	P_{opp}	Optical power
DUT	Device under test	QWIP	Quantum well infrared photodetector
E_g	Band gap energy	R	Resistance
E-H	Electron-hole	R_{opp}	Reflectance
E_{th}	Threshold energy	R_p	Projected range
F	Excess noise factor	RPL	Random Path Length
f	frequency	R_{res}	Responsivity
G_{opp}	Optical generation rate	R_s	Shunt resistance
h	Planck constant	RTA	Rapid thermal anneal
\hbar	Reduced Planck constant	S	Device average collection efficiency
HH	Heavy hole	SAM	Separate absorption and multiplication
I	Current	SRH	Shockley Reed Hall
I_A	Imaginary current	SIMOX	Separation by implantation of oxygen
I_n	Noise spectral density	SIMS	Secondary ion mass spectroscopy
I_{nAPD}	Noise spectral density of an amplified current	SWIR	Short-wavelength infrared
I_{ph}	Photocurrent	T	Absolute temperature

I-V	Current-voltage	TRIM	Transport of Ions in Matter
J_0	Saturation current density	v	Speed of light in a vacuum
J_b	Bulk current density	V_A	Test signal voltage
J_{diff}	Diffusion current density	V_{bi}	Built in potential
	Generation recombination c		
J_{GRBB}	Current density due to band to band transitions	V_{Ph}	Photovoltage
	Surface leakage per unit length	V_{PSD}	Phase sensitive voltage
J_s	Trap assisted generation recombination current	w	Multiplication region width
J_{SRH}	Total primary dark current density	α	Local electron impact ionisation coefficient
J_{tot}	Current density-voltage	α^*	Enabled impact ionisation coefficient
J-V	Ratio of the electron to hole impact ionisation coefficient	α_{opp}	Optical absorption coefficient
k	Boltzmann constant	β	Local hole impact ionisation coefficient
k		ε_r	Relative permittivity
LH	Light hole	η	External quantum efficiency
LIA	Lock-in amplifier		Refractive index of the anti-reflective coating
L_n	Diffusion length of electrons	η_{ARC}	
L_p	Diffusion length of holes	θ	Phase
LWIR	Long-wavelength infrared	λ_c	Cut-off wavelength
M	Avalanche gain	ξ	Electric field
m^*	Effective mass	τ_{eff}	Effective carrier lifetime
m_e	Electron effective mass	ω	Angular frequency
m_h	Hole effective mass	μ	Average
MIS	Metal insulator semiconductors		

1 Introduction

Light detection and measurement are powerful tools for non-destructive analysis, high speed communication, imagery and video. Semiconductors provide an excellent medium for facilitating light detection for three key reasons. 1) Semiconductors are highly sensitive to light as photo-generated carriers are not readily thermalized, or reemitted as photons, but induce a significant change in a variety of the semiconductor's electronic properties that can be accurately measured. 2) The band gap and band diagram of a device can be engineered to optimise performance 3) High manufacturability has enabled micro-scaling and mass production with very low costs and easy integration with read-out electronics for digitisation and further processing.

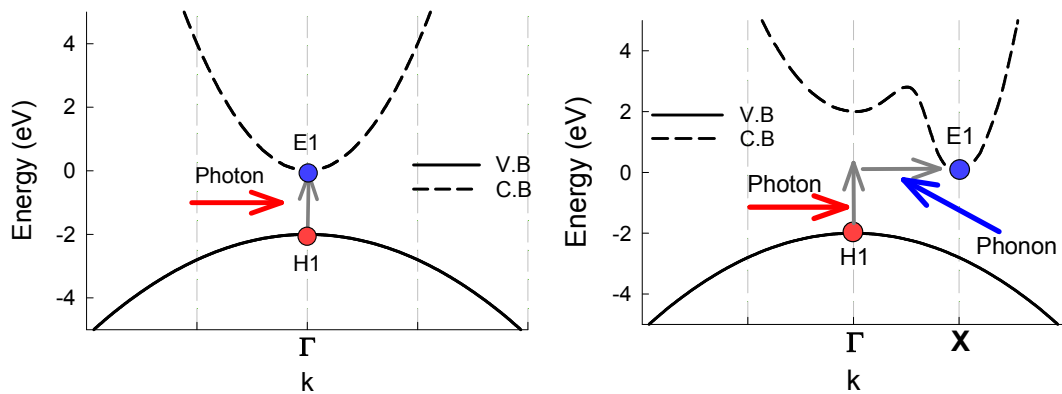


Figure 1.1 E-k diagrams of optical generation in a direct (left) and indirect (right) semiconductor

The detection of light using a semiconductor is facilitated through the absorption of a photon's energy to excite an electron to a higher energy state. Within a direct bandgap semiconductor, the absorption of a photon excites an electron directly from the valence band (V.B) to the conduction band (C.B) creating an electron-hole (E-H) pair as shown in Figure 1.1. Making use of the relatively long carrier lifetime in semiconductors, various devices have been designed to extract the photo-generated E-H pair facilitating the detection of light.

No energy states exist within the bandgap of a semiconductor, and therefore photons carrying less energy than the fundamental bandgap energy cannot be absorbed. The absorption edge of a semiconductor is referred to as the cut-off wavelength. As bandgap energy of a semiconductor also has a strong inverse relationship with the magnitude of the thermally generated noise of the detector, detector performance is optimised using a semiconductor with a cut-off wavelength equal the longest wavelength required for

detection. However, the design of a photon detector also requires the consideration of additional parameters including the optical absorption coefficient, manufacturability, uniformity, cost and electronic properties of the semiconductor. A brief review of common semiconductor materials and photon detectors is presented.

1.1 Semiconductors used in photon detectors

Unrivalled manufacturing, maturity and cheap processing costs enable Si detectors to dominate applications from visible to the near infrared (NIR) sharing the largest proportion of the detector market in terms of volume. However, Si has an indirect bandgap due to the minima of the conduction band and the maxima of the valence band occurring at different vectors of crystal momentum, k , within the first Brillouin zone as shown in Figure 1.1. To conserve energy and momentum during the absorption of a photon near the band edge of an indirect semiconductor, a third particle, such as a phonon, is required to accommodate the difference in crystal momentum. The three particle process has a significantly lower probability of occurring compared to a direct band to band transition, and causes indirect bandgap semiconductors to display a low optical absorption coefficient near the band edge. To maintain high quantum efficiency, indirect bandgap semiconductors require a greater length of material to achieve high optical absorption. However, the thicker optical absorption regions increase the carrier transit time resulting in a lower device bandwidth. Indirect bandgap semiconductors are therefore not well suited as high performance photon detectors. Ge also suffers from an indirect bandgap, however, the bandgap is narrower compared to Si, and Ge detectors provides useful response out to 1.6 μm while also benefiting from mature manufacturing.

Although III-V semiconductors are more expensive and less mature than elemental semiconductors, many III-V semiconductors have a direct bandgap. The electron transport of III-V semiconductors are also significantly greater than elemental semiconductors allowing for further improvements to the detector bandwidth. For example, the electron saturation velocity of Si is $1 \times 10^7 \text{ cms}^{-1}$ [1] while for InGaAs the peak saturation velocity is $2.9 \times 10^7 \text{ cms}^{-1}$ [2]. Epitaxial growth techniques for III-V semiconductors can provide layered III-V semiconductors with different bandgap energies to form heterojunctions for advanced detector optimisation to improve responsivity, speed and noise. The relationship between lattice constant and the bandgap energy of III-V semiconductors is shown in Figure 1.2 [3].

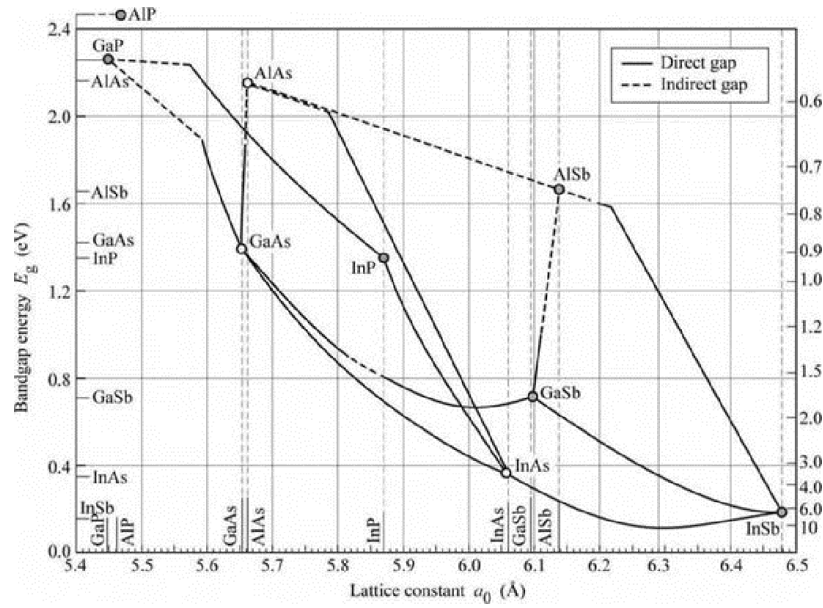


Figure 1.2: The bandgap energy and lattice constant of III-V semiconductors at room temperature [1]

Lattice match growth of III-V semiconductors to a binary substrate is required to maintain high crystal quality, and commercial III-V detectors are generally fabricated with $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, InAs or InSb absorption regions to provide cut off wavelengths of 1.7, 3.5 and 5.5 μm respectively [4]. $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ grown lattice matched to InP is one of the most mature III-V semiconductors covering telecommunications wavelengths. The intrinsic carrier concentration and minority carrier lifetime of semiconductors are highly important parameters for discussing the detector performance as they govern the magnitude of the thermally generated noise, as discussed in section 3.1. The minority carrier lifetime of intrinsic $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ at 300 K is $\approx 10 \mu\text{s}$ and $\approx 10 \text{ns}$ when doped P or N-type at $1 \times 10^{18} \text{cm}^{-3}$ [5]. The relatively long minority carrier lifetime and low intrinsic carrier concentration of $\approx 5 \times 10^{11} \text{cm}^{-3}$ [6] enables $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ detectors to be operated at room temperature with acceptable levels of thermally generated noise. InAs is utilised less extensively with comparably few commercial vendors. InAs has a bandgap of 0.35 eV at 300 K generating a large intrinsic carrier concentration of $\approx 1 \times 10^{15} \text{cm}^{-3}$. Although InAs detectors can be operated at room temperature, many applications require InAs detectors to operate at low temperatures to suppress the thermally generated noise to an acceptable level. Operating InAs detectors at a temperature of 200 K using Peltier coolers is usually sufficient to suppress thermal noise to an acceptable level. The intrinsic carrier concentration of InAs reduces to $\approx 7 \times 10^{12} \text{cm}^{-3}$ at 200 K and a minority carrier diffusion length of 1 μm in slightly N-type InAs at 200 K has also been reported [7]. InSb detectors are considered to be a mature technology, however, they require significant cooling due to the narrow bandgap of 0.18 eV at room temperature. InSb detectors are often operated at $\approx 80 \text{K}$ [6] with a minority carrier

concentration of $3 \times 10^9 \text{ cm}^{-3}$ at 77k. Lattice mismatched growth using sophisticated buffer layers has yielded detectors with acceptable crystal quality and cut-off wavelength between those covered by the lattice matched growth. Commonly grown lattice mismatched materials are extended InGaAs for 2.2 to 2.8 μm [8] and InAsSb for wavelengths $> 5.5 \mu\text{m}$ [9].

The II-VI semiconductor family has high potential for photon detectors as the band gap of the ternary alloy of CdTe and HgTe can be tuned to span across the short-wavelength infrared (SWIR) to long-wavelength infrared (LWIR) spectrum with only a 0.3 % increase in the lattice constant [10]. The distribution and production of HgCdTe is largely controlled by defence associates limiting the free study and publication. It is understood that there are major growth and fabrication challenges preventing HgCdTe from dominating the infrared detector market. Lattice matched CdZnTe substrates are many times the cost of III-V substrates while also only being a fraction of the size [10]. Non-lattice matched growth on Si substrates has been developed [11], however, the epitaxially grown crystal has significantly higher defect densities and suffers from thermal expansion mismatch issues. The strong dependence of band gap energy, thus the cut-off wavelength, on mercury composition causes uniformity issues with very high composition tolerances required to meet the demands of modern applications [12]. Growth and fabrication of HgCdTe is further complicated by the weak Hg bond which dissociate at low temperatures leading to high concentration of Hg vacancies at typical processing temperatures [13]. Consequently, production of HgCdTe is not suited to large scale manufacturing, and its use is limited to applications where the best performance possible is paramount, regardless of cost.

In addition to interband optical absorption, alternative electron transitions can be detected across Schottky barriers [14], metal insulator semiconductors (MIS) [15], blocked impurity band (BIB) [16], and quantum wells [6]. Although most detection methods cannot yet compete against the performance of optimised interband detectors, they provide compelling options for spectral tuning and can be implemented in mature, cheap, wide bandgap semiconductors. Two of the most promising detectors are quantum well infrared photodetectors (QWIPs) [17] and detectors made from type-II superlattice materials [18]. Both are typically implemented from III-V semiconductors with layer thickness comparable to the de Broglie wavelength of the carriers. Confinement of the carriers in one or more direction modifies the wave function, density of states and dispersion. Most structures are designed to operate across the mid-wavelength infrared (MWIR) or LWIR spectrum as competitors against interband HgCdTe photodetectors. In addition providing growth on a cheap large area substrate, quantum well detectors have a low intrinsic carrier concentration and reduced tunnelling current due to the higher effective electron mass. Furthermore, type

CHSH and CHLH Auger recombination is reduced in type-II superlattice materials as the heavy hole (HH) and light hole (LH) bands are split reducing the number of available transitions [19]. A schematic diagram of CHSH and CHLH Auger recombination are shown in Figure 1.3 with the schematic diagram of a type-II superlattice also shown. CHSH and CHLH Auger recombination transitions are reported to be the dominant recombination mechanism limiting the minority carrier lifetime, thus increasing thermally generated noise, in narrow bandgap semiconductors such as InAs, InSb and HgCdTe.

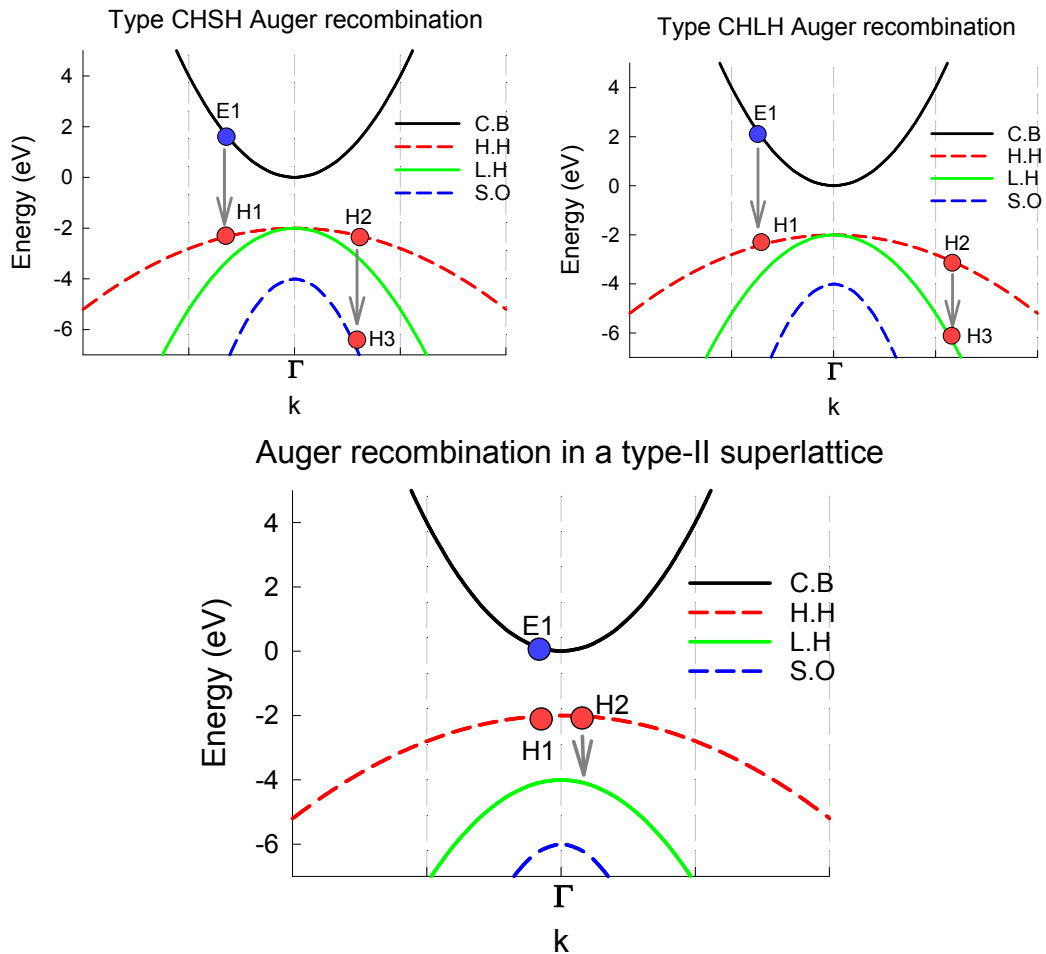


Figure 1.3: Top left - type CHSH Auger recombination where E1 and H1 recombine and H2 gains energy by moving to H3. Top right - type CHLH Auger recombination where E1 and H1 recombine and H2 gains energy by moving to H3. Bottom – Auger recombination in a Type-II superlattice is less likely to occur as H2 does not have many free states to transition into.

1.2 Photoconductors

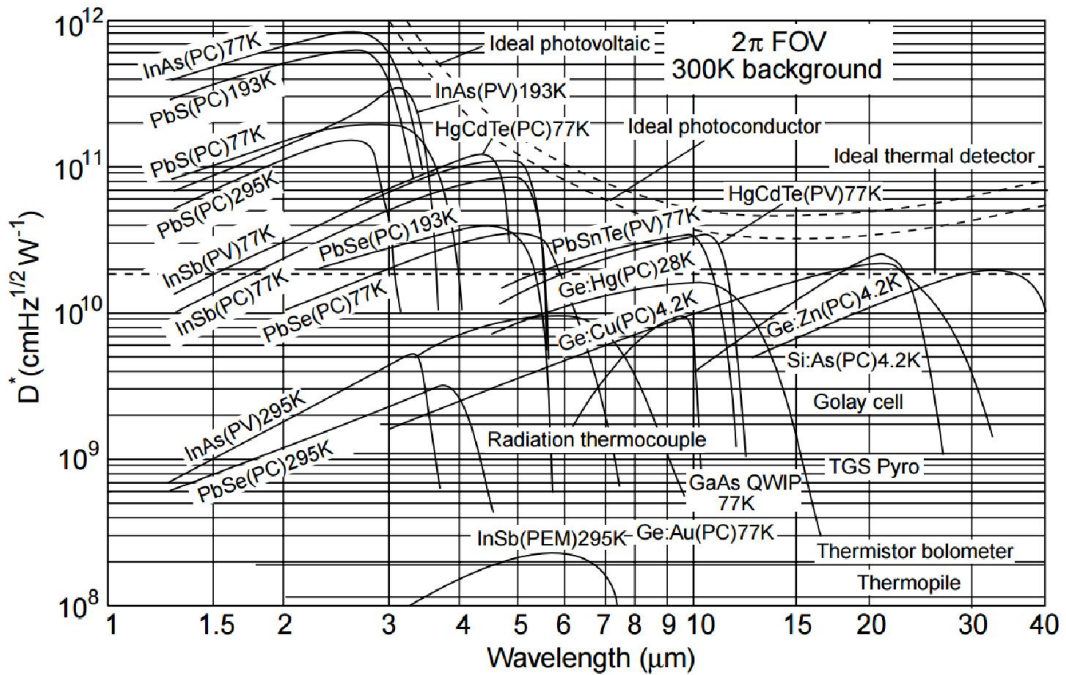


Figure 1.4: The detectivity of various commercial photoconductors (PC) and photodiodes (PV) at indicated temperatures. Measurement details can be found in [20].

Photoconductors are fabricated from homogenous semiconductor with non-rectifying contacts placed at either end of the active region, much like a semiconductor resistor. A voltage is applied to separate and extract the photo generated E-H pairs before they recombine, inducing a photocurrent. As discussed in section 3, detectivity is often used as a figure of merit when comparing the performance of detectors, and the detectivity of InSb, InAs and lead salt photoconductors are shown in Figure 1.4 [20]. Thermal generation of E-H pairs can be large in narrow bandgap semiconductors and cooling can be required to improve the signal to noise ratio. Alternatively the leakage current can be reduced by inducing a high density of deep-level impurities to reduce the intrinsic carrier concentration. However, traps can also capture photo-generated carriers and significantly reduce detector speed and responsivity. Photoconductors can also provide intrinsic gain which is useful for photon starved applications. Photoconductive gain is induced when the drift velocity of the carriers transiting the active region is significantly different. The slow moving carriers, that can also be trapped, creates a charge imbalance while it is in transit and consequently many of the fast moving carriers are injected into the active region in one transit of the slow carrier to maintain charge neutrality [21]. Photoconductor design has a significant trade-off between bandwidth, gain and dark current. Photoconductors are easy to manufacture due to their simple structure, however, advances in other detector technologies has limited use with

photodiodes generally providing higher performance and are more easily multiplexed onto a focal plane. Modern bolometers can provide similar performance with significantly lower manufacturing and operation costs replacing the applications where photoconductors were traditionally used. InSb and HgCdTe photoconductors provide a compelling option for some applications operating across the MWIR as moderate sensitivity can be achieved at Peltier cooled temperatures.

1.3 Photodiodes

A photodiode has a built-in potential generated by an electric field developed across a depleted space charge region that acts to separate photo-generated E-H pairs created within its vicinity. The separation and grouping of carrier types creates a net potential across the device as the E-H pairs seek to recombine providing electromotive force, as described by the photovoltaic effect. The internal electric field enables photodiodes to be operated at 0V, termed photoconductive mode, and consequently very low dark currents can be achieved compared to the ohmic leakage of a biased photoconductor. The response speed and responsivity of a photodiode can be increased by applying a small reverse bias voltage to extract the carriers at saturation velocity. The built in potential of a photodiode can be formed across any interface where significant charge transfer has occurred. Narrow bandgap photodiodes are often fabricated using a P-N junction to create a built-in potential, however, charge transfer can also occur across a heterojunction or Schottky barrier, although such methods typically result photodiodes with poorer performance [6]. Si photodiodes are used in most applications up to 1.1 μm , however, telecommunications applications require a direct bandgap semiconductor operating at longer wavelengths to which III-V semiconductors are mainly used. $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ based heterojunction photodiodes are widely employed across telecommunications wavelengths due to a high optical absorption coefficient and large saturation velocity. Traditional front illuminated P-i-N InGaAs photodiodes are limited to a bandwidth of ≈ 15 GHz while maintaining good responsivity, while optimised uni-travelling-carrier photodiodes have been reported with a bandwidth in excess of 300 GHz [22, 23]. InAs has a cut off wavelength of 3.5 μm and a higher optical absorption coefficient and saturation velocity compared to $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$. However, the narrow bandgap of InAs causes a significantly larger thermally generated noise compared to InGaAs photodiodes. Furthermore, the growth of InAs and InAs heterostructures based upon the 6.06 \AA lattice constant is less well explored compared to InGaAs, as discussed in greater detail in section 1.7. Consequently there are comparably few commercial vendors, or reports of InAs photodiodes. Commercial InAs photodiodes are mainly utilised in radiation thermometry and infrared spectroscopy applications [24]. InSb photodiodes are widely used

in radiation thermometry instruments as they provide response across the atmospheric transmission window of 3 – 5 μm [6]. HgCdTe photodiodes from the SWIR to LWIR are usually reported in a focal plane array format for imaging applications. HgCdTe photodiodes adopt a heterojunction to optimise performance, and SWIR photodiodes are often operated at room or 200 K, while MWIR compositions are operated at temperatures of ≈ 80 K [6].

1.4 Avalanche photodiodes

The input referred noise of front end amplifiers matched to the bandwidth of common photodiodes are of the order of $\approx 5\text{pAHz}^{-0.5}$ amassing a total input referred noise current of 300 nA over 4 GHz. Consequently although the detectivity of most photodiodes is very high, the sensitivity of the module employing a unity gain detector can be very poor due to the dominance of amplifier noise. When the amplifier noise is dominant, pre-amplification of the photocurrent can significantly improve the sensitivity of the detector module. An avalanche photodiode (APD) can be biased to generate a large electric field, under which charge carriers impact ionise and multiply. The sensitivity of a detector module employing an APD will continue to improve with increasing APD gain until the noise from the APD becomes dominant. Noise from an APD is generated through device leakage current, but also due to the stochastic nature of impact ionisation leading to 'excess' photocurrent noise after amplification. Optimisation of crystal quality, device design, and reduction of operating temperature can suppress the leakage current of an APD. The excess noise is reduced by decreasing the variance in gain experienced by each photo-generated carrier contributing to the average device gain. Impact ionisation and excess noise theory are discussed in detail in section 2.1, and it is shown that the excess noise of an APD is minimised when the hole and electron impact ionisation coefficients of a semiconductor are disparate, such that the ratio, k , deviates far from unity [25]. Impact ionisation rates are largely a material property and efforts to optimise APD performance have focused on characterizing new materials. Typical excess noise characteristics of InP [26], Si [27], $\text{Hg}_{0.5}\text{Cd}_{0.5}\text{Te}$ ($\lambda_c = 2.2 \mu\text{m}$) [28] and InAs [29] APDs are shown in Figure 1.5.

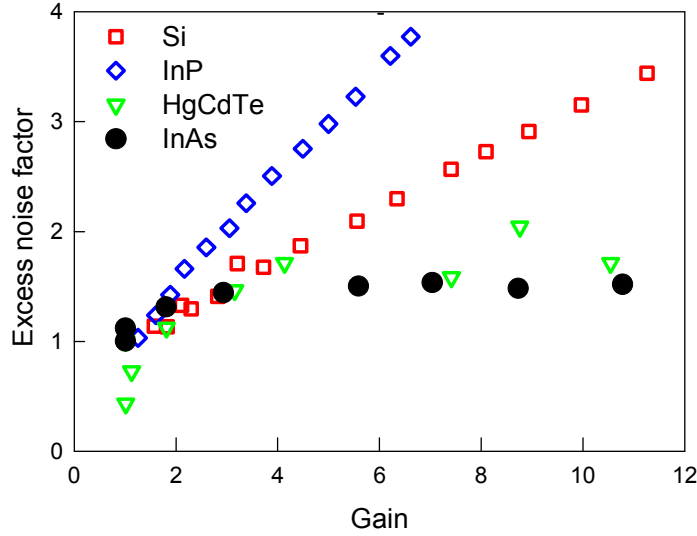


Figure 1.5: Excess noise characteristics of InP [26], Si [27], $\text{Hg}_{0.5}\text{Cd}_{0.5}\text{Te}$ ($\lambda_c = 2.2 \mu\text{m}$) [28] and InAs [29].

Si has a very low k value at low electric fields and thick Si APDs can achieve low excess noise [30]. However, such devices require high voltages to develop gain, and also operate with a low bandwidth due to long carrier transit times. III-V semiconductors can provide longer wavelength response with research largely driven by long haul telecommunications operating at $1.55 \mu\text{m}$ [31]. However, the impact ionisation coefficients of common III-V semiconductors tend to converge at large electric fields causing high excess noise as shown in Figure 1.6 for Si [30], GaAs [32], $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ [33], InAs [29]. InGaAs provides good absorption, but high tunnelling currents develop before significant avalanche gain can be achieved [34]. Telecommunications APDs therefore employ a heterojunction structure using separate materials for the absorption and multiplication regions termed a separate absorption and multiplication (SAM) APD [35]. For manufacturability, InP is widely used as the multiplication region, however, the excess noise is high due to unfavourable ionisation coefficients [36] limiting the useful gain to ≈ 20 (before the multiplication noise exceeds the amplifier noise). The excess noise performance of an APD can be improved by utilising a thin ($< 1 \mu\text{m}$) multiplication region [37] due to the dead space effect, which is discussed in section 2.3. As the lattice matched alloy $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ has larger band gap than InP, in recent years thin multiplication regions have been developed to reduce the excess noise of $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ APDs [38].

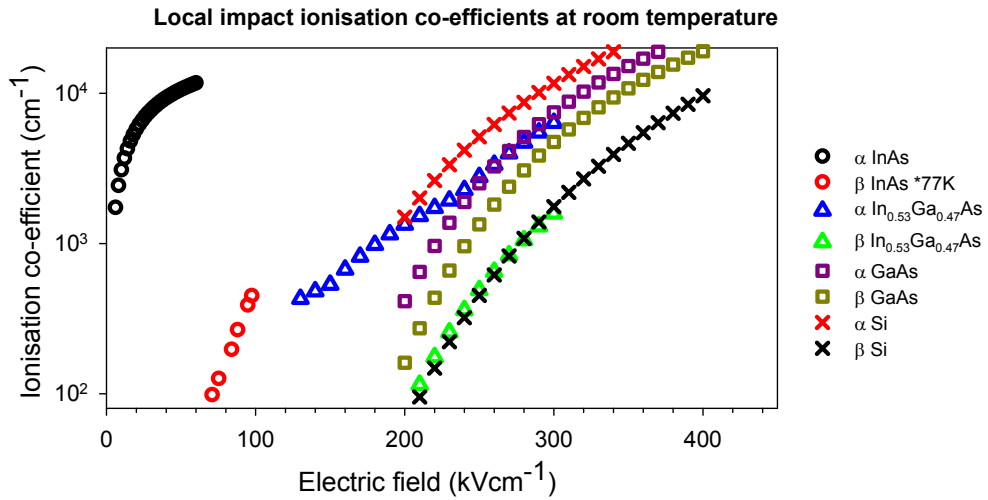


Figure 1.6: The local impact ionisation coefficients of for Si [30], GaAs [32], In_{0.53}Ga_{0.47}As [33], InAs [29].

The lack of suitable III-V semiconductors with naturally low k values has led research to engineer APD structures which enhance the multiplication of one carrier type, while suppressing that of the other. In 1980 it was hypothesised that electron impact ionisation could be locally enhanced at conduction band discontinuity as hot carriers transferred from a wide bandgap into a narrow bandgap semiconductor [39]. Improvements to avoid charge trapping at the heterojunctions were subsequently suggested utilising graded bandgap layers to create large discontinuities in the conduction-band, but a smooth valence band [40]. The resulting band structure resembled a staircase and research into staircase APDs was popular for many years. However, by the 1990s with no incontrovertible evidence presented, interest diminished. It was later established that it was not the premise of the staircase APD that was at fault, but the material system choice. Within the GaAs/AlGaAs heterojunctions used, charge carriers transfer out of the gamma valley before gaining sufficient energy to impact ionize, and the advantage of the conduction-band discontinuity is lost [41]. With advances in growth technology and impact ionisation theory, a recent publication has shown strong evidence for single carrier multiplication in a single-step staircase APD using AlInAsSb/InAsSb interfaces [42]. The deep gamma valley of InAsSb has a very low intervalley scattering rate and consequently hot electrons transferring into this material have a high probability of impact ionising. However, to whether higher orders of repeating step regions can be successfully grown remains to be seen and presents a significant challenge to extract useful gain from staircase APDs [43].

There are comparably very few reports of APDs operating at wavelengths beyond 1.65 μm . This is likely to be due to a combination of factors including, generation of large dark current and difficulties suppressing surface leakage and tunnelling currents in reverse biased

diodes. To achieve long wavelength response without using narrow bandgap semiconductors, a strain balanced type-II superlattice has been reported as the absorption region in a SAM APD lattice-matched to InP [44]. Such use for a type-II superlattice is a promising option for providing tuneable long wavelength response, however, there are significant growth and fabrication difficulties to overcome. Early work in 1967 tentatively reported the electron impact ionisation coefficient in InSb APDs is approximately 10 times larger than that of the hole impact ionisation rate as a promising material for low noise APDs [45]. However, the aforementioned difficulties have severely encumbered progress with the next significant report of InSb APDs only published in 2015 [46], although measurement of the low excess noise is yet to be confirmed. Early work on InAs APDs was not so promising with a poor k ratio being reported [47]. The validity of this early work was questioned by many researchers, however, the impact ionisation coefficient could not be verified. In 2008 electron dominated impact ionisation in InAs was reported [48], and quickly followed by measurements of the excess noise of InAs APDs [29] and the impact ionisation coefficients of InAs [49], as plotted in Figure 1.5 and Figure 1.6 respectively. These results provide incontrovertible evidence for true single carrier multiplication in InAs, and a highly promising semiconductor for low noise APDs discovered, to which this thesis is based upon. A review of InAs APDs is presented in section 1.7.

APDs with compositions of $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$ varying from $x = 0.7 - 0.2$ to achieve cut-off wavelengths of 1.3 to 11 μm have been measured to show a large variation in excess noise [50, 51]. The earliest work on $\text{Hg}_{0.38}\text{Cd}_{0.62}\text{Te}$ ($\lambda = 1.3 \mu\text{m}$) APDs reported low field resonant hole impact ionisation with a maximum k ratio of 30 achieved for an optimised composition [51, 52]. Electron dominated impact ionisation was later measured in $\text{Hg}_{0.78}\text{Cd}_{0.22}\text{Te}$ ($\lambda = 11 \mu\text{m}$), and unlike the resonant hole impact ionisation, was not limited to only low fields showing great potential for low noise, high gain APDs [50]. Improvement to growth, fabrication, and device design has recently yielded $\text{Hg}_{0.7}\text{Cd}_{0.3}\text{Te}$ APDs with a noiseless avalanche gain in excess of 1270 at 13.1 V at 80 K [28, 53]. The noiseless avalanche was due to electron only impact ionisation, but also ballistic electron transport [54]. Recently, through integration with low noise amplifiers $\text{Hg}_{0.7}\text{Cd}_{0.3}\text{Te}$ APD detector units have demonstrated remarkable sensitivity by achieving linear mode photon counting [55, 56]. However, exceptionally high material quality is required to support the high electric fields within HgCdTe APDs and compounds the already difficult manufacturing issues. Consequently production of HgCdTe APDs is limited and still after huge financial investment, commercially viable manufacturing is yet to be established.

1.5 Photomultiplier tube

The performance of the photomultiplier tube (PMT) is unrivalled with gain in excess of 1 million, negligible excess noise and low timing jitter. However, PMTs are based upon otherwise obsolete vacuum tube technology which are inherently fragile, bulky, require a supply voltage > 1000 V and are highly susceptible to magnetic fields. Furthermore, photocathode materials are limited to operating in the SWIR and have poor quantum efficiency of $\approx 2\%$ at wavelengths longer than $1 \mu\text{m}$. PMTs operate with absorption of a photon stimulating the emission of an electron by the photoelectric effect. The electron is accelerated in a vacuum and impinges on a cascade of dynodes causing further electrons to be emitted through secondary emission. The gain at each dynode is highly deterministic and consequently, many dynodes can be cascaded to achieve high gain incurring significant excess noise. PMTs are one of the few commercially available detector technologies providing single photon detection while operating in a linear mode.

1.6 Thermal detectors

Long wavelength photon detectors require significant cooling to suppress thermally generated dark current. Such cooling systems are costly, bulky and have high power consumption. Thermal detectors provide an attractive cheap alternative, however, the detector performance is significantly reduced. Thermal detectors thermalize the absorbed photon energy to heat a thin detector material changing its electronic properties. The properties of the detecting element measured are; resistance in bolometers, a voltage created by a thermoelectric effect in thermopiles, a voltage due to pyro-electricity in a pyrometer and the I-V characteristics in a diode type thermal detector. Bolometers are the most widely used thermal detector, providing excellent performance at room temperature. Furthermore, the uses of amorphous Si detecting elements has enabled micro-bolometer arrays to be fabricated using Si processes directly onto CMOS read out circuits. Such technology has enabled cheap fabrication of detector arrays operating at room temperature across the 7.5 to $14 \mu\text{m}$ spectrum, where room temperature objects have peak blackbody emissions.

1.7 InAs APDs

Narrow band gap semiconductors are acknowledged to be highly susceptible to surface leakage. In InSb photodiodes, surface leakage has largely been overcome through developments of the fabrication procedures, device design and use of passivation layers [57]. Surface leakage across the InAs surface however, was reported to be particularly severe due

to Fermi level pinning at the InAs surface producing a high sheet carrier concentration [58]. InAs APDs were pioneered by A. Marshall et. al, first focusing on growth and fabrication procedures [59]. Although significant previous work on the epitaxial growth of InAs had been carried out, A. Marshall reported the growth of InAs APDs using molecular beam epitaxy (MBE). From reflection high-energy electron diffraction (RHEED) observations, a thermal clean temperature of 500 °C was reported as being optimum. A trial and error approach was adopted to optimise the growth temperature with four growth temperatures of 470, 490, 500 and 520 °C utilised in the study. The defect density of the 470 °C growth temperature was far less than any of the other temperatures and produced a wafer with a shiny surface indicating a low defect density as shown in Figure 1.7 [59]. However, Maddox et. al reported high quality InAs utilising a growth temperature of 500 °C and a growth rate of 1 µm per hour [60]. Furthermore, dopant cells were cooled to idle temperatures (350 °C) during the growth of the intrinsic region to eliminate parasitic incorporation of dopant species achieving a very low unintentional background doping of $2 \times 10^{14} \text{ cm}^{-3}$. The significant difference in optimum growth temperature reported for InAs are likely to due to difficulties in determining the true wafer temperature in the MBE reactor.

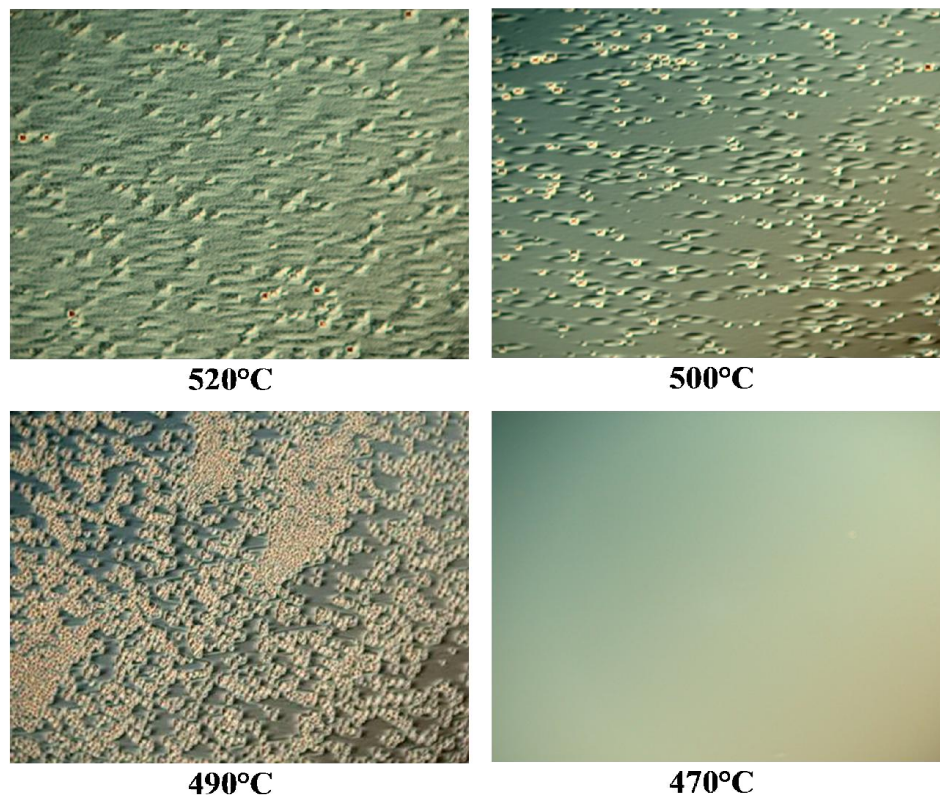


Figure 1.7: Photographs of the surface of InAs wafers grown at temperatures of 520, 500 490 and 470 °C [59]

Previous work has also been carried out on the epitaxial growth of InAs using Metalorganic vapour phase epitaxy (MOVPE), however, the material was reported with a very high background doping concentration of $2 \times 10^{17} \text{ cm}^{-3}$ due to unintentional carbon doping [61]. InAs APDs require increasingly thick structures, $\approx 10 \text{ }\mu\text{m}$, to achieve higher gain and so MOVPE growth techniques would be preferable over MBE.

Auger spectroscopy was used to investigate the surface conditions of InAs diodes prepared using a variety of wet chemical etching techniques. The study suggested that the high surface leakage in InAs could be due to the formation of an indium oxide after etching. A wet chemical etching recipe was developed to prevent the formation of indium oxide layer and was successful in significantly reducing the surface leakage current in reverse biased InAs diodes [59]. The low surface leakage measured in bulk InAs devices suggests the fermi level pinning effects may not cause significant surface leakage issues.

Development of etching and growth techniques enabled the gain and excess noise of InAs APDs to be measured accurately. The gain measured on InAs APDs is exponential and unlike any other established III-V APDs which generally show a sharp rise to breakdown [48]. This unusual behaviour is an artefact of electron only impact ionisation as holes are unable to sustain the avalanche breakdown by providing feedback and negate breakdown conditions from being reached. Excess noise and measurements confirmed true single carrier multiplication in InAs APD [29]. Due to the single carrier multiplication, InAs APDs have reported the largest gain-bandwidth product of any III-V APD [62]. Furthermore InAs APDs can achieve significant gain at a low bias voltages due to the high electron impact ionisation coefficient at low electric fields [63].

Characterisation of the impact ionisation coefficients of InAs was unusual when compared to other III-V semiconductors showing single carrier multiplication but also high impact ionisation coefficient at low electric fields, sharing similarities with long wavelength HgCdTe [29]. Impact ionisation theory of HgCdTe is well established, and observation of the HgCdTe band structure provides an accurate insight into the origins of the electron dominated impact ionisation [64]. The band structure of $\text{Hg}_{0.7}\text{Cd}_{0.3}\text{Te}$ is shown in Figure 1.8 [65]. The HH mass of HgCdTe remains fixed at $\approx 0.55 m_0$ across all IR compositions resulting in low hole-mobility with very high optical-phonon scattering. Holes therefore reside close to the HH band maxima over a wide electric field range due to inefficient energy gain. The effective mass of the gamma valley is approximately 30 times lighter, and the low optical phonon scattering yields a very high electron motility, approximately 100 times greater than hole mobility[66]. $\text{Hg}_{0.7}\text{Cd}_{0.3}\text{Te}$ has a very small band gap energy, E_g , of 0.29

eV, but unlike most III–V semiconductors, the ratio of the band gap energy to valley separation energy is very large with L and X valleys 1.5 and 2.5 eV higher respectively [67]. The intervalley phonon scattering rate from the gamma valley is low and the band structure of $\text{Hg}_{0.7}\text{Cd}_{0.3}\text{Te}$ can be simplified to electrons confined to the gamma valley and holes immobilised in the HH band. Under this simplified band structure, the minimum energy required for the carriers to impact ionise, defined as the threshold energy can be described as a function of the effective mass ratio [68]. Due to the strong asymmetry of effective masses in HgCdTe , the electron threshold energy is E_g while for holes it is $2E_g$. Hole impact ionisation is therefore very unlikely until very high electric fields are reached as carriers must attain a minimum energy of $2 E_g$ with inefficient energy gain from the electric field. Electron impact ionisation is very likely, even at low electric fields, as the threshold energy is low and carriers can gain energy quickly while remaining in the low scattering environment of the gamma valley [69]. It should also be noted that due to the very low scattering rates and low threshold energy, electrons are able to travel ballistically before impact ionising in HgCdTe yielding noiseless gain [53, 64]. HgCdTe band structure is therefore optimised for stimulating electron impact ionisation while suppressing that of holes.

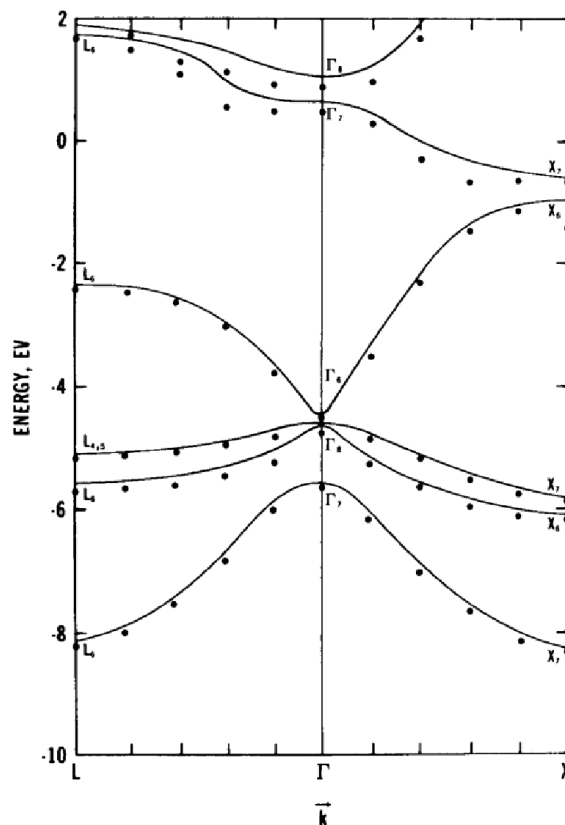


Figure 1.8: The band structure of $\text{Hg}_{0.7}\text{Cd}_{0.3}\text{Te}$ [65]

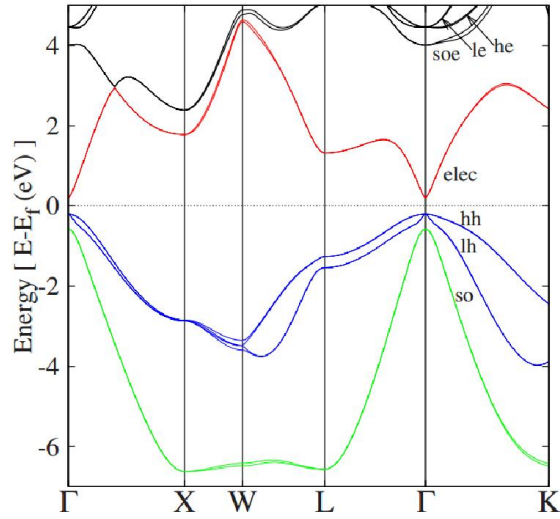


Figure 1.9: The band structure of InAs [70]

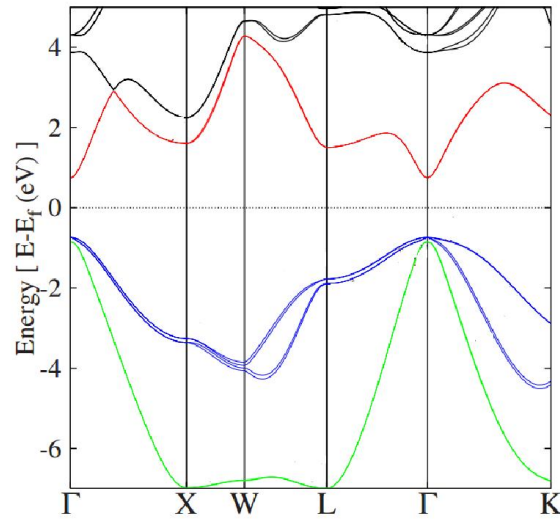


Figure 1.10: The band structure of InP [70]

Energy given with respect to the V.B	Hg _{0.7} Cd _{0.3} Te [67]	InAs [71]	InP [71]
E _g (eV)	0.29	0.35	1.35
E _L (eV)	1.79 (6.1E _g)	1.07 (3.05E _g)	1.94 (1.44E _g)
E _X (eV)	2.79 (9.62E _g)	1.37 (3.91E _g)	2.27 (1.68E _g)

Table 1.1: A comparison of some band structure properties of Hg_{0.7}Cd_{0.3}Te, InAs and InP

The band structure of InAs, shown in Figure 1.9, shares many similarities with HgCdTe, and not like other wide bandgap III-V semiconductors which are exemplified by the band structure of InP shown in Figure 1.10. Table 1.1 shows the X and L satellite valley energies compared to the bandgap energy for InAs, InP and HgCdTe. Electrons in both InAs and HgCdTe are able to gain the bandgap energy, $\approx E_{th}$, while remaining within the gamma valley. However, both satellite valleys within InP are less than $2E_g$ and consequently electrons in InP scatter around the lower mobility X and L valleys before able to gain E_{th} . While the impact ionisation process in InAs similar in principal to HgCdTe, the valley separation energies of InAs are relatively smaller and electrons begin to transfer out of the gamma valley in InAs at $\approx 2.5 \text{ kVcm}^{-1}$ as observed in drift velocity simulations [72]. The impact ionisation coefficient below such electric fields is negligible and therefore although the gamma valley is deep, carriers are not as well confined to the gamma valley as they are in HgCdTe. Monte Carlo simulations have shown that the while significant energy is gained from the gamma valley, a significant fraction of electrons transfer over to the L valley before impact ionising [73, 74]. The implications of this are that the electron impact ionisation rate of InAs is slightly lower compared to HgCdTe. Furthermore the energy gain of carriers with increasing electric field within the L valley is poor. The electron impact ionisation coefficient of InAs is only weakly dependant on the electric field.

As the electron impact ionisation coefficient is relatively independent of electric field, higher gain in InAs APDs is achieved with thicker avalanche regions. The thick avalanche region also is used to suppress the tunnelling current while achieving high gain. However, the background doping of the avalanche region must be kept low so to maintain an even electric field across the APD.

Another peculiarity of InAs APDs is that for any given bias, the gain is observed to decrease with decreasing temperature [29, 75]. Carrier scattering rates decrease significantly with reducing temperature and consequently, carriers achieve higher energies for the same electric field strength before being scattered. However, in all semiconductors but some compositions of HgCdTe, the bandgap and thus the threshold energy increase with decreasing temperature. Usually the increase in bandgap is outweighed by the reduced scattering rates, however, simulations have shown that in InAs the dependence on threshold energy is dominant [73]. It should also be noted that this effect has also been observed in InSb, [45] and at low electric fields in $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ [33].

Recent work has focused in optimising the performance of InAs APDs reducing the dark current and achieving higher gain by maintain wide avalanche regions with low background

doping. The dark current of mesa APDs has been shown to be dominated by a diffusion current between 300 and 175 K [76]. Low dark current has been achieved using a highly doped surface layer to increase the barrier to thermionic emission [77] and also a wide bandgap $\text{AlAs}_{0.16}\text{Sb}_{0.84}$ blocking layer with a large conduction band offset within the P-type region to block the diffusion of electrons generated at the surface [59]. At temperatures below 200 K, Shockley Reed Hall (SRH) generation and recombination currents dominate the dark current generated from within the intrinsic region [74]. Furthermore, the optimised wet etching procedure is generally been reported to produce significant leakage current in small area InAs APDs or at low temperatures [76]. In a comparative study the polymer SU-8 was identified as the most suitable passivation layer for mesa InAs APDs [78]. A recent publication has shown the surface leakage can be eliminated with the immediate use of SU8 passivation after wet chemical etching to lock-in the surface conditions [74].

1.8 Motivation and thesis organisation

Remote sensing is rapidly gaining popularity with increasing interest at SWIR and MWIR wavelengths, however, a commercially available detector providing gain at wavelengths greater than $1.7\ \mu\text{m}$ does not currently exist. Despite significant effort, HgCdTe APDs have not yet overcome the serious manufacturing issues, and the questions to whether these issues can be overcome are ever more pressing. Thermal detectors do not provide photon starved sensitivity while PMTs cannot operate at wavelengths longer than $1.7\ \mu\text{m}$. InAs is a widely accessible semiconductor with similar electronic properties to HgCdTe, but crucially, the potential for superior growth and fabrication which could promise high device yields on a comparatively cheap, and large area substrate. While InAs has a cut-off wavelength of InAs $3.5\ \mu\text{m}$, alloying with dilute amounts of Bismuth or Nitrogen has been shown to significantly reduce the bandgap energy while incurring minimal lattice strain for bandgap tuning; the first InAsBi photodiode was recently reported [79]. With InAs as a platform technology, a tuneable bandgap III-V semiconductor operating beyond telecommunications wavelengths could bring a tectonic shift in detector and sensing applications. However, current InAs APDs lack highly uniform and repeatable growth and fabrication procedure that is required to exploit InAs APDs for practical applications. All current InAs APDs utilise a mesa design, and although great progress has been made developing wet chemical etching procedures to reduce the surface leakage [59], complete removal of surface leakage current in small area mesa APDs remains a challenge and the surface chemistry of InAs remains poorly understood. Furthermore, while the excess noise of InAs APDs can compete with HgCdTe, the gain from the current mesa APDs is lower.

This thesis is primarily concerned with fabrication and characterisation of planar InAs APDs to achieve high gain. The motivation and summary of individual chapters are given below.

Chapter 2:

Background information on the core topics discussed in this thesis are presented including literature reviews on impact ionisation, avalanche gain, excess noise, ion implantation, annealing, premature breakdown in planar APDs and methods of mitigating the formation of electric field hotspots.

Chapter 3:

Figures of merit for detectors are discussed in addition to experimental techniques used to characterise InAs APDs in this thesis. The experimental techniques discussed are current-voltage (I-V), capacitance-voltage (C-V), responsivity and gain.

Chapter 4:

Photodiodes and APDs based on mature semiconductors such as Si, InGaAs/InP [80], InSb [81] and HgCdTe [82] utilise a planar topology to benefit from a simplified and economic fabrication process with high manufacturing yields, device uniformity and reliability, and excellent control over surface conditions. Furthermore adopting a planar topology gives additional degrees of freedom to design advanced heterostructures using wide bandgap lattice matched alloys. In order to fabricate planar InAs APDs, selective area doping techniques must be utilised, however, there are few reports of Zn diffusion or ion implantation into InAs. Zn diffusion has been utilised to fabricate planar InAs photodiodes with good results [83], however, Zn diffusion is unfavourable when fabricating low noise InAs APDs as the poor dopant control results in unavoidable doping near the saturation limit ($\approx 3 \times 10^{19} \text{ cm}^{-3}$) with a very short minority carrier diffusion length in Zn diffused material. To maintain low excess noise within InAs APDs, photons should be absorbed within the P-type layer, however, the thickness of the Zn diffused P-type required for high photon absorption is significantly longer than the minority carrier diffusion length. Consequently high responsivity could not be achieved with low excess noise. Ion implantation is a far more versatile selective area doping technique with excellent control over the doping profile and density. However, there are very few reports of ion implantation for P-type doping in InAs. A literature review of ion implantation for P-type doping is presented with Be implantation found to be the most suitable. Through the characterisation of diodes fabricated using Be implantation, the activation of Be in unannealed material was found to be poor. Annealing was investigated, and an optimised implantation and annealing procedure developed for selective area P-type doping InAs. The use of hot implants to reduce the

implant damage was also investigated. A procedure for fabricating planar InAs photodiodes was developed and the bulk and surface leakage currents of planar InAs photodiodes analysed. Diffusion of the Be implantation profile caused by annealing and hot implants were investigated using secondary ion mass spectroscopy (SIMS). The dominant leakage mechanisms in InAs photodiodes are discussed and optimised Be implantation profiles are investigated to maximise the detectivity of planar photodiodes. The detectivity is compared to other reports of planar and mesa InAs photodiodes fabricated using various methods. The majority of this work has been published in IEEE Transactions on Electron Devices [84].

Chapter 5:

Planar APDs were fabricated from 2 wafers, one of which had a very wide intrinsic region with low background doping to achieve very high gain. The activation energies of the bulk and surface leakage mechanisms were determined through analysing the temperature dependence of the dark current of planar APDs. The depletion width and background doping of high gain APDs were characterised and found to equal the largest reported for a mesa InAs APD. Due to the large depletion region, the gain at 200 K was the largest achieved for any InAs APD. The breakdown conditions of InAs APDs were investigated and it was found that the positive temperature dependence of the electron impact ionisation coefficient causes a thermal runaway in hotspots in planar InAs APDs biased near breakdown. Guard rings are designed to prevent the formation of electric field hotspots. The effectiveness of various guard ring structures was investigated from room temperature to 77 K and the results discussed. Recommended improvements to planar InAs APDs are discussed. The majority of this work has been published in IEEE Journal of Lightwave Technology [85].

Chapter 6:

It is becoming increasingly difficult and impractical to grow the thick structures with very low background doping to achieve gain in InAs APDs. To reduce the stringent growth requirements, a structure in which the avalanche gain develops laterally, perpendicular to the direction of growth, is discussed. The advantage of the lateral APDs is that it can be fabricated from only a thin layer of InAs. Various lateral APDs were simulated with an optimised device identified. N-type selective area doping using Si ion implantation and annealing were developed, and along with Be implantation, utilised to fabricate a range of lateral APDs. Responsivity measurements along with electric field simulations were performed to establish the carrier extraction mechanisms of the lateral APD structures. In a comparative gain study, enhanced lateral gain was measured in an optimised lateral APD structure. A conclusion to the work on lateral APDs presented in this thesis is presented before the recommended future direction for developing lateral APDs is discussed.

Chapter 7:

A conclusion to the work contained in this thesis is presented.

Chapter 8:

Based on the conclusions and drawing from my experiences, areas to prioritise future work are suggested.

Chapter 9:

The appendices to this works are contained.

1.9 References

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2 Background information

2.1 Impact ionisation

Impact ionisation is an electron or hole scattering mechanism in which a new E-H pair is generated. In principal, impact ionisation is the opposite of Auger recombination; a schematic diagram of an electron impact ionisation event in a direct bandgap semiconductor is shown in Figure 2.1. In the case of electron impact ionisation, the initiating electron, E1, is very hot after gaining energy from an electric field and occupies a high energy state in the conduction band. Impact ionisation has a non-zero probability only when the initiating electron's energy is greater than the bandgap and final states are available to the original and newly created electron-hole pair to conserve energy and momentum. The impact ionisation threshold energy, E_{th} , is defined as the minimum energy at which both of these conditions can be satisfied and a carrier with the threshold energy is said to be enabled. The impact ionisation event involves a coulombic interaction between the initiating carrier, E1, and a valence band electron, E3, with enough energy transferred to the valence electron to excite it into the conduction band, E4, creating an E-H pair. The electron transitions $E1 \rightarrow E2$ and $E3 \rightarrow E4$ are symmetrical such that the net energy and momentum of the scattering event = 0.

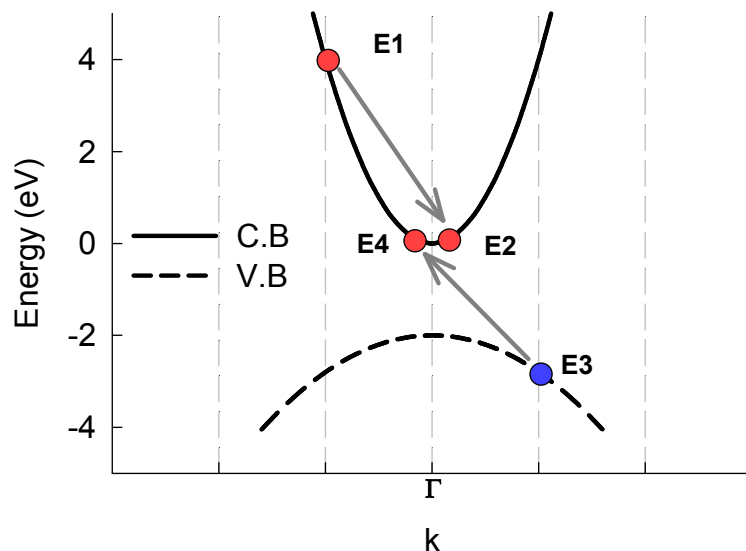


Figure 2.1: An *E-k* diagram of an electron-initiated impact ionisation event.

In the simple parabolic bands approximation, E_{th} of electrons in a semiconductor with direct parabolic bands is given by equation (2.1) [1] where m_e is the electron effective mass and m_h is the hole effective mass.

$$E_{th} = E_g \left(1 + \frac{m_e}{m_e + m_h} \right) \quad (2.1)$$

Until recently, MWIR HgCdTe is the only semiconductor to be accurately represented by such parabolic approximations [2]. All other semiconductors have significantly more complex band structures with anisotropies and relatively small energy gap separating the gamma and higher satellite valleys, leading to transfer of electrons to the higher valleys before they can acquire E_{th} . In this case, Monte Carlo simulations with the scattering rates in each valley are required to produce accurate impact ionisation modelling. The scattering rates of InAs are shown in Figure 2.2 [3] to illustrate the sophistication and complex nature of the Monte Carlo approach. The electron threshold energy in InAs at 77 K can be seen to be 0.97 eV, however, the impact ionisation rate is lower than intervalley scattering rates.

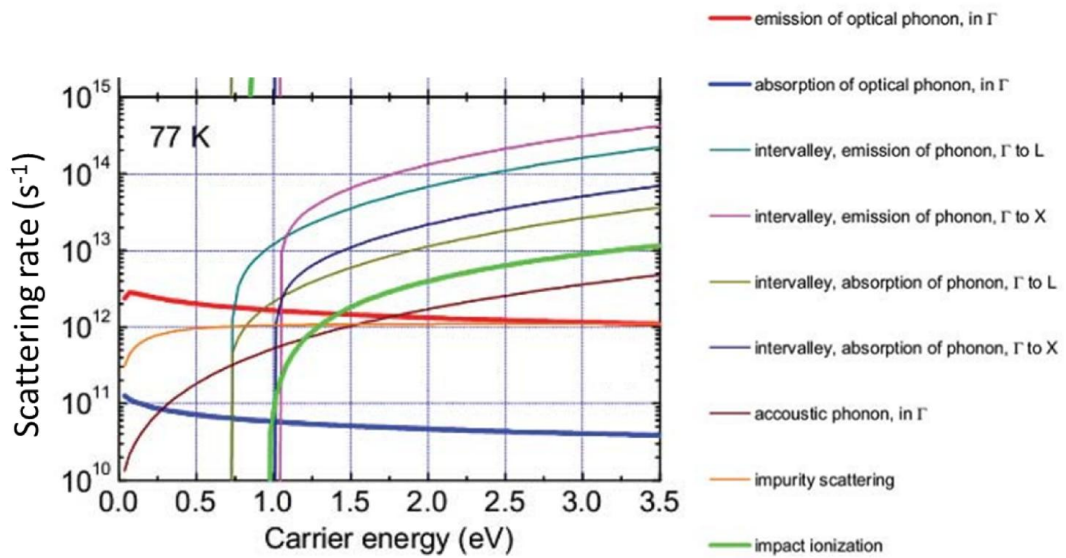


Figure 2.2: Electron scattering rates in InAs at 77 K [3]

With knowledge of the scattering rates, band structure and electronic properties of a semiconductor, Monte Carlo models can be used to simulate the gain of an APD. However, the use such a complex model to simulate gain and excess noise characteristics is impractical and required heavy computation. Furthermore many of the Monte Carlo parameters are unknown and are chosen based on interpolations or used as fitting parameters against experimental data.

Carrier energy, position, or time within an electric field cannot be used to accurately predict when a carrier will impact ionise. However, the stochastic nature of impact ionisation can be analysed statically to provide a highly simplified, but accurate description. Impact ionisation coefficients for electrons and holes represent the average number of times a carrier is likely to impact ionise over a unit distance for a given electric field. The reciprocal of the coefficient is equal to the average distance a carrier travels between impact ionising. The impact ionisation coefficients can be determined through deconvolution of measurements of avalanche gain from an APD with a wide multiplication region to ensure the carrier distribution is in equilibrium with the local electric field [4]. Mathematical equations for gain and excess noise as a function of the impact ionisation coefficients are therefore independent of device structure, and extremely useful tools for modelling and design. The impact ionisation coefficients for Si, GaAs, In_{0.48}GaAs and InAs are shown in Figure 1.6. At low electric fields, few carriers reach the required energy to impact ionise before being scattered and therefore impact ionisation events are rare with the ionisation coefficient being low. Carriers gain energy more rapidly in larger electric fields and are more likely to impact ionise before being scattered by an alternative mechanism.

2.2 Avalanche gain

R. J. McIntyre published the first complete derivations of mathematical expressions for the gain and excess noise of an APD in 1966 [5]. These expressions are referred to collectively as the Local Model due to the assumption that the carrier distribution at any point within the multiplication region is in equilibrium with the local electric field. The average gain, M , from injecting a carrier at position x within a multiplication region of an APD with width, w , can be expressed as a function of the impact ionisation coefficients as shown in equation (2.2). The solution contains a double integral as the offspring (hole), of an initial impact ionisation event initiated by an electron, travels in opposite direction within a high electric field region and may also initiate impact ionisation. Therefore an initiating carrier may generate a cascade of impact ionisation events creating avalanche gain as depicted in Figure 2.3.

$$M(x) = \frac{\exp\left[-\int_x^w \alpha(x-\beta)dx'\right]}{1 - \int_0^w \alpha \exp\left[-\int_{x'}^w (\alpha-\beta)dx''\right] dx'} \quad (2.2)$$

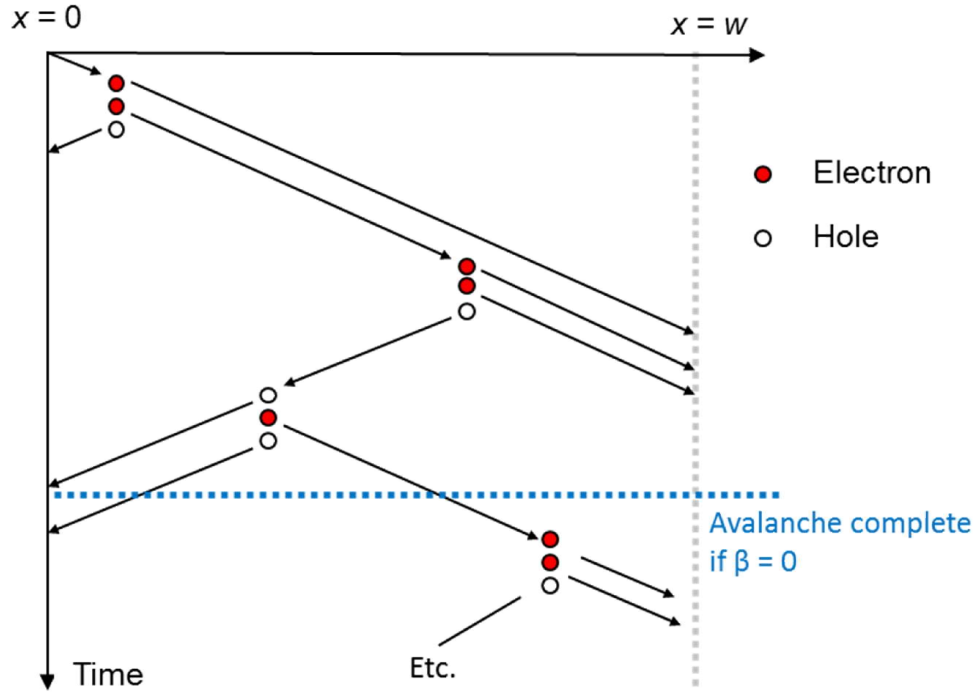


Figure 2.3: Schematic diagram of avalanche gain initiated by an electron. The avalanche duration is also indicated if holes cannot impact ionise.

For a semiconductor showing single carrier multiplication, where $\beta = 0$, the cascade is unidirectional and the electron carrier density exponentially increases across the multiplication region. Therefore the largest gain is achieved from pure electron injection in the P-type region as the carrier travels the full length of the multiplication region. Furthermore, the unidirectional avalanche gain has implications on the transit time limited bandwidth as all the carriers from the cascade will exit the multiplication region within one electron and hole transit time. In the case when either carrier can impact ionise anywhere within the multiplication region, higher gain is achieved concomitantly with increased avalanche duration resulting in fixed gain-bandwidth product. Therefore a semiconductor showing single carrier multiplication is highly desirable as APDs have short avalanche duration and an infinite gain-bandwidth product [6].

For the case of electron only impact ionisation and pure electron injection, the gain of an APD is given by equation (2.3) [5]. Without a feedback mechanism provided by hole impact ionisation, the avalanche cascade cannot become self-sustaining and therefore avalanche breakdown cannot occur. Hole impact ionisation is negligible until electric fields of 70 kVcm^{-1} in InAs while electron impact ionisation is significant at 10 kVcm^{-1} [7]. The electric field range over which InAs shows single carrier multiplication is large, however, the

electron impact ionisation coefficient does not significantly increase over this range as shown in Figure 1.6. Therefore high gain in InAs APDs is achieved with wide depletion region widths. Furthermore, assuming the APD is fully depleted, InAs APDs shown pure exponential gain characteristics as α and w are effectively constants.

$$M = \exp(\alpha w) \quad (2.3)$$

Most semiconductors are better characterised by $\alpha \approx \beta$, especially at large electric fields, and show gain characteristics with a sharp rise to breakdown. Breakdown conditions are reached when the second term of the denominator in equation (2.2) = 1 as the divide by 0 causes the gain to approach infinity. If $\alpha = \beta$ is an accurate approximation, the gain of the APD can be calculated by equation (2.4) [5].

$$M = \frac{1}{1 - \alpha w} \quad (2.4)$$

2.3 Excess noise

The noise spectral density, I_n , of a current, I , due to shot noise is given by equation (2.5).

$$I_n = \sqrt{2qI} \quad (2.5)$$

A perfect amplifier simply increases the magnitude of the noise spectral density by the signal gain. However, due to the stochastic nature of impact ionisation, excess noise factor, F , is also added with the noise spectral density of the photocurrent of an APD, I_{nAPD} , is given by equation (2.6).

$$I_{nAPD} = M\sqrt{2qIF} \quad (2.6)$$

Consider the impact ionisation frequency of a single carrier transiting a multiplication region assuming the hole offspring do not impact ionise. Under the assumption of the local model, i.e the carrier distribution at any point within the multiplication region is in equilibrium with the local electric field, the probability mass function (PMF) of the impact ionisation frequency, N_{ii} , across a multiplication of fixed width can be described by a Poisson distribution. The PMF of distributions with averages, μ , of 2, 6 and 10 were calculated using equation (2.7) and plotted in Figure 2.4. Excess noise is caused by fluctuations in the APD gain and therefore is represented by the distribution's variance. A Poisson distribution's mean is equal to the variance and therefore high gain, as achieved by larger μ , is concomitant with increased excess noise. While Figure 2.4 shows the PMF of a single

carrier, the excess noise factor captures fluctuations in the avalanche gain, including the offspring of the initiating carrier, as shown in equation (2.8).

$$P(N_{ii}) = \frac{\mu^{N_{ii}} e^{-\mu}}{N_{ii}!} \quad (2.7)$$

$$F(M) = \frac{\langle M^2 \rangle}{\langle M \rangle^2} \quad (2.8)$$

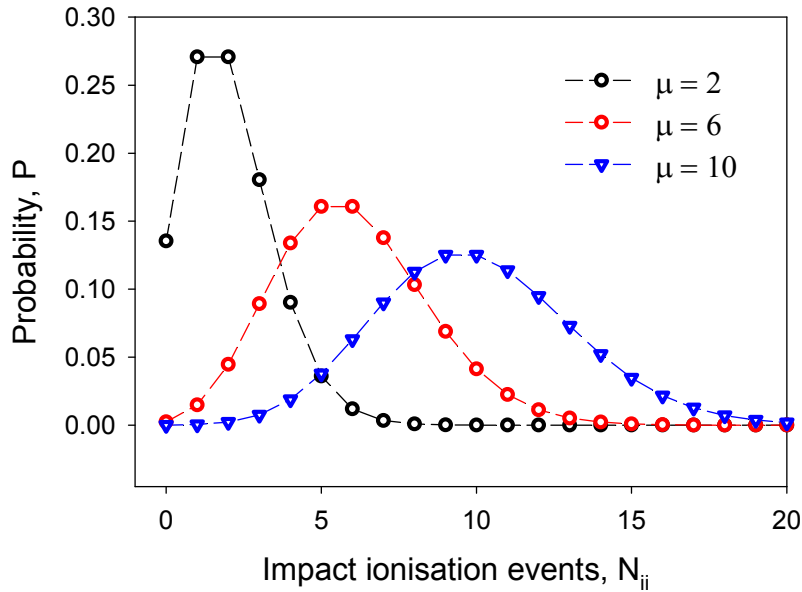


Figure 2.4: The probability mass function of impact ionisation frequency of a carrier transiting across a multiplication region for averages of 2,6 and 10.

An expression for the excess noise under pure electron injection as derived by McIntyre [5] is given in equation (2.9).

$$F(M) = kM + \left(2 - \frac{1}{M}\right)(1 - k) \quad (2.9)$$

Where $k = \beta/\alpha$

Excess noise characteristics are plotted in Figure 2.5 assuming that the ratio of the impact ionisation coefficients remains constant with increasing electric field. The excess noise is minimised when only a single carrier is able to impact ionise ($k = 0$). This is intuitive as the lack of a carrier feedback mechanism ensures that secondary impact ionisation cascades, initiated by holes, cannot be set in motion. Therefore the variance of the cascade length is significantly reduced.

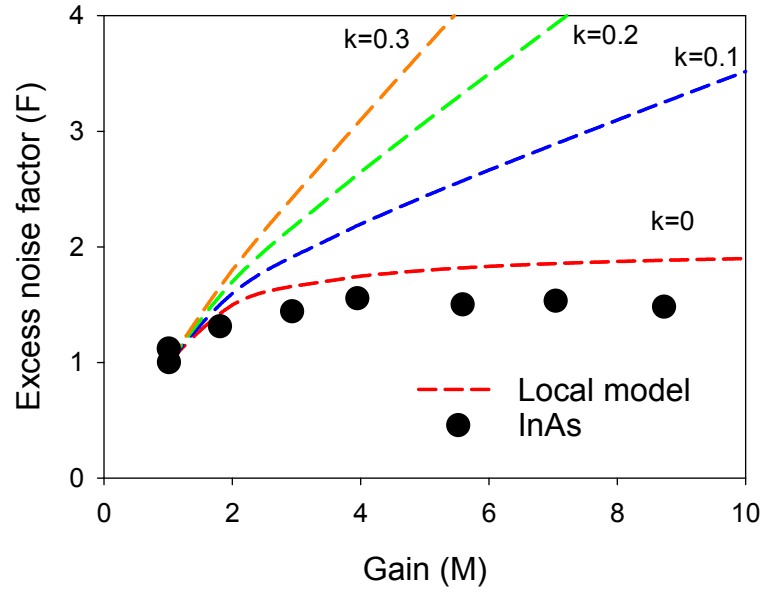


Figure 2.5: The excess noise characteristics for various k values. The measured excess noise characteristics of InAs are also shown.

While the local model provides a simple set of APD design tools and guidelines, the local approximation of carrier distribution has been shown to be invalid with significant overestimations of the gain and excess noise. The local approximation implies that the impact ionisation length probability density function (PDF) at any position within the APD can be described by an exponentially decaying distribution as plotted in Figure 2.6. However, when a carrier is injected into the multiplication region cold, or is scattered to the bottom of the conduction band after impact ionising, the threshold energy must be regained before impact ionisation. The minimum distance a carrier is required to travel to gain the threshold energy is termed the dead space, d_e , and can be calculated using equation (2.10) assuming no inelastic scattering where, ξ , is the electric field and, q , is the charge of an electron.

$$d_e = \frac{E_{th}}{q\xi} \quad (2.10)$$

A more accurate impact ionisation length PDF is shown in Figure 2.6. As the enabled impact ionisation coefficient, α^* , after the dead space is significantly shorter, and therefore more deterministic, the excess noise is reduced [8]. Dead space considerations are only usually relevant when the mean distance between impact ionisation events is comparable to the dead

space length. As discussed in section 1.4, the dead space effect can be exploited to reduce the excess noise in APDs by using thin multiplication regions. This principal has been particularly prominent in the design of telecommunications APDs where a semiconductor with favourable impact ionisation coefficients is not available [9]. The dead space effect is also observed in relatively thick InAs APDs as shown in Figure 2.5 [7] with measurements of the excess noise significantly lower than that predicted by the local model. In a more extreme case, the ionisation length PDF of $\text{Hg}_{0.7}\text{Cd}_{0.3}\text{Te}$ APDs can be described by a delta function with noiseless avalanche gain, or $F = 1$ [10]. The Random Path Length (RPL) [11] and Recurrence models [12] can account for the effects of dead space when simulating the gain and excess noise characteristics of APDs.

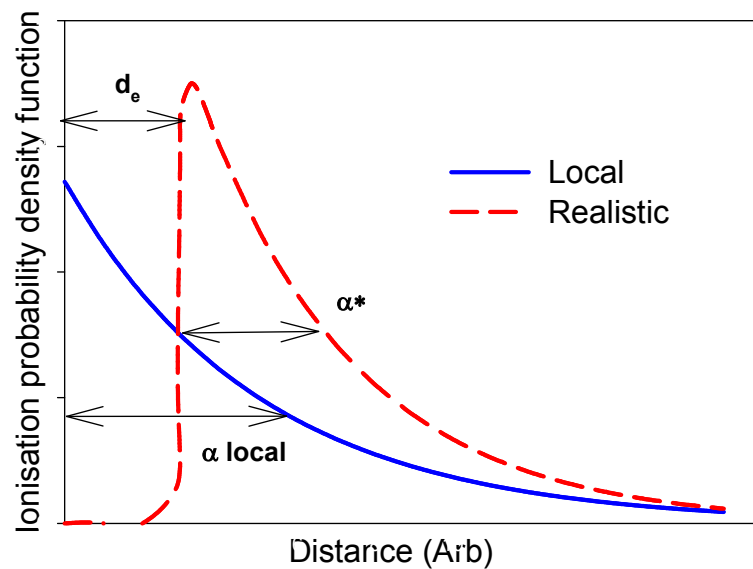


Figure 2.6: A probability density function of the ionisation path length of carriers assumed by the local model compared to a realistic model of a cold carrier.

2.4 Ion implantation introduction

Ion implantation is the process of electrostatically accelerating ionised atoms and impacting them into a target material. Perhaps the most appealing features of ion implantation when applied to semiconductor device fabrication are that precise amounts of almost any atom can be accurately implanted into the target within a very small thermal budget. Ion implantation is a versatile tool finding itself in wide variety of semiconductor device fabrication processes. Its main uses today are for implanting dopants, creating silicon on insulator substrates through the separation by implantation of oxygen (SIMOX) process, inflicting crystal damage for isolation and correcting the threshold voltage of transistors [13]. However the scope of this review is limited to doping through ion implantation.

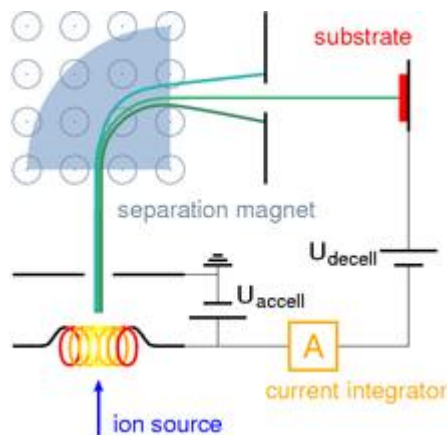


Figure 2.7: A schematic diagram of a simple ion implantation tool [16]

Ion implantation tools evolved from particle accelerators in the early 1950's, during an era where damage induced doping using ion bombardment was highly active. In 1954 William Shockley filed a revolutionary patent describing ion implantation as a method of introducing controlled amounts of impurities into a semiconductor to achieve substitutional doping instead of defect related doping [14]. This seemingly simple idea proved to be a major development as it enabled thermally stable and high quality doped regions to be fabricated. Shockley's revolutionary patent took 10 years before it was fully embraced by the Si industry with a timeline coinciding with; dramatic improvements to ion implantation tools; the development and understanding of annealing techniques to recover implanted crystal; the development of the planar process and also the invention of the self-aligned gate technique. A fascinating history of the developments of ion implantation is given by R. B. Fair [15]. A schematic diagram of the basic components of an implantation tool are shown in Figure 2.7 [16] consisting of an ion source, accelerator, mass selector and target. Ionised gas is extracted from the source by an electric field developed between two charged electrodes. Once accelerated, the ion beam is deflected in a magnetic field with the radius of curvature

proportional to the square root of the ions mass. The ion beam is purified by blocking the trajectory of impurities while ions of the correct mass exit through an aperture. The pure ion beam is further accelerated before being uniformly scanned over the target using steering electrodes. The target dose is measured by locating the target in a Faraday cup and integrating the beam current.

2.5 Implanted ion distributions

The distribution of implanted ions within a solid can usually be described by a Gaussian distribution with a skewness and kurtosis. The depth of an implant is often described by the projected range, R_p , which is defined as the distance from the surface to the peak concentration of the ion distribution. When modelling the implantation, straggle is used to describe the standard deviation of the Gaussian distribution. Selective area doping is achieved by using an implant mask which can be patterned to leave areas of the semiconductor exposed. The thickness of the masking material must be greater than the penetration depth of the ion in the masking material. The distribution of dopants varies from the uniform value when approaching the mask edge. The drop in concentration is achieved before the mask edge is reached and reduces to a value of a half directly underneath the mask. The roll off at a mask edge can be characterised by a Gaussian distribution with a lateral projected range and a lateral straggle. The orientation of a crystalline target with respect to the ion beam can also affect the ion distribution. The periodic voids found within a crystal lattice can channel the implanted ion, steering it along a particular plane by low impact collisions along a shallow angle, much like the propagation of light in a waveguide. However, alignment tolerances are small for achieving reproducible channelled implant profiles and so channelled implants are not common. Furthermore, unpredictable de-channelling can occur due to damage build up. Excellent implant reproducibility can be achieved in crystalline material by angling the crystal so that no major channels are easily penetrable from beam trajectory. Implants into (100) zinc blend crystals are carried out at an angle of 7° off axis to minimise channelling as this tilt angle lies halfway between the [100] and the [133] axis located at 14° . Channelling can also be reduced by carrying out the implant through a thin film of amorphous crystal. The amorphous crystal is used as a screen to scatter the trajectory of the ions before penetrating into the semiconductor. An ion implantation profile can be simulated using the software Transport of Ions in Matter (TRIM) [17] which is a Monte Carlo based program for calculating the stopping and range of ions into an amorphous target. Extensive work has been carried to verify the accuracy of TRIM across a wide range of energies from 10 eV - 2 GeV in numerous gaseous and solid targets. A full description of the calculations used in TRIM can be found in [18].

2.6 Ion implantation damage

Table 2.1 Energy dissipated in InAs from 200 keV ions (%) and the average number of vacancies produced per ion.

	Be	Mg	Zn
Ionisations	85.34	42.9	14.94
Phonons	0.15	0.05	0.08
Nuclear loss	14.51	57.05	84.98
Vacancies per ion	1293	4840	6926

The penetration depth of an ion into a target material depends on the material density, ion species, the energy through which the ion was accelerated and, in the case of a crystal, the orientation. Upon penetration into the target the ion loses kinetic energy to both electrons and target atom nuclei. Energy lost to the target electron cloud is termed electronic loss and target electrons are excited before recombining through either photon or phonon losses. Electronic loss is not damaging to the target, however, incident ions may become interstitial atoms where they rest. Ionisation loss is the main energy loss mechanism for high energy particles in a semiconductor which has comparatively heavy lattice atoms. Energy lost through collision with the target atom nuclei is termed nuclear loss. Nuclear collisions scatter the velocity of the ion and can damage the target lattice if sufficient kinetic energy is transferred to the target atom in the collision to displace it from its original lattice site. The displacement energy of a lattice atom is defined as the minimum energy required to break the electronic bond and eject it from the lattice site creating a Frenkel pair. The energy spent breaking the atom free of its electronic bond is lost as phonons and is called the lattice binding energy. After a collision the displaced atom will therefore travel with a kinetic energy equal to the collision energy minus the lattice binding energy. The displaced atom and the original ion will continue to transfer energy in this manner before coming to rest. Displaced atoms set into motion from a nuclear collision are termed recoils and a succession of displacements created by a recoiling atom is called a recoil cascade. Recoil cascades account for a significant percentage of the damage sustained during implantation as atoms of the same mass are efficient in transferring kinetic energy. Nuclear loss is dominant for ions travelling with low energy and with similar mass to the lattice atom. This is demonstrated in Table 2.1 as the energy loss percentage of Be, Mg, and Zn ions implanted into InAs 200 keV has been calculated using TRIM. Be ions with an atomic mass of 9.01 lose 85 % of their

energy through electronic loss which is not damaging to the lattice whereas Zn ions with an atomic mass of 65.38 lose 85 % of their energy through nuclear loss. While also producing substantially more implant damage, the Zn ions will also have a significantly shorter projected range than a Be ion implant at the same energy. An example of a simulated doping profile achieved using Be implantation into InAs at 200 keV at an angle of 7° is shown in Figure 2.8.

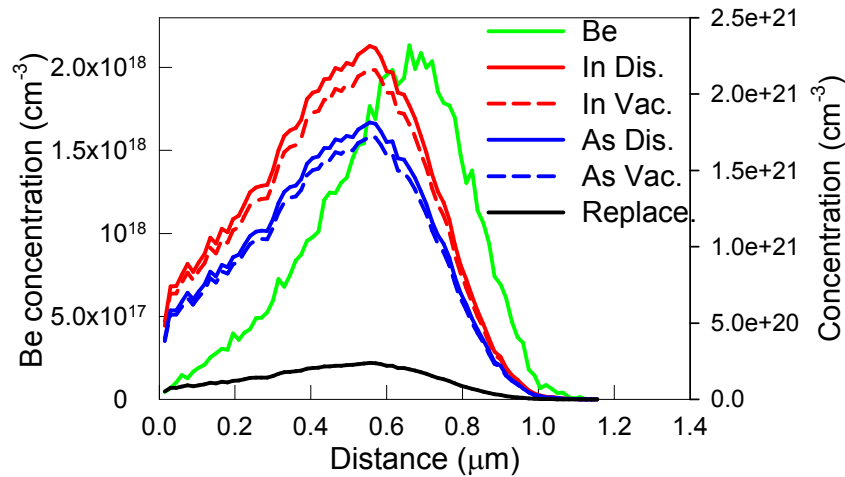


Figure 2.8: Be concentration from an implantation of $1 \times 10^{14} \text{ cm}^{-2}$ Be ions at 200 keV into InAs at 7° off axis. Also shown are the In and As displacement and vacancy concentrations caused by the implantation damage. The replacement collisions are also shown.

The implant damage profile follows a Gaussian distribution with a peak damage concentration just short of the projected range of the ion profile as shown in Figure 2.8 for Be implantation into InAs. The implant damage characteristics can be explained by electronic loss is high for energetic ions entering the target and after the ion has slowed near its projected range, nuclear stopping becomes dominant. Light implant damage is characterised by interstitials and vacancies at the peak of the projected range. With increasing dose, the damage areas begin to overlap and a buried amorphous layer will form just below the projected range. The amorphous region will grow towards the surface with increasing dose until the surface is completely amorphous. The damage profile for Be implantation into InAs is shown in Figure 2.8 and was calculated using displacement energy values of 6.7 eV for In and 8.5 eV for As with the lattice binding energy set as 12 eV [19]. Due to the lower lattice binding energy of In, more of the group III elements are displaced in InAs. A recoil that gives up its remaining energy displacing an identical lattice atom is termed a replacement collision and does not result in any damage. Figure 2.8 shows the net In and As vacancies are lower than the number of displacement events due to replacement collisions. The average number of vacancies caused by a Be, Mg and Zn atom have been

calculated for a 200 keV implant and is shown in Table 2.1. As expected, the implant damage from Be is significantly lower than the other heavier elements. It must be noted however, TRIM calculations do not account for dynamic annealing and consequently TRIM damage calculations are only valid for comparative studies. At room temperature greater than 99 % of the damage can anneal out due to the thermal energy [18].

2.7 Annealing

Implantation does not stand as an effective doping process on its own, annealing is required to repair lattice damage and encourage implanted atoms to take up substitutional lattice sites activating them as dopants [20]. Annealing accelerates the diffusion of defects encouraging them to annihilate as the crystal seeks a lower thermodynamically stable state [21]. However an appropriate annealing cycle is required to remove a particular type of implant damage as under certain conditions, defects can coalesce forming extended defects. Furthermore, the annealing cycle is constrained by a thermal budget which is defined as the maximum tolerable dopant diffusion to maintain acceptable device performance. Therefore an optimised annealing cycle removes the maximum amount of crystal damage while minimising dopant diffusion.

In a widely renowned paper by K. S. Jones et. al [22] the extended defects which arise in Si upon annealing can be classified into 5 categories. Damage categories 2 – 5 are concerned with crystal that has first been made amorphous through implantation. This type of damage is usually inflicted in shallow junctions when attempting to achieve extremely high doping concentrations. As will be discussed in section 2.9, amorphous crystal is to be avoided in compound semiconductors and so damage categories 2-5 are not reviewed further. Category 1 implant damage forms when the implantation dose is not sufficiently high enough to produce an amorphous region, and applies to light dopants at relatively low doses. The peak concentration of the implant damage is just short of the projected range and consists of point defects. Furnaces were originally used to activate implanted dopants at relatively low temperatures (500 – 550°C) which were found to be sufficient to achieve some degree of dopant activation. However, the low temperature annealing was found to cause the primary implant damage to coalesce and extended defects were produced if a doping density threshold was exceeded. The formation of the extended defects upon annealing was found to be relatively independent on implant energy, species and wafer orientation but occurred if the peak dopant concentration exceeded the critical density of $1.6 \times 10^{19} \text{ cm}^{-3}$. At the critical doping density, the additional atoms can no longer be accommodated by the lattice and significant stress is induced. Upon annealing the additional defects coalesce and the lattice

finds relief forming extended defect networks. The nature of the extended defects that form upon annealing is a function of annealing temperature. Annealing at 500 °C causes the point defects to coalesce forming stacking faults and rod like defects. At 700 °C the rod like defects and stacking faults are seen to dissolve, however, faulted dislocation loops begin to grow. Annealing at 900 °C causes the faulted dislocation loops to become perfect dislocation loops, and if the implantation dose was significantly above the critical dose, then a network of dislocation loops may form. The perfect dislocation loops are stable up to 1100 °C. For implants below the critical doping density, point defects do not coalesce upon annealing and are annihilated at a sufficient temperature.

The annealing temperatures required for Si causes significant dopant diffusion if held for a significant amount of time. Furthermore the long anneal times slow wafer production and creates a longer window for chamber contaminants to diffuse into the semiconductor. Rapid thermal annealing (RTA) was developed to solve these issues and is capable of achieving wafer temperatures in excess of 1000 °C with the annealing cycle lasting a matter of seconds. Rapid thermal annealing is achieved by passing a large current through two halogen lamps closely placed either side of two dummy wafers. The dummy wafers are used to absorb the lamp radiation and radiate the heat uniformly across the sample which is sandwiched between the dummy wafers. The temperature of the dummy wafers is monitored by a pyrometer and provides feed back to the lamp control. Pulsed laser annealing can be used for processes with extremely low thermal budgets with the laser pulse lasting a few nano seconds. Additionally the laser beam can be directed onto local regions of the wafer for selective area annealing applications. However, laser pulse annealing is time consuming and is avoided for mass production.

2.8 Hot implants

Implants with very high doses creating amorphous zones under damage category 2-5 are used to achieve high doping in Si. It was found that using an elevated target temperature, the threshold dose for creating amorphous regions in the crystal could be increased and the formation of defects reduced [22]. The reduction of implant damage with increasing implant temperature is attributed to dynamic annealing which used to describe the enhanced concurrent annealing during implantation due to the increased mobility of defects [23]. Hot implants are rarely used for Si fabrication as amorphous crystal is desired to achieve very high doping. The ability of Si to recrystallize with a very low defect density through annealing is one of the key components to its success. As will be discussed in section 2.9 the recrystallization of amorphous III-V semiconductors is problematic and producing

amorphous crystal to achieve high doping is not effective. For III-V semiconductors, focus is shifted towards to minimising implant damage which usually falls under damage category 1. For some compound semiconductors hot implants are an excellent way of minimising the damage sustained during implantation [24, 25], for example it was found that InAs could not be made fully amorphous under Si implantation if the sample was held at a temperature above 80 °C [26]. Additionally a much lower defect density was observed upon annealing compared to a sample implanted at cryogenic temperatures and annealed. Similar observations were also reported for Si implantation into InP at 150 °C and 180 °C for GaAs [25, 26]. It is widely accepted that there exists a critical threshold above which dynamic annealing becomes significant in compound semiconductors. At the critical temperature, significant shrinkage of primary implant damage clusters is observed due to thermally stimulated defect diffusion [27]. There has been little success in formulating an empirical expression to estimate the critical temperature of any given implant into any given material, and work exploring new ground is usually based upon an experimental approach. However trends observed across many pieces of work have enabled some rules of thumb to be derived which are as follows: wider bandgap materials, ions with high atomic mass and n-type dopants all require higher implant temperatures compared to their opposite [25, 27, 28]. However, little information exists to confirm if this trend continues outside of the most popular III-V semiconductors.

The implantation damage from Be and Mg ions into InAs at 200 keV was simulated using TRIM and is shown in Figure 2.9 and Figure 2.10 respectively. Damage clusters (local high numbers of point defects) are observed at the end of the projected range of the light Be ions and along the path of the Mg ions. The damage clusters are due to recoil cascades caused by recoiling In and As atoms shown by the pink and purple dots respectively. Displacements of either lattice atom caused by a collision with the implanted ion are shown by a white dot. It is clear that damage clusters form in InAs under implantation and so hot implants may prove to be effective in this material. However, no work has been previously published on this topic.

Hot implants are usually induced by elevating the temperature of sample holder in the implant tool, however dynamic annealing can be induced using a high beam current so that the heat created from the ion beam is large enough to promote significant dynamic annealing. However, the high beam current can cause uniform doping across large wafer areas.

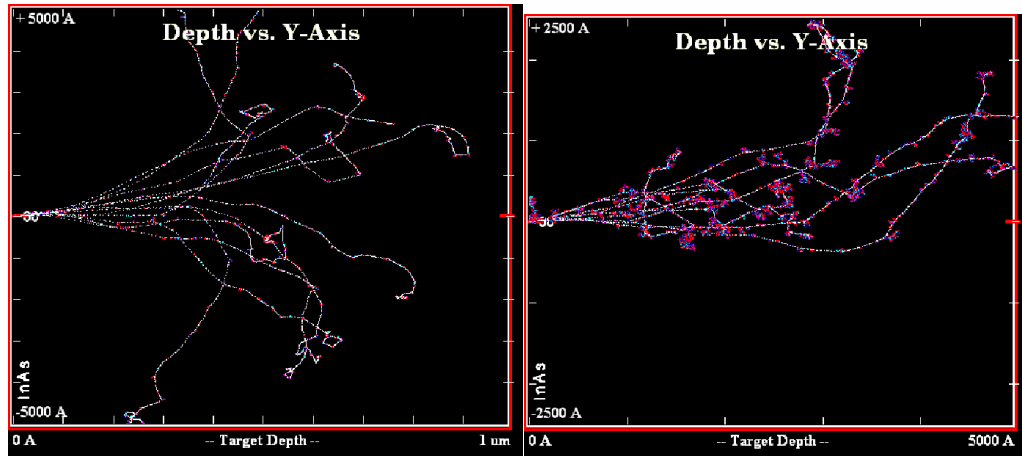


Figure 2.9: (Right) Be atoms implanted into InAs at 200 keV

Figure 2.10: (Left) Mg atoms implanted into InAs at 200 keV

2.9 Ion implantation and annealing in III-V semiconductors

Doping III-V semiconductors through implantation and annealing comes with increased difficulties compared to Si as both implantation and annealing cause local changes to the stoichiometry of a III-V semiconductor [20, 25, 29]. The loss in stoichiometry can be beyond the repair of annealing, and the residual implant damage can compensate the electrical activity of dopants [30]. This is further complicated since great differences in the activation of dopants and evolution of damage are observed across the III-V family from the sponge like surface created in InSb [31] to the amphoteric behaviour of group IV elements [32] to name the most extraordinary. Outgassing of the volatile group V element can occur during annealing causing a loss of stoichiometry at the semiconductor surface. These issues have encumbered the development of ion implantation techniques in III-V compounds [33]. Methods to reduce these effects have been developed and will be reviewed in the following section.

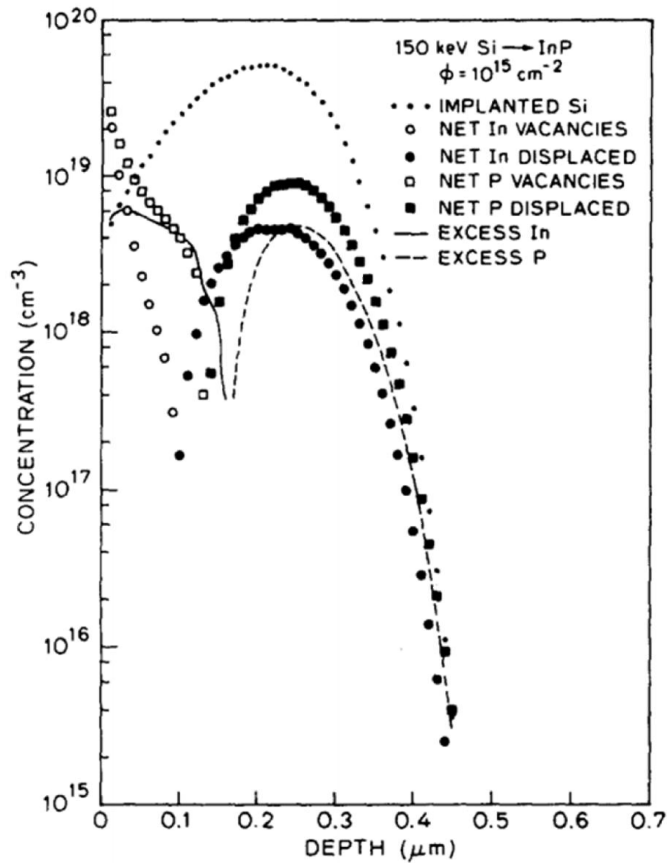


Figure 2.11: The stoichiometric distribution of InP implanted with $1 \times 10^{15} \text{ cm}^{-2}$ Si atoms at 150 keV [29].

The different physical properties of the constituents of a compound semiconductor cause them to display disparate recoil characteristics when involved in a nuclear collision. The ramification is that III-V semiconductors show a loss in local stoichiometry centred around the implantation profile as shown in Figure 2.11 for InP implanted with Si at a dose of $1 \times 10^{15} \text{ cm}^{-2}$ Si atoms at 150 keV [29]. The loss in stoichiometry is observed as a two stage process starting from a difference in the initial energy transfer to the recoiling atoms due to the lattice atoms having a dissimilar collision cross section. This then follows onto projected range of the recoiling atoms having distinctly different stopping distances as the stopping power is a strong function of atomic mass. However, in all binary III-V semiconductors, loss in stoichiometry is dominated by the difference in stopping distances rather than the difference in energy transfer characteristics. Consequently all III-V semiconductors have similar stoichiometric loss characteristics after implantation which can be described by an excess concentration of the heavy constituent elements at shallow depths and an excess of light constituent elements at great depths [29]. The transition point is around the peak of the implant damage profile where the greatest number of displacements occurs. This effect is exacerbated when the mass ratio between the constituent elements of a compound

semiconductor is high. For example, when implanting Si into InP as shown in Figure 2.11, the concentration of displaced lattice atoms is comparable to the dopant concentration and consequently, the net doping concentration is low. However, the constituent elements of GaAs are of similar mass and light Be atoms can be implanted with excellent activation and removal of the implant damage [34].

Severe loss in stoichiometry caused by implantation cannot be eliminated through annealing. This is due to the separation distance between the excess concentrations of displaced atoms being significantly greater than the migration distance the elements are able to diffuse over. Consequently the atoms needed to restore order to the lattice are not available upon annealing and an extended network of defects forms instead [29]. Unlike Si, recrystallization of highly damaged III-V semiconductor is poor and great emphasis is placed upon minimising the initial implant damage and avoiding amorphous crystal [23] which can be difficult when attempting to achieve very high doping concentrations. Reduction of the implant damage is primarily achieved by selecting implant species with a low atomic mass. Implants at elevated temperatures to encourage dynamic annealing are also particularly effective in III-V semiconductors as the implantation dose to achieve amorphous crystal is increased [25]. However, it should be noted that lower doping concentrations are generally achieved through implantation compared to epitaxially grown material [35].

The focus of much research on implantation into III-V semiconductors has been made on achieving high n-type doping for high speed n-MOS applications [33]. Si implantation is used for N-type doping due to its low diffusion coefficient enabling abrupt junctions to be fabricated [26, 36]. Additionally high dopant activation can be achieved compared to other donor elements such as C, S and Se [37]. However, high doses of Si are intertwined with high levels of implant damage. Consequently the doping activation is poor due to self-compensation and the formation of nearest neighbour neutral pairs [32, 38]. In order to reduce Si self-compensation, it has been suggested that a co implantation of the group V species can encourage Si to occupy group III lattice sites upon annealing and increase the net dopant activation [39]. However, co-implantation remains unpopular as incontrovertible evidence showing the benefits of co-implantation are still yet to be presented [40].

Annealing III-V semiconductors presents additional challenges compared to Si. The constituent elements of a compound semiconductor outgas at different rates which results in a stoichiometric imbalance remaining at the surface of the wafer after an annealing cycle if precautions are not taken [41]. In the case of III-V semiconductors, the group V elements are more volatile and outgas at a faster rate than the group III elements leaving the surface with

an excess concentration of the group III element. Three main techniques can be employed to prevent outgassing during annealing, these are generally referred to as overpressure, encapsulation or proximity anneals. Overpressure anneals are carried out in an atmosphere rich in the group V element preventing any outgassing. Encapsulation anneals are the most popular method of annealing and are carried out by coating the surface of the wafer with a thin film of material that acts as a physical barrier against outgassing. The encapsulating material is usually a dielectric that can withstand high temperature such as SiO_2 and must be a thin film to prevent mechanical stress on the wafer due to differences in thermal expansion coefficients. Proximity anneals are carried out with the sample sandwiched between two sacrificial wafers of the same material. An overpressure is created between the samples due to an initial outgassing which quickly diminishes once the overpressure is sustained. The drawback of this method is that there is a greater chance of incorporating impurities and causing damage to the sample surface when sandwiched between the sacrificial wafers.

2.10 Hotspots in planar APDs

Electric field hotspots are non-uniform localised regions of a P-N junction that develop a significantly higher electric field when reverse biased compared to the bulk of the device. Hotspots mainly develop as a result of the curvature of the depletion layer edge that forms as the junction is terminated. However, they can also occur due to irregularities in the device doping, geometry or contamination of the surface forming micro plasmas [42]. Hotspots are undesirable as they can trigger premature localised avalanche breakdown before significant gain has been developed in the bulk of the APD. Furthermore a large surface leakage current can be generated due to the enhanced surface electric field. In mesa APDs, a hotspot at the perimeter of the P-N junction can form if the bevel angle of the mesa is such that it causes the depletion region edge to pinch at the mesa surface. For example, the etching recipe used to fabricate InAs APDs produces a positive bevel angle of approximately 45° [43]. Consequently P-i-N APDs, where the intrinsic region is slightly N-type, develop a hotspot at the surface perimeter of the P-N junction as shown in Figure 2.12. Hotspots can be minimised in mesa P-i-N APDs by ensuring the bevel angle is close to 90° or by grading the doping in the P-type region.

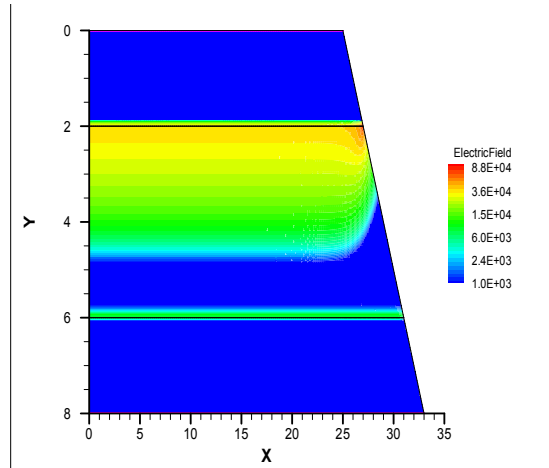


Figure 2.12: An electric field hotspot in a mesa P-i-N InAs APDs at -10 V

Planar junctions also suffer from hotspots developed along the arc of doping profile with the severity of a hotspot depending on the junction geometry. A rectangular doped region will contain both cylindrical and spherical geometries formed along each of the edges and at the corners of the rectangle respectively. Hotspots formed at the cylindrical junction (the corners of the rectangle) will breakdown at a significantly lower voltage compared to the spherical junction (along the sides of the rectangle). APDs are usually based upon a circular geometry to avoid cylindrical junctions. In a spherical junction the premature breakdown voltage as a proportion of the bulk breakdown voltage is directly related to r_j/w_d where r_j is the radius of the junction and w_d is the depletion width. In order to develop high gain in InAs APDs the depletion region width is required to be very thick compared to the P-type layer thickness. Consequently InAs APDs are expected to develop severe hotspots as confirmed by the electric field simulation of the cross section of a planar InAs APD at -10 V as shown in Figure 2.13. However, InAs may be more tolerant of hotspots compared to other semiconductors as there is a large electric field range over which only electrons impact ionise. Therefore InAs APDs can develop significant gain across the bulk of the device before the breakdown conditions in a hotspot are reached. In a semiconductor bearing similar impact ionisation coefficients, the gain is observed to increase rapidly with electric field, and consequently breakdown conditions will be reached before significant gain is developed across the bulk of the APD. To avoid premature breakdown and ensure low excess noise in InAs APDs, hole impact ionisation must be suppressed which becomes significant at 70 kVcm^{-1} . Furthermore, 70 kVcm^{-1} is the electric field strength at which tunnelling current becomes significant compared to the dark current as shown in Figure 2.14. Therefore the InAs APD shown in Figure 2.13 will not have broken down.

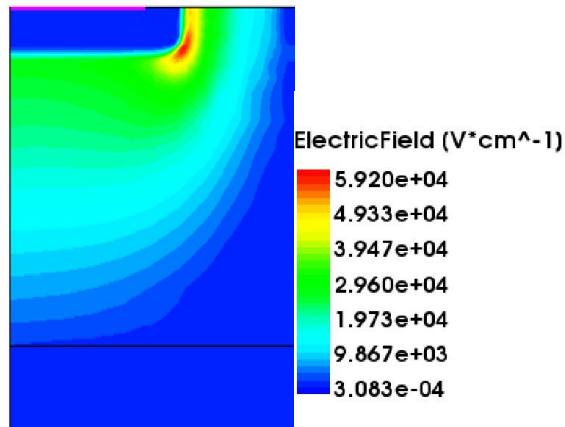


Figure 2.13: The electric field of a planar InAs APDs at -10 V reverse bias

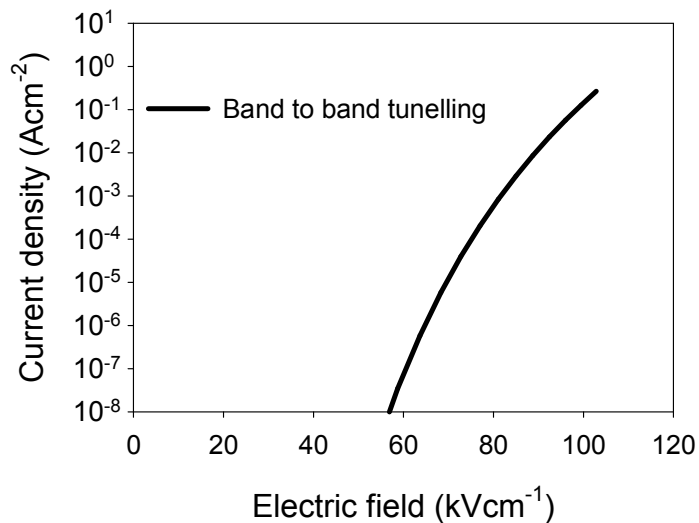


Figure 2.14: Current density due to band to band tunnelling current as function of electric field within a 2 μm thick InAs APD.

2.11 Methods of mitigating hotspots in planar APDs

Avoiding sharp corners only plays a small part in preventing premature breakdown in planar APDs and without any protection, premature breakdown is almost inevitable. There are two main methods of preventing edge breakdown 1) altering the local space charge directly underneath the main junction 2) incorporate floating guard rings to modulate the lateral electric field by forming equipotential surfaces that act to spread out the equipotential lines. Altering the space charge directly underneath the main junction can be achieved using ion implantation to form a buried layer of dopants. As the depletion region extends from the

junction, the peak electric field increases rapidly under the junction as it depletes through the buried charge layer. The low background doping at the edge of the junction enables the depletion region to grow freely enabling the peak electric field within the device to be developed underneath the main junction. This method works particularly well for homogenous APDs with relatively thick depletion regions such as Si APDs. An alternative method is used for InGaAs/InP SAMAPDs as the thin multiplication region, sensitivity to implant damage and complexity of heterojunction interfaces, makes implanting a buried charge sheet impractical in these devices. A step profile is formed in the P-type region using a double diffusion to produce a highly doped region extruding from the main junction. The intrinsic region between the extruded P-type region and N type region is narrowed and consequently the peak electric field within this region increases rapidly with applied bias compared to the thicker region at the edge of the APD. A double diffused junction is particularly effective in thin APDs, however, this method alone is not always sufficient to prevent edge breakdown. Floating guard rings can be used in addition to the double diffused junction to completely eliminate edge break down [44]. Floating guard rings are concentric doped regions that are isolated from the main junction forming back-to-back junctions laterally across the device. As the main junction is reverse biased the depletion region grows laterally eventually reaching the first floating guard ring. Once the guard ring has been reached the depletion region punches through the guard ring and continues depleting again from its other edge. The guard rings should be carefully placed so that punch through occurs before the electric field in the hotspot at the main junction becomes excessively large. After punch through the guard ring acts as an equipotential surface and limits the maximum electric field on the main junction and spreads the equipotential lines laterally. After punch through increasing the reverse bias of the APD causes a hotspot to build up on the guard ring edge. Multiple guard rings can be cascaded to suppress edge breakdown, however, the guard ring placement should be optimised so that the APD does not become excessively large.

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3 Experimental methods

Measurement and interpretation of data are both equally important for the correct characterisation of any system. APD noise and photon detection efficiency are primary performance markers and together determine the sensitivity of a detector. The performance of detectors is generally characterised by the signal to noise ratio under a given set of conditions. The noise equivalent power, NEP, given by equation (3.1), represents the optical power required to produce a unity signal to noise ratio within a bandwidth of 1 Hz where, R_{res} , is the responsivity. It has been assumed that the detector generates negligible Johnson noise. The noise component, I_{nAPD} , is therefore the multiplied shot noise of the total primary dark current as defined in equation (2.6). Contributions from 1/f noise have been ignored. I_{nAPD} is proportional to the detector area, and therefore NEP comparisons across detectors with significantly different optical areas can be misleading. The area normalised version, given in (3.2), is called the detectivity, D^* , where A is the detector area.

To characterisation an APD, it is necessary to perform electrical and optical measurements with current-voltage (I-V), capacitance-voltage (C-V), spectral response, responsivity and gain utilised in this thesis. Measurement details and interpretation methods are presented in this chapter.

$$NEP = \frac{I_{nAPD}}{R_{res}M} \quad (3.1)$$

$$D^* = \frac{\sqrt{A}}{NEP} \quad (3.2)$$

3.1 Current-Voltage

The noise of an APD is generated by excess noise and the dark current, and due to the unfavourable ionisation coefficients of most semiconductors, it is usually the excess noise that dominates at high gain. However, the electron dominated impact ionisation observed in InAs APDs ensures that the excess noise factor never exceeds a value of 2. Furthermore, the narrow bandgap of InAs generates a very large dark current at room temperature and consequently, control over the dark current becomes the focus of design efforts. The susceptibility of the InAs surface to high surface leakage and the intrinsic narrow bandgap make for a plethora of leakage mechanisms for generating dark current in InAs APDs.

Measurement and interpretation of the I-V characteristics is therefore highly important for evaluating performance and setting future direction.

3.1.1 Measurement details

Room temperature I-V measurements are usually the first measurement be performed on the device under test (DUT) as the forward I-V characteristics can yield the series resistance while the reverse can be used to assess contributions to the dark current from bulk and surface leakage indicating the quality of the fabrication and uniformity. I-V measurements at room temperature were performed using an Agilent B1505A, Keithley 236 source measurement unit (SMU) or HP4140B pico-ammeter. Electric contacts were made to the DUT using tungsten probes on a mechanical XYZ mount for the top contact. The back contact was placed onto a metal plate and connected to with an additional probe. Due to the high dark currents at room temperature, it is critical to ensure that the probe does not add series resistance that will generate a significant voltage drop. This can be achieved by ensuring that the probe tip is sharp and the metal back contact is clean. The planar InAs APDs were found to be sensitive to mechanical damage caused during probing and applying too much pressure, or measured in a mechanically noisy environment, i.e. vibrations from a pump, could significantly degrade the device performance. Mechanical robustness was achieved using a remote bond pad for probing as shown in Figure 3.1. Packaging APDs onto a TO-5 header with wire ball bonding to the remote band pad proved to be an even better method for reliability, however, bonding was only explored after work in this thesis was complete. I-V measurements were performed in low light levels to ensure negligible photocurrent. Measurements were performed on devices with a range of diameters and from various locations across the sample and assigned with a unique identification number to characterise the uniformity.

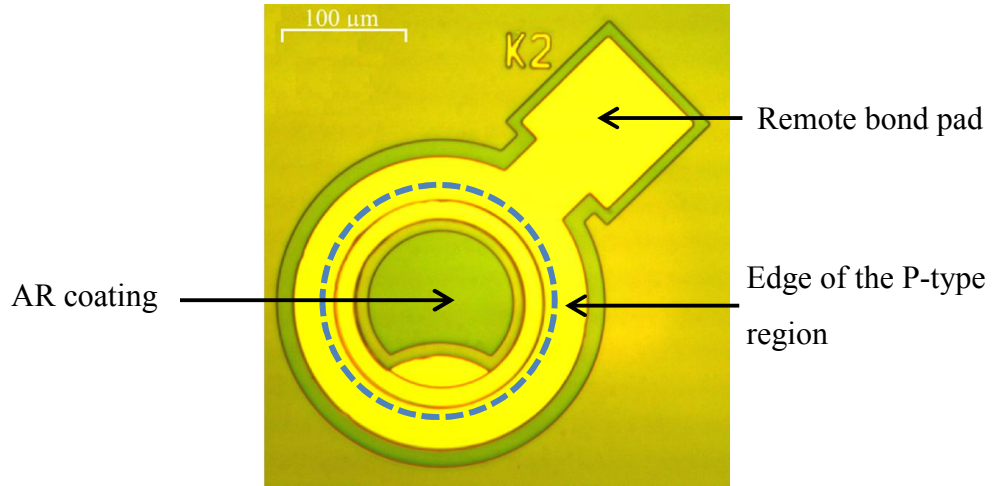


Figure 3.1: A photograph of a planar InAs APD with the edge of the P-type region indicated.

If APDs across a sample show high uniformity, it is possible to characterise the total primary dark current density (J_{tot}) of APDs of any size into bulk current density (J_b) and a surface leakage per unit length (J_s) so to characterise the sample. If surface leakage is negligible the total leakage of APDs with a range of diameters will be identical. This is commonly observed by plotting the current density-voltage (J-V) characteristics of APDs with a range of diameters on a single graph. However, diodes with a small radius generally have a larger total dark current density indicating significant surface leakage. The contributions to the total dark current due to bulk and surface leakage components at a given voltage can be calculated accurately by fitting J_b and J_s to experimental data using equation (3.3). Inspection of equation (3.3) shows that the ratio of surface to bulk leakage current increases with decreasing diode radii highlighting the importance of control over the surface conditions in small area APDs.

$$J_{tot} = J_b + J_s \quad (3.3)$$

$$\text{Where } J_b = \frac{I_b}{\pi r^2} \text{ and } J_s = \frac{I_s}{2\pi r}$$

3.1.2 Surface leakage

Surface leakage can be significant due to a high density of surface states, contamination of the surface, loss in stoichiometry or the formation of a highly conductive oxide layer. Due to the large number of variables, surface effects are difficult to model and the J_s -V characteristics unpredictable. Removal of the surface leakage current is achieved through optimising the fabrication procedure.

3.1.3 Bulk leakage

Bulk leakage of APDs is more predictable with well-defined models for all common leakage mechanisms. Figure 3.2 shows common bulk leakage mechanisms in a reverse bias P-i-N diode. Mechanisms 1 (7) and 2 (8) are band to band and trap assisted minority carrier generation in the P-type (N-type) region respectively. The minority carriers able to diffuse to the intrinsic region are separated in the electric field. Carriers generated within the intrinsic region are immediately separated by the electric field with generation mechanisms 3 and 4 describing band to band and trap assisted or SRH generation respectively. Mechanisms 5 and 6 describe trap assisted tunnelling and band to band tunnelling respectively.

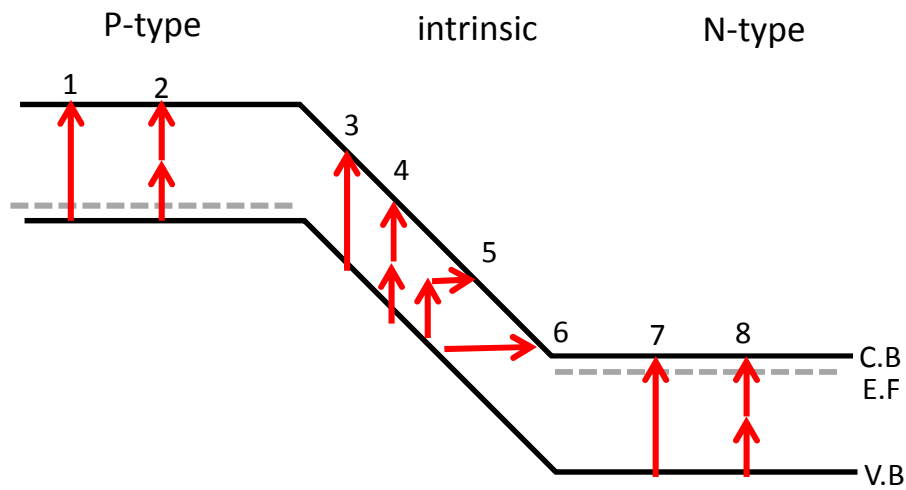


Figure 3.2: Common bulk leakage mechanisms in a reverse bias P-i-N diode.

Diffusion current:

The J-V characteristics of an APD due to diffusion current density, J_{diff} , can be described by equation (3.4), also called the ideal diode equation [1], where k is the Boltzmann constant, T is the absolute temperature, n_i is the intrinsic carrier concentration, D_n and D_p are the minority carrier diffusion coefficient, L_n and L_p are the minority carrier diffusion length, and N_A and N_D are the acceptor and donor density respectively. The diffusion current density approaches that of the saturation current density (J_0) in a reverse bias diode. Consequently, diffusion limited dark currents are characterised by a fixed dark current with increasing reverse bias voltage. This can often be observed in InAs APDs up to reverse bias voltages of 0.5 V. A key goal for reducing the diffusion current is to utilise highly doped cladding layers to ensure a large majority carrier concentration, however, this must be achieved without reducing the minority carrier diffusion length.

$$J_{diff} = J_0 \left(\exp\left(\frac{qV}{kT}\right) - 1 \right) \quad (3.4)$$

$$\text{Where } J_0 = q \left(\frac{D_n n_i^2}{L_n N_A} + \frac{D_p n_i^2}{L_p N_D} \right)$$

Generation-recombination:

Carriers generated within the depletion region are immediately separated by the electric field and such current generation is referred to as the generation-recombination current density. The generation-recombination current density due to band to band transitions, J_{GRBB} , can be calculated using equation (3.5) where w is the depletion width and b is the recombination constant. Upon first impression the generation current is observed to show the same voltage dependence as the diffusion current. However, the depletion width increases linearly with reverse bias voltage within a one side abrupt junction.

$$J_{GRBB} = q n_i^2 w b \left(\exp\left(\frac{qV}{kT}\right) - 1 \right) \quad (3.5)$$

Band to band generation currents are seldom observed as trap assisted generation is dominant in most semiconductors. In name of the authors publishing the first derivations, Shockley Read Hall generation describes trap assisted generation via a trap state within the bandgap [2, 3]. A highly simplified equation for calculating the SRH current density, J_{SRH} , is given by equation (3.6) where τ_{eff} is the effective carrier lifetime. The SRH process is proportional to the n_i rather than n_i^2 , and therefore significantly less temperature dependent compared to band to band or diffusion processes. SRH leakage is often the dominant mechanism in relatively wide bandgap semiconductors at room temperature while becoming significant in narrow bandgap semiconductors at low temperatures. SRH generation is the dominant leakage mechanism in InAs below temperatures of ≈ 175 K. The carrier lifetime is directly related to the crystal quality, and therefore SRH currents are an indicator of growth quality.

$$J_{SRH} = \frac{q n_i w}{2 \tau_{eff}} \left(\exp\left(\frac{qV}{2kT}\right) - 1 \right) \quad (3.6)$$

Tunnelling:

Classically, carriers can only escape a potential well once they have gain energy equal to, or greater than the barrier height containing them. Tunnelling is a quantum mechanical phenomenon which, due to the wave-like behaviour of electrons, enables carriers to tunnel through a potential barrier so long as a free state at the same energy level is available for the carrier to tunnel into. Band bending in a reverse biased a diode causes energy states within the conduction band and valence band to align forming an effective potential barrier. The probability of a carrier tunnelling through a barrier is inversely proportional to the barrier

width, therefore, the magnitude of the tunnelling current increases significantly with reverse bias voltage. The tunnelling current density in a reverse bias diode can be calculated using equation (3.7) [4] where \hbar is the reduced Planck constant, m^* is the combined effective mass, and a is a fitting parameter to adjust for the effective shape of the potential barrier. Due to the dependence on bandgap energy and effective mass, tunnelling currents in InAs APDs can be large before gain is developed. For example, the tunnelling current density at 70 kVcm^{-1} is $\approx 1 \times 10^{-5} \text{ Acm}^{-2}$ in a typical InAs APD. Therefore to achieve high gain and low tunnelling current, thick avalanche regions are required.

$$J_T = \frac{(2m^*)^{1/2} q^3 \xi V}{4\pi^2 \hbar E_g^{1/2}} \exp\left(-\frac{am^{*1/2} E_g^{3/2}}{q\hbar\xi}\right) \quad (3.7)$$

Forward I-V characteristics:

When forward biased, the voltage dependence of the pre-exponential term of the SRH current density is negligible and therefore can be assumed to be a constant, C , as can I_0 of the ideal diode equation. The similarity between the remaining terms enables a single variable, n , termed the ideality factor, to be used to represent both equations as shown in equation (3.8). Fitting of C and n to a diodes forward bias current reveals the dominant leakage mechanism in the forward bias. An ideality factor close to 1 indicates diffusion current while a value closer to 2 signifies generation and recombination process. The I-V characteristics of a diode in equilibrium will pass through the origin, however, due to the photovoltaic effect an optical flux can generate a significant open circuit voltage. The effects of photocurrent, I_{ph} , can be accounted for as shown in equation (3.8). Forward biasing the diode also causes a large current to flow through the diode. At high currents the series resistance becomes significant compared to the dynamic resistance and can cause a significant voltage drop. The series resistance can also be included in equation (3.8) with an iterative solution required to simulate the forward I-V characteristics. It is important to minimise the series resistance of diodes to increase the RC bandwidth.

$$I = C \left(\exp\left(\frac{q(V-IR)}{nkT}\right) - 1 \right) - I_{ph} \quad (3.8)$$

Shunt resistance:

Any non-rectifying leakage current component of a diode is usually attributed to the shunt resistance, R_s , described by equation (3.9). The shunt resistor provides an alternative current path for photocurrent and can cause power loss and non-uniform responsivity. The shunt resistance is most commonly applied to the dynamic impedance around 0V as the bulk rectifying leakage is very low.

$$R_s = \frac{V}{I} \quad (3.9)$$

Multiplied dark current:

All bulk leakage mechanisms, except for shunt resistance, can be multiplied by the avalanche gain of the APD. With knowledge of the generation profile, SRH and tunnelling currents generated at positions x within the multiplication region are multiplied by $M(x)$ calculated using equation (2.2). The diffusion current is multiplied by $M(0)$ or $M(w)$.

3.2 Capacitance-Voltage

C-V characterisation techniques can be used to determine the depletion region width, the doping profile and the built in potential of a diode. However, accurate C-V measurements on InAs APDs are challenging.

3.2.1 Measurement details

The C-V characteristics were measured using a HP4275LCR meter. The capacitance of the APD was calculated through measurements of the imaginary current, I_A , using an AC test signal of known amplitude, V_A , and frequency, f , as shown in equation (3.10). The AC test signal can be added onto a DC bias to determine the C-V characteristics of an APD. The amplitude of the test signal should remain small compared to the DC bias to ensure that the test signal does not cause significant DC biasing errors. The amplitude of the test signal was a factor of 0.1 of the applied bias voltage. As the capacitance of the APDs measured was of the order of a few pF, I_A was very small and sensitive to noise. Accurate measurement was only possible if the dark current of the APD was significantly less than the value of I_A . Due to the high dark current of InAs APDs at room temperature, all C-V characterisation presented in this thesis was carried out at 77K in a Janis low temperature probe station. The measurement phase angle was greater than 75° in all measurements to maintain an acceptable signal to noise ratio. High frequency test signals can be utilised to maximise I_A , however, high frequency measurements necessitate impedance matching of all components to minimise reflections. The Janis probe station measured a bandwidth of 10 MHz using unshielded probes, and therefore to avoid significant signal loss, measurements were performed using 1 MHz test signals. Significant measurement error can also be introduced through improper shielding of cables and isolated ground planes. This was evident if the C-V meter measured significant stray capacitance as the zero offset adjustment function could not execute.

$$C = \frac{I_A}{2\pi f V_A} \quad (3.10)$$

3.2.2 One sided abrupt junction approximation

The depletion width at a given bias voltage can be calculated using equation (3.12) where ϵ_r is the relative permittivity. A fully forward bias diode has zero capacitance as no depletion region exists. This effect can be used to calculate the built in potential, V_{bi} , of a diode, however, the capacitance cannot be measured under the high leakage currents of a forward bias diode. A plot of $1/C^2$ versus the applied voltage for a one side abrupt junction has a linear dependence as shown in equation (3.12) and the characteristic can simply be extrapolated to find the voltage at which $1/C^2 = 0$. The background doping concentration, N_i , at the depletion region edge can be calculated using equation (3.13). This technique is frequently used to calculate the background doping concentration of the intrinsic region of P-i-N structures.

$$w = \frac{\epsilon_0 \epsilon_r A}{C} \quad (3.11)$$

$$\frac{1}{C_j^2} = \frac{2}{q \epsilon_0 \epsilon_r N_i} (V_{bi} - V) \quad (3.12)$$

$$N(w) = \frac{2}{\epsilon_0 \epsilon_r q A^2} \left(\frac{dV_{bi}}{d\left(\frac{1}{C^2}\right)} \right) \quad (3.13)$$

3.2.3 One dimensional Poisson solver

After the depletion region has extended through the intrinsic region the assumption of a one sided abrupt junction is invalid. C-V characteristics can be fitted against a model to characterise the doping profile in the cladding layers. In house software based upon a one dimensional Poisson solver was utilised to model C-V characteristics of APDs with a full description available from [5].

3.3 Gain and Responsivity

The external quantum efficiency, η , of a detector is the fraction of incident photons that contribute to the photocurrent. Broken down into key components, a general expression for η is given by equation (3.14) where, R_{opp} , is the reflectance, α_{opp} , is the optical absorption

coefficient, d_{eff} , is the effective device thickness and, S , is the device average carrier collection efficiency.

$$\eta(\lambda) = S(1 - R_{\text{opp}})(1 - \exp(-\alpha_{\text{opp}}(\lambda)d_{\text{eff}})) \quad (3.14)$$

Although external quantum efficiency is a good marker of performance, the number of photons, and therefore the photocurrent, for a given optical power is related to photon energy. Responsivity, R_{res} , is a more convenient unit defined as the photocurrent per unit optical power, and is given in equation (3.15) where h is the Planck constant and v is the speed of light. The gain can be integrated into the responsivity so that over 100 % external quantum efficiency is possible, however, they are discussed as separate entities in this thesis.

$$R_{\text{res}} = \frac{\eta e}{h\nu} \quad (3.15)$$

3.3.1 Measurement details

An Agilent 8168C was used to perform responsivity measurements. The laser was focused onto the P-type region of the APD using lenses, or through coupling the laser into a single mode optical fibre and positioning the fibre close to the device to minimise divergence. To ensure all optical power was absorbed in the P-type region, responsivity measurements were performed on APDs with a diameter of 400 μm . As gain is a relative measurement, complete optical absorption is not required, however, the injection conditions must be accurately known. To ensure pure electron injection the APDs were designed with metal plating surrounding the edge of the P-type region as shown in Figure 3.1.

A schematic diagram of the setup is shown in Figure 3.3. The dark current was significant compared to the photocurrent and therefore the photocurrent was measured using phase sensitive detection using a SR830 lock-in amplifier (LIA). The phase sensitive detection method is discussed below. A sense resistor of 10 Ω was used to create a small photovoltage while incurring a negligible voltage drop due to the dark current. The laser was internally modulated providing the reference for the LIA. The responsivity can be calculated using equation (3.16) where P_{opp} is the optical power. If referring to the avalanche gain as a separate entity to the responsivity, precautions must be taken when defining the gain. Both the gain and responsivity increase with reverse bias voltage due to increased carrier collection efficiency from the depletion region extending into the cladding. While the avalanche gain is abrupt, the increase in carrier collection efficiency can be approximated by a simple linear relationship. A base line correction can be applied to extrapolate the primary

photocurrent, I_{pr} at a given voltage. Once the base line correction has been applied, the gain for a given bias can be calculated. Due to the long minority carrier diffusion length in P-type InAs, and the low voltages at which impact ionisation occurs, base line corrections are not necessary when performing gain measurements on InAs APDs.

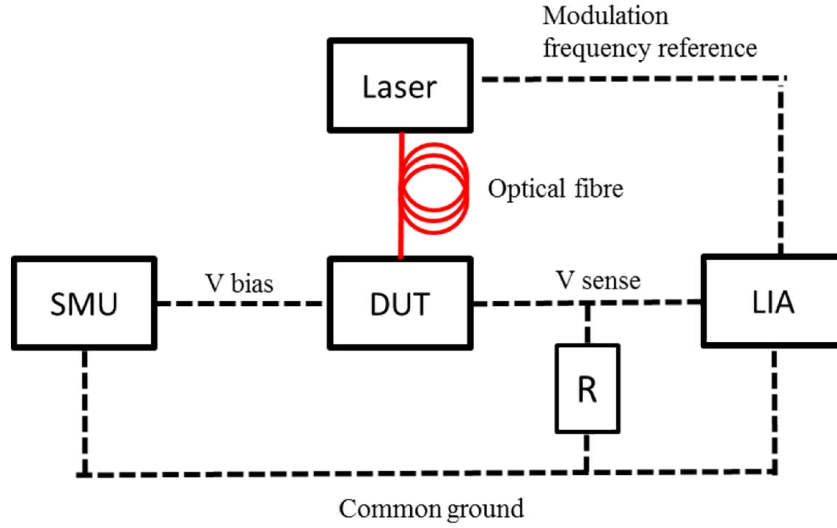


Figure 3.3: A schematic diagram of the photocurrent and gain setup

$$R_{res} = \frac{\sqrt{2}\pi P_{opp} V_{LIA}}{2R} \quad (3.16)$$

The LIA consist of a frequency mixer and a low pass filter. The photovoltage of amplitude, V_{ph} , phase, θ_{ph} and angular frequency, ω_{ph} , is multiplied by the sinusoidal reference voltage of amplitude, V_{ref} , phase, θ_{ref} and angular frequency, ω_{ref} , producing the phase sensitive voltage, V_{PSD} , given by equation (3.17). Expansion of the term, as shown in (3.18), reveals that the phase sensitive voltage contains two components. When the reference and the photovoltage are at the same angular frequency, the first term of (3.18) becomes DC and can be extracted using a high order low pass filter removing much of the noise. The clean DC phase sensitive voltage, given in equation (3.19), is proportional to the photovoltage amplitude. However, the phase sensitive voltage is also dependent on the phase lag between the signal and reference voltage. The phase dependence can be eliminated using a second phase locked loop mixing the original signal with the reference signal shifted by 90° . After expanding and taking the low pass component the second phase sensitive voltage, V_{2PSD} , becomes the same as (3.19) except with a phase difference relationship described by sine. V_{PSD} and V_{2PSD} can therefore be treated as vector coordinates and the phase dependence can be removed by calculating the absolute value.

$$V_{PSD} = V_{sig} V_{ref} \sin(\omega_{sig} t + \theta_{sig}) \sin(\omega_{ref} t + \theta_{ref}) \quad (3.17)$$

$$V_{PSD} = 0.5V_{sig}V_{ref}\cos\left((\omega_{sig} - \omega_{ref})t + \theta_{sig} - \theta_{ref}\right) - 0.5V_{sig}V_{ref}\cos\left((\omega_{sig} + \omega_{ref})t + \theta_{sig} + \theta_{ref}\right) \quad (3.18)$$

$$V_{PSD} = 0.5V_{sig}V_{ref}\cos(\theta_{sig} - \theta_{ref}) \quad (3.19)$$

The LIA displays the RMS value of the photovoltage. However, the laser used to perform gain and responsivity measurements was modulated by a square wave with a 100% extinction ratio. As the low pass filter of the LIA is very narrow, only the magnitude of the fundamental component of the signal is measured which is a factor of $2/\pi$ of the true photovoltage. Furthermore, the RMS value is measured requiring further correction by $\sqrt{2}$ which has also been applied to (3.16).

3.3.2 Anti-reflective coating

The reflected optical power from an uncoated semiconductor surface is $\approx 30\%$ accounting for considerable inefficiency. An anti-reflective (AR) coating is an optically transparent film covering the optical window of a detector that minimises the reflected optical power. The thickness of the AR coating is designed so that reflections from the AR coating are out of phase with those reflected from the semiconductor surface. The product of the reflected waves destructively interferes minimising the total reflected power. For a single layer AR coating the thickness of the AR coating, d_{arc} , should be equal to one quarter the wavelength within the AR coating. Reflections are completely eliminated when the reflected power from the AR coating and semiconductor are of equal magnitude. Equal reflected power is achieved when the refractive index of the AR coating, n_{ARC} , is equal to the geometric mean of the refractive index of the surrounding material. For InAs and Air with refractive indexes of 3.5 (at an optical wavelength of $2 \mu\text{m}$) [6] and 1 respectively, an ideal AR coating should have a refractive index of 1.87 as calculated using equation (3.20). The refractive index of SiN was measured to be 1.98 using ellipsometry techniques and using a 250 nm layer, the reflected optical power at $2 \mu\text{m}$ was theoretically reduced to 0.3% as calculated using equation (3.17). AR coating of this design was utilised on APDs presented in chapter 5. Single layers AR coating can only be optimised for a single wavelength, however, many optical measurements in this thesis were performed at $1.55 \mu\text{m}$. The reflectivity spectrum of a single layer AR coating can be calculated using equation (3.22) as plotted in Figure 3.4. The dispersion of InAs over this spectrum was not accounted for. The reflected power at $1.55 \mu\text{m}$ was calculated to be only 8%. A broadband response can be achieved using a multi-layer AR coating that provided significantly greater design flexibility.

$$\eta_{ARC} = \sqrt{\eta_{InAs} \eta_{air}} \quad (3.20)$$

$$d_{ARC} = \frac{\lambda}{4\eta_{ARC}} \quad (3.21)$$

$$R = \frac{r_a^2 + r_b^2 + 2r_1 r_2 \cos(2\theta)}{1 + r_a^2 r_b^2 + 2r_1 r_2 \cos(2\theta)}$$

where $r_a = \frac{\eta_{air} - \eta_{ARC}}{\eta_{air} + \eta_{ARC}}$, $r_b = \frac{\eta_{ARC} - \eta_{InAs}}{\eta_{ARC} + \eta_{InAs}}$ (3.22)

$$\theta = \frac{2\pi\eta_{ARC}d_{ARC}}{\lambda}$$

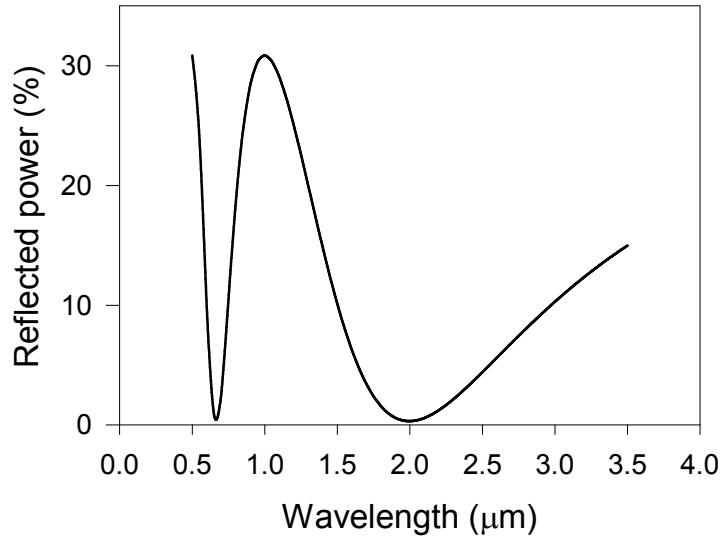


Figure 3.4: The calculated reflected optical power spectrum from a 250 nm layer of SiN on InAs

3.3.3 Optical absorption coefficient

The optical generation rate, G_{opp} , at depth, x , within a semiconductor is given by equation (3.23) where N_0 is the photon flux density. The normalised photo generated carrier distribution plotted in Figure 3.5 for wavelengths of 633 nm, 1.55 μm and 3.1 μm with optical absorption coefficients of $1.5 \times 10^5 \text{ cm}^{-1}$, $1.1 \times 10^4 \text{ cm}^{-1}$ and $5 \times 10^3 \text{ cm}^{-1}$ respectively [7].

$$G_{opp}(x) = (1 - R_{opp})N_0\alpha_{opp}\exp(-\alpha_{opp}x) \quad (3.23)$$

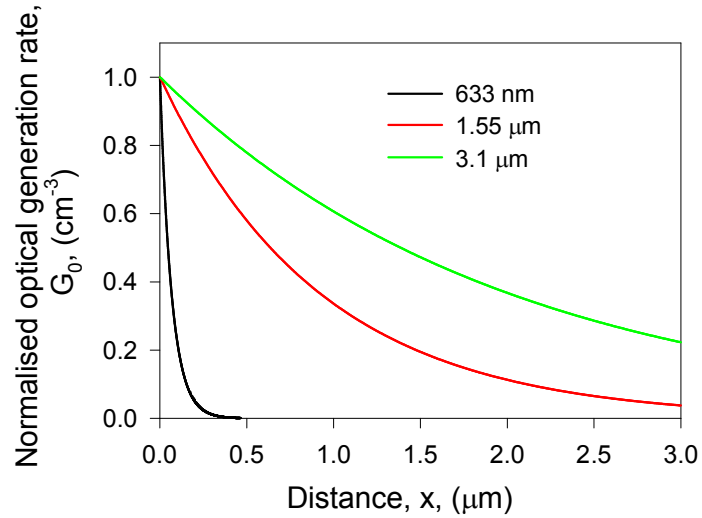


Figure 3.5: The normalised optical generation profile of 633nm and 1.55 and 3.1 μm photons in InAs.

3.3.4 Carrier collection

As shown in Figure 3.5 the optical generation rate is largest at the surface of the semiconductor. However, the surface of most semiconductors is characterised by a very high recombination rate caused by the excessively high defect density as the semiconductor terminates. As a larger proportion of carriers are generated near the surface at shorter wavelengths, the high surface recombination rate causes detectors to have a short cut off wavelength. Carriers injected away from the surface of the cladding layers are required to diffuse through to the depletion region edge to be collected. Therefore only carriers generated within the order of 1 minority carrier diffusion length are collected. Carriers absorbed within the intrinsic region of a P-i-N diode are immediately separated by the electric field making for a device with highly efficient and a very fast response time. However, for an APD, consideration must also be given to the excess noise and gain performance. The highest gain and lowest excess noise of an InAs APD is achieved using pure electron injection from the P-type region relying on diffusion to maintain responsivity. As shown in Figure 3.5, the thickness of the P-type region is required to be over 3 μm for > 99 % absorption at wavelengths longer than 1.55 μm. However, minority carrier diffusion length in P-type InAs has been reported to be in excess of 10 μm [8] nullifying the trade-off, and low excess noise and high responsivity APDs have been reported [9].

3.4 References

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4 Optimisation of Be implantation and annealing to fabricate planar InAs avalanche photodiodes

4.1 Introduction

It was widely believed that InAs APDs would suffer from unavoidable high surface leakage currents due to a heavy surface accumulation of electrons caused by fermi level pinning at the InAs surface. From 2005 – 2009 A. Marshall pioneered InAs APD developing wet chemical etching procedures that controlled the surface leakage and enabled the impact ionisation coefficients to be characterised. The difficulty in controlling the surface leakage in InAs is thought to be due oxidation forming a highly conductive indium oxide surface layer and not due to fermi level pinning [1]. However, the surface chemistry of InAs remains poorly understood and batch to batch variations in the I-V characteristics of mesa InAs APDs can be significant. Furthermore, suppressing the surface leakage at low temperatures or in small devices remains challenging. Early InGaAs/InP APDs were mesa devices, however, a planar structure was adopted for higher reliability and uniformity [2] [3].

In this chapter Be ion implantation and annealing conditions were optimised to demonstrate a method for selective area P-type doping in InAs. A fabrication procedure to produce highly uniform diodes was subsequently developed. The planar diodes showed low surface leakage and good lateral junction confinement. SIMS measurements were used to assess the diffusion of Be caused by annealing. The work from this chapter is published in [4].

4.2 Review of implantation and annealing in InAs for P-type doping

There is very little literature on implantation and annealing in InAs, however, it is clear that the implant damage should be minimised when attempting to dope InAs through ion implantation. Gerasimenko et. al [5] found Mg implantation into InAs to be ineffective for P-type doping and it was speculated that the radiation defects coalesced upon annealing forming extended defects which cancelled out the usual acceptor like behaviour of Mg. This result is slightly surprising as Mg implantation has been successfully used for P-type doping in InSb and InP which could be argued that are more sensitive to implant damage. InSb has a bandgap energy that is half that of InAs while InP has one of the lowest constituent element mass ratios out of the III-V semiconductor family at (0.27) compared to InAs at (0.65)

causing a significantly larger stoichiometric disturbance [6]. However, the peak doping concentration used in the study was $3 \times 10^{19} \text{ cm}^{-3}$ which is likely to approach the saturation limit of Mg within InAs although a reference to this could not be found. Doping to such high concentrations may cause extended defects to form upon annealing due to the excess concentration of Mg rather than being due to irreparable implant damage. Furthermore, anneals for a duration of 30 minutes were used resulting in severe dopant diffusion. Wang et al. [7] have reported the damage accumulation and lattice strain of Be implanted into InAs. Using an implant energy of 80 keV and a dose of $4 \times 10^{13} \text{ cm}^{-2}$, creating a peak Be concentration of $1.1 \times 10^{18} \text{ cm}^{-3}$, minimal lattice strain is introduced to the crystal and only point defects are formed during the implant. The effects of annealing on the implant damage were not explored in the study, nor were the electrical properties of Be implanted InAs tested.

Only these two studies were found in the literature that reported ion implantation into InAs for P-type doping, and due to the vast differences between the experimental procedures used, direct comparisons across the studies to select the better suited dopant are of no consequence. However, minimising implant damage is the key aim of implantation into III-V semiconductors and simulations using TRIM show that Be ions implanted at 200 keV will produce 3.7 times fewer vacancies per ion compared to Mg ions implanted at the same energy as shown in section 2.6. Furthermore, Be implantation is popular for P-type doping in a wide variety of other III-V semiconductors [8-10] and a commonly used dopant in the epitaxial growth of InAs. TRIM simulations have shown that significant damage clusters may form at the end of the projected range of the Be ions. Therefore hot implants may be beneficial to reduce the implant damage by encouraging dynamic annealing.

The redistribution of Be after annealing has shown to be significant at temperatures of 450 °C using furnace annealing for times of 30 mins [11]. However, the redistribution of Be from rapid thermal annealing has not been made clear. Furthermore, simulation software TRIM has been reported to be produce errors of up to 24 % when simulating the straggle Be implants into InAs [12].

4.3 Fabrication of P-i-N mesa diodes using Be implantation

Minimum noise in an InAs APD is achieved when all of the photons are absorbed within the P-type region of the device, so that pure electron injection is obtained. Using 1550 nm excitation (the wavelength at which the optical testing will be carried out) over 4.2 μm of InAs is required to achieve > 99% absorption. Achieving such a thick P-type region would require sacrificing the bandwidth and responsivity if the minority carrier diffusion length in

the P-type material is short. Therefore a careful trade-off must be made when designing an InAs APD to optimise all three parameters. The minority carrier diffusion length of epitaxially grown material can be in excess of 10 μm [13], however, damage from the implantation may create traps that act as recombination centres and could lower this value significantly. Therefore a 1 μm thick P-type region doped to a value of $1 \times 10^{18} \text{ cm}^{-3}$ will be used in this study which provides a good trade-off between responsivity and excess noise as $> 70 \%$ of 1550 nm photons will be absorbed in 1 μm of InAs. A minimum doping concentration of $1 \times 10^{18} \text{ cm}^{-3}$ will prevent significant depletion into the P-type region with applied bias and would enable a comparison against MBE grown P-type InAs to be made which is doped approximately to the same level. However, Be implantation into InGaAs has been frequently reported with activations efficiencies of 50 – 60 % [8, 14, 15] and therefore assuming a similar doping efficiency, a Be concentration of $2 \times 10^{18} \text{ cm}^{-3}$ was implanted. Simulations predicted that a flat doping profile to a depth of 0.75 μm , with the junction extending a total of 1 μm , could be realized from two Be⁺ implants with conditions of 200 keV at $1 \times 10^{14} \text{ cm}^{-2}$ and 70 keV at $3.8 \times 10^{13} \text{ cm}^{-2}$ which can be seen in Figure 4.1. The implantation was carried out at the University of Surrey Ion Beam Centre, 7 ° off the beam axis.

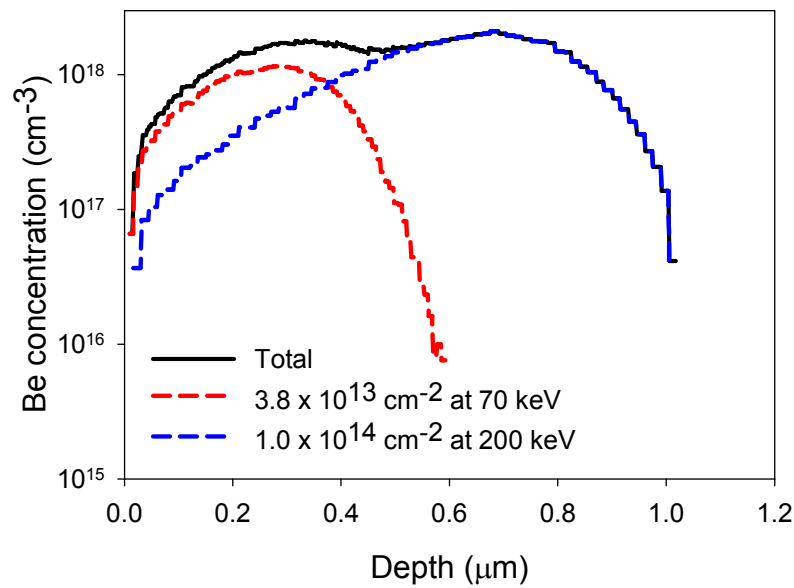


Figure 4.1: Be concentration resulting from two implants of $1 \times 10^{14} \text{ cm}^{-2}$ at 200 keV and $3.8 \times 10^{13} \text{ cm}^{-2}$ at 70 keV.

Samples were fabricated from InAs8 (see section 8.2 for epi wafer details) which was an InAs P-i-N wafer grown using MBE at 500 °C. The wafer consisted of a 1.5 μm thick Be doped P-type layer grown on a 4 μm intrinsic layer on a 2 μm Si doped N-type layer grown on an N+ (100) InAs substrate. Prior to implantation 2 μm was etched from the surface of

the wafer removing the existing P-type layer and the diffusion tail extending into the intrinsic region. Removal of 2 μm from the InAs surface was thought to be sufficient as previous SIMS characterisation of Be doping in InAs that has been grown by MBE has shown that the diffusion tail extends less than 200 nm. The two implants of $1 \times 10^{14} \text{ cm}^{-2}$ at 200 keV and $3.8 \times 10^{13} \text{ cm}^{-2}$ at 70 keV were scanned uniformly across the whole wafer which did not have an implant mask, referred to as a blanket implant. Samples were implanted at temperatures of 30, 100 and 200 $^{\circ}\text{C}$ to investigate the effects of dynamic annealing in InAs. After implantation, mesa diodes were fabricated using the procedure described in appendix 8.1.

4.4 Recovery of Be implanted mesa diodes through annealing

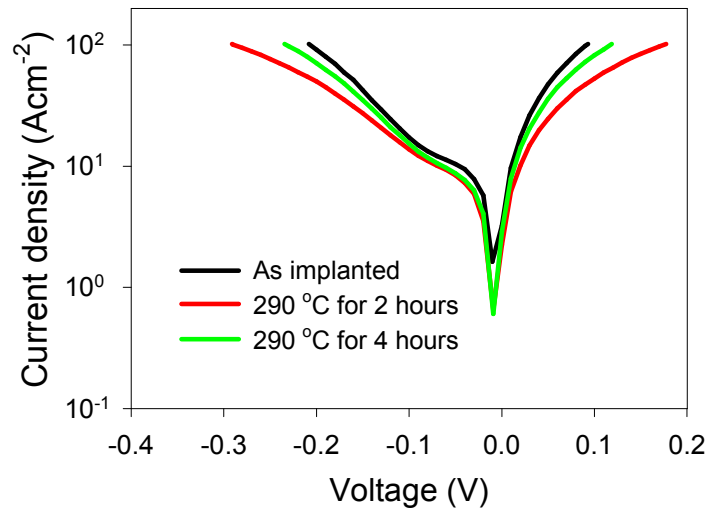


Figure 4.2: The J-V characteristics of mesa diodes after implantation. Also shown are the J-V characteristics of mesa diodes after an annealing at 290 $^{\circ}\text{C}$ for 2 and 4 hours.

The J-V characteristics of diodes implanted at room temperature and annealed in a furnace at a temperature of 290 $^{\circ}\text{C}$ for 2 and 4 hours are shown in Figure 4.2. The J-V characteristics of a diode implanted at room temperature and that with no annealing treatment is also shown. The slight difference in the J-V characteristics of the three diodes was caused by differences in the series resistance and no appreciable improvement to the J-V characteristic is observed upon annealing.

Annealing at higher temperatures is required for recovery and RTA was adopted to minimise Be diffusion during the high temperature anneals. The annealing cycle consisted of a linear ramp increasing from a temperature of 315 $^{\circ}\text{C}$ to the annealing temperature in 30 s. The annealing temperature was held for 30 s before being linearly ramped back down to 315 $^{\circ}\text{C}$

in 60 s. The annealing chamber was purged with nitrogen for the annealing cycle. Figure 4.3 shows the J–V characteristics of diodes implanted at room temperature and annealed at temperatures from 450 °C to 700 °C for 30 s. An unannealed diode is also shown for comparison. It is difficult to identify whether the slight rectifying behaviour observed from the 450 °C was due to Be activation, or if a Schottky junction at the metal semiconductor interface was the cause. However, the similarity between J-V characteristics of unannealed diode and the diode annealed at 450 °C suggests that Be activation, if any, was not significant at this temperature. Diodes annealed at 500 °C displayed a pronounced rectifying behaviour, however, the lowest dark current density between 0 and -1 V was measured in diodes that had been annealed at temperatures of 550 – 700 °C. Diodes annealed in this temperature range shared a similar dark current density of 1 Acm^{-2} between 0 and -1 V and a forward J-V characteristic that was limited by the series resistance of the semiconductor-metal interface.

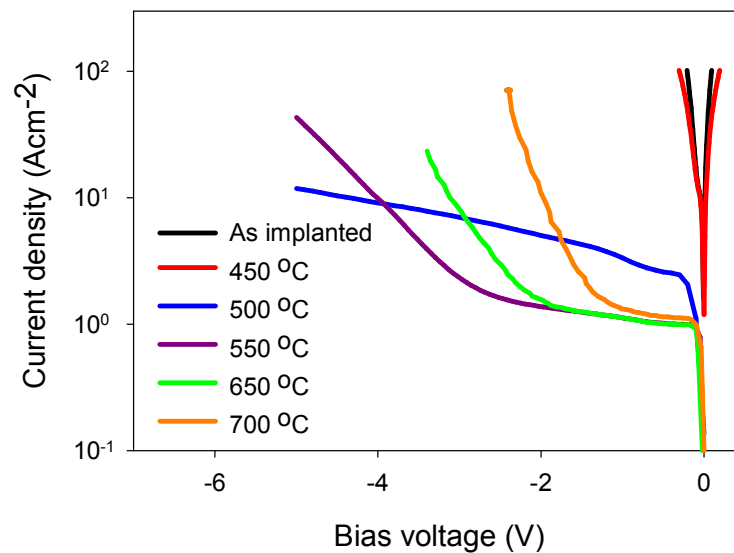


Figure 4.3: The J-V characteristics of diodes annealed at temperatures between 450 and 700 °C for 30 s. Also shown is the I-V characteristic of an unannealed diode.

Annealing at a temperature of 550 °C or above produced the lowest dark current in the diodes, however, at a reverse bias greater than -1 V, the gradient of the J-V characteristic is seen to suddenly increase. Furthermore, the reverse bias voltage at which the change in gradient occurs was observed to decrease with increasing annealing temperature. To investigate the origin of this additional leakage mechanism the I-V and C-V characteristics of samples annealed at 500 °C and 550 °C were measured at 77 K with the I-V characteristics plotted in Figure 4.5. The depletion width as a function of reverse bias voltage was extracted from the C-V characteristics and is shown in Figure 4.4. The depletion

width of the diodes are remarkably narrow considering the nominal intrinsic region thickness was estimated to be 2.5 μm after taking the 1 μm P-type region into consideration. The significantly narrower depletion width than expected suggests that the Be has diffused away from the surface of the wafer and into the sample. This corroborates with the observation that the sample annealed at 550 $^{\circ}\text{C}$ had a narrower depletion width than the sample annealed at 500 $^{\circ}\text{C}$. Assuming a one sided abrupt junction, the background doping of the intrinsic region was extracted from the C-V characteristics and found to be $8 \times 10^{15} \text{ cm}^{-3}$ at the junction and reaches a value of $1.1 \times 10^{16} \text{ cm}^{-3}$ extending 0.5 μm into the intrinsic region. A background doping of this magnitude is expected to induce a large electric field within the device and consequently a large tunnelling current could be generated.

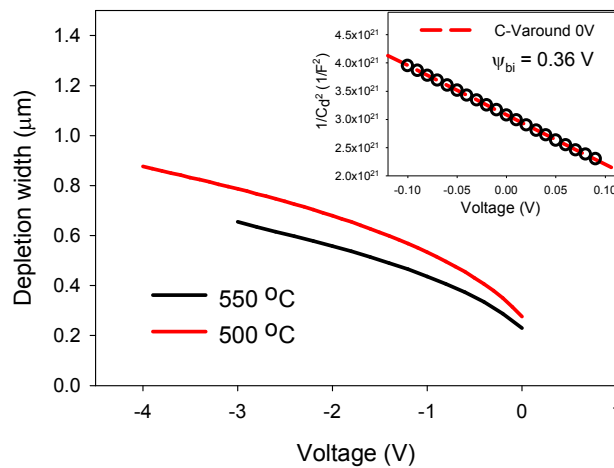


Figure 4.4: The depletion width as a function of voltage of mesa diodes annealed at 500 and 550 $^{\circ}\text{C}$ as determined from C-V measurements at 77 K. The insert shows the results of the C-V measurement used to calculate the built in potential of the diodes.

The theoretical J-V characteristics due to band to band tunnelling current (calculated using equation (3.7)) are plotted in Figure 4.4. An excellent fit could be achieved using a tunnelling parameter of 0.97 for both annealing temperatures. The acceptable range for the tunnelling parameter is considered to be 1.1 – 1.8 [16], however, avalanche gain was not accounted for in the model and consequently the tunnelling parameter will be required to increase to maintain an acceptable fit. Modelling of the tunnelling current agreed well with the measured data and confirmed the sharp increase in gradient of the I-V characteristics with increasing annealing temperature is an artefact of increased dopant diffusion rather than the evolution of extended defects. Figure 4.3 is an excellent example of the thermal budget constraints on an annealing cycle. An annealing temperature of 550 $^{\circ}\text{C}$ provides the maximum recovery while minimising Be diffusion to preserve the thickness of the intrinsic region. However a shorter annealing cycle may be required to suppress Be diffusion.

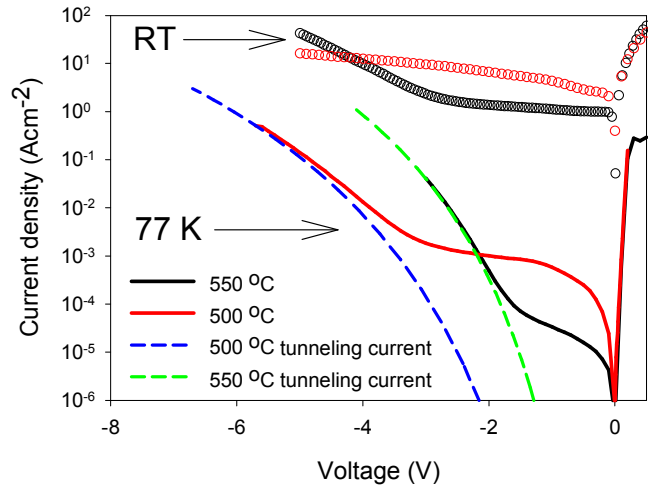


Figure 4.5: The room temperature and 77 K J-V characteristics of mesa diodes annealed at 500 and 550 °C. The modelled tunnelling current at 77 K is also shown.

4.5 Hot implants into InAs and post implant annealing

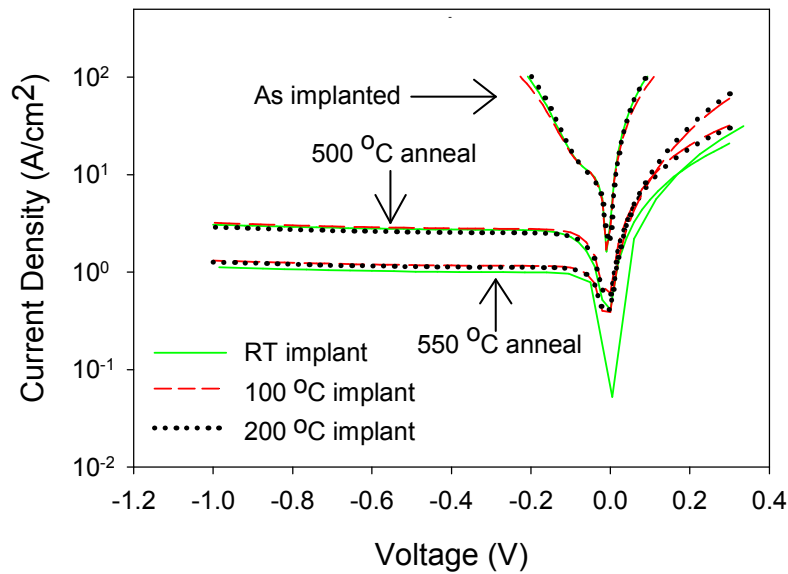


Figure 4.6: J–V characteristics of mesa InAs diodes which were implanted at RT, 100 °C, and 200 °C. In addition, the J–V characteristics of diodes annealed at 500 °C and 550 °C for 30 s from the three implant temperatures are also shown.

It has been reported that the implant temperature can have a pronounced effect on the resulting crystal quality within common III-V semiconductors [17], however, studies of dynamic annealing have not been carried out on InAs. Dynamic annealing may be useful in InAs as damage clusters are shown to form at the end of the projected range of Be ion when

simulated using TRIM as shown in section 2.8. However, it should be noted that TRIM simulations do not account for any dynamic annealing effects and therefore it is essentially simulating an implant at 0 K. To investigate the effects of dynamic annealing, implants were carried out on samples held at 30, 100 and 200 °C. The J-V characteristics of diodes implanted at 30, 100 and 200 °C are shown in Figure 4.6. In addition to this samples implanted at 30, 100 and 200 °C and annealed at 500 and 550 °C are also shown. The annealing temperature clearly segregates the J-V characteristics of the diodes into 3 distinct bands. Within each band the J-V characteristics of diodes from the hot implants closely resemble those implanted at 30 °C. Therefore the implant temperature are observed to have a negligible effect on Be implantation into InAs when studied through the observations of the diodes J-V characteristics. It is the post implant annealing that significantly affects the diodes performance due to recovery. Hot Be implants were not found to increase doping activation in GaAs and InP [10] indicating that the threshold temperature for dynamic annealing in these materials could be below room temperature. It is likely that the thermal energy at room temperature is sufficient to encourage the maximum amount of dynamic annealing in InAs.

4.6 MOVPE growth of InAs wafers with low background doping

InAs APDs require thick structures, $\approx 10 \mu\text{m}$, to achieve high gain and so MOVPE growth techniques would be preferable over MBE. However, low background doping and a low defect densities are also required with MOVPE growth techniques previously being reported to produce very high background doping due the parasitic incorporation of carbon [18]. A range of different InAs wafers were grown using MOVPE with a susceptor temperature of 590 °C. The best wafers were obtained using a slow initial growth rate of 3.8 \AA s^{-1} for 46 nm before the growth rate was increased to 7.6 \AA s^{-1} for the remainder of the structure. A slow initial growth rate was employed to planarize the substrate and help reduce the defect nucleation rate which can be exacerbated by the roughness of the polished substrate. The batch to batch variations in the quality of the InAs wafers from MOVPE were large even when using the same growth conditions. In the grower's opinion the two main causes for the large variation of the quality of InAs wafers were; there is a relatively small temperature range of $\approx 10 \text{ }^\circ\text{C}$ around 590 °C in which high quality InAs is grown, and the thermal contact between the wafer and susceptor is poor causing a large temperature uncertainty. Secondly, the batch to batch variations in the quality of the polished substrates were high as it was found during this project that the defect density of InAs wafers grown using the same growth conditions could be correlated with the manufacturers wafer batch numbers. Furthermore the InAs defects appear to trace faint polishing marks of the wafer.

InAs10, InAs11 and InAs13 were all from a ‘good batch’ of polished wafers and low defect densities and low background doping concentrations ($<5 \times 10^{14} \text{ cm}^{-3}$) were obtained, as discussed in section 5.3. The surface of the InAs appeared smooth with Nomarski microscope imaging of wafer InAs13 revealing a high density of minor defects that appeared as ripples on the wafer surface as shown in Figure 4.7. A few large area defects were also present that could be detected under visible light. Devices were occasionally fabricated over large area defects, as shown in Figure 4.8, and such devices were found to have a greater dark current compared to devices with no visible defects. This effect is discussed in section 4.7.

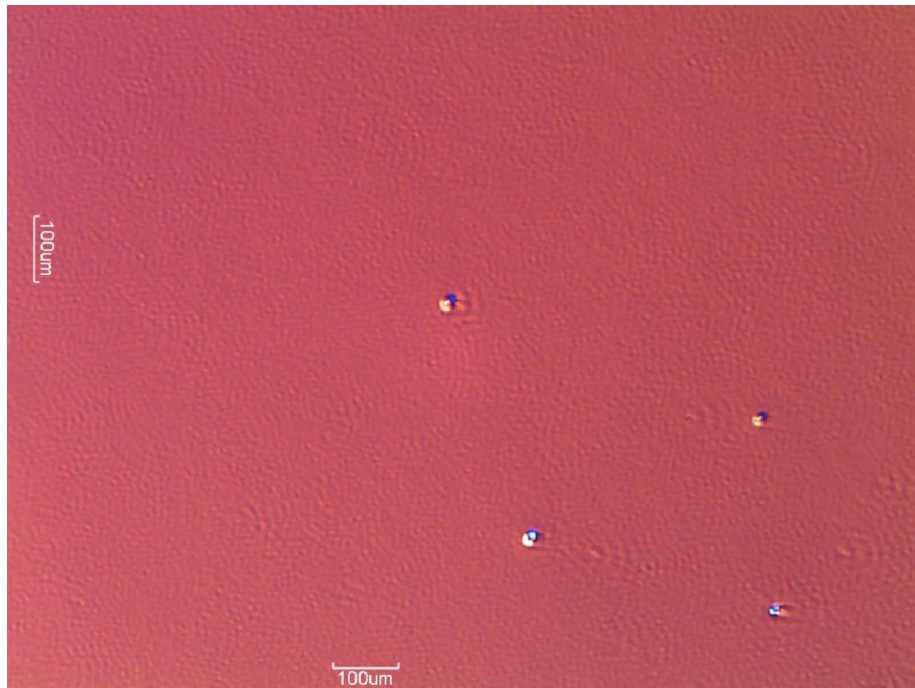


Figure 4.7: A Nomarski microscope image of InAs13

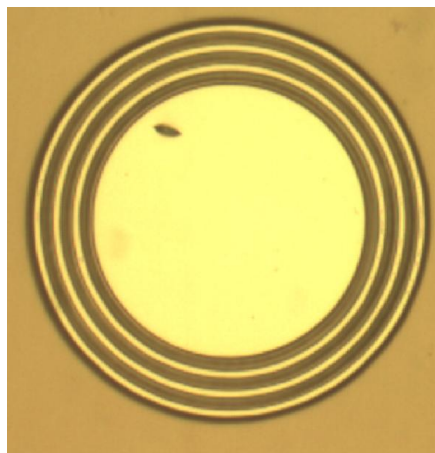


Figure 4.8: A photograph of an InAs APD with a large area defect

4.7 Fabrication of planar InAs APDs with low surface leakage

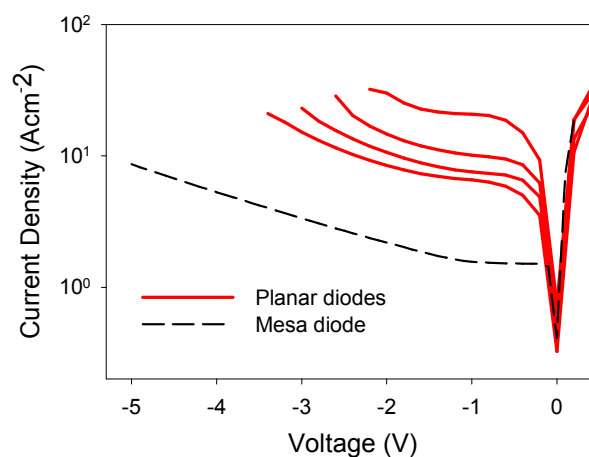


Figure 4.9: The J-V characteristics of planar InAs APDs. Also shown is the J-V characteristic of a mesa InAs APD fabricated using Be ion implantation for comparison.

A sample of InAs11 was cleaved from the wafer before receiving a three stage clean in N-butyle acetate, acetone and isopropyl alcohol. Ti/Au alignment marks were deposited onto the sample using photolithography and evaporation. A 5 μm thick mask of photoresist SPR220 was patterned to define the areas to be implanted. The sample was implanted with Be using conditions of $1 \times 10^{14} \text{ cm}^{-3}$ at 200 keV and $3.8 \times 10^{13} \text{ cm}^{-3}$ at 70keV at room temperature 7° off axis. After implantation the photoresist mask was removed in a positive photoresist remover EKC830 at 100°C . The EKC830 was removed using a three stage clean before the sample was annealed at 550°C for 30 s in a nitrogen rich atmosphere using proximity annealing between two un-doped InAs wafers. After annealing Ti/Au top and back contacts were deposited. The J-V characteristics of diodes fabricated using this method are shown in Figure 4.9 along with the J-V characteristic of a mesa diode annealed at 550°C and fabricated as described in section 4.4. The planar diodes showed a rectifying behaviour, however, the dark current density was significantly larger than measured in the mesa diode. Furthermore, the I-V characteristics of the planar diodes did not scale with either area or perimeter as shown in Figure 4.9. The poor uniformity observed in the planar I-V characteristic along with the high dark current is characteristic of high surface leakage. It is likely that the surface had been contaminated or damaged during fabrication processes. Early work fabricating planar InSb diodes using Be implantation found that 400 nm of material needed to be etched from the InSb surface as a final fabrication step to yield diodes with low surface leakage [19].

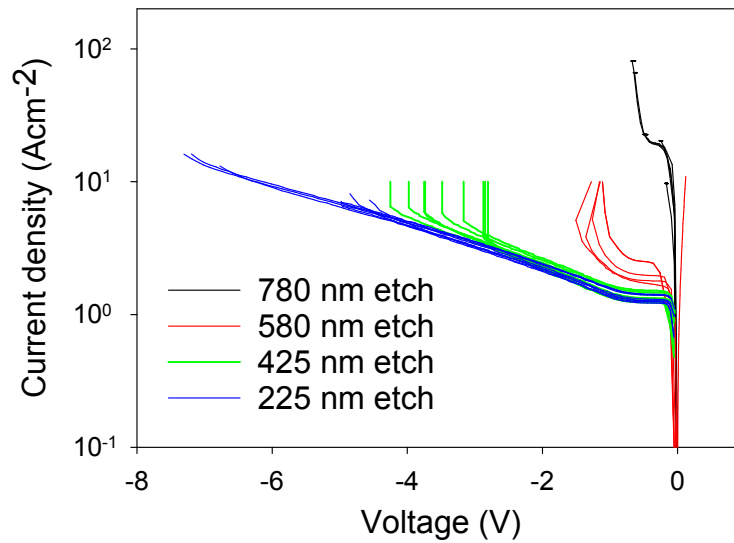


Figure 4.10: The J-V characteristics of planar InAs APDs with a surface etch to various depths.

To investigate if this technique is applicable, samples from InAs11 had 225, 425, 580 and 780 nm of material removed from the surface using wet chemical etching. The etching recipe used was $\text{H}_2\text{O}:\text{H}_2\text{O}_2:\text{HPO}_3$ in a ratio of 1:1:1 followed by a 10 s etch in $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ in a ratio of 1:8:80. Diodes with diameters ranging from 400 to 100 μm were measured from each of the samples with the J-V characteristics plotted in Figure 4.10. The J-V characteristics of the diodes etched 780 nm were extremely poor and hardly showed rectifying behaviour. A slight improvement was obtained from diodes etched to 580 nm although a premature breakdown was observed in all diodes before 2 V. Diodes from the 425 nm etch showed excellent scaling with area indicating low surface leakage and premature breakdown was observed before 4 V. Diodes that were etched to 225 nm showed bulk J-V characteristics agreeing with the J-V characteristic of the mesa APD. The success of the shallow etch indicates that the surface of the sample had been damaged or contaminated during fabrication and that the surface etch had restored good surface conditions. Etching 580 nm or more removed the majority of the highly doped junction leaving only the tail of the Be implant. Etching 580 nm is also seen to have a great effect on the dark current of the diodes and therefore indicates that the dark current is a strong function of junction depth or doping density. Furthermore, the junction depth also showed a strong relationship with the breakdown voltage. This is thought to be due to the electric field hotspots which are exacerbated in shallower junctions and will be discussed further in section 2.10. Although a surface etch can be utilised to fabricate InAs diodes with low surface leakage at room temperature, the fabrication procedure has retrogressed by relying

on wet chemical etching.

Planar Si, InGaAs/InP or HgCdTe APDs are fabricated using what can be termed a ‘self-passivation’ technique where the masking layer used to define the planar junction also forms the passivation layer of the APDs. The success of this method lies in that the mask and passivation layer can be deposited in a single step immediately after growth (often before being exposed to atmosphere) to perfectly preserve the surface from contamination, damage and in some cases oxide growth [2] [3]. In a crude self-passivation fabrication sequence, first a passivation layer such as Si or SiO₂ is deposited immediately after growth to minimise the contamination window. The passivation layer is then patterned and implanted or diffused forming the junction of the APD. The junction of the APD naturally terminates underneath the mask layer due to dopant diffusion and consequently the masking layer also forms a self-aligned passivation layer. Finally additional passivation or AR coating may be applied and contacts deposited. When fabricating III-V APDs SiN can be used as the passivation layer, however, SiN and SiO₂ are known to be poor passivation layers in InAs [1]. SU8 was found to be successful in passivating InAs [20], however, it is unsuitable for use in a self-passivation fabrication sequence as SU8 cannot withstand temperatures above 215 °C. Therefore to fabricate InAs APDs with low surface leakage a temporary surface passivation layer can be employed during fabrication before being removed as a SU8 passivation is applied. This method minimises the window that the InAs surface is un-passivated and vulnerable to contamination and damage.

A sample was cleaved from InAs11 and cleaned using a 3 stage clean. A 35 nm layer of SiO₂ was deposited onto the sample by plasma-enhanced chemical vapour deposition (PECVD) at 300 °C to protect the sample during further processing. The thin film also reduces channelling during ion implantation by scattering the trajectory of the Be ions before entering the InAs. The sample was patterned with 4 µm of photoresist SPR220 to expose circular regions with radii ranging from 7.5 to 200 µm. The wafer was implanted with Be at room temperature, 7° off axis using implant conditions of $1 \times 10^{14} \text{ cm}^{-3}$ at 200 keV and $3.8 \times 10^{13} \text{ cm}^{-3}$ at 70 keV to produce a 1 µm deep P⁺ region. After implantation the photoresist was removed and the sample was annealed at 550 °C for 30 s in a nitrogen rich atmosphere to recover the crystal. The SiO₂ film encapsulated the surface and prevented loss in surface stoichiometry due to As outgassing. The annealing caused significant Be diffusion away from the surface of the wafer and considerably increased the thickness of the P⁺ region. The SiO₂ layer was removed in a 10% hydrofluoric (HF) acid solution for 30 s. Following the buffered HF etch 250 nm of SiN was deposited at 300 °C by PECVD. A further buffered HF acid etch was used to define bond pads in the SiN layer as well as an anti-reflective (AR)

coating which maximised absorption at 2 μm . The remaining surface around the APD was passivated with 3.5 μm of SU-8. Ti/Au back and top contacts were deposited in addition to electrically isolated metal features overlapping the SU-8 at the junction perimeter to ensure a pure injection of photons when performing gain measurements. A photograph and a schematic diagram of an InAs planar APD fabricated using this method are shown in Figure 4.11.

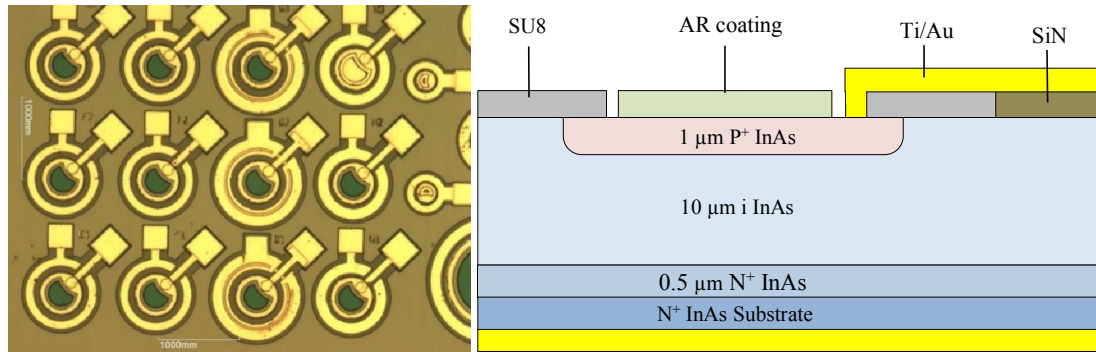
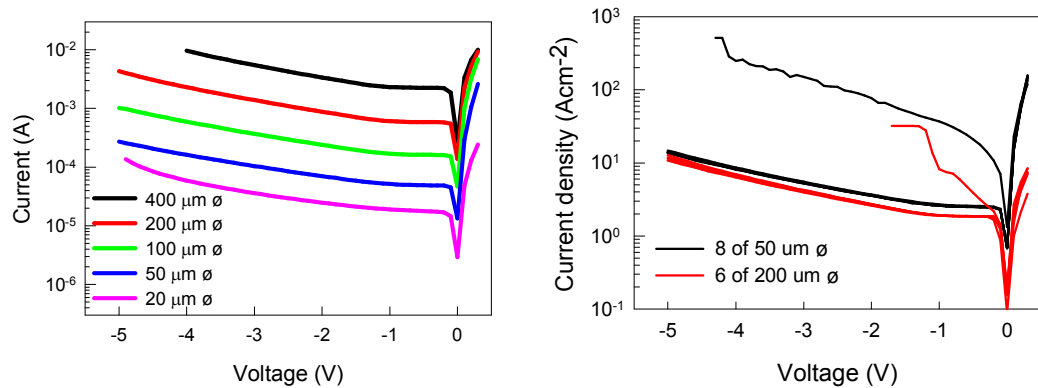


Figure 4.11: A micrograph of and a schematic diagram of a planar InAs APD

The I-V characteristics of planar APDs with diameters ranging from 400 to 20 μm are shown in Left, Figure 4.12. A surface etch was not required to produce planar APDs with excellent I-V characteristics confirming that the SiO_2 protective layer had preserved the surface quality of the InAs. Figure 4.13 shows the I-V characteristics of 6, 200 μm diameter planar APDs and 8, 50 μm diameter APDs from a single unit cell. One diode of each size displayed poor IV characteristics and inspection under a microscope revealed that both diodes had imperfections. It could not be determined if the imperfections were large crystal defects, as discussed in section 4.6, or if they were contaminants introduced during the fabrication process. Disregarding both of the damaged diodes, the average dark current of the 200 and 50 μm diameter planar APDs at -0.3 V was 582 and 49 μA with a standard deviation of 3 and 0.59 μA respectively. The sigma/mean corresponds to 0.52% and 1.21 % of the dark current of the 200 μm and 50 μm APDs respectively. The dark current variation of mesa InAs APD fabricated using the standard wet chemical etching recipe was found to be of 5% at -0.5 V across working pixels [21]. Furthermore, an array of SWIR (peak absorption at 1.5 μm) HgCdTe APDs developed by Raytheon is reported to have a non-uniformity of 8% operating at 300 K [22]. The dark current variation in APDs fabricated through the planar fabrication process is significantly lower than in both reports attesting to the highly uniform surface conditions achieved after growth and when not using wet chemical etching.

As the sample showed very high uniformity it is possible to separate the bulk and surface leakage components from the dark current for further analysis using equation (3.3). The bulk

leakage current is proportional to the diode's active area which in this case is taken to be the area implanted with Be. The surface leakage is proportional to the circumference of the active area.



Left, Figure 4.12: The J-V characteristics of planar APDs with diameters ranging from 400 to 20 μm diameter. Right, Figure 4.13: The J-V characteristics of 8, 50 μm diameter and 6, 200 μm diameter planar APDs.

Empirical fitting of equation (3.3) to the current measured in InAs APDs at -0.3 V was used to calculate the bulk and surface leakage current of APDs from wafer InAs11 at 296 K. This voltage was chosen as the largest dynamic resistance was observed around -0.4 V and avalanche gain is insignificant. An algorithm was used to search for the optimum values of the bulk and surface leakage which produced values of 1.3 Acm^{-2} and $4 \times 10^{-4} \text{ Acm}^{-1}$ respectively. The measured dark current and a fit of the bulk and surface leakage currents are shown in Figure 4.14. The analysis was carried out on APDs with diameters ranging from 400 to 50 μm . Diodes with diameters of 20 and 15 μm were also fabricated, however, a good fit could not be achieved when including them in the analysis. Be has been shown to diffuse rapidly during annealing in InAs and could significantly increase the active area of the small APDs. By fitting the radius of the small APDs against the fitted total dark current, the lateral diffusion was estimated to be $\sim 2.5 \mu\text{m}$.

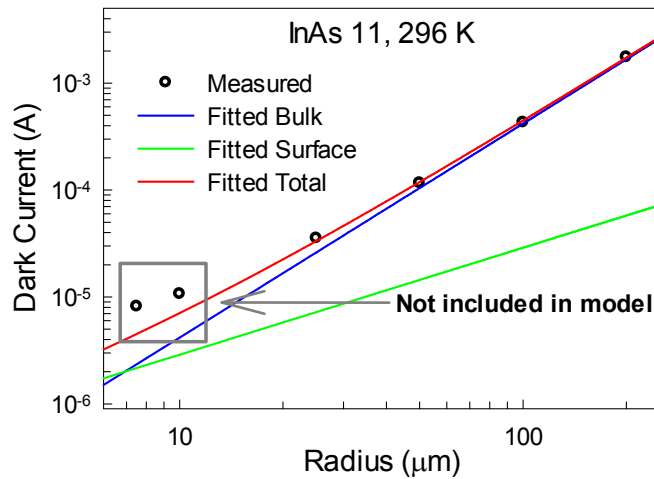


Figure 4.14: The measured dark current of planar InAs APDs of various radii at -0.3 V from wafer InAs11. The bulk and surface leakage currents calculated using empirical fitting are also shown.

The dark current density of the planar APDs from InAs11 was 1.3 Acm^{-2} at room temperature which is approximately one order of magnitude larger than the dark current density of an epitaxially grown mesa APD [23]. The intrinsic and N-type region of the planar APD were epitaxially grown and the current generated from these regions is expected to be very similar across the mesa and planar APDs. The higher dark current is therefore thought to originate in the P-type region of the APD and is verified by a study of the activation energy which is carried out in the next chapter.

The surface leakage current of mesa InAs APDs was found to be $2 \times 10^{-4} \text{ Acm}^{-1}$ at room temperature [23]. This is very similar to the value found for planar APDs in this study at $4 \times 10^{-4} \text{ Acm}^{-1}$. The similarity between surface leakage currents in planar and mesa InAs APDs may suggest that both leakage mechanisms have a similar origin. However, mesa InAs APDs have also been reported with negligible surface leakage currents [24]. The etching procedure was identical to [23], however, the surface was immediately passivated with SU-8 after etching. The success of the immediate passivation could be to prevent the formation of the highly conductive indium oxide layer re-forming after etching. InAs APDs may greatly benefit from the development of a self-passivation fabrication sequence to completely eliminate the surface leakage in InAs APDs by preventing the formation of the oxide layer. However, at present suitable passivation layer that could also act as a mask is not available.

4.8 Lateral diffusion of Be implanted APDs

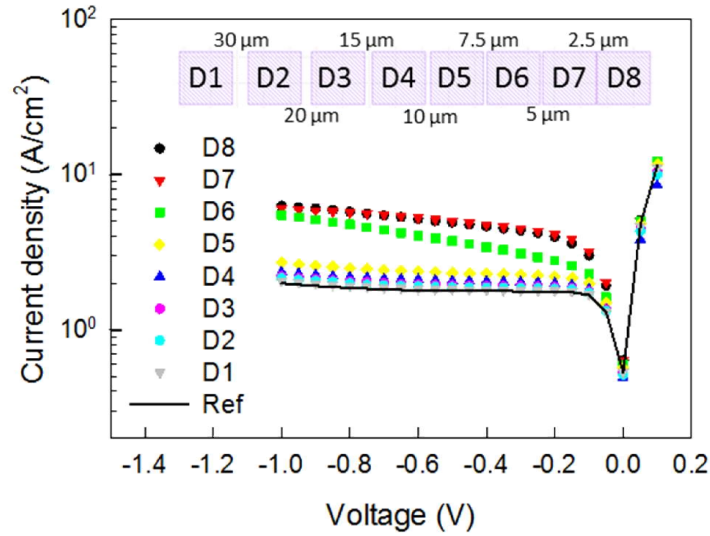


Figure 4.15: Schematic diagram of a linear array of 100 μm square planar InAs diodes fabricated with the various separation distances (insert). The J–V characteristics of the diodes from the linear array are shown in addition to the J–V characteristics of an isolated reference planar diode.

The Be implantation and annealing techniques could be used to fabricate an array of InAs photodiodes for imaging applications. It is therefore useful to consider the performance of the diodes when in an array geometry. A linear array of 100 μm square diodes was fabricated with various separation distances between neighbouring diodes. The J-V characteristic of each diode in the linear array is plotted in Figure 4.15 along with the J-V characteristic from a reference 100 μm diameter planar diode. The reference diode was located over 120 μm away from any other diode and can be considered as decoupled from any other device. A schematic diagram of the linear array is shown in the insert of Figure 4.15. Diodes D6, D7 and D8 have higher dark currents than the reference diode indicating incomplete isolation when the gap between diodes is less than 5 μm . For diode separation above 7.5 μm , the dark currents from D5 to D1 were found to asymptotically approach the dark current of the reference diode. The zero bias dark current of diodes D5 to D1 are within $\pm 6\%$ of the reference diode. Further optimization of implantation and annealing conditions, use of additional implantation to increase the resistivity of InAs or use of isolation trenches will be required to reduce the separation distance. However, annealing times less than 30 s could not be explored in the timeline of this work as the immediately available RTA unit is thought to be non-uniform when annealing for durations less than 30 s.

4.9 Redistribution of Be in InAs upon annealing

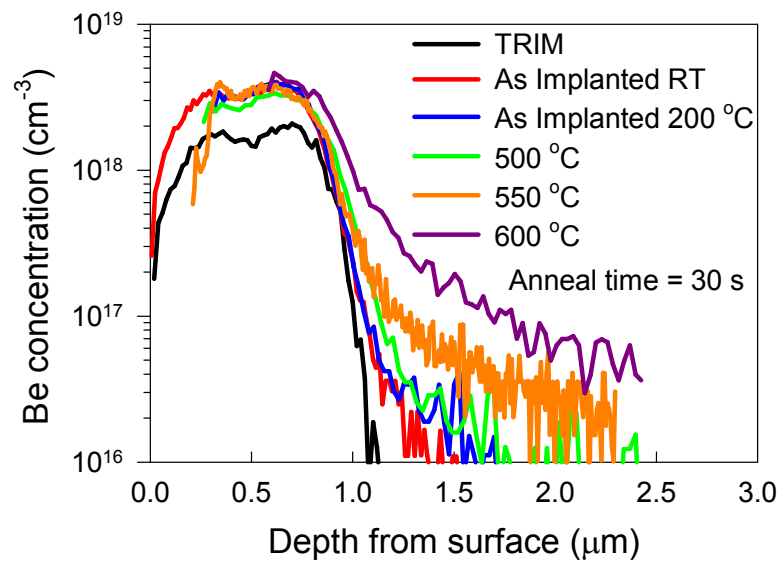


Figure 4.16: The concentration of Be implanted into InAs as simulated using TRIM. The Be concentration profiles as measured by SIMS are also shown for samples; as implanted at room temperature; as implanted at 200 °C; implanted at room temperature and annealed at 500, 550 and 600 °C.

Figure 4.16 presents Be profiles before and after post implant annealing as measured by SIMS. The Be profile generated using TRIM is included for comparison. The SIMS measurements were carried out on mesa samples which were fabricated using the procedure detailed in section 4.7. The finishing etch removed approximately 150 nm from the surface and the exact etch depth of each sample was measured using a Dektak and corrected for when plotted in Figure 4.16. The discrepancies seen in the absolute value of the Be concentration between the TRIM and SIMS studies are likely to be caused by a calibration error of the SIMS measurement. The Be profile of unannealed diodes is in good agreement with TRIM simulations with the results summarized in Table 4.1. Previous work reported errors of up to 24 % when simulating the straggle of Be implanted into InAs [11], however, this work found simulations to be very accurate. Discrepancies between the studies may be due to increased ion interactions with defects in higher doses, or perhaps some channelling was achieved. The substrate temperature during implantation was not found to alter the Be profile as the unannealed samples implanted at room 30 and 200 °C showed very similar Be distributions down approximately $3 \times 10^{16} \text{ cm}^{-3}$. Annealing at a temperature of 500 °C caused Be diffusion into the bulk of the sample. The Be profile of the tail of the samples annealed at 500 and 550 °C have been modelled by a Gaussian distribution with the results

summarized in Table 4.1. The redistribution of Be resulting from a 600 °C anneal for 30 s was much more severe, resulting in a severely distorted profile that could not be modelled by a Gaussian distribution. The peak Be concentration in the sample annealed at 600 °C for 30 s was found to be slightly larger than in the unannealed samples. This could simply be due to a SIMS measurement error, however, Mg implantation into InAs was found to cluster around extended defects upon annealing and caused large spikes in the SIMS measurements [5]. It is possible that the Be is behaving in a similar manner to Mg during high temperature annealing.

TABLE 4.1
SUMMARIZED RESULTS ANALYZING THE TAIL OF BE DISTRIBUTION FROM TRIM AND SIMS MEASUREMENTS.

Sample	Projected Range (nm)	Straggle (nm)	Peak Concentration (cm ⁻³)
TRIM	700	130	2.0×10^{18}
<i>SIMS (Unannealed, implanted at RT and 200 °C)</i>	645	147	4.0×10^{18}
<i>SIMS (Implanted at RT, annealed at 500 °C for 30 s)</i>	-	175	3.4×10^{18}
<i>SIMS (Implanted at RT, annealed at 550 °C for 30 s)</i>	-	190	3.9×10^{18}

4.10 Optimisation of Be implantation conditions

The planar APDs were measured to have a larger bulk dominated dark current compared to epitaxially grown mesa APDs. The increased dark current was suspected to be generated from the Be implanted region, as confirmed by gain measurements in section 5.4. The saturation current due to diffusion from the P-type region is given by equation (4.1).

$$J_P = \frac{qD_n n_i^2}{L_n N_a} \quad (4.1)$$

The high dark current is therefore due to a short minority carrier diffusion length or low acceptor concentration. Both parameters are closely related to the Be implant and recovery as remnant implant damage reduces the minority carrier diffusion length. The implant damage may be in the form of primary implant damage such as point defects, secondary defects that form as a result of the coalesces of primary implant damage upon annealing or Be interstitials due to incomplete Be activation. A low acceptor concentration could be due to low Be activation, or counter doping caused by the implant damage. However, it has also been hypothesised that the dark current of an InAs APD is dominated by thermionic emission at the P-type surface [25] and therefore a highly doped surface layer or a wide bandgap blocking layer can reduce the dark current of the APD [26]. Four new sets of implantation conditions were designed to probe these theories which will be used in comparative study against the original doping profile used to optimise the annealing.

4.10.1 Fabrication

Samples from InAs13 were fabricated into planar diodes using the fabrication procedure described in section 4.7. Five different doping profiles were achieved using Be implantation. Three identical doping profiles of varying doping concentrations were used to investigate the relationship between the implant dose and the electrical and optical properties. Another two doping profiles were designed with the intention to improve the responsivity and reduce the dark current of the Be implanted APDs.

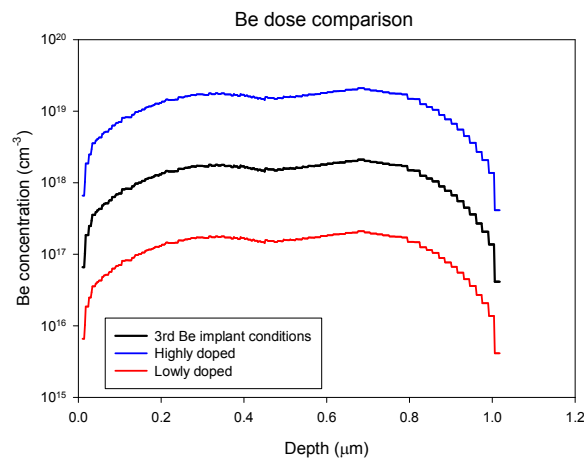


Figure 4.17: The p-type doping profiles of InAs APDs from two implants at energies of 70 and 200 keV using 3 different dose magnitudes simulated using TRIM.

The implant conditions used were $3.8 \times 10^{13} \text{ cm}^{-2}$ at 70 keV and $1 \times 10^{14} \text{ cm}^{-2}$ at 200 keV creating the doping profile shown in Figure 4.17. Two additional implants were carried out with the dose 1 order of magnitude higher and lower than this dose as shown in Figure 4.17. These structures were used to investigate how the dose of Be affects the performance of the

Be implanted diodes. A linearly graded doping profile was fabricated using 5 implants as shown in Figure 4.18. The linearly graded P-type doping created a low electric field across the P-type layer enhancing carrier extraction. The implantation conditions were $1.1 \times 10^{13} \text{ cm}^{-2}$ at 10 keV, $1.3 \times 10^{13} \text{ cm}^{-2}$ at 30 keV, $8 \times 10^{12} \text{ cm}^{-2}$ at 50 keV, $2.3 \times 10^{12} \text{ cm}^{-2}$ at 100 keV and $3 \times 10^{11} \text{ cm}^{-2}$ at 200 keV. A step graded doping profile was created using 4 implants consisting of a heavily doped surface region and lightly doped buried region. The heavily doped surface prevented punch through of the electric field to the contact and also acted as a barrier to thermionic emission. The lightly doped buried P-layer is expected to have lower implant damage and therefore the minority carrier diffusion length is expected to be high. Additionally a triangular electric field will be created as the diode is reverse biased to prevent hotspots from forming. The implant conditions used were $2 \times 10^{13} \text{ cm}^{-2}$ at 10 keV, $1.8 \times 10^{11} \text{ cm}^{-2}$ at 50 keV, $1.9 \times 10^{11} \text{ cm}^{-2}$ at 100 keV and $3.5 \times 10^{11} \text{ cm}^{-2}$ at 200 keV as shown in Figure 4.19. All implants were carried out 7° off axis at room temperature.

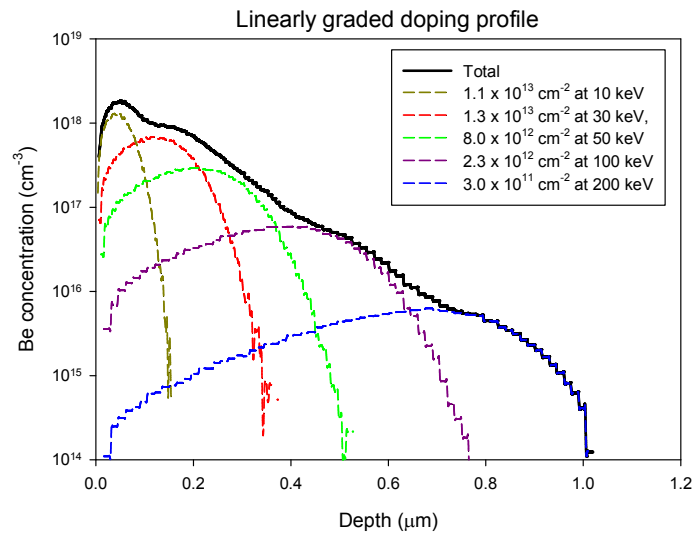


Figure 4.18: A linearly graded p-type doping profile of an InAs APD created using 5 implants simulated using TRIM.

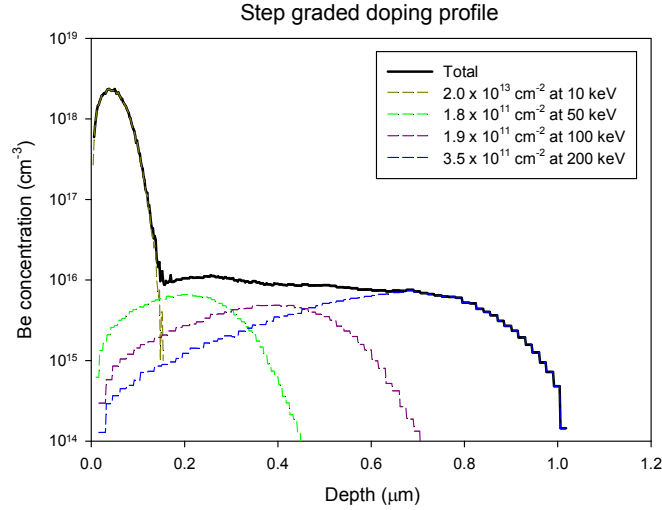


Figure 4.19: A step p-type doping profile of an InAs APD created using 4 implants simulated using TRIM.

4.10.2 Characterisation

The photocurrent due to the diffusion of electrons from the P-type region in a pin diode is given in equation 4.2 where the where G_0 is the generation rate and x is the distance the carriers must diffuse before being collected by an electric field. Greater than 70 % of 1550 nm photons will be absorbed within 1 μm of InAs as shown in Figure 3.5 and so responsivity measurements will give a strong indication of the relative minority diffusion length within each sample.

$$I_{ph} = \frac{qG_0}{\cosh\left(\frac{L_n}{x}\right)} \quad (4.2)$$

The responsivity of the sample with a doping density to $2 \times 10^{19} \text{ cm}^{-3}$ was found to be less than the sample doped to $2 \times 10^{18} \text{ cm}^{-3}$ with responsivity values of 0.24 and 0.45 A/W respectively. This result indicates that the minority carrier diffusion length in the P-type region is significantly reduced as the dose of the implant is increased, however, we are not able to identify whether this is simply due to higher SRH recombination due to a higher number of traps from damage sites, or because the capture rate of the electron has increased due to the increased donor concentration. The responsivity of the remaining 3 samples could not be measured due to the dark current being too high as shown in Figure 4.20.

By comparing the dark current of diodes with a flat doping profile a clear inverse relationship between the implant dose and the dark current is observed. The minority carrier

diffusion length has been identified to be the shorter in the sample showing the lower dark current. This relationship is the inverse of what was expected and suggests that the minority carrier diffusion length is not the dominating factor in determining that dark current from the P-type region. A positive dependence between the doping density and the dark current was observed indicating that the doping density within the P-type region is a strong factor in determining the dark current of the planar APDs. The poor J-V characteristics of the linearly graded and step graded diodes are therefore likely to be poor due to the doping density across the majority of the P-type region being low. Furthermore, in section 4.7 that the dark current of the diodes increased rapidly as the junction depth and doping concentration was reduced using etching which also corroborates with this conclusion.

The dark current of an epitaxially grown mesa diodes with a P-type doping density of $1 \times 10^{18} \text{ cm}^{-3}$ was lower than the planar diode with a Be concentration of $1 \times 10^{19} \text{ cm}^{-3}$. Therefore it is not only the doping density within the P-type region that requires consideration. Further analysis of the mechanism that determines the dark current in planar InAs APDs is required so that optimisation of the APD structure can be carried out.

The detectivity of the samples doped to 2×10^{18} and $2 \times 10^{19} \text{ cm}^{-3}$ were calculated at room temperature at -0.3 V under 1550 nm excitation and found to be 6.08×10^8 and $4.64 \times 10^8 \text{ cmHz}^{-1/2}\text{W}^{-1}$ respectively. The sample doped to $2 \times 10^{18} \text{ cm}^{-3}$ showed the highest detectivity and this doping profile will be analysed further in subsequent chapters.

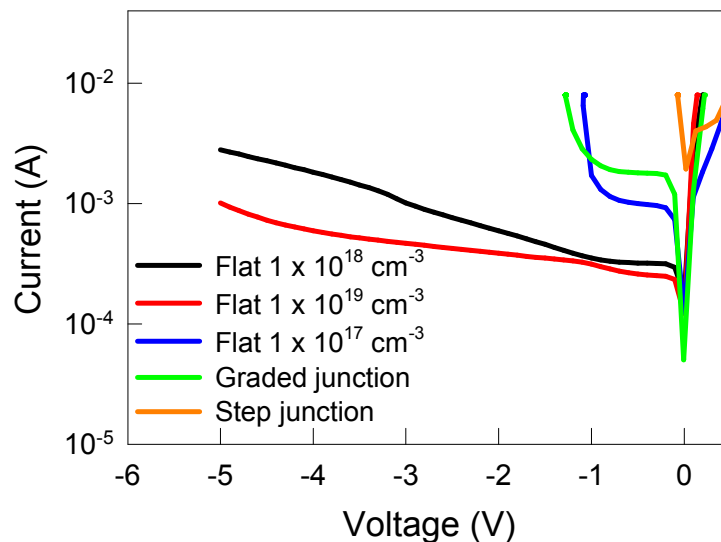


Figure 4.20: Comparison of the I-V characteristics of the 5 different implant conditions.

4.11 Comparison of the detectivity of Be implanted diodes

The J-V characteristics of a 200 μm diameter planar APD is shown in Figure 4.21 along with, a Zn diffused planar diode from Iwamura et al [27], a commercial photodiode from Judson and a mesa diode grown by MOVPE from Kerr et al [23]. All diodes apart from the Judson diode are reported to have low surface leakage and therefore the J-V characteristics are representative of the bulk current. As discussed in section 4.7, the higher dark current from the Be implanted diodes compared to the mesa is caused by the Be implantation and is investigated further in the next chapter. The Zn diffused sample showed a lower dark current than the Be implanted diodes, however, the concentration in the P-type layer was very high at $3 \times 10^{19} \text{ cm}^{-3}$ and the junction was only 0.2 μm thick and formed in the substrate rather than in epitaxially grown material. Consequently any comparison to identify the additional leakage mechanism is unfair.

The responsivity of the optimised Be implanted planar diode was found to be 0.45 A/W at 1550 nm producing a peak detectivity of $6.08 \times 10^8 \text{ cmHz}^{-1/2}\text{W}^{-1}$ at -0.3 V. The mesa diode had a responsivity of 0.6 A/W at 1550 nm and a detectivity of $2 \times 10^9 \text{ cmHz}^{-1/2}\text{W}^{-1}$ which is larger than the Be implanted APDs and attests to the quality of the epitaxially grown P-type layer. Measurements of the responsivity of the Zn diffused sample were not reported at 1550 nm, however, at 2.5 μm the responsivity was reported to be between 0.15 – 0.1 A/W [27]. This figure is low and may be explained by the narrow width of the device.

The Be implantation is thought to cause the large dark current in the Be implanted APDs. This will be explored further in the next chapter, however, optimisation of the Be implant conditions to increase the responsivity and lower the dark current could significantly improve the detectivity of the Be implanted APDs.

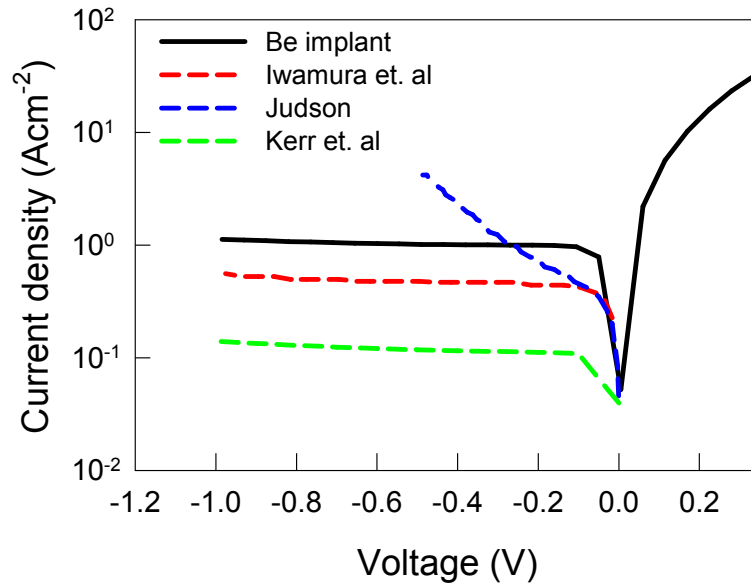


Figure 4.21: A comparison of the J-V characteristics of a Be implanted diode against Zn diffused diode from Iwamura et. al [27] a commercial device from Judson and a MOVPE grown diode from Kerr at. al [23].

4.12 Conclusion

Be implantation has been demonstrated as an effective method for selective area P-type doping InAs. The implant process appears to be destructive, typically resulting in poor electrical characteristics of unannealed material, however, good recovery can be achieved using RTA. Annealing at a temperature of 550 °C for 30 s provided the optimum conditions in terms of producing the lowest dark current in mesa diodes and preserving the as-implanted Be profile. Higher annealing temperatures did not produce better crystal quality and only caused further Be diffusion. Implants carried out at room temperature were found to be just as effective as hot implants.

A fabrication procedure was developed for producing highly uniform planar InAs APDs. Planar APDs showed low surface leakage current and were dominated by leakage through the bulk of the APD at room temperature. The dark current of the APDs were 1 Acm⁻² which is approximately one order of magnitude larger than a typical epitaxially grown mesa APD. Various implantation conditions were explored to optimise the detectivity of the planar InAs APDs. A detectivity of 6.08×10^8 cmHz^{-1/2}W⁻¹ at 1550 nm at room temperature was achieved using implant conditions to produce a P-type region 1 μm deep with a Be concentration of 2×10^{18} cm⁻³.

4.13 References

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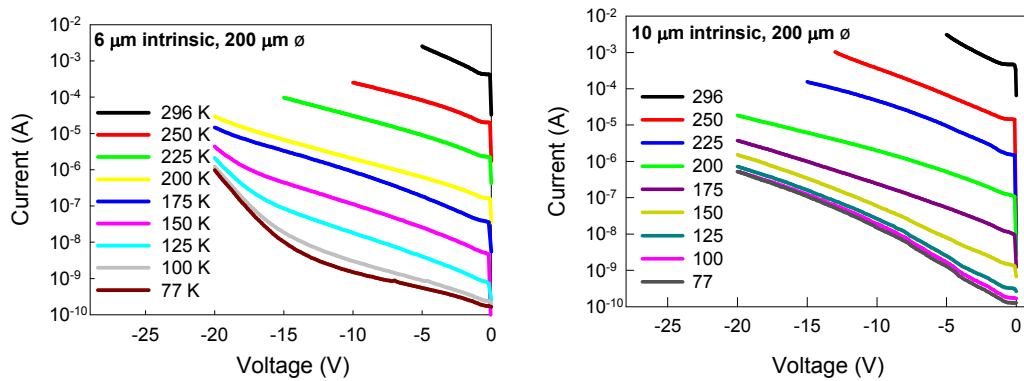
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5 Characterisation of High gain planar InAs APDs

5.1 Introduction

In this chapter planar APDs fabricated using Be ion implantation conditions are characterised. The temperature dependence of the dark current is investigated and fitted to Arrhenius equations to find the activation energy which is subsequently used to identify the origin of the dominant leakage mechanism. C-V measurements and fitting techniques are used to find the avalanche region width and background doping concentration. The gain at 200 K is measured to be larger than any other InAs APD, however, the APDs were found to breakdown prematurely at ≈ 26 V. Planar APD with guard rings were designed and fabrication and characterisation is also presented. The work from this chapter is published in [1].

5.2 Temperature dependence of the dark current



Left, Figure 5.1: The I-V characteristics of a 200 μm diameter APD from the 6 μm thick structure. Right, Figure 5.2: The I-V characteristics of a 200 μm diameter APD from the 10 μm thick structure.

Planar InAs APDs were fabricated from wafer InAs10 and InAs11 using the fabrication sequence described in section 4.7. Wafer InAs10 was grown with a thick intrinsic region of 10 μm and intended for high gain measurements while InAs11 was grown with a 6 μm thick intrinsic region and used in more general studies of planar InAs APDs. The planar APDs were passivated with 3.3 μm of SU-8 and had 250 nm thick SiN bond pads. A 250 nm thick single layer of AR coating was also used to optimise absorption at 2 μm.

The I-V characteristics of APDs from wafer InAs10 and InAs11 were measured at temperatures from 296 K and 77 with the I-V characteristics of a 200 μm diameter APD from both wafers plotted in Figure 5.1 and Figure 5.2 respectively. Wafer InAs10 displayed slightly lower dark current than InAs11 at low temperatures, however, this is thought to be due to InAs10 being in better thermal contact with the cold chuck. An identical method to that used in section 3.1 was used to calculate the bulk and surface leakage currents of the APDs at temperatures of 296, 250, 225 and 200 K for both wafers with the results plotted against the inverse of temperature in Figure 5.3. The activation energy, E_a , of the bulk and surface leakage currents was calculated by fitting the respective currents to Equation (5.1) yielding values of 0.45 eV and 0.25 eV respectively for the InAs10, and 0.42 eV and 0.24 eV for InAs11

$$I_d = T^2 \exp(-E_a / kT) \quad (5.1)$$

The activation energy of the bulk leakage mechanism is approximately equal to the bandgap of InAs and is therefore interpreted as a diffusion current from either of the highly doped layers. The discrepancy between the activation energy and the bandgap of InAs could be due to slight errors in determining the APD temperature or, the pre-exponential term of equation 1 having a larger temperature dependence than assumed. However, the bulk leakage activation energy measured here is similar to values reported for mesa InAs APDs which are also reported to have a diffusion limited bulk current at room temperature to 200 K [2, 3]. The surface leakage activation energy is closer to a value of half the bandgap indicating contribution from a generation-recombination process. The activation energy of the surface leakage in the planar APDS is also similar to that measured in mesa APDs. Surface leakage became the dominant leakage mechanism in APDs with a diameter of 200 μm at 200 K. The dominance of the surface leakage below 200 K caused significant errors when determining the true value of the bulk leakage current and so the analysis was stopped at 200 K. Additionally, the background (300 K thermal radiation) induced photocurrent became significant at 150 K further complicating the analysis at lower temperatures.

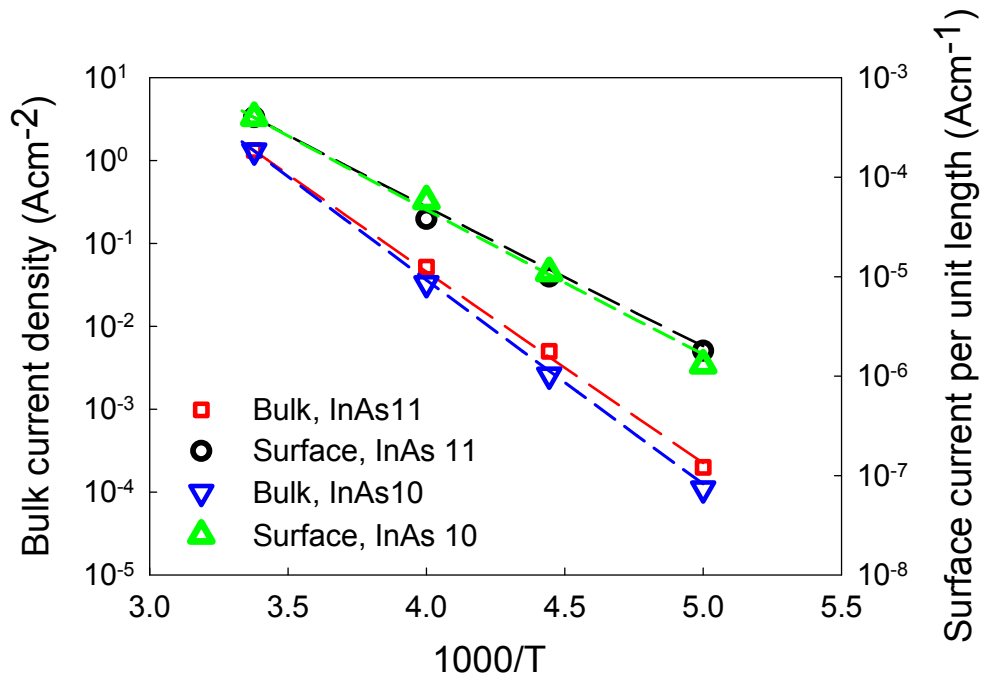


Figure 5.3: An Arrhenius plot of the bulk and surface leakage currents of APDs from wafer InAs10 and InAs11.

Although both planar APDs show a dark current dominated by a diffusion process, the dark current density of the planar APDs from both InAs10 and InAs11 was 1.3 Acm^{-2} at room temperature which is approximately one order of magnitude larger than the dark current density of an epitaxially grown mesa APD [4]. The intrinsic and N-type region of the planar APD were epitaxially grown and the current generated from these regions is expected to be very similar across the mesa and planar APDs. The increased diffusion current is therefore expected to be generated from the P-type region of the APD which can be verified by gain measurements as discussed in section 5.4. The large diffusion current measured in the planar APDs is therefore likely related to the implantation leading to the hypothesis that incomplete recovery of the crystal through annealing could reduce the minority carrier diffusion length, or that the activation of the Be is poor. Furthermore, the implantation profile shows low doping at the P-type surface layer of InAs and could cause a large thermionic emission at the P-type surface creating a large dark current. However, the activation energy of bulk leakage mechanism was found to be larger in the planar APDs compared to mesa APDs. Consequently the dark current of the planar APDs was found to reduce rapidly and converged with the dark current of mesa APDs at 200 K producing a dark current density of $400 \mu\text{Acm}^{-2}$. InAs APDs are likely to be operated at 200 K to reduce the dark current to an acceptable level. At this temperature the dark current is competitive with epitaxially grown mesa APDs.

In mesa APDs the bulk current is reported to swap between being dominated by diffusion current to a generation and recombination current in the range from 175 – 200 K. Although the bulk and surface leakage current of the planar APDs could not be determined at temperatures below 200 K the total dark current closely agrees with the the total dark current measured in mesa APDs and may indicate that the same mechanisms is present in planar APDs.

The surface leakage in the planar APDs was well controlled, however, it was not eliminated and still proved significant at low temperature or in APDs with a small diameter. In section 4.7 the surface leakage in planar APDs at room temperature was found to be very similar to that obtained from an optimised mesa APD and it was suggested that both could be due to the formation of a highly conductive indium oxide surface layer. The observation that the activation energy of the surface leakage is similar for both device topologies provides further evidence to support this theory.

5.3 Depletion width and background doping of high gain planar InAs APDs

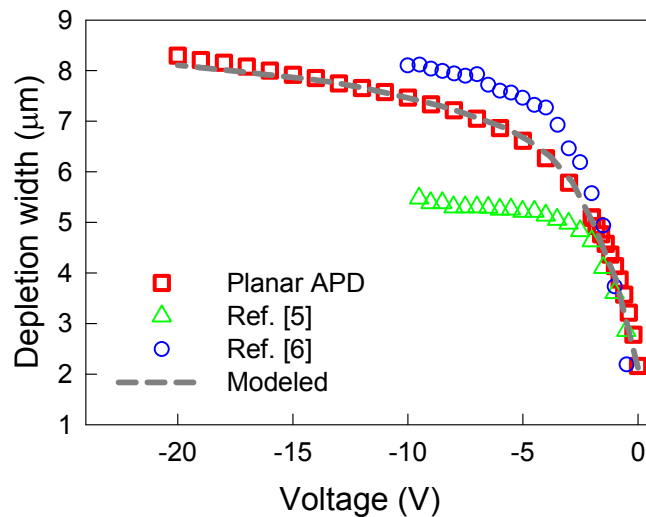


Figure 5.4: The measured depletion width vs reverse bias voltage characteristics of planar InAs APDs as deduced from capacitance-voltage measurements taken at 77 K in comparison with data from [5] and [6]. The simulated depletion width vs reverse bias voltage characteristics of the APD structure are also shown.

Thick avalanche regions with low background doping are required to achieve high gain in InAs APDs. Typically the depletion width of InAs APDs has been limited to 6 μm [5], however, recently a depletion width of 8 μm has been demonstrated [6]. Wafer InAs10 was

grown with a thick intrinsic region to increase the depletion width and achieve high gain from the APD. Figure 5.4 shows the depletion width versus reverse bias voltage characteristics of the planar APD as determined from Capacitance-Voltage (C-V) measurements at 77 K from InAs10. Equation (5.2) was used to calculate the depletion width as a function of reverse bias voltage of the planar APDs where ϵ is the permittivity, r is the radius of the APD and t_i is the intrinsic region thickness. The t_i term is included to account for the lateral depletion which can significantly increase the capacitance of small area APDs.

$$W_d(V) = \frac{\epsilon_0 \epsilon_r}{C_d(V)} \text{ where } C_d = C / (\pi r^2 + 2\pi r t_i(V)) \quad (5.2)$$

The depletion width of the APD approached 8 μm at -20 V which is similar to the maximum depletion width reported for a mesa InAs APD.

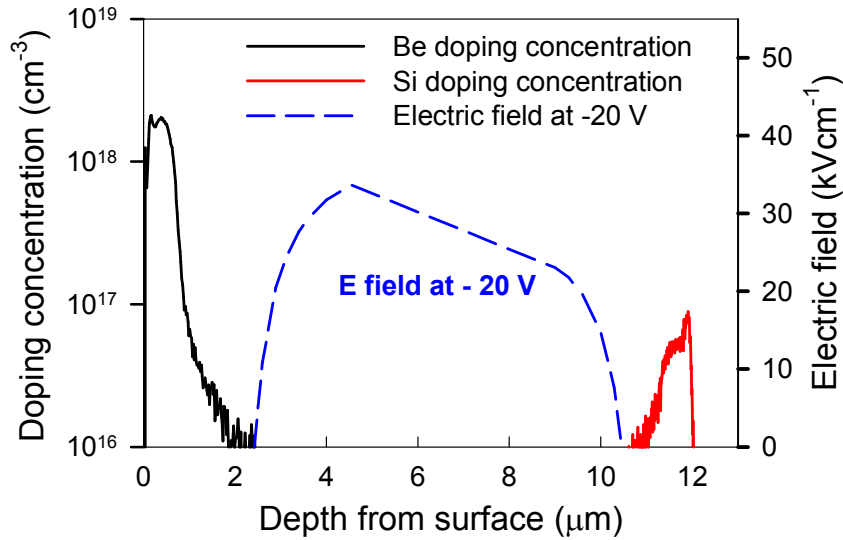


Figure 5.5: SIMS measurements of the Be and Si doping concentrations as a function of distance from the wafer surface. The electric field developed across the avalanche region of the APD at – 20 V is also shown.

To complement the C-V profiling analysis, Be and Si doping concentrations were measured using secondary ion mass spectrometry (SIMS) with the results shown in Figure 5.5. Be was implanted to a depth of 1 μm , however, the 550 $^{\circ}\text{C}$ anneal has driven the Be deeper into the APD forming a graded P-type region extending to a depth of 2 μm until the noise floor of the SIMS measurement was reached. Although the Be diffusion narrows the intrinsic region of the device, the graded P-type doping is desirable as the peak electric field within the APD is reduced due the low doping density at the junction. The graded P-type doping also increases the curvature of the spherical planar junction and alleviates the effects edge breakdown. Additionally, the thicker P-type region improves the excess noise performance

of the APD by decreasing mixed injection. With the knowledge of the diffusion rate of Be in InAs, the P-type grading of an APD could easily be tailored for specific applications by selecting an adequate annealing time to control the Be diffusion depth addressing both high gain and narrow pitch applications.

Si is known to be static in InAs during annealing [7], however, the Si dopants were traced into the intrinsic layer. As the Si tail only extends in the direction of epitaxial growth, parasitic incorporation of residual Si dopants from the reactor's chamber walls are suspected to cause the Si tail. Low background doping in the intrinsic region is required to maintain a uniform electric field across the avalanche region without inducing high tunnelling currents. As both the P and N-type doping profiles have shallow gradients, the background doping of the wafer was found by modelling the C-V characteristics of the APD using a one-dimensional Poisson solver rather than calculating the background doping from the incremental depletion width and assuming a one sided abrupt junction. The Si and Be doping concentrations within the APD were extrapolated from the SIMS measurements following the roll off of the diffusion tail down to the background doping level which was assumed to be n-type. An excellent fit between the experimental data and the modelled C-V characteristics is obtained for an intrinsic region background doping of $2 \times 10^{14} \text{ cm}^{-3}$ as shown in Figure 5.4.

With knowledge of the doping profile, the electric field within the APD was generated at -20 V as shown in Figure 5.5. The electric field is seen to be relatively flat across the device with the peak value reaching 33.5 kVcm^{-1} which is far below the value at which hole impact ionisation and tunnelling current can become significant in InAs APDs at 70 kVcm^{-1} . However, this model of the electric field was taken through the bulk of the device and is not indicative of the electric field hotspots formed at the periphery of the junction.

Due to the P-type doping of the planar APD being added post growth, excellent control of the doping profile and lower levels of background doping have been achieved from the planar structure resulting in very low background doping sustained over a large width. Previous reports of low background doping in InAs (below $5 \times 10^{14} \text{ cm}^{-2}$) have been achieved using Molecular Beam Epitaxy (MBE) which was preferred over MOVPE for reducing the incorporation of dicarbon deep-donors which are present in the MOVPE former [5]. However, the background doping level reported here is equal to lowest level reported using MBE growth [5]. The source of the background doping in the planar APDs was not determined. Since the growth of thick avalanche regions with low background doping are required for high gain InAs APDs, the development of planar APDs grown using MOVPE

rather than relying on MBE techniques is a welcomed development for targeting the lower cost APD market rivalling HgCdTe.

5.4 Responsivity and gain

Gain and responsivity measurements were performed using phase sensitive detection with a 1550 nm laser focused onto the P-type region of the APDs fabricated from InAs10 and InAs11. Using 1550 nm light, greater than 90% of the photons are absorbed in 2 μm which corresponds to the approximate depth of the P-type region as measured by SIMS. The responsivity was found to be 0.46 A/W at 296 K which is low compared to an epitaxially grown mesa InAs APD which was characterised at 0.55 A/W without AR coating [4]. This result supports the theory that the minority carrier diffusion length in the P-type region is significantly reduced due to implant damage. Photocurrent shunting can cause non-uniform responsivity across large area InAs photodiodes [8]. The shunt resistance of a planar APD with a diameter of 400 μm was found to be 57 Ω when measured between 0 to -0.1 V and 1.37 k Ω between -0.2 to -0.3 V. The series resistance was measured to be less than 15 Ω . The spatial responsivity of a 400 μm diameter planar InAs APD was mapped at room temperature at -0.3V and was found to have a uniform responsivity as shown in Figure 5.6.

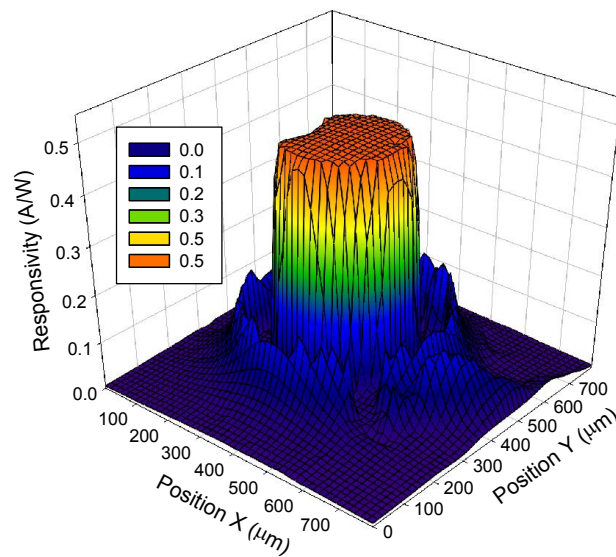


Figure 5.6: The spatial responsivity of a 400 μm diameter planar APD at -0.3 V at 296 K in response to 1550 nm wavelength light.

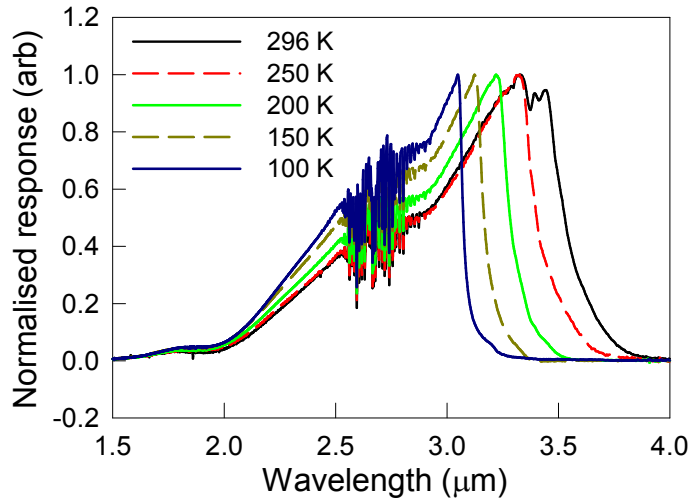


Figure 5.7: The spectral response of a planar InAs APD as a function temperature.

The spectral response of a packaged planar APD from InAs10 was measured as a function of temperature using a Fourier Transform Infrared Spectrometer (FTIR) with the devices held in a closed cycle helium cryostat. Measurements were performed over the temperature range from 296 to 200 K with the results shown in Figure 5.7 with the APD biased at -0.3 V. The interference on the measured signal observed between 2.5 and 2.8 μm is caused by atmospheric absorption effects due to strong absorption of water and carbon dioxide, and not an artefact of the detector response. The cut off wavelength was defined as the wavelength at which the responsivity has reduced to half of the peak value and was found to be 3.53 μm at 296 K reducing to a value of 3.07 μm at 100 K. Over this temperature range the bandgap has a linear temperature dependence of 0.269 meVK^{-1} which is in good agreement with published data [9]. The damage due to Be implantation was not observed to significantly change the spectral response of the APD.

The gain was measured on 17 APDs from InAs11 with diameters of 200 μm at room temperature and showed excellent uniformity. The 17 APDs were found to have an average gain of 5.2 at -4.5 V with a standard deviation of 0.08 corresponding to a sigma/mean of 1.5%. The gain at room temperature was also measured on APDs from InAs10 and is plotted in Figure 5.8 for comparison. It is often stated that larger gain at a particular bias voltage is achieved from InAs APDs with a thicker intrinsic region. However, the gain from InAs10 was found to be lower than InAs11 with a thinner intrinsic width for reverse bias voltages less 4 V. Under pure injection the gain of an InAs APD is simply given by $M = \exp(\alpha w)$. Wafer InAs11 was characterised to have a higher background doping and a thinner intrinsic region than InAs10 and consequently the peak electric field for a given voltage is larger in InAs11 than in InAs10 for a given voltage. At electric fields above $\approx 20 \text{ kVcm}^{-1}$ the electron

impact ionisation coefficient does not increase significantly with electric field and therefore higher gain is achieved from the thicker structure as frequently implied. However, at electric field strengths of below $\approx 20 \text{ kVcm}^{-1}$, at low bias voltages, the electron impact ionisation coefficient increases significantly with electric field and the increase in α outweighs the increase in w . Thus higher gain is achieved from the thinner structure. This is observed in Figure 5.8 at biases above 4 V, the gain of the thicker structure was larger as expected. Gain measurements could only be performed up to 5 V at room temperature before the dark current and gain was observed to drift due to a thermal runaway effect which is discussed in section 5.5.

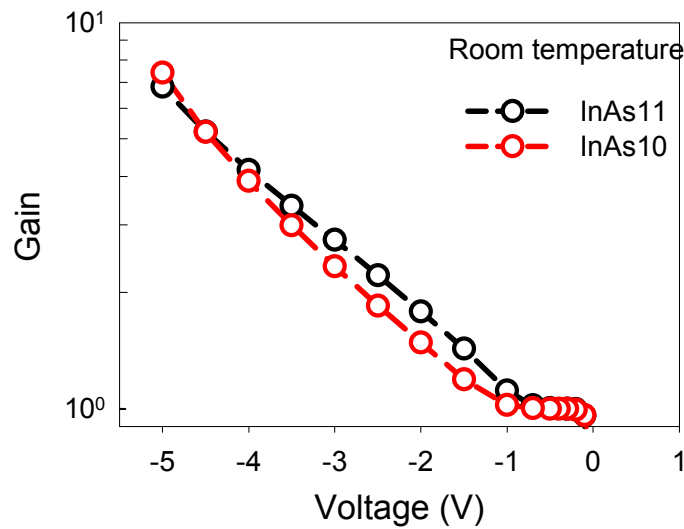


Figure 5.8: The gain of APDs fabricated from InAs10 and InAs11 at room temperature using 1550 nm excitation.

The gain from InAs10 was measured at 200 K and is shown in Figure 5.9 with a gain of 330 being achieved at -26 V. The gain measured from InAs11 achieved a peak gain of 75 at -24 V and once again showed a more rapid initial increase in gain before being surpassed at -3 V. The gain from a mesa InAs APD [2] and a $\text{Hg}_{0.62}\text{Cd}_{0.38}\text{Te}$ APD ($\lambda_c = 3.21 \mu\text{m}$) [10] operating at 200 K are also shown for comparison. Since the gain of an InAs APD is strongly dependant on the intrinsic region thickness, the gain of the planar APD reported here is the largest reported for an InAs APD. Furthermore, the gain is shown to be comparable with a state of the art $\text{Hg}_{0.62}\text{Cd}_{0.38}\text{Te}$ APD of similar cut-off wavelength.

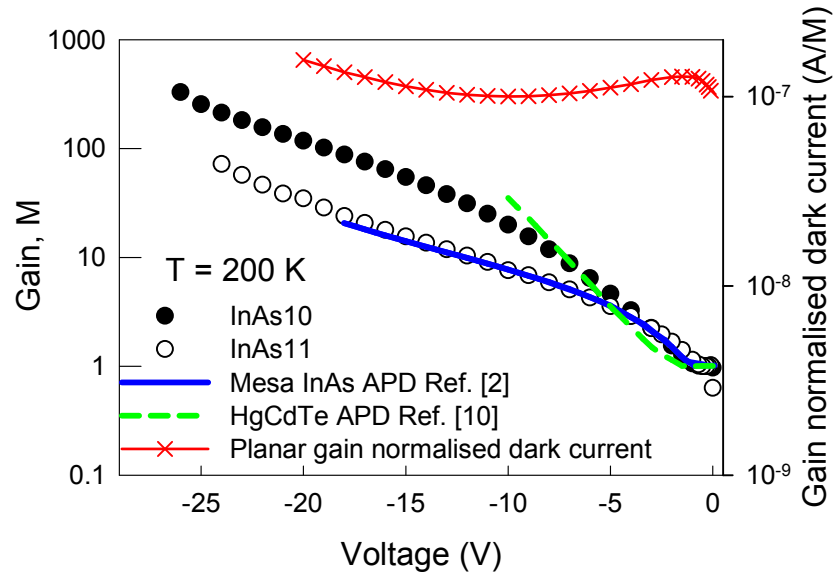


Figure 5.9: The gain of nominal 10 and 6 μm planar APD measured at 200 K using a 1550 nm laser in comparison to data from a mesa InAs APD at 200 K [2] and a $\text{Hg}_{0.62}\text{Cd}_{0.38}\text{Te}$ APD at 200 K [10]. The gain normalised dark current of the 200 μm diameter planar APD at 200 K is also shown.

The gain normalised dark current of a 200 μm diameter APD from InAs10 is shown in Figure 5.9 at 200 K and was found to remain relatively flat through the voltage range measured indicating that the dark current is multiplied at the approximately the same rate as the gain. The same finding was true for both InAs10 and InAs11 at room temperature. The dark current is therefore interpreted as being generated by a diffusion current from the P-type region of the APD which is simply multiplied in the same manner as a photocurrent. Additionally, due to the flatness of the gain normalised dark current, we can also conclude that the surface leakage of the APD remains low at large reverse bias voltages at 200 K.

5.5 Breakdown characteristics

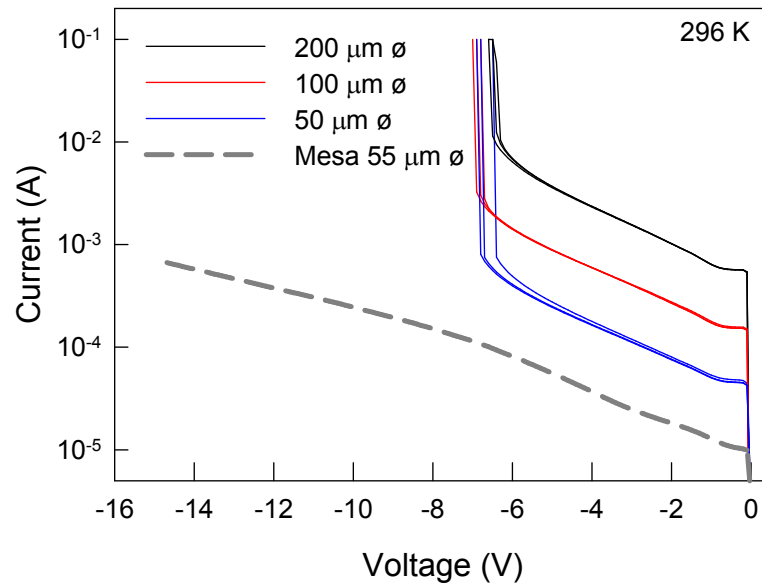


Figure 5.10: The breakdown characteristics of APDs from InAs11 at room temperature. The I-V characteristics of a mesa InAs APD at 290 K are also shown for comparison [11].

The I-V characteristics of APDs from InAs11 with diameters ranging from 200 to 50 μm were measured at room temperature with the results plotted in Figure 5.10. APDs were found to breakdown between -6 and -7 V using a compliance current of 10 mA to define breakdown. The breakdown voltage of the planar APDs is considered premature as mesa APDs with a similar intrinsic region widths can achieve a voltage in excess of 15 V at room temperature without breaking down as shown in Figure 5.10 [6, 11].

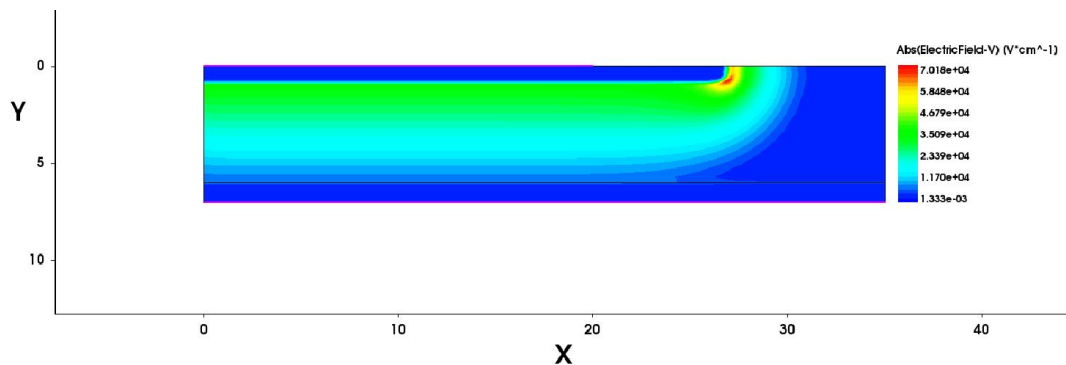


Figure 5.11: A false colour electric field plot of a cross section of a planar InAs APD at -10V

The device architecture required to achieve high gain in planar InAs APDs is expected to suffer from electric field hotspots due to the large ratio between the intrinsic region

thickness compared to the junction thickness as discussed in section 2.10. The electric field hotspots were suspected to cause premature breakdown at the periphery of the planar junction. Simulations of the electric field in a structure similar to InAs11 were carried out to assess the severity of electric field hotspots in the planar APDs. A planar InAs P-i-N APD was simulated with a 5 μm thick intrinsic region. The background doping of the intrinsic region of the wafer was found to be $5 \times 10^{15} \text{ cm}^{-3}$ as determined using C-V techniques at 77 K. The Si doping profile was assumed to be abrupt and was doped to $1 \times 10^{18} \text{ cm}^{-3}$. The P-type region was modelled on the as-implanted Be profile using two implants of 200 keV at $1 \times 10^{14} \text{ cm}^{-2}$ and 70 keV at $3.8 \times 10^{13} \text{ cm}^{-2}$ producing a junction approximately 1 μm deep. Diffusion of the Be and Si profile due to annealing, or parasitic incorporation from the chamber walls as measured by SIMS, were not accounted for.

Avalanche breakdown will only occur after significant hole impact ionisation has been established. Hole impact ionisation in InAs has not been measured at room temperature but for the purpose of this discussion will be assumed to be the same as at 77 K. Hole impact ionisation becomes significant an electric field of 70 kVcm^{-1} and increases rapidly thereafter [12], therefore breakdown in InAs is assumed to occur after the peak electric field has exceeded a value of 70 kVcm^{-1} . The peak electric field in APDs from InAs11 was simulated to reach 70 keV at -10 V reverse bias which is significantly larger than the breakdown voltage measured in the planar APDs at room temperature. However, this simulation only provides limited value due to the many unknown parameters used. Furthermore, it should be noted that Be diffusion caused by annealing has not been accounted for in the simulation and is likely to significantly reduce the severity of the hotspot by grading the doping region and increasing the curvature of the junction. A false colour plot of the electric field from a cross section of the APD from InAs11 is shown in Figure 5.11 at -10V.

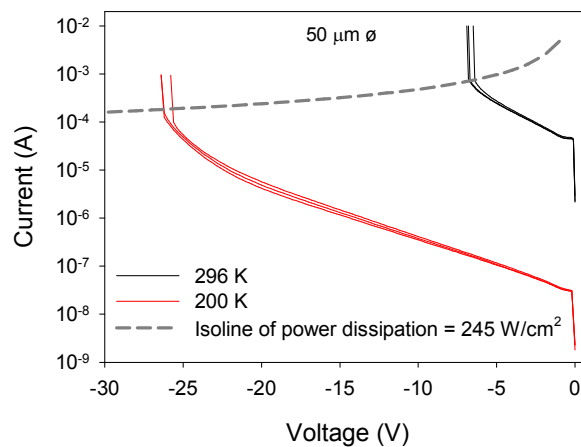


Figure 5.12: The breakdown characteristics of APDs with a body diameter of 50 μm are shown at room temperature and at 200 K. An isoline corresponding to a power dissipation of 245 Wcm^{-2} is also shown.

The breakdown characteristics of APDs with a diameter of 50 μm were measured at 200 K with the results plotted in Figure 5.12 along with the breakdown characteristics at room temperature. InAs is peculiar (relative to Si and GaAs) in that the electron impact ionisation coefficient is observed to have positive temperature dependence. Consequently, the breakdown voltage of the APDs increases as the temperature is reduced. At 200 K a voltage in excess of -26 V was achieved before break down which is larger than many recent reports of mesa InAs APDs, suggesting that high gain could be achieved from the planar structure. This result is quite remarkable as premature breakdown was found to be severe at room temperature. The power density at breakdown was found to be the same at both room temperature and 200 K. An isoline corresponding to a power dissipation density of 245 Wcm^{-2} is also plotted in Figure 5.12 and intersects both the room temperature and 200 K breakdown. The breakdown characteristics of the APDs have already been shown to display large temperature dependence. The high power dissipation in the APDs near breakdown could cause significant local heating of the APD, and therefore have a part in determining the breakdown characteristics.

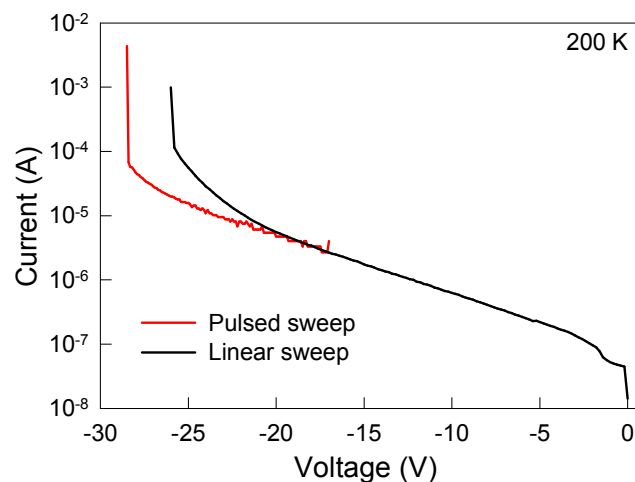


Figure 5.13: The I-V characteristics of APDs with a body diameter of 50 μm measured using a linear and pulsed sweep.

A pulsed bias scheme with a low duty cycle was used to measure the breakdown characteristics of the planar APD at 200 K and compared to the linear bias scheme usually used. The linear bias scheme had a 16 ms record time and sequentially increased the bias voltage from 0V until breakdown. The pulsed bias scheme biased the diode for 1 ms and recorded the voltage before returning to 0V for 1000 ms before recording the next measurement. Figure 5.13 shows the I-V characteristic of an APD measured using the two bias schemes at 200 K. At 20 V the pulsed and stepped bias scheme recorded similar values of the dark current in the APD, however, significant divergence is observed as large biases are applied. A larger breakdown voltage was achieved using the pulsed bias scheme

confirming that local device heating is a significant factor in determining the dark current and breakdown voltage of the planar APDs.

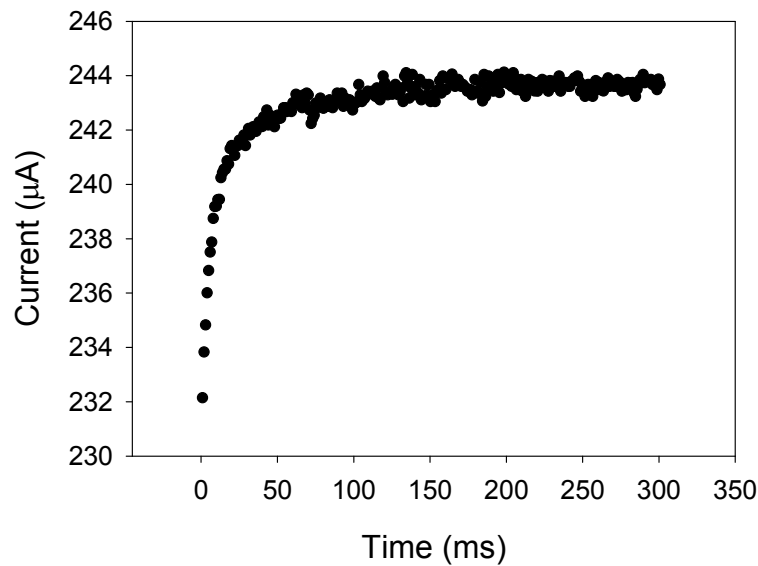


Figure 5.14: The I-V characteristics of APDs with a body diameter of 50 μm measured using a linear and pulsed sweep.

The dark current of a 200 μm diameter planar APDs was also found to increase with time when biased at a fixed voltage of -15 V over a period of several minutes as shown in Figure 5.14 (the APD was at 0V for some time before the measurement). After the bias was removed and the APD rested for several minutes the dark current returned to its original value upon biasing. The APD was passivated and as the dark current returns to its original value after resting suggests that the creeping dark current is not related to surface degradation. The increase in dark current followed a $1-\exp(-t)$ function showing a rapid initial increase in dark current before asymptotically approaching a fixed value. This behaviour is characteristic of a thermal systems step response, and therefore supports the theory of heating effects in InAs APDs. However, the measurement also shows that the heat dissipation with the APD can reach equilibrium with the heat loss as the APDs dark current stabilises.

It is hypothesised that a negative temperature dependence of impact ionisation coefficient in most semiconductors helps maintain stable gain characteristics within an APD. That is, a high level of local impact ionisation causes the temperature of the gain medium to increase. The increased temperature will reduce the local impact ionisation coefficient and quickly restore the avalanche build-up back to equilibrium. However, InAs is unique in that the electron ionisation coefficient shows a positive temperature dependence. Therefore InAs does not have an intrinsic quenching mechanism as the impact ionisation rate increases with

increasing temperature. Therefore, conditions could be achieved where the impact ionisation rate displays a thermal runaway effect ultimately leading to avalanche breakdown. The thermal runaway will be most prominent in an electric field hotspot due to the high levels of impact ionisation. However, a negative local impact ionisation coefficient is not the only mechanism capable of quenching the thermal runaway as heat will also be dissipated away from the hotspot.

For stable operation at high power densities, InAs APDs may require an active quenching or stabilisation circuit to prevent thermal runaway. Alternatively, a pulsed bias scheme could be used to achieve long term stability. However it should be noted that the thermal runaway effect observed in InAs is only significant if the power dissipation within the APD is high. Under such circumstances, avalanche gain from the APD may not be useful due to the high dark current. InAs APDs are more likely to be used in a region of lower dark current where the APDs show good stability.

The temperature of the APDs was reduced further to 100 K where the dark current had reduced by 3 orders of magnitude compared to 200 K. Consequently the power dissipation within the APDs is significantly reduced along with the electron impact ionisation coefficient. The J-V characteristics of APDs without a guard ring and with diameters of 200, 100 and 50 μm were measured and plotted in Figure 5.15. At low reverse biases the surface leakage dominated the dark current as seen by the largest current density being measured in the smallest APD. At large reverse biases the dark current increased rapidly and converged indicating that the dominant leakage mechanism at large biases is due to a bulk effect. The bulk leakage current at large reverse bias voltages is thought to be due to band-to-band tunnelling current rather than premature breakdown. The onset of the tunnelling current is likely to define the useful range over gain can be measured in the tunnelling current is a strong function of voltage once it becomes the dominant leakage mechanism. Consequently, tunnelling current rather than premature breakdown is likely to be the factor limiting the maximum useful gain achieved from an InAs APD at low temperatures.

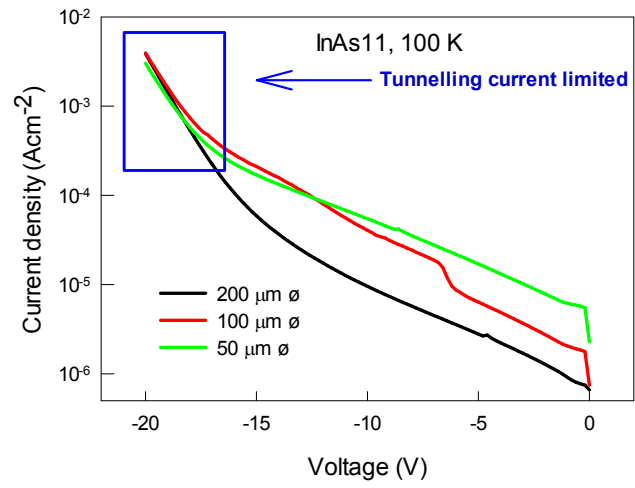


Figure 5.15: The J-V characteristics of APDs from InAs11 without a guard ring at 100 K.

5.6 Design of planar InAs APDs with guard rings

A thermal runaway effect generated in electric field hotspots is hypothesised to cause the premature breakdown measured in the planar APDs between room temperature and 200 K. Mitigation of the electric field hotspots using junction projection may be able to increase the breakdown voltage of the APDs and increase the gain.

Methods of mitigating premature breakdown due to electric field hotspots in planar APDs are reviewed in section 2.11. Double diffused junctions are well suited to APDs with thin multiplication regions, however, InAs APDs are required to have thick intrinsic regions to achieve high gain. Furthermore, the background doping of the intrinsic region should remain low and therefore altering the space charge directly underneath the junction is also unsuitable. A floating guard ring structure is likely to be the most suitable approach and can be formed from a single implantation step. In addition to increasing the breakdown voltage, guard rings have also been shown to reduce the surface leakage of APDs by reducing the surface electric field.

The manufacturing tolerance for fabricating an effective guard ring structures is small as variations in the background doping concentration of the intrinsic region or the doping profile of the main junction and guard ring can drastically alter the breakdown performance of the APD. Typically, many iterations of a well-controlled growth and fabrication program are required to achieve an optimised structure. However, the wafers grown in this study were obtained from a reactor on a communal growth program and therefore predetermination of the background doping within the tolerance required for effective guard ring support was impossible. The variation of the background doping concentration of the intrinsic region from wafers used in this study was expected to be from 1×10^{14} to $1 \times 10^{15} \text{ cm}^{-3}$. To account for this large variation in background doping, guard ring structures were designed to provide some protection across the extremes. The guard ring placement tolerance is relaxed slightly by increasing the number of guard rings used in the design. To give guarded InAs APDs the best chance of working, designs with one and two guard rings were explored.

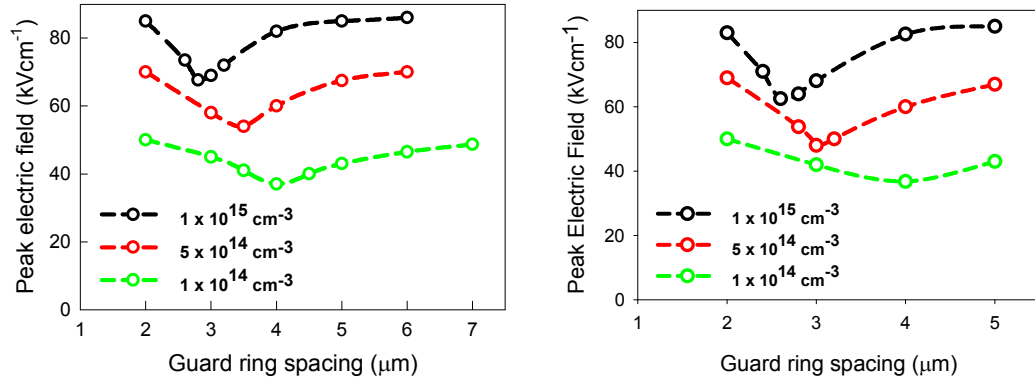


Figure 5.16: The peak electric field of 50 μm diameter planar InAs APDs at -10 V as a function of guard ring spacing one (Left) and two (Right) guard rings.

A 2-dimensional Poisson solver was used to simulate the electric field developed in planar InAs APDs with one and two guard rings. Lateral diffusion of Be caused by annealing was neglected in the initial APD simulations as the diffusion tail on the lateral doping profile was unknown. However, lateral straggle underneath the implantation mask was included in the design. The exact specification of the guard ring doping profile and wafer thickness is described in appendix 8.5. The peak electric field in guarded APDs was simulated for guard rings spaced 2 to 7 μm from the main junction across background doping concentrations varying from 1×10^{14} to $1 \times 10^{15} \text{ cm}^{-3}$. The guard ring spacing is defined as the width of the mask used to fabricate the guard rings, rather than the distance between the junctions. The peak electric field as a function of guard ring spacing for three background doping concentrations is shown in Figure 5.16 for APDs with one and two guard rings at a reverse bias voltage of 10 V. The background doping concentration has a large effect on determining the optimum guard placement in 1 and 2 guard ring structures. Additionally, correct guard ring placements become crucial for maintaining an electric field below 70 kV/cm when the background doping concentration of the wafer is high, however, if low background doping is achieved the tolerances are reduced significantly. The simulation results presented in Figure 5.16 and show that guard rings spaced 2.5 to 3.5 μm from the main junction are required to cover the expected background doping concentration range. However, lateral diffusion of Be caused by the 550 °C anneal had not been accounted for in the guard ring design. From section 4.8 the lateral Be diffusion was estimated to diffuse 2.5 μm and so guard rings spaced 3 – 6 μm from the main junction are simulated to provide good protection over the range of background doping conditions expected.

5.7 Fabrication and characterisation of a guard ring test structure

The effectiveness of guard ring designs can be assessed by comparing the breakdown voltage of APDs with and without guard rings. However, this analysis only provides limited feedback to the designer, and unexpected results caused by differences between the simulated and fabricated devices are difficult to identify. A guard ring test structure can be utilised to aid verification of guard ring designs. In a guard ring test structure, a contact is made to the floating guard ring and the potential adopted by the ring can be measured as a function of voltage applied to the main junction. The potential adopted by guard ring can be compared to simulation results to verify the design.

Simulations of the potential adopted by a single floating guard ring are plotted in Figure 5.17 as a function of the guard ring separation distance for APDs biased at -10 V. The guard ring design used in the simulations was identical to that used for simulations in Figure 5.16. Guard rings placed 2 μm from the main junction were simulated to adopt a potential of -10 V showing that a short circuit had formed between the main junction and the guard ring. The doping profile of the main junction and the guard ring have overlapped in this structure due to the lateral straggle of Be underneath the implantation mask. A potential of 0 V on the guard ring indicates that the depletion region edge has formed before punching through to the guard ring as the guard ring potential remains fixed to the bulk. This effect is seen to be a strong function of the background doping of the wafer. Guard rings operating in either a short circuit or 0 V regime do not offer protection to the APD. The effectiveness of guard rings adopting a potential between these two can be assessed through comparison with simulation results.

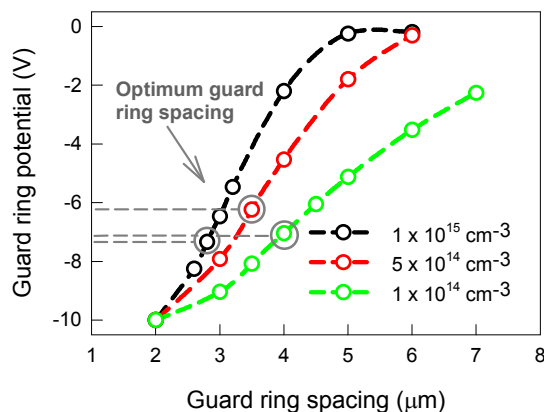


Figure 5.17: The voltage adopted by a floating guard ring as a function of distance from the main junction. The ideal voltage adopted by the guard ring to produce the lowest electric field is also shown

For an InAs APD operating at -10 V the optimum guard ring placement can be found from Figure 5.16 by locating the minimum electric field for a given background doping concentration. For a background doping of $1 \times 10^{15} \text{ cm}^{-3}$ the guard ring spacing that minimised the peak electric field was simulated to be $2.8 \mu\text{m}$ as shown on Figure 5.16. The $2.8 \mu\text{m}$ guard ring separation distance has been circled on Figure 5.17 and is expected to adopt a potential of -7.3 V. This value can be compared to the voltage measured on the guard ring test structure to provide direct feedback that the APD have been fabricated correctly. This process has been repeated for background doping densities of 5×10^{14} and $1 \times 10^{14} \text{ cm}^{-3}$. It can be seen that under the conditions simulated, an optimised guard ring will adopt a potential equal to 60-80 % of the applied voltage.

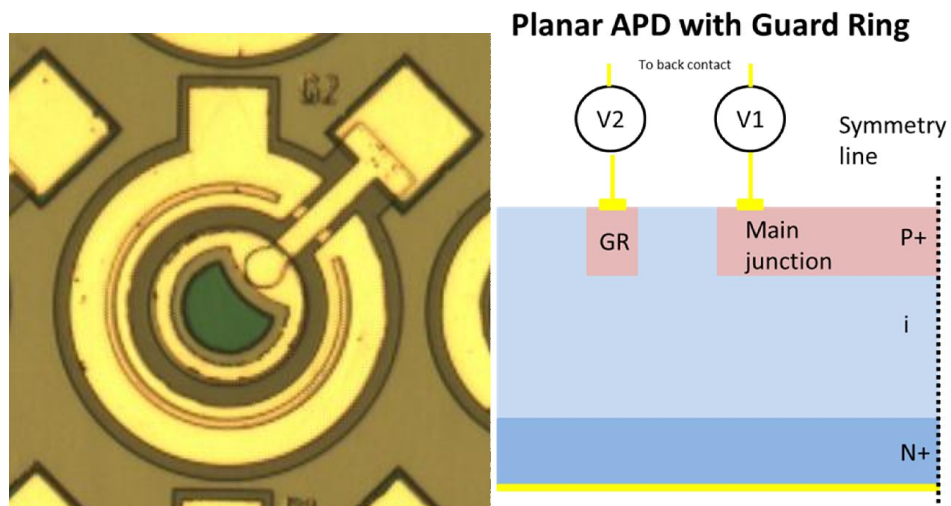


Figure 5.18: A photograph and a schematic diagram of the guard ring test structure.

Guard ring test structures were fabricated as detailed in section 4.7, however, the photoresist mask was also used to define a floating guard ring around the main junction during Be implantation. The thickness of the guard rings was increased to $30 \mu\text{m}$ so that metal contacts could be deposited onto the guard ring. Test structures were fabricated with guard rings spaced $3 - 6 \mu\text{m}$ from the main junction in line with simulations. In simulations, the width of the guard ring had no effect on the potential it adopts and guard rings with a thickness of $3 \mu\text{m}$ will be employed in the optimised designs.

A photograph and a schematic diagram of a guard ring test structure is shown in Figure 5.18. The potential adopted by the guard ring was measured as a function of the voltage applied to the main junction at room temperature. The results from APDs with main junction diameters of 200 and $50 \mu\text{m}$ from wafer InAs11 are shown in Figure 5.19. The short circuit voltage is marked on the graph for comparison. The guard ring potential is seen to decrease at any given voltage as the separation distance between the guard ring and the main junction is

increased. However, many of the guard ring structures follow the short circuit potential and do not show punch through. Guard ring showing such characteristics will not provide protection to the APD and simply act as a junction extension. Punch through was observed at ~ 0.5 V for the guard ring placed $5.5 \mu\text{m}$ from the main junction and at 1 V for the guard ring placed $6 \mu\text{m}$ away. Only these two structures will provide protection to the APD and mitigate hotspots. The potential of the guard ring placed $6 \mu\text{m}$ from the main junction follows a voltage of approximately $2/3$ of the applied bias which was simulated to be optimum for operation up to 10 V. However, $6 \mu\text{m}$ is the largest separation distance included in the design and indicated that the lateral Be diffusion was underestimated when being designed.

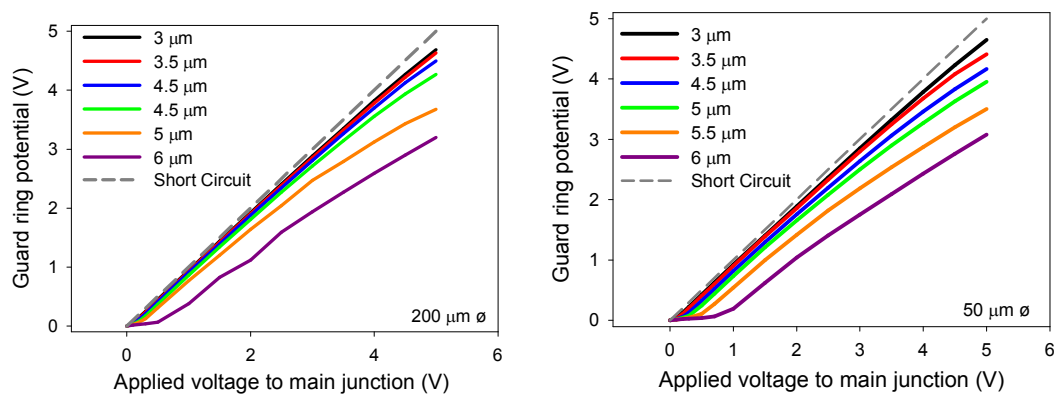


Figure 5.19: The potential adopted by floating guard ring at various distances from the main junction as a function of applied bias for an APD with a body diameter of $50 \mu\text{m}$ and $200 \mu\text{m}$. A short circuit is also shown for comparison.

5.8 Breakdown of planar InAs APDs with guard rings

The I-V characteristics of 8 APDs without guard rings and with a body diameter of $50 \mu\text{m}$ were biased to breakdown at room temperature with the I-V characteristics plotted in Figure 5.20. The I-V characteristics of APDs with one and two guard rings placed various distances from the main junction are plotted in Figure 5.20 and Figure 5.21 respectively with an enlarged graph of the breakdown also shown for each. The measurements presented are from a single unit cell to minimise wafer uniformities that may influence results.

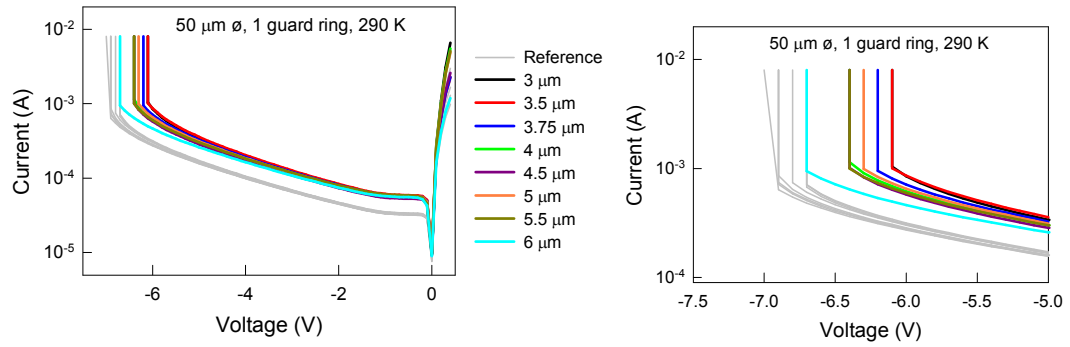


Figure 5.20: Left, the breakdown characteristics of 8 x 50 μm diameter planar APDs at 290 K. The breakdown characteristics of 50 μm diameter planar APDs with one guard ring spaced at various distances from the main junction is also shown. Right An enlarged graph of the breakdown characteristics.

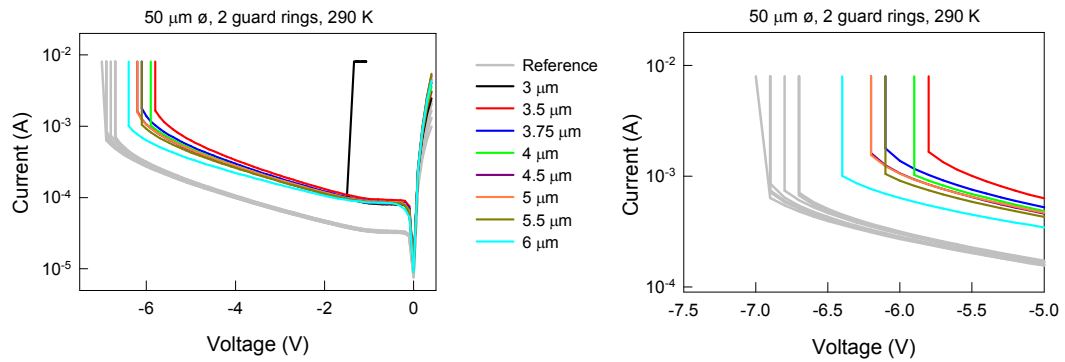


Figure 5.21: Left, the breakdown characteristics of 8 x 50 μm diameter planar APDs at 290 K. The breakdown characteristics of 50 μm diameter planar APDs with two guard ring spaced at various distances from the main junction is also shown. Right An enlarged graph of the breakdown characteristics.

The addition of guard rings was found to increase the dark current of the APDs with the dark current of APDs with 2 guard rings being larger than those with one. However, the dark current-density of the APDs (when including the area occupied by the guard rings) was found to have slightly reduced in the guarded APD structures. The breakdown voltage of 8 nominally identical reference APDs was found to vary between 6.7 to 7 V and indicates a tolerance in determining the breakdown voltage of the APDs due to fabrication and measurement non-uniformities. The variation in the breakdown voltage was suspected to be caused by slight variations in the series resistance of the APDs which was detected by measuring the forward I-V characteristics. A relationship between APDs showing a higher breakdown voltage and also a high series resistance was found, however, it was not corrected for as the forward resistance was also found to be slightly variable. Variations in

the APD series resistance could be caused by manually probing the APDs. One APD with two guard rings was found to breakdown uncharacteristically early and is considered to be a device failure. The breakdown voltage of APDs with guard rings is plotted as a function of the guard ring spacing as shown in Figure 5.22 for APDs with one and two guard rings. The breakdown voltage was found to have a weak but positive dependence on the guard ring spacing. The poor correlation is within the tolerance accountable for due to experimental non-uniformities in the series resistance of the APDs. Guard rings placed 6 μm from the main junction displayed the largest breakdown voltage in both 1 and 2 guard ring configurations which corroborates with results from the guard ring test structure. However, the breakdown voltage of APDs without guard rings was on average larger than APDs with guard rings. Furthermore APDs with 2 guard rings had on average a lower breakdown voltages than APDs with 1 guard ring going against theory and simulation results.

It is unclear why the breakdown voltage of the InAs APDs decreased when using guard rings as a non-optimised guard ring should not decrease the breakdown voltage. However one explanation could be that contaminates from the mask edges are transferred into the semiconductor through collisions with the implanted Be ions. The addition of guard rings increases the length of mask edges on a guarded APD and therefore the total contamination is also increased. However, there is no evidence to support this hypothesis. The simulation result in Figure 5.16 show a minima in the peak electric field for an optimised guard ring spacing. However, the breakdown voltage of the APDs in this study was only observed to increase with increasing guard ring separation distance suggesting that the minima was not reached. This also corroborates with observation from the guard ring test structure that the lateral Be diffusion has been underestimated and that guards rings placed at a distance greater than 6 μm from the main junction may increase the APD breakdown voltage further.

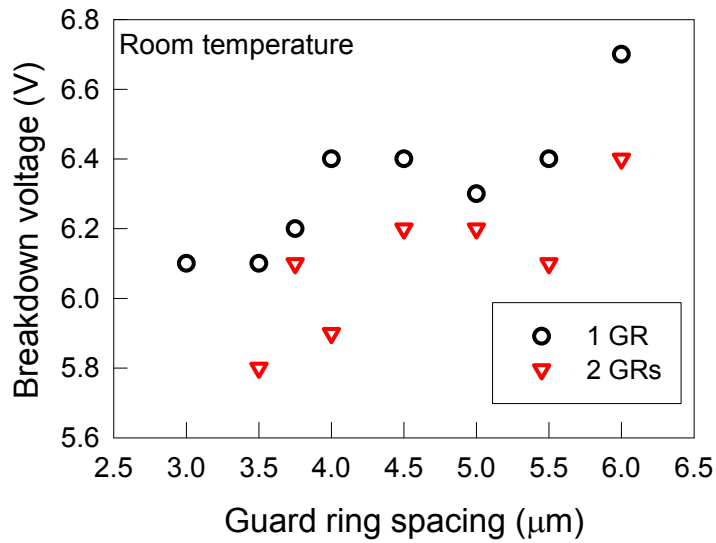


Figure 5.22: The breakdown voltage of InAs APDs with one and two guard ring as a function of guard ring spacing.

The breakdown characteristics of APDs with one and two guard rings were measured at 200 K with the results shown in Figure 5.23 and Figure 5.24 respectively along with the breakdown characteristics of reference APDs. An enlarged graph of the breakdown characteristics is also shown. InAs is peculiar in that the electron impact ionisation coefficient is observed to have positive temperature dependence. Consequently, the breakdown voltage of the APDs increases as the temperature is reduced. At 200 K the dark current of the APDs achieved a voltage in excess of -25 V before breaking down which is larger than any InAs APD reported in literature. This result is quite remarkable as premature breakdown was found to be severe at room temperature.

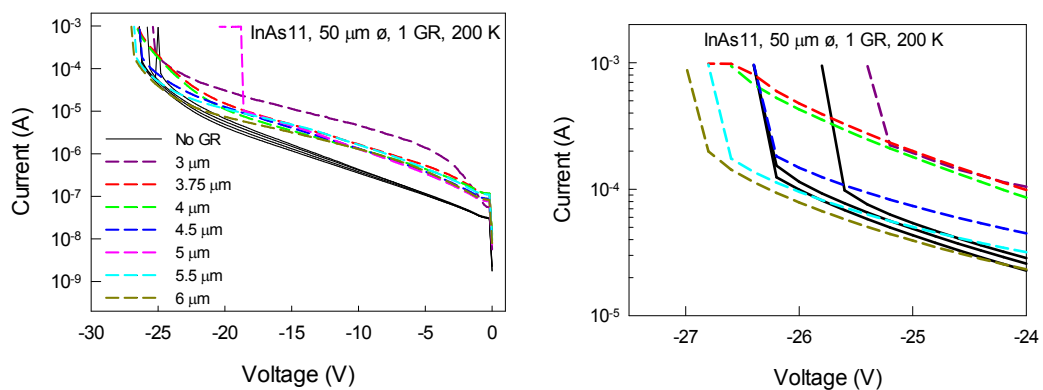


Figure 5.23: Left, the breakdown characteristics of 50 μm diameter planar APDs at 200 K. The breakdown characteristics of 50 μm diameter planar APDs with one guard ring spaced at various distances from the main junction is also shown. Right An enlarged graph of the breakdown characteristics.

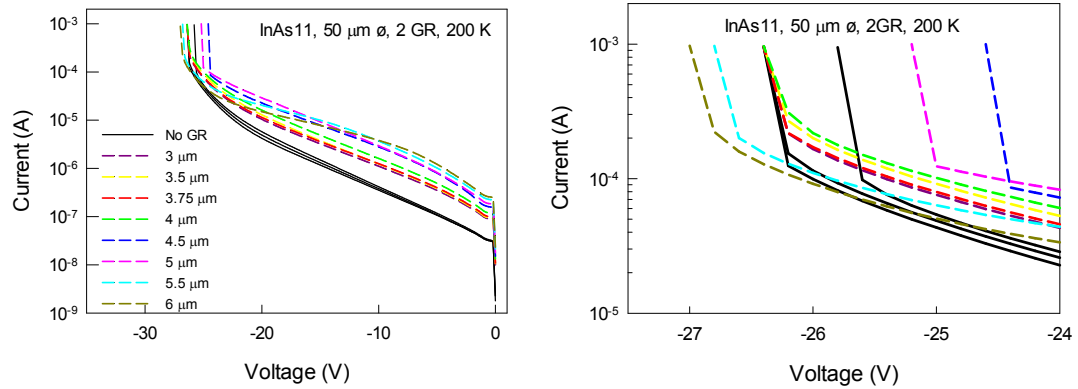


Figure 5.24: Left, the breakdown characteristics of 50 μm diameter planar APDs at 200 K. The breakdown characteristics of 50 μm diameter planar APDs with two guard rings spaced various distances from the main junction are also shown. Right, an enlarged graph of the breakdown characteristics of 50 μm diameter planar APDs at 200 K.

The dark current of all APDs had reduced by approximately 3.5 orders of magnitude by reducing the temperature from room temperature to 200 K. At voltages near breakdown the dark current of APDs with guard rings spaced 5.5 and 6 μm were measured to be lower than that of the reference diodes. In addition to this the guard rings spaced 5.5 and 6 μm from the main junction were observed to have a larger breakdown voltage than the reference APDs for both the 1 and 2 guard ring structures. The reduction in the dark current of the guarded APDs near breakdown is due to a reduction in the peak electric field in the hotspot. Reducing the electric field in the hotspot both reduces the local carrier generation rate within the hotspot while also reducing the surface electric field to reduce surface leakage. Guard rings placed 6 μm from the main junction were found to be successful in increasing the breakdown voltage of the APD, however, the increase in breakdown voltage was only 0.5 V corresponding to an increase of $\approx 2\%$.

5.9 Discussion

A planar InAs topology has been pursued to achieve higher reliability, uniformity and improve the manufacturing confidence. InAs APDs have shown a dark current uniformity (defined by the ratio of standard deviation to mean) of 0.52 %, a dark current density of 400 μAcm^{-2} at 200 K, and a gain of 330 at only -26 V which are either improved or equal to the performance achieved from mesa APDs. The gain of the planar InAs APDs matched that of state of the art HgCdTe APDs, however, there is clear room for improving the dark current as the dark current of HgCdTe APDs is still significantly lower. Surface leakage was present and contributed significantly to the dark current at low temperatures. Furthermore the bulk

leakage of the planar InAs APDs was larger than mesa APDs at room temperature. Optimisation of the responsivity and dark current of planar APDs was unsuccessful and it is clear that a better understanding of the mechanism that determines the dark current in InAs APDs is required to be able to see how to progress. Furthermore, reducing the dark current to reduce the overall power dissipation in InAs APDs appears to be key in achieving larger gain.

It was discussed that a self-passivation fabrication sequence could help to significantly reduce the surface leakage of the planar APDs, however, a suitable material has not yet been identified. An alternative solution could be to incorporate a wide bandgap lattice matched surface layer grown in-situ. The wide bandgap layer may be less susceptible to surface leakage. Additionally hard passivation layers such as SiN may be compatible with the wide bandgap semiconductor. Lattice matched wide bandgap alloys, such as AlAsSb and GaAsSb, are available to InAs. Furthermore, by moving the P-region to a wide-bandgap material, the diffusion current would be significantly reduced which could result in planar InAs APDs operating with very low dark currents. However, it is noted that by utilising a wide bandgap P-type layer, the infrared wavelengths would be absorbed within the intrinsic region of the APD causing a slight increase in excess noise and decrease in the gain.

A very wide intrinsic region was achieved from the planar InAs APD and consequently the largest gain from an InAs APD was achieved at 200 K. Increasing the depletion region to achieve larger gain from InAs APDs is becoming increasingly difficult due to difficulties in achieving a very low background doping concentration ($1 \times 10^{14} \text{ cm}^{-2}$) over the entire intrinsic region. The avalanche region of an InAs APD could instead flow laterally across the surface of the wafer to enable huge depletion regions to be achieved from only a thin epitaxially grown layer. This device design would greatly lift the stringent growth requirements. Lateral InAs APDs are explored in the next chapter.

5.10 Conclusion

The bulk leakage current in InAs planar APDs is generated by a diffusion process from the P-type region of the device within the temperature range of 296 to 200 K. The dark current of planar InAs APDs was found to be 1 Acm^{-2} at room temperature which is approximately 1 order of magnitude larger than a typical mesa APD. However, at 200 K the dark current of the mesa and planar APDs were found to be very similar at $400 \mu\text{Acm}^{-2}$. This is due to the dominance of SRH leakage from the intrinsic region in both structures within this temperature range. C-V characterisation of the planar APDs revealed a low background

doping of $\sim 2 \times 10^{14} \text{ cm}^{-3}$ was achieved with depletion widths as large as $\sim 8 \text{ }\mu\text{m}$. Consequently the planar APDs displayed a very high gain of 330 at -26 V at 200 K. Planar InAs APDs were found to breakdown at high bias voltages caused by an unusual thermal runaway effect due to the positive temperature dependence of the impact ionisation coefficients in InAs. The breakdown was most severe in electric field hotspots at the edge of the planar junction. Diffusion of the Be implanted profile caused by annealing acted to reduce the severity of the hotspots in the planar APDs, however, it was necessary to design guard ring structures to reduce the dark current and reduce premature breakdown at 200 K. Perhaps due to an underestimation of the lateral Be diffusion, guarded APDs only displayed a 0.5 V increase in breakdown voltage.

5.11 References

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6 Si implantation for N-type doping and the fabrication and characterisation of lateral APDs

6.1 Introduction

InAs APDs require a thick avalanche region with low background doping to yield high gain. However, the peak electric field must also be kept below 70 kVcm^{-1} to prevent hole impact ionisation and the onset of significant tunnelling current. To achieve low background doping, epitaxial growth techniques are utilised, however, growth rates are very slow and producing thick structures is time consuming. Furthermore, defects propagate through epitaxial layers and achieving high crystal quality in thick structures is challenging. To circumvent these issues the avalanche gain could develop laterally, parallel to the wafer surface, so that only a thin epitaxial layer is required to support the structure. The thickness of the epitaxial layer in a lateral APD would only be required to provide good optical absorption and therefore could be fabricated from $\approx 3 \mu\text{m}$ of InAs. Furthermore the lateral APD will give excellent control over the depletion width, and thus the gain, as the positions of the surface doped regions can be manipulated post growth. A schematic diagram of a planar APD requiring a thick epitaxial region and a lateral APD are shown in Figure 6.1.

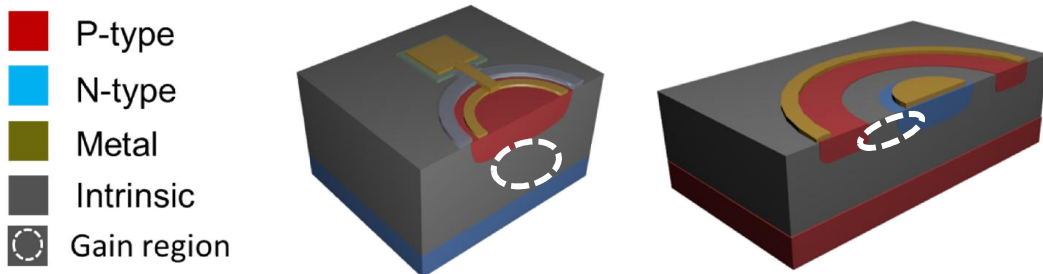


Figure 6.1: (Left) A schematic diagram of a cross section of a planar InAs APD. (Right) A schematic diagram of a cross section of a Lateral InAs APD

The lateral gain will be developed between P and N-type regions formed in the surface of the wafer. Be implantation can be utilised for P-type doping, however, selective area N-type doping in InAs is relatively unexplored. In this chapter Si implantation and annealing is developed as a method of selective area N-type doping in InAs. Lateral APD structures are simulated to assess the best design. A range of lateral APDs structures are fabricated using optimised Si and Be implantation and annealing conditions. The dark current, gain and responsivity of the various lateral APDs designs are characterised.

6.2 Review of implantation and annealing in InAs for N-type doping

Most N-type dopants have low diffusivity in semiconductors and therefore diffusion techniques are limited to producing very shallow doping profiles. McNally [1] demonstrated a 4 by 4 array of planar InAs photodiodes using S implantation into a P + substrate. The implant dose was $8 \times 10^{14} \text{ cm}^{-2}$ producing a peak concentration of $1 \times 10^{19} \text{ cm}^{-3}$ and after implantation samples were annealed at 450 °C for 1 hour. The photodiodes produced a peak detectivity of $1.3 \times 10^{11} \text{ cmHz}^{-1/2}\text{W}^{-1}$ at 3.1 μm at 77 K measured at 0 V and showed sigma/mean variation of 4 % across the array. Gerasimenko et al. [2] found that the activation of InAs implanted with sulphur peaks after annealing at a temperature of 350 °C for 30 minutes. Optimised implantation and annealing conditions were utilised to fabricate planar photodiodes with field plating to reduce the surface leakage. Using an optimised field plating voltage, the photodiodes showed low dark current at 0 V, however, the dark current rapidly increased with reverse bias voltage. Si implantation is preferred for N-type doping InGaAs showing low diffusivity and higher reported solubility compared to other n-type dopants S, Se, and Te [3]. Si implantation has a very low diffusivity in InAs and an implantation profile has reported negligible diffusion after annealing, furthermore, hot implants at 100 °C were found to significantly increase the dose required to produce amorphous crystal indicating that dynamic annealing may be significant in InAs [4]. Recently, Lind et. al [5] have reported the activation of Si implants with concentrations between $2 \times 10^{18} \text{ cm}^{-3}$ and $2 \times 10^{20} \text{ cm}^{-3}$. Using an implant temperature of 100 °C, a peak Si concentration of $4.9 \times 10^{19} \text{ cm}^{-3}$ was reported when annealing temperature of 700 °C for 30 s without producing amorphous crystal. Activation of Si was observed at 400 °C, which was the lowest temperature studied, and the highest activation was achieved by annealing at 700 °C for 30 s. It was also indicated that the activation of Si was less than 10 % which is surprisingly low compared to InGaAs. However, it should be noted that Van der Pauw Hall effect measurements are usually required to accurately measure the active doping concentration. Lind et. al reported that due to the very high surface leakage across the InAs test structures, Van der Pauw measurements could not be performed. All results were instead inferred from the Raman scattering spectra and no electrical measurements or characterisation was reported.

Si is anticipated to produce less implant damage and have a longer projected range compared to S due to its lower atomic mass. Furthermore Si has been shown to have low diffusivity with low diffusion of the implant profile upon annealing. For these reasons Si implantation will be investigated for selective area N-type doping in InAs. Lind et. al have not reported on the electrical characterisation of Si implantation into InAs and therefore a

study on the implant and annealing conditions will be necessary. The rules of thumb for dynamic annealing are that elements with higher atomic mass and N-type dopants have higher threshold energies. Although the threshold temperature of Be is below room temperature, the threshold temperature of Si is expected to be significantly larger. Furthermore, the activation energy of Si in InGaAs is almost double that of Be [6]. Consequently for the first time hot implants will be investigated for Si implantation into InAs.

6.3 Si implantation for selective area N-type doping

Samples were fabricated from InAs12 which was an InAs N-i-P wafer grown using MBE at 500 °C. The wafer consisted of a 2 µm thick Si doped N-type layer grown on a 8 µm intrinsic layer on a 2 µm Be doped P-type layer grown on an P+ (100) Zn doped InAs substrate. Prior to implantation 4 µm was etched from the surface of the wafer removing the existing N-type layer. Implanted N-type regions will be required to reduce contact resistance and confine the depletion region away from the contact metal. The implantation profile was simulated using TRIM with two implants of $6.5 \times 10^{13} \text{ cm}^{-2}$ at 190 keV and $1 \times 10^{13} \text{ cm}^{-2}$ at 60 keV producing a flat doping profile with a concentration of $2 \times 10^{18} \text{ cm}^{-3}$ to a depth of 300 nm with the junction extending to 500 nm as shown in Figure 6.2. The implants were carried out 7 ° off axis at Cutting Edge Ions in California, USA. Blanket implants were carried out at temperatures of 30, 100 and 200 °C to investigate the effect of dynamic annealing. After implantation samples were fabricated as mesa diodes with the fabrication procedure described in appendix 8.1.

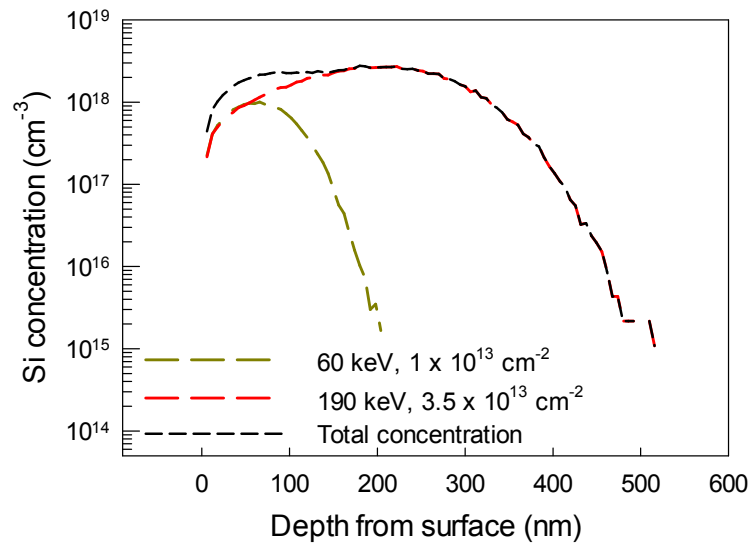


Figure 6.2: The Concentration of Si implanted into InAs 7 ° off the (110) axis at energies of 190 and 60 keV with doses of $3.5 \times 10^{13} \text{ cm}^{-2}$ and $1 \times 10^{13} \text{ cm}^{-2}$ respectively.

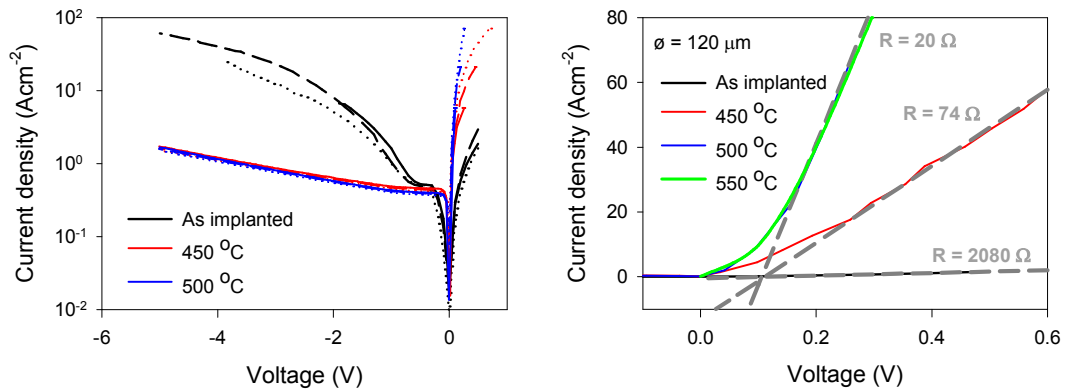


Figure 6.3: (Left) The J-V characteristics of diodes with diameters of 420, 220 and 120 μm implanted at 30 °C and annealed at 450 and 500 °C. The J-V characteristics of unannealed diodes are also shown. (Right) The series resistance fitted to the forward bias current of diodes with diameters 120 μm .

The J-V characteristics of mesa diodes with diameters of 420, 220 and 120 μm implanted at 30 °C and annealed at 450 and 500 °C are shown in Figure 6.3 along with the J-V characteristics of unannealed diodes. The J-V characteristics of diodes annealed at 550 °C are not plotted as the diodes showed high surface leakage current, however, the forward bias current is shown. Unannealed diodes were found to have low dark current density up to -0.5 V after which it increased rapidly. As the background doping type of the intrinsic region is N-type, the depletion in the diodes will be confined to the epitaxially grown layer and not

the Si implanted layer near 0 V. The rapid increase in dark current observed at reverse bias voltages greater than -0.5 V is therefore likely to coincide with the depletion region extending into the heavily damaged Si implanted region layer. Furthermore the series resistance of unannealed diodes was very high at 2 k Ω as calculated by fitting to the forward leakage current of a diode with a diameter of 120 μm as shown in Figure 6.3. Both observations indicate poor recovery in unannealed diodes implanted at room temperature. Annealing at 450 $^{\circ}\text{C}$ significantly improved the J-V characteristics and lowered the series resistance (annealing was carried out before the contacts were deposited), however, the lowest series resistance of only 20 Ω were measured in diodes annealed at 500 $^{\circ}\text{C}$ and 550 $^{\circ}\text{C}$. Although higher annealing temperatures reduced the series resistance of the diodes indicating better dopant activation and reduced damage, the dark current density was not significantly affected. The dark current density of Si implanted diodes was found to be significantly lower than that of Be implanted diodes at room temperature. For diodes implanted with Be, the dark current was a good indicator of the crystal quality as the dominant leakage mechanism was generated by a diffusion current from the implanted P-type region. However, analysis the dark current of Si implanted diodes showed that the dark current increased at approximately the same rate as that from Be implanted diodes, indicating that the dark current was dominated by diffusion current from the epitaxially grown P-type regions, and not the N-type Si implanted region. Therefore analysis of the dark current is not good indicator of recovery. The contact resistance of the diodes has contribution of both contacts, however, the back contact to the P-type region is significantly larger than the top contact to the implanted Si region and therefore a better indicator of recovery.

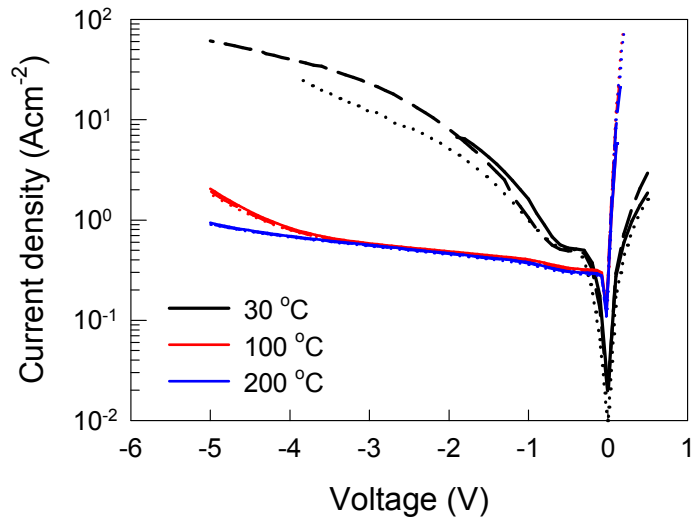


Figure 6.4: The J-V characteristics of diodes with diameters of 420, 220 and 120 μm implanted at 30, 100 and 200 $^{\circ}\text{C}$.

The J-V characteristics of unannealed diodes implanted at 30, 100 and 200 $^{\circ}\text{C}$ are shown in Figure 6.4. Diodes implanted at 100 and 200 $^{\circ}\text{C}$ showed significantly lower dark current density than those implanted at 30 $^{\circ}\text{C}$ indicating that hot implants were effective, furthermore, the forward resistance of diode implanted at 100 and 200 $^{\circ}\text{C}$ were very low. The dark current density of diodes implanted at 100 $^{\circ}\text{C}$ increased significantly compared to diodes implanted at 200 $^{\circ}\text{C}$ at voltages greater than 4 V. As both structures share the same doping profile and the diffusivity of Si and Zn (P-type dopant) is low at the annealing temperatures studied, the additional leakage cannot be attributed to band to band tunnelling as was the case for the Be annealing study. The additional leakage mechanism is therefore likely to be related to the high density of traps through incomplete recovery and in the form of very high SRH or trap assisted tunnelling. However, such analysis was not performed on the sample and no evidence is presented to support this hypothesis.

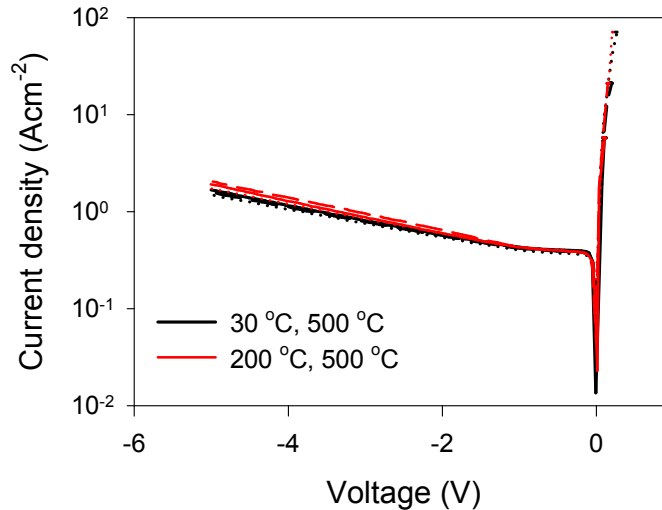


Figure 6.5: The J-V characteristics of diodes with diameters of 420, 220 and 120 μm implanted at 30 and 200 $^{\circ}\text{C}$ and annealed at 500 $^{\circ}\text{C}$.

The benefits of the hot implant are clear in unannealed diodes and to investigate whether annealed hot implants can further improve the diodes performance, diodes were implanted at 200 $^{\circ}\text{C}$ and annealed at 500 $^{\circ}\text{C}$ with the J-V characteristics shown in Figure 6.5. The J-V characteristics of diodes implanted at 30 and annealed at 500 $^{\circ}\text{C}$ are also plotted. The similarity between the dark current density and contact resistance indicates that that hot implants provide only a negligible difference after annealing. However, relatively large area diodes ($\text{Ø} = 120 \mu\text{m}$) were utilised for this study with relatively low doping densities required to achieve low forward resistance. Significantly higher doping densities may be required to maintain low contact resistance in small area diodes or devices, in which case further investigation of threshold implant temperature, which was found to lie between 100 and 200 $^{\circ}\text{C}$ may be useful. Furthermore hotter annealing temperatures may be required to observe the benefits of hot implants. The dark current density of Si implanted diodes was found to be 0.32 Acm^{-2} at -0.5 V at room temperature which is significantly lower than that of the Be implanted diodes with a dark current density of 1 Acm^{-2} at -0.5 V . Therefore diffusion current generated from the P-type region is still expected to dominate the dark current of the lateral APDs.

6.4 Si implantation profiles as measured by SIMS

The Si doping profile was measured using SIMS with the results plotted in Figure 6.6. The similarity between the unannealed sample implanted at 30 $^{\circ}\text{C}$ and the sample implanted at

200 °C and annealed at 550 °C shows that diffusion of Si upon annealing is negligible. This is expected as Si is reported to have a very low diffusion coefficient in InAs. However, a large discrepancy was observed between the SIMS results and the simulated doping profile calculated using TRIM. After discussion with the SIMS specialists, the origin of the long diffusion tail is likely to be caused by a SIMS calibration error, or contamination of the instrument after previously measuring a Si sample.

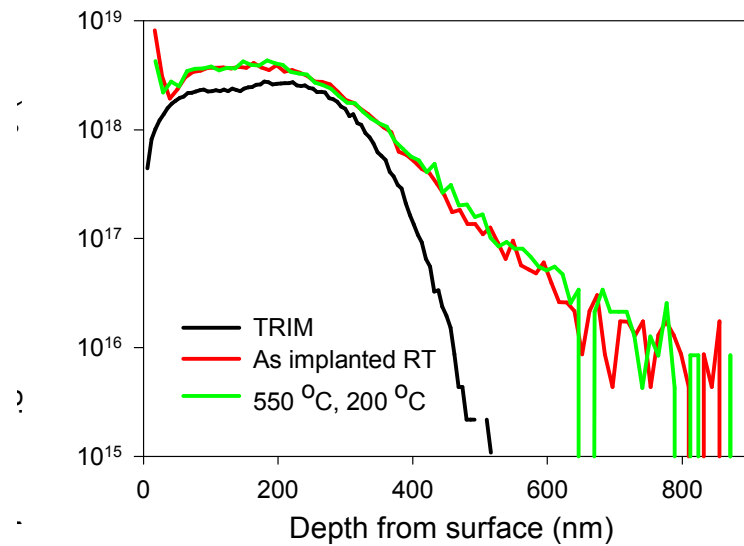


Figure 6.6: The concentration of Si implanted into InAs as simulated using TRIM. The Si concentration profiles as measured by SIMS are also plotted as implanted at room temperature and implanted at 200 °C and annealed at 550 °C

6.5 Lateral APD design

The growth and fabrication challenges of developing high gain InAs APDs are unusual as most APDs utilise a thin avalanche region to exploit the dead space effect to reduce excess noise and to achieve higher gain at a given bias voltage. Consequently there have been few reports of APDs adopting a lateral structure as thin avalanche regions can be epitaxially grown. Although developed to solve different challenges, a lateral structure referred to as high-density vertically interconnected photodiode (HDVIP) [7] is utilised in HgCdTe. A schematic diagram of the lateral multiplication region in a HDVIP structure is shown in Figure 6.7 [8]. Very high lateral gain with low excess noise has been measured from the HDVIP structure, and due to the similarities in the electronic properties of InAs and HgCdTe, the success of the HDVIP structure is encouraging for the lateral InAs APD concept. The HDVIP structure is fabricated using ion milling to produce a parallel plane P-N junction across the wafer surface as shown in Figure 6.7. Furthermore, the substrate is

removed to connect the via to readout electronics [7]. Although this fabrication procedure could be developed for InAs, it is highly complex. A lateral electric field region could simply be formed between P and N-type regions formed in the surface of the wafer, similar to the electron transport mechanism between a source and drain in a field effect transistor (FET), but under significantly larger electric fields.

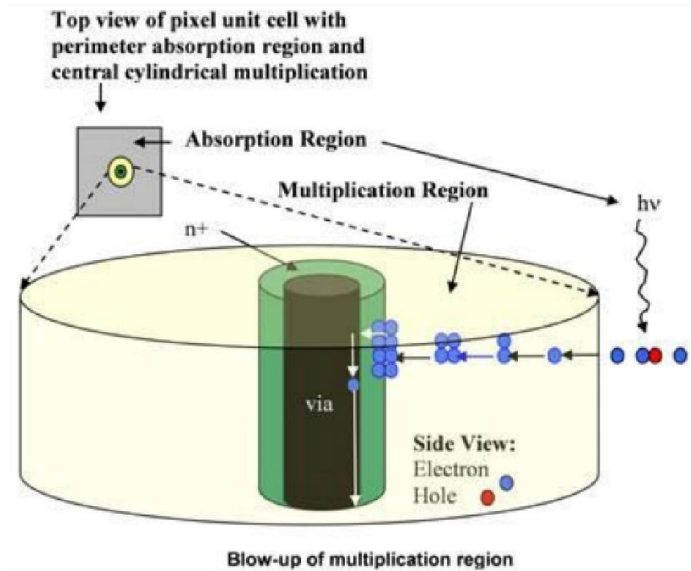


Figure 6.7: Schematic diagram of the lateral multiplication in a HgCdTe HDVIP [7].

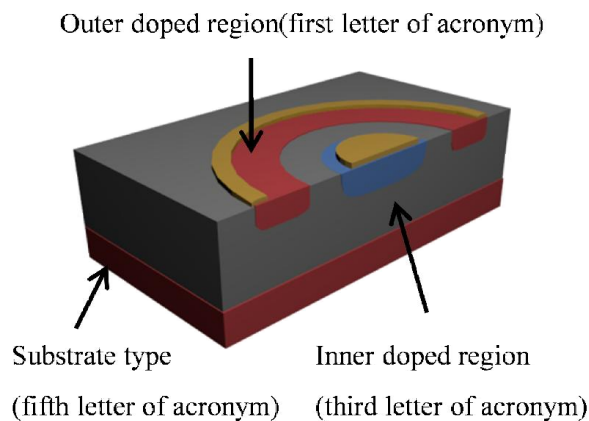


Figure 6.8: A schematic diagram of a cross section of a lateral InAs APD with labelled doped regions.

Simulations were carried out to aid the design of lateral structures. The multiplication region requires low background doping, and therefore surface doped P and N-type regions are formed in epitaxially grown material. The interface between the intrinsic epitaxially grown region and the substrate was anticipated to have a high defect density and therefore the depletion region was confined to the epi layer. A doped layer was utilised underneath the

intrinsic layer to confine the depletion region vertically, but enabling it to grow laterally between the surface P and N-type region. To mitigate the formation of electric field hotspots the lateral APD structures were based upon a cylindrical geometry. Therefore four configurations of lateral APDs are possible with the doping type of outer and inner surface regions in addition to the substrate type. Acronyms have been created for the different configurations as shown by the schematic diagram in Figure 6.8 and table 1 respectively.

Table 6.1: The peak electric field of various lateral APD structures at -10 V.

Structure	Acronym	Electric Field (kVcm ⁻¹)
N-type outer region Around a P-type inner region On a N-type substrate	NAPON	80
P-type outer region Around a N-type inner region On a N-type substrate	PANON	74
N-type outer region Around a P-type inner region On a P-type substrate	NAPOP	76
P-type outer region Around a N-type inner region On a P-type substrate	PANOP	59

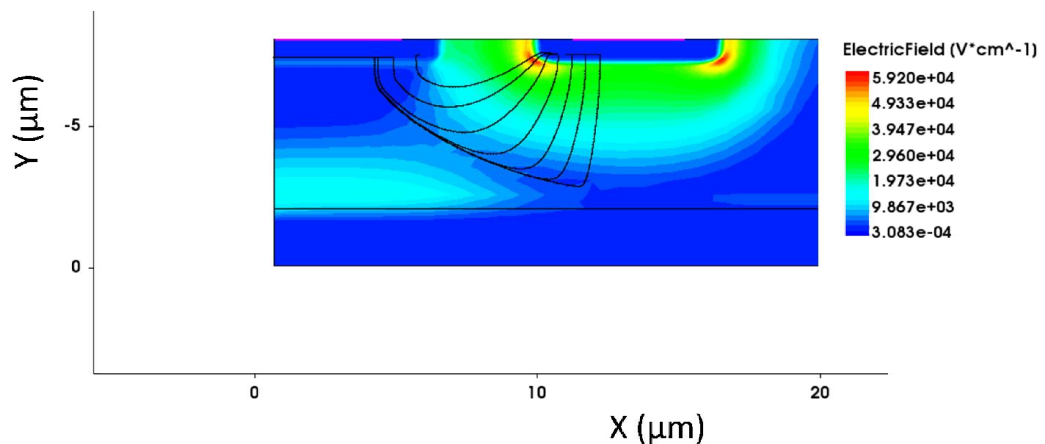


Figure 6.9: The electric field of half a cross section of a PANOP APD at -10 V reverse bias. The surface P-type region is 1 μm deep.

The intrinsic region thickness was 6 μm with a background doping of $5 \times 10^{14} \text{ cm}^{-3}$. A 5 μm lateral intrinsic region width was simulated between the inner and outer surface P and N-type regions. The depth of the P and N-type regions was 1 μm and matched the as implanted doping profile of the Be and Si implantation. Electric field simulations of the four simple lateral APD configurations were carried out with a false colour cross section of the electric field of the PANOP structure at -10 V is shown in Figure 6.9. Streamlines have been added to the electric field plot simulation of the PANOP structure in Figure 6.9 to approximately show the path taken by the avalanche pulse for various optical injection positions. The streamlines are plotted 1 μm deep within the surface P-type region and are spaced 500 nm apart beginning at the junction edge. Details of the simulations can be found in appendix 8.5. A significant lateral electric field was developed in structures with a P-type substrate (PANOP and NAPOP) with the streamlines showing most carriers take a lateral path as seen in Figure 6.10. Streamlines of structures with an N-type substrate (NAPON and PANON) flowed vertically through the junction and into the N-type substrate before reaching the contact. This is explained as the background doping type of the intrinsic region is N-type and therefore for structures with an N-type substrate, the lowest resistance path is provided by the substrate. However, an electric field forms between the P-type substrate and the intrinsic region which is slightly N-type. The electric field repels electrons and channels carriers towards the N-type surface contact as shown by the streamlines in Figure 6.9.

The peak electric field of each structure at -10 V reverse bias is shown in Table 6.1. The peak electric field was formed at a hotspot in all structures, however, the magnitude of the electric field was significantly lower in the PANOP structure. The P-type substrate and the outer P-type surface region in the PANOP structure worked to prevent the depletion region from pinching near the junction periphery, and thus reduce the severity of the hotspot. Therefore the PANOP structure is expected to show the largest breakdown voltage and also the most significant lateral gain. Simulations of the hotspot evolution in other structures were found to behave in a similar manner to the simulated traditional planar diodes and therefore may benefit from a guard ring or other electric field protection to prevent premature breakdown. However, diffusion of the P-type doping profile, as caused by annealing, is expected to reduce the severity of the hotspot by increasing the curvature of the junction. The path length for each streamline for the PANOP structure in Figure 6.9 differs significantly as does the magnitude of the electric field along the path. Furthermore electrons injected near the junction periphery will pass through the hotspot. Thus, the gain of the lateral APD is expected to vary significantly with injection position generating an uneven profile and generating significant excess noise. The electric field non-uniformities can be

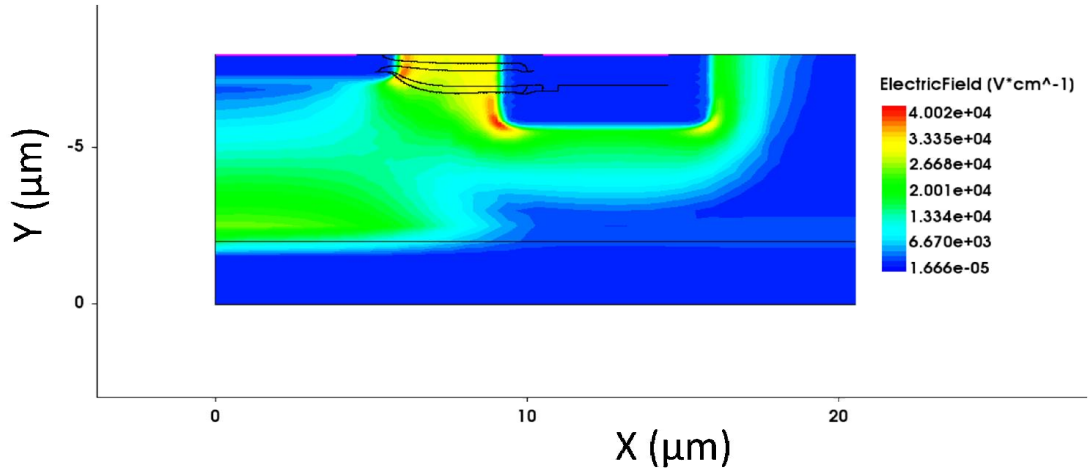


Figure 6.10: The electric field of half a cross section of a PANOP APD at -10 V reverse bias. The surface P-type regions is 2.5 μm deep.

reduced by increasing the depth of the surface P-type region as shown in Figure 6.10. The severity of the hotspots at the junction periphery are reduced from 59.2 to 40 kVcm^{-1} as the radius of the junction has been increased from 1 to 2.5 μm . Furthermore, by increasing the depth of the surface P-type region, the position of the hotspot is moved deeper into the device and away from the path of the photo generated carriers as shown by the streamlines. Most carriers in Figure 6.10 take a lateral path compared to Figure 6.9 as the longer vertical diffusion length and lower electric field encourages carriers to migrate laterally through the P-type region.

The lateral electric field across the PANOP APD with a lateral intrinsic region of 5 μm is plotted in Figure 6.11 at a depth of 0.5 μm at -10 V. The lateral depletion region is limited by the relatively small lateral intrinsic region width between surface P and N-type regions. Consequently tunnelling current will dominate at large reverse bias voltages before significant gain can develop. The lateral depletion width and thus the gain can be increased by increasing the lateral intrinsic region. The lateral electric field across a PANOP APD with a lateral intrinsic region width of 10 μm is plotted in Figure 6.11. As shown the depletion width is significantly increased by increasing the lateral separation between the surface contacts while the vertical thickness of the epitaxial grown layer remains unchanged. At -10 V the 10 μm lateral intrinsic region is fully depleted, however, significantly larger depletion regions can be achieved by increasing the separation distance of the surface contacts.

A strong electric field can be developed in the PANOP structure. Such a structure could be used to mitigate the requirement of thick epitaxial regions to achieve high gain in InAs

APDs as a lateral depletion width of 10 μm was achieved at 10 V within a structure with a 5 μm thick intrinsic epitaxial layer. The simulated depletion region width is significantly larger currently achieved from an InAs APD and has the potential to be significantly increased by simply increasing the separation distance of the surface doped regions. Furthermore the peak electric field was slightly reduced when increasing the lateral intrinsic region thickness.

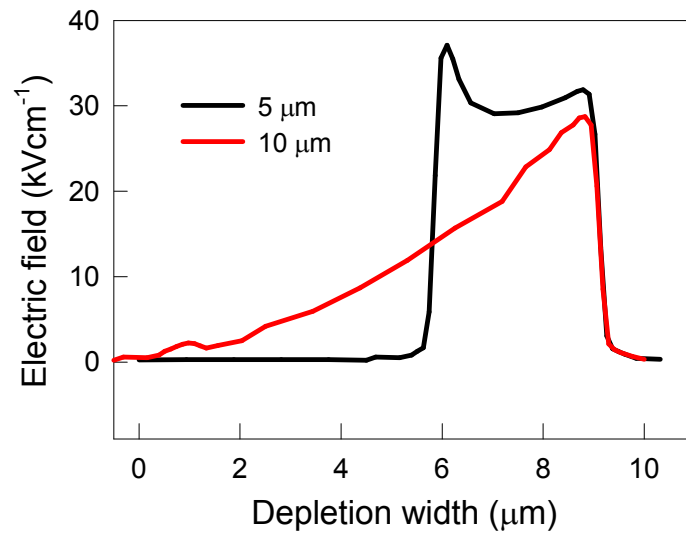


Figure 6.11: The lateral electric field across PANOP APDs with lateral intrinsic region thicknesses of 5 and 10 μm at -10 V reverse bias.

6.6 Fabrication of lateral InAs APDs

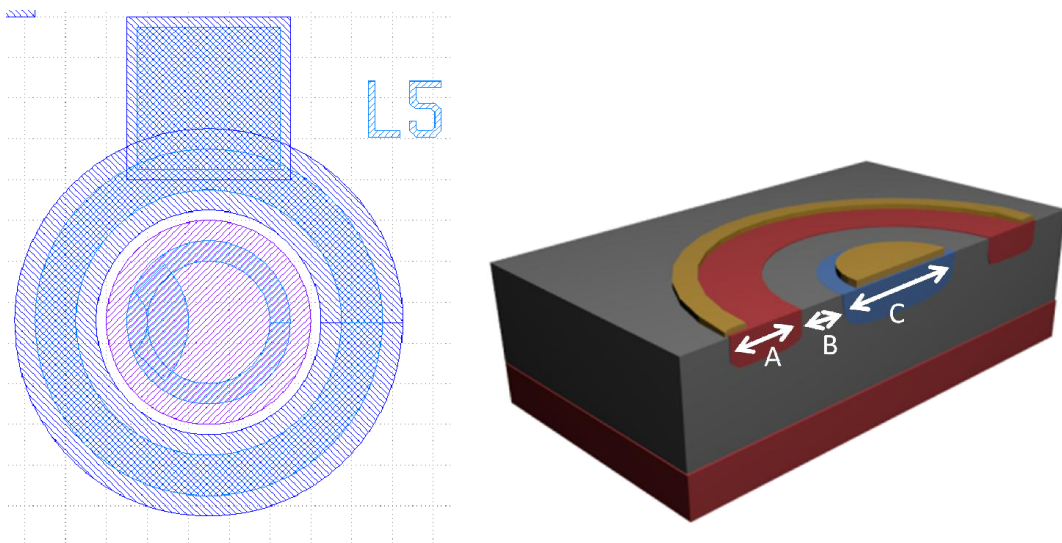


Figure 6.12: A schematic diagram of a lateral APDs. *A* is the outer ring thickness, *B* is the lateral intrinsic region thickness and *C* is the diameter of the central region.

The lateral APDs were based upon a cylindrical geometry to mitigate the formation of electric field hotspots and a new mask was designed to fabricate the lateral APDs. A stacked schematic diagram of the mask layers used to form the P and N-type surface doping and the contact metal are shown in Figure 6.12. A schematic diagram of a cross section of a lateral APD is also shown in Figure 6.12. The width of the surface ring doped region (A) was fixed at $40\ \mu\text{m}$ in all structures. Devices had lateral intrinsic region widths (B) of 5, 10 and $15\ \mu\text{m}$ and central region diameters (C) of 50, 100, 200 and $400\ \mu\text{m}$. All four variations of the doping configurations were fabricated. PANON and NAPON structures were fabricated from InAs14 which was an epitaxially grown P-i-N wafer with layer thicknesses of 2-6-1.5 μm . Before implantation, $3\ \mu\text{m}$ was etched from the surface of the wafer to remove the P-type region. PANOP and NAPOP were fabricated from InAs15 which was an epitaxially grown N-i-P wafer with layer thicknesses of 2-4-2 μm . Before implantation, $2.5\ \mu\text{m}$ was etched from the surface of the wafer to remove the N-type region. Unfortunately the PECVD had developed a serious fault requiring a new part with a long lead time. As sending the sample to another institution for deposition would contaminate the surface, the fabrication was carried out without the surface protection layer

All four samples had alignment marks deposited before being masked for Be implantation to form the P-type regions. The implant conditions were $1 \times 10^{14}\ \text{cm}^{-2}$ at 200 keV and $3.8 \times 10^{13}\ \text{cm}^{-2}$ at 70 keV producing a flat doping profile to 700 nm and is the same conditions used to fabricate the planar APDs. After implantation the mask was removed ECK830 heated to $100\ ^\circ\text{C}$ before being masked again for Si implantation to form the surface N-type regions. The implant conditions were $6.5 \times 10^{13}\ \text{cm}^{-2}$ at 190 keV and $1 \times 10^{13}\ \text{cm}^{-2}$ at 60 keV producing a flat doping profile to a depth of 300 nm and is the same conditions used in the Si implant study, the implant temperature was $30\ ^\circ\text{C}$. After two round trips to implant facilities, the PECVD had been repaired and 30 nm of SiO_2 was applied before the samples were annealed at $550\ ^\circ\text{C}$ for 30 s to activate the Be and Si. The anneal has been shown to cause significant diffusion of the Be doping profile with the junction forming $2.5\ \mu\text{m}$ deep. The Si doping profile shows negligible diffusion through annealing. The SiO_2 layer was removed in a buffered HF acid etch for 30 s before Ti/Au 20/200 nm thick contacts were deposited on both surface doped regions and the substrate. A picture of fabricated devices is shown in Figure 6.13.

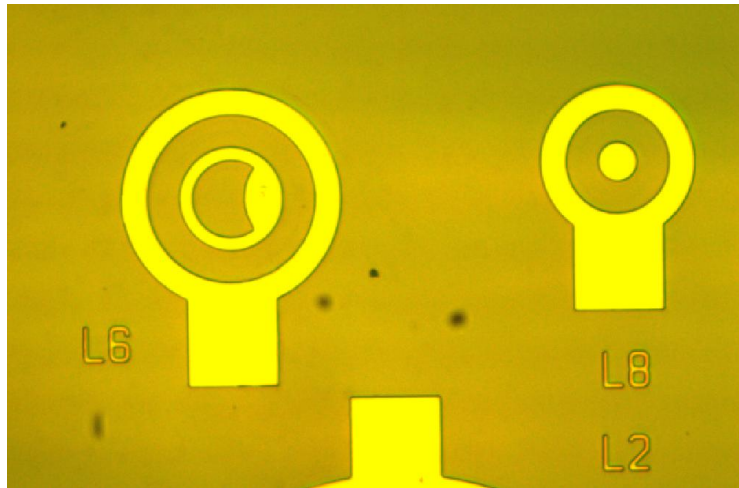


Figure 6.13: A picture of fabricated lateral InAs APDs.

6.7 I-V characteristics of lateral APDs

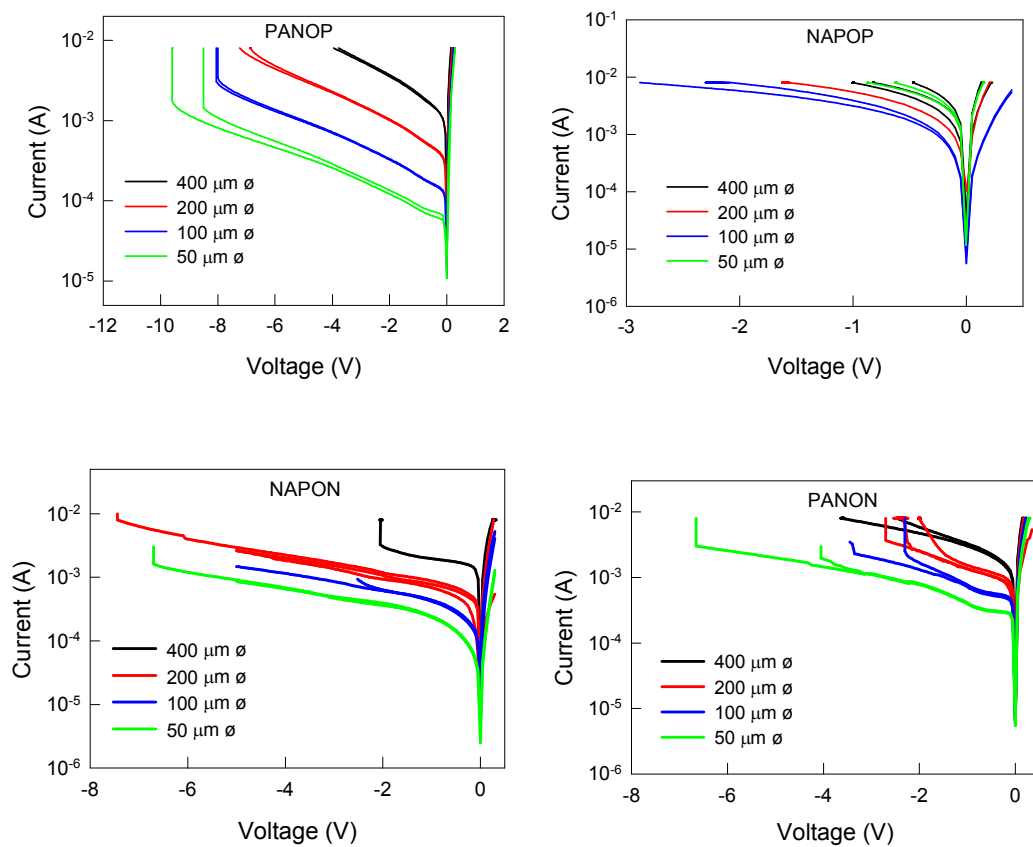


Figure 6.14: I-V characteristics of lateral APD structures with a 5 μm lateral intrinsic region width. The diameter refers to the central region.

The I-V characteristics of lateral APD structures with a 5 μm wide lateral intrinsic region are shown in Figure 6.14. The non-uniform I-V characteristics and high dark current measured in

some structures is indicative of high surface leakage. This is perhaps not too surprising as the surface protection layer could not be used. Attempts were made to reduce the surface leakage by utilising finishing etches of 30 s in buffered HF acid and 5 s in $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ in a ratio of 1:8:80, however, all were unsuccessful. The I-V characteristics of the PANOP structure were most uniform, showed the lowest dark current and also achieved the largest reverse bias voltage before breakdown. (Breakdown could only be measured on the smallest devices at room temperature due to current compliance limitations). Simulation results showed that the PANOP structure contained the lowest peak electric field for a given bias voltage of any of the lateral APD structures in addition to the planar APDs from chapter 4. The low peak electric field is likely to reduce both bulk and surface leakage currents and therefore I-V measurements corroborate with simulation results.

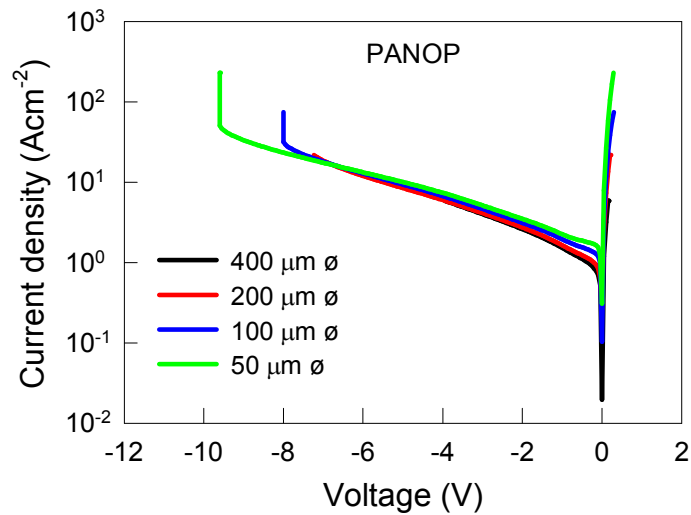


Figure 6.15: The J-V characteristics of PANOP APDs.

As discussed in section 6.3, the I-V characteristics of the lateral APDs is expected to be dominated by diffusion current from the P-type region. The diffusion current in the PANOP structure will receive contributions from the epitaxially grown P-type substrate in addition to the Be implanted surface P-type region. Characterisation of InAs15 before the P-type region was etched away revealed that the diffusion limited dark current density of the epitaxially grown P-type was 0.8 Acm^{-2} at 0.5 V. It is expected that the surface area over which diffusion current from the epitaxially grown P-type region is received is equal to the area of the central implanted surface region in addition to the lateral intrinsic region width. The surface area over which diffusion from the implanted P-type region is contributed is expected to equal to surface area of the nearest edge of the implanted ring region. Furthermore the magnitude of diffusion current from the implanted P-type region is 1 A cm^{-2} . As the current density expected from both P-type regions is similar, the dark current

density of PANOP APDs is expected to scale well with the total P-type surface area as shown in Figure 6.15. The good fit confirms that the dark current is generated as expected and the surface leakage is low.

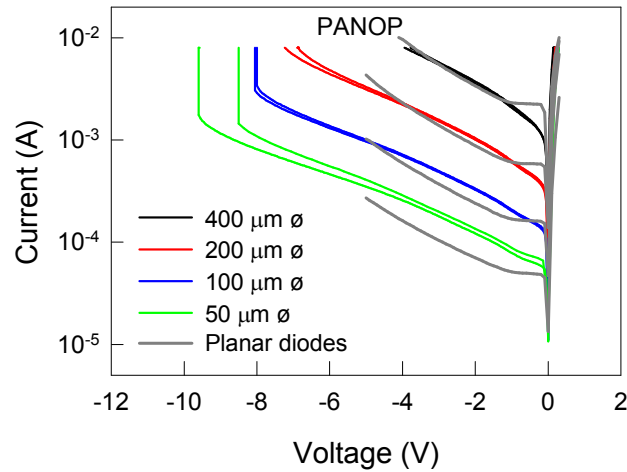


Figure 6.16: The I-V characteristics of PANOP APDs and planar APDs developed in chapter 3.

The dark current generated from the P-type region within planar APDs developed in chapter 3 had a distinctive I-V characteristics with the dark current increasing at the same rate as the gain as plotted in Figure 6.16. The dark current of the planar APDs across the voltage range from 0 and -0.5 V is constant as it is dominated by diffusion current and there is no avalanche gain. However, the dark current of the PANOP APDs do not share this similar characteristic with an exponentially increasing dark current from 0.1 V as plotted in Figure 6.16. As such the current leakage mechanism of the lateral APDs differs compared to planar APDs. To further investigate the current leakage mechanism, the lateral APD structures also had back contacts deposited. The I-V characteristics of the PANOP structure remained unchanged if measured between the central region and the back contact compared to the two surface contacts. However, the NAPON structure showed lower dark current when measuring the I-V characteristics between the surface contacts compared to when measuring between the middle contact and the back contact as shown in Figure 6.17. It is speculated that when measuring the I-V characterises between the surface contacts of the NAPON structure, carriers from the central P-type junction cannot diffuse the distance through the implanted P-type region to be collected by the N-type ring contact. However, when measured between the central and the back contact, carriers from the P-type region must only diffuse a short vertical distance before being collected by the N-type substrate.

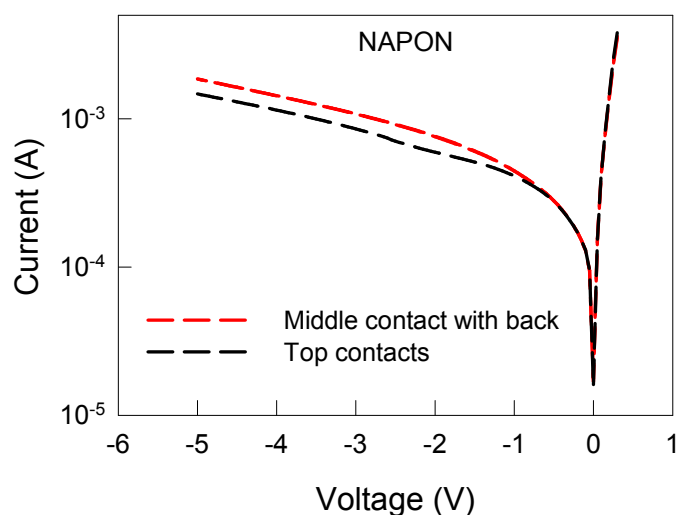


Figure 6.17: The I-V characteristics of a NAPON APD with a central diameter of 100 μm as measured between the top contacts and the middle surface contact and the back contact.

The I-V characteristics of PANOP structures with lateral intrinsic region thicknesses of 5, 10 and 15 μm are shown in Figure 6.18. The thicker lateral intrinsic region is expected to develop higher gain. It is interesting to note that thickness of the lateral intrinsic region width does not significantly affect the magnitude of the dark current at low reverse bias voltages. However, PANOP APDs with thicker intrinsic region widths consistently displayed a larger breakdown voltage. The breakdown mechanism of planar APDs was found to be due to a thermal runaway effect within an electric field hotspot. Without including the effects of Be diffusion, simulations presented in section 5.6 showed that the peak electric field in a planar structure at -10 V is 70 kVcm^{-1} while the peak electric field in the PANOP APD with a 5 μm lateral thickness is 40 kVcm^{-1} as show in section 6.5. Furthermore the peak electric field in the PANOP structure is found to reduce with increasing lateral intrinsic region thickness. The I-V results therefore agree well with simulation results. .

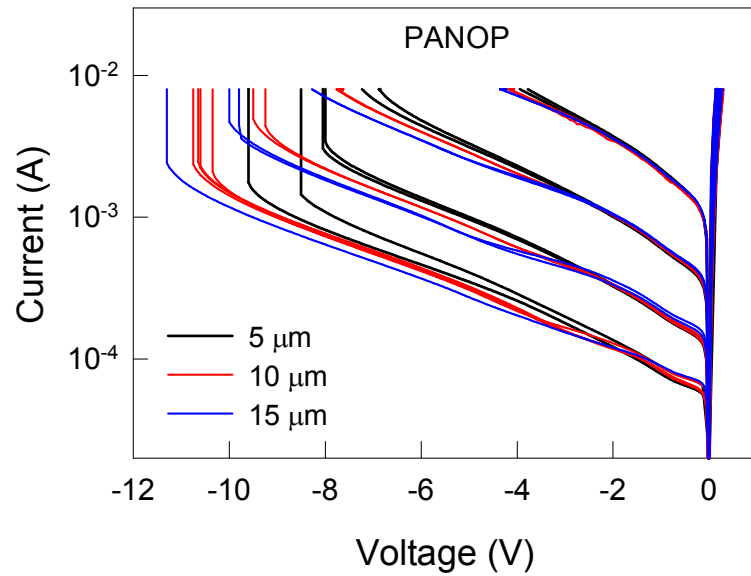


Figure 6.18: The I-V characteristics of PANOP APDs with lateral intrinsic region thicknesses of 5, 10 and 15 μm .

6.8 Responsivity of lateral APDs

The responsivity of the four lateral APD structures were measured at -0.3 V at room temperature using a 1550 nm and phase sensitive detection with a fundamental frequency of 270 Hz. The responsivity was found to be a strong function of position across the structures and responsivity line scans are shown in Figure 6.19 on devices with a central region diameter of 400 μm and a 5 μm lateral region width. The size of the optical spot was $\approx 20 \mu\text{m}$ in diameter and limited resolution.

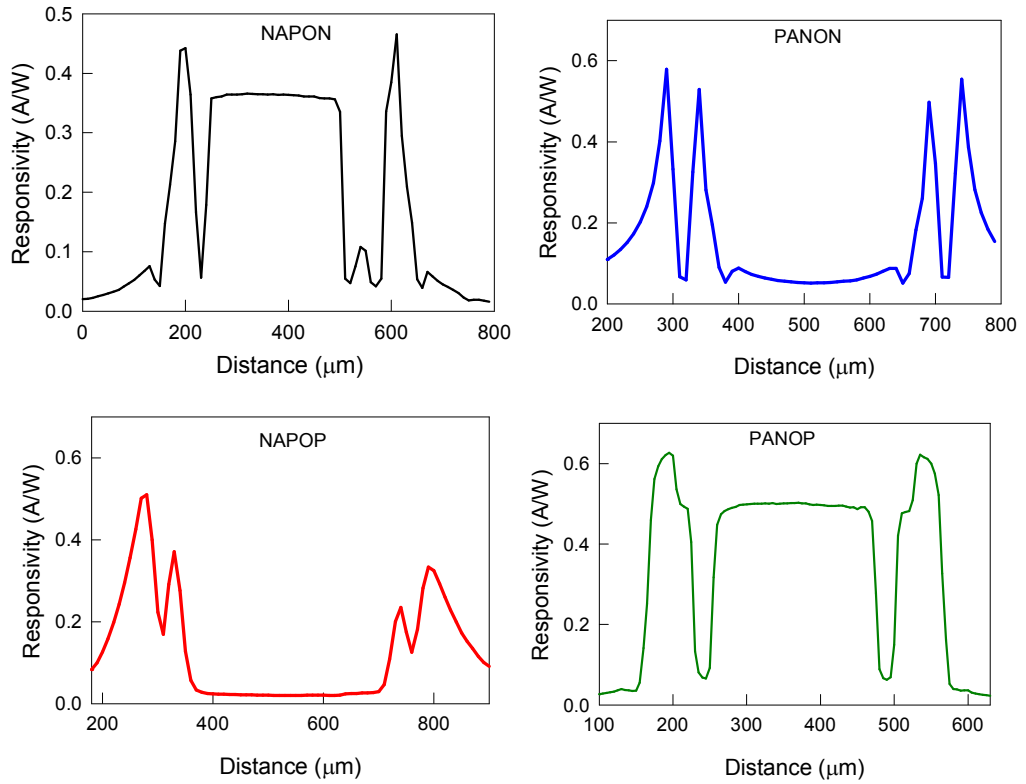


Figure 6.19: Responsivity line scans across the centre of lateral APDs at -0.3 V using a 1550 nm laser.

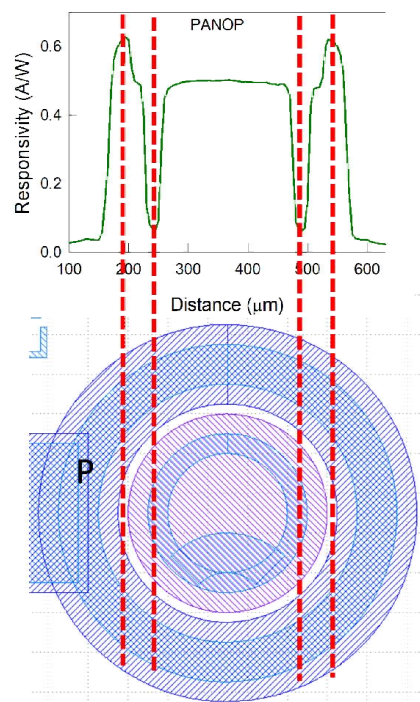


Figure 6.20: A responsivity line scan and a schematic diagram of a PANOP APD.

In all structures, the largest responsivity was measured when the optical spot was positioned over the intrinsic region as carriers are readily separated in the electric field. The low regions of responsivity coincide with the optical spot aligned with the metal contact. A schematic diagram has been aligned with a responsivity line scan from a PANOP structure in Figure 6.20 to aid understanding. When operating as an APD the highest gain and lowest excess noise is achieved using pure optical injection into the P-type region. The NAPON and PANON structure showed high responsivity across the P-type region. However, simulations indicated that structures with a N-type substrate develop strong vertical electric field and negligible lateral electric field. The flat responsivity profile across the central region of the NAPON structure is similar to the responsivity profile across a planar APD as show in Figure 5.6. Therefore the NAPON structure behaves like a planar P-i-N diode, except with surface N-type contacts. A similar argument hold for the PANON structure, except the vertical electric field is developed between the surface P-type ring region. A lateral electric field is expected to be developed on devices with a P-type substrate. Within the NAPOP structure, the responsivity across the central P-type region is poor. An electric field is not developed between the central P-type region and the substrate and so carriers are required to diffuse laterally through the intrinsic before being collected. As the diffusion length is much shorter than the radius of the central implant, the responsivity is poor. This effect is only observed using optical injection into the outer ring of the PANOP structure. The responsivity of the PANOP structure on the near side of the ring is high indicating that the injected carrier diffuse through the P-type region before reaching the depletion region edge and are transported in the lateral electric field to the N-type central contact. This result is highly encouraging and provides evidence for lateral carrier transport.

6.9 Gain of lateral APDs

Measurements of the gain were performed using a 523 nm laser as over 99% of the photons are absorbed within 300 nm ensuring pure injection. Phase sensitive detection was used to perform the measurements chopped at a frequency of 270 Hz. A photograph of the optical spot used to perform the gain measurements is shown in Figure 6.21 with the optical spot diameter estimated to be 20 μm . As only carriers injected at the edge of the P-type region are collected, pure injection was achieved by overlapped the optical spot onto the contact meal. The gain from PANOP APDs with a 5 μm lateral intrinsic region thickness is shown in Figure 6.21 along with a schematic diagram of the relative size and position of the optical spot. The largest gain was achieved using pure injection as confirmed by two positions

across the device. The gain for a given bias voltage was reduced as the optical injection became increasingly mixed as expected.

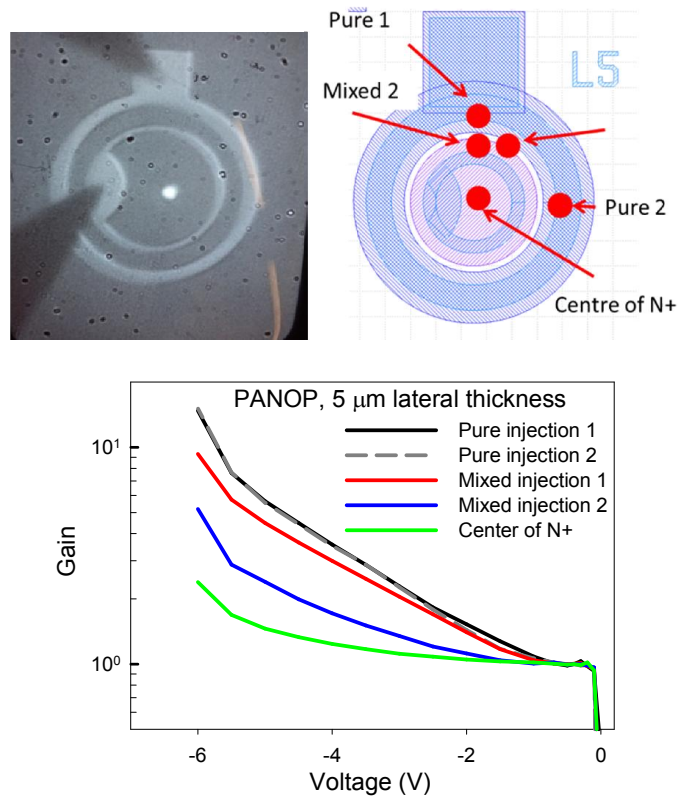


Figure 6.21: A photograph of the optical spot used to measure the gain on PANOP APDs. A schematic diagram of the relative size and position of the optical spot used to perform gain measurements. The gain vs. voltage characteristics of lateral APDs with a lateral intrinsic region thickness of 5 μm using a 523 nm laser is also shown.

The gain characteristic of a 2.1 μm thick mesa APD [9] are plotted in Figure 6.22 for comparison against the gain characteristics of the lateral APD under pure injection. The vertical intrinsic region thickness of the lateral APD is $\approx 2 \mu\text{m}$ underneath the P-type region while the lateral intrinsic region thickness $\approx 5 \mu\text{m}$. The gain from an InAs APD is given by $\exp(\alpha w)$, and similarity between the gain characteristics of the mesa and lateral APD up to -2.5 V is because over this region, the mesa is not fully depleted. However, at -2.5 V the intrinsic region is fully depleted, thus w becomes a constant, and the gain characteristics doubles over due to the significant lower rate of increase. Although the lateral APD shares the same vertical intrinsic region width of the mesa APD, the gain characteristics do not bend over, and instead continues to increase rapidly. This indicates that the depletion region width is still increasing in the direction of the avalanche gain. By comparison we have established that this continuation is not due to an increase of depletion region width in the

vertical direction, therefore the higher gain measured in the lateral APD is strong evidence for enhanced lateral gain from the PANOP structure.

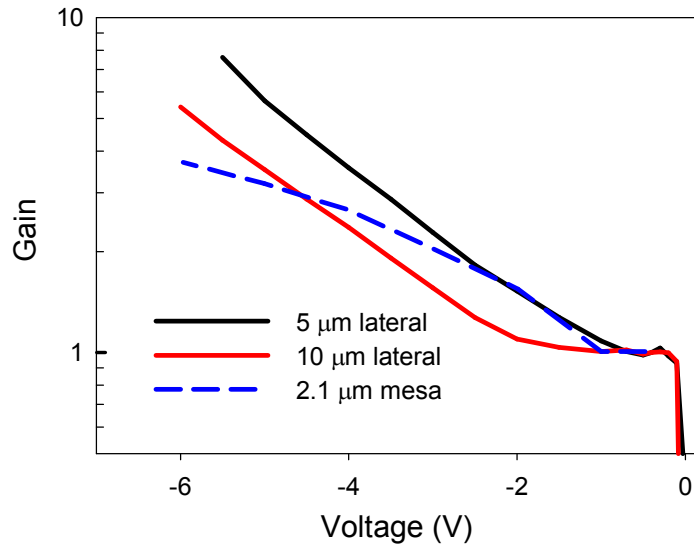


Figure 6.22: The gain of PANOP APDs with lateral intrinsic region thicknesses of 5 and 10 μm . The gain of a mesa APD with an intrinsic region of 2.1 μm is also shown [8].

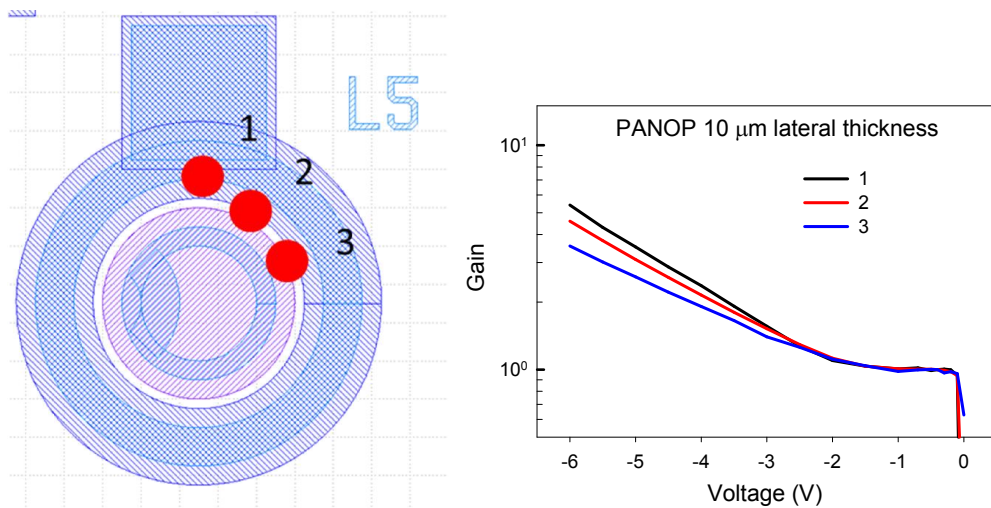


Figure 6.23: A schematic diagram of the relative size and position of the optical spot used to perform gain measurements in addition to the gain characteristics of PANOP APDs with a lateral intrinsic region thickness of 10 μm using a 523 nm laser

A schematic diagram of a PANOP APD with a 10 μm lateral intrinsic region thickness and the position of the optical spot used for gain measurements is shown in Figure 6.23. The gain from pure injection was not found to be significant until - 2 V, and consequently, the

gain at a given bias voltage was lower compared to the lateral structure with 5 μm lateral intrinsic region thickness, as shown in Figure 6.22. Lower gain in a thicker InAs APD was also observed in the gain characteristics of planar APDs from InAs10 and InAs11 as discussed in section 5.4. The larger gain from the thinner structure at low electric fields was attributed to the rapid increase of α with electric fields at $\approx 20 \text{ kVcm}^{-1}$. This effect becomes increasingly pronounced in InAs APDs with very wide depletion regions and low background doping. To further investigate this effect, the lateral electric field across PANOP APDs with 5 and 10 μm wide intrinsic regions was simulated and plotted in Figure 6.24 at reverse bias voltages of 2, 5, 10 and 20 V. The electron impact ionisation coefficient of InAs develops rapidly at $\approx 20 \text{ kVcm}^{-1}$, and the restricted depletion region of the 5 μm structure forces a larger proportion of the avalanche region over this electric field threshold for a given bias voltage. While the electric field of the 5 μm structure is represented by a trapezium, the electric field of the 10 μm structure shows a larger gradient, and at low bias voltages only a relatively small length of the multiplication region is above 20 kVcm^{-1} . Consequently at lower voltages, the gain from the 5 μm PANOP APD exceeds that of the 10 μm structure. However, at a reverse bias of 20 V, the comparison of the electric field profiles shows that a significantly longer region of the 10 μm structure is above 20 kVcm^{-1} , and therefore the 10 μm structure is anticipated to achieve a larger gain. Therefore the benefits of the wider lateral depletion region may only be apparent at higher gains as it prevents the bending over of the gain characteristics. However, gain measurements were limited to -6 V at room temperature due to current compliance limitations. The optical spot in the low temperature probe station cannot be positioned with the accuracy required to perform gain measurements on the PANOP APD.

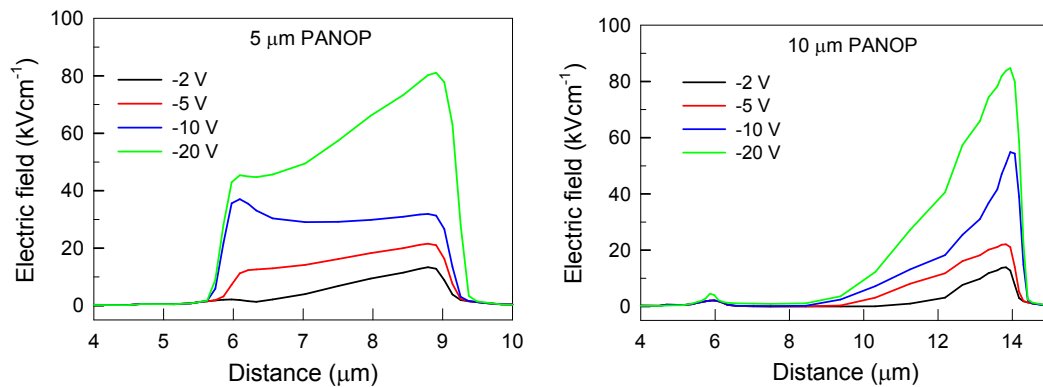


Figure 6.24: The simulated lateral electric field across PANOP structures with 5 (left) and 10 μm (right) lateral intrinsic region thicknesses at reverse bias voltages of 2, 5, 10 and 20 V.

6.10 Conclusion

Si implantation has been developed for selective n-type doping in InAs. Hot implants at 200 °C are effective at reducing the implant damage, however, excellent recovery can also be achieved through annealing at temperatures of 500 °C. The dark current density of mesa diodes fabricated using Si ion implantation and annealed at 500 °C were 0.32 Acm^{-2} at -0.5 V at room temperature. An APD with a lateral multiplication region was proposed to enable high gain to be achieved from InAs APDs with a relatively thin epitaxially grown layer. Si and Be ion implantation were utilised to fabricate lateral APDs with a range of doping configurations. A device with a P-type implanted ring around a N-type central contact on a P-type substrate, termed PANOP, was simulated to show the lowest electric field for a given voltage compared to a range of lateral devices, and also the planar APDs discussed in chapter 5. The I-V characteristics of PANOP APDs corroborated with simulation results and achieved a significantly larger reverse bias voltage before breakdown, with a positive correlation between the lateral separation distance and the breakdown voltage. A significantly larger gain from a PANOP APD was achieved at a given bias compared to a mesa APD with a similar vertical intrinsic region thickness. The enhanced gain confirms that a significantly wider multiplication with a lateral electric field had been achieved from the PANOP structure.

6.11 References

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7 Conclusion and future work

InAs is an extremely promising semiconductor for use as the multiplication region of APDs, however, the InAs surface is poorly understood and highly susceptible to surface leakage. The wet chemical etching recipe developed by A. Marshall et.al has enabled the impact ionisation coefficients in InAs to be studied [1]. However, highly uniform and repeatable growth and fabrication procedures are required to exploit InAs APDs for practical applications. The planar fabrication process is without etching and allows for the use of heterojunctions to bury the sensitive narrow bandgap layers. A highly uniform planar fabrication process was developed to solve such issues. A planar junction is typically fabricated after the growth using selective area doping Zn diffusion or ion implantation, however, such doping techniques are very poorly developed for InAs. Zn diffusion is thought to be unsuitable for InAs APDs adopting a P-i-N structure as optical absorption is required to be within the P-type region to suppress excess noise. Zn diffusion has very poor dopant control, and doping near the saturation limit causes a small minority carrier diffusion length and thus, poor responsivity. Ion implantation allows for superior control over dopant placement.

There has been little prior work on ion implantation for P-type doping InAs. N. N. Gerasimenko had reported the unsuitability of Mg implantation for P-type doping InAs due to the high defect density cancelling out the acceptor like properties of InAs [2]. In this work Be implantation and annealing are developed for selective area P-type doping in InAs. Be implantation was simulated to produce 3.7 times less interstitial defects in InAs compared to Mg. Furthermore the Be implant damage is concentrated locally due to its light mass and thus, low nuclear ion energy loss and short recoil cascade length, and therefore more easily recoverable through annealing. The implant conditions were evaluated through observations of the I-V characteristics of diodes. The implant damage and activation of Be is very low if not annealed. RTA at a temperature of 550 °C for 30 s provided the optimum conditions in terms of producing the lowest dark current of 1 Acm⁻² in mesa diodes and preserving the as-implanted Be profile. Higher annealing temperatures did not reduce the dark current further and only caused significant Be diffusion. Implants carried out at RT were found to be just as effective as hot implants.

A planar fabrication procedure utilising optimised Be implantation and annealing conditions was developed. A 30 nm protective layer of SiO₂ proved to be critical for achieving low surface leakage in the planar diodes. The SiO₂ protective layer acted to protect the InAs

surface from contamination and damage during fabrication. SU-8 passivation was utilised to lock in the surface conditions after the protective surface layer was removed. Remote bond pads and AR coating were utilised to increase robustness and responsivity of the photodiodes. Planar photodiodes were fabricated with low surface leakage and were characterised with a detectivity of $6.08 \times 10^8 \text{ cmHz}^{-1/2}\text{W}^{-1}$ at 1550 nm at room temperature.

The Be implantation conditions were utilised to fabricate APDs from a wafer with low background doping and a wide intrinsic region to achieve high gain. C-V characterisation of the planar APDs revealed a low background doping of $\sim 2 \times 10^{14} \text{ cm}^{-3}$ was achieved with depletion widths as large as $\sim 8 \text{ }\mu\text{m}$. Consequently the planar APDs displayed a very high gain of 330 at -26 V at 200 K. The I-V characteristics of planar InAs APDs were characterised over a range of temperature to investigate the dominant bulk and surface leakage mechanism. The bulk leakage current was found to have activation energy of 0.42 eV and generated by a diffusion process from the P-type region of the device within the temperature range of 296 to 200 K. Over the same temperature range, surface leakage was characterised with an activation energy of 0.24 eV and generated by a generation-recombination process from the intrinsic region. The dark current of planar InAs APDs was found to be 1 Acm^{-2} at room temperature which is approximately 1 order of magnitude larger than a typical mesa APD. However, at 200 K the dark current of the mesa and planar APDs were found to be very similar at $400 \text{ }\mu\text{Acm}^{-2}$. The low background doping and low surface leakage was attributed to the benefits of the planar fabrication process.

Premature breakdown limited the maximum gain achievable from planar APD which was approximately 6 V at room temperature and 26 V at 200 K. The high inverse temperature dependence of the breakdown voltage is the opposite of most other semiconductors. Pulsed I-V measurements at 200 K were used to increase the breakdown voltage from 26 to 28 V. Dark current data logging concluded that in InAs APDs, the breakdown conditions are determined by the power dissipation density within the APD, rather than the electric field strength. The critical power dissipation density of the planar diodes was found to be 245 Wcm^{-2} at which point the unique positive dependence of the impact ionisation coefficient in InAs causes a thermal runaway effect. The breakdown of the planar APDs occurs in the hotspots due to the high carrier generation rates. APDs with guard rings were designed to mitigate the formation of electric field hotspots and an optimised structure only provided a 2 % increase in breakdown voltage. However, it should be noted that the critical power density is large and therefore it is unlikely that planar InAs APDs will be operated under such conditions.

Si implantation was investigated for selective area N-type doping in InAs. Annealing was required to fabricate InAs diodes with low leakage current, with diodes annealed at 500 °C showing a dark current density of 0.32 Acm⁻² at -0.5 V at room temperature. Hot implants were also effective at reducing the implant damage and activating the Si with mesa diodes implanted at 200 °C sharing similar I-V characteristics to diodes implanted at 30 °C and annealed at 500 °C.

Achieving higher gain from an InAs APDs while utilising a conventional mesa or planar structure, where the carriers multiply in the direction of epitaxial growth, is increasing difficult due to slow epitaxial growth rates. To circumvent this issue, lateral InAs APDs were investigated with a multiplication region parallel to the wafer surface. The thickness of the lateral structure is only required to support high optical absorption while the multiplication width can be easily altered by increasing the distance between surface doped regions. Simulations were carried out to assess the evolution of the lateral electric field within a range of lateral device designs. The doping configuration of the PANOP structure acted to reduce the formation of electric field hotspots and also developed a strong lateral electric field. A range of lateral APDs were fabricated using optimised Si and Be implantation and annealing conditions. I-V characteristics of the PANOP structure were uniform and showed a breakdown voltage greater than 8 V in a structure with an inner diameter of 50 µm. The gain from a PANOP was found to be significantly larger at a given bias compared to a traditional mesa APD with a similar epitaxially grown thickness. The larger gain provided strong evidence for enhanced lateral gain from the PANOP APD. However, significant further work on the lateral APDs is required in order to achieve higher gain.

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7.1 Future Work

The room temperature dark current of planar InAs APDs is approximately 1 order of magnitude lower than the lowest dark current reported from a mesa InAs APD at room temperature [1]. The increased dark current has been identified as originating from the P-type region and therefore likely indicative of remnant implant damage. Optimisation of the responsivity and dark current of planar APDs was unsuccessful and it is clear that a better understanding of the mechanisms determining the dark current in planar InAs APDs is required. Zn diffusion is a far less intrusive doping method compared to implantation, and Zn diffusion may be used to fabricate InAs photodiodes with low dark current at room temperature. Iwamura et. al have used Zn diffusion to fabricate InAs diodes with a dark current density of 0.45 Acm^{-2} at -0.5 V at room temperature, however, the dark current increased rapidly at voltages greater than 1 V [2]. The results of a preliminary study of the use of Zn diffusion to fabricate InAs photodiodes can be found in appendix 8.3. Zn diffused photodiodes achieved a dark current density of 0.17 Acm^{-2} at -0.5 V which is a significant improvement compared to Be implantation. However, the responsivity was found to be significantly poorer at 0.17 A/W at $1.55 \text{ }\mu\text{m}$. Zn diffusion could be a promising alternative to Be implantation, however, further work is required to characterise the Zn diffused junction.

The room temperature primary dark current of various photodiodes and APDs are plotted against the detectors cut-off wavelength in Figure 7.1. The dark current density of Hamamatsu's extended InGaAs series of photodiodes appears to follow an exponential relationship with the regression line plotted [3]. Extrapolation of the trend considerably overestimates the dark current of the planar APDs developed in this work. To the authors knowledge, there is no published dark current data for HgCdTe APDs with a cut-off wavelength of $3.5 \text{ }\mu\text{m}$ at room temperature. However, the dark current density of 2.8 and $3 \text{ }\mu\text{m}$ HgCdTe APDs is only 1-2 orders of magnitude lower than both planar and mesa InAs APDs with a considerably longer cut off wavelength [4]. This comparison highlights the potential of InAs to rival HgCdTe APDs operating around the spectral region of $3 \text{ }\mu\text{m}$. However, the dark current density of InAs was taken from a $200 \text{ }\mu\text{m}$ diameter device, while the dark current of the HgCdTe APDs were characterised from $30\text{-}30 \text{ }\mu\text{m}$ pixels within an array. Based upon the characterisation of the leakage current of planar APDs, pixel sized InAs planar APDs would have a significantly larger current density due to contribution from the surface leakage. Therefore additional effort is required to reduce the surface leakage of InAs APDs. The dark current of InAs APDs at room temperature is currently limited by diffusion current. A simple solution to eliminate both the surface leakage and diffusion

current from the P-type region would be to use a heterojunction, with the P-type region formed within a wideband gap semiconductor. Semiconductors $\text{GaAs}_{0.085}\text{Sb}_{0.915}$ and $\text{Al}_{0.49}\text{In}_{0.51}\text{As}_{0.57}\text{Sb}_{0.43}$ can be lattice mated to InAs with bandgaps of 0.7 and 1.2 eV respectively. Wide bandgap semiconductors are usually far less susceptible to surface leakage and it is anticipated that the surface leakage would also be significantly reduced adopting such a method. However, it is noted that by utilising a wide bandgap P-type layer, the infrared wavelengths would be absorbed within the intrinsic region of the APD causing an increase in excess noise and decrease in the gain.

The dark current of homojunction MWIR HgCdTe detectors is also generated by a diffusion current from P-type region at high temperatures [5], however, Teledyne HgCdTe photodiodes employ a heterojunction to eliminate the diffusion current. Rule 07 is an empirical relationship for estimating the dark current of Teledyne HgCdTe photodiodes and is also plotted in Figure 7.1 [7]. The dark current of heterojunction HgCdTe photodiodes is significantly lower than that of the current InAs APDs. However, the SRH current of InAs APD has been shown to be ≈ 2.5 orders of magnitude lower than the diffusion current at room temperature [6]. Therefore the dark current of an optimised heterojunction InAs APD, utilising a planar structure to also eliminate surface leakage, could operate with the same dark current density as current state-of-the-art HgCdTe photodiodes. If the diffusion current were eliminated, or homojunction InAs APDs operated are below temperature of 175 K, control of SRH current, thus growth conditions, becomes increasingly important.

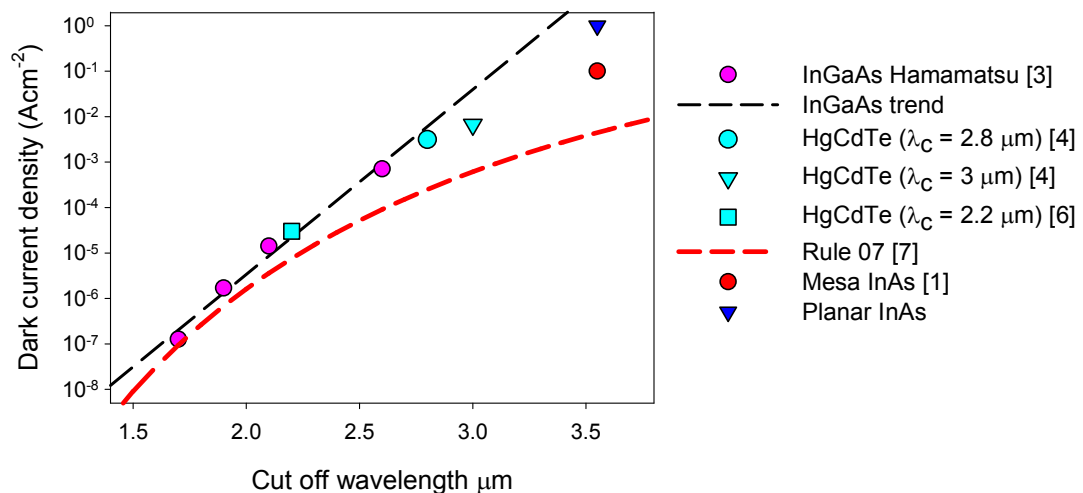


Figure 7.1: The dark current of commercial InGaAs photodiodes fabricated by Hamamatsu [3], HgCdTe APDs with cut of wavelengths of 2.2 [5], 2.8 and 3 μm [4], InAs APDs [1] and Teledyne HgCdTe photodiodes calculated using rule 07 [7].

Further work is required to characterise the lateral gain of the PANOP structure. The benefits of the lateral gain are expected to only be apparent at large gain values, however, such gain measurements could not be performed at room temperature. Low temperature gain measurements should be performed to reduce the power density so that higher gains can be measured. However, such measurements would require a redesign of the lateral APD structure as the low temperature probe station does not have the required optical injection accuracy to perform such measurements. A redesign is also necessary to improve two other key aspects of the PANOP APD. The carrier injection position needs to be reconsidered as only carriers injected a minority carrier diffusion length away from the depletion region are collected. Overcoming this issue requires the lateral APD structure to be redesigned with two possible topologies. Firstly the size of the lateral APDs could be reduced, and the lateral APDs used in an array format so that the distance between the depletion region edge of any two devices is ≈ 2 minority carrier diffusion lengths. This scheme would work well for an array, or also many single elements could be connected in parallel to form a single large area detector. An alternate design could be to use a waveguide to accurately inject carriers into the P-type region. Achieving a uniform lateral electric field may be crucial to achieving low noise, and also mitigating the formation of electric field hotspots. The PANOP structure is successful as the electric field formed between the P-type substrate and the intrinsic region that repels electrons. A highly uniform electric field could be developed using a P-type region that extends completely through the multiplication layer, and essentially forming a lateral perfect P-i-N APD. However, such a structure would require removal of the substrate, or the use of a buried insulating layer. Both of these suggestions move the lateral APD design closer to that already used in the HDVIP structure by HgCdTe.

The difficulty in achieving high gain with low excess noise is that a very wide avalanche gain region must be obtained while keeping the peak electric field below 70 kVcm^{-1} . Consequently the avalanche region in traditional APDs is limited before the peak electric field of 70 kVcm^{-1} is exceeded. While a the lateral APD relieves the stringent growth requirements of a thick structure to achieve high gain, a low background doping concentration is still required. The finite background doping of intrinsic InAs induces a significant electric field gradient across the avalanche region. The gain from a single $8 \mu\text{m}$ region in this work was limited to 330, however, to drastically increase the gain avalanche regions can be cascaded. For example by cascading 3 avalanche regions, each with a gain of 100, a total device gain of 1 million can in theory be achieved. A mesa InAs APD with two gain regions has been demonstrated [8], however, each gain region was very thin due to the use of epitaxial growth, and provided no enhancement in gain. To circumvent this issue avalanche gain regions can be cascaded laterally. A schematic diagram of a lateral cascaded

APD is shown in Figure 7.2. The Be and Si implantation techniques developed in this thesis could be used to form the doped regions of the lateral cascaded APD.

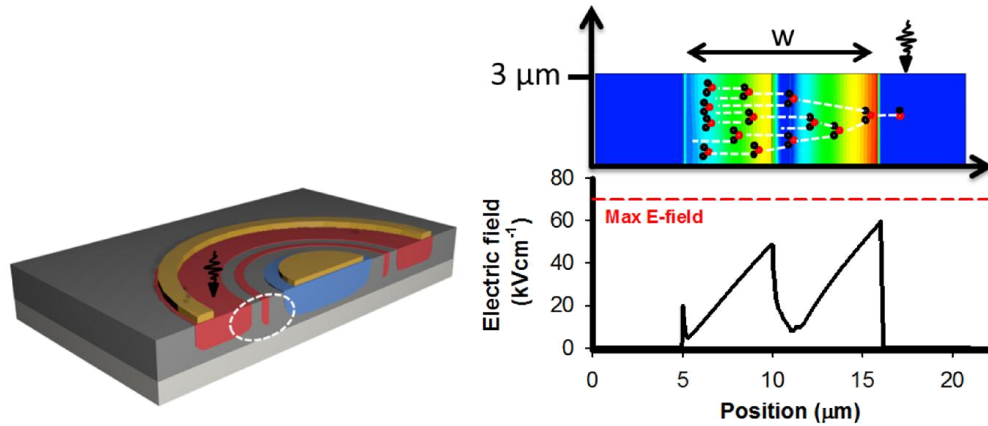


Figure 7.2: (Left) Schematic diagram of a cross section of a 2 stage lateral cascaded planar InAs APD. (Right) 2D electric field simulation of the avalanche gain region of a 2 stage lateral cascaded InAs APD. A cut of the electric field through the avalanche regions is also plotted.

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8 Appendices

8.1 Mesa fabrication procedure

Encapsulation annealing using a 30 nm of SiO₂ cap was employed throughout this study, although proximity anneals were also found to work well and produced identical results in a comparative study at 550 °C. After annealing the SiO₂ cap was removed using a buffered HF acid etch for 60 s. Ti/Au contacts with respective thicknesses of 20/200 nm were deposited onto the top and back of the samples. Circular mesa diodes of varying diameters were fabricated using a photolithographic mask of BPRS200 and wet chemical etching using H₂O:H₂O₂:HPO₃ in a ratio of 12:12:12 ml to define the mesa. The 1:1:1 etchant should be rested for 20 minutes after mixing after which the etching rate is approximately 1.1 µm per minute. However, it should be noted that the etchant can saturate quickly if etching lots of material. After being etched for approximately the correct amount of time, the depth of the mesa was measured on a Dektak profiler. It was often necessary to re-etch the mesa after measuring the height. After the correct depth had been reached (based upon an estimate) the sample was etched in H₂SO₄:H₂O₂:H₂O in a ratio of 1:8:80 ml for 30 s and rinsed in DI water. The etching mask was then removed in acetone and the sample cleaned in IPA. The sample was finally etched for 10 s in 1:1:1 and without rinsing in 1:8:80 for 15 s with a final long rinse in DI water at the end. This etching procedure has been shown to produce InAs diodes with low surface leakage current [1]. However, it was occasionally necessary to use an additional finishing etch of 30 s in buffered (10%) HF acid and a rinse in DI water.

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8.2 Wafer details

III-V national center wafer code	Reference code for this work	Comments
SF0317	InAs8	Top p doped layer etched away from an MBE grown P-i-N
MR3390	InAs10	MOCVD grown $N^- - i - N^+$ wafer with a 10 μm thick i region and a 250 nm cap
MR3387	InAs11	MOCVD grown in^+ wafer with a 6 μm thick i region.
SF0319	InAs12	Top n doped layer etched away from an MBE grown N-i-P
MR3856	InAs13	MOCVD grown in^+ wafer with a 6 μm thick i region.
MR2835	InAs14	MBE grown P-i-N wafer with layer thicknesses of 2-6-1.5 μm
SF0409	InAs15	MBE grown N-i-P wafer with layer thicknesses of 2-4-2 μm

8.3 Zn diffusion

Zn diffused planar photodiodes were prepared from wafer InAs13. The Zn diffusion was carried out at the NC and a new wafer number of MR4020 was assigned to the Zn diffused sample. Alignment marks were etched into the sample 1 μm deep. The thermal expansion coefficient for InAs is vastly different from SiN, and masks thicker than 170 nm were found to fracture when heated up to 500 $^{\circ}\text{C}$. A 150 nm SiN mask was deposited using PECVD at 300 $^{\circ}\text{C}$. Use of such a thin diffusion masks require to SiN to be of high quality to ensure Zn does not diffuse through the mas. Measurements of the refractive index is a useful measure of quality of SiN films used for Zn diffusion, and a refractive index between 2.04 and 2.1 at 633 nm was judged to be suitable for the Zn diffusion conditions used [1]. Optimisation of the SiH₄ flow rate yielded a mask with a refractive index of 2.04. The mask was patterned using photolithography and etched in a buffered HF solution for 3 minutes. The photoresist mask was removed and the sample thoroughly cleaned in acetone and IPA. The Zn diffusion was carried out in a MOCVD chamber using the following procedure. Heat from room temperature to 100 $^{\circ}\text{C}$ in 2 minutes and from 100 $^{\circ}\text{C}$ to 510 $^{\circ}\text{C}$ in 7 minutes. The Zn diffusion was carried out over 45 minutes at 510 $^{\circ}\text{C}$ using a dimethylzinc flow rate of 300 sccm. The wafer was cooled from 510 to 360 $^{\circ}\text{C}$ in 4 min and from 360 $^{\circ}\text{C}$ to 270 $^{\circ}\text{C}$ in 4 minutes 30 seconds. After the diffusion, the 150 nm thick SiN mask was removed in a buffered HF solution for 12 minutes. The Zn diffused diodes were passivated with SU8, had 250 nm thick SiN bond pads deposited and finally metalised with Ti/Au back and top contacts. AR coating was not used. SIMS results are shown in Figure 8.1 and the peak doping concentration was measured to be $2.8 \times 10^{19} \text{ cm}^{-3}$ and reached a depth of 2.5 μm .

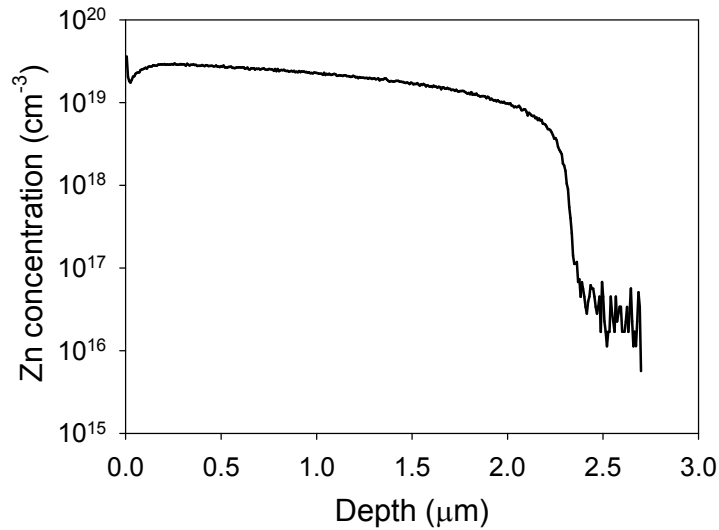


Figure 8.1: The Zn concentration profile as measured by SIMS

The I-V characteristics of 6, 200 μm diameter and 8, 50 μm diameter photodiodes are shown in Figure 8.2 and Figure 8.3 respectively. The 200 μm diameter photodiodes showed a dark current density of 0.17 Acm^{-2} at -0.5 V at room temperature which is significantly lower than that of the Be implanted diodes at 1 Acm^{-2} . However, the uniformity was found to be much poorer. Due to the low dark current, the power dissipation within the Zn diffused diodes was much low and therefore a significantly larger reverse bias voltage could be achieved. The diodes could not be made to breakdown at room temperature as a large tunnelling current dominated the dark current at reverse bias voltages of -6V . The responsivity of the Zn diffused diodes was found to be very low at 0.17 A/W at 1550 nm without any AR coating. This low responsivity is an artefact of the thick, and highly doped P-type region. The detectivity of the Zn diffused planar diodes was found to be $7.11 \text{ cmHz}^{-1/2}\text{W}^{-1}$ at -0.3 V which is larger than the Be implanted diodes with a detectivity of $6.08 \times 10^8 \text{ cmHz}^{-1/2}\text{W}^{-1}$. The gain of a Zn diffused APDs at room temperature measured using a 1550 nm laser is shown in Figure 8.4. Due to the thin epitaxial region used, the gain for a given bias voltage is very low.

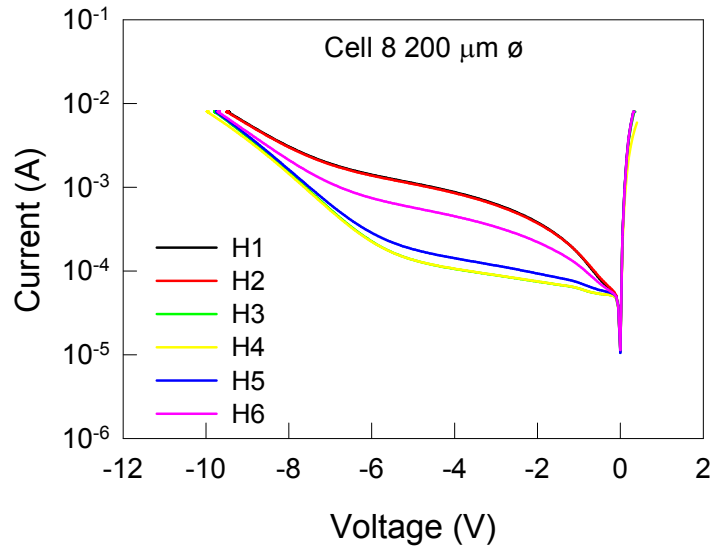


Figure 8.2: The I-V characteristics of 6, 200 μm diameter photodiodes

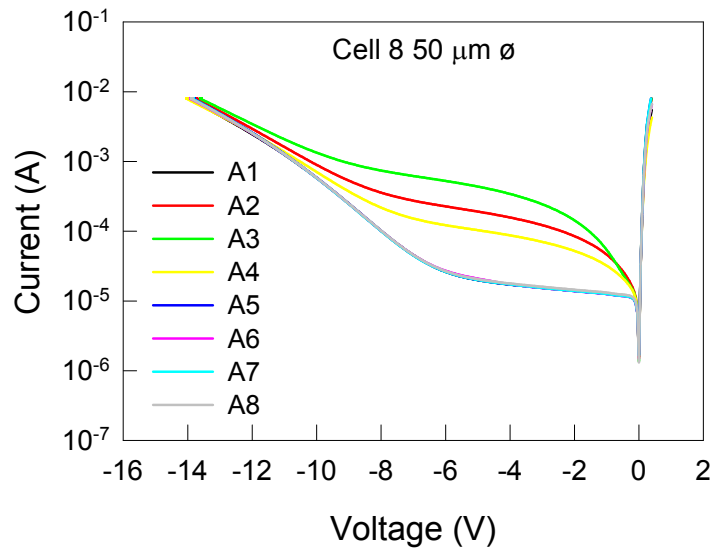


Figure 8.3: The I-V characteristics of 8, 50 μm diameter photodiodes.

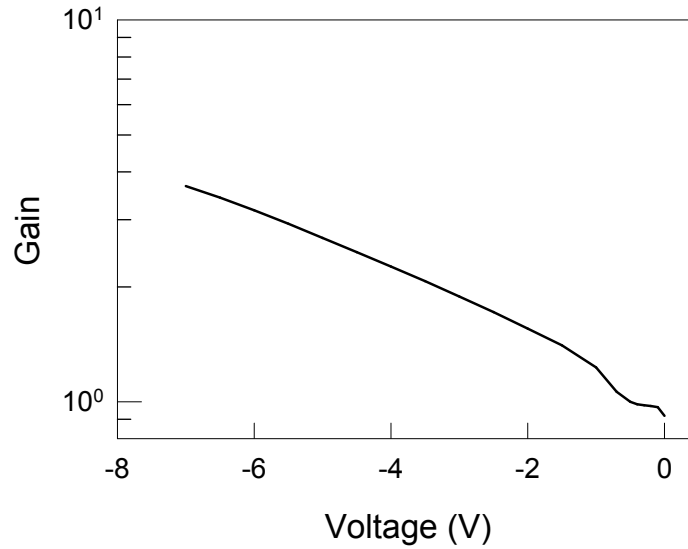


Figure 8.4: The gain of a 200 μm diameter Zn diffused APD at room temperature measured using a 1550 nm laser.

The temperature dependence of a 200 μm diameter APD is shown in Figure 8.5. The contributions from bulk and surface leakage have not been analysed, and should be carried out as future work. However, in order to minimise errors, the uniformity of the Zn diffused photodiodes should be first improved. Due to the narrow intrinsic region thickness, tunnelling, current dominated at large bias voltages. A comparison between the dark current of a Zn diffused and Be implanted APD are shown in Figure 8.6. Although the dark current of the Zn diffused sample is significantly lower at room temperature, the rate at which the dark current reduces with temperature is significantly lower, and at 200 K, both diodes showed approximately the same dark current density of $400 \mu\text{Acm}^{-2}$.

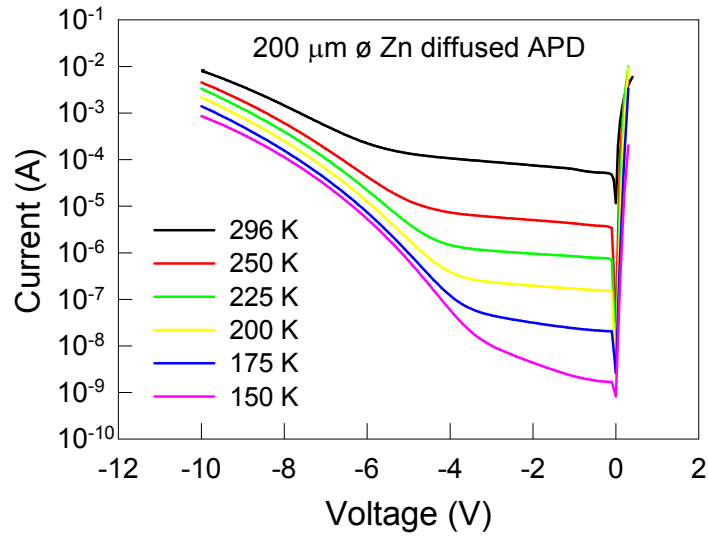


Figure 8.5: The I-V characteristics of a 200 μm diameter Zn diffused APD measured from 296 to 150 K.

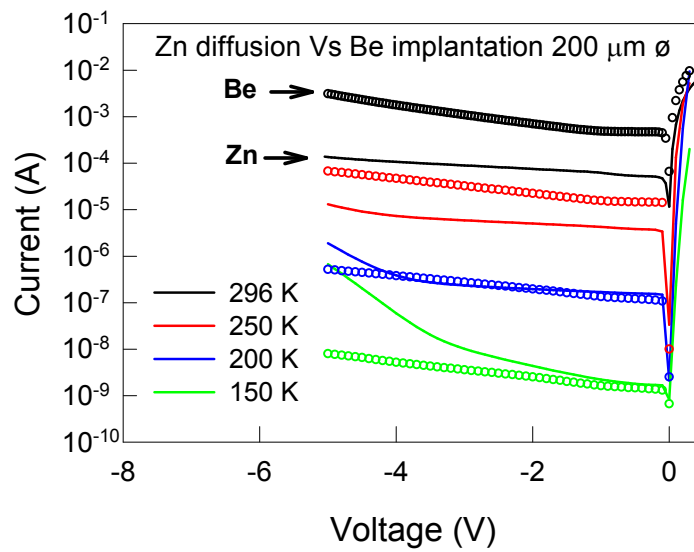


Figure 8.6: The I-V characteristics of a 200 μm diameter Zn diffused and Be implanted APD from 296 to 200 K.

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8.4 Planar fabrication procedure

The V7 mask set is designed to fabricate planar APDs using either Zn diffusion or ion implantation. A description of the mask set can be found in section 8.4.15 (Note: V7 also contains 4 masks for fabricating lateral APDs which are not to be used for this procedure). The devices fabricated from V7 will have top and back metal contact layers. A photograph and a schematic diagram of fabricated devices are shown in Figure 4.11. (Note: there is no grid etch layer and so a conducting substrate must be used).

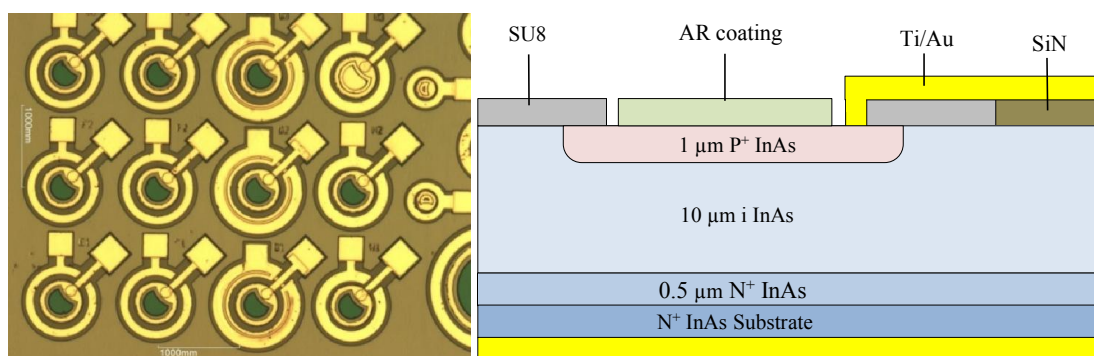


Figure 8.7: A micrograph of and a schematic diagram of a planar InAs APD

8.4.1 Cleaving

- Carefully place the wafer epi side down on a filter paper
- Pinning the wafer in place with some tweezers, cleave a sample from the wafer using a diamond tip scribing tool.
- The maximum sample size is limited to $\frac{1}{4}$ of a 2" wafer due to the V7 mask size. (Be very careful not to move the wafer around on the filter paper as this will scratch the sample)
- Blow away any semiconductor dust using the nitrogen gun
- Replace Epi wafer and name the sample in its box

8.4.2 Cleaning

It is VERY important that you do not use a cotton bud to clean the sample at this stage. The surface of the wafer is exposed and cleaning the sample with a cotton bud will cause surface damage resulting in high surface leakage across the planar diodes.

- Using the dedicated InAs 3-stage-clean beakers, pour out N-Butyl acetate (NB), Acetone and IPA.
- Warm the NB on a hotplate
- Soak sample in NB for 3 minute.
- Remove the sample from the NB and without drying place directly into the acetone and leave for 3 minute
- Remove the sample from the acetone and without drying, place directly into the IPA and leave for 3 minute
- Remove sample from IPA and dry with nitrogen gun
- Inspect the sample under a microscope
- If the sample looks dirty, repeat the 3 stage clean process (Note: InAs defects can often look like dirt as shown in Figure 8.8.
- If the dirt cannot be removed using the three stage clean then the last resort should be to use the cotton bud, however, a surface etch may be required to reduce the surface leakage.

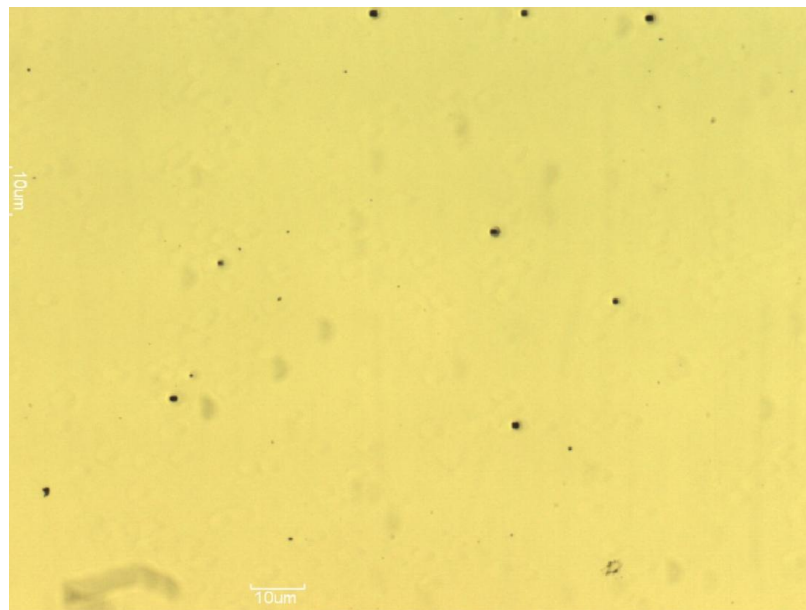


Figure 8.8: Picture of defects on an InAs wafer

8.4.3 Deposit the encapsulating layer

When InAs is heated to temperatures above 450 °C (during the annealing process), the arsenic will outgas at a significantly greater rate than the indium, causing an indium rich surface layer to form. To prevent this loss in stoichiometry during annealing, the InAs

surface can be encapsulated in a dielectric material such as SiN or SiO₂ which forms a physical barrier against the outgassing. There is a large difference between the thermal expansion co-efficient of dielectric materials and InAs. Thick layers of SiN or SiO₂ will induce significant stress during annealing and cause the encapsulating layer to fracture or induce damage to the InAs layer, therefore very thin films of SiN or SiO₂ should be used. During this work 35 nm films of SiO₂ were used, however, SiN is also suitable (possibly even a better choice as the thermal expansion co-efficient closely matches that of InAs). In addition to providing a barrier against outgassing, the encapsulating layer also protects the InAs surface against damage and contamination during the subsequent processing steps.

Only continue if the sample is very clean.

- Prepare the PECVD chamber by completing a dummy run for 10 minutes using an appropriate recipe. During this work the standard SiO₂ recipe was used with a deposition temperature of 300 °C.
- Calculate the deposition rate by completing a short (5min) deposition on a Si test sample. The deposition rate and film quality can be found through characterising the test sample using the elipsometer.
- Carefully load the sample into the chamber and begin the deposition of the encapsulating layer. During this work a 35 - 50 nm film was used which was deposited in 35 s using the standard SiO₂ recipe.
- Carefully load the sample into the chamber
- Unload the sample and let it cool before replacing it back in its box.

8.4.4 Pattern alignment marks

The alignment marks need to be defined in a separate step so that a reference to the implanted area is maintained after the implant mask has been removed.

- If the sample has been sitting around for a while after completing section 3 it is advised that the 3 stage clean is repeated by following section 2
- Bake sample on a 100 °C hot plate for 1 minute
- Allow to cool before placing on blue tacky paper
- Mount the sample onto the spinner and test the spin speed is 4000rpm
- Use a disposable pipette to drip some Hexamethyldisilazide (HMDS) onto the sample and then spin the sample at 4000 rpm for 30 s (Note: The HMDS supports good adhesion between the photoresist and SiO₂)

- Drip photoresist BPRS200 onto the sample and spin at 4000 rpm for 30 s
- Bake the sample for 1 minute at 100 °C to ensure the photoresist is fully dehydrated.
- Locate the first mask from the V7 mask set
- Using the alignment mask layer, align the mask to be roughly square to one of the sample crystal planes and then expose the sample.
- Develop the sample in the appropriate developer for 1 minute and rinse in DI water
- Inspect the sample under the microscope. If the exposure is poor then remove the photoresist in acetone. Complete a 3 stage clean and then restart the section.

8.4.5 Define alignment marks

It is recommended that the alignment mark are etched into the sample, however, they can also be deposited using metal. If metal is to be used then simply replace the ICP dry etching stage with an evaporation and lift off procedure using a suitable metal.

To etch through the SiO₂ protective layer

- Prepare the RIE chamber by completing a dummy run for 10 minutes using an appropriate recipe. During this work the standard SiO₂ etch recipe was used on RIE1
- Carefully load the sample into the chamber etch for ≈ 2 minutes to etch through the SiO₂ protective layer
- Unload the sample and replace it back into its box. (Note: Do not remove the photoresist before completing 5.4)

To etch the alignment marks

- Prepare the ICP chamber by completing a dummy run for 10 minutes using an appropriate recipe. During this work the GaAs-5 etch recipe was used on ICP1
- Carefully load the sample into the chamber and etch for the time required to produce alignment marks > 1 μm deep.
- Unload the sample and replace it back into its box.
- Remove the photoresist in acetone before completing a 3 stage clean

8.4.6 Mask for implantation

The implantation conditions should have been decided before completing this step as the implant conditions effect the choice of photoresist

- Pattern the sample for implantation by repeating section 4 except with the following changes
- Ensure that the photoresist thickness is larger than the projected range of the implanted ions within the photoresist. This can be modelled using ion implantation software SRIM and selecting one of the default photoresists as the target. In this work photoresist SPR220 spun at 4000-RPM was used (the photoresist span to a thickness of $\approx 4 \mu\text{m}$)
- If a thick photoresist (such as SPR220) was used, then increase the photoresist bake time to 2 minutes at 100 °C to ensure full dehydration
- Use the implantation mask

8.4.7 Send the sample for implantation

Samples were posted in membrane boxes to the implantation facility

8.4.8 Removing the photoresist after implantation

The implantation usually causes heavy crosslinking of the photoresist making it very difficult to remove. It may be necessary to use a cotton bud to aid removal of the photoresist, however, as the SiO₂ protective encapsulation layer is currently in place we can use a cotton bud without damaging the surface of the wafer.

- Fill a shallow beaker with resist stripper EKC830 and heat up to 100 °C
- Place the sample in EKC830 and swirl every now and again. If the photo resist is heavily crosslinked then it may a long time (>15 minutes) before the photoresist begins to dissolve. If the photoresist shows no signs of dissolving after 15 minutes, use a cotton bud on the photoresist.
- The sample may require numerous baths in EKC830 and 3 stage cleans before all of the photoresist has been removed

8.4.9 Annealing

The implanted dopants require activating before they become electrically active. This is achieved through annealing. Rapid thermal annealing is utilised to ensure that the activation efficiency is high whilst also minimising diffusion.

It is important to ensure that all of the photoresist has been removed (even the edge bead) before continuing

- Ensure that the correct annealing recipe is loaded and complete a dummy to ensure that the RTA is functioning correctly. During this work an annealing temperature of 550 °C for 30 s was found to be optimal. There is no pre-programmed routine for these conditions so engineering4 must be modified. The ramp up time from 300 to 550 °C is 30 s and the hold time is also 30 s. The cool down time was 1 minute.
- Carefully load the sample into the chamber and complete the annealing cycle
- Unload the sample and let it cool before replacing it back into its box.

8.4.10 Deposit the back contact

Sputter or evaporate a metal contact onto the back of the sample. In this work 20/200 nm thick Ti/Au contacts were used.

- If the sample has been sitting around for a while it is advised that the 3 stage clean is repeated by following section 2
- Carefully load sample into the sputterer/evaporator and deposit metal

8.4.11 Deposit top contacts

The encapsulating layer must be removed before the top contacts are deposited

- Complete a 3 stage clean
- A buffered HF acid etch is required to remove the SiO₂ encapsulation layer.
During this work an etch time of 30 s was found to be sufficient.
- Inspect the sample under a microscope to ensure that the sample is clean
- Pattern the sample for top contacts by repeating section 4 except the HMDS is not required and the top contact mask layer should be used
- Remove any photoresist remnants by O₂ ashing the sample in the barrel Asher for 1 minutes (Note: Ashing helps ensure a clean interface between the semiconductor and metal)
- Load the sample into the sputterer/evaporator and deposit contacts
- Complete the metalisation through lifting-off in acetone
- Complete a 3 stage clean

It is useful to characterise the I-V characteristics of the sample at this point to ensure that the surface leakage is low before the sample is passivated. If it is found that the surface leakage is very high, then a surface etch may be to reduce the surface leakage (See B. S. White thesis for details).

8.4.12 Deposit Bond pads

InAs APDs are highly sensitive to mechanical probing and it is highly recommended that remote bond pads are used when attempting to fully characterise a sample. The bond pads are constructed from SiN and SiO₂ to ensure a high bond yield, however, such dielectrics perform poorly as passivation layers on InAs APDs. Therefore the bond pads and passivation must be formed separately from two different materials. The bondpad mask also defines AR coating on the devices so the thickness of the bondpad layer should be chosen carefully to optimise absorption at the test wavelength (usually 1.55 μm)

- Complete a 3 stage clean
- Prepare the PECVD chamber by completing a dummy run for 10 minutes using an appropriate recipe. During this work the standard SiN recipe was used with a deposition temperature of 300 °C.
- Calculate the deposition rate by completing a short (5min) deposition on a Si test sample. The deposition rate and film quality can be found through characterising the test sample using the Elipsometer.
- Carefully load the sample into the chamber and begin the deposition of the bond pads/AR coating. In this work a 250 nm layer was used to optimise absorption at 2 μm .
- Unload the sample and let it cool before replacing it back in its box

The etch rate of SiN in HF acid was found to highly directional dependent and the etch rate parallel to the wafer surface was found to be many times larger compared to the etch rate in the direction of growth. As such the HF acid produced significant undercuts under the photoresist and drastically decreased the size of the bond pad. Dry etching can be used to produce very steep etch angle, however, dry etching damages the semiconductor surface and causes very high surface leakage. Therefore a mixture of both methods is recommended when defining the remote bond pads. Dry etching should be employed first until only 50-100 nm of SiN remains. HF etching should be used to finish off the sample.

- Pattern the sample using the ‘Bondpad’ mask by repeating section 4. (Note: Do not confuse the ‘bondpad mask’ with the ‘hard passivation’ mask. Since SiN and SiO₂ were found to perform poorly as passivation layers, the hard passivation mask should not be used)
- Prepare the RIE chamber by completing a dummy run for 10 minutes using an appropriate recipe. During this work the standard SiN etch recipe was used. (Note: Do not use the ICP if you have metal on your sample)
- Load a test piece of SiN into the RIE with half of the sample masked off so that the etch rate can be calculated
- Carefully load the sample into the chamber and etch for the appropriate amount of time
- Unload the sample and replace it back into its box (Note: Do not remove the photoresist)
- A buffered HF acid etch is required to remove the remaining SiN layer. Check to make sure that the SiN has been removed through observations under the microscope.
- Once the bondpads have been fully defined remove the photoresist in acetone
- Complete a 3 stage clean

8.4.13 Passivate with SU8

SU8 was found to be the most suitable passivation layer for InAs. SU8 is available in many viscosities which spin to a wide range of thicknesses. SU8-5 is relatively thick ($\approx 3\text{-}5\ \mu\text{m}$) and is utilised for fabricating mesa diodes since the thick passivation layer helps planarize the sample. However, the thick SU8 causes issues when forming subsequent metalisation layers as the photoresist tends to well up in the features of the SU8 passivation. To avoid this effect SU8-2 is preferred for fabricating planar devices as it spins to a thickness of $\approx 1\ \mu\text{m}$. It is useful to also prepare a few dummy samples so calibrate the exposure time for the metalisation process discussed in the next stage.

Note: Two hotplates are required for SU8 fabrication

- Bake sample on a 95 °C hot plate for 1 minute
- Allow to cool before placing on blue tacky paper
- Mount the sample onto the spinner and program the spin speed to form the correct SU8 thickness
- Use a disposable pipette to drip some SU8 onto the sample and then spin the sample

- Bake the SU8 at 65 °C for 1 minute and immediately move to the 95 °C hotplate for a further 1 minute
- Align the sample to the ‘SU8’ mask and expose for 2 s. (Note: Be sure to use mask aligner UV300 as SU8 has poor photosensitivity to light greater than 300 nm) Also (Note: Ensure that the exposure was well aligned as the SU8 is very difficult to remove once this step has been carried out)
- Bake the SU8 at 65 °C for 1 minute and immediately move to the 95 °C hotplate for a further 3 minutes
- Using a clean beaker, develop the sample in SU8 developer for 1 minute before immediately rinse in IPA for 1 minute (Note: Do not rinse the sample in DI water in-between these steps)
- Cure the SU8 by exposing the sample for 40s under UV 300 (Note: A mask should not be used)

8.4.14 Bond pad metallisation (broken field plating)

The issue of the photoresist welling in SU8 features can complicate the lift off stage. It is recommended that the following procedure is first completed on a test sample with SU8 features. If SU8-5 was used as the passivation layer, then it may be necessary to doubly expose and develop the sample with the bond pad mask in order to resolve the small features, such as diodes series A through D. Although there are two masks for metalising the bondpad layer, only ‘broken field plating’ should be used as it is the only layer that metallises the SiN bondpad to the device.

- Complete a 3 stage clean
- Pattern the sample using the ‘Broken field plating’ mask by repeating section 4. (Note: Do not use the solid field plating layer and HMDS is not required)
- Remove any photoresist remnants by O₂ ashing the sample in the barrel Asher for 1 minute
- Load the sample into the sputterer/evaporator and deposit contacts
- Complete the metalisation through lifting-off in acetone
- Complete a 3 stage clean

The fabrication is now complete.

8.4.15 V7 mask set description

The layers of the mask set are as follows

- Alignment marks

Shown in Figure 8.9 and used for alignment in photolithography.



Figure 8.9: Alignment marks (purple)

- Be Implant

Figure 8.10 shows the areas to be implanted with Be. Guard rings are 3 μm wide and are located 3 – 6 μm from the junction body. Diodes are included with 1 and 2 guard rings. Various test structures are also included.

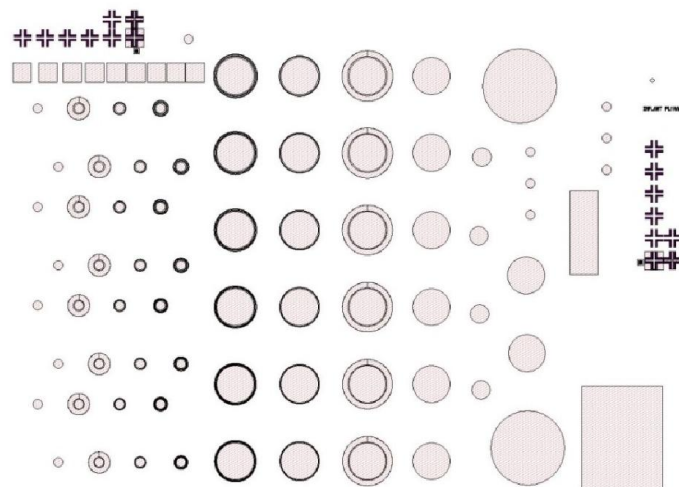


Figure 8.10: Be implant area (pink)

- Metal Contacts

Shown in Figure 8.11 and used to define the metal contacts on the diodes and test structures.

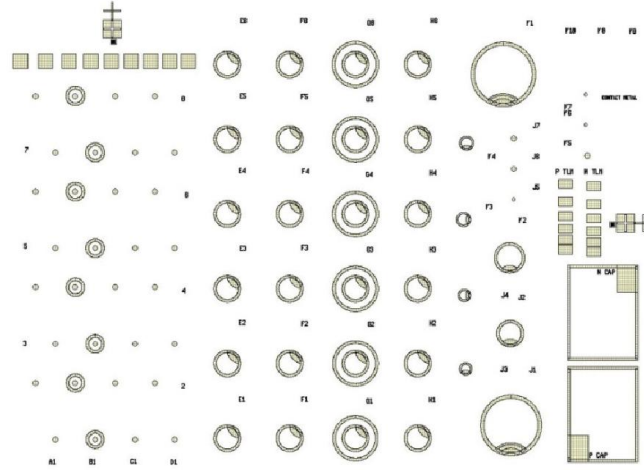


Figure 8.11: Metal contacts to planar diodes (gold)

- Hard passivation

Shown in Figure 8.12, hard passivation layers, such as SiO₂ or SiN, are usually deposited evenly onto the sample. The Hard passivation mask will be used to then define the passivation around the diodes active area and also open up windows to make the metal contacts accessible.

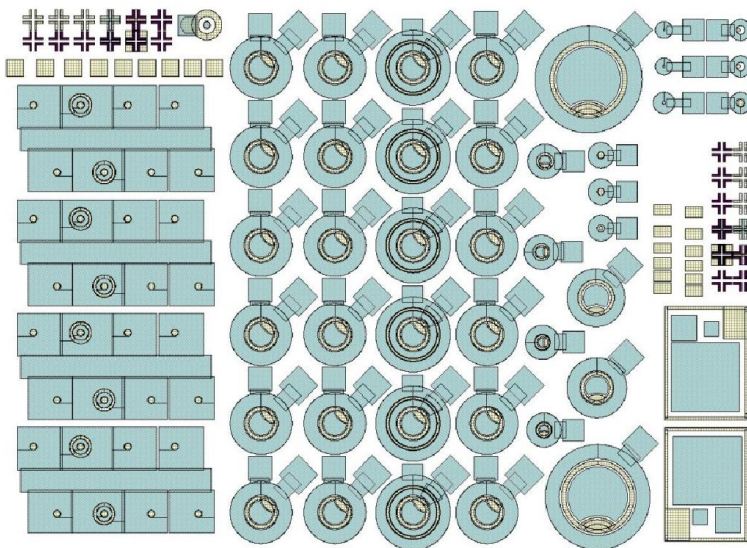


Figure 8.12: Hard passivation (blue)

- Soft Passivation

Shown in Figure 8.13, this follows the same process as above, except a soft passivation such as SU8 is used instead. The SU8 will not form the bond pads which will be formed by the mask layer below named 'Bond Pad'.

- Bond Pad

Also shown in Figure 8.13, this mask will be used with the mask set above to form the bond pads out of SiO_2 or SiN .

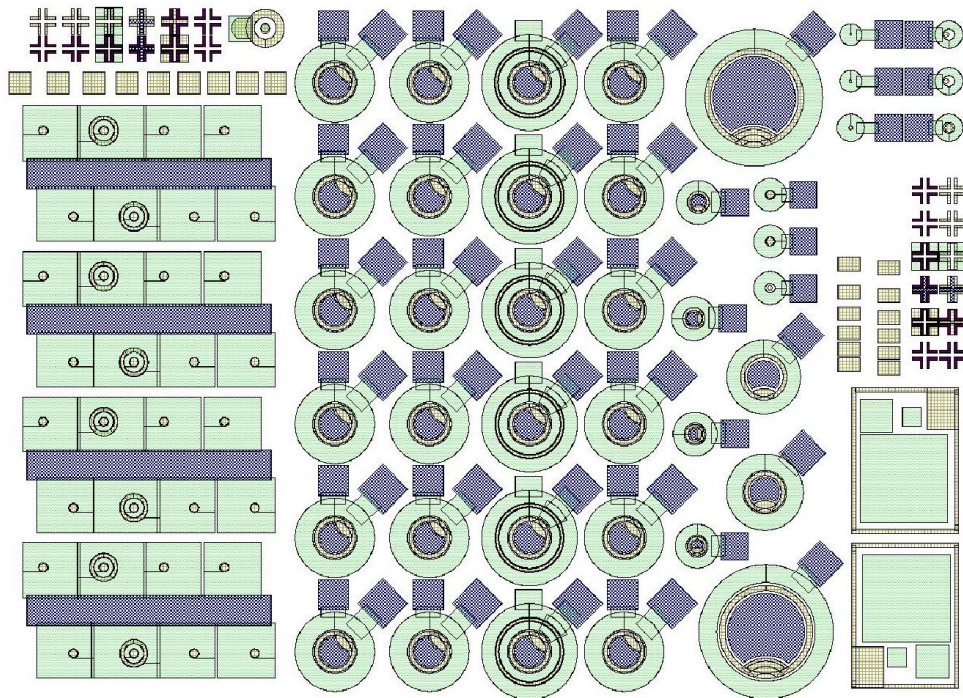


Figure 8.13: Soft passivation (green) and bond pad and AR coating (blue)

- Solid field plating

Shown in Figure 8.14, the metal of this field plating covers the entire junction boundary of the diode forming a complete ring. However, electrical contact to the device must be made by directly probing the device.

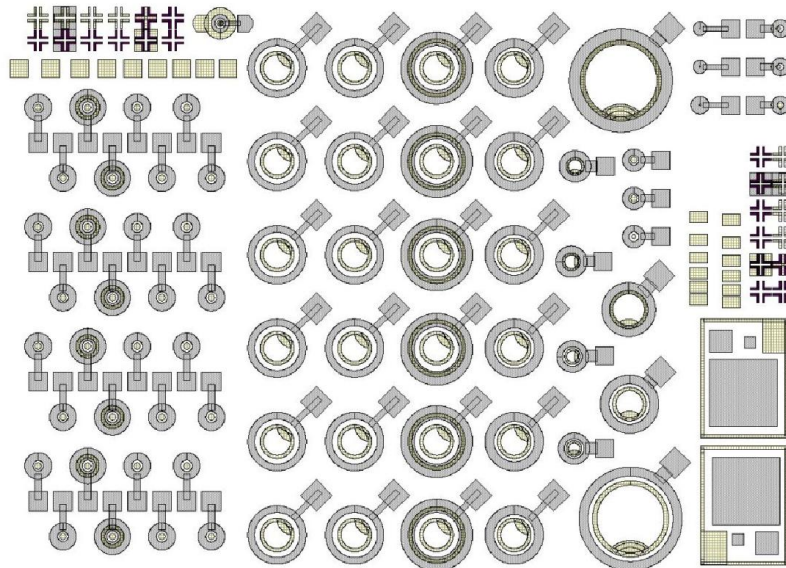


Figure 8.14: Solid field plating (silver)

- Broken field plating

Shown in Figure 8.15, there is a break in this field plating so that electrical contact to the device can be via an external bond pad.

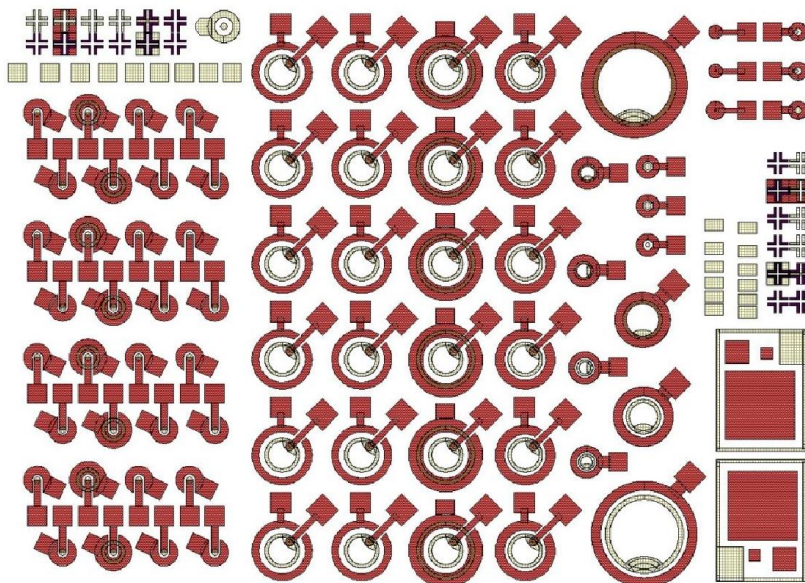


Figure 8.15: Broken field plating (scarlet)

8.5 Synopsys device simulations

Synopsys TCAD was utilised to perform simulations of the InAs APDs. The intrinsic region was 6 μm thick with n-type doping concentration of $5 \times 10^{14} \text{ cm}^{-3}$ if not stated otherwise. The substrate was doped to $1 \times 10^{18} \text{ cm}^{-3}$ and was 2 μm thick. P-type junctions were defined using two gaussian distributions to match the 200 and 70 keV energy implants. The 200 keV implant was described with a peak at 500 nm from the semiconductor surface with a longitudinal straggle of 130 nm and a lateral straggle of 315 nm. The 70 keV energy implant was described with by peak doping concentration at 54 nm with a straggle of 113 nm and a lateral straggle of 315 nm. The dopant diffusion due to annealing was not accounted for in the simulations. The peak doping concentration was assumed to be $1 \times 10^{18} \text{ cm}^{-3}$ as the activation efficiency is expected to be 50 %. The anode lied along the implant window from $x = 0$ to $x = 25 \mu\text{m}$. Devices were designed as half of a cross section around the $x = 0$ axis and cylindrical mathematics was used to generate a device.