Control of a Modular Multilevel Flying Capacitor Based STATCOM for Distribution Systems

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The candidate confirms that the work submitted is his/her own, except where work which has formed part of jointly-authored publications has been included. The contribution of the candidate and the other authors to this work has been explicitly indicated below. The candidate confirms that appropriate credit has been given within the thesis where reference has been made to the work of others.

Publications:

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2) *Nwobu, C.J.; Efika, I.B.; Oghorada, O.J.K.; Zhang, L. "A modular multilevel flying capacitor converter-based STATCOM for reactive power control in distribution systems", Power Electronics and Applications (EPE'15 ECCE-Europe), 2015 17th European Conference on, page(s): 1 – 9*
3) *Efika, I.B.; Nwobu, C.J.; Zhang, L., "Reactive power compensation by modular multilevel flying capacitor converter-based STATCOM using PS-PWM," in Power Electronics, Machines and Drives (PEMD 2014), 7th IET International Conference on , vol., no., pp.1-6, 8-10 April 2014*
4) *Nwobu, C.J.; Chong, B.V.P.; Zhang, L. "A novel phase locked loop scheme for grid voltage synchronisation using the energy operator", Power Electronics and Applications (EPE'15 ECCE-Europe), 2015 17th European Conference on, page(s): 1 – 10*

Chapter 3 of the thesis comprises work forming part of the 1st publication . Chapters 2, 5 and 6 of the thesis are comprised of work forming part of the 2nd publication and 3rd publication. Chapter 4 comprises work forming part of the publication in the 4th publication. The entire works in Chapters 1-8 are attributable to the candidate under the supervision of Dr. Li Zhang.

Assertion of moral rights (optional):

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Most importantly to God Almighty, My Sovereign Father,

Chukwu Ebuka, Chukwu Ebuka, (You are Great) Sorom Tobe Ya, (Join me and Worship Him) Ma'm kowa nmeso oma gi oh, (If I talk about your goodness), Chi ga eji, chi ga abo (Night will come, and Day will break), Ma'm kowa ihe oma Ine meren m oh (If I talk about the all the good things you do), Chi ga eji, chi ga abo (Night will come, and Day will break), Asi n'aru mu buru so onu (If all my body was my mouth), Ozughi inye gi ekele (It is not enough to praise you), Chi di nma (God is Good), Nare ekele (Take all the praise).

Abstract

Voltage fluctuation and power losses in the distribution line are problems in distribution networks. One method to mitigate these problems is by injecting reactive power into the network using a Static Synchronous Compensator (STATCOM). This can be used both for regulating the voltage and reducing the losses. A STATCOM is critically dependent on a grid synchronisation scheme that can accurately track the changes occurring in the grid phase and frequency. The Modular Multilevel Converter (MMC) is a promising topology for STATCOM applications because of its simple modular circuit structure that allows for higher voltage ratings, and conventionally uses a stack of sub-modules which are either two-level half or H-bridge converters.

As a novel alternative, the thesis investigates the practicality of a STATCOM based on a three-level flying capacitor (FC) converter. Two variants of this topology are presented; the FC Half-bridge and FC H-bridge. A comprehensive study is undertaken to compare these with the Half and H-bridge sub-module under STATCOM operation. Most importantly, an FC H-bridge-based STATCOM is investigated for reactive power compensation. The challenges of multilevel, multi-module PWM control schemes achieving good waveforms at low switching frequency, whilst maintaining module capacitor voltage balance, are thoroughly addressed. Simulation results validate the operation for both line voltage regulation and power factor correction. An experimental power system with an FC-based STATCOM rig is designed and built, and validates the simulation results for power factor correction. It demonstrates correct operation of a control scheme that includes a system for maintaining capacitor voltage balance.

Another new contribution is the investigation of a phase locking technique based on the Energy Operator (EO). The method, combining two different EO computations, is shown to achieve fast and accurate detection of frequency and phase angle when combined with an appropriate filter, and crucially operates well under unbalanced voltage conditions. The technique is compared with two other well-known phase locked loop (PLL) schemes, showing that it outperforms the others in terms of speed and accuracy. A hardware implementation of the EO-PLL validates the principle, showing the simplicity of the method.

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List of Abbreviations

PCC	Point of Common Coupling
TCSC	Thyristor Controlled Series Capacitor
SVC	Static VAR Compensator
SSSC	Static Series Compensator
STATCOM	Static Compensator
UPFC	Unified Power Flow Controller
UPQC	Unified Power Quality Conditioner
PLL	Phase Locked Loop
DDSRF	Decoupled Double Synchronisation Reference Frame PLL
CDSC-PLL	Cascaded Delay Signal Cancellation PLL
EO-PLL	Energy Operator PLL
SRF-PLL	Synchronisation Reference Frame PLL
NPC	Neutral Point Clamped Converter
FC	Flying Capacitor Converter
MMC	Modular Multilevel Converter
FC-MMC	Flying Capacitor Modular Multilevel Converter
PS-PWM	Phase-Shifting Pulse-Width Modulation
PD-PWM	Phase Deposition Pulse Width Modulation
FACTS	Flexible AC Transmission Systems
HVDC	High Voltage DC Transmission
LCC HVDC	Line Commutated Converter HVDC

Chapter 1
Introduction

1.1 Background Literature

Sustainable and clean ways of generating electricity from renewable natural sources like solar and wind now exist in the distribution grid network. This offers solutions for increasing the total power generation capacity and reducing environmental impact. However, the integration of solar and wind power generators poses a challenge as the conventional distribution grid structure is designed to allow mainly unidirectional power flow. There is also now the requirement of integrating the AC grid with the DC networks with the growing need for charging of electrical vehicles. Concerns are arising over how ageing electrical infrastructures built decades ago will cope with these changes.

The establishment of a more efficient distribution grid network is an effective solution to meeting the challenges posed. This advanced network, with reinforced electrical power infrastructures and improved communications, will allow optimum management of electricity distribution to consumers. It has sparked global interest and increased investment in improving the efficiency of the electrical power infrastructure. However, the guidelines for achieving this are still being developed as they involve the integration of various key sectors like IT, power generation, and communications.

The overall objective is to develop an intelligent digitised energy network delivering electricity in an optimum way from generating sources to the consumers. This can be viewed in two ways

1) The deployment of automated metering infrastructure that improves communication between energy suppliers and consumers, i.e. consumers can now also benefit from knowing how to optimise their energy usage and communicate effectively with energy suppliers.
2) The deployment in the distribution system of automated devices that allow operation of distribution infrastructure with greater efficiency and flexibility.

In short, the two arms of this strategy are improving the power metering and data communication, and improving the control of power flow within the network.

Power electronic devices are the enabling technology in achieving control of the power flow and research is led by industry and academic experts on their application in power systems. The future grid network needs considerable research in power flow control using Flexible AC Transmission Systems (FACTS), such as the Static Compensator (STATCOM) for reactive power compensation, and High Voltage transfer using HVDC systems as illustrated below in Figure 1.1.

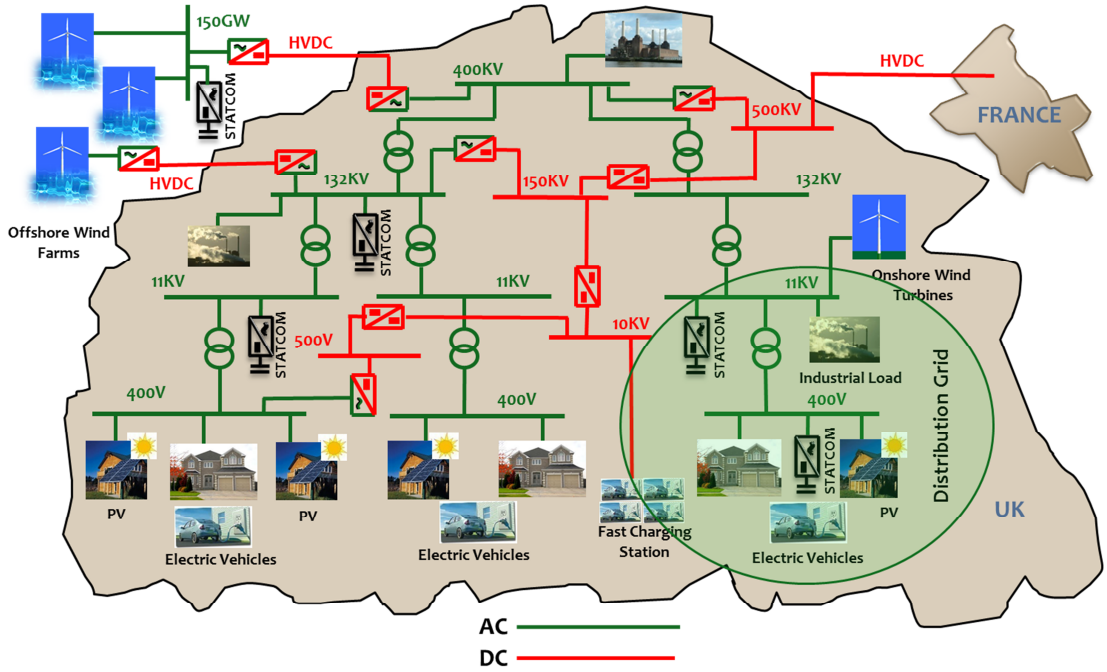


Figure 1.1: Future Transmission and Distribution Grid System

1.2 Flexible AC Transmission Systems

Research on Flexible AC Transmission systems (FACTS) dates back as far as the 1960's [1] when a proposal was made for the improvement of transient stability of a power network with series connected switched capacitors. The definitions and concepts were published in later years (1988) by Hingorani [2] but still failed to be realisable due to the poor response of power electronic devices and control systems at that time. FACTS controllers are generally categorised into three eras:

1st generation: which includes shunt and series connected devices:

- Thyristor Controlled Series Capacitor (TCSC)
- Static VAR Compensator (SVC)

2nd generation: which also includes shunt and series connected devices:

- Static Synchronous Series Compensator (SSSC)
- Static Compensator (STATCOM)

3rd generation: which combines series-shunt compensation devices:

- Unified Power Flow Controller (UPFC)
- Unified Power Quality Controller (UPQC)

1.2.1 Thyristor Controlled Series Capacitor (TCSC)

The Thyristor Controlled Series Capacitor (TCSC) is a series compensation scheme that works by varying the effective reactance of the transmission line to regulate active power flow. Its circuit is a combination of thyristor controlled capacitors and reactors /inductors across two nodes of the transmission line as shown in Figure 1.2 (a). This forms the nonlinear reactance X_m which is connected in series with the transmission line as shown in Figure 1.2 (b). Provided the transmission line resistance is much far less than its reactance, the active power can be regulated by varying the reactance X_m according to equation (1.1).

$$P_m = \frac{|V_1||V_2|}{X_m} \cdot \sin(\theta_1 - \theta_2) \qquad (1.1)$$

where, θ_1 = angle of the voltage at bus V_1 and θ_2 = angle of the voltage at bus V_2 .

The Thyristor Controlled Series Capacitor (TCSC) has been available commercially since the early 1990's. The first such installation was the thyristor switched series capacitor version (TSSC) in a 345 kV transmission line at the Kanawa River Substation [3]. Subsequent early installations are recorded in the 230 kV transmission lines at Kayentta Substation [4] and at the Slatt substation [5]. TCSC product ranges are still available from some companies, e.g. Siemens and ABB [6, 7] .

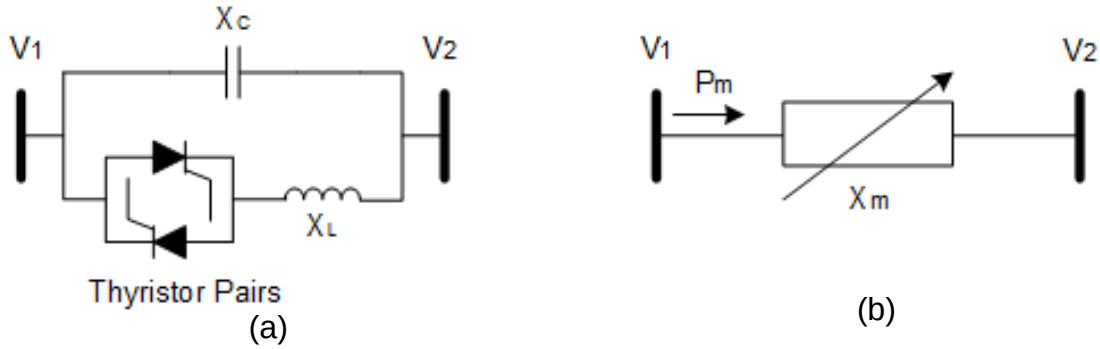


Figure 1.2: Thyristor Controlled Series Capacitor: (a) Thyristor Controlled Reactor with fixed capacitor (b) Variable reactance representation

1.2.2 Static VAR Compensator (SVC)

The Static VAR Compensator (SVC) is a parallel connected equivalent of the TCSC and acts like a nonlinear shunt-connected variable reactance $X_{m.}$ This generates or absorbs reactive power to enable voltage regulation across the line using either thyristor controlled capacitor banks (TSCs) or reactor banks (TCRs). The power circuit of an SVC with thyristor controlled reactors is as shown in Figure 1.3 (a). A nonlinear model representation is as shown in Figure 1.3 (b) where the reactance X_m is represented as equivalent susceptance $B_{m.}$ Assuming the resistance across the line is negligible, the reactive power can be regulated by adjusting the susceptance B_m using equation (1.2).

$$Q_m = -|V_1|^2 B_m \qquad (1.2)$$

This technology was introduced to improve the power quality in transmission lines. The first commercially available FACTS controllers for Static VAR Compensator (SVC) application to voltage control and stability improvement are dated as early as the late 1970's [8]. The major drawback is that it requires switching in of pre-calculated values of the capacitors and reactors. However, commercially available SVC's are still marketed by transmission grid equipment manufacturers like Siemens, GE Grid Solutions (Alstom) and ABB [9-11].

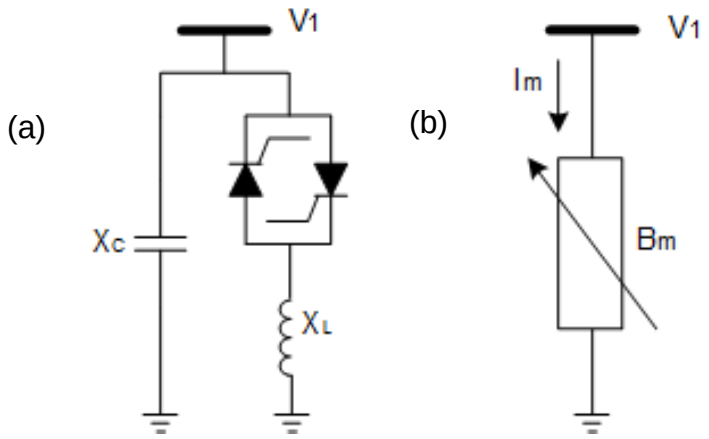


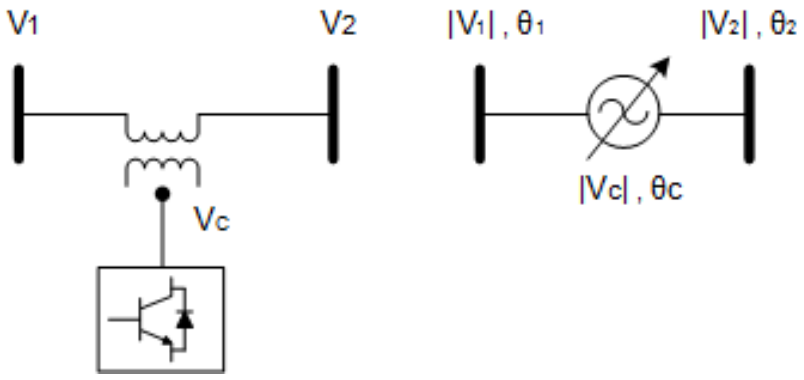
Figure 1.3: Static VAR Compensator: (a) TCR with fixed capacitor
(b) Variable susceptance representation

1.2.3 Static Synchronous Series Compensator (SSSC)

The second generation of FACTS controller replaced the thyristor - switched elements with power converters. The basic principle was the use of power converters coupled with reactive components to control the effective parameters of the transmission line. Similarly to first generation devices, the static series compensator (SSSC) would be series connected and be used to control the active power flow by varying the apparent impedance of the transmission line. However the SSSC provides additional functionality as it can provide also regulation of reactive power flow because of the converter's DC capacitor. Figure 1.4 (a)-(b) shows the power circuit configuration for the SSSC and its equivalent power circuit representation. The equivalent model can be represented as a series connected voltage source with variable magnitude V_C and phase angle $\angle\theta_C$. Adjusting the magnitude and phase angle regulates the active and reactive power flow across the line:

$$V_C = |V_C|(\cos\theta_C + j\sin\theta_C) \tag{1.3}$$

The Static Synchronous Series compensator (SSSC) is not as commonly used commercially as other FACTS devices. Most literature available for practical applications deals with laboratory scale investigations using various control schemes and methods [12-14]. Its commercial application is reported as part of the first early installation of a UPFC at the Inez Substation [8, 15] and more recently the KEPCO UPFC at Kangjin substation [16]. Transmission grid suppliers like ABB, Siemens and GE grid solutions at present do not have product ranges advertised on their websites.



(a) (b)

Figure 1.4: Static Synchronous Series Compensator: (a) Converter connected to network by series transformer (b) Equivalent power circuit representation

1.2.4 Static Synchronous Compensator (STATCOM)

The static synchronous compensator (STATCOM) is a shunt connected version of an SSSC. The shunt connected power circuit and its equivalent model are as shown in Figure 1.5 (a)-(b). This also regulates the active and reactive power flow across the line by controlling the magnitude and phase angle of the converter voltage. For an ideal STATCOM under reactive power operation with no active power loss, the reactive power is regulated based on equation (1.4).

$$Q_m = \frac{|V_1|^2 - |V_1||V_C|}{X_m} \cdot \cos(\theta_1 - \theta_C) \qquad (1.4)$$

The static synchronous compensator (STATCOM) is the most popularly used among the other FACTS controllers. Its first commercial application was for a 20 MVAR STATCOM using force-commutated thyristors by Kansai Electric Power Co. Inc. (KEPCO) and Mitsubishi Motors, inverters, in 1980 [17] . Following that, a 1 MVAR STATCOM using high power GTO inverters was developed by Westinghouse Electric Company [18]. Some other installations documented are the ±80 MVAR STATCOM in Japan (1991) [19]; the ±100 MVAR STATCOM at Sullivan substation (1996) [20] ; the 8 MVA STATCOM at Rejsby Hede wind farm (1997) [21] and the ± 200 MVAR STATCOM at Marcy substation (2001) [22]. A general list of more recent installations by different companies up to the year 2015 is presented in [23].

The first of the modular multilevel cascaded converter (MMC) based STATCOMs was reported in early 2001 with a 175 MVAR STATCOM

developed by Alstom [24]. Some other known installations are three-level ±100 MVAR STATCOM and Talega substation (2002) [25], while ABB has also installed six of these MMC STATCOM controllers known as SVC Light in Sweden, Germany, France, Finland and USA [26, 27].

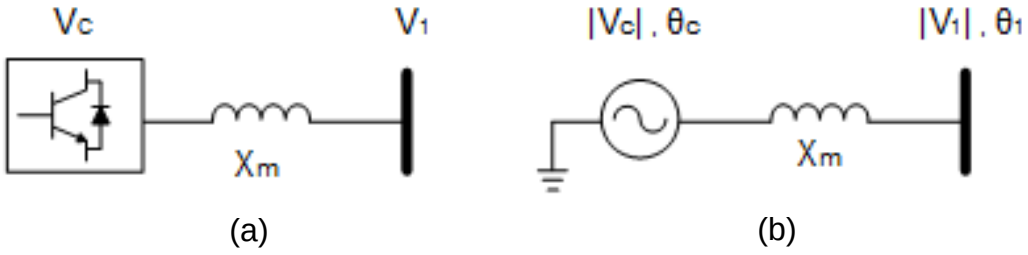


Figure 1.5: Static Synchronous Compensator: (a) Converter shunt connected to the network (b) Equivalent power circuit representation

1.2.5 Unified Power Flow Controller (UPFC)

The Static Synchronous Series compensator (SSSC) proposed by L. Gyugyi [28] was later extended to the concept of the Unified Power Flow Controller (UPFC). This third generation of FACTS controllers is a combination of series and shunt connected second generation devices. The main concept is for simultaneous implementation of both series and shunt connected compensators. The shunt connected device regulates the reactive power flow on the line whilst maintaining the common DC bus capacitor voltage at to be a fixed value whilst the series connected device controls the active power flow in the transmission line. [29-34] .

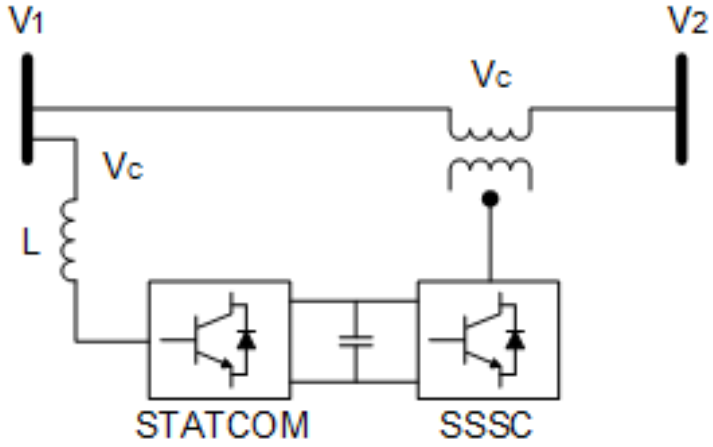


Figure 1.6: Unified Power Flow Controller

1.3 Multilevel Converter Topologies

The introduction of multilevel converters replaced the conventional two-level converters used for early STATCOM applications. The concept dates back to the early 1970's with the design of the three-level converter [35, 36], and is based on building up multiple voltage levels by stacking extra switches in the converter structure either through clamping diodes, capacitors or cascading converters.

The stacked levels produce a fraction of the DC source voltage resulting in (n) levels with $\left(\frac{V_{DC}}{2(n-1)}\right)$ across it. The resulting waveform is emulated as multiple voltage levels of DC pulses, and, depending on the switching scheme, harmonics and losses are reduced; hence there are little or no filter requirements. The major advantage is the reduced voltage stress as the total voltage is distributed across the switches. This results in lower power losses.

Multilevel converters have been studied extensively for STATCOM applications. Most popular are the Neutral Point Clamped (NPC) and the Flying capacitor (FC) converter. A review of the well-established standards for multilevel converters is presented in the literature [35, 37-46]. Currently, converters for STATCOM applications are commercially offered by a growing list of companies in the field [6, 7, 9, 10, 23, 27].

Although they are a well-established and proven technology, multilevel converters still present certain challenges such as improving the energy efficiency, power density, simplicity and cost [41]. Most multilevel converters like the NPC are used in medium voltage applications. Researchers in the past have addressed these issues and looked into possibilities of extending the technique for High voltage application [47-51].

1.3.1 Neutral Point Clamped Converter

The Neutral Point Clamped (NPC) Multi-level Converter was initially proposed by Nabae et al in 1981 [52]. It is also referred to as the diode clamped or multipoint clamped converter, as clamping diodes are used to clamp levels of switches to distinct voltage levels.

The Neutral point converter (NPC) belongs to the family of medium voltage high power converters (2.3 to 6.6 kV) and features medium to high voltage power devices. This makes it suitable for back-to back regenerative applications and it is more widely used in industry than the flying capacitor converter [41]. The 5-level NPC configuration is mostly used because of its

simple power circuit structure with a lower number of power devices and capacitors. Extending this to more levels is less attractive because there are higher and unevenly distributed losses across the power devices, most especially among the increased number of diodes. In addition, the DC link capacitor voltage becomes unbalanced under certain conventional modulation schemes which make is less feasible for higher power applications [53-55].

The five level configuration for the neutral point (NPC) converter, as shown in Figure 1.7, is capable of synthesizing five distinct voltage levels of 0, $+V_{DC}/2$, $-V_{DC}/2$, $+V_{DC}$ and $-V_{DC}$.

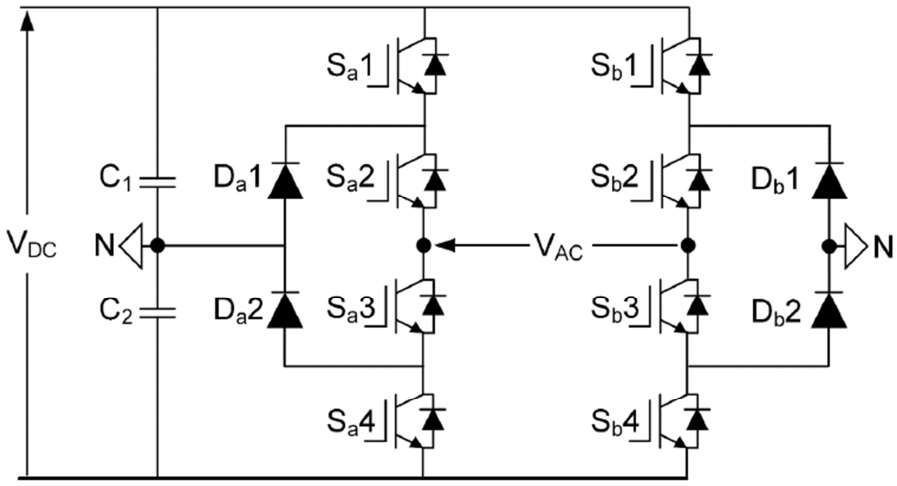


Figure 1.7: H-bridge Configuration of a Neutral Point Clamped Converter

In the full bridge configuration each leg of the converter (i.e. S_{a1} – S_{a4}, S_{b1} – S_{b4}) are clamped together by two diodes (D_{a1}, D_{a2}; D_{b1}, D_{b2}) and this prevents the voltage in one level from surpassing the next level. The complementary switching pairs are S_1, S_3 and S_2, S_4 on each leg which are not operated at the same switching state to prevent short-circuiting the voltage supply. It is also important to note that S_1 and S_4 cannot be switched on at the same time to prevent over voltage. Table 1.1 shows the valid switching states during operation

Table 1.1: Three-level neutral point clamped inverter switching states

Leg A Switches				Leg B Switches				V_{AC}
S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{b1}	S_{b2}	S_{b3}	S_{b4}	
1	1	0	0	0	0	1	1	V_{DC}
1	1	0	0	0	1	1	0	$+V_{DC}/2$
0	1	1	0	0	0	1	1	$+V_{DC}/2$
1	1	0	0	1	1	0	0	0
0	1	1	0	0	1	1	0	0
0	0	1	1	0	0	1	1	0
0	1	1	0	1	1	0	0	$-V_{DC}/2$
0	0	1	1	0	1	1	0	$-V_{DC}/2$
0	0	1	1	1	1	0	0	$-V_{DC}$

1.3.2 Flying Capacitor Converter

The Flying Capacitor (FC) Multi-level Converter was developed by Meynard and Foch [40, 56] and, instead of diodes as in the neutral point clamped converter; it uses capacitors to clamp the switches to distinct voltage levels. The application of the FC converter is covered well in literature [37, 38, 57-59]. Although the FC is well established, it has been less applicable in industry because higher switching frequencies (>1200Hz) are required to keep its capacitors balanced, whereas high power applications require switching in the range of 500-700 Hz [41]. In addition, the higher number of capacitors compared to the NPC makes its power circuit bulky and more expensive. However compared to the NPC, this converter presents more redundant switching states in achieving the multilevel voltage steps.

The five level configuration for the flying capacitor multi-level converter is as shown in Figure 1.8 and is capable of synthesizing five distinct voltage levels of 0, $+V_{DC}/2$ $-V_{DC}/2$ $+V_{DC}$ and $-V_{DC}$ at its output.

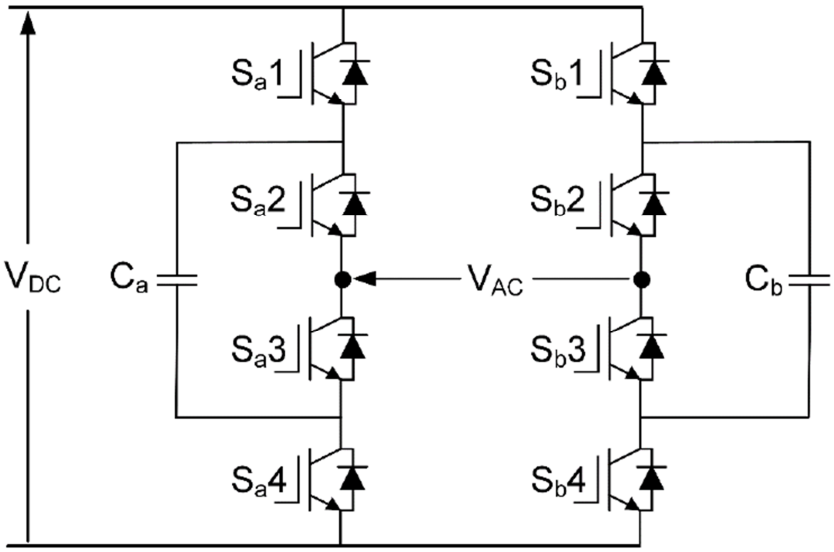


Figure 1.8: H-bridge configuration of a five-level Flying Capacitor Multilevel Inverter

The operating principle of this converter is that in each leg of the converter (i.e. S_{a1} – S_{a4}, S_{b1} – S_{b4}) the voltage stored in each capacitor (C_a and C_b) is half the DC link voltage. This makes the switches at each level (S_{a2}, S_{a3}; S_{b2}, S_{b3}) experience a fraction of the DC link voltage. The complementary switching pairs are S_1, S_4 and S_2, S_3 on each leg giving its valid operation states. For a 5-level converter there are 4 operating states (i.e. 1100, 1010, 0101, and 0011) giving (2^4 =16) possible switching. The voltage levels produced at each level can be increased by stacking two extra at switches at each leg with floating capacitors rated at $\frac{V_{DC}}{n}$ (n = number of levels).

Table 1.2 shows the valid switching states during operation

Table 1.2: Five-level flying capacitor multilevel switching states

Leg A Switches				**Leg B Switches**				**V_{AC}**	**C_a, C_b**
S_{a1}	**S_{a2}**	**S_{a3}**	**S_{a4}**	**S_{b1}**	**S_{b2}**	**S_{b3}**	**S_{b4}**		
1	1	0	0	0	0	1	1	V_{DC}	-
1	1	0	0	1	0	1	0	$+V_{DC}/2$	$C_b \downarrow$
1	1	0	0	0	1	0	1	$+V_{DC}/2$	$C_b \uparrow$
1	0	1	0	0	0	1	1	$+V_{DC}/2$	$C_a \uparrow$
0	1	0	1	0	0	1	1	$+V_{DC}/2$	$C_a \uparrow$
1	1`	0	0	1	1	0	0	0	-

1	0	1	0	1	0	1	0	0	$\downarrow C_a = C_b \uparrow$
1	0	1	0	0	1	0	1	0	$\uparrow C_a = C_b \uparrow$
0	1	0	1	1	0	1	0	0	$\uparrow C_a = C_b \uparrow$
0	1	0	1	0	1	0	1	0	$\downarrow C_a = C_b \downarrow$
0	0	1	1	0	0	1	1	0	-
1	0	1	0	1	1	0	0	$-V_{DC}/2$	$C_a \downarrow$
0	1	0	1	1	1	0	0	$-V_{DC}/2$	$C_a \uparrow$
0	0	1	1	1	0	1	-	$-V_{DC}/2$	$C_b \uparrow$
0	0	1	1	0	1	0	1	$-V_{DC}/2$	$C_b \downarrow$
0	0	1	1	1	1	0	0	$-V_{DC}$	-

1.4 Modular Multilevel Converter Topologies

A challenge posed by the multi-level converter structure is that much more complicated control schemes are required when the structure is extended to higher voltage levels. Also a failure at a certain voltage level could sometimes lead to the whole converter being taken offline if the control schemes are not sufficiently adaptable enough. In a practical power system application this could cause a down time (blackout) which is costly to the power system operators and providers.

With the introduction of the modular concept, where the output voltage is a combination of voltages at the output of various sub-modules, these issues can be tackled. A faulty sub-module can be taken offline awaiting replacement whilst the remaining modules are still in operation. This introduces some redundancy into the system operation and minimises the cost of operation.

The concept of modular multilevel converters dates back as far as the 1960's with the cascaded H-bridge topology [60]. The first implementation of this concept was for drive applications by Robicon Corporation (presently a part of Siemens) in the mid-1990's [61]. The power circuit was a cascade of nine H-bridges per phase but it required a complex phase shifting transformer arrangement to supply the isolated DC requirements. This made it expensive and less attractive for high power applications. Nevertheless,

this discovery encouraged further research interest in improving cascaded converter concepts in later years.

In the later years, Lai and Peng [42] presented a solution with a static synchronous compensator (STATCOM) for reactive power control based on the cascaded H-bridge. This eliminated the need for the complex phase shifting transformer initially proposed. Furthermore, Lenisacar and Marquart proposed an alternate configuration [62] that devised the name “Modular Multi-level Converters”. This proposal detailed a high power modular multi-level converter with significant cost and technical benefits based on cascading half-bridge converters to build up to a converter with a variable output DC terminal. This is a well-known method now used in high voltage DC applications (HVDC), mostly in the transmission grid.

1.4.1 Classification of Modular Multilevel Converters (MMC)

Modular Multilevel Converter have been described by different names in the past such as “cascade multilevel inverter”, series connected H-bridge multi-level inverter”, “chain link multilevel inverter”, “M2C”, and “M2LC” . In other to clarify the different types and variations in circuit structures and establish some consistency, Akagi [63] presented a classification and terminology for modular multilevel converters based on the power circuit configuration. The term “Modular multilevel cascade converter (MMCC)” was adopted with four family members namely:

- Single Star Bridge Cells (MMC-SSBC)
- Single Delta Bridge Cells (MMC-SDBC)
- Double Star Chopper Cells (MMC-DDCC)
- Double Star Bridge Cells (MMC-DSBC)

Figure 1.9 (a) – (c) shows the power circuit configuration for each member of the family. In the single star or single delta configurations, H-bridge sub-modules are used. It is uncommon to implement this with half-bridge cells due to their inability to reserve their polarity (unipolar voltage). For the double star configurations, two star configurations split across top and bottom arms are used. Under STATCOM operation, the top arm generates the 0 to $+V_{DC}$ voltage levels when the top consecutive sub-modules are switched in whilst the bottom arm generates 0 to $-V_{DC}$ similarly in the same way. Either half-bridge (chopper cells) or H-bridge cells sub-modules can be used. It is common use with half-bridge sub-modules as each arm is only required to operate in two quadrants (i.e. bipolar current with unipolar

voltage). H-bridge sub-modules on the other hand, has gathered some research interest for DC fault blocking. Recent literature of single/double star and delta configurations for different STATCOM power applications is presented in [64-72].

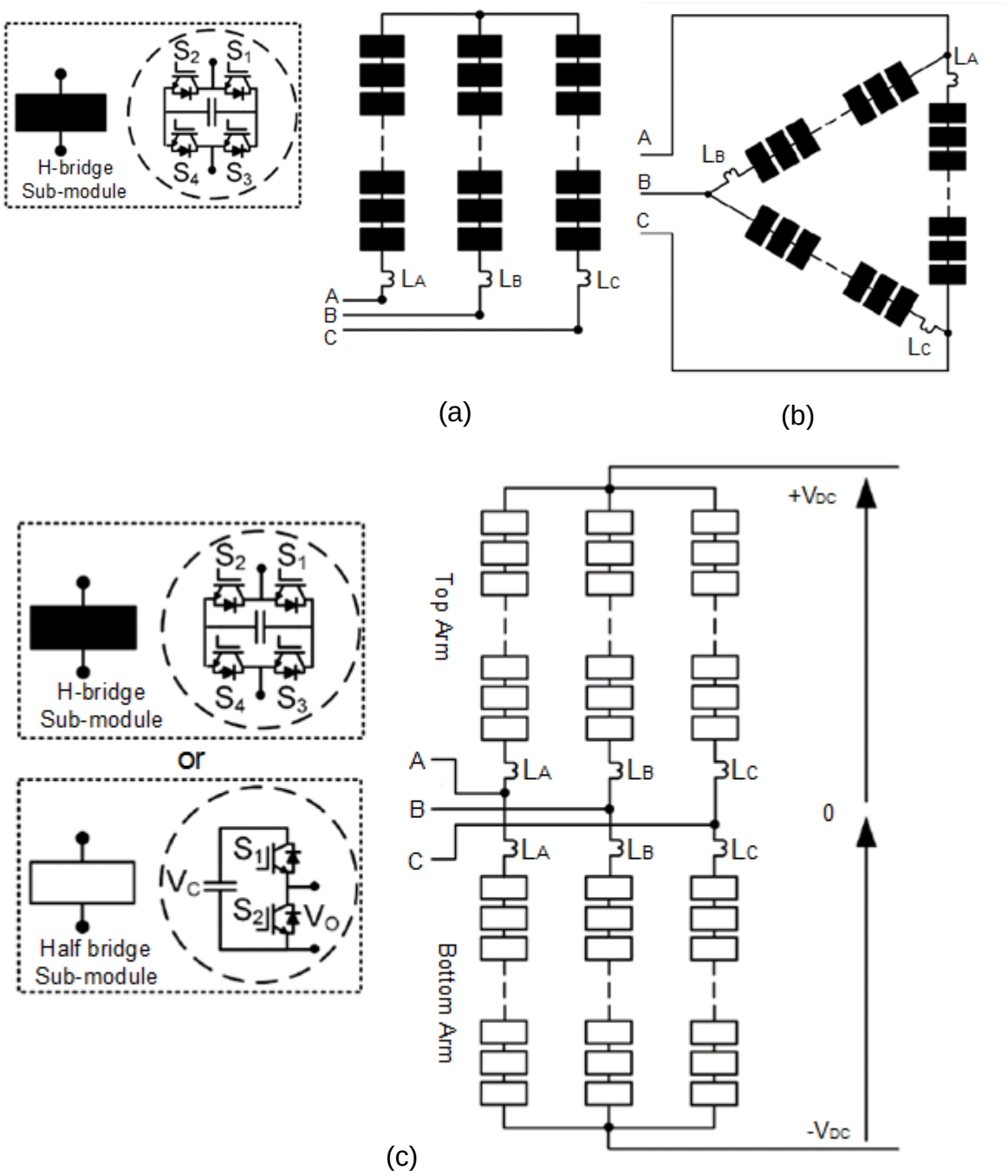


Figure 1.9: Power Circuit Configuration (a) Single Star Bridge Cells (b) Single Delta Bridge Cells (c) Double Star Chopper/Bridge Cells

1.4.2 Other MMC Sub-Module Configurations

Interest has recently been growing in alternate configurations for modular multi-level converters with different features. Some researchers focus on different sub-module concepts whilst other investigate alternate circuit structures. Most of the research has targeted HVDC applications. A review of recent developments in MMCC topologies is presented below.

1.4.2.1 Sub-Module Concepts

A comprehensive study of different sub-modules can be found in the literature [73-77]. Alternative concepts are either based on cascading variant of classical multilevel converters, such as flying capacitor (FC) and Neutral point clamped NPC types in either in their half-bridge or H-bridge configurations. Under the Flying Capacitor variant various sub-module concepts have been proposed such as the FC-MMC in this study [78-82] . Other includes using half-bridge FC sub-modules [75], modified FC sub-modules [83], FC-MMC for medium drive applications based on series connected sub-modules [84], new flying capacitor multilevel converter [85]. Neutral point clamped (NPC) sub-modules have been investigated [74] but have the least applicable features as their capacitors cannot be easily balanced. Modified versions of the NPC has been proposed to tackle this issue [74, 86]. Although various sub-module concepts have been proposed the MMC with half-bridge (chopper) sub-modules in double star configuration is have been widely accepted approach to building MMC's mostly in HVDC . Research is still on-going as to its relevance for in medium power distribution networks.

1.4.2.2 Other Circuit Structures

There is a continued interest in alternate MMC circuit structures to improve the converter power efficiency. Research both in academia and industry has suggested alternate configurations mostly for HVDC applications. Different topologies would aim to achieve different objectives, one of such is the Alternate Arm Converter (AAC) which reduces the number of sub-modules used by switching between both arms [87-90]. Others include the controlled transition bridge converter (CTB) which combines series connected "director switches" with sub-modules to improve the power flow [91] and the series bridge converter (SBC) which uses a series combination of sub-modules [92].

1.5 Role of STATCOM in Distribution Networks

Power electronic FACTS devices like STATCOM create more flexibility in controlling the power flow in distribution networks. When these devices are not used, the power flow depends mainly of the impedance between network buses. With a STATCOM connected, the power can be actively controlled using the converter by altering the current flowing through the network. This makes it possible to maintain constant power flow along a desired path when dynamic changes occur and under different loading conditions in the network [93, 94] .

Furthermore, the use of STATCOM allows to extend the useable capacity of existing distribution networks. A network can be made to operate close to its thermal capacity by controlling the power to be close to its thermal rating [93-97]. This optimises the usable capacity of the existing, new and upgraded distribution lines. Moreover, it helps to cool the overheating of cables when the I^2R losses are reduced by eliminating the reactive power across the line [94, 97].

Likewise, the STATCOM can alter the voltage capacity of the network. This is possible when used as voltage regulator during under voltage or over voltage conditions [98]. In under voltage condition, excess reactive current can be generated into the network to increase the voltage above or close to required nominal value. The opposite occurs in an over voltage condition were the converter absorbs reactive current restricting the voltage to its required level [98]. In addition, distribution line parameters tend to have a high (R/L) ratio (more resistive than inductive) due to varying loading conditions. Under such situations, the STATCOM provides support to keep voltage regulated even with the increased I^2R losses [99-102].

1.5.1 Benefits of MMC Based STATCOM

Early STATCOMs were based on either the two level converter or classical multilevel converters topologies such as Neutral point clamped (NPC) and Flying Capacitor converter (FC). Compared to the FC, the NPC has been more applicable industrially because of the lower number of devices used and lower cost. Both topologies have a power circuit structure that increases complexity with higher voltage ratings and the number of voltage steps cannot surpass the power rating of the switching devices. This limits these topologies for medium voltage application in the range of a few kilo-volts 2.3-6.6 kV [103] .

With the introduction of Modular Multilevel Converter (MMC), higher voltage ratings can be achieved with lower voltage stress on the devices. This allows for higher rated STATCOMs that can be installed on the 11kV and 33KV distribution networks. The modular nature of the converter allow for higher number of voltage steps to be achieved resulting to lower filtering size requirements. Hence, with the MMC-STATCOM new opportunities are created to extend power flow control at the higher rated distribution power networks.

1.6 Grid Voltage Synchronisation Schemes

Power electronic converter-based devices applied for the control of active and reactive power flow in the distribution networks should be able to operate under conditions of voltage unbalance and harmonic distortion. This requires the terminal voltages of devices such as the MMC converter-based STATCOMs to be synchronised to the distribution grid voltages. Hence, fast and reliable grid synchronisation schemes have become critical in controlling these converters under abnormal grid conditions. The performance of synchronisation methods should conform to the following desirable features:

- Frequency and Phase Angle Control: Ability to effectively track the frequency and phase variations when the grid voltage frequency or phase angle deviate from their nominal values.
- Harmonic Immunity: Ability to remain synchronised to the grid voltage under adverse harmonic distorted conditions by filtering out the harmonics in the grid voltage.
- Robustness under Unbalance Voltage: Ability to remain synchronised when there is an abnormal voltage condition like voltage sags or unbalanced three phase voltages.
- Fast Response : Responding quickly and accurately to transient changes occurring in the grid voltages.

Grid voltage synchronization schemes can be broadly categorised as open-loop and closed-loop methods. Figure 1.10 illustrates the classification of different schemes under this heading.

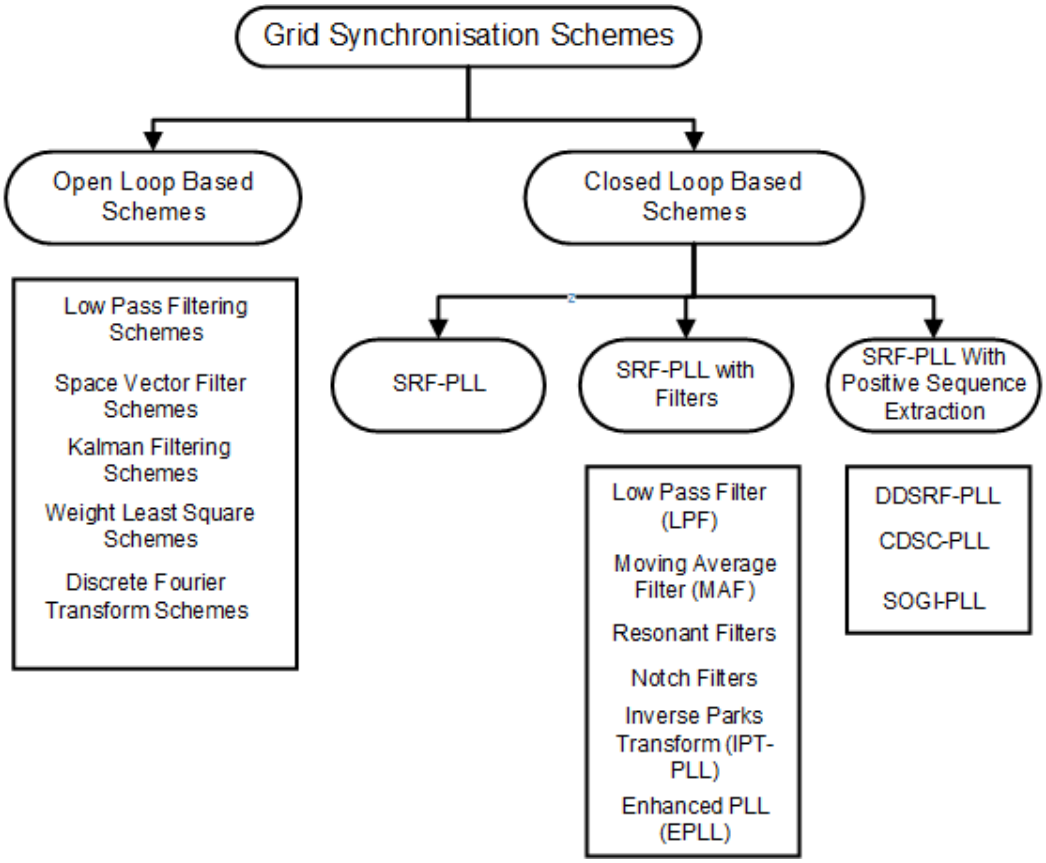


Figure 1.10: Classification of Grid Synchronisation Schemes

1.6.1 Open-Loop Schemes

Open-loop synchronization methods directly estimate the frequency and phase angle of the grid voltage fundamental component. This is done by processing the instantaneous samples of measured voltages as shown in Figure 1.11. They generally have the problems of being sensitive to noise, and some may be unstable due to using short window lengths for data samples. Their performances depend on their ability to filter distorted signals and adaptability to changes in frequency and phase angle of the grid voltages.

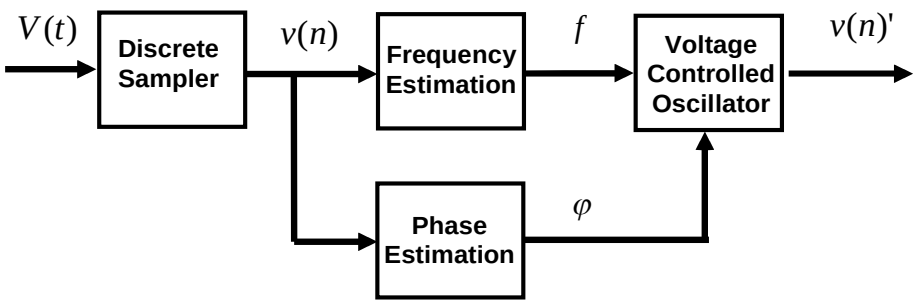


Figure 1.11: Basic structure of an open loop synchronisation technique

The following types of open loop synchronisation techniques have been identified in the literature [104] .

- **Low Pass Filtering (LPF) techniques:** In this approach, the signals are filtered with a low pass filter and the normalised signals are passed through a co-ordinate transformation matrix to compensate for the phase lag due to the low pass filter [105]. The disadvantage is that lower cut off frequencies make the response slower and it is sensitive to both the voltage unbalance and phase jumps [105-107].
- **Space Vector filter (SVF) techniques:** This technique is a low pass filter based on α-β components of the grid voltage. The filter uses a model of the grid voltage which is updated at every sample instant. Assuming the constant sampling time and frequency, the grid voltage is estimated at the next sample [105]. The scheme responds well to phase jumps and harmonic distortion but introduces a phase shift when the frequency changes.
- **Kalman Filtering (KF) techniques:** Kalman filtering is a well-known approach and has been applied extensively for synchronisation [108-111] . These techniques work well under unbalanced voltages, phase angle jumps and harmonic distortion and are frequency adaptive. The drawback here is that they are computationally intensive, have higher convergence times and are difficult in selecting covariance matrices.
- **Weighted Least Squares Estimation: (WLES) techniques:** This technique is used to estimate the positive and negative sequences separately. The response time is fast and it works under frequency variations. However, this scheme is sensitive to harmonic distortion [106, 112].
- **Discrete Fourier Transform (DFT) techniques:** This method is the most stable open-loop algorithm [113-115] and provides good filtering characteristics. There is good synchronisation when the voltage is corrupted with harmonics. However the DFT is prone to errors from frequency variations. This can be improved by either adjusting the window to match with the grid voltage fundamental element period [116] or adding a phase offset to cancel out the error produced using recursive DFT [109, 116, 117].

1.6.2 Closed-Loop Schemes

The key idea in almost all closed-loop schemes is having the phase angle of an internal oscillator aligned with that of the fundamental component of the grid voltage by a control loop. The well-known basic structure consists of three parts: the phase detector, loop filter and voltage controlled oscillator as shown in Figure 1.12. When applied to a balanced three-phase voltage, the phase detector is usually implemented by applying a Park transformation to track the phase angle error of the measured three phase voltage vector and estimated one. The loop filter determines the loop bandwidth and hence having the trade-off between the noise rejection and tracking speed of the scheme.

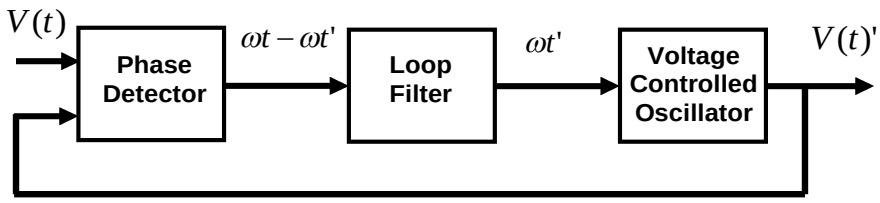


Figure 1.12: Basic structure of a closed loop synchronisation technique

Most closed loop synchronisation schemes are based on using the d-q synchronous reference frame for phase detection (SRF-PLL). Similar approaches are the pq-PLL using instantaneous real and imaginary power theory [118, 119]. Closed loop schemes can be categorized into three:

1.6.2.1 Classical SRF-PLL

This scheme is as shown in Figure 1.13. The phase detector consists of Clarkes and Parks vector transformation matrix. This resolves the three phase voltages into d and q stationary reference frame components based on the expression (1.5).

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \sin\theta & \cos\theta \\ -\cos\theta & \sin\theta \end{bmatrix} \begin{bmatrix} \sin(\theta - \varphi) \\ \cos(\theta - \varphi) \end{bmatrix} \tag{1.5}$$

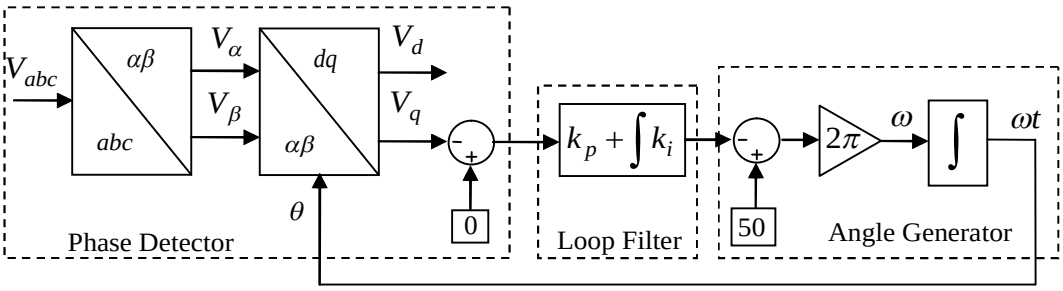


Figure 1.13: Synchronous Reference Frame PLL (SRF-PLL)

To achieve synchronisation, the P+I control (loop filter) and angle generator creates a closed loop feedback control that eliminates phase angle error φ by forcing the q component to be zero. This scheme works well for balanced voltage conditions but once the voltages become unbalanced the presence of negative and zero sequence components imposes a second order harmonic component on the d-q components. Under this condition, the loop filter bandwidth can be lowered to reduce the effect of the second order harmonic component but this causes increased delay in the scheme. The bandwidth (BW) can be set by using the closed loop transfer function of the system parameters in Figure 1.13. This can be expressed as shown in (1.6) and its resultant second order system shown in (1.7).

$$G(s) = \frac{sk_p + k_i}{s^2 + sk_p + k_i} \tag{1.6}$$

$$H(s) = \frac{s2\varsigma\omega_n + \omega_n^2}{s^2 + s2\varsigma\omega_n + \omega_n^2} \tag{1.7}$$

where, ς is the damping ratio and ω_n is the undamped natural frequency.

For a ς value of 0.707 the bandwidth for a second order system BW $\approx \omega_n$.

1.6.2.2 SRF-PLL with Filters

The above scheme can be used for unbalanced voltages and voltages corrupted with harmonics when adequate filters are used. When the measured voltages are transformed into the d-q vector form using the rotating reference frame, the higher frequency harmonics are present on their equivalent DC waveforms. It is possible to dampen the effect of these components using an additional filter placed before the loop filter as shown in Figure 1.14. Different types of filters have been investigated by researchers as possible solutions. Some include using low pass filters (LPF)

[120, 121], moving average filters (MAF) [120, 122, 123] , resonant filters [124] and notch filters [121] . The disadvantage of the added filtering is that in incurs additional delays, leading to slower response time.

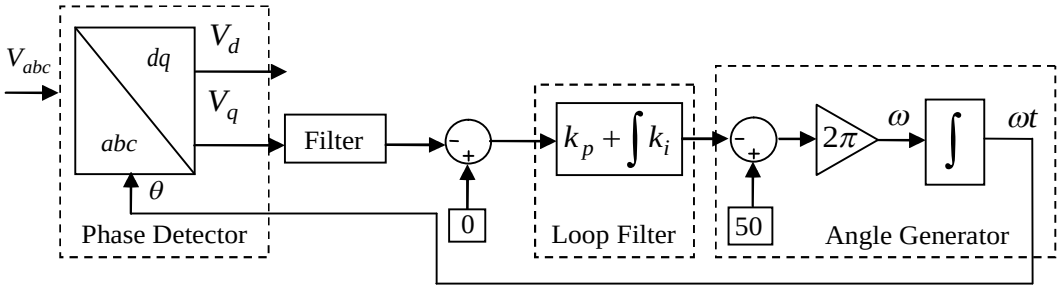


Figure 1.14: Filter +SRF-PLL

1.6.2.3 SRF-PLL with Positive Sequence Extraction

The distinctive feature compared to the classical SRF-PLL is that this works under unbalanced voltage conditions. Before the phase detection the symmetrical components of the grid voltages are extracted by Fortescue Theorem in (Appendix A.2). After extraction, synchronisation is achieved by applying the same SRF-PLL discussed above to the symmetrical positive sequence components of the voltage. Figure 1.15 shows the block diagram for the PLL scheme including positive sequence extraction. Extending with this feature allows for the SRF-PLL to cope under unbalanced voltage conditions. Various PLL schemes that use this method include the double synchronous reference frame (DDSRF-PLL) and cascaded delay signal cancellation (CDSC-PLL). The principles of DDSRF-PLL and CDSC-PLL schemes are described in Appendix B.2.

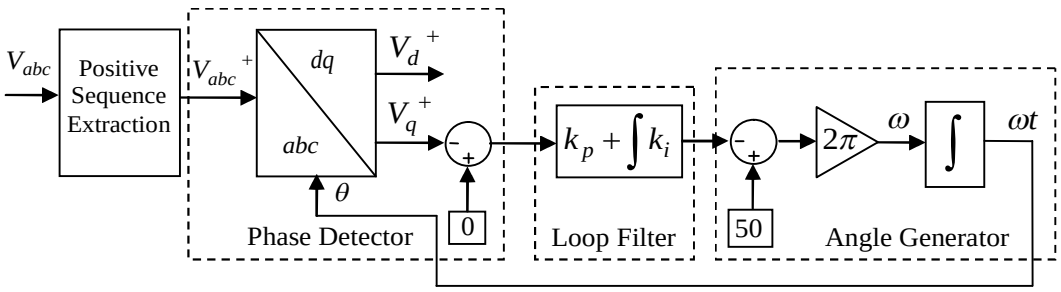


Figure 1.15: Positive Sequence Extraction + (SRF-PLL)

1.7 Aims, Objectives and Thesis Structure

The overall aim of this research is to investigate the practicality of a Flying Capacitor Modular Multilevel Converter-based STATCOM (FC-MMC) for reactive power compensation and voltage control in a distribution system. The key objectives are to:

1. Investigate and assess the performance of MMCs using different converter topologies as sub-modules in terms of power losses, footprint and cost.
2. Investigate the most suitable PWM schemes for the control of a MMC using three-level flying capacitor full-bridge inverter as the sub-module.
3. Analyse the control schemes for the FC MMC based STATCOM and evaluate the operational characteristics under reactive compensation.
4. Develop a novel grid synchronisation technique using the energy operator that could handle synchronisation in various voltage scenarios, balanced or unbalanced.
5. Design, implement and validate an experimental model of the Flying Capacitor Modular Multi-level Converter-based STATCOM for reactive power compensation.

The structure of the thesis is as follows:

Chapter 2

Chapter 2 presents an assessment of sub-module concepts for modular multilevel converters (MMC) under STATCOM applications. Guidelines for assessment are presented and the sub-modules are compared based on five metrics: footprint, cost, power efficiency, control capability and topology. This shows a comparison and explains the reasons for the choice of the Flying Capacitor Modular Multilevel Converter in this study.

Chapter 3

Chapter 3 discusses carrier modulation control techniques for the Flying Capacitor Modular Multilevel Converter. Two carrier based sinusoidal PWM schemes namely; phase disposition PWM (PD-PWM) and phase shifting PWM (PS-PWM) are discussed in detail. Simulation results are presented to validate each approach.

Chapter 4

Chapter 4 presents a novel synchronisation scheme based on the energy operator. It discusses the principles behind the development of the grid synchronisation technique and presents simulation and experimental validation of the technique under different voltage conditions.

Chapter 5

Chapter 5 presents system modelling and simulation of STATCOM for reactive power compensation using the Flying Capacitor Modular Multilevel Converter. Investigation into the voltage rating of the converter and choice of filter parameters in discussed in detail and a simulation study is carried out for reactive compensation under voltage regulation and power factor correction.

Chapter 6

Chapter 6 discusses the experimental system setup. The Hardware build-up components of Flying Capacitor Modular Multilevel Converter and software control using a DSP-FPGA interface in described in detail.

Chapter 7

Chapter 7 discusses the experimental validation of the Flying Capacitor Modular Multilevel Converter under reactive power compensation. Two tests are carried out the first without capacitor feed-back control and the latter with capacitor feed-back control. Experimental results are presented and discussed in detail.

Chapter 8

Chapter 8 summaries the findings made so far made in this research and provide recommendations for future work to be undertaken.

Chapter 2
Modular Multilevel Converter Sub-Module Assessment for STATCOM

A modular multilevel cascaded converter such as that presented by Marquardt *et al* [62] provides several advantages. Most obvious is its ease of scaling achieved by simply cascading additional sub-modules in series within each converter phase arm. Other advantage is multiple voltage levels, which with properly controlled switching can produce an output waveform with reduced harmonics and hence lower filtering requirements. There also include reduced voltage stresses applied to the components and hence enhanced reliability, cost effective design; ease of manufacturing and maintenance due to standardized converter sub-modules; and better operating efficiency. Research on the viability and effectiveness of MMCs intended for HVDC systems has been actively pursued by major world power equipment companies such as Siemens and ABB. Its application in building STATCOM devices for reactive power compensation has also been addressed [64, 66, 68].

The key element in an MMC is its constituent sub-modules and the converter topologies widely used for them are the Half-bridge and H-bridge. Other sub-module types being considered for MMC include the 5-level flying capacitor (FC) Half-bridge and H-bridge converter and a hybrid version which combines a half-bridge FC and a two-level half-bridge together [125]. MMC-based STATCOMs constructed with different types of sub-modules would present different operating characteristics, costs, complexity of control, and space requirements.

This chapter presents an assessment and comparison of four sub-module types used for a MMC-based STATCOM application. These are: Half-bridge, H-bridge, FC Half-bridge and FC H-bridge. Note that in the following discussions, modules and sub-modules are used interchangeably to name the same basic constituent unit in an MMC converter. The subsequent sections describe guidelines for comparing sub-module types under the following five metrics: footprint, cost, efficiency, control capability and topology.

2.1 Sub-Module Circuits Under Study

The four sub-module circuits assessed in this study are shown in Figure 2.1 (a) – (d).

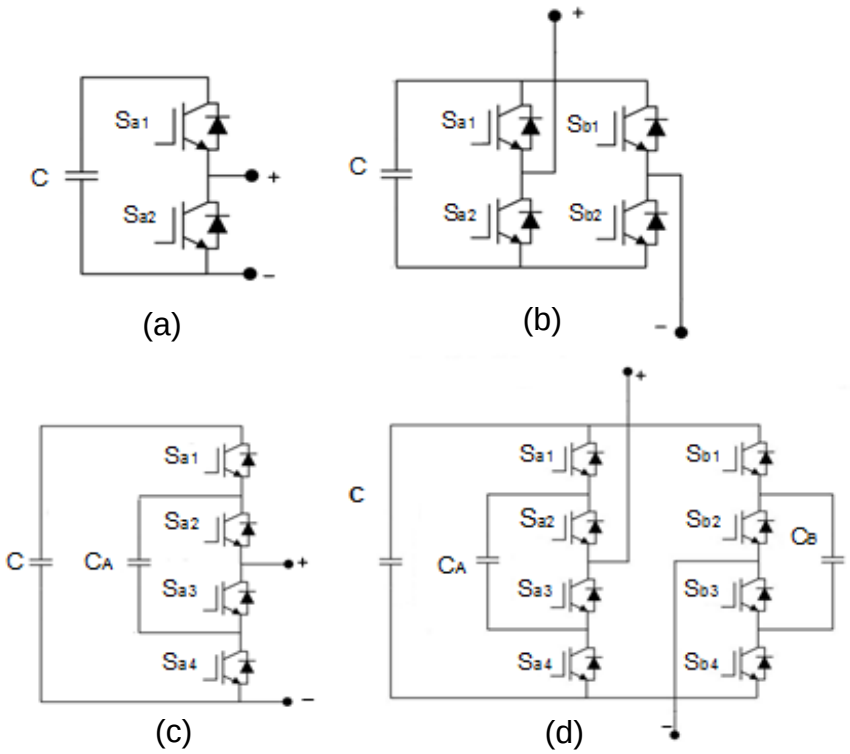


Figure 2.1: MMC Sub-modules (a) Half-Bridge (b) H-bridge (c) FC Half-bridge (d) FC H-bridge

For STATCOM application using the two Half-bridge modules shown in this figure, the double star configuration is required. With H-bridge and FC H-bridge the STATCOM is in a single star configuration. The sub-modules are matched to provide the same voltage rating with the same number of multilevel voltage steps.

2.1.1 Devices and Components for Sub-Modules

Before setting up the guidelines and criteria for the assessment, it is assumed that the STATCOMs to be investigated, regardless of the sub-module used, would be applied to a distribution grid rated at 20 kV. The main components in any of the four sub-modules above are the IGBT switch module comprising two complementary switches, each with an anti-parallel diode connected across it, and a heat sink. In addition there are the electrolytic capacitor and gate drive circuits. Identical devices and components are used for all sub-module topologies given above and these are listed in Table 2.1.

Table 2.1: Devices for Sub-Module Assessment

Device	Manufacturer	Specification
IGBT Switch Module	Infineon IKW30N60T Fisher Elektronics SK105/105SA Heat Sink	600V 30A R_{th} = 2K/W
Capacitor	Panasonic EETED2G561EA	400V, 560µF
Gate Electronics	Actel ProASIC3 FPGA Gate Drive Circuits LEM LV 25 transducers	Only the main parts are considered

Note for the devices listed the following assumptions are made:

1) The thermal dissipation for all IGBT switch heat sinks is rated at 2 kW.
2) Electrolytic capacitors are assumed to be used for all sub-modules, because they are cheaper and smaller. However it is recognised that they have shorter life and lower reliability, so in practice, film capacitors would be a better option due to their superior dielectric properties.
3) The gate drive electronics comprise an FPGA for digital control, transducers for current and voltage measurements and gate drivers.

2.1.2 Numbers of Sub-Modules Required

For building a STATCOM with nominal voltage of 20 kV using different converter topologies, the numbers of sub-modules required are different.

Using two-level half-bridge sub-modules which synthesize unipolar voltage, their corresponding STATCOM is in double star configuration. The total required number of sub-modules is

$$N = \frac{V_{pk-pk}}{V_{SM\ \ pk-pk}} = \frac{2 \times 20kV}{400V} = 100$$

On the other hand with two-level H-Bridge sub-modules the required number of sub-modules is

$$N = \frac{V_{pk-pk}}{V_{SM\ \ pk-pk}} = \frac{2 \times 20kV}{800V} = 50$$

Furthermore, with three-level FC Half-Bridge sub-modules the required number of sub-modules is

$$N = \frac{V_{pk-pk}}{V_{SM\ pk-pk}} = \frac{2 \times 20kV}{800V} = 50$$

Finally, with three-level FC H-Bridge sub-modules the required number of sub-modules is

$$N = \frac{V_{pk-pk}}{V_{SM\ pk-pk}} = \frac{2 \times 20kV}{1600V} = 25$$

2.2 Guidelines for Sub-Module Assessment

This section introduces general guidelines that would be used to assess the four sub-module types under the following five metrics: footprint, cost, efficiency, control capability and topology.

2.2.1 Footprint Assessment Guidelines

Figure 2.2 shows the arrangement and the footprint of an MMC Converter for a practical application according to that used by ABB and Alstom [126-129]. This is based on how the sub-modules are assembled for a MMC converter at the high voltage transmission grid network. It is assumed in this study, that the same arrangement is applied to an MMC-based STATCOM for a distribution grid network.

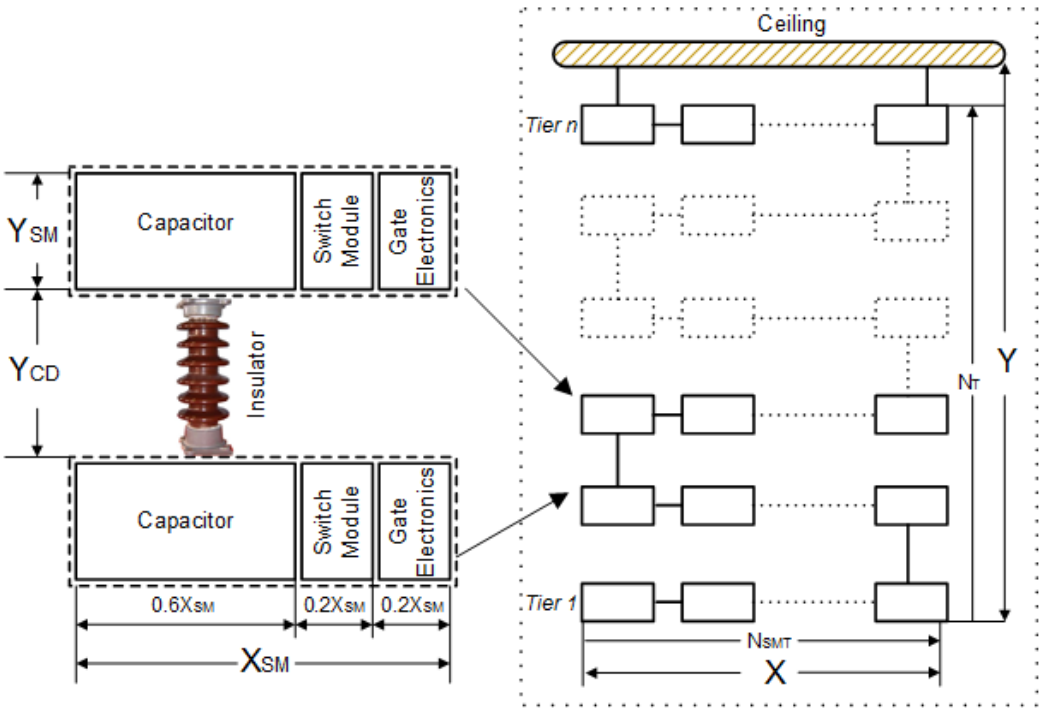


Figure 2.2: Guideline for Footprint Assessment (a) Sub-module Footprint with insulator (b) Platform Footprint with sub-modules

Each sub-module is normally enclosed in a contamination-free enclosure and suspended from the ceiling (earthing plane) of the housing platform as a means of protection against natural disasters like earthquakes [127-129]. The total height of the housing platform depends on the number of sub-modules and is also based on the unified insulation creepage distance (USCD) among each tiers of sub-modules. The recommended insulation gap (Y_{CD}) or unified specific creepage distance (USCD) as specified in IEC 60815 [130] is 3.5cm/kV. This is based on medium level of pollutants within the environment the converter is placed in.

The footprint of a converter is measured based on the total number of sub-modules required for a specified voltage rating and unified specific creepage distance (USCD). This is represented as a function of total width and height of the platform X and width Y respectively as shown in Figure 2.2 (b). Based on this, the footprint can be expressed as

$$\textit{Footprint} = \left(N_T Y_{SM} + (N_T + 1) Y_{CD}\right) \times N_{SMT} X_{SM} \tag{2.1}$$

where, N_T is the number of tiers of sub-modules required

Y_{SM} is the height of each sub-module

N_{SMT} = number of sub-modules in one tier

X_{SM} is the width of each sub-module

Y_{CD} is the tier to tier insulation clearance gap or distance

The tier to tier insulation clearance distance is based on the expression

$$Y_{CD} = USCD \times \frac{Voltage\ Rating\ of\ Converter}{N_T} \tag{2.2}$$

where, $USCD$ = 3.5cm/kV

In this assessment, five tiers are used in the arrangement of all the different sub-module types. Hence the tier - to - tier insulation clearance distance is calculated as

$$Y_{CD} = 3.5cm/kV \times \frac{20kV}{5} = 14cm \tag{2.3}$$

Table 2.2, shows the per-unit size of a sub-module based on the number of power devices.

Table 2.2: Devices and Per-unitised sizes

Device	Size per Sub-module (pu)	Comments
IGBT Switch Module	Width = 20% of X_{SM} = 0.2 Height = 100% of Y_{SM} = 1	$Y_{SM\ is}$ based on Heat Sink having the largest height of 20cm
Capacitor	Width = 60% of X_{SM} = 0.6	Typically around 50-60% of sub-module [126]
Gate Electronics	Width = 20% of X_{SM} = 0.2	

The sizes in the table are chosen so that a Half-bridge sub-module comprising 1 IGBT Module, 1 capacitor and 1 Gate Electronics forms a per-unitised width and height of a sub-module. The height Y_{SM} is based on a heat sink having the largest height of 20 cm and the total width X_{SM} is assumed as three times that at 60 cm. This gives a dimension of 20 cm × 60 cm for a Half-bridge sub-module.

The total number of sub-modules N can also be expressed in terms of the width and height of the platform

$$N = N_{SMT} \times N_T = \frac{V_{pk-pk}}{V_{SM\ pk-pk}} \tag{2.4}$$

In the case of the Half-bridge sub-modules, N_T = 5 and N_{SMT} = 20 giving a per-unitised platform size with a total of 5 tiers with 20 sub-modules per tier. (100 sub-modules).

Similarly, for the H-bridge and FC Half-bridge sub-modules, N_T = 5 and N_{SMT} = 10 giving a per-unitised platform size with a total of 5 tiers with 10 sub-modules per tier. (50 sub-modules)

Finally, for the FC H-bridge sub-modules, N_T = 5 and N_{SMT} = 5 giving a per-unitised platform size with a total of 5 tiers with 5 sub-modules per tier. (25 sub-modules) .

2.2.2 Cost Assessment Guidelines

The cost assessment should be based on the prices of the devices used in building a sub-module from their manufacturers. However the actual prices of these devices in a practical MMC converter are usually not disclosed by their manufacturers. Hence in this study, the assumption made is that the

cost of a sub-module is based on the price of the main devices from the UK Farnell website [131] to build up the practical converter (discussed in Chapter 6) as shown in Table 2.3.

Table 2.3: Price of Devices for One Sub-Module

Device	Manufacturer	Unit Cost (£)
IGBT Switch Module	IKW30N60T(1 pair) Heat Sink x 1	9.14 8.00
Capacitor	Panasonic EETED2G561EA	10.65
Gate Electronics	Actel ProASIC3 FPGA Gate Drive Circuitry LEM LV 25 transducers	6.75 9.1 49.75
		Total: 93.73

*The prices in the table to some degree, give a measure of an actual cost function for an industrial application. In practice, the actual cost of each item may differ.

2.2.3 Efficiency Assessment Guidelines

The efficiency of a sub-module is evaluated based on the device power losses, which are mainly conduction and switching losses. Two power loss calculation methods are available for MMC VSC sub-modules. The first, proposed by C.Oates et al [132], is an analytical method based on mathematical analysis of the power flowing through the converter. The latter method uses an average model detailed in IEC 62751 [133] for VSC-HVDC sub-modules and piecewise linear characteristics of the switches from the manufacturer's application note [134] to obtain conduction and switching losses [135-137]. This method is less cumbersome and is adopted in this work. It is assumed that the same modulation switching scheme is applied to all power devices in the different sub-module types at the same current and voltage rating.

Based on IEC 62751, nine power loss parameters (P_{V1} – P_{V9}) are defined as follows [135]:

P_{V1} – IGBT Conduction Losses

P_{V2} – Diode Conduction losses

P_{V3} – Other Valve Conduction Losses

P_{V4} – DC voltage dependent loss

P_{V5} – DC Capacitor Losses

P_{V6} – IGBT Switching losses

P_{V7} – Diode Turn-off Losses

P_{V8} – Snubber losses

P_{V9} – Valve electronics power consumption.

The study presented here is limited to the IGBT and Diode Conduction and Switching Losses, i.e. P_{V1} ,P_{V2} and P_{V6} ,P_{V7} respectively. These are the dominant contributors of the losses incurred in a sub-module.

Conduction Losses

In MMC converters, the IGBT switches and diodes have some form of resistive element which causes power dissipation when current flows through it. This is regarded as the on-state resistance and causes conduction losses over the conducting period of the switch [138, 139].

MMC converters have a large number of half or H-bridge converters interconnected and conduction loss patterns are stochastic in nature. For this reason, appropriate loss calculation methods are required to estimate conduction losses. This is evaluated either through simulations fed with precise curve fit data for device on-state voltage as a function of current[132, 137] or analytical method based on linear characteristics to achieve average conduction losses [132, 138, 140-143] . A rather simpler approach which has been used successfully for the past 20 years in LCC HVDC schemes [135] uses an approximation whereby the on-state voltage is modelled as a piecewise-linear characteristic as shown in Figure 2.3. This is used in this assessment and is described below

Based on this, the IGBT and diode conduction losses, P_{V1} and P_{V2}, are defined by (2.5) and (2.6) below [134].

$$P_{V1}(t) = V_{CE}(i_C) \cdot i_C(t) = V_{CE0} \cdot i_C(t) + R_{ON\_CE} \cdot {i_C}^2(t) \qquad (2.5)$$

$$P_{V2}(t) = V_F(i_C) \cdot i_C(t) = V_{F0} \cdot i_C(t) + R_{ON\_D} \cdot {i_C}^2(t) \qquad (2.6)$$

where, $V_{CE}(i_C) = V_{CE0} + R_{ON\_CE} \cdot i_C(t)$

V_{CE0} is the IGBT zero current collector-emitter voltage

i_C is the current flowing through the converter phase arm

R_{ON_CE} is the IGBT collector-emitter on-state resistance

$V_F(i_C) = V_{F0} + R_{ON\_D} \cdot i_C(t)$

V_{F0} is the zero current diode forward voltage

R_{on_D} is the diode on-state resistance.

The average losses over a switching period $t - t_0$ can be expressed as

$$P_{V1ave} = \frac{1}{t - t_0} \int_{t_0}^{t} P_{V1}(t) \cdot dt$$

$$P_{V1ave} = V_{CE0} \cdot \frac{1}{t - t_0} \int_{t_0}^{t} i_C(t) \cdot dt + R_{ON\_CE} \cdot \frac{1}{T_{SW}} \int_{t_0}^{t} {i_C}^2(t) \cdot dt$$

where, $t - t_0$ is the conduction period

Thus it is

$$P_{V1ave} = V_{CE0} I_{AVG} + R_{ON\_CE} {I_{RMS}}^2 \quad (2.7)$$

where, I_{AVG} , I_{RMS} are respectively the average and rms currents flowing through the converter phase arm.

Likewise, the diode conduction loss can be expressed as

$$P_{V2ave} = V_{F0} I_{AVG} + R_{on\_D} {I_{RMS}}^2 \quad (2.7)$$

and the total conduction loss is

$$P_{CON} = n_{CS} (P_{V1ave} + P_{V2ave}) \quad (2.8)$$

where,

n_{CS} is the number of complementary switch pairs

Using this method allow for the conduction losses to be calculated simply with the knowledge of V_{CE0} , V_{F0} and R_{ON} . and the time averaged losses are expressed in terms of their RMS and average current values.

The conduction loss is also related to the modulation switching scheme applied to the sub-modules and depends on the on-off state duty ratio of the complementary switches over a fundamental cycle. In practical applications for HVDC, a good approximation of the ratio of IGBT conduction to diode conduction losses under inverter mode is 80:20 for half-bridge and 50:50 for H-bridge sub-modules [135]. This approximation depends on the modulation index and the load power factor [138, 140-143].

Applying the same assumptions here to a STATCOM, the conduction power loss formula (2.8) can be expressed as

$$P_{CON} = n_{CS} (k_{IGBT} P_{V1ave} + k_D P_{V2ave}) \quad (2.9)$$

where, k_{IGBT} = 0.8 and k_D =0.2 for half-bridge sub-modules types

k_{IGBT} = 0.5 and k_D =0.5 for full-bridge sub-modules types

Furthermore, the values of V_{CEO} and V_{F0} can be obtained by piecewise linear interpolation of the I-V characteristics from the Infineon IKW30N60T IGBT datasheet [144]. The collector-emitter and diode on-state resistances (R_{ON_CE}, R_{ON_D}) are derived from the gradient of the I-V curves. These are illustrated in Figure 2.3

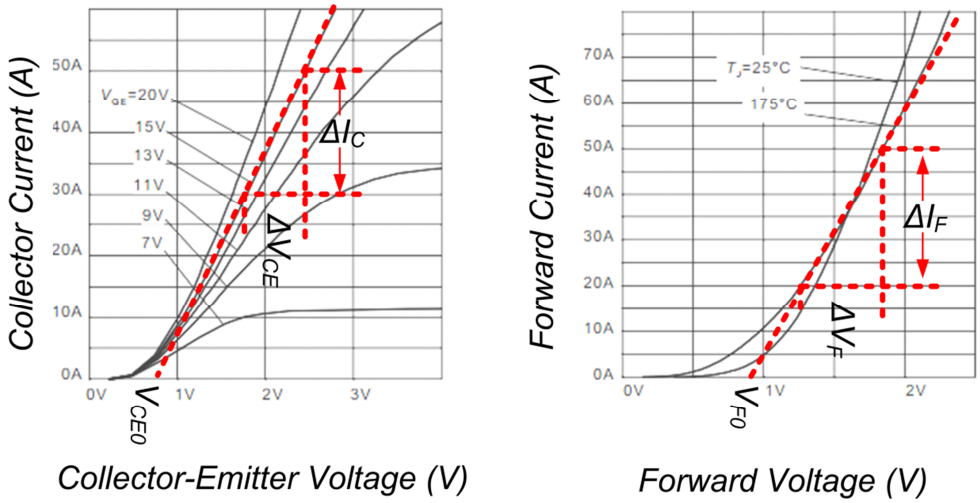


Figure 2.3: Characteristics of the IGBT Collector-Emitter Voltage to current and Diode Forward Voltage to current

Piecewise linear interpolations of the I-V curves in Figure 2.3 show the collector-emitter voltage and diode forward voltage at zero current to be V_{CEO} = 0.75 V and V_{F0} = 0.9 V respectively. Infineon's application note[134] recommends a tolerance margin of 0.4 V should be added to account for saturation characteristics. Hence, the collector-emitter voltage and diode forward voltage used in the work are V_{CEO} = 1.15 V and V_{F0} = 1.3 V respectively.

The on-state resistances (R_{ON_CE}, R_{ON_D}) can be calculated as shown in (2.10) and (2.11) below:

$$R_{ON\_CE} = \frac{\Delta V_{CE}}{\Delta I_C} = \frac{(2.4-1.7)}{(50-20)} = 0.035\Omega \tag{2.10}$$

$$R_{ON\_D} = \frac{\Delta V_F}{\Delta I_F} = \frac{(1.8-1.25)}{(50-20)} = 0.018\Omega \tag{2.11}$$

Having calculated the on and off-state resistance, it only remains to find an expression for the average current I_{AVG}, IGBT and diode zero current forward voltages, V_{CE}, V_F, and the IGBT and diode turn-on resistances, R_{on_CE}, R_{on_D}.

The average current I_{AVG} is related to the number of complementary switch pairs switched in over a fundamental cycle. Assuming half of the total sub-modules with complementary pair switches conduct over the positive half fundamental cycle and the other half over the negative half cycle, with the current following through the phase arm being sinusoidal $\left(i(t) = I_C \sin \omega t\right)$, the average current is expressed as

$$I_{AVG} = \frac{1}{\pi}\int_0^{\pi} I_C \sin \omega t \cdot dt = \frac{2}{\pi} I_C = 0.637 \cdot I_C \tag{2.12}$$

where, I_C is the peak current flowing through the converter phase arm

Switching Losses

The switching power losses occur during the time duration when the IGBT transits between its turn-on and turn-off states. During the IGBT turn-off period, there also is some contribution to switching energy being lost by the anti-parallel diodes. These switching power losses depend on the converter switching frequency, the load current, voltage across the switch and switching characteristics of the semiconductors[138, 140-143, 145-147]. The switching losses P_{SW} are expressed as shown in (2.13) – (2.15).

$$P_{SW} = n_{CS}\, f_{SW}\, (E_{ON} + E_{OFF}) \tag{2.13}$$

$$E_{ON} = f_{SW\_ON}(i_c(t), T_j(t)).\left(\frac{V_{CE}}{V_{CEref}}\right) \tag{2.14}$$

$$\begin{aligned} E_{OFF} &= f_{SW\_OFF}(i_c(t), T_j(t)).\left(\frac{V_{CE}}{V_{CEref}}\right) \\ &\quad + f_{SW\_OFF}(i_f(t), T_j(t)).\left(\frac{V_F}{V_{Fref}}\right) \end{aligned} \tag{2.15}$$

where, E_{ON} is the turn-on energy of the IGBT switch

E_{OFF} is the turn-off energy of the IGBT switch including the diode reverse recovery loss

f_{SW} is the switching frequency

f_{SW_ON} , f_{SW_OFF} are the switching energy function for turn on and turn off energies respectively.

V_{CEref} , V_{Fref} are reference voltages for IGBT and diode energy losses derived from the datasheet.

T_j is the junction temperature if the IGBT.

The energy loss depends on the instantaneous current flowing through the IGBT during each switching period and this varies with changes in the junction temperature of the switch. In two-level converters, calculation of switching losses in is easier because the switching periods are predictable and occur at regular intervals with little or no voltage fluctuations on the DC link. However in MMC converters, this is more complicated as the switching behaviour of the sub-modules are stochastic and less deterministic in nature and digital simulation is required for accurate evaluation of the switching behaviour [132, 135].

With the assumption that the switching events occurring in the MMC are uniformly distributed within a cycle, the simplified expression of the switching losses in (2.13) can be used where it is assumed to have a linear or piecewise correlation which is proportional the current flowing through [135]. In the total effect, the switching losses is the same as they would be if all switching events were taking place at a constant value of current equal to RMS current value. This is used in this assessment with the assumption that a pulse-width modulation scheme at 750 Hz allows for the complementary switch pairs in a sub-module to be switched 15 times during a fundamental cycle.

Furthermore, the IGBT turn-off and turn-off energies depends most importantly on the current following through the device [135] and following these assumption the turn-on and turn-off energies can be estimated from the curve shown in Figure 2.4 which shows the relationship between the switching energy loss and current obtained from the Infineon IKW30N60T IGBT datasheet [134, 144].

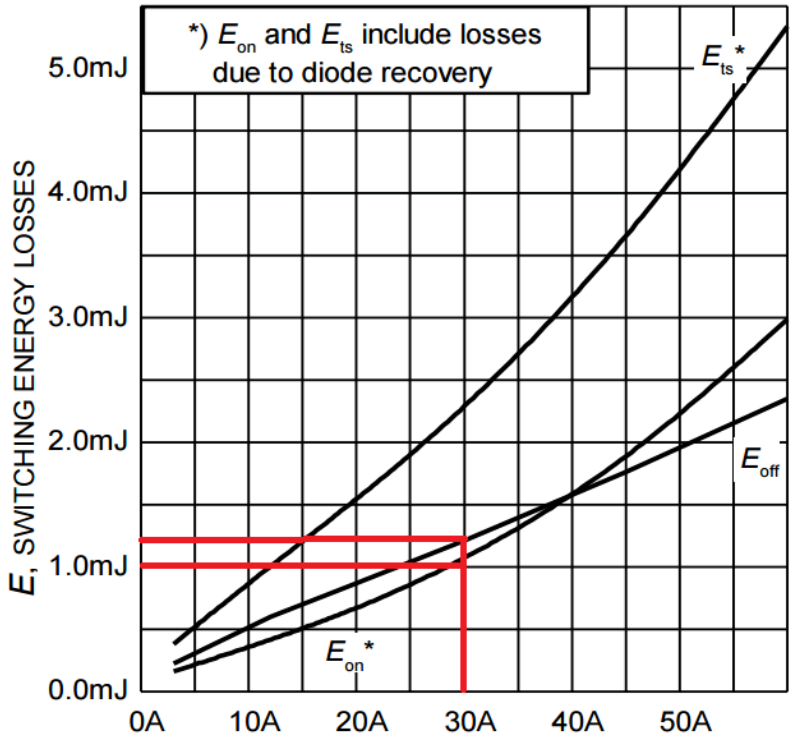


Figure 2.4:Characteristics of the IGBT current and switching energy losses [144].

This gives an energy turn-on loss of 1.0mJ and turn-off loss of 1.1mJ based on the IGBT device working at the rated current of 30A with a V_{CE} voltage of 400V at a junction temperature Tj of 175^{o}C .

Power Efficiency

The total power losses for the converter is a combination of the conduction and switching losses for all the sub-modules in converter and can be expressed as shown in (2.16).

$$P_{LOSS} = n_{SM}\,(P_{CON} + P_{SW}) \tag{2.16}$$

Hence, the power efficiency can be expressed as (2.17)

$$Efficiency\ (\%) = \left(1 - \frac{P_{LOSS}}{P_{CONV}}\right) \times 100 = \left(1 - \frac{P_{LOSS}}{V_{DC}\,I_{DC}}\right) \times 100 \tag{2.17}$$

where, P_{CONV} is the power rating of the converter assuming that the converter operates at its rated power level.

2.2.4 Control Assessment Guidelines

The control assessment is based on the possible ways of charging and discharging capacitors in each sub-module of a 20 kV MMC. This is based on the sub-module being able to charge or discharge its capacitor either during the inverter mode of operation through the switching states or rectifier mode of operation through the diodes. The idle state when no switching signal is applied and the sub-module acts as an uncontrolled rectifier is not considered as operating mode. This state is used as a start-up procedure to charge up the capacitors of the sub-modules in a modular multilevel converter and not under normal operation. In addition, the zero states (by-pass states) when both devices are off are neglected.

2.2.5 Topology Assessment Guidelines

The STATCOM topology assessment is based on the functionality of the configuration of the sub-module for a STATCOM application in either single star or double star MMC. A score based system is used to as a guide to assess the sub-module as shown in Table 2.4.

Table 2.4: Topology Score Based Guide

Topology	**Score**
Support Single-Star STATCOM Configuration	0.5
Support Double-Star STATCOM Configuration	0.5
Total Score	**1**

2.3 Assessment of Different Sub-Module Concepts

The guidelines from the previous section are used to assess the four sub-modules types introduced earlier when used as a STATCOM.

2.3.1 Half-Bridge Sub-Module

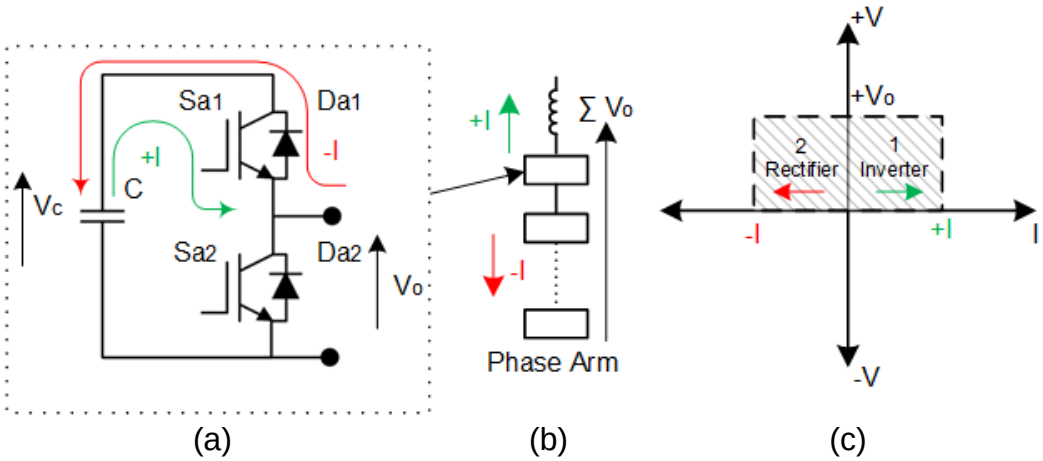


Figure 2.5: Half-bridge Sub-module: (a) Power Circuit showing Rectifier and Inverter Mode (b) Sub-module arrangement for one phase (c) Two Quadrant operation modes

The circuit configuration for this sub-module is as shown in Figure 2.5 (a). It uses only one capacitor connected in parallel with two complementary switches (Sa_1, Sa_2) with anti-parallel diodes (Da_1, Da_2). This has only two switching states and generates unipolar voltage levels, 0 and $+V_o$. Multiple of such sub-modules can be cascaded to obtain higher voltage levels as shown in Figure 2.5 (b). The two quadrant operation modes of this module are as shown in Figure 2.5 (c).

2.3.1.1 Footprint Assessment

Table 2.5 shows the per-unitised width of a half-bridge sub-module based on the number of power devices.

Table 2.5: Per-unit Width of a Half-bridge Sub-module

Device	Quantity	Width (p.u.)
IGBT Switch Module	1	0.2
Capacitor	1	0.6
Gate Electronics	1	0.2
Total X_{SM} in p.u.		**1**

The footprint for the 20kV MMC can be calculated as follows.

N_T = 5 , N_{SMT} = 20 , $Y_{SM} = 20\,cm$ and $X_{SM} = 60\,cm$

$$\textit{Footprint} = \left(N_T Y_{SM} + (N_T + 1)Y_{CD}\right) \times N_{SMT} X_{SM}$$
$$= \left(5 \times 20 + ((5+1) \times 14)\right) \times (20 \times (60 \times 1))$$
$$= 184\,cm \times 1200\,cm = 220800\,cm^2 = 22.08\,m^2$$

2.3.1.2 Cost Assessment

Table 2.6 shows the unit and total cost breakdown of the 20 kV MMC with 100 half-bridge sub-modules.

Table 2.6: Half-Bridge Sub-Module Cost Assessment

Device		Quantity	Unit Cost (£)
IGBT Switch Module		1	17.14
Capacitor		1	10.65
Gate Electronics	Actel ProASIC3 FPGA	1	6.75
	Gate Drive Circuitry	2	18.20
	LEM LV 25 transducers	1	49.75
Unit Cost			**102.49**
Total for 100 Sub-Modules			**10,249.00**

2.3.1.3 Efficiency Assessment

The efficiency for a phase arm of the 20 kV MMC can be calculated as follows.

$R_{ON\_CE} = 0.035\,\Omega$, $R_{ON\_D} = 0.018\ \Omega$, $I_{RMS} = \frac{30}{\sqrt{2}} A$, $I_{DC} = 30\,A$

$I_{AVG} = 0.637 \times 30 = 19.11A$ $V_{CE0} = 1.15V$, $V_{F0} = 1.3V$, $k_{IGBT} = 0.8$, $k_D = 0.2$

$$P_{V1ave} = \left(0.8 \times 1.15 \times 19.11\right) + 0.8 \times 0.035 \times \left(\frac{30}{\sqrt{2}}\right)^2 = 30.18W$$

$$P_{V2ave} = (0.2 \times 1.3 \times 19.11) + 0.2 \times 0.018 \times \left(\frac{30}{\sqrt{2}}\right)^2 = 6.59W$$

$$P_{CON} = 1 \times (30.18 + 6.59) = 36.77W$$

$$P_{SW} = 1 \times 750 \times (1.0 + 1.1) \times 10^{-3} = 1.575\,W$$

$$P_{LOSS\ \ 20\,KV} = 100 \times (36.77 + 1.575) = 3834.50\,W$$

$$Efficiency\,(\%) = \left(1 - \frac{3834.50}{20 \times 10^3 \times 30}\right) \times 100 = 99.36\,\%$$

2.3.1.4 Control Assessment

Table 2.7 shows the valid switching states for switch-diode pairs for rectifier and inverter modes of operation and Table 2.8 the total number of ways to charge and discharge capacitors.

Table 2.7: Switch and Diode States for Rectifier and Inverter Mode of Operations

Switch State		**Diode State**		**Vo**	**Rectifier Mode**	**Inverter Mode**
Sa_1	**Sa_2**	**Da_1**	**Da_2**		**I↑**	**I↓**
-	-	1	0	V_C	C↑	-
1	0	-	-	V_C	-	C↓

*↑= Charging, ↓= Discharging,

Table 2.8: Possible Ways to Charge and Discharge Capacitors

Mode of Operation	**No. of Ways Per Sub-module**		**Unit Total**
	Charging	**Discharging**	
Inverter Mode	0	1	**2**
Rectifier Mode	1	0	
Total No. of Ways (x 100 sub-modules)			**200**

The table shows that for half-bridge sub-modules there is only one way to charge and discharge the capacitor of each sub-module during operation. For the 20 kV STATCOM this gives a total of 200 ways to charge and discharge the capacitors.

There is also no inverter operation mode to charge the capacitors, so charging through rectifier mode employs feedback active power control during operation.

2.3.1.5 Topology Assessment

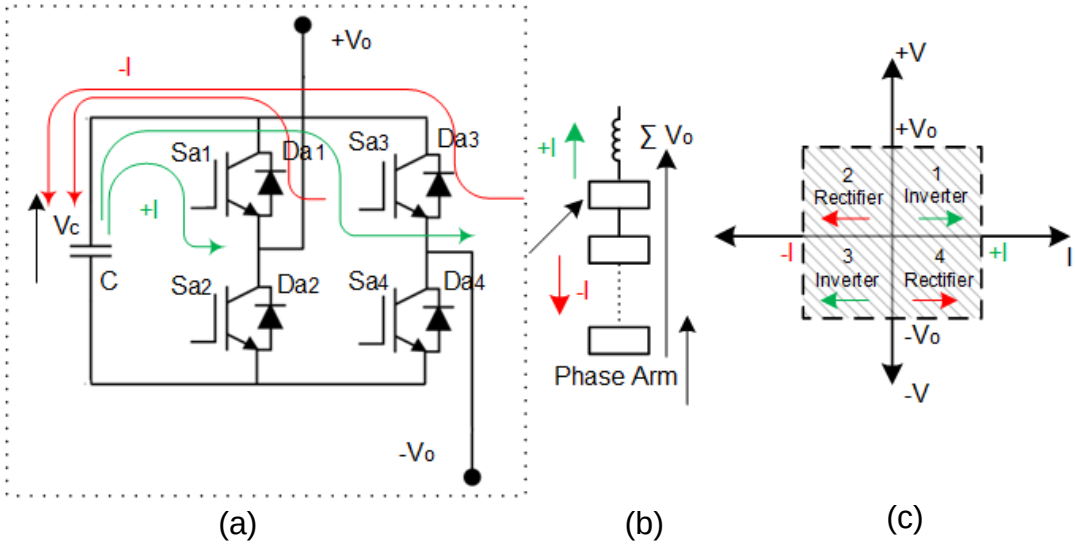
Table 2.9 shows the topology assessment of the half-bridge sub-module

Table 2.9: Topology Assessment of Half-Bridge Sub-Module

Topology	Score
Support Single-Star STATCOM Configuration	0
Support Double-Star STATCOM Configuration	0.5
Total Score	**0.5**

Due to its unipolar voltage nature the half-bridge can only be applied as a Double Star STATCOM.

2.3.2 H-Bridge Sub-Module



(a) (b) (c)

Figure 2.6:H-bridge Sub-module: (a) Power Circuit showing Rectifier and Inverter Modes (b) Sub-module arrangement for one phase (c) Four Quadrant operation modes

H-bridge sub-module is a topology used mostly for building single star MMC STATCOM. The circuit diagram is as shown in Figure 2.6 (a). Each sub-module is supplied by a capacitor connected in parallel with two pairs of complementary switches (Sa_1 Sa_2) , (Sa_3 Sa_4) with anti-parallel diodes (Da_1 Da_2), (Da_3 Da_4). This sub-module generates three distinct voltage levels, (0, $+V_0$, - V_0); and can be easily cascaded to obtain higher voltage levels. The bipolar voltage nature allows for a four quadrant operation with power flow in both directions as shown in Figure 2.6 (c). Quadrants 1 and 3 are the inverting mode of operation and allows for discharging the outer capacitor. C, when current flows in positive direction. Quadrants 2 and 4 are the

rectifier mode of operation and allow for charging the outer capacitor C when current flows in the negative direction.

2.3.2.1 Footprint Assessment

Table 2.10 shows the per-unit width of a H-bridge sub-module.

Table 2.10: Per-unit Width of a H-bridge Sub-module

Device	Quantity	Width (p.u.)
IGBT Switch Module	2	0.4
Capacitor	1	0.6
Gate Electronics	1	0.2
Total X_{SM} in p.u.		**1.2**

Using this sub-module, the Footprint for a 20 kV MMC can be calculated as follows

N_T = 5, N_{SMT} = 10 , $Y_{SM} = 20\,cm$ and $X_{SM} = 60\,cm$

$$\textit{Footprint} = \left(N_T Y_{SM} + (N_T + 1)Y_{CD}\right) \times N_{SMT} X_{SM}$$
$$= \left(5 \times 20 + ((5+1) \times 14)\right) \times (10 \times (60 \times 1.2))$$
$$= 184\,cm \times 720\,cm = 132480\,cm^2 = 13.25\,m^2$$

2.3.2.2 Cost Assessment

Table 2.11 shows the breakdown of unit and total cost of the 20 kV MMC with 50 H-bridge sub-modules.

Table 2.11:Half-Bridge Sub-Module Cost Assessment

Device		Quantity	Unit Cost (£)
IGBT Switch Module		2	34.28
Capacitor		1	10.65
Gate Electronics	Actel ProASIC3 FPGA	1	6.75
	Gate Drive Circuitry	4	36.40
	LEM LV 25 transducers	1	49.75
Unit Cost			**137.83**
Total for 50 Sub-Modules			**6,891.50**

2.3.2.3 Efficiency Assessment

The efficiency for the 20 kV MMC can be calculated using the same method as that for half-bridge module as follows. Note that R_{ON_CE} and R_{ON_CE} have the same values and $k_D = 0.5$ k_{IGBT} = 0.5, so IGBT and diode average power losses are given as

$$P_{V1ave} = (0.5 \times 1.15 \times 19.11) + 0.5 \times 0.035 \times \left(\frac{30}{\sqrt{2}}\right)^2 = 18.86W$$

$$P_{V2ave} = (0.5 \times 1.3 \times 19.11) + 0.5 \times 0.018 \times \left(\frac{30}{\sqrt{2}}\right)^2 = 16.47W$$

$$P_{CON} = 2 \times (18.86 + 16.47) = 70.66W$$

Their switching losses are

$$P_{SW} = 2 \times 750 \times (1.0 + 1.1) \times 10^{-3} = 3.15\,W$$

$$P_{LOSS\ 20\,KV} = 50 \times (70.66 + 3.15) = 3690.50\,W$$

So the efficiency is

$$Efficiency\ (\%) = \left(1 - \frac{3690.5}{20 \times 10^3 \times 30}\right) \times 100 = 99.38\%$$

2.3.2.4 Control Assessment

Table 2.12 shows the valid switching states for switches and diodes for both rectifier and inverter operations and Table 2.13 lists the total number of ways to charge and discharge capacitors in the 20 kV STATCOM.

Table 2.12:Switch and Diode States for Rectifier and Inverter Mode of Operation

Switch State				**Diode State**				**Vo**	**Rectifier Mode**	**Inverter Mode**
Sa_1	**Sa_2**	**Sa_3**	**Sa_4**	**Da_1**	**Da_2**	**Da_3**	**Da_4**		**I↑**	**I↓**
-	-	-	-	0	1	1	0	$-V_C$	C ↑	-
-	-	-	-	1	0	0	1	$+V_C$	C ↑	-
0	1	1	0	-	-	-	-	$-V_C$	-	C ↓
1	0	0	1	-	-	-	-	$+V_C$	-	C ↓

*↑= Charging, ↓= Discharging

Table 2.13: Possible Ways to Charge and Discharge Capacitors

Mode of Operation	**No. of Ways Per Sub-Module**		**Unit Total**
	Charging	**Discharging**	
Inverter Mode	0	2	**4**
Rectifier Mode	2	0	
Total No. of Ways (x 50 sub-modules)			**200**

The table shows for a H-bridge sub-module, there are two ways to charge and discharge the sub-module capacitor . For the 20 kV STATCOM this gives a total of 200 ways to charge and discharge the capacitors.

There are no switching states with the inverter modes that allow the outer capacitor (C) to charge. The capacitor is charged only through the rectifier mode and this can be implemented by using one feedback control.

2.3.2.5 Topology Assessment

Table 2.14 shows the topology assessment of the H-bridge sub-module

Table 2.14: Topology assessment of the H-bridge sub-module

Topology	**Score**
Support Single-Star STATCOM Configuration	0.5
Support Double-Star STATCOM Configuration	0.5
Total Score	**1.0**

Due to its bipolar voltage nature the H-bridge can be used to build STATCOMs in either Single Star or Double Star configuration.

2.3.3 FC-Half-Bridge Sub-Module

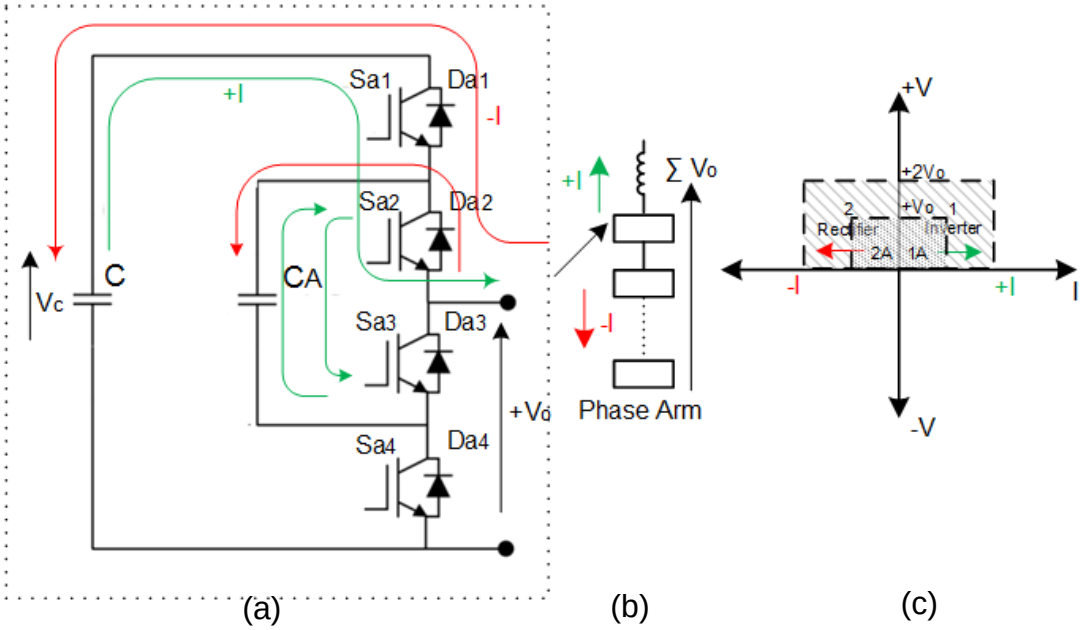


Figure 2.7: FC Half-bridge Sub-module: (a) Power Circuit showing Rectifier and Inverter Modes (b) Sub-module arrangement for one phase (c) I-V two Quadrant operations

The FC Half-bridge circuit configuration is as shown in Figure 2.7 (a). It consists of an outer capacitors (C) and an inner floating capacitor (C_A) connected in parallel with two complementary switch pairs (Sa_1,Sa_4) (Sa_2,Sa_3) with their corresponding anti-parallel diodes (Da_1 Da_4), (Da_2 Da_3) respectively. This sub-module generates three voltage levels, (0, $+V_0$, $+2V_0$). It has two quadrant operation modes (±I,+V) as shown in Figure 2.7 (c), Quadrants 1 for inversion and 2 for rectification. The charging and discharging of the outer capacitor (C) happens in quadrant 2 and quadrant 1 respectively, For inner capacitor C_A, which has only a half of the outer capacitor voltage, it can be charged in quadrant 1 by outer capacitor C when both Sa_1 and Sa_3 are turned on. C_A is also charged in quadrant 2 rectifier mode when switches Sa_2 and Sa_4 are on. Discharging of C_A occurs when in quadrant 1 at ½ V_O.

2.3.3.1 Footprint Assessment

Table 2.15 shows the per-unitised width of a FC Half-bridge Sub-module.

Table 2.15: Per-unit Width of a FC Half-Bridge Sub-Module

Device	Quantity	Width (p.u.)
IGBT Switch Module	2	0.4
Capacitor	3	1.8
Gate Electronics	1	0.2
Total X_{SM} in p.u.		**2.4**

.

The Footprint for the 20 kV MMC can be calculated as follows.

N_T = 5 , N_{SMT} = 10 , $Y_{SM} = 20\,cm$ and $X_{SM} = 60\,cm$

$$\textit{Footprint} = \left(N_T Y_{SM} + (N_T + 1)Y_{CD}\right) \times N_{SMT} X_{SM}$$

$$= \left(5 \times 20 + ((5+1) \times 14)\right) \times (10 \times (60 \times 2.4))$$

$$= 184\,cm \times 1440\,cm = 264960\,cm^2 = 26.50\,m^2$$

This is about 4.4 m^2 higher than that using the half-bridge sub-module, due to the additional inner capacitors, even though the number of modules is reduced by a half.

2.3.3.2 Cost Assessment

Table 2.16 shows the unit and total cost breakdown of the 20 kV MMC with 50 FC Half-bridge sub-modules.

Table 2.16:Half-Bridge Sub-Module Cost Assessment

Device		Quantity	Unit Cost (£)
IGBT Switch Module		2	34.28
Capacitor		3	31.95
Gate Electronics	Actel ProASIC3 FPGA	1	6.75
	Gate Drive Circuitry	4	36.40
	LEM LV 25 transducers	2	99.50
Unit Cost			**208.88**
Total for 50 Sub-Modules			**10,444.00**

2.3.3.3 Power Efficiency Assessment

The power efficiency for the 20 kV MMC can be calculated as follows $k_D = 0.2$

$$P_{V1ave} = (0.8 \times 1.15 \times 19.11) + 0.8 \times 0.035 \times \left(\frac{30}{\sqrt{2}}\right)^2 = 30.18W$$

$$P_{V2ave} = (0.2 \times 1.3 \times 19.11) + 0.2 \times 0.018 \times \left(\frac{30}{\sqrt{2}}\right)^2 = 6.59W$$

$$P_{CON} = 2 \times (30.18 + 6.59) = 73.54W$$

$$P_{SW} = 2 \times 750 \times (1.0 + 1.1) \times 10^{-3} = 3.15\,W$$

$$P_{LOSS\ 20\,KV} = 50 \times (73.54 + 3.15) = 3834.5W$$

$$Efficiency\ (\%) = \left(1 - \frac{3834.5}{20 \times 10^3 \times 30}\right) \times 100 = 99.36\%$$

2.3.3.4 Control Assessment

Table 2.17 shows the valid switching and diode states for rectifier and inverter mode of operation of the FC Half-bridge sub-module and Table 2.18 the total number of ways to charge and discharge capacitors.

Table 2.17:Switching and Diode States for Rectifier and Inverter Mode of Operation

Switch State				**Diode State**				**Vo**	**Rectifier Mode**	**Inverter Mode**
Sa_1	**Sa_2**	**Sa_3**	**Sa_4**	**Da_1**	**Da_2**	**Da_3**	**Da_4**		**I↑**	**I↓**
-	-	-	-	1	1	0	0	$2V_C$	C↑	-
1	0	1	0	-	-	-	-	V_C	-	C↓ C_A↑
1	1	0	0	-	-	-	-	$2V_C$	-	C↓
0	1	0	1	-	-	-	-	V_C	-	C_A↓
0	1	0	1	0	1	0	0	V_C	C_A↑	-
1	0	1	0	1	0	0	0	V_C	C_A↓ C↑	-

*↑= Charging, ↓= Discharging

Table 2.18:Possible Ways to Charge and Discharge Capacitors

Mode of Operation	**No. of Ways Per Sub-Module**		**Unit Total**
	Charging	**Discharging**	
Inverter Mode	1	2	6
Rectifier Mode	2	1	
Total No. of Ways (x 50 sub-modules)			**300**

The table shows for a FC Half-bridge sub-module, they are 3 ways to charge and 3 ways to discharge the capacitor of each sub-module during operation. This gives a total of 300 ways to charge and discharge the capacitors**.**

Compared to half-bridge and H-bridge sub-modules, it is now possible to charge inner floating capacitor C_A using switching states during the inverting mode. This can be exploited to charge and discharge C_A without the need for a feedback control.

2.3.3.5 Topology Assessment

Table 2.19 shows the topology assessment of the FC half-bridge sub-module

Table 2.19: Topology assessment of the FC Half-Bridge Sub-Module

Topology	**Score**
Support Single-Star STATCOM Configuration	0
Support Double-Star STATCOM Configuration	0.5
Total Score	**0.5**

Due to its unipolar voltage nature the FC half-bridge sub-module can only be applied as a Double Star STATCOM.

2.3.4 FC H-Bridge Sub-Module

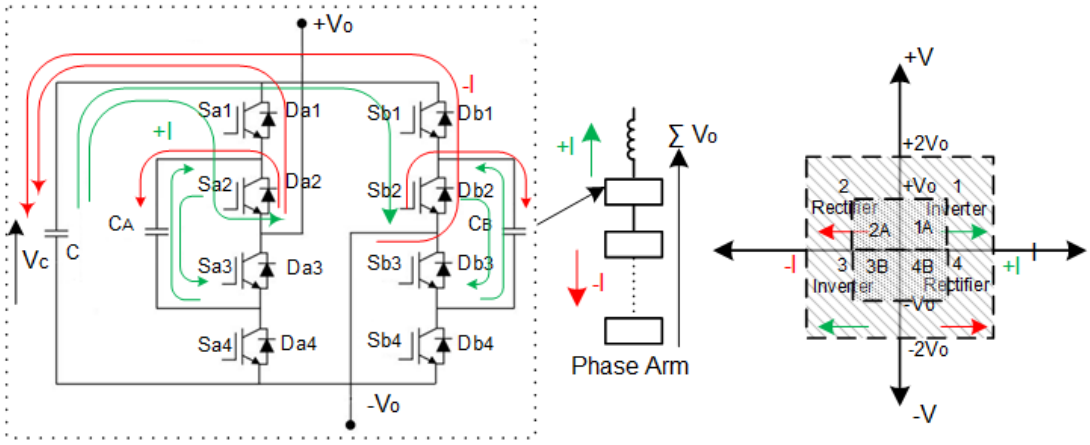


Figure 2.8:FC H-bridge Sub-module: (a) Power Circuit showing Rectifier and Inverter Mode (b) Sub-module arrangement for one phase (c) I-V four Quadrant operations

The configuration of this sub-module is based on combining two FC half-bridge converters connected across each other with a common outer capacitor (C)as shown in Figure 2.8 (a). It consists of one outer capacitor (C) and two inner floating capacitors (C_A, C_B) connected in parallel with four complementary switch pairs (Sa_1,Sa_4),(Sa_2,Sa_3), (Sb_1,Sb_4) and (Sb_2,Sb_3) and their corresponding anti-parallel diodes respectively. This generates five bipolar voltage levels, (0, $+V_C$, $+2V_C$, $-V_C$, $-2V_C$) and can be easily stacked to obtain higher voltage levels. There are four quadrant operation modes (±I,±V) as shown in Figure 2.8 (c).

2.3.4.1 Footprint Assessment

Table 2.20 shows the per-unitised width of a FC H-bridge sub-module

Table 2.20: Per-unit Width of a FC Full-bridge Sub-module

Device	Quantity	Width (p.u.)
IGBT Switch Module	4	0.8
Capacitor	4	2.4
Gate Electronics	1	0.2
Total X_{SM} in p.u.		3.4

The Footprint for the 20 kV MMC can be calculated as follows.

N_T = 5 , N_{SMT} = 5 , $Y_{SM} = 20\,cm$ and $X_{SM} = 60\,cm$

$$\textit{Footprint} = \left(N_T Y_{SM} + (N_T + 1) Y_{CD}\right) \times N_{SMT} X_{SM}$$
$$= \left(5 \times 20 + ((5+1) \times 14)\right) \times (5 \times (60 \times 3.4))$$
$$= 184\,cm \times 1020\,cm = 187680\,cm^2 = 18.77\,m^2$$

This is more than 5m^2 higher than that using H-bridge as sub-modules. With two additional inner capacitors this is expected. However the total number of sub-modules is reduced.

2.3.4.2 Cost Assessment

Table 2.21 shows the unit and total cost breakdown of the 20 kV MMC with 25 FC H-bridge sub-modules.

Table 2.21:H-Bridge Sub-Module Cost Assessment

Device		Quantity	Unit Cost (£)
IGBT Switch Module		4	68.58
Capacitor		4	42.60
Gate Electronics	Actel ProASIC3 FPGA	1	6.75
	Gate Drive Circuitry	8	72.80
	LEM LV 25 transducers	3	149.25
Unit Cost			**339.98**
Total for 25 Sub-Modules			**8,499.50**

2.3.4.3 Efficiency Assessment

The efficiency for the 20 kV MMC can be calculated as follows. $k_D = 0.5$

$$P_{V1ave} = \left(0.5 \times 1.15 \times 19.11\right) + 0.5 \times 0.035 \times \left(\frac{30}{\sqrt{2}}\right)^2 = 18.86W$$

$$P_{V2ave} = (0.5 \times 1.3 \times 19.11) + 0.5 \times 0.018 \times \left(\frac{30}{\sqrt{2}}\right)^2 = 16.47W$$

$$P_{CON} = 4 \times (18.86 + 16.47) = 141.32W$$

$$P_{SW} = 4 \times 250 \times (1.0 + 1.1) \times 10^{-3} = 6.3W$$

$$P_{LOSS\ 20\,KV} = 25 \times (141.32 + 6.3) = 3690.5W$$

$$\textit{Efficiency}\ (\%) = \left(1 - \frac{3690.5}{20 \times 10^3 \times 30}\right) \times 100 = 99.38\%$$

2.3.4.4 Control Assessment

Table 2.22 shows the valid switching states for switches and diodes for rectifier and inverter mode of operation of the FC H-bridge sub-module and Table 2.23 the total number of ways to charge and discharge the capacitors

Table 2.22:Switching and Diode States for Rectifier and Inverter Modes

Switch State				Diode State				Vo	Rectifier Mode	Inverter Mode
Sa_1 Sb_1	Sa_2 Sb_2	Sa_3 Sb_3	Sa_4 Sb_4	Da_1 Db_1	Da_2 Db_2	Da_3 Db_3	Da_4 Db_4		I↑	I↓
- -	- -	- -	- -	1 0	1 0	0 1	0 1	$+2V_C$	C ↑	-
- -	- -	- -	- -	0 1	0 1	1 0	1 0	$-2V_C$	C ↑	-
0 0	1 0	0 1	1 1	0 0	1 0	0 1	0 0	$+V_C$	C_A ↑	
1 0	0 0	1 1	0 1	1 0	0 0	0 0	0 1	$+V_C$	C_A ↓ C ↑	-
0 0	0 1	1 0	1 1	0 0	0 1	1 0	0 0	$-V_C$	C_B ↑	
0 1	0 0	1 1	1 0	0 1	0 0	0 0	1 1	$-V_C$	C_B ↓ C ↑	
0 1	0 1	1 0	1 0	-	-	-	-	$-2V_C$	-	C ↓
0 1	0 0	1 1	1 0	-	-	-	-	$-V_C$	-	C ↓ C_B ↑
0 0	0 1	1 0	1 1	-	-	-	-	$-V_C$	-	C_B ↓
1 0	1 0	0 1	0 1	-	-	-	-	$+2V_C$	-	C ↓
1 1	1 0	0 1	0 0	-	-	-	-	$+V_C$	-	C_B↓
1 0	1 1	0 0	0 1	-	-	-	-	$+V_C$	-	C ↓ C_B ↓
1 0	0 0	1 1	0 1	-	-	-	-	$+V_C$	-	C ↓ C_A ↑
0 0	1 0	0 1	1 1	-	-	-	-	$+V_C$	-	C_A ↓

1 1	0 1	1 0	0 0	-	-	-	-	$-V_C$	-	$C_A \downarrow$
0 1	1 1	0 0	1 0	-	-	-	-	$-V_C$	-	$C \downarrow C_A \downarrow$

*↑= Charging, ↓= Discharging

Table 2.23:Possible Ways to Charge and Discharge Capacitors

Mode of Operation	**No. of Ways Per Sub-Module**		**Unit Total**
	Charging	**Discharging**	
Inverter Mode	2	8	16
Rectifier Mode	4	2	
Total No. of Ways (x 25 sub-modules)			**400**

The table shows for a FC H-bridge sub-module they are 6 ways to charge and 10 ways to discharge both the outer and inner capacitors of each sub-module over a complete switching cycle. For the 20 kV STATCOM this gives a total of 400 ways to charge and discharge the capacitors.

There are also two inverter modes of operation to charge the inner floating capacitor (C_A ,C_B) and these can be exploited to reduce feedback controls of the inner floating capacitor by charging and discharging through the inverter mode of operation using switching states.

2.3.4.5 Topology Assessment

Table 2.24 shows the topology assessment of the FC H-bridge sub-module

Table 2.24: Topology assessment of the FC H-bridge Sub-Module

Topology	**Score**
Supports Single-Star STATCOM Configuration	0.5
Supports Double-Star STATCOM Configuration	0.5
Total Score	**1.0**

2.4. Discussion and Comparison of Sub-Module Concepts for STATCOM

Table 2.25: Comparison of Sub-Module Concepts based on a 20 kV MMC STATCOM

Assessment	Half-Bridge	H-Bridge	FC Half-Bridge	FC H-bridge
Footprint (m^2)	22.08	13.25 ✓	26.50	18.77
Cost (£)	10,249	6,891 ✓	10,444	8,499
Power Efficiency (%)	99.36	99.38 ✓	99.36	99.38 ✓
Control	200	200	300	400 ✓
Topology (Score)	0.5	1 ✓	0.5	1 ✓

Table 2.25 summarises the assessment of the performance of the sub-module concepts for STATCOM application. Based on the results in this table, the following conclusions can be drawn

- **Half-bridge**: This sub-module has a larger footprint and higher cost compared to the H-bridge and FC H-bridge. This is because for STATCOM application this topology can only be in a double star configuration and hence requires twice the numbers of sub-modules and capacitors. It also has a lower power efficiency and the least control capability in shaping the output voltage waveform. This sub-module would be suitable for HVDC application that offers an additional STATCOM functionality.

- **FC Half-bridge**: Similar to the Half-bridge case, this topology is also limited to a double star configuration for STACTOM application. However, it may be the least applicable for STATCOM as it has the largest footprint, highest cost and a lower power efficiency. The only favourable feature is that it provides more control options compared to the Half-bridge and H-bridge sub-modules.

- **H-Bridge:** This sub-module has the smallest footprint, lowest cost and the highest efficiency and can be used in both single and double star STATCOM. It also has the same control capability as the Half-

bridge. Hence for STATCOM application this provides the most favourable features and may be the best choice amongst the four others. This differs from the HVDC application which commonly uses the half-bridge sub-module.

- **FC H-bridge:** This sub-module is second amongst the four in terms of smaller footprint and lower cost. It can also achieve the same power efficiency as the H-bridge provided the switching actions are controlled properly. The topology can be used in both single and double star configuration for STATCOM. In terms of control, it offers the most control capability. Though the two additional inner capacitors may incur the issue of voltage imbalance, this can be resolved effectively by adequate selection of switching state sequence to ensure equal charging and discharging over a cycle. Hence, the total feedback control loop can be reduced as there might not be a necessary need of all the inner capacitor feedback control.

- **General Statements**: In this assessment,
  (a) The cost of building a STATCOM using either H-bridge or FC H-bridge sub-modules is generally lower than that of a half-bridge or FC half-bridge.
  (b) The additional cost of the difference in platform per m^2 might also increase the total cost.
  (c) All the sub-modules exhibit a power loss of approximately 0.6% but the H-bridge and FC H-bridge are shown to be the most efficient.

2.5. Summary

This chapter has shown detailed assessment and comparison of four MMC sub-module concepts for STATCOM applications, with respect to the footprint, cost, power efficiency, control and topology. Based on this assessment the H-bridge sub-module presents the lowest footprint, cost and losses making it the best choice for STATCOM applications and it is currently the preferred choice in industry. However, the investigations have shown that the FC H-bridge sub-module presents most of the control options and can reduce the number of control feedback loops required for capacitors. This makes the converter more flexible, and more suitable, for dynamic medium voltage applications.

Based on this assessment, the author in the following chapters investigate the feature of increased control of capacitors to minimise the number of feedback control loops using the FC H-bridge as a STATCOM. For the remainder of this write-up, the nomenclature FC-MMC representing “Flying Capacitor – MMC” would be used to simplify the description of an MMC with H-bridge flying capacitor sub-modules

Chapter 3
Pulse Width Modulation Schemes for FC-MMC

Pulse width modulation (PWM) control is a well-researched and known technique for controlling voltage source converters [57, 148-150] . In literature, extensive work on the methods and techniques of applying PWM control for modular multi-level converters (MMC) has been reported. This chapter investigates the application of two well-known carrier based sinusoidal PWM schemes namely; phase disposition PWM (PD-PWM) and phase shifting PWM (PS-PWM) for a modular multi-level converter (MMC) consisting of H-bridge flying capacitor sub-modules.

Both these schemes are assessed and compared based on three performance criteria; the output voltage total harmonic distortion (THD) , the optimal utilisation of their sub-modules and natural balancing control of their inner flying capacitors.

The chapter is so organised that the first section describes the fundamental principles of the sine-triangle based PWM schemes. The subsequent sections detail the principles of PD-PWM and PS-PWM schemes and their comparison for STATCOM application for a FC-MMC converter with nine voltage levels (peak to peak). Matlab Simulink software package is used for the simulation of both schemes.

3.1 Sine-Triangle Based PWM Modulation Schemes

A variety of sine-triangle-based PWM schemes has been established over the years for multi-level converters [57, 148-150]. In principle these schemes use at least one triangular carrier signal to compare a sinusoidal reference signal, their intersections determine switching pulse trains with sinusoidal varying durations used to control the switches accordingly.

The Fourier series expression for a periodic time varying voltage signal generated by sine-triangle based PWM schemes is given below:

$$
\begin{aligned}
v(t) = {} & \frac{a_{00}}{2} \qquad \text{1st Term (DC Bias)} \\
& + \sum_{n=1}^{\infty} \Big[\underbrace{a_{0n} \cos n(\omega_0 t + \phi) + b_{0n} \sin n(\omega_0 t + \phi)}_{\text{2nd Term (Fundamental + Baseband harmonics)}} \Big] \\
& + \sum_{m=1}^{\infty} \Big[\underbrace{a_{m0} \cos(m(\omega_c t + \theta_c)) + b_{0n} \sin(m(\omega_c t + \theta_c))}_{\text{3rd Term (Carrier Harmonics)}} \Big] \\
& + \sum_{m}^{\infty} \sum_{n}^{\infty} \Big[\underbrace{\begin{matrix} a_{mn} \cos(m(\omega_c t + \theta_c) + n(\omega_0 t + \phi) \\ + b_{mn} \sin(m(\omega_c t + \theta_c) + n(\omega_0 t + \phi) \end{matrix}}_{\text{4th Term (Sideband Harmonics)}} \Big]
\end{aligned}
\tag{3.1}
$$

where, a_{00} is the amplitude of DC bias/offset value and is normally zero.

a_{0n}, a_{m0}, a_{mn} and b_{0n}, b_{m0}, b_{mn} are the amplitudes of the harmonic components of corresponding terms.

n and m are the index values for the baseband and carrier.

ω_0 and ω_c are the angular frequency of the reference and carrier signal.

ϕ and θ_c are the phase shift of the reference and carrier signal.

The 1st term in the expression is the DC offset or bias whilst the 2nd term shows the fundamental component and its baseband harmonics. The 3rd and 4th term include the carrier harmonics and the side band harmonics due to difference between baseband and carrier harmonic components.

The general expression in (3.1) is true for most sine-triangle based PWM schemes for conventional multi-level converters.

The choice of a suitable PWM method usually depends on the individual power application requirements. Various methods have been proposed to assess in detail the characteristics of PWM schemes produced by converters, most notably is that investigated by Homles et al [149].

The following section explains in detail the PD-PWM and PS-PWM for the control of Flying Capacitor - MMC (FC-MMC)-based STATCOM.

For clarity the following nomenclature listed below would be used when describing the modulation schemes:

(a) Unit Cell: A unit cell is a pair of complimentary switches connected across a capacitor (half-bridge circuit). For instance, they are 4 unit cells in one sub-module in an FC-MMC.

(b) Switching frequency (f_s):This is the number of switching transitions of a unit cell within a fundamental cycle.

(c) Sub-module switching frequency (f_{sm}): This is the number of switching transitions of one sub-module within a fundamental cycle.

(d) Effective switching frequency(f_{sw}): This the resultant number of switching transitions noticed at the multilevel voltage output over a fundamental cycle.

(e) Frequency Modulation Index (m_f) : The is the ratio of the sub-module switching frequency to fundamental frequency.

$$m_f = f_{sm} / f_o \,, \qquad \text{where, } f_o \text{ is fundamental frequency}$$

3.2 Design Considerations for an FC-MMC-Based STATCOM

3.2.1 Structure of the FC-MMC

A three-phase FC-MMC may have many number of sub-modules based on the voltage levels required. The FC-MMC proposed in this study consists of six FC H-bridge Sub-modules, two chained in series per phase, and three phase limbs are connected in a star configuration as shown below.

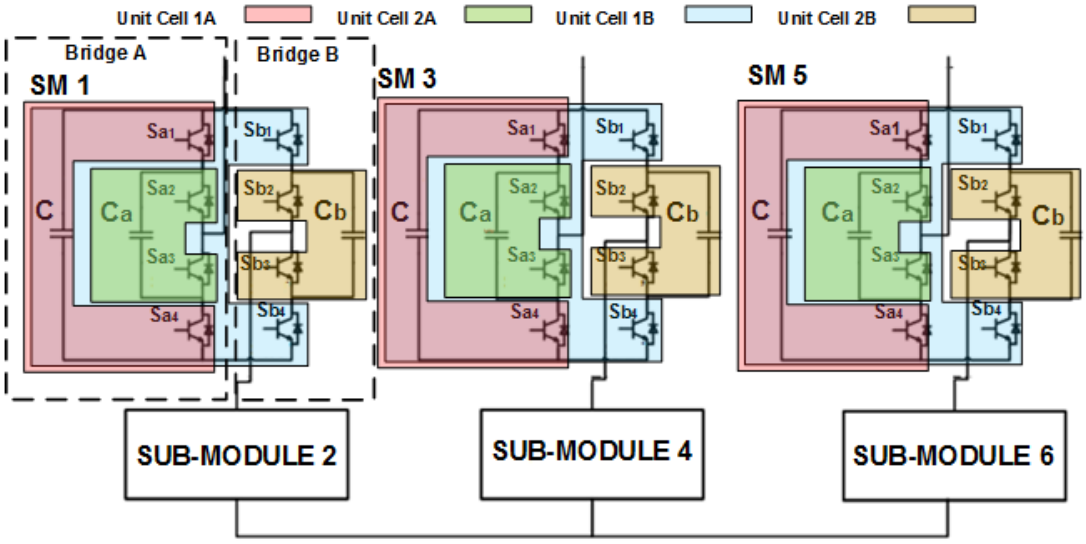


Figure 3.1: Circuit diagram of sub-modules in star configuration

Each sub-module comprises four unit cells noted in different colours as shown in Figure 3.1. For example, Unit Cell 1A consists of the switches S_{a1} and S_{a4} with capacitor C connected across them. The H-bridge structure can be looked at as two FC-Half Bridge converters with two cells at the left hand side (LHS) called Bridge A and opposite two cells on the right hand side (RHS) as Bridge B as shown in Figure 3.1.

The nomenclature “Bridge A” and “Bridge B” will be used in the following sections for the explanations of the PD-PWM and PS-PWM schemes.

3.2.2 Total Harmonic Distortion (THD)

3.2.2.1 Analysis of THD for Bipolar Switching

In sine-triangle based PWM schemes there are generally two ways of using the reference sinusoidal signal to generate the pulse trains to drive a unit cell. The first method is the bipolar switching as shown in Figure 3.2.

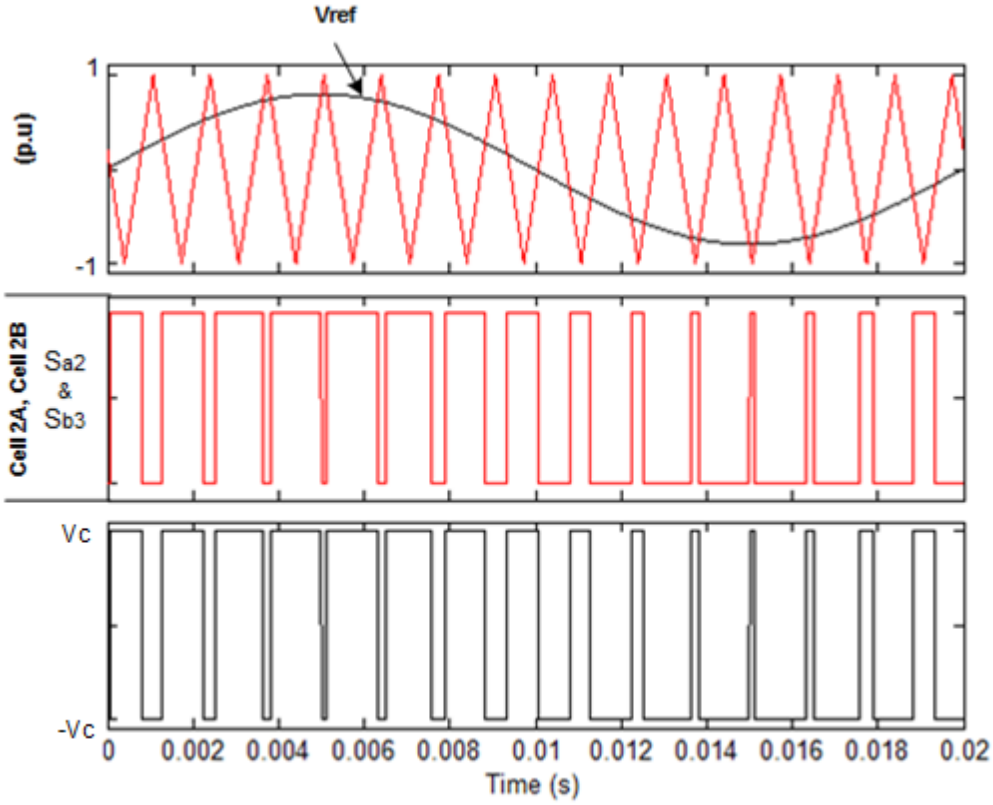


Figure 3.2: Bipolar Switching of Unit Cells

This uses one triangular carrier compared to one sinusoidal reference signal. The frequency of the triangular carrier (V_{tri}) establishes the switching frequency f_s of each sub-module and the reference signal (V_{ref}) controls the switch duty ratio. This drives switch pairs of two opposite unit cells. For example, for the two cells 2A and 2B S_{a2}, S_{b3} and S_{a3}, S_{b2} are treated as two switch pairs switching on and off simultaneously as follows.

$V_{ref} > V_{tri}$: S_{a2} and S_{b3} on-state and Vo = +Vc

$V_{ref} < V_{tri}$: S_{a3} and Sb2 on-state and Vo = -Vc

The resultant voltage output is of bipolar nature with two polarities ± Vc and contains harmonic components as shown in Figure 3.3. These harmonics appear as sidebands centred around the switching frequencies and its multiples. The frequencies at which the harmonics occur can be explained using a simplified version of (3.1) as shown [151] .

$$f_h = h \times f_o \tag{3.2}$$

$$f_h = (jm_f \pm k) f_o \tag{3.3}$$

where, h is the harmonic order , k is the side band of j times the modulation frequency index m_f and f_o is the frequency of the fundamental.

In bipolar switching, for odd values of j , the harmonics appear at odd values of m_f with side bands at even values of k . While for even values of j this occurs as side bands centred around even values of m_f . This is illustrated in the THD spectrum in Figure 3.3. For instance, at the frequency of m_f , the first side bands at $m_f \pm 2$. Likewise for frequency of $2m_f$, this occurs at $2m_f \pm 1$.

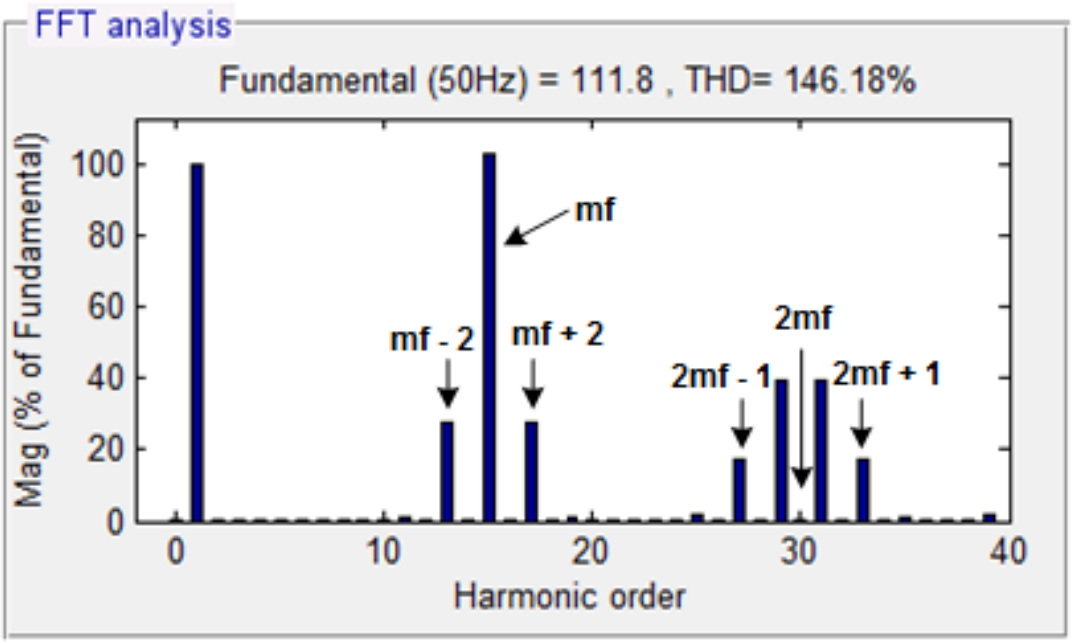


Figure 3.3: Total Harmonic Distortion (THD) for Bipolar Switching

3.2.2.2 Analysis of THD for Unipolar Switching

The unipolar method considers the FC H-bridge converter as two FC Half-bridge converters Bridge A and Bridge B . This then uses one triangular carrier and two reference sinusoidal signal phase shifted from each other by 180^0 as shown in Figure 3.4.

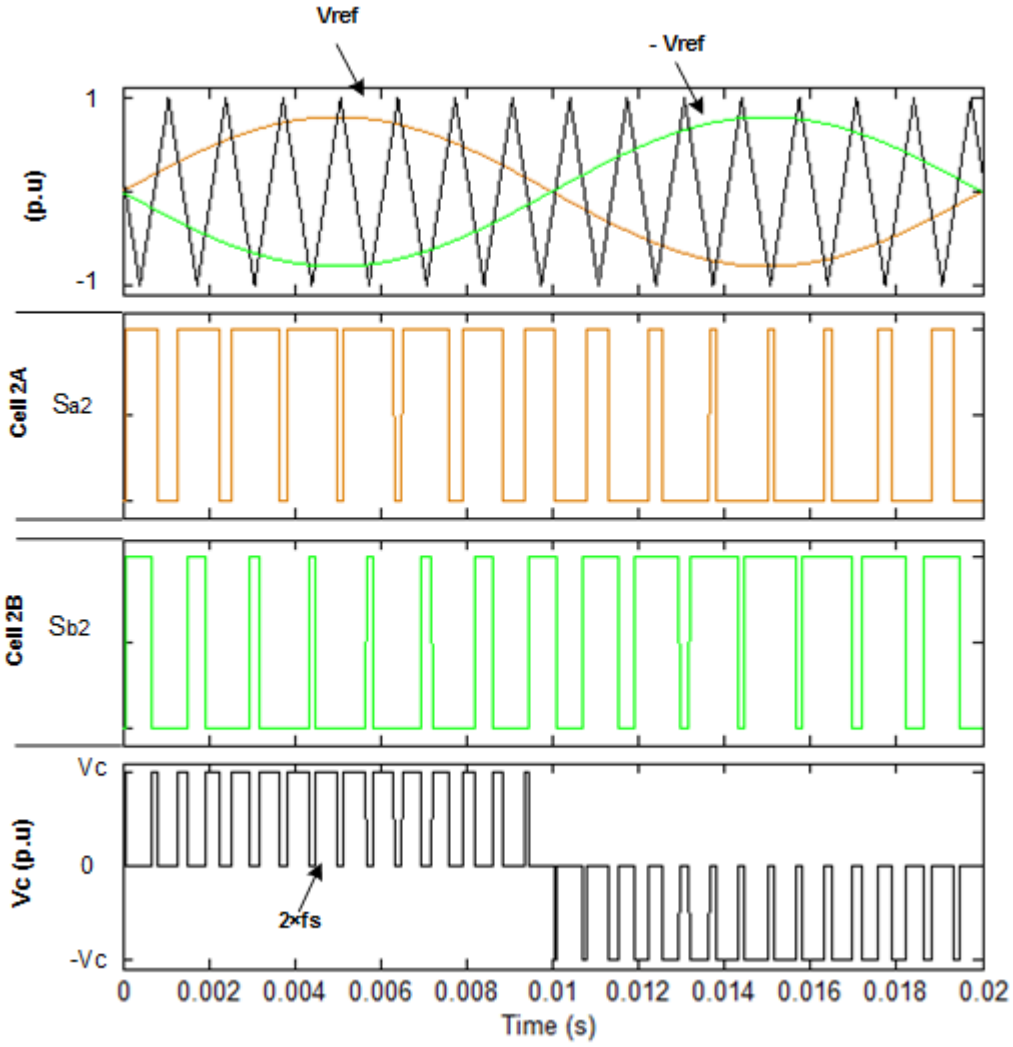


Figure 3.4: Unipolar Switching of Unit Cells

The first reference V_{ref} compared to the triangular carrier V_{tri} results in the pulse signal to drive the switch pair in a unit cell in Bridge A whilst the signal generated by anti-phase reference $-V_{ref}$ controls Bridge B. For example, the switching states for unit cell 2A with complementary switch pair Sa2, Sa3 are such that

$V_{ref} > V_{tri}$: S_{a2} on-state , S_{a3} off-state and Vo = +Vc

$V_{ref} < V_{tri}$: S_{a2} off-state , S_{a3} on-state and Vo = 0

This results in voltages of single polarity +Vc. The resultant output voltage is the difference between Bridge A and Bridge B as shown in Figure 3.4.

In unipolar switching, the anti-phase 180^0 reference signal causes all even harmonics at the switching frequency to be eliminated and they rather appear as sidebands at multiples of $2m_f$. In addition, the sub-module

switching frequency f_{sm} is doubled and the first harmonic moved higher up in the spectrum at $2m_f$ as shown in Figure 3.5.

Based on this, the harmonic frequency could be expressed in the form

$$f_h = j(2m_f \pm k) f_o \tag{3.4}$$

where, k must be an odd value showing the side bands at the multiples of $2m_f$. This is illustrated in Figure 3.6.

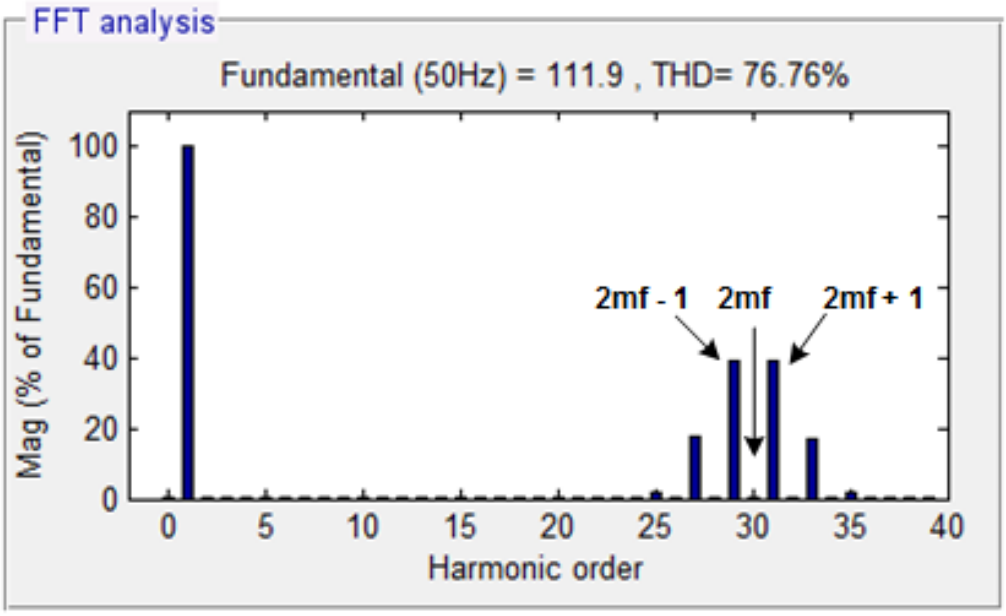


Figure 3.5:Total Harmonic Distortion (THD) for Unipolar Switching

Compared to bipolar switching, unipolar switching has a better harmonic characteristics within significantly lower harmonic content. Hence, this approach is used for both PD-PWM and PS-PWM schemes.

3.2.3 Natural Balancing Capability

Another important feature to consider when analysing PWM schemes for the FC-MMC is natural balancing property of the inner capacitors, C_A for cell 2A and C_B for cell 2B. If controlled properly using the PWM method, this can charge and discharge the inner flying capacitors adequately under normal operation. To investigate the natural balancing property under PWM schemes, the following features need to be considered.

(a) Capacitor Voltage Deviation from the mean level: This is the voltage variation due to charging and discharging the inner capacitors during one fundamental cycle. This is mainly characterised by the instantaneous current flowing through the capacitor (Cdv/dt) at the switching frequency f_s .

(b) Capacitor Voltage Drift: The is the mean voltage change from its nominal level when there is unequal charging and discharging of the inner capacitors. The voltage drifts away from its require value over a number of fundamental cycles. This occurs typically with most open loop balancing methods and is mainly due to unsymmetrical harmonics in the current waveform.

Figure 3.6 gives an illustration of the capacitor voltage deviation and voltage drift.

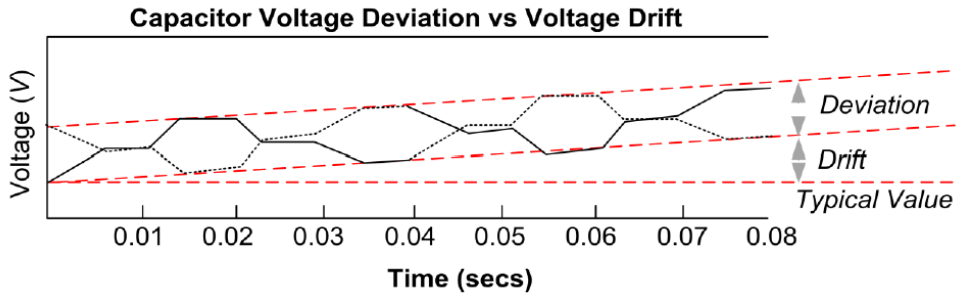


Figure 3.6: Illustration of Capacitor Voltage Deviation and Voltage Drift

3.2.4 Sub-Module Utilisation

This considers the number of times the switches in a sub-module changes their states during a fundamental cycle. This is based on both schemes operating at the same switching frequency f_s.

3.2.5 Circuit and PWM Parameters Used for Simulation

The parameters used in the simulation study for the comparison of PD-PWM and PS-PWM schemes are listed below in Table 3.1

Table 3.1 Parameters for FC-MMC Comparison

Load Parameters	**Value**
Three Phase Star Connected Balanced R-L Load	R= 10Ω L_A = 10mH
Converter Parameters	
Sub-module Outer Capacitor Voltage	V_C = 200 V
Sub-module Inner Capacitor Capacitance	C_A and C_B = 560 µF
Frequency Modulation Index	m_f = 15
Amplitude Modulation Index	m_a = 0.8

3.3. Phase Disposition PWM for FC-MMC

Phase-Disposition PWM is also known as level shift PWM as it involves using level shifted triangular carriers which are compared to the reference signals to generate the switching pulses. The number of triangular carriers is dependent on the number of voltage levels and they are in-phase distributed evenly across the positive and negative cycle. The number of triangular carriers required is determined by the number of unit cells in a half-bridge (e.g. Bridge A). In this case, there are 4 unit cells per phase, giving four voltage levels in total hence requiring four triangular carriers. The PD-PWM scheme for the FC-MMC simulated has the frequency modulation index mf =15 and resulting switching signals for one phase of the sub-modules are shown in Figure 3.7.

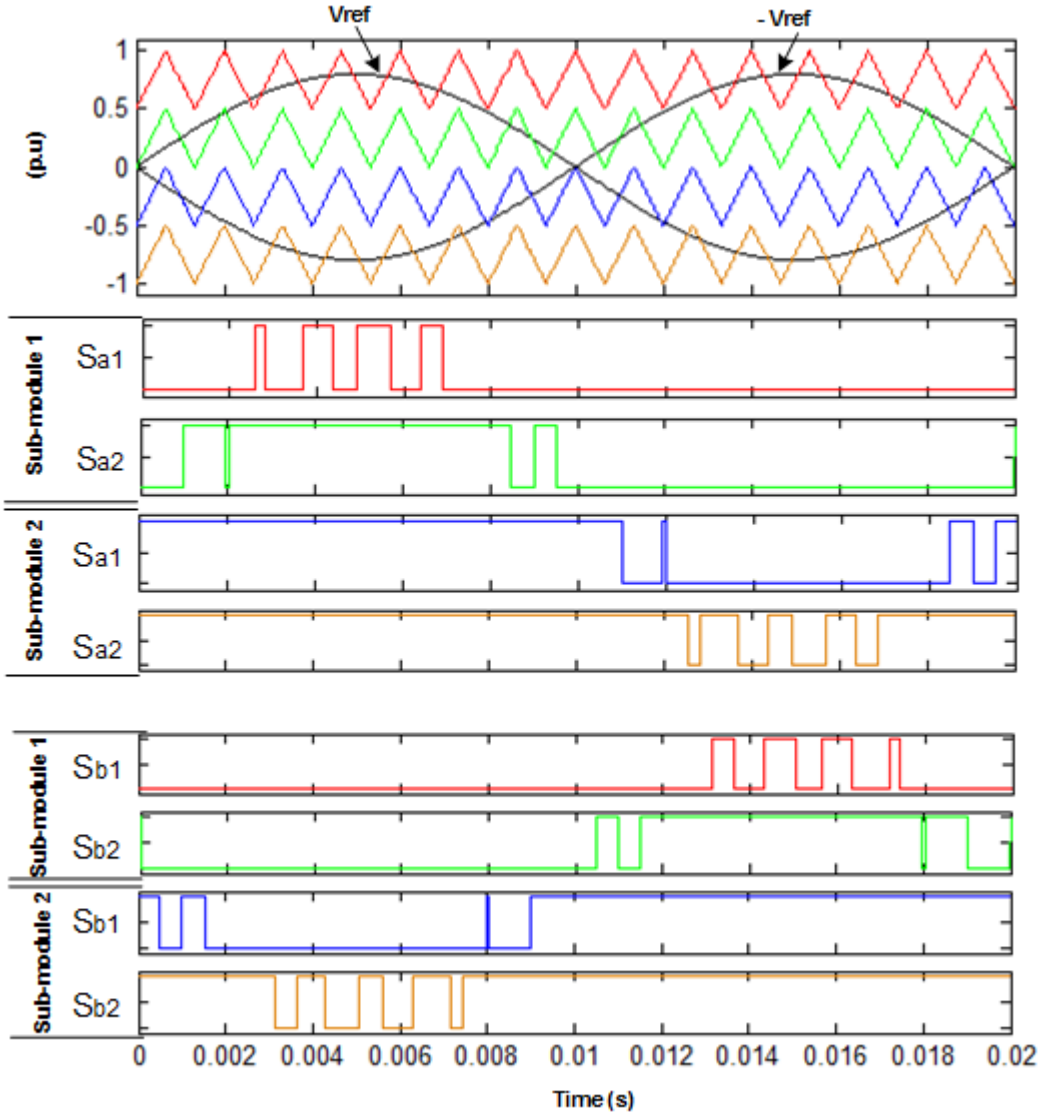


Figure 3.7: Phase Disposition PWM applied to FC-MMC at m_f = 15

In this approach, unipolar switching discussed earlier is used and two reference signals, V_{ref} and $-V_{ref}$, control Bridge A and Bridge B of the FC-MMC respectively. The two triangular carriers in the positive cycle drive the complementary switches Sa1, Sa4 and Sa2, Sa3 in the two unit cells in each sub-module (Bridge A). Likewise the other two triangular carriers in the negative cycle drive complementary switches Sb1, Sb4 and Sb2, Sb3 (Bridge B). The resultant phase output voltage of the FC-MMC is shown in Figure 3.8

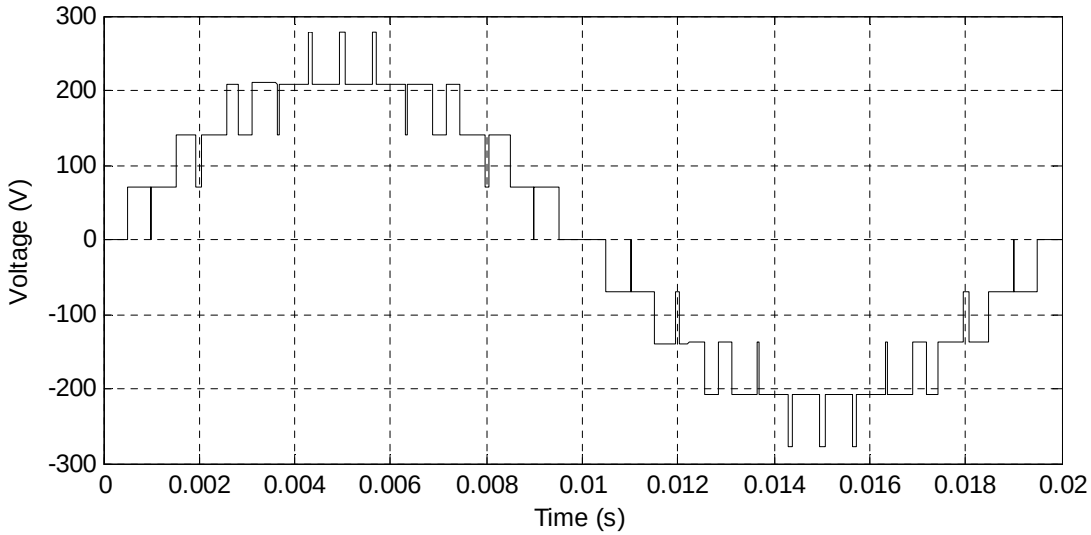


Figure 3.8: Phase Voltage of the FC-MMC under PD-PWM

3.3.1 Total Harmonic Distortion (THD) Analysis

The phase voltage and line voltage frequency spectra and the total harmonic distortion factors due to PD-PWM are as shown in Figure 3.9 and Figure 3.10 respectively.

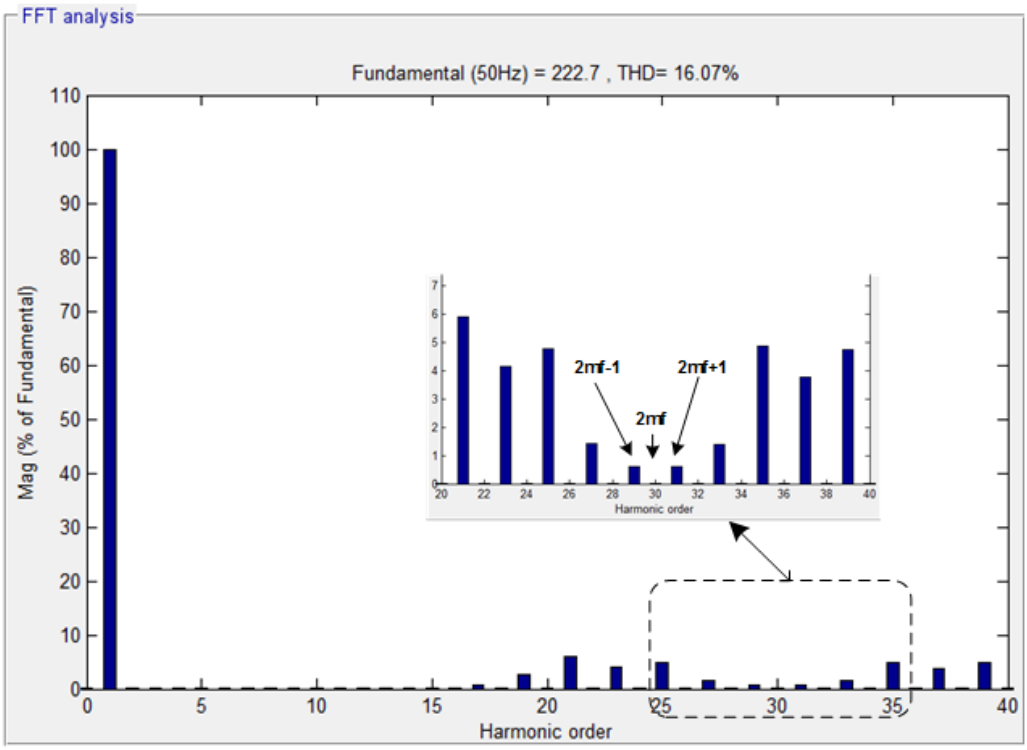


Figure 3.9: Phase voltage spectrum & THD value for PD-PWM at m_f =15

The harmonic orders in the spectrum can be expressed using the same expression for unipolar switching in (3.4).

$$f_h = j(2m_f \pm k) f_o \qquad \text{where, } f_h = h \times f_o$$

j = 1,2,3……. , k = 1,3,5 ….. odd numbers (3.5)

This expression is true provided all the level shifted triangular carriers are in phase.

The total harmonic distortion for the phase voltage spectra is 16.07%. Unipolar switching eliminates all the even harmonics multiples of $2m_f$ and they appear as side bands around odd harmonic orders. For instance, the first side bands at $2m_f$, (j = 1), noticed as shown in Figure 3.9 are

$$f_{29} = (2 \times 15 - 1) \times 50 = 1450\,Hz\,, \quad f_{31} = (2 \times 15 + 1) \times 50 = 1550\,Hz.$$

For line voltage spectra the total harmonic distortion is reduced to 12.47% , all 3rd order harmonics are eliminated and sideband harmonics appear around $2m_f$ and its multiples.

This can be expressed using the equation in (3.5) for

j = 1,2,3……. , k = 1 ,5,7 ….. odd numbers excluding odd multiples of 3

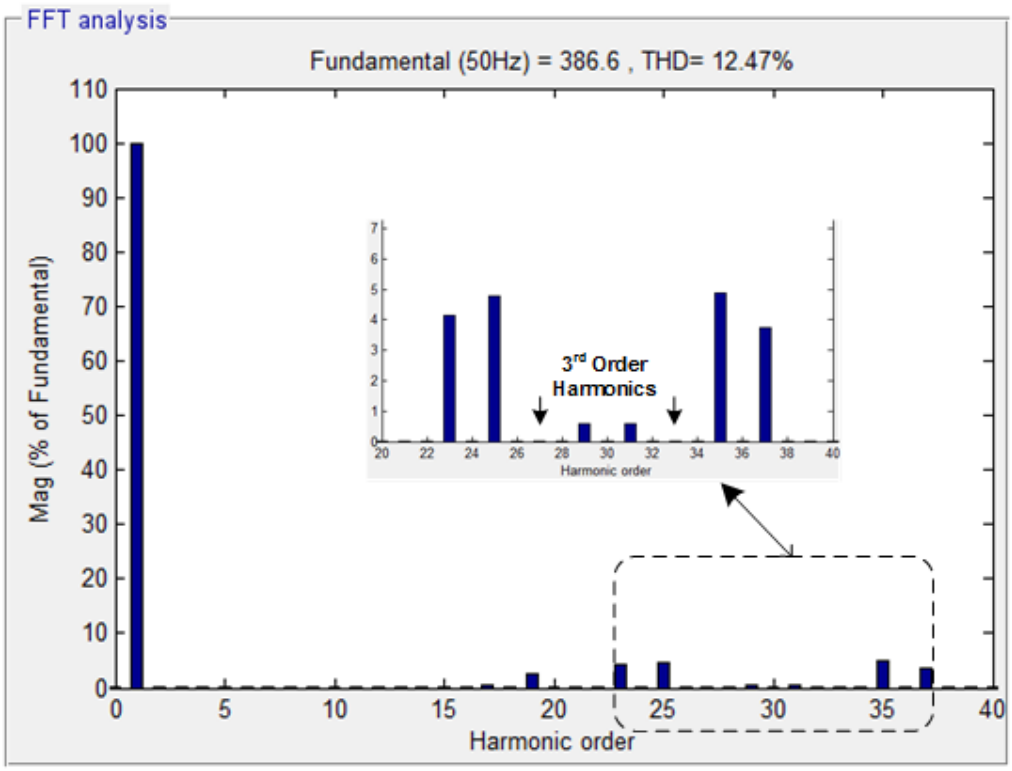


Figure 3.10:Line Voltage Spectrum & THD value for PD-PWM at m_f =15

3.3.2 Natural Voltage Balancing Capability

The natural balancing capability of the PD-PWM scheme is investigated using the switching states under one cycle operation. This is shown in Figure 3.11 for one sub-module.

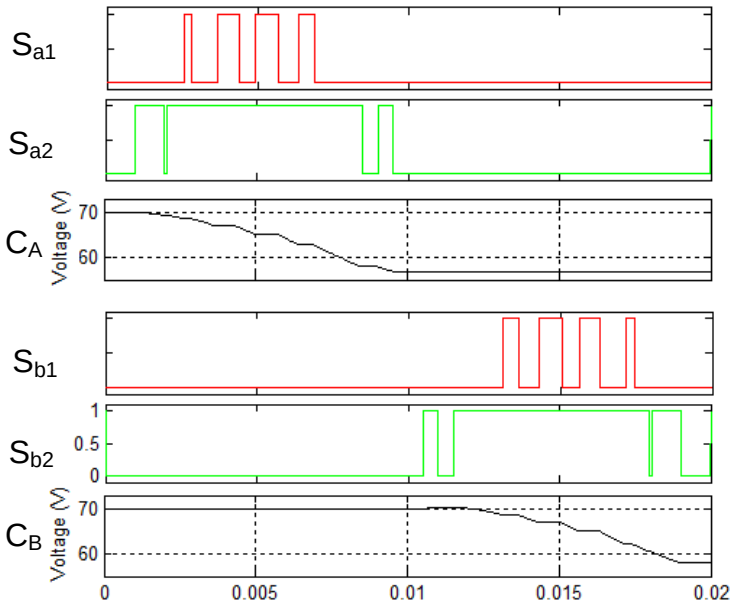


Figure 3.11: PD-PWM Switching actions for One sub-module in a fundamental cycle

As can be noticed, the capacitor voltages deviate away from the nominal value (70V). The switching signals are seen to discharge the inner capacitor C_A during the first half cycle and discharge the inner capacitor C_B over the negative half cycle. Thus, the capacitor voltage deviation is ±30V per cycle since they are not charged and then discharged equally over a cycle. Over time this will lead to an output voltage waveform with an unacceptable spectral quality. This makes using the PD-PWM scheme impractical for natural balancing of the capacitors. For typical application, feedback voltage control would be required to maintain the voltages of inner capacitors of each sub-module to be balanced.

3.3.3 Sub-Module Utilisation

The variations of the inner capacitor voltages in Figure 3.11 are attributed to the uneven utilization of the switches in a sub-module. The switch S_{a1} (red) experiences more switching stress, while switch S_{a2} (in green) remains turned-on for a longer time. This causes higher switching losses in S_{a1} and higher conduction losses in S_{a2}.

3.4 Phase Shifting PWM for FC-MMC

Phase-Shifting PWM is different from PD-PWM in that the triangular carriers are phase shifted from each other by an equal angle. The number of triangular carriers is also dependent on the number of voltage levels and is determined by the number of unit cells in a half-bridge (Bridge A). In this case, there are still four unit cells in total hence four triangular carriers. The phase shift angle between the carriers θ_C can be expressed as

$$\theta_c = 180^\circ /(N-1) \tag{3.6}$$

where N is the number of voltage levels in the FC-MMC from 0 to peak voltage. In this case N=5 giving 45^0.

Unipolar switching is still used here with two reference signals V_{ref} and $-V_{ref}$ controlling Bridge A and Bridge B of the FC-MMC respectively. In one sub-module, V_{ref} compared to two triangular carriers produces switching signals to drive the complementary switches S_{a1}, S_{a4} and S_{a2}, S_{a3} whilst $-V_{ref}$ compared with the same triangular carriers generates signals to drive the opposite complementary switches S_{b1}, S_{b4} and S_{b2}, S_{b3}.

The PS-PWM scheme for the FC-MMC at the frequency modulation index m_f = 5 and resulting switching signals for one phase of the sub-modules is shown in Figure 3.12. The resultant output voltage for a phase is shown in Figure 3.13.

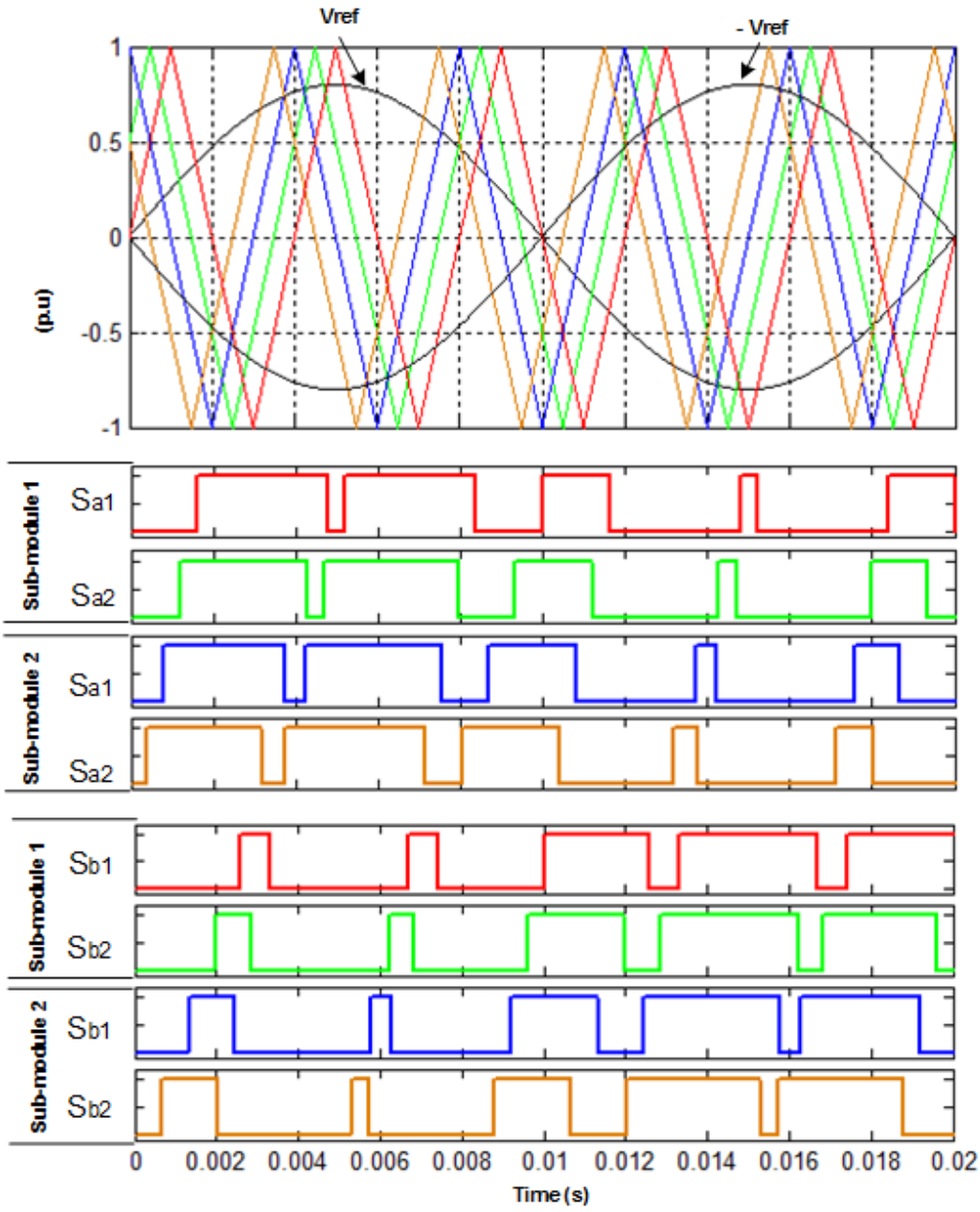


Figure 3.12:Phase Disposition PWM applied to FC-MMC at m_f = 5

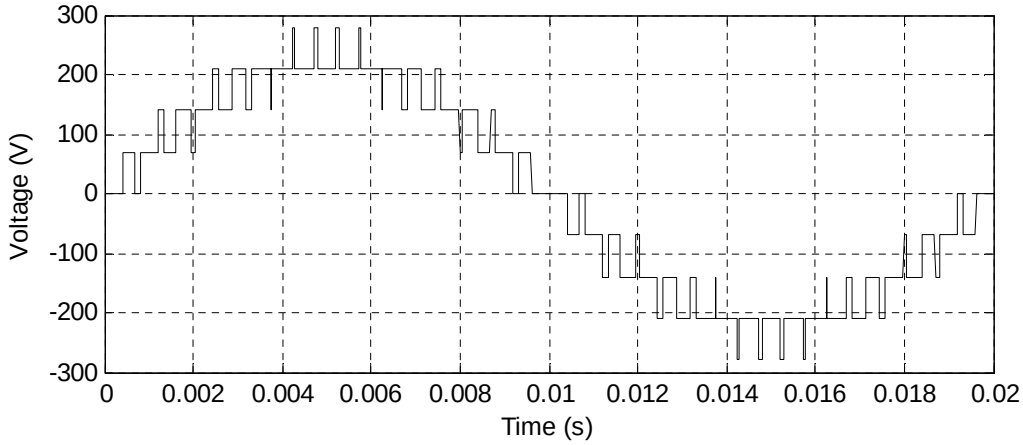


Figure 3.13:Phase Voltage of the FC-MMC under PS-PWM

3.4.1 Total Harmonic Distortion (THD) Analysis

The phase voltage and line voltage spectra for the total harmonic distortion analysis of the PS-PWM at m_f =15 are as shown in Figure 3.14 and Figure 3.15 respectively

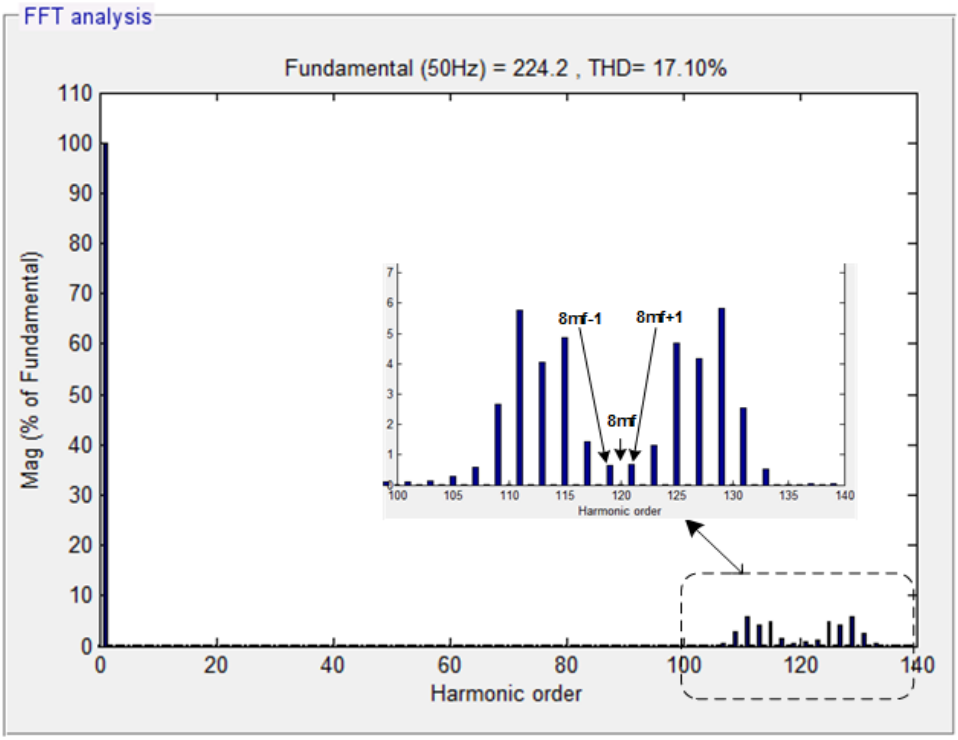


Figure 3.14: Phase Voltage Spectrum & THD value for PS-PWM at m_f =15

In the FC-MMC of Figure 3.1, there are in total 8 phase shift operations. Four phase shift signals for each of the four unit cells in Bridge A and the other four are for unit cells in Bridge B. With a phase delay θ_c between each

unit cells switching frequency at f_s this makes the effective switching frequency $f_{SW} = 8 \times f_s$. Hence, the harmonic orders in the spectrum can be expressed as shown in (3.7).

$$f_h = j(8m_f \pm k) f_o \qquad \text{where, } f_h = h \times f_o$$

j = 1,2,3……. , k = 1,3,5 ….. odd numbers (3.7)

This total harmonic distortion is at 17.10% and the unipolar switching eliminates all the even harmonics in the phase voltage spectra and they appear as side bands appear at odd harmonic orders around $8m_f$ and its multiples.

For instance for m_f = 15 the first side bands appear at $8m_f$, (j = 1), as shown

$f_{119} = (8 \times 15 - 1) \times 50 = 5950\ Hz$, $f_{121} = (8 \times 15 + 1) \times 50 = 6050\ Hz$.

Hence, the harmonics in the PS-PWM are shifted to the higher frequency spectrum for the same switching frequency used in PD-PWM scheme. For the line voltage spectra, the THD is at 13.7% and the 3rd order harmonics are eliminated with sideband harmonics appear around $8m_f$ and its multiples.

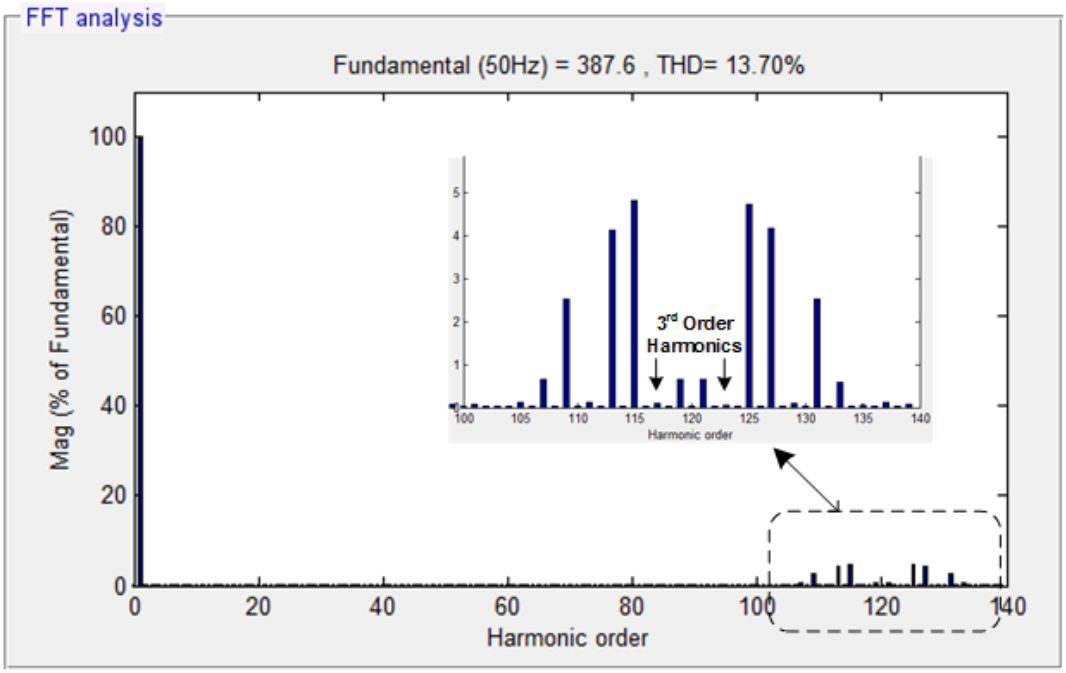


Figure 3.15: Line Voltage Spectrum & THD for PS-PWM at m_f =15

3.4.2 Natural Balancing Capability

The natural balancing capability of the PS-PWM scheme is investigated using the switching states under one cycle operation. This is shown for one sub-module at m_f =15 in Figure 3.26.

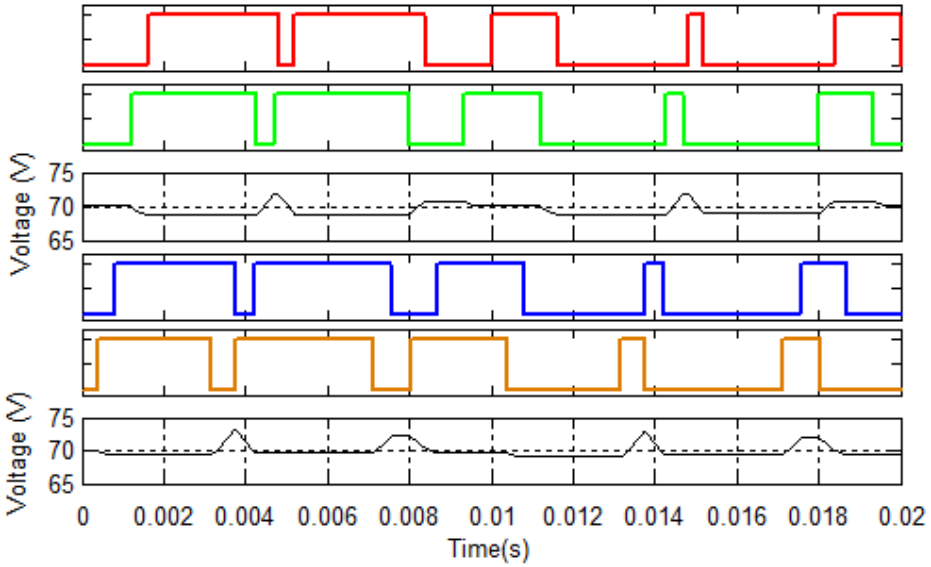


Figure 3.16: PS-PWM Switching actions in a fundamental cycle

The switching signals are symmetrical over the half cycle. Hence, capacitors are charged in the first half cycle and discharged in the second half cycle. As noticed, the capacitor voltages maintain the nominal voltage value of 70V. This demonstrates that the PS-PWM can achieve natural capacitor voltage balancing over each fundamental cycle. The capacitor voltage deviation is ±2V per cycle with no voltage drift. This gives an output voltage waveform with acceptable spectral quality and makes using the PS-PWM scheme practical for the FC-MMC.

3.4.3 Sub-Module Utilisation

The variations of the inner capacitor voltages in Figure 3.16 are attributed to the equal utilization of the switches in every half cycle. Hence the sub-modules are utilised equally. The switching signals in sub-module 1 shown in red and green colours indicate switches experiencing conduction and switching stresses over a cycle evenly. However there are more switching actions compared to PD-PWM but less conduction states.

3.5 Comparison of PD-PWM and PS-PWM Schemes

Table 3.2: Comparison of Modulation Techniques for FC-MMC

	PD-PWM	PS-PWM
Total Harmonic Distortion	✓	
Natural Balancing Capability		✓
Sub-Module Utilisation		✓

Table 3.2 summarises the comparison of the two sine-triangle based modulation schemes for FC-MMC control. Based on three criteria listed in this table, the following conclusions can be summarised below:

- The total harmonic distortion (THD): For the same 9 voltage levels FC-MMC , both PD-PWM and PS-PWM schemes give almost equal THD values at 16.01% and 17.10% for their respective output phase voltage waveforms. The slightly superior THD performance of PD-PWM is due to that it results in reduced converter switching actions. However using the PS-PWM the required filter size can be smaller since the harmonics present are shifted to higher frequency band
- Natural balancing capability: this is only achievable under PS-PWM scheme. For this to be obtainable when using PD-PWM scheme, the modulation approach would have to be modified to exchange charging and discharging states over a cycle.
- Sub-module utilisation: this is shared equally in PS-PWM compared to PD-PWM. Although, the PS-PWM would generally have more switching losses compared to conduction losses, the PD-PWM would have more conduction losses compared to switching losses. The cumulative effect makes PS-PWM incurring more power losses than PD-PWM in general.

In summary, the PS-PWM scheme has more favourable features for the MMC STATCOM application and is thus applied in this work.

3.6. Summary

This chapter has presented two sine-triangle based PWM modulation schemes for the FC-MMC STATCOM. Both schemes were investigated in detail in terms of harmonic spectrum of the output voltage waveforms, natural balancing capability of their inner capacitors and sub-module utilisation. Compared to the PD-PWM, PS-PWM offers the most benefits according to the criteria of low total harmonic distortion (THD) factor, natural balancing capability and even sub-module utilization of an FC-MMC.

Chapter 4
Synchronisation of Grid Connected Converters Using the Energy Operator

Grid synchronisation technique is of high importance to a STATCOM. Generally fast and accurate grid voltage phase angle detection is crucial for the stable operation of a STATCOM working under both balanced and unbalanced power networks. The latter occurs frequently in distribution systems. This may be caused by large unbalanced loads, for example single-phase electric traction systems or arc furnaces, and it may also be caused by asymmetrical transient faults in the system. For example, large motors particularly are known to cause transient grid faults when starting [152]. Most common grid faults are single line-to-ground faults which are often of short duration (100ms-600ms) [153-155] and it is required that during the unbalanced grid voltage conditions the grid synchronization scheme can recognize the faults quickly and lock on the grid frequency and phase angle so that the devices like STATCOMs can function normally to minimise the disturbances to the load, i.e. ride through the grid faults [156-159].

This chapter presents a new synchronization technique, called the energy operator phase locked loop (EO-PLL), which can track the grid voltage fundamental frequency and phase angle variations for under both grid voltage balanced and unbalanced conditions.

The chapter starts by presenting the principles and algorithm of the proposed EO-PLL scheme. Simulation studies of the EO-PLL scheme and its comparison to other two well-known PLL methods are presented in Appendix B.2. Finally, an experimental implementation of the EO-PLL scheme and results obtained are described in Section 4.4.

4.1 Grid Synchronisation Based on Energy Operator

4.1.1 Literature Review of the Energy Operator

Originated by Herbert M. Teager [160] and expounded by Kaiser [161], the energy operator technique has been applied widely and successfully in signal processing for the demodulation of speech signals [162].

In power applications, the interest in energy operator has been growing over the years. Most literature available investigates it for voltage flicker and amplitude change detection [163-166]. More recent literature has proposed to use the technique for fault diagnosis of induction motors through demodulating the stator current before applying FFT analysis [167]. It has also been applied for online symmetrical component decoupling from three-phase voltages in combination with the Fortescue theorem[168]. Recently the technique has been tried for identification of real and reactive power changes, e.g. for measuring the power factor [169]. Application for estimation of single phase grid frequency has also been reported [170, 171]. Hitherto, to the author's knowledge, no literature has explored the application of the energy operator technique for power grid synchronization under unbalanced voltage conditions.

4.1.2 Principle of Energy Operator

In communication signal processing, the energy of the continuous time varying signal $x(t)$ is expressed as (4.1) [162].

$$E[x(t)] = \int_{-\infty}^{\infty} \left|x(t)\right|^2 dt \tag{4.1}$$

This expression is similar but not the same as the notion of energy in electrical systems which is expressed is terms of the instantaneous power (4.2)

$$E[v(t)] = \frac{1}{Z}\int_{-\infty}^{\infty} \left|v(t)\right|^2 dt \tag{4.2}$$

where, $x(t)$ now represents time varying voltage signal $v(t)$ and Z is the impedance of the transmission medium i.e. transmission or distribution line

The expression in (4.1) comes from the fact that in communication systems the resistance of the transmission medium is negligible or non-existent [172-174]. Hence the equation in (4.1) gives the SI unit of volt/sec which is not a

correct representation of energy in electrical systems given as volt/sec/ohm or Joules.

Similarly, this notion can be used to explain the energy of mechanically oscillating motion. The principle derived from newton's laws of motion a conceptual un-damped mechanical oscillator described by $m\ddot{x}(t)+kx=0$.

$$m\frac{d^2x(t)}{dt^2}+kx=0 \tag{4.3}$$

The expression in (4.3) describes the motion an object of a mass m suspended by a string with constant k and is a simple harmonic motion sinusoidal nature $x(t)=A\cos(\omega t+\phi_x)$

where, $x(t)$ represents the position of the object at time t

A is the amplitude of the oscillation

$\omega=\sqrt{\frac{k}{m}}$ is the frequency of the oscillation

ϕ_x is the initial phase when $(\phi_x=0)$

The total energy of the object is the sum of the potential and kinetic energy expressed as

$$E[x(t)]=\frac{1}{2}kx^2+\frac{1}{2}mv^2 \tag{4.4}$$

where, v in this case represents the velocity

By substituting $v=dx/dt$ and $x(t)=A\cos(\omega t+\phi_x)$ we get the total energy to be

$$E[x(t)]=\frac{1}{2}m\omega^2A^2 \tag{4.5}$$

This expression shows that the energy is directly proportional to the amplitude and frequency. Similarly like in (4.2), the mass is dependent on the inertia which is the resistance of the object to any change in motion [175, 176] . This can also be neglected when looked at as an energy in signal processing. This observation is what prompted Kasier to derivate the expression for the term known as the 'energy operator' [161, 165, 177, 178].

The term "operator" in this context is derived from quantum and classical physics and describes the motion of oscillatory objects in a vector space [179-181] . This term in signal processing describes the correlation in between processing stagse of an input signal and it corresponding output

signal. For example, digital filters are regarded as an operator on a signal [178]. Hence, the term “energy operator” originated by Kasier describes some correlation to the energy in mechanical oscillatory motion in (4.5). This is derived from trigonometric manipulations and is described in the subsequent sub sections.

4.1.2.1 Continuous Time Model

Applying this concept to the grid sinusoidal voltage of a power system with constant frequency and amplitude given as (4.6)

$$v_x(t) = V_x \cos(\omega t + \phi_x) \tag{4.6}$$

The energy operator on the voltage signal can be represented as (4.7)

$$\begin{aligned} E[v_x(t)] &= \dot{v}_x{}^2(t) - v_x(t)\ddot{v}_x(t) \\ &= \left(-\omega V_x \sin(\omega t + \phi_x)\right)^2 \ldots\ldots \\ &\quad -V_x \cos(\omega t + \phi_x) \times -\omega^2 V_x \cos(\omega t + \phi_x) \\ &= \omega^2 V_x{}^2 \end{aligned} \tag{4.7}$$

The significance of expression (4.7) is that the amplitude-frequency product of a sinusoid can be found from time-localised estimates of the voltage and its first two time derivatives, with the result being independent of the instant at which the estimates are made. This expression is what is regarded as the energy operator. The energy operator (EO) is a time-domain technique that estimates the energy of a time varying signal [18] by using first and second derivatives of the signal**.**

4.1.2.2 Discrete Time Model

In practice, the instantaneous energy operator on a time varying voltage signal $v_x(t)$ must be estimated by using a discretized version of (4.7). This is derived from three equally spaced samples of the signal, given by (4.8) – (4.10)

$$v_x(n) = V_x \cos(\Omega_x n + \phi_x) \tag{4.8}$$

$$v_x(n-1) = V_x \cos(\Omega_x (n-1) + \phi_x) \tag{4.9}$$

$$v_x(n+1) = V_x \cos(\Omega_x (n+1) + \phi_x) \tag{4.10}$$

where $\Omega_x = \frac{2\pi f}{f_s}$, is the discrete angle per sample, f is the signal frequency, f_s is the sampling frequency. Hence the sample period $T_s = 1/f_s$ and $\Omega_x = T_S \omega$.

Applying trigonometric identities (Appendix B1.1), the product of the equations in (4.9) and (4.10) can be expressed as (4.11)

$$v_x(n+1)v_x(n-1) = V_x{}^2 \cos^2(\Omega_x n + \phi_x) - V_x{}^2 \sin^2(\Omega_x) \quad (4.11)$$

For a high enough sampling frequency, the discretized energy operator algorithm can be expressed by substituting (4.8) into (4.11), the equation is given as (4.12)

$$\begin{aligned} E[v_x(n)] &= v_x(n)^2 - v_x(n+1)v_x(n-1) \\ &= V_x{}^2 \sin^2(\Omega_x) \\ &= V_x{}^2 \Omega_x{}^2 = V_x{}^2 T_S^2 \omega^2 \end{aligned} \quad (4.12)$$

Equation (4.8) shows that with just three sample shifts of the original voltage signal, its instantaneous energy can be resolved. Thus for a high sampling frequency the instantaneous energy can be estimated in a time interval of $3 \times T_S$.

4.1.2.3 Effect of Sampling Frequency in Energy Estimation

When using discrete time model for energy estimation, the choice of sampling frequency affects the estimation results. Figure 4.1 shows a plot illustrating the estimated energies of a voltage signal $v_x(t) = \cos(\omega_f t + \phi_x)$ over one fundamental cycle at various sampling frequencies f_s = 0.5 kHz, 1 kHz, 2 kHz and 5 kHz. All estimates have shown that the results converge to their steady state values within a period of 3 sample delays $3 \times T_s$ as expected. For example, for a sampling frequency of 1 kHz, it takes 3ms for the operation to converge. Likewise for sampling frequency of 5 kHz, the steady-state occurs after about 600µs. Moreover, these results show that for higher sampling frequencies the estimated energy values are higher and more accurate. For example, when f_s= 5 kHz, the estimated energy converges to 9.9x10^4 Vrads/s. However when f_s= 0.5 kHz, estimated energy value converges to about 8.7x10^4 Vrads/s. The difference is due to the use of approximation $\sin^2(\Omega_x) = (\Omega_x)^2 = (\omega T_s)^2$ in deriving Equation 4.12. This approximation is only adequate when sample period T_s is very small. Thus one can see from the plots in this figure that when f_s = 5 kHz the estimated energy is deemed sufficiently accurate. However as the sampling frequency

decreases the energy value reduces and when f_s = 0.5 kHz, the lowest frequency value tested, there is a big gap in estimated energy compared to that obtained at 5 kHz.

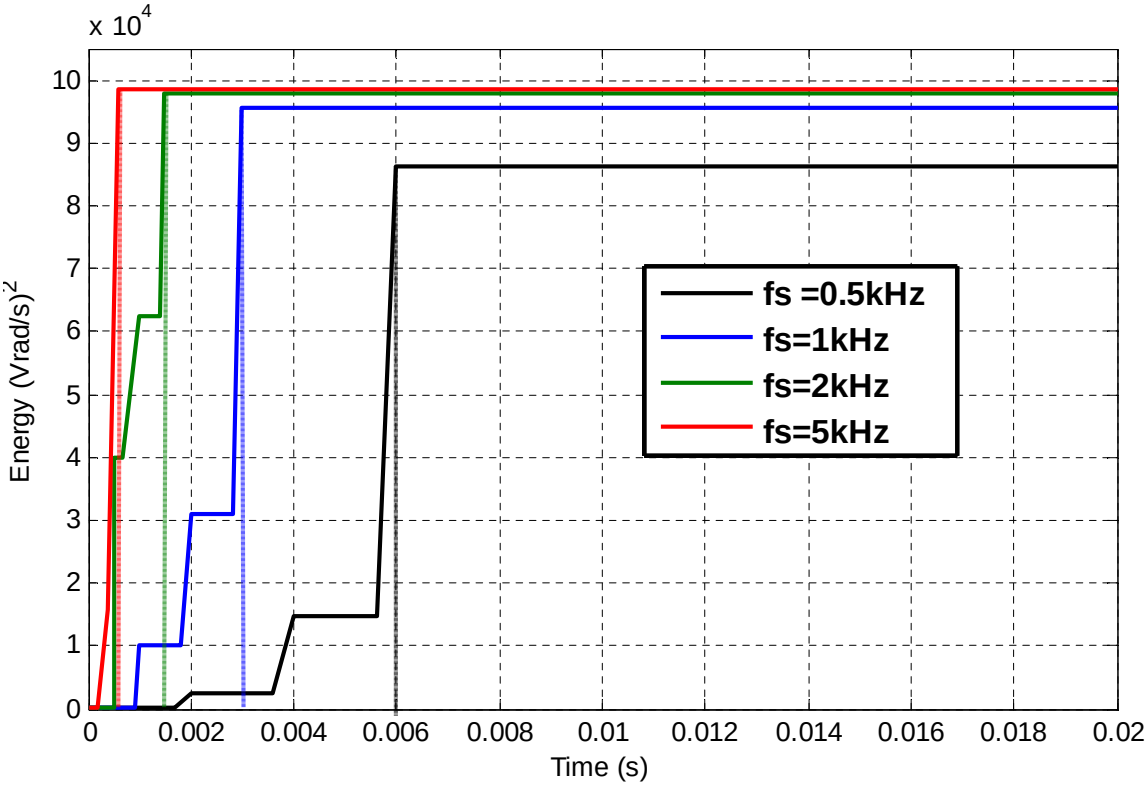


Figure 4.1: Energy of voltage signal at different sampling frequencies

4.1.3 Frequency Estimation Using Energy Operator

4.1.3.1 Continuous Time Model

Following the above principle, the method can be applied to estimate the frequency of a sinusoidal signal. This is explained below.

A frequency dependent relationship can be derived by applying expression (4.7) to the derivative of the sinusoidal phase voltage, i.e. $\dot{v}_x(t)$, thus we have

$$\begin{aligned} E[\dot{v}_x(t)] &= \ddot{v}_x{}^2(t) - \dot{v}_x(t)\dddot{v}_x(t) \\ &= \left(-\omega^2 V_x \cos(\omega t + \phi_x)\right)^2 - \left(-V_x \sin(\omega t + \phi_x)\right)\times \\ &\qquad \left(-\omega^3 V_x \sin(\omega t + \phi_x)\right) \\ &= \omega^4 V_x{}^2 \left(\sin^2(\omega t + \phi_x) + \cos^2(\omega t + \phi_x)\right) \\ &= \omega^4 V_x{}^2 \end{aligned} \tag{4.13}$$

This yields an energy estimate of $\dot{v}_x(t)$, and then by dividing (4.13) by (4.7) to eliminate V_x^2 and taking the square root of the result, the frequency of can be deduced as expressed below

$$f = \frac{1}{2\pi}\sqrt{\frac{E[\dot{v}_x(t)]}{E[v_x(t)]}} \tag{4.14}$$

This shows that the frequency of a sinusoid signal can be derived from the estimates of the energies of itself and its first order derivative. This result can be applied to estimate the instantaneous frequency of the grid voltage signal for synchronization.

4.1.3.2 Discrete Time Model

In discrete time, the discrete energy separation algorithm (DESA-2) [162] based on the weighted average of energies of each sample will be employed. In this method, the derivative of $v_x(n)$ defined by (4.13) can be approximated as the average of two finite differences using its pro and after samples i.e.

$$\begin{aligned}\dot{v}_x(n) &\approx \frac{1}{2}\left(\frac{v_x(n+1)-v_x(n)}{T_s}+\frac{v_x(n)-v_x(n-1)}{T_s}\right)\\ &= \frac{v_x(n+1)-v_x(n-1)}{2T_s}\end{aligned} \tag{4.15}$$

Substituting (4.8) – (4.10) into (4.15) gives

$$\dot{v}_x(n) \approx \frac{V_x\cos(\Omega_x(n+1)+\phi_x)-V_x\cos(\Omega_x(n-1)+\phi_x)}{2T_s} \tag{4.16}$$

which can then be simplified using trigonometric identities (Appendix B1.2) to

$$\dot{v}_x(n) \approx V_x\sin(\Omega_x)\sin(\Omega_x n+\phi_x) \tag{4.17}$$

Applying (4.12) for energy in discrete time signals the energy $E[\dot{v}_x(n)]$ can be shown to be

$$\begin{aligned}E[\dot{v}_x(n)] &= \ddot{v}(n)^2 - \dot{v}_x(n+1)\dddot{v}_x(n-1)\\ &= V_x{}^2\sin^2(\Omega_x)\left(\sin^2(\Omega_x n+\phi_x)-\begin{pmatrix}\sin(\Omega_x(n+1)+\phi_x)\\ \times\sin(\Omega_x(n-1)+\phi_x)\end{pmatrix}\right)\end{aligned} \tag{4.18}$$

With further application of identities (Appendix B1.3), this expression can be simplified to

$$E[\dot{v}_x(n)] = V_x{}^2 \sin^4(\Omega_x) \tag{4.19}$$

Similar to the continuous time form an expression for the discrete angular frequency Ω_x can be deduced by taking the ratio of the energy expressed in (4.19) to $E[v_x(n)]$ in (4.12), thus this gives

$$\frac{E[\dot{v}_x(n)]}{E[v_x(n)]} = \frac{V_x{}^2 \sin^4 \Omega_x}{V_x{}^2 \sin^2 \Omega_x} = \sin^2 \Omega_x = \frac{1 - \cos 2\Omega_x}{2} \tag{4.20}$$

This leads to the derivation of the frequency as

$$f_x = \frac{1}{2\pi T_s} \sin^{-1}\left(\sqrt{\frac{E[\dot{v}_x(n)]}{E[v_x(n)]}}\right)$$

$$or \quad \frac{1}{4\pi T_s} \cos^{-1}\left(\sqrt{1 - \frac{2E[\dot{v}_x(n)]}{E[v_x(n)]}}\right)$$

This expression shows that identification of measured signal frequency is not dependent on its voltage magnitude but on the voltage samples within the data window.

4.1.3.3 Effect of Sampling Frequency in Frequency Estimation

Figure 4.2 illustrates the estimated frequencies of a voltage signal $v_x(t) = V_x \cos(\omega_f t + \phi_x)$ at various sampling frequencies f_s = 0.5 kHz, 1 kHz, 2 kHz and 5 kHz. The frequency estimation of the grid voltage requires only five consecutive samples of the signal and the estimated results for all sampling frequencies converges their steady state values of 50Hz within a period of 5 sample delays . For example for sampling frequency of 5 kHz, the steady-state occurs at 0.001s. Naturally, as shown in the Figure, the slower the sampling rate the longer the delay for the result to converge. There is no error difference in during steady due to the fact that the approximation ($\sin^4(\Omega_x)/\sin^2(\Omega_x)$) in equation (4.20) is very small even for the least frequency of 0.5 kHz.

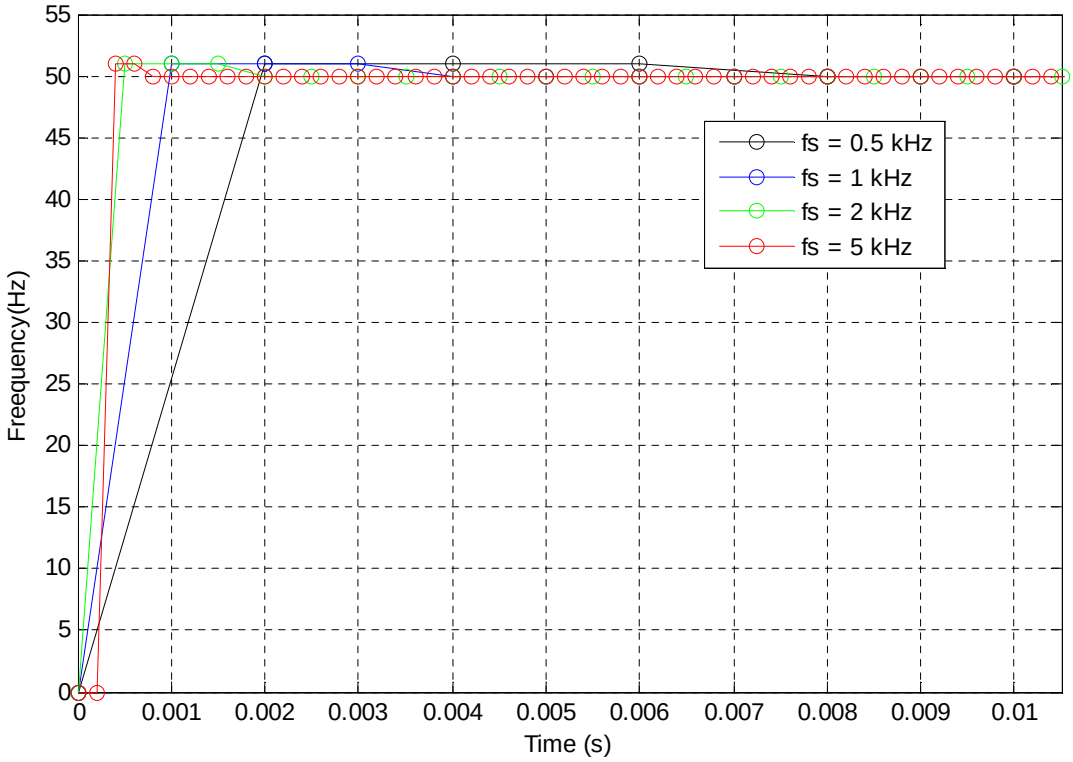


Figure 4.2: Frequency estimates of voltage signal at different sampling frequencies

4.1.4 Phase Estimation Using Energy Operator

4.1.4.1 Continuous Time Model

Apart from frequency, grid synchronization requires accurate and rapid estimation of grid voltage phase angle. The EO algorithm estimates the phase angle through the determination of the phase difference between two signals $v_x(t)$ and $v_y(t)$. The energy cross products [169] of these two are defined as

$$E[v_{xy}(t)] = \dot{v}_x(t)\dot{v}_y(t) - v_x(t)\ddot{v}_y(t) \tag{4.21}$$

$$E[v_{yx}(t)] = \dot{v}_y(t)\dot{v}_x(t) - v_y(t)\ddot{v}_x(t) \tag{4.22}$$

Since both these two voltages are sinusoidal functions of the same frequency, i.e. $v_x(t) = V_x \sin(\omega t + \phi_x)$ and $v_y(t) = V_y \sin(\omega t + \phi_y)$ the energy expression (4.21) can be written as

$$
\begin{aligned}
E[v_{xy}(t)] &= \dot{v}_x(t)\dot{v}_y(t) - v_x(t)\ddot{v}_y(t) \\
&= \omega^2 V_x V_y ((\sin(\omega t + \phi_x)\sin(\omega t + \phi_y)..... \\
&\qquad + \cos(\omega t + \phi_x)\cos(\omega t + \phi_y)) \\
&= \omega^2 V_x V_y \cos(\phi_x - \phi_y)
\end{aligned}
\tag{4.23}
$$

Likewise an expression (4.22) can be written by interchanging variables in (4.23), hence resulting in the same formula as (4.23), namely

$$E[v_{yx}(t)] = \omega^2 V_x V_y \cos(\phi_x - \phi_y) \tag{4.24}$$

Using expressions (4.23), (4.24) and combining them with the product of $E[v_x(t)]$ and $E[v_y(t)]$ from (4.7), one can derive the phase angle difference $\theta_{xy} = \theta_x - \theta_y$ between voltages $v_x(t)$ and $v_y(t)$ as

$$
\begin{aligned}
&\frac{E[v_{xy}(t)] + E[v_{yx}(t)]}{2\sqrt{E[v_x(t)] \times E[v_y(t)]}} = \frac{2V_x V_y \omega^2 \cos\theta_{xy}}{2V_x V_y \omega^2} = \cos\theta_{xy} \\
&\textit{hence } \theta_{xy} \quad = \cos^{-1}\left(\frac{E[v_{xy}(t)] + E[v_{yx}(t)]}{2\sqrt{E[v_x(t)] \times E[v_y(t)]}}\right)
\end{aligned}
\tag{4.25}
$$

The above shows the phase difference between two sinusoidal functions can be derived from the estimates of their respective energies and cross energies. This expression can be applied to estimate the instantaneous phase differences between any two of the three phases of the supplied voltage for synchronization.

4.1.4.2 Discrete Time Model

Similarly in discrete time form, the discrete cross energies of the two voltages $v_x(n)$ and $v_y(n)$ are given by (4.26) and (4.27) below.

$$E[v_{xy}(n)] = v_x(n)v_y(n) - v_x(n+1)v_y(n-1) \tag{4.26}$$

$$E[v_{yx}(n)] = v_y(n)v_x(n) - v_y(n+1)v_x(n-1) \tag{4.27}$$

Since $v_x(n)$ is defined by (4.7) and the second signal is taken as

$$v_y(n) = V_y \cos(\Omega_y n + \phi_y), \tag{4.28}$$

Using (4.8) and (4.28) the equation (4.26) can be expressed as

$$E[v_{xy}(n)] = V_x V_y \begin{pmatrix} \cos(\Omega_x n + \phi_x)\cos(\Omega_x n + \phi_y) \\ -\cos(\Omega_x (n+1) + \phi_x)\cos(\Omega_x (n-1) + \phi_y) \end{pmatrix} \tag{4.29}$$

Applying trigonometric identities (Appendix B1.4), this can be reduced to (4.30).

$$\begin{aligned} E[v_{xy}(n)] &= \frac{V_x V_y}{2}\left(\cos(\phi_x - \phi_y) - \cos(2\Omega_x + \phi_x - \phi_y)\right) \\ &= \frac{V_x V_y}{2}\left(\cos\theta_{xy} - \cos(2\Omega_x + \theta_{xy})\right) \end{aligned} \tag{4.30}$$

The alternate expression obtained by interchanging variables in (4.30) is

$$E[v_{yx}(n)] = \frac{V_x V_y}{2}\left(\cos\theta_{xy} - \cos(2\Omega_x - \theta_{xy})\right) . \tag{4.31}$$

It may be expected that the symmetrical expression obtained by averaging (4.30) and (4.31) will give lower noise errors in practice as it uses all 6 samples of the original signals, and it also leads to a simpler expression. With further trigonometric manipulation (Appendix B1.4), the sum of energies from two discrete time voltage variables can be simplified as

$$\begin{aligned} E[v_{xy}(n)] + E[v_{xy}(n)] &= V_x V_y \cos\theta_{xy}(1 - \cos 2\Omega_x) \\ &= 2V_x V_y \cos\theta_{xy} \sin^2\Omega_x \end{aligned} \tag{4.32}$$

Using expression (4.32) and the product of discrete energies $E[v_x(n)]$ and $E[v_y(n)]$ from (4.12), the expression for the phase angle difference $\theta_{xy} = \theta_x - \theta_y$ between both voltages in discrete time form can be derived as

$$\begin{aligned} \frac{E[v_{xy}(n)] + E[v_{yx}(n)]}{2\sqrt{E[v_x(n)] \times E[v_y(n)]}} &= \frac{2V_x V_y \cos\theta_{xy} \sin^2\Omega_x}{2V_x V_y \sin^2\Omega_x} = \cos\theta_{xy} \\ \theta_{xy} &= \cos^{-1}\left(\frac{E[v_{xy}(n)] + E[v_{yx}(n)]}{2\sqrt{E[v_x(n)] \times E[v_y(n)]}}\right) \end{aligned} \tag{4.33}$$

This is a simple formula requiring only 3 samples of each voltage $v_x(n)$ $v_y(n)$.

4.1.4.3 Effect of Sampling Frequency in Phase Estimation

Figure 4.3 illustrates the phase difference between two voltage signals $v_a(t) = \cos(\omega t + 0)$ and $v_c(t) = \cos(\omega t + 120)$ at various sampling

frequencies f_s = 0.5 kHz, 1 kHz, 2 kHz and 5 kHz. .This figure shows how the phase angle between the two voltages, which may be two phase voltages of a three-phase grid system, can be estimated. The phase estimation of the grid voltage requires only three consecutive samples of the signal and all frequencies conform at 120 degrees phase angle within $3 \times T_S$. Tracking of the phase is also shown to be accurate for all sampling frequencies. The phase rise and dip noticed is due to erroneous samples in the moving data frame during the 3 sample delay. This is shown to improve with higher sampling frequencies.

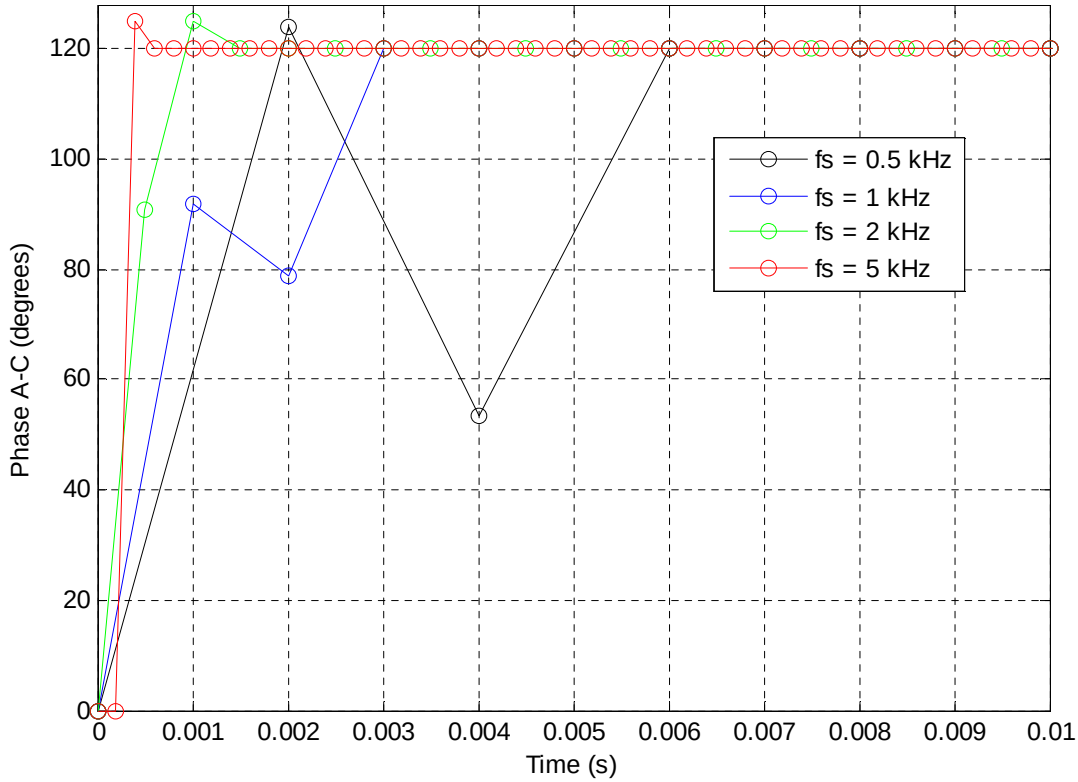


Figure 4.3: Phase angle estimation of a voltage signal at different sampling frequencies

4.2 Energy Operator Phase Locked Loop (EO-PLL)

Applying the solutions above in Section 4.1.3 and Section 4.1.4, the open loop energy operator-based phase locked loop scheme can be derived for voltage synchronization in any single or three-phase AC systems.

4.2.1 Energy Operator PLL (EO-PLL) Algorithm

Fig. 4.4 shows the block diagram of the energy operator phase locked loop algorithm which is explained below:

1. The samples of the measured three phase voltages $V_a(t)$, $V_b(t)$ and $V_c(t)$, are placed in a moving data window, of five samples for each phase. (the minimum number of samples needed) in a first-in and first-out (FIFO) order.
2. The sampled data are processed by using a chosen digital filter.
3. The filtered three-phase data are transformed into their equivalent α-β components in stationary reference frame. The α-β stationary reference frame serves as a reference to track the phase angle deviation between v_α and v_a under unbalance conditions as shown in Figure 4.5.
4. Using one of the three-phase voltages, say $V_a(n)$, and setting it as the reference $V_y(n)$, evaluating the energy and cross energy operators of one of the processed voltage components $v_\alpha(n)$, this leads to calculation of $E[v_\alpha(n)]$, $E[\dot{v}_y(n)]$, $E[v_y(n)]$, $E[v_{\alpha y}(n)]$, $E[v_{y\alpha}(n)]$ using equations (4.12), (4.18), (4.26) and (4.27).
5. Applying the results above, the frequency f_α and the phase relative to the alpha vector $\theta_{\alpha y}$ (in this case $\theta_{\alpha a}$) is evaluated using equations (4.20), (4.33) respectively.
6. Similarly steps (4) and (5) can be done for $V_b(n)$ Phase B and $V_c(n)$ Phase C by setting it as the reference $V_y(n)$ to get $\theta_{\alpha b}$ and $\theta_{\alpha c}$.
7. Finally, updating with the corresponding phase angles from step (5) and (6) give the phases θ_a θ_b and θ_c then integrating with the estimated frequency f_α creates a synchronized PLL signal for each phase.

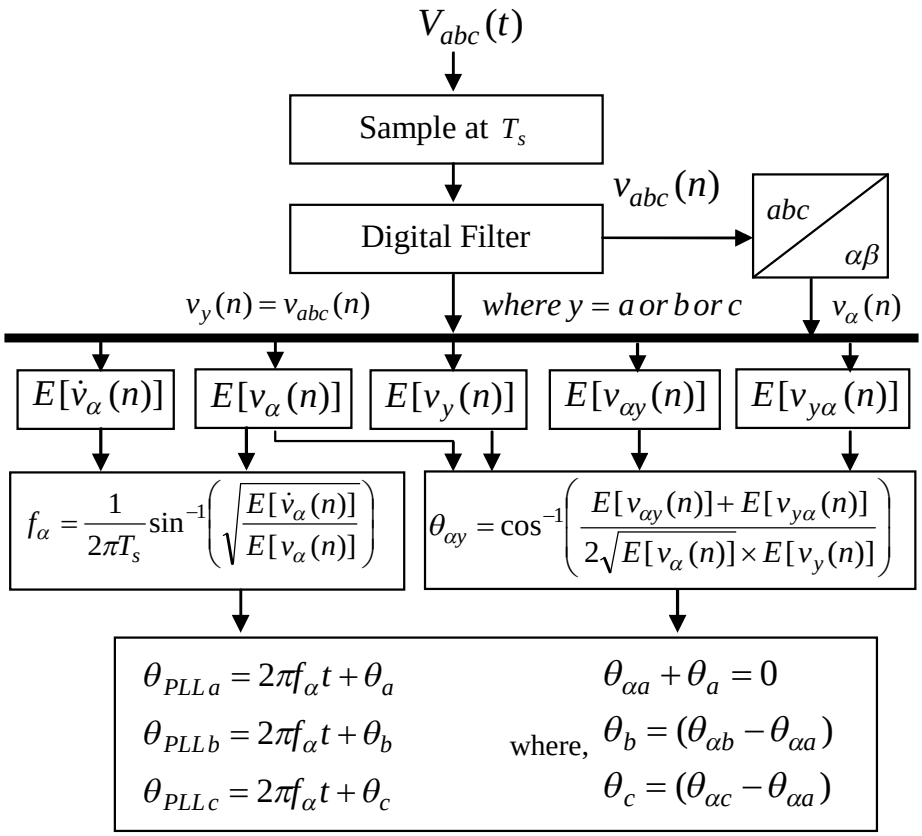


Figure 4.4: Block Diagram of EO-PLL Implementation

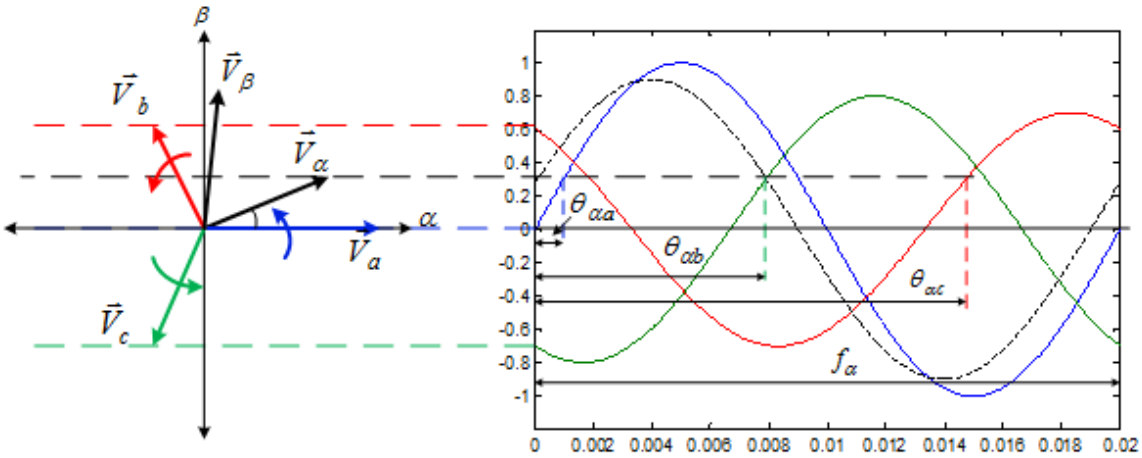


Figure 4.5: Graphical Illustration of EO-PLL Under Unbalanced Voltages

4.2.2 Features of EO-PLL Scheme

The key feature of the technique lies in its concurrent evaluations of three phase voltages for frequency and their relative phase angles for unbalanced voltage detection. The rationale can be explained by considering the angular difference between v_α and v_β components. Under a balanced condition this is 90°, and deviation from this value indicates the occurrence of voltage imbalance.

The algorithm evaluates this angular difference using procedure (3) above. With individual phase frequencies evaluated this leads to the estimation of individual phase angles. This approach is not dependent on the voltage amplitude and does not require positive sequence extraction.

In addition, as an open loop-based algorithm the EO-PLL is computationally more efficient and faster in responding to grid frequency variation than any of the closed-loop approaches.

Furthermore this individual phase-angle based analysis enables the tracking of single phase voltages and is beneficial for single phase application in three-phase distribution systems where loads vary at the different phases.

4.2.3 Filtering Requirements

Being a sample-based technique, the EO-PLL method is sensitive to noise [161]. This is like the other open-loop based methods, such as Mann and Morrison, Rockefeller and Udren algorithms[114, 182], involving estimation of derivatives from closely spaced samples. Thus it is important to have a suitably chosen sampling frequency and carefully designed filters, for the proposed EO algorithm to perform fast and accurate tracking of the grid voltage. A compromise between fast response speed and high accuracy is the key design issue for digital filters, and often a trial and error approach is required.

For measured grid voltage samples a band pass filter centred at the nominal grid frequency is appropriate. Moving average filters have been employed in [169] and digital filters including low order infinite-impulse-response (IIR), finite-impulse-response (FIR), DFT based filters such as recursive discrete Fourier transform (RDFT) and interpolated discrete Fourier transform (IpDFT) [115, 170] have all been suggested. However the use of DFT-based filters is at the expense of high computational cost and slower transient response as they require at least one fundamental cycle window length. For

this work, the DFT approach has been chosen because it is stability and accuracy.

In principle DFT transforms N equally spaced samples in the time domain into N complex values in the frequency domain representing the input signal.

The DFT and inverse DFT (IDFT) are based on equations given by (4.34) and (4.35) respectively:

$$V_{kf}(n) = \sum_{n=0}^{N-1} v(n)\, e^{-j\frac{2\pi kn}{N}} \quad \text{where n = 0…N-1} \tag{4.34}$$

$$v_{kf}(n) = \frac{1}{N} \sum_{n=0}^{N-1} V_{kf}(n)\, e^{j\frac{2\pi kn}{N}} \tag{4.35}$$

where, k is the frequency index, n is the sample count and N is the number of voltage samples present in the window.

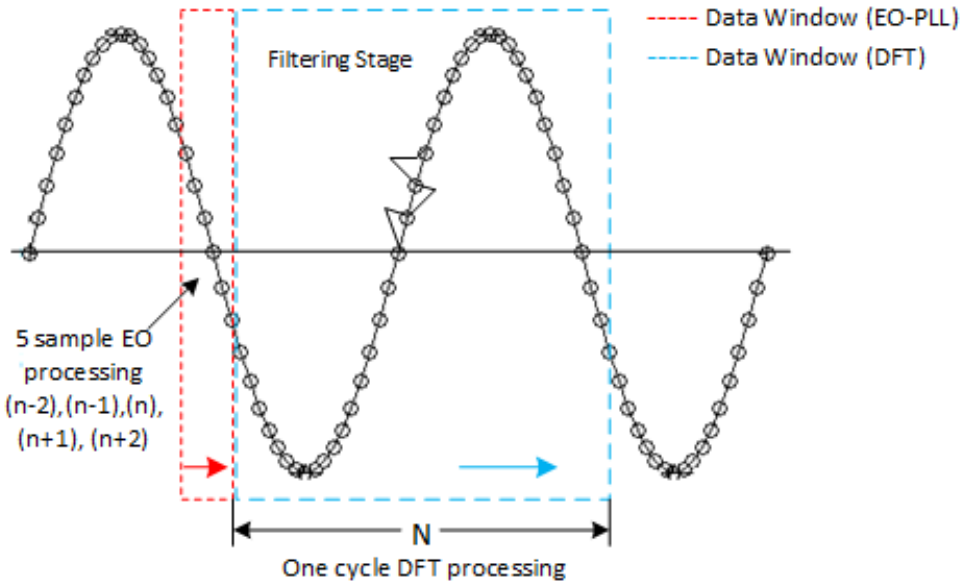


Figure 4.6: Data processing stages with a DFT as a filter

Figure 4.6 illustrates the data processing stages involved when using a DFT as a filtering algorithm. The key parameters are the sampling rate and data window. The former needs to be fast enough to prevent aliasing, the latter needs to be wide enough so that no frequency leakage occurs. In the application of the grid voltage signal which has a stable frequency around 50 Hz, it is relatively easy to choose both parameters. The sampling frequency chosen is 5kHz and widow width is for one fundamental cycle (200 samples).

Applying the above two expressions, implements a filter at the 50Hz fundamental frequency. The resulting expression is obtained from (4.34) after filtering, as given below.

$$v_{50}(n) = \frac{1}{N}\sum_{n=0}^{N-1} V_{50}(n)\, e^{j\frac{2\pi n}{N}} \tag{4.36}$$

4.3 Simulation Studies of EO-PLL Scheme

To validate the presented design approach, this section discusses a simulation study of the EO-PLL under three different grid voltage conditions. These include balanced voltage, unbalanced voltage due to grid faults and voltage corrupted with harmonics. For studying the EO-PLL scheme operating under the second condition, two popular closed loop PLL schemes which have been reported to be able to handle the situation; the Double Second Order Generalised Integrator (DDSRF-PLL) and Cascaded Delayed Signal Cancellation (CDSC-PLL) are used for comparison. The principles of both schemes are explained in Appendix B.2.

4.3.1Performance of EO-PLL with Balanced Voltage

The ability of the EO-PLL is investigated using a balanced three phase voltage under the condition when a transient change in frequency occurs. The performance of the scheme is assessed in terms of the response time and accuracy. The data sampling frequency is fixed at 5 kHz.

4.3.1.1Simulation Results

Figure 4.7 shows the frequency and phase angle estimated by the EO-PLL algorithm. At the time intervals 0.02 < t < 0.06, the voltages are balanced and the EO-PLL algorithm responds to track the frequency of 50Hz. At time instant t = 0.06s, the frequency of the three-phase voltages is raised from 50-55Hz, the EO-PLL algorithm responds and the frequency converges quickly to the correct value within 1ms. As can be seen in Figure 4.7 (d)-(e), the phase difference is kept to be -120° and+120° respectively since the three-phase voltages are well-balanced with similarly a fast response.

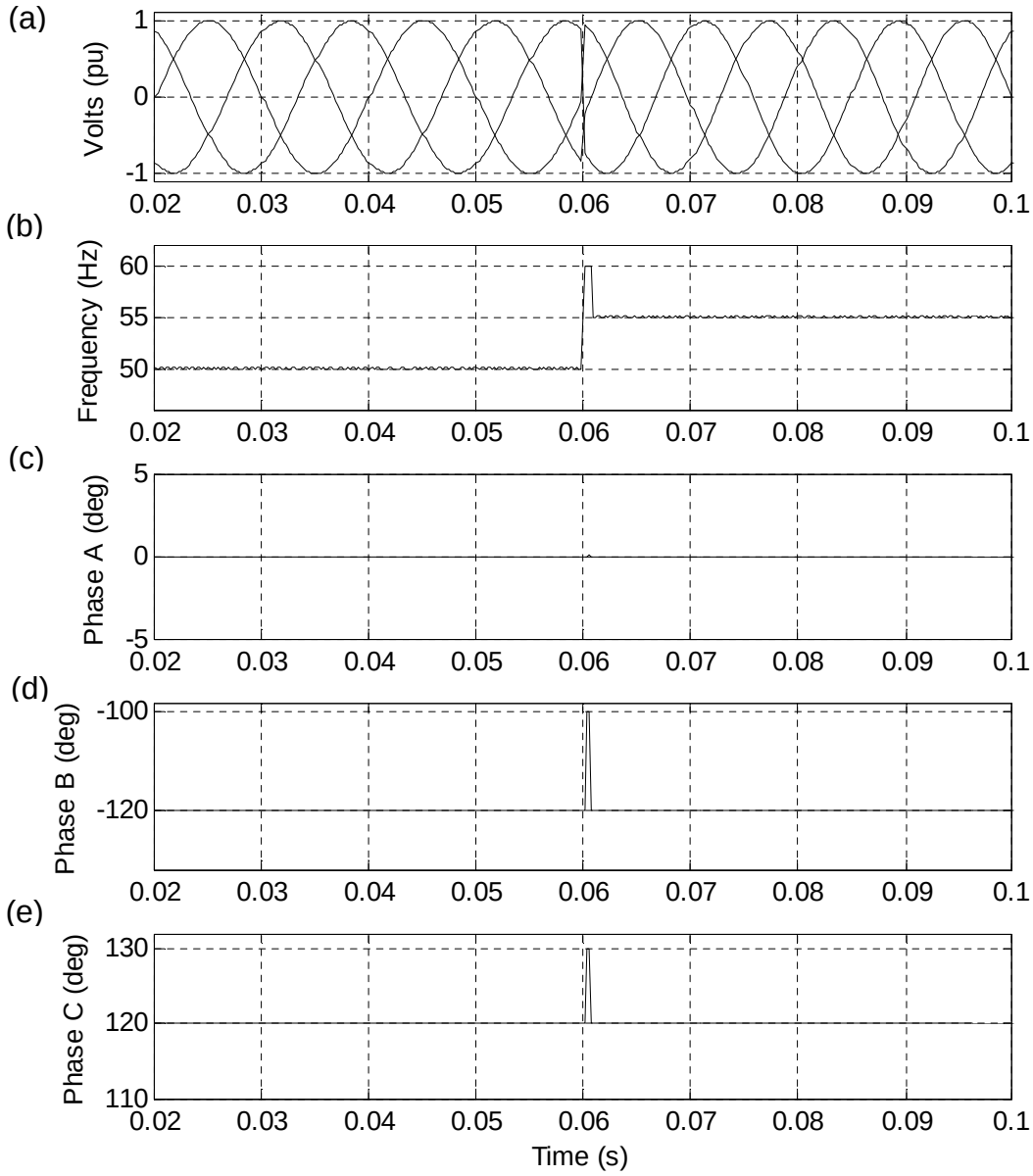


Figure 4.7: EO-PLL Under Balanced Voltage Conditions

4.3.2 Performance of EO-PLL with Unbalanced Voltage

DDSRF-PLL and CDSC-PLL are now compared with the proposed EO-PLL scheme in terms of response time, accuracy and computational efficiency.

It is well known that definition guidelines to classify voltage sags are still a highly debated topic [183, 184]. More recent guidelines, IEEE Std C37.242-2013 [185] with respect to previous clauses in IEEE std C37.118.1-2011 and IEC 61850-90-5 [185-187], detail some requirements for phase monitoring

units under unbalanced signals. A similar test approach is used here to compare response times of the three schemes.

Two network faults are investigated, the single phase grid fault (type B) resulting voltage sag of -20% at Phase A and a phase to phase grid fault (type C) voltage sag of -20% at Phases B and C respectively at a nominal frequency of 50Hz.

The phasor diagrams for both cases are shown in Figure 4.8. The proportional and integral gains of the P+I controllers in the DDSRF-PLL and CDSC-PLL are set to have the same bandwidth of 300Hz. All grid voltage measurements are normalized with respect to the base voltage. The sampling frequency for the EO-PLL is at 2 kHz.

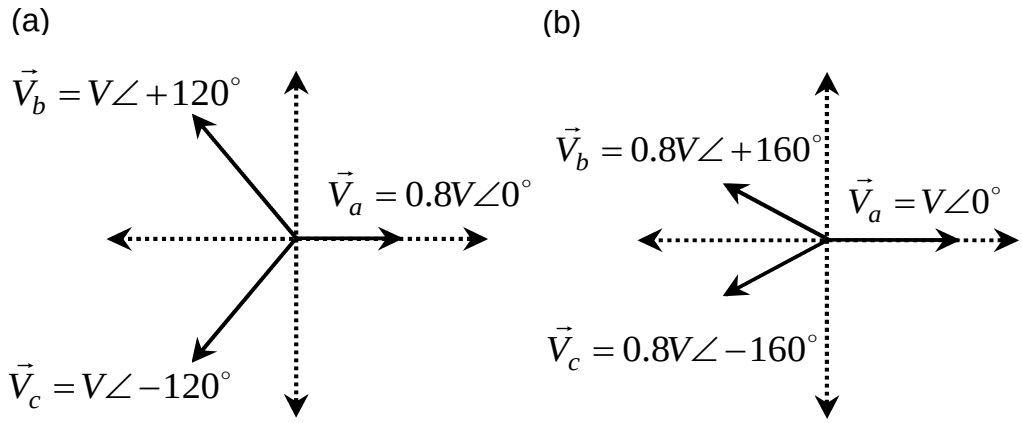


Figure 4.8: (a) Single phase grid fault – Type B (b) Phase to phase grid fault -Type C

4.3.2.1 Simulation Results - Type B Fault

Figure 4.9 and Figure 4.10 illustrate the ability of the three schemes to synchronize to grid voltages under this fault condition. The power system and synchronization schemes operate normally until at time 0.2s, the grid fault occurs with a frequency variation of 0.1Hz. As expected there is a 20% voltage drop in Phase A to 0.8 pu. The DDSRF-PLL scheme is seen to settle down to steady state after 3 cycles (0.06s) whilst the CDSC-PLL achieves this within 2 cycles (0.04s). The EO-PLL is shown to be a better scheme since it shows the fastest response in tracking the frequency after 2.5 ms ($5\times T_s$) and phase change of the individual voltages after 1.5 ms ($3\times T_s$).

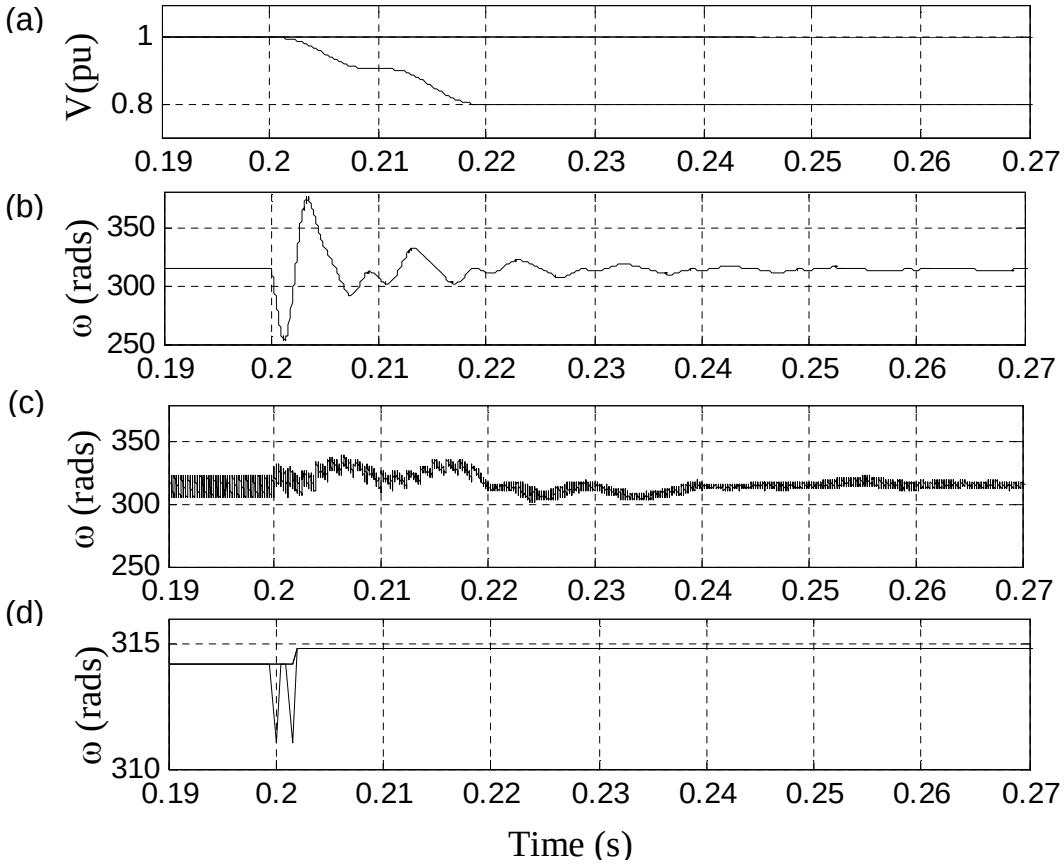


Figure 4.9: Comparison of response times for frequency tracking under type B fault (a) Peak Voltage (pu) (b) DDSRF-PLL, (c) CDSC-PLL, (d) EO-PLL

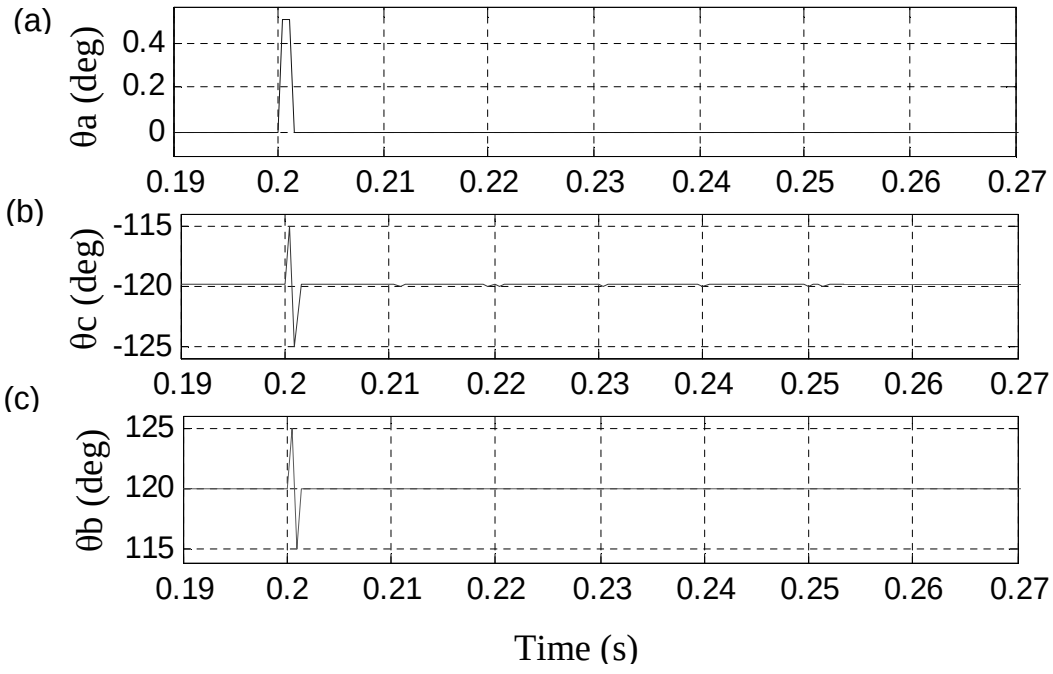


Figure 4.10: EO-PLL Estimation of Phase Angles under type B fault; (a) Phase A (degrees) (b) Phase C (degrees), (c) Phase B (degrees)

4.3.2.2 Simulation Results - Type C Fault

Figure 4.11 and Figure 4.12 show the results of the same three PLL schemes under type C grid fault. The DDSRF-PLL scheme is seen to reach steady state after 3 cycles (0.06s) whilst the CDSC-PLL achieves this within 2 cycles (0.04s). Similarly, the EO-PLL is shown to be superior, since it has the fastest response speed in tracking the frequency after 2.5 ms ($5\times T_s$) and phase change of the individual voltages within 1.5 ms ($3\times T_s$). In addition, unlike the other two schemes, with the EO-PLL the frequency and phase angle converge to their respective correct values with no transient oscillations as shown in these two figures,

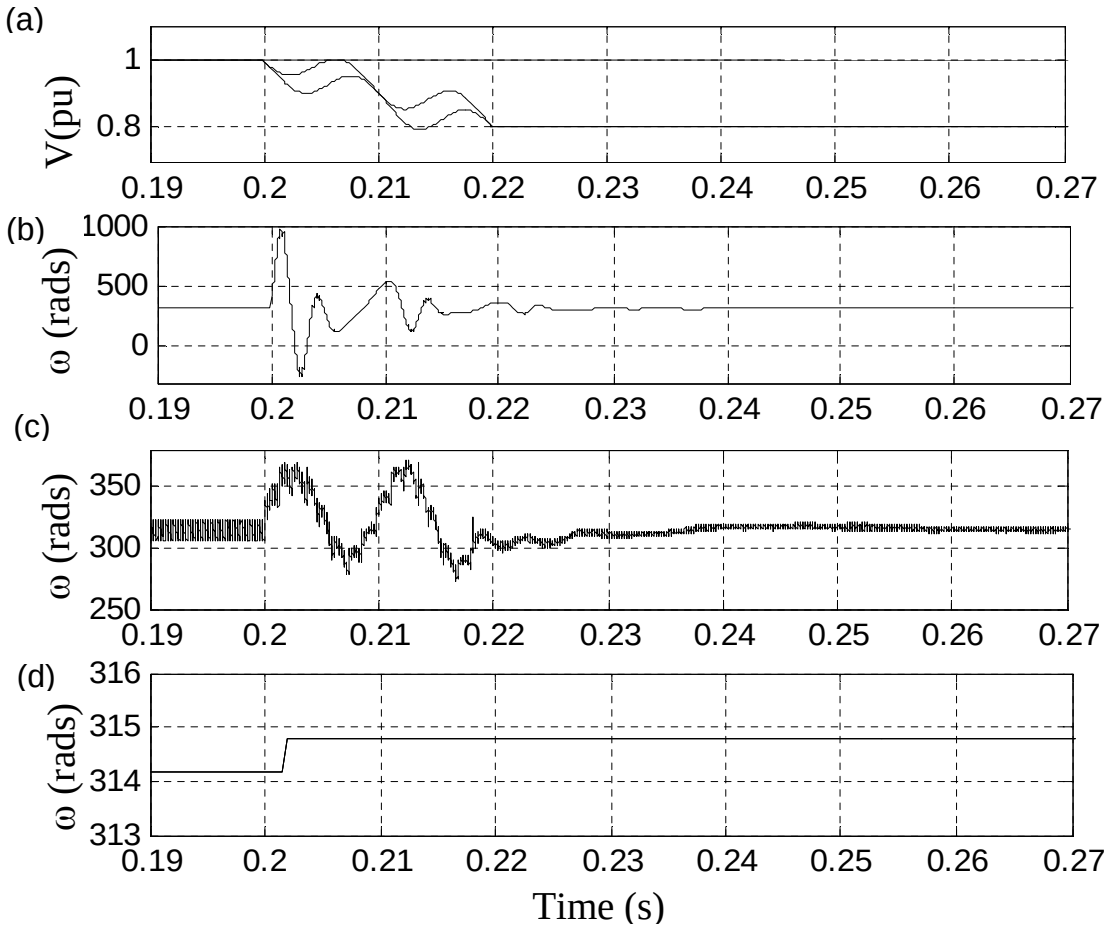


Figure 4.11: Comparison of response times of schemes for angular frequency tracking under type C fault (a) Peak Voltage (pu) (b) DDSRF-PLL, (c) CDSC-PLL, (d) EO-PLL

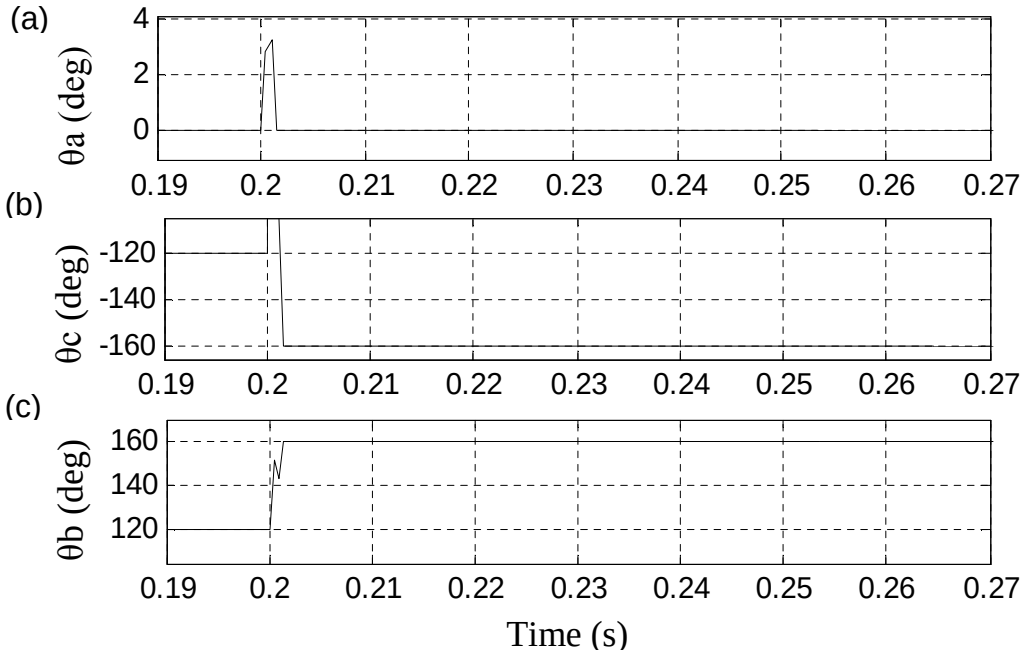


Figure 4.12: EO-PLL Estimation of Phase Angles under type C fault; (a) Phase A (degrees) (b) Phase C (degrees), (c) Phase B (degrees)

4.3.2.3 Computational Complexity

Based on the SIMULINK models used in the above investigations, the computational complexity of each scheme is summarized in Table 4.1. In terms of simple arithmetic calculations EO-PLL has a higher number of operations than that of DDSRF, but is significantly less than CDSC. It uses least number of trigonometric calculations; consequently the response time for the EO-PLL is also significantly faster compared to both DDSRF and CDSC schemes.

Table 4.1: Complexity of the Schemes Based on Performance

Method	Number of Operations		Response Time
	Arithmetic	Cos and Sine	
EO-PLL	30	7	$5\times T_s$
DDSRF	17	8	0.06s
CDSC [2,8,16]	76	16	0.04s

4.3.3 Performance of EO-PLL with Voltage Corrupted with Harmonic Noise

A combined EO-PLL scheme with a DFT filter discussed earlier in Section 4.2.3 can provide a solution for synchronisation for voltage corrupted with harmonic noise. These are now investigated in terms of response time, accuracy. The harmonic distortions injected on these voltages were based on IEC 61000-3-6 compatibility level standards for low and medium voltage networks [188]. This is summarized in Table 4.2 below. The data sampling frequency is fixed at 5 kHz.

Table 4.2: Compatibility Levels For Individual harmonic Voltages in Low and Medium Voltage Networks Reproduced from IEC 6100-3-6.

Odd harmonics non-multiple of 3		**Odd harmonics multiple of 3**		**Even harmonics**	
Harmonic Order (h)	Harmonic Voltage (%)	Harmonic Order (h)	Harmonic Voltage (%)	Harmonic Order (h)	Harmonic Voltage (%)
5	6	3	5	2	2
7	5	9	1.5	4	1
11	3.5	15	0.4	6	0.5
13	3	21	0.3	8	0.5
$17 \le h \le 49$	$2.27.\frac{17}{h} - 0.27$	$21 < h \le 45$	0.2	$10 \le h \le 50$	$0.25.\frac{10}{h} + 0.25$

4.3.3.1 Simulation Results

Figure 4.13 shows an example of unbalanced three-phase voltages and their corresponding waveforms after being processed by DFT filter. At time 0.06s, step changes in magnitudes of -20% and -50% are imposed on Phases B and C voltages respectively. As can be seen in Figure 4.13 (d) after a time delay of 0.021 s (one fundamental cycle + $5\times T_s$) the frequency estimation is completed and in Figure 4.13 (d)-(f) estimations of three phase angles are converged within a duration of 0.0206s (one fundamental cycle + $3\times T_s$). These results highlights the fact that the time required for implementing EO-PLL algorithm is significantly shorter than that of DFT. The total response time for this PLL algorithm is mainly due to the duration of the DFT window.

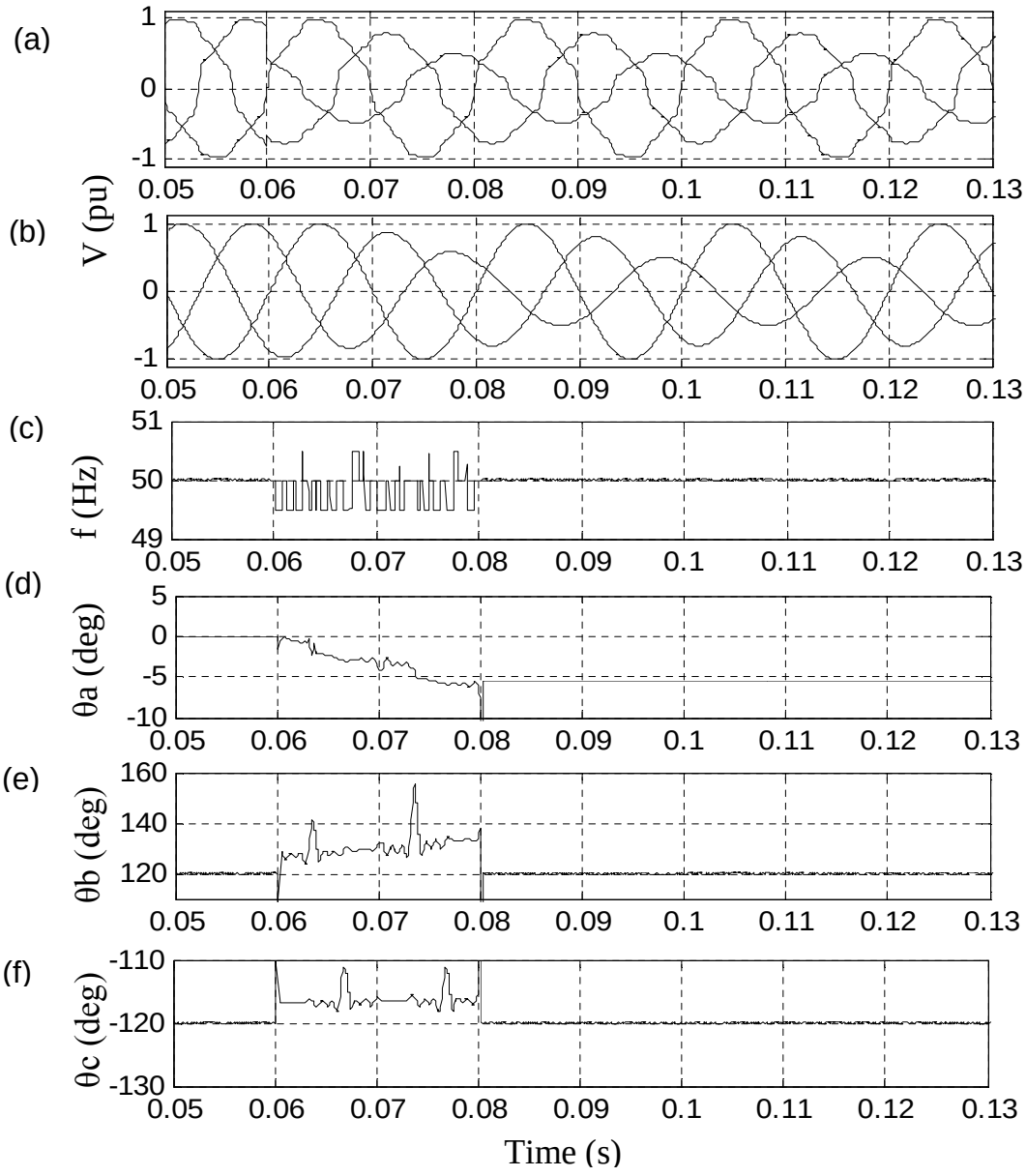


Figure 4.13: (a) Voltage with harmonics, (b) Voltage after DFT, (c) frequency detection, (d) –(f) Phase detection (A,B,C)

4.4 Experimental Validation of EO-PLL

The performance of the EO-PLL synchronization technique has been verified experimentally using a practical setup, as shown in Figure 4.14. This consists of a 96 MHz mbed NXP LPC1768 microcontroller as an AC voltage generator for 50Hz 3-phase voltage signals, and a 120 MHz EA NXP LPC4088 microcontroller acting as the signal processing and control unit and is able to provide high enough resolution and sample rate for the internal A2D converters. In this study, phase estimation is validated by the phase deviation caused between the α-β voltage vectors and frequency estimation using the v_α voltage vector.

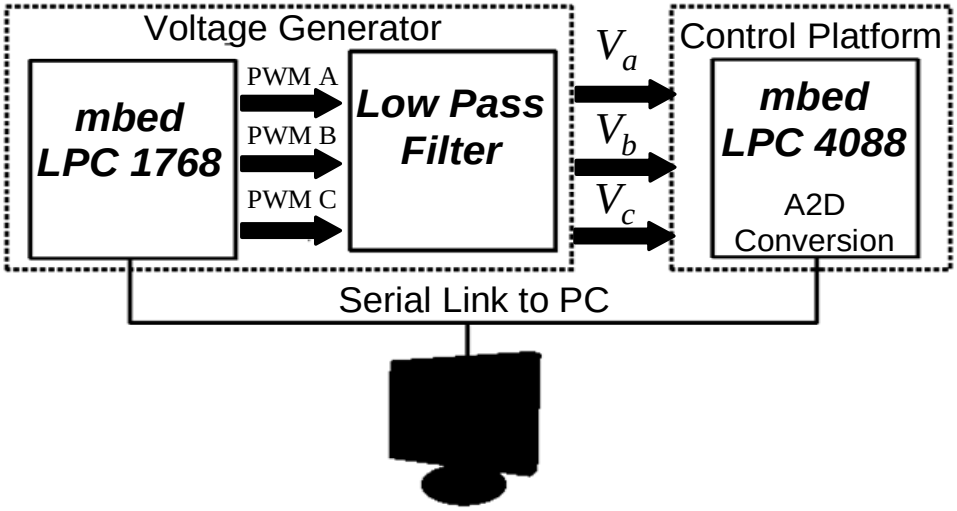


Figure 4.14: EO-PLL hardware test circuit setup

4.4.1 Voltage Generation

The LPC1768 micro-controller was programmed to generate a 3-phase voltage, emulating the AC grid voltage, produced as a 20 kHz PWM signal via the PWM output pins. Voltage generation is realised using a sine lookup table (LUT) of length=400 and phase indices initialised at 0, 267 and 133 for phases A, B and C respectively.

This device was also programmed to introduce grid conditions of frequency and phase change, and voltage imbalance by variation of the modulating index in a given phase.

The C-code listing for the device is given in Appendix B 3.1. Figure 4.15 shows the flowchart for the signal generation program.

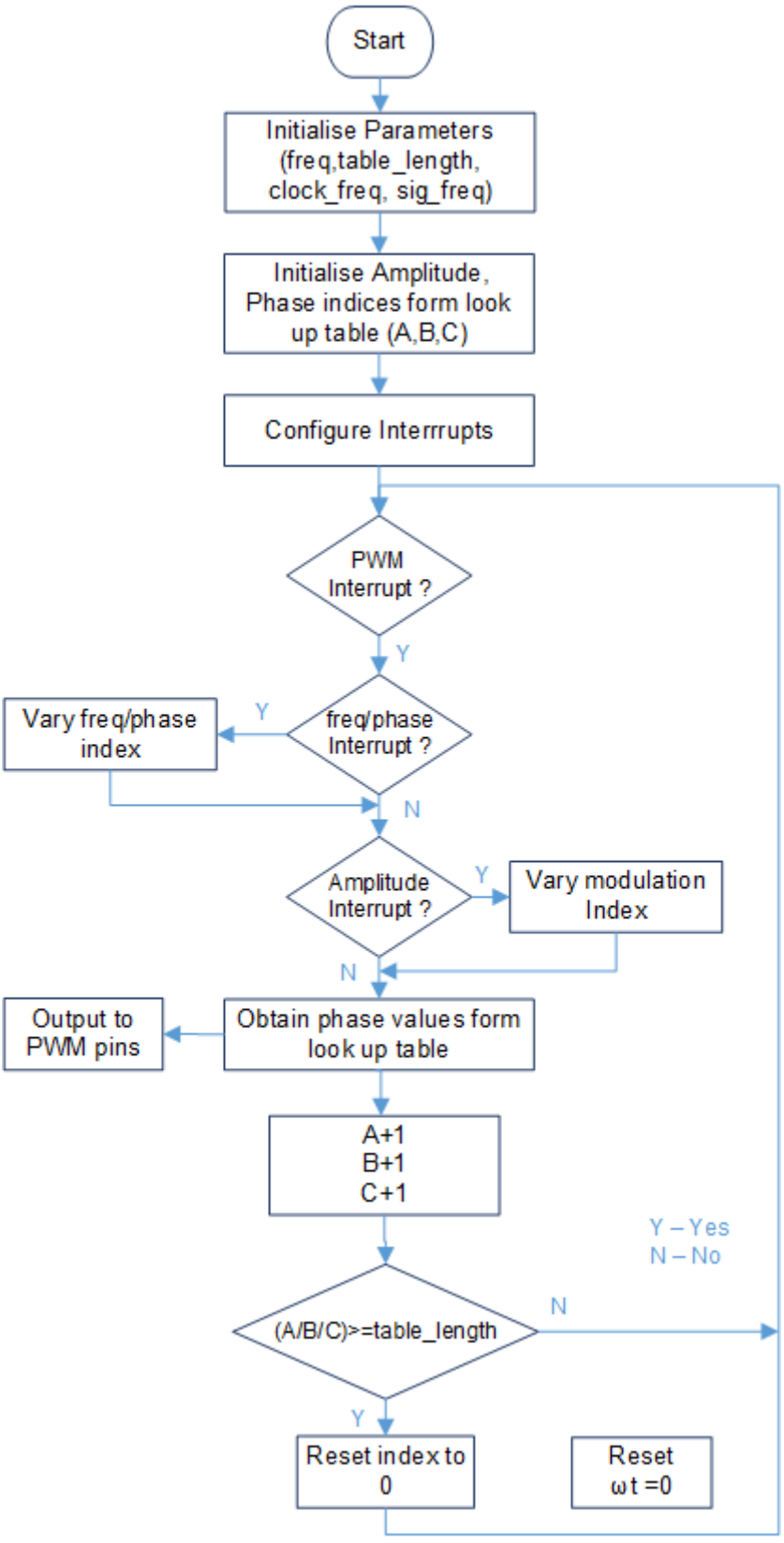


Figure 4.15: Voltage Generation Program Flow Chart

4.4.1.1 Filtering Requirements

For this experiment, the amplitude, frequency and phase of the PWM voltage waveform can be varied to create grid voltage fault scenarios. In other to see the actual voltage signal, a RC low pass filter is constructed at a cut off frequency of 60Hz with component values chosen as R= 8kΩ, C = 0.33µF. This low pass filter is different from that used in pre-filtering stage described in the EO-PLL.

The choice of the filter at the pre-filtering stage depends mainly on the low and high frequency harmonics present in the sinusoidal voltages and the A/D sampling frequency. Since the EO-PLL is a sample based technique, it is prone to noise and there is a trade-off between sampling time, harmonics and delays. Higher sampling frequencies require more complex digital filters to get accurate estimation with lower delays whereas lower sampling frequencies lead to estimations with less filtering but with larger delays. The DFT as discussed earlier in Section 4.2.3 has been successfully implemented as filter and shown to handle high frequency estimations with energy operator [170]. This is mainly because it can be used as a selective band pass filter with a narrow frequency bandwidth. Although this works well at high frequencies, there is still an imminent one cycle delay (20ms)

At the pre-filtering stage of in this experiment, a moving average filter is used and is programmed within the mbed LPC 4088 control platform. This averages the calculated frequency and phase estimations over 10 sample steps resulting in a minimum delay of 10ms at 1 kHz sampling. Although this is a crude estimation, it gives accurate results with acceptable ripple deviations and the time delay is shorter compared to the DFT. This makes this application possible in system controllers with multiple A/D samplers that can work at different sampling frequencies.

.

4.4.2 Signal Processing

The EO-PLL technique involves large mathematical computations. This calls for a processor with a high processing speed, suitable memory and preferably floating point arithmetic, to reduce on processing delays. The EA LPC4088 was chosen for its relatively high clock speed of 120 MHz, 8 MB flash memory and ability to implement floating point operations.

The output of the RC filter is applied to analog-to-digital converter (ADC) pins of the LPC4088 to enable the estimation of frequency, phase and derivation of the PLL angle using the EO-PLL model. Figure 4.16 shows the program flowchart for this device. Results obtained at each stage of the program are sent to the PC via a serial link to allow enable online analysis.

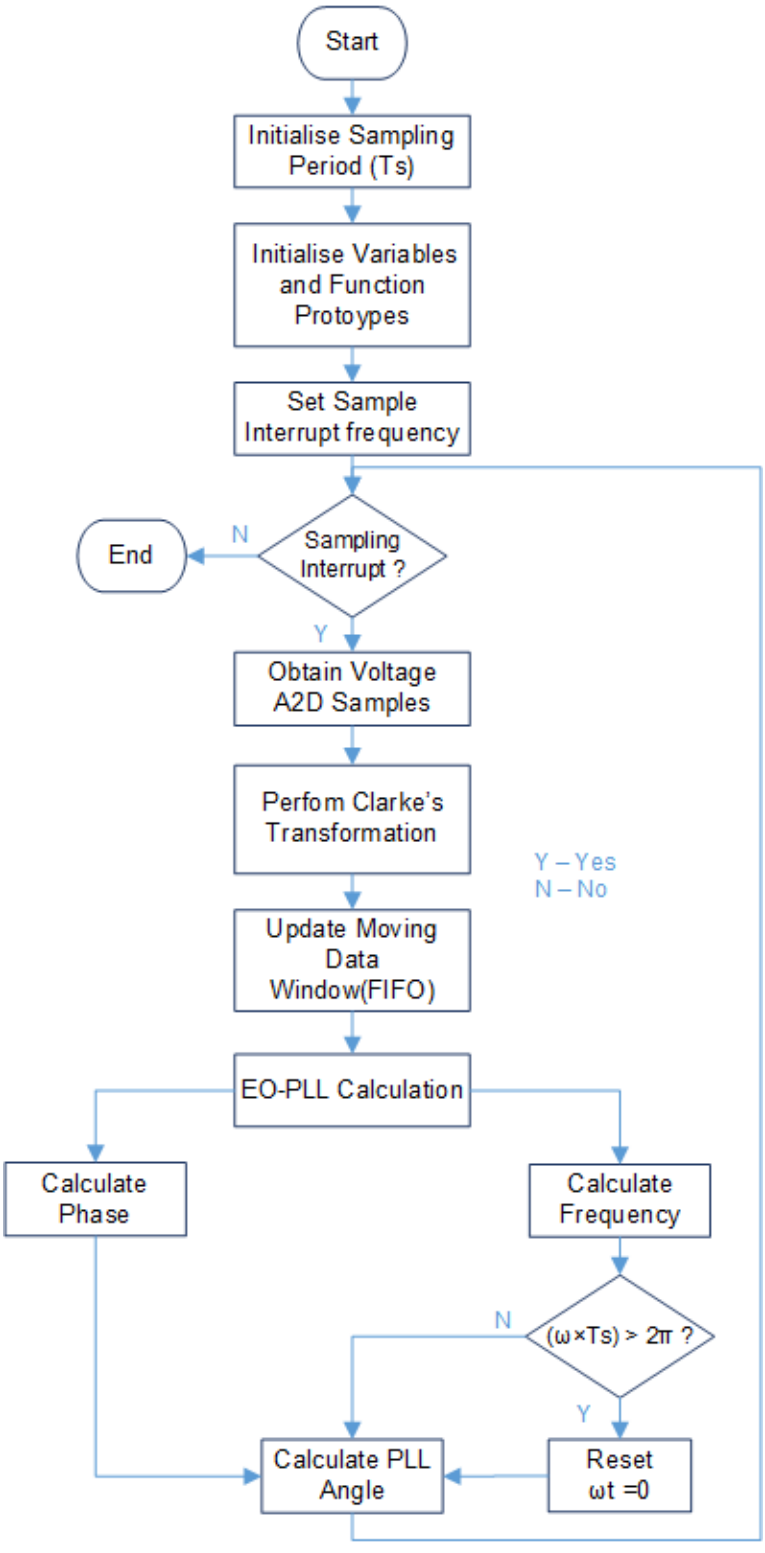


Figure 4.16: Program Flow Chart for EO-PLL Scheme

4.4.3 Experimental Studies of EO-PLL Scheme

The ability of the EO-PLL scheme is investigated under balanced voltage and unbalanced voltage. In this study, the data sampling frequency is fixed at 1 kHz and a moving average filter at 10 sample instants is used at the digital filtering stage to reduce the noise to achieve more accurate results. This introduces a delay response of at least 10 ms under transient changes.

4.4.3.1 Performance of EO-PLL with Balanced Voltage

Figure 4.17 shows the frequency and phase angle estimated by the EO-PLL algorithm. At the time intervals 19.94 < t < 19.98, the voltages are balanced and the EO-PLL algorithm responds to track the frequency of 50Hz. At time instant t = 19.98s, the frequency of the three-phase voltages is raised from 50-55Hz, the EO-PLL algorithm responds and the frequency converges quickly to the correct value. Though there is a ripple of ±1 Hz observed due to the noise remaining in the voltage signal even with the use of the moving average filter. The phase angle estimation gives the angle between v_α and v_β vectors derived from α-β transformation of the 3-phase voltage waveforms. As can be seen in Figure 4.17 (c), the angular difference is kept to be 1.57 rads (90°) since the three-phase voltages are well-balanced. The small phase ripple of approximately ±0.03 rads can be noticed and is also due to the noise in the measured data. The settling time of approximately 10 ms is observed.

Figure 4.18 shows the nature of the estimations without the pre-filtering stage. The response times are faster within 5ms but compared to Figure 4.17 the waveforms are shown to have more noise. The frequency ripple observed is now within ± 3Hz and the phase ripple larger at ±0.1 rads.

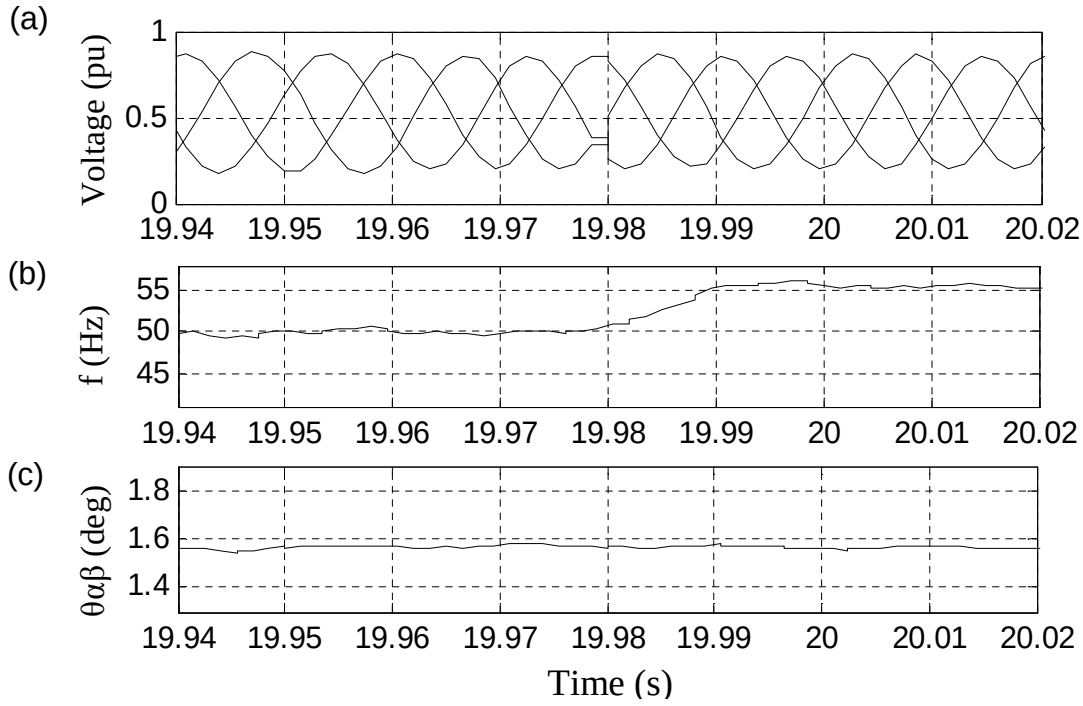


Figure 4.17: Experimental EO-PLL tracking changes in frequency from 50-55 Hz: a) Generated 3-phase voltage, b) estimated frequency, c) estimated phase

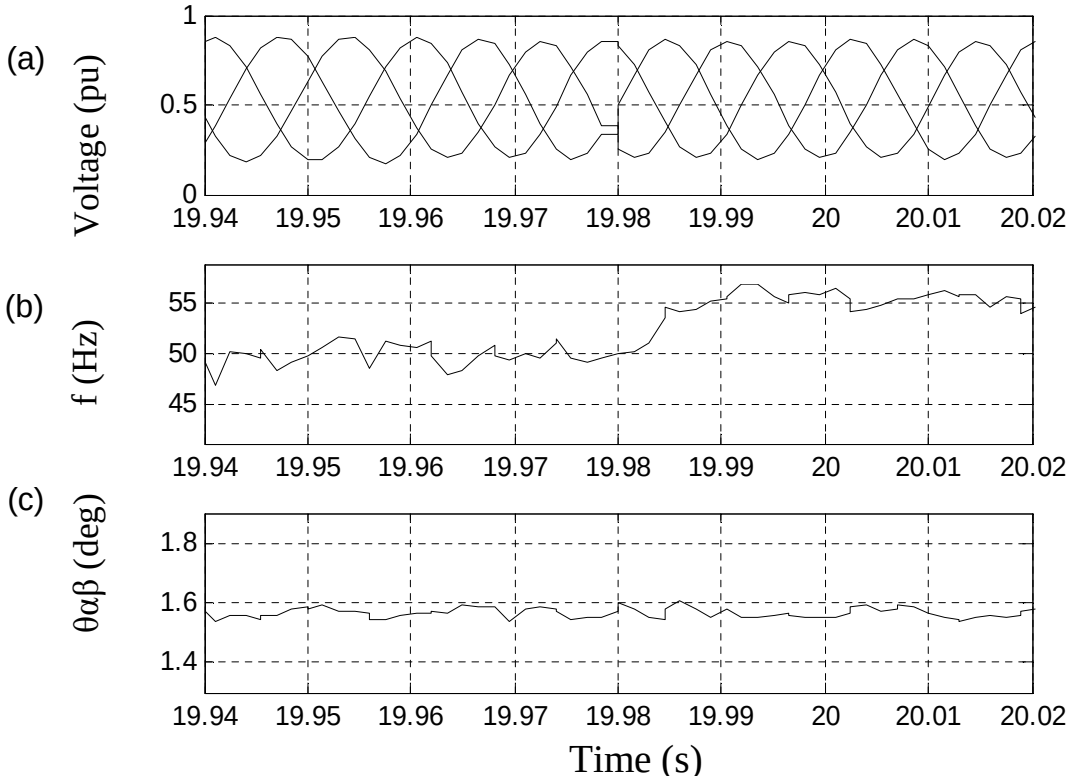


Figure 4.18:Experimental EO-PLL tracking changes in frequency from 50-55 Hz with no pre-filtering : a) Generated 3-phase voltage, b) estimated frequency, c) estimated phase

4.4.3.2 Performance of EO-PLL with Unbalanced Voltage

To investigate the EO-PLL's capability of tracking unbalanced grid voltage, the generated three-phase voltages were varied with a 50% and 80% magnitude reductions respectively in phase-B and phase-C voltages at 50.08 s as shown in Figure 4.19 (a). The technique is seen to accurately track the frequency and phase in each case. As the voltage is unbalanced and phase unsymmetrical, the measured phase value changes from the ideal 1.57 rads to 1.8 rads. The result converges quickly to the correct phase value within 10 ms. The phase and frequency ripple observed are the same as that of previous case with a frequency and phase ripple of ±1 Hz and ±0.03 rads respectively.

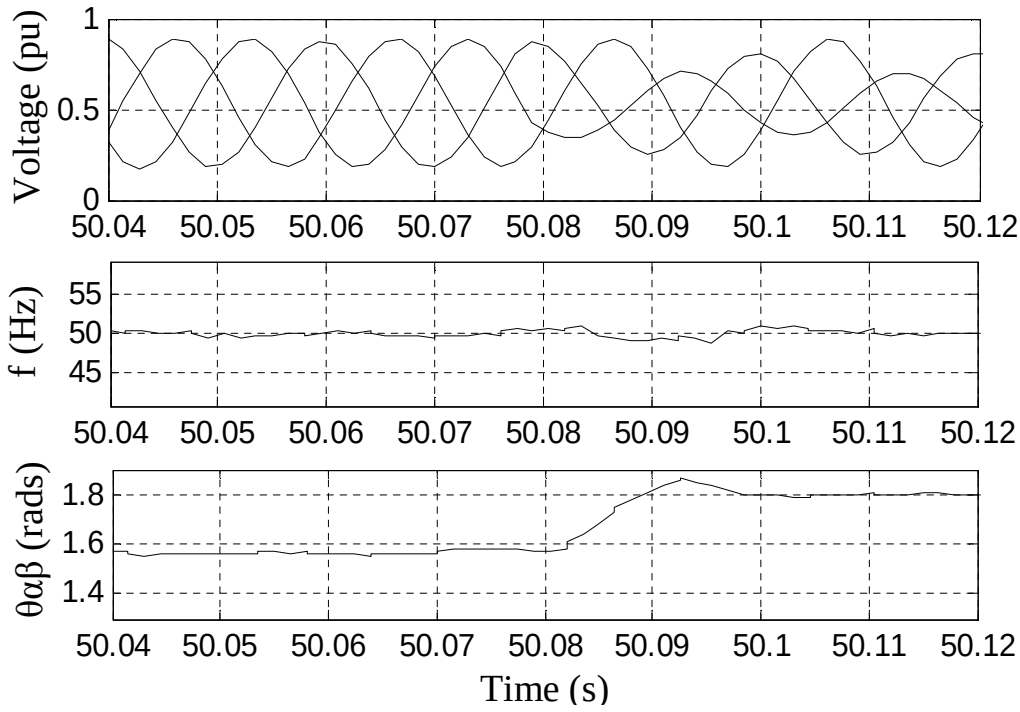


Figure 4.19: Detected result for 50% and 80% reduction in phase-B and phase-C respectively amplitude: a) Generated 3-phase voltage, b) estimated frequency, c) estimated phase

Figure 4.20 shows the nature of the estimations without the pre-filtering stage. Compared to Figure 4.17 the waveforms are shown have more noise and the frequency ripple is at ± 5Hz and the phase ripple larger at ±0.1 rads. This shows the effect of harmonics within the 60Hz cut-off frequency band.

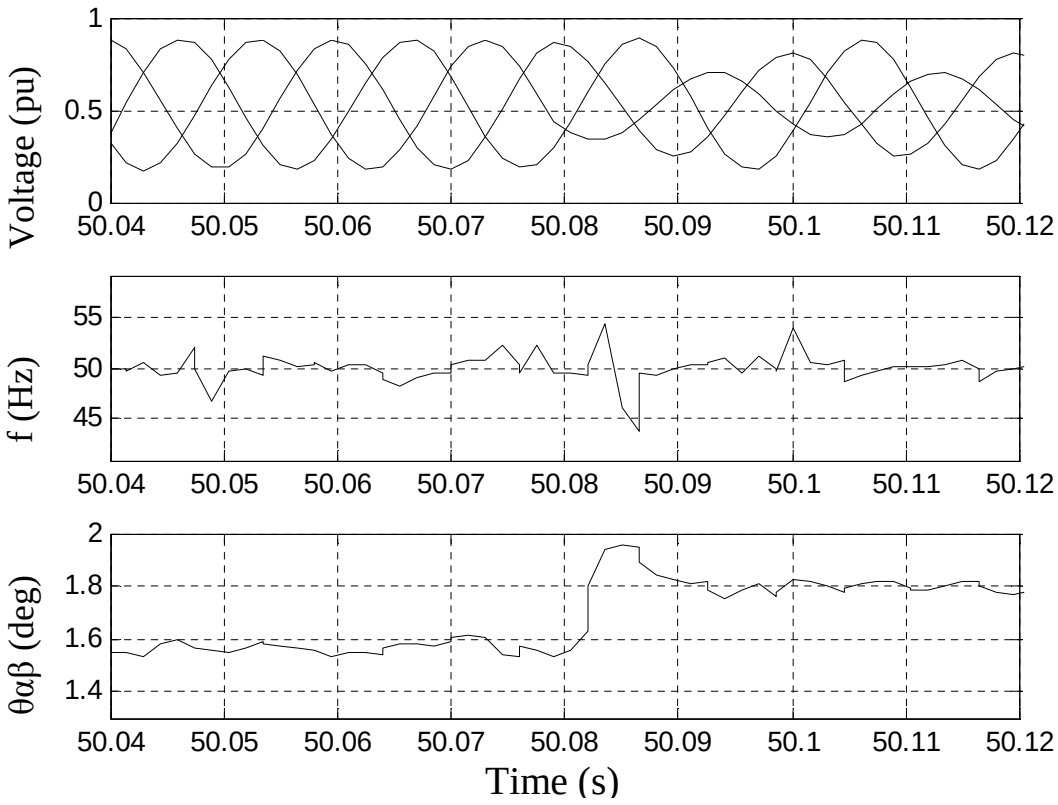


Figure 4.20: Detected result for 50% and 80% reduction in phase-B and phase-C respectively amplitude with no pre-filtering: a) Generated 3-phase voltage, b) estimated frequency, c) estimated phase

4.5 Conclusions

A novel EO-PLL technique has been presented and its principle and implementation procedures were explained. This open-loop PLL scheme combines two different EO operations and has been shown to achieve fast and accurate detection of frequency and phase angle when combined with an appropriate filter. Comparative studies of this technique with two other well-known closed-loop PLL schemes have been performed under two unbalanced voltage conditions. Results have shown that the EO-PLL outperformed the others in terms of fast response speed and good accuracy in tracking. Further validation of this technique has been carried out by investigating this technique under voltage harmonics. Simulation results show the technique works well when a suitable filter is chosen. Finally, a hardware implementation of this EO-PLL has also been reported in this chapter showing the simplicity of the method.

Chapter 5
FC-MMC Based STATCOM

This chapter presents the application of the FC-MMC discussed in Chapter 3 to function as a STATCOM for voltage regulation and reactive power compensation in power distribution systems. It starts by reviewing the power flow relationships of a simple system with two voltage sources, one representing the voltage at the PCC and the other a voltage-sourced converter, connected on the same node and separated by only an inductive impedance. Conditions for this system to achieve either equal voltage magnitudes or unity power factor are analysed. Following this analysis the chapter explores the relationships of the minimum required power (and voltage ratings) of the converter with the filter impedance and load power when used for reactive compensation. Subsequently, the application of an FC-MMC as a STATCOM for a simple balanced three-phase power system is investigated via simulation. The study investigates this STATCOM for two operating conditions:

- Regulating the PCC voltage magnitude to maintain it at the required level;
- Reactive power compensation to achieve power factor correction at the PCC.

Simulation results for the above study are presented with detailed discussions.

5.1 Power Flow Analysis

Figure 5.1 shows a one-line representation of a three-phase system with the grid modelled Thevenin equivalent consisting a voltage source V_S and impedance $Z_S = R_S + jX_S$, supplying power $P_L + jQ_L$ to an inductive load. An FC-MMC STATCOM is connected with the load at the point of common coupling (PCC) through its filter impedance $Z_C = R_C + jX_C$ Z_C. The converter supplies reactive power Q_C to the PCC.

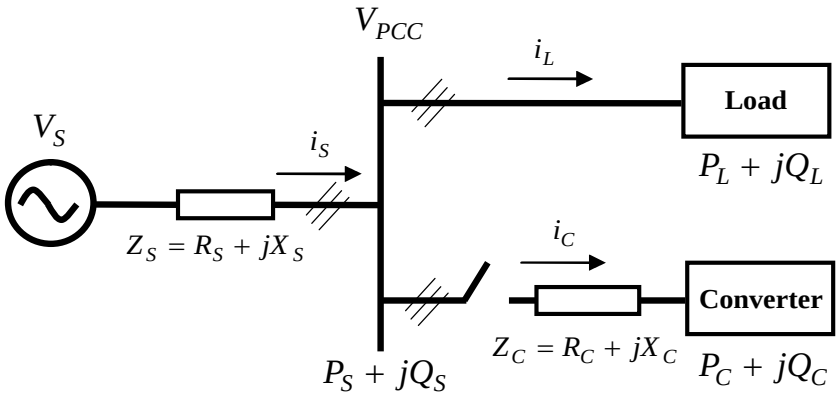


Figure 5.1: Single Line Diagram of Power System

With the converter unconnected, the current through Z_S is the same as that through the load $(i_S = i_L)$ and causes a voltage drop $\Delta V = V_S - V_{PCC}$ between the grid side and PCC.

Considering an inductive load, the current i_S can be determined by the complex power of the load and taking V_{PCC} as the reference $(V_{PCC} = V\angle 0^0)$ as

$$i_S = \frac{P_S - jQ_S}{V_{PCC}} \quad , \tag{5.1}$$

and the voltage drop along the line impedance is

$$\Delta V = i_S Z_S = R_S i_S + jX_S i_S \tag{5.2}$$

from (5.1)

$$\Delta V = (R_S + jX_S)\frac{P_S - jQ_S}{V_{PCC}}$$

$$\Delta V = \frac{(R_S P_S + X_S Q_S)}{V_{PCC}} + j\frac{(X_S P_S - R_S Q_S)}{V_{PCC}} \tag{5.3}$$

Thus ΔV can be resolved into its vector components $\Delta V = \Delta V_{R_S} + j\Delta V_{X_S}$ and expressed as

$$\Delta V_{R_S} = \frac{(R_S P_S + X_S Q_S)}{V_{PCC}} \tag{5.4}$$

$$\Delta V_{X_S} = \frac{(X_S P_S - R_S Q_S)}{V_{PCC}} \tag{5.5}$$

where, ΔV_{R_S} and ΔV_{X_S} are respectively the real and imaginary voltage drops due to the active power, reactive power and distribution line impedance.

Phasor diagrams showing the relationships of voltages and current in the system are given in Figure 5.2.

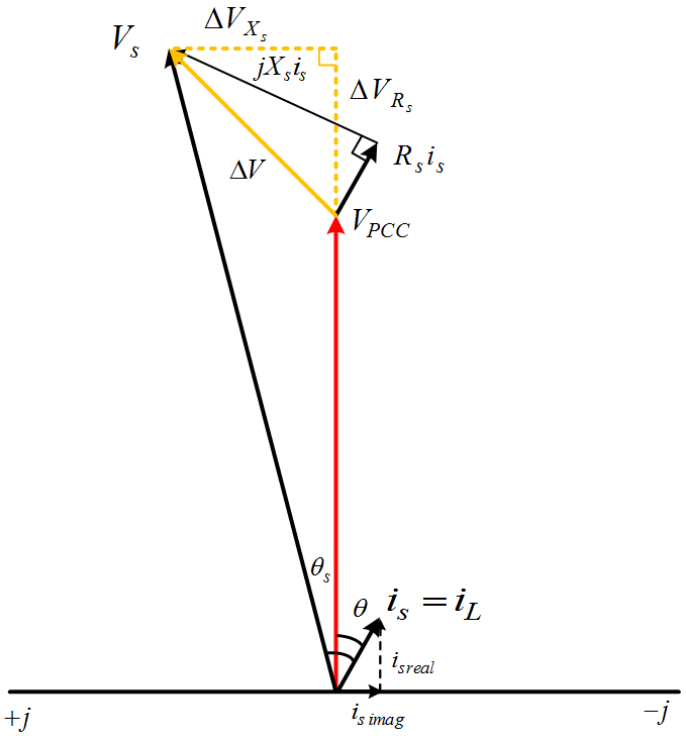


Figure 5.2: Phasor Diagram between Grid Side and PCC

5.1.1 PCC Voltage Regulation

The converter based compensator can be controlled to supply adequate amount of reactive power Q_C so that to achieve $|V_S| = |V_{PCC}|$. The condition for this is analysed below: Considering the real and imaginary components of voltage drop across the line impedance due to load and compensating currents, we have relationship between V_S and V_{PCC} given as $|V_S| = |(V_{PCC} + \Delta V_{R_S}) + j\Delta V_{X_S}|$

$$|V_S|^2 = (V_{PCC} + \Delta V_{R_S})^2 + \Delta V_{X_S}{}^2$$

Substituting ΔV_{R_S} and ΔV_{X_S} using (5.4) and (5.5) respectively gives

$$|V_S|^2 = \left[V_{PCC} + \frac{(R_S P_S + X_S Q_S)}{V_{PCC}}\right]^2 + \left[X_S P_S - \frac{(R_S Q_S)}{V_{PCC}}\right]^2 \qquad (5.6)$$

where, $Q_S = Q_L + Q_C$

Taking V_{PCC} as reference, Equation (5.6) can be written in terms of the line current $i_{S\,real} + ji_{S\,imag}$ (with no compensation, this equals to the load current) flowing through the line impedance $R_s + jX_s$ as expressed by (5.7) below. (Derivation in Appendix C)

$$|V_S|^2 = \left[V_{PCC} + \left(R_S i_{S\,real} - X_S i_{S\,imag}\right)\right]^2 + \left[X_S i_{S\,real} + R_S i_{S\,imag}\right]^2 \qquad (5.7)$$

Assuming R_s is negligibly small, and the current angle relative to V_{PCC} is, θ (Figure 5.2), the above becomes

$$|V_S|^2 = \left[V_{PCC} + \left(X_S i_S \sin\theta\right)\right]^2 + \left(X_S i_S \cos\theta\right)^2 \qquad (5.8)$$

By expanding squares on the right-hand-side and simplifying, equation (5.8) becomes

$$|V_S|^2 = |V_{PCC}|^2 + |2V_{PCC} X_S i_S \sin\theta| + |(X_S i_S)|^2 \qquad (5.9)$$

Then to obtain $|V_S|^2 = |V_{PCC}|^2$, we set, $|2V_{PCC} X_S i_S \sin\theta| + |(X_S i_S)|^2 = 0$

This leads to

$$\sin\theta = -\frac{X_S i_S}{2V_{PCC}}, \quad \theta = -\sin^{-1}\left(\frac{X_S i_S}{2V_{PCC}}\right), \qquad (5.10)$$

This means that to regulate the reactive power for making the magnitude of V_{PCC} equal to that of V_S, the current phasor through line impedance should lead V_{PCC} by θangle.

Alternatively, by taking V_S as the reference, the phase angle θ_S between the current and V_S phasor required to achieve $|V_S| = |V_{PCC}|$ can be derived in the same manner. In this case the following formula can be written:

$$|V_{PCC}|^2 = \left[V_S - \left(X_S i_S \sin\theta_s\right)\right]^2 + \left[X_S i_S \cos\theta_S\right]^2 \qquad (5.11)$$

This has the same form as (5.8), hence to enable $|V_S| = |V_{PCC}|$

$$\theta_S = \sin^{-1}\left(\frac{X_S i_S}{2V_S}\right) = -\theta \qquad (5.12)$$

Thus the condition to control the STATCOM for achieving $|V_S| = |V_{PCC}|$ is clear, the reactive current from the compensator, added to the original load current, must be chosen to ensure that the current through the line impedance leads V_{PCC} , but lags V_s , by an equal angles as shown in Figure 5.3. This means that both the PCC and source sides supply the same reactive power to the line.

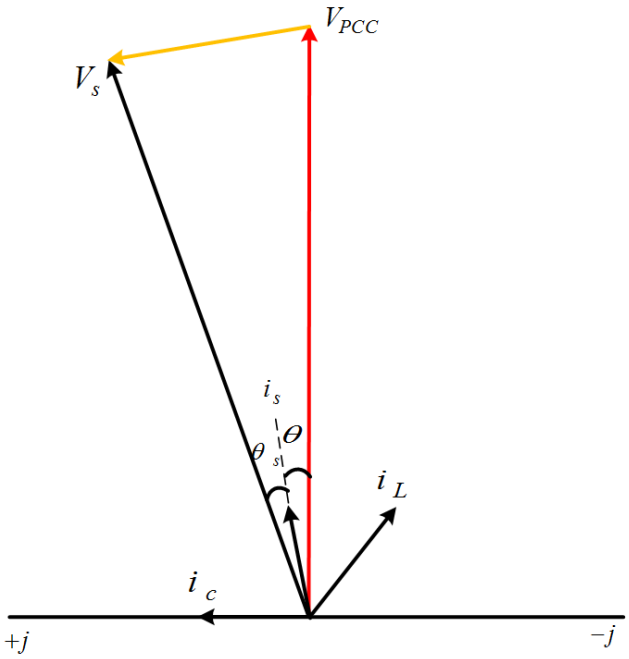


Figure 5.3: Phasor Diagram showing $|V_S| = |V_{PCC}|$ operation

5.1.2 Unity Power Factor Correction

Another case is to compensate the load reactive power Q_L for achieving unity power factor. The reactive power from the compensator Q_C must be equal in magnitude and opposite in direction to Q_L such that $Q_S = Q_L + (-Q_C) = 0$.

The new voltage drop along the distribution line parameters is shown below:

$$\Delta V = (R_S + jX_S)\frac{P_S - j0}{V_{PCC}} \tag{5.13}$$

$$\Delta V = \frac{R_S P_S}{V_{PCC}} + j\frac{X_S P_S}{V_{PCC}}$$

In this case, ΔV is now totally independent of reactive power Q_S , but only caused by the active power current flowing through the distribution line impedance. This implies that to obtain unity power factor supply using reactive power compensation, it is not possible to achieve PCC voltage

regulation of $|V_S| = |V_{PCC}|$ at the same time. Phasor diagrams showing fundamental relationships of voltage and current phasor in the system are shown in Figure 5.4

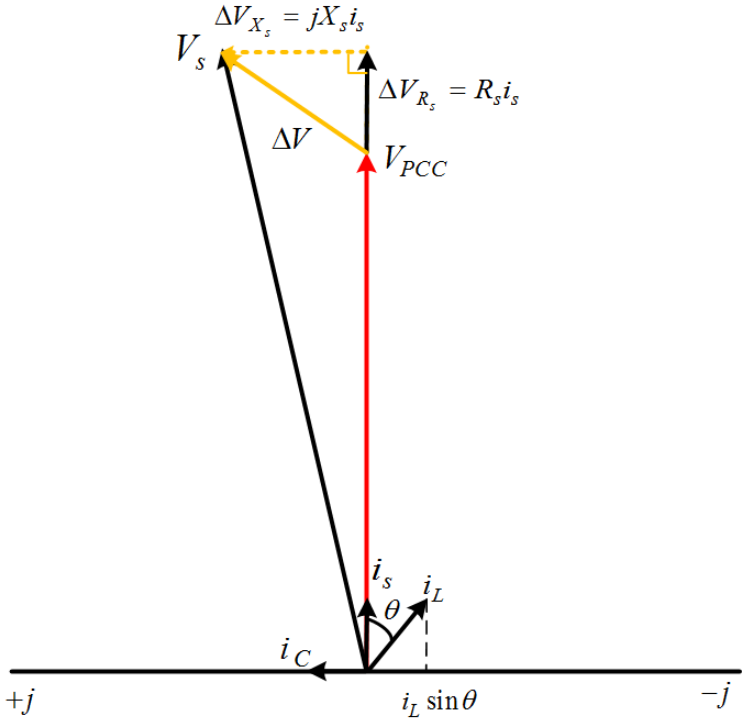


Figure 5.4: Phasor Diagram showing Unity Power Factor Operation

5.2 Power Rating of Converter

The FC-MMC STATCOM operates on a variable voltage scheme and the difference between its output AC terminal voltage and PCC line voltage determines the amount of current and hence power flowing between them. For reactive power compensation, the rating of the converter can be based on the maximum required reactive power Q_C to be generated. In general, this is to be about 20-30% of the load power [189, 190] . This then determines the converter DC-capacitor voltage V_{DC} and the maximum output voltage $(\vec{V}_C)$ as shown in Figure 5.5. The converter's current $\vec{i}_C$ is given as

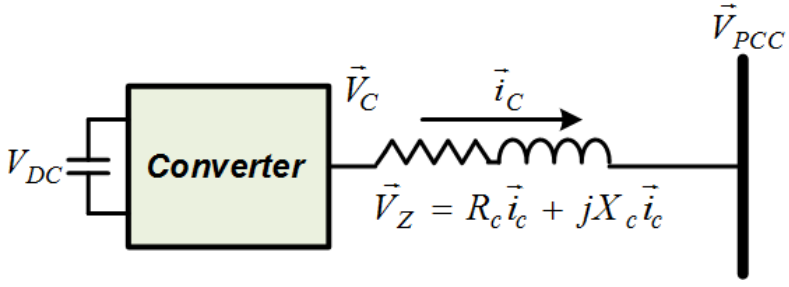


Figure 5.5: Voltage-Current relationship between Converter and PCC

$$\vec{i}_C = \frac{P_C + jQ_C}{\vec{V}_{PCC}} = \frac{\vec{V}_{PCC} - \vec{V}_C}{Z_C} \tag{5.14}$$

Figure 5.6, show the phasor diagram for the relationships between the PCC and Converter voltages. This explains the relationship between all parameters under reactive power compensation such as voltage and current vectors. The voltage vector $\vec{V}_C$ is the total voltage across all the sub modules of a MMC converter. In this case, this represents bipolar FC H-bridge sub modules switching between ±V_{DC} connected in a single star configuration. The modulation index is expressed as

$$m_a = \frac{V_{C\,pk}}{N \times V_{DC_{SM}}} = \frac{V_{C\,pk}}{V_{DC\min}} \tag{5.15}$$

where, N is the total number of sub-modules switched in and $V_{DC_{SM}}$ the DC voltage across each sub-module. All voltage vectors in Figure 5.6 are represented with respect to their peak values.

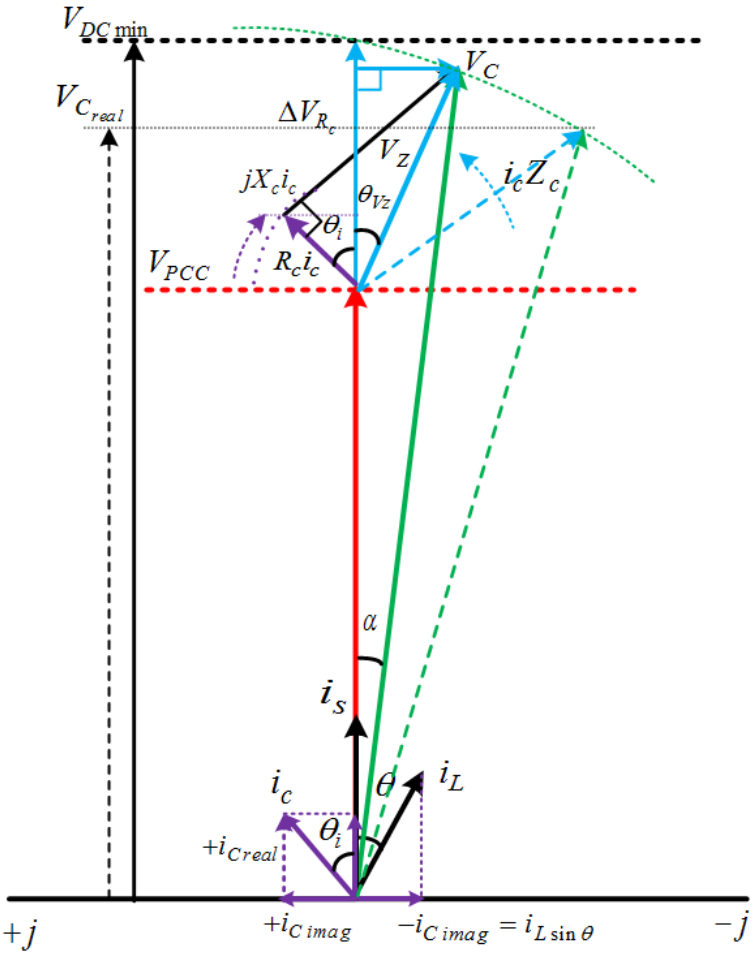


Figure 5.6: Phasor Diagram between Converter and PCC voltages & currents

Based on this diagram, the following relationships are valid for the converter's operation under reactive power compensation.

1. The power rating of the converter is determined based on either the maximum reactive power absorbed by the load if unity power factor correction is required or by the distribution line parameters for PCC voltage regulation. For the former, if the load maximum power factor angle is θ, the maximum absorbed reactive current by the load is $i_L \sin(\theta)$ as shown in Figure 5.6. For the latter it depends on the maximum allowed percentage voltage drop to the nominal voltage level of the distribution line, this will enable estimation of the maximum reactive current required from the STATCOM.
2. For unity power factor correction, the total reactive current component at the PCC equals zero $(i_{S imag} = i_{L imag} + i_{C imag} = 0)$ so the converter's maximum reactive current is the negative of that of the load $(i_{C imag} = -i_{L imag} = -i_L \sin\theta)$ and varies based on the power factor at the load side.
3. The converter's active current $i_{C real}$ is equal to that required to compensate switching and capacitor losses hence keeping the DC capacitor voltage balanced.
4. The operating region of the converter's current angle is assumed to be between $45^\circ < \theta_i < 90^\circ$ i.e. from $i_{C real} = i_{C imag}$ to $i_{C real} = 0$. Within this range it means that the converter generates higher reactive current than real current. Current angle below 45° implies that the converter absorbs more active current than the reactive current which cannot be true for a STATCOM.
5. The product of the maximum converters current phasor $i_{C\max} \angle\theta_i$ and filter impedance $R_C + jX_C$ determines the voltage difference vector $V_Z \angle\theta_{Vz}$ between V_C and V_{PCC}. Hence, the maximum operating limits of the converter.
6. Referring to Figure 5.6, rotating the converter's current angle $\angle\theta_i$ in the clockwise direction from 90° towards 45° (an increase of the converter's active current) causes an anticlockwise rotation voltage difference vector V_Z resulting to higher $V_{C real}$ (an increase of the DC capacitor voltage rating).
7. The maximum reactive compensation capacity depends on the total energy that can be stored in the DC capacitors. For each sub-module,

this is relates to the capacitance C and the voltage across the capacitors $\left(E_{SM} = \left(1/2\right) C V_{DC_{SM}}{}^2\right)$. More reactive power leads to a higher DC voltage V_{DC} and more energy requirements.

5.2.1 DC Capacitor Voltage Rating

Figure 5.7 shows two triangles, 1 and 2, formed by all voltage vectors.

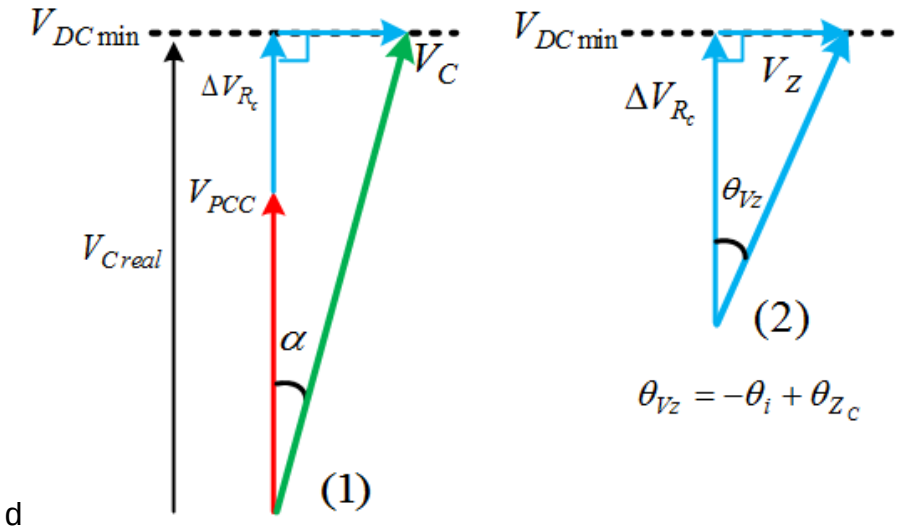


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Figure 5.7: Simplified Phasor Diagram between Converter and PCC voltages

These can lead to the derivation of an expression for DC capacitor voltage. which is based on the PCC voltage V_{PCC}, load power factor angle θ at the PCC and voltage across the filter impedance $(V_Z = i_C Z_C)$, without a prior knowledge of the converter voltage magnitude and angle $V_C \angle \alpha$. Clearly the DC Capacitor voltage is related to the reactive power supplied to the load by STATCOM and is analysed below.

The DC-Capacitor voltage V_{DC}, required to provide the reactive power compensation depends on the real part of the converter voltage phasor $V_{C\,real}$ taking the PCC voltage vector $(\vec{V}_{PCC} = V_{PCC} \angle 0^\circ)$ as the reference. Resolving triangle (1) in Figure 5.7.

$$V_{C\,real} = V_{PCC} + \Delta V_{R_c} = V_C \cos\alpha \quad \text{with}$$

$$V_C \cos\alpha \le V_{DC} \tag{5.16}$$

From the above the DC voltage V_{DC} is shown to be dependent on the converter's voltage and angle $V_C \angle \alpha$ and PCC voltage V_{PCC}. Hence, to determine the DC voltage the values of the converter's voltage and angle α need to be known.

Alternatively, resolving triangle (2) in Figure 5.7 a solution for ΔV_{R_C} in (5.16) can be found based on using the voltage phasor $\vec{V}_Z$

$$V_Z \angle \theta_{Vz} = \left| i_C Z_C \right| \angle (-\theta_i + \theta_{Z_C}) \tag{5.17}$$

$$\Delta V_{R_C} = V_Z \cos(\theta_{Vz}) \tag{5.18}$$

where, $\angle \theta_{Vz} =$ the angle between the $\vec{V}_Z$ and $\vec{V}_{PCC}$ phasor.

$\angle \theta_i =$ the angle between the current phasor and the $\vec{V}_{PCC}$ phasor

$\angle \theta_{Z_C} =$ filter impedance angle projection towards $\vec{V}_{PCC}$ phasor

Substituting equation (5.18) into (5.16), the DC voltage V_{DC} can be expressed as

$$\begin{aligned} V_{DC} &= V_{PCC} + V_Z \cos(\theta_{Vz}) \\ &= V_{PCC} + \left| i_C \times Z_C \right| \cos(-\theta_i + \theta_{Z_C}) \end{aligned} \tag{5.19}$$

where,

$$\left| i_C \right| = \sqrt{{i_{C\,real}}^2 + {i_{C\,imag}}^2}\ ,\ \theta_i = \tan^{-1}\left(\frac{i_{C\,imag}}{i_{C\,real}} \right) \tag{5.20}$$

$$\left| Z_C \right| = \sqrt{{R_C}^2 + {X_C}^2} \qquad ,\theta_{Z_C} = \tan^{-1}\left(\frac{X_c}{R_c} \right) \tag{5.21}$$

This gives an expression for the V_{DC} minimum value which is independent of the converter's voltage magnitude and angle $V_C \angle \alpha$. V_{DC} is determined by the fixed filter parameters and the maximum reactive power required from the converter which defines i_C and $\angle \theta_i$.

The magnitude of the filter impedance $\left| Z_C \right|$ can also be expressed as a factor k_f of the magnitude of load impedance $\left| Z_L \right|$.

$$\left| Z_C \right| = k_f \times \left| Z_L \right| \tag{5.22}$$

where = k_f is a percentage factor.

Assuming the maximum current rating of the converter is the same as the load side, so $(i_{C\max} = i_{L\max})$, (5.22) can be expressed as

$$|Z_C| = \left(\frac{k_f \times |V_{PCC}|}{|i_{L\max}|} \right) = \frac{|V_Z|}{|i_{C\max}|} \tag{5.23}$$

Consequently we have V_z expressed as a certain k_f times of the PCC voltage V_{PCC} ,

$$|V_Z| = k_f \times |V_{PCC}| \tag{5.24}$$

Note that k_f is normally about 20-30% of V_{PCC} [189, 190]. In addition, according to the expression (5.21) the filter parameters can be expressed in terms of k_c as

$$\theta_{Z_C} = \tan^{-1}(k_c) \tag{5.25}$$

5.2.1.1 Energy Requirements of Sub-Module Capacitors

In the case of the capacitor, the voltage ripple in each module characterises the exchange of energy within the converter. A high voltage ripple would cause a higher energy deviation requiring a larger size capacitor [191, 192]. Moreover, the low order harmonic frequency observed in the ripples of the MMC converters is a function of the equivalent series resistance and this reduces the capacitor life time [193]. This is essential in determining how to size each capacitor for STATCOM applications and researchers have studied these voltage ripple effects to find alternate solutions to help tackle this issue [194-197]. This is essential in determining how to size each capacitor for STATCOM applications. More recent research [197] show the energy relationship of the capacitor of the sub-modules to reactive power capacity of an MMC STATCOM. This is as described below..

Taking the converters voltage V_C as reference, the relationship between the PCC voltage V_{PCC} and R-L filter parameters is given as

$$v_c - v_{PCC} - R_{i_c} - L\frac{di_c}{dt} = 0 \tag{5.26}$$

where, $v_c = V_C \sin(\omega t + \alpha_v)$, $i_c = I_C \sin(\omega t + \alpha_i)$ and $v_{PCC} = V_{PCC} \sin(\omega t)$

The capacitor voltage variation V_{SM} is proportional to the current I_{SM} flowing through the DC side of each sub-module given as

$$I_{SM} + C\frac{dV_{SM}}{dt} = 0 \tag{5.27}$$

Assuming the losses are negligible and switching events neglected, The input power on the AC side is equal to the output power on the DC side

$$V_{SM} I_{SM} = v_c i_c$$

$$I_{SM} = \frac{v_c}{V_{SM}} i_c \tag{5.28}$$

Replacing I_{SM} from (5.28) in (5.27) gives

$$\frac{v_c}{V_{SM}} i_c + C \frac{dV_{SM}}{dt} = 0 \tag{5.29}$$

The expressions in (5.26) and (5.29) represent the behaviour of the sub-module capacitors of the MMC converter.

An expression of the energy in a sub-module can be derived by solving the differential in (5.29) given as

$$E_{SM} = \frac{C V_{SM}^{\,2}}{2} = E_{SM}(t_0) + \int_{t_0}^{t} v_c i_c \; dt \tag{5.30}$$

where, $E_{SM}(t_0)$ represents the energy stored at the sub-module capacitor at time $t = t_0$.

Assuming the voltage and current are without harmonics and replacing $v_c = V_C \sin(\omega t + \alpha_v)$ and $i_c = V_C \sin(\omega t + \alpha_i)$ in (5.30),

$$E_{SM} = E_{SM}(t_0) + \int_{t_0}^{t} V_C I_C \sin(\omega t + \alpha_v) \sin(\omega t + \alpha_i) \, dt$$

Solving the equation, and with trigonometric identities a simplified expression for the energy of a sub-module is given as

$$E_{SM} = E_{SM}(t_0) + \frac{1}{2} \int_{t_0}^{t} V_C I_C (\cos(\alpha_v - \alpha_i) - \cos(2\omega t + \alpha_v + \alpha_i)) \, dt$$

$$E_{SM} = E_{SM}(t_0) + \frac{1}{2} V_C I_C (\sin(\alpha_v - \alpha_i) - \frac{1}{4} \sin(2\omega t + \alpha_v + \alpha_i)) \tag{5.31}$$

The expression in (5.31) show the relationship of energy in capacitor to the reactive power . The angle sum and differences between the converter voltage α_v and current α_i is function of the reactive power flowing through the converter. Also noticed is the contribution of the second order harmonic seen on the sub-module capacitor voltage of MMC converters.

5.2.1.2 Converter Filter Design Consideration

The choice of filter topology and associated parameters depends on the lowest order harmonic generated by the converter to be eliminated. Passive low pass filter configurations such as LCL filter and simple R-L filter could be used at the converter side. The latter may be a transformer internal impedance. The design criteria are often set by having a cut-off frequency sufficiently close to the grid fundamental frequency, with low power losses and small size. An R-L filter is chosen in this study and the cut-off frequency can be expressed as

$$f_{cut} = \frac{R_C}{2\pi L_C} \tag{5.32}$$

Assuming the fundamental frequency is f_o , we have

$$\left(\frac{f_o}{f_{cut}}\right) = \left(f_o \times \frac{2\pi L_C}{R_C}\right) = \frac{X_C}{R_C} = k_c = \tan\theta_{Z_C} \tag{5.33}$$

From (5.33) it can be seen that the cut-off frequency depends mainly on k_c . Setting the range of filter cut-off frequency between 100Hz – 1kHz results in k_c varying between 0.5 →0.05 respectively. Higher $k_c < 1$ implies the increased resistance compared to reactance, leading to lower cut-off frequencies, but using larger filter inductors.

In an FC-MMC type converter, a favourable feature is that the required filter reactance X_C or filter size reduces with the increased number of voltage levels. This component limits the reactive power capability but also helps in the reduction of harmonic components. Thus the improved nature of the converter voltage makes it possible for lower sized filter parameters to be used at the same k_c ratio further reducing the resistive power losses. The following subsection details a case study variations of DC bus voltage and shows how the choice of coupling reactance affects this.

5.2.2 Case Study: Variations of DC-Bus Voltage Rating

The variation of filter parameters discussed above may change the DC-bus voltage rating and limit the reactive power capability. This can be analysed according to equations (5.19)-(5.25) for determining the minimum DC

capacitor voltage required for the converter and the magnitude of the filter impedance $|Z_C|$.

Substituting the equations (5.32)-(5.33) and solving for the DC voltage V_{DC} the minimum required DC voltage under the valid operating range of $\angle\theta_i$ can be derived.

A MATLAB program (Appendix C.3) has been used to evaluate the DC-capacitor voltage changes according to the changes of converter current phase angle and filter parameter k_c. This show the possible reactive power range under operation.

Figure 5.7 and Figure 5.8 shows the results which represents the minimum required DC voltage under the operating range of $\angle\theta_i$ from 45° to 90° (100% to 0% compensation) at different filter ratios k_c which corresponds to cut-off frequencies between 100 Hz – 1 kHz. The reactive current, $i_{C\,imag}$ supplied by the converter is set to enable the load side maximum power factor $\cos\theta = 0.87$. The figures show the limits of the DC voltage under full reactive power compensation range.

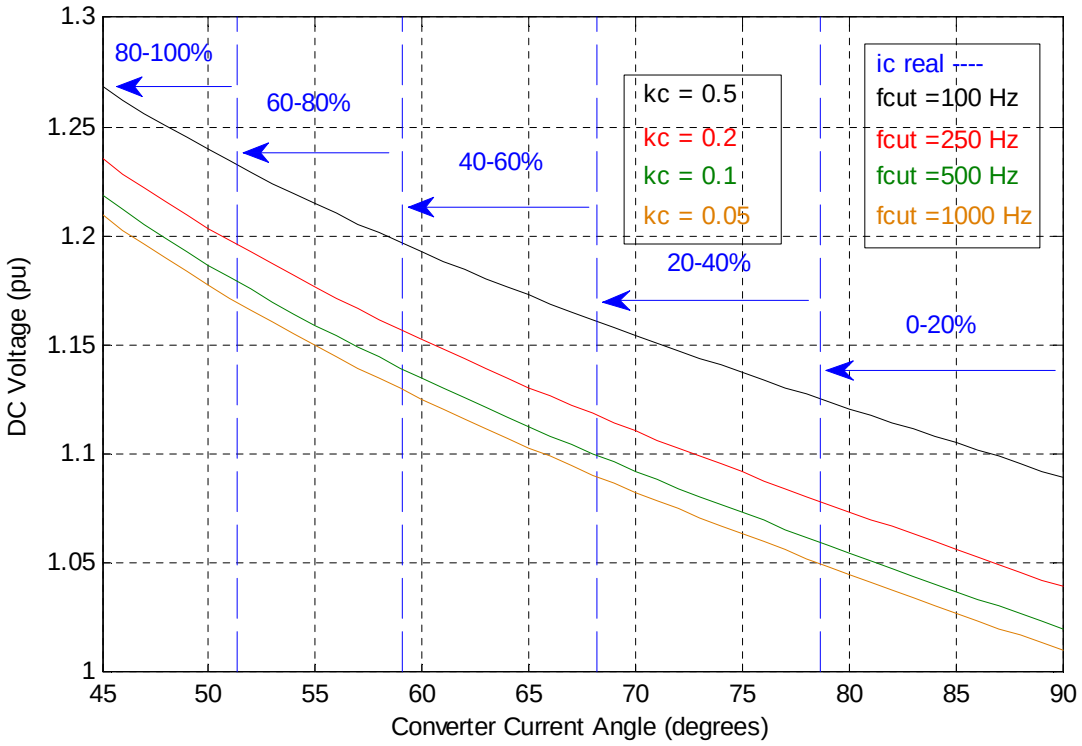


Figure 5.8: Changes in Converter Current phase Angle Vs Required DC Voltage when k_f = 0.4 for fc between 100Hz to 1kHz.

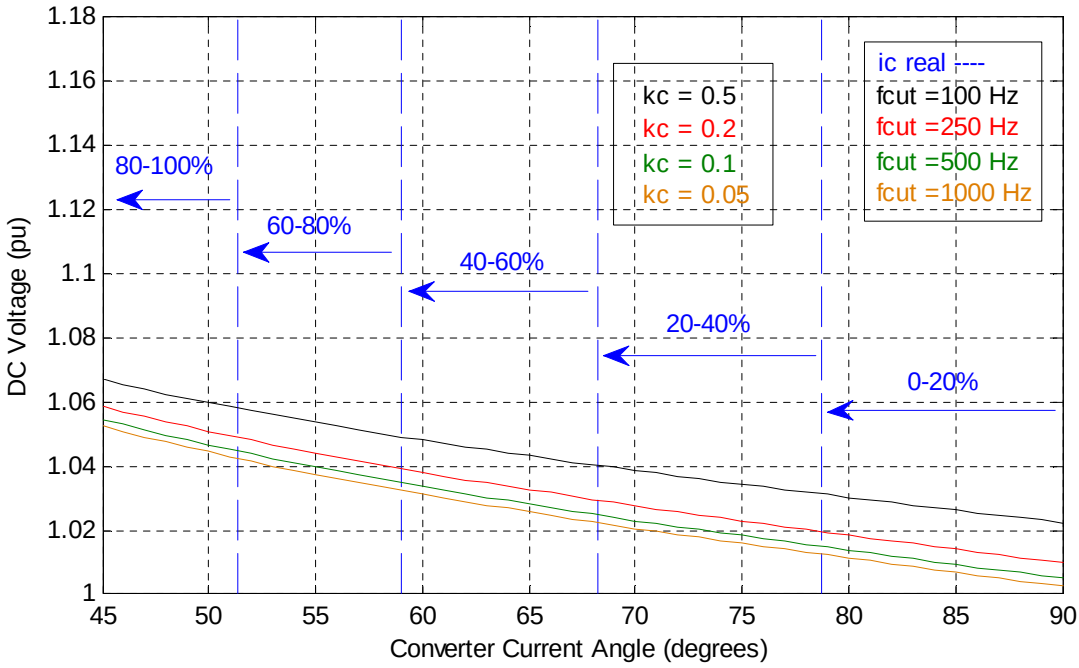


Figure 5.9: Changes in Converter's Current Angle Vs Required DC Voltage when k_f = 0.1 for fc 100Hz – 1kHz.

Figure 5.8 illustrates the scenario when the k_f factor is set to 0.4 corresponding to the filter impedance being 40% of the load impedance. The minimum DC voltage V_{DC} required at full operation mode (100%) is shown to be 27% higher than the PCC voltage V_{PCC}, corresponding to the STATCOM real current being equal to reactive compensating current $i_{Creal} = i_{Cimag}$. Assuming a typical STATCOM requires low i_{Creal} to compensate for the power losses, the region of current angle lies within the 0-20% as shown in the figure, then the required minimum DC voltage would be 13% higher than the PCC voltage.

Figure 5.9 shows similar conditions for a lower k_f factor of 0.1 (filter impedance being 10% of that of load impedance). This illustrates a possible scenario for an FC-MMC converter which has a higher number of discrete voltage levels hence giving a lower filter impedance and size. In such a case, the converter can still work within its full reactive power range and the additional DC bus voltage could be as low as 3% and 7% of the PCC voltage for the current angle in the ranges of 0-20% and up to 100% respectively. Hence, the lower sized filters allows for a lower rated converter with full reactive compensation capacity.

In summary, the above analysis shows for MMC converters the choice of filters relates power rating of the converter under reactive compensation. The DC-capacitor voltage increases with the increase of filter impedance X/R ratio k_c , hence the decrease of the filter cut off frequency. On the other hand the required DC-capacitor voltage rises with the increase of real current drawn by the converter for power loss compensation.

5.3 Simulation Studies of an FC-MMC STATCOM

Having analysed the power flow relationships of a simple power system with a converter-based STATCOM for reactive compensation, this section studies the application of an FC-MMC STATCOM for PCC voltage regulation and power factor control through simulation.

5.3.1 Power System Configuration

Figure 5.10 shows the configuration of the simulated power network, with power rating of 3.3 kVA and phase voltage rating of 110 V, for reactive power compensation using an FC-MMC STATCOM. At the converter side, each phase has two series connected sub-modules, each of which is a 5-level Flying-capacitor full- bridge converter; hence there are in total four flying capacitors and two DC bus capacitors per phase, giving in total 9 voltage levels. The converter is connected to the PCC via an inductive filter, with some losses represented as resistance R. The load side is modelled to imitate a feeder bus consisting of three inductive loads whose combined reactive power corresponds to a power factor of 0.87. Load 1 consumes 50% of the total reactive power whilst Load 2 and Load 3 share the remainder 50% equally.

Using the DC voltage relationship curve in the Figure 5.8, the converter filter parameters are set to achieve a cut off frequency of 160Hz. k_f factor is at 0.4 giving filter parameters of 10 Ω, 10mH and the minimum DC voltage V_{DC} is set at 27% of V_{PCC} (at 100% mode). This corresponds to a converter phase voltage of 140V split equally across the two sub-modules at each phase.

Table 5.1 below summarises parameters in this power system.

Table 5.1: Power System Parameters FC-MMC

Rating	Value
PCC Side	3.3 kVA (110V, 10A)
Distribution Line	Aluminium PI TX line (d= 10mm, s= 1m) L = 1.8mH/km PCC Voltage Regulation L =2mH, R = 0.5 Ω, X= 1.57 Ω Unity Power Factor Correction L = 8mH, R =0.2 Ω, X = 2.51Ω
Load Side	1.65 kVA (110V, 5A) Load: 22 Ω, 42mH Power factor = 0.86 lagging
Converter Side	3 kVA (200V, 5A) Filter: 10 Ω, 10mH, X/R = 0.31, f_{cut} = 160Hz. DC Capacitor rating (per sub-module): 70V, 1.12mF Module Flying Capacitor: 35V, 0.56mH
Switching frequency	750 Hz

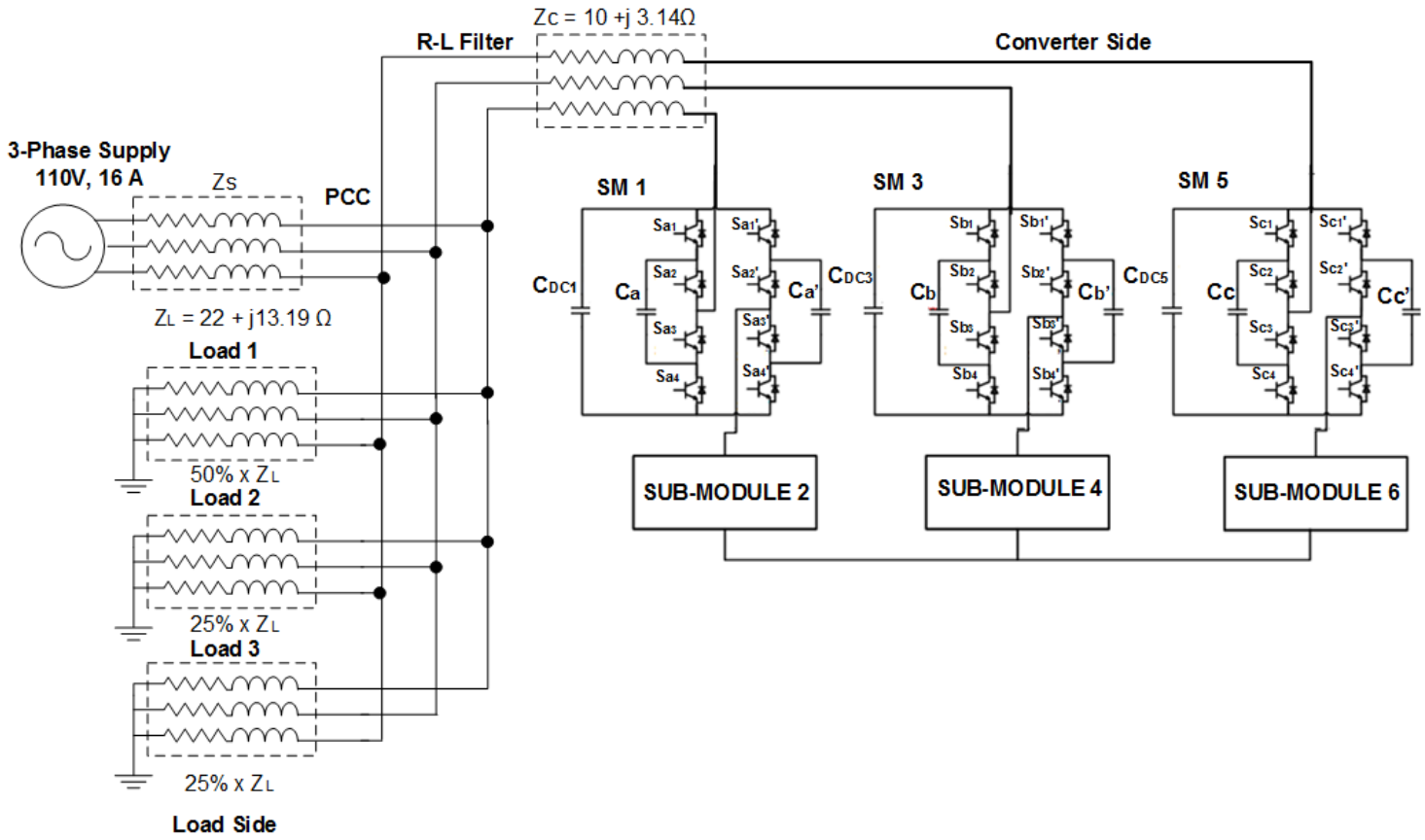


Figure 5.10: Simulation Power System Configuration

5.3.2 Control System Implementation

To achieve PCC voltage regulation and power factor correction, the STATCOM control scheme must provide the following functions.

- Sub-Module DC voltage balancing control,
- PCC voltage control, and
- Converter AC Current Control

Crucial requirement for the control scheme to perform the above functions properly is that it must remain synchronized with the PCC voltage under all system operating conditions. Thus the simulated controller comprises of the following parts:

- A voltage synchronisation technique for synchronizing the converter voltages (i.e. voltages at the terminals AC, BC, CC) to that of the PCC.
- Measurement systems for accurate acquisition of the voltages and currents as well as converting such values to their equivalents in the d-q synchronous reference frame as required.

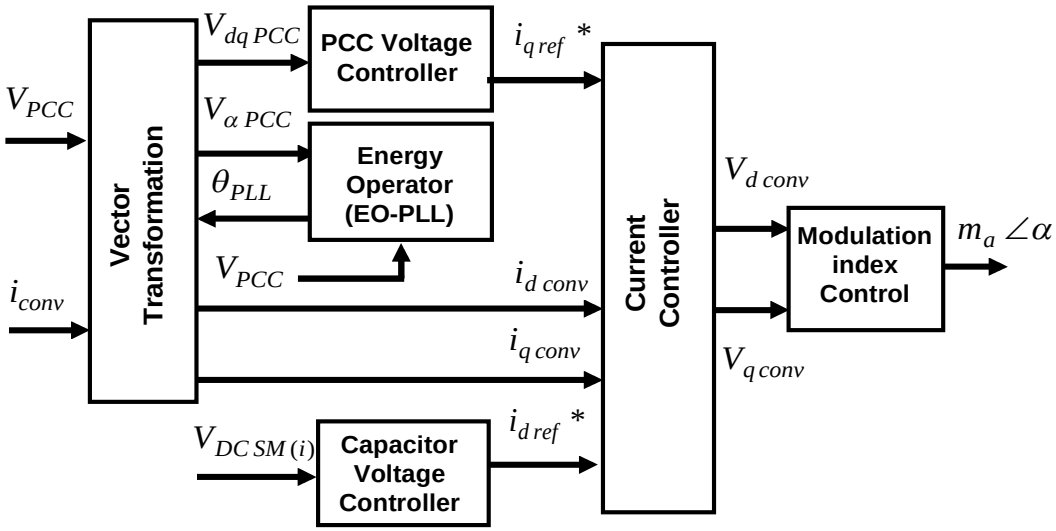


Figure 5.11: Block Diagram of Control Scheme

Figure 5.11 shows the block diagram of the whole control system comprising three controllers performing respectively the three functions described above. On the left hand side it gives all measured voltage and current signals, including voltages at PCC, converter and capacitor DC voltages.

Then the AC signals are transformed to their corresponding α-β and d-q representations taking the PCC voltage as the reference vector. Grid voltage synchronisation is achieved using the Energy Operator Phase Locked Loop scheme proposed in Chapter 4 with a sampling rate of 20kHz. Maintaining DC voltage balance is through using a feedback DC voltage controller as shown in the lower part of the diagram and described in sub-section 5.3.3. The output of this controller defines the required d-axis current for STATCOM and is supplied as the reference current value to the current controller. The required q-axis current value for STATCOM control should be evaluated according to whether it is for PCC voltage regulation or system power factor correction. For the former, the magnitude of the PCC voltage is measured and a feedback controller is used to determine $i_{qref}{}^{*}$. For the latter, $i_{qref}{}^{*}$ is evaluated by measuring the reactive current consumed by the inductive loads, and set to the inverse of the measured value in the case of unity power factor correction. Using the calculated reference d-q current values and taking the measured STATCOM AC terminal current as feedback signals, a current controller shown on the right-hand-side of the diagram is applied to determine the STATCOM ac terminal voltage vector $V_{d\,conv}, V_{q\,conv}$. This converter current controller is described below in sub-section 5.3.5.

5.3.3 Sub-Module DC Voltage Control

As shown in Figure 5.11 there are 6 sub-modules in the simulated three-phase FC-MMC. Their DC voltages should ideally be maintained at the required levels by the respective outer capacitors. However due to converter switching losses and switching pattern variations the module voltages fluctuate and may move away from their desired levels. DC-bus voltage controllers are, therefore, required to ensure that voltage across each phase limb to be at the specified value. The block diagram of a DC bus voltage controller is as shown in Figure 5.12. The scheme assumes that the three-phase voltages at PCC-bus are balanced and STATCOM delivers balanced compensation currents. Hence the controller takes the average value of the three-phase limb voltages, $V_{DC\,(avg)}$ as the controlled signal, and in this case it is calculated as

$$V_{DC(avg)} = \frac{\sum_{i=1}^{6} V_{DC\,SM}\,(i)}{3} \tag{5.34}$$

where, i = number of modules and in this study i = 6, $V_{DC}\ SM\ (i)$ represents DC-voltage across each individual sub-module.

The reference DC voltage $V_{DC\,ref}{}^{*}$ is compared with V_{DCavg} and the error is passed onto the P+I regulator in order to generate the d-component of the converters reference current. It is assumed that the inner flying capacitors of the sub-modules can achieve natural balance using PS-PWM modulation scheme as described in Chapter 3, hence do not require any feedback control.

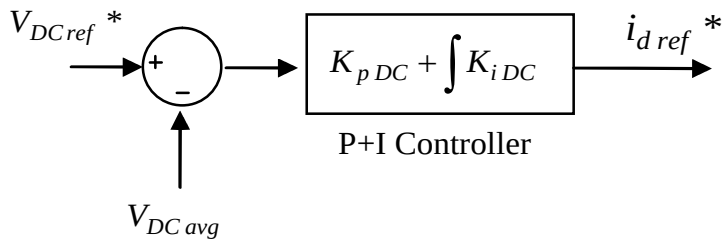


Figure 5.12: Capacitor DC Voltage Controller

5.3.4 PCC Voltage Control

The PCC Voltage regulation loop aims to maintain the magnitude of the PCC voltage at the required level given as $V_{PCC\,ref}{}^{*}$. This is achieved by evaluating the adequate reactive current supplied by the STATCOM to the PCC. A simple P+I controller is used to determine the required reactive current $i_{q\,ref}{}^{*}$ based on the voltage difference between the PCC voltage and the required level $V_{PCC\,ref}{}^{*}$. V_{mag} represents the measured voltage magnitude at the PCC calculated as shown in (5.35).

$$V_{mag} = \sqrt{V_{d\,pcc}{}^{2} + V_{q\,pcc}{}^{2}} \tag{5.35}$$

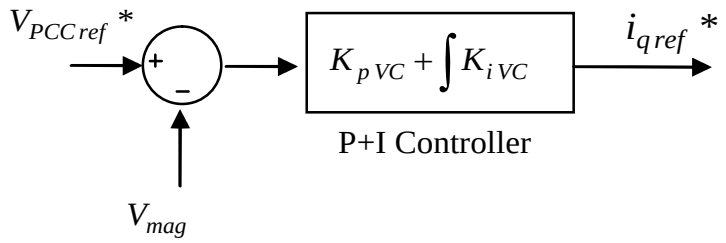


Figure 5.13: PCC Voltage Controller

5.3.5 Current Controller

The current controller adjusts the converter AC terminal voltage by regulating the reactive current flow between the converter and PCC. Using two feedback P+I controllers, the measured converter current d and q components $i_{d\,conv}, i_{q\,conv}$ follow their respective references $i_{dref}{}^{*}, i_{qref}{}^{*}$ set by Sub-module DC voltage and PCC voltage controllers. The output control signals generate the d-q voltage elements that adjust the PWM scheme modulation index to give the required converters voltage magnitude and phase angle.

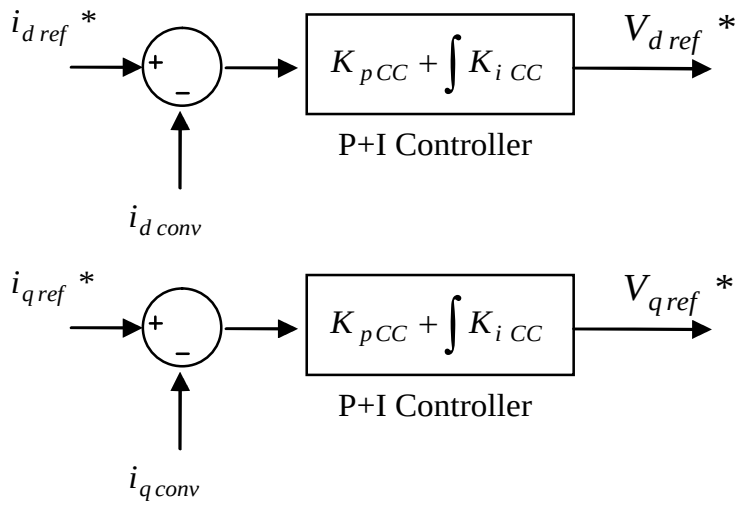


Figure 5.14: Current Controller

5.4 Simulation Results and Discussions

The system shown in Figure 5.10 has been set for reactive power compensation at the PCC bus point of a three-phase distribution network The focus is to compensate for the reactive power at the PCC. Two different cases are studied; One is to mitigate the voltage drop at PCC generated when there is a large load increase. The other is to compensate for the reactive power consumed by the load side hence improve the system power factor. Matlab Simulink software is used to simulate both cases.

5.4.1 Regulation of PCC Voltage

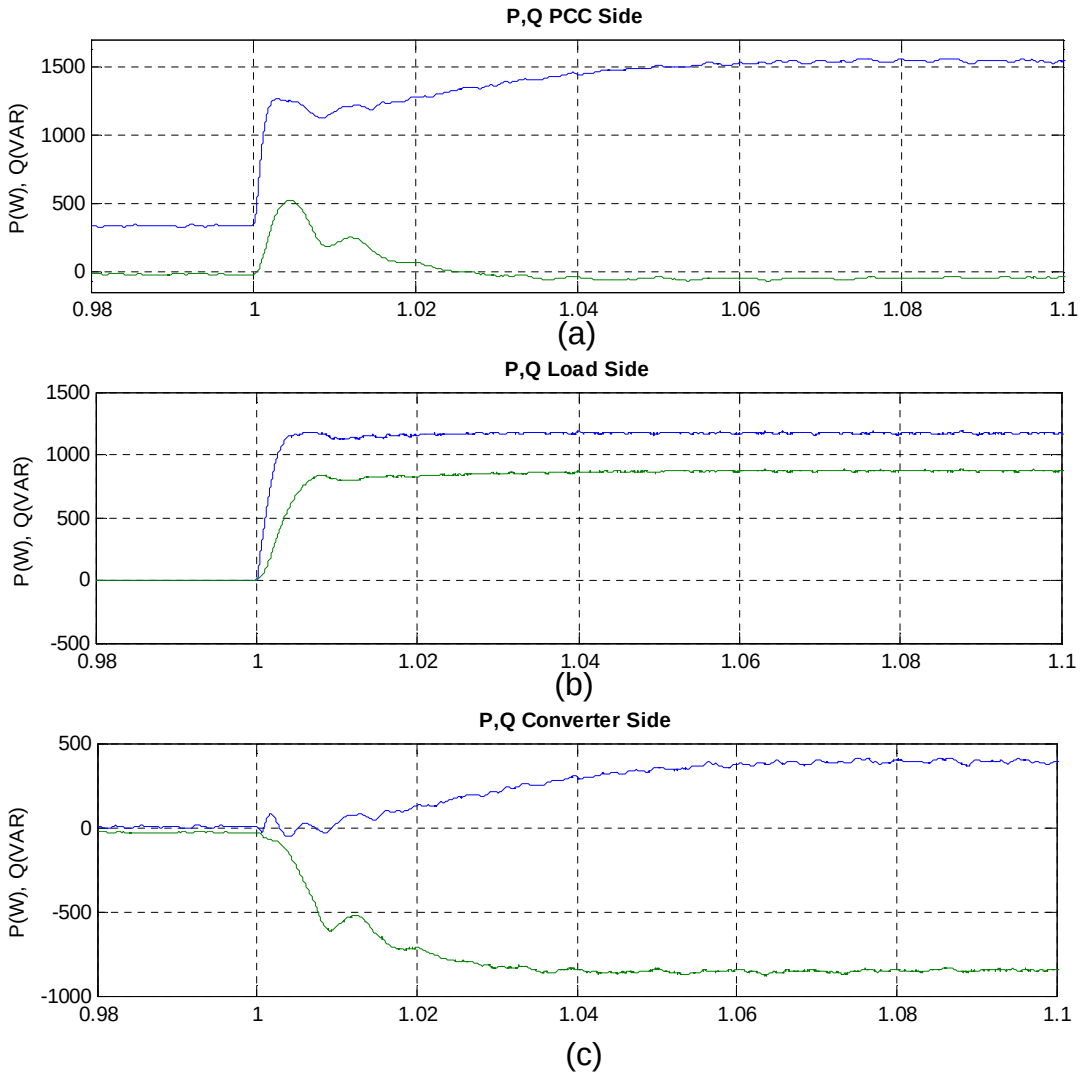
This study requires introducing a significant voltage drop, at the supply side when a large load increase occurs. The distribution line impedance is set at 2.51 Ω (0.2Ω, 8mH). The X:R ratio is greater than 1 implying the line inductance contributes more to voltage drop. The simulation parameters are listed in Table 5.1 and the total simulation time is 2s.

The converter compensates current throughout the whole simulation period. A resistive load consuming minimal power (330W) is used initially to keep the converter running at the start (0s < t < 1s) before the actual inductive load is switched in at t = 1s. The proportional and integral gains of the P+I controller for current controller, PCC voltage controller and Capacitor voltage controller are set using trial and error approach based on characteristic step response of second-order systems to K_{pCC}= 0.09 K_{iCC} = 500, K_{pVC} = 0.1 K_{iVC} = 400 and K_{pDC} = 15 K_{iDC} = 200 respectively. The sample times for three controlled are set at 20kHz and the converter switching frequency set at 750Hz.

5.4.1.1 Responses of Active and Reactive Power

Figures 5.15 (a)-(c) show the active and reactive power at the PCC, Load and Converter sides respectively.

From time t = 1s when the inductive loads are switched in, the total active and reactive powers drawn by the load rise respectively to 1200W and 850VAR with a transient delay of about 3ms. In response to the PCC voltage drop due to the load increment the converter generated reactive power to compensate the voltage drop is shown to be -880 VAR. This is greater than the reactive power drawn by the load +850 VAR and as a result a minimal reactive power of -30 VAR is absorbed at the PCC. A total active power of 1470 W is drawn at the PCC from the Grid which is the a sum of the active power consumed by the load and STATCOM. Note the controller transient response time is about 30ms and no power overshoot, which is the preferred performance.



Blue – Active Power, Green – Reactive Power

Figure 5.15: Active and Reactive Power Responses, (a) PCC Side, (b) Load Side, (c) Converter Side

5.4.1.2 PCC Side Voltage and Current Responses

Figures 5.16 (a)-(c) show the responses of the three-phase voltage and current waveforms, magnitudes of voltage and current, and power factor angle during the period of converter control.

From the start 0s < t < 1s, PCC voltage is at 1 pu, the converters current is at 0.2 pu and the power factor angle at 4^{o} .From t = 1s, the load is switched on causing a voltage magnitude drop as shown in Figure 5.16 (b) to 0.7 pu, Due to effective control it rises quickly to the required nominal level at 1pu within a transient delay of nearly 10ms .The PCC current increases to a

transient peak of about 0.7 pu but slowly settles down to 0.82 pu (4.1 A) within 60ms. The grid power factor angle also varies due to the load increase and drops down to -22^o as the load is inductive. It then rises to 2^o due to STATCOM compensation of reactive power. Clearly both PCC voltage and power factor responses satisfy the control requirement. The converter terminal voltages (before filter) are shown in Figure 5.17

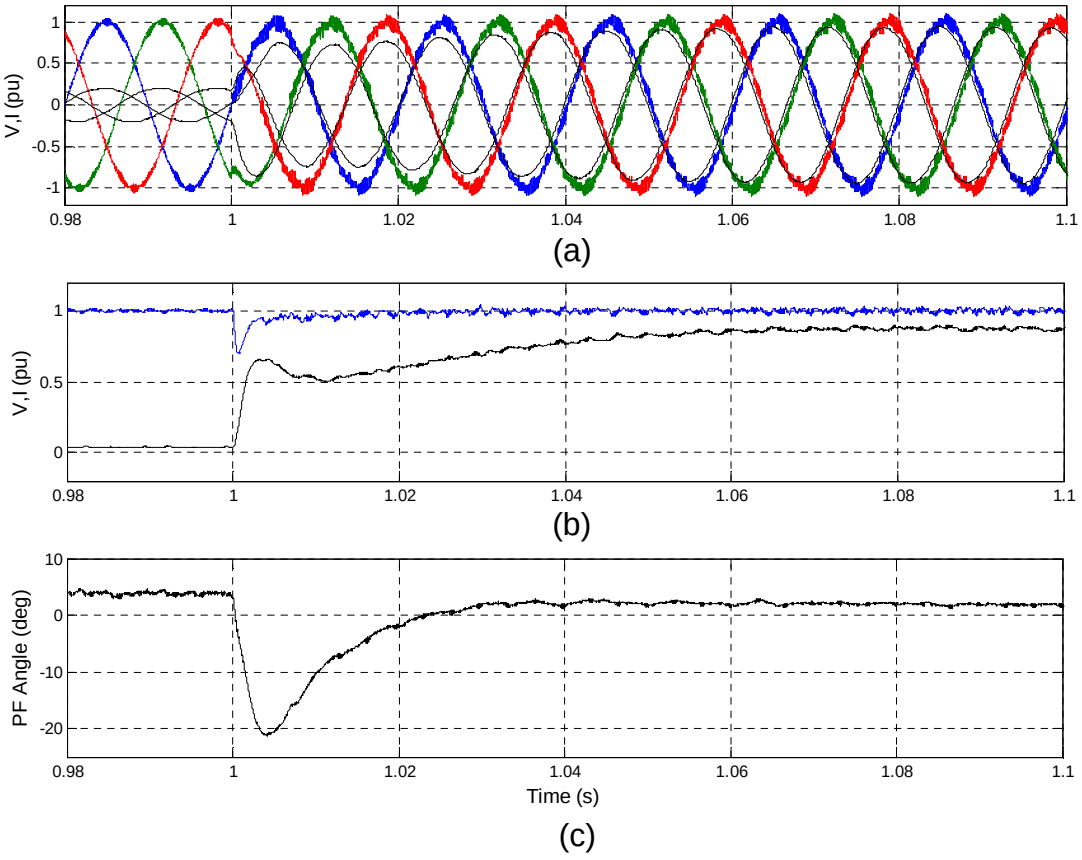


Figure 5.16: (a) Three Phase Voltage and Current, (b) Voltage Magnitude and Current Magnitude, (c) Power Factor Angle

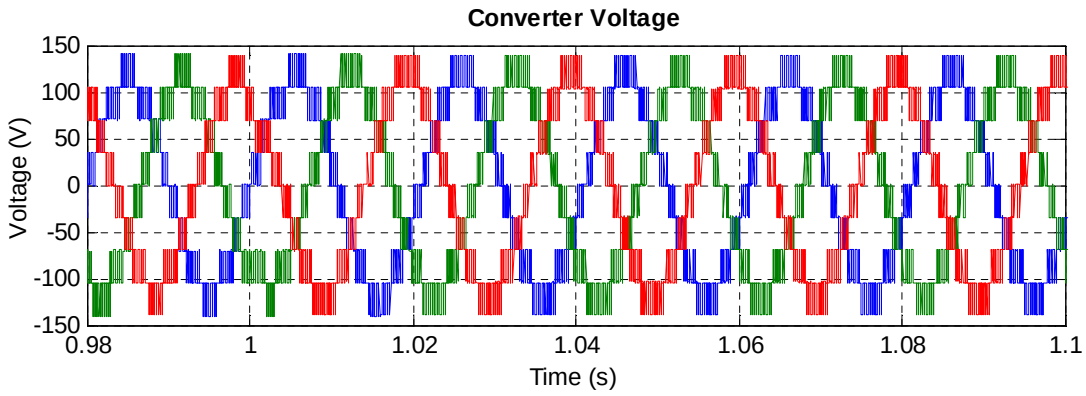


Figure 5.17: Converters Terminal Voltages

5.4.1.3 Converter DC Capacitor Voltage

Figures 5.18 (a)-(f) show the variations of the converter sub-module outer capacitor voltage waveforms. Clearly all the sub-module capacitor voltages are well balanced.

The capacitor voltage peak to peak ripple percentages increase with increased current flowing through the converter and the maximum is ±0.42%. This is well within the desired ±10% maximum requirement.

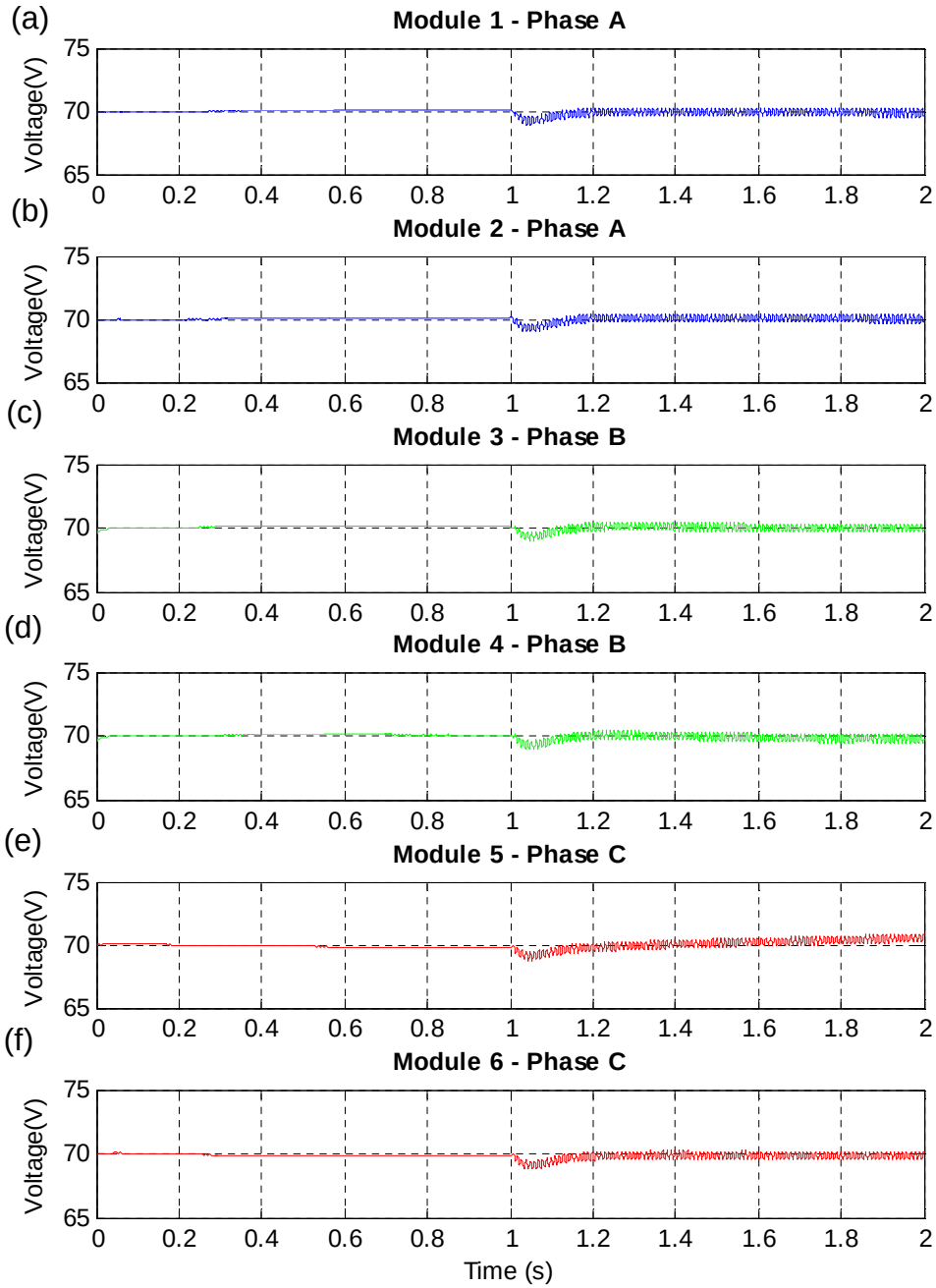


Figure 5.18: Outer Capacitor Waveforms

Figures 5.19 (a)-(c) show the inner capacitor voltage waveforms which are all balanced properly varying around 35 V, corresponds to half of the outer capacitor DC voltage of 70 V. As discussed earlier in Chapter 3 certain phases tend to deviate slightly away from the expected nominal voltage of 35V due to the open loop nature of PSPMW modulation control. However as can be seen from Figure 5.19, the variations are all within the required range, hence do not affect the performance of compensation.

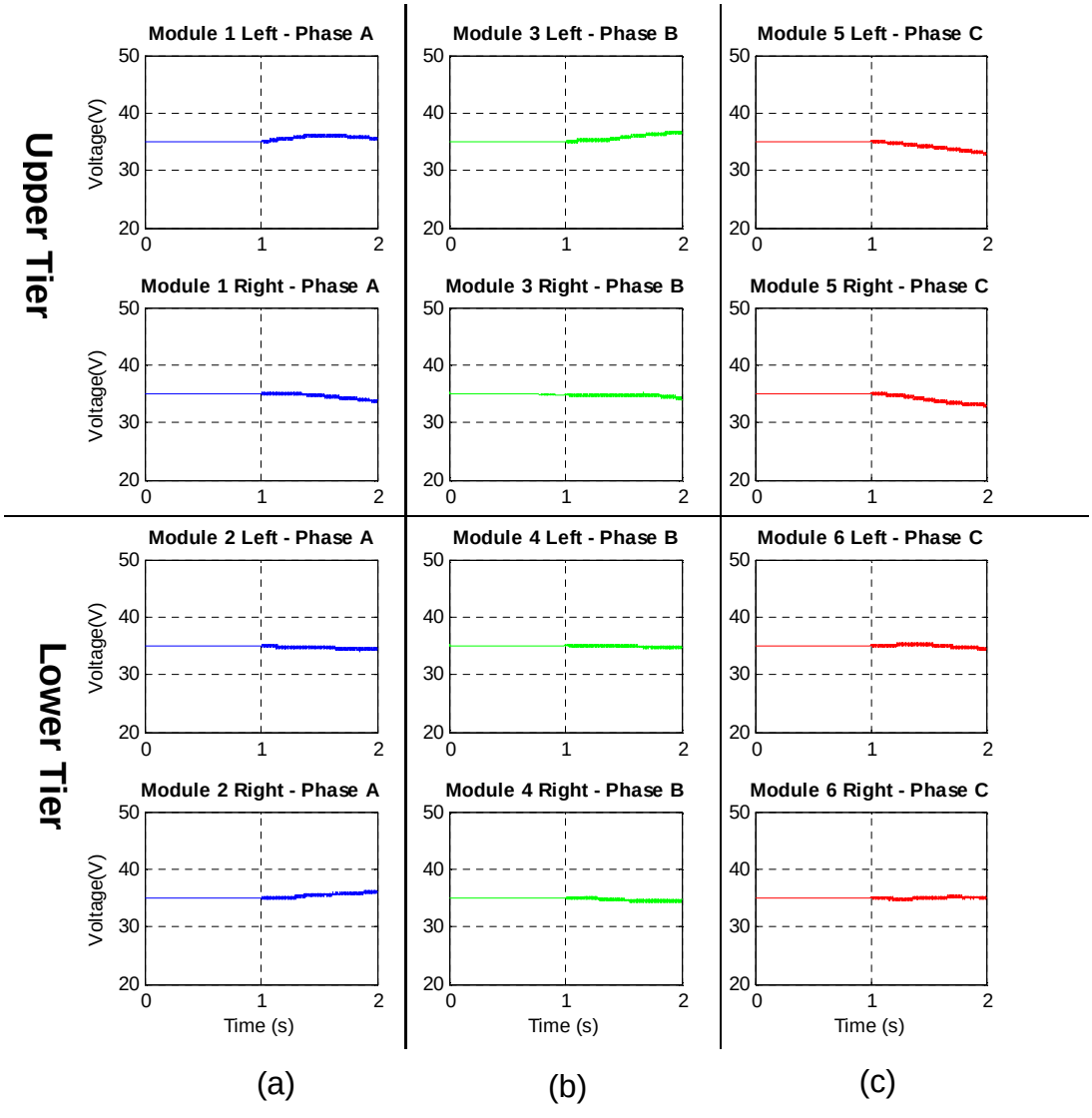


Figure 5.19: Inner Capacitor Waveforms

5.4.2 Power Factor Correction Control

The above system shown in Figure 5.10 has also been set for reactive power compensation at the PCC for improved power factor operation.

At the start of the operation (0s < t < 1s), the converter pre-charges its outer capacitors of the sub-modules so that their voltages are at the required levels using the capacitor voltage controller.

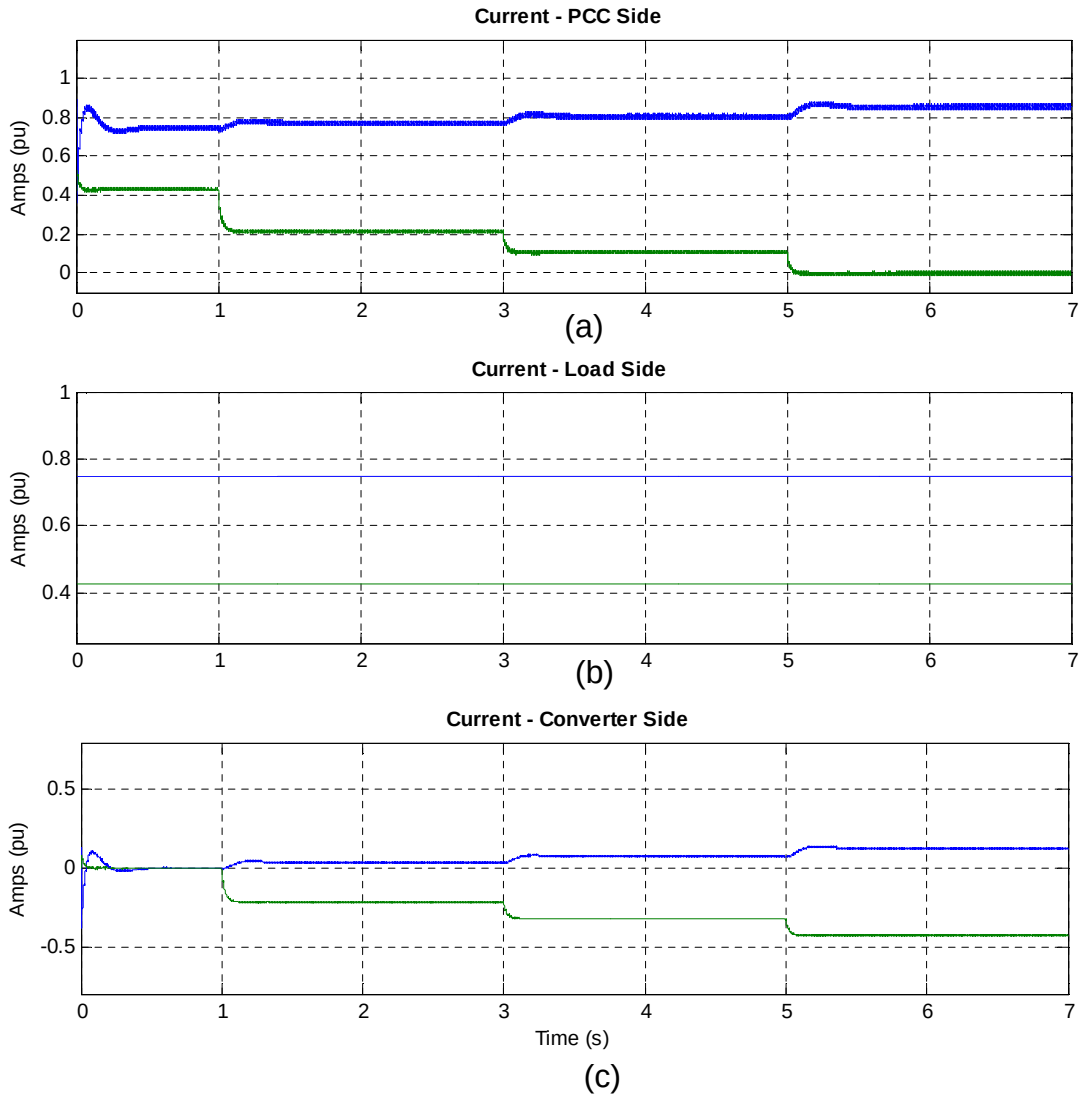
Initially at the start all three loads are connected to the PCC and the converter's controller selectively compensates the load consumed reactive power at each load bus point load at different time intervals. Load 1 (50%) at 1s ≤ t< 3s, then Load 1,2 (75%) at 3s ≤ t < 5s and finally Load 1,2,3 (100%) at 5s ≤t< 7s.

The simulation parameters are set to the same as that listed in the Table 5.1. Proportional and integral gains for the current controllers and Capacitor voltage controller are set to K_{pCC} = 0.09 K_{iCC} = 20 and K_{pDC} = 7 K_{iDC} = 50 respectively. The converter switching frequency is set at 750Hz.

5.4.2.1 Active and Reactive Current Responses

Figures 5.20 (a)-(c) show the responses of active and reactive current at the PCC, Load and Converter sides.

It can be seen that for each load increment the corresponding reactive corresponding current at PCC reduces steadily as expected from 2.2A (0.44 pu) to 1.1A (0.22 pu) and 0.55A (0.11pu), then to 0A. On the load side the reactive current is maintained constant. Meanwhile the converter side reactive current magnitude increases from 0A to 0.55A (0.11pu) and 1.1A (0.22 pu), then to 2.2A (0.44 pu). The i_{dconv} active current vector is shown to increase slightly due to the active power required to keep the capacitors balanced and the current consumed by the 10 Ω filter resistance. Consequently, an increase in the $i_{d\ pcc}$ current is observed from the initial 3.75A (0.75 pu) to 3.85 A (0.77 pu), 4.05 A (0.81) pu and 4.25 A (0.85 pu) at 50%, 75% and 100% compensation respectively. Steady state response is achieved within 80ms at each load increment.



Blue – Active Current Compenent, Green – Reactive Current Component

Figure 5.20: d-q current responses under STATCOM Control (a) PCC Side, (b) Load Side, (c) Converter Side

5.4.2.2 PCC Side Voltage and Current Responses

Figures 5.21 (a)-(d) show the supply side three-phase voltage and current waveforms, current magnitudes and power factor angle for at different loading levels

The PCC current magnitude is shown to increase at the start when t = 0s, depicting the active current required to charge the converters capacitors. Within the first 200ms of each loading condition, the PCC side currents per unit magnitude and power factor angle are shown to settle to steady states. Their values are be $0.87\angle 30^{\circ}$, $0.8\angle 15^{\circ}$, $0.83\angle 7.5^{\circ}$, $0.85\angle 0^{\circ}$ corresponding to actual current values of $4.35A\angle 30^{\circ}$, $4A\angle 15.37^{\circ}$, $4.15A\angle 7.46^{\circ}$, $4.25A\angle 0^{\circ}$

for the 0%, 50%, 75% and full compensation mode respectively. Hence, the reactive power is gradually reduced down to zero as expected.

The converter terminal voltages at 100% mode (before filter) is shown in Figure 5.22

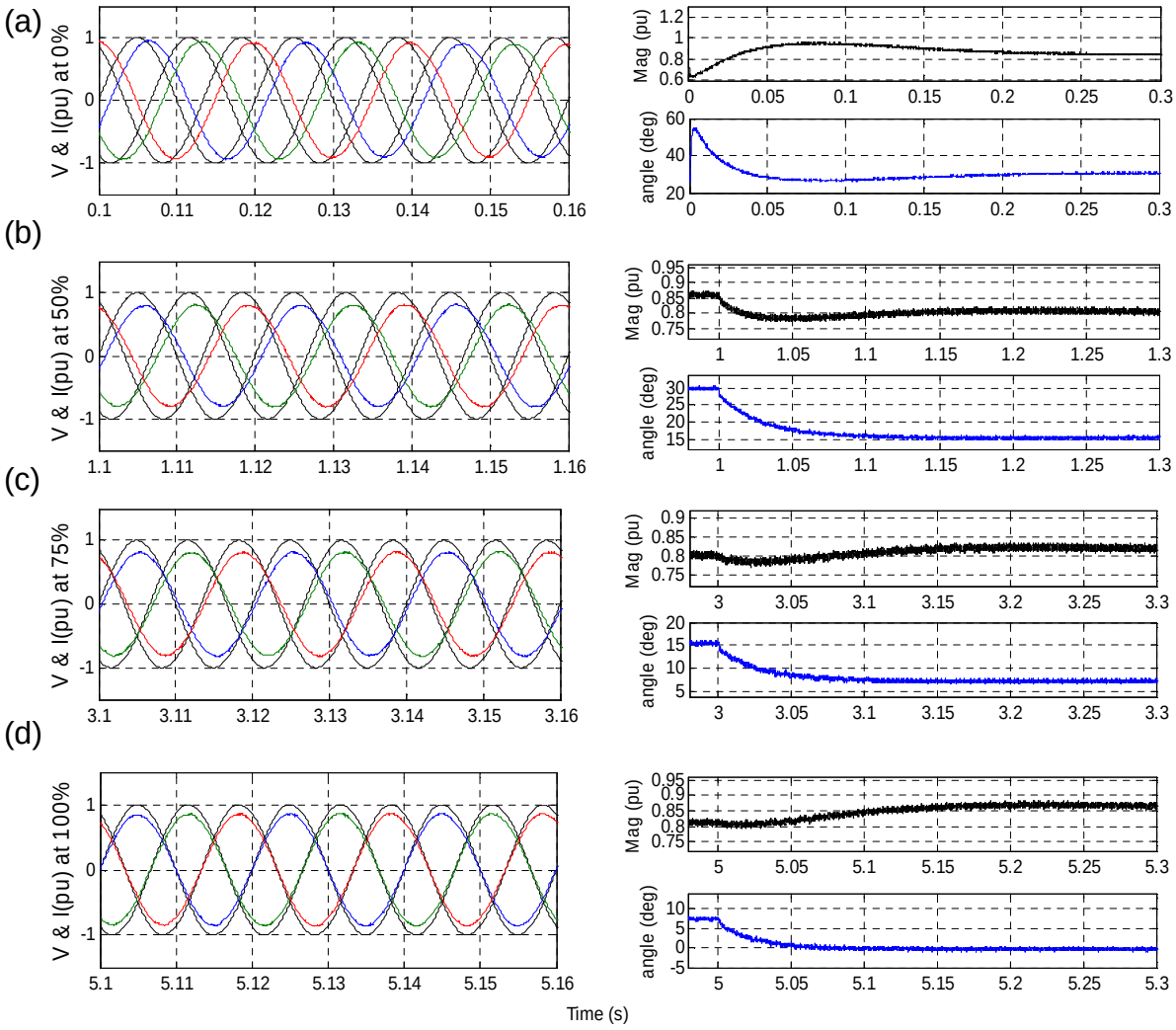


Figure 5.21: Voltage, Current and Power Factor Angle, (a) no compensation, (b) 50% compensation, (c) 75% compensation, (d) 100% compensation

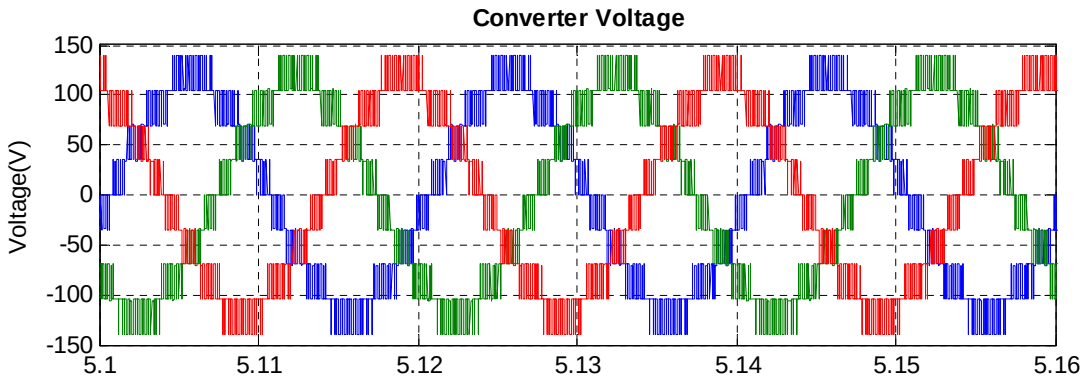


Figure 5.22: Converters Terminal Voltages

5.4.2.3 Converter DC Capacitor Voltage

Figures 5.23 (a)-(f) show variations of the outer capacitor voltage waveforms which show they are balanced properly.

The capacitor voltage peak to peak ripple increases with current flowing through the converter is ±0.4%. This is well within the desired ±10% maximum requirement.

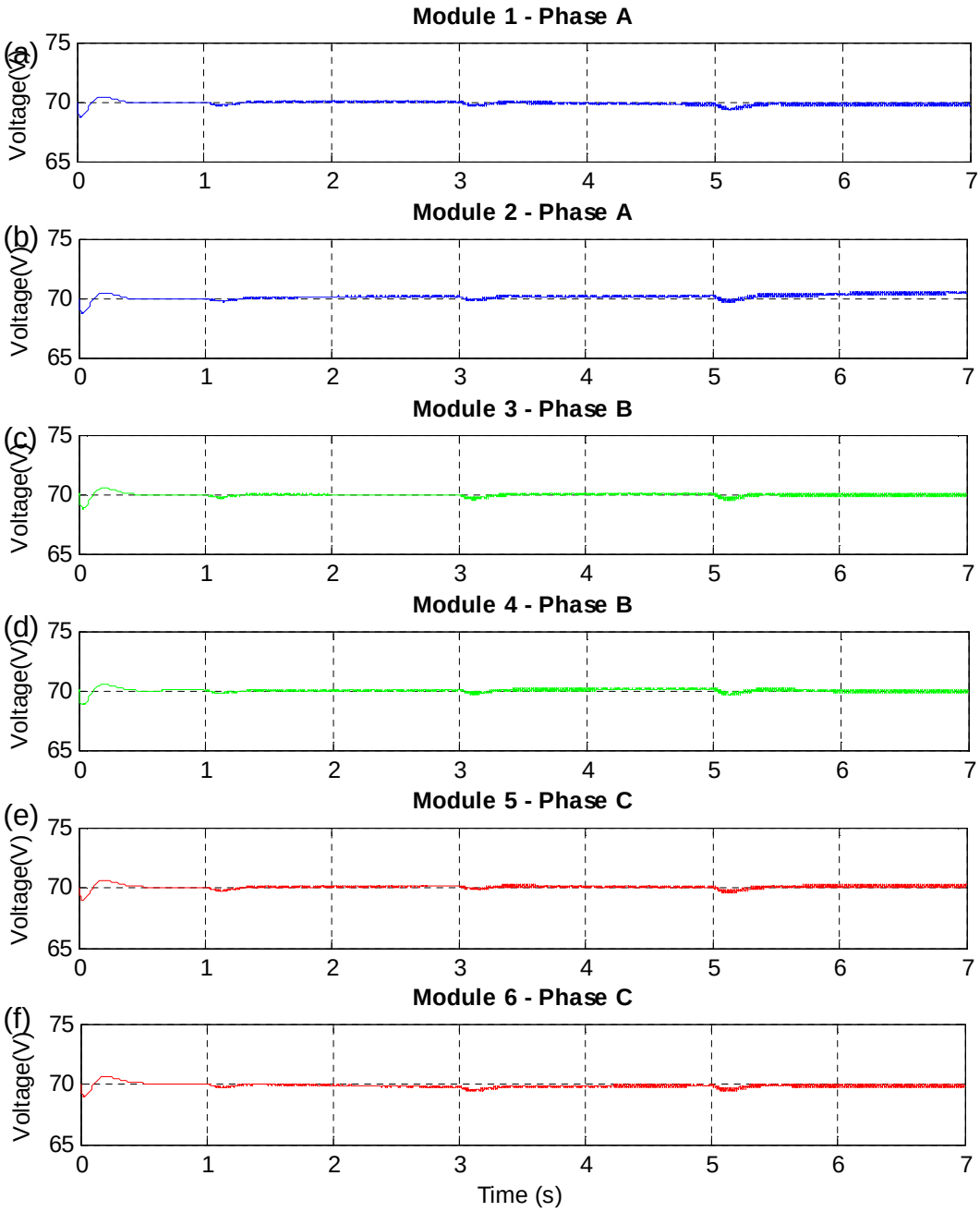


Figure 5.23: Outer Capacitor Waveforms

Figures 5.24 (a)-(c) show 10 cycle representation of the inner capacitor voltage waveforms at full compensation mode.

The inner capacitor voltages are shown to balance properly all maintained around 35 V which corresponds to half the outer capacitor DC voltage of 70 V. As discussed earlier in Chapter 2 certain phases tend to deviate slightly away from the expected nominal voltage.

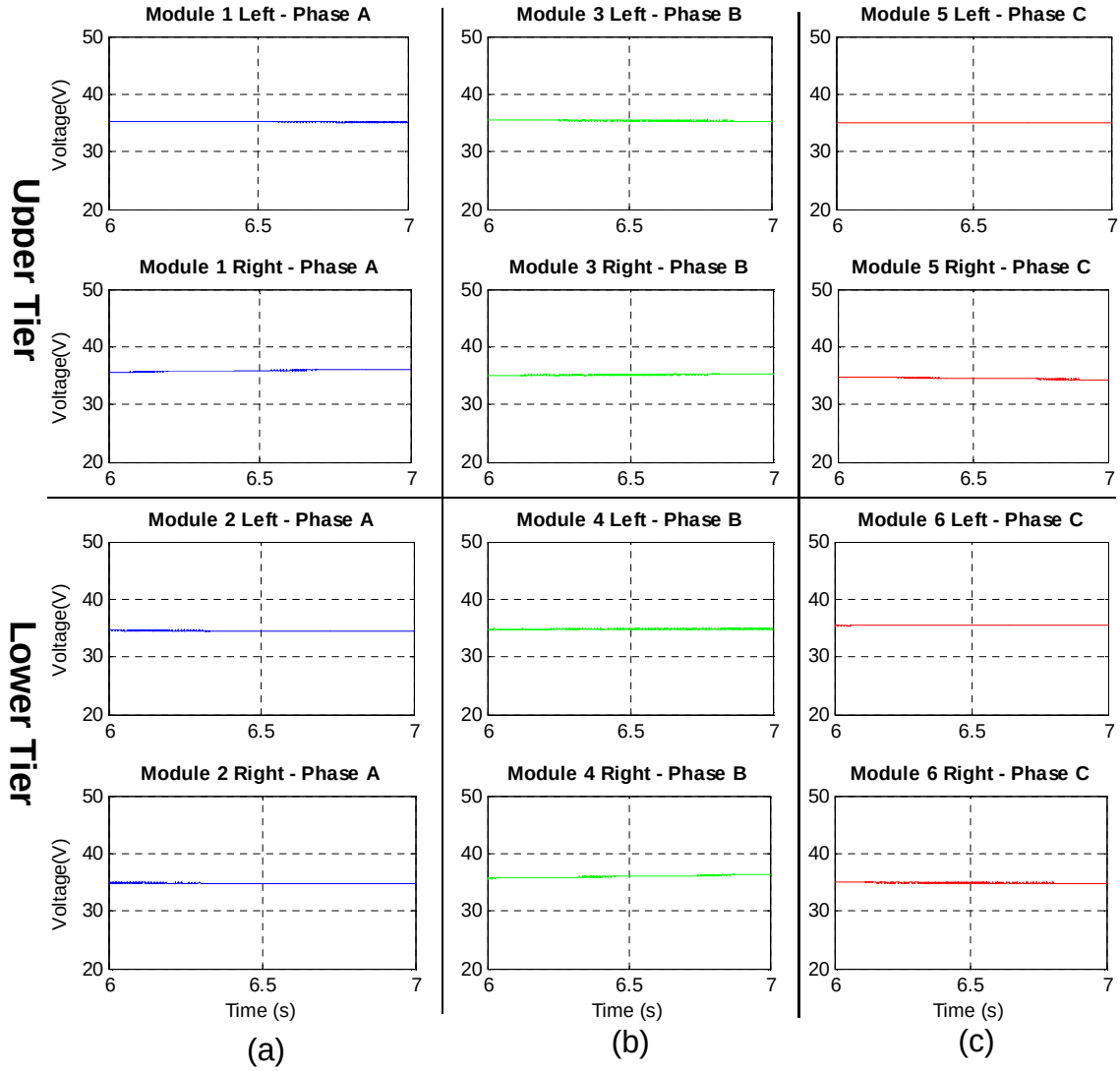


Figure 5.24: Inner Capacitor Waveforms

5.5 Conclusions

This chapter analysed the voltage and current phasor relationships when a power converter-based STATCOM is used in a three-phase balanced system. The analysis has led to the derivation of a novel method for directly determining the minimum required DC voltage ratings of the converter used for reactive compensation. The method only requires knowledge of the maximum load reactive power and converter filter impedance. Simulation study of an FC-MMC converter used for obtaining either PCC voltage regulation or power factor correction through reactive power compensation has been presented. With the control system designed the simulation results obtained show that converter responses are accurate with acceptable transient speed and no overshoot. The PCC voltage has been shown to be controlled to its nominal level despite a large load increase. The power factor of the system is maintained near unity for consecutive load inductive current increments.

Chapter 6
Experimental System

The control algorithms presented in the previous chapters and modulation schemes for converters need to be practically verified. This requires design and implementation of a scaled-down STATCOM based on a Flying Capacitor MMC already built by a previous PhD student at the University of Leeds Control and Power Applications laboratory. The author developed the system for closed loop control operation, which included the test power system, test power supply for sub-modules, data acquisition unit including capacitor feedback voltage measurement hardware and the DSP-FGPA software program codes. A simplified block diagram of the system is as shown in Figure 6.1. Apart from the converter itself, the essential element for this STATCOM is the complete control system formed by a measurement unit, its interface to the digital devices such as DSP and FPGA, and a software package for driving them to implement all data processing and control functions. This chapter covers the design and construction of the experimental system completed by the author. It starts by presenting the overall configuration of the FC-MMC-based STATCOM, showing clearly the connections of various hardware and software units. Subsequently the main part of the whole system, the FC-MMC, is described by presenting its modular structure, the circuit diagram for each of the 24 power cell cards, their protection and power supply circuits. Following the converter the hardware implementation for the system to perform control functions is discussed. There are two essential elements for this; an array of transducers for measuring voltage and current values from the FC-MMC and controlled power system, and digital devices for data acquisition and implementation of control algorithms. The latter comprises of a digital signal processor (DSP) and Field gate programmable array (FPGA), and its output drives a total of 48 switches. In addition, an Isolated DC power supply was required and built. This is to control the pre-charge action of the outer capacitors of the all six FC-MMC units at the initial testing stage. The details of all these devices and circuits and their interface to each other are presented in detail.

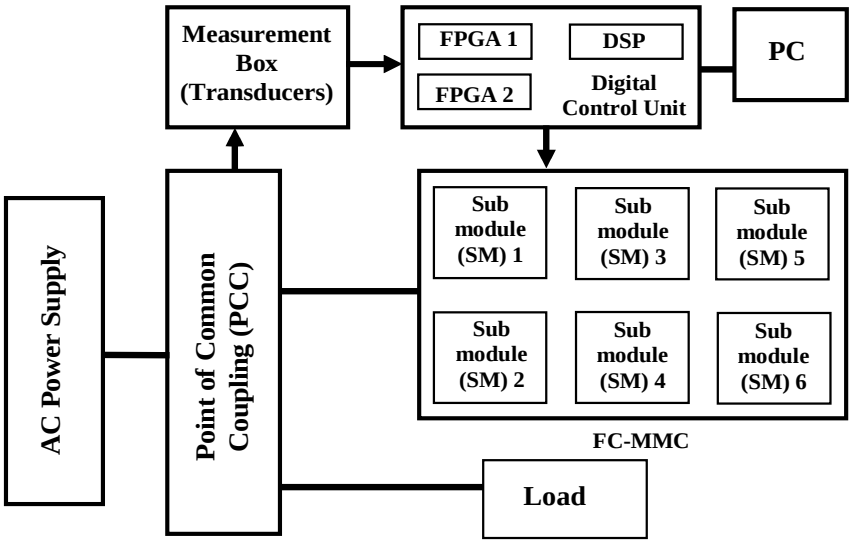


Figure 6.1: Block Diagram of FC-MMC STATCOM

6.1 The Structure of FC-MMC

The key feature of the experimental FC-MMC shown in Figure 6.2 is that it was constructed by interconnecting a number of basic power cells. This offers two advantages to the FC-MMC; it is scalable to suit higher or lower voltage ratings, and reconfigurable to form different converter topologies.

The chosen basic power cell is a two-level half-bridge converter consisting of a capacitor and a pair of complementary semiconductor switches. The constructed circuit card is as shown in Figure 6.2 (a) . The choice of this as the fundamental building block makes it easy to scale up converter voltage levels as multiples of such cell cards can be chained up. Also, it is very flexible when used to configure various converter topologies. For example, to form an H-bridge converter, two such cell cards can be connected in parallel with at their DC voltage terminals. Furthermore, for a 5-level half-bridge, the output voltage terminals of one cell card would connect in parallel to the capacitor of the other as shown in Figure 6.2 (b). To construct a 5-level full-bridge FC converter, four such cell cards are needed. These are grouped into pairs, the two cell cards in each pair are linked in series, and two pairs are connected in parallel as shown in Figure 6.3.

Using these basic cell cards to build an experimental three-phase FC-MMC, the number of cell cards required depends on the desired voltage levels the MMC should generate. In the prototype shown in Fig 6.4 (a), 9 voltage levels per phase are desired, so two 5-level full-bridge FC converters, called sub-

modules, are needed for each phase, and six for three phases. As already described, one such module, shown in Figure 6.4, needs four basic cell cards, so building six modules requires a total of 24 cards. Figure 6.4(a) shows a single module as constructed and one phase limb of the converter formed by connecting two such modules in series. The complete three-phase 9-level FC-MMC constructed from six modules is shown in Figure 6.4(b).

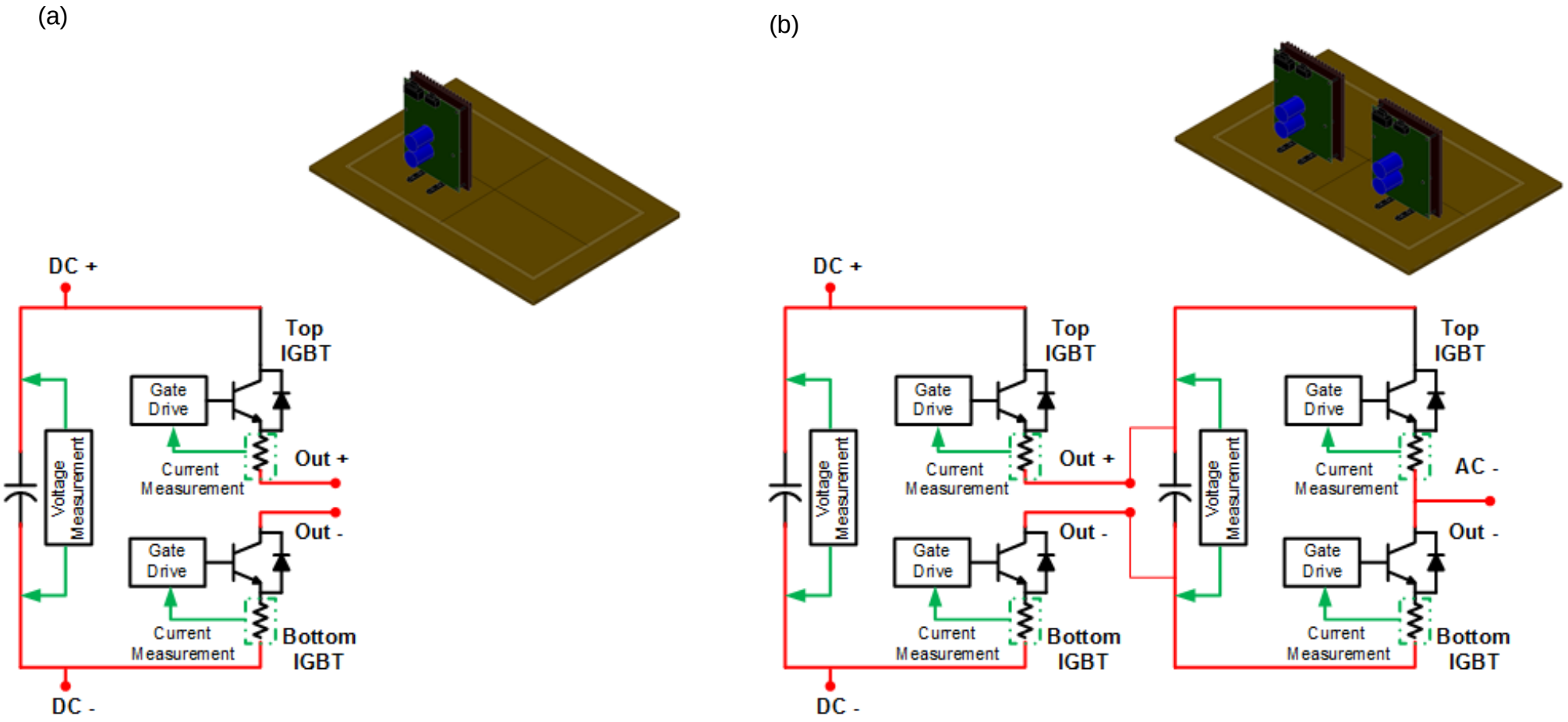


Figure 6.2: (a) Unit Power Cell (Half-bridge), (b) 5-level Half-bridge Flying Capacitor

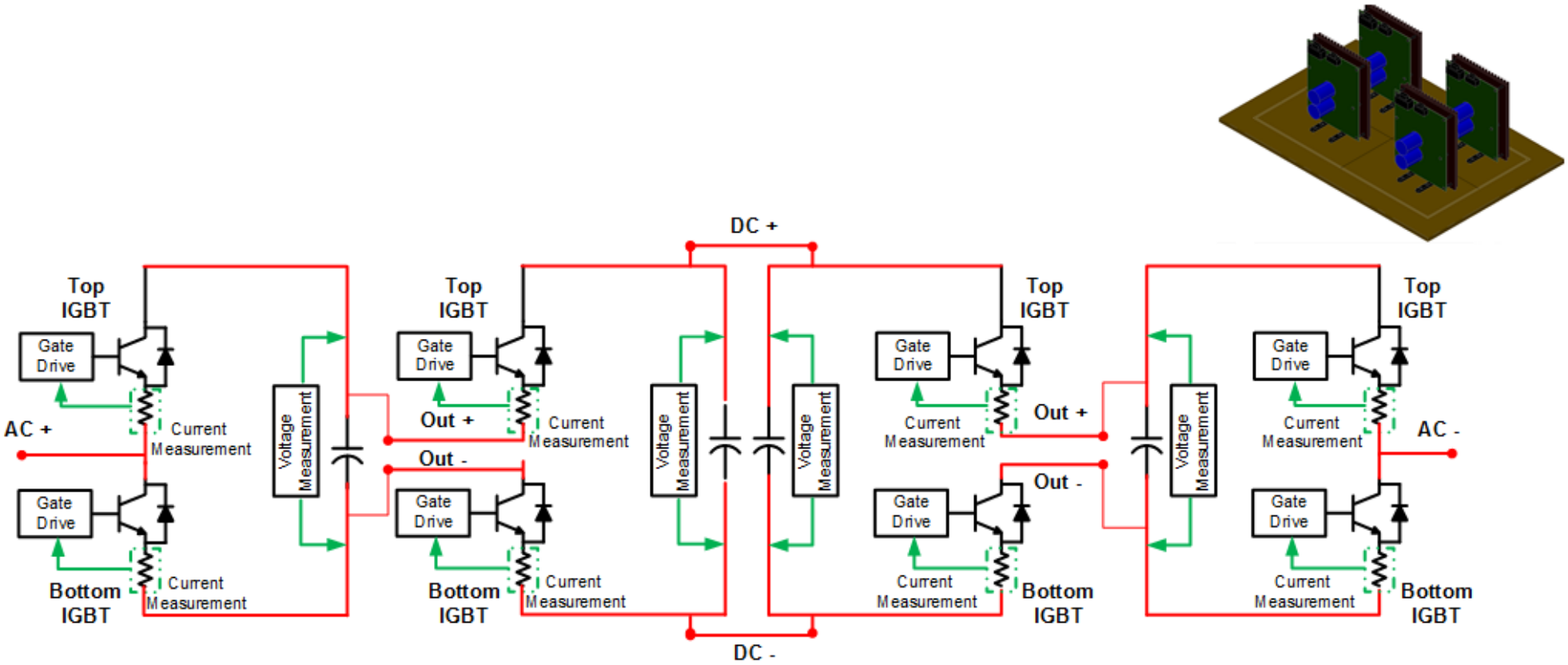


Figure 6.3: 5-level Full bridge Flying Capacitor

(a)

(b)

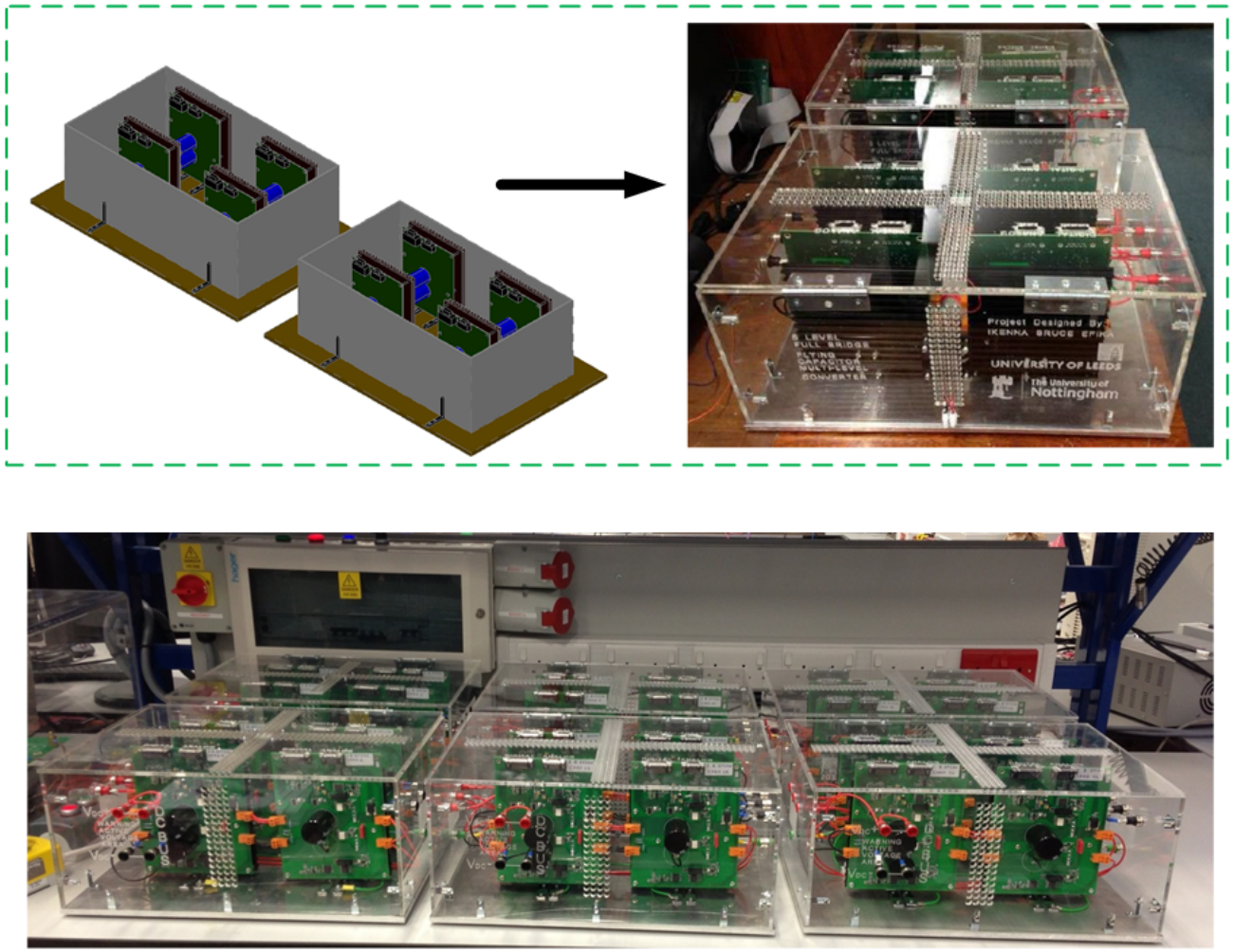


Figure 6.4: (a) Single Phase 5-level MMC-FC, (b) Three-Phase 5-level MMC-FC

6.1.1 Power Circuit of Cell Card

The circuit layout for the power cell card is a design of the Control and Power Applications Group at the University of Leeds [58] and is shown in Figure 6.5. Apart from the key elements, a pair of complementary IGBT-diode devices and a capacitor, the initial design of each of these card consists of an isolated 15V regulated DC-DC converter for power supply for the gate drive circuits, voltage and current sensing circuits and over current protection circuits as shown in Figure 6.5. Further modifications have been made for receiving switching pulses from fibre optic transmitter-receiver. Each power cell card is a surface mount double layer printed circuit board (PCB) as shown in Figure 6.6. The PCB creepage and clearance distances are designed to withstand up to maximum of 800V,15A. S-R latching circuits are used to reset the protection circuitry when over voltage and current faults occur. Figure 6.7 shows the power cell card after surface mount components have been populated. Further detailed explanations of the power cell card components will be discussed in subsequent sections.

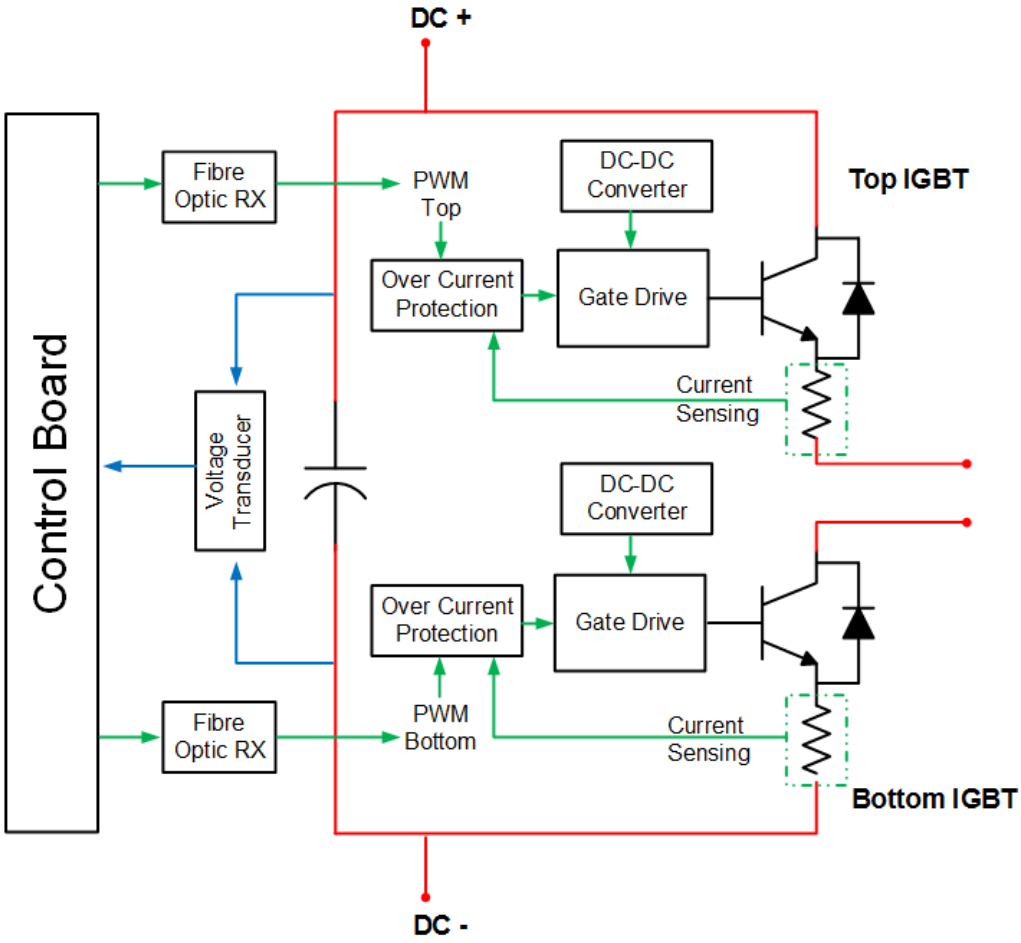


Figure 6.5: Unit Power Cell Circuit Diagram

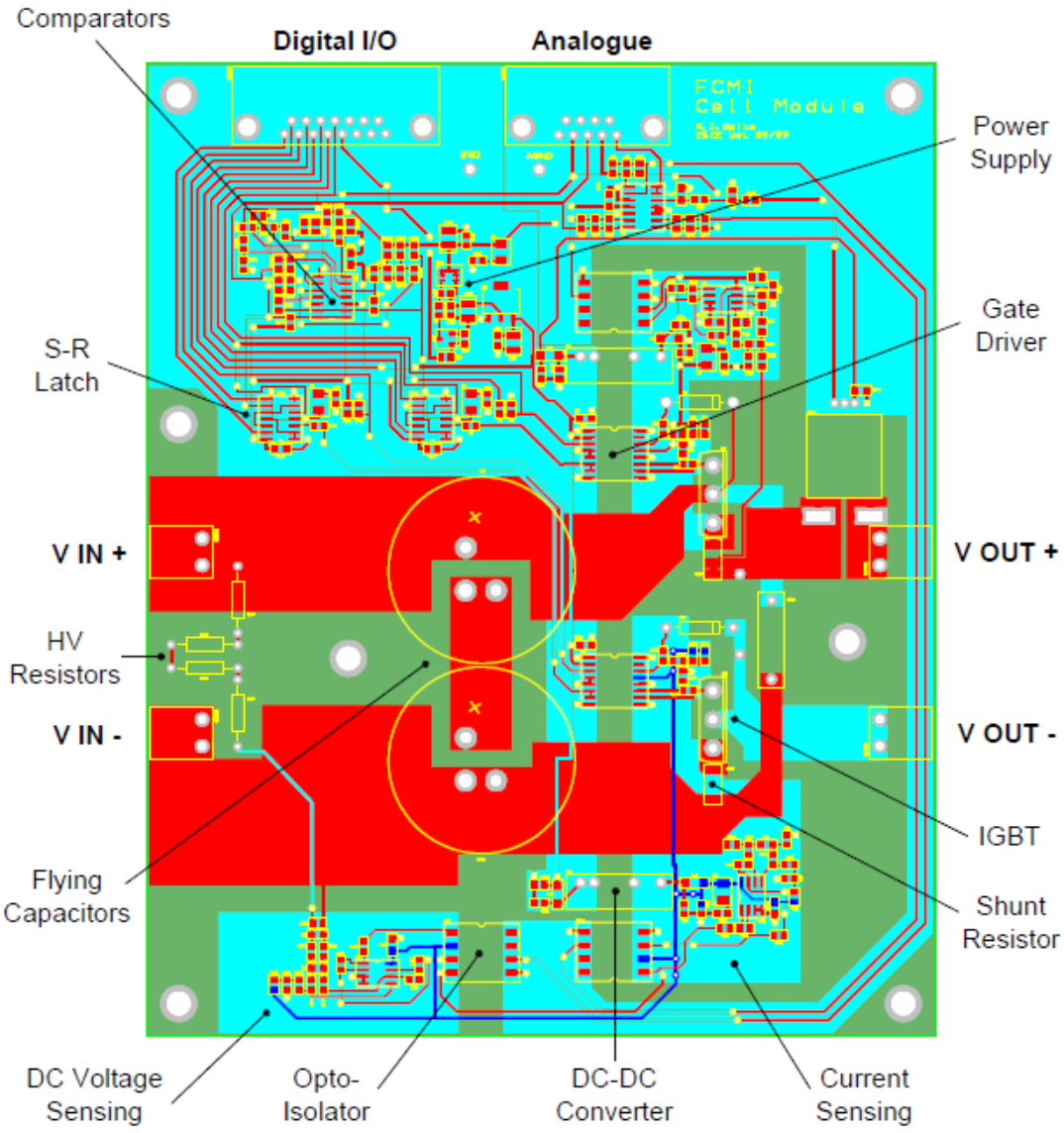


Figure 6.6: Unit Power Cell Card PCB Design

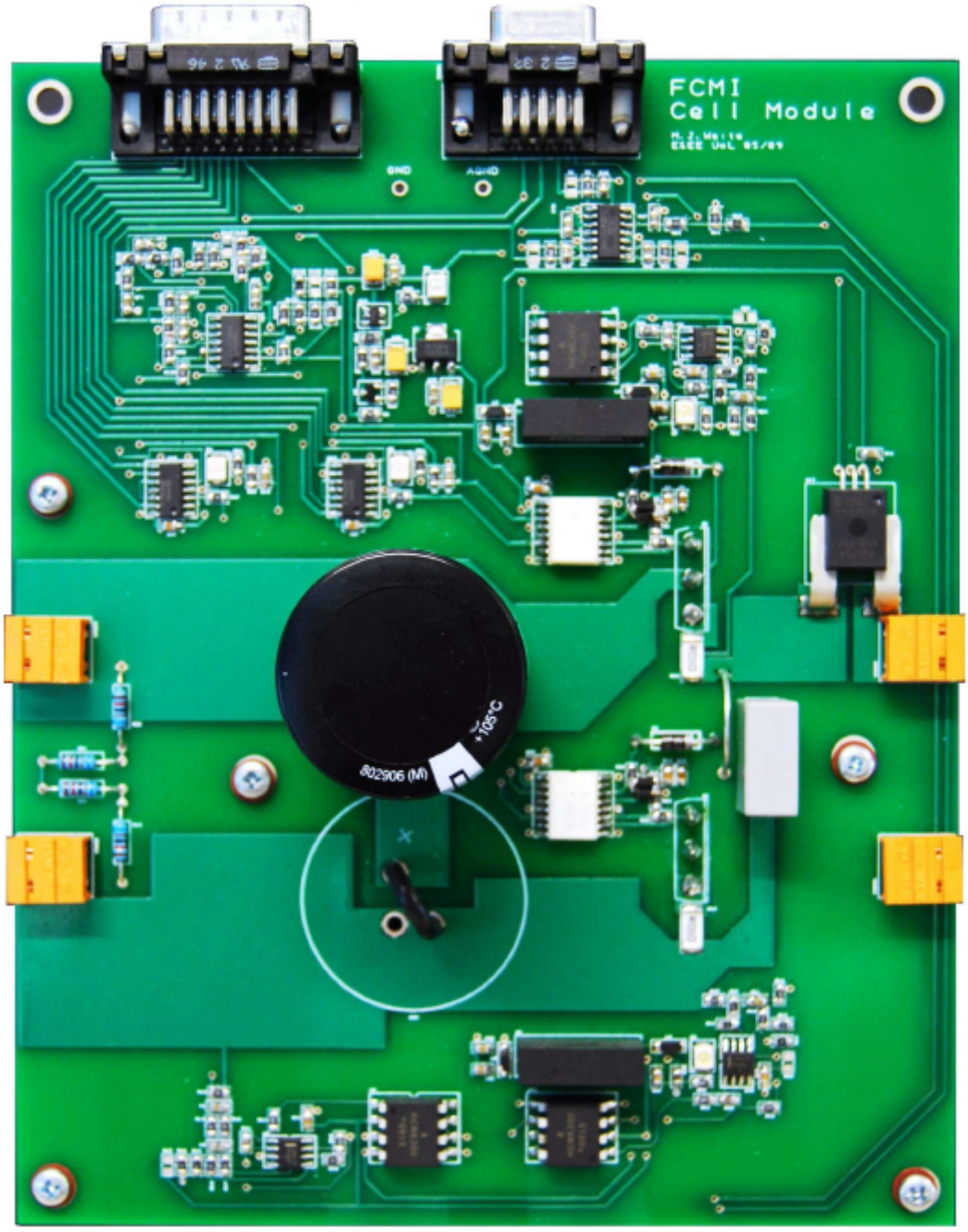


Figure 6.7: Manufactured PCB

6.1.2 Gate Drive Circuit

The gate drive circuit provides the required voltage to drive the IGBT switches to switch on or off. The IC device used is the ACPL-332J from Avago technologies [198] and is a combined package with opto-coupler isolation and gate drive electronics. This provides galvanic isolation between the analogue and digital control signals. The IC device also has additional protection functionality with miller clamping and desaturation detection to slowly turn off the IGBT when there is insufficient or over current flowing through.

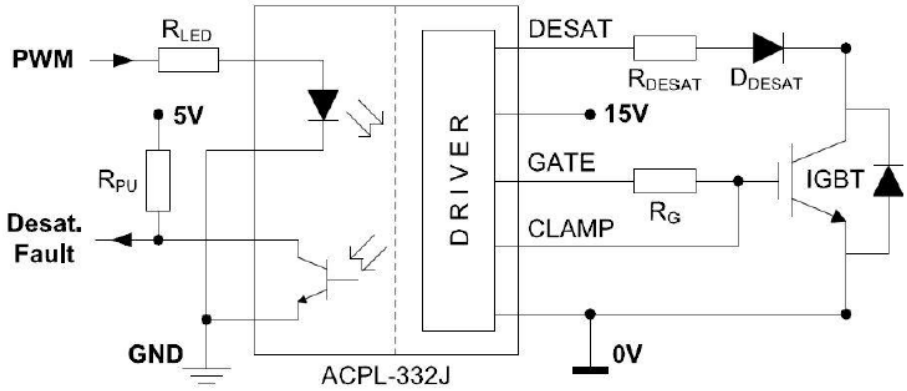


Figure 6.8: Gate Drive Circuit

6.1.3 Fibre Optic Transmitter/Receiver Circuit

To further enhance galvanic isolation and prevent signal interference, fibre optic transmitter and receiver circuits were included in the modified version of the above described power drive circuit. These are based on Avago's technologies HBFR-1521 transmitter and HBFR-2531 receivers [199] and are populated on a PCB board as shown in Figure 6.9. Provision is made on the PCB boards for the 5V power supply that powers the DC-DC converters for the gate drives in each power cell card.

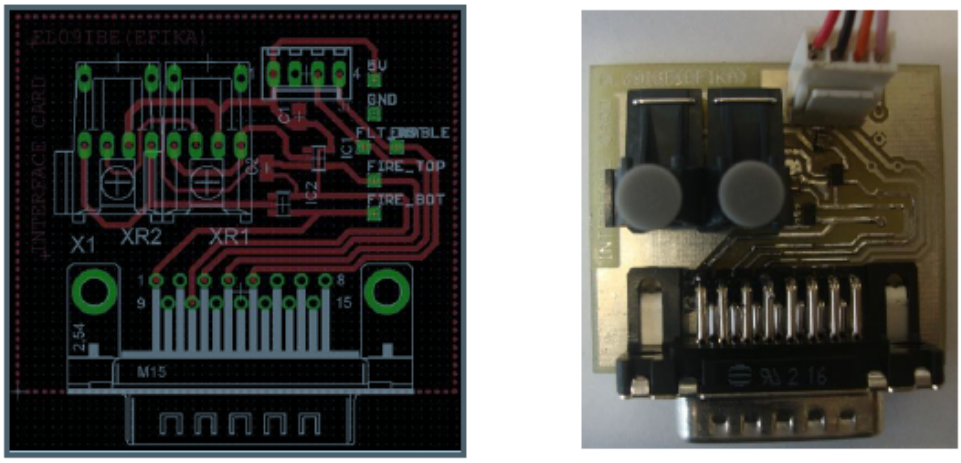


Figure 6.9: Fibre Optic Receivers PCB Design

Figure 6.10 shows the circuit diagram of the fibre optic receiver and transmitter. The switching control signals from the digital device are applied to the transmitter data input terminal to be converted into light signals, they are then propagated through the HFBR EU5100 fibre optic cable, The receiver on the other end of the cable is connected to the opt-coupler on the power cell card via D15 sub connectors. The schematic for the design is as shown in Figure 6.11

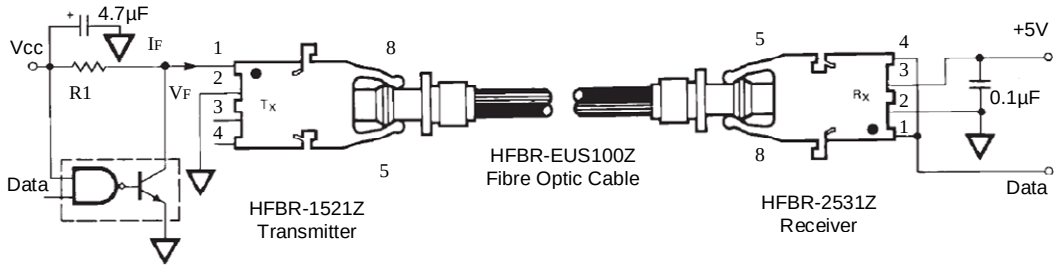


Figure 6.10: Fibre Optic Transmitter and Receiver Circuit Diagram

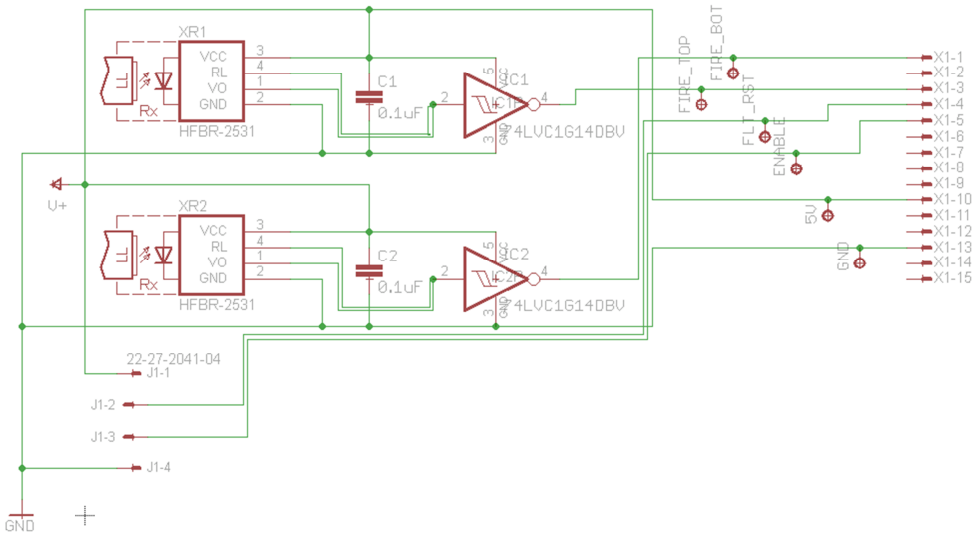


Figure 6.11: Schematic for Fibre Optic Transmitter and Receiver

6.1.4 Power Supplies for Cell Cards

The power supply layout for the power cell cards is shown in Figure 6.12. The circuit has four different power supplies at 3.3V, 5V, 15V and ± 15V. The 5V power supply is connected across all the sub-module boxes and is the main supply used to power up all the on-board electronics on the power cell cards. These are distributed via the fibre optic PCB connectors, as explained earlier in Section 6.1.2.

The 3.3 V power supply provides power for the some on-board devices in the protection circuitry and is generated each through linear voltage regulators as shown in Figure 6.13. A P-channel MOSFET with the aid of an NPN transistor creates a switchable transition within the 3.3 V rail that allow activates the power when then enable signal is received. Other devices on the on isolated power end require a 5V power supply.

The 15V power supplies are generated using the 1W switch mode DC-DC converters shown in Figure 6.14 and powers the gate drive electronics. A L-C low pass filter with a cut of frequency of 70kHz (L = 1µH, C = 4.7µ) is fitted at both end to suppress high frequency noise. power supply powers up the voltage transducer for the electronics at the non-isolated side including the.

The ± 15Vpower supply is provided using a switch mode AC-DC converter and powers up the voltage transducers for the capacitors on each cell card.

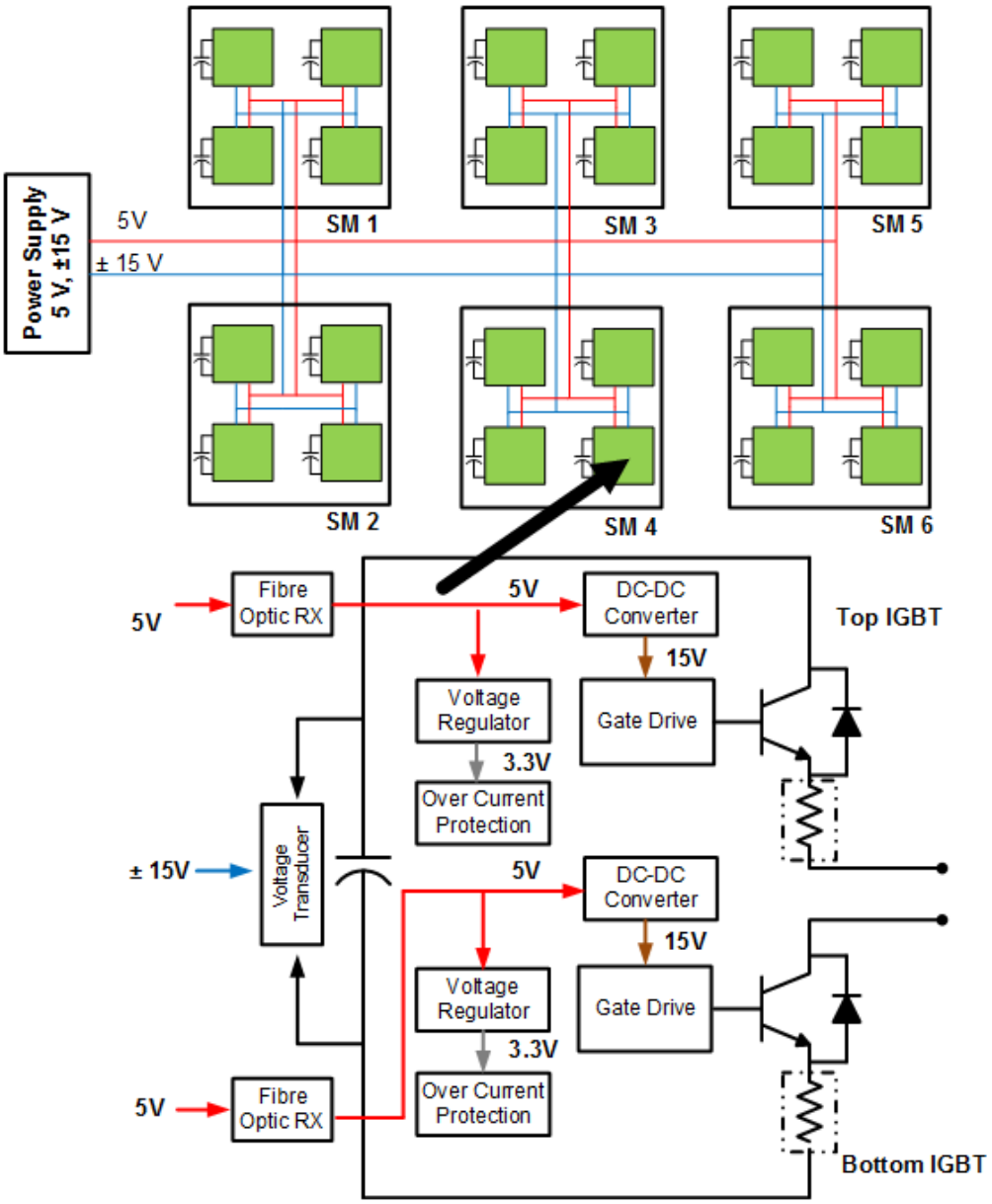


Figure 6.12: Power Supply Layout

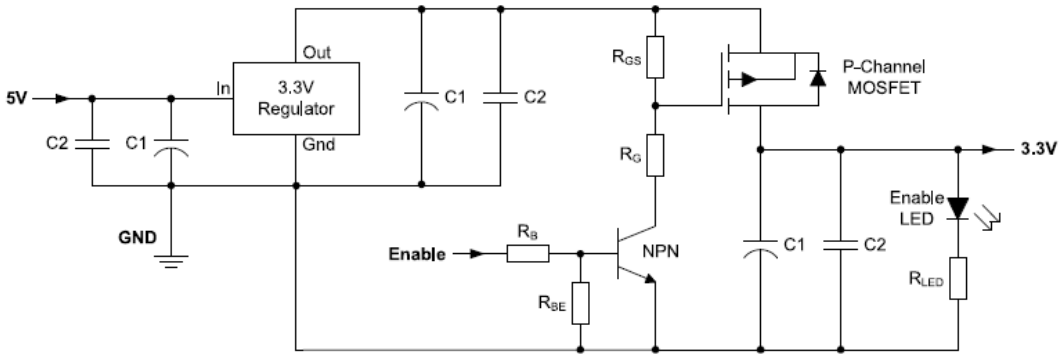


Figure 6.13: +3.3 V Switch Mode Power Supply

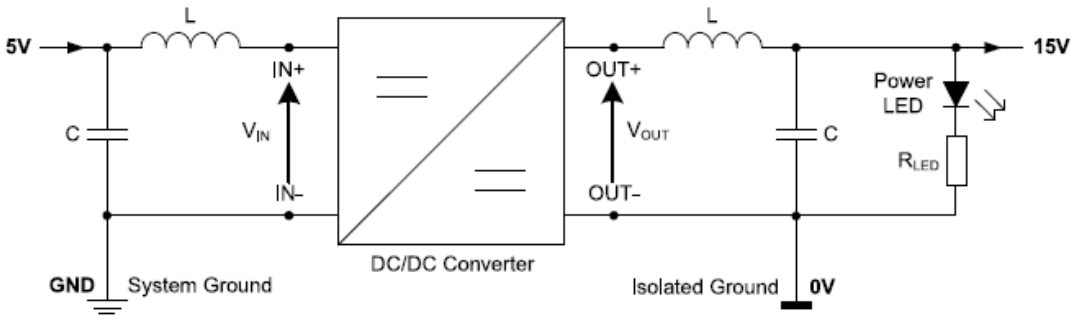


Figure 6.14: +15V Switch Mode Power Supply

6.1.5 Isolated DC Power Supply

In order to pre-charge the outer capacitors on each sub-module and test at higher voltages in an open loop scenario, a variable isolated DC voltage power supply was built. This comprised of a three-phase auto transformer connected with two isolated transformer at each phase as shown in Figure 6.15.

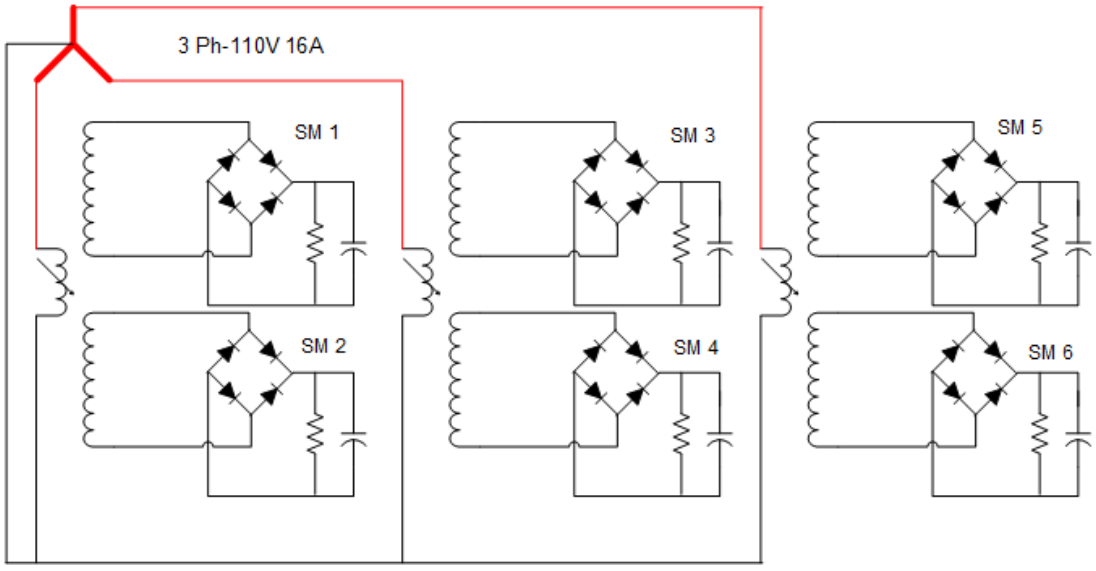


Figure 6.15: Isolated DC Power Supply Circuit

The three-phase auto-transformer provides a variable voltage up to the rated 110V power supply in the laboratory and is rated at 16 A per phase. The isolating transformer used is 110V-220V Clairtronic 625VA toroidal transformer and is configured as a 1:2 step-up transformer realising maximum of 220 V_{DC} for each outer capacitor. This would allow for the each phase of the converter to provide 440 V_{Pk-Pk} at each phase. A diode bridge rectifier with a maximum rated voltage of 600V was used to convert the AC to DC voltages and a large capacitor Aerox ALS31A 3300µF was used to suppress the 100Hz ripples to realise good quality DC voltage.

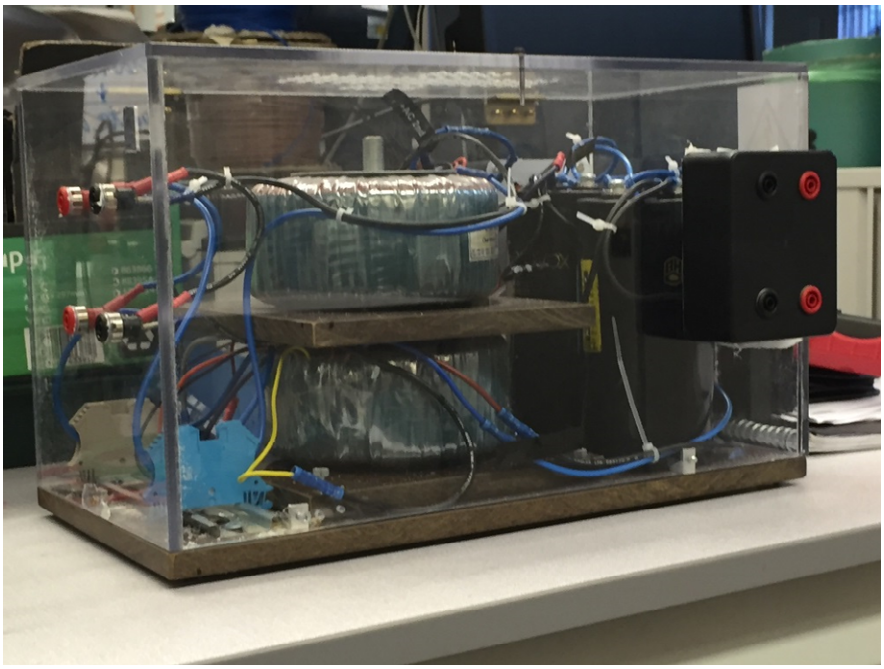


Figure 6.16: Built Isolated DC Power Supply (One Phase)

6.1.6 Power Components

6.1.7.1 Switching Device

The switching device used in the power cell card is an Infineon IKLW30N6OT [144] and is coupled together with an anti-parallel fast recovery diode T0-247. The device characteristics are summarised in Table 6.1. The low collector-emitter saturation voltage and faster turn-on and turn-off times help reduce the device losses although the actual device losses are mainly due to conduction losses and switching losses (dependent on the modulation scheme).

Table 6.1: IGBT Characteristics

Parameter	Value
Maximum collector-emitter voltage V_{CE}	600 V
Maximum DC collector current I_C	30 A
Short-circuit collector $I_{C(SC)}$	275 A
Short-circuit withstand time t_{SC}	5 µs
Collector-emitter saturation voltage $V_{CE(sat)}$	1.5 – 1.9 V
Gate-emitter threshold voltage $V_{GE(Th)}$	4.1 – 5.7 V
Total turn-on time t_{on}	44 – 50 ns
Total turn-off time t_{off}	300 – 382 ns

6.1.7.2 Capacitors

The capacitor selected for use in the power cell card is a Panasonic TD-ED series large can aluminium electrolytic capacitor [200]. The capacitor is rated at 400V and was selected according to the simulation model and design requirements, giving a suitable dc ripple within the ±10% of the mean value. Table 6.2 summaries the capacitor device characteristics.

Table 6.2: Capacitor Characteristics

Parameter	Value
Capacitance	560 µ ± 20%
Maximum working voltage	400 V_{DC}
Maximum surge voltage	450 V_{DC}
Maximum RMS ripple current (120 Hz)	5.52A
Maximum RMS ripple current (10 kHz)	7.70 A
Lifetime	3000h

6.2 Data Acquisition Unit

To enable the above presented converter functioning as a STATCOM, a data acquisition unit was constructed. The hardware structure of this unit comprises a measurement box installed with multiple transducers for measuring the voltage and current values of the AC and DC parts of the power system and the FC-MMC. The measured analogue signals are then applied to DSP of the digital control unit for conversion into digital form and used for control signal calculation. The details of these are discussed in the subsequent sections.

6.2.1 Voltage Measurement

The voltage measurement circuit comprises of voltage transducers employed to capture the AC voltages at the source, load and converter. The LEM LV 25-P voltage transducers were used [201]. These transducers have good accuracy and provide a good resolution of the voltage signal with a conversion ratio of 1:2.5. They have good linear characteristics with low linearity error and have high immunity to noise and external interference. Isolation is also provided between the primary and secondary coil and this prevent coupling of the low voltage control signals. The same transducers were employed to measure the outer capacitors on the converter. The maximum voltage of the device is 500 V able to withstand the rated voltage of the capacitor of the cell card at 400V. The power circuit for the transducer is as shown in Figure 6.17.

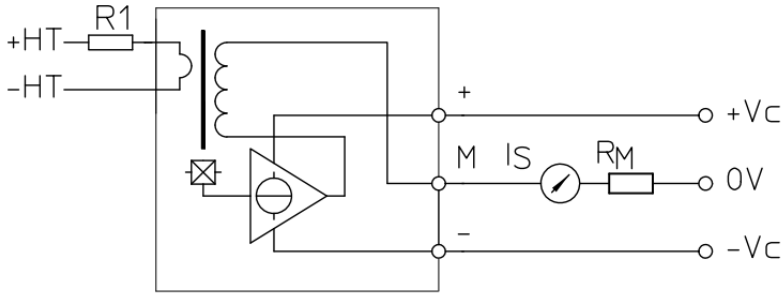


Figure 6.17: Voltage Transducer Circuit

The transducers are powered up through a ±15V power supply. The resistor R_1 is calculated such that the rated voltage produces a rated primary current of 10mA. This ensures that the transducer is operating and establishes its

optimum accuracy range. The expression to find the maximum measurable voltage is as shown in (6.4) . The current is stepped up at the secondary coil by a factor of 2.5 and, with the aid of the burden resistor R_M , this can be scaled up to measurable voltage range.

$$V_{M(msx)} = \frac{V_{in(\max)}}{R_1} \times 2.5 \times R_M \tag{6.4}$$

6.2.2 Current Measurement

The current measurement circuit comprises hall effect current transducers employed to capture the current flowing at the PCC, load side and converter side. The LEM LA 55-P current transducers were used [202]. These transducers provide a good resolution of the current signal with a conversion ratio of 1:1000 and have good linearity and immunity to external interference. The maximum current rating of the device is 50 A able to withstand the rated current of 10A of the power system. The power circuit for the current transducer is as shown in Figure 6.18.

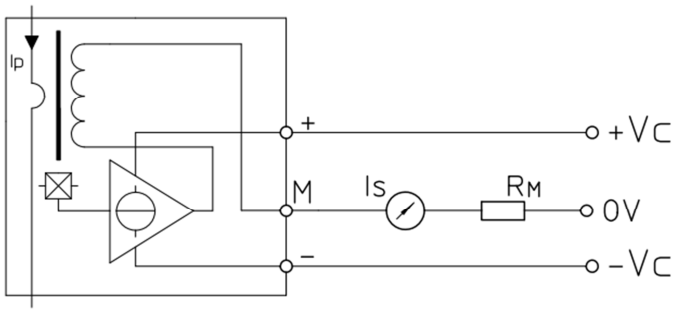


Figure 6.18: Current Transducer Circuit

The current transducers have similar operation as those described earlier in Section 6.2.1 powered by same ±15V power supply and a scaled up using a burden resistor R_M . The expression to find the maximum attainable current is as shown in (6.5).

$$V_{M(msx)} = I_{in(\max)} \times \frac{1}{1000} \times R_M \tag{6.5}$$

6.2.3 Measurement PCC Box Layout

The measurement box consists of a combination of 9 LEM LV-25-P voltage transducers and 9 LEM LA 55-P current transducers, as seen in Figure 6.19. A group consisting of three transducers measure the source side, load side and converter side voltage and current respectively. At the rear are

connectors from which carry the capacitor voltage analogue feedback signals to the break out connectors highlighted in red. Shielded ribbon cables were used to avoid interference between signals. Figure 6.20 shows the built box. Figure 6.21 and Figure 6.22 show the PCB schematic for the printed circuit boards.

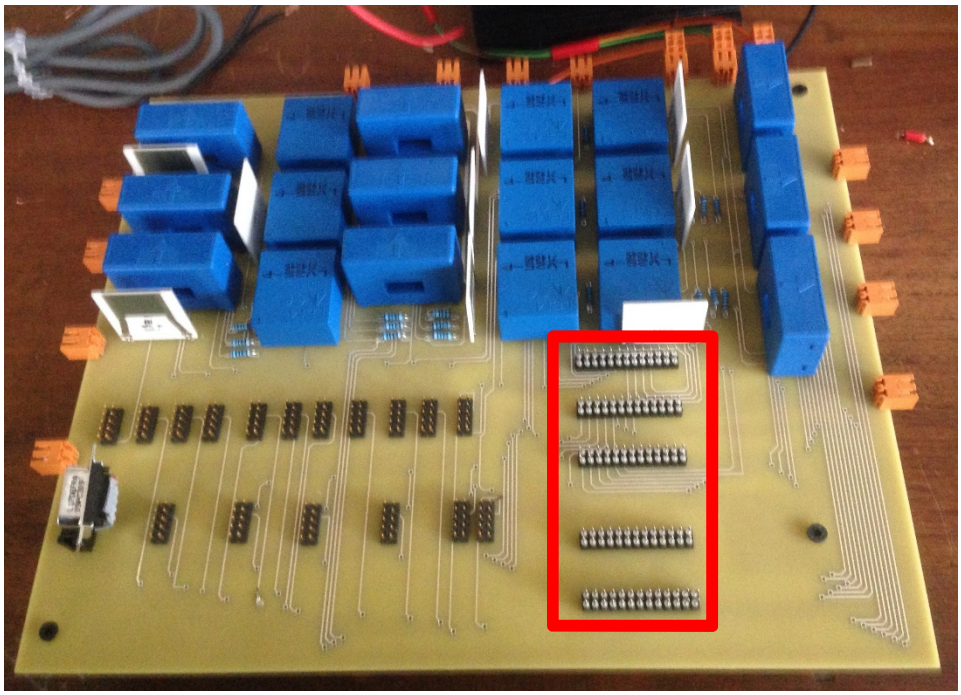


Figure 6.19: Populated PCB of PCC Measurement Box

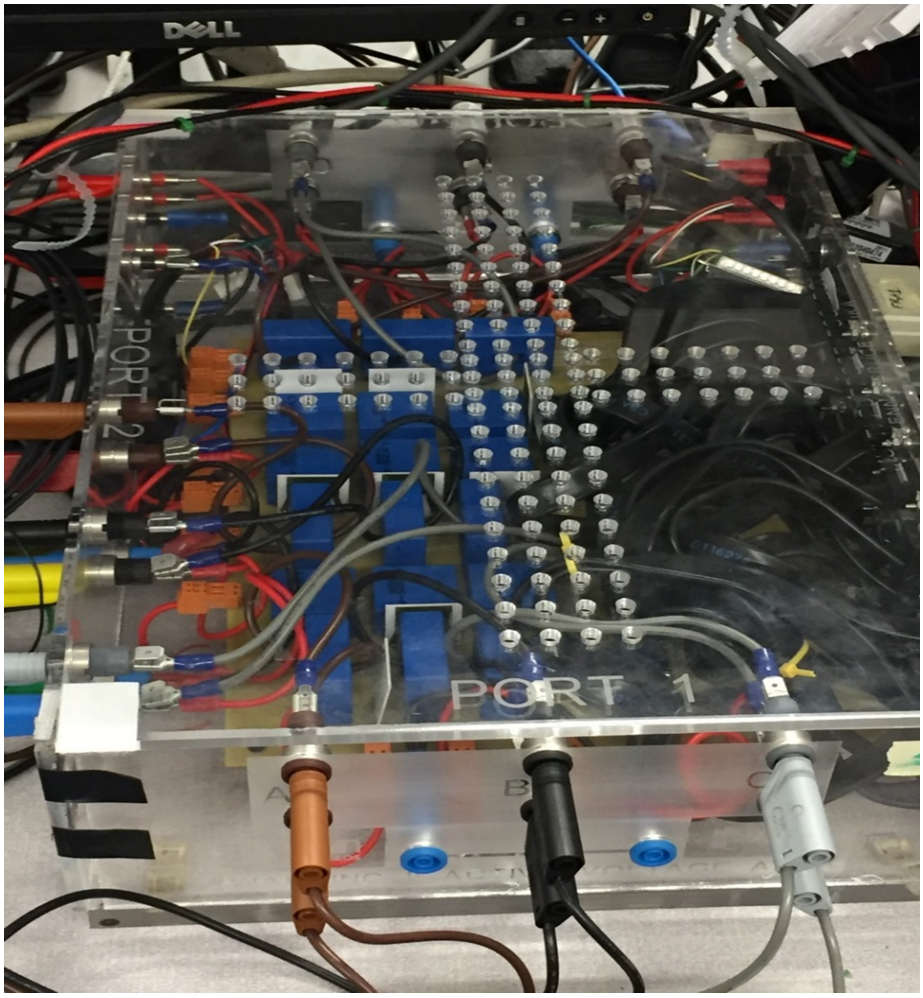


Figure 6.20: Built PCC Measurement Box

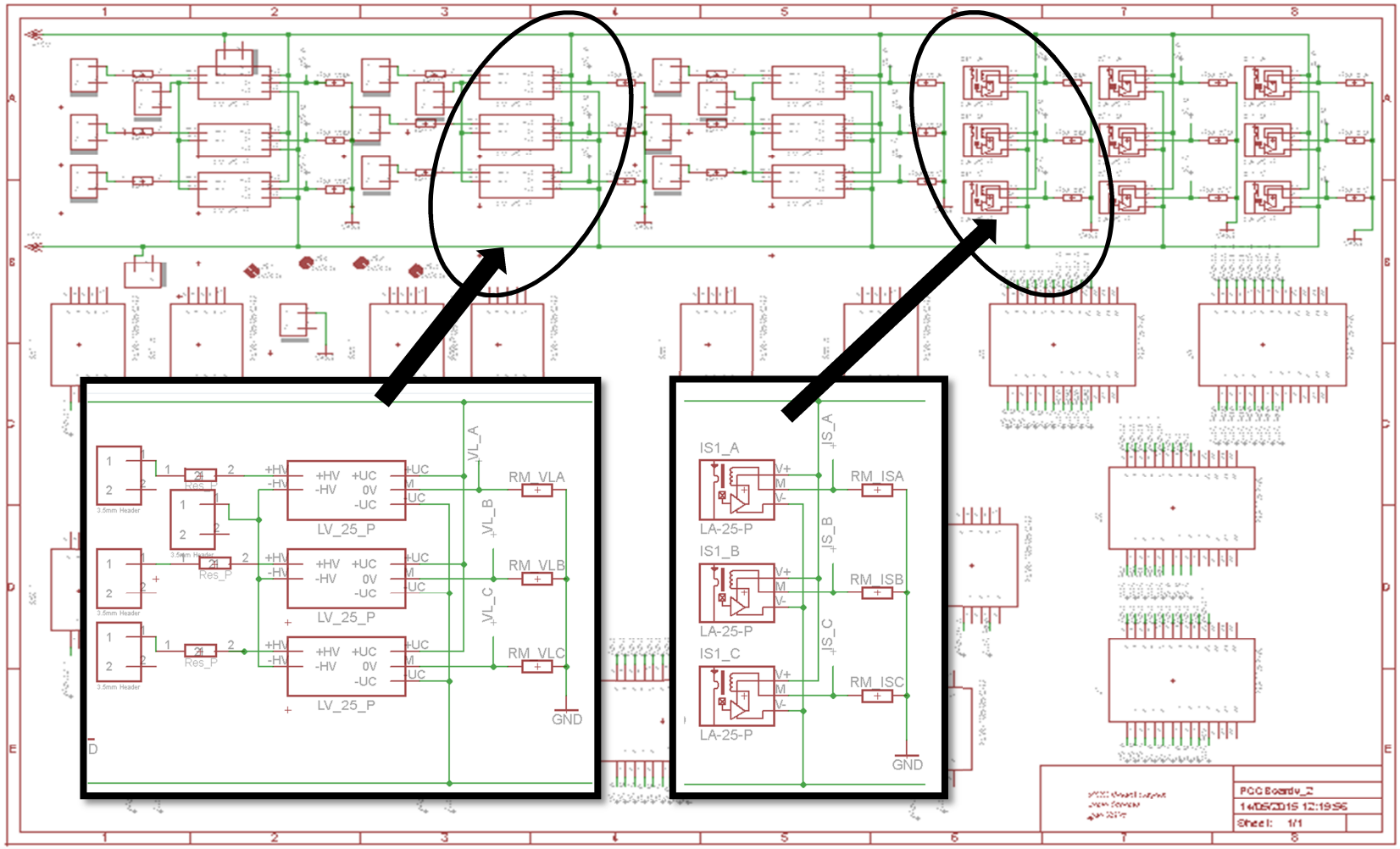


Figure 6.21: Schematic for PCC Measurement Box

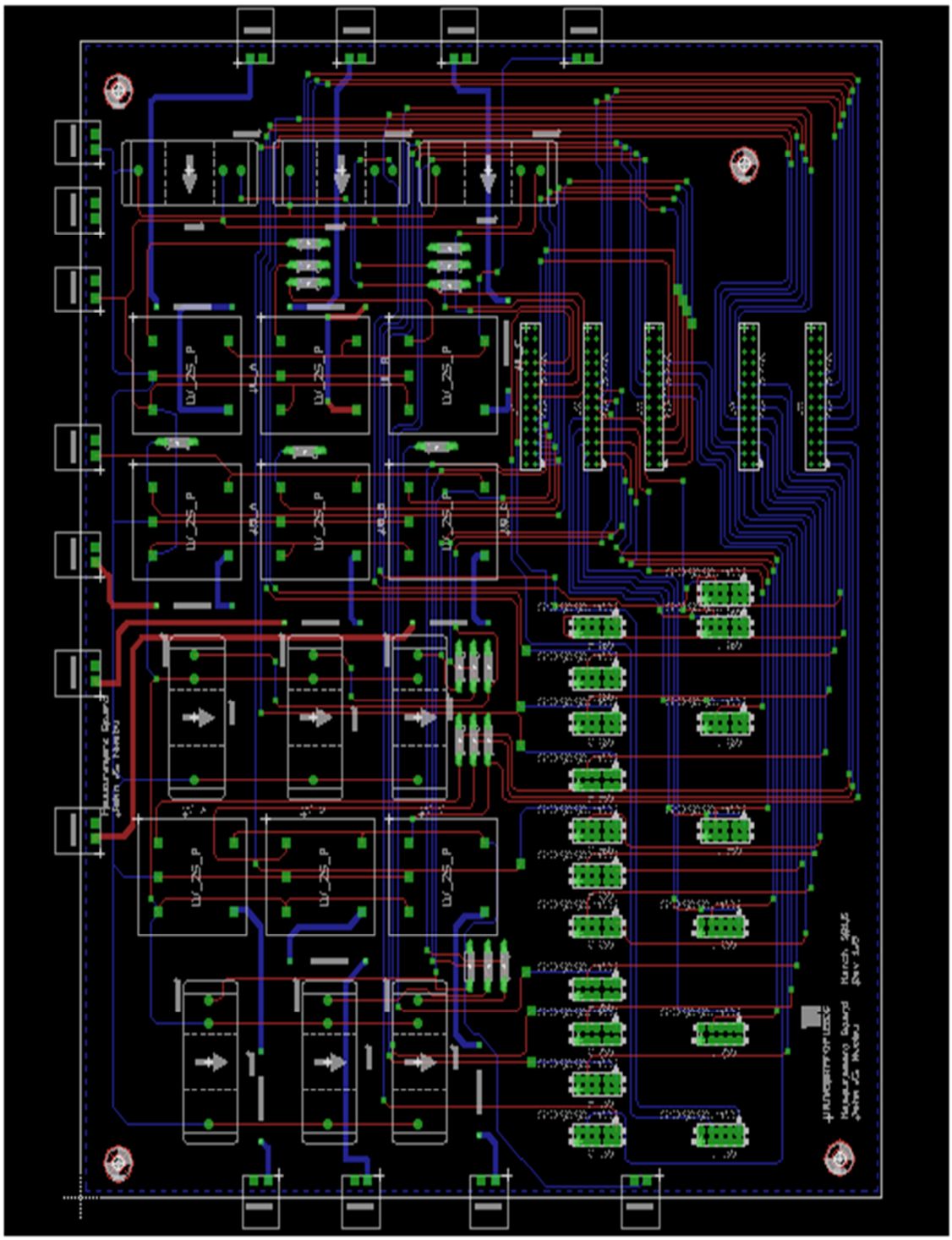
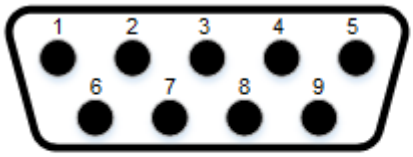


Figure 6.22: PCB Schematic for PCC Measurement Box

6.2.4.1 Pin layout Power Cell Card Feedback

The feedback signals for each unit cell card are distributed via 9-way D-sub connectors to the measurement box. Three D-sub connectors convey signals for each sub-module, two for the inner capacitor measured signals and one for the outer capacitors. Hence a total of 18 9-way D-sub connectors are used to convey analogue feedback signals for the total six sub-modules. Figure 6.23 shows in the pin layout of the feedback signals measured.



Pin Configuration
1 – Analogue Ground
2 – Bottom Switch Current
3 – Top Switch Current
4 – Capacitor Voltage
5 – Output Current
6 to 9 – No connection

Figure 6.23: Pin layout Feedback Signals

Pins 2 and 3 carry measured current flowing through the respective top and bottom IGBT's. Pin 4 is connected to the output from the voltage transducers at the each capacitor.

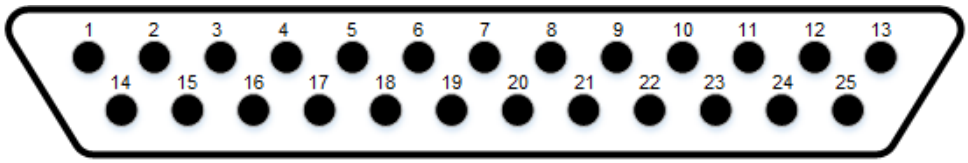
6.2.4.2 Pin layout Breakout Connectors

All measured signals including PCC voltage and current, outer capacitor and inner capacitor voltages are distributed to the FPGA Board via four 25-way D-sub connectors for analogue to digital conversion. Two FPGA cards to be described in the following section were used. Each FPGA card is limited to a total of 20 analogue signals per card, hence the arrangement of the signal were arranged in a way two possible types of application can be undertaken

- Application with outer capacitors: Comprising of PCC side voltage measurements $V_{PCC\,abc}$ for synchronisation, PCC, load and converter current signals $I_{PCC\,abc}$, $I_{L\,abc}$, $I_{C\,abc}$ load side current and outer capacitors V_{DCM1}-V_{DCM6}. As phase shifting PWM is the proposed scheme, the inner capacitors would be controlled effectively to balance by switching.
- Application with inner capacitors: This comprises of all the 12 inner capacitor voltages measurement and would be possible if an additional FPGA card is available in the future.

Figure 6.24 shows the layout for all 25-way D-sub connectors. All other unused measured signals are provided at the last connector J5 for aid

future users of this box to allow for creation of breakout boards that can route signals in different settings for various applications.



Pin Configuration (Connector J1)

1 to 3 – PCC Voltage (Phase A to Phase C)
4 to 6 – Converter Current (Phase A to Phase C)
7 to 9 – Load Current (Phase A to Phase C)
10 – Capacitor Voltage (Sub-Module 1)
14 -23 – Ground
Other Pins – No connection

Pin Configuration (Connector J2)

1 to 5 – Capacitor Voltage (Sub-Module 2 to 5)
6 to 8 – PCC Current (Phase A to Phase C)
14 -21 – Ground
Other Pins – No connection

Pin Configuration (Connector J3)

1 to 3 – PCC Voltage (Phase A to Phase C)
4 to 6 – Converter Current (Phase A to Phase C)
7 to 10 – Inner Capacitor Voltage
(Sub-Module 1 to 2)
14 -23 – Ground
Other Pins – No connection

Pin Configuration (Connector J4)

1 to 8 – Inner Capacitor Voltage
(Sub-Module 3 to 6)
14 -21 – Ground
Other Pins – No connection

Figure 6.24: Pin Layout for Breakout Connectors

6.3 Devices and Digital Control Unit

The digital device for the control unit is a combination of an ACTEL Pro Asic 3 FPGA module and a Texas Instrument 32 bit floating point digital signal processor (DSP). The software for the control unit processes the measured data from the transducers and converts them into digital form for use to perform power flow control actions. The FPGA modules are populated on a printed circuit board designed by the Power Electronics, Machine and Control Group (PEMC) at the University of Nottingham.

The DSP communicates with the FPGA through its external memory interface (EMIF), and a host port interface (HPI) daughter card is used to monitor the EMIF in real time during operation. The FPGA card performs two main functions:

1) Sampling the measured signals and transmitting them across to DSP to perform control actions through an interrupt routine
2) Translating received control actions from the DSP to generate switching signals for the converter.

Additional functions for analogue/digital conversion and digital input/output operations are included.

Code Composer Studio software using C programming an Assembly code is used for programming at the DSP whilst Libero SoC is used to program the FPGA board. Figure 6.25 shows the layout of this setup.

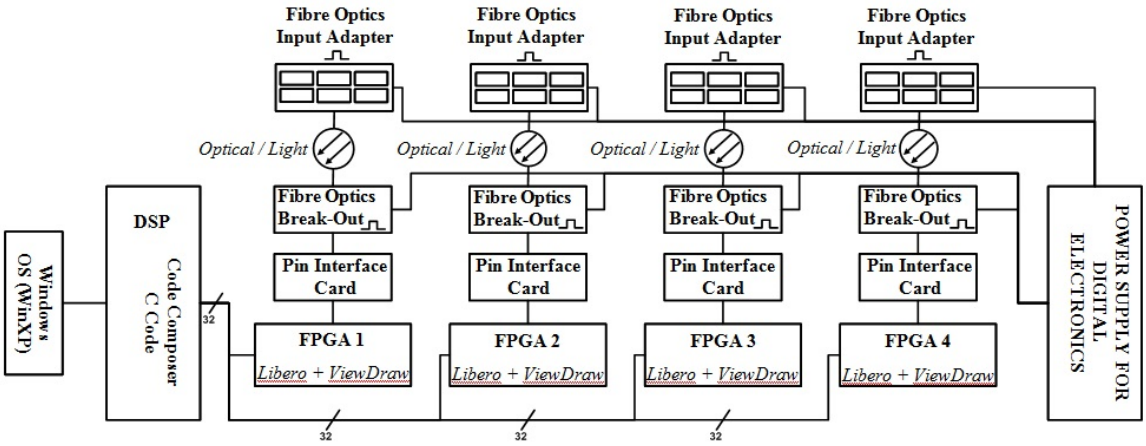


Figure 6.25: Block Diagram Software Control Unit

6.3.1 FPGA Cards

The FPGA card consists of the following components as shown in Figure 6.26.

(a) Actel ProASIC III FPGA Chip for data processing
(b) Three Phillips LVC16245A bidirectional buffers
(c) One Phillips 74LVC245A bidirectional buffers
(d) 26 pin I/O Header connectors
(e) Fault monitor display LED
(f) 10-way programming connector for Flash Pro 4
(g) Burden resistors for A/D converter at ±5V voltage range
(h) 4-way header connector for Set/Reset Enable under faults
(i) 25-way D-Sub connector for input A/D signals
(j) 10 LTC 1407A-1 Analogue to Digital converters .

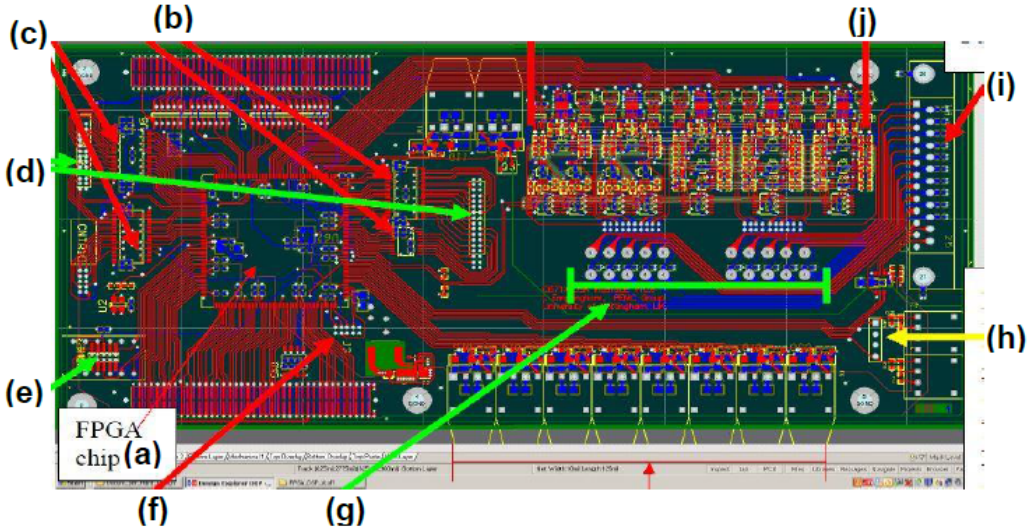


Figure 6.26: Actel Pro Asic 3 FPGA Layout

The FPGA Cards sits on an 32 bit external memory interface EMIF and communicates via a 32 bit data bus and a 7 bit address bus with the DSP. One FPGA acts as a master which triggers the interrupt service routine that allows responsible for conveying the generated PWM switching signals. The FPGA cards stackable and fibre optic break out boards connect the fibre optic transmitters to the I/O ports as shown in Figure 6.27. A total of 48 fibre optics are available per FPGA card and can extended to other FPGA cards if required..

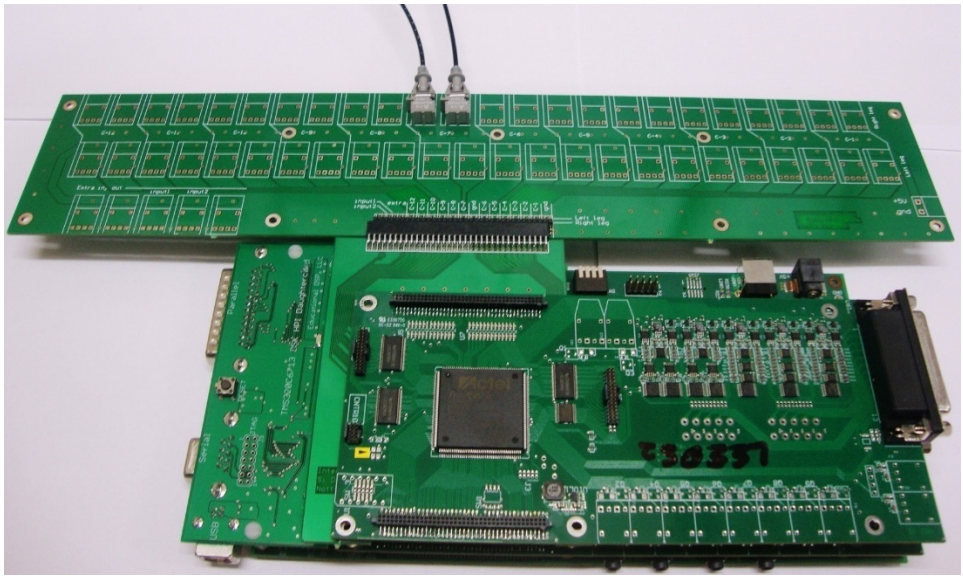


Figure 6.27: FPGA with Fibre Optic Break Out Boards

6.3.1.1 Analogue to Digital Conversion

Analogue to Digital conversion is done by the on-board Linear Technology LTC 1407-1 converters [203]. The circuit diagram is as shown in Figure 6.28. The LTC 1407-1 is a 14 bit 3Msps A/D converter capable of sampling simultaneously two differential inputs. The burden resistors on the FPGA are selected such that they convert the ± 5V measurable range at the A/D inputs into the required ± 0.3 V. The 14-bit sampled data from each differential inputs are multiplexed into a 32-bit data that is controlled by a state machine programme on the FPGA . The state machine can be set to be interrupt driven and operates such that it controls the sampling action using the set interrupt frequency of the interrupt service routine. Hence a sampling action is performed at every interrupt instant.

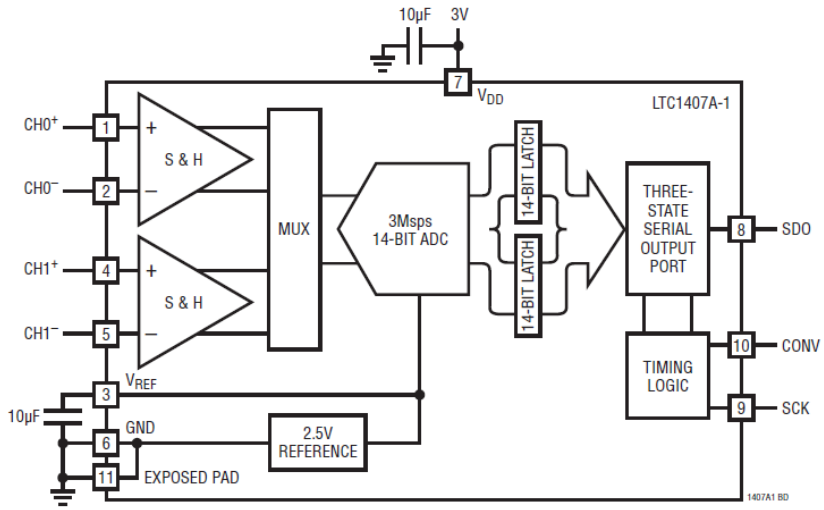


Figure 6.28: Power Circuit of ADC Converters

6.3.1.2 Interrupt Signal Generator

The interrupt signal generator is created based on a 16 bit counter in the FPGA program as seen in Figure 6.29. The counter is triggered by enable or PWM reset control signal. The PWM period set the interrupt frequency and is set by the MSB 16 bits in the Register 0 (DPR0). See Appendix E for Register Allocation. The PWM period is based on the expression in (6.6).

PWM Period = 0xFFFF – Hex (desired time – 1 clock cycle) (6.6)

where, Desired time = Clock frequency/desired frequency.

The interrupt counter can also be triggered after each next period and can be cleared by power down control action on FPGA. An interrupt frequency of 10kHz (0xEC780000) was deemed sufficient for this experiment.

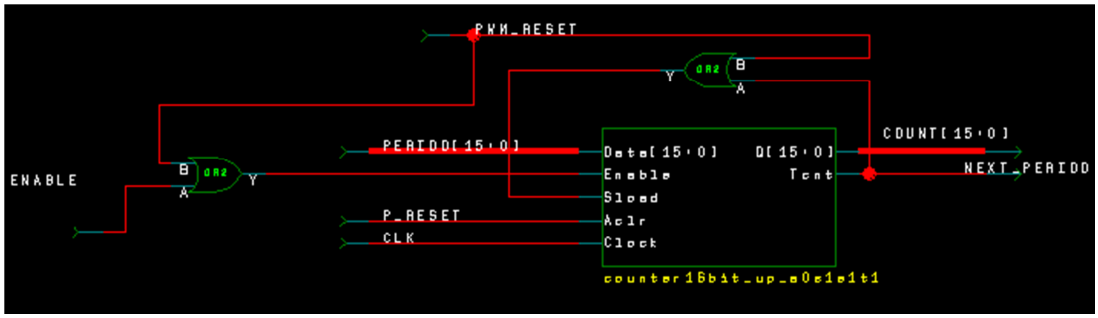


Figure 6.29: 16-bit Interrupt Counter

6.3.1.3 Modulation Unit

The modulation unit controls the generation of the phase shifted PWM signals for the IGBT switches. It consists of the carrier regeneration unit and pulse generation unit.

The carrier generation unit generates the required four triangular waveforms which are phase shifted by 45° from each other. These are translated by the clock frequency at 10 MHz following the expressions (6.7) to the get required phase initialisation integers (6.08) as shown in Figure 6.30.

$$UPLIM = \frac{f_{clk}}{2 \times f_{carr}} \tag{6.7}$$

$$INT(n) = \frac{n-1}{n_{\max}} \times UPLIM \tag{6.8}$$

where, n = number of carriers, $UPLIM$ = upper limit of carriers, f_{carr} = frequency of the carrier and f_c = clock frequency.

The lower limit INT(1) is set to be zero. The Libero View diagram showing a section of the three carrier generation units is as shown in Figure 6.31. The carrier signals are generated with 16 bit up-down counters and resets counter direction anytime it reaches its upper and lower limit.

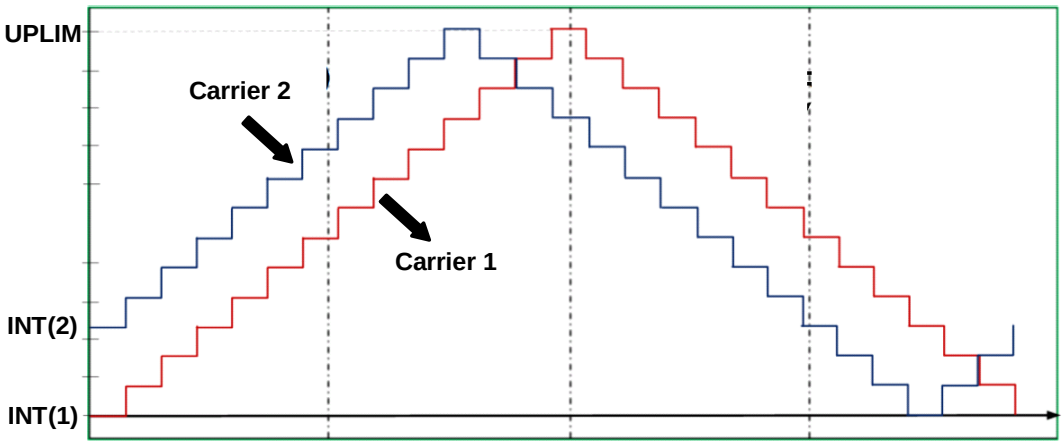


Figure 6.30: Triangular Carrier Generation

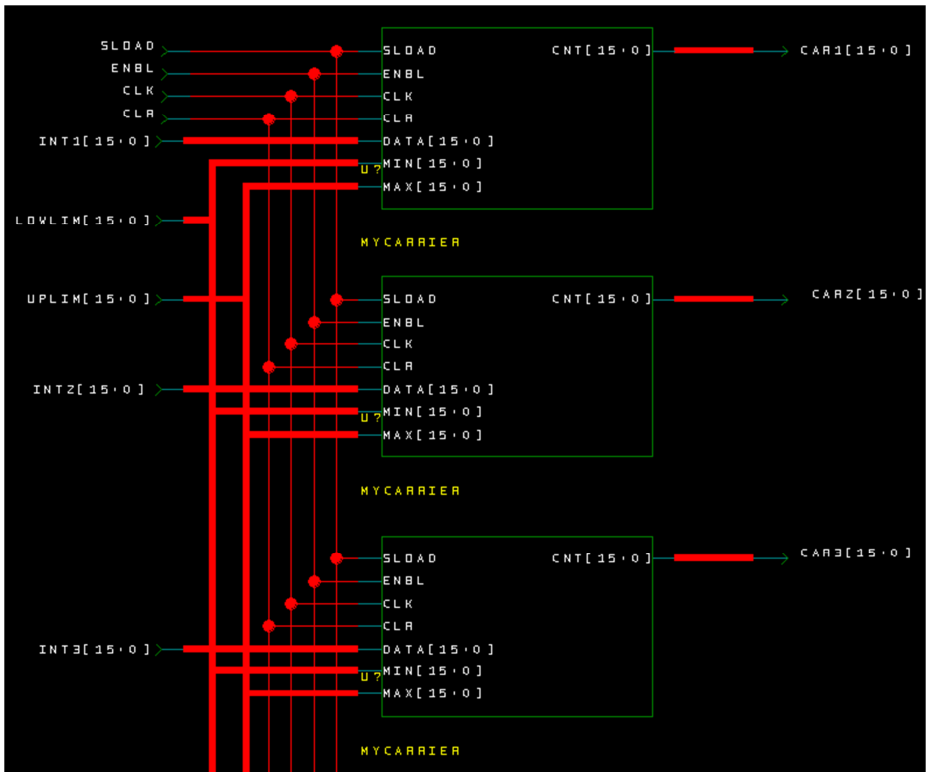


Figure 6.31: Carrier Generation Unit in FPGA

The pulse generation unit consists of a 16 bit comparator that compares the carrier signals to 16 bit sine wave modulation index reference from the DSP and generates through D-type flip-flops switching signals for each IGBT device on the cell card. The Libero View diagram showing a section of the six pulse generation units is as shown in Figure 6.32.

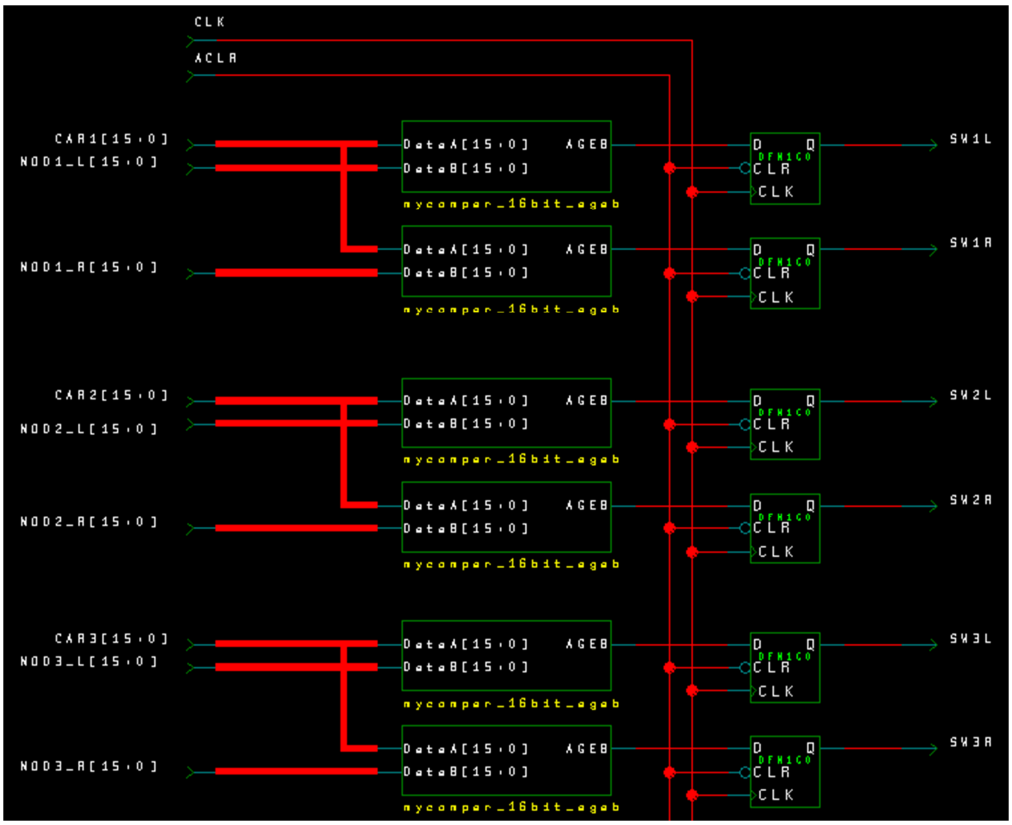


Figure 6.32: Pulse Generation unit in FPGA

6.3.1.4 Fault Trip Unit

The fault trip unit consist of a watchdog timer ensures protection of the system by monitoring the communication and creating software and hardware trips whenever there is loss in the signal. Protection is ensured by switching of the gate signals whenever a fault occurs. Hardware trips require fast processing and are set at the FPGA whilst software trips act as a backup programmed in the DSP.

6.3.2 Digital Signal Processor

The DSP is a Texas Instrument TMS320C6713 high speed floating point processor with a clock frequency of 225MHz as shown in Figure 6.33. This DSP is built on Harvard architecture and can perform eight operation per instruction which is more than enough for the chosen power application. The DSP also provides external peripheral such as the external memory interface with extended to the expansion memory port for the FPGA. There is also a Host Port Interface daughter card interface which allows to be connected to a PC. An Educational DSP LLC DSK6713HPI HPI daughter card is used and provides real time access of data variables to the external

memory whilst the DSP is in operation. The DSP serves as the main control centre and has two main functions:

1) Receiving and translating the measured A/D signals to implement power control action
2) Sending reference control signals for the carrier and pulse generation units in the FPGA as described earlier in Section 6.3.1.3.

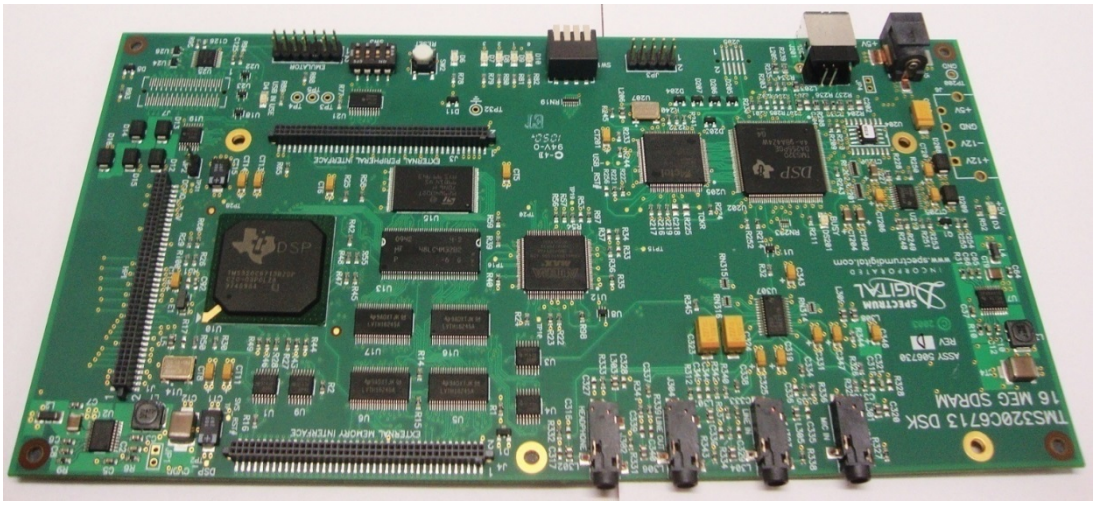


Figure 6.33: Texas Instrument TMS320C6713 DSP

6.3.2.1 Data Register Allocation

The DSP is the main control centre and acts as a Master to the FPGA. This is possible through data and control registers created using the external memory interface. Each register is a 32 bits long and the 4 MSB bits are used as address bits. They are a total of 31 data registers. A summary of the functionality of each register is as shown in the data sheet available in Appendix E. DPR0 and DPR1 are control registers for interrupt and A/D control, DPR3-DPR7 are data registers that store the A/D conversion data, DPR8 and DPR9 are control registers that handle hardware/software trips and the watchdog timer. DPR14 - DPR30 are data registers that contain the data to be sent to the FPGA for the PWM switching.

6.3.2.2 Calibration

To have acceptable control signals to implement control actions all signals from the A/D converters are calibrated and converted back to their original form in the DSP using the expressions (6.09) –(6.11).

$$S_{norm} = \left(S - S_{mid}\right) / S_{mid} \tag{6.09}$$

$$S_{mid} = \left(S_{pk-pk} / 2\right) - S_{pk} \tag{6.10}$$

$$S_{actual} = S_{norm} \times C_f \tag{6.11}$$

where, S is the16 bit signal from the A/D converter register, S_{mid} is the midpoint or zero level and gets rid of offsets produced by the transducers, S_{norm} is the normalised signal and C_f the conversion factor of the transducers.

6.3.2.3 Program Overview

A flow chart in Figure 6.34 shows the main and sub program routines of how the software program is set up. The main routine is mainly an initialisation routine that sets all the initial control variables and sets the external memory interface for use. The control main routine consist of two sub routines

1) FPGA initialisation sub-routine: This routine resets the FPGA to its default state by clearing the all counters and sets up the external interrupt service routine. Next, the watchdog timer is enabled and the PWM dead time set and finally the initial values for the triangular carriers are allocated to their respective registers. This routine then remains in an idle state waiting for the external interrupt to be triggered.
2) PWM sub-routine: This is the interrupt service routine which occurs when an external interrupt is triggered from the FPGA. This routine reads all the A/D signals and performs control actions to sine wave modulation index references which are sent back to the FPGA.

Detailed flow charts of the sub-routine program flow are shown.

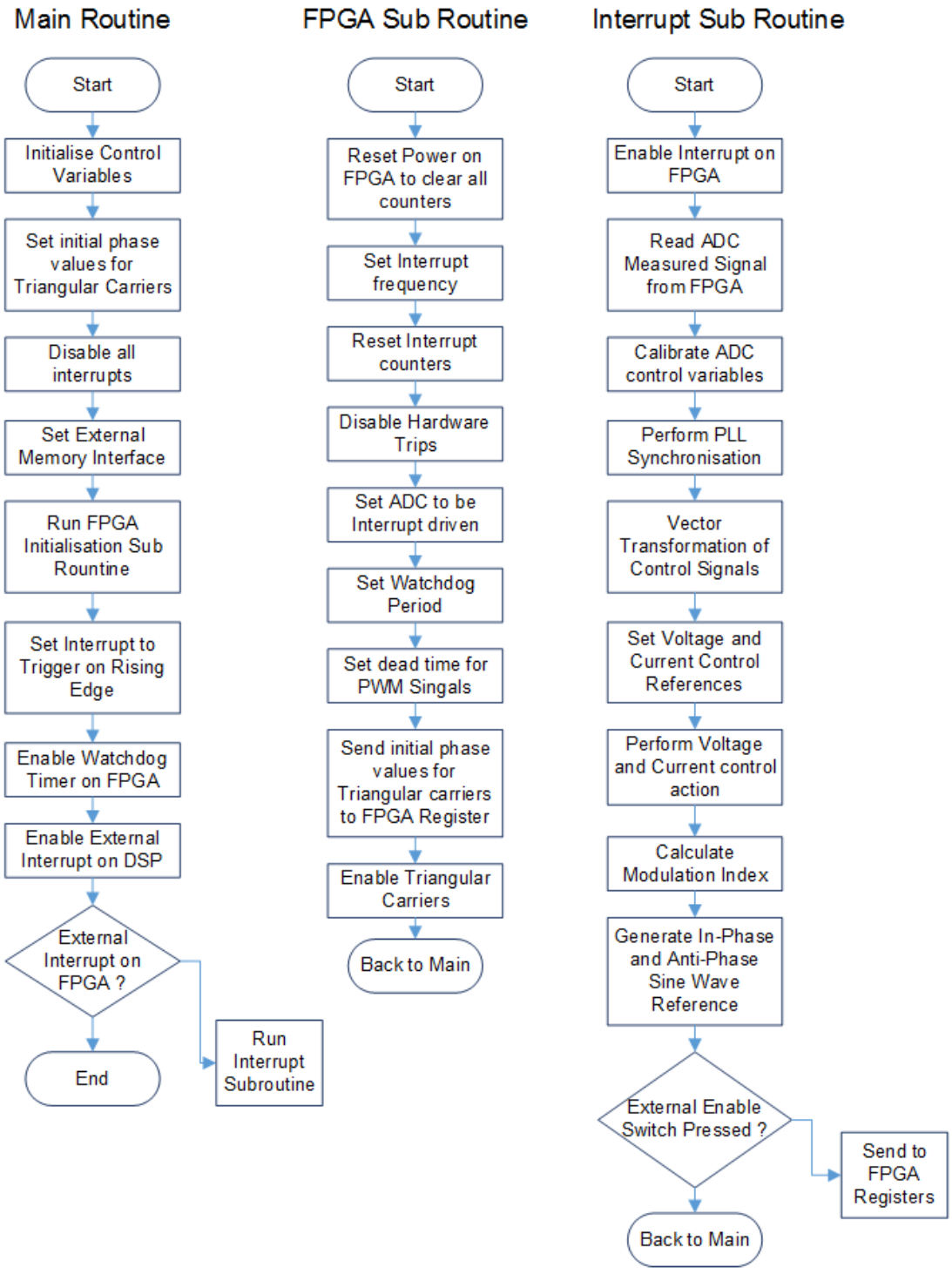


Figure 6.34: Program Flow Chart for Main Routine and Sub Routine

6.4 Conclusions

This chapter has presented the constructed MMC-FC–based STATCOM in detail, including the converter itself, hardware devices and software for data acquisition and control function implementation. The modular structure of the MMC-FC has been the main focus, and its construction, being essentially a collection of 24 power cell cards connected in a specified form, has been described. The circuit diagram of each of these cards was given and the flexibility in using them to scale up a converter for higher voltage operations or building a different converter has been illustrated. Another feature lies in the insertion of fibre optic transmitter-receivers and optical cables in the IGBT gate drive circuit. This provides higher electrical isolation and creepage distance, eliminating the usual retriggering problems of using opto-couplers and noise interference. In addition the chapter presented in detail all the facilities necessary for the FC-MMC to perform the control functions of a STATCOM, including measurement and data acquisition hardware designed and built by the author, DSP-FPGA devices and the software driving them.

Chapter 7
Experimental Validation

The built prototype STATCOM presented in the previous chapter requires to be applied to controlling a practical power system so that its entire structure can be validated and its operational performance can be evaluated. To carry out this task an emulation of a representative power distribution system is required which should consist of an input feeding source supplying a variable inductive load through a lumped equivalent model of a three – phase transmission line. The prototype STATCOM should be connected at the load end for controlling load reactive power. In addition the network should be made to allow flexible variation of its parameters so that the performance of the STATCOM under different operating conditions can be assessed and compared.

This chapter presents experimental tests of the prototype STATCOM when functioning as a reactive power controller. It starts by presenting the design and construction of a scaled down power distribution system; the ratings and component parameters for this network are set according to those used in Chapter 5. Subsequently the digital implementations of the voltage and current control schemes and the phase locking algorithm for the STATCOM are described. Experimental tests are then performed for two configurations of the converter:

- Sub-module voltages maintained by DC voltage supplies,
- Sub-module voltages maintained by DC Voltage closed loop control.

The results of these tests are presented and discussed in the chapter.

7.1 Power System Configuration

The modelled power network designed for testing the STATCOM's capability for reactive power compensation is set to imitate a single feeder bus point of a three-phase distribution network. Figure 7.1 shows the circuit diagram of the constructed power system. This is categorised into three main power subsystems:

- The PCC side subsystem which consists of an existing 110V 3-phase laboratory supply connected with 1:2 step-up auto transformer and a transmission line reactance.

- The load side subsystem which is set to represent reactive power load consumption within the network and consists of a resistive-inductive network modelled using 20Ω, 5A rheostats and 42mH, 5A inductors to realise maximum 0.86 power factor.
- The converter side subsystem which consists of the built test prototype 5-level Modular Multilevel Converter consisting of 3-level based FC sub-modules coupled together at the point of common coupling through a resistive-inductive filter network modelled to represent a simplified model of a converter transformer.

Table 7.1 summaries the power ratings of the system. The experimental setup is as shown in Figure 7.2.

Table 7.1: Power System Characteristics

Rating	Value
PCC Side	3.3 kVA (110V, 10A)
Distribution Line	Aluminium PI TX line (d= 10mm, s= 1m, l=1 km) L =2mH, R = 0.5 Ω, X= 1.57 Ω
Load Side	1.65 kVA (110V, 5A) Load: 22 Ω, 42mH Power factor = 0.86 lagging
Converter Side	3 kVA (200V, 5A) Filter: 10 Ω, 10mH DC Capacitor rating (per module): 100V, 1.12mF Module Flying Capacitor: 50V, 0.56mH
Switching frequency	750 Hz

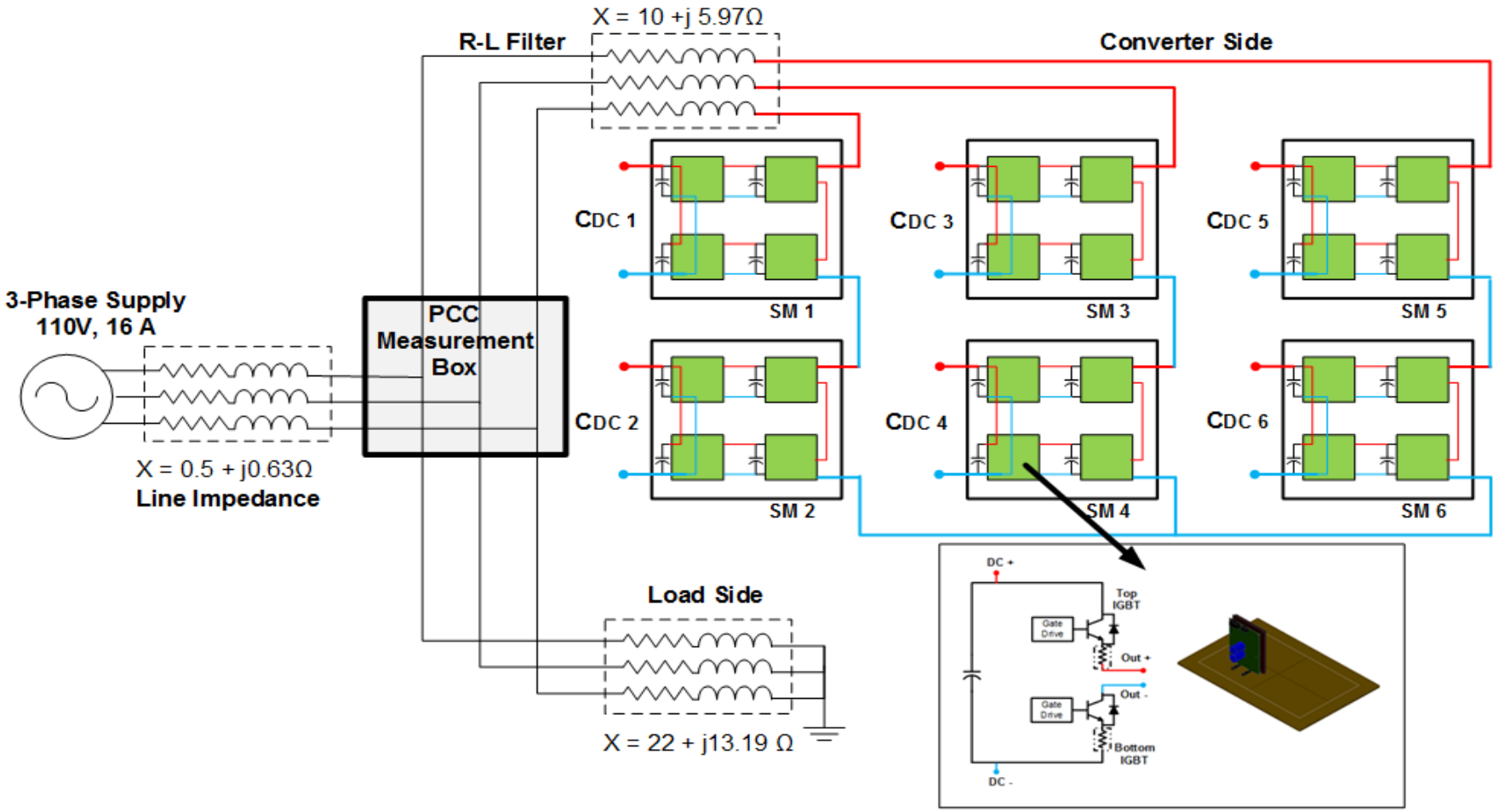


Figure 7.1: Experimental Power System Configuration

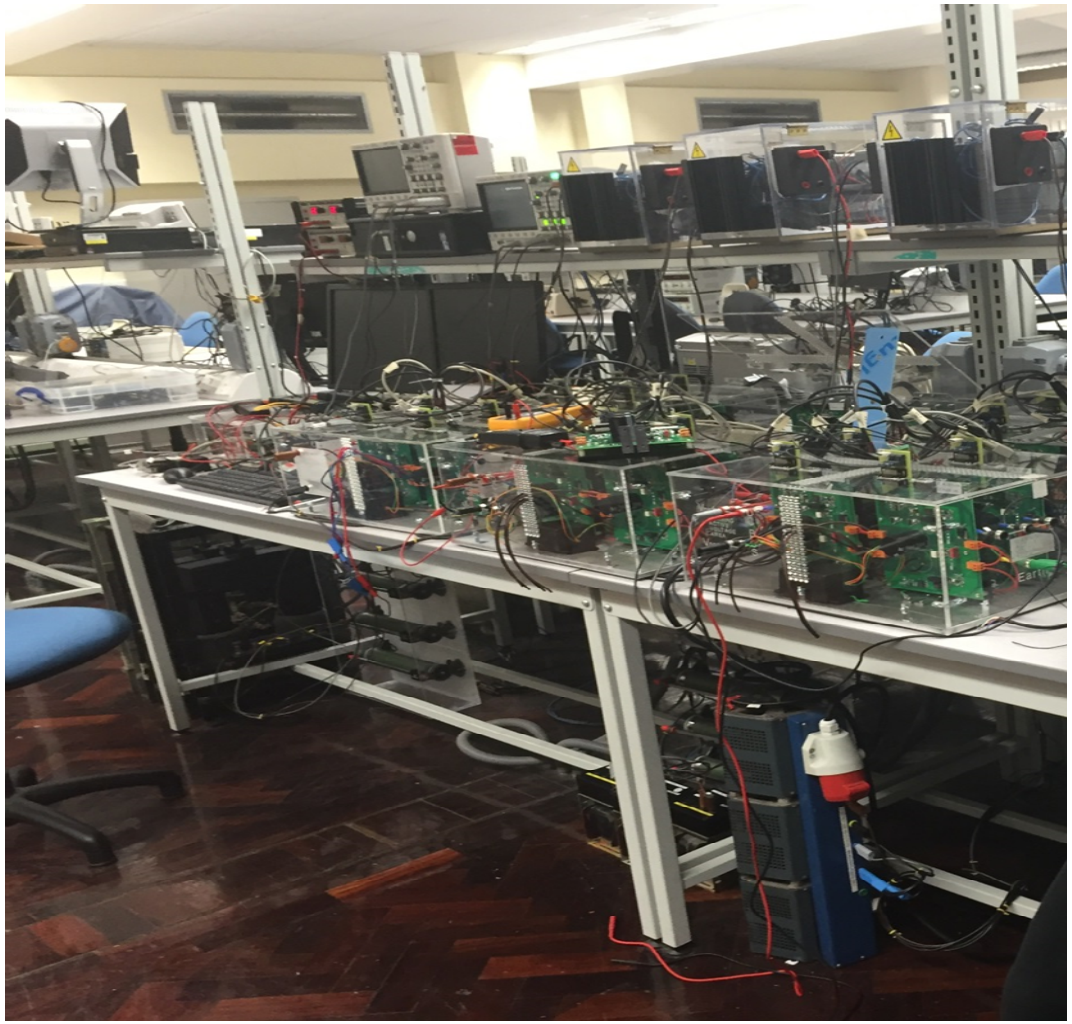


Figure 7.2: Experimental Setup

7.2 Control System Implementation

Implementation of the control system is based on the built converter and is designed to enable it to perform reactive power compensation at the load end. The system is tested for unity power factor correction and the load side is modelled to imitate the same compensation requirements described in Chapter 5. The software control is as described earlier in Section 6.3.1.1. During each interrupt loop the calibrated three-phase voltage and current control signals are transformed by vector control into two- dimensional stationary and synchronous reference frames. The control system was then checked for safe operation using the software trips before grid voltage synchronisation is implemented. Figure 7.3 shows a block diagram of the experimental control system. The converter current and voltage controls are based on the discretised proportional and integral control algorithm to be described in the subsequent sections and implements closed loop current control under the two converter configurations.

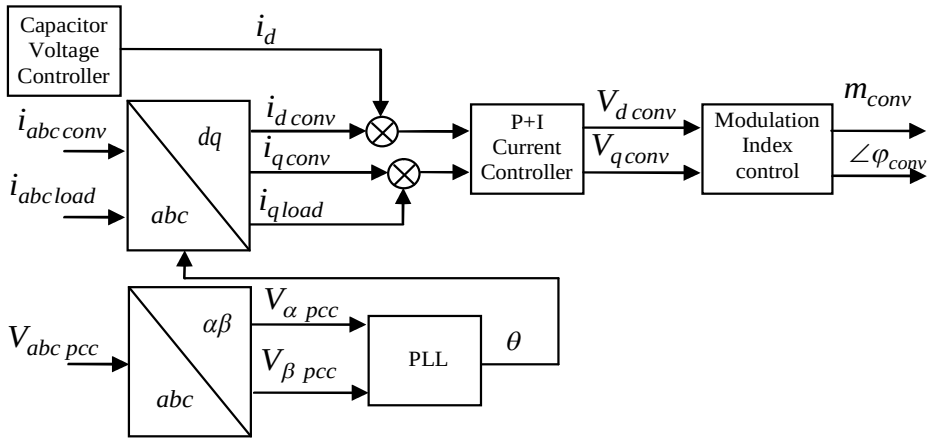


Figure 7.3: Block Diagram of the Control System

7.2.1 Grid Synchronisation

As discussed earlier in Chapter 4, the choice of grid voltage synchronisation is mainly based on the grid voltage requirements and various advanced schemes can be implemented. The system under study is a balanced system with equal three phase voltages and the α-β synchronisation scheme was chosen for practical implementation. This was based on it being most effective for balanced system with less requirement of no feedback compared to the conventional synchronous reference frame SRF scheme. The energy operator scheme introduced and implemented in Chapter 4 was

considered but not used because a further signal processing study was required to design a suitable band pass digital filter that would enable its operation at 10 kHz interrupt frequency. Figure 7.4 shows the results for initial test for grid synchronisation. The converter voltage at 250Hz switching frequency is shown to follow the ac voltage at the PCC.

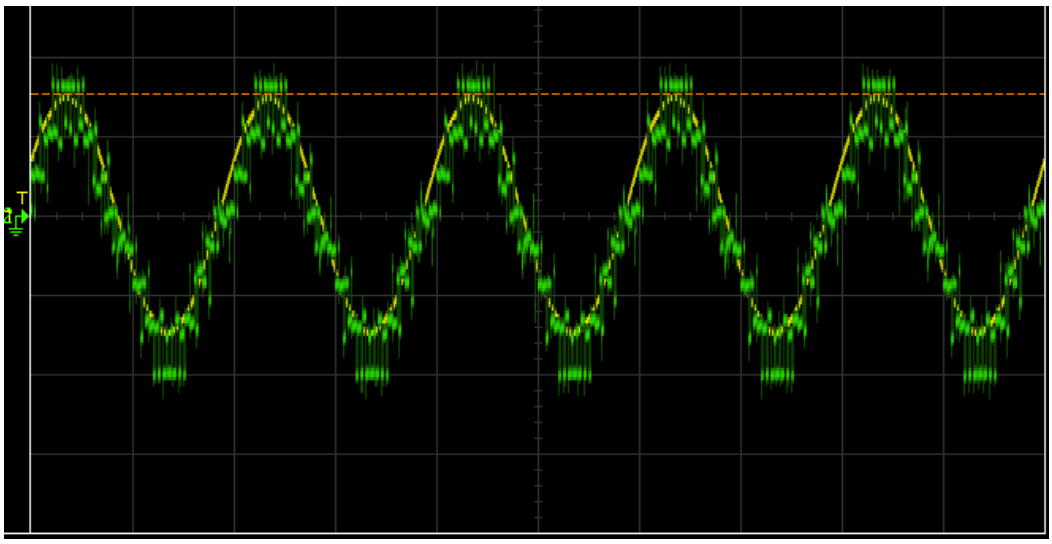


Figure 7.4: Synchronised Voltage (One Phase)

7.2.2 Discrete PI Control

Proportional and integral controls are used to control the converter current $d-q$ vectors to follow the required control references. Figure 7.5 shows the block diagram for a proportional integral controller. In order to implement the proportional integral control during the interrupt routine, a discretised version for the P+I control is required and is derived by using the backward difference of discrete samples based on the following expressions (6.12) – (6.15).

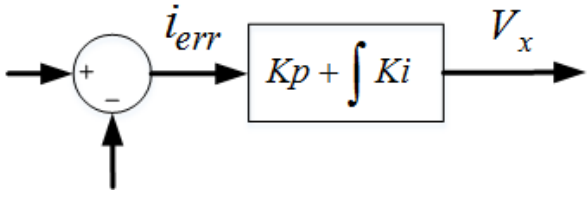


Figure 7.5: Block Diagram P+I Controller

$$V_x = \left(k_p \times i_{err} \right) + \left(k_i \times \int i_{err} \right) \qquad (6.12)$$

Then taking the second derivative using backward difference the expression in (6.12) can be expressed as

$$\frac{d}{dt}V_x = \left(k_p \times \frac{d}{dt} i_{err} \right) + \left(k_i \times \frac{d}{dt} \int i_{err} \right)$$

$$\frac{V_x - V_{x\,prev}}{T_s} = \left(k_p \times \frac{i_{err} - i_{err\,prev}}{T_s} \right) + \left(k_i \times i_{err} \right) \qquad (6.13)$$

The discrete model of the controller can be made more accurate by taking the moving average of the backward difference of the error, such that $i_{errr} = \left(\frac{i_{err} + i_{err\,prev}}{2} \right)$. Hence (6.13) can be expressed as

$$V_x = k_p \times \left(i_{err} - i_{err\,prev} \right) + \left(k_i T_s \times \frac{i_{err} + i_{err\,prev}}{2} \right) + V_{x\,prev} \qquad (6.14)$$

$$V_x = \left(\frac{k_i T_s}{2} + k_p \right) \times i_{err} + \left(\frac{k_i T_s}{2} - k_p \right) \times i_{err\,prev} + V_{x\,prev} \qquad (6.15)$$

where V_x is either the d or q vector element of the voltage, i_{err} is the P+I controller current error, k_p is the proportional gain, k_i is the integral gain and T_s the sampling or interrupt period.

The discrete model of proportional-integral controller is applied for control actions within the inner current controller and outer dc capacitor voltage controller.

7.2.3 Capacitor Pre-Charge Control

The $i_{d\,conv}$, $i_{q\,conv}$ components of the current are representatives of the active and reactive power generated or absorbed by the converter respectively. The capacitor pre-charge control is possible by controlling the converters i_{dconv} component whilst setting $i_{q\,conv}$ to be zero. This allows for active power to be absorbed by the converter which in then charges up the voltage of the outer capacitor. Figure 7.6 shows the block diagram for the pre-charge control. The voltage is restrained to be charged up to the set pre-fined level by controlling V_{dcref} in the DC bus controller. This generates the required reference i_{dref} active current that maintains the voltages at the capacitor to be balanced.

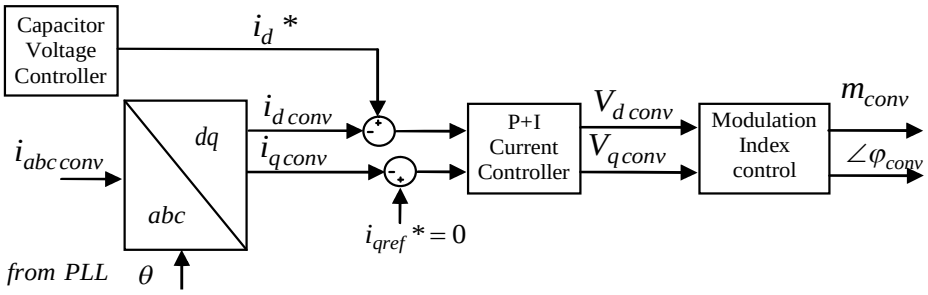


Figure 7.6: Block Diagram for Pre-Charge Control

7.3 Results and Discussion

The system shown in Figure 7.1 has been set for reactive power compensation at the PCC bus point of a three-phase distribution network The focus is to compensate for the power factor due to load side inductive impedance. Two different cases are studied; one having each sub-module powered by a DC power supply so that DC-bus voltage is kept constant. The other having the sub- modules DC bus voltages maintained by the capacitors hence capacitor voltage control is performed. The converter switching frequency is set at 750Hz.

The test scenarios are the same for both studies. An inductive load is connected at the load side to absorb a maximum reactive power of 1.2 kVAR. Within the first 1s of operation, the converter is controlled to act in its pre-charge mode until steady state and the voltages of the outer capacitors charged up to the required voltage. At time durations 1s ≤ t< 3s, 3s ≤ t < 5s and 5s ≤t< 7s the converter is set to compensate at lower and maximum loading conditions at 50%, 75% and 100% respectively.

7.3.1 Sub-module Voltages maintained by DC Power Supply

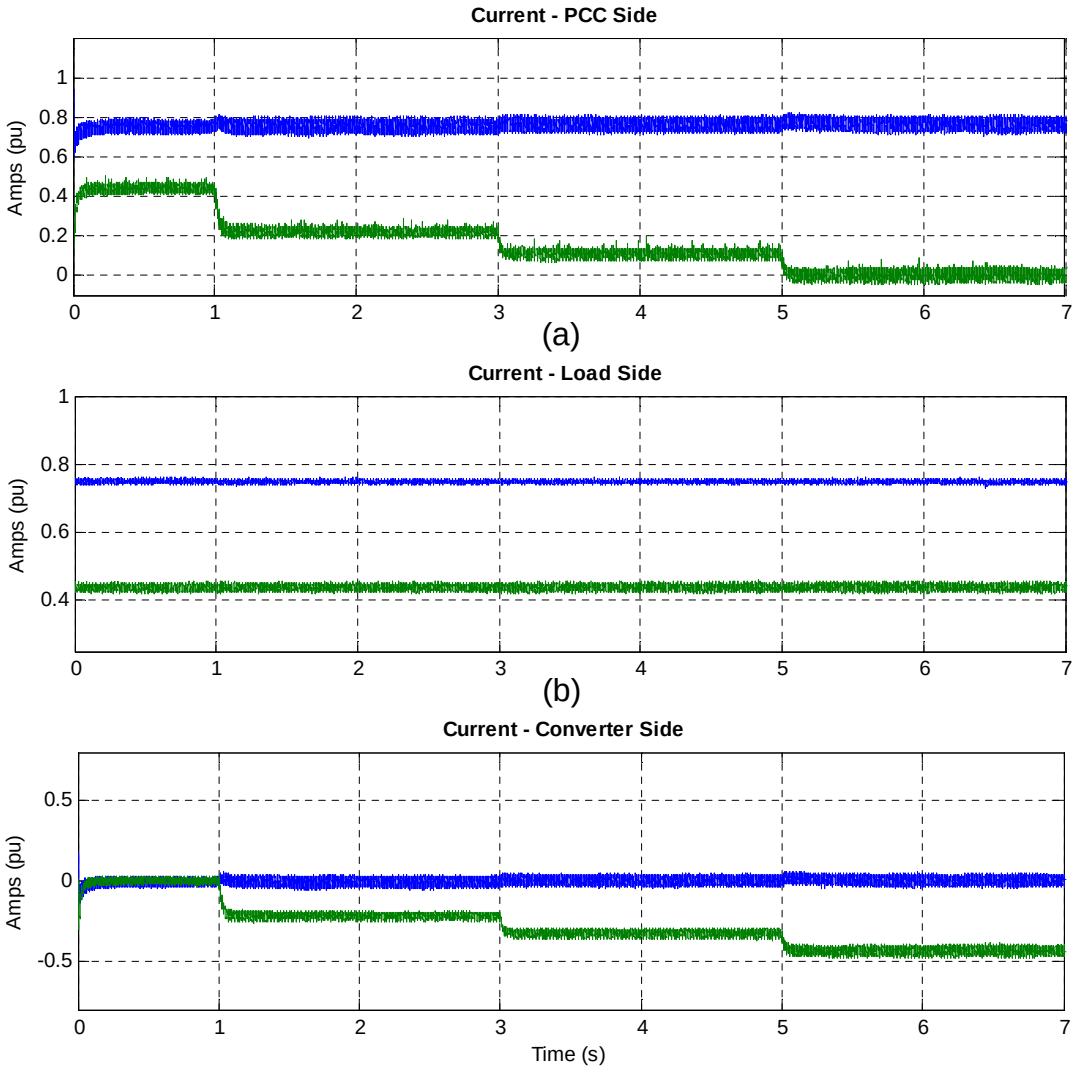
The experimental parameters are the same that listed in the Table 7.1 and conform to the simulation study in Section 6. Proportional and integral control gains for the current controllers are set to 0.09 and 20 respectively.

7.3.1.1 Vector Control Signals

Figure 7.7 (a)-(c) show the active d and reactive q current components for current and the PCC, Load and Converter sides. All currents are also normalised to per unit values by dividing by their respective base value of 5A.

Within the time interval 0s < t ≤ 1s, corresponds to the no compensation mode. The PCC reactive current vector $i_{q\ pcc}$ corresponds to the maximum inductive load at the load side $i_{q\,l}$ consuming a reactive current of 2.2 A (0.44 pu). The converter current vectors i_{dconv} and i_{qconv} are shown to be controlled effectively at zero showing no compensation.

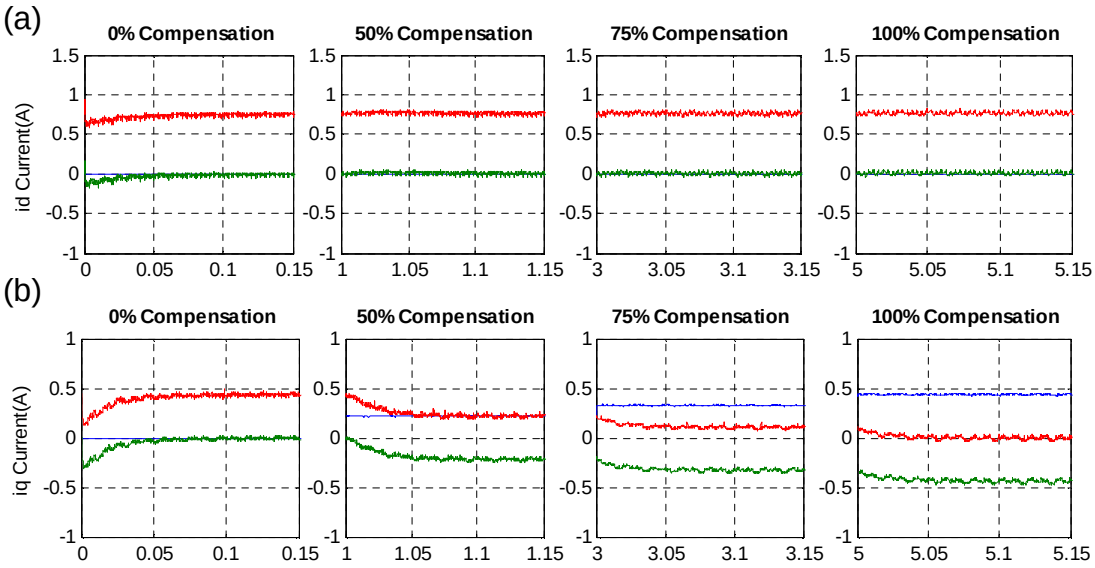
At time intervals 1s <t ≤ 3s, 3s <t ≤ 5s and 5s <t ≤ 7s, the result shows the converter operating in its 50%, 75% and full compensation mode respectively. The reactive current vector $i_{q\ pcc}$ is seen reducing to be approaching full compensation mode as expected, with a reactive current of 1.1A, 0.55A, 0A (i.e. 0.22 pu, 0.11 pu, 0 pu) for the 50%, 75% and full compensation mode respectively. The i_{dconv} active current component is shown to be at constant zero as set in the controller, resulting in no change to active current vector $i_{d\ pcc}$ of 3.8 A (0.76 pu) at the PCC.



Blue – Active Current Compenent, Green – Reactive Current Component

Figure 7.7: d-q current responses under STATCOM Control (a) PCC Side, (b) Load Side, (c) Converter Side

Figures 7.8 (a)-(b) show the system currents of the STATCOM and their corresponding reference set points at 0% 50%, 75% and 100% compensation. It shows clearly that the i_q current at the PCC starts reducing once the converter starts compensation. Based on controller parameters, the response time of 50ms is shown and considered to be fast. This is the same for all conditions. The i_{dconv} is set to be zero throughout since DC power supplies are used for the sub-modules and the d-component of the converters current as shown follows promptly

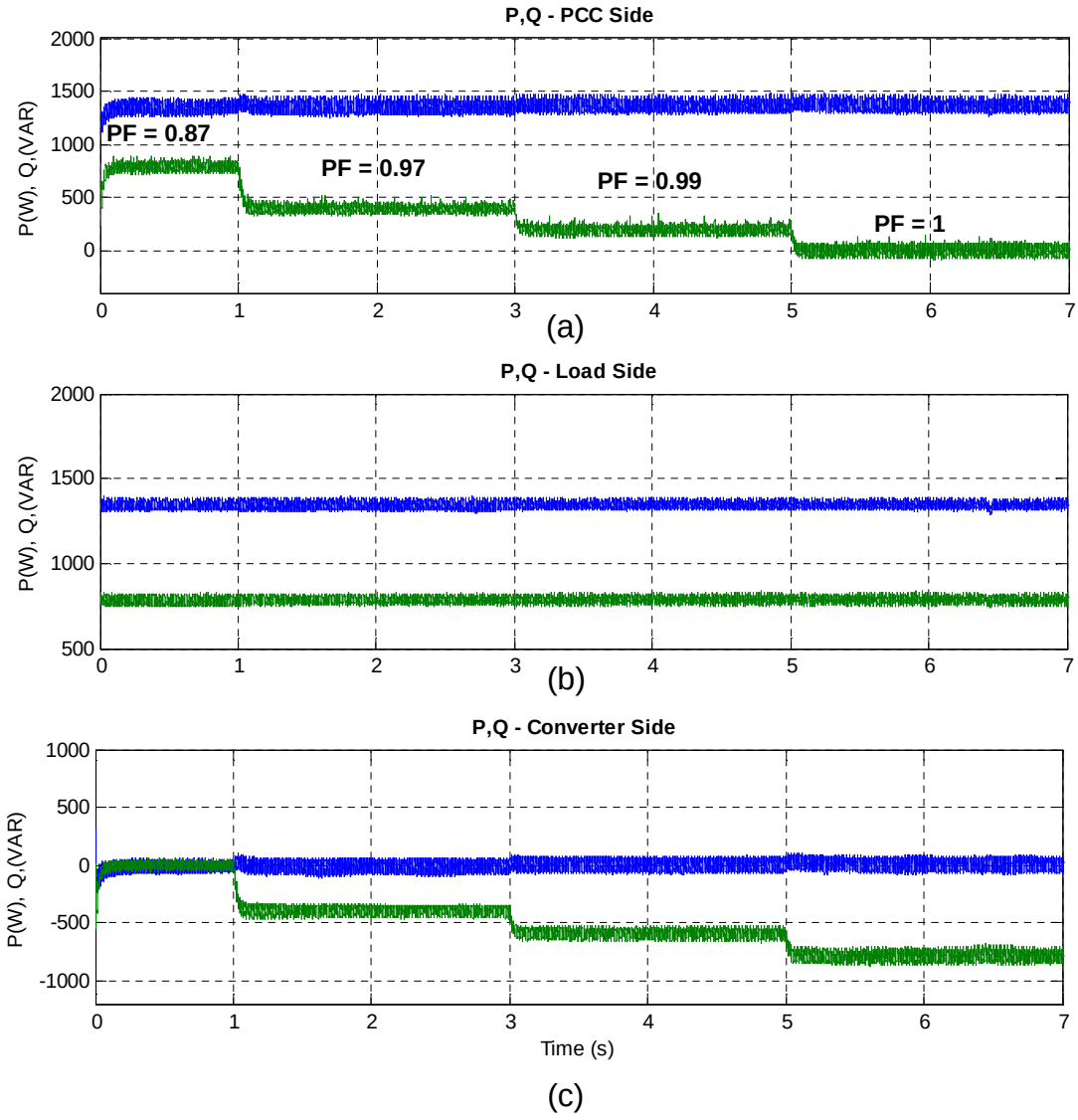


Blue – Current Reference, Green – Converter Current, Red – PCC Current

Figure 7.8: Response time of STATCOM current under each load condition Signals, (a) id current, (b) iq current

7.3.1.2 Active and Reactive Power

Figures 7.9 (a)-(c) show the active and reactive power at the PCC, Load and Converter side respectively. The maximum reactive power absorbed by the load side is 800 VAR and with STATCOM control, the power factor at the PCC is moving towards 100% compensation. The generated reactive power is -400 VAR, -600 VAR, and -800 VAR corresponding to the 50%, 75% and 100% compensation respectively. The active power is shown to be the same at 1.35 kW as expected as the controller is set to only generate reactive power to the load. The response time is shown to be fast at 50ms.



Blue – Active Power, Green – Reactive Power

Figure 7.9: Active and Reactive Power Responses, (a) PCC Side, (b) Load Side, (c) Converter Side

7.3.1.3 PCC Side Waveforms

Figures 7.10 (a)-(d) show the per unit values of three-phase voltages and current, current magnitude and power factor angle at the different load conditions.

The PCC current magnitude is shown to be decreasing, depicting a elimination of the $i_{q\ pcc}$ component. Within the first three cycles of each mode of operation, the PCC side currents per unit magnitude and power

factor angle are shown to be $0.88\angle 30.07^{\circ}$, $0.79\angle 16.14^{\circ}$, $0.77\angle 8.24^{\circ}$, $0.76\angle 0^{\circ}$ corresponding to actual current values of $4.4A\angle 30.07^{\circ}$, $3.95A\angle 16.14^{\circ}$, $3.85A\angle 8.24^{\circ}$, $3.80A\angle 0^{\circ}$ for the 0%, 50%, 75% and full compensation mode respectively. 100% compensation is achieved within time interval 5s <t ≤ 7s with power factor angle equals zero.

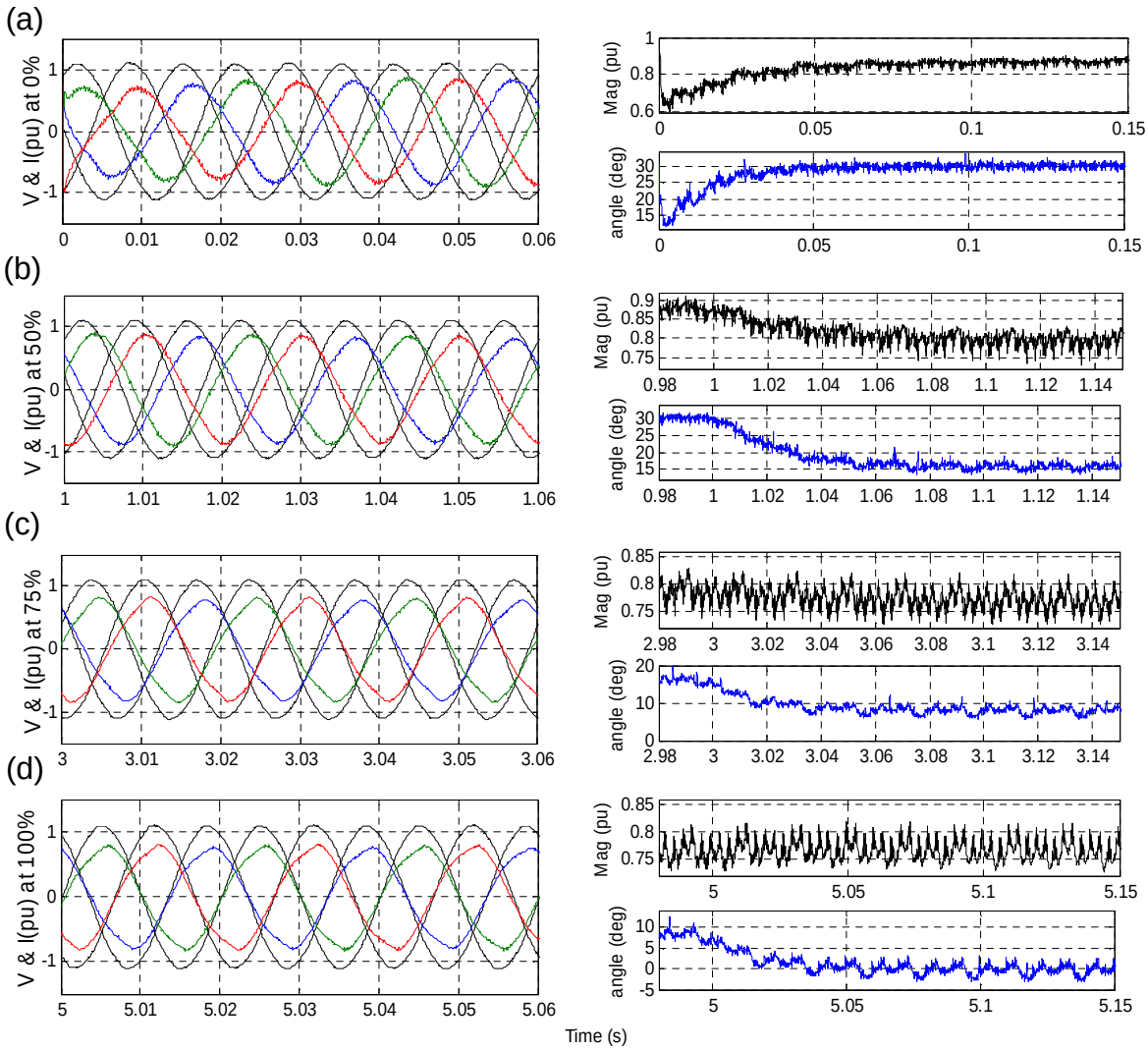


Figure 7.10: Voltage, Current and Power Factor Angle, (a) Zero compensation, (b) 50% compensation, (c) 75% compensation, (d) Full compensation

7.3.1.4 Converter Side Waveforms

Figure 7.11 (a)-(d) shows the three-phase voltages and current, active and reactive power at different load conditions.

The converter current magnitude is shown to be increasing at +90^{o} phase angle, depicting purely capacitive current generation at PCC. Within the first three cycles of each mode of operation, the converter side currents per unit magnitude and power factor angle are shown to be $0.22\angle 90^{\circ}$, $0.33\angle 90^{\circ}$, $0.44\angle 90^{\circ}$ corresponding to actual current values of $1.1A\angle 90^{\circ}$, $1.65A\angle 90^{\circ}$, $2.2A\angle 90^{\circ}$, for the 50%, 75% and full compensation mode respectively.

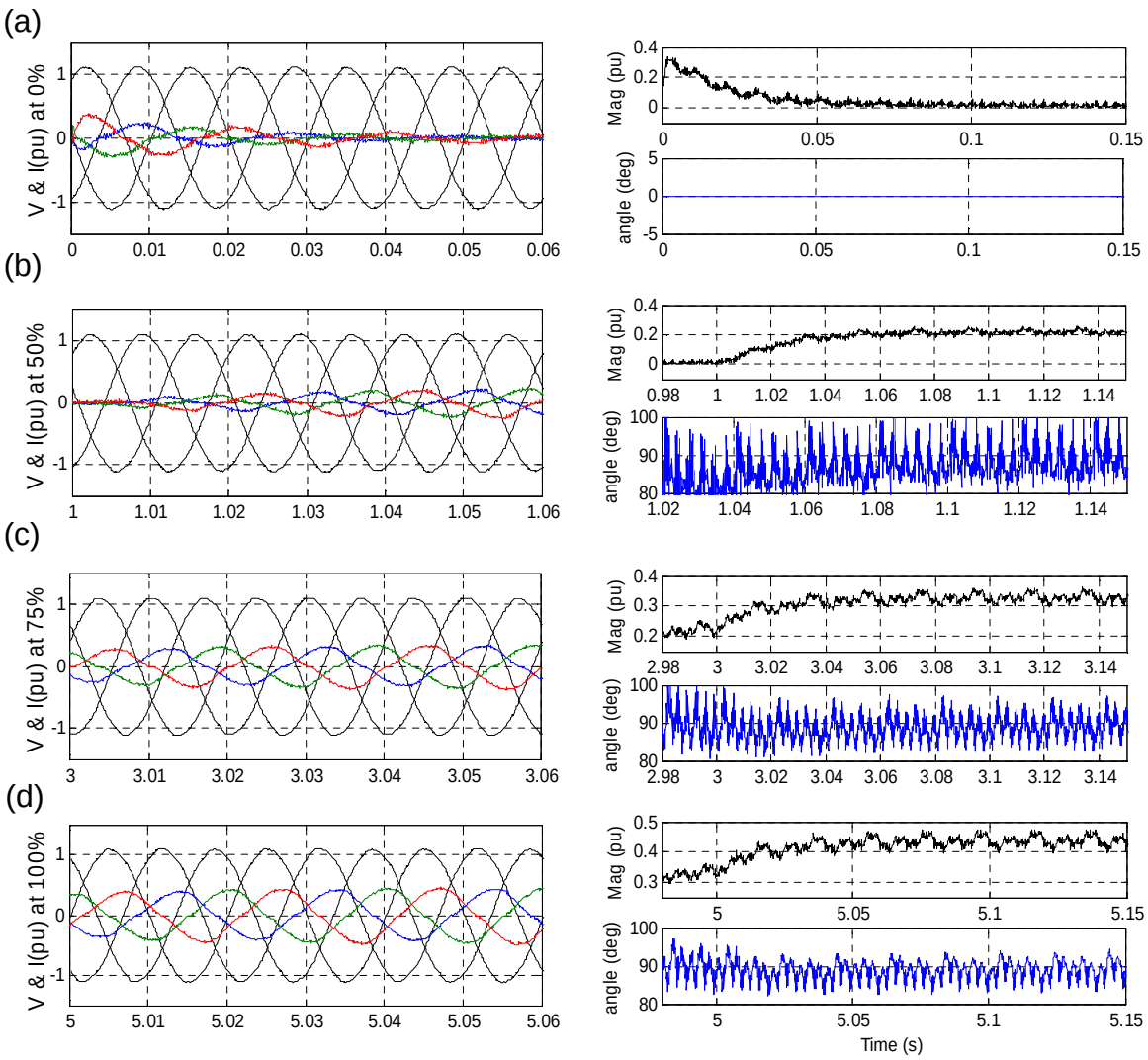


Figure 7.11: Voltage, Current and Converter Angle, (a) Zero compensation, (b) 50% compensation, (c) 75% compensation, (d) Full compensation

Figure 7.12 (a)-(c) shows the converter voltage modulation index, synchronisation angle and converters three-phase voltage waveform.

The modulation index is shown to be increasing at each mode of operation. At the start, 0 <t ≤ 1, the converter modulation index is at 0.69 with angle of

0.07 rads in the positive direction. This is due to the fact that the converter adjusts to meet the filter requirements as there is no active or reactive power generation. At time intervals 1 <t ≤ 3, 3 <t ≤5 and 5 <t ≤ 7 , the converter adjusts to meet the current demand and has modulation index and converters angles of $0.77\angle -0.11$ rads, $0.83\angle 0.16$ rads and $0.9\angle 0.20^{\circ}$ rads.

Figure 7.12 (c) shows synchronisation been achieved with phase locked loop clocking at each fundamental cycle and Figure 7.12 (d) shows the 5 level converter output voltage at full compensation mode.

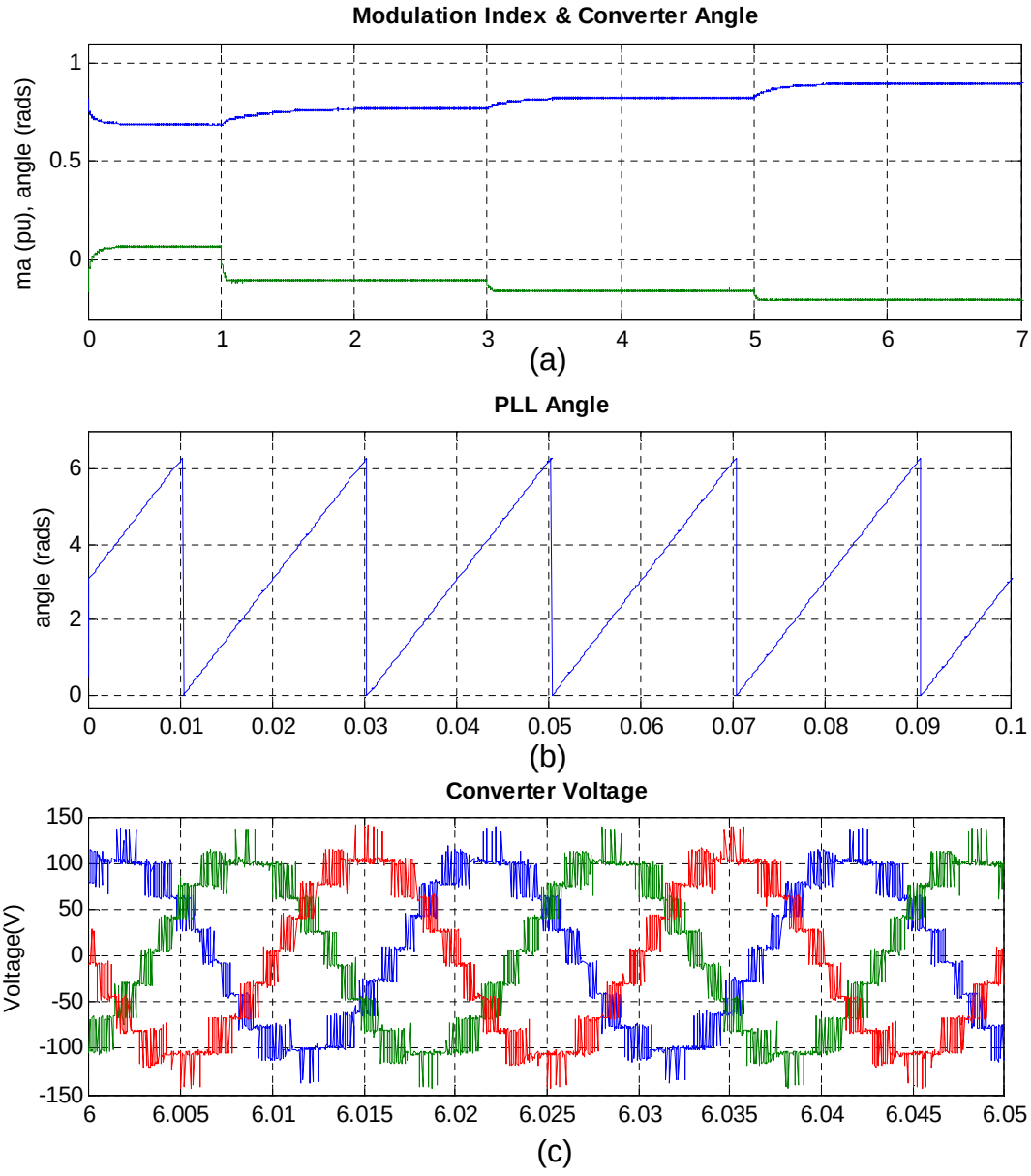


Figure 7.12: (a)Converter Modulation Index and Angle, (b) PLL Angle, (c) Converter Voltages Full Compensation

7.3.1.5 Capacitor Balancing

Figures 7.13 (a)-(f) show the outer capacitor voltage waveforms.

The outer capacitor voltages are shown to be decreasing at each mode of operation This is a result of the voltage of the DC power supply used being unregulated. There is total internal impedance of is 5.3Ω in the path. This implies that an increase in the converter current corresponds to an increased voltage drop across the outer capacitors, in this case the voltage varies from 5.83V to 8.75V and 11.66 V at 50%,70% and 100% compensation respectively. The outer capacitors voltages at each of the phases are also shown to be balanced properly in the steady state.

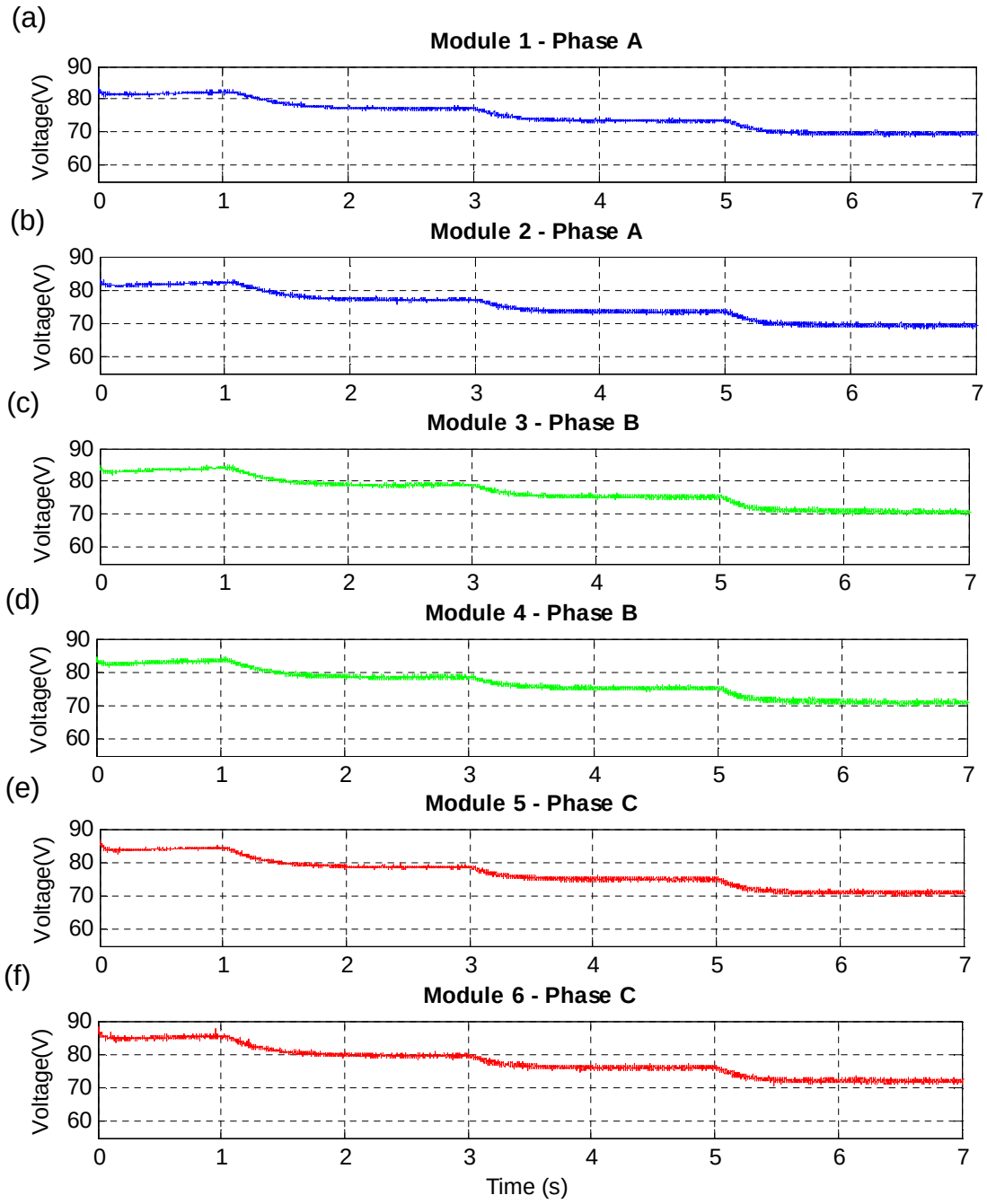
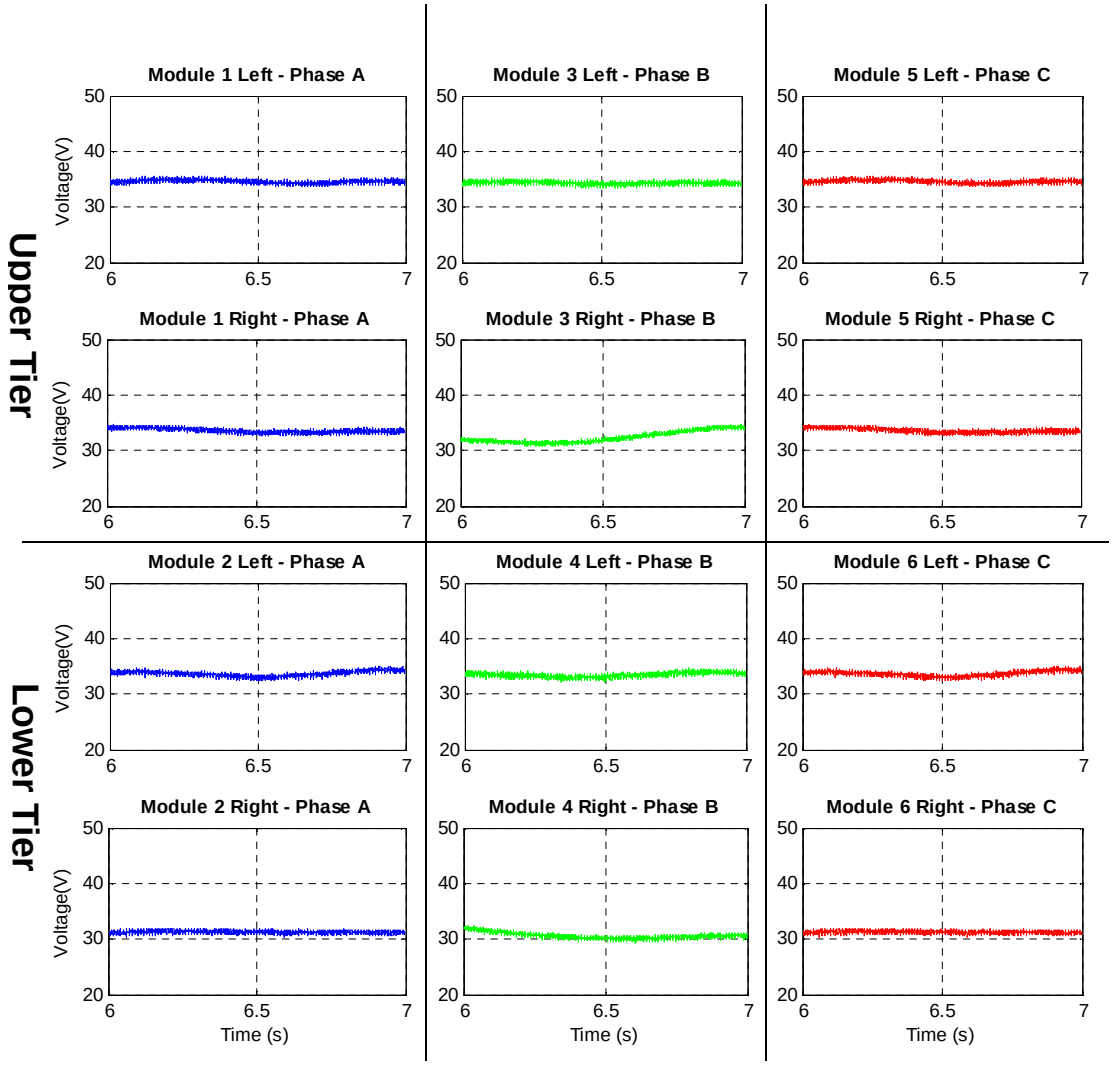


Figure 7.13: Outer Capacitor Voltages

Figures 7.14 (a)-(c) show 10 cycle representation of the inner capacitor voltage waveforms at full compensation mode.

The inner capacitor voltages are shown in Fig 7.14 to balance properly around 35 V which corresponds to half of the outer capacitor DC voltage of 70 V. As discussed earlier in Chapter 3 due to natural balancing of the PS-PWM technique, based on the modulation index, the duty ratio of certain phases like Phase C tend to drift slightly away from the expected nominal voltage at 35V.



(a) (b) (c)

Figure 7.14: Inner Capacitor Voltages

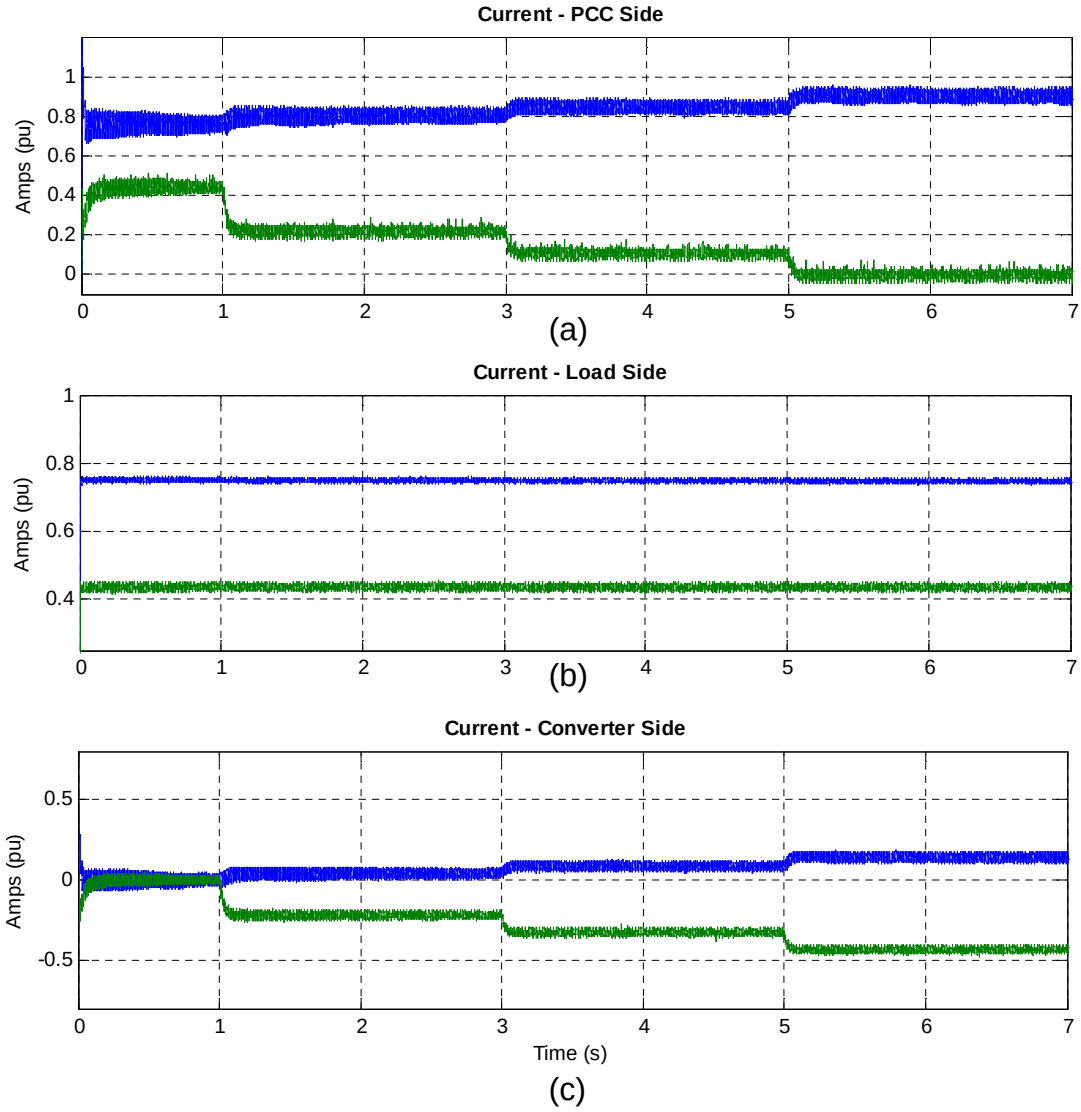
7.3.2 Sub-module Voltages maintained by DC Voltage Control

In this scenario, closed loop feedback control is implemented to effectively control voltages of the outer capacitors. Proportional and integrals control gains for the current and DC voltage controllers are set to 0.09, 20 and 5, 10 respectively

7.3.2.1 Vector Control Signals

Figures 7.15 (a)-(c) show the active and reactive current at the PCC, Load and Converter sides.

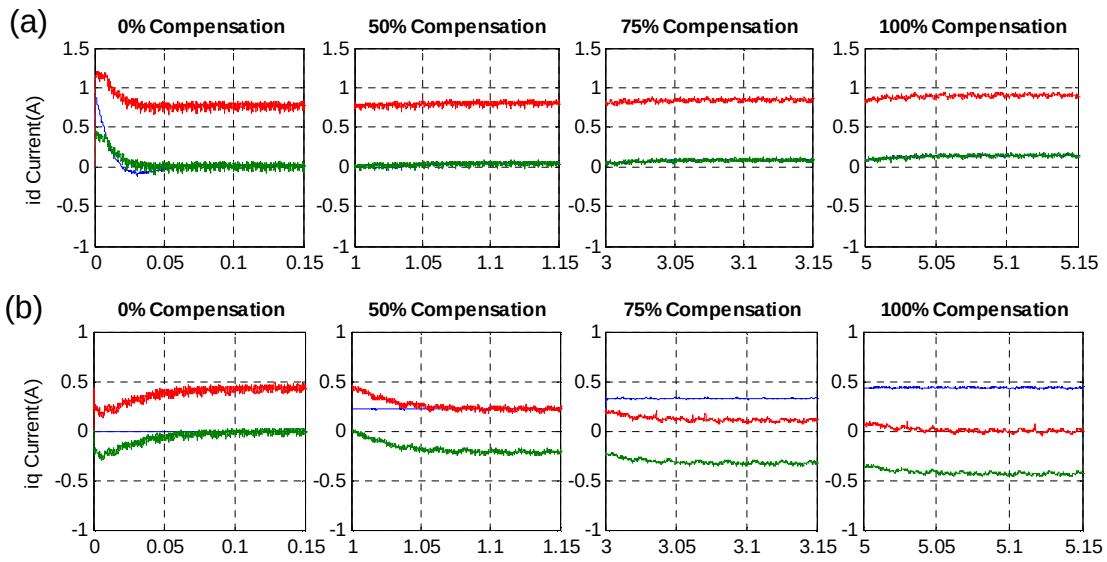
At time intervals 1s <t ≤ 3s, 3s <t ≤ 5s and 5s <t ≤ 7s, shows the converter operating at its 50%, 75% and 100% compensation mode respectively. It can be seen that the reactive current at PCC is reducing steadily as expected from 1.1A (0.22 pu) to 0.55A (0.11pu), then to 0A corresponding to 50%, 75% and 100% compensation modes. On the load side the reactive current is maintained constant. Meanwhile the converter side reactive current magnitude increases from 0A to 0.55A and 1.1A. The i_{dconv} active current vector is shown to increase slightly due to absorbed active power required to keep the capacitors balanced and the current consumed by the 10 Ω filter resistance. This causes an increase in the $i_{d\ pcc}$ current from the initial 3.8A (0.76 pu) to 4 A (0.8 pu), 4.2 A (0.84) pu and 4.5 A (0.9 pu) at 50%, 75% and full compensation respectively.



Blue – Active Current Compenent, Green – Reactive Current Component

Figure 7.15: d-q current control, (a) PCC Side, (b) Load Side, (c) Converter Side

Figures 7.16 (a)-(b) show the STATCOM current responses and their corresponding reference values at 0% 50%, 75% and 100% compensation. Clearly, the response time fast is considered fast since steady state are reached within 50ms.



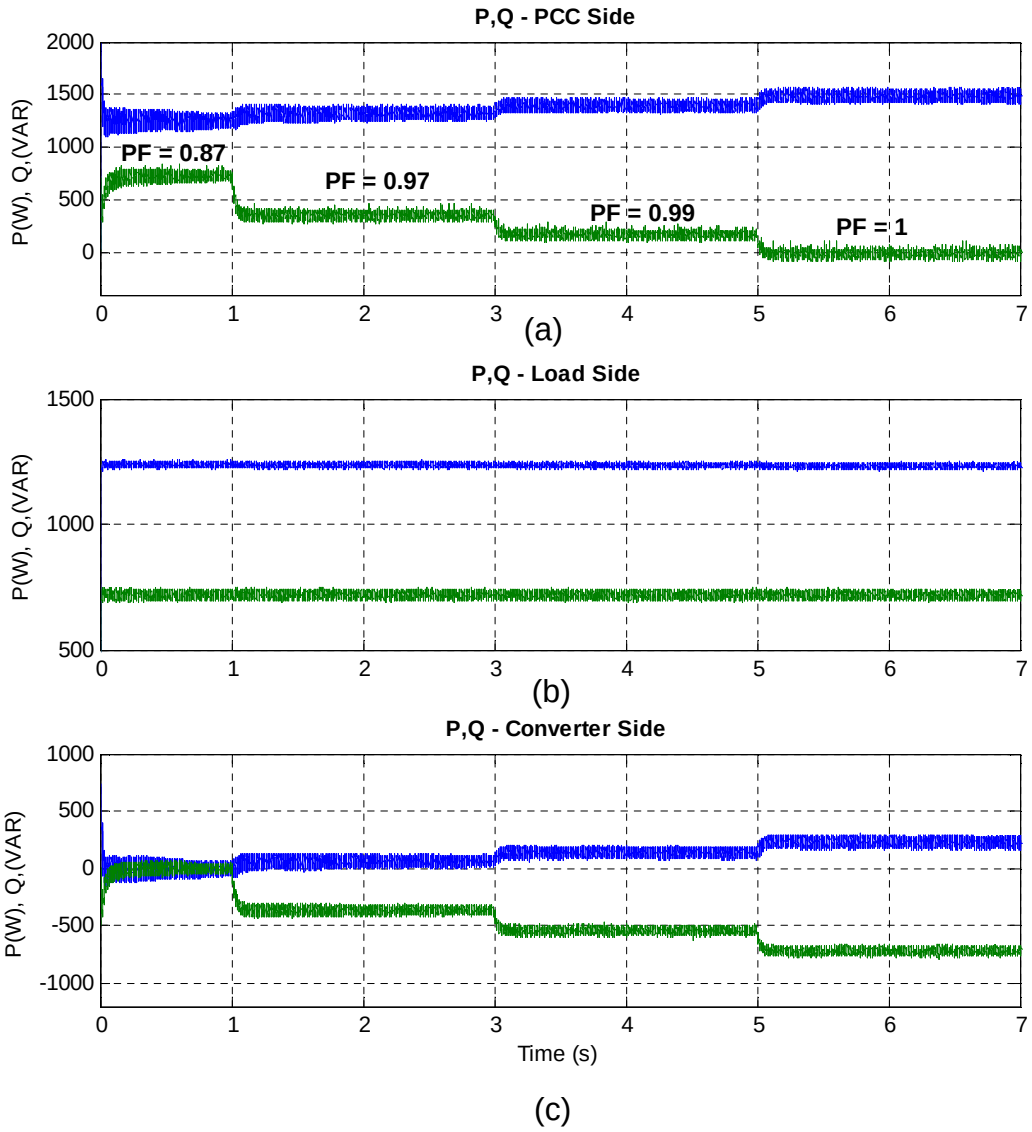
Blue – Current Reference, Green – Converter Current, Red – PCC Current

Figure 7.16: Response time of STATCOM current under each load condition Signals, (a) id current, (b) iq current, (a) id current, (b) iq current

7.3.2.2 Active and Reactive Power

Figures 7.17 (a)-(c) show the active and reactive power at the PCC, Load and Converter sides respectively.

The reactive power at the PCC is shown to approach zero with the same values as that in Section 7.3.1.2. The difference here is the active power at the PCC is the increasing due to the active power required to keep the capacitors balanced and also power consumed by the filter resistance. At time intervals 1s <t ≤ 3s, 3s <t ≤ 5s and 5s <t ≤ 7s, the active powers are 1.45 kW, 1.53 kW and 1.63 kW at the 50%, 75% and full compensation modes. The response time is also fast, achieving steady state within 50ms.



Blue – Active Power, Green – Reactive Power

Figure 7.17: Active and Reactive Power, (a) PCC Side, (b) Load Side, (c) Converter Side

7.3.2.3 PCC Side Waveforms

Figures 7.18 (a)-(d) show the three-phase voltages and currents, current magnitudes and power factor angle at different loading conditions.

The PCC current magnitude is shown to increase at the start when t = 0s, depicting the active current required to charge the converters capacitors. Within the first three cycles of each mode of operation, the PCC side currents per unit magnitude and power factor angle are shown to settle to

steady states. Their values are be $0.88\angle 30.07^{\circ}$, $0.83\angle 15.37^{\circ}$, $0.85\angle 7.46^{\circ}$, $0.9\angle 0^{\circ}$ corresponding to actual current values of $4.4A\angle 30.07^{\circ}$, $4.15A\angle 15.37^{\circ}$, $4.25A\angle 7.46^{\circ}$, $4.5A\angle 0^{\circ}$ for the 0%, 50%, 75% and full compensation mode respectively. Hence, the i_{qcc} is gradually reduced down to zero as expected.

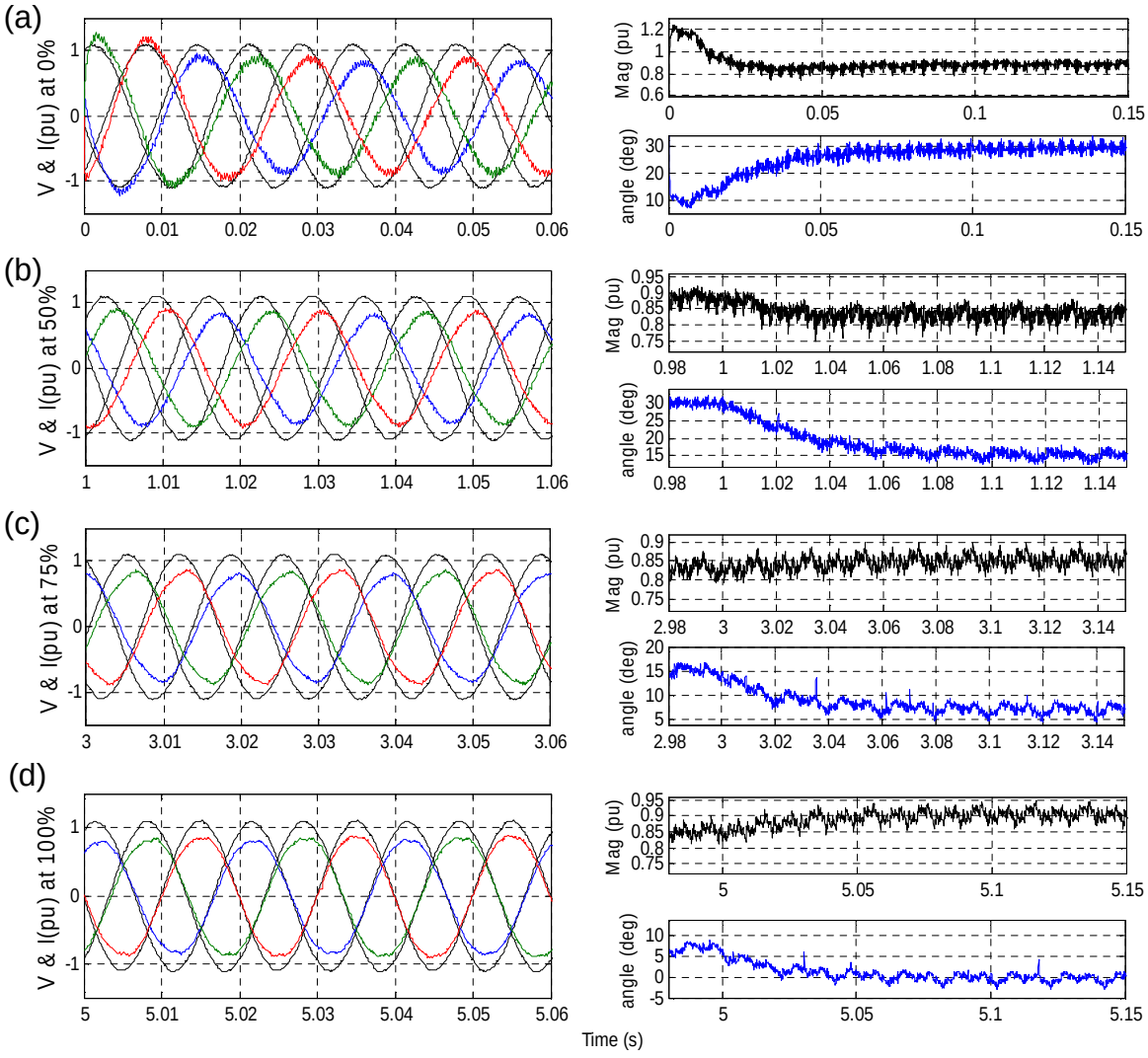


Figure 7.18: Voltage, Current and Power Factor Angle, (a) Zero compensation, (b) 50% compensation, (c) 75% compensation, (d) Full compensation

7.3.2.4 Converter Side Waveforms

Figure 7.19 (a)-(d) shows the three-phase voltages and current, active and reactive powers at the converter side for different loading conditions.

The converter current magnitude is shown to be increasing at the start to charge the capacitors. Within the first three cycles of each mode of operation, the converter side currents per unit magnitude and power factor

angle are shown to settle to steady state. Their value are be zero, $0.23\angle 77.20^{\circ}$, $0.34\angle 76.37^{\circ}$, $0.46\angle 72.34^{\circ}$ corresponding to actual current values of $1.15A\angle 77.20^{\circ}$, $1.70A\angle 76.37^{\circ}$, $2.3A\angle 72.34^{\circ}$, for the 50%, 75% and full compensation mode respectively.

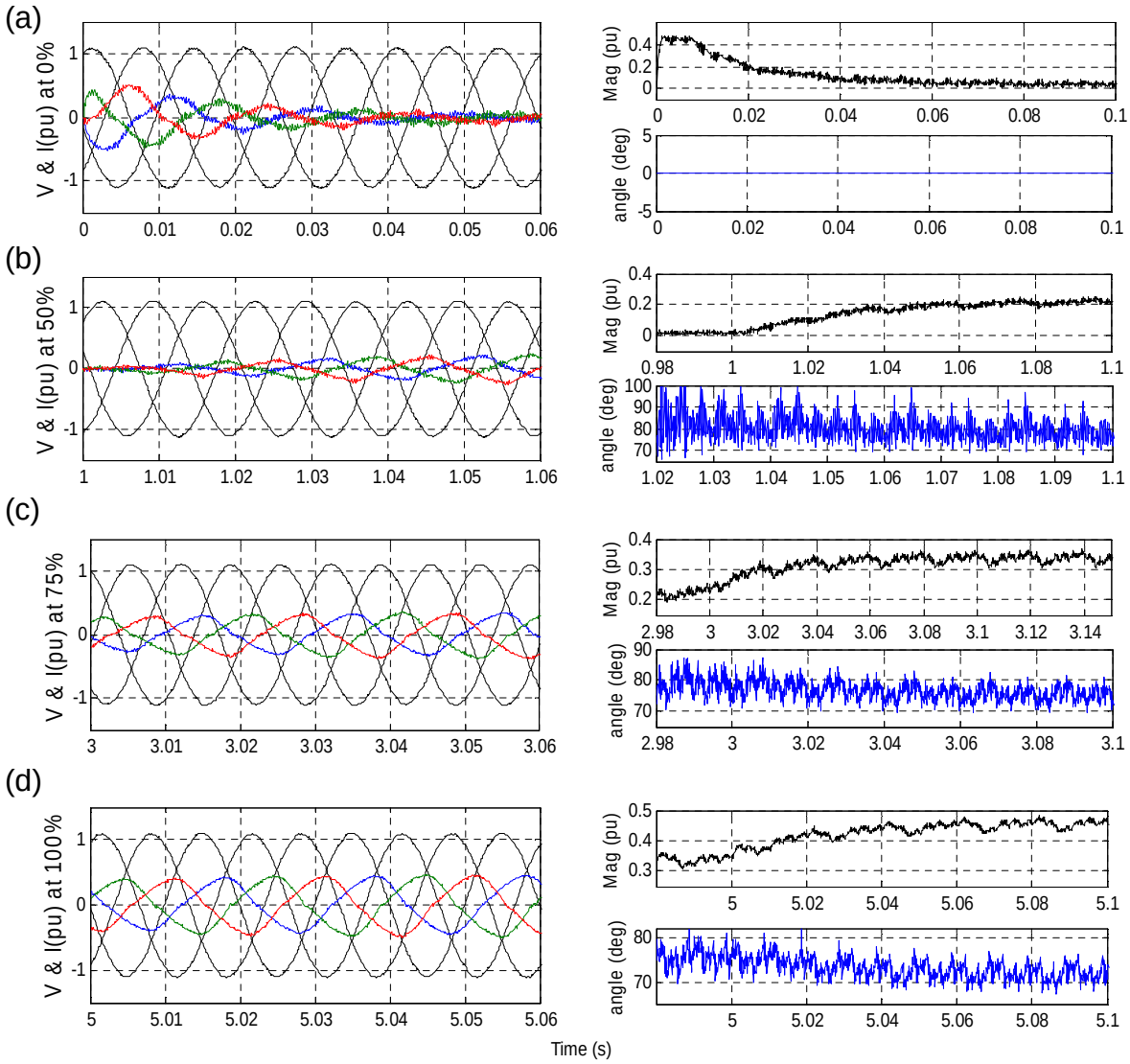


Figure 7.19: Voltage, Current and Converter Angle, (a) Zero compensation, (b) 50% compensation, (c) 75% compensation, (d) Full compensation

Figures 7.20 (a)-(c) shows the converters voltage modulation index, synchronisation angle and converters three-phase voltage waveforms.

The modulation index is shown to be controlled effectively. For time intervals 1s <t ≤ 3s, 3s <t ≤5s and 5s <t ≤ 7s , the converter adjusts its terminal voltages to meet the current demand and the modulation index and converter angles are adjusted to $0.82\angle -0.11^{\circ}$ rads, $0.83\angle 0.18^{\circ}$ rads and $0.83\angle -0.24$ rads.

Figure 7.20 (c) shows synchronisation been achieved with phase locked loop clocking at each fundamental cycle and Figure 7.20 (d) shows the 5 level converter output voltage at full compensation mode

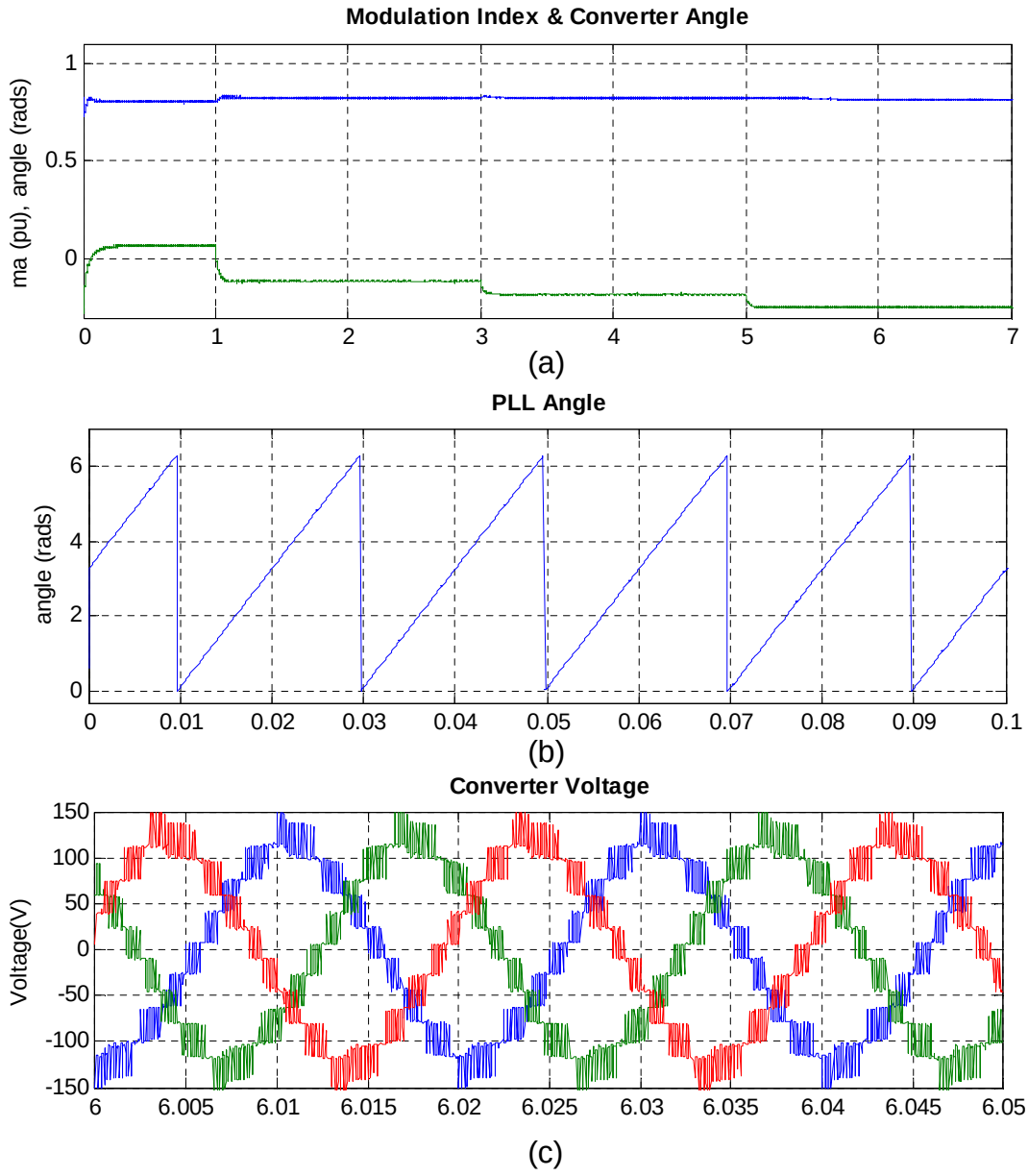


Figure 7.20: (a)Converter Modulation Index and Angle, (b) PLL Angle, (c) Converter Voltages Full Compensation

7.3.2.5 Capacitor Balancing

Figures 7.21 (a)-(f) show variations of the outer capacitor voltage waveforms.

The outer capacitors voltages at each of the phases are also shown to balance properly. The capacitor voltage peak to peak ripple increases with current flowing through the converter is ±4.3%. This is well within the desired ±10% maximum requirement.

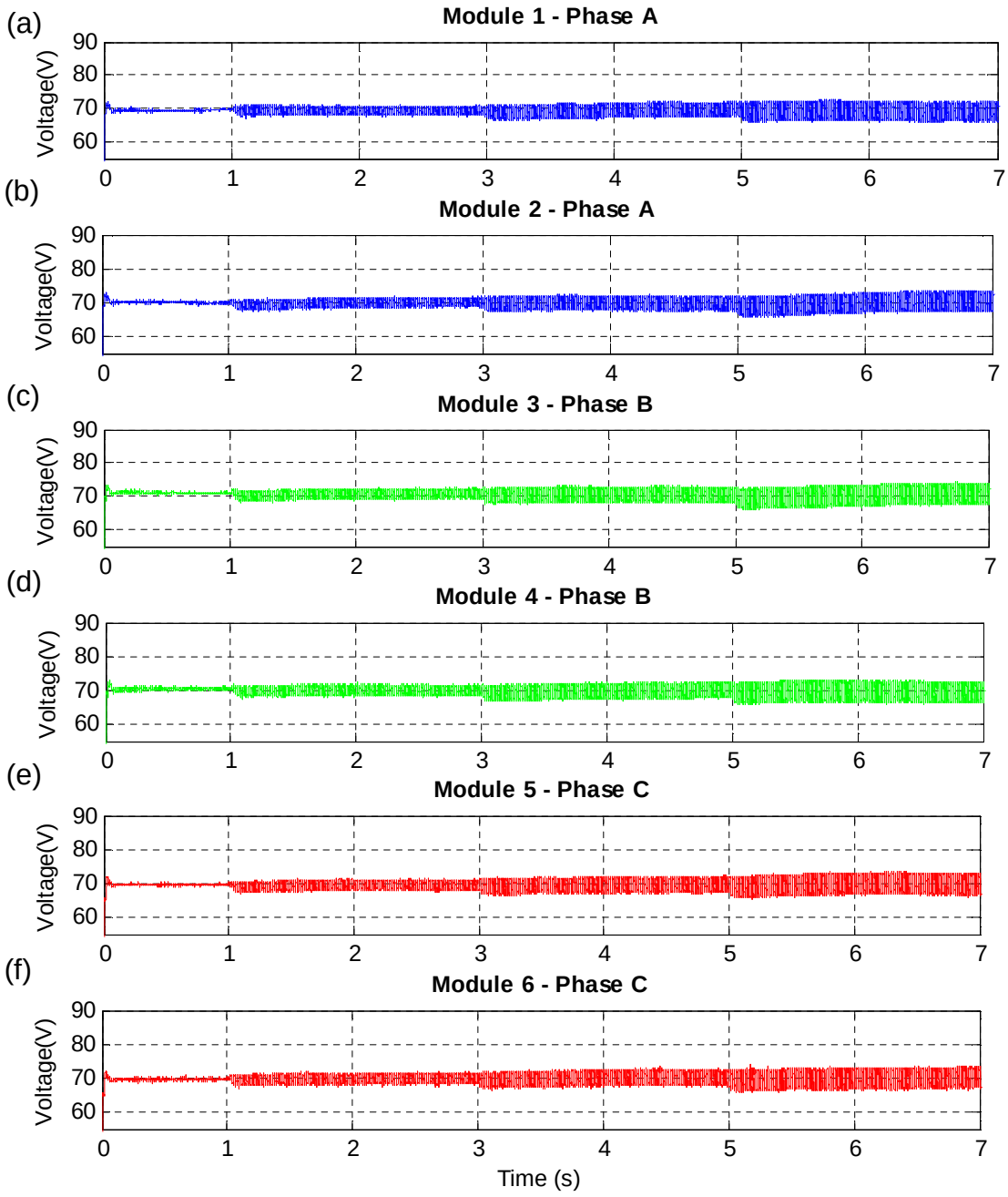


Figure 7.21: Outer Capacitor Waveforms

Figures 7.22 (a)-(c) show 10 cycle representation of the inner capacitor voltage waveforms at full compensation mode.

The inner capacitor voltages are shown to balance properly varying around 35 V which corresponds to half the outer capacitor DC voltage of 70 V. As discussed earlier in Chapter 3 certain phases tend to drift slightly away from the expected nominal voltage at 35V.

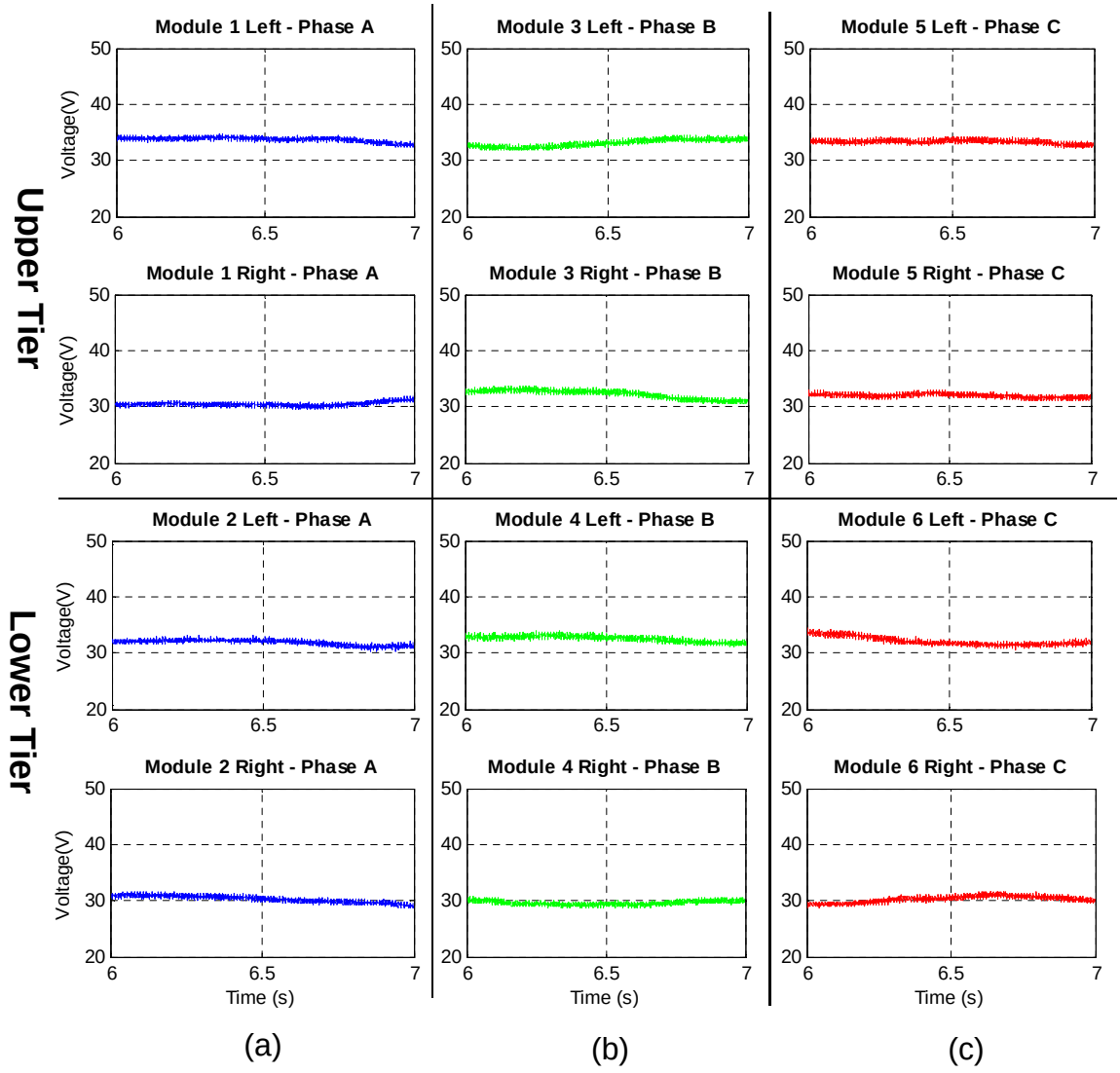


Figure 7.22: Inner Capacitor Waveforms

7.3 Comparison with Simulation Results

The test conditions and parameters used for the experimental study are made to match that of the simulation study in Chapter 5. Both results are shown to be similar under unity power factor correction. The reactive current at the PCC is shown to approach zero with the same values from 2.2A (0.44 pu) to 1.1A (0.22 pu) and 0.55A (0.11pu), then to 0A. On the load side the reactive current is maintained constant. Meanwhile the converter side reactive current magnitude increases from 0A to 0.55A (0.11pu) and 1.1A (0.22 pu), then to 2.2A (0.44 pu). The significant changes noticed are

- The increased noise in d-q current and voltage measured vectors in the experiments.
- The reduced transient response times at each load increment which has duration of 80 ms in the simulations and 50 ms in the experiments.
- The PWM switching transitions in the converters voltage waveform which is less ideal because actual and not ideal switching devices are used.

The increased noise and ripple in the capacitor voltage waveforms in the experiment due to more realistic harmonic variations in the current flowing through the sub-module capacitor and the capacitors electrical properties.

7.4 Conclusions

This chapter has discussed the experimental validation of the MMC-FC converter for reactive power compensation. The control system implementation has been discussed in detail showing that synchronisation is achieved and the current and voltage controllers perform control actions. Two converter configurations were discussed for reactive power compensation. Firstly, using a DC power supply and finally with capacitor feedback control. All results have been presented and discussed clearly in detail.

Chapter 8 will present future recommendations to give more insight about further possible research work within this study.

Chapter 8
Conclusions and Future Recommendations

8.1 Conclusions

This research has focused on investigating modular multilevel converters for STATCOM applications. The topology proposed is based on Flying Capacitor H-bridge sub-modules. To the author's knowledge, no study so far has investigated the features of an MMC using flying capacitor converters as sub-modules and its detailed application as a STATCOM. The feasibility studies via simulation and experimental validation have shown the converter to be applicable for reactive power compensation. This research helps to fill the knowledge gap in existing sub-module concepts for MMC STATCOM applications.

The individual contributions and achievements of this study are as summarised below.

- A comprehensive study was carried out to assess the usability of four sub-module concepts for MMC in STATCOM applications. The author established clear guidelines for the assessment based on the footprint, cost, power efficiency, control requirements and topology configuration of the converter. From this assessment, it was established that H-bridge sub-modules are the most feasible for STATCOM applications, followed by FC H-bridge sub-modules. The half-bridge and FC half-bridge were shown to have the least benefits for STATCOM applications and to be preferable for HVDC applications.
- The study has discussed in detail how to exploit the open-loop natural balancing feature of the FC-MMC STATCOM to achieve the inner flying capacitors voltage balance. Modulation schemes that can exploit this feature were discussed in detail, based on their total harmonic distortion and switching utilisation. The benefits and trade-offs were discussed and simulation and experimental studies to validate performance were presented.
- A significant outcome of this research work is the development of a novel synchronisation scheme using the energy operator. The principles of this technique were explained, showing its favourable and unfavourable points. The simplified method with an improved filter could prove to be ground breaking, providing a synchronisation

scheme with faster response times. The scheme was tested and shown to work with possible grid voltage scenarios adhering to IEEE specified recommendations of unbalance voltage conditions and harmonics.

- Further contributions of the work were to expand on already known literature for reactive power compensation. Based on this, the author developed via phasor analysis a new approach to rating the voltage of an MMC converter. This has considered carefully the influence of the filters and their cut-off frequencies. As a result, depending on the power application and reactive requirements the voltage rating of the converter can be chosen accordingly.
- The design considerations for modularity of the cell cards in the experimental power rig has proved beneficial in enhancing further study that is still on-going at the university.
- Finally, a closed loop control system for validating the FC-MMC converter has been developed. Results were shown to match the simulation study in Chapter 5, confirming good performance with all the capacitors balanced properly.

At the time of writing, four published conference papers have been derived from the work based in Chapters 3,4, and 5. Two journal publications are under consideration based on Chapters 2, 6 and 7 and Chapter 4. One journal paper is in preparation.

8.2 Future Recommendations

The current research undertaken can still be improved and foster further ideas to be investigated in the future. Suggested extensions of this work are summarised below:

- Investigation in this study was for balanced operation. The FC-MMC can also be validated under unbalanced current and voltage condition. Negative sequence reactive control for compensation would further enhance the viability of the FC-MMC converter.
- In addition, a more detailed experiment power loss assessment can be developed for the converter. This would require upgrading the converter control platform.
- Furthermore, the converter reactive compensation can investigated with the converter in this delta configuration and a detailed comparison taken to investigate the better approach.

Finally, there is a the possibility of using an adaptive DFT filter with the energy operator scheme to reduce frequency deviation error. This would further improve the response delay noticed. Wavelet filters can also be considered as an alternate approach to further reducing the delay time.

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Appendix A

A.1 Multilevel Converter Current Paths

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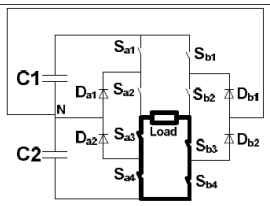
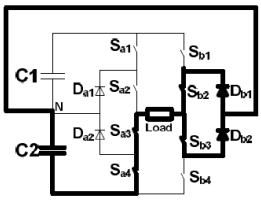
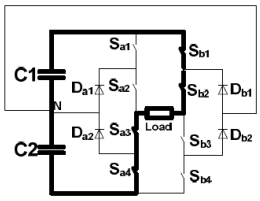
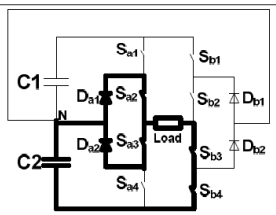
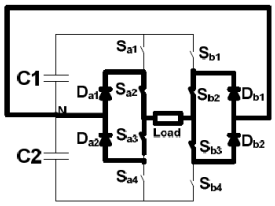
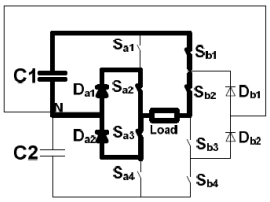
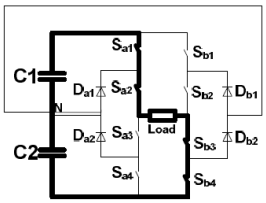
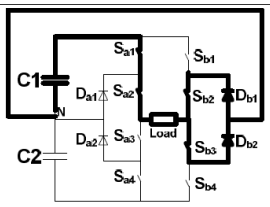
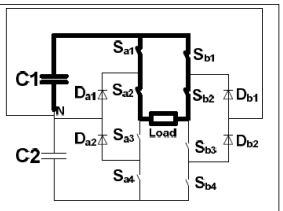
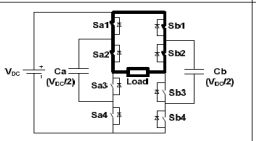
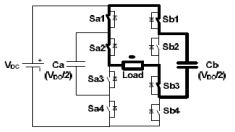
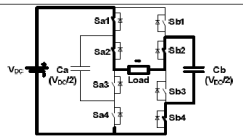
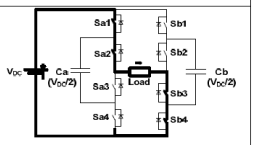
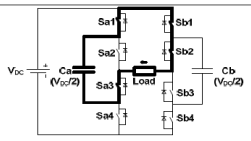
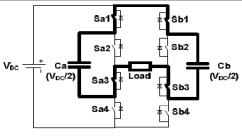
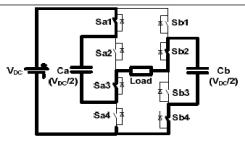
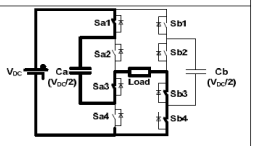
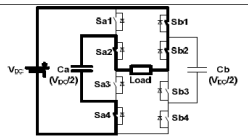
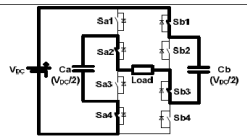
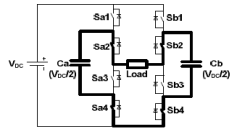
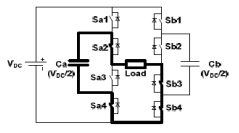
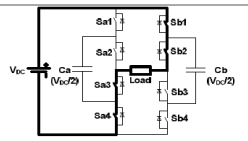
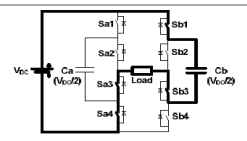
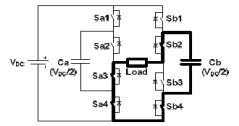
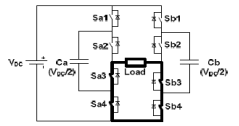
0011			
0110			
1100			

Current Paths for three-level neutral point clamped inverter switching states

Sa \ Sb	1100	1010	0101	0011
1100				
1010				
0101				
0011				

Current Paths for five-level flying capacitor multilevel inverter switching states

A.2 Fortescue Theorem

$$\begin{bmatrix} \vec{V}_a \\ \vec{V}_b \\ \vec{V}_c \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{bmatrix}\begin{bmatrix} V^0 \\ V^+ \\ V^- \end{bmatrix}$$ where $a = 1\angle 120^\circ$ and $a^2 = 1\angle -120^\circ$

The transformation matrix A is

$$A = \begin{bmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{bmatrix}$$ and its inverse is

$$A^{-1} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix}$$

Hence,

$$\begin{bmatrix} V^0 \\ V^+ \\ V^- \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix}\begin{bmatrix} \vec{V}_a \\ \vec{V}_b \\ \vec{V}_c \end{bmatrix}$$

Appendix B

B.1 Energy Operator Trigonometric Identities

Using the two trigonometric identities

$$\cos(A+B)\cos(A-B) = \frac{1}{2}\cos(2A) + \cos(2B)$$

$$\cos(2A) = 2\cos^2 A - 1 \tag{B1.1}$$

$$\cos A - \cos B = 2\sin\left(\frac{A+B}{2}\right)\sin\left(\frac{A-B}{2}\right) \tag{B1.2}$$

$$\sin^2 A = \frac{1-\cos 2A}{2}$$

$$\sin B \sin C = \frac{\cos(B-C) - \cos(B+C)}{2} \tag{B1.3}$$

where, $A = \Omega_x n + \phi_x, B = \Omega_x (n+1) + \phi_x, C = \Omega_x (n-1) + \phi_x$

Using the trigonometric identity and solving for A→E

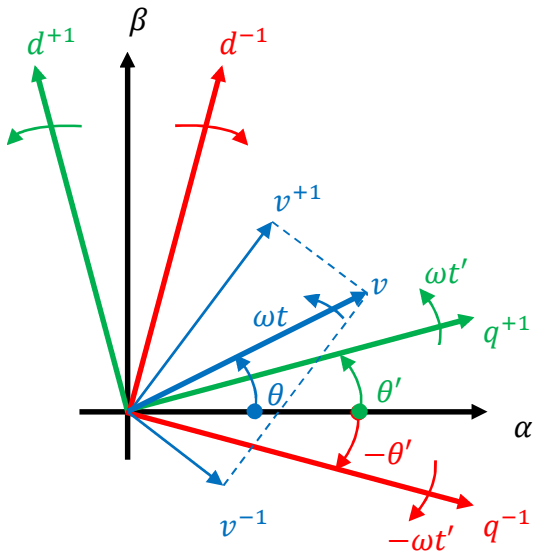
$$\cos A \cos B = \frac{1}{2}\left(\cos(A-B)\cos(A+B)\right) \tag{B1.4}$$

where, $A = \Omega_x n + \phi_x,\ B = \Omega_x (n+1) + \phi_y,$
$E = \Omega_x (n+1) + \phi_y,\ F = \Omega_x (n-1) + \phi_y$

B.2 Principles of PLL Schemes Used for Comparison

B.2.1 Decoupled Double Synchronous Reference Frame (DDSRF)

The decoupled double synchronous reference frame (DDSRF) synchronisation scheme eliminates the oscillations at 2ω observed with the d-q frame for unbalanced grid voltage conditions. This is eliminated using two synchronous reference frames with a cross-decoupling system to extract the positive sequence of the voltages. Figure below shows the graphical illustration of the positive-sequence and negative-sequence components of the unbalanced voltage vector with a DDSRF. The two reference frames, dq^n dq^m rotate at $n\omega t'$ and in the opposite direction $-n\omega t'$.



Double Synchronous Reference Frame (DDSRF)

where, $n=+1$, $m=-1$ denotes the positive sequence and negative sequence reference frame with rotational speed of $\theta'=\omega t'$ and $-\theta'=-\omega t'$ respectively.

The phase angle θ' is detected by the PLL and the objective is to achieve synchronization applying SRF-PLL after the positive sequence d-q components are extracted to make $\theta'=\theta$.

The positive and negative sequences can be expressed in the $\alpha-\beta$ reference frames as shown in (B1.1).

$$v_{\alpha\beta}=v_{\alpha\beta}{}^{n}+v_{\alpha\beta}{}^{m}=\begin{bmatrix}v_\alpha\\ v_\beta\end{bmatrix}=V^{+1}\begin{bmatrix}\sin(n\omega t+\phi^n)\\ \cos(n\omega t+\phi^n)\end{bmatrix}+V^{-1}\begin{bmatrix}\sin(m\omega t+\phi^m)\\ \cos(m\omega t+\phi^m)\end{bmatrix}$$

$$v_{\alpha\beta} = v_{\alpha\beta}{}^{+1} + v_{\alpha\beta}{}^{+1} = \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = V^{+1}\begin{bmatrix} \sin(\omega t + \phi^{+1}) \\ \cos(\omega t + \phi^{+1}) \end{bmatrix} + V^{-1}\begin{bmatrix} \sin(-\omega t + \phi^{-1}) \\ \cos(-\omega t + \phi^{-1}) \end{bmatrix} \quad \text{(B1.1)}$$

This can be expressed in the d-q reference frame as shown in (B1.2) – (B1.5)

$$v_{dq} = v_{dq}{}^{n} + v_{dq}{}^{m}$$

where,

$$v_{dq}{}^{n} = \begin{bmatrix} v_d{}^{n} \\ v_q{}^{n} \end{bmatrix} = \underbrace{V^{n}\begin{bmatrix} \cos\phi^{n} \\ \sin\phi^{n} \end{bmatrix}}_{DC\ terms} + \underbrace{V^{m}\cos\phi^{m}\begin{bmatrix} -\cos((n-m)\omega t) \\ \sin((n-m)\omega t) \end{bmatrix} + V^{m}\sin\phi^{m}\begin{bmatrix} \sin((n-m)\omega t) \\ \cos((n-m)\omega t) \end{bmatrix}}_{AC\ terms} \quad \text{(B1.2)}$$

$$v_{dq}{}^{n} = \begin{bmatrix} v_d{}^{n} \\ v_q{}^{n} \end{bmatrix} = \begin{bmatrix} \bar{v}_d{}^{n} \\ \bar{v}_q{}^{n} \end{bmatrix} + \begin{bmatrix} \tilde{v}_d{}^{n} \\ \tilde{v}_q{}^{n} \end{bmatrix} \quad \text{(B1.3)}$$

$$v_{dq}{}^{m} = \begin{bmatrix} v_d{}^{m} \\ v_q{}^{m} \end{bmatrix} = \underbrace{V^{m}\begin{bmatrix} \cos\phi^{m} \\ \sin\phi^{m} \end{bmatrix}}_{DC\ terms} + \underbrace{V^{n}\cos\phi^{n}\begin{bmatrix} -\cos((n-m)\omega t) \\ -\sin((n-m)\omega t) \end{bmatrix} + V^{n}\sin\phi^{n}\begin{bmatrix} -\sin((n-m)\omega t) \\ \cos((n-m)\omega t) \end{bmatrix}}_{AC\ Terms} \quad \text{(B1.4)}$$

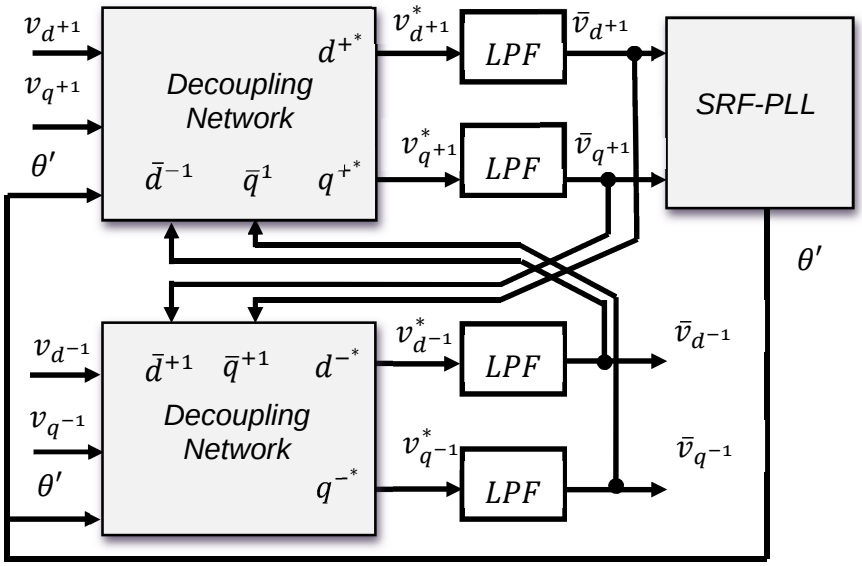
$$v_{dq}{}^{m} = \begin{bmatrix} v_d{}^{m} \\ v_q{}^{m} \end{bmatrix} = \begin{bmatrix} \bar{v}_d{}^{m} \\ \bar{v}_q{}^{m} \end{bmatrix} + \begin{bmatrix} \tilde{v}_d{}^{m} \\ \tilde{v}_q{}^{m} \end{bmatrix} \quad \text{(B1.5)}$$

Using (B1.2)-(1.5), when *n* is +1 and *m* is -1, the DDSRF scheme can be expressed in the form (B1.6), (B1.7)

$$\begin{bmatrix} \bar{v}_d{}^{+1} \\ \bar{v}_q{}^{+1} \end{bmatrix} = \begin{bmatrix} v_d{}^{+1} \\ v_q{}^{+1} \end{bmatrix} - \bar{v}_d{}^{-1}\begin{bmatrix} -\cos(2\omega t) \\ \sin(2\omega t) \end{bmatrix} - \bar{v}_q{}^{-1}\begin{bmatrix} \sin(2\omega t) \\ \cos(2\omega t) \end{bmatrix} \quad \text{(B1.6)}$$

$$\begin{bmatrix} \bar{v}_d{}^{-1} \\ \bar{v}_q{}^{-1} \end{bmatrix} = \begin{bmatrix} v_d{}^{-1} \\ v_q{}^{-1} \end{bmatrix} + \bar{v}_d{}^{+1}\begin{bmatrix} -\cos(2\omega t) \\ -\sin(2\omega t) \end{bmatrix} - \bar{v}_q{}^{+1}\begin{bmatrix} -\sin(2\omega t) \\ \cos(2\omega t) \end{bmatrix} \quad \text{(B1.7)}$$

Both equations show that the positive and negative sequences of the d-q components consist of DC components and AC components at 2ω . The amplitude of AC terms in dq^{+1} depends on the DC terms in dq^{-1} and vice versa. Hence, to completely eliminate the effect of these oscillations, a decoupling network and low pass filters are used to extract the DC component of the positive sequence using the equations (B1.6) and (B1.7). This is as shown in the Figure below.



Decoupling Network + SRF-PLL (DDSRF-PLL)

The SRF-PLL scheme is used afterwards at the positive sequence d-q components to achieve synchronisation. The limitation of this technique is that the decoupling network can only eliminate one harmonic component at a time. This implies it won't work properly when the three phase voltages have multiple harmonics.

B 2.2 Cascaded Delay Signal Cancellation (CDSC-PLL)

This method utilises the half-wave symmetry property of sinusoids to cancel out selected harmonics. This is done by summing the signal harmonic components with respective half-cycle delayed versions.

In order to derive a general expression of the required delay time a DSC operator is defined as shown in (B1.8) [204] .

$$DSC_n[v(t)] = \frac{1}{2}\left[v(t) + v\left(t - \frac{T}{n}\right)\right] \qquad \text{(B1.8)}$$

where, the delay time is *1/n* of the fundamental period.

Applying $DSC_n(.)$ operator to the *d-q* component harmonic references gives

$$\begin{aligned} DSC_n[{v_d}^h] &= \frac{1}{2}\left[{v_d}^h(t) + {v_d}^h\left(t-\frac{T}{n}\right)\right] \\ &= \frac{1}{2}\left[\sqrt{2}V\cos(h\omega t+\varphi_h) + \sqrt{2}V\cos\left(h\omega\left(t-\frac{T}{n}\right)+\varphi_h\right)\right] \\ &= \sqrt{2}V\cos\left(h\omega t+\varphi_h-\frac{h\pi}{n}\right)\cos\left(\frac{h\pi}{n}\right) \end{aligned} \quad \text{(B1.9)}$$

$$\begin{aligned} DSC_n[{v_q}^h] &= \frac{1}{2}\left[{v_q}^h(t) + {v_q}^h\left(t-\frac{T}{n}\right)\right] \\ &= -\frac{1}{2}\left[\sqrt{2}V\sin(h\omega t+\varphi_h) + \sqrt{2}V\sin\left(h\omega\left(t-\frac{T}{n}\right)+\varphi_h\right)\right] \\ &= -\sqrt{2}V\sin\left(h\omega t+\varphi_h-\frac{h\pi}{n}\right)\cos\left(\frac{h\pi}{n}\right) \end{aligned} \quad \text{(B1.10)}$$

where ± *h,* represents the harmonic order in the positive or negative sequence *d-q* frame.

Hence, (B1.9) and (B1.10) can be re-written in form of the complex j operator (B1.11).

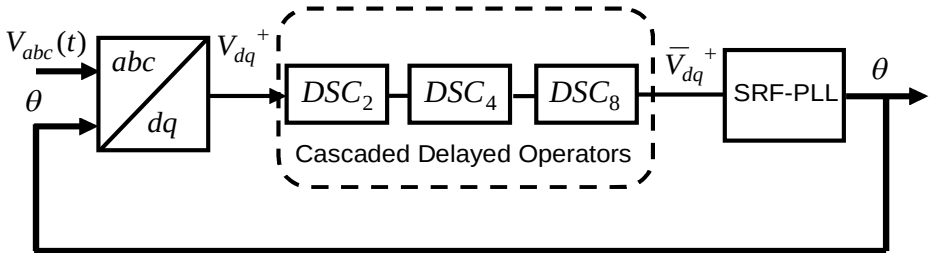
$$DSC_n[(V_d + jV_q)^h] = \vec{v}_{dq}{}^h\left(\cos\frac{h\pi}{n}\right).e^{-j\frac{h\pi}{n}} = \vec{v}_{dq}{}^h\, G_{DSC\,n}(h) \quad \text{(B1.11)}$$

where, $G_{DSC\,n}(h)$ represents the gain magnitude of the operator

Provided $\left|G_{DSCn}(h)\right| = 0$ can be solved in (1.33), the time delay time $\frac{T}{n}$ can be calculated to eliminate the various *h* order harmonics.

$$n = \left|\frac{h}{2k \pm (1/2)}\right| \quad \text{(B1.12)}$$

The figure below shows the generalised block diagram for the CDSC scheme for *n = 2, 4 and 8.*



B.3 C-Code for Energy Operator Experiments

B 3.1 C-Code for Voltage Generation

```
/*****************************************************************/
int main()
{
PWMH1.period( 1.0f / (float) SWITCHING_FREQ);
PWM_ticker.attach(&sine_PWM_gen, 1.0f/(float)(UPDATE));
PWM2_ticker.attach(&sine_PWM_gen2, 1.0f/(float)(UPDATE2));
pc.baud(460800);
while(1) {
c.printf("%f, %f, %f, %f,\n\r", Va, Vb, Vc,count);
}
}
79
//Function to generate a three phase waveform
void sine_PWM_gen()
{
if (count<=100) {
if (count <= 20.0000) {
Vc =(sine_table[C]);
Vb =(sine_table[B]);
Va =sine_table[A];
} else if(count >= 20.00 && count <= 40.0000) {
//Variation of modulation index one phase
Vc =(0.5*(1-0.8))+(0.8*sine_table[C]);
Vb =sine_table[B];
Va =sine_table[A];
} else if(count >= 50.00 && count <= 60.0000) {
//Variation of modulation index two phases
Vc =(0.5*(1-0.8))+(0.8*sine_table[C]);
Vb =(0.5*(1-0.5))+(0.5*sine_table[B]);
Va =sine_table[A];
} else {
Vc =(sine_table[C]);
Vb =(sine_table[B]);
Va =sine_table[A];
}
//output to PWM ports
PWMH1.write(Va);
PWMH2.write(Vb);
PWMH3.write(Vc);
A++;
B++;
C++;
if(A==400) { A=0; }
if(B==400) { B=0; }
if(C==400) { C=0; }
count = count + 0.00005;
leds = 1;
```

```
}
else {
//Vc =(sine_table[C]);
// Vb =(sine_table[B]);
//Va =sine_table[A];
}
}
// Function to vary frequency
void sine_PWM_gen2()
{
if (count < 100.0000) {
} else {
Vc =(sine_table[C]);
Vb =(sine_table[B]);
80
Va =sine_table[A];
PWMH1.write(Va);
PWMH2.write(Vb);
PWMH3.write(Vc);
A++;
B++;
C++;
if(A==400) { A=0; }
if(B==400) { B=0; }
if(C==400) { C=0; }
count = count + 0.00004167;
leds = 15;
}}
```

Appendix C
Fundamental Power Relationships

In the case of the three phase vector equivalent, the compensator can be an ideal voltage regulator when it can be controlled over a sufficiently wide range to supply a purely reactive current $I_{sqnew} = I_{sq} + I_{cq}$.

$$\begin{aligned}
\Delta V &= I_s \times Z_s \\
\Delta V &= I_{s\,real} + jI_{s\,imag}\left(R_s + jX_s\right) \\
\Delta V &= \left(R_s I_{s\,real} - X_s I_{s\,imag}\right) + j\left(X_s I_{s\,real} + R_s I_{s\,imag}\right) \\
\Delta V &= \Delta V_R + \Delta V_X
\end{aligned} \qquad \text{(C1.1)}$$

C.1 Clarkes and Parks Transformation

Consider the three-phase symmetrical and balanced electromagnetic quantities such as voltage (also current, flux), with magnitude *V*, frequency *f*, angular velocity $\omega=2\pi f$ and phase angle $\theta=0$. When it is referred to the stationary 3-phase abc reference frame:

$v_a(t) = V\sin(\omega t + \theta)$, $v_b(t) = V\sin(\omega t + \theta_o + 120^\circ)$, $v_c(t) = V\sin(\omega t + \theta_o - 120^\circ)$.

Clarke's transformation gives a representation of three-phase voltage vector in a stationary two-dimensional (α-β) reference frame. The matrix representation for the power invariant form of Clarke's transformation is as shown by equations (C1.7)-(C1.9)

$$\begin{bmatrix} \vec{V}_\alpha \\ \vec{V}_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} \vec{V}_a \\ \vec{V}_b \\ \vec{V}_c \end{bmatrix} \qquad \text{where} \qquad \text{(C1.7)}$$

$$\vec{V}_\alpha = \sqrt{\frac{2}{3}}\left(\vec{V}_a - \frac{1}{2}\vec{V}_b - \frac{1}{2}\vec{V}_c\right) \quad \text{and} \qquad \text{(C1.8)}$$

$$\vec{V}_\beta = \sqrt{\frac{2}{3}}\left(\frac{\sqrt{3}}{2}\vec{V}_b - \frac{\sqrt{3}}{2}\vec{V}_c\right) \qquad \text{(C1.9)}$$

The inverse matrix representation for the power invariant form of Clarke's transformation is shown as

$$\begin{bmatrix} \vec{V}_a \\ \vec{V}_b \\ \vec{V}_c \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} \vec{V}_\alpha \\ \vec{V}_\beta \end{bmatrix} \qquad \text{(C1.10)}$$

The $\frac{2}{3}$ factor is a normalising factor that ensures the Clarke's transformation is a unit circle (i.e. 1.5 to 1 p.u.) and the square root $\sqrt{\frac{2}{3}}$ ensures that this is kept when power is considered (power circle normalised to 1 pu) *i.e.* $\sqrt{\frac{2}{3}}\, V \times \sqrt{\frac{2}{3}}\, I = \frac{2}{3} P$.

The stationary α-β reference frame can be further transformed into a d-q frame rotating synchronous with a chosen reference frame at the angular frequency ω. The matrix for transforming from α-β to d-q according to power invariant form of Park's transformation is as shown below

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \sin\theta & \cos\theta \\ -\cos\theta & \sin\theta \end{bmatrix} \begin{bmatrix} \vec{V}_\alpha \\ \vec{V}_\beta \end{bmatrix} \qquad \text{(C1.11)}$$

$$V_d = \sqrt{\frac{2}{3}} \left(\vec{V}_\alpha \sin\theta + \vec{V}_\beta \cos\theta \right) \qquad \text{(C1.12)}$$

$$V_q = \sqrt{\frac{2}{3}} \left(-V_\alpha \cos\theta + V_\beta \sin\theta \right) \qquad \text{(C1.13)}$$

where $\theta = \omega t$

The inverse matrix for the power invariant form of Park's transformation from to d-q to α-β is shown

$$\begin{bmatrix} \vec{V}_\alpha \\ \vec{V}_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \sin\theta & \cos\theta \\ -\cos\theta & \sin\theta \end{bmatrix} \begin{bmatrix} V_d \\ V_q \end{bmatrix} \qquad \text{(C1.14)}$$

Using equations (2.02) and (2.03) the transformation can be further simplified to a direct abc to d-q transformation as

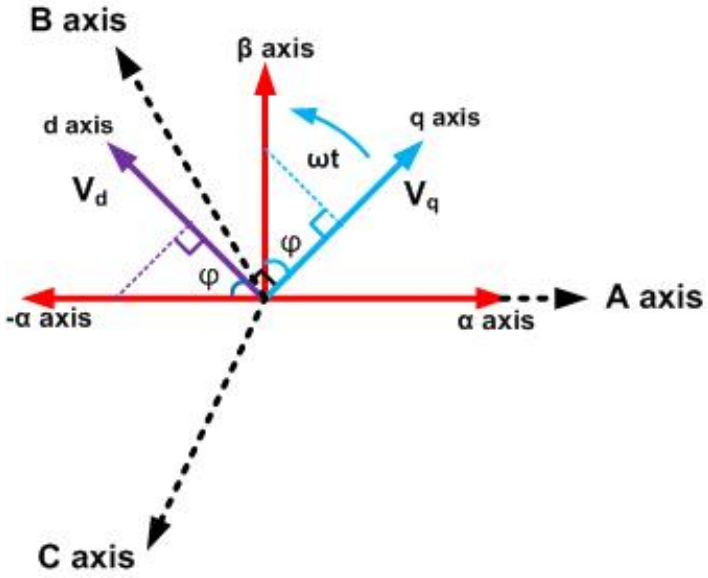
$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \sin\theta & - & \left(\frac{1}{2}\sin\theta + \frac{\sqrt{3}}{2}\cos\theta \right) & - & \left(\frac{1}{2}\sin\theta + \frac{\sqrt{3}}{2}\sin\theta \right) \\ \cos\theta & - & \left(\frac{1}{2}\cos\theta + \frac{\sqrt{3}}{2}\sin\theta \right) & - & \left(\frac{1}{2}\cos\theta + \frac{\sqrt{3}}{2}\sin\theta \right) \end{bmatrix} \begin{bmatrix} \vec{V}_a \\ \vec{V}_b \\ \vec{V}_c \end{bmatrix} \qquad \text{(C1.15)}$$

$$\sin\left(\theta \pm \frac{2\pi}{3}\right) = -\frac{1}{2}\sin\theta \pm \frac{\sqrt{3}}{2}\cos\theta$$
$$\cos\left(\theta \pm \frac{2\pi}{3}\right) = -\frac{1}{2}\cos\theta \mp \frac{\sqrt{3}}{2}\sin\theta \qquad \text{(C1.16)}$$

Substituting the trigonometric identity in (C1.16) results in (C.17),

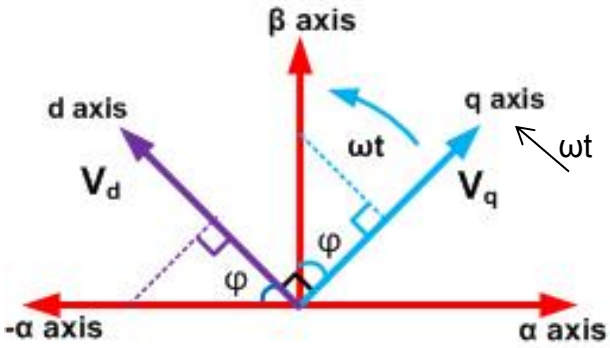
$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \sin\theta & \sin\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta + \frac{2\pi}{3}\right) \\ \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \end{bmatrix} \begin{bmatrix} \vec{V}_a \\ \vec{V}_b \\ \vec{V}_c \end{bmatrix} \qquad \text{(C1.17)}$$

Figure below illustrates the three-phase voltage and its representations in α-β and d-q reference frames through Parks and Clarks Transformation.



Parks and Clarks Transformation

C.2 Derivation of Decoupling Operator $(e^{j\theta})$



Parks Transformation

Figure 2.3 shows a voltage vector in d-q reference frame. The phase angle φ is the displacement or phase shift between this voltage vector and the synchronous reference frame and based on the arrow indicated direction of rotation it is a lagging phase angle. The voltage vector in α-β and d-q forms could be written as complex quantities $V_\alpha + jV_\beta \;\; and \;\; V_d + jV_q$ respectively.

Assuming unity magnitude we have

$\vec{V}_\alpha = \sin(\theta - \varphi) \;\; and \;\; \vec{V}_\beta = \cos(\theta - \varphi)$, then Park's transformation matrix can be re-written as

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \sin\theta & \cos\theta \\ -\cos\theta & \sin\theta \end{bmatrix} \begin{bmatrix} \sin(\theta - \varphi) \\ \cos(\theta - \varphi) \end{bmatrix} \qquad \text{(C.18)}$$

Neglecting the $\sqrt{\frac{2}{3}}$ normalising factor

$$V_d = \sin\theta \sin(\theta - \varphi) + \cos\theta \sin(\theta - \varphi) \;\; = \;\; \cos\varphi$$

$$V_q = -\cos\theta \sin(\theta - \varphi) + \sin\theta \cos(\theta - \varphi) \;\; = \;\; \sin\varphi$$

$$V_d + jV_q = \cos\varphi + j\sin\varphi \qquad \text{(C1.19)}$$

$$V_d - \; Active\, component \;,\; V_q - \; \text{Re}\, active \;\; Component$$

The parks transformation can be expressed in term of an operator $e^{j\theta}$

$$V_d + jV_q = [operator] \times (V_\alpha + jV_\beta) \qquad \text{(C1.20)}$$

Substituting the operator $-je^{j\theta}$ in equation (C1.20) results in

$$V_d + jV_q = \left[-je^{j\theta}\right] \times (V_\alpha + jV_\beta)$$

$$where \quad -je^{j\theta} = -j(\cos\theta + j\sin\theta) = \sin\theta - j\cos\theta$$

$$V_d + jV_q = (\sin\theta - j\cos\theta) \times \sin(\theta - \varphi) + j\cos(\theta - \varphi)$$

$$V_d + jV_q = \left(\sin\theta \sin(\theta - \varphi) + \cos\theta \cos(\theta - \varphi)\right) + j\left(\sin\theta \cos(\theta - \varphi) - \cos\theta \sin(\theta - \varphi)\right) = \cos\varphi + j\sin\varphi$$

C.3 Matlab Code for Case Study

```
thetai = 45:1:90;
thetai_rad = (thetai/180)*pi;
theta= (30/180)*pi;
Vpcc = 1;
Isreal =1*cos(-theta);
Isimag =1*sin(-theta);

Icimag = -Isimag;
Icreal = Icimag./tan(thetai_rad);

Icmag = sqrt(Icreal.^2+Icimag^2);

Sratio = 0.5; %limited to 10 max


thetaz = atan(Sratio);
thetaz_deg = (thetaz/pi)*180;

Zmag = 0.1;

Vzmag = Icmag*Zmag;
thetavz= -thetai_rad+thetaz;
thetavz_deg = (thetavz/pi)*180;

b=Vzmag.*cos(thetavz);

Vdc= Vpcc+b;

Rconv = (Vpcc.*Icmag.*sin(thetai_rad));
Pconv = (Vpcc.*Icmag.*cos(thetai_rad));
x = 1:0.01:1.3;
y20= ones(1,31).*78.69;
y40= ones(1,31).*68.20;
y60= ones(1,31).*59.04;
y80= ones(1,31).*51.34;

figure(1);

plot(thetai,Vdc);
hold on;
plot(y20,x);
hold on;
plot(y40,x);
hold on;
plot(y60,x);
hold on;
plot(y80,x);
hold on;
grid on;
```

Appendix D
Current Protection Circuitry

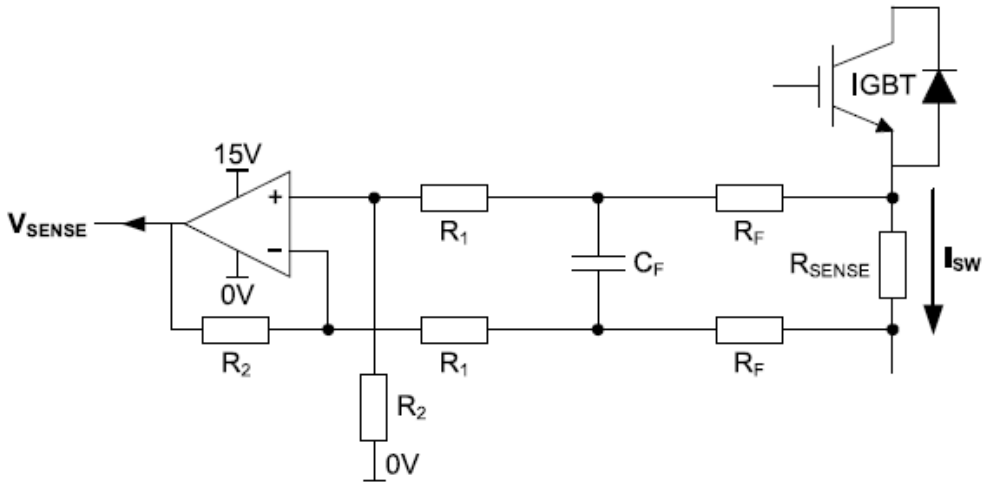
D.1 Current Sensing Circuit

Over-current protection is applied to each IGBT switching device to prevent its forward current surpassing some pre-defined rated limits. The circuit uses a combination of a differential amplifier current sensing circuit and an op-amp comparator circuit as shown in Figure 6.11. In the current sensing circuit, a shunt resistance of low value (10mΩ) is connected at the emitter of each IGBT switch and provides a minimal power dissipation and voltage drop when the switch conducts. In order to achieve measurable signals, a differential amplifier circuit is used to amplify the measured voltage to a 0-3V voltage range. The scale of amplification is determined by the resistor values R_1 , R_f and R_2 following the relationship in (D1.1). RC Low pass filters are included to create a certain amount of differential mode filtering and remove unwanted noise spikes that occur during switching.

$$V_{SENSE} = \frac{R_2}{R_1 + R_f} \times I_{SW} \times R_{SENSE} \quad \text{(D1.1)}$$

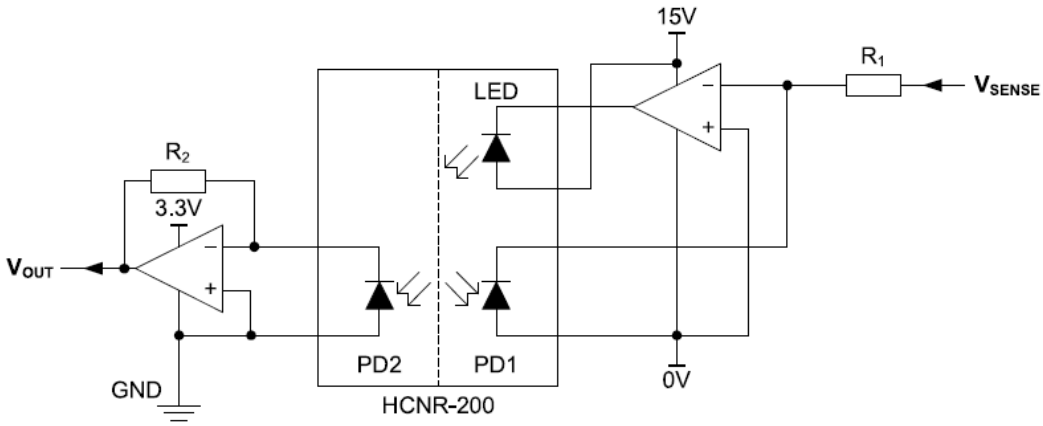
$$f_c = \frac{1}{2\pi \times C_f \times 2R_f} \quad \text{(D1.2)}$$

$$V_{OUT} = \frac{R_2}{R_1} \times V_{SENSE} \quad \text{(D1.3)}$$



Current Sensing Circuit

The gate and over current electronics share a common 15V DC power supply. Hence to prevent coupling issues and provide isolation, a linear opto-coupler (HNCR-200) is used as shown in the figure below. This opto-coupler contains two photo-detectors. The second detector and a feedback amplifier provide linearity following the expression (D1.3), so eliminating the non-linear characteristics exhibited by LEDs. The trans impedance amplifier at the isolated side is powered from a separate 3.3V voltage regulator on the power cell card.

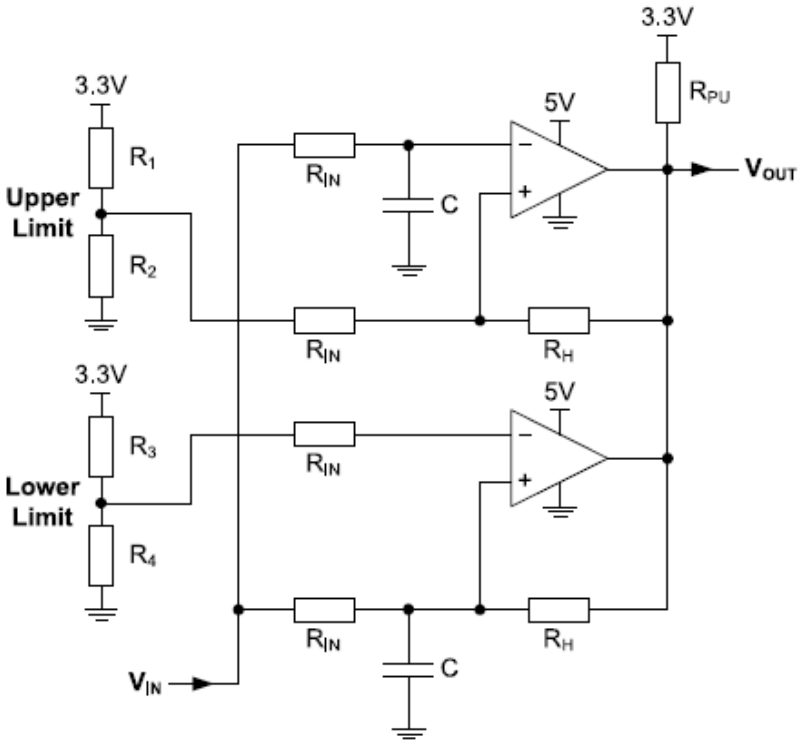


Linear opto-isolation circuit

D.2 Current Limiter Circuit

The measured 0-3V signal is fed into a current limiter circuit as shown in the figure below. This uses op-amp comparators with pre-defined lower and upper limits set by potential dividers $R_1 - R_4$

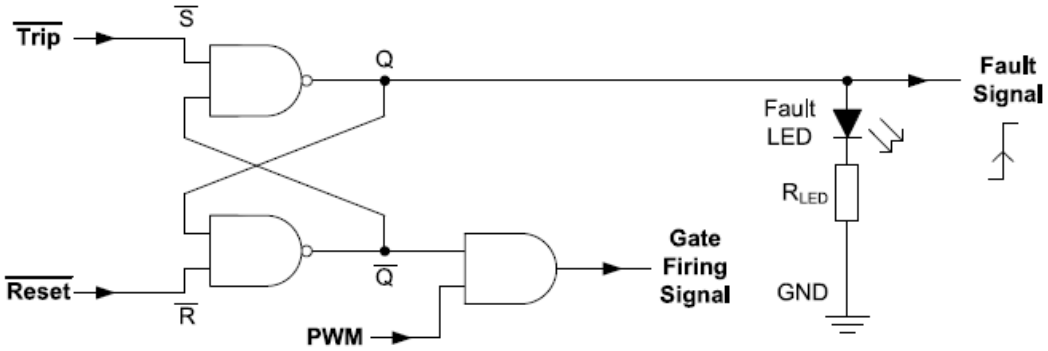
Once an over- or under-current condition is detected at the set thresholds, a fault voltage signal is triggered at the output. The upper and lower limit circuits are in OR configuration with a pull-up resistor R_{PU} to maintain the circuit in a low active state when the fault is triggered. The current limits are based on the current ratings of the converter. The resistor R_H in the positive feedback path provides a small amount of hysteresis to prevent instability around the point of output transition.



Current Limiter Circuit

Once an over current condition occurs, a latching circuit is used to retain the active low state and disconnect firing signals from the IGBT switches . To reset the circuit back to its active high state and back to normal operation, a Set/Reset (S/R) latch circuit comprising of two NAND gates and shown in the figure below is used. The set state results when the trip is detected $Q = 1$ and reset switch is at the zero position $\overline{Q} = 0$. Hence the

faults red LED on the power cell card is lit . Once reset state is toggled from the controller to its high state, the power cell card to its normal operating condition with $Q = 0$.



Over Current Protection Circuit

Appendix E
DSP and FPGA Register Allocation

DPR0_1 0xA0000000;

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Read	PPD															
Write	PPD															

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	PRS	PEN	ADM	CIP	ADM	ZFR			PWR	0		RTR	MEN	SMC	SMB	SMA
Write	PRS	PEN	ADM	CIP	ADM	ZFR			PWR	AST				SMC	S MB	SMA

PPD	PWM_PERIOD	0xFFFF – (desired time - 1 clock cycle)
PRS	PWM_RESET	Active High
PEN	PWM_ENABLE	Active High
PFL	PWM_FIFO_LEVEL	
PWR	Power on reset	Active low - temporary
CIP	Current Direction Input Polarity	0 = Active Low, 1 = Active High
ZFR	Encoder zero pulse polarity 0 = reset on rising edge, 1 – reset on falling edge	
ADM	A2D multiplex	0 = software driven 1=pwm interupt driven.
AST	A2D Converter Start	Active High
SMA	State Machine A enable	Active High
SMB	State Machine B enable	Active High
SMC	State Machine C enable	Active High
RTR	reset trip button state	Active low
MEN	Enable button state	

DPR1_1 0xA0000100;

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Read	LOT	DOS	SDAr	SCLr	TEM	C										
Write	PVE															

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	UI7	UI6	UI5	UI4	UI3	UI2	UI1	UI0	ABY	CINC	CINB	CINA	PFU	PEM	PAE	PAF
Write	PVT															

LOT Loss of Tracking (from Resolver)-
DOS Degradation of Signal (from Resolver)

PVE	PWM_VECTOR	
PVT	PWM_VECTOR_TIME	
PAF	PWM_FIFO_Almost Full	No. of words in FIFO > 250, Active High
PAE	PWM_FIFO Almost Empty	No. of words in FIFO ≤ 2, Active High
PEM	PWM_FIFO_EMPTY	Active High
PFU	PWM_FIFO_FULL	Active High
CINA	Current Direction Input, PhaseA	Active High
CINB	Current Direction Input, PhaseB	Active High
CINC	Current Direction Input, PhaseC	Active High
ABY	A2D converters Busy	1 = Busy
UI1-7	User input 1 to 7	
TEM C	temperature input C, 12 bit	
SCLr	I2C Serial clock line (bit used to read bus)	
SDAr	I2C Serial Data / Address line (bit used to read bus)	

DPR2_1 0xA0000200;

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Read	SDAw	SCLw												PSC gen_ sload	PSC gen_ CLR	PSC gen_ EN
Write	SDAw	SCLw												PSC gen_ sload	PSC gen_ CLR	PSC gen_ EN

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	EN5	EN4	EN3	EN2	EN1	ENBL	RDVL	SEL	DATAA							
Write	EN5	EN4	EN3	EN2	EN1	ENBL	RDVL	SEL	DATAA							

RDVL to select between angular position and velocity registers, RDVL is held **high** for angular position
RDVL is held **low** for angular velocity
EN0 – EN5 Enable signals for the output PWM, active high
SEL Select pin for PWM source, 0 standard PWM, 1 Space Vector PWM
DATAA Dead Time Value

SCLw I2C Serial clock line (bit used to drive bus)
SDAw I2C Serial Data / Address line (bit used to drive bus)

PSCgen_EN PSCgen enable, port 1, active HIGH
PSCgen_CLR PSCgen clear, port 1, active LOW
ENBL Enable signal for the output PWM, port 1, active HIGH

DPR3_1 0xA0000300;

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Read	AD1															
Write																

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	AD0															
Write																

DPR4_1 0xA0000400;

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Read	AD3															
Write																

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	AD2															
Write																

AD2 A2D Data, Channel 2
AD3 A2D Data, Channel 3

DPR5_1 0xA0000500;

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Read	AD5															
Write																

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	AD4															
Write																

AD4 A2D Data, Channel 4
AD5 A2D Data, Channel 5

DPR6_1 0xA0000600;

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Read	AD7															
Write																

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	AD6															
Write																

AD6 A2D Data, Channel 6
AD7 A2D Data, Channel 7

DPR7_1 0xA0000700;

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Read	AD9															
Write																

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	AD8															
Write																

AD8 A2D Data, Channel 8
AD9 A2D Data, Channel 9

DPR8_1 0xA0000800;

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Read	HT23	HT22	HT21	HT20	HT19	HT18	HT17	HT16	HT15	HT14	HT13	HT12	HT11	HT10	HT9	HT8
Write																

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	HT7	HT6	HT5	HT4	HT3	HT2	HT1	HT0	ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0
Write									ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0

ST0 – ST15	Software Trip	Active High
HT0 – HT15	Hardwareware Trip	Active High

HT0	FIFO empty trip
HT1	Watchdog Trip
HT2	Channel 0 trip
HT3	Channel 1 trip
HT4	Channel 2 trip
HT5	Channel 3 trip
HT6	Channel 4 trip
HT7	Channel 5 trip
HT8	Channel 6 trip
HT9	Channel 7 trip
HT10	Channel 8 trip
HT11	Channel 9a trip
HT12	Channel 9b trip
HT13	Clamp over stress
HT14	External trip 2
HT15	PWM FIFO Full
HT22	External trip
HT23	Clamp Over Voltage
HT16	Loss of Signal (from Resolver)
HT17	Degradation of Signal (from Resolver)
HT18	Loss of Tracking (from Resolver)

DPR9_1 0xA0000900;

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Read															WEN	0
Write															WEN	W8R

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	W_PERIOD															
Write	W_PERIOD															

W_PERIOD	Watchdog Period Register	Period = 0xFFFF – W_PERIOD
WSR	Watchdog Service	Active High
WEN	Watchdog Enable	Active High
	User Input 1	Active High

DPR10_1 0xA0000A00;

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Read									TEM	B						
Write																

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read					TEM	A										
Write																

TEM A	Temperature channel A
TEM B	Temperature channel B

DPR11_1 0xA0000B00;

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Read	DTD								UTD							
Write	DTD								UTD							

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	CTT															
Write	CTT															

CTT	Clamp trip time	sets counter trip level based on counter divisors below
UTD	Up time divider	Sets Up counter period = FPGAclock period / UTD+1
DTD	Down timeme divider	Sets down counter period = FPGAclock period / DTD+1

DPR12_1 0xA0000C00;

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Read	TE23	TE22	TE21	TE20	TE19	TE18	TE17	TE16	TE15	TE14	TE13	TE12	TE11	TE10	TE9	TE8
Write	TE23	TE22	TE21	TE20	TE19	TE18	TE17	TE16	TE15	TE14	TE13	TE12	TE11	TE10	TE9	TE8

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	TE7	TE6	TE5	TE4	TE3	TE2	TE1	TE0								
Write	TE7	TE6	TE5	TE4	TE3	TE2	TE1	TE0								

TE = trip enable, number = hardware trip channel, 0 = enable, 1 = dissabled

DPR13_1 0xA0000D00;

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Read	POS	RAW														
Write	Data_0															

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	POS	LAT														
Write																

POS RAW	raw encoder position	Instantaneous value from the quadrature encoder interface
POS LAT	Latched encoder position	Value from encoder interfaced, but latched on PWM interrupt
Data_0	32 bit for pwm_out[0]	

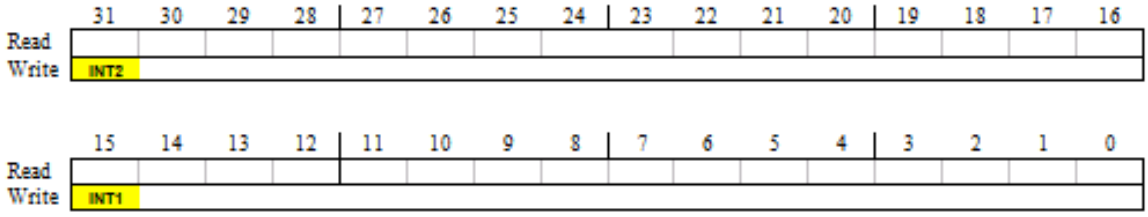
DPR14_1 0xA0000E00;

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Read																
Write	UP LIM															

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read																
Write	LOW LIM															

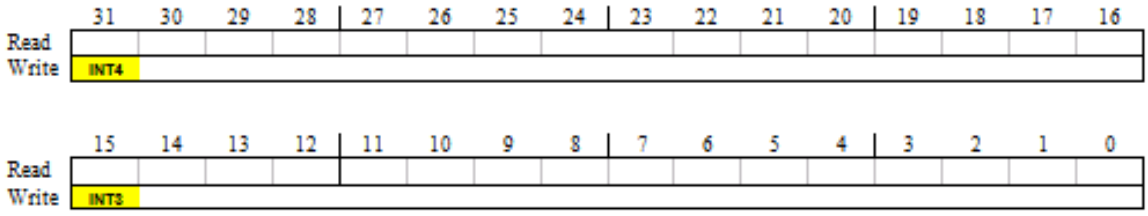
Data_1 32_bit for pwm_out[1]

DPR15_1 0xA0000F00;



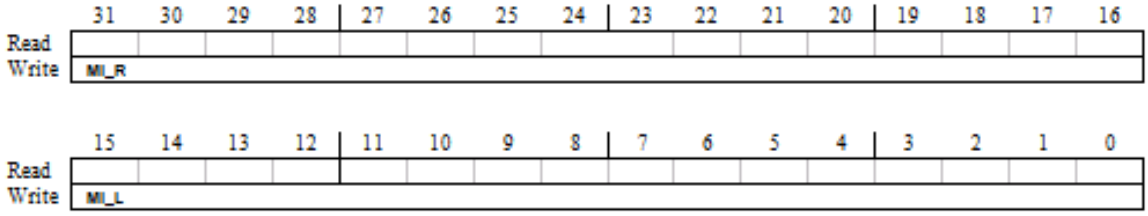
Data_2 32_bit for pwm_out[2]

DPR16_1 0xA0001000;



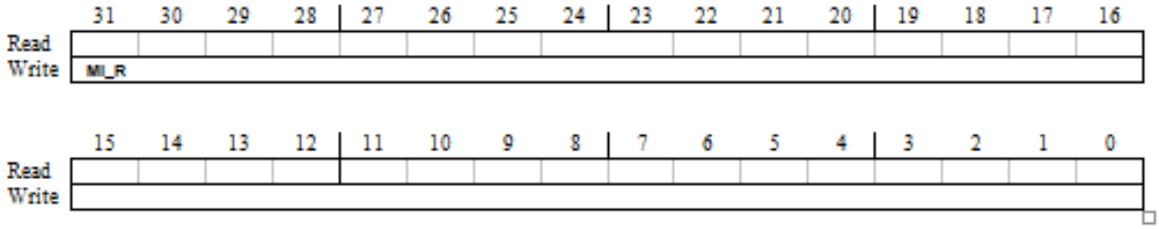
Data_3 32_bit for pwm_out[3]

DPR17_1 0xA0001100;



MI_R 16-bit modulation index for right leg of 1st cell in phase A
MI_L 16-bit modulation index for left leg of 1st cell in phase A

DPR18_1 0xA0001200;



MI_R 16-bit modulation index for right leg of 2nd cell in phase A
MI_L 16-bit modulation index for left leg of 2nd cell in phase A

DPR19_1 0x A0001300;

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Read																
Write	MI_R															

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read																
Write																

MI_R 16-bit modulation index for right leg of 3rd cell in phase A
MI_L 16-bit modulation index for left leg of 3rd cell in phase A

DPR20_1 0xA0001400;

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Read																
Write	LC3								LC2							

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read																
Write	LC1								LC0							

LC0 LED Character 0
LC1 LED Character 1
LC2 LED Character 2
LC3 LED Character 3

DPR21_1 0xA0001500;

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Read																
Write																

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read													LRS	AUD		
Write													LRS	AUD		

AUD LED Auxiliary data for programming bit pattern
LRS LED RS pin state.

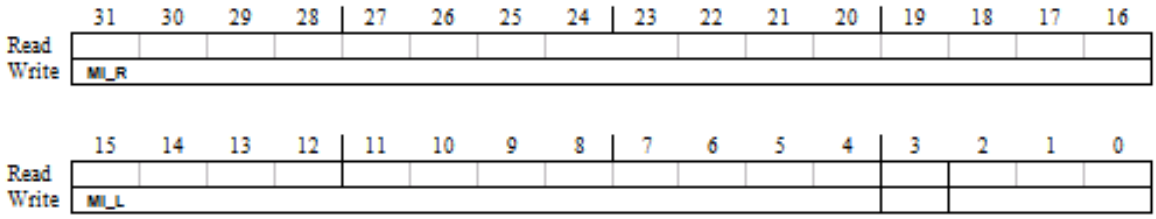
DPR22_1 0xA0001600;

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Read																
Write	MI_R															

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read																
Write	MI_L															

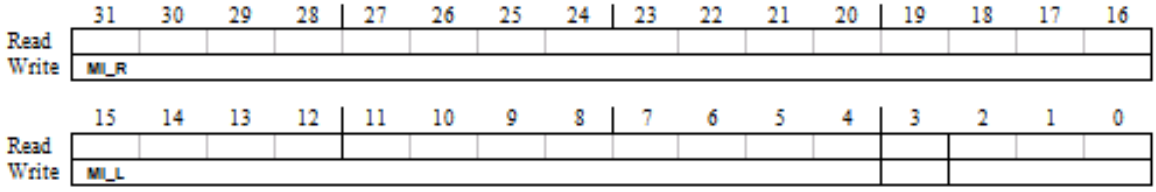
MI_R 16-bit modulation index for right leg of 4th cell in phase A
MI_L 16-bit modulation index for left leg of 4th cell in phase A

DPR23_1 0xA0001700;



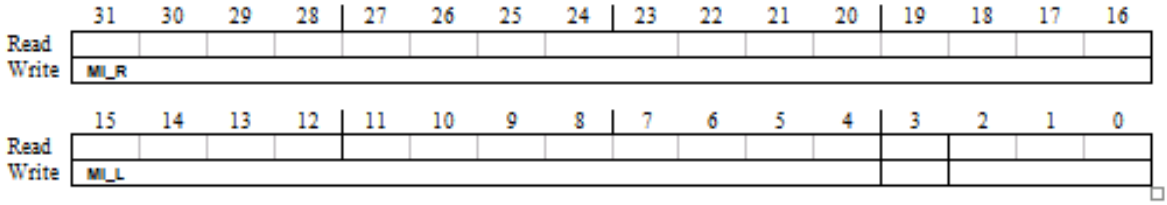
MI_R 16-bit modulation index for right leg of 1st cell in phase B
MI_L 16-bit modulation index for left leg of 1st cell in phase B

DPR24_1 0xA0001800;



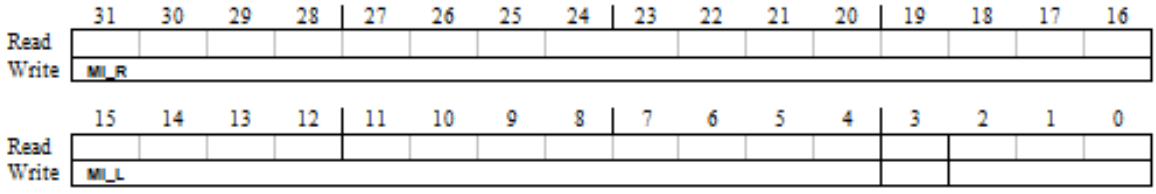
MI_R 16-bit modulation index for right leg of 2nd cell in phase B
MI_L 16-bit modulation index for left leg of 2nd cell in phase B

DPR25_1 0xA0001900;



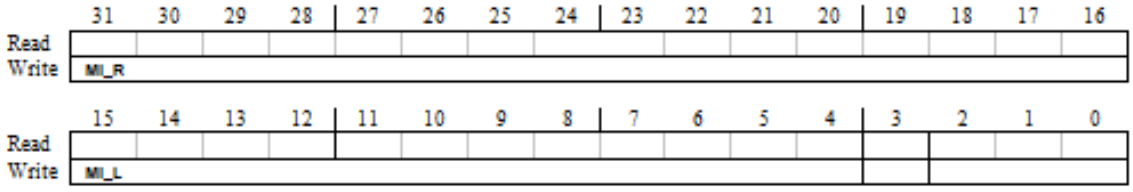
MI_R 16-bit modulation index for right leg of 3rd cell in phase B
MI_L 16-bit modulation index for left leg of 3rd cell in phase B

DPR26_1 0xA0001A00;



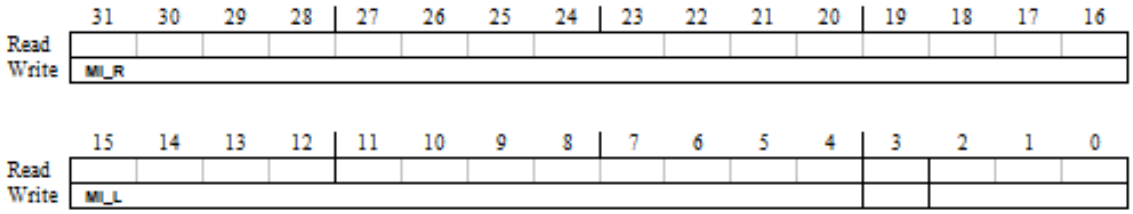
MI_R 16-bit modulation index for right leg of 4th cell in phase B
MI_L 16-bit modulation index for left leg of 4th cell in phase B

DPR27_1 0xA0001B00;



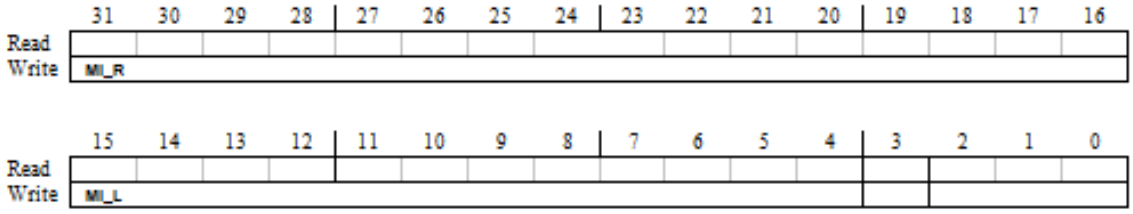
MI_R 16-bit modulation index for right leg of 1st cell in phase C
MI_L 16-bit modulation index for left leg of 1st cell in phase C

DPR28_1 0xA0001C00;



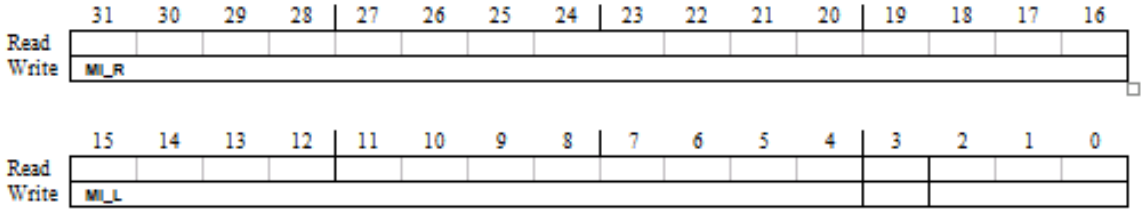
MI_R 16-bit modulation index for right leg of 2nd cell in phase C
MI_L 16-bit modulation index for left leg of 2nd cell in phase C

DPR29_1 0xA0001D00;



MI_R 16-bit modulation index for right leg of 3rd cell in phase C
MI_L 16-bit modulation index for left leg of 3rd cell in phase C

DPR30_1 0xA0001E00;



MI_R 16-bit modulation index for right leg of 4th cell in phase C
MI_L 16-bit modulation index for left leg of 4th cell in phase C