



THE DESIGN OF HIGH EFFICIENCY POWER AMPLIFIERS FOR IN-CAR AUDIO USE

By

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Abstract

Switched mode, Class-D power amplification allows for high efficiency power amplification of an audio signal. This thesis investigates its application to high power car audio systems where there is a demand for efficient high power amplification. Examination of the present car audio power amplifiers, which comprise a switched mode power supply combined with a linear output stage, has shown that there is significant scope for improvement in efficiency and power density.

A novel power stage in which the attributes of a switched-mode power supply and full bridge output stage is presented. It is demonstrated that elimination of the intermediate DC supply results in an amplifier which has a significantly lower part count, size and cost compared to conventional designs.

Two different modulation schemes are explored (PWM and PDM) with a view to finding the most suitable for the new power stage. The theoretical performances of the modulators are verified by practical measurements. The design of high order Delta-Sigma modulators is difficult as they show unstable behaviour and an alternative design methodology has been presented to ease this task.

The mechanisms which introduce distortion in a practical amplifier are discussed, and for the case of a PWM driven output stage, a new model is presented to predict the effect of dead time on harmonic distortion. This form of distortion is shown to be the dominant cause of open loop non-linearity. The use of feedback is also investigated and yields a factor of 20 improvement in amplifier total harmonic distortion.

The design throughout has been supported with practical results and these have illustrated the importance for careful circuit layout in high frequency switching systems.

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1 Introduction

The advent of the compact disc in 1983 has heralded a rapid progression in the application of digital audio techniques to consumer products. Digital audio storage and transmission is now commonplace (digital TV, DVD, Minidisk etc) and has brought benefits such as increased dynamic range and low noise floors.

Although the use of digital technology has revolutionised consumer audio, one part of the audio chain which has remained largely unchanged is the conventional analogue technology used for final audio power amplification. Most consumer audio power amplifiers have power ratings of a few tens of Watts and heat generated by the use of linear amplifiers for such applications is easily dissipated. However, for applications where conversion efficiency is paramount (e.g. portable battery powered equipment), linear technology is not suitable or where high power output is required, the amplifiers tend to be large and dissipate excessive heat.

Digital or, Class-D power amplifiers, first suggested by Baxandall [1.1], use output transistors in a high frequency switching manner with the audio information being conveyed in the timing of the switching events. This approach offers three main advantages over the more conventional linear technique.

- The use of the power handling devices in an on or off state offers a significant increase in power conversion efficiency over linear amplifiers.
- The entire power conversion process (up to the switching drive signals) can be undertaken digitally and this offers improvements in the amplifier fidelity similar to those seen with compact disc (very low distortion and signal to noise ratio).
- Digital circuitry requires no set-up steps (e.g. bias setting) which can make the production of digital amplifiers cheaper.

In high-power audio amplifier systems, it is the increase in conversion efficiency that makes the use of Class-D amplifiers attractive. Indeed, Class-D amplifiers are now commonplace in commercial PA systems [1.2] where the power rating is of the order of kilowatts. These systems use analogue modulation techniques to control the switching transistors and thus offer similar fidelity performance to their linear counterparts at very much higher conversion efficiency.

This thesis is concerned with the use of Class-D techniques for in-car audio where there is a particular requirement for high efficiency since the power is drawn from a limited energy low voltage supply. A novel class-D structure in which the intermediate DC supply is eliminated is described in detail. A new model enabling accurate prediction of dead time distortion in PWM modulated class-D systems is also presented.

1.1 In-Car Audio Power Amplifiers

In the USA in recent years, the market need for high power car audio amplification has grown with ever increasing demands on power and performance. A number of manufacturers [1.3, 1.4, 1.5] commercially produce in-car power amplifiers with ratings up to 500W per channel, and an example of one of these is shown in Figure 1.1. These units tend to be physically large and can run very hot. A typical state of the art amplifier utilises a linear output stage driven by a switched-mode power supply (SMPS) as shown in Figure 1.2. The SMPS is used to boost the 12V DC voltage from the car battery to the $\sim\pm 50\text{V}$ required by the linear output stage. To maintain a reasonable efficiency, the switching elements forming the primary side bridge circuit are realised with paralleled MOSFETs to keep the conduction loss to a minimum. In the linear amplifier section, many paralleled bipolar devices are again used in order to dissipate the losses over a large silicon area to limit the maximum operating temperatures.

Typically, the amplifier is mounted inside the car boot where the ambient temperature can be relatively high. The linear technology used in the conventional output stage is inefficient and although the amplifier contains thermal protection, it is likely to cut out before full continuous power output is achieved. Furthermore, since the amplifier power source is a battery, energy wasted as heat will cause an additional load on the car electrical system and will compromise the operating time of the amplifier. An additional alternator may be required to ensure an adequate electrical supply for the amplifier.

The efficiency of the overall amplifier will be the combined efficiencies of the power supply and the linear output stage. The efficiency of the power supply in the amplifier of Figure 1.2 was measured by disconnecting the linear output stage and loading the positive power rail with a variable load. The input voltage was maintained at a nominal 12V and Figure 1.3(a) shows the measured conversion efficiency as a function of the output power. Figure 1.3(b) shows the measured power loss in the SMPS. The input and output powers were measured using a high accuracy power analyser (see Appendix E).

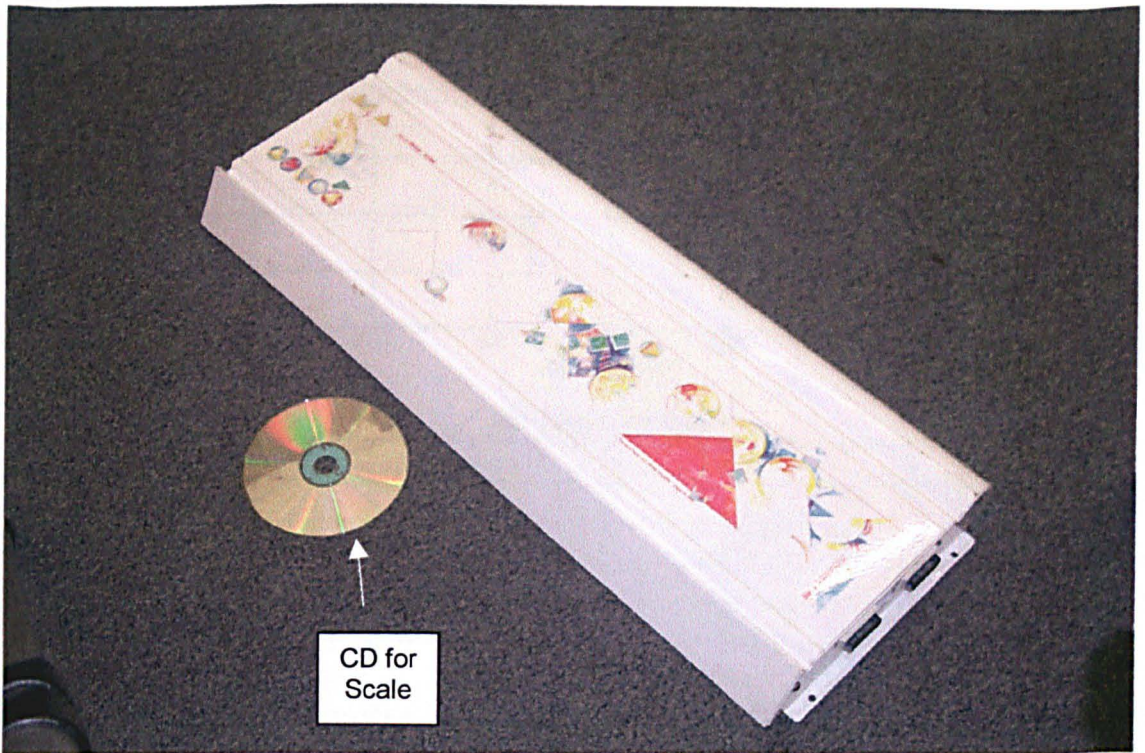


Figure 1.1 – Precision Power A1200 (500W per channel in-car audio amplifier)

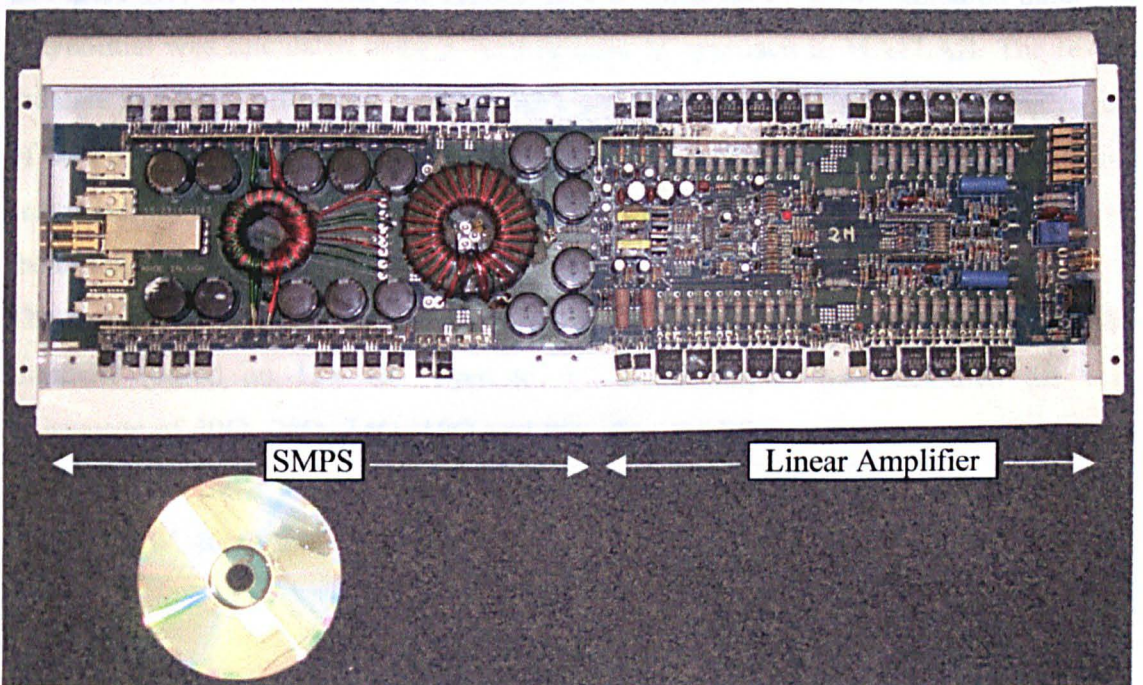


Figure 1.2 - Present in-car power amplifier circuitry (500W per channel)

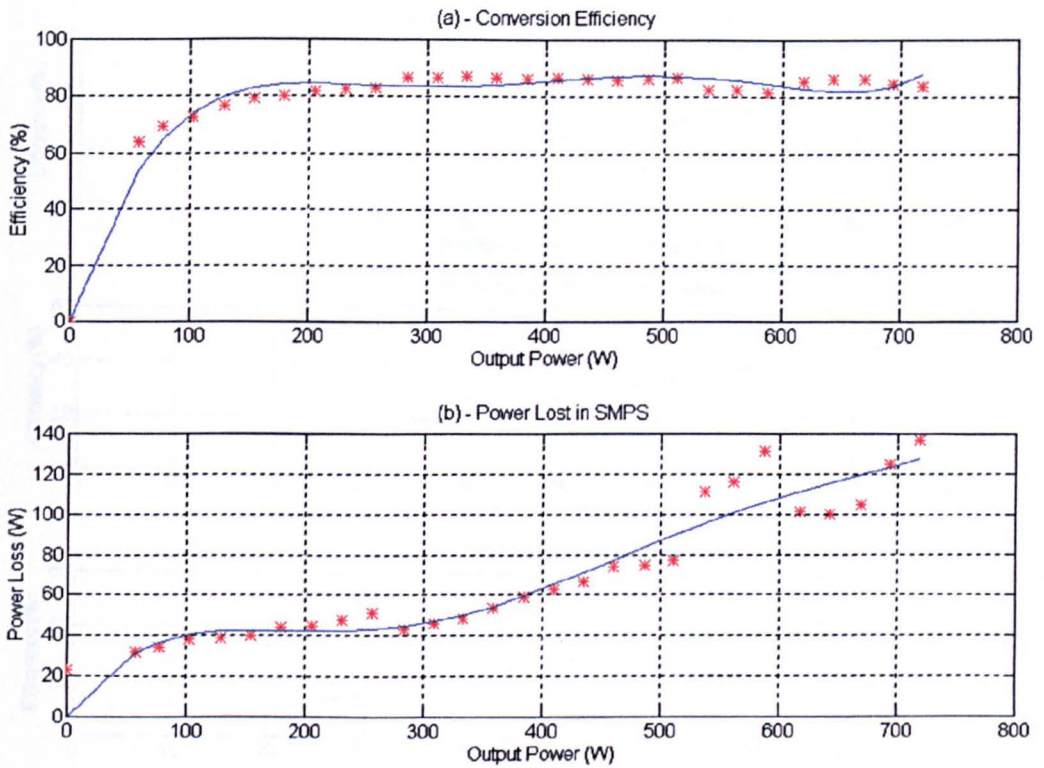
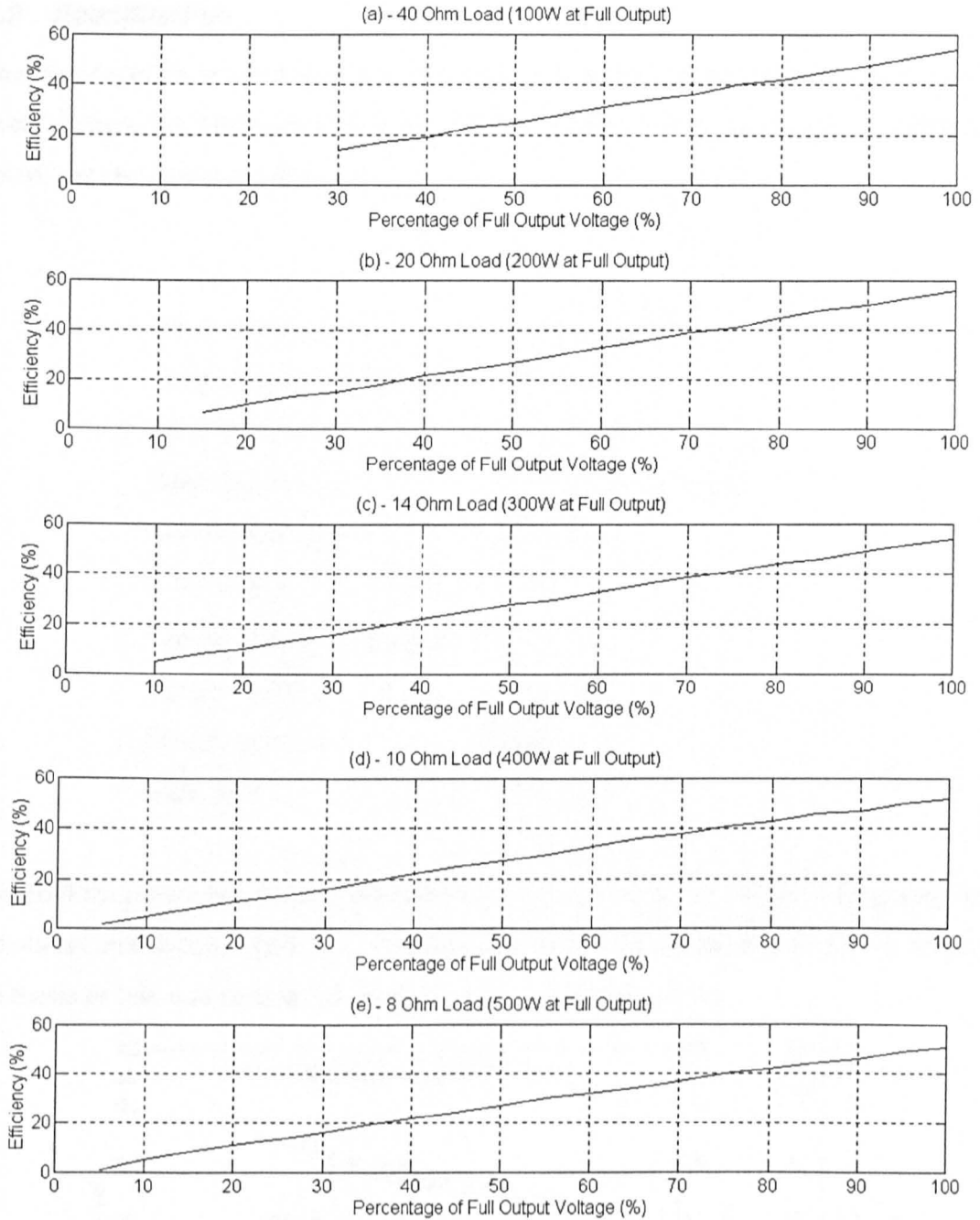


Figure 1.3 - Measured efficiency and power loss in the amplifier SMPS

In Figure 1.3, the solid blue line represents a polynomial fit to the measured data. The polynomial was calculated using a least squares fit approach in MATLAB. The results indicate an SMPS efficiency between 80% and 90% over most of the operating region of the power amplifier. Compared to the linear output stage, this efficiency is very high and therefore the overall amplifier conversion efficiency is likely to be dominated by the efficiency of the linear output stage.

The linear output stage was reconnected and the total conversion efficiency of the amplifier (based on 12V DC input to AC audio output) was measured for load resistances of 40 Ω , 20 Ω , 14 Ω , 10 Ω and 8 Ω . The amplifier was configured in bridged mode and for these load resistances, the power outputs at full 90V peak are 100W, 200W, 300W, 400W and 500W respectively, Figure 1.4.



Efficiency based on sinewave output into a unity power factor load

Figure 1.4 - Conversion efficiencies of full amplifier system

As would be expected, the overall conversion efficiency is relatively independent of the load resistance used. The profiles confirm that the linear amplifier has a significant impact on overall efficiency and at best, the amplifier is 50% efficient.

1.2 Specification

The target specification of the Class-D system is based on the specifications of a present linear design, the Precision Power PC21400 amplifier, which is capable of delivering 350W per channel into a 4Ω load.

Power Bandwidth	4.5Hz – 100kHz
Total Harmonic Distortion	0.02%
Input Topology	Differential
Input Sensitivity	150mV – 12V RMS
Input Impedance	10k
Load Impedance (stereo)	2-8Ω
Load Impedance (bridged)	4-8Ω
Supply Voltage	11-15V
Damping Factor	>500
Slew Rate	>50V/μs

The 100kHz power bandwidth presented above is excessive when the hearing area of a human is considered, Figure 1.5. A bandwidth of 20kHz was stipulated for the work in the thesis as this was considered adequate for a car audio system.

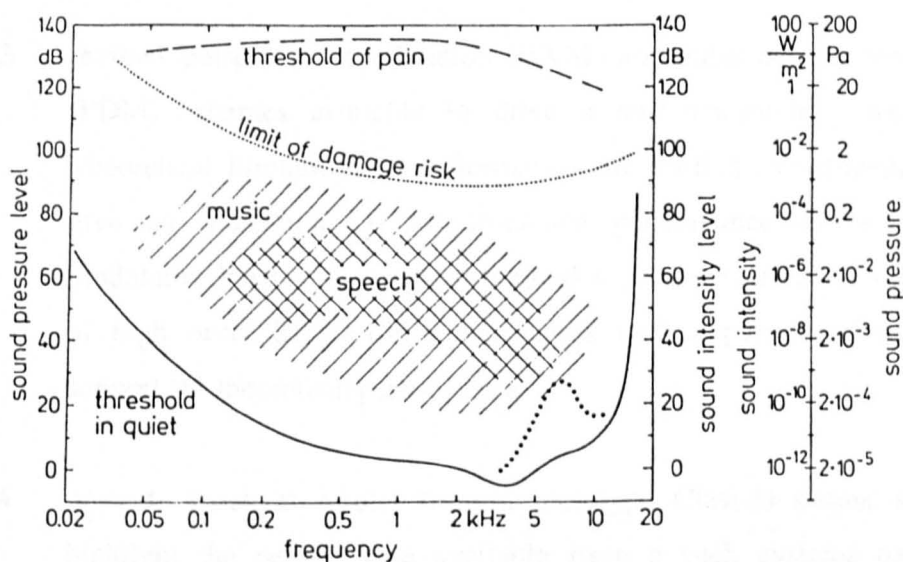


Figure 1.5 - Hearing area for a typical adult human (Source - [1.6])

The figure shows that most humans can only perceive frequencies up to 14kHz although the argument for high power bandwidth can be supported through subjective testing.

The target and harmonic distortion figure was also relaxed to 0.1%. Although this is poorer than the 0.02% offered by the linear amplifier, it is deemed that this is acceptable for in car audio use. Also, the equipment available to measure the spectral content of the amplifier has a dynamic range of 70dB which is close to the required 60dB range required to measure 0.1% distortion.

1.3 Research Overview

The thesis investigates the development of a high efficiency Class-D amplifier system for in-car audio use. The aim is to produce a system with much higher conversion efficiency than the present linear system and simultaneously reduce the part count. This will lead to a system with higher power density and lower cost.

Chapter 2 provides an overview of the operation of both linear and conventional switched-mode amplifier systems. In particular, the factors affecting the operational efficiency of both these types of amplifiers will be discussed. This will give an indication of the likely improvement available through the implementation of switched-mode technology.

Chapter 3 reviews pulse width modulation (PWM) and pulse density modulation (PDM) schemes available to drive a switched-mode power stage. Theoretical limitations in performance are verified experimentally and give an indication of the attainable performance for a practical modulator. Furthermore, a new methodology is presented for the design of high order Sigma-Delta modulators with experimental results to support the theoretical performance.

Chapter 4 presents practical results from a prototype Class-D output stage to highlight the performance available from a such systems using the modulation technique discussed in chapter 3. In particular, the conversion efficiency is measured and shown to be significantly higher than a linear output stage. Much of the chapter is dedicated to an

investigation of distortion mechanisms within the power stage. Specifically, an analytical method of predicting the harmonic distortion caused by the necessary introduction of a dead time between the switching of the power devices in the output stage is discussed. The chapter concludes with a discussion of the methods available for the implementation of closed loop control to minimise harmonic distortion.

Chapter 5 proposes a new integrated power stage which combines the attributes of an SMPS and Class-D output stage and eliminates the need for an intermediate DC supply and associated filter components. The chapter discusses the development of the power stage and pertinent design issues to its successful operation. In particular, the importance of careful circuit layout to minimise parasitic effects and the use of planar magnetic circuits to minimise transformer leakage inductance are highlighted.

Chapter 6 gives the results of applying both PWM and PDM modulation strategies to the new power stage developed in Chapter 5. Two methods for partial soft switching are developed. Distortion mechanisms present in the new power stage are highlighted and supported with results taken for both open and closed operation. Finally, the operational efficiency of the complete converter is measured and possible improvements are discussed.

Figure 2.1 - Generic flow of power stage

2 Amplifier Operation

2.1 Introduction

At the heart of the power conversion process in an audio amplifier is application of the power transistor to allow a small signal to control a much larger power signal. There are a number of amplifier circuits available, which fall under one of two main categories: -

- Linear Amplifiers, in which the power transistor operates in its linear region
- Switching Amplifiers in which the power transistor operates in its switching states, i.e. saturated on or off.

This chapter reviews the general operation of both types of amplifier. More specifically, the factors affecting the efficiency of both types of amplifier are discussed and the linear amplifier operation is augmented with results from a prototype power stage. The practical operation of a switching amplifier is covered in Chapter 4.

2.2 Linear Operation

Although a large number of linear output stages have been developed, they are mostly based around the basic stage as shown in Figure 2.1. (The power stage is shown with BJT's although MOSFETs can also be used).

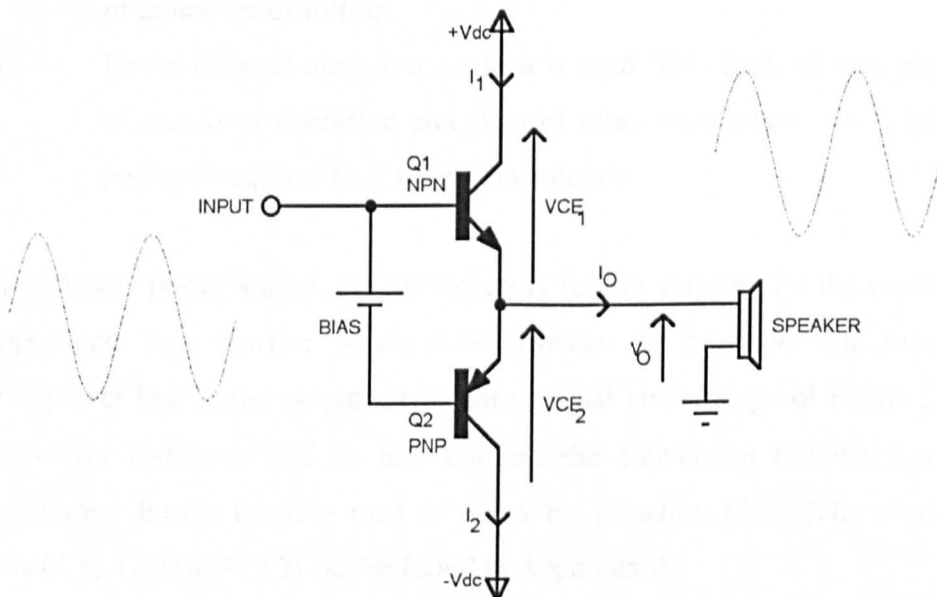


Figure 2.1 - Generic linear power stage

The power stage consists of two emitter-followers, one to provide positive output voltage and the other to provide negative output voltage. The transistors must be biased into conduction to reduce crossover distortion and the level of bias used in practice determines the class of the amplifier. There are four main classes of linear amplifiers and these are described below.

- Class-A** Under Class-A operation, both transistors always remain in conduction. To achieve this, the bias current must be set to be greater than the peak output current. The maximum efficiency of this power stage is therefore 50% and this is achieved for maximum sinewave output voltage into a purely resistive load. This class of operation offers the most linear output stage but suffers from very poor efficiency.
- Class-AB** Under Class-AB operation, the output transistors are biased slightly into conduction (typically a few tens of mA). This level of bias offers a greater operating efficiency than Class-A operation but suffers from poorer linearity. This class of operation is the most commonly used for audio output stages.
- Class-B** Under Class-B operation, the output transistors are biased to be just on the point of conduction. This offers an increase in efficiency of up to approximately 75% but the output stage can exhibit relatively high levels of crossover distortion.
- Class-C** Under Class-C operation, no bias is used. This leads to very high levels of crossover distortion and is most often used where very high output power is required (e.g. radio transmitters)

With these linear power stages, the efficiency is further reduced by the nature of the load impedance. Any reactive power flow between the amplifier and load causes additional power loss in the output stage. For an ideal power stage of Figure 2.1, with zero cross-over distortion and no bias current, the conversion efficiency, η , for a sinewave output into a reactive load is given by Equation (2.1) (The working for Equations (2.1), (2.2) and (2.3) can be found in Appendix A).

$$\eta = 25\pi \frac{V_P}{V_{DC}} \cos(\phi) \quad (2.1)$$

Where, V_P is the sinewave amplitude
 V_{DC} is the DC link supply voltage
 ϕ is the phase shift of the load.

Thus, peak efficiency occurs when the peak output voltage approaches the DC supply rails and when the load has unity power factor (i.e. is purely resistive). Similarly, the power lost in the output stage, P_L , can be found and is shown in Equation (2.2).

$$P_L = \frac{4V_P V_{DC} - V_P^2 \pi \cos(\phi)}{2\pi|Z|} \quad (2.2)$$

Where, $|Z|$ is the magnitude of the load impedance

The peak power loss in the linear power stage can be found through differentiation of (2.2) and exists over two ranges of power factor as shown in (2.3). The working can be found in appendix A.

$$P_{LOSS} \Big|_{MAX} = \begin{cases} \frac{2}{|Z| \cos(\phi)} \left(\frac{V_{DC}}{\pi} \right)^2 & \frac{2}{\pi} \leq \cos(\phi) \leq 1 \\ \frac{V_{DC}^2 (4 - \pi \cos(\phi))}{2\pi|Z|} & 0 \leq \cos(\phi) < \frac{2}{\pi} \end{cases} \quad (2.3)$$

Both the conversion efficiency and power loss are functions of the complex load impedance as well as the peak output voltage relative to the power supply rails. In practice, the impedance of a loudspeaker system will vary considerably over the design frequency range. A single electromagnetic drive unit will have electrical and mechanical resonance's and if a number of units are connected in parallel in combination with crossover networks to cover the full bandwidth, a complicated impedance will result.

The complex impedance of a 300W single low frequency (40Hz-2kHz) base drive unit, mounted in free air, is shown in Figure 2.2. It is evident that the magnitude of the impedance can vary significantly from the nominal 8Ω and the phase shift is as much as 50° . Using Equation (2.3), Figure 2.3 shows that this load impedance could result in a power loss of up to 40W for a 100W rated linear power stage.

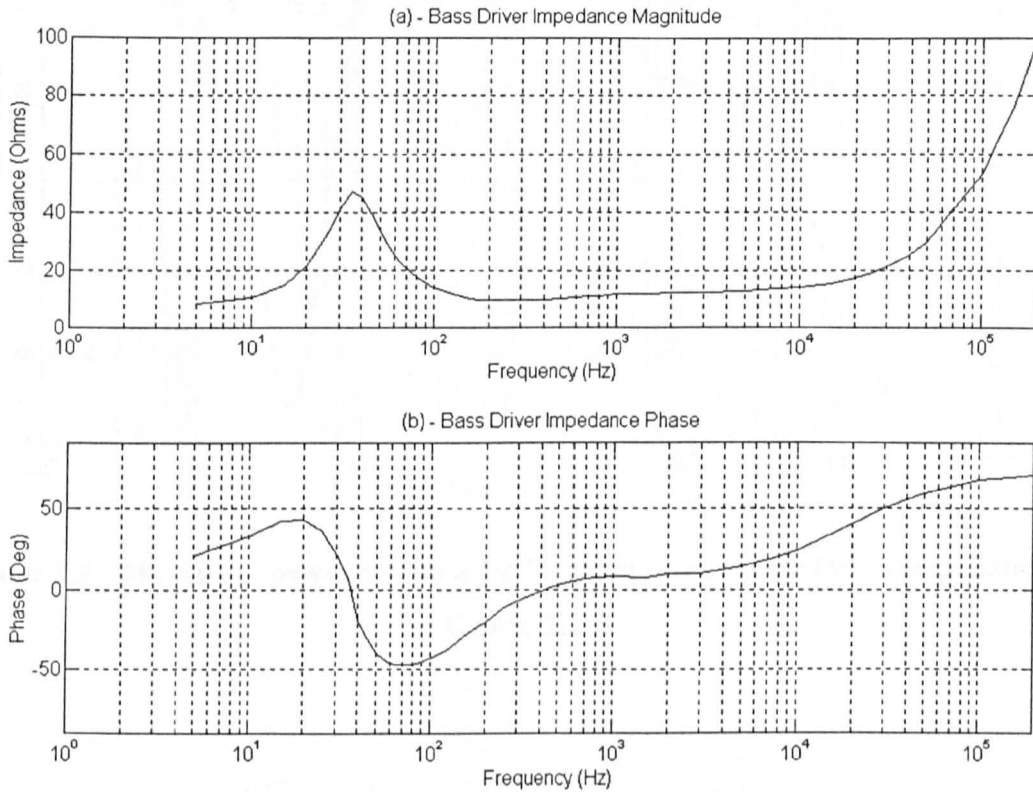


Figure 2.2 - Typical bass driver impedance profile

The band of frequencies up to 300Hz shows the largest phase shift over the useful band of the loudspeaker and Figure 2.4 plots the calculated efficiency profile over this range using the measured impedance data of Figure 2.2 and Equation (2.1). The profile shows that the large phase shift of the loudspeaker around resonance can drop the power stage efficiency by more than 20% although it is the peak output voltage relative to the DC rail voltage that has the largest effect on efficiency. To verify the calculated efficiency profile, the actual efficiency of a Class-B linear power stage was measured with the bass drive loudspeaker as a load as shown in Figure 2.5. The supply rails were set to $\pm 6V$ with a steady state bias current of 50mA.

A single drive unit is, however, not representative of a full range speaker system. In order to assess the impedance of a typical system, a three-way loudspeaker was constructed, Figure 2.6.

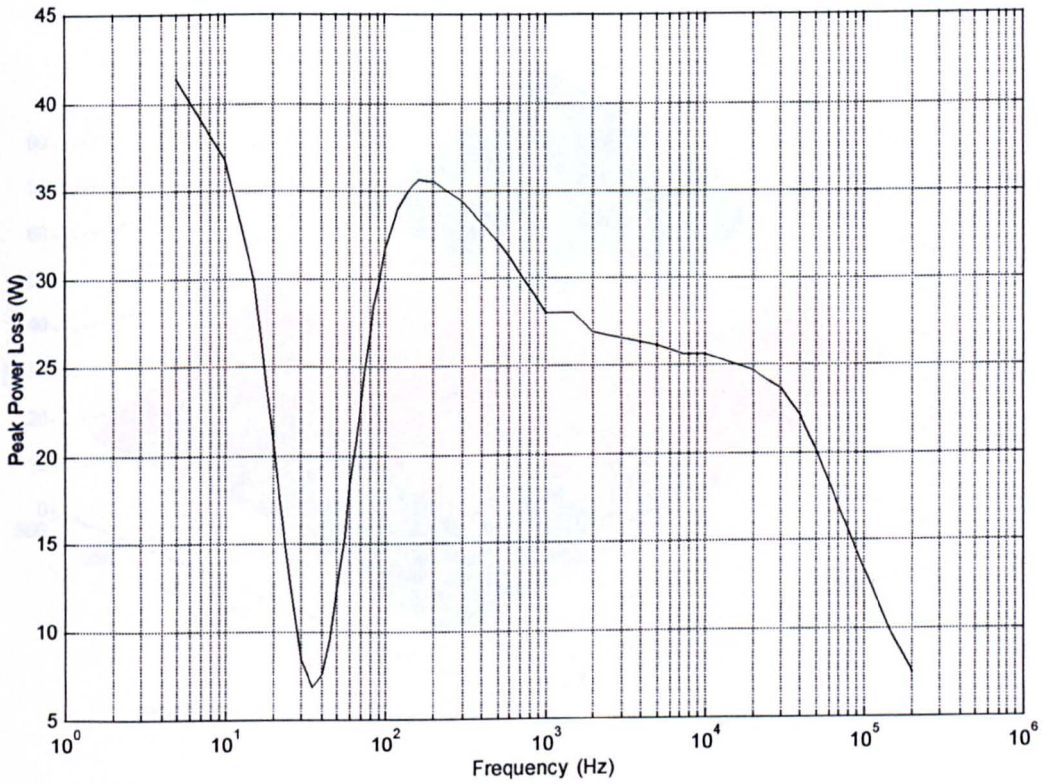


Figure 2.3 - Maximum power loss in a 100W rated power stage (With impedance of Figure 2.2)

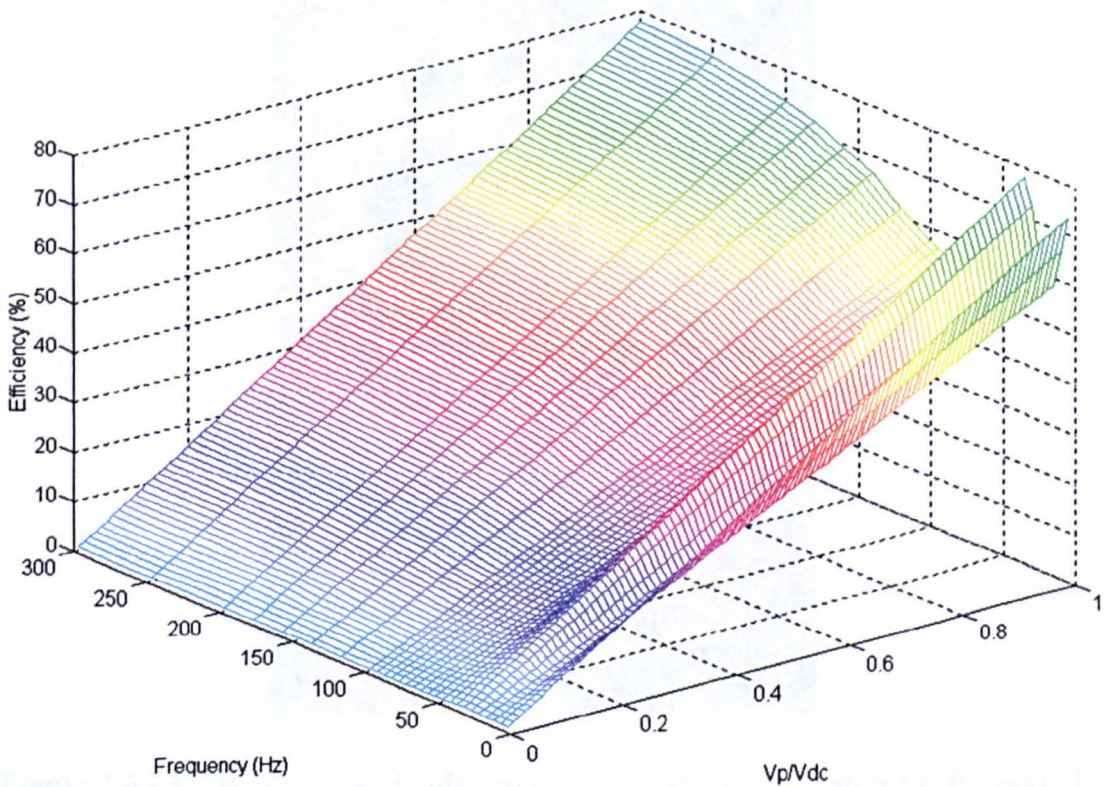


Figure 2.4 – Calculated efficiency profile for single bass driver

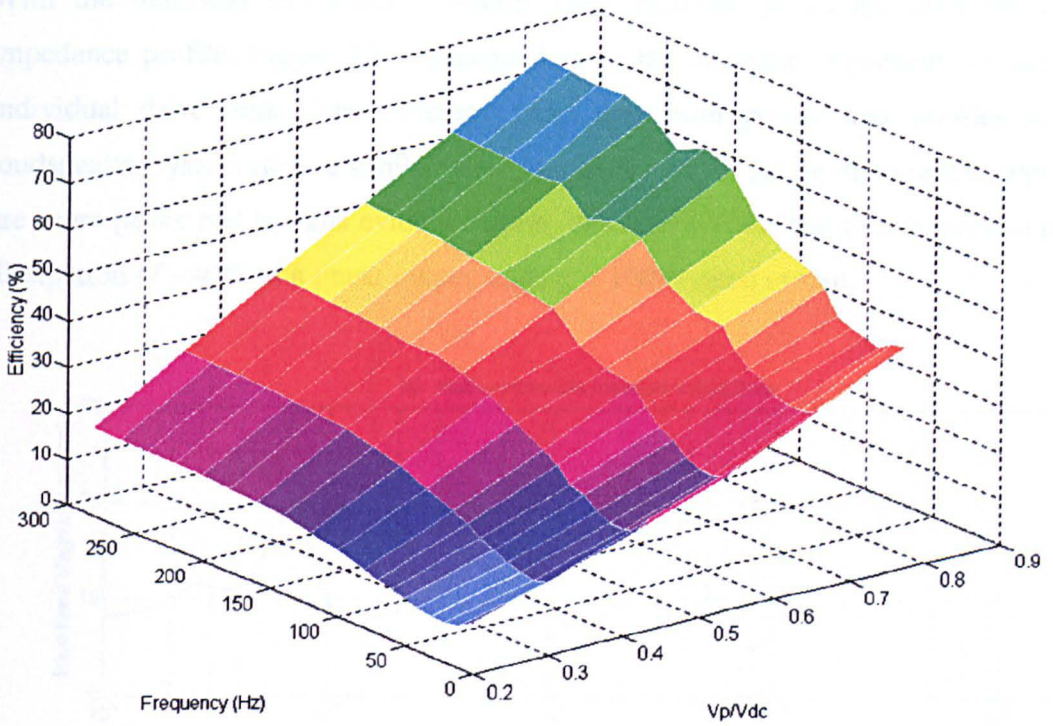


Figure 2.5 - Measured efficiency profile with single bass driver load



Figure 2.6 - 300W Multiway loudspeaker system (Fire extinguisher is for scale!)

With the multiway loudspeaker system, three resonant peaks are observed in the impedance profile, Figure 2.7, corresponding to the resonant frequencies of the three individual drive units. The efficiency and maximum power loss profiles for the loudspeaker system show a similar behaviour to that of the single drive unit except there are more peaks and troughs evident. Again, this load would lead to a maximum power dissipation of $\sim 40\text{W}$ in a linear output stage at a 100W rated output.

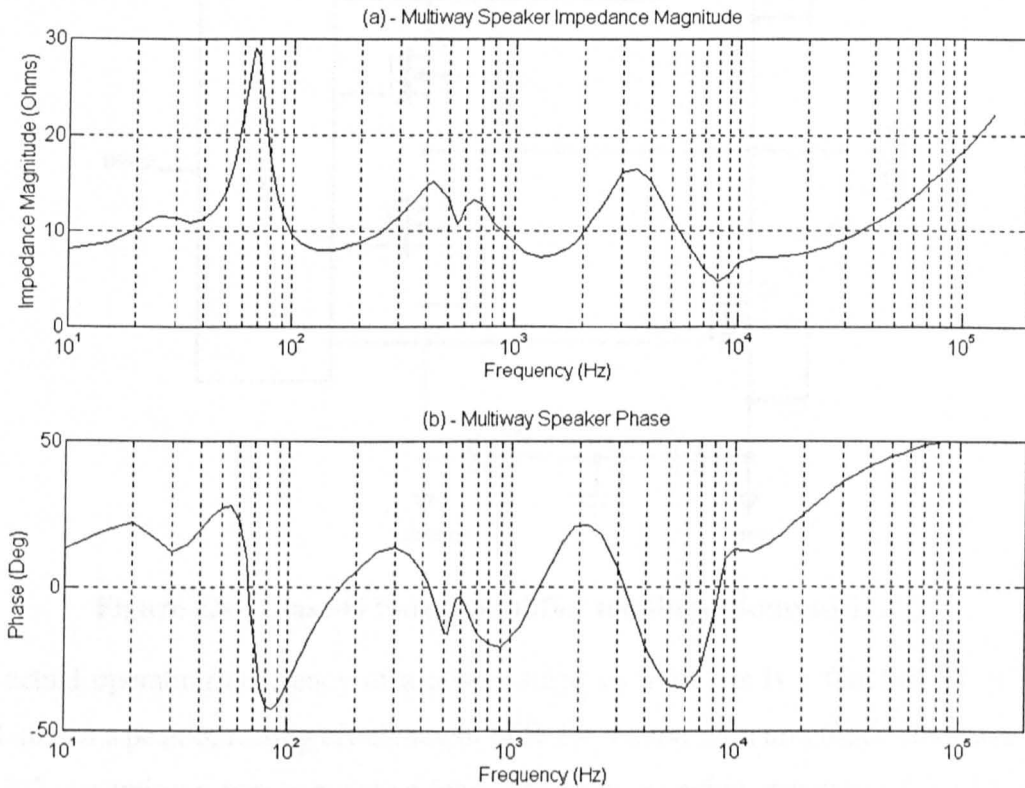


Figure 2.7 - Impedance profile for a multiway loudspeaker

The main cause of inefficiency is the potentially large voltage drop across the power devices when they are in conduction, which is maximised with a reactive load. One way of addressing this problem without resorting to the complexity of the Class-D approach was first developed by Hitachi in 1977 and is discussed by Raab [2.1]. This ‘Class-G’ approach uses two or more linear power stages operating in tandem with different supply voltages, Figure 2.8.

Devices Q3 and Q4 form a high power Class-B stage and are supplied from $\pm V_{dc}$ rails. Q1 and Q2 form a low power Class-B stage and are supplied from lower voltage

($\pm aV_{dc}$) rails where $a < 1$. Low output signal levels are driven by Q1 and Q2 whilst signals above aV_{dc} are driven by Q3 and Q4.

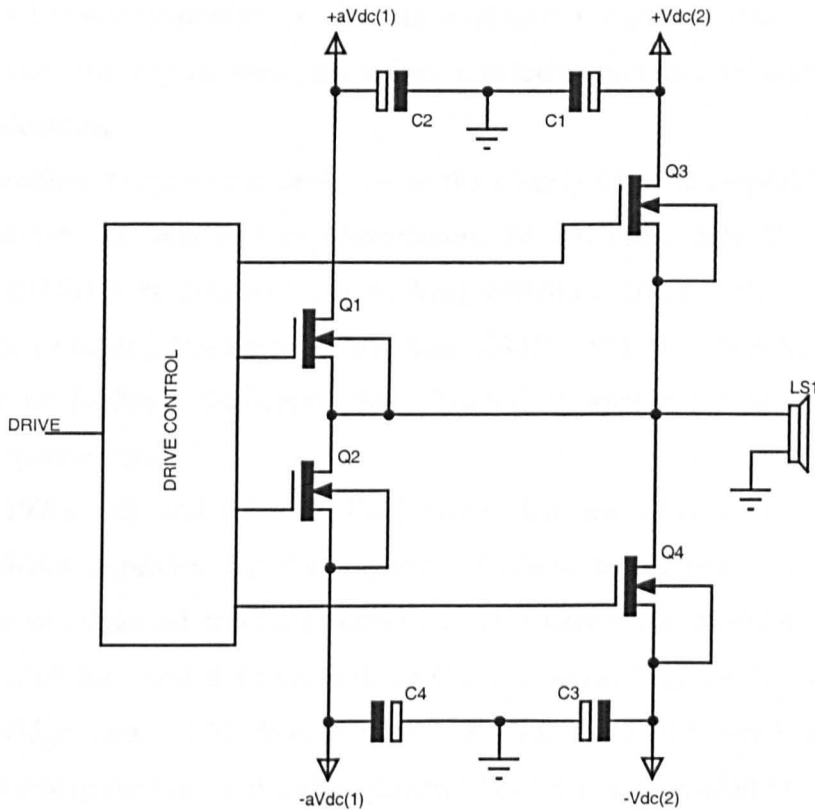


Figure 2.8 - Class-G linear amplifier topology (Source - [2.1])

The actual operating efficiency of a power stage such as this is a function of 'a' and [2.1] quotes a peak operating efficiency of 86% for a maximum amplitude sinewave and $a=0.707$, assuming a purely resistive load. The corresponding maximum for a Class-B stage is 78.5% (see Equation (2.1)). A further increase to 89% is possible for a Class-G stage consisting of three Class-B sections.

In reality, a music signal is not a pure sinewave but consists of relatively low signals with large transient peaks. Thus, the actual operating efficiency of a linear power stage is likely to be a good deal lower than the theoretical maximum.

Another method, conceived of by Soundcraft in 1977 and developed by Jensen [2.2], adapts the Class-G approach by actually modulating the voltage rail by the input signal. This technique, known as Class-H, allows for optimum efficiency in the output stage. Whilst offering improved efficiency, both Class-G and Class-H necessitate additional power supplies which can increase the system cost and complexity.

2.3 Switched-Mode Operation (Class-D)

The Class-D or switched-mode technique was first proposed by Baxandall in the early 1960s and led to the appearance of Class-D amplifiers for audio applications [2.3, 2.4, 2.5]. The poor linearity of these amplifiers restricted their use to high power, low fidelity applications.

The main problem faced by the designers of these early Class-D amplifiers was in the devices available for practical implementation. At the time, only Bipolar Junction Transistors (BJTs) were available and the long switching times of this type of device restricted the switching frequency to less than 50kHz. With this switching frequency, high levels of foldback distortion (See Chapter 3) appear in the baseband and compromise performance.

In the late 1970s Cuk and Erickson [2.6] explored a new Class-D topology using a coupled inductor approach but the majority of research has been focussed on the development of advanced feedback techniques and alternative modulation strategies. Indeed, some of the latest developments in Class-D technology are based around the simple H-Bridge stage [2.7]. Whilst very high fidelity digital amplifiers are now beginning to emerge in high-end audio systems [2.8] the main application area of digital amplifiers still remains in high power audio amplification. With operating efficiencies of between 80% and 90%, high power digital audio amplifiers can offer a substantially higher power density than their linear counterparts.

As the name suggests, switched-mode operation utilises the output power devices in either their fully saturated or cut-off state. In addition to the inherently higher conversion efficiency due to the switching action, the regenerative energy associated with a reactive load is returned to the DC link rails rather than being dissipated.

2.3.1 Topologies

Two main topologies are used to achieve the power amplification, namely the voltage source half bridge converter and the full bridge converter as shown in Figure 2.9. With the half bridge converter, a positive pulse from the modulator switches SW1 on and SW2 off placing a voltage of $+V_{dc}$ across the filter input and vice versa for $-V_{dc}$. The full bridge converter operates in much the same manner with SW1 and SW4 and SW2 and SW3 operated in tandem to place a voltage of $\pm V_{dc}$ across the filter.

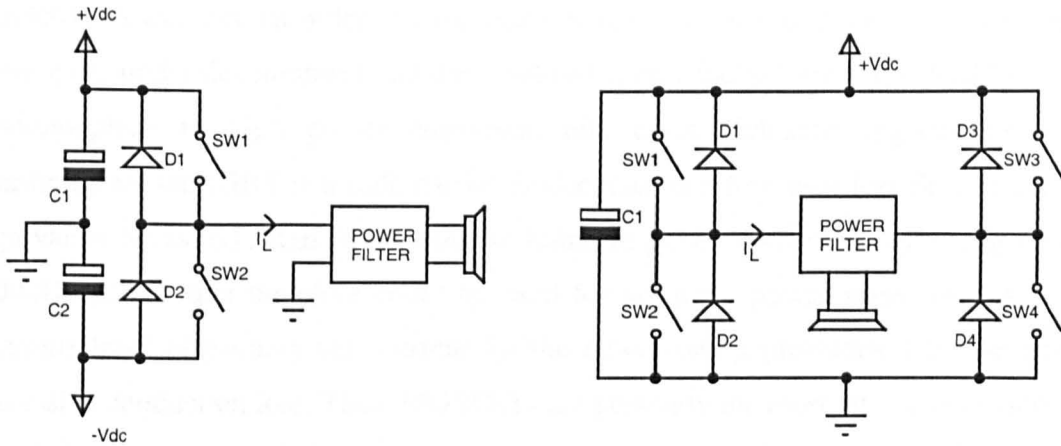


Figure 2.9 – Half bridge (left) and full bridge (right) topologies

Of the half and full bridge configurations, it would seem that the half bridge converter is superior to the full bridge due to its relative simplicity with half the number of semiconductor devices. However, in [2.9], Lai and Smedley point out that the half-bridge topology is only suitable at low power since the existence of a DC component at the center point of the two switches will lead to a DC component in the load current, I_L . When this occurs, and SW1 is on, C1 is discharged. However, when SW1 is turned off and SW2 is turned on, the same direction of current will charge up C2. Since the DC links can normally only supply power in one quadrant, this charging action will tend to cause an imbalance in the supply voltages. Lai and Smedley go on to suggest that even if a DC component doesn't exist at the center point, a low frequency component in the signal will lead to excessive power supply ripple. Although this problem could be solved by simply designing a 2-quadrant capability into the power supplies, the full bridge converter is less sensitive to this problem and therefore represents a better choice at high power levels. Furthermore, the full bridge operation allows for twice the peak output voltage from the amplifier, compared to a single ended power stage with the same power supply.

2.3.2 Device Choice

The power switches in either of the above converter topologies can be realised with any active semiconductor switch and the choice of device technology depends on the specific requirements of the amplifier. The most suitable device is the one that offers lowest conduction loss, the fastest switching time and the lowest drive requirements. Early Class-D amplifiers used BJTs [2.5], however, developments in device technology have made the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) a more

attractive device due an order of magnitude increase in switching speed. New types of device are under development and the Insulated Gate Bipolar Transistor (IGBT) is now commonplace in high power converters due to its inherent rugged behaviour. Furthermore, the IGBT is a bulk carrier device and therefore uses less Silicon than an equivalent MOSFET. IGBTs can now be found in power converters switching at over 100kHz [2.10], and therefore could be used for an audio power stage. However, the extreme level of primary side current for the power rating precludes their use due to excessive conduction loss. Thus, MOSFETs are presently the most attractive devices for a switching audio power stage.

2.3.3 Loss Mechanisms

Loss in a Class-D output stage can be encountered in a number of ways: -

- Switching loss in the power devices
- Conduction loss in the power devices
- Loss in the power device drive circuitry
- Loss in the passive power filter components
- High frequency loss in the loudspeaker caused by the presence of switching frequency components.

Correct design of the power filter will minimise loss in the filter and high frequency loss in the loudspeaker. Loss in the gate drive circuitry is likely to be small compared to the switching and conduction loss and only affects efficiency at low power outputs. Thus, the dominant loss mechanisms are switching and conduction loss.

2.3.3.1 Switching Loss

The finite time taken for a practical power MOSFET to switch between states results in an energy loss during the transition. The switching time and therefore the energy lost during the switching transition are dependent on both the MOSFET parasitic elements, the particular circuit topology being used and capability of the gate-drive circuitry. Due to the use of the dead time in the Class-D power stages and the inductive nature of the load, the switching behaviour is governed by transition of the load current either to or from a freewheeling diode. Consider one leg of an H-Bridge power stage as shown in Figure 2.10.

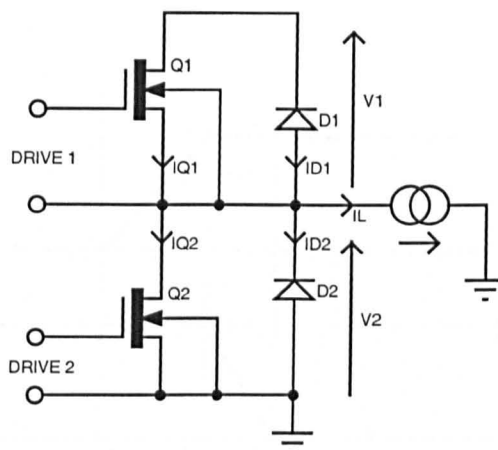
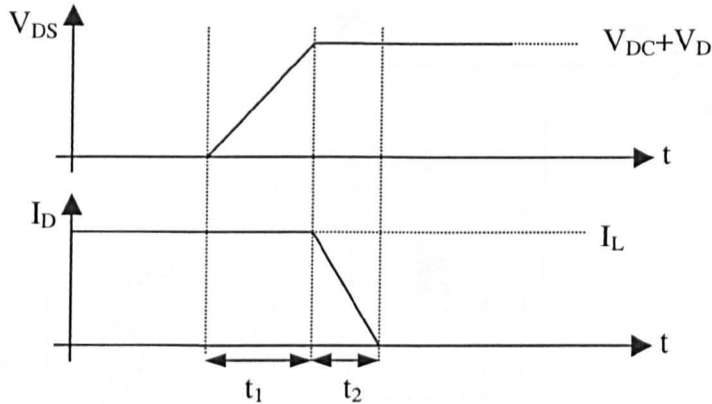


Figure 2.10 - Single leg of an H-bridge output stage

For a positive load current, I_L , as indicated on the figure, switching device Q2 on or off will not affect the output voltage, V_2 , since the current will simply transfer from Q2 to D2 or vice-versa. Thus, the loss incurred for this switching condition is negligible. However, if Q1 is switched on or off, the load current will transfer from D2 to Q1 or vice-versa. This commutation causes a change in the output voltage, V_2 , and therefore a loss will be incurred in the switching device. A similar situation is encountered if the load current is negative and Q2 is switched on or off.

The situation for the power MOSFETs turning off can be modelled relatively simply. Consider the case when the load current is negative and device Q2 switches off. The load current can only be supported in D1 when it becomes forward biased and thus Q2 will continue to support the current until V_2 has risen to a diode drop, V_D , above V_{DC} . Therefore, the Drain-Source voltage of Q2 and its Drain current can be approximated as shown in Figure 2.11. During time t_1 , the drain-source voltage rises in an approximately linear fashion until diode D1 becomes forward biased. The load current then transfers in a relatively linear manner from Q2 to D1. During both t_1 and t_2 , the voltage across and the current through Q2 are simultaneously non-zero; this leads to a large instantaneous power dissipation. Diode D1 only begins to conduct when the voltage across is very small (equal to the forward bias voltage) and therefore it suffers minimal switching loss.



**Figure 2.11 - Voltage across and current through Q2 during it switching off
(Negative load current)**

If the rates of change of both the current and voltage are taken as linear, then the energy lost during this transition, $E_{(OFF)}$ is as Equation (2.4).

$$E_{(OFF)} = \frac{1}{2} I_L (V_{DC} + V_D) (t_1 + t_2)$$

(2.4)

The diode drop, V_D , is likely to be small compared to the DC supply voltage and is often neglected. The shorter the transition times, t_1 and t_2 , the lower the loss incurred during switching. The mechanisms affecting t_1 and t_2 are functions of the MOSFET parasitic capacitances, the transient capability of the gate-drive and the transconductance of the MOSFET, [2.11]. The model proposed by Mohan, Undeland and Robbins [2.11] for the MOSFET switching off is shown in Figure 2.12. C_{gs} and C_{gd} represent the MOSFET parasitic capacitances which have to be charged and discharged via R1 and the gate-drive circuitry during switching events.

Figure 2.13 shows the MOSFET gate-source voltage, $i_{gs}(t)$, gate current, $i_g(t)$, drain current, $i_D(t)$ and the drain-source voltage, $v_{DS}(t)$ during the switch off event.

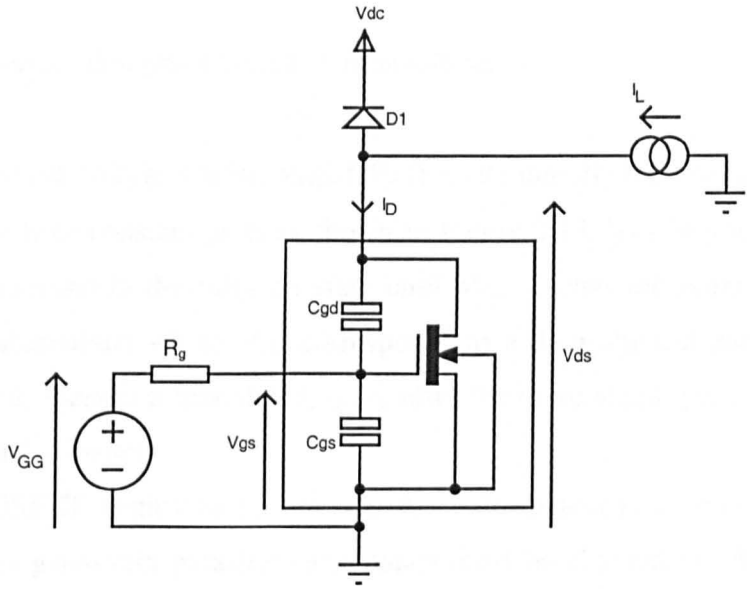


Figure 2.12 - MOSFET equivalent circuit with parasitic capacitance (Source - [2.11])

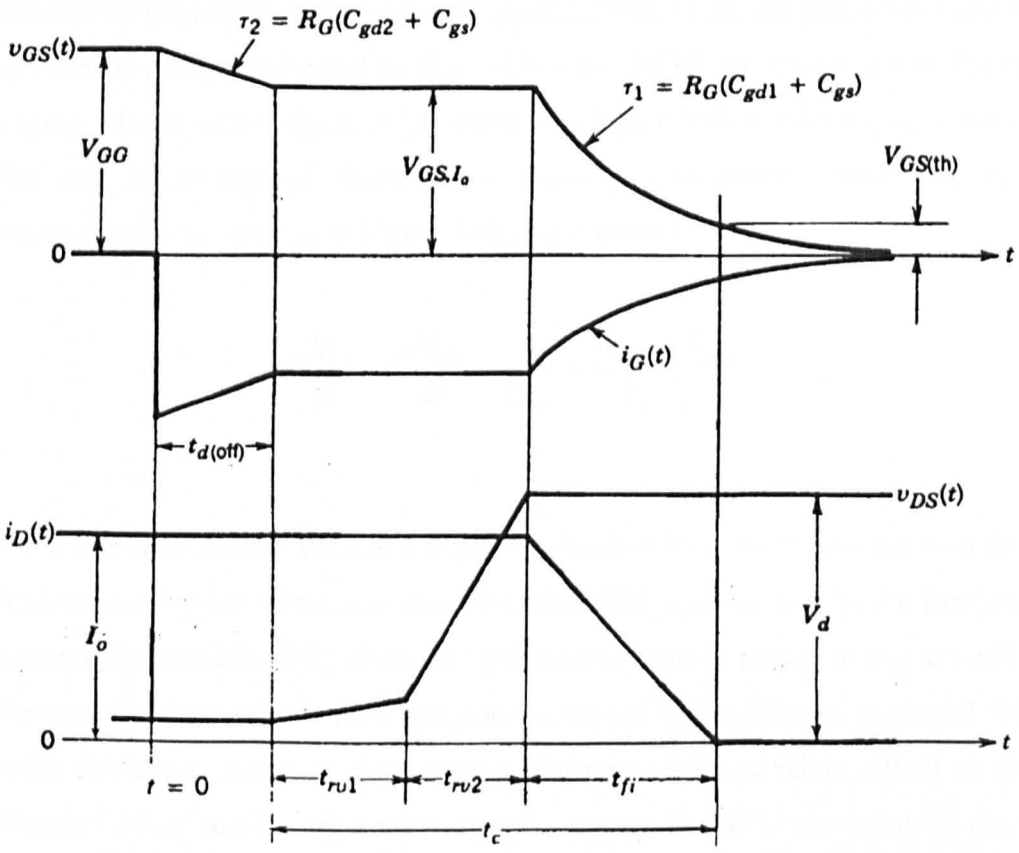


Figure 2.13 - MOSFET waveforms during a turn off event (Source - [2.11])

The turn-off process, described in [2.11], is as follows: -

1. At $t=0$, the drive voltage source, V_{GG} , falls from its initially high value (typically 12-15V) with a time constant of τ_2 as shown in Figure 2.13. V_{GS} begins to fall but the MOSFET remains in the fully on state until V_{GS} reaches the point on the device transfer characteristic where V_{GS} corresponds to a drain current equal to the load current. Thus, there is a time delay, $t_{d(off)}$, after the drive signal goes low before the device begins to switch.
2. As the MOSFET begins to switch off, the voltage across it begins to rise and therefore the gate-drain parasitic capacitance must be charged via R_G . During this time, the gate-source voltage remains at the constant level needed to support the full load current. Thus, the rate of change of drain-source voltage is equal to the rate of change of drain-gate voltage and this is as shown in Equation (2.5). During this period, the rate of change of drain-source voltage takes two distinct values governed by two different values of C_{gd} . At first, the MOSFET is still in the ohmic region and the equivalent circuit is as shown in Figure 2.14(a). Here, the gate drain capacitance is relatively large and equal to C_{gd1} . When the MOSFET moves out of the ohmic region into the active region, C_{gd1} changes to C_{gd2} which is a lower capacitance and the rate of change of drain-source voltage is increased. These two regions correspond to t_{rv1} and t_{rv2} in Figure 2.13 respectively.

$$\frac{dV_{DS}}{dt} = \frac{dV_{GD}}{dt} = \frac{i_g}{C_{gd}} = \frac{V_{GS, I_o} - V_{GG}}{R_G C_{gd}}$$

(2.5)

3. Once the drain-source voltage has reached such a level as to forward bias D_1 , the load current begins to transfer from the MOSFET drain to D_1 . As the load current decreases in the MOSFET drain, the gate source voltage begins to fall according to the transfer characteristic until the gate-source voltage equals the threshold voltage when the drain-current is zero. During this time, the equivalent circuit is that of Figure 2.14(c) and the time taken for the current to fall is governed by the time taken to discharge C_{gs} and C_{gd1} via R_G (The time constant is τ_1 in Figure 2.13)

4. When the MOSFET is fully switched off, the diode supports the full load current and the parasitic capacitances continue to charge as in Figure 2.14(d).

The crossover time t_c is therefore equal to that of t_1+t_2 in Figure 2.11 and is governed by three main factors: -

1. The magnitude of the parasitic capacitances, C_{gs} and C_{dg} .
2. The value of the gate drive resistance, R_G .
3. The transient performance of the gate drive circuit.

The parasitic capacitances are functions of the device construction. High power devices tend to use a greater silicon area and therefore tend to have high parasitic capacitances. Thus, to minimise the device switching time, the gate drive resistance should be as low as possible. The minimum value is governed by the maximum current drive capability of the drive circuitry. In addition, if a very low gate resistance is used, care must be taken to minimise parasitic inductance in the gate drive circuitry to avoid oscillations causing multiple switching events. In practice, typical transition times are of the order of tens of nanoseconds.

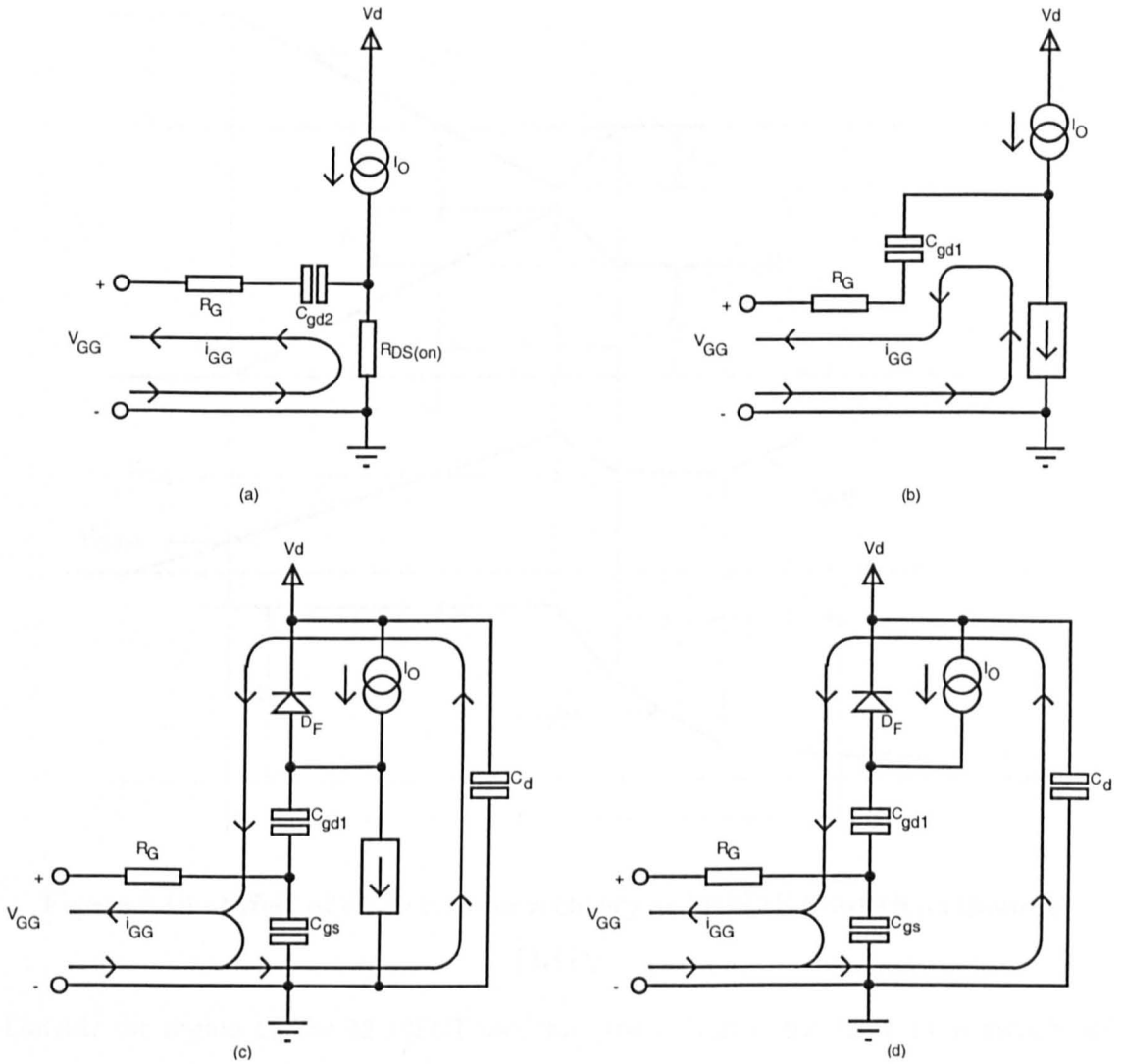


Figure 2.14 - Equivalent circuits during MOSFET switch off (Source - [2.11])

The behaviour of the circuit when the MOSFET is switched on is quite different from the turn-off behaviour. When the MOSFET turns on, the load current is transferred from the freewheel diode to the MOSFET. As the diode switches off, it undergoes reverse recovery and causes an additional current to flow in the MOSFET. Figure 2.15 shows the behaviour over the MOSFET turn on period with the diode suffering reverse recovery.

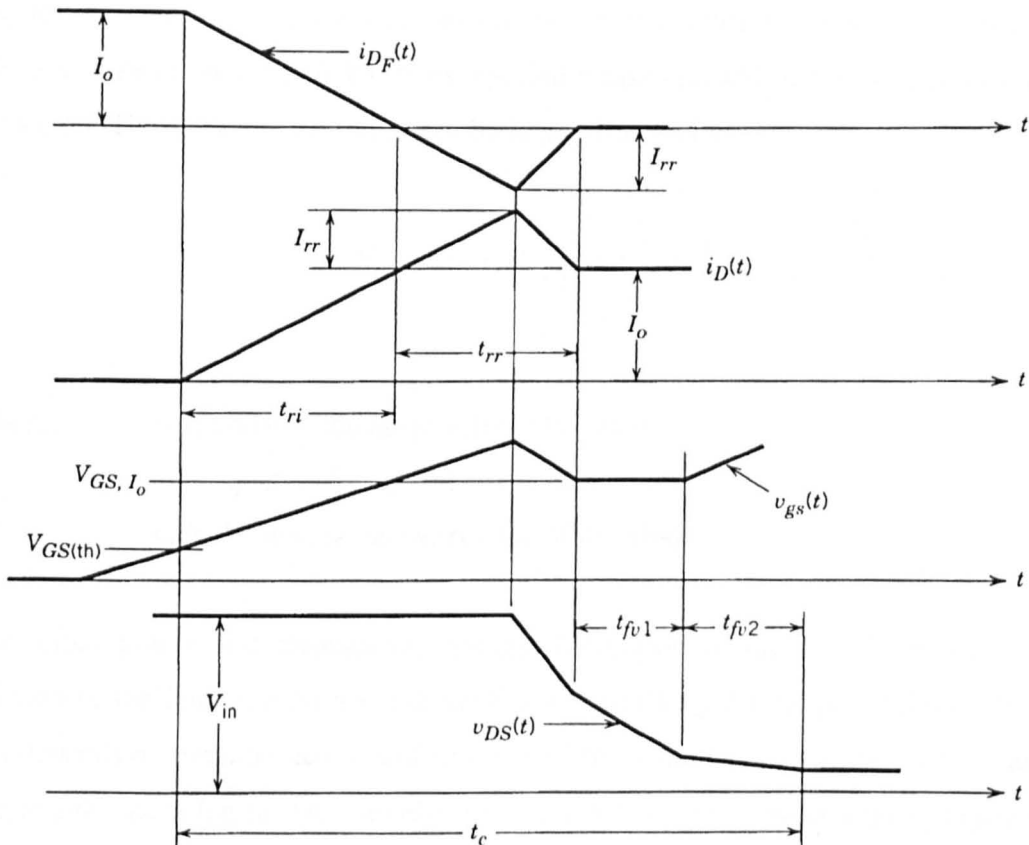


Figure 2.15 - Effect of diode reverse recovery at MOSFET switch on (Source - [2.11])

Outside the region t_{rr} , the MOSFET switching behaviour is the same as at switch off except the events are reversed. The difference with the case of the reverse recovery is that the current supported by the MOSFET increases beyond the load current to a value I_{rr} higher. When the diode has recovered, it turns off very quickly (depending on the 'snappiness' of the diode) and the MOSFET drain current falls back to the normal load current level. Thus, the diode reverse recovery causes an additional time, t_{rr} , when the MOSFET experiences loss.

The reverse recovery time, t_{rr} and the peak reverse recovery current, I_{rr} are linked by the reverse-recovery charge which must be removed during the recovery period. If the rate of change of reverse current (governed by the external circuit) is low then I_{rr} can be relatively small at the expense of a long recovery time. A large rate of change of recovery current will yield a very short recovery period but this also will increase the peak current in the MOSFET.

Since the level of reverse recovery and reverse recovery time are a function of the rate of change of the load current during switching, it is more difficult to model the turn on

loss level. A reasonable approximation can be had if the turn on losses are calculated in the same way as the turn off losses except that it takes an additional time, t_{rr} , to turn the device on. Thus, the turn on losses can be approximated by: -

$$E_{(ON)} = \frac{1}{2} I_L V_{DC} (t_1 + t_2 + t_{rr}) \quad (2.6)$$

Where, t_1 is equal to the drain voltage fall time
 t_2 is equal to the current rise time
 t_{rr} is the reverse recovery time of the diode

The actual power lost through the energy dissipation in the switching events is a function of the load current and the number of switching events per second, which in turn depends on the modulation strategy. For a PWM strategy, the situation is relatively simple since each leg of the H-Bridge will switch from +Vdc to ground and ground to +Vdc once per switching cycle. This corresponds to each of the four MOSFETs suffering a turn on and a turn off loss once per cycle. If the switching frequency currents are assumed to be small compared to the fundamental current then the overall switching loss can be calculated based on the fundamental current alone.

For a fixed DC link supply and switching behaviour, the switching loss is dependent on the switched current alone and an estimation of this can be obtained by averaging the load current and using this value in Equation (2.6). Thus, if each of the four devices turns on and off in a cycle, the total power stage switching loss is approximately: -

$$P_{LOSS(TOT)} = 4 \times F_s \times \frac{1}{2} I_{L(ave)} V_{DC} (t_{rr} + 2t_c) \quad (2.7)$$

Where, F_s is the switching frequency
 t_c is the switching time without reverse recovery (t_1+t_2)
 V_{DC} is the DC link supply voltage
 $I_{L(AVE)}$ is the average magnitude of the load current

$I_{L(AVE)}$ is simply: -

$$I_{L(ave)} = \frac{2\hat{I}}{\pi} \quad (2.8)$$

Where, \hat{I} is the peak load current

2.3.3.2 Conduction Loss

The conduction loss suffered by the power devices in the Class-D stage is relatively straight-forward to quantify. Since the dead-time in practice is likely to be less than 5% of the switching period, the conduction loss can be estimated to a good degree of accuracy by assuming the load current always flows in the power MOSFETs. Indeed, the use of power MOSFETs in preference to BJTs allows synchronous rectification whereby the MOSFET channel supports the load current in preference to the anti-parallel diode. Since the MOSFET has a lower voltage drop during conduction, this allows for an increase in the operational efficiency. If this assumption is made then at any one time, in an H-bridge power stage the load current flows through two power MOSFETs and the conduction loss is then simply: -

$$LOSS_{Conduction} = 2 \times I_{R.M.S.}^2 \cdot R_{DS(on)} \quad (2.9)$$

For most of the range of modulation depths, where the fundamental current is significantly greater than the switching frequency current, $I_{R.M.S.}$ can be approximated to the fundamental.

2.3.3.3 Soft Switching

The heating of the power MOSFET caused by switching loss can be reduced by using snubber networks. These circuits operate during the switching transitions to support the load current whilst the device switches, effectively reducing the switching stress on the device. The actual overall loss is not reduced but is transferred from the MOSFET to the snubber. This is beneficial since the MOSFET functions better when it is cold ($R_{DS(on)}$

increases with temperature). Snubbers are available for both turn-on and turn-off transitions.

2.3.3.4 Resonant Switching

Resonant switching techniques are a development of snubber technology which use extra passive and active components to force either the current through or the voltage across the device to zero whilst it switches. The difference between snubbers and resonant systems is that snubbers tend to redirect the switching loss to another part of the circuit whilst resonant systems reduce overall switching loss.

Various methods are available for resonant switching, one of which is to use a resonant link. With this approach, the DC link supplying the H-Bridge output stage is periodically forced to zero during which time, the power stage can switch without loss. Other techniques [2.12,2.13,2.14] use tuned circuits to force zero voltage commutation. All of these techniques, however, complicate the circuit design and require additional passive components. Furthermore, although resonant switching can result in lower EMI and increased efficiency, the voltage and/or current stresses of the switching device can be higher than the hard-switched equivalents.

2.4 Hybrid Systems

With an approach similar to that of the Class-G amplifier, hybrid systems consisting of a Class-D and linear output stage in parallel have been demonstrated [2.15,2.16,2.17,2.18]. These systems use the Class-D amplifier to provide the majority of the power and a linear amplifier to improve the fidelity. A typical implementation is shown in Figure 2.16 [2.15]

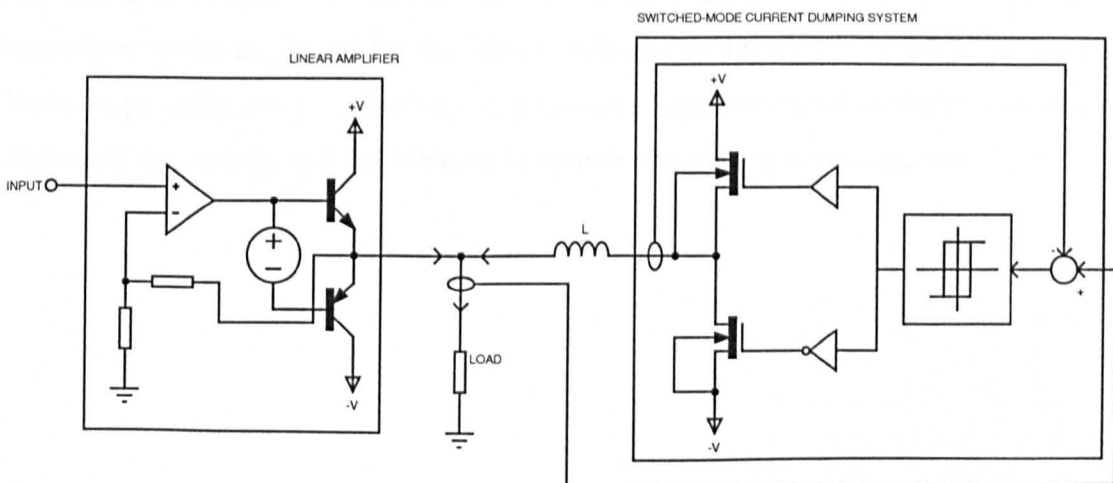


Figure 2.16 - Hybrid Linear/Class-D Amplifier (Source - [2.15])

In this system, the linear amplifier acts as a controlling master with the Class-D stage acting as a high power slave system. In effect, the linear power stage supplies the ripple current and any transient currents, which cannot be provided by the Class-D stage. The only filter component required is the coupling inductance, L . For a high power bandwidth, this coupling inductance must be small but this compromises the losses in the linear power stage, which has to provide a higher cancellation ripple current. Literature reports that these hybrid systems can reach peak efficiencies in excess of 90% [2.16] and typically operate above 80% over the full dynamic range of the amplifier whilst maintaining the hi-fidelity associated with linear amplifiers.

2.5 Conclusions

The use of a linear output stage in high power car audio applications results in a system that is at best 50% efficient. In practice, the reactive nature of the load impedance can reduce this efficiency by a further 20%. Although supporting literature has demonstrated various techniques through which a linear power stage can be made more efficient, the use of a Class-D output stage will allow for an increase in operational efficiency to greater than 80% over most of the operating range of the amplifier.

A Class-D power output stage suitable for high power applications has been discussed and its dominant loss mechanisms analysed. At the high switching frequencies required in practice, it is expected that the switching loss will dominate the efficiency profile and as such a detailed discussion of its cause has been presented. In Chapter 4, it is demonstrated that the switching loss in a hard switching converter can be minimised through careful design of the gate drive circuitry and although soft switching techniques are available which will reduce the switching loss, the additional complexity is considered to be excessive for the likely performance increase. The high fidelity of a linear stage and the high efficiency of a Class-D stage are found in the hybrid systems discussed earlier although the increase in system complexity is unattractive.

3 Modulation Strategies

3.1 Introduction

The chapter discusses what is essentially the heart of the Class-D amplifier system – that is the modulator circuitry. The purpose of the modulator is to take an audio frequency signal and convert it to a high frequency switching waveform which contains the audio information within its baseband. This high frequency signal is then increased in voltage by the power output stage and filtered to attenuate the high frequency switching components and recover the baseband audio signal. The baseband audio signal will then be at a higher power level than the original input signal to the modulator.

The type of modulation strategy is governed by the restrictions imposed by the power stage. More specifically, the output voltage from the H-Bridge power stage can be in one of three states; zero voltage, positive voltage or negative voltage. This limitation in resolution of output pulse amplitude forces the choice of a modulation strategy which conveys the audio information in the timing of the switched edges. Thus, the dynamic range of the amplifier is achieved with resolution in time rather than resolution in pulse amplitude. A perfect amplifier would simply amplify the level of the applied audio signal within the baseband in order that it can drive power into a loudspeaker. In practice the high frequency modulation colours the original audio baseband signal with additional high frequency components, baseband noise and harmonic terms. The level of these additional terms relative to the original signal gives a measure of the performance of the modulator and the modulators will be designed to offer a 20kHz bandwidth and a 60dB dynamic range. All frequency components inside the 20kHz baseband, other than the original signal, will be designed to be 60dB below the original signal level.

Two generic modulation techniques are compared; namely pulse width modulation (PWM) and pulse density modulation (PDM). The theoretical performance of both these types of modulator will be discussed and the limitations encountered with practical implementation highlighted. The chapter includes the description of a new design methodology for high order $\Delta\Sigma$ modulators.

3.2 Pulse Width Modulation

The basic method employed with PWM is to use the baseband audio signal to modulate the duty cycle of a high frequency square wave. A number of methods can be employed to achieve this modulation with the main difference being the targeted implementation technology, i.e. analogue or digital.

3.2.1 Analogue PWM

Natural sampling is a simple analogue PWM technique in which the instantaneous value of the audio signal is compared to a high frequency reference waveform. By using a sawtooth reference, only one of the pulse edges is modulated and with a triangle reference, double edge modulation is achieved. A typical generic implementation is shown in Figure 3.1.

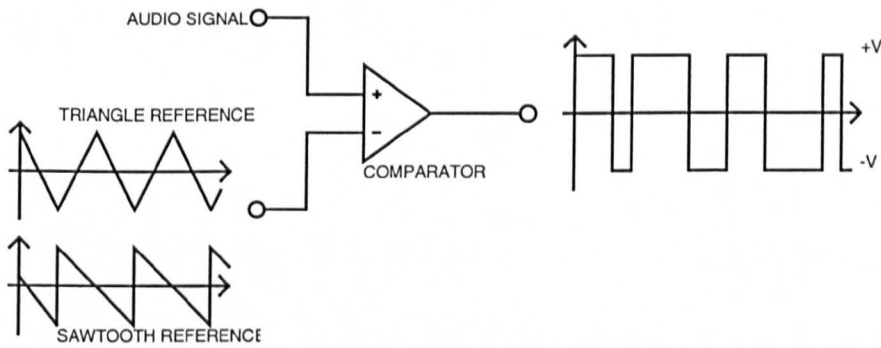


Figure 3.1 - Natural sampling PWM

If an ideal natural sampling process is assumed, analytical methods [3.1] can be employed to predict the frequency content of the modulated signal. For single-sided modulation with a sawtooth reference and the output pulses at $\pm V$, the PWM output spectrum for a single tone input, ω_v , is as Equation (3.1).

$$x(t) = V \times \begin{cases} M \cos(\omega_v t) & \text{Base - Band Signal} \\ - \sum_{m=1}^{\infty} \frac{2}{m\pi} (\sin(m\omega_c t) - J_0(m\pi M) \sin(m\omega_c t - m\pi)) & \text{Switching Frequency Components} \\ - \sum_{m=1}^{\infty} \sum_{n=\pm 1}^{\pm \infty} \frac{2}{m\pi} J_n(m\pi M) \sin\left(t(m\omega_c + n\omega_v) - m\pi - \frac{n\pi\omega_v}{2}\right) & \text{Combinatorial Components} \end{cases} \quad (3.1)$$

Where, M is the modulation depth
 J_n is an n^{th} order Bessel function of the first kind
 ω_v is the fundamental frequency
 ω_c is the triangle wave frequency

The PWM output spectrum contains the original baseband signal, components at integer multiples of the switching frequency and combinatorial terms around each switching frequency component. The spectra produced by double-sided modulation with a triangular reference is similar to that produced by single-sided in that it contains switching frequency and combinatorial terms as well as the fundamental signal. The symmetry of the process results in combinatorial terms that occur only at sidebands placed at even multiples of the signal frequency.

Equation (3.2) gives the spectra content for double-sided modulation where the variables are as defined for Equation (3.1).

$$x(t) = V \times \left\{ \begin{array}{ll} M \cos(\omega_v t) & \text{Base Band Signal} \\ + \sum_{m=1}^{\infty} \frac{4}{m\pi} J_0\left(\frac{mM\pi}{2}\right) \sin\left(\frac{m\pi}{2}\right) \cos(m\omega_c t) & \text{Switching Frequency Components} \\ - \sum_{m=1}^{\infty} \sum_{n=\pm 1}^{\pm\infty} \frac{4}{\pi n} J_n\left(\frac{mM\pi}{2}\right) \sin\left(\frac{\pi}{2}(n+m)\right) \cos(m\omega_c t + n\omega_v t) & \text{Combinatorial Components} \end{array} \right. \quad (3.2)$$

The spectral content of the naturally sampled PWM output is best visualised graphically. Figure 3.2 shows the spectral content up to the first switching frequency component of single and double sided modulators with a 100kHz switching frequency, a 5kHz baseband signal at modulation depths of 25% and 75% with the output pulse height at $\pm 5V$.

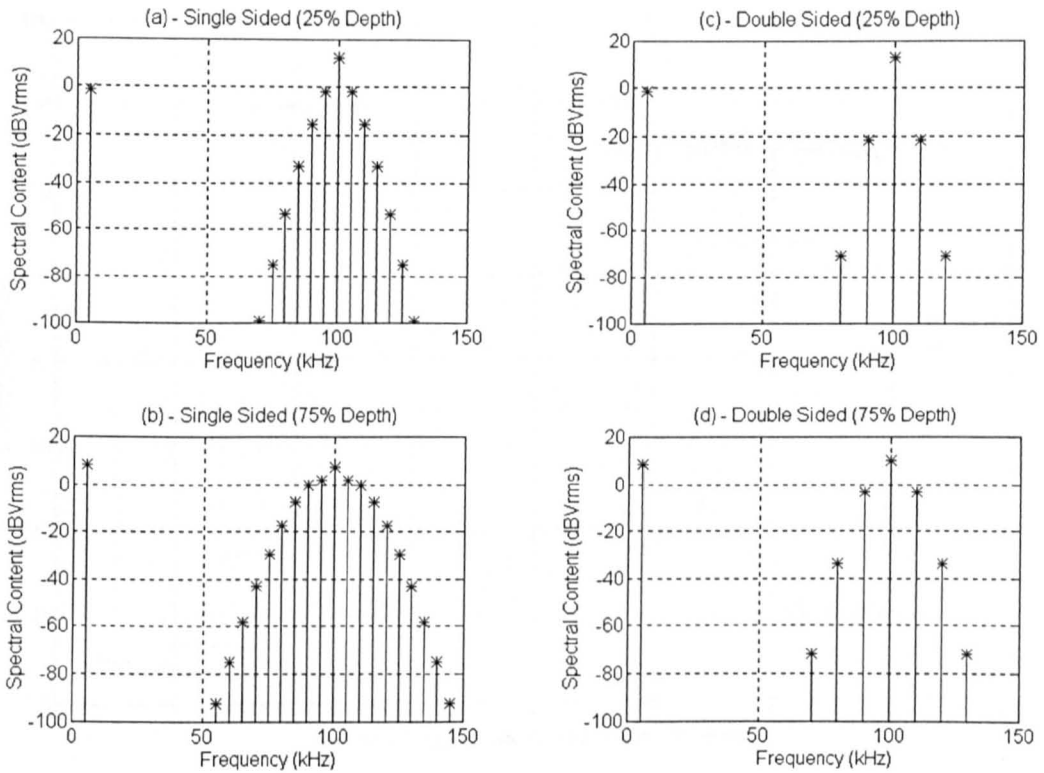


Figure 3.2 – Calculated spectral content of naturally sampled sine wave

The additional frequencies introduced by the natural sampling process are evident although it should be noted that there are no forward harmonic distortion terms in the baseband. In this ideal modulator, the only cause of baseband distortion will be through image spectra from the first switching frequency component folding back into the baseband. This type of distortion is known as combinatorial distortion and is the factor determining the minimum possible switching frequency for a given audio bandwidth. The switching frequency must be high enough such that the levels of the combinatorial terms within the baseband are below the required threshold. The double-sided modulation scheme offers improved performance over the single sided since both edges of the switching waveform are used to convey information.

If it assumed that the highest frequency in the baseband is fixed, for example 20kHz, the dynamic range of the modulator can be predicted as a function of switching frequency by comparing the maximum baseband signal level to the highest in-band combinatorial term. Figure 3.3 shows the dynamic range as a function of normalised switching frequency for both single and double-sided modulators.

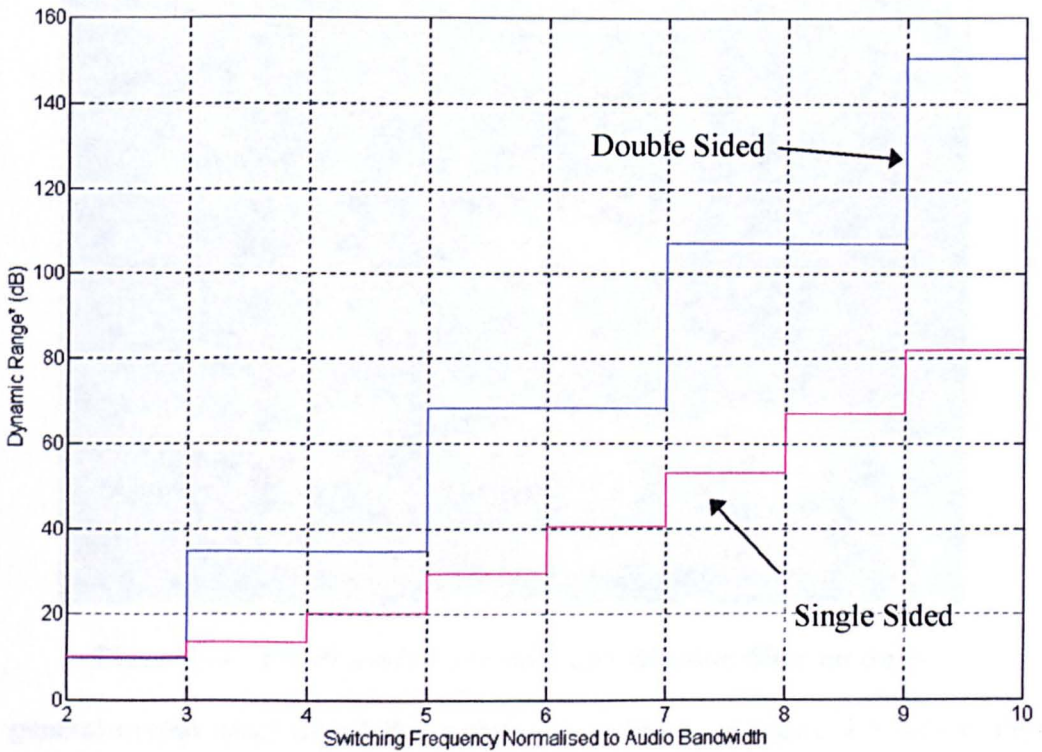


Figure 3.3 - Dynamic range as a function of normalised switching frequency

In Figure 3.3, a worst case scenario of full modulation depth is used and the dynamic range calculated by comparing the fundamental magnitude to the level of the first combinatorial term to fall within the baseband. The benefit of using the triangular reference to achieve double-sided modulation is evident from Figure 3.3 with the superior achievable dynamic range. The stepped nature of the profiles is a result of the manner in which the dynamic range is calculated. The step edges coincide with a combinatorial term lying at the same frequency as the fundamental signal. For the double sided modulation strategy, the required switching frequency for a dynamic range of 60dB is five to seven times the baseband bandwidth. Thus, for 20kHz bandwidth, the required switching frequency is around 140kHz. Therefore, for the rest of this section on natural sampling, a double-sided strategy will be assumed.

In order to verify the operation of naturally sampled PWM, a modulator was constructed. Details of the construction are given in Appendix C. The modulator design allows the user to modify the anti-aliasing filter by changing a single PCB. The modulator/filter was housed in a screened aluminium box to minimise interference as shown in Figure 3.4.

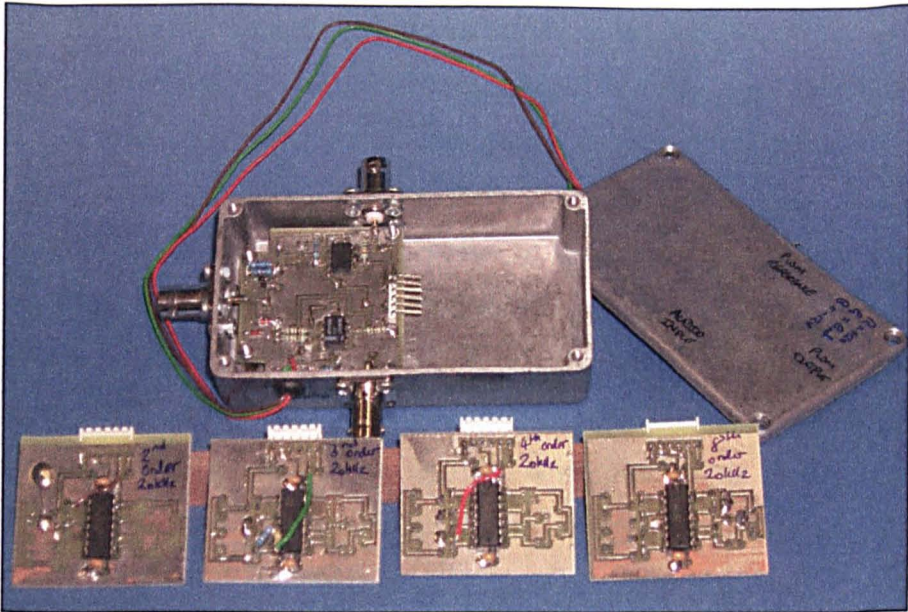


Figure 3.4 - PWM modulator with anti-aliasing filter modules

The general output spectrum of the modulator is shown in Figure 3.5 below. Figure 3.5(a) shows the spectra with a 10kHz fundamental whilst Figure 3.5(b) shows the spectra with a 20kHz fundamental.

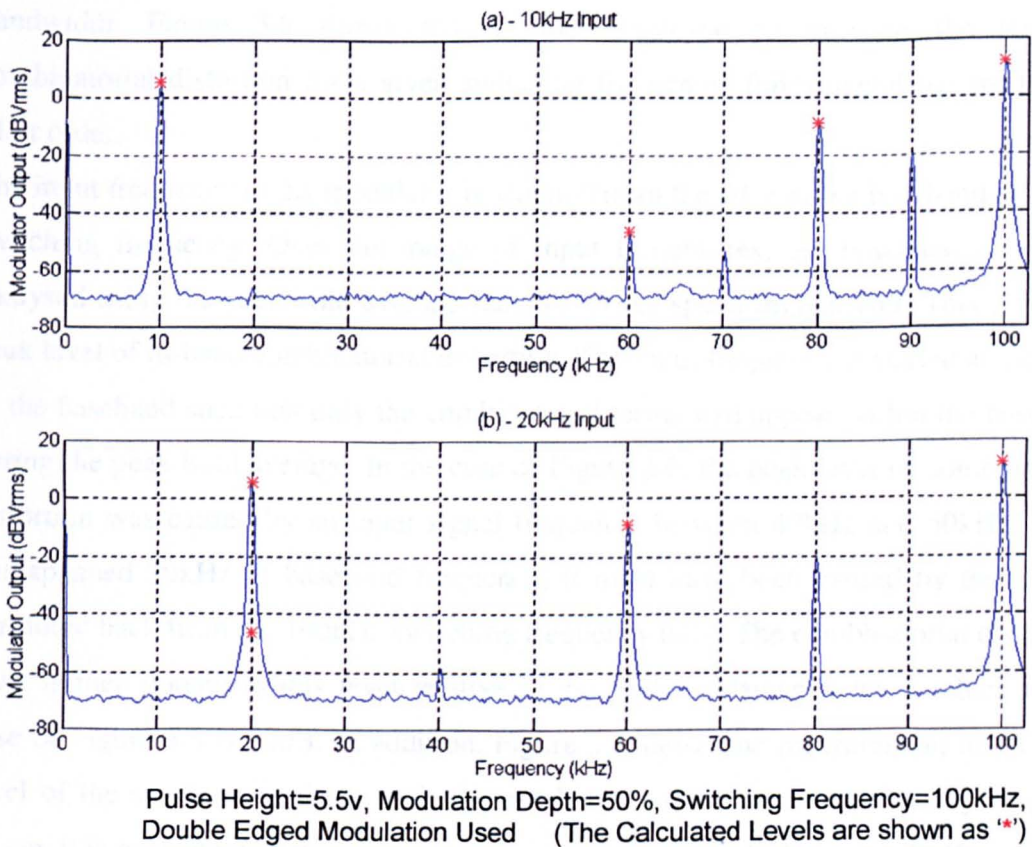


Figure 3.5 - Measured spectral content of natural sampling PWM

The main difference between the calculated and measured spectra is the presence of combinatorial terms at all integer multiples back from the first switching harmonic, whereas Equation (3.2) predicts that only even integer multiples should be present. A likely cause of the extra terms is asymmetry in the triangle reference waveform. Any asymmetry will cause the triangle reference to look more like a sawtooth waveform, which will lead to the presence of the extra terms.

The increase in fundamental frequency in Figure 3.5(b) over that of Figure 3.5(a) demonstrates the need for an anti-aliasing filter. With no anti-aliasing filter, input signals beyond 20kHz will lead to large combinatorial terms folding back into the baseband. Indeed, with a 20kHz input, Figure 3.5(b) shows that the second signal harmonic back from the first switching component is just beginning to enter the base band and is significantly higher than the noise floor. Although most input signals to the modulator are already band-limited, noise and interference may exist at higher frequencies and lead to combinatorial distortion.

Since the out of band attenuation of any anti-aliasing filter is finite, there is a trade off between required filter order and switching frequency for a given fundamental bandwidth. Figure 3.6 shows the method employed to measure the level of combinatorial distortion for a given switching frequency, fundamental bandwidth and filter order.

The input frequency to the modulator is scanned from the edge of the baseband up to the switching frequency. Over this range of input frequencies, the baseband content is analysed using the peak hold average function of the spectrum analyser. This gives the peak level of in-band combinatorial distortion. The input frequency is started at the edge of the baseband such that only the combinatorial terms will appear within the baseband during the peak hold average. In the case of Figure 3.6, the peak level of combinatorial distortion was caused by an input signal frequency between 40kHz and 50kHz. Since this spanned 20kHz of baseband frequency, it must have been caused by the second harmonic back from the 100kHz switching frequency used. The combinatorial distortion level is then quoted as this level relative to the peak fundamental level, which in the case of Figure 3.6 is 50dB. In addition, Figure 3.6 shows the measurement noise floor level of the spectrum analyser with this particular bandwidth. With this experimental set-up, it is possible to measure combinatorial distortion levels down to -70dB, which is in-line with the amplifier requirements.

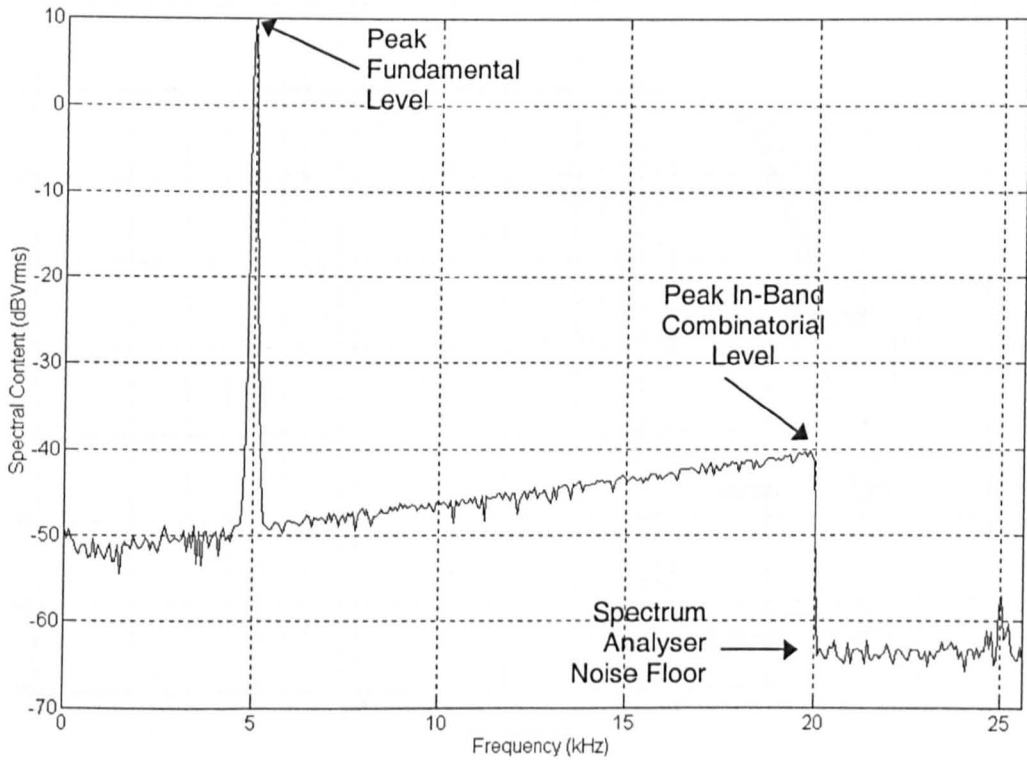


Figure 3.6 - Measurement of combinatorial distortion

The combinatorial distortion levels were measured for a second, third and fourth order anti-aliasing filter all with corner frequencies of 20kHz. The switching frequency was varied from 100kHz to 200kHz and the combinatorial distortion level calculated as described above. For all tests, the voltage pulse height was 5.5V and the modulation depth was 75%. The measured transfer functions of the three filters are shown in Figure 3.7.

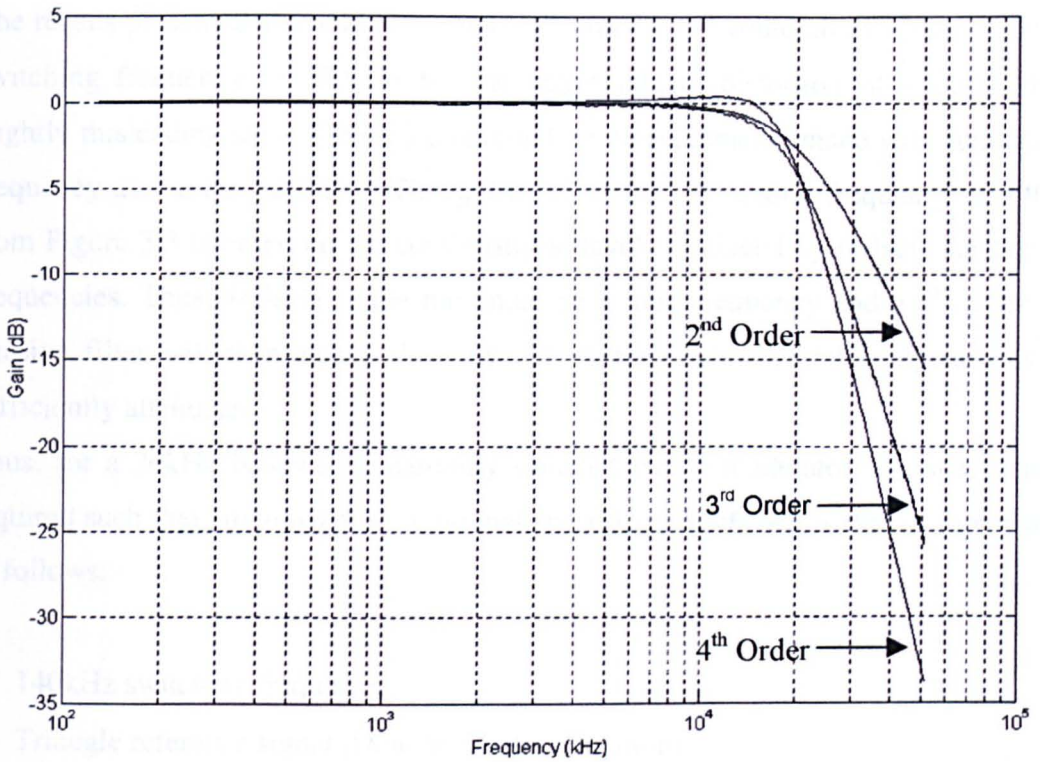


Figure 3.7 - Measured anti-aliasing filter characteristics

With these anti-aliasing filters, the trade-off between filter order and switching frequency for a 20kHz bandwidth modulator is shown in Figure 3.8.

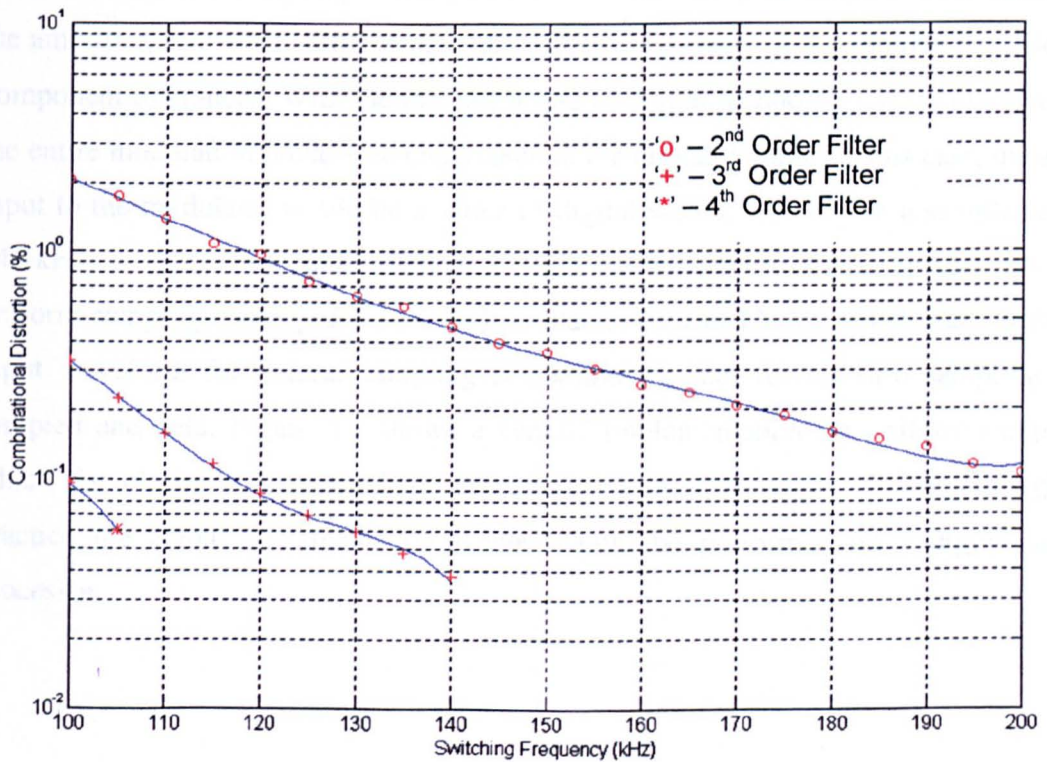


Figure 3.8 - Measured combinatorial distortion levels

The results presented above indicate that a 4th order filter would allow for a reduction in switching frequency to 100kHz for the target inband distortion of -60dB. This is slightly misleading since Figure 3.8 is based on measurements made with fundamental frequency above the baseband. The specification of a switching frequency of 140kHz from Figure 3.3 is based on the combinatorial levels produced by in-band fundamental frequencies. Thus, 140kHz is the minimum switching frequency and a 3rd order anti-aliasing filter will then ensure that any out of band fundamental component is also sufficiently attenuated.

Thus, for a 20kHz bandwidth, naturally sampled PWM modulator, the specifications required such that any unwanted additional spectra are 60dB below the fundamental are as follows: -

- 140kHz switching frequency
- Triangle reference signal (Double sided modulation)
- Third order Butterworth anti-aliasing filter with a corner at 20kHz.

3.2.2 Digital PWM

Whilst the natural sampling PWM process can meet the performance requirement for the amplifier, it is essentially an analogue process and therefore susceptible to noise and component tolerances. With the increasing use of digital technology, it is attractive that the entire modulation process be undertaken in the digital domain. In this case, the audio input to the modulator would be a series of digital words, typically at a sample rate of 44.1kHz. A simple way to implement a PWM strategy in the digital domain is to use uniform sampling. This process is very similar to natural PWM except that where the input waveform for natural sampling is continuous, that for uniform sampling is a sampled and held. Figure 3.9 shows a generic implementation for uniform sampling, which for clarity is expressed as an equivalent ideal analogue circuit although in practice the actual waveform comparison would be performed on a digital signal processor.

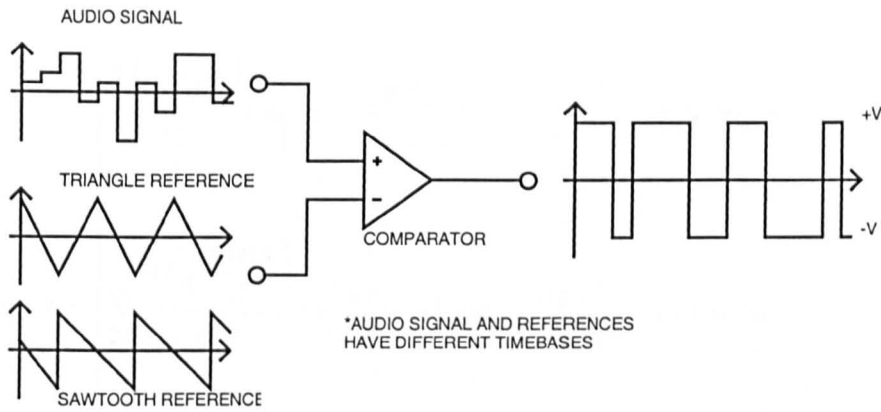


Figure 3.9 - Uniform sampling

Again, the double Fourier approach [3.2] can be used to calculate the spectrum of the uniform sampled audio signal. This technique gives the frequency component magnitudes as in Equation (3.3) below. A similar expression exists for double-sided uniform sampling, Equation (3.4), and the predicted spectral content for both single and double-sided uniform PWM is shown in Figure 3.10. The modulator parameters are 100kHz switching frequency, 5kHz baseband signal, modulation depths of 25% and 75% and an output of $\pm 5V$.

$$x(t) = V \times \begin{cases} \frac{2J_1(\pi M q)}{\pi q} \sin\left(\omega_v t - \frac{\pi}{2}(1 + 2q)\right) & \text{Fundamental} \\ \sum_{n=1}^{\infty} \frac{2J_n(n\pi M q)}{n\pi q} \sin\left(n\omega_v t - \frac{n\pi}{2}(1 + 2q)\right) & \text{Forward Harmonics} \\ + \sum_{m=1}^{\infty} \frac{2(1 - J_0(m\pi M))}{m\pi} \sin(m\omega_c t) & \text{Switching Frequency Components} \\ - \sum_{m=1}^{\infty} \sum_{n=\pm 1}^{\pm\infty} \frac{2J_n[(m+nq)\pi M]}{(m+nq)\pi} \sin\left((m\omega_c + n\omega_v)\left(t - \frac{\pi}{\omega_c}\right) - \frac{n\pi}{2}\right) & \text{Combinatorial Components} \end{cases} \quad (3.3)$$

Comparison of Figure 3.2 and Figure 3.10 shows that the uniform sampling PWM process introduces significant forward harmonic distortion terms in addition to the combinatorial foldback terms. The combinatorial terms, however, are lower than those introduced by natural sampling.

$$x(t) = V \times \left\{ \begin{array}{l} \frac{4J_1\left(\frac{\pi Mq}{2}\right)}{\pi q} \cos\left(\omega_v t - \frac{q\pi}{2}\right) \quad \text{Fundamental} \\ \sum_{n=1}^{\infty} \frac{4J_n\left(\frac{n\pi Mq}{2}\right)}{n\pi q} \sin\left(\frac{n\pi}{2}\right) \cos\left(n\omega_v t - \frac{nq\pi}{2}\right) \quad \text{Forward Harmonics} \\ - \sum_{m=1}^{\infty} \sum_{n=\pm 1}^{\pm\infty} \frac{4J_n\left[\frac{\pi}{2} M(m+nq)\right]}{(m+nq)\pi} \sin\left((m+n)\frac{\pi}{2}\right) \times \\ \quad \cos\left(n\omega_v t + m\omega_c t - \frac{nq\pi}{2}\right) \quad \text{Combinatorial Components} \end{array} \right.$$

(3.4)

Where, q is equal to ω_v/ω_c

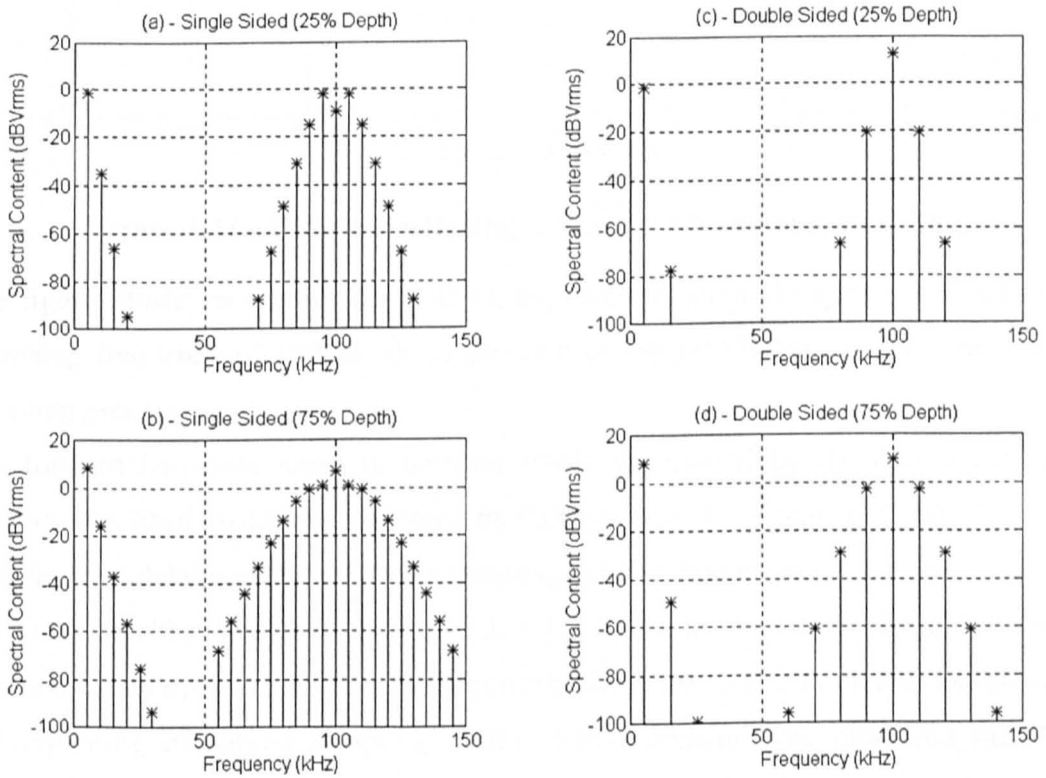


Figure 3.10 - Calculated spectra for uniform sampling

Since the dominant cause of distortion in a uniform sampling scheme is the presence of forward harmonic terms, these can be used to derive the THD of the modulator. The

combinatorial terms are significantly lower than the forward harmonics and will only effect the THD figure for low oversampling ratios. Figure 3.11 gives the THD based on these terms as a function of switching frequency. The signal frequency was specified as 6kHz as this is the highest frequency term which has a third harmonic in the 20kHz baseband. The modulation depth was set to a worst case of 100%.

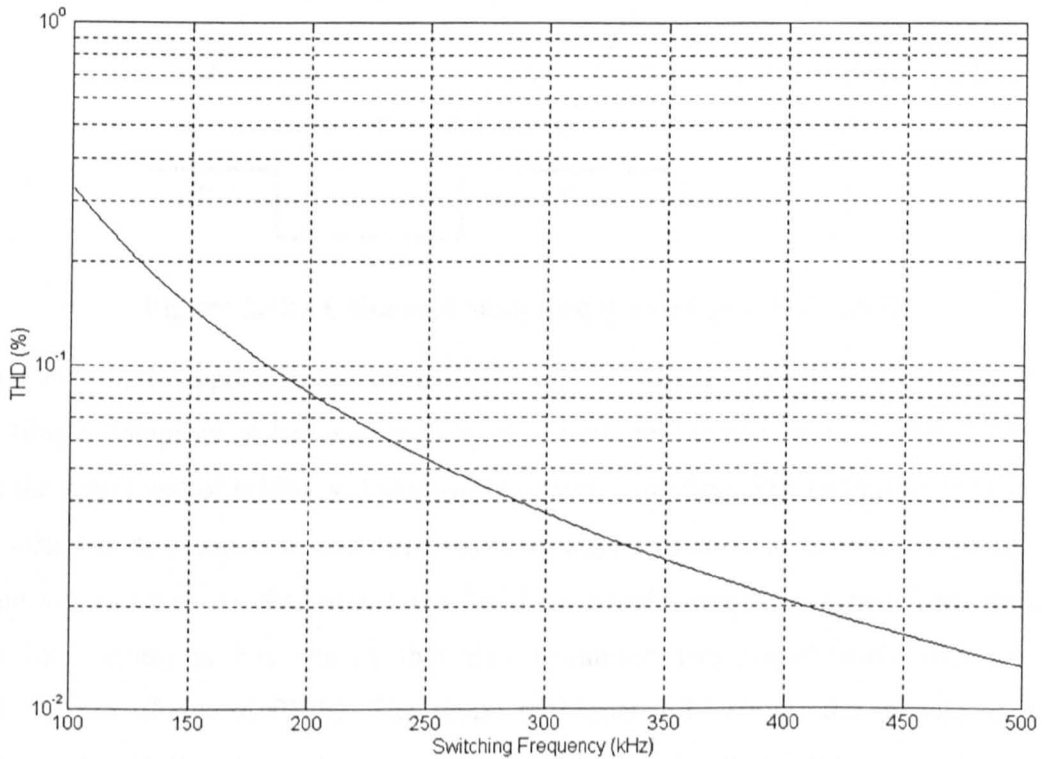


Figure 3.11 - THD vs. switching frequency for uniform sampling

The figure illustrates that for 0.1% THD, the uniform sampling system will require a switching frequency of 180kHz in comparison to the 140kHz required by the natural sampling process.

The forward harmonic terms in uniform PWM are caused by the duty cycle error between the ideal (naturally sampled) modulation and the sampled & held (uniform sampling) modulation. The enhanced sampling process first proposed by Leigh, Mellor, and Cheetham [3.2] and developed in [3.3, 3.4, 3.5] can be used in the digital domain to reduce the duty cycle error and achieve performance close to that of natural sampling by approximating to natural sampling in the digital domain. The enhanced sampling process uses a linear interpolation technique as shown in Figure 3.12.

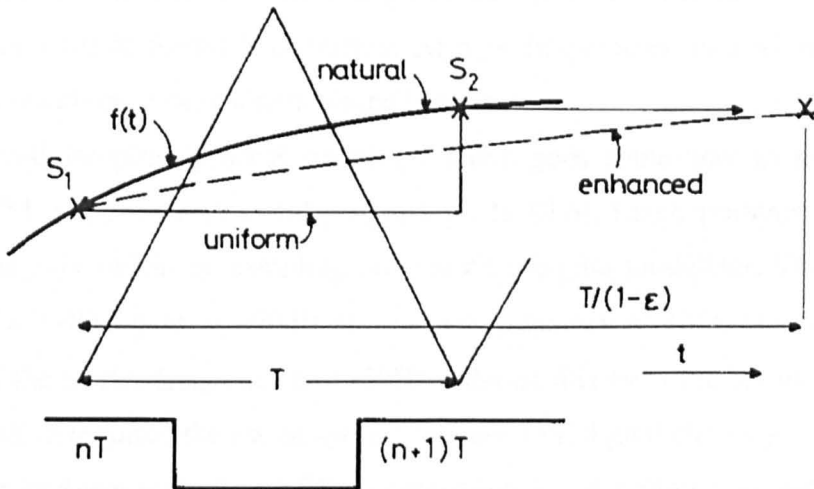


Figure 3.12 - Enhanced sampling process (Source - [3.3])

This technique approximates to natural sampling in a digital implementation by reaching a compromise between high level of harmonic distortion in uniform sampling and the high level of foldback distortion in natural sampling. The technique interpolates the sampled data between samples to give an approximation to natural sampling. The value of ϵ (0 to 1) determines the level to which sampling varies from uniform sampling. Analysis has shown that this technique can significantly improve the performance of digital PWM. The graph in Figure 3.13 shows the calculated THD performance of the enhanced sampling for a 20kHz bandwidth amplifier.

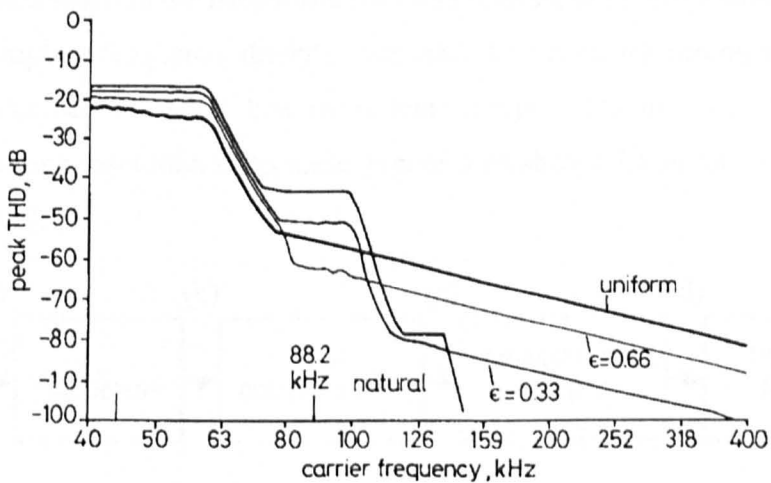


Figure 3.13 - Relative THD performance of sampling strategies (Source - [3.3])

Figure 3.13 shows that for low switching frequencies uniform sampling is optimal due to the lower level of foldback distortion. At high frequencies, natural sampling is the best due to the absence of inherent inband harmonics.

The enhanced sampling process described above goes some way to making a fully digital PWM amplifier a practical proposition. In [3.6], Leigh presents the results of implementing the enhanced sampling process on a digital modulator. This system was capable of a THD figure of -90dB at a carrier frequency of 132kHz with $\epsilon=0.35$. An increase of the carrier frequency to 176kHz reduced this even further to -110dB . This implementation required the use of specialised fast TTL digital circuitry.

One further problem with digital PWM generation is the timing resolution required in the generation process. For a modulator running at 100kHz with a required dynamic range of 16 bits, the edges of the PWM waveform must be defined to an accuracy of $\pm 140\text{ps}$. Not only is this difficult to realise on the DSP, the output power devices in the power stage have switching times several orders of magnitude longer than this. Thus, there is a requirement to reduce the timing resolution requirement of the PWM edges.

Hiorns and Sandler [3.7] have presented a technique based on noise shaping to achieve a lower timing requirement. The approach used is to increase the sampling rate of the input data through interpolation and re-quantise the data at a lower resolution. In-band resolution is maintained by shaping the quantisation noise floor to reduce it in the baseband at the expense of an increase at higher frequencies. The increase in sampling frequency allows space in the bandwidth for this noise-shaping procedure. Although the increase in sampling frequency directly increases the necessary timing resolution, the reduction in number of output bits more than compensates for this and an overall relaxation in timing resolution is possible. Figure 3.14 shows the structure of the system proposed in [3.7].

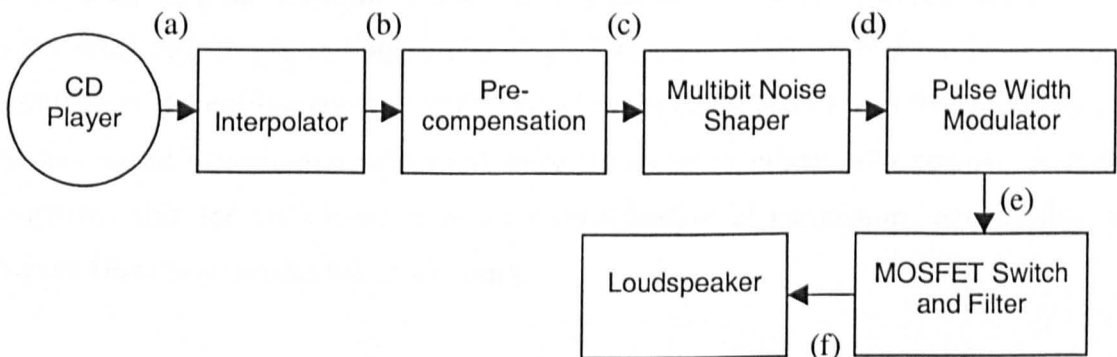


Figure 3.14 - Oversampled noise shaping PWM system (Source - [3.7])

The data from the CD is 16-bit and arrives at a rate of 44.1kHz. Eight times interpolation is used to create a 16-bit data stream at a rate of 352.8kHz at point 'b'. The sampling type converter implements a pre-compensation scheme to linearise the uniform PWM process (similar to that proposed in [3.3]). Thus, the multibit noise shaper receives 16-bit data at a rate of 352.8kHz. The noise shaper used in [3.7] was a fourth order type and allowed for a reduction to 8-bits with a loss of only 2dB in baseband resolution over the 16-bit data. The result of this signal processing is a PWM stage being driven by an 8-bit word at a rate of 352.8kHz. This equates to a timing resolution of 11ns in the pulse edges, which is far more practical than the 140ps required with the 16-bit implementation. The general noise-shaping/bit reduction structure is based on re-quantisation of the input data at a lower resolution. The dynamic range associated with the input word length is maintained by using feedback around the quantiser to filter the in-band quantisation noise, Figure 3.15.

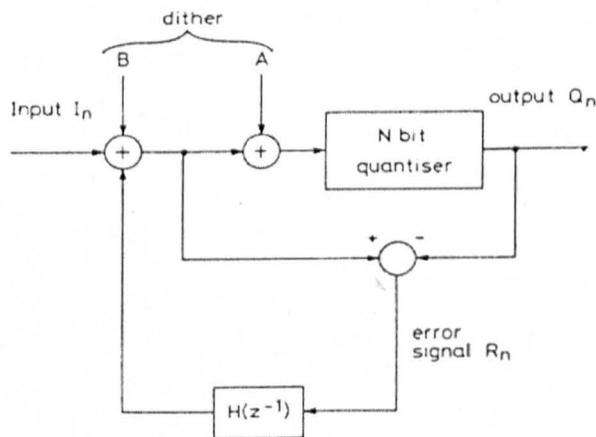


Figure 3.15 - Noise-shaping transfer function (Source - [3.7])

The transfer function of $H(z^{-1})$ is chosen to minimise the noise transfer function (NTF) in the base-band. In this case, $H(z^{-1})$ is a time delay element.

If the noise-shaping technique is taken to the extreme, it is possible to reduce the 16-bit word input to a single bit output. If a single bit output word is used, the pulse output from the modulator is a constant width (equal to the clock period) and PWM generation of this signal is then straightforward since the pulse is either fully positive or fully negative. This approach leads to another classification of modulators, namely that of Sigma-Delta or pulse density modulators.

3.3 Pulse Density Modulation

Pulse Density Modulation (PDM) is based on a single bit quantiser within a feedback loop. The quantiser is clocked at a rate very much greater than the Nyquist frequency and the output signal used to shape the quantisation noise. Early PDM was achieved with the Delta Modulator [3.8] as shown in Figure 3.16.

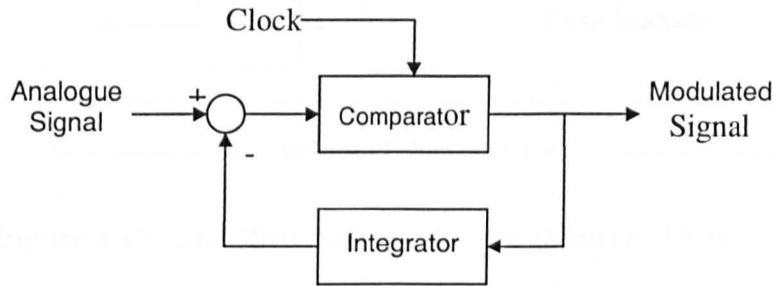


Figure 3.16 - Delta modulator

The comparator acts as a single bit quantiser, which conveys information about the derivative of the input signal. The action of the integrator in the feedback loop is to force the average of the difference between the analogue signal and the output to zero. This early form of PDM is simple but suffers from excessive in band quantisation noise. In addition, the oversampling requirement of this simple modulator was required to be in excess of 5000 for good reproduction of speech [3.9]. This level of oversampling leads to impractical switching rates in the power output stage.

In 1963, with reference to Delta modulator, Inose and Yasuda [3.10] stated that a Delta modulator is incapable of transmitting a DC component. Furthermore, its dynamic range and SNR are inversely proportional to the signal frequency and the final integration causes accumulative errors. By adding an integrator to the input of the Delta modulator, Inose and Yasuda solved these problems and coined the term for the new modulator as the Delta-Sigma Modulator. More recently, this has been adapted to form the Sigma-Delta Modulator ($\Sigma\Delta$). Figure 3.17 shows the modified Delta modulator.

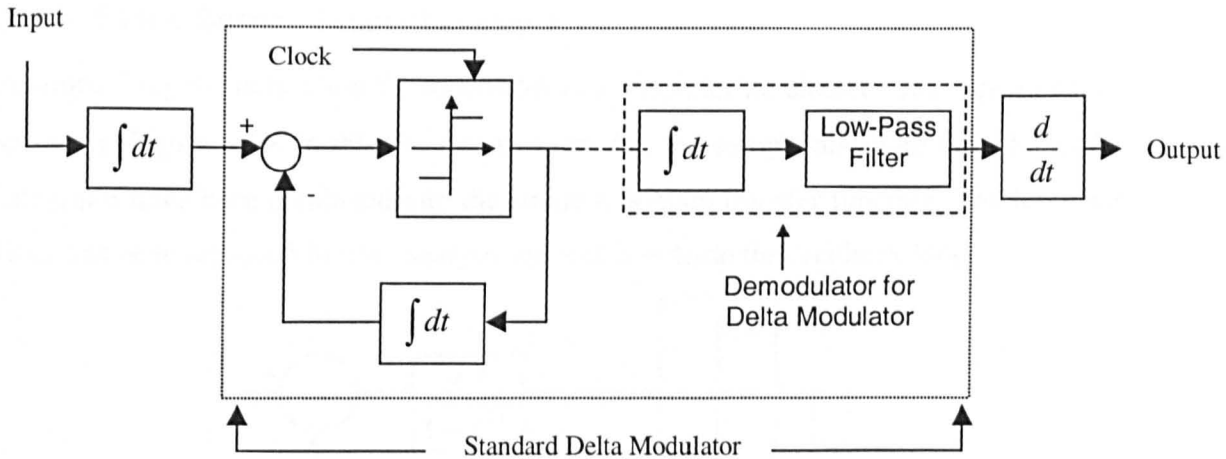


Figure 3.17 - Modified delta modulator (Source - [3.10])

The addition of the integrator at the modulator input must be followed by the addition of a differentiator at the output to restore the original signal. The modulator of Figure 3.17 can be simplified by combining the two integrators at the front end (through linear subtraction) and effectively cancelling out the differentiator and integrator in the demodulation section. Figure 3.18 shows the resulting modulator – namely the $\Sigma\Delta$ modulator.

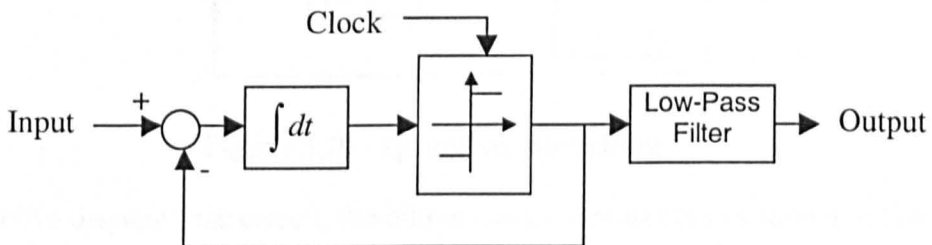


Figure 3.18 - Simplification of modified delta modulator ($\Sigma\Delta$ Modulator)

As well as resulting in a modulator that has a dynamic range and SNR that are both independent of the signal frequency, the modification has resulted in a system which only requires a low-pass filter for demodulation. This is beneficial since power amplification will be possible by simply increasing the voltage of the quantised levels and passing the output through the conventional low-pass audio filter. Inose and Yasuda go on to suggest that the integrator in the $\Sigma\Delta$ structure can be replaced by a higher order function which will introduce a greater noise-shaping effect and increase the in-band SNR.

3.3.1 First & Second Order Modulators

A simple way to analyse the $\Sigma\Delta$ modulator is to consider its discrete time equivalent as shown in Figure 3.19. In this discrete time model, the sample and hold circuit and the integrator have been combined into the single z-domain transfer function. The low-pass filter has been removed for this analysis since it is outside the feedback loop.

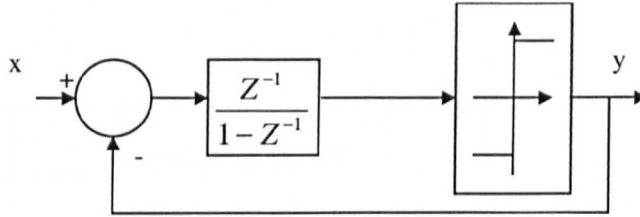


Figure 3.19 – Discrete time equivalent

The quantiser can be modelled as a unity gain element that introduces an error signal, e , as shown in Figure 3.20.

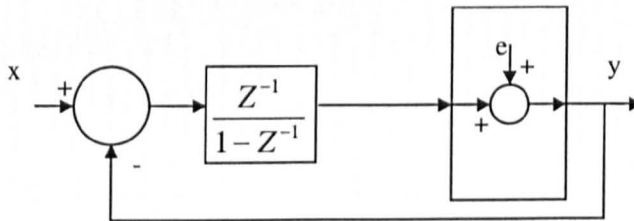


Figure 3.20 - Quantiser modelling

With the above discrete time circuit, the output can be represented as shown in Equation (3.5). Thus, the output of the modulator consists of the input signal delayed by a sample period and the first order difference of the error signal.

$$y[n] = x[n]z^{-1} + e[n](1 - z^{-1})$$

(3.5)

Other than causing a phase shift between modulator input and output, the input signal is unaffected by the modulation process. The first order difference of the error signal has the effect of shaping the quantisation noise. In continuous time, the first order difference term can be represented by multiplication of the error term by $2 \sin\left(\frac{\omega T}{2}\right)$, where T is the sampling period. Noise-shapers with this type of error-transfer function are known

as sinusoidal and the noise power is reduced at low frequency (baseband) at the expense of an increase at higher frequency.

The output spectral content of the $\Sigma\Delta$ modulator will consist of the original input signal with additional quantisation noise. Simulation of this first order modulator with a 6kHz tone sampled at 200kHz demonstrates the shaped nature of the quantisation noise, Figure 3.21.

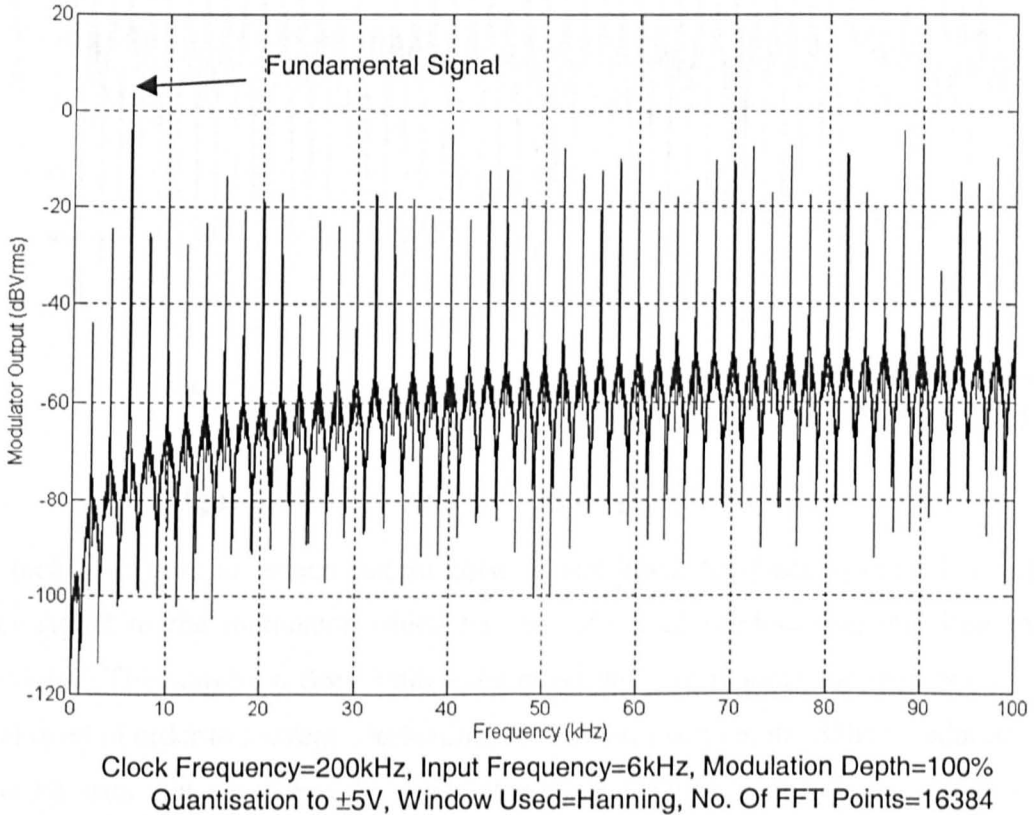
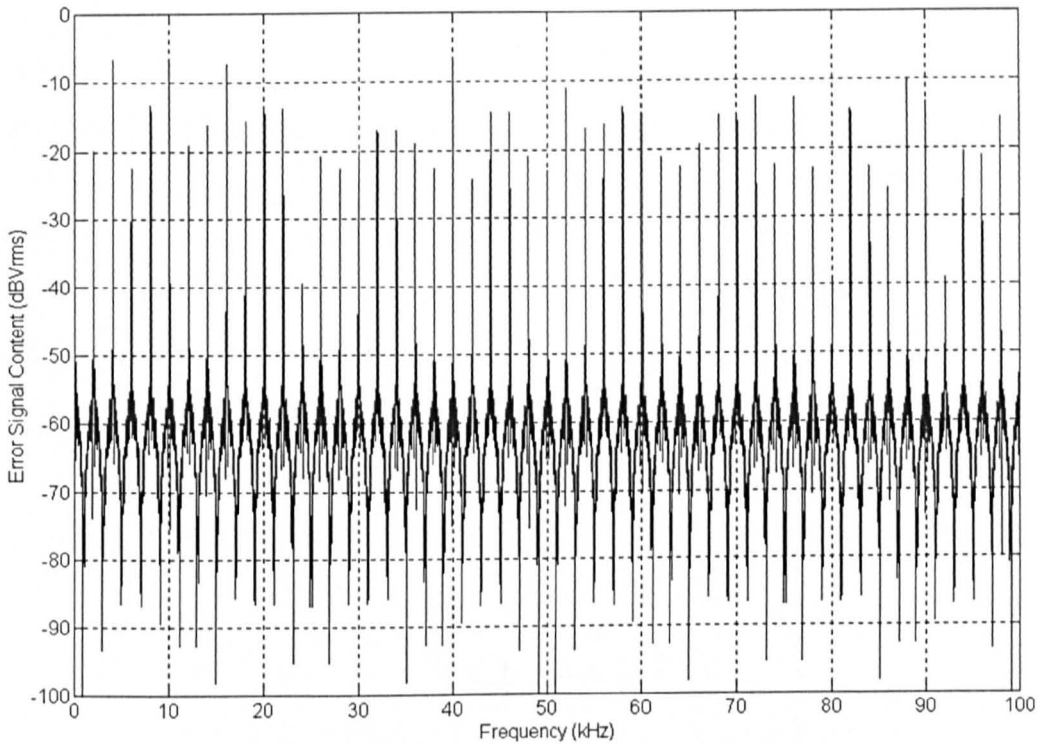


Figure 3.21 – Simulated spectrum from a first order $\Sigma\Delta$ modulator

Figure 3.21 shows the noise-shaping effect of $\Sigma\Delta$ modulation on the quantisation noise with the modulator noise floor falling away at low frequencies. It is evident that there is significant content in the spectrum other than the noise floor and the fundamental 6kHz tone. The additional content, termed pattern noise [3.11], is due to limit cycling in the modulator due to the non-linear quantisation. Equation (3.5) does predict the overall spectrum trend although the actual quantisation noise is highly coloured. Figure 3.22 shows the spectral content of the quantisation noise for the same simulation conditions as for Figure 3.21 and it is evident that the quantisation noise is far from random.



Clock Frequency=200kHz, Input Frequency=6kHz, Modulation Depth=100%
Quantisation to $\pm 5V$, Window Used=Hanning, No. Of FFT Points=16384

Figure 3.22 - Spectral content of quantisation error

One technique used to reduce pattern noise in non-linear feedback systems is to add a dither signal to the modulator which has the effect of randomising the limit cycle behaviour. This approach does whiten the noise but also reduces the maximum input signal level in order to prevent overloading of the quantiser; i.e. the SNR is reduced.

It can be seen that for a realistic modulator clock frequency of 200kHz, the in-band noise floor is too high for the required amplifier performance. To be able to achieve the required specification, the quantisation noise needs to be both whitened and shaped more to lower the in-band noise floor.

In theory, the SNR of the first order $\Sigma\Delta$ modulator can be approximated by Equation (3.6) [3.11].

$$SNR = \frac{\pi}{6} (OSR)^{-3/2}$$

(3.6)

For a 60dB SNR, the oversampling ratio (OSR) must be of the order of 64 and therefore for an audio bandwidth of 20kHz, a modulator clock frequency of greater than 2.5MHz

would be required. This would still lead to an impractical switching frequency in the power stage.

Equation (3.5) showed that a first order modulator noise is the first difference of the quantisation noise. The modulator noise can be shaped even more by introducing more feedback loops to make the modulator noise a higher order difference of the quantisation noise. The discrete time equivalent of a second order modulator is shown in Figure 3.23. [3.11].

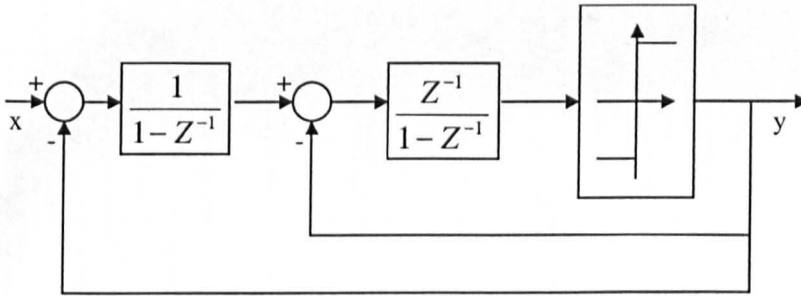


Figure 3.23 - Second order $\Sigma\Delta$ modulator

If the error signal is assumed to be white then the output of the modulator, y , can be expressed as in Equation (3.7).

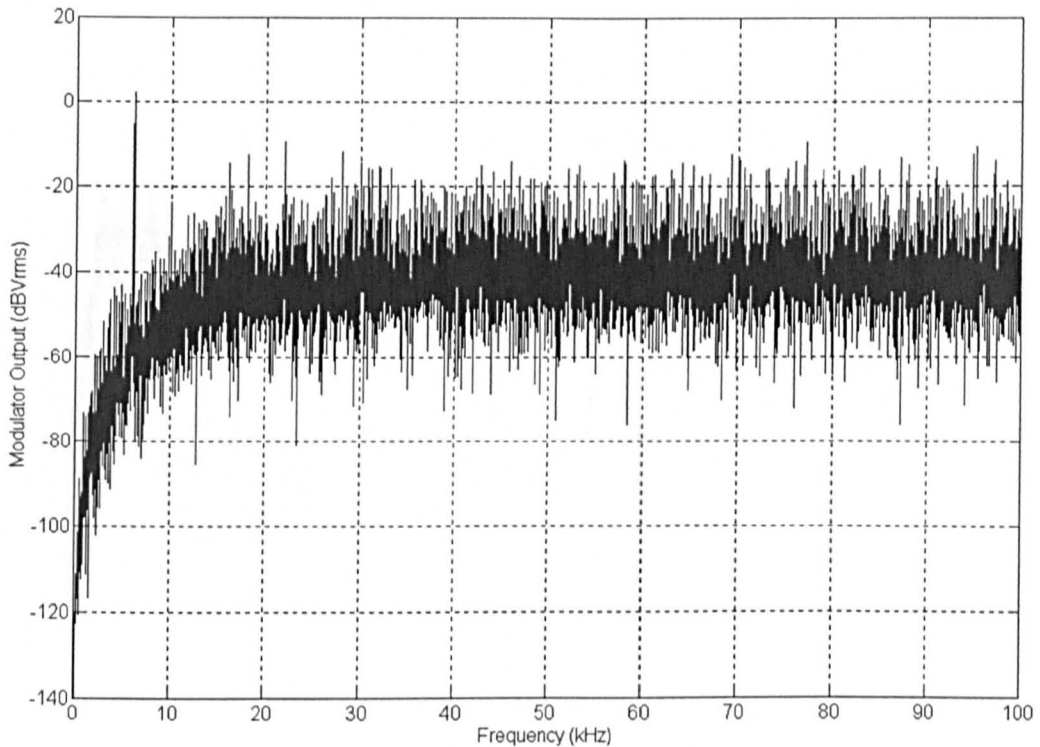
$$y[n] = x[n]z^{-1} + e[n](1 - z^{-1})^2 \quad (3.7)$$

Again, the output of the modulator consists of the input signal (delayed by one sample period) and the shaped error signal. In this case, the noise shaping function is second order. It can be shown [3.11] that the SNR of this second order structure is as shown in Equation (3.8).

$$SNR = \frac{\pi^2}{\sqrt{60}} (OSR)^{-5/2} \quad (3.8)$$

For a SNR of 60dB, the second order modulator would only require an oversampling ratio of 18. This would lead to a clock frequency of 720kHz, which is beginning to approach a more realistic level for a power output stage. For a practical clock frequency of 200kHz, Equation (3.8) suggests a SNR of 30dB for a 20kHz bandwidth modulator. The simulation of this second order modulator with an input of a 6kHz input with 200kHz switching frequency gives a frequency spectrum as shown in Figure 3.24. The

predicted SNR is close to that simulated level over the 20kHz bandwidth. In this simulation, the input modulation depth has been limited to 0.8 to prevent overloading of the quantiser.



Clock Frequency=200kHz, Input Frequency=6kHz, Modulation Depth=80%
Quantisation to $\pm 5V$, Window Used=Hanning, No. Of FFT Points=16384

Figure 3.24 - Simulated spectrum for second order $\Sigma\Delta$ modulator

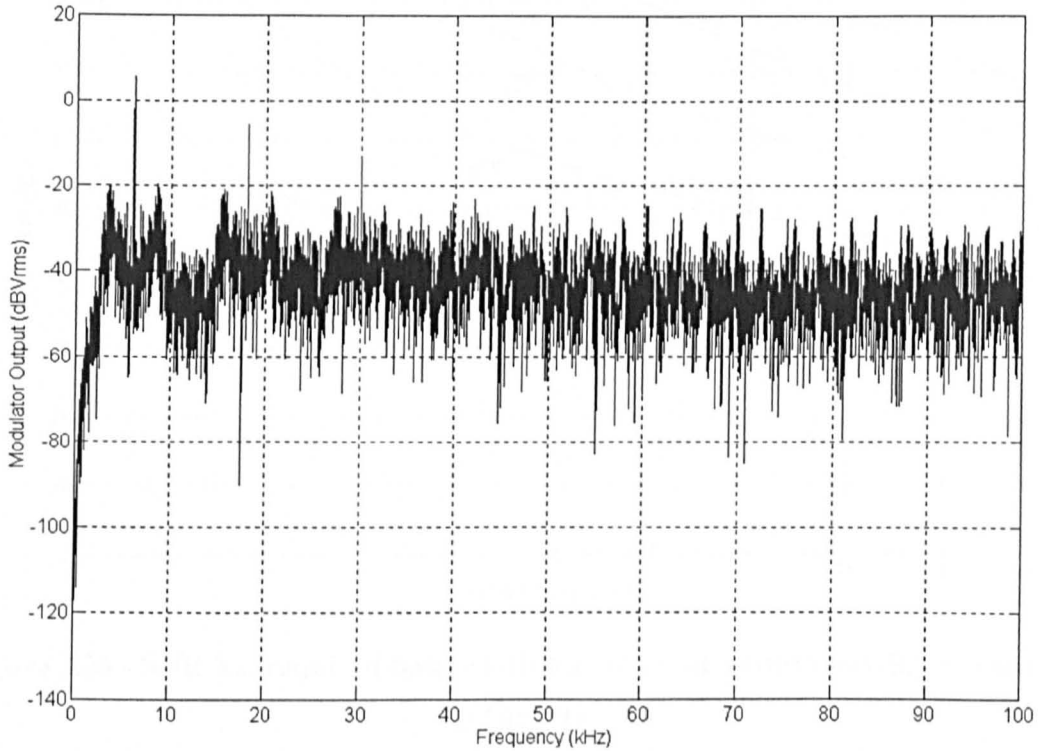
Comparison of Figure 3.21 with Figure 3.24 reveals that the second order modulator not only shapes the quantisation noise more markedly at low frequencies but also the pattern noise so prevalent in the first order modulator has been reduced. The modulator noise is less coloured since the limit cycle behaviour is more random in the second order system.

The benefits introduced with the increasing filter order do not come without problems. Although the second order modulator is unconditionally stable, full modulation depth is not possible due to overloading of the quantiser. Indeed, if a full modulation depth is used then the modulator output spectrum is as shown in Figure 3.25.

Figure 3.25 shows that the effect of overloading the quantiser is two-fold.

1. Odd order harmonic distortion terms appear
2. Noise floor increases at low frequency

Although the increase in modulator order has yielded better performance, the required performance level is still beyond the capability of the second order modulator.



Clock Frequency=200kHz, Input Frequency=6kHz, Modulation Depth=100%
Quantisation to $\pm 5V$, Window Used=Hanning, No. Of FFT Points=16384

Figure 3.25 - Simulated second order spectrum with 100% modulation depth

Assuming the modulator is stable, the SNR can be predicted for a general n^{th} order modulator [3.11] as shown in Equation (3.9).

$$SNR = \frac{\pi^n}{2\sqrt{3(2n+1)}} (OSR)^{\left(n+\frac{1}{2}\right)}$$

(3.9)

As will be demonstrated later, the practical class-D power stage used in the research has a maximum operating frequency of around 300kHz and for this clock frequency, the SNR as a function of required audio bandwidth and modulator order can be calculated using Equation (3.9). Figure 3.26 shows the SNR as a function of required bandwidth for 1st to 8th order modulators all clocked at 300kHz. Evidently, for a 20kHz bandwidth and 60dB SNR, a fourth order modulator is required. Since quantiser overloading limits the maximum achievable modulation depth and Equation (3.9) assumes full modulation depth, in practice an order greater than four may be required.

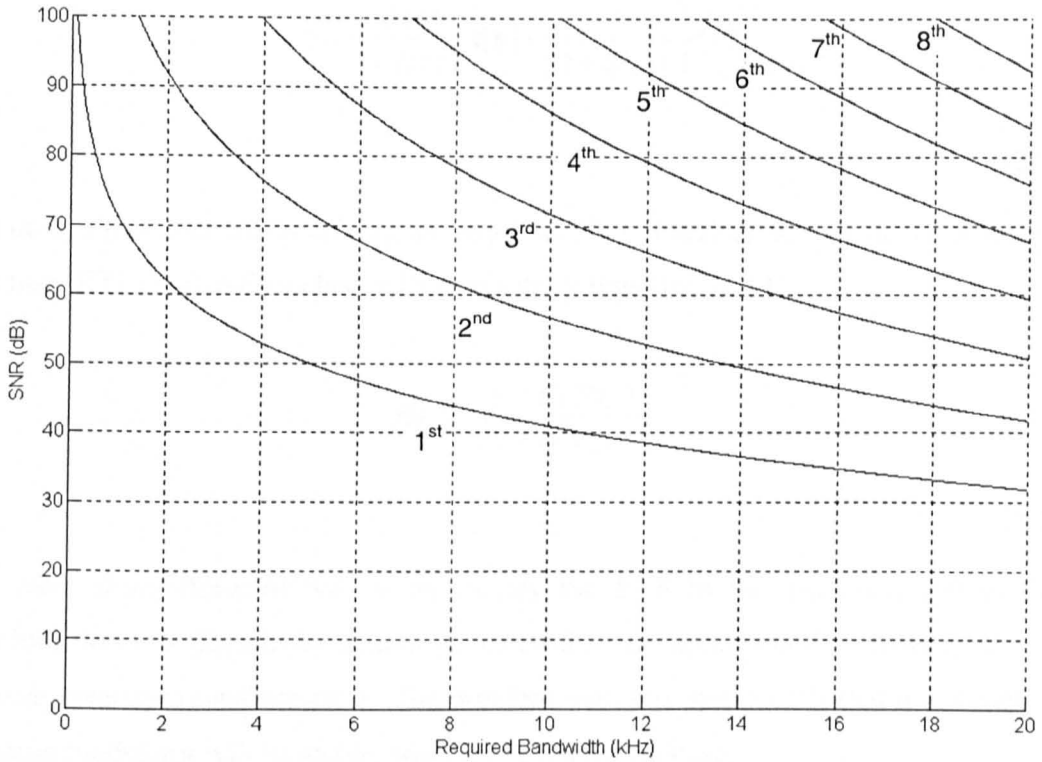


Figure 3.26 - SNR Vs. required bandwidth for 1st to 8th order modulators clocked at 300kHz

3.3.2 Higher Order Design

A number of topologies exist for high order modulator implementation. A simple technique is to use a single feedback loop and a high order filter as shown in Figure 3.27.

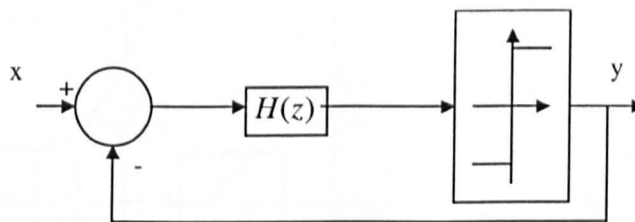


Figure 3.27 - High order implementation

With this structure, a single feedback loop is used and the integrator replaced by a high order transfer function $H(z)$. The output of the modulator can now be expressed as in Equation (3.10).

$$y = \frac{H(z)}{1+H(z)}x[n] + \left(\frac{1}{1+H(z)}\right)e[n]$$

(3.10)

The design proceeds by specifying the required filter characteristic for the error transfer function (ETF) and to then choose $H(z)$ to satisfy Equation (3.11).

$$H(z) = \frac{1 - ETF(z)}{ETF(z)}$$

(3.11)

The most straightforward way is to specify the ETF in the s-domain and to then transform to the z-domain by whichever method seems appropriate (bilinear transform, impulse invariant transform etc.). The problem with this approach is that it assumes the resulting modulator will be stable, which may not be the case.

An approach used by Kershaw and Sandler [3.12] is to specify the filter order and use an automatic adaptive algorithm to modify the position of the poles and zeroes of $H(z)$ in order to find the combination which produces a stable modulator with the lowest inband SNR. The filter structure used in [3.12] is shown in Figure 3.28 and is based on a series of integrators with feedforward and feedback terms.

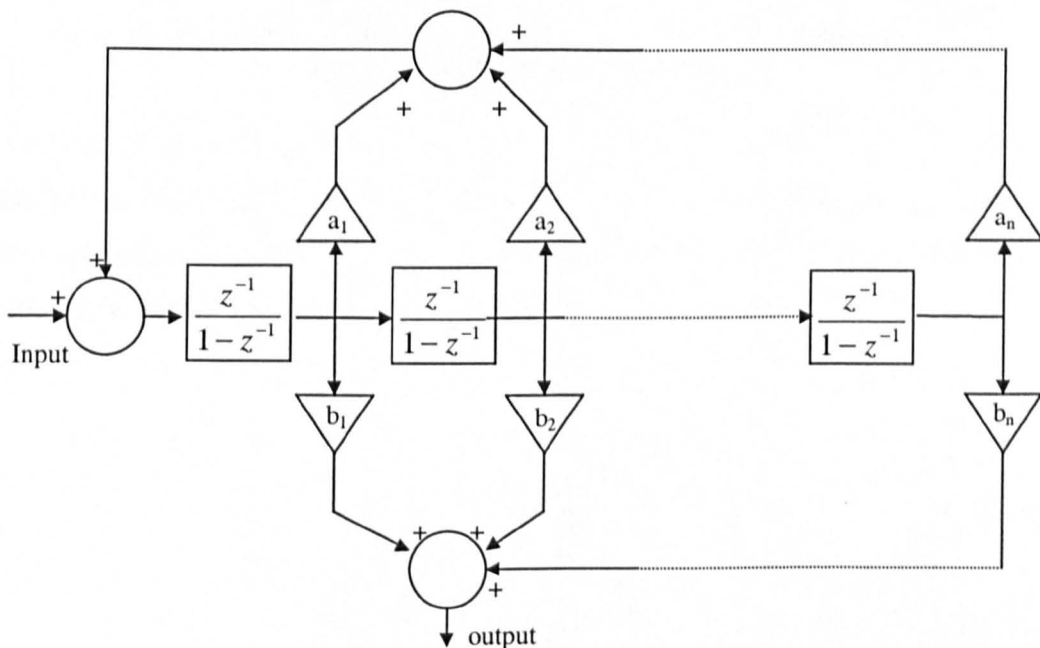


Figure 3.28 - Generalised structure for $H(z)$

The transfer function of the structure shown above can be expressed as in Equation (3.12).

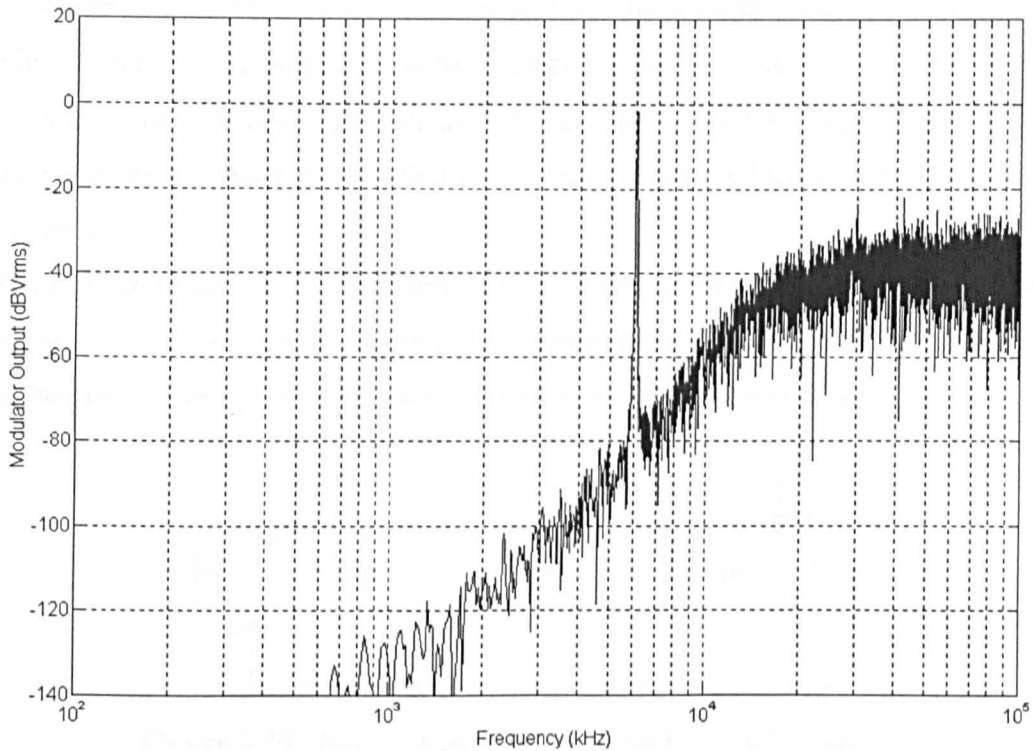
$$H(z) = \frac{b_1(z-1)^{n-1} + b_2(z-1)^{n-2} + \dots + b_{n-1}(z-1) + b_n}{(z-1)^n + a_1(z-1)^{n-1} + \dots + a_{n-1}(z-1) + a_n} \quad (3.12)$$

Using the automatic Adaptive Method, the coefficients for first to fourth order topologies found by Kershaw and Sandler are as shown in Table 3.1.

Coefficients	Filter Order			
	1	2	3	4
b1	1.0	1.0	1.0	1.0
b2	-	0.395625	0.5	0.5459
b3	-	-	0.1301	0.133846
b4	-	-	-	0.022432
a1	0.0059375	0.0028125	0.00001	0.008564844
a2	-	0.00075	0.00116	0.00151
a3	-	-	0.0	0.000001
a4	-	-	-	0.0

Table 3.1 - Optimised coefficients

A simulation of a fourth order modulator using the coefficients above gives the spectrum as shown in Figure 3.29. In practice, the dynamic range of the coefficients above will cause problems with a practical implementation and a more optimal structure for $H(z)$ would lead to an easier implementation.



Clock Frequency=300kHz, Input Frequency=6kHz, Modulation Depth=50%
Quantisation to $\pm 5V$, Window Used=Hanning, No. Of FFT Points=16384

Figure 3.29 – Simulated spectrum from fourth order $\Sigma\Delta$ modulator

Figure 3.29 indicates that the noise spectrum of the fourth order modulator is indeed more random than that of the first and second order types. The maximum modulation depth achievable with this modulator is 50% and the result of exceeding this level is to cause the modulator to lock up into either the positive or the negative state.

Although the modulator noise is now relatively white, the in-band noise floor level is still in excess of the required minimum. If this fourth order modulator were used in practice, it would need to be clocked in the region of 700kHz to achieve an in-band dynamic range of 60dB.

The level of in-band noise is determined by not only the order of the noise shaping function but also the corner frequency at which it begins to attenuate the noise floor. The ideal scenario would be such that the noise-shaping function forces the noise floor to a low enough level that when it enters the baseband, it is at the required 60dB below the fundamental signal.

3.3.3 Alternative Design Methodology

The approach adapted here similarly uses the same single feedback loop and high order filter approach as in Figure 3.27. The method is based on that proposed in [3.13] which

specifies the desired error transfer function and then uses a root-locus approach to verify stability. Since the $\Sigma\Delta$ modulator is to be implemented in analogue circuitry, the new methodology uses the same approach as [3.13] except the analysis is performed in the s -domain and the quantiser is modelled as a linear element, which introduces a random noise signal.

From [3.14] consider a simple one degree of freedom feedback system with an additive noise source, d , as shown in Figure 3.30. Conventionally, 'd' would represent sensor noise but the new design method uses it to model the quantisation noise.

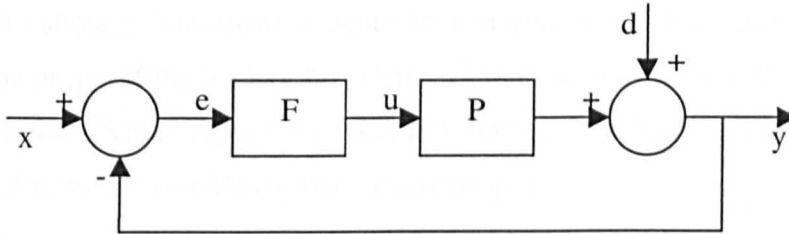


Figure 3.30 - Single degree of freedom feedback system

The output of the single degree of freedom system is that shown in Equation (3.13).

$$y = \frac{FP}{1+FP}x + \frac{1}{1+FP}d \quad (3.13)$$

If FP is large in the baseband, the input signal passes through the system relatively unaffected whilst the disturbance signal is attenuated. Furthermore, if FP is large, then changes in the plant frequency response, P , will have little impact on the overall closed loop frequency response. It is not enough to simply specify the noise-shaping function since this may lead to an unstable system. In [3.14], Belanger provides the following methodology for designing a stable system by defining the Sensitivity and Complimentary Sensitivity functions, $S(s)$ and $T(s)$ as in Equation (3.14).

$$\text{Sensitivity } S(s) = \frac{1}{1+FP} \text{ and Complementary Sensitivity } T(s) = \frac{FP}{1+FP} \quad (3.14)$$

$S(s)$ represents the noise-shaping function whilst $T(s)$ represents the signal transfer function. It should be noted that $T(s)=1-S(s)$ and therefore specification of $S(s)$ will

automatically specify $T(s)$ (and vice-versa). The controller transfer function can now be expressed as in Equation (3.15).

$$F(s) = \frac{T(s)}{S(s)P(s)} \quad (3.15)$$

In order that the controller is realisable, it must have a proper or strictly proper transfer function. For this to be the case, Belanger states that $F(S)$ is proper (strictly proper) if the excess of poles over zeroes of $T(s)$ is equal to (greater than) that of $P(s)$. Since $S(s)=1-T(s)$, the above requirement is equivalent to saying that the controller transfer function will be proper if the leading N_T coefficients of the numerator and denominator of $S(s)$ are identical (Where N_T is pole excess of $T(s)$). I.e., if $S(s)$ has the form shown in Equation (3.16) then $F(s)$ will be proper and realisable.

$$S(s) = \frac{s^n + a_{n-1}s^{n-1} + \dots + a_{m+1}s^{m+1} + (a_m - b_m)s^n + \dots + (a_0 + b_0)}{s^n + a_{n-1}s^{n-1} + a_0} \quad (3.16)$$

With $S(s)$ chosen such that the resulting controller is realisable for the given plant frequency response, the closed loop system stability is dependent on the following three functions showing stability: -

- $T(s)$
- $P^{-1}(s)$
- $P(s)S(s)$

To apply this system to $\Sigma\Delta$ modulator design, the disturbance signal is the quantisation noise, the plant $P(s)$ is a zero-order hold element and the controller $F(s)$ is the noise-shaping element. A first order approximation of a zero-order hold is that given by Equation (3.17) where T is the sample period of the zero order hold.

$$P(s) = \frac{1}{\frac{T}{2}s + 1}$$

(3.17)

The noise-shaping transfer function, $S(s)$, is required to be a high pass characteristic in order that the in-band noise floor is low. Equation (3.17) has a pole excess of one and therefore to realise a strictly proper controller, the leading two terms of the numerator and denominator of $S(s)$ must be identical.

3.3.3.1 Practical Implementation

Consider the case of $S(s)$ being a second order Butterworth high pass filter with a corner frequency of 20kHz. Equation (3.18) gives the transfer function of this filter.

$$S(s) = \frac{s^2}{s^2 + (1.78 \times 10^5)s + (1.58 \times 10^{10})}$$

(3.18)

The controller will be realisable if the leading two coefficients of the numerator and denominator of $S(s)$ are identical. Therefore, $S(s)$ must be modified as shown in Equation (3.19).

$$S(s) = \frac{s^2 + (1.78 \times 10^5)s}{s^2 + (1.78 \times 10^5)s + (1.58 \times 10^{10})}$$

(3.19)

By changing the high pass characteristic $S(s)$ into one that results in a proper controller, the noise-shaping function has been altered. Figure 3.31 shows the magnitude responses of the simple second order high pass filter and the modified second order filter.

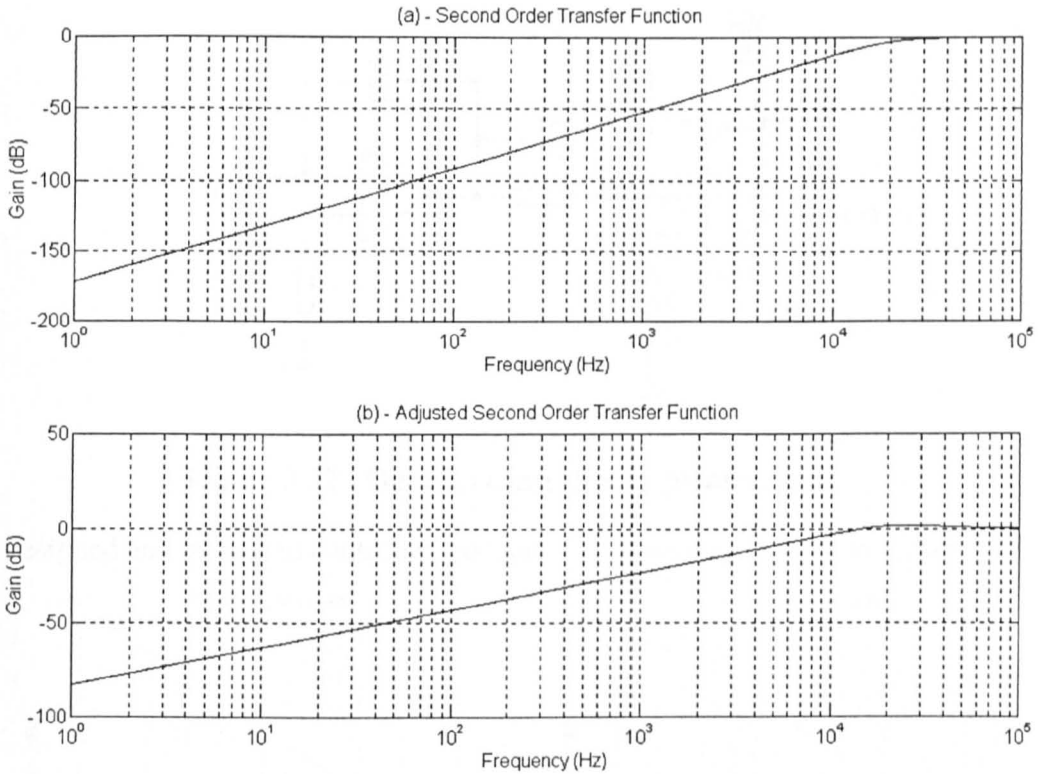


Figure 3.31 - Normal and adjusted second order transfer functions

The necessity to have a proper controller has resulted in the movement of one of the error transfer function zeroes away from DC to approximately 28kHz. This results in a lowering of the roll-off at low frequencies to 20dB/decade, i.e. approximately equivalent to a first order modulator.

For the second order response as described in Equation (3.19), the controller transfer function can be determined using Equations (3.15) and (3.17). For a sample and hold clock frequency of 200kHz, the required controller transfer response is as shown in Equation (3.20).

$$F(s) = 39500 \frac{s + 400000}{s(s + 178000)} \quad (3.20)$$

The controller was implemented using an integrator followed by a pole-zero network as shown in Figure 3.32.

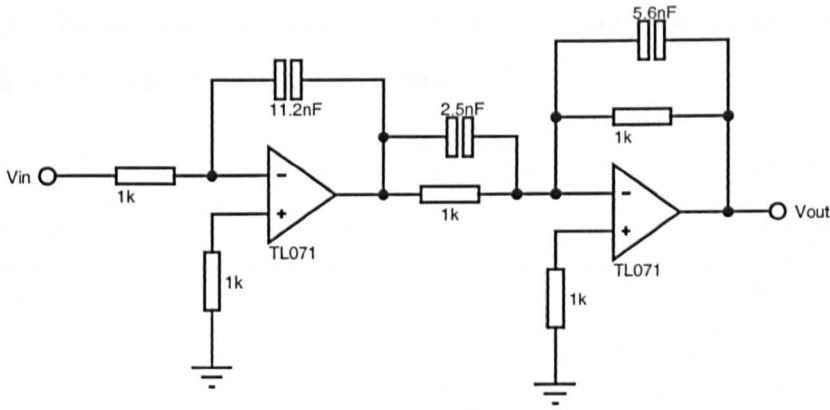


Figure 3.32 - Op-amp controller implementation

The designed and measured controller frequency responses are shown in Figure 3.33.

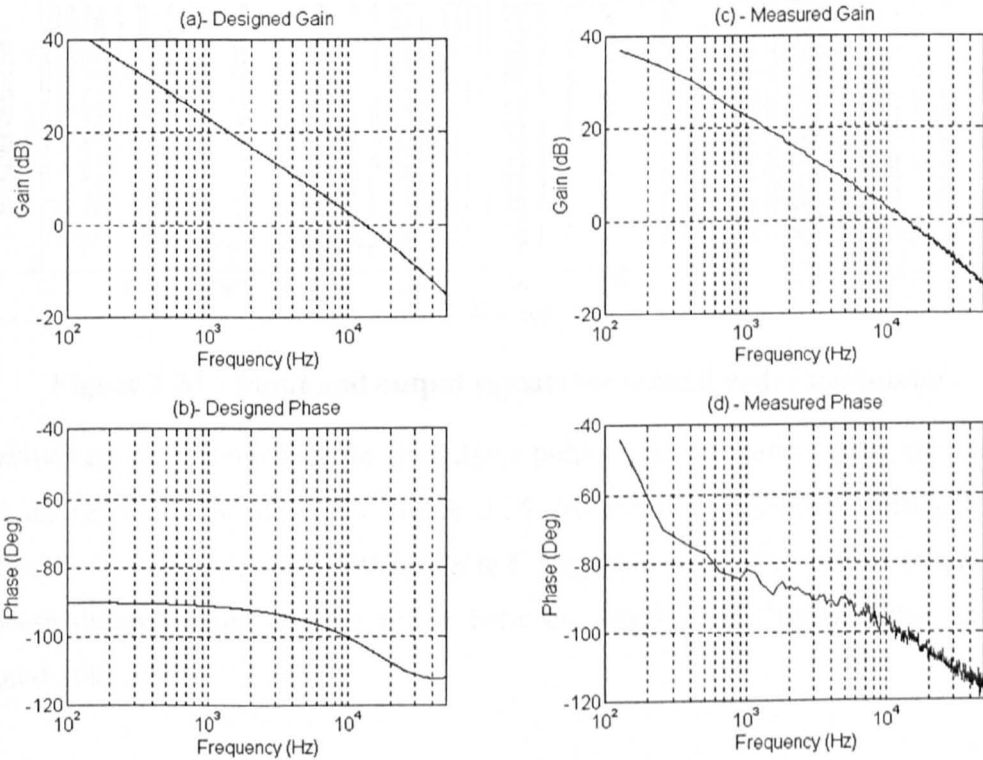


Figure 3.33 - Design and measured controller frequency responses

Comparison of the designed and measured gains shows a very close correlation. Although the phase responses show a significant difference at low frequency, this is most likely due to measurement error in the first few points from the spectrum analyser. The rest of the modulator was realised with a comparator, d-type flip-flop and pulse shaping circuit (see appendix C). The modulator stability was verified first by simulation and then in practice with a 200kHz clocked modulator and 1.2kHz input

frequency at 90% modulation depth. The graph in Figure 3.34 shows a typical input audio signal and output modulation waveform.

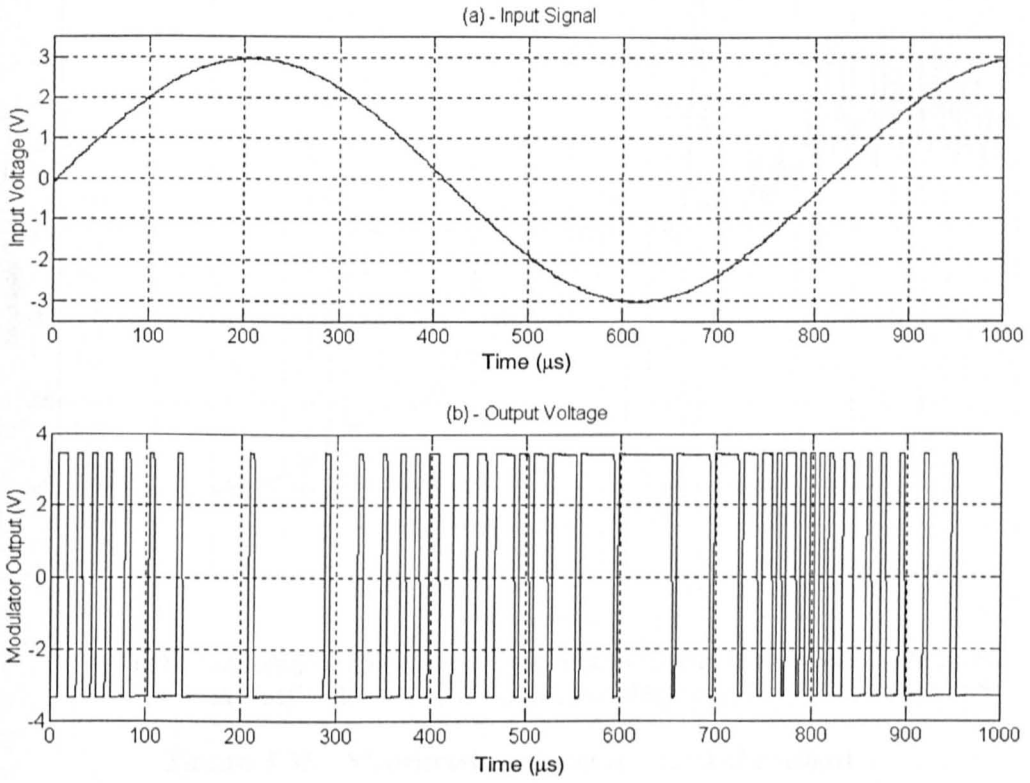
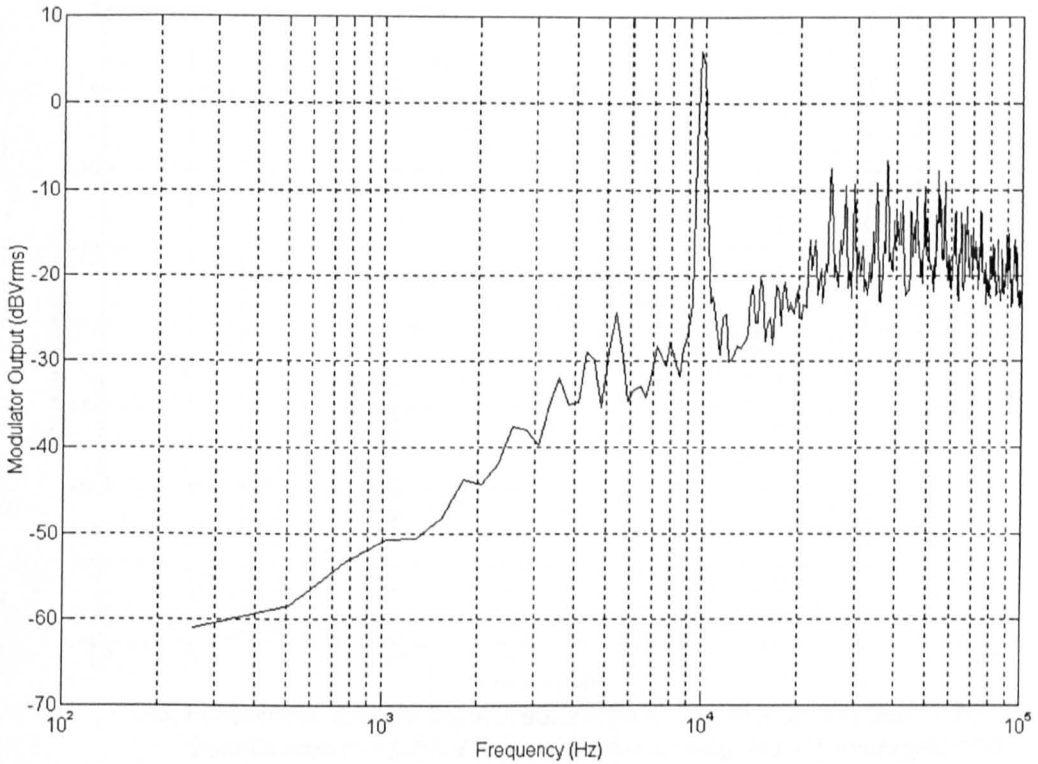


Figure 3.34 - Input and output signals for second order modulator

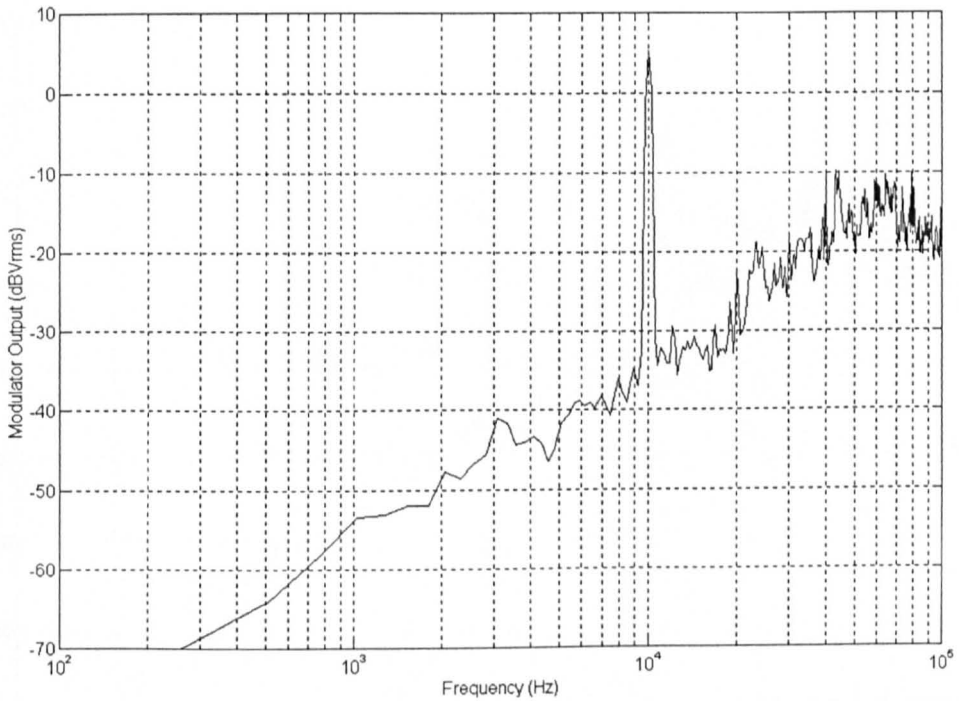
The actual spectral content of the modulator output was examined using the dynamic signal analyser and is shown in Figure 3.35. Whilst the noise-floor rolls off at the expected first-order rate of 20dB/decade (c.f. Figure 3.31(b)), the corner frequency of the noise-shaping filter appears to be between 40kHz and 50kHz rather than the designed 20kHz.



Clock Frequency=200kHz, Input Frequency=10kHz, Modulation Depth=75%
Quantisation to $\pm 3.4V$, Window Used=Hanning, No. Of Averages=100

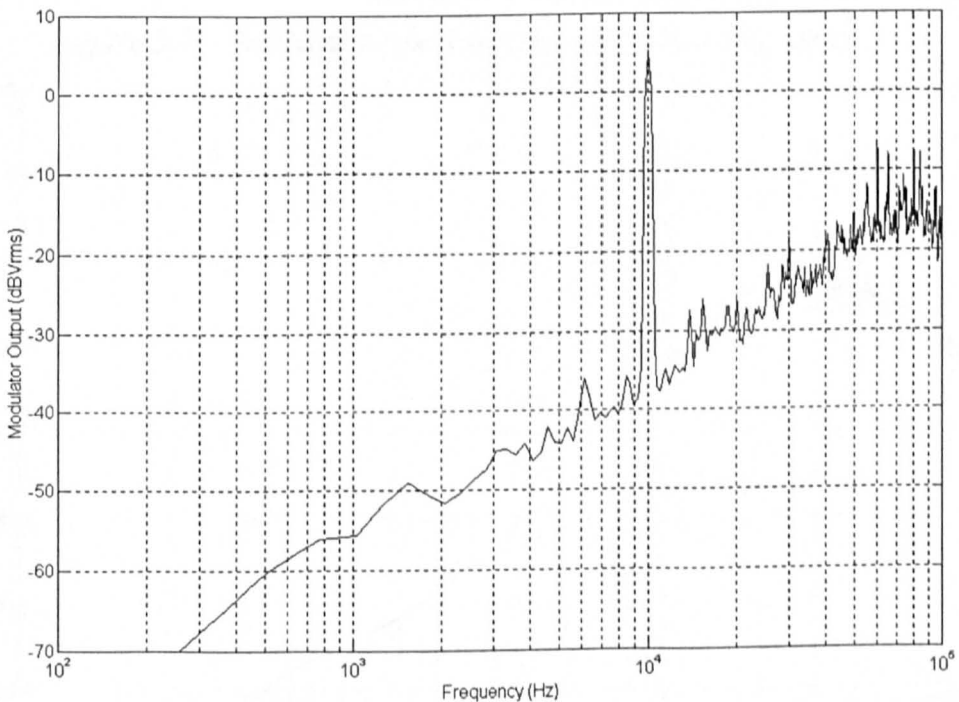
Figure 3.35 - Measured modulator spectral content

The noise-shaping function shows an under-damped response, which suggests that the loop gain of the practical modulator is higher than expected. Experimentation with the clock frequency for the same controller implementation shows that the clock frequency has a small effect on the noise shape. Figure 3.36 and Figure 3.37 show the measured spectral content for clock frequencies of 300kHz and 400kHz respectively. The increase in clock frequency has the effect of increasing the corner frequency of the error transfer function. This is due to the increase in bandwidth of the plant frequency response (see Equation (3.17)). The effect of changing the designed corner frequency of the error transfer function can be seen in Figure 3.38, Figure 3.39 and Figure 3.40. These spectra are taken from a second order modulator with a designed corner frequency of 5kHz and clock frequencies of 200kHz, 300kHz and 400kHz respectively. The lower corner frequency is apparent with this modulator and the under-damped nature of the error transfer function (ETF) is more evident.



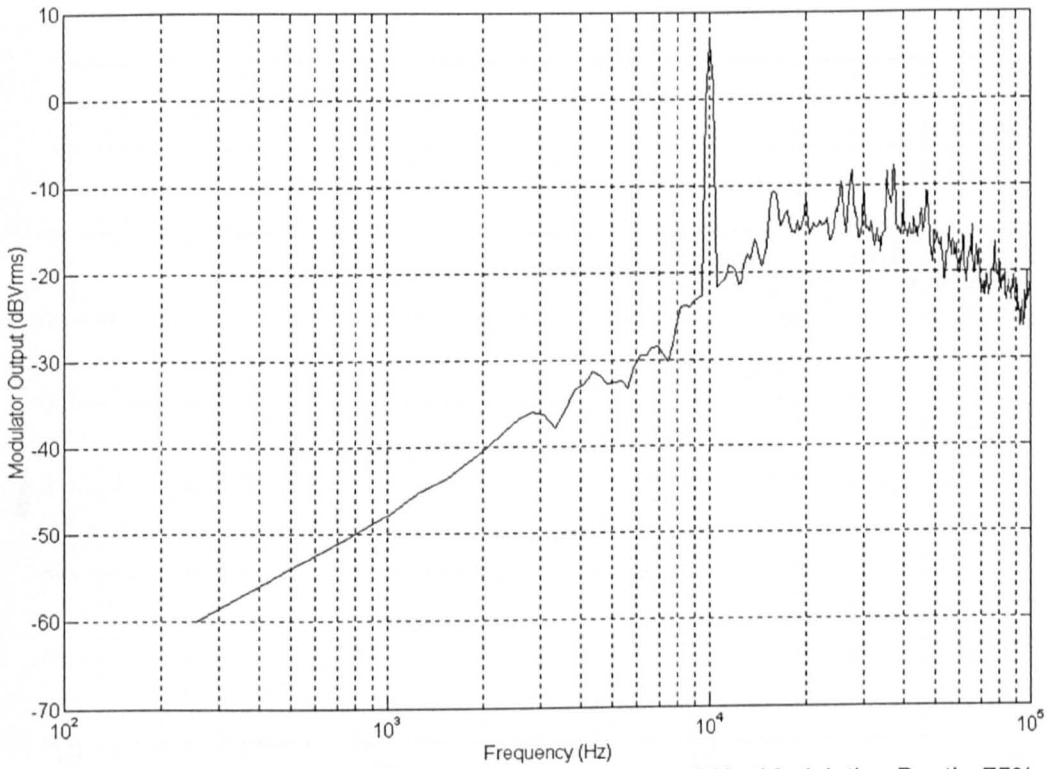
Clock Frequency=300kHz, Input Frequency=10kHz, Modulation Depth=75%
 Quantisation to $\pm 3.4V$, Window Used=Hanning, No. Of Averages=100
 2nd Order 20kHz Corner Designed Error Transfer Function

Figure 3.36 - Modulator spectral content (20kHz design corner)



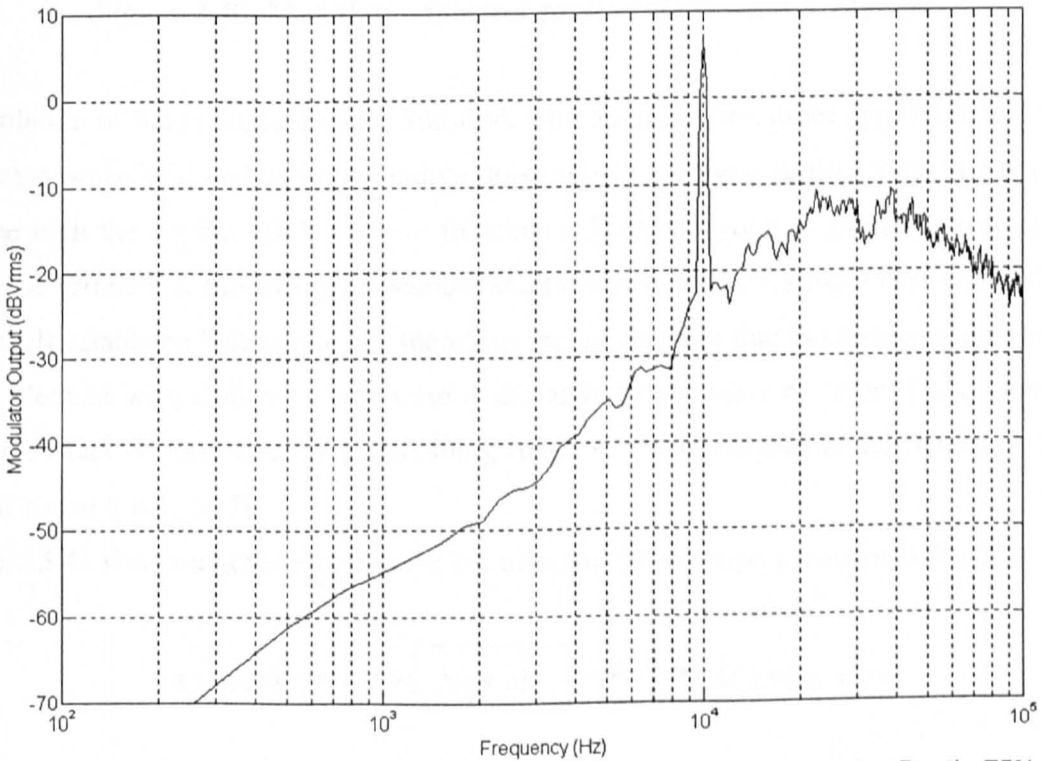
Clock Frequency=400kHz, Input Frequency=10kHz, Modulation Depth=75%
 Quantisation to $\pm 3.4V$, Window Used=Hanning, No. Of Averages=100
 2nd Order 20kHz Corner Designed Error Transfer Function

Figure 3.37 - Modulator spectral content (20kHz design corner)



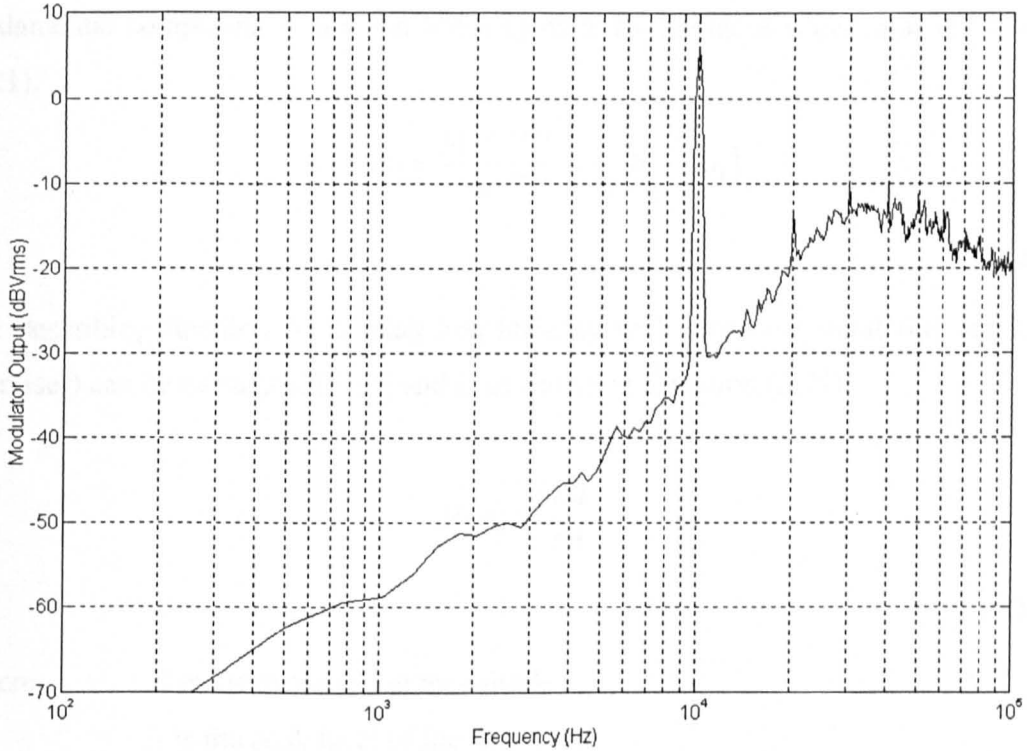
Clock Frequency=200kHz, Input Frequency=10kHz, Modulation Depth=75%
 Quantisation to $\pm 3.4V$, Window Used=Hanning, No. Of Averages=100
 2nd Order 5kHz Corner Designed Error Transfer Function

Figure 3.38 - Modulator spectral content (5kHz design corner)



Clock Frequency=300kHz, Input Frequency=10kHz, Modulation Depth=75%
 Quantisation to $\pm 3.4V$, Window Used=Hanning, No. Of Averages=100
 2nd Order 5kHz Corner Designed Error Transfer Function

Figure 3.39- Modulator spectral content (5kHz design corner)



Clock Frequency=400kHz, Input Frequency=10kHz, Modulation Depth=75%
 Quantisation to $\pm 3.4V$, Window Used=Hanning, No. Of Averages=100
 2nd Order 5kHz Corner Designed Error Transfer Function

Figure 3.40- Modulator spectral content (5kHz design corner)

Simulation of the modulator using Simulink with a simple first order approximation for the zero order hold and additive random noise source for the quantiser yielded a noise-shape with the correct 20kHz corner frequency. Therefore, one of the approximations must be erroneous. Modelling the sample and hold element by a simple first order filter is a well-established technique and therefore, the assumption that the quantiser is a unity gain element with additive white noise is the more likely cause of error. The quantiser could in fact be modelled by a describing function where its gain is dependent on the input signal level [3.15].

Figure 3.41 shows a generic non-linear element and its effect on a sinusoidal input.

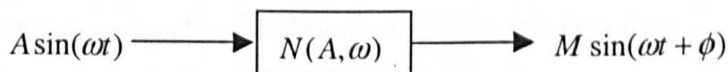


Figure 3.41 – Describing function representation of a non-linear element

The actual describing function, $N(A, \omega)$, is defined in [3.15] as the complex ratio of the fundamental component of the non-linear element by the input sinusoid as in Equation (3.21).

$$N(A, \omega) = \frac{M e^{j(\alpha\omega + \phi)}}{A e^{j\alpha\omega}} = \frac{1}{A} (b_1 + j a_1) \quad (3.21)$$

The describing function for a relay non-linearity with sinewave input (i.e. single bit quantiser) can be calculated [3.15] and is as shown in Equation (3.22).

$$N(A) = \frac{4M}{\pi A} \quad (3.22)$$

Where, M is the quantisation magnitude
 A is the peak level of the sinewave.

Note that this particular describing function is independent of frequency due to the single-valued nature of the non-linearity. Thus, the gain of the single-bit quantiser can vary from zero for infinitely large inputs, to infinity for infinitesimally small inputs. This variation in gain is the most likely cause of the under-damped error transfer function seen in Figure 3.35. If the quantiser is modelled as a variable gain element, the single-degree of freedom system of Figure 3.30 becomes as shown in Figure 3.42.

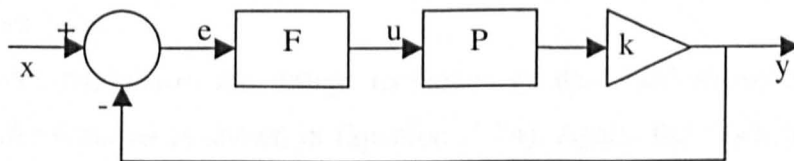


Figure 3.42 - Single degree of freedom system with variable gain element

The noise-shaping function defined in Equation (3.13) now becomes: -

$$ETF(s) = \frac{1}{1 + kFP} \quad (3.23)$$

The impact of the variable gain, k , can be seen if the noise shaping function is plotted for the second order modulator designed for 20kHz corner frequency. Figure 3.43 shows the resulting ETF with k varied from 1 to 10.

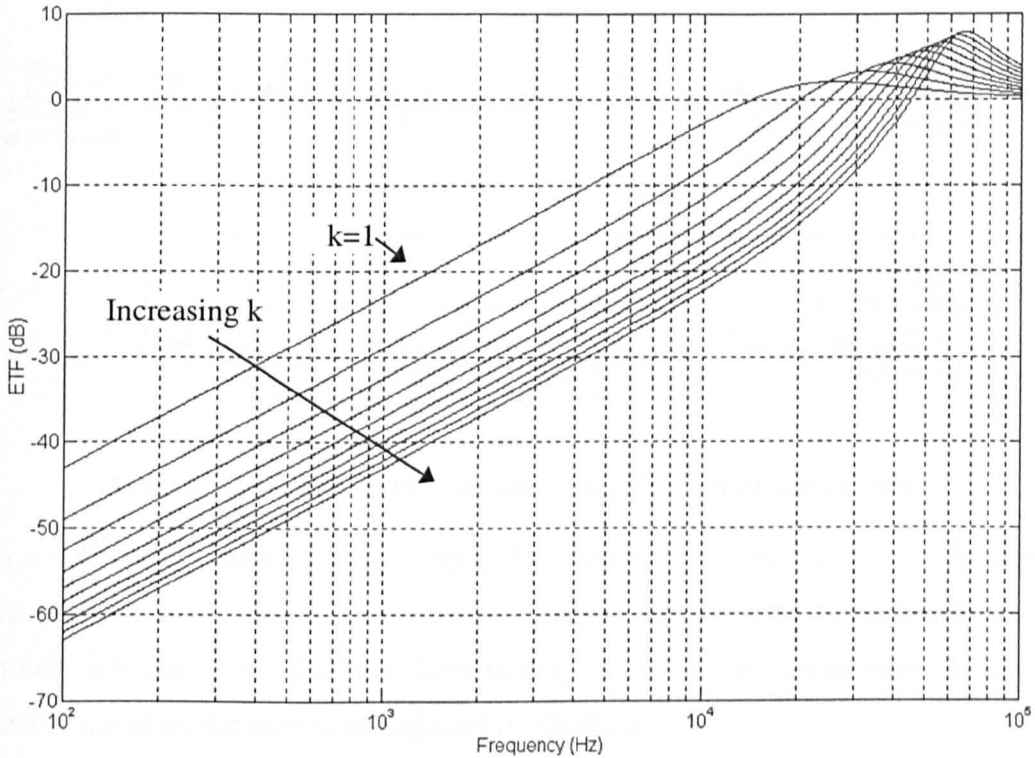


Figure 3.43 - Error transfer function with k varied from 1 to 10

With $k=1$, the ETF shows the same behaviour as Figure 3.31(b) which is to be expected. As the gain increases, the ETF becomes increasingly under-damped and the effective corner frequency increases. Whilst this is beneficial in lowering the inband noise floor, the out-of band noise increases and this is likely to compromise the stability of higher order modulators.

For a third order modulator, the design methodology described above results in a controller transfer function as shown in Equation (3.24). Again, the clock frequency is chosen as 200kHz.

$$F(s) = 50 \frac{(s + 400000)(1579s + 0.99 \times 10^8)}{s^2(s + 251000)} \quad (3.24)$$

When constructed, this modulator showed an unstable behaviour in that it locked up into low frequency oscillations with the input signal having no influence on the output signal. The modulator was simulated using Simulink™ to establish whether the

oscillation was a problem with the practical implementation or a problem with the design methodology. Figure 3.44 shows the model used in Simulink™ to verify the stability of the third order modulator.

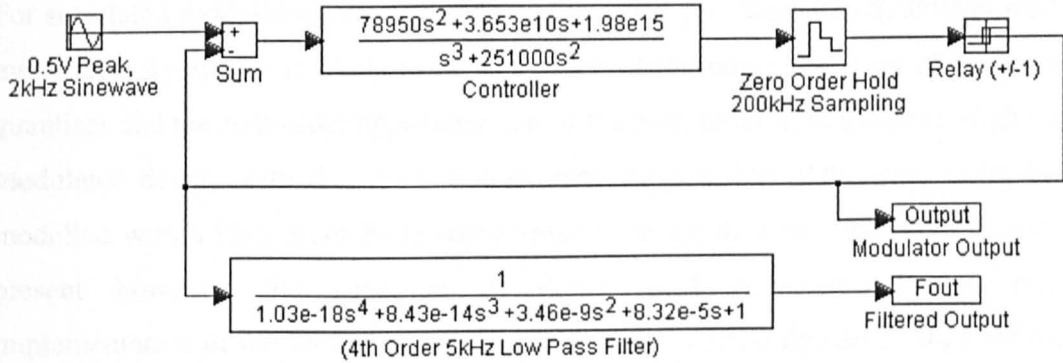


Figure 3.44 – Simulink™ model of the 3rd order modulator

With a 0.5V peak, 2kHz sinewave input, the simulation of the third order modulator above demonstrated stability. The modulator output, and the output after being filtered is shown in Figure 3.45. The waveform is very pure since the input signal is only at 2kHz and therefore the oversampling ratio is effectively 50.

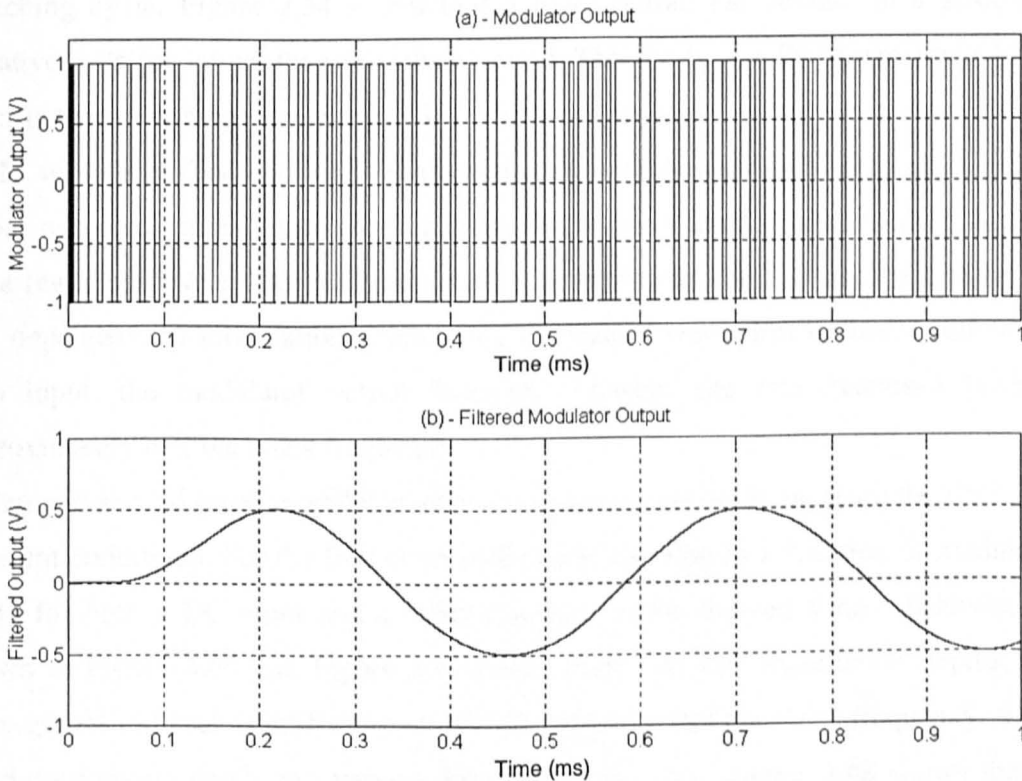


Figure 3.45 - Filtered third order modulator output

The simulation demonstrates that the new design methodology can result in stable high order modulators although with practical implementation, problems do arise. The most likely cause of the failure of the practical modulators beyond second order is through problems such as slew rate and DC offset within the op-amps used for realisation.

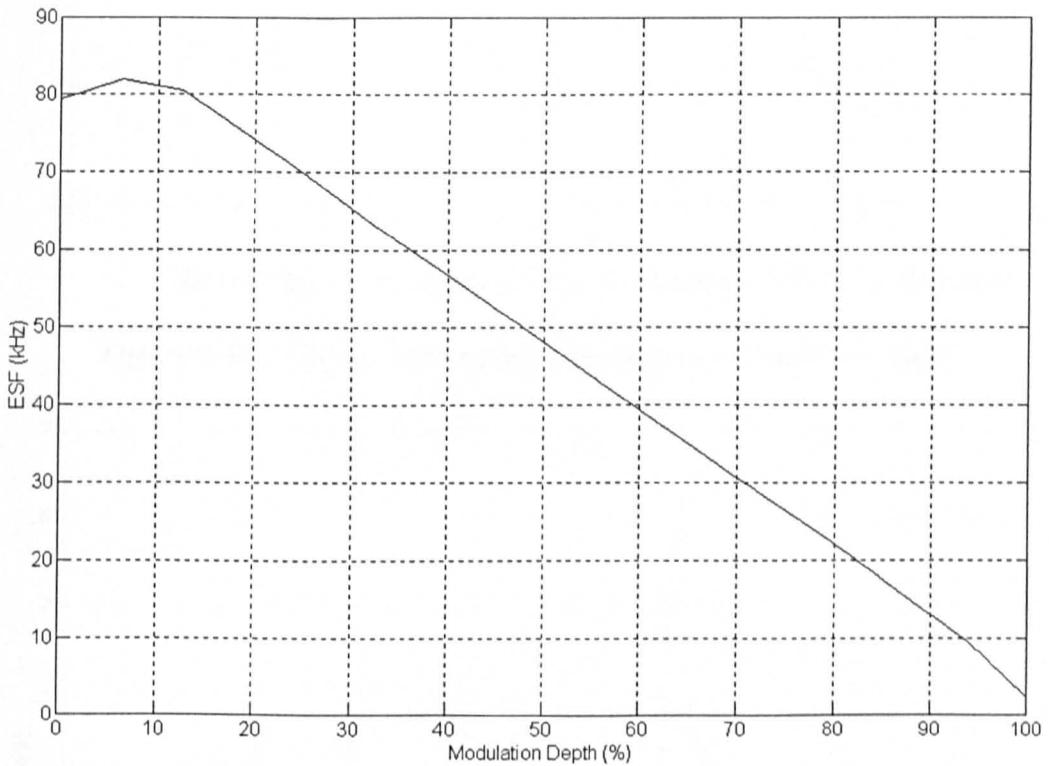
For simulated modulators of order greater than three, this design methodology results in instability. Again this is likely to be as a result of the non-linear gain of the single-bit quantiser and the first order approximation of the zero-order hold element. Higher order modulator design with this methodology may be possible if the zero order hold is modelled with a high order Pade approximation rather than the first order element. At present however, the spectrum of Figure 3.36 demonstrates that practical implementation of the second order modulator gives a 35dB dynamic range for a clock frequency of 300kHz for a 20kHz bandwidth amplifier. To achieve the required 60dB resolution with this modulator, the available bandwidth would have to be reduced to 1kHz and the power filter designed to reject anything above this frequency.

3.4 Effective Switching Frequency

Whereas a PWM waveform will have one low to high and one high to low transition per switching cycle, Figure 3.34 shows that a PDM output can remain in a positive or negative state for longer than one clock period. This leads to a PDM waveform having an effective switching frequency (ESF) which can be significantly lower than that of a PWM waveform. The ESF will be a function of modulation depth since a larger input signal will result in an increased likelihood of the modulator state remaining the same for a few clock cycles. As the modulator order increases, the ESF is likely to become less dependent on modulation depth since the output waveform is more random. For zero input, the modulator output ‘bounces’ between the two quantised levels at approximately half the clock frequency.

A first and second order modulator were constructed in order to measure the ESF under different conditions. For the first order modulator, the ESF as a function of modulation depth for both a DC input and a 6kHz sinewave input showed similar behaviour, as shown in Figure 3.46 and Figure 3.47 respectively. At low modulation depths, both these graphs indicate an ESF close to 100kHz which is half the clock frequency. With a fixed modulation depth and varying baseband frequency, Figure 3.48 shows that the ESF is relatively constant with frequency. In-fact, the ESF for the first order modulator is mainly dependent on modulation depth.

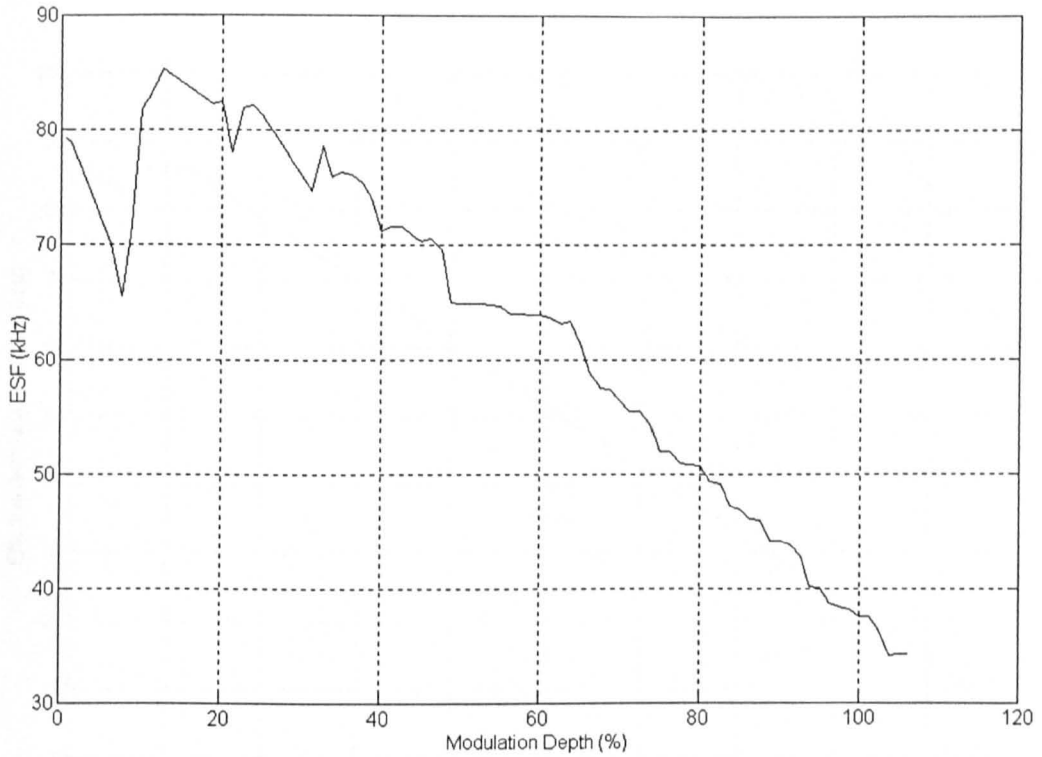
For the second order modulator, the DC characteristic in Figure 3.49 shows very similar behaviour to the DC characteristic for the first order modulator. A significant difference becomes apparent when an increasing modulation depth sinewave input is used. Whereas the first order modulator showed an almost linearly decreasing ESF with modulation depth, Figure 3.50 shows that the ESF of the second order modulator does not significantly vary with modulation depth. This is most likely due the increased randomness of the third order modulator over the first order. Interestingly, the ESF of the third order modulator shows a stronger variation with baseband frequency, Figure 3.51.



DC Input, Clock Frequency=200kHz, First Order Modulator

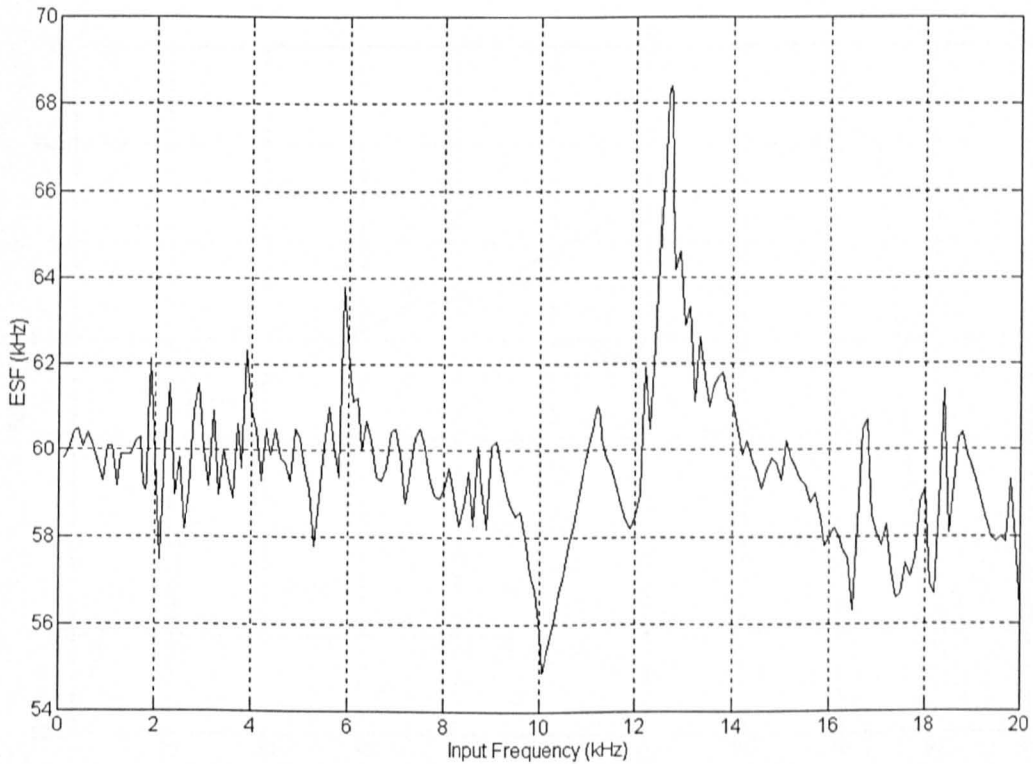
Figure 3.46 - ESF for first order modulator and DC input

The ESF profile of Figure 3.46 demonstrates that a PDM modulator can be clocked at 2.5 times the clock frequency of a corresponding PWM modulator for an equivalent switching rate.



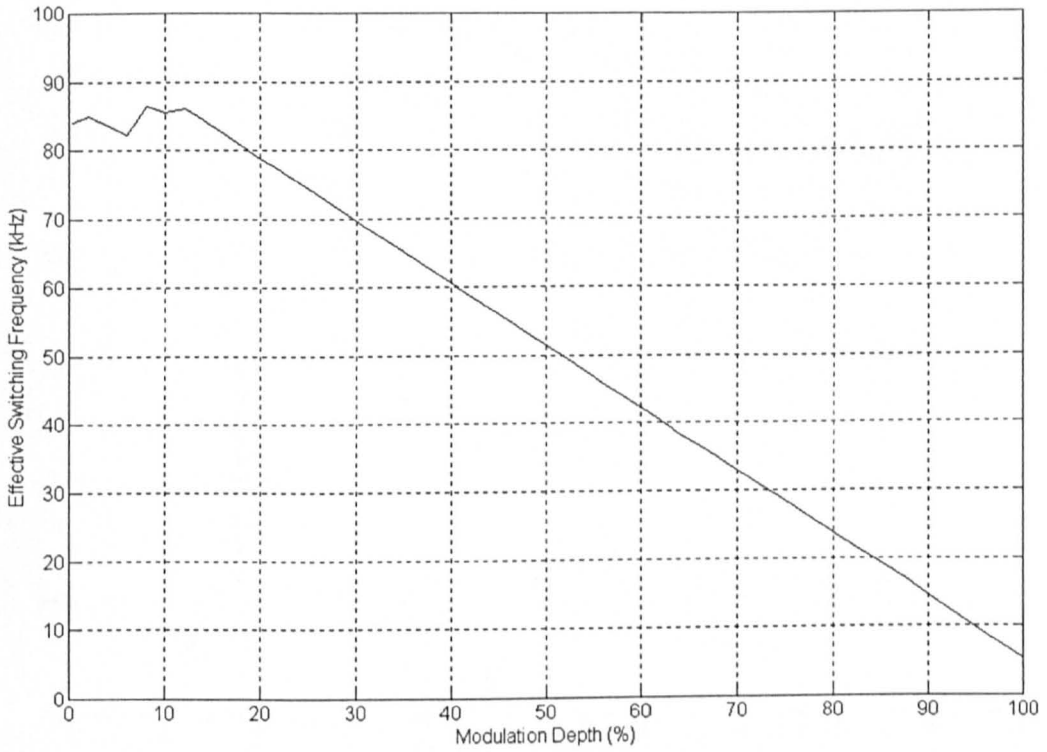
6kHz Sinewave Input, Clock Frequency=200kHz, First Order Modulator

Figure 3.47 - ESF for first order modulator and sinewave input



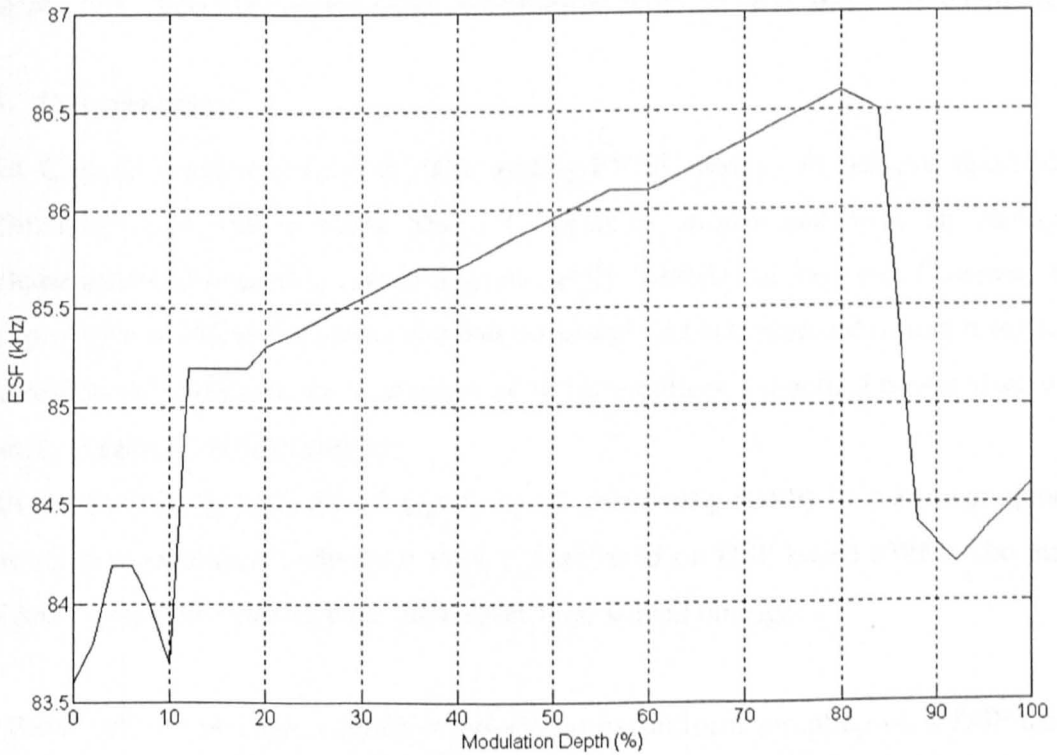
60% Depth Sinewave Input, Clock Frequency=200kHz, First Order Modulator

Figure 3.48 - ESF for variable frequency sinewave input for a first order modulator



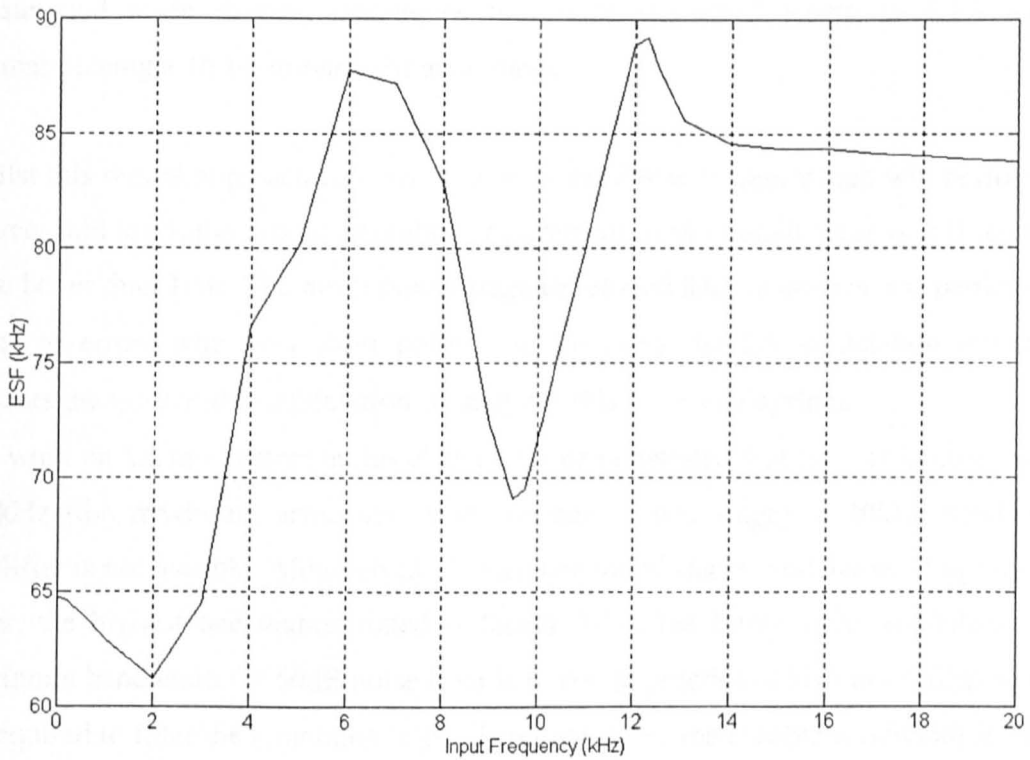
Clock Frequency=200kHz, DC Input, Second Order Modulator

Figure 3.49 - ESF for second order modulator and DC input



Clock Frequency=200kHz, Constant 6kHz Sinewave Input, Second Order Modulator

Figure 3.50- ESF for second order modulator and sinewave input



Clock Frequency=200kHz, 60% Sinewave Modulation Depth, Second Order Modulator

Figure 3.51 - ESF for second order modulation with variable sinewave frequency

3.5 Conclusions

Most Class-D amplifiers to date have used a PWM strategy to achieve reasonable performance and with a 60dB SNR, it has been shown that with an analogue implementation, a switching rate of approximately 150kHz can be used. However, the analogue system still suffers from inherent noise and with a theoretical timing resolution requirement of ± 140 ps for the equivalent of 16-bit accuracy, a practical power stage will severely compromise performance.

With the increasing viability of digital signal processing (DSP) in consumer goods, more recent modulation techniques have concentrated on DSP based PWM. The main problems with DSP systems have previously been solved through: -

- Reduction of harmonic distortion introduced by uniform sampling on a DSP using pre-compensation schemes.

- Reduction of the timing resolution requirement of the output stage by using over-sampled noise shaping techniques to reduce the word length to 8-bit whilst maintaining a 16-bit in-band dynamic range.

Whilst this digital approach can lead to a practical PWM system which will perform to the required level, the timing resolution requirement of the output stage is still required to be better than 10ns. The novel power stage developed later in chapter 5 is particularly prone to errors with very short pulses and therefore the $\Sigma\Delta$ modulation technique presents the most viable modulation strategy for this particular system.

The work on $\Sigma\Delta$ modulators in this chapter has demonstrated that for a switching rate of 300kHz (the maximum achievable with the new power stage), a 20kHz bandwidth amplifier is not feasible. Although [3.13] has mentioned stable modulators of up to sixth order, the highest one demonstrated is fourth. With the fourth order modulator, the maximum bandwidth for 60dB noise floor is 6kHz. In practice, a high order filter would be required to filter the remaining in-band component so the useable bandwidth is likely to be lower than this.

The practical modulators resulting from the new design methodology have indicated that the achievable dynamic range for a 300kHz switching frequency is 35dB for a 20kHz bandwidth. If 60dB is required, the bandwidth must be dropped to the region of 1kHz. Further work on the new design methodology should lead to stable higher order modulators and the most likely problem with the methodology now is the modelling of the zero-order hold. A higher order approximation to the zero-order order, for example a high order Pade approximation, should result in stable high order designs.

4 Prototype Class-D Power Stage

4.1 Introduction

In order to understand the performance limitations of a practical Class-D power stage, a prototype H-Bridge was constructed, Figure 4.1. The power devices chosen will allow for load currents of up to 30A and a link voltage of up to 200V. In free-air, the heatsink has a dissipation potential of $0.7^{\circ}\text{C}/\text{W}$ and therefore will allow for the dissipation of power losses of up to 100W (Assuming an ambient below 40°C). The dead time can be set independently on each power MOSFET from 200ns to $10\mu\text{s}$. Full circuit diagrams of the amplifier are given in appendix C.

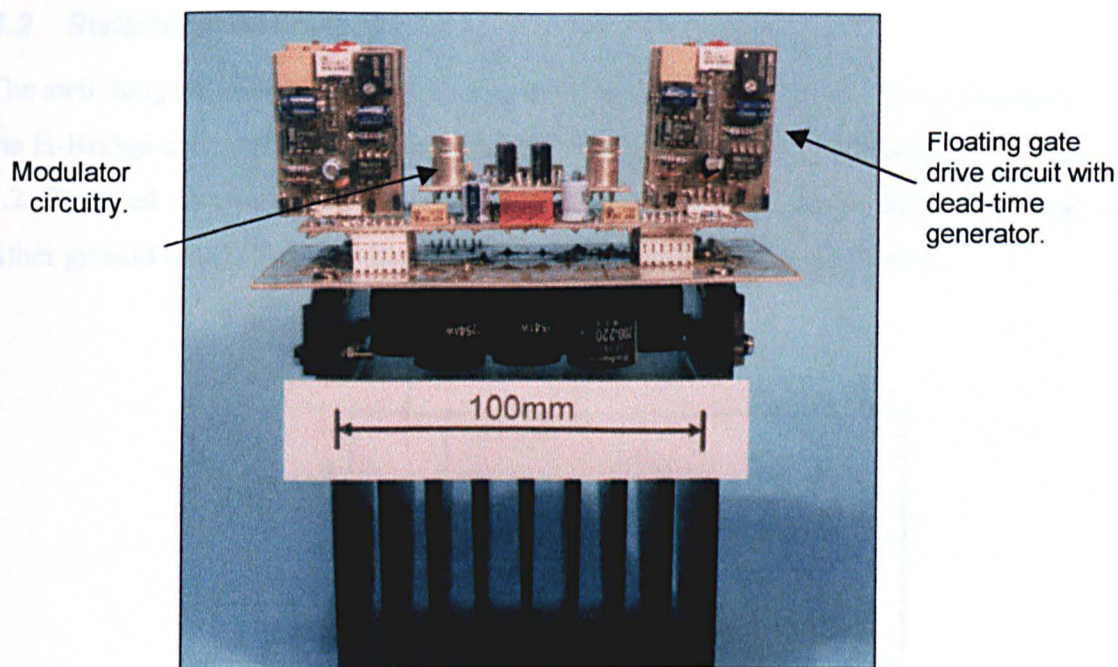


Figure 4.1 - Full bridge power converter

The layout was optimised as to minimise the effect of parasitic inductance by keeping all devices of each of the two power stage legs very close to one-another, placing the DC link decoupling capacitors adjacent to the power semiconductors and using a coplanar bus-bar arrangement. The modulation circuitry can be changed easily by replacing a single PCB on the top of the power stage.

The power stage has been used to measure typical operating efficiencies and to examine the behaviour of the power devices under real switching conditions. In addition, the mechanisms leading to output waveform distortion are examined. The power filter is not

incorporated into the power stage to allow for flexibility in changing the load characteristics. Examination of the power stage behaviour was targeted towards two main objectives: -

1. An analysis of the power semiconductor switching behaviour to compare the predicted losses with measured efficiencies.
2. An analysis of non-ideal operational characteristics of the power stage and their impact on distortion.

The chapter concludes with a discussion of the methods which can be used in practice to linearise the power stage in order to meet the Hi-Fidelity requirements of the amplifier.

4.2 Switching Behaviour

The switching behaviour of the H-Bridge devices was examined by using a single-leg of the H-Bridge and analysing the currents and voltages during the switching event, Figure 4.2. The load current polarity was set by connecting the non-driven end of the load to either ground or +45V for positive and negative load currents respectively.

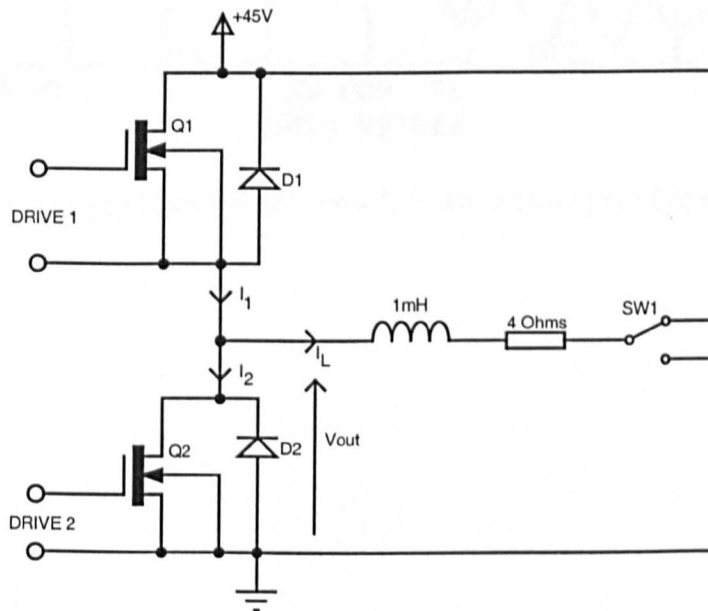


Figure 4.2 - Single leg used for switching behaviour analysis

The individual device currents, I_1 and I_2 , were measured in-circuit using a high bandwidth Rogowski coil (See appendix E for specifications) whilst V_{OUT} was measured using a $\times 100$ high bandwidth oscilloscope probe. For both the positive and

negative load current, the single leg was driven at 50% duty cycle to give a continuous load current of approximately 5A. In all cases, the gate drive resistances were set to 2Ω . For the negative load current, Figure 4.3 and Figure 4.4 show I_1 and I_2 respectively when Q2 switches off whilst Figure 4.5 and Figure 4.6 show I_1 and I_2 when Q2 switches on. With a positive load current, Figure 4.7 and Figure 4.8 show I_1 and I_2 respectively when Q1 switches off whilst Figure 4.9 and Figure 4.10 show I_1 and I_2 when Q1 switches on. All plots are at a timebase of 50ns/div.

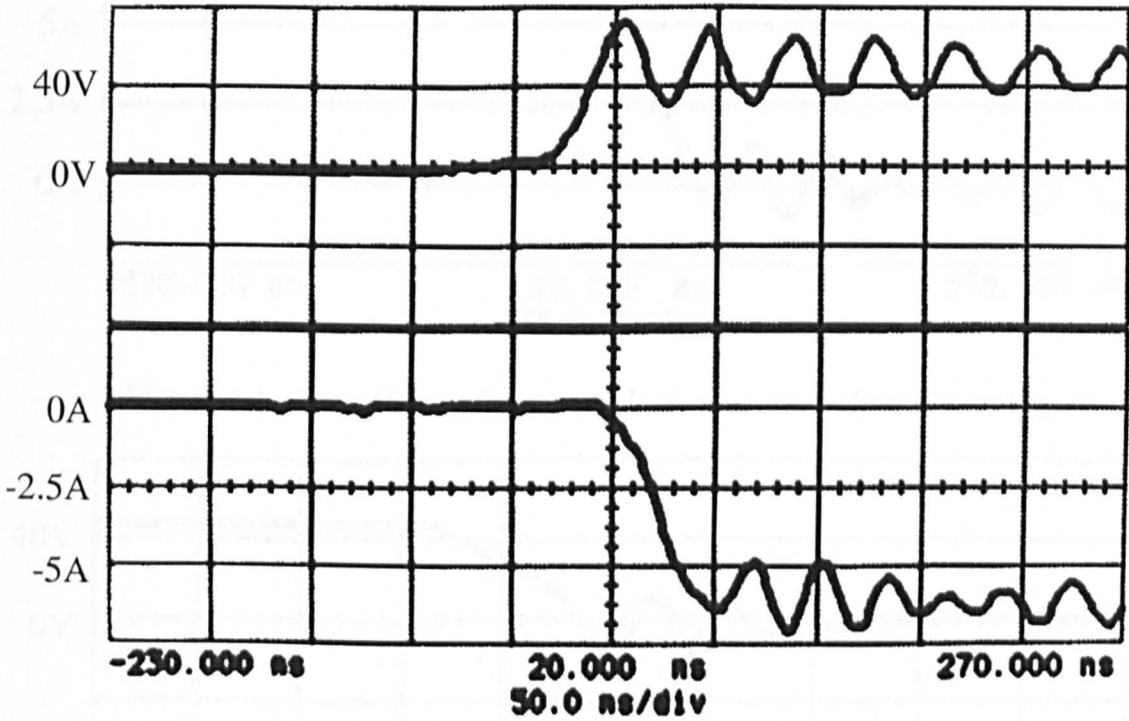


Figure 4.3 – V_{OUT} (Upper trace) and I_1 (Lower trace) for Q2 turning off

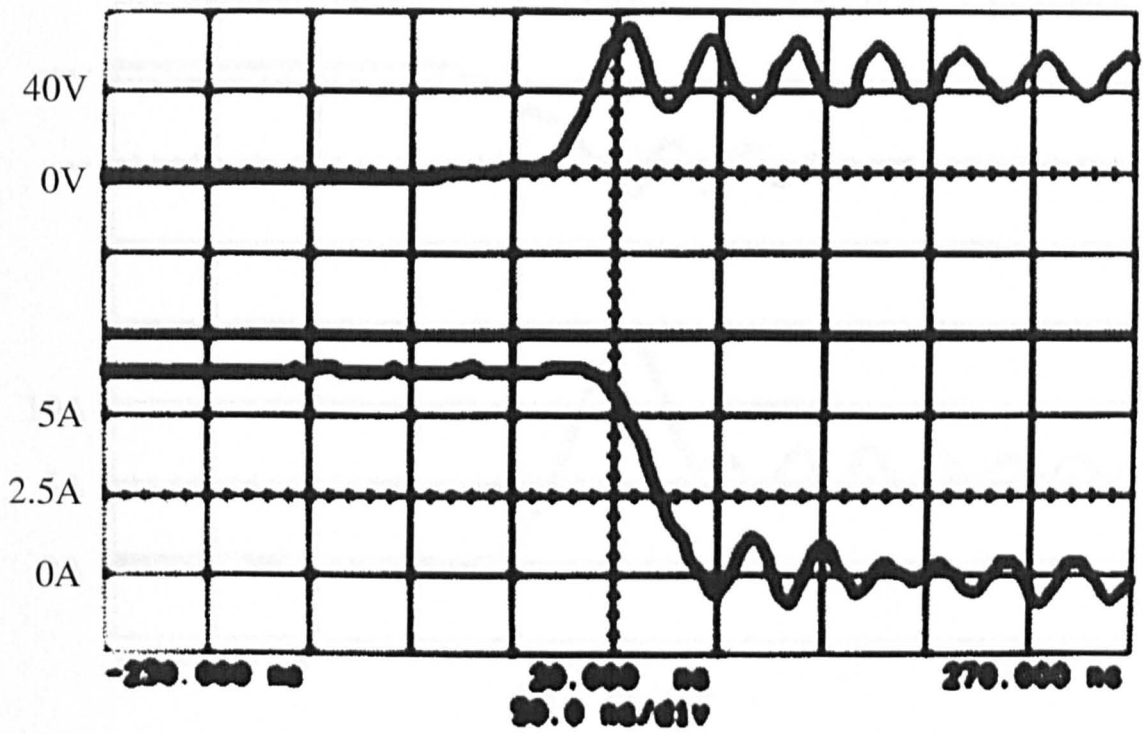


Figure 4.4 – V_{OUT} (Upper trace) and I_2 (Lower trace) for Q2 turning off

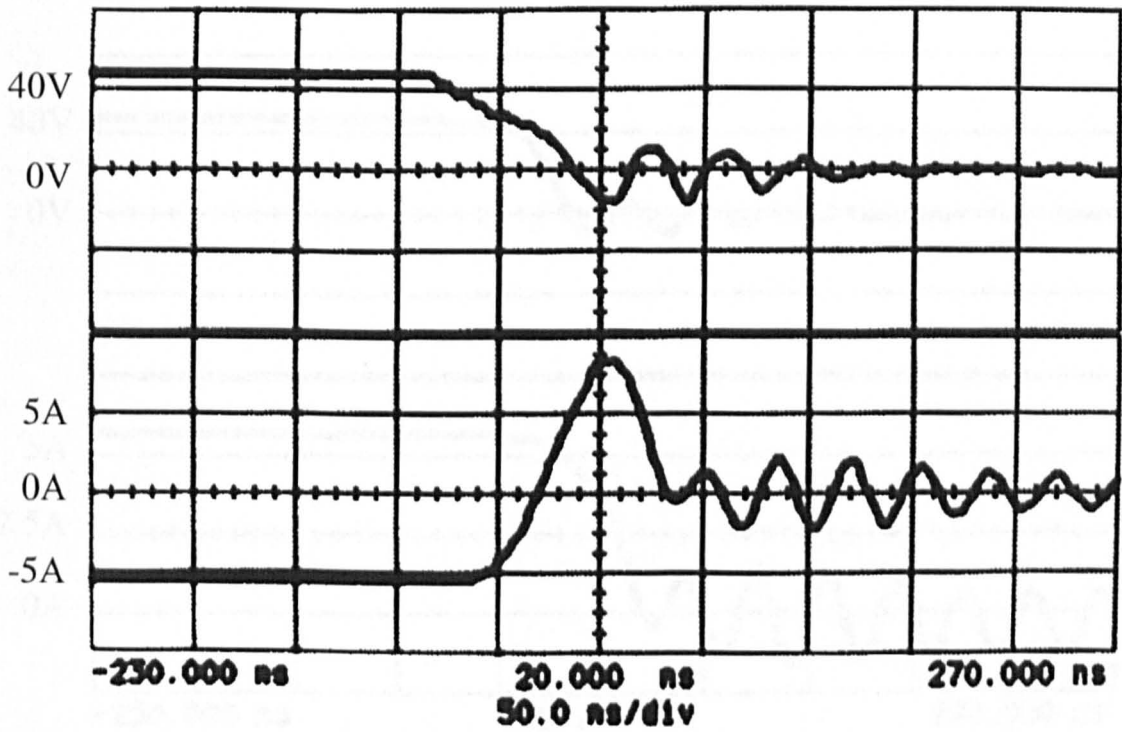


Figure 4.5 – V_{OUT} (Upper trace) and I_1 (Lower trace) for Q2 turning on

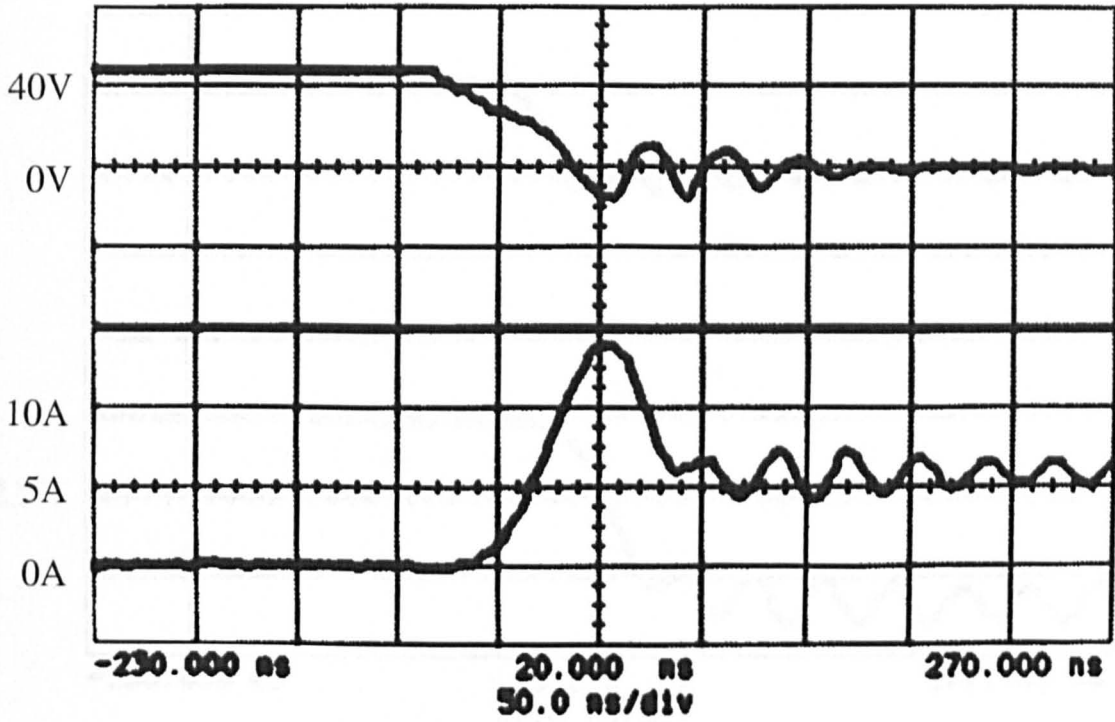


Figure 4.6 – V_{OUT} (Upper trace) and I_2 (Lower trace) for Q2 turning on

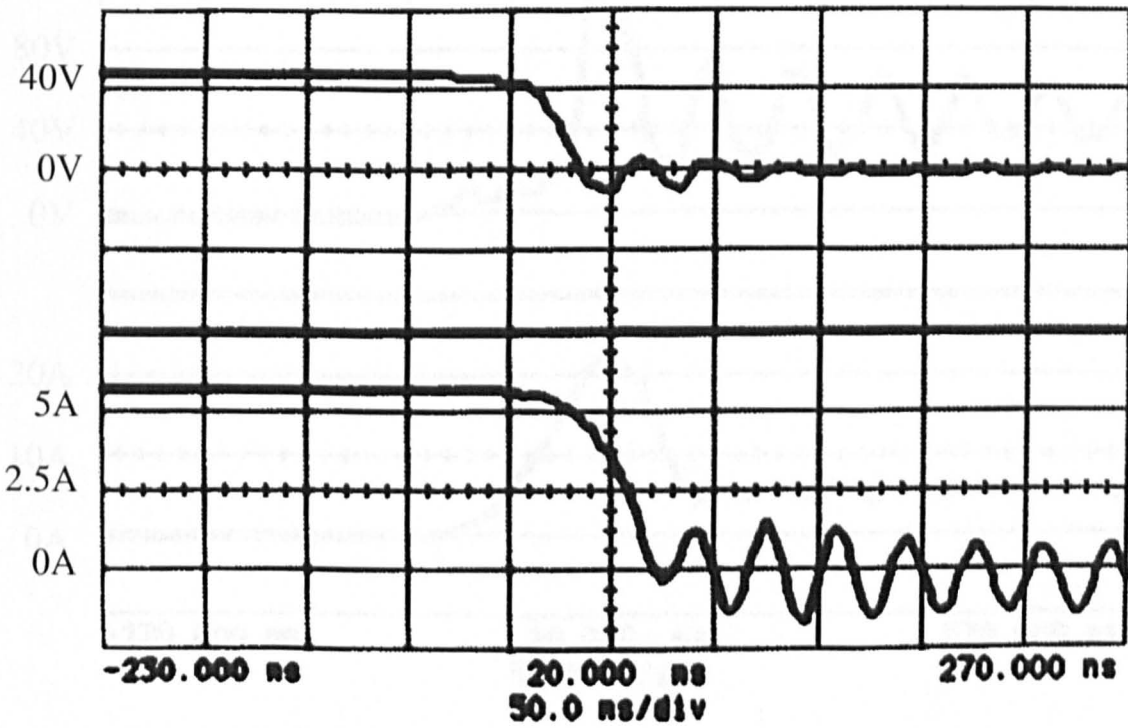


Figure 4.7 – V_{OUT} (Upper trace) and I_1 (Lower trace) for Q1 turning off

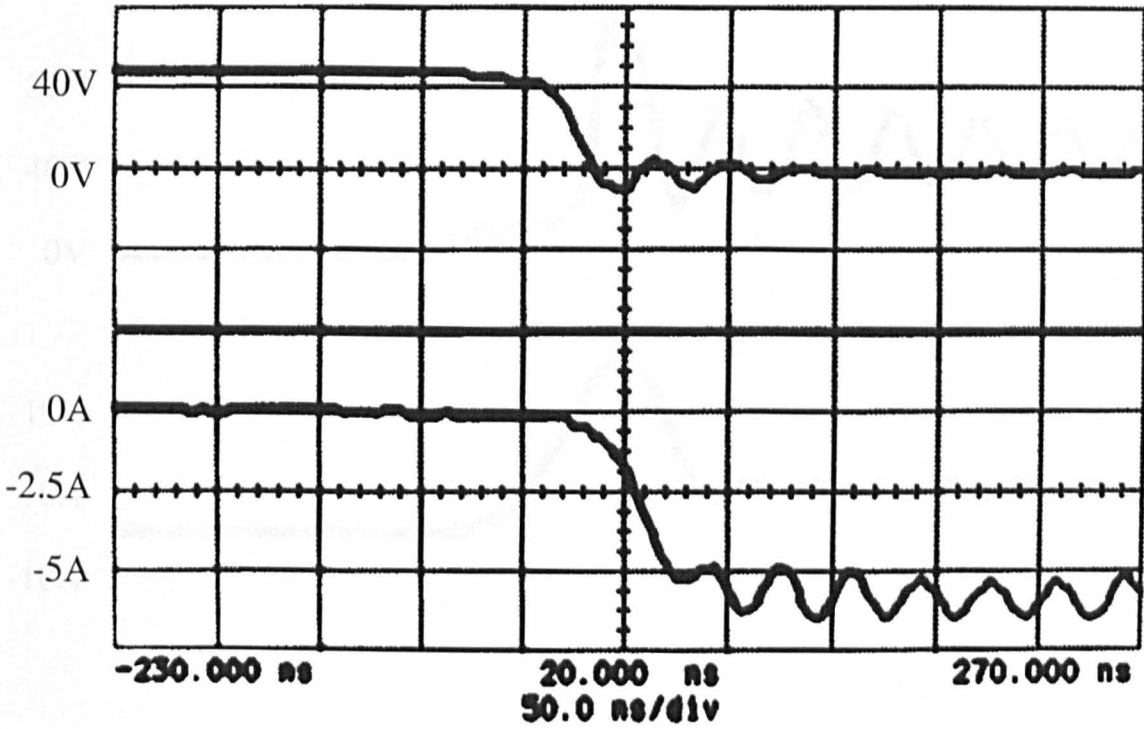


Figure 4.8 – V_{OUT} (Upper trace) and I_2 (Lower trace) for Q1 turning off

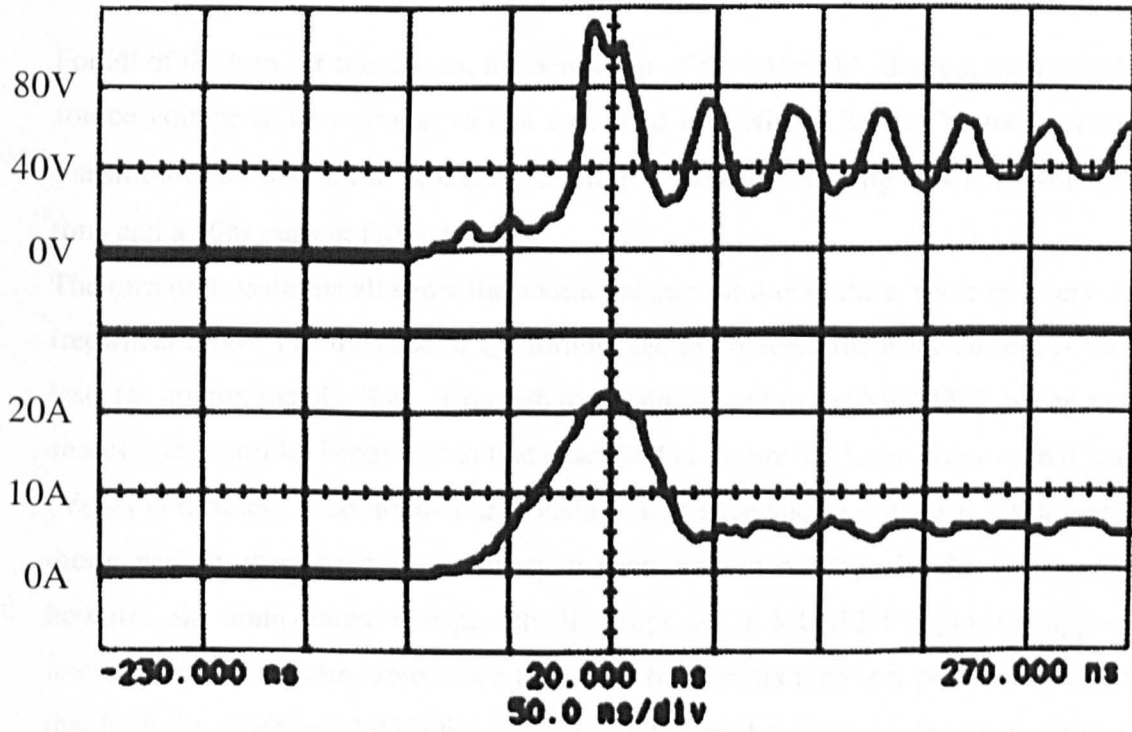


Figure 4.9 – V_{OUT} (Upper trace) and I_1 (Lower trace) for Q1 turning on

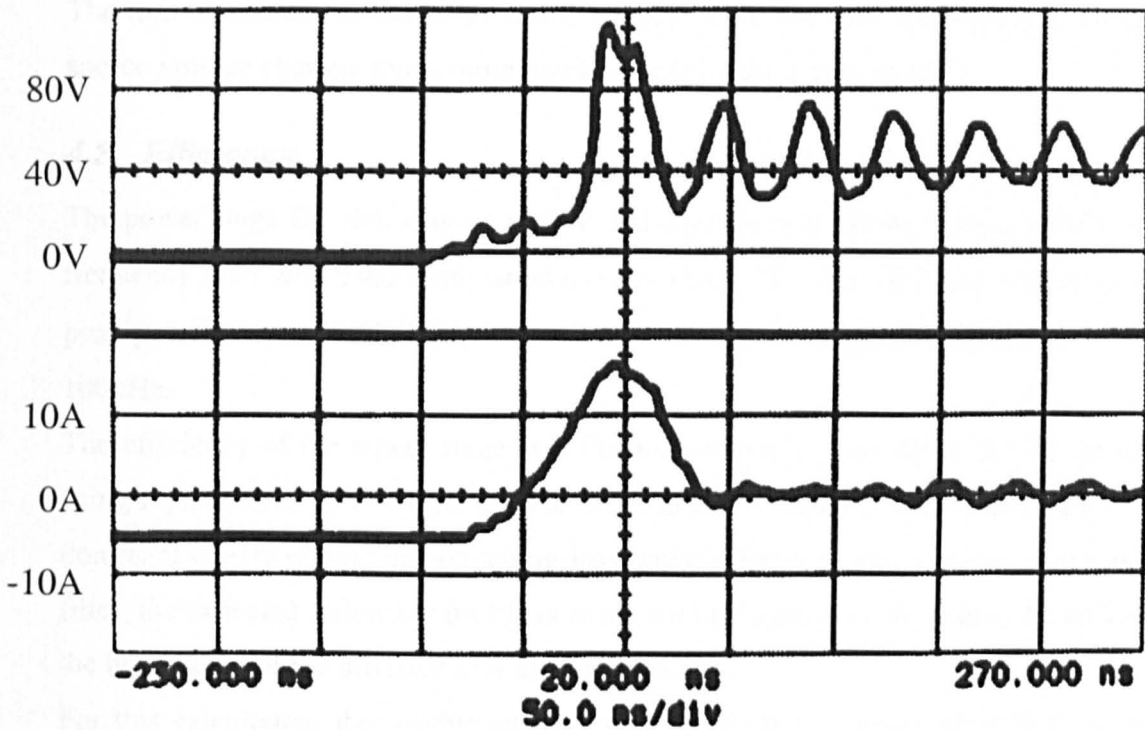


Figure 4.10 – V_{OUT} (Upper trace) and I_2 (Lower trace) for Q1 turning on

For all of the turn off transitions, the behaviour of the MOSFET drain current and drain-source voltage is very similar to that described in section 2.3.3.1. The total switch off transition time, with a 2Ω gate drive resistor is 75ns, comprising of a 25ns voltage rise time and a 50ns current fall time.

The turn on transitions all show the additional current due to the reverse recovery of the freewheel diode. For the case of Q2 turning on, the reverse recovery current is 9A and lasts for approximately 50ns. Although the drain current in the MOSFET during turn on shows a very similar behaviour to that described in Figure 2.15, the drain-source voltage (V_{OUT}) is different. The drain-source voltage was expected to remain at +Vdc until the diode had reached its peak recovery current and then drop. In the measurements however, the drain-source voltage actually drops as the MOSFET begins to support the load current and reaches zero when the diode finishes its recovery period. This implies that both the diode and MOSFET will suffer additional loss due to the reverse recovery period. Therefore, a simple way to model the turn on losses is to assume that the waveforms are the same as for turn off except that the transition takes an additional time, t_{rr} , to take place.

The turn on characteristics of Q1 and Q2 appear to be slightly different since the drain-source voltage changes much more quickly for Q1 than it does for Q2.

4.3 Efficiency

The power stage DC link was set to 60V and a fourth order Butterworth, 20kHz corner frequency filter with a 4 Ω termination used as a load. This 60V DC link will allow for a peak power output of 450W into the 4 Ω load. The power stage was driven by PWM at 100kHz.

The efficiency of the power stage as a function of modulation depth can be estimated using Equations (2.7), (2.8) and (2.9) as developed in Chapter 2. If it is assumed that the dominant causes of loss are switching loss, conduction loss and I^2R loss in the power filter, the expected efficiency profile is as shown in Figure 4.11(a). Figure 4.11(b) gives the breakdown of the different loss mechanisms.

For this calculation, the conduction loss was based on the power MOSFETs with an $R_{DS(on)}$ of 70m Ω each, the switching transition time, t_c , taken as 75ns and the reverse recovery time, t_{rr} , taken as 50ns. The inductors in power filter had a measured DC resistance of 100m Ω and since the polypropylene capacitors used have very low series resistance, the loss in the inductors was taken as the dominant filter loss.

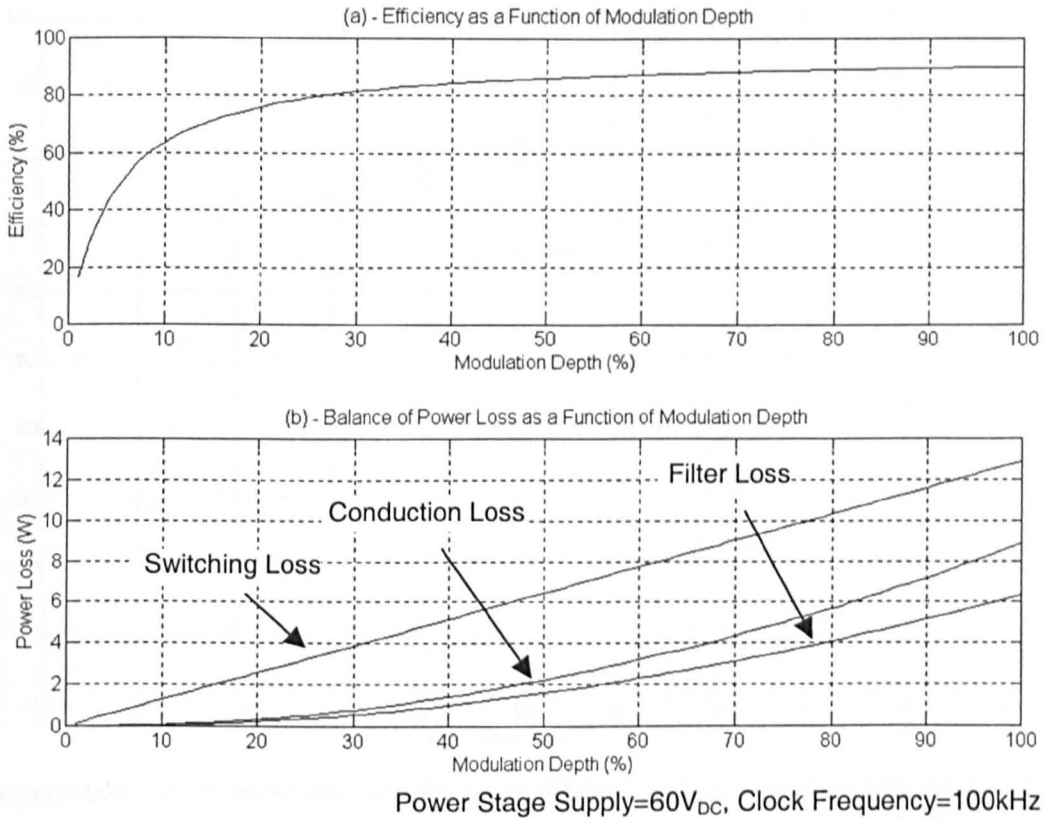
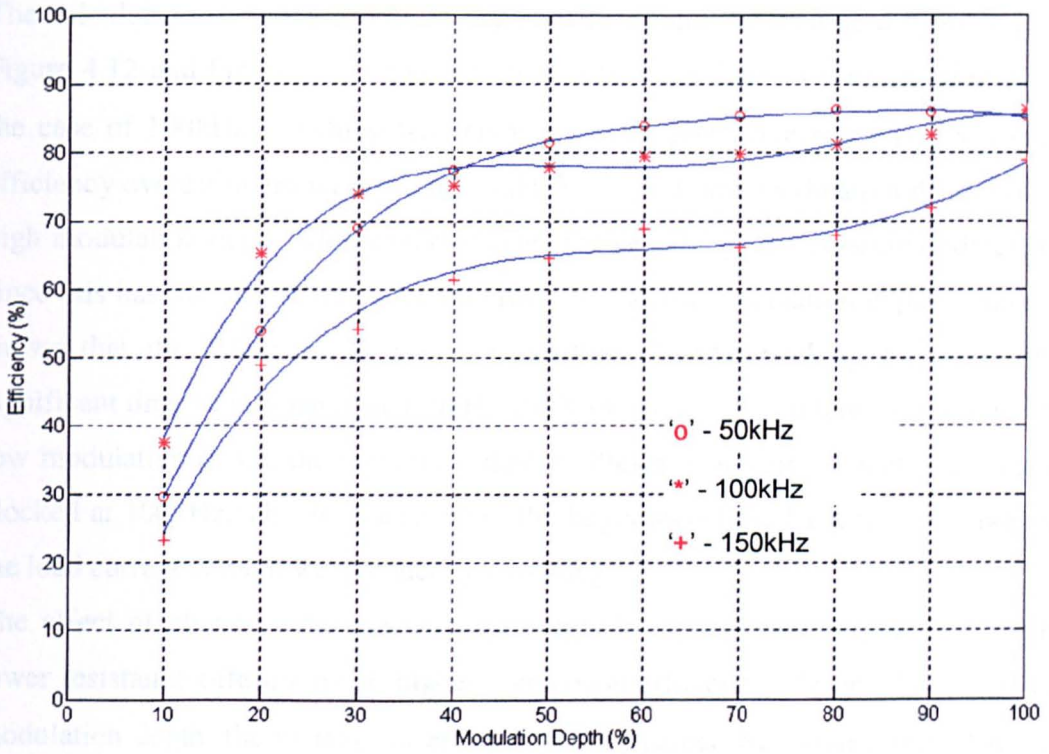


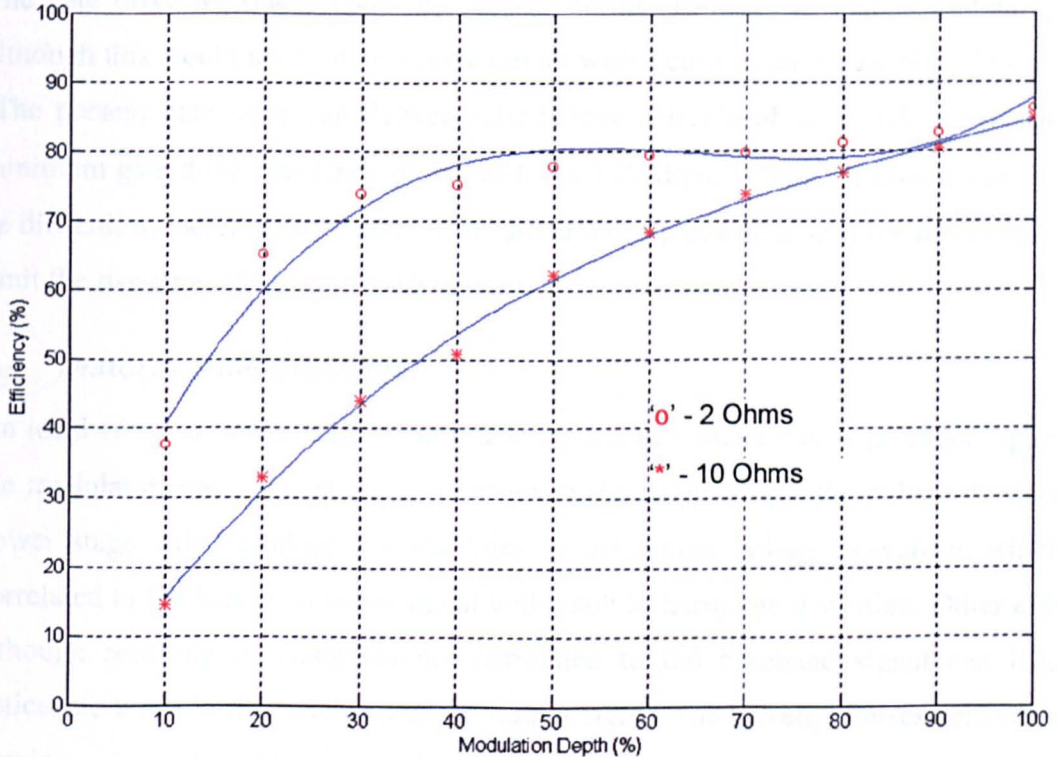
Figure 4.11 - Calculated efficiency profile and balance of loss for prototype power stage

The calculations suggest that the switching loss component dominates the loss in the overall amplifier, which is to be expected from the high switching frequencies used. In practice, the loss is likely to be higher than that calculated using Equations (2.7), (2.8) and (2.9) since the load current also consists of switching frequency components. At low modulation depths, the loss due to switching frequency components will have a relatively higher impact on the efficiency since the output power is lower. Therefore, in practice, the efficiency curve will show a more gradual increase in efficiency with modulation depth. The actual efficiency of the power stage was measured using a high bandwidth power analyser (See appendix E for specifications) to measure the input power to the DC link and the output power after the filter. The operating efficiency was measured for three different switching frequencies, 50kHz, 100kHz and 150kHz, in order to examine the relative impact of switching frequency on the overall efficiency, Figure 4.12. One further efficiency profile was taken at 100kHz switching frequency with the gate drive resistors increased from 2Ω to 10Ω to examine the effect of the gate drive impedance on loss, Figure 4.13. In the two figures, the solid blue line again represents a polynomial fit to the data.



DC supply=60V, Fourth order filter with 4Ω resistive load, 100Hz fundamental frequency, 2Ω gate drive resistors

Figure 4.12 - Measured efficiency profiles at different switching frequencies



DC supply=60V, Fourth order filter with 4Ω resistive load, 100Hz fundamental frequency, 100kHz switching frequency

Figure 4.13 - Efficiency at 100kHz switching frequency for different gate drive resistors

The calculated efficiency profile of Figure 4.11(a) and the measured profiles given in Figure 4.12 and Figure 4.13 show a very similar behaviour with modulation depth. In the case of 100kHz switching frequency, with 2Ω gate drive resistors, the calculated efficiency overestimates the measured value by 20% at low modulation depth and 5% at high modulation depth. This would suggest the switching loss is being underestimated since this has the largest influence on efficiency at low modulation depths. Figure 4.12 shows that the efficiency is a strong function of the switching frequency with a significant drop in efficiency at 150kHz clock frequency. It is interesting to note that at low modulation depth, the system clocked at 50kHz is actually less efficient than that clocked at 100kHz. This is as a result of the larger switching frequency components in the load current at the lower frequency switching.

The effect of changing the gate drive resistors is evident from Figure 4.13 with the lower resistance offering much higher conversion efficiency. Over a large part of the modulation depth, the increase in efficiency to be gained by moving from 10Ω to 2Ω resistance is greater than 20%. At higher switching frequencies, the difference is likely to be even greater since the switching loss will dominate the efficiency profile.

The gate drive resistance could be reduced further in order to reduce switching loss although this would necessitate a drive circuit with a current drive capability beyond 6A (The present gate drive can deliver pulsed drive currents of up to 6A which gives a minimum gate drive resistance of 2Ω with the 12V drive voltage). Furthermore, it may be difficult to increase the speed much further since parasitic gate drive inductance will limit the rise-time of the gate drive current.

4.4 Distortion Mechanisms

An ideal Class-D power stage would have an output voltage that is an exact replica of the modulator input, except for an increase in the amplitude of the pulses. A practical power stage will introduce non-idealities to the output voltage waveform which, if correlated to the baseband audio signal will result in harmonic distortion. Other effects, although resulting in distortion not correlated to the baseband signal can lead to noticeable tones in the baseband of the output signal which compromises performance. Previous work by Erickson and Middlebrook, [4.1], has discussed the different distortion mechanisms in an H-Bridge output stage. In single and three-phase motor drive applications, it has been shown [4.2,4.3,4.4,4.5] that DC link ripple and the use of dead-time cause significant harmonic distortion in the load current waveform. In

studying a half bridge output stage, Attwood [4.6] highlights seven effects through which distortion of the baseband audio signal can occur. These are as follows: -

1. Poor tracking between upper and lower output device switching times, both at low analogue outputs and over the whole dynamic range, causing asymmetric errors in the pulse widths.
2. Pulse amplitude errors dependent on output load power, particularly noticeable during the transition between negative and positive half-cycles.
3. Unwanted RF ripple appearing in the PWM comparator section, causing incorrect timing in the pulse edges.
4. Layout and decoupling problems giving rise to common impedance paths, and overshoots during switching transitions.
5. Lost pulses near extremes of modulation.
6. Use of dominant-pole compensation does not fully realise the performance capability of PWM amplifiers.
7. Power supply ripple.

Of the seven effects described above, for an open-loop modulator, the dominant factors affecting linearity are #2 and #7. The use of identical devices can reduce the impact of #1. New control techniques [4.7] have alleviated mechanisms #3 and #6 whilst careful circuit design and layout can minimise #5.

In a mains supplied amplifier, typically the DC link supply would be derived using a simple mains transformer, rectifier and smoothing capacitor arrangement. If this were the case, then components at twice the mains frequency may appear directly on the output voltage waveform, and result in an audible 100Hz tone at the speaker. Although this 100Hz tone is uncorrelated to the signal frequency, its presence at even modest levels can cause annoyance to the listener. In high power systems, it is more likely that a switched-mode power supply (SMPS) would be used due to size and cost savings. A typical SMPS is likely to switch at ultrasonic frequencies and as such, the DC link ripple will be inaudible. It is important, however, to lock the SMPS switching frequency to a division of the output stage switching frequency to avoid 'beat' frequencies appearing in the audio output. In high power car audio systems, the only choice is to use a SMPS to boost the voltage since the primary voltage source is at 12V.

The pulse amplitude errors highlighted in #2 are caused by the combination of a number of different effects.

- When the freewheel diodes conduct, they have a voltage drop of 1-2V which is significantly different from the voltage drop across the power MOSFET. This effect will be minimal since the synchronous rectification operation of the power MOSFET ensures that the load current is being support by the MOSFET for greater than 95% of the time.
- The power MOSFETs have a conduction voltage drop determined by the load current and on resistance ($R_{DS(on)}$). Thus, the output voltage pulse height will be modulated by the load current, and since the load current consists predominantly of the baseband audio signal, harmonic distortion will occur. In addition, the $R_{DS(on)}$ of the power device increases with junction temperature and therefore, at high output levels, the modulation of the pulse height will be more severe.
- Even if a SMPS is used to power the output stage, the DC link will still not be a perfect voltage source. The DC link will have a dynamic behaviour governed by the transient response of the SMPS and impedance of the connection wires between supply and output stage. The end result of the non-ideal DC link is that the voltage supplied to the output stage will be a function of the load current drawn and therefore the DC link voltage will be modulated by the baseband audio signal. This will only cause a problem at the lower end of the audio spectrum where large transient peaks of power are often found.
- In practice, the single quadrant nature of the power supply necessitates a large decoupling capacitor across the H-Bridge to ensure the DC link ripple is not excessive.

It is common practice to delay the turn-on of all the active switches such that no two devices in the same 'leg' are on simultaneously. If two devices in the same leg were to conduct simultaneously, a shoot-through current would destroy both devices. This delay results in an instant, twice per switching cycle, when none of the active devices are conducting. This period is commonly referred to as dead time and during this time, the load current is supported by the freewheel diodes. The dead-time period must at a

minimum be equal to the switching time of the power devices ($\sim 50\text{ns}$ for power MOSFETs) but is often made larger to ensure shoot-through cannot occur.

In addition to the pulse amplitude distorting effects described by Attwood, the use of dead time can result in pulse-width errors. If any of the distortion mechanisms are correlated to the baseband signal, harmonic distortion terms will appear in the output voltage.

4.4.1 Dead Time

The impact of the use of dead time for PWM and PDM driven power stages will differ quite markedly. The behaviour under PWM control is relatively predictable since during a switching cycle there will always be a high to low and a low to high transition of the output voltage. The dead time behaviour can therefore be analysed by averaging the effect of the error over a single switching cycle.

When the power stage is driven by a PDM modulator, the output voltage can remain in the same positive or negative state for more than a single switching period. This makes the behaviour under PDM more difficult to predict since it cannot be averaged over a single switching cycle.

4.4.1.1 PWM Driven

With reference to Figure 2.9 (Repeated in Figure 4.14 for clarity), for the full bridge converter, when the load current, I_L , is positive during the dead time, diodes D2 and D3 will conduct.

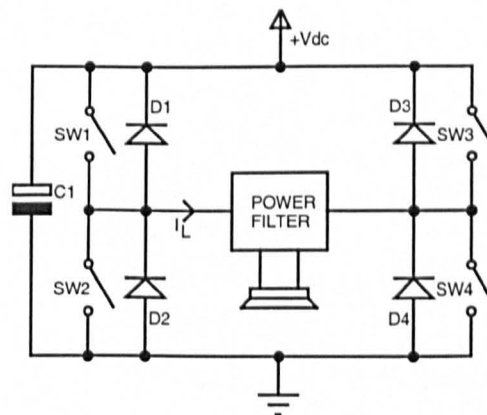


Figure 4.14 – Full Bridge power stage

Figure 4.15 shows the measured effect for a positive load current and a PWM driven power stage. Comparison of the duty cycle of the modulator output and power stage

output demonstrates that, due to the uncontrolled current during the dead-time, the power stage output duty cycle and hence the average output voltage, is lower than demanded. For a negative load current, the effect is similar except that diodes D1 and D4 conduct to give an output duty cycle that is higher than demanded. Figure 4.16 shows the measured modulator duty cycle and power stage output duty cycle for a negative load current. The duty cycle error for both Figure 4.15 and Figure 4.16 is equal to the dead time normalised to the switching period length. For example, a $4\mu\text{s}$ dead time with $25\mu\text{s}$ period gives a duty cycle error of 16%.

For the cases presented in Figure 4.15 and Figure 4.16, the load current is continuous. When the load current becomes discontinuous, it becomes possible that a zero current period can exist during the dead time. Figure 4.17 illustrates operation when the load current approaches zero. If the load current falls to zero during the dead time period, the free-wheel diodes will turn-off and the output voltage will momentarily float since no power devices are in conduction; it will then oscillate around zero volts.

As the load current passes through zero, the length of this floating period changes and the effective duty cycle error decreases. Although the behaviour is oscillatory, the reduction in duty cycle error is approximately proportional to the level of the current, Figure 4.18.

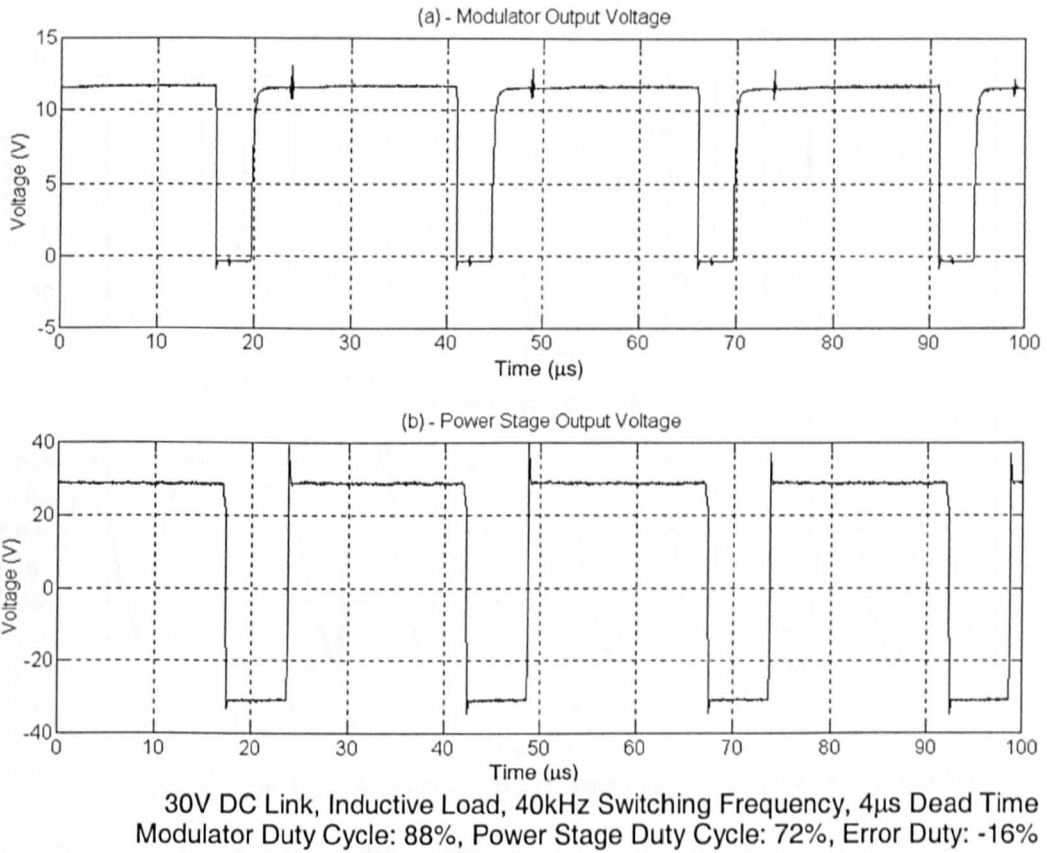


Figure 4.15 - Effect of dead time for a positive inductive load current

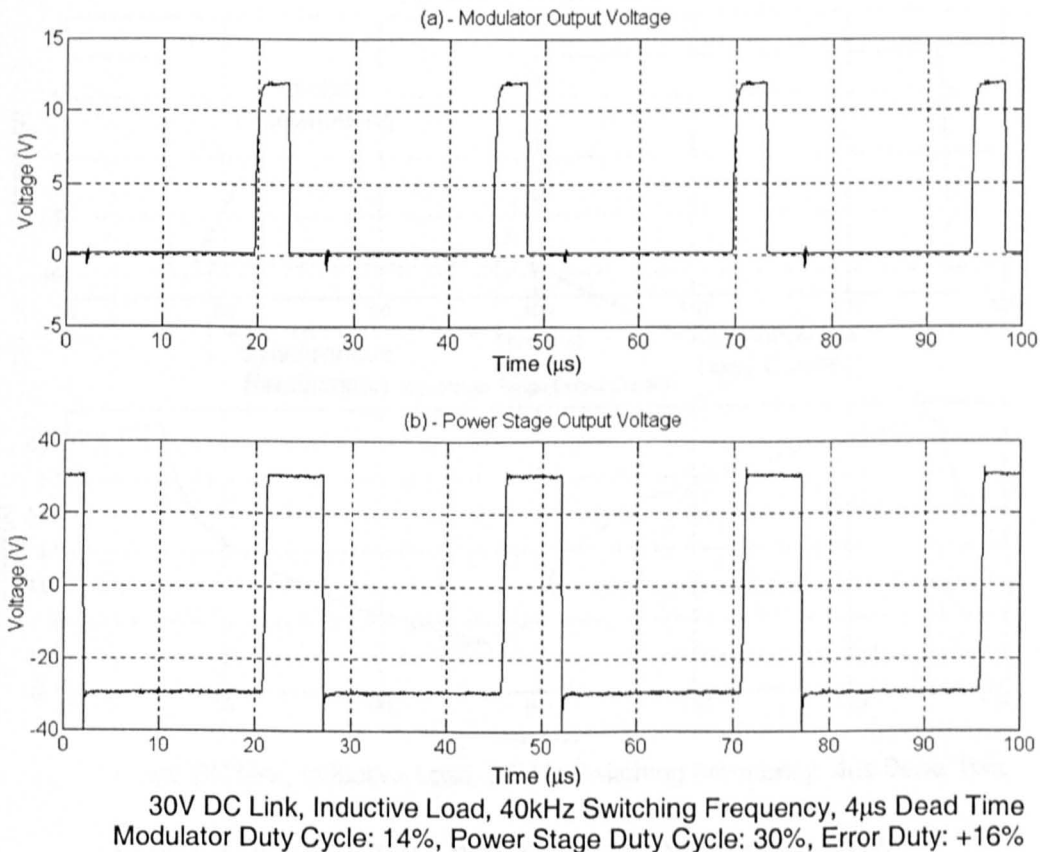


Figure 4.16 - Effect of dead time for a negative inductive load current

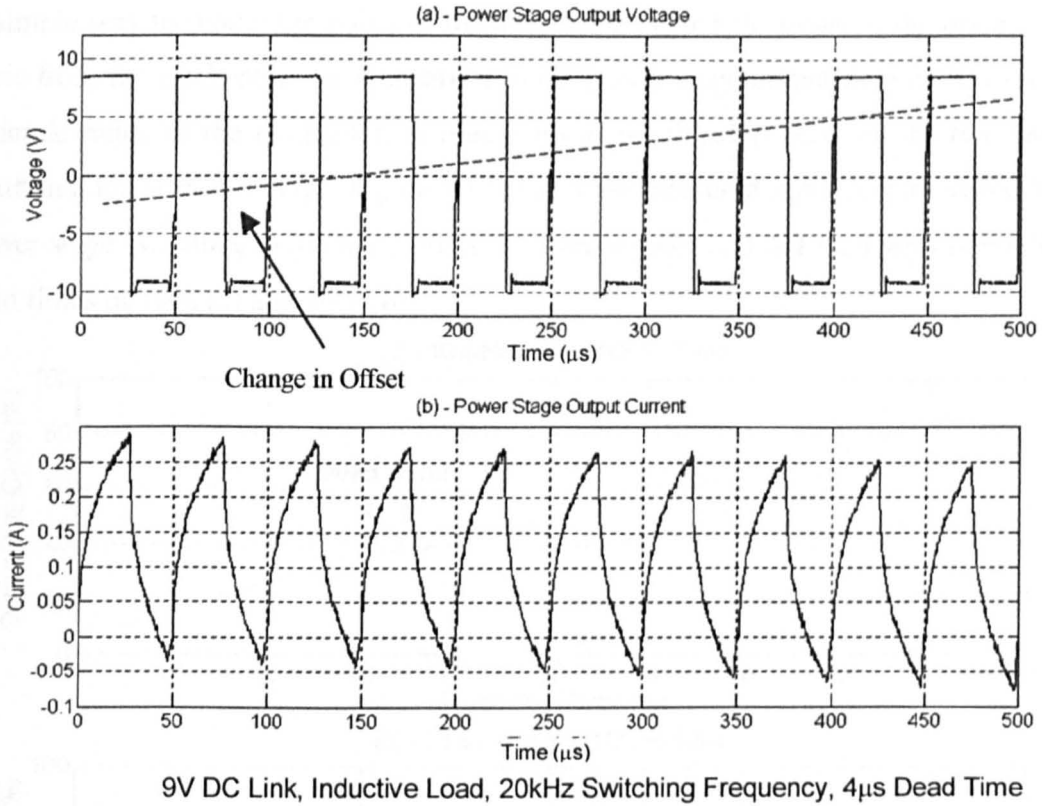


Figure 4.17 - Onset of discontinuous current during the dead time

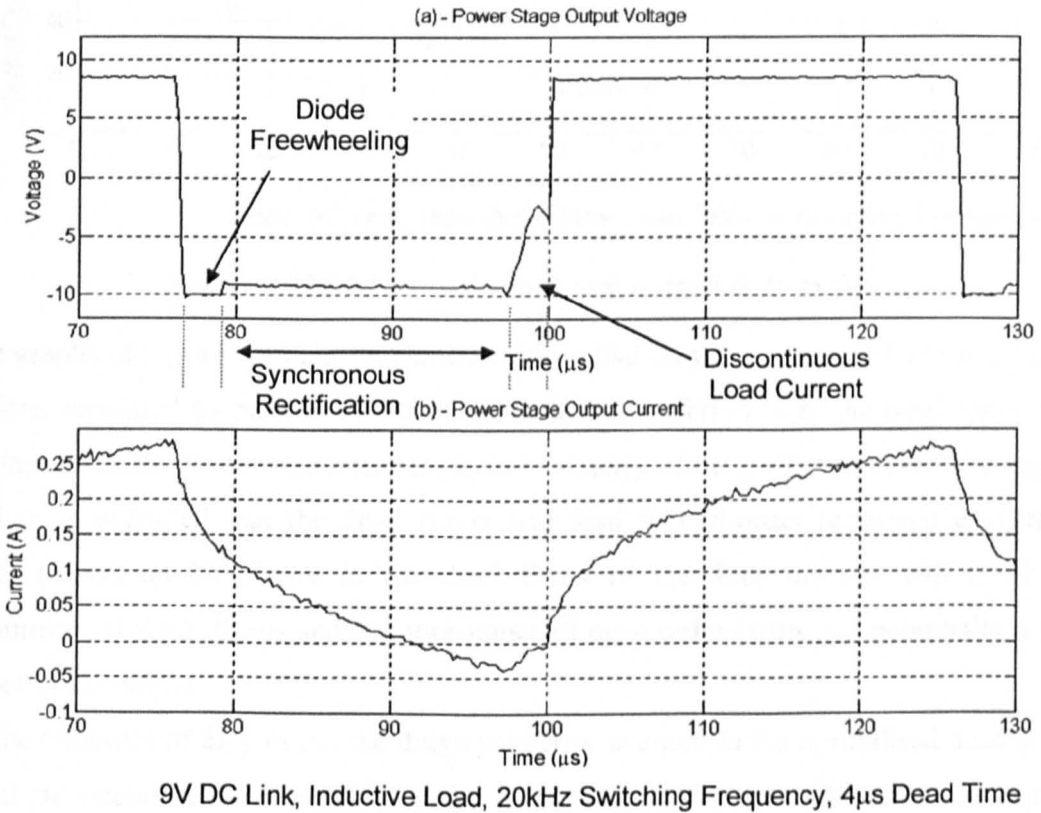


Figure 4.18 – Behaviour under discontinuous load current

A simple way to model the effect of the duty cycle error is to measure the driven duty cycle from the modulator and compare it to the power stage output duty cycle over the dynamic range of the modulator. A purely linear relationship between the two would result in a linear power stage. Figure 4.19 shows the measured input/output profile for a power stage switching at 100kHz into a third order filter and 4Ω load with normalised dead times of 10% (a) and 20% (b).

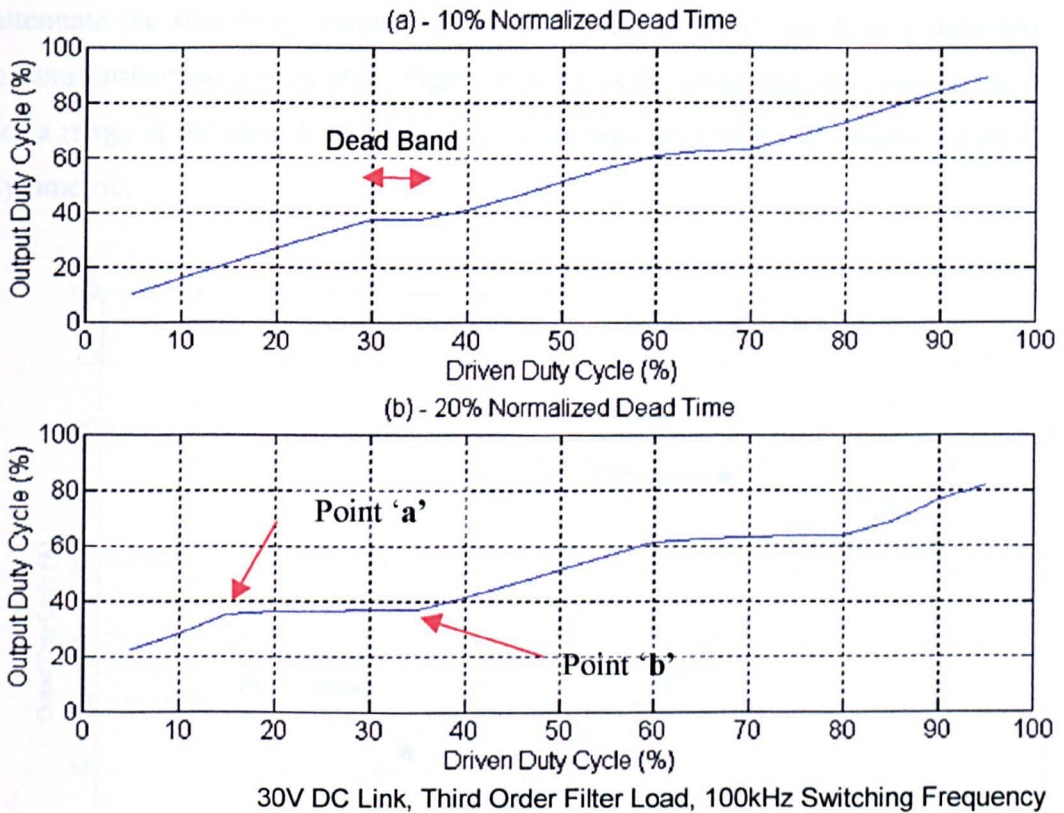
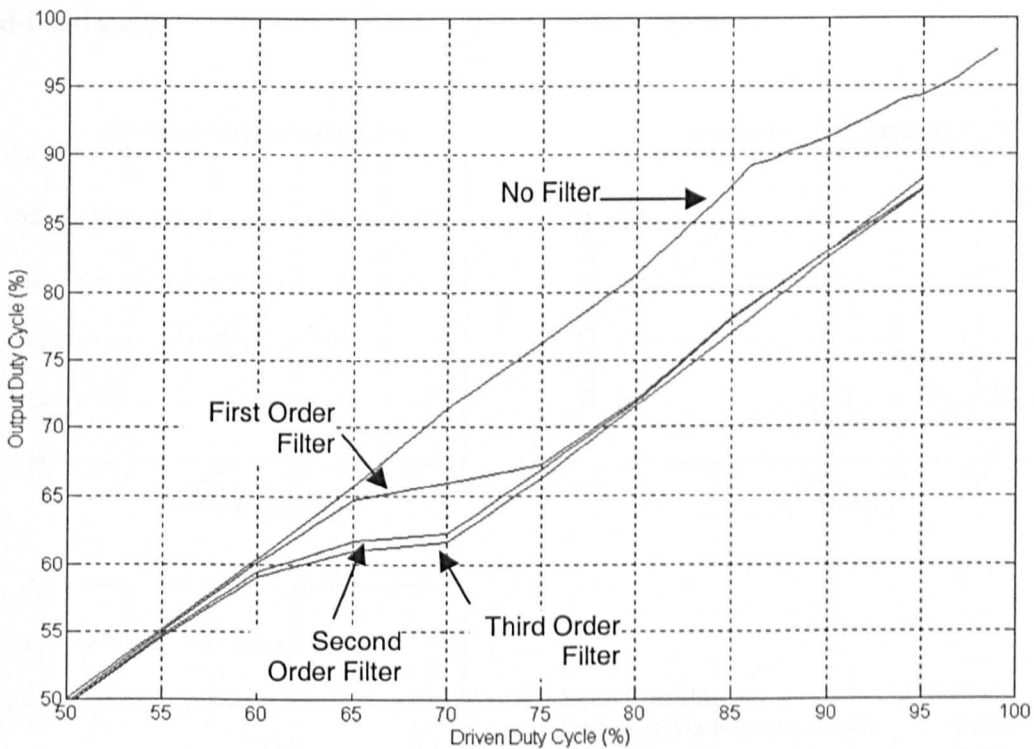


Figure 4.19 - Measured input and output duty cycles

The graphs of Figure 4.19 have a similar form in that they are comprised of three linear regions separated by periods of constant output duty referred to as the dead band. The symmetry of the power converter results in symmetry of the profile around 50% and as such it is expected that the dead bands will lead to odd-order harmonic distortion. Furthermore, an imbalance in the dead times of the four devices will result in asymmetrical dead bands and the appearance of even order terms and potentially a DC offset in the output.

At the extremes of duty cycle, the duty cycle error is equal to the normalised dead time. Point 'b' occurs at the same duty cycles for both the 10% and 20% cases and can be shown to be a function of the load impedance. The dead-band length is equal to the normalised duty cycle and point 'a' occurs at the end of this. Since the level of the

switching frequency ripple current is dependent on the load impedance presented to the power stage, different order filters will result in the dead band occurring at different levels. A high order filter will present a large impedance at the switching frequency in order that it will attenuate the high frequency components of the PWM spectra and reduce loss. The consequence of this is that the switching frequency ripple current is small and therefore point 'b' will be close to 50% duty. A lower order filter will not attenuate the switching components as effectively and will result in a dead band that occurs further away from 50%. Figure 4.20 gives the measured input/output duty cycles for a range of different loads. For duty cycles less than 50%, the results are rotationally symmetric.



30V DC Link, 11.3 Ω Termination, 100kHz Switching Frequency, 10% dead time

Figure 4.20 - Dead band levels for different loads

With no filter and a purely resistive 11.3 Ω load, Figure 4.20 shows that the input/output duty cycle relationship is relatively linear. When filters are introduced between the power stage and the resistive load, the dead band becomes evident and with increasing filter order, the dead band moves closer to 50% duty cycle as expected.

A relatively simple way to model the harmonic distortion introduced by dead time is to treat the dead band as being flat as illustrated in Figure 4.21(a). The harmonic levels

produced by the dead time can then be quantified by considering the impact of the dead band on a sinewave driven duty cycle. Since there is a direct relationship between duty cycle and fundamental output voltage, the duty cycle error for the sinewave can be used to describe the output voltage error over one fundamental cycle. This voltage error is harmonically related to the fundamental and Fourier analysis of its voltage profile can then be used to predict the corresponding harmonic levels.

Figure 4.21 illustrates the effect of the dead time on a typical sinewave driven modulator. Figure 4.21(a) shows the input/output duty cycle transfer function of the power stage. Figure 4.21(b) shows the input duty cycle demand from the modulator and Figure 4.21(c) gives the resulting duty cycle output from the power stage. In Figure 4.21(a), the value 'k' is defined as the level above (or below) the 50% level at which the dead-band starts.

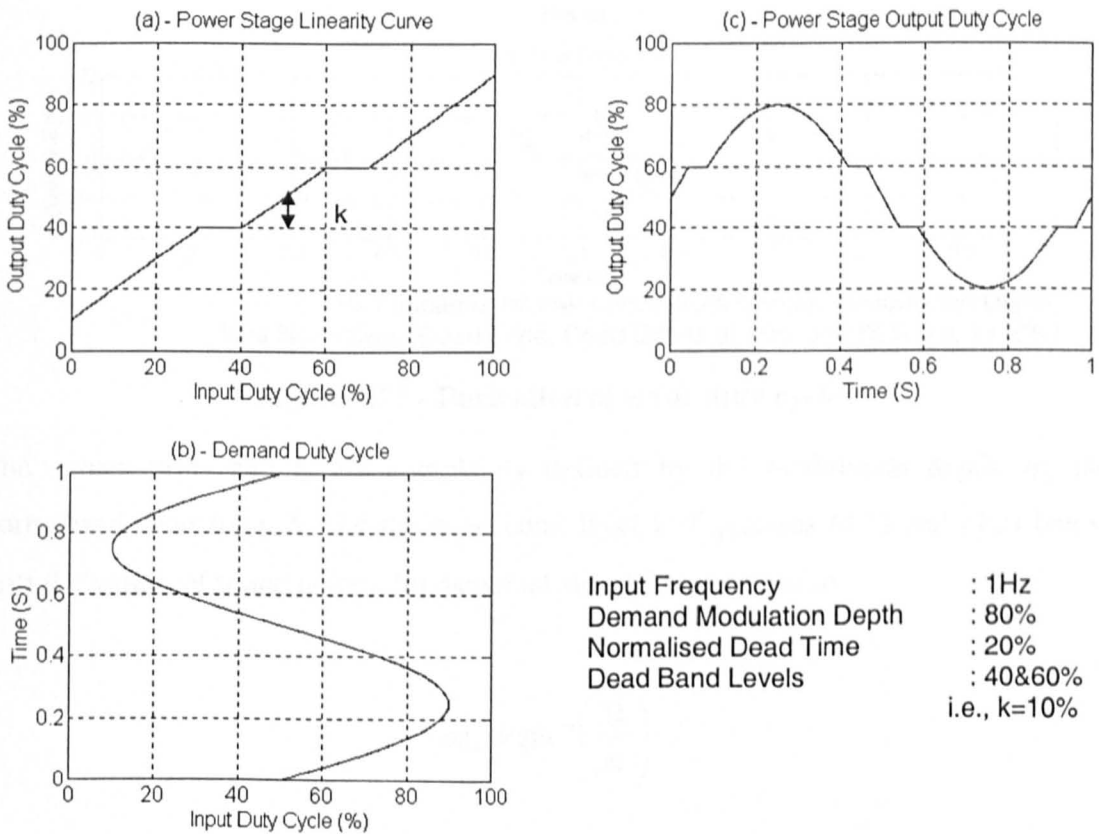


Figure 4.21 - Effect of non-linearity on sinewave input

The harmonic distortion due to the non-linearity will be the harmonic content of the difference between the demand duty cycle and the output duty cycle. The fundamental

level will also be affected by the non-linearity but it is easier to quantify this once the harmonic levels have been defined. The method is to consider a duty cycle error defined as the output duty cycle subtracted from the demand duty cycle, Figure 4.22.

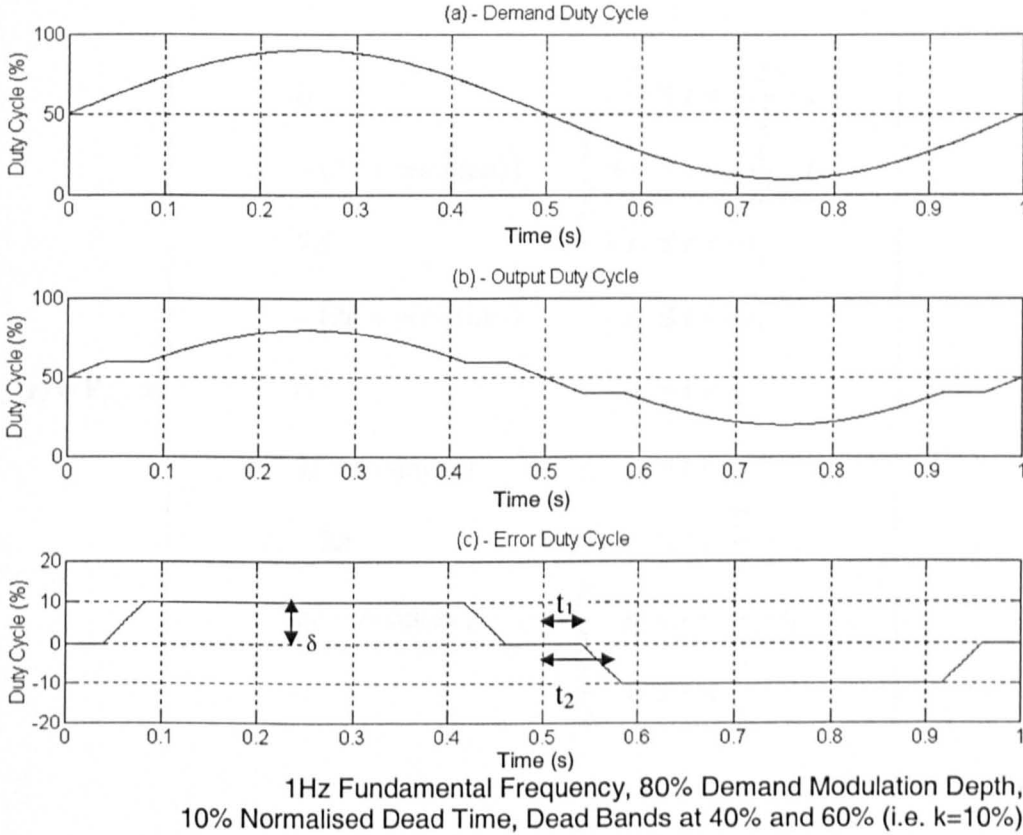


Figure 4.22 - Derivation of error duty cycle

The values of t_1 and t_2 are completely defined by the modulation depth, m , the normalised dead time, δ , and the dead band level k . Equations (4.1) and (4.2) below give the values of t_1 and t_2 for a fundamental signal frequency of ω .

$$\omega t_1 = \sin^{-1}\left(\frac{2k}{m}\right) \quad (4.1)$$

$$\omega t_2 = \sin^{-1}\left(\frac{2(k + \delta)}{m}\right) \quad (4.2)$$

If $\delta=0$, then $t_1=t_2$ and the power stage is perfectly linear. These definitions of t_1 and t_2 completely define the error duty cycle. The corresponding error output voltage is as shown in Equation (4.3).

$$V_{error}(t) = V_{DC} \times \left\{ \begin{array}{ll} 0 & -\frac{T}{2} \leq t < -\frac{T}{2} + t_1 \\ -(2k + m \sin(\omega t)) & -\frac{T}{2} + t_1 \leq t < -\frac{T}{2} + t_2 \\ 2\delta & -\frac{T}{2} + t_2 \leq t < -t_2 \\ -(2k + m \sin(\omega t)) & -t_2 \leq t < -t_1 \\ 0 & -t_1 \leq t < t_1 \\ 2k - m \sin(\omega t) & t_1 \leq t < t_2 \\ -2\delta & t_2 \leq t < \frac{T}{2} - t_2 \\ 2k - m \sin(\omega t) & \frac{T}{2} - t_2 \leq t < \frac{T}{2} - t_1 \\ 0 & \frac{T}{2} - t_1 \leq t < \frac{T}{2} \end{array} \right\} \quad (4.3)$$

With the error voltage now described over one fundamental cycle, simple Fourier analysis can be used to predict the harmonic distortion. The DC component of the signal is zero and since the function described by Equation (4.3) is odd, the error can be described as in Equation (4.4).

$$V_{error}(t) = \sum_{n=1}^{\infty} b_n \sin(n\omega_0 t) \quad (4.4)$$

Where,

$$b_n = \frac{2}{T} \int_{\frac{T}{2}}^{\frac{T}{2}} V_{error}(t) \times \sin(n\omega_0 t) dt \quad (4.5)$$

Solution of Equation (4.5) with V_{error} as defined in Equation (4.3) yields the harmonic levels as described in Equations (4.6) and (4.7). (A full worked solution can be found in appendix A)

$$b_n \Big|_{n > 1} = \frac{4V_{DC}(1 - \cos(n\pi))}{n\pi(n^2 - 1)} \times \left(\begin{aligned} &\frac{mn}{2}(\sin(n\omega t_1)\cos(\omega t_1) - \sin(n\omega t_2)\cos(\omega t_2)) \\ &\quad + \delta \cos(n\omega t_2) \\ &\quad + k(\cos(n\omega t_2) - \cos(n\omega t_1)) \end{aligned} \right) \quad (4.6)$$

And,

$$b_n \Big|_{n = 1} = \frac{4V_{DC}}{\pi} \left(\frac{m\omega}{2}(t_1 - t_2) + k(\cos(\omega t_1) - \cos(\omega t_2)) - \delta \cos(\omega t_1) \right) \quad (4.7)$$

The term for $n=1$ represents the loss in fundamental voltage as a result of dead time. Figure 4.23 shows a typical output current profile for an inductive load. The dead-band occurs when the current passes through zero. Thus, the component of the error voltage at the fundamental frequency will be phase displaced with respect to the fundamental driving voltage and the resulting fundamental level will be the vector addition of the two.

Since the dead band occurs when the load current passes through zero, the phase shift between the original fundamental and the error fundamental will be equal to the phase shift of the load impedance at the fundamental frequency.

In order to begin verification of the result above, the harmonic content of the output of the H-bridge was measured and the spectral content up to the 12th harmonic is shown in Figure 4.24 below. The predicted levels from Equation (4.6) are also plotted on the figure.

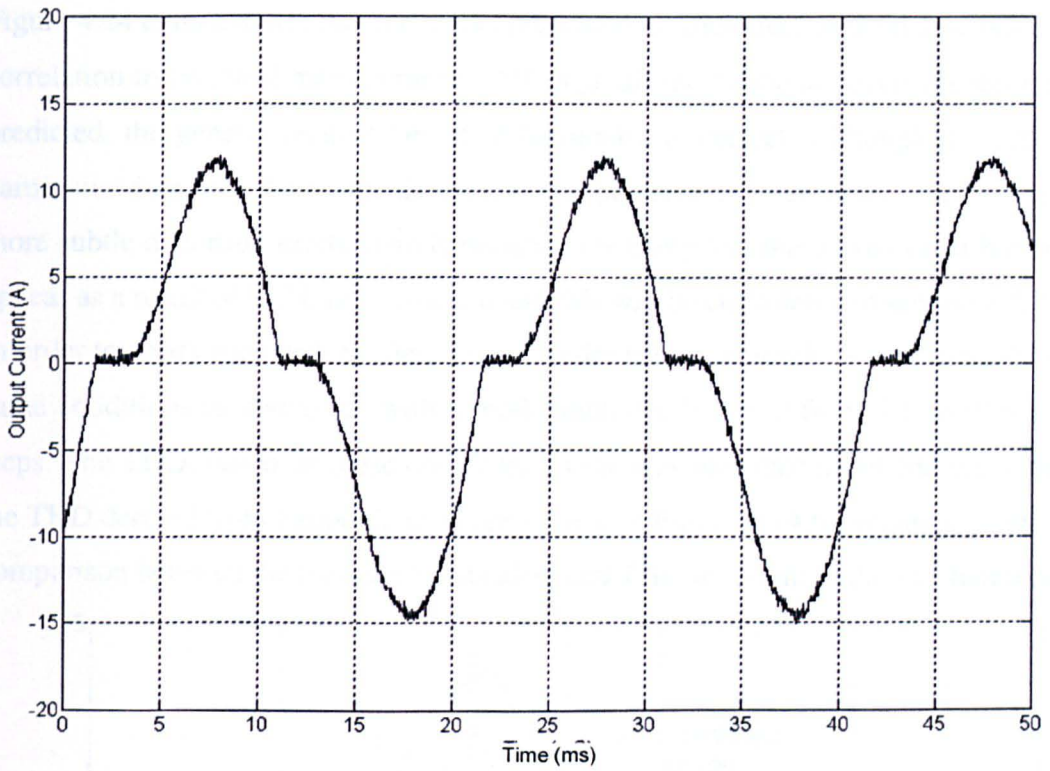
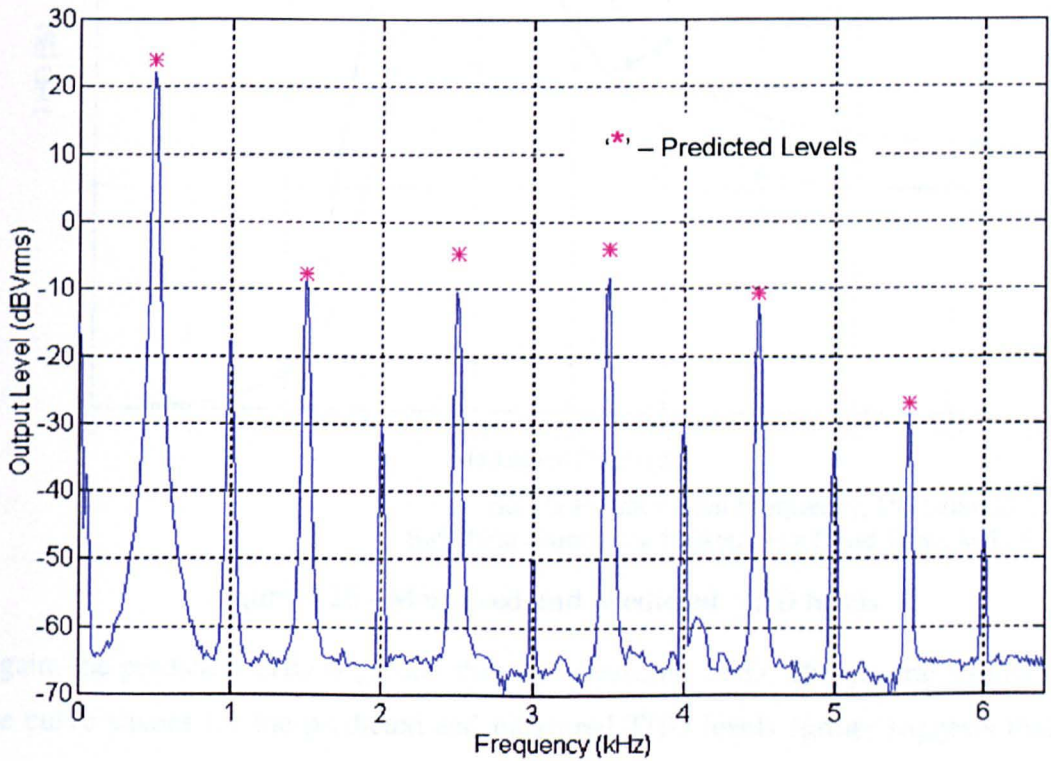


Figure 4.23 – Measured output fundamental current



500Hz Fundamental Frequency, 75% Modulation Depth, DC Link=30V,
Switching Frequency 100kHz, 1 μ s Dead Time, k=11%

Figure 4.24 – Measured and predicted spectral content up to 6kHz

Figure 4.24 demonstrates that the model presented for the effect of dead time has a good correlation to practical measurements. Although all the harmonic levels are not exactly predicted, the general relative height of harmonics is correct. Although the odd-order harmonics dominate the harmonic content, the presence of even order terms suggests a more subtle distortion mechanism is present. It is likely that these even order harmonics appear as a result of DC link fluctuation and this will be considered in section 4.4.2.

In order to verify the result further, the odd-order harmonic levels were recorded for the same conditions as above but with a modulation depth varied from 5% to 95% in 5% steps. The THD, based on these odd order levels, was then calculated and compared to the THD derived from harmonic levels predicted by Equation (4.6). Figure 4.25 shows a comparison between the measured and calculated THD levels up to the 11th harmonic.

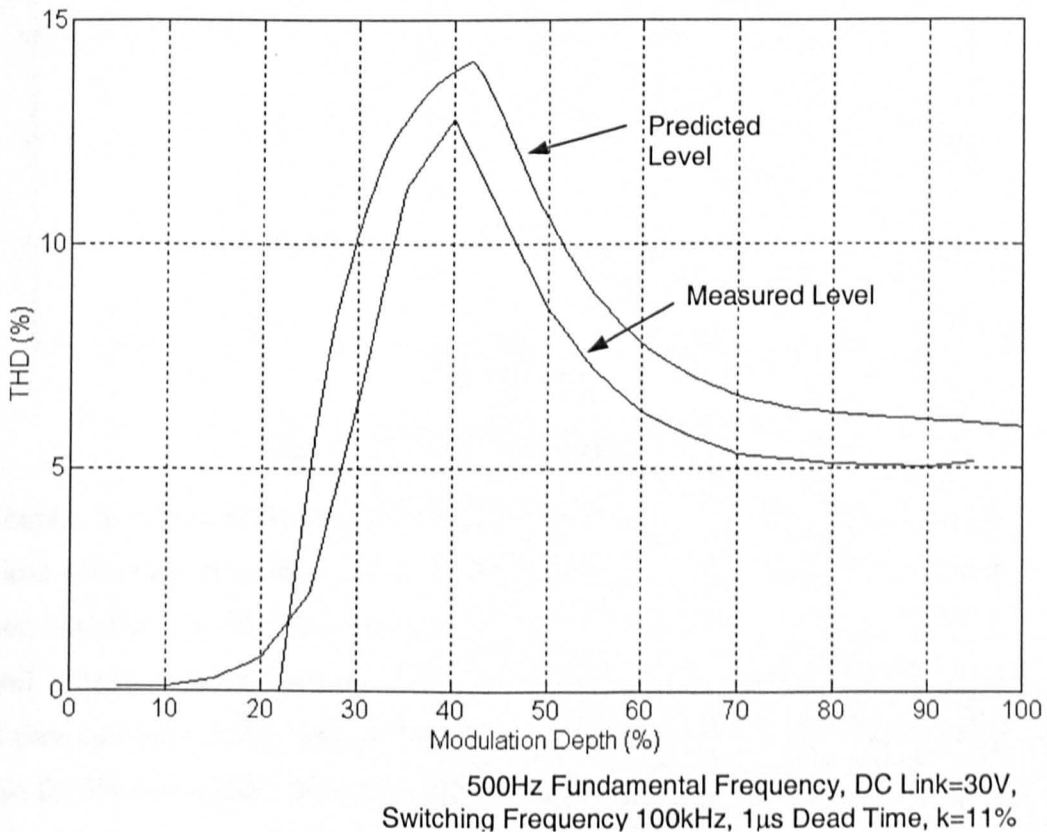


Figure 4.25 - Measured and predicted THD levels

Again, the predicted THD is greater than the measured THD. The general similarity of the curve shapes for the predicted and measured THD levels further suggests that the model presented is reasonably accurate. Note that the THD level is relatively low for modulation depths below ~22% i.e. for modulation depths giving peak duty cycles below the dead band level of 11%. A modulation depth of 22% results in a peak duty cycle of 61%, which is the start of the dead band level.

The model has been used to predict THD behaviour for a range of normalised dead times in order to gauge the likely levels of dead time distortion in a practical system. Figure 4.26 shows the calculated THD profiles for a system with a dead band level of $k=11\%$ and a range of normalised dead times from 1% to 10%.

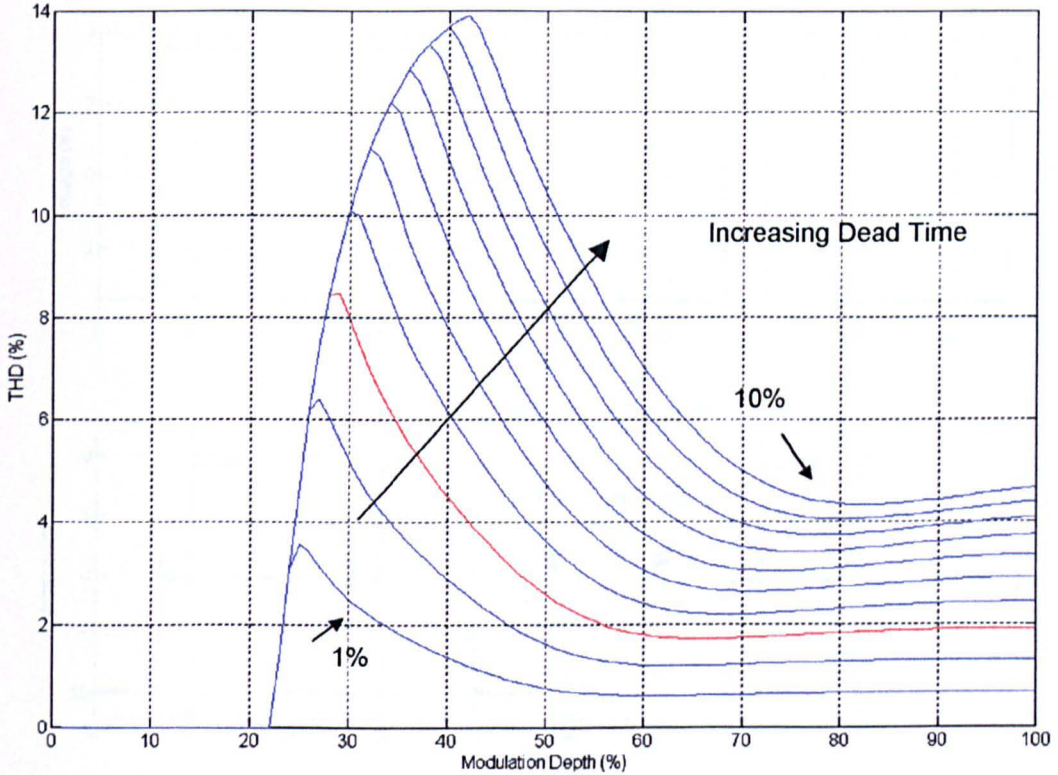


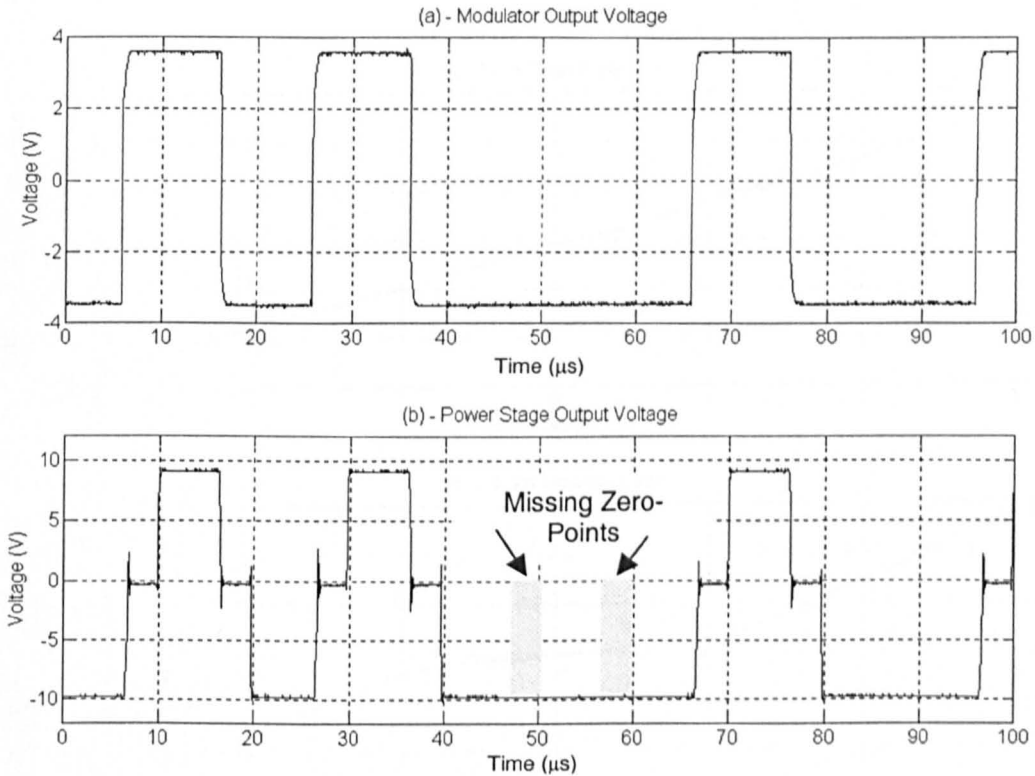
Figure 4.26 - Calculated THD profiles

In Chapter 3, it was concluded that in order to realise a dynamic range of 60dB, the required switching frequency for a double edged, naturally sampled PWM system is around 140kHz. The MOSFET power stage has a minimum dead time requirement of around 200ns to prevent the onset of shoot through and this would suggest a normalised dead time of below 3% is difficult to achieve. The red line in Figure 4.26 indicates the profile for 3% normalised dead time and demonstrates the open loop dead time THD for a practical power stage is in the worst case as high as 8%.

4.4.1.2 PDM Driven

The effect of dead time on a PDM driven power stage is more difficult to quantify due to the stochastic nature of the pulse train from the modulator. Again, consider the case of the power stage loaded with a purely resistive load and run from a PDM modulator. Figure 4.27(a) shows the output of the PDM modulator and Figure 4.27(b) shows the corresponding power stage output pulse.

In Figure 4.27, the missing zero points will contribute to an error offset similar to that with a PWM driven power stage except that their effect must be averaged over a number of clock cycles. To examine the impact of the dead time on the PDM driven power stage, a similar approach to that above was adopted.



DC Link=30V, Clock Frequency=50kHz, 4 μ s Dead Time, Purely Resistive Load

Figure 4.27 - Effect of dead time on voltage output for PDM

By applying a DC level to the modulator and averaging the output from the power stage, a characteristic curve for the power stage can be developed. Figure 4.28 shows the curves measured with two different types of load. In Figure 4.28, the DC input voltage and average power stage output voltage are used since the concept of duty cycle does not apply to a PDM driven system. Since the modulator quantises to $\pm 3.4\text{V}$, a DC input magnitude of 3.4V corresponds to the modulator running at full modulation depth and is equivalent to a PWM system with 100% modulation depth.

Although the impact of the dead time on linearity is not immediately apparent for the plot in Figure 4.28(a), the increased inductance used in Figure 4.28(b) yields a curve with a distinct non-linearity. However, the pre-determined dead-bands encountered under PWM do not appear when PDM is used and it is more difficult to model the effect. In addition, when higher order modulators are used, the switching waveform becomes more random and changes the nature of the linearity curves.

For input signals close to full modulation depth, the number of switching edges per second with PDM reduces (see Chapter 3). This effectively reduces the number of dead-time errors per second so it is reasonable to suggest that the THD from a PDM driven power stage will decrease with increasing modulation depth.

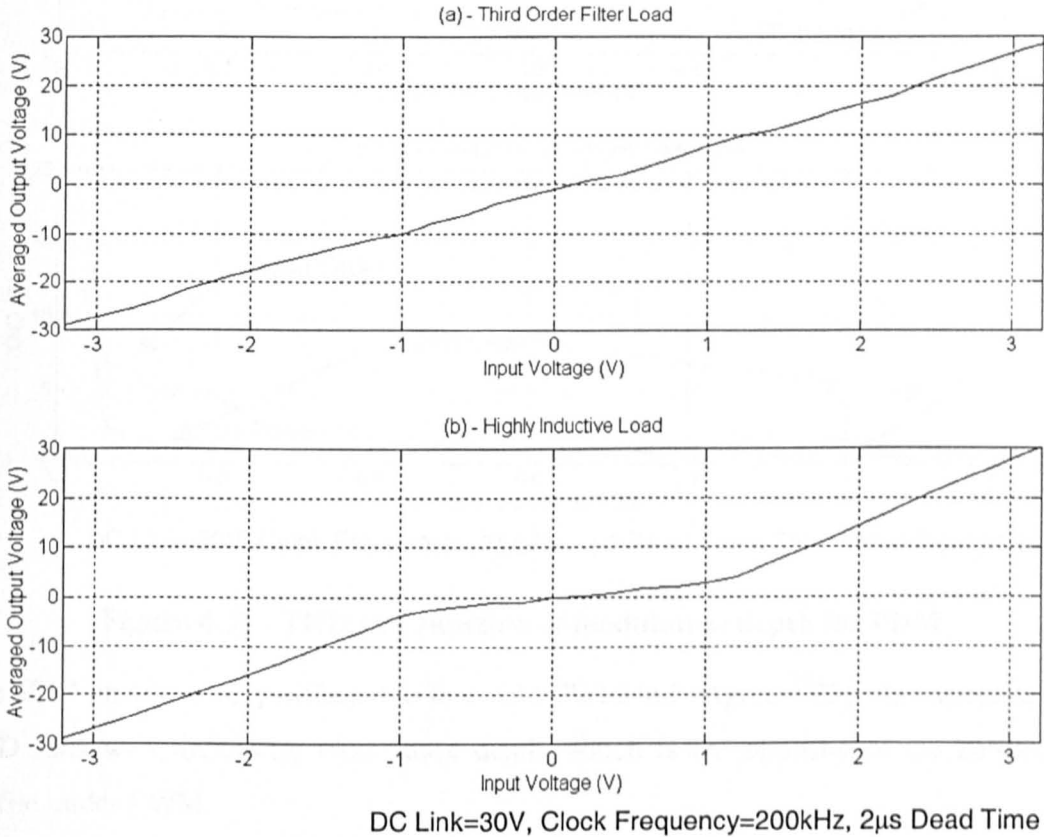


Figure 4.28 - Input/Output profiles for PDM driven power stage

In order to assess the level of harmonic distortion introduced by the non-linearity above, the THD was measured for the power stage driven by a first order modulator. Again, the symmetry of the profiles of Figure 4.28 about 50% would suggest that, in similarity with the PWM case, the dominant PDM distortion will be odd-order.

Figure 4.29(a) shows the resulting THD as a function of modulation depth whilst Figure 4.29(b) shows the relative split of THD between odd and even harmonics. At low modulation depth, the even order terms seem to dominate the THD figure. At higher modulation depth, the THD figure is more balanced between odd and even content whilst at modulation depths greater than unity, clipping occurs and the THD becomes dominated by the odd order terms.

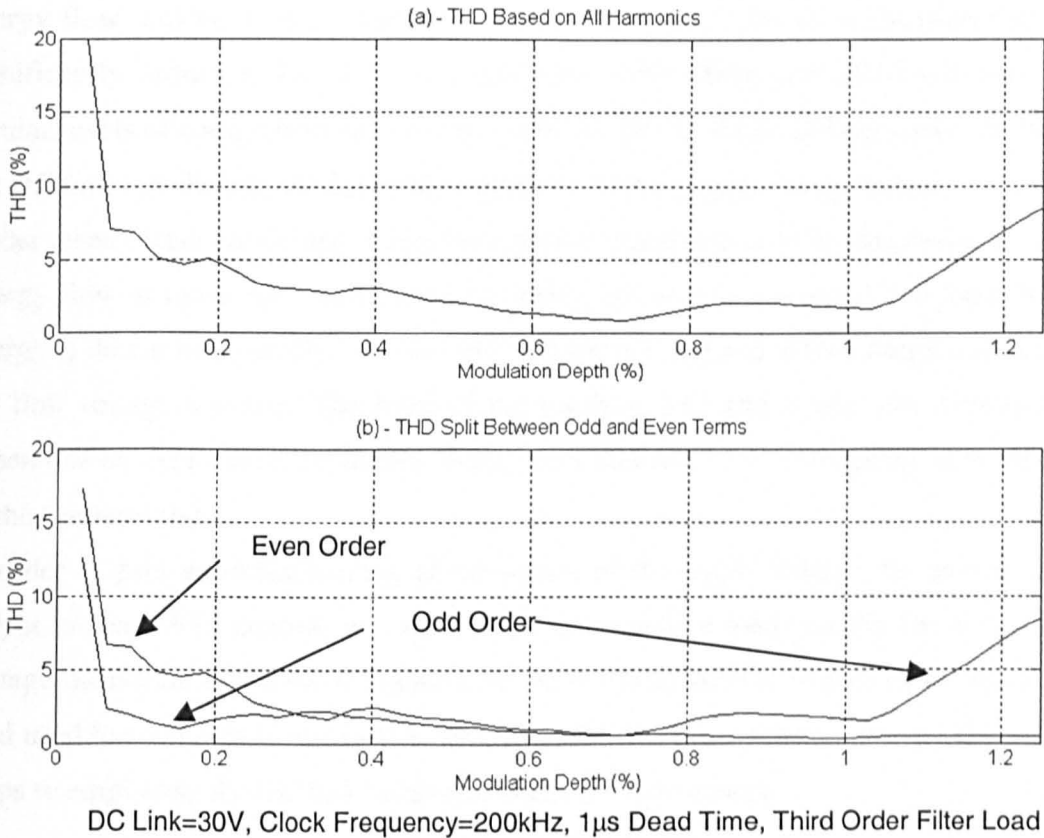


Figure 4.29 - THD as a function of modulation depth for PDM

The THD profile is very different to that with PWM (c.f. Figure 4.25). As expected, the THD falls with increasing modulation depth, which is the opposite of the behaviour profile under PWM.

It is interesting to note that in comparing Figure 4.25 and Figure 4.29, the PDM driven power stage does seem to offer lower THD figures for the same operating conditions. As the order of the driving modulator is increased, the power stage waveform will contain a higher number of switching events and likelihood of the power stage being held in the positive or negative state for a number of cycles is lessened. This will have the effect of flattening the THD-Modulation depth profile.

The effect of increasing the clock frequency or dead time has the same effect for a PDM driven power stage as it has for PWM driven.

4.4.2 DC Link Fluctuation

As mentioned earlier, the DC link supplying power to the output stage is not ideal. In addition, the level of reactive energy flow between the load and power stage is a strong function of load impedance. Since the load impedance varies significantly in both magnitude and phase over the baseband, the level of DC link ripple due to reactive

energy flow will be a strong function of frequency. The type of modulation will not significantly influence the DC link ripple since both PWM and PDM will result in similar levels of energy flow between the load and power stage. In both cases, ripple on the DC link will directly modulate the amplitude of the output voltage pulses.

Under steady state conditions, a sinewave driven reactive load will experience a cyclic energy flow at twice the fundamental frequency between power stage and load. When energy is drawn from the DC link, the link voltage will fall and when energy is returned, the link voltage will rise. The level of the resulting DC link ripple will therefore be dependent on the level of oscillatory energy flow and will have a frequency at twice that of the fundamental.

In order to gain an understanding of the nature of the ripple voltage, the power stage output, under PWM control, was driven into an inductive load and the DC link ripple voltage measured as shown in Figure 4.30. At the fundamental frequency of 50Hz, the load used has a power factor of 0.4, which results in a large reactive energy flow. This helps to emphasise the DC link behaviour under reactive energy.

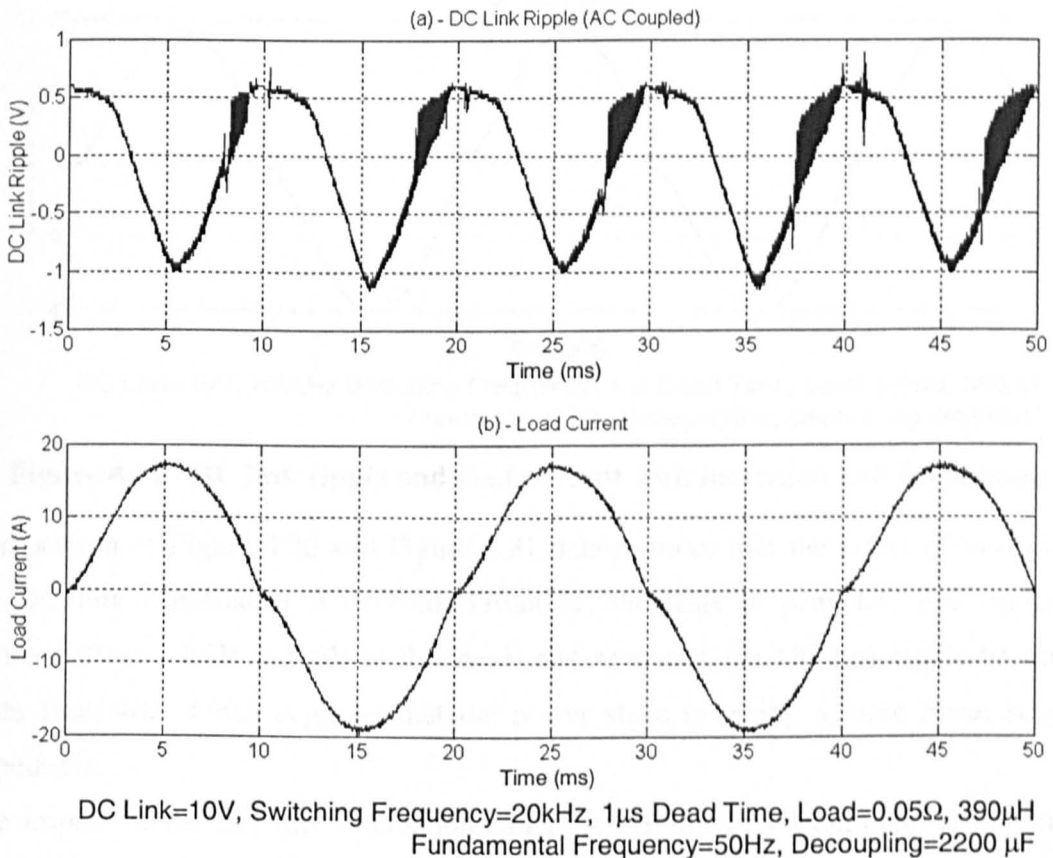


Figure 4.30 - Typical DC link ripple voltage and load current

The fundamental frequency of the ripple voltage is equal to twice the fundamental frequency of the load current. The non-linearity of the DC link supply can be seen with

the ‘flattening’ of the peaks of the ripple voltage. For the waveforms of Figure 4.30 the DC link decoupling capacitance comprised ten 220 μ F electrolytic capacitors connected in parallel. By increasing the level of DC link capacitance, the ripple current can be reduced as shown in Figure 4.31. The waveforms in Figure 4.31 corresponds to the power stage run under identical conditions as for Figure 4.30 except that an additional 22000 μ F capacitor was connected in parallel with the 2200 μ F to give a total DC link capacitance of 24200 μ F.

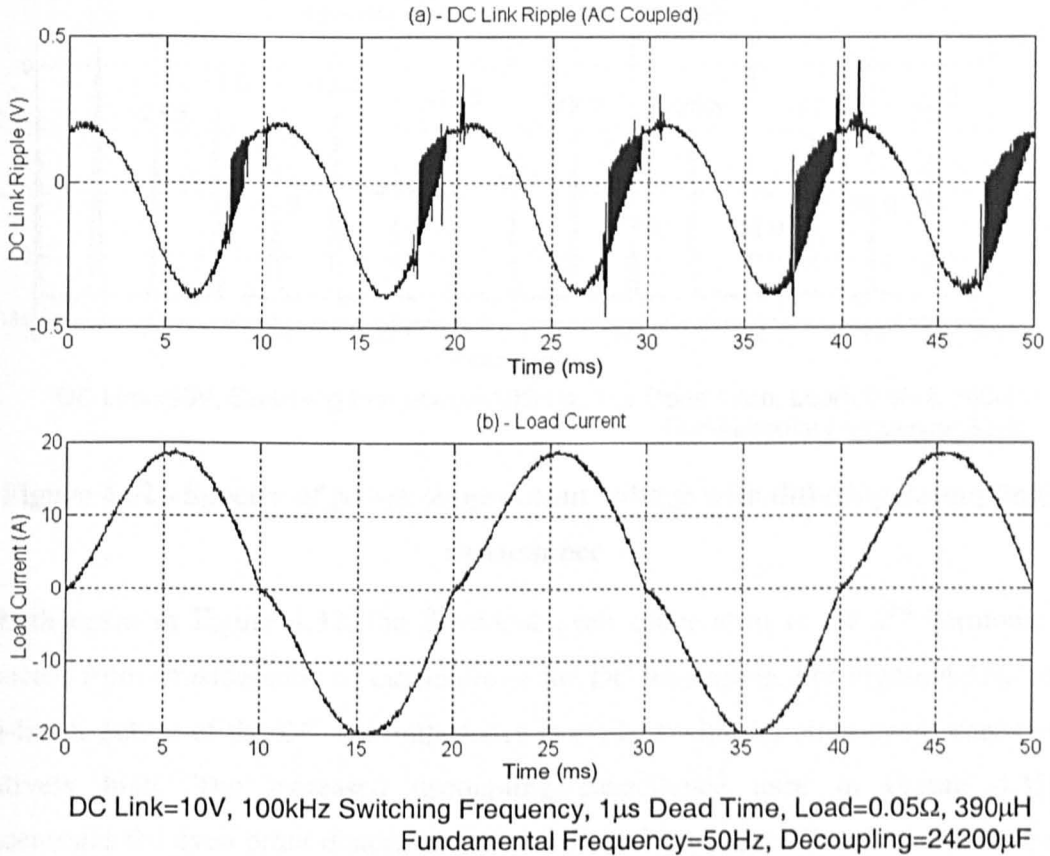


Figure 4.31 - DC link ripple and load current with increased link decoupling

Comparison of Figure 4.30 and Figure 4.31 demonstrates that the effect of increasing the DC link capacitance is twofold. Primarily, the peak to peak DC link ripple is reduced (from \sim 1.5V to 0.6V in this case) and secondly, the DC link ripple becomes more sinusoidal which suggests that the power stage is seeing a more linear supply impedance.

The impact of the DC link fluctuation can be ascertained by examining the spectral content of the power stage output voltage. Figure 4.32 shows the measured spectral content of the output voltage for Figure 4.30 and Figure 4.31.

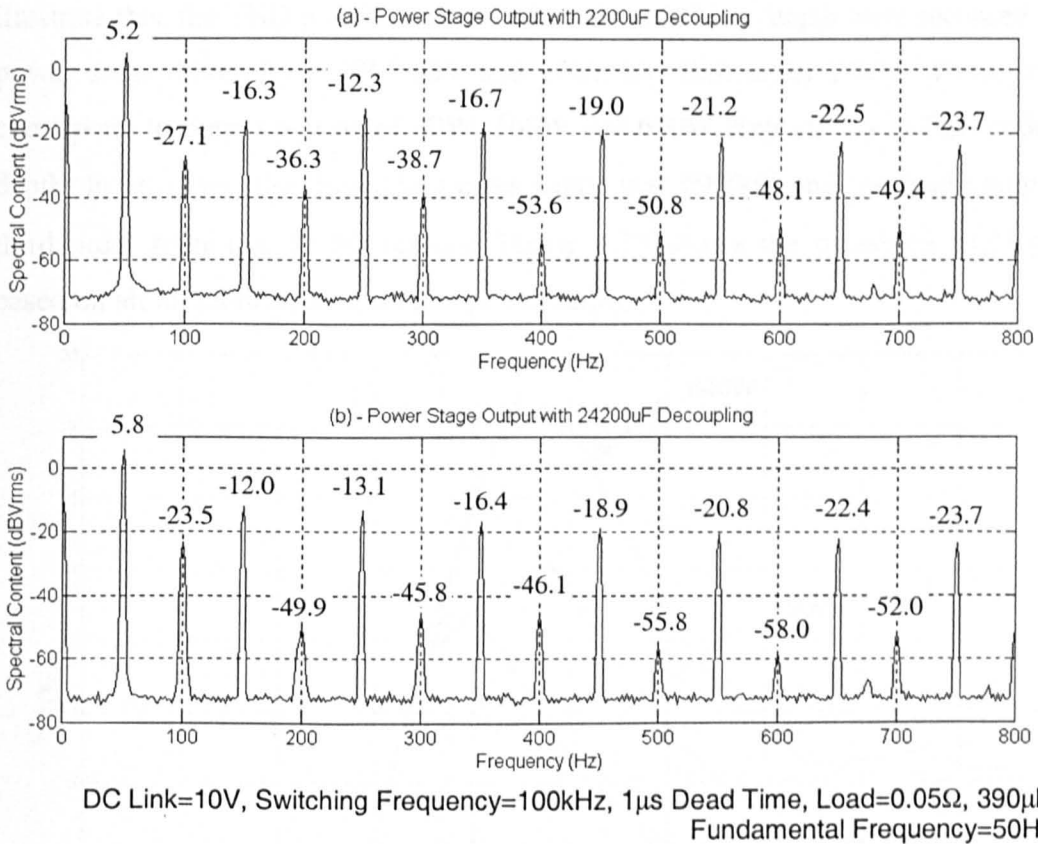


Figure 4.32 - Spectra of power stage output voltage with differing decoupling capacitance

In both cases in Figure 4.32, the dominant even order term is the 2nd harmonic as expected from consideration of the nature of the DC link ripple. For Figure 4.32(a), the non-linear nature of the DC link impedance is evident with the other even order terms relatively high. The increased decoupling capacitance used in Figure 4.32(b) concentrates the even order distortion into the second harmonic. This is not necessarily beneficial since the presence of the larger second harmonic will be more intrusive than if the energy was spread in other even order terms. Moreover, the level of the third harmonic is also affected by the lower level of decoupling. Between the two plots, all the other odd order terms remain the same but there is a small increase in the fundamental level. The measurements taken above demonstrate the behaviour of the DC link in an extreme case of a purely inductive load, which is the worst case for causing DC link ripple since the load operates with a phase shift of almost 90°. With a more realistic filter and load impedance, the DC link ripple will be lower.

For a given level of decoupling capacitance, the DC link ripple will be a function of the reactive energy flow and, therefore, a function of the output power of the amplifier. To

illustrate this, the THD profiles as a function of modulation depth were recorded for the power stage driven by a 30V, 60V and 120V DC link under PWM. These voltages correspond to output powers of 40W, 160W and 640W respectively at full modulation depth. In all cases, the decoupling capacitance was 6900 μ F and the load comprises a third order filter and 11.3 Ω resistor. Figure 4.33 shows the measured THD profile, based on all harmonics, for the three power ratings.

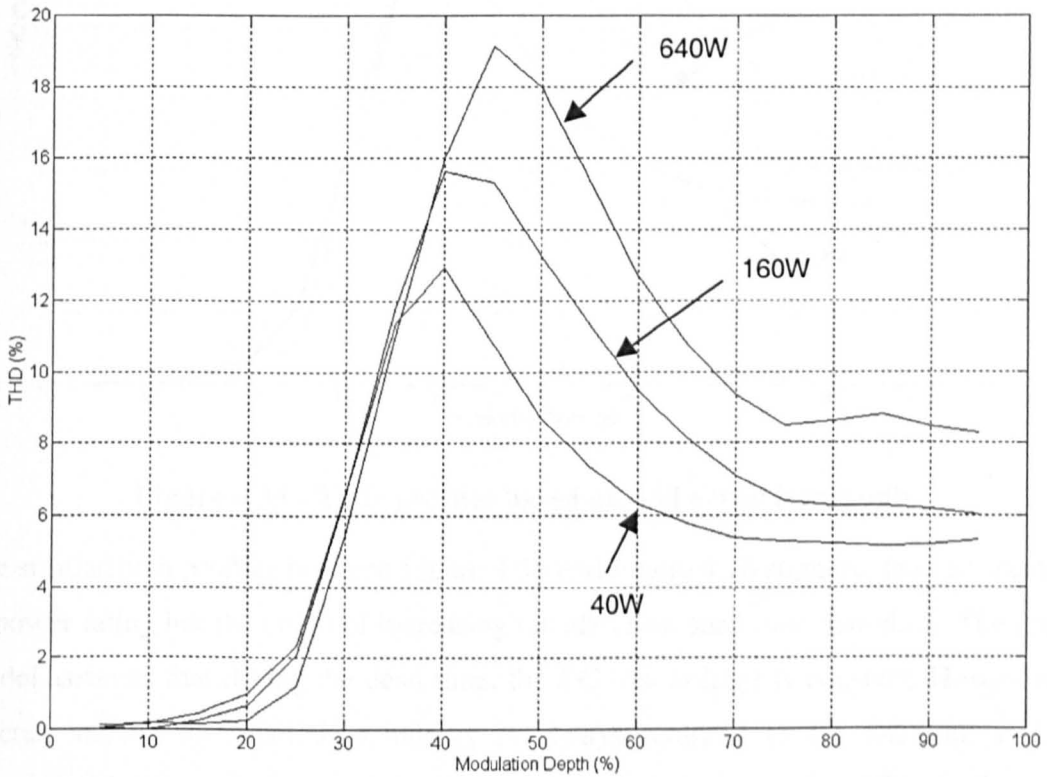


Figure 4.33 - THD as a function of maximum output power

Increasing the power rating of the amplifier has a major impact on the THD profile. Although the THD profiles above are based on the content of all signal harmonics, they show a very similar behaviour to the curves obtained for dead time distortion where just odd-order terms are considered. If the THD profiles for the three different power ratings are calculated based just on the odd-order terms, the graph of Figure 4.34 results.

Comparison of Figure 4.33 and Figure 4.34 demonstrates that the odd-order terms still dominate the THD profile, even at the increased power rating.

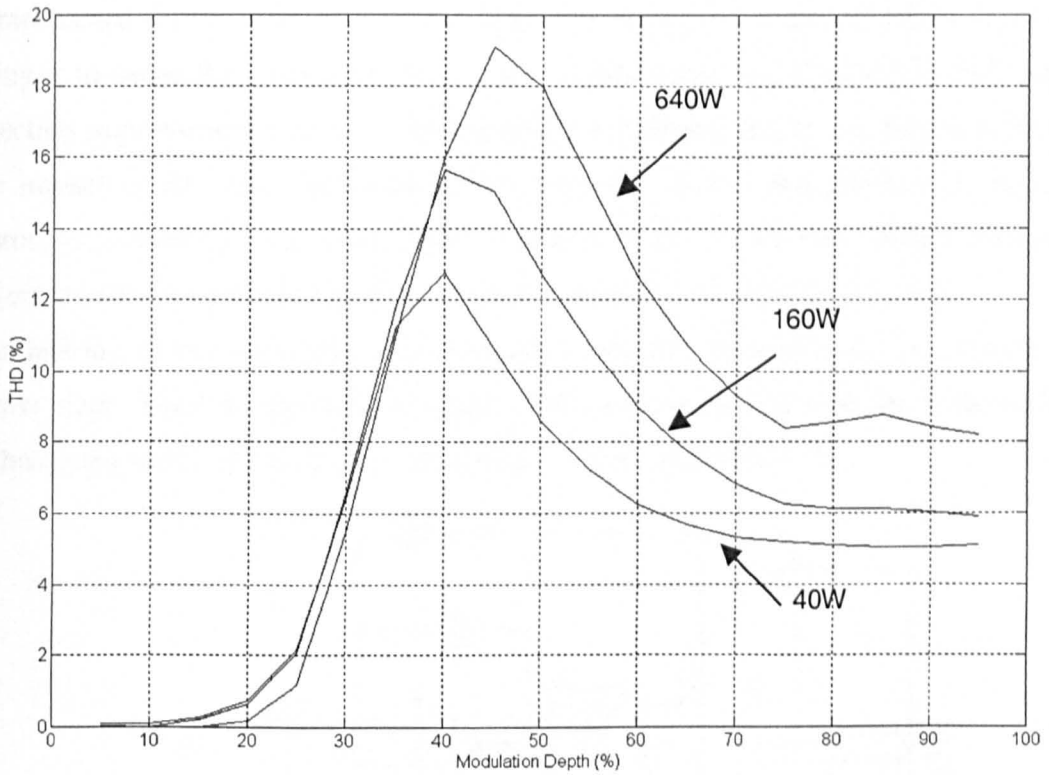


Figure 4.34 - THD profiles based on odd order terms only

The similarity in profiles between Figure 4.34 and Figure 4.26 suggests that the increase in power rating has the effect of increasing the effective dead time distortion. The initial model assumes that during the dead time, the DC link voltage is constant. However, in practice during the dead time, energy is always returned to the DC link via the freewheel diodes and this will cause the DC link voltage to rise. This leads to an increased error voltage and a higher THD profile. As the power rating for the amplifier increases, the energy returned to the DC link is higher for a given modulation depth and therefore the effect will be greater.

4.5 Use of Feedback

Whether the power stage is driven by PWM or PDM, the power amplification process is essentially non-linear. By using feedback from the power stage output, the impact of the non-linearity can be minimised resulting in a system that should perform to the required fidelity.

4.5.1 Under PWM

Since PWM driven power stages have been used for a number of years, various feedback schemes have been proposed to increase their linearity. Smith [4.9]

compensated for the effect of DC link ripple by feeding back the DC link voltage and using it to shape the input audio signal. It is claimed that this achieved a 40dB ripple rejection improvement over conventional PWM amplifiers. Whilst this approach lessens the impact of DC link fluctuation on the linearity, it does not address the issue of distortion caused by dead time. Direct feedback of the power stage output voltage is required and this approach has been adopted in more recent designs [4.7, 4.8].

Vanderkooy [4.10] highlights two techniques that can be employed to linearise the power stage. The first approach, based on a Hysteresis controller was one of the earliest techniques used [2.4] and its basic operation is shown in Figure 4.35.

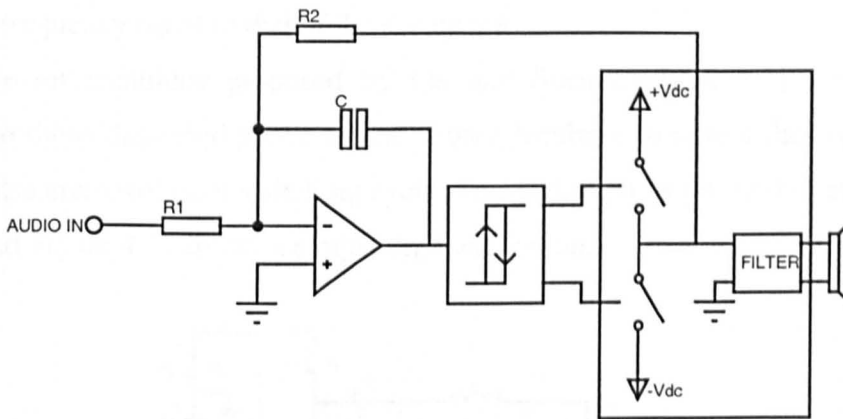


Figure 4.35 - Basic hysteresis controlled PWM power stage

In this control scheme, the switching frequency in the output stage is not fixed but is dependent on the hysteresis level in the power stage and the integrator time constant. As the signal amplitude increases, the effective switching frequency falls and this is beneficial in reducing switching loss. In addition, since the feedback effectively ensures the pulse area is correct at the end of every cycle, it is very effective at reducing the impact of power stage non-linearities. The drawback of this power stage is that at large modulation depths, the effective switching frequency approaches zero and this causes severe problems for the output filters. The ‘Entrained’ controller, shown in Figure 4.36, proposed by Vanderkooy, adapts the hysteresis controller in order to fix the switching frequency whilst retaining the benefits of distortion reduction through feedback.

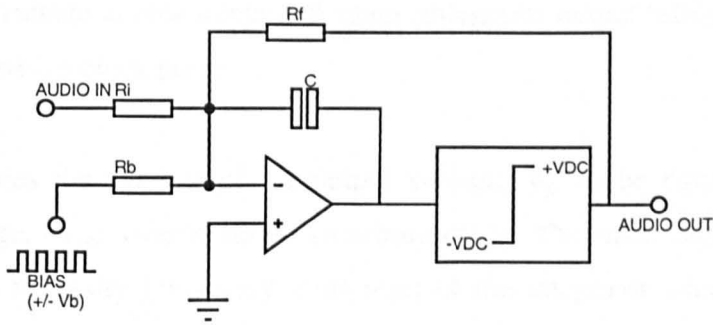


Figure 4.36 - 'Entrained' PWM controlled power stage

In this approach a square wave bias signal forces the output stage to switch at a minimum frequency equal to that of the square wave.

A more recent technique proposed by Lai and Smedley [2.9, 4.8] uses a similar principle to those described above in that it uses feedback to obtain the correct output voltage pulse area over each switching cycle. This technique is referred to as 'one-cycle control' and Figure 4.37 shows a simple implementation.

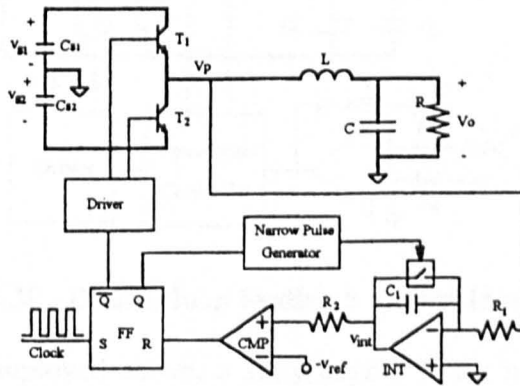


Figure 4.37 - Simple one-cycle control (Source – [4.8])

The basic approach used in one-cycle control is as follows: -

1. When a clock pulse arrives, the flip-flop is clocked, which sets \bar{Q} low and Q high. This switches T_2 on and T_1 off.
2. The output of the integrator then begins to rise from its initial value (due to the inversion in the op-amp integrator).
3. When the integrator output is above $-V_{ref}$, the comparator resets the flip-flop, forcing Q low and \bar{Q} high. This switches T_2 off, T_1 on and triggers the narrow pulse generator to reset the integrator.

- The output voltage is now integrated again (integrator output falls) until the system is restarted with a clock pulse.

This action forces the average of the output voltage, V_p , to be equal to that of the reference voltage, $-V_{ref}$, over a single switching cycle. The main drawback with this approach is the necessity for a very short reset of the integrator which in practice is difficult to achieve.

The feedback techniques discussed so far all use the output voltage from the power switches as a feedback signal. Any non-linearity in the filter will therefore compromise system linearity. In [2.9] Lai and Smedley use one-cycle control and additional negative feedback, in the form of a conventional phase lead compensation network, to linearise the power filter. Figure 4.38 shows the system with this double feedback approach.

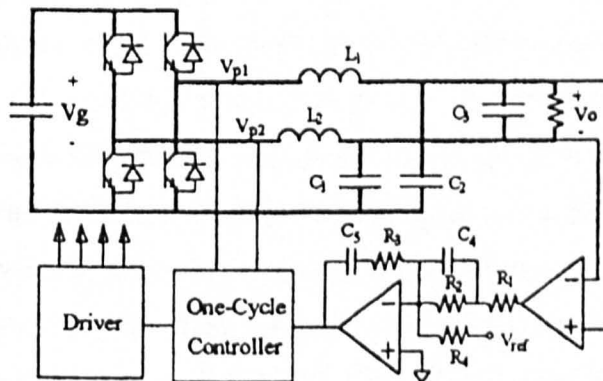


Figure 4.38 - Double loop feedback system (Source - [2.9])

With the controller employed above, a sixty degree phase margin was achieved and results from an experimental prototype demonstrated a THD of around 0.1% over the full bandwidth (compared to 0.5% with only the one-cycle control employed).

Thus, the performance achievable with closed loop control can match that of linear amplifiers. Optimal system performance, however, will be achieved only if the power stage is designed to be as linear as practically possible before feedback is added.

4.5.2 Under PDM

To date, little work has been done using feedback with a PDM driven power stage. However, the standard PDM modulator uses feedback as an inherent part of its operation. By simply including the power stage within the feedback loop as shown in Figure 4.39, the error introduced by the power stage can be corrected for. The only additional circuitry required is a differential amplifier to convert the power stage output

voltage to a signal referenced to ground and an attenuation block to reduce the voltage pulse level to one that the modulator can accept. This attenuation effectively controls the gain of the amplifier.

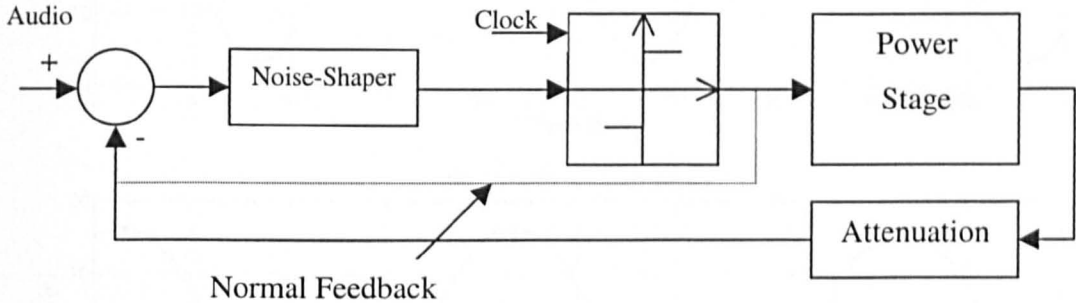


Figure 4.39 - Implementation of a closed loop PDM driven power stage

The use of closed loop control raises a number of practical issues. Due to the use of dead time, a minor delay, equal to the dead time, is introduced between the power stage input and output, which could potentially destabilise an originally stable modulator. The dead time delay should therefore be included in the original $\Sigma\Delta$ modulator design to ensure stability. If the modulator is to be implemented in the digital domain, an A/D converter must be included in the feedback path. Even though the distortion effects have been modelled by averaging the high frequency waveform, the actual mechanisms are very short, for example 200ns, and therefore the A/D converter must be run at a very high frequency to capture the distortion effects. Since high performance A/D converters are expensive, this could compromise the realistic implementation of a digital system.

The improvement in linearity can be demonstrated by comparing the current for open and closed loop PDM driven power stage. A simple analogue modulator was used and Figure 4.40 shows the output current in an open loop (a) and closed loop (b) power stage.

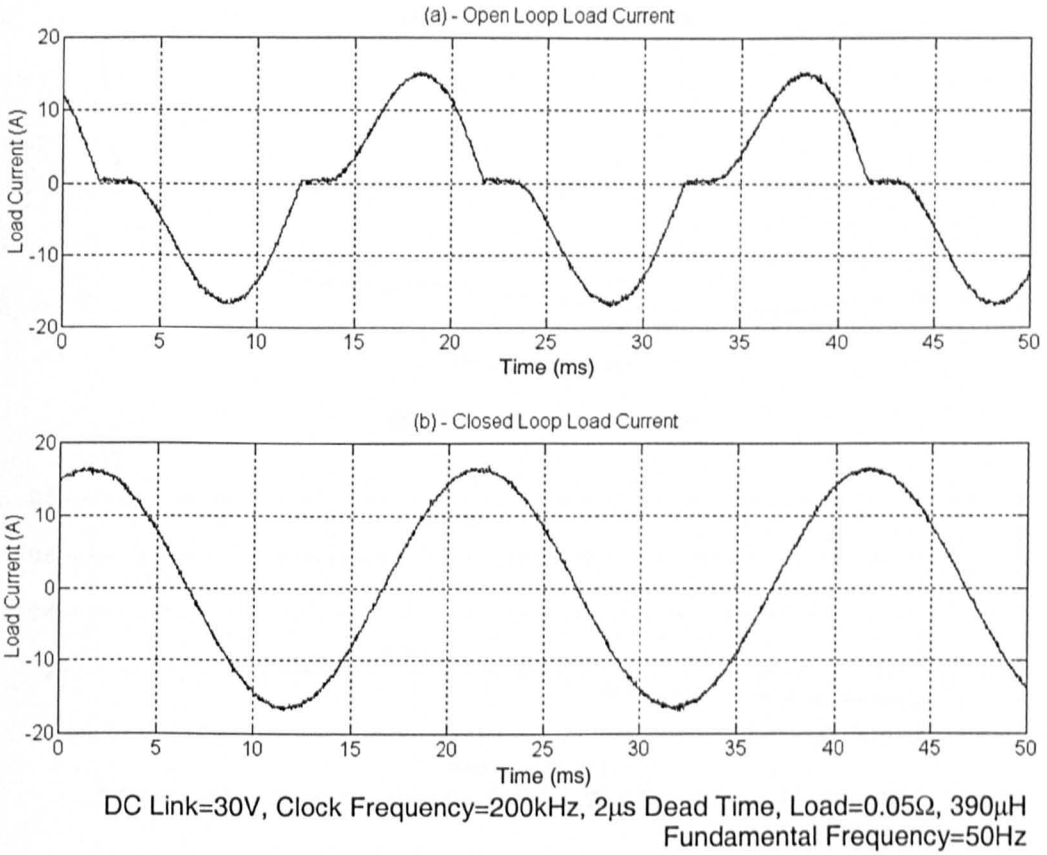


Figure 4.40 - Effect of closed loop control on linearity

Under closed loop control, the ‘crossover’ distortion introduced by the non-linearity is practically eliminated and the improvement can be seen when the THD profiles of the open and closed loop control cases are compared, Figure 4.41. The THD profile of the closed loop amplifier, Figure 4.41, is much the same for the open loop case except that all the figures are approximately 26dB lower.

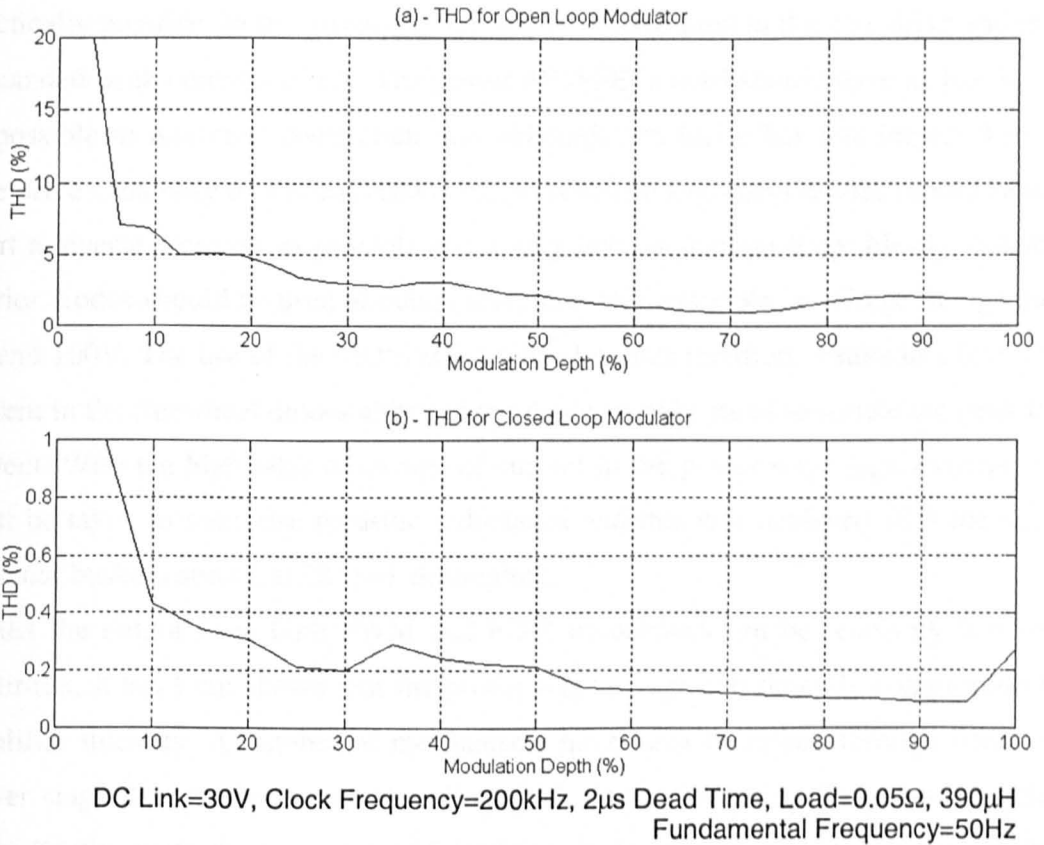


Figure 4.41 - Open and closed loop THD profiles

Although the closed loop modulator offers increased linearity, the THD is still above the desired level required of around 0.1%. It is important, therefore, that the open loop linearity is optimised before feedback is used.

In conventional closed-loop control systems, the higher the open loop gain in the baseband, the lower will be the impact of any non-linearity in the power stage assuming the system remains stable in closed loop control. Therefore, increasing the gain of the noise-shaper should decrease the impact of system non-linearity. In addition, the use of double feedback in the PWM driven power stage further increased system performance and it should be possible to apply this to a PDM driven system.

4.6 Conclusions

Tests on a prototype have demonstrated that a Class-D power stage can offer conversion efficiencies approaching 90%. At the switching frequency required for reasonable fidelity (~150kHz), the switching loss in the power stage forms the dominant loss mechanism and therefore the design of the gate drive circuitry has a critical impact on the conversion efficiency. Specifically, the gate drive resistance should be as low as

practically possible. In the prototype, 2Ω resistors were used in the gate drive and these demanded peak currents of 6A. The power MOSFETs used should have as low $R_{DS(on)}$ as possible to minimise conduction loss although this factor has less impact than the gate drive capability on the conversion efficiency. The freewheel diodes should have as short a reverse recovery as possible and a very low conduction drop. Ideally, Schottky barrier diodes should be used although these are only available in voltage ratings up to around 100V. The use of the MOSFETs as synchronous rectifiers results in a low RMS current in the freewheel diodes although the diode must be rated to handle the peak load current. With the high rates of change of current in the power stage legs, extreme care must be taken to minimise parasitic inductance and this was achieved with the use of coplanar busbars and local DC link decoupling.

Whilst the output from both PWM and PDM modulators can be relatively free from distortion, it has been shown that the power output stage can severely compromise the amplifier linearity. A number of mechanisms have been described through which the power stage distorts the baseband audio signal. At the switching frequencies required for hi-fidelity performance, the use of dead time is the largest single factor to contribute to distortion and the effect manifests itself in odd-order terms. The level of distortion is also dependent on the type of load presented to the amplifier. A purely resistive load results in the lowest THD whilst the reactive energy flow associated with an inductive filter load causes both dead-time error and DC link ripple.

An accurate model for the effect of dead time with a bipolar PWM strategy has been developed and a worst case THD of 8% is a realistic level for a power stage switching at 140kHz with a dead time of 200ns. Under PDM, the distortion is more difficult to describe but shows a generally decreasing behaviour with modulation depth and is lower than that of an equivalent PWM driven amplifier.

The high levels of open loop distortion necessitate the use of feedback to linearise the power stage. PWM control has been explored in depth in recent years and has resulted in systems that can perform at least as well as their linear counterparts. The more successful strategies have used a feedback technique which corrects for errors over a single switching cycle. A simple feedback strategy has been explored with a PDM driven power stage and has been shown effective at reducing the open loop distortion by a factor of 20. All the feedback strategies discussed are only effective at reducing the

open loop distortion and therefore the power stage must be made as linear as possible before feedback is added.

With a fixed minimum dead time, the normalised dead time will increase with switching frequency. Thus, higher switching frequencies will tend to lead to higher dead time distortion and this limits the performance of the stage. Conversely, a decrease in switching frequency will result in lower dead time distortion. However, a reduction in switching frequency will be accompanied by an increase in foldback distortion introduced by the modulator and therefore an optimal switching frequency will exist where the combined foldback and harmonic distortion is lowest.

5 Integrated Power Stage

5.1 Introduction

The conventional H-Bridge power output stage discussed in Chapter 4 represents the preferred topology for the majority of Class-D amplifier designs. However, in order to realise a complete amplifier system, the output stage requires a steady, high voltage DC supply. The method used to generate this supply depends on the nature of the initial energy source (i.e. AC or DC) and its power rating.

For a mains powered amplifier, a standard transformer/rectifier arrangement offers a simple solution, although this type of power supply is bulky and inefficient and its use is normally restricted to low power applications. When used for high power applications, the power transformer and smoothing capacitors are often the single highest cost in the amplifier system. In addition, the DC rail smoothing capacitors need to have high capacity in order to sufficiently attenuate the 100Hz ripple present on the output and are therefore costly and bulky. In addition, the DC rail smoothing capacitors, which are usually high capacity electrolytic types in order to sufficiently attenuate the 100Hz ripple on the output, are costly, bulky and of poor long term reliability.

Developments in switched mode power supply (SMPS) technology have now presented a practical alternative to the simple transformer/rectifier arrangement and even at moderate power levels offer advantages over the traditional arrangement. The benefit to be gained with a SMPS is the dramatic reduction in transformer size and DC filter capacitors, due to ultrasonic switching frequencies, and a significant increase in conversion efficiency. In addition, the switching nature of this type of supply facilitates the use of feedback control strategies to give very good regulation and dynamic behaviour. However, even with a SMPS, a large smoothing capacitance is required due to the single quadrant nature of the power supply and the requirement to store regenerative energy from the reactive load.

For car audio applications, the primary energy source is the 12V car battery and since this energy source is DC, a SMPS must be used to give the boost in voltage level required. For example, a typical 500W output stage would require a 64V DC link when driving into a 4 Ω loudspeaker.

The conventional linear or Class-D amplifier systems used in car audio are made up of the elements as shown in Figure 5.1(a) and (b) respectively. The class-D amplifier requires an additional output filter, which is not needed with a linear power output stage.

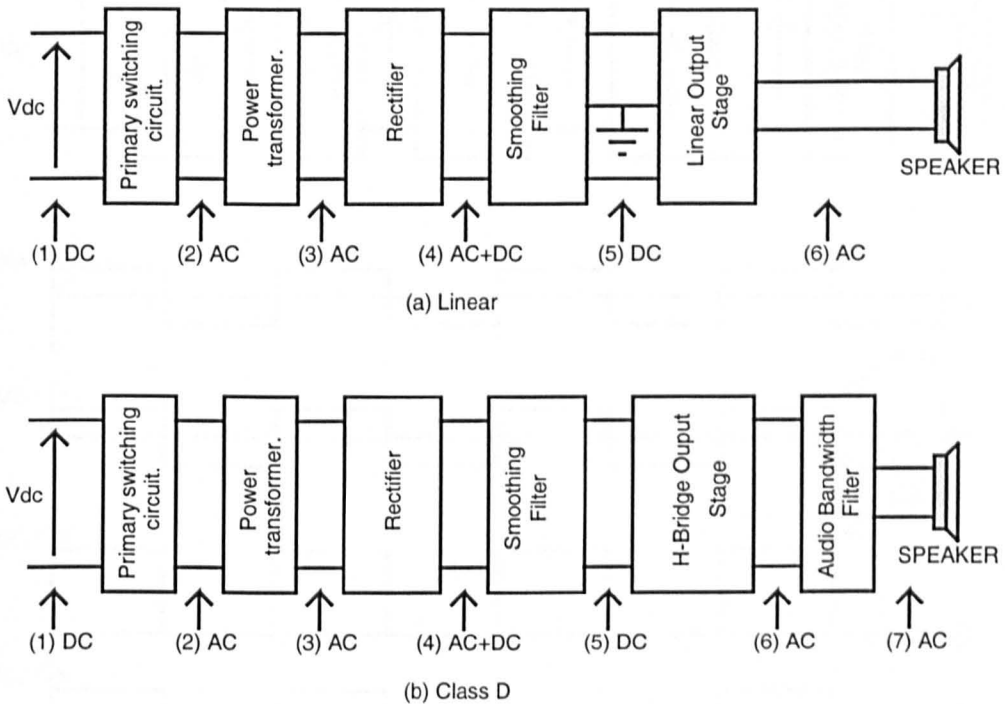


Figure 5.1 – Conventional in-car audio power amplifier

Both these systems require a SMPS and typically, as shown in Chapter 1, Figure 1.2, the current state of the art amplifier uses a push-pull SMPS that occupies over half the volume of the entire amplifier. The majority of the SMPS volume is occupied by the twelve decoupling capacitors required for the main 12V supply and the six capacitors and large ferrite inductor of the output filter.

The focus of this chapter is the development of a power stage which combines the SMPS and H-Bridge output stage by eliminating the requirement for an intermediate DC supply, thereby eliminating the need for a large DC rail reservoir capacitor and smoothing inductor. Not only will this reduce the size of the overall converter, it will also allow for a cost reduction. The approach is to direct the voltage pulses provided by the secondary of the SMPS to the load using the H-Bridge to form the required audio signal. As will be demonstrated later, this also will allow for a partial soft switching system since the voltage across the H-Bridge will be zero for a short period within each cycle.

Figure 5.2 gives the structure of the proposed power stage and simplified voltage at different parts of the circuit.

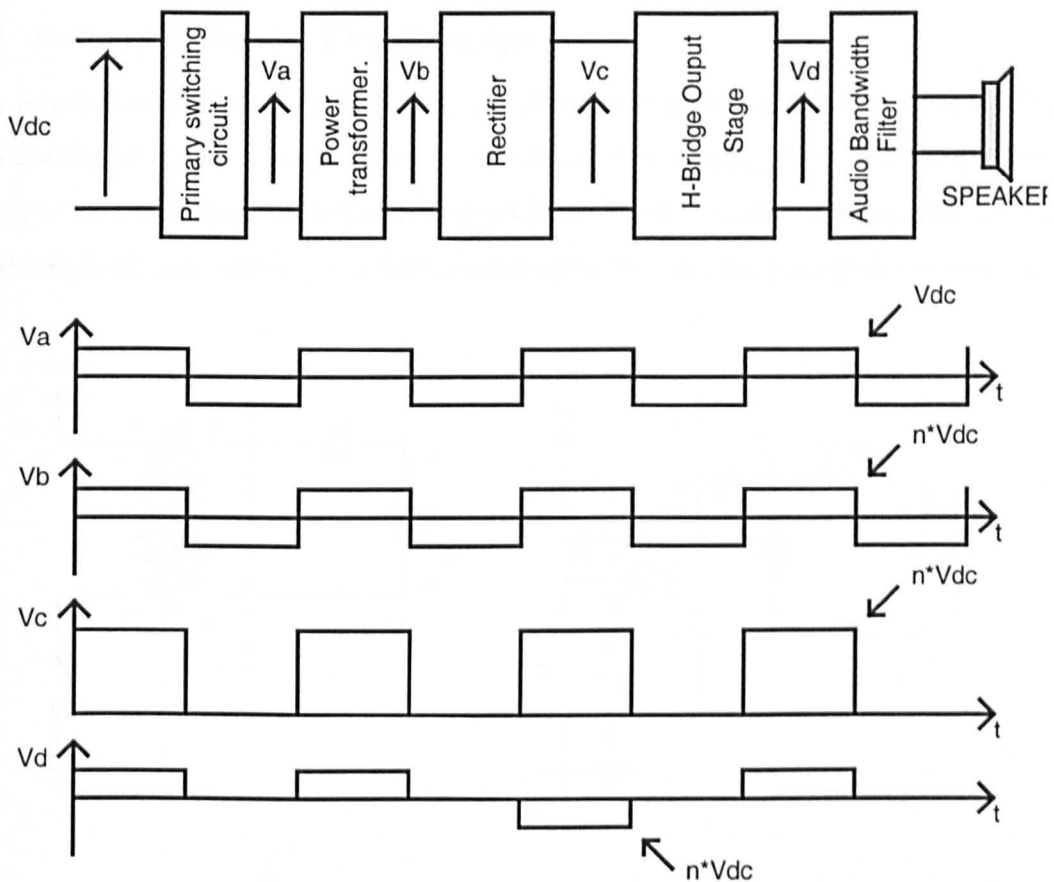


Figure 5.2 - Function of proposed power stage

The function of the primary switching circuit is to provide a high voltage pulse stream to the H-Bridge output stage. The output stage can be driven using PDM by switching the primary stage at a constant duty cycle and then using the H-Bridge to choose pulse polarity. Alternatively, PWM can be realised by varying the duty cycle of the primary switch and the using the power stage to choose pulse polarity. One further benefit of this power stage is that there is a period every switching cycle when the voltage across the H-Bridge is zero and therefore the H-Bridge can be switched under zero voltage conditions, thereby minimising switching loss. Through the action of the H-Bridge choosing pulse polarity, the effective maximum pulse frequency from the output of the H-Bridge is half the frequency of the primary switching device. Therefore, the primary switching device must be designed to deliver pulses at a frequency of twice the maximum required modulation switching frequency.

The design of the power stage was considered as two separate sections; the design of the primary switching circuit and transformer and the design of the H-Bridge & secondary side circuit. The modulation of the new power stage will be covered in Chapter 6.

5.2 Primary Switching Circuit Design

The function of the primary switching circuit is to transform the battery input voltage into a series of higher voltage pulses. A suitable circuit topology for this function can be found by considering present SMPS designs [5.1]. Figure 5.3 shows the circuit diagrams for the flyback converter (a), the forward converter (b), and the push-pull converter (c).

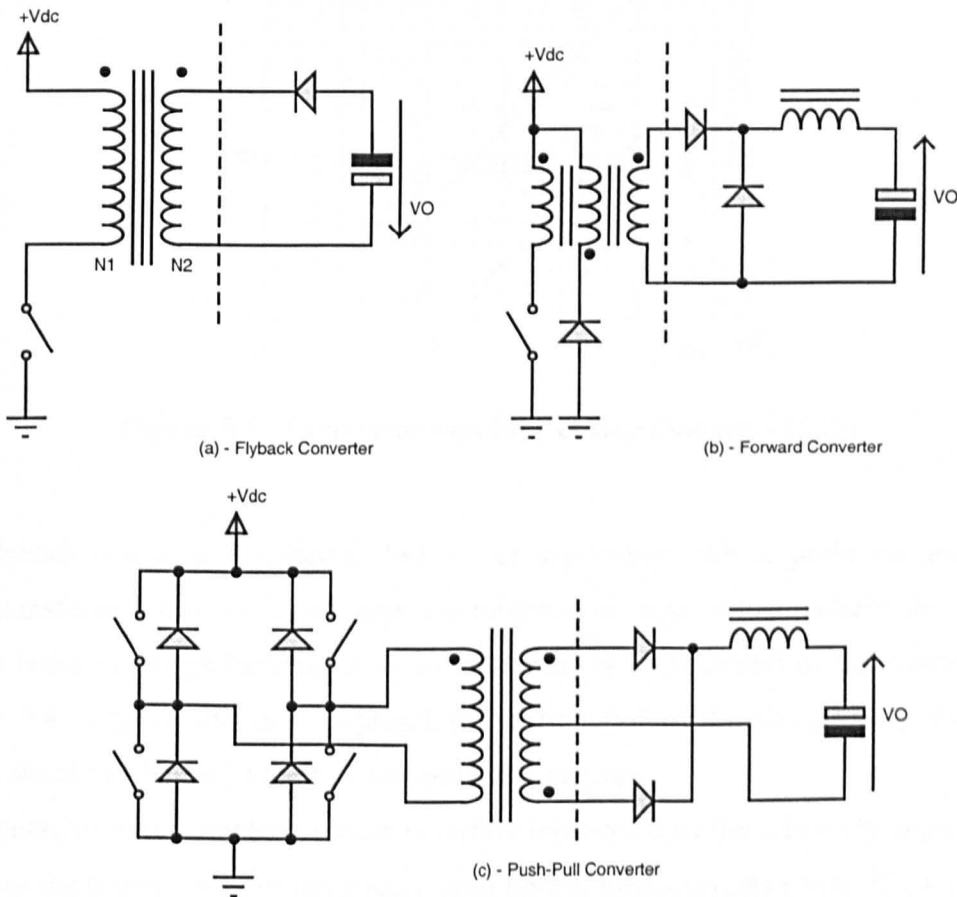


Figure 5.3 - SMPS circuit topologies

These different topologies can be subdivided into two main categories; circuits that drive the transformer core in uni-polar flux (Flyback and Forward Converters) and circuits that drive the transformer core in bi-polar flux (Push-Pull Converters).

Circuit topologies operating with uni-polar flux tend to require a larger transformer core than a similarly rated bi-polar flux converter. As such, the uni-polar converters are found in low to middle power rated equipment whilst the bipolar converters are generally found in middle to high power rating region. Philips [5.2] give an approximate design guide as shown in Figure 5.4.

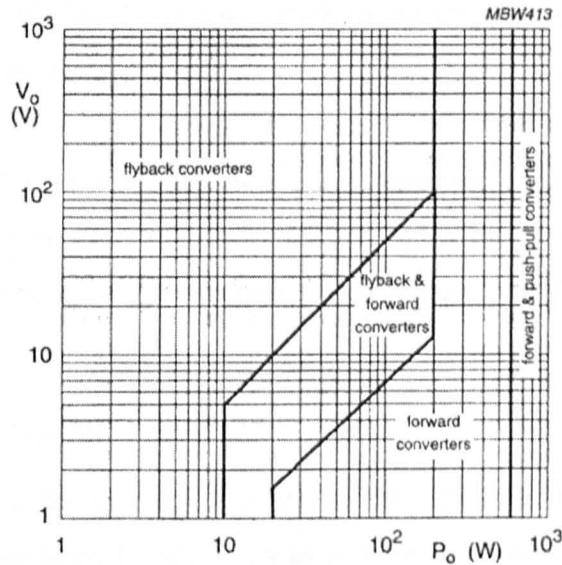


Figure 5.4 - Converter topology choice (Source – [5.2])

The flyback converter is suited to low power applications where problems associated with transformer leakage inductance are minimal or high voltage where the lack of output inductor brings benefits. For the 500W rating requirement of the power stage, Figure 5.4 suggests the most appropriate circuit topology for the primary switching circuit should be based on the forward converter primary.

Consideration of the topology choice is further influenced by the relatively large current levels in the primary side of the circuit, with typical peak currents above 100A and low input voltages. The resistance of the path through which the primary current flows must be minimised in order to achieve the highest possible efficiency. The forward converter topology is an attractive choice since there is only one semiconductor device in the primary current path and this, combined with the use of busbars or heavy gauge PCB, will minimise conduction loss.

The benefit of having a single switching device can further be exploited by placing the device on the high side of the transformer. This is conducive to reducing the EMI from

the converter since the drain connected tab on the device package is at a fixed potential. With the device located on the low side, as in Figure 5.3(b), the drain oscillates from zero volts during device conduction, to high voltage during device blocking. This will lead to charging and discharging of the parasitic capacitance between tab and heatsink at the frequency of the switching waveform and cause high frequency currents to flow in the heatsink, resulting in EMI emissions. If the device is in the high side, the tab remains at the DC supply level and a reduction in the EMI level is possible. However, the use of the device in the high side requires a floating gate drive circuit that adds to cost and complexity.

Although the forward converter only runs the transformer in uni-polar flux, the high switching frequency being used will result in a physically small transformer. With these issues in mind, it was decided that the forward converter primary side topology would be used for the primary converter.

5.2.1 Initial Design Issues

In order to understand the issues important in the design of the primary switching circuit, a prototype converter, Figure 5.5, was constructed. The converter was designed to deliver 100W into a purely resistive secondary side load at a switching frequency of 300kHz and a duty cycle of 50% from a 12V DC supply. For the 11.3Ω load used, a turns ratio of 1:4 is required between primary and secondary to boost the output voltage to 48V. Although the resistive load is not an accurate representation of the load presented by the H-Bridge output of the proposed amplifier, it provided a simple means of highlighting many of the operating conditions of the primary side circuit.

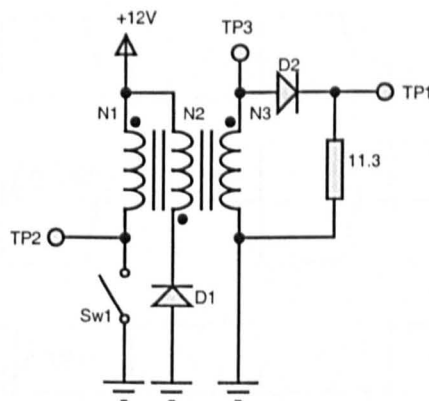


Figure 5.5 - Primary side test circuit

The primary switch was realised with a single low $R_{\text{DS(on)}}$ ($10\text{m}\Omega$) power MOSFET driven by a signal generator via a totem pole buffer stage. A Philips ETD39 core with a centre pole area of 125mm^2 was used with two primary turns, N_1 , and eight secondary turns, N_2 . The tertiary winding, N_3 was wound with a single turn to ensure the circuit was able to run at the required 50% duty cycle. Figure 5.6 shows the prototype circuit including a large decoupling capacitor for the 12V DC link.

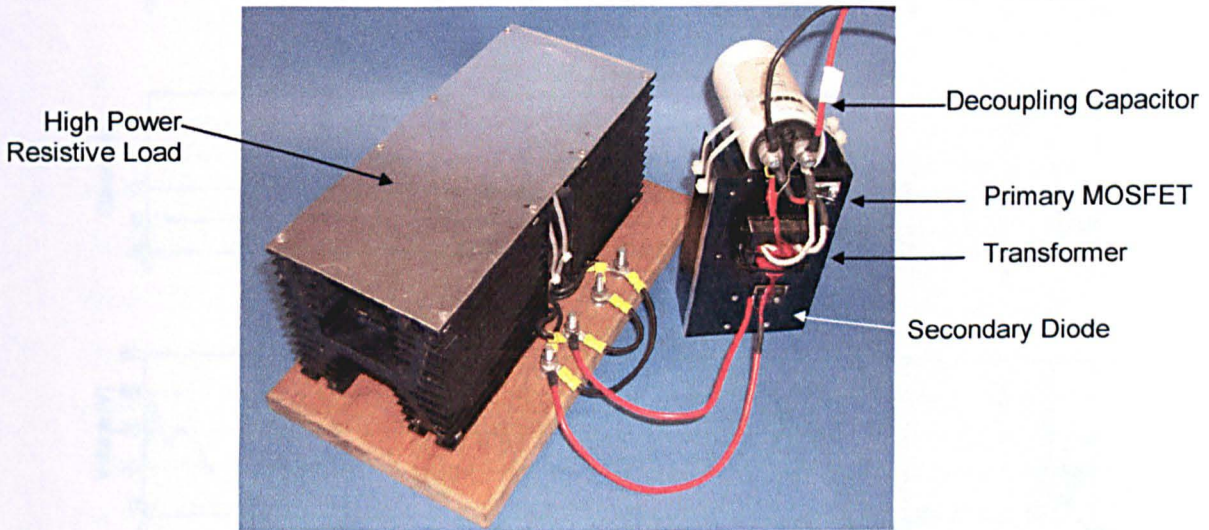


Figure 5.6 - Prototype primary circuit (Drive circuit not shown)

For a forward converter, with the secondary connected as in Figure 5.5, the idealised circuit waveforms would be as in Figure 5.7.

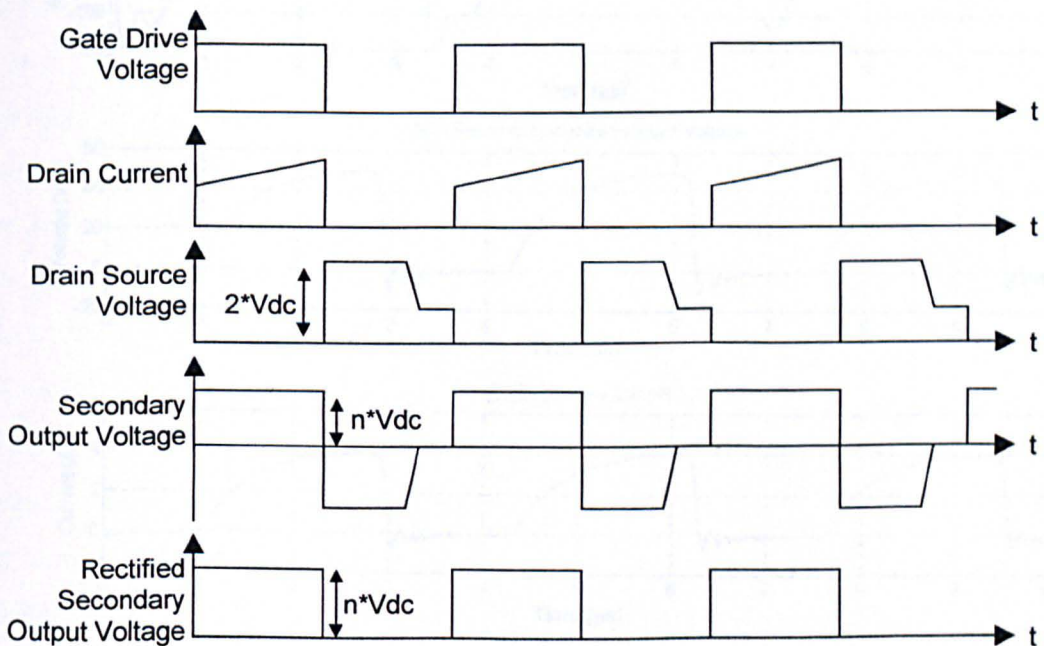


Figure 5.7 - Idealised forward converter waveforms (not to scale)

The power stage was run with the operating parameters described above and Figure 5.8 (a-f) shows the measured circuit waveforms.

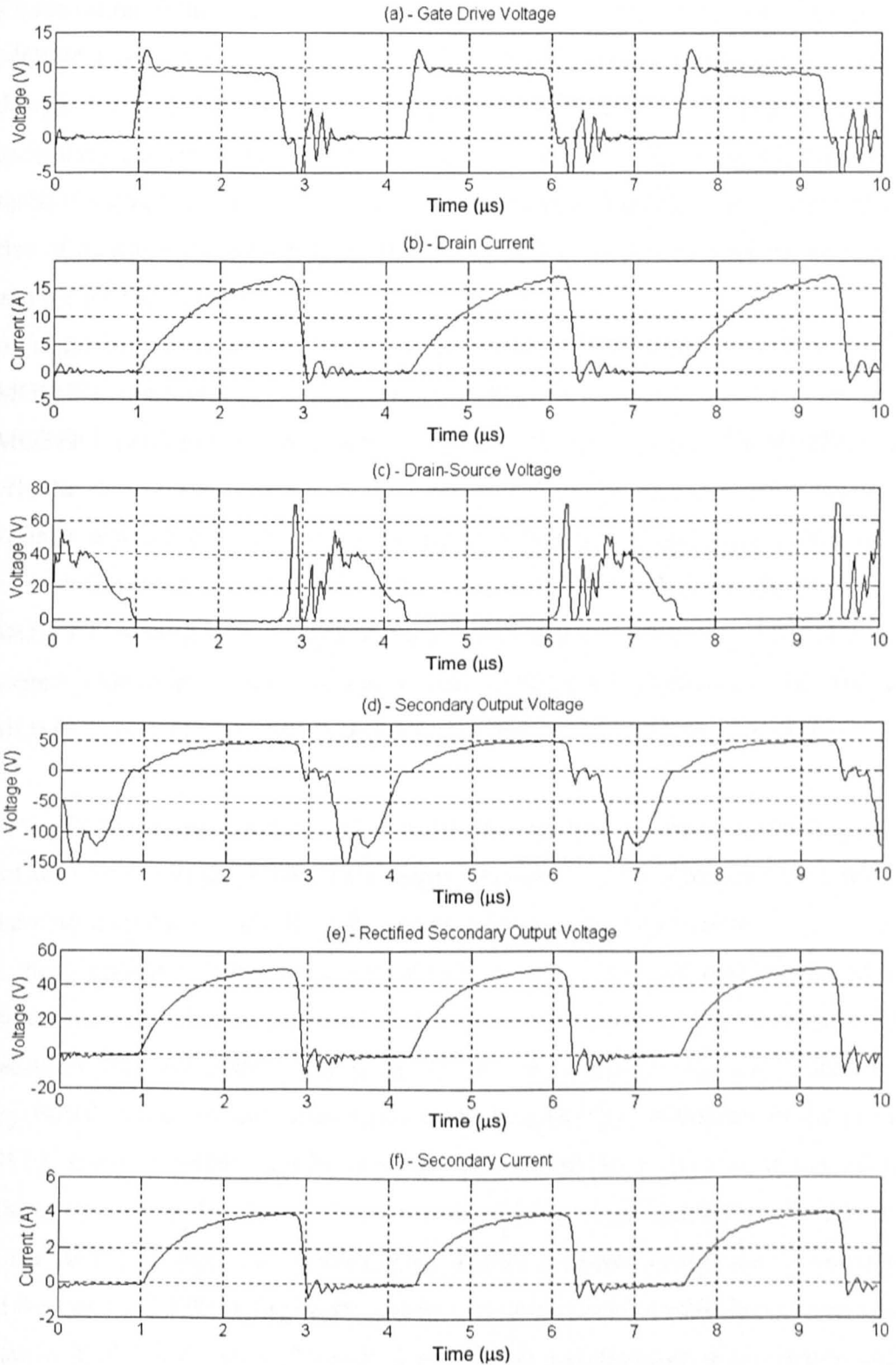


Figure 5.8 - Prototype circuit waveforms

Two important considerations become evident from these measured waveforms.

1. Examination of the load resistor voltage, Figure 5.8(e), shows that when the primary MOSFET is switched on, the actual output voltage rises exponentially towards the designed 48V level rather than giving the desired square-wave pulses. Since the secondary current waveform, Figure 5.8(f), is very similar in profile to the load resistor voltage, it can be assumed as ideal resistor. Therefore, the relatively slow rise of output voltage must be attributed to parasitic inductances of the transformer and the primary side circuit.
2. A further indication of which parasitic elements are dominant can be obtained if the MOSFET drain-source voltage, Figure 5.8(c), is examined at the point of the MOSFET switching off. With ideal operation, Figure 5.7, when the MOSFET turns off, the drain-source voltage should rise to approximately three times the supply voltage at which point the core demagnetisation occurs. From the measured results, it is evident that the behaviour in this case is far from ideal. At the point of the MOSFET turning off, a large voltage spike appears across the MOSFET drain source. This spike is large enough to cause avalanche breakdown of the 60V rated MOSFET, resulting in additional power loss and potential device destruction.

Both the effects described above can be attributed to parasitic inductance on the primary side of the circuit and any referred secondary inductance. Any inductance in series with the main primary current will limit the rate of change of primary current.

From the exponential shape of the output voltage across the load resistor, the primary parasitic inductance can be estimated. With a 1:4 turns ratio of the transformer taken into account, the total primary side parasitic inductance was estimated at 250nH. If the energy stored in this parasitic inductance were dissipated by breakdown of the primary MOSFET every switching cycle, it would amount to 10W of loss at the 300kHz switching frequency. For the 100W converter, this is a significant loss. Furthermore, since the energy storage is a function of the square of current and if the converter was run at the desired 500W rating under similar conditions, the parasitic energy loss would amount to 260W. This level of loss is unacceptable and therefore minimisation and/or recapture of this energy is essential.

The main sources of parasitic inductance are the self-inductances of the interconnection wires and the transformer leakage inductance. Figure 5.9 indicates elements that contribute to the total primary parasitic inductance.

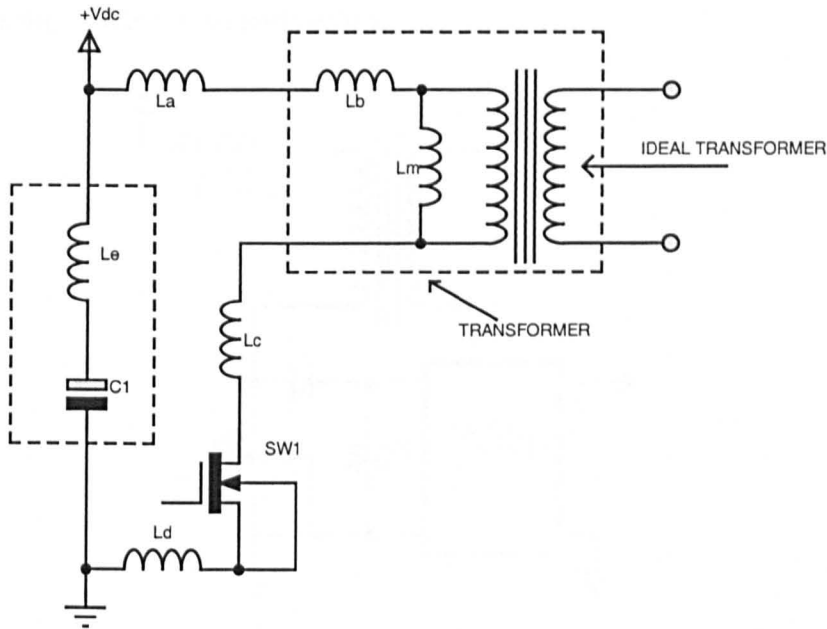


Figure 5.9 - Primary current path with parasitic inductances

In the figure, L_a represents the inductance of the connection wire from the decoupling capacitor to the start of the transformer winding, L_b represents the total leakage inductance of the transformer referred to the primary winding, L_c represents the inductance due to the connection wire between the transformer and the drain of the MOSFET, whilst L_d represents the inductance of the connection between the MOSFET source and decoupling capacitor. Finally, L_e is the parasitic inductance of the decoupling capacitor.

L_a , L_c and L_d can be minimised by using as short a length of wire as possible and minimising the loop area of the primary current path. The transformer leakage inductance, L_b , is a function of the transformer geometry and represents the level of coupling between primary and secondary. The inductance of the decoupling capacitance can be reduced using a combination of electrolytic and polypropylene capacitors.

If the layout of the primary side is optimised such that the loop area of the primary path is minimal, then the dominant cause of parasitic inductance is the transformer leakage. The transformer leakage can be minimised through careful design as discussed in section 5.2.2 and recapture of the energy stored in the leakage inductance is then

possible by placing an active snubber across the MOSFET drain-source. The active snubber clamps the peak voltage and returns the energy contained in the leakage inductance to the primary DC link. Figure 5.10 shows the placement of the active snubber and the equivalent primary side circuit under the assumption that leakage inductance is the dominant parasitic effect.

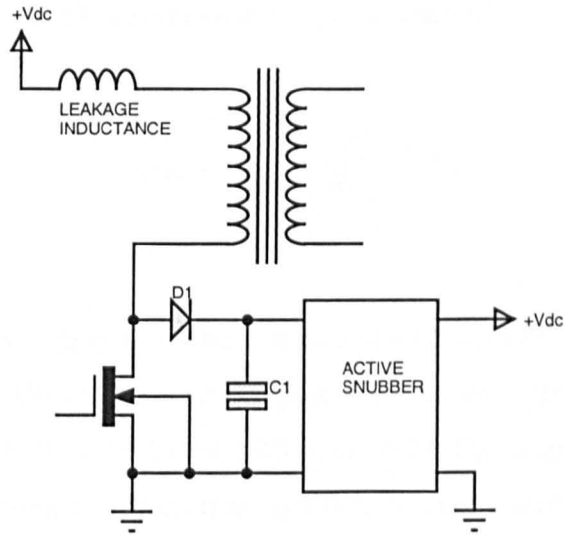


Figure 5.10 - Active snubber placement

When the primary MOSFET switches off, the leakage inductance forces the voltage to rise across the MOSFET. When this voltage equals the clamp level of the snubber diode D1 conducts and the energy stored within the leakage inductance is dumped into capacitor C1 (which must be low impedance type, i.e. polypropylene). The active snubber then ‘bleeds’ the energy away and returns it to the initial 12V DC link. The only drawback of this arrangement is that the diode D1 must be rated such that it can transiently handle the full peak primary current of $\sim 100\text{A}$ and therefore may be expensive.

The use of an active snubber serves a dual role in that it removes the need for a demagnetisation winding since the core can demagnetise by returning energy to the snubber. Furthermore, if the snubber clamp level were set to around 50V (i.e. close to the 60V rating of the device), it would be possible to run the primary side to a duty cycle greater than 50%. In fact, with a 50V clamp level and 12V input voltage, the core will demagnetise three times faster than it magnetises and therefore it should be possible to run the power stage up to 75% duty cycle. Not only will this reduce the power rating of the snubber, since the peak primary current will be lower, it will also increase overall system efficiency due to lower R.M.S. currents in the whole converter.

It is possible to quantify the power rating requirement of the snubber if it is assumed that all the energy stored within the leakage inductance is transferred into the snubber every switching cycle. The power rating requirement is then simply the product of this energy and the switching frequency of the converter. Equation (5.1) gives the snubber power requirement as a function of leakage inductance (L_L), converter power (P_C), duty cycle (δ), DC link voltage (V_{DC}) and switching frequency (F_S).

$$P_{SNUBBER} = \frac{1}{2} L_L \left(\frac{P_C}{\delta V_{DC}} \right)^2 F_S \quad (5.1)$$

For a minimum of 10V supply from the battery and with a 500W converter switching at 300kHz, Figure 5.11 shows the snubber power rating requirement as a function of leakage inductance for duty cycles of 50% and 75%. The impact of high switching frequency and high primary side current results in a large snubber power requirement for even modest leakage inductance levels. In order to make the converter a practical proposition, the snubber power requirement should be as low as possible and the initial design figure will be such that the snubber power is less than 50W (10% of the converter power level). To achieve this, the power transformer should be designed to have a leakage inductance of below 75nH. (See Figure 5.11 for 75% duty cycle)

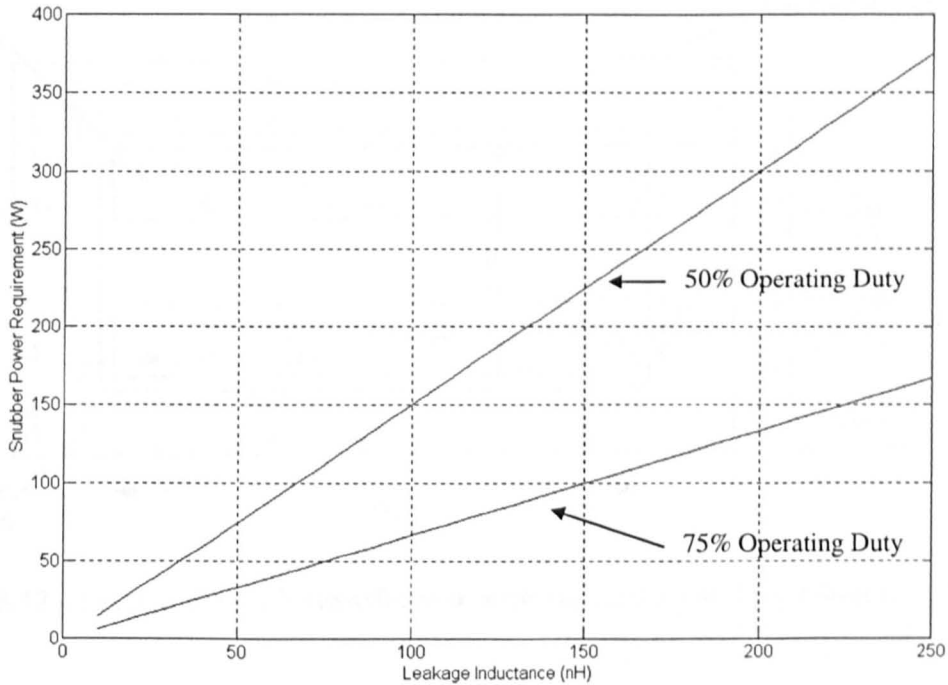


Figure 5.11 - Snubber power requirement as a function of leakage inductance

5.2.2 Transformer Design for Minimum Leakage

In general terms, the closer the primary and secondary windings are to one-another in a transformer, the better the coupling and the lower the leakage inductance. Detailed analyses have been undertaken to understand the causes of transformer leakage inductance [5.3] and the most often used approach is to consider the flux in the transformer under a short-circuited secondary condition. In this situation, the energy stored in the transformer flux can be equated to the energy stored in the leakage inductance. In the case of a general transformer, where windings are wound on top of one another, Snelling [5.4] has estimated the leakage inductance using this method. Figure 5.12 shows a cross-section through a transformer with the secondary winding wound on top of the primary. The left-hand side of Figure 5.12 shows the nature of the flux profile under the short-circuited secondary conditions. The right hand side shows the resulting Magneto-Motive Force (MMF) over the height of the winding. The core is assumed to have a high enough permeability such that the energy stored within it is negligible compared to the energy stored within the windings and the space between them. The following analysis is taken from [5.4].

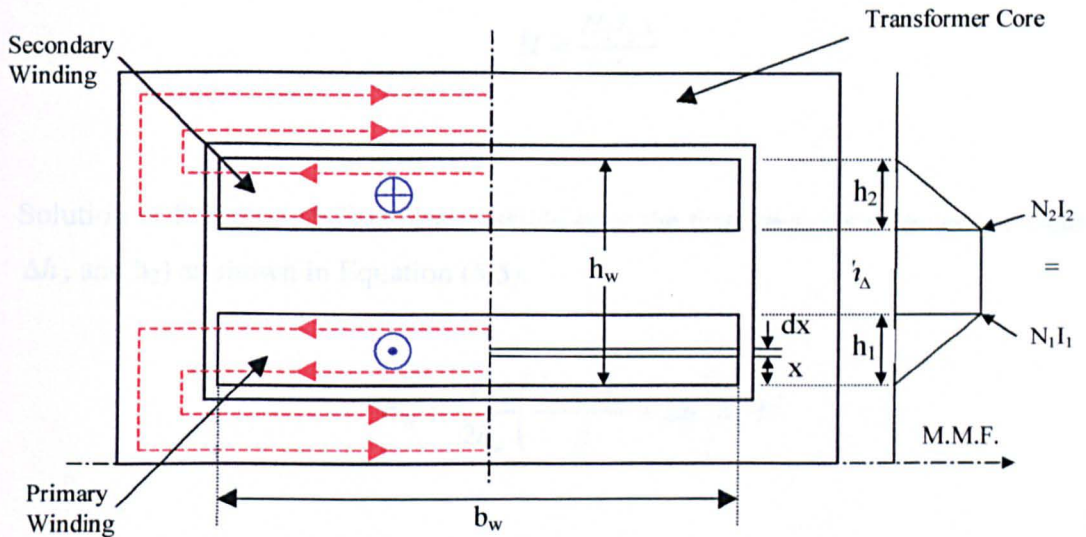


Figure 5.12 - Section through transformer with shorted secondary (Source - [5.4])

The energy stored in the elemental layer, dx , where the magnetic field is of strength H , in a material of relative permeability μ is given by Equation (5.2) where l_w is the depth of the winding and b_w is the width of the winding.

$$E_H = \frac{1}{2} \mu l_w b_w \int H^2 dx \quad (5.2)$$

From Ampere's law the field strength as a function of x can be found using Equation (5.3).

$$\oint H ds = N_1 I_1 \frac{x}{h_1} \quad (5.3)$$

Equation (5.3) assumes a linear change in field strength through the winding as shown in Figure 5.12. Assuming the field strength is constant along the path of the flux within the winding, and the energy stored within the magnetic core is negligible, Equation (5.3) can be rewritten as shown in Equation (5.4).

$$H = \frac{N_1 I_1 x}{h_1 b_w} \quad (5.4)$$

Solution of Equation (5.2) is now possible over the three regions of magnetic field. (h_1 , Δh , and h_2) as shown in Equation (5.5).

$$E_H = \frac{\mu l_w}{2b_w} \left(\frac{h_1 + h_2}{3} + \Delta h \right) N_1^2 I_1^2 \quad (5.5)$$

Equating E_H to the energy stored in an inductor ($\frac{1}{2} LI^2$) yields the leakage inductance as seen by the primary as shown in Equation (5.6).

$$L_P = \frac{\mu l_w N_1^2}{b_w} \left(\frac{h_1 + h_2}{3} + \Delta h \right) \quad (5.6)$$

Equation (5.6) suggests that a transformer geometry that has broad, flat windings (i.e. l_w small and b_w large) will result in the lowest leakage inductance. Physically close windings will also result in a small Δh .

Of the transformer geometry's shown in Figure 5.13(a-d), the planar topology of type (a) most closely matches these requirements. The physical separation between windings of this geometry can be made very small and this type of transformer is likely to offer the lowest leakage inductance. This is confirmed in [5.5].

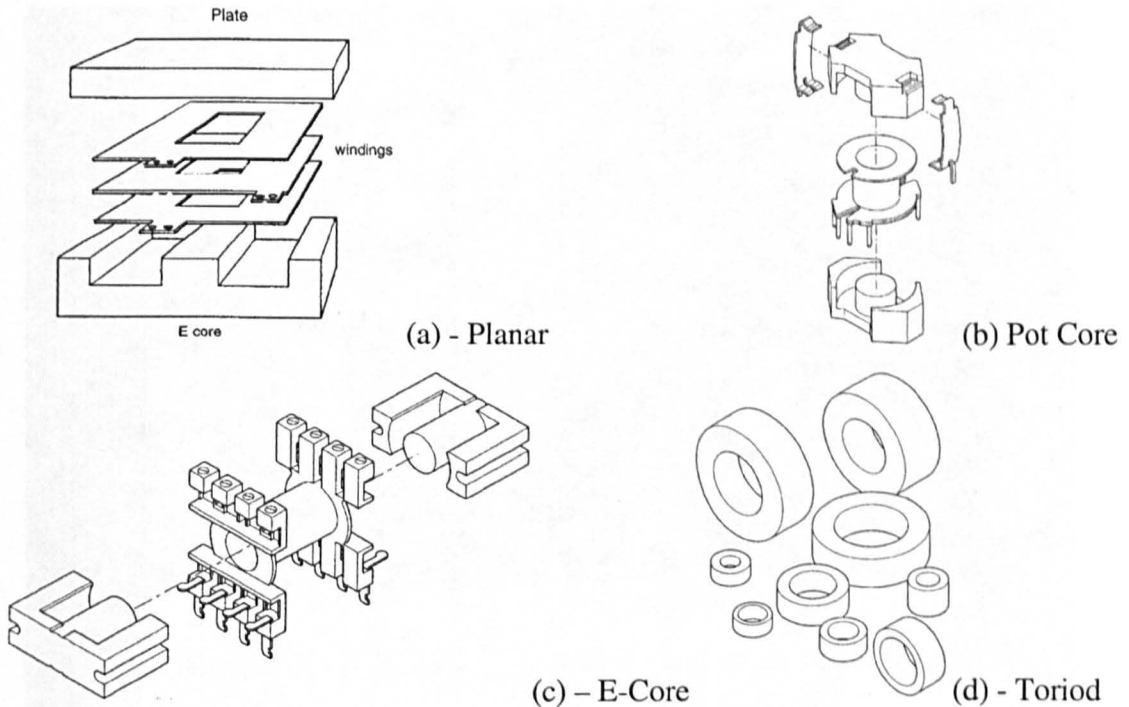


Figure 5.13 - Common transformer geometry's

If the planar type core is used then it becomes possible to fabricate the transformer windings on a PCB. This has a number of benefits: -

- The transformer fabrication is straightforward since the only step after PCB etching would be to cut holes in the PCB and fix the core in place. This simple construction will lead to reduced manufacturing costs.
- Since the windings are precisely located on the PCB, the leakage inductance will be very similar over a batch of transformers, thus ensuring minimal variation in the design parameters of the circuit.
- With the transformer being integrated into the converter PCB, the full layout of the primary side can be optimised to reduce loop areas since connection wires from the PCB to the transformer can be fabricated on the PCB.

In order to assess the possible reduction in leakage inductance to be had, a prototype planar transformer was constructed. The transformer was designed for 300kHz operation with a turns ratio of 1:4. The windings were formed on a PCB as shown in Figure 5.14. The top plate of the planar transformer has been removed to show the secondary winding more clearly. The primary winding is on the other side of the PCB.

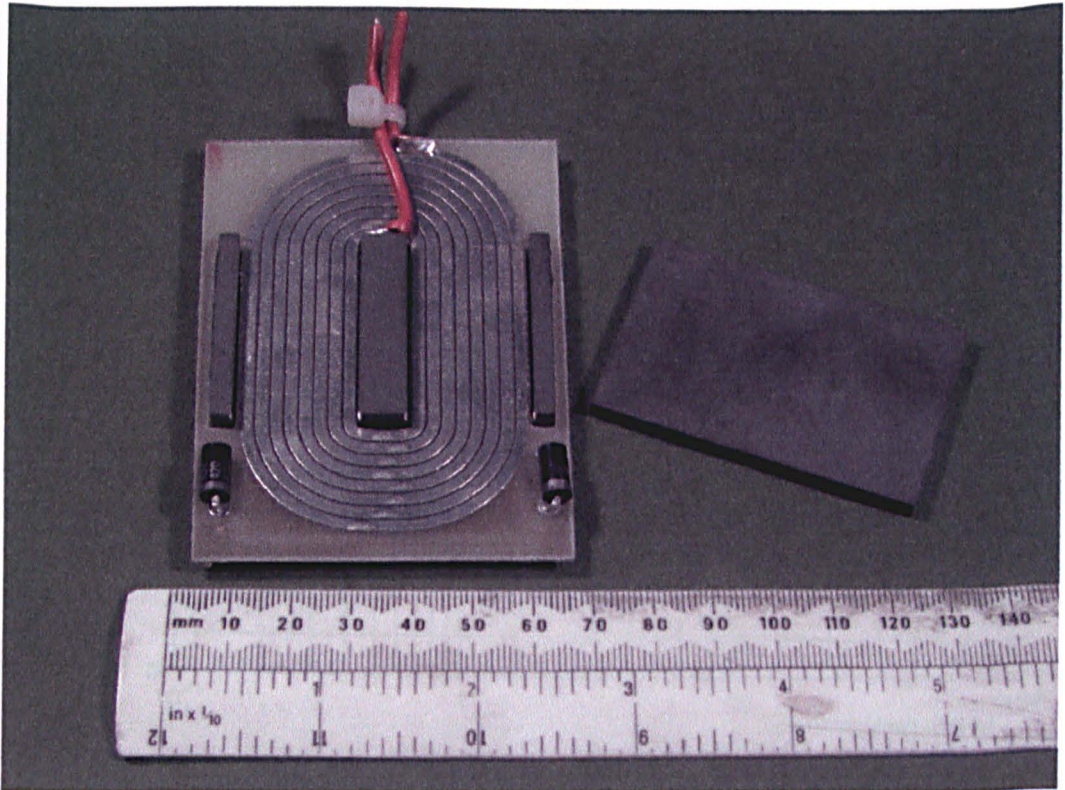


Figure 5.14 - Planar transformer construction

The core chosen was of a standard ferrite grade (3C8) and designed to operate at a peak flux density of 100mT, which is approximately one quarter the saturation flux density of the ferrite material used. Thus the core is presently oversized and will be optimised later. The transformer was tested in the circuit used in Figure 5.5 and from an analysis of the secondary induced voltage, the total primary side leakage was estimated to be 180nH which is a 30% reduction over the original E-Core design. Improved layout of the secondary and primary circuitry would be expected to reduce this value further.

5.2.2.1 Optimisation of Core Material and Size

At the high switching frequency required by the power stage, ferrite core materials currently offer the lowest loss per unit volume for a given transformer size. The measure of a ferrite material performance can be attained using a performance factor [5.2], which gives a measure of the power throughput that a core can handle at a certain core loss. Figure 5.15 shows a typical performance factor graph based on the range of ferrite material grades available from a particular manufacturer. The graph gives the maximum peak flux density and operating frequency for a specific core loss density.

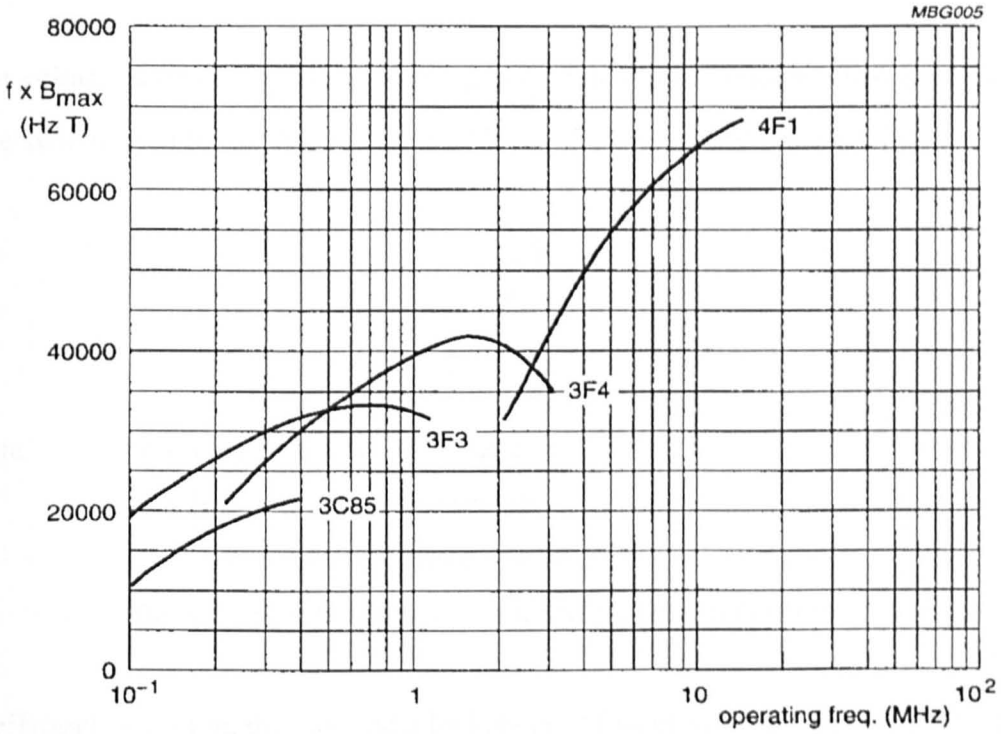


Figure 5.15 - Performance factor of ferrite materials (Source – [5.2])

Since the power transformer is to be operated at around 300kHz, Figure 5.15 shows that the choice of material grade is between 3C85 or 3F3. Of the two, the 3F3 material offers the highest performance factor and will lead to a smaller power transformer for a given power rating and core loss. By minimising the size of the power transformer, the parasitic elements are also minimised. The B-H loop and specific power loss graphs for 3F3 material are shown in Figure 5.16(a) and Figure 5.16(b) respectively.

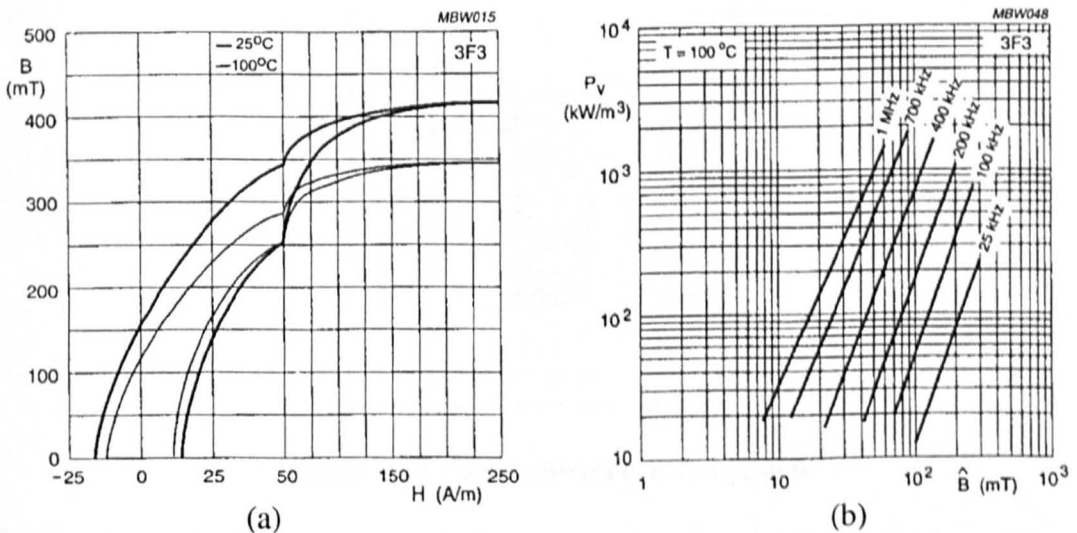


Figure 5.16 - B-H loop and specific core loss graphs for 3F3 ferrite

(Source – [5.2])

If the voltage across the primary winding is assumed to be constant during the on time of the switch, then the change in core flux level, \hat{B} , is given by Equation (5.7).

$$\hat{B} = \frac{V_{DC} T_{ON}}{N_P A_C} \quad (5.7)$$

Where, V_{DC} is the primary DC voltage
 T_{ON} is the on time of the switch
 N_P is the number of primary turns
 A_C is the effective area of the magnetic path in the core

For efficient operation, the core must be kept out of saturation and from Figure 5.16(a), a peak working flux density of 200mT is well away from the knee of the B-H curve. For worst case conditions of $V_{dc}=15V$ and $T_{ON}=2.5\mu s$ equivalent to 75% duty at 300kHz, then the minimum turns-area product is $188mm^2$.

The maximum number of primary turns will be dictated by the available winding breadth, the maximum RMS primary current and the allowable temperature rise of the PCB copper. Figure 5.17 illustrates the winding breadth available for the planar transformer.

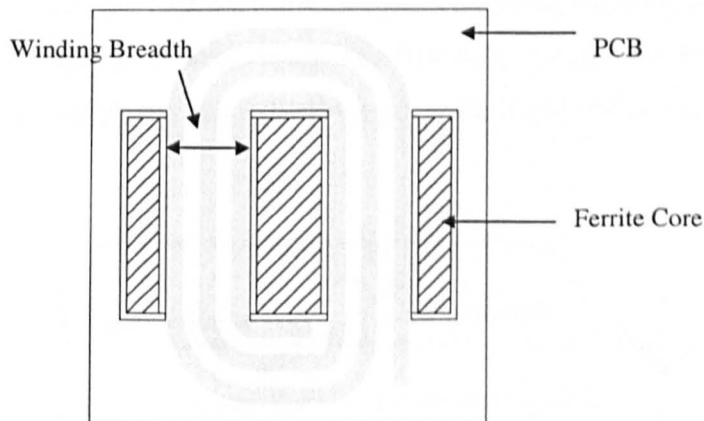


Figure 5.17 - Transformer arrangement

The maximum RMS current, which the primary winding has to support, is given by Equation (5.8).

$$I_{RMS} = \frac{P_C}{V_{DC} \sqrt{\delta}}$$

(5.8)

Where, P_C is the required power rating
 V_{DC} is the main primary DC supply voltage
 δ is the operating duty cycle of the converter

For a 500W converter with a worst case input voltage of 10V and a duty cycle of 50%, Equation (5.8) indicates a peak R.M.S. current of 70A. The maximum current which the PCB transformer winding can carry is a function of the cross-sectional area of the PCB track, the allowable temperature rise of the track above ambient and the ability of the track to dissipate power to the ambient conditions. Since a PCB track is very flat and thin it will have a high surface area to cross-sectional area ratio; hence it will have a good heat dissipation capability and it is possible to run the PCB tracks at very much higher current densities than the 3-5A/mm² typically used for circular cross-section conductors.

In order to assess the current capability of the PCB, an experiment was undertaken to measure the temperature rise of a PCB track for a range of different currents. The experiment was carried out for both 1oz and 2oz PCB, which corresponds to a copper thickness of 0.035mm and 0.070mm respectively. Measurements were taken for both tinned and untinned 1oz and 2oz board but the increase in current carrying capability of the tinned boards was found negligible. Thus, the following results are based on the untinned boards. The measurements were based on a 'standard test' PCB track as shown in Figure 5.18 below.

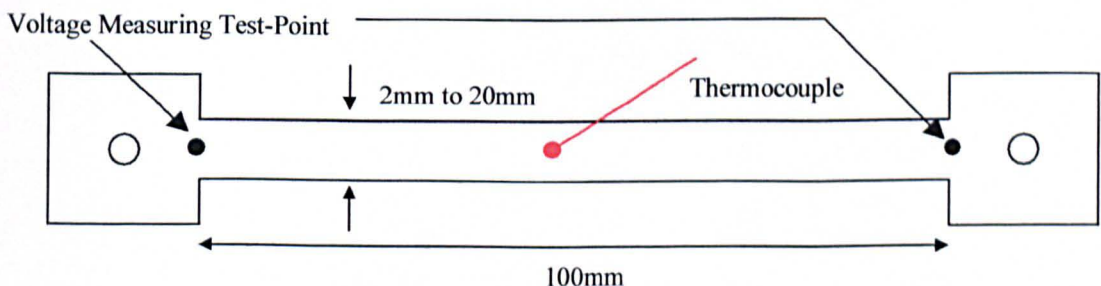


Figure 5.18 - Test PCB track geometry

The track width was varied from 2mm to 20mm in 2mm steps and the temperature measured by a thermocouple in the centre of the track. Each track was subjected to currents leading to temperatures of up to 120°C and the whole process carried out for 1oz and 2oz board. In addition to the temperature measurement, the voltage drop across the 10cm length of track was recorded to give the track resistance. A DC current was used to ease measurement and although it is recognised that skin effect will increase the effective track resistance at high frequencies, the results from the measurement will give a good indication of temperature rise.

The measured temperature rises above ambient (25°C) for both 1oz and 2oz board are shown in Figure 5.19(a) and (b) respectively. Figure 5.20 gives the measured copper loss per cm of track for the different track widths and board thicknesses. These power loss curves do not follow the expected squared relationship with current due to the effect of track temperature rises increasing the copper resistivity. The results confirm that the PCB tracks can support a high current density. For example, with a temperature rise of 100°C, the 20mm wide track on the 2oz board is supporting a current density of 51A/mm². In comparison, the 20mm wide track on the 1oz board is supporting a slightly higher 65A/mm². This is an order of magnitude increase of the normal design current density for a cylindrical conductor.

For a worst case primary side RMS current of 70A, Figure 5.19 dictates that 2oz PCB board must be used with at least a 20mm wide track. This will lead to a maximum track temperature of 100°C above ambient and a power loss of 1W/cm.

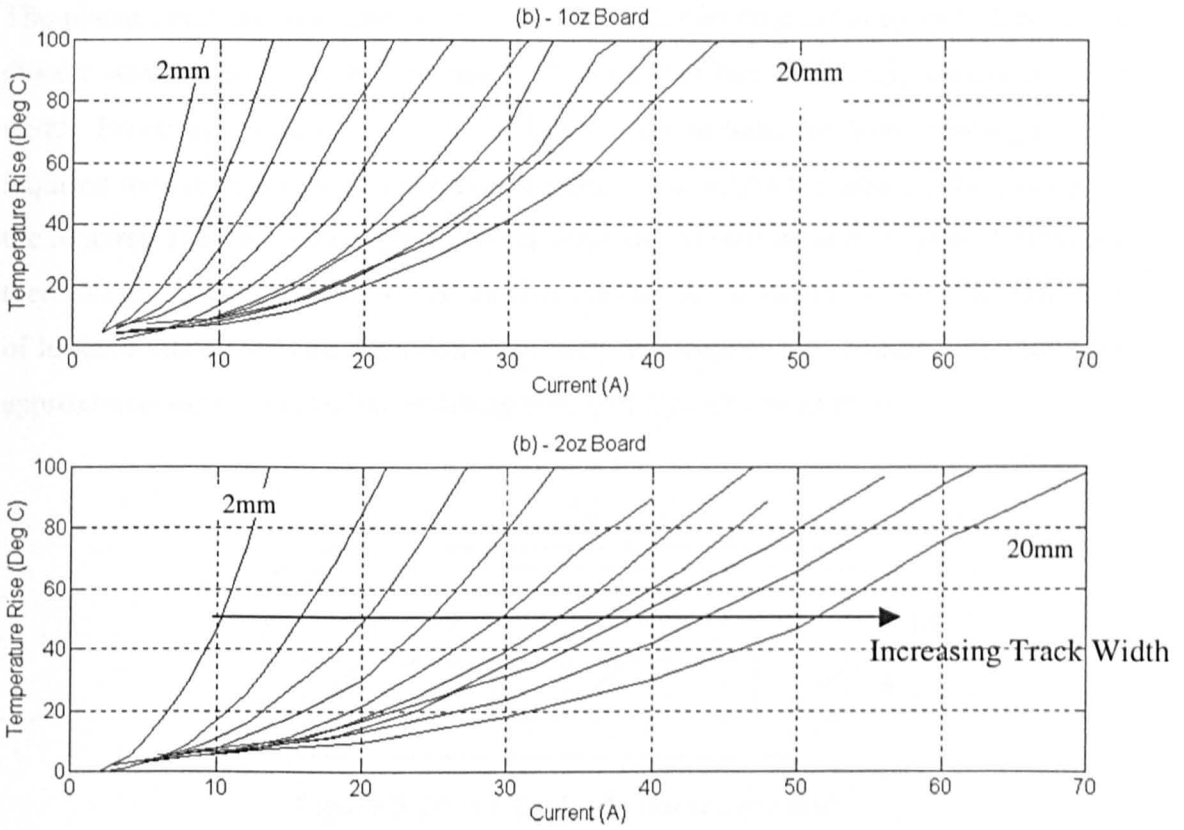


Figure 5.19 - PCB track temperature rises

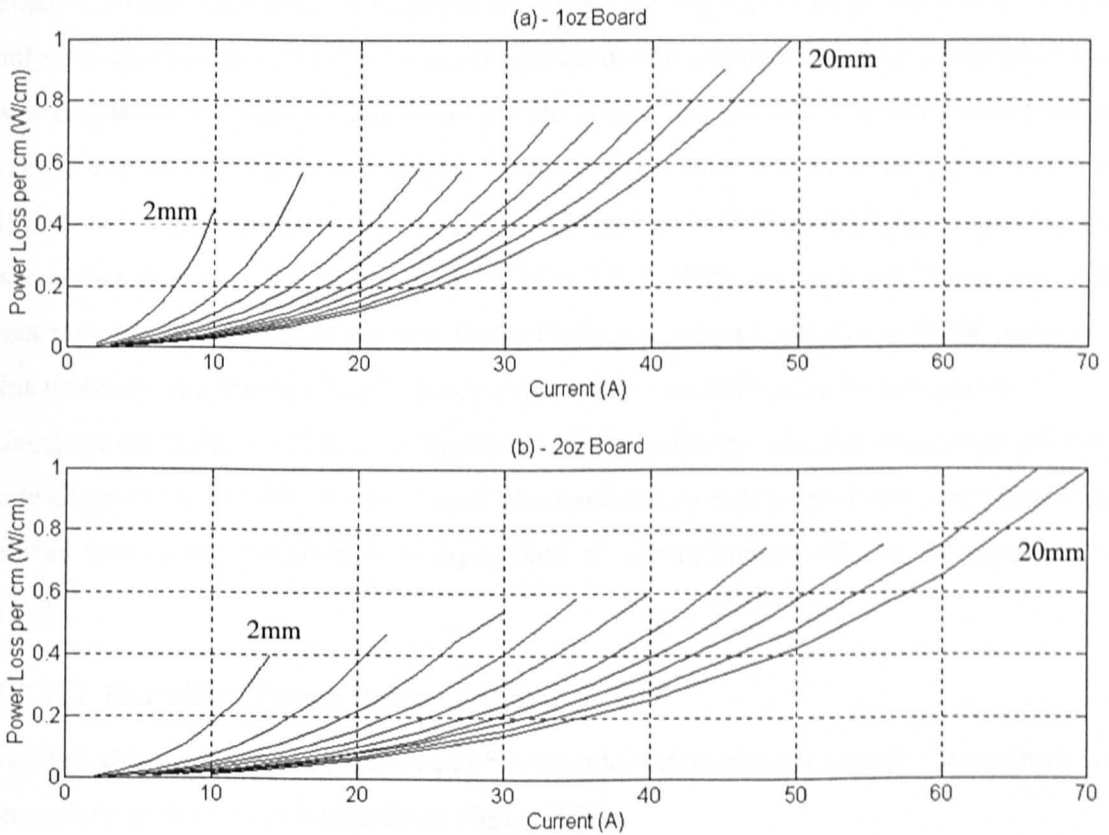


Figure 5.20 - Power loss per cm track length

The planar cores are available in 3F3 material and offer core areas up to 511mm^2 . The closest standard size core has an area of 194mm^2 but has a relatively narrow winding width. However, by cutting one of the larger cores in half, the large winding breadth required for the 20mm wide track can be maintained whilst the area can be reduced to the required 188mm^2 . Although the larger cores would operate at a lower peak flux, and therefore experience lower loss, the smaller the core the better in terms of minimisation of leakage inductance and reduction of primary side copper loss. Figure 5.21 shows the approximate dimensions of the resulting core (All dimensions in mm).

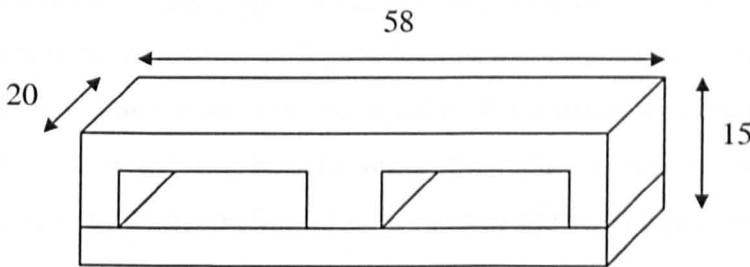


Figure 5.21 - Optimised planar core size

Since a 20mm wide track is required to handle the high level of primary side current, only a single primary turn can be accommodated on a single layer. The centre pole area was measured at 160mm^2 and therefore the single turn results in a turns-area product very close to the required 188mm^2 . The modified core has an effective volume of 13000mm^3 and at the peak flux density of 200mT at 300kHz switching frequency, the worst-case core loss, based on Figure 5.16 is 7.8W. With nominal 12V input, the peak flux reduces to 160mT and the core loss will drop to around 5W. For a 500W converter, this amounts to a 1% loss in efficiency drop which was deemed to be acceptable.

Using an estimate of 120mm for the length of the primary turn, the worst-case primary side copper loss is 12W. With an equivalent secondary side copper loss, the worst-case power loss in the transformer is equivalent to approximately 6% of the total power output.

5.2.2.2 Required Turns Ratio

The transformer turns ratio was found by considering an idealised output pulse from the secondary of the power transformer, Figure 5.22.

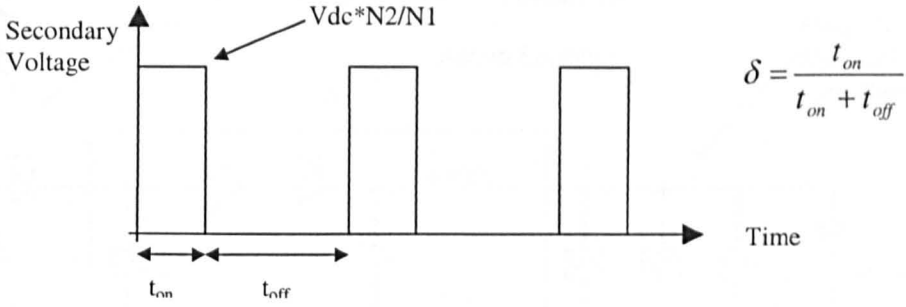


Figure 5.22 - Useful transformer output voltage

The peak fundamental voltage output of the new switching amplifier will be equal to the average of the voltage waveform of Figure 5.22 as a consequence of the action of the output filter. This average level must be equal to the maximum required peak output voltage to ensure full power can be achieved at the reduced available duty cycle. This analysis results in a required transformer turns ratio as shown in Equation (5.9).

$$n = \frac{N_2}{N_1} = \frac{1}{\delta V_{DC}} \sqrt{2P_o R_L} \tag{5.9}$$

- Where, δ is the duty cycle
- V_{DC} =Primary Side DC link
- P_o =Output Power
- R_L =Nominal Load Impedance

At the desired amplifier output of 500W into a 4Ω load at a duty cycle of 75% and a worst case DC link of 10V, the required turns ratio is 1:8.4. This reduces to 1:8 if the maximum duty cycle is allowed to reach 80% and this will be the chosen ratio.

5.2.3 Active Snubber Design

The active snubber can be realised using a simple buck converter circuit as shown in Figure 5.23.

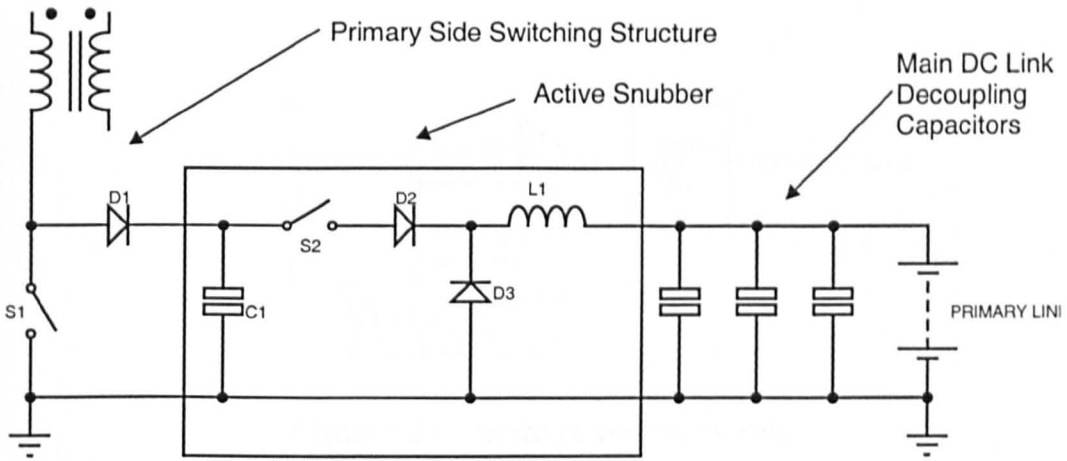


Figure 5.23 - Active snubber implementation

During the off time of the main primary switch, S1, D1 conducts and directs transformer magnetisation energy into capacitor C1, causing the voltage across it to rise. This clamp voltage is compared against a reference level, to control the duty cycle of S2, which is increased to transfer energy from C1, thereby reducing the clamp voltage. The energy is returned directly back to the primary DC link decoupling capacitors. Diode D2 is included to prevent a large impulsive current from charging C1 via the primary link at an initial power turn on.

For a continuous current in L₁, the transfer function of the buck converter is as shown in Equation (5.10).

$$\frac{V_{DC}}{V_{CLAMP}} = \delta$$

(5.10)

Thus, the operating duty cycle for a fixed clamp level is dependent on the initial DC link voltage. For a 50V clamp level and 12V nominal link voltage, the required operating duty cycle will be 24%. It is not possible to simply run the snubber at constant duty cycle due to the variation in the DC supply voltage and the power transfer dependent effects of loss in the snubber components. Therefore, the snubber was run under closed loop control to maintain a constant clamp voltage and this was achieved using the simple control circuit shown in Figure 5.24.

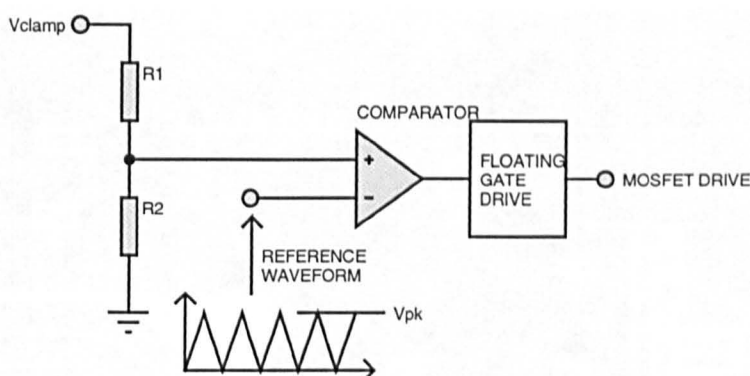


Figure 5.24 - Snubber control circuit

In order to test the snubber a prototype was constructed. The prototype snubber circuit was designed to operate from a separate clock from the main power stage in order that its action would be fully independent. The clock frequency of the snubber was set to 50kHz to ensure efficient operation. Since the exact level of regenerative power is unknown, the semiconductors in the snubber were rated to accommodate a maximum power transfer of 200W. Although this gives a snubber that is likely to be over-rated, the circuit can be optimised at a later stage.

The snubber was initially tested using a power supply under current control to drive power into the snubber capacitor for several different voltage clamp levels, with the output of the snubber connected to a large 12V lead-acid battery. At up to 200W, the snubber maintained an efficiency of above 90% and in the expected operating region of 50W demonstrated an efficiency of above 93%.

5.2.4 Full Primary Circuit Utilising a Planar Transformer

Figure 5.25 shows the lower and upper PCB layouts of the final primary converter circuit. The right hand side of the layout contains the 200W rated active snubber and its control and drive circuitry. The middle section of the board consists of the 12V supply connections and a bank of four decoupling capacitors. The left-hand side of the board consists of the power transformer and primary switch, the latter being formed from three parallel power MOSFETs.

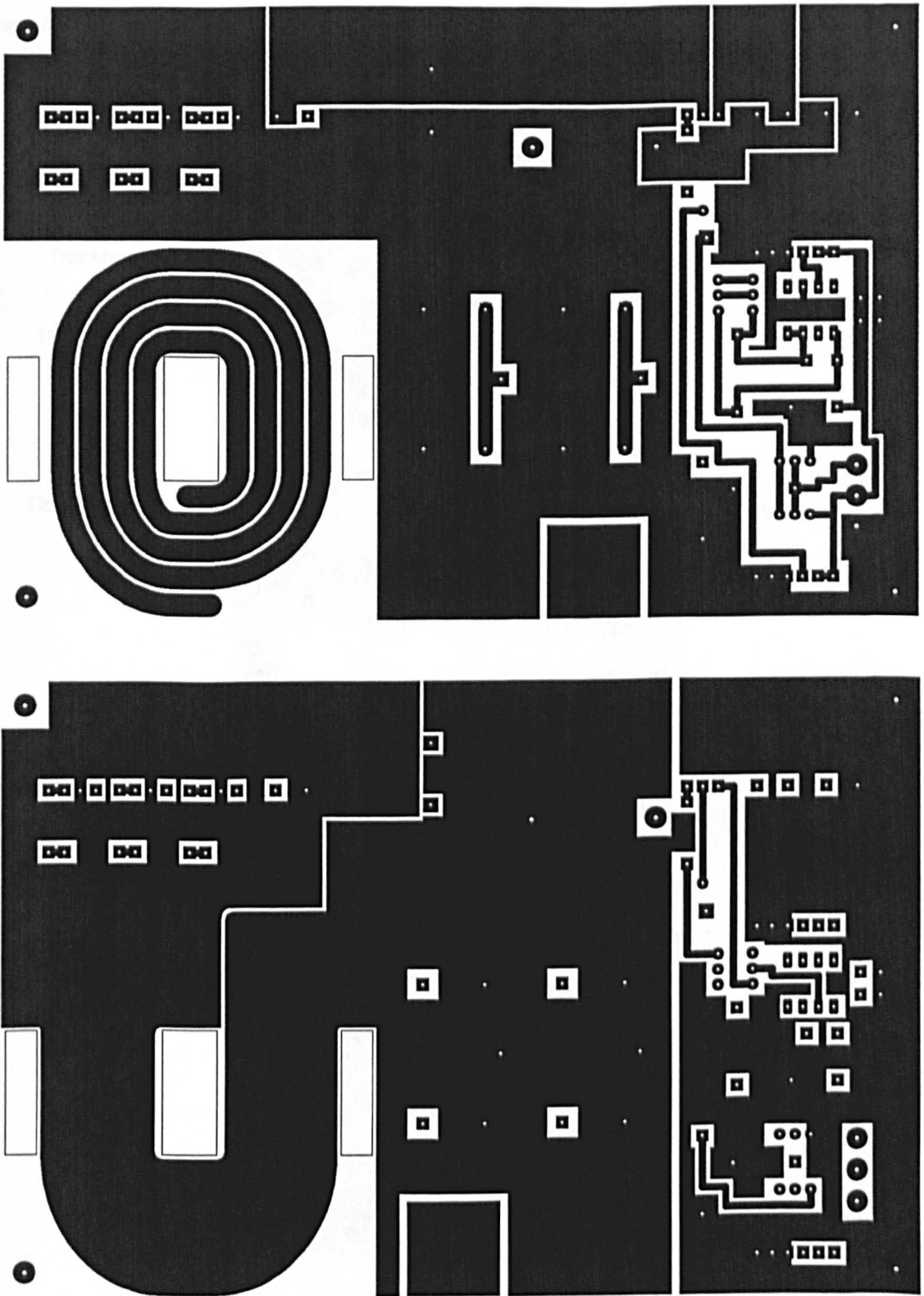


Figure 5.25 - Primary side power stage layout

The single primary turn can be seen on the upper PCB layer whilst the corresponding lower PCB layer supports half of the interleaved secondary winding. The other half of

the winding was realised with another PCB placed above the upper PCB layer. Figure 5.26 shows the fully constructed prototype primary side circuit.

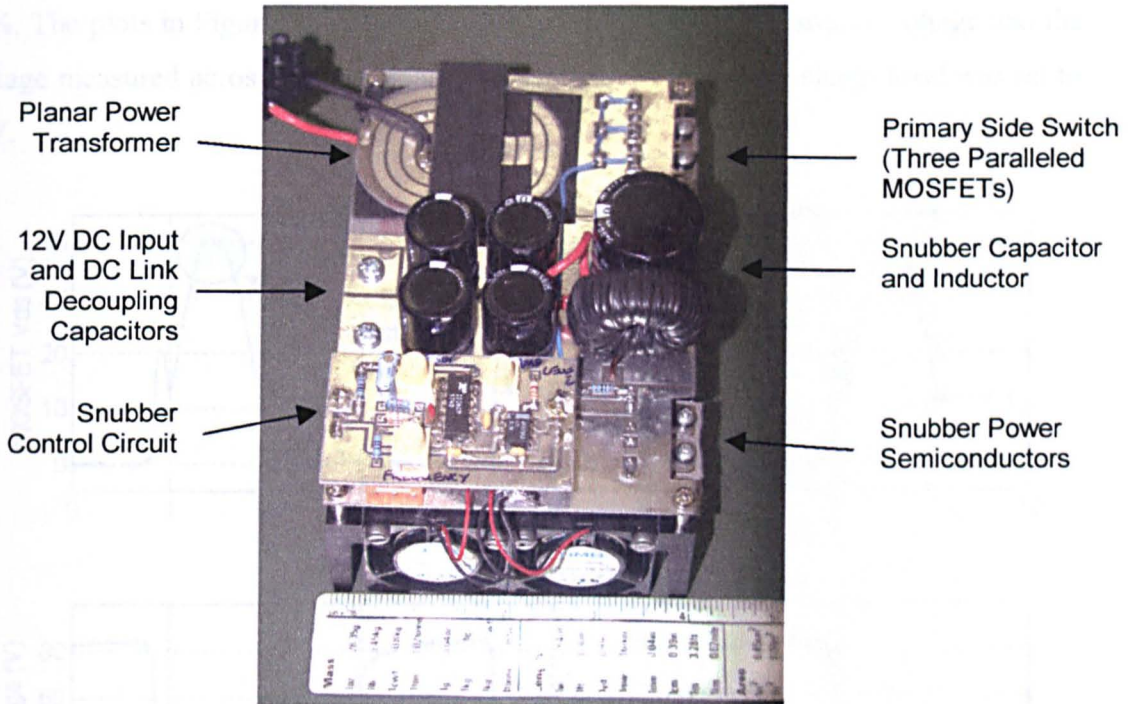


Figure 5.26 - Prototype primary power stage

The power transformer construction is shown more clearly in Figure 5.27 with the interleaved secondary winding in the forefront of the picture.

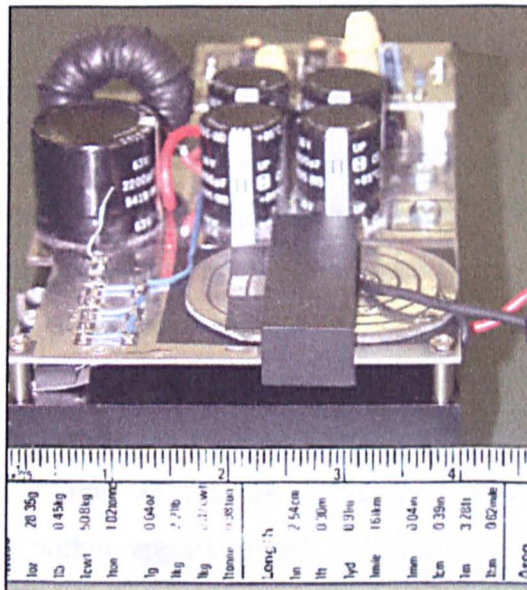


Figure 5.27 - Primary power stage detailing power transformer

As before, the circuit was initially tested with a low inductance resistive load connected with a diode across the secondary of the transformer as in Figure 5.5. The power stage was supplied with 12V DC and driven at 300kHz with a duty cycle of approximately 50%. The plots in Figure 5.28 show the primary MOSFET drain-source voltage and the voltage measured across the secondary side resistor. The snubber clamp level was set to 40V.

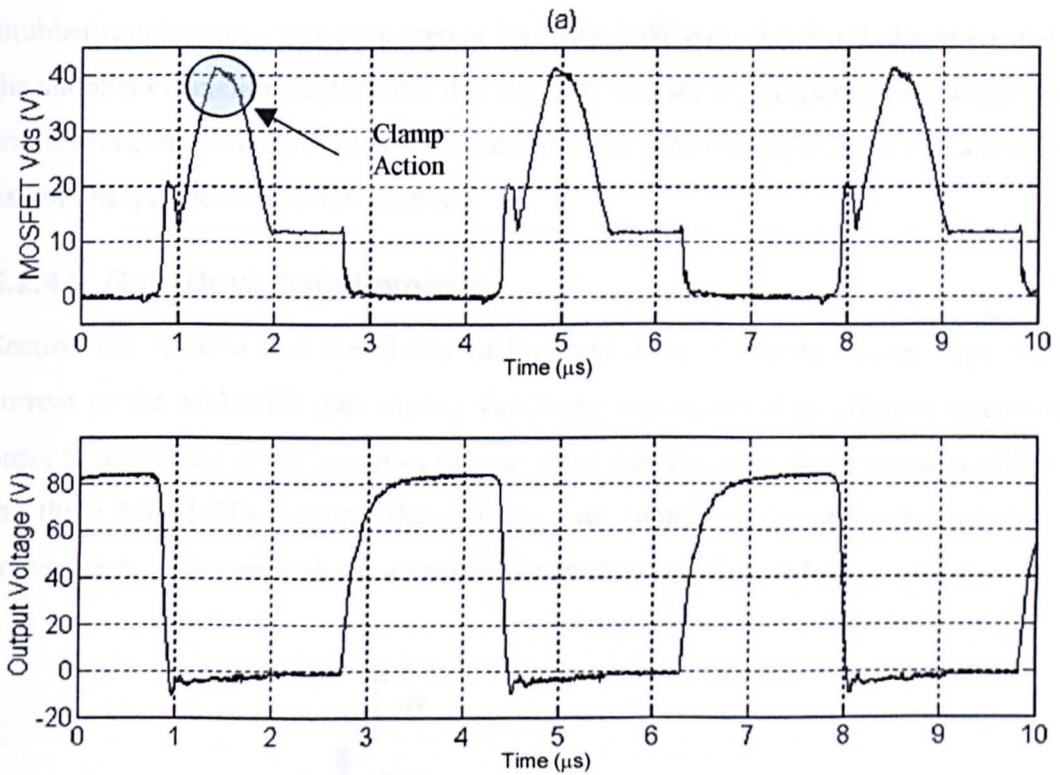


Figure 5.28 - Primary MOSFET Drain-Source voltage and output voltage

Comparison of Figure 5.8 with Figure 5.28 shows that the design effort placed in the minimisation of the primary side parasitic inductance has significantly improved the rise time of the output voltage. Although the output voltage is not ideal, its shape indicates leakage inductance of less than 40nH which is 16% of the value obtained with the initial test circuit and E-core. Secondly, the action of the active snubber has prevented the large voltages appearing across the primary MOSFET switch. The MOSFET drain-source voltage is a lot cleaner as a result of the 40V clamp level. Thus, the core demagnetisation occurs within approximately 1 μs and duty cycles above 50% are possible.

5.2.4.1 In Circuit Snubber Behaviour

In order to quantify the required snubber rating, the power stage was switched at 300kHz with a 50% duty cycle, the load on the secondary varied from 10W to 200W and the current returned by the snubber to the primary link measured. Above 200W, the primary side devices were destroyed and therefore on the final system, lower on-resistance, higher power devices will be needed. Before destruction however, the peak snubber return power was measured at less than 10W over this band of powers and with the snubber efficiency above 90%, this suggests that the actual power requirement of the snubber is considerably lower than expected. This is beneficial since it will allow for the use of cheaper devices in the snubber.

5.2.4.2 Gate Drive Requirements

Section 4.3 showed that the ability of the gate drive circuit to deliver high transient current to the MOSFET gate during switching was essential to efficient operation. In order to assess the relative impact of gate drive capability on new converter efficiency, the three MOSFETs forming the primary side switch in the prototype primary side converter were driven with the arrangement as shown in Figure 5.29.

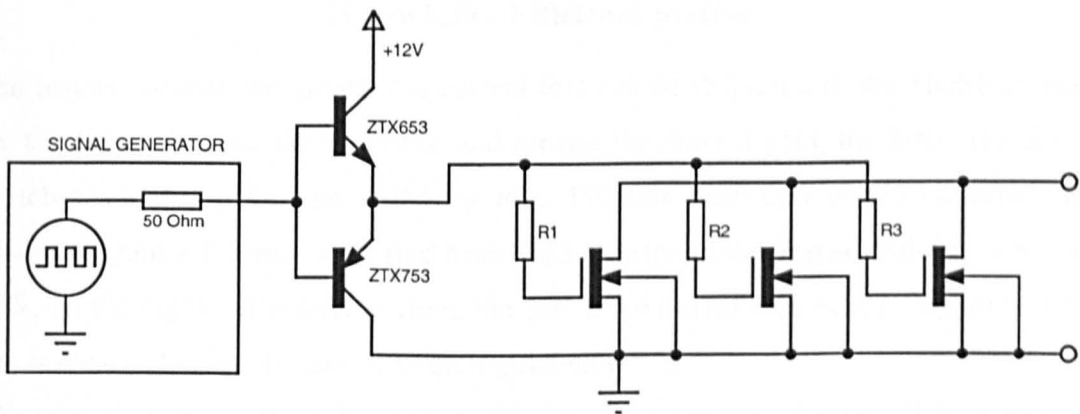
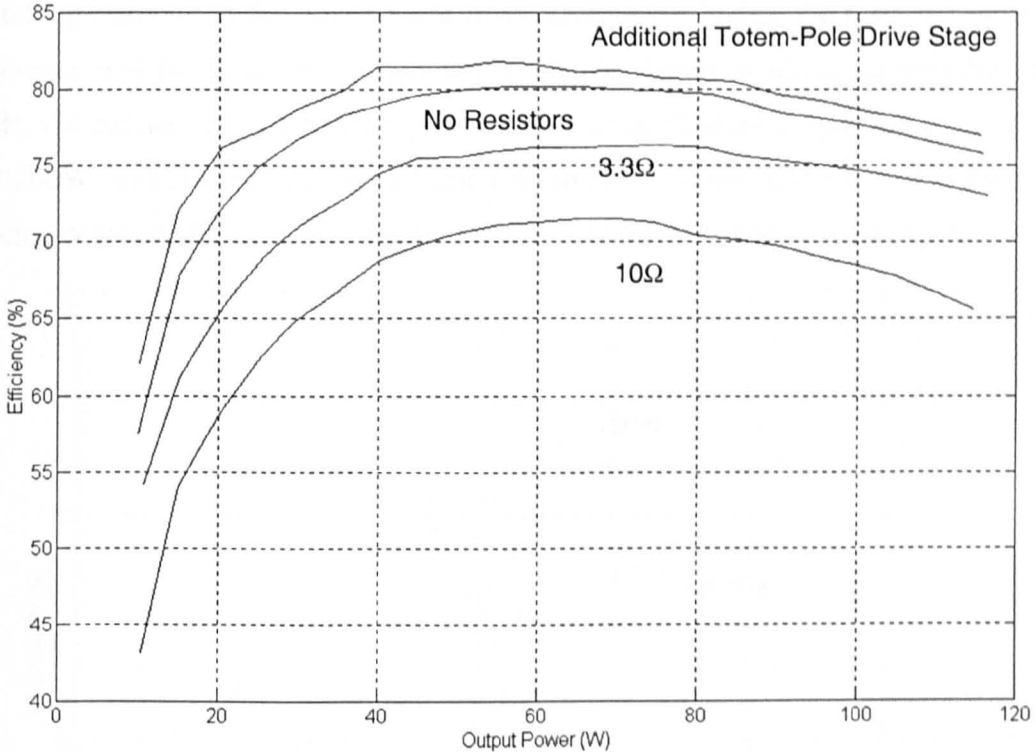


Figure 5.29 - Gate drive circuit

The efficiency of the power converter was measured under four different gate drive arrangements: -

- R1 to R3 as 10 Ω resistors
- R1 to R3 as 3.3 Ω resistors
- R1 to R3 replaced by wire links.
- R1 to R3 as wire links and another totem-pole stage cascaded to give additional current gain.

The graph in Figure 5.30 shows the efficiency profile as a function of output power for the prototype system for the four different gate drive arrangements.



12V DC Supply, 300kHz Switching Frequency, 50% Duty Cycle

Figure 5.30 – Efficiency profiles

The results indicate the greater the current that can be delivered to the MOSFET gate, i.e. the lower the gate drive resistor and greater the current gain, the faster the device switches and the lower the switching loss. For this particular power converter, the efficiency gain achieved by moving from 10Ω resistors to having no resistors is around 10%. At the higher gate drive current, the gate drive circuit experienced higher loss but this is outweighed by the gain in overall efficiency.

The overall shape of the efficiency profiles remains similar between all four plots of Figure 5.30. Since the transformer core loss is independent of output power, it dominates the efficiency plot at low power output. As the output power level rises, the core loss relative to the output power falls and the efficiency rises. As the power level continues to rise, I^2R loss begins to dominate and the efficiency begins to fall, peak efficiency occurring when the core loss is approximately equal to the copper loss.

5.2.4.3 Effect of Duty Cycle

As discussed in section 5.2.1, the higher the operating duty cycle, the lower the peak switching currents in the power stage and therefore the higher the overall conversion efficiency will be. In order to examine the relative benefit of increased operating duty cycle, the primary circuit efficiency was measured at constant output powers of 100W and 200W for duty cycles ranging from 15% to 50%. Figure 5.31 shows the measured efficiency profile for these two conditions as a function of the driven duty cycle.

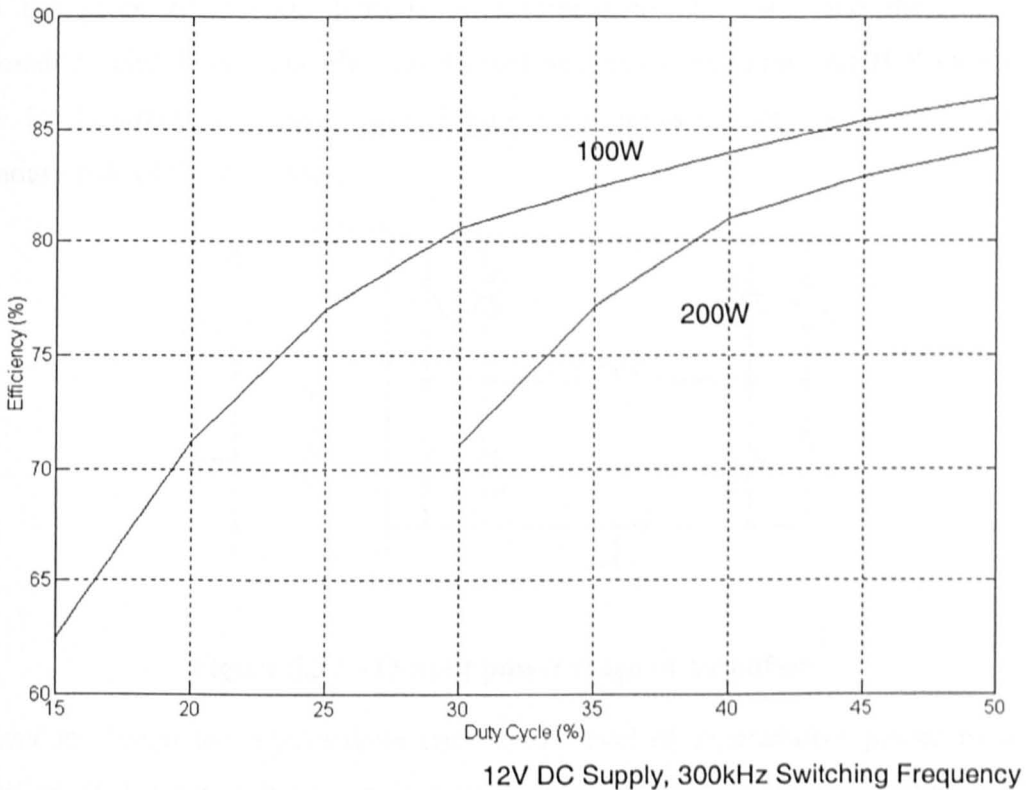


Figure 5.31 - Efficiency vs. operating duty cycle

The efficiency characteristics follow the expected trends of higher duty giving more efficient operation. For this particular converter, a change from 25% to 50% duty cycle results in an efficiency increase of around 10%. Extrapolation of the curves in Figure 5.31 suggests an operating efficiency of greater than 90% at 75% duty cycle operation.

5.3 Secondary Side Structure

The output from the power transformer secondary winding is a series of bipolar voltage pulses. The voltage pulse corresponding to the instant when the primary side device is switched on allows power transfer across the transformer. The amplifier output power stage uses an H-Bridge circuit to convert this pulse train into a series of positive or negative pulses to be fed to the output filter and loudspeaker. Since the transformer

output voltage is bipolar, some intermediate circuitry will be required to ensure that the H-Bridge only receives positive voltage pulses since any negative input voltage will forward bias the bridge diodes. In addition, due to the reactive nature of the load, bi-directional power transfer between the amplifier and load is a requirement of the power stage. In a conventional amplifier, this requirement is satisfied since the large DC supply decoupling capacitors act as a buffer to any energy that regenerates into the DC link.

With the proposed circuit, there is no intermediate DC filter and therefore, the intermediate circuit between the transformer secondary winding and H-Bridge must allow for bi-directional power flow. Figure 5.32 shows the general structure of the secondary side of the converter.

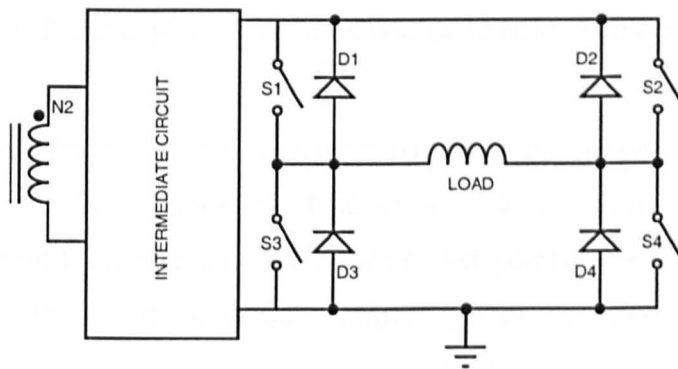


Figure 5.32 – Output power stage of amplifier

In order to design the intermediate circuit, the level of regenerative power must be quantified. If this power level is only a small fraction of the total power output, then it can be simply dissipated with little impact on overall efficiency. Should, however, the return power level be large, a path must be provided for it to be returned to the primary supply.

The ratio between the level of the forward power and return power will depend on the impedance of the load, the switching frequency and the modulation depth of the signal. The impedance of the load is a combination of the impedance of the loudspeaker and the passive power filter. When a multiway loudspeaker is used, the load characteristics are further complicated by the crossover elements and the combination of drive units.

5.3.1 Return Power Level

Consider a general reactive load driven by a sinusoidal voltage source. The product of the instantaneous voltage and current is given in Equation (5.11) and shows the nature of the resulting power flow.

$$P(t) = \frac{\hat{V}^2}{2|Z|} (\cos \varphi - \cos(2\omega t - \varphi)) \quad (5.11)$$

Where, \hat{V} is the peak applied voltage
 $|Z|$ is the magnitude of the load impedance (at ω rad/s)
 φ is the load phase shift in radians (at ω rad/s frequency).

If the load phase shift is non-zero then there will be points when $P(t)$ is negative, i.e. instantaneous power flow is from the load to the voltage source. The overall return power can be found by averaging these return power points over a fundamental cycle. Equation (5.12) gives the result of this integration, and the working can be found in Appendix A.

$$P_{RETURN} = \frac{\hat{V}^2}{2\pi|Z|} (\varphi \cos \varphi - \sin \varphi) \quad (5.12)$$

As would be expected, Equation (5.12) indicates the return power level is maximum and equal to the forward power level when the load is purely reactive. A practical load will have an impedance magnitude and phase shift which are both functions of frequency and therefore, the return power level will be a strong function of signal frequency.

To quantify the likely magnitude of return power, the impedance of the fourth order filter and 4Ω loudspeaker combination used in Chapter 4 was measured. Equation (5.12) was then used to compute the return power level as a function of frequency for a 64V peak driving voltage, specified to deliver 500W into a 4Ω load. Figure 5.33 shows the measured impedance (a), measured phase shift (b) and calculated return power level (c).

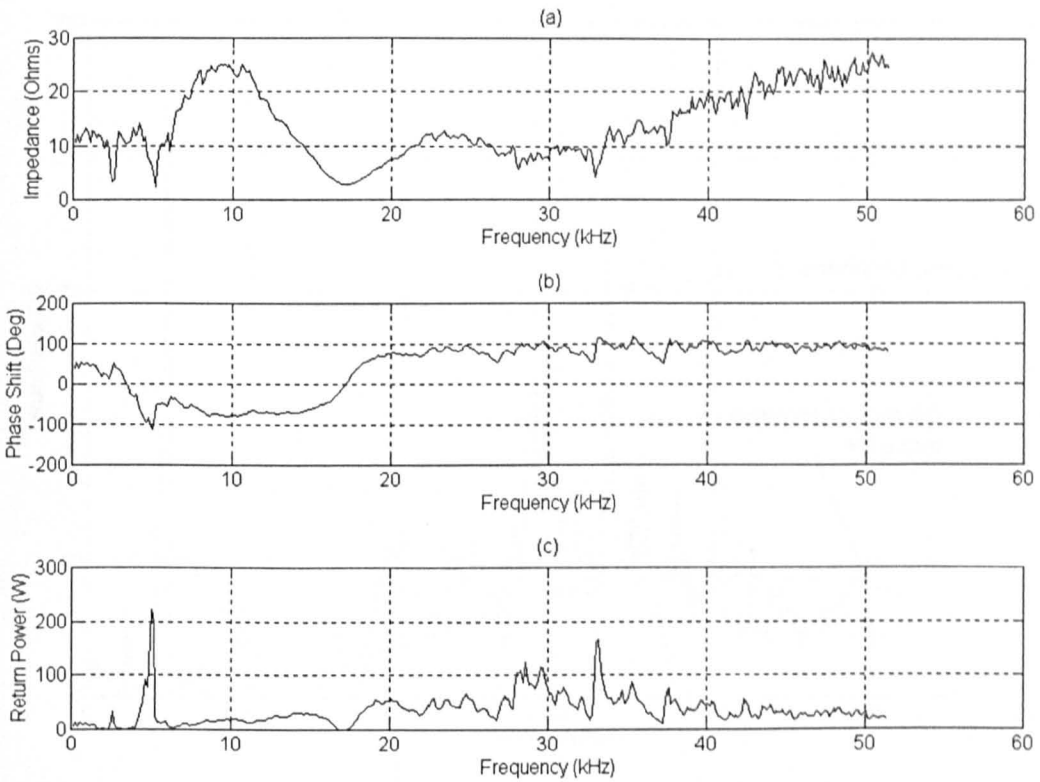


Figure 5.33 - Measured load impedance and calculated return power

The profile of the return power level demonstrates the complex nature of the combined loudspeaker/filter impedance. The calculated return power shows a number of high magnitude peaks and for the purpose of comparison, the return power profile was also calculated for an ideal resistive 4Ω termination of the filter. This is plotted together with that of the actual loudspeaker in Figure 5.34. This figure demonstrates that when a purely resistive 4Ω termination is used, the peaks at 5kHz and 32kHz no longer exist. Figure 5.34 also shows that the underlying profile for the filter/loudspeaker case approximately follows that of the ideal resistive termination. However, with a practical loudspeaker, spikes in the filter/loudspeaker return power profile are observed due to the reactive components in the loudspeaker combining with the filter impedance.

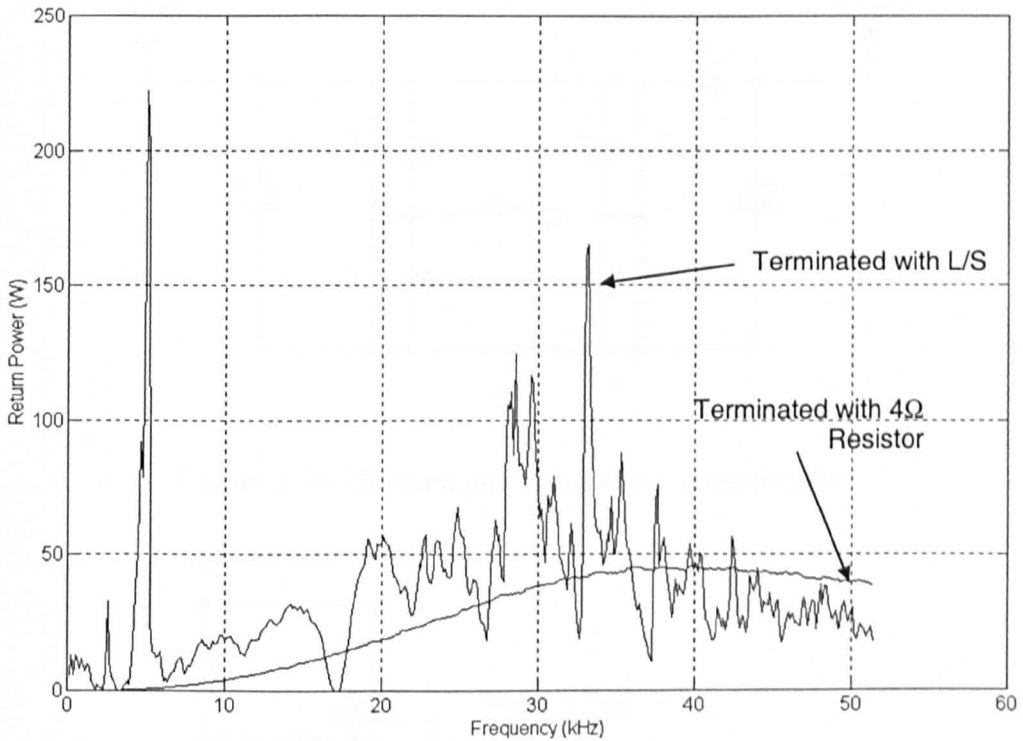


Figure 5.34 - Comparison of return power levels

The actual spectral content of the voltage applied to the filter is not in fact a pure sinusoid but is a function of the modulation strategy, switching frequency, modulation depth and fundamental frequency. For a PWM driven system, the H-Bridge output signal contains the baseband signal, the switching frequency, its harmonics and image spectra about each switching component. Whereas for a PDM strategy, the fundamental baseband frequency is accompanied by the shaped noise floor and switching frequency components. Therefore, the return power level will depend on a number of factors, however it will comprise of two major components: -

can be

1. A component due to the baseband signal, i.e. below 20kHz,
2. A component due to the switching frequency and harmonics.

An empirical approach was used to quantify the return power levels seen in practice. A conventional H-Bridge circuit was modified such that the power drawn by the H-Bridge could be monitored separately from the power it returns. This was achieved using two diodes as shown in Figure 5.35. The return power was clamped using a power transistor operated in its linear region as shown in Figure 5.36.

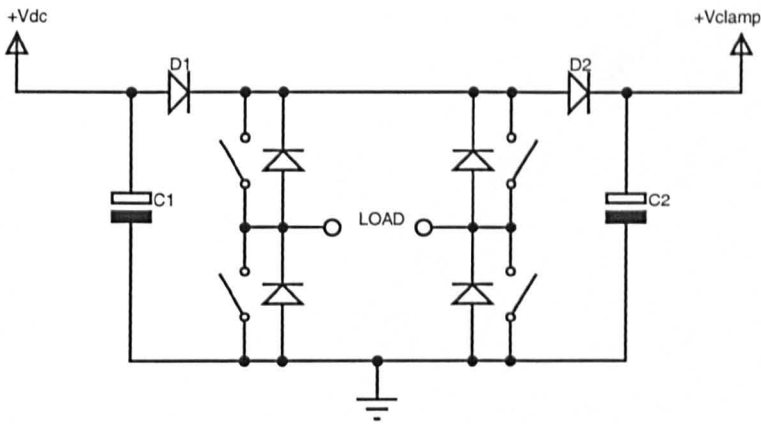


Figure 5.35 - Return power measurement circuit

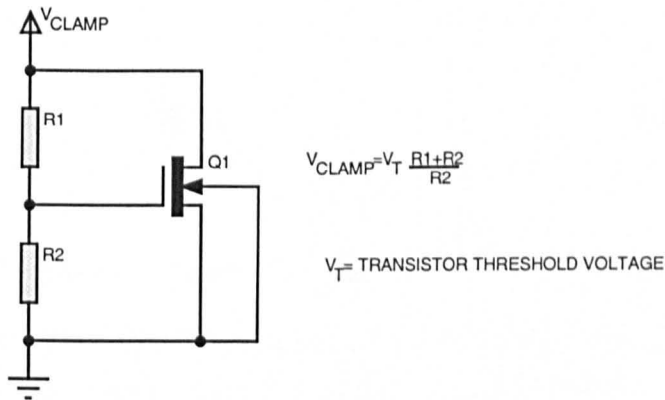


Figure 5.36 - Linear active clamp circuit

The test circuit was switched at 100kHz with a 1μs dead time and operated at 30V DC supply and a clamp voltage of 35V. The load used was the fourth order filter and 4Ω loudspeaker. For a 50% duty cycle, the load current and voltage are as shown in Figure 5.37. The operation of the clamp circuit is evident with the load voltage reaching ±35V during the regenerative period. When power is drawn by the load, the load voltage falls back to the 30V DC supply level.

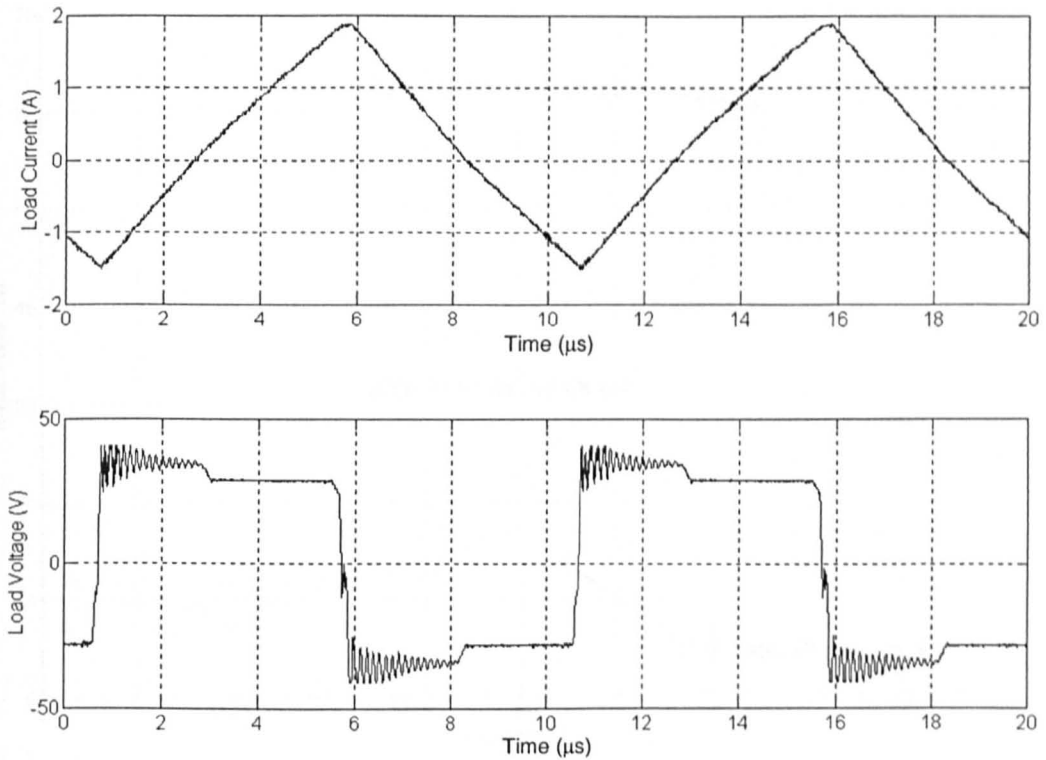


Figure 5.37 - Load current and voltage for power measurement circuit

Initially, the return power was measured as a function of baseband frequency with the circuit switches under PWM control, over the range of 500Hz to 20kHz and for modulation depths of 25%, 50% and 75%. With a nominal 4Ω load, these modulation depths correspond to output power levels of 7W, 28W and 63W respectively. The results of the test are shown in Figure 5.38.

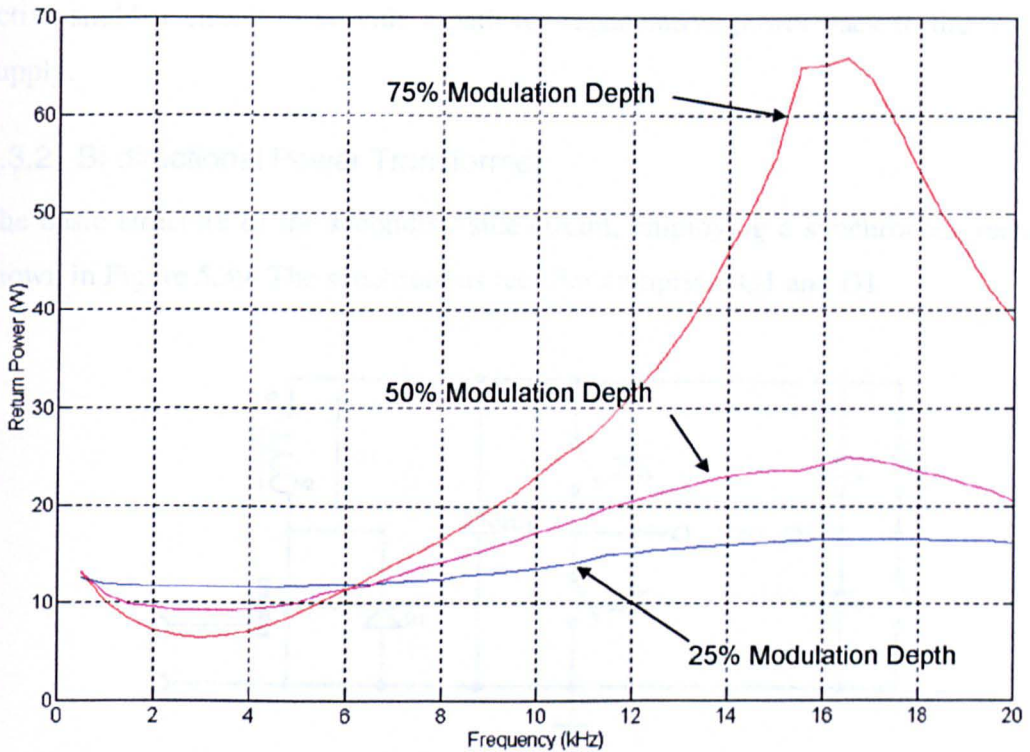


Figure 5.38 - Return power levels as a function of baseband frequency

At 25% modulation depth, the level of return power is relatively independent of frequency and suggests that the switching frequency component of the return power is dominant. As the modulation depth increases, the relative size of baseband return power increases and the dependency of return power on baseband frequency becomes more acute. From the graph, the return power associated with the switching frequency is around 12W whilst the reactive characteristic of the loudspeaker results in a return power exceeding 65W.

The baseband components will dominate the total return power and the peak levels are high relative to the output power. Thus, it is desirable to find a method of recovering the return power and two methods of accomplishing this were investigated: -

1. Allowing bi-directional power transfer across the transformer
2. Use of an active snubber to send power back to the primary

In method 1 it is proposed that the main power transformer is used as a bi-directional power flow path. In this case, simple rectification of the secondary voltage is no longer possible and synchronous rectification must be employed. The second method uses an

active snubber circuit to provide a path for regenerative power back to the initial DC supply.

5.3.2 Bi-directional Power Transformer

The basic structure of the secondary side circuit, employing a synchronous rectifier is shown in Figure 5.39. The synchronous rectifier comprises Q1 and D1.

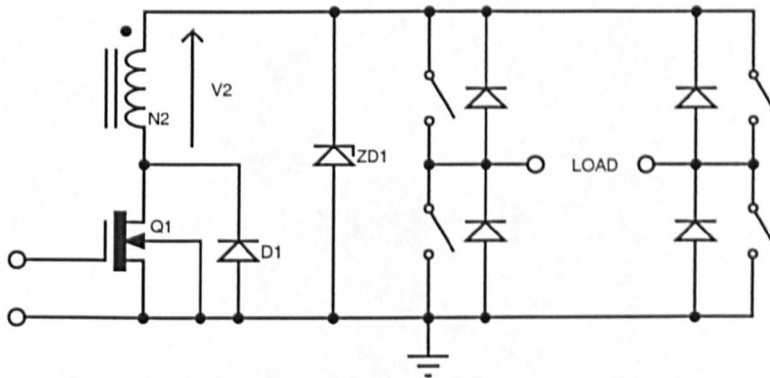


Figure 5.39 - Bi-directional transformer circuit

The operation of this circuit is as follows: -

1. When the primary side circuit switches on, the voltage across the secondary winding, V_2 , rises and Q1 is then switched on.
2. The H-Bridge can now be switched to provide a positive or negative voltage pulse.
3. If power is being delivered to the load, current flows out of N2 and into the H-bridge circuit. If power is being returned by the load, a current flows into N2 and therefore out of the primary winding and into the initial primary DC link.
4. When the primary side device switches off, Q1 is turned off and the H-Bridge is switched into a freewheel state by switching either both upper or both lower devices on.
5. The zener diode is used to protect the output stage from voltage spikes which may occur in the transition times between the primary side turning off and the H-bridge switching into the freewheel state.

Power MOSFETs are the ideal devices for the active switches in this topology since it is a requirement that the switches can conduct current in either direction. A prototype bi-directional power stage was designed to deliver 500W into a 4Ω load, and is shown in Figure 5.40.

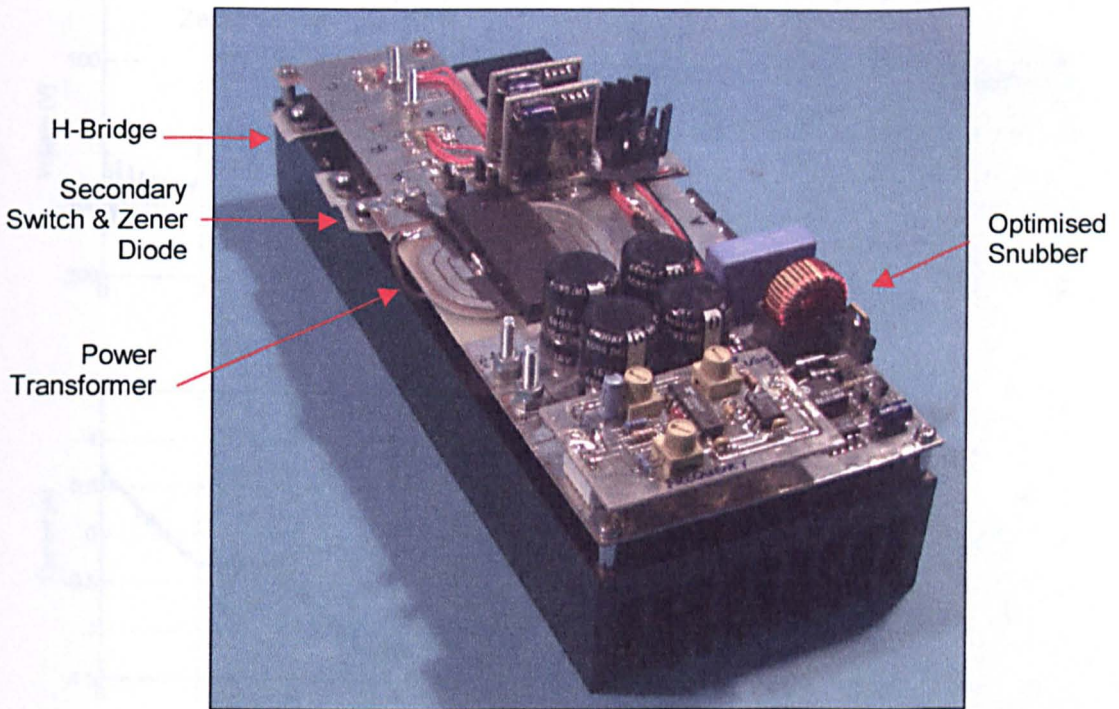
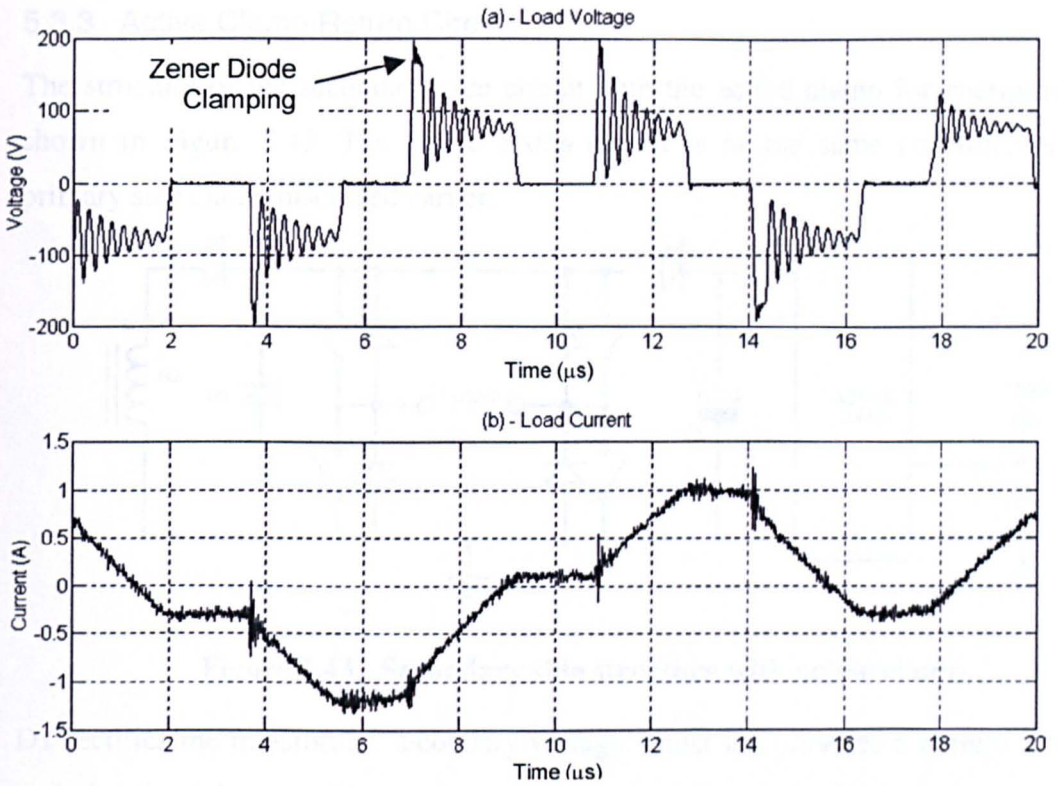


Figure 5.40 - Full power stage with bi-directional power transformer

With this prototype, the primary side snubber design was optimised to a power rating of 50W and the secondary side zener diodes rated at 10W. As an initial test, the H-Bridge output was driven with a PDM strategy, with the zero voltage switching realised through the use of time delays as illustrated in Figure 6.2 in Chapter 6. The H-Bridge output was loaded with the fourth order filter and 4Ω loudspeaker combination. Figure 5.41 gives the power stage output voltage and current whilst Figure 5.42 gives the power stage output voltage and secondary winding current.

Examination of the load current and voltage in Figure 5.41 demonstrates that the power stage can act in all four quadrants since all four combinations of voltage and current polarity are demonstrated. The freewheel action of the load current is illustrated during the zero voltage periods of the output voltage. Bi-directional power flow across the transformer is demonstrated during the non-zero voltage periods with the bipolar nature of the transformer secondary winding current of Figure 5.42(b). The basic operation of the bi-directional transformer circuit is thus verified although the excessive oscillations may lead to EMI emissions. The oscillations occur across the power transformer as a result of the interaction between the primary side leakage inductance and the parasitic capacitance of the bridge devices and zener diode.



Power Stage Supply=12V_{DC}, Clock Frequency=300kHz, Load = 10Ω, 1.2mH, 50% Duty Cycle

Figure 5.41 - Load voltage and current with bi-directional transformer circuit

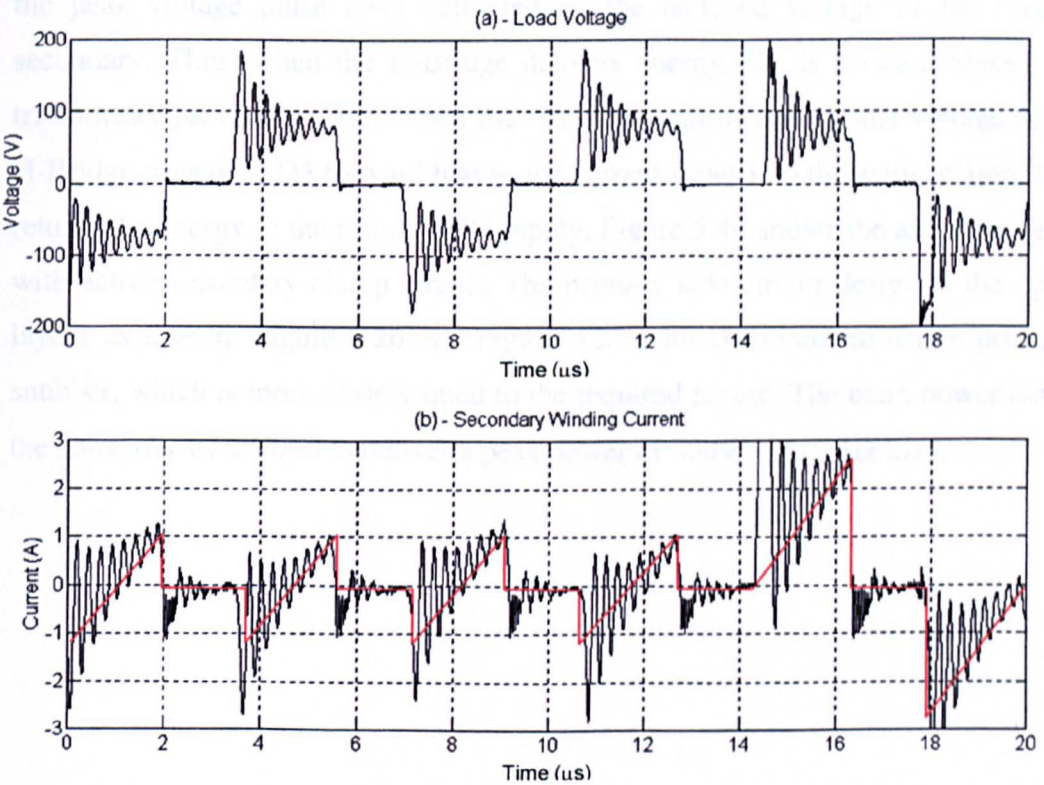


Figure 5.42 - Load voltage and secondary winding current with bi-directional transformer circuit (red lines indicate the underlying current profile)

5.3.3 Active Clamp Return Circuit

The structure of the secondary side circuit with the active clamp for energy return is shown in Figure 5.43. The active clamp circuit is of the same construction as the primary side clamp discussed earlier.

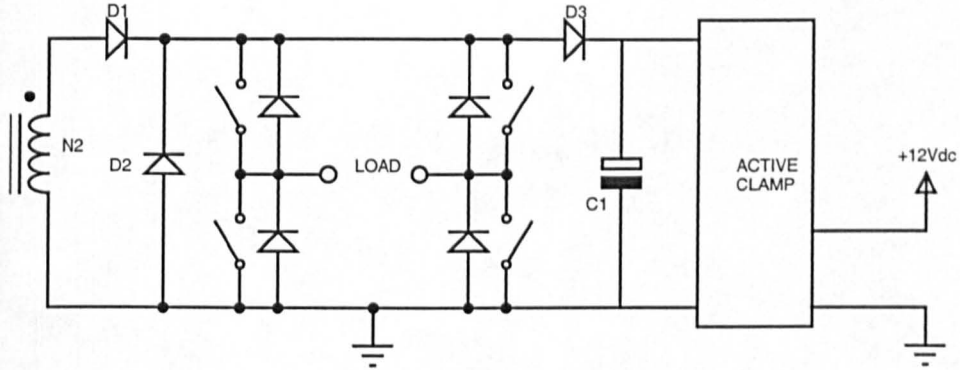


Figure 5.43 - Secondary side structure with active clamp

D1 rectifies the transformer secondary voltage whilst D2 provides a current freewheel path for times between the primary side turning off and the bridge switching into a freewheel state. The active clamp maintains the voltage across C1 to a few volts above the peak voltage pulse level delivered by the rectified voltage of the transformer secondary. Thus, when the H-Bridge delivers energy, D1 is forward biased and the transformer provides power. When the H-Bridge returns energy, the voltage across the H-Bridge rises until D3 forward biases and current flows into the active clamp; this then returns the energy to the primary DC supply. Figure 5.44 shows the amplifier prototype with active secondary clamp circuit. The primary side circuit design is the optimised layout as used in Figure 5.26 and Figure 5.27 with an improved active primary side snubber, which is more closely rated to the required power. The main power devices of the converter were sized to deliver a peak power of 500W into a 4Ω load.

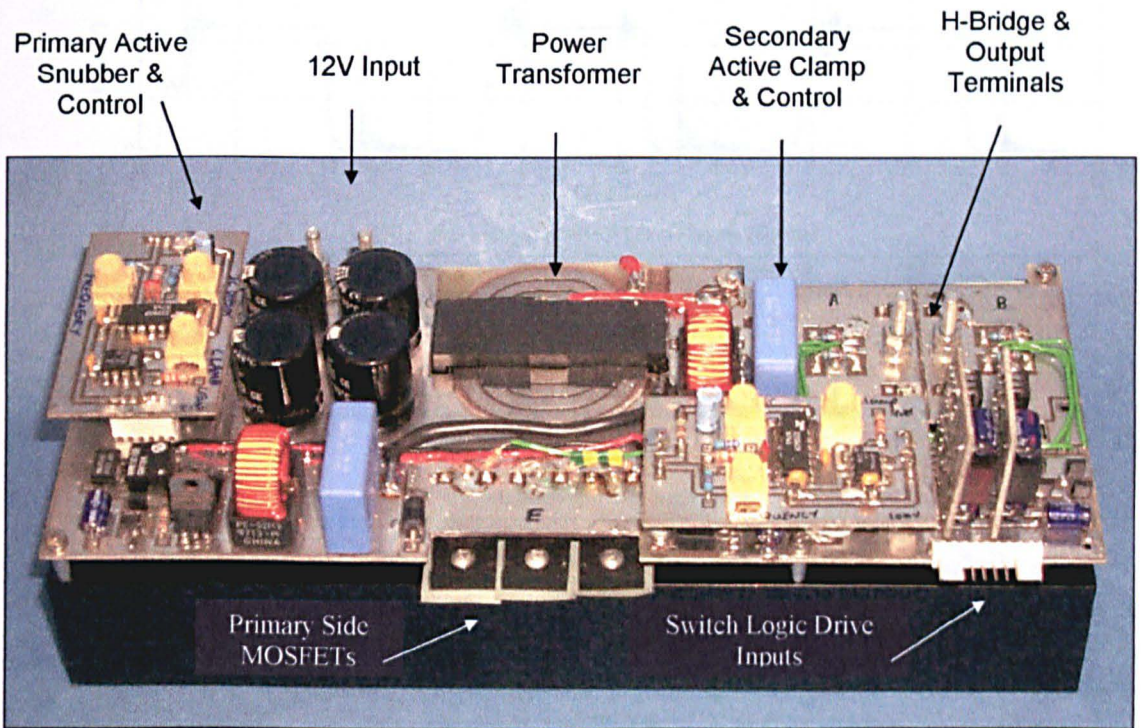


Figure 5.44 - Full prototype with secondary active snubber

The secondary side rectifier is rated at 200V and this will allow a maximum voltage of 25V across the primary winding when the core is demagnetising. Therefore, the clamp level of the primary side snubber can be set to a maximum of $(12+25)=37\text{V}$. This corresponds to a maximum operating duty cycle of the primary side switch of 68%. For the worst case input voltage of 15V, the maximum operating duty cycle is reduced to 63%.

Since the transformer turns ratio is 1:8, the output pulse height from the secondary is 96V for a 12V DC supply. However, for initial tests, the secondary clamp level was set to 150V, which is much greater than the peak supply pulse height. The clamp level will be reduced once the initial circuit operation has been verified.

In order to demonstrate power flow in two quadrants, the 11.3Ω resistor was used as a load and the converter configured to deliver an output voltage consisting of a series of positive and negative voltage pulses. Figure 5.45 a-e shows the primary side gate drive, primary side MOSFET Vds, secondary winding voltage, rectified secondary voltage and load voltage respectively. The power stage was supplied with 12V, run at 50% duty cycle with a primary side clamp level of 30V.

In order to verify four quadrant converter operation, the resistive load was replaced with an inductor with measured parameters of $L=102\mu\text{H}$ and $R=0.06\Omega$ and the resultant waveforms are shown in Figure 5.46 a-f.

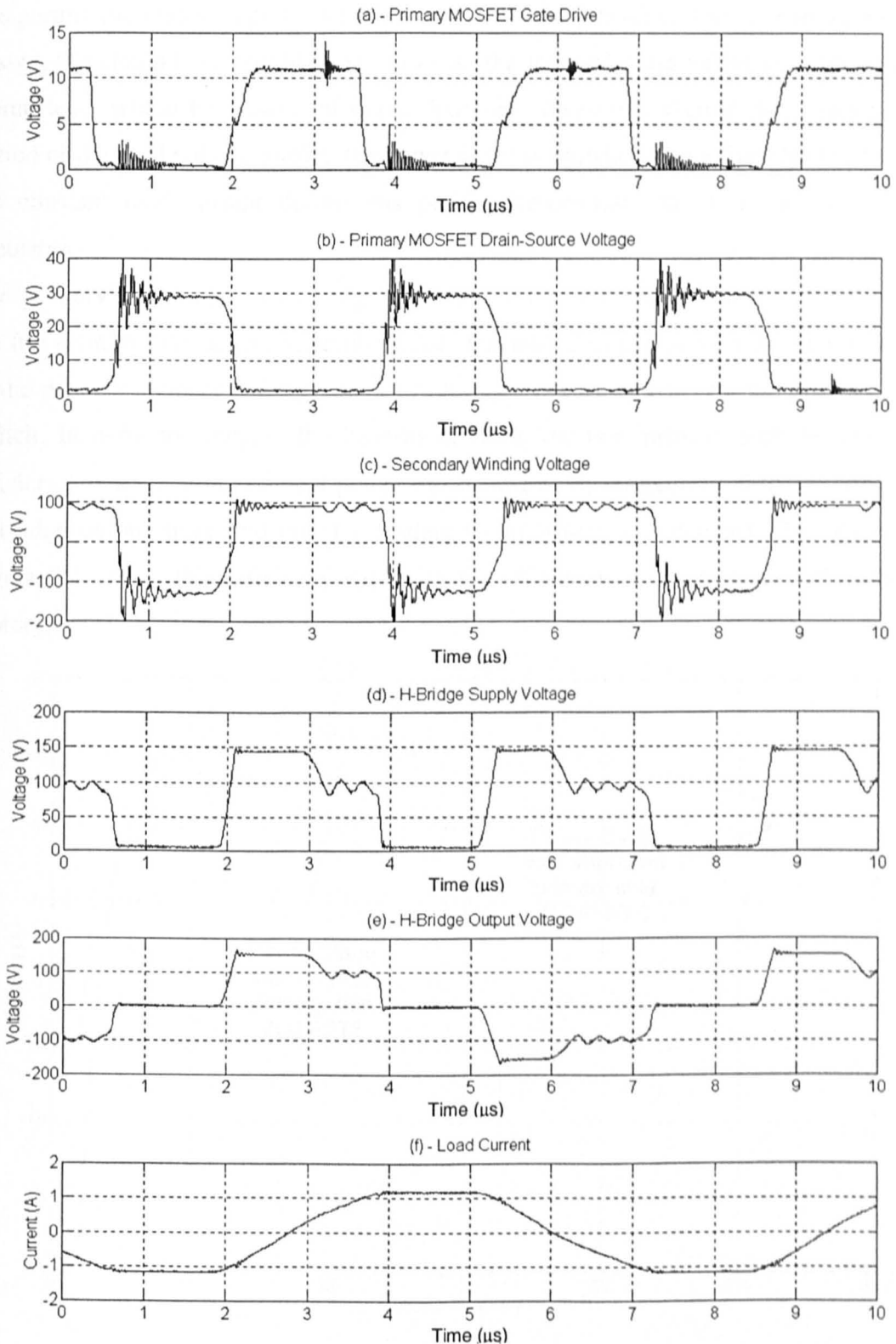


Figure 5.46 - Converter waveforms with inductive load

In order to verify four quadrant converter operation, the resistive load was replaced with an inductor with measured parameters of $L=102\mu\text{H}$ and $R=0.06\Omega$ and the resultant waveforms are shown in Figure 5.46 a-f.

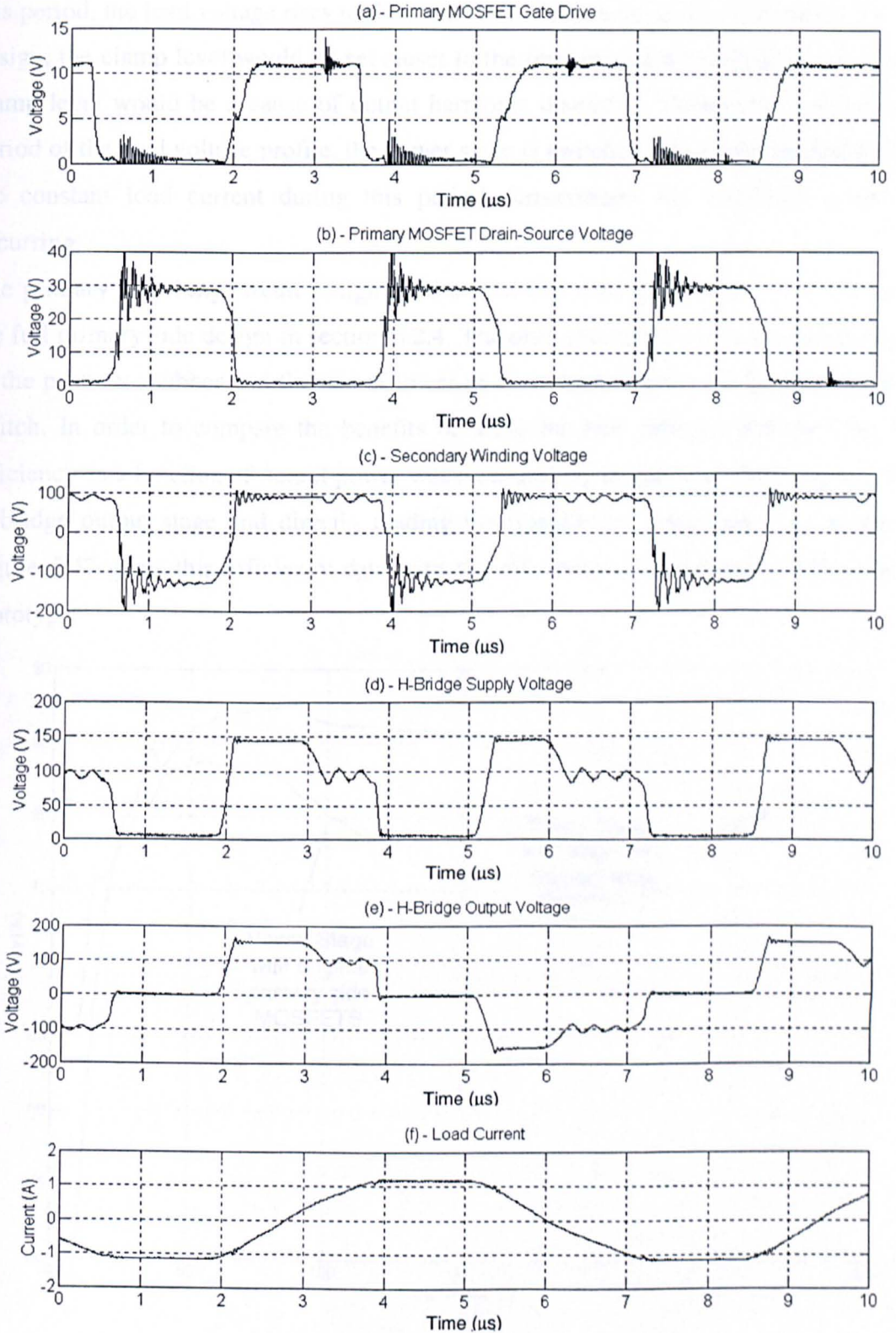


Figure 5.46 - Converter waveforms with inductive load

Examination of the load current and load voltage, Figure 5.46 (e) and (f), verifies that the converter can operate in all four quadrants. When the load current and voltage are simultaneously of opposite polarity, energy is being returned from the load and during this period, the load voltage rises to the secondary clamp level of 150V. In an optimised design, the clamp level would be set closer to the forward pulse height as an excessive clamp level would be a cause of output harmonic distortion. During the zero voltage period of the load voltage profile, the power stage is switched into a freewheel state and the constant load current during this period demonstrates the freewheel action is occurring.

The primary switching circuit design used on the two converters above is a replica of the full primary side design in section 5.2.4. The only changes were in the optimisation of the primary snubber and the use of lower on-resistance devices for the primary side switch. In order to compare the benefits of using the new primary side devices, the efficiency as a function of output power was measured by temporarily disconnecting the H bridge output stage and directly loading the transformer secondary. The graph of Figure 5.47 gives this efficiency data with the efficiency of the original full primary prototype.

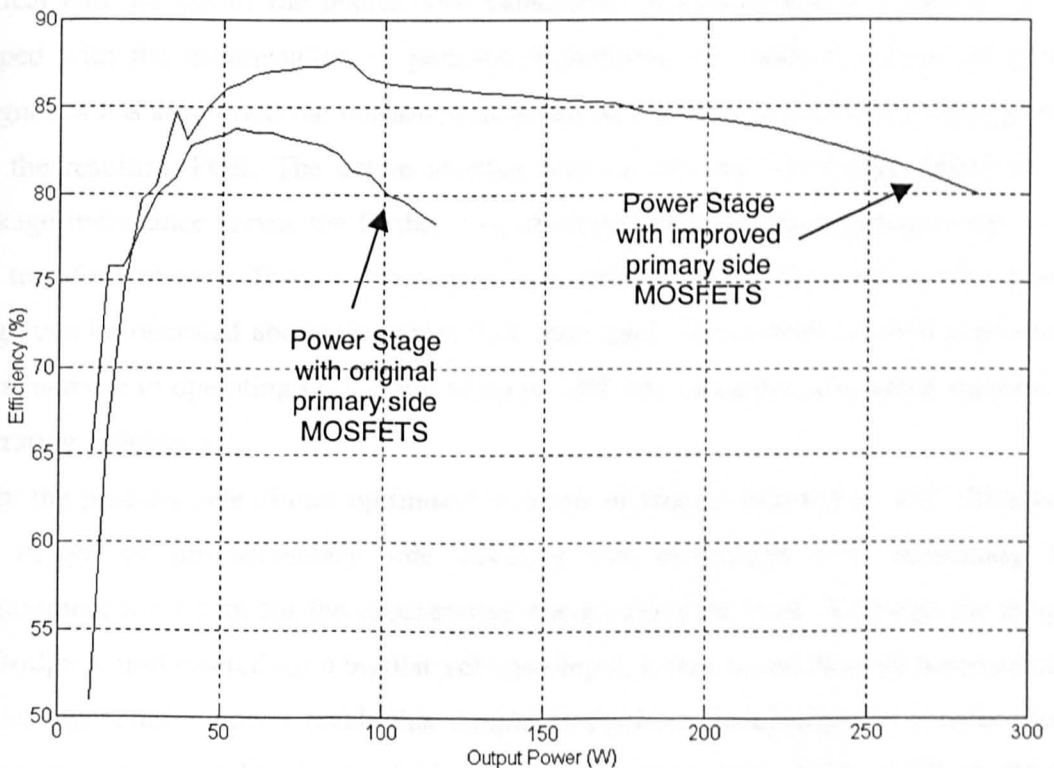


Figure 5.47 - Comparison of primary side efficiencies

The figure indicates that the optimised primary side design can now deliver power at greater than 80% efficiency over most of the operating range. Measurements beyond 300W were not possible due to the current capability of the power analyser used to measure the DC input current. However, through extrapolation of the efficiency profile, it is believed that the efficiency of the forward conversion path will be above 70% at the 500W required output power.

5.4 Conclusions

The prototype converters presented in this chapter have proved the basic concept of the novel converter. The design effort has removed the necessity for an intermediate DC supply and therefore eliminated the intermediate filter components.

The design of the primary side circuit was found to be dominated by the need to lower parasitic inductance of the transformer as far as possible. Due to the high primary currents, the energy stored in parasitic circuit inductances must be recaptured to ensure efficient operation. The transformer leakage inductance has been shown to be the dominant parasitic inductance and recapture of the energy stored within it has been achieved with an active snubber. The layout of the primary switching circuit is also critical and the use of the planar core transformer integrated into the main PCB has helped with the minimisation of parasitic inductance. In addition, the use of planar magnetics has simplified the construction of the power stage and ensured a low profile for the resulting PCB. The active snubber used to recover the energy stored in the leakage inductance serves the further role of recapturing the magnetising energy from the transformer core. Thus, a demagnetisation winding is not required and the power stage can be operated above the usual 50% duty cycle found with forward converters. This increase in operating duty cycle of up to 75% has yielded a substantial increase in operating efficiency.

With the primary side circuit optimised in terms of transformer design and efficiency, the design of the secondary side circuitry was concerned with addressing the requirement for a path for the regenerative energy from the load. Although the simple H-Bridge output catered for a bipolar voltage output, it was found through measurement of the regenerative power levels that simple dissipation, for example in a zener diode clamp, was unacceptable due to the level of in-efficiency this would introduce. Of the two methods used to return this power to the initial DC link, the active snubber approach offered the simplest solution. The use of the bi-directional transformer

topology is potentially cheaper since it only requires the addition of a synchronous rectifier although parasitic oscillation will compromise its performance.

With the improved gate drive circuitry and higher operating duty cycles, the forward power conversion path was found to have a peak efficiency of greater than 80%. The main cause of power loss is in the primary side switching MOSFETs. The current being switched (peak of 100A) for the power rating of the converter (500W) is large and conduction loss in the primary side devices of this converter is the dominant factor in reducing efficiency. At present, three devices are used in parallel and more could be used although the extra cost involved and problems encountered with driving multiple devices would be unwelcome.

The removal of the intermediate DC stage has not been without drawbacks. The removal of the DC link smoothing capacitors has resulted in the need to provide a path for the regenerative energy back to the initial DC link. The power rating required for this regenerative path has been shown to be a strong function of the impedance presented by the load and is therefore difficult to quantify. The next chapter deals with modulation of the novel power stage and following its implementation, allows for measurement of the return power levels.

It is expected that the novel power stage will suffer from similar distortion causing effects as the conventional power stage discussed in Chapter 4. The feedback techniques discussed in Chapter 4 will be directly applicable to the novel power stage and will allow the power stage to achieve distortion levels comparable to its linear counterparts.

6 Integrated Power Stage Modulation and Switching Scheme

6.1 Introduction

The switching amplifier presented in the previous chapter has demonstrated that it is possible to dispense with the requirement for an intermediate DC supply and reservoir filter to produce a direct conversion path from the 12V battery. The proposed power stage design can deliver power in all four quadrants with output duty cycles from zero to approximately 70% and has been optimised to operate at a 300kHz switching frequency.

To obtain audio output, the power stage needs to be driven by an appropriate modulation strategy and the application of both PWM and PDM is discussed in this chapter. In addition, the distortion mechanisms introduced by the new power stage are analysed and compared to those described in Chapter 4. Finally, the feedback techniques used to linearise conventional Class-D power stages are applied to the new power stage to give an indication of the likely level of performance obtainable from the proposed Class-D system. Although both of the secondary side power return circuits will offer the four quadrant requirement, the circuit with the secondary side active clamp is used for the results in this chapter since it offers the greatest flexibility in operating parameters.

6.2 Switching Strategy

In the proposed power stage, the output H-Bridge is supplied with a pulsed DC link and can therefore be switched without loss. The switching strategy will be such that when the voltage pulse supplied to the H-Bridge falls to zero, the bridge will switch into a freewheel state as discussed earlier. Two different methods have been employed to control the switching of the power stage. The first centres on using appropriate time delays to ensure the correct switching sequence. The second approach uses direct measurement of the link voltage to ensure zero voltage switching. The relative advantages and disadvantages of both of these methods will be compared.

The exact interface logic required differs between PDM and PWM driven systems, however, for each case, two signals are derived to drive the power stage, one to define the pulse polarity and the other to define pulse duration.

To aid the description of the two switching strategies, consider the output power stage shown in Figure 6.1. The primary side switch and the four output switches are denoted as A to E as shown in the figure.

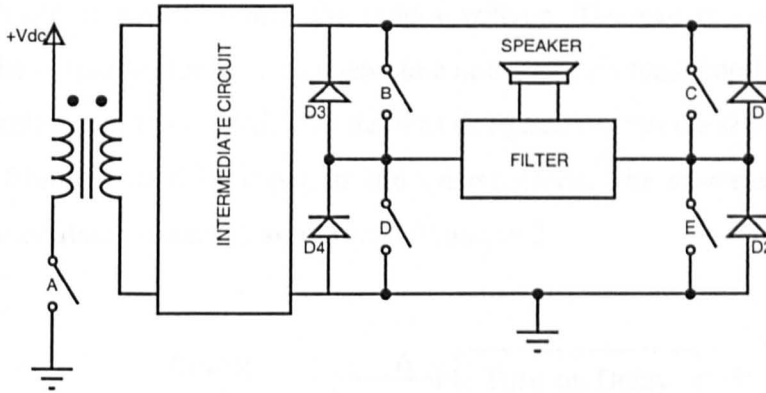


Figure 6.1 - Full generic power stage

6.3 Time-Delay Operation

The operation of this strategy is based on introducing a delay into the switching of the power semiconductors, A-E. The turn off transitions of devices B and C are delayed whilst the turn on transitions of devices A, D and E are delayed. The length of the delay will be similar in duration to the dead-time employed in a conventional Class-D power stage, typically less than 500ns.

Consider the switching sequence required for the system changing from the freewheel state (devices D and E on) to a positive output voltage pulse (devices A, B and E on) and back to a freewheel state. The sequence is as follows: -

- The signal to provide a positive voltage pulse arrives. The turn on of device A is delayed and during this time, device B switches on and device D is switched off. The load current is transferred from device D to device B.
- After the short delay, device A switches on and drives the secondary output voltage high. With devices B and E on during this period, a positive voltage pulse appears across the load.
- The signal to reset into the freewheel state arrives and device A switches off, sending the secondary voltage back to zero. For the short delay time, devices B and

E remain switched on and then device D switches on whilst device B switches off, transferring the load current to device D.

The switching sequence is similar for the negative pulse configuration except that it is devices C, D and E which control the output voltage. The use of switching delays ensures that the output bridge only changes state under zero voltage conditions.

A programmable array logic (PAL) device was designed to provide the five switching logic signals from the modulator output and system clock. The systematic diagram of the interface/modulator system is as shown in Figure 6.2.

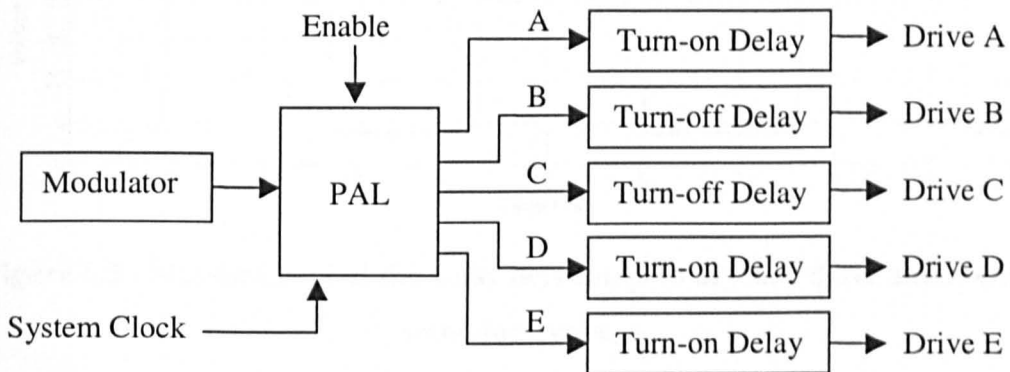


Figure 6.2 - System diagram of time-delay modulator/power stage interface

The delays were set up in practice by comparing the drive signals to the four bridge devices to the secondary voltage generated by the switching of device A. There is an inherent delay between the logic drive signal for device A changing state and the corresponding change in the voltage pulse appearing across the secondary. Figure 6.3 shows that the delay is approximately 200ns during the turn-on transition and 250ns during the turn-off transition.

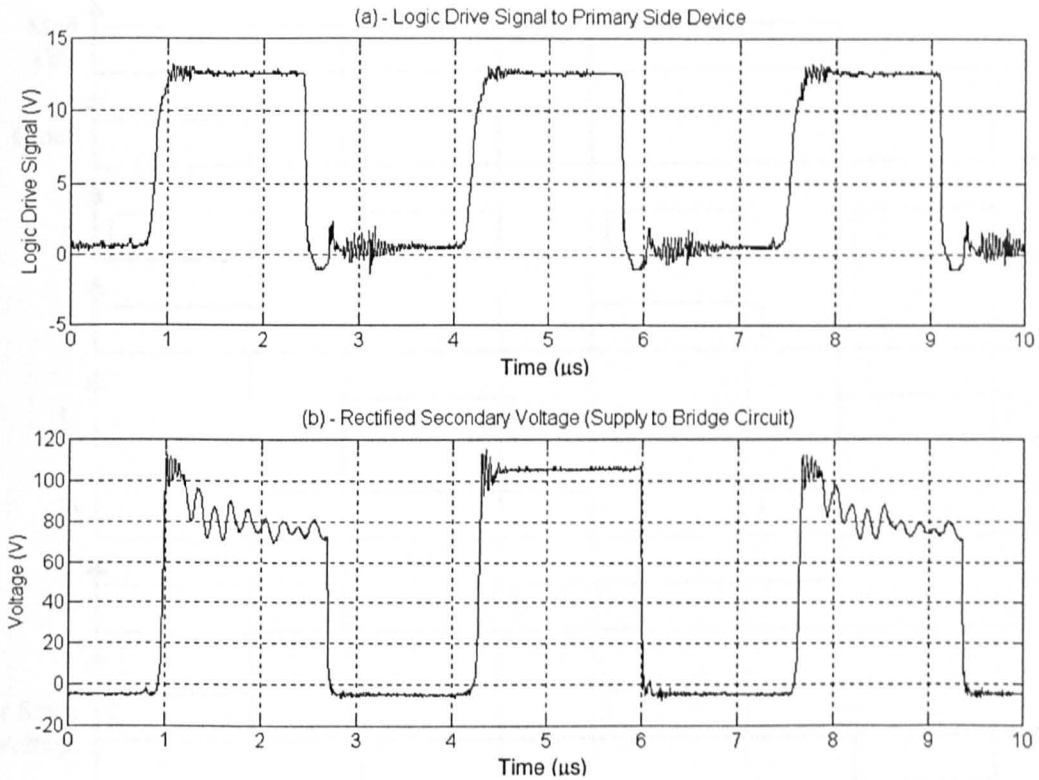


Figure 6.3 - Measurement of the delay between primary side drive and rectified secondary voltage

6.3.1 Application to PDM

Under PDM, the output will consist of a series of pulses of constant width and changing polarity. Two signals are available from the modulator, namely the clock signal and the modulator output. In this case, the modulator output signal defines the polarity of the pulse and the clock signal determines the operating duty cycle. Figure 6.4 gives the timing diagram that will result in zero voltage switching for the PDM driven system. The logic required in the PAL of Figure 6.2 to generate the switching signals from the clock and modulator output is shown in Table 6.1. Since the sample and hold element on the $\Sigma\Delta$ modulator is triggered by the rising edge of the clock signal, the duty cycle of the clock can be used to set the duty of the secondary pulses to a maximum of 70%.

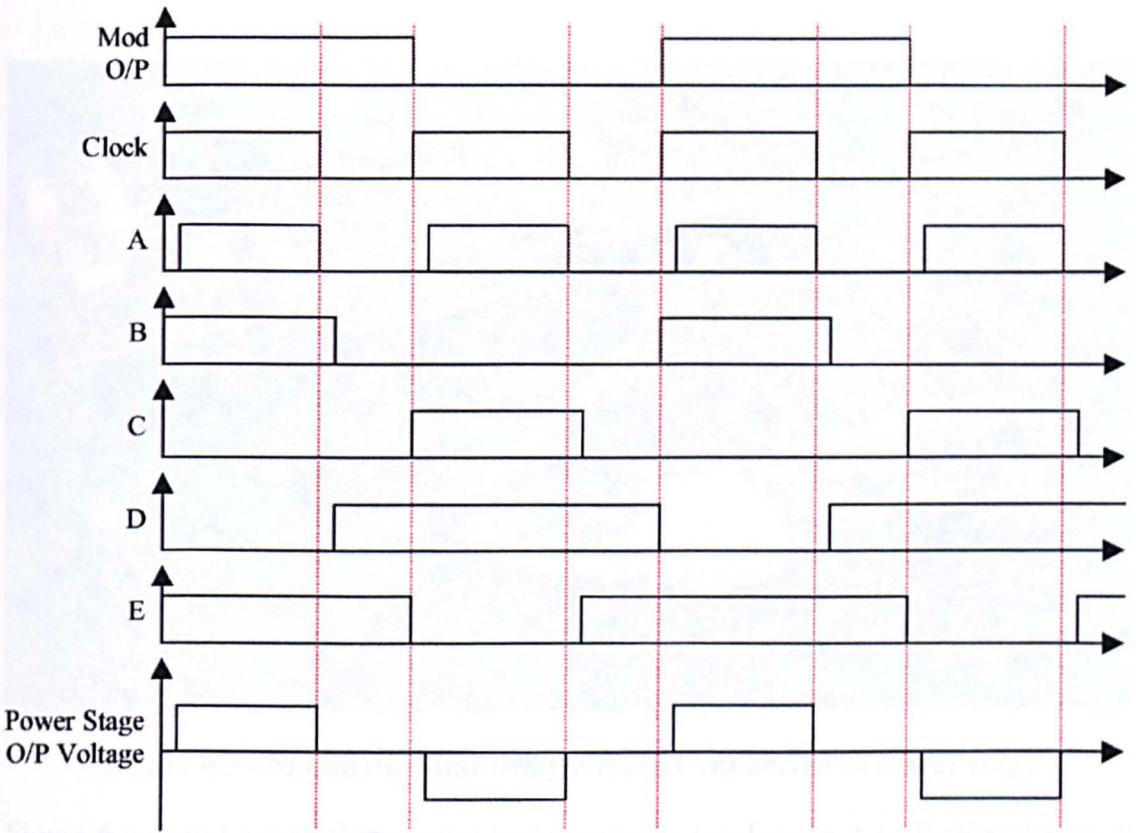


Figure 6.4 – Timing diagram for PDM operation

Enable	Modulator Output	Clock	Output State	A	B	C	D	E
0	0	0	Off	0	0	0	0	0
0	0	1	Off	0	0	0	0	0
0	1	0	Off	0	0	0	0	0
0	1	1	Off	0	0	0	0	0
1	0	0	Freewheel	0	0	0	1	1
1	0	1	Negative Pulse	1	0	1	1	0
1	1	0	Freewheel	0	0	0	1	1
1	1	1	Positive Pulse	1	1	0	0	1

Table 6.1 - Logic required for PDM interface

In the modulator interface circuit, design care was taken to isolate analogue and digital power supplies. Furthermore, the interface and modulator circuitry were mounted inside a metal box to provide shielding. BNC connectors and a differential audio input were used to keep signals as clean as possible. The full design can be found in appendix C. Figure 6.5 shows the arrangement used to connect the modulator/interface circuitry to the power stage.

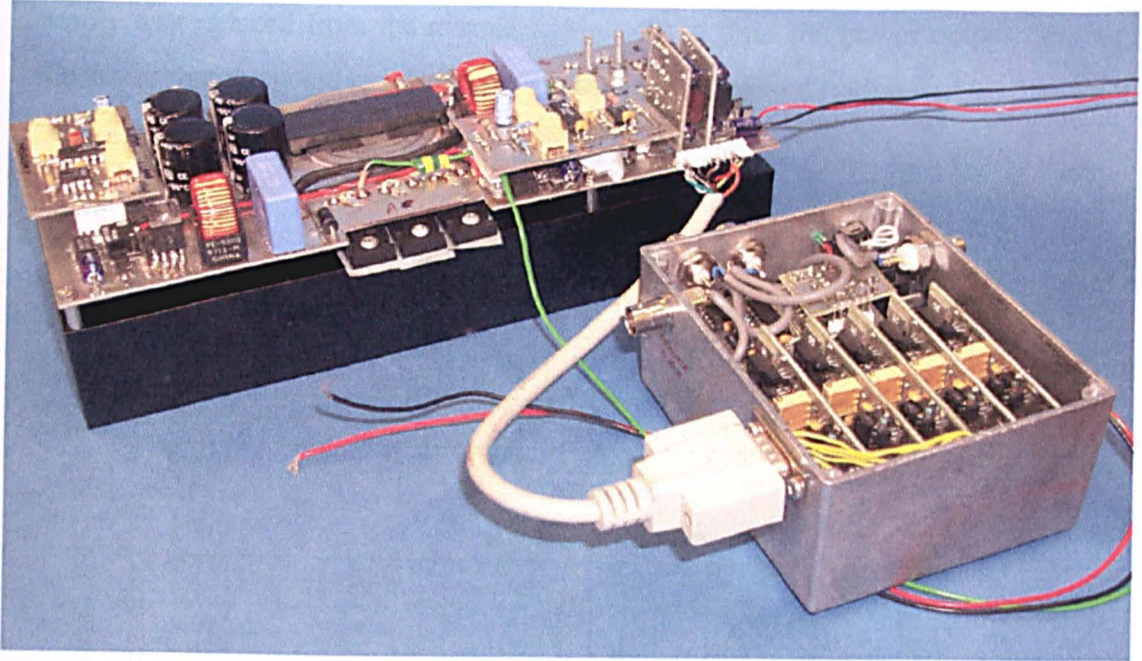


Figure 6.5 - Modulator/time delay circuitry connected to power stage

Figure 6.6 shows a typical measured logic sequence for devices A to E from the clock and modulator output signals.

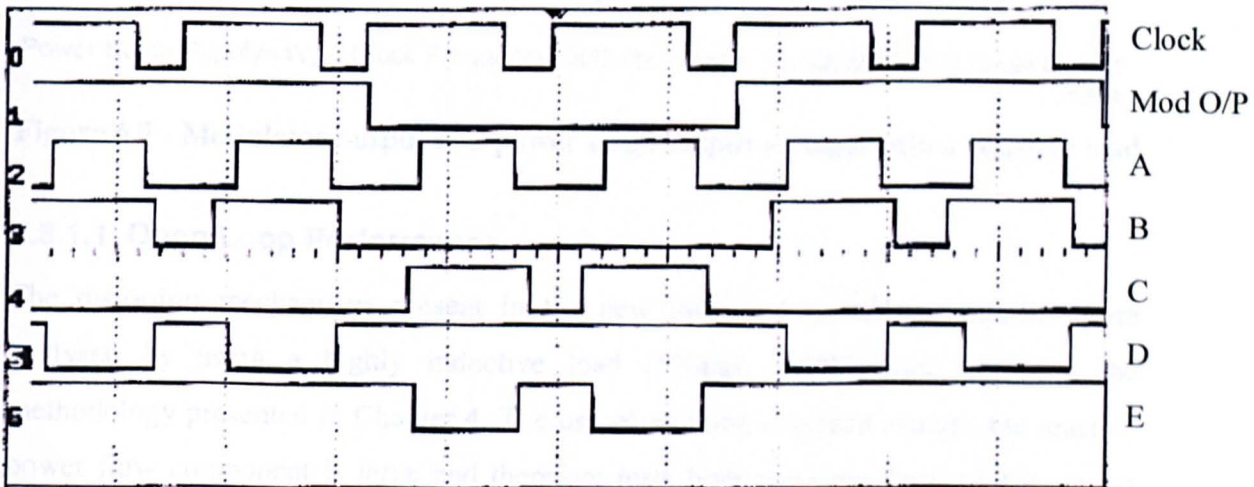
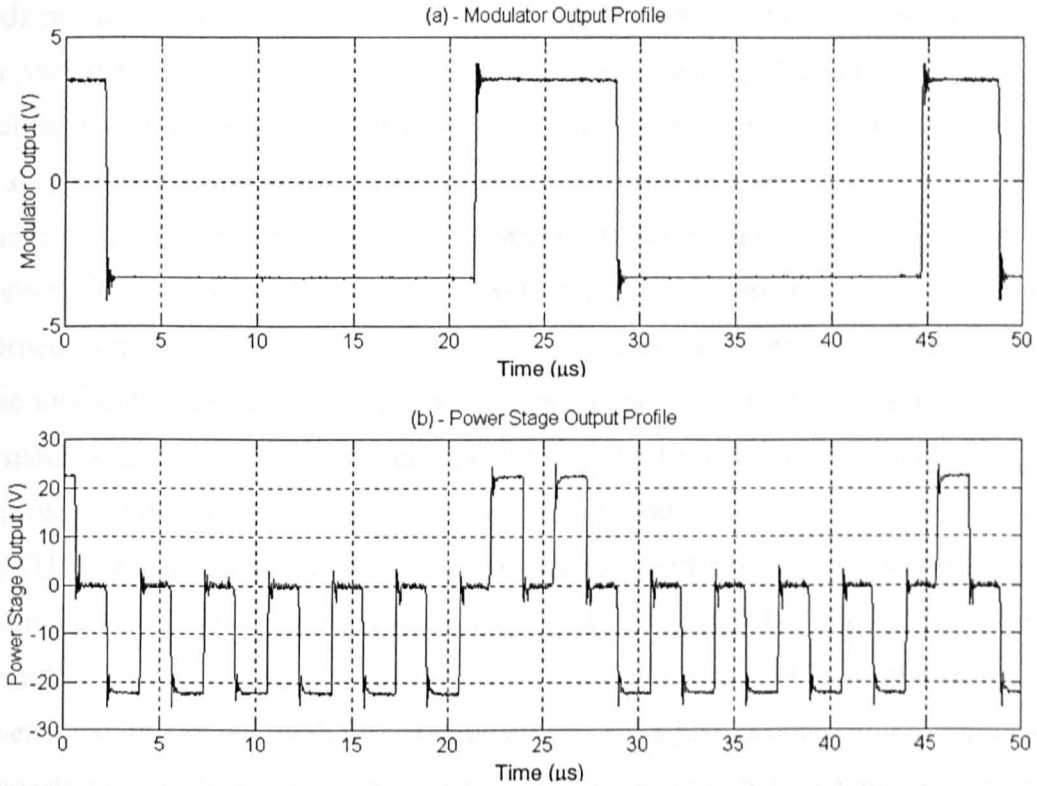


Figure 6.6 - Typical logic sequence from interface output (2 μ s/div)

The output from the power stage was initially tested by loading it with the resistive 11.3 Ω load. This load makes it possible to verify that all the delays have been set correctly, and that the resulting positive and negative pulses are of the same duration. Any mismatch in the length of the positive and negative pulses will cause a DC offset in the output signal, which may damage the loudspeaker load. Figure 6.7 shows the

modulator output and power stage output with pulse waveforms. Note that the input supply was reduced from the normal 12V to 4V to limit the power output. The figure illustrates that the positive and negative pulses are of equal duration.



Power Stage Supply= $4V_{DC}$, Clock Frequency= 300kHz , Load = 11.3Ω , 50% Duty Cycle Output Pulse

Figure 6.7 - Modulator output and power stage output voltages into a resistive load

6.3.1.1 Open Loop Performance

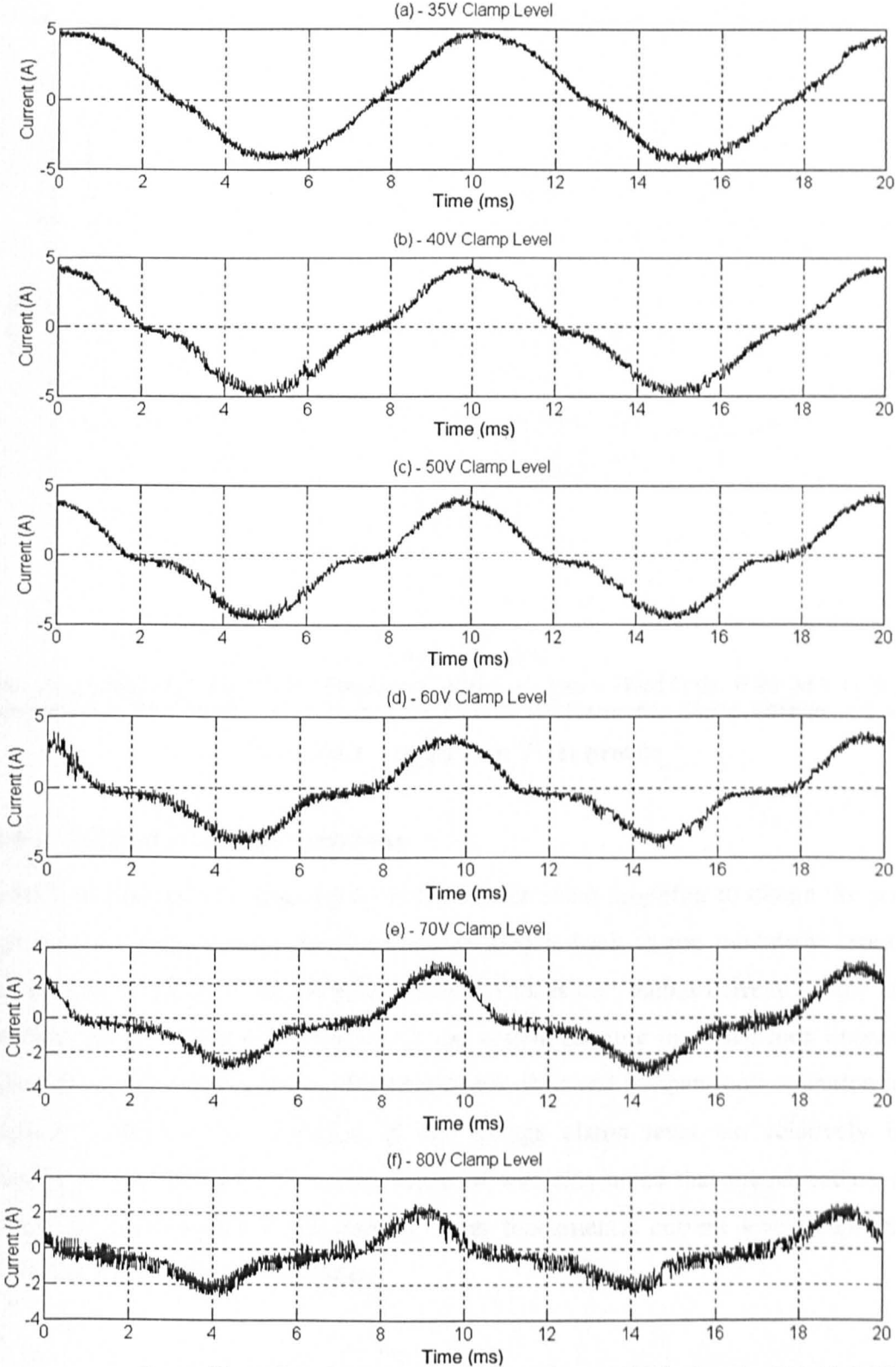
The distortion mechanisms present in the new proposed switching amplifier were analysed by using a highly inductive load ($590\mu\text{H}$, 0.05Ω) and following the methodology presented in Chapter 4. The use of an inductive load ensures the reactive power flow component is large and therefore tests both the main forward conversion path and the secondary side snubber reactive energy recovery path. Any non-idealities in the circuit operation will appear as a distortion of the fundamental current shape.

The main distortion mechanism present in the new power stage is due to the action of the secondary side snubber. When the power flow is regenerative, the voltage pulse height rises above the normal level until it reaches the clamp voltage level. Thus, during the regenerative period, the voltage-time product of the output voltage pulse is greater than required and therefore more energy is removed from the load. This effect will

introduce additional distortion, the level of which will be a function of the clamp voltage level and the power factor of the load.

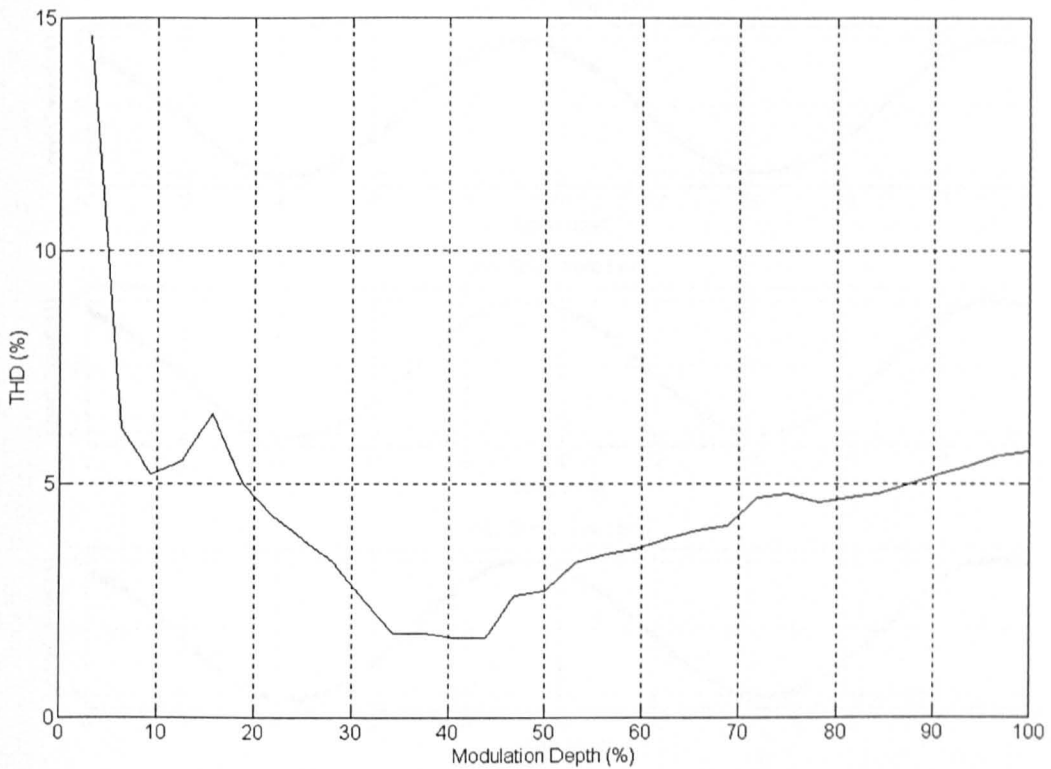
To examine the effect of secondary side clamp level on the fundamental current shape, a fundamental frequency of 100Hz and a DC supply of 5V were used. The clamp level was varied from 35V, slightly greater than the secondary pulse height, to 80V. The resulting measured output current waveforms, Figure 6.8, demonstrate that the impact of the secondary side clamp voltage on harmonic distortion is severe. Even with the clamp voltage set to a modest 5V above the normal pulse height, a high level of distortion is observed, Figure 6.8(b). As the clamp level rises, a higher proportion of the energy is returned to the primary supply and this is reflected in the lower output current for the same modulation depth. The effect is most pronounced when the fundamental current approaches zero since all of the energy put into the load during a switching cycle is removed, resulting in the flat regions of the current profile.

The THD was measured as a function of modulation depth for this open loop modulator, Figure 6.9. The clamp level was set to 100V and with a 12V DC supply, this gives an overhead of 4V in the snubber operation. Comparison of the THD profile of the new power stage, Figure 6.9, with that of the conventional Class-D power stage, Figure 4.29 demonstrates that the profiles are in fact relatively similar in both magnitude and shape. The THD measurements below 20% modulation depth are slightly misleading since the signal harmonics are approaching the noise floor of the amplifier. Thus, the open loop distortion for this power converter is of the order of 5%.



Power Stage Supply=5V_{DC}, Clock Frequency=300kHz, Load = 590μH, 0.05Ω,

Figure 6.8 - Open loop output current profile with varying secondary side clamp level



Power Stage Supply=12V_{DC}, Clock Frequency=300kHz, Load = Third Order Filter with 11.3Ω Termination, 100Hz Fundamental Frequency, Data to 10th Harmonic, Clamp Voltage =100V

Figure 6.9 – Open loop THD profile

6.3.1.2 Closed Loop Performance

Closed loop control was achieved by using a differential amplifier to obtain the power stage output voltage before the filter and to feed it back to the modulator input, as described in section 4.5. Figure 6.10 shows the measured output current for the same conditions as for Figure 6.8, except with the system running in closed loop operation. Under the closed loop operation, the dead-bands observed in open-loop operation have disappeared. Indeed, the variation of the voltage clamp level has relatively little influence on the fundamental current shape. It was also noted that the secondary side snubber ran considerably cooler for the same fundamental current level, implying a much lower level of energy removal.

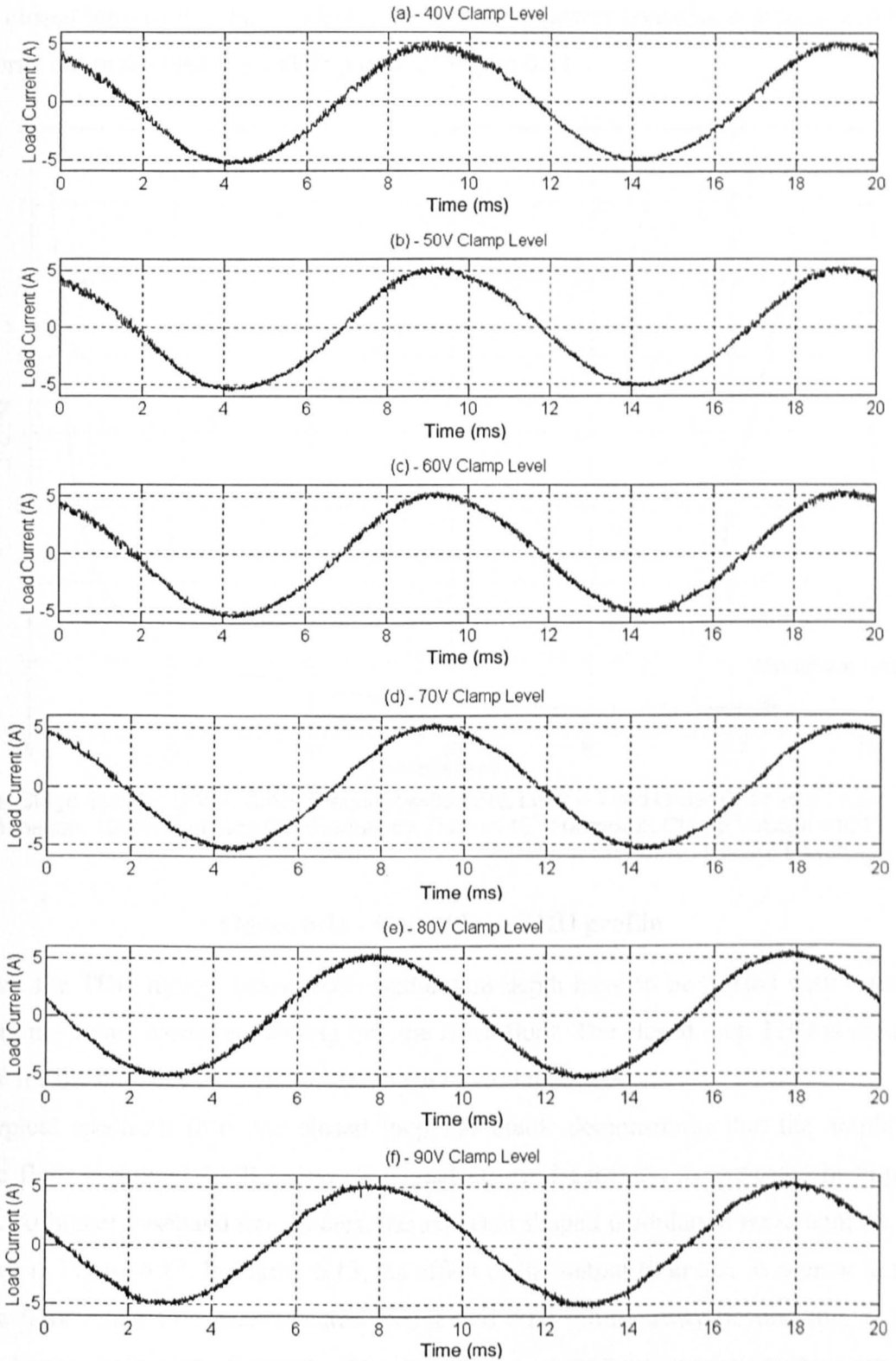
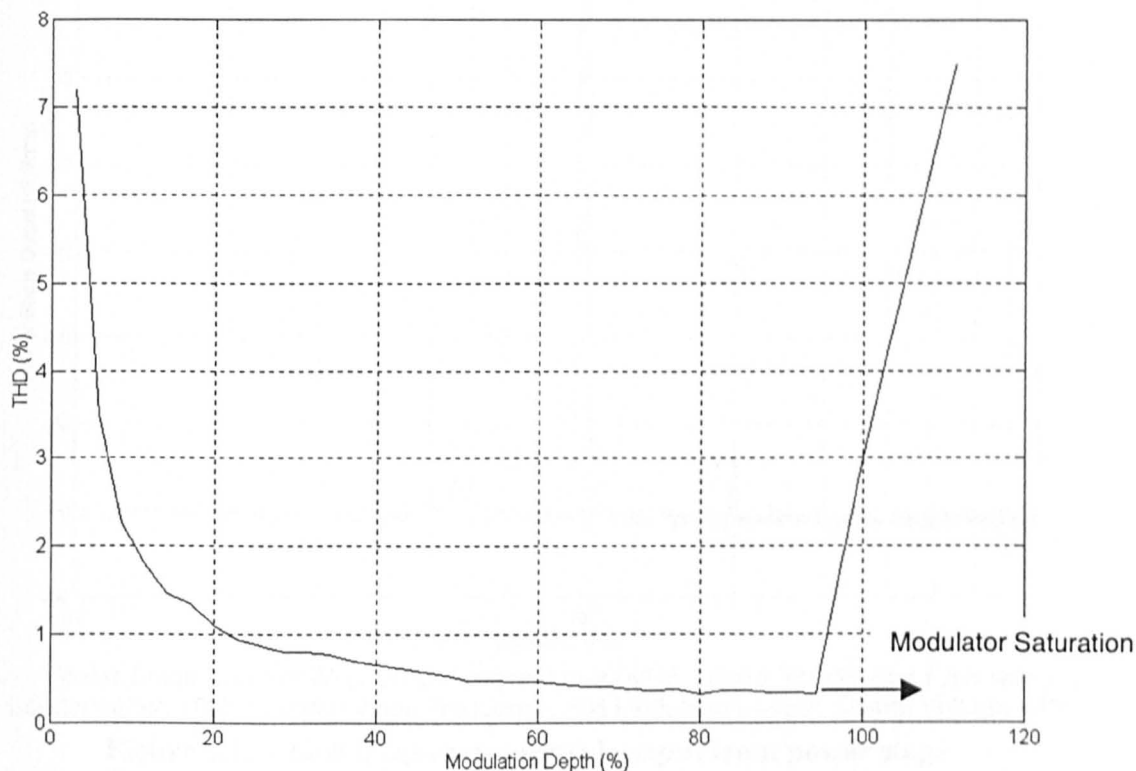


Figure 6.10 – Closed loop output current profile with varying secondary side clamp level

The closed loop control has evidently linearised the power conversion process and this is borne out in the measured THD profile of Figure 6.11

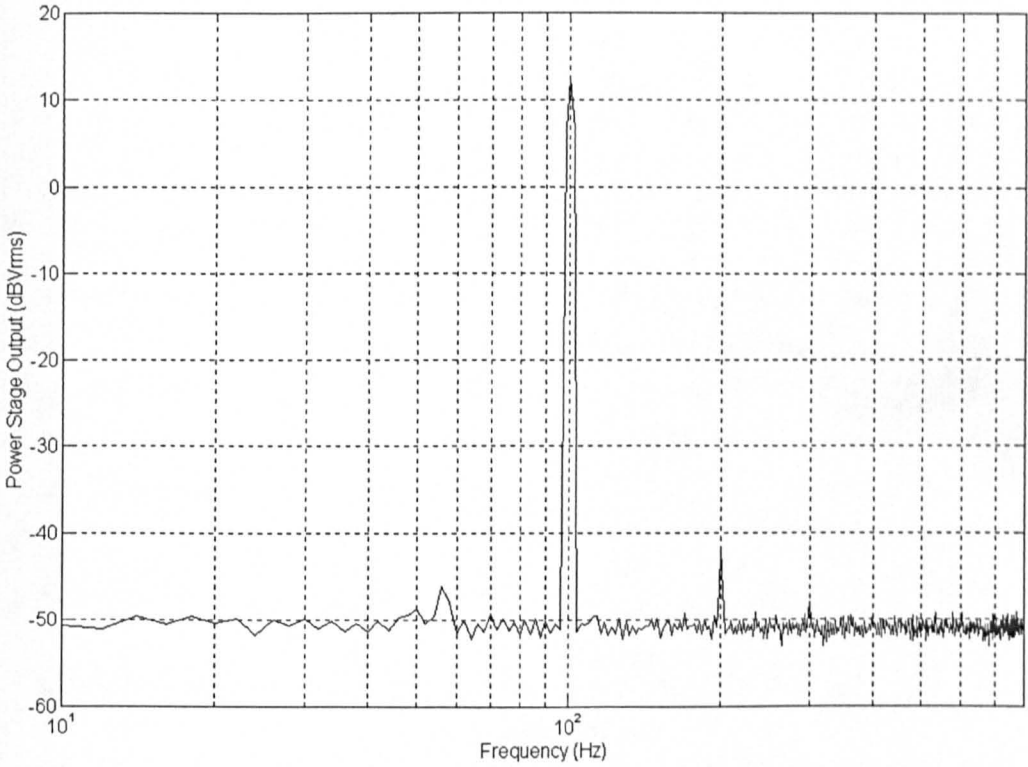


Power Stage Supply=12V_{DC}, Clock Frequency=300kHz, Load = Third Order Filter with 11.3Ω Termination, 100Hz Fundamental Frequency, Data to 10th Harmonic, Clamp Voltage =100V
20* Differential Probe Used for Feedback

Figure 6.11 - Closed loop THD profile

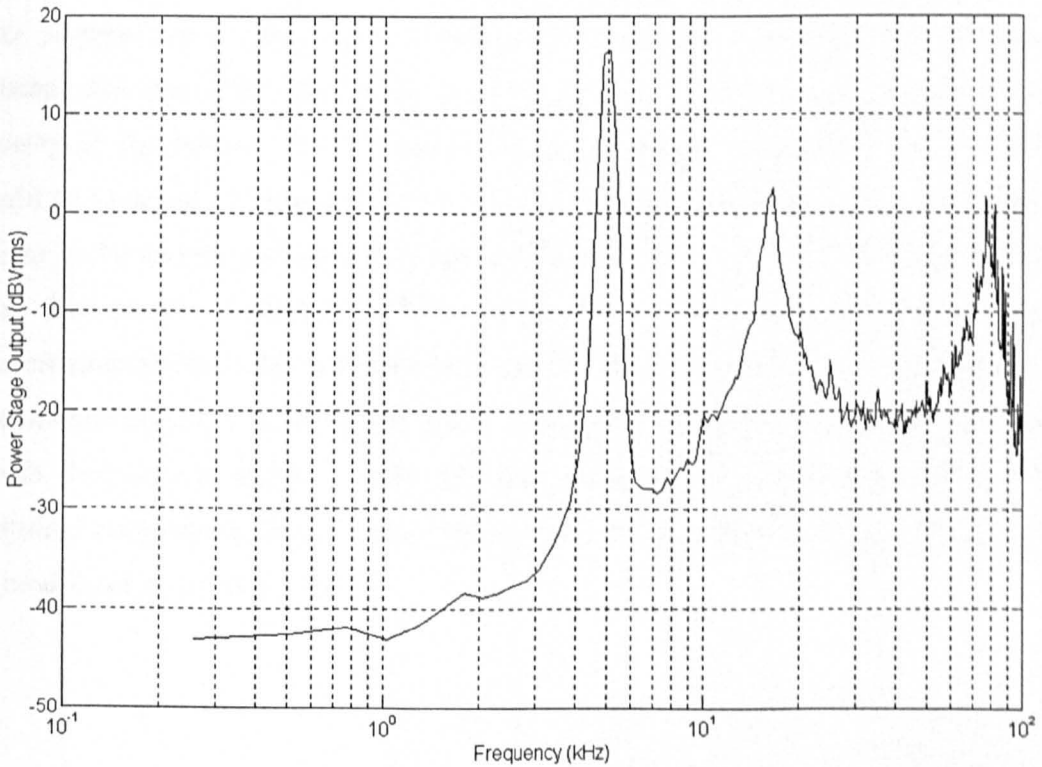
Again, the THD figures below 20% modulation depth have to be treated with caution due to the signal harmonics falling into the noise floor. The closed loop THD is around 0.5% for the majority of the amplifier range of modulation depths.

A typical spectrum from the closed loop modulator demonstrates that the amplifier noise floor is around 60dB below the signal at low frequency, as indicated in Figure 6.12. At higher baseband frequencies, the expected shaped modulation noise appears, as shown in Figure 6.13. In Figure 6.13, the effect of the output filter can be seen with the noise floor rising to a peak towards 20kHz and then falling away beyond this as the filter begins to attenuate the noise. It is interesting to note the secondary peak at around 80kHz, which is due to the loudspeaker impedance underloading the filter at high frequency. By replacing the speaker with the purely resistive load, this secondary peak disappears, Figure 6.14. In practice, it may be necessary to use a compensation network avoid damage to the high frequency drive units in a loudspeaker system.



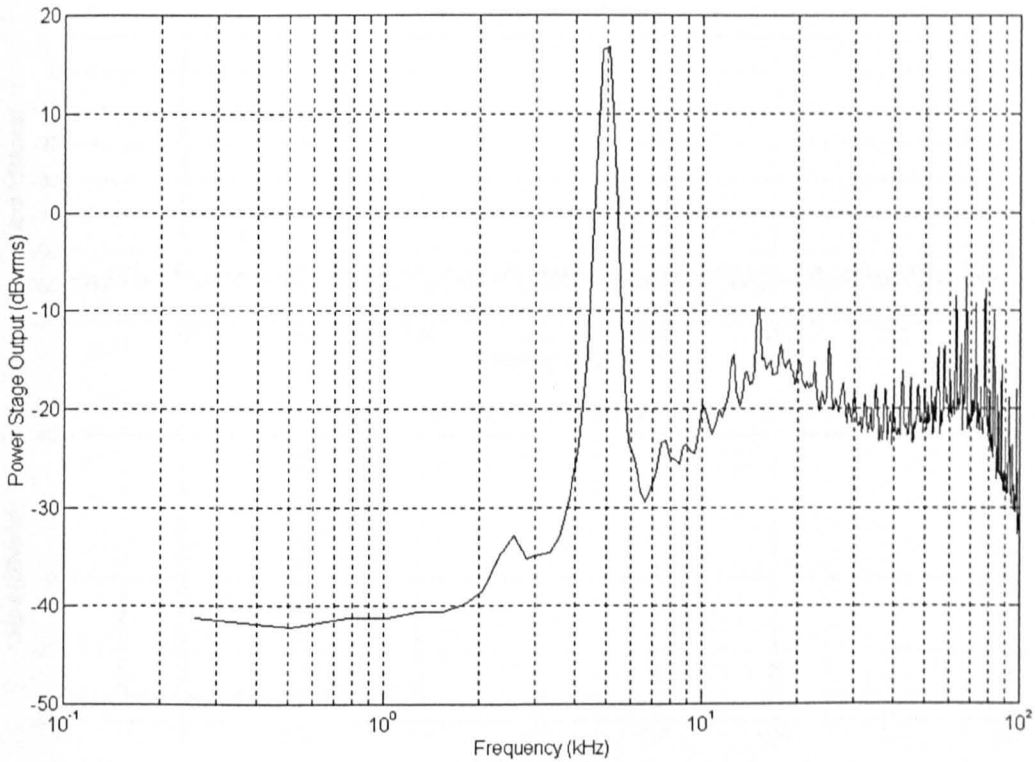
Power Stage Supply=5V_{DC}, Clock Frequency=300kHz, Load = Third Order Filter with 4Ω Loudspeaker, 100Hz Fundamental Frequency, Full Modulation Depth, Clamp Voltage =40V

Figure 6.12 - Low frequency spectral output from power stage



Power Stage Supply=5V_{DC}, Clock Frequency=300kHz, Load = Third Order Filter with 4Ω Loudspeaker, 5kHz Fundamental Frequency, Full Modulation Depth, Clamp Voltage =40V

Figure 6.13 - Full band spectral content (Loudspeaker load)



Power Stage Supply=5V_{DC}, Clock Frequency=300kHz, Load = Third Order Filter with 11.3Ω Resistive Termination, 5kHz Fundamental Frequency, Full Modulation Depth, Clamp Voltage =40V

Figure 6.14 - Full band spectral content (Resistive load)

After comparison of the output voltage and current into a resistive load, it became apparent that the differential probe used for feedback was a major limitation in the linearity of the system. With a resistive load, the output voltage and current spectra should be identical and Figure 6.15 shows that this is in fact far from the case. Both the current probe and the differential probe were battery driven as to eliminate mains borne noise. The current probe has a 5MHz bandwidth and is therefore suited to accurate measurement of the 100Hz fundamental signal. The figure shows that in addition to the fundamental signal, the differential probe also picks up, or generates, substantial other signals that do not appear in the spectrum measured by the current probe. These additional components then cause problems with linearity since they are fed back into the modulator as an error signal.

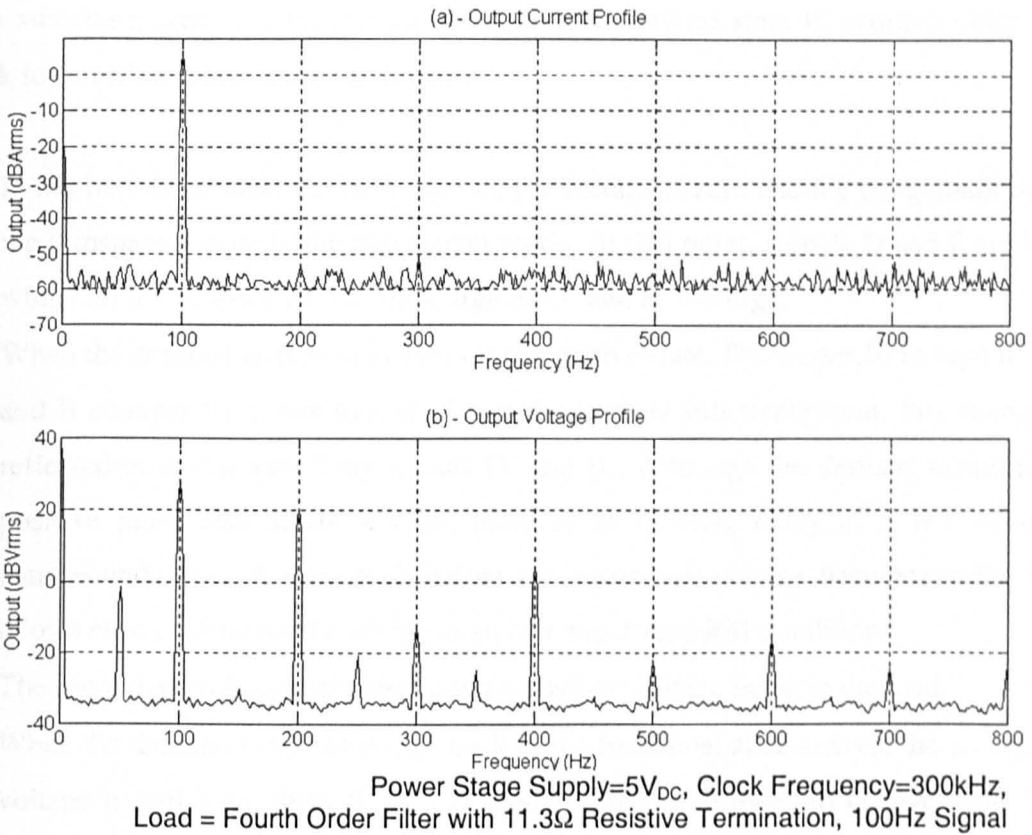


Figure 6.15 - Measured current and voltage in resistive load

6.4 Bridge Voltage Monitoring Operation

With bridge voltage monitoring, a transparent latch system is used to ensure that the bridge only switches under zero voltage conditions. Time delays are not used implicitly with this scheme but appear as a result of the circuit operation.

The system operates as shown in Figure 6.16.

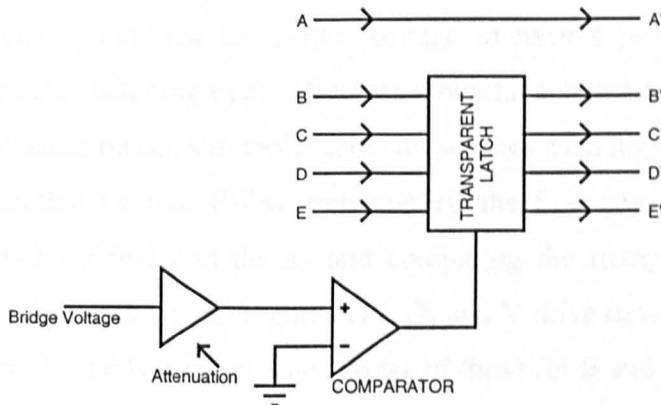


Figure 6.16 - Voltage monitoring / transparent latch system

The switching sequence for the transition from freewheel state to positive pulse and back to freewheel state is now as follows: -

- In the freewheel state, the H-Bridge supply voltage is zero and the comparator holds the transparent latch in the transparent mode. At this point, signals D and E are high whilst all the others are low. Thus, signals D' and E' are high.
- When the demand arrives to switch into a positive state, D changes from high to low and B changes from low to high. Since the latch is still transparent, this change is reflected in device switching signals D' and B'. Although the demand signal for a positive pulse also sends A high, there is an inherent delay of a few hundred nanoseconds after A goes high before the secondary voltage becomes high. This allows enough time for the bridge to switch under zero loss conditions.
- The secondary voltage rises, providing a positive voltage pulse to the load.
- When the demand signal to switch back to the freewheel state arrives, the secondary voltage is still high, thus, B', C', D' and E' are not allowed to change state. The primary side switch, A, however, can turn off and when the secondary voltage has fallen to zero, the comparator signals the transparent latch to let the logic signals change and therefore, device B turns off and device D turns on. Thus, all the secondary side switching transitions are undertaken at zero voltage. A similar process occurs for a negative voltage pulse.

6.4.1 Application to PWM

Over one switching cycle, the integrated power stage can provide a positive or negative pulse of duty cycle up to about 70%. Thus, it is more suited to a unipolar PWM strategy since a bipolar scheme requires the output voltage to have a positive and negative voltage during a single switching cycle. Whereas a bipolar scheme switches each leg of the H-Bridge in opposite phase, a unipolar scheme switches each leg independently. The two legs are controlled by two PWM comparators, the first comparing the triangle reference to the audio signal and the second comparing the triangle reference to an inverted version of the audio signal, Figure 6.17. (X and Y drive devices B and C whilst the drive for devices D and E is simply the inverse of those for B and C respectively).

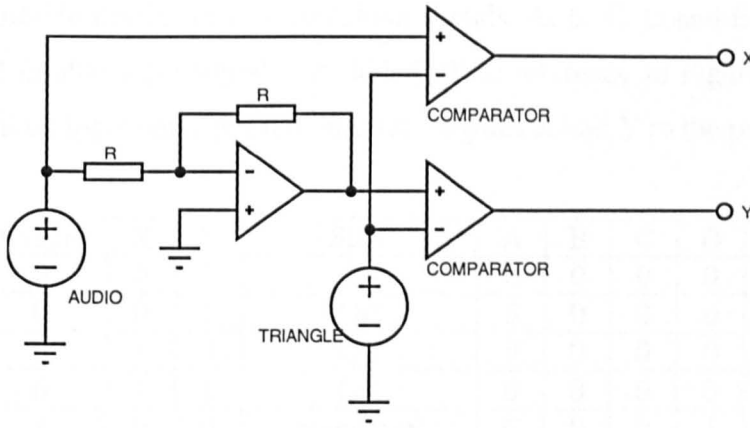


Figure 6.17 - Unipolar PWM generation

For zero audio demand signal, the legs of the H-Bridge switch in phase giving zero output voltage. As the demand signal magnitude increases, the duty cycle of one leg increase whilst that of the other decreases, giving a net positive or negative output.

A simple bipolar PWM modulator was described in section 3.2.1 and Figure 6.18 below shows the difference in operation between a unipolar and a bipolar switching scheme.

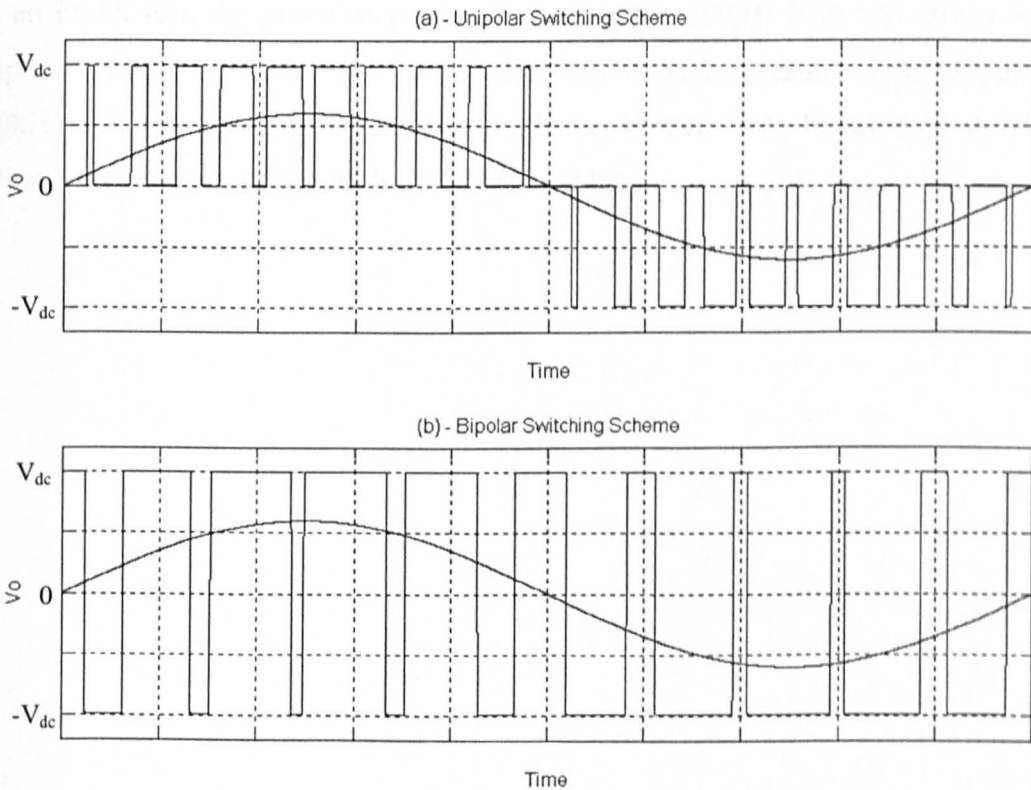


Figure 6.18 - Unipolar and bipolar switching schemes

The unipolar switching scheme effectively doubles the frequency of the switching harmonics and reduces the peak switching frequency ripple current [6.1].

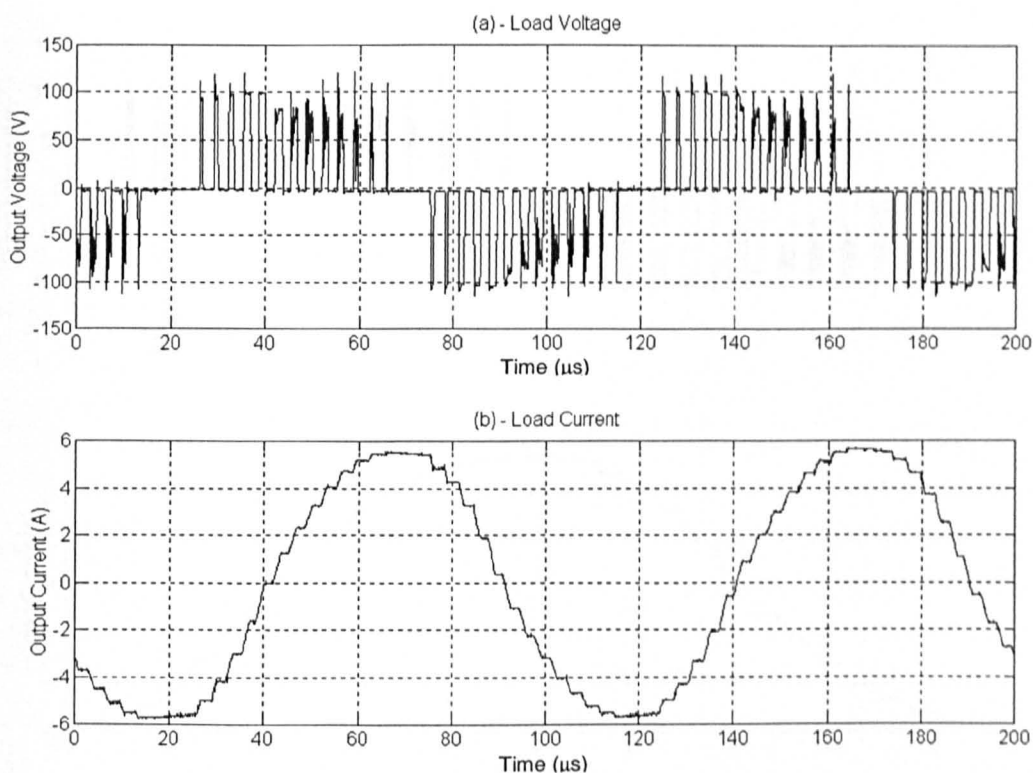
Logic is required to derive the five switching signals, A, B, C, D and E, from X and Y. An additional Enable logic signal is included. With reference to Figure 6.1, Table 6.2 gives the required logic description to interface signals X and Y to the power stage.

Enable	X	Y	State	A	B	C	D	E
0	0	0	Off	0	0	0	0	0
0	0	1	Off	0	0	0	0	0
0	1	0	Off	0	0	0	0	0
0	1	1	Off	0	0	0	0	0
1	0	0	Freewheel	0	0	0	1	1
1	0	1	Negative Pulse	1	0	1	1	0
1	1	0	Positive Pulse	1	1	0	0	1
1	1	1	Freewheel	0	0	0	1	1

Table 6.2 - Logic Derivation for Unipolar PWM Interface

This logic was realised using a fast PAL chip (7.5ns propagation delay) and the voltage monitoring system was used to ensure that the bridge switches under zero loss conditions.

As an initial test, the power stage was loaded with a 100 μ H load and driven by the unipolar PWM generator clocked at 150kHz. This frequency results in output pulses at 300kHz and the maximum modulation depth was limited 70%. Figure 6.19 shows the output load voltage and current for the inductive load.



Power Stage Supply=12V_{DC}, Modulation Depth=70%, 10kHz Sinewave Fundamental
 Secondary Clamp=100V, Load=100 μH , Modulation Frequency 150kHz

Figure 6.19 - Output load voltage and current

The reactive power flow due to the inductive load is evident from the load voltage waveform. During regenerative action, the voltage pulses rise in magnitude to the 100V level of the secondary side clamp. When the amplifier is providing energy to the inductor, the pulse height falls back to 80V (The voltage pulse height delivered by the main power transformer). This clamping action has an impact on the fundamental current shape since the higher voltage during the regenerative period causes a greater rate of change of load current, effectively steepening the sine-wave edge during this period. This can be seen more clearly in Figure 6.20.

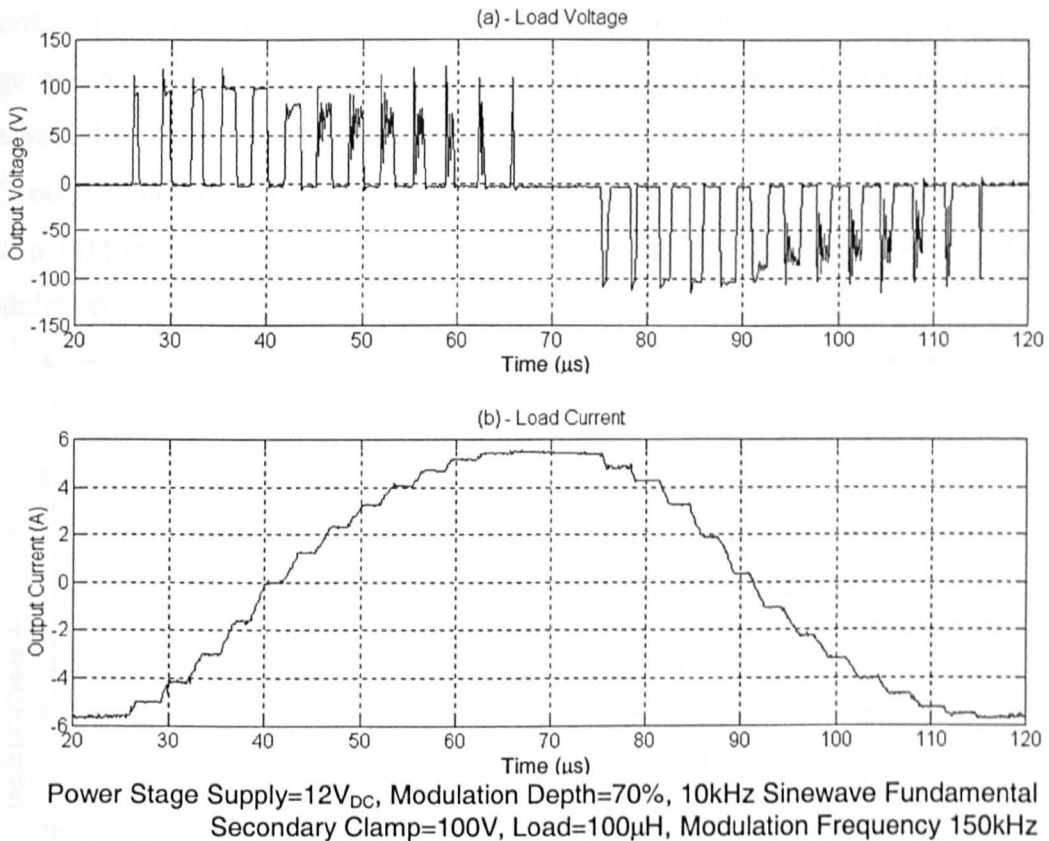


Figure 6.20 - Load current and behaviour showing regenerative action

Although the operation of the power stage will not result in the dead time distortion seen in the conventional H-Bridge Class-D system, there are three other effects now through which distortion can occur: -

- Increased voltage pulse height during regenerative action.
- The inability of very narrow pulses to progress through the power stage.
- Voltage pulse height variation with load current (Similar to DC link ripple in a conventional Class-D power stage).

The distortion due to pulse height increase during regenerative action can be minimised by using an 'intelligent' secondary snubber. The snubber would monitor the typical pulse height from the secondary winding and adjusts its clamp level to always be a small amount higher. Voltage pulse height variation whilst potentially causing significant distortion is unlikely to be as dominant as the inability of narrow voltage pulses to progress through the power stage.

In order to examine the impact of the narrow pulse exclusion, the linearity of the power stage was measured in much the same way as adopted in Chapter 3. The input demand was varied to cover the full range of allowable modulation depths and the average (or DC) output current was measured. The load consisted of a $100\mu\text{H}$ inductor in series with a 16Ω resistor and Figure 6.21 shows the linearity up to the maximum allowable modulation depth.

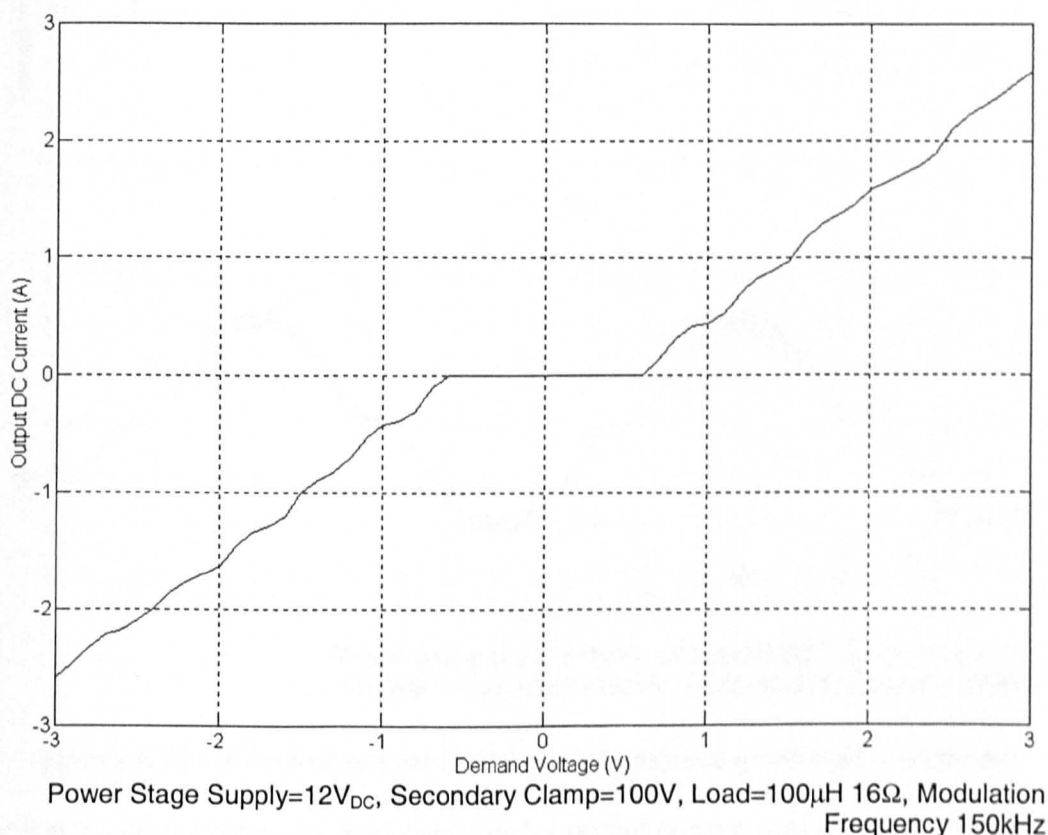


Figure 6.21 - DC linearity curve

The demand voltage magnitude of 3V corresponds to an operation pulse duty cycle of approximately 75%, which is the maximum attainable from the power stage. The inability of narrow pulses to progress through the power stage is evident from the large dead band symmetrical around zero demand. Outside this dead band, the power stage shows near linear behaviour. This non-linearity is unfortunately at the centre of the linearity characteristic and will lead to high harmonic distortion in practice. Indeed, it will demonstrate very similar distortion behaviour to that found in an unbiased Class C linear output stage.

The load current for a low frequency demand signal was measured to demonstrate the affect of the non-linearity on a sine-wave and Figure 6.22 shows the demand signal (a) and the output load current (b).

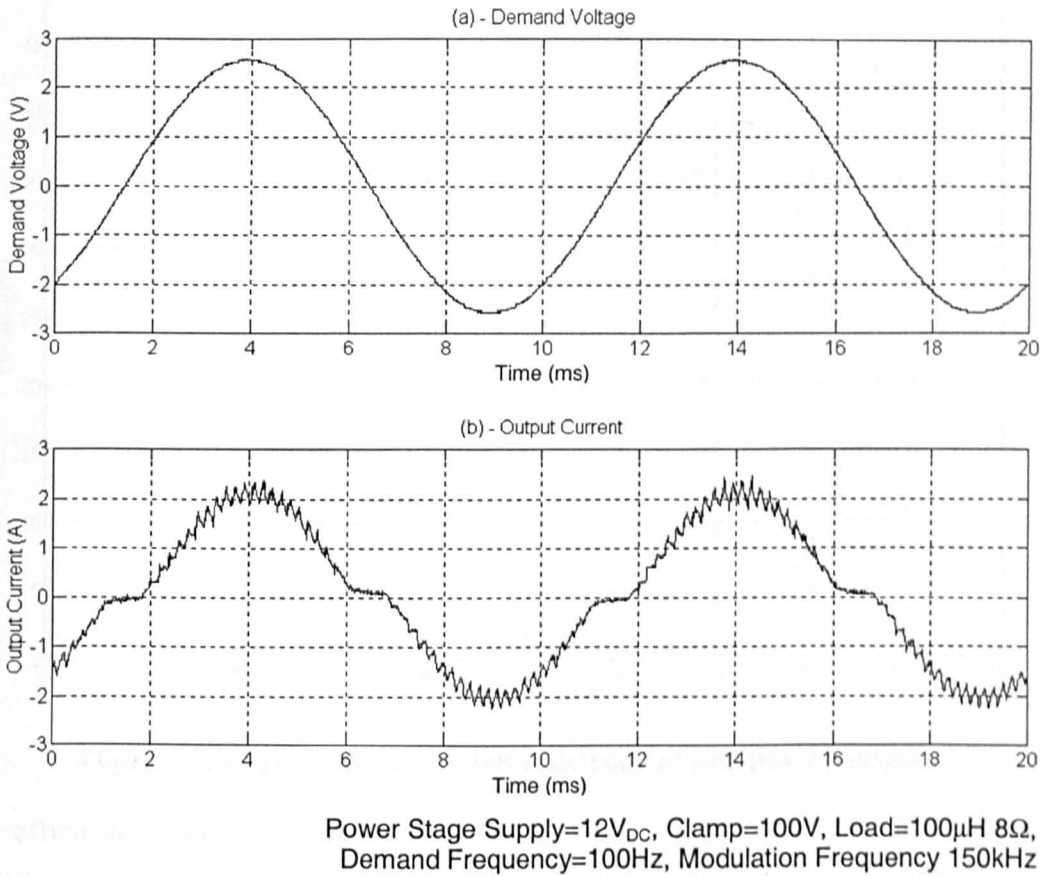


Figure 6.22 - Effect of narrow pulse disappearance on sinewave demand

The non-linearity causes the dead bands in the output current profile and these will lead to odd-order harmonic distortion.

6.5 Operational Efficiency

The power conversion efficiency of the primary side through the main power transformer was demonstrated at above 80%, Figure 5.47. In practice, the reactive nature of the output filter and load will result in a net power flow back through the secondary side snubber resulting in a lowering of the overall efficiency.

Under PDM and closed loop control, the conversion efficiency with a fourth order filter and 4Ω termination was measured. This initial test was undertaken at low power with a 5V main DC supply. With a pulse duty cycle of 70%, this should lead to an average power output of 100W at full modulation depth. Figure 6.23 gives the efficiency as a function of modulation depth for this load. The efficiency was measured using a high

bandwidth power analyser with the input power taken as the power drawn from the main DC supply and the output as the AC power in the load, after the power filter.

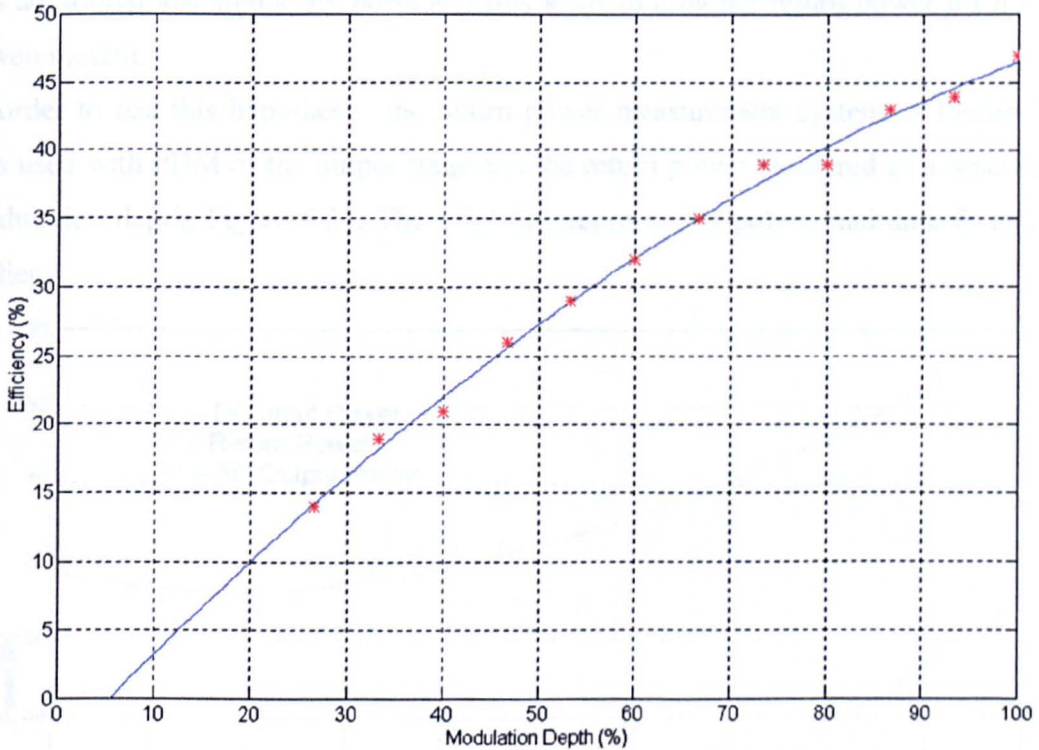


Figure 6.23 - Overall conversion efficiency at low power output

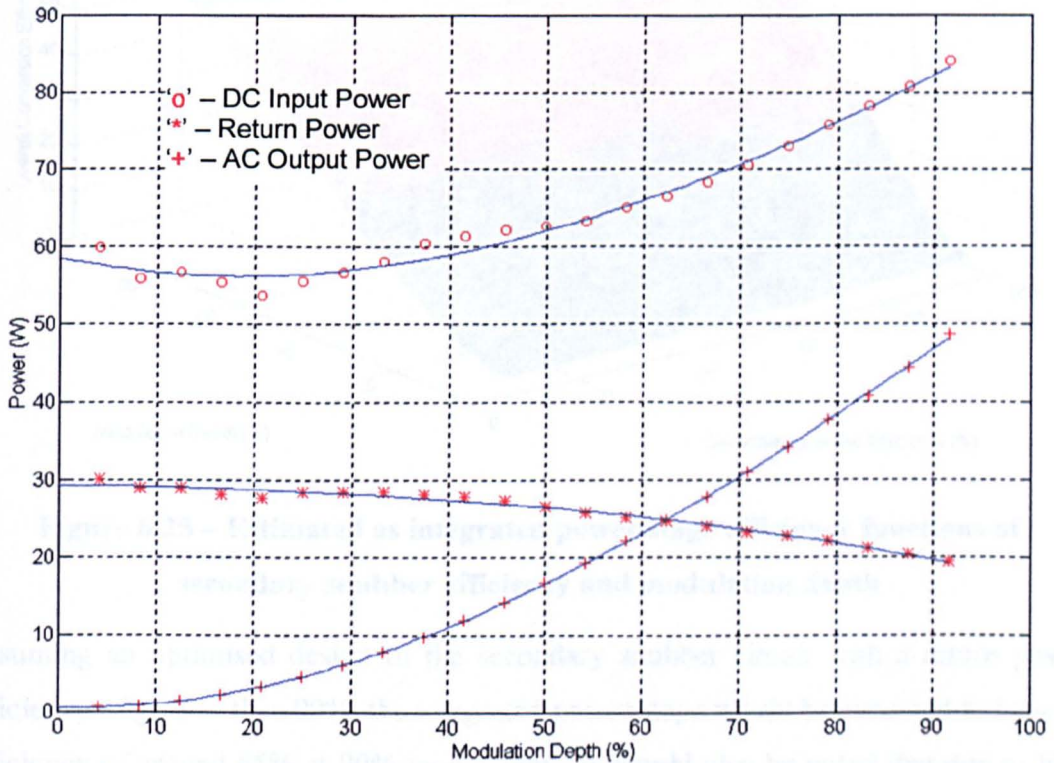
This efficiency profile unfortunately demonstrates poor performance of the overall amplifier system. Since the forward conversion path has been demonstrated to operate efficiently, the poor performance must be due to two main factors: -

- Loss in the power filter
- Excessive loss in the secondary side snubber.

The series resistance of the filter was measured at $200\text{m}\Omega$ and for a 4Ω load, this represents an efficiency drop of 5%. Furthermore, in practice, the filter inductors immediately after the power stage also carry a relatively high ripple current at the switching frequency and this leads to a small additional loss. At present, the secondary side snubber is not optimised and in practice, it showed excessive loss. The snubber also appears to be under-rated since operation at the full 12V DC link voltage with a reactive load has resulted in its destruction on a number of occasions. One reason for a larger than expected return power is the nature of the PDM output spectra. Whereas the PWM output consists of the fundamental frequency, the switching frequency and harmonics

around the switching frequency, the PDM spectrum contains significantly more energy at low frequencies in addition to the fundamental signal. The power filter has to filter this additional low frequency noise and this leads to a higher return power for a PDM driven system.

In order to test this hypothesis, the return power measurement system of Figure 5.35 was used with PDM of the output stage and the return power measured as a function of modulation depth, Figure 6.24. The solid line represents a polynomial data fit as used earlier.



H-Bridge Supply=30V, Return Clamp=31V, Load =Fourth Order Filter with 4Ω Loudspeaker, Demand Frequency=100Hz, Clock frequency=300kHz, Dead Time=400nS, First Order Modulator, Closed Loop Operation

Figure 6.24 - Measured input, output and return power levels under PDM

The profiles of Figure 6.24 support the argument that the return power level under PDM is significantly greater than that in the equivalent PWM modulator. Indeed, the clamp return power is typically 60% of the full output power and remains close to this level over the full range of modulation depths. Consequently, a poor efficiency of the energy return snubber will severely compromise the operation efficiency of the new power stage and is the cause of the results in Figure 6.23.

Using the measured data of Figure 6.24, the amplifier efficiency was estimated as a function of modulation depth and efficiency of the secondary side snubber circuit, Figure 6.25.

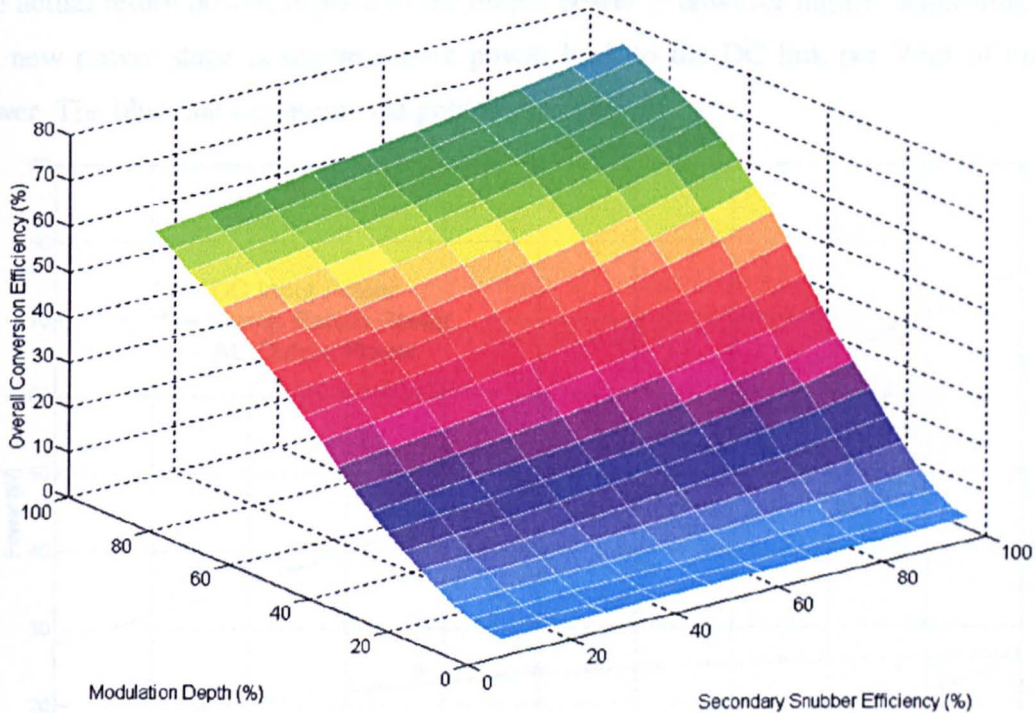
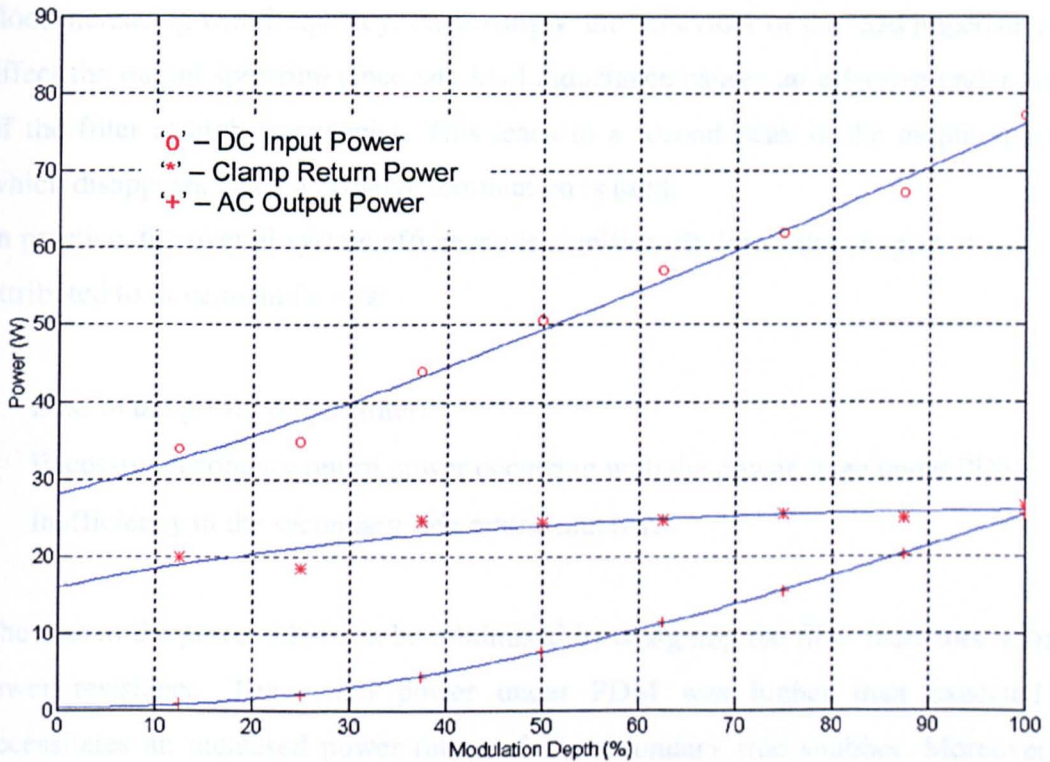


Figure 6.25 – Estimated as integrated power stage efficiency functions of secondary snubber efficiency and modulation depth

Assuming an optimised design of the secondary snubber circuit with a return power efficiency of greater than 90%, the integrated power stage would be expected to have an efficiency of around 65% at 90% modulation. It should also be noted that due to high levels of return power, it was only possible to test the amplifier at maximum output powers \approx 50W, Figure 6.24. At higher output powers a further improvement in efficiency would be expected

In order to compare the conventional Class-D power stage and the new power stage, the secondary side snubber was removed from the new power stage and the linear active clamp circuit connected in its place. This allows for direct measurement of the return power in the new power stage under a PDM regime. The measurement conditions were maintained as for the H-Bridge power measurements and with a 5V main link voltage, the measured pulse heights at the power stage output were 37V. Consequently, the linear active clamp circuit was set to 40V. The duty cycle was set to 70%, giving 25W

output power at maximum modulation depth. Figure 6.26 shows the measured powers up to full modulation depth. The relative levels of power flow in the new power stage under PDM show a similar behaviour to those of the normal H-Bridge in Figure 6.24. The actual return power, relative to the output power is however higher, suggesting that the new power stage is sending more power back to the DC link per Watt of output power. The blue line represents the polynomial data fit.



DC Supply=5V, Active Clamp=40V (Normal Pulse Height=37V),
Load =Fourth Order Filter with 4Ω Loudspeaker,
Demand Frequency=100Hz, Clock frequency=300kHz, Closed Loop Operation

Figure 6.26 - Measured power flow in new power stage under PDM

6.6 Conclusions

Modulation of the new power stage has been demonstrated under both PWM and PDM modulation schemes. Distortion under both modulation schemes distortion occurs as a result of the increased output voltage during regenerative power flow through the secondary side snubber. The distortion has been shown to be strong function of the voltage clamp level and therefore the use of an intelligent snubber, which tracks the normal voltage pulse height, will assist in minimising this form of distortion. PWM operation is further compromised due to the inability of narrow pulses to progress through the power stage.

Closed loop operation under PDM has demonstrated that the power stage can deliver a THD figure of 0.5% and although this is above the desired 0.1%, further improvements to the differential amplifier in the feedback loop will lower this figure. The differential probe used in the present feedback loop was prone to EMI interference and this is likely to raise the harmonic distortion.

Under closed loop PDM operation, the power stage output spectrum showed the noise floor increasing with frequency. Interestingly, the behaviour of the load impedance does affect the output spectrum since any load inductance causes an effective under-loading of the filter at high frequencies. This leads to a second peak in the output spectrum, which disappears when a resistive termination is used.

In practice, the overall system efficiency is significantly lower than expected and this is attributed to three main factors: -

- Loss in the power output filter.
- Excessive secondary return power occurring with the power stage under PDM.
- Inefficiency in the secondary side return snubber.

The loss in the power filter can be minimised by designing the filter inductors to have a lower resistance. The return power under PDM was higher than expected and necessitates an increased power rating of the secondary side snubber. Moreover, the efficiency of this snubber is critical to system efficiency and should be considered more closely. Since the return power is so high relative to the output power, the argument for using the amplifier with the bi-directional power transformer is strengthened. Here, the highly efficient forward conversion path is used to send the regenerative energy back to the primary and this should yield an increase in efficiency. A small energy recovery snubber will be required, however, to provide an energy return path between the primary side switching off and the output H-Bridge freewheeling the load current.

7 Summary and Conclusions

This thesis has described the results of applying switched-mode techniques to the development of a high power car audio amplifier. The present linear amplifiers have been shown to be at best 50% efficient with the efficiency dropping significantly with the reactive loads found in practice. Alternative linear designs have been highlighted which can offer higher conversion efficiency although the extra complexity involved is considered prohibitive. Literature reports that Class-D amplification can yield conversion efficiencies beyond 80% and the application of this technology to a car audio system would result in a smaller, lighter and cheaper amplifier.

A further requirement of the car audio amplifier is a front-end switched mode power supply to provide the high voltage DC rails for the amplifier. In practice the power supply and associated output filter represents over 50% of the volume and cost of the amplifier, and introduces a further element of loss. The thesis explores methods of combining the power supply and a switching amplifier to reduce the overall size, component count and cost of the amplifier system, whilst improving its efficiency.

Traditionally, a PWM scheme is used to modulate the switches in the power output stage and in theory, can offer the required performance for a realistic switching frequency of 140kHz. In practice however, PWM requires the output voltage pulses to be defined to an accuracy of $\pm 100\text{ps}$ and this is not attainable in a practical power stage. Signal processing techniques using noise-shaping can lessen this requirement although high accuracy is still required. Consequently, the practical Class-D power stages are more suited to the constant width pulses to be found with PDM. The use of single bit quantisation in PDM results in a highly linear modulation scheme. In order to achieve a minimum 60dB noise floor and 20kHz power bandwidth, it has been shown that a PDM modulator with at least a fourth order noise-shaper is required. Modulators of order greater than two can show unstable behaviour and therefore a new design methodology, based on a linear feedback system, has been explored. The methodology has resulted in stable modulators up to third order and it is believed that with a higher order model for the sample and hold element, stable modulators beyond third order will be attainable. The effective switching frequency of a PDM driven system has been shown to be

significantly less than for PWM. Therefore, a PDM system can be driven at up to 2.5 times the clock frequency of a PWM system for equivalent switching loss. At present, the second order modulator achieved in practice doesn't offer the required performance for a full bandwidth system and therefore the amplifier is more suited to a sub-woofer application.

The prototype H-Bridge constructed in Chapter 4 has verified that Class-D amplifiers can indeed offer conversion efficiency in excess of 80%. The switching times of the MOSFETs used in the power stage were measured at 75ns and this, combined with the 50ns reverse recovery of the freewheel diodes has shown that the switching loss is the dominant loss mechanism in the converter. Conduction loss in the output filter and devices is estimated to be equal to half the switching loss. Since the switching loss component is dominant, the capability of the gate drive circuitry used in practice has been shown to have a critical influence on overall efficiency, with efficiency variations of greater than 20% seen between different gate drive systems.

The practical operation of a Class-D amplifier does not provide an ideal replication of the input switching signal and this distortion can have a significant effect on the fidelity of the system. Of the distortion mechanisms highlighted, the necessary use of dead time is the major cause of power stage non-linearity. The uncontrolled current during the dead time not only reduces the output signal level but also introduces high levels of odd-order harmonic distortion. A model has been developed which can predict the level of open loop THD under PWM control. For a practical power stage switching at 140kHz, the use of 200ns dead time results in a peak THD of 8%. It is difficult to reduce the dead time much below 200ns and therefore this gives an indication of the likely open loop performance of the power stage.

Under PDM, the THD is more difficult to predict although empirical measurements suggest that the PDM scheme is less susceptible to dead time distortion. A secondary cause of harmonic distortion in a practical amplifier is the effect of poor DC link compliance.

Reactive power flow between the load and the amplifier causes the DC link to fluctuate at twice the signal frequency, resulting in a 2nd and other even order harmonic terms to

appear in the output spectrum. These levels, however, are significantly less than those introduced by dead time and can be minimised with the use of a large link capacitor.

Reduction of the distortion to acceptable levels has been achieved through closed loop operation. Feedback schemes which operate on a cycle by cycle basis offer the highest attenuation of the harmonic distortion and this is easily achieved for PDM by simply feeding back the power stage output to the modulator input. This technique has resulted in a factor of 20 reduction in the THD for a PDM system.

The main focus of the research presented in this thesis is concerned with the development of a new power stage topology specifically for in-car audio use. To this end, a power stage was developed which removes the requirement for an intermediate high DC voltage supply and reservoir capacitor. Removal of this stage has resulted in a physically smaller system, which uses approximately half the number of decoupling capacitors found in the present system. Moreover, removal of this DC stage has allowed for soft switching of the output stage. In practice, the major design problems encountered with the development of this power stage were related to the energy stored in parasitic inductances in the circuit and providing an efficient path for the reactive energy in the loudspeaker load to be returned to the input supply.

Through careful circuit design and the use of integrated magnetics, the primary side parasitic inductance was reduced to 16% of the level of the initial prototype circuit. The integrated nature of the transformer also eases fabrication of the power stage since the windings are realised on the PCB. Recapture of the energy stored in the transformer leakage inductance was achieved with an active snubber which also removes the need for an extra demagnetisation winding on the transformer. Furthermore, the snubber allows for a duty cycle of up to 70% and this has been shown to increase the efficiency of the power conversion process. Again, the performance of the gate drive circuitry has been shown to significantly influence the conversion efficiency, in this case by as much as 10%. The optimal design of the primary side of the converter has resulted in a forward conversion path, with an efficiency, which peaks at 88% and is above 80% between 30W and 300W output.

Since reactive energy is transferred cyclically between the amplifier and its load, removal of the intermediate DC stage and its energy storage capacitors has presented the need for an energy return path to the primary 12V supply. The power-rating requirement for the return path was found through measurements and differs significantly for PWM and PDM. Other than the fundamental output signal, the PWM spectrum mainly contains energy at high frequency. This high frequency component produces only a small amount of return power PWM. Thus, for PWM, the fundamental signal frequency component is the dominant cause of return power.

Under PDM, there is significant spectral energy at low frequency and this leads to a high level of return power. The magnitude of the return power was underestimated in the integrated power stage design and the use of an active snubber has resulted in inefficient operation. Optimisation of this snubber or the use of the bi-directional power transformer circuit should increase the initially disappointing efficiency. However, assuming a capability of providing an efficient return path for the load reactive energy, the overall efficiency of the proposed integrated power stage was estimated to exceed 65%.

The new power stage was run under both open and closed loop operation with the level of the secondary side active clamp being significant in the cause of distortion. Again, the second order modulator gave 35dB dynamic range for a 20kHz bandwidth and this could be improved with a higher order design.

Future Work

There are a number of areas in which further research should improve the performance of the new amplifier.

1. Further development of the high order $\Delta\Sigma$ modulator design through the use of a high order Pade approximation to the sample and hold modulator element. Also, the power stage introduces a small time delay, equal to the dead time, which will

influence the closed loop stability of the amplifier. This delay should be included in the modulator design to ensure a stable system.

2. The output filter at present has an output resistance of $200\text{m}\Omega$, which leads to excessive loss in the filter inductors. This filter resistance should be decreased by either using a heavier gauge wire or by using inductors with ferrite cores to reduce the copper loss.
3. Improving the return power efficiency, such that it is similar to that of the main forward conversion path. This can be achieved by either employing bi-directional transformer circuit or by increasing the power rating and efficiency of the secondary side snubber.
4. At present, the EMI produced by the power stage has not been measured and for a commercial system, this would need to be quantified.

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9 Appendix A – Mathematical Proofs

9.1 Working for Equations (2.1), (2.2) and (2.3)

The efficiency of the generic power stage shown in Figure 2.1 (repeated below) can be found through consideration of each of the transistors collector current and collector-emitter voltage.

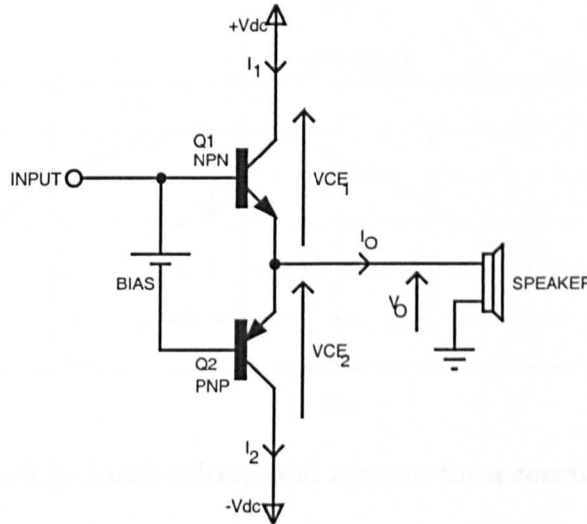


Figure 9.1 - Generic linear power stage

For an ideal power output stage (i.e. no cross-over problems and zero bias), the output load voltage and load current for a sinewave demand will be as shown in Figure 9.2.

Due to the symmetry of the system, the power dissipation in both devices will be similar and it is therefore sufficient to calculate the power lost in a single device over one cycle and then double it to yield the total power loss.

Consider the power lost in Q1. The device will only dissipate power when the load current is positive so the power lost in Q1 over a single cycle is: -

$$P_{LOSS} = \frac{1}{T} \int_{\frac{\phi}{\omega}}^{\frac{T+\phi}{2\omega}} V_{CE} I_C dt = \frac{1}{T} \int_{\frac{\phi}{\omega}}^{\frac{T+\phi}{2\omega}} (V_{DC} - V_p \sin(\omega t)) \times I_p \sin((\omega t) - \phi) dt$$

(9.1)

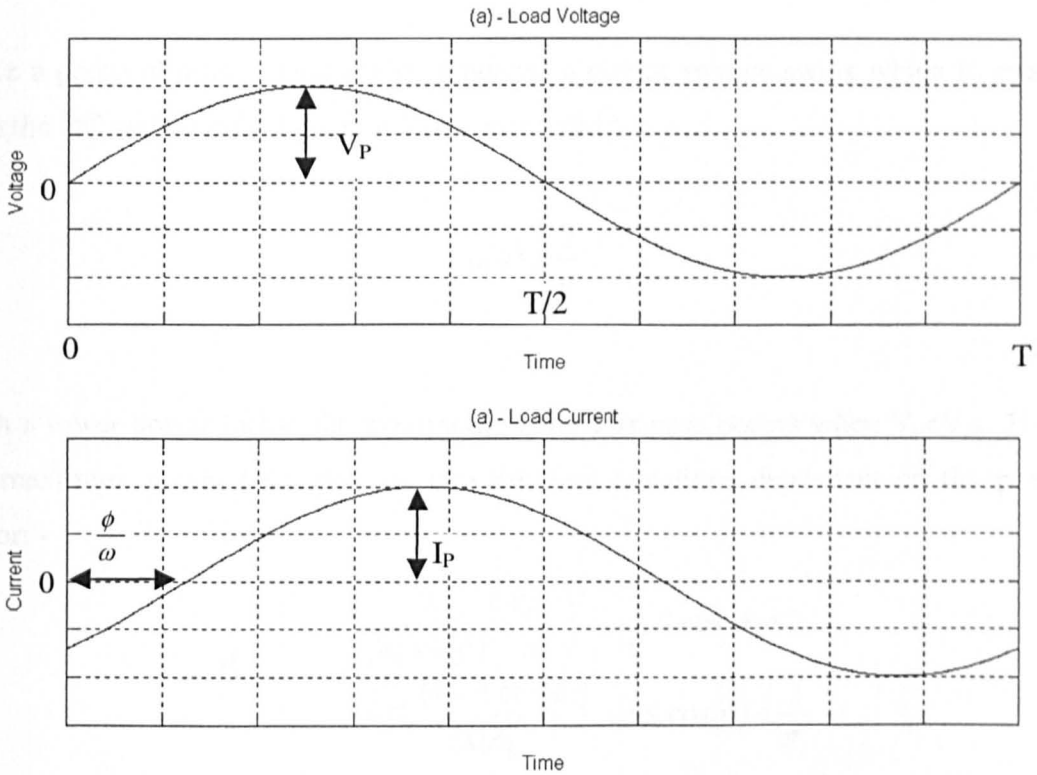


Figure 9.2 - Load voltage and current for a reactive load

Using $I_P = \frac{V_P}{|Z|}$, the power loss in a single device is: -

$$P_{Loss} = \frac{4V_P V_{DC} - V_P^2 \pi \cos(\phi)}{4\pi|Z|} \quad (9.2)$$

Therefore, the total power loss in the output stage is: -

$$P_{Loss} = \frac{4V_P V_{DC} - V_P^2 \pi \cos(\phi)}{2\pi|Z|} \quad (9.3)$$

The maximum level of power dissipation can be found through differentiation of P_{Loss} and occurs when: -

$$V_P = \frac{2V_{DC}}{\pi \cos(\phi)} \quad (9.4)$$

Since a practical power stage cannot produce an output voltage swing which is greater than the DC supply rails, Equation 8.4 is only valid for: -

$$\cos(\phi) \geq \frac{2}{\pi} \quad (9.5)$$

With a lower power factor, the maximum power loss case occurs when $V_p = V_{dc}$. Thus, the maximum power loss takes on two different equations dependent on the power factor: -

$$P_{LOSS} \Big|_{MAX} = \begin{cases} \frac{2}{|Z| \cos(\phi)} \left(\frac{V_{DC}}{\pi} \right)^2 & \frac{2}{\pi} \leq \cos(\phi) \leq 1 \\ \frac{V_{DC}^2 (4 - \pi \cos(\phi))}{2\pi |Z|} & 0 \leq \cos(\phi) < \frac{2}{\pi} \end{cases} \quad (9.6)$$

The power stage efficiency can be found simply by considering the total output power as: -

$$P_{OUT} = \frac{\hat{V}^2}{2|Z|} \cos(\phi) \quad (9.7)$$

Therefore, the conversion efficiency is: -

$$Efficiency, (\%) = \frac{100 \times P_{OUT}}{P_{OUT} + P_{LOSS}} = 25\pi \frac{V_p}{V_{DC}} \cos(\phi) \quad (9.8)$$

9.2 Working for Equations (4.6) and (4.7)

The solution presented in Equations (4.6) and (4.7) is found through Fourier analysis of the error voltage defined over a fundamental cycle as: -

$$V_{error}(t) = V_{DC} \times \left\{ \begin{array}{ll} 0 & -\frac{T}{2} \leq t < -\frac{T}{2} + t_1 \\ -(2k + m \sin(\omega t)) & -\frac{T}{2} + t_1 \leq t < -\frac{T}{2} + t_2 \\ 2\delta & -\frac{T}{2} + t_2 \leq t < -t_2 \\ -(2k + m \sin(\omega t)) & -t_2 \leq t < -t_1 \\ 0 & -t_1 \leq t < t_1 \\ 2k - m \sin(\omega t) & t_1 \leq t < t_2 \\ -2\delta & t_2 \leq t < \frac{T}{2} - t_2 \\ 2k - m \sin(\omega t) & \frac{T}{2} - t_2 \leq t < \frac{T}{2} - t_1 \\ 0 & \frac{T}{2} - t_1 \leq t < \frac{T}{2} \end{array} \right\} \quad (9.9)$$

Due to the odd-nature of this waveform and the fact it has no DC component, the solution is given by: -

$$V_{error}(t) = \sum_{n=1}^{\infty} b_n \sin(n\omega_0 t) \quad (9.10)$$

Where,

$$b_n = \frac{2}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} V_{error}(t) \times \sin(n\omega_0 t) dt \quad (9.11)$$

The simplest way to proceed is to find the Fourier integral for each of the components of $V_{error}(t)$ and then to combine them to find the overall solution. Furthermore, the solution for the component at the fundamental frequency ($n=1$) must be evaluated separately due to the nature of the solution.

Firstly, consider the solution for b_n when $n=1$.

$$b_1 = \frac{2}{T} \int_{\frac{T}{2}}^{\frac{T}{2}} V_{error}(t) \times \sin(\omega t) dt = \frac{2V_{DC}}{T} \left\{ \begin{array}{l} \int_{\frac{T}{2}+t_2}^{\frac{T}{2}+t_1} -(2k + m \sin(\omega t)) \sin(\omega t) dt \quad (a) \\ \int_{\frac{T}{2}+t_2}^{-t_2} 2\delta \sin(\omega t) dt \quad (b) \\ \int_{\frac{T}{2}+t_2}^{-t_1} -(2k + m \sin(\omega t)) \sin(\omega t) dt \quad (c) \\ \int_{-t_2}^{t_2} (2k - m \sin(\omega t)) \sin(\omega t) dt \quad (d) \\ \int_{\frac{T}{2}-t_2}^{t_1} -2\delta \sin(\omega t) dt \quad (e) \\ \int_{\frac{T}{2}-t_1}^{t_2} (2k - m \sin(\omega t)) \sin(\omega t) dt \quad (f) \\ \int_{\frac{T}{2}-t_2} \end{array} \right.$$

(9.12)

The solutions are: -

$$(a) = \frac{1}{8\pi} (8kT(\cos(\omega t_1) - \cos(\omega t_2)) + mT(\sin(2\omega t_2) - \sin(2\omega t_1)) + 4m\pi(t_1 - t_2))$$

(9.13)

$$(b) = \frac{-2T\delta}{\pi} \cos(\omega t_2)$$

(9.14)

$$(c) = \frac{1}{8\pi} (8kT(\cos(\omega t_1) - \cos(\omega t_2)) + mT(\sin(2\omega t_2) - \sin(2\omega t_1)) + 4m\pi(t_1 - t_2))$$

(9.15)

$$(d) = \frac{1}{8\pi} (8kT(\cos(\omega t_1) - \cos(\omega t_2)) + mT(\sin(2\omega t_2) - \sin(2\omega t_1)) + 4m\pi(t_1 - t_2))$$

(9.16)

$$(e) = \frac{-2T\delta}{\pi} \cos(\omega t_2)$$

(9.17)

$$(f) = \frac{1}{8\pi} (8kT(\cos(\omega t_1) - \cos(\omega t_2)) + mT(\sin(2\omega t_2) - \sin(2\omega t_1)) + 4m\pi(t_1 - t_2)) \quad (9.18)$$

Fortunately, these part solutions are similar so the overall solution is relatively simple: -

$$b_{n=1} = \frac{V_{dc}}{\pi} (8k(\cos(\omega t_1) - \cos(\omega t_2)) + m(\sin(2\omega t_2) - \sin(2\omega t_1)) + 2m(\omega t_1 - \omega t_2) - 8\delta \cos(\omega t_2)) \quad (9.19)$$

Using,

$$\sin(\omega t_1) = \frac{2k}{m} \quad \text{and} \quad \sin(\omega t_2) = \frac{2(k + \delta)}{m}$$

This simplifies to: -

$$b_{n=1} = \frac{4V_{dc}}{\pi} \left(k(\cos(\omega t_1) - \cos(\omega t_2)) + \frac{m}{2}(\omega t_1 - \omega t_2) - \delta \cos(\omega t_2) \right) \quad (9.20)$$

For the higher order harmonics, the analysis is identical except that b_n is defined as: -

$$b_n = \frac{2}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} V_{error}(t) \times \sin(n\omega t) dt = \frac{2V_{DC}}{T} \left\{ \begin{array}{l} \int_{-\frac{T}{2}+t_2}^{-\frac{T}{2}+t_1} -(2k + m \sin(\omega t)) \sin(n\omega t) dt \quad (a) \\ \int_{-\frac{T}{2}+t_1}^{-t_2} 2\delta \sin(n\omega t) dt \quad (b) \\ \int_{-\frac{T}{2}+t_2}^{-t_1} -(2k + m \sin(\omega t)) \sin(n\omega t) dt \quad (c) \\ \int_{-t_2}^{t_2} (2k - m \sin(\omega t)) \sin(n\omega t) dt \quad (d) \\ \int_{t_1}^{\frac{T}{2}-t_2} -2\delta \sin(n\omega t) dt \quad (e) \\ \int_{\frac{T}{2}-t_1}^{\frac{T}{2}-t_2} (2k - m \sin(\omega t)) \sin(n\omega t) dt \quad (f) \end{array} \right. \quad (9.21)$$

The part solutions are now: -

$$(a) = \frac{-\cos(n\pi)}{n\omega(n^2-1)} \left(\begin{array}{l} 2k(1-n^2)(\cos(n\omega t_2) - \cos(n\omega t_1)) \\ + mn^2(\cos(n\omega t_2)\sin(\omega t_2) - \cos(n\omega t_1)\sin(\omega t_1)) \\ + mn(\sin(n\omega t_1)\cos(\omega t_1) - \sin(n\omega t_2)\cos(\omega t_2)) \end{array} \right) \quad (9.22)$$

$$(b) = \frac{2\delta}{n\omega} \cos(n\omega t_2)(\cos(n\pi) - 1) \quad (9.23)$$

$$(c) = \frac{1}{n\omega(n^2-1)} \left(\begin{array}{l} 2k(1-n^2)(\cos(n\omega t_2) - \cos(n\omega t_1)) \\ + mn^2(\cos(n\omega t_2)\sin(\omega t_2) - \cos(n\omega t_1)\sin(\omega t_1)) \\ + mn(\sin(n\omega t_1)\cos(\omega t_1) - \sin(n\omega t_2)\cos(\omega t_2)) \end{array} \right) \quad (9.24)$$

$$(d) = \frac{1}{n\omega(n^2-1)} \left(\begin{array}{l} 2k(1-n^2)(\cos(n\omega t_2) - \cos(n\omega t_1)) \\ + mn^2(\cos(n\omega t_2)\sin(\omega t_2) - \cos(n\omega t_1)\sin(\omega t_1)) \\ + mn(\sin(n\omega t_1)\cos(\omega t_1) - \sin(n\omega t_2)\cos(\omega t_2)) \end{array} \right) \quad (9.25)$$

$$(e) = \frac{2\delta}{n\omega} \cos(n\omega t_2)(\cos(n\pi) - 1) \quad (9.26)$$

$$(f) = \frac{-\cos(n\pi)}{n\omega(n^2-1)} \left(\begin{array}{l} 2k(1-n^2)(\cos(n\omega t_2) - \cos(n\omega t_1)) \\ + mn^2(\cos(n\omega t_2)\sin(\omega t_2) - \cos(n\omega t_1)\sin(\omega t_1)) \\ + mn(\sin(n\omega t_1)\cos(\omega t_1) - \sin(n\omega t_2)\cos(\omega t_2)) \end{array} \right) \quad (9.27)$$

Note that (a)=(f), (b)=(e) and (c)=(d) and simplification gives: -

$$b_n = \left\{ \begin{array}{l} \frac{2V_{DC}(1 - \cos(n\pi))}{n\pi(n^2 - 1)} \left(\begin{array}{l} 2k(1 - n^2)(\cos(n\omega t_2) - \cos(n\omega t_1)) \\ + mn^2(\cos(n\omega t_2)\sin(\omega t_2) - \cos(n\omega t_1)\sin(\omega t_1)) \\ + mn(\sin(n\omega t_1)\cos(\omega t_1) - \sin(n\omega t_2)\cos(\omega t_2)) \end{array} \right) \\ + \frac{4V_{DC}\delta}{n\pi} \cos(n\omega t_2)(\cos(n\pi) - 1) \end{array} \right. \quad (9.28)$$

And therefore,

$$b_n = \frac{2V_{DC}(1 - \cos(n\pi))}{n\pi(n^2 - 1)} \left\{ \left(\begin{array}{l} 2k(1 - n^2)(\cos(n\omega t_2) - \cos(n\omega t_1)) \\ + 2n^2((k + \delta)\cos(n\omega t_2) - k\cos(n\omega t_1)) \\ + mn(\sin(n\omega t_1)\cos(\omega t_1) - \sin(n\omega t_2)\cos(\omega t_2)) \end{array} \right) \right. \\ \left. - 2\delta \cos(n\omega t_2)(n^2 - 1) \right\} \quad (9.29)$$

Hence,

$$b_n = \frac{4V_{DC}(1 - \cos(n\pi))}{n\pi(n^2 - 1)} \left(\begin{array}{l} + \frac{mn}{2}(\sin(n\omega t_1)\cos(\omega t_1) - \sin(n\omega t_2)\cos(\omega t_2)) \\ + \delta \cos(n\omega t_2) \\ + k(\cos(n\omega t_2) - \cos(n\omega t_1)) \end{array} \right) \quad (9.30)$$

9.3 Working for Equation (5.12)

For a reactive load driven by a sinusoidal voltage source, the phase shifted current flow causes a bi-directional power flow at twice the fundamental frequency of the driving voltage source as shown in Equation (9.31).

$$P(t) = \frac{\hat{V}^2}{2|Z|} (\cos \varphi - \cos(2\omega t - \varphi)) \quad (9.31)$$

Where \hat{V} is the peak applied voltage, $|Z|$ is the magnitude of the load impedance (at ω rad/s) and φ is the load phase shift in rad (at ω rad/s frequency). Figure 9.3 shows the nature of this power flow (in this case for a phase shift of $\pi/4$).

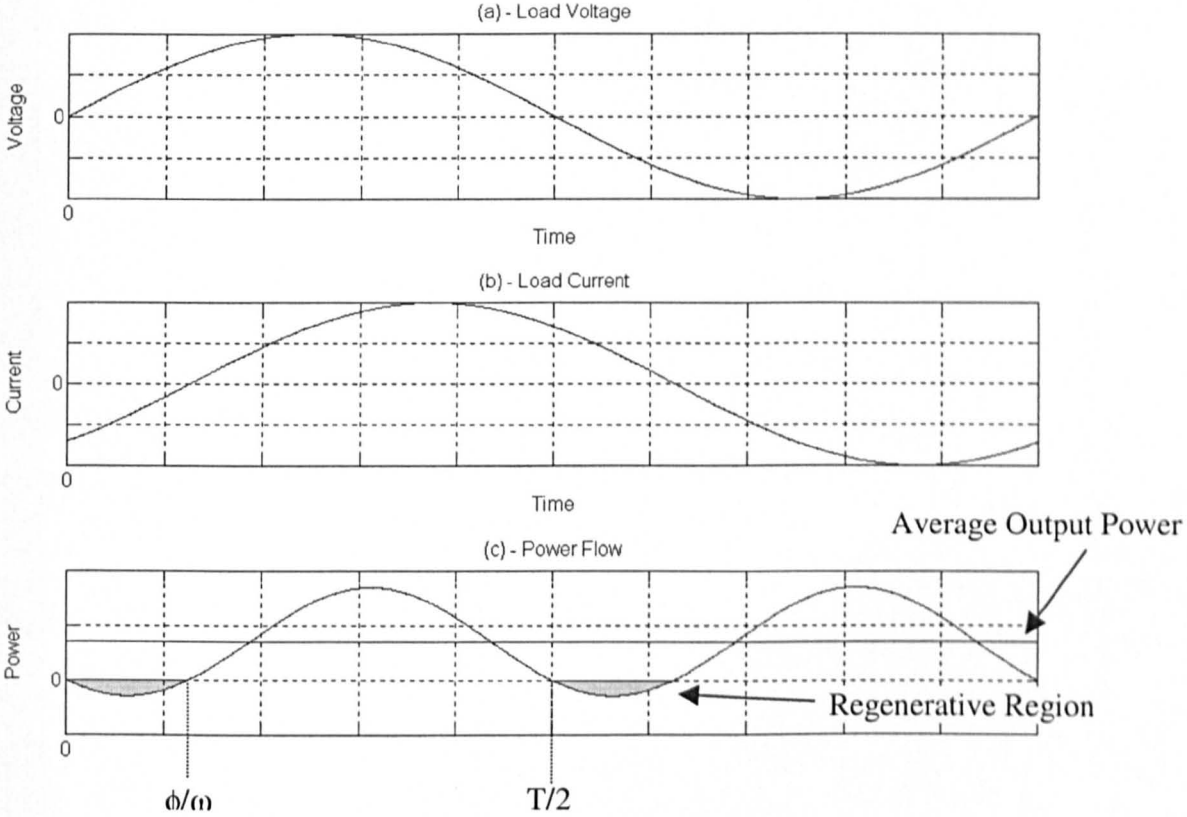


Figure 9.3 - Power flow in a reactive load

The level of return power can be found by calculating the energy returned during the regenerative period and averaging it over one cycle of the power flow waveform. Mathematically, this is equivalent to Equation (9.32) below.

$$P_{RETURN} = \frac{2}{T} \int_0^{\phi/\omega} \frac{\hat{V}^2}{2|Z|} (\cos \varphi - \cos(2\omega t - \varphi)) dt$$

(9.32)

Solution of (9.32) gives the return power as shown in (9.33) below.

$$P_{RETURN} = \frac{\hat{V}^2}{2\pi|Z|} |(\varphi \cos \varphi - \sin \varphi)| \tag{9.33}$$

The first design objective is to minimize the return loss. A higher return loss is preferable since it indicates a greater mismatch between the impedance of the antenna and the impedance of the feed line. This will result in a higher loss of power and a higher level of attenuation in the system. The second design objective is to maximize the level of radiation in the desired direction. This is achieved by maximizing the radiation pattern in the desired direction.



Figure 10: Radiation pattern of a horn antenna with different horn lengths.

The results in figure 10 show that the radiation pattern of the horn antenna is highly directional. The radiation intensity is highest in the direction of the horn's axis and decreases significantly as the angle theta increases. This is due to the geometry of the horn, which focuses the radiation into a narrow beam.

With a horn length of 100 cm, the radiation pattern is highly directional, with the main lobe centered at 0 degrees. As the horn length increases, the radiation pattern becomes narrower and more directional, with the main lobe becoming more pronounced and the side lobes becoming less significant. This is due to the geometry of the horn, which focuses the radiation into a narrow beam.

10 Appendix B - Filter Design

The first design choice is to decide what order filter to use. A higher order filter is preferable since it will offer increased attenuation of the switching frequency components. However, a higher order filter will be larger and will have a higher equivalent series resistance than a lower order filter. The graphs in Figure 10.1 show the level of attenuation achieved at the switching frequency for a number of different order filters and filter types.

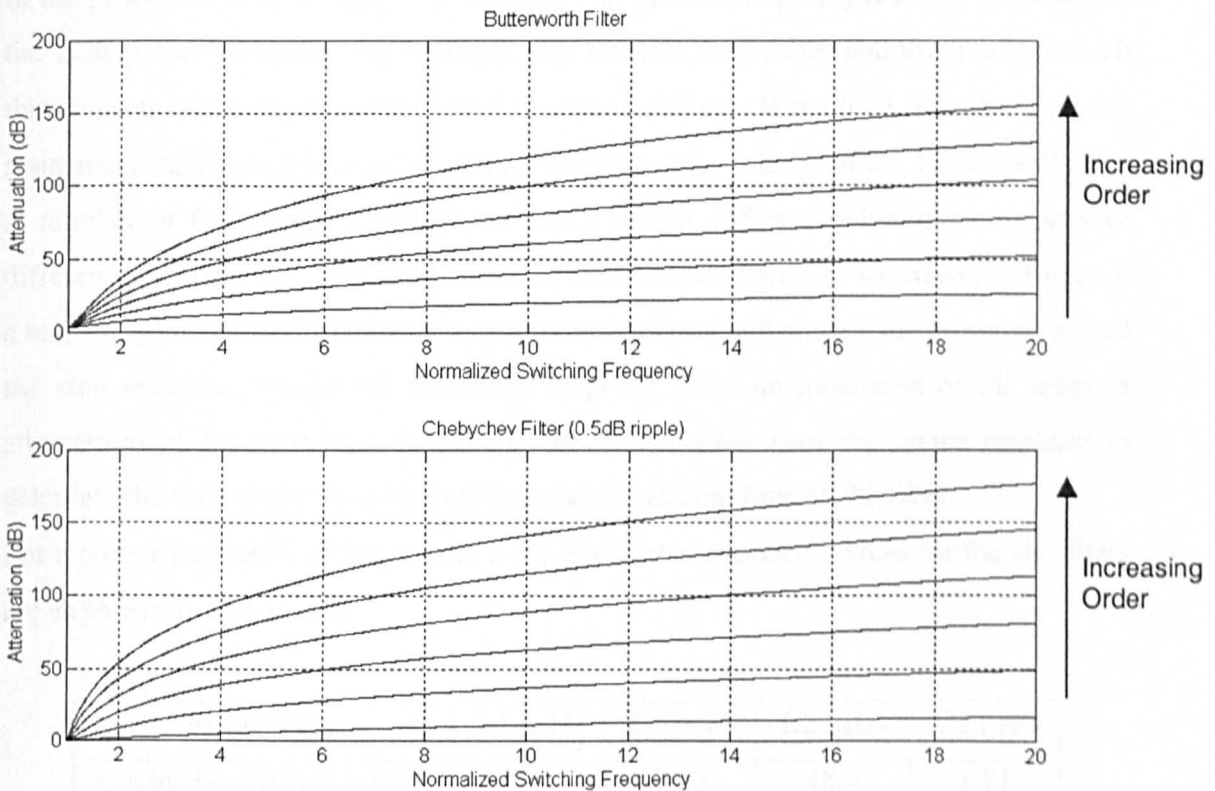


Figure 10.1 - Level of switching frequency attenuation with different order filters

The x-axis in Figure 10.1 represents the switching frequency normalised to the filter corner frequency. The six curves in each graph represent the attenuation profile for 1st to 6th order filters (with the 6th order giving the highest).

With both the PWM and PDM driven power stages, the likely switching frequency will be around 150kHz. For a low pass corner frequency of 20kHz, this will give from 20dB to 110dB attenuation with the Butterworth filters or 15dB to 130dB with the Chebychev filters. In [9.1], Himmelstoss utilises a fourth order filter which is likely to give around

70 to 80dB of attenuation with a 20kHz baseband and 150kHz switching frequency. A fourth order filter can be implemented as shown in Figure 10.2

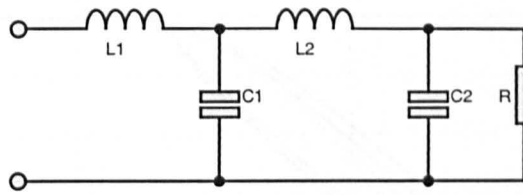


Figure 10.2 - Fourth order filter prototype

In the process of filter design, it is assumed that the load is purely resistive. In practice, the loudspeaker presents a very complicated reactive impedance and the level to which this impacts on filter performance will be discussed later. If the load is treated as a 4Ω resistance, standard tables can be used to find component values of L_1 , L_2 , C_1 and C_2 .

A number of filter types are available which utilise different polynomials to achieve different performances. Himmelstoss uses three design criteria in specifying a filter for a half bridge converter: frequency response (attenuation and phase), the group delay and the step response. Whilst the frequency response gives an indication of the level of attenuation of the switching frequency, the group delay uses the phase response to calculate the time delay for different frequencies passing through the filter.

For a corner frequency of 20kHz and a 4Ω load, the component values for the six filters are as shown in Table 10.1.

Filter Type	L_1 (μH)	C_1 (μF)	L_2 (μH)	C_2 (μF)
Chebyshev (0.5dB ripple)	45.7	3.75	48.4	1.81
Legendre	51.3	3.3	45.5	1.27
Butterworth	48.7	3.13	34.4	0.76
Linear Phase	48.4	2.07	23.5	0.58
Maximally Flat	47.8	1.94	19.5	0.42
Gaussian	46.2	1.67	15.6	0.36

Table 10.1 - Component values for the six filters

Whilst the value of inductor L_1 does not vary much between filter types, the other component values vary significantly between types. In terms of the physical size of the filter, the smaller the component values the better. In general, the Gaussian filter would

be the smallest. The attenuation characteristics of the six filters are shown in Figure 10.3. (Figure 10.3 to Figure 10.6 are reproduced from [9.1]).

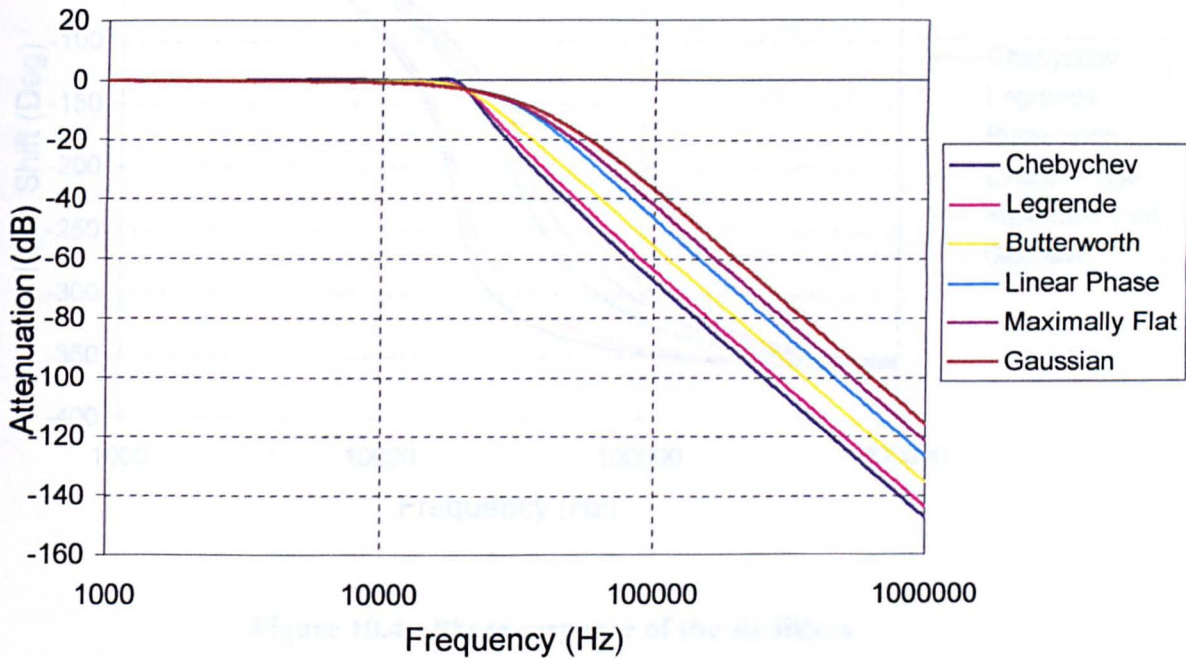


Figure 10.3 - Attenuation characteristics of the six filters

Of the six filters analysed, the Chebychev polynomials offer the largest attenuation of the switching frequency component. This, however, is at the expense of the pass-band ripple and poor phase characteristic. The phase response of the six filters is shown in Figure 10.4.

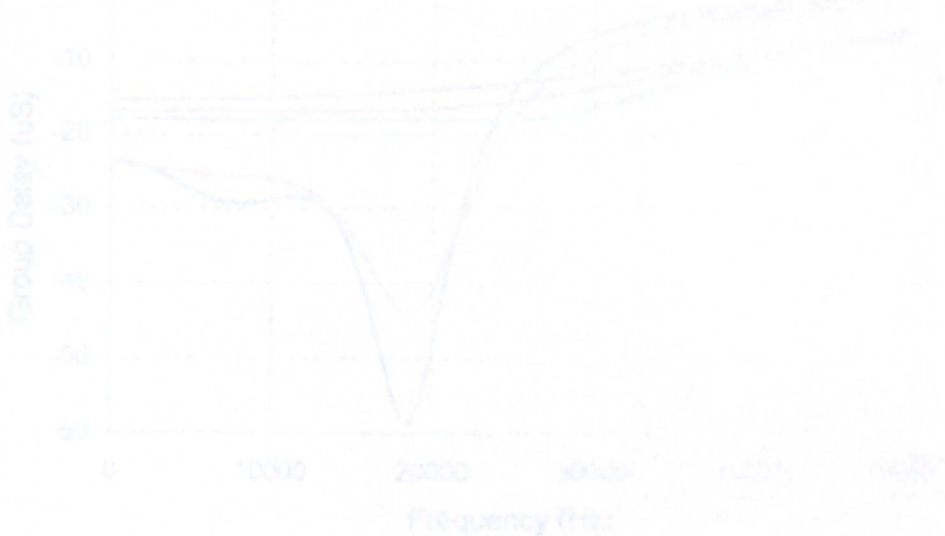


Figure 10.4 - Group delay of the six filters

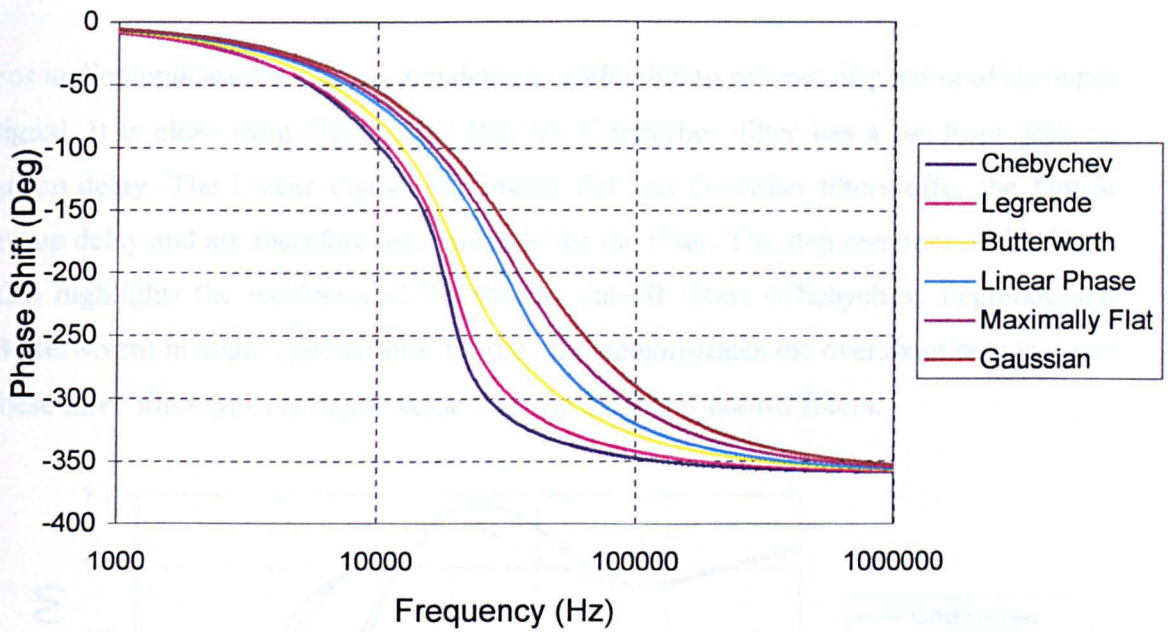


Figure 10.4 - Phase response of the six filters

The phase shift of the Chebychev filter is the highest and Figure 10.5 below shows the group delay of each filter type over the audio band. (The group delay effectively is the gradient of the phase response – a flat group delay indicating that all frequencies are delayed by exactly the same amount of time).

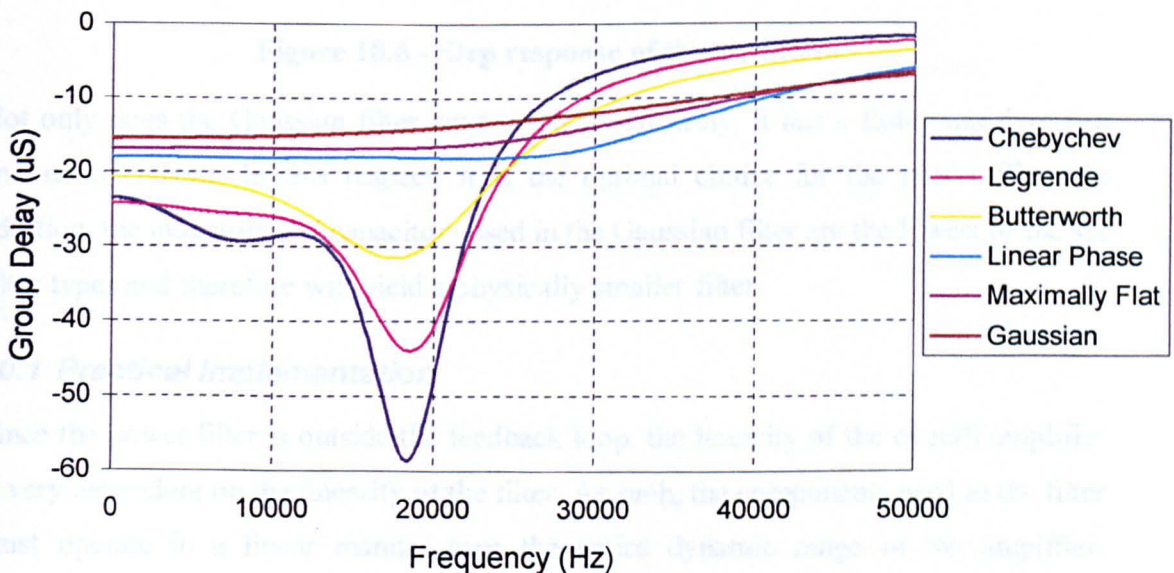


Figure 10.5 - Group delay of the six different filters

For audio applications, a flat group delay is preferable to prevent dispersion of the input signal. It is clear from Figure 10.5 that the Chebychev filter has a far from uniform group delay. The Linear Phase, Maximally flat and Gaussian filters offer the flattest group delay and are therefore most suitable for the filter. The step response of the filters also highlights the weakness of the sharper cut-off filters (Chebychev, Legendre and Butterworth) in audio applications. Figure 10.6 demonstrates the overshoot behaviour of these three filter types is much worse than the smoother cut-off filters.

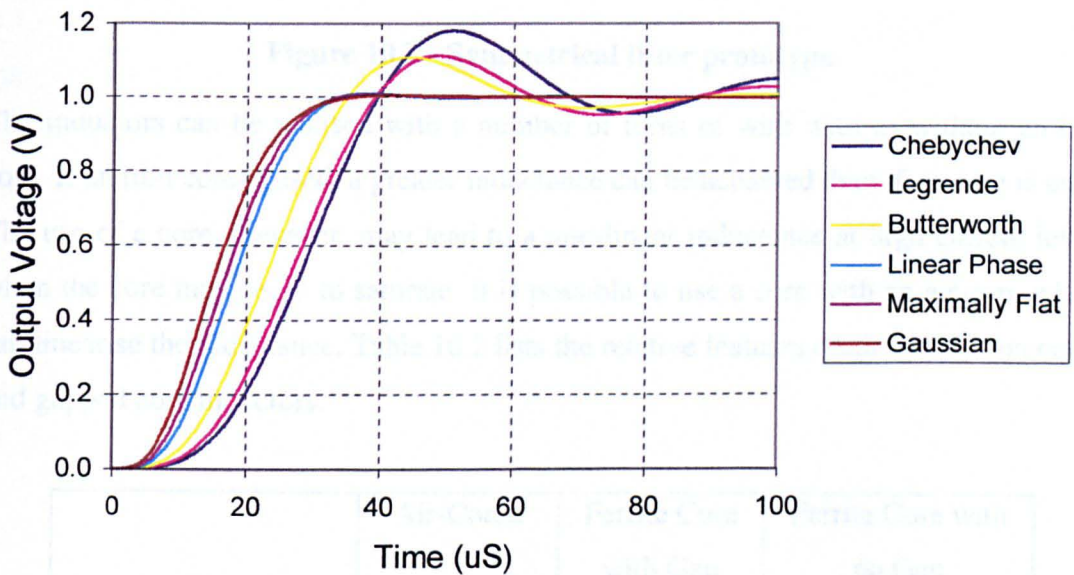


Figure 10.6 - Step response of the six filters

Not only does the Gaussian filter have a flat group delay, it has a faster transient rise and no overshoot. In this respect, it is the optimal choice for the power filter. In addition, the inductors and capacitors used in the Gaussian filter are the lowest of the six filter types and therefore will yield a physically smaller filter.

10.1 Practical Implementation

Since the power filter is outside the feedback loop, the linearity of the overall amplifier is very dependent on the linearity of the filter. As such, the components used in the filter must operate in a linear manner over the entire dynamic range of the amplifier. Polypropylene capacitors will offer very linear performance and low ESR and are readily available in the voltage and capacitance values required. The inductors, however, must be custom designed for the filter. Due to the low output load resistance,

the series resistance of the inductors must be as low as possible in order to achieve high efficiency. In order to achieve a symmetrical design, the circuit shown in Figure 10.2 can be adapted by halving the inductor values and using the circuit as shown in Figure 10.7.

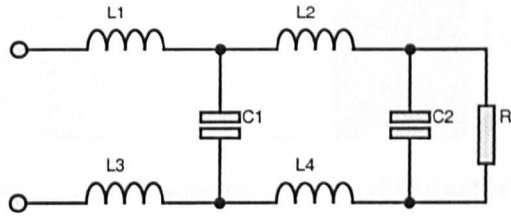


Figure 10.7 - Symmetrical filter prototype

The inductors can be realised with a number of turns of wire with or without an iron core. If an iron core is used, a greater inductance can be achieved than if no core is used. The use of a core, however, may lead to a non-linear inductance at high current levels when the core may begin to saturate. It is possible to use a core with an air-gap, which can linearise the inductance. Table 10.2 lists the relative features of air-cored, iron cored and gapped core inductors.

	Air-Cored	Ferrite Core with Gap	Ferrite Core with no Gap
Size	Largest	Middle	Smallest
Linearity	Most Linear	Middle	Least Linear
Leakage Flux (EMI)	Highest	Middle	Lowest

Table 10.2 - Relative Aspects of Inductor Types

The larger the air-gap, the more the inductor will behave like an air-cored device whilst the shorter the air-gap, the more the core material properties will dominate behaviour.

In order to maintain the linearity of the amplifier, it was decided that air-cored inductors would be used. If major EMI problems do result then the best solution would seem to be the use of a gapped core for the inductor.

The design of an air-core inductor is complicated by the fact that the field produced by this type of inductor can be large and therefore inductance calculation is somewhat difficult. Fortunately, previous work [9.2] using first principles, supported by empirical measurements has eased the design of air-cored inductors and in [9.3], Dickason gives

three equations from which it is possible to specify the inductor parameters completely. The equations are all based on the generic air-cored design where a solenoid type winding is used. Figure 10.8 shows a section through such an inductor.

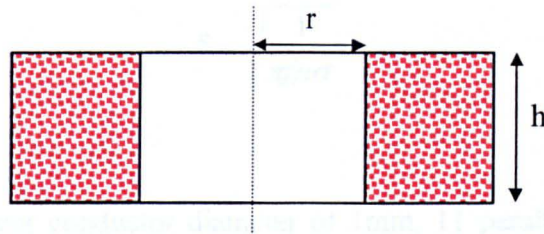


Figure 10.8 - Generic air cored inductor

Dickason gives the design equations for two inductor aspect ratios; $r=h$ and $r=2h$. The larger radius design is utilised when very small inductances are required and are difficult to achieve with the aspect ratio of $r=h$.

If the required inductance is L (μH), the DC resistance R (Ω), then the core parameters are as follows: -

$r = h$	$r = 2h$
$h = \sqrt{\left(\frac{L}{866R}\right)}$	$h = \sqrt{\left(\frac{L}{956R}\right)}$
$N = 6.28\sqrt{\left(\frac{L}{h}\right)}$	$N = 4.16\sqrt{\left(\frac{L}{h}\right)}$
$d = \frac{0.841h}{\sqrt{N}}$	$d = \frac{0.738h}{\sqrt{N}}$

Where all dimensions are in cm and N is the required number of turns. For the low values of filter inductance required, the $r=2h$ aspect ratio will be used. For the filter construction described in Figure 10.7, two $23.1\mu\text{H}$ and two $7.8\mu\text{H}$ inductors are required. With an allowable DC resistance of $50\text{m}\Omega$ per inductor, the required dimensions are $h=7\text{mm}$, $N=24$ turns and $d=1\text{mm}$ for the $23.1\mu\text{H}$ inductor and $h=4\text{mm}$, $N=18$ turns and $d=0.7\text{mm}$ for the $7.8\mu\text{H}$ inductor.

To minimise high frequency loss due to the skin effect, Litz wire must be used to wind the inductors. The skin depth can be calculated using Equation (10.1) and for copper at

a frequency of 150kHz, the skin depth is 0.17mm giving a maximum conductor diameter of 0.34mm. The closest available strand diameter is 0.3mm.

$$\delta = \sqrt{\frac{1}{\pi f \mu \sigma}} \quad (10.1)$$

To achieve an equivalent conductor diameter of 1mm, 11 parallel strands of 0.3mm-diameter wire are required and for the 0.7mm equivalent, 5 strands of 0.3mm wire are required. The required capacitance for each of the filter capacitance's was realised with the parallel connection of a number of polypropylene capacitors. Figure 10.9 shows the resulting filter prototype and test loudspeaker.

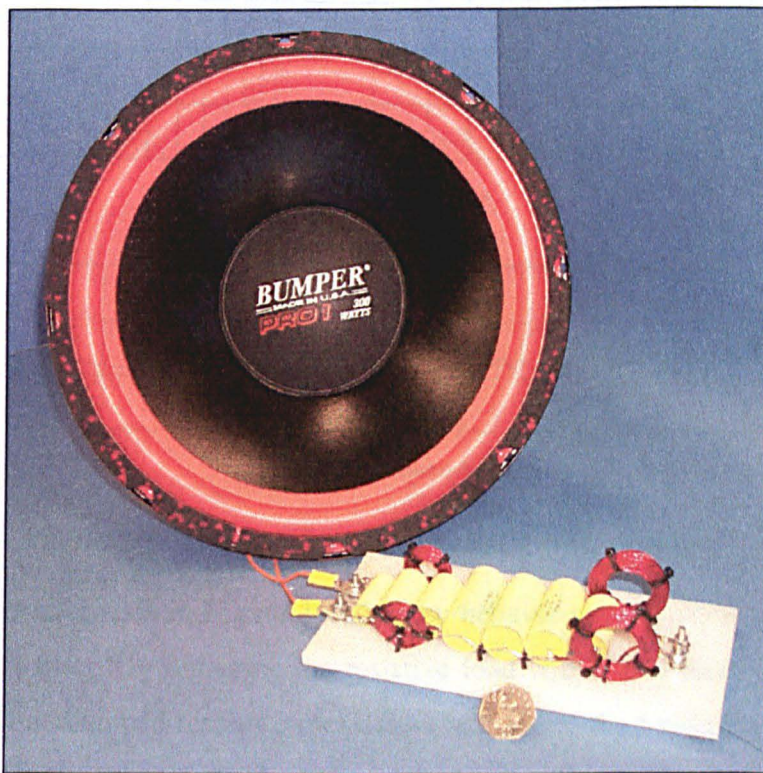


Figure 10.9 - Fourth order filter prototype and loudspeaker

The emphasis placed on making the filter as linear as possible has resulted in a physically large filter. The filter could be made smaller by using non-polarised electrolytic capacitors and ferrite cored inductors.

10.2 Characterisation

Using a real loudspeaker will result in a filter termination that is only resistive at very low frequencies. Consequently, the nature of the filter characteristic will be affected. Firstly, the small signal filter transfer characteristic with a 4Ω resistive termination is measured and Figure 10.10 shows the resulting gain, phase and group delay. The corresponding gain, phase and group delay as measured with a loudspeaker termination is shown in Figure 10.11.

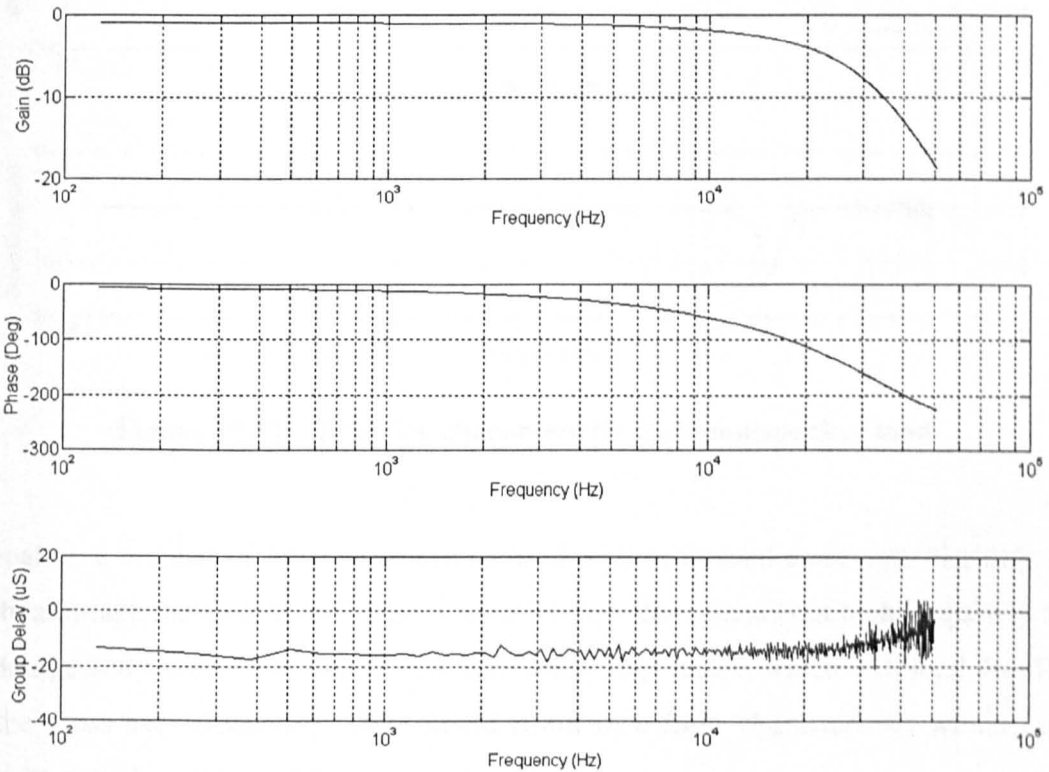


Figure 10.10 - Transfer characteristic with resistive load

The three characteristics in Figure 10.10 show behaviour very close to the profiles of the theoretical filter. By replacing the resistive load with a real loudspeaker, the filter takes on an underdamped response (peak is $\sim 15\text{dB}$ above the baseband level). This has a consequence of severely effecting the group delay. The cause of this peak is most likely attributable to the voice coil inductance of the loudspeaker. At the cross-over frequency of 20kHz , the inductance will increase the impedance of the load and this leads to an underdamped system.

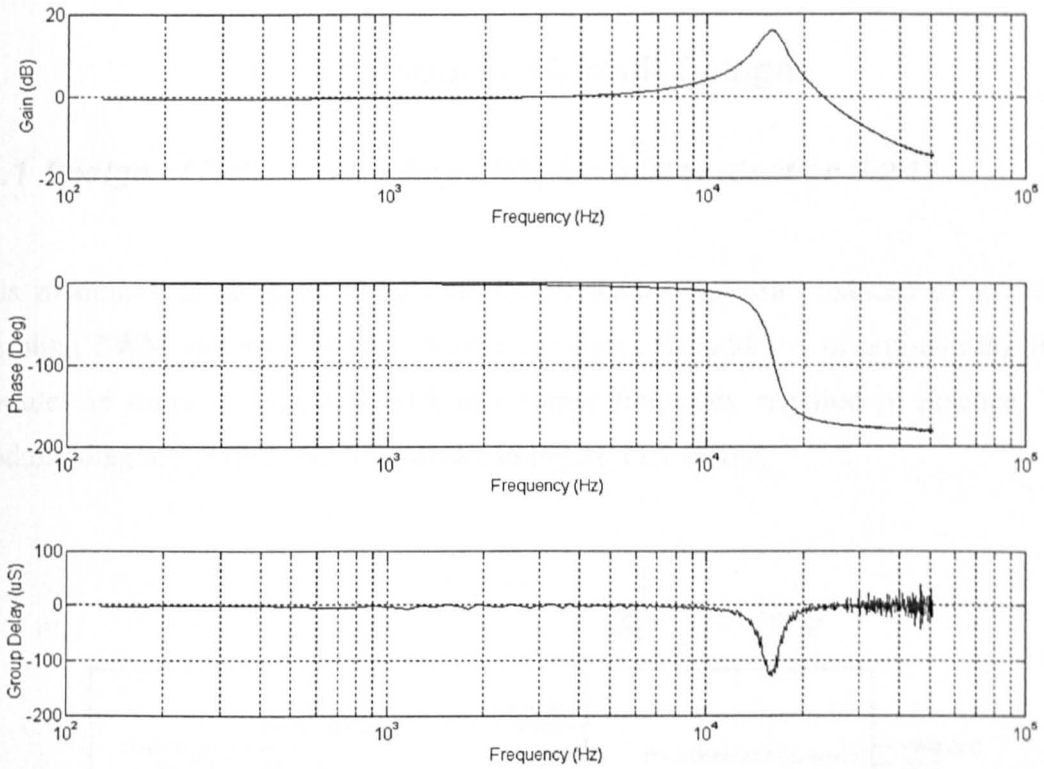


Figure 10.11 - Transfer characteristic with loudspeaker load

In reality, a number of drive units will be used with associated cross-over circuitry. As such, although the impedance of the woofer will rise considerably at high frequency, the midrange and tweeter drive units will have lower impedance, which will load the filter at the cross-over frequency. This should result in a filter characteristic, which more closely resembles the ideal Gaussian prototype.

11 Appendix C – Circuit Designs

11.1 Design of Natural Sampling PWM Modulator (Section 3.2.1)

This modulator is designed to validate the theoretical spectra produced by a natural sampling PWM system. The modulator also allows the addition of anti-aliasing filter modules in order to find the order and corner frequency required in practice. The modular diagram of this system is shown in Figure 11.1 below.

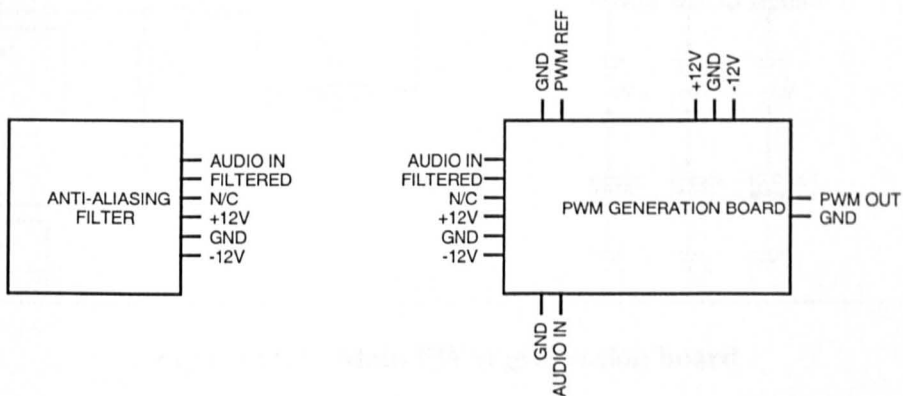


Figure 11.1 - System diagram of PWM modulator

The anti-aliasing filter (on the left in Figure 11.1) is implemented on a plug-in PCB, which allows for easy filter swapping. The main PWM circuit (on the right in Figure 11.1) routes the audio input signal (AUDIO IN) through to the anti-aliasing filter which then passes the filtered signal (FILTERED) back to the PWM board for comparison to the PWM reference signal (PWM REF). The resulting PWM signal is then fed out (PWM OUT). The circuitry for the main PWM generation board is shown in Figure 11.2 below. The circuit diagrams for the 2nd, 3rd and 4th order anti-aliasing filters are shown in Figure 11.3, Figure 11.4 and Figure 11.5 respectively. All filters were designed to a 20kHz corner frequency using Butterworth polynomials. The input reference signal is buffered with an inverting amplifier to ensure a clean reference source at the PWM comparator.

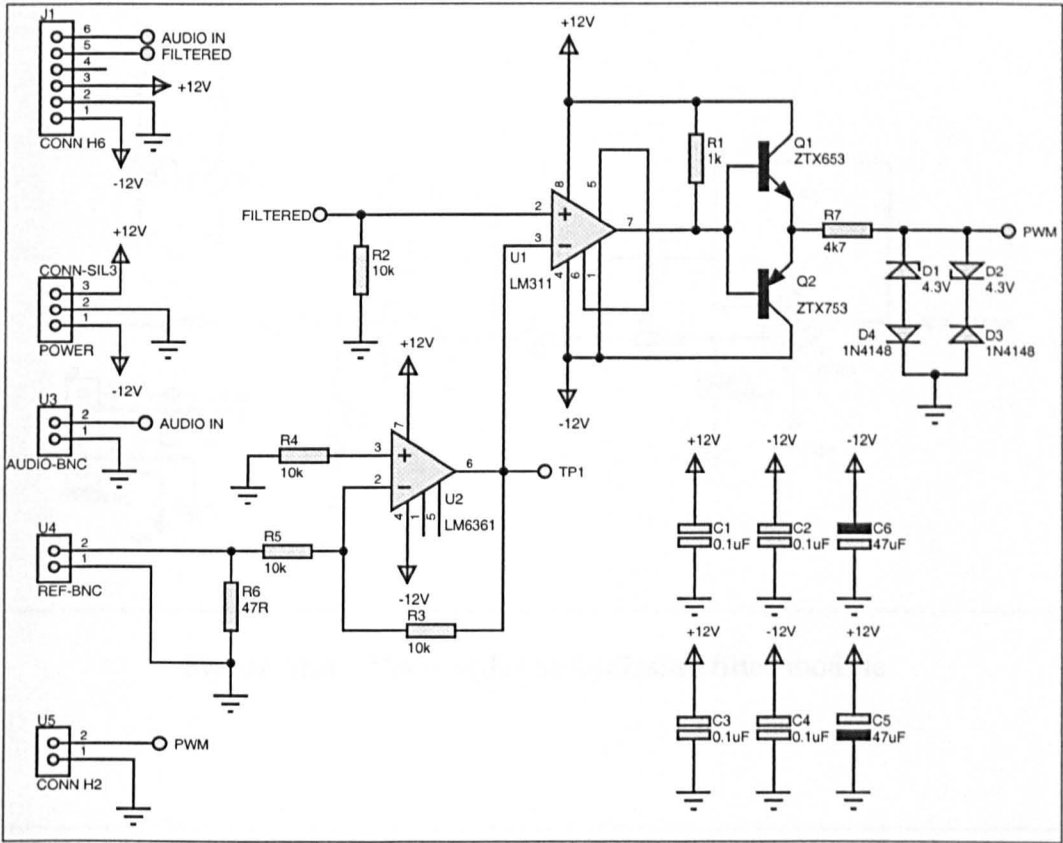


Figure 11.2 - Main PWM generation board

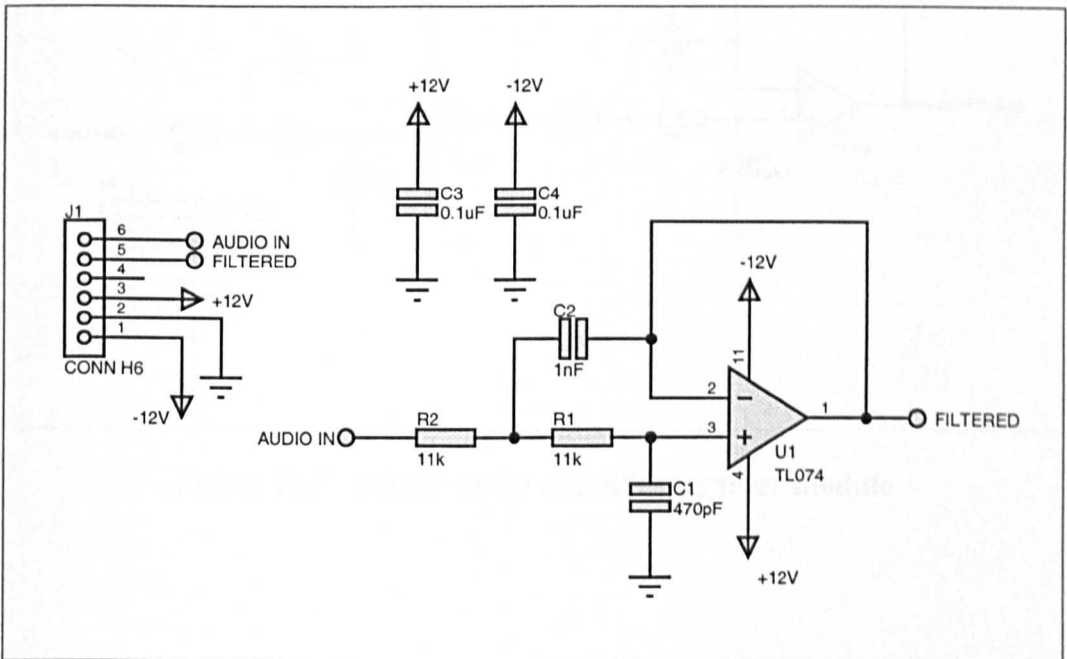


Figure 11.3 - Second order anti-aliasing filter module

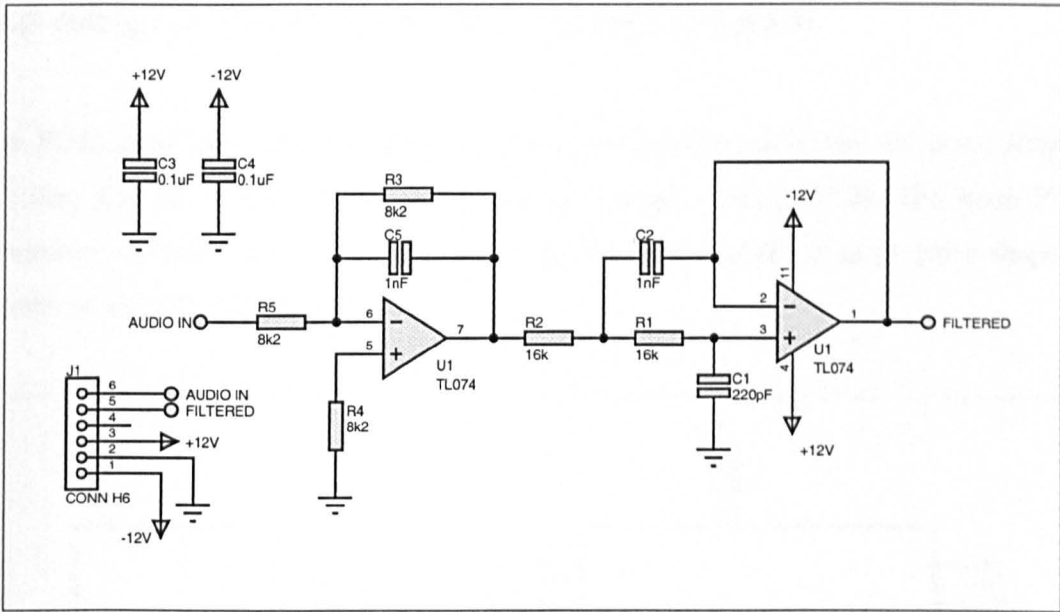


Figure 11.4 - Third order anti-aliasing filter module

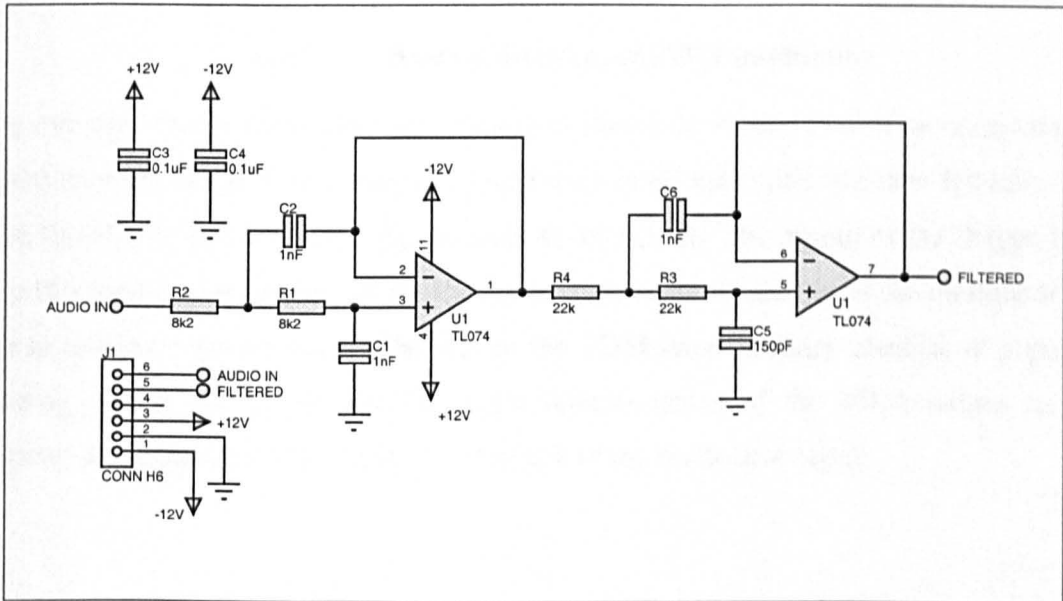


Figure 11.5 - Fourth order anti-aliasing filter module

11.2 Design of PDM Modulator System (Section 3.3.3.1)

The PDM modulator was designed in a modular fashion such that the noise-shaping circuitry can be changed by simply changing a single plug-in PCB. The main PDM generation circuit is shown on the right of Figure 11.6 and the plug-in noise shaper is shown on the left of Figure 11.6.

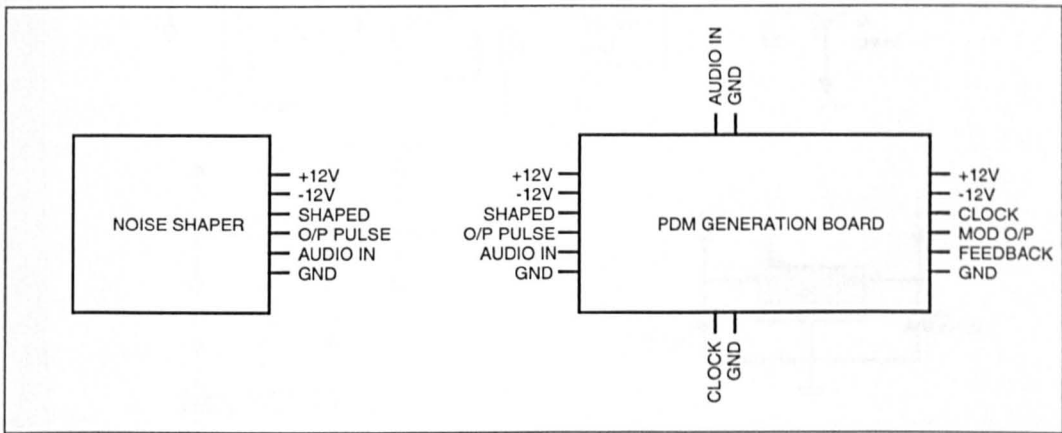


Figure 11.6 - System diagram of PDM modulator

The circuitry of the PDM generation board is shown in Figure 11.7. The noise-shaped signal from the noise-shaper board is quantised around zero volts and then fed into a D-type flip-flop which is clocked by the main system clock. The output of the D-type flip-flop is a logic representation of the modulator output and is fed out of the modulator for use in driving a power stage. The rest of the PDM base circuitry consists of a pulse-shaping circuit which converts the logic representation of the PDM output into a positive and negative pulse stream to feedback to the modulator input.

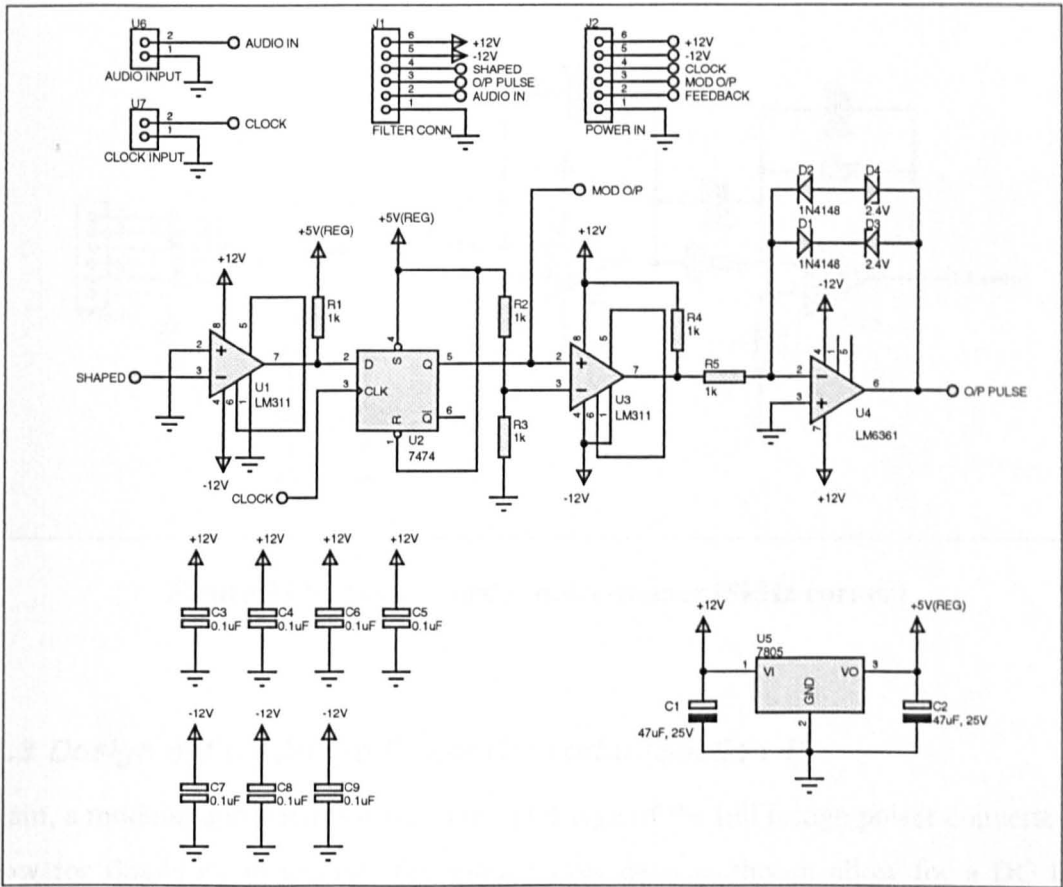


Figure 11.7 - PDM base circuitry

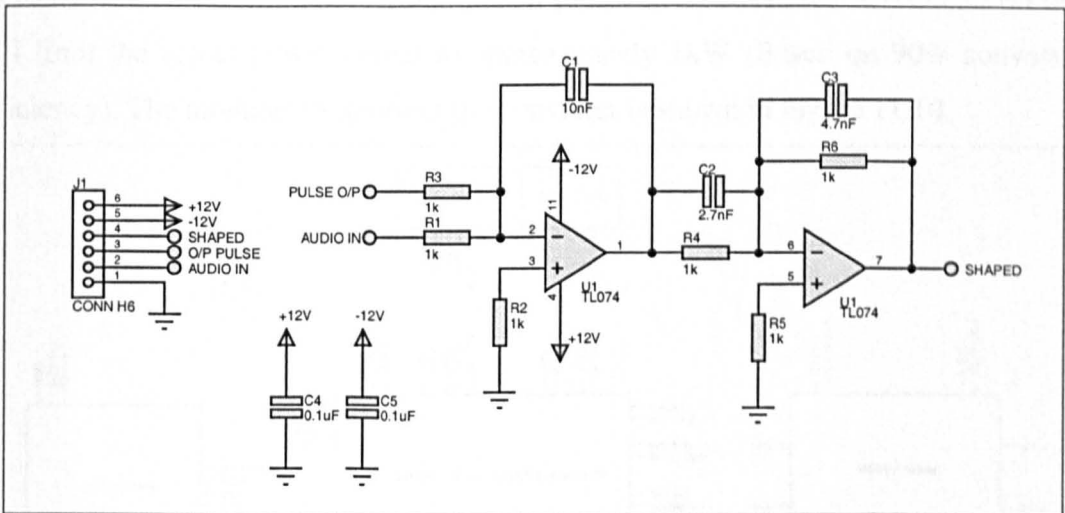


Figure 11.8 - Second order noise-shaper (20kHz corner)

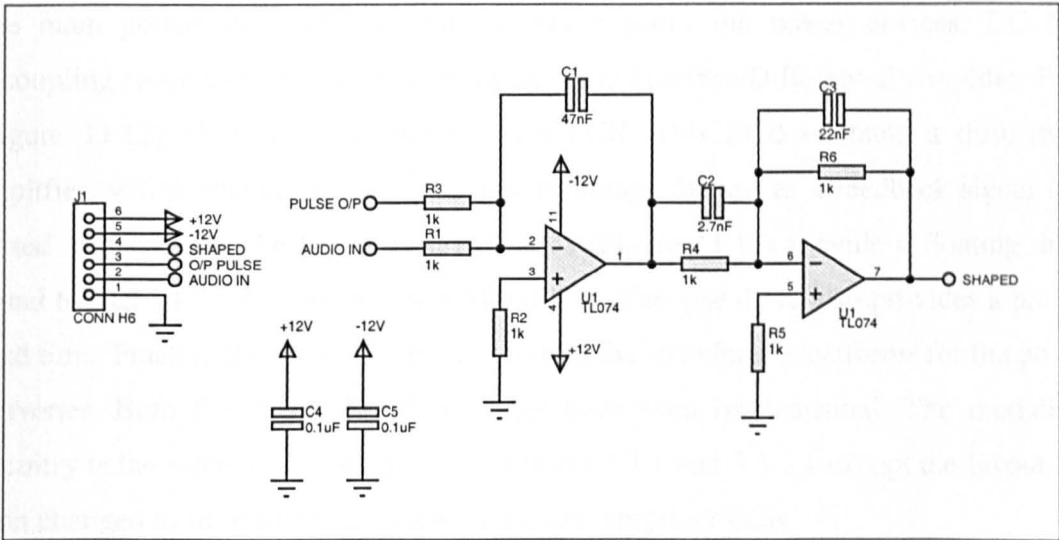


Figure 11.9 - Second order noise-shaper (5kHz corner)

11.3 Design of Full-Bridge Power Converter (Section 4)

Again, a modular approach was taken in the design of the full bridge power converter to allow for flexibility in testing. The main power devices chosen allow for a DC link voltage of up to 200V and a peak load current of 30A. This allows for a peak power of up to 6kW although the thermal dissipation potential of the heatsink (0.75°C/W) used will limit the actual power output to approximately 1kW (Based on 90% conversion efficiency). The modular structure of the converter is shown in Figure 11.10.

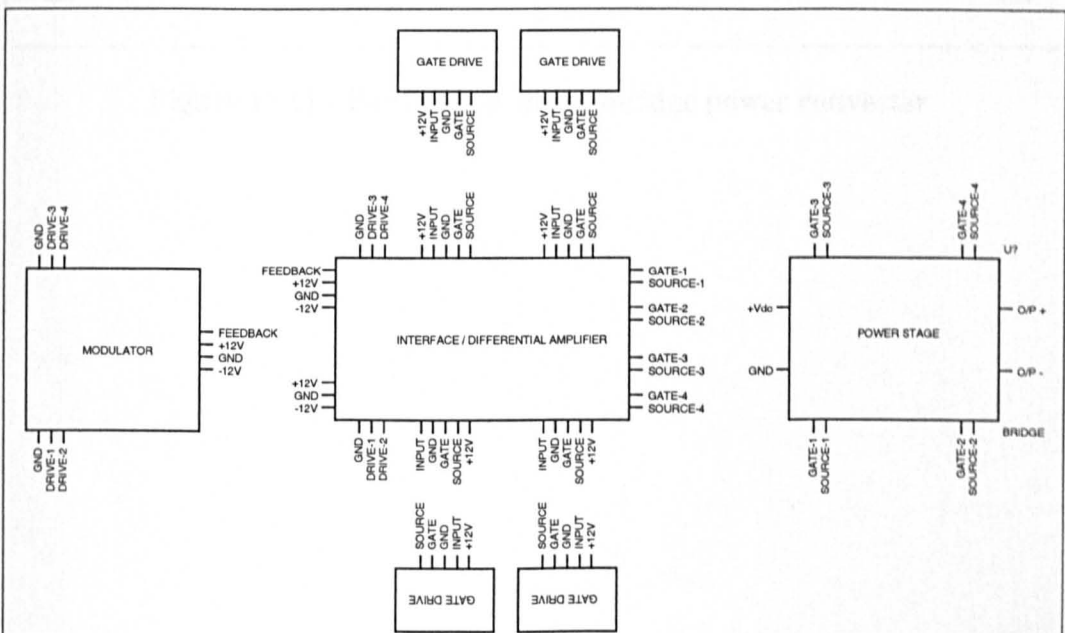


Figure 11.10 - Modular structure of full-bridge power converter

The main power stage PCB (Figure 11.11) contains the power devices, DC link decoupling capacitors and power connections. The Interface/Differential Amplifier PCB (Figure 11.12) plugs into the power stage PCB. This PCB contains a differential amplifier, which attenuates the actual output voltage for use as a feedback signal in a closed loop design. The four gate drive PCBs (Figure 11.13) provide a floating drive signal to each of the four main power MOSFETs. The gate drive also provides a pre-set dead time. Finally, the modulator PCB provides the switching waveforms for the power converter. Both PWM and PDM strategies have been implemented. The modulator circuitry is the same as that specified in sections 3.2.1 and 3.3.3.1 except the layout has been changed to fit onto the interface/differential amplifier PCB.

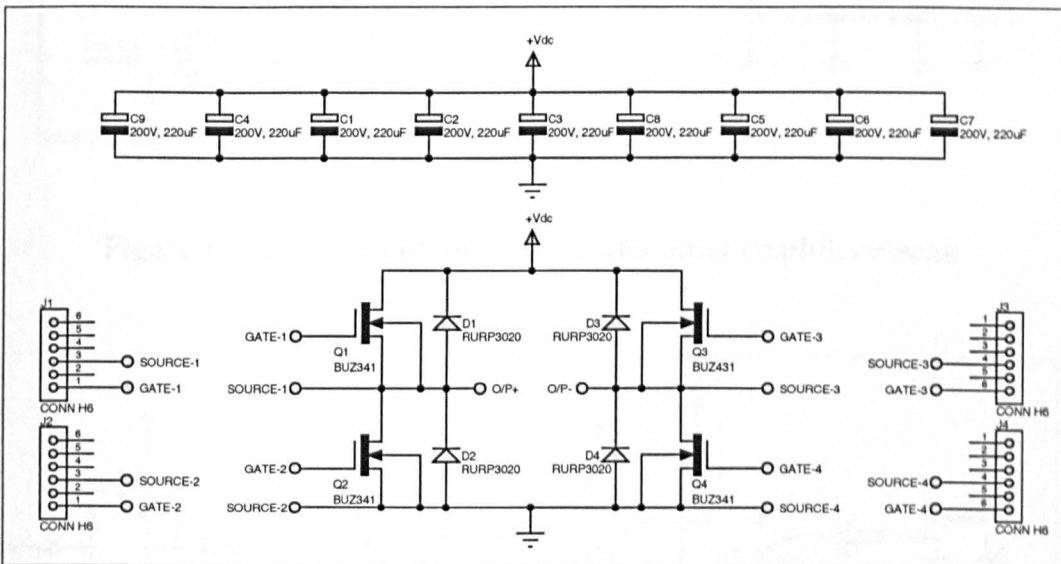


Figure 11.11 - Power stage of full-bridge power converter

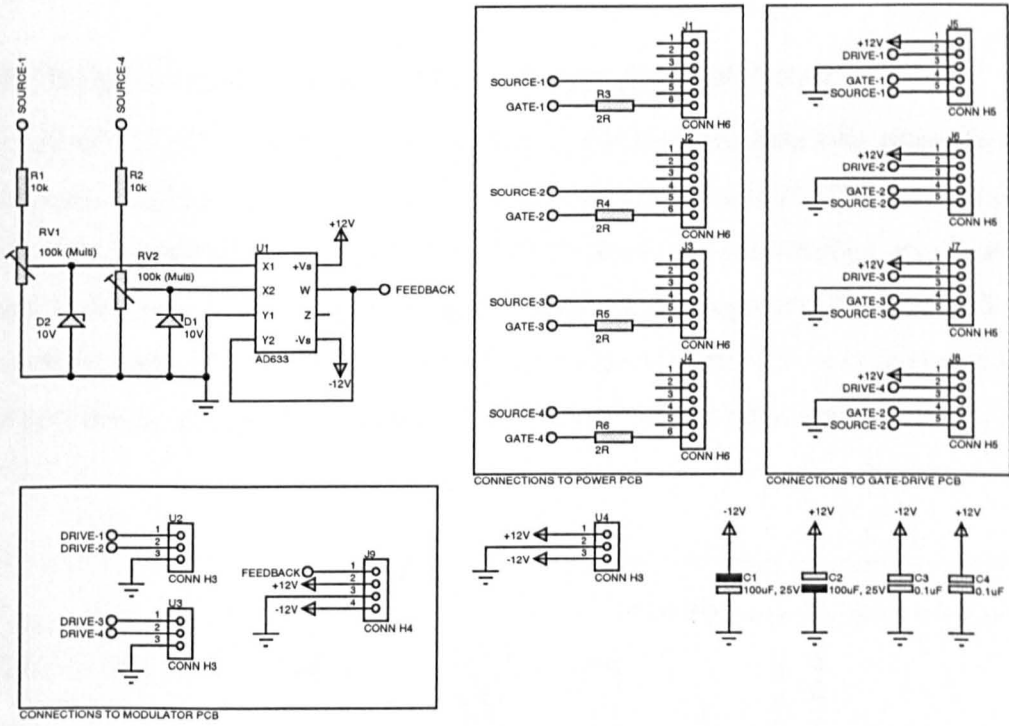


Figure 11.12 - Design of interface / differential amplifier circuit

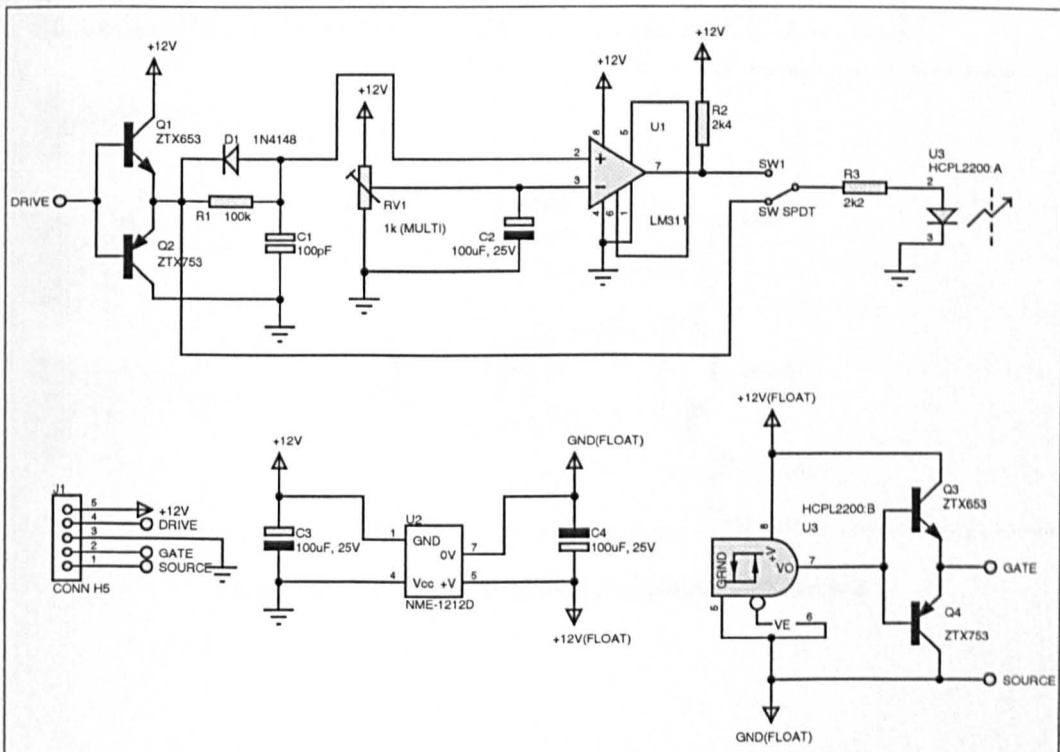


Figure 11.13 - Design of floating gate drive / dead time generator

11.4 Design of Full Primary Side Prototype (Section 5.2.4)

The full primary side power stage consists of the primary switching element, power transformer, energy recovery snubber and snubber control circuit. The snubber control circuit was implemented on a plug-in PCB to allow for optimisation at a later date. Figure 11.14 shows the full primary power stage PCB design and Figure 11.15 shows the snubber control circuit. (The layout of the design in Figure 11.14 is shown in section 4.2.4 and details the optimised layout for minimum leakage inductance).

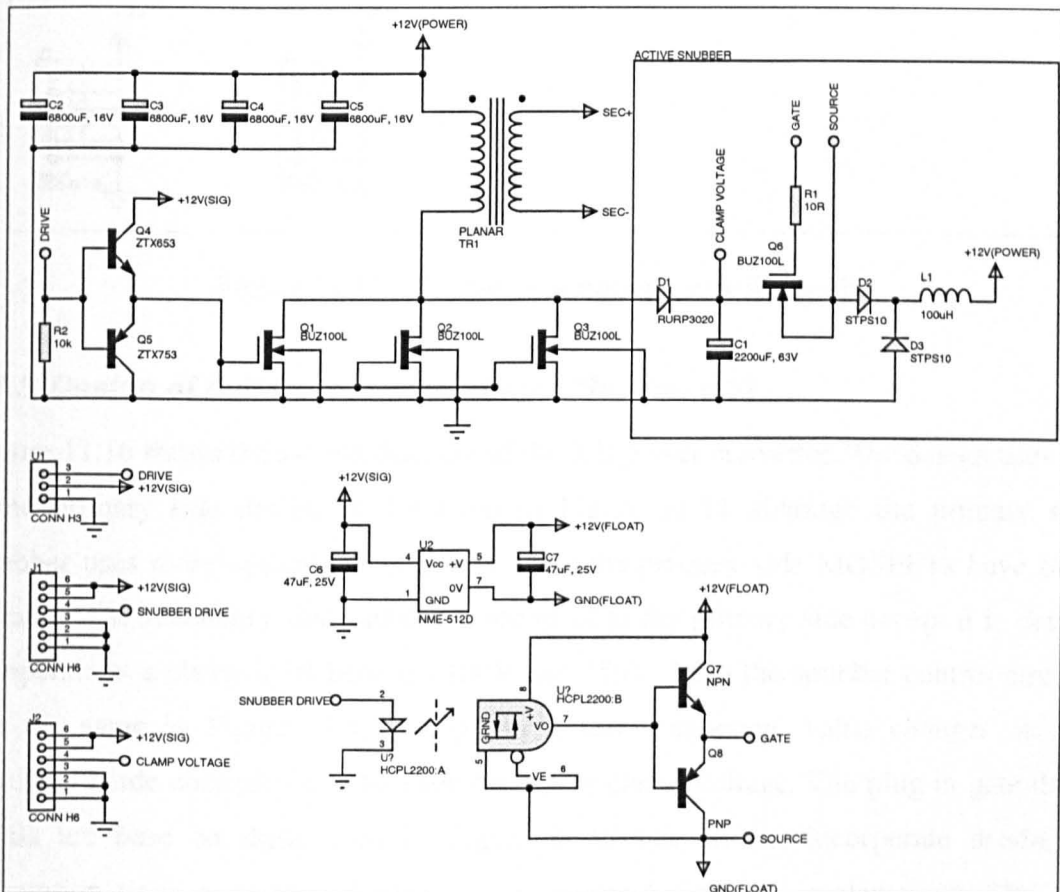


Figure 11.14 - Design of full primary side circuit

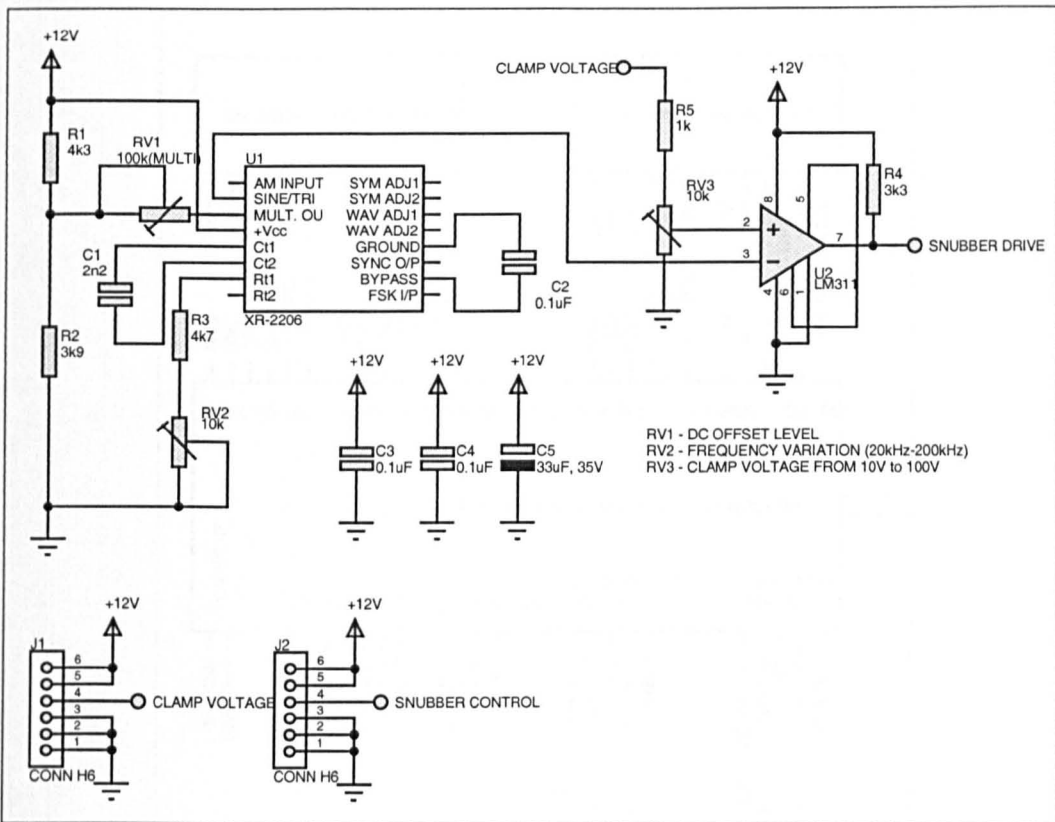


Figure 11.15 - Design of snubber control circuit

11.5 Design of Full Novel Power Stage (Section 5.3)

Figure 11.16 shows the system diagram of the full power converter. The design uses the same primary side design as described in Figure 11.14 although the primary side snubber uses more optimised components and the primary side MOSFETs have been updated. The secondary side snubber is identical to the primary side except it is design to operate at a clamp level between 100V and 150V. Both the snubber control circuits are the same as Figure 11.15 except for a few component value changes on the secondary side controller to allow for the higher clamp voltage. The plug in gate drive PCBs are base on those used in Figure 11.13 but do not incorporate dead-time generation since a variety of switching strategies have been implemented. The full power stage circuit diagram is shown in Figure 11.17.

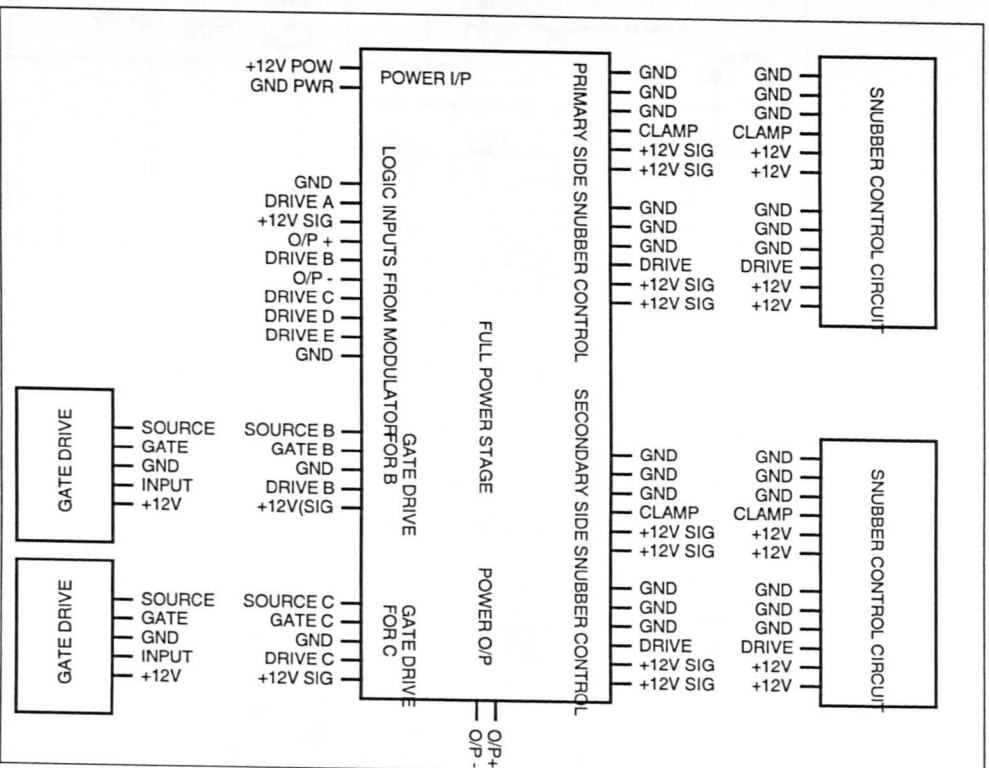


Figure 11.16 - System diagram of full novel power converter

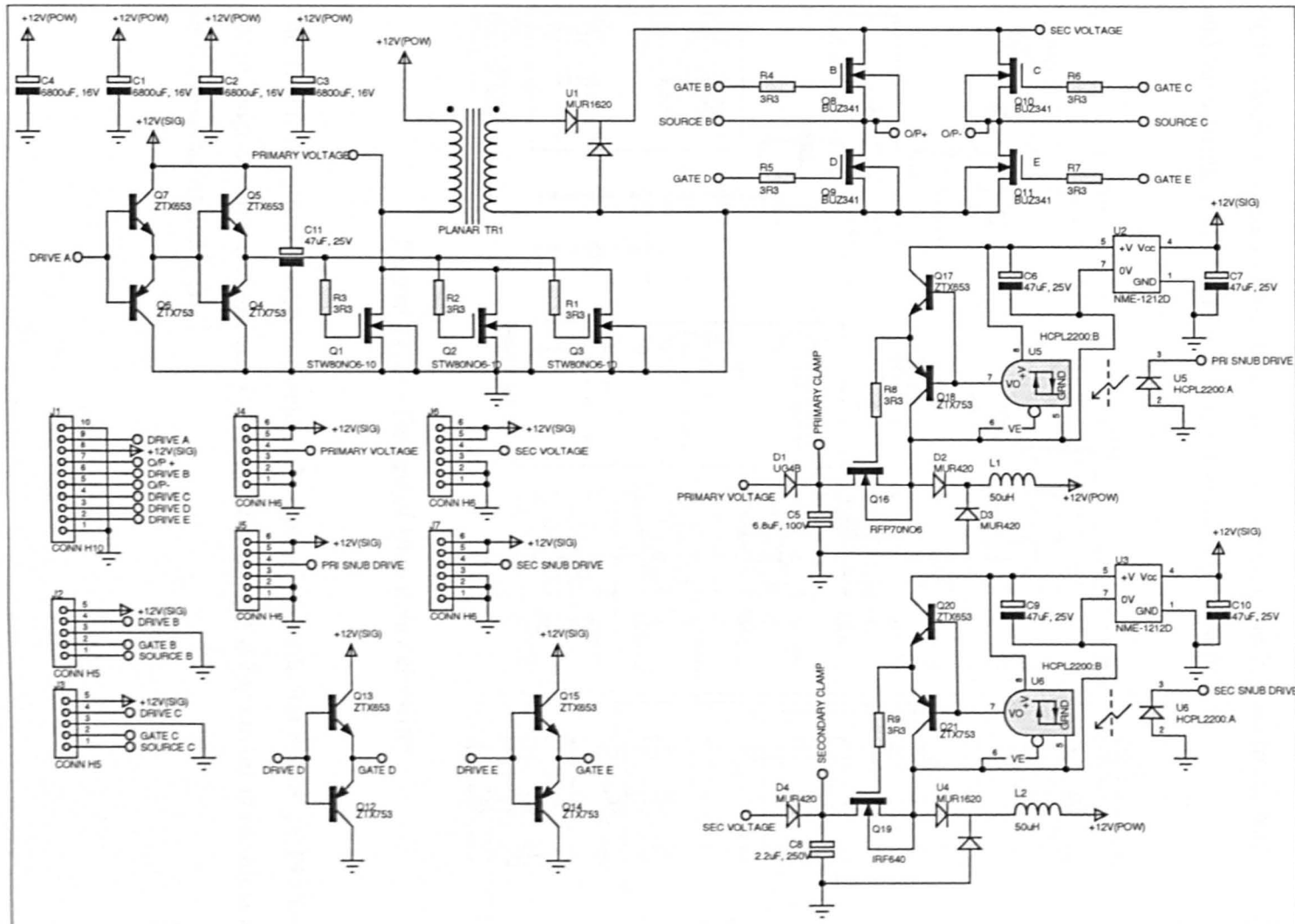


Figure 11.17 - Design of full novel power stage

11.6 Design of Time-Delay Modulator Interface Circuit (Section 6.3)

This system is again designed in a modular fashion. Separate analogue and digital power supplies were used to obtain optimal performance. Figure 11.18 shows the main PCB which incorporates the differential audio input, the PAL chip for logic generation and the separate regulators for the analogue and digital supplies.

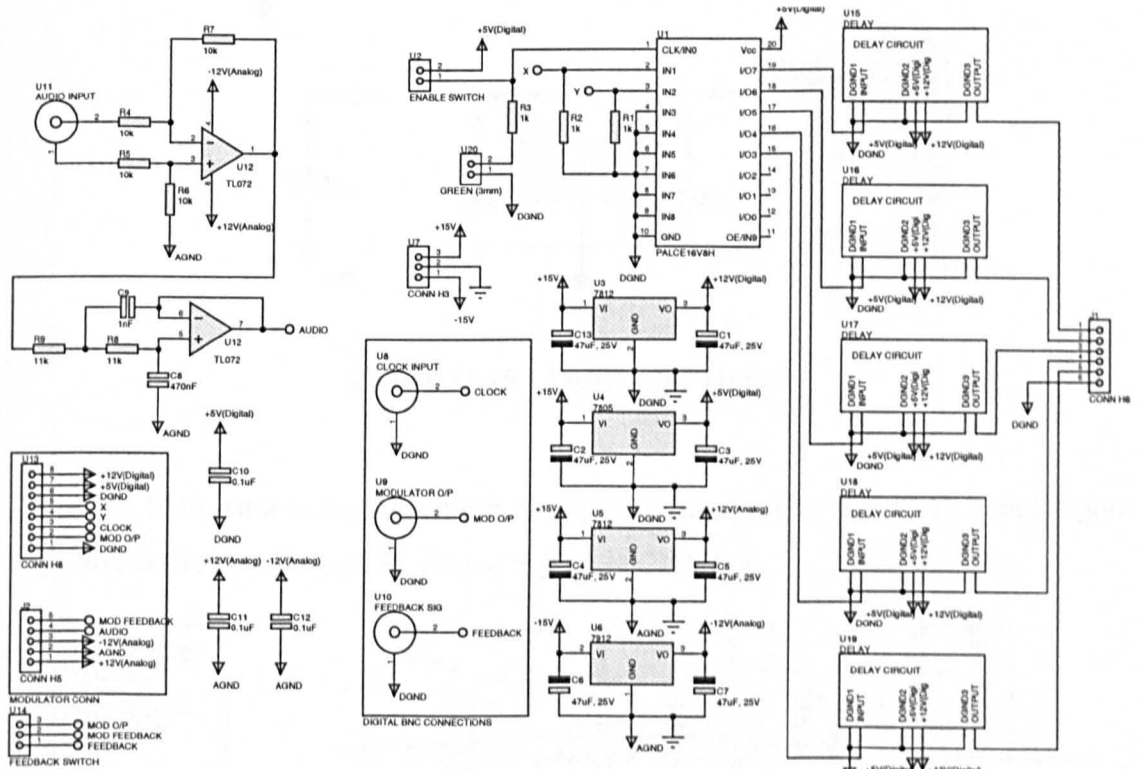


Figure 11.18 - Design of time delay circuitry

The time delay circuits were implemented on plug in boards and Figure 11.19 shows the circuit diagram for a turn-on delay circuit. The turn-off delay circuit is identical except for the reversal of diode D1.

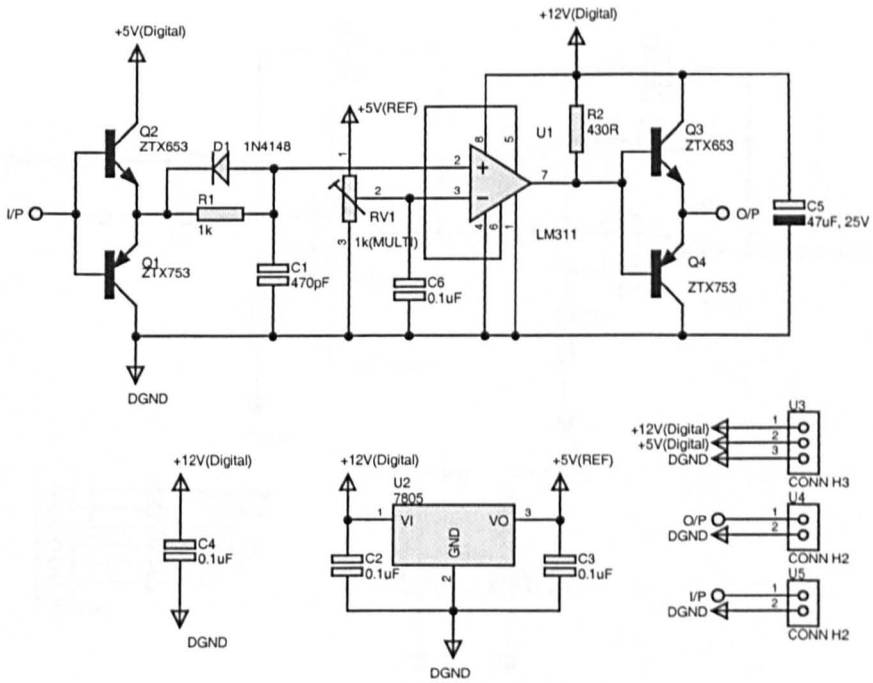


Figure 11.19 - Time delay circuit

The PDM Modulator was a second order type (as specified in Figure 11.7 and Figure 11.8) and is shown in Figure 11.20 and Figure 11.21 below.

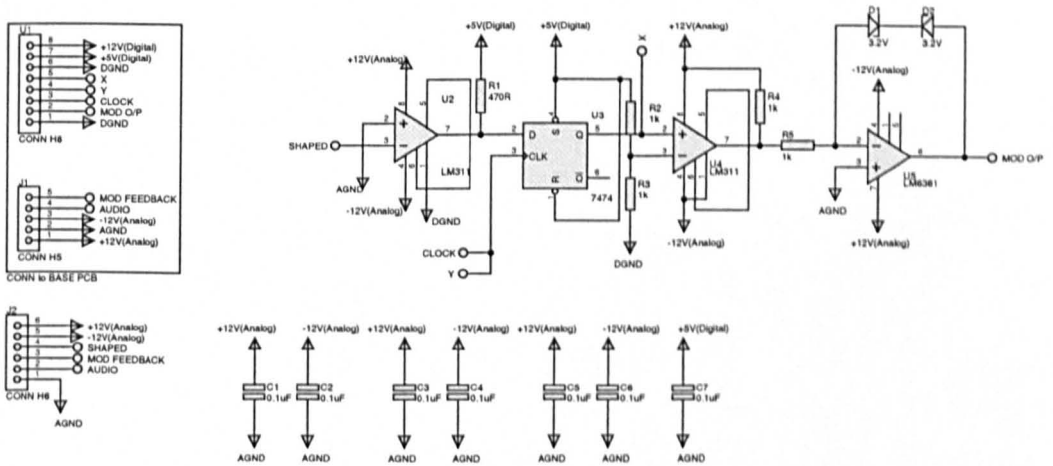


Figure 11.20 - PDM base circuitry

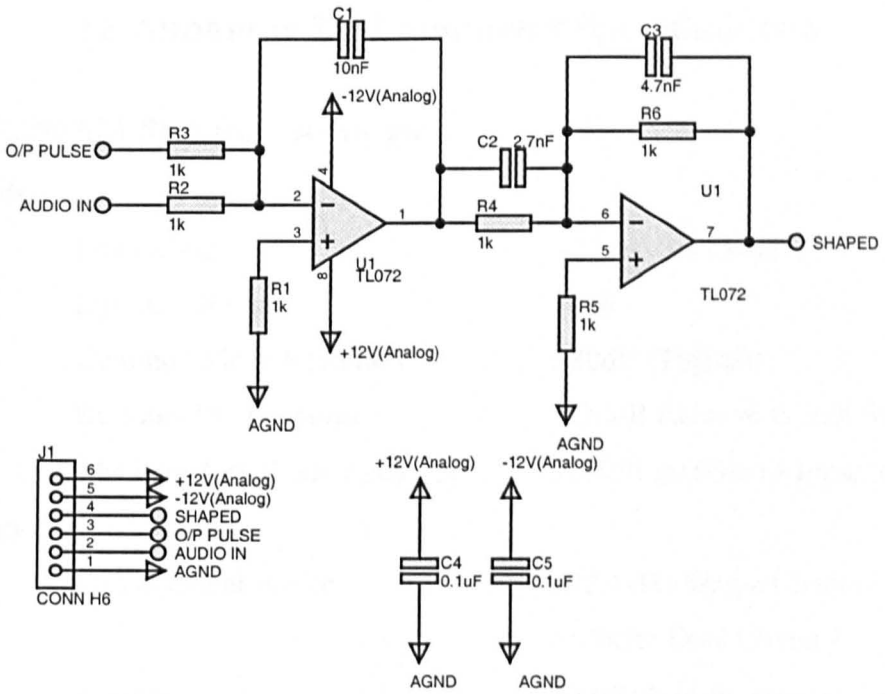


Figure 11.21 - 2nd order noise shaper

12 Appendix D - Equipment Specifications

12.1 HP 35660A Spectrum Analyser

Amplitude

Input Range	+27dBV to -51dBV
Dynamic Range	70dB
Common Mode Rejection	>80dB (Typical)
Residual DC Response	<-30dB Relative to Full Scale
Absolute Amplitude Accuracy	$\pm 0.5\text{dB} \pm 0.03\%$ of Input Range

Frequency

Measurement Range	102.4kHz Single Channel 51.2kHz Dual Channel
Accuracy	$\pm 0.003\%$ of frequency reading
Windowing	Uniform Flat Top Hanning

12.2 NORMA D6000 High Bandwidth Power Analyser

Voltage Measurements

Bandwidth	DC-2MHz
Measurement Error	Typically $\pm 1\%$

Current Measurements

Bandwidth	DC-1.2MHz
Measurement Error	Typically $\pm 1\%$

12.3 PEM Rogowski Coil

Bandwidth	5MHz
Sensitivity	20mV/A