The University of Sheffield

A New Switching Technique for Minimisation of DC-link Capacitance in Switched Reluctance Machine Drives

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Summary

In a switched reluctance (SR) drive, the transfer of the de-fluxing energy in stator windings back to the dc-link results in a large dc-link capacitance. This limits its applications where weight and size of the drive are restricted. This thesis describes a control technique for the dc-link capacitance minimisation in an SR drive. The proposed control technique maintains the constant power transfer between the dc supply and the H-bridge converter. The average dc-link current over a switching period is kept constant.

When the output of the integrator, i.e., the average dc-link current, reaches a predefined value proportional to the torque demand, appropriate switching takes place. This is achieved by integrating the dc-link current in each switching period. This technique is called dc-link current integration control (DLCIC). The de-fluxing current from the outgoing phase is not fed back to the dc-link capacitor. Instead, it is transferred to the incoming phase to prevent a negative dc-link current, which causes a fluctuation in the capacitor voltage.

Extensive simulation studies of the DLCIC and other techniques reported in literature have been performed and the simulation results from DLCIC are compared with those from other techniques such as Hysteresis Current Control (HCC) and Pulse Width Modulation Current Control (PWMCC). It has been shown that the peak-to-peak voltages across the dc-link capacitor from DLCIC are the lowest amongst other techniques.

The operational speed range of the DLCIC is determined and the optimal turn-on and turn-off angles are proposed. Filter components under the DLCIC operation has been designed and compared with the filter for HCC. It is shown that the weight of the filter for DLCIC is far lower than that for HCC. The proposed control technique have been validated by experiments. The experimental results show that at the dc-link voltage

ripple which results from DLCIC is much lower than that from HCC. This demonstrates that DLCIC can minimise the dc-link capacitance in an SR machine drive.

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Symbols & Nomenclature

a	Duty cycle in [2.9]
A_{cu}	Cross section area of copper wire
a_n	Duty cycle of outgoing phase
a_{n+1}	Duty cycle of incoming phase
B_{max}	Maximum permissible flux density
C	Dc-link capacitor
C_d	Dumping capacitor
C_w	Width of inductor core
D	Optimal duty cycle for PWMVC
d	Diameter of cable
DC_{avg}	Average dc-link current
DC_{dmd}	Dc current demand
DC_dmd	Dc current demand
d_{cu}	Weight density of copper wire
delta_T	Switching period
D_g	Optimal duty cycle for PWMV in [3.6]
DLCIC	Dc-link Current Integration Control
DPh1	Phase1 dwell signal
DPh2	Phase2 dwell signal
DPh3	Phase3 dwell signal
dSPACE	Digital Signal Processing And Control Engineering
dwell	Dwell period signal
f_{com}	Commutation frequency
FFT	Fast Fourier Transform
H_{ac}	AC harmonic
h_b	Thickness of bobbin
HCC	Hysteresis Current Control
H_{dc}	DC harmonic

i	current
IC	Initial Condition
i_c	Dc-link capacitor current
$I_{c,rms}$	Maximum rms current of dc-link capacitor
I_{dc}	Dc-link current
$I_{dc,max}$	Maximum average dc-link current in MIL-STD-416E
IGBT	Insulated Gate Bi-polar Transistor
I_{in}, i_{in}	Input current, supply current
$I_{in,p2p}$	Input current ripple
i_n	Outgoing phase current
i_{n+1}	Incoming phase current
i_0	Average current drawn by converter, average dc-link current
I_p	Peak current of inductor
I_{ph}	Phase current
I_{ph1}	Phase1 current
I_{ph2}	Phase2 current
I_{ph3}	Phase3 current
$I_{ph,rms}$	Rms phase current
K_2	Aspect ratio of coil window
L	Input inductance
l	Length of cable
L_a	Inductance at aligned position
l_{av}	Average length of coil
L_d	Recovery winding
$Loss$	Copper loss in winding
$lower\_sw$	Lower switch
L_{ph}	Phase inductance
L_u	Inductance at un-aligned position
$L(\theta,i)$	Phase inductance at position θ with current i
MIL	Military standard

MIL-STD-416E	Requirement for the control of electromagnetic interference characteristic of subsystems and equipment [4.16]
MIL-STD-704F	Aircraft electric power characteristic standard [4.15]
mmf	Magnetomotive force
MUX	Multiplexer
N	Number of turns of inductor
N_{ph}	Number of phase in SR machine
N_r	Number of rotor poles
P	Machine power
PCI	Peripheral Component Interconnect
Ph1	Phase1
Ph2	Phase2
Ph3	Phase3
PI	Proportional - integral
PWM	Pulse Width Modulation
PWMCC	Pulse Width Modulation Current Control
PWMVC	Pulse Width Modulation Voltage Control
R	Phase winding resistance
R_a	Inverse inductance at aligned position
R_L	Input resistance
RMS, rms	Root Mean Square
rpm	Revolutions per minute
R_s	Equivalent series resistance of dc-link capacitor
R_{th}	Thermal resistance of dc-link capacitor
R_{ua}	Inverse inductance at un-aligned position minus inverse inductance at aligned position
$S_{1,n}$	Upper switching signal of phase n converter
$S_{2,n}$	Lower switching signal of phase n converter
R_{ph}	Phase winding resistance
SR	Switched Reluctance
T	Machine torque

t	time
T_a	Ambient temperature
T_{avg}	Average torque
T_c	Dc-link capacitor temperature
THD	Total Harmonic Distortion
T_{ph}	Phase torque
T_{ph1}	Phase1 torque
T_{ph2}	Phase2 torque
T_{ph3}	Phase3 torque
T_{p2p}	Torque ripple, peak-to-peak torque
T_s	Switching period
$TURNS$	Number of turns of phase winding
$T(\theta,i)$	Instantaneous torque at position θ with current i
T/I	Torque per ampere
T/I^2R	Torque per copper loss
UHC	Unipolar Hysteresis Control
$upper\_sw$	Upper switching signal
$U(s)$	Input of system
v	Load voltage
V_c	Dc-link capacitor voltage
$V_{c,p2p}$	Dc-link capacitor voltage ripple
V_{dc}	Dc supply voltage
VHC	Voltage Hysteresis Control
V_{lower}	Lower limit of dc-link capacitor voltage
V_t	Terminal voltage of phase winding
V_{t1}	Terminal voltage of phase1
V_{t2}	Terminal voltage of phase2
V_{t3}	Terminal voltage of phase3
V_{upper}	Upper limit of dc-link capacitor voltage
V_0	Average dc-link capacitor voltage
W'	Co-energy

W_e	Electrical input energy
W_f	Stored field energy
W_m	Mechanical output energy
W_{mag}	Magnetic energy
W_n	De-fluxing energy of outgoing phase
W_{n+1}	Fluxing energy of incoming phase
W_w	Width of inductor window
x	Ratio of flux at aligned position to flux at optimal turn-off angle
$X(s)$	Response of system
Z_p	Impedance of constant power load
ΔV_{max}	Voltage gap between supply voltage and upper limit voltage
ΔV_{min}	Voltage gap between supply voltage and lower limit voltage
ε	Stroke angle
ζ	Damping ratio of system
θ_a	Aligned position
θ_{adv}	Angular distance between θ_{on} and θ_m in [3.1]
θ_{a2}	Middle point between θ_m and θ_a
θ_m	Corner point of phase inductance
θ_{off}	Turn-off angle
θ_{on}	Turn-on angle
θ_u	Un-aligned position
μ	Permeability of conductor
ΣT_{ph}	Summation of phase torque
$\psi(\theta_{off})$	Flux linkage at turn-off angle
$\psi(\theta_{on})$	Flux linkage at turn-on angle
$\psi_a(I_{dmd})$	Flux linkage of demand current at aligned position
$\psi_{a2}(I_{dmd})$	Flux linkage of demand current at θ_{a2}
$\psi_m(I_{dmd})$	Flux linkage of demand current at θ_m
$\psi_u(I_{dmd})$	Flux linkage of demand current at un-aligned position

ω	Rotational speed
ω_n	Natural frequency

Chapter 1

Introduction

1.1 Introduction

The interest in switched reluctance (SR) machines has increased during the last forty years. With the advanced technologies in the power electronics devices and controls, the SR machines are prevalently utilised as an alternative to conventional electrical machines such as induction or brushless DC/AC machines. [1.1-1.5]. The SR machines possess many advantages [1.3-1.16]. For example, their configuration and winding structure are simple. These make the construction process and the machines themselves economically comparing to classical machines with the same power. Moreover, due to no rotor magnet and no commutator, SR machines lead to low maintenance and high reliability. Since the current of SR machines is unipolar, the converter used to feed the currents is simple and independently controlled by each phase of the converter. All of these are the fault tolerance features which are attractive to safety critical applications such as aircraft and electric vehicles [1.15-1.24]. Even in a fault condition, the drive system can be reconfigured to operate continuously.

Due to the highly nonlinear relationship between machine torque and phase currents, torque ripple and acoustic noise are the main disadvantages of SR machines. These problems have been well documented in most SR machine literatures. Other issues associated with SR machines are also widely researched such as the improvement of power electronics drives [1.25-1.28] and the dynamic response of the phase current control [1.29-1.32]. However, there is a further problem with SR machine drives, that is, the use of the dc-link capacitor making them less reliable, bulky and heavy [1.24].

The dc-link capacitor is installed to buffer the energy between a converter and a dc supply. It also reduces the ac harmonic drawn from into the dc supply source [1.76]. Those functions lead to the excessive size and weight of the dc-link capacitor bank. If the dc-link capacitance can be minimised the SR machine drives will be compact, light-weight, and more reliable. Many researches have been attempting to reduce the dc-link capacitance. Minimising capacitance is particularly important in applications such as aerospace system where electrolytic capacitor cannot be used because of reliability requirements. In these applications, it is necessary to use film capacitor which are much less energy density, as describe in Section 1.3.

In a SR machine drive with AC supplies the capacitor of the front-end converter is claimed to be reduced in [1.33-1.35] by controlling the front-end converter. In [1.36-1.39], the dc-link capacitance is reduced by a power factor correction. However, the power conversion or PFC circuits are added into the system. This increases the system cost and compromises the system efficiency.

In this research, a dc voltage supply as the energy source for SR machine drives is considered, and an asymmetric H-bridge converter is employed to keep the benefits of the fault tolerance of the SR converter circuit. The control technique to reduce the dc-link capacitance via the H-bridge converter is addressed in this thesis. This chapter describes the basic principles of the switched reluctance machine, the torque production,

the converter, the basic operation, and the dc-link capacitor voltage. Then, the organisation of the thesis are illustrated.

1.2 Basic Structure of SR Machine

Switched reluctance machines have salient poles on both stator and rotor. Figure 1.1 shows the structure of a switched reluctance machine with 12 stator poles and 8 rotor poles.

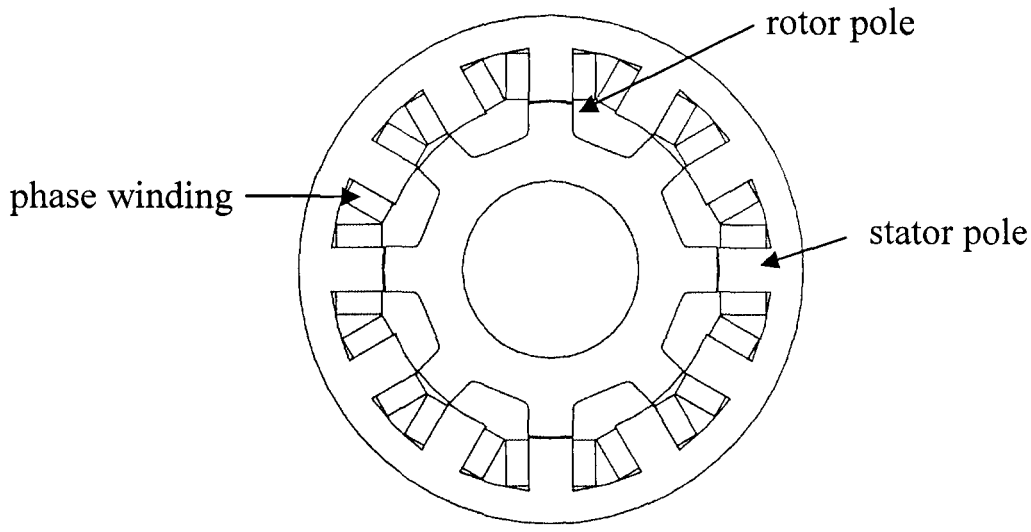


Figure 1.1: Switched reluctance machine structure

The windings are placed on the stator. The rotor consists simply of the ferromagnetic poles and back-iron. At stator poles, the current is fed through the phase winding. The electromagnetic field is produced to draw the rotor poles which are moved to align with the stator poles. The electrical energy from the phase windings is released and converted into mechanical energy. After that, the next phase winding, which is called incoming phase, is fed by the electrical energy and the rotor poles moves to the next stator poles. The rotor is moved by the sequence of the energised phase windings. This procedure is similar to the procedure of the stepper motor. However, the control loop of the stepper motor is an open loop and no position feedback while the SR machine is a close loop control with the rotor position sensor. In Section 1.2, the basic theories about

the SR machine, such as the electromagnetic equations, the torque production, the conduction state, the control methods and the converter circuit, are described.

1.2.1 Electromagnetic Equations

From Faraday's law, the voltage of the phase winding of the SR motor is represented as

$$V_t = R_{ph} i_{ph} + \frac{d\psi}{dt} \tag{1.1}$$

where

V_t is terminal voltage of the phase winding

R_{ph} is the resistance of the phase winding.

i_{ph} is the phase current.

ψ is the flux linkage.

When the phase current is multiplied into both side of (1.1), the equation can be written as (1.2).

$$i_{ph} V_t = i_{ph}^2 R_{ph} + i_{ph} \frac{d\psi}{dt} \tag{1.2}$$

The term on the left hand side is the instantaneous electrical input power. On the right hand side, term of i^2R is copper loss and the last term is the power of the stored field energy and the mechanical energy. This can be write in an energy equation as,

$$dW_e = Loss + dW_f + dW_m \tag{1.3}$$

where

W_e is electrical input energy.

$Loss$ is the copper loss in the winding.

W_f is the stored field energy.

W_m is the mechanical output energy.

Figure 1.2 illustrates the flux linkage and current relationship of an electromagnetic system. The shaded area is called stored field energy, W_f, which is defined as

$$W_f = \int_0^{\psi_1} i(\psi, \theta) d\psi \tag{1.4}$$

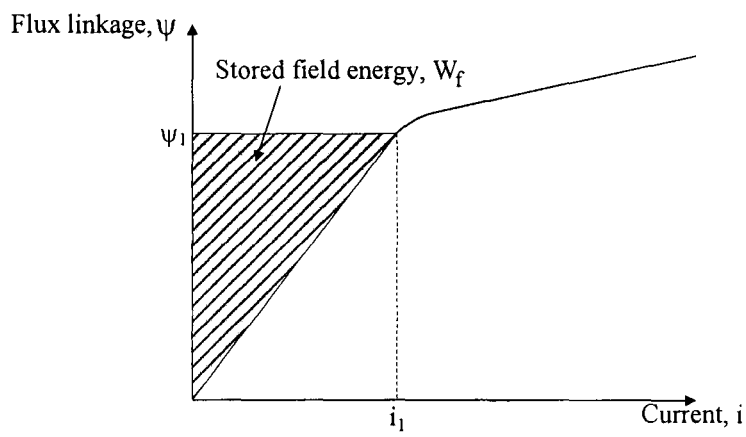


Figure 1.2: Definition of stored field energy

The flux linkage - current curve can be applied with the SR machine operation as in Figure 1.3. An SR motor moves from one position (θ_{on}) to another position (θ_{off}) with a constant current. At the beginning, the electrical energy is fed to the terminal winding of the SR machine. The phase current rises from 0 to i_{ph}. Then, the phase current is controlled to be constant. The rotor moves from θ_{on} to θ_{off}. The flux linkage also moves from the flux level at θ_{on}, $\psi(\theta_{on})$, to the flux level at θ_{off}, $\psi(\theta_{off})$. The input energy from the start until this point is equal to the area in the red trapezoid, area $0\theta_{on}\theta_{off}\psi(\theta_{off})$, which is also equal to the right side term of (1.3) when loss is neglected. After that, the phase current is ejected and the stored field energy at θ_{off} is also discharged. The discharged energy, called de-fluxing energy, is equal to the area in the shade W_f and the mechanical energy is equal to the area in the loop $0\theta_{on}\theta_{off}$.

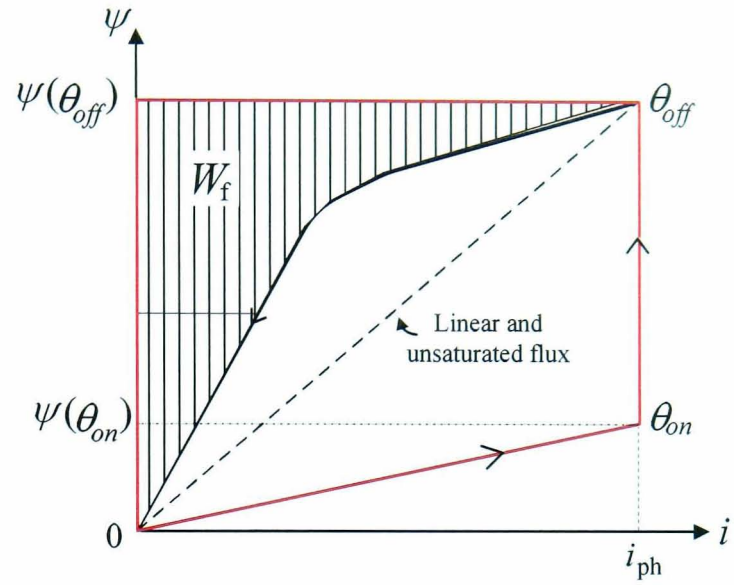


Figure 1.3: Energy conversion loop of SR motor

From Figure 1.3, it can be seen that the characteristic of the flux linkage ψ is nonlinear where the stored field energy and the mechanical energy are not easy to calculated. For the purpose of illustration, the flux linkage may be assumed to be linear and unsaturated flux, as shown in Figure 1.3.

Without loss of generality, the flux linkage is defined as the product of the inductance and the current, the equation of the flux-linkage can be expressed as

$$\psi(\theta,i) = L(\theta,i)\cdot i \tag{1.5}$$

where $L(\theta,i)$ is the phase inductance at the position θ with the current i.

The stored field energy W_f in Figure 1.3 is estimated as

$$W_f = \frac{1}{2}L(\theta,i)\cdot i^2 \tag{1.6}$$

Thus, the rate of change of the stored field energy can be described by

$$\begin{aligned}\frac{dW_f}{dt} &= \frac{d\left[\frac{1}{2}L(\theta,i)\cdot i^2\right]}{dt} \\ &= L(\theta,i)\cdot i\frac{di}{dt} + \frac{1}{2}i^2\frac{dL(\theta,i)}{dt}\end{aligned} \tag{1.7}$$

In order to derive the phase inductance profile in the power equation (1.2), (1.1) is converted as a function of the rotor position and the phase current in (1.8)

$$V_t = R_{ph} i_{ph} + \frac{\partial \psi}{\partial i_{ph}} \frac{di_{ph}}{dt} + \frac{\partial \psi}{\partial \theta} \frac{d\theta}{dt} \tag{1.8}$$

From (1.5), $\frac{\partial \psi}{\partial i}$ is defined as the phase inductance L(θ,i) and term $\frac{\partial \psi}{\partial \theta} \frac{\partial \theta}{\partial t}$ is the back electromotive force (EMF). Then, (1.8) can be adapted to (1.9)

$$V_t = i_{ph} R_{ph} + L(\theta, i) \frac{di_{ph}}{dt} + i_{ph} \frac{dL(\theta, i)}{dt} \tag{1.9}$$

When (1.9) is multiplied by the phase current and the power equation can be presented as (1.10)

$$\begin{aligned} dW_e = i_{ph} V_t &= i_{ph}^2 R_{ph} + L(\theta, i) \cdot i_{ph} \frac{di_{ph}}{dt} + i_{ph}^2 \frac{dL(\theta, i)}{dt} \\ &= i_{ph}^2 R_{ph} + L(\theta, i) \cdot i_{ph} \frac{di_{ph}}{dt} + \frac{1}{2} i_{ph}^2 \frac{dL(\theta, i)}{dt} + \frac{1}{2} i_{ph}^2 \frac{dL(\theta, i)}{dt} \end{aligned} \tag{1.10}$$

From (1.7) and (1.10), it can be seen that the rate of change of the stored field energy is a part of the power equation such that

$$\begin{aligned} dW_e &= i_{ph}^2 R_{ph} + \frac{d\left[\frac{1}{2} L(\theta, i) \cdot i_{ph}^2\right]}{dt} + \frac{1}{2} i_{ph}^2 \frac{dL(\theta, i)}{dt} \\ &= Loss + dW_f + dW_m \end{aligned} \tag{1.11}$$

From the definition of the general torque in (1.12)

$$T = \frac{dW_m}{d\theta} \tag{1.12}$$

Torque per phase of SR machine is described that

$$T_{ph} = \frac{1}{2} i_{ph}^2 \cdot \frac{dL(\theta,i)}{dt} \frac{dt}{d\theta}$$
$$= \frac{1}{2} i_{ph}^2 \frac{dL(\theta,i)}{d\theta} \tag{1.13}$$

where T_{ph} is the torque per phase of the SR machine

1.2.2 Torque Production

Generally, the torque production equation of SR machines does not fit with the d-q axis torque equation as ac motors [1.40]. The torque of SR machines is produced by the propensity of the rotor poles to align with the stator poles to shorten the flux linkage distance. When the electric current flows in the stator phase winding, the stator poles of that phase produce the flux linkage. The nearest rotor poles are drawn to align with those stator poles, and the inductance of the machine phase rises. The relationship between the inductance, the movement of the rotor, and the phase current is schematically presented in Figure 1.4. In this figure, θ_{on} is the position that the phase current starts to rise or the starting point of the dwell period. At θ_{off}, the phase current starts to discharge since it is the end of the dwell period. The relationship between the rate of the change of the phase inductance and the machine torque is explained as followed.

When the edge of the rotor pole aligns with the edge of the stator pole, as shown in Figure 1.5(a), the phase inductance at θ_m starts to rise. When the rotor moves to the position where the stator pole is in the border of the rotor pole, Figure 1.5(b), the increment of the phase inductance is ceased at the maximum inductance, L_a. When the centre of the rotor pole moves to the align position with the centre of the stator pole, in Figure 1.5(c), that position is called the align position, θ_a. Then, if the rotor rotation continues the rotor pole and the stator pole are apart. The edge of the stator pole and the edge of the rotor are aligned again, in Figure 1.5(d). The phase inductance starts to decrease. When the inductance stops decreasing, the rotor pole is completely separated from the stator pole. The phase inductance is at the minimum, L_u. For this reason, the

direction and the amplitude of the machine torque rely on the changing rate of the phase inductance.

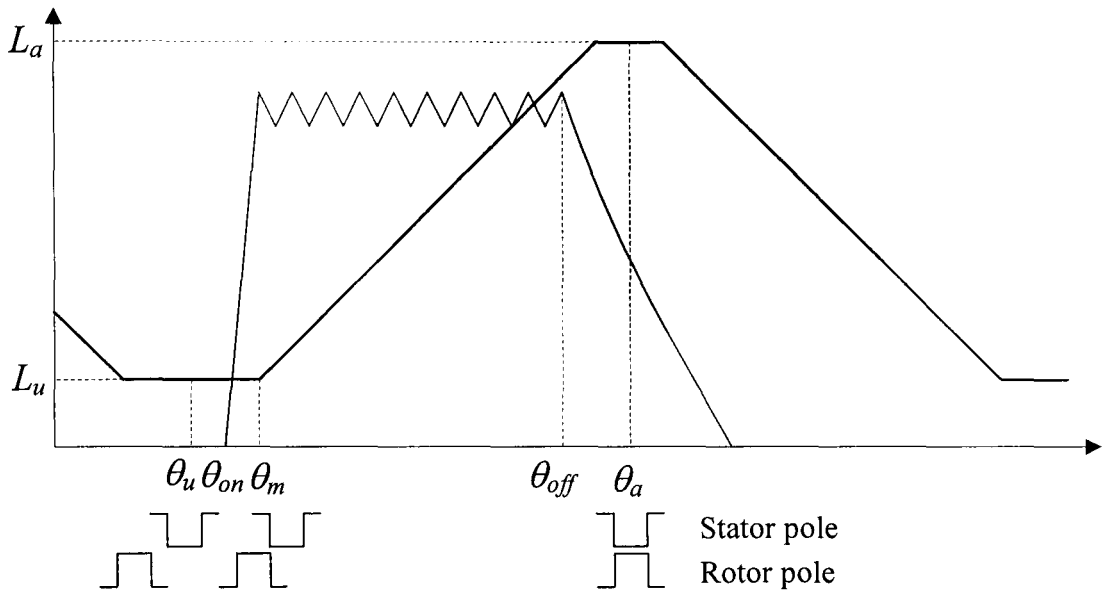


Figure 1.4: Relationship among phase current, phase inductance, and rotor position

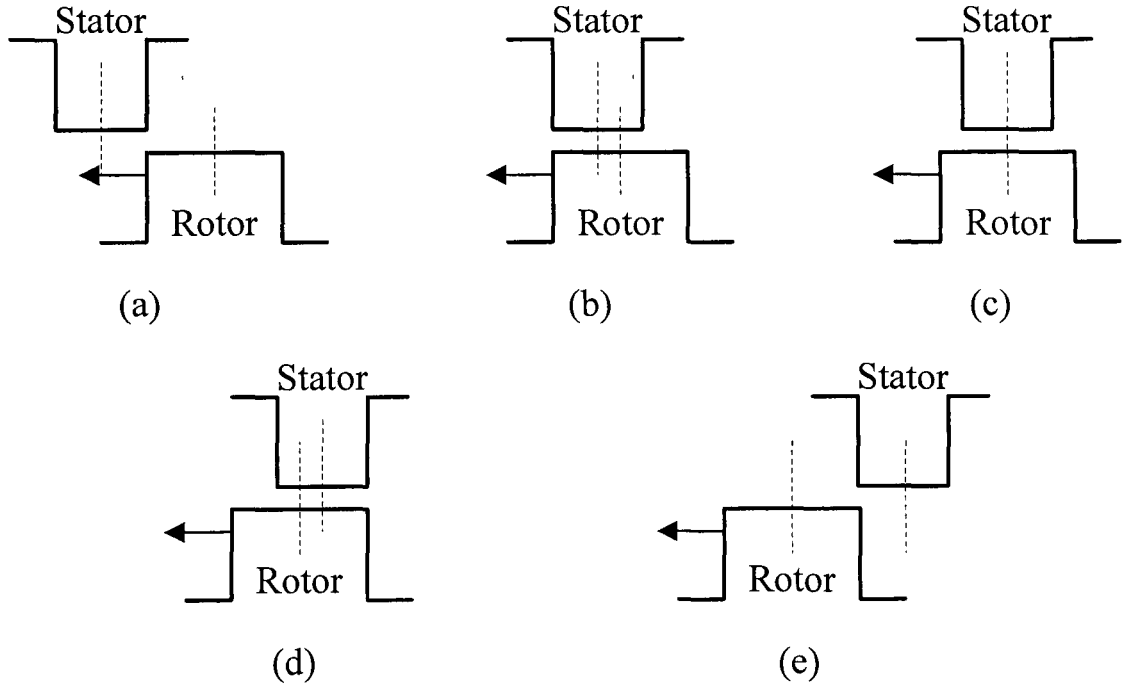


Figure 1.5: Stator and rotor movement

The relationship among the ideal phase inductance, the phase current and the phase torque is presented in Figure 1.6. The phase current, I_{ph}, is fed constantly in an

electrical cycle, from θ_u to θ_u. If the slope of the phase inductance is positive, the phase torque is positive at $+T_{ph}$. This torque is called the motoring torque. On the other hand, if the slope of the phase inductance is negative, the phase torque is negative at $-T_{ph}$. This torque is called the generating torque. If the slope of the phase inductance is zero, the phase torque is zero. To obtain the continuous motoring torque, the phase current is excited during the increasing inductance region from one phase to another phase, as shown in Figure 1.7. In a three-phase motor, the excitation phase currents of phase1 (I_{ph1}), phase2 (I_{ph2}) and phase3 (I_{ph3}) are fed consecutively. The machine torque is produced from the summation of those phase torque.

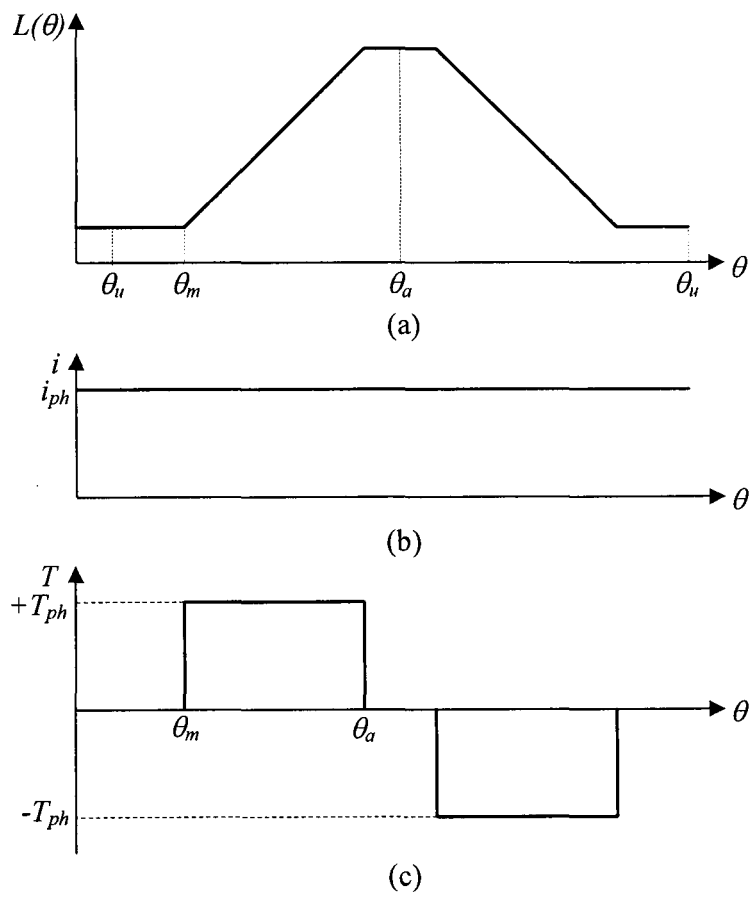


Figure 1.6: Relationship among (a) phase inductance, (b) phase current, and (c) phase torque

The machine torque is the summation of the rate of change of energy from each machine phase with the position, as expressed by

$$T(\theta, i_{ph}) = \sum_{ph=1}^{n} \frac{\partial W_m(\theta, i_{ph})}{\partial \theta} \tag{1.14}$$

where

T is torque of a machine phase.

W_m is the mechanical output energy of each phase.

i_{ph} is the phase current.

θ is the rotor position of the phase.

n is the number of the machine phase.

To simplify (1.14), the linkage flux is assumed to be non-saturable and linear. The simplified instantaneous torque equation becomes

$$T(\theta, i) = \sum_{ph=1}^{n} \frac{1}{2} i_{ph}^2 \frac{dL_{ph}}{d\theta} \tag{1.15}$$

where L_{ph} is the phase inductance.

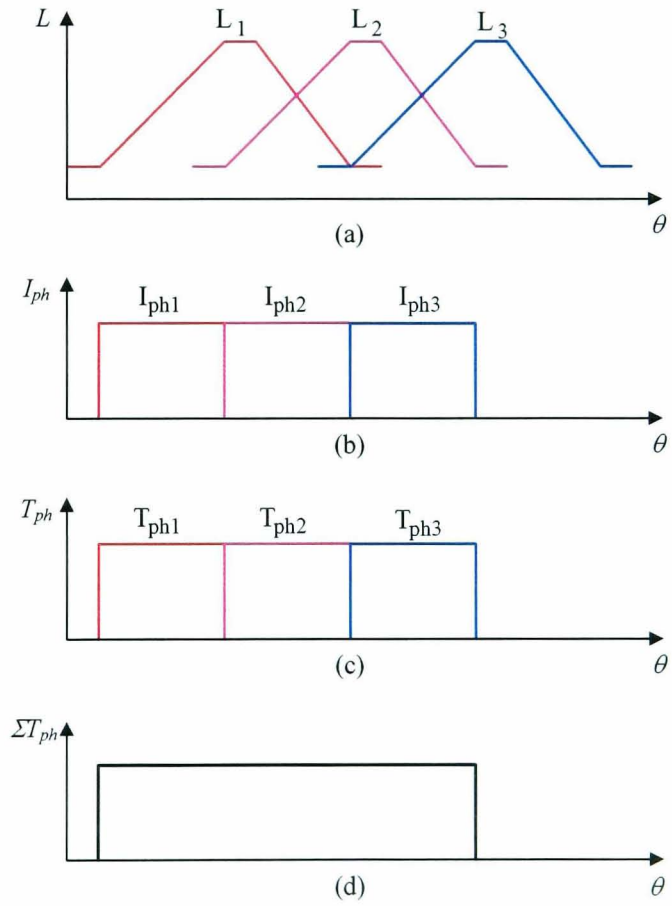


Figure 1.7: Ideal phase inductance (a), phase currents (b), phase torques (c) and machine torques (d)

Practically, the inductance, the phase current, the phase torque and the machine torque are not ideal, since the magnetic flux of SR machines is non-linear. The phase inductance does not increase and decrease linearly with the rotor position, as shown in Figure 1.8. The figure shows the simulated inductance, phase currents, phase torques and the machine torque in a practical case. The inductance in Figure 1.8 is not like an ideal trapezoid inductance, as shown in Figure 1.7. Further, the phase currents cannot keep flat and smooth. The phase torques are also slightly different from the ideal waveform. Consequently the machine torque (ΣT_{ph}) of the practical waveform has large ripple.

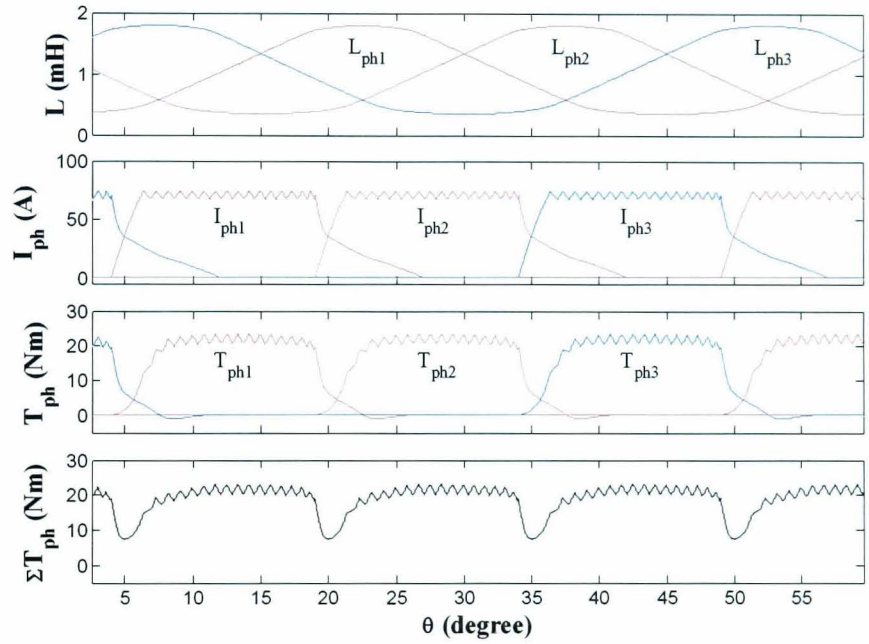


Figure 1.8: Practical phase inductance, phase currents, phase torques and machine

For decades, there are many researches proposing several methods to alleviate such problems. Those methods are categorised into 2 approaches. One method is to alter the design of SR machines, while the other is to improve the control scheme. In [1.41-1.44], the geometric design of the stator and rotor poles is enhanced by optimising the pole arcs, notches, air gaps and pole tips. Although these have been more or less achieved to reduce the torque ripple, some expenses, such as average torque and motor weight, are sacrificed [1.42]. For the control scheme, those methods are categorised into the following groups:

Current or flux waveform profiling: This method is a conventional way to minimise the torque ripple of SR machines [1.45]. The phase current waveform is calculated for a smooth torque before being installed into the control memory. Then, the pre-calculated phase current waveform is tracked during the machine operation. Sometimes flux linkage is used instead of the phase current [1.46]. In the calculation process, the optimisation, the torque sharing profile, or the overlapping between the phase currents are used to reduce the torque ripple [1.47-1.55]. However, at the low inductance slope region, high peak current may occurs. In [1.56], both current and voltage waveforms are optimised to prevent the spike voltage.

Feedback control: This method is to use feedback control to reduce the torque ripple. The machine parameters are directly and indirectly fed back to the controller and the demand torque is adjusted to eliminate the torque ripple. In [1.57-1.58], the torque is directly measured and fed back to the torque hysteresis controller. On the other hand, the machine torque is estimated and controlled by measured phase currents and positions in [1.59-1.60]. In [1.61], the co-energy is used to calculate and control torque. In [1.62], the flux linkage feedback is employed and linearly determined by measuring the machine position and phase currents. Still, the estimated toque is complex and inaccurate.

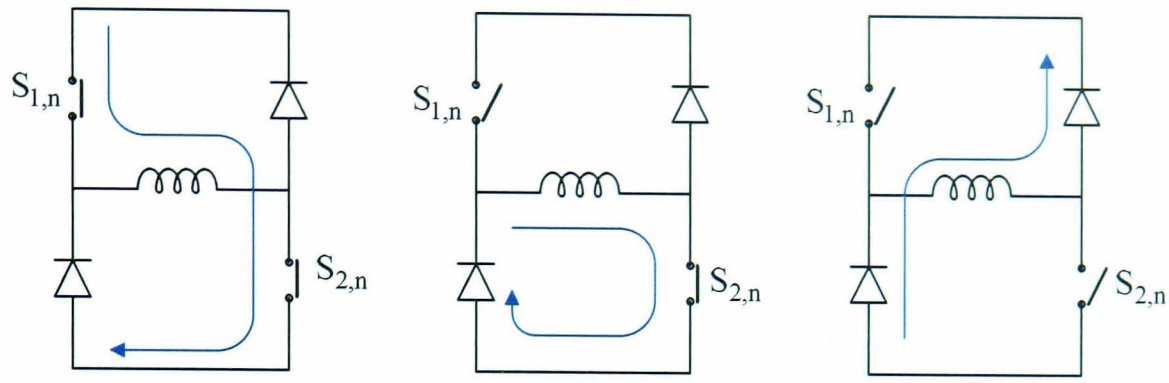
Intelligence control: In this method, iterative learning, fuzzy logic, and neutral network are applied to control the SR machines. In [1.63-1.64], the iterative learning control is used in learning process with the feedforward compensator. The production of the learning control is the current profile for minimum torque ripple. For fuzzy logic, it is used in various parts of the machine control. In [1.65], the fuzzy logic is used to find the optimal turn-off angle to minimise the torque ripple. Sometimes it is used to generate the demand current in the current loop [1.66] or generate the torque demand in the speed loop [1.67]. The neural network is used in torque estimation learning process in [1.68-1.69]. The torque estimator is created and employed in the experiment.

Nevertheless, due to the complex computation, the intelligence control is slow and not good in the dynamic response.

Other control: Cheok [1.70] presents a control method which uses flux and current to control SR machines. The space voltage vector from ac machines is applied to SR machines. In [1.70], it is claimed that the benefits of this technique are no need for torque and current profile or complex computation. The torque ripple is automatically reduced. However, the torque estimation module is used and only three-phase machine can be applied.

1.2.3 Soft Chopping, Hard Chopping and Conduction State

Current chopping is a method for feeding the electrical current into the SR machine phase winding. This is usually achieved using a half bridge circuit as shown in Figure 1.9. In [1.71], chopping is classified into 2 types: soft chopping and hard chopping. Each type includes several conduction states. However, in this thesis, the chopping is classified as an individual conduction state. Three conduction states of the chopping are described. The first state is called 'turn-on' state, as shown in Figure 1.9(a), when $S_{1,n}$ and $S_{2,n}$ are turned on. The current flows into the phase winding. The second state, in Figure 1.9(b), is called 'soft turn-off ' in which $S_{2,n}$ is turned on and $S_{1,n}$ is turned off. The phase current freewheels within the converter and the phase winding. The third state, in Figure 1.9(c), is called ' hard turn-off ' when both $S_{1,n}$ and $S_{2,n}$ are turned off. The phase current is discharged from the phase winding.



(a) Turn-on (b) Soft turn-off (c) Hard turn-off

Figure 1.9: Switch conduction states

1.2.4 Current Control and Voltage Control

In this thesis, there are 3 types of conventional methods used to control SR machines: hysteresis current control (HCC) [1.3], pulse-width modulation current control (PWMCC) [1.50] and pulse-width modulation voltage control (PWMVC) [1.90].

In HCC, the phase current is controlled to swing up and down in a narrow band, which is called hysteresis band, as shown in Figure 1.10. The starting point to control the phase current is the turn-on angle (θ_{on}). At θ_{on}, the phase converter is in the 'turn-on' state. The phase current rises fast until it reaches the upper limit of the hysteresis band. Then, the soft turn-off state occurs in the converter. The amplitude of the phase current is gradually dropped until the lower limit of the hysteresis band. The converter is changed to the turn-on state again. This process is repeated and stopped at the turn-off angle (θ_{off}). The converter is in the hard turn-off state. The phase current is discharged from the phase winding. The period from θ_{on} to θ_{off} is called the dwell period.

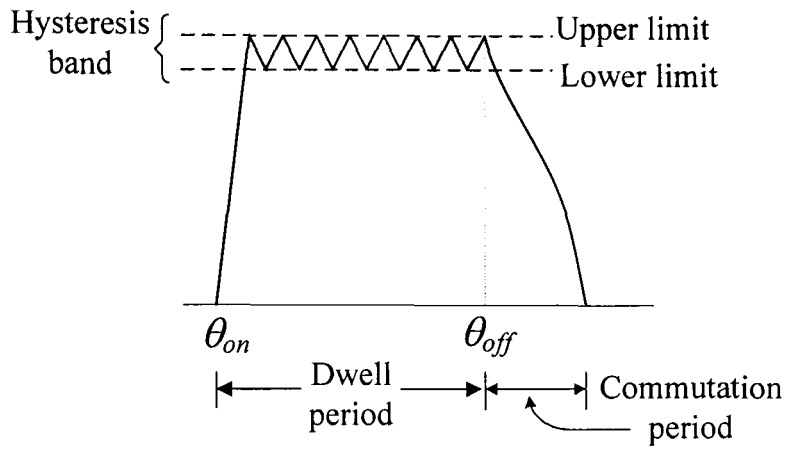


Figure 1.10: Phase current controlled by HCC

After passing the dwell period, that phase is called the outgoing phase and the next phase is called the incoming phase. The phase current of the outgoing phase is discharged and the phase current of the incoming phase is charged. The period from θ_{off} to the end of the phase current of the outgoing phase is called the commutation period.

Pulse width modulation (PWM) is a common technique for current control and voltage control of motors. The difference between PWMCC and PWMVC is a duty cycle. The duty cycle in PWMVC is constant during the dwell period while that in PWMCC is varied and is controlled by a PI controller. PWMCC is used in Chapter 2 for comparing the simulation results with other techniques when the dwell period is equal to the stroke period. The stroke period is found from (1.16). It is noticed that when the dwell period is equal to the stroke period, there is no overlap between the dwell period of each phase.

$$\varepsilon = \frac{360}{N_{ph} \times N_r} \tag{1.16}$$

where

ε is stroke angle in degree unit.

N_{ph} is the phase number of the SR machine.

N_r is the number of the rotor poles.

The PWMVC is used when the optimal turn-on angle can be applied since the beginning period which the phase current rises from zero to the demand current is longer than that of PWMCC. PWMVC is applied in Chapter 3 for the flux analysis.

1.2.5 Power Converter Circuit

The function of the converter is to apply appropriate voltage to the phase winding to facilitate electromechanical energy conversion. The converter circuit of the SR machine is simpler and more robust than those of other machines since the phase current is unipolar. The polarity of the phase current is independent of the direction of the torque. The converter just supplies the current to the phase winding without considering the polarity of the current. The conventional converter of the SR machines is called asymmetric H-bridge converter which has 2 switches and 2 diodes per phase. This converter is designed to operate with unipolar currents. The 3-phase H-bridge converter for an SR machine is shown in Figure 1.11.

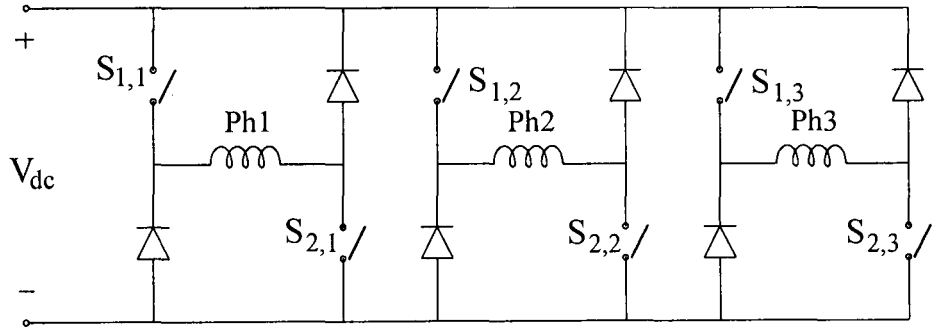


Figure 1.11: Three-phase H-bridge converter

In several literature, the converter has been developed to reduce loss and cost and to improve the efficiency. Some of the converters are briefly described here.

R-dump

Figure 1.12 shows three-phase converter with a shared resistor. This converter is designed to reduce the number of power components. It uses one switch and one diode per phase. The mid point of each phase is connected to a common point via a diode. The resistor connected between the common point and the positive terminal of the dc

supply is installed to dissipated the energy which is released during the turn-off of a phase winding, referred to as the de-fluxing energy. The capacitor between the dump resistor (R_d) and the ground is snubber capacitor. It decrease the voltage spike during the turn-off transient. The R-dump converter is simple and easy to exploit [1.28]. However, the resistor results in longer time for suppressing the de-fluxing energy [1.71]. To correct this, the turn-off angle is shifted to be early. By doing so, the converter is inefficient.

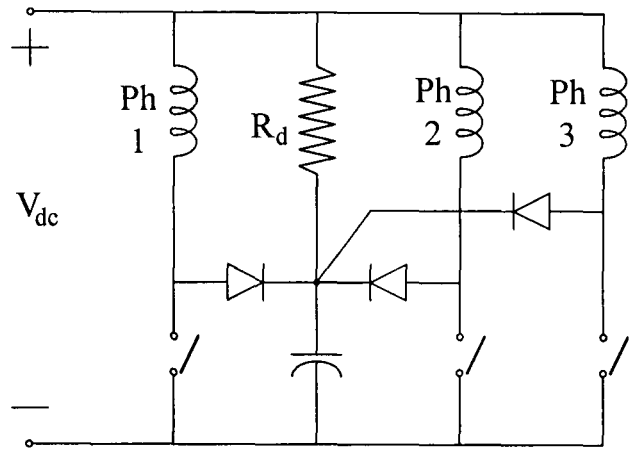


Figure 1.12: R-dump converter

C-dump

Figure 1.13 presents the C-dump circuit. This circuit consists of 1 switch, 1 diode per phase and other 4 components for a buck converter and a dump capacitor (C_d). The function of the dump capacitor is to partially store and gradually deliver the de-fluxing energy to the dc supply by chopping of the buck converter [1.72]. The de-fluxing energy is not completely discharged to the dc supply. The recovery winding (L_d) receives partially the discharging energy. The discharging of the C-dump takes place during the turn-on period of the phase winding.

The main advantage of the circuit is minimising the number of the switches per phase with independent phase current control and more efficient utilisation of energy [1.28]. Nevertheless, the buck converter components and the dump capacitor are large and the voltage across the dump capacitor has to be kept higher than the supply voltage in order to rapidly discharge the phase current [1.8].

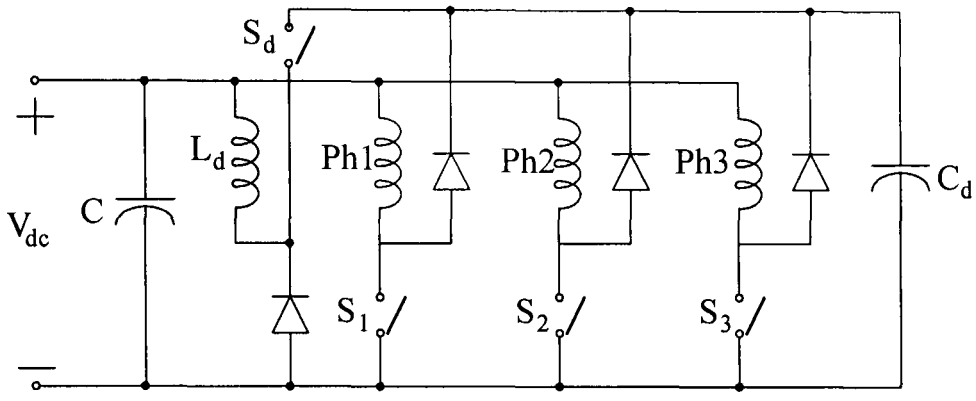


Figure 1.13: C-dump circuit

Bifilar

This type of the SR converter also has 1 switch and 1 diode per phase, as shown in Figure 1.14. The machine winding has to be altered to have 2 windings per phase: primary and secondary windings. The primary winding couples closely with the secondary winding. The de-fluxing energy is discharged via the secondary winding. The benefit of this converter is to reduce the number of the power electronic components by using magnetic coupling. However, the coupling is not ideal in a practical system. The peak voltage of the switch is twice of the supply voltage and the magnetic coupling between the primary and the secondary winding is imperfect [1.71]. High turn-off spikes occur and snubber circuits are needed [1.72]. Since the bifilar converter has 2 windings per phase, it increases the slot volume in the machine. This reduces the power density of the SR machine [1.73].

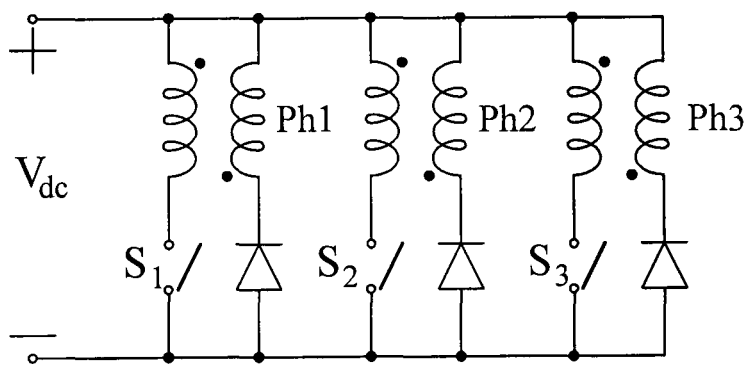


Figure 1.14: Bifilar converter circuit

Split dc supply

This converter uses only 1 switch and 1 diode per phase. The advantage of this circuit is one switch and one diode per phase. The two-phase circuit of the split dc supply converter is illustrated in Figure 1.15. The dc-link capacitor is split into 2 capacitors in series. Half of the dc supply voltage is applied to the phase winding at any time. However, the voltage across the free wheeling diode is still full of the dc supply. The disadvantage is that the charging between the capacitors has to balance carefully and the soft turn-off is not possible [1.71].

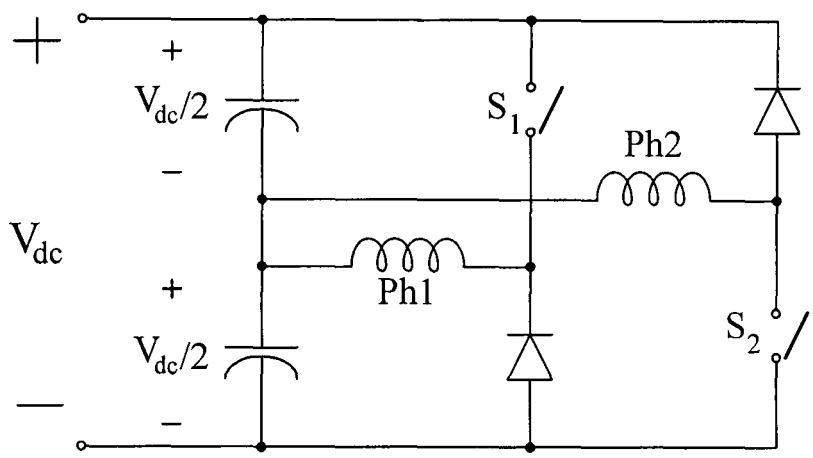


Figure 1.15: Split dc supply circuit

Share switch

Figure 1.16(a) shows the two-phase converter circuit which has 3 switches and 3 diodes. The number of the switches in the converter is reduced by utilising the switches between phases. Apart from reducing the number of power electronic components, the benefits of this converter is that the soft turn-off can be realised in this converter. However, the drawback of this converter is that the middle switch has to withstand 2 times of the phase current. Moreover, during a commutation period, the phase currents are not independent since the adjoining phases cannot be fluxed and de-fluxed at the same time. This reduces the fault tolerance property of the converter.

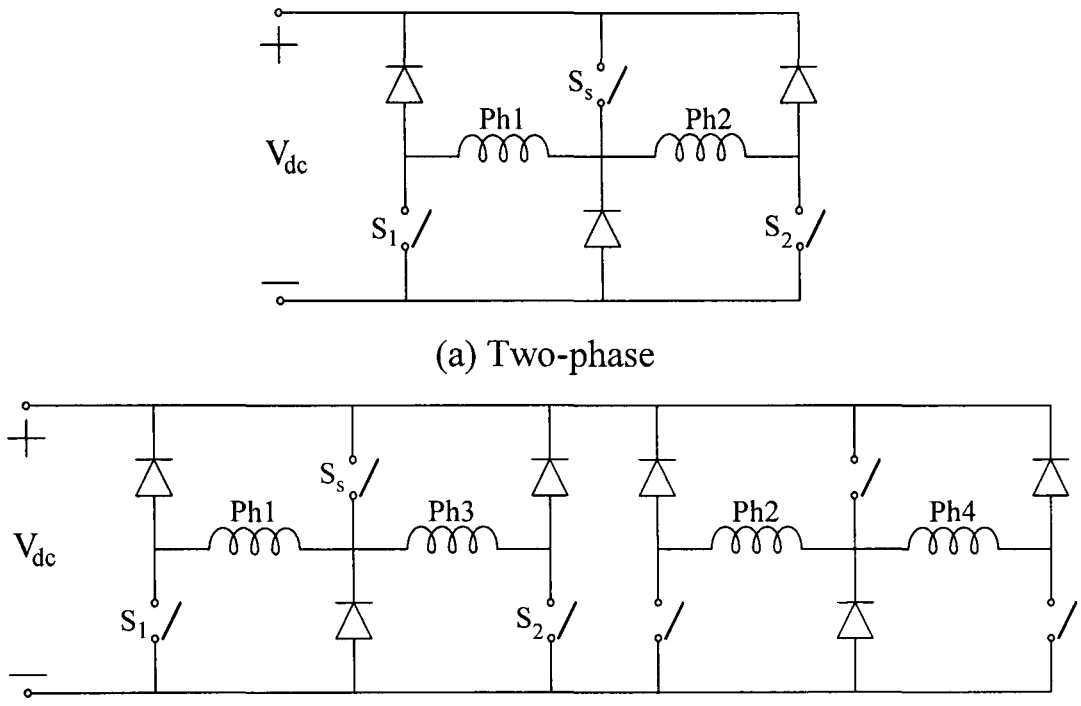


Figure 1.16: Shared switch converter

Due to the previous stated control problem, the shared switch converter is developed to a four-phase converter, as shown in Figure 1.16(b). While phase1 is de-fluxed, phase2 can be fluxed in the same time since phase1 is not placed next to phase2. It is placed next to phase3 and phase2 is placed next to phase4. Although the four-phase converter is developed to increase the control flexibility, the fault tolerance is still not as good as the asymmetrical H-bridge converter since each phase of this converter is not truly independent [1.71].

1.3 Dc-link Capacitor

DC link capacitors (C) are mounted between a dc supply (V_{dc}) and the converter in SR machine drives, as shown in Figure 1.17. The function of the dc-link capacitor is to buffer the transferred energy between the dc supply and the converter and to keep the supply voltage stable and smooth [1.74-1.75]. In aerospace application, the drive must meet the military (MIL) standards of power quality at its terminals when connected to a

dc supply. Further details of MIL standards is in Chapter 4. It is therefore necessary to include series *RL* filter components, R_{filter} and L_{filter}. The function of L_{filter} is to attenuate the supply current harmonic and that of R_{filter} is to provide some damping for second order filter. If a long cable is used between the dc supply and the converter, the inductance and resistance of the cable (L_{cable} and R_{cable}) can be lump into RLC representation.

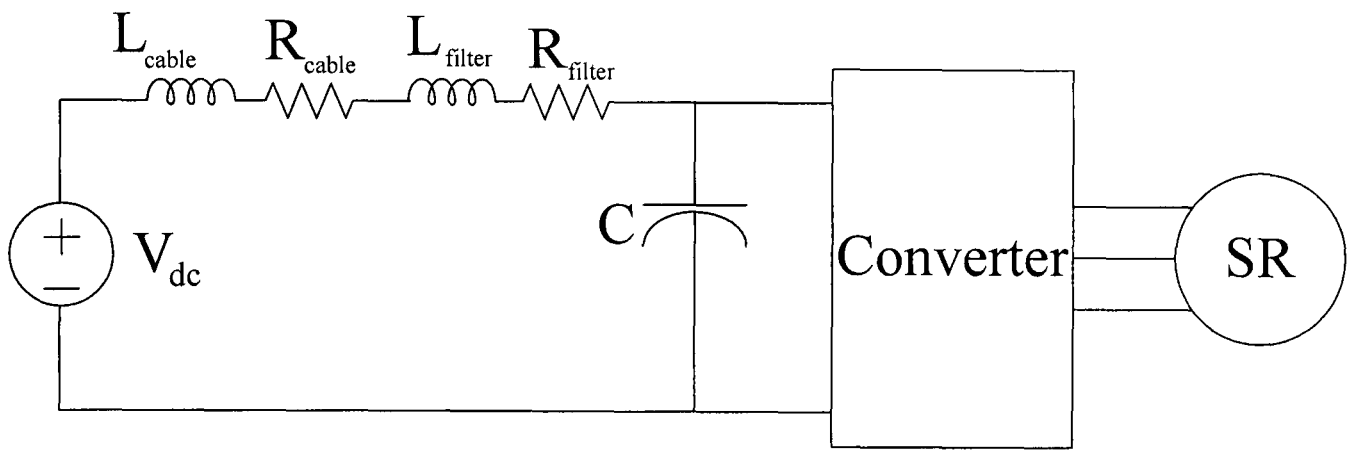


Figure 1.17: Schematic of SR machine drive

The basic requirements for the good dc-link capacitor include high Root Mean Square (rms) current capability, high operation voltage, low equivalent series resistance (ESR) and low equivalent series inductance (ESL), wide range of operation temperature, long life time, and high capacitance density [1.77-1.81]. Generally, the size of the dc-link capacitor of an SR machine is large since it buffers a large amount of the de-fluxing energy from the outgoing phase. Thus, the electrolytic capacitor is often used as a dc-link capacitor in the SR drive due to the high capacitance density and low price. However, it has some drawbacks such as a short life time and low ambient temperature [1.82 -1.84]. Furthermore, it possibly explodes in failure mode [1.85]. This makes the reliability of the electrolytic capacitor low.

Film capacitors are a good alternative especially in safety critical applications since they have long life time expectancy, capable of ac current operation, and the self healing property which make it highly reliable. Yet the capacitance density of the film capacitor is low. Although the features per unit such as weight, volume and even price of the

electrolytic capacitor and the film capacitor are approximate, the capacitance of the film capacitor is approximately 10 times lower than that of the electrolytic capacitor [1.86]. This is a large obstacle to use the film capacitors in high power density applications and safety critical applications. The minimisation of the dc-link capacitance is therefore essential to resolve this problem.

Most literatures for minimization of the dc-link capacitance consider the capacitor between AC system and DC system where a front-end converter is used to control the input voltage [1.33-1.34, 1.86-1.88]. There are only 2 papers which offer control method to reduce the dc-link capacitance in SR machines. The power balancing control during the commutation period is proposed in [1.75]. The de-fluxing energy which is discharged from the outgoing phase is controlled equally to the fluxing energy of the incoming phase. This reduces the de-fluxing energy charging back to the dc-link capacitor during the commutation period. The other approach addresses the reduction of the dc-link capacitor voltage ripple by direct control [1.89]. The dc-link voltage is measured and limited by a switching control technique. The details of both papers are described in the next chapter.

1.4 Organisation of Thesis

As stated previously, switched reluctance machines have many advantages due to the unique construction of the machine and the converter characteristics, especially in the aspect of the fault tolerance which is desirable for safety critical applications. The dc-link capacitor, however, might be the weakest part of the machine drive [1.24]. The film capacitors have been used as an alternative since they are non-polarized and can operate in a high temperature ambient. However, the size and weight of the film capacitors are excessive. The capacitance of the dc-link capacitors should be reduced without compromising the SR drive performance.

This thesis proposes a new technique which is called dc-link current integration control (DLCIC). DLCIC reduces the dc-link capacitance without compromising the stability and power quality of the SR drive. The principle of DLCIC is to balance the power transfer between the dc supply and the SR converter. The average dc-link current during the switching period is maintained constant. When the average dc-link current is constant, the current drawn from the dc supply is also constant.

The objective of this thesis is

1) to develop the new technique, DLCIC, which is used to reduce the peak-to-peak dc-link voltage across the capacitor, compared to the HCC
2) to determine optimal turn-on and turn-off angles of DLCIC.
3) to compare the capacitance and the filter weight between the DLCIC and HCC.
4) to verify that DLCIC can operate in a practical system by implementing it in experiments.

The thesis is organised as follows. In Chapter 2, the principles of DLCIC and the mode of operation are described in detail. The techniques such as HCC and other control technique from literatures are explained and the simulations are performed. The outcomes from the simulations among the control techniques such as phase current and capacitor voltage are compared. The spectra which are obtained by taking the Fast Fourier Transform (FFT) of the dc-link currents from the described techniques are compared and analysed.

The optimal turn-on and turn-off angles of HCC and DLCIC are analysed and explained in Chapter 3. The properties of both control methods such as phase currents and torque per ampere from the optimal angles of HCC and DLCIC are compared and analysed. The operation speed range of DLCIC is determined. The machine fluxes due to the phase currents which result from HCC, Pulse Width Modulation Voltage Control (PWMVC) and DLCIC are compared. Based on these analyses, an analytical approach to estimate the optimal turn-on and turn-off angles of DLCIC are described.

In Chapter 4, the input filters which are used in the operation of DLCIC and HCC are designed. The dc-link capacitance and the weight of the filter are compared. In Chapter 5, the experiments of DLCIC and HCC are carried out and explained in detail. Both control techniques are performed on the same machine and drive system, as well as the dc-link capacitor. The structure and the design of hardware and software are illustrated. The experimental outcomes from HCC and DLCIC are shown and compared. The spectra of the dc-link currents from both techniques are generated and compared by using FFT. The results of this research work are summarised and the future works are suggested in Chapter 6.

1.5 Reference

[1.1] F. J. Bartos. (1999, Nov. 1) 'Forward To The Past' With SR technology. *Control Engineering Mag.*

[1.2] A. F. Anderson, "Development history," in *Electronic Control of Switched Reluctance Machines*, T. J. E. Miller, Ed., ed: Newnes, 2001, pp. 6-33.

[1.3] B. K. Bose, "Power Electronics and Motor Drives Recent Progress and Perspective," *Industrial Electronics, IEEE Transactions on,* vol. 56, pp. 581-588, 2009.

[1.4] T. Humiston and P. Pillay, "Flux weakening operation of switched reluctance motors," in *Proc. Power Engineering Society Winter Meeting, 2001. IEEE*, 2001, pp. 1372-1377 vol.3.

[1.5] P. C. Kjaer, P. Nielsen, L. Andersen, and F. Blaabjerg, "A new energy optimizing control strategy for switched reluctance motors," *Industry Applications, IEEE Transactions on,* vol. 31, pp. 1088-1095, 1995.

[1.6] A. G. Jack, B. C. Mecrow, and J. Haylock, "A comparative study of permanent magnet and switched reluctance motors for high performance fault tolerant applications," in *Industry Applications Conference, 1995. Thirtieth IAS Annual Meeting, IAS '95., Conference Record of the 1995 IEEE*, 1995, pp. 734-740 vol.1.

[1.7] P. J. Lawrenson, J. M. Stephenson, N. N. Fulton, P. T. Blenkinsop, and J. Corda, "Variable-speed switched reluctance motors," *Electric Power Applications, IEE Proceedings B,* vol. 127, pp. 253-265, 1980.

[1.8] C. Pollock and A. Michaelides, "Switched reluctance drives: a comparative evaluation," *Power Engineering Journal,* vol. 9, pp. 257-266, 1995.

[1.9] M. E. Elbuluk and M. D. Kankam, "Potential starter/generator technology for future aerospace application," *Aerospace and Electronic Systems Magazine, IEEE,* vol. 11, pp. 17-24, 1996.

[1.10] X. M. Zhu, S. K. Panda, P. K. Dash, and S. H. Tan, "Experimental investigation of variable structural PID control for switched reluctance motor drives," in *Power Electronics and Drive Systems, 1997. Proceedings., 1997 International Conference on*, 1997, pp. 205-210 vol.1.

[1.11] K. I. Hwu and C. M. Liaw, "DC-link voltage boosting and switching control for switched reluctance motor drives," *Electric Power Applications, IEE Proceedings -,* vol. 147, pp. 337-344, 2000.

[1.12] I. Husain and S. A. Hossain, "Modeling, Simulation, and control of switched reluctance motor drives," *Industrial Electronics, IEEE Transactions on,* vol. 52, pp. 1625-1634, 2005.

[1.13] K. M. Rahman and S. E. Schulz, "High-performance fully digital switched reluctance motor controller for vehicle propulsion," *Industry Applications, IEEE Transactions on,* vol. 38, pp. 1062-1071, 2002.

[1.14] L. Szabo and M. Ruba, "On fault tolerance increase of switched reluctance machines," in *EUROCON 2009, EUROCON '09. IEEE*, 2009, pp. 734-739.

[1.15] M. Ruba, C. Oprea, and L. Szabo, "Comparative study on Switched Reluctance Machine based fault-tolerant electrical drive systems," in *Electric Machines and Drives Conference, 2009. IEMDC '09. IEEE International*, 2009, pp. 987-992.

[1.16] K. W. E. Cheng, Y. P. B. Yeung, C. Y. Tang, X. D. Xue, and D. Sutanto, "Topology analysis of switched reluctance drives for electric vehicles," in *Power Electronics and Variable Speed Drives, 2000. Eighth International Conference on (IEE Conf. Publ. No. 475)*, 2000, pp. 512-517.

[1.17] B. A. Kalan, H. C. Lovatt, and G. Prout, "Voltage control of switched reluctance machines for hybrid electric vehicles," in *Proc. Power Electronics Specialists Conference, 2002. pesc 02. 2002 IEEE 33rd Annual*, 2002, pp. 1656-1660.

[1.18] C. Hung-Chun and C. Liaw, "A battery powered switched-reluctance motor drive established using three-phase power module," in *Proc. Power Electronics and Drive Systems, 2009. PEDS 2009. International Conference on*, 2009, pp. 643-648.

[1.19] R. B. Inderka, M. Menne, and R. W. A. A. De Doncker, "Control of switched reluctance drives for electric vehicle applications," *Industrial Electronics, IEEE Transactions on,* vol. 49, pp. 48-53, 2002.

[1.20] S. E. Schulz and K. M. Rahman, "High-performance digital PI current regulator for EV switched reluctance motor drives," *Industry Applications, IEEE Transactions on,* vol. 39, pp. 1118-1126, 2003.

[1.21] J. Reinert, R. Inderka, M. Menne, and R. W. De Doncker, "Optimizing performance in switched reluctance drives," in *Applied Power Electronics Conference and Exposition, 1998. APEC '98. Conference Proceedings 1998., Thirteenth Annual*, 1998, pp. 765-770 vol.2.

[1.22] J. R. Briso-Montiano, R. Karrelmeyer, and E. Dilger, "Simulation of Faults by means of Finite Element Analysis in a switched Reluctance Motor," in *Proc. COMSOL Multiphysics User's Conference*, Frankfurt, 2005, pp. 225 - 231.

[1.23] Y. Zhen Zhong, T. W. Martin, and J. C. Balda, "An investigation of multiphase excitation nodes of a 10/8 switched reluctance motor with short flux path to maximize its average torque," in *Industrial Electronics, 2000. ISIE 2000. Proceedings of the 2000 IEEE International Symposium on*, 2000, pp. 390-395 vol.2.

[1.24] A. Boglietti, A. Cavagnino, A. Tenconi, and S. Vaschetto, "The safety critical electric machines and drives in the more electric aircraft: A survey," in *Industrial Electronics, 2009. IECON '09. 35th Annual Conference of IEEE*, 2009, pp. 2587-2594.

[1.25] K. Jaehyuck and R. Krishnan, "Single-controllable-switch-based switched reluctance motor drive for low-cost variable- speed applications," in *Proc. Energy Conversion Congress and Exposition, 2009. ECCE 2009. IEEE*, 2009, pp. 2535-2542.

[1.26] R. Krishnan, P. Sung-Yeul, and H. Keunsoo, "Theory and operation of a four-quadrant switched reluctance motor drive with a single controllable switch-the lowest cost four-quadrant brushless motor drive," *Industry Applications, IEEE Transactions on,* vol. 41, pp. 1047-1055, 2005.

[1.27] A. M. Staley and R. Krishnan, "Single controllable switch power converter for SRM drive systems," in *Proc. Industrial Electronics Society, 2005. IECON 2005. 31st Annual Conference of IEEE*, 2005, p. 6 pp.

[1.28] R. Krishnan and P. Materu, "Design of a Single-Switch-Per-Phase Converter for Switched Reluctance Motor Drives," in *Proc. Industrial Electronics Society, 1988. IECON '88. Proceedings., 14 Annual Conference of*, 1988, pp. 773-779.

[1.29] J. Liang, D. H. Lee, G. Xu, and J. W. Ahn, "Analysis of Passive Boost Power Converter for Three-Phase SR Drive," *Industrial Electronics, IEEE Transactions on,* vol. 57, pp. 2961-2971, 2010.

[1.30] S. K. Panda, X. M. Zhu, and P. K. Dash, "Fuzzy gain scheduled PI speed controller for switched reluctance motor drive," in *Proc. Industrial Electronics, Control and Instrumentation, 1997. IECON 97. 23rd International Conference on*, 1997, pp. 989-994 vol.3.

[1.31] A. Dahmane, F. Meebody, and F. M. Sargos, "A novel boost capacitor circuit to enhance the performance of the switched reluctance motor," in *Proc. Power Electronics Specialists Conference, 2001. PESC. 2001 IEEE 32nd Annual*, 2001, pp. 844-849 vol.2.

[1.32] C. Hung-Chun and C. Liaw, "On the Front-End Converter and Its Control for a Battery Powered Switched-Reluctance Motor Drive," *Power Electronics, IEEE Transactions on,* vol. 23, pp. 2143-2156, 2008.

[1.33] G. Bon-Gwan and N. Kwanghee, "A DC-link capacitor minimization method through direct capacitor current control," *Industry Applications, IEEE Transactions on,* vol. 42, pp. 573-581, 2006.

[1.34] H. Namho, J. Jinhwan, and N. Kwanghee, "A fast dynamic DC-link power-balancing scheme for a PWM converter-inverter system," *Industrial Electronics, IEEE Transactions on,* vol. 48, pp. 794-803, 2001.

[1.35] F. D. Kieferndorf, M. Forster, and T. A. Lipo, "Reduction of DC-bus capacitor ripple current with PAM/PWM converter," *Industry Applications, IEEE Transactions on,* vol. 40, pp. 607-614, 2004.

[1.36] C. Jui-Yuan and L. Chang-Ming, "Development of a Switched-Reluctance Motor Drive With PFC Front End," *Energy Conversion, IEEE Transactions on,* vol. 24, pp. 30-42, 2009.

[1.37] J. Corda and M. Oljaca, "Harmonic analysis of current waveforms in the D.C. link capacitor of a switched reluctance drive," presented at the Fifth Internation Conference on Electrical Machines and Drives, London, UK, 1991.

[1.38] I. Krishnan and S. Lee, "Effect of power factor correction circuit on switched reluctance motor drives for appliances," in *Proc. Applied Power Electronics Conference and Exposition, 1994. APEC '94. Conference Proceedings 1994., Ninth Annual*, 1994, pp. 83-89 vol.1.

[1.39] J. Reinert and S. Schroder, "Power-factor correction for switched reluctance drives," *Industrial Electronics, IEEE Transactions on,* vol. 49, pp. 54-57, 2002.

[1.40] D. A. Staton, W. L. Soong, and T. J. E. Miller, "Unified theory of torque production in switched reluctance and synchronous reluctance motors," *Industry Applications, IEEE Transactions on,* vol. 31, pp. 329-337, 1995.

[1.41] V. Prabhakar, M. Balaji, S. Ramkumar, and V. Kamaraj, "Influence of stator and rotor profiles on torque ripple minimization in SRM," in *Proc. Power Electronics, 2006. IICPE 2006. India International Conference on*, 2006, pp. 403-406.

[1.42] J. Hur, G. H. Kang, J. Y. Lee, J. P. Hong, and B. K. Lee, "Design and optimization of high torque, low ripple switched reluctance motor with flux barrier for direct drive," in *Proc. Industry Applications Conference, 2004. 39th IAS Annual Meeting. Conference Record of the 2004 IEEE*, 2004, p. 407 Vol.1.

[1.43] N. K. Sheth and K. R. Rajagopal, "Optimum pole arcs for a switched reluctance motor for higher torque with reduced ripple," *Magnetics, IEEE Transactions on,* vol. 39, pp. 3214-3216, 2003.

[1.44] C. Yong Kwon, Y. Hee Sung, and K. Chang Seop, "Pole-Shape Optimization of a Switched-Reluctance Motor for Torque Ripple Reduction," *Magnetics, IEEE Transactions on,* vol. 43, pp. 1797-1800, 2007.

[1.45] H. Hannoun, M. Hilairet, and C. Marchand, "Comparison of instantaneous and average torque control for a switched reluctance motor," in *Proc. Industrial Electronics, 2008. ISIE 2008. IEEE International Symposium on*, 2008, pp. 675-680.

[1.46] K. Russa, I. Husain, and M. E. Elbuluk, "Torque-ripple minimization in switched reluctance machines over a wide speed range," *Industry Applications, IEEE Transactions on,* vol. 34, pp. 1105-1112, 1998.

[1.47] S. K. Sahoo, S. Dasgupta, S. K. Panda, and X. Jian-Xin, "A Lyapunov Function-Based Robust Direct Torque Controller for a Switched Reluctance Motor Drive System," *Power Electronics, IEEE Transactions on,* vol. 27, pp. 555-564, 2012.

[1.48] X. D. Xue, K. W. E. Cheng, and S. L. Ho, "Optimization and Evaluation of Torque-Sharing Functions for Torque Ripple Minimization in Switched Reluctance Motor Drives," *Power Electronics, IEEE Transactions on,* vol. 24, pp. 2076-2090, 2009.

[1.49] I. Husain, "Minimization of torque ripple in SRM drives," *Industrial Electronics, IEEE Transactions on,* vol. 49, pp. 28-39, 2002.

[1.50] I. Husain and M. Ehsani, "Torque ripple minimization in switched reluctance motor drives by PWM current control," *Power Electronics, IEEE Transactions on,* vol. 11, pp. 83-88, 1996.

[1.51] P. C. Kjaer, J. J. Gribble, and T. J. E. Miller, "High-grade control of switched reluctance machines," *Industry Applications, IEEE Transactions on,* vol. 33, pp. 1585-1593, 1997.

[1.52] I. Agirman, A. M. Stankovic, G. Tadmor, and H. Lev-Ari, "Adaptive torque-ripple minimization in switched reluctance motors," *Industrial Electronics, IEEE Transactions on,* vol. 48, pp. 664-672, 2001.

[1.53] N. T. Shaked and R. Rabinovici, "New procedures for minimizing the torque ripple in switched reluctance motors by optimizing the phase-current profile," *Magnetics, IEEE Transactions on,* vol. 41, pp. 1184-1192, 2005.

[1.54] L. Venkatesha and V. Ramanarayanan, "Torque ripple minimisation in switched reluctance motor with optimal control of phase currents," in *Proc. Power Electronic Drives and Energy Systems for Industrial Growth, 1998. Proceedings. 1998 International Conference on*, 1998, pp. 529-534 Vol. 2.

[1.55] J. Y. Chai and C. M. Liaw, "Reduction of speed ripple and vibration for switched reluctance motor drive via intelligent current profiling," *Electric Power Applications, IET,* vol. 4, pp. 380-396, 2010.

[1.56] A. M. Stankovic, G. Tadmor, Z. J. Coric, and I. Agirman, "On torque ripple reduction in current-fed switched reluctance motors," *Industrial Electronics, IEEE Transactions on,* vol. 46, pp. 177-183, 1999.

[1.57] R. B. Inderka and R. W. De Doncker, "DITC-direct instantaneous torque control of switched reluctance drives," in *Proc. Industry Applications Conference, 2002. 37th IAS Annual Meeting. Conference Record of the*, 2002, pp. 1605-1609 vol.3.

[1.58] N. H. Fuengwarodsakul, M. Menne, R. B. Inderka, and R. W. De Doncker, "High-dynamic four-quadrant switched reluctance drive based on DITC," *Industry Applications, IEEE Transactions on,* vol. 41, pp. 1232-1242, 2005.

[1.59] K. Youn-Hyun, L. Han-Seoung, K. Sol, and L. Ju, "Advanced torque control of switched reluctance motor," in *Proc. Industrial Electronics, 2001. Proceedings. ISIE 2001. IEEE International Symposium on*, 2001, pp. 1798-1803 vol.3.

[1.60] P. Chancharoensook, "Direct instantaneous torque control of a four-phase switched reluctance motor," in *Proc. Power Electronics and Drive Systems, 2009. PEDS 2009. International Conference on*, 2009, pp. 770-777.

[1.61] P. C. K. Luk and K. P. Jinupun, "Direct work control technique for switched reluctance motors," in *Proc. Power Electronics and Motion Control Conference, 2004. IPEMC 2004. The 4th International*, 2004, pp. 1044-1048 Vol.2.

[1.62] P. G. Barrass and B. C. Mecrow, "Flux and torque control of switched reluctance machines," *Electric Power Applications, IEE Proceedings -,* vol. 145, pp. 519-527, 1998.

[1.63] N. C. Sahoo, J. X. Xu, and S. K. Panda, "Low torque ripple control of switched reluctance motors using iterative learning," *Energy Conversion, IEEE Transactions on,* vol. 16, pp. 318-326, 2001.

[1.64] S. K. Sahoo, S. K. Panda, and J. Xu, "Indirect torque control of switched reluctance motors using iterative learning control," *Power Electronics, IEEE Transactions on,* vol. 20, pp. 200-208, 2005.

[1.65] M. Rodrigues, P. J. Costa Branco, and W. Suemitsu, "Fuzzy logic torque ripple reduction by turn-off angle compensation for switched reluctance motors," *Industrial Electronics, IEEE Transactions on,* vol. 48, pp. 711-715, 2001.

[1.66] S. Mir, M. E. Elbuluk, and I. Husain, "Torque-ripple minimization in switched reluctance motors using adaptive fuzzy control," *Industry Applications, IEEE Transactions on,* vol. 35, pp. 461-468, 1999.

[1.67] B. Singh, V. K. Sharma, and S. S. Murthy, "Performance analysis of adaptive fuzzy logic controller for switched reluctance motor drive system," in *Proc. Industry Applications Conference, 1998. Thirty-Third IAS Annual Meeting. The 1998 IEEE*, 1998, pp. 571-579 vol.1.

[1.68] J. G. O'Donovan, P. J. Roche, R. C. Kavanagh, M. G. Egan, and J. M. D. Murphy, "Neural network based torque ripple minimisation in a switched reluctance motor," in *Proc. Industrial Electronics, Control and Instrumentation, 1994. IECON '94., 20th International Conference on*, 1994, pp. 1226-1231 vol.2.

[1.69] Z. Lin, D. S. Reay, B. W. Williams, and X. He, "Torque Ripple Reduction in Switched Reluctance Motor Drives Using B-Spline Neural Networks," *Industry Applications, IEEE Transactions on,* vol. 42, pp. 1445-1453, 2006.

[1.70] A. D. Cheok and Y. Fukuda, "A new torque and flux control method for switched reluctance motor drives," *Power Electronics, IEEE Transactions on,* vol. 17, pp. 543-557, 2002.

[1.71] T. J. E. Miller, "Switched reluctance motors and their control," vol. 31. Oxford: Magna Physics Publishing and Clarendon Press, 1993.

[1.72] M. Barnes and C. Pollock, "Power electronic converters for switched reluctance drives," *Power Electronics, IEEE Transactions on,* vol. 13, pp. 1100-1111, 1998.

[1.73] R. Krishnan, "Switched Reluctance Motor Drives: Modeling, Simulation, Analysis, Design, and Applications", CRC Press, 2001.

[1.74] J. W. Kolar and S. D. Round, "Analytical calculation of the RMS current stress on the DC-link capacitor of voltage-PWM converter systems," *Electric Power Applications, IEE Proceedings -,* vol. 153, pp. 535-543, 2006.

[1.75] C. R. Neuhaus, N. H. Fuengwarodsakul, and R. W. De Doncker, "Control Scheme for Switched Reluctance Drives With Minimized DC-Link Capacitance," *Power Electronics, IEEE Transactions on,* vol. 23, pp. 2557-2564, 2008.

[1.76] C. Broche, J. Lobry, P. Colignon, and A. Labart, "Harmonic reduction in DC link current of a PWM induction motor drive by active filtering," *Power Electronics, IEEE Transactions on,* vol. 7, pp. 633-643, 1992.

[1.77] D. Montanari, K. Saarinen, F. Scagliarini, D. Zeidler, M. Niskala, and C. Nender, "Film Capacitor for Automotive and Industrail Applications," presented at the CARTS Europe, Helsinki, Finland, 2008.

[1.78] G. Terzulli and B. W. Peace. (Jan. 9, 2012). *Film technology to replace electrolytic technology.* Available: http://www.avx.com/docs/techinfo/filmtech.pdf

[1.79] W. J. Sarjeant, J. Zirnheld, and F. W. MacDougall, "Capacitors," *Plasma Science, IEEE Transactions on,* vol. 26, pp. 1368-1392, 1998.

[1.80] M. Bramoulle, "Electrolytic or film capacitors?," in *Proc. Industry Applications Conference, 1998. Thirty-Third IAS Annual Meeting. The 1998 IEEE*, 1998, pp. 1138-1141 vol.2.

[1.81] F. Esteban and I. Vazquez. (2006). *Film capacitors for DC-link application in industrail converters.* Available: http://www.ec-central.org/CARTSEurope/2008/index.html

[1.82] K. Kretschmar and H. P. Nee, "An AC converter with a small DC link capacitor for a 15 kW permanent magnet synchronous integral motor," in *Power Electronics and Variable Speed Drives, 1998. Seventh International Conference on (Conf. Publ. No. 456)*, 1998, pp. 622-625.

[1.83] E. Sawyer, "New Inverter layout and DC Link Capacitor integration for increased system density and performance," in *Industrial Electronics, 2008. IECON 2008. 34th Annual Conference of IEEE*, 2008, pp. 2818-2822.

[1.84] F. Schimpf and L. Norum, "Effective use of film capacitors in single-phase PV-inverters by active power decoupling," in *Proc. IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society*, 2010, pp. 2784-2789.

[1.85] L. L. Macomber, "Aluminum Electrolytic Capacitors in Power Electronics," presented at the Applied Power Electronics Conference and Exposition (APEC), Fort Worth, TX, 2011.

[1.86] S. J. Forrest, "AC Fed Direct Converter for a Switched Reluctance Machine in Aerospace Applications," Ph.D. thesis, Dept. EEE, University of Sheffield, Sheffield, 2010.

[1.87] J. G. Hwang, P. W. Lehn, and M. Winkelnkemper, "Control of grid connected AC-DC converters with minimized DC link capacitance under unbalanced grid voltage condition," in *Proc. Power Electronics and Applications, 200- European Conference on*, 2007, pp. 1-10.

[1.88] A. Kotsopoulos, J. L. Duarte, and M. A. M. Hendrix, "A predictive control scheme for DC voltage and AC current in grid-connected photovoltaic inverters with minimum DC link capacitance," in *Proc. Industrial Electronics Society, 2001. IECON '01. The 27th Annual Conference of the IEEE*, 2001, pp. 1994-1999 vol.3.

[1.89] C. R. Neuhaus and R. W. De Doncker, "DC-link voltage control for Switched Reluctance Drives with reduced DC-link capacitance," in *Proc. Energy Conversion Congress and Exposition (ECCE), 2010 IEEE*, 2010, pp. 4192-4198.

[1.90] J. J. Gribble, P. C. Kjaer, and T. J. E. Miller, "Optimal commutation in average torque control of switched reluctance motors," *Electric Power Applications, IEE Proceedings -*, vol. 146, pp. 2-10, 1999.

Chapter 2

Proposed switching technique

2.1 Introduction

The principle of operation and potential converter topologies for switched reluctance (SR) machines have been described in detail in Chapter1. The problems of dc-link capacitors in relation to an aerospace application are also addressed in Chapter1. For example, the volume and weight of the dc-link capacitor to meet the requirement of stability and power quality in a safety critical application may be too high. A new technique is proposed in this chapter to reduce the required dc-link capacitance, whilst maintaining stability and power quality.

The new technique, which is called the Dc-Link Current Integration Control (DLCIC), provides the means to reduce the capacitance of the dc-link capacitor. The function of the dc-link capacitor is to filter out high frequency current from the converter, and hence to reduce the peak to peak voltage which fluctuates at the input terminals of the converter. If the peak to peak voltage is diminished, the capacitance of the dc-link

capacitor can be reduced, and consequently reduces the weight and volume of the capacitor.

In this chapter, the literatures which propose the techniques to minimise the dc-link current capacitance are reviewed. The principles of DLCIC will be explained and the simulation program will be described and analysed. The results from the simulation, such as the capacitor voltage and the input current from the dc supply, will be shown and compared with other control techniques such as Hysteresis Current Control (HCC). Furthermore, the analysis of the dc-link current by Fast Fourier Transform (FFT) will be performed and discussed.

2.2 Review of Literature

The de-fluxing energy of SR machines, which is up to 30% of the stroke energy, is fed back to the dc supply and dc-link capacitance [2.1-2.7]. This is the main reason for the requirement of an increased dc-link capacitance, compared to other machine and drive combinations, which may effect the reliability and stability of the drive system. Reducing the size of the dc-link capacitor yields many benefits such as a reduction in the cost and volume of the converter circuit. Nonetheless, there are few papers that propose techniques to reduce the dc-link capacitor size of the SR drive.

Liang *et al.* [2.8] proposes a method to reduce the dc-link capacitance by adding an auxiliary commutation winding inside an SR machine, as shown in Figure 2.1. The de-fluxing energy of the outgoing phase is transferred to the extra winding and then is gradually fed to the incoming phase winding without passing through the dc-link current path. Since the energy transfer between the outgoing phase and the auxiliary winding is directly coupled by magnetic linkage, the phase current of the outgoing phase is discharged much faster than the case without the extra winding. This also makes the turn-off angle of the outgoing phase closer to the aligned position.

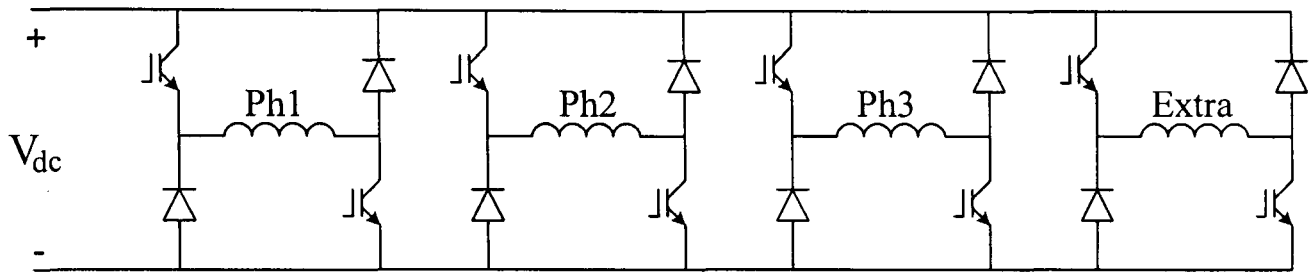


Figure 2.1: Asymmetric half bridge converter with auxiliary winding

The efficiency of the machine is increased since the excess energy is brought back to the incoming phase without causing a negative torque. The machine torque of the incoming phase rises due to the excess energy, but this leads to increased torque ripple. With the extra winding in the SR machine, the motor design is altered and another phase circuit in the converter has to be added. These increase the cost and the weight of the machine and drive.

There are only 2 papers which propose methods to reduce the dc-link capacitance without altering the converter circuit and the machine design. The first paper is from Neuhaus *et al.* [2.9]. It prevents the de-fluxing energy from flowing back to the dc-link capacitor during the commutation period. The other method is presented in [2.10] where the voltage of the dc-link capacitor is directly controlled.

2.2.1 Power Balancing Control

From [2.9], since a significant amount of de-fluxing energy in an SR machine is fed back to the dc-link capacitor which is used as a filter or buffer, it is assumed that if the de-fluxing energy is controlled, the dc-link capacitance can be reduced. The rate of change of magnetic energy of the outgoing phase and the incoming phase are balanced to avoid the energy from the motor flowing back to the dc-link capacitor. The de-fluxing power of the outgoing phase is equal to the fluxing power of the incoming phase. This technique is called Power Balancing Control (PBC). The absolute values of the differential change of the energy in outgoing phase and incoming phase during the commutation period are controlled to be equal, as expressed in (2.1)

$$-\frac{dW_n}{dt} = \frac{dW_{n+1}}{dt} \tag{2.1}$$

where

W_n is the de-fluxing energy of the outgoing phase.

W_{n+1} is the fluxing energy of the incoming phase.

From the current characteristic of the magnetic energy is given by (2.2)

$$\frac{dW_{mag}}{dt} = i(\psi,\theta)\frac{d\psi}{dt} \tag{2.2}$$

where

W_{mag} is the magnetic energy.

i is the current in the coil.

ψ is the flux linkage.

θ is the position angle of the machine.

Substituted (2.2) into (2.1) gives the change of the magnetic energy (2.3)

$$-i_n\frac{d\psi_n}{dt} = i_{n+1}\frac{d\psi_{n+1}}{dt} \tag{2.3}$$

where

i_n is the outgoing phase current.

i_{n+1} is the incoming phase current.

ψ_n is the outgoing flux linkage.

ψ_{n+1} is the incoming flux linkage.

With Pulse Width Modulation (PWM) control method, the change of the flux linkage is calculated as

$$\frac{d\psi}{dt} = a \cdot V_{dc} \tag{2.4}$$

where

a is the duty cycle.

V_{dc} is the dc supply voltage.

Then, (2.3) can be simplified as

$$-i_n a_n \cdot V_{dc} = i_{n+1} a_{n+1} \cdot V_{dc} \tag{2.5}$$

where

a_n is the duty cycle of the outgoing phase.

a_{n+1} is the duty cycle of the incoming phase.

In [2.9], the incoming phase current is not controlled in order to make the machine torque growing quickly. Thus, the duty cycle of the incoming phase is generated from the demand torque. The outgoing phase current is controlled by the duty cycle as follows:

$$a_n = -a_{n+1} \frac{i_{n+1}}{i_n} \tag{2.6}$$

Figure 2.2 shows the phase current (I_{ph}) of the outgoing phase and the incoming phases and the dc-link current (I_{dc}) during the commutation period. The discharging current of the outgoing phase is controlled by the duty cycle. The duty cycle of the incoming phase is around 0.2 and that of the outgoing phase is around -0.27. The de-fluxing process is retarded. At the beginning of the phase commutation, the duty cycle of the outgoing phase is less than 5%. The phase current is set to freewheel to prevent too fast de-fluxing. Hence, at the beginning of the commutation period, the outgoing phase current is not discharged until the incoming phase current is sufficient large so that the de-fluxing duty cycle is over 5%.

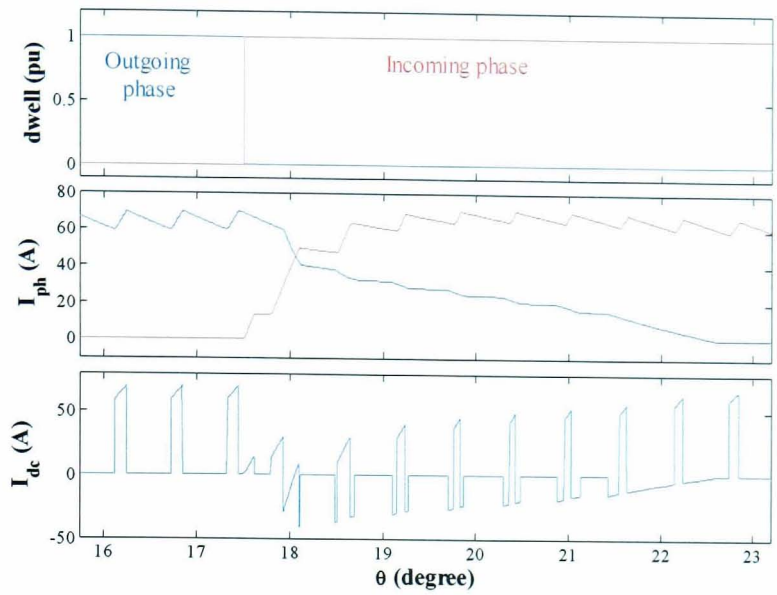


Figure 2.2: Phase current and dc-link current from PBC during commutation period $a_n \approx -0.27$ and $a_{n+1} \approx 0.2$

2.2.2 Voltage Hysteresis Control

The voltage of the dc-link capacitor during the commutation period is directly limited in [2.10]. This technique is called Voltage Hysteresis Control (VHC). As the dc-link capacitor voltage mainly fluctuates during the commutation period, the switching scheme during this period is controlled to reduce the voltage ripple. The benefit of VHC is not only that the H-bridge converter circuit is not altered, but it can be applied to the drive configuration that uses HCC. The voltage waveform and the switching state (*Sw state*) of VHC are illustrated in Figure 2.3.

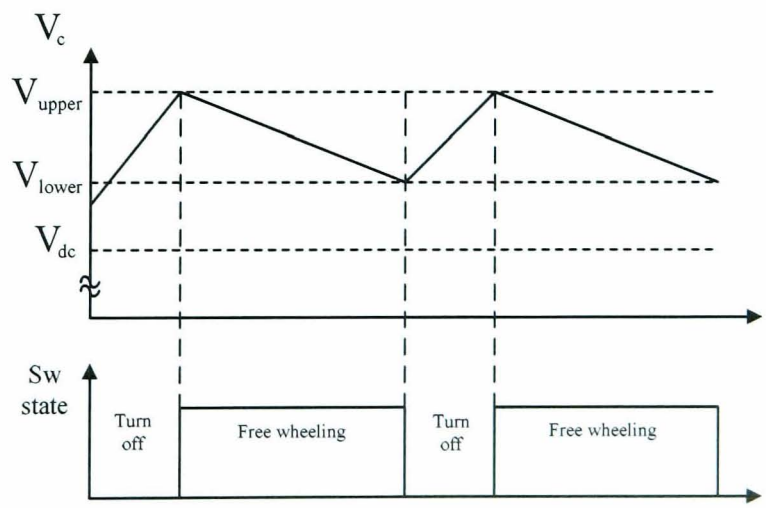


Figure 2.3: Capacitor voltage and switching states of VHC

In VHC, the capacitor voltage is controlled similarly to the phase current in HCC. The capacitor voltage is fed back to the controller and compared with the predefined upper limit and lower limit as follows:

$$V_{upper} = V_{dc} + \Delta V_{\max}$$
$$V_{lower} = V_{dc} + \Delta V_{\min} \tag{2.7}$$

where

V_{upper} is the upper limit of the capacitor voltage band.

V_{lower} is the lower limit of the capacitor voltage band.

ΔV_{max} is the voltage gap between the supply voltage and the upper limit.

ΔV_{min} is the voltage gap between the supply voltage and the lower limit.

Both voltages of the tolerance bands are higher than the nominal capacitor voltage. The control of the capacitor voltage is operated when the outgoing phase current is discharged and the capacitor voltage is higher than the defined limits.

Although the converter of both the techniques in [2.9-2.10] is not altered, the power supply circuit which is used in the techniques is a diode rectifier which is directly connected to the voltage source without any input filter. The characteristic of this power supply circuit is that the de-fluxing current cannot flow back to the supply. However, this causes the harmonic current in the supply. Both the control schemes yield satisfactory capacitor voltage results when the diode rectifier is connected directly to the dc-link capacitor, but if an inductive input filter is employed between the rectifier and the dc-link capacitor, the ripple of the capacitor voltage will be much large, as will be shown in Section 2.4.3.

2.3 Principle of Dc-Link Current Control

Figure 2.4 presents a power circuit of an SR machine drive. Ideally, the input current (I_{in}) is dc current, the current flowing through the dc-link capacitor (i_c) is ac current, and

the dc-link current (I_{dc}) is composed of the ac component and the dc component. The ac component in the dc-link current is filtered out by the dc-link capacitor (C).

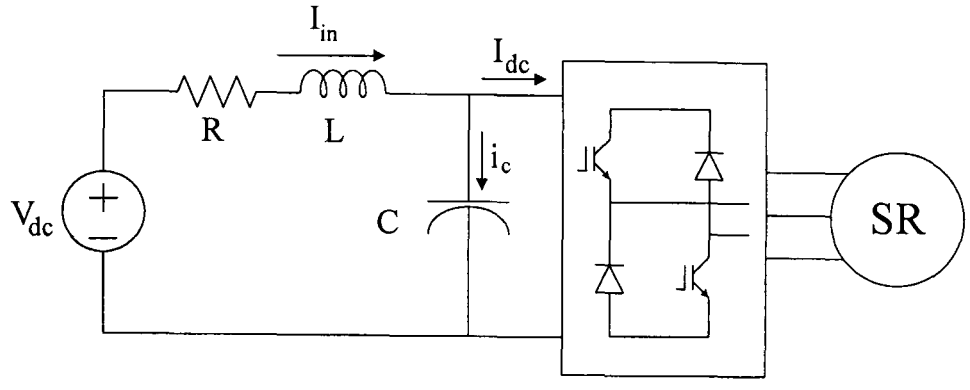


Figure 2.4: Power circuit of a switched reluctance machine

Generally, the ac component of the dc-link current comprises of 2 major harmonic frequencies: the commutation frequency and the switching frequency. The commutation frequency is relatively low and increases with the speed, as shown in (2.8). At low speeds, the commutation frequency is quite low.

$$f_{com} = \frac{rpm \times N_r \times N_{ph}}{60} \tag{2.8}$$

where

f_{com} is the commutation frequency.

rpm is the machine speed where the unit is rpm.

N_r is the number of the rotor poles.

N_{ph} is the number of the machine phase.

The switching frequency for PWM operation of the converter is much high. Since the dc-link capacitor provides a low impedance path for the high frequency component which can be easily filtered, the DLCIC technique aims to eliminate the low frequency component in the dc-link current. To achieve this, the average dc-link current in each switching period is maintained constant. Hence, only the dc component, which is the proportional to the power transfer from the dc supply to the SR machine, and the high frequency switching component, which can be easily attenuated by filtering, remain in the dc-link current.

Figure 2.5 shows the dc-link current pulses and the switching period (T_s). The average dc-link current of each switching period is the shaded area divided by the switching period, T_s. The dc-link current is integrated and divided by a constant switching period to find the average value. When the average dc-link current reaches the demanded value, the converter is turn-off in freewheeling mode. The dc-link current becomes zero during the rest of the switching period. So, the average dc-link current can be maintained constant during each switching period.

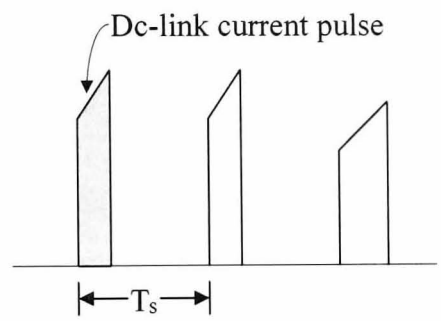


Figure 2.5: Dc-link current pulses

2.3.1 Switching Technique

Generally, at the beginning of each switching period, in Figure 2.6(a), both switches in the convert phase circuit ($S_{1,n}$ and $S_{2,n}$) are turned on. The current flows into the phase winding and this causes a positive dc-link current. The average dc-link current over the switching period T is given by

$$I_{dc,avg} = \frac{\int_0^{T_s} I_{dc}\,dt}{T_s} \tag{2.9}$$

where

$I_{dc,avg}$ is the average of the dc-link current.

I_{dc} is the dc-link current.

T_s is a constant switching period.

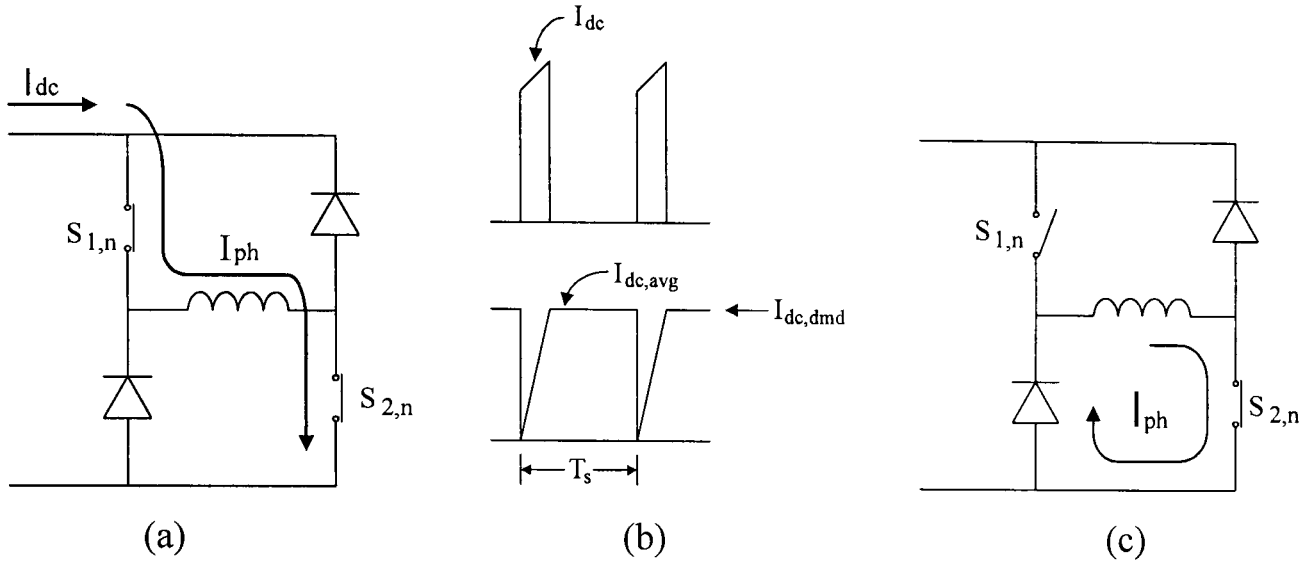


Figure 2.6: dc-link current, average dc-link current and circuit diagram

When the two active switches are turned on, the phase current (I_{ph}), the dc-link current (I_{dc}) increases and the average dc-link current ($I_{dc,avg}$) increase, as shown in Figure 2.6(b). When the average dc-link current or the integrator output reaches the dc current demand level ($I_{dc,dmd}$), the upper switch ($S_{1,n}$) is turned off. The phase current flows through $S_{2,n}$ and the freewheeling diode, as presented in Figure 2.6(c). The resulting dc-link current is zero. The average dc-link current is constant until the end of the switching period. At the end of the switching period, the integrator or the average dc-link current is reset to zero before a new switching period starts. This describes how the switches of the converter circuit are controlled when there is one phase current conducting at the time.

2.3.2 Commutation period

When the dwell period passes, the active phase is changed from an outgoing phase to an incoming phase. During the commutation period, the de-fluxing current is discharged from the outgoing phase, resulting in a negative dc-link current component. Meanwhile a positive dc-link current component flows into the incoming phase to establish the phase flux-linkage. This current is referred to as fluxing current.

Since the negative dc-link current can cause a high capacitor voltage fluctuation, at the beginning of the commutation period, the outgoing phase is not allowed to discharge the

de-fluxing current as HCC does in order to prevent the negative dc-link current. Instead, the outgoing phase current freewheels until the incoming phase current is sufficiently higher. When the incoming phase current is higher than the outgoing phase current, the de-fluxing current is discharged when the incoming phase is drawing a positive dc-link current, as shown in Figure 2.7. This prevents negative dc-link current. Furthermore, the switching events in every switching period are controlled from the output of the dc-link current integrator or according to the average dc-link current. In Figure 2.7, the dc current demand is 10A.

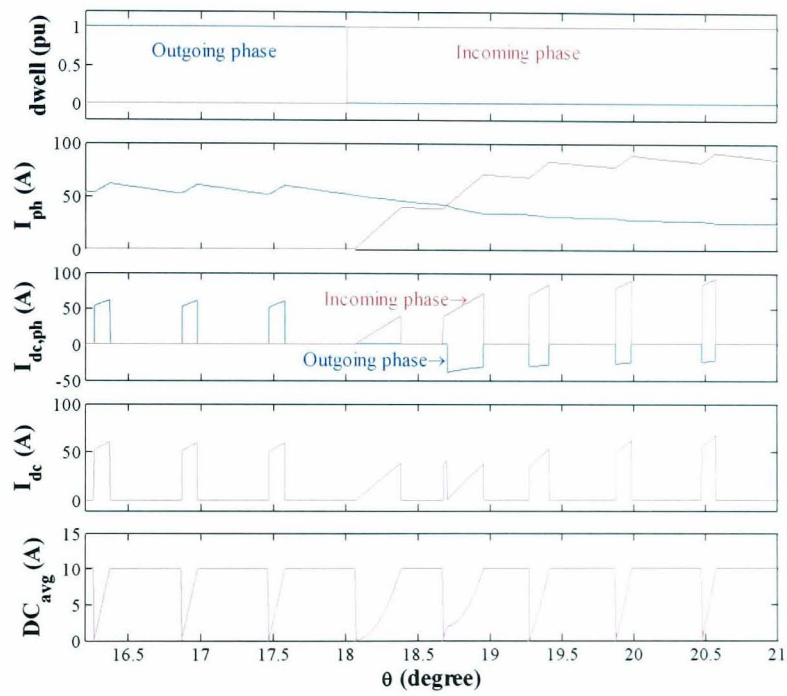
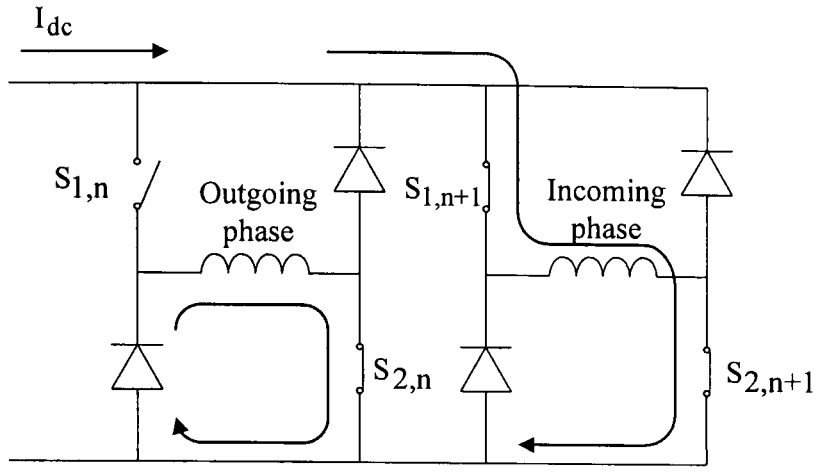


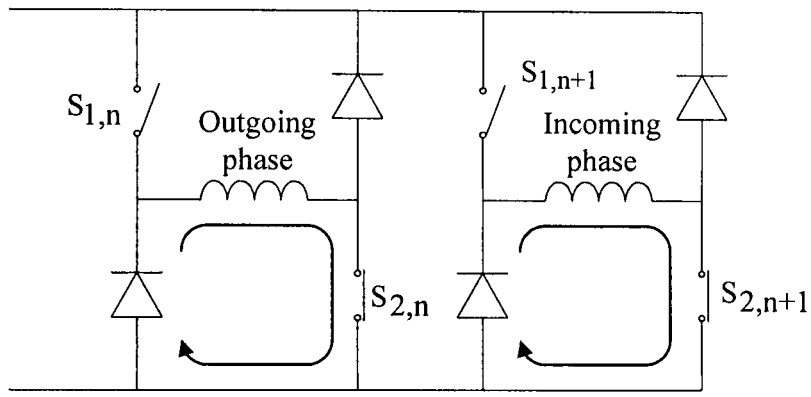
Figure 2.7: Dc-link current waveform during commutation period

Figure 2.8 shows the switching technique during the commutation period. In Figure 2.8(a), when the incoming phase current is lower than that in the outgoing phase, and only one switch in the outgoing phase circuit is turned on, the phase current free wheels. Both switches of the incoming phase circuit are turned on. The incoming phase current increases. The dc-link current, which is contributed by the incoming phase only, is integrated to obtain the average dc-link current. When the average dc-link current reaches the dc current demand, the incoming phase is turned into free-wheeling mode, as shown in Figure 2.8(b), and the resulting dc-link current becomes zero.

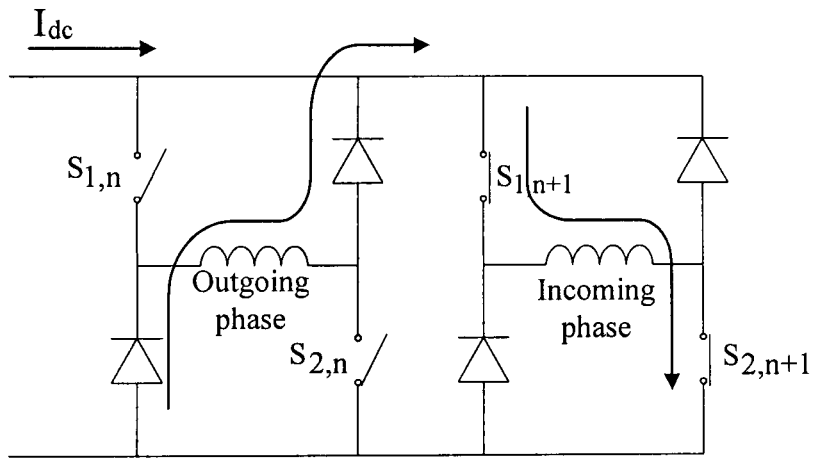
When the incoming phase current is greater than the outgoing phase current, the current in the outgoing phase is allowed to discharge when the incoming phase is charging. Both switches of the outgoing phase are turned off when both switches of the incoming phase are turned on, as shown in Figure 2.8(c). The de-fluxing current of the outgoing phase flows into the incoming phase winding. During this period, the dc-link current still flows into the converter. The amplitude of the incoming phase current is high because it receives the current from the dc link and the outgoing phase.



(a)



(b)

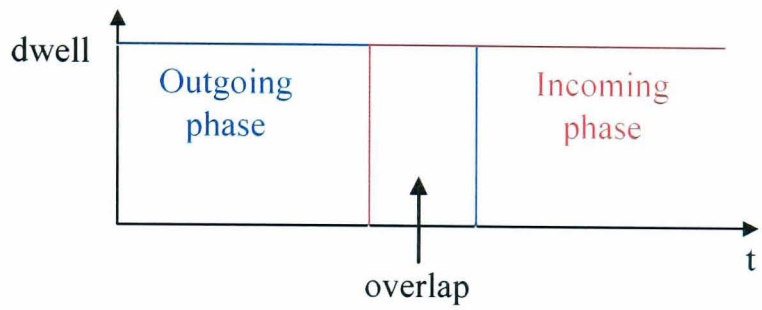


(c)

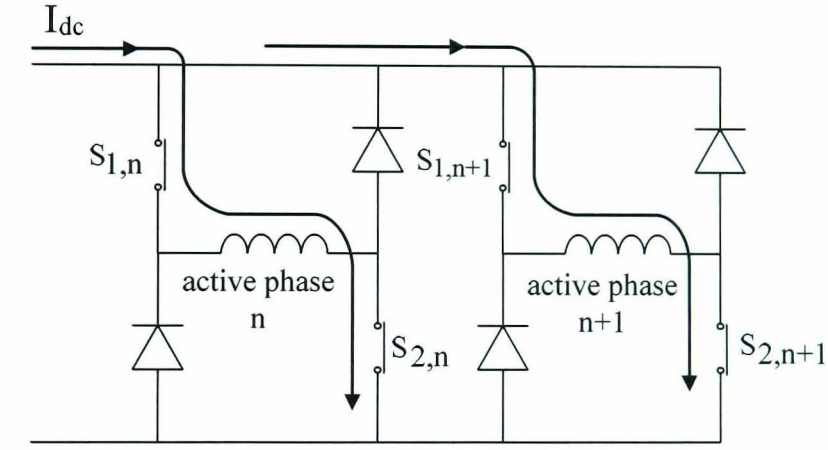
Figure 2.8: Converter circuit during commutation period

2.3.3 Overlapping period

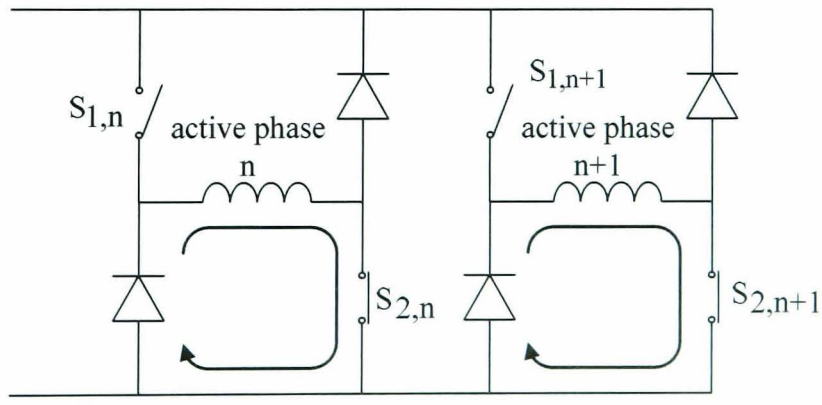
Since in the SR machine operation, the dwell period is not necessary to be equal to the stroke period, the dwell period may be longer than the stroke period when an overlap between the adjacent dwell signals occurs as shown in Figure 2.9(a). This sometimes improves efficiency and reduces the torque ripple of the SR machine. Figure 2.9 shows the current paths and switching states during the overlapping period.



(a)



(b)



(c)

Figure 2.9: Converter circuit diagram during overlap period

When the dwell periods overlap, there are 2 active phases to charge the fluxing current. Active phase n is active before the overlapping period and still active during the overlapping period. Active phase n+1 becomes active during the overlapping period. At the beginning of a switching period, both active phases are turned on, the dc-link current is distributed into 2 active phases, as shown in Figure 2.9(b). When the average dc-link current reaches the dc demand level, both phases are turned off in a soft switching mode shown in Figure 2.9(c).

2.4 Simulation Program

In the previous section, the principle of DLCIC has been explained. In this section, the principle is applied in simulation programs using Matlab/Simulink. The principle is simulated with a 3-phase 12-slot/8-pole SR machine. The electrical cycle is 45° mechanical degrees and the stroke angle is 15° mechanical degrees. At the beginning of a switching period, the switches in the converter circuit of the active phase are turned on. The dc-link current appears and the phase current flows in the phase winding. The dc-link current is integrated and the average of the dc-link current is obtained. When it reaches to the defined dc current demand level, a switch in the converter circuit is turned off in a soft switching mode.

From this description, two signals will be generated for the control. One is the turn-on signal which is used at the beginning of each switching period for turning on the switches in the converter circuit. The other is the turn-off signal. When the average dc-link current reaches the defined level, this signal is generated to turn off the converter in a switching period.

Figure 2.10 shows the simulation program of DLCIC. The magenta block (SR machine block) is the non-linear model of the SR machine. This block yields the phase current and torques. The input of this block is the terminal voltages of the phase windings and

the rotor position angle. The yellow block (dc-link current block) is the dc-link current block which determines the dc-link current, calculates the average dc-link current and generates the turn-off signal. The blue block is DLCIC block. The DLCIC principle is applied to generates the switching signals for the 3-phase converter circuit.

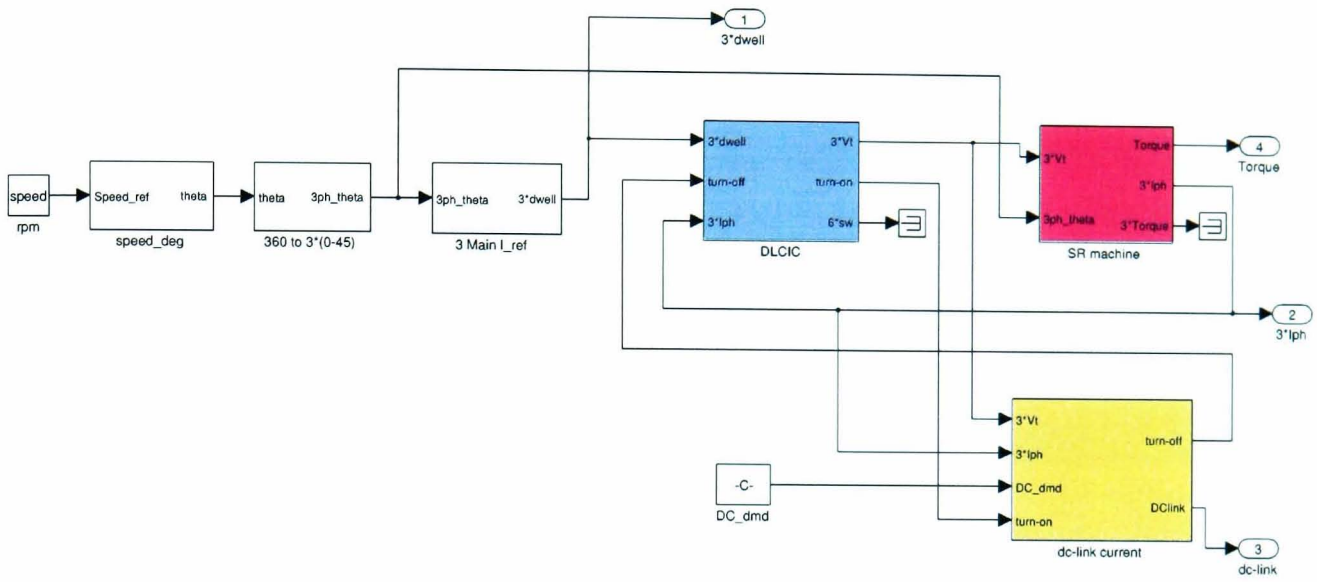


Figure 2.10: Simulation program of DLCIC

Other blocks are for obtaining the defined speed, position angles, and the defined dc current demand (DC_{dmd}) since in the operation, the speed and the dc current demand are assumed to be constant. In the DLCIC, the dc current demand is used as a torque demand. The dc current demand is a function of the phase current demand in HCC when the dwell period is equal to the stroke period. On the other hand, when the dwell period is extended, the dc current demand is dependant on the phase current demand and the machine speed.

In this simulation, it is assumed that the mechanical load can be modelled as a simple speed-stiff constant speed load. Hence the mechanical output power can be controlled by a fix set point, current demand (DC_{dmd}) in the model. In principle, it would be possible to add mechanical model to present a speed controller in the place of DC_{dmd}.

From Figure 2.10, the speed is integrated to obtain rotor mechanical position, which is used to determine the phase dwell signals. When a phase dwell signals is equal to 1, it is the active. The phase current flows to the winding. If the dwell signal is equal to 0, the phase is deactivated. In this section, three blocks in Figure 2.10 are described in detail, the SR machine block, the dc-link current block and the DLCIC block.

2.4.1 SR Machine Block

The switched reluctance model in the simulation program is a non-linear model. The torque and the current calculation of each phase are separated according to rotor position angle with respect to phase. The phase current of the SR machine in the simulation is calculated from (2.10).

$$V_t = Ri_{ph} + \frac{d\psi(i_{ph},\theta)}{dt} \tag{2.10}$$

where

V_t is the terminal voltage of the phase winding.

R is the resistance in the phase winding.

i_{ph} is the phase current.

ψ is the flux linkage of that phase.

θ is the rotor position angle with respect to that phase.

t is time.

The flux is obtained by

$$\psi(i_{ph},\theta) = \int_0^t (V_t - Ri_{ph})dt \tag{2.11}$$

The equation in (2.11) is implemented in the Simulink model, as shown in Figure 2.11. The figure presents one phase of the SR model program. The output of the integrator provides the flux linkage. Then, the flux-linkage is converted to flux per turn before being fed to the green lookup table with the position angle of that phase. The green lookup table outputs magnetomotive force (*mmf*) and the phase current is obtained from mmf, as

$$i_{ph} = {mmf}/{TURNS} \tag{2.12}$$

where

TURNS is the number of turns of the phase winding.

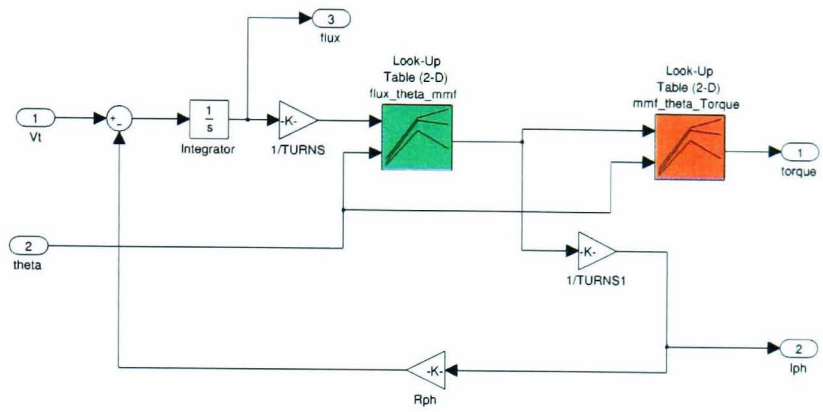


Figure 2.11: One phase of switched reluctance machine model

The phase torque is obtained from the orange lookup table in Figure 2.11 by submitting the magnetomotive force (mmf) and position angle. The machine torque is calculated from the summation of all the phase torques.

2.4.2 Dc-link Current Block

Figure 2.12 shows the dc-link current block. The dc-link current in the dc-link block is obtained from the phase current and the terminal voltage. Then, it is integrated and divided by the switching period (delta_T) for the average dc-link current. The average dc-link current is compared with the dc current demand (*DC_dmd*) and fed through the relay block to generate the turn-off signal. When the signal is equal to 1, the switch in the active phase is turned off. The turn-off signal is fed to the DLCIC block in Figure 2.10 to produce the switching signals for the active phase.

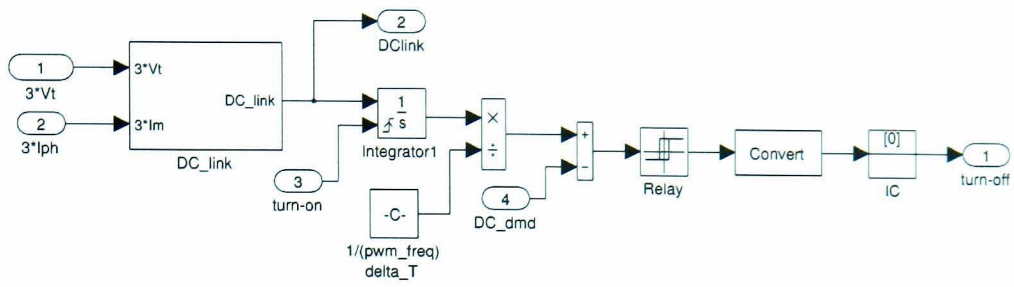


Figure 2.12: Turn-off signal production program

2.4.3 Dc-Link Integration Current Control Block

The objective of the DLCIC block in Figure 2.10 is to generate the switching signal for the converter of the 3-phase SR machine. Figure 2.13 represents the schemetic of the DLCIC block. Three large blocks in the middle of the figure, which are labelled 'Switching signal Ph1', 'Switching signal Ph2', and 'Switching signal Ph3', generate the switching signals for the three-phase converter.

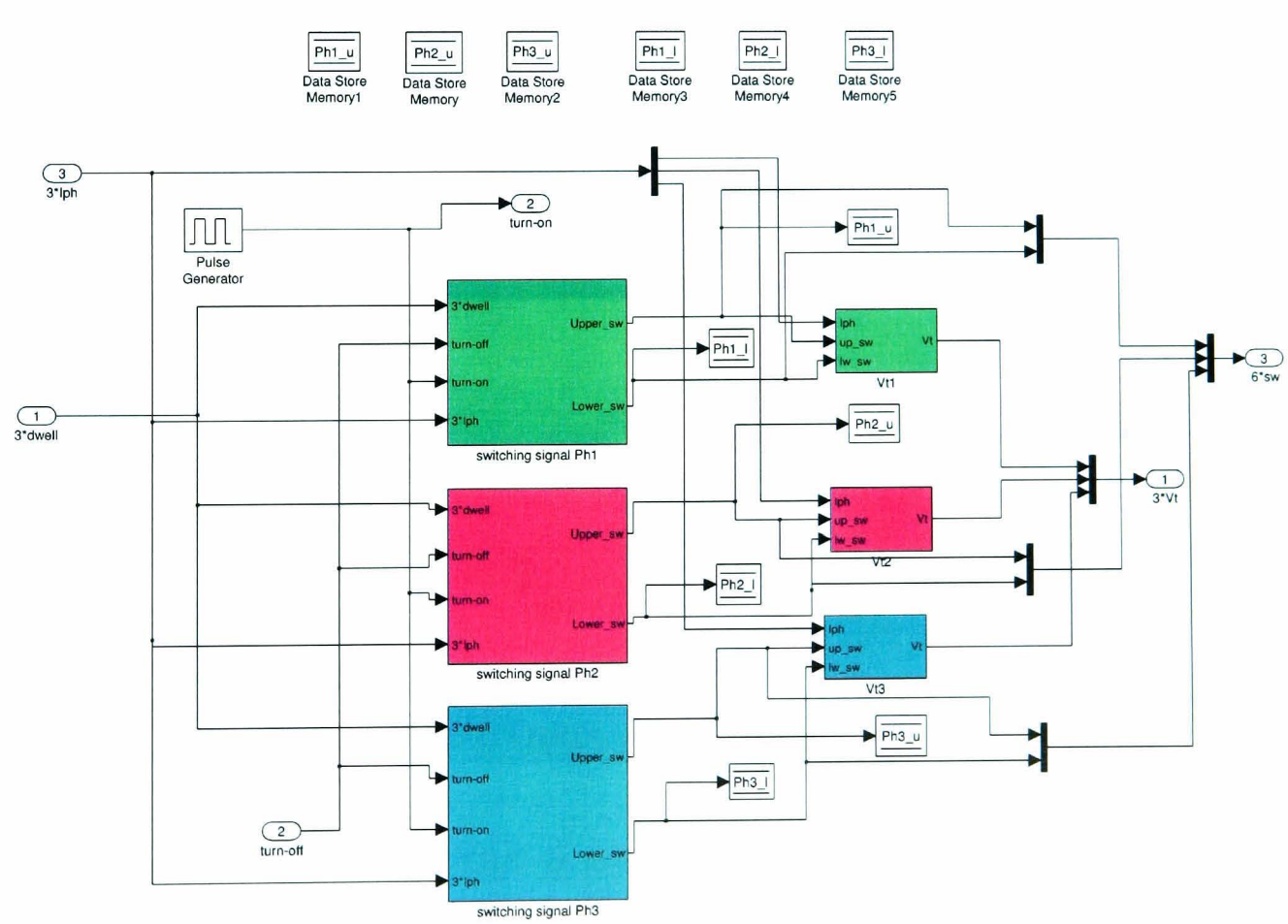


Figure 2.13: DLCIC block

The colours of the blocks are used for indentifying each phase, green, magenta, and light blue for phase1, phase2 and phase3, respectively. Since the switching signals cannot be applied directly to the SR machine block in Figure 2.10, the switching signals of each phase are converted to the terminal voltage. The small blocks on the right hand side which are labelled 'Vt1', 'Vt2', and 'Vt3' converts the switching signals to the terminal voltages for phase1, phase2 and phase3. The Pulse Generator block generates the Pulse Width Modulation (PWM) signal which is used as the turn-on signal in the switching signal blocks and a reset signal in Dc-link current block in Figure 2.12. For the switching signal blocks, there are two further subsystems per phase, which generate the upper switching signal and lower switching signal.

Upper Switching Signal Subsystem

Figure 2.14 shows the block diagram which is used to generate the upper switching signal. The process begins at the blue block which is the triggered subsystem. When the rising edge occurs at the trigger input, the data at In1 input will be delivered to Out1 output.

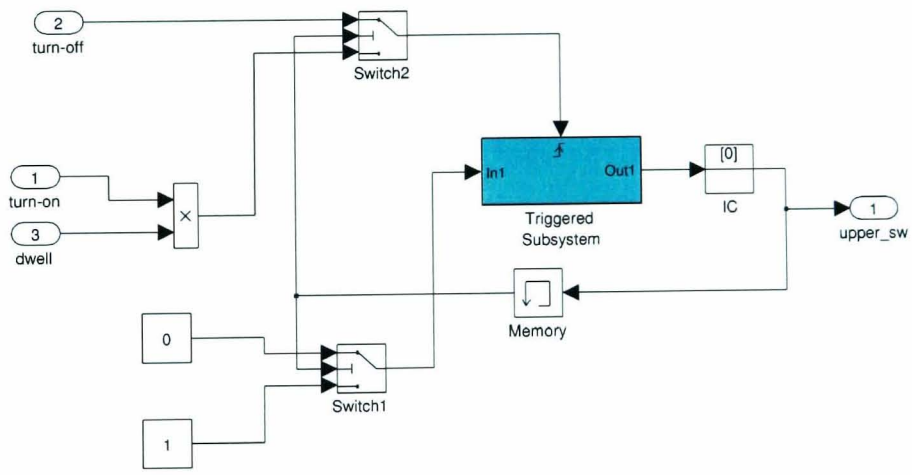


Figure 2.14: Upper switching signal generator

At the beginning, the data at Out1 is set to be 0 (zero) by the initial condition block (*IC*). The upper switching signal (*upper_sw*) is zero. Hence, the control inputs of Switch1 and Switch2 are equal to zero. Switch1 and Switch2 blocks are set that if the

control input is '0', the third input at the switch block is selected to the output, and if the control input is '1', the first input is selected to the output. Thus, the output of Switch1 is equal to '1' since the control input is '0'. In1 input is also one. Similarly, the output of Switch2 is from the AND of the turn-on signal and the phase dwell signal. If that phase is active or within the dwell period, the dwell signal is equal to one, otherwise the dwell signal is equal to zero. When the dwell signal is '1', the output of switch2 is the turn-on signal.

When the rising edge of the turn-on pulse enters the trigger input at the triggered subsystem, the data of In1 input, which is 1, is passed to the Out1 output. The upper switching signal (*upper_sw*) is changed from zero to one. The control inputs of Switch1 and Switch2 now become '1'. The output of Switch1 is changed to '0' and the output of Switch2 is connected to the turn-off signal. So, the trigger input of the Triggered Subsystem will wait for the rising edge of the turn-off signal.

Meanwhile, since the switches of the converter are turned on, the average dc-link current will rise and when it reaches to the dc current demand, the logic state of the turn-off signal changes from '0' to '1'. When the rising edge of the turn-off pulse occurs at the trigger input, zero at the input In1 is passed to the output Out1. Consequently, the upper switching signal (*upper_sw*) is changed to zero again. This will turn the upper switch of the active phase off. The control inputs of Switch1 and Switch2 are turned to zero again. The output of Switch1 is '1'. So is the In1 input. The output of Switch2 is reconnected to the turn-on pulse and the Triggered Subsystem will wait for the rising edge from the new turn-on pulse for the next switching period.

The upper switching signal is periodically altered between zero and one until the dwell signal is equal to zero. The active phase is changed to inactive. There is no turn-on signal going to the trigger input of the Triggered Subsystem. If the upper switching signal is still equal to one, the Triggered Subsystem is waiting for a turn-off pulse. When the turn-off pulse arrives and the upper switching signal is changed to zero, and it

will not become one again until both the dwell signal and turn-on signal are equal to one.

Lower Switching Signal Subsystem

From the description of the upper switching signal subsystem, the phase current is controlled by the upper switch during the dwell period, meanwhile the lower switch is kept on for the duration of the dwell period. When the rotor position is outside the phase dwell period, the upper switch is turned off and the de-fluxing current is controlled by the lower switch. Figure 2.15 illustrates the flowchart diagram of the lower switching signal generator of phase1. For the sake of simplicity, only the principle of the lower switching signal generation is explained.

To reduce the ripple of the dc-link capacitor voltage, the negative dc-link current is prevented since it causes significant capacitor voltage fluctuates. The lower switch is controlled to allow the de-fluxing current being fed back to the dc-link when the current in the incoming phase is greater than that in the outgoing phase and when the upper switch of the incoming phase is on. Consequently, when the incoming phase draws a current greater than in the incoming phase, the lower switch is turned off, allowing the de-fluxing current being fed back to the dc-link via the freewheeling diodes. The de-fluxing current is fed to the incoming phase. Otherwise, the switch is turned on and the de-fluxing current is dissipated via the phase winding.

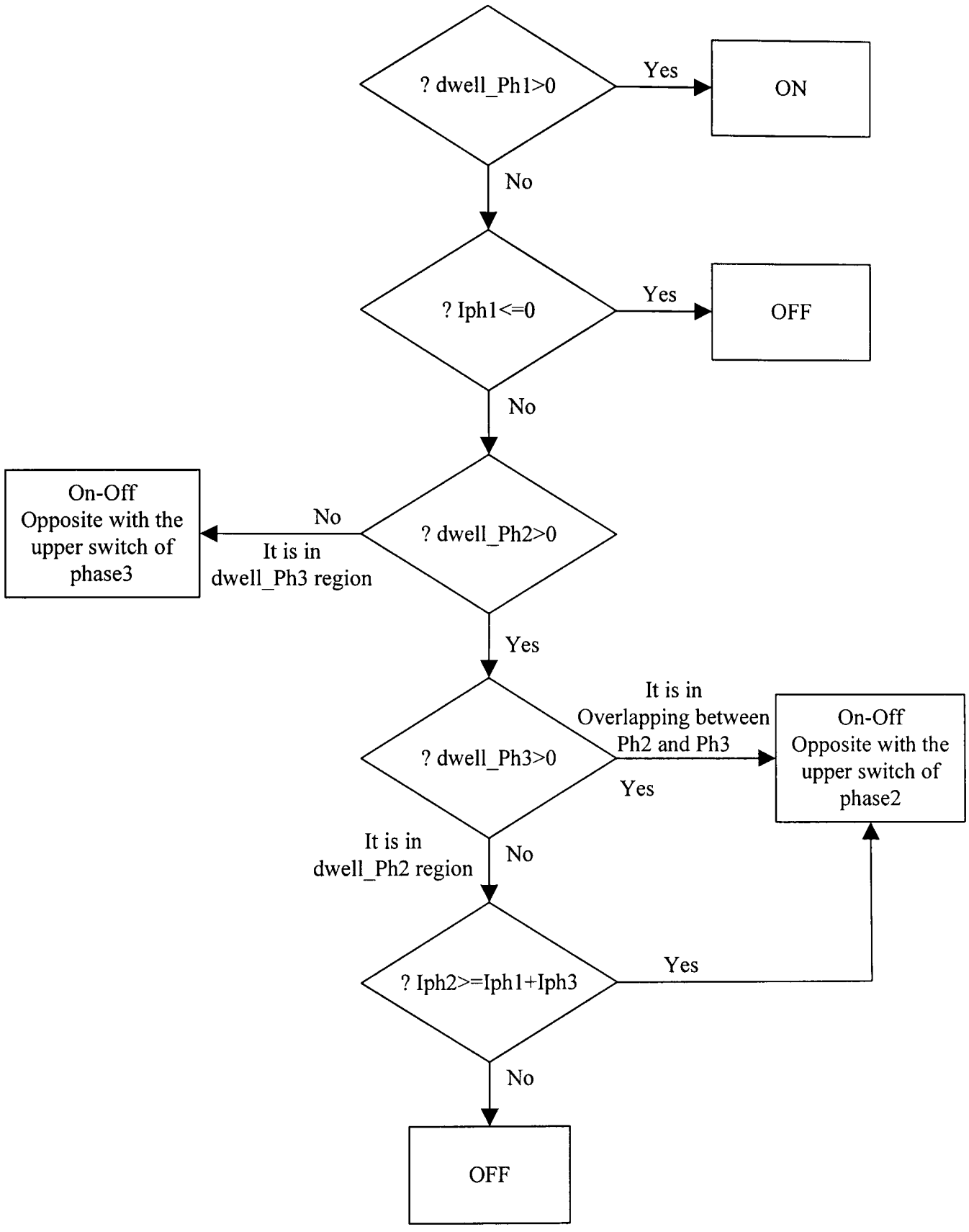


Figure 2.15: Flowchart of lower switching signal generator of phase1

2.4.4 Capacitor Voltage Calculation

The dc-link capacitor voltage is determined from the dc-link current output of the dc-link current block in Figure 2.10. Two power circuits have been simulated. One is the circuit in Figure 2.16 which represents the dc bus bar voltage rail with an input filter which is employed to attenuate the harmonic current from the converter. The other circuit is shown in Figure 2.17. It is a simplified circuit representing a dc supply derived from an AC to DC diode rectifier.

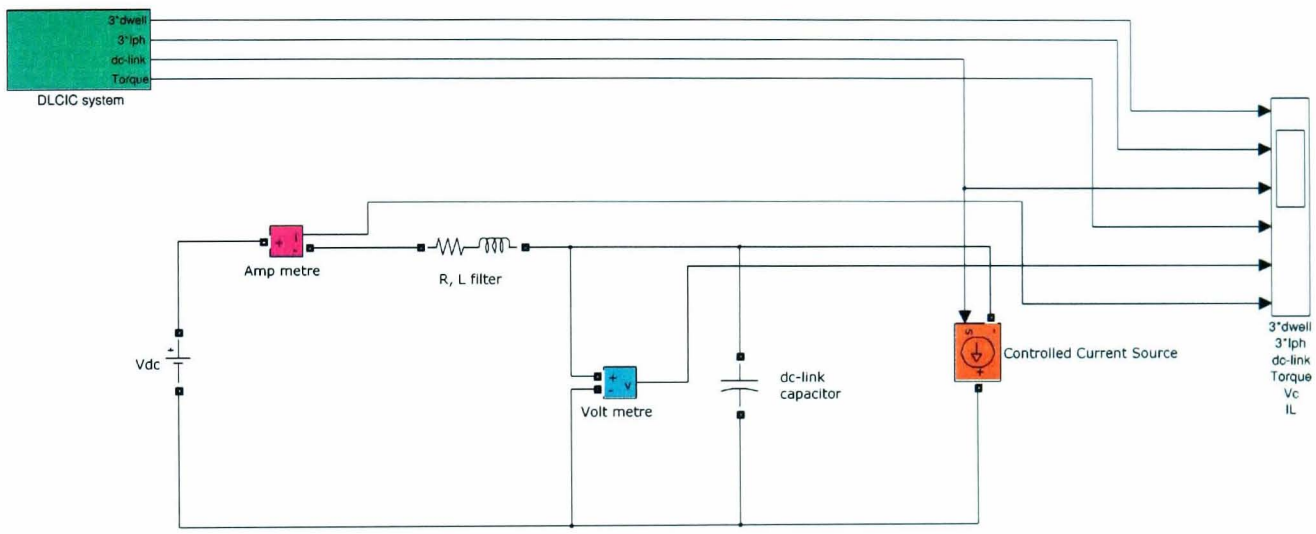


Figure 2.16: Bus bar power circuit calculating capacitor voltage

In Figure 2.16 and Figure 2.17, the dc-link current is fed to the controlled current source, the orange block which is parallel connected across the dc-link capacitor. The capacitor is connect to the dc supply voltage, 270V, through the R,L filter which represents the combined effect of the cable and the input filter [2.11 - 2.13].

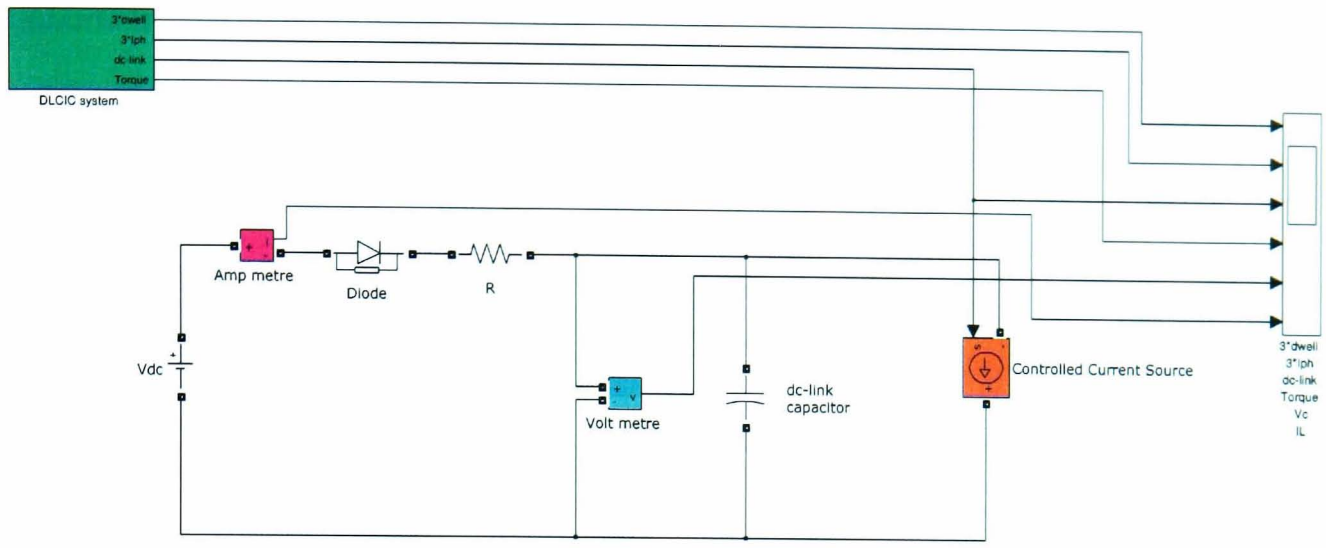


Figure 2.17: Diode rectifier power circuit program

2.5 Result Comparison

In this section, the simulation results of Dc-link Current Integration Control (DLCIC) are compared with those of other techniques under the same conditions such as the dc-link capacitance, the demand torque, the turn-on and turn-off angles. The simulated results which are shown in this section are the dwell signals, the phase currents, the dc-link current, the capacitor voltage, the input current and the machine torque. The key indicator is the dc-link capacitor voltage ripple since the objective of this project is to reduce the dc-link capacitance while keeping the voltage ripple below a given limit. If the ripple of the dc-link capacitor voltage from a given technique is less than that from other techniques, it is assumed that technique has more potential in reducing the dc-link capacitance than the other techniques.

2.5.1 Compared Techniques

Five techniques are compared with the DLCIC in the simulation study. The first is Hysteresis Current Control (HCC) since it is a conventional control for an SR machine. The second is PWM Current Control (PWMCC) which uses the phase current feedback to control phase voltage via PWM modulation. The third and forth techniques are those reported by Neuhause, et al., as described in Section 2.2. For the Power Balancing

Control (PBC) in [2.9], the output power of the outgoing phase is controlled to be equal to the input power of the incoming phase during the commutation period. The other technique from [2.10] is Hysteresis Voltage Control (HVC). For this technique, the feedback of the dc-link capacitor voltage is directly controlled during the commutation period. During the dwell period, it operates as HCC. The fifth technique is Unipolar Hysteresis Control (UHC). This technique is similar to HCC except during the commutation period, in which all the outgoing phase current is fed to the incoming phase and there is no negative dc-link current. Most of these are previously explained in detail except for the PWMCC and the UHC.

PWM Current Control (PWMCC)

This is a close-loop current control. The duty cycle of the voltage PWM depends on the phase current and demand torque. Figure 2.18 represents the block diagram of the PWMCC. In the current loop, the phase currents are compared with the demands and the error are fed to the PI control block to generate the duty cycle and to control the current and torque.

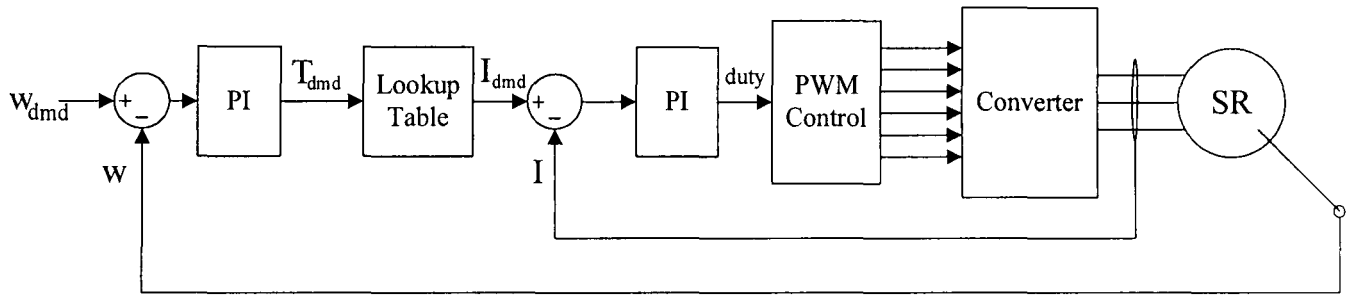


Figure 2.18: Block diagram of PWMCC

Unipolar Hysteresis Control (UHC)

Since in the HCC the de-fluxing current from the outgoing phase is fed back to the dc-link capacitor and the dc supply, resulting in a large voltage fluctuation in the dc-link capacitor. This method is aimed to eliminate this problem. All of the de-fluxing current is managed to supply to the incoming phase. There is no return of the de-fluxing current or the negative dc-link current to the dc supply.

Figure 2.19 shows the phase current and the dc-link current of the UHC. The SR machine is operated by the HCC during the dwell period. The dc-link current during this period is positive since the converter draws current is from the dc-link. During the commutation period, the de-fluxing current is circulated in the outgoing phase winding until the current of the incoming phase is greater than the de-fluxing current. Then, both the active switches in the outgoing phase converter are turn-off and the de-fluxing current is allowed to feed into the incoming phase when it is charging. The dc-link current during the commutation period remains positive. There is only positive dc-link current in this technique. Thus, it is called Unipolar Hysteresis Control (UHC).

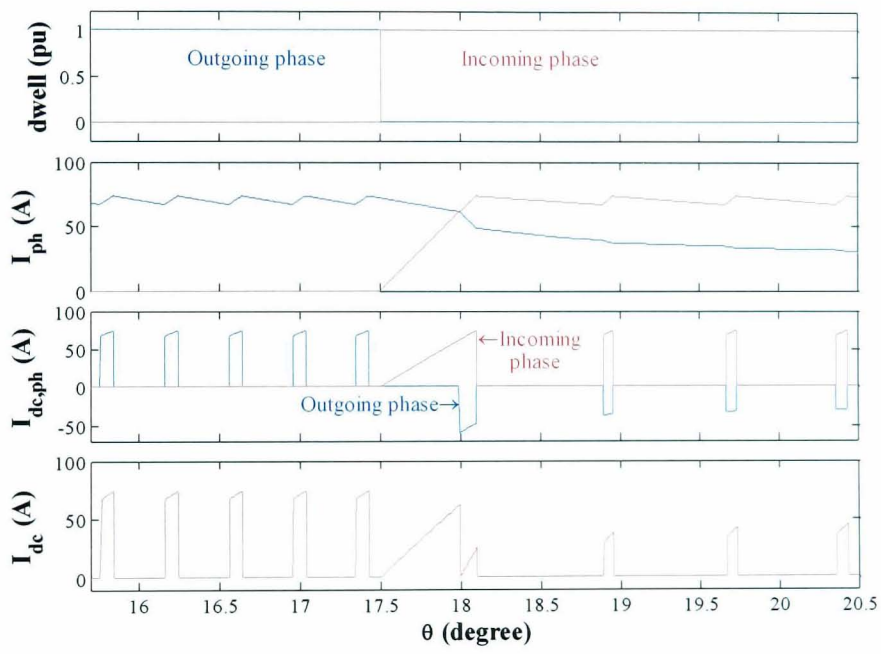


Figure 2.19: Phase current and dc-link current of UHC

2.5.2 Power Supply Circuits

Not only six techniques are compared, the simulation results also provides for the capacitor voltage and the input current of two power supply circuits commonly used in industries. The diode rectifier voltage supply converts the electricity from AC to DC. It is also used in [2.9-2.10]. To eliminate the voltage ripple due to the rectifier effect, the circuit is simplified as shown in Figure 2.20. The other type of the dc supply is the voltage source from dc bus bars. In Figure 2.21, the dc bus bar circuit is composed of

an inductor and an resistor which include the effect of the parasitic and input filter [2.14 - 2.16].

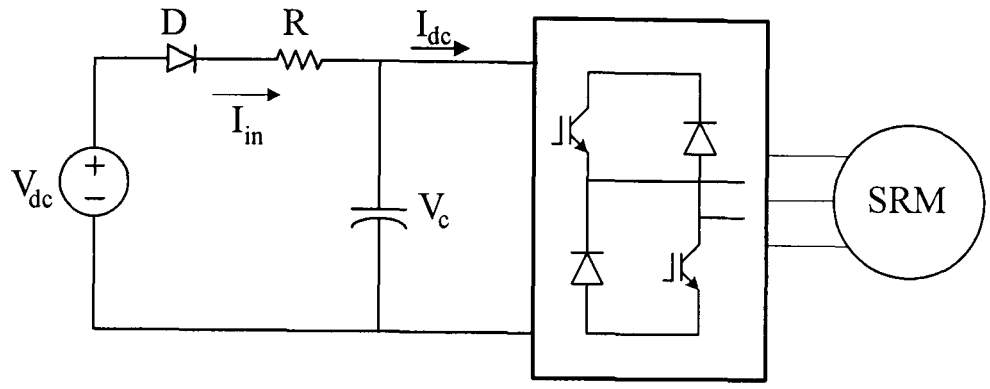


Figure 2.20: Diode rectifier supply circuit

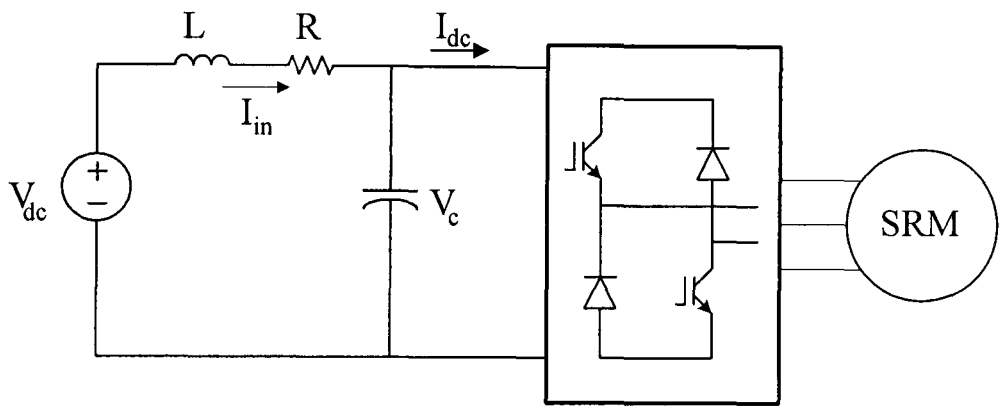


Figure 2.21: Dc bus bar supply circuit

2.5.3 Simulation Results

All the simulation results in this section are obtained from MATLAB/Simulink under an operation speed of 1000 rpm. The details of the SR machine and the filter parameters are provided in Table 2.1. Figure 2.22 represents the flux linkage and current characteristic curve of the SR machine. The supply voltage for the simulation is 270V. Within the techniques compared by simulations, some have a variable switching frequency such as HCC and the others have constant switching frequency such as PWMCC. The results from variable switching frequency techniques are first shown and they are followed by those from the constant switching frequency techniques for the comparison purpose. The switching frequency in the constant switching frequency techniques is set to 10 kHz. Each simulation employs a turn-on angle at 2.5° and a turn-

off angle at 17.5°. From this, the dwell period is equal to the stroke period, where there is no overlap between the dwell period.

Table 2.1: Details of SR machine and filters

SR machine		Filter	
Number of Phase	3	Resistance (Ω)	0.1
Number of Stator poles	12	Inductance (mH)	0.46
Number of Rotor poles	8	Capacitance (μF)	1000
Rated torque (Nm)	20		
Rated power at 30000 rpm (kW)	13.5		

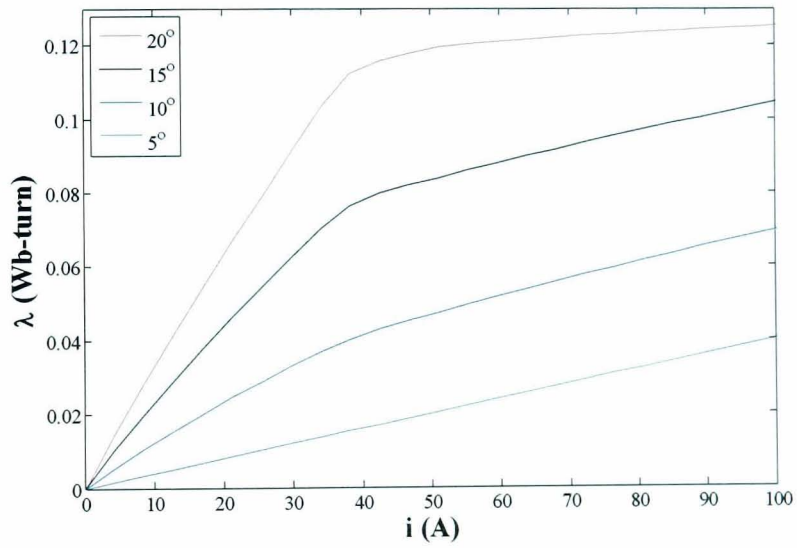
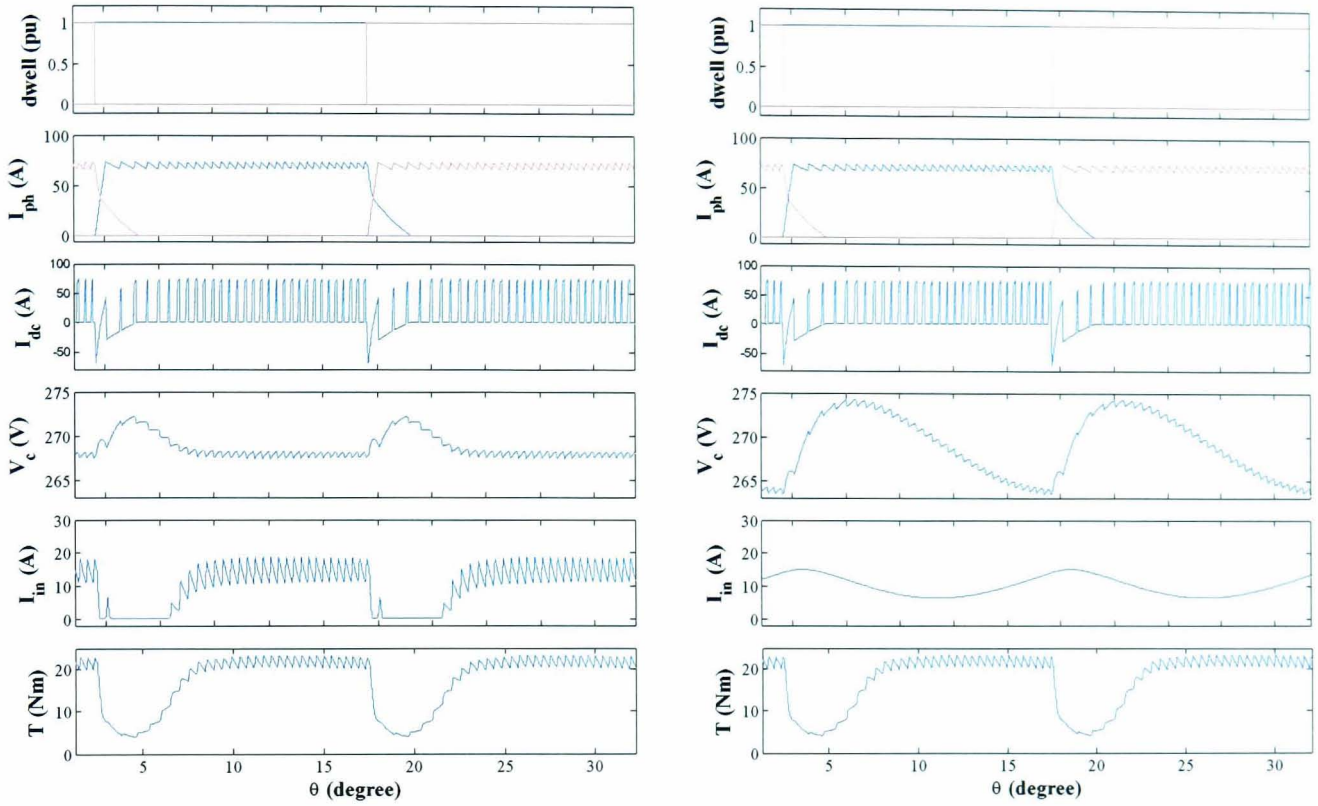


Figure 2.22: Flux linkage and current characteristic curve

Hysteresis Current Control

Figure 2.23 shows the simulation results from the HCC. The phase current is controlled and maintained constant during the dwell period. However, HCC does not fix the frequency. The band of the hysteresis current is fixed at ±3.5A which is resulted in a typical switching frequency at 12.4kHz at the rated torque, 20Nm. When the dwell period is ended, both the active switches of the outgoing phase are turned-off, and the phase current is discharged back to the dc-link, causing negative dc-link current. Figure

2.23(a) is the results from the diode rectifier power circuit and Figure 2.23(b) is the results from the dc bus bar power circuit.



(a) diode rectifier (b) dc bus bar

Figure 2.23: Simulation results from HCC (30° corresponds to 5 ms)

Although the phase currents (I_{ph}), the dc-link current (I_{dc}), and the machine torque (T) with the two different power supplies are similar, the capacitor voltage (V_C) and the input current (I_{in}) are different. For the diode rectifier circuit, when the negative dc-link current occurs, the capacitor voltage overshoots, but no energy can be transferred back to the dc supply. Consequently, the current I_{in} drawn from the supply is zero. When the negative dc-link current ends, the capacitor voltage gradually reduces and finally becomes constant again.

For the dc bus bar circuit, the negative dc-link current also causes significant overshoot voltage across at the dc-link capacitor. A part of the energy is transferred back to the supply as evident by the decrease in the supply current I_{in}. When the negative dc-link current diminishes, the capacitor voltage decreases until the negative dc-link current takes place again. The voltage ripple of the dc bus bar circuit is higher than that of the

diode rectifier circuit due to the presence of the inductive filter. As the current in the supply fluctuates the energy stored in the inductor increases or decreases. A part of this energy variation will be transferred to the capacitor, resulting extra voltage fluctuation. On the other hand, the input current ripple of the diode rectifier circuit is higher than that of the dc bus bar circuit.

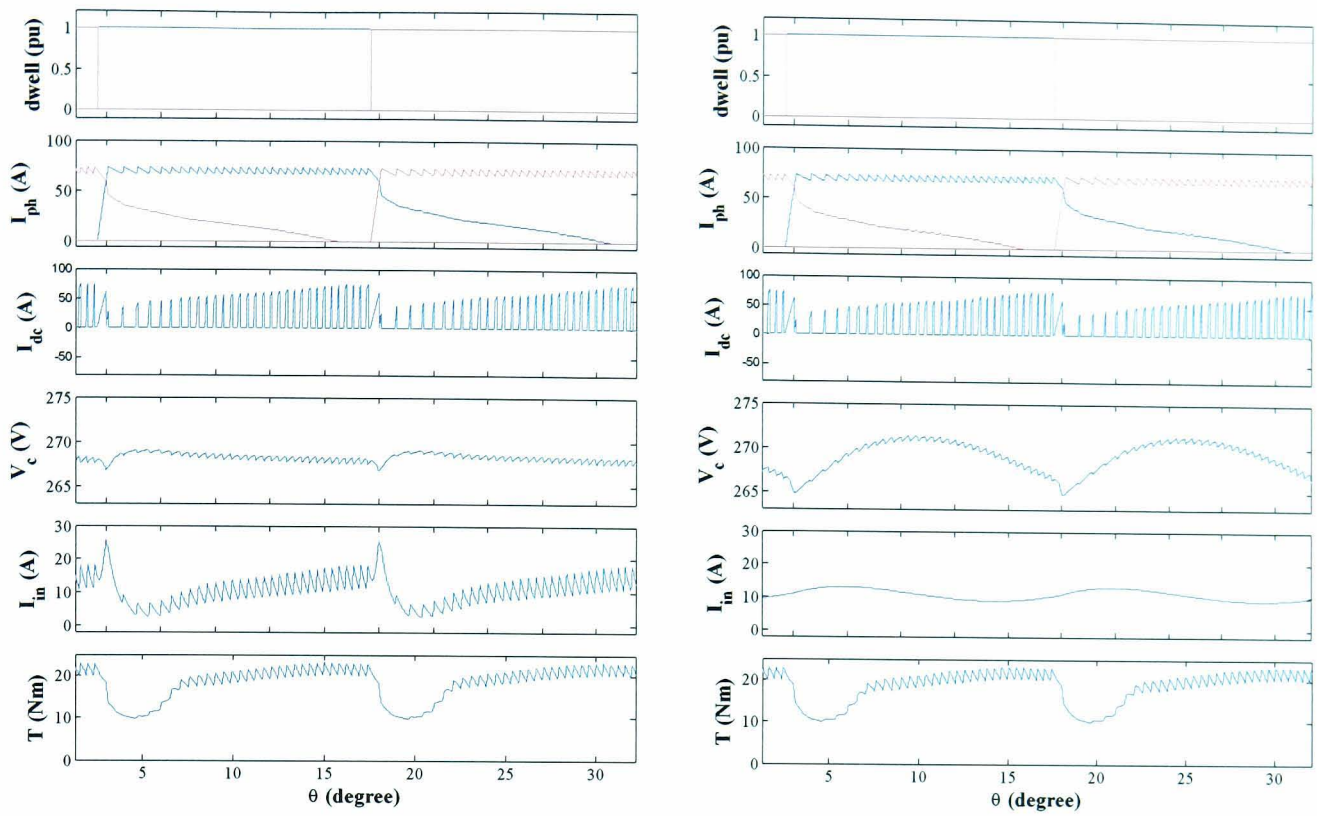
In Figure 2.23(a), due to the effect of the diode in the power circuit, the input current (I_{in}) is zero during the overshoot period of the capacitor voltage. The current fluctuation can cause the AC harmonic in the grid. In Figure 2.23(b), although the input current of the dc bus bar circuit oscillates, the variation is much smaller.

For the purpose of comparison in the remaining section, the HCC reference is regards as the 100% baseline against which other methods are compared.

Unipolar Hysteresis Control (UHC)

Since the control scheme of the UHC is similar to the HCC, no additional feed-back input signal is required. In the dwell period, the SR machine is operated under the HCC. During the commutation period, the outgoing phase current is allowed to flow back to the dc-link only when the incoming phase draws a greater current. This results in only positive dc-link current, or uni-polar dc-link current, as shown in Figure 2.24.

Figure 2.24(a) presents the UHC simulation results from the diode rectifier power circuit and the results from the dc bus bar power circuit are shown in Figure 2.24(b). Since there is no negative dc-link current, the ripples of the dc-link capacitor voltage is reduced to 50% of the HCC, baseline. The capacitor voltage ripple in the diode rectifier circuit is 48% of the HCC and the capacitor voltage ripple in the dc bus bar circuit is at 60% of that from HCC. The capacitor voltage ripple of the UHC is caused by current fluctuation since the motor draws a larger current at the beginning of the dwell period [2.17]. This shows that the dc-link capacitor voltage fluctuations are not entirely due to the occurrence of the negative dc-link current.



a) diode rectifier (b) dc bus bar

Figure 2.24: Simulation results from UHC (30° corresponds to 5 ms)

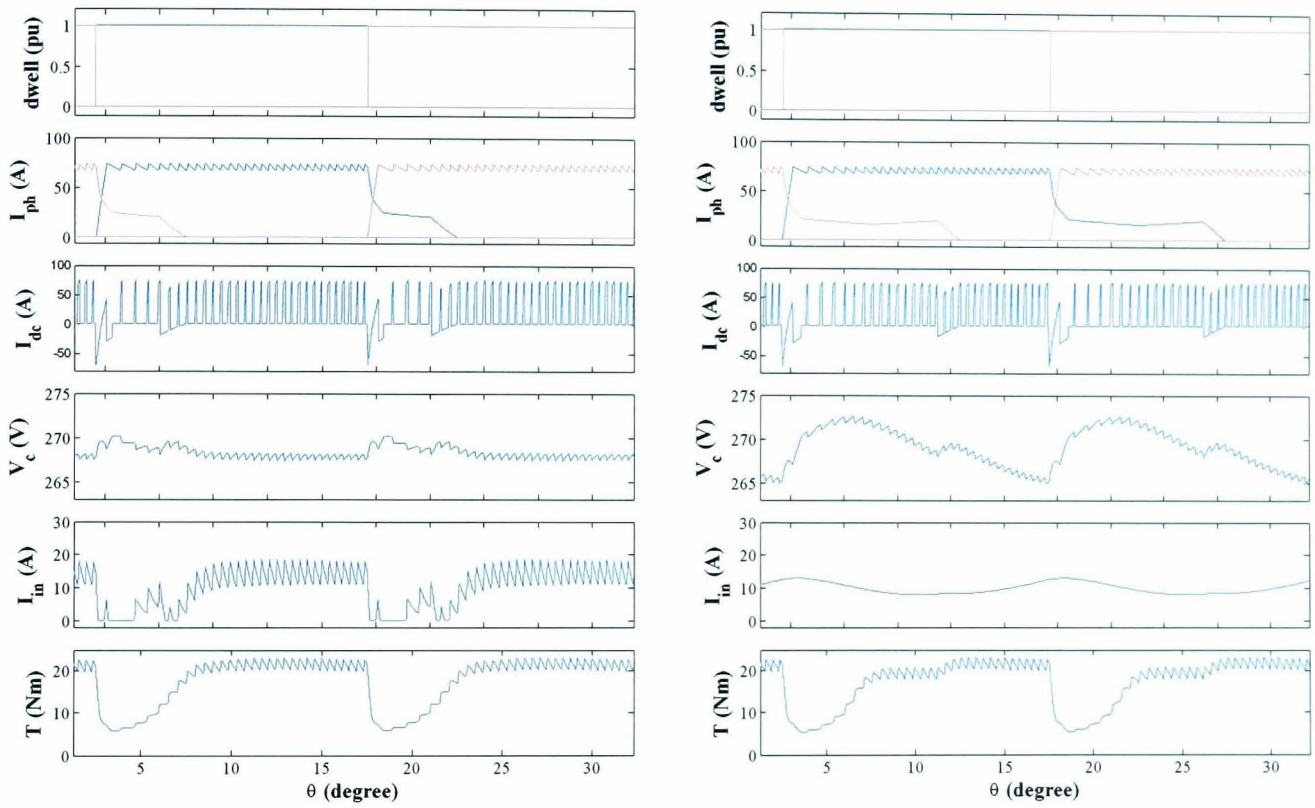
The benefit from this technique is not only in the capacitor voltage (V_C), but also in the input current (I_{in}). The input current in the diode rectifier circuit does not reach zero though there is a current surge at the beginning of the dwell period due to rapid increase in the phase current. In the HCC, there is no surge because the de-fluxing current is fed to the dc-link at the same time when the phase current increases. The input current in Figure 2.24(b) does not vary significantly because the inductive filter smoothes the current. Moreover, the input current in the bus bar circuit has a lower current ripple than that from the HCC in Figure 2.24(b) since there is no negative dc-link current.

For the machine torque (T) waveforms, it can be seen that the torque ripple from the UHC in Figure 2.24 is lower than that from the HCC in Figure 2.24 since after the dwell period, the outgoing phase current does not decrease to zero quickly. Consequently, it can produce some torque before the incoming phase can yield the demand torque. However, the machine torque at the beginning of the dwell period is lower than that at

the end of the dwell period since the long current tail of the outgoing phase produces negative torque.

Voltage Hysteresis Control (VHC)

The control scheme of the VHC is different from the HCC only during the commutation period. In that period, the capacitor voltage is measured and controlled within a hysteresis band. Figure 2.25 shows the simulation results of the VHC with a voltage hysteresis band of ±2 V.



a) diode rectifier (b) dc bus bar

Figure 2.25: Simulation results from VHC (30° corresponds to 5 ms)

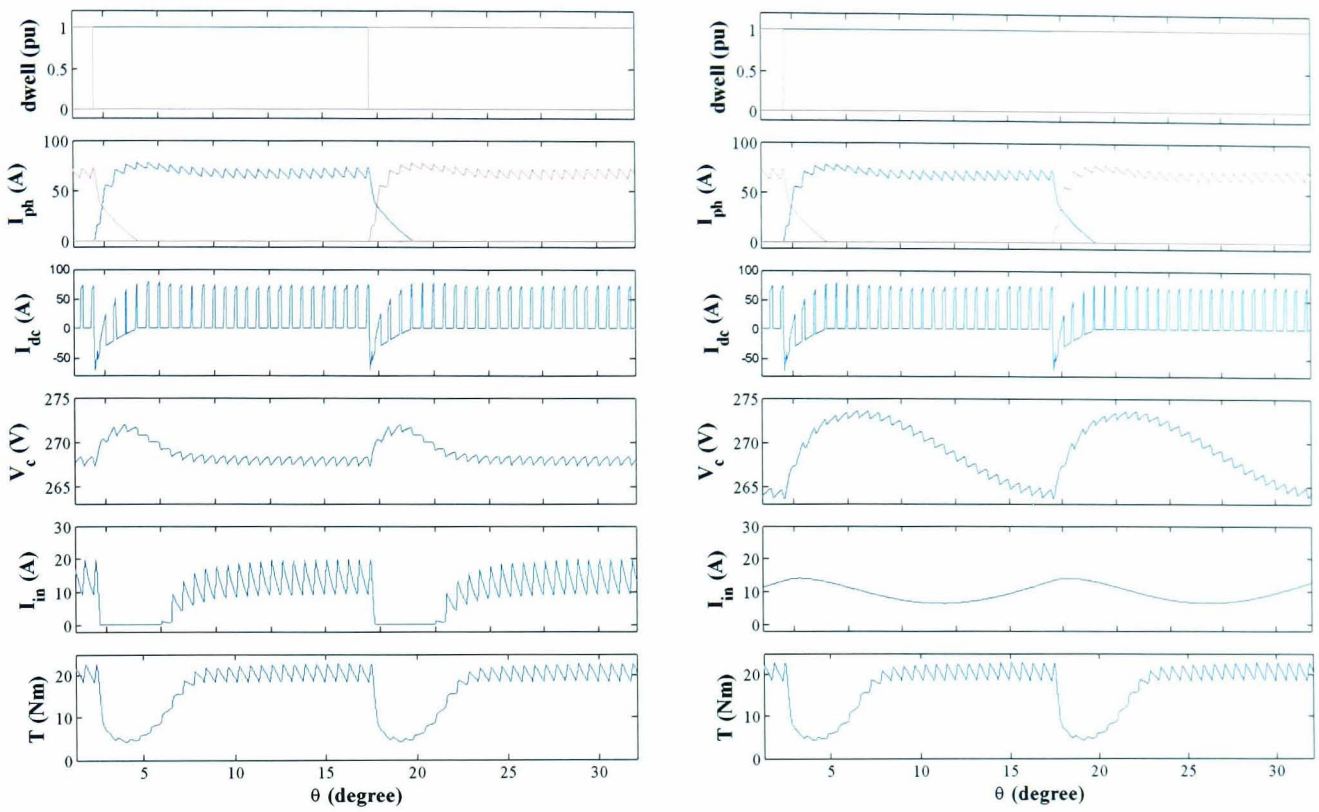
As can be seen, the advantage of this technique is that the phase current tail is shorter than that of the UHC. Although in Figure 2.25(b) the phase current tail is longer than that in Figure 2.25(a), both of the phase current tails are shorter than those in Figure 2.24. For the capacitor voltage, this method can reduce the voltage ripple with the diode rectifier power circuit by 45% of the HCC voltage ripple, while with the dc bus bar circuit, it can reduce 30% of the voltage ripple of the HCC. This shows that the VHC is more effective with the diode rectifier circuit than with the dc bus bar power

circuit. The difference is due to the inductive filter. In the dc bus bar circuit with the inductive filter, a part of energy variation in the inductor will be transferred to the capacitor leading to extra voltage ripple whereas in the diode rectifier circuit no inductor is employed.

In Figure 2.25(a), the input current drops to zero during the commutation period. This may cause the current harmonic in the AC grid. The input current in the dc bus bar power circuit in Figure 2.25(b) has small ripples. For the simulation results of the machine torque, the VHC differs from other techniques in that the two different types of power circuits yield different machine torque waveforms. This is caused by the much different phase currents. The inductor in the dc bus bar power circuit extends the current tail of the outgoing phase and results in negative torque which reduces the output torque of the machine, as shown evidently around 10° in Figure 2.25(b).

Pulse Width Modulation Current Control (PWMCC)

PWMCC is employed to compare with other techniques which have a constant switching frequency since the switching frequency in the HCC is not fixed. This method use a PI current controller to generate PWM voltage signal with a constant switching frequency. Figure 2.26 shows the simulation results of the PWMCC.



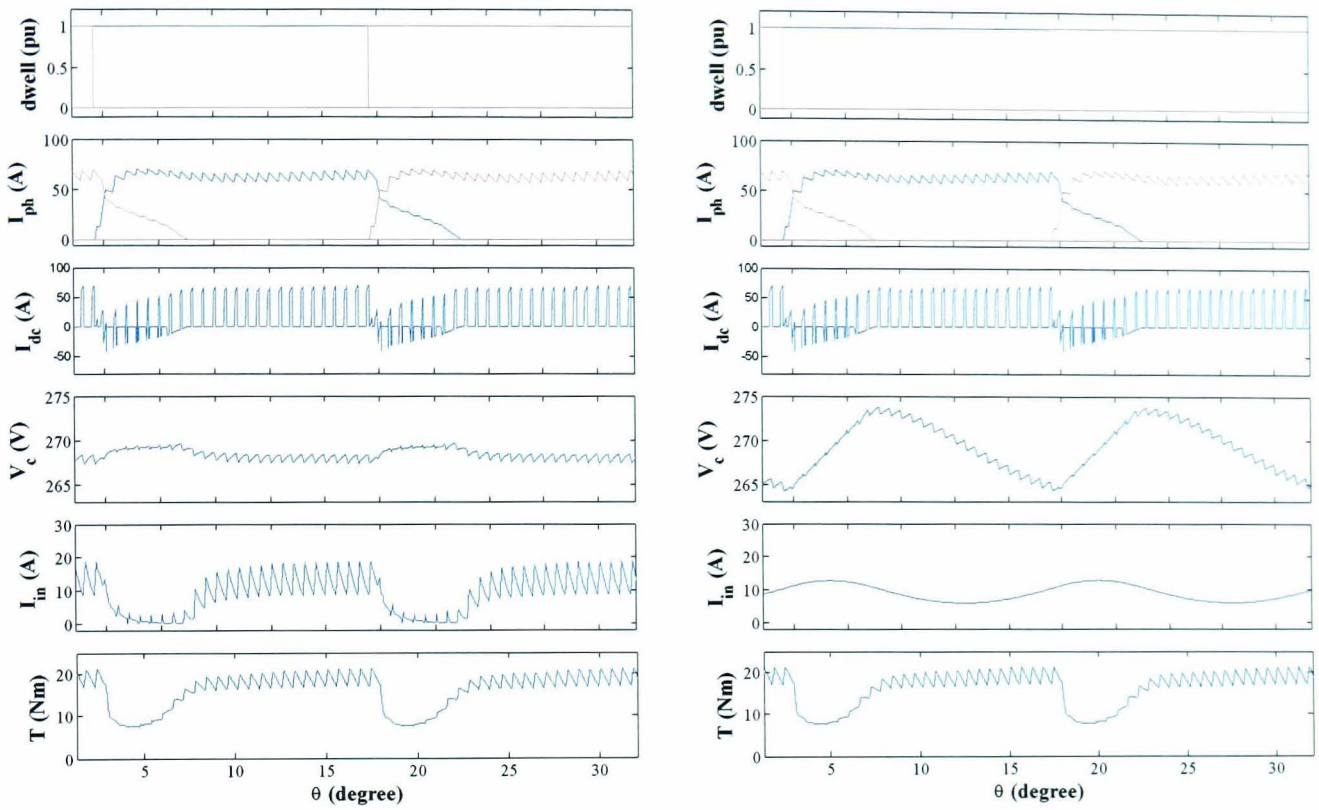
a) diode rectifier (b) dc bus bar

Figure 2.26: Simulation results from PWMCC (15° = 2.5 ms)

The results from the diode rectifier power circuit are illustrated in Figure 2.26(a) and the results from the dc bus bar power circuit are in Figure 2.26(b). Since the PWMCC is controlled with a fixed switching period, the phase current of this technique rises slower than that of the HCC, but the patterns and the amplitudes of other results are similar to those of the HCC. For example, the ripple of the capacitor voltage from the PWMCC in the dc bus bar circuit is 10.04V and that from the HCC is 10.96V. The difference is less than 1 V.

Power Balancing Control (PBC)

In the PBC, PWMCC is applied during the dwell period. The balance of power transfer is used during the commutation period. the de-fluxing energy from the outgoing phase is injected to the incoming phase in the same amount. Figure 2.27 shows the simulation results of the PBC.



a) diode rectifier (b) dc bus bar

Figure 2.27: Simulation results from PBC (15° = 2.5 ms)

The capacitor voltage from the diode rectifier circuit in Figure 2.27(a) is completely different from that in Figure 2.27(b) which results from the dc bus bar circuit. In Figure 2.27(a), the amplitude of the voltage ripple is very low while that in Figure 2.27(b) is significantly higher even though the same control technique is applied. The high voltage ripple in Figure 2.27(b) is caused by the inductor in the dc bus bar circuit. Due to the control scheme, the de-fluxing energy from the outgoing phase is fed to the incoming phase. Almost no energy is required from the dc-link capacitor. This cause the energy stored in the inductor to be transferred to the capacitor as shown in Figure 2.28, and nearly constant increase in the capacitor voltage. At the end of the commutation the converter draws the current from the dc-link, and the capacitor voltage starts to decrease.

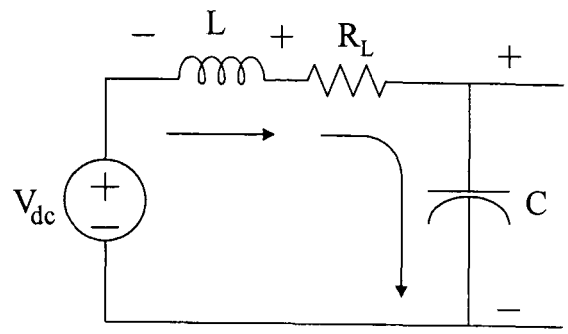


Figure 2.28: Stored energy in inductor transferred to capacitor

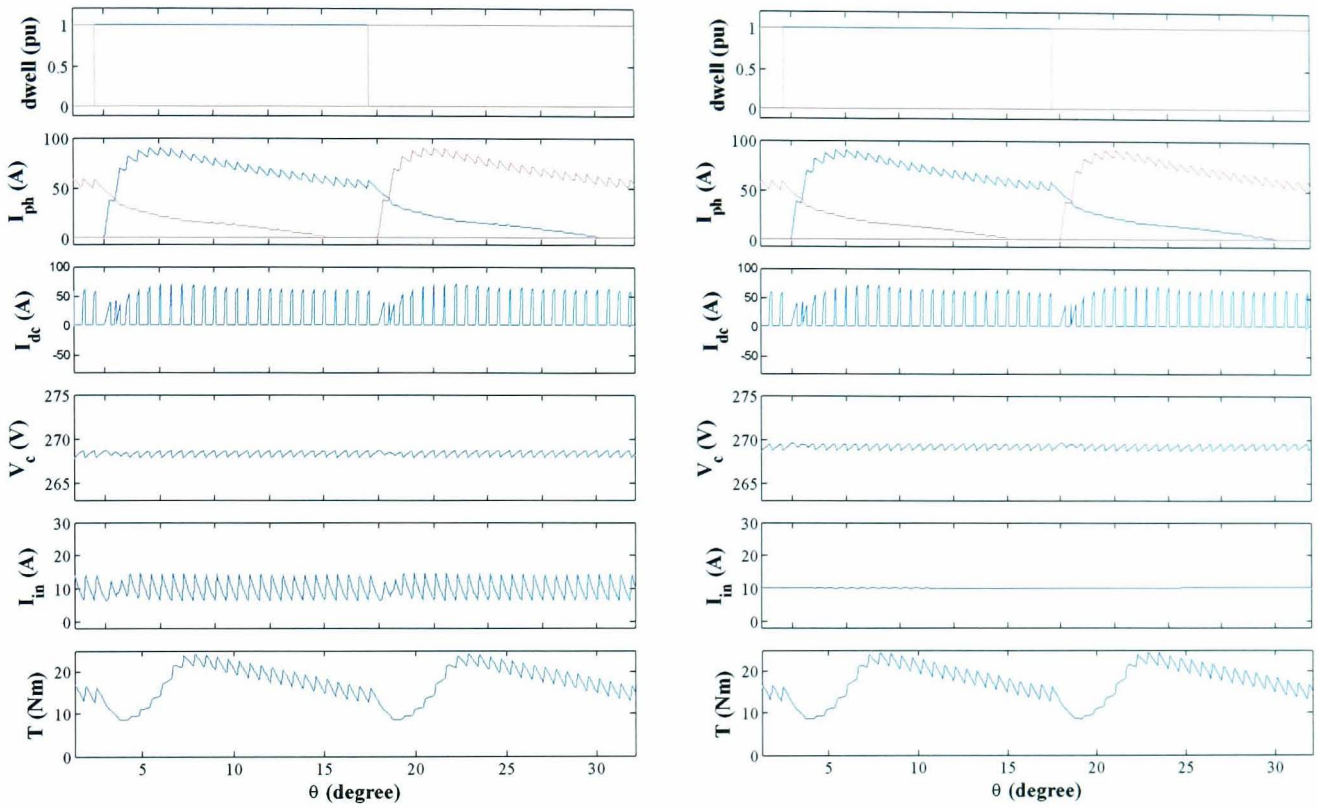
The input current from the diode rectifier circuit is almost all zero during the commutation since there is no energy transferred to and from the converter. Consequently, the input current fluctuation is much greater. The input current in the dc bus bar circuit is similar to that from other techniques and smoothed by the inductor. The torque ripple in the PBC is slightly less than that in the PWMCC since after the turn-off angle, the phase current is still high but, the tail is shorter, yielding positive torque.

Dc-Link Current Integration Control (DLCIC)

The DLCIC is different from other techniques in that it maintains a constant average dc-link current over a switching period during the phase conduction and commutation. Figure 2.29 shows the simulation results of the DLCIC where Figure 2.29(a) presents the results from the diode rectifier power circuit and Figure 2.29(b) presents the results from the dc bus bar power circuit.

The capacitor voltages from both the circuits in Figure 2.29(a) and (b) are virtually identical, and is much smoother compared with the other techniques. Since the average dc-link current in every switching period is constant, the energy transfer to the converter is constant. The dc-link capacitor buffers the same amount of the energy in a switching cycle in each stroke. Thus, the input and output energy of the dc-link capacitor is low and there is no accumulative energy to be stored in the capacitor during the stroke period. The input current of the DLCIC is also constant, especially in Figure 2.29(b), with the dc bus bar circuit, since it is further filter out by the inductor. In Figure 2.29(a), the input current increases and decreases along with the charging and

discharging steps of the dc-link capacitor since there is no inductor to smooth the current.



a) diode rectifier (b) dc bus bar

Figure 2.29: Simulation results from DLCIC (15° = 2.5 ms)

Since the machine torque depends on phase current, but the phase current is not directly controlled in DLCIC. As can be seen from Figure 2.29, at the beginning of the dwell period, the machine torque is high since the amplitude of the phase current is increased. The incoming phase receives the current from the outgoing phase and the dc-link. Although the current in the outgoing phase may produce negative torque, it is much less than the positive torque from the incoming phase. The machine torque of the DLCICI decreases along with the decay in the outgoing phase current. This is different from the torque waveforms of the UHC in Figure 2.24 since it controls a constant phase current. When there is no additional current from the outgoing phase current, the phase current of the active phase is still gradually decreased due to the increase in electromagnetic force (EMF) voltage [2.17-2.21]. Hence, the machine torque from the DLCIC is not

constant by nature. However, the torque ripple from Figure 2.29 is less than the torque ripple from HCC and PWMCC in Figure 2.23 and Figure 2.26.

The average dc-link current ($I_{dc,avg}$), the average torque (T_{avg}), the torque ripple (T_{p2p}), the capacitor voltage ripple ($V_{c,p2p}$), the rms phase current ($I_{ph,rms}$), torque per copper loss (T/I^2R), and torque per ampere (T/I), in Figure 2.23 - 2.29 are summarised in Table 2.2 and Table 2.3. Table 2.2 presents the details from the diode rectifier power circuit and Table 2.3 presents the results from the dc bus bar power circuit.

The results from both tables are similar except for the capacitor voltage ripple due to the effect of the power supply circuits. From the tables, the lowest voltage ripple is from DLCIC. The voltage ripples from the PWMCC in both tables are close to those from the HCC. The voltage ripple from other techniques such as the UHC, and the VHC are reduced by around 50% of the HCC voltage ripple. For the PBC, the voltage ripple from the diode rectifier circuit is 50% of the HCC, whereas the voltage ripple of the PBC with the dc bus bar circuit is quite close to that of the HCC. This is because during the commutation, there is no energy transfer between the converter and the dc-link. The inductor current in the dc bus bar circuit charges the dc-link capacitor. This causes the high fluctuation in the capacitor voltage of the dc bus bar circuit.

From both the tables, the torque ripples from the HCC and the PWMCC are the highest. The torque ripple of DLCIC is less than those of HCC and PWMCC when the dwell period is equal to the stroke period. Torque ripples from other techniques are lower than those of HCC and PWMCC since the current tails are longer. This long current tail overlapping with the incoming phase current results in the similar effect to that of the overlapping in the dwell periods which smoothes the torque ripple.

Table 2.2 Simulation results from diode rectifier power circuit

Technique	$I_{dc,avg}$ (A)	T_{avg} (Nm)	T_{p2p} (Nm)	$V_{c,p2p}$ (V)	$I_{in,p2p}$ (A)	$I_{ph,rms}$ (A)	T/I^2R (10^{-2} Nm/W)	T/I(10^{-1} Nm/A)
HCC	9.74	17.08	19.24	4.82	18.56	40.41	6.15	4.23
UHC	10.47	18.06	13.25	2.35	23.23	42.26	5.95	4.27
VHC	9.98	17.54	17.24	2.68	18.56	40.75	6.21	4.30
PWMCC	9.32	16.41	18.62	4.73	19.77	39.31	6.25	4.17
PBC	8.77	15.73	13.35	2.35	18.86	37.18	6.69	4.23
DLCIC	9.83	17.03	15.93	0.89	8.77	40.77	6.03	4.18

Table 2.3 Simulation results from dc bus bar power circuit

Technique	$I_{dc,avg}$ (A)	T_{avg} (Nm)	T_{p2p} (Nm)	$V_{c,p2p}$ (V)	$I_{in,p2p}$ (A)	$I_{ph,rms}$ (A)	T/I^2R (10^{-2} Nm/W)	T/I (10^{-1} Nm/A)
HCC	9.75	17.10	19.24	10.96	8.73	40.42	6.16	4.23
UHC	10.49	18.10	13.14	6.67	4.19	42.33	5.94	4.28
VHC	9.82	16.99	17.90	7.70	5.11	41.09	5.92	4.14
PWMCC	9.36	16.41	18.63	10.05	7.71	39.31	6.25	4.18
PBC	8.77	15.73	13.88	9.62	6.94	37.18	6.69	4.23
DLCIC	9.86	16.99	16.44	1.03	0.30	41.06	5.93	4.14

The rms phase current from the UHC and VHC is higher than that from the HCC since their phase current tails are longer than that from the HCC. The rms phase current from the DLCIC is higher than that from the PWMCC due to the same reason. Although the phase current tail of the PBC is longer than that of the PWMCC, the rms phase current from the PBC is lower. This is because during the commutation period, the magnitude of the phase current of PWMCC is higher than that of the PBC, due to higher capacitor voltage. This results in faster increase in the phase current of PWMCC. In addition, the phase current of the PBC is the lowest among all techniques. This causes the average torque of PBC being also the lowest.

Although the torque per copper loss and the torque per ampere from all techniques are close, the values of the HCC and PWMCC are higher than those of the DLCIC since the rms phase current of the DLCIC is higher. The torque per copper loss of DLCIC is lower than that of PBC since the rms phase current of DLCIC is much higher than that of PBC. The phase current tail of DLCIC is longer than that of PBC. The torque per copper loss of the PBC is higher than those of the PWMCC and HCC since although the average torque of PBC is low, the rms phase current of the PBC is also low. Although the phase current tail of PBC is longer than that of PWMCC, the phase current level of PBC is lower than that of PWMCC. During the commutation period, the incoming phase current of PBC charges the current only from the outgoing phase while the incoming phase current of PWMCC charges from the dc-link current and the outgoing phase. The phase current of PBC increase slower than that of PWMCC and it is also lower than that of PWMCC. This makes the torque per copper loss of the PBC highest.

From Figure 2.23 - 2.29 and Table 2.2 and Table 2.3, the ripple of the dc-link capacitor voltage from DLCIC is lowest than those from the other techniques although the torque per copper loss of DLCIC is slightly lower than those of the HCC and PWMCC since the phase current tail of the DLCIC is longer that of the two techniques.

2.6 Spectrum of Dc-link Current

The dc-link current affects the voltage of the dc-link capacitor since it is the dynamic input of the power circuit. Since the current harmonics at and above the switching frequency can be easily filtered, the harmonic at integer multiples of the commutation frequency is of great importance. Hence, in this section, FFT is utilised to analyse the dc-link current spectrum. Since the machine speed is 1000 rpm and the commutation frequency is 400 Hz, the spectrum is shown in the low frequency range from 1 - 2000 Hz.

Since the simulation results from two types of the power circuits are shown in Section 2.4, in this section the spectra of the dc-link currents from the two power circuits are illustrated. Although the dc-link currents of each technique from the two power circuits are very similar, it is not exactly the same. The power circuit slightly affects the dc-link current of VHC in Figure 2.25. The harmonics of the dc-link current in the commutation frequency range from the dc bus bar power circuit are presented in Figure 2.18(a) for the machine speed of 1000 rpm. The amplitude of the harmonics from the DLCIC is very low when comparing with those from the other techniques. It shows that there is almost no harmonic in the commutation frequency range from the DLCIC. The commutation frequency harmonics is the cause of the large fluctuation in the capacitor voltage, and in the input current.

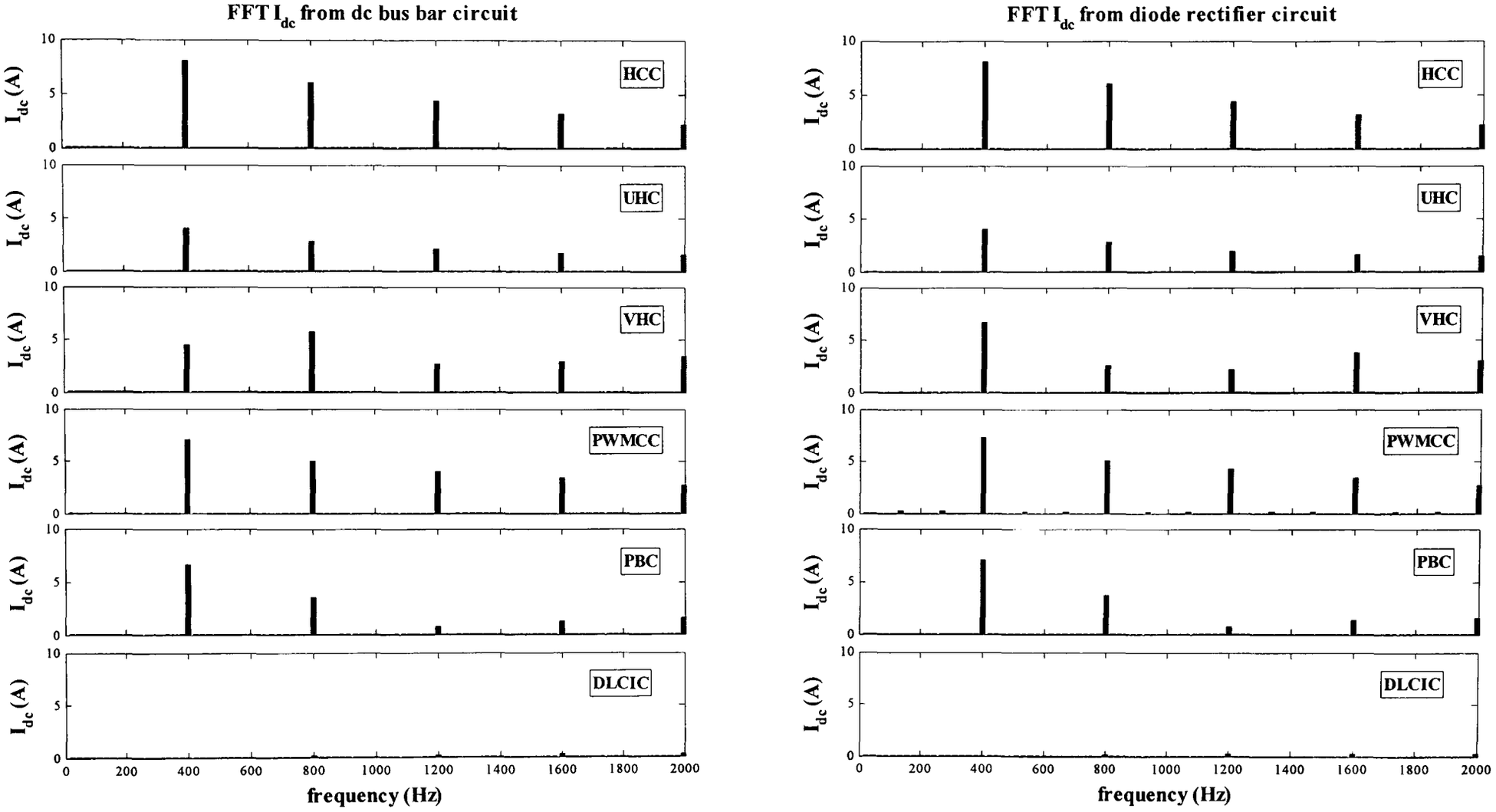
Moreover, the highest amplitudes of the dc-link current harmonics from the other techniques are at the commutation frequency, 400 Hz, except for the VHC, where it occurs at the twice of the commutation frequency. The harmonics at the commutation frequency from the dc-link current result in the high fluctuation in the dc-link capacitor voltage since the low frequency harmonics is hard to be filtered out [2.23 - 2.27].

Figure 2.30 (b) presents the harmonics spectra of the dc-link currents which are obtained with the diode rectifier power circuit under the six techniques. The harmonics

in the commutation frequency range from DLCIC are almost zero. A similar trend to those in Figure 2.30 (a) is observed. The harmonics in the commutation frequency range are very low even in the dc-link current. Thus, it is seen that the commutation frequency harmonics in the capacitor voltage of DLCIC are very low and so is the voltage ripple.

2.7 Conclusion

In this chapter, the principle of the DLCIC has been proposed and described in order to reduce the capacitance of the dc-link capacitor in an SR machine drive. The simulation results of the DLCIC such as the dc-link capacitor voltage and the input current with the dc bus bar power circuit and the diode rectifier power circuit are shown. Furthermore, the simulation results are compared with those obtained from other techniques, i.e., HCC, UHC, VHC, PWMCC, PBC. It has been shown that the capacitor voltage ripples from the DLCIC with either power circuits are very low when comparing with those of the other techniques. Since the capacitor voltage fluctuates at the commutation frequency, the harmonics of the dc-link current in the commutation frequency range from the DLCIC are also compared with those of the other techniques. The spectra show that the harmonics in the commutation frequency range from the DLCIC are the lowest among the six methods.



(a) (b)

Figure 2.30: Dc-link current spectrum from dc bus bar circuit and diode rectifier

2.8 Reference

[2.1] P. J. Lawrenson, J. M. Stephenson, N. N. Fulton, P. T. Blenkinsop, and J. Corda, "Variable-speed switched reluctance motors," *Electric Power Applications, IEE Proceedings B,* vol. 127, pp. 253-265, 1980.

[2.2] W. F. Ray, "Switched reluctance drives," in *Proc. Energy Efficient Environmentally Friendly Drive Systems Principles, Problems Application (Digest No: 1996/144), IEE Colloquium on*, 1996, pp. 3/1-3/9.

[2.3] K. M. Rahman and S. E. Schulz, "High-performance fully digital switched reluctance motor controller for vehicle propulsion," *Industry Applications, IEEE Transactions on,* vol. 38, pp. 1062-1071, 2002.

[2.4] P. J. Lawrenson, J. M. Stephenson, N. N. Fulton, P. T. Blenkinsop, and J. Corda, "Variable-speed switched reluctance motors," *Electric Power Applications, IEE Proceedings B,* vol. 127, pp. 253-265, 1980.

[2.5] T. A. Lipo and F. Liang, "Variable reluctance drive system," U.S. Patent, 1995.

[2.6] B. K. Bose, "Power electronics and motor drives-recent technology advances," in *Proc. Industrial Electronics, 2002. ISIE 2002. Proceedings of the 2002 IEEE International Symposium on*, 2002, pp. 22-25 vol.1.

[2.7] R. Krishnan and P. N. Materu, "Analysis and design of a low-cost converter for switched reluctance motor drives," *Industry Applications, IEEE Transactions on,* vol. 29, pp. 320-327, 1993.

[2.8] F. Liang, L. Yuefeng, and T. A. Lipo, "A new variable reluctance motor utilizing an auxiliary commutation winding," *Industry Applications, IEEE Transactions on,* vol. 30, pp. 423-432, 1994.

[2.9] C. R. Neuhaus, N. H. Fuengwarodsakul, and R. W. De Doncker, "Control Scheme for Switched Reluctance Drives With Minimized DC-Link Capacitance," *Power Electronics, IEEE Transactions on,* vol. 23, pp. 2557-2564, 2008.

[2.10] C. R. Neuhaus and R. W. De Doncker, "DC-link voltage control for Switched Reluctance Drives with reduced DC-link capacitance," in *Proc. Energy Conversion Congress and Exposition (ECCE), 2010 IEEE*, 2010, pp. 4192-4198.

[2.11] L. Han, X. Wen, G. Chen, F. Zhao, and J. Gao, "A Practical Software Strategy to Reduce DC Bus Bar Surge Voltage in AC Drives Fed by VSI," in *Proc. Power Electronics Specialists Conference, 2007. PESC 2007. IEEE*, 2007, pp. 497-502.

[2.12] M. C. Caponet, F. Profumo, R. W. De Doncker, and A. Tenconi, "Low stray inductance bus bar design and construction for good EMC performance in power electronic circuits," *Power Electronics, IEEE Transactions on,* vol. 17, pp. 225-231, 2002.

[2.13] B. Beker, J. L. Hudgins, J. Coronati, B. Gillett, and S. Shekhawat, "Extraction of parasitic circuit elements in a PEBB for application in the virtual test bed," in *Proc. Industry Applications Conference, 1997. Thirty-Second IAS Annual Meeting, IAS '97., Conference Record of the 1997 IEEE*, 1997, pp. 1217-1221 vol.2.

[2.14] H. J. Beukes, J. H. R. Enslin, and R. Spee, "Busbar design considerations for high power IGBT converters," in *Proc. Power Electronics Specialists Conference, 1997. PESC '97 Record., 28th Annual IEEE*, 1997, pp. 847-853 vol.2.

[2.15] H. Wen, W. Xiao, H. Li, and X. Wen, "Analysis and minimisation of DC bus surge voltage for electric vehicle applications," *Electrical Systems in Transportation, IET,* vol. 2, pp. 68-76, 2012.

[2.16] M. Frisch, Erno, x, and T., "Power module with additional low inductive current path," in *Proc. Integrated Power Electronics Systems (CIPS), 2010 6th International Conference on*, 2010, pp. 1-6.

[2.17] S. Dixon and B. Fahimi, "Enhancement of output electric power in switched reluctance generators," in *Proc. Electric Machines and Drives Conference, 2003. IEMDC'03. IEEE International*, 2003, pp. 849-856 vol.2.

[2.18] F. R. Salmasi, B. Fahimi, H. Gao, and M. Ehsani, "Sensorless control of switched reluctance motor drive based on BEMF calculation," in *Proc. Applied Power Electronics Conference and Exposition, 2002. APEC 2002. Seventeenth Annual IEEE*, 2002, pp. 293-298 vol.1.

[2.19] O. Cornea, D. Popovici, and A. Argeseanu, "A switched reluctance motor drive model using standard simulink library components," in *Proc. Optimization of Electrical and Electronic Equipment, 2008. OPTIM 2008. 11th International Conference on*, 2008, pp. 69-74.

[2.20] T. Humiston and P. Pillay, "Flux weakening operation of switched reluctance motors," in *Proc. Power Engineering Society Winter Meeting, 2001. IEEE*, 2001, pp. 1372-1377 vol.3.

[2.21] T. J. E. Miller, "Converter Volt-Ampere Requirements of the Switched Reluctance Motor Drive," *Industry Applications, IEEE Transactions on,* vol. IA-21, pp. 1136-1144, 1985.

[2.22] W. Honghua, "Analysis and reduction of vibration of switched reluctance motor drives in voltage pulse width modulation mode," in *Proc. Power Electronics and Motion Control Conference, 2009. IPEMC '09. IEEE 6th International*, 2009, pp. 850-854.

[2.23] C. Y. Wu and C. Pollock, "Time domain analysis of vibration and acoustic noise in the switched reluctance drive," in *Proc. Electrical Machines and Drives, 1993. Sixth International Conference on (Conf. Publ. No. 376)*, 1993, pp. 558-563.

[2.24] J. Y. Chai, Y. W. Lin, and C. M. Liaw, "Comparative study of switching controls in vibration and acoustic noise reductions for switched reluctance motor," *Electric Power Applications, IEE Proceedings -*, vol. 153, pp. 348-360, 2006.

[2.25] C. H. Rivetta, A. Emadi, G. A. Williamson, R. Jayabalan, and B. Fahimi, "Analysis and control of a buck DC-DC converter operating with constant power load in sea and undersea vehicles," *Industry Applications, IEEE Transactions on,* vol. 42, pp. 559-572, 2006.

[2.26] M. U. Iftikhar, D. Sadarnac, and C. Karimi, "Input Filter Damping Design for Control Loop Stability of DC-DC Converters," in *Proc. Industrial Electronics, 2007. ISIE 2007. IEEE International Symposium on*, 2007, pp. 353-358.

[2.27] K. Louati, D. Sadarnac, and C. Karimi, "Input filter influence on the control stability of DC/DC converters," in *Proc. Industrial Electronics, 2004 IEEE International Symposium on*, 2004, pp. 1165-1171 vol. 2.

[2.28] M. Baumann, U. Drofenik, and J. W. Kolar, "New wide input voltage range three-phase unity power factor rectifier formed by integration of a three-switch buck-derived front-end and a DC/DC boost converter output stage," in *Proc. Telecommunications Energy Conference, 2000. INTELEC. Twenty-second International*, 2000, pp. 461-470.

Chapter 3

Determination of Optimal Turn-on and Turn-off Angles

3.1 Introduction

The dc-link current integration control (DLCIC) has been described in the previous chapter and can reduce the voltage ripple of the dc-link capacitor when comparing with other techniques. This implies the dc-link capacitance is consequently reduced.

In literatures, several research papers have been published to determine the optimal turn-on and turn-off angles for SR motors [3.1 - 3.8]. In some papers, the optimal angles are decided by maximising the efficiency [3.3 - 3.5], while in others by maximising the average torque [3.6 - 3.8]. In [3.6], the optimal angles are found by maximising the average torque and maximising the area of the energy conversion loop. This technique has been adopted here to find the optimal angles of DLCIC. The flux trajectory of the optimal DLCIC is compared with the flux of the hysteresis current

control (HCC) and the pulse width modulation voltage control (PWMVC) in order to find the optimal angles of DLCIC. The procedure to find the optimal angle of DLCIC is described subsequently.

In this chapter, the method to find the optimal turn-on and turn-off angles as well as the speed operation range of DLCIC, will be investigated and analysed. In the first half of this chapter, the speed range of the DLCIC operation will be found. The optimal turn-on and turn-off angles of the HCC described in [3.6] have been simulated and compared with that of the DLCIC obtained from numerical simulation. The numerical process of how to find the optimal turn-on and turn-off angles of DLCIC is explained. The characteristic graphs such as average torque and torque per ampere which are resulted from the HCC and DLCIC are analysed and compared. Then, the operation speed range of DLCIC is determined. In the second half, flux variations which are resulted from HCC, PWMVC, and DLCIC are compared. The optimal turn-off angles of the DLCIC are determined from the flux variation characteristics of HCC and PWMVC, and the optimal turn-on angles of DLCIC are found by the numerical trend obtained from the turn-on angles of HCC.

3.2 Optimal turn-on and turn-off under HCC and PWMVC

In order to find the optimal angles of the dc-link current integration control (DLCIC), the optimal operation of hysteresis current control (HCC) and pulse width modulation voltage control (PWMVC) must be found. Since the DLCIC maintains a constant average dc-link current, it seems to be a control method between the HCC current control and the PWM voltage control. Thus, the results from the HCC and PWMVC are used as references to find optimal angles of the DLCIC. The operation procedures of the HCC and PWMVC from [3.6] have been adopted since they propose a simple procedure to find the optimal turn-on and turn-off angles, which produce the maximum average torque. Moreover, the average dc-link current values of HCC are used as

references of the dc-link current demand in the DLCIC. The flux variation under PWMVC has been analysed in order to determine optimal turn-off angle of the DLCIC.

3.2.1 Hysteresis current control (HCC)

The optimal angles of HCC are adopted from 2 papers. The turn-on angle is determined according to [3.1] and the turn-off angle to [3.6]. To find the optimal turn-on angle of the HCC, the variation of the phase inductance with the rotor angle in relation to the phase current as shown in Figure 3.1 is considered. The inductance curve in Figure 3.1 is estimated from the actual inductance curve which is calculated from a finite element, as shown in Figure 3.2.

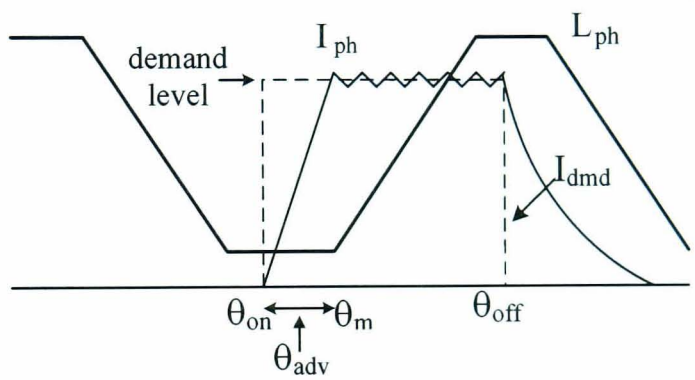


Figure 3.1: Relationship among θ_{on}, θ_m, and θ_{adv}

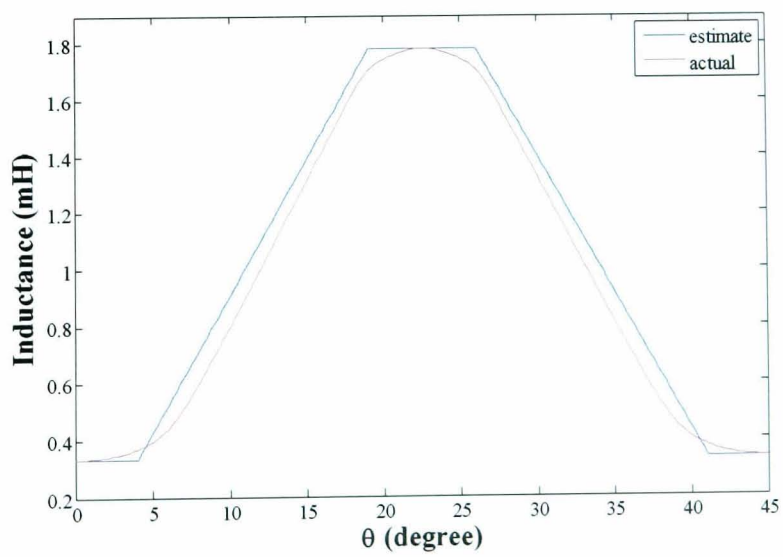


Figure 3.2: Actual and estimated phase winding inductance of SR machine

At the turn-on angle (θ_{on}), the switches of the converter for the active phase are turned on. This allows the phase current to directly rise from zero to the demand level at the corner point (θ_m) of the inductance curve. The optimal turn-on angle (θ_{on}) equation [3.1] is shown in (3.1), as

$$\theta_{on} = \theta_m - \theta_{adv} \tag{3.1}$$

and

$$\theta_{adv} = \frac{L_u \cdot \omega}{V_{dc}} I_{ph} \tag{3.2}$$

where

L_u is the inductance at the unaligned position.

ω is the rotational speed.

V_{dc} is the voltage of the DC supply.

I_{ph} is the phase current of SR machine.

The optimal turn-off angles are found by maximising the flux loop area of the phase current with the condition that the phase current at the turn-off angle is equal to the phase current demand (I_{dmd}). Beyond the turn-off angle (θ_{off}), the voltage across the phase winding is equal to the negative supply voltage ($-V_{dc}$). This causes the phase current speedily drops. In the optimal scenario, the phase current assumingly decreases across the aligned position. The flux ratio, x, at the aligned position varies from $\frac{1}{\sqrt{2}}$ to $\frac{2}{3}$ of the flux at the optimal turn-off position. The optimal turn-off angle equation of HCC in [3.6] is shown as

$$\theta_{off} = -\frac{\theta_m}{2}\left(-\frac{R_a}{R_{ua}} + \sqrt{\left(\frac{R_a}{R_{ua}}\right)^2 + 4\left(\frac{I_{dmd}(1-x)\omega}{R_{ua}V_{dc}\theta_m}\right)}\right) \tag{3.3}$$

where

R_a is the inverse of the inductance at the aligned position, $\frac{1}{L_a}$

R_{ua} is the inverse of the inductance at the un-aligned position minus the inverse of the inductance at the aligned position, $\frac{1}{L_u} - \frac{1}{L_a}$

I_{dmd} is the demand current level

x is the ratio of the flux at the aligned position to the flux at the optimal turn-off angle, varied between $\frac{1}{\sqrt{2}}$ to $\frac{2}{3}$

It is noted that the aligned position in (3.3) is equal to zero degree. Thus, the turn-off angle is converted so that the unaligned position is zero.

The optimal turn-on and turn-off angles of the SR machine have also been found by numerical simulations. The optimal turn-on and turn-off angles from the analytical equations in (3.1) and (3.3) are compared with those from the numerical simulation in Figure 3.3 and Figure 3.4. The average torques of the analytical and numerical angles are also compared in Figure 3.5. Although some of the numerical and analytical turn-on and turn-off angles in Figure 3.3 and Figure 3.4 are not close, the average torque from the analytical equations agree with the average torque from the numerical simulation. The analytical equation for the optimal turn-on and turn-off angles, (3.1) and (3.3), can be approximately used as the optimal turn-on and turn-off angles for the SR machine.

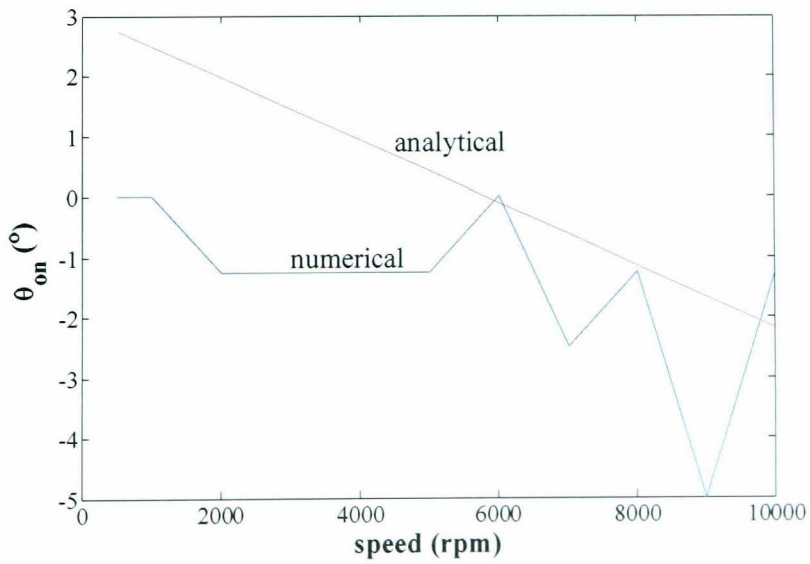


Figure 3.3: Numerical and analytical turn-on angle of HCC

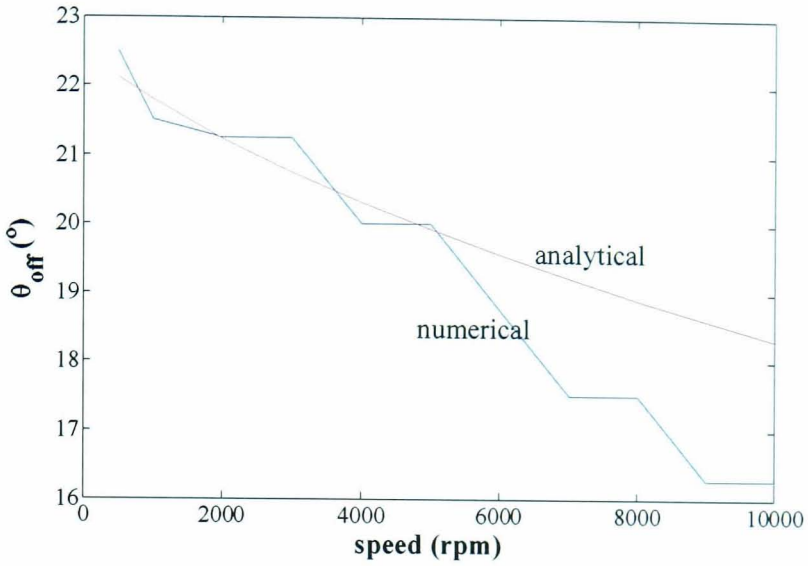


Figure 3.4: Numerical and analytical turn-off angle of HCC

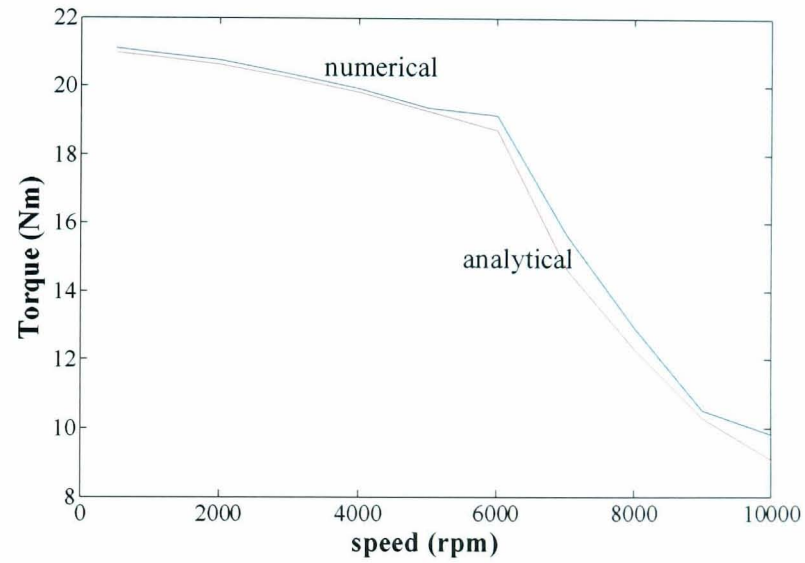


Figure 3.5: Numerical and analytical average torque of HCC

3.2.2 Pulse width modulation constant voltage control (PWMVC)

Pulse width modulation constant voltage control (PWMVC) is a control method which keep the average terminal voltage of the phase winding constant by using a constant duty cycle. The principle of finding the turn-on, turn-off and duty cycle here is adapted from [3.6]. The optimal angles of PWMVC are calculated from the flux variation at a given current demand (I_{dmd}), as shown in Figure 3.6. The rate of change of the flux linkage over the corner point (θ_m) to the aligned position (θ_a) is equal to the difference

between the flux linkage of the demand current at the aligned position ($\psi_a(I_{dmd})$) and that at the unaligned position ($\psi_u(I_{dmd})$). Thus, the optimal duty cycle in [3.6] is found from

$$D_g = \frac{\omega}{V_{dc}} \frac{\left(\psi_a(I_{dmd}) - \psi_u(I_{dmd})\right)}{\theta_a - \theta_m} \tag{3.4}$$

where

θ_a is the aligned rotor position.

I_{dmd} is the demand phase current.

$\psi_a(I_{dmd})$ is the flux linkage of the demand phase current at the aligned position.

$\psi_u(I_{dmd})$ is the flux linkage of the demand phase current at the un-aligned position.

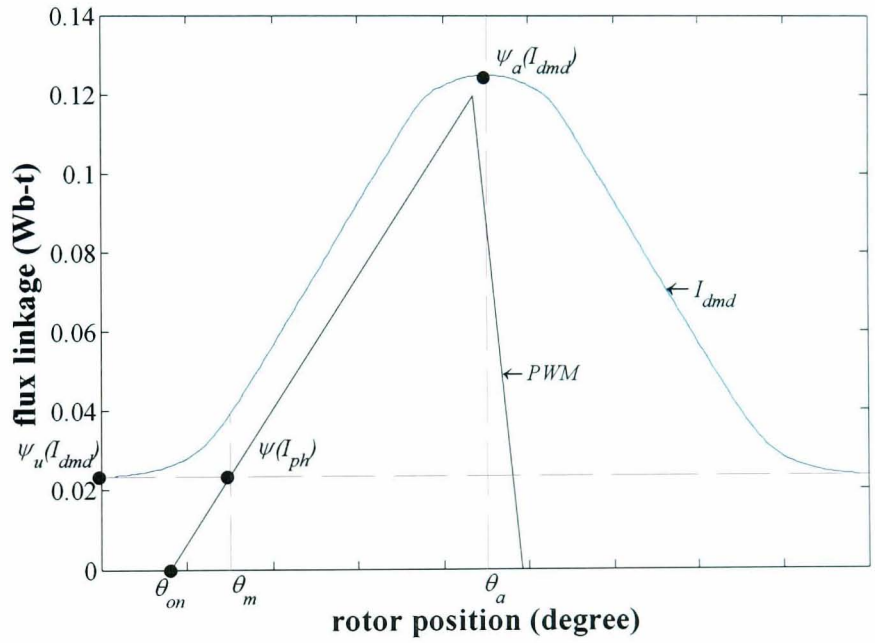


Figure 3.6: Phase current flux and demand current flux in [3.6]

With that duty cycle, the optimal turn-on angle (θ_{on}) is then found by

$$\theta_{on} = \theta_m - \frac{\omega L_u i_{dmd}}{D_g V_{dc}} \tag{3.5}$$

The optimal turn-off (θ_{off}) of PWMVC is determined similarly to that of HCC by maximising the flux linkage loop. The necessary condition at the optimal turn-off angle is defined by

$$\psi_{off} - D_g \frac{V_{dc}}{\omega}(\theta_{off} - \theta_{on}) = 0 \tag{3.6}$$

where ψ_{off} is the flux linkage at the turn-off angle (θ_{off})

Hence, the optimal turn-off angle in [3.6] is obtained, as

$$\theta_{off} = \frac{D_g}{D_g + \left(\frac{1}{1-x}\right)} \theta_{on} \tag{3.7}$$

where x is the ratio of the flux at the aligned position to the flux at the optimal turn-off angle, varied between $\frac{1}{\sqrt{2}}$ to $\frac{2}{3}$, as shown in Section 3.2.1.

The resulting phase current of the PWMVC from (3.4), (3.5), and (3.7) is much less than the demand phase current of the HCC since the flux of the optimal PWMVC phase current is lower than the flux of the HCC demand current. For the purpose of comparison, the flux of the PWMVC phase current should be increased to be equal to the flux of the HCC demand current (I_{dmd}), as shown in Figure 3.7.

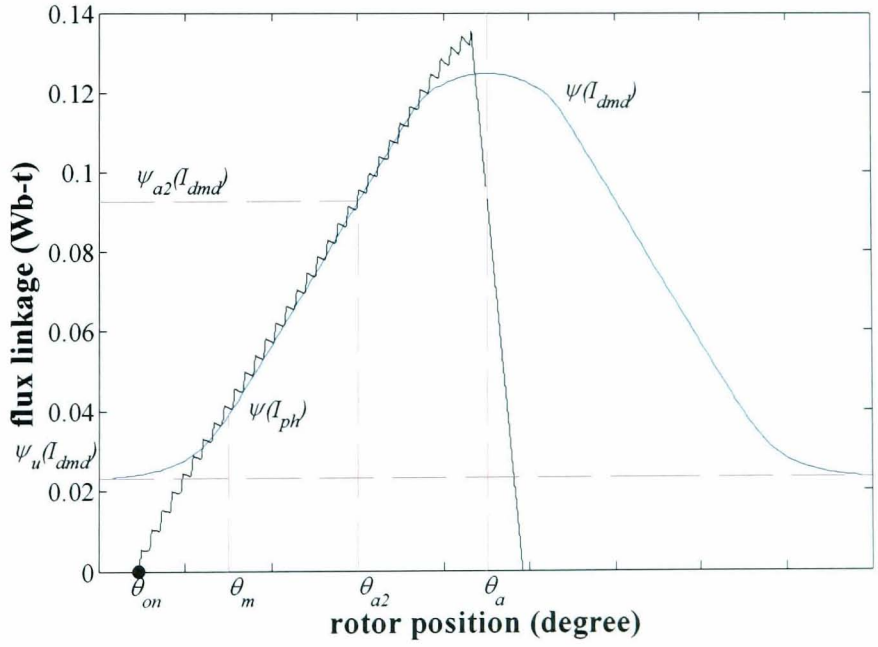


Figure 3.7: Comparison of flux linkage of demand current and PWMVC

To achieve this, the duty ratio of the PWMVC should be adjusted as follows. The flux of the phase current at the corner point (θ_m) of the inductance curve in Figure 3.7 is equal to the flux of the demand current at the same point. The slope of the phase current flux is found from the slope of the demand current flux between the corner point (θ_m) and the middle point (θ_{a2}) between the corner point and the aligned position. Moreover, the effect of the winding resistance is also included here since it is significant at the low speed range. The optimal duty cycle used in this chapter is presented, as

$$D = \frac{1}{V_{dc}}\left[RI_{dmd} + \omega \frac{\psi_{a2}(I_{dmd}) - \psi_m(I_{dmd})}{\theta_{a2} - \theta_m} \right] \tag{3.8}$$

where

θ_{a2} is the middle point between θ_m and θ_a.

$\psi_{a2}(I_{dmd})$ is the demand current flux at θ_{a2}.

$\psi_m(I_{dmd})$ is the demand current flux at θ_m.

R is the phase resistance of the SR machine.

From (3.8) and Figure 3.7, the optimal turn-on angle is obtained by,

$$\theta_{on} = \theta_m - \frac{\omega L_m I_{dmd}}{DV_{dc} - I_{dmd} R} \tag{3.9}$$

where L_m is the inductance of the demand phase current at θ_m

In the same way as (3.7), the optimal turn-off angle used in this chapter is derived as follows,

$$\theta_{off} = \frac{\theta_{on}}{1 + \frac{(V_{dc} + RI_{dmd})}{(DV_{dc} - RI_{dmd})(1 - x)}} \tag{3.10}$$

In this section, the equations to find the optimal turn-on and turn-off angles of HCC and PWMVC are described. The method to find the optimal turn-on and turn-off angles of DLCIC from the numerical simulation will be explained in the next section.

3.3 Determination of Optimal Angles by Numerical Simulation

While hysteresis current control (HCC) uses the optimal turn-on and turn-off angles to operate the switched reluctance machine at a given speed and torque, the optimal angles of dc-link current integration control (DLCIC), introduced in Chapter 2, are yet to be established. To find the optimal angles of the DLCIC, the average dc-link current obtained from HCC, is employed as the dc-link current demand for DLCIC. It is used to limit the average level of the dc-link current. This is to ensure the comparison of the two methods has the same basis.

To find the optimal angles of the DLCIC by numerical simulation, the dc current demand is kept as a constant value and the turn-on and turn-off angles are varied. The turn-off angle is chosen first as it is the main factor that influence the average torque [3.6]. Although the average torque (T_{avg}) is considered as the first priority to select the turn-off angle, the torque per copper loss (T/I^2R) and the peak to perk torque ripple (T_{p2p}) are also taken into account. After choosing the numeric optimal turn-off angle (θ_{off}), the numeric optimal turn-on angles(θ_{on}) are varied and selected with the same criteria.

For example, at 20-Nm torque and 100-rpm speed, the variation of the average torque (T_{avg})with turn-off angle for different values of turn-on angles is shown in Figure 3.8.

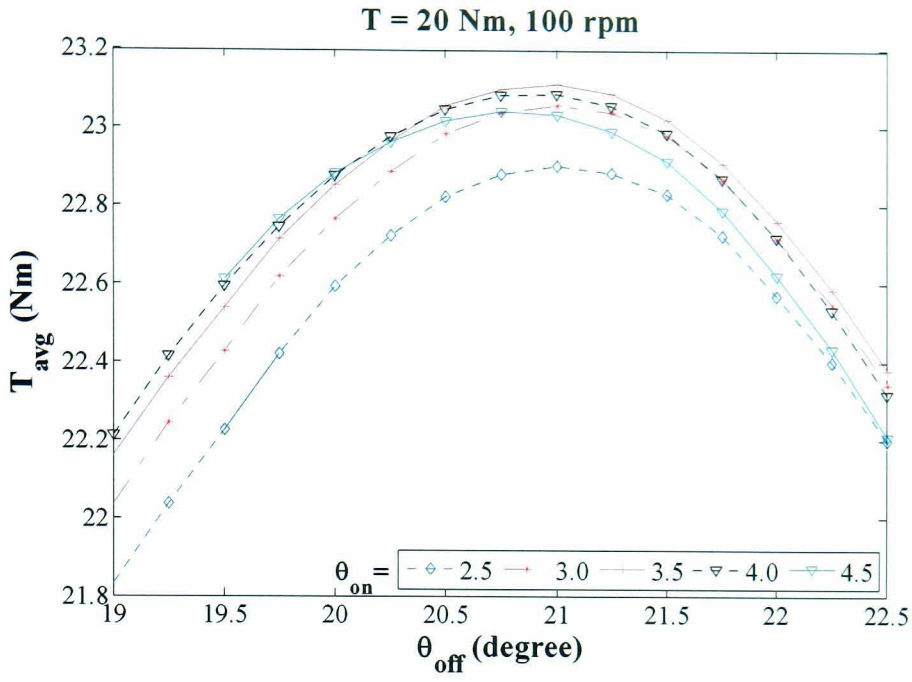


Figure 3.8: Variation of T_{avg} of DLCIC with θ_{off} at T = 20 Nm, 100 rpm

Turn-off angle at 21° yields the maximum average torque and has been chosen for the optimal turn-off angle. The torque per copper loss (T/I^2R) in Figure 3.9 also presents a similar trend while Figure 3.10 shows the variation of the peak-to-peak torque ripple (T_{p2p}) and indicates that at 21°, the peak-to-peak torque ripple is relatively low.

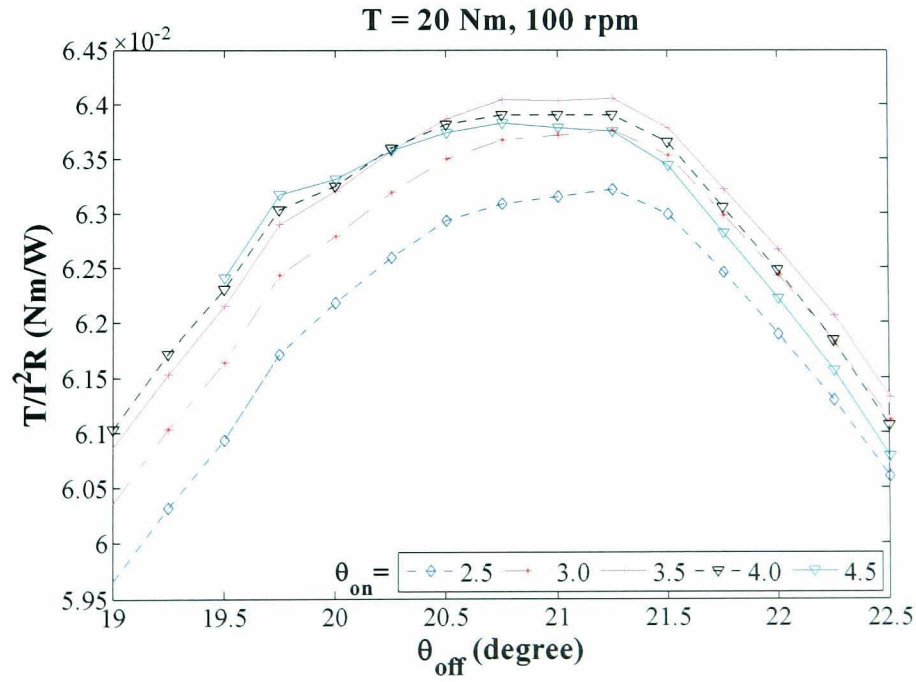


Figure 3.9: Variation of T/I^2R of DLCIC with θ_{off} at T = 20 Nm, 100 rpm

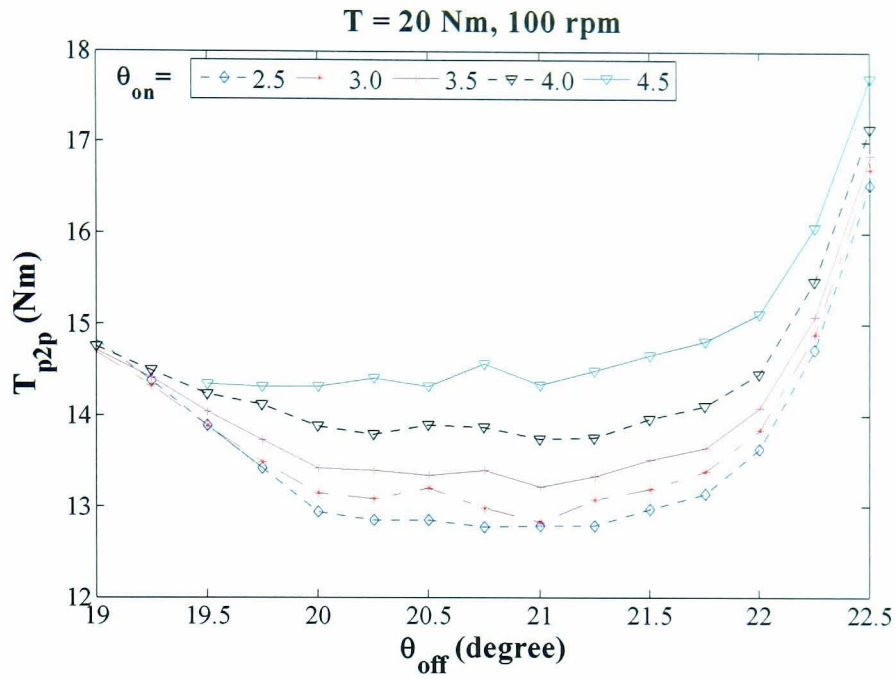


Figure 3.10: Variation of T_{p2p} of DLCIC with θ_{off} at T = 20Nm, 100rpm

Hence, the optimal turn-off angle is determined at 21°. The turn-on angles have been varied and the resulting variation of the average torque (T_{avg}), torque per copper loss (T/I^2R) and peak-to-peak torque (T_{p2p}) are illustrated in Figure 3.11, Figure 3.12 and Figure 3.13, respectively.

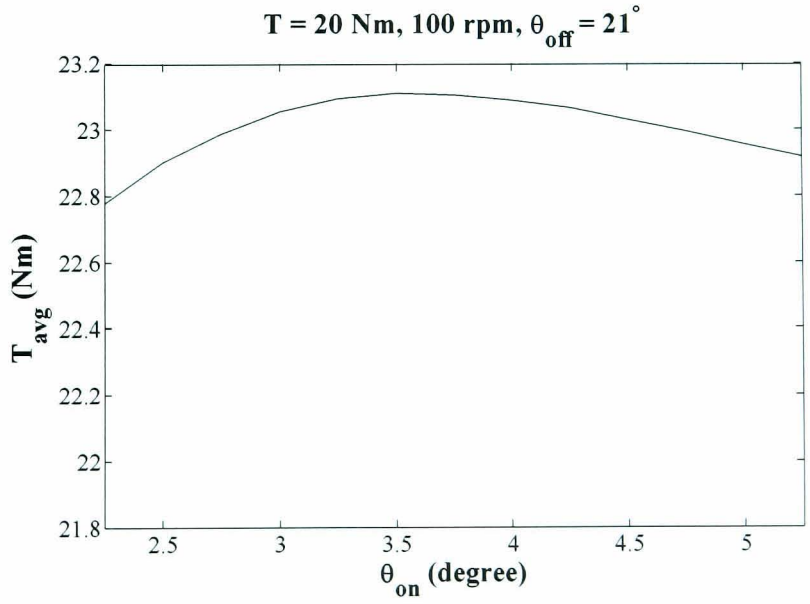


Figure 3.11: Variation of average torque of DLCIC with θ_{on} at T = 20Nm, 100rpm

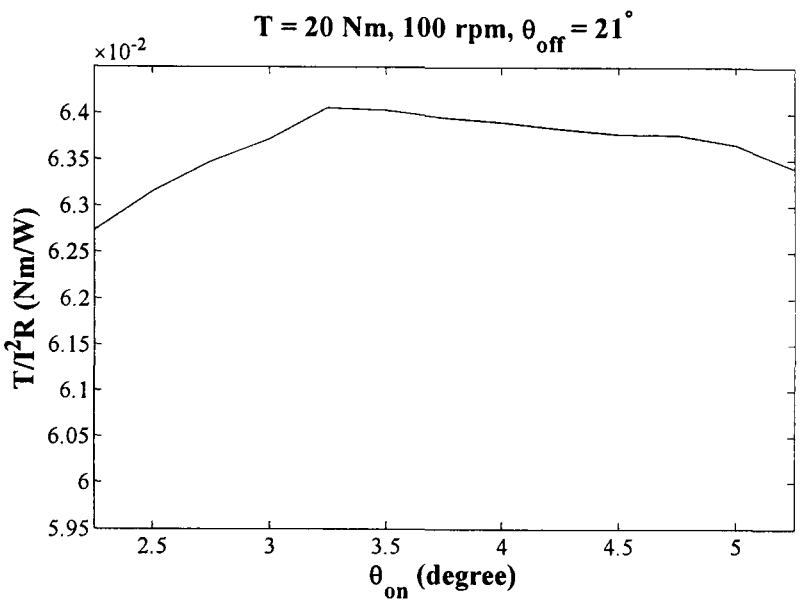


Figure 3.12: Variation of T/I^2R of DLCIC with θ_{on} at T = 20Nm, 100rpm

From these figures, the optimal turn-on angle at 3.5° has been chosen. At this angle, the average torque (T_{avg}) is maximum, the torque per copper loss (T/I^2R) is also high, and torque ripple (T_{p2p}) is relatively low.

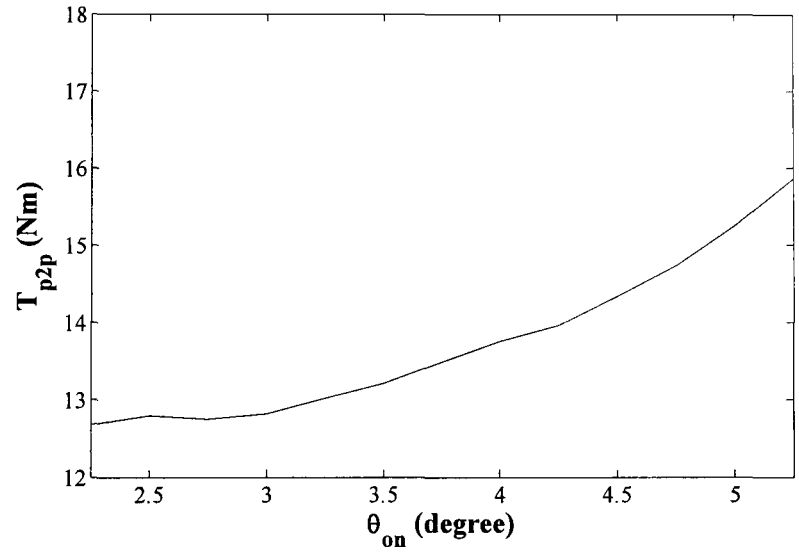


Figure 3.13: Variation of T_{p2p} of DLCIC with θ_{on} at T = 20Nm, 100rpm

Although in a very low speed range, e.g., 100 rpm, DLCIC is able to operate in all combinations of the turn-on and turn-off angles, in the high speed range, e.g., 3000 rpm, this is no longer possible. For instance, the average dc-link current of the DLCIC cannot reach the dc current demand as shown in Figure3.14. At 20Nm and 3000rpm,

when turn-on angle is equal to 2° and turn-off angle is 18.75°, the average dc-link current at the beginning of dwell period cannot reach to the dc current demand.

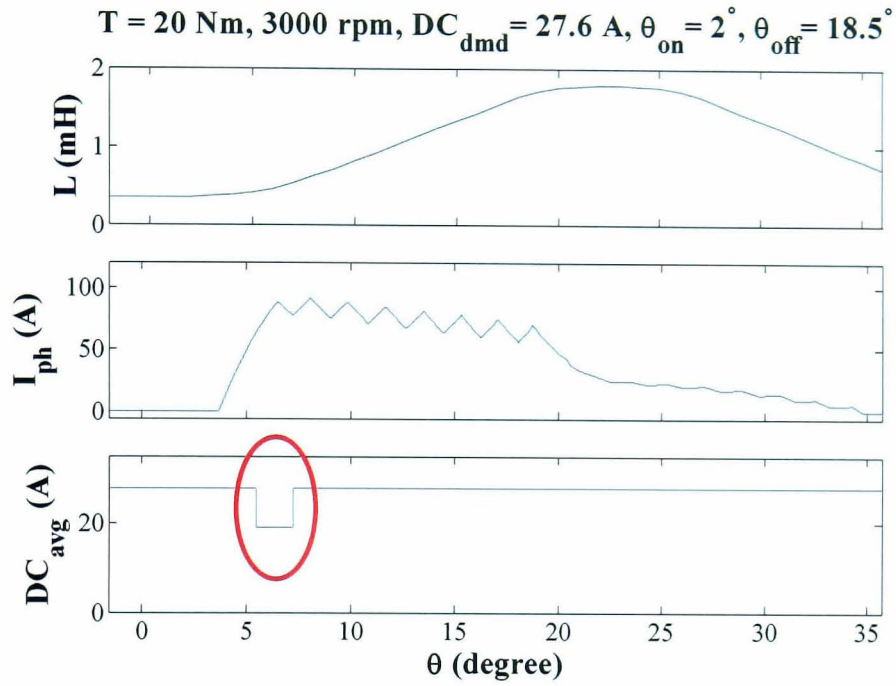


Figure 3.14: Average dc-link current less than dc current demand

Furthermore, when turn-off angle is 20° and turn-on angle is 2°, the phase current tail, which is the phase current beyond the turn-off angle, rises instead of falling when the rotor angle enters the generator zone where the slope of the phase inductance (L) is negative. In Figure 3.15, since the phase current (I_{ph}) rises in the generator zone, the machine torque (T) is negative. When the uncontrolled generating operation occurs, the average dc-link current (DC_{avg}) is negative and cannot reach the dc current demand (DC_{dmd}). These events should not allow to happen in the real operation. The operating range of turn-on and turn-off angles of the DLCIC is therefore limited. Hence, their boundary should be identified.

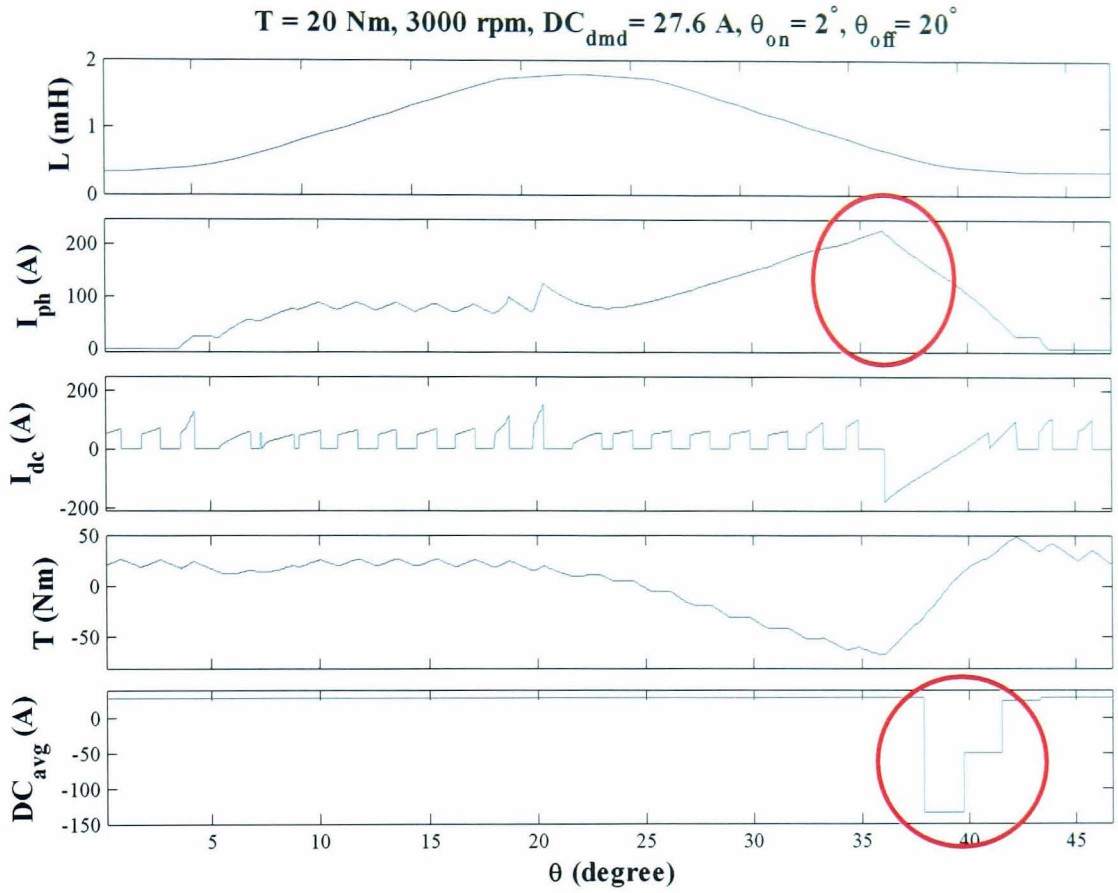


Figure 3.15: Phase current increasing in generator zone

3.4 Comparison between DLCIC and HCC

In the previous section, the process to acquire the numerical optimal turn-on and turn-off angles of dc-link current integration control (DLCIC) has been described. In this section, the operation speed range of DLCIC is determined by the characteristic comparison between hysteresis current control (HCC) and DLCIC, such as the average torque, torque per copper loss and rms phase current, at the rated torque, 20Nm. Then, the operation speed range of the DLCIC is determined. The characteristics at torques lower than the rated torque and within the operational speed range, are investigated, by simulations of 3-phase SR machine. To have the same basis for the DLCIC and HCC, the dc current demand of DLCIC is taken from the average dc-link current of HCC.

3.4.1 Operation Speed Range

Since a typical motor is designed to operate at the rated torque, the torque and current characteristics between the DLCIC and HCC at 20 Nm, the rated torque, are compared to find the operation speed range of DLCIC. Table 3.1 presents the speed, turn-on and turn-off angle details of the numerical optimal DLCIC. The comparisons of the average torques (T_{avg}), torque per ampere (T/I), torque per copper loss (T/I^2R), rms phase current ($I_{ph,rms}$), and peak-to-peak torque (T_{p2p}) ripple between HCC and DLCIC are shown in Figure 3.16, Figure 3.17, Figure 3.18, Figure 3.19 and Figure 3.20, respectively.

Table 3.1: Speed, turn-on and turn-off angle of optimal DLCIC at rated torque

speed (rpm)	θ_{on} ($^{\circ}_{mech}$)	θ_{off} ($^{\circ}_{mech}$)
100	3.5	21
500	3.25	19.75
1000	3	19.5
2000	2.5	19
3000	1.75	19
4000	-1	18.25
5000	-3	17.5
6000	-6	16
7000	-4.5	16
8000	-6	14.25
9000	-7.5	12.75
10000	-13.5	7.5

From Figure 3.16, it can be seen that most of the average torques (T_{avg}) from the DLCIC are close to those from HCC since the dc current demand, which is a main factor that influence the average torque, is taken from the average dc-link current of HCC. Torque per ampere (T/I) and torque per copper loss (T/I^2R) graphs are similar, as shown in Figure 3.17 and Figure 3.18. When the speed is below 3000 rpm, these values from the

DLCIC are higher than those from the HCC, but after 3000 rpm, torque per ampere and torque per copper loss from the DLCIC are less than those from the HCC. This is because the rms phase currents (I_{rms}) of the DLCIC over the speeds of 100 - 3000 rpm are lower than those of the HCC in the same speed. However, it is evident that from Figure 3.20, the torque ripples (T_{p2p}) of the DLCIC are much higher than those of the HCC. Hence, the operation speed range of DLCIC should not beyond by 3000 rpm. When the speed is higher than 3000 rpm, the machine operation will be switched to the HCC.

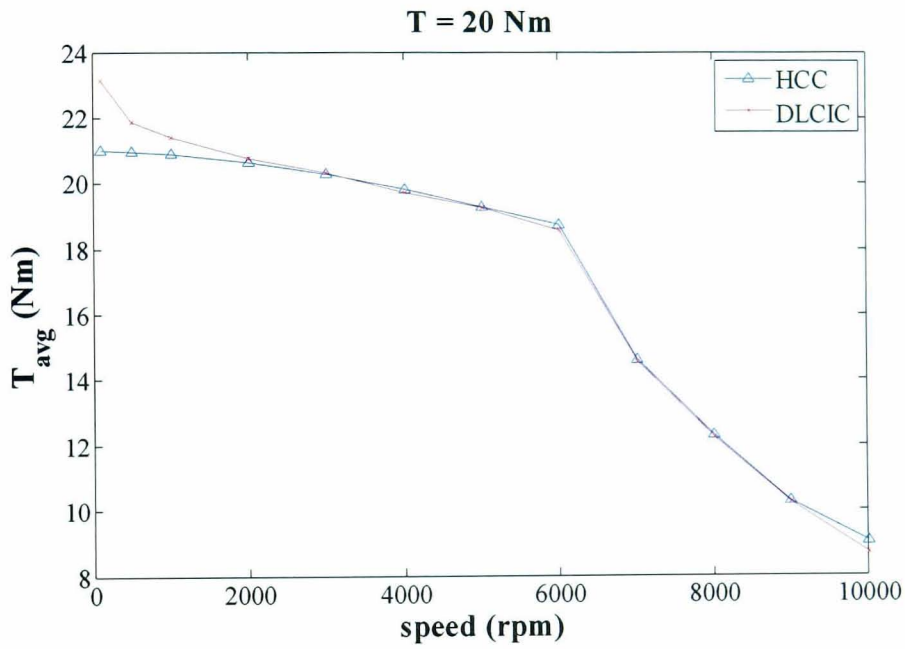


Figure 3.16: Comparison of average torque between HCC and DLCIC at 20 Nm

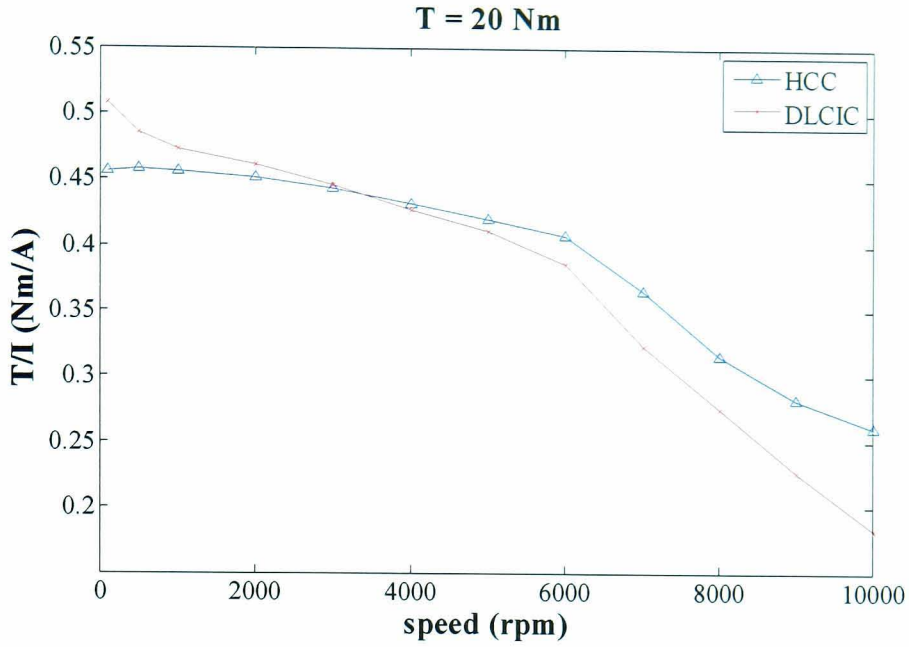


Figure 3.17: Comparison of torque per ampere between HCC and DLCIC at 20 Nm

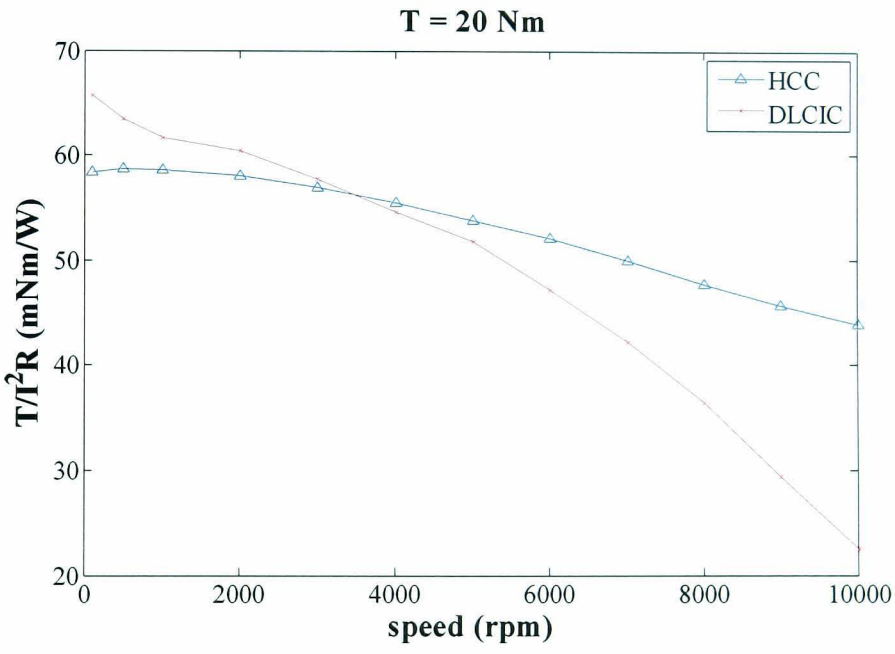


Figure 3.18: Comparison of torque per copper loss between HCC and DLCIC at 20 Nm

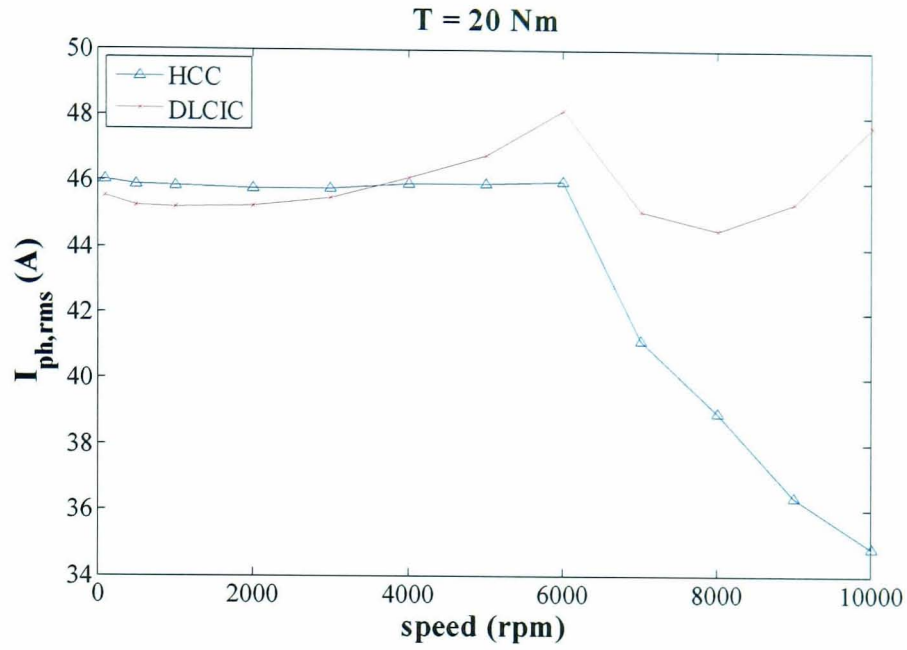


Figure 3.19: Comparison of rms phase current between HCC and DLCIC at 20 Nm

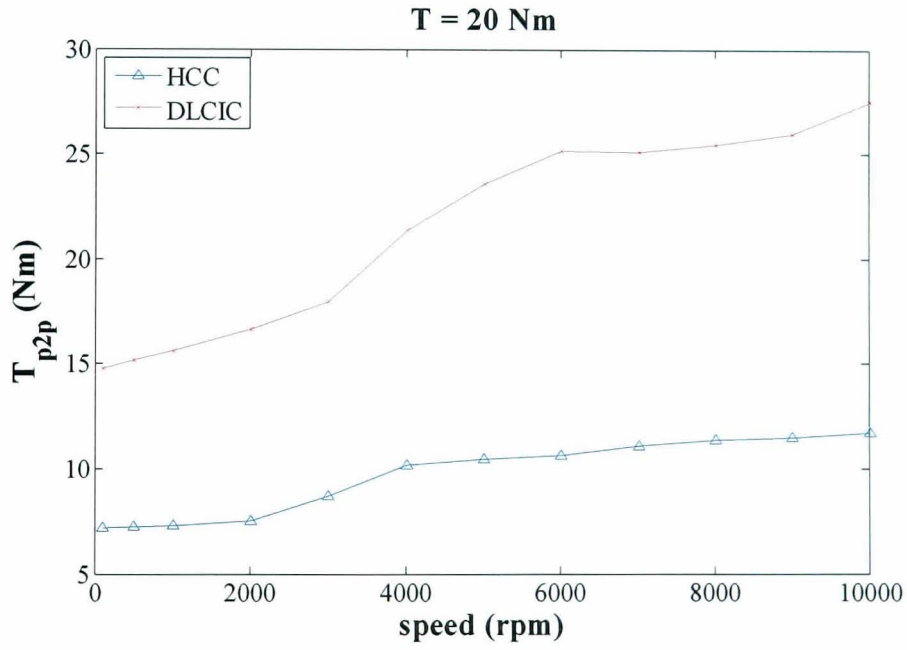


Figure 3.20: Comparison of torque peak-to-peak between HCC and DLCIC at 20 Nm

Although most of the average torques of DLCIC in Figure 3.16 are close to those of HCC, in the low speed range, 100 - 500 rpm, the average torque of DLCIC is higher than those of HCC since during the dwell period, most of the machine torque and the phase torque of DLCIC are higher than those of HCC, as shown in Figure 3.21. The figure compares the phase inductance (L), phase current (I_{ph}), phase torque (T_{ph}), and

machine torque (T) of DLCICL and HCC at 20 Nm, and 100 rpm. The phase current of the DLCIC over the period from 7° to 18° is higher than that of HCC and the variation of the phase inductance with the rotor position during that period is positive. These result in the average torque of DLCIC being higher than that of HCC.

Although the average torque of DLCIC in the low speed range, 100 - 500 rpm, is higher than that of HCC, the rms phase current of DLCIC is lower than that of HCC, as shown in Figure 3.18. This is because the dwell period of HCC is much longer than that of DLCIC, as shown in Figure 3.21. The phase current of HCC is high and constant from 3° to 22.5°, while the phase current of DLCIC is slightly higher than HCC during 7° to 18°. Therefore, the rms phase current of HCC is higher than that of DLCIC.

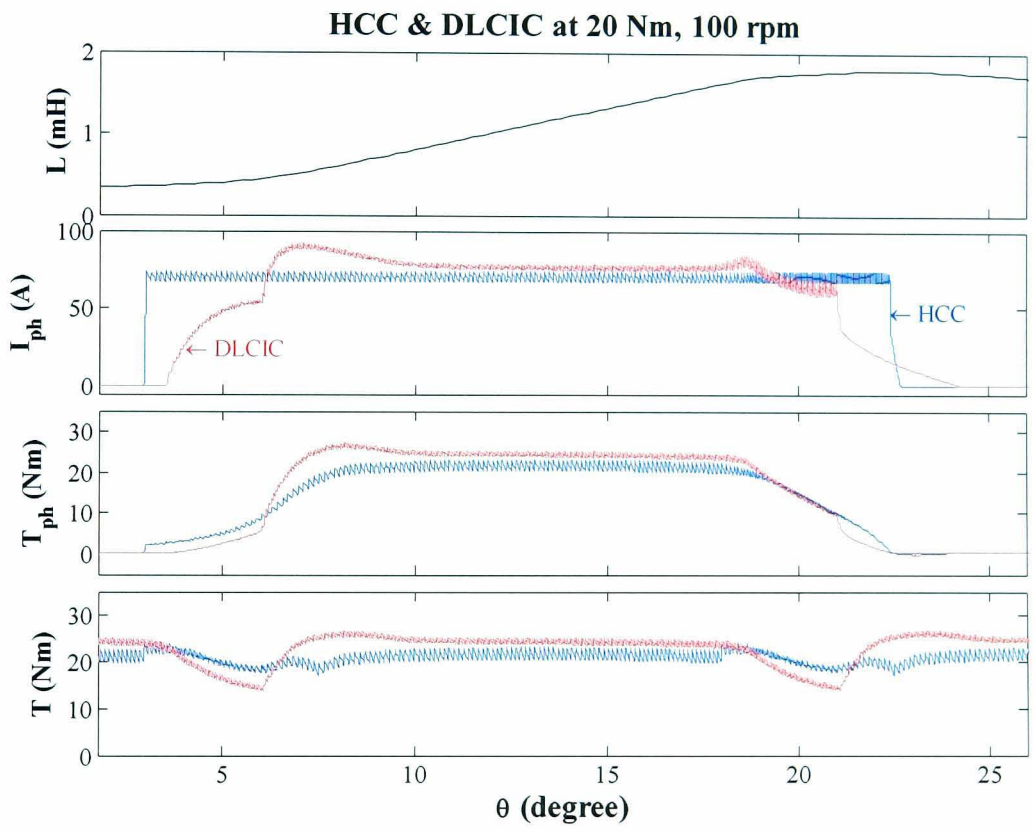


Figure 3.21: Comparison of current and torque of DLCIC and HCC at 20Nm, 100 rpm

The benefit of the long dwell period in HCC is the low torque ripple. The torque ripples (T_{p2p}) of HCC are always lower than those of DLCIC, as shown in Figure 3.20. However, the long dwell period cannot help to reduced the torque ripple in DLCIC. Figure 3.22 presents the overlap of the phase currents due to the long dwell period in DLCIC at 20 Nm, 100 rpm. During the overlap of the dwell period, the dc-link current,

which is maintain a constant average, is forced to fed 2 phase windings in the same time. The current and the torque of the outgoing phase rapidly reduce while those of the incoming phase slowly increase. Thus, the machine torque is substantially low since the slope of the inductance of the incoming phase is low. Hence, during the overlap period, a significant drop of the machine torque occurs.

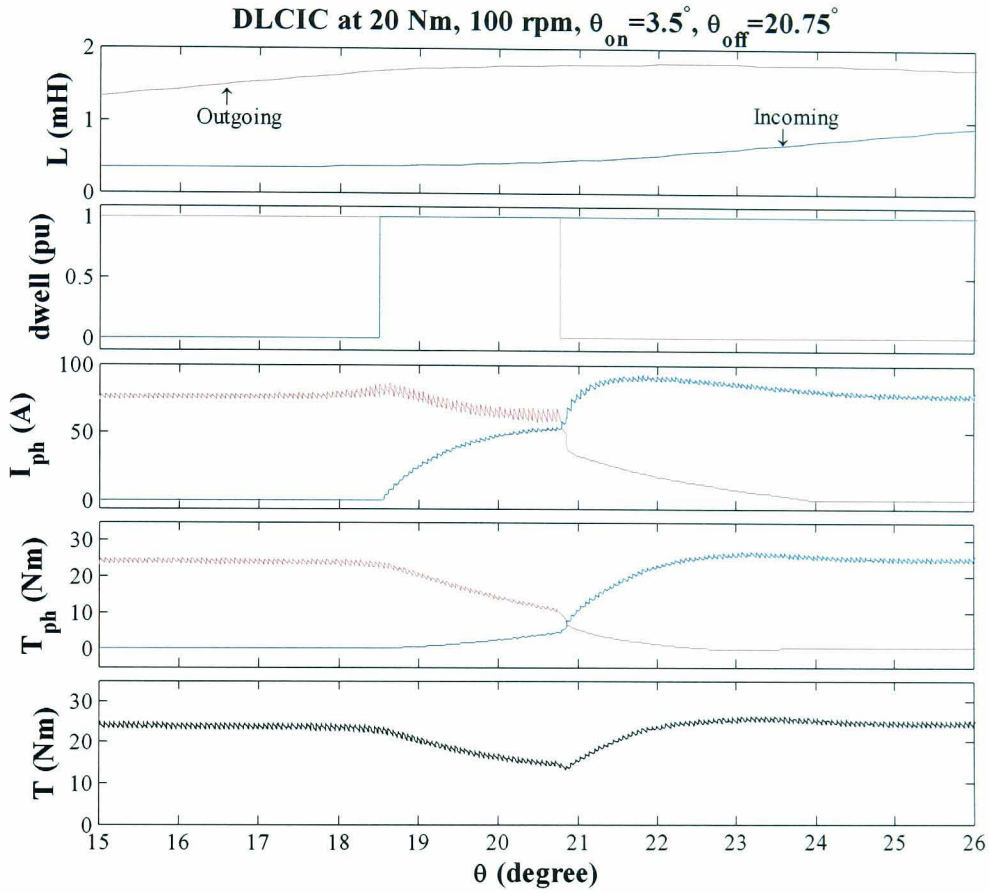


Figure 3.22: Overlapping dwell period of DLCIC at 20Nm, 100rpm

On the other hand, without the overlapped dwell period in Figure 3.23, during the commutation, the phase current of the outgoing phase decreases quickly and the phase current of the incoming phase slowly increases due to the need for maintaining a constant dc-link current. The torque of the incoming phase is low and the resulting torque ripple of DLCIC without overlapping dwell period might be higher than that with the overlapping dwell period.

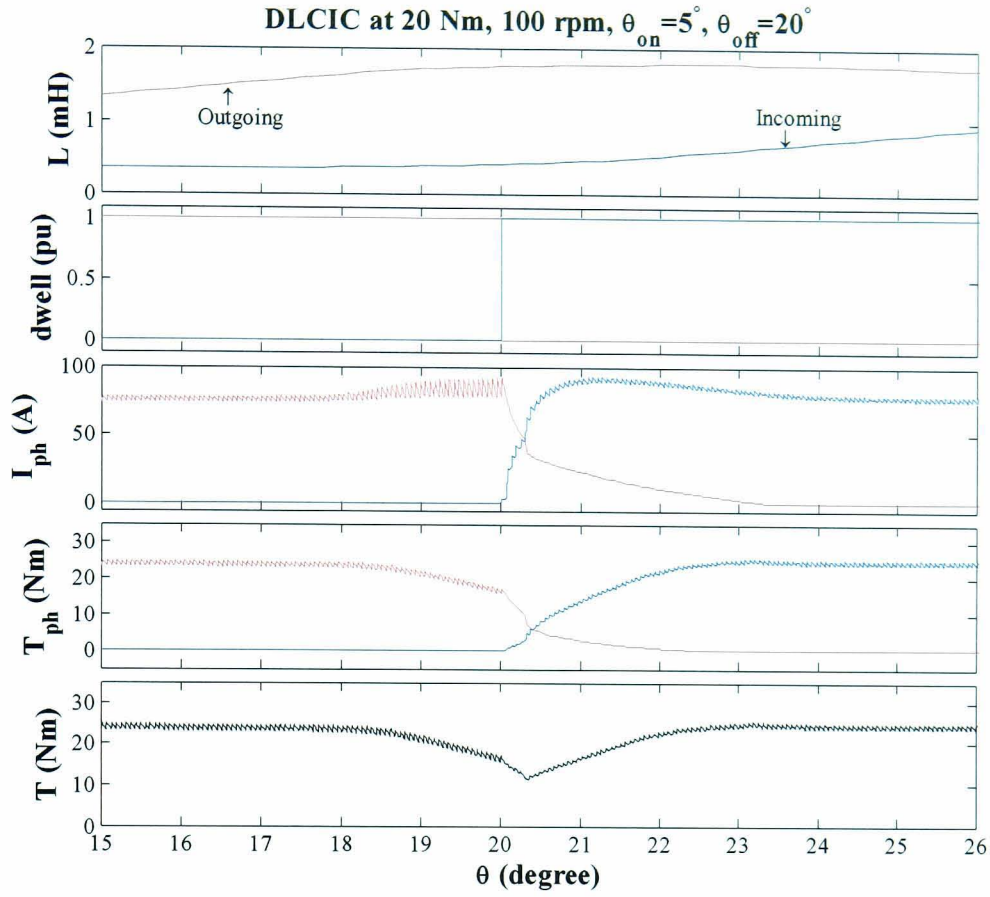


Figure 3.23: Commutation period without overlap of dwell period of DLCIC

Although the dc current demand of DLCIC is equal to the average dc-link current of HCC, the rms value of the phase current which results from DLCIC is different from those of HCC, as shown in Figure 3.19. The rms phase current of HCC is relatively constant when the speed is varied from 100 rpm to 6000 rpm. At the speed above 6000 rpm, the HCC is gradually turned into single pulse operation and becomes completely single pulse operation at 10000 rpm. Consequently, the phase current decreases with increase in speed. However, the rms phase current of DLCIC is not smooth as that of HCC. It looks like a parabolic curve until 6000 rpm, then dramatically drops and rises again.

There are two factors which affects the rms current of DLCIC. One is the dc current demand. Since the principle of DLCIC is to maintain a constant average dc-link current as the dc current demand, if the dc current demand rises, the rms phase current is increased accordingly.

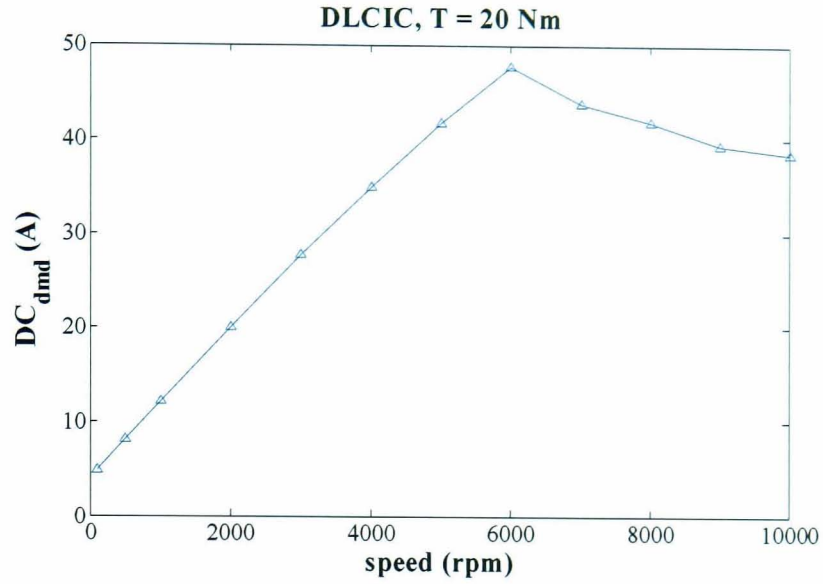


Figure 3.24: Variation of dc current demand with speed at 20Nm

The other is the speed. When the machine speed increases, for a given output torque, the dc current demand increases until 6000 rpm, as shown in Figure 3.24. When the dc current demand and the speed rise, the turn-on angle has to be advanced to maintain the average dc-link current being equal to the demand. The dwell period is then longer and the rms phase current is higher.

In Figure 3.19, above 6000 rpm, when the SR machine is gradually turned into the single pulse mode, the dc current demand reduces. Consequently, in the range of 6000 rpm to 8000 rpm the rms phase current reduces. Beyond 8000 rpm, the machine operates in a high speed range. The phase current during the turn-off time decreases slowly. Moreover, in a switching period, the turn-off time is shorter than the turn-on time. Consequently, the rms phase current of the DLCIC beyond 8000 rpm increases again. The machine operates as a single pulse completely at 10000 rpm. These explain the reasons of the unusual curve of the DLCIC phase current in Figure 3.19.

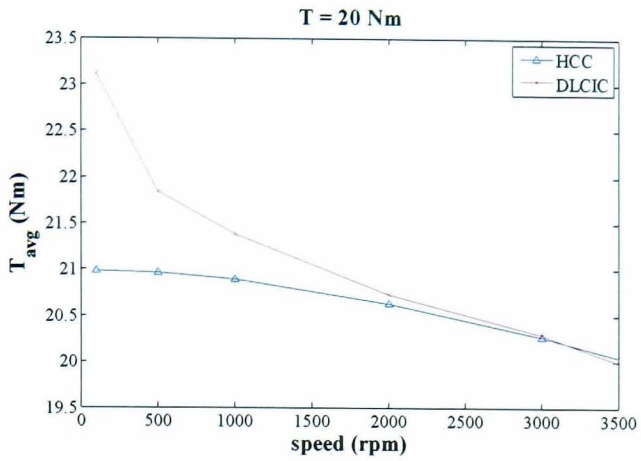
In summary, the performance of the DLCIC deteriorates compared to the HCC when the speed is greater than 3000 rpm. The operation speed range of DLCIC is, therefore, chosen from 100 to 3000 rpm.

3.4.2 Performance Evaluation of DLCIC

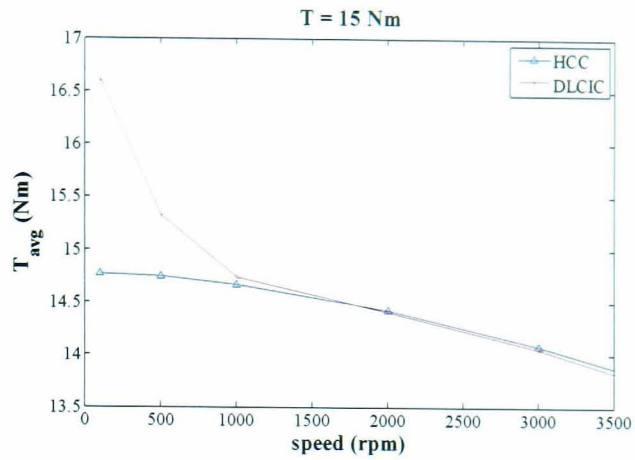
After the speed range of DLCIC is defined, 100 - 3000 rpm, the characteristics of DLCIC during the operation speed range are investigated in more detail.

Torque average (T_{avg})

Figure 3.25 compares the average torque from DLCIC and HCC at 20, 15, 10 and 5 Nm. The patterns of the average torque in Figure 3.25 (a) - (d) are similar. When the speed is very low speed, the average torque of DLCIC is higher than that of HCC since during the positive inductance slope period, the phase current of DLCIC is higher than that of HCC, as explained in Section 3.4.1. When the speed increases, the average torques of DLCIC is close to those of HCC since the dc current demand of DLCIC is taken from the average dc-link current of HCC. This implies the torque production capability of a DLCIC is slightly better than that of the HCC.



(a)



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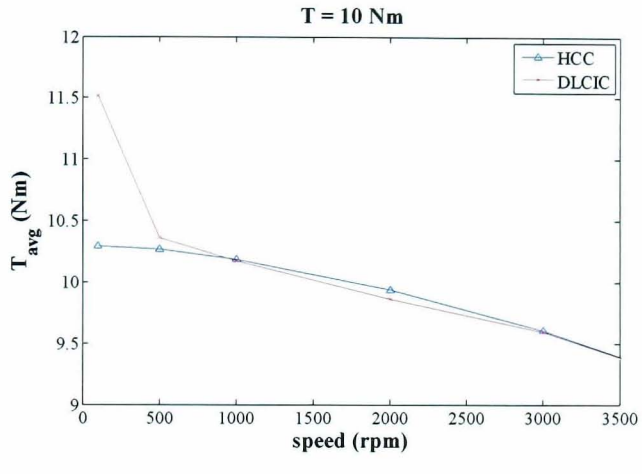
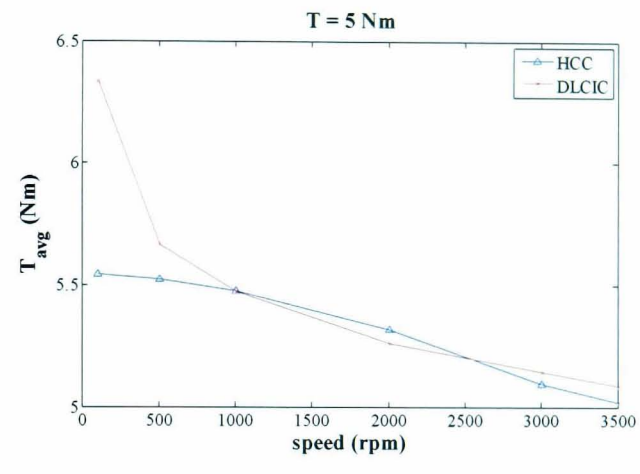


(c)



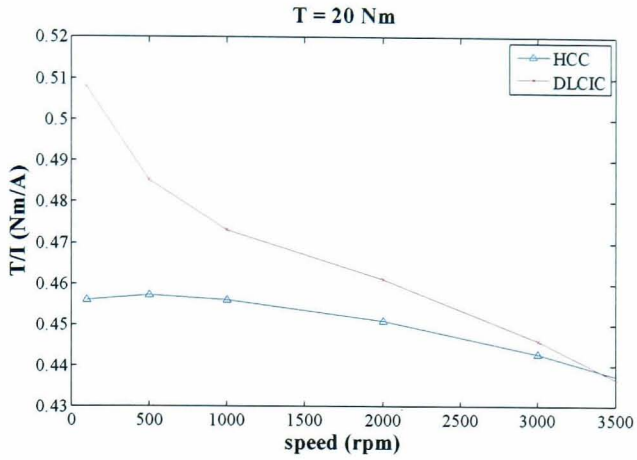
(d)

Figure 3.25: Comparison of average torque at T = 20, 15, 10 and 5 Nm

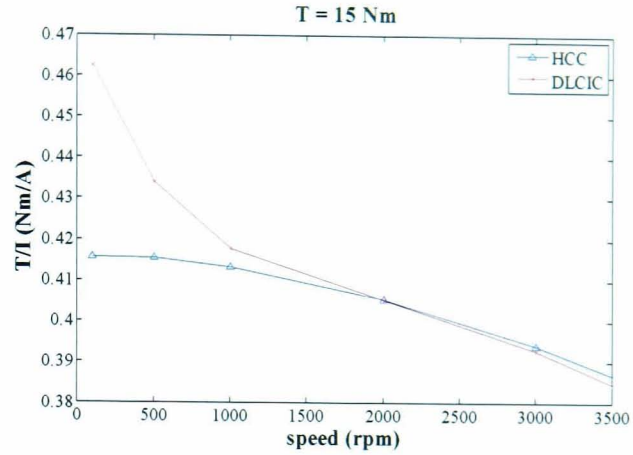
Torque per ampere (T/I)

The comparisons of torque per rms ampere between DLCIC and HCC at torque 20, 15, 10 and 5 Nm are shown in Figure 3.26. The torque per ampere characteristics at 20 and 15 Nm shown in Figure 3.26 (a) and (b) for the DLCIC and HCC are still similar. The intersection of the HCC and DLCIC curves is shifted from 3000 rpm in Figure 3.26 (a) to 2000 rpm in Figure 3.26 (b). The torque per ampere graphs of DLCIC in Figs. 3.26 (c) and (d) are different from those in Figure 3.26 (a) and (b).

In Figs. 3.26 (c) and (d), torque per ampere values of DLCIC in the 1000 - 2000 rpm speed range are lower than those of HCC. Over the speed range, the reason of the lower torque per ampere of DLCIC is that the rms phase current of DLCIC is slightly higher than that of HCC, as shown in Figure 3.27. However, the difference is very marginal.



(a)



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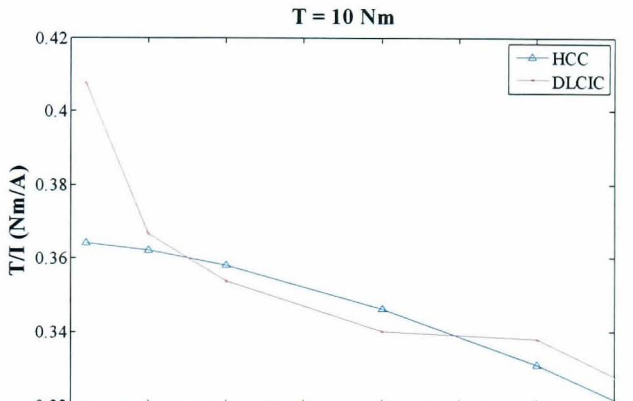

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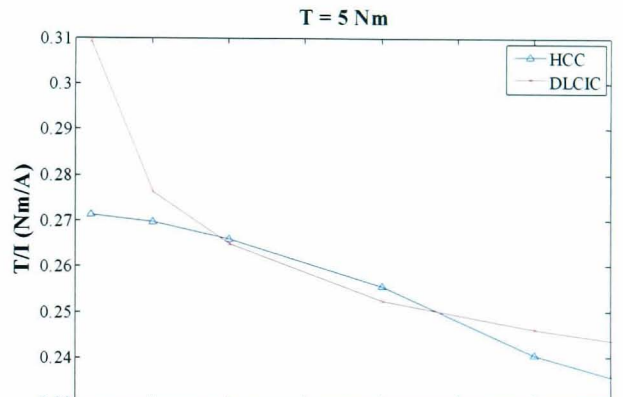
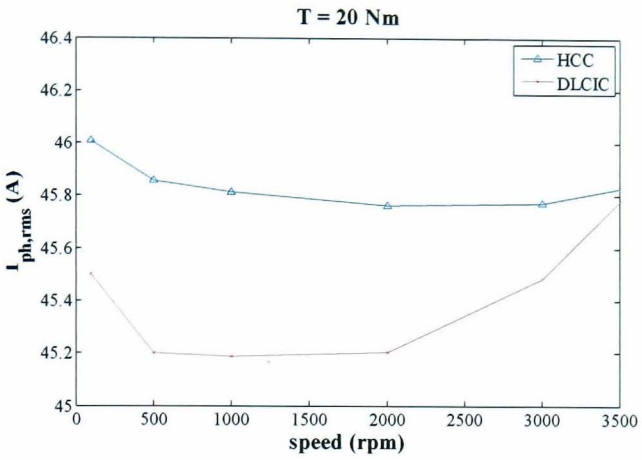


(d)

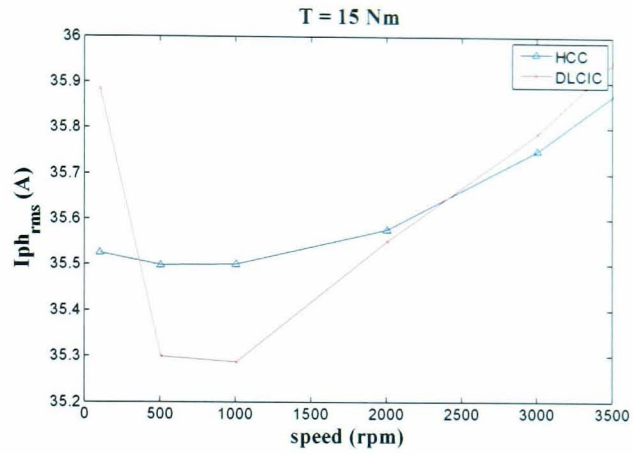
Figure 3.26: Comparison of torque per ampere at T = 20, 15, 10 and 5 Nm

The reason why the rms phase current of DLCIC at 5 Nm, 1000 rpm is higher than that of HCC is explained by comparing with the phase current and torque waveform of DLCIC and HCC. At this operation point, the rms phase current of DLCIC is slightly lower than that of HCC as shown in Figure 3.27 (b). As will be seen from Figs. 3.28 (a) and (b), the current of the HCC is maintained constant during the dwell period, which is longer than that of DLCIC. In contrast, the phase current of the DLCIC rises to a higher level initially due to the fact that the energy in the outgoing phase is transferred to the incoming phase. It then decreases slowly. However, the phase current of the DLCIC has a long tail after the turn-off angle due to the fact that the voltage applied to the outgoing phase is greater than -Vdc. The different phase current waveforms of DLCIC

and HCC result in a small difference in rms currents, which are dependent on torque and speed.



(a)



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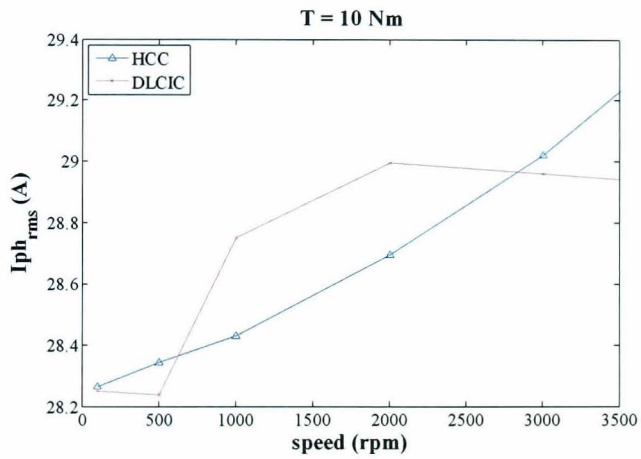
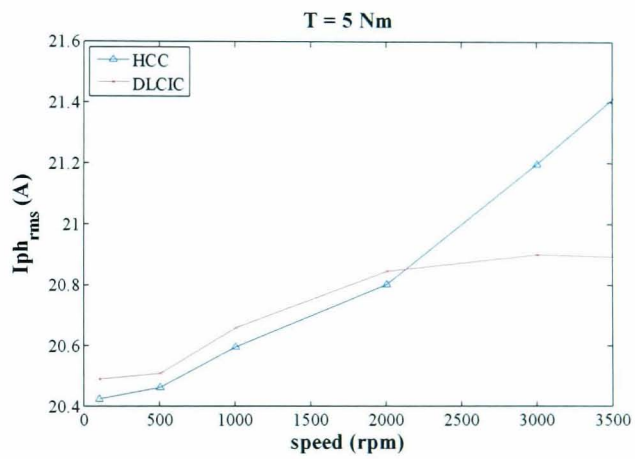
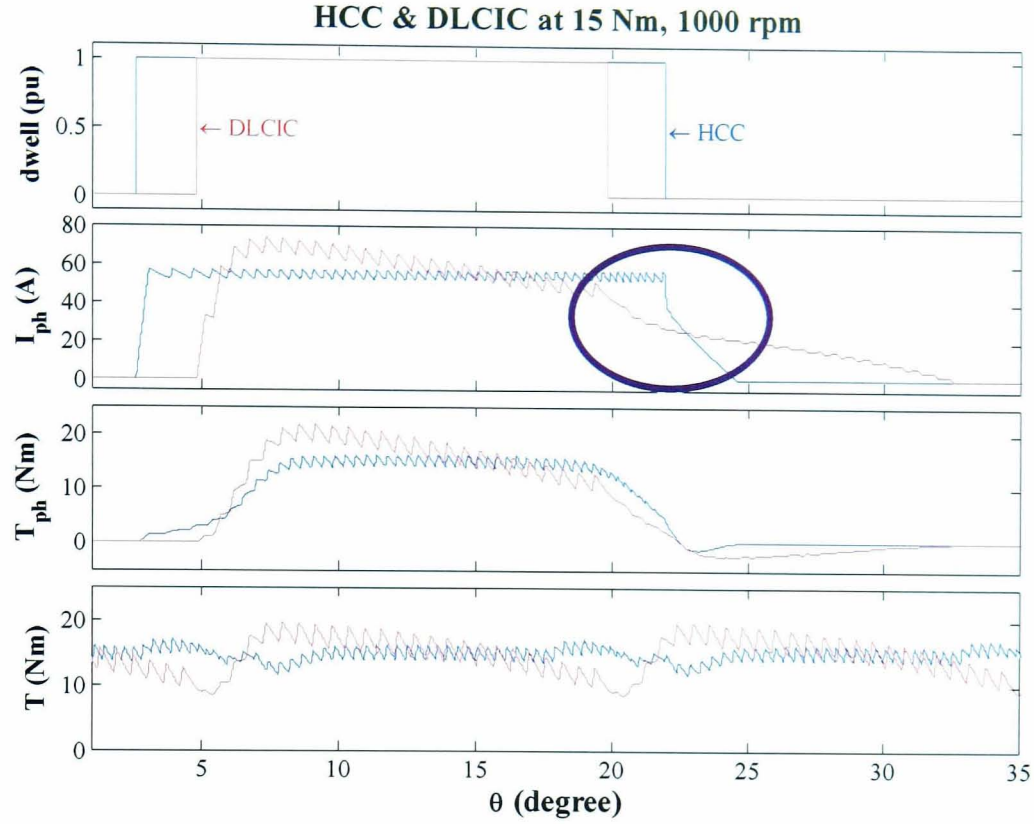


(c)

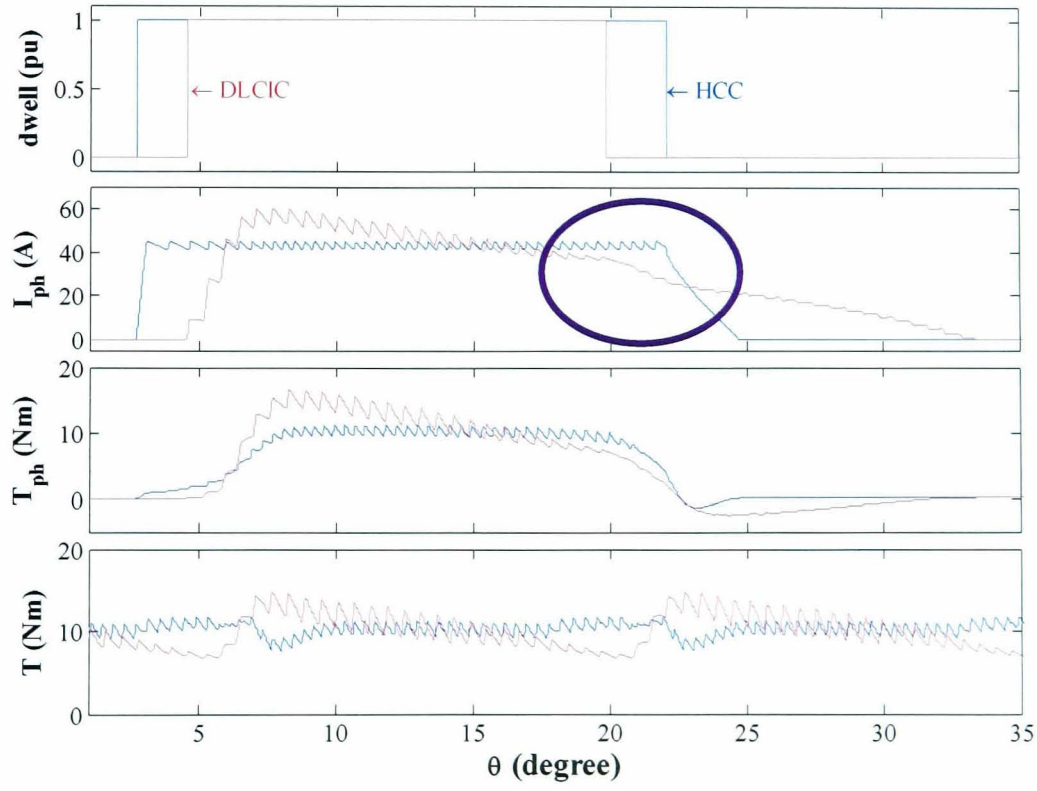


(d)

Figure 3.27: Comparison of rms phase current at T = 20, 15, 10 and 5 Nm



(a)



(b)

Figure 3.28: Comparison of phase current and torques of DLCIC and HCC at 15 and 10 Nm, 1000 rpm

The cause of the slow decrease in phase current after the turn-off angle is the low average terminal voltage resulting from the DLCIC switching process. For better illustration, the phase currents at 20 Nm and 5 Nm are employed to describe the variation of average terminal voltage in Figure 3.29.

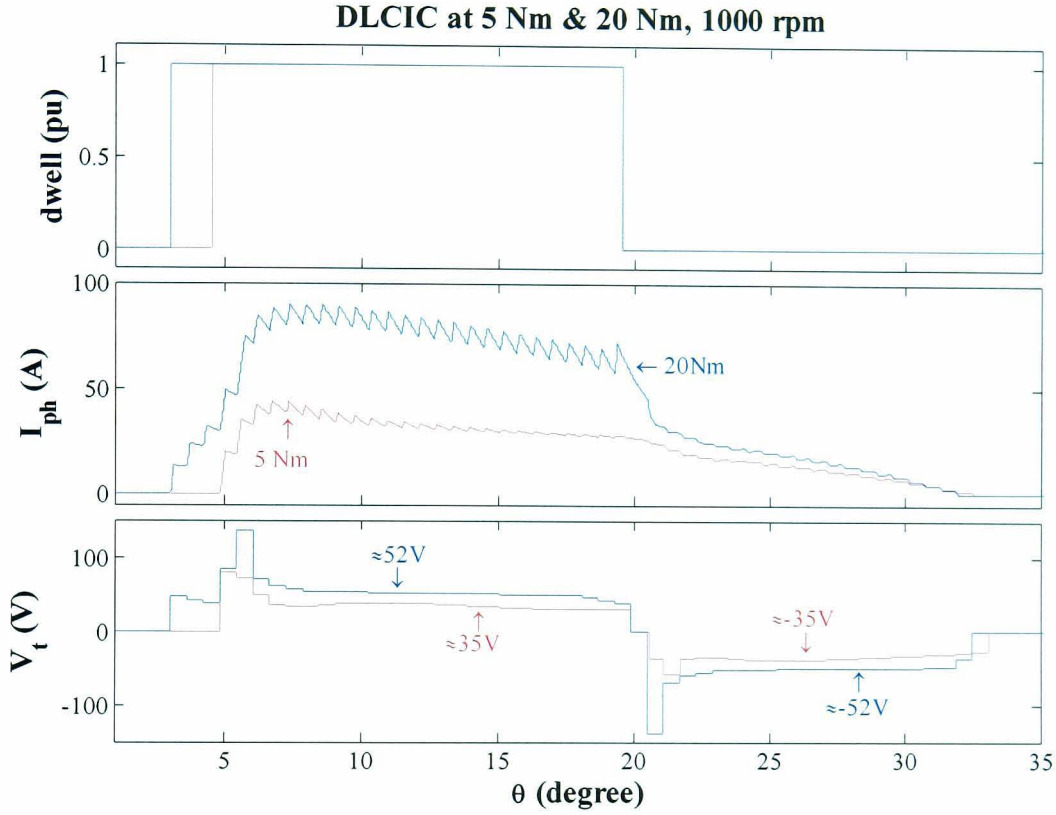


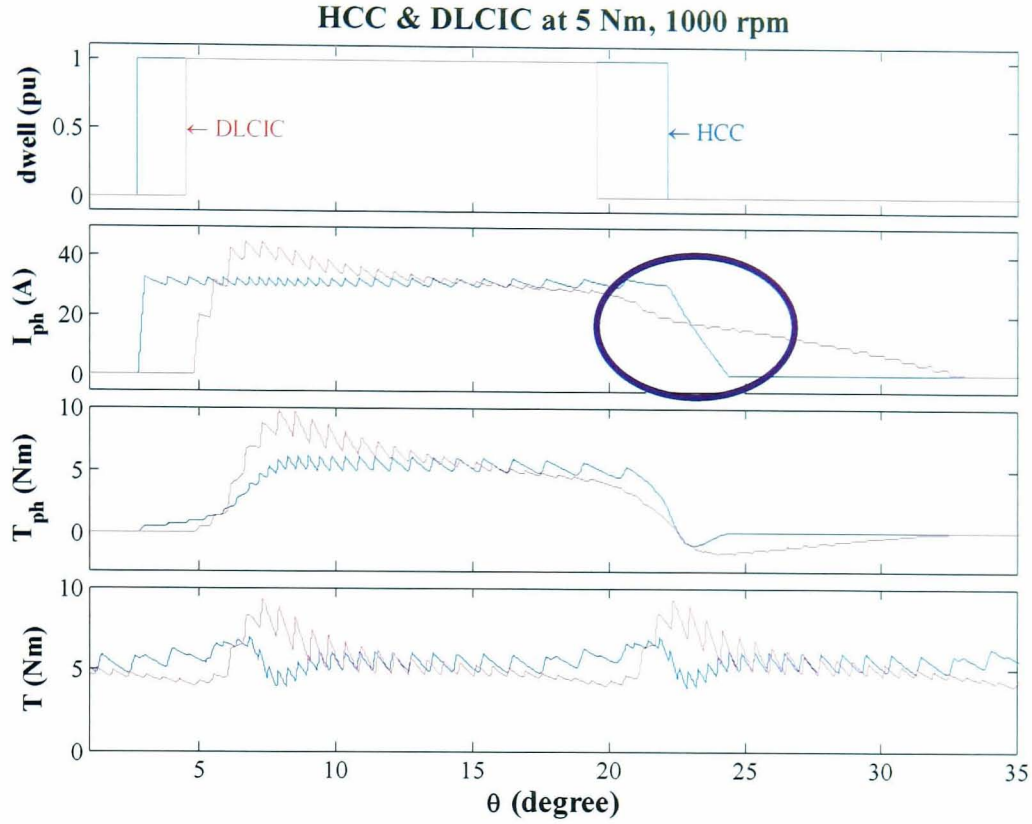
Figure 3.29: Average terminal voltage of DLCIC at 20 Nm and 5 Nm

The dwell signal, the phase current, and the average terminal voltage of each switching period of DLCIC at 20 Nm and 5 Nm are represented in Figure 3.29. The turn-off angles of both DLCIC signals are the same at, 19.5°. Although the phase current for 20 Nm torque at the turn-off angle is much higher that of 5 Nm, their turn-off periods, during which the phase current decay to zero are similar. The average terminal voltage applied to the outgoing phase for 5 Nm torque, of -35V, is less negative than that for the 20 Nm torque, -52V. This causes turn-off period for 5 Nm torque to be as long as or even longer than the turn-off period for 20 Nm torque, while the magnitudes of the phase currents are very close. The relatively long tail of the DLCIC at low torque is the cause of slightly higher rms current compared to the HCC.

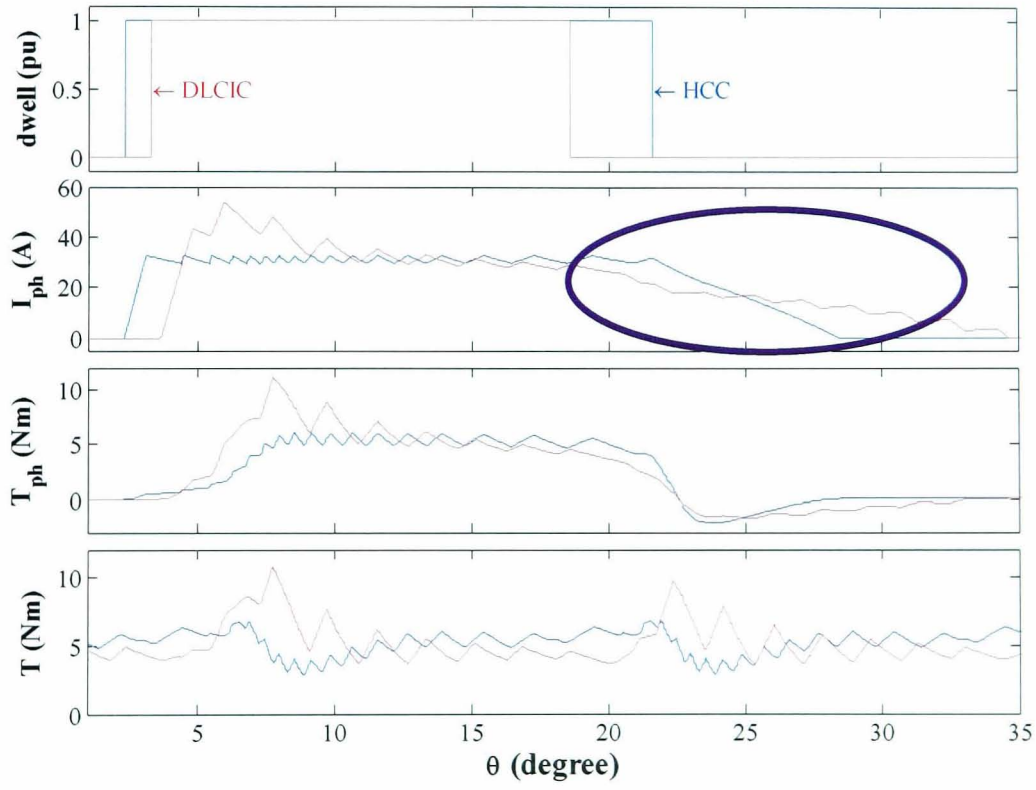
From Figure 3.27 (c) and (d), the rms phase currents of DLCIC become lower than that of HCC again at 3000 rpm. The comparisons of the phase currents between the HCC and DLCIC at 1000 and 3000 rpm of 5 Nm torque are shown in Figure 3.30. The phase current tail of HCC at 3000 rpm is much longer than that at 1000 rpm. Although the phase current tail of DLCIC at 3000 rpm is also longer than that at 1000 rpm, the turn-off time ratio between the DLCIC and HCC at 1000 rpm is definitely higher than the that at 3000 rpm. Hence, the rms phase current of HCC at 3000 rpm in Figure 3.27 (d) becomes higher than that of DLCIC. This is the reason for the higher torque per ampere of DLCIC than that of HCC at 3000 rpm of 10 and 5 Nm in Figure 3.26 (c) and (d).

For the peak-to-peak torques or torque ripples of DLCIC, although the demand torques are changed from 20 Nm to 15 Nm, 10 Nm, or 5 Nm, the torque ripples of DLCIC are still much higher than those of HCC, as shown in Figure 3.31. From previous figures such as Figure 3.28 and Figure 3.30, the torque of DLCIC is higher than that of HCC at the beginning of the dwell period. Since at the beginning of the dwell period, the incoming phase under DLCIC receives current from 2 sources, the outgoing phase current and the dc-link current, the phase current of DLCIC is higher than that of HCC. This results in the phase torque and the machine torque of DLCIC at the beginning of the dwell period higher than those of HCC.

At the end of the dwell period as shown in Figure 3.28 and Figure 3.30, the phase current and the torque of DLCIC are usually lower than those of HCC due to the effect of back emf and the overlap of the dwell periods. At the end of the dwell period, the back emf is higher than that at the beginning of the dwell period. Thus, the decreasing rate of the phase current is faster. The phase current and the machine torque of DLCIC at the end of dwell period are low due to a constant switching frequency and a constant average dc-link current imposed by the control scheme.



(a)



(b)

Figure 3.30: Comparison of phase current and torques of DLCIC and HCC at 1000 and 3000 rpm, 5 Nm

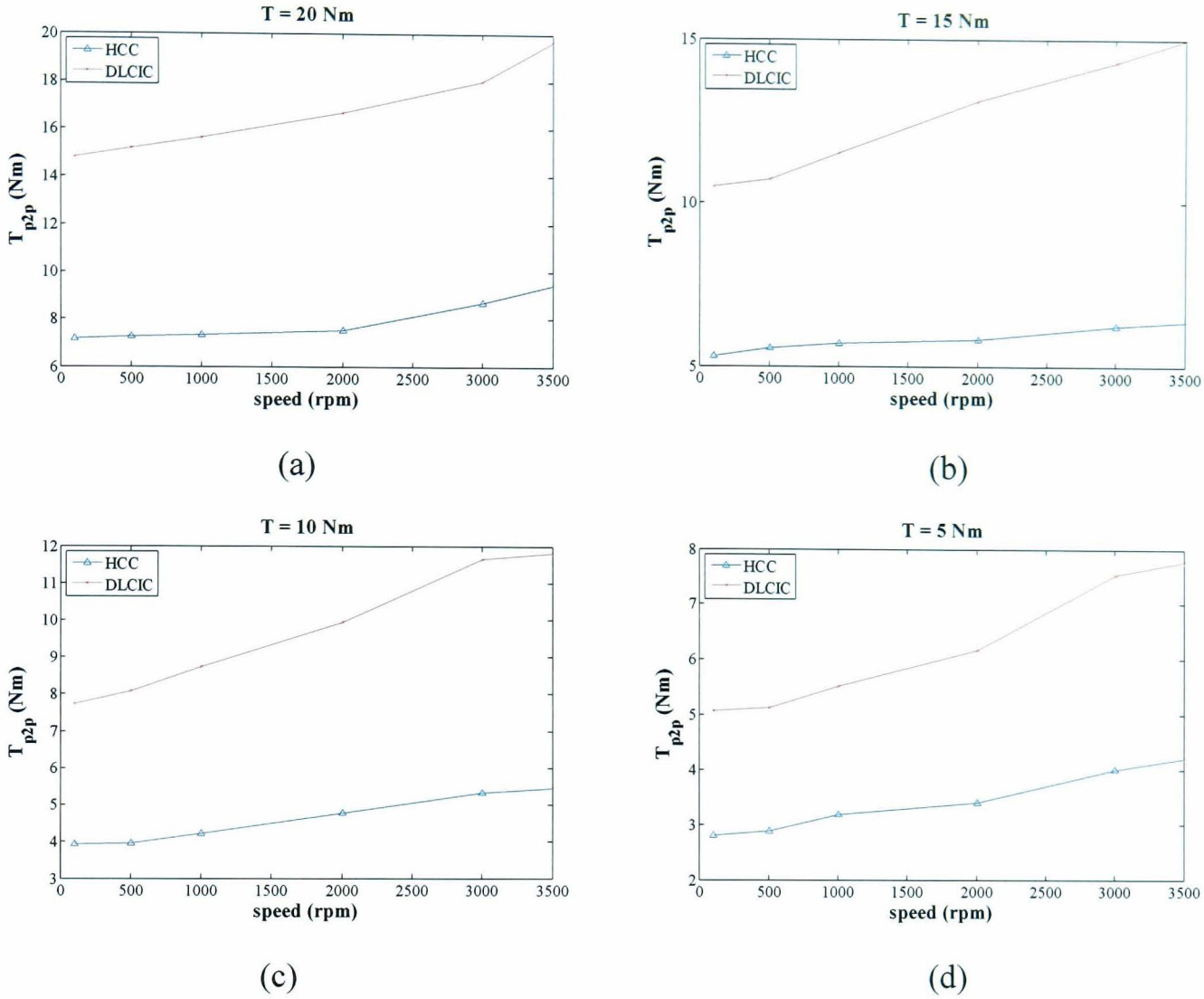


Figure 3.31: Comparison of peak-to-peak torque at T = 20, 15, 10 and 5 Nm

Most of DLCIC operations have a short overlapping period at the end of the dwell. The dc-link current has to feed 2 phase windings at the same time. Consequently the torque of the incoming phase is low while the torque of the outgoing phase is much reduced. Hence, the minimum of the machine torque of DLCIC is lower than that of HCC. From this explanation, the torque ripple of DLCIC is always higher than that of HCC.

3.5 Estimation of Optimal Turn-on and Turn-off Angles

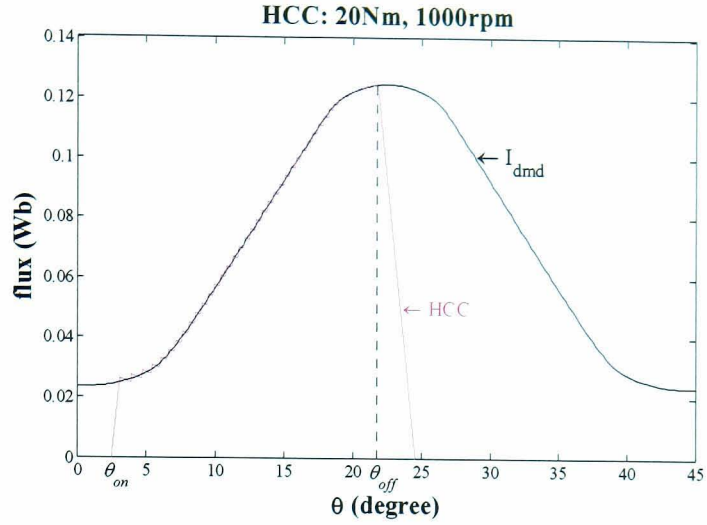
The optimal turn-on and turn-off angles of dc-link current integration control (DLCIC) are found by the numerical simulation in Section 3.3. However, the process to obtain

the optimal angles is tedious and consumes a long time. Hence, the estimation of the optimal turn-on and turn-off angles of DLCIC is required. In this section, the process to determine optimal turn-on and turn-off angles of DLCIC by analysing the flux trajectory [3.6] is proposed. Since under the DLCIC a constant average dc-link current is maintained, the control imposed by the DLCIC is neither the current control nor the voltage control. The fluxes from both Hysteresis Current Control (HCC) and Pulse Width Modulation Voltage Control (PWMVC) are analysed and compared with the flux from the DLCIC.

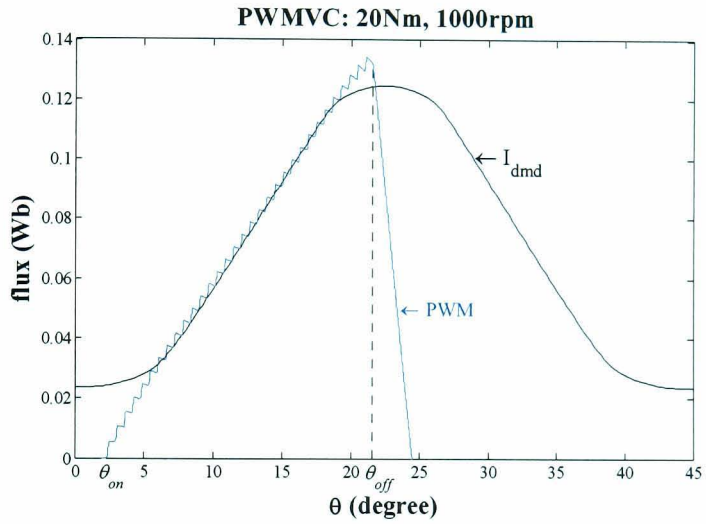
3.5.1 Optimal Turn-off Angles

To find the optimal turn-off angle of DLCIC, flux trajectory analysis described in [3.6] is utilised. For turn-off angle, two conditions of the phase current flux are of important [3.6]. First is the terminal voltage of the phase winding after the turn-off angle. Second is the flux linkage at the turn-off angle. Figure 3.32 presents the flux variations of HCC, PWMVC, and DLCIC for the same torque and speed demand. The flux of HCC rises rapidly from zero to the demand current flux and tracks along with it. The flux of PWMVC increases linearly due to constant voltage control.

After the turn-off angle, the fluxes of HCC and PWMVC speedily decrease since the negative supply voltage is applied to the phase winding. This generates the negative dc-link current which makes the voltage fluctuation in the dc-link capacitor. To reduce the voltage fluctuation, the DLCIC is aimed to eliminate the negative dc-link current. The current in the outgoing phase is synchronously released during the turn-on period of the incoming phase. The resulting flux of DLCIC after turn-off angle decreases slowly and is approximately parallel to the flux of the demand current (I_{dmd}) between fully aligned and unaligned positions. The terminal voltage of the phase winding is found by this paralleling flux condition. The DLCIC flux at the turn-off angle is assumed to equal the demand current flux.



(a)



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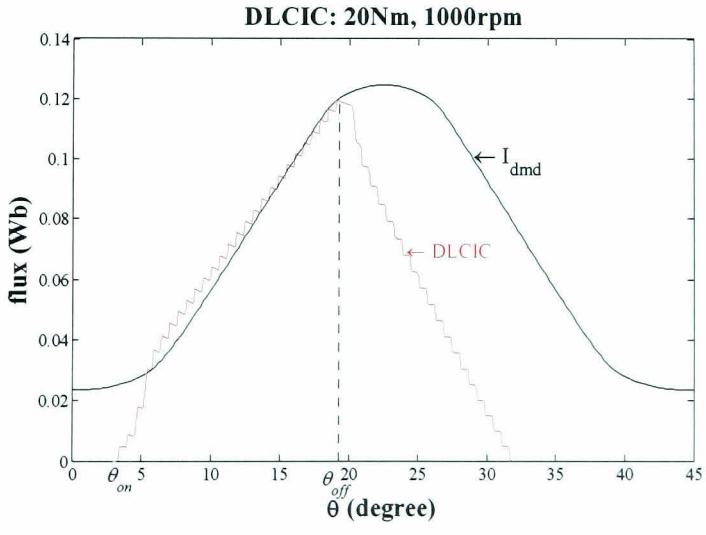


(c)

Figure 3.32: Flux of HCC, PWMVC, and DLCIC at 20Nm, 1000 rpm

Since the flux slope of DLCIC is assumed to be in parallel with the negative slope of the demand current flux, the duty cycle of DLCIC during the de-fluxing is assumed to equal to the negative duty cycle of PWMVC in (3.8), Section 3.2.2.

The relationship between the rotor position and flux linkage during the de-flux period [3.6] is expressed as

$$\theta_{de-flux} = \theta_{off} - \frac{\omega}{DV_{dc}}\left(\psi_{de-flux} - \psi_{off}\right) \tag{3.11}$$

where

$\theta_{de\text{-}flux}$ is the position of the machine during the de-fluxing period.

D is the duty cycle of PWMVC from (3.8).

$\psi_{de\text{-}flux}$ is the flux linkage at $\theta_{de\text{-}flux}$ during the de-fluxing period

ψ_{off} is the flux linkage at turn-off angle

To find the optimal turn-off angle with the maximum average torque in [3.6], the aligned position is set to zero degree and the flux linkage at the aligned position is equal to $x \cdot \psi_{off}$ when x is around $1/\sqrt{2}$ to $2/3$, as stated in Section 3.2.1. From (3.11), flux linkage at the turn-off angle is

$$\psi_{off} = \frac{\theta_{off} \cdot DV_{dc}}{\omega \cdot (x-1)} \tag{3.12}$$

This is from the condition that the flux linkage at the turn-off angle of DLCIC is approximately equal to the flux linkage of the demand current, where the turn-off angle is obtained from

$$\psi_{off} = \frac{I_{dmd}}{R_a - \dfrac{R_{ua} \cdot \theta_{off}}{\theta_m}} \tag{3.13}$$

where

R_a is the inverse of the inductance at the aligned position, $\frac{1}{L_a}$.

R_{ua} is the inverse of the inductance at the un-aligned position minus the inverse of the inductance at the aligned position, $\frac{1}{L_u} - \frac{1}{L_a}$.

θ_m is the corner point of the inductance curve.

I_{dmd} is the demand current.

Using (3.12) and (3.13), the optimal turn-off angle can be written as

$$\theta_{off} = -\frac{\theta_m}{2}\left(-\frac{R_a}{R_{ua}} + \sqrt{\left(\frac{R_a}{R_{ua}}\right)^2 + 4\left(\frac{I_{dmd}(1-x)\omega}{DV_{dc}\cdot R_{ua}\theta_m}\right)}\right) \tag{3.14}$$

Then, the turn-off angle in (3.14) is converted from the position reference system in which the aligned position is defined at zero degree to the position reference system in which the unaligned position is set to zero degree. Figure 3.33 compares the variation of the numerical optimal turn-off angle and the analytical optimal turn-off angle at the rated torque with speed.

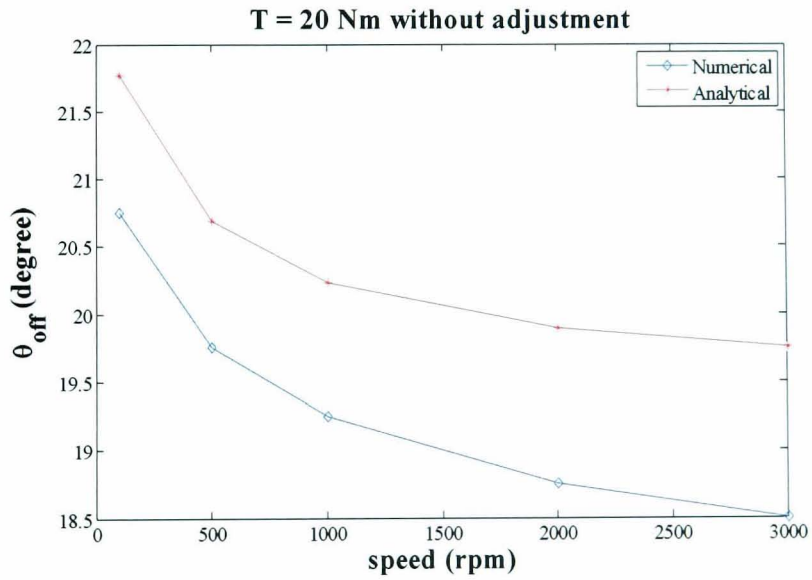


Figure 3.33: The comparison of the numerical and the analytical turn-off angles without adjustment

The trend of the analytical and numerical optimal turn-off angle are very close, but a gap exists. This is because the period in which the outgoing phase current is freewheeling until the incoming phase current becomes after behind the turn-off angle is not considered. Hence, the optimal turn-off angles from (3.14) should be advanced. The advance angle is calculated from the analytical optimal turn-off angle in (3.14) at 3000 rpm, 20 Nm since the dc current demand is maximum at the rated torque and 3000 rpm is the highest speed. The analytical turn-off angle is advanced around 5 - 6 %.

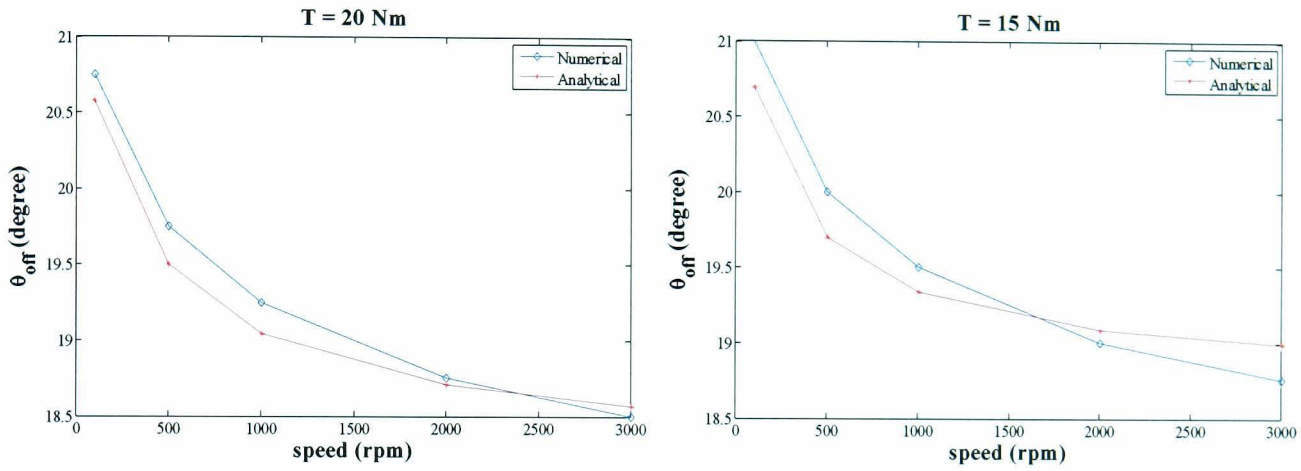


Figure 3.34: The comparison between the numerical and analytical turn-off angles

Figure 3.34 compares the variations of the numerical turn-off angle and analytical turn-off angle after adjustment with speed for 20, 15, 10 and 5 Nm. The analytical optimal

turn-off angles after adjustment are closed to the numerical optimal turn-off angles and can be used for the optimal analytical turn-off angles.

3.5.2 Optimal Turn-on Angles

In previous section, the optimal turn-off angles are found from the de-fluxing curve. However, this cannot be applied to determine the optimal turn-on angle. The optimal turn-on angles of DLCIC are found from the comparison of the optimal turn-on angles of HCC with that of the DLCIC obtained through numerical simulations. As can be seen from Figure 3.35, the slope of the optimal turn-on angle variation of DLCIC and HCC at 20 Nm is almost parallel. The optimal turn-on angles for both decrease with speed, while the optimal turn-on angles of PWMVC are constant.

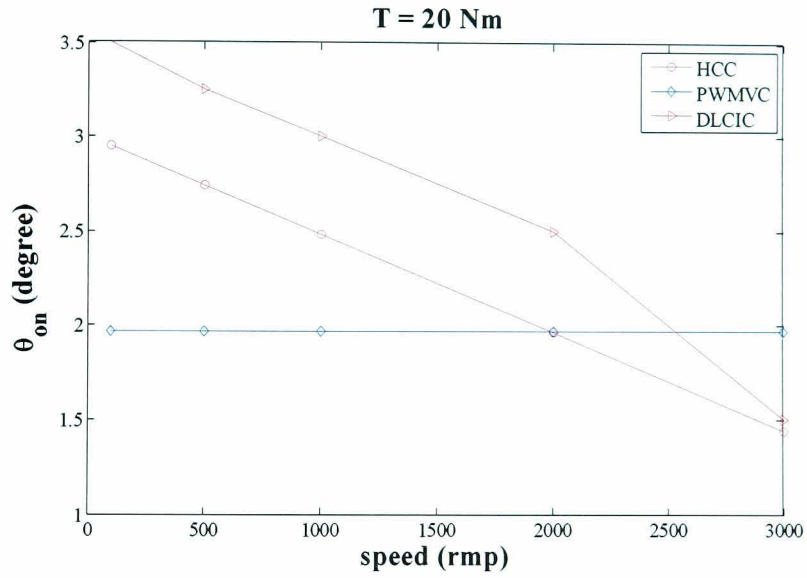
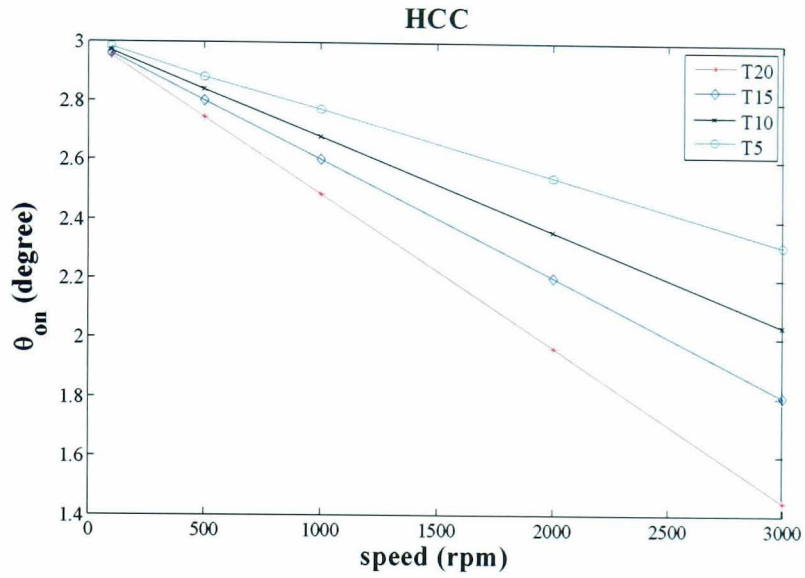


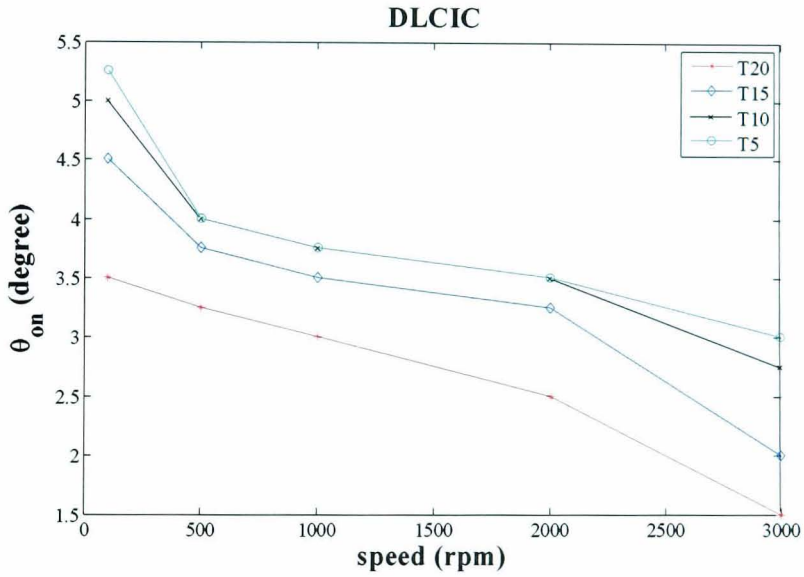
Figure 3.35: Variation of optimal turn-on angle of HCC, PWMVC and DLCIC at 20 Nm

The variations of the optimal turn-on angles of HCC and DLCIC with the speeds at 20, 15, 10 and 5 Nm are presented in Figure 3.36. The slope of the optimal turn-on angle of HCC increases with torque. In contrast, the slope of the optimal angles of DLCIC for a given torque are not constant. Since the turn-on angle has less influence on the machine average torque, the slope of optimal turn-on angle variation with speed at 20 Nm is employed to estimate the optimal turn-on angle of the DLCIC for any torque. This is

because the average slope of the optimal turn angle variation with the speed for the DLCIC at different torque is virtually constant.



(a)



(b)

Figure 3.36: Variation of turn-on angle of HCC and DLCIC at 20, 15, 10, and 5 Nm

To fully determine the optimal turn-on angle variations of the DLCIC with speed and torque, the optimal turn-on angle variations of HCC, PWMVC, and DLCIC with torque are compared at 3000 rpm. Since 3000 rpm is the maximum operation speed of DLCIC, its optimal turn-on angle is more sensitive. Figure 3.37 shows the numerical optimal

turn-on angle of DLCIC is between those of HCC and PWMVC at 3000 rpm. This is because the operation of DLCIC is neither current control nor voltage control. Consequently, the analytical optimal turn-on angles of DLCIC at 3000 rpm are estimated as the average of those of the HCC and PWMVC. The resulting analytical optimal turn-on angle variations are compared with the numerically simulated values in Figure 3.38.

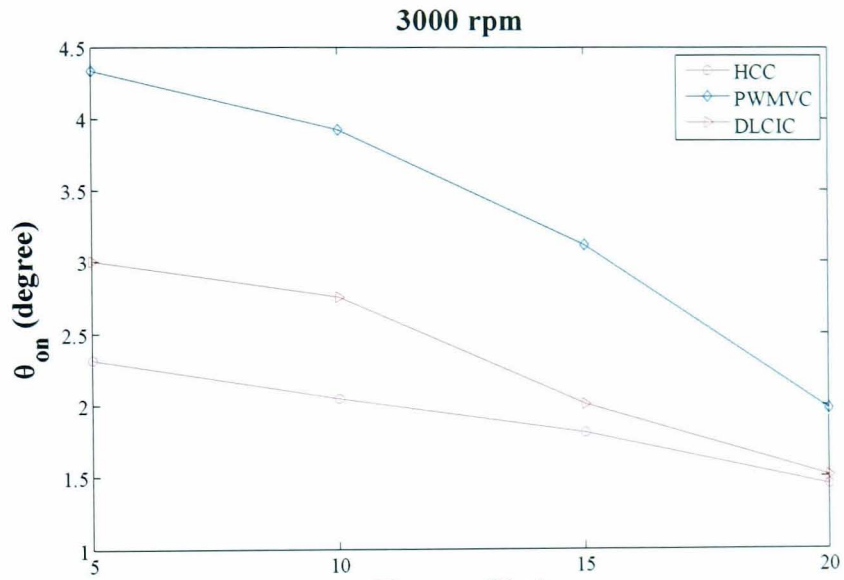
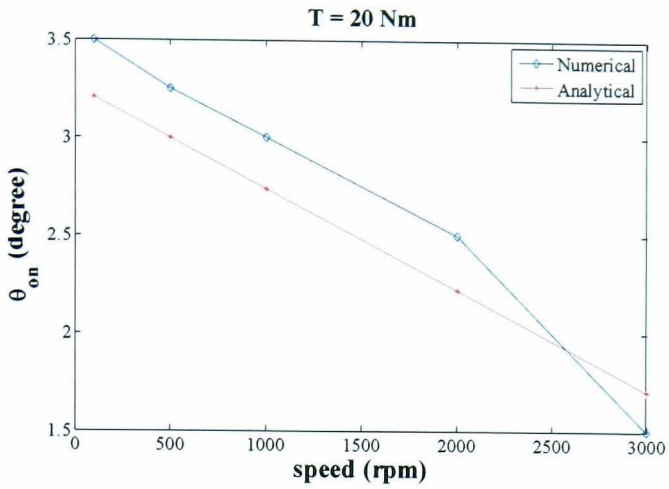
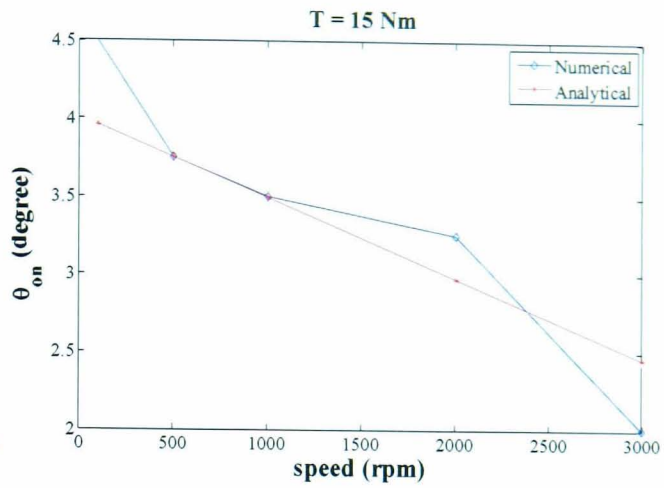


Figure 3.37: Variation of turn-on angle with torque at 3000 rpm



(a)



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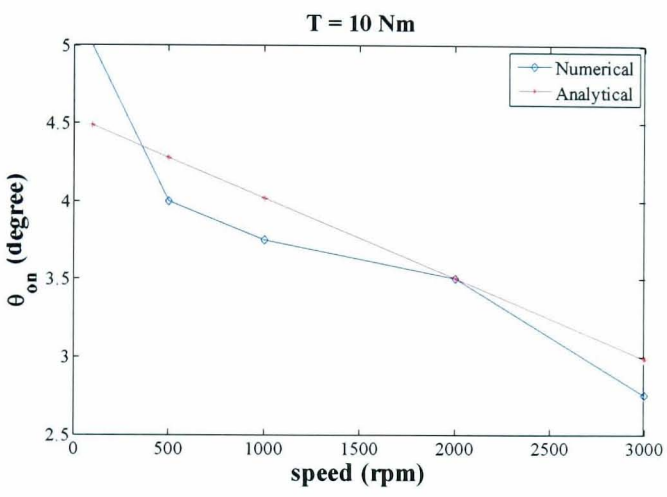

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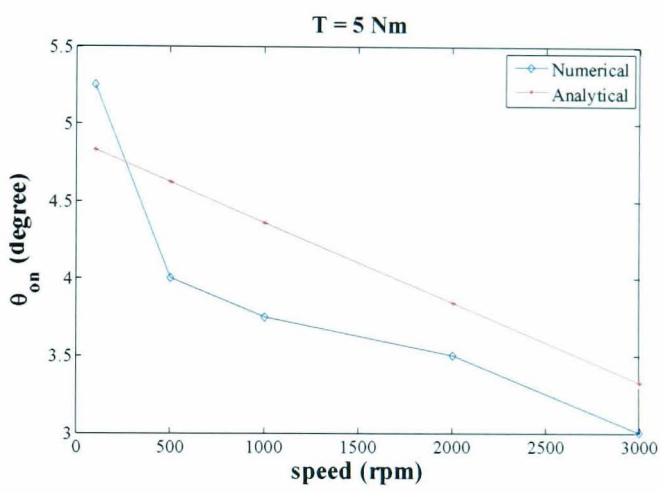
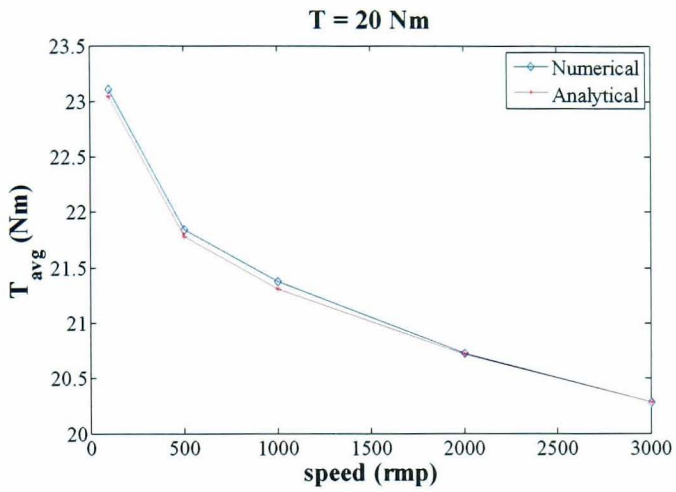


(d)

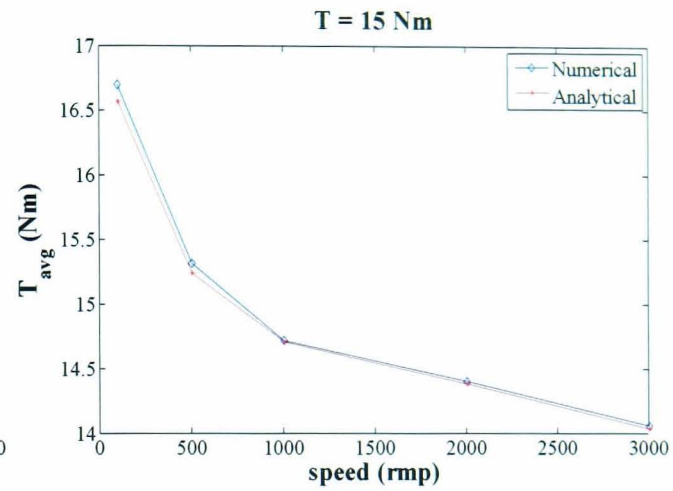
Figure 3.38: The comparison between the numerical and analytical turn-on angles

As is evident from Figure 3.38, the analytical and the numerical optimal turn-on angles are close. The comparisons of the average torque and torque per ampere which are obtained using the numerical and analytical turn-on and turn-off angles are given in Figure 3.39 and Figure 3.40. The torque per ampere values with the analytical optimal turn-on and turn-off angles over the speed range of 2000 - 3000 rpm in Figure 3.40 (a) are slightly higher than those with the numerical optimal turn-on and turn-off angles. Since the analytical optimal turn-on angle at 20 Nm, 2000 rpm is smaller than that of the numerical optimal turn-on angle, the dwell period with the analytical optimal turn-on and turn-off angles is longer than that of the numerical ones. Consequently, the rms phase current with the analytical angles is higher than that with the numerical angles.

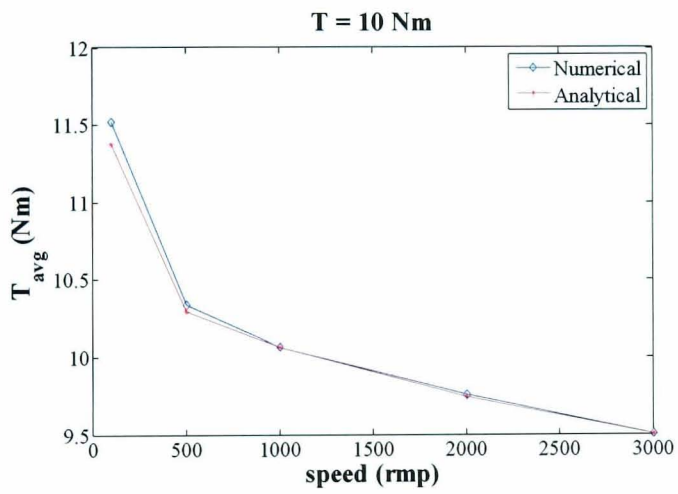
Nevertheless, the difference between two is very small. Thus, the analytical optimum turn-on and turn-off angles can be used to implement the DLCIC.



(a)



(b)



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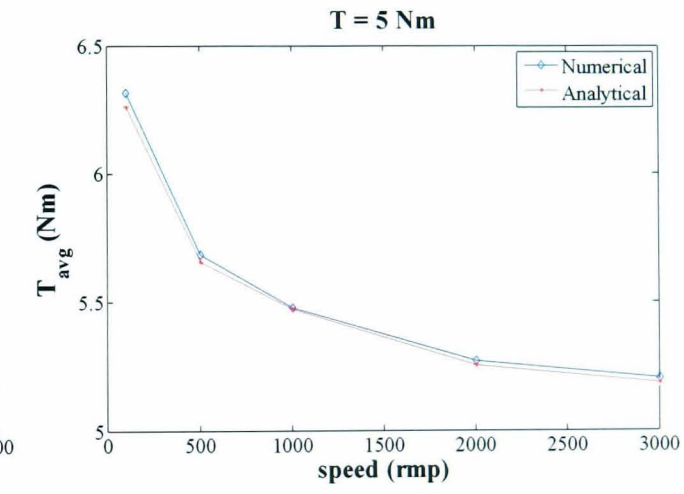


(d)

Figure 3.39: Comparison of average torque of numerical and analytical optimal angles

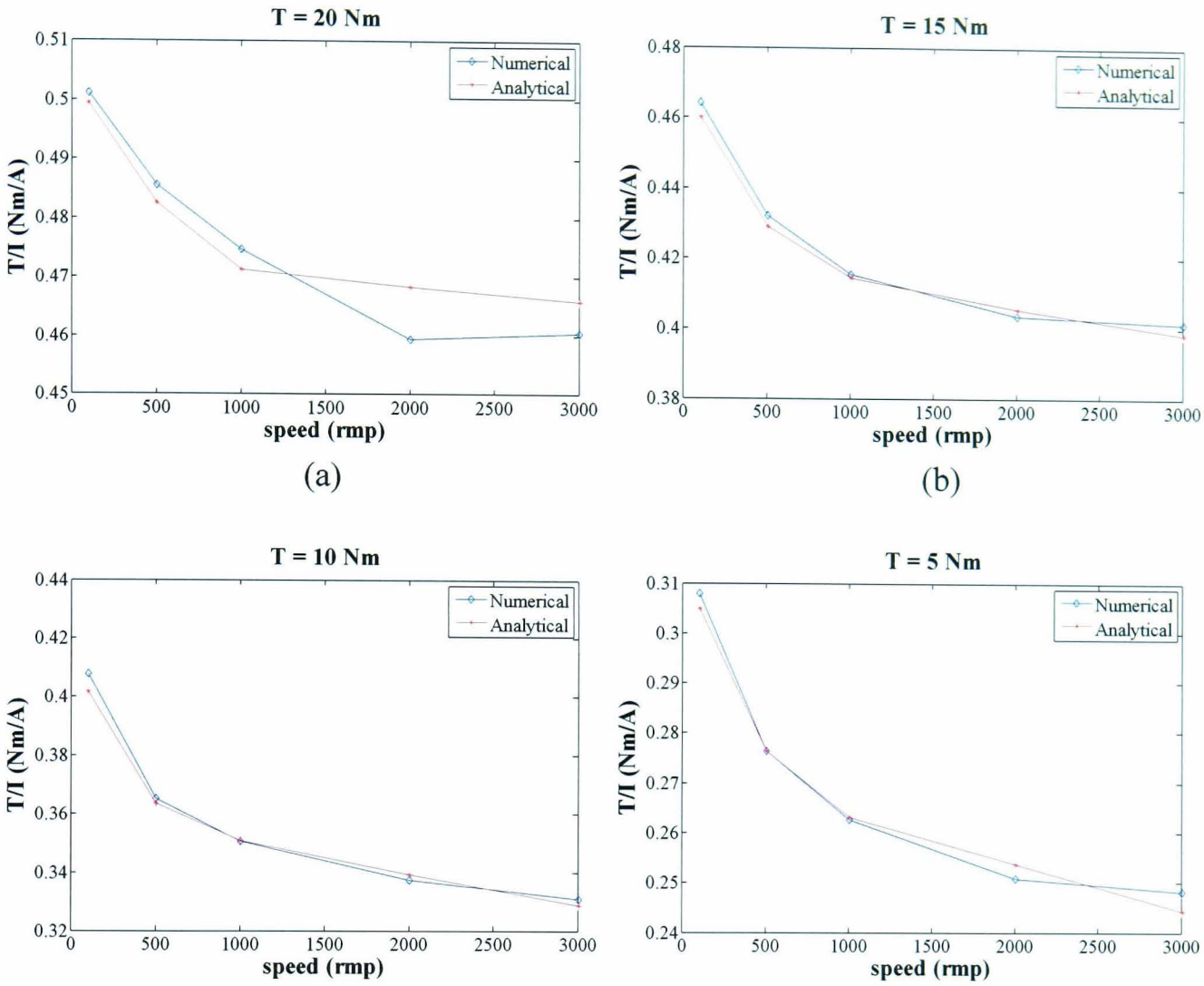


Figure 3.40: Comparison of torque per ampere of numerical and analytical optimal angles of DLCIC

3.6 Conclusion

In this chapter, the optimal turn-on and turn-off angles of the DLCIC are firstly found by extensive numerical simulation and the operation speed range of DLCIC is defined. The operational characteristics of the DLCIC with optimal turn-on and turn-off angles are analysed, and compared with HCC. Since the process of finding the numeric optimal angles of DLCIC is tedious and time consuming, the estimation of the optimal turn-on and turn-off angle is established. To estimate the optimal turn-off angles, the flux linkages from HCC, PWMVC and DLCIC are compared and analysed. The

optimal turn-on angles of DLCIC are estimated from the optimal turn-on angles of HCC at the rated torque. After the analytical optimal turn-on and turn-off are generated, the average torque and the torque per ampere from them are compared with those obtained with the numerical optimal turn-on and turn-off angles. The average torque and the torque per ampere from the analytical and numerical optimal turn-on and turn-off angles are closed. Hence, the analytical optimal turn-on and turn-off angles can be used in the speed range below 3000 rpm.

3.7 Reference

[3.1] B. K. Bose, T. J. E. Miller, P. M. Szczesny, and W. H. Bicknell, "Microcomputer Control of Switched Reluctance Motor," *Industry Applications, IEEE Transactions on,* vol. IA-22, pp. 708-715, 1986.

[3.2] R. C. Becerra, M. Ehsani, and T. J. E. Miller, "Commutation of SR motors," *Power Electronics, IEEE Transactions on,* vol. 8, pp. 257-263, 1993.

[3.3] P. C. Kjaer, P. Nielsen, L. Andersen, and F. Blaabjerg, "A new energy optimizing control strategy for switched reluctance motors," *Industry Applications, IEEE Transactions on,* vol. 31, pp. 1088-1095, 1995.

[3.4] C. Mademlis and I. Kioskeridis, "Performance optimization in switched reluctance motor drives with online commutation angle control," *Energy Conversion, IEEE Transactions on,* vol. 18, pp. 448-457, 2003.

[3.5] I. Kioskeridis and C. Mademlis, "Maximum efficiency in single-pulse controlled switched reluctance motor drives," *Energy Conversion, IEEE Transactions on,* vol. 20, pp. 809-817, 2005.

[3.6] J. J. Gribble, P. C. Kjaer, and T. J. E. Miller, "Optimal commutation in average torque control of switched reluctance motors," *Electric Power Applications, IEE Proceedings -,* vol. 146, pp. 2-10, 1999.

[3.7] J. J. Gribble, P. C. Kjaer, C. Cossar, and T. J. E. Miller, "Optimal commutation angles for current controlled switched reluctance motors," in *Power Electronics and Variable Speed Drives, 1996. Sixth International Conference on (Conf. Publ. No. 429)*, 1996, pp. 87-92.

[3.8] S. Jong-yun, C. Hyun-Rok, Y. Hyong-yeol, S. Jung-Chul, K. Kwang-Heon, L. Young-Cheol, and J. Do-Hyun, "Speed control method for switched reluctance motor drive using self-tuning of switching angle," in *Industrial Electronics, 2001. Proceedings. ISIE 2001. IEEE International Symposium on*, 2001, pp. 811-815 vol.2.

Chapter 4

Filter Design

4.1 Introduction

In order to attenuate the ac harmonics from the switched reluctance (SR) drive and to isolate the disturbance from the dc supply network, it is necessary to include a low pass filter between the dc supply (V_{dc}) and the converter stage. The primary objective of the input filter is to dampen the ripples of the capacitor voltage and the ripples of the input current (I_L). For this purpose, many designs employ a low cut-off frequency which is composed of a large inductor and capacitor [4.3]. The cut-off frequency is generally designed to be less than the ripple frequency by around 10 times [4.1].

Nonetheless, the filter may induce significant performance degradations of the drive system [4.2-4.4]. The interaction between the input filter and the constant power load, which behaves dynamically as a negative impedance, may also lead to the system instability [4.5-4.14]. The stability equation, which governs the values of the capacitor and inductor, is found from the second order transfer function between the average of

the capacitor voltage and the dc supply voltage. The power quality lines for the dc-link capacitor and the input inductor are constructed from the spectrum of the capacitor voltage and the input current plotted against military (MIL) standards, [4.15-4.16]. The capacitance and the inductance in the filters are chosen from a crossing point between the stability lines and the power quality lines for a given damper resistance. The lightest weight of the input filter component set, which consists of the input resistor, input inductor and dc-link capacitor, is chosen.

In this chapter, two filter designs are considered for comparison. The first filter is designed for the combined operation of dc-link current integration control (DLCIC) and hysteresis current control (HCC). In the low speed range (i.e., 100 - 3000 rpm), DLCIC is employed. Above 3000 rpm, HCC is used. The second filter is designed for HCC over the entire operation range. One of the benefits from the proposed method is a much lighter input filter, compared to that of HCC. In this chapter, the supply side low pass filter is designed. Since the major concerns are to satisfy the stability and the power quality criteria, the cut-off frequency is not directly specified within the filter design.

4.2 Design Scenario Selection

The RLC filters is sited between the dc supply (V_{dc}) and the H-bridge converter, as shown in Fig. 4.1.

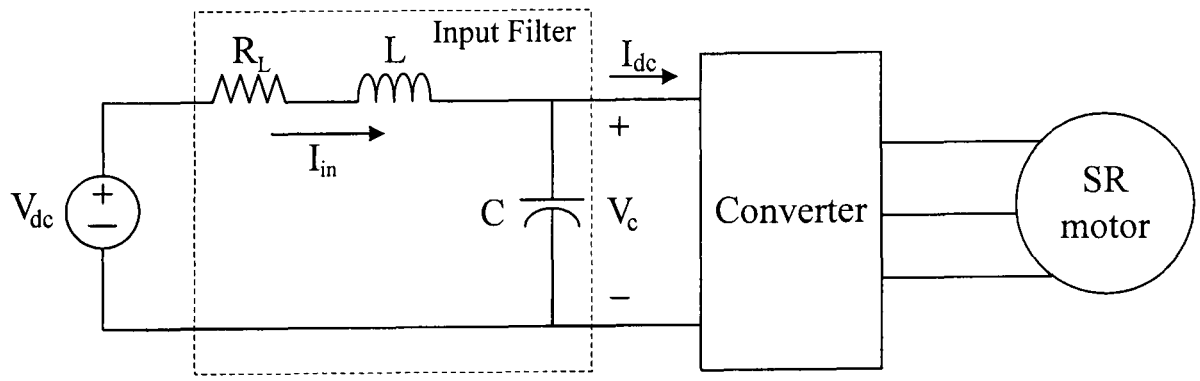


Figure 4.1: RLC low pass filter with converter as machine drive

The dc supply (V_{dc}) is assumed to be an ideal voltage source. However, any loss and parasitic inductance in the cable can be lumped input resistance (R_L) and input inductance (L).

The first process of the filter design is to chose the design scenario. Since the total harmonic distortion (THD) is used as a key factor for the filter design in [4.17-4.19], it has been adopted to find the design scenario where the peak to peak of the dc-link capacitor voltage is at a maximum. As will became apparent in the experimental chapter, it is not possible to directly measure the dc-link current between the dc-link capacitors and the converter in hardware. Therefore, in this thesis, THD is generated from the simulated dc-link current. The THD of the dc-link current analysed by Fast Fourier Transform (FFT) and THD is found from (4.1),

$$THD = \frac{\sqrt{\sum (H_{ac}^2)}}{H_{dc}} \tag{4.1}$$

where H_{ac} is the ac harmonic spectrum of the dc-link current and H_{dc} is the dc harmonic (fundamental harmonic) of the dc-link current. Thus, the fluctuation is increased with THD. This equation shows that the ripple of the dc-link capacitor voltage increases with THD since the sum of the ac harmonic is increased.

At the same speed and same demand torque, the peak to peak voltages of the dc-link capacitor using the DLCIC technique is much lower than when using the HCC technique. Thus, in the combined operation, when DLCIC is operated at the speed 100 -3000 rpm and above 3000 rpm, HCC is performed, the dc-link current from HCC at 3000 rpm is used to produce THD to find the design scenario. In the HCC operation, the dc-link current of HCC is definitely used to find the design scenario.

As the demand phase current of the rated demand torque is highest among those of other demand torques, the dc-link currents at the rated demand torque are analysed here. The peak to peak of the dc-link capacitor voltage (V_C) and the input current (I_L) are maximum at the rated demand torque.

Figure 4.2 presents THD of the dc-link current of the hysteresis current control (HCC). As previous stated, for the combined operation, the maximum THD of the combined operation is chosen from THD of HCC at the speed 3000 rpm. For the HCC operation, the HCC is operated entirely all speed range. Hence, the maximum of THD has been chosen at 100 rpm, which is the lowest speed. After the design scenarios are chosen, the dc-link currents from both scenarios are employed to calculate the stability and power quality for a given set of the filter parameters.

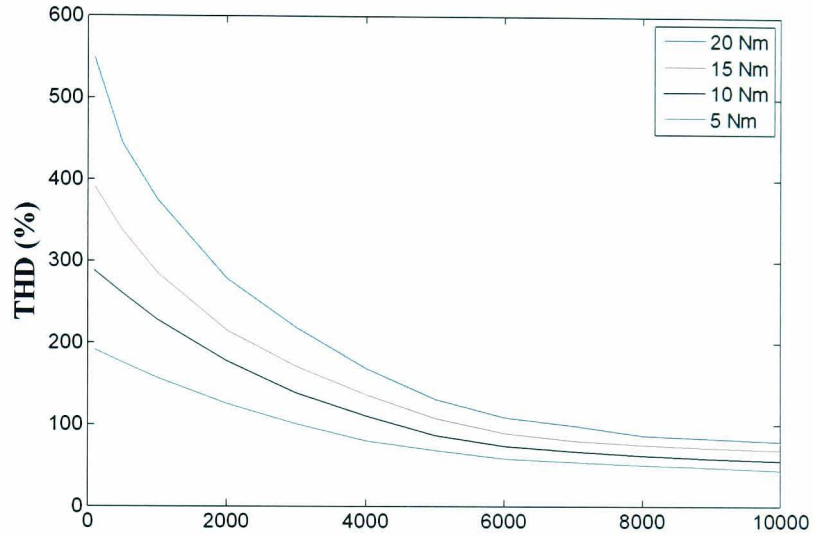


Figure 4.2: THD of dc-link current from HCC at rated torque

4.3 Stability and Power Quality

In this section, the processes to calculate the input inductance and the dc-link capacitance of the input filter from the stability and the power quality are described. In order to ensure satisfactory operation of the filter under all condition it is necessary to determine the stability limit for a given combination of filter parameters. There are a number of techniques for predicting stability of such second-order system, including Nyquist criterion [4.10], impedance/admittace method [4.31-4.32], Bode plot [4.30], and Root Locus [4.23]. In this thesis a method based on feedback linearization technique from [4.5] was adopted.

4.3.1 Stability

When the converter operates under tightly regulated feedback control at a certain speed and torque, the machine acts as a constant power load. This causes the negative impedance at the input terminal of the converter [4.5, 4.9, 4.20-4.21]. Figure 4.3 displays the circuit diagram of the input filter and the machine load which acts as a constant power load. The current source (i_0) represents as a constant power load. The derivative of the load power is zero as

$$dP = idv + vdi = 0 \tag{4.2}$$

where P is the power of the load, i is the load current and v is the load voltage.

The small signal impedance of the constant power load is found from

$$Z_P = \frac{dv}{di} = -\frac{v}{i} \tag{4.3}$$

where Z_P is the impedance of the constant power load.

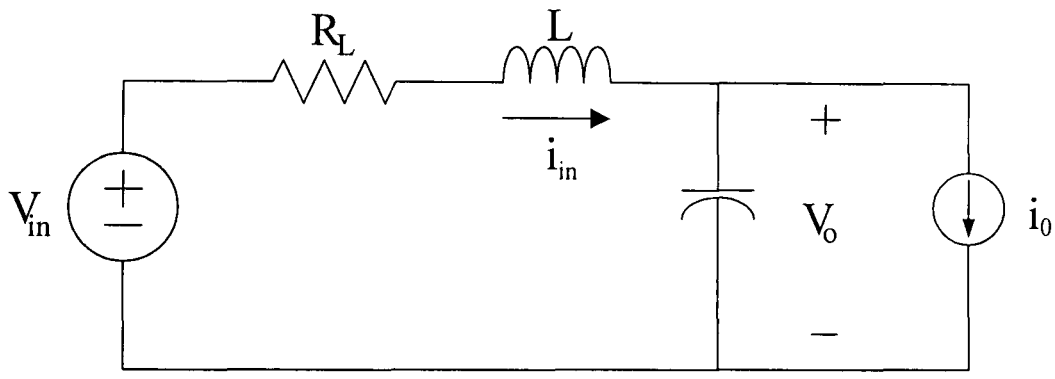


Figure 4.3: Input filter circuit diagram with constant power load

When the machine operates at a constant torque and speed, the machine power is shown as

$$P = V_0 i_0 \tag{4.4}$$

where V_0 is the average input voltage of the converter and i_0 is the average current drawn by the converter.

From (4.3) and (4.4), the impedance of the constant power load is rewritten as

$$Z_P = -\frac{V_0}{i_0} = -\frac{V_0^2}{P} \tag{4.5}$$

From Figure 4.3, the transfer function is expressed by,

$$\frac{V_0}{V_{dc}} = \frac{1/LC}{s^2 + \left(\frac{R_L}{L} - \frac{P}{V_0^2 C}\right)s + \left(\frac{1}{LC} - \frac{PR_L}{V_0^2 LC}\right)} \tag{4.6}$$

where

V_{dc} is the dc supply voltage.

R_L is the resistance of the low pass input filter.

L is the inductance of the low pass input filter.

C is the dc-link capacitance of the input filter.

The second order system equation is represented as

$$\frac{X(s)}{U(s)} = \frac{\omega_n^2}{s^2 + 2\varsigma\omega_n s + \omega_n^2} \tag{4.7}$$

where

$X(s)$ is the response of the system.

$U(s)$ is the input of the system.

ω_n is the natural frequency.

ζ is the damping ratio of the system.

The damping ratio and the natural frequency can now be expressed by combining (4.6) and (4.7), as

$$2\varsigma\omega_n = \frac{R_L}{L} - \frac{P}{V_0^2 C} \tag{4.8}$$

and

$$\omega_n^2 = \frac{1}{LC}\left(1 - \frac{PR_L}{V_0^2}\right) \tag{4.9}$$

Then, from (4.8) and (4.9), the dc-link capacitance variation with the inductance to satisfy a required damping for a given damping resistance (R_L), load power (P_0) and capacitor voltage (V_0) is described as,

$$\frac{R_L^2}{L^2}C^2 - \left[\frac{2R_L P}{LV_0^2} + \frac{4\varsigma^2}{L}\left(1 - \frac{PR_L}{V_0^2}\right)\right]C + \frac{P^2}{V_0^4} = 0 \tag{4.10}$$

Equation (4.10) is referred to as the stability capacitance - inductance line. Thus, the dc-link capacitance is found from (4.10) when other variables are substituted.

The load power (P) is substituted by the maximum input power of the SR machine, 13.5 kW, from Chapter3, which represent the worst condition [4.24]. The average output voltage of the input filter (V_0) is estimated by the dc supply voltage, 270V. This value is also used in the simulation to find the average dc-link current. The damping ratio is the minimum damping ratio, 0.03, from [4.22-4.23]. The input resistance of the low pass filter is varied among 0.01, 0.05, 0.1 and 0.2 Ω.

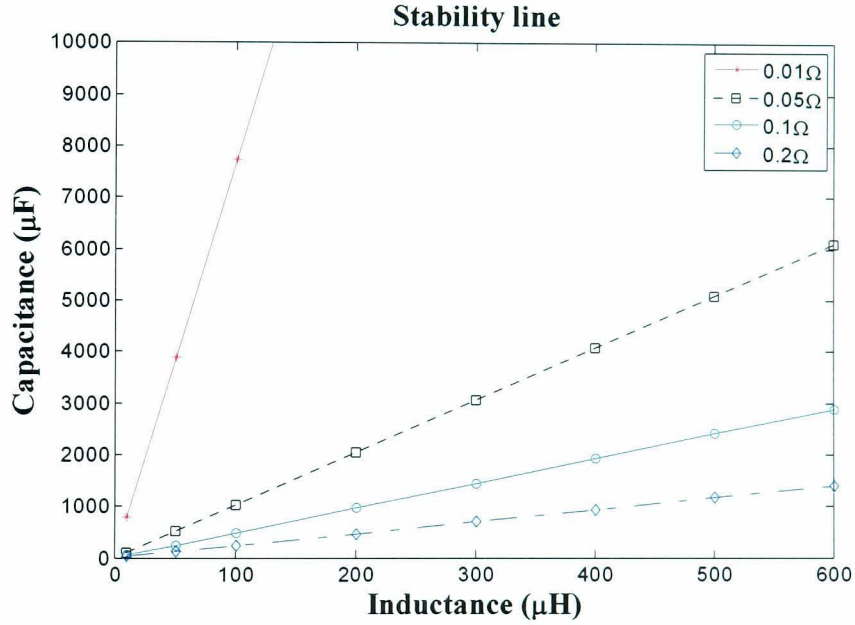


Figure 4.4: Stability lines with varied input resistances

The stability lines of the input inductance and the dc-link capacitance in the low pass filter are represented in Figure 4.4. The 4 stability lines are produced from the input resistance as previous stated. Any capacitance - inductance combination above these lines indicates that the system will be stable with a damping ratio greater or equal to 0.03. From Figure 4.4, the dc-link capacitance is decreased with the input resistance.

Nevertheless, a high input resistance reduce the efficiency of the drive system by reason of the high loss in the resistor.

4.3.2 Power Quality

After the process of the stability lines are described in the previous section. In this section, the required capacitance - inductance relationship referred to as power quality lines are established. The objective of the power quality line is to find the minimum capacitance and inductance for the input filter. There are two power quality requirements in [4.24]. One is the power quality for the dc-link capacitor voltage defined in the MIL-STD-704F standard [4.15] and the other one is the power quality for the input current defined in the MIL-STD-416E standard [4.16].

A power quality line describes the capacitance - inductance relationship, in a similar manner to the stability line. The capacitance in the power quality line is the minimum capacitance which makes the capacitor voltage and the input current satisfied the two standards.

To find the minimum capacitance, input resistance (R_L) and input inductance (L) are varied for computing the capacitor voltage (V_C) and the input current (I_L). The input resistance is also varied from 0.01Ω to 0.2Ω as showing in Section 4.3.1. The input inductance is varied from the minimum inductance, 10μH. For given values of the input resistance and input inductance, the dc-link capacitor is firstly specified with a low capacitance. Then, those input filter components, input resistor, input inductor and dc-link capacitor, are employed to compute the input current and the capacitor voltage from the simulated dc-link current of the design scenario. Subsequently, the resulting waveforms of the capacitor voltage and input current are analysed by FFT to obtain the spectrums. Those spectrums are plotted along with the standards for the following 3 conditions,

1. The ripple, peak to peak voltage of the dc-link capacitor is within 10% of the dc supply voltage, 27V.

2. The harmonic spectrum of the capacitor voltage normalize to the supply voltage (V_{dc}) is within the MIL-STD-704F standard, as shown in Table 4.1.
3. The harmonic spectrum of the input current normalize to the maximum average dc-link current ($I_{dc,max}$) is within the MIL-STD-416E standard, as shown in Table 4.2.

Table 4.1 shows the limit of the capacitor voltage harmonic spectrum normalize to the supply voltage according to the MIL-STD-704F standard [4.15]. Table 4.2 shows the limit of the input current harmonic spectrum normalising to the maximum average dc-link current, according to the MIL-STD-416E standard [4.16]. The maximum average dc-link current is the average dc-link current at the rated torque and 6000 rpm, as shown in Chapter 3.

Table 4.1: Limit of dc-link capacitor voltage harmonic component according to MIL-STD-704F standard

Frequency	10 Hz	1 kHz	5 kHz	50 kHz	500 kHz
% of V_{dc}	0.316%	3.16%	3.16%	0.316%	3.16×10^{-3}%

Table 4.2: Limit of input current harmonic component according to MIL-STD-416E standard

Frequency	40 Hz	1 kHz	5 kHz	50 kHz	150 kHz
% of $I_{dc,max}$	1%	5%	5%	0.5%	0.056%

If one of the three conditions is not passed, the specified capacitance value is increased. The capacitor voltage and the input current are calculated again. Then, the spectrum of the voltage and the current are re-plotted against the standards. This process is repeated until all of the three conditions are satisfied, with a minimum capacitance value. The process to find the power quality are illustrated in Figure 4.5.

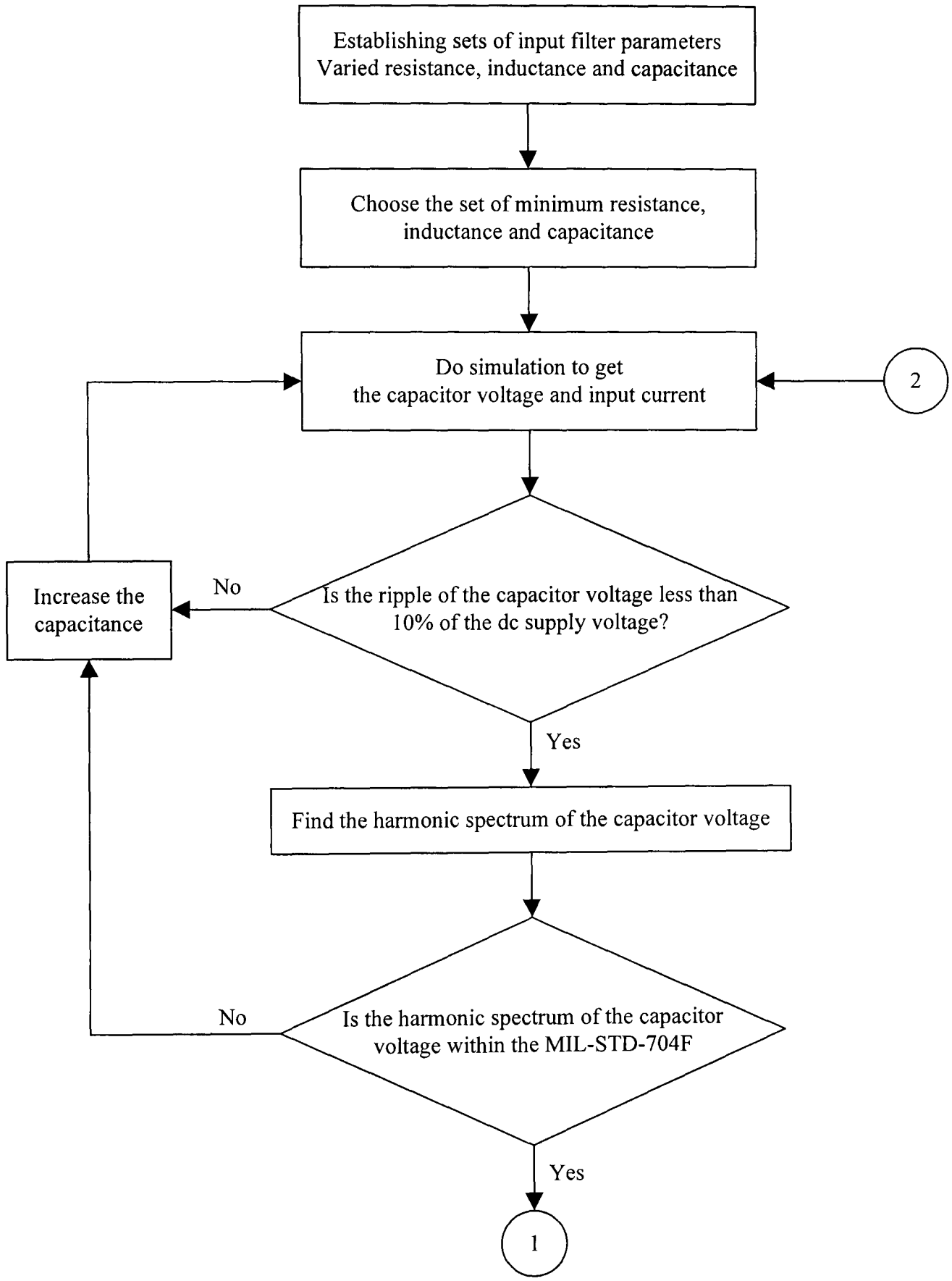


Figure 4.5: Power quality process (a)

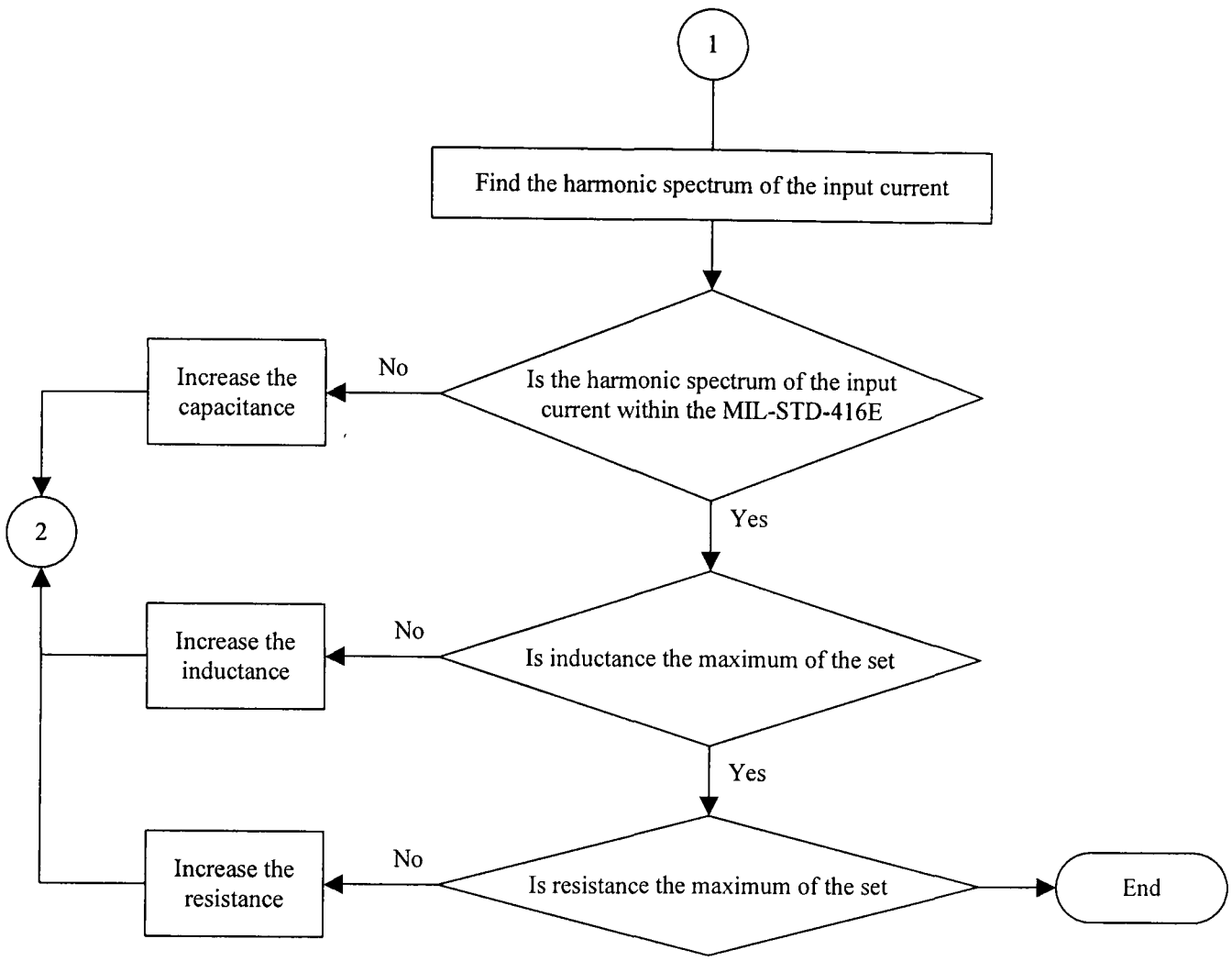
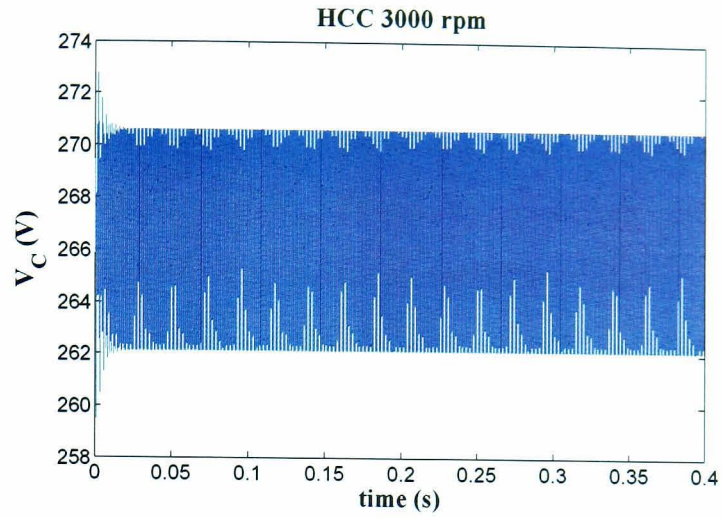
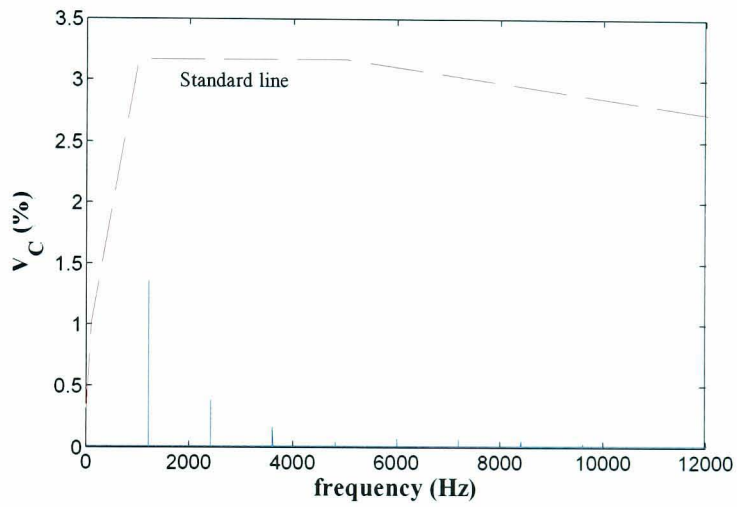


Figure 4.5: Power quality process (b)

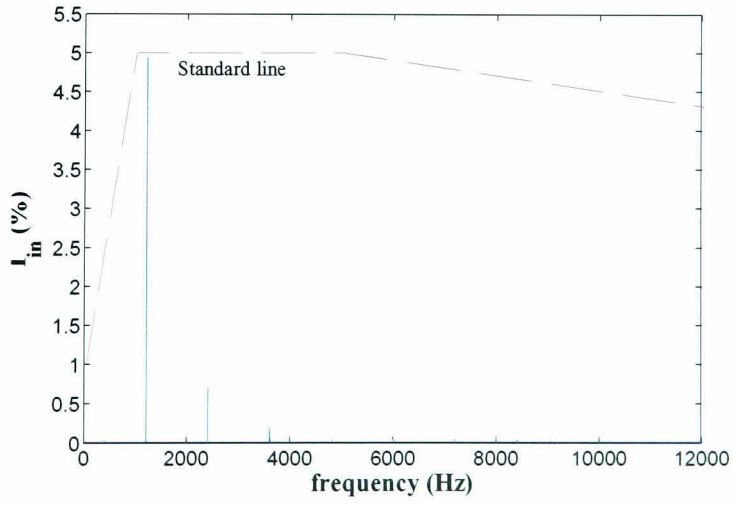
Figure 4.6 presents an example where the filter components, input resistor, input inductor, and dc-link capacitor, satisfy the three conditions. From this example, the minimum capacitance is 933 μF when the input inductance is 195.4 μH and the input resistance is 0.1 Ω. The capacitor voltage is computed from the simulated dc-link current of the design scenario which is from the HCC at 3000 rpm for the combined control. In Figure 4.6(a), the capacitor voltage, 8.53V, of which the peak to peak voltage is less than 10% of the supply voltage, is illustrated. Figure 4.6(b) presents the spectrum of the capacitor voltage as a percentage below the dashed standard line. Figure 4.5(c) shows the spectrum of the input current as a percentage which is also below the standard line.



(a) dc-link capacitor voltage



(b) spectrum of dc-link capacitor voltage



(c) spectrum of input current

Figure 4.6: Example of 3 condition achievement to find minimum capacitance

The minimum capacitances in the previous paragraph where the spectrum and capacitor voltage satisfy the three conditions with a varied input inductance for a given input resistance are plotted in a power quality line. Figure 4.7 shows the power quality lines for the combined control filter design. These lines are determined against the dc-link current of the HCC at 3000 rpm, which is the design scenario in Section 4.2. In Figure 4.8, the power quality lines for the filter design with the HCC are presented in Figure 4.8. Those lines are established from the dc-link current of the HCC at 100 rpm, as selected in Section 4.2.

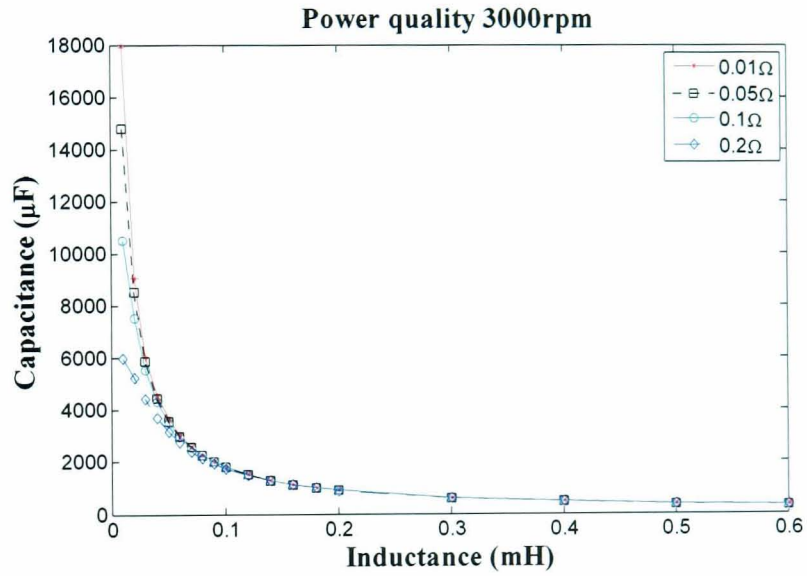


Figure 4.7: Power quality lines from hysteresis 3000rpm

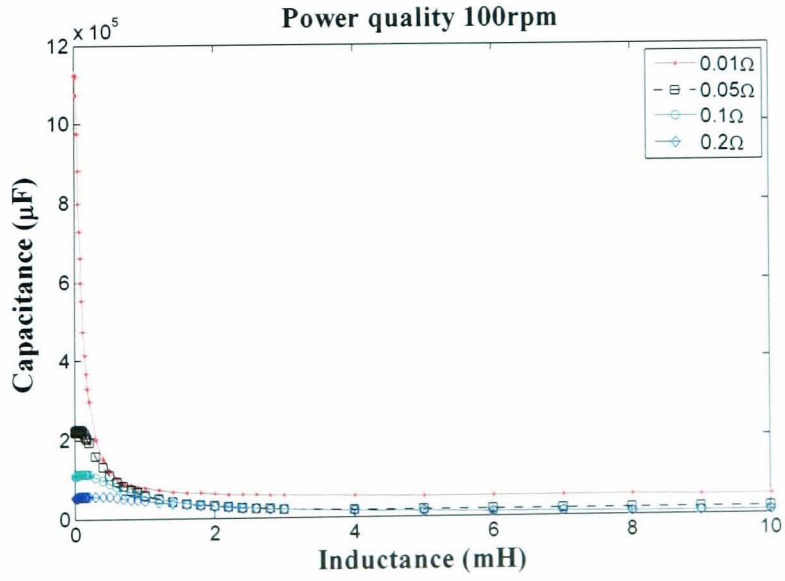


Figure 4.8: Power quality lines from hysteresis 100rpm

4.3.3 Filter Component Values

After the stability lines and the power quality lines are established in the previous sections, the dc-link capacitance and the input inductance from both lines can be determined for each given input resistance in this section.

By way of examples, for the filter design with the combined control, Figure 4.9 represents the graph of the stability line and the power quality line for which the input resistance is 0.01 Ω. Any capacitance and any inductance values in the shade region above the stability line and the power quality line may be selected for the designed filter. However, the aim of this research is to minimise the capacitance which occurs at the intersection point of the lines. Thus, the capacitance and the inductance at the intersection are chosen for the filter. From Figure 4.9, the selected capacitance is 3760μF and the selected inductance is 0.048mH.

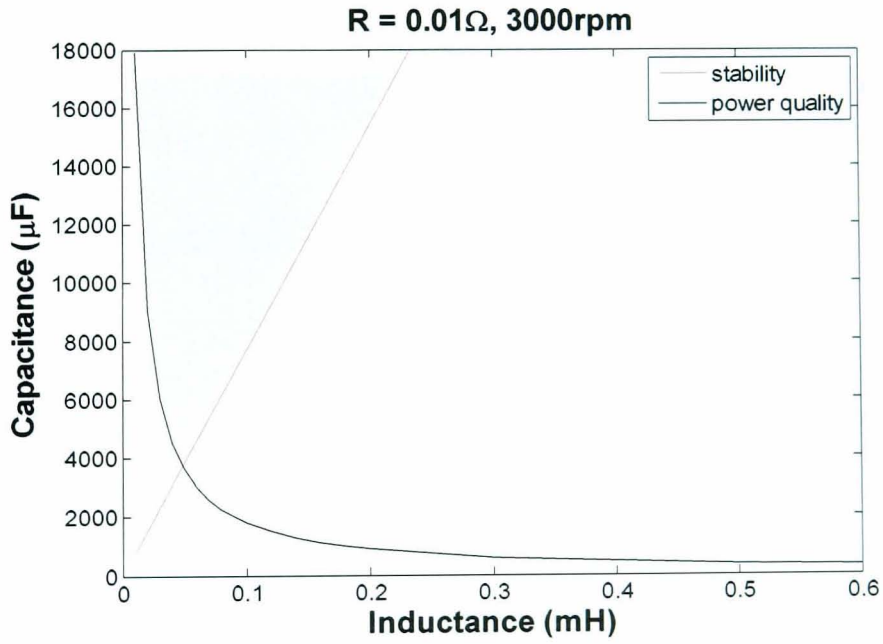


Figure 4.9: stability line and power quality when R_L = 0.01 Ω

For the combined control, the graphs of stability line and the power quality line, where the input resistances (R_L) are 0.05, 0.1 and 0.2, are similarly presented in Figure 4.10,

Figure 4.11, and Figure 4.12, respectively. The capacitance and the inductance at the crossing point from Figure 4.10 are selected at 1361μF and 0.134mH consequently. From Figure 4.11, the selected capacitance is 933μF and the selected inductance is 0.195mH. In Figure 4.12, the input resistance is 0.2Ω. The dc-link capacitance is chosen at 653μF and the input inductance is chosen at 0.282mH. From Figure4.10 - Figure4.12, it can be seen that when the input resistance increases, the range of the possible selected capacitance and inductance is wider.

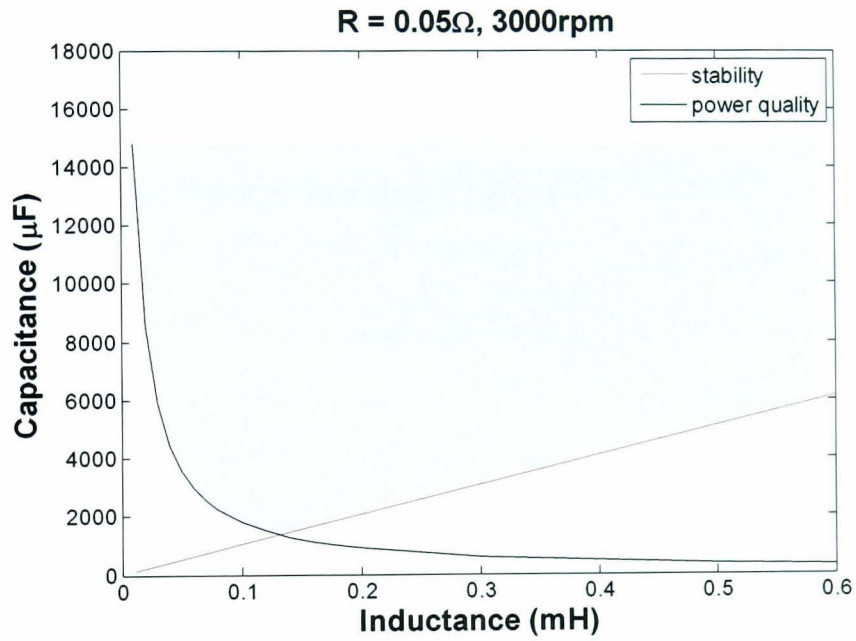


Figure 4.10: stability line and power quality when $R_L = 0.05\ \Omega$

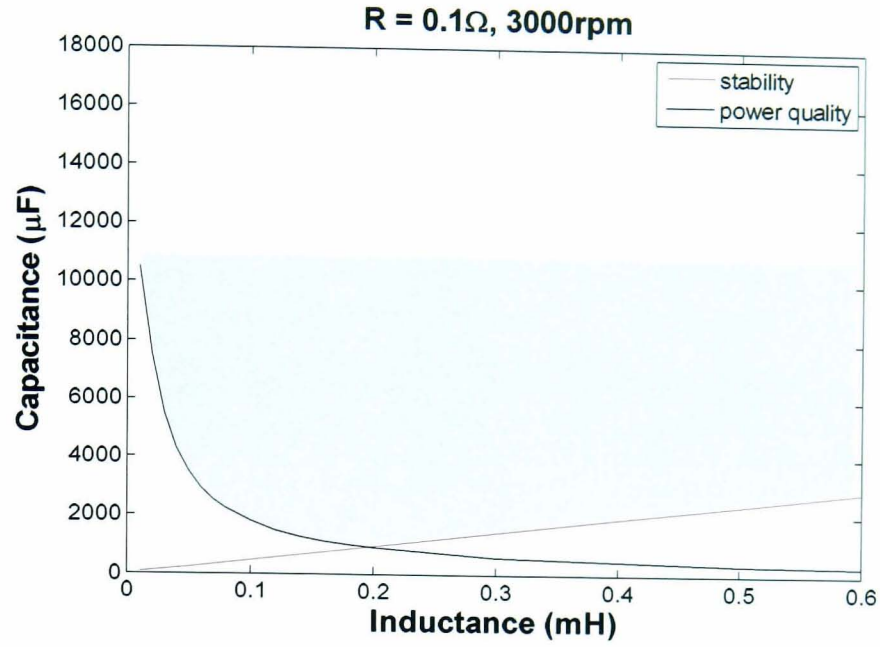


Figure 4.11: stability line and power quality when $R_L = 0.1\ \Omega$

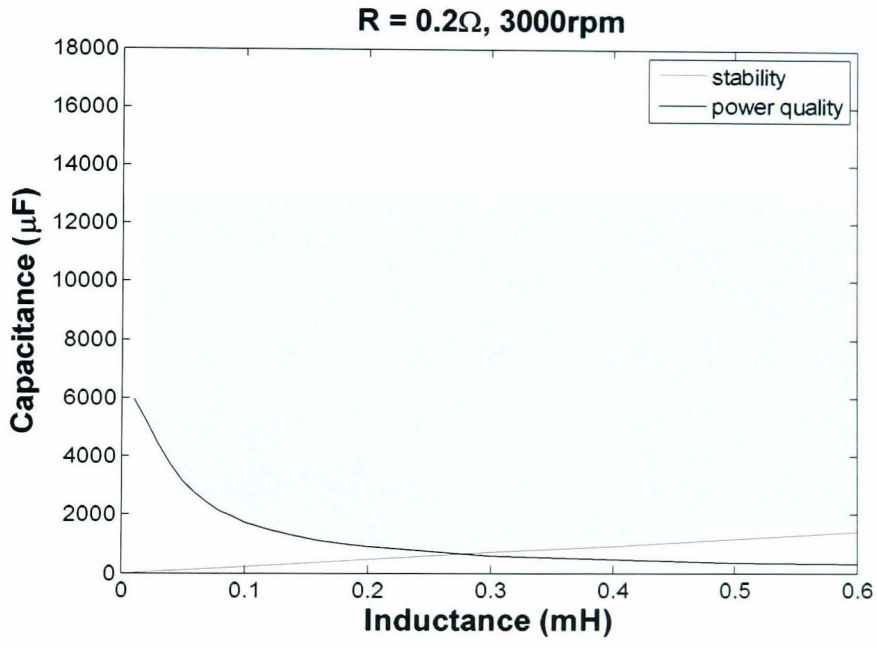


Figure 4.12: stability line and power quality when $R_L = 0.2\ \Omega$

The graphs of the stability lines and the power quality lines for the filter design with the HCC are similar to those graphs in Figure 4.9 - Figure 4.12, and the capacitance and the inductance can be determined in the same way. Table 4.3 summarises the values of the input resistance, input inductance and dc-link capacitance for both filter designs.

Table 4.3: Filter component values of filter designs

DLCIC + HCC		
R (Ω)	L (mH)	C (μF)
0.01	0.048	3760
0.05	0.134	1361
0.1	0.195	933
0.2	0.282	653
HCC		
0.01	0.890	68,870
0.05	2.450	24,934
0.1	3.596	17,170
0.2	5.170	11,797

From Table 4.3, when the input resistance is higher, the resulting filter capacitance is lower because the input resistance acts as a damping resistor. However, this gives a larger voltage across the resistor and more power dissipation in the input filter.

In contrast, the filter inductance increases with the increase of the input resistance. With a low capacitance, it is necessary to increase the inductance in order to attenuate the harmonics of the input current below the standard limit. Hence, it is not clear, which design shown in Table 4.3 yields the minimum weight. The answers are found in the next section.

4.4 Weight of Filters

From the previous section, the input inductance and the dc-link capacitance of the filter designs with the certain input resistances have been found. When the dc-link capacitance decreases, the input inductance increases. The trade-off among the filter components happens. So, the total weight of the input filter are estimated to compare

and find the lightest set of the input filter components. The process to find the weight of each component of the input filter is described in this section

4.4.1 Inductor weight

The inductor weight is calculated in this section. The process begins with the general inductor design [4.25-4.26]. Then, the inductor weight is calculated as follows [4.22]. The inductor weight is composed of the weight of the copper wire and the iron core, as

$$W_t = W_{cu} + W_{iron} \tag{4.11}$$

where

W_t is the total weight of the inductor.

W_{cu} is the weight of the copper wire.

W_{iron} is the weight of the iron core.

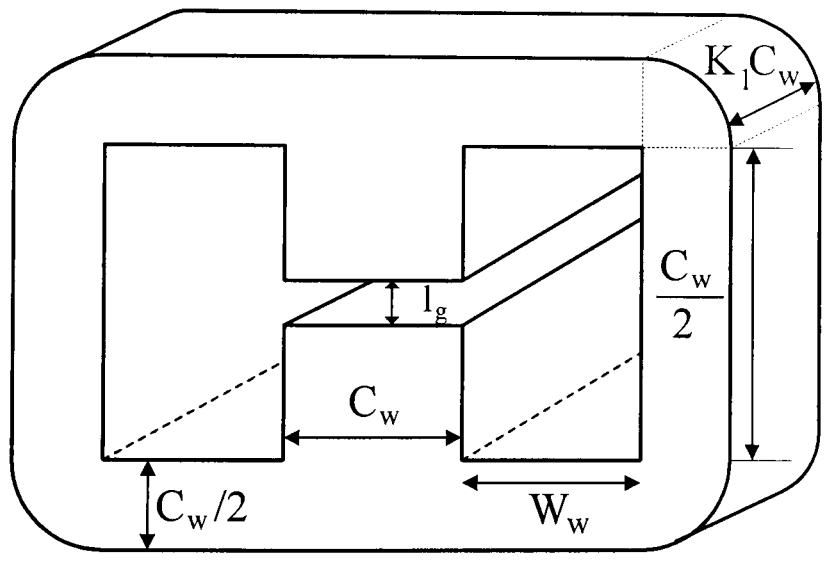


Figure 4.13: Dimension diagram of inductor core

Figure 4.13 represents the iron core of the double-E core of the inductor. The relationship between the inductance and the width of the inductor core is revealed as

$$LI_p = NB_{\max} K_1 C_w^2 \tag{4.12}$$

where

L is the designed inductance.

I_p is the peak current of the inductor.

N is the number of turns.

B_{max} is the maximum permissible flux density.

K_1 is a form factor coefficient.

C_w is the width of the inductor core.

The weight of the iron core is given as

$$W_{iron} = K_1 C_w^2 [2W_w (K_2 + 1) + C_w (1 + \pi/4)] \tag{4.13}$$

where

W_w is the width of the inductor window.

K_2 is the aspect ratio of the coil window.

The weight of the copper wire is found from

$$W_{cu} = d_{cu} N A_{cu} l_{av} \tag{4.14}$$

where

d_{cu} is the weight density of the copper wire.

A_{cu} is the cross section area of the copper wire.

l_{av} is the average length of the coil.

where

$$l_{av} = 2[C_w (1 + K_1) + 2h_b] + \pi W_w \tag{4.15}$$

where

h_b is the thickness of the bobbin.

From the maximum input current from Chapter3, 50A, the graph of the relationship between the inductor weight and the inductance is presented in Figure 4.14.

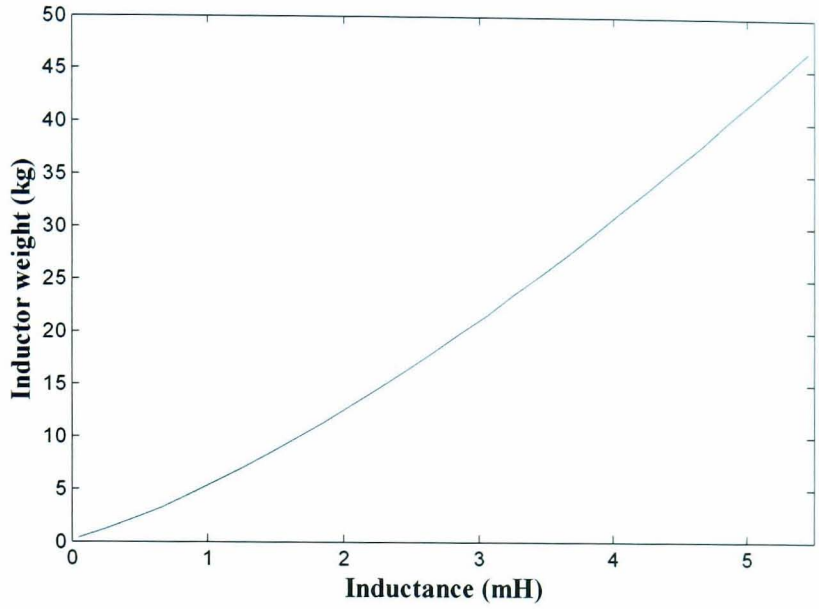


Figure 4.14: Inductor weight variation with inductance

4.4.2 Capacitor weight

The capacitor weight is estimated from the technical data of commercially manufactured dc-ac film-foil capacitors. Two different dc voltage ratings of 450V [4.33] and 700V [4.27] are considered. The lower rating results in a lower weight but at the expense of a reduced voltage margin from the 270V nominal dc link voltage. Curve fitting was used to estimate the relationship between the weight and the capacitance at voltage ratings of 450V and 700V. The relationship between the capacitor weight and the capacitance is shown in Figure 4.15.

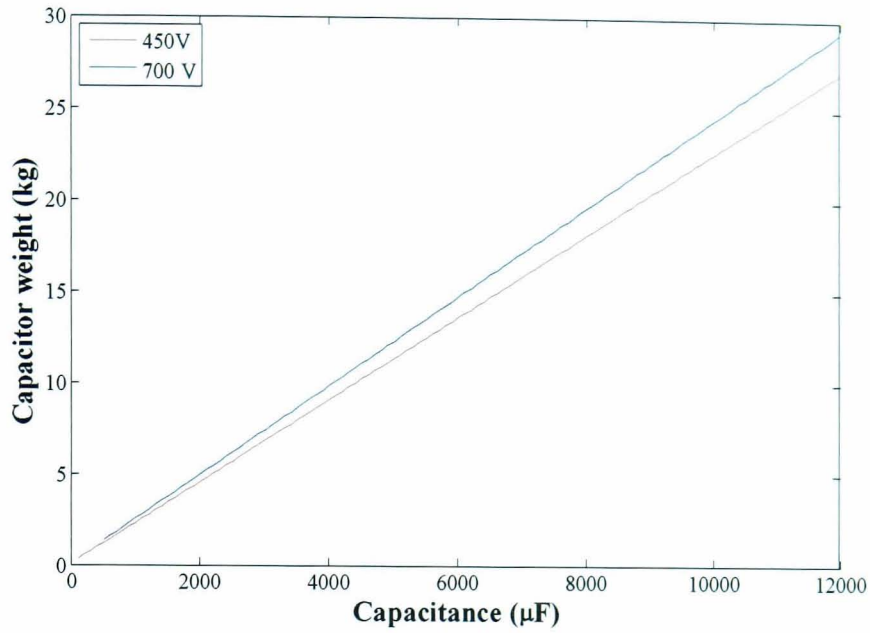


Figure 4.15: Capacitor weight variation with capacitance

4.4.3 Resistor weight

The resistor weight depends on the dissipated power rate of the resistor. From Section 4.3, the given input resistances are 0.01, 0.5, 0.1 and 0.2 Ω and the maximum inductor is 50A. Thus, the dissipated power is varied from 25W to 500W. Due to the wide range of the dissipated power, two types of commercial resistors are used to calculate the weight of input resistors. For the low power range of the power dissipation resistors, 5 - 50W, Vishay wire wound resistors are used. For the high power range of the power dissipation resistor, 50 - 500W, Vishay cement resistors are employed. The graph of the estimated relationship between the resistor weight and the power rating of the resistor is illustrated in Figure 4.16.

After the weight of all resistors, inductors and capacitors are determined, the weight data of the resistance, inductance and capacitance are shown in Table 4.4 and Table 4.5.

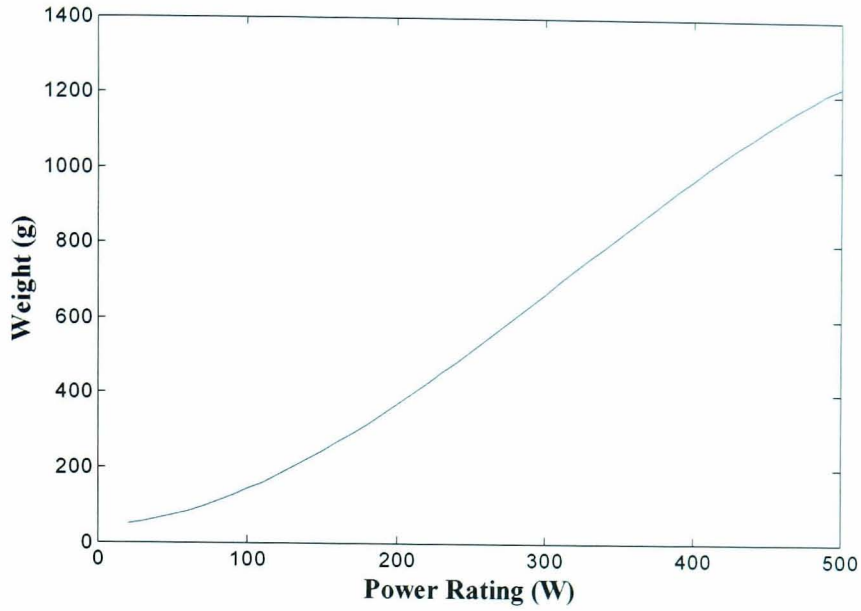


Figure 4.16: Resistor weight variation with resistance

Table 4.4: Filter component weight for the combine control

R_L	L	C (450V / 700V)			total weight
0.01 Ω	0.048 mH	3760 μF	8.54 kg	450V	8.84 kg
0.05 kg	0.25 kg		9.25 kg	700V	9.55 kg
0.05 Ω	0.134 mH	1361 μF	3.14 kg	450V	3.93 kg
0.19 kg	0.60 kg		3.41 kg	700V	4.20 kg
0.1 Ω	0.195 mH	933 μF	2.17 kg	450V	3.54 kg
0.51 kg	0.86 kg		2.37 kg	700V	3.74 kg
0.2 Ω	0.282 mH	653 μF	1.54 kg	450V	4.01 kg
1.22 kg	1.25 kg		1.69 kg	700V	4.16 kg

Table 4.4 presents the weight of the filter components for the designed filter with the combined control. The chosen filter components are from the lightest weight set which the input resistance is 0.1Ω. For HCC, the weights of the filter are shown in Table 4.5. The lightest weight filter set is also the 0.1Ω resistor set.

Table 4.5: Filter component weight for hysteresis current control (HCC)

R_L	L	C (450V / 700V)			total weight
0.01 Ω	0.89 mH	68870 μF	155.03 kg	450V	159.64 kg
0.05 kg	4.56 kg		167.60 kg	700V	172.21 kg
0.05 Ω	2.45 mH	24934 μF	56.18 kg	450V	72.56 kg
0.19 kg	16.19 kg		60.75 kg	700V	77.13 kg
0.1 Ω	3.60 mH	17170 μF	38.71 kg	450V	66.02 kg
0.51 kg	26.80 kg		41.86 kg	700V	69.17 kg
0.2 Ω	5.17 mH	11797 μF	26.62 kg	450V	70.72 kg
1.22 kg	42.88 kg		28.79 kg	700V	72.89 kg

From both tables, the lightest weights of the filter component for the combine control and HCC are the set of 0.1-Ω resistor. The 450-V rated capacitor yields lighter weight of the filter set than the 700-V rated capacitor. The weight of the filter for the combined control which 450-V rated capacitor is used is 3.54 kg and that for the HCC is 66.02 kg. Therefore, the weight of the filter for HCC is 18.65 times of that for the combined control, when the 450-V rated capacitor is used. When the 700-V rated capacitor is used, the weight of the chosen filter set for the combined control is 3.74 kg and that of the HCC is 69.17 kg. The ratio of the filter weight which is used the 700-V rated capacitor between the combined control and the HCC is 18.49 times.

After the filter components have been designed, the filters will be checked with the simulation of the dc link integration control, and the thermal stress on the capacitor occurring from the rms dc-link current is also assessed.

4.5 Design analysis

After the filter components based on the minimum weight are selected, simulations are performed to ascertain whether the operation of DLCIC is effective as expected with the designed filter. Furthermore, the dc-link capacitor will be assured that it can tolerate the thermal stress during the machine operation.

4.5.1 DLCIC examination

Although DLCIC is proved that the peak to peak of the capacitor from DLCIC is much lower than that of HCC, all designed scenarios are from HCC. If the designed filter is been used with DLCIC, whether the voltage ripple and the spectrums of the capacitor voltage and input current are still below the standard limits. Hence, in this section, the operation of DLCIC with the designed filter is examined to determine the capacitor voltage and input current from DLCIC satisfy the three conditions of the military standards, as stated in Section 4.3.2.

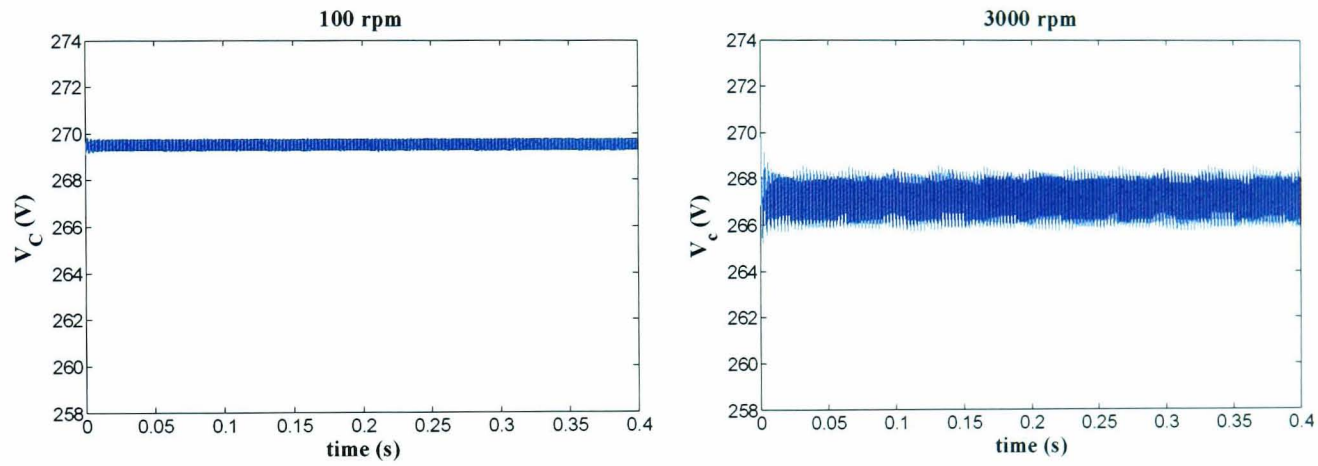
The capacitor voltage ripple and the spectrums from the voltage and current of DLCIC have been inspected at the rated demand torque. The speeds of the test are chosen at 100 rpm and 3000 rpm because the speed range of DLCIC is from 100 rpm to 3000 rpm. If the voltage and the current at these speeds are approved, it is implied that the filter design can be utilised with the DLCIC operation at the speeds between 100 rpm and 3000 rpm.

Figure 4.17 shows the capacitor voltages from DLCIC at 100 rpm and 3000 rpm. Although the capacitor voltage ripple at 3000 rpm is higher than that at 100 rpm, in both graphs the capacitor voltage ripple is not higher than 27 V or 10% of the dc supply voltage. Hence, the operation of DLCIC passes the first condition.

Figure 4.18 presents the spectrum of the capacitor voltages. The red dashed line is the standard line from MIL-STD-704F. The harmonics of the capacitor voltage are not

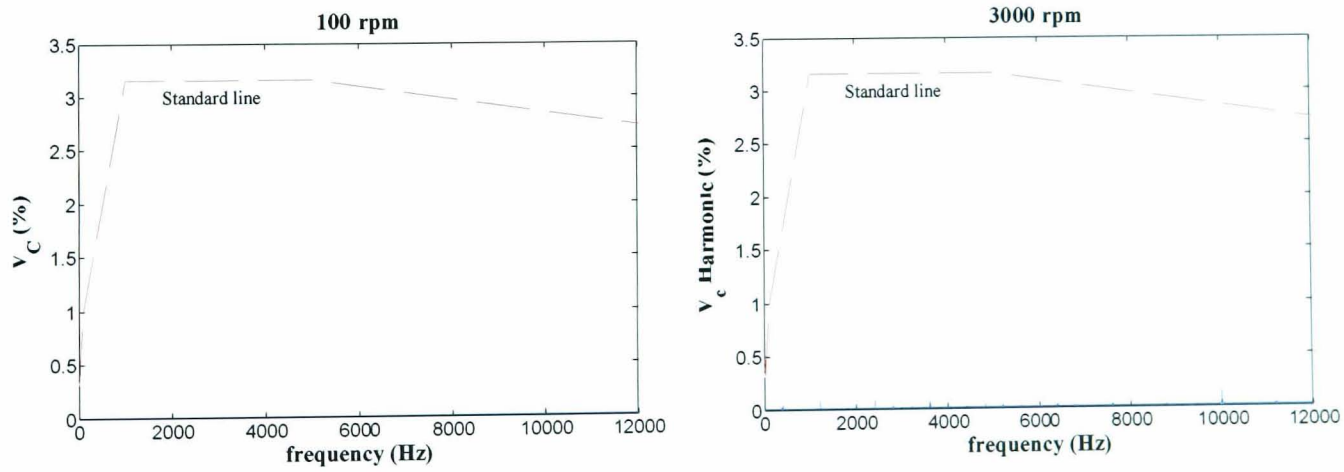
supposed to be beyond that line. From the figure, the harmonics of DLCIC at 100 rpm and 3000 rpm are still below the standard line.

Figure 4.19 shows the harmonics of the input currents, and it has the dashed standard line, similar to Figure 4.18. As expected, the harmonics of the input current from DLCIC in Figure 4.19 are not beyond the standard limit. Hence, it can be seen that the designed filter and DLCIC can well cooperate in the speed range of 100 - 3000 rpm.



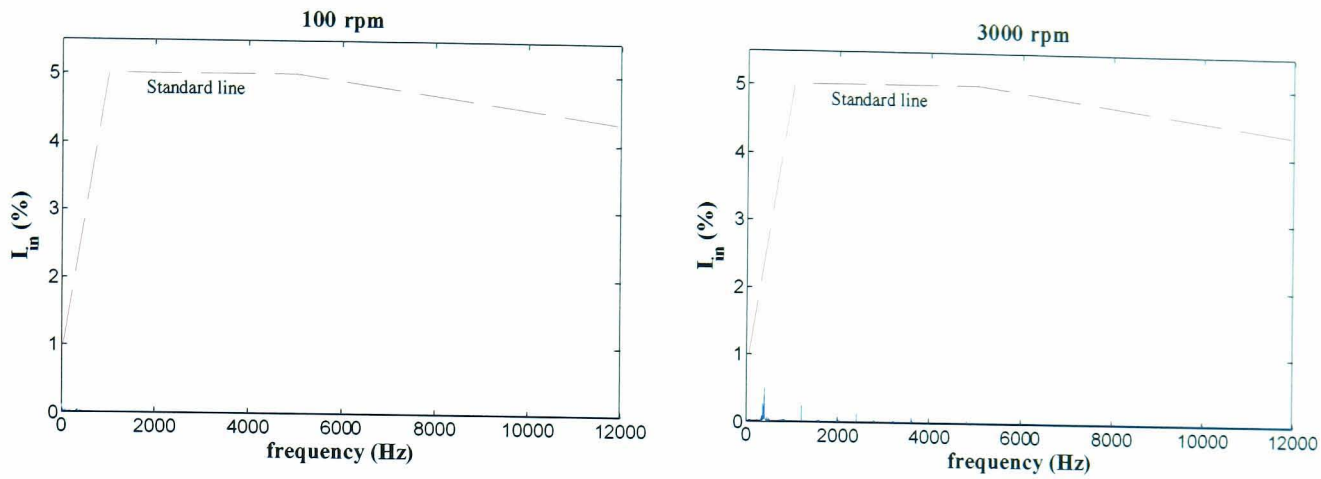
(a) (b)

Figure 4.17: Capacitor voltage of DLCIC



(a) (b)

Figure 4.18: Spectrums of capacitor voltage of DLCIC



(a) (b)

Figure 4.19: Spectrum of input currents of DLCIC

4.5.2 Thermal Stress of Dc-link Capacitor

Since the capacitor temperature and frequency have a strong influence on the life time of the capacitor, it is important that the filter capacitor life is not shorten due to the excessive thermal stress in the dc-link capacitor [4.28-4.29, 4.34]. The capacitor temperature is determined from

$$T_c = T_a + I_{c,rms}^2 R_s R_{th} \tag{4.16}$$

where

T_c is the temperature of the dc-link capacitor.

T_a is the ambient temperature.

$I_{c,rms}$ is the maximum rms current of the dc-link capacitor.

R_s is the equivalent series resistance of the dc-link capacitor.

R_{th} is the thermal resistance of the dc-link capacitor.

The thermal stress examinations are done for both designed filters. The simulations has been done at the rated torque. The rms current in the dc-link capacitor of both filters are calculated in Table 4.6 and Table 4.7.

Table 4.6 shows the rms currents in the dc-link capacitor in the case that DLCIC and HCC are combined for the SR machine operation. The maximum rms current from

HCC occurs at 4000 rpm, 44.8178 A. The capacitance from the designed filter is 933 μF. From the film foil capacitor datasheet [4.27], the equivalent series resistance of the capacitor (R_s) is 0.5 mΩ and the thermal resistance (R_{th}) is 2.1°C/W.

Table 4.6: Rms current in dc-link capacitor at the rated torque for the combined control

Control method	speed (rpm)	$I_{c,rms}$ (A)
DLCIC	100	19.36
	500	21.83
	1000	24.75
	2000	27.90
	3000	29.29
HCC	3000	43.14
	4000	44.82
	5000	42.67
	6000	35.97
	7000	31.96
	8000	29.96
	9000	28.57
	10000	26.43

When the ambient temperature is 40°C, from (4.16), the capacitor temperature is 42.11°C. This capacitor temperature is much lower than the hotspot temperature limitation of the capacitor, which is 70°C. Thus, the 933 μF capacitor can be used without compromising its life time.

Table 4.7 presents the rms currents of the dc-link capacitor for the HCC filter design. The maximum rms current also occurs at 4000 rpm, 44.2682 A. For the HCC operation, the designed capacitance is 17170 μF. However, the maximum capacitance of the capacitor in the datasheet is 2000 μF. Thus, eight of the 2000 μF capacitors are parallel

connected as the 17170-μF capacitor. The current through a 2000 μF capacitor is $\frac{1}{8}$ of the current from Table 4.7.

Table 4.7: Rms current of dc-link capacitor for hysteresis current control operation

Control method	speed (rpm)	$I_{c,rms}$ (A)
HCC	100	18.71
	500	25.32
	1000	30.83
	2000	37.86
	3000	42.36
	4000	44.27
	5000	42.26
	6000	35.65
	7000	31.81
	8000	29.90
	9000	28.52
	10000	26.38

With the 0.5 mΩ equivalent series resistance and the 1.4°C/W thermal resistance, the capacitor temperature is 40.02°C when the ambient temperature is 40°C. This is far from the hotspot temperature, 70°C. So, the 17170 μF capacitor can be used in the filter without shorten the capacitor life.

4.6 Conclusion

The second order input filter design for the switched reluctance machine has been described. Two filter designs are considered in this chapter. One is designed for DLCIC at 100 - 3000 rpm, and HCC above 3000 rpm. The other is designed for the HCC only. The stability and the power quality standards from [4.15-4.16] are used in the filter design. Further, the design inspection is performed. The capacitor voltage and

the input current from DLCIC during 100 - 3000 rpm are simulated with the designed filter and the spectra are found to satisfy the required standards. The thermal stress in the dc-link capacitor is also examined. It has also been shown that the filter, which is designed for the combined control is approximately 18 times lighter than the designed filter for HCC.

4.7 Reference

[4.1] S. Girinon, H. Piquet, N. Roux, and B. Sareni, "Analytical input filter design in DC distributed power systems approach taking stability and quality criteria into account," in *Power Electronics and Applications, 2009. EPE '09. 13th European Conference on*, 2009, pp. 1-10.

[4.2] F. C. Lee and Y. Yuan, "Input-Filter Design for Switching Regulators," *Aerospace and Electronic Systems, IEEE Transactions on,* vol. AES-15, pp. 627-634, 1979.

[4.3] D. C. Hamill and T. Ong Tiam, "Analysis and design of an active ripple filter for DC-DC applications," in *Applied Power Electronics Conference and Exposition, 1995. APEC '95. Conference Proceedings 1995., Tenth Annual*, 1995, pp. 267-273 vol.1.

[4.4] M. U. Iftikhar, D. Sadarnac, and C. Karimi, "Input Filter Damping Design for Control Loop Stability of DC-DC Converters," in *Industrial Electronics, 2007. ISIE 2007. IEEE International Symposium on*, 2007, pp. 353-358.

[4.5] A. Emadi and M. Ehsani, "Negative impedance stabilizing controls for PWM DC-DC converters using feedback linearization techniques," in *Energy Conversion Engineering Conference and Exhibit, 2000. (IECEC) 35th Intersociety*, 2000, pp. 613-620 vol.1.

[4.6] A. Khaligh, "Realization of Parasitics in Stability of DC-DC Converters Loaded by Constant Power Loads in Advanced Multiconverter Automotive Systems," *Industrial Electronics, IEEE Transactions on,* vol. 55, pp. 2295-2305, 2008.

[4.7] A. B. Awan, B. Nahid-Mobarakeh, S. Pierfederici, and F. Meibody-Tabar, "Nonlinear Stabilization of a DC-Bus Supplying a Constant Power Load," in *Industry Applications Society Annual Meeting, 2009. IAS 2009. IEEE*, 2009, pp. 1-8.

[4.8] L. Xinyun, A. J. Forsyth, and A. M. Cross, "Negative Input-Resistance Compensator for a Constant Power Load," *Industrial Electronics, IEEE Transactions on,* vol. 54, pp. 3188-3196, 2007.

[4.9] A. Khaligh, A. M. Rahimi, and A. Emadi, "Negative Impedance Stabilizing Pulse Adjustment Control Technique for DC/DC Converters Operating in Discontinuous Conduction Mode and Driving Constant Power Loads," *Vehicular Technology, IEEE Transactions on,* vol. 56, pp. 2005-2016, 2007.

[4.10] P. Liutanakul, A. B. Awan, S. Pierfederici, B. Nahid-Mobarakeh, and F. Meibody-Tabar, "Linear Stabilization of a DC Bus Supplying a Constant Power Load: A General Design Approach," *Power Electronics, IEEE Transactions on,* vol. 25, pp. 475-488, 2010.

[4.11] S. Kim and S. S. Williamson, "Negative impedance instability compensation in more electric aircraft DC power systems using state space pole placement control," in *Vehicle Power and Propulsion Conference (VPPC), 2011 IEEE*, 2011, pp. 1-6.

[4.12] P. Liutanakul, S. Pierfederici, A. Bilal, B. Nahid-Mobarakeh, and F. Meibody Tabar, "Stability investigation of inverter motor drive system with input filter - Optimisation of the DC-link capacitance value," in *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE*, 2008, pp. 3728-3734.

[4.13] A. Kwasinski and P. T. Krein, "Stabilization of constant power loads in Dc-Dc converters using passivity-based control," in *Telecommunications Energy Conference, 2007. INTELEC 2007. 29th International*, 2007, pp. 867-874.

[4.14] F. Arteche, B. Allongue, F. Szoncsó, and C. Rivetta, "EMI Filter Design and Stability Assessment of DC Voltage Distribution based on Switching Converters," presented at the 7th Workshop on Electronics for LHC Experiments, LEB 2001, Stockholm, Sweden 2001.

[4.15] *Aircraft Electric Power Characteristic*, MIL-STD-704F, 2004

[4.16] *Requirements for the control of Electromagnetic Interference Characteristics of Subsystems and Equipment*, MIL-STD-461E, 1999

[4.17] A. Mariscotti, "Analysis of the DC-link current spectrum in voltage source inverters," *Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on,* vol. 49, pp. 484-491, 2002.

[4.18] B. P. McGrath and D. G. Holmes, "A General Analytical Method for Calculating Inverter DC-Link Current Harmonics," in *Industry Applications Society Annual Meeting, 2008. IAS '08. IEEE*, 2008, pp. 1-8.

[4.19] A. Eid, H. El-Kishky, M. Abdel-Salam, and M. T. El-Mohandes, "On Power Quality of Variable-Speed Constant-Frequency Aircraft Electric Power Systems," *Power Delivery, IEEE Transactions on,* vol. 25, pp. 55-65, 2010.

[4.20] A. Emadi, A. Khaligh, C. H. Rivetta, and G. A. Williamson, "Constant power loads and negative impedance instability in automotive systems: definition, modeling, stability, and control of power electronic converters and motor drives," *Vehicular Technology, IEEE Transactions on,* vol. 55, pp. 1112-1125, 2006.

[4.21] C. H. Rivetta, A. Emadi, G. A. Williamson, R. Jayabalan, and B. Fahimi, "Analysis and control of a buck DC-DC converter operating with constant power load in sea and undersea vehicles," *Industry Applications, IEEE Transactions on,* vol. 42, pp. 559-572, 2006.

[4.22] A. Griffo and J. Wang, "Design optimization of passive DC filters for aerospace applications," in *Power Electronics, Machines and Drives (PEMD 2010), 5th IET International Conference on*, 2010, pp. 1-6.

[4.23] A. Griffo and J. Wang, "Stability assessment of electric power systems for 'more electric' aircraft," in *Power Electronics and Applications, 2009. EPE '09. 13th European Conference on*, 2009, pp. 1-10.

[4.24] J. Mavier, "Moet Coordination Memorandum," unpublished

[4.25] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications, and Design*, 2nd ed.: John Willey & Sons, 1995.

[4.26] S. Chandrasekaran, S. A. Ragon, D. K. Lindner, Z. Gurdal, and D. Boroyevich, "Optimization of an Aircraft Power Distribution Subsystem," *Journal of Aircraft,* vol. 40, pp. 16-26, 2003.

[4.27] *Capacitors for Power Electronics*, 4th ed., WestCode Co., Chippenham, UK, 2004.

[4.28] J. W. Kolar and S. D. Round, "Analytical calculation of the RMS current stress on the DC-link capacitor of voltage-PWM converter systems," *Electric Power Applications, IEE Proceedings -,* vol. 153, pp. 535-543, 2006.

[4.29] M. Bierhoff and F. W. Fuchs, "DC link harmonics of three phase voltage source converters influenced by the pulse width modulation strategy-an analysis," in *Industrial Electronics Society, 2005. IECON 2005. 31st Annual Conference of IEEE*, 2005, p. 6 pp.

[4.30] G. Zhao, J. Lui, and M. Han, "Design of Input Filters Considering the Stability of STATCOM System," *Journal of Power Electronics,* vol. 11, pp. 904-913, 6, November 2011.

[4.31] S. D. Sudhoff, S. F. Glover, P. T. Lamm, D. H. Schmucker, and D. E. Delisle, "Admittance space stability analysis of power electronic systems," *Aerospace and Electronic Systems, IEEE Transactions on,* vol. 36, pp. 965-973, 2000.

[4.32] S. D. Sudhoff and S. F. Glover, "Three-dimensional stability analysis of DC power electronics based systems," in *Proc. Power Electronics Specialists Conference, 2000. PESC 00. 2000 IEEE 31st Annual*, 2000, pp. 101-106 vol.1.

[4.33] EPCOS, "Film capacitors - Power electronic capacitors," B25655 datasheet, Oct. 2009.

[4.34] H. Saren, O. Pyrhonen, J. Luukko, O. Laakkonen, and K. Rauma, "Verification of frequency converter with small DC-link capacitor," in *Proc. Power Electronics and Applications, 2005 European Conference on*, 2005, pp. 10 pp.-P.10.

Chapter 5

Experimental Results

5.1 Introduction

In the previous chapters, the DC-link current integration control (DLCIC) has been proposed and described. The simulation studies have been carry out to compare it with other techniques, and its operation speed range has been determined. In this chapter, DLCIC is applied and implemented in experiments to validate that it is able to operate in a practical system and can reduce the dc-link capacitor voltage ripple when comparing with the hysteresis current control (HCC).

An overview of the hardware components employed in the experimental drive system is introduced. An existing 13.5 kW (at 36000 rpm), 3 phase prototype SR machine and converter are used as a means for the experimental validation. A 15 kW (at 42000 rpm) dynamometer is coupled as a load. A dSPACE platform is used to realise speed loop control with the proposed DLCIC technique. The hardware limitations such as the dc-link current measurement and position measurement, which affects the control circuit designs, are also described. Then, the principles of the control circuits for both HCC

and DLCIC are explained. The experimental results from HCC and DLCIC are compared and analysed.

5.2 SR Drive System (Hardware)

Figure 5.1 illustrates the schematic diagram of hardware platform for the experiment. The SR hardware consists of 4 parts.

1. SR machine, dynamo and position sensors
2. Converter
3. Current control
4. Speed control

They will briefly described in the subsequent sections.

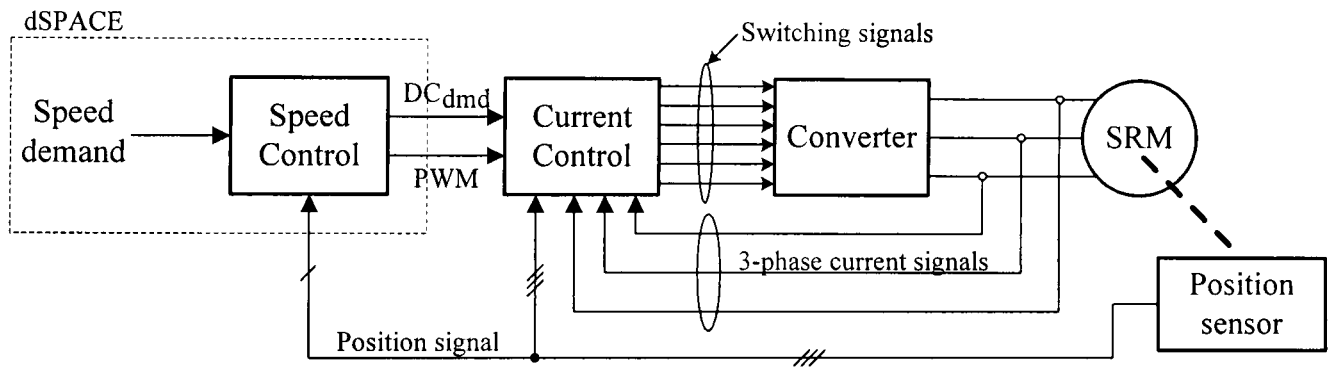


Figure 5.1: Schematic diagram of experimental hardware

5.2.1 SR machine, Dynamometer and Position Sensor

In the experiment, the SR machine is coupled to a dynamometer, which is operated as a machine load. The position sensors are fixed around the rotor shaft on the frame of the SR machine stator.

The SR motor is a 13.5 kW, 3 phase switched reluctance machine. It has 12 stator poles and 8 rotor poles. The stroke angle is 15° mechanical degrees. Although the maximum speed of the SR motor is 37,000 rpm, it is not operated higher than 3000 rpm in the experiments due to the operation speed range, which is defined in Chapter3. Figure 5.2

shows the SR motor and the dynamometer coupled together. The dynamometer is a 15kW, 3 phase induction machine with 4 Nm maximum torque. Although the rated torque of the SR motor is 20 Nm, as a result of the limited dynamometer torque, the maximum load torque in the experiment is 4 Nm.

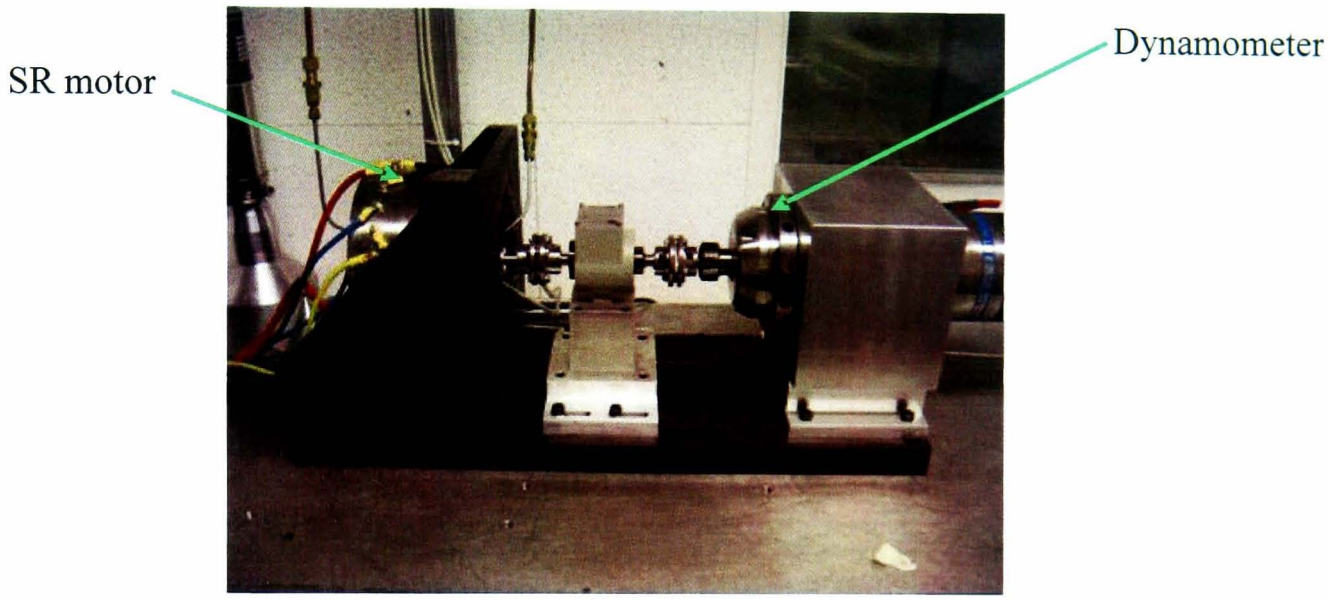


Figure 5.2: SR motor coupled to dynamometer

The rotor position sensors are composed of 3 opto-schmitt sensors which are attached to the motor frame opposite to the rotor output shaft, as shown in Figure 5.3(a) and each opto-schmitt sensor is displace 120°, as shown in Figure 5.3(b).

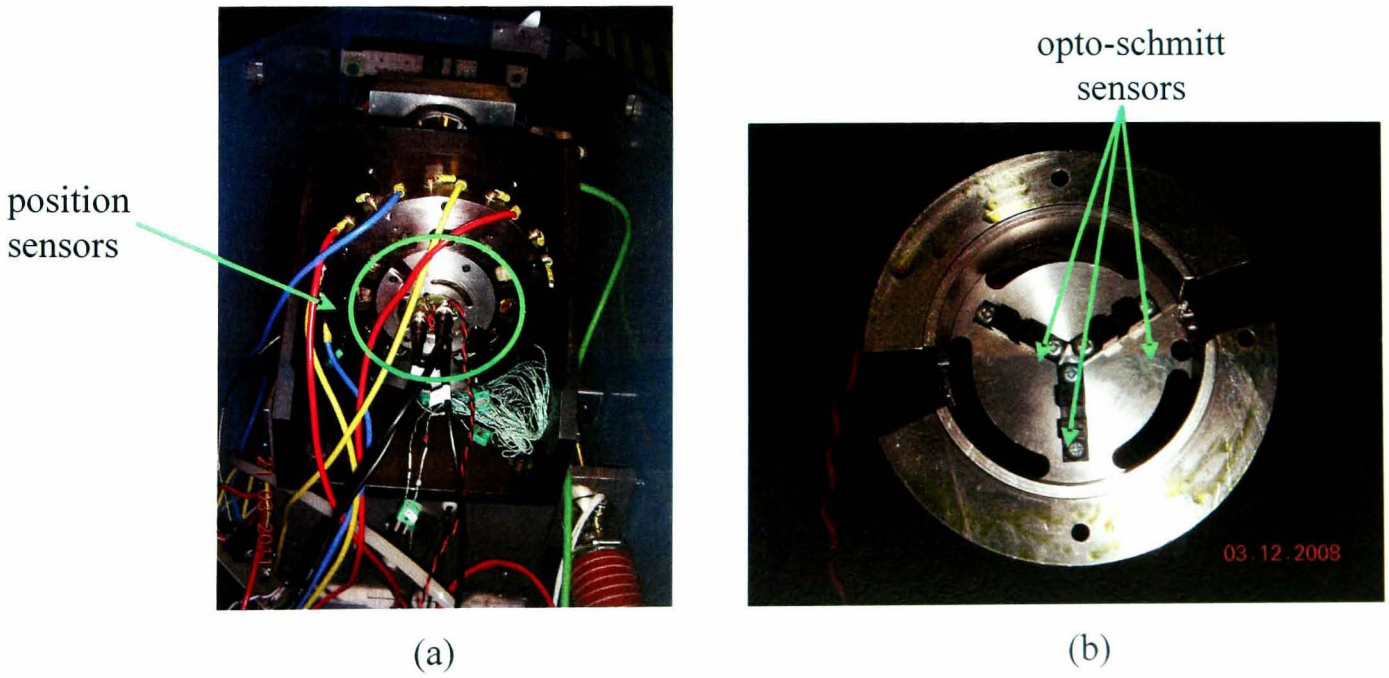


Figure 5.3: Opto-schimtt position sensor

The opto-schmitt sensors operate together with a claw-pole ring which is shown in Figure 5.4. It has 8 equally spared teeth and slots. The width of each teeth is 22.5°.

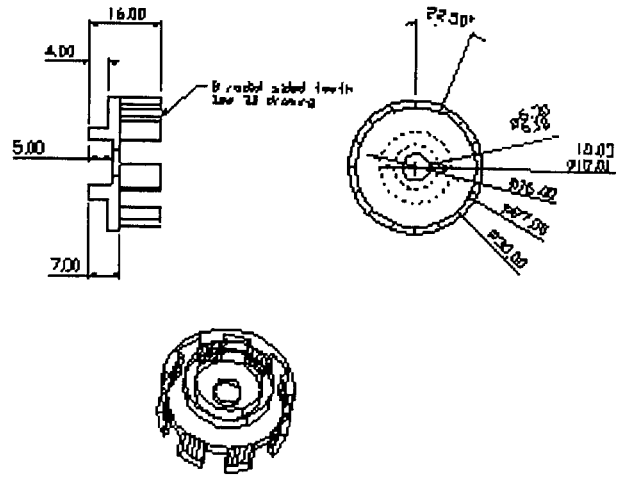


Figure 5.4: Position sensor encoder

The claw-pole ring is fixed on the rotor concentrically. When the rotor rotates, the teeth of the ring also rotates and moves through the optical path of the opto-schmitt sensors. Consequently the opto-schmitt sensors generate digital square waves with 50% duty cycle whose the electrical period equals to that of the SR machine, 45° mechanical degrees.

The digital position signals from those opto-schmitt sensors are illustrated in Figure 5.5. The rising edge of phase1 (*Ph1*) is at the position of 3° mechanical degrees with respect to the unaligned position, and the width of the pulse is 22.5°. The position signals of phase2 (*Ph2*) and phase3 (*Ph3*) are shifted by 15° and 30° mechanical degrees, respectively.

From the position signals, the dwell signals (DPh) are established, as shown in Figure 5.5(b). The turn-on angle of the dwell signal for phase1 is at 3° or at the rising edge of phase1 signal. It is kept on over the dwell angle, 15°, and turned off at the rising edge of the next phase position signal. Since the dwell signals are generated from the position signals, the turn-on and turn-off angles in the experiment are fixed.

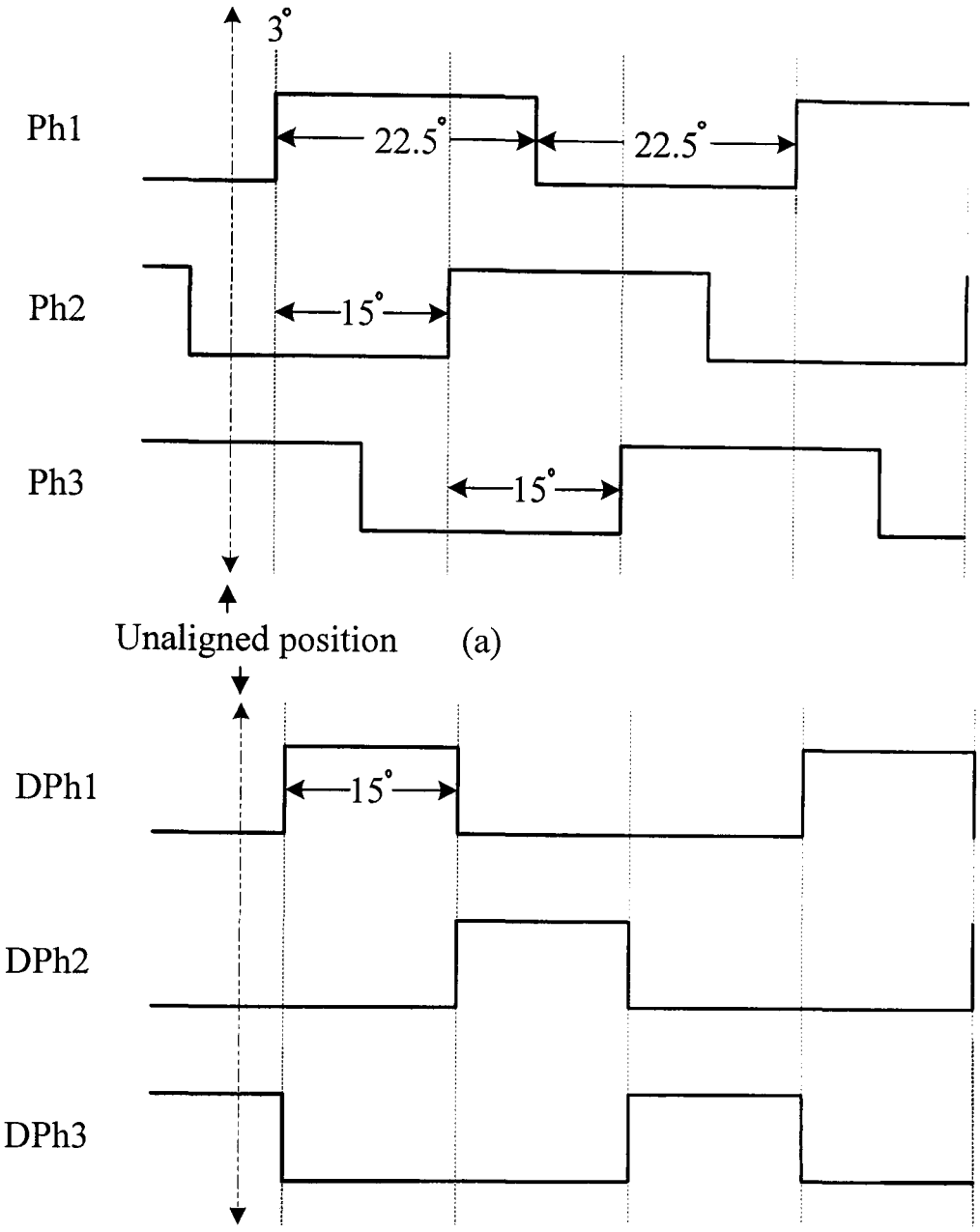


Figure 5.5: Position signals (a) and dwell signals (b)

5.2.2 Converter

From Figure 5.1, the converter block receives switching signals from the current control block and controls the current of the phase winding in the SR machine. In the experiment, the converter block is comprised of a fibre optic transmission and receiving circuit, a H-bridge converter and a dc supply, as shown in Figure 5.6. The dc supply, Regatron, connected to the converter is capable of 16-kW at 270 V with a maximum

current of 50 A. The digital switching signals from the current control boards are fed to the fibre optic circuit. Then, the circuit converts the switching signals to the optical signals, and transmits them to the H-bridge converter.

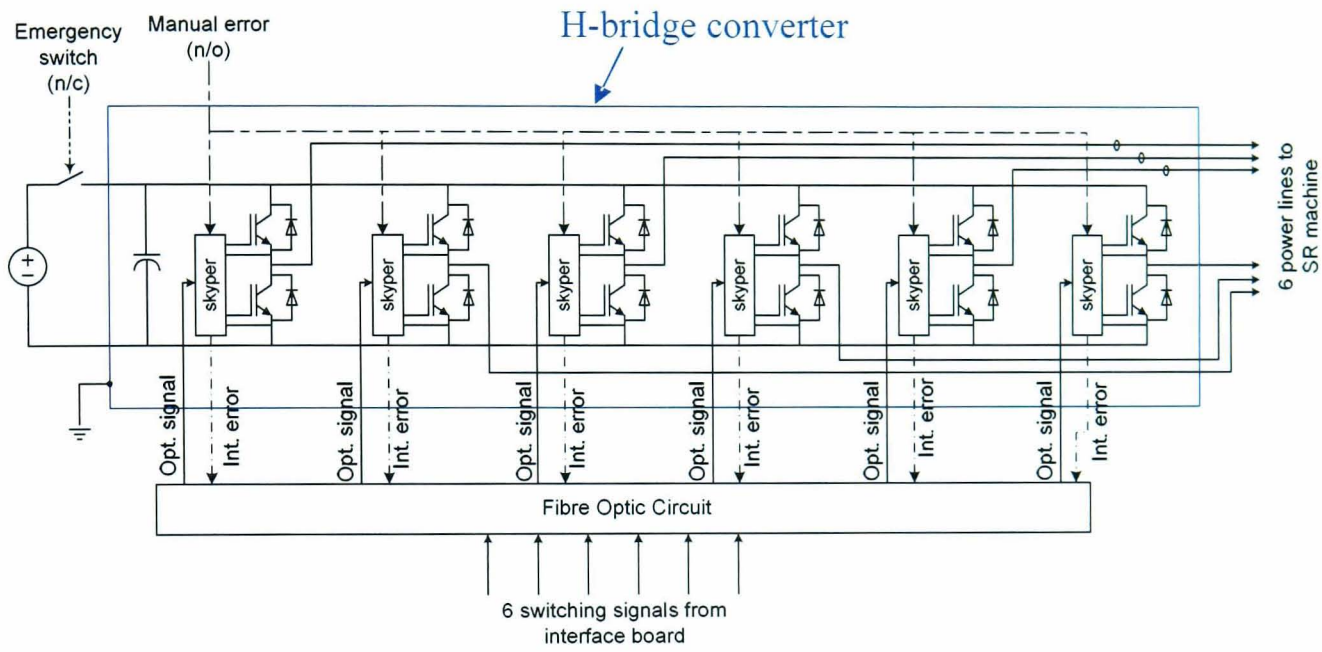
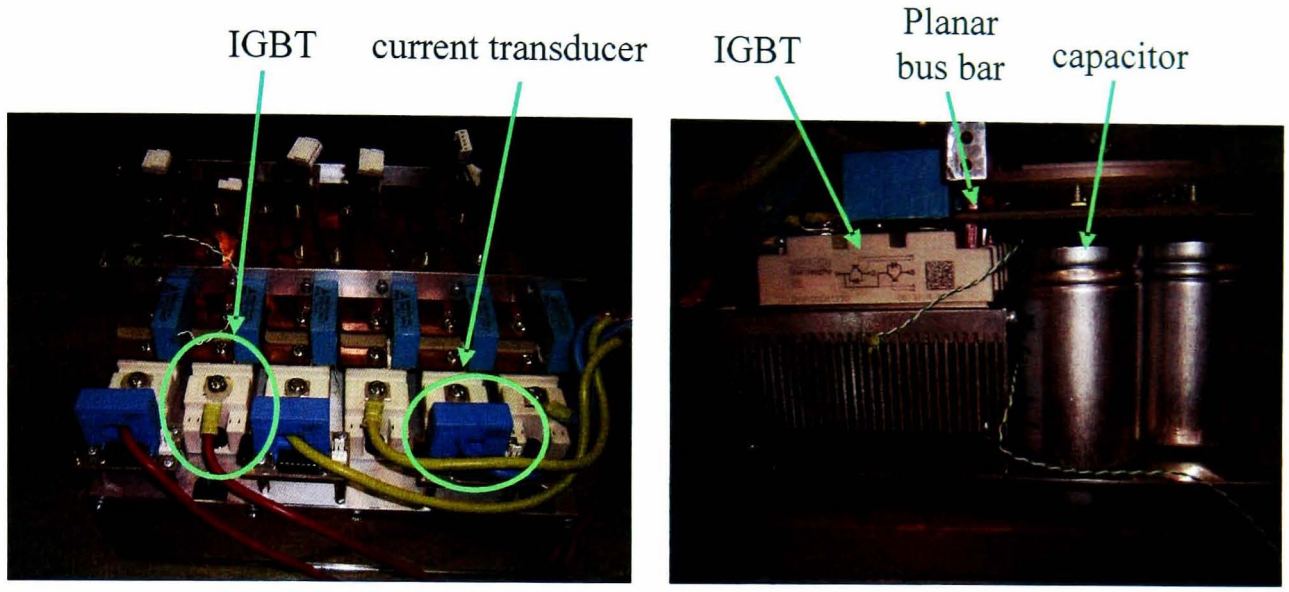


Figure 5.6: Fibre optic, H-bridge converter and dc supply diagram

The H-bridge converter in Figure 5.6 consists of 6 standard half bridge IGBT modules. Each module has 2 switches and 2 diodes. Only one active switch and one diode in each module are used to form an asymmetric H-bridge which drives one phase of the SR machine. Skyper, is the gate drive for the IGBT modules. The switching signals are transmitted to Skypers via the optic fibre and controlled turn-on and turn-off of the IGBTs.

The phase current transducers and the dc-link capacitors are also accommodated in the H-bridge converter box, as shown in Figure 5.7. In Figure 5.7(a), the current transducers are mounted to measure the phase current through the power cables from the IGBT modules. The dc-link capacitor bank in Figure 5.7 (b) is an existing hardware. It is made up of fixed 8×40μF (320μF) metal film-foil capacitors and installed next to the IGBT switches via two planar bus bars. This bus bar design makes it difficult to insert a dc-link current sensor. Instead, the dc-link current is reconstructed

from the measured phase currents. The dc-link current reconstruction circuit will be explained in the current control section.



(a) (b)

Figure 5.7: Current transducer (a) and dc-link capacitor (b)

5.2.3 Current Control

The current control block consists of 3 circuit boards. Since in the experiments, both of the HCC and DLCIC are implemented for the purpose of comparison, two control circuit boards are constructed for the two current control techniques, HCC and DLCIC. The other circuit board is built for the dc-link current reconstruction. The dc-link currents from both HCC and DLCIC are recorded, analysed and compared. The dc-link current is obtained from measured phase currents and switching signals, according to (5.1).

$$I_{dc} = \sum_{n=1,2,3} \left(- I_{phn} \cdot \overline{S_{1,n}} \cdot \overline{S_{2,n}} \right) + \left(I_{phn} \cdot S_{1,n} \cdot S_{2,n} \right) \tag{5.1}$$

where

I_{dc} is the calculated dc-link current.

I_{phn} is the measured phase n current.

$S_{1,n}$ is the logic state (1,0) of the upper switch in the phase n converter circuit.

$S_{2,n}$ is the logic state (1,0) of the lower switch in the phase n converter circuit.

Figure 5.8 shows the circuit block diagram of the dc-link reconstruction according to (5.1).

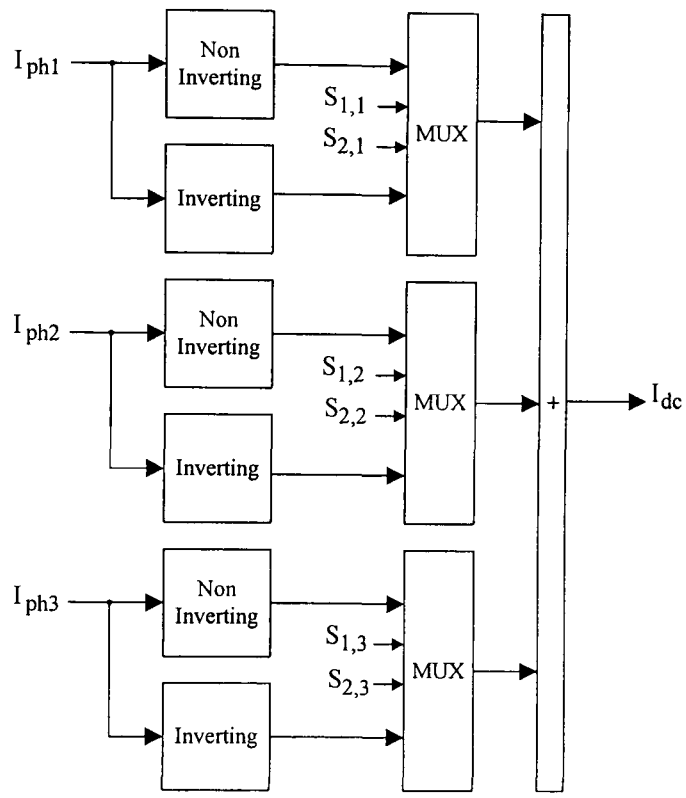


Figure 5.8: Circuit block diagram of dc-link current reconstruction

The phase currents and the switching signals are used to reconstruct the dc-link current. A phase current, which is always positive, is passed through a non-inverting and inverting circuits to obtain its positive and negative values. Next, the positive and negative phase currents are selected by a multiplexer (MUX) according to the switching logics of the phase converter. After that, contributions of each phase dc-link current are summed to provide the dc-link current of the SR drive.

For the current control board of HCC and DLCIC, they will be described in detail with speed controls in Section 5.3.

5.2.4 Speed Control

A real time control dSPACE system is used for the speed control loop for HCC and DLCIC. dSPACE consists of both hardware and software for the signals processing. Figure 5.9 shows the functional block diagram of the dSPACE system for the speed loop control. The hardware parts are DS5001, DS4002 and DS2101 which are Peripheral Component Interconnect (PCI) cards and are installed in a dSPACE case, as shown in Figure 5.10.

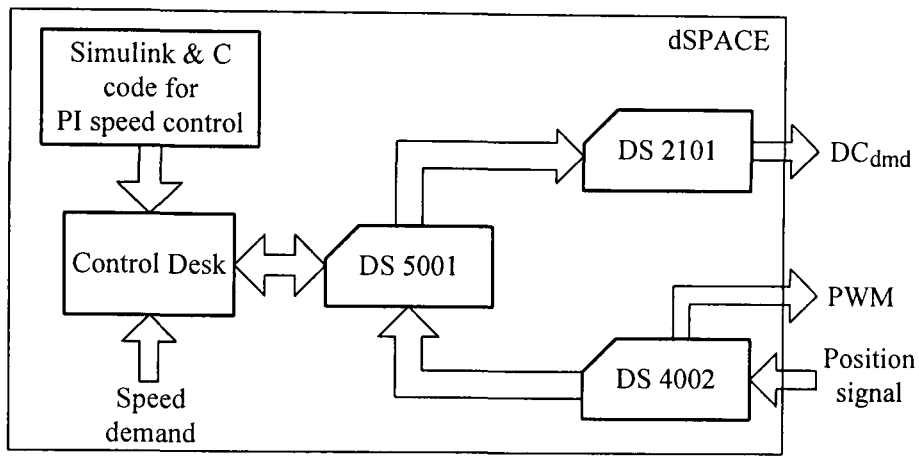


Figure 5.9: Functional block diagram of dSPACE platform

DS4002 is a timing and digital input - output (I/O) board which is equiped with an 8-channel BNC terminators. A position signal is fed through one of these channels to calculate the machine speed. DS4002 also generates the PWM signal for DLCIC. DS2101 is a digital to analog (D/A) conversion board which is connected with a 5-channel BNC terminal board. It generates analog signals for the phase current demand for HCC and the dc current demand for DLCIC. DS 5001 is the processor board that communicates wiht the PC via control desk user interface. The optic signal is used to connect DS 5001 card in the dSPACE case and the PC.

In the software parts for dSPACE, there are 2 programs involving. One is Matlab Simulink. The control programs are generated and recorded in Matlab via C code and Simulink. For examples, the speed calculation is programmed in C code, and the speed loop PI control is programmed in Simulink. Then, the programs are converted into a

real-time control mode. The other program is ControlDesk. The variables from the programs are observed and changed by ControlDesk program during the machine operation.

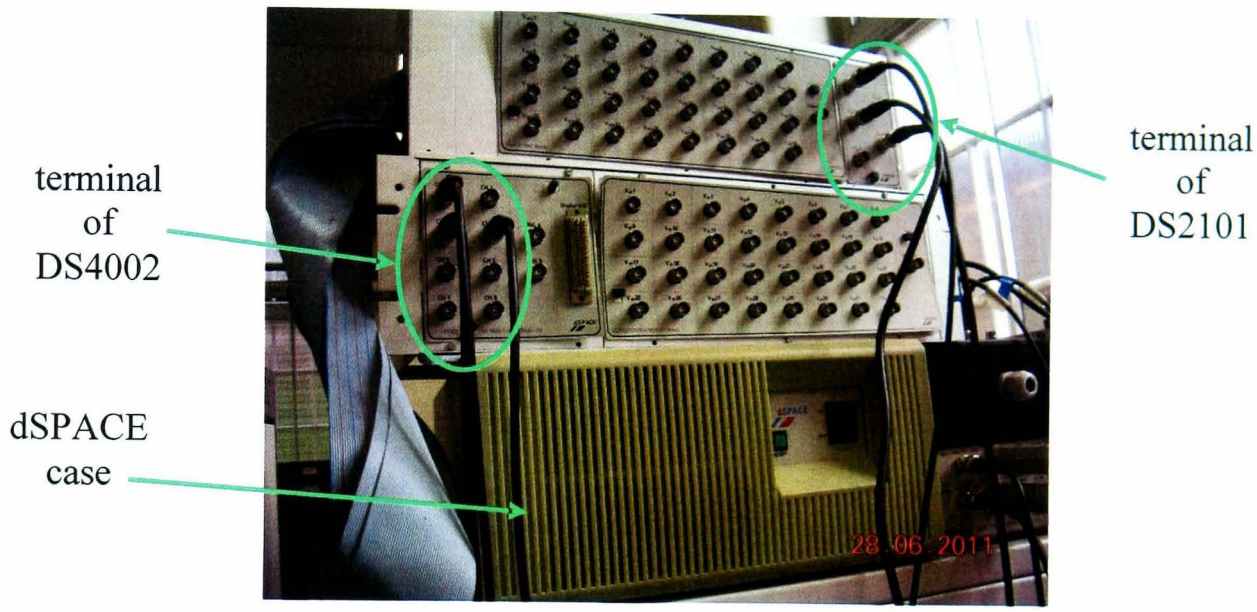


Figure 5.10: dSPACE and terminal board of DS4002 and DS2101

5.3 Current Control Schemes

Since the speed control and current control of HCC and DLCIC are different, the hardware of the current control board and the software of the speed control of both controls are separate.

5.3.1 Hysteresis Current Control (HCC)

Figure 5.11 shows the schematic diagram of HCC. For the speed loop control in dSPACE, one of the position signals is submitted to dSPACE via DS4002 which is used to calculate the machine speed. Then, the machine speed is fed to the PI control block in Simulink for the speed feedback. The PI block produces the demand torque to a look up table. The lookup table yields the phase current demand which is connected to analog signals by DS2101 as the input to the current control board.

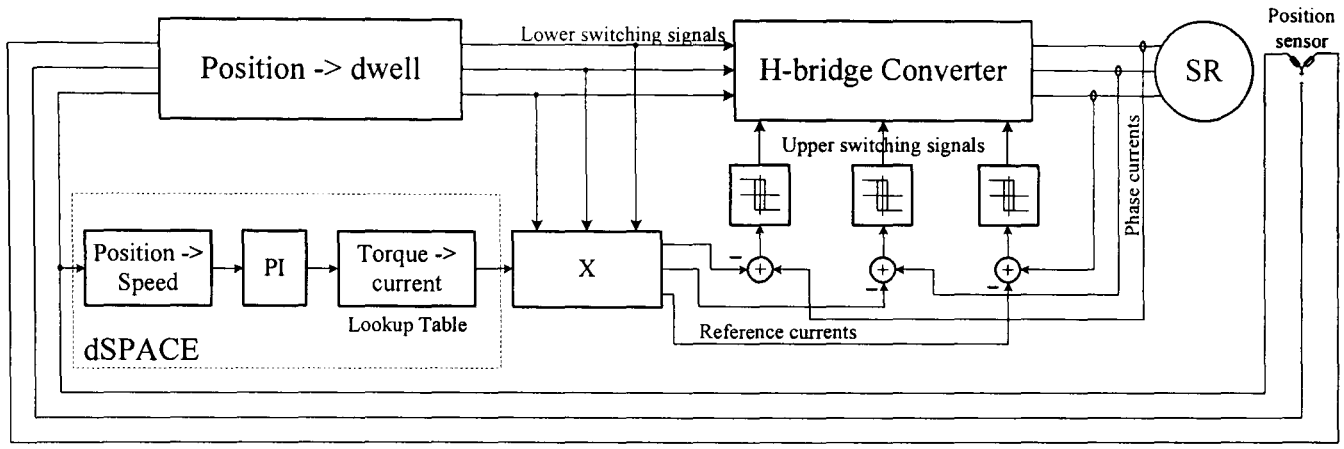


Figure 5.11: Schematic diagram of HCC

The phase currents of the HCC are controlled to swing within the hysteresis band in the soft chopping current control mode. Figure 5.12 shows the switch characteristic of soft chopping mode in the experiment. At the beginning, both the upper switch ($S_{1,n}$) and the lower switch ($S_{2,n}$) of a phase converter circuit are turned on. Then, the phase current flows into the machine winding, as shown in Figure 5.12 (a). When the phase current rises and reaches the upper level of the hysteresis band, the upper switch is turned off while the lower switch is still turned on. The phase current circulates within the phase winding, as shown in Figure 5.12 (b). The phase current drops until the lower level of the hysteresis band. Then, the upper switch is turned on again, as in Figure 5.12(a). The process is repeated until the rotor position is outside the dwell period with respect to the phase. Both upper switch ($S_{1,n}$) and lower switch ($S_{2,n}$) are turned off after the dwell angle is reached and the de-flux current is discharged via two diodes, as shown in Figure 5.12 (c).

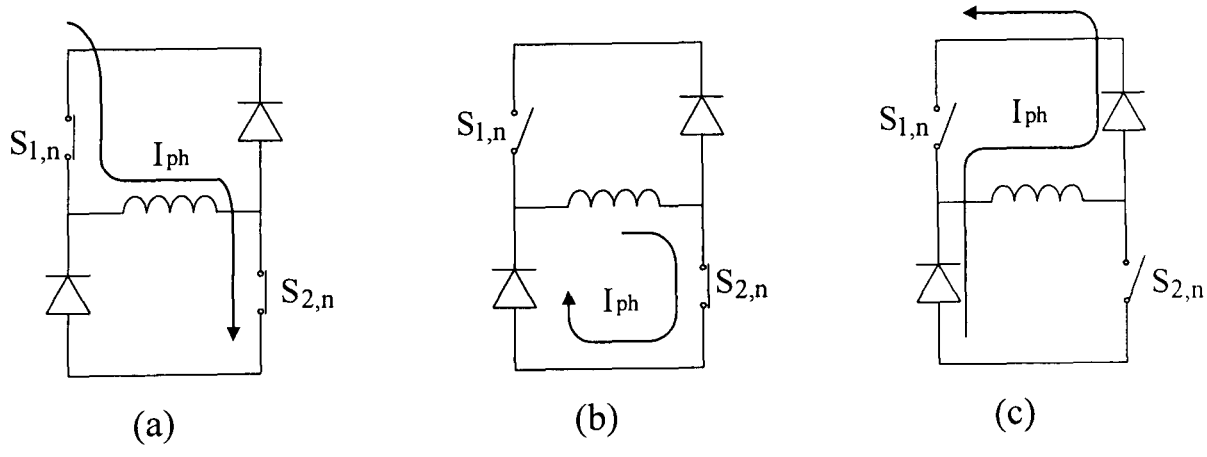


Figure 5.12: Switch characteristic of HCC

In the current control board, the switching signals for the upper switches and the lower switches are processed separately. The lower switching signals of the three phases are generated from the dwell signals, which are created from three-phase position signals, as described in Section 5.2.1. For the signals for the upper switches in Figure 5.11 the phase current demand from the dSPACE is multiplied by the dwell signals to form the reference currents for each phase. Then, those reference currents are compared with the actual phase currents in the hysteresis circuits. The upper switching signals for the three phases are obtained from the outputs of the hysteresis comparators.

The current control circuit board of the HCC is shown in Figure 5.13. Six BNC terminals at the bottom of the board are the output terminals of the six switching signals. Three BNC terminals on the left side of the board are the position signal inputs. The input of the measured phase currents are also on the left side of the HCC board. The measured phase currents are converted to voltage signals. They are also available at the phase current output terminals on the top of the HCC board, for the purpose of display in an oscilloscope.

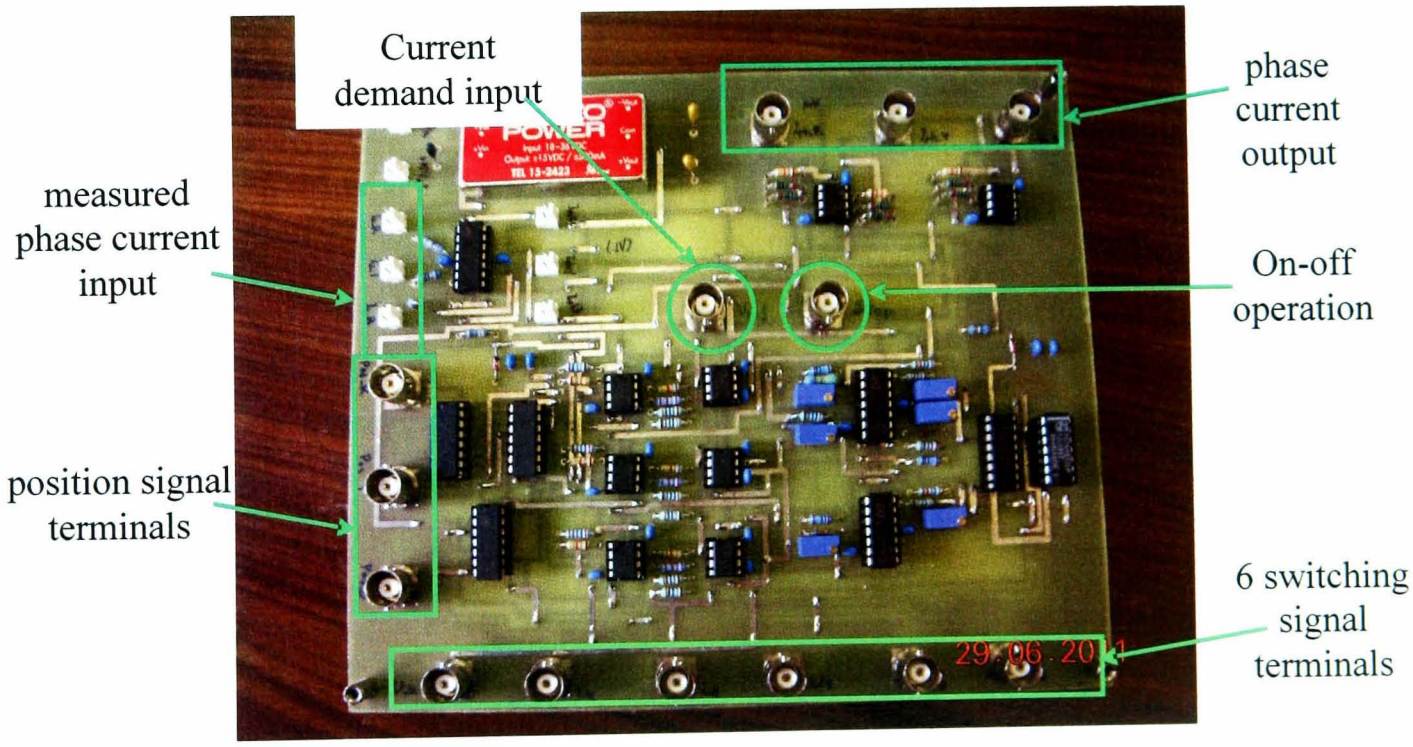


Figure 5.13: HCC current control circuit board

The phase current demand input is in the middle of the board. From the circuit design, the phase current demand is varied from 0 to 10 V, which is equivalent to 0 to 100 A of the actual phase current. The hysteresis band is designed at ± 3.5 A or ±0.35V, which is one twentieth of the rated current. The input terminal next to the phase current demand terminal is for enabling and disabling the machine operation. This signal is controlled from ControlDesk program via DS2101. The hysteresis circuit schematic is in Appendix B.

5.3.2 Dc-link Current Integration Control (DLCIC)

For dc-link current integration control (DLCIC), ideally the dc-link current should be directly measured and integrated over a switching PWM period, to determine the average of the dc-link current. Since the dc-link capacitors are connected to the converter with planar bus bars, it is difficult to insert a current transducer between the dc-link capacitor and the converter. Further, the use of an additional dc-link current transducer increases the cost. Instead, the dc-link current is obtained via a dc-link current reconstruction circuit. The resulting dc-link current average is processed to generate 6 switching signals, as shown in Figure 5.14.

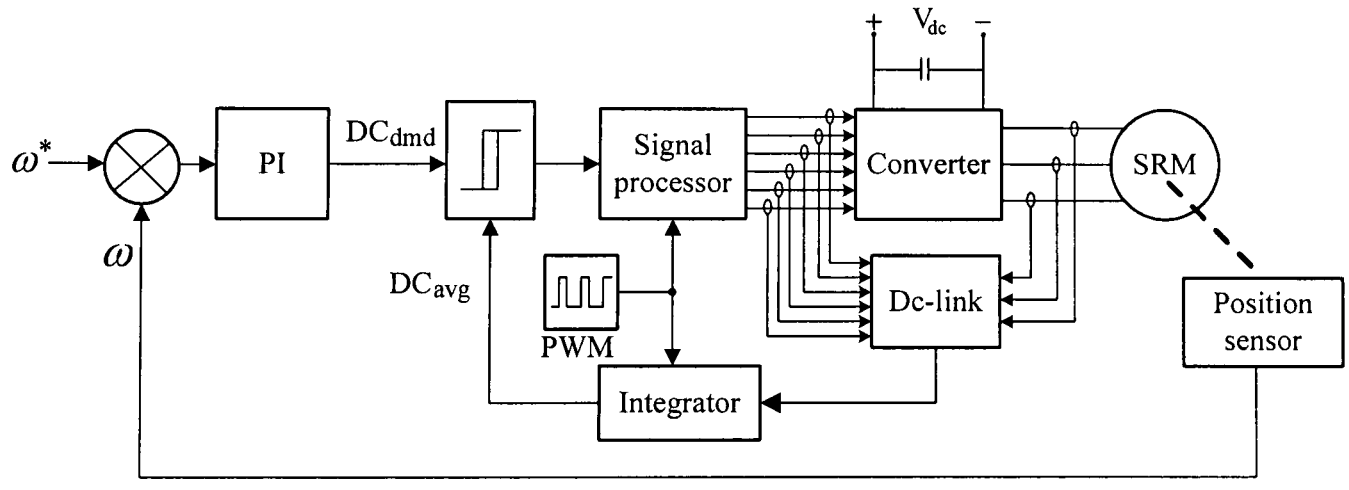


Figure 5.14: Control diagram of DLCIC

Figure 5.15 shows the block diagram of DLCIC with a dc-link current reconstruction circuit in detail. The block diagram in Figure 5.15 is described in 4 modules: the dSPACE, dc-link current control, upper switching signals, and lower switching signals.

The function of dSPACE for the DLCIC is similar to that for the HCC. DS4002 acquires the position signals, calculates the machine speed and generates the dc-link current demand. Furthermore, the dSPACE also generates PWM signals for the DLCIC and a reset signal for the integrator circuit.

The dc-link current control module is composed of the dc-link current reconstruction circuit, the integrator circuits, and the comparator circuits which are grouped in Figure 5.16. The function of this module is to produce turn-on and turn-off signals for the upper switching signal module.

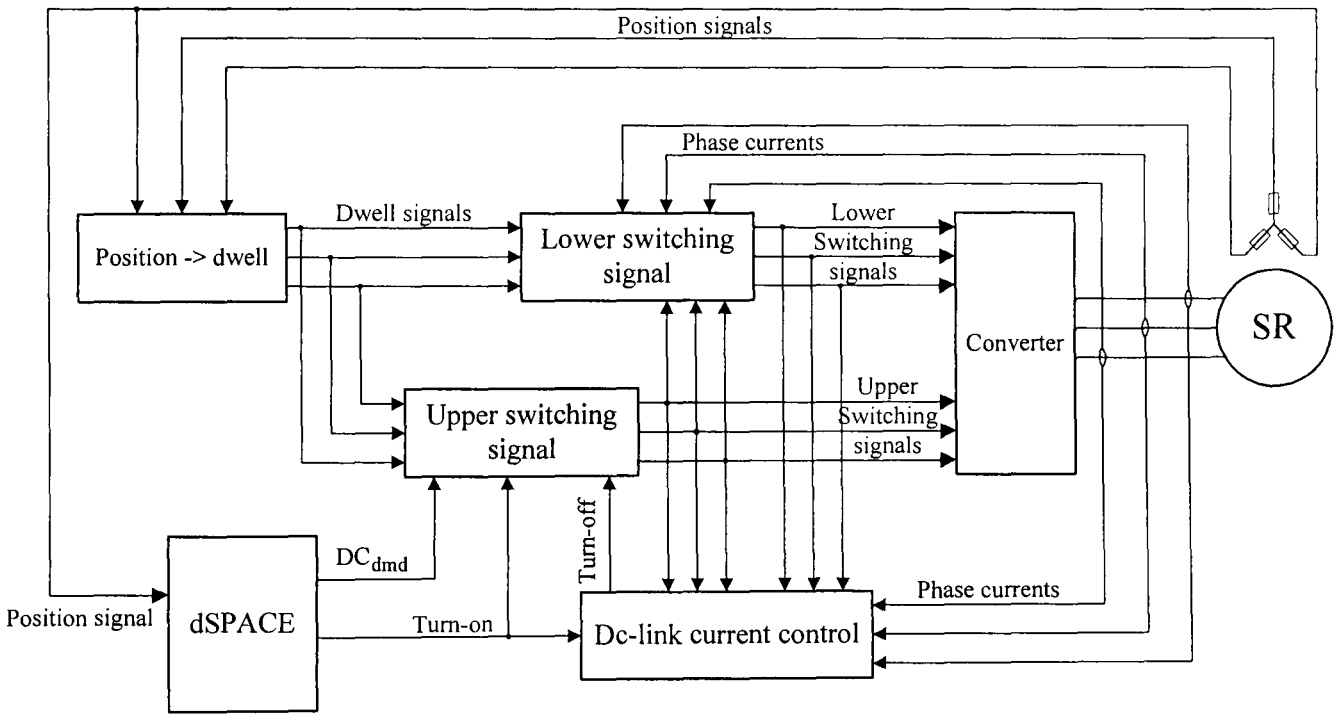


Figure 5.15: Module block diagram of DLCIC

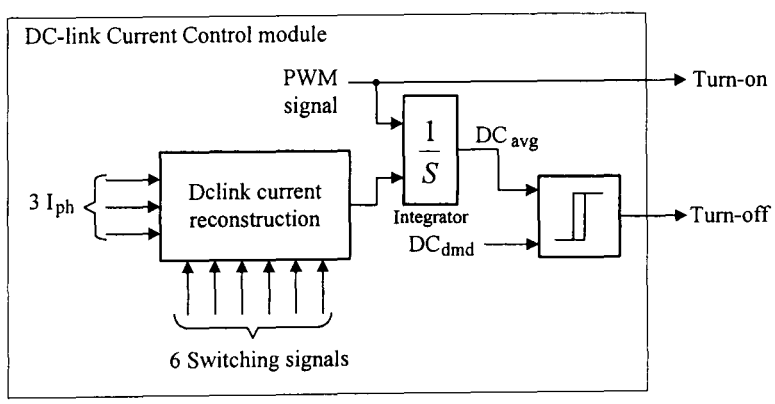


Figure 5.16: Dc-link current control module

The average dc-link current from the integrator is the average value of each switching period since the integrator is reset in every switching period by a PWM signal from dSPACE. Although turn-on signal and reset signal for the integrator in Figure 5.16 are ideally from the same source, they are not exactly the same in the experiment since the reset signal of the integrator in the experiment, ACF2101, is the inverse of the turn-on signal. Furthermore, if the reset signal of the integrator and the turn-on signal were the same signals, turn-off signal would slightly overlap with turn-on signal. This will effect the accuracy of the average dc-link current. Thus, the reset signal of the integrator is designed to slightly lead turn-on signal, around 2.5 μs, as shown in Fig 5.17, to ensure that the integrator is zeroed before the next PWM cycle. The switching signal period (T) is 100 μs.

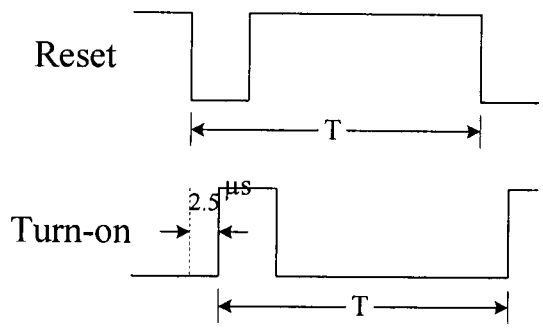


Figure 5.17: Turn-on and integrator reset signal

The reconstructed dc-link current is integrated to form the average dc-link current (DC_{avg}). Then, it is compared with the dc current demand (DC_{dmd}) and Turn-off signal is generated after the comparator.

The turn-on and turn-off signals from the dc-link current control module are transferred to the upper switching signal module which generates the switching signals for the upper switches in the converter circuit. The circuit diagram of the upper switching signal module is in Figure 5.15. The upper switch in each phase of the converter circuit controls the phase current. The truth table of the upper switching signal ($S_{I,n}$) is shown in Table 5.1.

Table 5.1 Truth table of upper switching signal

dwell	Turn-on	Turn-off	$S_{1,n}(t)$	$S_{1,n}(t+1)$
0	x	x	x	0
1	↑	x	0	1
1	x	↑	1	0

During the dwell period, the lower switch is always turned on while the upper switch is turned on and turned off repeatedly to control the average dc-link current. Outside the dwell signal, the upper switch is always turned off while the lower switch is turned on and turned off to control the phase current. Hence, the upper switch of the converter is enabled to operate during when the dwell signal is high.

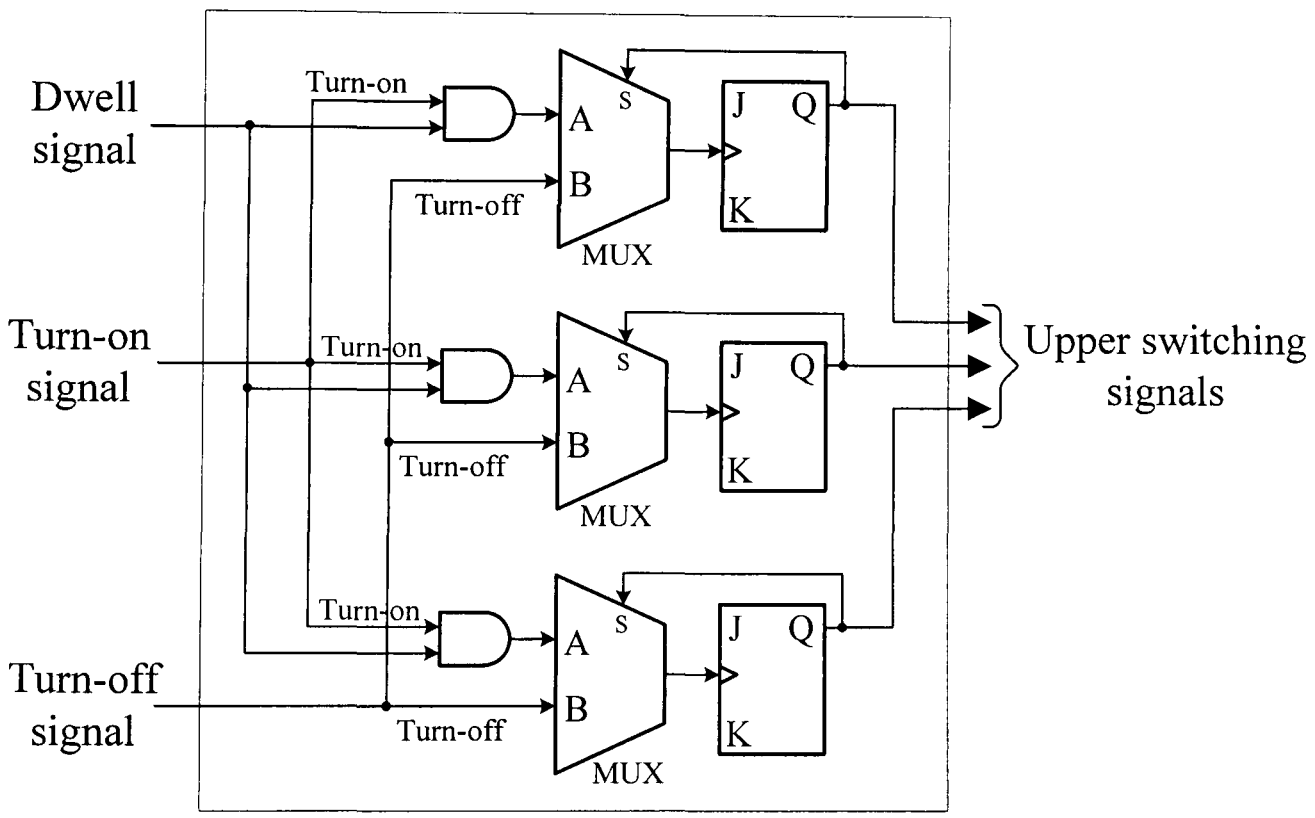


Figure 5.18: Upper Switching module

Figure 5.18 shows the upper switching signal circuit. The J-K flip-flop is set to be a toggle flip-flop (T flip-flop). If the logical state of pin Q is low, the next logical state will be high and vice versa after the clock signal. Pin Q of J-K flip-flop is connected to the selecting pin (pin s) of the multiplexers (MUX). If the logical state of pin S is low, the signal from pin A is selected to be the output of the MUX. The signal at pin A is

combined with the dwell signal and the turn-on signal. If the dwell signal is high, the turn-on signal will be an output of the MUX and will be the clock signal for the J-K flip-flop. When the flip-flop is activated by the rising edge of the turn-on signal, the Q state will be changed from low to high. The upper switching signal is high and the signal at pin S is also high. If the signal of pin S is high, the output of the MUX is selected from pin B, which is turn-off signal. When the rising edge of the turn-off signal arrives, the state Q will be set to low. The upper switching signal is low. The next cycle of the upper switching signal begins.

Without the dwell signal, the logical state of pin Q and pin S is low, the signal from pin A, which is selected to be the MUX output, is low due to the low state of the dwell signal. So, there is no rising edge for the clock of the flip-flop and there is no change in the upper switching signal. If the logical state of pin S is high without the dwell signal, the turn-off signal from pin B will be selected. Then, the upper switch is turned off until the next dwell signal.

The function of the lower switching signal, as stated previously, is to control the de-fluxing phase current during a phase commutation period synchronously with the rise of the incoming phase current. This is done to prevent the negative dc-link current. Thus, this control begins when the dwell signal becomes zero, the lower switch is still turned on while the upper switch of the outgoing phase is turned off. The outgoing phase current is freewheel until the incoming phase current is greater than the outgoing phase current. Subsequently, the outgoing phase current is discharged as the incoming phase current is charged. Thus, the lower switch of the outgoing phase is turned off when the upper switch of the incoming phase is turned on. These process can be summarised into 7 steps, A - G. Table 5.2 describes an example for the lower switching signal of phase1.

Table 5.2 Conditions and state variables of lower switching signal of phase1

Condition	Description
A	▪ When the logical state of the phase1 dwell signal is true (*dwell1* = 1), the lower switch is turned on, i.e., $S_{2,1} = 1$; ▪ else, go to condition B.
B	▪ *dwell1* = 0. ▪ If the phase current of phase1 is higher than zero ($I_{ph1} > 0$), go to condition C. ▪ If the phase current is equal to or less than zero, the lower switch is turned off, i.e., $S_{2,1} = 0$.
C	▪ *dwell1* = 0 and $I_{ph1} > 0$. ▪ If the logical state of the dwell signal of phase2 (*dwell2*) is true (*dwell2* = 1) , go to condition D; ▪ else, go to condition F.
D	▪ *dwell1* = 0, $I_{ph1} > 0$, and *dwell2* = 1. ▪ If the phase current of phase2 ($I_{ph,2}$) is higher than the sum of the phase1 current ($I_{ph,1}$) and phase3 current ($I_{ph,3}$), i.e., $I_{ph2} > I_{ph1} + I_{ph3}$, the lower switch is turned off, i.e., $S_{2,1} = 0$; ▪ else, go to condition E.
E	▪ *dwell1* = 0, $I_{ph1} > 0$, *dwell2* = 1, and $I_{ph2} < I_{ph1} + I_{ph3}$. ▪ If the upper switching signal of phase2 is turned on ($S_{1,2} = 1$), the lower switch of phase1 is turned off, i.e., $S_{2,1} = 0$; ▪ else, the lower switch of phase1 is turned on, i.e., $S_{2,1} = 1$, and the phase1 current flows freewheeling.
F	▪ *dwell1* = 0, $I_{ph1} > 0$, and *dwell2* = 0. ▪ If the dwell signal of phase3 is true (dwell3 = 1) , go to condition G. ▪ else, the lower switching signal is false ($S_{2,1} = 0$). This condition occurs when the amplitude of the demand current is zero.

Condition	Description
G	▪ *dwell1* = 0, $I_{ph1} > 0$, *dwell2* > 0, and *dwell3* = 1. ▪ If the upper switching signal of phase3 is true ($S_{1,3}$ = 1), the lower switch of phase1 is turned off, i.e., $S_{2,1}$ = 0. The de-fluxing current of phase1 is discharged to phase3 winding. ▪ else, the lower switching signal is true ($S_{2,1}$ = 1), and the phase1 current flows freewheeling.

From the state variables and the description in Table 5.2, the truth table of lower switching signal of phase1 is obtained in Table 5.3.

Table 5.3 Truth table of lower switching signal of phase1

A	B	C	D	E	F	G	$S_{2,1}$
1	x	x	x	x	x	x	1
0	0	x	x	x	x	x	0
0	1	1	1	1	x	x	0
0	1	1	1	0	x	x	1
0	1	1	0	x	x	x	1
0	1	0	x	x	1	1	0
0	1	0	x	x	1	0	1
0	1	0	x	x	0	x	0

where 'x' is don't care signal which can be true or false. The logic state equation of the lower switching signal is described as (5.2).

$$S_{2,1} = A + B \cdot [C \cdot (\overline{E} + \overline{D}) + \overline{C} F \overline{G}] \tag{5.2}$$

Figure 5.19 shows the logic diagram of the lower switching signal of phase1. Similar circuits can be derived for the lower switching signal of phase2 and phase 3, except the phase number. If the circuit in Figure 5.19 will be changed from phase1 to phase2, the

phase number is shifted from phase1 to phase2, phase2 to phase3 and phase3 to phase1. For examples, the phase current of phase1 (I_{ph1}) in Figure 5.18 is replaced by I_{ph2}. The lower switching circuit of phase1 ($S_{2,1}$) is replaced by that of phase2 ($S_{2,2}$). The dwell signal of phase2 (*dwell2*) is replaced by that of phase3 (*dwell3*) and the dwell signal of phase3 (*dwell3*) is replaced by that of phase1 (*dwell1*). The current control board of the DLCIC is shown in Figure 5.20 and the detail of DLCIC circuit schematic is in Appendix A.

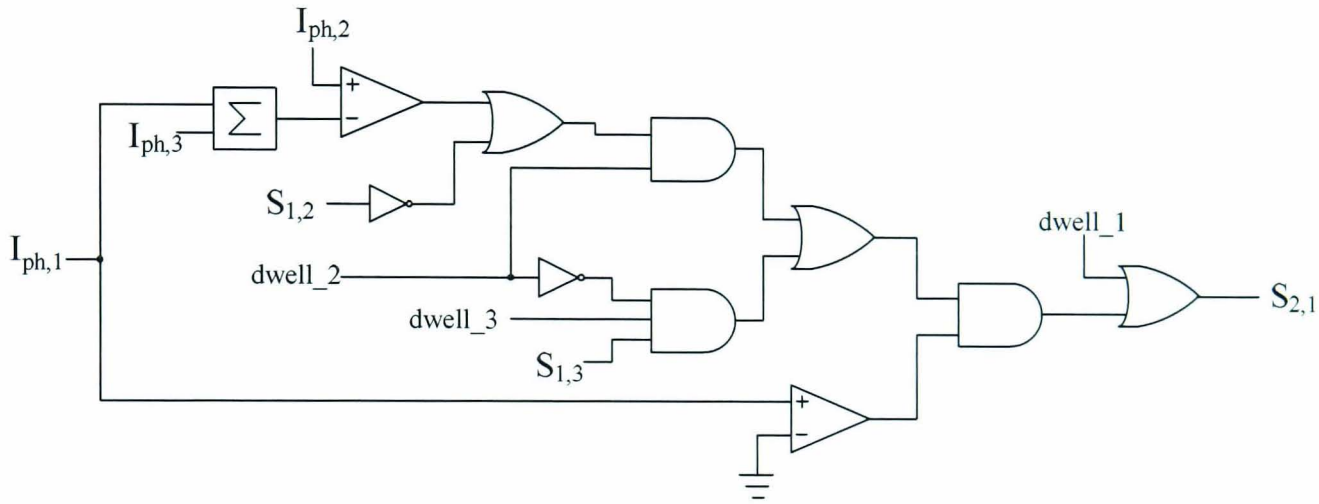


Figure 5.19: Logic circuit diagram of lower switching signal of phase1

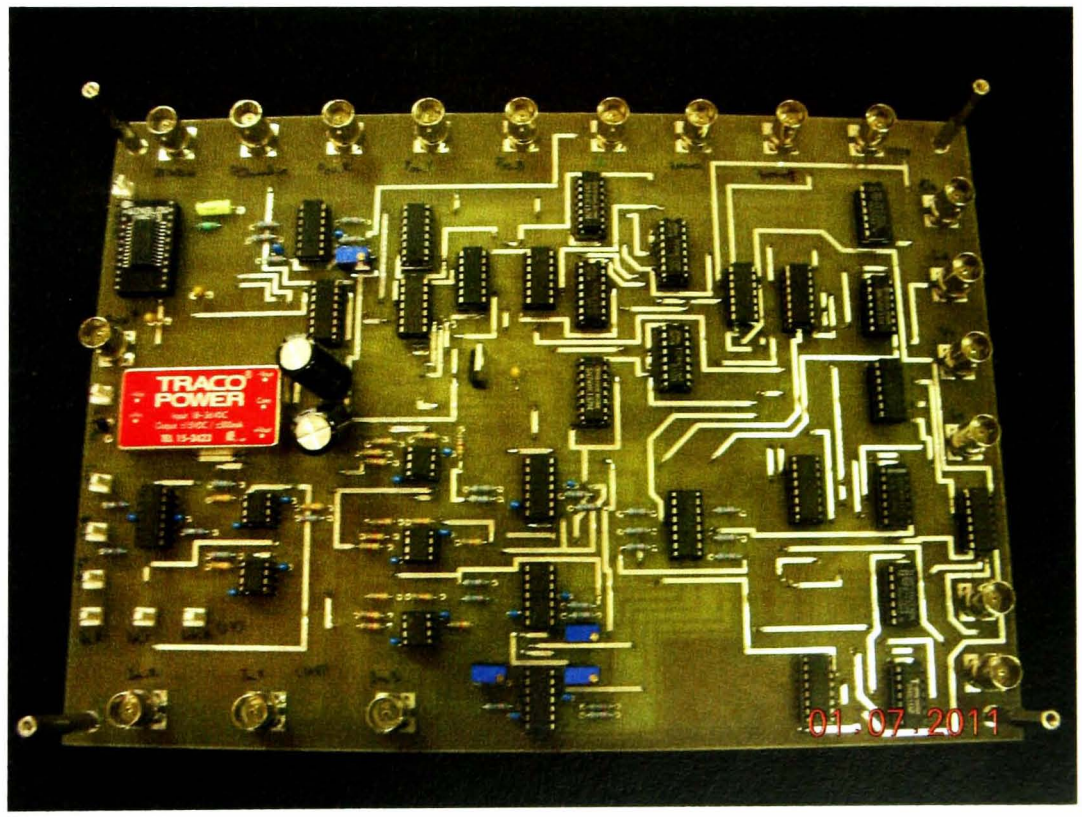


Figure 5.20: DLCIC current control circuit board

5.4 Experimental Results

Since the operation speed of DLCIC is 100 - 3000 rpm which is determined already in Chapter3, the experimental tests are designed to accomplish DLCIC and HCC at the speeds 100, 500, 1000, 2000, and 3000 rpm and at the maximum torque of the load machine, 4 Nm. The turn-on angle and turn-off angle are constant at 3° and 18° respectively.

Dwell signals (*dwell*), phase current (I_{ph}), the dc-link currents (I_{dc}), the capacitor voltage (V_C), the input current (I_{in}) and the machine torque (T) are measured during the experiment. Figure 5.21 shows the supply circuit and the SR machine. It indicates where the measure signals are. The input resistor and the input inductor represent the parasitic resistance and inductance of the power cables.

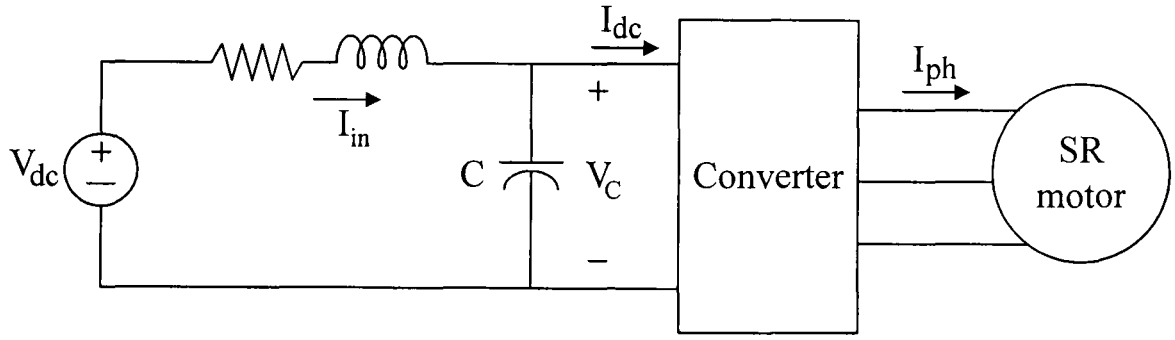


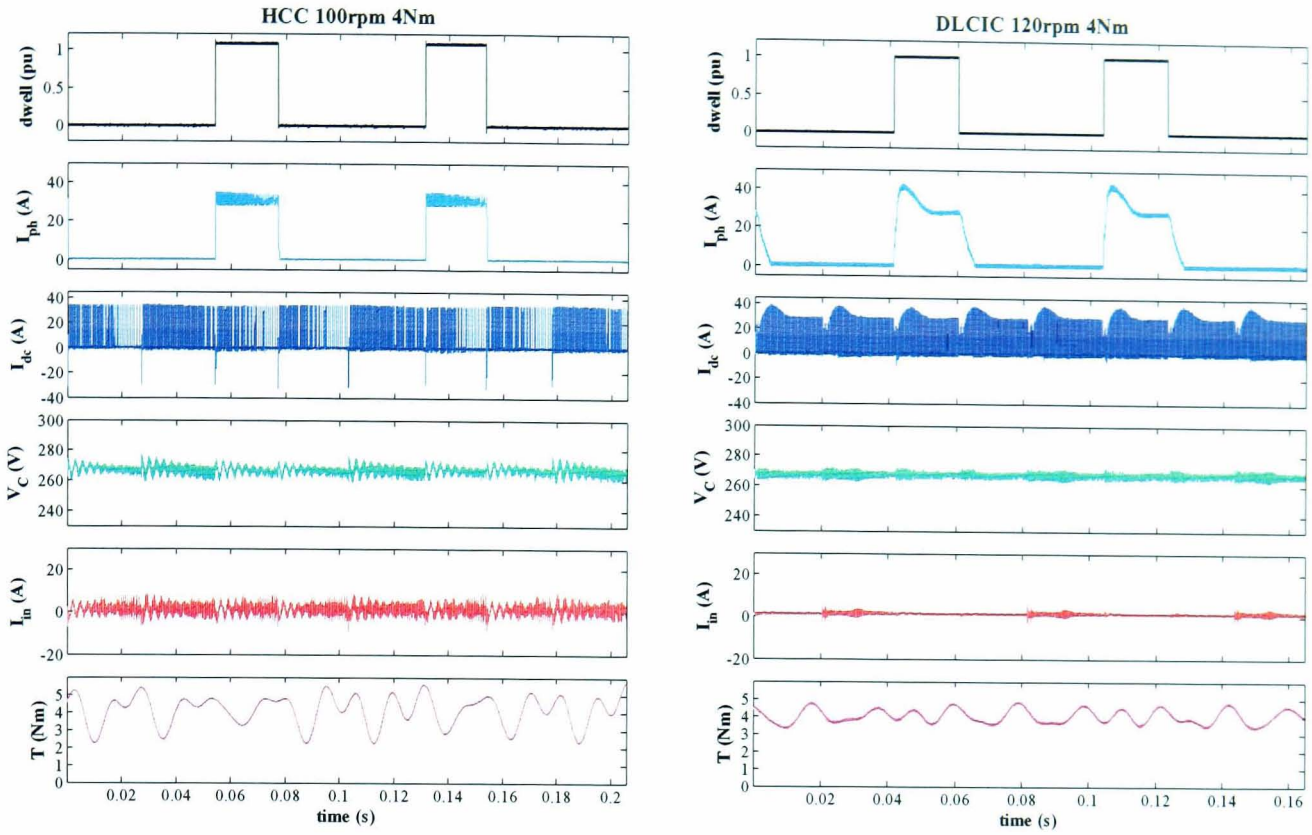
Figure 5.21: Places of the measured signals

In the experiment, the SR machine is coupled with a dynamometer and the operation starts with the speed control from the SR machine with zero load torque. The operation starts from 0 rpm and reaches the demand speed under speed feedback control. Then, the load torque is gradually added up to the demand torque and the resultant signals are recorded. All of the measured signals are recorded by Yokokawa Digital Scope DL750 with a sampling rate at 10 MHz. The dwell signal, the phase current and the dc-link current are brought from the control board to the scope. The dc-link capacitor voltage is read by a high bandwidth voltage differential probe, Tektronix P3210. The input current is observed by AC/DC current probe, Tektronix TCPA300. The machine torque

is measured by a torque transducer, Magtrol TMHS 306, of which the sensitivity is 1V/Nm.

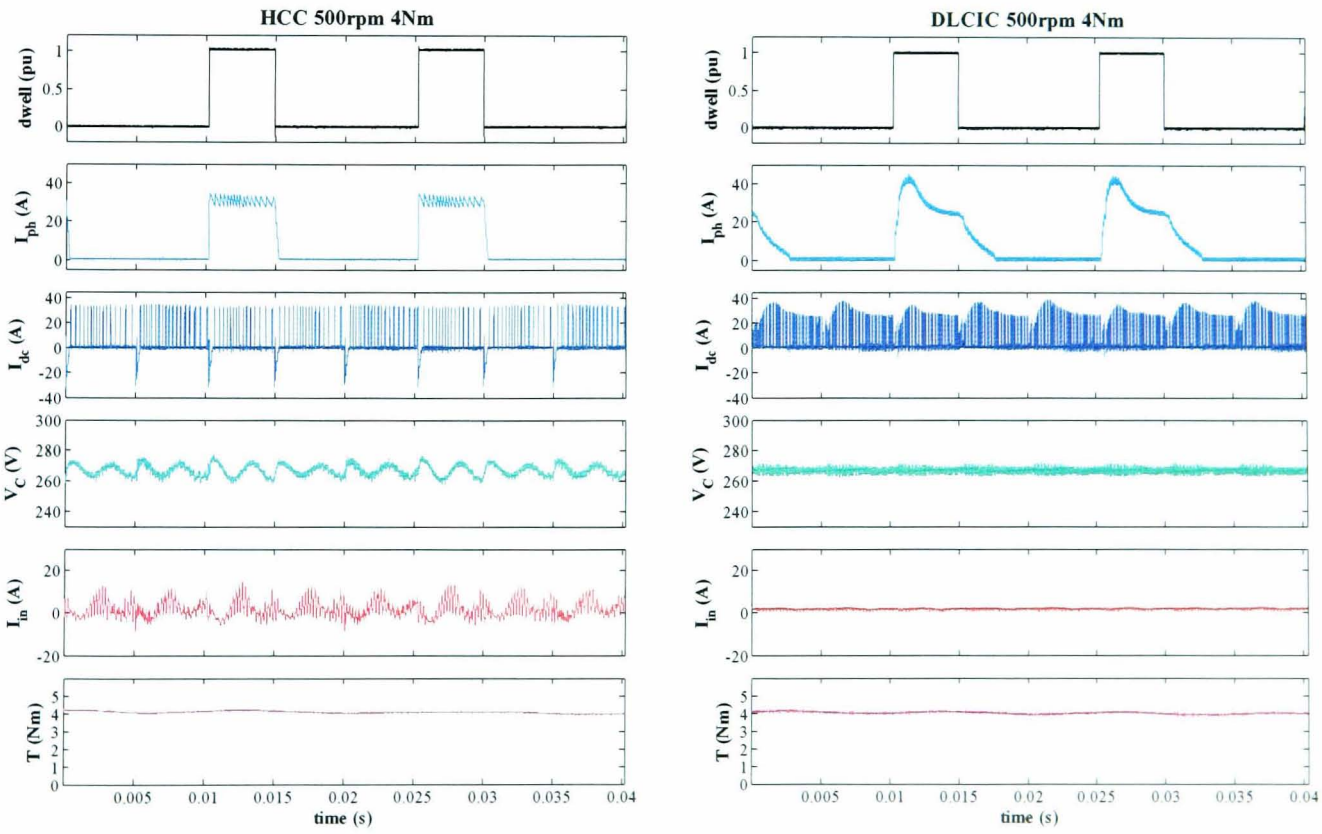
Figure 5.22 to Figure 5.26 represent the experimental results of both techniques, the HCC and the DLCIC, at 4Nm load torque, and 100, 500, 1000, 2000, and 3000 rpm, respectively. The phase currents of DLCIC during the dwell period are different from those of HCC. At the beginning of the dwell period, the phase currents of DLCIC are higher than those of HCC since the dc-link current and the outgoing phase current feed the active phase current. All of the outgoing phase current is fed to the incoming phase to prevent the negative dc-link current.

For the capacitor voltages in all of these figures, the peak to peak values or the voltage ripple of the dc-link capacitor voltages from the HCC are higher than those from DLCIC at the same speed. For example, at 3000 rpm the voltage ripple of HCC is 20.7 V and that of DLCIC at the same speed is 11.3V. The difference is about 50%. This is the results of the constant energy transfer during a switching period. Not only the voltage ripple of the dc-link capacitor is reduced, the ripple of the input current is also reduced. The input currents (I_{in}) from DLCIC are much less fluctuated than that from the HCC. Table 5.4 presents the peak to peak details of the dc-link capacitor voltages and the peak-to-peak of the supply current at various speeds.



(a) (b)

Figure 5.22: Experimental results at 100 rpm



(a) (b)

Figure 5.23: Experimental results at 500 rpm

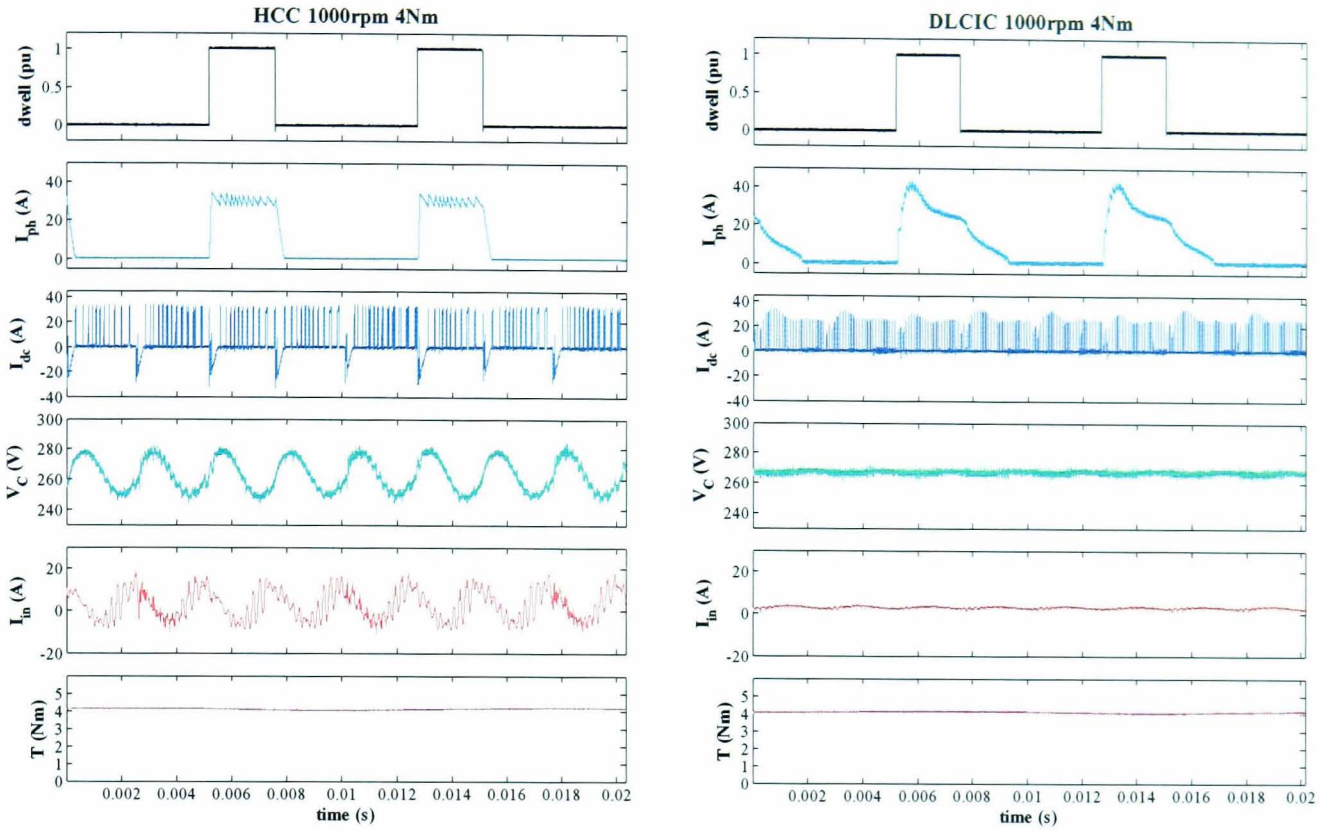


Figure 5.24: Experimental results at 1000 rpm

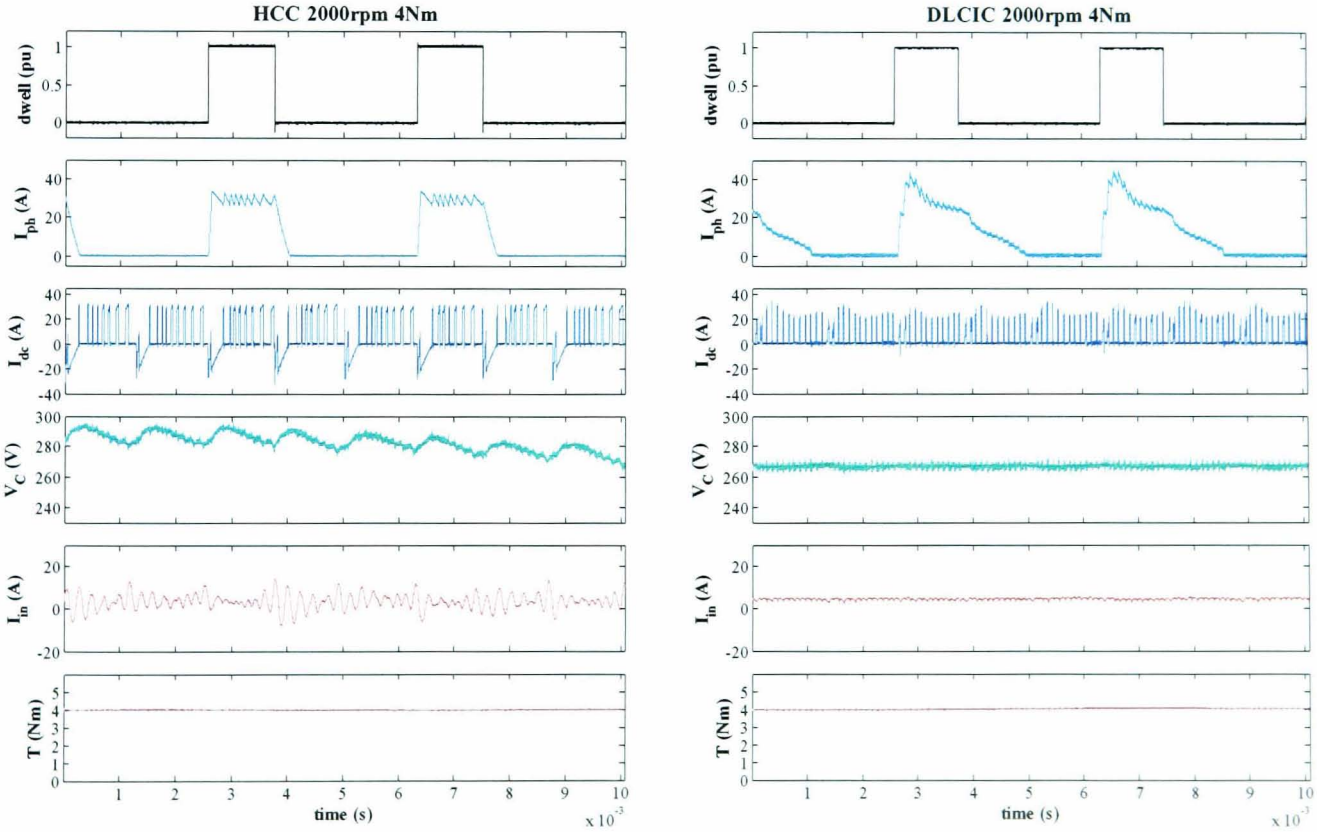


Figure 5.25: Experimental results at 2000 rpm

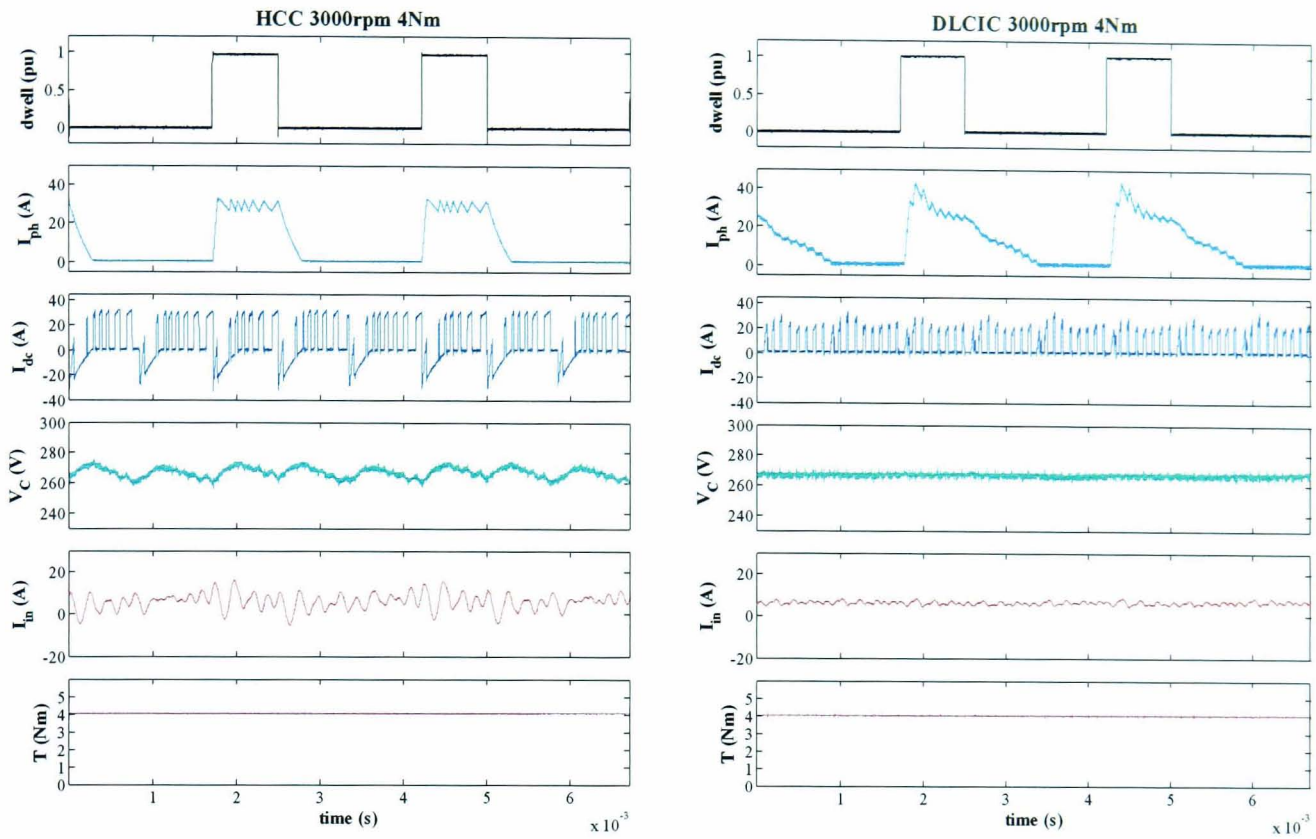


Figure 5.26: Experimental results at 3000 rpm

Table 5.4 Peak to peak capacitor voltage and supply current of HCC and DLCIC

speed (rpm)	Voltage ripple (V)		Supply current ripple (A)	
	HCC	DLCIC	HCC	DLCIC
100	18.3	14.0	20.58	10.17
500	23.0	11.7	24.42	2.67
1000	40.6	12.0	31.1	3.58
2000	40.7	11.0	30.08	3.5
3000	20.7	11.3	22.08	5.17

From Figure 5.25, it can be seen that the capacitor voltage (V_C) is slightly inclined. If the time range of the graph is extended, as shown in Figure 5.27, it is seen that the capacitor voltage is fluctuated at a frequency lower than the commutation frequency. This fluctuation is likely caused by the interaction between the non-ideal power supply

and the speed loop control since the frequency of the voltage fluctuation is 40 Hz which is equal to the speed loop control bandwidth. Due to this fluctuation, the supply current spikes tripped the supply as the peak supply current was over the current protection level. The experimental results cannot be recorded.

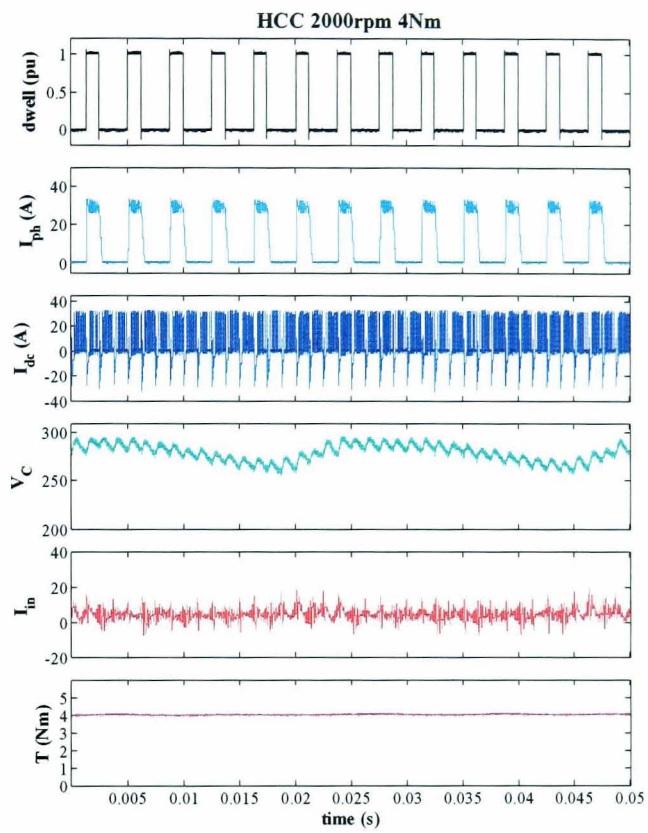


Figure 5.27: Fluctuation of capacitor voltage at 2000 rpm

The supply voltage has to increase from 270V to 290V to improve stability [5.1] and to reduce the peak-to-peak of the supply current. Since the motor operates with a constant torque and a constant speed which is similar to the constant power load, when the voltage is increased, the current is consequently decreased [5.2 -5.7]. The supply voltages in Figs. 5.24 and 5.26 are 290V. Although the capacitor voltage ripple is slightly reduced due to an increase of the supply voltage, the peak-to-peak voltage of DLCIC in Figure 5.25 is still much lower than that of the HCC at the same speed.

The effect from input filter interaction with the speed loop also shows in the HCC results at 1000 rpm. It is seen that the capacitor voltage ripple and the input current ripple are high, but their magnitudes are not too large to be unable to trip the power

supply. The control bandwidth of the speed loop affects significantly the experimental results of HCC in the speed range of 1000 - 2000 rpm. However, it almost does not affect the experimental results of DLCIC.

The problem of DLCIC occurs at the speed of 100 rpm. The phase current suddenly increases and this causes the power supply tripped. The experimental results of DLCIC at 100 rpm cannot be recorded due to the supply tripping. The rotor rotates in steps and the speed is not smooth. This causes the spikes in the phase current of DLCIC at 100 rpm. Hence, to prevent the spikes, the machine speed has to be increased from 100 rpm to around 120 rpm to smooth the speed. Thus, the experimental results are recorded via the oscilloscope. However, this problem should be avoided if the dynamometer operates in speed control mode, and the SR drive under tests in torque control modes.

Since many experimental results are affected by the speed loop problem, simulations of the experimental conditions are performed for the simulation model validation. The simulation conditions are chosen from the experiment at 3000 rpm which are least affected by the speed loop control problem. The simulations are performed by assuming that the machine rotates at a constant speed, 3000 rpm, without the speed ripple. Figure 5.28 shows the simulation block diagram. The inductance and resistance of the filter are estimated from the parasitic inductance and resistance and the internal inductance and resistance of the power supply. They are 100 μH and 0.2Ω since the length of the supply cable is 25 m and meanders through the laboratory. The inductance is approximated as (5.2) [5.8].

$$L = 0.002l\left[\ln\frac{4l}{d} - 1 + \frac{\mu}{4}\right] \tag{5.2}$$

where

d is the diameter of the cable.

l is the length of the cable.

μ is permeability of the conductor which is around 1.

Figure 5.29 and Figure 5.30 compares the experimental results and the simulation results from the HCC and DLCIC.

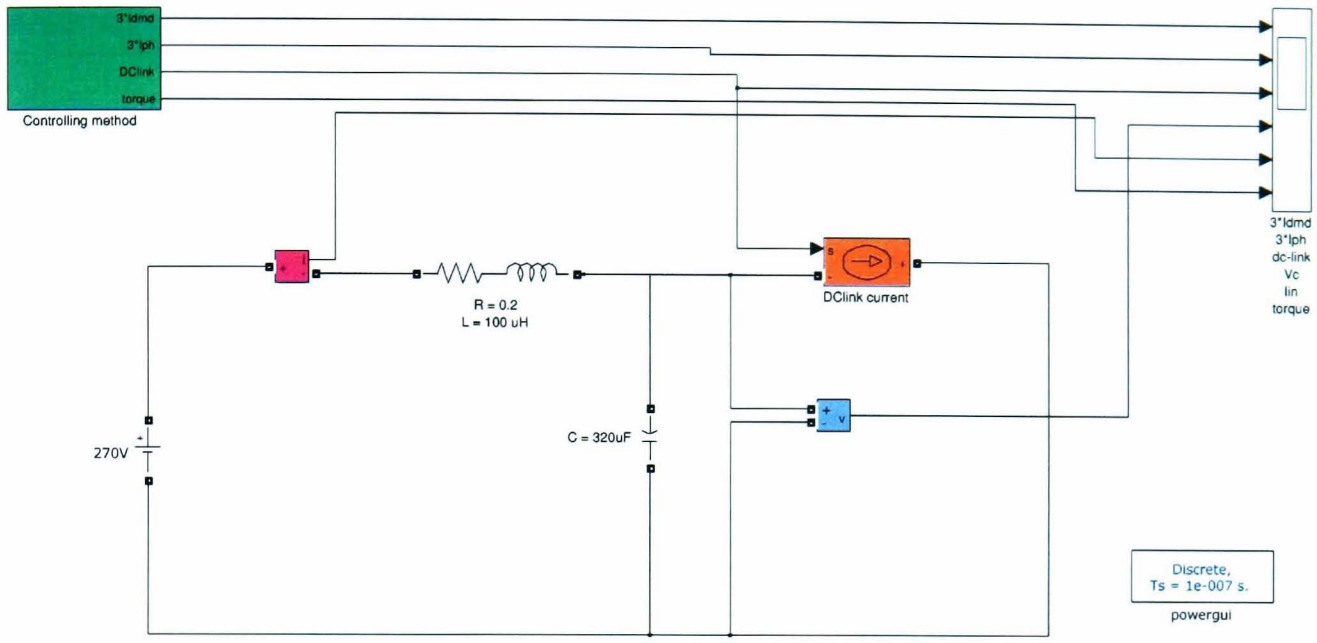
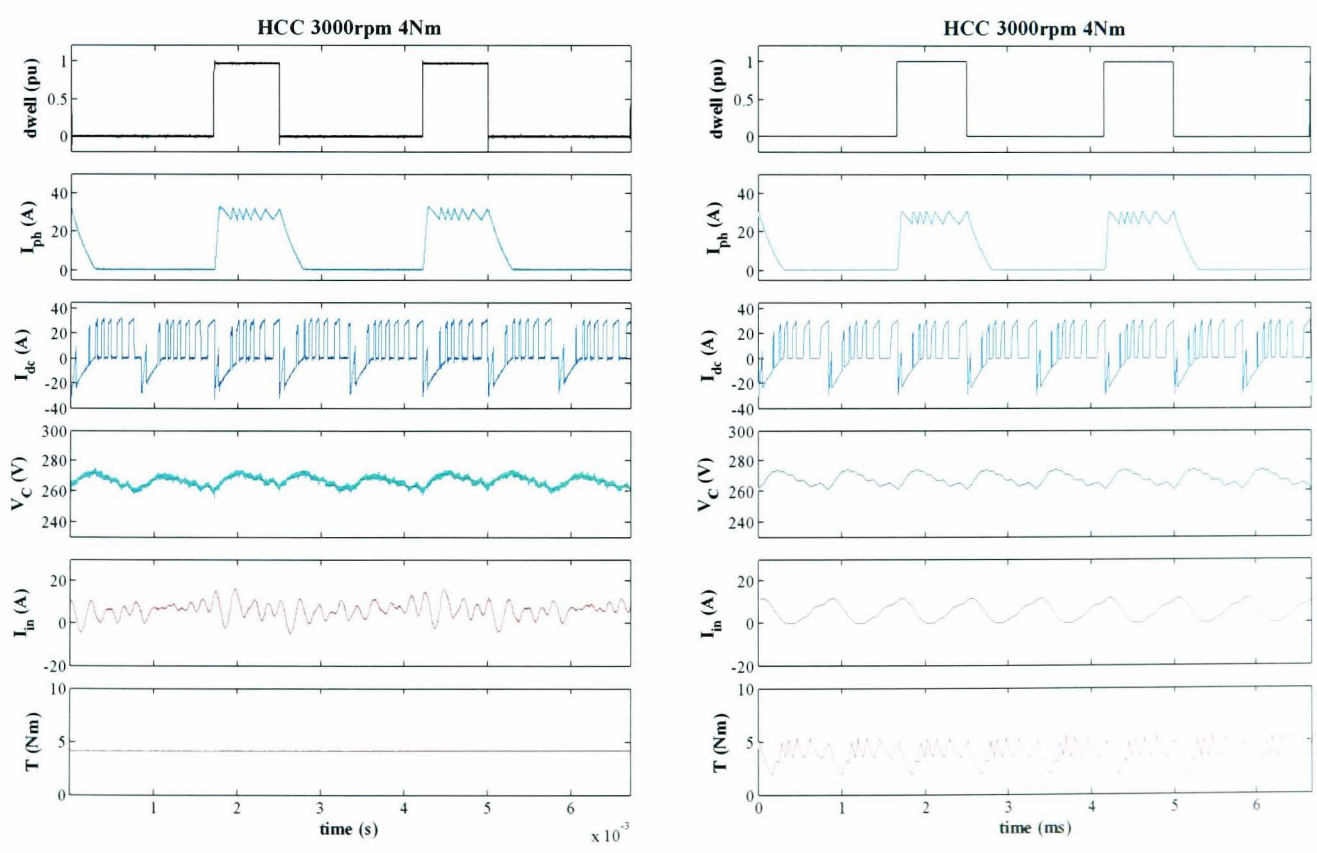
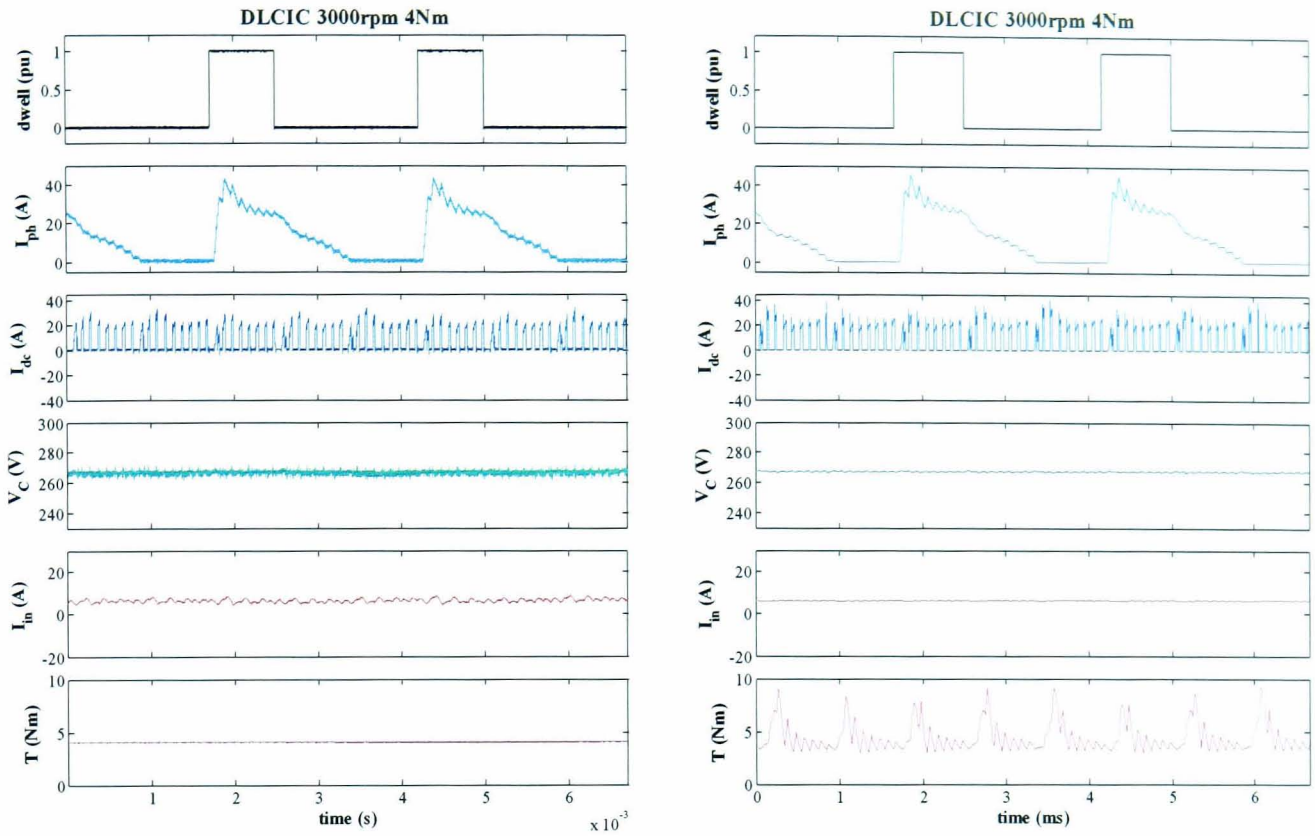


Figure 5.28: Simulation circuit for experimental results



(a) Experiment (b) Simulation

Figure 5.29: Comparison of Experiment result and Simulation result of HCC



(a) Experiment (b) Simulation

Figure 5.30: Comparison of Experiment result and Simulation result of DLCIC

The simulated and measured phase currents in Figure 5.29 and Figure 5.30 are very close, so are the dc-link currents. This validates the simulation model of the SR machine drive. Moreover, the simulated and measured capacitor voltages from both the HCC and DLCIC are comparable. It is seen that the capacitor voltages of DLCIC in Figure 5.30 are smooth while those of HCC in Figure 5.29 have significant ripples. This confirms that DLCIC can reduces the ripple of the dc-link capacitor voltage.

Although the simulated and measured input current of DLCIC in Figure 5.30 are very similar, those of the HCC in Figure 5.29(a) and Figure 5.29(b) are quite different. This is likely caused by the fact that the power supply used in the experiment limits the fluctuation of the supply current. Hence, the measured input current from the HCC in Figure 2.29(a) is not exactly fluctuated at the commutation frequency. In Figure 5.30, the DLCIC naturally limits the ripple of the dc-link capacitor voltage. Consequently, the ripple of the input current reduces. Thus, the input current in Figure 5.30 (a) is similar to that in Figure 5.30(b).

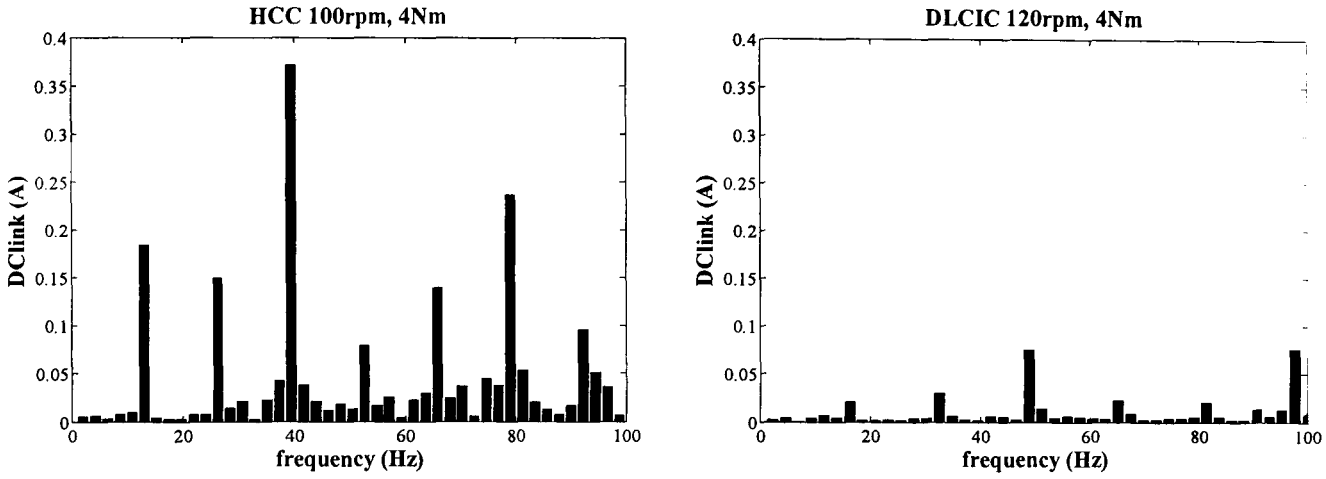
It is noticed that most of the torques from the experimental results are fairly smooth which contrast with the simulation results. This is due to the low pass filter which is built-in the torque transducer. The cut-off frequency of that low pass filter is 40 Hz. Thus, most of the machine torques from the results are smooth.

The voltage ripples of DLCIC from 100 rpm to 3000 rpm are clearly less than those from the HCC. The ripples from the supply currents of the DLCIC are also less than those of the HCC. In the next section, the dc link current harmonics at these speed are analysed and compared.

5.5 Harmonics of Dc-link Current

The harmonics of the dc-link current effect the voltage ripple and the life time of the capacitor [5.9-5.11]. However, the capacitor voltages and the supply currents showing in the last section may be affected by the speed loop control. To avoid such an effect, in this section, the harmonics of the dc-link current at the commutation frequency of HCC and DLCIC at 4 Nm, 100, 500, 1000, 2000, and 3000 rpm are compared and analysed by FFT. This will provide evidence that DLCIC can filter the low frequency harmonics and prevent them to return to the dc supply.

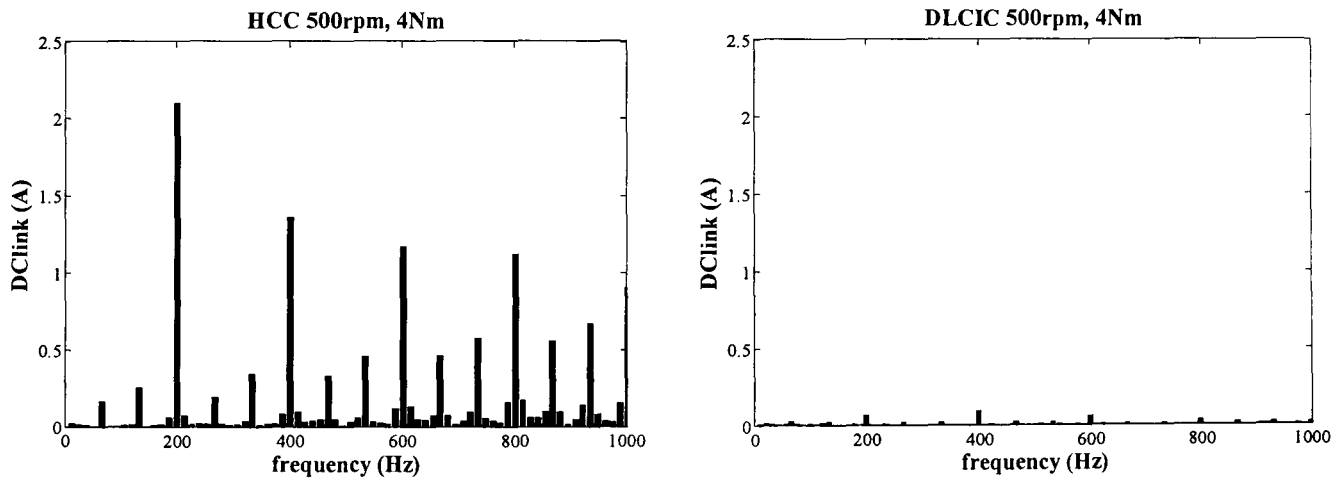
Since the experimental results of the DLCIC at 100 rpm cannot be collected, the dc-link current which is converted to the frequency domain is obtained the operation at the speed 120 rpm. Figure 5.31 shows the spectrum of the dc-link current from the HCC at 100 rpm and from the DLCIC at 120 rpm. It can be seen that the highest harmonic from the HCC in Figure 5.31(a) is 0.37 A at the commutation frequency, 40 Hz, while the highest harmonic from the DLCIC is 0.08 A at 48 Hz, which is the commutation frequency of 120 rpm. Although the machine speed of the DLCIC is slightly higher than that of the HCC, the harmonic at the commutation frequency from the DLCIC is much lower than that of the HCC.



(a) (b)

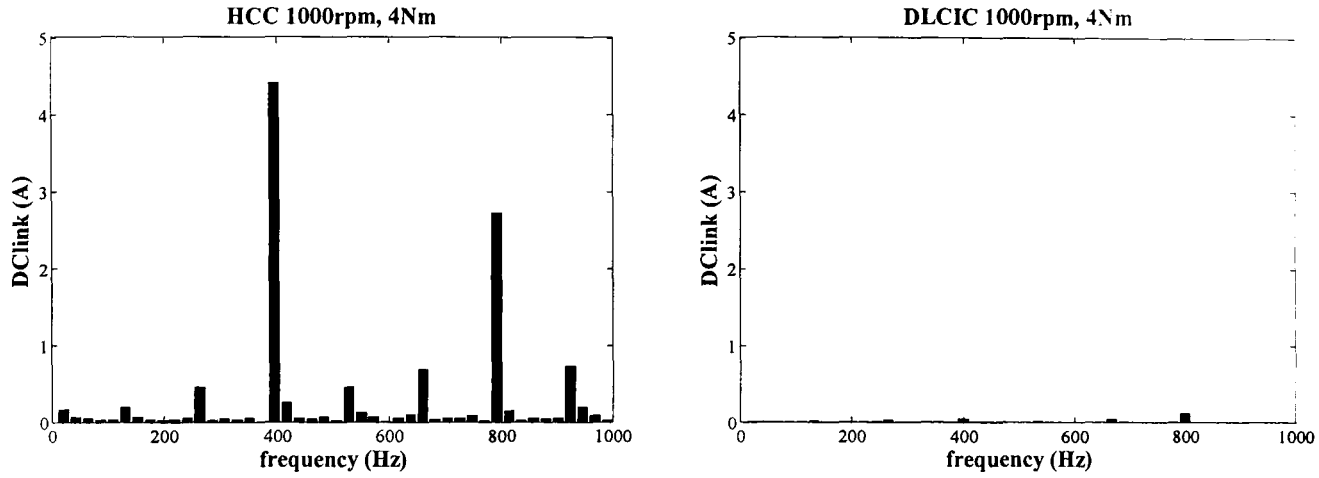
Figure 5.31: Harmonics of dc-link current at 100 rpm

Figure 5.32 to Figure 5.35 show the dc-link current harmonics from the HCC and DLCIC at the speeds of 500, 1000, 2000, and 3000 rpm. In Figure 5.32, at 500 rpm the commutation frequency is 200 Hz. The highest harmonic of the HCC at the commutation frequency in Figure 5.31(a) is much higher than the highest harmonic of the DLCIC in Figure 5.32 (b). It is clearly seen that the harmonics in the low frequency range from the DLCIC are much lower than those from HCC and this causes the low capacitor voltage ripple by the DLCIC.



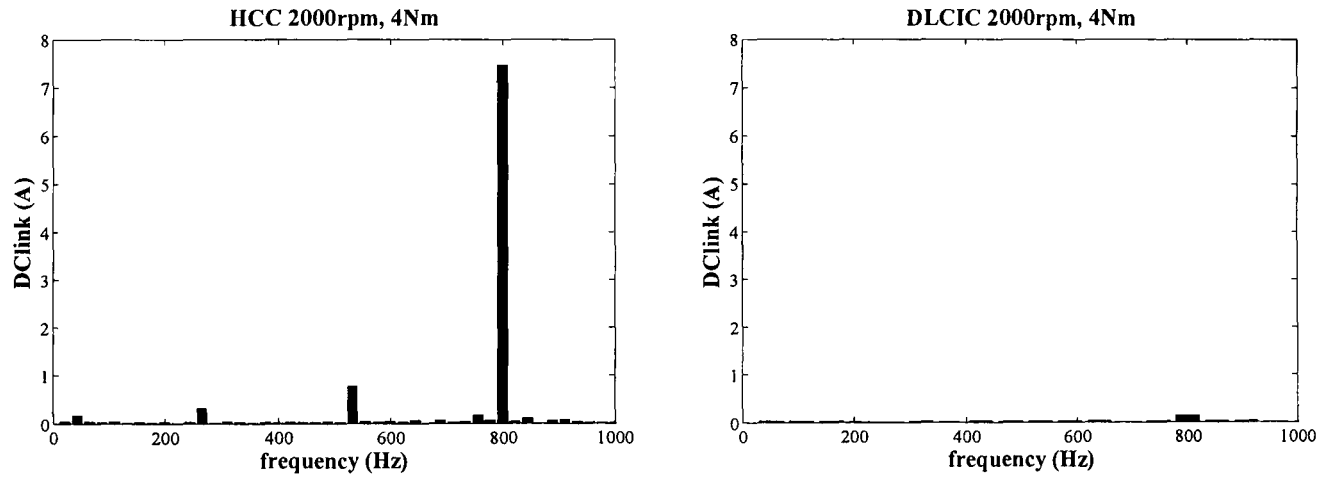
(a) (b)

Figure 5.32: Harmonics of dc-link current at 500 rpm



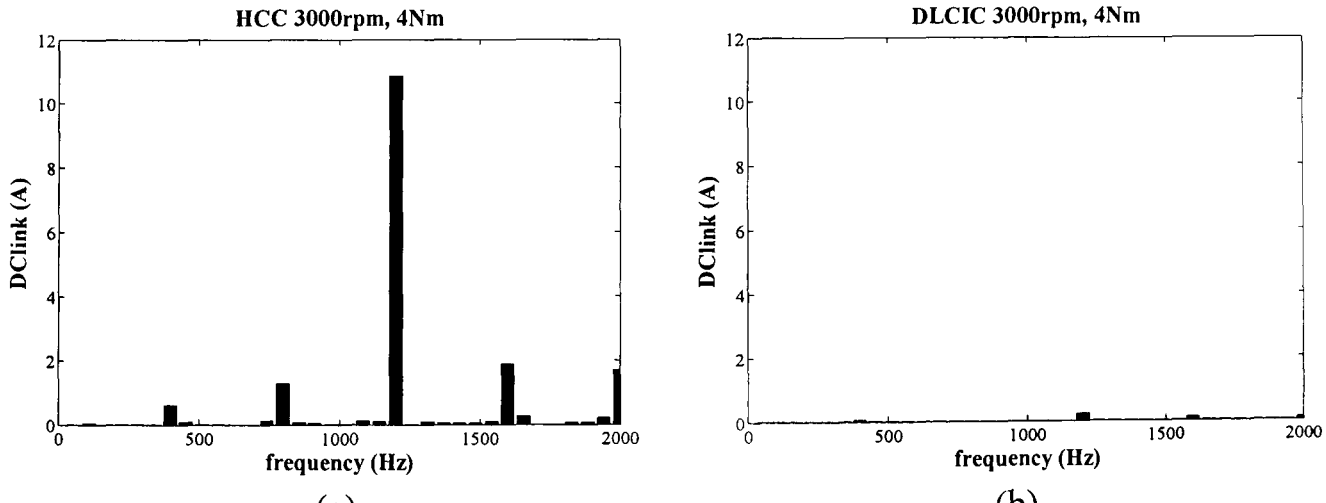
(a) (b)

Figure 5.33: Harmonics of dc-link current at 1000 rpm



(a) (b)

Figure 5.34: Harmonics of dc-link current at 2000 rpm



(a) (b)

Figure 5.35: Harmonics of dc-link current at 3000 rpm

From Figure 5.33 to Figure 5.35, it is apparent that the harmonics in the low frequency range from the DLCIC are much lower than those from the HCC. Especially at the commutation frequency, the harmonics at the commutation frequency from the HCC are high due to the negative dc-link current while the harmonics from the DLCIC are low even at the commutation frequency. This confirms that the DLCIC generates the low ripples of capacitor voltage and the low ripples of the supply current. The current harmonics of the DLCIC flowing back to the supply grid are lower than those of the HCC as well.

5.6 Conclusion

In this chapter, the experiments and details are unveiled. The experimental components and instruments, the signal flows and the control circuits are described. The control techniques in the experiments are HCC and DLCIC. The experimental results from the same demand torque and the same machine speed for both techniques are compared. From the experimental results, the peak to peak values of the dc-link capacitor voltage and the supply current from DLCIC is lower than those from HCC. This shows that DLCIC can reduce the dc-link voltage ripple when compared with those from HCC.

Moreover, since the dc-link voltage ripple might be effected from other factors such as a speed loop, the dc-link current is analysed by using FFT. The harmonics of the dc-link currents from the HCC and DLCIC are compared. The harmonics in a low frequency range of DLCIC are much lower than those of HCC. DLCIC can reduce the harmonics which are the cause of the voltage ripple in the dc-link capacitor. This demonstrates that the DLCIC can minimise the dc-link capacitance when comparing to HCC.

5.7 Reference

[5.1] L. Han, J. Wang, and D. Howe, "Stability assessment of distributed DC power systems for 'more-electric' aircraft," in *Proc. Power Electronics, Machines and Drives, 2008. PEMD 2008. 4th IET Conference on*, 2008, pp. 661-665.

[5.2] A. Emadi, A. Khaligh, C. H. Rivetta, and G. A. Williamson, "Constant power loads and negative impedance instability in automotive systems: definition, modeling, stability, and control of power electronic converters and motor drives," *Vehicular Technology, IEEE Transactions on,* vol. 55, pp. 1112-1125, 2006.

[5.3] G. Hongwei, F. R. Salmasi, and M. Ehsani, "Inductance model-based sensorless control of the switched reluctance motor drive at low speed," *Power Electronics, IEEE Transactions on,* vol. 19, pp. 1568-1573, 2004.

[5.4] L. Xinyun, A. J. Forsyth, and A. M. Cross, "Negative Input-Resistance Compensator for a Constant Power Load," *Industrial Electronics, IEEE Transactions on,* vol. 54, pp. 3188-3196, 2007.

[5.5] A. Khaligh, A. M. Rahimi, and A. Emadi, "Negative Impedance Stabilizing Pulse Adjustment Control Technique for DC/DC Converters Operating in Discontinuous Conduction Mode and Driving Constant Power Loads," *Vehicular Technology, IEEE Transactions on,* vol. 56, pp. 2005-2016, 2007.

[5.6] A. Griffo and J. Wang, "Design optimization of passive DC filters for aerospace applications," in *Proc. Power Electronics, Machines and Drives (PEMD 2010), 5th IET International Conference on*, 2010, pp. 1-6.

[5.7] C. H. Rivetta, A. Emadi, G. A. Williamson, R. Jayabalan, and B. Fahimi, "Analysis and control of a buck DC-DC converter operating with constant power load in sea and undersea vehicles," *Industry Applications, IEEE Transactions on,* vol. 42, pp. 559-572, 2006.

[5.8] F. W. Grover, "Inductance calculations : working formulas and tables". New York Van Nostrand, 1946.

[5.9] A. Mariscotti, "Analysis of the DC-link current spectrum in voltage source inverters," *Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on,* vol. 49, pp. 484-491, 2002.

[5.10] B. P. McGrath and D. G. Holmes, "A General Analytical Method for Calculating Inverter DC-Link Current Harmonics," in *Industry Applications Society Annual Meeting, 2008. IAS '08. IEEE*, 2008, pp. 1-8.

[5.11] A. Eid, H. El-Kishky, M. Abdel-Salam, and M. T. El-Mohandes, "On Power Quality of Variable-Speed Constant-Frequency Aircraft Electric Power Systems," *Power Delivery, IEEE Transactions on,* vol. 25, pp. 55-65, 2010.

Chapter 6

Conclusion and Future Work

6.1 Conclusion

This thesis introduces a control technique for the dc-link capacitance minimisation in switched reluctance (SR) machines. The structures of SR machines are simple without magnets. This leads to an inherent fault tolerant characteristic of this machine and allows its operation in harsh environments. Furthermore, the conventional converter of SR machines, H-bridge converters, also have the fault tolerance characteristic which is used as separated phase control [6.1]. This characteristic makes the SR machine drive attractive in safety critical applications such as aircrafts and electric vehicles. However, the dc-link capacitor bank in the SR converter is large and heavy. This is a major concern in the applications where the space and weight are limited.

The characteristic of the phase current commutation and the machine torque are investigated in Chapter1. The cause of the large dc-link capacitor in the SR drive is also explained. The magnetic energy in the field winding is discharged when the dwell

period is over. If this energy is stored in the dc-link capacitor without control, sufficient capacitance is required to limit the dc-link voltage ripple below an acceptable level. The principle of the proposed control is to maintain a constant average dc-link current over the switching period. The discharged energy or the dc-fluxing current is transferred from the outgoing phase to the incoming phase without causing any negative dc-link current. The conduction state and the power circuits of SR machine are also investigated in Chapter1.

The principle of the proposed control, dc-link current integration control (DLCIC), and the simulation studies are detailed in Chapter 2. Moreover, the literatures, which are also suggested the control techniques to minimise the dc-link capacitance, are investigated and simulated. The simulation results from several techniques, such as Hysteresis Current Control (HCC) and Pulse width Modulation Current Control (PWMCC), are compared. The peak-to-peak voltage ripple of the dc-link capacitor from DLCIC is less than those from all other techniques and it is only 10% of that from HCC. Furthermore, the ripple of the input current from DLCIC is also much less than those from other techniques. The harmonics of the dc-link current from these techniques are compared in Chapter 2. The harmonics in the commutation frequency range, which are the main cause of the dc-link voltage fluctuation, of the DLCIC are less than those of other controls. It has been shown that if the harmonics at the commutation frequency and its integer multiplies are very low, the harmonics of the capacitor voltage will be low too.

While the DLCIC can reduce the voltage ripple of the dc-link capacitor in SR drives, the optimal turn-on and turn-off angles of DLCIC are determined by the numerical analysis in Chapter 3. The characteristics of the optimal turn-on and turn-off angles of DLCIC from the numerical analysis are compared with the optimal characteristics of HCC. The average torques of HCC and DLCIC are close because the average dc-link currents of DLCIC are controlled to be equal to those of HCC. The torque per copper loss of DLCIC at the speed below 3000 rpm is higher than that of HCC. Thus, the operational speed range of DLCIC is determined to be below 3000 rpm.

However, the torque ripples of DLCIC are much higher than those of HCC. At the beginning of the dwell period, the current from the outgoing phase is transferred to the incoming phase and the current from the dc link also flows to the incoming phase. Thus, the phase current of the incoming phase of DLCIC is higher than the phase current of HCC. At the end of the dwell period, the phase current of DLCIC is lower than that of HCC. The phase current decreases quickly during the soft switch turn-off period due to the high back EMF voltage.

Moreover, the analytical optimal turn-on and turn-off angles of DLCIC are established in Chapter3. The equation of the optimal turn-off angle is analysed from the characteristic of the flux linkage. Since the phase current of DLCIC is gradually discharged after the turn-off angle, the flux linkage also decreases gradually which mirrors the flux linkage of Pulse Width Modulation Voltage Control (PWMVC) before the turn-off angle. Hence, the optimal turn-off angle concept of PWMVC in [6.2] is adapted and applied to find the optimal turn-off angle of DLCIC. The analytical turn-on angle of DLCIC is estimated from the trend of the turn-on angle of DLCIC and HCC since the variation of the turn-on angle of DLCIC is virtually similar to that of HCC. The analytical optimal turn-on and turn-off angles are compared with those obtained numerically. It has been shown that while differences exist between the two, they do not cause noticeable differences in the SR drive performance.

Since the operational speed range of DLCIC is determined to be below 3000 rpm, HCC will be used to operate above 3000 rpm, if the SR machine operates in a wide speed range. The Total Harmonic Distortion (THD) graph of the dc-link current from HCC has been shown in Chapter 4. The lower the machine speed is, the higher the THD. Thus, the capacitance of the SR drive which combines both DLCIC and HCC is sized at 3000 rpm for HCC operation. Furthermore, the dc-link capacitance for only HCC operation has also been sized for the purpose of comparison and the design scenario of this case is HCC at 100 rpm.

Since the dc-link capacitor is generally a part of the low pass filter, not only the dc-link capacitance is designed, the input resistance and the input inductance have also been designed in Chapter 4. The weight of all input filter components from DLCIC and HCC are compared.

The stability of the system and the power quality in terms of the capacitor voltage and the supply current are considered in the filter design. The variation of the dc-link capacitance and the input inductance from the stability equation of the system are plotted with difference values of input resistances. The power quality lines which satisfy the military standard [6.3-6.4] in term of the harmonics of the dc-link capacitor voltage and the supply current, are also plotted against the capacitance and inductance with variation of the resistance. The capacitance and the inductance at the intersection of the stability line and the power quality line at each input resistance are used to calculate the filter weights with the consideration of heat dissipation. Then, the weights of each filter satisfying the stability and power quality are compared and the lightest weight has been selected. It has been shown that the input filter weight of HCC is 18 times heavier than that of DLCIC. This confirms that DLCIC can minimise the dc-link capacitance and the weight of the whole input filter.

The experimental results in Chapter 5 have validated that DLCIC can be implemented in practical system. The detail of the motor, drive, other equipment and the schematic diagrams are also presented. There are some limitations presented in the experiment. For example, the dc-link current cannot be directly measured since the planar bus bars are directly connected to the dc-link capacitor. The dc-link current is re-constructed by the switching signals and the phase currents. The rated load torque cannot be performed in the experiment since the maximum torque of the dynamometer is at 4 Nm.

Although there are some disturbances from the speed loop, the experimental results still show that the voltage ripple across the dc-link capacitor from DLCIC is much less than that from HCC. To validate the theoretical analysis and simulation model, the experiment and simulated results at 3000 rpm are compared. For DLCIC, the

experimental and simulation results are similar in most quantities such as the phase current. However, the capacitor voltage and the supply current are different. For HCC, most of the experimental results are similar to the simulation results except the supply current. This is because the power supply is not an ideal power supply as used in the simulation. It does not allow large current fluctuation. In Chapter 5, the harmonics of the dc-link current at the commutation frequency from HCC and DLCIC are compared. It is shown that the harmonics from DLCIC are far less than those from HCC.

6.2 Future Work

In this thesis, the control method of a switched reluctance machine has been proposed to minimise the dc-link capacitance in the drive. The principle of the control, the comparison of the simulation results, the optimal turn-on and turn-off angle and the experimental results are presented. However, the load torque in the experiment is limited at 4 Nm. Experiments at the rated torque should be performed in the future to confirm the simulation results at 20 Nm since the operational speed range of DLCIC is determined on base the operation at rated torque. To eliminate the influence of speed fluctuation on the results, experiments should also be performed by setting the dynamometer at a constant speed and operating the SR drive under the torque control mode

The operational speed range of DLCIC for the SR machine is determined by the numerical analysis at the rated torque. The torque per unit copper loss at the machine speed of 3000 rpm or below from DLCIC is higher than that from HCC. Thus, the determined operational speed range is below 3000 rpm while the base speed is 10000 rpm. This coincides with the low speed range of SR machine being defined a one-third of the base speed [6.5]. The same process can be applied to other SR motors to find out the operational speed range of DLCIC. Thus, if the studies of the DLCIC operational speed range of other SR drives show that it coincides with the low speed range of the

motors, a general guideline can be established to determine a suitable operation range of the proposed DLCIC.

Another interesting topic for further study is the vibration and acoustic noise of SR machine from DLCIC. It is stated in [6.6] that the ripple of the dc-link voltage affects the radial force, which is the main cause of vibration and acoustic noise in SR machines [6.7]. The radial force is small when the rotor position is far from the aligned position and increases when the rotor position is near to the aligned position [6.8]. Furthermore, the radial force is high when the phase current is high. The phase current of DLCIC is high at the beginning of the dwell angle and then is reduced at the end of the dwell period when close to the alignment. This means that the phase current is lower when the stator and rotor tooth are aligned. Hence, the radial force from DLCIC is probably less than that from the conventional method. The further study of this topic is interesting.

6.3 Novel Contributions

The following are believed to be the original contributions of this research :

- A novel control technique to minimisation of the dc-link capacitance in an SR drives (DLCIC) has been proposed, analysed and validated.
- Unipolar Hysteresis Control (UHC) technique for the dc-link voltage ripple reduction has also been developed and analysed. The simulation results of UHC are presented and compared with those obtained from the Hysteresis Current Control (HCC) and DLCIC. Although the voltage ripple of UHC is higher than that of DLCIC, it is reduced to 60% of HCC.
- The influence of dc power supply circuit on the dc-link voltage ripple has been analysed. It has been shown that the inductance in the supply circuit affects both dc-link voltage and current ripples, and drive system stability.

- The numerical optimal turn-on and turn-off angles of DLCIC have been analysed and compared with the results from the optimal HCC.
- The analytical optimal turn-on and turn-off angle estimation has been proposed, and validated through the simulation comparison.
- The filter design for DLCIC has been proposed. It has been shown that the filter which is designed for the combined control, DLCIC and HCC, is approximately 18 times lighter than the designed filter for HCC.
- DLCIC has been validated with dSPACE system and a good correlation between the experimental results and the simulation results has been found.

6.4 Reference

[6.1] W. Cao, B. C. Mecrow, G. J. Atkinson, J. W. Bennett, and D. J. Atkinson, "Overview of Electric Motor Technologies Used for More Electric Aircraft (MEA)," *Industrial Electronics, IEEE Transactions on,* vol. 59, pp. 3523-3531, 2012.

[6.2] J. J. Gribble, P. C. Kjaer, and T. J. E. Miller, "Optimal commutation in average torque control of switched reluctance motors," *Electric Power Applications, IEE Proceedings -,* vol. 146, pp. 2-10, 1999.

[6.3] *Aircraft Electric Power Characteristic*, MIL-STD-704F, 2004

[6.4] *Requirements for the control of Electromagnetic Interference Characteristics of Subsystems and Equipment*, MIL-STD-461E, 1999

[6.5] G. Gallegos-Lopez, "Sensorless Control," in *Electronic Control of Switched Reluctance Machines*, T. J. E. Miller, Ed., ed: Newnes, 2001, pp. 133-170.

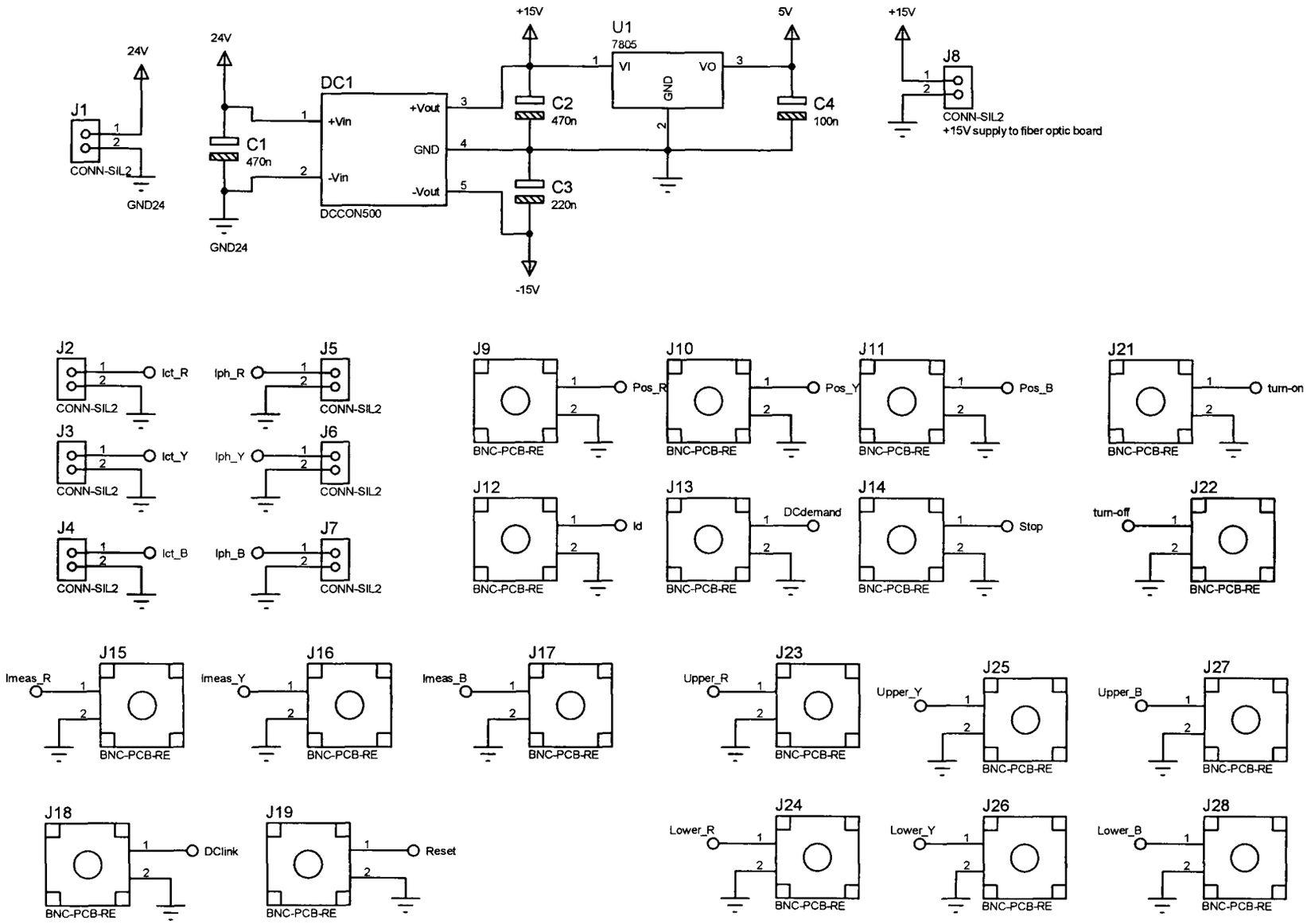
[6.6] C. Jae-Hak, A. Joonseon, and L. Ju, "The characteristic analysis of switched reluctance motor considering DC link voltage ripple on hand and soft chopping modes," in *Proc. Magnetics Conference, 2005. INTERMAG Asia 2005. Digests of the IEEE International*, 2005, pp. 933-933.

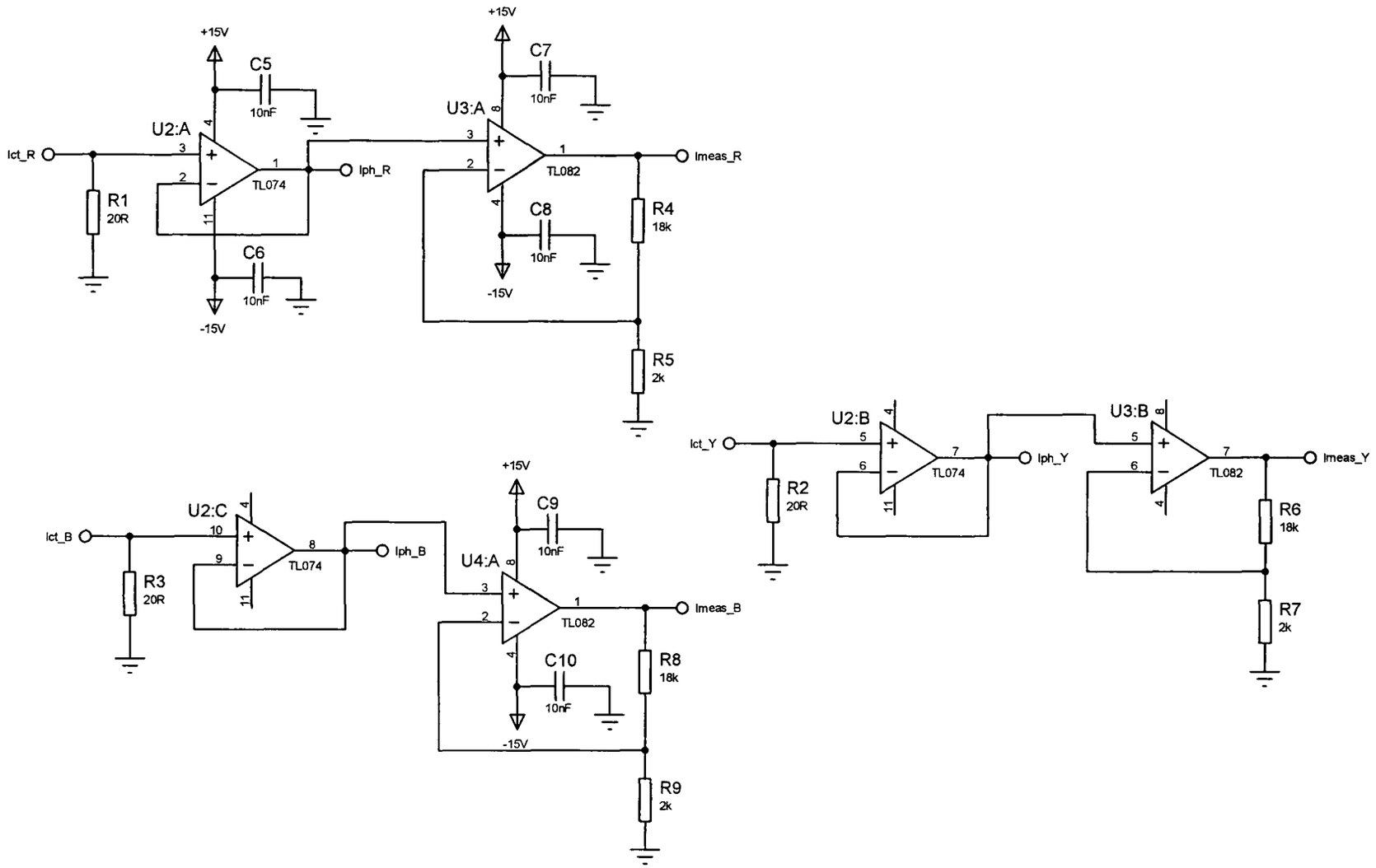
[6.7] C. Y. Wu and C. Pollock, "Analysis and reduction of vibration and acoustic noise in the switched reluctance drive," *Industry Applications, IEEE Transactions on,* vol. 31, pp. 91-98, 1995.

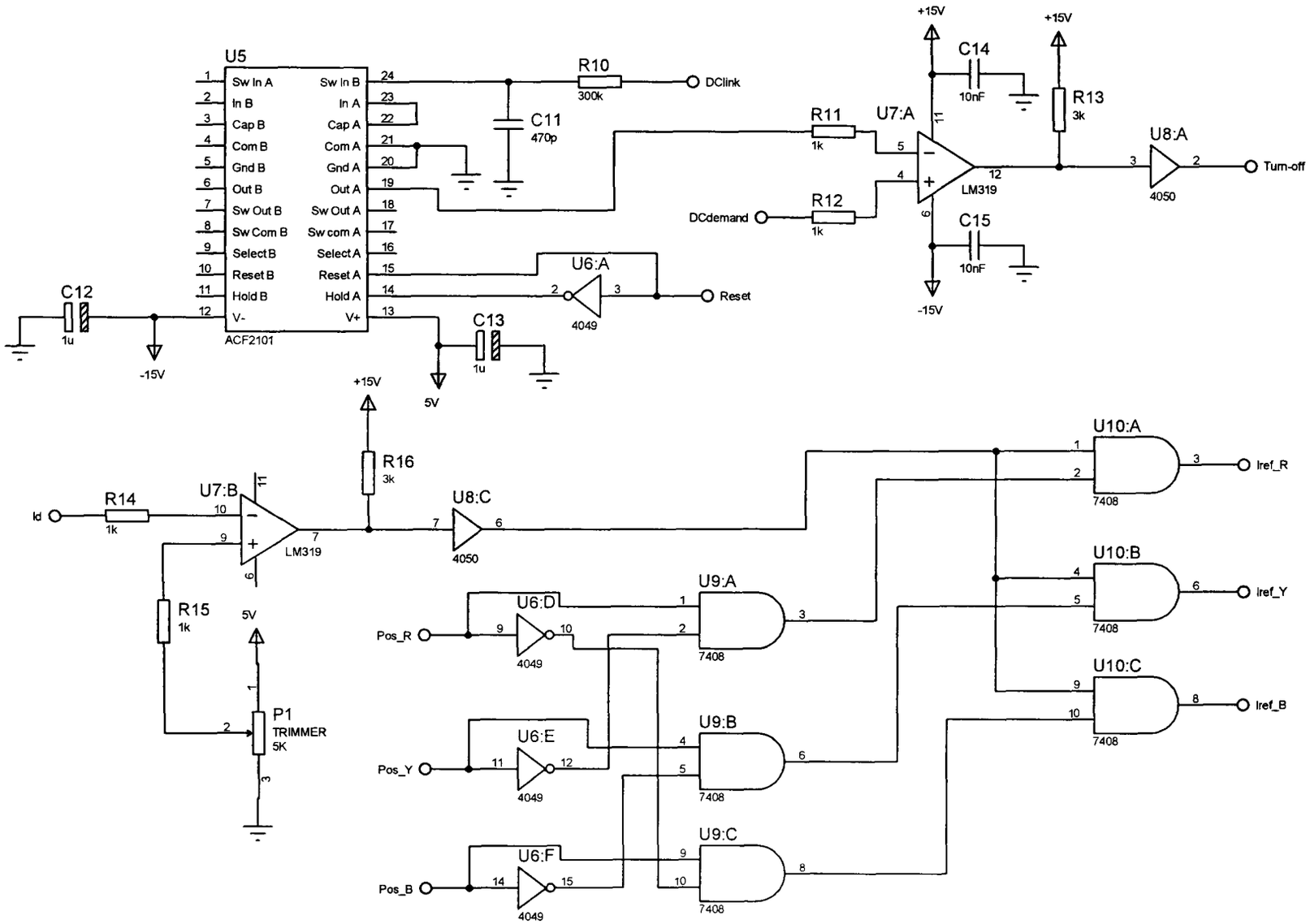
[6.8] C. Y. Wu and C. Pollock, "Time domain analysis of vibration and acoustic noise in the switched reluctance drive," in *Proc. Electrical Machines and Drives, 1993. Sixth International Conference on (Conf. Publ. No. 376)*, 1993, pp. 558-563.

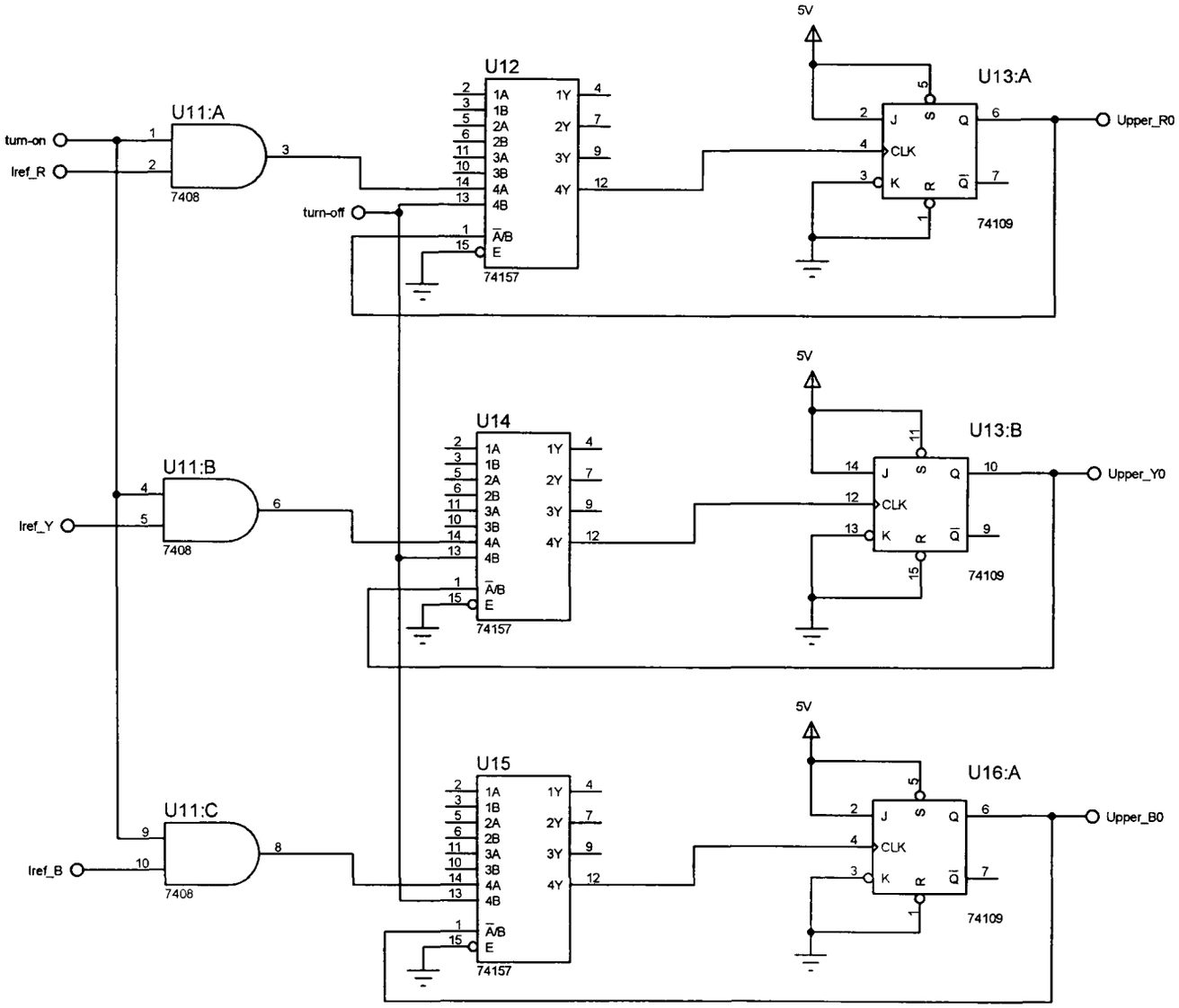
Appendix A

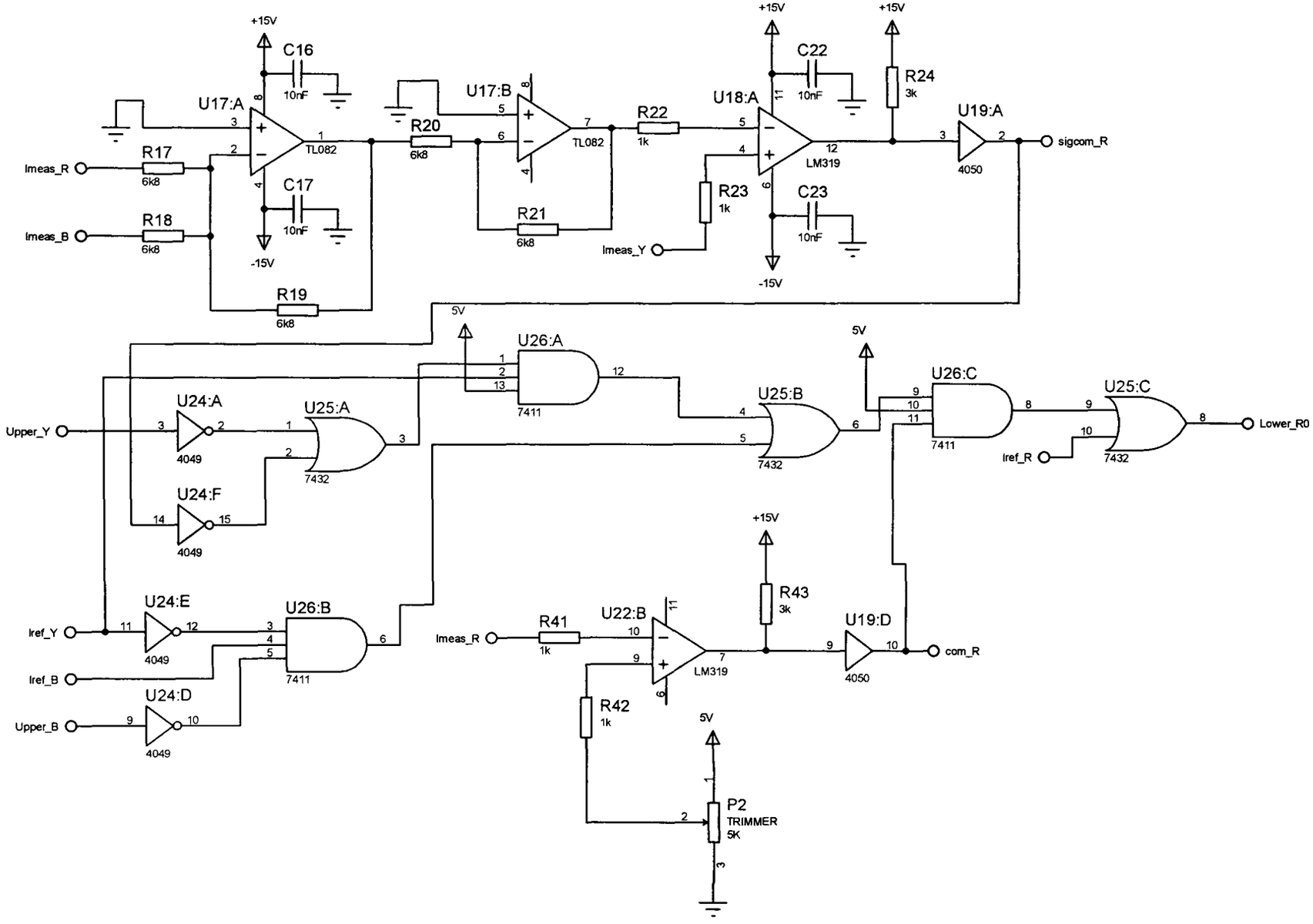
DC-Link Current Integration Control Circuits

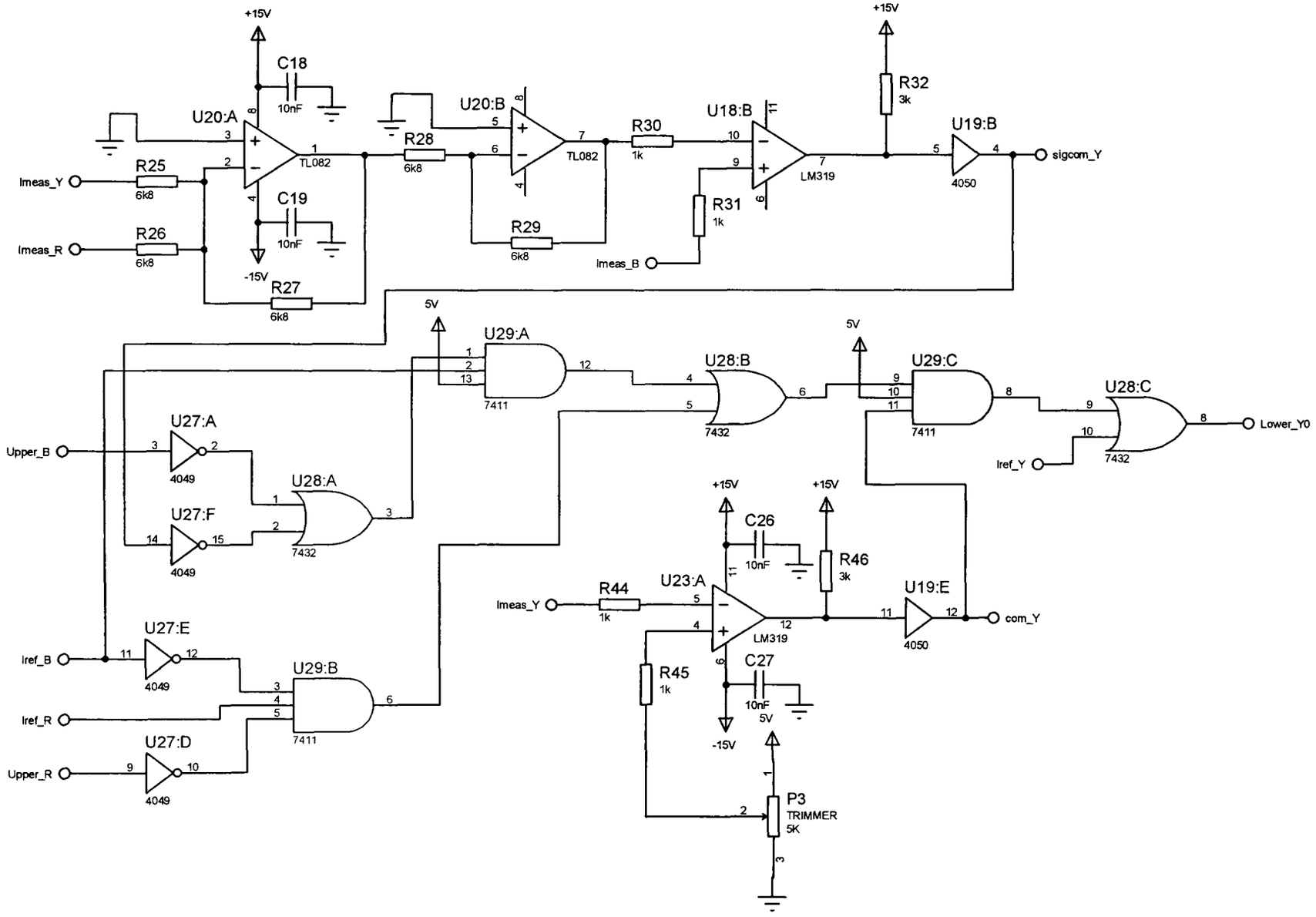

24V
J1
CONN-SIL2
GND24
24V
C1
470n
DC1
+Vin
-Vin
+Vout
GND
-Vout
DCCON500
GND24
+15V
C2
470n
C3
220n
-15V
U1
7805
VI
VO
GND
5V
C4
100n
+15V
J8
CONN-SIL2
+15V supply to fiber optic board
J2
Ict_R
CONN-SIL2
J3
Ict_Y
CONN-SIL2
J4
Ict_B
CONN-SIL2
J5
Iph_R
CONN-SIL2
J6
Iph_Y
CONN-SIL2
J7
Iph_B
CONN-SIL2
J9
Pos_R
BNC-PCB-RE
J10
Pos_Y
BNC-PCB-RE
J11
Pos_B
BNC-PCB-RE
J21
turn-on
BNC-PCB-RE
J12
Id
BNC-PCB-RE
J13
DCdemand
BNC-PCB-RE
J14
Stop
BNC-PCB-RE
J22
turn-off
BNC-PCB-RE
J15
Imeas_R
BNC-PCB-RE
J16
Imeas_Y
BNC-PCB-RE
J17
Imeas_B
BNC-PCB-RE
J23
Upper_R
BNC-PCB-RE
J25
Upper_Y
BNC-PCB-RE
J27
Upper_B
BNC-PCB-RE
J18
DClink
BNC-PCB-RE
J19
Reset
BNC-PCB-RE
J24
Lower_R
BNC-PCB-RE
J26
Lower_Y
BNC-PCB-RE
J28
Lower_B
BNC-PCB-RE

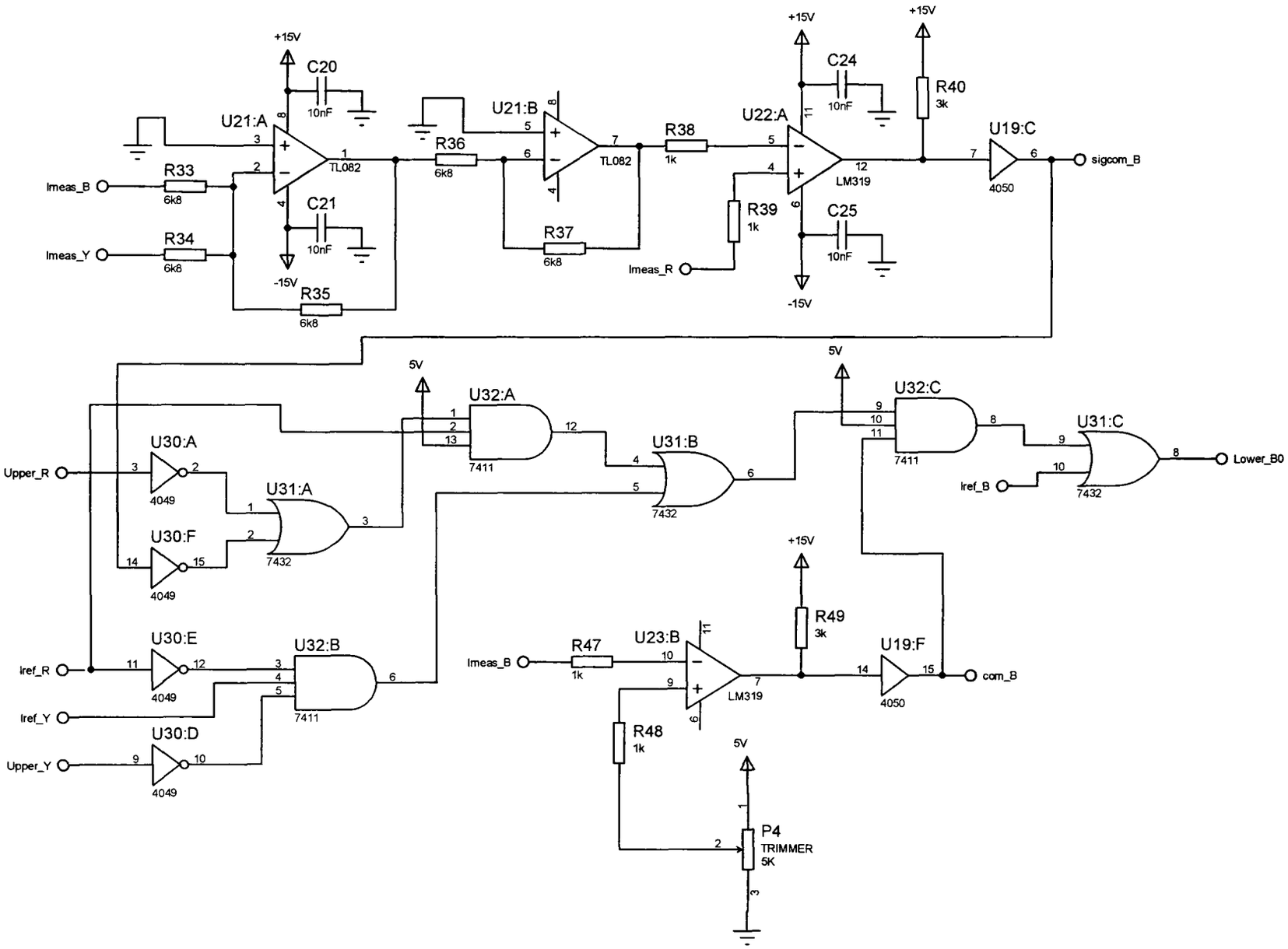

+15V
C5
10nF
U2:A
Ict_R
R1
20R
TL074
Iph_R
C6
10nF
-15V
+15V
C7
10nF
U3:A
TL082
Imeas_R
R4
18k
C8
10nF
-15V
R5
2k
+15V
C9
10nF
U2:C
Ict_B
R3
20R
TL074
Iph_B
U4:A
TL082
Imeas_B
C10
10nF
R8
18k
-15V
R9
2k
U2:B
Ict_Y
R2
20R
TL074
Iph_Y
U3:B
TL082
Imeas_Y
R6
18k
R7
2k

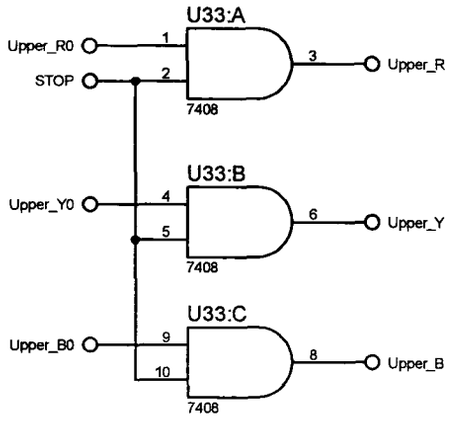

U5
ACF2101
Sw In A
In B
Cap B
Com B
Gnd B
Out B
Sw Out B
Sw Com B
Select B
Reset B
Hold B
V-
Sw In B
In A
Cap A
Com A
Gnd A
Out A
Sw Out A
Sw com A
Select A
Reset A
Hold A
V+
R10
300k
DClink
C11
470p
C12
1u
-15V
C13
1u
5V
U6:A
4049
Reset
+15V
C14
10nF
R13
3k
U7:A
LM319
R11
1k
R12
1k
DCdemand
U8:A
4050
Turn-off
C15
10nF
-15V
R16
3k
R14
1k
Id
U7:B
LM319
U8:C
4050
R15
1k
5V
P1
TRIMMER
5K
U6:D
4049
Pos_R
U6:E
4049
Pos_Y
U6:F
4049
Pos_B
U9:A
7408
U9:B
7408
U9:C
7408
U10:A
7408
Iref_R
U10:B
7408
Iref_Y
U10:C
7408
Iref_B

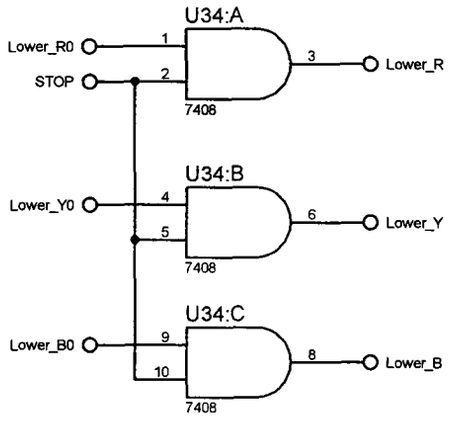

U11:A
turn-on
Iref_R
7408
U12
1A
1B
2A
2B
3A
3B
4A
4B
A/B
E
1Y
2Y
3Y
4Y
74157
turn-off
5V
U13:A
J
S
Q
CLK
K
R
Q
74109
Upper_R0
U11:B
Iref_Y
7408
U14
74157
U13:B
74109
Upper_Y0
U11:C
Iref_B
7408
U15
74157
U16:A
74109
Upper_B0


+15V
C16
10nF
U17:A
TL082
R17
6k8
Imeas_R
R18
6k8
Imeas_B
C17
10nF
-15V
R19
6k8
R20
6k8
U17:B
TL082
R21
6k8
R22
1k
+15V
C22
10nF
U18:A
LM319
R23
1k
Imeas_Y
C23
10nF
-15V
+15V
R24
3k
U19:A
4050
sigcom_R
5V
U26:A
7411
U24:A
4049
Upper_Y
U25:A
7432
U24:F
4049
U25:B
7432
5V
U26:C
7411
U25:C
7432
Iref_R
Lower_R0
U24:E
4049
Iref_Y
Iref_B
U26:B
7411
U24:D
4049
Upper_B
+15V
R43
3k
U22:B
LM319
R41
1k
Imeas_R
R42
1k
U19:D
4050
com_R
5V
P2
TRIMMER
5K


+15V
C18
10nF
U20:A
TL082
R25
6k8
Imeas_Y
R26
6k8
Imeas_R
C19
10nF
-15V
R27
6k8
R28
6k8
U20:B
TL082
R29
6k8
R30
1k
U18:B
LM319
R31
1k
Imeas_B
+15V
R32
3k
U19:B
4050
sigcom_Y
5V
U29:A
7411
U28:B
7432
5V
U29:C
7411
U28:C
7432
Lower_Y0
Iref_Y
U27:A
4049
Upper_B
U28:A
7432
U27:F
4049
U27:E
4049
Iref_B
U29:B
7411
Iref_R
U27:D
4049
Upper_R
+15V
+15V
C26
10nF
R46
3k
U23:A
LM319
R44
1k
Imeas_Y
R45
1k
C27
10nF
5V
-15V
U19:E
4050
com_Y
P3
TRIMMER
5K

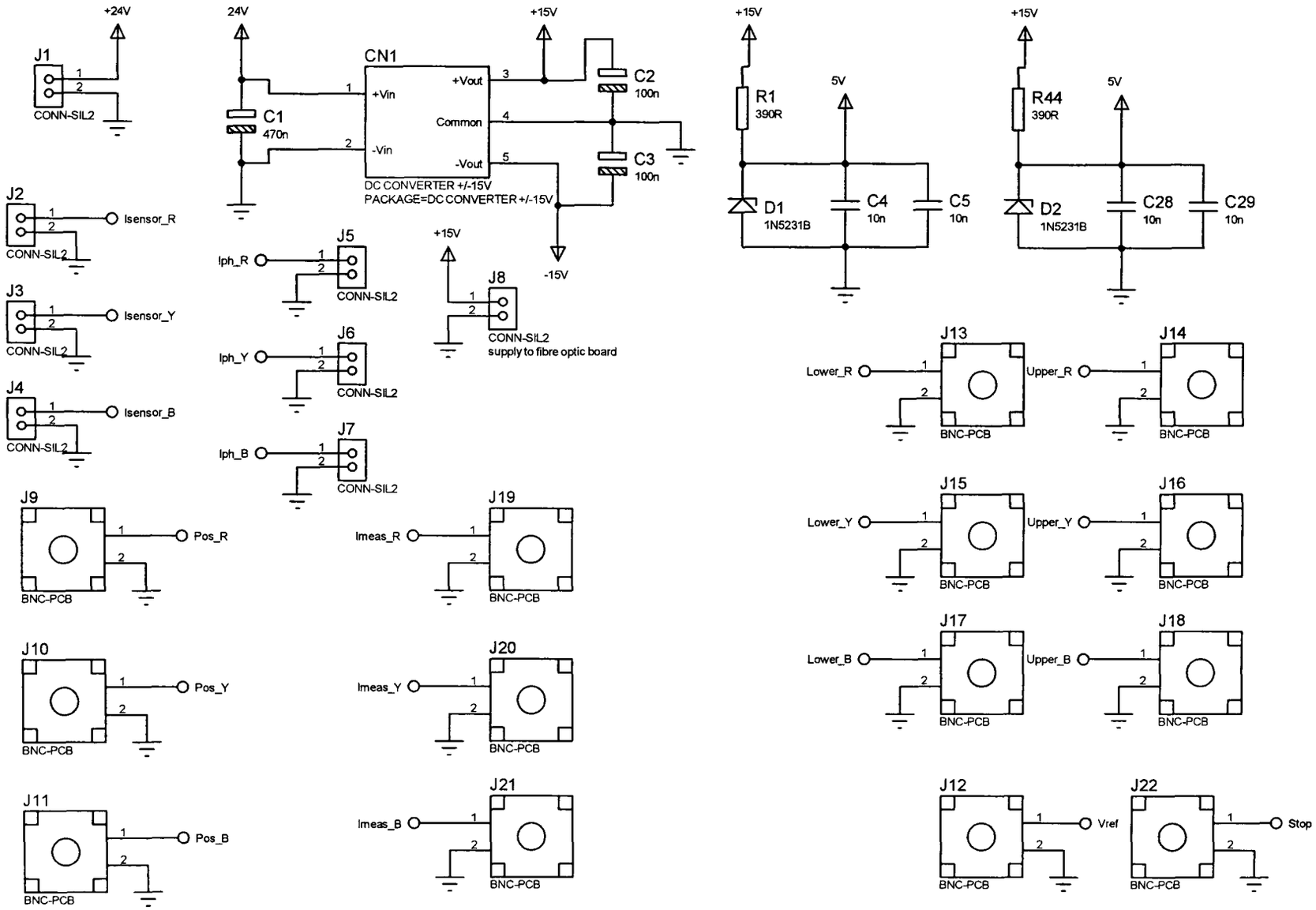

+15V
C20
10nF
U21:A
R33
6k8
Imeas_B
R34
6k8
Imeas_Y
C21
10nF
-15V
R35
6k8
TL082
R36
6k8
U21:B
R37
6k8
TL082
R38
1k
U22:A
R39
1k
Imeas_R
C24
10nF
C25
10nF
R40
3k
LM319
U19:C
4050
sigcom_B
5V
U32:A
7411
U31:B
7432
U32:C
7411
U31:C
7432
Lower_B0
Iref_B
Upper_R
U30:A
4049
U31:A
7432
U30:F
4049
U30:E
4049
U32:B
7411
Iref_R
Iref_Y
U30:D
4049
Upper_Y
U23:B
LM319
R47
1k
R48
1k
R49
3k
U19:F
4050
com_B
P4
TRIMMER
5K

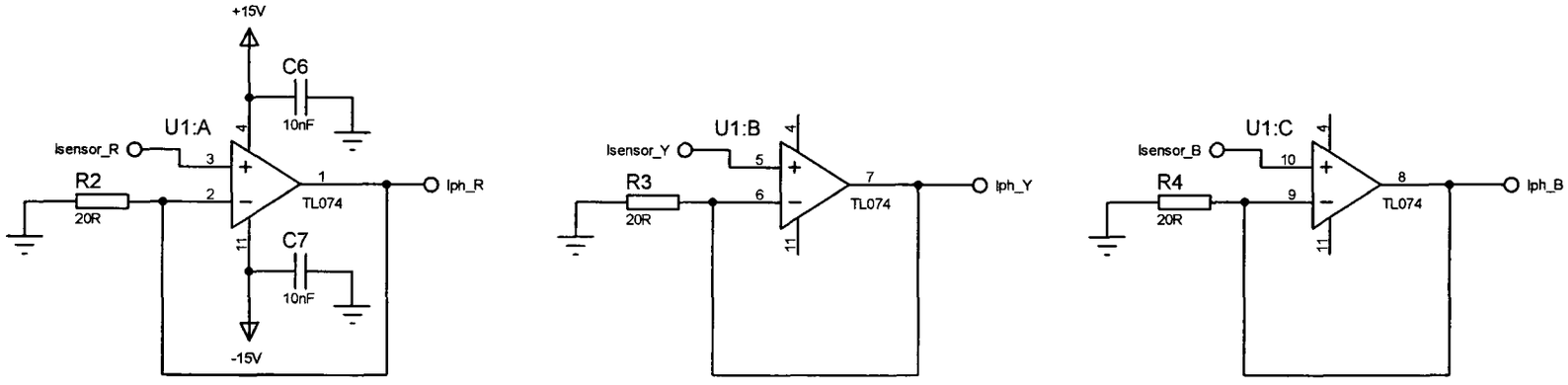

U33:A
Upper_R0
STOP
1
2
3
Upper_R
7408
U33:B
Upper_Y0
4
5
6
Upper_Y
7408
U33:C
Upper_B0
9
10
8
Upper_B
7408

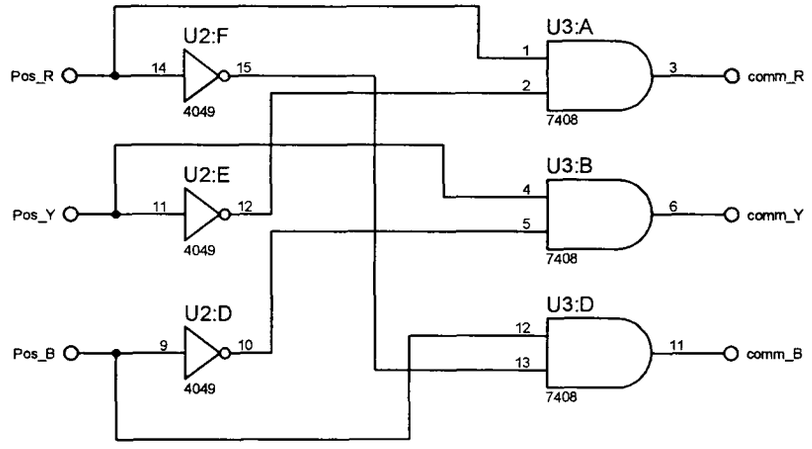

U34:A
Lower_R0
STOP
1
2
3
Lower_R
7408
U34:B
Lower_Y0
4
5
6
Lower_Y
7408
U34:C
Lower_B0
9
10
8
Lower_B
7408

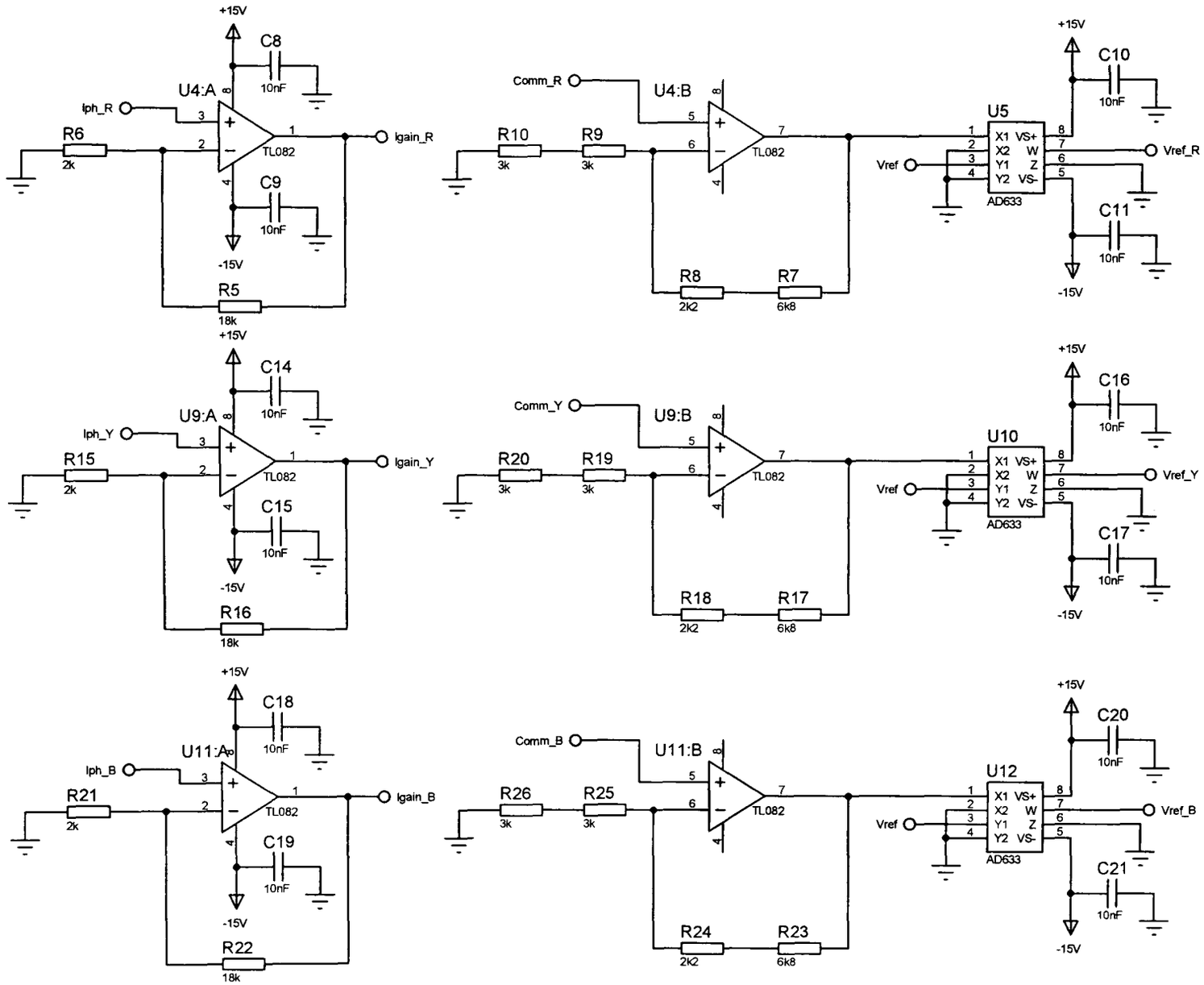
Appendix B

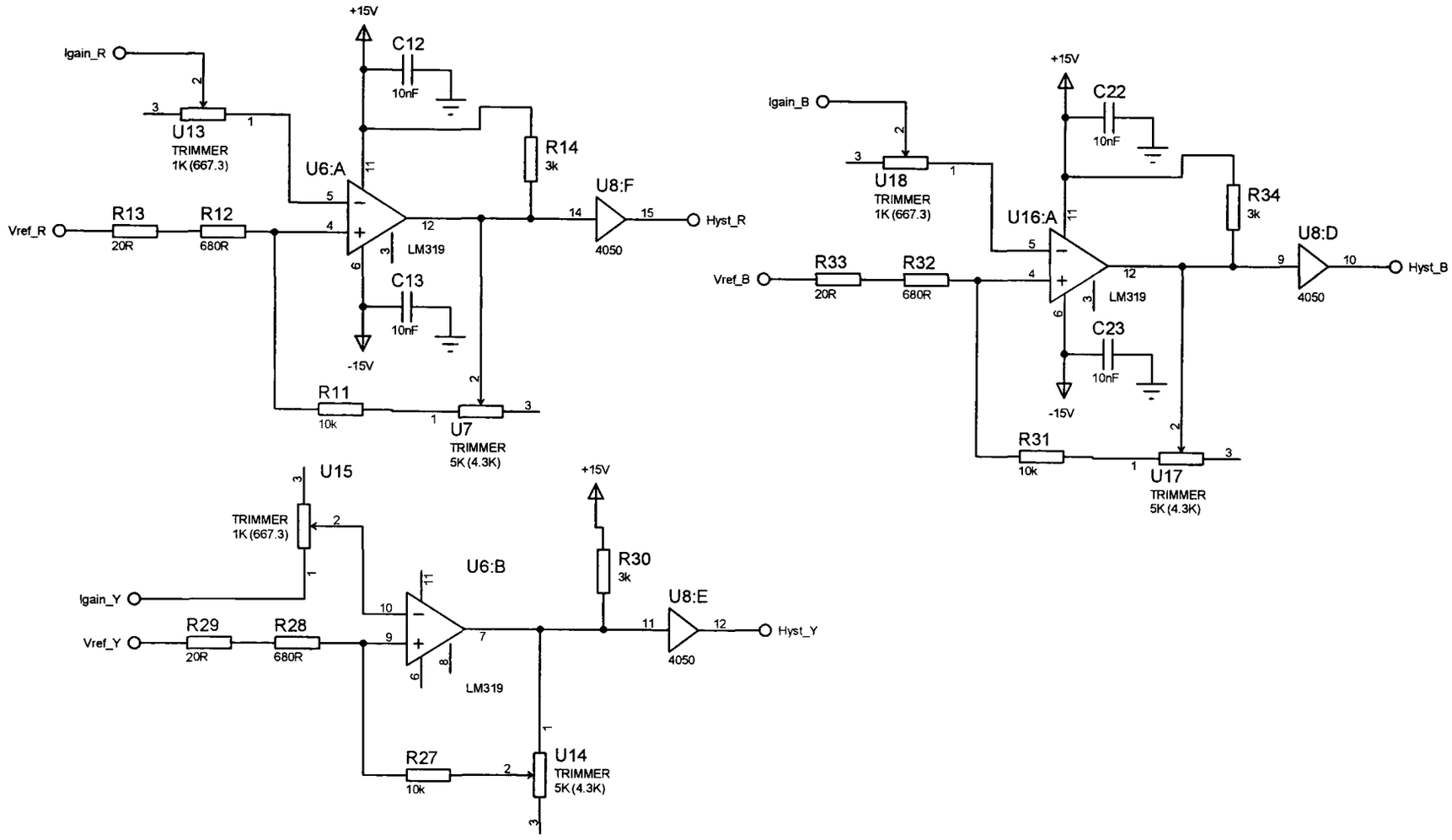
Hysteresis Current Control Circuits

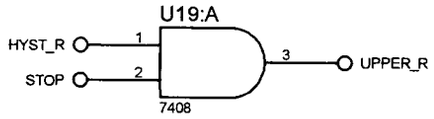

+24V
J1
CONN-SIL2
24V
CN1
+Vin
-Vin
+Vout
Common
-Vout
C1
470n
C2
100n
C3
100n
DC CONVERTER +/-15V
PACKAGE=DC CONVERTER +/-15V
+15V
-15V
J2
Isensor_R
J3
Isensor_Y
J4
Isensor_B
J5
Iph_R
J6
Iph_Y
J7
Iph_B
J8
CONN-SIL2
supply to fibre optic board
R1
390R
5V
D1
1N5231B
C4
10n
C5
10n
R44
390R
D2
1N5231B
C28
10n
C29
10n
J13
Lower_R
Upper_R
BNC-PCB
J14
J9
Pos_R
J10
Pos_Y
J11
Pos_B
J19
Imeas_R
J20
Imeas_Y
J21
Imeas_B
J15
Lower_Y
Upper_Y
J16
J17
Lower_B
Upper_B
J18
J12
Vref
J22
Stop

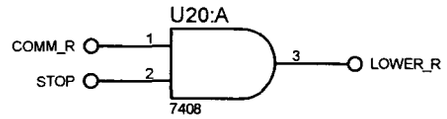

+15V
C6
10nF
U1:A
Isensor_R
3
4
+
R2
2
−
1
Iph_R
TL074
20R
11
C7
10nF
-15V
U1:B
Isensor_Y
5
4
+
R3
6
−
7
Iph_Y
TL074
20R
11
U1:C
Isensor_B
10
4
+
R4
9
−
8
Iph_B
TL074
20R
11

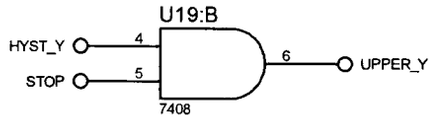

U2:F
Pos_R
14
15
4049
U2:E
Pos_Y
11
12
4049
U2:D
Pos_B
9
10
4049
U3:A
1
2
3
comm_R
7408
U3:B
4
5
6
comm_Y
7408
U3:D
12
13
11
comm_B
7408

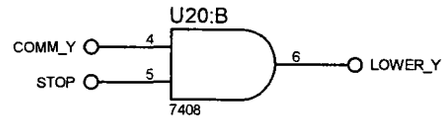

+15V
C8
10nF
U4:A
Iph_R
R6
2k
TL082
Igain_R
C9
10nF
-15V
R5
18k
Comm_R
U4:B
R10
3k
R9
3k
R8
2k2
R7
6k8
U5
AD633
Vref
Vref_R
C10
10nF
C11
10nF
C14
10nF
U9:A
Iph_Y
R15
2k
Igain_Y
C15
10nF
R16
18k
Comm_Y
U9:B
R20
3k
R19
3k
R18
2k2
R17
6k8
U10
Vref_Y
C16
10nF
C17
10nF
C18
10nF
U11:A
Iph_B
R21
2k
Igain_B
C19
10nF
R22
18k
Comm_B
U11:B
R26
3k
R25
3k
R24
2k2
R23
6k8
U12
Vref_B
C20
10nF
C21
10nF

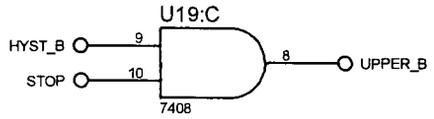

Igain_R
Vref_R
R13
20R
R12
680R
+15V
C12
10nF
U13
TRIMMER
1K (667.3)
U6:A
LM319
R14
3k
U8:F
4050
Hyst_R
C13
10nF
-15V
R11
10k
U7
TRIMMER
5K (4.3K)
Igain_B
Vref_B
R33
20R
R32
680R
U18
TRIMMER
1K (667.3)
U16:A
LM319
C22
10nF
R34
3k
U8:D
4050
Hyst_B
C23
10nF
-15V
R31
10k
U17
TRIMMER
5K (4.3K)
U15
TRIMMER
1K (667.3)
Igain_Y
Vref_Y
R29
20R
R28
680R
U6:B
LM319
+15V
R30
3k
U8:E
4050
Hyst_Y
R27
10k
U14
TRIMMER
5K (4.3K)

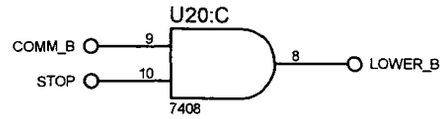

U19:A
HYST_R
STOP
1
2
3
UPPER_R
7408

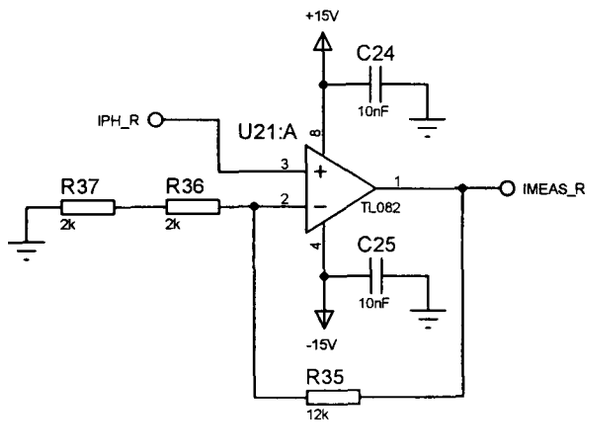

U20:A
COMM_R
STOP
1
2
3
LOWER_R
7408

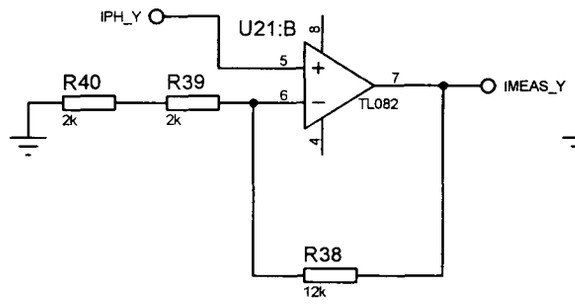

U19:B
HYST_Y
STOP
4
5
6
UPPER_Y
7408

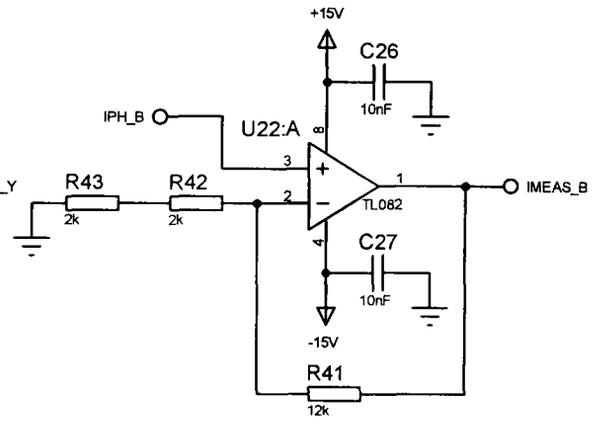

U20:B
COMM_Y
STOP
4
5
6
LOWER_Y
7408


U19:C
HYST_B
STOP
9
10
8
UPPER_B
7408


U20:C
COMM_B
STOP
9
10
8
LOWER_B
7408


+15V
C24
10nF
IPH_R
U21:A
R37
R36
2k
2k
TL082
IMEAS_R
C25
10nF
-15V
R35
12k


IPH_Y
U21:B
R40
R39
2k
2k
TL082
IMEAS_Y
R38
12k


+15V
C26
10nF
IPH_B
U22:A
R43
R42
2k
2k
TL082
IMEAS_B
C27
10nF
-15V
R41
12k

Appendix C

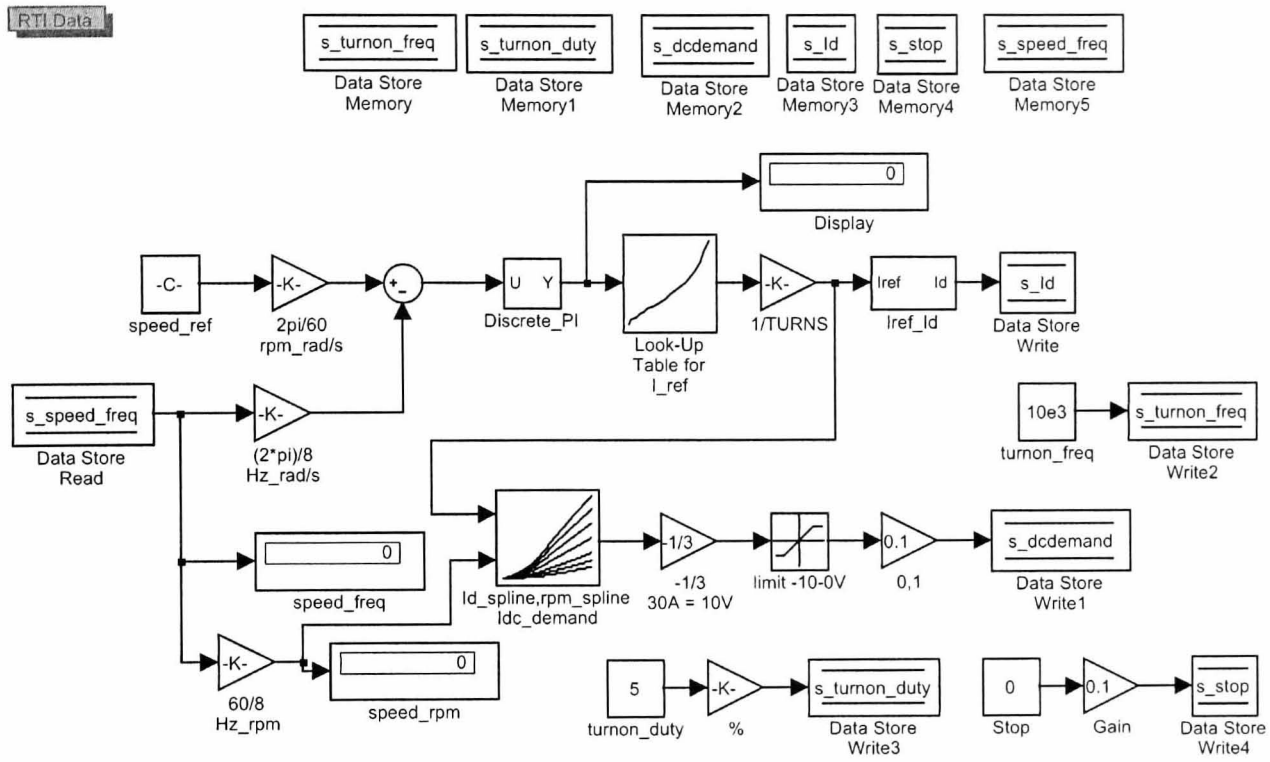
DC-Link Current Integration Control Programs

C.1 Initial m-file

```
% ========= INITIALISING VALUES FOR DCInt SRM speed loop Lab  ======================

clear

turns_per_phase = 76;                       % number of turns per phase
NR = 8;                                     % number of rotor poles
NS = 12;                                    % number of stator poles
NPH = 3;                                    % number of phases
CYCLE = 360/NR;                             % repeat angle for lookup table = 45 deg
TURNS = turns_per_phase/(NS/NPH);           % number of turns for linkage flux = 19
Rph = 0.17;                                 % phase resistance
J = 0.004;                                  % shaft inertia (RB2009 HP spool) = 0.2
B = 0.0015;                                 % assuming a damping coefficient

VDC = 270;                                  % Input DC Voltage

speed_ref = 100;                                % speed of the machine in rpm
pwm_freq =10e3;

Tl = 0;             % torque load (Nm)

Ts = 0.1;        % settling time
zeta = 1.2;           % damping ratio

Bl = Tl/(speed_ref*(2*pi/60));

Kp = (8*J/Ts) - (B + Bl);                   % Kp in PI control
Ki = (4/(Ts*zeta))^2 * J;                   % Ki in PI control

load ('suave_flux.txt')
load ('suave_torque.txt')
load ('suave_dclink.txt')

% ==================== FLUX ========================

% Calculating flux table (fff)
% theta(deg)(theta_spline) - column, mmf(Ni)(mmf_spline) - row

q = 100;                                    % Precision

[m,n] = size(suave_flux);
mmf(2:n) = [suave_flux(1,2:n)]';
mmf(1) = 0;
mmf_spline = [0:max(mmf)/(q-1):max(mmf)]';

theta = [suave_flux(2:m,1)]';
theta_spline = [0:max(theta)/(q-1):max(theta)]';

% extract target flux
f(:,2:n) = suave_flux(2:m,2:n);
f(:,1) = zeros(m-1,1);

for k = 1 : length(theta)
    ff(:,k) = interp1(mmf,f(k,:),mmf_spline,'cubic');
end

fff = interp2(theta,mmf_spline,ff,theta_spline',mmf_spline,'cubic');

fli = (0:max(max(f))/(q-1):max(max(f)))';

for k = 1:q
    I_fn_psi_theta(:,k) = interp1(fff(:,k),mmf_spline',fli);
end

for x = 1:length(fli)
    for j = 1:length(fli)
```

```
        if isnan(I_fn_psi_theta(x,j)) == 1
            I_fn_psi_theta(x,j) = 1;
        end
    end
end

for x = 1:length(fli)
    for j = 1:length(fli)
        if I_fn_psi_theta(x,j) == 1
            I_fn_psi_theta(x,j) = (I_fn_psi_theta(x-1,j)-I_fn_psi_theta(x-
2,j))+I_fn_psi_theta(x-1,j);
        end
    end
end

% ============================ TORQUE ================================
% Calculating torque table (ttt)
% theta(deg)(theta_spline) - column, mmf(Ni)(mmf_spline) - row

[m,n] = size(suave_torque);

t(:,2:n) = suave_torque(2:m,2:n);

for k = 1:length(theta)
    tt(:,k) = interp1(mmf,t(k,:),mmf_spline,'cubic');
end

ttt = interp2(theta,mmf_spline,tt,theta_spline',mmf_spline,'cubic');

% Using for calculating the referece current(Iref)(from mmf) from the rough torque (tor)
tor = [0 3.5 8.79 14.5 19 25 30.25 35.5 46.58 55 74.25 85.7 93 99 105]';

% ============================ INDUCTANCE TABLE ================================
% Calculating inductance table (induct2)
% theta(deg)(theta_spline) - column, current (I_spline) - row

I_spline = mmf_spline/TURNS;

for k = 2:q
    induct1(k,:) = TURNS*fff(k,:)/I_spline(k);          % I_spline(1) = 0
end
induct2 = induct1(2:q,:);

I_spline1 = I_spline(2:q);

% ==================== DClink_demand ====================
Id(2:5) = [31, 43, 54, 70]';
rpm(1:7) = [100 500 1000    2000    3000    4000    5000];
Id(1) = 0;

DC1(1,1:7) = zeros(1,7);
DC1(2,:) = [1.014616    1.9209917   3.0378897   5.1559521   7.0942549   8.9870674
10.305631];
DC1(3,:) = [1.9202875   3.5470959   5.5445727   9.383206    12.976679   16.176743
18.968187];
DC1(4,:) = [2.9626571   5.2710105   8.1226982   13.672006   18.964966   23.892237
28.299222];
DC1(5,:) = [4.8182  8.0694  12.1059 20.0331 27.6837 34.93   41.6515];

Id_spline = [0:1:100]';
for k = 1:length(rpm)
    DC2(:,k) = interp1(Id,DC1(:,k),Id_spline,'cubic');
end
Idc_demand = DC2;
rpm_spline = rpm;
```

C.2 Simulink program



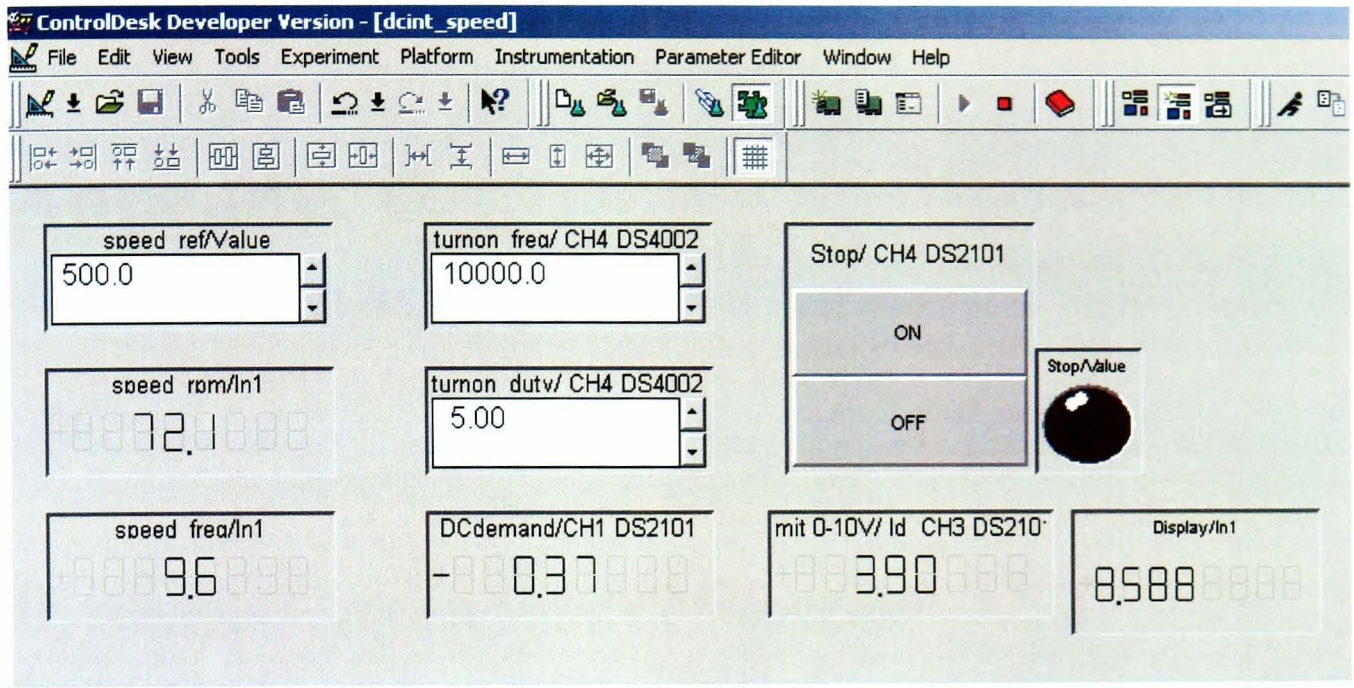
C.3 Real Time Model C-file

```
/**********************************************************************************

   Include file DCInt_speed_usr.c:

   Definition of functions for user-defined initialization,
   system I/O, and background process code.

   RTI1005 4.6 (05-Dec-2003)
   Thu Feb 17 11:12:09 2011

   Copyright (c) 1997-2003 dSPACE GmbH, GERMANY

 **********************************************************************************/

/* ================================================================================ */
/* =====  Define file version macro. Never change this value.  ============== */
/* ================================================================================ */
#define USER_CODE_FILE_VERSION 5
/* ================================================================================ */

/* Insert #include directives for header files here. */

#include "c:\DSPACE\DS1005\RTLib\brtenv.h"
#include "c:\DSPACE\DS1005\RTLib\ds4002.h"
#include "c:\DSPACE\DS1005\RTLib\phsint.h"
#include "c:\DSPACE\DS1005\RTLib\ds2101.h"

#if defined(_INLINE)
# define __INLINE static inline
#else
# define __INLINE static
#endif

dsfloat read_freq = 400, read_duty = 0.5, ped, freq, duty;
dsfloat t_freq[5], t_duty[5];
long edge[12], time[12];
long i, count, j;

dsfloat turnon_freq = 10000.0;
dsfloat reset = 0.95;
dsfloat turnon = 0.05;
dsfloat delay = 2.5e-6;
long state11, state12;
long state41, state42, state43;

dsfloat dcdemand = -0.2;
dsfloat Id = 0.2;
dsfloat stop = 0.5;

static void usr_initialize(void)
{
ds4002_init(DS4002_1_BASE);      /* initialize DS4002 board */
ds4002_read_init(DS4002_1_BASE,3,DS4002_BOTH,0);

ds4002_output_init();                  /* prepare program variables */
ds4002_define_entry();               /* entry point = program start */

/* ch1: main clock genergator, reset signal, triggers to ch4 */
    state11 = ds4002_define_state
    (DS4002_DELAY((1-reset)/turnon_freq),                    /* after delay 0.05/freq */
     DS4002_HIGH,                                  /* set output HIGH */
     0,                                  /* do not trigger or interrupt */
     DS4002_CONTINUE,                      /* continue with next state */
     0);                                /* no loop counter or jump value */

     state12 = ds4002_define_state
```

```
     (DS4002_DELAY(reset/turnon_freq),                /* after delay duty/freq */
     DS4002_LOW,                                   /* set output LOW */
     DS4002_MASK(4) + DS4002_INTERRUPT,
                /* trigger channels 4, generate host interrupt */
     DS4002_GOTO,                 /* goto entry point (= first state) */
     0);                            /* no loop counter or jump value */
ds4002_load_states ( DS4002_1_BASE, 1);
                                  /* download program for channel 1 */

/* ch4 Turn-on signal output */
ds4002_output_init();                /* prepare program variables */
ds4002_define_entry();              /* entry point = program start */
state41 = ds4002_define_state
    (DS4002_WAIT,                             /* wait for trigger event */
    DS4002_LOW,                /* after trigger event set output LOW */
    0,                             /* do not trigger or interrupt */
    DS4002_CONTINUE,                  /* continue with next state */
    0);                             /* no loop counter or jump value */

state42 = ds4002_define_state
    (DS4002_DELAY(delay),      /* after the delay period */
    DS4002_HIGH,                            /* set output HIGH */
    0,                             /* do not trigger or interupt */
    DS4002_CONTINUE,               /* continue with next state */
    0);                           /* no loop counter or jump value */

state43 = ds4002_define_state
    (DS4002_DELAY(turnon/turnon_freq),      /* after turnon duty period */
    DS4002_LOW,             /* set output LOW */
    0,                       /* do not trigger or interupt */
    DS4002_GOTO,             /* go to entry point (=first state) */
    0);                      /* no loop counter or jump value */

ds4002_load_states(DS4002_1_BASE, 4);     /* download program to ch4 */
ds4002_start_channels(DS4002_1_BASE, DS4002_MASK(1)+DS4002_MASK(4));

ds2101_init(DS2101_1_BASE);          /* initialize DS2101 board */
ds2101_set_range(DS2101_1_BASE,1,DS2101_RNG10);
ds2101_set_range(DS2101_1_BASE,3,DS2101_RNG10U);
ds2101_set_range(DS2101_1_BASE,4,DS2101_RNG10U);
}


__INLINE void usr_sample_input(void)
{
}


__INLINE void usr_input(void)
{
j = 0;
count = 12;
ds4002_read_overlapped(DS4002_1_BASE,3,&count,edge,time);
for(i=0; i<(count-2); i++)
    {
    if(edge[i])      /* true = rising, false = falling edge */
        {
        ped = DS4002_TIME2FLOAT(time[i] - time[i+2]);
        freq = 1/(ped);
        t_freq[j] = freq;
        duty = DS4002_TIME2FLOAT(time[i+1] - time[i+2])/ped;
        t_duty[j] = duty;
        j++;
        }
    }

read_freq = (t_freq[1]+t_freq[2]+t_freq[3]+t_freq[4]+t_freq[0])/5;
read_duty = (t_duty[1]+t_duty[2]+t_duty[3]+t_duty[4]+t_duty[0])/5;
s_speed_freq = read_freq;
```

```
}


__INLINE void usr_output(void)
{
turnon_freq = s_turnon_freq;
turnon = s_turnon_duty;

/* update ch1_reset signal */
ds4002_update_state(DS4002_1_BASE, 1, state11,
    DS4002_DELAY ((1-reset)/turnon_freq),                /* after delay (1-
reset)/turnon_freq */
    DS4002_HIGH,                                    /* set output HIGH */
                /* please note:
                update of trigger or interrupt data is not possible! */
    DS4002_CONTINUE,                          /* continue with next state */
    0);                                  /* no loop counter or jump value */

ds4002_update_state(DS4002_1_BASE, 1, state12,
    DS4002_DELAY(reset/turnon_freq),                  /* after reset/turnon_freq */
    DS4002_LOW,                                    /* set output LOW */
    DS4002_GOTO,                    /* goto entry point (= first state) */
    0);                                  /* no loop counter or jump value */

DS4002_EXEC_CMD(DS4002_1_BASE, DS4002_CMD_IMMEDIATE, 1); /* advance
         swinging buffer immediately and update currently used delays */

/* update ch4_turn on signal */
ds4002_update_state(DS4002_1_BASE, 4, state41,
    DS4002_WAIT,         /* wait for the trigger time */
    DS4002_LOW,         /* after trigger event set output LOW */
    DS4002_CONTINUE,     /* continue with the next state */
    0);                  /* no loop counter or jump value */
ds4002_update_state(DS4002_1_BASE, 4, state42,
    DS4002_DELAY(delay),      /* after the delay period */
    DS4002_HIGH,          /* set output HIGH */
    DS4002_CONTINUE,      /* continue with the next state */
    0);                   /* no loop counter or jump value */
ds4002_update_state(DS4002_1_BASE, 4, state43,
    DS4002_DELAY(turnon/turnon_freq),      /* after turnon_duty/turnon_freq period */
    DS4002_LOW,         /* set output LOW */
    DS4002_GOTO,         /* goto entry point (=first state) */
    0);                  /* no loop counter or jump value */
DS4002_EXEC_CMD(DS4002_1_BASE, DS4002_CMD_NEWDATA, 4);
                        /* advance swinging buffer to be used with the next delay */

dcdemand = s_dcdemand;
Id = s_Id;
stop = s_stop;

ds2101_out(DS2101_1_BASE, 1, dcdemand);
ds2101_out_uni(DS2101_1_BASE, 3, Id);
ds2101_out_uni(DS2101_1_BASE, 4, stop);
}


static void usr_terminate(void)
{
}


static void usr_background(void)
{
}


#undef __INLINE

/****** [EOF] ************************************************************/
```

C.4 Control Desk Program



Appendix D

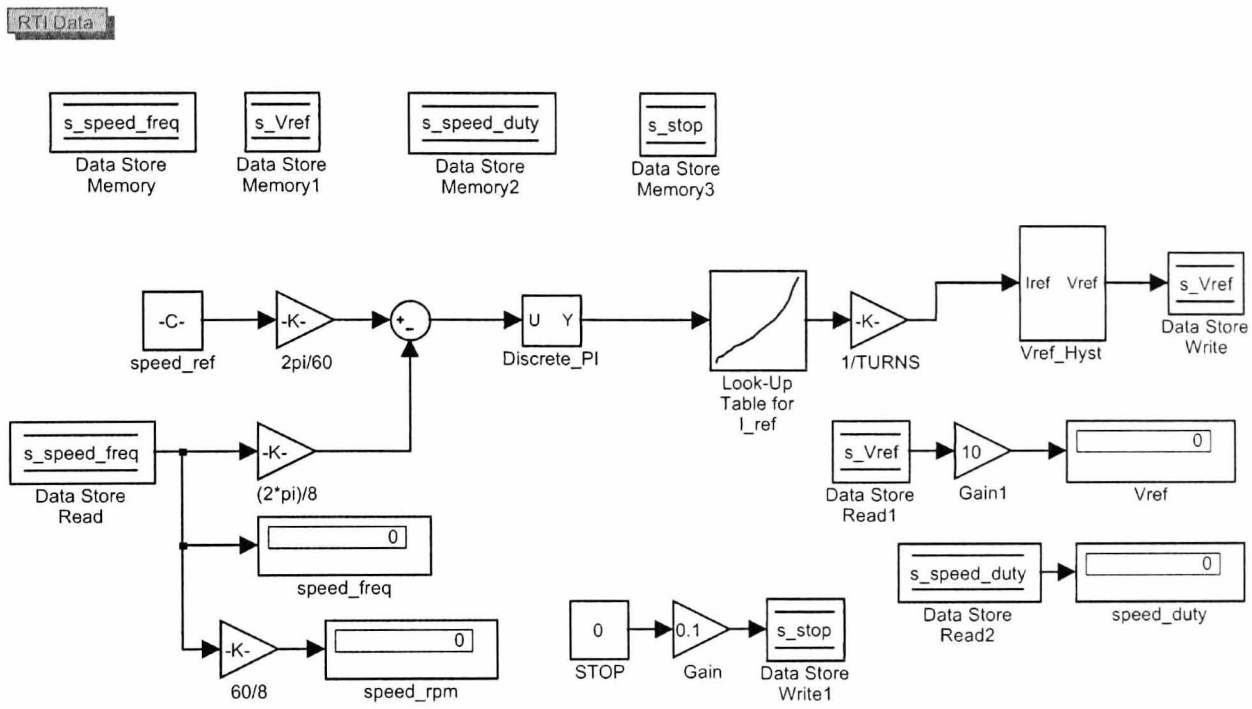
Hysteresis Current Control Programs

D.1 Initial m-file

```
% ========= INITIALISING VALUES FOR Hysteresis SRM Lab ======================

clear

turns_per_phase = 76;                       % number of turns per phase
NR = 8;                                     % number of rotor poles
NS = 12;                                    % number of stator poles
NPH = 3;                                    % number of phases
CYCLE = 360/NR;                             % repeat angle for lookup table = 45 deg
TURNS = turns_per_phase/(NS/NPH);           % number of turns for linkage flux = 19
Rph = 0.17;                                 % phase resistance
J = 0.004;                                  % shaft inertia (RB2009 HP spool) = 0.2
B = 0.0015;                                 % assuming a damping coefficient

VDC = 270;                                  % Input DC Voltage

thetaon = 5;                                % turn-on angle
thetaoff =  thetaon + 15;                       % turn-off angle for Lab
if thetaon < 0
    thetaon = 45 + thetaon;
end

speed_ref = 500;                                % speed of the machine in rpm
Tl = 0;             % torque load (Nm)

Ts = 0.1;        % settling time
zeta = 1.2;          % damping ratio

Bl = Tl/(speed_ref*(2*pi/60));
Kp = (8*J/Ts) - (B + Bl);                   % Kp in PI control
Ki = (4/(Ts*zeta))^2 * J;                   % Ki in PI control

%Idemd = 43;
band = 3.5;

load ('E:\Matlab\DCInt_Analysis\suave_flux.txt')
load ('E:\Matlab\DCInt_Analysis\suave_torque.txt')

% ==================== FLUX ==========================

% Calculating flux table (fff)
% theta(deg)(theta_spline) - column, mmf(Ni)(mmf_spline) - row

q = 100;                                    % Precision

[m,n] = size(suave_flux);
mmf(2:n) = [suave_flux(1,2:n)]';
mmf(1) = 0;
mmf_spline = [0:max(mmf)/(q-1):max(mmf)]';

theta = [suave_flux(2:m,1)]';
theta_spline = [0:max(theta)/(q-1):max(theta)]';

% extract target flux
f(:,2:n) = suave_flux(2:m,2:n)*4;               % Multiply by 4 since the coils connect
in series
f(:,1) = zeros(m-1,1);

for k = 1 : length(theta)
    ff(:,k) = interp1(mmf,f(k,:),mmf_spline,'cubic');
end

fff = interp2(theta,mmf_spline,ff,theta_spline',mmf_spline,'cubic');
```

```
fli = (0:max(max(f))/(q-1):max(max(f)))';

for k = 1:q
    I_fn_psi_theta(:,k) = interp1(fff(:,k),mmf_spline',fli);
end

for x = 1:length(fli)
    for j = 1:length(fli)
        if isnan(I_fn_psi_theta(x,j)) == 1
            I_fn_psi_theta(x,j) = 1;
        end
    end
end

for x = 1:length(fli)
    for j = 1:length(fli)
        if I_fn_psi_theta(x,j) == 1
            I_fn_psi_theta(x,j) = (I_fn_psi_theta(x-1,j)-I_fn_psi_theta(x-
2,j))+I_fn_psi_theta(x-1,j);
        end
    end
end

% ============================ TORQUE ================================
% Calculating torque table (ttt)
% theta(deg)(theta_spline) - column, mmf(Ni)(mmf_spline) - row

[m,n] = size(suave_torque);

t(:,2:n) = suave_torque(2:m,2:n);

for k = 1:length(theta)
    tt(:,k) = interp1(mmf,t(k,:),mmf_spline,'cubic');
end

ttt = interp2(theta,mmf_spline,tt,theta_spline',mmf_spline,'cubic');

% Using for calculating the referece current(Iref)(from mmf) from the rough torque (tor)
tor = [0 3.5 8.79 14.5 19 25 30.25 35.5 46.58 55 74.25 85.7 93 99 105]';
```

D.2 Simulink program



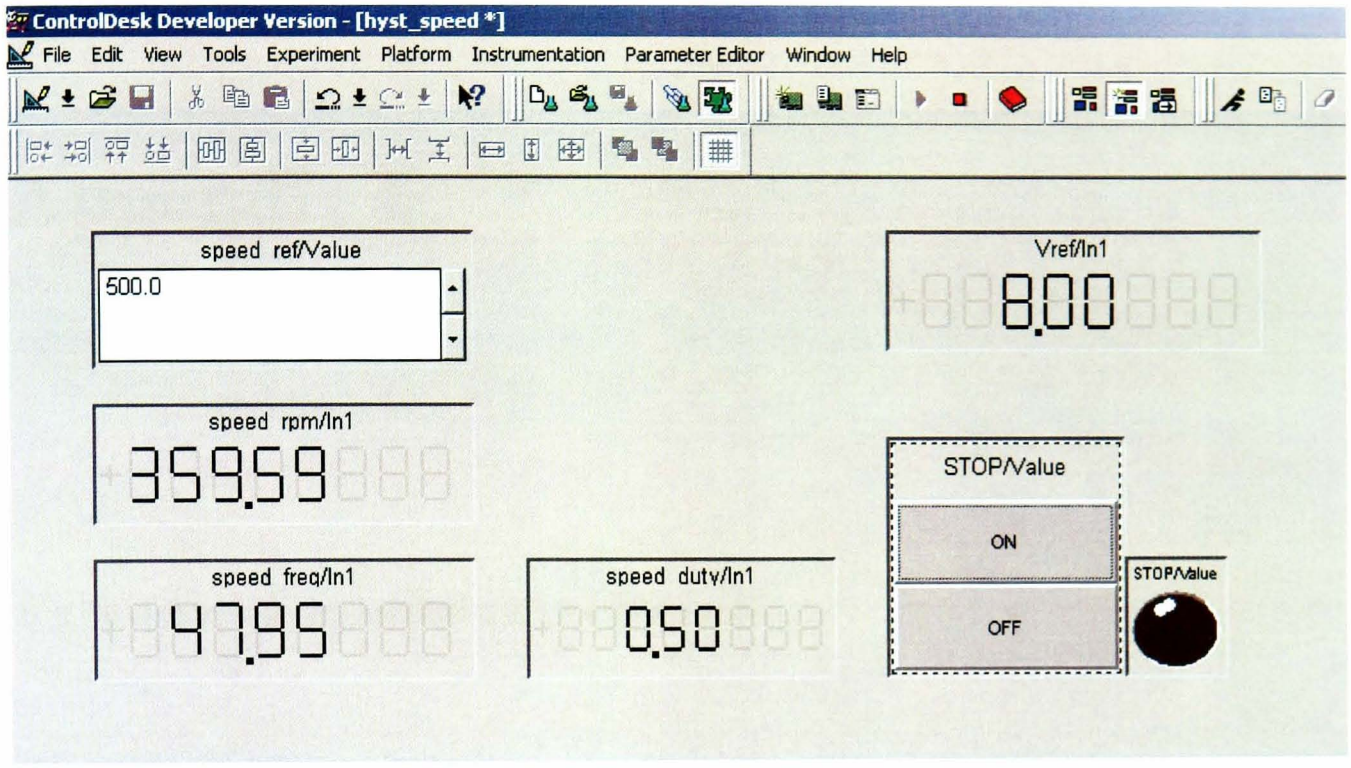
D.3 Real Time Model C-file

```
/**********************************************************************************

   Include file Hyst_speed_usr.c:

   Definition of functions for user-defined initialization,
   system I/O, and background process code.

   RTI1005 4.6 (05-Dec-2003)
   Thu Dec 16 16:09:32 2010

   Copyright (c) 1997-2003 dSPACE GmbH, GERMANY

 **********************************************************************************/

/* ================================================================================ */
/* =====  Define file version macro. Never change this value.  ============== */
/* ================================================================================ */
#define USER_CODE_FILE_VERSION 5
/* ================================================================================ */

/* Insert #include directives for header files here. */

#include "c:\DSPACE\DS1005\RTLib\brtenv.h"
#include "c:\DSPACE\DS1005\RTLib\ds4002.h"
#include "c:\DSPACE\DS1005\RTLib\phsint.h"
#include "c:\DSPACE\DS1005\RTLib\ds2101.h"

#if defined(_INLINE)
# define __INLINE static inline
#else
# define __INLINE static
#endif

dsfloat read_freq = 400, read_duty = 0.5, ped, freq, duty;
dsfloat t_freq[5], t_duty[5];
long edge[12], time[12];
long i, count, j;

dsfloat Vref = 0.5, stop = 0.0;

static void usr_initialize(void)
{
ds4002_init(DS4002_1_BASE);      /* initialize DS4002 board */
ds4002_read_init(DS4002_1_BASE,3,DS4002_BOTH,0);

ds2101_init(DS2101_1_BASE);      /* initialize DS2101 board */
ds2101_set_range(DS2101_1_BASE,1,DS2101_RNG10U);
ds2101_set_range(DS2101_1_BASE,2,DS2101_RNG10U);
}


__INLINE void usr_sample_input(void)
{
}


__INLINE void usr_input(void)
{
j = 0;
count = 12;
ds4002_read_overlapped(DS4002_1_BASE,3,&count,edge,time);
for(i=0; i<(count-2); i++)
    {
    if(edge[i])      /* true = rising, false = falling edge */
        {
```

```
        ped = DS4002_TIME2FLOAT(time[i] - time[i+2]);
        freq = 1/(ped);
        t_freq[j] = freq;
        duty = DS4002_TIME2FLOAT(time[i+1] - time[i+2])/ped;
        t_duty[j] = duty;
        j++;
        }
    }

read_freq = (t_freq[1]+t_freq[2]+t_freq[3]+t_freq[4]+t_freq[0])/5;
read_duty = (t_duty[1]+t_duty[2]+t_duty[3]+t_duty[4]+t_duty[0])/5;
s_speed_freq = read_freq;
s_speed_duty = read_duty;
}


__INLINE void usr_output(void)
{
Vref = s_Vref;
stop = s_stop;
ds2101_out_uni(DS2101_1_BASE, 1, Vref);
ds2101_out_uni(DS2101_1_BASE, 2, stop);
}


static void usr_terminate(void)
{
}


static void usr_background(void)
{
}
```

```
#undef __INLINE

/****** [EOF] ************************************************************/
```

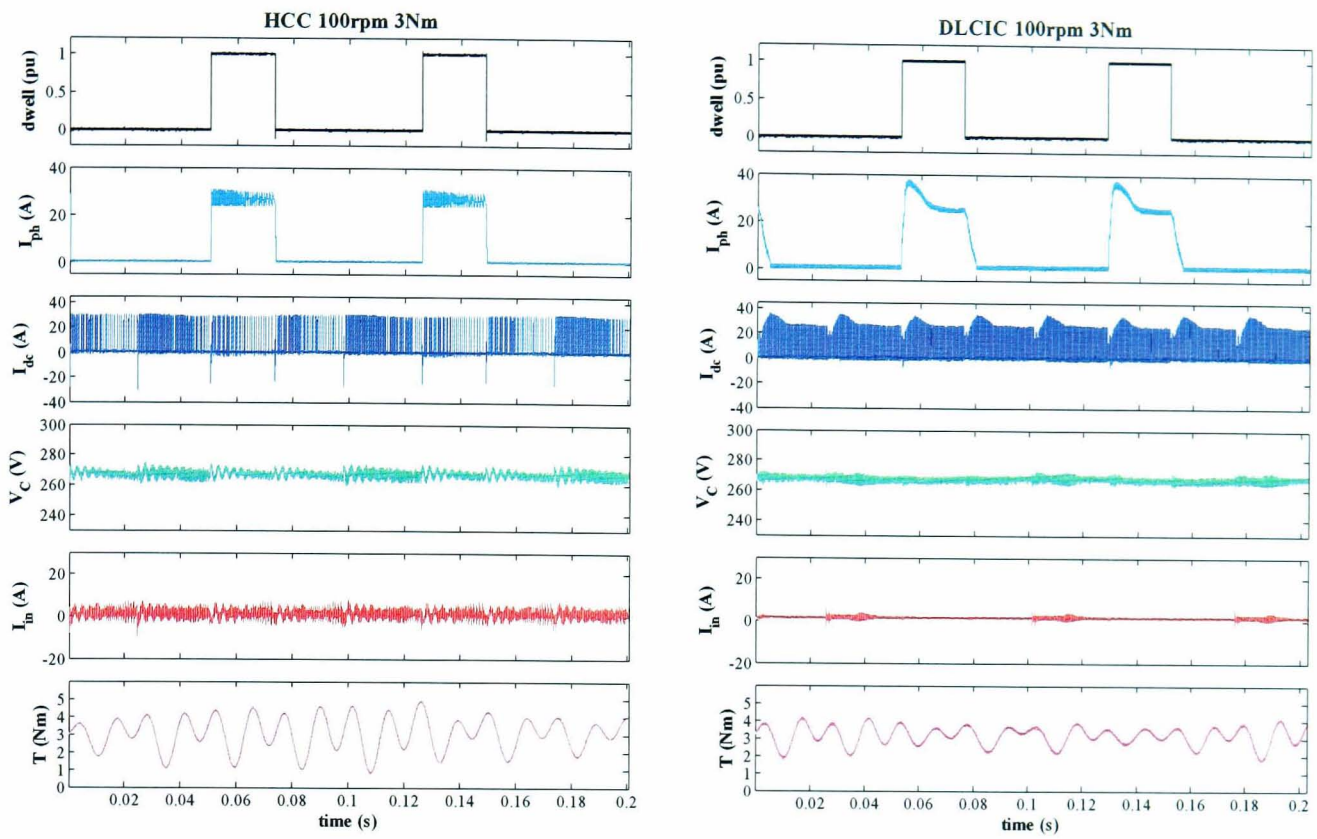
D.4 Control Desk Program



Appendix E

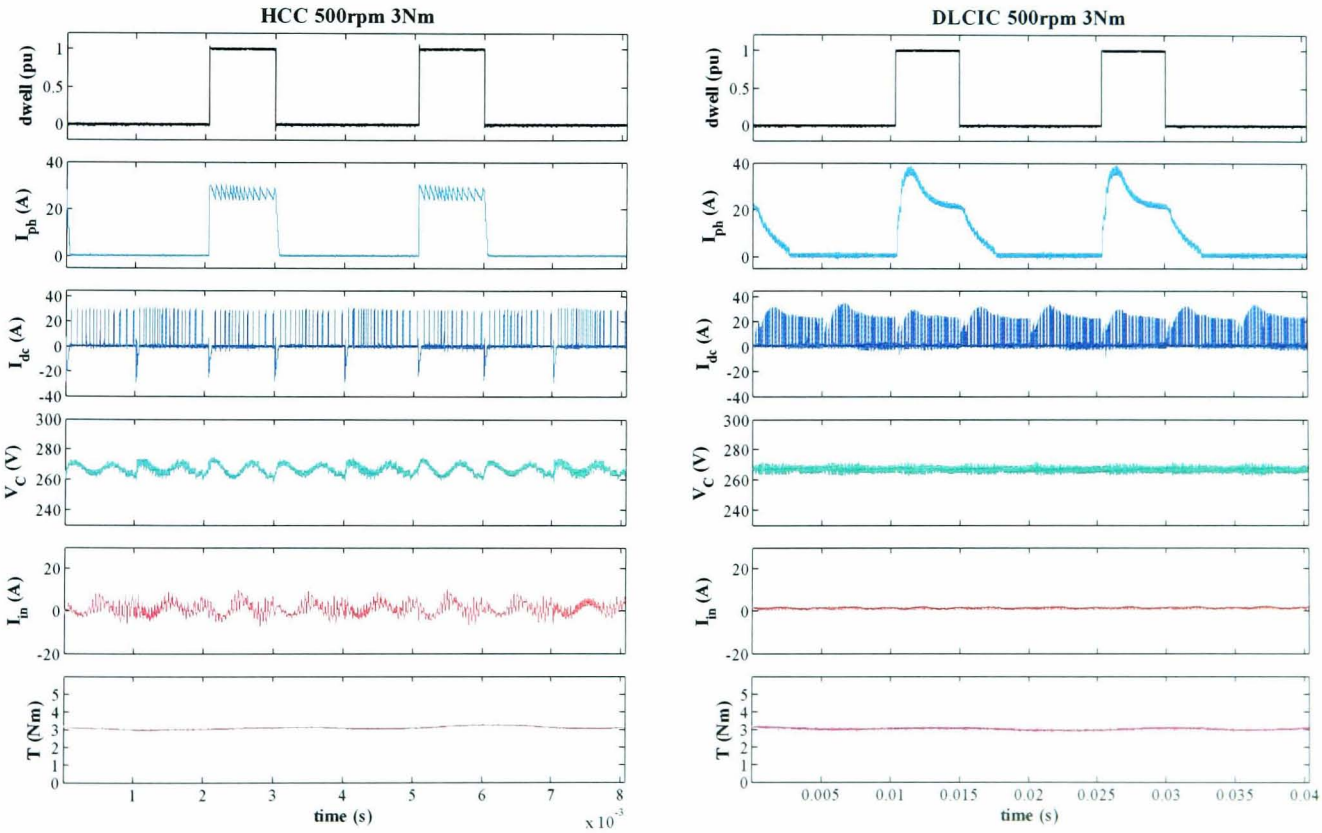
Extended Experimental Results

E.1 Load torque 3 Nm



(a) (b)

Figure E.1: Experimental results at 3Nm 100 rpm



(a) (b)

Figure E.2: Experimental results at 3Nm 500 rpm

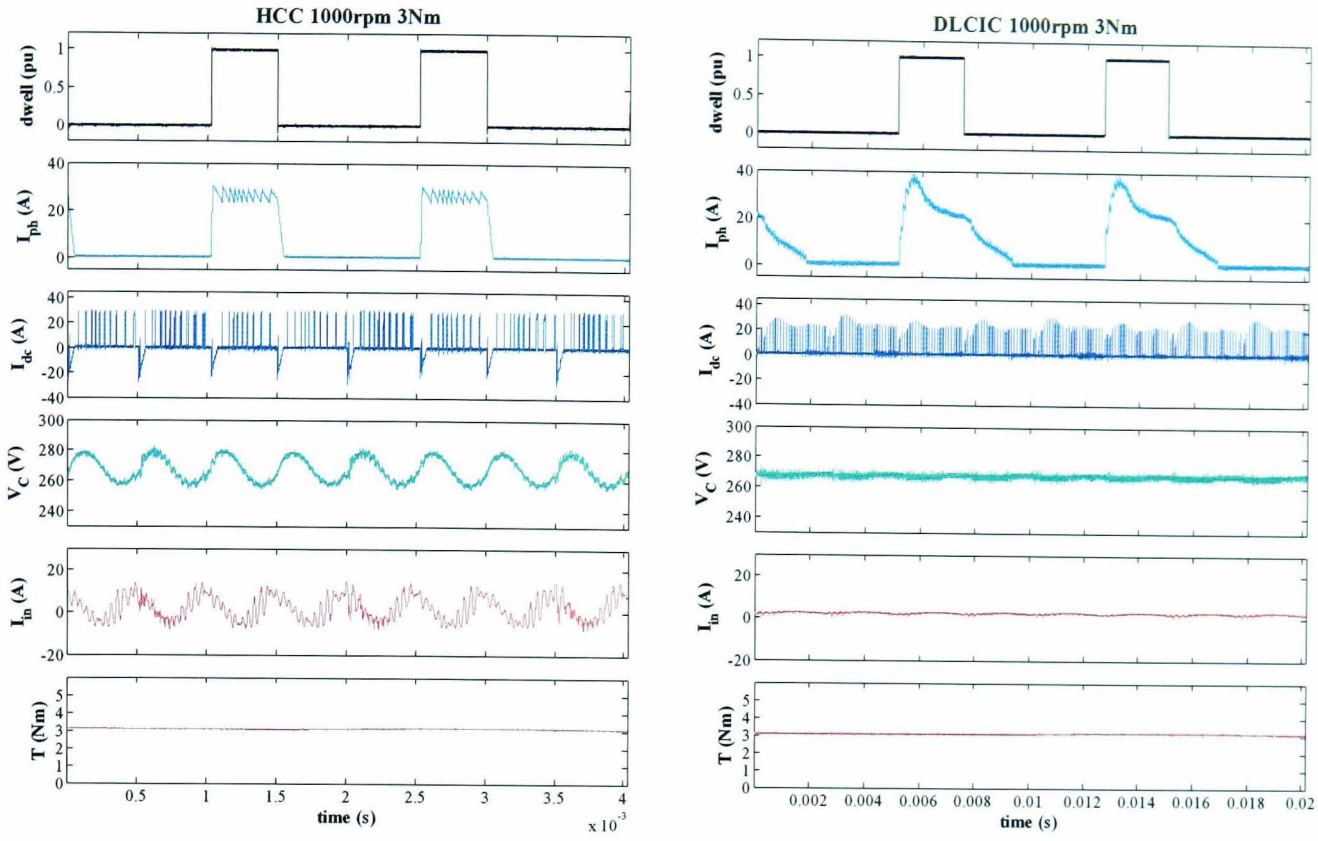


Figure E.3: Experimental results at 3Nm 1000 rpm

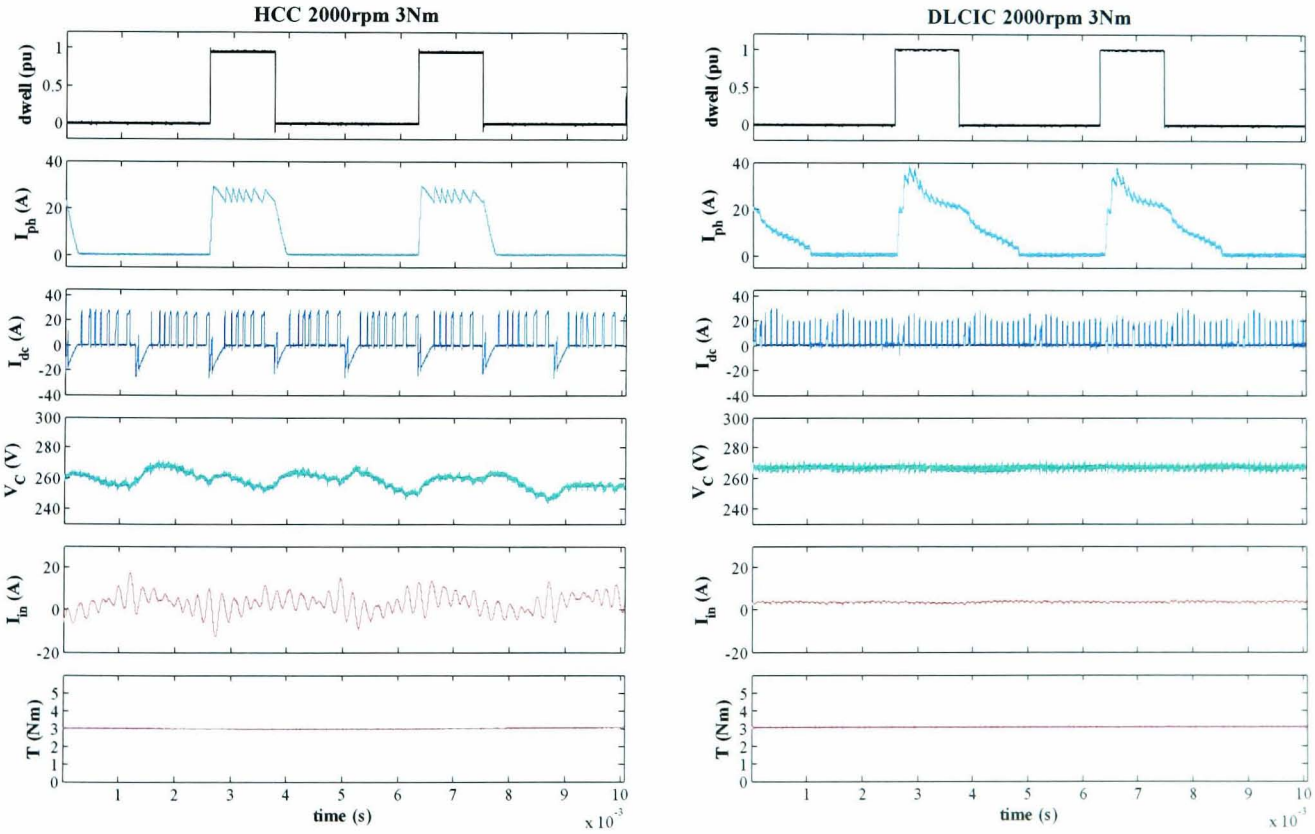


Figure E.4: Experimental results at 3Nm 2000 rpm

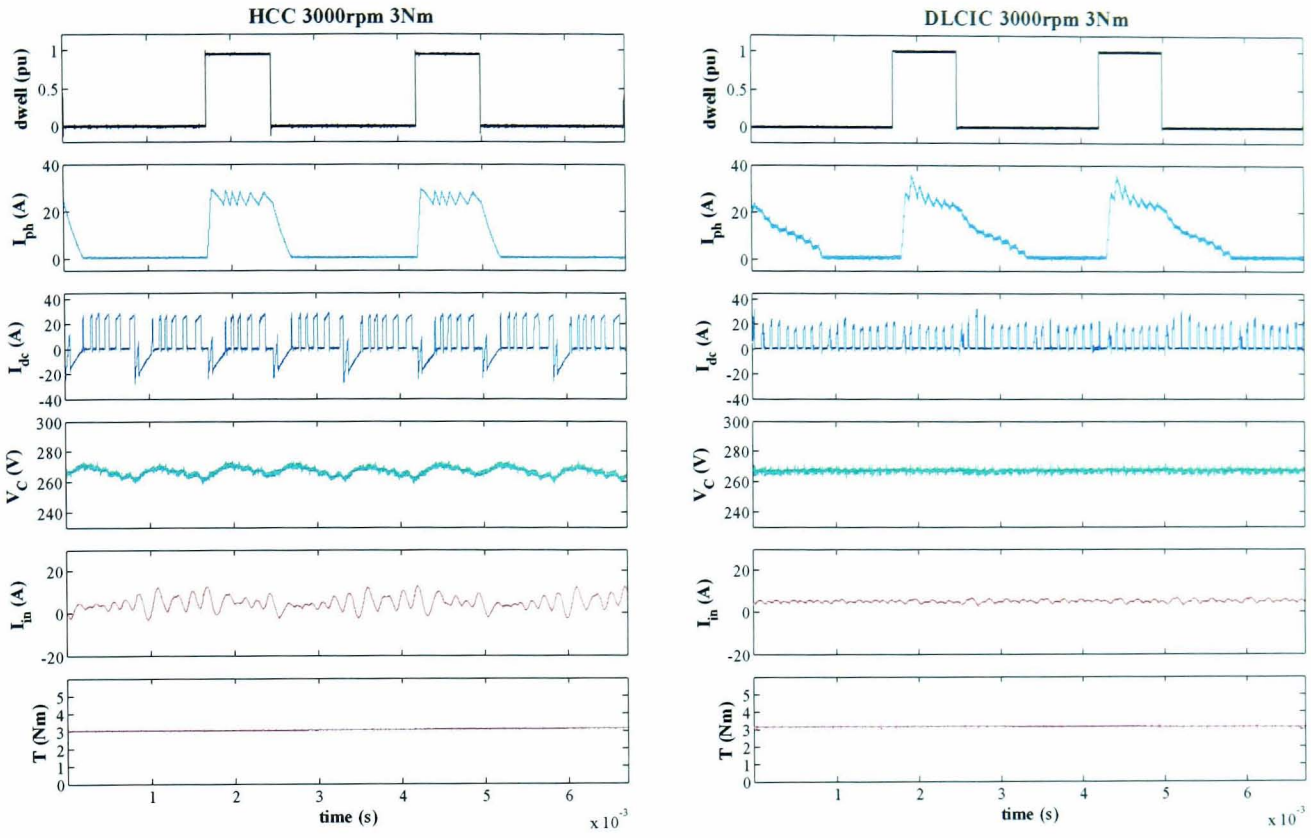
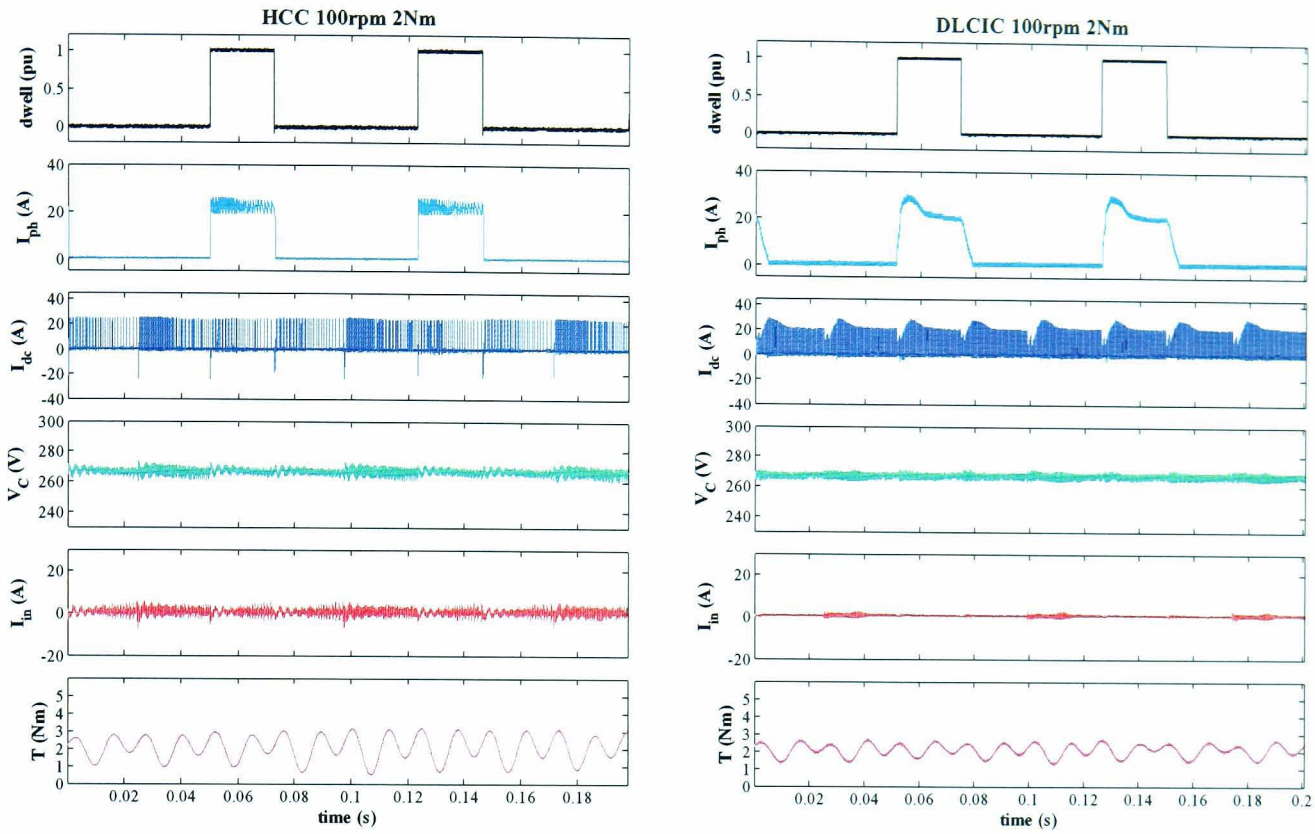


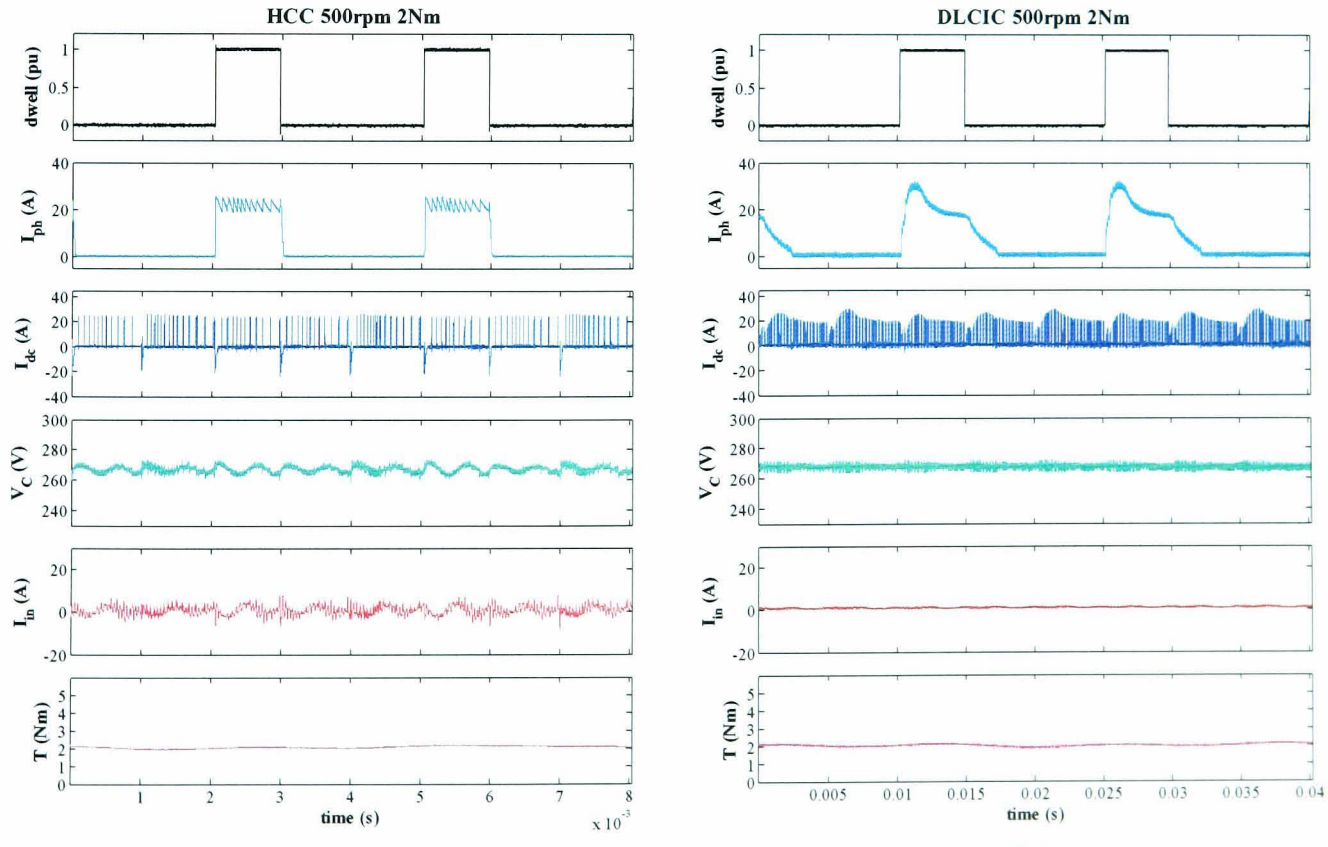
Figure E.5: Experimental results at 3Nm 3000 rpm

E.2 Load torque 2 Nm



(a) (b)

Figure E.6: Experimental results at 2Nm 100 rpm



(a) (b)

Figure E.7: Experimental results at 2Nm 500 rpm

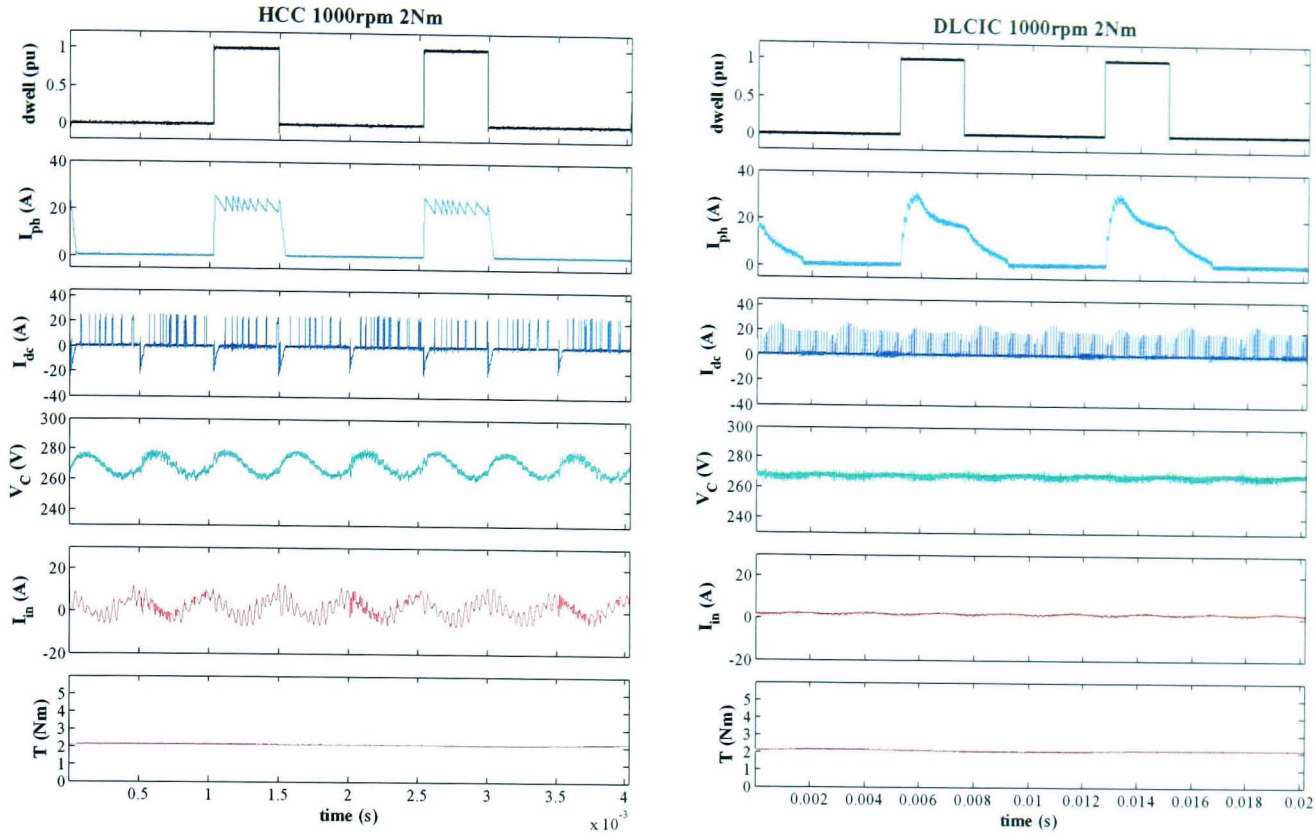


Figure E.8: Experimental results at 2Nm 1000 rpm

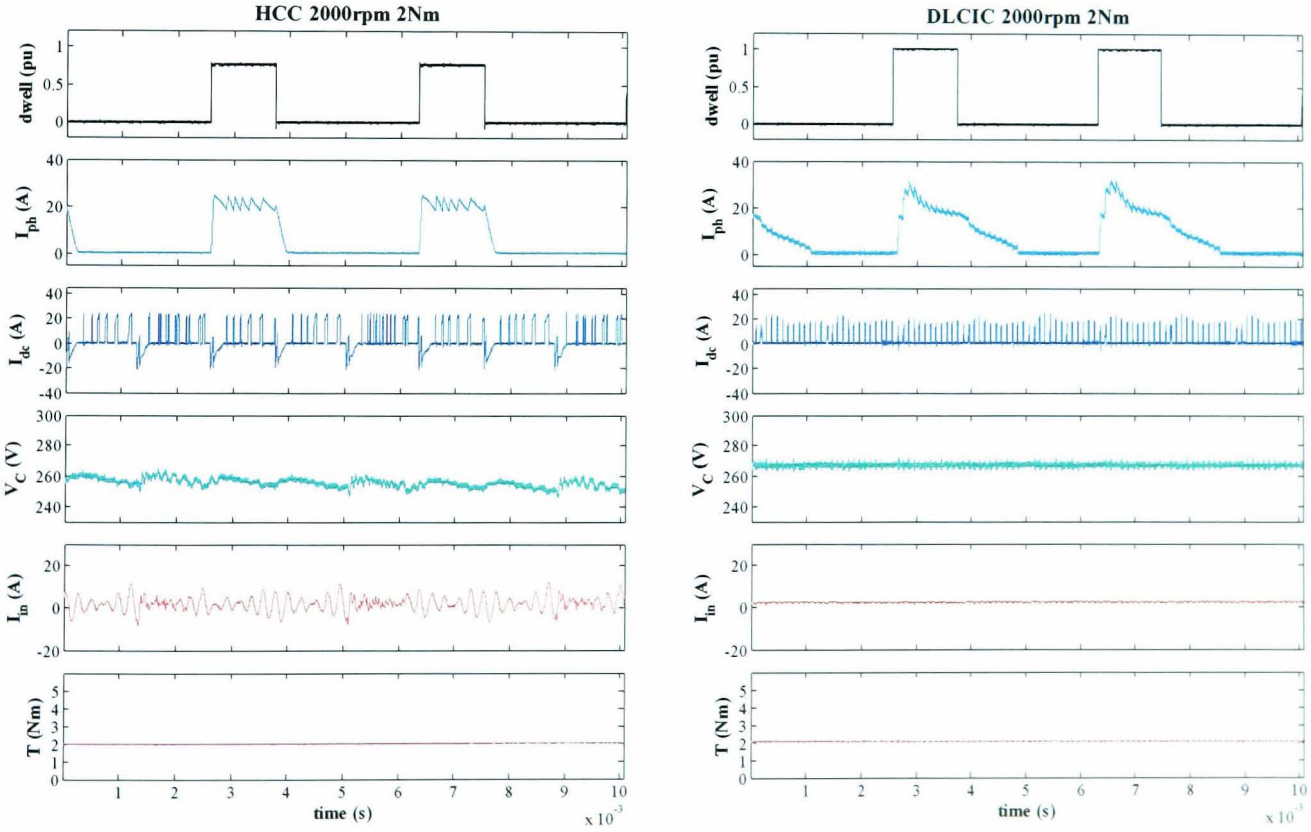


Figure E.9: Experimental results at 2Nm 2000 rpm

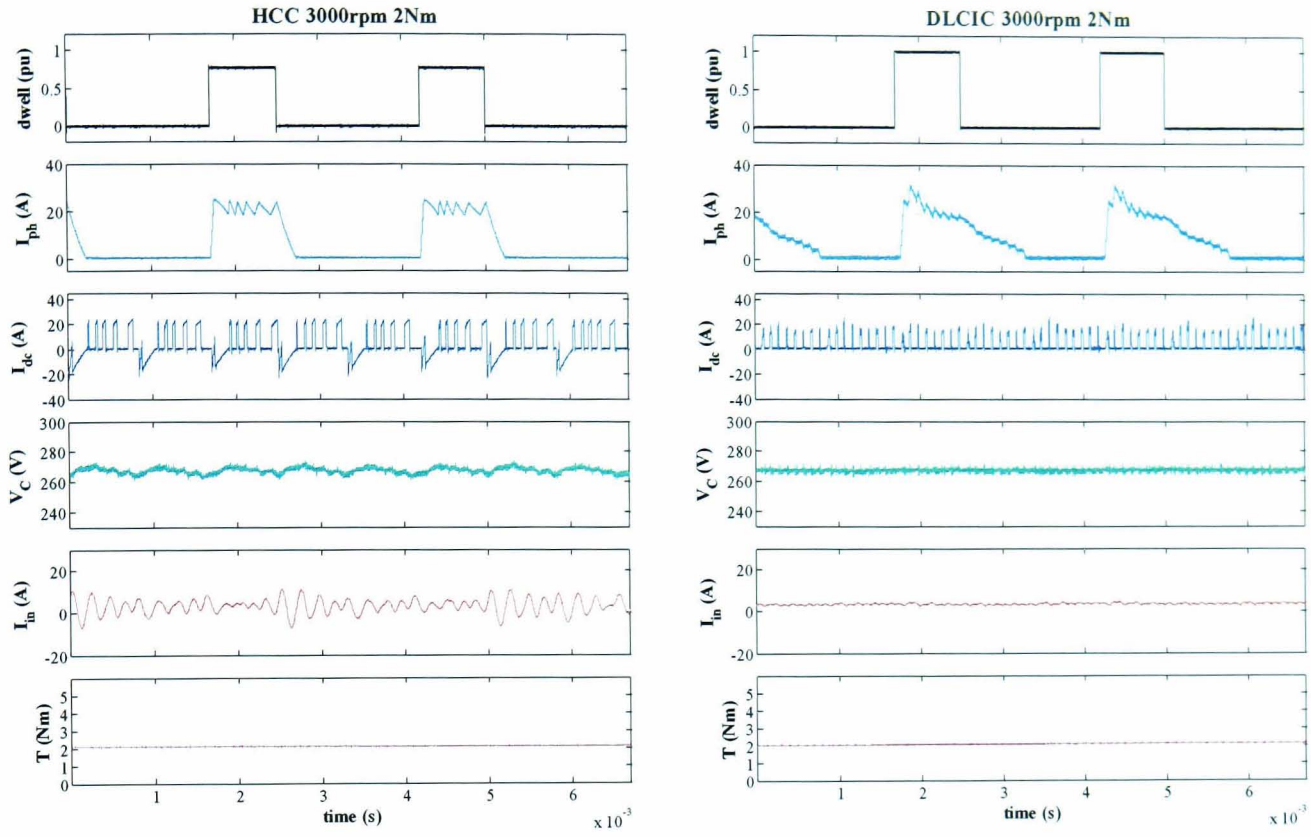
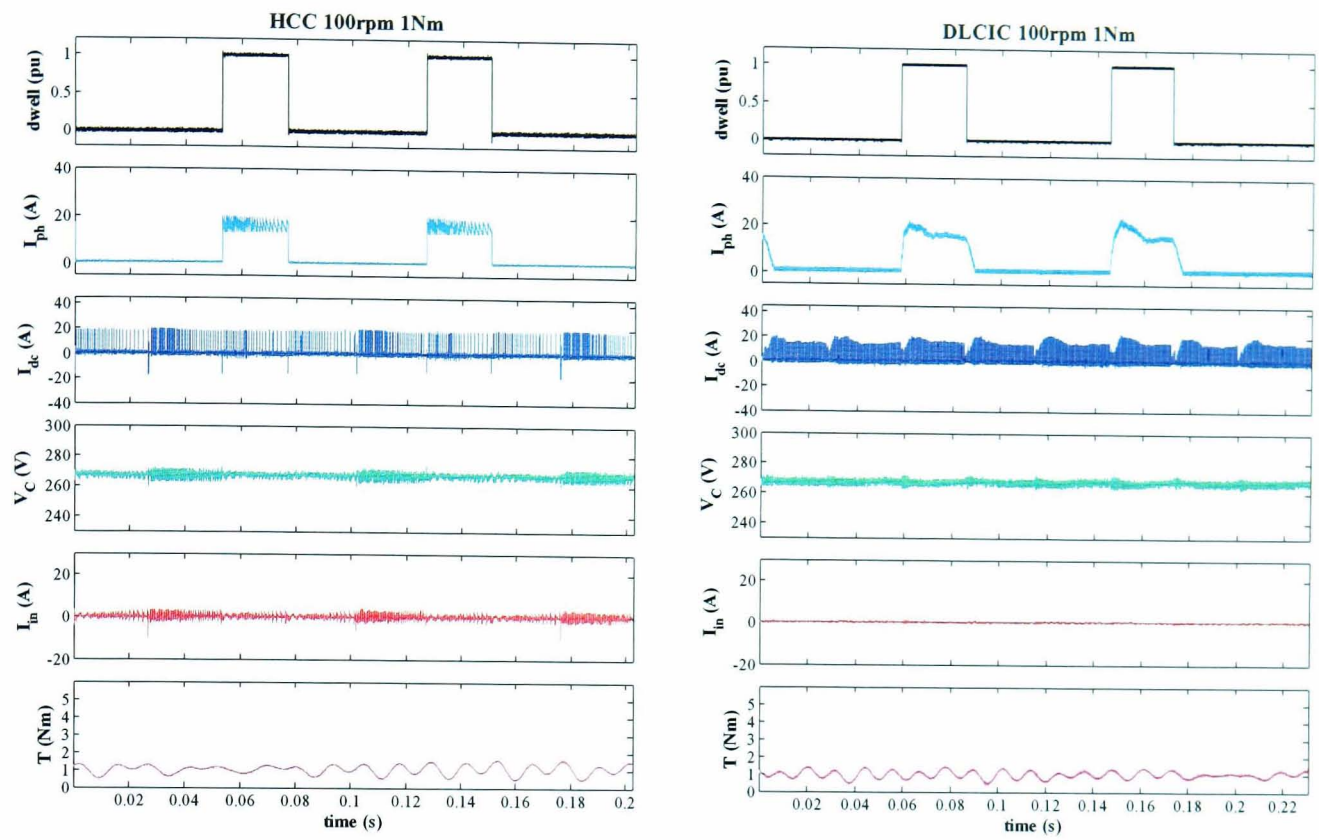


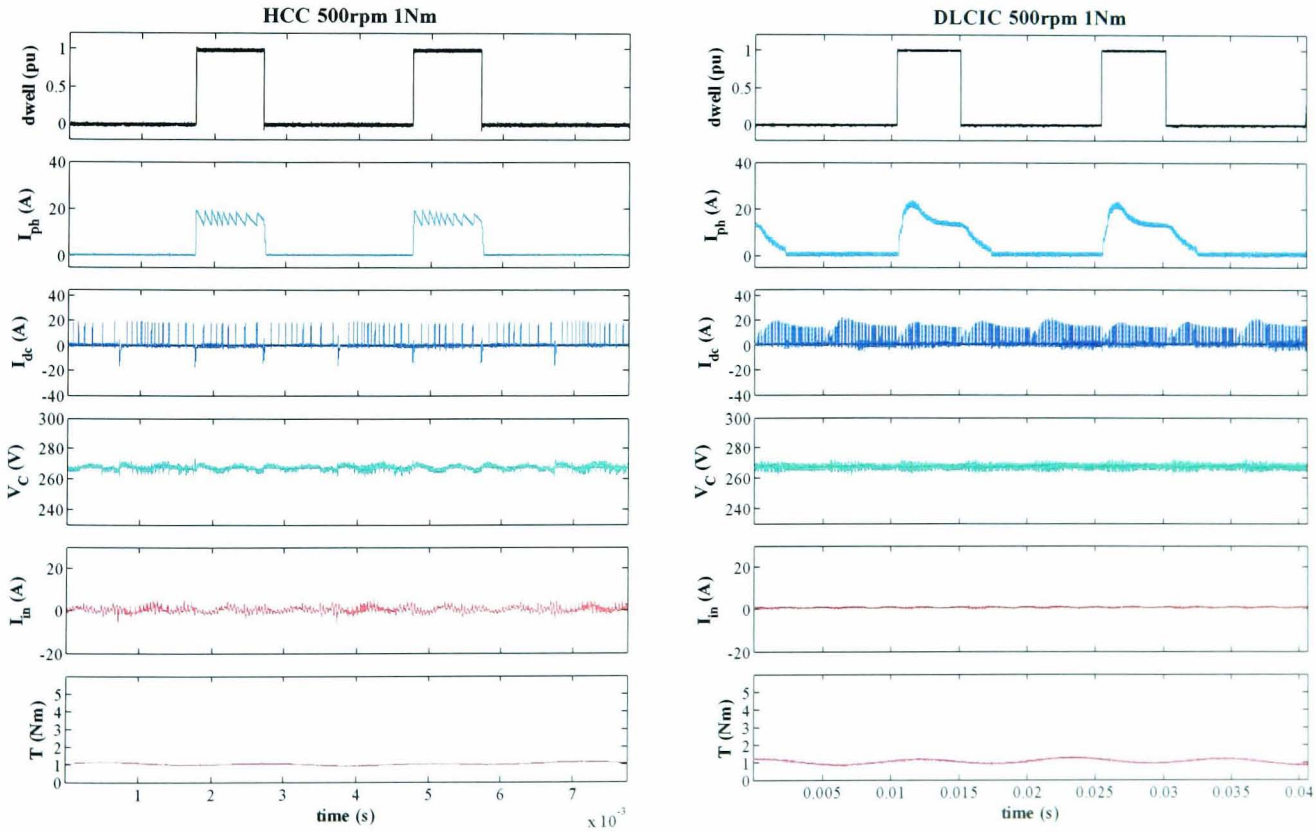
Figure E.10: Experimental results at 2Nm 3000 rpm

E.3 Load torque 1 Nm



(a) (b)

Figure E.11: Experimental results at 1Nm 100 rpm



(a) (b)

Figure E.12: Experimental results at 1Nm 500 rpm

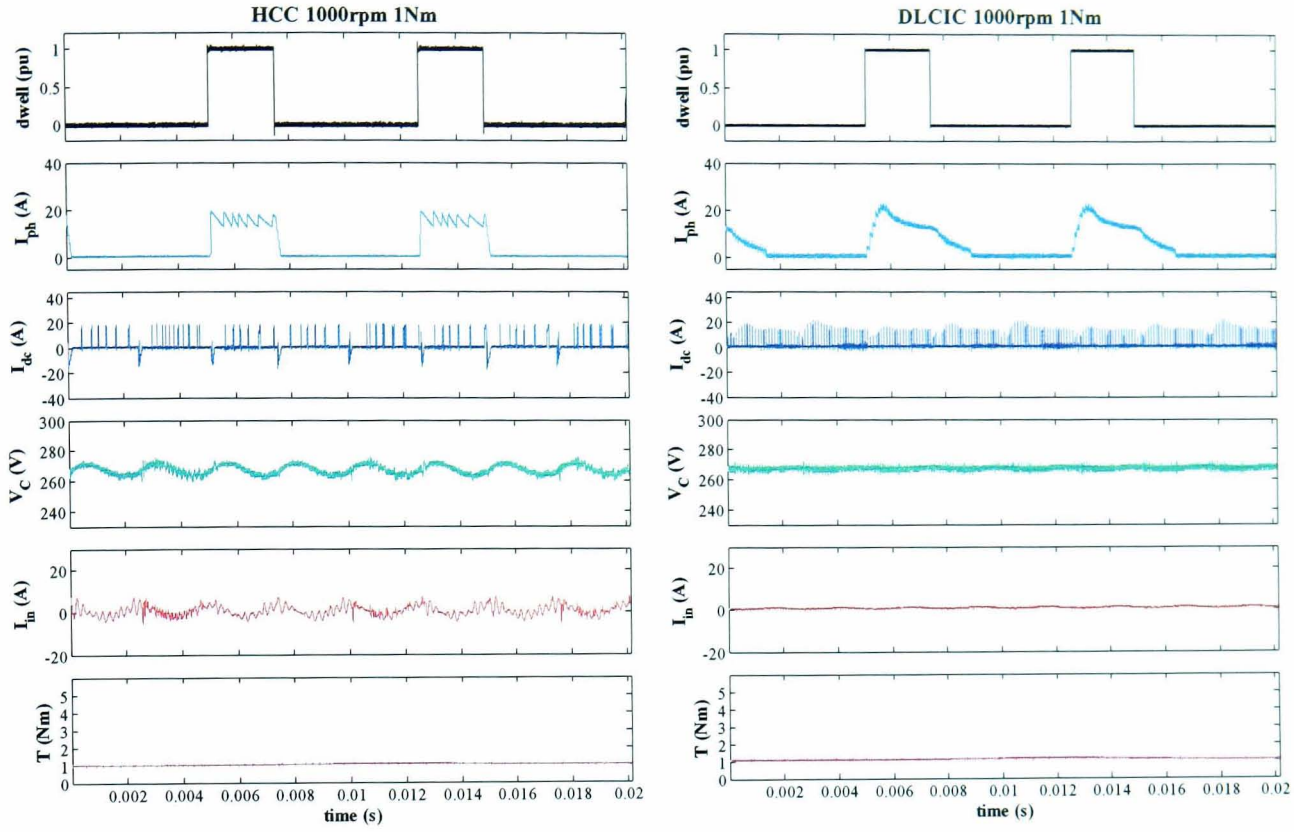


Figure E.13: Experimental results at 1Nm 1000 rpm

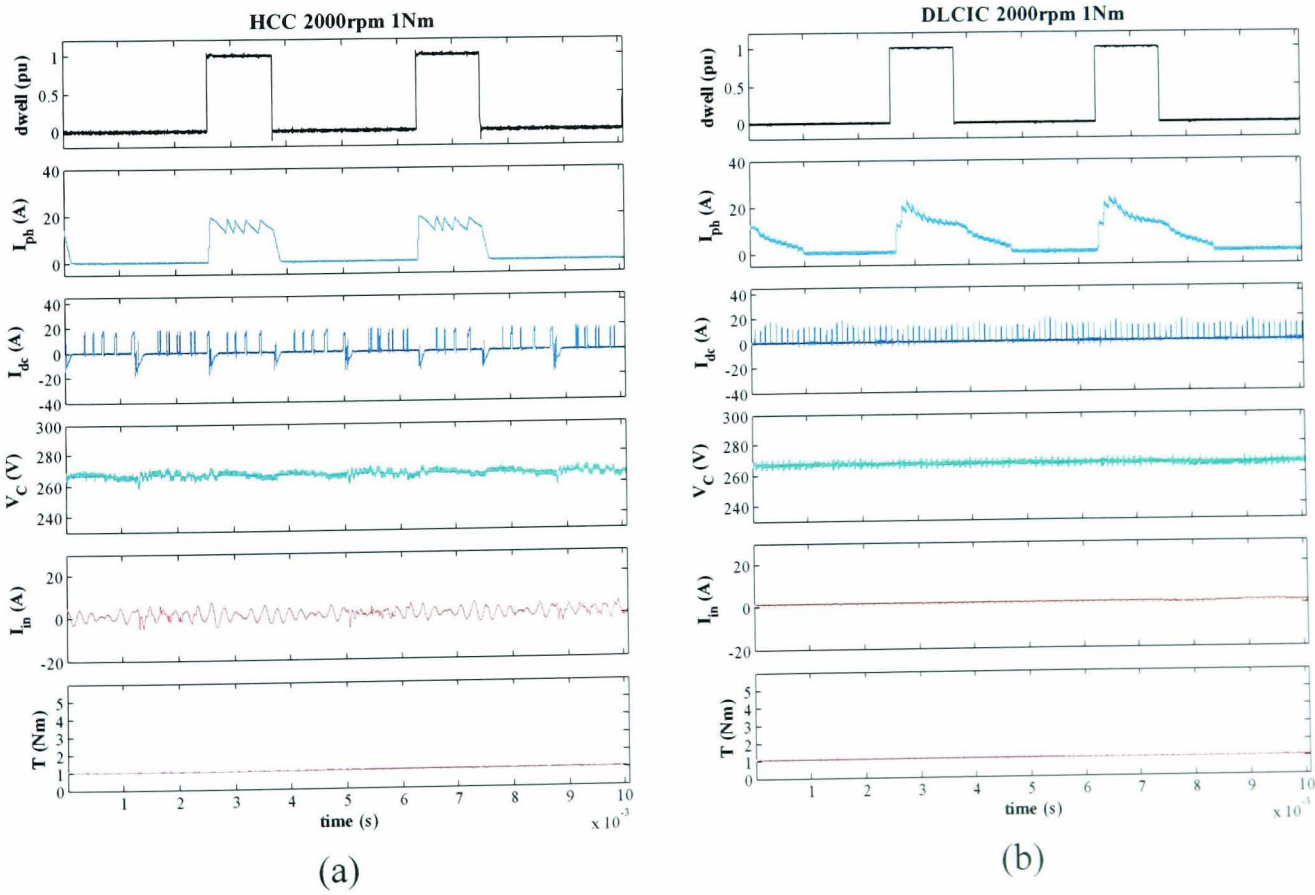


Figure E.14: Experimental results at 1Nm 2000 rpm

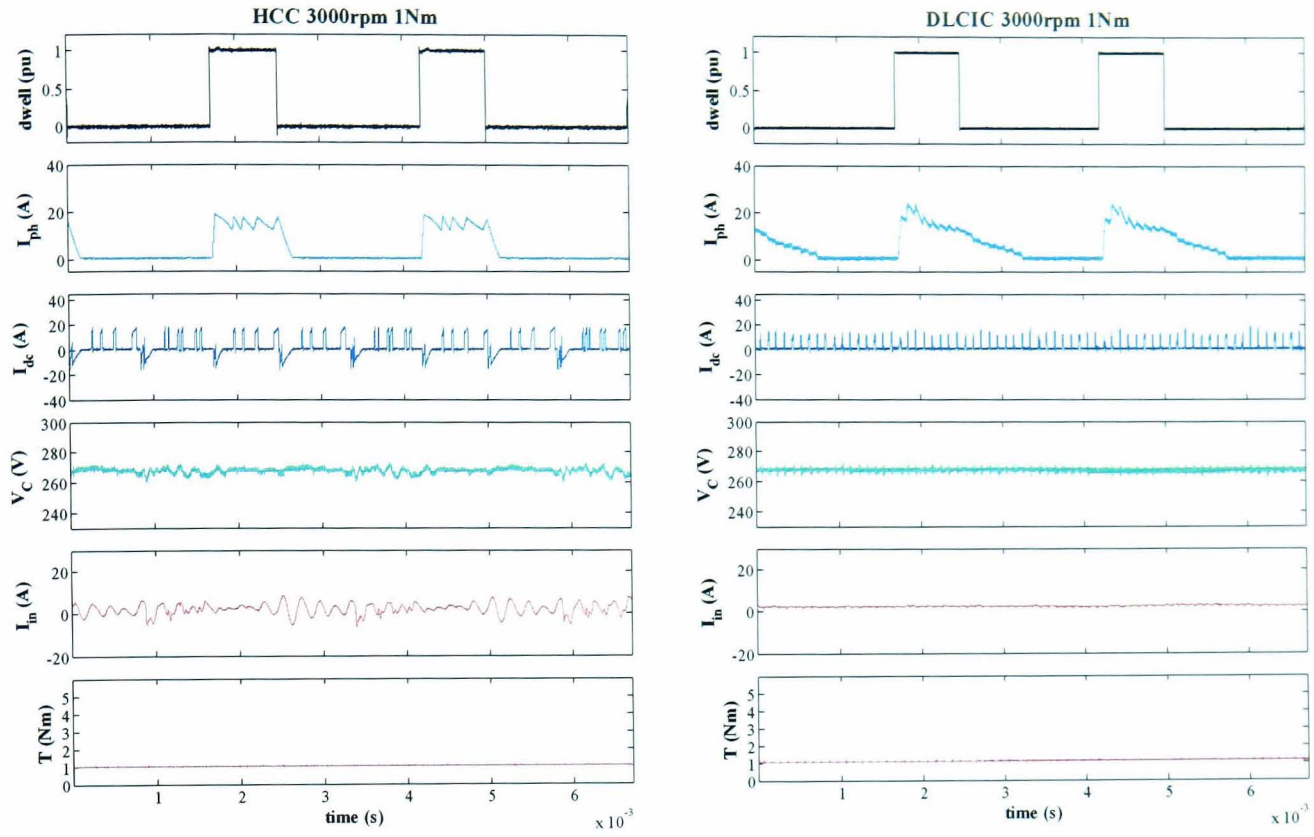


Figure E.15: Experimental results at 1Nm 3000 rpm

Appendix F

List of publications

The work presented in this thesis has be disseminated by publications at international conferences, details of which are given below.

W. Suppharangsan and J. Wang, "A new switching technique for DC-link capacitor minimisation in switched reluctance machine drives," in *Proc. Power Electronics, Machines and Drives (PEMD 2010), 5th IET International Conference on*, 2010, pp. 1-6.

W. Suppharangsan and J. Wang, "Experimental Validation of a New Switching Technique for Dc-link Capacitor Minimisation in Switched Reluctance Machine Drives," poster session presented at *6th IET International Conference*, Bristol UK, 2012.