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Impedance Control and Stability of DC/DC Converter Systems

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Abstract

Cascaded DC/DC converter systems (or 'cascaded systems') have instability problems; i.e., although the subsystems may work well individually, the whole system may be instable due to the impedance interaction among these subsystems. To solve this problem, a family of impedance-based stabilisation methods are proposed in this thesis.

First, parallel-virtual-impedance (PVI) and series-virtual-impedance (SVI) control strategies are proposed to stabilise cascaded systems via shaping the load input impedance. Theoretically, the PVI or SVI control strategy connect a virtual impedance in parallel or series with the input port of the load converter so that the magnitude or phase of the load input impedance can be modified within a very small frequency range. Therefore, with the PVI or SVI control strategy, the cascaded system can be stabilised with minimal compromise of the load performance. Then, based on the PVI and SVI control strategies, adaptive-PVI (APVI) and adaptive-SVI (ASVI) control strategies are proposed by introducing an adaptive mechanism to change the impedance. With the APVI or ASVI control strategy, the load converter can be stably connected to different source converters without changing its internal structure. It is also shown that the ASVI control strategy is better than the APVI control strategy and can make the cascaded system more stable. Moreover, a minimum-ripple-point-tracking (MRPT) controller is proposed and utilised to solve the potential problem of the ASVI control strategy. Finally, a source-side SVI (SSVI) control strategy and a *VRLC* damper are proposed to stabilise the cascaded system with better source performance or input filter performance, respectively.

All the proposed stabilisation and control methods are validated by extensive experimental results.

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Nomenclature

AACC Adaptive active capacitor converter

APVI Adaptive parallel virtual impedance

ASVI Adaptive series virtual impedance

CCM Continuous current mode

CPL Constant power load

CPS Centralized power system

DCM Dis-continuous current mode

DPS Distributed power system

DSP Digital signal processor

EMI Electro magnetic interference

FPGA Field programmable gate array

GaN Gallium Nitride

GM Gain margin

MCU Micro-controller unit

MPPT Maximum power point tracking

MRP Minimum ripple point

MRPT Minimum Ripple point tracking

PI Proportional integral

PLL Phase-locked-loop

PM Phase margin

PO Perturb and observe

PV Photovoltaic

PVI Parallel virtual impedance

PWM Pulse width modulation

Q Quality factor

SAC Stabilized via amplitude compensation

SiC Silicon Carbide

SPC Stabilized via phase compensation

SSVI Source-side series virtual impedance

STA Sinusoidal tracking algorithum

SVI Series virtual impedance

THD Total harmonic distortion

UPS Uninterrupted power supply

VRLC Virtual RLC

ZOH Zero-order hold

Chapter 1

Introduction

1.1 Background

Nowadays, there are two types of 'power supply' architectures (Luo, 2005), centralised power system (CPS) and distributed power system (DPS). Fig. 1.1 illustrates the structures of CPS and DPS.

Fig. 1.1(a) shows the two typical features of CPS (Luo, 2001): a) there is only one power conversion stage in CPS, and b) there are many output voltages generated by CPS. The advantages of CPS include its concentrating of all power processing and thermal management technologies into a single converter that can be designed, subcontracted, or purchased as a stand-alone item (Bo, 2003). As a result, CPS is very popular in traditional electronic equipment, i.e., old computer or server power supply systems (Bodi, 1988). However, the CPS has two unavoidable disadvantages (Ye et al., 2002; Ren et al., 2005): a) It is not easy to achieve redundant design; b) Partial failure may destroy the whole system. These drawbacks mean that the CPS often fails to provide adequate performance for new generations of electronic equipment, especially for some large power applications such as space stations (Thomas and Hallinan, 1990; Lee et al., 1988), aircraft (Sarlioglu and Morris, 2015), new communication systems (Liu et al., 2007b), electrical vehicles (Emadi et al., 2006) and renewable energy systems (Arai et al., 2008).

DPS was developed in order to overcome the drawbacks of CPS (Thorsell, 1990; Schulz et al., 1990; Karlsson and Svensson, 2003). As shown in Fig. 1.1(b), DPS has the following characteristics (Luo, 2001): a) there are multiple power conversion stages in DPS; b)

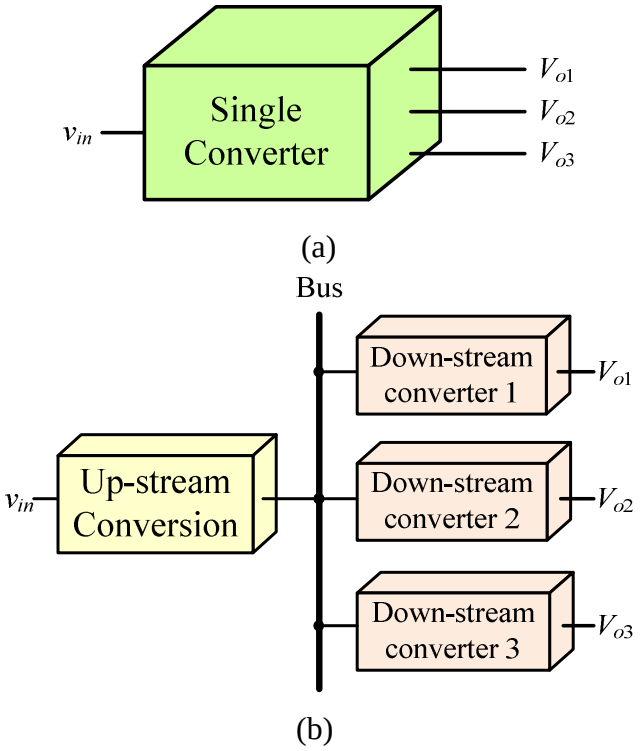


Figure 1.1: Two types of 'power supply' architectures: (a) CPS. (b) DPS (Luo, 2005).

intermediate voltage bus is around the whole system; c) multiple upstream or downstream power converters are connected to the same voltage bus; d) each downstream power converter is located near its own load to provide the load voltage. It is worthy of mention that, in Fig. 1.1(b), the upstream conversion stage could be either a power converter or an electro-magnetic interference (EMI) filter. With these characteristics, the major disadvantages of CPS are entirely eliminated by DPS, and a consequence DPS is becoming increasingly popular (Boroyevich et al., 2010).

However, DPS also has two disadvantages: a) as DPS is formed by lots of power converters, its cost is higher than that of CPS; and b) the interaction between the power converters may cause instability problems for the entire DPS. The former shortage is unavoidable in practice, i.e., if the DPS is utilised, its relatively high cost should be accepted. However for the latter shortage, the instability problem can be solved by effective stabilisation methods. That is also the main research topic in this thesis.

DPS can be divided into DC DPS (Hua et al., 1994) and AC DPS (Shi et al., 2014), according to types of intermediate voltage bus. A typical DC DPS is presented in Fig.

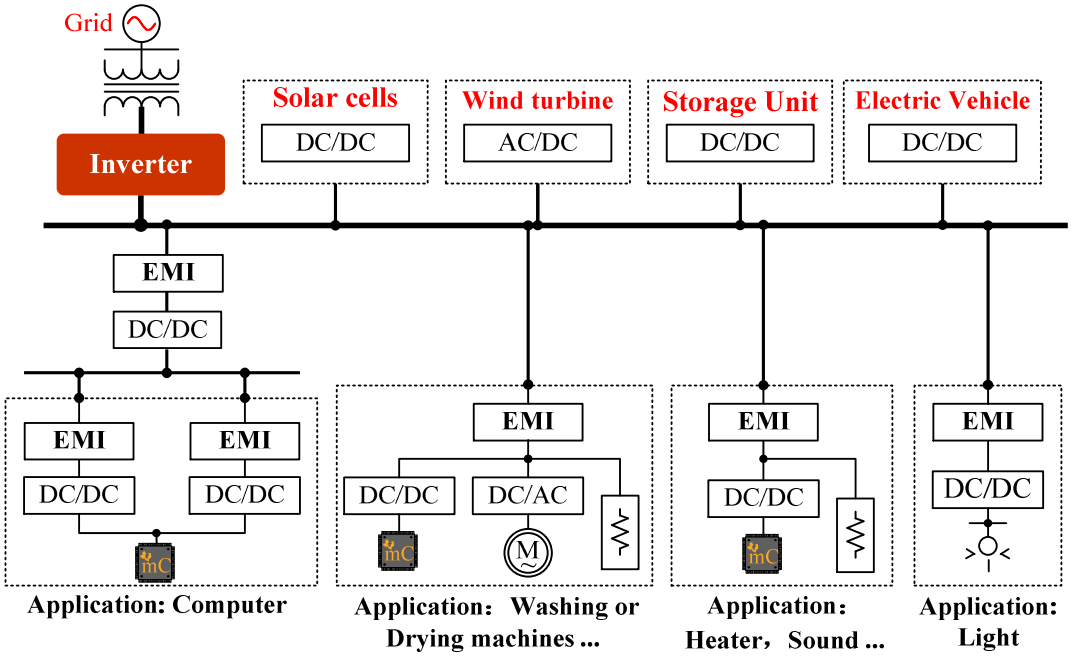


Figure 1.2: A typical DC DPS.

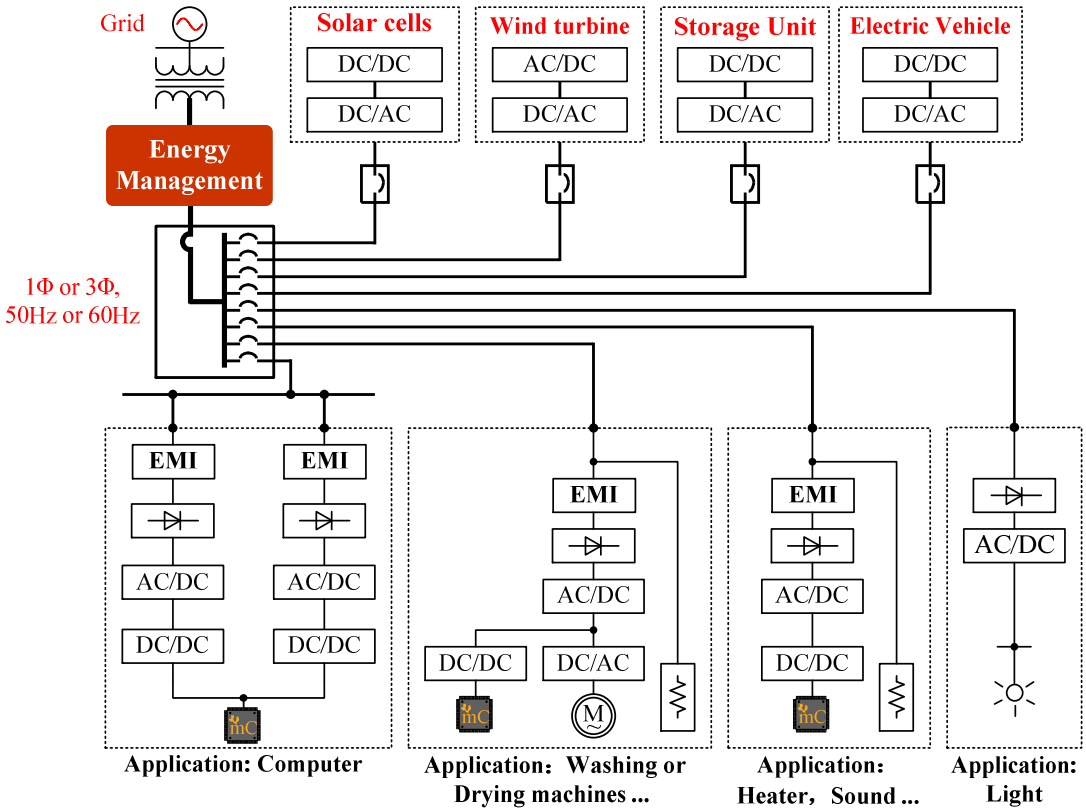


Figure 1.3: A typical AC DPS.

1.2. As shown, it is composed of a number of power converters, such as DC/DC converter, DC/AC inverter and AC/DC rectifier; and all the power converters are connected to the same DC voltage bus. Fig. 1.3 shows a typical AC DPS. In contrast to the DC DPS, the above power converters in AC DPS are all connected to the same AC voltage bus, instead of the DC voltage bus. It is worth pointing out that both DC DPS and AC DPS are two different structures of DPS, and it is hard to say which is better or worse (Xu and Cheng, 2011). However, the DC DPS is the only one studied in this thesis.

1.1.1 DC Distributed Power Systems (DC DPS)

As shown in Fig. 1.4, most DC DPS can be derived from combinations of four basic configurations (Luo, 2001), which are cascading, paralleling, split source and split load. A description of these architectures and their characteristics is given below.

1.1.1.1 Cascaded System

As shown in Fig. 1.4(a), the cascaded system includes at least two power conversion stages, and these power conversion stages are all interconnected by DC voltage bus. There are three advantages to the cascaded system. First, due to the application of the DC voltage bus, each power converter can be placed near its corresponding load to improve the regulation precision and dynamic performance of the load voltage. Second, the DC bus voltage can appropriately be raised to decrease the power loss caused by the line impedance. Finally, multiple power conversion stages are suitable for the wide input voltage application.

1.1.1.2 Paralleled System

As shown in Fig. 1.4(b), the paralleled system shares a common source and load of its sub-converters. It usually has three advantages. First, since the output power of each power converter is only one part of the system power, the thermal design of each power converter becomes easier. Second, although the paralleling structure increases the number of the power semiconductor devices and passive components, the electric and thermal stress of each power converter is greatly reduced. Finally, the redundant and modular design is very easy to be achieved by the paralleled system, which is also convenient for increasing the capacity of the system.

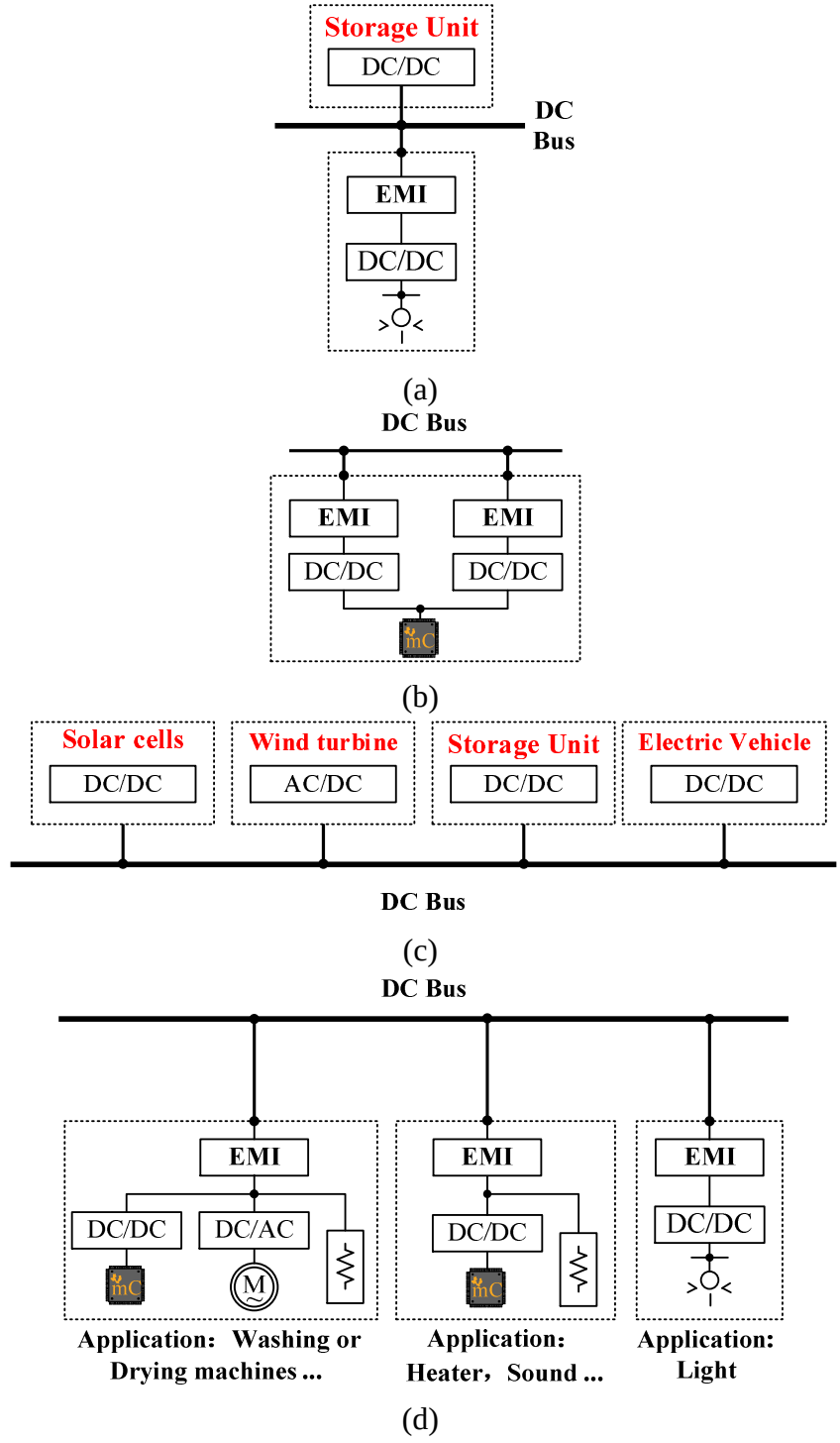


Figure 1.4: Basic structures of DC DPS: (a) cascading; (b) paralleling; (c) source splitting; (d) load splitting.

1.1.1.3 Source Splitting

Source splitting structure is shown in Fig. 1.4(c). It allows the use of separate power sources to supply a common load. This structure is very suitable for uninterrupted power supply (UPS), i.e., if the main power source is not working, backup energy can be connected to the DC voltage bus, supporting the system via the source splitting structure.

1.1.1.4 Load Splitting

As shown in Fig. 1.4(d), the load splitting structure is a configuration where separate power converters are utilised to feed different loads. This structure is suitable for a large-scale power supply system, such as a spacecraft (Lingjie et al., 2013), shipboard (McCoy and Amy, 2009) and DC micro-grid (Kwasinski and Onwuchekwa, 2006). These systems usually have many loads physically distributed over substantial distances. However, with the load splitting structure, separate power converters can be located in close proximity to each load to provide adequate regulation.

With the above four typical structures, DC DPS has become increasing popular, and its applications range from small, several hundred watt personal computers (Heath, 1991), through to kilo watt electronic vehicle systems (Kassakian, 2000), to mega watt micro-grid systems as well as other high-power applications found in smart grid systems (Lee et al., 2012).

1.1.2 The Instability Problem of Cascaded DC/DC Converter Systems

As discussed before, cascaded structure is a typical connection structure of DC DPS. Thanks to the advantages of the cascaded structure, the cascaded DC/DC converter system (also called as cascaded system) is becoming increasingly popular in various applications, such as space stations, shipboards, battery charging systems, and some other electrical devices comprising of two or more converters (Blaabjerg et al., 2005; Shamsi and Fahimi, 2013; Ovalle et al., 2015). A typical cascaded system is depicted in Fig. 1.5. Its upstream and downstream converters are called source and load converters, respectively. However, the closed-loop controlled load converter acts as a constant power load (CPL) and behaves as negative impedance in a small-signal analysis (Kwasinski and Onwuchekwa, 2011). As

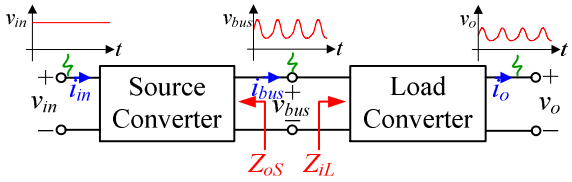


Figure 1.5: A typical cascaded DC/DC converter system.

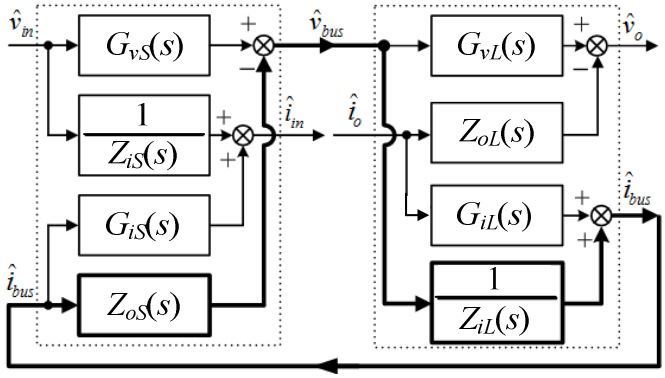


Figure 1.6: Two-port network model of the cascaded system.

a result, the stability of the cascaded system may be deteriorated by CPL, with the oscillating phenomenon then appearing in the cascaded system as shown in Fig. 1.5. This is the instability problem of the cascaded system (Zhang et al., 2013; Konig et al., 2014; Du et al., 2013). The fundamental concept of CPL and its negative resistor characteristics are explained in Appendix A.

1.1.2.1 Reason for the Instability Problem

In order to further reveal the instability reason of the cascaded system, the two-port network model of the cascaded system of Fig. 1.5 is depicted in Fig. 1.6. Here, v_{in} and i_{in} are the input voltage and current of the cascaded system, respectively. v_{bus} and i_{bus} are the bus voltage and current of the cascaded system, respectively, and v_o and i_o the output voltage and current of the cascaded system, respectively. In Fig. 1.6, $G_{vX}(s)$ is the closed loop input to output voltage transfer function of the source ($X = S$) or load converter ($X = L$); $Z_{iX}(s)$ is the closed loop input impedance of the source or load converter; $G_{iX}(s)$ is the closed loop load to input current transfer function of the source or load converter; and $Z_{oX}(s)$ is the closed loop output impedance of the source or load converter. According to Fig. 1.6, the four basic input-to-output transfer functions of the cascaded system can be derived as

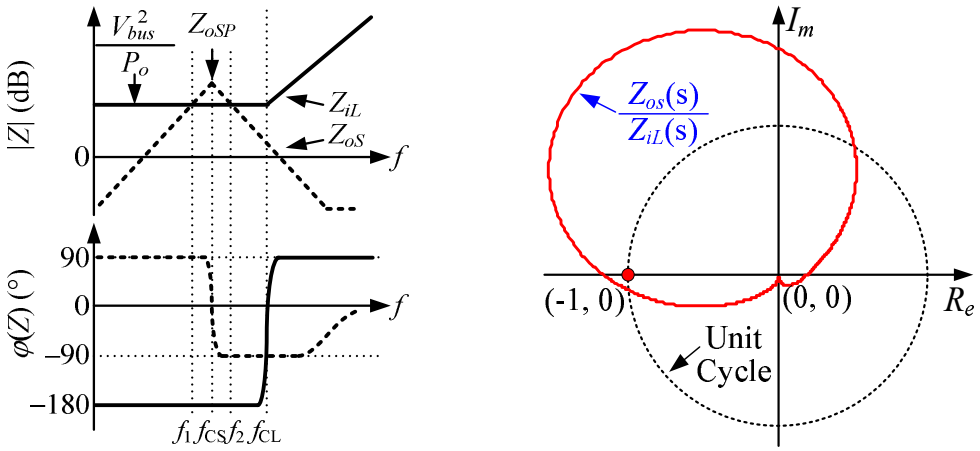


Figure 1.7: Bode plots and Nyquist plot of the typical unstable cascaded system: (a) Bode plots; (b) Nyquist plot.

follows:

$$\left.\frac{\hat{i}_{in}(s)}{\hat{v}_{in}(s)}\right|_{\hat{i}_o=0} = \frac{G_{vS}(s)G_{iS}(s)/Z_{iL}(s)}{1+T_m(s)} + \frac{1}{Z_{iS}(s)} \tag{1.1}$$

$$\left.\frac{\hat{v}_o(s)}{\hat{v}_{in}(s)}\right|_{\hat{i}_o=0} = \frac{G_{vS}(s)G_{vL}(s)}{1+T_m(s)} \tag{1.2}$$

$$\left.\frac{\hat{i}_{in}(s)}{\hat{i}_o(s)}\right|_{\hat{v}_{in}=0} = \frac{G_{iS}(s)G_{iL}(s)}{1+T_m(s)} \tag{1.3}$$

$$\left.\frac{\hat{v}_o(s)}{\hat{i}_o(s)}\right|_{\hat{v}_{in}=0} = -Z_{oL}(s) - \frac{G_{iL}(s)G_{vL}(s)Z_{oS}(s)}{1+T_m(s)} \tag{1.4}$$

where

$$T_m(s) = \frac{Z_{oS}(s)}{Z_{iL}(s)} \tag{1.5}$$

It is known that, if the source and load converters are stable individually, there will be no right half plane (RHP) poles in the numerator expressions of (1.1) $\sim$ (1.4). Therefore, at this moment, the stability of the cascaded system will be determined by $T_m(s)$, i.e., if $T_m(s)$ meets the Nyquist criteria, the cascaded system is stable, otherwise, the system is unstable. As a result, $T_m(s)$ is also called the minor loop gain of the cascaded system (Zhang et al., 2015).

As discussed before, the mismatch between $Z_{oS}(s)$ and $Z_{iL}(s)$ is the basic instability

reason of the cascaded system. Actually, this instability phenomenon can be predicted by Middlebrook criterion (Middlebrook, 1979; Turner et al., 2013; Feng et al., 2002), i.e., as shown the Bode plots in Fig. 1.7(a), if the amplitude of the source output impedance $|Z_{oS}|$ is intersected with the amplitude of the load input impedance $|Z_{iL}|$, and if the cut-off frequency f_{CS} of the source converter is lower than the cut-off frequency f_{CL} of the load converter, the cascaded system is unstable even if the converters can work well individually. In Fig. 1.7(b), the Nyquist plot of Fig. 1.7(a) is also depicted, as seen, the system loop gain $Z_{oS}(s)/Z_{iL}(s)$ indeed encircles $(-1,\ j0)$, which further proves that the cascaded system is unstable in this case.

Therefore, even though the subsystems can work well individually, the cascaded system may suffer instability problem due to the interaction between $Z_{oS}(s)$ and $Z_{iL}(s)$. It should be stressed that the above instability problem refers to the slow scale instability problem, and not the fast scale instability problem. This is because the analysis of the above instability problem is based on state-space average model which ignores the information around the switching frequency of power converters. It is also worth pointing out that all the instability problems and analysis refer only to slow scale instability cases in this thesis.

1.1.2.2 Characteristics of Source Output Impedance and Load Input Impedance

As discussed above, the instability problem of the cascaded system is caused by the intersection of the source output impedance and load input impedance. Therefore, the characteristics of the source output impedance and the load input impedance are reviewed in this sub-section. Some important conclusions have been drawn from the existing literature and summarised here (S. Abe and Ninomiya, 2006; Hankaniemi et al., 2005; Middlebrook and Cuk, 1976; Sable et al., 1991; Kazimierczuk and Starman, 1999; Abe et al., 2008; Thandi et al., 1999).

a) Output impedance of the source converter Z_{oS}: Z_{oS} is the output impedance of the source converter independent on its load. The characteristic of Z_{oS} is depicted by dotted lines, as shown in Fig. 1.7(a). Here, if the source converter is a switching-mode power supply, f_{CS} is the cut-off frequency of its voltage loop. If the source converter is a *LC* input filter, f_{CS} is the filter resonant frequency. It is obvious that, Z_{oS} is similar to the output impedance of a *LC* filter. If $f < f_{CS}$, Z_{oS} presents the characteristics of an inductance; and

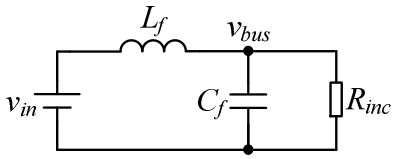


Figure 1.8: The equivalent circuit model of the cascaded system — A CPL cascaded with a *LC* input filter.

if $f > f_{CS}$, Z_{oS} presents the characteristic of the source output filter capacitor. It is worth pointing out that, for the source converter, its open-loop output impedance is higher than its closed-loop output impedance, and if the source converter is a *LC* input filter, its output impedance is higher than other type source output impedance (S. Abe and Ninomiya, 2006).

b) Input impedance of the load converter Z_{iL}: Generally, Z_{iL} refers specifically to the input impedance of the load converter operating in continuous current mode (CCM). The characteristic of Z_{iL} is depicted by solid lines, as shown in Fig. 1.7(a), where f_{CL} is the cut-off frequency of the voltage loop of the load converter. If $f < f_{CL}$, Z_{iL} behaves as a negative resistor with the value of $-\frac{V_{bus}^2}{P_o}$ (Hankaniemi et al., 2005), where V_{bus} is the intermediate bus voltage and P_o is the output power of the load converter; and if $f > f_{CL}$, Z_{iL} behaves as an inductor. It is worth mentioning that when $f < f_{CL}$, $|Z_{iL}|$ is inversely proportional to P_o (Middlebrook and Cuk, 1976; Sable et al., 1991; Kazimierczuk and Starman, 1999).

1.1.2.3 Physical Explanation of the System Instability Problem

According to sub-section 1.1.2.2, Z_{oS} is similar to the output impedance of a *LC* filter, and Z_{iL} behaves as a negative resistor if the load converter is controlled as a CPL. Therefore, from the impedance point of view, the cascaded system can be simplified into an equivalent *LC* input filter cascaded with a negative resistor. As shown in Fig. 1.8, L_f and C_f are the inductance and capacitor of the equivalent *LC* input filter, respectively. R_{inc} is the equivalent negative resistor.

As shown in Fig. 1.8, the transfer function of the system can be described by the well-known second-order function:

$$T(s) = \frac{v_{bus}}{v_{in}} = \frac{1}{s^2 L_f C_f + s\frac{L_f}{R_{inc}} + 1} \tag{1.6}$$

By introducing the resonant frequency ω_o and the damping factor ζ, (1.6) can be re-

arranged in a more familiar format:

$$T(s) = \frac{1}{\frac{s^2}{\omega_o^2} + 2\zeta\frac{s}{\omega_o} + 1} \tag{1.7}$$

where

$$\omega = \frac{1}{\sqrt{L_f C_f}} \tag{1.8}$$

$$\zeta = \frac{L_f \omega_o}{2R_{inc}} \tag{1.9}$$

If the input is excited with a unit-step function, the following Laplace equation can be obtained:

$$Y(s) = \frac{1}{\frac{s^2}{\omega_o^2} + 2\zeta\frac{s}{\omega_o} + 1}\frac{1}{s} \tag{1.10}$$

To obtain the response in the time domain, the inverse Laplace transform is utilised in (1.10). The result can be derived as:

$$Y(t) = 1 - \frac{e^{-\zeta\omega_o t}}{\sqrt{1-\zeta^2}} sin(\omega_d t + \theta) \qquad for\, \zeta < 1 \tag{1.11}$$

where

$$\omega_d = \omega_o\sqrt{1-\zeta^2} \tag{1.12}$$

$$\theta = cos^{-1}(\zeta) \tag{1.13}$$

It is known that, the poles affecting (1.7), denoted ρ_1 and ρ_2, represent the denominator roots for which $s^2 + 2\zeta\omega_o s + \omega_o^2 = 0$. Depending on ζ value, these poles affect the stability of the system described by (1.10) (Ozbay, 1999):

- $\zeta < 0$ — In that case, poles affecting (1.10) feature a positive real portion. Whatever the excitation level, the transient response diverges.

- $\zeta = 0$ — This particular case implies two pure imaginary poles $\rho_{1,2} = \pm j\omega_o$, making the system output permanently oscillating (no decay).

- $\zeta > 0$ — The two poles now have a real portion (ohmic losses), and the system exhibits different responses depending on whether $\zeta > 1$ (over-damping), $\zeta = 1$ (critical damping), or $0 < \zeta < 1$ for which we obtain a decaying oscillating response.

According to (1.9), if $R_{inc} < 0$, then $\zeta < 0$, and therefore the whole system will be unstable and its transient response diverge at any level of excitation. That is the physical explanation of why a CPL may become unstable with its *LC* input filter. In addition, it can also be seen that the -180^o phase resulted by the load negative resistor characteristic is the main reason for the instability of the cascaded system (Abe et al., 2008; Thandi et al., 1999).

1.1.2.4 The Worst Case of Instability Problem in Cascaded Systems

Due to the characteristics of Z_{oS}, when the source converter is a *LC* filter, its output impedance is higher than other types of source converters (S. Abe and Ninomiya, 2006). Due to the characteristics of Z_{iL}, when the load converter operates at a full load, it has the lowest negative resistor. According to (1.9) and (1.11), the lower negative resistor, the larger oscillation of the unstable cascaded system. Therefore, the worst case of instability problem of a cascaded system occurs at full load and when the source converter is a *LC* input filter (Zhang et al., 2013).

1.2 Literature Review

Since the instability problem is very likely to occur in a practical cascaded system, the question of how to solve the instability problem of the cascaded system has been receiving increasing attention. At present, many impedance-based stabilisation methods have been proposed for the cascaded system, and they can be divided into two types: hardware-based (Erickson and Maksimov, 2001; Cespedes et al., 2011; Marx et al., 2012; Abe et al., 2008; Zhang et al., 2013) and software-based (Rahimi and Emadi, 2009; Karppanen et al., 2007; Wu and Lu, 2015; Li et al., 2015; Liu et al., 2007a; Wang et al., 2005). For hardware-based methods, the passive components, such as resistors, capacitors, inductors, and converters are utilised to change the source output impedance or load input impedance to stabilise the cascaded system. For software-based methods, advanced control methods are utilised to modify the source output impedance or load input impedance to ensure the stability of the cascaded system.

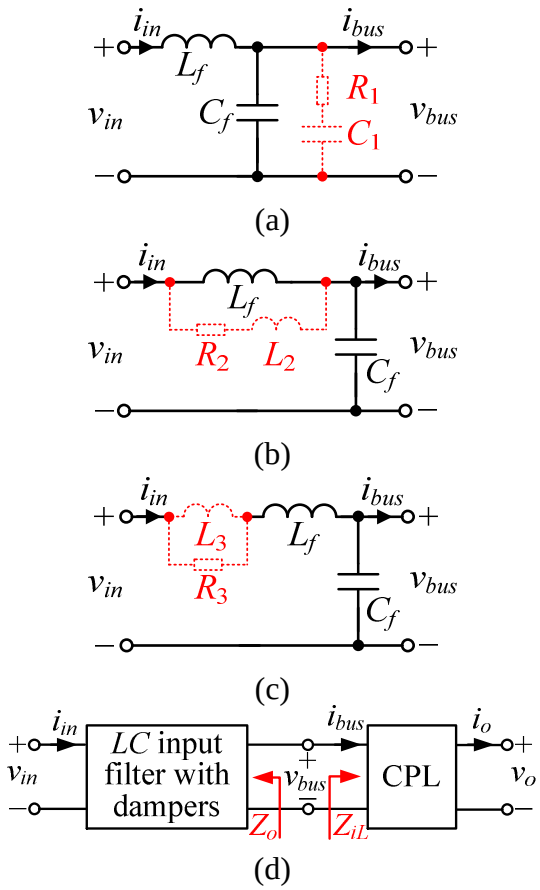


Figure 1.9: Typical dampers and their application: (a) *RC* parallel damper; (b) *RL* parallel damper; (c) *RL* series damper; (d) Application.

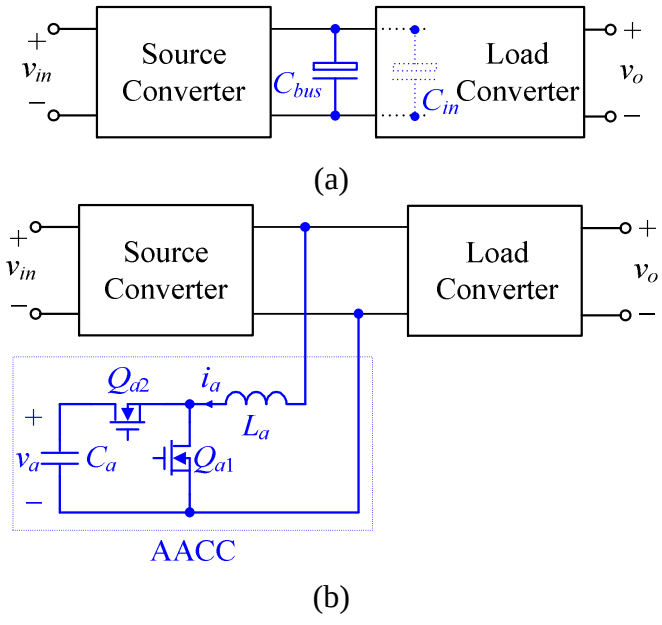


Figure 1.10: Stabilise the cascaded system by adding bus capacitor or adaptive active capacitor converter: (a) adding bus capacitor; (b) adding adaptive active capactior converter.

1.2.1 Hardware-Based Stabilisation Methods

Since the reduced system damping caused by the CPL is the root cause of the instability problem in cascaded systems (Middlebrook, 1979), the most intuitive hardware-based method is to increase the system damping by using dampers (Erickson and Maksimov, 2001; Cespedes et al., 2011; Marx et al., 2012). Three typical dampers are depicted in Fig. 1.9, where the elements in the dashed line are used for damping. Due to the structure and position of the damper, the three dampers are called the *RC* parallel damper (Fig. 1.9(a)), the *RL* parallel damper (Fig. 1.9(b)) and the *RL* series damper (Fig. 1.9(c)), respectively. In the system shown in Fig. 1.9(d) with these dampers, the peak of the output impedance of the *LC* input filter can be damped, and a total separation between $|Z_o|$ and $|Z_{iL}|$ ensured to stabilise the whole system.

It is worth pointing out that if the input filter is a π, *LCL* or other high order filters, the above dampers may be not useful. This is because the characteristic of the output impedance of these high order filters is more complex than the *LC* filter. For instance, the output impedance of the *LC* filter only contains one resonant peak, but the output impedance of both π and *LCL* filters contain two resonant peaks. However, the above dampers cannot simultaneously damp two resonant peaks. It is also worth pointing out that, the input filter only refers to the *LC* filter and the high order filters will not be discussed in this thesis. In addition, if the source stage is a closed-loop converter with *LC* output filter, the above dampers are not suitable either. Though the above dampers can dampen the output impedance of the closed-loop converter, they also increase the order of the converter and may make the converter itself unstable. As a result, the above dampers are specifically proposed for the application whose source stage is a *LC* input filter.

However, in some cascaded systems, the source converter is a switching power converter, and not a *LC* input filter. For instance, in electric vehicle on-board DC power systems, the feeder of the CPL is usually another power converter. It is clear that the passive dampers in Fig. 1.9 may not be suitable for such cascaded systems. Therefore, another two hardware-based stabilisation methods are proposed as shown in Fig. 1.10 (Abe et al., 2008; Zhang et al., 2013).

In Fig. 1.10(a), the capacitance of the bus capacitor C_{bus} (Abe et al., 2008; 2006) or the original load input capacitor C_{in} (An and Lu, 2016) is increased. As a result, both the source converter and the load converter are entirely decoupled by the C_{bus} or C_{in}. Thus, system stability is also ensured. However, this stabilisation method has some unavoidable drawbacks: 1) in order to stabilise the cascaded system, a large capacitance value of the bus capacitor is required and the electrolytic capacitor has to be utilised. However, the electrolytic capacitor also means worse reliability for the cascaded system (Ma et al., 2013); 2) a larger C_{bus} or C_{in} results in poor dynamic performance of the cascaded system (Thandi et al., 1999); and 3) a larger C_{bus} or C_{in} reduces the system power density (Cao et al., 2015).

In order to overcome the drawbacks of the stabilisation method in Fig. 1.10(a), an auxiliary DC/DC converter, known as an adaptive active capacitor converter (AACC), is proposed to mimic the function of C_{bus} (Zhang et al., 2013). Fig. 1.10(b) presents a typical structure of an AACC, which contains a capacitor, an inductor and two switchers. It is worth mentioning that the capacitor in the AACC is very small and can be realised by a film capacitor. Therefore, this AACC not only has the same stabilisation function as C_{bus}, but also does not deteriorate the reliability of the cascaded system. In addition, the AACC ensures the dynamic performance of the cascaded system via an advanced control method. However, the weak side of the AACC stabilisation method is that an extra DC/DC converter is required resulting in additional cost and power losses. Therefore, as with the larger C_{bus} or C_{in}, the AACC also reduces the power density of the system.

1.2.2 Software-Based Stabilisation Methods

As hardware-based stabilisation methods can lead to significant power loss, software-based methods based on advanced control of the source converter (Rahimi and Emadi, 2009; Karppanen et al., 2007; Wu and Lu, 2015; Li et al., 2015) or the load converter (Liu et al., 2007a; Wang et al., 2005) are proposed.

Fig. 1.11 shows the existing software-based stabilization methods for the source converter (Rahimi and Emadi, 2009; Karppanen et al., 2007; Wu and Lu, 2015; Li et al., 2015). In Fig. 1.11(a), an inductor current inner loop is introduced to the source converter to add a virtual resistor in a series with the filter inductor (Rahimi and Emadi, 2009; Karppanen et al., 2007). With this virtual resistor, the resonant peak of the source output impedance

can be damped, and hence the stability of the cascaded system is ensured. In Fig. 1.11(b), the droop control is utilised by the source converter (Wu and Lu, 2015). As a result, a large virtual resistor is added in the series, with the output of the source converter to damp the oscillation of the cascaded system. In Fig. 1.11(c), the output voltage differential inner loop is used by the source converter to add a virtual resistor in parallel with its output (Li et al., 2015). With this output voltage differential inner loop, the output impedance of the source converter can be greatly reduced so that the system instability problem can be solved.

Fig. 1.12 presents the existing software-based stabilisation methods for the load converter (Liu et al., 2007a; Wang et al., 2005). In Fig. 1.12(a), a stabilising power is injected into the load converter (Liu et al., 2007a). With this injected power, a virtual capacitor or resistor is equivalently added in parallel with the input port of the load converter to remove its CPL characteristic. In Fig. 1.12(b), the regulation signal maps of the source converter is developed and sent to the control block of the load converter to shape the load input impedance (Wang et al., 2005).

1.3 Motivation and Objective

As discussed above, prior to this research, many impedance-based solutions have been proposed to stabilise the cascaded system, and they can be classified into two types: hardware-based (Erickson and Maksimov, 2001; Cespedes et al., 2011; Zhang et al., 2013) and software-based (Rahimi and Emadi, 2009; Karppanen et al., 2007; Wu and Lu, 2015; Li et al., 2015; Liu et al., 2007a; Wang et al., 2005). However, though these stabilisation methods are able to stabilise the cascaded system, they share three drawbacks.

Firstly, most software-based stabilisation methods focus on changing the source output impedance, whilst the software-based stabilisation methods of regulating the load input impedance are rarely reported. However, load software-based stabilisation methods are necessary in practice. For instance, if the source converter is a *LC* input filter, existing source software-based stabilisation methods cannot control the *LC* input filter and cannot stabilise the cascaded system. Though passive dampers can be utilised at this moment, doing so brings significant power loss to the cascaded system. Therefore, of the existing

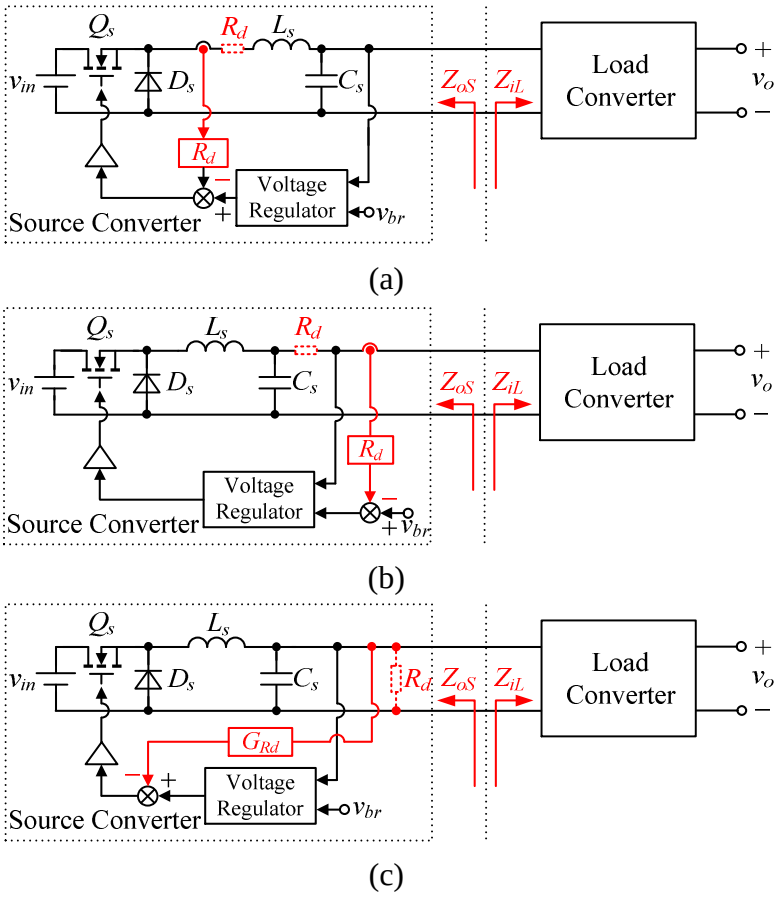


Figure 1.11: Software-based stabilisation methods for source converters: (a) adding virtual resistor in series with the filter inductor; (b) adding virtual resistor in series with the source output; (c) adding virtual resistor in parallel with the source output.

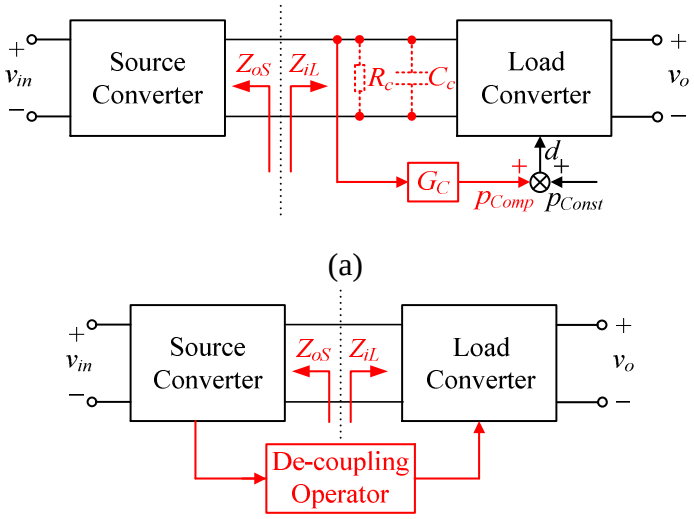


Figure 1.12: Software-based stabilisation methods for load converters: (a) adding virtual resistor or capacitor in parallel with the load input; (b) sending the regulation signal from source converter to load converter.

stabilisation methods, only the method in (Liu et al., 2007a) is suitable in this case. It is worth pointing out that though the method in (Wang et al., 2005) is also a load stabilisation software-based method, it requires the regulation signal from the source control block. Thus, this method is also unachievable when the source converter is a *LC* input filter.

Secondly, most of the existing stabilisation methods need the information of both the regulated converter and the other converters. For instance, the existing load stabilisation methods need to shape the load input impedance according to the characteristics of the source output impedance. Similarly, the existing source stabilisation methods need to shape the source output impedance according to the characteristics of the load input impedance. In other words, when the source or load converter changes, the existing load or source stabilisation method must be re-designed, which increases the development cycles and cost of the whole cascaded system. In (Zhang et al., 2013), the authors studied this problem and proposed that AACC be used to stabilise the cascaded system without requiring any information of the source or load converter. However, AACC reduces the power density of the cascaded system and is unacceptable for weight-limited or/and volume-limited systems, such as aircraft and hybrid electrical vehicles power supply systems (Wen et al., 2012; Wang et al., 2011).

Thirdly, all the existing stabilisation methods are focused on how to shape the source output impedance or load input impedance, but ignore their impact on the original performance of the cascaded system. However, stabilising the cascaded system can impede keeping the original performance of the cascaded system. For instance, if the load converter wants to achieve a good dynamic performance, its input impedance should be controlled as a negative resistor from small signal analysis, but this negative resistor characteristic is bad news for the stability of a cascaded system. Another example is that of the passive dampers: though the existing *RC* or *RL* dampers can damp the output impedance of the source converter and stabilise the cascaded system, they also bring slower dynamic performance and reduce EMI ability of the source converter.

Therefore, the objective of this thesis is to propose a family of software-based stabilisation methods to overcome the above drawbacks. It will do so in the following ways:

a) To overcome the first drawback, this thesis proposes a family of load software-based stabilisation methods to shape the load input impedance only in a specific frequency range.

As a result, the proposed load software-based stabilisation methods would not only stabilise the cascaded system, but also keep most of the performance of the original load converter.

b) To overcome the second drawback, this thesis introduces the adaptive function to the proposed load software-based stabilisation methods. With the adaptive stabilisation methods, the load converter would stably connect to different source converters without changing its internal structure.

c) To overcome the third drawback, this thesis investigates the impact of the existing stabilisation methods via two-port network analysis, and proposes two software-based methods to stabilise the cascaded system while improving the system performance.

However, it should be stressed that all the proposed methods are devoted to solving the instability problem of the cascaded system formed by just one source converter and one load converter.

1.4 Outline of the Thesis

There are nine chapters in this thesis. Chapter 1 is the introduction, and Chapters 2 to 8 present the proposed stabilisation methods. Chapter 9 concludes the thesis and makes suggestions for further work. The thesis is organised as follows.

In Chapter 2, a parallel-virtual-impedance (PVI) control strategy is proposed to solve the instability problem of the cascaded system. It connects a virtual impedance in parallel with the input port of the load converter so that the magnitude or phase of the load input impedance is modified in a very small range of frequency. As a result, with the PVI control strategy, the cascaded system can be stabilised with minimised load compromise. The requirements, design considerations and experimental verification of the PVI control strategy are presented in this chapter.

Since the PVI control strategy can add a virtual impedance in parallel with the load converter to stabilise the cascaded system with minimised load compromise, it seems natural that a corresponding virtual impedance can also be added in series with the load converter to realise the same function. Therefore, a series-virtual-impedance (SVI) control strategy is proposed in Chapter 3, which can also be treated as the development and complement of the PVI control strategy. The concept, derivation, control realisation and experimental

verification of the SVI control strategy are presented in Chapter 3.

Though a family of load stabilisation methods, such as PVI and SVI control strategies, are proposed in Chapters 2 and 3 respectively, they require detailed information on the source converters. As a result, if the source converter is changed, the PVI or SVI control strategy must be re-designed for the load converter. It is obvious that the characteristics of the PVI and SVI control strategies increase the development cycles and cost of the cascaded system. In order to solve this problem, the adaptive function is introduced to the PVI control strategy to generate another new control strategy — the adaptive-PVI (APVI) control strategy in Chapter 4. With the APVI control strategy, the load converter can be stably connected to different source converters without changing its internal structure. The concept, realisation and experimental verification of the APVI control strategy are presented in Chapter 4.

In Chapter 5, it is shown that the cascaded system can be stabilised via amplitude compensation (SAC) or phase compensation (SPC) for the input impedance of the load converter. Both PVI and SVI control strategies are essentially two realisation methods for SAC and SPC. Therefore, the SAC and SPC are firstly analysed and compared in Chapter 5. It is shown here that, though both SAC and SPC can stabilise the cascaded system, the system utilising the SAC is unconditionally stable, but conditionally stable when utilizing the SPC, i.e., the cascaded system with SAC is more stable than that with SPC. After this, the comparison is also carried out for the PVI and SVI control strategies. The results shows that the PVI control strategy has inevitable limitations when realising the SAC during the whole load and input voltage range of the load converter, though the SVI control strategy does not have limitations. Therefore, compared to the PVI control strategy, the SVI control strategy is more suitable for the SAC. Furthermore, the adaptive concept proposed in Chapter 4 is also introduced here to the SVI control strategy to generate the adaptive-SVI (ASVI) control strategy. Similar to the APVI control strategy, the ASVI control strategy stably connects the load converter to different source converters without changing its internal structure. Moreover, the ASVI control strategy can make the cascaded system more stable than the APVI control strategy. The concept, control block, realisation and experimental verification of the ASVI control strategy are also presented in Chapter 5.

The ASVI control strategy utilises a proportional-integral (PI) controller to find the

centre frequency of the ASVI. However, this PI controller may miss the right frequency with excessive proportional or integral coefficients and lead to the failure of the ASVI control strategy. Although this potential problem may not arise with small proportional and integral coefficients, it is a potential problem for the ASVI control strategy. To make the ASVI control strategy more reliable, this problem is studied in Chapter 6. The relationship between the bus voltage ripple and the centre frequency of the ASVI is firstly analysed. It is found that the relationship curve behaves like an inverted power-voltage curve of a PV cell. Therefore, a perturb and observe (P&O) algorithm based minimum-ripple-point-tracking (MRPT) controller is proposed to find the centre frequency of ASVI instead of the original PI controller. With the MRPT controller, the ASVI control strategy can find the centre frequency of the ASVI without the above problem. Furthermore, in order to find the centre frequency of ASVI quickly, the sinusoidal-tracking-algorithm (STA) is further introduced into the MRPT controller to improve its processing speed. Both the potential problem of the original ASVI control strategy with the PI controller and the effectiveness of the improved ASVI control strategy with the proposed MRPT controller are discussed and experimentally verified in Chapter 6.

The analysis in Chapters 2 to 6 indicates that the ASVI control strategy is the best load stabilisation method for the cascaded system. The ASVI control strategy can not only make the cascaded system become an unconditional stable system via shaping the load input impedance, but also changes the load input impedance only in a very small frequency range to minimise its impact on the original load converter.

However, though the ASVI control strategy has already greatly reduced its impact on the load converter, its rest impact is negative. In order to solve this problem, Chapter 7 moves the ASVI from the load side to the source side via a proposed source-side SVI (SSVI) control strategy for the source converter. The proposed SSVI control strategy not only has the same stabilisation function with the ASVI control strategy, but also improves the performance of the source converter. In addition, since the SSVI control strategy is realised by changing the control block of the source converter, the performance of the load converter is not affected. Therefore, the SSVI control strategy can be treated as a supplement to, and improvement on, the ASVI control strategy. Additionally, due to the method of realisation, the SSVI control strategy also can be divided into the source stabilisation

methods of the cascaded system. It is also worth pointing out that since the SSVI control strategy stabilises the system by reducing the source output impedance, it is also suitable for the DPS with multiple upstream converters and one downstream converter.

As discussed above, the *LC* filter at the input of a DC/DC converter may cause instability when the converter is controlled as a CPL and one of the effective solutions is to reduce the output impedance of the *LC* input filter by different stabilisation dampers. In Chapter 8, the impact of these dampers on the *LC* filter is analysed via two-port network analysis, and it is found that the existing dampers all degrade the performance of the original *LC* input filter to some extent. In order to overcome this issue, an *RLC* damper is proposed to stabilise the whole system while improving the performance of the *LC* input filter. In addition, this *RLC* damper is also designed to achieve real robustness against the parameter variations of the *LC* input filter. Furthermore, in order to avoid the power loss when physically implementing the damper, a control strategy for the CPL is proposed to implement the *RLC* damper as a virtual *RLC* (*VRLC*) damper. The actual effectiveness of the *VRLC* damper and its impact on the CPL are fully evaluated via two-port network analysis, and experimentally verified in Chapter 8.

Finally, Chapter 9 concludes the thesis and makes recommendations for future work.

1.5 Major Contributions

The major contribution of this research is to propose a family of impedance-control-based methods to stabilise the cascaded system without the drawbacks of the existing solutions. It achieves this primarily in six ways:

1. A set of virtual-impedance-based control strategies are proposed in this thesis – PVI (Chapter 2) and SVI (Chapter 3). The PVI and SVI control strategies connect a virtual impedance in parallel or series with the input impedance of the load converter so that the magnitude or phase of the load input impedance is modified in a small frequency range to ensure the stability of the whole system. Since PVI and SVI control strategies only modify the load input impedance in a very small frequency range, they can stabilise the cascaded system with minimised load compromise. Therefore, the PVI and SVI control strategies can not only be treated as the development and com-

plement of the load stabilisation methods, but also as good solutions for overcoming the contradiction between the stability and performance of the cascaded system. In addition, it is worthy of mention that, since both PVI and SVI control strategies realise the impedance decoupling of the source and load converters, it could not only solve the instability problem of the cascaded system but also have the benefit of removing the input capacitor of the load converter whose original main function is impedance decoupling.

2. Adaptive concept is introduced to stabilisation methods to generate two novel software-based stabilisation methods: APVI (Chapter 4) and ASVI (Chapter 5) control strategies. With the APVI and ASVI control strategies, the load converter can be stably connected to different source converters without changing its internal structure. In contrast to the existing stabilisation methods, the APVI and ASVI control strategies avoid the redesign of the load converter, and hence save the cost for the cascaded system.

3. The SAC and SPC methods are compared in Chapter 5. It is known that both SAC and SPC are two popular load stabilisation methods for the cascaded system. However, prior to this thesis, there was no clear conclusion on which was better or worse. This thesis, however, finds that though both SAC and SPC can stabilise the cascaded system, the system utilising the SAC is unconditionally stable but conditionally stable when utilising the SPC, i.e., the cascaded system with SAC is more stable than that with SPC.

4. The PVI and SVI control strategies are compared in Chapter 5. The results indicate that the PVI control strategy has inevitable limitations when realising the SAC during the whole load and input voltage range of the load converter, whilst the SVI control strategy does not have limitations. Therefore, the SVI control strategy is more suitable for the SAC than the PVI control strategy.

5. The potential problem of the ASVI control strategy is solved in Chapter 6. Though the ASVI control strategy is so far the best load stabilisation method, it is not perfect. Since the ASVI control strategy utilises a PI controller to find the centre frequency of the ASVI, the PI controller may miss the right frequency with excessive proportional or integral coefficients and cause the failure of the ASVI control strategy. Although

this problem will not necessarily arise with small proportional and integral coefficients, it is potentially an issue for the ASVI control strategy. To make the ASVI control strategy more reliable, a MRPT controller is proposed to replace the original PI controller. With the MRPT controller, the ASVI control strategy could find the centre frequency of the ASVI without the aforementioned problem arising. In addition, the MRPT controller is further improved by STA to help it quickly find the centre frequency of ASVI.

6. SSVI control strategy is proposed to stabilise the cascaded system while improving the performance of the source converter (Chapter 7). Though the existing stabilisation methods can stabilise the cascaded system, they all degrade the performance of the original cascaded system to some extent. Even the proposed PVI and SVI control strategies only keep most of the performance of the load converter: they cannot improve it. However, the SSVI control strategy solves this problem by not only making the cascaded system stable, but also making the source converter work better. In addition, it is worth pointing out that since the SSVI control strategy stabilises the system by reducing the source output impedance, it is not only suitable for the cascaded system with one upstream converter and one downstream converter, but also for the distributed power system with multiple upstream converters and one downstream converter.

7. *VRLC* damper is proposed to stabilise the cascaded system while improving the performance of the *LC* input filter (Chapter 8). Though the existing dampers can solve the instability problem between the CPL and its *LC* input filter, they degrade the performance of the original *LC* input filter to some extent. In order to overcome this drawback, a *VRLC* damper is proposed. This can not only stabilise the cascaded system, but also improve the performance of the *LC* input filter and improve the system efficiency compared to the existing dampers.

1.6 List of Publications

1. Xin Zhang, Qing-Chang Zhong, "Improved Adaptive-Series-Virtual-Impedance Control Incorporating Minimum Ripple Point Tracking for Load Converters in DC Sys-

tems", IEEE Transactions on Power Electronics, Volume: 31, Issue: 12, 8088-8095, 2016

2. Xin Zhang, Qing-Chang Zhong, Wen-Long Ming, “A Virtual *RLC* Damper to Stabilize DC/DC Converters Having an *LC* Input Filter while Improving the Filter Performance", IEEE Transactions on Power Electronics, Volume: 31, Issue: 12, 8017-8023, 2016.

3. Xin Zhang , Qing-Chang Zhong, Wen-Long Ming, "Stabilization of a Cascaded DC Converter System via Adding a Virtual Adaptive Parallel Impedance to the Input of the Load Converter", IEEE Transactions on Power Electronics, Volume: 31, Issue: 3, 1826 – 1832, 2016.

4. Xin Zhang, Qing-Chang Zhong, Wen-Long Ming, “Stabilization of Cascaded DC/DC Converters via Adaptive Series-Virtual-Impedance Control of the Load Converter", IEEE Transactions on Power Electronics, Volume: 31, Issue: 9, 6057 - 6063, 2016.

5. Wen-Long Ming, Qing-Chang Zhong and Xin Zhang, “A single-phase four-switch rectifier with significantly reduced capacitance,” IEEE Transactions on Power Electronics, Volume: 31, Issue: 2, 1618-1632, 2016.

6. Xin Zhang ,Qing-Chang Zhong, Wen-Long Ming,"Adaptive series-virtual-impedance control strategy for the load converter to improve the stability of the cascaded system", IEEE PEDG, Vancouver, Canada, 27-30 June 2016.

7. Xin Zhang ,Qing-Chang Zhong, Wen-Long Ming,"Source-side Series-virtual-impedance Control Strategy to Stabilize the Cascaded System with Improved Performance", IEEE ECCE, Milwaukee, Wisconsin, USA, 18-22 September 2016.

8. Xin Zhang ,Qing-Chang Zhong, Wen-Long Ming,"A Novel Stabilization Method of DC/DC Converters Having an *LC* Input Filter via Utilizating a Virtual *RLC* Damper", IEEE ECCE, Milwaukee, Wisconsin, USA, 18-22 September 2016.

9. Xin Zhang , Xin-Bo Ruan, Qing-Chang Zhong, "Improving the Stability of Cascaded DC/DC Converter Systems via Shaping the Input Impedance of the Load Converter

With a Parallel or Series Virtual Impedance", IEEE Transactions on Industrial Electronics, Volume:62 Issue:12, Pages: 7499 – 7512, 2015.

10. Xin Zhang ,Qing-Chang Zhong, Wen-Long Ming, Xin-Bo Ruan,"Stabilization of a cascaded DC system via adding a virtual impedance in series with the load converter", IEEE PEDG 2015, Pages: 677-683.

11. Xin Zhang ,Qing-Chang Zhong, Wen-Long Ming, Xin-Bo Ruan,"Stabilization of a cascaded DC system via adding a virtual impedance in parallel with the load converter", IEEE PEDG 2015, Pages: 335-341.

12. Xin Zhang ,Qing-Chang Zhong, Wen-Long Ming, S. Gadelovits, " Impedance-based local stability criterion for standalone photovoltaic-battery hybrid system", IEEE PEDG 2015, Pages: 717-723.

13. Xin Zhang ,Qing-Chang Zhong, Wen-Long Ming,"Fast scale instability problem of cascaded buck conversion system and its phase-shifted-carrier solution", IEEE ECCE 2015, Pages: 2684 - 2689.

Chapter 2

Parallel-Virtual-Impedance (PVI) Control for Load Converters

As discussed in Chapter 1, a load stabilisation method is necessary for the cascaded system because the source output impedance cannot be changed by control method in some special applications. For instance, if the source converter is a *LC* input filter, the existing software-based source stabilisation method cannot modify its output impedance and cannot stabilise the cascaded system either. Therefore, this chapter proposes a parallel-virtual-impedance (PVI) control strategy, which connects a virtual impedance in parallel with the input port of the load converter so that the magnitude or phase of the load input impedance is modified in a small frequency range, thus solving the instability problem of the cascaded system. As a result, even if the source converter is a *LC* input filter, the cascaded system still can be stabilised with the minimised load compromise via the proposed PVI control strategy. The requirements and design consideration of the PVI control strategy are discussed in this chapter.

The rest of this chapter is organised as follows. In Section 2.1, the basic idea of the load shaping method is discussed, and the concept, derivation and realisation of the PVI control strategy are presented. Two design examples of the PVI control strategy are then given in Section 2.2. Based on the design examples, two experimental/simulation cascaded systems are fabricated to verify the effectiveness of the PVI control strategy in Sections 2.3 and 2.4, respectively; and in Section 2.5, this Chapter is summarised.

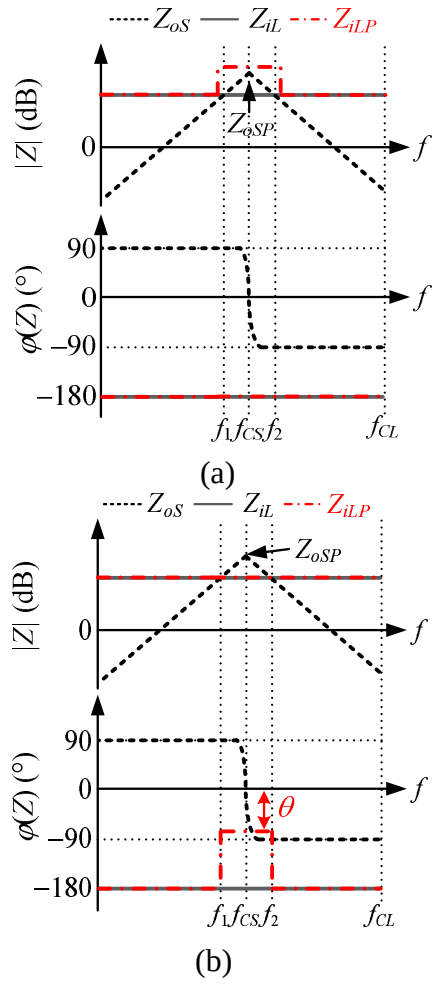


Figure 2.1: Basic idea of load shaping methods: (a) only increasing $|Z_{iL}|$ at $[f_1,\ f_2]$ to make a total separation between $|Z_{oS}|$ and $|Z_{iL}|$; (b) only changing $\varphi(Z_{iL})$ at $[f_1,\ f_2]$ to ensure $|\varphi(Z_{oS}) - \varphi(Z_{iL})| < 180^0$ at $[f_1,\ f_2]$.

2.1 PVI Control Strategy

2.1.1 Basic Idea of Load Shaping Methods

It is understood that if the designer wants to make the cascaded system stable while keeping most of the dynamic performance of the original load converter, the best method is to change Z_{iL} only in the vicinity of the intersection frequencies of $|Z_{oS}|$ and $|Z_{iL}|$. Here, Z_{oS} is the source output impedance, and Z_{iL} is the load input impedance. As shown in Fig. 2.1, f_1 and f_2 are the intersection frequencies of $|Z_{oS}|$ and $|Z_{iL}|$.

Fig. 2.1 illustrates that there are two better ways to regulate Z_{iL}: (a) only increasing $|Z_{iL}|$ between f_1 and f_2 to make a total separation of $|Z_{oS}|$ and $|Z_{iL}|$ (See Fig. 2.1(a));

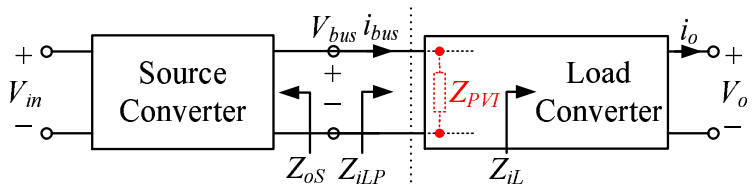


Figure 2.2: A cascaded system with parallel virtual impedance.

and (b) only increasing $\varphi(Z_{iL})$ at $[f_1,\ f_2]$ to ensure $|\varphi(Z_{oS}) - \varphi(Z_{iL})| < 180^0$ during $[f_1,\ f_2]$ ((See Fig. 2.1(b))). In Fig. 2.1, Z_{iLP} is the input impedance of the load converter with the latter proposed PVI control strategy.

2.1.2 Expression of the Parallel-Virtual-Impedance $Z_{PVI}(s)$

In fact, the load shaping idea in Section 2.1.1 can be realised by adding a virtual impedance $Z_{PVI}(s)$ in parallel with the load input port. As shown in Fig. 2.2, after adding $Z_{PVI}(s)$, the shaped load input impedance $Z_{iLP}(s)$ can be expressed as

$$Z_{iLP}(s) = Z_{iL}(s) \parallel Z_{PVI}(s) = \frac{Z_{iL}(s) \cdot Z_{PVI}(s)}{Z_{iL}(s) + Z_{PVI}(s)} \tag{2.1}$$

where $Z_{iL}(s)$ is the original input impedance of the load converter and if $f < f_{CL}$ its expression is $-V_{bus}^2/P_o$. Here, V_{bus} and P_o are the input voltage and output power of the load converter, respectively.

a) According to Fig. 2.1(a), if a total separation between $|Z_{oS}|$ and $|Z_{iLP}|$ is needed and the minimised change of Z_{iL} is also required, Z_{iLP} should satisfy:

$$If\{f \in [f_1,\ f_2]\} \quad \rightarrow \quad |Z_{iLP}| > Z_{oSP} \tag{2.2}$$

$$If\{f \notin [f_1,\ f_2]\} \quad \rightarrow \quad Z_{iLP} = Z_{iL} \tag{2.3}$$

where Z_{oSP} is the peak value of $|Z_{oS}|$.

According to (2.2) and (2.3), Z_{iLP} can be further expressed as

$$Z_{iLP} \quad = \quad \begin{cases} -|Z_{iL1}| & f \in [f_1,\ f_2] \\ Z_{iL} & f \notin [f_1,\ f_2] \end{cases} \tag{2.4}$$

where $|Z_{iL1}| > Z_{oSP}$ is the amplitude of Z_{iLP} during $[f_1,\ f_2]$.

According to (2.1) and (2.4), in order to ensure $|Z_{iL}|$ become $|Z_{iLP}|$ as shown in Fig. 2.1(a) successfully, Z_{PVI} can be selected as

$$\begin{aligned} Z_{PVI} &= \frac{Z_{iL}Z_{iLP}}{Z_{iL}-Z_{iLP}} = \begin{cases} \frac{\left(V_{bus}^2/P_o\right)|Z_{iL1}|}{\left(-V_{bus}^2/P_o\right)-(-|Z_{iL1}|)} & f \in [f_1,\ f_2] \\ +\infty & f \notin [f_1,\ f_2] \end{cases} \\ &= \begin{cases} -\frac{V_{bus}^2|Z_{iL1}|}{V_{bus}^2-|Z_{iL1}|P_o} & f \in [f_1,\ f_2] \\ +\infty & f \notin [f_1,\ f_2] \end{cases} \end{aligned} \tag{2.5}$$

b) Similarly, according to Fig. 2.1(b), if $|\varphi(Z_{oS})-\varphi(Z_{iLP})| < 180^0$ is needed to be ensured within $[f_1,\ f_2]$ and the minimised change of Z_{iL} is also required, Z_{iLP} should satisfy:

$$If\{f \in [f_1,\ f_2]\} \rightarrow |\theta| < 90^0 \tag{2.6}$$

$$If\{f \notin [f_1,\ f_2]\} \rightarrow \varphi(Z_{iLP}) = \varphi(Z_{iL}) \tag{2.7}$$

where θ is the phase of Z_{iLP} during $[f_1,\ f_2]$.

According to (2.6) and (2.7), Z_{iLP} can be further expressed as

$$Z_{iLP} = \begin{cases} \left(V_{bus}^2/P_o\right)e^{j\theta} & f \in [f_1,\ f_2] \\ Z_{iL} & f \notin [f_1,\ f_2] \end{cases} \tag{2.8}$$

According to (2.1) and (2.8), in order to ensure $|Z_{iL}|$ become $|Z_{iLP}|$ as shown in Fig. 2.1(b) successfully, Z_{PVI} can be selected as

$$\begin{aligned} Z_{PVI} &= \frac{Z_{iL}Z_{iLP}}{Z_{iL}-Z_{iLP}} = \begin{cases} \frac{-\left(V_{bus}^2/P_o\right)\left[\left(V_{bus}^2/P_o\right)e^{j\theta}\right]}{\left(-V_{bus}^2/P_o\right)-\left[\left(V_{bus}^2/P_o\right)e^{j\theta}\right]} & f \in [f_1,\ f_2] \\ +\infty & f \notin [f_1,\ f_2] \end{cases} \\ &= \begin{cases} \frac{V_{bus}^2}{P_o}\cdot\frac{e^{j\theta}}{1+e^{j\theta}} & f \in [f_1,\ f_2] \\ +\infty & f \notin [f_1,\ f_2] \end{cases} \end{aligned} \tag{2.9}$$

In summary, if the Z_{PVI}, which is expressed by (2.5), is added in parallel with the load input impedance, a total separation between $|Z_{oS}|$ and $|Z_{iLP}|$, as shown in Fig. 2.1(a), can be realised. If the Z_{PVI}, as expressed at (2.9), is added in parallel with the load input impedance, $|\varphi(Z_{oS})-\varphi(Z_{iLP})| < 180^0$ within $[f_1,\ f_2]$, as shown in Fig. 2.1(b), can be

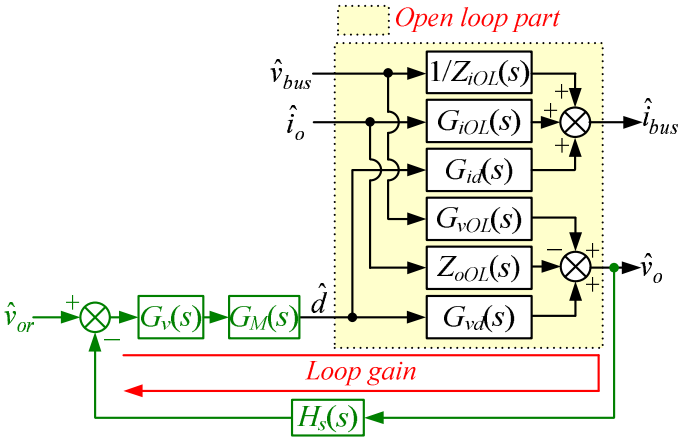


Figure 2.3: Small signal block diagram of the original load converter.

Table 2.1: Definitions of variables and transfer functions in load converter

$\hat{v}_{bus}$	Perturbation of the bus voltage
$\hat{i}_o$	Perturbation of the load current
$\hat{i}_{bus}$	Perturbation of the bus current
$\hat{d}$	Perturbation of the duty cycle
$\hat{v}_o$	Perturbation of the output voltage
$\hat{v}_{or}$	Perturbation of the output voltage reference
$G_v(s)$	Transfer function of the voltage regulator
$G_M(s)$	Transfer function of the modulator
$Z_{iOL}(s)$	Open-loop input impedance
$G_{vd}(s)$	Control to output voltage transfer function
$G_{id}(s)$	Control to input current transfer function
$Z_{oOL}(s)$	Open-loop output impedance
$H_s(s)$	Sampling coefficient of the output voltage
$G_{iOL}(s)$	Open-loop load to input current transfer function
$G_{vOL}(s)$	Open-loop input to output voltage transfer function

ensured.

2.1.3 Derivation of the PVI Control Strategy

As shown in Section 2.1.2, with Z_{PVI}, the cascaded system can be stabilised by changing $|Z_{iL}|$ or $\varphi(Z_{iL})$ in a very small frequency range to minimise the load compromise. Hence, in this section, a PVI control strategy for the load converter is proposed to realise Z_{PVI}.

First of all, the small signal block diagram of the original load converter is presented in Fig. 2.3. As seen, v_{bus} and i_{bus} are the input voltage and current of the load converter, respectively; and v_o and i_o are the output voltage and current of the load converter, respect-

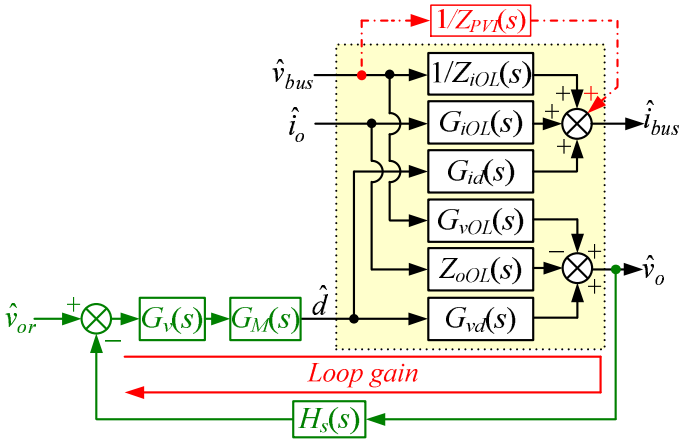


Figure 2.4: Small signal block diagram of the load converter with Z_{PVI}.

ively. d is the duty cycle of the load converter. $Z_{iOL}(s)$, $G_{iOL}(s)$, $G_{id}(s)$, $G_{vOL}(s)$, $Z_{oOL}(s)$ and $G_{vd}(s)$ are the six basic open-loop transfer functions of the load converter. In addition, for the original load converter, a voltage closed-loop is utilised, where $H_s(s)$ and $G_v(s)$ are the sampling coefficient and voltage regulator transfer function of the output voltage, respectively, and $G_M(s)$ is the transfer function of the modulator. All the variables and transfer functions of Fig. 2.3 are described in Table 2.1.

$Z_{iL}(s)$ is the input impedance of the original load converter. Therefore, for the original load converter, its i_{bus} and v_{bus} have the following relationship:

$$\frac{i_{bus}}{v_{bus}} = \frac{1}{Z_{iL}(s)} \tag{2.10}$$

If Z_{PVI} is required to be added in parallel with the input port of the load converter, the relationship between i_{bus} and v_{bus} is changed to:

$$\frac{i_{bus}}{v_{bus}} = \frac{1}{Z_{iL}(s)} + \frac{1}{Z_{PVI}(s)} \tag{2.11}$$

According to (2.11), the small signal block diagram of the load converter can be changed to Fig. 2.4.

As shown in Fig. 2.4, $1/Z_{PVI}$ is introduced to the control block between the v_{bus} and i_{bus} directly. From the small signal block diagram point of view, Fig. 2.4 achieves the purpose of adding Z_{PVI} in parallel with the input port of the load converter. However, from the control point of view, this method cannot be realised directly. It is because any converter

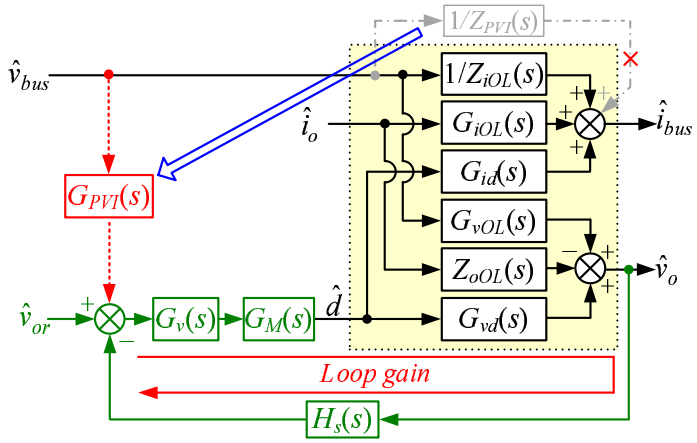


Figure 2.5: The PVI control strategy.

is only controlled by its duty cycle. In order to address this issue, the output of $1/Z_{PVI}$ is moved to the output voltage reference and equivalent adjustments are made to the transfer function to $G_{PVI}(s)$, as shown in Fig. 2.5.

According to Fig. 2.5, if $G_{PVI}(s)$ is required to realise the parallel virtual impedance $1/Z_{PVI}$, the following relationship can be obtained:

$$\hat{v}_{bus} \cdot \frac{1}{Z_{PVI}(s)} = \hat{v}_{bus} \cdot G_{PVI}(s) \cdot G_v(s) \cdot G_M(s) \cdot G_{id}(s) \cdot \frac{1}{1+T_v(s)} \tag{2.12}$$

where $T_v(s) = H_s(s)G_v(s)G_M(s)G_{vd}(s)$ is the voltage loop gain of the load converter.

According to (2.12), the expression of $G_{PVI}(s)$ can be derived as:

$$G_{PVI}(s) = \frac{1}{Z_{PVI}(s)} \cdot \frac{1+T_v(s)}{G_v(s) \cdot G_M(s) \cdot G_{id}(s)} \tag{2.13}$$

Up to this point, Fig. 2.3 $\sim$ Fig. 2.5 present the whole derivation process of the PVI control strategy; and $G_{PVI}(s)$ is the input-impedance-regulator of the PVI control strategy.

2.1.4 Realisation of the PVI Control Strategy

As discussed above, $G_{PVI}(s)$ is the key point of the PVI control strategy. Therefore, methods of realising $G_{PVI}(s)$ are discussed carefully in this section. According to (2.5), (2.9) and Fig. 2.5, the expression of $G_{PVI}(s)$ can be derived as:

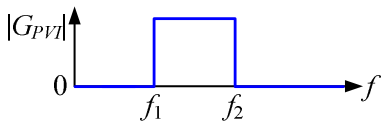


Figure 2.6: Characteristic of $|G_{PVI}(s)|$.

a) To achieve a total separation between $|Z_{oS}|$ and $|Z_{iLP}|$, $G_{PVI1}(s)$ is

$$G_{PVI1}(s) = \begin{cases} -\frac{V_{bus}^2 - |Z_{iL1}|P_o}{V_{bus}^2|Z_{iL1}|} \cdot \frac{1+T_v(s)}{G_v(s)\cdot G_M(s)\cdot G_{id}(s)} & f \in [f_1,\ f_2] \\ 0 & f \notin [f_1,\ f_2] \end{cases} \tag{2.14}$$

b) To ensure $|\varphi(Z_{oS}) - \varphi(Z_{iLP})| < 180^0$ at f_1 and f_2, $G_{PVI2}(s)$ is

$$G_{PVI2}(s) = \begin{cases} \frac{P_o}{V_{bus}^2} \cdot \frac{1+e^{j\theta}}{e^{j\theta}} \cdot \frac{1+T_v(s)}{G_v(s)\cdot G_M(s)\cdot G_{id}(s)} & f \in [f_1,\ f_2] \\ 0 & f \notin [f_1,\ f_2] \end{cases} \tag{2.15}$$

According to (2.14) and (2.15), $G_{PVI}(s)$ is a frequency-based piecewise transfer function, where $|G_{PVI}(s)| > 0$ within $[f_1,\ f_2]$ and $|G_{PVI}(s)| = 0$ outside $[f_1,\ f_2]$ as shown in Fig. 2.6. Hence, a band-pass filter $G_{BPF}(s)$ can be utilised to help achieve $G_{PVI}(s)$. In other words, (2.14) and (2.15) can be re-expressed as (2.16) and (2.17), respectively.

$$G_{PVI1}(s) = -\frac{V_{bus}^2 - |Z_{iL1}|P_o}{V_{bus}^2|Z_{iL1}|} \cdot \frac{1+T_v(s)}{G_v(s)\cdot G_M(s)\cdot G_{id}(s)} \cdot G_{BPF}(s) \tag{2.16}$$

$$G_{PVI2}(s) = \frac{P_o}{V_{bus}^2} \cdot \frac{1+e^{j\theta}}{e^{j\theta}} \cdot \frac{1+T_v(s)}{G_v(s)\cdot G_M(s)\cdot G_{id}(s)} \cdot G_{BPF}(s) \tag{2.17}$$

where $G_{BPF}(s)$ adopts a typical second order band-pass filter, which is composed of a second order high-pass filter and a second order low-pass filter, given as

$$G_{BPF}(s) = \frac{s^2}{s^2 + (2\pi f_1/Q_H)s + (2\pi f_1)^2} \cdot \frac{(2\pi f_2)^2}{s^2 + (2\pi f_2/Q_L)s + (2\pi f_2)^2} \tag{2.18}$$

where Q_H and Q_L are quality factors of the high-pass and low-pass filter, respectively.

According to (2.16) and (2.17), $G_{PVI}(s)$ is easy to realise using digital control chips, such as a digital signal processor (DSP), field programmable gate array (FPGA) and micro-

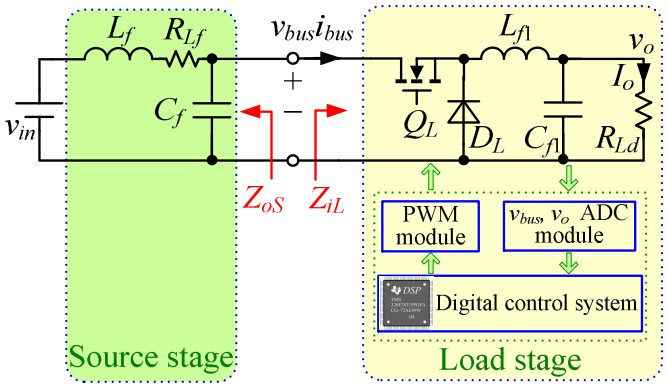


Figure 2.7: The System I.

Table 2.2: Parameters of the System I

Parameter	L_f	C_f	L_{f1}	C_{f1}	R_{Ld}
Value	700 μH	68 μF	33 μH	2400 μF	1.44Ω

controller unit (MCU).

2.2 Design Example

As illustrated in Chapter 1, the worst instability phenomena are most likely to occur when the source converter is a *LC* input filter. Buck and Boost converters are two typical DC/DC converters, so a 100 W cascaded system, which consists of a *LC* input filter and a 48 V - 12 V Buck converter, and a 200 W cascaded system, which includes a *LC* input filter and a 24 V - 48 V Boost converter, are designed in this section.

2.2.1 System I — a Buck Converter with a *LC* Input Filter

A 100 W cascaded system with a *LC* input filter (source stage) and a 48 V - 12 V Buck converter (load stage) has been designed, and are shown at Fig. 2.7. The Buck converter operates at 100 kHz. The cut-off frequency and phase margin of the voltage close loop of the Buck converter is set to 20 kHz and 45^o, respectively. The corresponding system parameters are summarised in Table 2.2.

The output impedance Z_{oS} of the *LC* input filter is given in (2.19), where R_{Lf} is the parasitic resistor of L_f and the measured value is 0.1 Ω. According to the small-signal circuit model of the Buck converter (Cuk, 1976), the input impedance Z_{iL} of the Buck

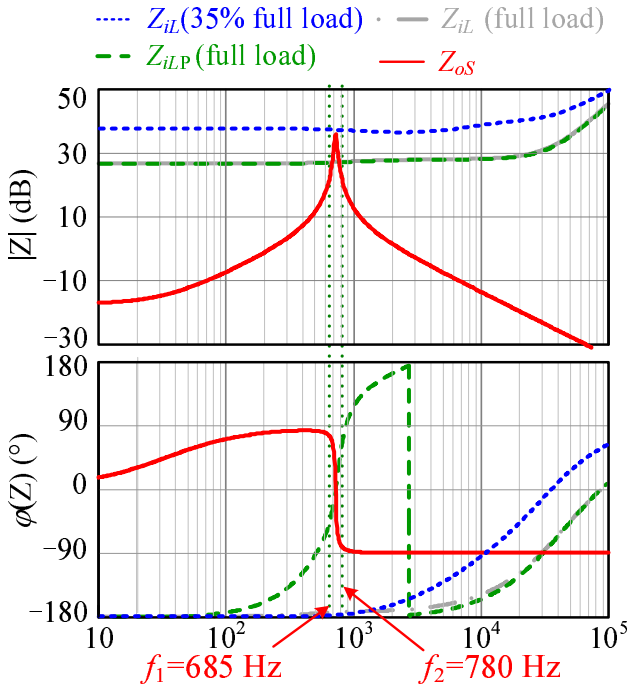


Figure 2.8: Bode plots of Z_{oS} and Z_{iL} of the System I.

converter can be expressed as (2.20).

$$Z_{oS}(s) = \left(sL_f + R_{Lf}\right) / \left(s^2 L_f C_f + sR_{Lf}C_f + 1\right) \tag{2.19}$$

$$Z_{iL}(s) = \left[\frac{1}{1+T_v(s)} \cdot \frac{sC_{f1}D^2 + \frac{D^2}{R_{Ld}}}{s^2 L_{f1}C_{f1} + s\frac{L_{f1}}{R_{Ld}} + 1} - \frac{T_v(s)}{1+T_v(s)} \cdot \frac{P_o}{V_{bus}^2}\right]^{-1} \tag{2.20}$$

where P_o and D are the output power and the duty cycle of the Buck converter, respectively.

Fig. 2.8 shows the Bode plots of Z_{oS} and Z_{iL} in the example system. As seen above, when the load is lower than 35% full-load, the system is stable; otherwise, the cascaded system is unstable and the oscillation should occur at about 685 Hz theoretically (Wildrick, 1993).

To conveniently solve the instability problem, Z_{iL} is designed to a positive resistor within $[f_1,\ f_2]$ to ensure $|\varphi(Z_{oS}) - \varphi(Z_{iLP})| < 180^0$, i.e., θ is set to 0 at (2.17). By the small signal model of Buck converter (Cuk, 1976) and (2.17), the expression of $G_{PVI}(s)$ can be derived as

$$G_{PVI}(s) = G_{PVI1}(s) \cdot P_o \cdot G_{BPF}(s) \tag{2.21}$$

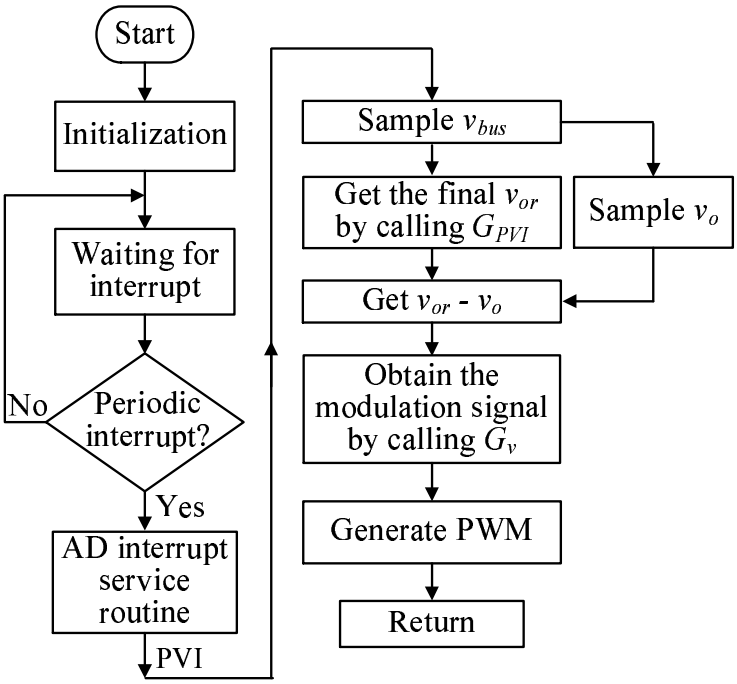


Figure 2.9: Software flowchart of the PVI control strategy.

where

$$G_{PVI1}(s) = \frac{2H_s(s)R_{Ld}}{V_{bus}V_o\left[s^2L_{f1}C_{f1} + s\left(R_{Ld}C_{f1} + L_{f1}/R_{Ld}\right) + 2\right]} \tag{2.22}$$

here, in $G_{BPF}(s)$, $f_1 = 685\,Hz$ and $f_2 = 780\,Hz$; $Q_H = 0.707$ and $Q_L = 0.707$.

The Bode plot of the modified input impedance, Z_{iLP}, is shown with dashed line in Fig. 2.8. As seen, $|\varphi(Z_{oS}) - \varphi(Z_{iLP})| < 180^0$ at f_1 and f_2. Therefore, the cascaded system will be stable and the design of $G_{PVI}(s)$ is appropriate.

Since the PVI control strategy is realised by the DSP TMS320F28335 in practice, its software flowchart is presented in Fig. 2.9. Both input and output voltage of the load converter are sampled to provide the necessary information for the PVI control strategy and to calculate the final reference of output voltage. With the final output voltage reference, the load converter is regulated by the compensator $G_v(s)$.

2.2.2 System II — a Boost Converter with a *LC* Input Filter

Fig. 2.10 shows a 200 W cascaded system consisting of a *LC* input filter (source stage) and a 24 V - 48 V Boost converter (load stage) operated at 100 kHz. Since the Boost converter is a non-minimum phase system, a proportional–integral (PI) controller is employed as

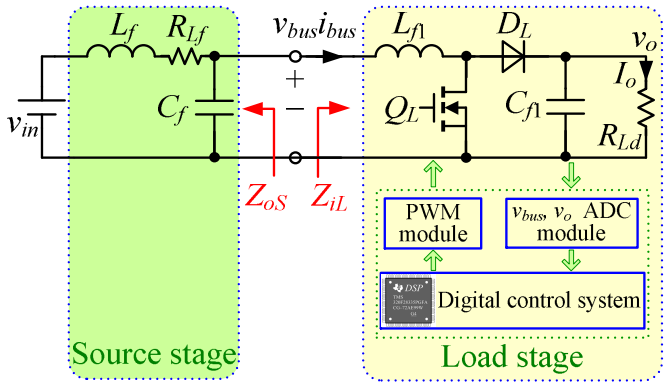


Figure 2.10: The System II.

Table 2.3: Parameters of the System II

Parameter	L_f	C_f	L_{f1}	C_{f1}	R_{Ld}
Value	250 μH	330 μF	720 μH	450 μF	11.52 Ω

the compensator, and the cut-off frequency and phase margin of the voltage closed loop of the Boost converter is set to 2.5 kHz and 32^o, respectively. The corresponding system parameters are summarised in Table 2.3.

The output impedance Z_{oS} of the *LC* input filter has been given in (2.19), thus it is not repeated here. Owing to the small-signal circuit model of the Boost converter (Cuk, 1976), the input impedance Z_{iL} of the Boost converter can be expressed as (2.23).

$$Z_{iL}(s) = \left[\frac{1}{1+T_v(s)} \cdot \frac{sC_{f1}R_{Ld}+1}{s^2L_{f1}C_{f1}R_{Ld}+sL_{f1}+R_{Ld}(1-D)^2} - \frac{T_v(s)}{1+T_v(s)} \cdot \frac{P_o}{V_{bus}^2} \right]^{-1} \tag{2.23}$$

where D and P_o are the duty cycle and output power of the Boost converter, respectively.

Fig. 2.11 shows the Bode plots of Z_{oS} and Z_{iL} in the example system, as seen when the load is lower than 20% full-load and the cascaded system is stable. Otherwise, the cascaded system is unstable and the oscillation occurs at theoretically about 520 Hz (Wildrick, 1993).

In order to solve the instability problem conveniently, Z_{iL} is designed to a positive resistor within $[f_1,\ f_2]$ to ensure $|\varphi(Z_{oS}) - \varphi(Z_{iLP})| < 180^0$, i.e., θ is set to 0 at (2.17). Then, according to the small signal model of Boost converter (Cuk, 1976) and (2.17), the expression of $G_{PVI}(s)$ can be derived as

$$G_{PVI}(s) \approx G_{PVI1}(s) \cdot G_{BPF}(s) \tag{2.24}$$

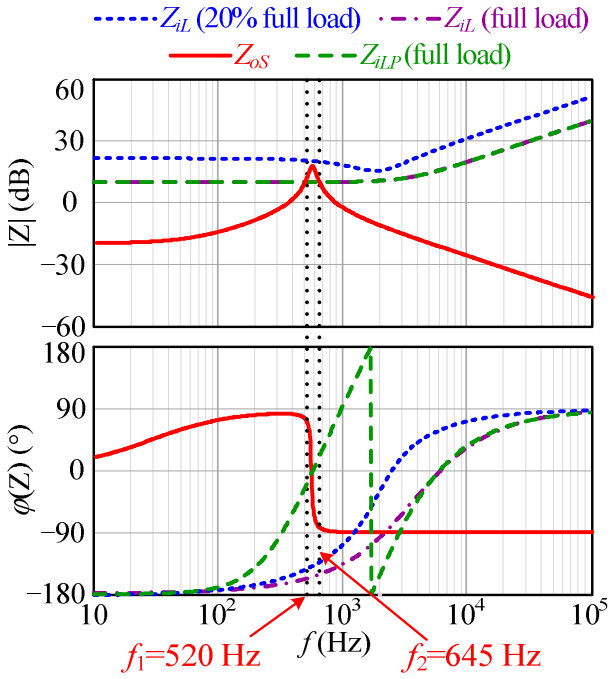


Figure 2.11: Bode plots of Z_{oS} and Z_{iL} of the System II.

where

$$G_{PVI1}(s) = \frac{2H_s(s)P_o}{V_{bus}V_o} \cdot \frac{R_{Ld} - sL_{f1}/(1-D)^2}{sC_{f1}R_{Ld} + 2} \tag{2.25}$$

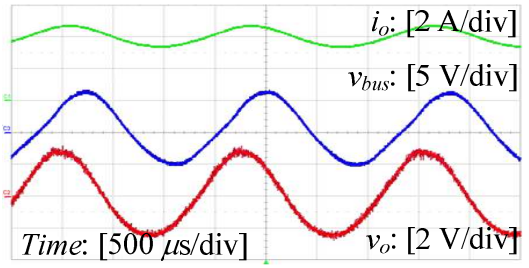
Also, for $G_{BPF}(s)$, f_1 = 520 Hz and f_2 = 645 Hz, $Q_H = Q_L = 0.707$.

The Bode plot of the modified input impedance, Z_{iLP}, is represented by a dashed line in Fig. 2.11, with $|\varphi(Z_{oS}) - \varphi(Z_{iLP})| < 180^0$ at f_1 and f_2. Therefore, the improved cascaded system is stable and the design of $G_{PVI}(s)$ is appropriate.

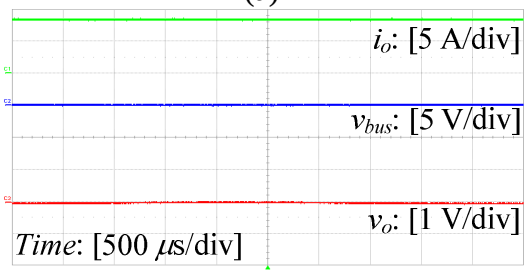
In practice, the Boost converter is also controlled by DSP TMS320F28335, and its PVI control strategy can be realised according to the software flowchart in Fig. 2.9. Since the flowchart has already been explained in Section 2.2.1, it is not repeated here.

2.3 Experimental Verification

According to the design examples, two experimental systems have been fabricated and tested in the lab to verify the validity of the PVI control strategy.

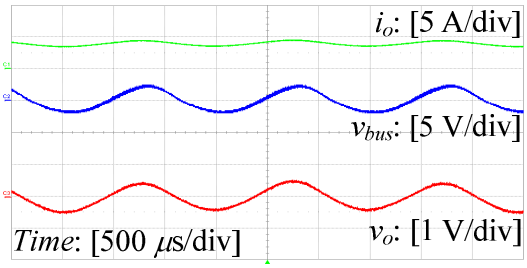


(a)

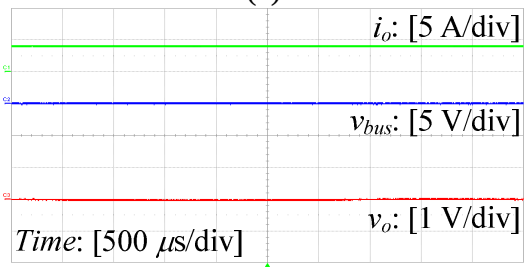


(b)

Figure 2.12: Experimental waveforms of System I at full load: (a) without PVI control strategy, (b) with PVI control strategy.



(a)



(b)

Figure 2.13: Experimental waveforms of System I at half load: (a) without PVI control strategy, (b) with PVI control strategy.

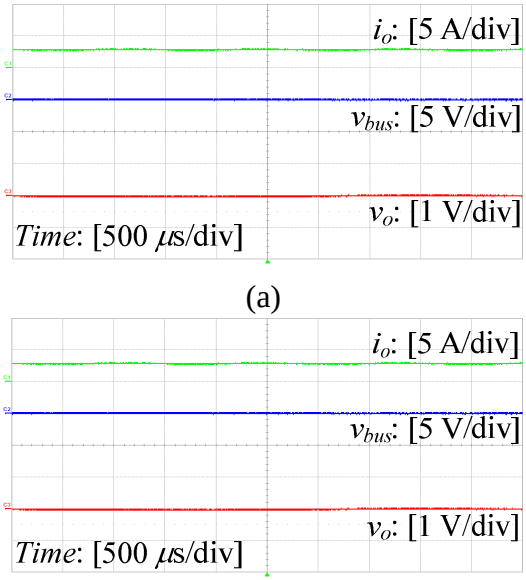


Figure 2.14: Experimental waveforms of System I at light load: (a) without PVI control strategy, (b) with PVI control strategy.

2.3.1 System I — a Buck Converter with a *LC* Input Filter

System I is a 100 W cascaded system consisting of a *LC* input filter and a 48 V - 24 V digital-controlled Buck converter. Its topology, parameters and control algorithm are presented in Fig. 2.7, Table 2.2 and Fig. 2.9, respectively.

The experimental results of System I with/without the PVI control strategy at different loads are given in Figs. 2.12 to 2.14, where the waveforms of v_{bus} and v_o are their ac components to clearly show the oscillation. As seen in Figs. 2.12(a) and 2.13(a), System I is unstable at full load and half load when the PVI control strategy is absent, and the oscillating frequencies of the bus voltage and output voltage are both about 685 Hz, which concurs with the conclusion at Fig. 2.8. As shown in Fig. 2.12(b) and Fig. 2.13(b), when the PVI control strategy is incorporated, System I becomes stable at full load and half load, and no oscillation occurs in v_{bus} and v_o. Fig. 2.14(a) shows the experimental waveforms of i_o, v_{bus} and v_o at 35% full-load without the PVI control strategy. It shows that System I is stable, which is consistent with Fig. 2.8. Besides, as shown in Fig. 2.14(b), System I is also stable at 35% full-load when the PVI control strategy is utilised.

In order to further show the zoomed waveforms of System I with/without the PVI control strategy at full load, its simulation results are given at Figs. 2.15(a) and (b). According

to the zoomed waveforms in Fig. 2.15, the PVI control strategy indeed solves the instability problem of System I.

Based on Fig. 2.15(a), the harmonic distribution histogram of System I without PVI control strategy at full load is presented at Fig. 2.16. It is shown that, without the PVI control strategy, there is an obvious harmonic component of i_o, v_{bus} and v_o at 700 Hz, which is around the oscillation frequency. According to Fig. 2.16, the oscillation deteriorates the quality of i_o, v_{bus} and v_o: with the total harmonic distortion (THD) of the unstable i_o, v_{bus} and v_o at 9.488%, 13.969% and 9.488%, respectively.

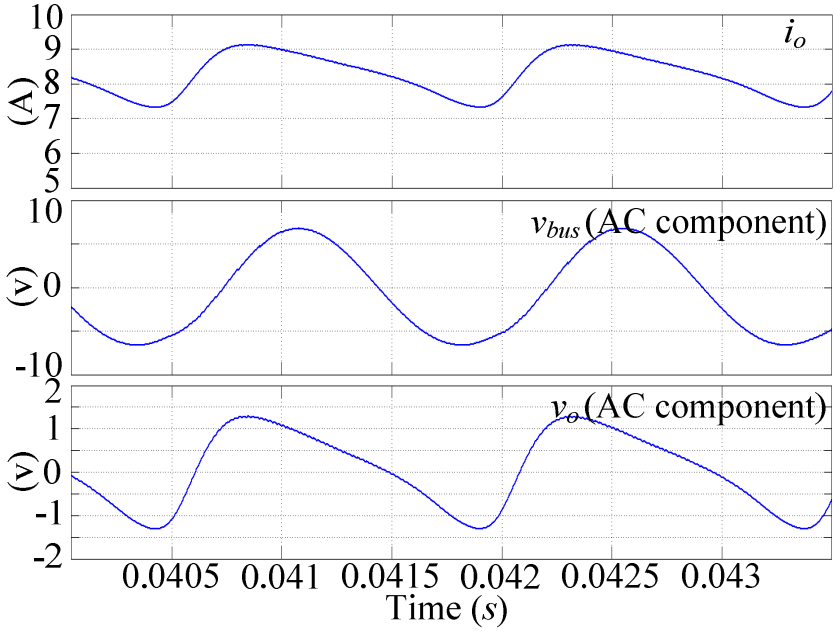
Based on Fig. 2.15(b), the harmonic distribution histogram of System I with PVI control strategy at full load is presented at Fig. 2.17. It can be seen that there is no obvious harmonic component of i_o, v_{bus} and v_o with the PVI control strategy. Therefore, the PVI control strategy indeed solves the instability problem of System I at full load. In addition, compared to Fig. 2.16, the PVI control strategy also improves the quality of i_o, v_{bus} and v_o: with the THD of stable i_o, v_{bus} and v_o reduced to 0.013%, 0.001% and 0.013%, respectively.

Fig. 2.18(a) shows the dynamic performance of System I when its load steps between 10% and 100% full-load at the rated input voltage (48 V) indicating that the dynamic performances of System I with PVI control strategy are good. Fig. 2.18(b) shows the dynamic performance of System I when its input voltage steps between 80% (38.4 V) and 120% (57.6 V) rated voltage at full load. It can be seen that the dynamic performance of System I with PVI control strategy is also good.

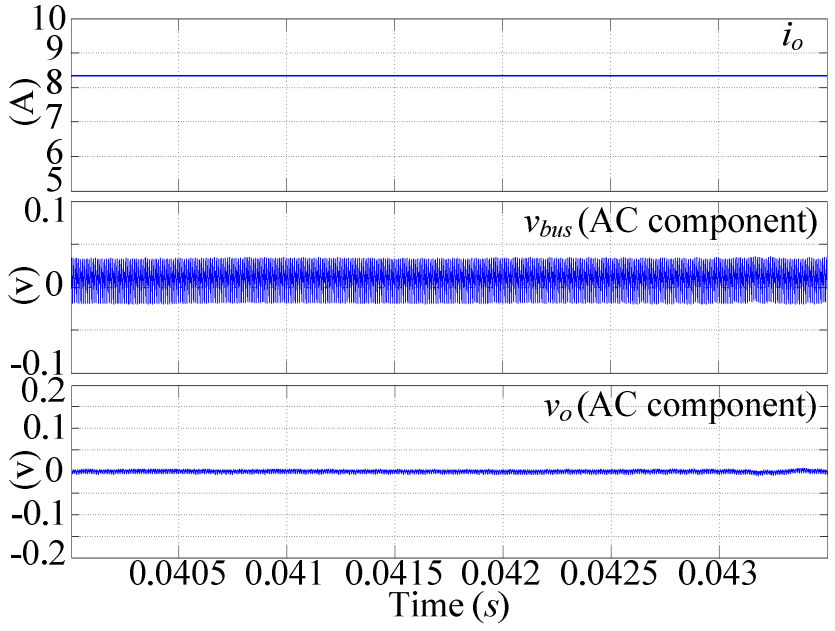
2.3.2 System II — a Boost Converter with a *LC* Input Filter

A 200W cascaded system with a *LC* input filter and a 24 V - 48 V digital-control-based Boost converter is fabricated. Its topology, parameters and control algorithm have already been described in Fig. 2.10, Table 2.3 and Fig. 2.9, respectively.

The experimental results of System II with/without the PVI control strategy at different loads are given in Figs. 2.19 to 2.21, where the waveforms of v_{bus} and v_o are their ac components to clearly show the oscillation. As seen in Figs. 2.19(a) and 2.20(a), System II is unstable at full load and half load when the PVI control strategy is absent, and the oscillating frequencies of the bus voltage and output voltage are both approximately 520 Hz, which concurs with the conclusion at Fig. 2.11. As shown in Fig. 2.19(b) and Fig.

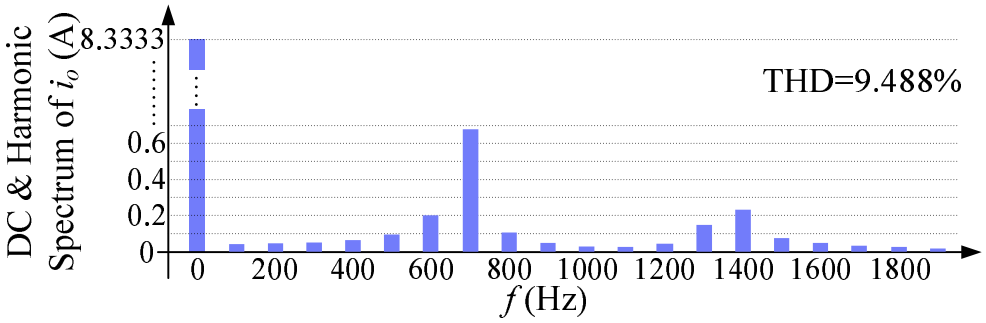


(a)

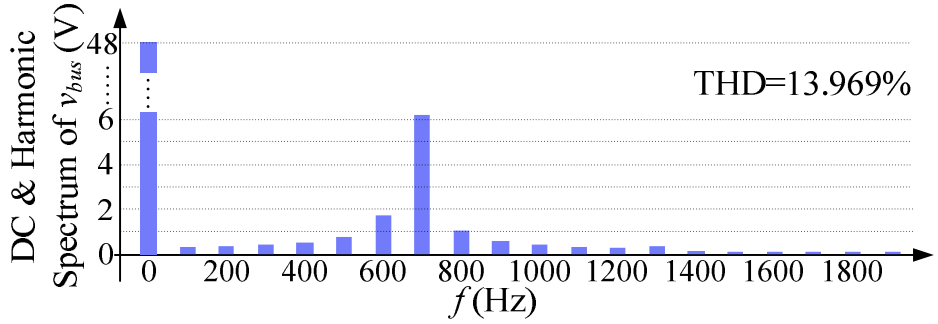


(b)

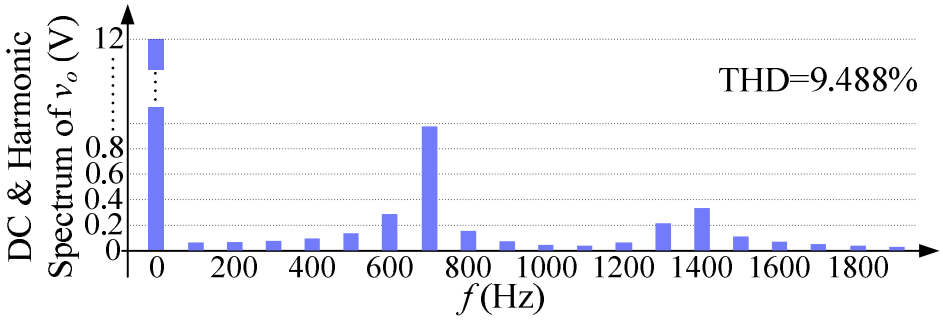
Figure 2.15: Simulation waveforms of System I at full load: (a) without PVI control strategy, (b) with PVI control strategy.



(a)



(b)



(c)

Figure 2.16: Harmonic distribution histogram of System I without PVI control strategy at full load: (a) i_o, (b) v_{bus}, (c) v_o.

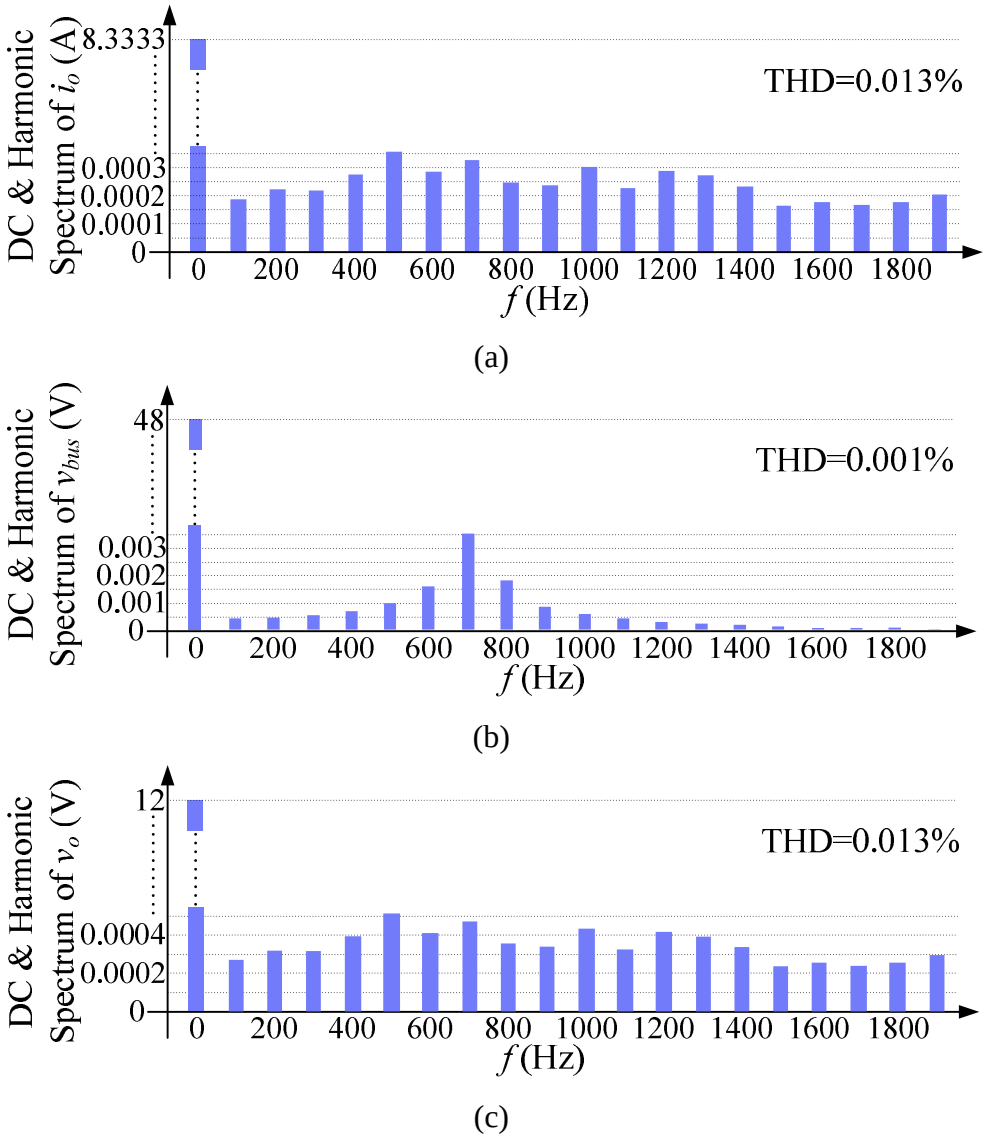


Figure 2.17: Harmonic distribution histogram of System I with PVI control strategy at full load: (a) i_o, (b) v_{bus}, (c) v_o.

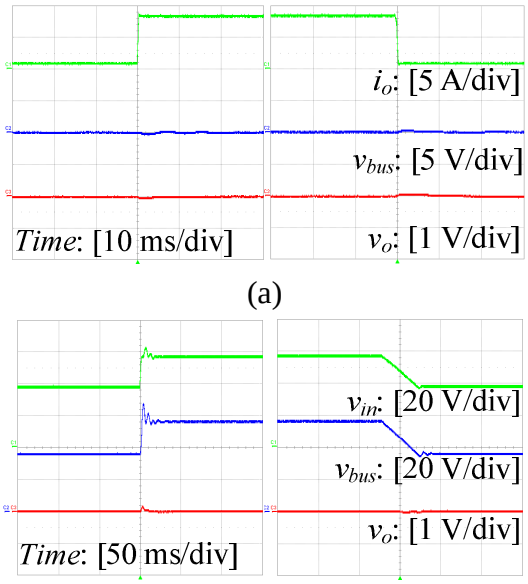


Figure 2.18: Dynamic experimental waveforms of System I with PVI control strategy: (a) load changing between 10% load and 100% load, (b) input voltage changing between 80% rated voltage and 120% rated voltage.

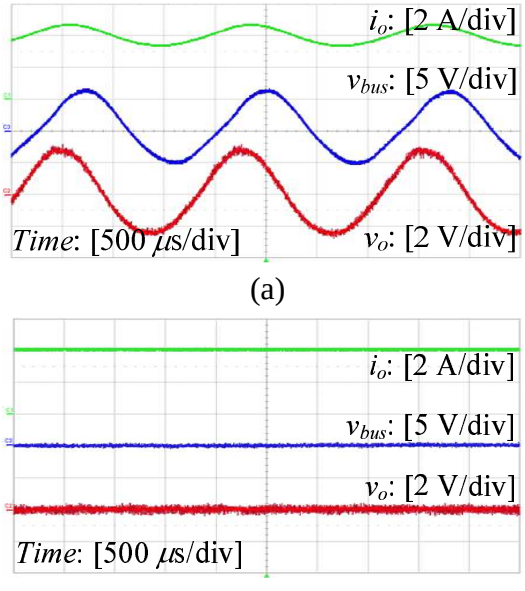
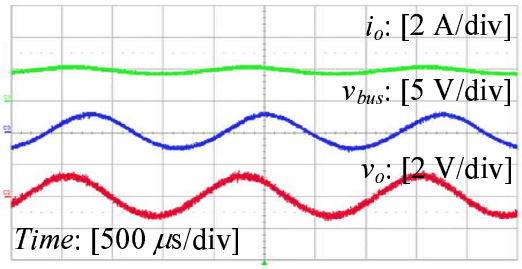
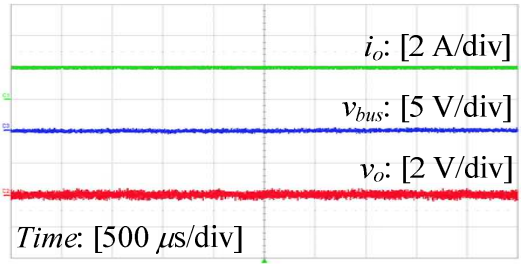


Figure 2.19: Experimental waveforms of System II at full load: (a) without PVI control strategy, (b) with PVI control strategy.



(a)



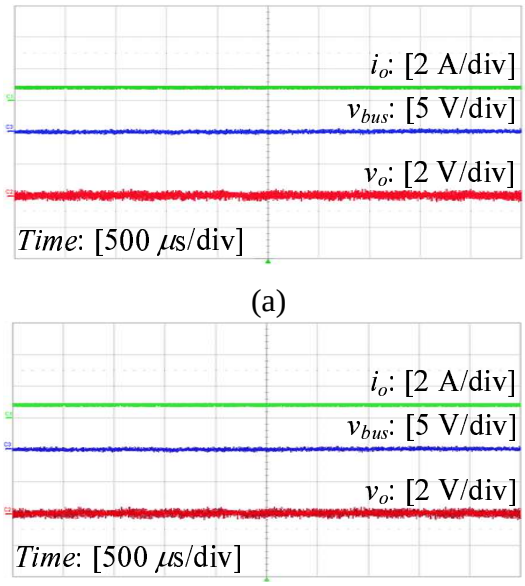
(b)

Figure 2.20: Experimental waveforms of System II at half load: (a) without PVI control strategy, (b) with PVI control strategy.

2.20(b), when the PVI control strategy is incorporated, System II becomes stable at full load and half load, and no oscillation occurs in v_{bus} and v_o. Fig. 2.21(a) shows the experimental waveforms of i_o, v_{bus} and v_o at 20% full-load without the PVI control strategy. It is shown here that System II is stable, which is consistent with Fig. 2.11, and Fig. 2.21(b) indicates that System II is stable at 20% full-load when the PVI control strategy is utilised.

Fig. 2.22(a) shows the dynamic waveforms of System II when its load steps between 10% and 100% full-load at the rated input voltage (24 V). The dynamic performance of System II with PVI control strategy is good. Fig. 2.22(b) shows the dynamic performance of System II with the input voltage steps between 80% (19.2 V) and 120% (28.8 V) rated voltage at full load. It is shown that the dynamic performance of System II with PVI control strategy is good.

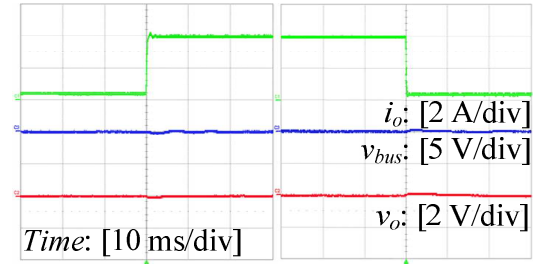
The above two examples indicate that the PVI control strategy is effective and feasible in practice.



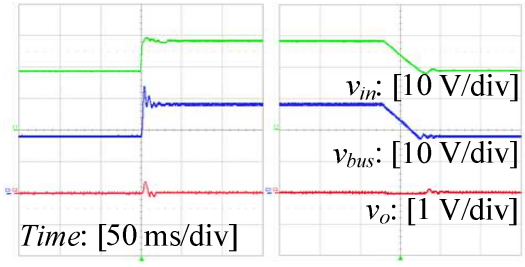
(a)

(b)

Figure 2.21: Experimental waveforms of System II at light load: (a) without PVI control strategy, (b) with PVI control strategy.



(a)



(b)

Figure 2.22: Dynamic experimental waveforms of System II with PVI control strategy: (a) load changing between 10% load and 100% load, (b) input voltage changing between 80% rated voltage and 120% rated voltage.

2.4 Simulation Verification

2.4.1 Simulation Verification of System I with the Consideration of the Load Input Capacitor

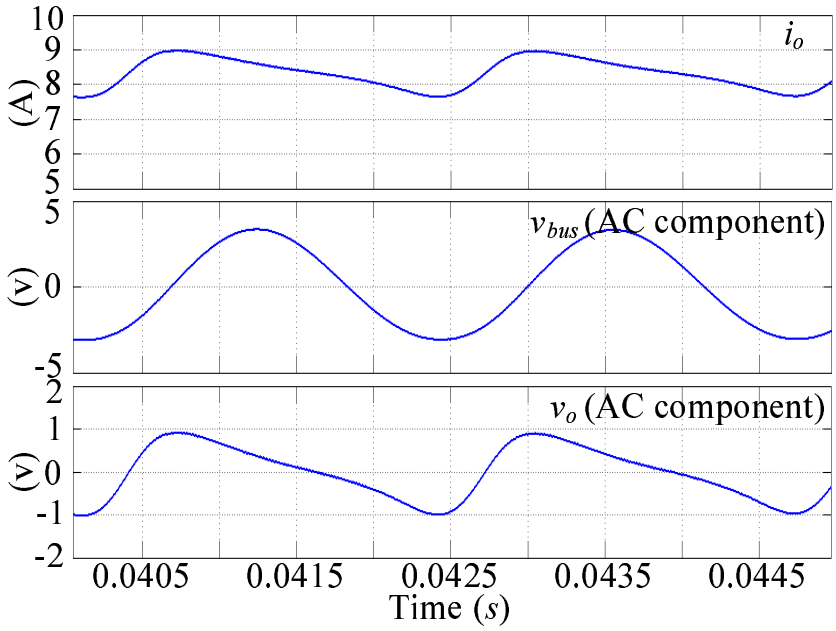
The input capacitor is usually a necessary component of DC/DC converters in practice. Therefore, a simulink model adding a 110 μF input capacitor to the Buck converter of Fig. 2.7 has been built in Matlab to verify the accuracy of the PVI control strategy.

The simulation results of System I with consideration of load input capacitor at different loads are given in Figs. 2.23 to 2.25. As with the above experimental results, the simulation waveforms of v_{bus} and v_o are also their ac components and clearly show the oscillation. As seen in Figs. 2.23(a) and 2.24(a), System I is unstable at full load and half load when the PVI control strategy is absent. As shown in Fig. 2.23(b) and Fig. 2.24(b), when the PVI control strategy is incorporated, System I becomes stable at full load and half load, and no oscillation occurs in v_{bus} and v_o. Fig. 2.25(a) shows the simulation waveforms of i_o, v_{bus} and v_o at 35% full-load without the PVI control strategy. It shows that System I is stable. As shown in Fig. 2.25(b), System I is also stable at 35% full-load when the PVI control strategy is utilised. It is worth pointing out that thanks to the added input capacitor, the oscillation waveforms in Figs. 2.23(a) and 2.24(a) are smaller than those in Figs. 2.12(a) and 2.13(a).

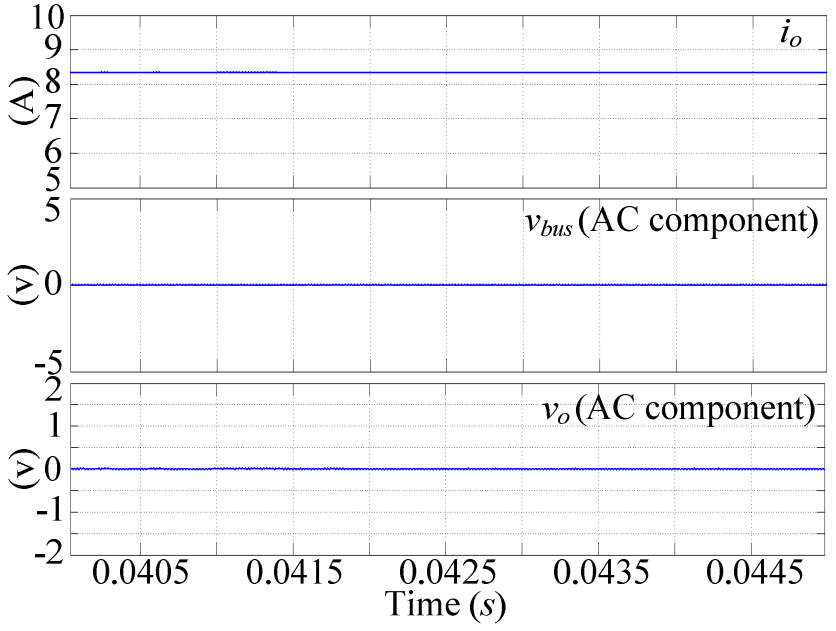
Fig. 2.26(a) shows the load dynamic performance of System I with the PVI control strategy and the added load input capacitor. It shows that when the load steps between 10% and 100% full-load at the rated input voltage (48 V), the dynamic performance of System I is good. Fig. 2.26(b) shows the input voltage dynamic performance of System I with the PVI control strategy and the added load input capacitor. It also shows that with the input voltage steps between 80% (38.4 V) and 120% (57.6 V) rated voltage at full load, the dynamic performance of System I is also good.

2.4.2 Simulation Verification of System II with the Consideration of the Load Input Capacitor

Similarly, a simulink model adding a 110 μF input capacitor to the Boost converter in Fig. 2.10 has also been built in Matlab to verify the accuracy of the PVI control strategy.

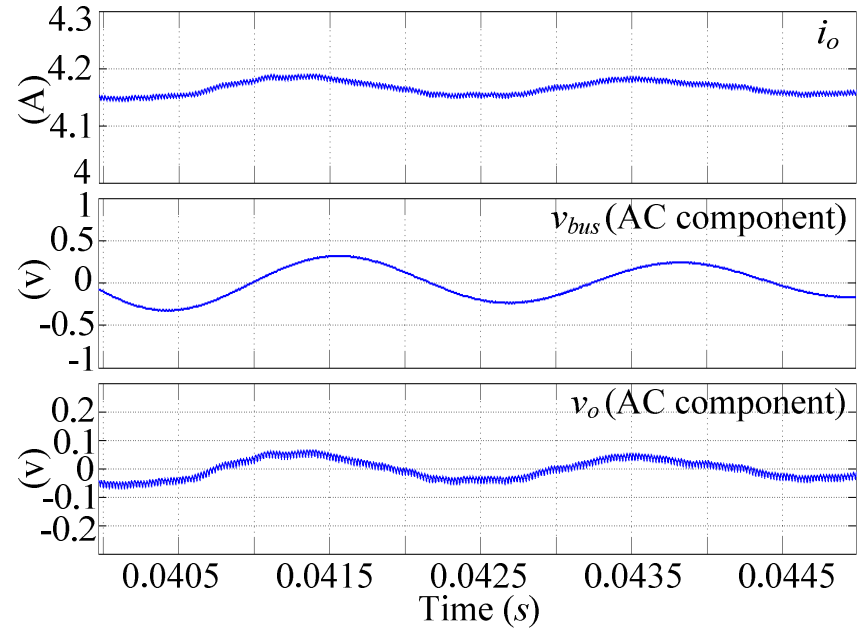


(a)

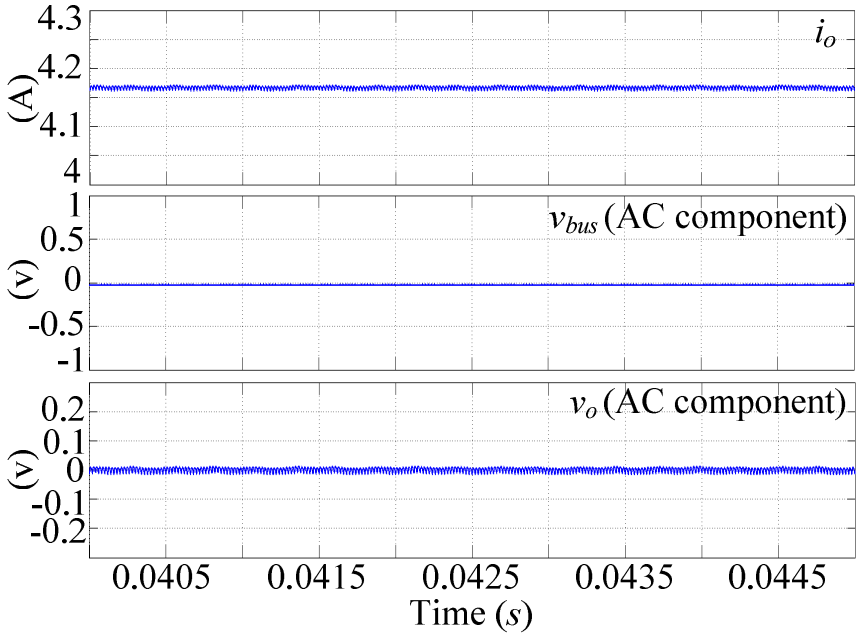


(b)

Figure 2.23: Simulation waveforms of System I with the added load input capacitor at full load: (a) without PVI control strategy, (b) with PVI control strategy.

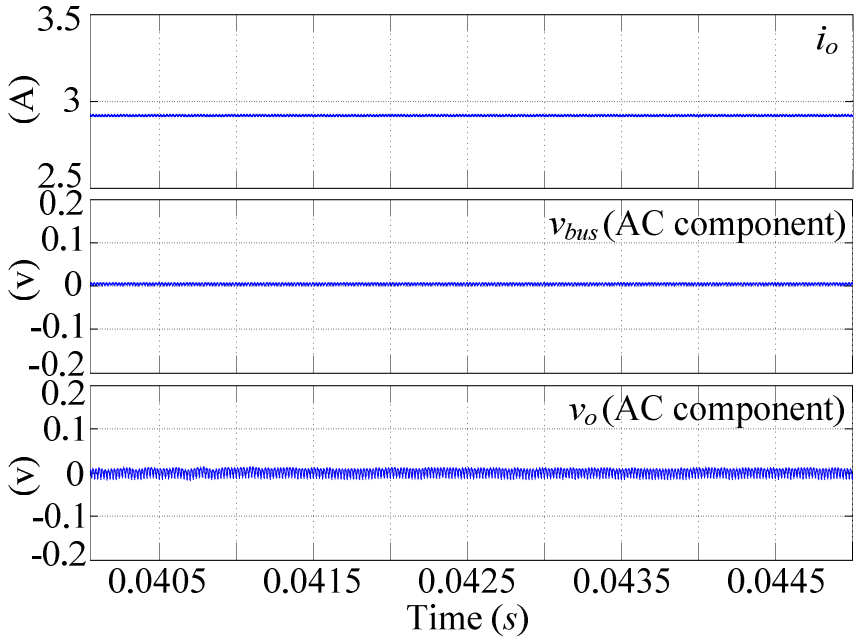


(a)

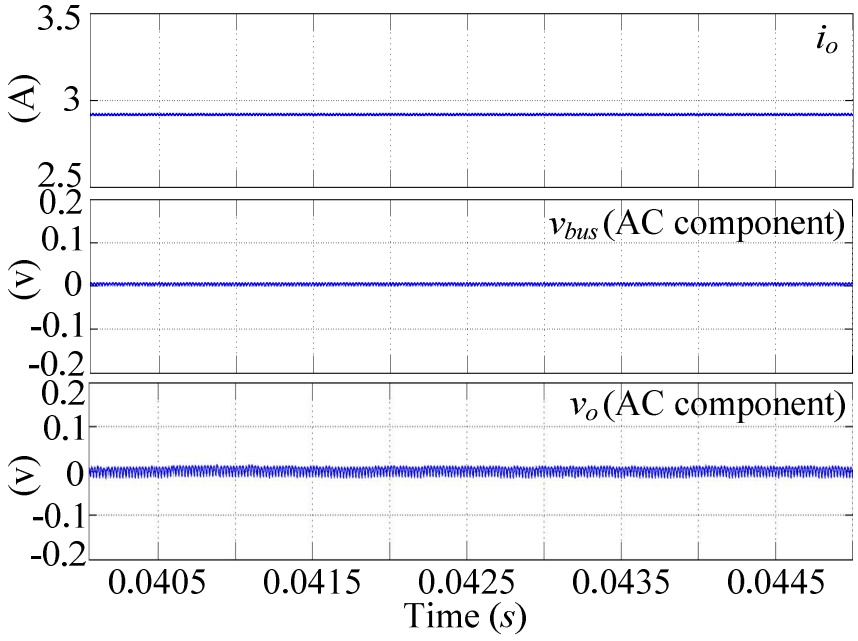


(b)

Figure 2.24: Simulation waveforms of System I with the added load input capacitor at half load: (a) without PVI control strategy, (b) with PVI control strategy.

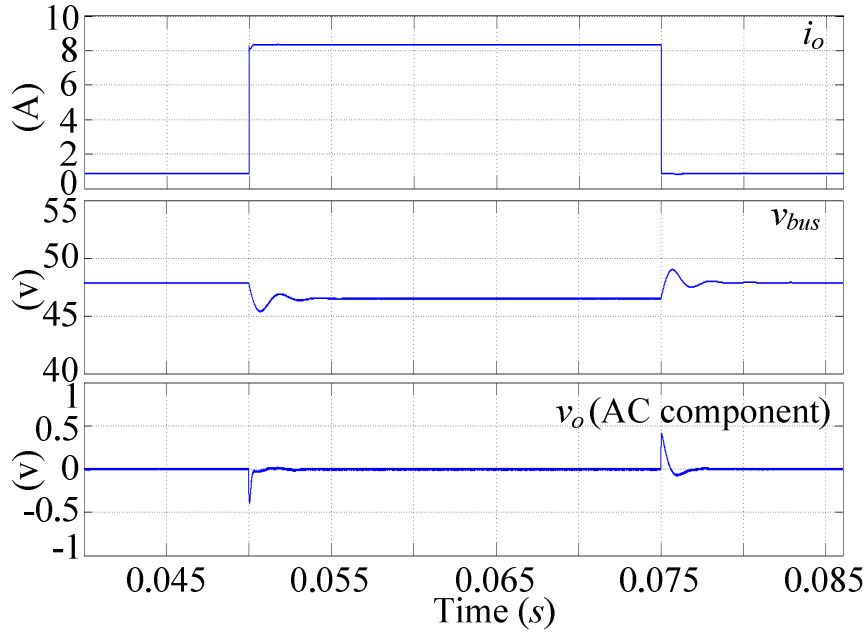


(a)

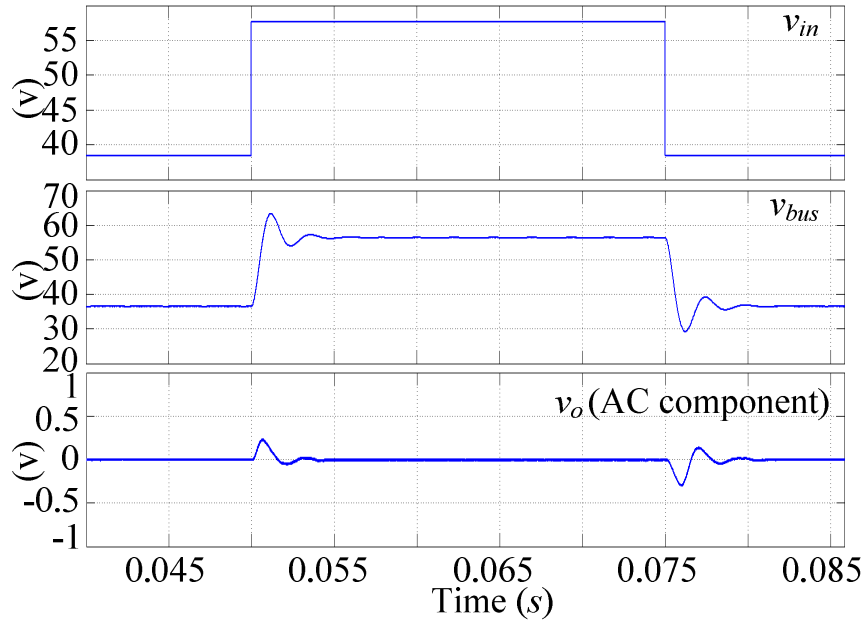


(b)

Figure 2.25: Simulation waveforms of System I with the added load input capacitor at light load: (a) without PVI control strategy, (b) with PVI control strategy.



(a)



(b)

Figure 2.26: Dynamic simulation waveforms of System I with PVI control strategy and the added load input capacitor: (a) load changing between 10% load and 100% load, (b) input voltage changing between 80% rated voltage and 120% rated voltage.

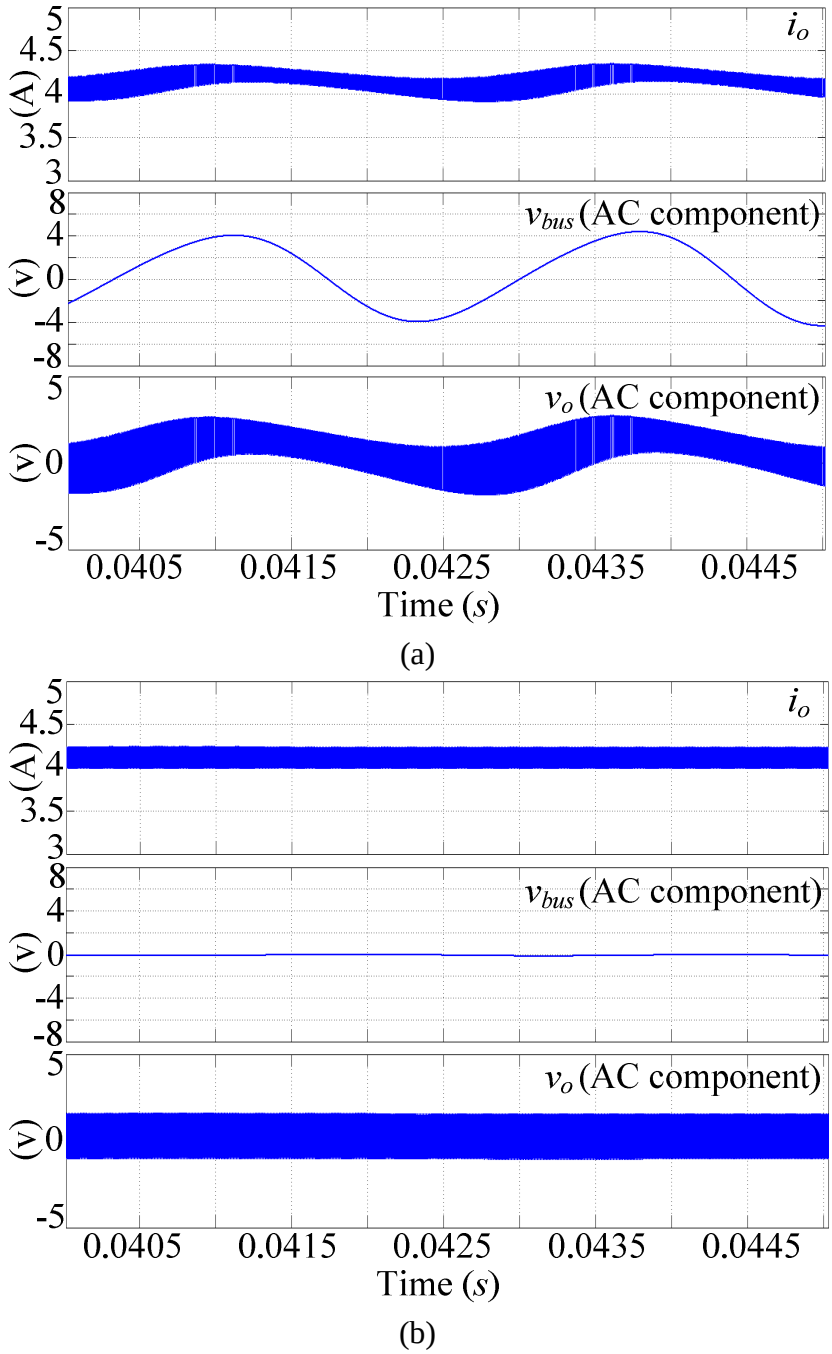
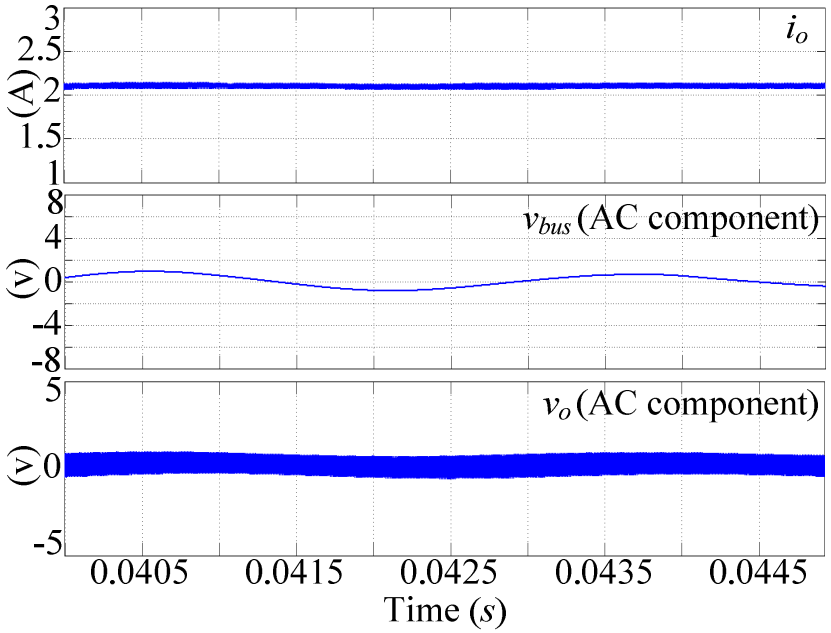
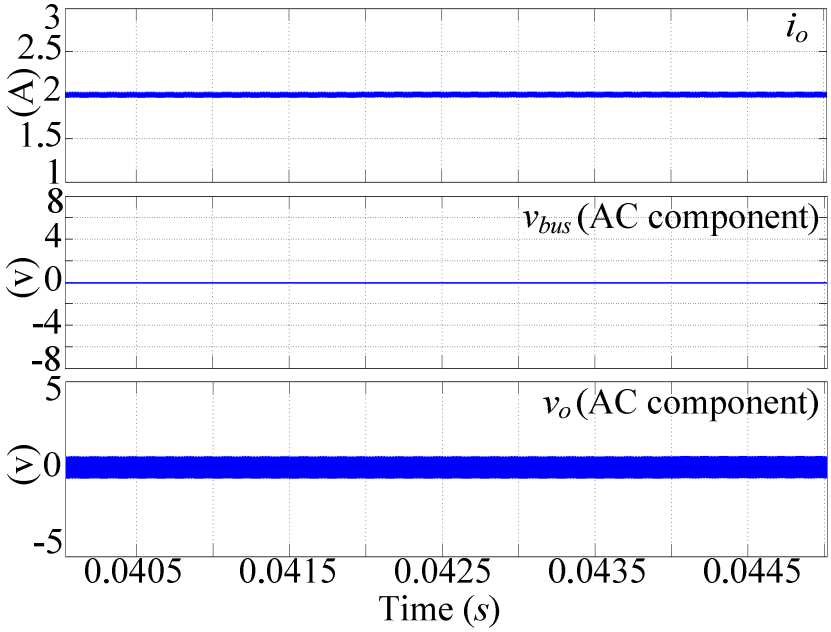


Figure 2.27: Simulation waveforms of System II with the added load input capacitor at full load: (a) without PVI control strategy, (b) with PVI control strategy.



(a)



(b)

Figure 2.28: Simulation waveforms of System II with the added load input capacitor at half load: (a) without PVI control strategy, (b) with PVI control strategy.

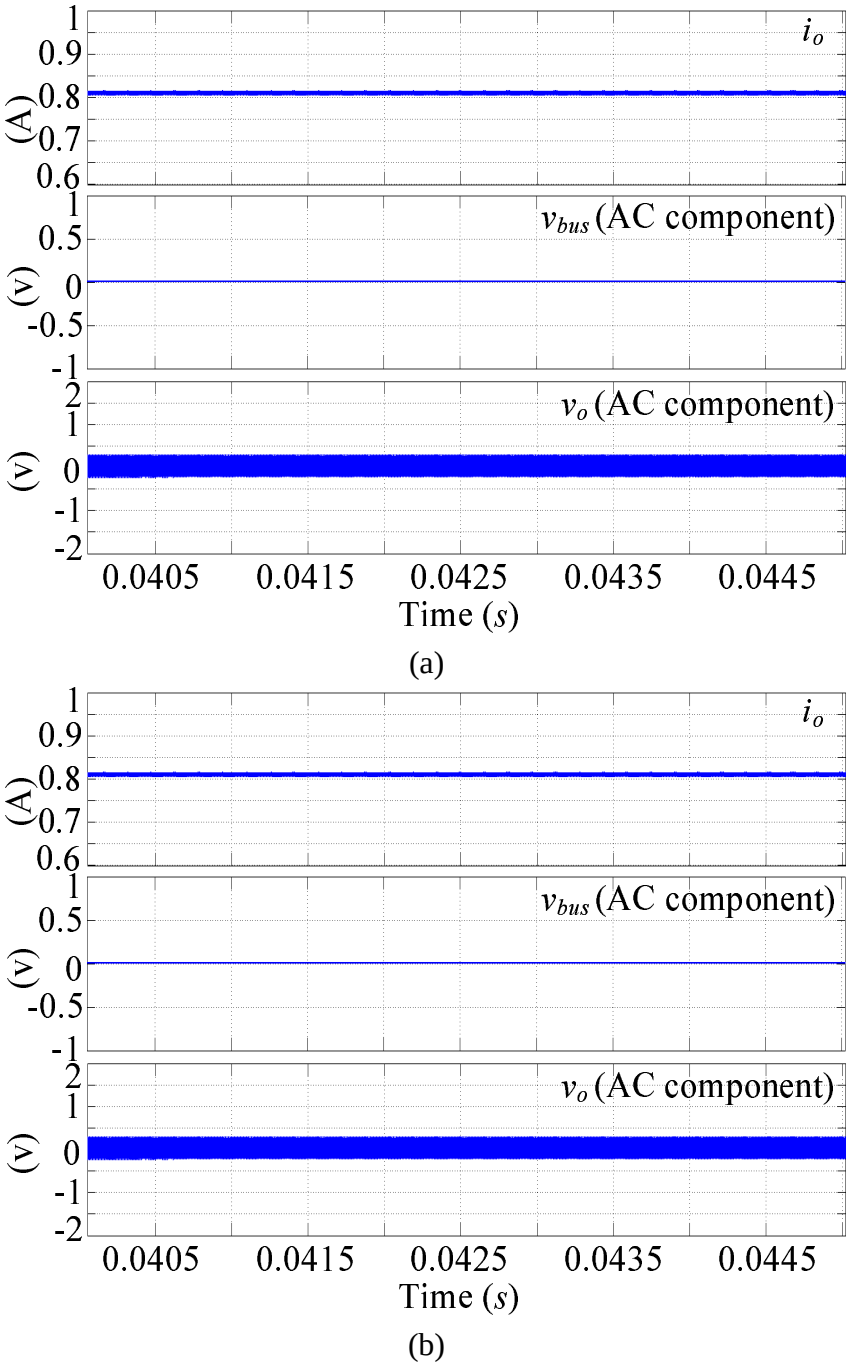
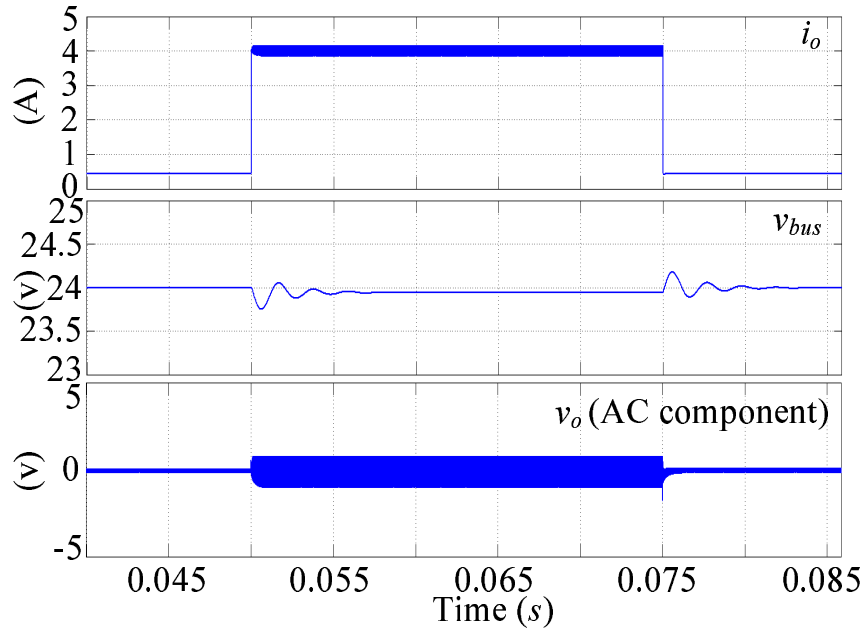
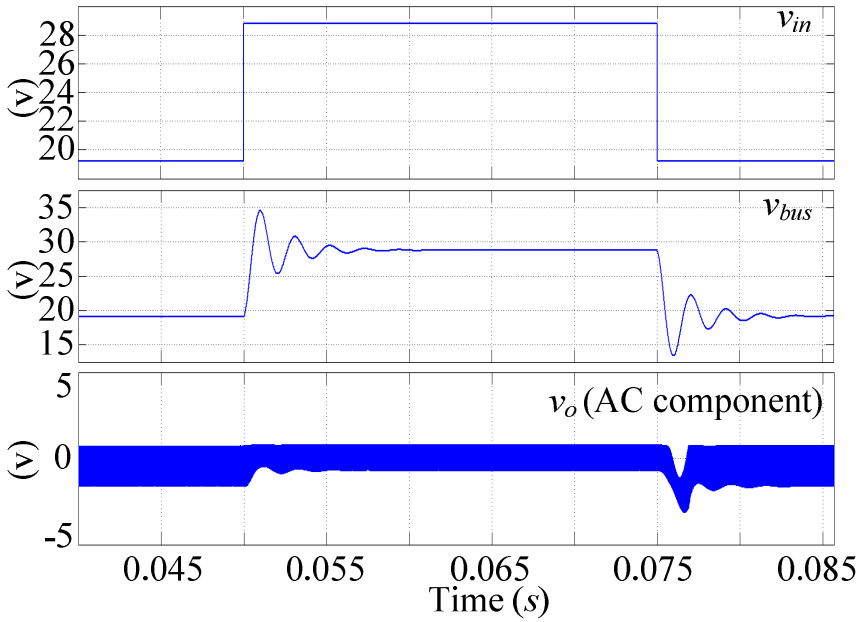


Figure 2.29: Simulation waveforms of System II with the added load input capacitor at light load: (a) without PVI control strategy, (b) with PVI control strategy.



(a)



(b)

Figure 2.30: Dynamic simulation waveforms of System II with PVI control strategy and the added load input capacitor: (a) load changing between 10% load and 100% load, (b) input voltage changing between 80% rated voltage and 120% rated voltage.

The simulation results of System II with consideration of load input capacitor at different loads are given in Figs. 2.27 to 2.29. Similar to the above experimental results, the simulation waveforms of v_{bus} and v_o are also their ac components and clearly show the oscillation. As seen in Figs. 2.27(a) and 2.28(a), System II is unstable at full load and half load when the PVI control strategy is absent. As shown in Fig. 2.27(b) and Fig. 2.28(b), when the PVI control strategy is incorporated, System II becomes stable at full load and half load, and no oscillation occurs in v_{bus} and v_o. Fig. 2.29(a) shows the simulation waveforms of i_o, v_{bus} and v_o at 20% full-load without the PVI control strategy. It shows that System II is stable. In addition, as shown in Fig. 2.29(b), System II is also stable at 20% full-load when the PVI control strategy is utilised. It is worth pointing out that, thanks to the added input capacitor, the oscillation waveforms in Figs. 2.27(a) and 2.28(a) are smaller than those in Figs. 2.19(a) and 2.20(a).

Fig. 2.30(a) shows the load dynamic waveforms of System II with the PVI control strategy and the added load input capacitor. It shows that with load steps between 10% and 100% full-load at the rated input voltage (24 V), the dynamic performance of System II is good. Fig. 2.30(b) shows the input voltage dynamic performance of System II with the PVI control strategy and the added load input capacitor. It also shows that with the input voltage steps between 80% (19.2 V) and 120% (28.8 V) rated voltage at full load, the dynamic performance of System II is also good.

The above simulation results demonstrate that the PVI control strategy is effective and feasible when the load converter contains input capacitors.

2.5 Summary

In order to solve the instability problem of the cascaded system, a PVI control strategy is proposed in this chapter. This research shows that the PVI control strategy modifies the input impedance of the load converter only in a small range of frequencies. Therefore, it not only stabilises the whole system, but also ensures a good dynamic performance of the load converter. Furthermore, the proposed method can be realised by a simple digital control algorithm, thus this approach is feasible in practice. Finally, two example systems are fabricated to validate the correctness of the PVI control strategy.

Chapter 3

Series-Virtual-Impedance (SVI) Control for Load Converters

In Chapter 2, a PVI control strategy is proposed to stabilise the cascaded system with the minimised load compromise. Since the PVI control strategy can add a virtual impedance in parallel with the load converter to realise its function, it can be assumed that a corresponding virtual impedance also can be added in the series with the load converter to realise the same function. Therefore, a series-virtual-impedance (SVI) control strategy is proposed in this chapter, which can also be treated as a development of, and complement to the PVI control strategy. The concept, derivation and design examples of the SVI control strategy are discussed carefully in this chapter. Similar to the PVI control strategy, the SVI control strategy is also verified by two experimental/simulation cascaded systems.

The other parts of this chapter are arranged as follows: in Section 3.1, the basic idea of load stabilisation methods, the concept and realisation of the SVI control strategy are studied. Following that, two design examples of the SVI control strategy are presented in Section 3.2; and two experimental/simulation cascaded systems are fabricated to verify the effectiveness of the SVI control strategy in Sections 3.3 and 3.4, respectively. Finally, Section 3.5 concludes the chapter.

3.1 SVI Control Strategy

3.1.1 Basic Idea of Load Shaping Methods

As discussed in Chapter 2, when a designer wants to keep the cascaded system stable while keeping a better performance of load converter, the best load stabilisation method is to change Z_{iL} only in the vicinity of the intersection frequencies of $|Z_{oS}|$ and $|Z_{iL}|$. Here, Z_{oS} is the source output impedance, and Z_{iL} is the load input impedance.

As shown in Fig. 3.1, there are two better ways to regulate Z_{iL}:

(a) Make a total separation of $|Z_{oS}|$ and $|Z_{iL}|$ by increasing $|Z_{iL}|$ only during $[f_1, f_2]$ (See Fig. 3.1(a));

(b) Ensure $|\varphi(Z_{oS}) - \varphi(Z_{iL})| < 180^0$ at f_1 and f_2 by increasing $\varphi(Z_{iL})$ only during $[f_1, f_2]$ (See Fig. 3.1(b)). Here, f_1 and f_2 are the intersection frequencies of $|Z_{oS}|$ and $|Z_{iL}|$.

Note, in Fig. 3.1, Z_{iLS} is the input impedance of the load converter with the latter proposed SVI control strategy.

3.1.2 Expression of the Series-Virtual-Impedance $Z_{SVI}(s)$

The load shaping idea in Section 3.1.1 can be realised by adding a virtual impedance $Z_{SVI}(s)$ in series with the load input port. As shown in Fig. 3.2, the shaped load input impedance $Z_{iLS}(s)$ can be expressed as

$$Z_{iLS} = Z_{iL} + Z_{SVI} \tag{3.1}$$

where Z_{iL} is the original input impedance of the load converter and if $f < f_{CL}$ its expression is $-V_{bus}^2/P_o$. Here, V_{bus} and P_o are the input voltage and output power of the load converter, respectively.

a) As illustrated in Fig. 3.1(a), if a total separation between $|Z_{oS}|$ and $|Z_{iLS}|$ is needed and the minimised change of Z_{iL} is also required, Z_{iLS} should satisfy:

$$If\{f \in [f_1, f_2]\} \quad \rightarrow \quad |Z_{iLS}| > Z_{oSP} \tag{3.2}$$

$$If\{f \notin [f_1, f_2]\} \quad \rightarrow \quad Z_{iLS} = Z_{iL} \tag{3.3}$$

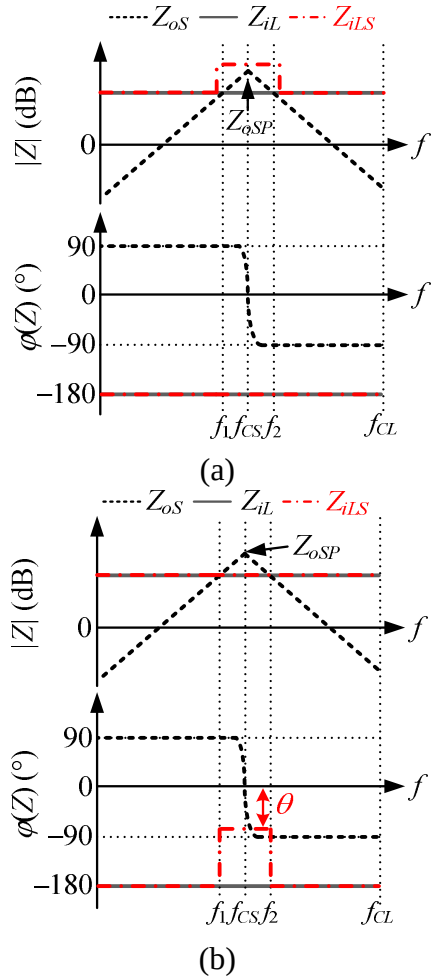


Figure 3.1: Basic idea of load shaping methods: (a) only increasing $|Z_{iL}|$ at $[f_1,\ f_2]$ to make a total separation between $|Z_{oS}|$ and $|Z_{iL}|$; (b) only increasing $\varphi(Z_{iL})$ at $[f_1,\ f_2]$ to ensure $|\varphi(Z_{oS}) - \varphi(Z_{iL})| < 180^0$ at $[f_1,\ f_2]$.

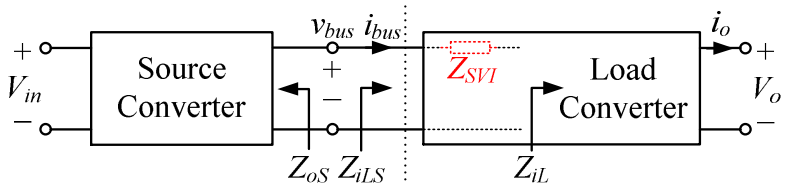


Figure 3.2: A cascaded system with series virtual impedance.

where Z_{oSP} is the peak value of $|Z_{oS}|$.

According to (3.2) and (3.3), Z_{iLS} could be further expressed as

$$Z_{iLS} = \begin{cases} -|Z_{iL1}| & f \in [f_1,\, f_2] \\ Z_{iL} & f \notin [f_1,\, f_2] \end{cases} \tag{3.4}$$

where $|Z_{iL1}| > Z_{oSP}$ is the amplitude of Z_{iLS} during $[f_1,\, f_2]$.

According to (3.1) and (3.4), in order to ensure $|Z_{iL}|$ successfully becomes $|Z_{iLS}|$ as shown in Fig. 3.1(a), Z_{SVI} can be selected as

$$\begin{aligned} Z_{SVI} &= Z_{iLS} - Z_{iL} = \begin{cases} -|Z_{iL1}| - \left(-V_{bus}^2/P_o\right) & f \in [f_1,\, f_2] \\ Z_{iL} - Z_{iL} & f \notin [f_1,\, f_2] \end{cases} \\ &= \begin{cases} \left(V_{bus}^2/P_o\right) - |Z_{iL1}| & f \in [f_1,\, f_2] \\ 0 & f \notin [f_1,\, f_2] \end{cases} \end{aligned} \tag{3.5}$$

b) Similarly, according to Fig. 3.1(b), if $|\varphi(Z_{oS}) - \varphi(Z_{iLS})| < 180^0$ is to be ensured within $[f_1,\, f_2]$ and the minimised change of Z_{iL} is also required, Z_{iLS} should satisfy:

$$If\,\{f \in [f_1,\, f_2]\} \;\rightarrow\; |\theta| < 90^0 \tag{3.6}$$

$$If\,\{f \notin [f_1,\, f_2]\} \;\rightarrow\; \varphi(Z_{iLS}) = \varphi(Z_{iL}) \tag{3.7}$$

where θ is the phase of Z_{iLS} during $[f_1,\, f_2]$.

According to (3.6) and (3.7), Z_{iLS} could be further expressed as

$$Z_{iLS} = \begin{cases} \left(V_{bus}^2/P_o\right) e^{j\theta} & f \in [f_1,\, f_2] \\ Z_{iL} & f \notin [f_1,\, f_2] \end{cases} \tag{3.8}$$

According to (3.1) and (3.8), in order to ensure $|Z_{iL}|$ successfully becomes $|Z_{iLS}|$ as shown in Fig. 3.1(b), Z_{SVI} can be selected as

$$\begin{aligned} Z_{SVI} &= Z_{iLS} - Z_{iL} = \begin{cases} \left(V_{bus}^2/P_o\right) e^{j\theta} - \left(-V_{bus}^2/P_o\right) & f \in [f_1,\, f_2] \\ Z_{iL} - Z_{iL} & f \notin [f_1,\, f_2] \end{cases} \\ &= \begin{cases} \left(V_{bus}^2/P_o\right) \cdot \left(1 + e^{j\theta}\right) & f \in [f_1,\, f_2] \\ 0 & f \notin [f_1,\, f_2] \end{cases} \end{aligned} \tag{3.9}$$

Table 3.1: Definitions of variables and transfer functions in load converter

$\hat{v}_{bus}$	Perturbation of the bus voltage
$\hat{i}_o$	Perturbation of the load current
$\hat{i}_{bus}$	Perturbation of the bus current
$\hat{d}$	Perturbation of the duty cycle
$\hat{v}_o$	Perturbation of the output voltage
$\hat{v}_{or}$	Perturbation of the output voltage reference
$G_v(s)$	Transfer function of the voltage regulator
$G_M(s)$	Transfer function of the modulator
$Z_{iOL}(s)$	Open-loop input impedance
$G_{vd}(s)$	Control to output voltage transfer function
$G_{id}(s)$	Control to input current transfer function
$Z_{oOL}(s)$	Open-loop output impedance
$H_s(s)$	Sampling coefficient of the output voltage
$G_{iOL}(s)$	Open-loop load to input current transfer function
$G_{vOL}(s)$	Open-loop input to output voltage transfer function

In summary, if the Z_{SVI}, which is expressed by (3.5), is added in the series with the load input impedance, the total separation between $|Z_{oS}|$ and $|Z_{iLS}|$ shown in Fig. 3.1(a) can be achieved. If the Z_{SVI}, which expressed by (3.9), is added in the series with the load input impedance, $|\varphi(Z_{oS}) - \varphi(Z_{iLS})| < 180^0$ within $[f_1, f_2]$ as shown in Fig. 3.1(b) can be ensured.

3.1.3 Derivation of the SVI Control Strategy

According to Section 3.1.1, with Z_{SVI}, the cascaded system can be stabilised by increasing $|Z_{iL}|$ or $\varphi(Z_{iL})$ in a very small frequency range to minimise the load compromise. Hence, in this section, a SVI control strategy for the load converter is proposed to realise Z_{SVI}.

First of all, the small signal block diagram of the original load converter is presented in Fig. 3.3. v_{bus} and i_{bus} are the input voltage and current of the load converter, respectively. v_o and i_o are the output voltage and current of the load converter, respectively. d is the duty cycle of the load converter. $Z_{iOL}(s)$, $G_{iOL}(s)$, $G_{id}(s)$, $G_{vOL}(s)$, $Z_{oOL}(s)$ and $G_{vd}(s)$ are the six basic open-loop transfer functions of the load converter. In addition, for the original load converter, a voltage closed-loop is utilised, where $H_s(s)$ and $G_v(s)$ are the sampling coefficient and voltage regulator transfer function of the output voltage, respectively; and $G_M(s)$ is the transfer function of the modulator. All the variables and transfer functions of Fig. 3.3 are described in Table 3.1.

$Z_{iL}(s)$ is the input impedance of the original load converter. Therefore, for the original

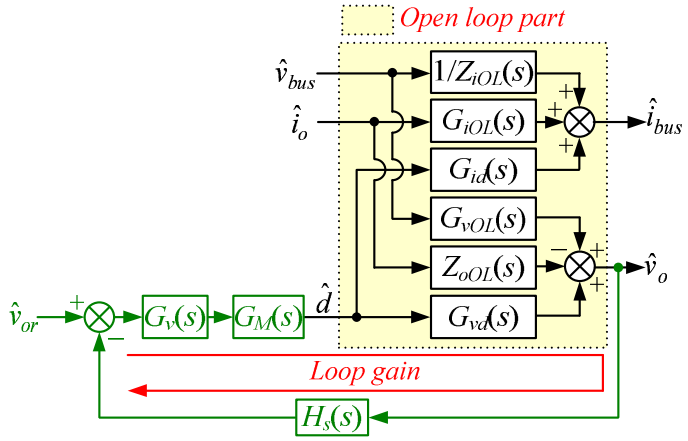


Figure 3.3: Small signal block diagram of the original load converter.

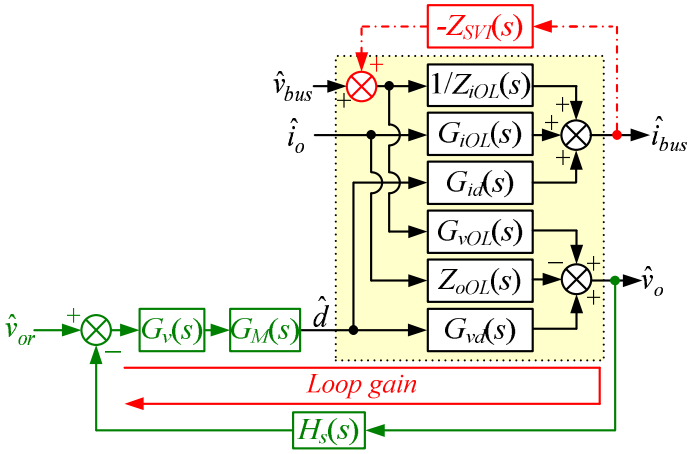


Figure 3.4: Small signal block diagram of the load converter with the paralleled virtual impedance.

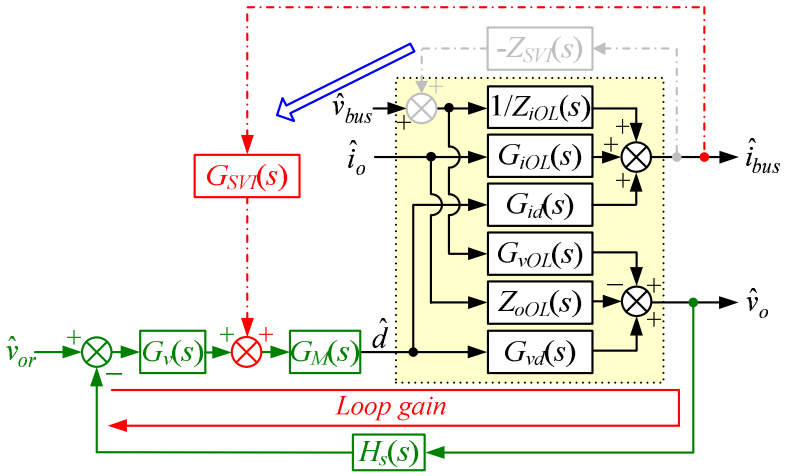


Figure 3.5: Derivation of the SVI control strategy.

load converter, its v_{bus} and i_{bus} have the following relationship:

$$v_{bus} = Z_{iL}(s) i_{bus} \tag{3.10}$$

If Z_{SVI} is added in the series with the input port of the load converter, the relationship between v_{bus} and i_{bus} is changed to:

$$v_{bus} - Z_{SVI}(s) i_{bus} = Z_{iL}(s) i_{bus} \tag{3.11}$$

As indicated by (3.11), the small signal block diagram of the load converter can be changed to Fig. 3.4.

Fig. 3.4 illustrates that $-Z_{SVI}$ is introduced to the control block between the v_{bus} and i_{bus} directly. From the small signal block diagram point of view, Fig. 3.4 achieves the purpose of adding Z_{SVI} to the series with the input port of the load converter. However, from the control point of view, this method cannot be realised directly. It is because that any converter is only controlled by its duty cycle. In order to address this issue, the output of $-Z_{SVI}$ is moved to the output voltage reference, with equivalent adjustments to the transfer function to $G_{SVI}(s)$, as shown with the Fig. 3.5.

Fig. 3.5 shows that when $G_{SVI}(s)$ is required to realise the series virtual impedance Z_{SVI}, the following relationship can be obtained:

$$\hat{i}_{bus} \cdot [-Z_{SVI}(s)] \cdot \frac{1}{Z_{iL}(s)} = \hat{i}_{bus} \cdot G_{SVI}(s) \cdot G_M(s) \cdot G_{id}(s) \cdot \frac{1}{1 + T_v(s)} \tag{3.12}$$

where $T_v(s) = H_s(s) G_v(s) G_M(s) G_{vd}(s)$ is the voltage loop gain of the load converter.

According to (3.12), the expression of $G_{SVI}(s)$ can be derived as:

$$\begin{aligned} G_{SVI}(s) &= -\frac{Z_{SVI}(s)}{Z_{iL}(s)} \cdot \frac{1 + T_v(s)}{G_M(s) \cdot G_{id}(s)} \\ &= Z_{SVI}(s) \cdot \frac{[1 + T_v(s)] \cdot P_o}{G_{id}(s) \cdot G_M(s) \cdot V_{bus}^2} \end{aligned} \tag{3.13}$$

Up to this point, Fig. 3.3 $\sim$ Fig. 3.5 represent the whole derivation process of the SVI control strategy, and $G_{SVI}(s)$ is the input-impedance-regulator of the SVI control strategy.

3.1.4 Realisation of the SVI Control Strategy

According to Section 3.1.3, $G_{SVI}(s)$ is the key point of the SVI control strategy. Therefore, methods of realising $G_{SVI}(s)$ are discussed in this section.

According to (3.5), (3.9) and Fig. 3.5, the expression of $G_{SVI}(s)$ can be derived in the following ways:

a) To achieve a total separation between $|Z_{oS}|$ and $|Z_{iLS}|$, $G_{SVI1}(s)$ is

$$G_{SVI1}(s) = \begin{cases} \left[\left(V_{bus}^2/P_o\right) - |Z_{iL1}|\right] \cdot \frac{[1+T_v(s)]\cdot P_o}{G_{id}(s)\cdot G_M(s)\cdot V_{bus}^2} & f \in [f_1,\, f_2] \\ 0 & f \notin [f_1,\, f_2] \end{cases} \tag{3.14}$$

b) To ensure $|\varphi(Z_{oS}) - \varphi(Z_{iLS})| < 180^0$ at f_1 and f_2, $G_{SVI2}(s)$ is

$$G_{SVI2}(s) = \begin{cases} \left(V_{bus}'^2/P_o\right) \cdot \left(1+e^{j\theta}\right) \cdot \frac{[1+T_v(s)]\cdot P_o}{G_{id}(s)\cdot G_M(s)\cdot V_{bus}^2} & f \in [f_1,\, f_2] \\ 0 & f \notin [f_1,\, f_2] \end{cases} \tag{3.15}$$

According to (3.14) and (3.15), $G_{SVI}(s)$ is a frequency-based piecewise transfer function, where $|G_{SVI}(s)| > 0$ within $[f_1,\, f_2]$ and $|G_{PVI}(s)| = 0$ outside $[f_1,\, f_2]$ as shown in Fig. 3.6. Hence, a band-pass filter $G_{BPF}(s)$ can be utilised to help achieve $G_{SVI}(s)$, i.e., (3.14) and (3.15) can be re-expressed as (3.16) and (3.17), respectively.

$$G_{SVI1}(s) = \left[\left(V_{bus}'^2/P_o\right) - |Z_{iL1}|\right] \cdot \frac{[1+T_v(s)]\cdot P_o}{G_{id}(s)\cdot G_M(s)\cdot V_{bus}^2} \cdot G_{BPF}(s) \tag{3.16}$$

$$G_{SVI2}(s) = \left(V_{bus}'^2/P_o\right) \cdot \left(1+e^{j\theta}\right) \cdot \frac{[1+T_v(s)]\cdot P_o}{G_{id}(s)\cdot G_M(s)\cdot V_{bus}^2} \cdot G_{BPF}(s) \tag{3.17}$$

where $G_{BPF}(s)$ adopts a typical second order band-pass filter, which is composed of a second order high-pass filter and a second order low-pass filter, given as

$$G_{BPF}(s) = \frac{s^2}{s^2 + (2\pi f_1/Q_H)s + (2\pi f_1)^2} \cdot \frac{(2\pi f_2)^2}{s^2 + (2\pi f_2/Q_L)s + (2\pi f_2)^2} \tag{3.18}$$

where Q_H and Q_L are quality factors of the high-pass and low-pass filter, respectively.

According to (3.16) and (3.17), $G_{SVI}(s)$ can be easily realised by digital control chips, such as a digital signal processor (DSP), field programmable gate array (FPGA) and micro-

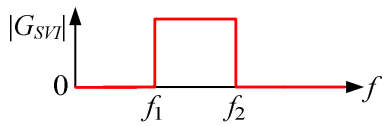


Figure 3.6: Characteristic of $|G_{SVI}(s)|$.

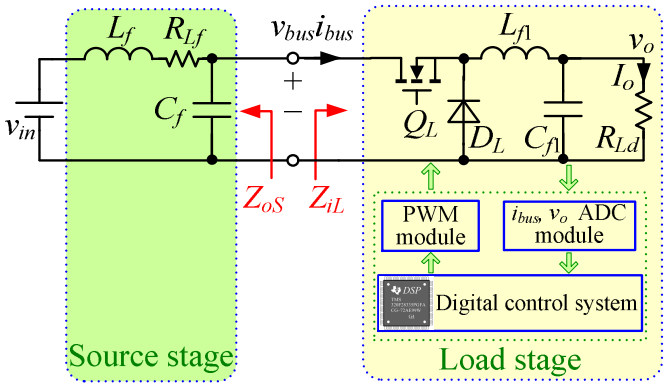


Figure 3.7: The System I.

controller unit (MCU).

3.2 Design Example

As discussed in Chapter 1, the worst instability phenomena are most likely to occur when the source converter is a *LC* input filter. As Buck and Boost converters are two typical DC/DC converters, a 100 W cascaded system, which consists of a *LC* input filter and a 48 V - 12 V Buck converter, and a 200 W cascaded system, which includes a *LC* input filter and a 24 V - 48 V Boost converter, are designed in this section.

3.2.1 System I — a Buck Converter with a *LC* Input Filter

A 100 W cascaded system with a *LC* input filter (source stage) and a 48 V - 12 V Buck converter (load stage) is designed, which is shown in Fig. 3.7. The Buck converter is operated at 100 kHz. The cut-off frequency and phase margin of the voltage close loop of the Buck converter are set to 20 kHz and 45^o, respectively. The corresponding system parameters are summarised in Table 3.2.

The output impedance Z_{oS} of the *LC* input filter is given in (3.19), where R_{Lf} is the parasitic resistor of L_f and the measured value is $0.1\,\Omega$. According to the small-signal

Table 3.2: Parameters of the System I

Parameter	L_f	C_f	L_{f1}	C_{f1}	R_{Ld}
Value	700 μH	68 μF	33 μH	2400 μF	1.44Ω

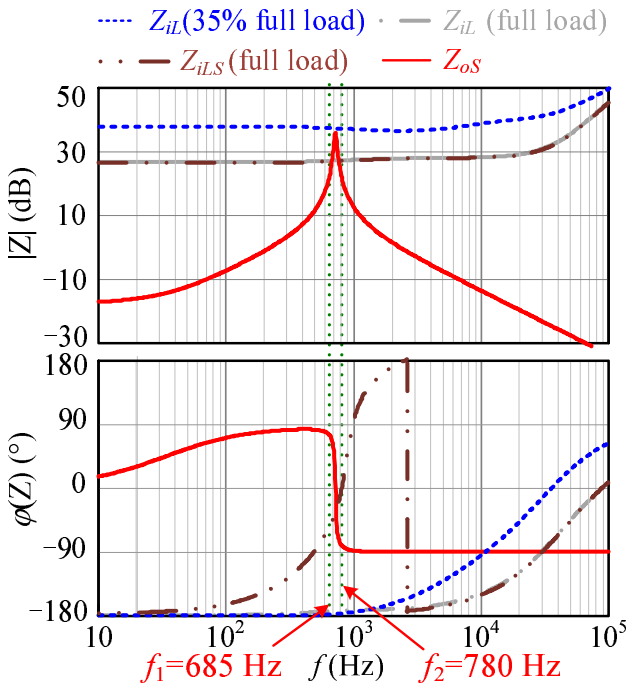


Figure 3.8: Bode plots of Z_{oS} and Z_{iL} of the System I.

circuit model of the Buck converter (Cuk, 1976), the input impedance Z_{iL} of the Buck converter can be expressed as (3.20).

$$Z_{oS}(s) = \frac{sL_f + R_{Lf}}{s^2 L_f C_f + sR_{Lf} C_f + 1} \tag{3.19}$$

$$Z_{iL}(s) = \left[\frac{1}{1+T_v(s)} \cdot \frac{sC_{f1}D^2 + \frac{D^2}{R_{Ld}}}{s^2 L_{f1} C_{f1} + s\frac{L_{f1}}{R_{Ld}} + 1} - \frac{T_v(s)}{1+T_v(s)} \cdot \frac{P_o}{V_{bus}^2} \right]^{-1} \tag{3.20}$$

where P_o and D are the output power and the duty cycle of the Buck converter, respectively.

Fig. 3.8 shows the Bode plots of Z_{oS} and Z_{iL} in the example system: when the load is lower than 35% full-load, the cascaded system is stable; otherwise, the cascaded system is unstable and the oscillation occurs at approximately 685 Hz theoretically (Wildrick, 1993).

To solve the instability problem conveniently, Z_{iL} is designed as a positive resistor within $[f_1,\ f_2]$ to ensure $|\varphi(Z_{oS}) - \varphi(Z_{iLS})| < 180^0$, i.e., θ is set to 0 at (3.17). By the

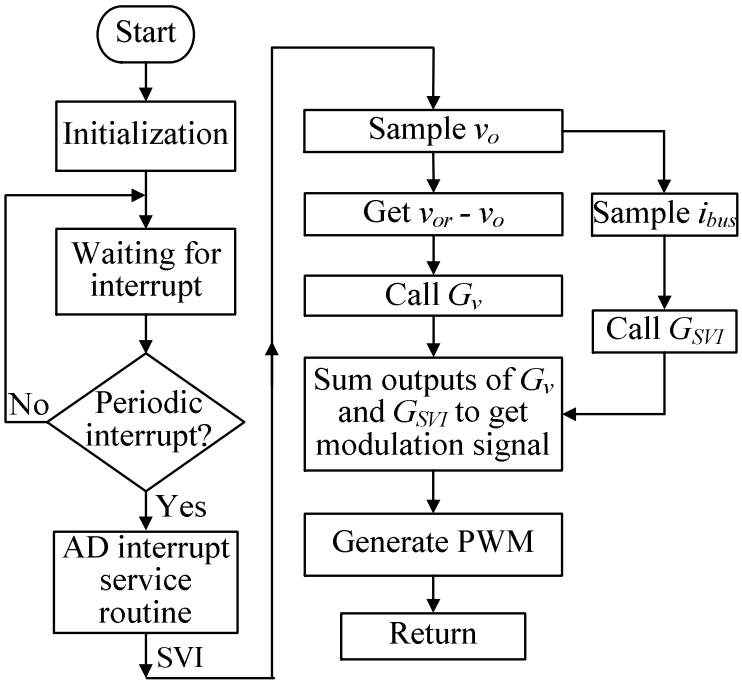


Figure 3.9: Software flowchart of the SVI control strategy.

small signal model of the Buck converter (Cuk, 1976) and (3.17), the expression of $G_{SVI}(s)$ can be derived as

$$G_{SVI}(s) = G_{SVI1}(s) \cdot G_{BPF}(s) \tag{3.21}$$

where

$$G_{SVI1}(s) \approx \left(1 - \frac{1 + sR_{Ld}C_{f1}}{s^2 L_{f1}C_{f1} + s\left(R_{Ld}C_{f1} + L_{f1}/R_{Ld}\right) + 2}\right) \cdot \frac{2V_M R_{Ld}}{V_{bus}D} \tag{3.22}$$

here, in $G_{BPF}(s)$, $f_1 = 685\,Hz$ and $f_2 = 780\,Hz$; $Q_H = 0.707$ and $Q_L = 0.707$.

The Bode plot of the modified input impedance, Z_{iLS}, is shown with double dotted-dashed line in Fig. 3.8, with $|\varphi(Z_{oS}) - \varphi(Z_{iLS})| < 180^0$ at f_1 and f_2. Therefore, the cascaded system will be stable and the design of $G_{SVI}(s)$ is appropriate.

As the SVI control strategy is realised by a DSP TMS320F28335 in practice, its software flowchart is presented in Fig. 3.9. The input current i_{bus} and the output voltage v_o of the load converter are sampled to provide the necessary information for the SVI control strategy and output voltage regulation. The algorithm obtained the modulation signal by adding the output of $G_{SVI}(s)$ to the output of $G_v(s)$. It then generated the PWM signal by

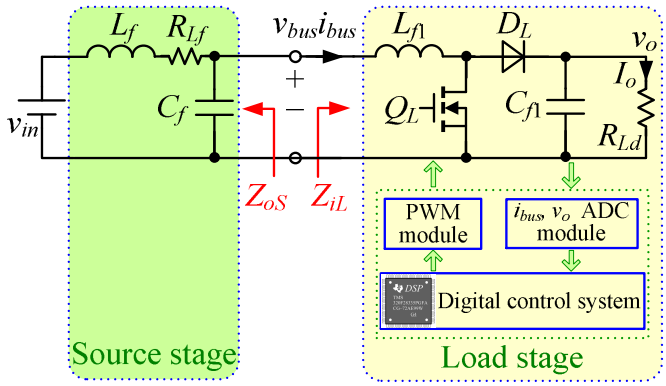


Figure 3.10: The System II.

Table 3.3: Parameters of the System II

Parameter	L_f	C_f	L_{f1}	C_{f1}	R_{Ld}
Value	250 μH	330 μF	720 μH	450 μF	11.52 Ω

PWM module.

3.2.2 System II — a Boost Converter with a *LC* Input Filter

Fig. 3.10 shows a 200 W cascaded system consisting of a *LC* input filter (source stage) and a 24 V - 48 V Boost converter (load stage) operated at 100 kHz. Since the Boost converter is a non-minimum phase system, a proportional–integral (PI) controller is employed as the compensator and the cut-off frequency and phase margin of the voltage closed loop of the Boost converter are set to 2.5 kHz and 32^o, respectively. The corresponding system parameters are summarised in Table 3.3.

The output impedance Z_{oS} of the *LC* input filter is given in (3.19), and is threrefore not repeated here. According to the small-signal circuit model of the Boost converter (Cuk, 1976), the input impedance Z_{iL} of the Boost converter can be expressed as (3.23).

$$Z_{iL}(s) = \left[\frac{1}{1+T_v(s)} \cdot \frac{sC_{f1}R_{Ld}+1}{s^2L_{f1}C_{f1}R_{Ld}+sL_{f1}+R_{Ld}(1-D)^2} - \frac{T_v(s)}{1+T_v(s)} \cdot \frac{P_o}{V_{bus}^2} \right]^{-1} \tag{3.23}$$

where D and P_o are the duty cycle and output power of the Boost converter, respectively.

Fig. 3.11 shows the Bode plots of Z_{oS} and Z_{iL} in the example system: when the load is lower than 20% full-load, the cascaded system is stable; otherwise, the cascaded system is

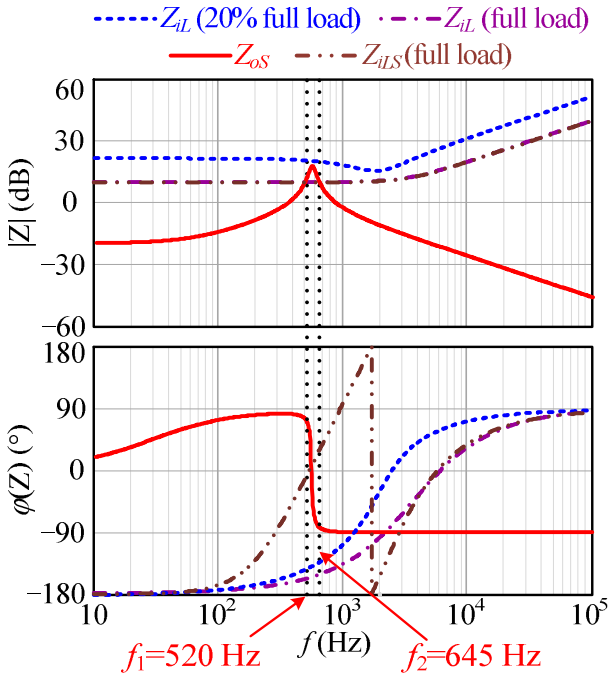


Figure 3.11: Bode plots of Z_{oS} and Z_{iL} of the System II.

unstable and the oscillation occurs at approximately 520 Hz theoretically (Wildrick, 1993).

In order to conveniently solve the instability problem, Z_{iL} is designed as a positive resistor within $[f_1,\ f_2]$ to ensure $|\varphi(Z_{oS}) - \varphi(Z_{iLS})| < 180^0$, i.e., θ is set to 0 at (3.17). According to the small signal model of Boost converter (Cuk, 1976) and (3.17), the expression of $G_{SVI}(s)$ can then be derived as

$$G_{SVI}(s) \approx G_{SVI1}(s) \cdot G_{BPF}(s) \tag{3.24}$$

where

$$G_{SVI1}(s) = \frac{2V_M[s^2 L_{f1} C_{f1} R_{Ld} + sL_{f1} + R_{Ld}(1-D)^2]}{v_o(sC_{f1}R_{Ld} + 2)} \tag{3.25}$$

Also, for $G_{BPF}(s)$, f_1 = 520 Hz and f_2 = 645 Hz, $Q_H = Q_L = 0.707$.

The Bode plot of the modified input impedance, Z_{iLS}, is represented by a double dotted-dashed line in Fig. 3.11, with $|\varphi(Z_{oS}) - \varphi(Z_{iLS})| < 180^0$ at f_1 and f_2. Therefore, the improved cascaded system is stable and the design of $G_{SVI}(s)$ is appropriate.

In practice, the Boost converter is also controlled by DSP TMS320F28335, and its SVI control strategy can be realised by the software flowchart in Fig. 3.9. Since the flowchart

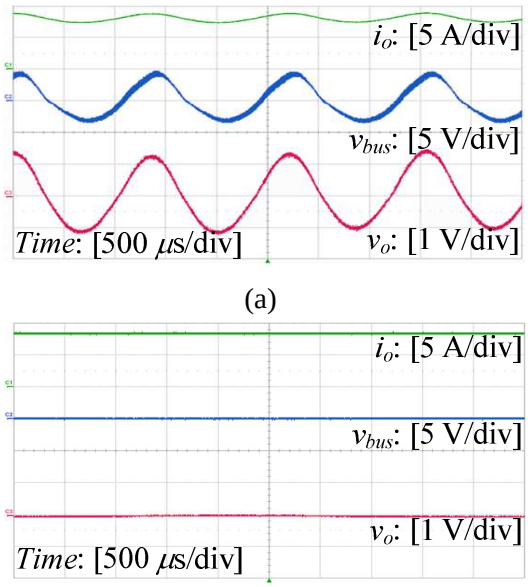


Figure 3.12: Experimental waveforms of the System I at full load: (a) without SVI control strategy, (b) with SVI control strategy.

has already been explained in Section 3.2.1, it is not repeated here.

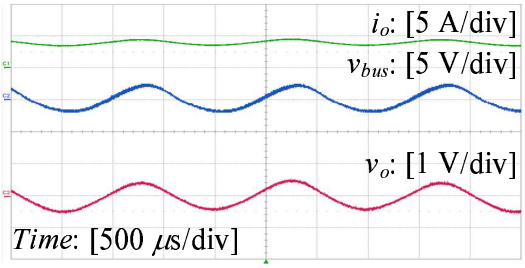
3.3 Experimental Verification

According to the design examples, two experimental systems have been fabricated and tested in the lab to verify the validity of the SVI control strategy.

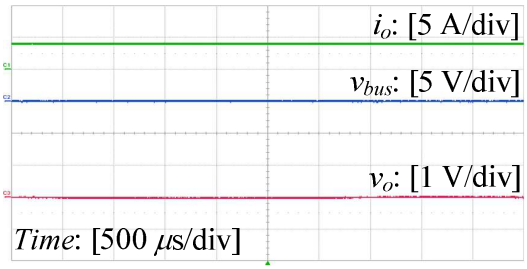
3.3.1 System I — a Buck Converter with a *LC* Input Filter

System I is a 100 W cascaded system consisting of a *LC* input filter and a 48 V - 12 V digital-controlled Buck converter. Its topology, parameters and control algorithm are presented in Fig. 3.7, Table 3.2 and Fig. 3.9, respectively.

The experimental results of System I with/without the SVI control strategy at different loads are given in Figs. 3.12 to 3.14 respectively, where the waveforms of v_{bus} and v_o are their ac components to clearly show the oscillation. As seen in Figs. 3.12(a) and 3.13(a), System I is unstable at full load and half load when the SVI control strategy is absent, and the oscillating frequencies of the bus voltage and output voltage are both about 685 Hz, which concurs with the conclusion at Fig. 3.8. As shown in Fig. 3.12(b) and Fig. 3.13(b),



(a)



(b)

Figure 3.13: Experimental waveforms of the System I at half load: (a) without SVI control strategy, (b) with SVI control strategy.

when the SVI control strategy is incorporated, System I becomes stable at full load and half load, and no oscillation occurs in v_{bus} and v_o. Fig. 3.14(a) shows the experimental waveforms of i_o, v_{bus} and v_o at 35% full-load without the SVI control strategy. This shows that System I is stable, which is consistent with Fig. 3.8. As shown in Fig. 3.14(b), System I is also stable at 35% full-load when SVI control strategy is utilised.

Fig. 3.15(a) shows the dynamic performance of System I when its load steps between 10% and 100% full-load at the rated input voltage (48 V). It shows that the dynamic performance of System I with SVI control strategy is good. Fig. 3.15(b) shows the dynamic performance of System I when its input voltage steps between 80% (38.4 V) and 120% (57.6 V) rated voltage at full load; and shows that the dynamic performance of System I with SVI control strategy is also good.

3.3.2 System II — a Boost Converter with a *LC* Input Filter

A 200 W cascaded system with a *LC* input filter and a 24 V - 48 V digital-control-based Boost converter is fabricated. Its topology, parameters and control algorithm are described in Fig. 3.10, Table 3.3 and Fig. 3.9, respectively.

The experimental results of System II with/without the SVI control strategy at different

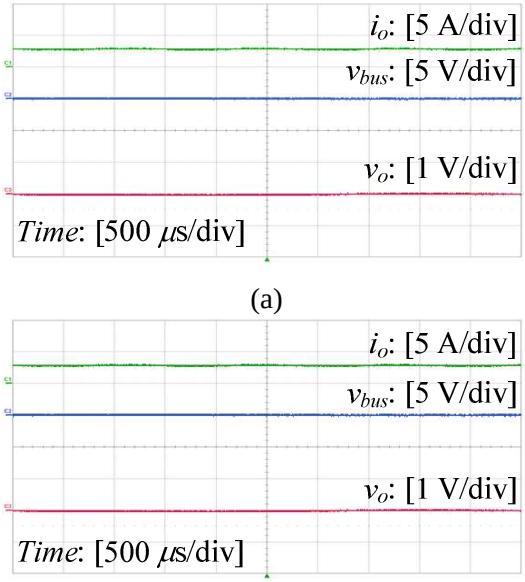


Figure 3.14: Experimental waveforms of the System I at light load: (a) without SVI control strategy, (b) with SVI control strategy.

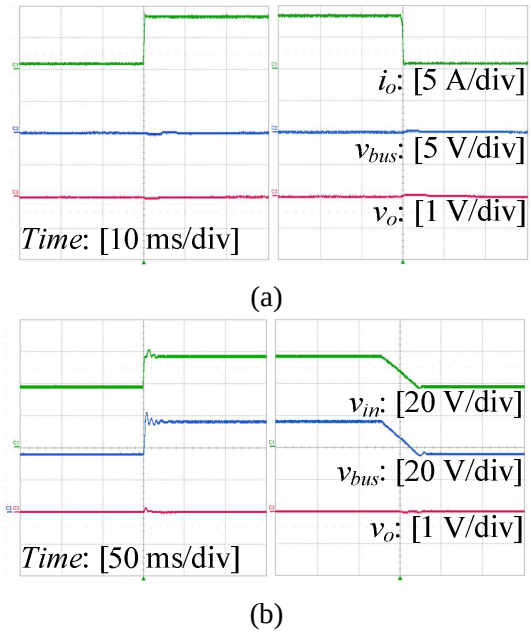


Figure 3.15: Dynamic experimental waveforms of the System I with SVI control strategy: (a) load changing between 10% load and 100% load, (b) input voltage changing between 80% rated voltage and 120% rated voltage.

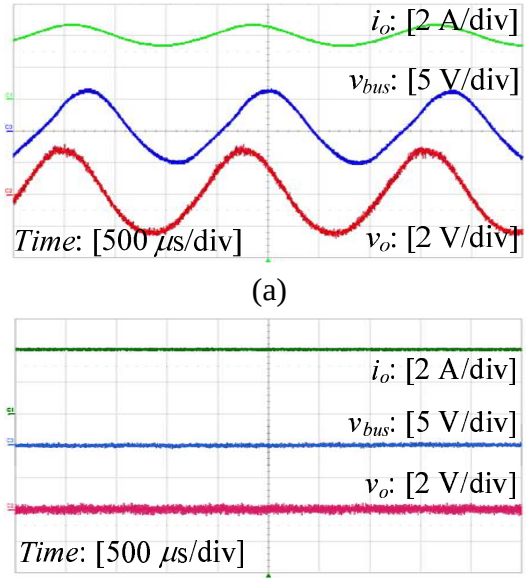


Figure 3.16: Experimental waveforms of the System II at full load: (a) without SVI control strategy, (b) with SVI control strategy.

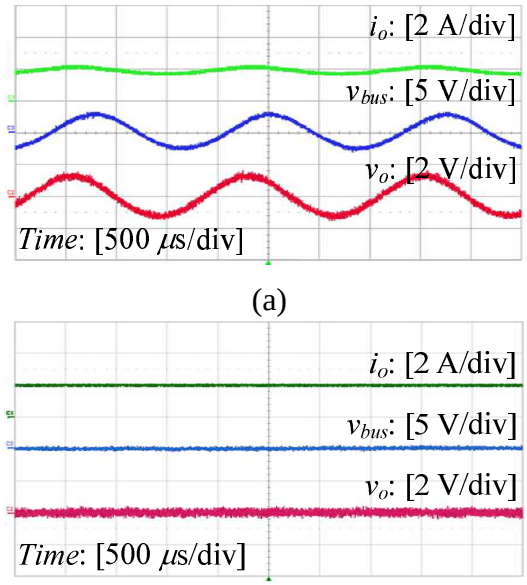
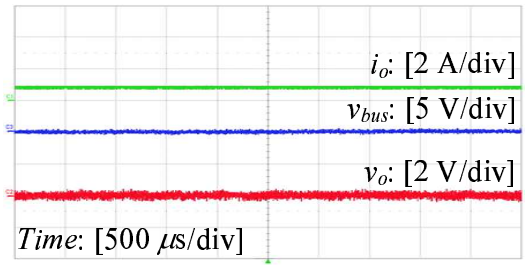
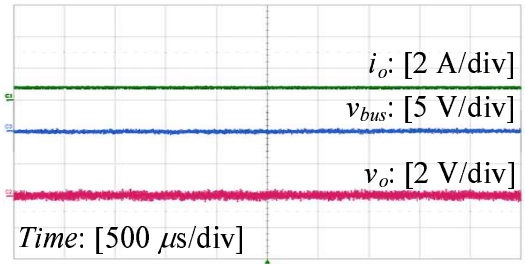


Figure 3.17: Experimental waveforms of the System II at half load: (a) without SVI control strategy, (b) with SVI control strategy.



(a)



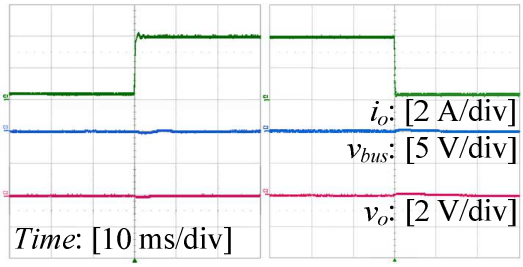
(b)

Figure 3.18: Experimental waveforms of the System II at light load: (a) without SVI control strategy, (b) with SVI control strategy.

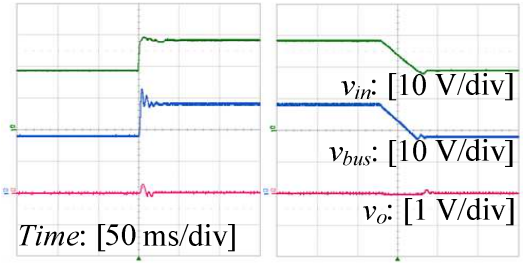
loads are given in Figs. 3.16 to 3.18, where the waveforms of v_{bus} and v_o are their ac components to clearly show the oscillation. As seen in Figs. 3.16(a) and 3.17(a), System II is unstable at full load and half load when the SVI control strategy is absent, and the oscillating frequencies of the bus voltage and output voltage are both approximately 520 Hz, which concurs with the conclusion in Fig. 3.11. As shown in Fig. 3.16(b) and Fig. 3.17(b), when the SVI control strategy is incorporated, System II becomes stable at full load and half load, and no oscillation occurs in v_{bus} and v_o. Fig. 3.18(a) shows the experimental waveforms of i_o, v_{bus} and v_o at 20% full-load without the SVI control strategy. System II is stable, which is consistent with Fig. 3.11. In addition, as shown in Fig. 3.18(b), System II is stable at 20% full-load when the SVI control strategy is utilised.

Fig. 3.19(a) shows the dynamic waveforms of System II when its load steps between 10% and 100% full-load at the rated input voltage (24 V). The dynamic performance of System II with SVI control strategy is good. Fig. 3.19(b) shows the dynamic performance of System II with the input voltage steps between 80% (19.2 V) and 120% (28.8 V) rated voltage at full load. It is also indicated that, the dynamic performance of System II with SVI control strategy is good.

The above two examples indicate that the SVI control strategy is effective and feasible



(a)



(b)

Figure 3.19: Dynamic experimental waveforms of the System II with SVI control strategy: (a) load changing between 10% load and 100% load, (b) input voltage changing between 80% rated voltage and 120% rated voltage.

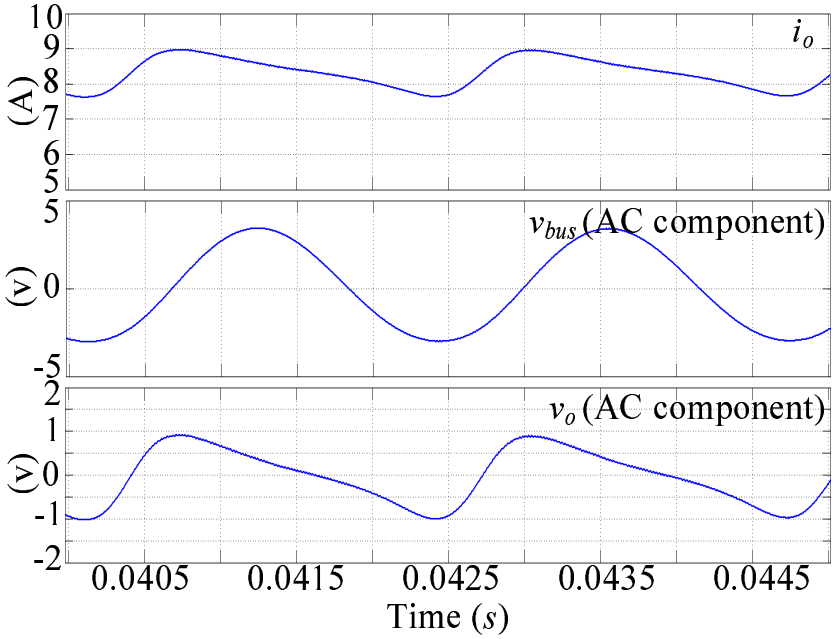
in practice.

3.4 Simulation Verification

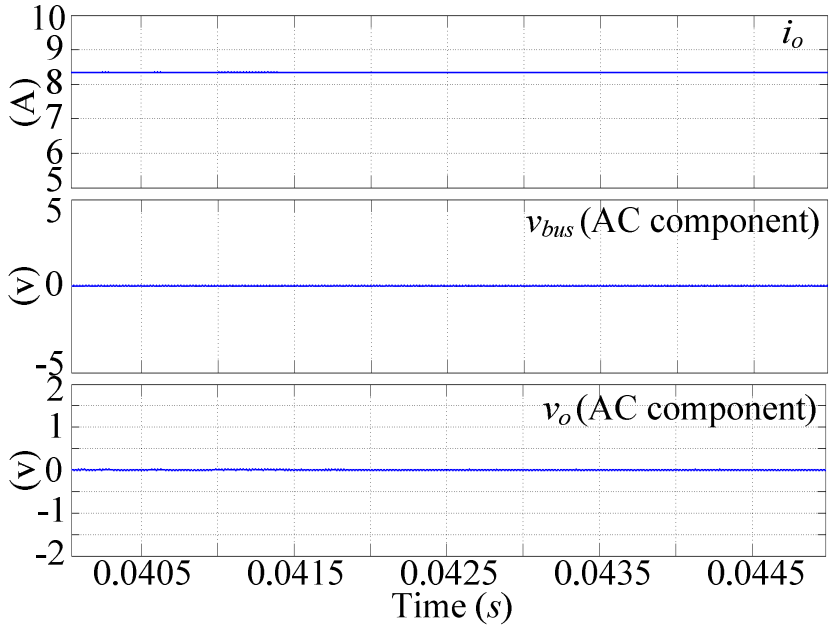
3.4.1 Simulation Verification of System I with the Consideration of the Load Input Capacitor

The input capacitor is usually a necessary component of DC/DC converters in practice. Therefore, a simulink model which adds a 110 μF input capacitor to the Buck converter of Fig. 3.7 has been built in Matlab to verify the accuracy of the SVI control strategy.

The simulation results of System I with consideration for the load input capacitor at different loads are given in Figs. 3.20 to 3.22. Similar to the above experimental results, the simulation waveforms of v_{bus} and v_o are also their ac components to clearly show the oscillation. As seen in Figs. 3.20(a) and 3.21(a), System I is unstable at full load and half load when the SVI control strategy is absent. As shown in Fig. 3.20(b) and Fig. 3.21(b), when the SVI control strategy is incorporated, System I becomes stable at full load and half load, and no oscillation occurs in v_{bus} and v_o. Fig. 3.22(a) shows the simulation waveforms

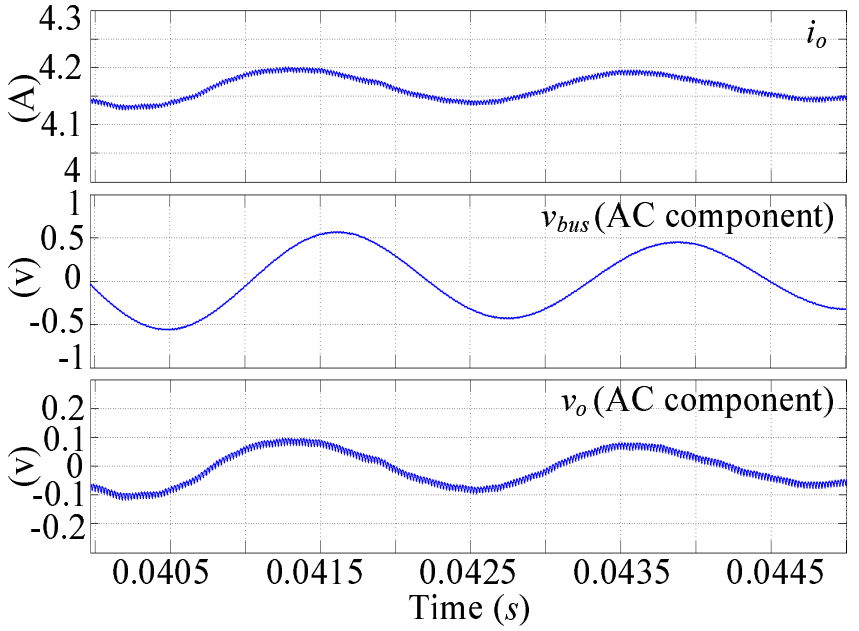


(a)

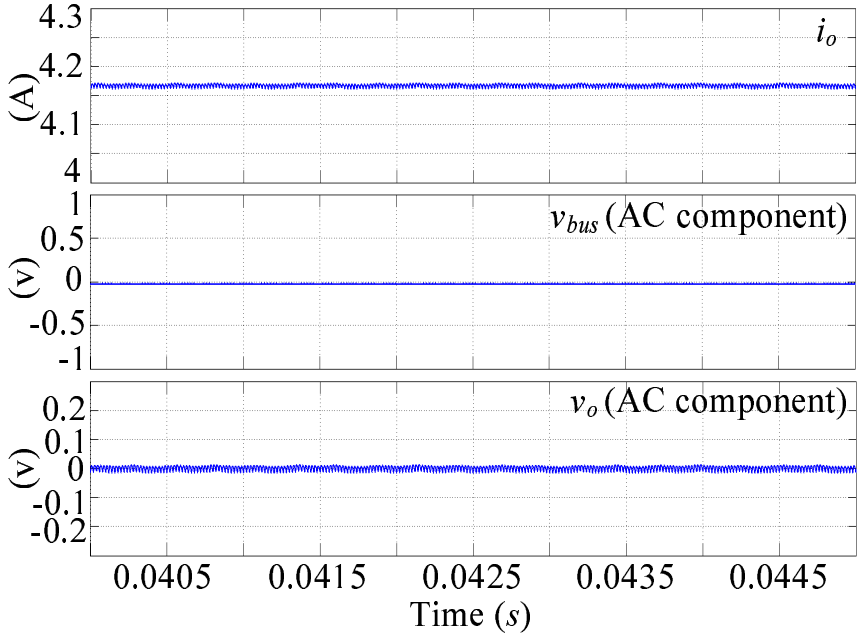


(b)

Figure 3.20: Simulation waveforms of the System I with the added load input capacitor at full load: (a) without SVI control strategy, (b) with SVI control strategy.



(a)



(b)

Figure 3.21: Simulation waveforms of the System I with the added load input capacitor at half load: (a) without SVI control strategy, (b) with SVI control strategy.

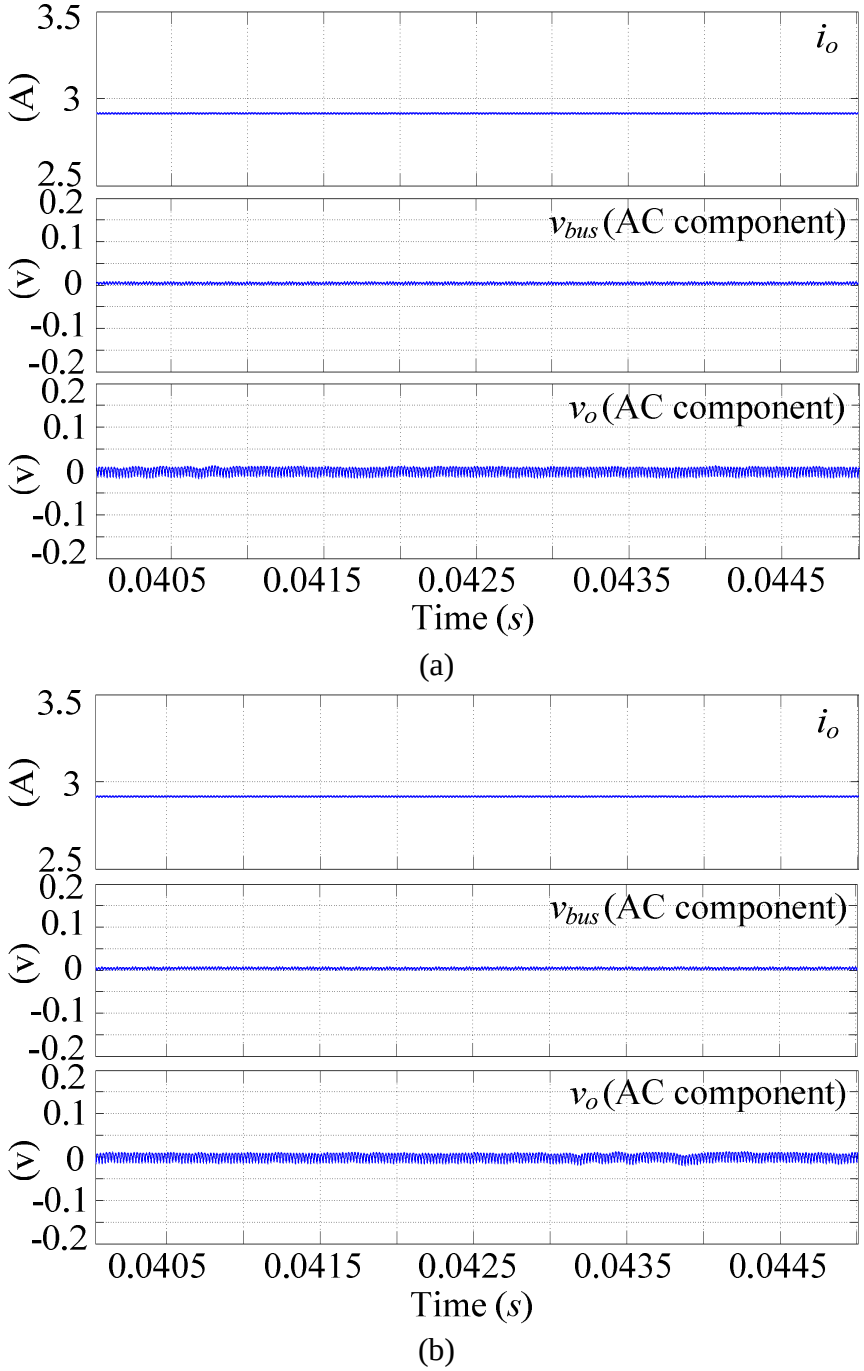


Figure 3.22: Simulation waveforms of the System I with the added load input capacitor at light load: (a) without SVI control strategy, (b) with SVI control strategy.

of i_o, v_{bus} and v_o at 35% full-load without the SVI control strategy. It shows that System I is stable. In addition, as shown in Fig. 3.22(b), System I is also stable at 35% full-load when the SVI control strategy is utilised. It is worth pointing out that, thanks to the added input capacitor, the oscillation waveforms in Figs. 3.20(a) and 3.21(a) are smaller than those in Figs. 3.12(a) and 3.13(a).

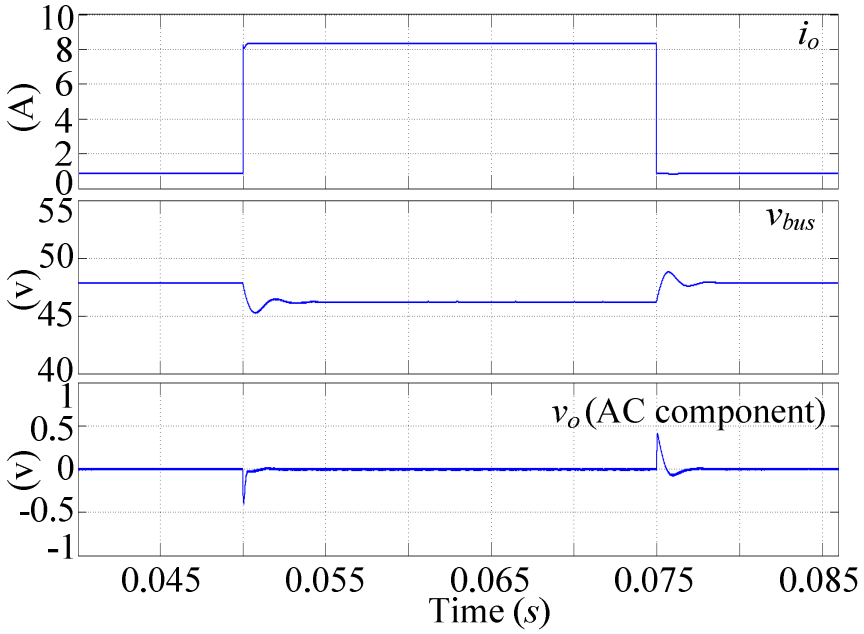
Fig. 3.23(a) shows the load dynamic performance of System I with the SVI control strategy and added load input capacitor. It shows that with the load steps between 10% and 100% full-load at the rated input voltage (48 V), the dynamic performance of System I is good. Fig. 3.23(b) shows the input voltage dynamic performance of System I with the SVI control strategy and the added load input capacitor. It also shows that with the input voltage steps between 80% (38.4 V) and 120% (57.6 V) rated voltage at full load, the dynamic performance of System I is also good.

3.4.2 Simulation Verification of System II with the Consideration of the Load Input Capacitor

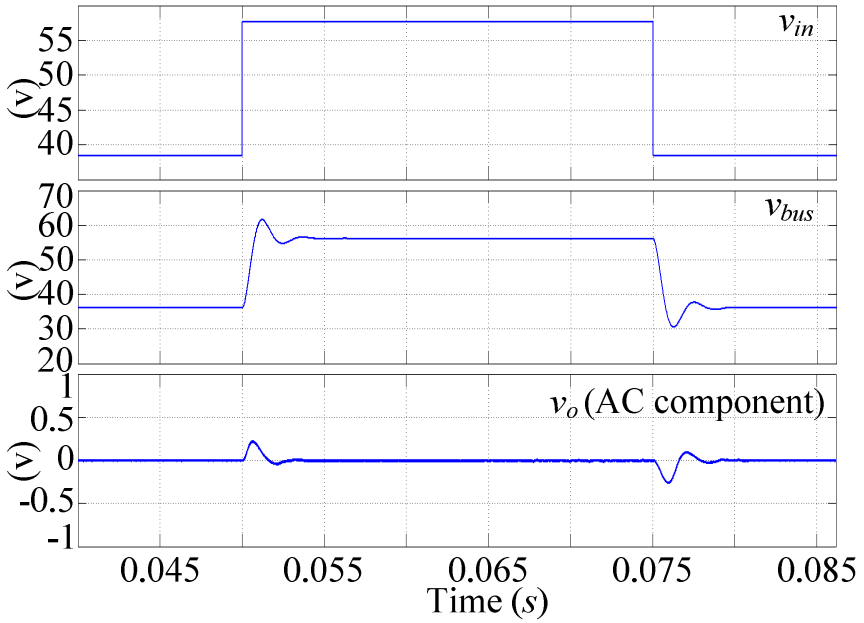
Similar to Section 3.4.1, a simulink model adding a 110 μF input capacitor to the Boost converter of Fig. 2.10 has been built in Matlab to verify the accuracy of the SVI control strategy.

The simulation results of System II with consideration for the load input capacitor at different loads are given in Figs. 3.24 to 3.26. Similar to the above experimental results, the simulation waveforms of v_{bus} and v_o are also their ac components to clearly show the oscillation. As seen from Figs. 3.24(a) and 3.25(a), System II is unstable at full load and half load when the SVI control strategy is absent. As illustrated by Fig. 3.24(b) and Fig. 3.25(b), when the SVI control strategy is incorporated, System II becomes stable at full load and half load, and no oscillation occurs in v_{bus} and v_o. Fig. 3.26(a) shows the simulation waveforms of i_o, v_{bus} and v_o at 20% full-load without the SVI control strategy. It shows that System II is stable. In addition, as shown in Fig. 3.26(b), System II is also stable at 20% full-load when the SVI control strategy is utilised. It is worth pointing out that, thanks to the added input capacitor, the oscillation waveforms in Figs. 3.24(a) and 3.25(a) are smaller than those in Figs. 3.16(a) and 3.17(a).

Fig. 3.27(a) shows the load dynamic waveforms of System II with the SVI control



(a)



(b)

Figure 3.23: Dynamic simulation waveforms of the System I with SVI control strategy and the added load input capacitor: (a) load changing between 10% load and 100% load, (b) input voltage changing between 80% rated voltage and 120% rated voltage.

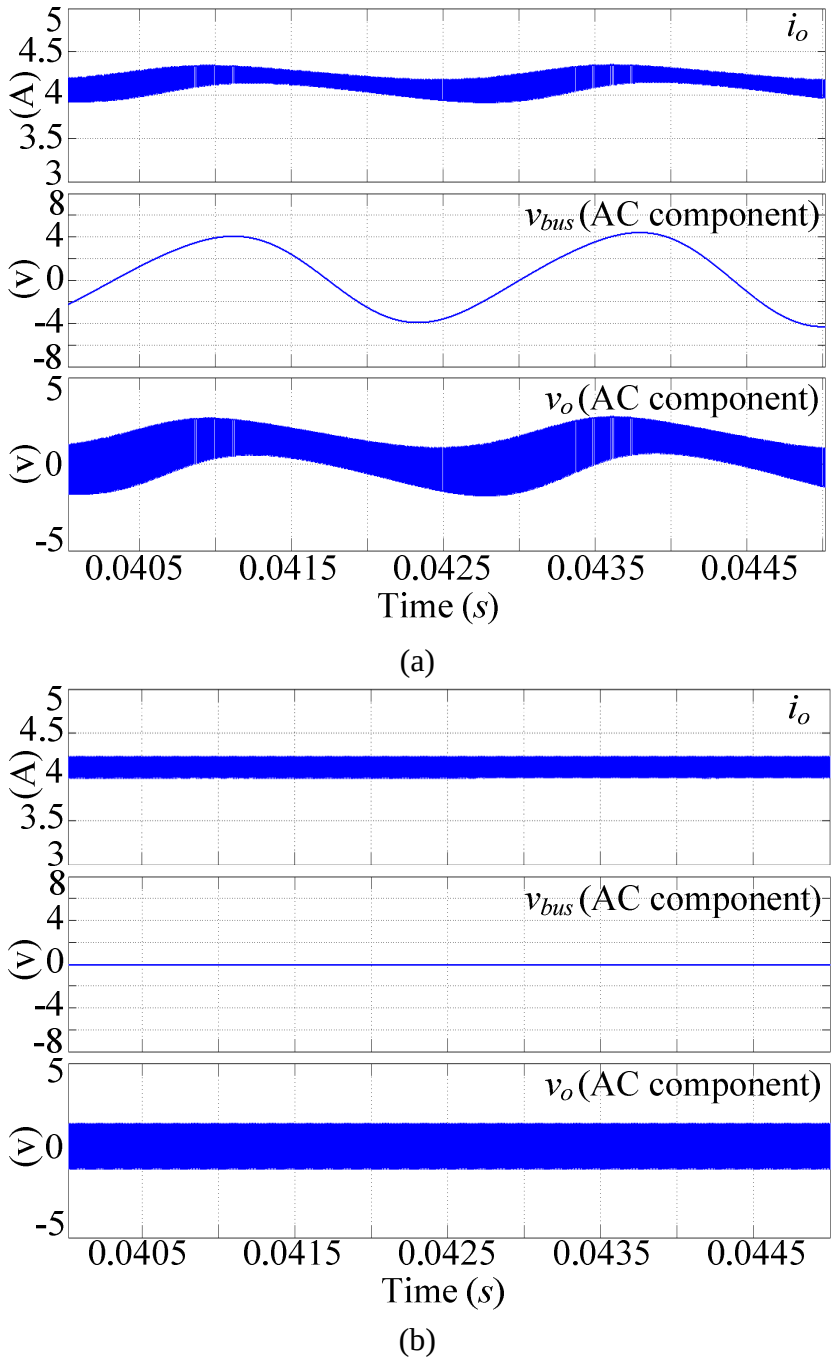
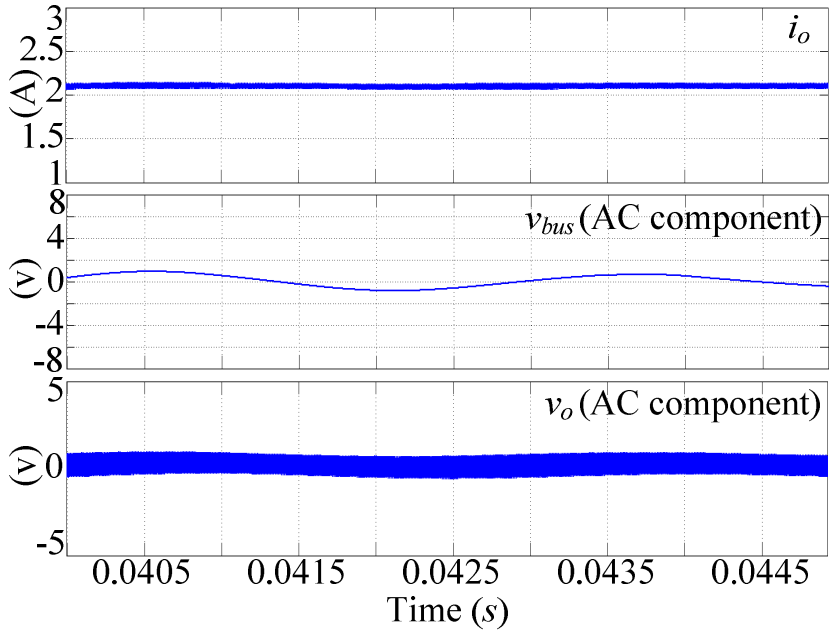
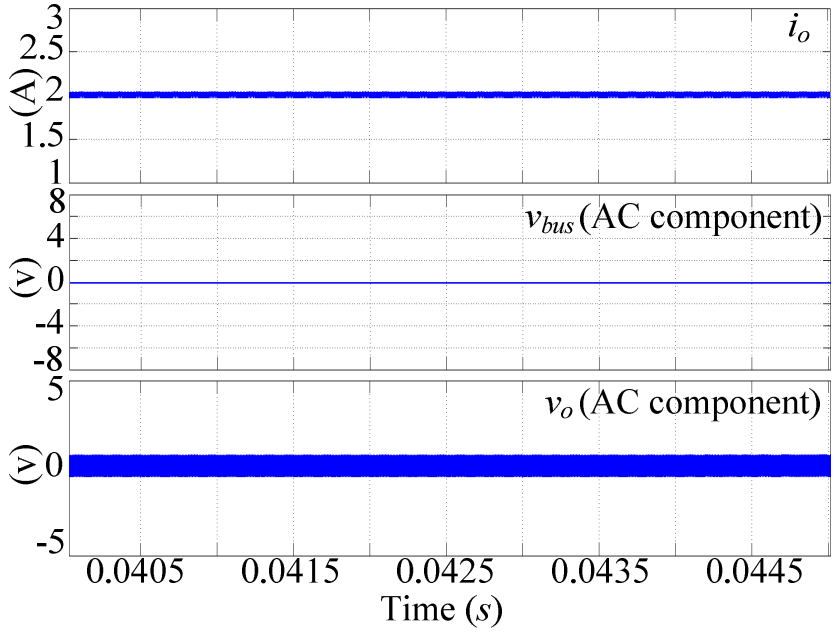


Figure 3.24: Simulation waveforms of the System II with the added load input capacitor at full load: (a) without SVI control strategy, (b) with SVI control strategy.



(a)



(b)

Figure 3.25: Simulation waveforms of the System II with the added load input capacitor at half load: (a) without SVI control strategy, (b) with SVI control strategy.

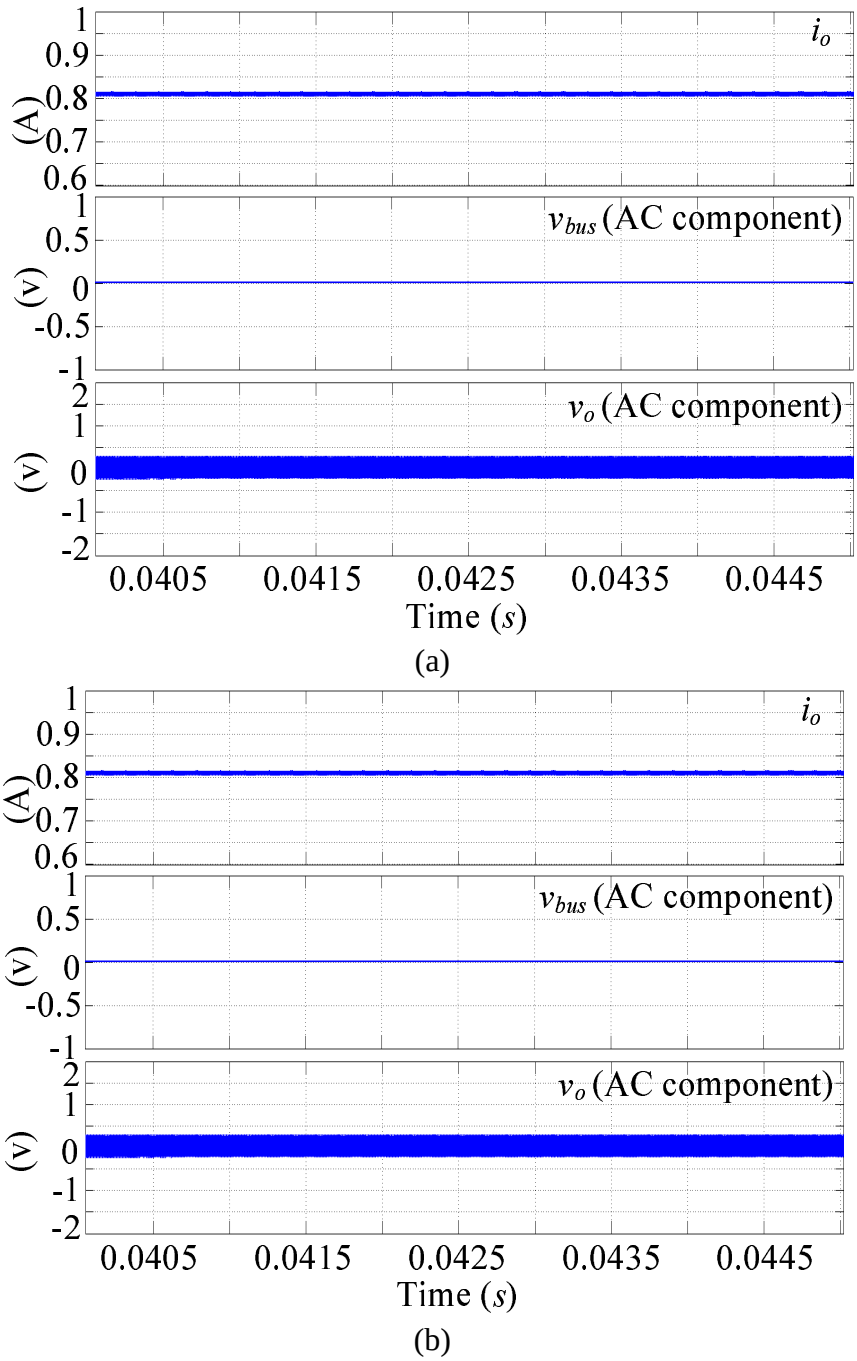
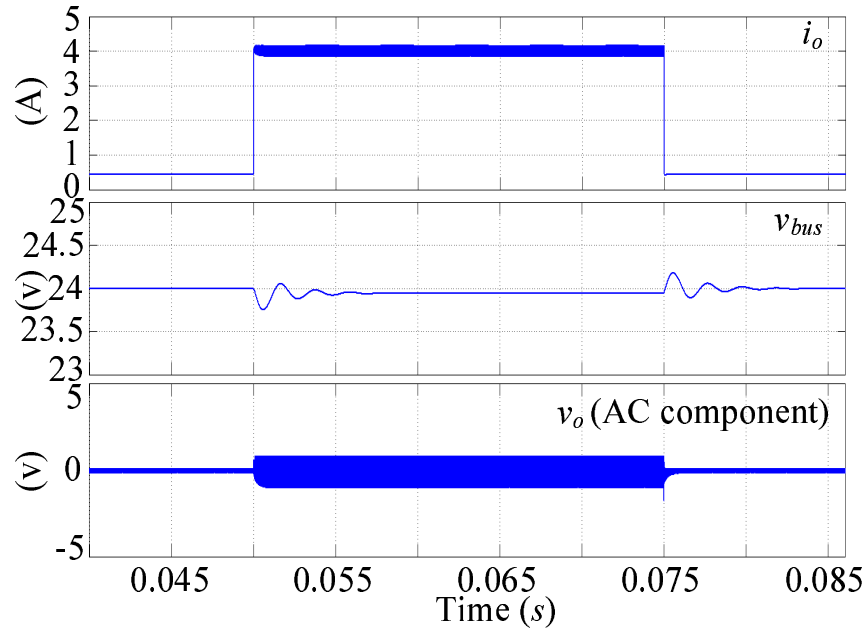
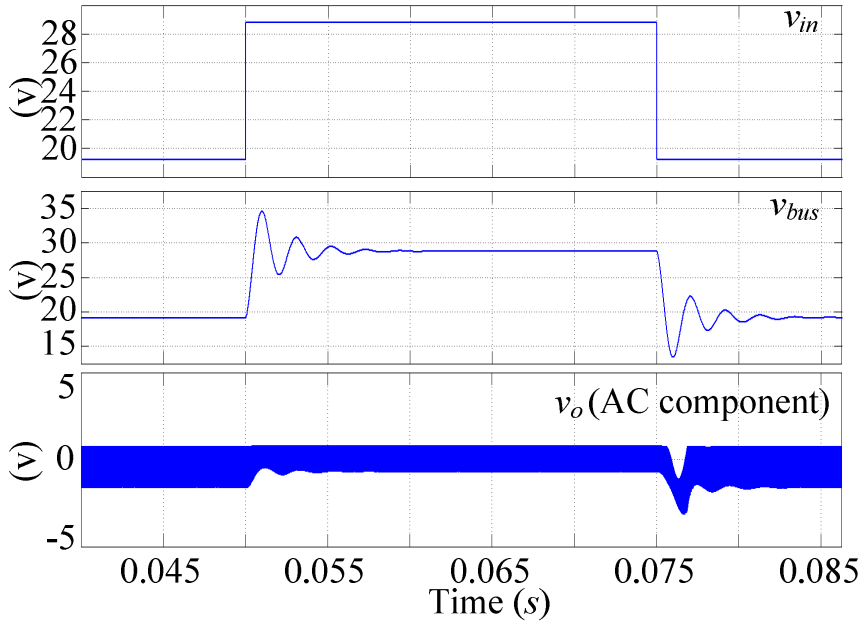


Figure 3.26: Simulation waveforms of the System II with the added load input capacitor at light load: (a) without SVI control strategy, (b) with SVI control strategy.



(a)



(b)

Figure 3.27: Dynamic simulation waveforms of the System II with SVI control strategy and the added load input capacitor: (a) load changing between 10% load and 100% load, (b) input voltage changing between 80% rated voltage and 120% rated voltage.

strategy and the added load input capacitor. It shows that with the load steps between 10% and 100% full-load at the rated input voltage (24 V), the dynamic performance of System II is good. Fig. 3.27(b) shows the input voltage dynamic performance of System II with the SVI control strategy and the added load input capacitor. It also shows that with the input voltage steps between 80% (19.2 V) and 120% (28.8 V) rated voltage at full load, the dynamic performance of System II is also good.

The above simulation results indicate that the SVI control strategy is also effective and feasible when the load converter contains the input capacitor.

3.5 Summary

Based on the idea of the PVI control strategy, another load stabilisation method is proposed in this chapter: the SVI control strategy. The SVI control strategy adds a virtual impedance in the series with the load converter to modify the input impedance in a very small frequency range. As a result, it can not only stabilise the cascaded system, but also ensure a good dynamic performance of the load converter. Similar to the PVI control strategy, the proposed SVI control strategy can also be realised by a simple digital control algorithm. Thus, the SVI control strategy is feasible in practice as well. In addition, the SVI control strategy can be treated as a development of, and complement to the PVI control strategy. Finally, two example systems are fabricated to validate the accuracy of the SVI control strategy.

Chapter 4

Adaptive-PVI (APVI) Control for Load Converters

In Chapters 2 and 3, a family of load stabilisation methods, PVI and SVI control strategies, are proposed. Compared to the existing stabilisation methods, both PVI and SVI control strategies take into account the stability of the cascaded system and the dynamic performance of the load converter.

However, although the proposed PVI and SVI control strategies are more competitive than the other existing stabilisation methods, they require detailed information about the source converter when designing their impedance regulator. In other words, if the source converter is changed, either the PVI or SVI control strategy must re-design its impedance regulator. Obviously, this creates conflict with the purpose of the modularity design of the cascaded system, hence increasing the system development cycles. It is worth pointing out that this problem also occurs in the existing stabilisation methods.

In order to solve the above problem, the adaptive function is first introduced into the PVI control strategy in this chapter to generate a new stabilisation method: Adaptive PVI (APVI) control strategy. The APVI control strategy connects a self-regulated virtual impedance in parallel with the input port of the load converter. Thanks to this adaptive virtual impedance, the load converter can change its input impedance adaptively with different source converters to stabilise the whole system. The APVI control strategy can therefore make all the load converters into stable modules in different cascaded systems. Furthermore, the APVI control strategy inherits the advantage of the PVI control strategy, such as only modifying the load input impedance in a very small frequency range to keep the

original dynamic performance of the load converter. Therefore, the APVI control strategy can be treated as an improved method of the PVI control strategy, which makes the PVI control strategy more competitive in practice.

The rest of this chapter is organised as follows: in Section 4.1, the stability preferred load input impedance for the APVI control strategy is discussed. The adaptive concept, realisation method and operation flow of the APVI control strategy are then discussed in Section 4.2. Following that, two different cascaded systems composed by two different *LC* input filters and the same load converter, are designed and experimentally implemented to verify the effectiveness of the proposed APVI method in Section 4.3. Finally, Section 4.4 concludes the chapter.

4.1 Stability-preferred Input Impedance of the Load Converter with the APVI Control Strategy

Fig. 4.1(a) shows the Bode plots of the source output impedance Z_{oS} and the load input impedance Z_{iL} in a typical instability case. Here, if the source converter is a switching-mode power supply, f_{CS} is the cut-off frequency of its voltage loop; if the source converter is a *LC* input filter, f_{CS} is the filter resonant frequency. In addition, f_{CL} is the cut-off frequency of the voltage loop of the load converter. Z_{oSP} is the peak value of $|Z_{oS}|$. According to Fig. 4.1(a), the cause of the instability can be summarised as follows: if $|Z_{oS}|$ is intersected with $|Z_{iL}|$, and if f_{CS} is less than f_{CL}, the cascaded system is unstable even if the subsystems can work well individually (Sun, 2009). The -180^o phase resulting from the load negative resistor characteristic is the main cause of the instability in the cascaded system (Zhang et al., 2015). According to Fig. 4.1(a), the worst instance of instability problems in a cascaded system occurs at full load and with the source converter being a *LC* input filter.

As seen in Chapters 2 and 3, there is nothing more desirable than changing Z_{iL} only in the vicinity of the intersection frequencies (f_1 and f_2) of $|Z_{oS}|$ and $|Z_{iL}|$, to stabilise the cascaded system while keeping a better dynamic performance from the load converter. Therefore, this chapter only increases the phase of Z_{iL} during $[f_1, f_2]$, which can ensure $|\varphi(Z_{oS}) - \varphi(Z_{iL})| < 180^0$ at the intersection frequencies range. Such shaping $\varphi(Z_{iL})$ method not only keeps the advantage of the existing PVI control strategy, but is also con-

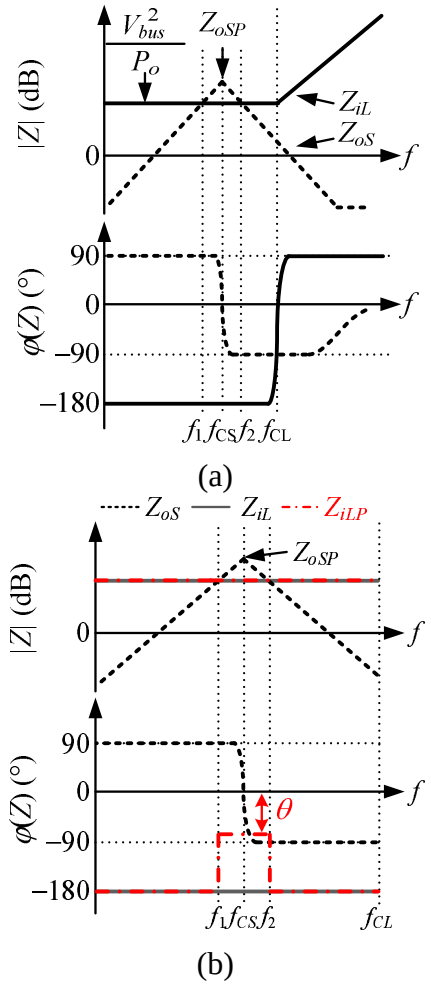


Figure 4.1: Instability reason and stability-preferred input impedance of the load converter with the APVI control strategy: (a) instability reason; (b) stability-preferred input impedance of the load converter.

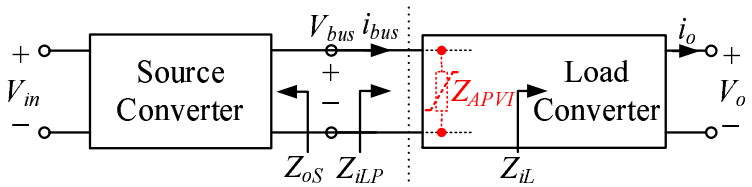


Figure 4.2: A cascaded system with adaptive parallel-virtual-impedance.

ducive to the realisation of the latter proposed APVI control strategy. As shown in Fig. 4.1(b), the stability-preferred input impedance of the load converter Z_{iLP} can be expressed as

$$Z_{iLP} = \begin{cases} -|Z_{iL1}|e^{j\theta} & f \in [f_1,\, f_2] \\ Z_{iL} & f \notin [f_1,\, f_2] \end{cases} \tag{4.1}$$

where, Z_{iL} is the original input impedance of the load converter, $|Z_{iL1}|$ and θ are the magnitude and phase of the improved input impedance of the load converter within $[f_1,\, f_2]$. In order to ensure $|\varphi(Z_{oS}) - \varphi(Z_{iLP})| < 180^0$, θ should satisfy $\theta \in (-90^0, 90^0)$. Since $|\varphi(Z_{oS}) - \varphi(Z_{iLP})| < 180^0$ at $[f_1,\, f_2]$, $|Z_{iL1}|$ can be any values. In order to minimise the resulting effect on the load converter, $|Z_{iL1}|$ is designed to be equal to $|Z_{iL}|$ (see Fig. 4.1(b)).

4.2 APVI Control Strategy

4.2.1 Adaptive-Parallel-Virtual-Impedance Z_{APVI} and its Adaptive Approach

As shown in Fig. 4.2, if a virtual impedance Z_{APVI} is added in parallel with the input port of the load converter, the load input impedance is changed to

$$Z_{iLP} = Z_{iL} \parallel Z_{APVI} = \frac{Z_{iL} \cdot Z_{APVI}}{Z_{iL} + Z_{APVI}} \tag{4.2}$$

where Z_{iL} is the original load input impedance and equal to $-V_{bus}^2/P_o$ when $f < f_{CL}$. Here, V_{bus} and P_o are the input voltage and output power of the load converter, respectively.

According to (4.1) and (4.2), where the load input impedance is needed to meet (4.1), Z_{APVI} should be

$$Z_{APVI} = \begin{cases} \left(V_{bus}^2/P_o\right) \cdot \left[e^{j\theta}/(1+e^{j\theta})\right] & f \in [f_1,\, f_2] \\ +\infty & f \notin [f_1,\, f_2] \end{cases} \tag{4.3}$$

As seen from (4.3), within $[f_1,\, f_2]$, Z_{APVI} is a constant value, which is determined by the load converter, otherwise, $Z_{APVI} = +\infty$. Since f_1 and f_2 are very close to f_{CS} (see Fig. 4.1(a)), the frequency characteristics of Z_{APVI} are also affected by the source converter. In other words, for an actual load converter, if its source converter is changed, the frequency

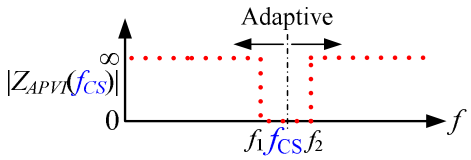


Figure 4.3: Adaptively parallel-virtual-impedance $Z_{APVI}(f_{CS})$.

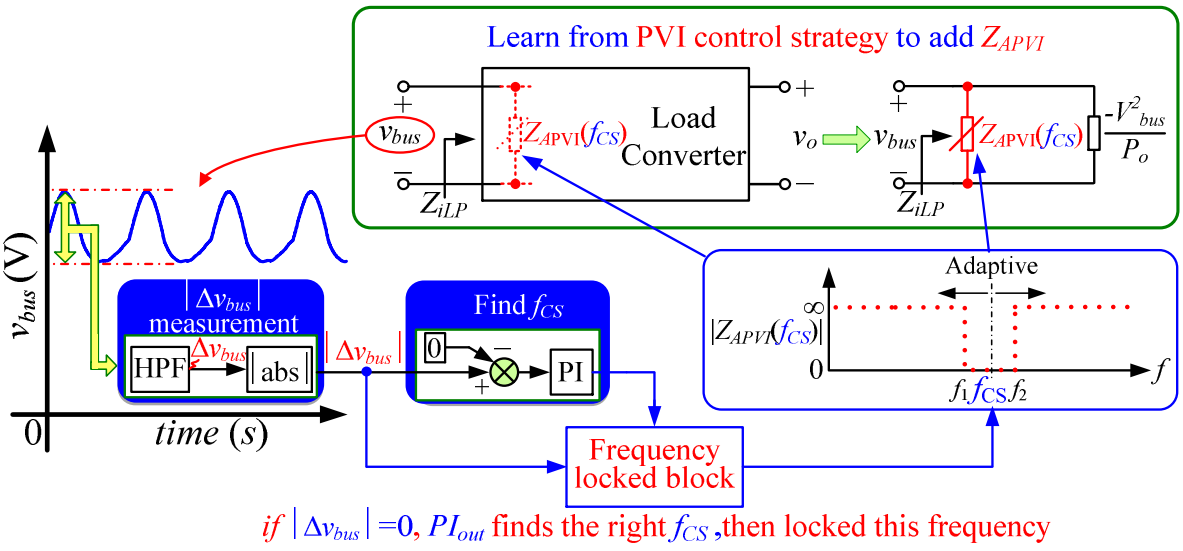


Figure 4.4: Basic idea of the adaptive approach of $Z_{APVI}(f_{CS})$.

characteristics of Z_{APVI} must be changed accordingly. It is presumed that if Z_{APVI} can be changed adaptively according to different source converters, as seen in Fig. 4.3, the load converter does not necessarily need to be changed any more. Therefore, realising the adaptive virtual impedance $Z_{APVI}(f_{CS})$ is the main aim of the proposed APVI control strategy.

Fig. 4.3 illustrates that $Z_{APVI}(f_{CS})$ is a function with respect to f_{CS}. Therefore, the key purpose of realising $Z_{APVI}(f_{CS})$ is to find f_{CS} when the source converter is changing. In order to solve this problem, an adaptive approach, as shown in Fig. 4.4, is proposed in this chapter. There are four basic steps to this approach. Firstly, $|\triangle v_{bus}|$ is sampled and sent to the positive input of a proportional–integral (PI) controller and compared with the PI negative input 0. Secondly, the output of the PI controller is set as the f_{CS} of $Z_{APVI}(f_{CS})$. Thirdly, according to (4.3) and the PVI control strategy in Chapter 2, $Z_{APVI}(f_{CS})$ is added to the input port of the load converter via control method. Finally, if $|\triangle v_{bus}|$ becomes 0, it means $Z_{APVI}(f_{CS})$ has found the right f_{CS} via the PI controller. At this point, a frequency-

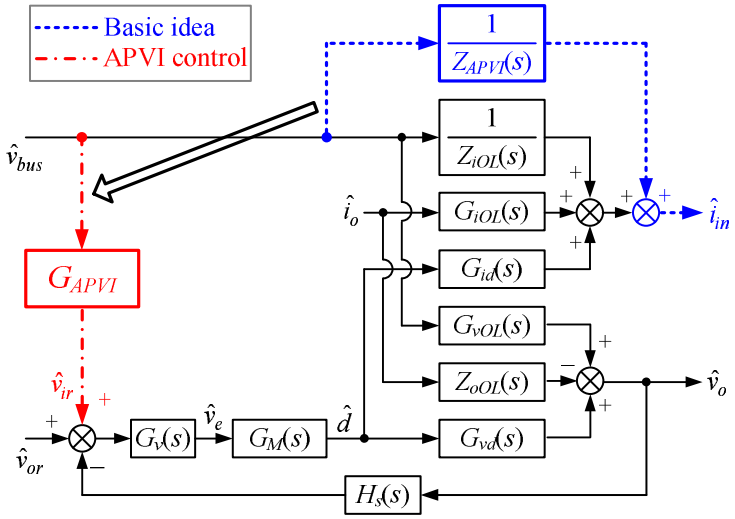


Figure 4.5: Concept of the APVI control strategy.

locked block starts working to lock the right f_{CS} for the $Z_{APVI}(f_{CS})$. According to Fig. 4.4, with the proposed adaptive approach, $Z_{APVI}(f_{CS})$ can find its right f_{CS} when the source converter changes.

It is worth pointing out that Fig. 4.4 not only shows the basic adaptive approach of realising $Z_{APVI}(f_{CS})$, but also the main idea of the proposed APVI control strategy. Using Fig. 4.4, the APVI control strategy and its detailed realisation method will be discussed in Sections 4.2.2 and 4.2.3, respectively.

4.2.2 The APVI Control Strategy

Fig. 4.5 shows the small-signal control block of the original load converter. Its variables and transfer functions are described in Table 4.1. If Z_{APVI} must be added in parallel with the input port of the load converter, one intuitive way is to introduce $1/Z_{APVI}$ to the control block between the input voltage and input current (as represented with dashed lines in Fig. 4.5). However, this method cannot be achieved by control directly. In order to address this issue, the output of $1/Z_{APVI}$ is moved to the output voltage reference and equivalent adjustments to the transfer function to $G_{APVI}(s)$, as shown by the dot-dashed lines. Fig. 4.5 is the concept of the proposed APVI control strategy, and $G_{APVI}(s)$ is expressed as

$$G_{APVI}(s) = \frac{1}{Z_{APVI}(s)} \cdot \frac{1 + T_v(s)}{G_v(s) \cdot G_M(s) \cdot G_{id}(s)} \tag{4.4}$$

Table 4.1: Variables and transfer functions of load converter

$\hat{v}_{bus}$	Perturbation of the bus voltage
$\hat{i}_o$	Perturbation of the load current
$\hat{i}_{bus}$	Perturbation of the bus current
$\hat{d}$	Perturbation of the duty cycle
$\hat{v}_o$	Perturbation of the output voltage
$\hat{v}_{or}$	Perturbation of the output voltage reference
$G_v(s)$	Transfer function of the voltage regulator
$G_M(s)$	Transfer function of the modulator
$Z_{iOL}(s)$	Open-loop input impedance
$G_{vd}(s)$	Control to output voltage transfer function
$G_{id}(s)$	Control to input current transfer function
$Z_{oOL}(s)$	Open-loop output impedance
$H_s(s)$	Sampling coefficient of the output voltage
$G_{iOL}(s)$	Open-loop load to input current transfer function
$G_{vOL}(s)$	Open-loop input to output voltage transfer function

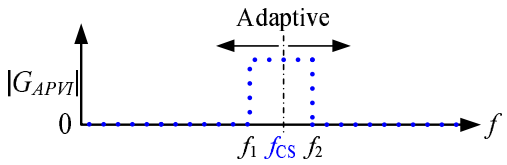


Figure 4.6: Adaptive characteristic of $|G_{APVI}(s)|$.

where $T_v(s) = H_s(s)G_v(s)G_M(s)G_{vd}(s)$ is the voltage-closed loop gain of the load converter.

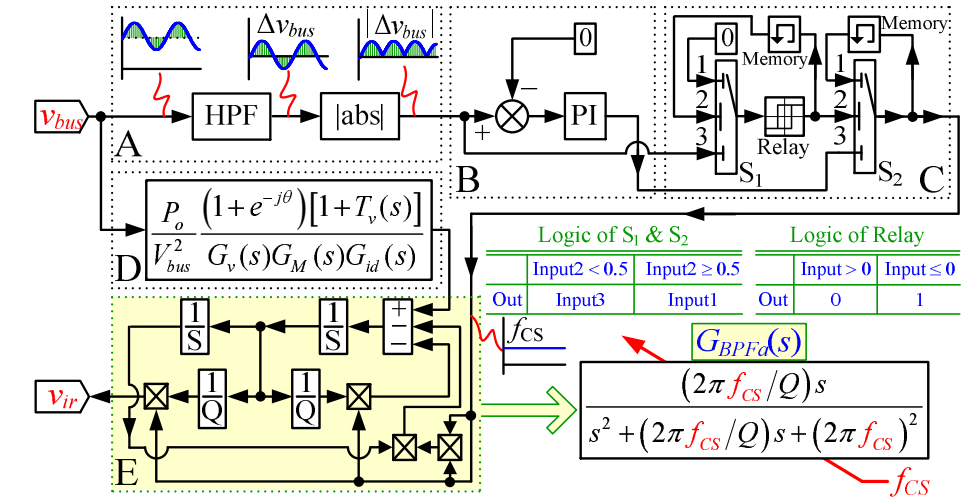
Note: since the derivation of $G_{APVI}(s)$ is very similar to $G_{PVI}(s)$ in Chapter 2, it will not be repeated here.

4.2.3 Realisation of the APVI Control Strategy

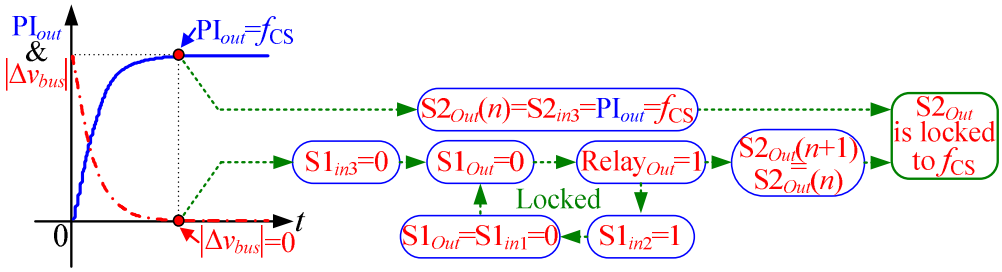
Substituting (4.3) for (4.4), the adaptive regulator $G_{APVI}(s)$ can be further derived as

$$G_{APVI}(s) = \begin{cases} \frac{P_o(\frac{1+e^{j\theta}}{e^{j\theta}})[1+T_v(s)]}{V_{bus}^2 G_v(s)G_M(s)G_{id}(s)} = \frac{P_o(1+e^{-j\theta})[1+T_v(s)]}{V_{bus}^2 G_v(s)G_M(s)G_{id}(s)} & f \in [f_1, f_2] \\ 0 & f \notin [f_1, f_2] \end{cases} \tag{4.5}$$

As seen in (4.5), $G_{APVI}(s)$ is an adaptive frequency-based piecewise function, which is shown in Fig. 4.6, where $|G_{APVI}(s)|$ is a non-zero value within $[f_1, f_2]$ and zero outsides $[f_1, f_2]$. Since f_1 and f_2 are very close to f_{CS}, an adaptive band-pass filter $G_{BPFa}(s)$, whose



(a)



(b)

Figure 4.7: Realisation of the $G_{APVI}(s)$: (a) control circuit of $G_{APVI}(s)$; (b) adaptive mechanism of $G_{APVI}(s)$.

centre frequency is f_{CS}, can be utilised to realise $G_{APVI}(s)$, i.e.,

$$G_{APVI}(s) = G_{APVI1}(s) \cdot G_{BPFa}(s) \tag{4.6}$$

where

$$G_{APVI1}(s) = \frac{P_o}{V_{bus}^2} \frac{(1+e^{-j\theta})[1+T_v(s)]}{G_v(s)G_M(s)G_{id}(s)} \tag{4.7}$$

$$G_{BPFa}(s) = -\frac{s(2\pi f_{CS}/Q)}{s^2+s(2\pi f_{CS}/Q)+(2\pi f_{CS})^2} \tag{4.8}$$

where, Q is the quality factor of the band pass filter, whose initial value is recommended as 0.707 and can be changed manually as needed; f_{CS} is changed adaptively according to different source converters. For (Cuk, 1976), the numerator degree of $G_{APVI}(s)$ is always lower than its denominator degree for all DC/DC converters. As a result, $G_{APVI}(s)$ is a proper transfer function that can be fully implemented by digital chips.

To ensure $G_{APVI}(s)$ can realise $Z_{APVI}(s)$ and find f_{CS} adaptively, a specific control circuit for $G_{APVI}(s)$ is proposed in this section. Fig. 4.7(a) illustrates this control circuit which contains five parts and operates as follows:

In Part A, v_{bus} first goes through a high-pass-filter (HPF) and an absolute value block to extract $|\triangle v_{bus}|$. Following this, $|\triangle v_{bus}|$ goes through Parts B and C to find f_{CS} adaptively. As shown in Figs. 4.7(a) and (b), the adaptive mechanism of Parts B and C can be explained as: in Part B, $|\triangle v_{bus}|$ is firstly compared with 0, meanwhile, its error is amplified by a PI controller. Therefore, the output of the PI controller, PI_{out}, can be expressed as:

$$PI_{out}(t) = K_p\,|\triangle v_{bus}(t)| + K_i \int_0^t |\triangle v_{bus}(t)|\,dt \tag{4.9}$$

where K_p and K_i are the proportional and integral coefficients of PI controller, respectively.

According to (4.9), if the system is unstable, $|\triangle v_{bus}| > 0$, PI_{out} would be increased from zero. By Fig. 4.7(a), PI_{out} also decides the centre frequency of $Z_{APVI}(s)$. Therefore, once PI_{out} is increased to f_{CS}, $Z_{APVI}(s)$ will find its right centre frequency, stabilise the cascaded system and make $|\triangle v_{bus}| = 0$. Then according to Part C and Fig. 4.7(b), the input 3 of S_1 is equal to $0 \rightarrow$ the output of S_1 becomes $0 \rightarrow$ the output of *Relay* changes to $1 \rightarrow$ the input 2 of S_1 changes to $1 \rightarrow$ the output of S_1 is changed to the input 1 of S_1 and becomes 0 again$\rightarrow$ the output of *Relay* is locked as 1. Therefore, the output of S_2, $S2_{Out}$, is always equal to its previous value

$$S2_{Out}(n+1) = S2_{Out}(n) = f_{CS} \tag{4.10}$$

where $n+1$ and n represent the time $n+1$ and its previous time n, respectively. Both are after PI_{out} finding f_{CS}.

According to Fig. 4.7 and (4.10), as $S2_{Out}$ is equal to f_{CS} before the relay is locked, the centre frequency of $Z_{APVI}(s)$ is finally locked as f_{CS} and will not be changed any more. At the same time, v_{bus} is sent to Part D to realise $G_{APVI1}(s)$ in (4.7). Both of the outputs of Parts C and D are then sent to Part E, where the $G_{BPFa}(s)$ can be achieved. Finally, the output of $G_{APVI}(s)$ can be obtained from the output of Part E.

Note that, though $G_{APVI}(s)$ can lock f_{CS} as the final centre frequency of $G_{BPFa}(s)$ after finding it, too large K_p and K_i parameters should be avoided in the design of the PI con-

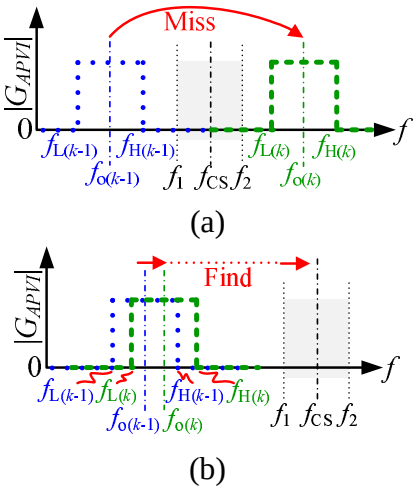


Figure 4.8: Impact of K_p and K_i on $G_{APVI}(s)$: (a) large K_p and K_i; (b) small K_p and K_i.

troller in Part B of Fig. 4.7. As can be seen in Fig. 4.8(a), this is because if K_p and K_i are too large, this may cause the output of the PI controller to increase so much during a sampling period, and consequently for f_{CS} to be skipped. For this reason, small K_p and K_i are preferred for the PI controller (Fig. 4.8(b)). The only compromise is that the $G_{APVI}(s)$ may spend a slightly longer time before the right f_{CS} is founded. However, if the APVI controller finds the right f_{CS}, the PI controller will be disabled and the K_p and K_i do not affect any steady or dynamic performance of the load converter. Therefore, small K_p and K_i are accepted in practice.

4.2.4 Operation Flow of the APVI Control Strategy

Fig. 4.9 gives the operation flow of the APVI control strategy. First of all, the user needs to check both source and load converters to make sure they can work well individually. Then, if the cascaded system is unstable, $G_{APVI}(s)$ will be utilised. For $G_{APVI}(s)$, its initial value of Q is set as 0.707. This is because Q=0.707 can ensure a relatively narrow passband for $G_{BPFa}(s)$, and if 0.707 is also suitable for Q, the $G_{APVI}(s)$ not only can stabilise the cascaded system, but also keep the original dynamic performance of the load converter. However, if the system is still unstable, this means that 0.707 is too much larger than Q, i.e., the bandwidth of $G_{BPFa}(s)$ is smaller than $(f_2 - f_1)$. As a result, the user should reduce Q and test the system again until the suitable Q is found.

It is worth pointing out that, though the type of the typical input voltage feed-forward

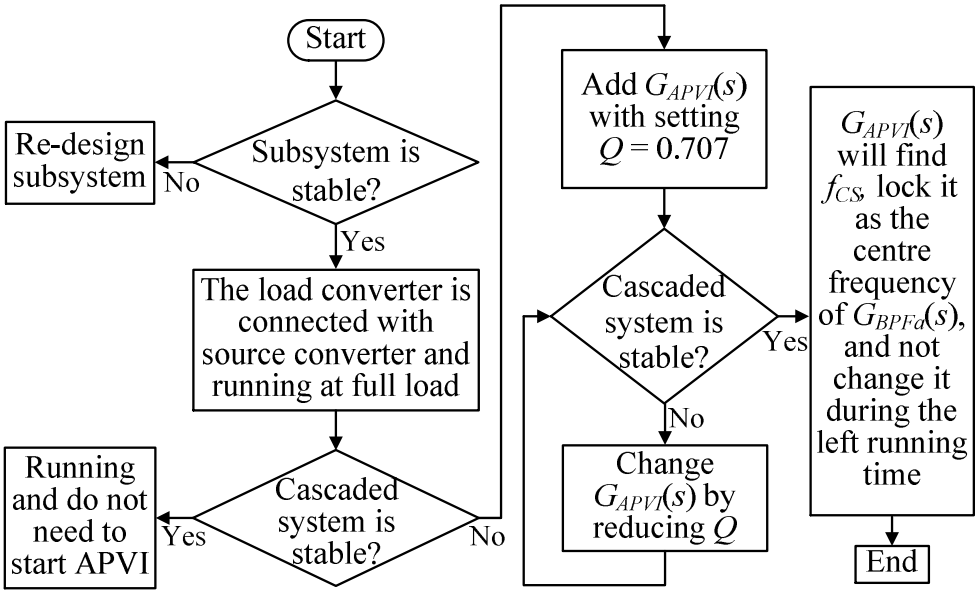


Figure 4.9: Operation flow of the APVI control method.

control loop seems similar to the proposed APVI control block, they are in fact entirely different. The purpose of the typical input voltage feed-forward control loop is to regulate the input impedance of the load converter to a pure negative resistor within the whole frequency range. However, the purpose of the APVI control method is to remove the negative resistor characteristic from the input impedance of the load converter. As a result, the proposed APVI control method can stabilise the cascaded system, but the typical input voltage feed-forward method cannot.

4.3 Experimental Verification

As the worst instability phenomena are most likely to arise in a cascaded system whose source converter is a *LC* input filter, the APVI control strategy is applied into two such unstable 100 W cascaded systems. As shown in Fig. 4.10, the two cascaded systems utilise the same load stage, which is a 48 V-24 V Buck converter with a 20 kHz switching frequency. If the load stage is connected to the source stage 1, which is an input filter formed by a 6 mH inductor and a 150 μF capacitor, the first unstable system is formed. On the other hand, if the load converter is connected to the source stage 2, which is an input filter whose inductor and capacitor are 6 mH and 60 μF, respectively, the second unstable

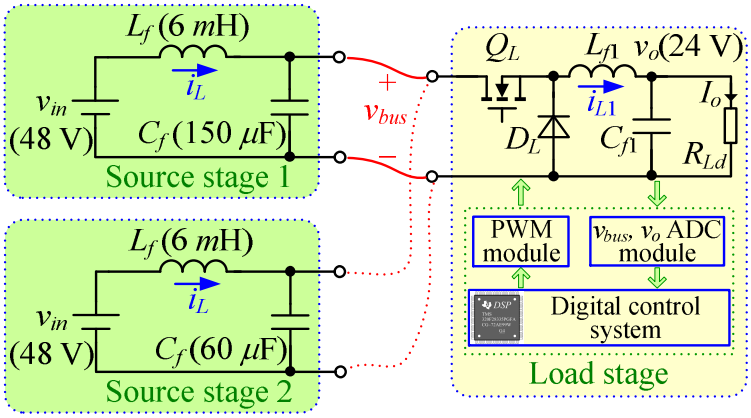


Figure 4.10: Example cascaded systems.

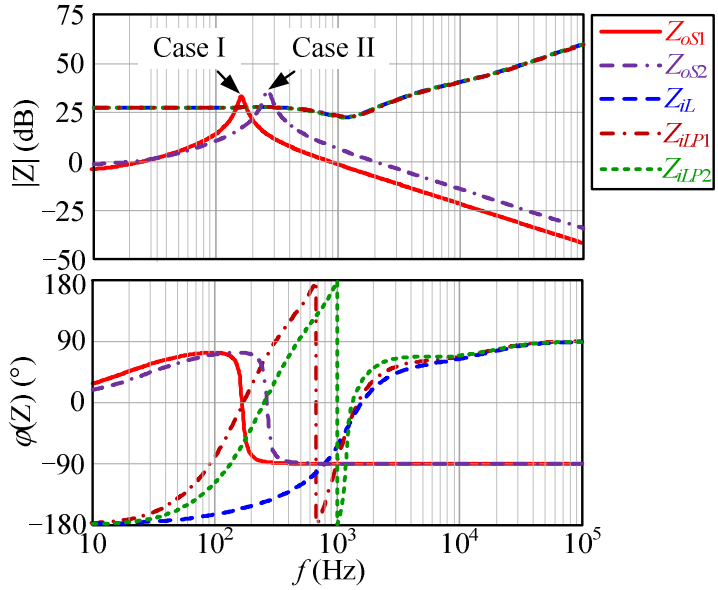


Figure 4.11: Bode plots of example systems at full load.

system is formed. It is worth pointing out that, since the load switching frequency in this chapter is different to that discussed in Chapter 2, the parameters of the *LC* input filter are also different.

Fig. 4.11 shows the Bode plots of the example systems, where Z_{oS1}, Z_{oS2} and Z_{iL} are the output impedance of source stage 1, the output impedance of source stage 2 and the input impedance of the load converter at full load, respectively. It can be seen that both of the two cascaded systems are unstable.

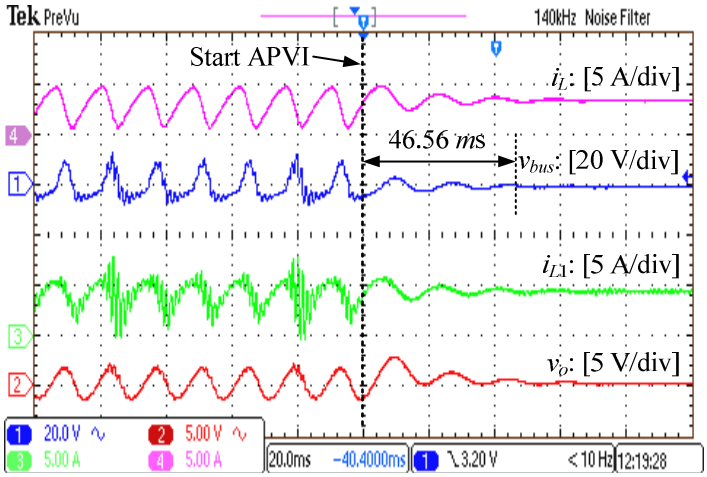
According to Figs. 4.5 and 4.7, an adaptive input impedance regulator $G_{APVI}(s)$ is introduced to the load converter. Here, θ is selected as 0. Then, as shown in Fig. 4.11, Z_{iL}

is modified into Z_{iLP1} in the first cascaded system and Z_{iLP2} in the second cascaded system adaptively. In both cases, $|\varphi(Z_{oS}) - \varphi(Z_{iLP})| < 180^0$ at the intersection frequencies of $|Z_{oS}|$ and $|Z_{iL}|$. Therefore, the modified cascaded system with the APVI control method is stable and the design of $G_{APVI}(s)$ is appropriate. In addition, Fig. 4.11 shows that, $G_{APVI}(s)$ can achieve a modified input impedance in Fig. 4.1(b), i.e., only changing the phase of the load input impedance in a very small frequency range, which minimise the resulting effect on the load converter.

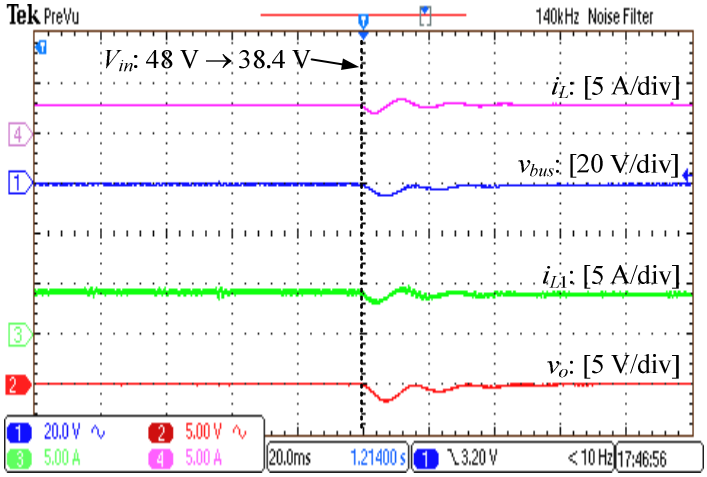
The experimental results of the first example system are given in Fig. 4.12, where the waveforms of v_{bus} and v_o are their ac components to clearly show the oscillation (i_L, v_{bus}, i_{L1} and v_o are illustrated in Fig. 4.10). As seen in Fig. 4.12(a), this cascaded system is unstable without the APVI control strategy. After the APVI control strategy was utilised, it spent about 45.56 ms to adjust the parameters of $G_{APVI}(s)$ and to stabilise the cascaded system automatically. Fig. 4.12(b) shows the dynamic waveforms of the modified system with the APVI control strategy when its input voltage steps down from 100% rated to 80% rated voltage at the full load. It seems that, the APVI control strategy can work well during an input voltage change. Fig. 4.12(c) shows the dynamic waveforms of the modified system with the APVI control strategy when its load increases from 10% rated to 100% rated load at the rated input voltage. This demonstrates that the APVI control strategy can also work well during a load change.

Similarly, Figs. 4.13(a), (b) and (c) give the steady state waveforms, input voltage and load dynamic waveforms of the second example system. Again, it verifies that the APVI control strategy can not only solve the instability problem of the cascaded system adaptively, but also work well during the dynamic process. The above experimental results can be said to have verified the effectiveness of the proposed APVI control strategy.

It is worth pointing out that, though the APVI control strategy introduces the adaptive function to the PVI control strategy and can be treated as an improved PVI control strategy, it needs relatively more time to search the centre frequency of the APVI. Therefore, the execution time of the APVI algorithm is longer than that of the PVI algorithm. Since the switching period of a converter should be larger than the algorithm execution time, the load experimental switching frequency is decreased from 100 kHz in Chapter 2 to 20 kHz in this chapter. Since low switching frequency always leads to a larger inductor and capacitor



(a)



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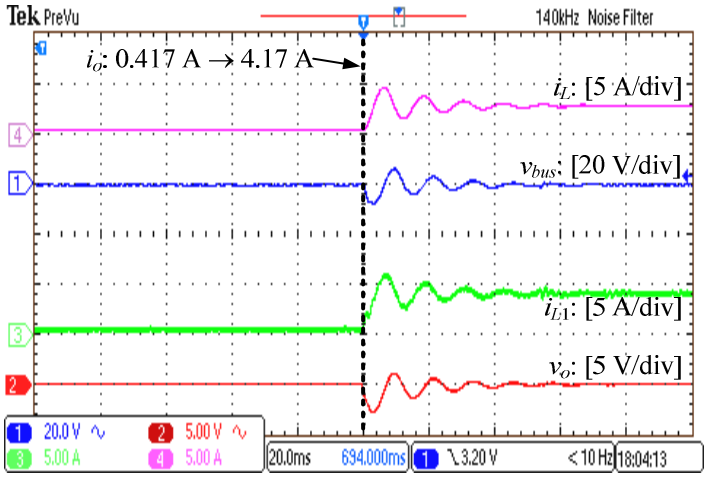
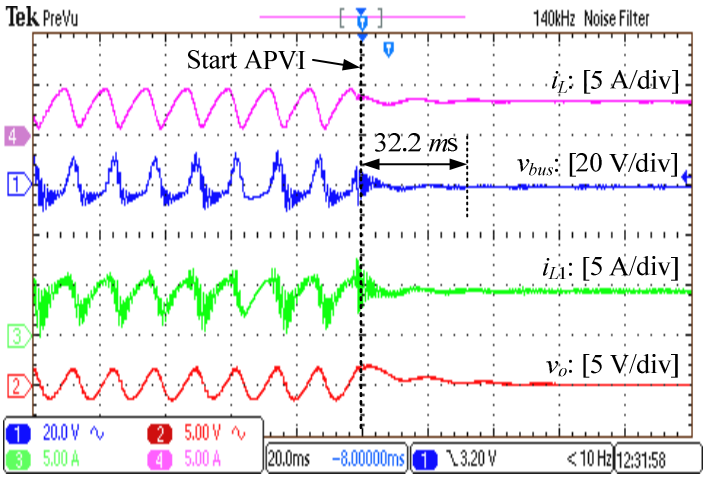
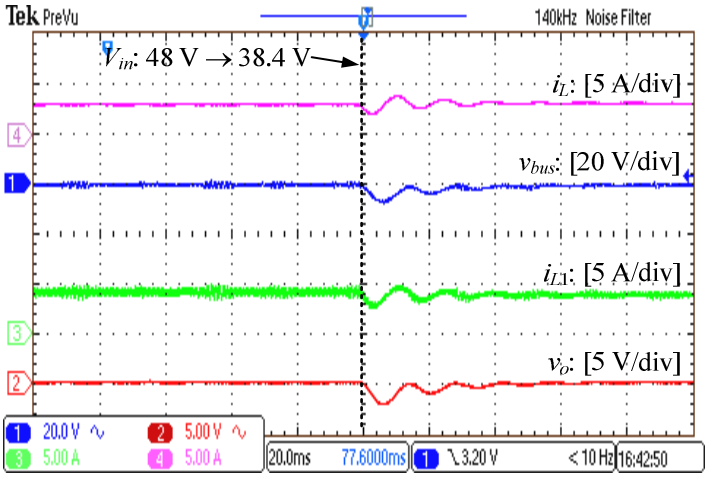


(c)

Figure 4.12: Experimental waveforms of the first cascaded system with the APVI control strategy: (a) steady state waveforms with rated input voltage and rated load, (b) dynamic waveforms when the input voltage steps down from 100% rated to 80% rated voltage at full load, (c) dynamic waveforms when the load increases from 10% rated to 100% rated load at rated input voltage.



(a)



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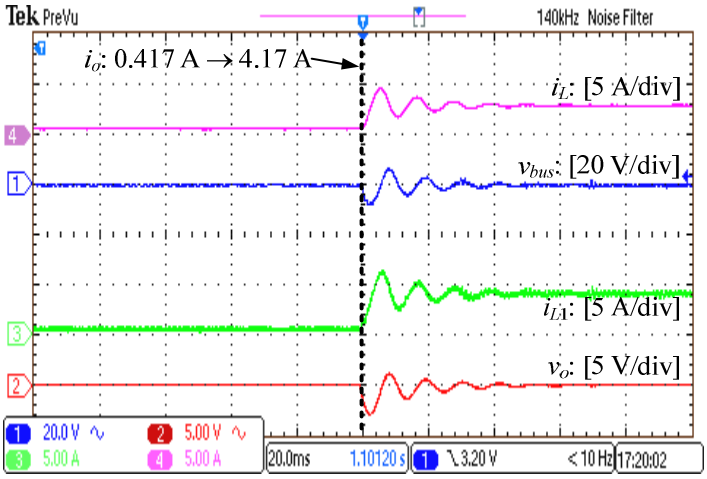


(c)

Figure 4.13: Experimental waveforms of the second cascaded system with the APVI control strategy: (a) steady state waveforms with rated input voltage and rated load, (b) dynamic waveforms when the input voltage steps down from 100% rated to 80% rated voltage at full load, (c) dynamic waveforms when the load increases from 10% rated to 100% rated load at rated input voltage.

of the *LC* input filter, the parameters of the *LC* input filter in this chapter are also different from that discussed in Chapter 2. Therefore, the relatively longer algorithm execution time is the restriction of the APVI control strategy.

4.4 Summary

In order to solve the instability problem and maintain the modularisation characteristics of the cascaded system, an APVI control strategy is proposed in this chapter. This demonstrates that the APVI control strategy can adaptively regulate the input impedance of the load converter for different source converters by adding a self-regulated virtual impedance in parallel with the load converter. As a result, the APVI control strategy means that the load converter can be designed as a standard module stably connected to any source converter. Additionally, the APVI control strategy also inherits the advantage of the PVI control strategy to keep most of the dynamic performance of the load converter. Therefore, the APVI control strategy can be treated as an improved method of the PVI control strategy. Finally, the APVI control strategy has been experimentally verified on two cascaded systems.

Chapter 5

Adaptive-SVI (ASVI) Control for Load Converters

As demonstrated in Chapters 2 and 3, the cascaded system can be stabilised via amplitude compensation (SAC) or phase compensation (SPC) for the input impedance of the load converter. Since both SAC and SPC can be realised by both PVI and SVI control strategies, a further analysis of SAC/SPC and a further investigation of the PVI / SVI control strategies are carried out in this chapter. Firstly, it is shown that the cascaded system adopting the SAC is unconditionally stable, but conditionally stable when adopting the SPC, i.e., the cascaded system with SAC is more stable than that with SPC. It is then noted that the PVI control strategy has inevitable limitations when realising the SAC during the whole load and input voltage range of the load converter, but the SVI control strategy does not have limitations. In other words, the SVI control strategy is more competent for the SAC. Furthermore, in order to stably connect a load converter to different source converters, such as *LC* input filters and traditional DC/DC converters, without changing its internal structure, the adaptive function is also introduced to the traditional SVI control strategy in this chapter. With the Adaptive SVI (ASVI) control strategy, the series-virtual-impedance is able to adaptively regulate its characteristic to stabilise the cascaded system according to different source converters.

It should be stressed that although the adaptive characteristics of the ASVI control strategy are similar to those of the APVI control strategy, they are entirely different from in terms of physical concept, stabilisation method and realisation approach. The APVI control strategy adds a virtual impedance in parallel with the load converter by an APVI

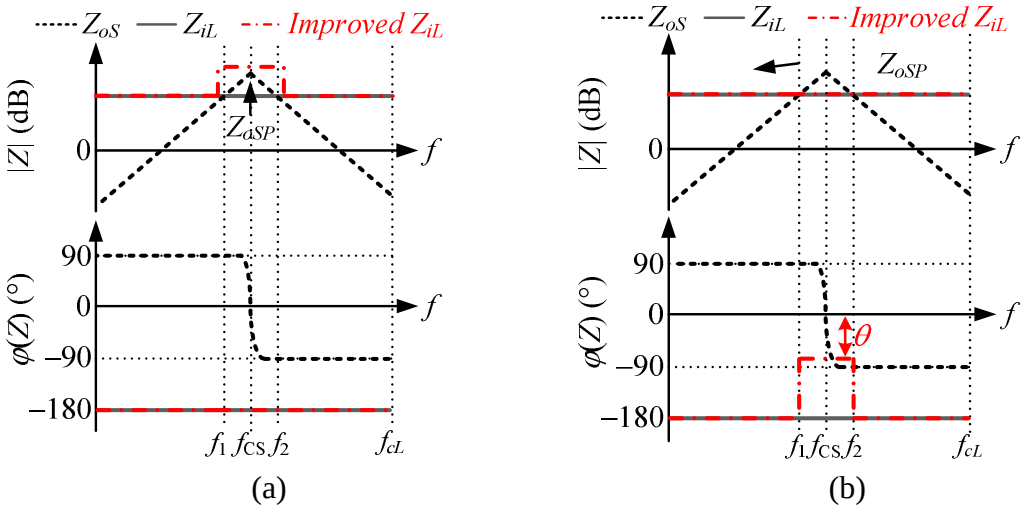


Figure 5.1: Bode plots of SAC and SPC: (a) SAC; (b) SPC.

controller to realise SPC. However, the ASVI control strategy adds a virtual impedance in the series with the load converter by an ASVI controller to realise SAC. Since SAC is more stable than SPC, the ASVI control strategy is superior to the APVI control strategy.

The remaining parts of this chapter are organised as follows: in Section 5.1, SAC and SPC are compared. The PVI and SVI control strategies are then compared in Section 5.2. Following this, the concept, realisation and impact of the ASVI control strategy are discussed in Section 5.3. Section 5.4 gives the experimental verification of the proposed ASVI control strategy. Finally, Section 5.5 concludes the chapter.

5.1 Stabilisation via Amplitude Compensation (SAC) and Phase Compensation (SPC)

As SAC and SPC are two effective stabilisation methods for the load converter, they are reviewed and compared carefully in this section. As shown in Figs. 5.1(a) and (b), SAC increases $|Z_{iL}|$ to keep a total separation with $|Z_{oS}|$, while SPC increases $\varphi(Z_{iL})$ to ensure $|\varphi(Z_{oS}) - \varphi(Z_{iL})| < 180^0$ at the intersection frequencies (f_1 and f_2 in Fig. 5.1) of $|Z_{iL}|$ and $|Z_{oS}|$. As both SAC and SPC only change Z_{iL} in a very small frequency range, they can stabilise the cascaded system with the minimised load performance compromise.

However, though both SAC and SPC can stabilise the cascaded system with minimised performance degradation, their stabilising effects are essentially different, as can be seen

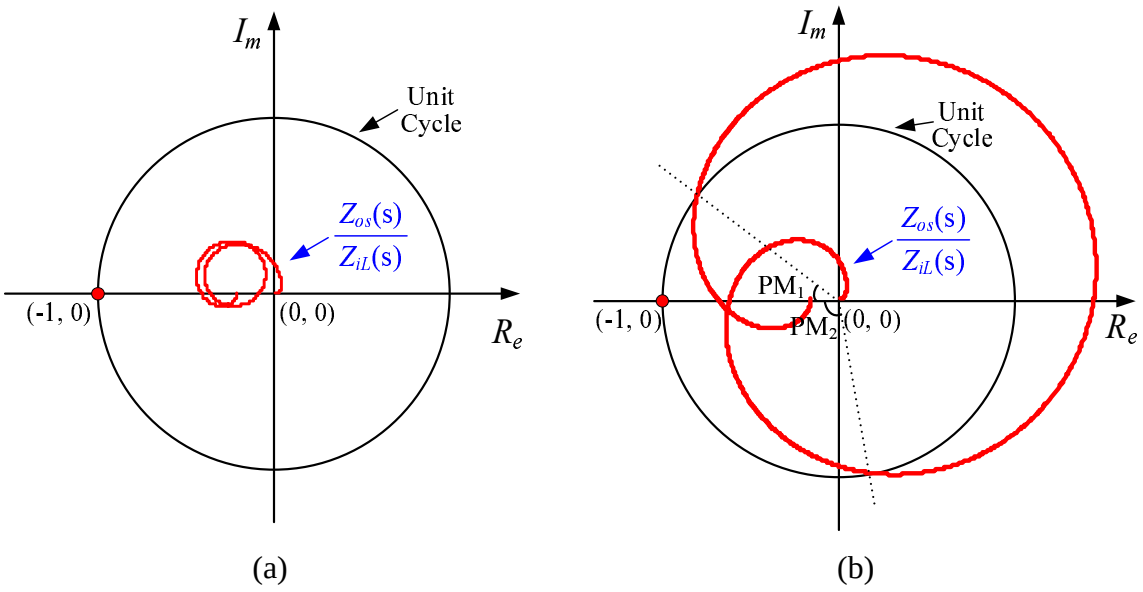


Figure 5.2: Nyquist plots of Z_{oS}/Z_{iL} with SAC and SPC: (a) with SAC; (b) with SPC.

from the Nyquist plots of two typical cases shown in Fig. 5.2. For the SAC, since it increases $|Z_{iL}|$ and ensures $|Z_{iL}| > |Z_{oS}|$ in the whole frequency range, the system loop gain Z_{oS}/Z_{iL} always stays inside the unit cycle, as shown in Fig. 5.2(a) (Middlebrook, 1979). Hence, with the SAC, the improved cascaded system is an unconditionally stable system. However, for the SPC, it only increases $\varphi(Z_{iL})$ to ensure $|\varphi(Z_{oS}) - \varphi(Z_{iL})| < 180^0$ during $(f_1,\ f_2)$ but does not change $|Z_{iL}|$. As a result, for the SPC, though Z_{oS}/Z_{iL} does not encircle $(-1,\ j0)$, it intersects with the unit cycle, i.e., the stability of this system still depends on the phase margin of Z_{oS}/Z_{iL}, see PM_1 and PM_2 in Fig. 5.2(b). In other words, with the SPC, the improved cascaded system is actually a conditionally stable system. Therefore, the SAC is more stable than the SPC and should be considered the preferred stabilisation method to shape the load input impedance.

5.2 Comparison of PVI and SVI Control Strategies

SAC is the preferred load stabilisation method. As noted in Chapters 2 and 3, as it can be realised by both PVI and SVI control strategies, a comparison of PVI and SVI control strategies is carried out in this section.

5.2.1 Limitation of PVI Control Strategy When Realising the SAC

As illustrated by Fig. 5.3, SAC can be realised by the PVI control strategy via adding a virtual impedance Z_{PVI} in parallel with the load converter. As the input impedance of the original load converter is $-V_{bus}^2/P_o$, the improved load input impedance Z_{iLP} can be expressed as

$$Z_{iLP} = \frac{-Z_{PVI} \cdot \left(V_{bus}^2/P_o\right)}{Z_{PVI} - \left(V_{bus}^2/P_o\right)} \tag{5.1}$$

where P_o and V_{bus} are the output power and voltage of the load converter, respectively. According to the PVI control strategy in Chapter 2, Z_{PVI} is a constant positive resistor inside $[f_1,\ f_2]$ and $+\infty$ outside $[f_1,\ f_2]$. Thus, $|Z_{iLP}|$ is only increased during $[f_1,\ f_2]$.

According to (5.1), during $[f_1,\ f_2]$, the curve of $|Z_{iLP}|$ to $\frac{P_o}{V_{bus}^2}$ is depicted in Fig. 5.4. As seen, $|Z_{iLP}|$ has three characteristics: 1) $|Z_{iLP}|$ is monotonically increased from $|Z_{PVI}|$ to $+\infty$ when $\frac{P_o}{V_{bus}^2}$ increases from 0 to $\left|\frac{1}{Z_{PVI}}\right|$; 2) $|Z_{iLP}|$ is monotonically decreased from $+\infty$ to 0 when $\frac{P_o}{V_{bus}^2}$ increases from $\left|\frac{1}{Z_{PVI}}\right|$ to $+\infty$; 3) $|Z_{iLP}| = |Z_{PVI}|$ when $\frac{P_o}{V_{bus}^2} = 0$ or $\frac{P_o}{V_{bus}^2} = \left|\frac{2}{Z_{PVI}}\right|$ respectively. Therefore, if the peak value of $|Z_{oS}|$ is Z_{oSP}, and if a total separation between $|Z_{oS}|$ and $|Z_{iLP}|$ (i.e., SAC) during the full load and input voltage range of the load converter is required, the curve of $|Z_{iLP}|$ during $[f_1,\ f_2]$ should be limited in the shadow part of Fig. 5.4, i.e., $|Z_{PVI}|$ should satisfy the following conditions:

$$|Z_{PVI}(j2\pi f)| \ > \ |Z_{oSP}|\,10^{\frac{GM}{20}} \qquad f \in [f_1,\ f_2] \tag{5.2}$$

$$\frac{2}{|Z_{PVI}(j2\pi f)|} \ > \ Max\left(\frac{P_o}{V_{bus}^2}\right)_L \qquad f \in [f_1,\ f_2] \tag{5.3}$$

where GM is the gain margin of $\frac{Z_{oS}}{Z_{iLP}}$ and its unit is $dB\Omega$. $Max\left(\frac{P_o}{V_{bus}^2}\right)_L$ is equal to $\frac{P_{oM}}{V_{bM}^2}$, where P_{oM} and V_{bM} are the maximum power and the minimum input voltage of the load converter, respectively.

According to (5.2) and (5.3), the selection range of $|Z_{PVI}|$ can be derived as

$$|Z_{oSP}|\,10^{\frac{GM}{20}} < |Z_{PVI}(j2\pi f)| < \frac{2V_{bM}^2}{P_{oM}} \quad f \in [f_1,\ f_2] \tag{5.4}$$

By (5.4), during $[f_1,\ f_2]$, the value of $|Z_{PVI}|$ is effective if and only if the following

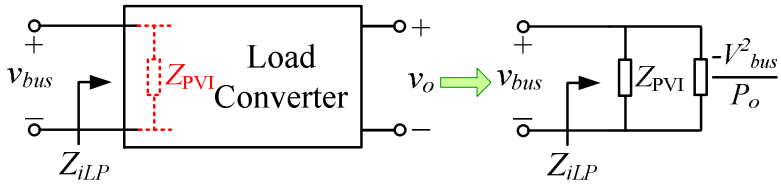


Figure 5.3: The PVI control strategy and its physical concept.

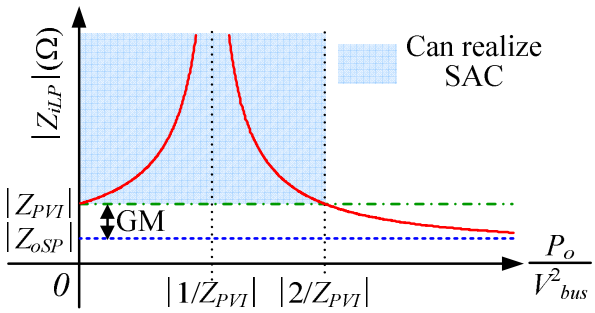


Figure 5.4: Requirement of Z_{PVI} during $[f_1,\ f_2]$ when realising the SAC

condition is satisfied

$$|Z_{oSP}|\,10^{\frac{GM}{20}} < \frac{2V_{bM}^2}{P_{oM}} \tag{5.5}$$

In other words, if (5.5) is not satisfied, the PVI control strategy cannot help the cascaded system realise the SAC during the whole load and input voltage range of the load converter. As a result, (5.5) is the limitation of the PVI control strategy when realising the SAC.

5.2.2 Advantage of SVI Control Strategy When Realising the SAC

Though PVI control strategy has inevitable limitations when achieving the SAC, the SVI control strategy is fully competent for the SAC without limitation. As shown in Fig. 5.5, SAC can be realised by the SVI control strategy via adding a virtual impedance Z_{SVI} in series with the load converter. The improved load input impedance Z_{iLS} is expressed as

$$Z_{iLS} = Z_{SVI} - \left(V_{bus}^2/P_o\right) \tag{5.6}$$

where Z_{SVI} is a constant negative resistor inside $[f_1,\ f_2]$ and 0 outside $[f_1,\ f_2]$ according to analysis in Chapter 3. Similar to $|Z_{iLP}|$, $|Z_{iLS}|$ is also only increased during $[f_1,\ f_2]$.

According to (5.6), during $[f_1,\ f_2]$, the curve of $|Z_{iLS}|$ to $\frac{P_o}{V_{bus}^2}$ is depicted in Fig. 5.6. As seen, $|Z_{iLS}|$ is monotonically decreased from $+\infty$ to $|Z_{SVI}|$ when $\frac{P_o}{V_{bus}^2}$ increases from

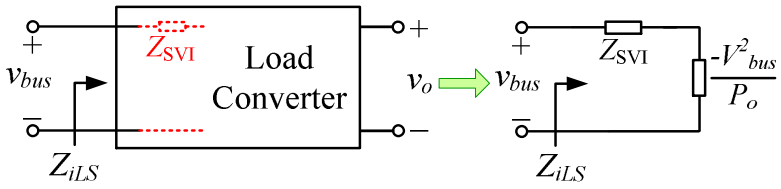


Figure 5.5: The SVI control strategy and its physical concept.

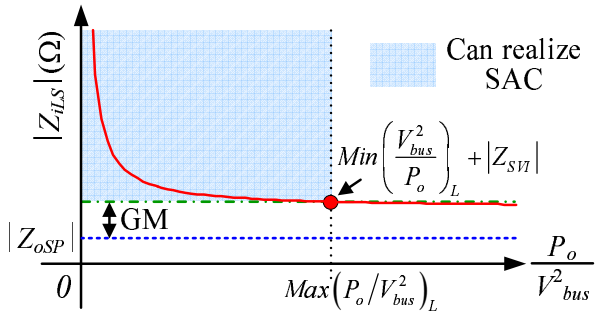


Figure 5.6: Requirement of $|Z_{SVI}|$ during $[f_1,\ f_2]$ when realising the SAC.

0 to $+\infty$. In addition, the value of $|Z_{iLS}|$ is equal to $Min\left(\frac{V^2_{bus}}{P_o}\right)_L + |Z_{SVI}|$ when $\frac{P_o}{V^2_{bus}} = Max\left(\frac{P_o}{V^2_{bus}}\right)_L$. Here $Min\left(\frac{V^2_{bus}}{P_o}\right)_L = \frac{V^2_{bM}}{P_{oM}}$, $Max\left(\frac{P_o}{V^2_{bus}}\right)_L = \frac{P_{oM}}{V^2_{bM}}$. Therefore, if the SAC must be realised by the SVI control strategy during the full load and input voltage range of the load converter, the curve of $|Z_{iLS}|$ during $[f_1,\ f_2]$ should be limited in the shadow part of Fig. 5.6, i.e., $|Z_{SVI}|$ should satisfy the following condition:

$$Min\left(\frac{V^2_{bus}}{P_o}\right)_L + |Z_{SVI}(j2\pi f)| > |Z_{oSP}|\,10^{\frac{GM}{20}} \qquad f \in [f_1,\ f_2] \tag{5.7}$$

According to (5.7), the requirement of $|Z_{SVI}|$ can be derived as

$$|Z_{SVI}(j2\pi f)| > |Z_{oSP}|\,10^{\frac{GM}{20}} - \frac{V^2_{bM}}{P_{oM}} \qquad f \in [f_1,\ f_2] \tag{5.8}$$

Obviously, for the cascaded system, during $[f_1,\ f_2]$, a higher $|Z_{SVI}(j2\pi f)|$ can always be found to meet the requirement of (5.8). As a result, the SVI control strategy can help the cascaded system to realise SAC during the whole load and input voltage range of the load converter without limitation. This is also the advantage of the SVI control strategy when realising SAC.

Therefore, the SVI control strategy is more suitable for the SAC than the PVI control

strategy.

5.3 The ASVI Control Strategy

5.3.1 Adaptive-Series-Virtual-Impedance Z_{ASVI} and its Adaptive Approach

According to (5.6) and Fig. 5.5, if $|Z_{iL}|$ must be changed to $|Z_{iLS}|$, Z_{SVI} can be selected as

$$Z_{SVI} = \begin{cases} Z_{iLS} + \left(V_{bus}^2/P_o\right) & f \in [f_1,\, f_2] \\ 0 & f \notin [f_1,\, f_2] \end{cases} \tag{5.9}$$

(5.8) and (5.9) llustrate that during $[f_1,\, f_2]$, $|Z_{SVI}|$ should be large enough to ensure that $|Z_{iLS}| > |Z_{oS}|$. In addition, as f_1 and f_2 are very close to f_{CS} (See Fig. 5.1(a)), the frequency characteristics of Z_{SVI} are also affected by the source converter. In other words, if Z_{SVI} wants to become an adaptive series-virtual-impedance Z_{ASVI} to help the load converter realise SAC with different source converters, it should satisfy three basic requirements: 1) when $f \in [f_1,\, f_2]$, $|Z_{ASVI}|$ should be large enough to ensure a total separation between $|Z_{iLS}|$ and $|Z_{oS}|$; 2) when $f \notin [f_1,\, f_2]$, $|Z_{ASVI}|$ should be small enough to minimise the impact of the ASVI control strategy on the original load converter; 3) $[f_1,\, f_2]$ could be changed adaptively according to different source converters. In line with these requirements, the adaptive characteristics can be introduced into a well known non-ideal resonant controller to achieve the improved adaptive resonant controller. As shown in Fig. 5.7, this adaptive controller can mimic Z_{ASVI} as

$$Z_{ASVI}(s) = -\frac{2K_r\left(2\pi f_{RC}\right)s}{s^2 + 2\left(2\pi f_{RC}\right)s + \left(2\pi f_{CS}\right)^2} \tag{5.10}$$

where f_{CS} is determined by the source converter and can be changed adaptively. f_{RC} is the bandwidth at $-3dB$ cut-off frequency of the $Z_{ASVI}(s)$, whose value is recommended as $5Hz$. $|Z_{ASVI}(s)|$ during $(f_{CS} - f_{RC},\quad f_{CS} + f_{RC})$ is equal to $\frac{K_r}{\sqrt{2}}$, whose value is not affected by f_{CS} and can choose $100\,\Omega$ as its initial value. It is worth pointing out that in most cases $\frac{K_r}{\sqrt{2}} = 100\,\Omega$ is large enough for $|Z_{ASVI}(s)|$ to avoid the intersection between $|Z_{iLS}(s)|$ and $|Z_{oS}(s)|$ during the whole load and input voltage range of the load converter. However, even

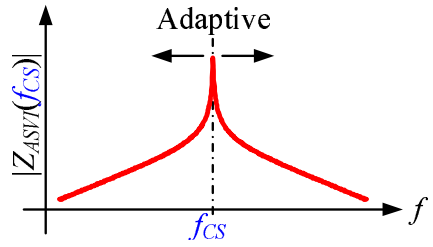


Figure 5.7: Characteristic of $|Z_{ASVI}(f_{CS})|$.

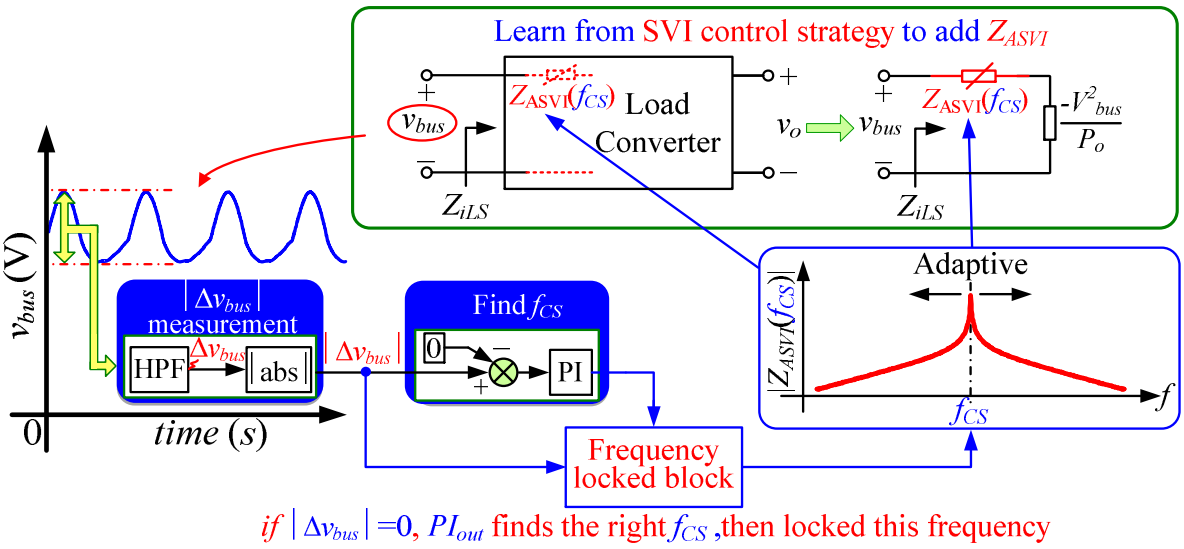


Figure 5.8: Basic idea of the adaptive approach of $Z_{ASVI}(f_{CS})$.

if it is not enough, K_r can be increased and tested by the user flexibly until the suitable K_r is found.

As discussed above, the realising of the adaptive virtual impedance $Z_{ASVI}(f_{CS})$ is the main aim of the proposed ASVI control strategy. According to Fig. 5.7, $Z_{ASVI}(f_{CS})$ is a function with respect to f_{CS}. Therefore, the key purpose of realising $Z_{ASVI}(f_{CS})$ is finding f_{CS} when the source converter changes. In order to solve this problem, this chapter utilises a similar adaptive approach to Chapter 4. As illustrated in Fig. 5.8, there are four basic steps to this adaptive approach. Firstly, $|\triangle v_{bus}|$ is sampled and sent to the positive input of a proportional–integral (PI) controller and compared with the PI negative input 0. Secondly, the output of the PI controller is set as f_{CS} of $Z_{ASVI}(f_{CS})$. Thirdly, as shown in (5.10) and the SVI control strategy in Chapter 3, $Z_{ASVI}(f_{CS})$ is added to the input port of the load converter via the control method. Finally, if $|\triangle v_{bus}|$ becomes 0, it indicates that $Z_{ASVI}(f_{CS})$ has found the right f_{CS} via the PI controller. At this point, a frequency-locked block begins

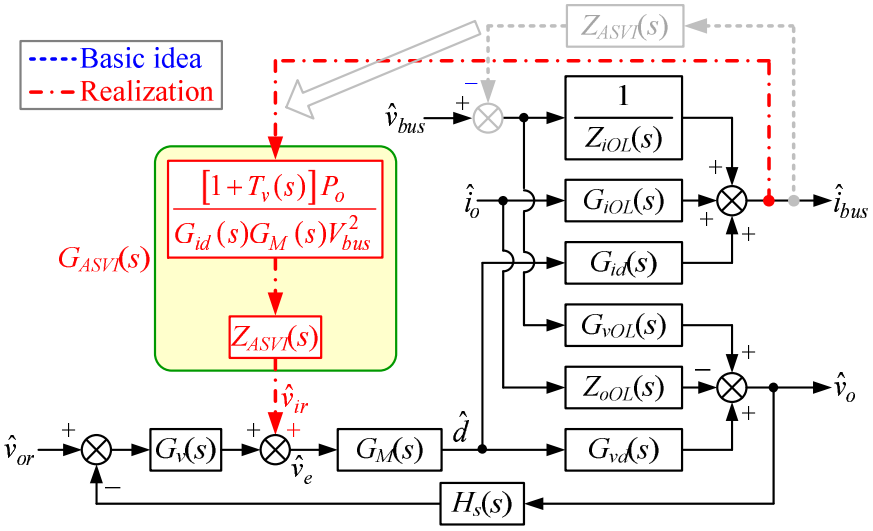


Figure 5.9: The ASVI control strategy

to lock the right f_{CS} for the $Z_{ASVI}(f_{CS})$. As a result, the above adaptive approach allows $Z_{ASVI}(f_{CS})$ to find the right f_{CS} when the source converter is changing.

It is worth pointing out that Fig. 5.8 not only shows the basic adaptive approach of realising $Z_{ASVI}(f_{CS})$, but also the main idea of latter proposed ASVI control strategy. Based on Fig. 5.8, the ASVI control strategy and its detailed realisation method will be discussed in Sections 5.3.2 and 5.3.3, respectively.

5.3.2 Concept of the ASVI Control Strategy

Fig. 5.9 shows the small-signal control block diagram of the original load converter. Its variables and transfer functions are described in Table 5.1 as well. If $Z_{ASVI}(s)$ is to be added to the series with the input port of the load converter, one intuitive method is to introduce $Z_{ASVI}(s)$ to the control block between the load input current and load input voltage (as shown by the dashed lines in Fig. 5.9). This is also the basic idea of the ASVI control strategy. However, this method cannot be achieved by control directly. In order to address this issue, the output of $Z_{ASVI}(s)$ is moved to the output of $G_v(s)$, adjusting the transfer function to $G_{ASVI}(s)$, as shown by the dot-dashed lines in 5.9. Here, Fig. 5.9 is the concept

Table 5.1: Variables and transfer functions of load converter

$\hat{v}_{bus}$	Perturbation of the bus voltage
$\hat{i}_o$	Perturbation of the load current
$\hat{i}_{bus}$	Perturbation of the bus current
$\hat{d}$	Perturbation of the duty cycle
$\hat{v}_o$	Perturbation of the output voltage
$\hat{v}_{or}$	Perturbation of the output voltage reference
$G_v(s)$	Transfer function of the voltage regulator
$G_M(s)$	Transfer function of the modulator
$Z_{iOL}(s)$	Open-loop input impedance
$G_{vd}(s)$	Control to output voltage transfer function
$G_{id}(s)$	Control to input current transfer function
$Z_{oOL}(s)$	Open-loop output impedance
$H_s(s)$	Sampling coefficient of the output voltage
$G_{iOL}(s)$	Open-loop load to input current transfer function
$G_{vOL}(s)$	Open-loop input to output voltage transfer function

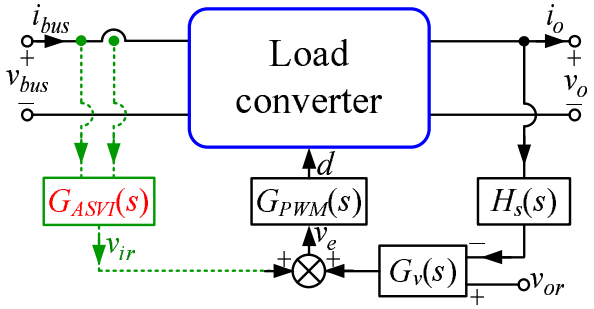


Figure 5.10: Control system of the load converter with the ASVI control strategy.

of the ASVI control strategy and $G_{ASVI}(s)$ is expressed as:

$$\begin{aligned} G_{ASVI}(s) &= Z_{ASVI} \cdot \frac{[1+T_v(s)]P_o}{G_{id}(s)G_M(s)V_{bus}^2} \\ &= \frac{-2K_r(2\pi f_{RC})s}{s^2+2(2\pi f_{RC})s+(2\pi f_{CS})^2} \cdot \frac{[1+T_v(s)]P_o}{G_{id}(s)G_M(s)V_{bus}^2} \end{aligned} \tag{5.11}$$

where $T_v(s) = H_s(s)G_v(s)G_M(s)G_{vd}(s)$ is the loop gain of the voltage closed-loop of the load converter.

Note: since the derivation of $G_{ASVI}(s)$ is very similar to $G_{SVI}(s)$ in Chapter 3, it will not be repeated here.

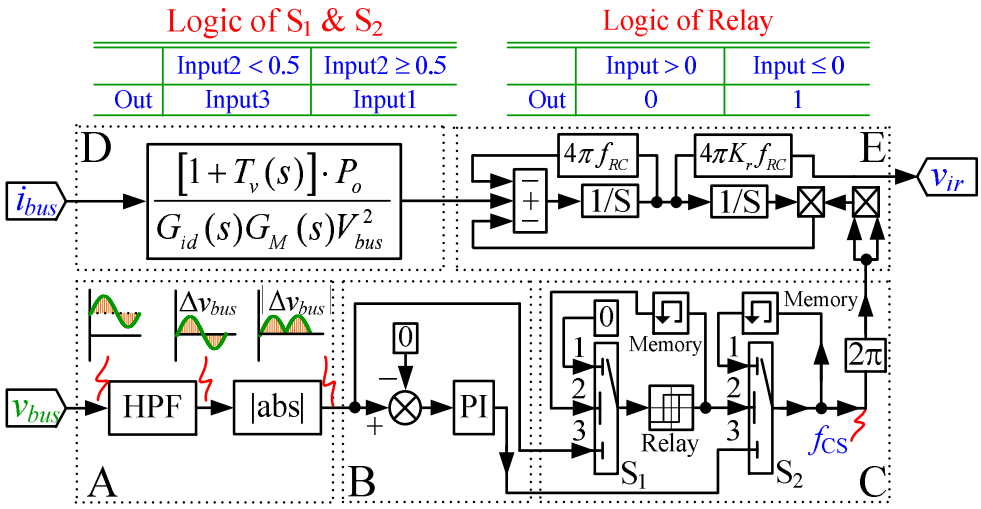


Figure 5.11: Realisation of $G_{ASVI}(s)$.

5.3.3 Realisation of the ASVI Control Strategy

According to Fig. 5.9, the control system of the load converter with the ASVI control strategy is further presented in Fig. 5.10. In contrast to the control system of the original load converter, the ASVI control strategy adds only $G_{ASVI}(s)$ to the original control system (as shown with dashed lines in Fig. 5.10). Therefore, realising $G_{ASVI}(s)$ is the key to the ASVI control strategy. In addition, as shown in Fig. 5.10, both i_{bus} and v_{bus} are sampled to help achieve $G_{ASVI}(s)$ in practice.

According to (5.11) and Fig. 5.9, $G_{ASVI}(s)$ can be achieved by Fig. 5.11. As shown in Fig. 5.11, in Part A, v_{bus} first goes through a high-pass filter $\frac{s}{s+15}$ and an absolute value block to extract $\triangle v_{bus}$. Following this, $|\triangle v_{bus}|$ is sent to Part B and compared with zero, whilst, its error is amplified by a proportional–integral (PI) controller. If the system is unstable, the output of this PI controller is increased from zero, regulating the centre frequency of $Z_{ASVI}(s)$. If the output of the PI controller arrives at f_{CS}, $Z_{ASVI}(s)$ will find its right frequency characteristics, stabilise the cascaded system and make $|\triangle v_{bus}| = 0$. Then according to Part C, the input 3 of S_1 is equal to 0 $\rightarrow$ the output of S_1 becomes 0 $\rightarrow$ the output of *Relay* changes to 1 $\rightarrow$ the input 2 of S_1 changes to 1 $\rightarrow$ the output of S_1 is changed to the input 1 of S_1 and becomes 0 again$\rightarrow$ the output of *Relay* is locked as 1, which locks the output of S_2 as the final centre frequency of $Z_{ASVI}(s)$ and does not change it during the remaining running time. At the same time, i_{bus} is sent to Part D to realise $\frac{[1+T_v(s)]P_o}{G_{id}(s)G_{PWM}(s)V_{bus}^2}$. Then, the output of Part D is sent to Part E, where $Z_{ASVI}(s)$ can be achieved by taking

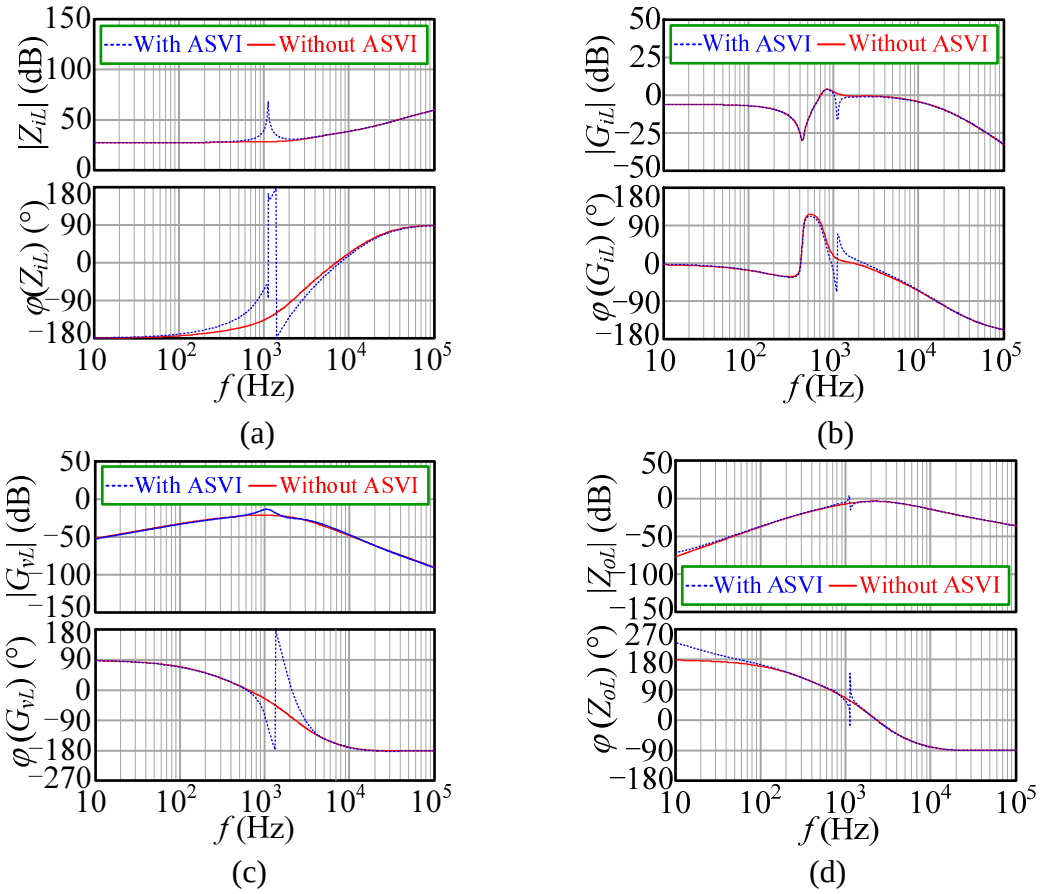


Figure 5.12: Bode plots of the load converter with/without the ASVI control strategy: (a) $Z_{iL}(s)$; (b) $G_{iL}(s)$; (c) $G_{vL}(s)$; (d) $Z_{oL}(s)$.

its centre frequency from Part C. Finally, the output of $G_{ASVI}(s)$ can be obtained from the output of Part E. It is worth pointing out that, according to the analysis in Chapter 4, in order to ensure $Z_{ASVI}(s)$ finds f_{CS} effectively, too large K_p and K_i parameters should be avoided during the design process of the PI controller in Part B. In addition, as Chapter 4 has described how the PI control scheme is used to get the frequency adaptive scheme of the $Z_{ASVI}(s)$, it is only briefly explained here.

In summary, the proposed ASVI control strategy can be realised by Figs. 5.10 and 5.11.

5.3.4 Impact of the ASVI Control Strategy on the Load Converter

The performance of the load converter can be evaluated using two-port network analysis with four typical transfer functions (Arnedo, 2008): the closed-loop input impedance $Z_{iL}(s)$, the closed-loop load to input current transfer function $G_{iL}(s)$, the closed-loop input to out-

put voltage transfer function $G_{vL}(s)$ and the closed-loop output impedance $Z_{oL}(s)$. Therefore, to evaluate the impact of the ASVI control strategy on the load converter in a clear way, the Bode plots of $Z_{iL}(s) \sim Z_{oL}(s)$ of a specific load converter with/without the ASVI control strategy are depicted in Fig. 5.12. Here, the source and load converters correspond to the source converter I and the load converter in Fig. 5.13.

According to Fig. 5.12, though the proposed ASVI control strategy changes the features of $Z_{iL}(s) \sim Z_{oL}(s)$, it keeps most of the dynamic performance of the original load converter. This phenomenon can be explained as follows: since $Z_{ASVI}(s)$ only plays its role during $[f_1,\ f_2]$, but becomes zero outside $[f_1,\ f_2]$, the ASVI control strategy only affects the performance of the load converter during $[f_1,\ f_2]$. As a result, the ASVI control strategy can be considered an acceptable stabilisation method for the load converter.

5.4 Experimental Verification

In this section, the ASVI control strategy is applied to a 100 W unstable cascaded system, which contains one load converter and three different source converters. As shown in Fig. 5.13, the source converter I is a 100 V - 48 V / 50 kHz Buck converter, source converters II & III are two different *LC* input filters, and the load converter is a 48 V-24 V / 20 kHz Buck converter. Here, in order to compare the ASVI control strategy and the APVI control strategy, the source converters II & III and the load converter are the same as the converters in the experimental system of Chapter 4. The main circuit and parameters of the experimental system are also presented in Fig. 5.13. For convenience, the system is referred to work at Cases I, II and III when the load converter is connected to source converters I, II and III, respectively.

In Case I, the Bode plots of the cascaded system when the input voltage of the load converter is varied between 80% rated input voltage ($38.4V$) and 120% rated input voltage ($57.6V$) are presented in Figs. 5.14(a) and (b), where Z_{oS}, Z_{iL} and Z_{iLS} are the output impedance of the source converter, the original load input impedance and the load input impedance with the ASVI control strategy, respectively. As seen, when v_{bus} is changed from $38.4V$ to $57.6V$, though $|Z_{iL}(s)|$ is intersected with $|Z_{oS}(s)|$, $|Z_{iLS}(s)|$ is always larger than $|Z_{oS}(s)|$. Similarly, the Bode plots of the experimental system at Case I when the load

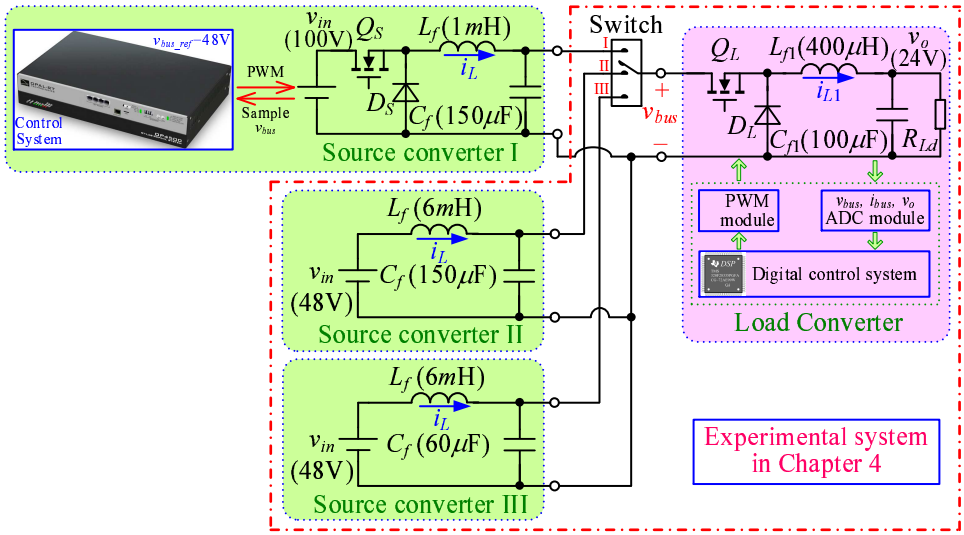


Figure 5.13: The experimental system.

is varied during 10% full load (10W) and 100% full load (100W) are presented in Figs. 5.14(c) and (d). It can be noted that, when p_o varies from 10W to 100W, the ASVI control strategy can ensure a total separation between $|Z_{oS}(s)|$ and $|Z_{iLS}(s)|$ as well.

The experimental results in Case I of the cascaded system are given in Fig. 5.15. Fig. 5.15(a) shows the unstable cascaded system can be regulated to a stable system by the ASVI control strategy. In addition, by Figs. 5.15(b) and (c), the cascaded system can work well with the ASVI control strategy whether during input voltage changing or load changing process. One might ask if the ASVI control strategy cannot find its right centre frequency, what will happen to the cascaded system. Is the oscillation of the cascaded system serious or mitigated? To answer these questions, two definitions are firstly defined: 1) the wrong ASVI control strategy — the ASVI control strategy with a wrong centre frequency; 2) the right ASVI control strategy — the ASVI control strategy with a right centre frequency. Fig. 5.16 presents the simulation waveforms in Case I of the cascaded system with the wrong and right ASVI control strategies. In Fig. 5.16, the cascaded system works without ASVI control strategy before 0.2s. During $[0.2s,\ \ 0.25s]$, the cascaded system works with a wrong ASVI control strategy. After 0.25s, the cascaded system works with a right ASVI control strategy. Three conclusions can be obtained from Fig. 5.16: 1) the cascaded system is unstable without the ASVI control strategy; 2) even if the ASVI does not find its right centre frequency, it will not make the system more unstable, but still can suppresses the

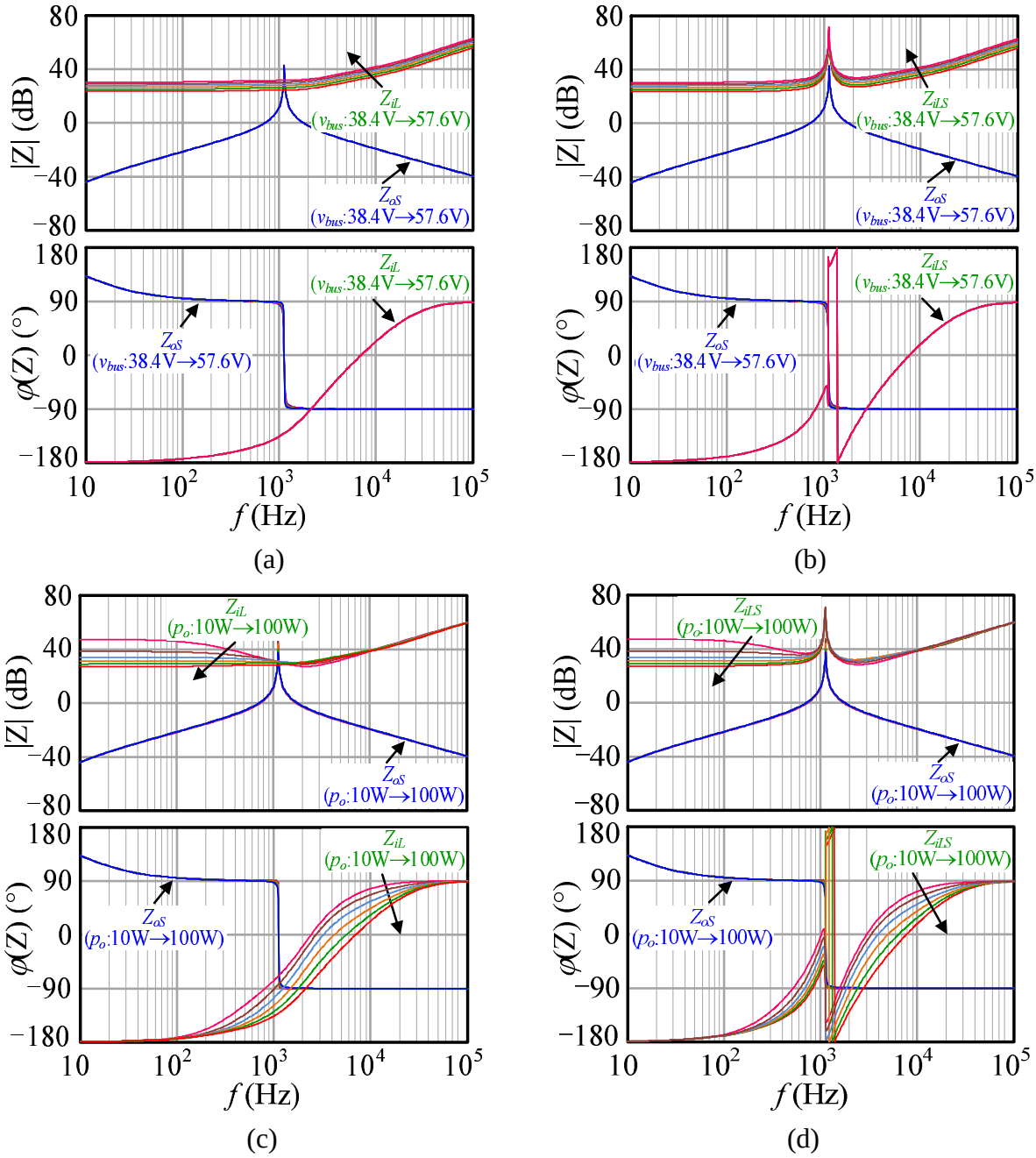
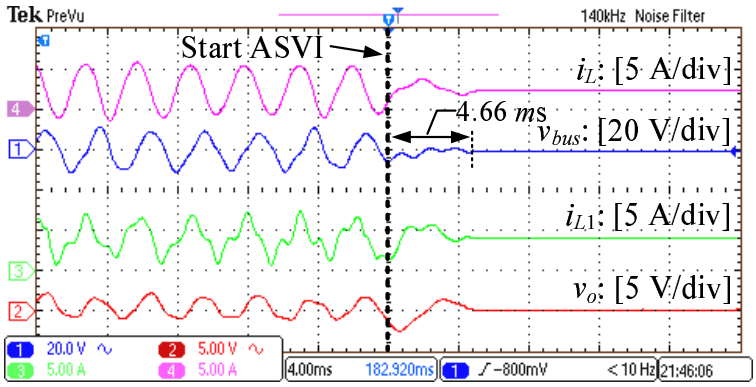
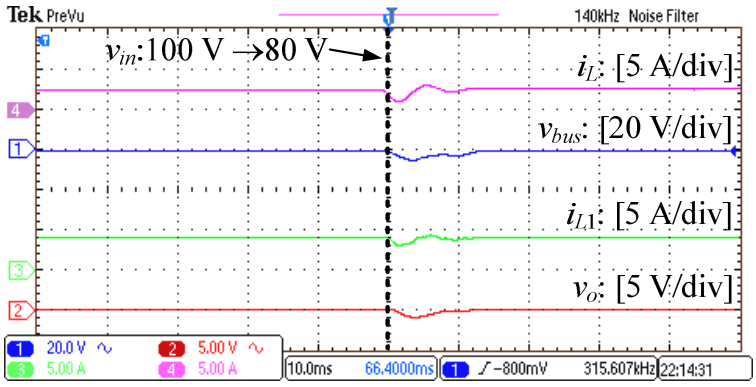


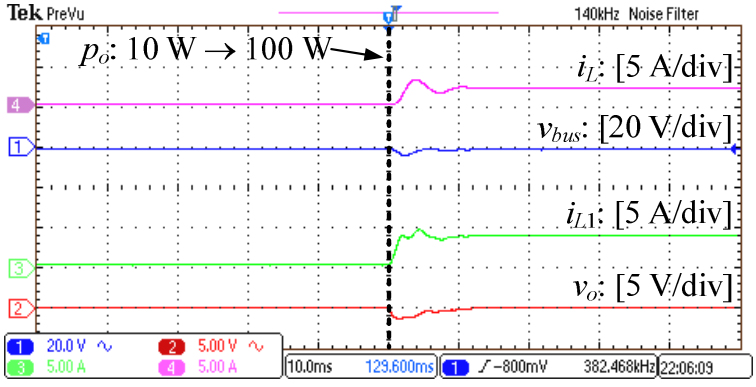
Figure 5.14: Bode plots in Case I of the experimental system with different working conditions: (a) without the ASVI control strategy, $v_{bus}: 38.4V \rightarrow 57.6V$, $p_o = 100W$; (b) with the ASVI control strategy, $v_{bus}: 38.4V \rightarrow 57.6V$, $p_o = 100W$; (c) without the ASVI control strategy, $v_{bus} = 48V$, $p_o: 10W \rightarrow 100W$; (d) with the ASVI control strategy, $v_{bus} = 48V$, $p_o: 10W \rightarrow 100W$.



(a)



(b)



(c)

Figure 5.15: Experimental waveforms in Case I of the cascaded system: (a) steady state waveforms with rated input voltage and rated load, (b) dynamic waveforms when the input voltage steps down from 100% rated to 80% rated voltage at full load, (c) dynamic waveforms when the load increases from 10% rated to 100% rated load at rated input voltage.

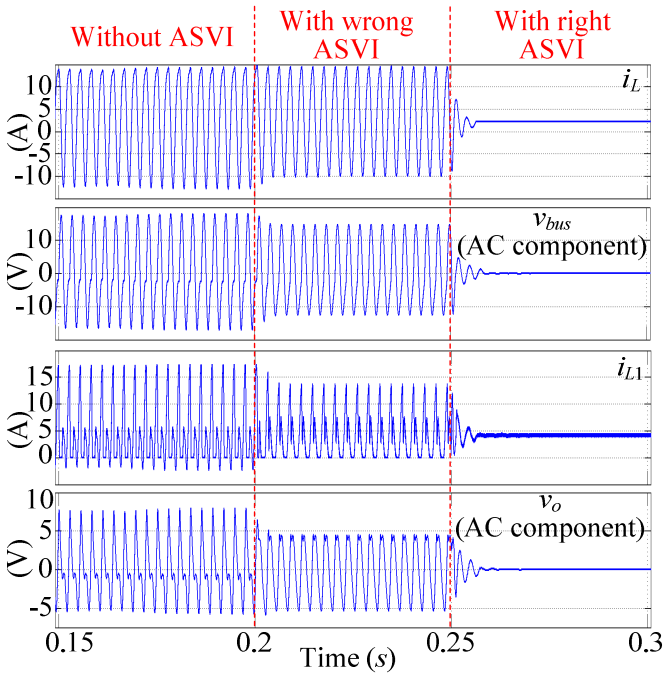


Figure 5.16: Simulation waveforms in Case I of the cascaded system with the wrong and right ASVI control strategies.

system oscillation; 3) if the ASVI finds its right centre frequency, the cascaded system can become stable.

Similarly, both the Bode plots and experimental results in Cases II & III are given in Figs. 5.17 $\sim$ 5.18 and Figs. 5.20 $\sim$ 5.21, respectively. In both cases, the ASVI control strategy can ensure a total separation of $|Z_{oS}(s)|$ and $|Z_{iLS}(s)|$ and make the whole system work well both at steady-state and in dynamic conditions. It is worth pointing out that compared to the experimental results in Chapter 4, in Cases II and III, the APVI method requires 45.56 ms and 32.2 ms to stabilise the unstable system, respectively, but the ASVI method needs only 20.08 ms and 8.79 ms. Moreover, in Cases II and III, the ASVI control method reduces both the overshoot and regulation time of the load converter when its input voltage and load changing. Therefore, the ASVI control strategy is superior to the APVI control strategy.

The simulation waveforms in Cases II and III with the wrong and right ASVI control strategies are also presented at Figs. 5.19 and 5.22, respectively. In both cases, the cascaded system is unstable without the ASVI control strategy. However, even if the ASVI does not find its right centre frequency, the ASVI control strategy will not make the system more

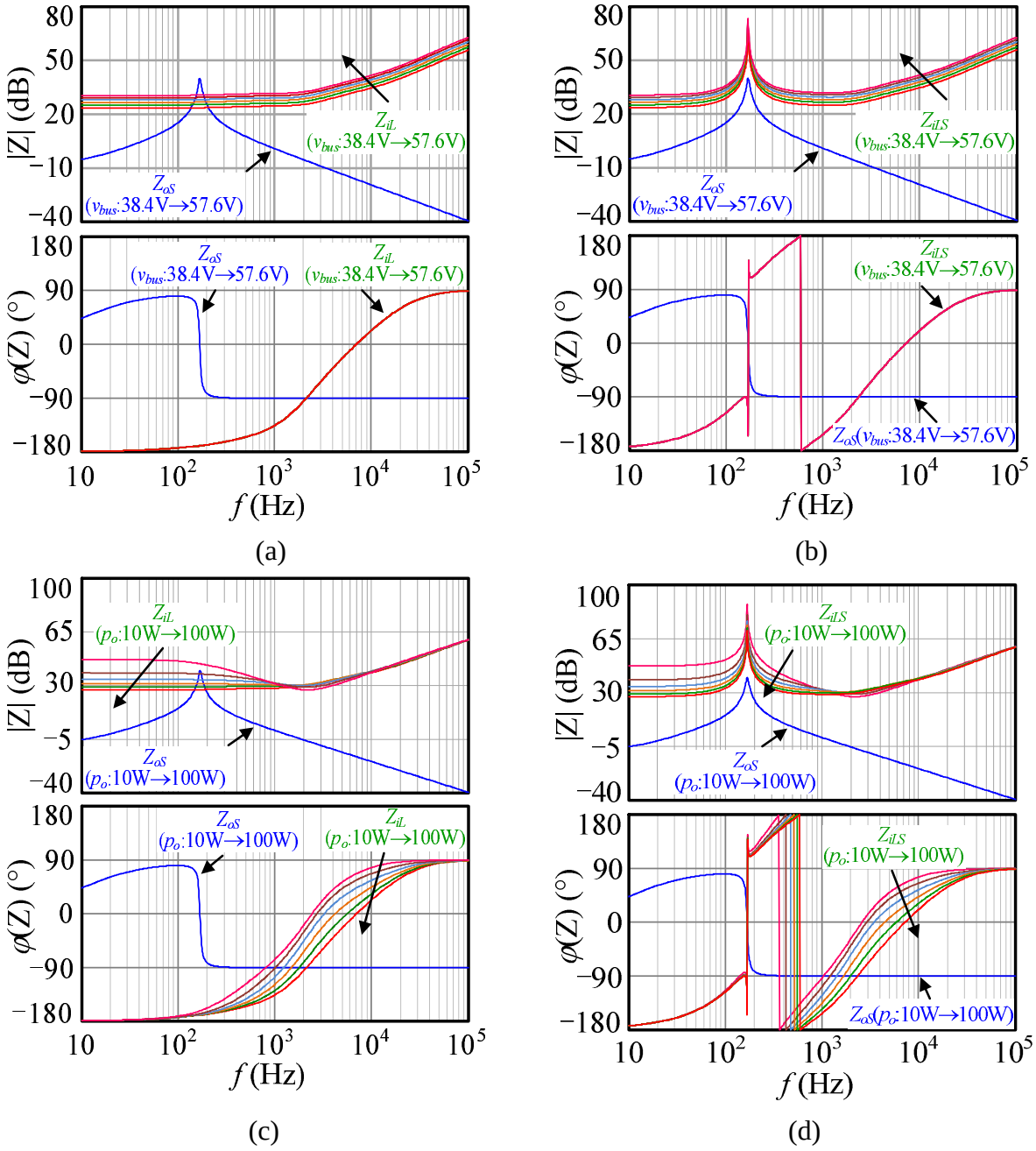


Figure 5.17: Bode plots in Case II of the experimental system with different working conditions: (a) without the ASVI control strategy, $v_{bus}: 38.4V \rightarrow 57.6V$, $p_o = 100W$; (b) with the ASVI control strategy, $v_{bus}: 38.4V \rightarrow 57.6V$, $p_o = 100W$; (c) without the ASVI control strategy, $v_{bus} = 48V$, $p_o: 10W \rightarrow 100W$; (d) with the ASVI control strategy, $v_{bus} = 48V$, $p_o: 10W \rightarrow 100W$.

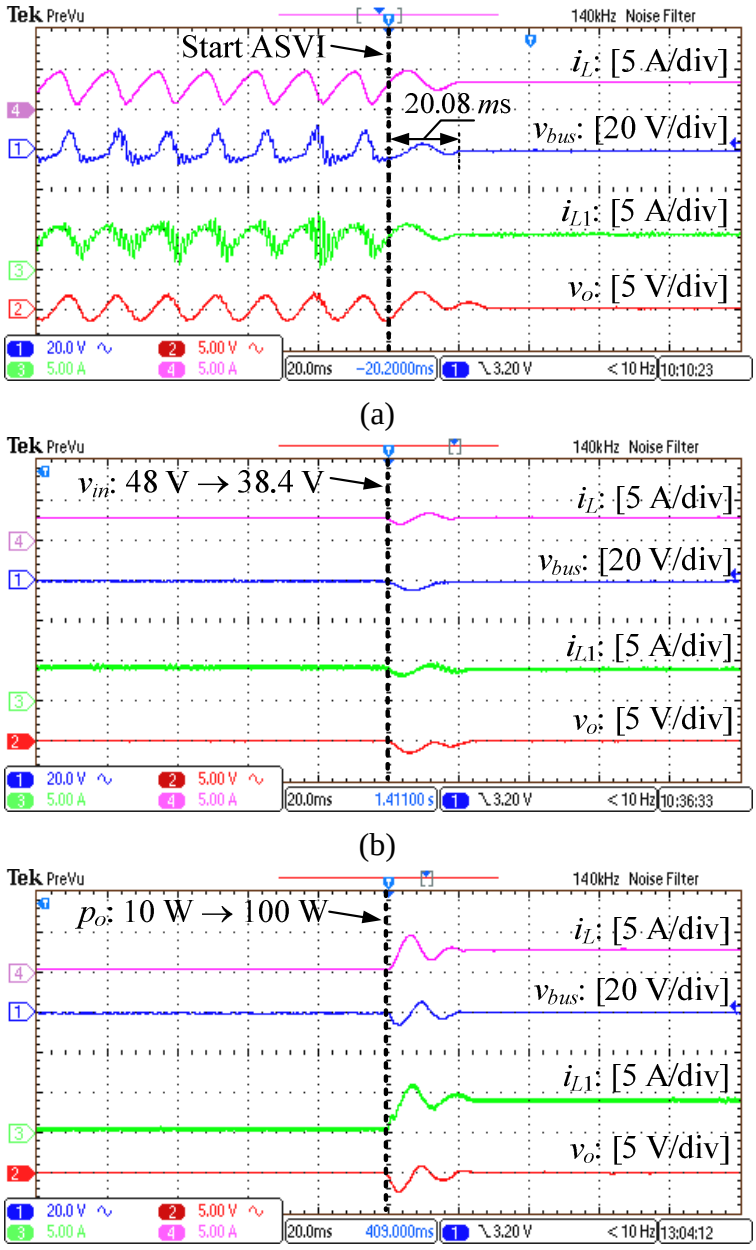


Figure 5.18: Experimental waveforms in Case II of the cascaded system: (a) steady state waveforms with rated input voltage and rated load, (b) dynamic waveforms when the input voltage steps down from 100% rated to 80% rated voltage at full load, (c) dynamic waveforms when the load increases from 10% rated to 100% rated load at rated input voltage.

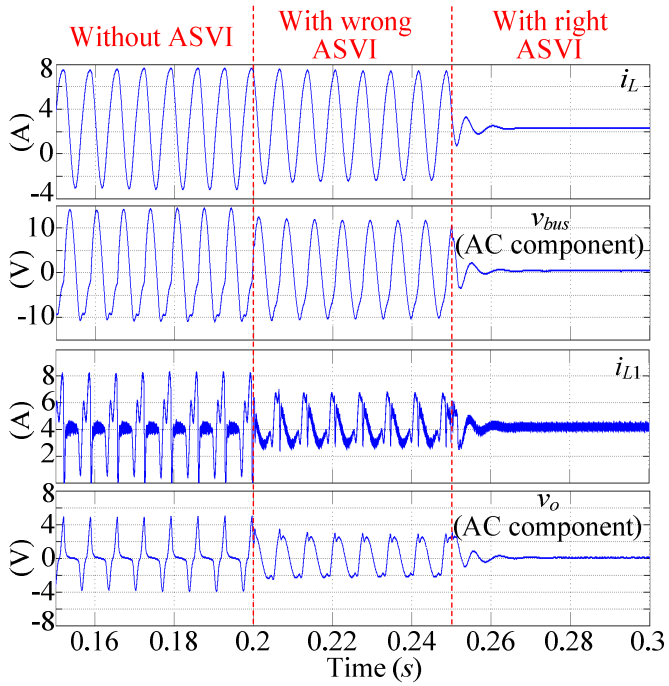


Figure 5.19: Simulation waveforms in Case II of the cascaded system with the wrong and right ASVI control strategies.

unstable, but can still suppress the system oscillation. In addition, when the ASVI finds the right centre frequency, the cascaded system becomes stable.

According to Fig. 5.14 $\sim$ Fig. 5.21, the ASVI control strategy can not only stabilise the load converter cascaded with a *LC* input filter, but also the load converter cascaded with a Buck converter. These experimental results also can be explained by the theory. Fig. 5.10 illustrates that the ASVI controller $G_{ASVI}(s)$ needs only the information of i_{bus} and v_{bus} to shape the input impedance of the load converter, thus, it is independent of the internal structure of the source converters. Therefore, no matter the source converter is a *LC* input filter or Buck converter, the same information (i_{bus} and v_{bus}) is provided to $G_{ASVI}(s)$ to help the ASVI control strategy stabilise the whole system. The above experimental results also show that the ASVI control strategy is feasible and effective in practice.

5.5 Summary

SAC and SPC, two typical load shaping stabilisation methods, are analysed and compared in this chapter. This analysis reveals that although both SAC and SPC can stabilise the

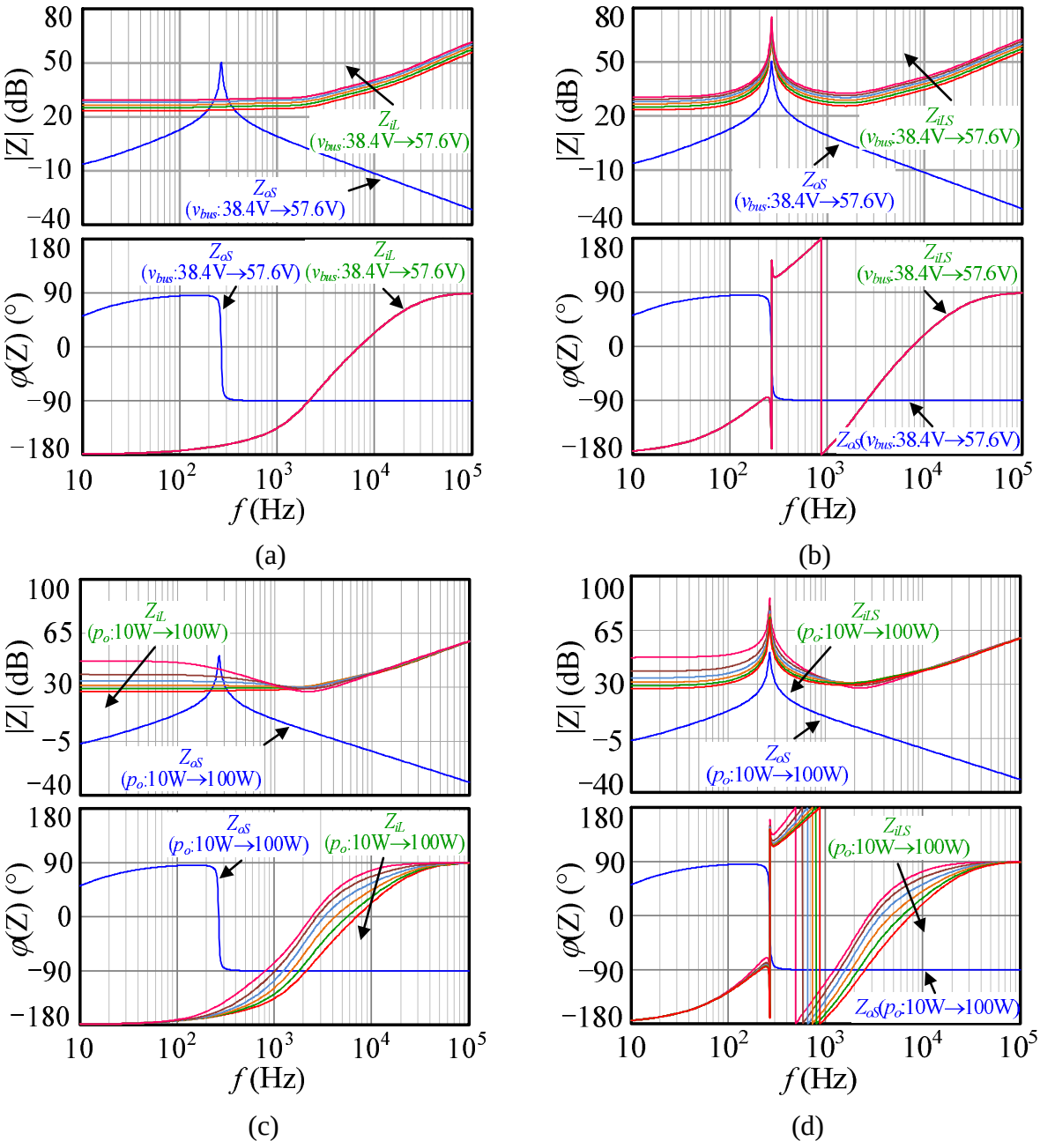
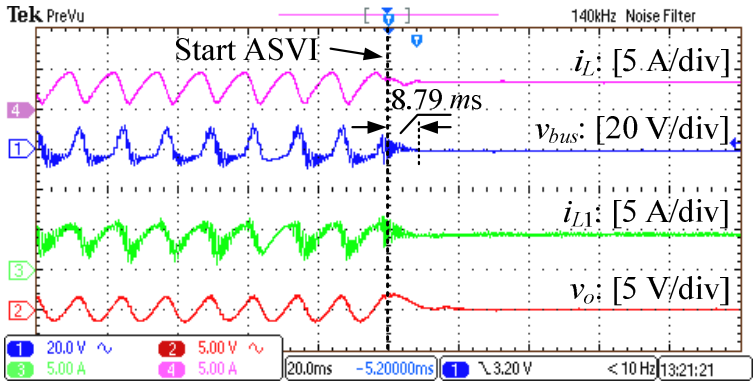
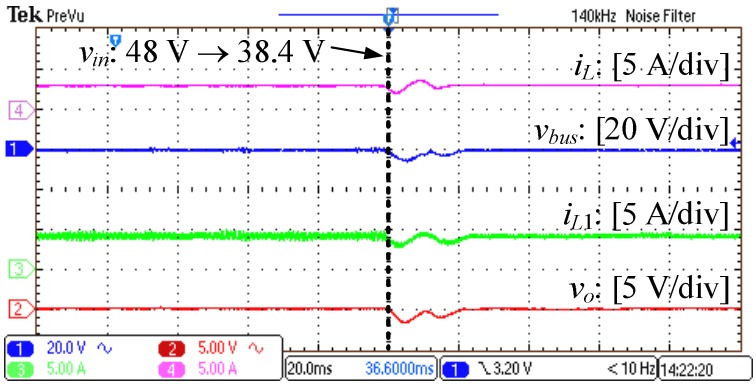


Figure 5.20: Bode plots in Case III of the experimental system with different working conditions: (a) without the ASVI control strategy, $v_{bus}: 38.4V \rightarrow 57.6V$, $p_o = 100W$; (b) with the ASVI control strategy, $v_{bus}: 38.4V \rightarrow 57.6V$, $p_o = 100W$; (c) without the ASVI control strategy, $v_{bus} = 48V$, $p_o: 10W \rightarrow 100W$; (d) with the ASVI control strategy, $v_{bus} = 48V$, $p_o: 10W \rightarrow 100W$.



(a)



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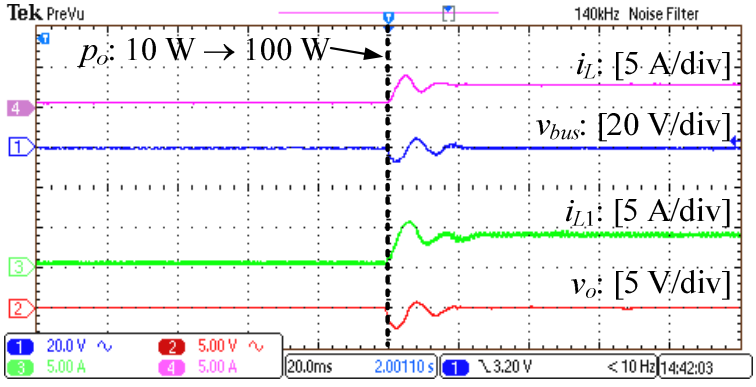


(c)

Figure 5.21: Experimental waveforms in Case III of the cascaded system: (a) steady state waveforms with rated input voltage and rated load, (b) dynamic waveforms when the input voltage steps down from 100% rated to 80% rated voltage at full load, (c) dynamic waveforms when the load increases from 10% rated to 100% rated load at rated input voltage.

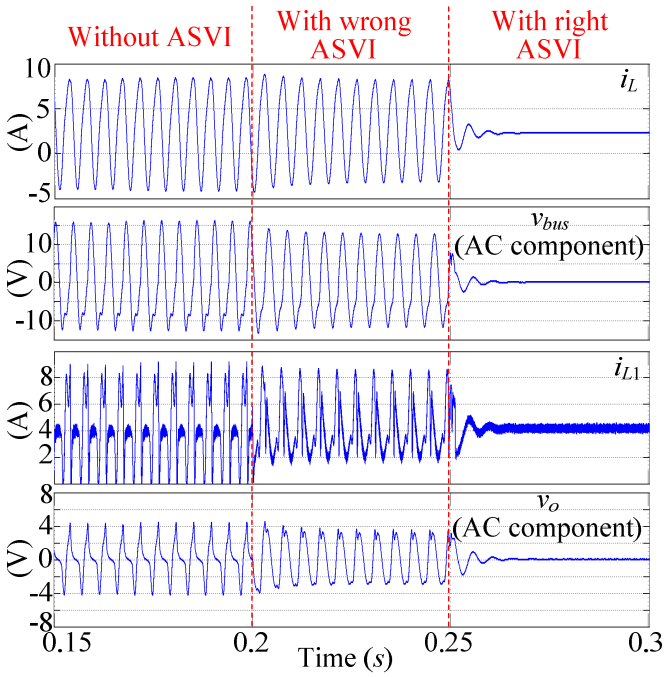


Figure 5.22: Simulation waveforms in Case III of the cascaded system with the wrong and right ASVI control strategies.

cascaded system, the system utilising the SAC is unconditionally stable, but conditionally stable when utilising the SPC. The cascaded system with SAC is therefore more stable than that with SPC. In addition, as the SAC can be realised by both the PVI and SVI control strategies, the PVI/SVI control strategies are also compared here. The results shows that the PVI control strategy has inevitable limitations when realising the SAC during the whole load and input voltage range of the load converter, but that the SVI control strategy does not have limitations. Therefore, the SVI control strategy is more suitable for the SAC than the PVI control strategy. Moreover, in order to stably connect the load converter to different source converters, such as *LC* input filters and traditional DC/DC converters, without changing its internal structure, an ASVI control strategy is further proposed in this chapter. This proposed ASVI control strategy allows the load converter can shape its input impedance to stabilise the cascaded system with different source converters. Finally, the ASVI strategy has been experimentally verified on a cascaded system composed by a load converter and three different source converters.

Chapter 6

Improved ASVI Control with Minimum Ripple Point Tracking for the Load Converter

The ASVI control strategy is an attractive load stabilisation method for cascaded systems thanks to its adaptive capacity for different source converters and better performance for load converters. However, as discussed in Chapters 4 and 5, this ASVI control strategy has a potential problem in that, as it utilises a proportional-integral (PI) controller to find the centre frequency of the ASVI, the PI controller may miss it with excessive proportional or integral coefficients, leading to the failure of the ASVI control strategy. Although this potential problem may not arise with small proportional and integral coefficients, it is a potential issue for the ASVI control strategy. To make the ASVI control strategy more reliable, a minimum-ripple-point-tracking (MRPT) controller is proposed in this chapter to replace the original PI controller. With the MRPT controller, the centre frequency of ASVI is found via the perturb and observe (P&O) algorithm, which ensures the ASVI control strategy does not have the potential for this problem. Furthermore, in order to quickly find the centre frequency of ASVI, the sinusoidal-tracking-algorithm (STA) is further incorporated into the MRPT controller to improve its processing speed. Finally, a load converter cascaded with different *LC* input filters is fabricated to validate the effectiveness of the proposed MRPT controller.

6.1 The ASVI Control Strategy and the Motivation of the MRPT Controller

6.1.1 Review of the ASVI Control Strategy

According to Chapter 5, there are three basic purposes of the ASVI control strategy: (a) make a total separation between $|Z_{iL}|$ and $|Z_{oS}|$ (See Fig. 6.1(a)); (b) only increase $|Z_{iL}|$ during a very small frequency range (See Fig. 6.1(a)); (c) change $|Z_{iL}|$ adaptively according to different source converters. Each of these purposes brings its own benefit to the ASVI control strategy. The first purpose ensures the cascaded system works as an unconditionally stable system whose system loop gain Z_{oS}/Z_{iL} always stays inside the unit cycle as shown in Fig. 6.1(b). The second purpose guarantees that the ASVI control strategy can stabilise the cascaded system with minimised load performance compromise. The final purpose is for the load converter to stably connect to different source converters without changing its internal structure. The above benefits make the ASVI control strategy the more competitive among the existing stabilisation methods of the cascaded system.

In theory, the ASVI control strategy can be realised by adding an adaptive virtual impedance Z_{ASVI} into the series with the load input port. As shown in Fig. 6.1(c), the improved load input impedance Z_{iLS} can be expressed as

$$Z_{iLS} = Z_{ASVI} + Z_{iL} \tag{6.1}$$

where $Z_{iL} = -V_{bus}^2/P_o$. Here, V_{bus} and P_o are the input voltage and output power of the load converter, respectively.

According to Fig. 6.1(a), Z_{iLS} should satisfy:

$$If\{f \in [f_1,\, f_2]\} \quad \rightarrow \quad |Z_{iLS}| > |Z_{oS}| \tag{6.2}$$

$$If\{f \notin [f_1,\, f_2]\} \quad \rightarrow \quad Z_{iLS} = Z_{iL} \tag{6.3}$$

where f_1 and f_2 are the intersection frequencies of $|Z_{iL}|$ and $|Z_{oS}|$ as shown in Fig. 6.1(a).

As observed in Chapter 5, in order to ensure that $|Z_{iL}|$ successfully becomes $|Z_{iLS}|$,

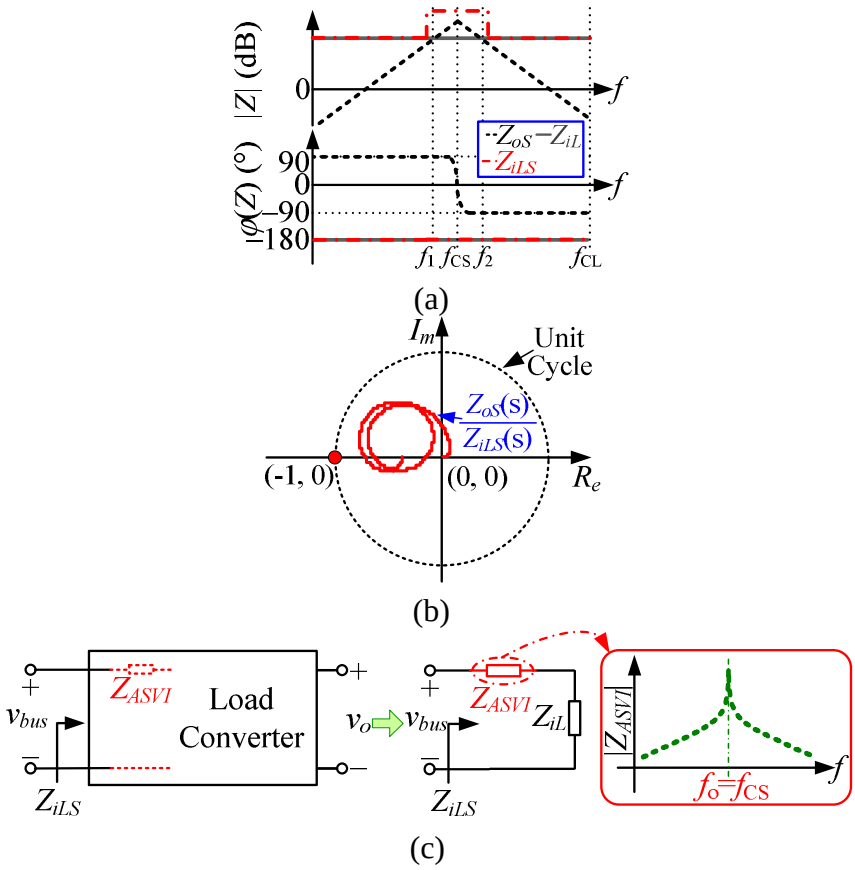


Figure 6.1: Purposes and concept of the ASVI control strategy: (a) purposes of the ASVI control strategy — described by Bode plots; (b) purposes of the ASVI control strategy — described by Nyquist curve; (c) concept of the ASVI control strategy.

Z_{ASVI} can be selected as

$$Z_{ASVI}(s) = -\frac{2K_r(2\pi f_{RC})s}{s^2 + 2(2\pi f_{RC})s + (2\pi f_{CS})^2} \tag{6.4}$$

where f_{CS} is the cut-off frequency of the source converter and is also the centre frequency of Z_{ASVI}. By Fig. 6.1(a), f_{CS} is very close to f_1 and f_2. f_{RC} is the bandwidth at $-3dB$ cut-off frequency of the $Z_{ASVI}(s)$. During $(f_{CS}-f_{RC},\quad f_{CS}+f_{RC})$, $|Z_{ASVI}(s)| = K_r/\sqrt{2}$. As noted in Chapter 5, both f_{RC} and K_r are flexible determined by the user and their initial values are recommended as $5Hz$ and 100Ω, respectively. The characteristics of Z_{ASVI} are also presented in Fig. 6.1(c).

According to (6.4) and Fig. 6.1(c), Z_{ASVI} has three characteristics: (a) when $f \in [f_1,\ f_2]$, $|Z_{ASVI}|$ is large enough to ensure a total separation of $|Z_{iLS}|$ and $|Z_{oS}|$; (b) when $f \notin [f_1,\ f_2]$, $|Z_{ASVI}|$ is small enough to minimise the impact of the ASVI control strategy on the original

load converter; (c) when the source converters changes, $|Z_{ASVI}|$ only needs to regulate its centre frequency to the new f_{CS} to adapt to this change. Therefore, conceptually, the ASVI control strategy indeed can be realised perfectly by adding Z_{ASVI} to the series, with the load input impedance shown in Fig. 6.1(c).

It is clear that realising Z_{ASVI} is the key point of the ASVI control strategy. As discussed in Chapter 5, this Z_{ASVI} can be realised by adding an impedance regulator $G_{ASVI}(s)$ to the original load converter. 6.2 illustrates that $G_{ASVI}(s)$ samples the input voltage and current of the load converter and adds its output to the output of the voltage regulator $G_v(s)$. Here, $G_{ASVI}(s)$ can be expressed as

$$G_{ASVI}(s) = Z_{ASVI}(s) \cdot \frac{[1+T_v(s)]P_o}{G_{id}(s)G_M(s)V_{bus}^2} \tag{6.5}$$

where $T_v(s)$ is the loop gain of the voltage closed-loop of the original load converter; $G_{id}(s)$ is the control to the input current transfer function of the original load converter; and $G_M(s)$ is the modulator transfer function of the original load converter.

To ensure $G_{ASVI}(s)$ can realise $Z_{ASVI}(s)$ and especially can find f_{CS} adaptively, a specific control circuit for $G_{ASVI}(s)$ is proposed in Chapter 5. As shown in Fig. 6.3(a), this control circuit contains five parts and operates as follows.

In Part A, v_{bus} first goes through a high-pass-filter (HPF) and an absolute value block to extract $|\triangle v_{bus}|$. Following this, $|\triangle v_{bus}|$ goes through Parts B and C to find f_{CS} adaptively. As shown in Figs. 6.3(a) and (b), the adaptive mechanism of Parts B and C can be explained as: in Part B, $|\triangle v_{bus}|$ is firstly compared with 0, whilst, its error is amplified by a PI controller. Therefore, the output of the PI controller, PI_{out}, can be expressed as:

$$PI_{out}(t) = K_p\,|\triangle v_{bus}(t)| + K_i \int_0^t |\triangle v_{bus}(t)|\,dt \tag{6.6}$$

where K_p and K_i are the proportional and integral coefficients of PI controller, respectively.

According to (6.6), if the system is unstable, $|\triangle v_{bus}| > 0$, PI_{out} is increased from zero. By Fig. 6.3(a), PI_{out} also decides the centre frequency of $Z_{ASVI}(s)$. Therefore, once PI_{out} is increased to f_{CS}, $Z_{ASVI}(s)$ will find its right centre frequency, stabilise the cascaded system and make $|\triangle v_{bus}| = 0$. Then, as observed in Part C and Fig. 6.3(b), the input 3 of S_1 is equal to $0 \rightarrow$ the output of S_1 becomes $0 \rightarrow$ the output of *Relay* changes to $1 \rightarrow$ the input

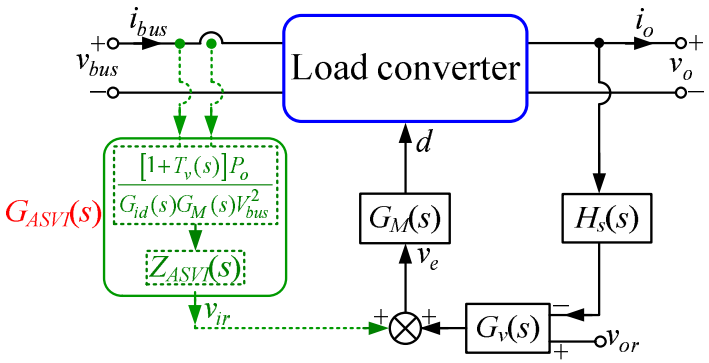
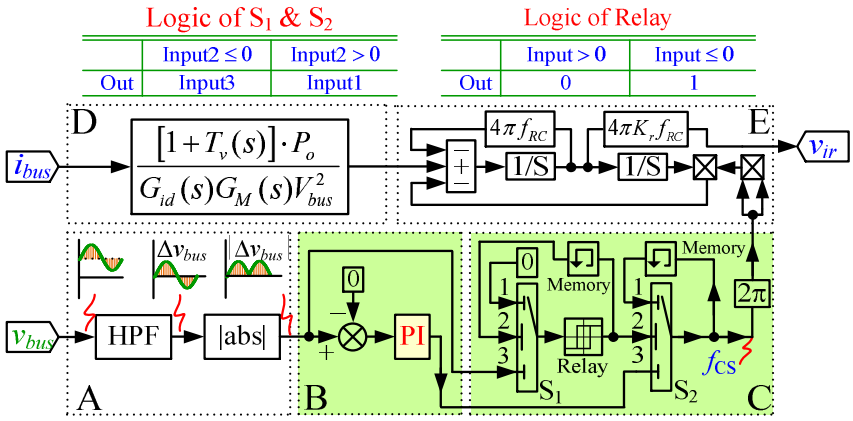
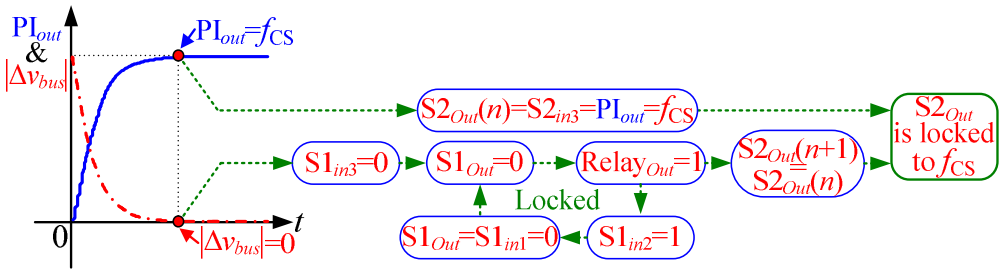


Figure 6.2: Realisation of the ASVI control strategy via adding $G_{ASVI}(s)$.



(a)



(b)

Figure 6.3: Realisation of the $G_{ASVI}(s)$: (a) control circuit of $G_{ASVI}(s)$; (c) adaptive mechanism of $G_{ASVI}(s)$.

2 of S_1 changes to 1 $\rightarrow$ the output of S_1 is changed to the input 1 of S_1 and becomes 0 again$\rightarrow$ the output of *Relay* is locked as 1. Therefore, the output of S_2, $S2_{Out}$, is always equal to its previous value

$$S2_{Out}(n+1) = S2_{Out}(n) = f_{CS} \tag{6.7}$$

where $n+1$ and n represent the time $n+1$ and its previous time n, respectively. Both of them are after PI_{out} finding f_{CS}.

According to Fig. 6.3 and (6.7), as $S2_{Out}$ is equal to f_{CS} before the relay is locked, the centre frequency of $Z_{ASVI}(s)$ is finally locked as f_{CS} and will not be changed further. At the same time, i_{bus} is sent to Part D to realise $\frac{[1+T_v(s)]P_o}{G_{id}(s)G_{PWM}(s)V_{bus}^2}$. Then, both the outputs of Parts C and D are sent to Part E, where the $Z_{ASVI}(s)$ can be achieved. Finally, the output of $G_{ASVI}(s)$ can be obtained from the output of Part E.

Note that in the ASVI control strategy, the PI controller plays an important role in helping $G_{ASVI}(s)$ find f_{CS} adaptively.

6.1.2 Potential Problem of the ASVI Control Strategy

As described in Section 6.1.1, the PI controller is the key controller for helping the ASVI control strategy to find the centre frequency of ASVI. However, as discussed in Chapter 5, if K_p or K_i is too large, the PI controller may miss the right frequency and cause the failure of the ASVI control strategy. This is a potential problem of the ASVI control strategy.

As shown in Fig. 6.4(a), when K_p and K_i are too large, this can cause PI_{out} to increase to such a degree during a sampling period that f_{CS} is skipped. Unfortunately, for the ASVI control strategy, if f_{CS} is skipped, $G_{ASVI}(s)$ is unable to find it again. In other words, the ASVI control strategy fails with large K_p and K_i.

The detailed failure mechanism is explained in Fig. 6.4(b). As noted, if PI_{out} exceeds f_{CS}, $Z_{ASVI}(s)$ misses its right centre frequency, the cascaded system is still unstable and $|\triangle v_{bus}| > 0$. According to the control Part C of Fig. 6.3(a), the input 3 of S_1 is larger than 0 $\rightarrow$ the output of S_1 is larger than 0 $\rightarrow$ the output of *Relay* is equal to 0 $\rightarrow$ the input 2 of S_1 is equal to 0 $\rightarrow$ the output of S_1 is still equal to the input 3 of S_1 and larger than 0 $\rightarrow$ the output of *Relay* is always larger than 0 $\rightarrow$ the output of S_2 is always equal to the input 3 of S_2. Since the input 3 of S_2 is also connected with PI_{out}, the output of S_2 at this moment can

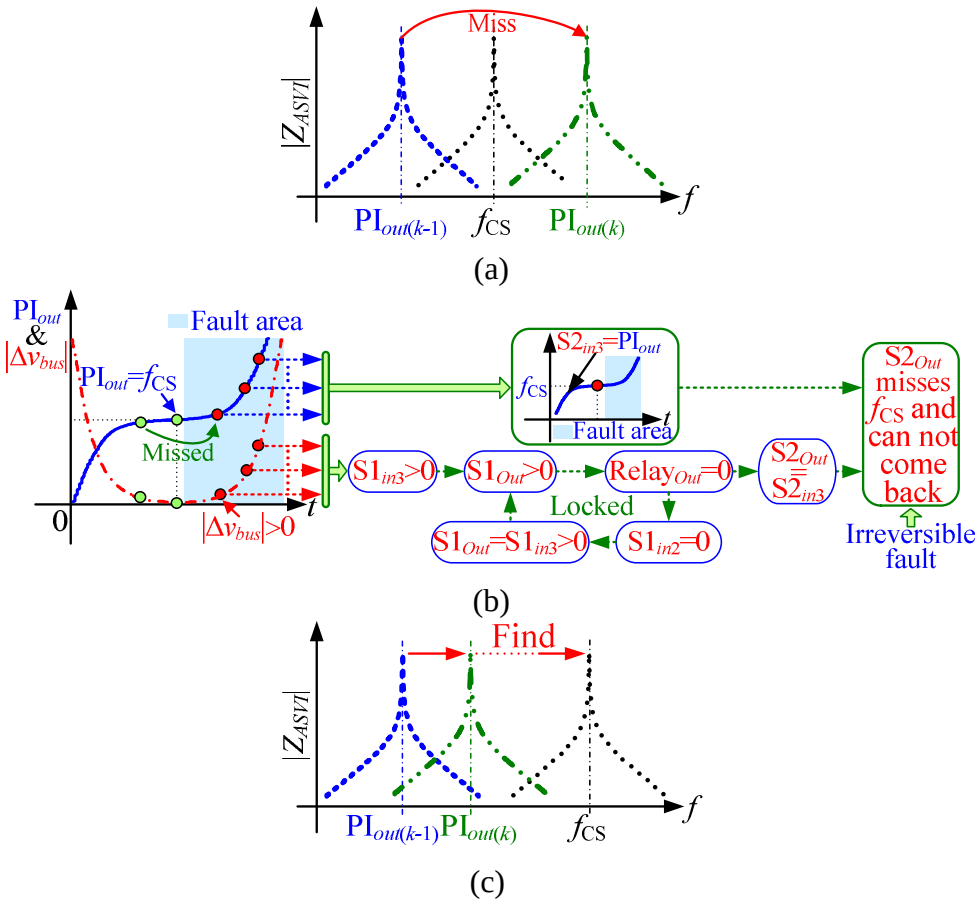


Figure 6.4: The potential problem and its existing prevention method of the ASVI control strategy: (a) miss f_{CS} with excessive PI control parameters; (b) failure mechanism; (c) existing prevention method in Chapter 5 — using small K_p and K_i.

be expressed as

$$S2_{Out} = PI_{out} > f_{CS} \tag{6.8}$$

According to (6.6), as $|\triangle v_{bus}| > 0$, PI_{out} will keep continue to increase due to its integral function. By (6.8), $S2_{Out}$ will also continue to increase. As $S2_{Out}$ also provides the centre frequency for $Z_{ASVI}(s)$, the centre frequency of $Z_{ASVI}(s)$ will be farther away from f_{CS} and never return, as shown in Fig. 6.4(b).

Therefore, the PI controller may miss the right centre frequency of $Z_{ASVI}(s)$ with large K_p and K_i and lead to the failure of the ASVI control strategy. To avoid this problem, small K_p and K_i are recommended in Chapter 5 to prevent the permanent unstable situation. As shown in Fig. 6.4(c), if the K_p and K_i are small enough, the PI controller can always help $Z_{ASVI}(s)$ to find the right centre frequency. This is also the only existing method for

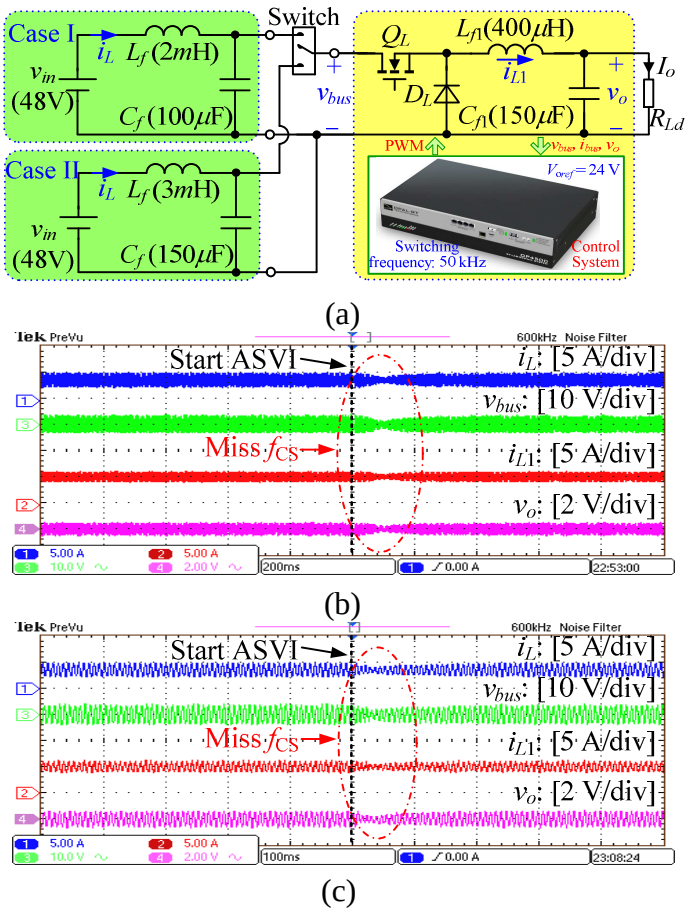


Figure 6.5: Experimental system and its failure Cases of the ASVI control strategy with the same PI controller in Chapter 5: (a) experimental system; (b) Case I; (c) Case II.

prevention the potential problem of the ASVI control strategy.

6.1.3 The Motivation of the MRPT Controller

As noted in Section 6.1.2, although small K_p and K_i may prevent the fault of the ASVI control strategy, this is only a temporary solution. This is because the engineer or user cannot have a clear concept of K_p and K_i for the ASVI controls strategy, i.e., how small is small, or how large is large. Different cascaded systems give different answers.

In order to further elaborate on the limitations of the prevention method proposed in Chapter 5, a 120 W, 48 V - 24 V / 50 kHz Buck converter cascaded with two different *LC* input filters is fabricated. As illustrated in Fig. 6.5(a), if the Buck converter is connected to the filter with $L_f = 2mH$, $C_f = 100\mu F$, the system is referred to Case I. If the Buck converter is connected to the filter with $L_f = 3mH$, $C_f = 150\mu F$, the system is referred

to Case II. Since this cascaded system is unstable at both Cases I and II, the ASVI control strategy is applied into such unstable system and selects $K_p = 10$, $K_i = 20$ for its PI controller, whose parameters are the same as the PI parameters in Chapter 5, and already proved to be small enough in their original experimental systems. However, as shown in Figs. 6.5(b) and (c), the K_p and K_i are still too large for the example system in Fig. 6.5(a). Whether the example system is working in Case I or Case II, the ASVI controller has failed to stabilise the cascaded system. Note the dashed lines in Figs. 6.5(b) and (c): $|\triangle v_{bus}|$ first decreases and then increases, after enabling the ASVI control strategy. It clearly shows that in this example system, $K_p = 10$, $K_i = 20$ are indeed too large for the PI controller, which causes the PI_{out} to close, miss and be farther away from the right centre frequency of $Z_{ASVI}(s)$.

Therefore, in practice, the engineer should spend a lot of time testing the PI parameters many times to find a sufficiently small one for the ASVI control strategy. Clearly, the proposed prevention method in Chapter 5 increases the time cost for the cascaded system, and reduces the competitiveness of the ASVI control strategy. Since the PI controller is the root of the potential problem of the ASVI control strategy and changing the PI parameters is merely a palliative solution, the PI controller could instead by replaced by another reliable controller. It is for this reason that the current chapter proposes the MRPT controller.

6.2 The Improved ASVI Control Strategy with the MRPT Controller

6.2.1 The Relationship Between the Centre Frequency of $Z_{ASVI}(s)$ and $|\triangle v_{bus}|$ — the Inspiration of the MRPT Controller

As noted in Section 6.1.2, the potential problem of the ASVI control strategy is its PI controller. It may miss the right centre frequency of $Z_{ASVI}(s)$ and cause the failure of the ASVI control strategy. Therefore, the relationship between the centre frequency of $Z_{ASVI}(s)$ and $|\triangle v_{bus}|$ is carefully analysed in this section. For convenience, the centre frequency of $Z_{ASVI}(s)$ is hereinafter referred to as f_o.

To reveal the relationship between f_o and $|\triangle v_{bus}|$ clearly, the Bode plots of Z_{iL}, Z_{iLS} and Z_{oS} of a specific cascaded system with different f_o are depicted in Figs. 6.6(a) and (b). Here, this example system is the same as the experimental system in Fig. 6.5(a).

Figs. 6.6(a) and (b) are the Bode plots of this system in Cases I and II, respectively. For both cases, it is only when $f_o = f_{CS}$, that $|Z_{iL}|$ is increased by $Z_{ASVI}(s)$ correctly and a total separation is made between $|Z_{iLS}|$ and $|Z_{oS}|$. Otherwise, whether f_o is increased or decreased, as long as f_o is far away from f_{CS}, $|Z_{iLS}|$ and $|Z_{oS}|$ are intersected and their intersection becomes increasingly serious.

It is understood that the more serious the intersection between $|Z_{iLS}|$ and $|Z_{oS}|$, the larger the oscillation bus voltage of the cascaded system which occurs (Wildrick, 1993). Therefore, Figs. 6.6(a) and (b) suggest that $|\triangle v_{bus}|$ will increase when f_o is far away from f_{CS}. In order to verify this idea, the measured $\frac{|\triangle v_{bus}|}{V_{bus}}$ versus $\frac{f_o}{f_{CS}}$ of the above experimental system are also presented in Fig. 6.6(c). Whether at Case I or Case II, the minimum $|\triangle v_{bus}|$ always appears at $f_o = f_{CS}$ and $|\triangle v_{bus}|$ increases when f_o is far away from f_{CS}.

It is worth pointing out that, Fig. 6.6(c) actually presents a very significance phenomenon, i.e., the $\frac{|\triangle v_{bus}|}{V_{bus}}$ vs $\frac{f_o}{f_{CS}}$ curve behaves like an inverted power-voltage curve of a PV cell (Liu et al., 2008). As the maximum power point of the PV cell can be found by the maximum power point tracking (MPPT) controller, it seems likely that the minimum $|\triangle v_{bus}|$ of the cascaded system could be found by a similar MPPT controller. By Fig. 6.6(c), if the minimum $|\triangle v_{bus}|$ is found, the cascaded system also becomes stable. This is the initial inspiration for the proposed MRPT controller.

6.2.2 Basic Idea of the MRPT Controller

In Fig. 6.6(c), a MRPT controller is proposed to help the ASVI control strategy find f_{CS} instead of the original PI controller. With this MRPT controller, the ASVI control strategy could eliminate the potential problem caused by the original PI controller. The basic principle of the MRPT controller is described in this section.

Fig. 6.7(a) illustrates that the MRPT controller actually learns the perturb and observe (P&O) algorithm (Liu et al., 2008) from the MPPT controller, with f_o is perturbed by a small increment in the MRPT controller, and the resulting change of $|\triangle v_{bus}|$ measured. Where the resulting change of $|\triangle v_{bus}|$ is negative, the perturbation of f_o moves $|\triangle v_{bus}|$ closer to the minimum ripple point (MRP). Thus, further f_o perturbations in the same direction (that is, with the same algebraic sign) should move $|\triangle v_{bus}|$ toward the MRP. If the resulting change of $|\triangle v_{bus}|$ is positive, $|\triangle v_{bus}|$ has been moved away from the MRP, and

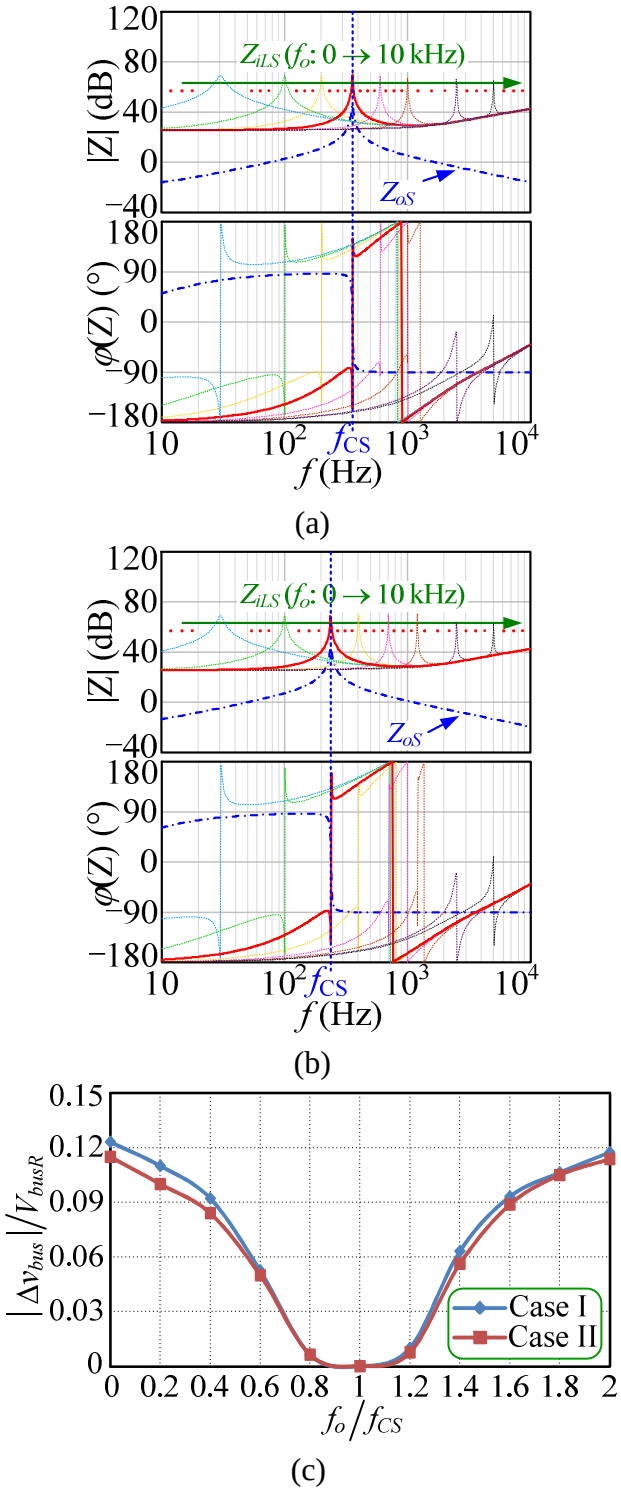


Figure 6.6: Impact of f_o change on the ASVI control strategy: (a) Bode plots of Z_{iL}, Z_{iLS} and Z_{oS} at Case I; (b) Bode plots of Z_{iL}, Z_{iLS} and Z_{oS} at Case II; (c) the relationship between f_o and $|\triangle v_{bus}|$.

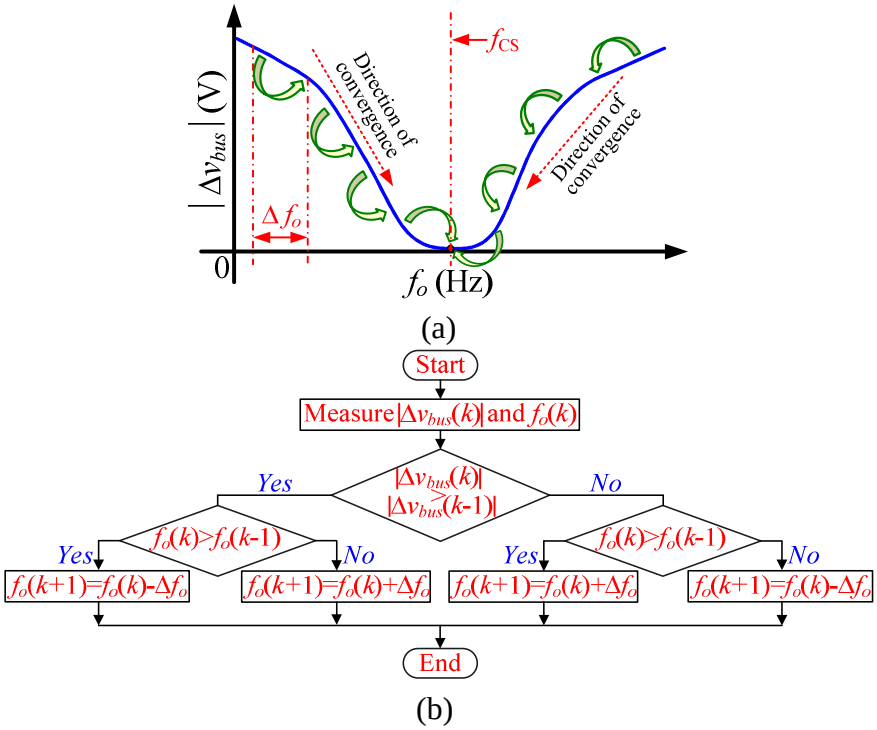


Figure 6.7: Basic idea and algorithm flowchart of the MRPT controller: (a) basic idea; (b) algorithm flowchart.

the algebraic sign of the perturbation should be reversed to move back toward the MRP. Fig. 6.7(b) illustrates this algorithm in a detailed flowchart. Here, $|\triangle v_{bus}(k-1)|$ and $|\triangle v_{bus}(k)|$ are $|\triangle v_{bus}|$ at time $k-1$ and k respectively. $f_o(k-1)$, $f_o(k)$ and $f_o(k+1)$ are f_o at time $k-1$, k and $k+1$, respectively. Between time k and time $k+1$, the MRPT controller works as follows:

$$If\{|\triangle v_{bus}(k)| > |\triangle v_{bus}(k-1)| \;\&\; f_o(k) > f_o(k-1)\} \rightarrow f_o(k+1) = f_o(k) - \triangle f_o \quad (6.9)$$

$$If\{|\triangle v_{bus}(k)| > |\triangle v_{bus}(k-1)| \;\&\; f_o(k) < f_o(k-1)\} \rightarrow f_o(k+1) = f_o(k) + \triangle f_o \quad (6.10)$$

$$If\{|\triangle v_{bus}(k)| < |\triangle v_{bus}(k-1)| \;\&\; f_o(k) > f_o(k-1)\} \rightarrow f_o(k+1) = f_o(k) + \triangle f_o \quad (6.11)$$

$$If\{|\triangle v_{bus}(k)| < |\triangle v_{bus}(k-1)| \;\&\; f_o(k) < f_o(k-1)\} \rightarrow f_o(k+1) = f_o(k) - \triangle f_o \quad (6.12)$$

where $\triangle f_o$ is the perturbation size of f_o. In order to avoid the oscillation caused by the P&O algorithm (Liu et al., 2008), a smaller $\triangle f_o$ is recommended in the MRPT controller.

As indicated by (6.9) $\sim$ (6.12), even when the output of the MRPT controller is increased rapidly and skips f_{CS}, it is still able to return and find it. Therefore, the MRPT

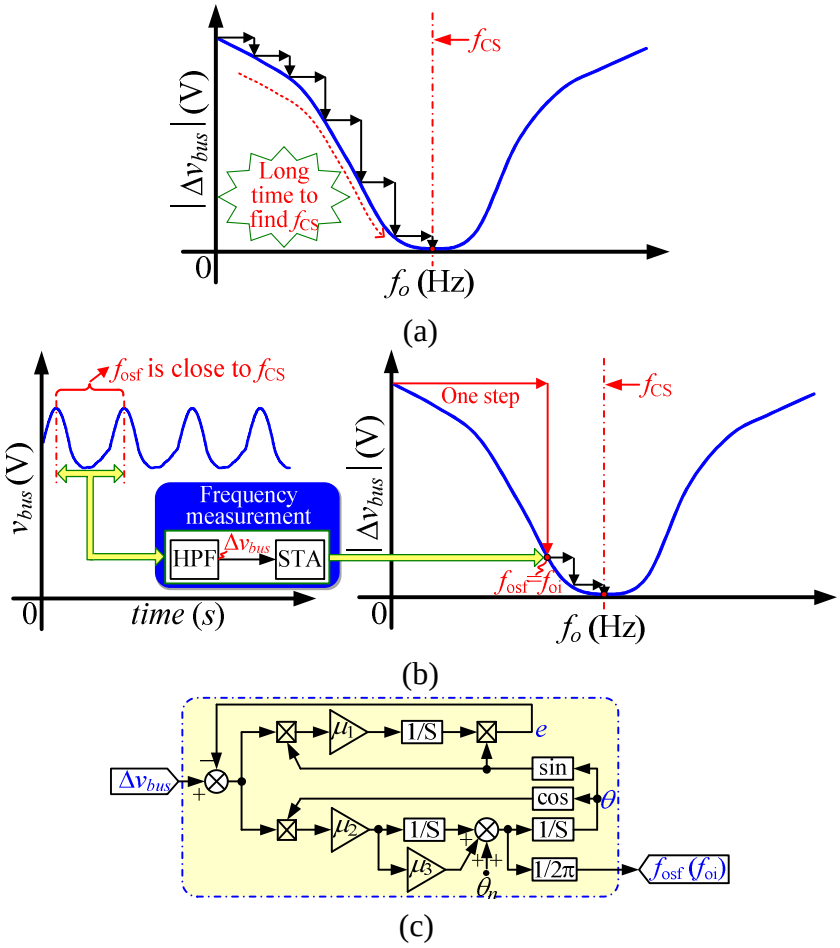


Figure 6.8: Improvement of the MRPT controller: (a) slow processing speed of the MRPT controller; (b) improvement of the MRPT controller; (c) control block of STA.

controller indeed eliminates the potential problem of the original ASVI control strategy.

6.2.3 Improvement of the MRPT Controller with Sinusoidal-Tracking-Algorithm (STA)

As observed in Section 6.2.2, a smaller $\triangle f_o$ is needed in the MRPT controller to avoid the oscillation caused by the P&O algorithm. However, a smaller $\triangle f_o$ also means a slower processing speed of the MRPT controller as shown in Fig. 6.8(a). In order to solve this problem, the MRPT controller is further improved with STA in this section.

It is understood that if the system is unstable due to the intersection between $|Z_{iLS}|$ and $|Z_{oS}|$, the fundamental frequency of $\triangle v_{bus}$ will be very close to f_{CS} (Zhang et al., 2015; Wildrick, 1993). Therefore, if the fundamental frequency of $\triangle v_{bus}$ can be pre-measured

and pre-set as the initial frequency of f_o before enabling the MRPT controller, it can reduce much of the processing time for the MRPT controller to find the f_{CS}. This is the key point to improve the MRPT controller. For convenience, the fundamental frequency of $\triangle v_{bus}$ and the initial frequency of f_o are hereafter referred to as f_{osf} and f_{oi}, respectively.

As shown in Fig. 6.8(b), the above idea can be realised simply by a HPF and a STA: v_{bus} first goes through the HPF to extract $\triangle v_{bus}$, then the STA (Zhong and Hornik, 2013) measures f_{osf} from $\triangle v_{bus}$. f_{osf} is then set as f_{oi}. Therefore, before starting the MRPT controller, its output is already very close to f_{CS}, which can greatly shorten the processing time of the MRPT controller to find the f_{CS}. As a result, the MRPT controller is indeed improved by a fast processing speed.

As discussed before, the STA plays an important role in improving the MRPT controller. Therefore, its detailed operational principle and design criteria are specially explained as follow.

First, the STA is essentially a phase-locked-loop (PLL), whose objective and estimated signals are $\triangle v_{bus}(t)$ and its fundamental component $e(t)$, respectively. $\triangle v_{bus}(t)$ and $e(t)$ are assumed to be

$$\begin{aligned} \triangle v_{bus}(t) &= \sum V_{mi} \sin \theta_{gi} + n(t) && (6.13) \\ e(t) &= E(t) \sin \theta(t) \\ &= E(t) \sin(\int_0^t \omega(\tau) d\tau + \delta(t)) && (6.14) \end{aligned}$$

where V_{mi} and θ_{gi} are the amplitude and phase of the i-th harmonic component of $\triangle v_{bus}(t)$; $n(t)$ represents the noise on $\triangle v_{bus}(t)$; $E(t)$ and $\theta(t) = \int_0^t \omega(\tau) d\tau + \delta(t)$ are the amplitude and phase of $e(t)$.

Then, the state vector of the STA is defined as $\psi(t) = [E(t)\, \omega(t)\, \delta(t)]^T$. So the problem of designing the STA can be formulated as finding the optimal vector $\psi(t)$ that minimises the cost function

$$\begin{aligned} J(\psi(t), t) &= d^2(t) \\ &= [\triangle v_{bus}(t) - e(t)]^2 && (6.15) \end{aligned}$$

where $d(t) = \triangle v_{bus}(t) - e(t)$ is the tracking error of the STA.

In order to solve the optimisation problem, formulate

$$\frac{d\psi(t)}{dt} = -\mu \frac{\partial[J\psi(t),t]}{\partial\psi(t)} \quad \Rightarrow \quad \begin{cases} \frac{dE(t)}{dt} = 2\mu_1 d\sin\theta \\ \frac{d\omega(t)}{dt} = 2\mu_2 E d\cos\theta \\ \frac{d\theta(t)}{dt} = \omega + \mu_3 \frac{d\omega}{dt} \end{cases} \tag{6.16}$$

(6.16) is the basis for implementing the STA as shown in Fig. 6.8(c). As illustrated in (6.16) and Fig. 6.8(c), there are three control parameters in STA: μ_1 is the integral coefficient of the integral controller of the STA amplitude loop. μ_2 and μ_3 form a PI controller $\mu_2(\mu_3 + \frac{1}{s})$ of the STA frequency loop. In general, the larger μ_1, μ_2 and μ_3, the higher the bandwidth of STA and the faster the response. However, too large a μ_2 should be avoided (Zhong and Hornik, 2013) as it may cause instability of STA if a larger phase jump of $\triangle v_{bus}$ occurs. In this chapter, μ_1, μ_2 and μ_3 are selected as 10, 35 and 2 respectively for the experimental system in Fig. 6.5(a).

According to Fig. 6.8(c), when the frequency loop of STA enters its steady state, STA can extract f_{osf} from $\triangle v_{bus}$ and also provide f_{osf} as the initial frequency for f_o. Therefore, with the STA, the improved MRPT controller not only inherits the advantages of the basic MRPT controller to eliminate the potential problem of the original ASVI control strategy, but also ensures the improved ASVI control strategy to quickly stabilise the cascaded system.

6.2.4 Realisation of the MRPT Controller

According to Section 6.1.1, the ASVI control strategy adds only an impedance regulator $G_{ASVI}(s)$ to the original control system of the load converter. Therefore, Fig. 6.9 shows the practical implementation circuit of $G_{ASVI}(s)$ with the MRPT controller. When the single-pole-double-throw switcher S_0 is connected to its input 1, STA is disabled and the circuit is for the $G_{ASVI}(s)$ with the basic MRPT controller. When S_0 is connected to its input 2, STA is enabled and the circuit is for the $G_{ASVI}(s)$ with the improved MRPT controller. As observed earlier, this circuit utilises Parts B and C to realise the function of STA and the basic MRPT controller, respectively. Also, when STA is enabled, Part B extracts the f_{osf} from $\triangle v_{bus}$ and sends it into Part C to provide the initial frequency for f_o. As the detailed operational principle of the basic MRPT controller and STA were explained in Sections

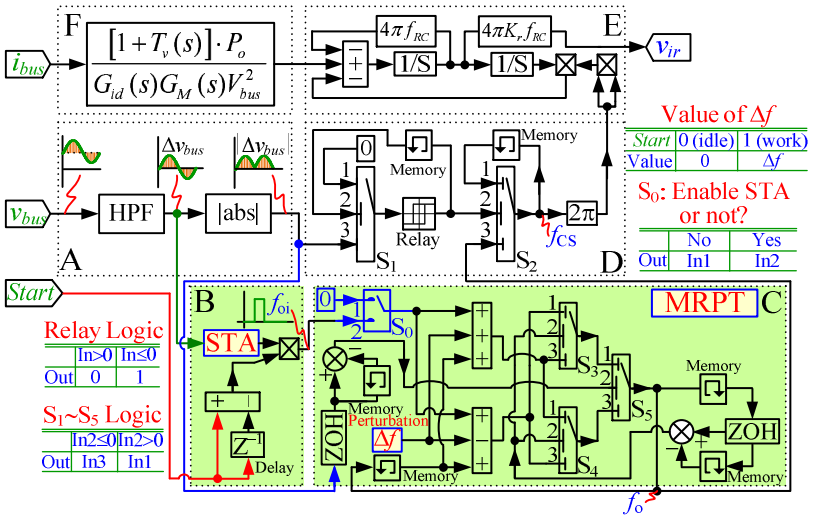


Figure 6.9: Implementation circuit of $G_{ASVI}(s)$ with the MRPT controller.

6.2.2 and 6.2.3 respectively, they will not be repeated here. In Fig. 6.9, the logic of $S_1 \sim S_5$, *Relay* and *Start* are also presented.

6.3 Experimental Verification

In this section, the improved ASVI control strategy with the proposed MRPT controller are applied to the experimental system in Fig. 6.5(a). In this experiment, the sampling time step and $\triangle f_o$ of the MRPT controller are 10 ms and 25 Hz, respectively. The control parameters μ_1, μ_2 and μ_3 of the STA are 10, 35 and 2, respectively.

Firstly, the improved ASVI control strategy with the basic MRPT controller is utilised by the experimental system. The experimental waveforms in Cases I and II are presented at Figs. 6.10(a) and (b) respectively, whilst the definition of i_L, v_{bus}, i_{L1} and v_o are illustrated in Fig. 6.5(a). It is noted that, in both cases, the improved ASVI control strategy with the basic MRPT controller works well and is able to stabilise the cascaded system. In contrast to the experimental results in Figs. 6.5(b) and (c), the basic MRPT controller eliminates the potential problem of the original ASVI control strategy. However, in Figs. 6.10, its stabilisation time is a little longer. As discussed above, this is caused by the slow processing speed of the basic MRPT controller.

The improved ASVI control strategy with the improved MRPT controller utilising STA, is then applied to the experimental system. The experimental waveforms in Cases I and

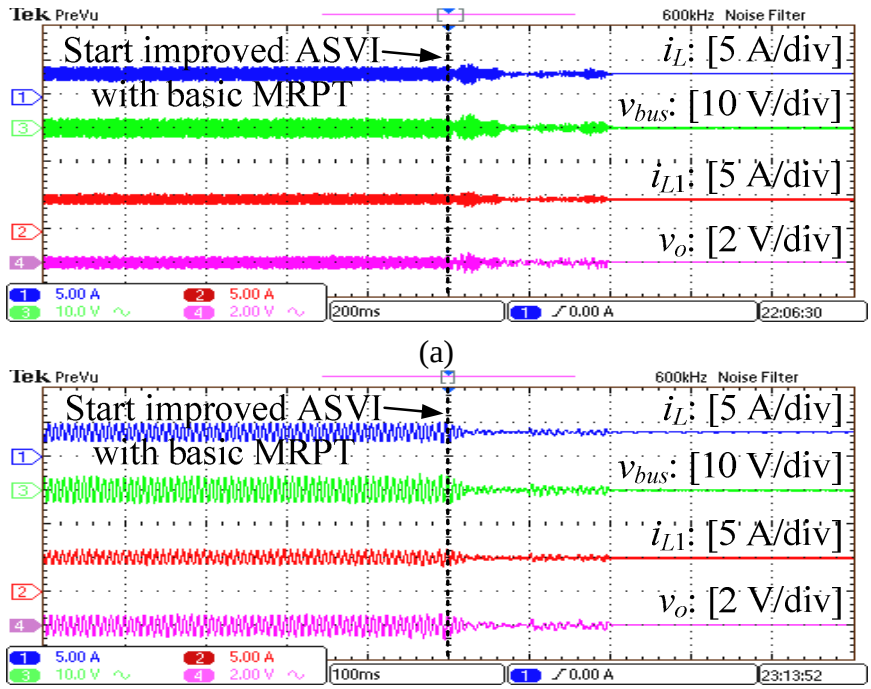


Figure 6.10: Experimental waveforms at Cases I & II with the improved ASVI control strategy incorporating the basic MRPT controller: (a) Case I; (b) Case II.

II are presented at Figs. 6.11 and 6.12, respectively. In Case I, the steady state waveforms, input voltage dynamic waveforms and load dynamic waveforms of experimental systems are presented in Figs. 6.11(a), (b) and (c), respectively. According to Fig. 6.11(a), the improved MRPT controller and the improved ASVI control strategy not only stabilise the cascaded system, but also require much less stabilisation time than that of the basic MRPT controller. Additionally, Figs. 6.11(b) and (c) indicate that the cascaded system can work well with the improved ASVI control strategy incorporating the improved MRPT controller, whether during input voltage changing (v_{bus} : $48V \rightarrow 38.4V$) or load changing (p_o : $10W \rightarrow 120W$) processes. Similarly, in Case II, the steady state waveforms, input voltage dynamic waveforms and load dynamic waveforms of experimental system are presented in Figs. 6.12(a), (b) and (c), respectively. Again, it has been verified that the improved ASVI control strategy with the improved MRPT controller not only stabilises the cascaded system with a fast speed, but also works well during the dynamic processes.

These experimental results thus verified the effectiveness of the ASVI control strategy with the MRPT controller.

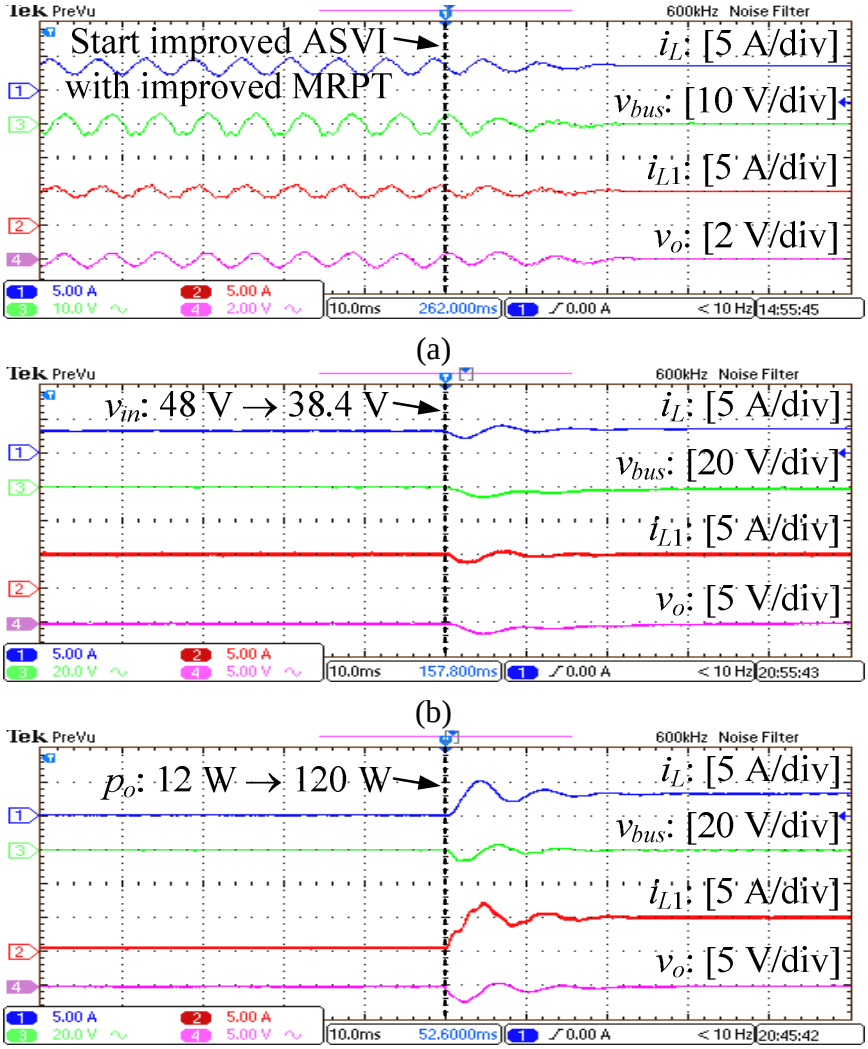


Figure 6.11: Experimental waveforms at Cases I with the improved ASVI control strategy incorporating the improved MRPT controller: (a) steady state waveforms with rated input voltage and load, (b) dynamic waveforms when the input voltage steps down from 100% to 80% rated voltage at full load, (c) dynamic waveforms when the load increases from 10% to 100% rated load at rated input voltage.

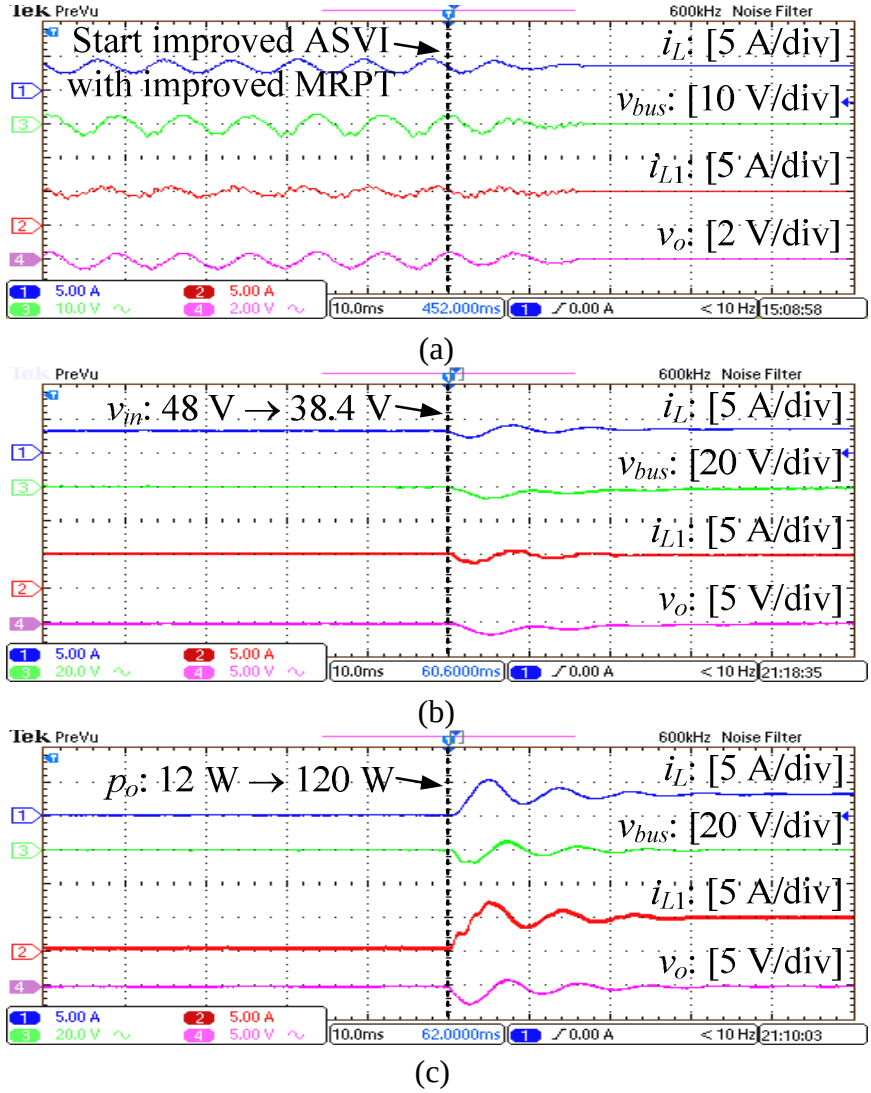


Figure 6.12: Experimental waveforms at Cases II with the improved ASVI control strategy incorporating the improved MRPT controller: (a) steady state waveforms with rated input voltage and load, (b) dynamic waveforms when the input voltage steps down from 100% to 80% rated voltage at full load, (c) dynamic waveforms when the load increases from 10% to 100% rated load at rated input voltage.

6.4 Summary

The traditional ASVI control strategy utilises a PI controller to find the centre frequency of the ASVI. However, this PI controller may miss the right frequency with excessive proportional or integral coefficients and cause the failure of the ASVI control strategy. Though this problem has been discussed in Chapters 4 and 5, it has not yet been solved, thus this chapter looks again at the problem. The relationship between the bus voltage ripple and the centre frequency of the ASVI is firstly analysed. From this, it is clear that their relationship curve behaves like an inverted power-voltage curve of a PV cell. Therefore, a P&O algorithm based MRPT controller is proposed to find the centre frequency of ASVI, in place of the original PI controller. With the MRPT controller, the ASVI control strategy can find the centre frequency of the ASVI without the above problem. Furthermore, in order to shorten the stabilisation time of the improved ASVI control strategy, the STA is also utilised to improve the processing speed of the proposed MRPT controller. In this chapter, both the potential problem of the original ASVI control strategy with the PI controller and the effectiveness of the improved ASVI control strategy with the proposed MRPT controller are experimentally verified on an actual cascaded system.

Chapter 7

Source-side SVI (SSVI) Control to Stabilise Cascaded Systems and Improve the Source Performance

Based on the analysis in Chapters 2 to 6, the ASVI control strategy is so far the best load stabilisation method for the cascaded system. It can not only make the cascaded system an unconditional stable system by shaping the load input impedance, it also changes just the load input impedance in a very small frequency range, minimising its impact on the original load converter. However, though the ASVI control strategy has already greatly reduced its impact on the load converter, its remaining impact is negative. In order to solve this problem, this chapter moves the ASVI from the load side to the source side via a source-side SVI (SSVI) control strategy for the source converter. The proposed SSVI control strategy not only has the same stabilisation function as the ASVI control strategy, it also improves the performance of the source converter. In addition, since the SSVI control strategy is realised by changing the control block of the source converter, the performance of the load converter is not affected. Therefore, the SSVI control strategy can be treated as a supplement and expansion of the ASVI control strategy. Moreover, depending on the method of realisation, the SSVI control strategy can be divided into the source stabilisation methods of the cascaded system. It is also worth pointing out that as the SSVI control strategy stabilises the system by reducing the source output impedance, it is not only suitable for the cascaded system with one upstream converter and one downstream converter, but also for the distributed power system with multiple upstream converters and one downstream

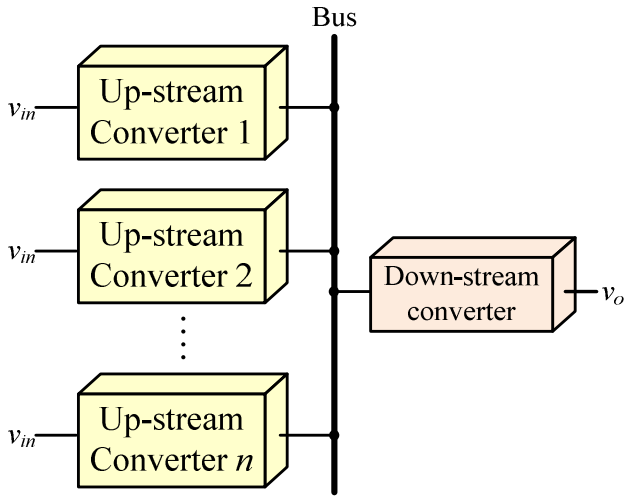


Figure 7.1: Distributed power system with multiple upstream converters and one downstream converter.

converter as shown in Fig. 7.1.

In this chapter, the impact of the ASVI control strategy on the load converter and the impact of the SSVI control strategy on the source converter are analysed via two-port network analysis. The concept and realisation approach of the SSVI control strategy are also discussed in detail. The remaining parts of this chapter are organised as follows: the impact of the ASVI control strategy on the load converter is analysed via two-port network analysis in Section 7.1. The SSVI control strategy is then proposed and its impact on the source converter discussed in Section 7.2. Following this, a 100 W, 48 V - 32 V - 24 V cascaded system is experimentally employed to verify the effectiveness of the SSVI control strategy in Section 7.3. Section 7.4 then concludes this chapter.

7.1 Impact of the ASVI Control Strategy on the Load Converter via Two-Port Network Analysis

In this section, the generic two-port network models of the load converter with and without the ASVI control strategy are first derived. Then, the impact of the ASVI control strategy on the load converter is analysed based on a specific cascaded system.

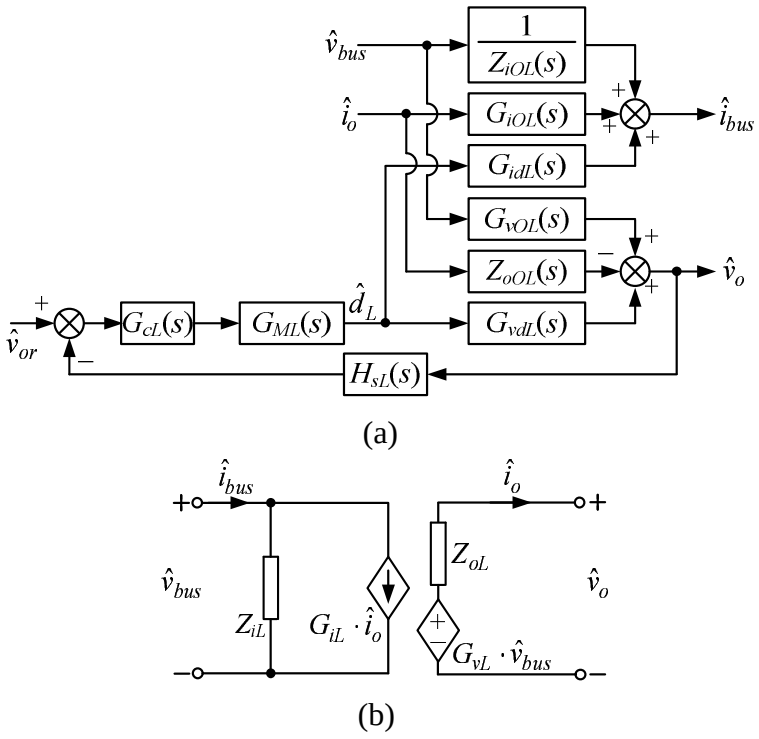


Figure 7.2: Two-port network model of the original load converter: (a) block diagram; (b) two-port network model.

7.1.1 Two-Port Network Model of the Original Load Converter

In Fig. 7.2(a), the small signal block diagram of the original load converter is presented, presenting v_{bus} and i_{bus} as the input voltage and current of the load converter, respectively. v_o and i_o are the output voltage and current of the load converter, respectively. d_L is the duty cycle of the load converter. $Z_{iOL}(s)$, $G_{iOL}(s)$, $G_{idL}(s)$, $G_{vOL}(s)$, $Z_{oOL}(s)$ and $G_{vdL}(s)$ are the six basic open-loop transfer functions of the load converter, whose definitions are referred to Fig. 7.2(a). In addition, for the original load converter, a voltage closed-loop is utilised, where $H_{sL}(s)$ and $G_{cL}(s)$ are the sampling coefficient and voltage regulator transfer function of the output voltage, respectively, and $G_{ML}(s)$ is the transfer function of the modulator.

According to Fig. 7.2(a), the generic two-port network model of the original load converter is derived and presented in Fig. 7.2(b), where $Z_{iL}(s)$ is the closed loop input impedance; $G_{iL}(s)$ is the closed loop load to input current transfer function; $G_{vL}(s)$ is the closed loop input to output voltage transfer function; $Z_{oL}(s)$ is the closed loop output impedance. The performance of the original load converter can be fully described by $Z_{iL}(s) \sim Z_{oL}(s)$

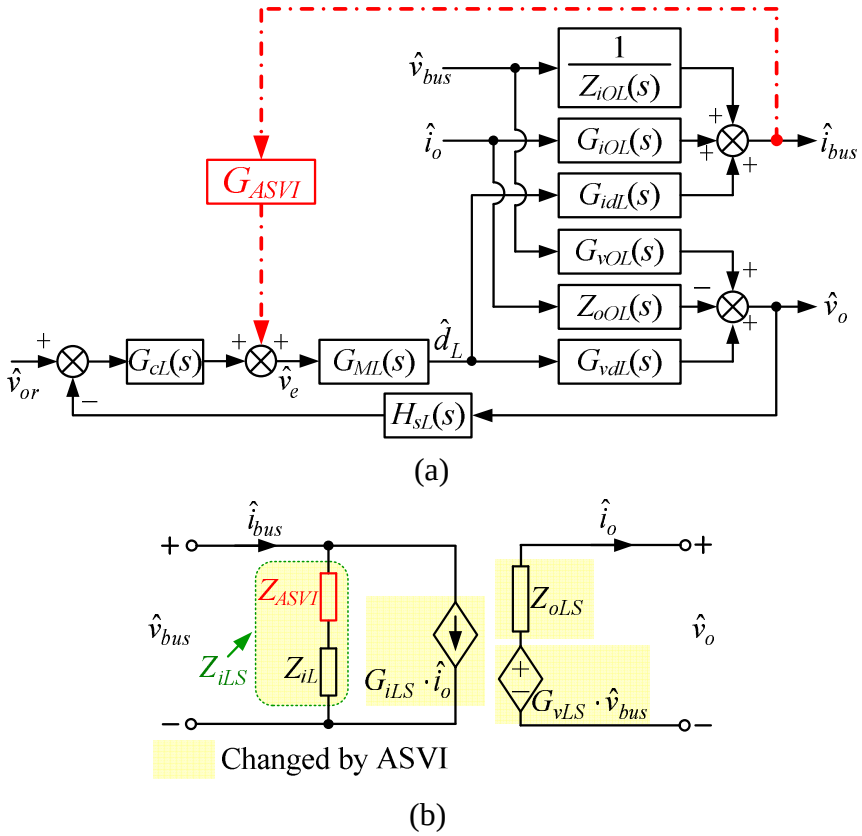


Figure 7.3: Two port network model of the load converter with the ASVI control strategy: (a) block diagram; (b) two-port network model.

(Arnedo, 2008), whose expressions can be derived as

$$Z_{iL}(s)=\left.\frac{\hat{v}_{bus}(s)}{\hat{i}_{bus}(s)}\right|_{\hat{i}_o(s)=0}=\left[\frac{1}{Z_{iOL}(s)}\frac{1}{1+T_{vL}(s)}-\frac{T_{vL}(s)}{1+T_{vL}(s)}\left(\frac{1}{Z_{iOL}(s)}-\frac{G_{idL}(s)G_{vOL}(s)}{G_{vdL}(s)}\right)\right]^{-1} \tag{7.1}$$

$$G_{iL}(s)=\left.\frac{\hat{i}_{bus}(s)}{\hat{i}_o(s)}\right|_{\hat{v}_{bus}(s)=0}=G_{iOL}(s)-\frac{Z_{oOL}(s)G_{idL}(s)}{G_{vdL}(s)}\frac{T_{vL}(s)}{1+T_{vL}(s)} \tag{7.2}$$

$$G_{vL}(s)=\left.\frac{\hat{v}_o(s)}{\hat{v}_{bus}(s)}\right|_{\hat{i}_o(s)=0}=\frac{G_{vL}(s)}{1+T_{vL}(s)} \tag{7.3}$$

$$Z_{oL}(s)=-\left.\frac{\hat{v}_o(s)}{\hat{i}_o(s)}\right|_{\hat{v}_{bus}(s)=0}=\frac{Z_{oOL}(s)}{1+T_{vL}(s)} \tag{7.4}$$

where $T_{vL}(s)=H_{sL}(s)G_{cL}(s)G_{ML}(s)G_{vdL}(s)$ is the loop gain of the voltage closed-loop of the original load converter.

7.1.2 Two-Port Network Model of the Load Converter With the ASVI Control Strategy

According to Chapter 5, in order to stabilise the cascaded system, the ASVI control strategy adds an adaptive virtual impedance $Z_{ASVI}(s)$ in series with $Z_{iL}(s)$ to avoid the intersection between $|Z_{oS}(s)|$ and $|Z_{iL}(s)|$. As shown in Fig. 7.3(a), this $Z_{ASVI}(s)$ is actually realised by introducing an impedance regulator $G_{ASVI}(s)$ to the control block of the load converter. The expression of $G_{ASVI}(s)$ is:

$$G_{ASVI}(s) = Z_{ASVI}(s) \cdot \frac{[1+T_{vL}(s)]P_o}{G_{idL}(s)G_{ML}(s)V_{bus}^2} \tag{7.5}$$

where

$$Z_{ASVI}(s) = \begin{cases} Z_{iLS}(s) - Z_{iL}(s) & f \in [f_1,\, f_2] \\ 0 & f \notin [f_1,\, f_2] \end{cases} \approx \frac{-2K_r(2\pi f_{RC})s}{s^2+2(2\pi f_{RC})s+(2\pi f_{CS})^2} \tag{7.6}$$

here, $Z_{iLS}(s)$ is the improved $Z_{iL}(s)$ by the ASVI control strategy. $|Z_{iLS}(s)| > Z_{oSP}$ during $(f_1,\, f_2)$ and $Z_{iLS}(s) = Z_{iL}(s)$ outside $(f_1,\, f_2)$. $f_{RC} = Max[(f_{CS}-f_1),(f_2-f_{CS})]$ is the bandwidth at $-3dB$ cut-off frequency of the $Z_{ASVI}(s)$. $|Z_{ASVI}(s)|$ during $(f_{CS}-f_{RC},\, f_{CS}+f_{RC})$ is equal to $\frac{K_r}{\sqrt{2}}$ and also is equal to $|Z_{iLS}(j2\pi f_{CS}) - Z_{iL}(j2\pi f_{CS})|$.

According to Fig. 7.3(a), the generic two-port small signal model of the load converter with SVI control strategy is presented in Fig. 7.3(b). $Z_{iLS}(s)$, $G_{iLS}(s)$, $G_{vLS}(s)$ and $Z_{oLS}(s)$ are the improved $Z_{iL}(s)$, $G_{iL}(s)$, $G_{vL}(s)$ and $Z_{oL}(s)$ with the ASVI control strategy, respectively. Their expressions can be derived as

$$Z_{iLS}(s) = \left.\frac{\hat{v}_{bus}(s)}{\hat{i}_{bus}(s)}\right|_{\hat{i}_o(s)=0} = Z_{iL}(s) + Z_{ASVI}(s) \tag{7.7}$$

$$G_{iLS}(s) = \left.\frac{\hat{i}_{bus}(s)}{\hat{i}_o(s)}\right|_{\hat{v}_{bus}(s)=0} = G_{iL}(s) \cdot \left(1 - \frac{T_{iL}(s)}{1+T_{vL}(s)}\right)^{-1} \tag{7.8}$$

$$G_{vLS}(s) = \left.\frac{\hat{v}_o(s)}{\hat{v}_{bus}(s)}\right|_{\hat{i}_o(s)=0} = \left(G_{vOL}(s) + \frac{G_{vdL}(s)}{Z_{iOL}(s)G_{idL}(s)}\frac{T_{iL}(s)}{1-T_{iL}(s)}\right)\left(1+\frac{T_{vL}(s)}{1-T_{iL}(s)}\right)^{-1} \tag{7.9}$$

$$Z_{oLS}(s) = -\left.\frac{\hat{v}_o(s)}{\hat{i}_o(s)}\right|_{\hat{v}_{bus}(s)=0} = \left(Z_{oOL}(s) + \frac{G_{vdL}(s)G_{iOL}(s)}{G_{idL}(s)}\frac{T_{iL}(s)}{1-T_{iL}(s)}\right)\left(1+\frac{T_{vL}(s)}{1-T_{iL}(s)}\right)^{-1} \tag{7.10}$$

where $T_{iL}(s) = G_{ASVI}(s)G_{idL}(s)G_{ML}(s)$.

According to (7.7), the ASVI control strategy adds $Z_{ASVI}(s)$ to the series with $Z_{iL}(s)$ to

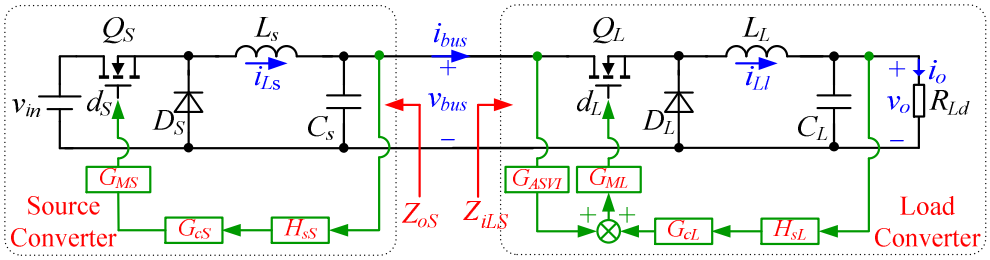


Figure 7.4: Example system with the ASVI control strategy.

Table 7.1: Parameters of the example system with the ASVI control strategy

v_{in}	48V	v_o	24V	f_{sS}	20kHz	L_S	$1mH$	L_L	$450\mu H$	H_{sS}, H_{sL}	0.1	$G_{cS} = 5 + \frac{100}{s}$	$G_{cL} = 3.723e^9 \cdot \left(\frac{s+6.356e^3}{s+6.283e^5}\right)^2$
v_{bus}	32V	P_o	100W	f_{sL}	100kHz	C_S	$150\mu F$	C_L	$220\mu F$	G_{MS}, G_{ML}	1/2.34		

form the final input impedance of the load converter $Z_{iLS}(s)$. By (7.6), $|Z_{iLS}(s)|$ is always larger than $|Z_{oS}(s)|$, thus, the ASVI control strategy can ensure the system stability.

However, according to (7.8) $\sim$ (7.10), though the ASVI control strategy shapes $Z_{iL}(s)$ to ensure the system stability, all the transfer functions of the load converter have already been changed by it. Here, in order to show the changed transfer functions clearly, all of the changed transfer functions are also marked by shadow areas in Fig. 7.3(b).

7.1.3 Impact of the ASVI Control Strategy on the Load Converter

According to Sections 7.1.1 and 7.1.2, though the ASVI control strategy can stabilise the cascaded system by shaping $Z_{iL}(s)$, it in fact changes all the transfer functions of the original load converter. In order to evaluate the impact of ASVI control strategy on the load converter clearly, a detailed cascaded system is taken as an example to aid the analysis in this section. The main circuit and control block of this example system are depicted in Fig. 7.4, and the parameters of the example system are presented in Table 7.1.

According to (7.1) and (7.7), Bode plots of $Z_{iL}(s)$ and $Z_{iLS}(s)$ of the example system are depicted in Fig. 7.5(a). These suggest that the ASVI control strategy can increase $|Z_{iL}(s)|$ during (f_1, f_2) to ensure a total separation between $|Z_{iLS}(s)|$ and $|Z_{oS}(s)|$. Therefore, the stability of the cascaded system is guaranteed. However, it is worthy pointing out that, since the negative resistor characteristic of $Z_{iL}(s)$ is also changed by the ASVI control strategy during (f_1, f_2) (See Fig. 7.5(a)), the ASVI control strategy actually has negative impact on $Z_{iL}(s)$ from the load performance point of view.

According to (7.2) and (7.8), Bode plots of $G_{iL}(s)$ and $G_{iLS}(s)$ in the example system can be depicted and presented in Fig. 7.5(b). As seen, $G_{iLS}(s)$ is different with $G_{iL}(s)$ during $(f_1,\ f_2)$, however, the difference is very small and can be ignored.

According to (7.3) and (7.9), Bode plots of $G_{vL}(s)$ and $G_{vLS}(s)$ in the example system can be plotted and presented in Fig. 7.5(c). These show that $|G_{vLS}(s)|$ is larger than $|G_{vL}(s)|$ at a lower frequency. Since $G_{vL}(s)$ reflects the suppression ability of v_o to the disturbance of v_{bus} and the smaller $|G_{vL}(s)|$ the better, the ASVI control strategy has a negative impact on $G_{vL}(s)$.

According to (7.4) and (7.10), Bode plots of $Z_{oL}(s)$ and $Z_{oLS}(s)$ in the example system can be plotted and presented in Fig. 7.5(d). Similar to $G_{vLS}(s)$, $|Z_{oLS}(s)|$ is larger than $|Z_{oL}(s)|$ at a lower frequency. As a larger $|Z_{oL}(s)|$ also means a worse dynamic performance of v_o to i_o, the ASVI control strategy has a negative impact on $Z_{oL}(s)$.

In summary, though the ASVI control strategy can stabilise the cascaded system by shaping $Z_{iL}(s)$, this affects all the transfer functions and deteriorates the performance of $Z_{iL}(s)$, $G_{vL}(s)$ and $Z_{oL}(s)$. This is the limitation of the ASVI control strategy.

7.2 The SSVI Control Strategy

7.2.1 The Concept of the SSVI Control Strategy

As shown in Fig. 7.6, the ASVI control strategy adds $Z_{ASVI}(s)$ to the series with $Z_{iL}(s)$, to form the final load input impedance $Z_{iLS}(s)$ and ensure $|Z_{iLS}(s)|$ is always larger than $|Z_{oS}(s)|$ to stabilise the cascaded system. However, as discussed above, the ASVI control strategy deteriorates the performance of the load converter. In order to solve this problem, the $Z_{ASVI}(s)$ is moved from load side to source side, thus changing the control block of the source converter instead of the load converter in this section. To distinguish it from the ASVI control strategy, this proposed solution is called the 'SSVI control strategy'.

As depicted in Fig. 7.6, since $Z_{ASVI}(s)$ is in a series with $Z_{iL}(s)$ and $Z_{oS}(s)$ simultaneously, the SSVI control strategy has the same stabilisation function as the ASVI control strategy. The only difference between the SSVI and ASVI control strategies is in their physical concepts, i.e., the ASVI control strategy keeps a total separation between $|Z_{oS}(s)|$ and $|Z_{iL}(s)|$ by increasing $|Z_{iL}(s)|$, but the SSVI control strategy realises this by decreasing

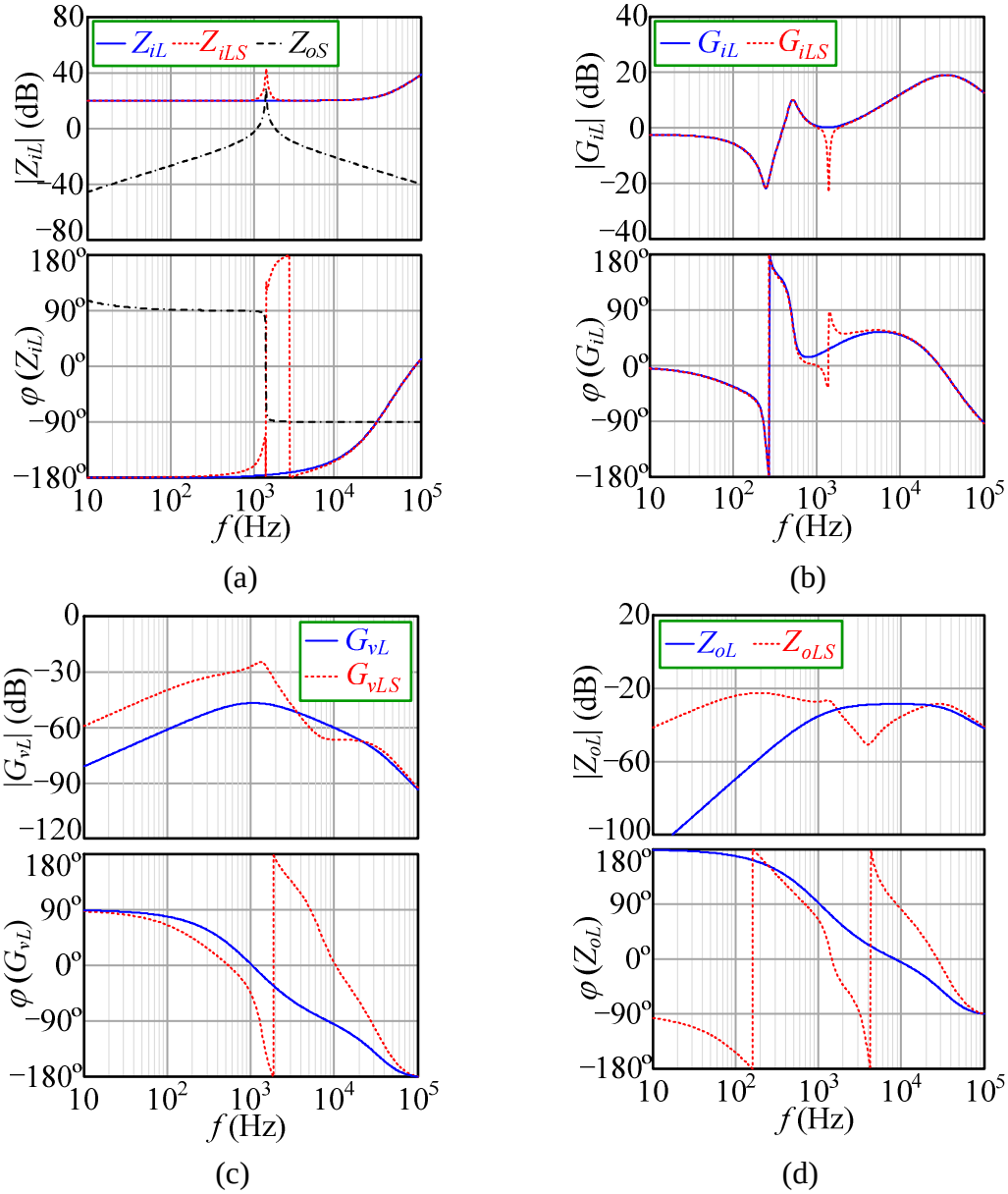


Figure 7.5: Bode plots of the load converter with or without the ASVI control strategy: (a) $Z_{iL}(s)$ and $Z_{iLS}(s)$; (b) $G_{iL}(s)$ and $G_{iLS}(s)$; (c) $G_{vL}(s)$ and $G_{vLS}(s)$; (d) $Z_{oL}(s)$ and $Z_{oLS}(s)$.

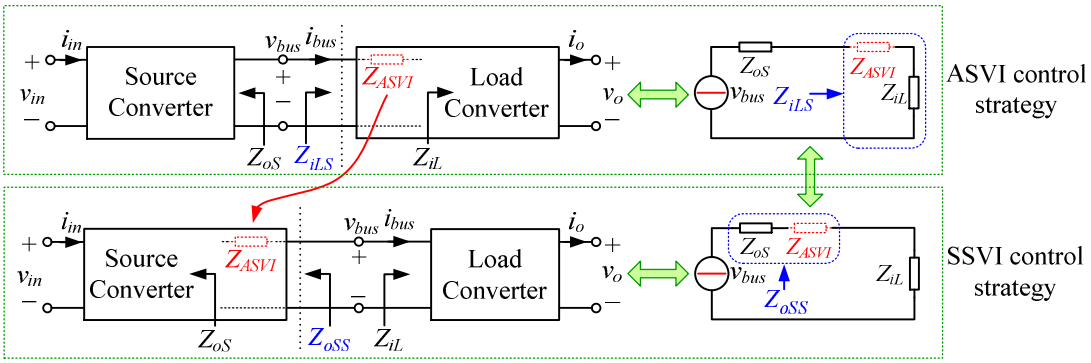


Figure 7.6: Concept of the SSVI control strategy.

$|Z_{oS}(s)|$. However, in later sections, it will be shown that, this small difference helps the SSVI control strategy to overcome the drawback of the ASVI control strategy, i.e., not deteriorating but in fact improving the performance of the source converter without bringing any impact to the load converter when stabilising the cascaded system.

7.2.2 Realisation of the SSVI Control Strategy

The small signal control block of the original source converter is presented in Fig. 7.7(a). v_{in} and i_{in} are the input voltage and current of the source converter, respectively. d_S is the duty cycle of the source converter. $Z_{iOS}(s) \sim G_{MS}(s)$ have the same definitions as $Z_{iOL}(s) \sim G_{ML}(s)$ in Fig. 7.2(a), where the only difference is the subscript S denotes 'source converter'. As with the dotted line in Fig. 7.7(a), the intuitive way to add $Z_{ASVI}(s)$ to a series with $Z_{oS}(s)$ is by introducing $Z_{ASVI}(s)$ between $\hat{i}_{bus}$ and $-\hat{v}_{bus}$ directly. However, this method cannot be achieved by control directly. In order to address this issue, the output of $Z_{ASVI}(s)$ moves to the output of the voltage regulator $G_{cS}(s)$ and equivalently adjusts the transfer function to $G_{SSVI}(s)$, as shown by the dot-dashed lines.

According to Fig. 7.7(a), if $G_{SSVI}(s)$ is required to realise $Z_{ASVI}(s)$, the following relationship is in force:

$$-\hat{i}_{bus} \cdot Z_{ASVI}(s) = \hat{i}_{bus} \cdot G_{SSVI}(s) \cdot G_{MS}(s) \cdot G_{vdS}(s) \cdot \frac{1}{1+T_{vS}(s)} \tag{7.11}$$

where $T_{vS}(s) = H_{sS}(s)G_{cS}(s)G_{MS}(s)G_{vdS}(s)$ is the loop gain of the voltage closed-loop of the original source converter.

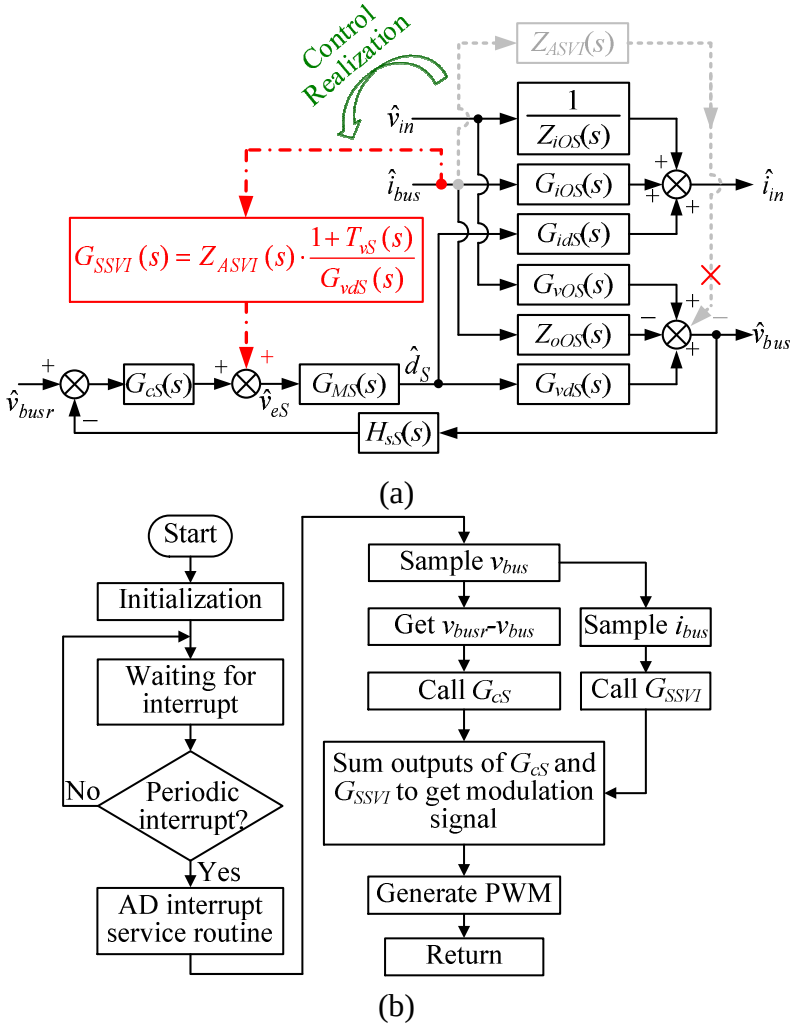


Figure 7.7: The SSVI control strategy: (a) control block; (b) algorithm.

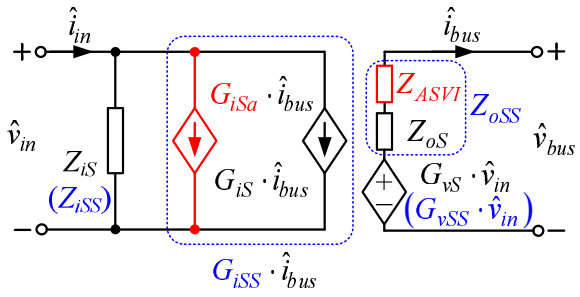


Figure 7.8: Two-port network model of the source converter with the SSVI control strategy.

According to (7.11), the expression of $G_{SSVI}(s)$ can be derived as

$$G_{SSVI}(s) = -Z_{ASVI}(s) \cdot \frac{1+T_{vS}(s)}{G_{vdS}(s)G_{MS}(s)} \tag{7.12}$$

Up to this point, Fig. 7.7(a) presents the fully controlled block of the proposed SSVI control strategy.

The proposed SSVI control strategy can be implemented by a digital signal processor, such as DSP TMS320F28335. The mechanism for this is presented in Fig. 7.7(b), with both v_{bus} and i_{bus} sampled to provide the necessary information for the SSVI control strategy and the output voltage regulation. The algorithm obtains the modulation signal by adding the output of $G_{SSVI}(s)$ to the output of $G_{cS}(s)$, and then generates d_S by pulse-width modulation (PWM).

7.2.3 Impact of the SSVI Control Strategy on the Source Converter

According to Fig. 7.7(a), the generic two-port small signal model of the source converter with the SSVI control strategy can be derived and presented in Fig. 7.8. $Z_{iS}(s)$, $G_{iS}(s)$, $G_{vS}(s)$ and $Z_{oS}(s)$ are the four basic input-to-output closed-loop transfer functions of the original source converters. $Z_{iSS}(s)$, $G_{iSS}(s)$, $G_{vSS}(s)$ and $Z_{oSS}(s)$ are the improved $Z_{iS}(s)$, $G_{iS}(s)$, $G_{vS}(s)$ and $Z_{oS}(s)$ by the SSVI control strategy, respectively. Their expressions can be derived as

$$\begin{aligned}
Z_{iSS}(s) = \left.\frac{\hat{v}_{in}(s)}{\hat{i}_{in}(s)}\right|_{\hat{i}_{bus}(s)=0} &= \left[\frac{1}{Z_{iOS}(s)}\frac{1}{1+T_{vS}(s)} - \frac{T_{vS}(s)}{1+T_{vS}(s)}\left(\frac{1}{Z_{iOS}(s)} - \frac{G_{idS}(s)G_{vOS}(s)}{G_{vdS}(s)}\right)\right]^{-1} \\
&= Z_{iS}(s) \qquad (7.13) \\
G_{iSS}(s) = \left.\frac{\hat{i}_{in}(s)}{\hat{i}_{bus}(s)}\right|_{\hat{v}_{in}(s)=0} &= \left[G_{iOS}(s) - \frac{Z_{oOS}(s)G_{idS}(s)}{G_{vdS}(s)}\frac{T_{vS}(s)}{1+T_{vS}(s)}\right] + \left[\frac{T_{iS}(s)}{1+T_{vS}(s)}\right] \\
&= G_{iS}(s) + G_{iSa}(s) \qquad (7.14) \\
G_{vSS}(s) = \left.\frac{\hat{v}_{bus}(s)}{\hat{v}_{in}(s)}\right|_{\hat{i}_{bus}(s)=0} &= \frac{G_{vOS}(s)}{1+T_{vS}(s)} = G_{vS}(s) \qquad (7.15) \\
Z_{oSS}(s) = -\left.\frac{\hat{v}_{bus}(s)}{\hat{i}_{bus}(s)}\right|_{\hat{v}_{in}(s)=0} &= \frac{Z_{oOS}(s)}{1+T_{vS}(s)} + Z_{ASVI}(s) = Z_{oS}(s) + Z_{ASVI}(s) \qquad (7.16)
\end{aligned}$$

where $T_{iS}(s) = G_{SSVI}(s)G_{idS}(s)G_{MS}(s)$.

According to (7.16), the SSVI control strategy adds $Z_{ASVI}(s)$ into the series with $Z_{oS}(s)$

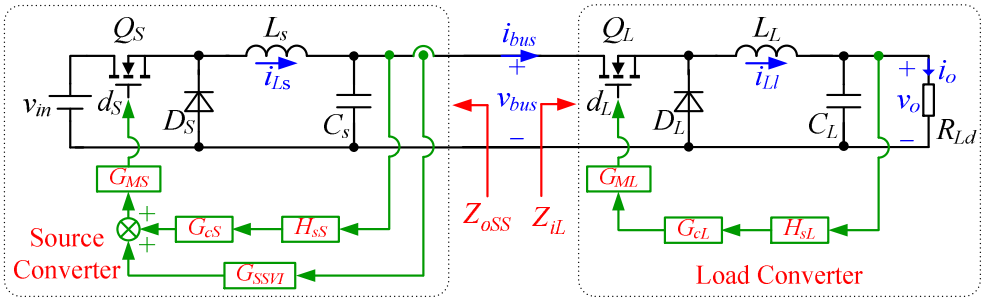


Figure 7.9: Example system with SSVI control strategy.

to form the final output impedance of the source converter $Z_{oSS}(s)$. By Fig. 7.6, the SSVI control strategy realises the same stabilisation function with the ASVI control strategy, so the SSVI control strategy can guarantee the stability of the cascaded system. According to (7.13) and (7.15), the SSVI control strategy keeps the original performance of $Z_{iS}(s)$ and $G_{vS}(s)$. According to (7.14), the SSVI control strategy changes the original performance of $G_{iS}(s)$. In Fig. 7.8, the above changed transfer functions are marked by dash borders.

As with the ASVI control strategy, in order to evaluate the impact of the SSVI control strategy on the source converter, the same example system shown in Fig. 7.4 is utilised to aid the analysis in this section. The only difference is that this example system utilises the SSVI control strategy instead of the ASVI control strategy. The main circuit and control block of the example system with the SSVI control strategy are depicted in Fig. 7.9. The parameters of the example system can be found in Table 7.1.

According to (7.13) and (7.15), Bode plots of $Z_{iS}(s)$ & $Z_{iSS}(s)$ and $G_{vS}(s)$ & $G_{vSS}(s)$ of the example system are depicted in Figs. 7.10(a) and (c), respectively. It can be observed that the SSVI control strategy does not make any changes of $Z_{iS}(s)$ and $G_{vS}(s)$.

According to (7.14), Bode plots of $G_{iS}(s)$ & $G_{iSS}(s)$ of the example system can be plotted and presented in Fig. 7.10(b). The SSVI control strategy increases the amplitude of $G_{iS}(s)$ at a higher frequency. As $G_{iS}(s)$ reflects the suppression ability of i_{in} to the disturbance of i_{bus} and the smaller $|G_{iS}(s)|$ the better, the SSVI control strategy has a negative impact on $G_{iS}(s)$. However, it is worth mentioning that since the SSVI control strategy only increases $|G_{iS}(s)|$ on the high frequency range, the impact is minimal in practice.

According to (7.16), Bode plots of $Z_{oS}(s)$ & $Z_{oSS}(s)$ of the example system are depicted in Fig. 7.10(d). The SSVI control strategy decreases $|Z_{oS}(s)|$ in the whole frequency range

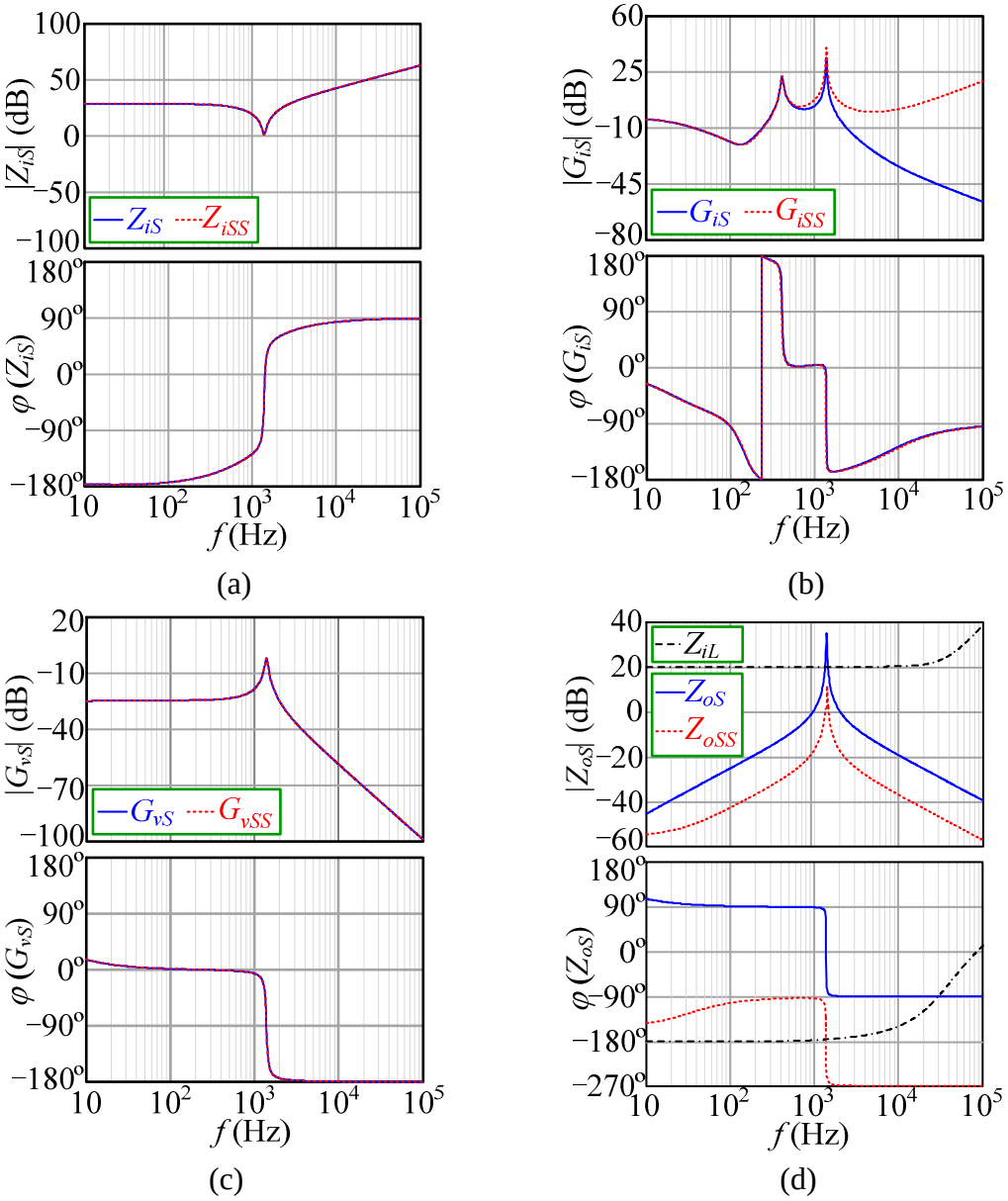


Figure 7.10: Bode plots of the source converter without or with the SSVI control strategy: (a) $Z_{iS}(s)$ and $Z_{iSS}(s)$; (b) $G_{iS}(s)$ and $G_{iSS}(s)$; (c) $G_{vS}(s)$ and $G_{vSS}(s)$; (d) $Z_{oS}(s)$ and $Z_{oSS}(s)$.

Table 7.2: Comparison for ASVI and SSVI control strategies

	Affected converter	$Z_{i(L/S)}(s)$	$G_{i(L/S)}(s)$	$G_{v(L/S)}(s)$	$Z_{o(L/S)}(s)$	Cascaded system	Evaluation
ASVI	Load converter	Negative	Little change	Negative	Negative	Stable	SSVI is better
SSVI	Source converter	No change	Little change	No change	Postitive	Stable	than ASVI

to avoid the intersection with $|Z_{iL}(s)|$. Therefore, the stability of the cascaded system is guaranteed. In addition, since $Z_{oS}(s)$ is the closed-loop output impedance of the source converter, the smaller $|Z_{oS}(s)|$ the better. Hence, the SSVI control strategy also has positive impact on $Z_{oS}(s)$ from the source performance point of view.

In summary, the SSVI control strategy can stabilise the cascaded system by reducing $|Z_{oS}(s)|$. It has no impact on $Z_{iS}(s)$ and $G_{vS}(s)$, a negligible negative impact on $G_{iS}(s)$ and a positive impact on $Z_{oS}(s)$.

According to Figs. 7.5 and 7.10, both the impact of the ASVI control strategy on the load converter and the impact of the SSVI control strategy on the source converter are concluded and compared in Table 7.2. The SSVI control strategy not only has the same stabilisation function as the ASVI control strategy, but also has a more positive impact on the original cascaded system than the ASVI control strategy. From this point of view, the SSVI control strategy is superior to the ASVI control strategy.

7.3 Experimental Results

In this chapter, the example cascaded system presented in Fig. 7.9, is fabricated to validate the SSVI control strategy. Its circuit, control block, parameters and Bode plots can be found in Section 7.2.3, and will not be repeated here. As shown in Fig. 7.11, to make the verification more available, the source converter is controlled by DSP TMS320F28335, and the load converter is a special custom power module from TRACO POWER company.

The experimental results of the cascaded system with the SSVI control strategy are given in Fig. 7.12. As shown in Fig. 7.12(a), this cascaded system is unstable without the SSVI control strategy. After enabling the SSVI control strategy, the cascaded system becomes stable. This phenomenon is also consistent with Bode plots in Fig. 7.10(d). The input voltage dynamic waveforms of the cascaded system with the SSVI control strategy at full load are presented in Figs. 7.12(b) and (c). In Fig. 7.12(b), the input voltage of the

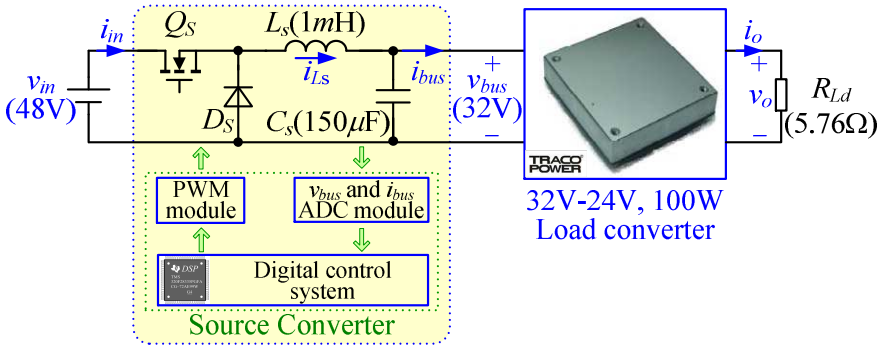


Figure 7.11: Experimental system.

cascaded system changes from 80% rated voltage (38.4 V) to 100% rated voltage (48 V). In Fig. 7.12(c), the input voltage of the cascaded system changes from 48 V to 38.4 V. This indicates that the SSVI control strategy can work well during any input voltage changes. The load dynamic waveforms of the cascaded system with the SSVI control strategy at rated input voltage are presented in Figs. 7.12(d) and (e). In Fig. 7.12(d), the load of the cascaded system changes from 10% full load (10 W) to 100% full load (100 W). In Fig. 7.12(e), the load of the cascaded system is changing from 100 W to 10 W. This also indicates that the SSVI control strategy can work well during any load changes

The dynamic experimental waveforms of the source converter with or without the SSVI control strategy are shown in Figs. 7.13 and 7.14, respectively. It is shown that, with the SSVI control strategy, the input voltage dynamic performance of the source converter is the same as the original performance. Moreover, with the SSVI control strategy, the load dynamic performance of the source converter is better than the original performance of the source converter. This is because the SSVI control strategy reduces $|Z_{oS}(s)|$, does not have an impact on $Z_{iS}(s)$ and $G_{vS}(s)$, and has a negligible negative impact on $G_{iS}(s)$.

According to Fig. 7.12 $\sim$ Fig. 7.14, the SSVI control strategy not only stabilises the cascaded system, but also improves the performance of the source converter.

7.4 Summary

The ASVI control strategy is further investigated in this chapter. It is understood that though the ASVI control strategy can stabilise the cascaded system and limit its impact on the load converter in a very small frequency range, it brings a negative impact to the load

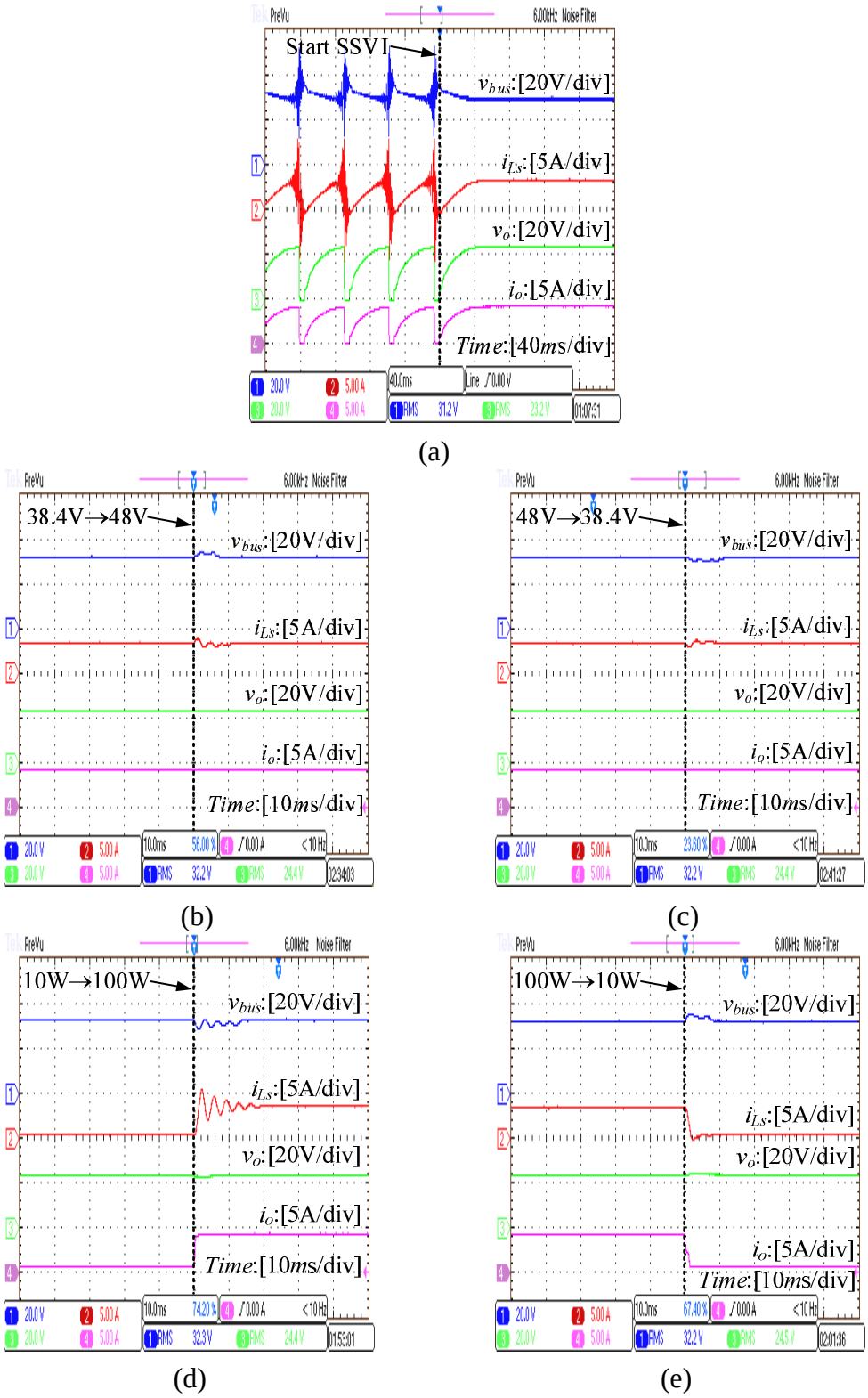


Figure 7.12: Experimental waveforms of the cascaded system with the SSVI control strategy: (a) steady state waveforms when $V_{in} = 48V$, $P_o = 100W$, (b) dynamic waveforms when V_{in} steps up from 38.4 V to 48 V, (c) dynamic waveforms when V_{in} steps down from 48 V to 38.4 V, (e) dynamic waveforms when P_o increases from 10 W to 100 W, (f) dynamic waveforms when P_o decreases from 100 W to 10 W.

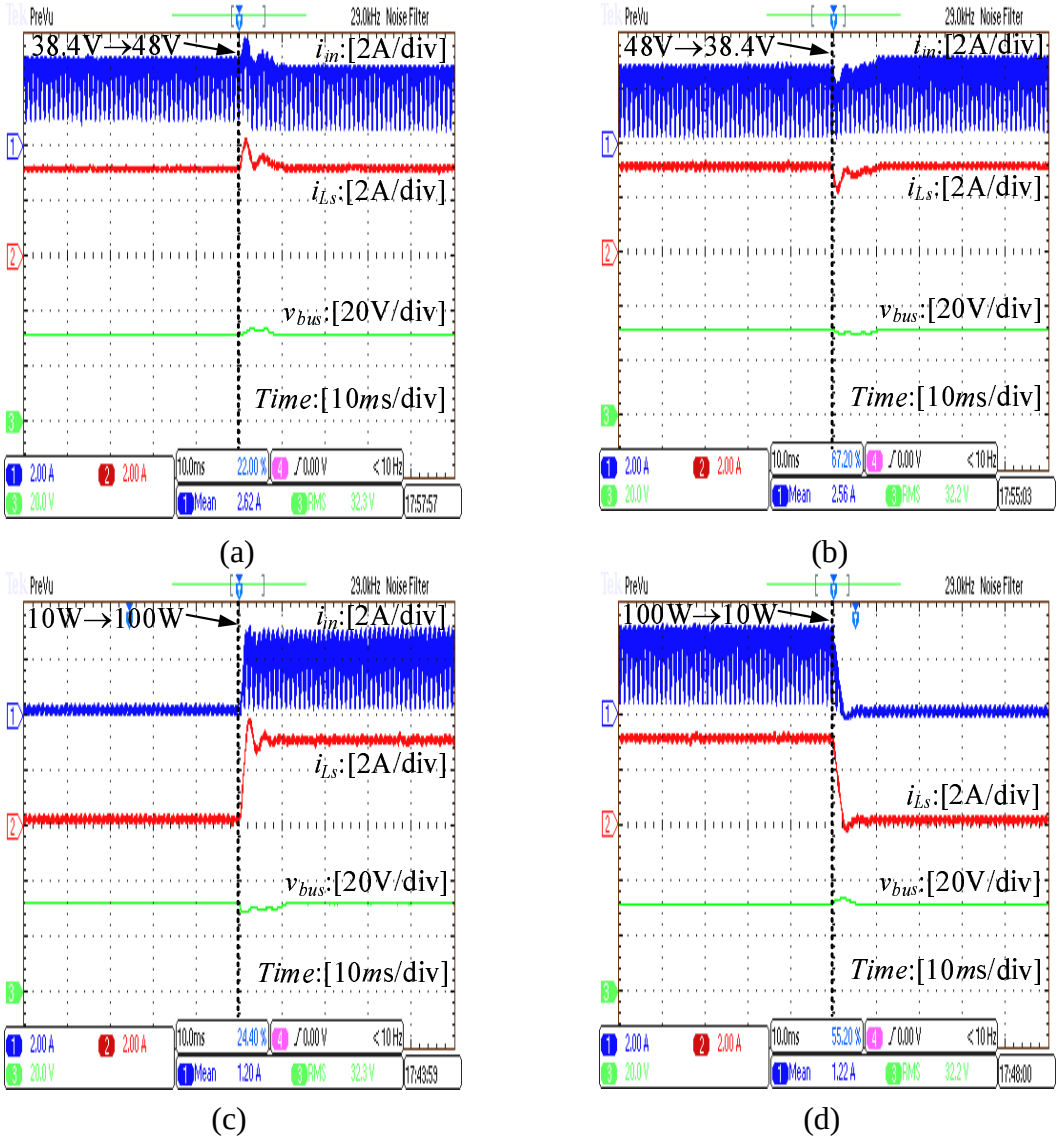


Figure 7.13: Dynamic waveforms of the original source converter without the SSVI control strategy: (a) V_{in} steps up from 38.4 V to 48 V, (b) V_{in} steps down from 48 V to 38.4 V, (c) P_o increases from 10 W to 100 W, (d) P_o decreases from 100 W to 10 W.

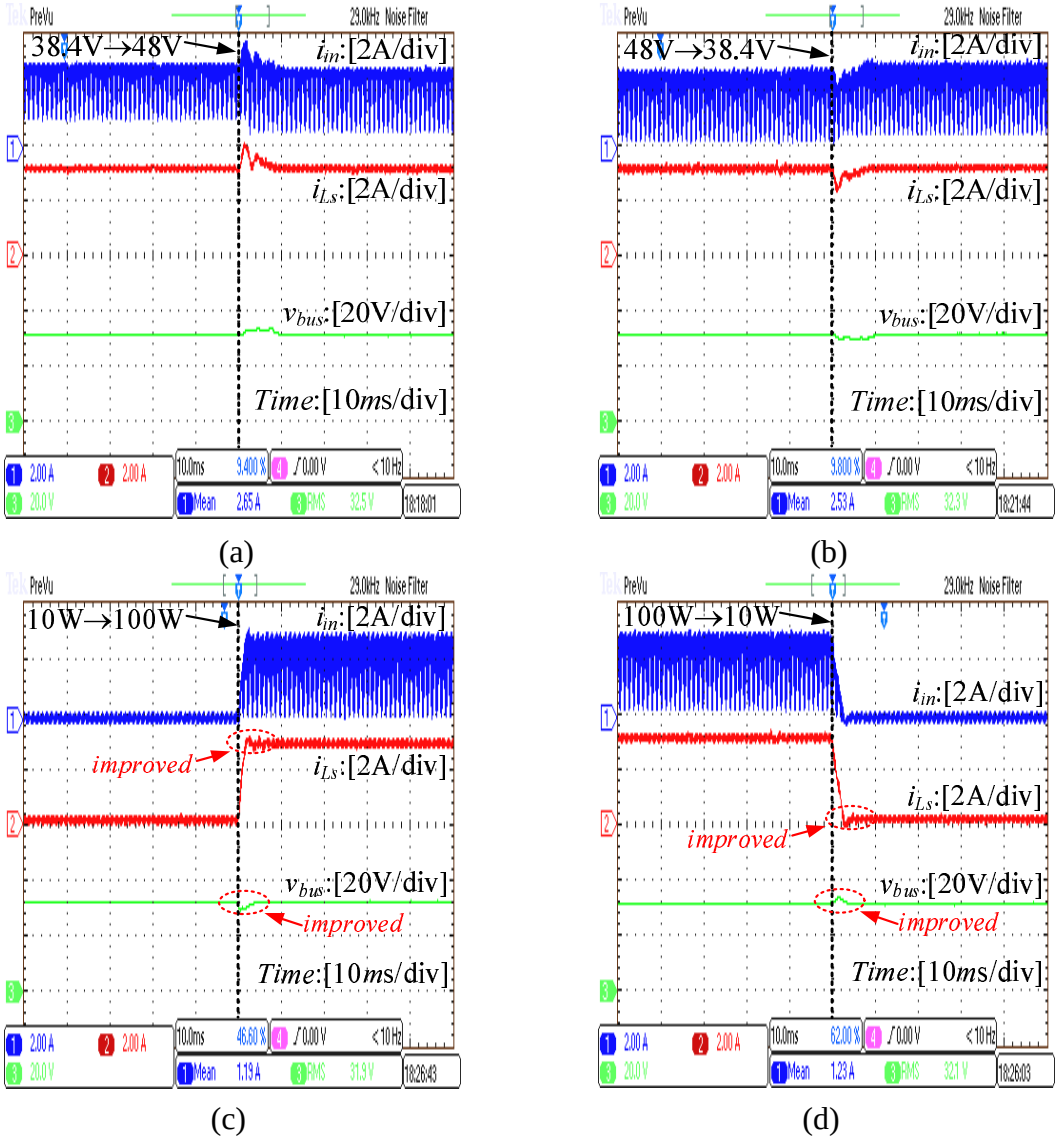


Figure 7.14: Dynamic waveforms of the source converter with the SSVI control strategy: (a) V_{in} steps up from 38.4 V to 48 V, (b) V_{in} steps down from 48 V to 38.4 V, (c) P_o increases from 10 W to 100 W, (d) P_o decreases from 100 W to 10 W.

converter. In order to solve this problem, the SSVI control strategy is proposed. The SSVI control strategy moves the ASVI from load side to source side by changing the control block of the source converter instead of the load converter. As a result, the SSVI control strategy not only has the same stabilisation function as the ASVI control strategy, but also improves the performance of the source converter. In addition, since the SSVI control strategy is realised by changing the control block of the source converter, the performance of the load converter is not affected. Therefore, the SSVI control strategy is an improvement on the ASVI control strategy. It is also worth pointing out that as the SSVI control strategy stabilises the system by reducing the source output impedance, it is not only suitable for the cascaded system with one upstream converter and one downstream converter, but also for the distributed power system with multiple upstream converters and one downstream converter. Finally, the proposed SSVI strategy has been experimentally verified on a 100 W, 48 V - 32 V - 24 V cascaded system.

Chapter 8

Virtual *RLC* Damper for the *LC* Input Filter to Stabilise Cascaded Systems and Improve the Filter Performance

As discussed in Chapters 2 to 7, the *LC* filter at the input of a DC/DC converter may cause instability when the converter is controlled as a constant power load (CPL). As the reduced system damping caused by the CPL is the root of the instability problem in cascaded systems (Middlebrook, 1979), the most intuitive solution is to increase the system damping by using dampers (Erickson and Maksimov, 2001; Cespedes et al., 2011; Marx et al., 2012). Three typical dampers are depicted in Fig. 8.1, where the elements in the dashed line are used for damping. According to the structure and position of the damper, the three dampers are called the *RC* parallel damper (Fig. 8.1(a)), the *RL* parallel damper (Fig. 8.1(b)) and the *RL* series damper (Fig. 8.1(c)), respectively. For the system shown in Fig. 8.1(d) with these dampers, the peak of the output impedance of the *LC* input filter can be damped and a total separation between $|Z_o|$ and $|Z_{iL}|$ ensured to fulfil Middlebrook stability criterion (Middlebrook, 1979). Here, Z_o is the output impedance of the damped *LC* input filter and Z_{iL} is the input impedance of the CPL.

Although these filter dampers can stabilisze the cascaded system, their impact on the *LC* input filter is always ignored and rarely reported. In this chapter, their impact was carefully analysed via two-port network analysis, and it was found that all these dampers degrade the original *LC* input filter performance to some extent. To solve this problem, a *RLC* damper is proposed which could not only can stabilise the system whilst improving

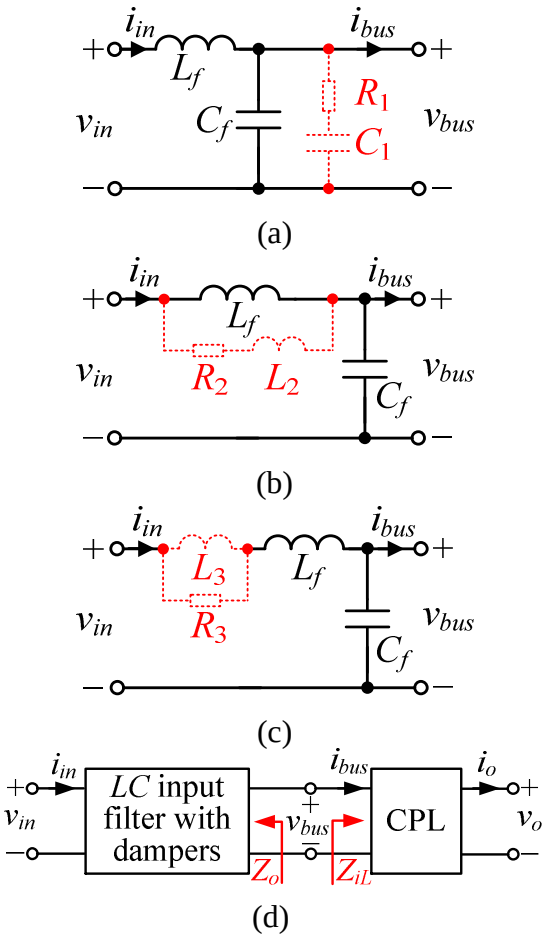


Figure 8.1: Typical dampers and their application: (a) *RC* parallel damper; (b) *RL* parallel damper; (c) *RL* series damper; (d) application.

the performance of the *LC* input filter, but also achieve high robustness to the parameter variations of the *LC* input filter. Based on the *RLC* damper, a virtual *RLC* (*VRLC*) damper is further proposed to avoid the power loss of the passive components by changing the control block of the CPL. The actual effectiveness of this *VRLC* damper and its impact on the CPL are also discussed. It should be stressed that although the *VRLC* damper is similar to the PVI control strategy in Chapter 2, they are fundamentally different. The PVI control strategy stabilises the system by shaping the load input impedance, without considering the source performance. However, the *VRLC* damper stabilises the system by shaping the output impedance of the *LC* input filter whilst improving the filter performance. Finally, the proposed *VRLC* damper is experimentally verified by a 100 W 48 V - 24 V Buck converter with a *LC* input filter.

The remaining parts of this chapter are organised as follows: in Section 8.1, the existing dampers and their impact on the *LC* input filter are discussed. The *RLC* damper is proposed in Section 8.2, where its design consideration, advantages/disadvantages and impact on the *LC* input filter are also analysed. Following that, the *RLC* damper is virtual realised in Section 8.3, where the control and effectiveness of the *VRLC* damper are also discussed. In Section 8.4, both the existing dampers and proposed *VRLC* damper are utilised as an actual cascaded system, whose experimental results verify the effectiveness of the *VRLC* damper. Finally, Section 8.5 concludes the chapter.

8.1 Existing Dampers and Their Impact on the *LC* Input Filter

8.1.1 Review of the Existing Dampers

In this section, the existing dampers are reviewed under the same design principle: $6dB\Omega$ system gain margin (GM) (Wildrick, 1993).

8.1.1.1 *RC* Parallel Damper

According to (Erickson and Maksimov, 2001), Fig. 8.1(a) and $6dB\Omega$ GM stability requirement, the components C_1 and R_1 of the *RC* parallel damper can be designed as

$$C_1 = n_1 C_f \tag{8.1}$$

$$R_1 = R_{of} \cdot \sqrt{\frac{(2+n_1)\cdot(4+3n_1)}{2\cdot n_1^2\cdot(4+n_1)}} \tag{8.2}$$

where

$$R_{of} = \sqrt{\frac{L_f}{C_f}} \tag{8.3}$$

$$n_1 = \frac{R_{of}^2}{\left(Z_{iL}/10^{\frac{6}{20}}\right)^2}\left\{1+\sqrt{1+4\frac{\left(Z_{iL}/10^{\frac{6}{20}}\right)^2}{R_{of}^2}}\right\} \tag{8.4}$$

8.1.1.2 *RL* Parallel Damper

According to (Erickson and Maksimov, 2001), Fig. 8.1(b) and $6\,dB\Omega$ GM stability requirement, the components L_2 and R_2 of the *RL* parallel damper can be designed as

$$L_2 = n_2 L_f \tag{8.5}$$

$$R_2 = R_{of} \cdot \sqrt{\frac{n_2 \cdot (3+4n_2) \cdot (1+2n_2)}{2 \cdot (1+4n_2)}} \tag{8.6}$$

where

$$n_2 = \frac{1}{4}\left\{ \sqrt{1+4\frac{\left(Z_{iL}/10^{\frac{6}{20}}\right)^2}{R_{of}^2}} - 1 \right\} \tag{8.7}$$

8.1.1.3 *RL* Series Damper

According to (Erickson and Maksimov, 2001), Fig. 8.1(c) and $6\,dB\Omega$ GM stability requirement, the components L_3 and R_3 of the *RL* series damper can be designed as

$$L_3 = n_3 L_f \tag{8.8}$$

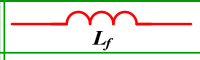
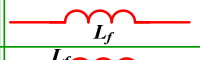
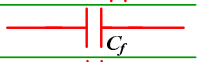
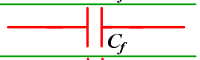
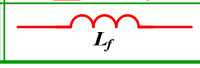
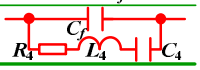
$$R_3 = R_{of} \cdot \left[\frac{(1+n_3)}{n_3} \cdot \sqrt{\frac{2 \cdot (1+n_3) \cdot (4+n_3)}{(2+n_3) \cdot (4+3n_3)}} \right]^{-1} \tag{8.9}$$

where

$$n_3 = \left[\sqrt{1+4 \cdot \frac{\left(Z_{iL}/10^{\frac{6}{20}}\right)^2}{R_{of}^2}} + 3 \right] \cdot \left\{ \frac{\left(Z_{iL}/10^{\frac{6}{20}}\right)^2}{R_{of}^2} - 2 \right\}^{-1} \tag{8.10}$$

All the above dampers can ensure a total separation of $|Z_o|$ and $|Z_{iL}|$ to stabilise the system (Erickson and Maksimov, 2001; Cespedes et al., 2011). However, their impact on the *LC* input filter has not been analysed sufficiently in the existing literature. For this reason, the impact of existing dampers on the *LC* input filter is carefully analysed here using the two-port network model in Sections 8.1.2 and 8.1.3.

Table 8.1: Definitions of $A_x(s)$ and $B_x(s)$ in different dampers

LC input filter	A_x	B_x
Original (x=0)		
RC parallel damper (x=1)		
RL parallel damper (x=2)		
RL series damper (x=3)		
Proposed damper (x=4)		

8.1.2 Two-Port Network Model of the *LC* Input Filter with Different Dampers

In Fig. 8.2(a), the generic two-port network circuit model of the *LC* input filter with different dampers is presented, where v_{in} and v_{bus} are the filter input and output voltage, respectively; i_{in} and i_{bus} are the filter input and output current, respectively; and $A_x(s)$ and $B_x(s)$ represent the impedance of the filter inductor branch and capacitor branch, respectively. A further description of $A_x(s)$ and $B_x(s)$ is presented in Table 8.1. In Fig. 8.2(b), the two-port block diagram of Fig. 8.2(a) is given, where $Z_{ox}(s)$ is the output impedance; $1/Z_{ix}(s)$ is the input voltage to input current transfer function; $G_{vx}(s)$ is the input to output voltage transfer function; $G_{ix}(s)$ is the load to input current transfer function. Here, the subscript $x = 0 \sim 4$ denotes with no damper, *RC* parallel damper, *RL* parallel damper, *RL* series damper and the latter proposed damper, respectively. As is known, the performance of the *LC* input filter can be fully described by $Z_{ox}(s) \sim G_{ix}(s)$, which can be derived as

$$Z_{ox}(s) = -\left.\frac{\hat{v}_{bus}(s)}{\hat{i}_{bus}(s)}\right|_{\hat{v}_{in}(s)=0} = \frac{A_x(s)\cdot B_x(s)}{A_x(s)+B_x(s)} \tag{8.11}$$

$$1/Z_{ix}(s) = \left.\frac{\hat{i}_{in}(s)}{\hat{v}_{in}(s)}\right|_{\hat{i}_{bus}(s)=0} = \frac{1}{A_x(s)+B_x(s)} \tag{8.12}$$

$$G_{vx}(s) = \left.\frac{\hat{v}_{bus}(s)}{\hat{v}_{in}(s)}\right|_{\hat{i}_{bus}(s)=0} = \frac{B_x(s)}{A_x(s)+B_x(s)} \tag{8.13}$$

$$G_{ix}(s) = \left.\frac{\hat{i}_{in}(s)}{\hat{i}_{bus}(s)}\right|_{\hat{v}_{in}(s)=0} = \frac{B_x(s)}{A_x(s)+B_x(s)} \tag{8.14}$$

It is worth noting that according to (8.13) and (8.14), $G_{vx}(s)$ and $G_{ix}(s)$ have the same expression.

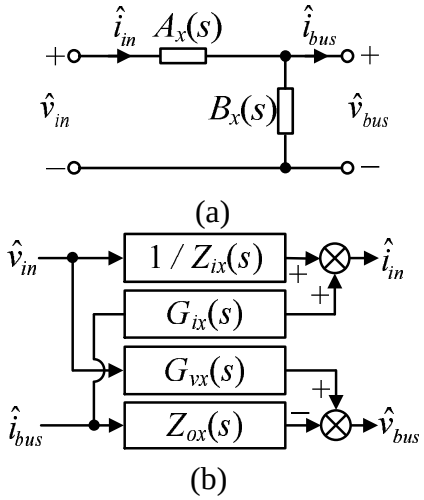


Figure 8.2: Generic two-port network model of the *LC* input filter with different dampers: (a) circuit model; (b) block diagram.

8.1.3 Impact of Existing Dampers on the *LC* Input Filter via Two-port Network Analysis

According to Section 8.1.2, the performance of the *LC* input filter can be fully evaluated by two-port network analysis with four transfer functions: $Z_{ox}(s)$, $1/Z_{ix}(s)$, $G_{vx}(s)$ and $G_{ix}(s)$, where $Z_{ox}(s)$ reflects the impact of the (load) current i_{bus} on the (load) voltage v_{bus}; $1/Z_{ix}(s)$ reflects the impact of (input) voltage variations of v_{in} on the (input) current i_{in}; $G_{vx}(s)$ reflects the impact of (input) voltage variations of v_{in} on the (load) voltage v_{bus}; $G_{ix}(s)$ reflects the impact of the (load) current i_{bus} on the (input) current i_{in}. However, all the existing dampers are only focused on how to damp $|Z_{ox}(s)|$ to ensure the system stability while ignoring their other impact on $Z_{ox}(s)$, $1/Z_{ix}(s)$, $G_{ix}(s)$ and $G_{vx}(s)$. Therefore, in order to analyse the impact of the existing dampers on the *LC* input filter, the existing dampers impact on $Z_{ox}(s)$, $1/Z_{ix}(s)$, $G_{vx}(s)$ and $G_{ix}(s)$ are thoroughly analysed in this section. Moreover, in order to show the results in a clear way, a specific *LC* input filter is taken as an example to facilitate the analysis. The parameters of the example *LC* input filter and its dampers are given in Table 8.2, where the existing dampers are designed, according to (Erickson and Maksimov, 2001), with $6\,dB\Omega$ system GM. In addition, For the CPL, its Z_{iL} is equal to $-V_{bus}^2/P_o$, where P_o is the output power of the CPL and its value is also listed in Table 8.2.

According to (8.11), Table 8.1 and Table 8.2, the Bode plots of $Z_{ox}(s)$ with different

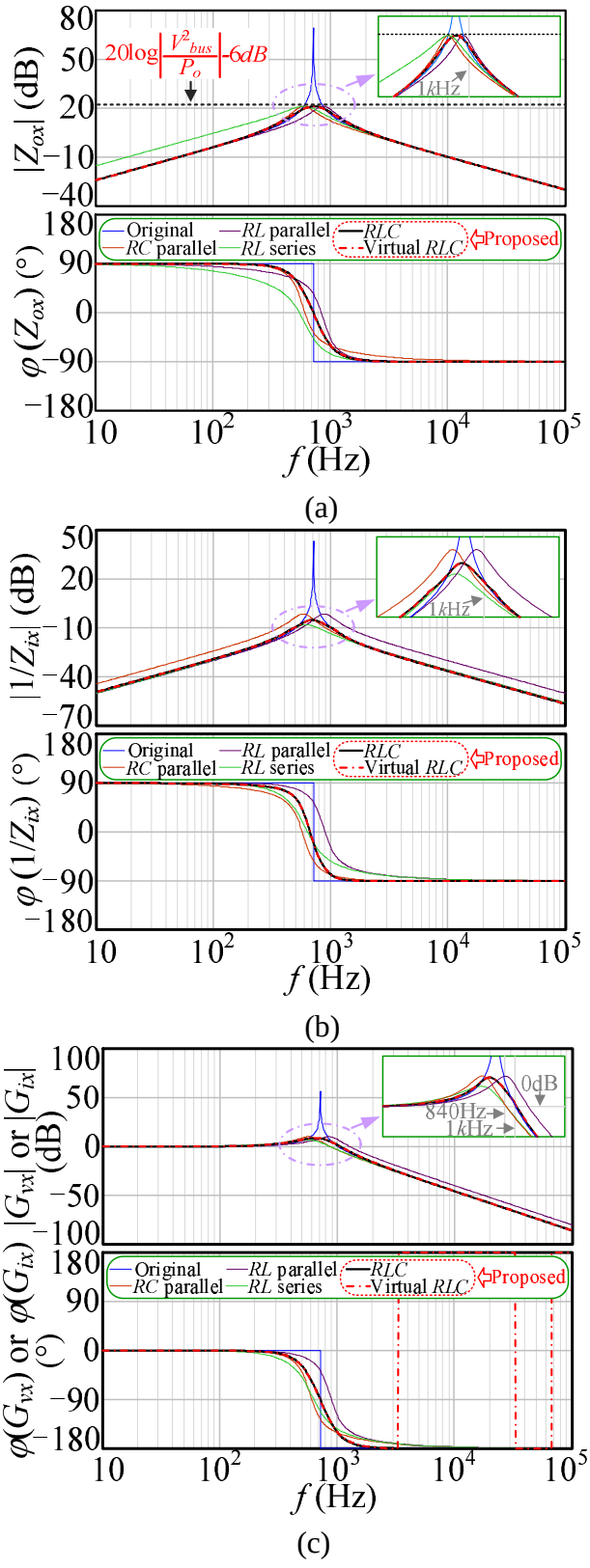


Figure 8.3: Impact of different dampers on the *LC* input filter: (a) $Z_{ox}(s)$; (b) $1/Z_{ix}(s)$; (c) $G_{vx}(s)$ & $G_{ix}(s)$.

Table 8.2: Parameters of the example *LC* input filter with different dampers

PARM.	*Value*	*PARM.*	*Value*	*PARM.*	*Value*	*PARM.*	*Value*
V_{in}	48 V	C_f	50 μF	L_2	1.5 mH	L_4	1.9 mH
V_{bus}	48 V	R_1	6.5 Ω	R_3	1.7 Ω	C_4	27 μF
P_o	100 W	C_1	60 μF	L_3	1 mH		
L_f	1 mH	R_2	6.5 Ω	R_4	11.5 Ω		

dampers are depicted in Fig. 8.3(a). It can be seen that the peak of $|Z_{ox}(s)|$ can be damped by all the dampers to ensure $6dB\Omega$ GM stability of the cascaded system. However, the *RL* series damper increases $|Z_{ox}(s)|$ at the lower frequency range. Since a higher $|Z_{ox}(s)|$ means a poorer suppression of v_{bus} to the disturbance of i_{bus}, the *RL* series damper has a worse impact on $Z_{ox}(s)$.

According to (8.12), Table 8.1 and Table 8.2, the Bode plots of $1/Z_{ix}(s)$ with different dampers are presented in Fig. 8.3(b). It is shown that, though the peak of $|1/Z_{ix}(s)|$ can be damped by all the dampers, the *RC* parallel and *RL* parallel dampers increase $|1/Z_{ix}(s)|$ at the lower and higher frequency ranges, respectively. Since a higher $|1/Z_{ix}(s)|$ means a worse suppression ability of i_{in} to the disturbance of v_{in}, both *RC* parallel and *RL* parallel dampers have a worse impact on $1/Z_{ix}(s)$.

By (8.13) and (8.14), since $G_{vx}(s)$ and $G_{ix}(s)$ have the same expression, they are depicted by the same Bode plots in Fig. 8.3(c).

When $G_{vx}(s)$ has a higher cut-off frequency, v_{bus} has a quick dynamic response to v_{in}. Hence, the higher the cut-off frequency of $G_{vx}(s)$, the better. According to Fig. 8.3(c), the cut-off frequency of $G_{vx}(s)$ is increased when adopting the *RL* parallel damper, but reduced when adopting the *RC* parallel or *RL* series dampers. Therefore, the *RL* parallel damper has better impact, but the *RC* parallel and *RL* series dampers have a worse impact on $G_{vx}(s)$.

For $G_{ix}(s)$, since it reflects the suppression capability of i_{in} to the harmonic of i_{bus}, it determines the resistance to electromagnetic interference (EMI) of the *LC* input filter (Erickson and Maksimov, 2001). From this perspective, the lower the cut-off frequency of $G_{ix}(s)$ and the smaller the $|G_{ix}(s)|$, the better. According to Fig. 8.3(c), the resonant peak of $|G_{ix}(s)|$ can be damped by all the dampers, the cut-off frequency and amplitude of $G_{ix}(s)$ is reduced by both *RC* parallel and *RL* series dampers. However, the *RL* parallel damper increases the cut-off frequency and amplitude of $G_{ix}(s)$. Therefore, both *RC* parallel and *RL* series dampers have a better impact, though the *RL* parallel damper has worse impact

Table 8.3: Impact on *LC* input filter with different dampers

Damper \ Impact	$Z_{ox}(s)$	$1/Z_{ix}(s)$	$G_{vx}(s)$	$G_{ix}(s)$	System stability
Without damper	Normal	Normal	Normal	Normal	Unstable
RC PAR.	Better	Worse	Worse	Better	Stable
RL PAR.	Better	Worse	Better	Worse	Stable
RL SER.	Worse	Better	Worse	Better	Stable
Proposed damper	Better	Better	Better	Better	Stable

on $G_{ix}(s)$.

The impact of the existing dampers on the *LC* input filter is concluded in Table 8.3. Although all the dampers are able to realise their stabilisation functions, they degrade the performance of the *LC* input filter to some extent. Note that, the impact of the damper to be proposed later on the *LC* input filter is also included in Table 8.3 for comparison.

8.2 The Proposed *RLC* Damper

8.2.1 Design Principle of the Proposed *RLC* Damper

To overcome the drawbacks of the existing dampers, a *RLC* damper is proposed, and this is added in parallel with the output of the *LC* input filter and composed by a resistor R_4, an inductor L_4 and a capacitor C_4 (See Fig. 8.4(a)). The impedance of this *RLC* damper can be expressed as $Z_{RLC}(s) = R_4 + sL_4 + (1/sC_4)$, whose Bode plot is depicted in Fig. 8.4(b). The characteristics of $Z_{RLC}(s)$ are similar to those of a band-stop filter, whose stop-band is $(f_1,\ f_2)$: If $f < f_1$, $Z_{RLC}(s) = 1/sC_4$; If $f \in [f_1,\ f_2]$, $Z_{RLC}(s) = R_4$; If $f > f_1$, $Z_{RLC}(s) = sL_4$. Thus, the *RLC* damper only plays its damper function during $[f_1,\ f_2]$, in which R_4 is equivalently added in parallel with Z_{o0}. Here, $f_1 = 1/(2\pi R_4 C_4)$ and $f_2 = R_4/(2\pi L_4)$.

For the CPL and its input *LC* filter, if their system does not have enough stability GM, $|Z_{o0}(s)|$ will be intersected with $\left|Z_{iL}/10^{(GM/20)}\right|$. As $Z_{o0}(s) = sL_f/\left(s^2L_fC_f+1\right)$ and $Z_{iL}(s) = -V_{bus}^2/P_o$, the Bode plots of $Z_{o0}(s)$ and $Z_{iL}/10^{(GM/20)}$ are depicted in Fig. 8.4(c). As seen, $|Z_{o0}(s)|$ is intersected with $\left|Z_{iL}/10^{(GM/20)}\right|$ at f_L and f_H, where

$$f_L = \frac{1}{2\pi}\cdot\frac{P_o 10^{(GM/20)}}{2C_f V_{bus}^2}\left[\sqrt{1+4V_{bus}^4\frac{C_f}{\left(P_o 10^{(GM/20)}\right)^2 L_f}}-1\right] \tag{8.15}$$

$$f_H = \frac{1}{2\pi}\cdot\frac{P_o 10^{(GM/20)}}{2C_f V_{bus}^2}\left[\sqrt{1+4V_{bus}^4\frac{C_f}{\left(P_o 10^{(GM/20)}\right)^2 L_f}}+1\right] \tag{8.16}$$

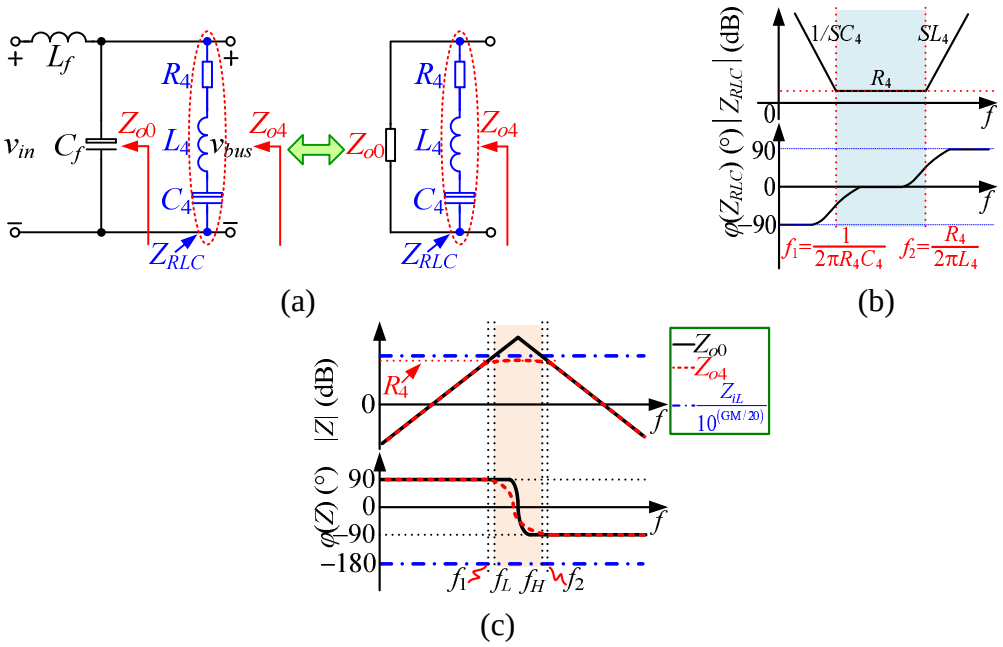


Figure 8.4: The *RLC* damper: (a) structure; (b) characteristics; (c) design principle.

Since $Z_{o4}(s) = Z_{o0}(s) \parallel Z_{RLC}(s)$ and according to the Figs. 8.4(b) and (c), if the system GM is required to be realised with a minimum impact of the *RLC* damper, three basic design principles of the *RLC* damper should be satisfied: (1) $R_4 = \left|(V_{bus}^2) / \left[P_o 10^{(GM/20)}\right]\right|$; (2) $f_1 = f_{Lmin}$; (3) $f_2 = f_{Hmax}$. Here, f_{Lmin} is the minimum value of f_L, f_{Hmax} is the maximum value of f_{Hmax}. Following these design principles, the Bode plot of $Z_{o4}(s)$ is plotted with dashed lines in Fig. 8.4(c). $|Z_{o4}(s)|$ is only changed during $[f_1,\ f_2]$ and always lower than $\left|Z_{iL}/10^{(GM/20)}\right|$ to ensure the system GM.

8.2.2 Parameters Selection of the Proposed *RLC* Damper to Achieve High Robustness against the Variations of L_f and C_f

According to Section 8.2.1, the impedance characteristics of the *RLC* damper behave like the band-stop filter shown in Fig. 8.4(b), whose stop-band is $(f_1,\ f_2)$. As discussed above, if the *RLC* damper wants to stabilise the whole system with a minimum impact on the *LC* input filter, f_1 and f_2 should be equal to f_{Lmin} and f_{Hmax}, respectively. However, according to (8.15) and (8.16), both f_L and f_H are affected by L_f and C_f. In Figs. 8.5 (a) and (b), the curves of $\frac{f_L}{f_{LR}}$ vs $\frac{L_f}{L_{fR}}$ or $\frac{C_f}{C_{fR}}$ are presented respectively. L_{fR} and C_{fR} are the rated value of L_f and C_f respectively, f_{LR} is the value of f_L under L_{fR} and C_{fR}. f_L is monotonically

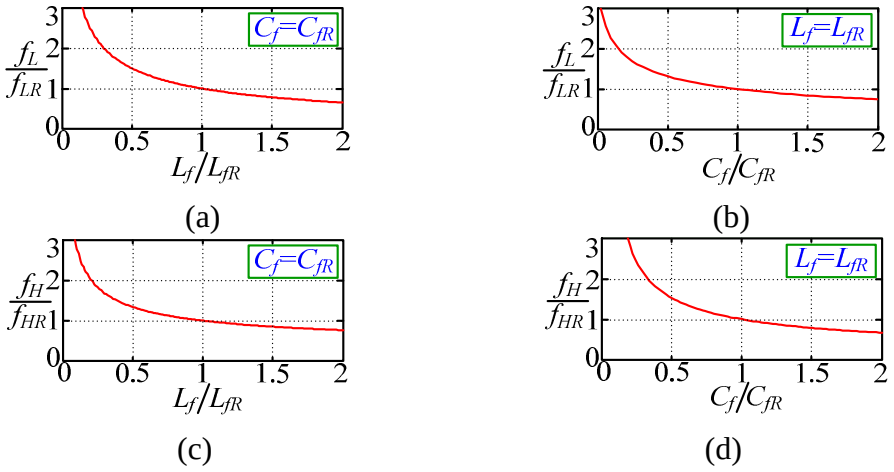


Figure 8.5: The relationship between f_L, f_H and L_f, C_f: (a) $\frac{f_L}{f_{LR}}$ vs $\frac{L_f}{L_{fR}}$; (b) $\frac{f_L}{f_{LR}}$ vs $\frac{C_f}{C_{fR}}$; (c) $\frac{f_H}{f_{HR}}$ vs $\frac{L_f}{L_{fR}}$; (d) $\frac{f_H}{f_{HR}}$ vs $\frac{C_f}{C_{fR}}$.

decreased when L_f or C_f increases. Similarly, the curves of $\frac{f_H}{f_{HR}}$ vs $\frac{L_f}{L_{fR}}$ or $\frac{C_f}{C_{fR}}$ are also presented in Figs. 8.5 (c) and (d) respectively, where f_{HR} is the value of f_H under L_{fR} and C_{fR}. It is shown that, f_H is also monotonically decreased when L_f or C_f increases.

In practice, the value of L_f and C_f are not constant, but vary according to different operation conditions, such as working frequency and temperature. It is assumed that the value of L_f or C_f varies between $(\alpha_L L_{fR} \sim \beta_L L_{fR})$ and $(\alpha_C C_{fR} \sim \beta_C C_{fR})$ respectively, then by Fig. 8.5, the expression of f_{Lmin} and f_{Hmax} can be derived as

$$f_{Lmin} = \frac{1}{2\pi} \cdot \frac{P_o 10^{(GM/20)}}{2\beta_C C_{fR} V_{bus}^2} \left[\sqrt{1 + 4V_{bus}^4 \frac{\beta_C C_{fR}}{\left(P_o 10^{(GM/20)}\right)^2 \beta_L L_{fR}}} - 1 \right] \tag{8.17}$$

$$f_{Hmax} = \frac{1}{2\pi} \cdot \frac{P_o 10^{(GM/20)}}{2\alpha_C C_{fR} V_{bus}^2} \left[\sqrt{1 + 4V_{bus}^4 \frac{\alpha_C C_{fR}}{\left(P_o 10^{(GM/20)}\right)^2 \alpha_L L_{fR}}} + 1 \right] \tag{8.18}$$

Since $f_1 = f_{Lmin}$ and $f_2 = f_{Hmax}$, by Fig. 8.4(b), (8.17) and (8.18), the parameters of the *RLC* damper can be selected as

$$L_4 = R_4 / \left\{ \frac{P_o 10^{(GM/20)}}{2\alpha_C C_{fR} V_{bus}^2} \left[\sqrt{1 + 4V_{bus}^4 \frac{\alpha_C C_{fR}}{\left(P_o 10^{(GM/20)}\right)^2 \alpha_L L_{fR}}} + 1 \right] \right\} \tag{8.19}$$

$$C_4 = 1 / \left\{ \frac{R_4 P_o 10^{(GM/20)}}{2\beta_C C_{fR} V_{bus}^2} \left[\sqrt{1 + 4V_{bus}^4 \frac{\beta_C C_{fR}}{\left(P_o 10^{(GM/20)}\right)^2 \beta_L L_{fR}}} - 1 \right] \right\} \tag{8.20}$$

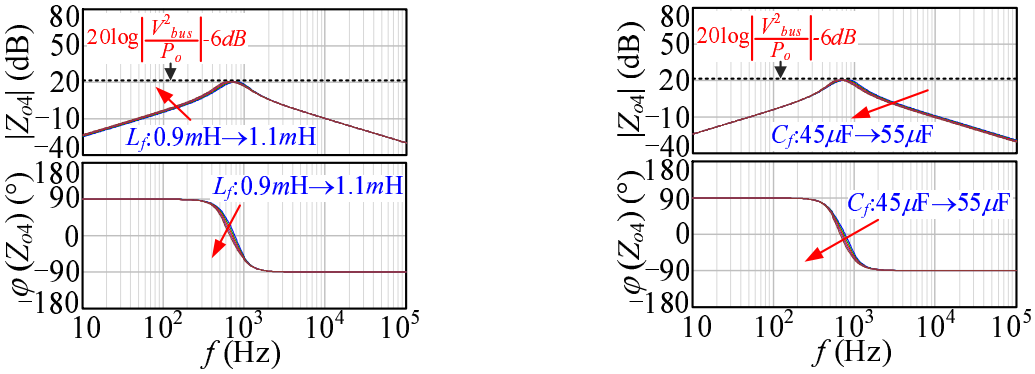


Figure 8.6: Bode plots of $Z_{o4}(s)$ when L_f or C_f changes: (a) $L_f : 0.9mH \rightarrow 1.1mH$, $C_f = 50\mu F$; (b) $L_f = 1mH$, $C_f : 45\mu F \rightarrow 55\mu F$.

where $R_4 = \left|V_{bus}^2 / \left[P_o 10^{(GM/20)}\right]\right|$.

In order to further verify the correctness of the robust design of the *RLC* damper, (8.19) and (8.20) are substituted in the example *LC* input filter in Table 8.2 to calculate R_4, L_4 and C_4 under the following assumptions: $\alpha_L = \alpha_C = 0.9$; $\beta_L = \beta_C = 1.1$. It can then be obtained that, $R_4 = 11.5\Omega$, $L_4 = 1.9mH$ and $C_4 = 27\mu F$. Based on the calculated parameters, the Bode plots of $Z_{o4}(s)$ with the variations of L_f or C_f are depicted in Figs. 8.6(a) and (b), respectively. It is shown that, whether L_f or C_f vary within $0.9 \sim 1.1$ of its rated value, $|Z_{o4}(s)|$ is always lower than $\left|Z_{iL}/10^{(GM/20)}\right|$ ($GM = 6dB$) to realise its damping function. Therefore, the designed *RLC* damper indeed achieves high robustness against the variations of L_f and C_f.

8.2.3 The Impact of the Proposed *RLC* damper on the *LC* Input Filter

According to (8.11)∼(8.14), Table 8.1 and Table 8.2, the Bode plots of $Z_{ox}(s)$, $1/Z_{ix}(s)$, $G_{vx}(s)$ and $G_{ix}(s)$ of the *LC* input filter with the proposed *RLC* damper can be depicted and presented in Fig. 8.3 as well. In contrast to the existing dampers, though the *RLC* damper has the same stabilisation function, it has better impact on all the transfer functions (e.g., $Z_{ox}(s)$, $1/Z_{ix}(s)$, $G_{vx}(s)$ and $G_{ix}(s)$) of the *LC* input filter. The impact of the proposed *RLC* damper on the *LC* input filter is recorded in Table 8.3 as ' proposed damper '. Here, it is shown that, the proposed *RLC* damper is superior to the existing dampers.

It is worth pointing out that although the proposed *RLC* damper can stabilise the cas-

caded system with a better performance of the *LC* input filter than the existing dampers, it has two potential risks as a high order damper: 1) the *RLC* damper increases the system order, thus, if the *RLC* damper is not designed very well and fails to stabilise the cascaded system, the system instability problem may became more serious for the increased system order; 2) the *RLC* damper needs more passive components, which may cause unacceptable power loss and volume to the cascaded system. To avoid the first potential risk, the *RLC* damper should strictly abide by the proposed design principle to ensure the cascaded system is stable. To avoid the second potential risk, the *RLC* damper can be virtually realised by the control method proposed in the following section.

8.3 Virtual Implementation of the Proposed *RLC* Damper

As is well known, the adoption of passive damper can lead to significant power loss. In order to avoid this problem, a control strategy is proposed in this chapter to realise the proposed *RLC* damper as a virtual *RLC* (*VRLC*) damper.

8.3.1 Concept and Implementation of the *VRLC* Damper

As shown in Fig. 8.4(a), as the proposed *RLC* damper must be added in parallel with output port of the *LC* input filter, it can be realised by putting a virtual *RLC* damper in parallel with the input port of the CPL via control method to avoid additional power loss. This is the initial inspiration for the *VRLC* damper.

As shown in Fig. 8.7(a), the small-signal control block of a typical CPL is presented. Its variables and transfer functions are described in Table 8.4. Obviously, one intuitive way of realising the *VRLC* damper is to introduce its admittance $1/Z_{RLC}(s)$ to the control block of the CPL between its input voltage v_{bus} and input current i_{bus}, as shown in the dark dot-dashed lines in Fig. 8.7(a). However, this method cannot be achieved by control directly, and as a result the output of $1/Z_{RLC}(s)$ is actually moved to the output voltage reference and equivalently adjusts the transfer function to $G_{RLC}(s)$, as represented by the dashed lines in Fig. 8.7(a).

According to Fig. 8.7(a), if $G_{RLC}(s)$ is required to realise the virtual *RLC* damper

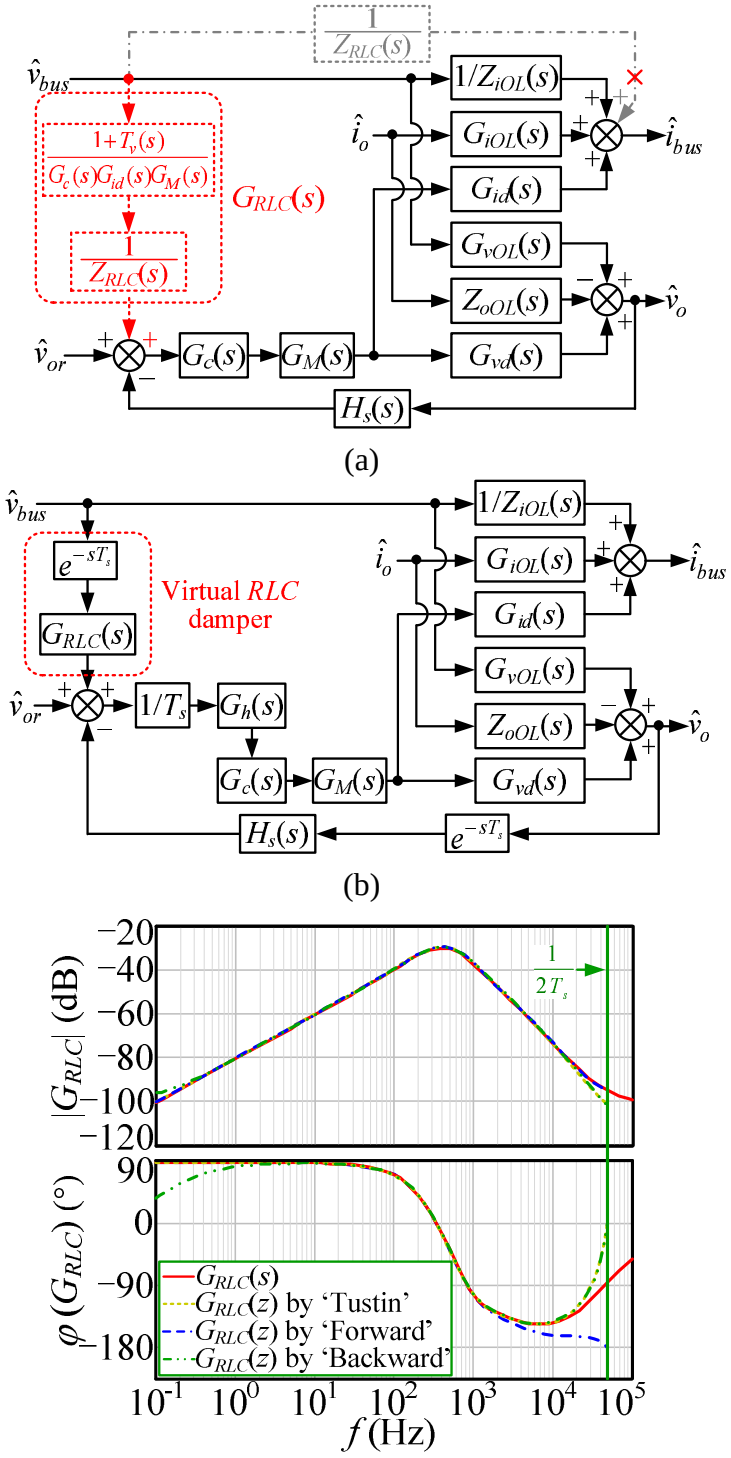


Figure 8.7: Control strategy of the *VRLC* damper: (a) concept; (b) digital implementation; (c) different discretization effect of $G_{RLC}(s)$.

Table 8.4: Variables and transfer functions of the CPL

$\hat{v}_{bus}$	Perturbation of the bus voltage
$\hat{i}_o$	Perturbation of the load current
$\hat{i}_{bus}$	Perturbation of the bus current
$\hat{d}$	Perturbation of the duty cycle
$\hat{v}_o$	Perturbation of the output voltage
$\hat{v}_{or}$	Perturbation of the output voltage reference
$G_c(s)$	Transfer function of the voltage regulator
$G_M(s)$	Transfer function of the modulator
$Z_{iOL}(s)$	Open-loop input impedance
$G_{vd}(s)$	Control to output voltage transfer function
$G_{id}(s)$	Control to input current transfer function
$Z_{oOL}(s)$	Open-loop output impedance
$H_s(s)$	Sampling coefficient of the output voltage
$G_{iOL}(s)$	Open-loop load to input current transfer function
$G_{vOL}(s)$	Open-loop input to output voltage transfer function

$1/Z_{RLC}(s)$, the following relationship can be obtained:

$$\hat{v}_{bus} \cdot \frac{1}{Z_{RLC}(s)} = \hat{v}_{bus} \cdot G_{RLC}(s) \cdot G_c(s) \cdot G_M(s) \cdot G_{id}(s) \cdot \frac{1}{1+T_v(s)} \tag{8.21}$$

where $T_v(s) = H_s(s)G_c(s)G_M(s)G_{vd}(s)$ is the loop gain of the voltage closed loop of the CPL.

According to (8.21), the expression of $G_{RLC}(s)$ can be derived as:

$$G_{RLC}(s) = \frac{1}{Z_{RLC}(s)} \cdot \frac{1+T_v(s)}{G_c(s) \cdot G_{id}(s) \cdot G_M(s)} \tag{8.22}$$

Up to this point, Fig. 8.7(a) fully presents the concept of the *VRLC* damper and shows the whole derivation process of $G_{RLC}(s)$.

In practice, the *VRLC* damper can be implemented by a digital control chip, such as a Digital Signal Processor (DSP) or a Micro-controller Unit (MCU). In Fig. 8.7(b), the digital control based small signal model of the CPL with the *VRLC* damper is presented. The digital control introduces two types of delay to the control system: the computation delay and the pulse width modulation (PWM) delay (Holmes et al., 2009). The computation delay is one sampling period in the commonly used synchronous sampling scheme, which can be modelled as $e^{-T_s s}$. The PWM delay is caused by the zero-order hold (ZOH) effect, which can be expressed as $G_h(s) = \left(1-e^{-T_s s}\right)/s \approx T_s e^{-0.5T_s s}$. Here, T_s is the sampling time of the digital control system.

According to Fig. 8.7(b), the *VRLC* damper actually only adds $G_{RLC}(s)$ to the original control system of the CPL. Hence, realising $G_{RLC}(s)$ is the key to realise the *VRLC* damper. Since Backward Euler, Forward Euler and Tustin are three typical discretization methods in digital control, they are all utilised to convert $G_{RLC}(s)$ to $G_{RLC}(z)$. In order to compare their discretization effect clearly, the Bode plots of $G_{RLC}(s)$ and $G_{RLC}(z)$ with different discretization methods of a specific CPL are depicted in Fig. 8.7(c), where the example CPL corresponds to the experimental system in Section 8.4. According to Fig. 8.7(c), $G_{RLC}(z)$ with the Tustin discretization method is the closest to $G_{RLC}(s)$. Therefore, the Tustin discretization method is selected to convert $G_{RLC}(s)$ to $G_{RLC}(z)$ in the final digital control system of this chapter.

8.3.2 Effectiveness Evaluation of the *VRLC* Damper

Since the purpose of the *VRLC* damper is to mimic the *RLC* damper by changing the control block of the *CPL*, the actual effectiveness of the *VRLC* damper is evaluated carefully with the comparison of the *RLC* damper in this section.

According to Fig. 8.7(b), the input impedance of the CPL with the *VRLC* damper $Z_{iL}^{V}(s)$ can be derived as

$$Z_{iL}^{V}(s) = \left.\frac{\hat{v}_{bus}(s)}{\hat{i}_{bus}(s)}\right|_{\hat{i}_o(s)=0} = \left(\frac{1}{Z_{iL}(s)} + \frac{1}{Z_{VRLC}(s)}\right)^{-1} \tag{8.23}$$

where

$$Z_{iL}(s) = \left[\frac{1}{Z_{iOL}(s)}\frac{1}{1+T_{vd}(s)} - \frac{T_{vd}(s)}{1+T_{vd}(s)}\left(\frac{1}{Z_{iOL}(s)} - \frac{G_{id}(s)G_{vOL}(s)}{G_{vd}(s)}\right)\right]^{-1} \tag{8.24}$$

$$Z_{VRLC}(s) = \left(1+T_{vd}(s)\right)/T_{id}(s) \tag{8.25}$$

$$T_{vd}(s) = (1/T_s)\,e^{-sT_s}G_h(s)H_s(s)G_c(s)G_M(s)G_{vd}(s) \tag{8.26}$$

$$T_{id}(s) = (1/T_s)\,e^{-sT_s}G_h(s)G_{RLC}(s)G_{id}(s)G_M(s)G_c(s) \tag{8.27}$$

By (8.23), the *VRLC* damper adds a virtual impedance $Z_{VRLC}(s)$ in parallel with $Z_{iL}(s)$ to mimic $Z_{RLC}(s)$ as shown in Fig. 8.8(a). Thus, if the effectiveness of the *VRLC* damper is to be evaluated, only one question need be answered: whether $Z_{VRLC}(s)$ is equal to $Z_{RLC}(s)$

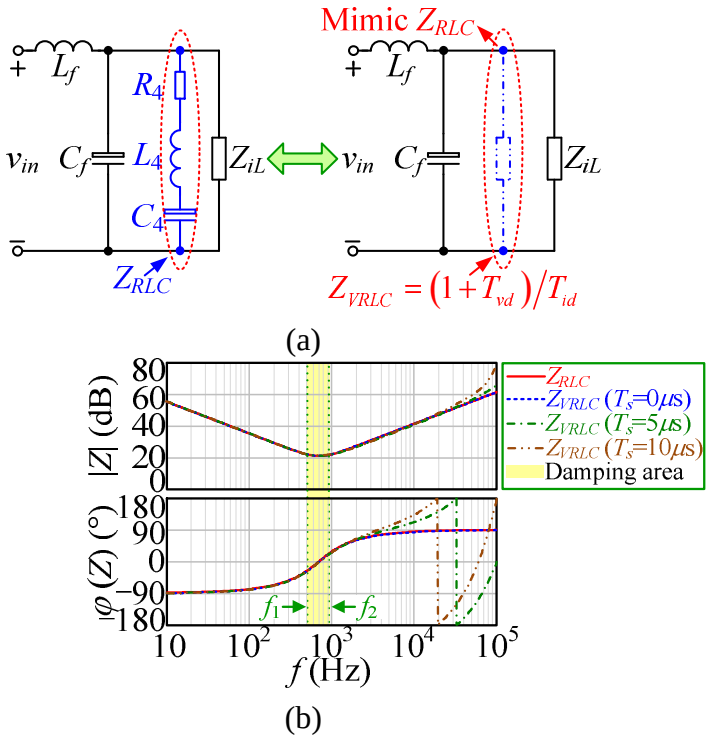


Figure 8.8: Comparison of the *RLC* and *VRLC* dampers: (a) function comparison; (b) Bode plots of $Z_{RLC}(s)$ and $Z_{VRLC}(s)$.

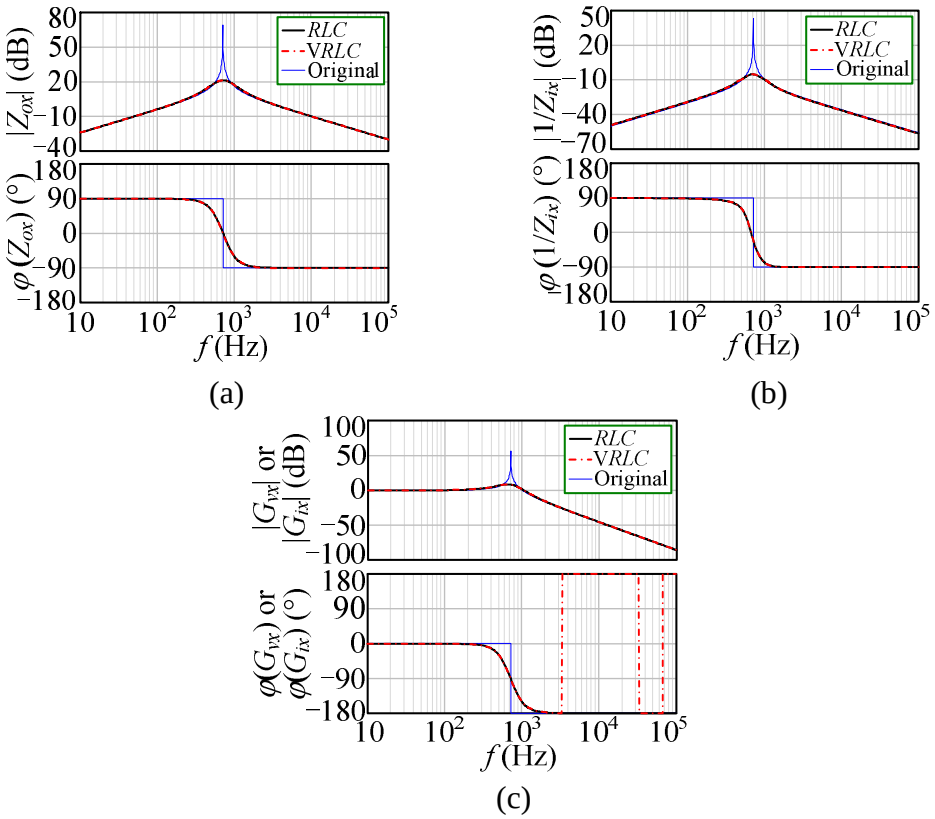


Figure 8.9: Impact of *RLC* and *VRLC* dampers on the *LC* input filter: (a) $Z_{ox}(s)$; (b) $1/Z_{ix}(s)$; (c) $G_{vx}(s)$ & $G_{ix}(s)$.

or not? As a result, (8.22) is substituted by (8.25) and $Z_{VRLC}(s)$ is re-written as

$$Z_{VRLC}(s) \approx Z_{RLC}(s) \cdot \left(\frac{e^{1.5sT_s} + T_v(s)}{1 + T_v(s)} \right) \tag{8.28}$$

According to (8.28), if $T_s = 0$, $Z_{VRLC}(s)$ is equal to $Z_{RLC}(s)$; if $T_s \neq 0$, $Z_{RLC}(s)$ and $Z_{VRLC}(s)$ will become different near the sampling frequency, and the larger T_s, the bigger the difference. In order to compare $Z_{RLC}(s)$ and $Z_{VRLC}(s)$ clearly, the Bode plots of $Z_{RLC}(s)$ and $Z_{VRLC}(s)$ of a specific CPL are further depicted in Fig. 8.8(b), where the example CPL corresponds to the experimental system in Section 8.4. As seen, the curves of $Z_{RLC}(s)$ and $Z_{VRLC}(s)$ are indeed completely coincident when $T_s = 0$. And if $T_s \neq 0$, $Z_{RLC}(s)$ and $Z_{VRLC}(s)$ only become different near sampling frequency and their difference is bigger with the increase of T_s. The Bode plots in Fig. 8.8(b) support the accuracy of (8.28).

Therefore, the effectiveness of the *VRLC* damper is only affected by the time delay (or sampling time) of the digital control system and the smaller time delay the better. In this chapter, considering T_s cannot be smaller than the execution time of the program, $10\,\mu s$ is selected as the sampling time for the experimental system. As shown in Fig. 8.8(b), when $T_s = 10\,\mu s$, though $Z_{VRLC}(s)$ becomes difference with $Z_{RLC}(s)$ at high frequencies, it is the same with $Z_{RLC}(s)$ at other frequency range, especially in the damping frequency area of the *RLC* damper. Therefore, for the experimental system, the *VRLC* damper can mimic the *RLC* damper very well.

In addition, in order to compare the impact of the *RLC* and *VRLC* dampers on the *LC* input filter, the Bode plots of $Z_{ox}(s) \sim G_{ix}(s)$ of the *LC* input filter with both *RLC* and *VRLC* dampers are also depicted in Fig. 8.9. It can be seen that both *RLC* and *VRLC* dampers can improve the performance of the *LC* input filter, and that their impacts are almost the same. It is worth pointing out that, in order to compare the impact of the proposed dampers and the existing dampers on the *LC* input filter, the Bode plots in Fig. 8.9 are also presented in Fig. 8.3, which clearly shows that both *RLC* and *VRLC* dampers have a better impact than the existing dampers on the *LC* input filter. In addition, both *RLC* and *VRLC* dampers are referred to as 'proposed damper', and their impact on the *LC* input filter are also recorded as 'proposed damper' in Table 8.3.

8.3.3 The Impact of the *VRLC* Damper on the CPL

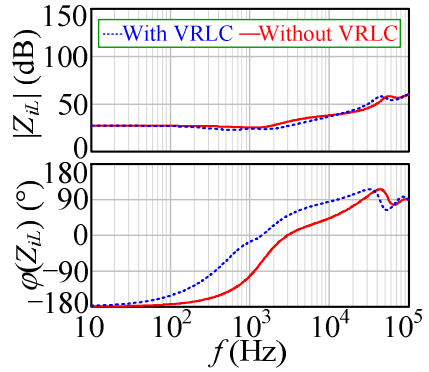
The performance of the CPL can be fully evaluated by a two-port network with four typical transfer functions (Arnedo, 2008): the closed-loop input impedance $Z_{iL}(s)$, the closed-loop output impedance $Z_{oL}(s)$, the closed-loop load to input current transfer function $G_{iL}(s)$ and the closed-loop input to output voltage transfer function $G_{vL}(s)$. Therefore, in order to evaluate the impact of the *VRLC* damper on the CPL in a clear way, the Bode plots of $Z_{iL}(s) \sim Z_{oL}(s)$ of a specific CPL with/without the *VRLC* damper are depicted in Fig. 8.10.

In Fig. 8.10, the example CPL corresponds to the experimental system in Section 8.4. Other than adding $Z_{VRLC}(s)$ in parallel with $Z_{iL}(s)$ to mimic the function of the $Z_{RLC}(s)$, the *VRLC* damper keeps most of the other performances of the original CPL. Therefore, the *VRLC* damper is also acceptable in practice.

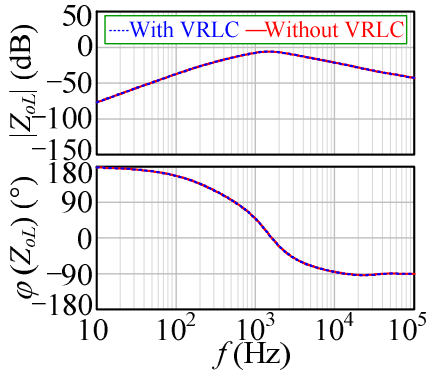
8.4 Experimental Verification

In this chapter, experimental results from a 100 W cascaded system that consists of a *LC* input filter and a 48 V / 24 V digital controlled (sampling frequency is 100 kHz) Buck converter, are shown to validate the *VRLC* damper. The main circuit and parameters of the cascaded system are presented in Fig. 8.11(a), which also shows the parameters of the *VRLC* damper: $R_4 = 11.5\,\Omega$, $L_4 = 1.9\,mH$, $C_4 = 27\,\mu F$. When there is no dampers utilised in this system, the steady-state experimental waveforms at rated load and input voltage are given in Fig. 8.11(b). This system is unstable without any dampers.

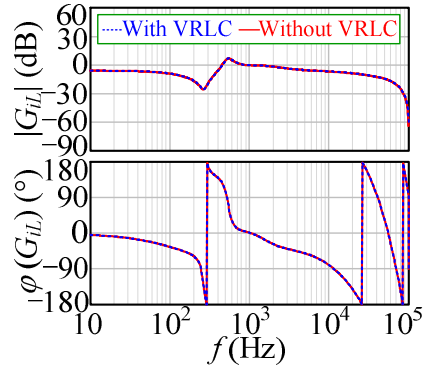
In Fig. 8.12, the full load experimental results are given of the cascaded system with different dampers when the input voltage changing from 80% rated voltage (38.4 V) to 100% rated voltage (48 V), where i_{in}, v_{bus}, i_{L1} and v_o are defined in Fig. 8.11, v_{bus} and v_o are their ac components. Three conclusions can be obtained from Fig. 8.12. Firstly, though the cascaded system is unstable without dampers, it can be stabilised by the existing dampers or the *VRLC* damper. Thus, both the existing dampers and the *VRLC* damper have the same stabilisation function. Secondly, with these dampers, the cascaded system works well during input voltage changing. Thirdly, a distinctly better dynamic performance from the *LC* input filter is obtained by the *VRLC* damper than by the existing stabilisation dampers. The dynamic performances of the *LC* input filter with different dampers are presented and



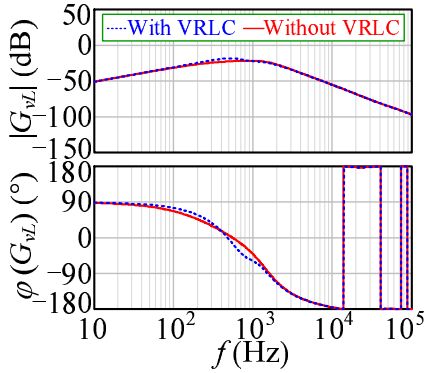
(a)



(b)



(c)



(d)

Figure 8.10: Impact of the *VRLC* damper on the CPL: (a) $Z_{iL}(s)$; (b) $Z_{oL}(s)$; (c) $G_{iL}(s)$; (d) $G_{vL}(s)$.

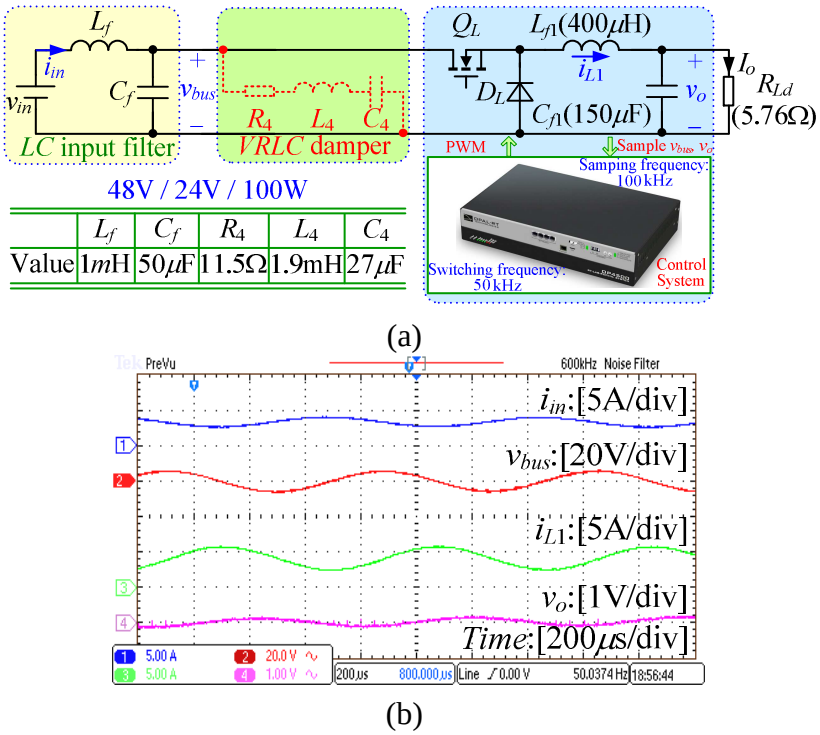
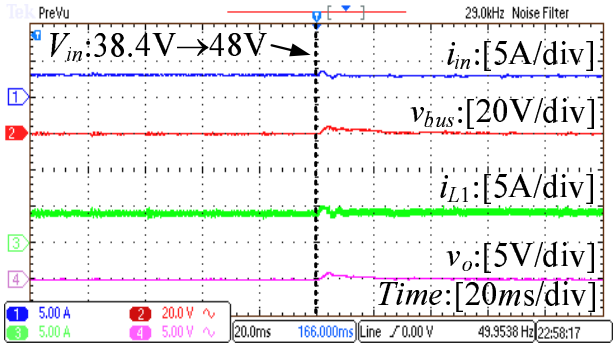


Figure 8.11: The experimental system: (a) main circuit; (b) steady state experimental waveforms at rated conditions without any dampers.

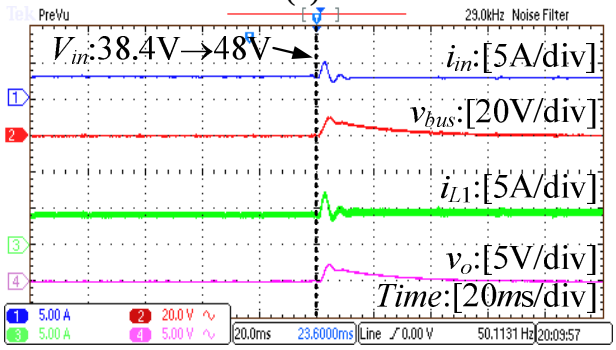
further compared in Fig. 8.13, where $\sigma_{I_{in}}$ and $t_{I_{in}}$ are the overshoot and regulation time of i_{in}, respectively, and $\sigma_{V_{bus}}$ and $t_{V_{bus}}$ are the overshoot and regulation time of v_{bus}, respectively. It is further shown that when the input voltage changes, the dynamic indicators of the *LC* input filter with *VRLC* damper are superior to those of the existing stabilisation dampers. It is also worth mentioning that, for a fair comparison, in this experiment the existing dampers are all realised by passive components as reported in the original literature (Erickson and Maksimov, 2001; Cespedes et al., 2011).

Similarly, when the output power is changed from 10 W to 100 W under rated input voltage, the experimental results of the cascaded system and the dynamic indicators of the *LC* input filter with different dampers are given in Figs. 8.14 and 8.15, respectively. Again, it has been verified that when the load changes, the *VRLC* damper has a better dynamic impact on the *LC* input filter than the existing dampers.

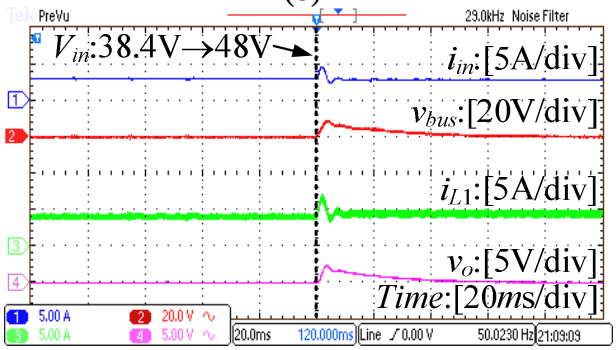
The efficiency curves of the experimental system with different dampers vs output power and input voltage are measured and plotted in Figs. 8.16(a) and (b), respectively. It is shown that, with the *VRLC* damper, the system efficiency is clearly improved. This



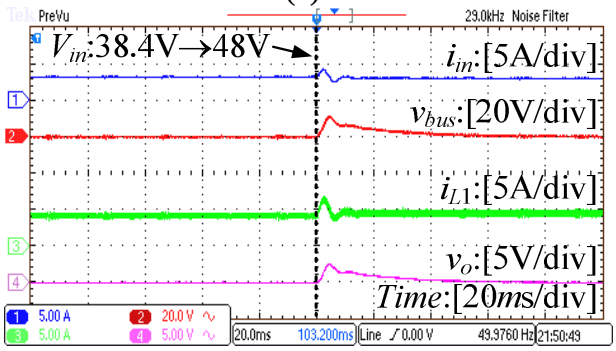
(a)



(b)



(c)



(d)

Figure 8.12: Experimental waveforms with different dampers when system input voltage changed from 80% to 100% rated voltage at full load: (a) with *VRLC* damper; (b) with *RC* parallel damper; (c) with *RL* parallel damper; (d) with *RL* series damper.

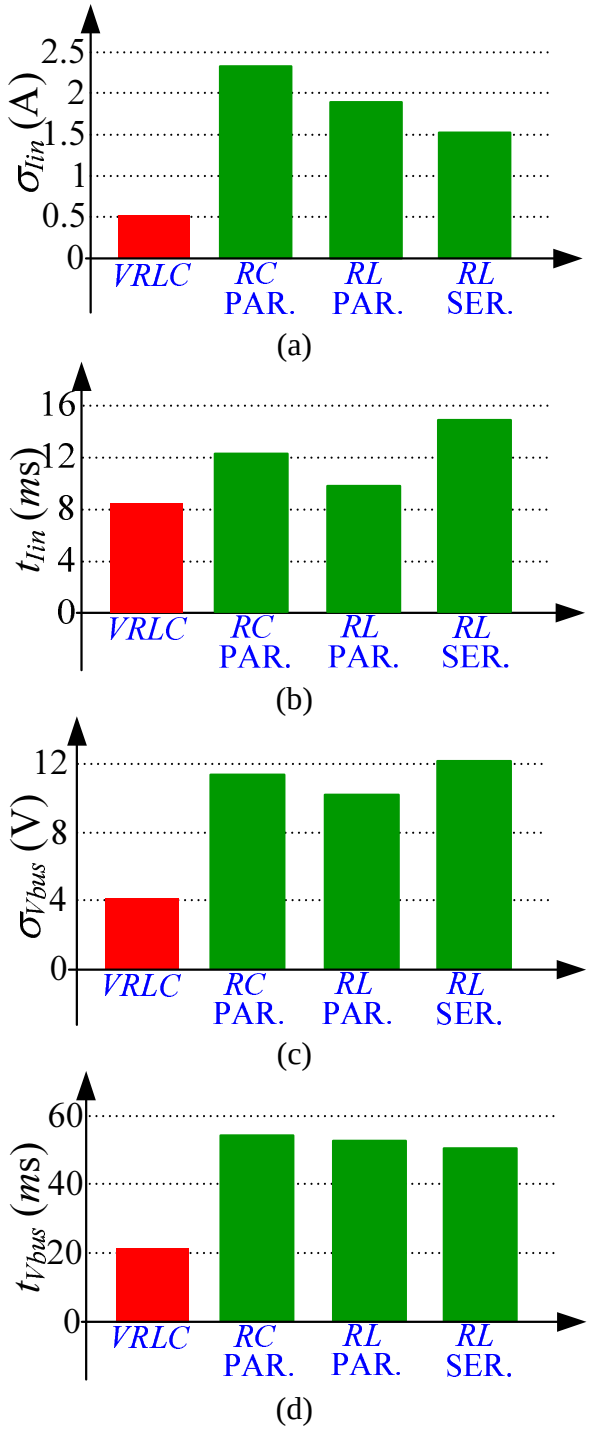
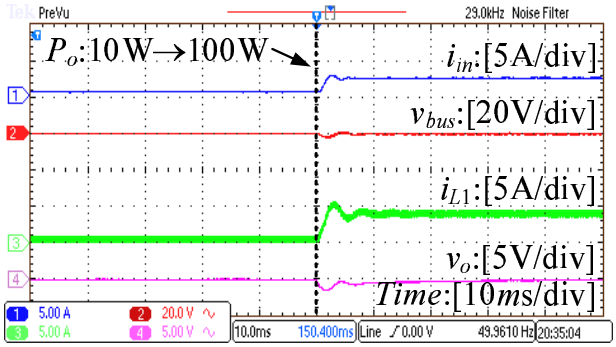
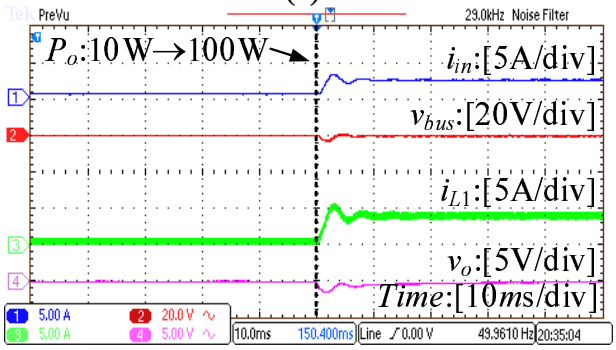


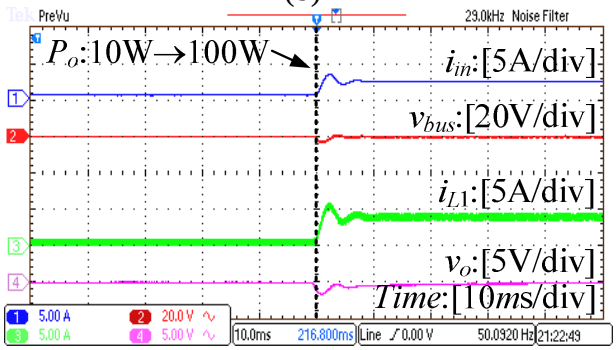
Figure 8.13: Comparison of $\sigma_{I_{in}}$, $t_{I_{in}}$, $\sigma_{V_{bus}}$ and $t_{V_{bus}}$ with different dampers when system input voltage changed from 80% to 100% rated voltage at full load: (a) $\sigma_{I_{in}}$; (b) $t_{I_{in}}$; (c) $\sigma_{V_{bus}}$; (d) $t_{V_{bus}}$.



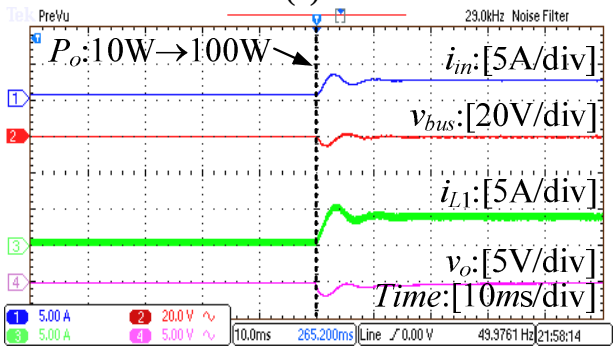
(a)



(b)



(c)



(d)

Figure 8.14: Experimental waveforms with different dampers when system output power changed from 10 W to 100 W at rated input voltage: (a) with *VRLC* damper; (b) with *RC* parallel damper; (c) with *RL* parallel damper; (d) with *RL* series damper.

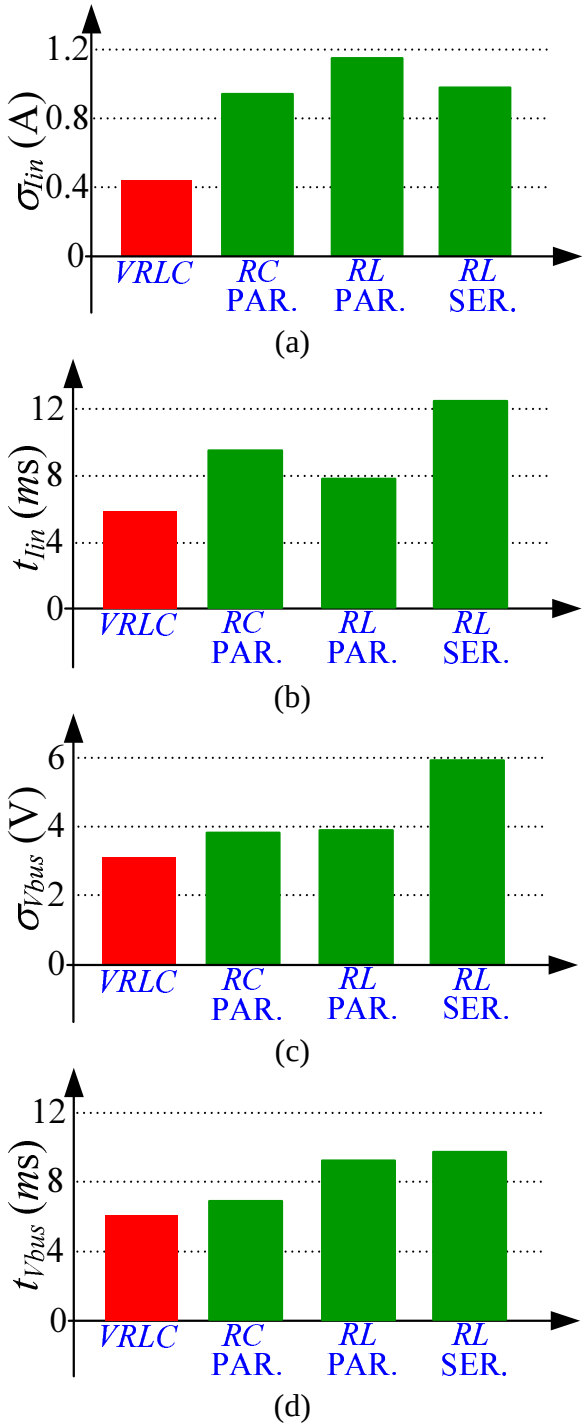


Figure 8.15: Comparison of $\sigma_{I_{in}}$, $t_{I_{in}}$, $\sigma_{V_{bus}}$ and $t_{V_{bus}}$ with different dampers when system output power changed from 10 W to 100 W at rated input voltage: (a) $\sigma_{I_{in}}$; (b) $t_{I_{in}}$; (c) $\sigma_{V_{bus}}$; (d) $t_{V_{bus}}$.

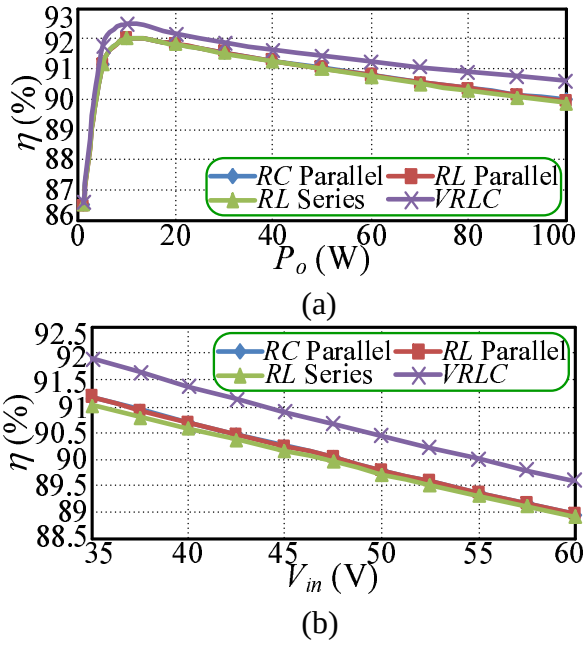


Figure 8.16: System efficiency curves with different dampers: (a) efficiency vs p_o at rated v_{in}; (b) efficiency vs v_{in} at rated p_o.

phenomenon can be explained as follows: the *VRLC* damper is realised by the control method, but the existing dampers depend on passive components, thus the *VRLC* damper avoids the power loss of the damper.

Therefore, according to Fig. 8.12 $\sim$ Fig. 8.16, the *VRLC* damper can not only stabilise the whole system, but also have a better impact on the performance of the *LC* input filter and improve the system efficiency compared with existing dampers.

8.5 Summary

The impact of the existing dampers (e.g., *RC* parallel damper, *RL* parallel damper and *RL* series damper) on the *LC* input filter has been, firstly, analysed using the two-port network model described in this chapter. It was found that although the above dampers could solve the instability problem of the CPL with its *LC* input filter, they degraded the performance of the original *LC* input filter to some extent. In order to overcome this, a *RLC* damper is proposed here. With this damper, the whole system can be stabilised whilst improving the performance of the *LC* input filter. In addition, the *RLC* damper is robustly resists the parameter variations of the *LC* input filter. In order to avoid the power loss

caused by passive components, the proposed *RLC* damper is further virtually implemented by control. This indicates that the *VRLC* damper not only has the same effectiveness as the *RLC* damper, but also improves the efficiency of the whole system compared to the existing dampers. Finally, the *VRLC* damper has been experimentally verified in a 100 W cascaded system.

Chapter 9

Conclusions and Future Work

This chapter summarises the work of the whole thesis and concludes with some valuable recommendations for future work.

9.1 Conclusions

In this thesis, existing stabilisation methods for the cascaded system have been reviewed. It is highlighted that although these stabilisation methods can stabilise the cascaded system, they have unavoidable drawbacks, e.g., they do not have enough load stabilisation methods, they require all the information on the cascaded system, they degrade the original performance of the cascaded system, and so on. In order to overcome these drawbacks, a family of software-based stabilisation methods has been proposed by this thesis.

Firstly, a set of virtual-impedance-based control strategies, named PVI and SVI control strategies, are proposed. The PVI or SVI control strategy connects a virtual impedance in parallel or series with the input impedance of the load converter so that the magnitude or phase of the load input impedance is modified in a very small frequency range. As a result, with the PVI or SVI control strategy, the cascaded system can be stabilised with minimal load compromise. Therefore, both the PVI and SVI control strategies can not only be treated as developments of, and complements to the load stabilisation methods, but can also be treated as good solutions to overcome the contradiction between the stability and performance of the cascaded system.

Based on the PVI and SVI control strategies, adaptive-PVI (APVI) and adaptive- SVI (ASVI) control strategies are further proposed to incorporate the adaptive function. With

the APVI or ASVI control strategy, the load converter can be stably connected to different source converters without changing their internal structure. In this thesis, the APVI and ASVI control strategies are also carefully compared. It is found that the ASVI control strategy can transform the cascaded system into an unconditional stable system without any limitations, but the APVI control strategy cannot. As a result, the ASVI control strategy is superior to the APVI control strategy.

Though the ASVI control strategy is thus far the most competitive load stabilisation method, it is not perfect. As the ASVI control strategy utilises a PI controller to find the centre frequency of the ASVI, this PI controller may miss the right frequency with excessive proportional or integral coefficients and cause the failure of the ASVI control strategy. Although this problem may not arise with small proportional and integral coefficients, it is a hidden problem for the ASVI control strategy. To make the ASVI control strategy more reliable, a MRPT controller is proposed to replace the original PI controller. With the MRPT controller, the ASVI control strategy can find the centre frequency of the ASVI without encountering the problem. Furthermore, in order to find the centre frequency of ASVI quickly, the STA is further introduced into the MRPT controller to improve its processing speed. Therefore, the improved MRPT controller makes the improved ASVI control strategy more competitive.

In addition, stabilising the cascaded system is always in conflict with maintaining the original performance of the cascaded system. Though the proposed PVI/SVI and APVI/ASVI control strategies have already minimised their impact on the cascaded system in a very small frequency range, the rest of their impact is negative. In order to resolve this, a SSVI control strategy and a *VRLC* damper are proposed in this thesis. With the SSVI control strategy, the cascaded system can be stabilised with a better dynamic performance of the source converter. Similarly, the *VRLC* damper can stabilise the cascaded system while improving the performance of the input filter. Therefore, both the SSVI control strategy and the *VRLC* damper overcome the contradiction between the stability and performance of the cascaded system perfectly. In addition, since the SSVI control strategy stabilises the system by changing the control block of the source converter, it is not only suitable for the cascaded system with one upstream converter and one downstream converter, but also for the distributed power system with multiple upstream converters and one

downstream converter.

Therefore, the stabilisation methods proposed in this thesis overcome all of the drawbacks of the existing solutions. As a consequence, it is believed that these stabilisation methods will become increasingly popular in the near future.

9.2 Future Work

In order to further stabilise the cascaded system, there is specific research that should be conducted in the future.

1. Applying the PVI/SVI/APVI/ASVI control strategies into the AC/DC rectifier and DC/AC inverter: in this thesis, the PVI/SVI/APVI/ASVI control strategies are only proposed to change the input impedance of the DC/DC converter. However, the cascaded system still has other types of load converters, such as AC/DC rectifier and DC/AC inverter. Therefore, they also need the above impedance control methods if the system is unstable. Considering the essence of the PVI/SVI/APVI/ASVI control strategies is adding a special virtual impedance in parallel or series with the input port of the load converter to shape the load input impedance, future research efforts should focus on how realising these virtual impedances on the AC/DC rectifier and DC/AC inverter.

2. Applying the SSVI control strategy to the AC/DC rectifier: in this thesis, the SSVI control strategy is proposed to shape the output impedance of the DC/DC converter. However, the cascaded system may sometimes use the AC/DC rectifier as the source converter. Therefore, it is preferable to realise the SSVI control strategy on the AC/DC rectifier. Considering the essence of the SSVI control strategy is adding a virtual impedance in the series with the output port of the source converter to shape the source output impedance, methods of realising this virtual impedance on the AC/DC rectifier can be considered by future research work.

3. Needing to reduce the program execution time of the proposed stabilisation methods. With the development of the new semiconductor devices, such as Gallium Nitride (GaN) and Silicon Carbide (SiC) switches, their switching frequency can be

greatly increased, which is the benefit of the new semiconductor devices. However, for power converters, switching frequency is also limited by the program execution time of their control methods. Therefore, if the program execution time of the proposed stabilisation methods is too great, it will limit the new semiconductor devices application in power converters.

4. Developing stabilisation methods for the three-phase AC cascaded system: in this thesis, the cascaded system refers to the cascaded DC/DC converter system. However, if the cascaded system is a three-phase AC cascaded system (i.e., its intermediate bus voltage is a three-phase AC voltage), the stability criteria and the impedance requirement of the source or load converters will be entirely different. Therefore, it is better to develop the stabilisation methods for the three-phase AC cascaded system which can also be included in the future work program.

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Appendix A

Fundamental Concepts of Constant Power Load (CPL) — Negative Resistor Characteristic

First, with regard to any closed-loop converter, as its loop strives to maintain a constant output voltage or current, it also tries to maintain a constant output power P_{out} to a particular load. From this point of view, any closed-loop converter can be treated as a constant power load (CPL).

If an ammeter is then inserted into a series with the CPL, and the input line modulated, one will find that as its input voltage V_{in} grows, its input current i_{in} diminishes, which strives to keep P_{out} constant. Therefore, from this input side, the CPL looks like a negative resistor, which can also be explained as follows.

Where the CPL is assumed to have 100% efficiency, its behaviour can be described via a few lines of algebra:

$$P_{in} = P_{out} = I_{in}V_{in} = I_{out}V_{out} \tag{A.1}$$

where, P_{in}, I_{in} and V_{in} are the input power, input current and input voltage of the CPL respectively. P_{out}, I_{out} and V_{out} are the output power, output current and output voltage of the CPL respectively.

Then, the inverse of the DC transfer ratio μ, can be obtained by rearranging (A.1):

$$\frac{V_{in}}{V_{out}} = \frac{I_{out}}{I_{in}} = \mu \tag{A.2}$$

The static input resistance of the CPL can simply be calculated from

$$R_{in} = \frac{V_{in}}{I_{in}} \tag{A.3}$$

The incremental resistance can be expressed as

$$R_{inc} = \frac{dV_{in}}{dI_{in}} \tag{A.4}$$

This expression represents the way this resistance moves with perturbations. Via simple manipulations, the incremental resistance can be formulated:

$$V_{in} = \frac{P_{in}}{I_{in}} \tag{A.5}$$

$$P_{in} = P_{out} = R_L I_{out}^2 \tag{A.6}$$

where, R_L can represent another switching regulator, a simple resistor, or a linear regulator.

Plugging (A.6) into (A.5) and deriving as (A.4) suggests yield

$$\frac{dV_{in}}{dI_{in}} = \frac{d}{dI_{in}} \frac{R_L I_{out}^2}{I_{in}} \tag{A.7}$$

$$R_{inc} = -R_L \frac{I_{out}^2}{I_{in}^2} = -R_L \mu^2 \tag{A.8}$$

(A.8) can then be reformulated as

$$R_{inc} = -\frac{V_{out}}{I_{out}} \mu^2 = -\frac{V_{out}^2}{P_{out}} \mu^2 = -\frac{V_{in}^2}{P_{out}} \tag{A.9}$$

Therefore, if a converter operates as a CPL, its input impedance behaves as a negative resistor. Please keep in mind that, the DC/DC converter only acts as a CPL and has a negative input impedance within the cut-off frequency of its closed loop. In other words, if the same converter operated in open-loop or at higher frequency band, it would lose its negative input impedance.