A Multi-level Multi-Modular Flying Capacitor Voltage Source Converter for High Power Applications

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The candidate confirms that the work submitted is his own, except where work which has formed part of jointly-authored publications has been included. The contribution of the candidate and the other authors to this work has been explicitly indicated below. The candidate confirms that appropriate credit has been given within the thesis where reference has been made to the work of others.

Selected Publications:

1. I.B. Efika, and L. Zhang: 'A Cascaded Flying Capacitor Multilevel Converter for HVDC and FACTS'. Proc. UHVnet 2011 Colloquim, Winchester, United Kingdom.
2. I.B. Efika, and L. Zhang: 'An Overlapping Hexagon Space Vector Modulation Scheme applied to a Cascaded Floating Capacitor Modular Multilevel Converter'. Proc. EPE 2013 Conference, Lille, France.
3. I.B. Efika, C.J. Nwobu, and L. Zhang: 'Cascaded Modular Flying Capacitor Converter Using Wavelet-Energy Operator Synchronisation for Unbalanced Grid Voltages'. Proc. UHVnet 2013 Colloquim, Glasgow, United Kingdom.
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5. I.B. Efika, and L. Zhang: 'Unipolar PSPWM scheme for High Voltage Applications'. Proc. UHVnet 2014 Colloquim, Surrey, United Kingdom.

Chapters 3 and 4 of this thesis comprise work forming part of the 2nd, 4th, and 5th publications respectively. All work in Chapters 1, 2, 3, and 4 are attributable to the candidate under the supervision of Dr. Li Zhang. All work in Chapter 5 are attributable to the candidate under the supervision of Dr. Li Zhang with some advice from Dr. Alan Watson and Prof. Jon Clare.

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Most importantly … To God

Chukwu bu onye nāzùm dika aturu; ó dighi ihe kọrọm.

N'ebe-ita-nri nke ahihia ndu ka O nēme ka m'makpu; N'akuku miri nke izu-ike ka Ọ nedum nwayo.

Ọ nēweghachi nkpuru-obim; Ọ nēdum n'uzọ nile nke ezi omume n'ihi aha-Ya.

Ọzọ, asi na ejem ije na ndagwurugwu onyinyo ọnwu, M'gaghi-atu egwu ihe ọjọ ọ bula; n'ihi na Gi onwe-gi nọyerem: Ndele-Gi na nkpa-n'aka-Gi, ha onwe-ha nākasim obi.

I nēdo table n'usoro n'irum n'anya ndi nākpaḅum: I tewo isim manu; ikom bu inwebiga-ihe-ókè.

Nání idi-nma na ebere gāḅasom ubọchi nile nke ndum: M'gēbi kwa n'ulo Jehova rue ogologo ubọchi nile. (ABU ỌMA 23: 1-6).

Abstract

Two vital and dynamically changing issues are arising in the electric grid - an increase in electrical power demand, and subsequent reduction in power quality. Power electronics based solutions such as the Static Synchronous Compensator are increasingly deployed to mitigate power quality issues while High Voltage DC Transmission converters are currently installed to support the existing grid transmission capacity. Both applications require high power and high voltage power converters using switching devices with limited voltage ratings. The advent of Modular Multilevel Converters (MMC) is one of the recent responses to this need. These use half or full H-bridge circuits stacked up to form a chain, and hence can withstand high voltages using lower-rated switching devices.

This thesis introduces a new member into the MMC family, i.e the Modular Multi-level Flying Capacitor Converter (MMFCC). This uses a three-level flying capacitor full-bridge circuit as a sub-module and offers features of modularity, scalability and fault tolerance. The choice of FC topology in place of the simple H-bridge stems from the FC's ability to offer two extra voltage levels in the sub-module output and hence more degrees of freedom per module in controlling the voltage waveform. A three-level full-bridge FC sub-module uses three capacitors - an outer one for supporting the sub-module voltage, and two inner floating ones with half of the outer one's capacitance and voltage rating. This use of slightly more complex FC sub-modules gives the benefits of a modular structure but without using twice as many sub-modules with their associated capacitors for the same total voltage. The thesis presents the principles of this topology, switching states redundancies and a method for capacitor voltage balancing.

Also discussed are: the configuration of MMCC including the MMFCC in Single-Star Bridge-Cell (SSBC) or Single-Delta Bridge-Cell (SDBC) for FACTS and Battery Energy Storage System (BESS) applications; and Double-Star Chopper-Cell (DSCC) or Double-Star Bridge-Cell (DSBC) for HVDC systems.

A novel overlapping hexagon pulse width modulation scheme is introduced and discussed for switching control of the MMFCC. This uses multiple hexagons all centred on one point, the same in number as the cascaded FC

sub-modules, which are phase displaced relative to each other. The approach simplifies the modulation algorithm and brings flexibility in shaping the output voltage waveforms for different applications.

An MMFCC experimental rig was designed and built in-house to validate some of the simulation results obtained for the modulation of this new topology. Details of the rig as well as results captured are discussed.

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Acronyms

VSC	Voltage Source Converter
STATCOM	Static Synchronous Compensator
HVDC	High Voltage Direct Current
FACTS	Flexible AC Transmission Systems
FCC	Flying Capacitor Converter
DCC	Diode Clamped Converter
NPC	Neutral Point Converter
CHB	Cascaded H Bridge
MMC	Modular Multilevel Converter
OHSVM	Overlapping Hexagon Space Vector Modulation
PSPWM	Phase Shifted Pulse Width Modulation
PDPWM	Phase Disposition Pulse Width Modulation
SVM	Space Vector Modulation
SHE	Selective Harmonics Elimination
AAC	Alternate Arm Converter
MMFCC	Modular Multilevel Flying Capacitor Converter
FC-H	Flying Capacitor Hybrid
SSFCC	Single Star Flying Capacitor Circuit
DSFCC	Double Star Flying Capacitor Circuit
BESS	Battery Energy Storage System
PLL	Phase Locked Loop

Chapter 1
Introduction

1.1 Background Literature

Decades of development in semiconductor devices present opportunities for many applications of power electronic converters. Advances in semiconductor and device physics disciplines such as wide band-gap materials steer towards the development of more robust and even higher-power solid state switches to serve as building blocks in power electronic converters for high power applications.

In electric grid applications, power capacity and quality are predominant directives which also list as key specifications during the design of power electronics converters. A notable power electronics based grid application is the Static Synchronous Compensator (STATCOM) which is installed to facilitate the realisation of stringent electric power quality requirements. Academic impact of the concept can be observed from the early 90's [1] albeit that industrial implementation was not until the late 90's, both in the United States (Sullivan's Static Synchronous Compensator) and the birth of the "modular" STATCOM in the United Kingdom [2].

High Voltage Direct Current (HVDC) systems are another application which use power electronics as the enabling technology [3]. Besides bulk power transfer between two interconnected electric grids which increases the capacity of both grids, a HVDC system provides other functions to support power quality, such as AC fault blocking and reactive power support.

The realisation of STATCOM technology and other Flexible AC Transmission Systems (FACTS) together with the HVDC installations across the globe support the smart and super grid concepts which are gradually becoming a reality.

1.1.1 High Power Applications – The smart and super grid concept

The evolution of an electric grid is mainly driven directly by changes in quality and quantity of power demand which is normally a result of industrialisation and population growth. In developed countries such demand growth is currently low or negligible. On the other hand, developing countries

experience a noticeable and rapid annual increase in demand. These regions are where noticeable changes in the electric grid are expected in the near future.

In certain developing countries such as Nigeria, this impact has begun to materialise. Figure 1.1 displays the percentage change in annual electric consumption (base in kWh) for one developed country (United Kingdom) and three developing countries: Kenya; Nigeria; and Ethiopia between 1971 and 2010 [4]. The consumption values[1] observed for the year 1971 are used as base values for per-unitization (Refer to Appendix A.1 for data).

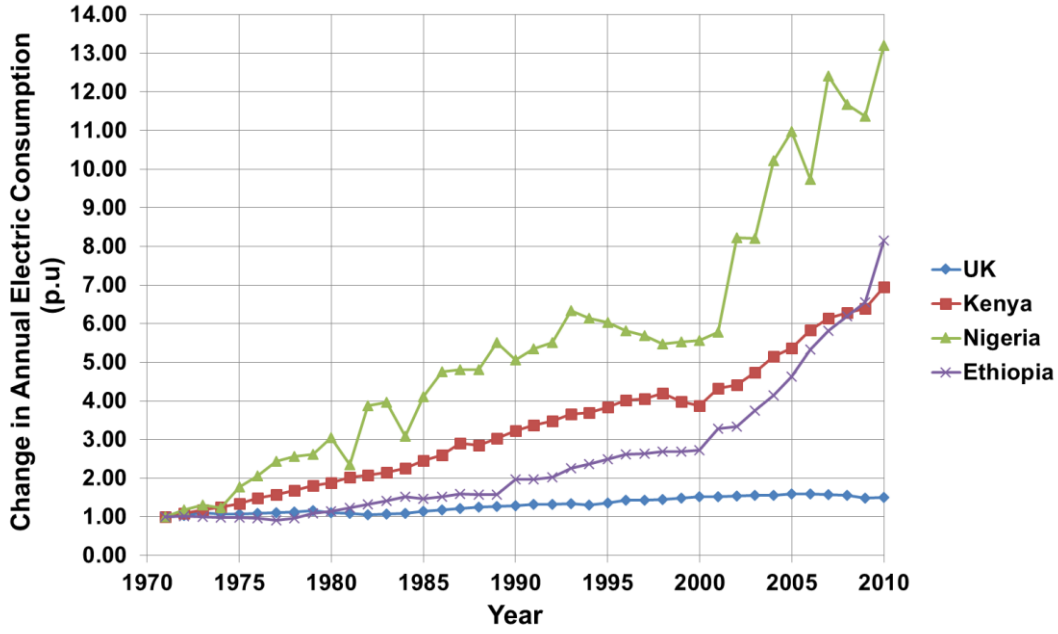

Figure 1.1: Per-unit Change in annual electric consumption for UK, Kenya, Nigeria and Ethiopia between 1970 and 2010.

A continual increase in annual electric consumption is reflected in Figure 1.1 especially for the developing countries, with Nigeria showing an increase of almost 13 times between 1971 and 2010. The United Kingdom plot shows an increase to only 1.5 times the base value (Note this is only an indication of rate of change, UK's consumption value is higher than the rest by an order of hundreds). Clearly developing countries must strive to adopt similar

[1] Annual electricity consumption values for year 1971 (used as base values for per-unitisation): UK – 237.8 TWh; Kenya – 0.9 TWh; Nigeria - 1.6TWh; and Ethopia – 0.5 TWh.

infrastructural changes and philosophies for electric grid management to reduce the alarming rate of rise in electricity consumption.

The smart-grid and super-grid philosophy proposes a generation of electrical networks that tackle grid evolutionary requirements both on a local and global scale.

The smart grid concept introduces systems which enable the utilisation of conventional as well as renewable energy sources to realise a stable and efficient network with minimal environmental impact. In the present deregulated grid, power flow is still mainly unidirectional, from the generating sector (power plants) to the transmission sector and the distribution sector. The smart grid concept promotes a change to a real-time and bi-directional flow of power and information. This introduces a multi-disciplinary field with formidable challenges, most of which are well beyond the scope of this work.

A key aspect of the smart grid concept which is within the scope of this research work is the deployment of several power electronic solutions, such as:

- Battery Energy Storage Systems (BESS) which capture and store electric energy in an electric grid, and supply such energy rapidly (within milliseconds) of demand [5-7];
- Transmission and distribution level FACTS devices such as STATCOMs that dynamically alter an electrical line's parameters to ensure the transfer of high quality power [1, 2, 8];
- Distribution level power electronic converters for interfacing renewable sources with the grid.

Many groups are actively researching the smart grid topic and much literature is available [5-7, 9-18].

The super grid concept introduces a means of interconnecting several electric grids with the main aim being the facilitation of electric power exchange on a global scale. It has often been called the "DC grid", which highlights HVDC as the main enabling system with power electronics as the main enabling technology. Although the main technology required to realise the super grid is available, full development is anticipated to be decades away, partly because of geopolitical implications [19].

Smart-grid and super-grid systems present economic and technical benefits and supplement or replace conventional applications of AC systems but

create additional requirements for the introduction of power electronic systems.

1.1.2 Power Electronics – The enabling technology

A power electronic converter is a circuit normally comprising a plurality of power semiconductor devices and in certain arrangements an auxiliary clamping component (capacitor, inductor, battery, etc.) [20]. While different implementations show variations in device state control and converter configuration based on specific requirements, the main aim of a converter circuit is to interface two homogenous or heterogeneous power systems and enable unidirectional or bi-directional power flow.

Advances in the semiconductor and device physics disciplines enabled the transition away from mercury arc valves to solid-state devices such as the thyristor. With a rugged nature and high current handling capacity, thyristor-based power electronic devices were key, as their implementations in six-pulse, twelve-pulse and twenty-four-pulse configurations provided a platform for implementing diverse high power applications. However, the commutation of a thyristor is quite slow by nature (typically around 300 μs) as well as limited in scope as the device can only be line-commutated and conduct in one direction. As a result, the output of thyristor based systems contain low order harmonics making the system reliant on complex and expensive damping and filtering circuits.

Higher speed switching (typically around 2μs) solid-state devices (MOSFETs, IGBTs) are now available and supported the development of the two-level voltage source converters (2L-VSC). In the 2L-VSC system, a careful modulation technique is applied to such a switch. As a result the system's output will contain harmonics which appear around the switching frequency, thus a high switching frequency produces higher-order harmonics that are easier to filter. An inherent limitation in two-level VSCs is the need to switch at high frequencies as this results in high switching losses that are unacceptable at high power levels. For instance a 1% loss in a 700 MW HVDC converter (i.e. 7 MW) results in a £21,000,000[2] project cost.

[2] The bid price for a HVDC converter comprises a "mandatory" mark-up amount that reflects the converter's lifetime power losses (e.g. 30 years). The "watts" to "price" conversion rate is provided by the customer and typically within the range of £2 - £5/Watt. The value of £3/Watt was

1.2 Overview of Multilevel Converter Topologies

Multilevel converters provide an alternative for realising high power converters.

The concept of multiple voltage levels from a converter can be dated back to 1975 with the design of the three level converter [21, 22].

Multiple voltage levels are provided by stacking extra levels of switches in the converter structure, either through clamping diodes, capacitors or by just cascading electrically isolated cells together.

Consider an inverter with input voltage (V_{DC}) consisting of stacked cells. Each cell synthesizes only a fraction of the input voltage and in most cases, a resulting system with (n_c) stacked cells, will have each level experiencing only a n_c^{th} portion of V_{DC} across it, significantly reducing the voltage stress on the switches in each cell. Studies show that the staircase waveform synthesized at the output contains lower harmonics and has a lower THD at both high and low frequencies of operation. However the inclusion of extra power components (switches, capacitors, and diodes) introduces control complexities and system loss evaluation is more difficult to perform. A brief outline of the established standards for multilevel converters is presented as they have been widely reviewed [23-33].

1.2.1 Neutral Point Clamped (NPC) Converter

Initially proposed by Nabae et al in 1981 [34], the Neutral-Point Clamped (NPC) converter is also known as the diode clamped converter. Diodes are used as the voltage clamping devices to connect extra levels of cells and facilitate synthesising the distinct voltage levels. The most basic form of this converter is the three-level configuration which provides an output with three distinct voltage levels: 0; $V_{DC}/2$; and V_{DC}. A three-level NPC converter is shown in Figure 1.2 first in half bridge, then in H-bridge configuration.

The extra level of switches on each leg of the converter in both configurations (i.e S_a1, S_a4; S_b1, S_b4) is clamped to the neutral point via two diode pairs (D_a1, D_a2; D_b1, D_b2) consequently preventing the voltage in one level from surpassing that in the next level. The equipotential neutral point (N) is provided by two capacitors in series C_1 and C_2 hence the voltage

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adopted in this study such that a 7 MW loss results in a £21,000,000 mark-up.

across these capacitors must be balanced to ensure undistorted levels in the converter output voltage waveform.

Consider the half-bridge arrangement shown in Figure 1.2a, the operating principle is as follows:

- The switching states for S_a1 and S_a2 are co-ordinated in such manner that the voltage that reflects across the AC output (V_{AC}) is either 0, $+0.5V_{DC}$, or $+V_{DC}$.
- **Valid operating states**:
    1. With the devices S_a1 and S_a2 both switched ON, the full DC voltage ($+V_{DC}$) is reflected across the AC output.
    2. With the device S_a1 switched OFF; and S_a2 ON, the voltage across the capacitor C_2 (i.e. $V_{DC}/2$) reflects across the AC output via the clamping diode (D_a1). Diode D_a1 is forward-biased or reverse-blocking depending on the direction of current.
    3. With the devices S_a1 and S_a2 both switched OFF, the AC output is electrically tied to ground i.e. $V_{AC} = 0$.
- **Invalid operating states**:
    1. With the device S_a1 switched ON; and S_a2 OFF, the diode D_a1 goes into forward blocking mode, preventing current from the DC source or the capacitor C_1 to the AC side. The diode D_a2 also blocks a current path from establishing between the capacitor C_2 and the AC side.
- The switching state for S_a3 is always a binary opposite of S_a1 and S_a4 a binary opposite of S_a2. This prevents short-circuit conditions from occurring across the DC rail and the capacitors (C_1, C_2).

The same principle is applicable in the H-bridge configuration shown in Figure 1.2b (i.e. to S_b1, S_b2, S_b3, S_b4). Both “half bridges” that make up the H-bridge are controlled to produce the resulting multilevel voltage waveform.

Switching state redundancies are available as shown in Table 1.1 and this is beneficial as switching stress can be shared among the devices and are also required to balance DC link capacitors C_1 and C_2.

Table 1.1 illustrates the possible operating states for the full-bridge neutral point clamped multilevel inverter, while Figure 1.3 shows the current paths that established by applying the different states.

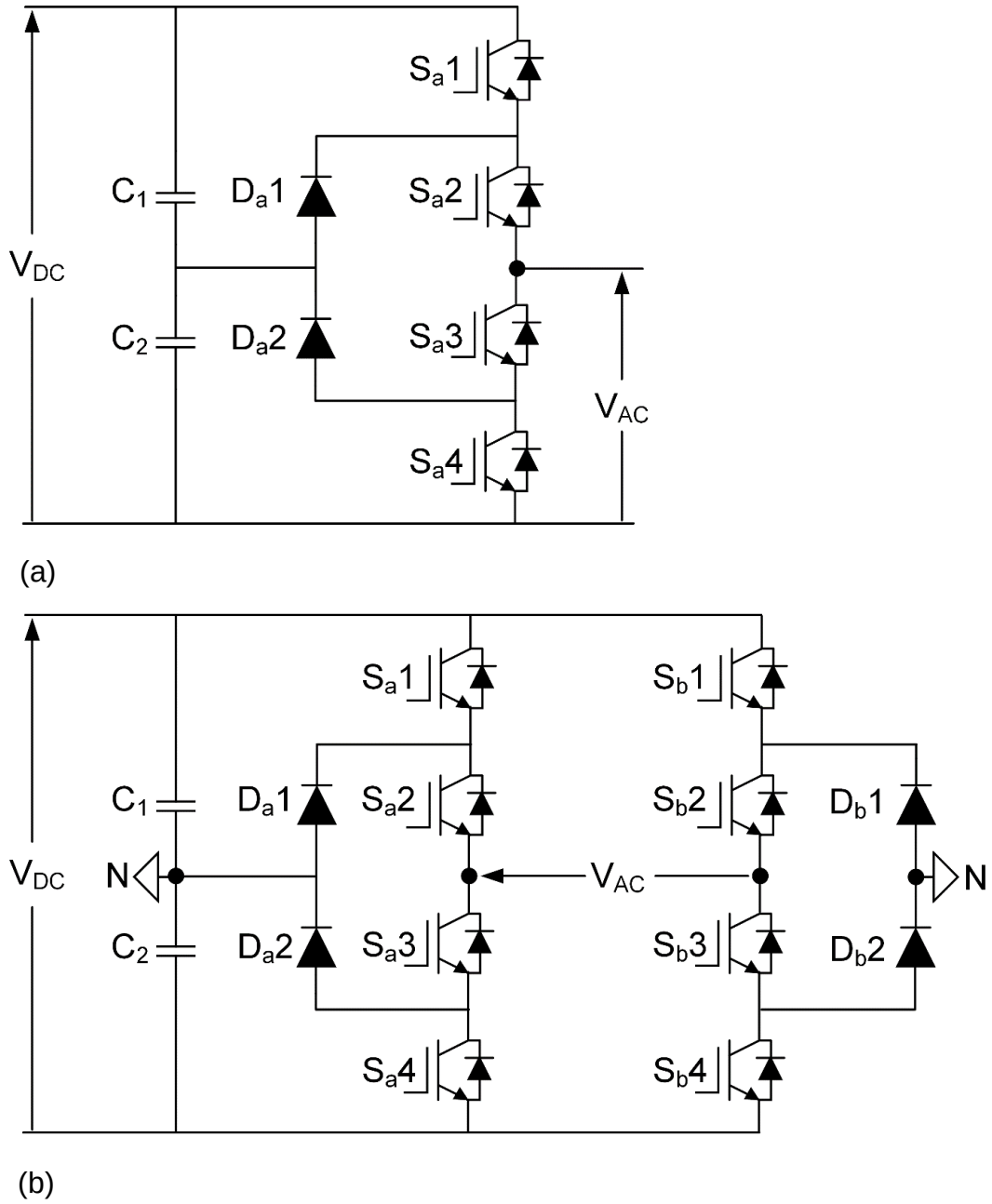

Figure 1.2: A three-level neutral point clamped (NPC) converter in: (a) half; and (b) H-bridge configuration.

Note that only the main current paths are shown albeit that in reality two other current paths exist which provide:

- current sharing through anti-parallel and clamping diodes; or
- current continuity through anti-parallel diodes when the main current path is suddenly interrupted due to a change in switching state.

The state 1001 is invalid as it results in an over voltage condition.

Table 1.1: Valid states for a three- level NPC converter

Leg A Switches				Leg B Switches				V_{AC}
S_a1	S_a2	S_a3	S_a4	S_b1	S_b2	S_b3	S_b4	
1	1	0	0	0	0	1	1	V_{DC}
1	1	0	0	0	1	1	0	$+V_{DC}/2$
0	1	1	0	0	0	1	1	$+V_{DC}/2$
1	1	0	0	1	1	0	0	0
0	1	1	0	0	1	1	0	0
0	0	1	1	0	0	1	1	0
0	1	1	0	1	1	0	0	$-V_{DC}/2$
0	0	1	1	0	1	1	0	$-V_{DC}/2$
0	0	1	1	1	1	0	0	$-V_{DC}$

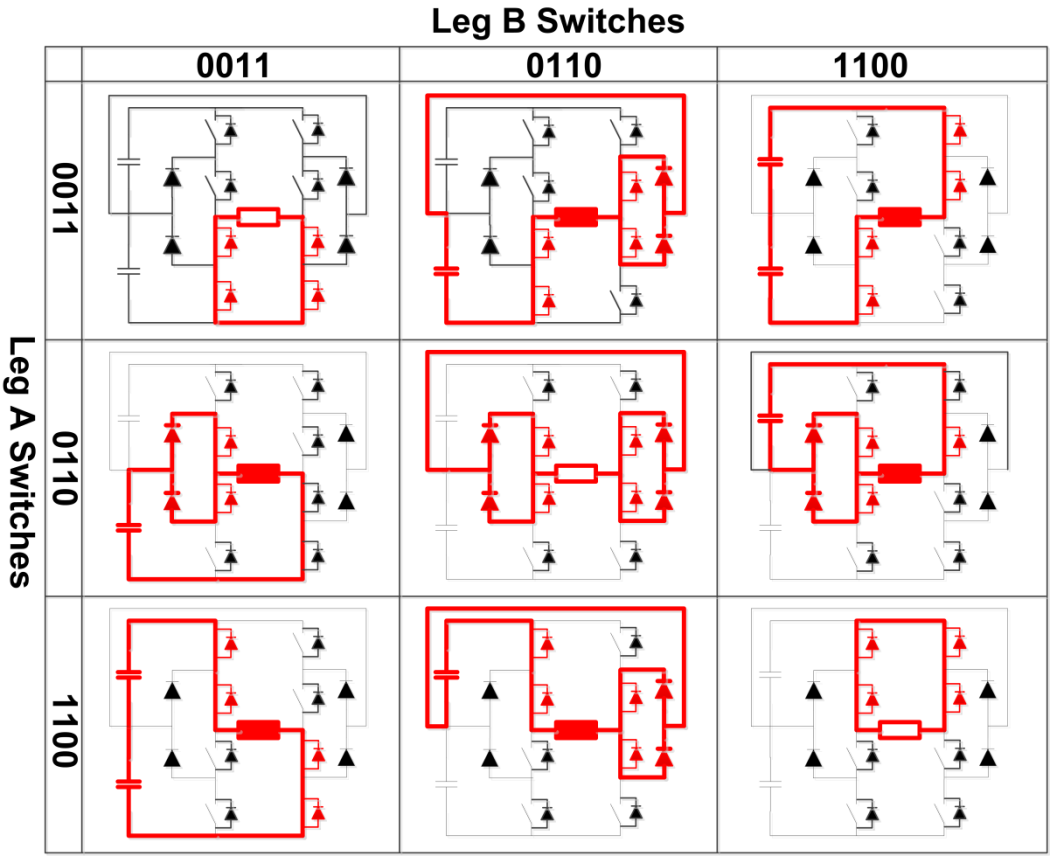

Figure 1.3: Possible current paths for a three-level NPC converter in H-bridge configuration. Current can flow in either direction.

Table 1.2 expresses the power devices requirement while extending the diode clamped converter.

Table 1.2: Power device requirements for NPC converter

Component	Quantity
Levels (Positive to Zero)	m
Switches and parallel diodes (per leg)	2(*m*-1) X 2
Clamp diodes	(*m*-1)(*m*-2)
Capacitors	*m*-1

There is a complexity involved in deriving the rating of the clamping diodes, since they, during certain switching instants, may experience higher than expected voltage levels thus any further extension would result in an expensive system.

A key challenge in controlling this converter is balancing the neutral-point capacitors. The absence of adequate redundant switching states makes this task difficult to achieve. Applications of this topology include a wide range of variable speed drives [35, 36]. It is currently applied in some medium power grid utility applications [37-41].

1.2.2 Cascaded H-Bridge (CHB) Converter

The cascaded H-Bridge (CHB) topology is based on the series connection of multiple electrically isolated standard H-bridge modules and is well reviewed [27, 31]. Each module is supplied by an isolated DC source (V_{DC}/n), where “n” represents the number of cascaded H-bridges per phase.

Figure 1.4 shows one leg of a three-level CHB converter topology. With each module capable of generating (V_{DC}/n, 0, -V_{DC}/n), the final AC output is a cascade of the separate AC outputs on each level and proper modulation control of the converter ensures an output with low total harmonic distortion value and harmonic content. In the CHB topology the absence of clamping devices (capacitors, diodes) reduces the number of power components. In practice the CHB topology is modular and less complex to control, however the requirement of several isolated DC supplies results in an expensive converter arrangement.

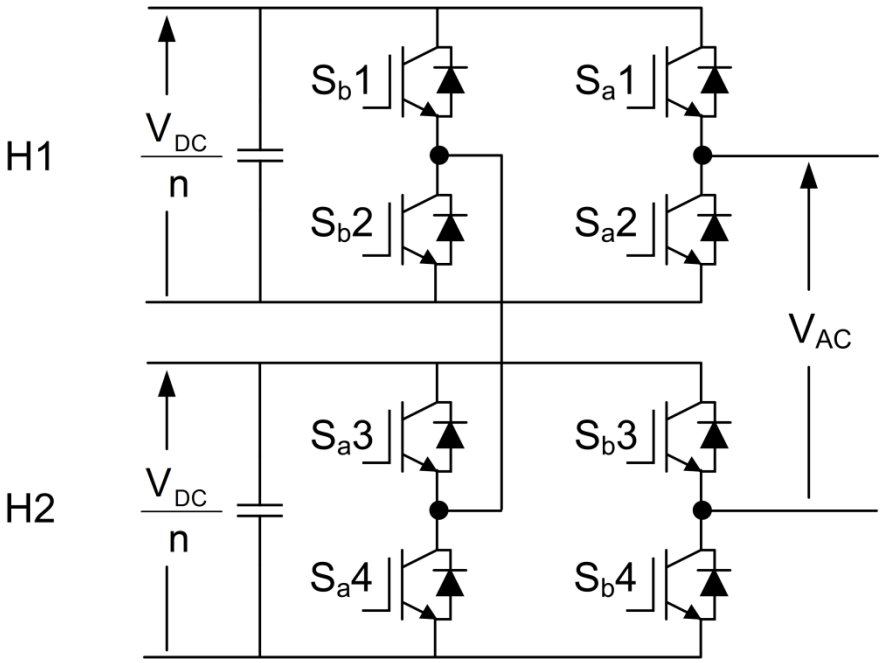

Figure 1.4: A single phase 3-level Cascaded H-bridge (CHB) topology.

The arrangement shown in Figure 1.4 is one phase of a 3-level CHB converter topology formed from a cascade connection of two H-bridge modules. The operating principle for each H-bridge is as follows (for instance consider the H-bridge formed from S_a1, S_a2, S_b1 and S_b2):

- The switching states for S_a1 and S_b1 are toggled in such manner that the voltage reflected across the H-bridge output is either 0, $+V_{DC}/n$, or $-V_{DC}/n$.
- The switching states for S_a2 and S_b2 are always operated in complementary manner to S_a1 and S_b1. This prevents creating a short circuit condition across the DC supply of the H-bridge.

The same principle is applicable to the second H-bridge (i.e. to S_a3, S_a4, S_b3, S_b4) but depending on the modulation technique implemented, the switching operation of H_2 may be phase- displaced and/or disposed to produce the resulting multilevel voltage waveform.

Table 1.3 illustrates the possible operating states for the 3-level CHB topology, while Figure 1.5 shows the current paths for one phase of a CHB inverter. There are four valid operating states (1001, 1010, 0101 and 0110) for a CHB inverter with two H-Bridges per phase, thus a total of 16 (i.e 2^4) switching states are available.

The converter can be configured to include extra levels by increasing the number of H-bridges as shown in Table 1.4.

Table 1.3: Valid switching states for a 3- level Cascaded H-bridge topology

S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{b1}	S_{b2}	S_{b3}	S_{b4}	V_{AC}
1	0	0	1	1	0	0	1	+ V_{DC}
1	0	0	1	1	0	1	0	+V_{DC}/2
1	0	0	1	0	1	0	1	+V_{DC}/2
1	0	1	0	1	0	0	1	+V_{DC}/2
0	1	0	1	1	0	0	1	+V_{DC}/2
1	0	0	1	0	1	1	0	0
1	0	1	0	1	0	1	0	0
1	0	1	0	0	1	0	1	0
0	1	0	1	1	0	1	0	0
0	1	0	1	0	1	0	1	0
0	1	1	0	1	0	0	1	0
0	1	1	0	0	1	0	1	-V_{DC}/2
0	1	1	0	0	1	0	1	-V_{DC}/2
1	0	1	0	0	1	1	0	-V_{DC}/2
0	1	0	1	0	1	1	0	-V_{DC}/2
0	1	1	0	0	1	1	0	- V_{DC}

Switching redundancies are present in this topology while producing the voltage levels: $V_{DC}/2$; 0; and $-V_{DC}/2$ as shown in Table 1.3. This makes it possible to control the converter such that the voltage stress is shared amongst the switches on each level.

Benefits of this system include the absence of excessive power components and a neutral point which reduces control complexities. However the presence of isolated power supplies per level limits this topology to only applications which do not rely on the presence of a single DC supply.

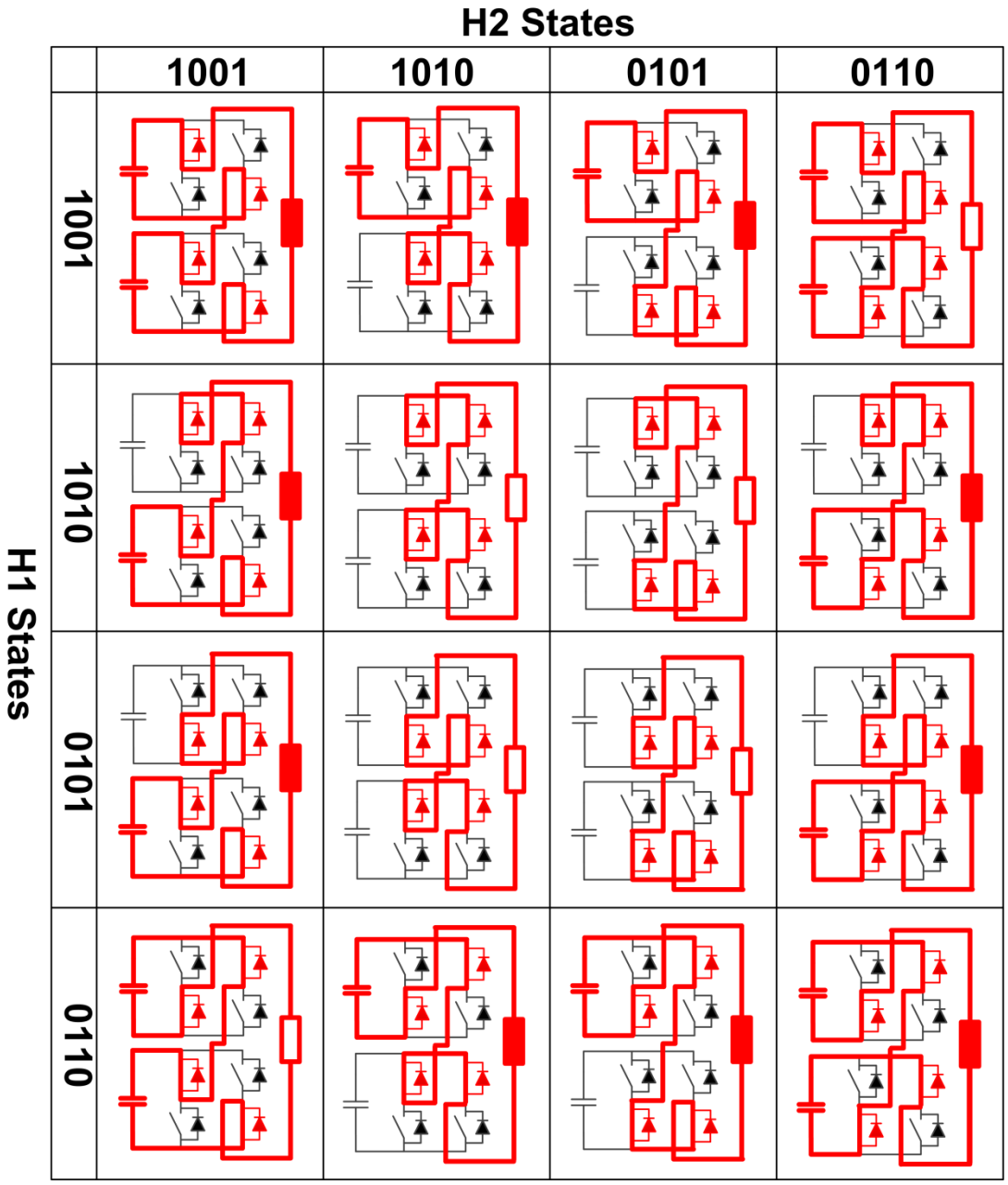

Figure 1.5: Current paths for a 3- level Cascaded H-bridge topology.

Table 1.4: Component requirements for a Cascaded H-bridge topology

Component per leg	Quantity
Levels (Positive to Zero)	m
Isolated Power Supplies	(*m*-1)
Switches and parallel diodes (per leg)	4(*m*-1)

Recommended applications for this topology include interfacing renewable energy sources to the grid, such as the voltage source converter in a grid-connected wind turbine application and implementation of FACTS devices, for instance in a distribution-level STATCOM device.

1.2.3 Flying Capacitor Clamped (FCC) Converter

The FCC was developed by Meynard and Foch [30]. capacitors set the intermediate voltage levels of this topology. Each voltage level in the converter AC output is formed as a result of the complementary switching action of a pair of switches. The result is a current path formed that bypasses or goes through the floating capacitor in that level.

The basic principle behind operating the FCC converter involves creating a path for current to flow either from the DC link or clamping capacitors to the load. As the clamping capacitors ideally have a known value (V_{DC}/n_C) where n_C is the number of cells, different voltage levels are achieved by altering the path of current flow, connecting or disconnecting the capacitors via the switches.

Figure 1.6 shows the circuit for a three-level flying capacitor converter: first in half bridge; then in full bridge configuration. The half-bridge FCC arrangement is capable of synthesising three AC voltage levels: 0; $V_{DC}/2$; and V_{DC} as this is a two-quadrant configuration. As the FCC H-bridge arrangement is a four-quadrant arrangement, five voltage levels can be produced: V_{DC}; $V_{DC}/2$; 0; $-V_{DC}/2$; and $-V_{DC}$.

Consider the half-bridge arrangement shown in Figure 1.6a, this arrangement is controlled as described below:

- The switching states for S_a1 and S_a2 are chosen in such manner that the current that flows to the V_{AC} terminals is supplied: completely by the DC source; by the capacitor C_a (thus discharging occurs); or a combination of both (thus charging occurs).
- **Valid operating states**:
    1. With the devices S_a1 and S_a2 both switched ON, the full DC voltage ($+V_{DC}$) is reflected across the AC output.
    2. With the device S_a1 switched OFF; and S_a2 ON, the voltage across the capacitor (ideally $V_{DC}/2$) reflects across the AC output. During this switching instant, the capacitor discharges.

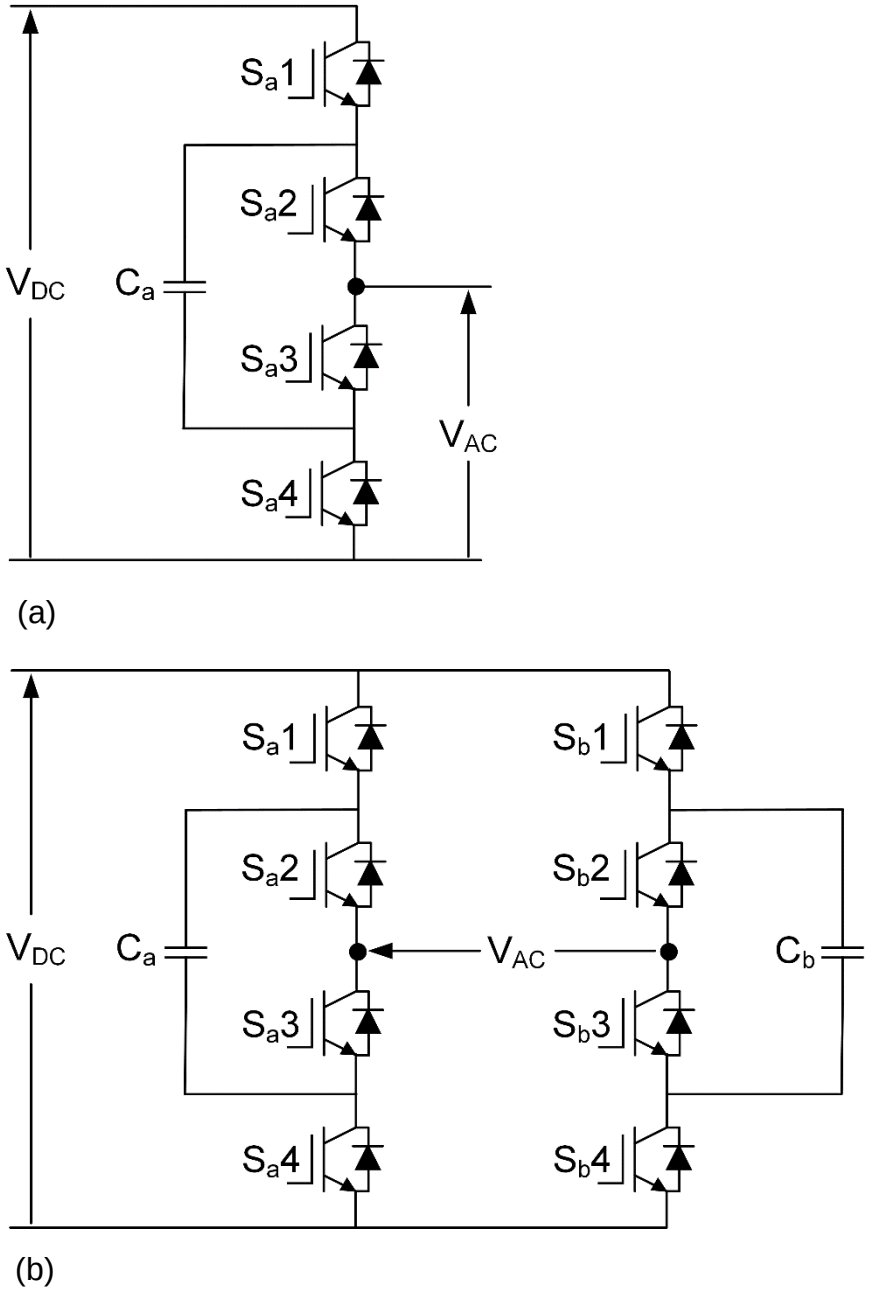

Figure 1.6: A three-level Flying Capacitor Clamped (FCC) converter in: (a) half; and (b) H-bridge configuration.

3. With the device S_a1 switched ON; and S_a2 OFF, the difference between V_{DC} and the capacitor voltage (i.e. ideally V_{DC} -V_{DC}/2) reflects across the AC output. During this switching instant, the capacitor charges.

4. With the devices S_a1 and S_a2 both switched OFF, the AC output is electrically tied to the negative V_{DC} terminal hence $V_{AC} = 0$.

- **Invalid operating states**:

Besides violation of the necessary complementary operation, there are no invalid switching states for the FCC topology.

- For complementary switching operation: S_a4 is always a binary opposite of S_a1; and S_a3 a binary opposite of S_a2. This prevents short-circuit conditions from occurring across the DC rail and the capacitor (C_a).

The principle described above is applicable in the H-bridge configuration shown in Figure 1.6b (i.e. to S_b1, S_b2, S_b3, S_b4). The two “half bridges” that make up the H-bridge arrangement are controlled to produce the resulting multilevel voltage AC waveform.

To realise the correct intermediate voltage levels at $V_{DC}/2$ (and $-V_{DC}/2$ in the H-bridge arrangement) the voltage level in each flying capacitor (C_a and C_b) must be maintained at half the DC link voltage (V_{DC}). Redundant switching states are available as shown in Table 1.5 with two main benefits:

- The switching stress can be shared among the devices in a bridge; and
- It is easier to balance the flying capacitors via an open loop rotation algorithm or closed loop selection algorithm during modulation.

Table 1.5 illustrates the possible operating states for the three-level FCC topology in H-bridge arrangement, while Figure 1.7 shows the current paths for the different switching states. As all four switching states (1100, 1010, 0101 and 0011) are valid for the two half-bridge networks (i.e.: S_a1, S_a2, S_a3, S_a4; and S_b1, S_b2, S_b3, S_b4), there are a total of 16 (i.e 2^4) operating states for the three-level FCC H-bridge.

In a practical system, switching the flying capacitors in and out of the circuit cause charging/discharging depending on the polarity of current. Thus voltages across the clamping capacitors (C_a and C_b) will vary during operation. It is then necessary to maintain their required voltage level otherwise voltage distortions will appear on the converter AC output waveform. The redundancies present in the switching states which are shown in Table 1.5 and the current paths established during switching

(Figure 1.7) make it possible for capacitor balancing to be achieved through proper switching state selection while the converter output voltage is synthesised.

Table 1.5: Valid switching states for three- level FCC in H-bridge arrangement.[3]

S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{b1}	S_{b2}	S_{b3}	S_{b4}	V_{AC}	C_a	C_b
1	1	0	0	0	0	1	1	+ V_{DC}	NC	
1	1	0	0	1	0	1	0	+V_{DC}/2	NC	↓
1	1	0	0	0	1	0	1	+V_{DC}/2	NC	↑
1	0	1	0	0	0	1	1	+V_{DC}/2	↑	NC
0	1	0	1	0	0	1	1	+V_{DC}/2	↓	NC
1	1	0	0	1	1	0	0	0	NC	
1	0	1	0	1	0	1	0	0	$C_a = C_b$	
1	0	1	0	0	1	0	1	0	$C_a = C_b$	
0	1	0	1	1	0	1	0	0	$C_a = C_b$	
0	1	0	1	0	1	0	1	0	$C_a = C_b$	
0	0	1	1	0	0	1	1	0	NC	
1	0	1	0	1	1	0	0	-V_{DC}/2	↓	NC
0	1	0	1	1	1	0	0	-V_{DC}/2	↑	NC
0	0	1	1	1	0	1	0	-V_{DC}/2	NC	↑
0	0	1	1	0	1	0	1	-V_{DC}/2	NC	↓
0	0	1	1	1	1	0	0	- V_{DC}	NC	

The presence of capacitors as the clamping devices makes the FCC topology expensive to implement, especially in high power applications such as transformer-less grid tied systems. In such applications, the clamping capacitors need to be rated at a certain percentage of the total DC bus voltage rating. This topology also has its benefits as the presence of capacitors makes it suitable for use as a compensation device in certain

[3] NC – Not connected; ↓ - Discharge; ↑ - Charge

“medium power” FACTS applications (around 11 kV, 1 kA) such as for active power filtering.

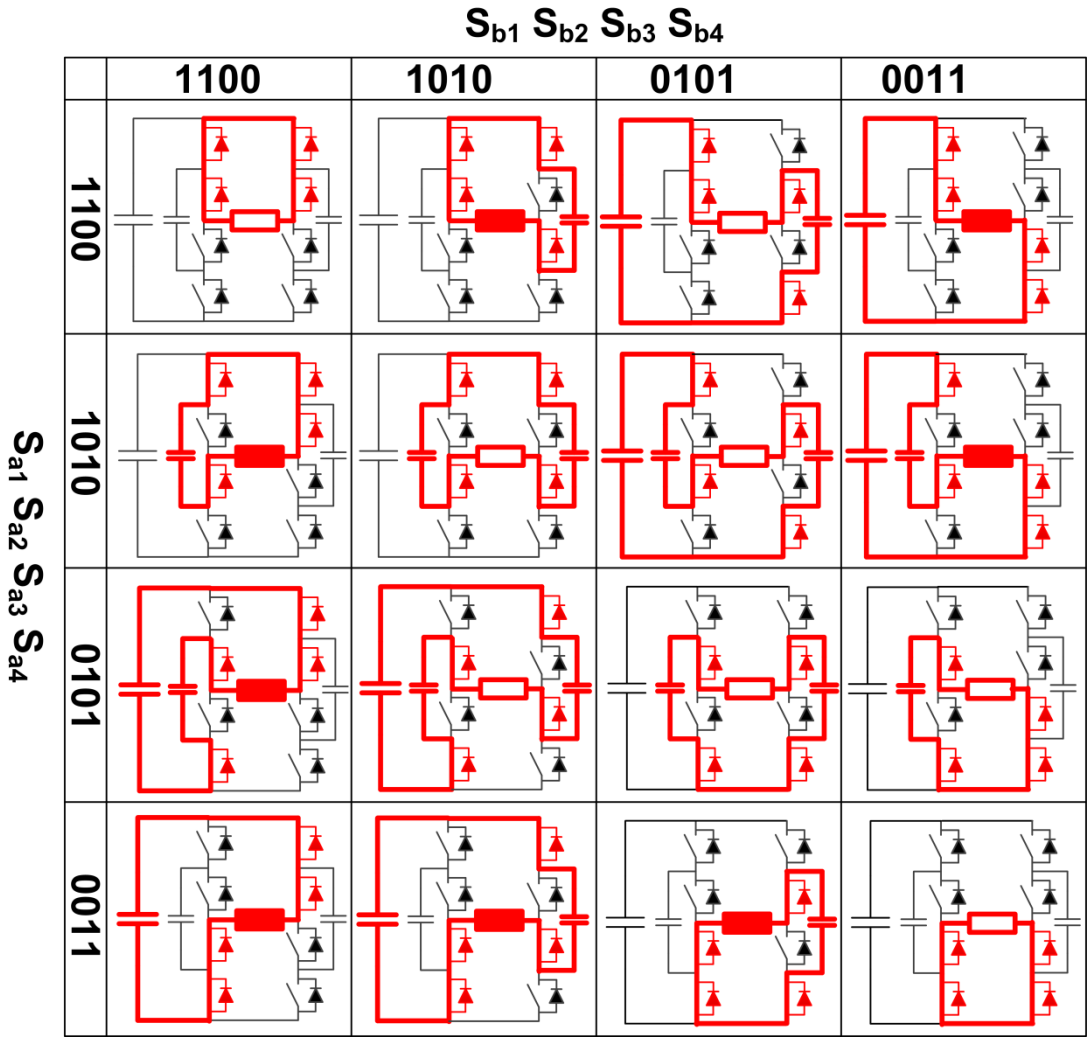

Figure 1.7: Current paths for a 3- level Flying Capacitor Clamped topology.

Extending the FCC topology to include extra levels involves increasing the number of clamping capacitors and complementary switch pairs as expressed in Table 1.6.

Table 1.6: Component requirements for a Flying capacitor clamped half-bridge topology

Component per leg	Number
Voltage Levels	m
Switches and parallel diodes	2(m-1)
DC Link Capacitors	m-1
Clamp capacitors	(m-3)/2

1.3 Component requirements for conventional multilevel topologies

The plot in Figure 1.8 shows the power component requirements for a three-phase configuration of the NPC, CHB and the FC. Note that all topology structures considered produce the same number of voltage levels. Five different groups of plots (DC bus, switches, capacitors, diodes and total) are shown, with each group containing three bar-plots to represent number of each component used for the three topologies as described in the legend (green-NPC, blue-FC, red-CHB).

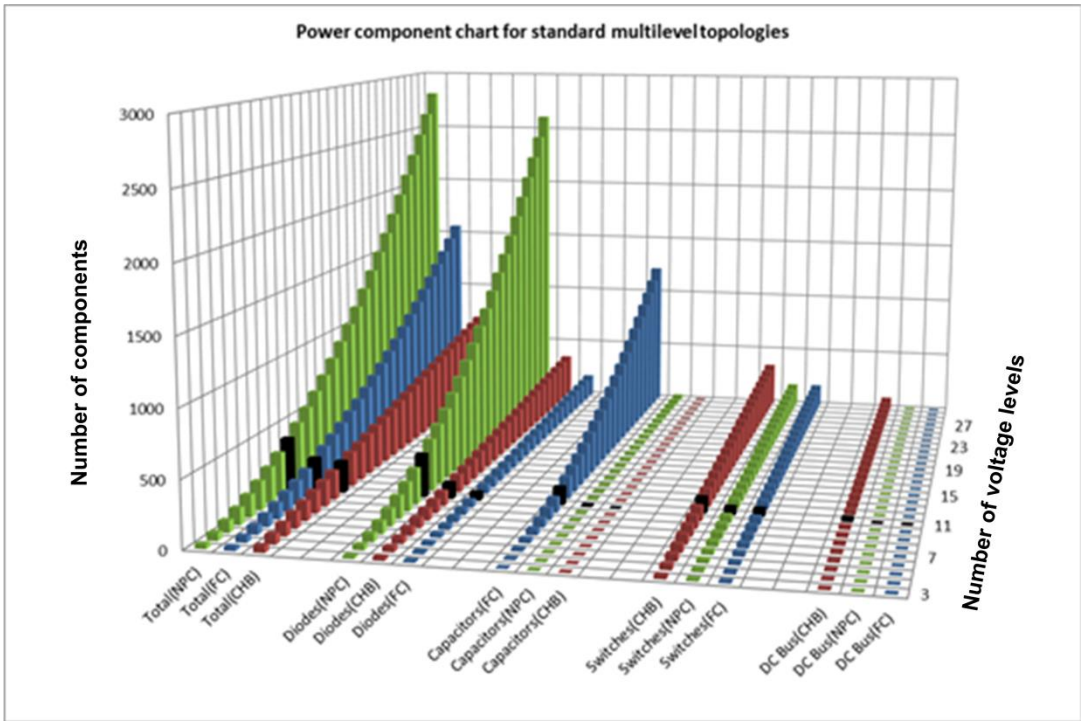

Figure 1.8: Component requirements for FC, NPC and CHB topologies.

The plots shown in Figure 1.8, were generated using the contents of Table 1.7. As well converter device requirements for an 11-level (0 to positive peak) output voltage are highlighted in black.

In Figure 1.8 is, all the capacitors and diodes (including anti-parallel diodes) are considered to have the same rating. It is assumed that these devices are series connected to achieve the required voltage level. This assumption is made to ensure consistency in the analysis provided. In a practical application, such devices can be distinctly selected to match required voltage levels.

Table 1.7: Power Component Requirements For Standard Multilevel Topologies[4]

	NPC	CHB	FC
DC Bus	1	$p(m-1)$	1
Capacitors	$p(m-1)$	0	$\frac{p}{2}(m-3)$
Diodes	$p[2(m-1)+(m-1)(m-2)]$	$4p(m-1)$	$2p(m-1)$
Switches	$2p(m-1)$	$4p(m-1)$	$2p(m-1)$

The total number of devices required increases relatively with the number of output levels as Figure 1.8 depicts. The NPC topology shows the highest rate of rise in number of power components required as the output level increases, while the CHB topology requires the least. This translates directly to the power losses expended on each topology.

1.4 Modular Multilevel Cascaded Converter – the new concept

It is clear from the above writing that conventional multilevel power converters rely on clamping devices (capacitors, diodes or galvanic isolated DC links) to stack up more voltage levels. Such a configuration is difficult to extend further rendering the conventional circuits practically impossible to

[4] m – Number of output voltage levels; p = Number of phase legs.

implement after certain voltage levels, especially if specifications for interconnecting distributed resources (IEEE 1547) are adhered to. Hence conventional multilevel topologies remain limited to medium level power applications. Recent development has led to the implementation of modular multilevel cascaded converters (MMCCs), a new breed of power electronic converter [42, 43]. In a MMCC topology, a power module is used as a basic building block and multiple modules are stacked to meet an application's power level requirements. In this context, "power module" refers to a basic circuit configuration comprising semiconductor switches which are switched in or out of circuit to provide access to an energy storage device. The topology has no known extension limitations and commercial systems exist with such configurations, however the control of this topology introduces several challenges. By nature, the topology presents several current paths, thus during operation, phenomena termed "circulating currents" may occur. The mitigation of this phenomenon is an active area of research in several institutes [21, 44-46]. Another key challenge involves maintaining balance in the energy storage element in each module as this is difficult in practice and requires sophisticated modulation algorithms, thus is also a subject of active research [47-49].

Hitherto the basic building blocks in an MMCC as well as emerging parallel and series variants, for example, the Alternate Arm Converter (AAC) [50], employed either half or full-bridge circuits with a capacitor. The review of the features of conventional multilevel converters, such as the diode clamped or flying capacitor types, suggests that it is possible to use any one or both of them as the building blocks for an MMCC, hence exploiting their advantages and increasing their range of applications to include higher power. Several investigations have produced significant publications, and industrial applications are in existence which confirm the versatility of the MMC for medium to ultra-high power applications [2, 51, 52], making the MMC circuit architecture of primary interest in this research work.

1.5 Research Aim, Objectives and Thesis Structure

The topic of this project stems from the desire to seek an alternative structure as the building block for an MMCC while exploiting attractive features offered by the conventional multilevel converters. The overall aim is to investigate the use of the 3-level flying-capacitor H-bridge circuit as the structure to form a new MMCC, the Modular Multi-level Flying Capacitor

Converter (MMFCC). This will involve developing suitable modulation schemes and applications, exploiting MMFCC advantages as redundancy of switching states is evaluated.

The specific objectives for achieving the research aim are defined as follows:

- Exploiting this topology and evaluating how the FCC module fits into the MMCC topology structure thereby forming the MMFCC.
- Considering the switching states, corresponding current paths and capacitor charging/discharging modes available,
- Operational analysis of this topology in single- and double star configurations, and single- and double delta configurations, for high-power applications.
- Investigating some adapted and novel multilevel modulation schemes for the MMFCC, in terms of harmonic performance and switching utilisation and losses.
- Designing and building an experimental prototype MMFCC demonstrator for practical validation of the converter model developed in Matlab-Simulink. Developing control techniques for this converter to function as a static synchronous compensator, and hence evaluating its feasibility in high power applications using the validated converter model,

The structure of the thesis is as follows:

Chapter 2:

In this chapter, the Modular Multilevel Converter concept is introduced and the family classification is presented as well as emerging topologies. The implementation of the 3-level FCC circuit at MMC module level, which results in the Modular Multilevel Flying Capacitor Converter (MMFCC), is then introduced and discussed.

Chapter 3:

Within this section, an assessment exercise performed, to qualify five basic candidate sub-module concepts during the research work, is discussed. Criteria used to assess each sub-module concept were footprint, cost, redundancy, efficiency and performance. This helps to establish a rationale behind the choice of the 3-level FC H-bridge sub-module concept for extension and further evaluation during the rest of the research.

Chapter 4:

Modulation control techniques are introduced in Chapter 4 to handle the sophisticated co-ordination required by a single-star MMFCC topology. Also within this section, the newly-developed overlapping multilevel hexagon space vector modulation (OMHSVM) scheme is described.

Simulation results are presented to validate the presented modulation concepts.

Chapter 5:

The experimental rig developed during the course of the research is described in Chapter 6. Following detailed discussion of the power circuit, the different subsystems (DSP, FPGA cards) which make up the control hardware platform are discussed in detail. Experimental waveforms obtained are used to validate the converter performance simulated in Chapter 4.

Chapter 6:

A summary of the findings revealed during the research work is provided in Chapter 6, and recommendations to guide future advancement of this work are also provided.

Chapter 2

Modular Multilevel Converters

The cascaded H-bridge topology is formed by chaining a set of H-bridges and is therefore inherently “modular” -bridges. Its first industrial implementation by Robicon Corporation [53], was considered an impressive advance in the field. The system involved a total cascade of nine H-bridges (3 per phase) in the converter phase arms; however a complex star-delta-star phase shifting transformer arrangement was required to supply the isolated DC requirements of each H-bridge. The converter configuration offered attractive benefits yet was costly to extend for high power applications. Nonetheless this limitation experienced by Robicon Corporation while implementing the CHB topology fostered research interest in realising a more industry-friendly high power converter.

In response Leniscar and Marquardt presented the Modular Multi-Level Converter (M2LC) [54, 55] initially introduced in [56]. The proposal detailed a high power converter with significant technical and cost benefits. One of these was its easy scalability achieved by simply cascading additional modules in series within each converter phase arm.

This chapter presents detailed discussions of the developments in the area of modular multilevel converters. A generalized family classification of topologies is first discussed, based on its constituents, followed by some emerging architectures. Afterwards, a different module concept, the 3-level FCC module is introduced as a replacement for the H-bridge cell and a quadrant system is described to show the control degrees of freedom available to the 3-level FCC multilevel module. A hybrid version of the 3-level FCC module, which has been termed within this chapter as the FC-H module, is also described in brief to cover ideal modulation waveforms and temporary circuits formed during its different switching instants.

The terms “cell” and “module” are used interchangeably and refer to the basic building block i.e. H-bridge, half-bridge or FCC circuit, for each MMC topology. The author is aware that the term “sub-module” is also used in other literature to express the same idea.

2.1 Modular Multilevel Converter (MMC) Configurations

In an MMC topology, each converter phase comprises at least an “arm” built up from a stack of sub-modules. An inductor is normally inserted either at the top or bottom of the stack and this depends on physical installation limits such as the footprint available on site. This “buffer” inductor serves the purpose of limiting the in-rush current to the converter arm as well as limiting di/dt in the converter’s current waveforms during the different switching actions.

2.1.1 Sub-Modules Using Half-Bridge Cells [54]

A half-bridge cell comprises two switching devices, two diodes and a DC energy storage element (i.e. capacitor, super-capacitor or battery) as illustrated in Figure 2.1(a). Each cell is capable of producing a two state output voltage: 0 or $+V_C$, where V_C is the voltage of the associated DC source (see Table 2.1). Thus each cell acts as a controllable unipolar voltage source. The current flow through each cell can be bidirectional, hence it gives two quadrant operation. For high voltage applications, multiples of such cells are used as sub-modules and the terminals of these are cascaded to form one phase arm with the inductor mentioned above connected at one end as shown in Figure 2.1(b) .

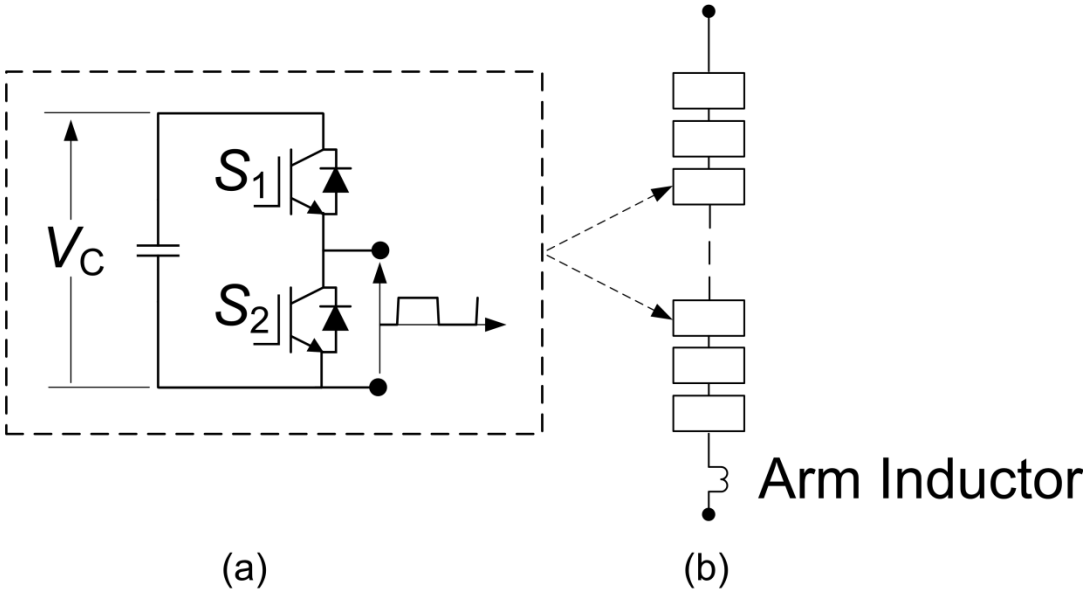

Figure 2.1: (a) Half-Bridge Cells and (b) one converter phase arm.

Table 2.1: Valid Half-Bridge Module Switching States.

V_O - cell output voltage; I_O – cell current direction; and Vc - capacitor voltage (↓ = Discharging, ↑ = Charging, NC = No Change)

S_1	S_2	V_O	V_C	
			$+I_O$	$-I_O$
1	0	+Vc	↑	↓
0	1	-Vc	↓	↑

The main benefit of realising the sub-modules by half-bridge cells is their simplicity in comparison to using other topologies. However a limitation is the inability to suppress, by converter action, fault currents arising from DC-side short circuits. This is because each switching device, either MOSFET or IGBT, is equipped with an integral inverse parallel diode, forming an uncontrollable rectifier. Though the current technology has made DC-bus faults rare and AC circuit breaker tripping is tolerable, such defect is still a concern to be addressed.

2.1.2 Sub-Modules Using H-Bridge Cells

The use of a H-bridge cell as sub-module has also been investigated [3]. With four switch-diode combinations and one energy storage element of the same type as its half-bridge counterpart above, this offers three-state output voltage as listed in Table 2.2 and bidirectional current flow, hence giving four-quadrant operation as shown in Figure 2.2(a).

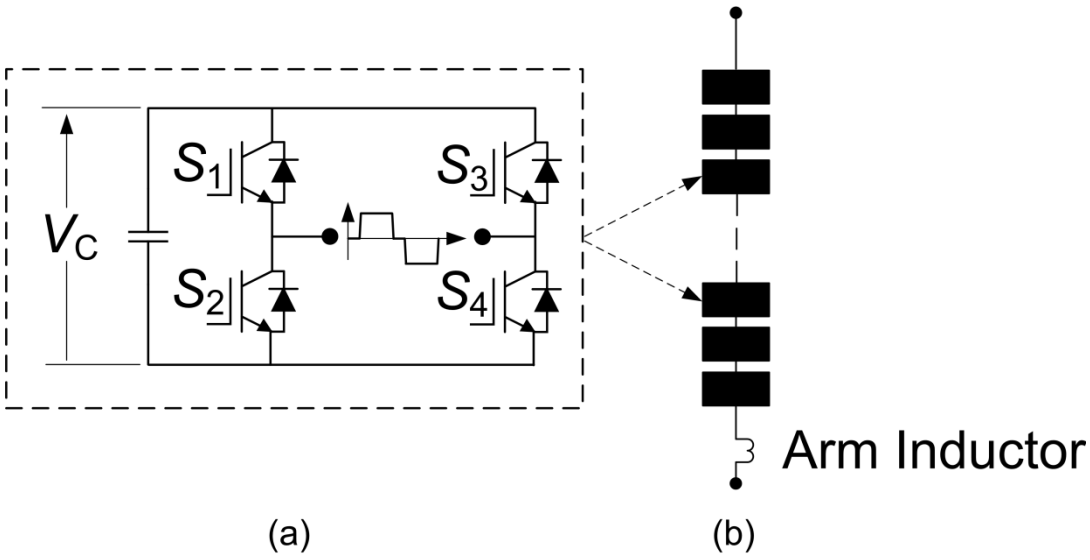

Figure 2.2: (a) H-Bridge Cells and (b) one converter phase arm.

The phase arm is realised by chain connection of multiple cells as shown in Figure 2.2(b). Clearly, compared with the half-bridge cells, using this module within the topology doubles the number of semiconductor devices. However it is capable of suppressing DC faults by converter action.

Table 2.2: Valid H-bridge Cell Switching States.

V_O - cell output voltage; I_O – cell current direction; and Vc - capacitor voltage (↓ = Discharging, ↑ = Charging, NC = No Change)

S_1	S_2	S_3	S_4	V_O	V_C	
					$+I_O$	$-I_O$
1	0	0	1	+Vc	↑	↓
0	1	1	0	-Vc	↓	↑
0	1	0	1	0	NC	NC
1	0	1	0	0	NC	NC

Notes for Table: The convention for the converter current is, +ve current is one that flows into the converter; and negative current flows out of the converter.

2.1.3 Classification of Modular Multilevel Converters

Since its inception, various names have been given to the modular multilevel topology, such as cascade multilevel converter, modular multilevel converter, M2LC, M2C and chain-link converter. To establish consistency, both in naming and understanding, a review and classification of this family of converters was conducted in 2010 [43]. In this review, the name “Modular Multilevel Cascaded Converters” (MMCC) was adopted for this family of converters. The following categories are specified within:

- Single Star Bridge Cells (MMCC-SSBC)
- Single Delta Bridge Cells (MMCC-SDBC)
- Double Star Chopper Cells (MMCC-DSCC)
- Double Star Bridge Cells (MMCC-DSBC)

Note that each of the converters in this category presents certain characteristics that either increase or reduce suitability when applied in one application or the other. To ensure consistency with existing literature, the term “arm” is used to refer to a cascade of modules that act together to synthesise the same portion of an output (AC or DC) in an MMC. The author

is aware the other nomenclature such as converter “limb” or “phase limb” may be used in other literature. In the topologies described it is also assumed that the storage element used is a capacitor.

In this thesis, the format adopted for discussing the MMCC family involves a further categorisation into the following:

- No DC link (Single- Bridge Cells: SSBC, SDBC)
- Common DC link (Double Star- Cells: DSCC, DSBC)

The “No DC link” category includes the MMCC-SSBC and MMCC-SDBC circuits, while the Common DC link category includes the MMCC-DSCC and MMCC-DSBC circuits.

Although the MMCC-SSBC and MMCC-DSBC are more popular circuits, especially for industrial implementation, all the categories are discussed in this section including the double delta circuit which was not reviewed in [43].

2.2.4 Single- Bridge Cells

This type of MMCC is typically built from H-bridge modules. Several such modules are series-connected to form each converter arm. It is not common to implement half-bridge modules in the single-star arrangement due to the limitation presented by the inability to reverse voltage polarity. Moreover fewer redundancies are available for module capacitor energy exchange.

This topology can support applications which do not require a DC link. Such requirement is common for certain applications: Flexible AC Transmission systems (FACTS) devices such as Static Compensator (STATCOM); Battery Energy Storage Systems (BESS) [22, 57-60]; and grid interface converters for integrating distributed renewable energy sources [61].

Single- Star Bridge Cells (MMCC-SSBC)

The configuration of a three-phase MMCC in single-star arrangement and built from H-bridge cells is illustrated in Figure 2.3. Each converter arm comprises a number of H-bridge modules series connected to form two arm terminals: an AC and a DC terminal. The AC terminal for each converter arm (U, V, W) is connected to one phase of the AC line (A, B, C) typically via a transformer and/or a line reactor of known value: Lc_A, Lc_B, Lc_C. The DC terminals for each converter arm are connected to a common node, that forms the converter’s neutral point which may be grounded or left “floating” depending on application requirements like transformer set-up.

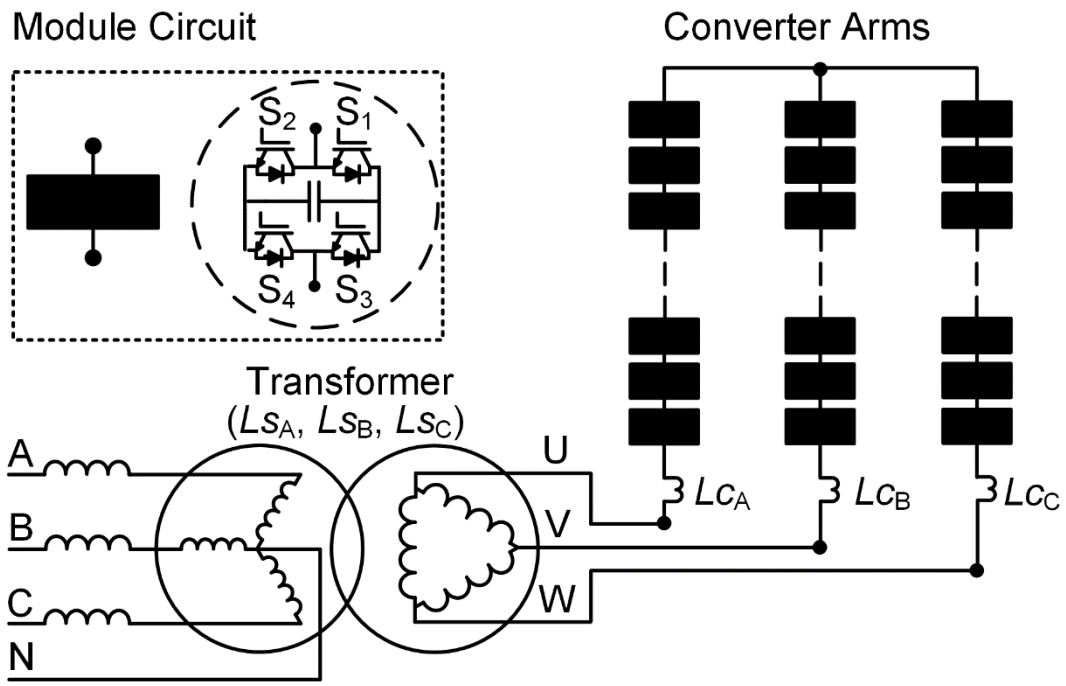

Figure 2.3: MMCC Single Star topology using H-bridge modules.

The connection between the converter and the AC line i.e. transformer arrangement is chosen based on application requirements and typically specified by the customer. Some points considered while making this choice are:

- Type of AC grid (three- or four- wire system).
- Level of isolation required between the converter and AC grid.
- Ratings required for the converter's AC current and terminal voltages in relation to the grid current and voltage.
- Build, physical size and means of transporting the transformer.

Figure 2.3 shows a star-delta type transformer arrangement and the star-neutral point is grounded at the grid side. This arrangement is suitable when a four-wire AC system is present and sufficient grid-converter isolation is required. The converter's terminal voltages are supplied by the delta side of the transformer and the neutral point is left "floating". This arrangement reduces certain project costs. For instance there is no longer a need for grounding transformers and disconnector switches at the converter side.

Other common AC connection (transformer) arrangements include:

- Star-Delta (with floating star);
- Star-Star (with grounded or floating star); and
- Delta-Star (with grounded or floating star).

Assuming that the voltage level (V_C) is maintained across each module capacitor, then each converter arm will synthesise an AC waveform with up to ($2n.V_C + 1$) voltage levels (where n is the number of H-bridge modules in the converter arm). The different switching states available to a H-bridge module and corresponding module capacitor voltage are as shown in Table 2.2.

Consider connecting this MMCC-SSBC to a balanced three-phase source, each phase current flows into one phase arm through an equivalent series impedance presented by the transformer and AC line (Ls_A, Ls_B, Ls_C), the converter arm inductor (Lc_A, Lc_B, Lc_C) and the chained modules. The energy storage components are either charged or discharged depending on the direction of phase current and individual module switching states. Clearly there is only one current path in each phase arm. Hence circulating currents do not exist in this topology. Based on this functionality, the MMCC-SSBC topology will only interact with positive-sequence components in a power system, making it attractive only for smart grid applications with stiff and symmetrical AC supplies such as distribution-side STATCOM or BESS applications.

Single- Delta Bridge Cells

The configuration of a single delta bridge cell-based MMCC is as illustrated in Figure 2.4. Each converter arm (A-B; B-C; and C-A) comprises “n” series-connected modules and three such arms are connected in delta form. There is neither a common neutral point nor common DC link hence the transformer arrangement must either be in floating-star or delta configuration at the converter side.

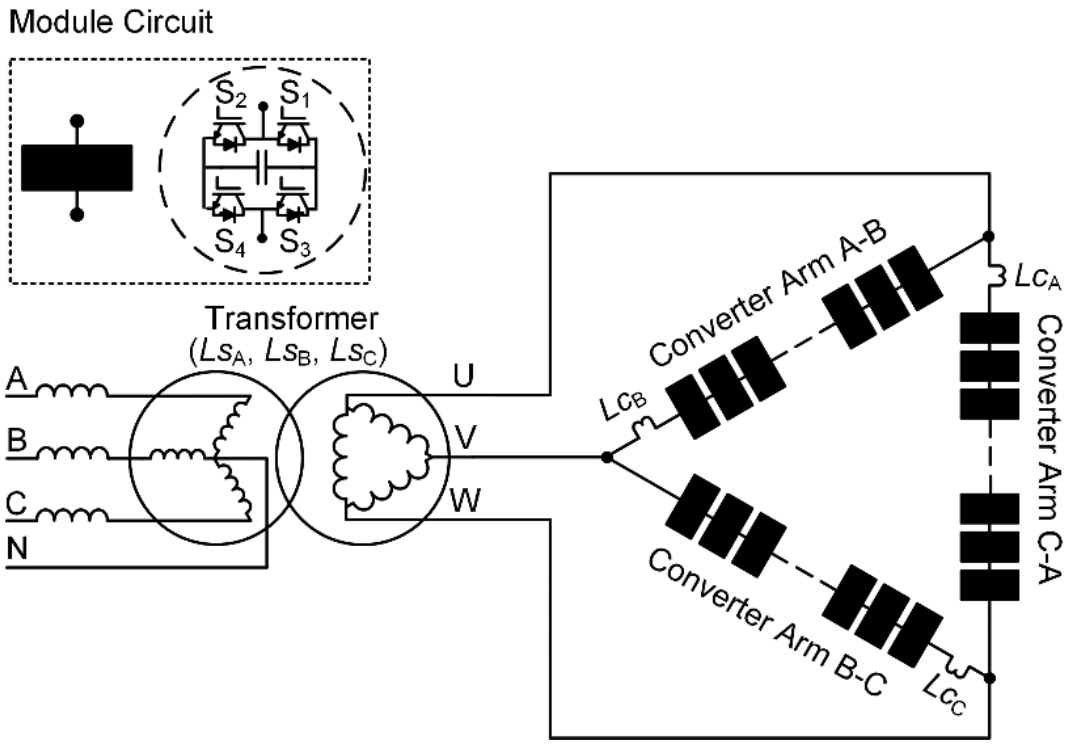

Figure 2.4: MMCC Single Delta topology using H-bridge modules.

The switching states in Table 2.2 still govern the output voltages for each H-bridge cell but the delta configuration introduces circulating phase currents, making it possible for an inverter with this topology to interact with both positive- and negative-sequence symmetrical components.

Consider an AC current flowing from Phase-A through at the converter-side transformer terminal “U” shown in Figure 2.4. An ideal path for this current would be to split at the converter connection point between converter arms: A-B; and C-A. The portion of current that flows through both converter arms is determined by the voltage across each arm at that instant. Multiple return paths are available via terminals “V” and/or “W”, again determined by the voltage across the converter arm B-C. These extra paths allow for the current to “circulate” within the converter at each instant. A case for this is presented in [46], where an investigative study is presented for a 5 kVA PWM controlled MMCC in single delta bridge cell configuration. This was deployed with the aim of realising negative-sequence reactive power control in a STATCOM application. As a result of this functionality, the MMCC-SDBC is attractive for smart grid power applications that may involve unsymmetrical AC systems. It is also suitable for Battery Energy Storage System (BESS) applications as it also allows interaction active power components in a grid.

Ratings for Single- Bridge Arrangements

When rating the arms in a single star (Figure 2.3) or single-delta (Figure 2.4) structure, it is important to note that voltage rating (thus number of modules) and current rating (thus current rating for module switches) for the converter arms are affected by the secondary-side transformer arrangement. This is qualified in Table 2.3.

Table 2.3: Ratings for Single- Star and Delta topologies.

	Single Star Converter	Single Delta Converter
Grounded Star	$V_{rating} = \frac{V_{\text{L-L}}}{\sqrt{3}}; I_{rating} = I_{\text{PH}}$	Not Applicable
Floating Star	$V_{rating} = \frac{V_{\text{L-L}}}{\sqrt{3}}; I_{rating} = I_{\text{PH}}$	$V_{rating} = V_{\text{L-L}}; I_{rating} = \frac{I_{\text{PH}}}{\sqrt{3}}$
Delta	$V_{rating} = \frac{V_{\text{L-L}}}{2\sqrt{3}}; I_{rating} = I_{\text{PH}}\sqrt{3}$	$V_{rating} = \frac{V_{\text{L-L}}}{\sqrt{3}}; I_{rating} = I_{\text{PH}}$

where

$V_{\text{L-L}}$ is the line to line voltage value at converter side.

I_{PH} is the phase current at converter side

According to Table 2.3, the voltage rating for an MMCC-SDBC topology is "√3" times more than that of an equivalent MMCC-SSBC topology when a floating star converter-side transformer arrangement is used and 2 times more when a delta converter-side transformer arrangement is used.

Also, the current rating for an MMCC-SDBC topology is "√3" less than that of an equivalent MMCC-SSBC topology regardless of the transformer arrangement. This means that switches (IGBT's) of a lower current rating (which are cheaper) may be used within the H-bridge modules but more H-bridge modules are required in series.

Main control objectives for a MMCC circuit application implementing single-bridge modules/cells include ensuring equal and constant voltages module capacitors as well as the control of symmetrical positive (single-star) and/or negative (single-delta) sequence components on the AC terminals.

2.1.4 Double- Bridge Arrangements

This arrangement of MMCC allows the use of half- or H-bridge modules and the choice of either depends primarily on the type of application and sort of functionality provided by the converter. Several such modules are series-

connected to form each converter arm and the arrangement is an extension of the single- star or delta topology such that a double star or double delta circuit may be realised. The double star bridge cell (MMCC-DSBC) supports applications that require a common DC link and has become popular over the past half-decade as the enabling technology for HVDC applications.

The arrangement realised by extending into a double delta bridge cell topology (MMCC-DDBC) has neither been reviewed in any academic publications nor received industrial interest. This is possibly because no extra functionality has been identified by using such an arrangement.

The MMCC-DSBC and MMCC-DDBC topology structures are introduced in the following text. For the case of the MMCC-DSBC topology some basic analysis is provided to highlight some of the research interest and focus placed on this topology at the moment. Typical converter ratings are also provided.

Double- Star Bridge Cells

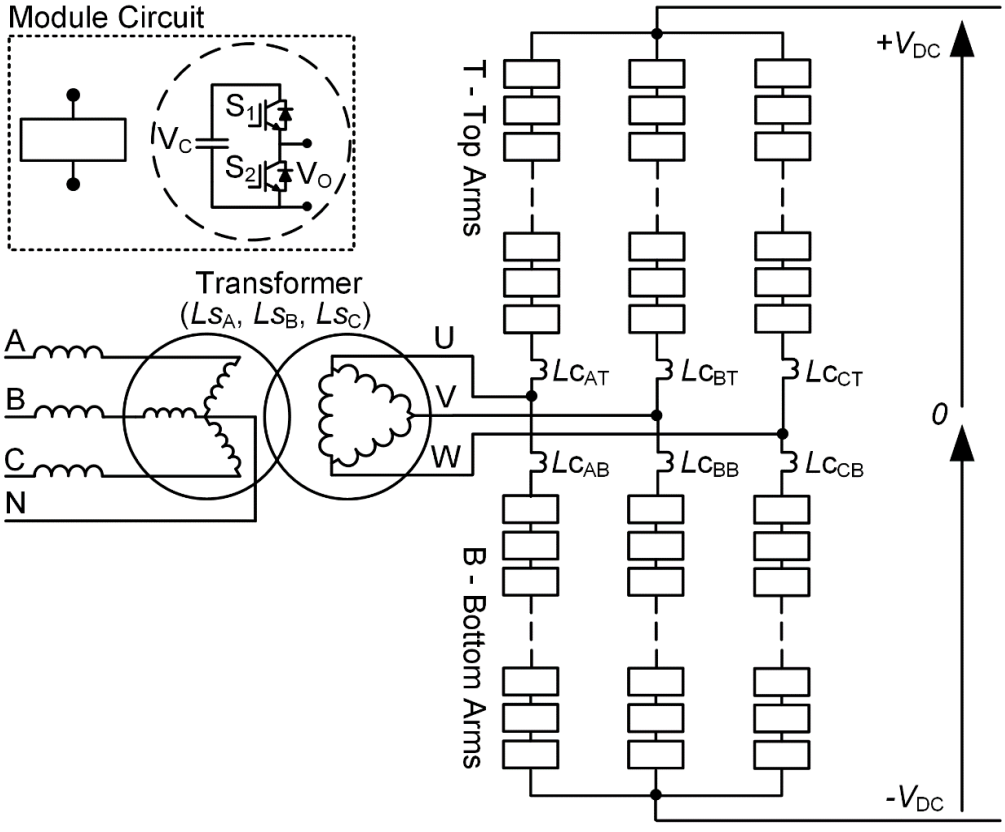

Figure 2.5: MMCC Double Star Bridge Cell topology using half-bridge modules.

Figure 2.5 shows the double star topology of a MMCC. A half-bridge arrangement is shown as the module circuit and it is uncommon for H-bridge modules to be applied in this topology. This is because each converter arm is required to operate in only two quadrants (i.e. bipolar current and unipolar voltage) hence the half-bridge module is sufficient.

Unlike the single- star and delta arrangements the double star topology is built from six converter arms connected as pairs to form each converter phase i.e. as three top arms and three bottom arms. Essentially the topology comprises two single-star circuits with phase-parallel connected AC terminals. In each phase the top and the bottom arms are connected through converter arm reactors Lc_{AT}, Lc_{AB}, Lc_{BT}, Lc_{BB}, Lc_{CT}, Lc_{CB} to form common AC phase terminals (U, V, W). The three top arms are connected to form a common positive DC terminal ($+V_{DC}$) while the three bottom arms form the negative DC terminal ($-V_{DC}$).

The “phase-parallel” configuration of the top and bottom arms result in several current paths available within this topology thus allowing the “circulating current” phenomenon to occur.

The half-bridge module circuit shown in Figure 2.5 comprises a capacitor and two semiconductor power switches (S_1; and S_2). These are typically IGBTs and can be controlled to synthesise two output voltage levels at V_O. Assuming the voltage level (V_C) is maintained across each module, then each converter arm will synthesise an AC waveform with up to ($n.V_C$ + 1) voltage levels (where n is the number of half-bridge modules in the converter arm). The different operating states available to a half-bridge module are outlined in Table 2.1. The module output voltage (V_O) for each state and resulting consequence to the module capacitor voltage (V_C) (i.e. charging or discharging) is also specified.

Similar derivation may be applied to the single and double star circuits to determine power demand levels. However a more sophisticated current control strategy is required for the double star circuit due to the several control variables namely: three AC currents; six arm currents; and DC current. More so, the circulating currents must be controlled. An equivalent circuit for the converter is shown in Appendix B.1 outlining several composite and complex closed circuits formed by the double star topology during operation. This is used to establish certain expressions that describe the circulating currents within the double star topology.

Circulating current is a dominant issue in the control of the double star MMCC circuit and is a subject of research [21, 45]. It is often considered during design of the control of the topology and mostly at the inner loop current controller [48, 49, 62].

In Chapter 3 the different tiers of control required for proper management of a Modular Multilevel converter are introduced and those essential for managing the circulating currents within the converter are highlighted.

The MMCC-DSBC topology has attracted industrial interest due to its ease of extension and application versatility. Many power electronics industries have produced either a prototype or commercial-ready version of this topology especially for application to HVDC schemes.

Double- Delta Bridge Cells

Following through from the classification in [43], it is then possible to implement a double delta bridge or chopper cell (DDBC or DDCC). However this circuit has neither been reviewed academically nor established practically as the presence of a double delta circuit, even though more expensive, presents no significant benefits. From an application perspective, the Double Delta circuit is also limited as it does not provide a common DC link.

However, the MMCC-DDBC topology presents the possibility of separately controlling each delta converter and the circulating current through the delta connected arms and facilitates active power exchange between the cells capacitors in each arm.

Figure 2.6 presents a configuration with a double delta circuit connected to a 3-phase AC supply. Such a circuit will control both positive and negative sequence symmetrical components and in practice it can be used as an inverter for reactive power compensation as well as a harmonic filter.

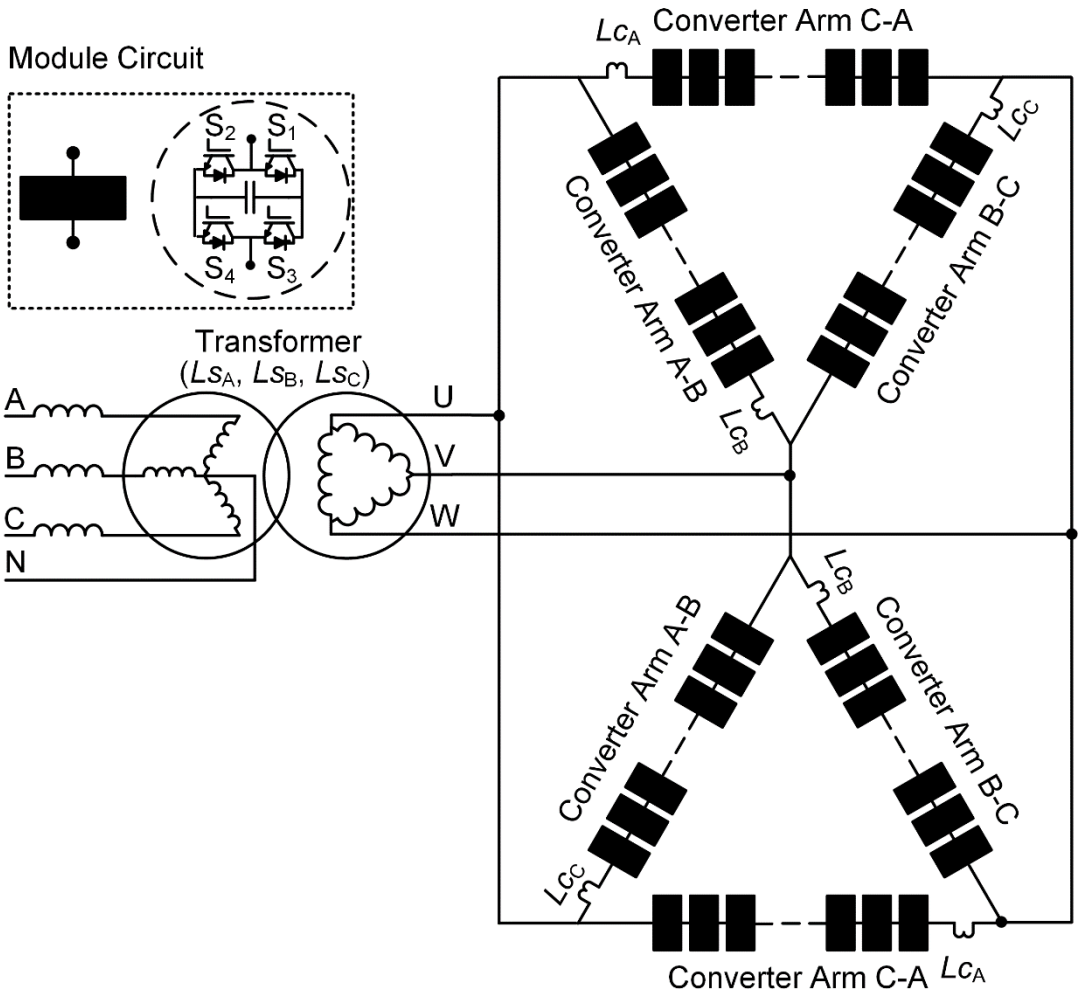

Figure 2.6: MMCC Double-Delta topology using H-bridge modules.

As shown in Figure 2.6, a double-delta topology is built up using H-bridge cells and comprises two single-delta converters (top and bottom delta converters) hence it presents six phase arms comprising of “n” number of bridge cells in each arm. The AC supply terminals are tapped from the connection points on each phase in the delta configuration.

There are no extra benefits from the complexity that is such an extension, except possibly for increasing current capacity which may be achieved via less complicated means (e.g. increasing module switch current rating, choice of converter transformer, etc.). Further analysis is not conducted for this topology.

2.1.4.1 Voltage and Current Ratings for the Double- Star Arrangement

It is important to know the voltage and current rating for the converter arms in a double- star (Figure 2.5) structure as these ratings help in choosing the number of modules as well as the current rating of module switches. The

effect of converter transformer arrangement is already qualified in Table 2.3 thus Table 2.4 focuses on generalised converter arm ratings for an MMCC-DSBC topology.

Table 2.4: *I – V* Ratings for the Double Star Bridge Cell topology.

Arm Rating	Voltage (*V*)	Current (*A*)	
		Inverter	Rectifier
Operating	$V_{ARM\_TOP} = V_{DC} - V_{AC}$ $V_{ARM\_BOTTOM} = V_{AC} - V_{DC}$	$I_{Top} = \frac{I_{DC}}{3} + \frac{I_{AC}}{2}$ $I_{Bottom} = \frac{I_{DC}}{3} - \frac{I_{AC}}{2}$	$I_{Top} = -\frac{I_{DC}}{3} - \frac{I_{AC}}{2}$ $I_{Bottom} = -\frac{I_{DC}}{3} + \frac{I_{AC}}{2}$
Peak	$V_{ARM\_Peak} = \lvert V_{DC} + V_{AC} \rvert$	$I_{ARM\_Peak} = \left\lvert \frac{I_{DC}}{3} + \frac{I_{AC\_Peak}}{2} \right\rvert$	

where

V_{DC} is a DC voltage portion, the total DC rail voltage is $\pm V_{DC}$ i.e. $2V_{DC}$.

V_{AC} is the AC voltage applied to the converter (this is either a phase or line-line voltage depending on the transformer arrangement chosen).

V_{ARM_TOP} is the voltage applied across the top converter arm during operation. See Figure 2.7.

V_{ARM_BOTTOM} is the voltage applied across the bottom converter arm during operation.

V_{ARM_Peak} is the maximum voltage value of the converter arm (top or bottom). See Figure 2.7.

I_{DC} is a DC current absorbed or supplied by an inverter or rectifier.

I_{AC} is an AC current absorbed or supplied by an inverter or rectifier.

I_{Top} is a combination of AC and DC currents that flow through the top converter arm. See Figure 2.7.

I_{Bottom} is a combination of AC and DC currents that flow through the bottom converter arm.

I_{ARM_Peak} is the peak current value experienced at the converter arm (top or bottom). See Figure 2.7.

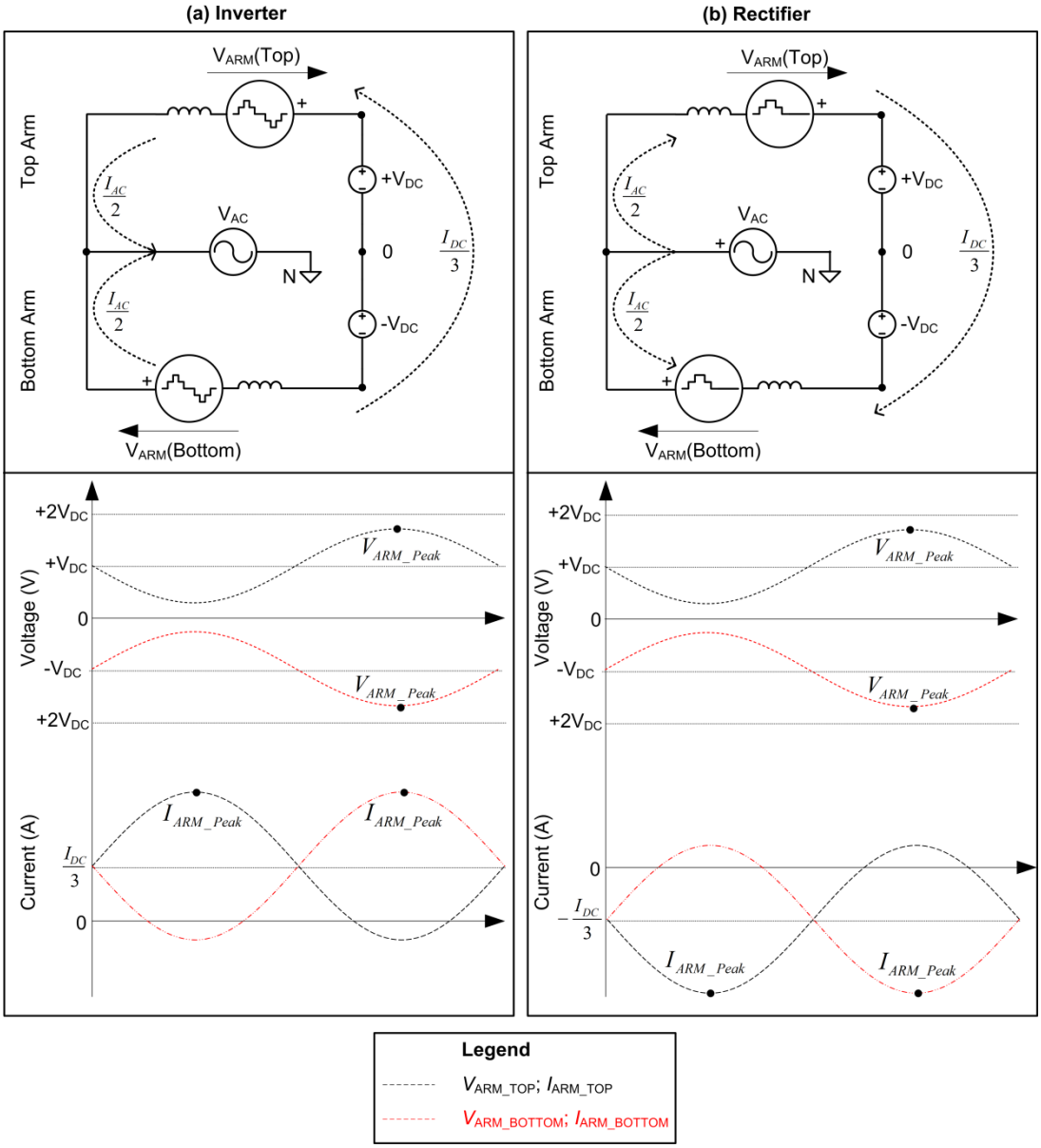

Figure 2.7: 1 phase of MMCC-DSBC showing basic operating principle and peak ratings during (a) inversion; and (b) rectification.

In Figure 2.7 the equivalent circuit for one phase of an MMCC-DSBC topology is shown in order to outline the current paths via the top and bottom converter arm in that phase. This allows the basic operating principle to be discussed and the converter arm ratings established.

The equivalent circuit is shown as an AC voltage V_{AC} connected to the DC rail $\pm V_{DC}$ via the top and bottom converter arms such that the top and bottom arms experience the voltages $(+V_{DC}-V_{AC})$ and $(-V_{DC}+V_{AC})$ respectively.

V_{AC} is either a line or phase voltage depending on the transformer arrangement implemented. For instance V_{AC} is a phase voltage if a star-delta

transformer is used or a line voltage when a star-star transformer arrangement is implemented. A neutral point *N* is shown as a reference for the AC voltages while a ground point *0* is used a reference for the DC side voltages. To simplify the circuit analysis/discussions *N* and *0* are assumed to be at equipotential (this is the case only for an ideal system i.e. Symmetrical AC voltages and stiff DC voltages).

As the AC voltage alternates between positive and negative peak values during each cycle, the peak operating voltage (V_{ARM_Peak}) observed in the top and bottom converter arms is $|V_{DC}+V_{AC}|$. However, in the design of a practical MMCC-DSBC system, each converter arm is rated up to $|2V_{DC}|$ instead. This is done to accommodate an "unlikely" but possible scenario when all the cells in a complementary converter arm are completely bypassed exposing the other arm to voltages up to $2V_{DC}$. Such a scenario is typically as a result of local protection trips reacting to a cascading fault current local to one arm. Incidentally such voltage rating also provides each converter arm with a certain percentage redundancy which helps guarantee minimal converter downtime.

As an inverter (Figure 2.7a), a third of the total DC current flows into the top and bottom converter arms while each arm contributes half the AC current.

As a rectifier (Figure 2.7b), half the AC current flows via the top and bottom converter arms to contribute a third of the total DC current.

Thus in any case each converter arm experiences a combination of AC and DC currents with peak values up to ($\left|\frac{I_{DC}}{3}+\frac{I_{AC\_Peak}}{2}\right|$). This value is essential when choosing the current rating for the components each module, especially the switches.

2.1.5 Emerging MMCC Configurations

The emergence of new MMCC configurations is driven by a need for more compact high voltage converters with extremely low converter losses to drive applications for the smart and super-grid concepts. Academic and industrial researchers are constantly investigating more MMCC configurations.

Current research focus is on MMCC topologies for HVDC applications. Hence the realisation from such investigations are geared towards solutions with common DC link. The hybrid converter reviewed in this work are

classified as: series- and parallel-hybrid topologies. This classification describes the method/configuration of connecting the converter arms between the AC and DC sides. Figure 2.8 shows both configurations.

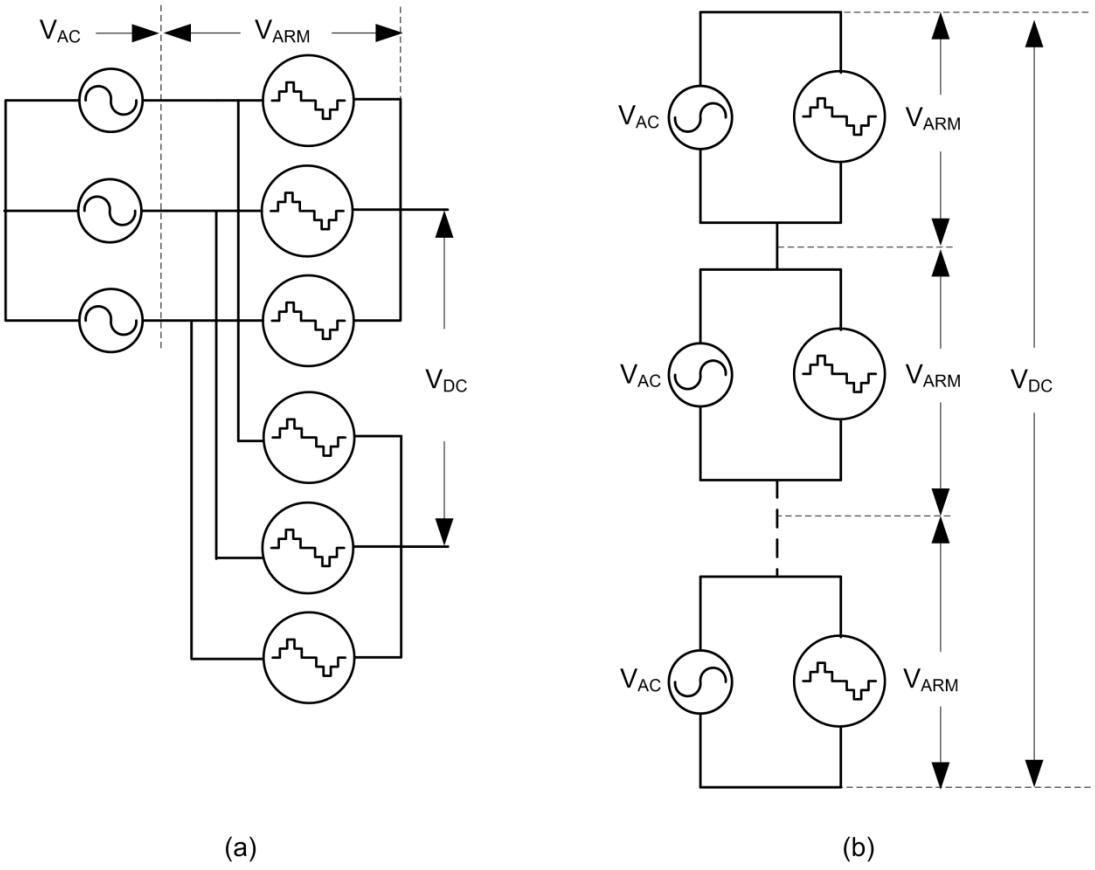

Figure 2.8: Hybrid MMCC Classification based on DC connection showing (a) parallel-hybrid; and (b) series-hybrid configuration.

Based on this classification the MMCC-DSBC topology is inherently of parallel-type connection i.e. the converter arms are connected in parallel between the AC and DC sides.

Hybrid MMCC with Parallel Connection (The Alternate Arm Converter – AAC)

For parallel-hybrid topologies, the connection between the AC and DC side is of parallel type but each converter arm is built from a cascade of different cells or devices to establish V_{ARM}. Different topologies will aim to achieve different objectives, but the main motive in a parallel-hybrid configuration is to provide more control options in the transition of the current flowing in each converter arm as it flows through the circuit. One such example is found in the Alternate Arm Converter (AAC) which showcases the use of director switches (also known as selector switches) to force a prescribed path for the

current through in each phase [44], thus allowing the flow of circulating currents to be governed. Extra functionality such as DC fault blocking is possible depending on the cell type chosen to build up each converter arm.

The selector switches serve the function of choosing which converter arm is activated as the current flows either from AC line to DC terminals or vice versa. Incidentally, the position of the selector switches presents a means of dividing the double star circuit into two single star circuits and three modes of operation are presented. The AAC can function normally as a rectifier/inverter or as two separate MMCC-SSBC circuits which can be operated independently or simultaneously as inverters. During a DC-fault ride-through scenario it is then possible to reconfigure the converter for utility support purposes (STATCOMs, harmonics filters, etc.).

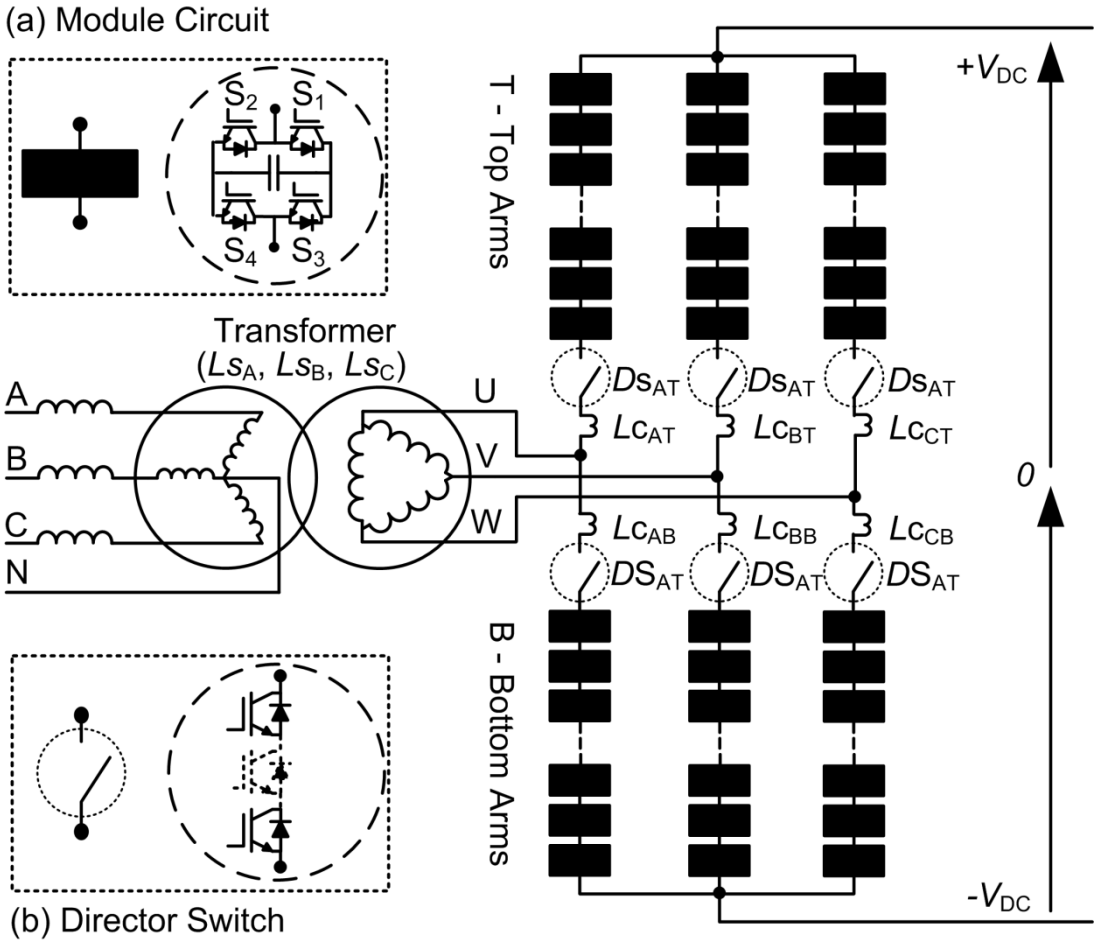

Figure 2.9: The Alternate Arm Converter showing (a) module; and (b) Director switch circuit.

Figure 2.9 shows one parallel hybrid arrangement, an alternate arm converter. The AC line terminals (A, B, C) are connected to the converter AC terminals (U, V, W) via a star-delta transformer connection. The top and

bottom converter arm in each converter phase comprises a series connection of:

- a converter limb reactor (Lc_{AT}, Lc_{AB}, Lc_{BT}, Lc_{BB}, Lc_{CT}, Lc_{CB}) that limits the rapid current transients can occur during switching. This reactor value is also chosen typically smaller than that in the MMCC-DSBC topology such that quick control of circulating current during an "over-lap period" may be achieved [44];
- a director switch (DS_{AT}, DS_{AB}, DS_{BT}, DS_{BB}, DS_{CT}, DS_{CB}): a semiconductor switching assembly (Figure 2.9b) used to connect or disconnect each converter arm into or out of the circuit. This provides extra degrees of control freedom that ensure that an optimal current is transferred between the AC and DC system for a certain DC power value; and
- a series connection of modules (Figure 2.9a) that when collectively controlled provide a required converter arm voltage that governs the flow of current between the AC and DC sides via that arm.

The number of modules required for the AAC is reduced as the director switches are rated to provide voltage support. Switching loss reduction is also suggested in [44], particularly if soft-switching (especially zero-current switching) is adopted for the control of the selector switches.

The Alternate Arm Converter is an active research topic and a subject of several publications. In [63-65] a system level analysis is provided for the topology suggesting a 40% decrease in the number of modules per converter arm compared against an MMCC-DSBC topology of the same rating. Some of the enhanced converter control techniques developed for the AAC are discussed in [50, 66], such as the application of an extended overlap period for the control of the director switches to realise enhanced energy management within the converter, as well as third-order harmonic voltage injection to reduce converter losses. Power loss and thermal analysis were performed for the AAC over a period of 200 seconds. This is presented in [67], which suggests a reduction in switching losses when compared against MMCC-DSBC topology.

One of the main benefits of the AAC is its ability to ride through AC faults and block DC faults, these features are discussed in [68] and [44] respectively.

The choice and build of the semiconductor switching assembly for the director switches (Figure 2.9b) is still an active research topic. Perhaps with the current research into wide band-gap semiconductor devices, the near future will present more sophisticated semiconductor devices to better serve at such a capacity.

MMCC Series-Hybrid Connection (The Series Bridge Converter -SBC)

A series-hybrid MMCC still comprises of a series stack of cells on each converter phase arm. However a series connection of the converter arms (U, V, W) forms the DC rail. One such topology is the Series Bridge Converter (SBC) presented in [69] as shown in Figure 2.10.

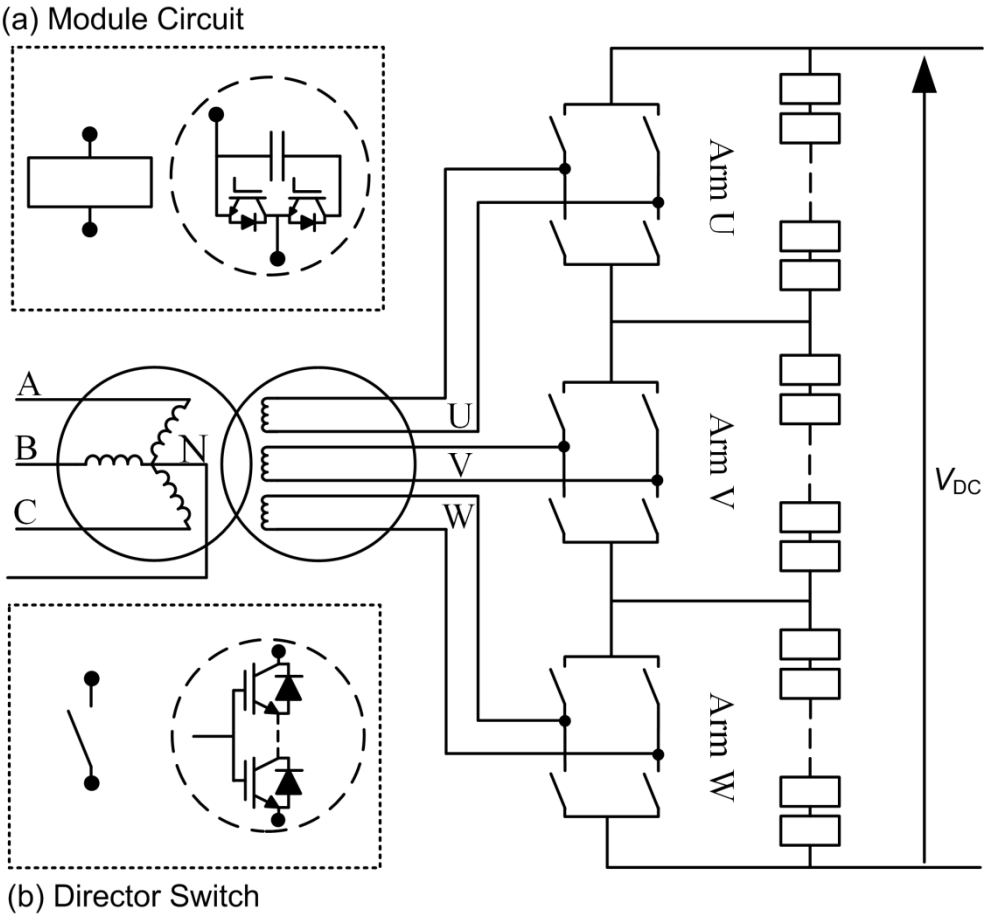

Figure 2.10: The Series Bridge Converter showing (a) module; and (b) Director switch circuit.

As shown in Figure 2.10, The SBC is built up using only three converter arms (U, V, W). Each converter arm comprises an H-bridge circuit connected in parallel with a series string of modules (chain-link). The three arms are connected in series to provide or receive power from the DC link.

For instance with the converter operating as an inverter, the 3-phase AC waveforms are generated as follows:

In each arm:

- the Chain-link receives energy from the DC link and is controlled to generate three quasi-sinusoidal but full-wave rectified waveforms (with each waveform displaced 120^0 from the other);
- the H-Bridge circuit is controlled to “invert” the rectified waveform provided by the Chain-link every 180^0 thus generating a quasi-sinusoidal AC waveform; and
- the resulting AC waveform is coupled to the AC line via three single phase transformers.

Investigations have shown a possible converter footprint reduction (from sub-module count reduction) when compared with an MMCC-DSBC topology of similar power rating. As well, the SBC is capable of advanced functionality such as active DC filtering due to its configuration and control [70]. The converter footprint is smaller than that of the MMCC-DSBC and AAC making this topology attractive for offshore applications where footprint is at a premium. As a result the SBC topology is a subject of active research [69, 71].

Voltage and Current Ratings for the AAC and SBC

The ratings for the chainlinks and director switches for the AAC and SBC are shown in Table 2.5. For the AAC these ratings are established from [50, 63], however as ratings for the SBC chainlinks and director switches are unclear in the relevant literature [69-71], Figure 2.11 is provided to support the specifications.

Table 2.5: *I – V* Ratings for the AAC and SBC.

Rating	Voltage (*V*)	Current (*A*)
AAC	$V_{ARM} = V_{\mathrm{DC}};\ V_{DS} = V_{\mathrm{AC}} - \frac{V_{\mathrm{DC}}}{2}$	$I_{ARM} = \left(\frac{I_{\mathrm{DC}}}{3} + \frac{I_{\mathrm{AC}}}{2} \right)$
SBC	$V_{ARM} = \frac{V_{\mathrm{DC}}}{3};\ V_{DS} = V_{\mathrm{AC}} - \frac{V_{\mathrm{DC}}}{3}$	$I_{ARM} = \frac{I_{\mathrm{AC}}}{2} + I_{\mathrm{DC}};\ I_{DS} = I_{\mathrm{AC}}$

where

V_{DC} is the total DC rail voltage.$\pm V_{DC}$ for the AAC and V_{DC} for the SBC.

V_{AC} is the AC voltage applied to the converter (this is either a phase or line-line voltage depending on the transformer arrangement chosen).

V_{ARM} is the voltage rating of the chainlink.

I_{DC} is a DC current absorbed or supplied by an inverter or rectifier.

I_{AC} is an AC current absorbed or supplied by an inverter or rectifier.

I_{ARM} is current rating of the chainlink.

I_{DS} is current rating of the Director Switch.

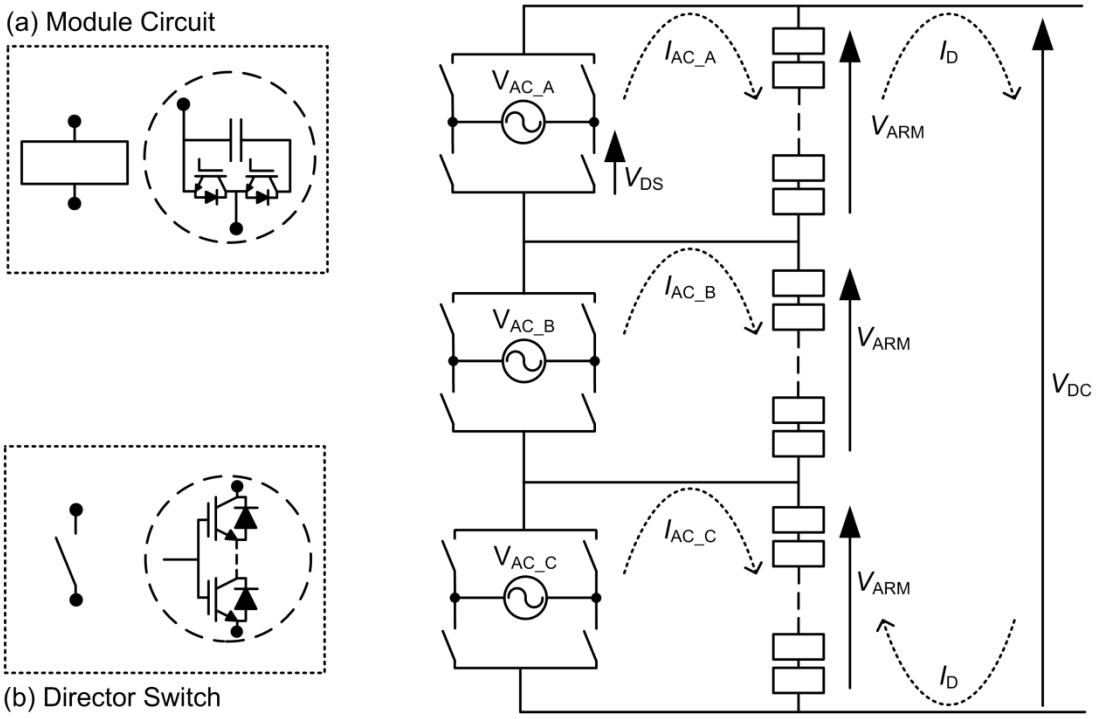

Figure 2.11: SBC basic operating principle to support specification for peak ratings.

In Figure 2.7 the circuit for a SBC is shown which outlines the current paths as well as establishes peak voltage and current expectations within the converter.

The circuit shows each phase of a three-phase AC line $V_{AC\_(A, B, C)}$ connected to a H-bridge built using four director switches. The H-bridges are connected in series via their DC terminals to form the DC rail ($+V_{DC}$, 0) and three converter arms (one for each H-bridge) are connected to the DC terminals of

the H-bridges such that a combination of AC and DC currents flows via the converter arms while only AC currents flow via the director switches. This arrangement supports ratings specified in Table 2.5 for the converter arms (V_{ARM}) and director switches (V_{DS}) in the SBC.

To summarise the findings in Table 2.5, the SBC is expected to offer further size (hence cost) reduction than the AAC compared to a MMCC-DSBC because:

- There is a lower requirement for peak voltage rating for each converter arm; and
- In reality building such a converter while adhering to voltage clearance requirements needs the erection of only two equipment columns (i.e. one for the converter arms and one for the director switches).

Table 2.5 also suggests that the peak current rating for the converter arms is expected to increase and although this needs further clarification, it is immediately evident that the SBC is an attractive topology for offshore applications (wind farm power transmission) while the AAC is suitable for interconnecting AC/DC system which are prone to faults.

2.2 Discussion and Comparison of MMCC Configurations

In this section a discussion is presented in order to compare the following described topologies:

- MMCC-SSBC
- MMCC-SDBC
- MMCC-DSBC
- AAC
- SBC

These topologies were developed to tackle different applications' suitability, making them difficult to compare directly across common criteria. To tackle this difficulty, the topologies are first compared using standard system design criteria and against a range of applications (FACTS, HVDC, Offshore Power Transmission).

A filled radar chart is used to graphically present comparison for each group above and express the rank of each topology. This type of chart is a good platform for comparing different systems which are normally not directly

comparable. A table is also provided showing how the topology ranks are determined.

System Design Criteria

Every system has to consider the five basic design parameters:

- Size (and Weight): Some applications place a high premium on cost, weight or both. For instance in an offshore application a design with smaller (footprint) is more attractive, while for an aerospace application size and weight reduction are of equal and great importance.
- Cost: This is the overall cost for choosing a certain design/technology (not just the direct financial cost). For instance using a star-star instead of a star-delta transformer incurs an extra “cost” in terms of grounding transformers.
- Efficiency: System efficiency is important in the choice of any design but it becomes more stringent in applications that operate in high orders of magnitude. For instance in a 600MW HVDC application, 1% loss implies 6 million watts of heat to dissipate.
- Performance: This is often associated with how closely the system output tracks a prescribed reference (or fundamental). For a converter certain qualities are used to track performance such as: dynamic response to step changes/faults, harmonic content, etc.
- Reliability: This is associated with the robustness of the system. In summary it is a reflection of how much tolerance is exhibited by the system before shut-down is required.

Each application accords more importance to some of the design parameters than the others. For instance for a FACTS application, size and performance may be of greatest importance while for a HVDC application size, efficiency and reliability will often hold great importance.

To capture this variance, a ranking system is developed to capture the suitability of each topology to the different applications. Basically the topology rank is obtained by multiplying an importance value by a suitability value. The importance values are in a range of 1 – 3 and allocated to each system design parameter for each application where:

- 1: Low importance;
- 2: Medium importance; and
- 3: High importance.

On the other hand, the suitability values range are allocated to each topology and reflect how much the topology meets the system design parameter. The suitability values are in a range of 1 – 5, where:

- 0: Not Applicable;
- 1: Unsuitable;
- 2: Somewhat unsuitable;
- 3: Neutral;
- 4: Somewhat suitable; and
- 5: Very Suitable.

Final ranking is achieved by multiplying the suitability and importance values.

Topology Ranking for a FACTS Application

Table 2.6: Converter topology ranking for a FACTS application.

	SSBC	**SDBC**	**DSBC**	**AAC**	**SBC**
Size	10	10	4	6	8
Cost	8	8	4	8	8
Efficiency	6	6	6	8	8
Performance	3	12	15	15	9
Reliability	4	4	4	5	3
Total	**31**	**40**	**33**	**42**	**36**

Importance values: Size (2); Cost (2); Efficiency (2); Performance (3); Reliability (1).

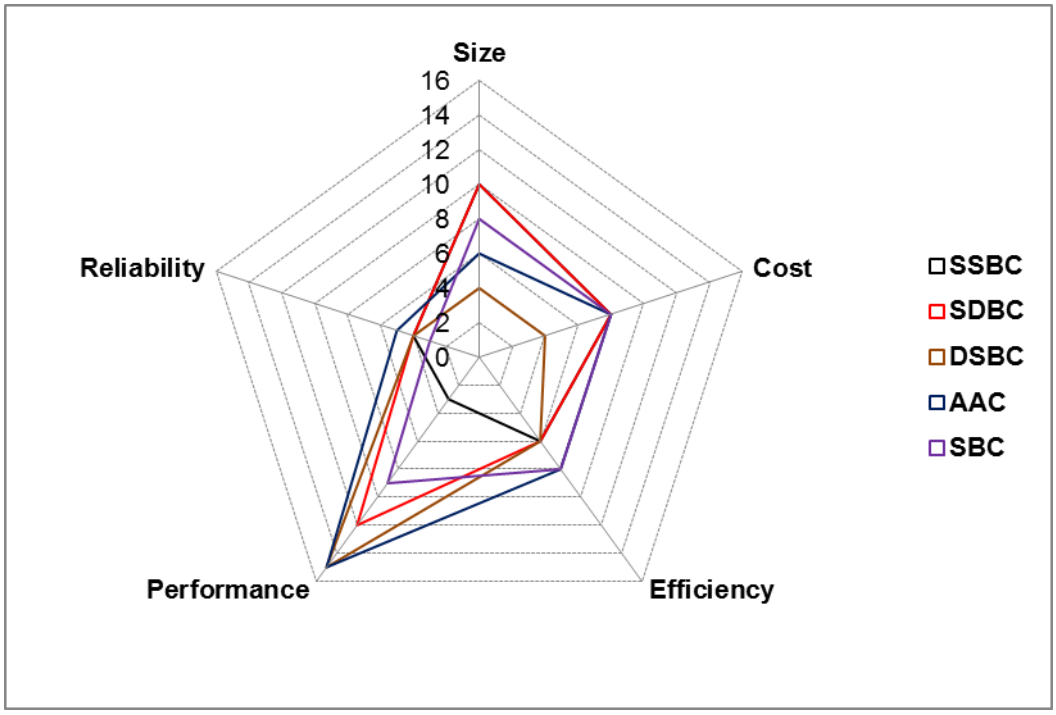

Figure 2.12: Filled radar showing topology ranking for FACTS applications.

Topology Ranking for a HVDC Application

Table 2.7: Converter topology ranking for a HVDC application.

	SSBC	SDBC	DSBC	AAC	SBC
Size	0	0	4	6	8
Cost	0	0	2	4	4
Efficiency	0	0	9	12	12
Performance	0	0	15	15	9
Reliability	0	0	12	15	9
Total	**0**	**0**	**42**	**52**	**42**

Importance values: Size (2); Cost (1); Efficiency (3); Performance (3); Reliability (3).

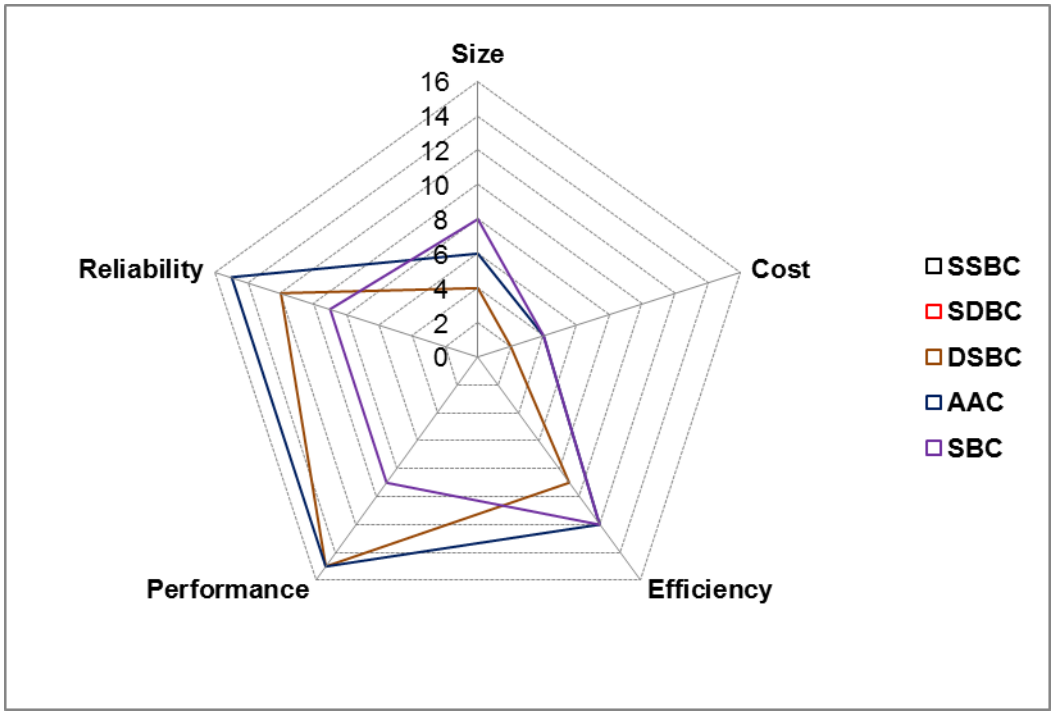

Figure 2.13: Filled radar showing topology ranking for a HVDC application.

Topology Ranking for Offshore Power Transmission

Table 2.8: Converter topology ranking for an offshore power transmission application.

	SSBC	SDBC	DSBC	AAC	SBC
Size	0	0	6	9	15
Cost	0	0	4	8	8
Efficiency	0	0	6	8	8
Performance	0	0	6	8	8
Reliability	0	0	12	12	12
Total	**0**	**0**	**34**	**45**	**51**

Importance values: Size (3); Cost (2); Efficiency (2); Performance (2); Reliability (3).

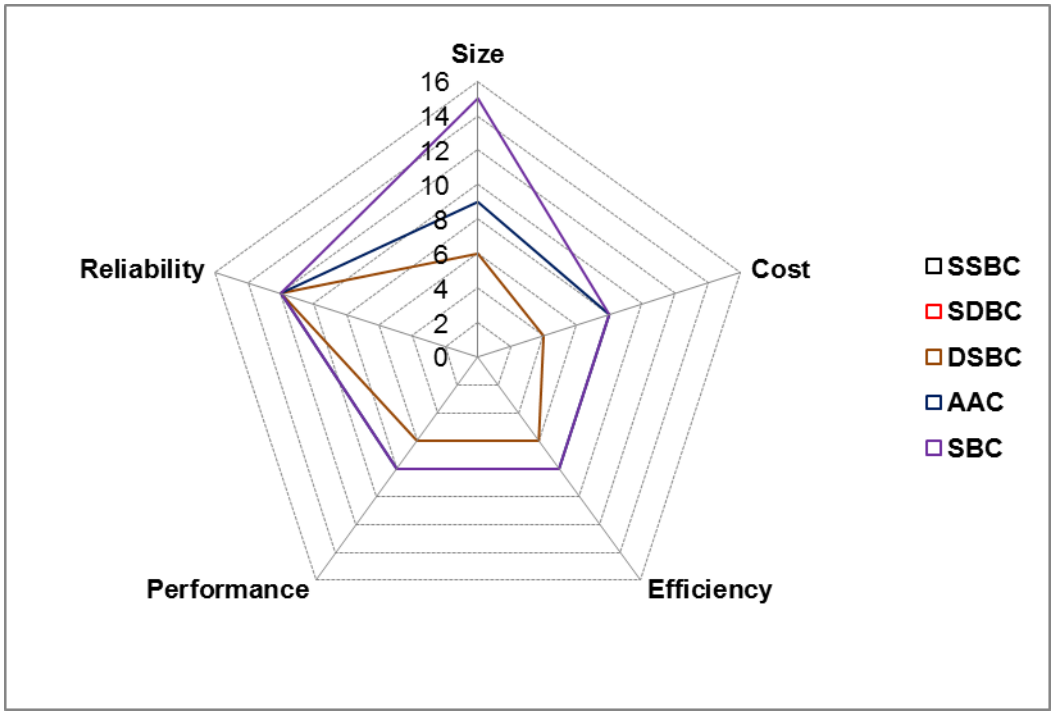

Figure 2.14: Filled radar showing topology ranking for an offshore power transmission application.

2.3 Summary

The concept of Modular Multilevel Cascade Converters has been reviewed as the fundamental background for describing the proposed topology based on a different module structure.

The chapter presented the two converter topologies most commonly used as sub-modules in MMCCs. The discussions highlighted their main features; sub-modules using half-bridge cells, though using fewer semiconductor devices, cannot suppress DC faults by converter operation; sub-modules with a full-bridge cell can suppress DC faults by using the switching devices.

The chapter then gave a comprehensive review of four modular multilevel converter topologies; MMCC-SSBC , MMCC-SDBC, MMCC-DSBC and MMCC-DDBC. It was shown that the former two use H-bridge cells as modules and are suitable only for STATCOM and BESS applications. In contrast the latter two double arm configurations use half-bridge cells as modules and are only for HVDC converters. An extensive analysis was given of the phenomenon of circulating current occurring in MMCC-DSBC. The chapter also reviewed the emerging forms of MMC, such as AAC and SBC.

Comparisons of all the topologies according to five well-known criterion were given.

Chapter 3
MMFC Converter Sub-module Benchmarking

So far, previous discussions have focused on topologies with modifications to the system-wide converter structure but all using the conventional half- or H-bridge sub-modules within each converter phase arm. Other emerging converter topologies such as flying capacitor or diode clamped converters may also be used to form sub-modules for the MMCCs.

This chapter presents a new set of sub-modules for MMCC based on the flying capacitor topology. These are:

- 3-level half-bridge flying capacitor cells;
- 3-level H-bridge flying capacitor cells; and
- 3-level Hybrid H-bridge flying capacitor cells.

Before exploring these topologies for specific applications, their features, advantages and shortcomings as compared with their two well-known and well-used counterparts need to be assessed and quantified against a set of clearly defined criteria or metrics. Thus in this chapter a set of practically-oriented metrics for evaluating sub-modules for modular multilevel converters is established. These are first applied to evaluate the typical half- and H-bridge sub-modules. They are then applied to the flying capacitor - based sub-module concepts, and results are compared. Codifying these metrics provides a potentially useful tool for practical designers of converter-based equipment.

The 3-level H-bridge flying capacitor sub-module is chosen for further investigation in this research, because it offers more degrees of control freedom at the sub-module level.

3.1 Sub-module Benchmark Analysis

A set of guidelines and assumptions used while assessing the different sub-module concepts are outlined. Assumptions are backed either by data from a manufacturer's datasheet or relevant publications. The following five metrics are established for assessing the sub-module concepts: footprint; cost; redundancy; efficiency; and performance.

3.1.1 Guidelines for Assessing Sub-module concepts

The main components that form the sub-module concepts investigated are a combination of at least one of each item below: power semiconductor switch; Capacitor; Heat Sink(s); and Gate Electronics Module (GEM).

Table 3.1 outlines the device options chosen and used to derive values for the sub-module assessment metrics.

Table 3.1: Devices used for sub-module assessment parameters based on hardware rig.

Device	Manufacturer reference	Comments
Switch Module	IKW30N60T (Infineon)	600 *V*, 30 *A* Power IGBT
Capacitor	EETED2G561EA (Panasonic)	600 V, 560µF Capacitor
Heat Sink	SK105/105SA (Fisher Elektronics)	Chosen specifically for its compensating thermal impedance (R_{th} = 2 K/W) to match maximum switch module operation.
Gate Electronics Module (GEM)	FPGA (ProASIC3) Transducers (LEM)	Only the key parts that vary across the different sub-module concepts are considered.

Three points are worth noting:

In a power conversion application anti-parallel diodes are typically included either as separate physical devices or parasitic/body diodes connected across each power semiconductor switch. The declaration of a power semiconductor switch S_1; S_2; .. ; S_X by the author is inclusive of such a diode i.e. D_1; D_2; …; D_X.

Certain power conversion applications e.g. Battery Energy Storage Systems use batteries in place of capacitors. But such applications are not investigated during this study.

A pair of switches is operated in a complementary manner to avoid short circuit of a sub-module capacitor.

In practice, devices are selected to match an application's requirements and may present a different voltage, current or capacitance rating. The devices listed in Table 3.1 are selected mainly to support further investigations including software and hardware evaluation conducted during the research.

3.1.1.1 Sub-module Footprint Assessment

To ensure consistency, the footprint assessment of each sub-module concept is based on the requirements for a 60 kV converter arm, with the geometry as shown in Figure 3.1.

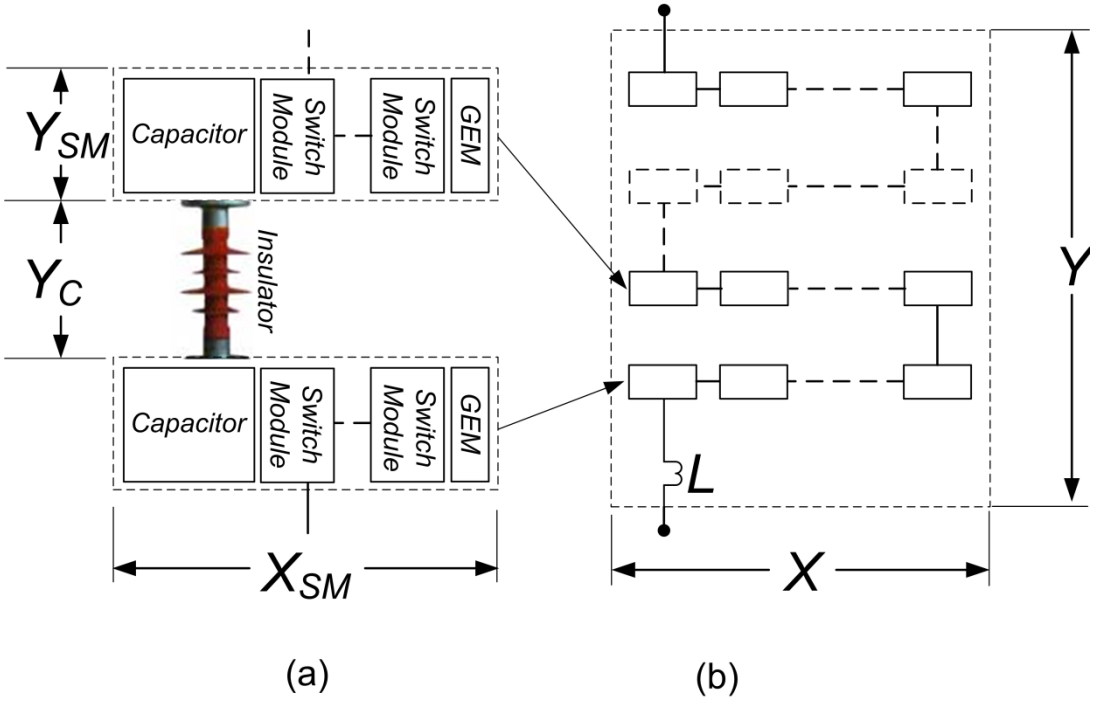

Figure 3.1: Guideline for footprint assessment (a) sub-module showing insulator with gap/clearance distance; (b) typical phase arm layout .

The sub-module hardware set-up used for the footprint assessment is shown in Figure 3.1(a) while a typical converter phase arm layout is shown in Figure 3.1(b). This arrangement outlines the capacitor, the Switch module; and the GEM. It is assumed that the footprint for the heat sink is included in that of the Switch module.

The total footprint value for a 60 kV converter arm is derived as a function of the width (X) and height (Y) of the converter arm as expressed in (3.1) and the following factors are taken into consideration:

- the number of sub-modules tiers required to realise the 60 *k*V converter arm.
- recommended gap/clearance distance between each sub-module tier as specified in IEC60815[1]; and
- sub-module width as a function of component count i.e. number of switch modules and capacitors required for each sub-module concept.

$$Footpr\,\mathrm{int} = \left[n_T.Y_{SM} + (n_T + 1)Y_C\right] \times X_{SM}.n_{ST} \qquad \textbf{3.1}$$

where n_{ST} is the number of sub-modules per tier. The value of 10 is chosen here for ease in analytical calculations.

n_T is the number of sub-module tiers required for a 60 *k*V arm. The total number of sub-modules for a 60 kV arm is n_T *times* n_{ST}.

Y_{SM} is the sub-module height. A value of 20 cm is used (This is based on the height specified for the SK105 heat sink in Table 3.1 plus 25%).

X_{SM} represents the per-unitised sub-module width. Values are chosen based on Table 3.2.

Y_C is the inter-tier clearance distance. The value is chosen based on expression (3.2).

$$Y_C = USCD \times \frac{60kV}{n_T} \qquad \textbf{3.2}$$

where *USCD* = 36.5 mm/kV.

The values in Table 3.2 are chosen so that a half-bridge sub-module i.e. with 1 switch module; 1 capacitor and 1 GEM presents a per-unitised width of 1 p.u. This is a typical ratio experienced with a sub-module for high voltage applications.

Also, the footprint values are presented in cm rather than cm^2 since the width of the sub-module is per-unitised.

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[1] IEC 60815: Guide for the selection and dimensioning of high-voltage insulators for polluted conditions; Definitions, information and general principles.

Table 3.2: Per-unitised values for sub-module width.

Device	Width (p.u)
Switch Module[2]	X_S = 0.2 per Switch module
Capacitor	X_C = 0.6 per Capacitor
GEM	X_{GEM} = 0.2 per GEM
Total (X_{SM})	$X_{SM} = X_S + X_C + X_{GEM}$

3.1.1.2 Sub-module Cost Assessment

Cost assessment is performed using Table 3.3. Again the total cost used is the cost of building a 60 kV converter arm.

Table 3.3: Guidelines for assessing sub-module cost.

Device	Part Number	Unit Cost (£)[3]
Switch Module	IKW30N60T (1 Pair)	8.94
Capacitor	EETED2G561EA	8.15
Heat Sink	SK105	10.65
GEM	FPGA Board (ProASIC3)	6.00
	Gate Drive + Isolation (ACPL-332J; MEV1S0515SC)	9.1
	Voltage Transducer (LEM LV 25-P)	42.41

3.1.1.3 Sub-module Redundancy Assessment

Redundancy is determined for each sub-module concept based on the number of transition states available (i.e. states that result in sub-module voltage variation due to the converter arm current direction). For instance a

[2] A pair of switches operated in a complementary manner to avoid short circuit of a sub-module capacitor.

[3] Values based on Farnell (uk.farnell.com) prices for each part at the time of assessment.

half-bridge sub-module has only 2 transition states. The state when both devices are off is not considered an operating mode. This mode can be used for black- start[4] of a Modular Multilevel Converter, and not during normal operation.

3.1.1.4 Sub-module Efficiency Assessment

The assessment of sub-module efficiency is based primarily on an analytical method for calculating the losses of an MMC-based VSC HVDC. This is an adaptation of a semiconductor manufacturer application note [72] and with IEC 62751[5] as reference. This loss assessment method defines nine loss categories (P_{V1} to P_{V9}) for such an HVDC converter arm, however only four of these are adopted and they are sufficient to provide the metrics for sub-module efficiency, namely:

- Conduction losses for IGBT (P_{V1}) and diode (P_{V2}); and
- Switching losses P_{V6} and P_{V7} for IGBT and diode respectively.

Conduction losses

Two methods are available for ascertaining the conduction losses. One relies on intensive digital simulations fed with relatively accurate curve-fit data for device on-state voltage as a function of current [73-75]. The other method relies on the use of piecewise linear characteristics to obtain time-averaged conduction losses [76]. The latter method is less cumbersome and thus is adopted during this work.

The instantaneous conduction losses P_{V1}^{*} and P_{V2}^{*} are calculated using the expressions in (3.3) and (3.4)

$$P_{V1}^{*} = V_{CE0}.I_{ARM} + R_{ON\_T}.I_{ARM}^{2} \qquad \textbf{3.3}$$

$$P_{V2}^{*} = V_{F0}.I_{ARM} + R_{ON\_D}.I_{ARM}^{2} \qquad \textbf{3.4}$$

where V_{CE0} is the IGBT on-state zero-current collector-emitter voltage.

---

[4] In this context, black-start refers to the start-up procedure for a Modular Multilevel Converter, when there is DC link voltage but no AC voltage.

[5] IEC62751 – Determination of power losses in voltage sourced converter (VSC) valves for HVDC.

R_{ON_T} is the IGBT on-state resistance.

V_{F0} is the zero-current diode forward voltage.

R_{ON_D} is the diode on-state resistance.

I_{ARM} is the instantaneous value of converter arm current.

The values used for V_{CE0} and V_{F0} are obtained via piecewise linear interpolation [72] and using Infineon's IKW30N60T datasheet [77]. This is shown in Figure 3.2.

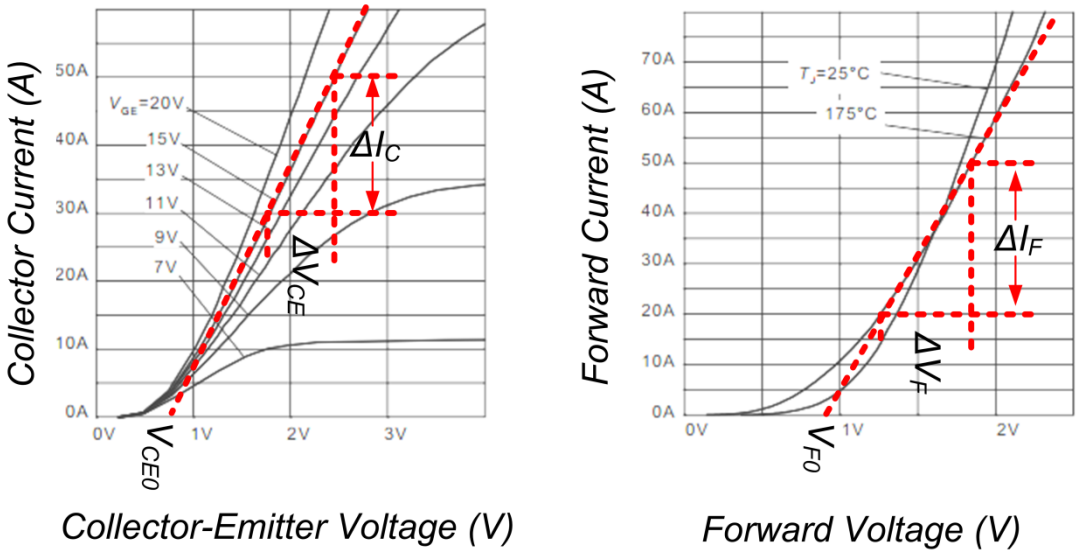

Figure 3.2: Determination of current-dependent device parameters (a) V_{CE0} and R_{ON_T}; and (b) V_{F0} and R_{ON_D}.

Based on Figure 3.2, V_{CE0} = 0.75 V and V_{F0} = 0.9 V, while R_{ON_T} and R_{ON_D} are derived as shown in (3.5). References [72] and [78] recommend that a margin of around 0.4 *V* be added to account for tolerance between typical and maximum collector-emitter saturation characteristics, thus the values are adjusted accordingly such that V_{CE0} = 0.75 + 0.4 = 1.15 V; and V_{F0} = 0.9 + 0.4 = 1.3 V.

$$R_{ON\_T} = \frac{\Delta V_{CE}}{\Delta I_C} = \frac{(2.4-1.7)V}{(50-30)A} = 0.035\Omega$$
$$R_{ON\_D} = \frac{\Delta V_F}{\Delta I_F} = \frac{(1.8-1.25)V}{(50-20)A} = 0.018\Omega \qquad \textbf{3.5}$$

The time-averaged conduction losses P_{V1} and P_{V2} are calculated using the average and RMS converter arm currents as shown in (3.6) and (3.7).

$$P_{V1} = V_{CE0}.I_{AVG} + R_{ON\_T}.I_{RMS}^2 \quad \textbf{3.6}$$

$$P_{V2} = V_{F0}.I_{AVG} + R_{ON\_D}.I_{RMS}^2 \quad \textbf{3.7}$$

where I_{AVG} is the converter arm average current.

I_{RMS} is the converter arm R.M.S current.

Figure 3.3 describes the time varying functions of the converter arm current and voltage that are used for assessing each sub-module. This is typical wave-shape for a converter arm within a MMC-DSBC topology and operating as an AC to DC converter.

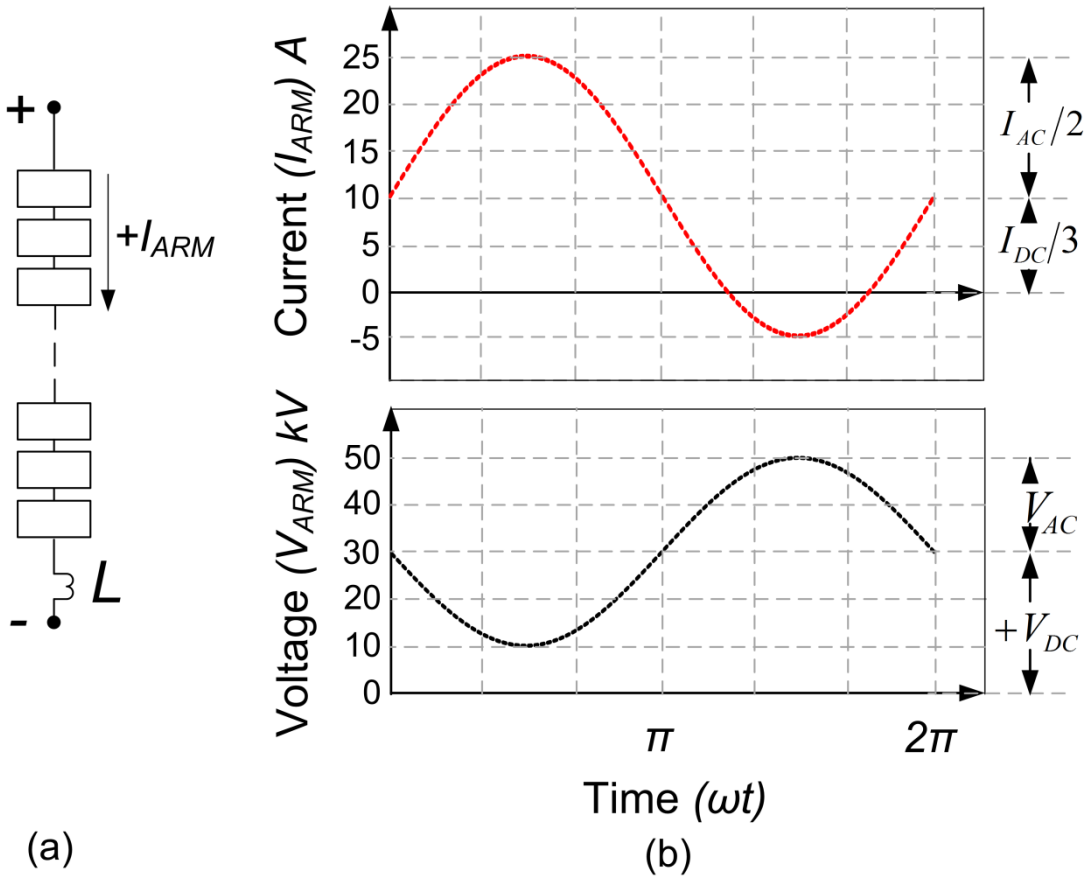

Figure 3.3: (a) Converter arm and (b) time varying function of arm current and voltage.

Based on the converter arm current shown in Figure 3.3(b) the average current is simply the D.C value. On the other hand, the mean square value is the sum of the separate AC and DC mean square values such that (3.6) and (3.7) are re-written as shown in (3.8) and (3.9) to reflect an adaptation from [76] for a converter arm in a MMC-DSBC rectifier.

$$P_{V1} = 0.2V_{CE0}.\frac{I_{DC}}{3} + 0.2R_{ON\_T}\left(\frac{I_{AC}^2}{4} + \frac{I_{DC}^2}{9}\right) \quad \textbf{3.8}$$

$$P_{V2} = 0.8V_{F0}.\frac{I_{DC}}{3} + 0.8R_{ON\_D}.\left(\frac{I_{AC}^2}{4} + \frac{I_{DC}^2}{9}\right) \quad \textbf{3.9}$$

(3.8) and (3.9) show that there is always current passing through devices even though with voltage $V_{CE0,}$ V_{F0}. The conduction loss is thus a sum of all IGBT and diode conduction losses as shown in (3.10).

$$P_{COND} = n_{CS}\left(P_{V1} + P_{V2}\right) \quad 3.10$$

where n_{CS} is the number of complementary switch pairs / sub-module i.e. switch modules.

Switching losses

It is assumed that all the sub-modules are switched in 3 times during each fundamental cycle (i.e. 150 Hz for a 50 Hz fundamental) as is the case when a carrier-based switching scheme with a 150 Hz carrier is used. In practice a sophisticated “active select and sort” optimisation algorithm is typically used so that only the required number of sub-modules are switched during each cycle to achieve a desired criterion e.g. sub-module capacitor voltage variation; sub-module loss per cycle; Total Harmonic Distortion; or a combination of either.

The switching loss P_{SW} is calculated as shown in (3.11)

$$P_{SW} = n_{CS} f_{SW}(E_{ON} + E_{OFF}) \quad \textbf{3.11}$$

where f_{SW} is the sub-module switching frequency. 150Hz is used.

E_{ON} is turn-on energy (including tail and diode reverse recovery). 1.0mJ

E_{OFF} is turn-on energy (including tail and diode reverse recovery). 1.1mJ

Values for E_{ON} and E_{OFF} are obtained from Infineon’s IKW30N60T datasheet [77].

Total losses for a 60 kV Converter Arm

To account for the differences in voltage output capacity in each sub-module concept, the loss assessment values used are based on a 60 k*V* converter arm rather than for an individual sub-module. This will account for the fact that the total number of sub-modules required to realise the same converter arm is different for each sub-module concept.

The loss for a 60 kV converter arm is calculated using the values obtained from (3.10) and (3.11) as shown in (3.12) while the efficiency is calculated using (3.13).

$$P_{LOSS\_60kV} = n_{SM}\left(P_{COND} + P_{SW}\right) \qquad \textbf{3.12}$$

$$Efficiency\ (p.u) = 1 - \frac{P_{LOSS\_60kV}}{\sqrt{\left(V_{AC}^2 + V_{DC}^2\right)\left(\frac{I_{AC}^2}{4} + \frac{I_{DC}^2}{9}\right)}} \qquad \textbf{3.13}$$

where V_{DC} is a DC voltage portion i.e DC rail voltage is $\pm V_{DC}$ = ±30kV (See Figure 3.3b).

V_{AC} is the AC voltage applied to the converter arm = 20kV as shown in Figure 3.3(b).

3.1.1.5 Sub-module Performance Assessment

At system level, qualities such as Total Harmonic Distortion (THD) are typically used to assess converter performance but this is insufficient for sub-module level analysis. Table 3.4 presents an alternative yet simple means as the sub-module performance assessment. This is a “score based” method assessing the number of functions a converter built by a particular sub-module can perform.

Table 3.4: Assessing sub-module performance.

Functionality	Score
Supports Single Star Bridge cell (SSBC) topology	0.25
Supports Single Delta Bridge cell (SDBC) topology	0.25
Supports Double Star Bridge cell (DSBC) topology	0.25
Supports DC Fault Blocking and DC Fault Ride Through	0.25

Basically each sub-module is scored based on the functionalities (and topologies) supported.

3.1.2 Benchmark Analysis for the Half-bridge Sub-module

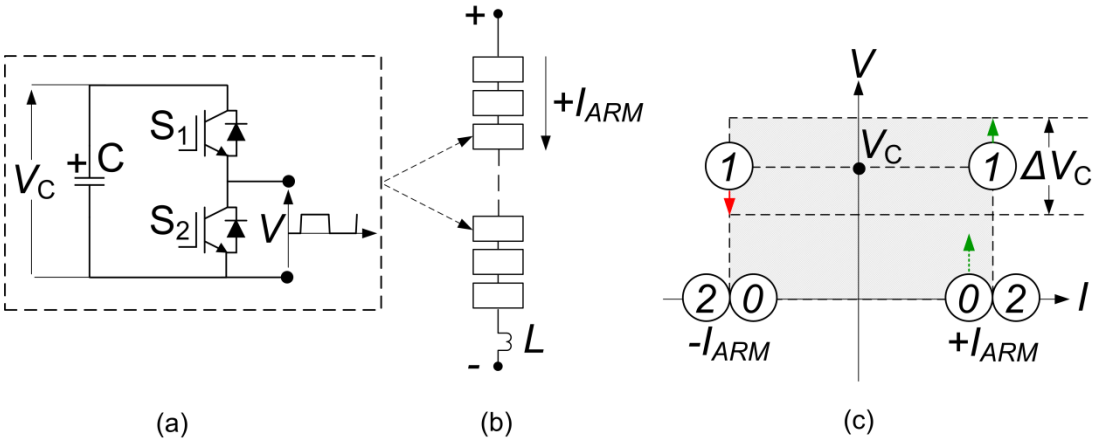

Figure 3.4: Half-bridge analysis showing sub-module (a) configuration; (b) cascade arrangement for converter arm (c) *I-V* Quadrant showing operation and transition states.

The sub-module configuration for a half-bridge arrangement is shown in Figure 3.4(a) and outlines one switch module i.e. two power semiconductor devices (S_1; S_2) connected in parallel across the sub-module capacitor C. The sub-module positive and negative output terminals are realised between S_1; S_2 and at the emitter (or drain if MOSFET is used) of S_2 respectively. The cascade arrangement for a converter arm is shown in Figure 3.4(b) and operation is such that each sub-module presents a voltage (*0* or V_C volts). The converter arm voltage at each switching instant is the sum of all active sub-module voltages. Figure 3.4(c) shows how the operating states for the half-bridge sub-module distribute across a quadrant plane occupying only two quadrants (±*I; V*). The transitional states, i.e. states that result in sub-module capacitor voltage variation, are also shown in Table 3.5.

Table 3.5: Half-bridge Sub-module Operating and Transition States.

V – output voltage; I_{ARM} – arm current direction; and *V*c - capacitor voltage showing transition (↓ = Discharging, ↑ = Charging, NC = No Change)

State	S_1	S_2	*V*	
			$+I_{ARM}$	$-I_{ARM}$
0	0	1	0	0
1	1	0	↑*V*c	↓*V*c

Half-bridge Footprint Assessment

Table 3.6: Per-unitised width for Half-bridge Sub-module.

Device	Quantity	Width (p.u)
Switch Module	1	0.2
Capacitor	1	0.6
GEM	1	0.2
***Total* (X_{SM}) p.u.**		**1.0**

$$Y_C = USCD \times \frac{60kV}{n_T} = 3.6cm/kV \times \frac{60kV}{10} = 21.9cm$$

$$Footpr\,\text{int} = \left[n_T.Y_{SM} + (n_T + 1)Y_C\right] \times X_{SM}.n_{ST}$$
$$= \left[10 \times 20 + (10+1)21.9\right] \times 1.0 \times 10 = 4409cm$$

Half-bridge Cost Assessment

Table 3.7: Half-bridge Sub-module Cost Assessment.

Device		**Quantity**	**Cost (£)**
Switch Module		1	8.94
Capacitor		1	8.15
Heat Sink		1	10.65
GEM	FPGA Board	1	6.00
	Gate Drive + Isolation	2	18.2
	Voltage Transducer	1	42.41
		Total	**94.35**
		Total for 60kV arm (i.e x 100)	**9435**

Half-bridge Redundancy Assessment

Figure 3.4(c) outlines 2 transition states in State 1 which cause the sub-module capacitor voltage value to increase or decrease. Careful sub-module management is typically applied to maintain the capacitor voltage within a band ΔV_C. This can be achieved using a passive carrier-based modulation technique with natural balancing or via an active selection algorithm.

Half-bridge Efficiency Assessment

$$P_{V1} = \left[0.2 \times 1.15 \times \frac{30}{3}\right] + \left[0.2 \times 0.035\left(\frac{30^2}{4} + \frac{30^2}{9}\right)\right] = 4.58W$$

$$P_{V2} = \left[0.8 \times 1.3 \times \frac{30}{3}\right] + \left[0.8 \times 0.018 \times \left(\frac{30^2}{4} + \frac{30^2}{9}\right)\right] = 15.08W$$

$$P_{COND} = 1 \times (4.58 + 15.08) = 19.66W$$

$$P_{SW} = 1 \times 150 \times (1.0 + 1.1) \times 10^{-3} = 0.315W$$

$$P_{LOSS\_60kV} = 100 \times (19.66 + 0.315) = 1997.5W$$

$$Efficiency\ (\%) = \left(1 - \frac{1997.5}{\sqrt{(20^2 + 30^2) \times \left(\frac{30^2}{4} + \frac{30^2}{9}\right)}}\right) \times 100 = 99.69\%$$

This value is based on the fact that all sub-modules are switched in every cycle (e.g. when a passive[6] carrier-based PWM scheme is used).

In practice a sophisticated optimisation-based algorithm is typically used to actively select only the required number of sub-modules while optimizing for sub-module capacitor voltage tolerance as well as losses. This has been proven to reduce losses down to 1% [62, 73, 76, 79].

Table 3.8: Half-bridge sub-module efficiency using guideline[7].

Parameter	**Value**
n_{CS} (number of switch modules per sub-module)	1
P_{V1} (3.8)	4.58 W
P_{V2} (3.9)	15.08 W
P_{COND} (3.10)	19.66 W
P_{SW} (3.11)	0.315 W
n_{SM} (number of sub-modules in 60kV arm)	100
P_{LOSS_60kV} (3.12)	1997.5 W
Efficiency (3.13) in %	**99.69%**

[6] Passive carriers can be phase-locked to their reference signal or free-running but without the capability of phase/amplitude adjustment.

[7] V_{CEO} = 1.15 *V*; R_{ON_T} = 0.035 Ω; V_{FO} = 1.3 *V*; R_{ON_D} = 0.018 Ω; f_{SW} = 150 *Hz;* E_{ON} = 1.0 *mJ;* E_{OFF} = 1.1 *mJ;* I_{DC} = 30 *A*; I_{AC}; 30 *A*; V_{DC} = 20 *kV*; V_{AC} = 30 *kV*

Half-bridge Performance Assessment

Table 3.9: Half-bridge sub-module performance.

Functionality	Score
Supports Single Star Bridge cell (SSBC) topology	0
Supports Single Delta Bridge cell (SDBC) topology	0
Supports Double Star Bridge cell (DSBC) topology	0.25
Supports DC Fault Blocking and DC Fault Ride Through	0
Total	**0.25**

3.1.3 Benchmark Analysis for the H-bridge Sub-module

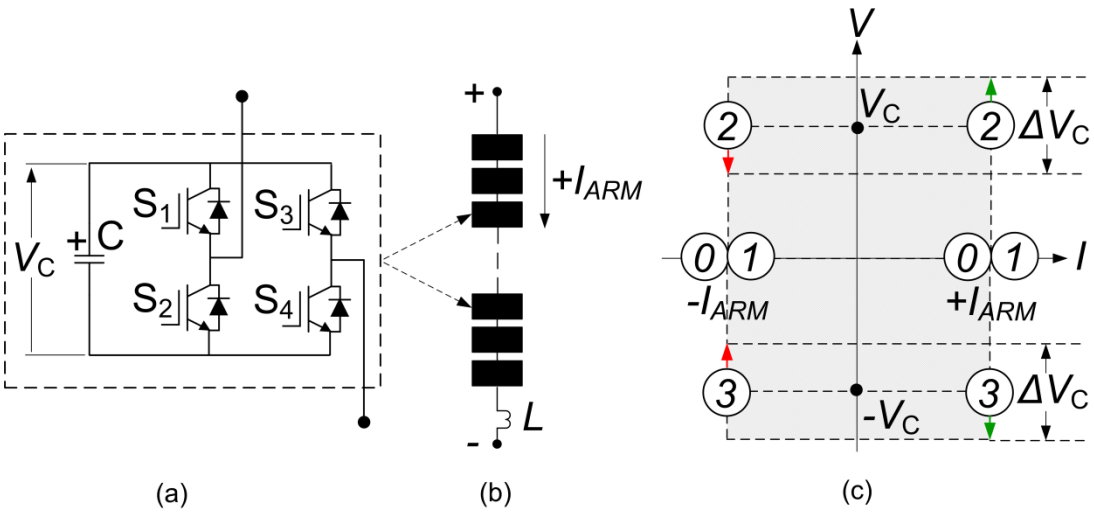

Figure 3.5: H-bridge analysis showing sub-module (a) configuration; (b) cascade arrangement for converter arm (c) *I-V* Quadrant showing operation and transition states.

The sub-module configuration for a H-bridge arrangement is shown in Figure 3.5(a) and outlines two switch modules (S_1,S_2 and S_3,S_4) both connected in parallel across the sub-module capacitor C. The sub-module positive and negative output terminals are realised between S_1_S_2 and S_3_S_4 respectively. The cascade arrangement for a converter arm is shown in Figure 3.5(b) and operation is such that each sub-module presents a voltage (*0*, V_C or $-V_C$ volts). The converter arm voltage at each switching instant is the sum of all active sub-module voltages. Figure 3.5 (c) shows how the operating states for the H-bridge sub-module distribute across an *I-V* quadrant plane occupying all four quadrants (±*I;* ±*V*). The transitional states are also shown in Table 3.10.

Table 3.10: H-bridge Sub-module Operating and Transition States.

V – output voltage; I_{ARM} – arm current direction; and *V*c - capacitor voltage showing transition (↓ = Discharging, ↑ = Charging, NC = No Change)

State	S_1	S_2	S_3	S_4	*V*	
					$+I_{ARM}$	$-I_{ARM}$
0	0	1	0	1	0	0
1	1	0	1	0	0	0
2	1	0	0	1	↑*V*c	↓*V*c
3	0	1	1	0	↓-*V*c	↑-*V*c

H-bridge Footprint Assessment

Table 3.11: Per-unitised width for H-bridge Sub-module.

Device	Quantity	Width (p.u)
Switch Module	2	0.4
Capacitor	1	0.6
GEM	1	0.2
***Total* (X_{SM}) p.u.**		**1.2**

$$Y_C = USCD \times \frac{60kV}{n_T} = 3.6cm/kV \times \frac{60kV}{10} = 21.9cm$$

$$Footpr\,\text{int} = \left[n_T.Y_{SM} + (n_T + 1)Y_C\right] \times X_{SM}.n_{ST}$$
$$= \left[10 \times 20 + (10+1)21.9\right] \times 1.2 \times 10 = 5290.8cm$$

H-bridge Cost Assessment

Table 3.12: H-bridge Sub-module Cost Assessment.

Device		**Quantity**	**Cost (£)**
Switch Module		2	17.88
Capacitor		1	8.15
Heat Sink		2	21.30
GEM	FPGA Board	1	6.00
	Gate Drive + Isolation	4	36.40
	Voltage Transducer	1	42.41
		Total	**132.14**
		Total for 60kV arm (i.e x 100)	**13214**

H-bridge Redundancy Assessment

Figure 3.4(c) outlines 4 transition states from States 2 and 3 which cause the sub-module capacitor voltage to transition (charge or discharge). This is two times more than are available in the half-bridge sub-module.

H-bridge Efficiency Assessment

$$P_{V1} = \left[0.2 \times 1.15 \times \frac{30}{3}\right] + \left[0.2 \times 0.035\left(\frac{30^2}{4} + \frac{30^2}{9}\right)\right] = 4.58W$$

$$P_{V2} = \left[0.8 \times 1.3 \times \frac{30}{3}\right] + \left[0.8 \times 0.018 \times \left(\frac{30^2}{4} + \frac{30^2}{9}\right)\right] = 15.08W$$

$$P_{COND} = 2 \times \left(4.58 + 15.08\right) = 39.32W$$

$$P_{SW} = 2 \times 150 \times (1.0 + 1.1) \times 10^{-3} = 0.63W$$

$$P_{LOSS\_60kV} = 100 \times (39.32 + 0.63) = 3995W$$

$$Efficiency\ (\%) = \left(1 - \frac{3995}{\sqrt{(20^2 + 30^2) \times \left(\frac{30^2}{4} + \frac{30^2}{9}\right)}}\right) \times 100 = 99.38\%$$

99.38% is the efficiency of one converter arm. This value is based on the fact that all sub-modules are switched in every cycle (e.g. when a passive carrier-based PWM scheme is used). One assumption made is that special consideration is not placed on the choice of transition between states. For instance, it would be desirable to transition from State 1 to State 2 or from State 0 to State 3 (refer to Table 3.10) when a positive or negative voltage is required respectively or vice versa when zero volts is required. With such consideration it is possible to reduce the switching losses by around 25%. However the switching loss is only 1.57% of the total sub-module loss thus such contribution may be plausibly neglected.

Table 3.13: H-bridge sub-module efficiency using guideline[8].

Parameter	**Value**
n_{CS} (number of switch modules per sub-module)	2
P_{V1} (3.8)	4.58 W
P_{V2} (3.9)	15.08 W
P_{COND} (3.10)	39.32 W
P_{SW} (3.11)	0.62 W
n_{SM} (number of sub-modules in 60kV arm)	100
P_{LOSS_60kV} (3.12)	3995 W
Efficiency (3.13) in %	**99.38%**

H-bridge Performance Assessment

[8] V_{CEO} = 1.15 *V*; R_{ON_T} = 0.035 Ω; V_{FO} = 1.3 *V*; R_{ON_D} = 0.018 Ω; f_{SW} = 150 *Hz;* E_{ON} = 1.0 *mJ;* E_{OFF} = 1.1 *mJ;* I_{DC} = 30 *A*; I_{AC}; 30 *A*; V_{DC} = 20 *kV*; V_{AC} = 30 *kV*

Table 3.14: H-bridge sub-module performance.

Functionality	Score
Supports Single Star Bridge cell (SSBC) topology	0.25
Supports Single Delta Bridge cell (SDBC) topology	0.25
Supports Double Star Bridge cell (DSBC) topology	0.25
Supports DC Fault Blocking and DC Fault Ride Through	0.25
Total	**1.00**

In addition to being able to support the SSBC and SDBC topologies, using an H – bridge sub-module within an MMCC in double star topology allows DC fault blocking. During a DC fault (short-circuit), the DC voltage collapses to almost zero. For a converter with a half-bridge sub-modules, a circuit is formed between the AC line and DC short-circuit through the anti-parallel diodes of the lower sub-module IGBTs in the converter phase arm (even with early fault detection and with both IGBT's switched off). The peak amplitude values typical of such fault current can be in the order of several hundred thousand amps and certainly damage any conducting devices.

For a converter built from H-bridge sub-modules it is possible to prevent the AC line from feeding into the DC short-circuit i.e block the DC fault current by recreating the "absent" DC link voltage. This is achieved by inserting the sub-module capacitance in reverse (State 3) causing the converter phase arm to present a voltage of negative amplitude (but same amplitude and polarity with the DC link voltage when referred to the DC neutral point) thereby preventing the AC side from feeding fault current into the DC short-circuit.

The use of H-bridge sub-modules in a MMC-DSBC topology has not been industrially evaluated as it does not present an economical solution over the half-bridge sub-module. In any case a sophisticated optimisation-based algorithm can be applied to actively select only the required number of sub-modules while optimizing for sub-module capacitor voltage tolerance as well as losses.

3.2 Analysis of Flying Capacitor Sub-Module Concepts

3.2.1 Sub-modules Using Flying Capacitor Half-bridge Cells

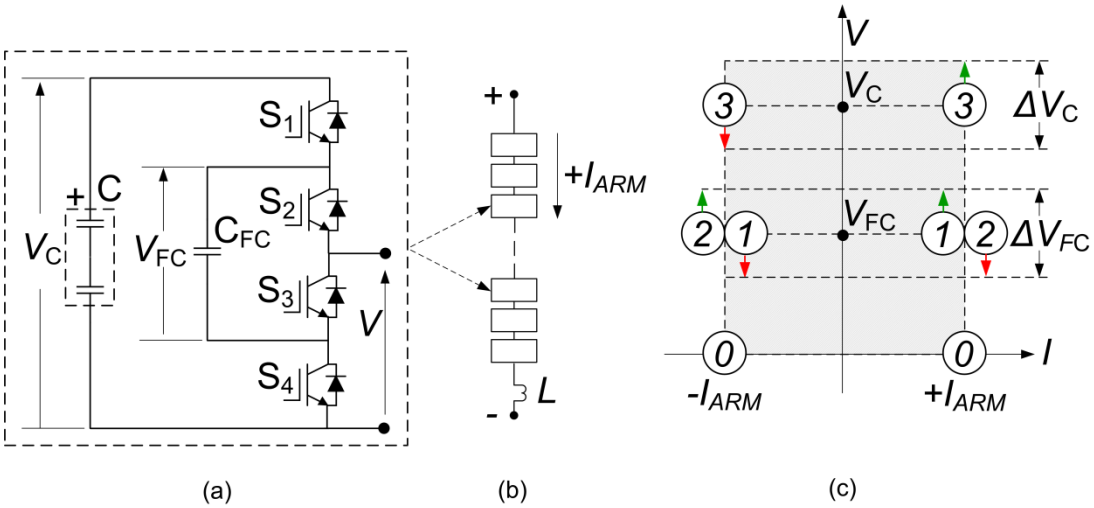

Figure 3.6: Flying Capacitor Half-bridge analysis showing sub-module (a) configuration; (b) cascade arrangement for converter arm (c) *I-V* Quadrant showing operation and transition states.

The sub-module configuration for a FC half-bridge (flying capacitor half-bridge) arrangement is shown in Figure 3.6(a) and outlines two switch modules (S_1,S_4 and S_2,S_3) connected in parallel across the sub-module capacitor C and flying capacitor C_{FC} respectively. For consistency in power rating the sub-module capacitor is shown to comprise two capacitors to match the typical/desired value of the flying capacitor voltage (i.e. $V_{FC} = 0.5V_C$). The sub-module positive and negative output terminals are realised between S_2,S_3 and at the negative terminal of the sub-module capacitor respectively.

The cascade arrangement for a converter arm is shown in Figure 3.6(b) and operation is such that each sub-module can present a voltage of: *0*, V_{FC}, V_C-V_{FC} or V_C volts (i.e typically *0*, $0.5V_C$ or V_C when careful voltage balancing is observed). Figure 3.6(c) shows how the operating states for the FC half-bridge sub-module distribute across an *I-V* quadrant plane occupying two quadrants (±*I; +V*) but with the option to synthesise 3 voltages.

The transitional states are also shown in Table 3.15.

Table 3.15: Flying Capacitor Half-bridge Sub-module States.

V – output voltage; I_{ARM} – arm current direction; and V_C, V_{FC} sub-module, flying capacitor voltage showing transition (↓ = Discharging, ↑ = Charging, NC = No Change).

State	S_1	S_2	S_3	S_4	V	
					$+I_{ARM}$	$-I_{ARM}$
0	0	0	1	1	0	0
1	0	1	0	1	$\uparrow V_{FC}$	$\downarrow V_{FC}$
2	1	0	1	0	$(\uparrow V_C - \downarrow V_{FC})$	$(\downarrow V_C - \uparrow V_{FC})$
3	1	1	0	0	$\uparrow V_C$	$\downarrow V_C$

FC Half-bridge Footprint Assessment

Table 3.16: Per-unitised width for FC Half-bridge Sub-module.

Device	Quantity	Width (p.u)
Switch Module	2	0.4
Capacitor	3	1.8
GEM	1	0.2
***Total (X_{SM})* p.u.**		**2.4**

$$Y_C = USCD \times \frac{60kV}{n_T} = 3.6cm/kV \times \frac{60kV}{5} = 43.8cm$$

$$Footpr\,\text{int} = \left[n_T.Y_{SM} + (n_T + 1)Y_C\right] \times X_{SM}.n_{ST}$$
$$= \left[5 \times 20 + (5+1)43.8\right] \times 2.4 \times 10 = 8707.2cm$$

FC Half-bridge Cost Assessment

Table 3.17: FC Half-bridge Sub-module Cost Assessment.

Device		**Quantity**	**Cost (£)**
Switch Module		2	17.88
Capacitor		3	24.45
Heat Sink		2	21.3
GEM	FPGA Board	1	6.00
	Gate Drive + Isolation	4	36.40
	Voltage Transducer	2	84.82
		Total	**190.85**
		Total for 60kV arm (i.e x 50)	**9542.5**

Half-bridge Redundancy Assessment

Figure 3.4(c) outlines 6 transition states (2 each in State 1, 2 and 3 shown in Table 3.15) which cause the sub-module capacitor and flying capacitor voltage to charge or discharge. Careful sub-module management is typically applied to maintain the capacitor voltage within a band ΔV_C as well as the capacitor voltage within the band ΔV_{FC}. This can be achieved using a passive carrier-based modulation technique with natural balancing or via an active selection algorithm.

FC Half-bridge Efficiency Assessment

$$P_{V1} = \left[0.2 \times 1.15 \times \frac{30}{3}\right] + \left[0.2 \times 0.035 \left(\frac{30^2}{4} + \frac{30^2}{9}\right)\right] = 4.58W$$

$$P_{V2} = \left[0.8 \times 1.3 \times \frac{30}{3}\right] + \left[0.8 \times 0.018 \times \left(\frac{30^2}{4} + \frac{30^2}{9}\right)\right] = 15.08W$$

$$P_{COND} = 2 \times (4.58 + 15.08) = 39.32W$$

$$P_{SW} = 2 \times 150 \times (1.0 + 1.1) \times 10^{-3} = 0.62W$$

$$P_{LOSS\_60kV} = 50 \times (32.32 + 0.62) = 1997W$$

$$Efficiency\ (\%) = \left(1 - \frac{1997}{\sqrt{(20^2 + 30^2) \times \left(\frac{30^2}{4} + \frac{30^2}{9} \right)}} \right) \times 100 = 99.69\%$$

Table 3.18: FC Half-bridge sub-module efficiency using guideline[9].

Parameter	**Value**
n_{CS} (number of switch modules per sub-module)	1
P_{V1} (3.8)	4.58 W
P_{V2} (3.9)	15.08 W
P_{COND} (3.10)	39.32 W
P_{SW} (3.11)	0.62 W
n_{SM} (number of sub-modules in 60kV arm)	50
P_{LOSS_60kV} (3.12)	1997 W
Efficiency (3.13) in %	**99.69%**

[9] V_{CEO} = 1.15 *V*; R_{ON_T} = 0.035 Ω; V_{FO} = 1.3 *V*; R_{ON_D} = 0.018 Ω; f_{SW} = 150 *Hz;* E_{ON} = 1.0 *mJ;* E_{OFF} = 1.1 *mJ;* I_{DC} = 30 *A*; I_{AC}; 30 *A*; V_{DC} = 20 *kV*; V_{AC} = 30 *kV*

FC Half-bridge Performance Assessment

Table 3.19: Half-bridge sub-module performance.

Functionality	**Score**
Supports Single Star Bridge cell (SSBC) topology	0
Supports Single Delta Bridge cell (SDBC) topology	0
Supports Double Star Bridge cell (DSBC) topology	0.25
Supports DC Fault Blocking and DC Fault Ride Through	0
Total	**0.25**

3.2.2 Sub-modules Using Flying Capacitor H-bridge Cells

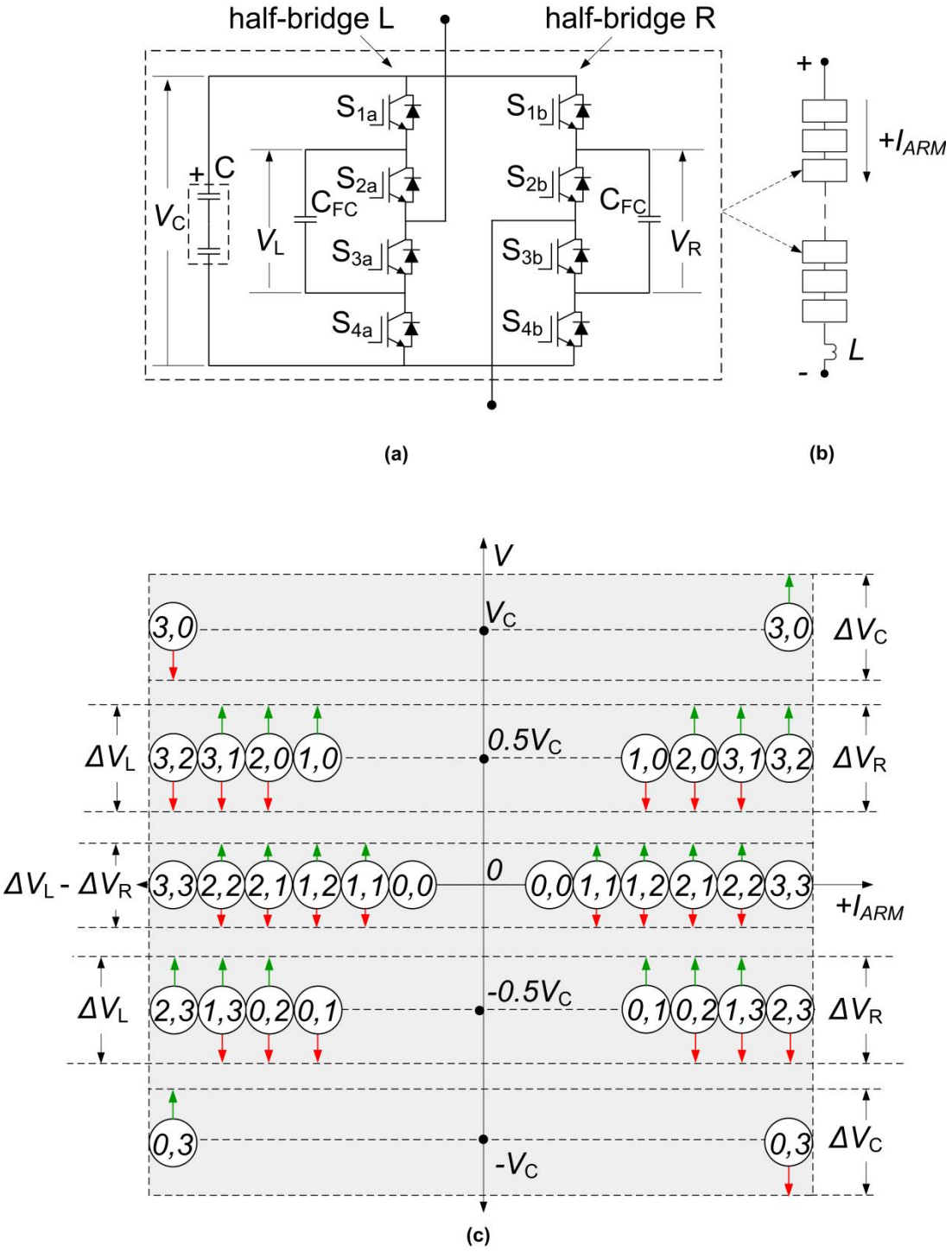

Figure 3.7: Flying Capacitor H-bridge analysis showing sub-module (a) configuration; (b) cascade arrangement for converter arm (c) *I-V* Quadrant showing operation and transition states.

The sub-module configuration for a FC H-bridge (flying capacitor H-bridge) arrangement is shown in Figure 3.7(a). This outlines the use of two flying capacitor half-bridge arrangements (half bridge L and R) thus comprising a

total of four switch pairs (S_{1a},S_{4a}; S_{2a},S_{3a}; S_{1b},S_{4b}; S_{2b},S_{3b}) one sub-module capacitor C and corresponding flying capacitors for each half-bridge C_{FC_L} and C_{FC_R}. For consistency in power rating the sub-module capacitor is shown as comprising two capacitors to match the typical/desired value of the flying capacitor voltage (i.e. $V_L = V_R = 0.5V_C$).

The cascade arrangement for a converter arm is shown in Figure 3.7(b) and operation is such that each sub-module can present an approximate voltage of: - V_C, $-0.5V_C$, 0, $0.5V_C$ or V_C volts (assuming a careful voltage balancing is applied). Figure 3.7(c) shows how the operating states for the FC half-bridge sub-module distribute across an *I-V* quadrant plane occupying all four quadrants ($\pm I; \pm V$).

The transitional states are shown in Table 3.20.

Table 3.20: Flying Capacitor H-bridge Sub-module State Combinations and Transitions.

V – output voltage; I_{ARM} – arm current direction; and V_C, V_{FC} sub-module, flying capacitor voltage showing transition (↓ = Discharging, ↑ = Charging, NC = No Change).

State L[10]	State R[11]	*V*		
		$+I_{ARM}$	$-I_{ARM}$	
0	0	0	0	
3	3	0	0	
2	2	$(\downarrow V_L - \uparrow V_R) \approx 0$	$(\uparrow V_L - \downarrow V_R) \approx 0$	Transition State Combination
2	1	$(\uparrow V_C - \downarrow V_L - \downarrow V_R) \approx 0$	$(\downarrow V_C - \uparrow V_L - \uparrow V_R) \approx 0$	
1	2	$(\downarrow V_C - \uparrow V_L - \uparrow V_R) \approx 0$	$(\uparrow V_C - \downarrow V_L - \downarrow V_R) \approx 0$	
1	1	$(\uparrow V_L - \downarrow V_R) \approx 0$	$(\downarrow V_L - \uparrow V_R) \approx 0$	
3	2	$\uparrow V_R \approx 0.5V_C$	$\downarrow V_R \approx 0.5V_C$	
2	3	$\downarrow V_L \approx -0.5V_C$	$\uparrow V_L \approx -0.5V_C$	
3	1	$(\uparrow V_C - \downarrow V_R) \approx 0.5V_C$	$(\downarrow V_C - \uparrow V_R) \approx 0.5V_C$	
1	3	$(\uparrow V_L - \downarrow V_C) \approx -0.5V_C$	$(\downarrow V_L - \uparrow V_C) \approx -0.5V_C$	
0	2	$(\uparrow V_R - \downarrow V_C) \approx -0.5V_C$	$(\downarrow V_R - \uparrow V_C) \approx -0.5V_C$	
2	0	$(\uparrow V_C - \downarrow V_L) \approx 0.5V_C$	$(\downarrow V_C - \uparrow V_L) \approx 0.5V_C$	
0	1	$\uparrow -V_R \approx -0.5V_C$	$\downarrow -V_R \approx -0.5V_C$	
1	0	$\downarrow V_L \approx 0.5V_C$	$\uparrow V_L \approx 0.5V_C$	
3	0	$\uparrow V_C$	$\downarrow V_C$	
0	3	$\downarrow -V_C$	$\uparrow -V_C$	

[10] **(S_{1a}: S_{2a}: S_{3a}: S_{4a})**: **0** = (0:0:1:1); **1** = (0:1:0:1); **2** = (1:0:1:0); **3** = (1:1:0:0).

[11] **(S_{1b}: S_{2b}: S_{3b}: S_{4b})**: **0** = (0:0:1:1); **1** = (0:1:0:1); **2** = (1:0:1:0); **3** = (1:1:0:0).

FC H-bridge Footprint Assessment

Table 3.21: Per-unitised width for FC H-bridge Sub-module.

Device	**Quantity**	**Width (p.u)**
Switch Module	4	0.8
Capacitor	4	2.4
GEM	1	0.2
***Total (X_{SM})* p.u.**		**3.4**

$$Y_C = USCD \times \frac{60kV}{n_{ST}} = 3.6cm/kV \times \frac{60kV}{5} = 43.8cm$$

$$Footpr\,\text{int} = \left[n_T.Y_{SM} + (n_T + 1)Y_C\right] \times X_{SM}.n_{ST}$$
$$= \left[5 \times 20 + (5+1)43.8\right] \times 3.4 \times 10 = 7867.6cm$$

FC Half-bridge Cost Assessment

Table 3.22: FC H-bridge Sub-module Cost Assessment.

Device		**Quantity**	**Cost (£)**
Switch Module		4	35.76
Capacitor		4	32.60
Heat Sink		4	42.60
GEM	FPGA Board	1	6.00
	Gate Drive + Isolation	8	72.80
	Voltage Transducer	3	127.23
		Total	**316.99**
		Total for 60kV arm (i.e x 50)	**15849.5**

FC H-bridge Redundancy Assessment

Figure 3.7(c) and Table 3.20 outline the transition states which cause the sub-module capacitor and flying capacitor voltage to charge or discharge. This is possible because of the 2^4 i.e. 16 state combinations for the switch modules in the left and right half-bridge legs. A total of 14 out of the 16 combinations result in sub-module and/or flying capacitor voltage transitions and when the current direction is considered a total of 28 possible voltage transitions are revealed. Careful sub-module management is typically applied to maintain the capacitor voltage within a band ΔV_C as well as the capacitor voltage within the band ΔV_L, ΔV_R. This is essential in order to maintain the typical (or approximate) sub-module output voltage during such transition when:

- $V = V_C$;
- $V \approx 0.5V_C = V_L = V_R = (V_C - V_L) = (V_C - V_R)$; and
- $V \approx 0 = (V_L - V_R) = (V_C - V_L - V_R)$.

This can be achieved using a passive carrier-based modulation technique with natural balancing or via an active selection algorithm.

FC H-bridge Efficiency Assessment

$$P_{V1} = \left[0.2 \times 1.15 \times \frac{30}{3}\right] + \left[0.2 \times 0.035\left(\frac{30^2}{4} + \frac{30^2}{9}\right)\right] = 4.58W$$

$$P_{V2} = \left[0.8 \times 1.3 \times \frac{30}{3}\right] + \left[0.8 \times 0.018 \times \left(\frac{30^2}{4} + \frac{30^2}{9}\right)\right] = 15.08W$$

$$P_{COND} = 4 \times (4.58 + 15.08) = 78.64W$$

$$P_{SW} = 4 \times 150 \times (1.0 + 1.1) \times 10^{-3} = 1.26W$$

$$P_{LOSS\_60kV} = 50 \times (78.64 + 1.26) = 3995W$$

$$Efficiency\ (\%) = \left(1 - \frac{1997}{\sqrt{\left(20^2 + 30^2\right) \times \left(\frac{30^2}{4} + \frac{30^2}{9} \right)}} \right) \times 100 = 99.39\%$$

99.39% is the efficiency of one converter arm.

Table 3.23: FC H-bridge sub-module efficiency using guideline[12].

Parameter	**Value**
n_{CS} (number of switch modules per sub-module)	1
P_{V1} (3.8)	4.58 W
P_{V2} (3.9)	15.08 W
P_{COND} (3.10)	78.64 W
P_{SW} (3.11)	1.26 W
n_{SM} (number of sub-modules in 60kV arm)	50
P_{LOSS_60kV} (3.12)	3995 W
Efficiency (3.13) in %	**99.39%**

FC H-bridge Performance Assessment

Table 3.24: FC H-bridge sub-module performance.

Functionality	**Score**
Supports Single Star Bridge cell (SSBC) topology	0.25
Supports Single Delta Bridge cell (SDBC) topology	0.25
Supports Double Star Bridge cell (DSBC) topology	0.25
Supports DC Fault Blocking and DC Fault Ride Through	0.25
Total	**1.0**

[12] V_{CEO} = 1.15 *V*; R_{ON_T} = 0.035 Ω; V_{FO} = 1.3 *V*; R_{ON_D} = 0.018 Ω; f_{SW} = 150 *Hz;* E_{ON} = 1.0 *mJ;* E_{OFF} = 1.1 *mJ;* I_{DC} = 30 *A*; I_{AC}; 30 *A*; V_{DC} = 20 *kV*; V_{AC} = 30 *kV*

3.2.3 Sub-modules Using Flying Capacitor Hybrid H-bridge Cells

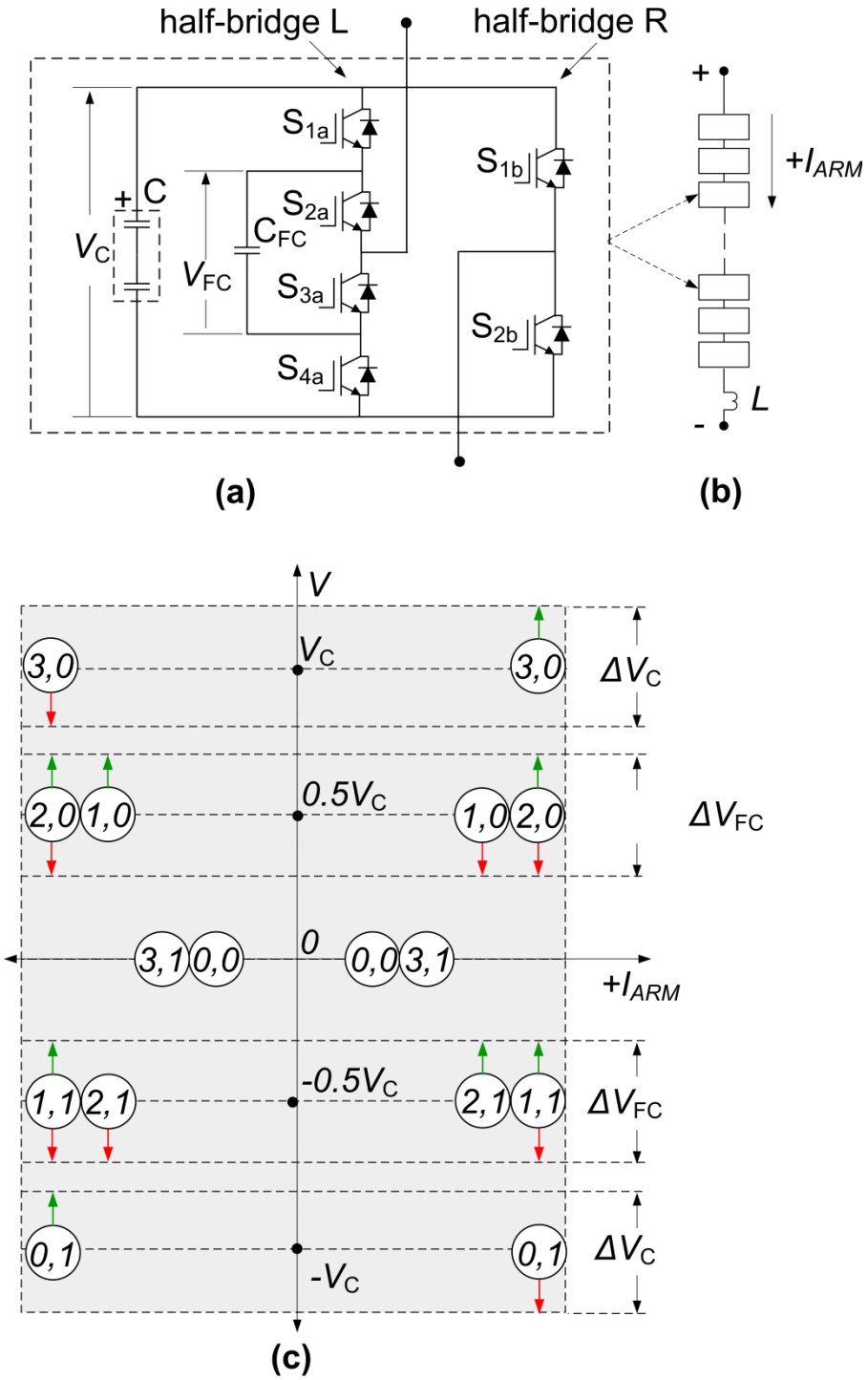

Figure 3.8: Flying Capacitor Hybrid H-bridge analysis showing sub-module (a) configuration; (b) cascade arrangement for converter arm (c) *I-V* Quadrant showing operation and transition states.

The sub-module configuration for a FC Hybrid H-bridge (flying capacitor hybrid H-bridge) arrangement is shown in Figure 3.8(a). This outlines a

hybrid combination of a flying capacitor half-bridge (half-bridge L) and a standard half-bridge (half-bridge R) thus comprising a total of three switch pairs (S_{1a},S_{4a}; S_{2a},S_{3a}; and S_{1b},S_{2b}), one sub-module capacitor C and one flying capacitor C_{FC} for the left half-bridge. For consistency in power rating the sub-module capacitor is shown to comprise two capacitors to match the typical/desired value of the flying capacitor voltage (i.e. $V_L = V_R = 0.5V_C$).

The cascade arrangement for a converter arm is shown in Figure 3.8(b) and operation is such that each sub-module can present an approximate voltage of: - V_C, $-0.5V_C$, 0, $0.5V_C$ or V_C volts (when careful voltage balancing is applied). Figure 3.8(c) shows how the operating states for the FC Hybrid H-bridge sub-module distribute across an *I-V* quadrant plane occupying all four quadrants ($\pm I; \pm V$).

The operating states and resulting transitions are shown in Table 3.25.

Table 3.25: Flying Capacitor Hybrid H-bridge Sub-module State Combinations and Transitions.

V – output voltage; I_{ARM} – arm current direction; and V_C, V_{FC} sub-module, flying capacitor voltage showing transition (↓ = Discharging, ↑ = Charging, NC = No Change).

State L[13]	State R[14]	V		
		$+I_{ARM}$	$-I_{ARM}$	
0	0	0	0	
3	1	0	0	
2	1	↓V_{FC} ≈ $-0.5V_C$	↑V_{FC} ≈ $-0.5V_C$	Transition States
1	1	(↑V_{FC} - ↓V_C) ≈ $-0.5V_C$	(↓V_{FC} - ↑V_C) ≈ $-0.5V_C$	
2	0	(↑V_C - ↓V_{FC}) ≈ $0.5V_C$	(↓V_C - ↑V_{FC}) ≈ $0.5V_C$	
1	0	↓V_{FC} ≈ $0.5V_C$	↑V_{FC} ≈ $0.5V_C$	
3	0	↑V_C	↓V_C	
0	1	↓$-V_C$	↑$-V_C$	

FC Hybrid H-bridge Footprint Assessment

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[13] **(S_{1a}: S_{2a}: S_{3a}: S_{4a})**: **0** = (0:0:1:1); **1** = (0:1:0:1); **2** = (1:0:1:0); **3** = (1:1:0:0).

[14] **(S_{1b}: S_{2b})**: **0** = (0:1); **1** = (1:0).

Table 3.26: Per-unitised width for FC Hybrid H-bridge Sub-module.

Device	**Quantity**	**Width (p.u)**
Switch Module	3	0.6
Capacitor	3	1.8
GEM	1	0.2
***Total (X_{SM})* p.u.**		**2.6**

$$Y_C = USCD \times \frac{60kV}{n_T} = 3.6cm/kV \times \frac{60kV}{5} = 43.8cm$$

$$Footpr\,\text{int} = \left[n_T.Y_{SM} + (n_T + 1)Y_C\right] \times X_{SM}.n_{ST}$$
$$= \left[5 \times 20 + (5+1)43.8\right] \times 2.6 \times 10 = 9432.8cm$$

FC Hybrid H-bridge Cost Assessment

Table 3.27: FC H-bridge Sub-module Cost Assessment.

Device		**Quantity**	**Cost (£)**
Switch Module		3	26.82
Capacitor		3	24.45
Heat Sink		3	31.95
GEM	FPGA Board	1	6.00
	Gate Drive + Isolation	6	54.6
	Voltage Transducer	2	84.82
		Total	**228.64**
		Total for 60kV arm (i.e x 50)	**11432**

FC Hybrid H-bridge Redundancy Assessment

Figure 3.8(c) and Table 3.25 outline the transition states which cause the sub-module capacitor and flying capacitor voltage to charge or discharge. There are 2^3 i.e. 8 state combinations for the switch modules in the left and right half-bridge legs. 6 out of the 8 combinations result in sub-module and/or flying capacitor voltage transitions and when the current direction is considered a total of 12 possible voltage transitions are available.

FC Hybrid H-bridge Efficiency Assessment

$$P_{V1} = \left[0.2 \times 1.15 \times \frac{30}{3}\right] + \left[0.2 \times 0.035 \left(\frac{30^2}{4} + \frac{30^2}{9}\right)\right] = 4.58W$$

$$P_{V2} = \left[0.8 \times 1.3 \times \frac{30}{3}\right] + \left[0.8 \times 0.018 \times \left(\frac{30^2}{4} + \frac{30^2}{9}\right)\right] = 15.08W$$

$$P_{COND} = 3 \times (4.58 + 15.08) = 58.98W$$

$$P_{SW} = 3 \times 150 \times (1.0 + 1.1) \times 10^{-3} = 0.95W$$

$$P_{LOSS\_60kV} = 50 \times (58.98 + 0.95) = 2996.5W$$

$$Efficiency\ (\%) = \left(1 - \frac{2996.5}{\sqrt{(20^2 + 30^2) \times \left(\frac{30^2}{4} + \frac{30^2}{9}\right)}}\right) \times 100 = 99.54\%$$

99.54% is the efficiency of one converter arm.

Table 3.28: FC H-bridge sub-module efficiency using guideline[15].

Parameter	Value
n_{CS} (number of switch modules per sub-module)	1
P_{V1} (3.8)	4.58 W
P_{V2} (3.9)	15.08 W
P_{COND} (3.10)	58.98 W
P_{SW} (3.11)	0.95 W
n_{SM} (number of sub-modules in 60kV arm)	50
P_{LOSS_60kV} (3.12)	2996.5 W
Efficiency (3.13) in %	**99.54%**

FC Hybrid H-bridge Performance Assessment

Table 3.29: FC H-bridge sub-module performance.

Functionality	Score
Supports Single Star Bridge cell (SSBC) topology	0.25
Supports Single Delta Bridge cell (SDBC) topology	0.25
Supports Double Star Bridge cell (DSBC) topology	0.25
Supports DC Fault Blocking and DC Fault Ride Through	0.25
Total	**1.0**

[15] V_{CEO} = 1.15 *V*; R_{ON_T} = 0.035 Ω; V_{FO} = 1.3 *V*; R_{ON_D} = 0.018 Ω; f_{SW} = 150 *Hz;* E_{ON} = 1.0 *mJ;* E_{OFF} = 1.1 *mJ;* I_{DC} = 30 *A*; I_{AC}; 30 *A*; V_{DC} = 20 *kV*; V_{AC} = 30 *kV*

3.2.4 Discussion and Comparison of Sub-module Configurations

Table 3.30: Comparison of the different sub-module concepts based on requirements for a 60 *k*V converter arm.

Sub-module Assessment	Half-bridge	H-bridge	FC Half-bridge	FC H-bridge	FC Hybrid
Footprint (cm)	4409 ✓	5291	8707	12335	9433
Cost (£)	9435 ✓	13214	9543	15849	11432
Redundancy (states)	2	4	6	28 ✓	12
Arm Efficiency (%)	99.69 ✓	99.38	99.69 ✓	99.39	99.54
Performance (Rank)	0.25	1.00 ✓	0.25	1.00 ✓	1.00 ✓

Table 3.30 summarises the assessment performed on the different sub-module concepts based on requirements for building a 60 *k*V converter arm.

The following facts can be extracted from the results summarised above.

- The half-bridge sub-module concept presents the lowest per-unitised footprint, cost and losses, making this concept the choice for implementation in HVDC applications which require such attributes, especially since scaling is usually in the order of a few hundred units (e.g. up to 600 *k*V). However, the small number of redundancy states available and performance/functionality supported limits the scope of application of this concept. For instance, in a STATCOM application the converter arm is expected to synthesise both positive and negative voltages, while in a HVDC application DC fault blocking is provided by reversing the voltage polarity of a converter arm thus "blocking" the fault current from flowing through. Both functionality events are not supported by a half-bridge submodule.
- The H-bridge sub-module concept may be implemented if such functionality events are compulsory in an application, but at the expense of 20% more per-unitised footprint and 40% extra cost (as well as double the converter losses). However the fact that only two "extra" redundancy states are available makes it difficult to justify the extra expense for this sub-module concept unless specific changes are made at the topology level (e.g. as in the Series Bridge and Alternate Arm converters) which significantly reduces the sub-module count.

- The FC half-bridge sub-module has the same performance limits as the half-bridge sub-module but with a higher footprint requirement and only 4 more redundancy states making further assessment of this concept less interesting.
- The flying capacitor H-bridge sub-module concept presents about $2^1/_2$ times larger footprint and is 70% more expensive than the half-bridge concept. These are not attractive attributes in an application with high sub-module scaling. However, the FC H-bridge concept is very attractive in an application with "moderate[16]" scaling. There are 26 more redundant states and the ability to reverse voltage allows higher performance with support for more topology structures as well as fault blocking.
- Preference between the FC H-bridge and FC-Hybrid concepts mainly depends on application requirements. For instance in a medium voltage application where efficiency/cost/footprint have the highest priority (e.g Battery Energy Storage Systems) the FC Hybrid concept is more attractive than the FC H-bridge but vice versa for an application where transient performance of the converter has a higher priority (e.g STATCOM, active power filters).

In this assessment the same types of components (capacitors, switch modules, etc.) are used for implementing each sub-module configuration. The assessment is conducted in this manner for consistency, but the likelihood in practice is that components would be specifically selected to implement the different sub-module concepts. For instance, one capacitor (instead of two) with the appropriate rating (V_C) would be implemented as the sub-module capacitor in the flying capacitor based concepts. This would result in lower cost and footprint values per sub-module. Furthermore, the choice of a modulation strategy that properly utilises the redundant states, especially in the FC H-bridge concept allows flying capacitors with lower capacitances to be used, thus resulting in lower footprint and cost values per sub-module.

[16] Moderate scaling in this context, refers to medium voltage applications as specified in IEEE 1623-2004 (1 to 100 *k*V). This is typical for FACTs applications (STATCOMS, Active power filters, e.t.c).

3.3 Summary

This chapter has evaluated and compared the five basic candidate topologies as sub-modules for a modular multilevel converter. These are half-bridge, H-bridge, FC half-bridge, FC H-bridge and FC hybrid. Criteria studied were footprint, cost, redundancy, efficiency and performance.

It has been shown that amongst all candidates topologies, the half-bridge sub-module offers lowest footprint and cost and highest efficiency, hence it has been preferred currently by various companies as the building block for HVDC converters. The FC H-bridge, on the other hand, has the highest footprint and cost, however it has the highest number of redundant switching states, hence offering more degrees of freedom in control at the sub-module level making it flexible for converters requiring high performance dynamic control. This topology is also versatile, able to work for all functions involving either unidirectional or bidirectional current flow, and can support fault blocking and DC fault ride-through. These features make it a good candidate for applications with "moderate[17]" scaling. Comparing the half-bridge, H-bridge circuits and FC H-bridge has not been investigated so extensively, hence, setting the theme of this research.

[17] Moderate scaling in this context, refers to medium voltage applications as specified in IEEE 1623-2004 (1 to 100 *k*V). This is typical for FACTs applications (STATCOMS, Active power filters, e.t.c).

Chapter 4
MMFC Converter Control and Modulation Studies

Following the choice of the FC H-bridge topology for the sub-modules of the modular multilevel converter, this chapter investigates a suite of techniques for the modulation of a single star MMFCC converter. Extensive discussions cover the Selective Harmonic Elimination Technique and various sine-carrier based modulation schemes. Their basic principles, and computational procedures and features, are explored in detail.

Based on the above a novel “Overlapping Hexagon Space Vector Modulation” (OH-SVM) technique has been developed by the author as an adaptation of the multilevel space vector pulse width modulation technique.

This method is shown to offer a number of favourable features for the modulation control of the MMFCC, including ease of duty cycle computation and capacitor voltage balancing. The rationale of the technique, and computational algorithms, are discussed in detail. For convenience the converter setup adopted for the modulation studies is shown in Figure 4.1

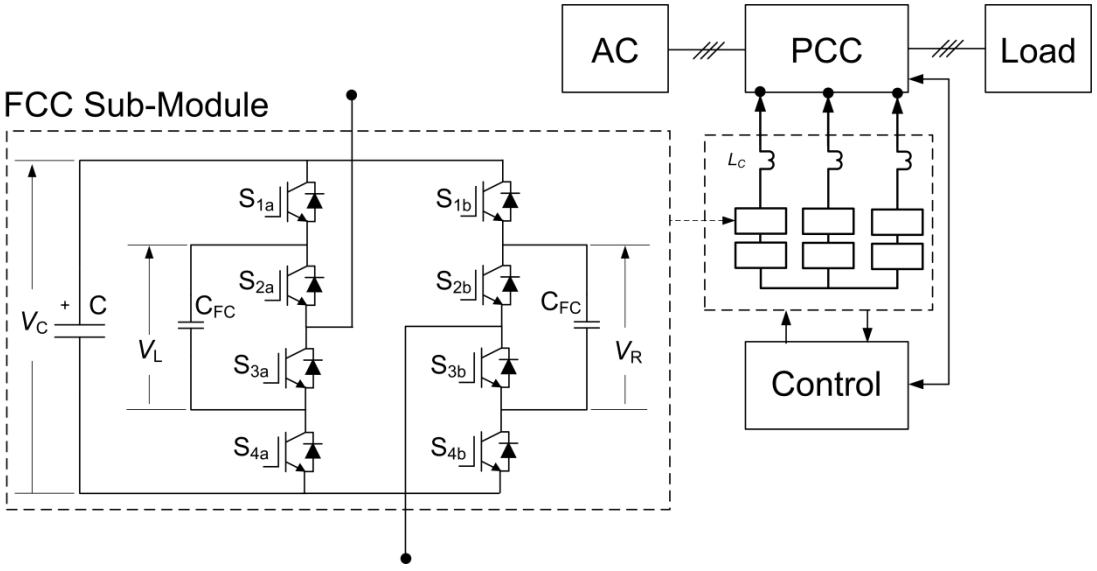


Figure 4.1: MMFCC converter and sub-module setup for modulation studies.

An outline of the three-level Flying capacitor H-bridge sub-module adopted for the modulation studies is shown in Figure 4.1 and two such sub-modules are represented to form each converter phase arm. The sub-module capacitor is denoted as *C* and the flying capacitors as C_{FC}.

Simulation results are provided demonstrating the good harmonic performance and flexibility in coping with dynamic voltage variations. Simulation setup and associated scripts are outlined in Appendix D.

A comparison of all the modulation schemes presented is provided in a summary section using performance metrics, such as capacitor voltage variation, total harmonic distortion, dynamic response and computational complexity.

4.1 Converter Modulation Techniques

The primary objective of any converter modulation technique, for any topology, is to convert the instantaneous reference voltage, i.e the value demanded by the desired sinusoidal output waveform, into switching signals. Classic PWM modulation techniques widely covered in the literature include sine-triangle PWM are implemented easily using analogue or digital electronic circuits. Another well-used scheme for low to medium power drives is current-hysteresis or tolerance-band PWM, chosen mainly for its fast dynamic response. Space Vector Modulation (SVM) is an attractive technique that uses a combination of space phasor and vector reference frames which render benefits such as ease of digital implementation with the hexagon symmetry offering up to 1.15 p.u of extra modulation depth. The staircase or Selective Harmonics Elimination (SHE) scheme is also well-known and attractive for medium to high power applications due to its low switching frequency. Such classic modulation techniques are well proven but limited when extension to higher levels, i.e for modular multilevel or cascaded converter applications, is considered.

Some extensions to the classic modulation techniques are available to cater for conventional multilevel topologies and are covered in the literature [31, 80-92]. Techniques such as the Phase-Shift PWM, Amplitude-Disposition (or Phase Disposition) PWM, Multilevel SVM, Multilevel hysteresis PWM and Multi-Level selective harmonic elimination PWM are some of the available extensions. This suite of “extended” PWM techniques normally aim to operate at low per-device switching frequency, while retaining a satisfactory output harmonic spectrum. Such PWM techniques are limited when applied to modulation of converter phase arms with several hundred sub-modules. To tackle such applications, modulation concepts based on active select and

sort optimisation have become a growing research interest. A representative example is also presented.

To improve readability the following nomenclature is used to describe these modulation studies:

(a) Average converter switching frequency (f_S). This is a determining factor of the converter voltage harmonic quality. The converter switching frequency is derived as the number of notches/per cycle multiplied by the fundamental frequency. A notch is defined as a step change in the voltage waveform caused by a change in sub-module switching state which results in an increase or decrease in the phase arm voltage.

(b) Sub-module switch frequency (f_{SS}). This is the major factor affecting converter switching losses. The sub-module switch frequency is defined as the number of switching transitions for each sub-module complementary switch pair within one fundamental cycle. A transition is a change of a device operating state from 0 (blocking) to 1 (conducting). Preferably all devices within the converter phase arm should have comparable f_{SS} values but this varies depending on the modulation scheme implemented.

(c) Modulation amplitude index or amplitude modulation index (m_A). This is a control variable used to adjust the converter phase limb peak voltage to match a demand (reference) voltage value.

(d) Sub-module capacitor voltage drift. This occurs when the time spent charging the sub-module capacitor is continuously not equal to time spent discharging, causing the voltage to charge (or discharge) continuously thus drifting away from the typical value over after a number of fundamental cycles. This issue is typical with modulation techniques that utilise open-loop balancing and further escalated when the current being synthesised is not symmetrical.

(e) Sub-module capacitor voltage deviation. This is a voltage variation experienced due to the sub-module switching actions and can be measured over a fundamental period. This is mainly defined by the sub-module capacitance value, however the modulation scheme plays a part in this voltage variation due to the mathematical relationship between the capacitance and instantaneous current at the instant of switching.

The difference between the terms capacitor voltage deviation and drift is shown in Figure 4.2.

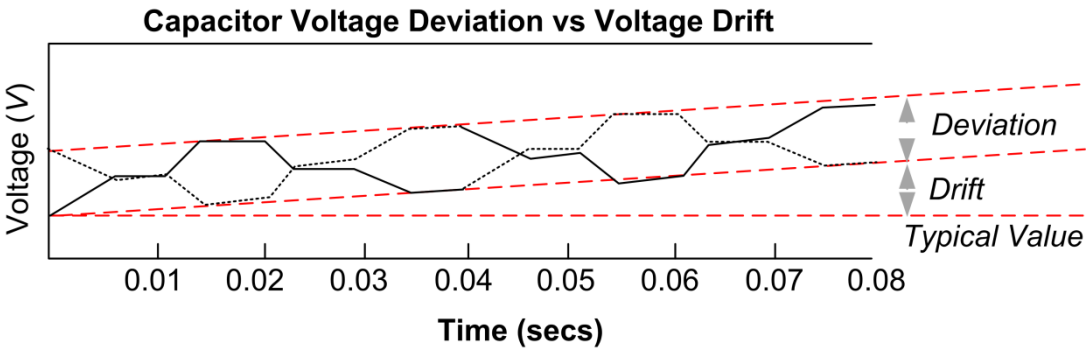


Figure 4.2: Capacitor Voltage Variation in one Module of MMFCC with SHE modulation (no capacitor balancing).

In practice, the sub-module switching frequency (f_{SS}) is used to estimate the the charge/discharge cycle of the sub-module capacitor as well as for the flying capacitors using the number of sub-module switching transitions[1]. This fall out of the scope of this research work.

Values of other practical parameters of an MMFCC converter, as used in the simulation study of the modulation techniques, are shown in Table 4.1.

Table 4.1: Parameters for MMFCC Modulation Simulator

Load Side Parameters		
Parameter		**Value**
V_{ph} peak across load @ 1 p.u m_a	V_s	1 kV
Three Phase Load (Star Connection)	L_S R_S	12mH 57.6Ω
Converter Side Parameters		
Sub-module capacitor (C) voltage set-point	V_C	500 V
Module Flying Capacitors (Capacitance)	C	1mF

General objectives for each modulation concept investigated and for each converter phase arm include:

[1] A sub-module transition is a change from one state to another. The states are: State 2 (Output = V_C); State 0 (Output = 0); and State 1 (Output = V_{FC}). V_C is the capacitor voltage; V_{FC} = flying capacitor voltage.

1. Provision of 16 gate control signals to each submodule (as 8 complementary pairs, with 4 pairs in each sub-module.)
2. Maintaining the pair of sub-module flying capacitor voltages (V_L, V_R) within acceptable tolerance values of half the defined sub-module capacitor voltage set-point value (250 V).

In practical systems, other objectives can include protection functionalities e.g. local co-ordination of: device desaturation, sub-module over-current and over-voltage assist; etc. Such are not the focus of the underlying investigations.

4.1.1 Modulation using Selective Harmonic Elimination

The selective harmonic elimination PWM technique is an attractive converter modulation technique for circuits where low switching frequency (i.e low loss) is a priority. The technique relies on a set of switching times carefully calculated to control the converter output voltage to a desired magnitude while supressing a selected number of harmonics. The amplitude of harmonic components tend to fall in inverse proportion to frequency, thus lower order harmonic components constitute more disturbance in a system. Hence regular practice is to attempt to suppress the lower order harmonic components.

For an MMFCC topology, the switching actions needed to control the fundamental and suppress selected harmonics are implemented across the series-connected modules resulting in different voltage levels. This realises a staircase-shaped converter phase arm voltage, hence the common term for this extension is “level shifting” SHE [84, 86, 93]. Such adaptation allows the level shifting SHE to provide modulation of the MMFCC at a device switching frequency close to the fundamental while retaining good harmonic quality.

A basic level shifting SHE principle applied to an MMFCC converter phase arm comprising two FCC sub-modules is shown in Figure 4.3. In the case illustrated, the sub-module switch frequency, f_{SS}, is equal to the AC fundamental frequency as each device switches once during the cycle. In the positive half cycle, four distinct voltage steps ($0.5V_C$; $1.0V_C$; $1.5V_C$; and $2.0V_C$) are activated at four firing computed angles (α_1, α_2, α_3, α_4). Additionally the quarter (and half) wave symmetry of the target reference waveform allows an adaptation of the already computed firing angles for:

- deactivation of the voltage steps during the second quarter of the positive half cycle using angles $\pi/2+\alpha_4$, $\pi/2+\alpha_3$, $\pi/2+\alpha_2$, $\pi/2+\alpha_1$.
- activation of the voltage steps during the first quarter of the negative half cycle using angles $\pi+\alpha_1$, $\pi+\alpha_2$, $\pi+\alpha_3$, $\pi+\alpha_4$; and
- deactivation of the voltage steps during the second quarter of the negative half cycle using angles $3\pi/2+\alpha_4$, $3\pi/2+\alpha_3$, $3\pi/2+\alpha_2$, $3\pi/2+\alpha_1$.

A total of 8 voltage steps is present in the waveform synthesized using level-shifted SHE. The steps are more obvious when the sub-module switching signals are observed and imply a converter switching frequency of 8 times the AC fundamental frequency (i.e f_S = 400Hz for a 50Hz AC signal).

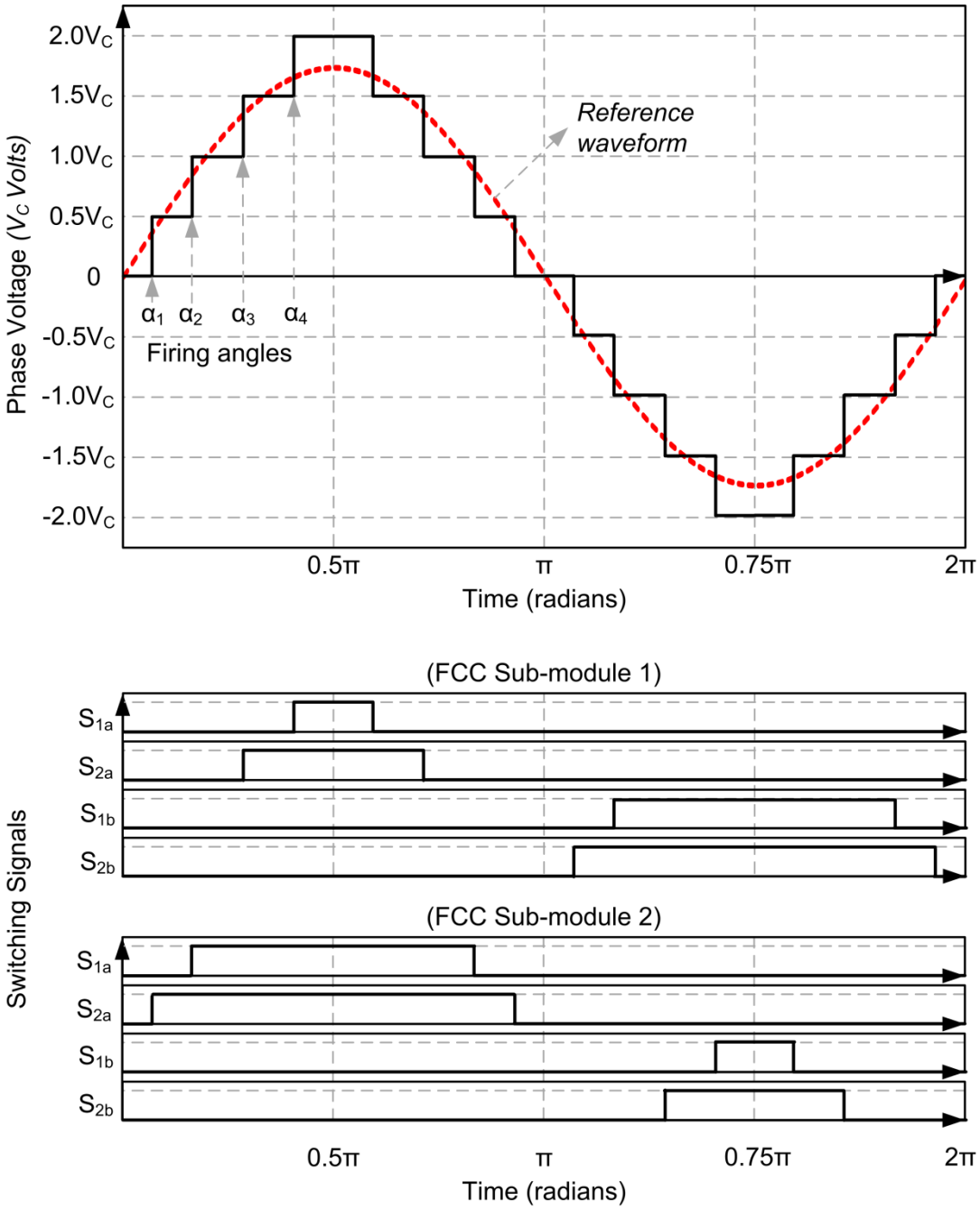


Figure 4.3: Principle of Level-shifted Selective Harmonic Suppression applied to the MMFCC phase arm .

The implementation in Figure 4.3 is a possible example that primarily demonstrates the multilevel SHE modulation principle for the MMFCC. In reality while applying the switching signals the following must be considered:

- Equal sub-module utilisation within each converter phase arm.
- Symmetrical switching utilisation between the positive and negative half cycle (at least over a plurality of fundamental cycles).

Such considerations are important to mitigate the issue of sub-module capacitor and flying capacitor voltage drift and minimise deviation.

The multilevel SHE algorithm for the MMFCC involves two key stages: angle computation and switching signal generation.

4.1.1.1 Angle Computation using Newton Raphson iterative method

It may be preferred that the four switching angles computed for the case in Figure 4.3 should suppress the fifth, seventh and eleventh odd harmonics while controlling the AC fundamental magnitude to the desired m_a value. All third-order harmonic components and their multiples (triplen harmonics) cancel out in the line-line waveform because of the three-phase converter arrangement. Based on this, the triplen components are not considered for suppression during the computation of firing angles. The four switching angles required are computed by solving the following four non-linear simultaneous equations in (4.1).

$$\begin{aligned}
f_1(\alpha_1,\alpha_2,\alpha_3,\alpha_4) &= \cos(\alpha_1)+\cos(\alpha_2)+\cos(\alpha_3)+\cos(\alpha_4)-2.m_a\frac{\pi}{2}=0\\
f_2(\alpha_1,\alpha_2,\alpha_3,\alpha_4) &= \cos(5.\alpha_1)+\cos(5.\alpha_2)+\cos(5.\alpha_3)+\cos(5.\alpha_4)=0\\
f_3(\alpha_1,\alpha_2,\alpha_3,\alpha_4) &= \cos(7.\alpha_1)+\cos(7.\alpha_2)+\cos(7.\alpha_3)+\cos(7.\alpha_4)=0\\
f_4(\alpha_1,\alpha_2,\alpha_3,\alpha_4) &= \cos(11.\alpha_1)+\cos(11.\alpha_2)+\cos(11.\alpha_3)+\cos(11.\alpha_4)=0
\end{aligned} \qquad \textbf{4.1}$$

This can be expressed using the matrix expression as

$$F(X)=\begin{bmatrix} f_1(\alpha_1,\alpha_2,\alpha_3,\alpha_4)\\ f_2(\alpha_1,\alpha_2,\alpha_3,\alpha_4)\\ f_3(\alpha_1,\alpha_2,\alpha_3,\alpha_4)\\ f_4(\alpha_1,\alpha_2,\alpha_3,\alpha_4)\end{bmatrix}=\begin{bmatrix} f_1(X)\\ f_2(X)\\ f_3(X)\\ f_4(X)\end{bmatrix} \qquad \textbf{4.2}$$

where $X=\begin{bmatrix}\alpha_1\\ \alpha_2\\ \alpha_3\\ \alpha_4\end{bmatrix}$;

and the solution to the expression in (4.2) is the basis for the computation of the firing angles required for SHE converter co-ordination and is typically solved using:

- An iterative numerical algorithm. This is commonly used and constitutes algorithms such as the Newton-Raphson and the Secant Iterative methods.
- A Genetic – Optimization algorithm. This is normally implemented to resolve more dense non-linear expressions (i.e with more variables). Some known methods within this class are the Trust Region Dogleg, Trust Region Reflective or Levenberg-Marquardt methods [94-96].

The author has chosen to implement an iterative numerical algorithm. Specifically the Newton Raphson iterative method was implemented for the computation of four firing angles.

The Newton-Raphson method involves replacing the expression in (4.2) by the first two terms of their Taylor series [97-99]. Thus the linear expression for *F*(x) becomes

$$F(X) = F(X_0) + {\partial F(X)}/{\partial X}\Big|_{X=X_0}(X - X_0); \qquad \textbf{4.3}$$

${\partial F(X)}/{\partial X}$ is a matrix with partial derivative elements otherwise known as the Jacobian, *J*, matrix. Its elements are expanded for the expression in (4.3) as shown in (4.4):

$$J = \frac{\partial(f_1, f_2, f_3, f_4)}{\partial(\alpha_1, \alpha_2, \alpha_3, \alpha_4)} = \begin{bmatrix} {\partial f_1}/{\partial \alpha_1} & {\partial f_1}/{\partial \alpha_2} & {\partial f_1}/{\partial \alpha_3} & {\partial f_1}/{\partial \alpha_4} \\ {\partial f_2}/{\partial \alpha_1} & {\partial f_2}/{\partial \alpha_2} & {\partial f_2}/{\partial \alpha_3} & {\partial f_2}/{\partial \alpha_4} \\ {\partial f_3}/{\partial \alpha_1} & {\partial f_3}/{\partial \alpha_2} & {\partial f_3}/{\partial \alpha_3} & {\partial f_3}/{\partial \alpha_4} \\ {\partial f_4}/{\partial \alpha_1} & {\partial f_4}/{\partial \alpha_2} & {\partial f_4}/{\partial \alpha_3} & {\partial f_4}/{\partial \alpha_4} \end{bmatrix} \qquad \textbf{4.4}$$

If the vector X_0 (α_1, α_2, α_3, α_4) represents the initial estimate of the solution for the firing angles, successive estimates of the firing angles can be expressed as

$$X_{n+1}(\alpha_1, \alpha_2, \alpha_3, \alpha_4) = X_n(\alpha_1, \alpha_2, \alpha_3, \alpha_4) - \frac{F(X_n(\alpha_1, \alpha_2, \alpha_3, \alpha_4))}{J} \qquad \textbf{4.5}$$

The numerical iteration loops continuously until either disrupted or the solution convergence criterion condition described by (4.6) is satisfied.

$$X_{n+1}(\alpha_1, \alpha_2, \alpha_3, \alpha_4) - X_n(\alpha_1, \alpha_2, \alpha_3, \alpha_4) = \Delta X_n(\alpha_1, \alpha_2, \alpha_3, \alpha_4) \leq \varepsilon \qquad \textbf{4.6}$$

where ε is a predefined error tolerance value used to terminate the iteration.

Appendix D.2 outlines the Matlab code for solving the expression in (4.2) using the Newton-Raphson method. Results obtained from the code in Appendix (B.1) are:

m_A = 0.8 are α_1=0.4311, α_2=0.7947, α_3=0.9956, α_4=1.2023

The main issue with using the Newton-Raphson iterative method for solving the SHE-PWM equations is a requirement to define all the Jacobian partial-derivative functions ($\partial f_i / \partial \alpha_j$ where i, j = 1, 2, 3, 4). Extending this technique to control more angles is tedious. For instance to solve for 12 firing angles a total of 144 Jacobian elements must first be obtained through derivation. Using the Secant Method (Appendix D.3) is less tedious as the differential elements in the Jacobian matrix are substituted with finite differential variables, however with some compromise of accuracy.

It is well known that the solution of non-linear equation presents convergence issues. Providing adequate initial values increases the possibility of convergence but this means one must already be aware of the solution being sought after. This poses a limitation in any SHE algorithm practically implemented, where it is more difficult to estimate such solutions.

Firing angles computed for the MMFCC converter phase arm for m_a value in the range from 0.1 to 1.0 are shown in Table 4.2 and must meet the range criteria shown in (4.7).

Only firing angles that satisfy the criteria may be applied to control the sub-module switches. In Table 4.2 the firing angles that do not meet this criteria are “greyed out”. For instance, when m_A = 0.1, only the first two alpha angles computed (0.1726, 1.4963) result in device activation. The other two firing angles (1.7621, 2.1595) are clearly out of bounds based on (4.7) and hence are not used for switch activation. During such a case the MMFCC phase arm voltage waveform will comprise only three distinct levels (0, 0.5V_C and V_C).

Table 4.2: Firing angles computed for different modulation indices.

m_A	α_1 (rad)	α_2 (rad)	α_3 (rad)	α_4 (rad)
0.1	0.1726	1.4963	1.7621	2.1595
0.2	0.2201	1.2203	1.7787	2.0767
0.3	0.2782	1.3756	1.6764	1.6764
0.4	0.3418	1.0919	1.4999	1.7898
0.5	0.3815	0.9758	1.2951	1.7620
0.6	0.3857	0.8760	1.1894	1.6249
0.7	0.6304	0.8356	1.0659	1.3316
0.8	0.4311	0.7947	0.9955	1.2023
0.9	0.6036	0.2172	0.8519	1.2020
1.0	0.1748	0.3865	0.7113	1.0781

$$0 \le (\alpha_1, \alpha_2, \alpha_3, \alpha_4) \le \frac{\pi}{2} \qquad \textbf{4.7}$$

$$\frac{\pi}{2} \approx (1.5708)$$

4.1.1.2 Switching signal generation (Sub-module switch activation)

To derive the switching signals for the two sub-module switches in each converter phase arm the computed firing angles alongside the converter voltage phase angle (*ωt*) are considered. Typical implementation involves the use of a finite state machine that considers the state of the converter voltage phase angle as it cycles between 0 and 2π. This enables the firing angles to be recomputed and applied every quarter cycle thus achieving a more dynamic converter response to changes in m_A. However, a "real-time" angle resolver is rarely used in practice as convergence of numerical iteration process is uncertain. Rather a look-up table similar to Table 4.2 is normally populated with pre-computed values. This provides "best fit" firing angles to a modulation controller in order to match demanded modulation index values.

Figure 4.4: Activation of Switches from Firing Angles

The firing angles generated from an angle resolver (or look-up table as discussed) are fed into a Finite state machine together with the rotational angle (ωt). The Finite state machine generates the converter limb states (0, 1, 2, 3 or 4) which are fed into a module selector that determines the states (0, 1 or 2) to be activated in each module. As the FCC modules are in full bridge arrangement, the module leg activation sub-system decodes the states into module-leg states. Finally the module-leg states are submitted to a switch activation sub-system to generate the switching states for the sub-module switches in each converter phase. Figure 4.5 outlines a sample flowchart to complement the discussions for Figure 4.4.

Results captured for the MMFCC under SHE modulation are shown in Figure 4.6 - Figure 4.9 for m_A = 0.8. In Figure 4.6, the waveforms shown are for Phase-A of the converter except for the line-line voltage which describes the voltage between Phases A and B.

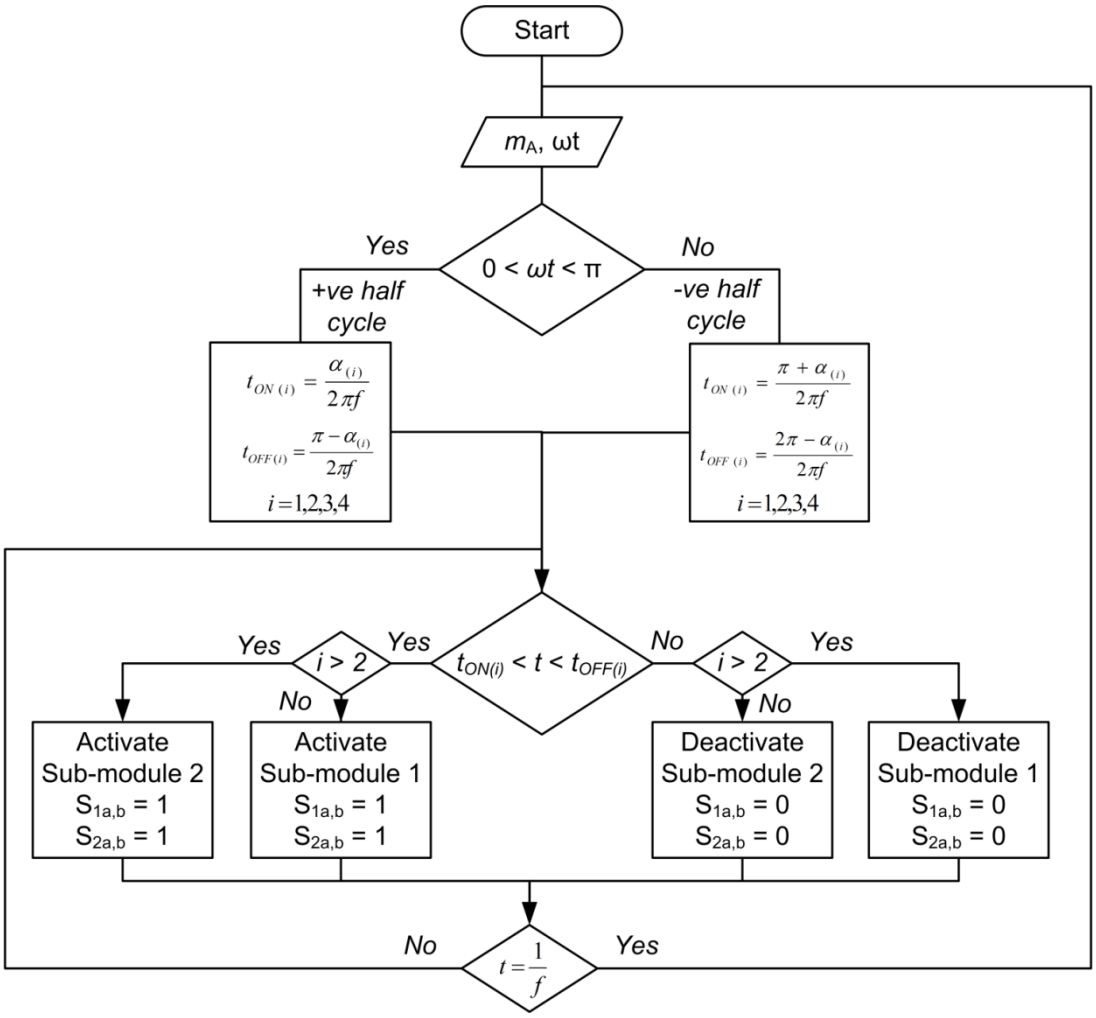


Figure 4.5: Flowchart for generating switching signals and activating the MMFCC sub-modules using multilevel SHE-PWM.

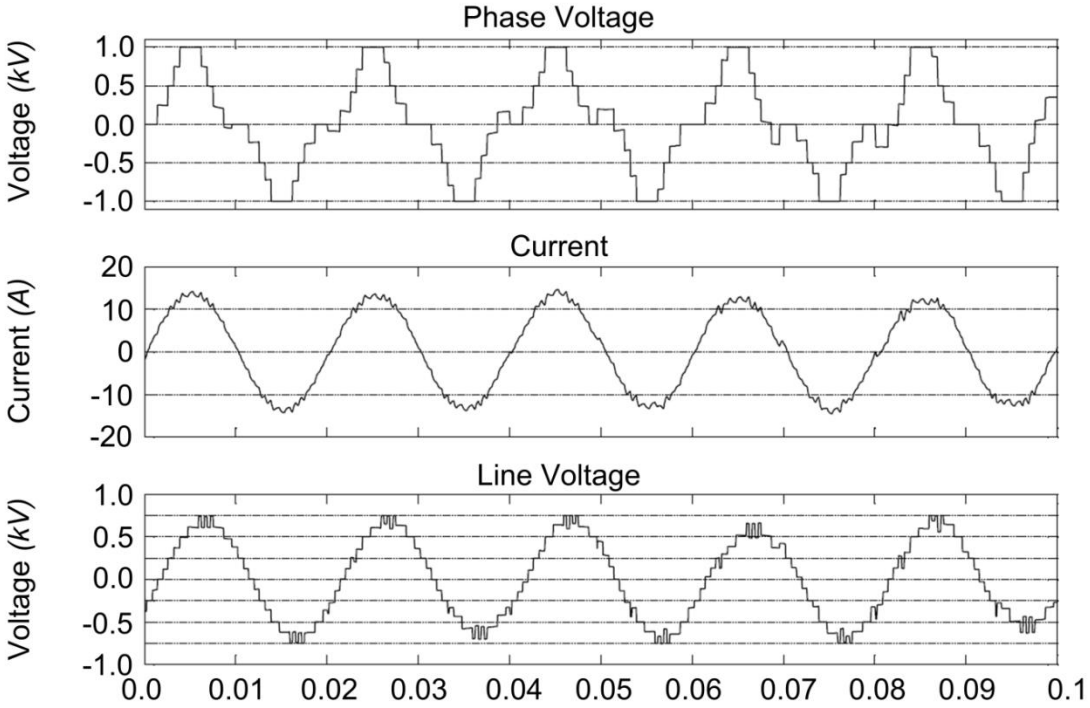


Figure 4.6: Converter Output using SHE-PWM Modulation (m_A = 0.8).

The results of FFT analysis performed on the phase and line-line voltage waveforms are shown in Figure 4.7, which confirm the targeted harmonic components are indeed supressed.

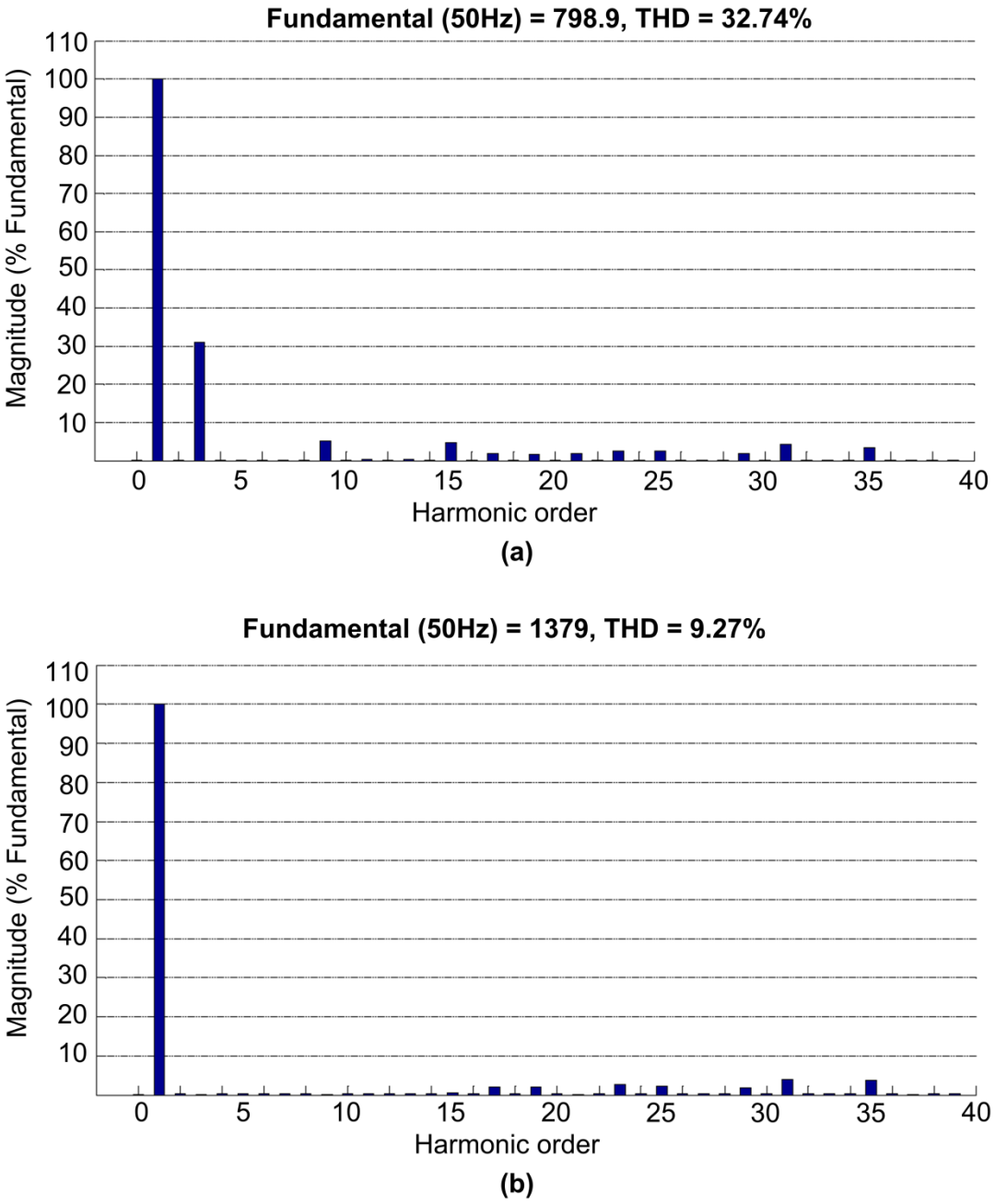


Figure 4.7: THD for SHE modulation showing (a) Phase and (b) Line Voltage.

At m_A = 0.8 the angles (α_1= 0.4313, α_2= 0.7946, α_3= 0.9954, α_4= 1.2021) were applied to cancel the 5th, 7th and 11th harmonic components. This corresponds with 250Hz, 350Hz and 550Hz in Figure 4.5 and it is obvious that these components are supressed.

Also to note, the triplen (3rd order) components i.e the 150Hz, 450Hz, etc which are present in the Phase voltage FFT chart are suppressed in that for the line-line voltage. The method described thus far does not account for

capacitor voltage variation which if left “uncontrolled” diverges from the expected value and results in further harmonic content in the converter voltages. Figure 4.8 shows the effect “un-monitored switching” has on the flying capacitor voltages.

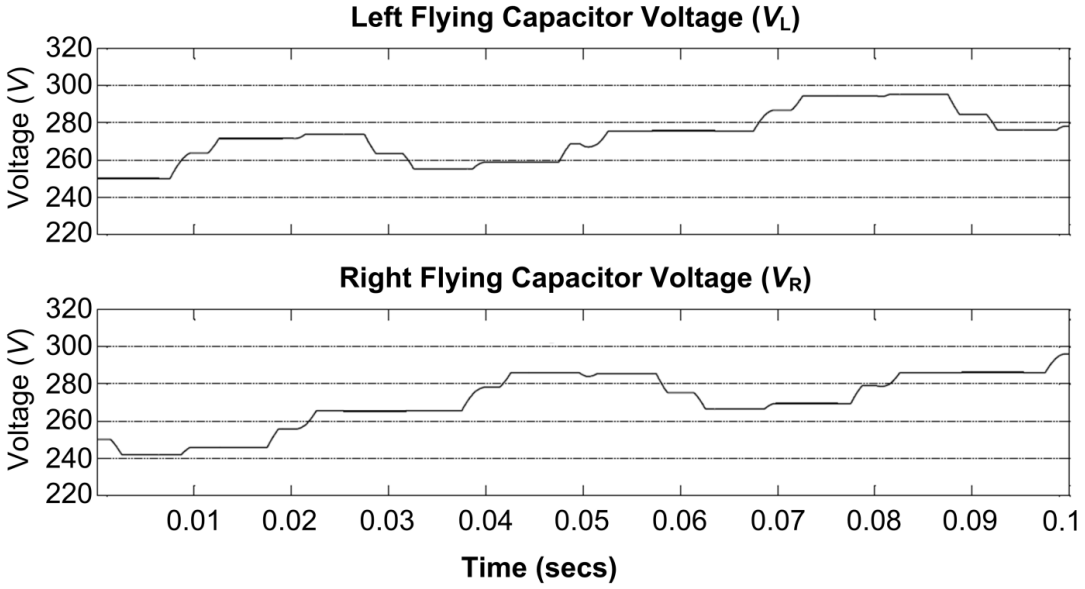


Figure 4.8: Capacitor Voltage Variation in one Module of MMFCC with SHE modulation (no capacitor balancing).

Such divergence also manifests in the converter voltage waveforms. This is evident from around 0.02 secs in the phase voltage waveforms shown in Figure 4.6. Eventually the capacitor voltages either charge to the DC rail or discharge to 0. To avoid the divergence that results from uncontrolled capacitor voltage variation, a capacitor balancing algorithm based on the FCC redundant states [88] is applied within the switch activation sub-system.

As a result, the flying capacitors now vary about a prescribed voltage value. Figure 4.9 shows the same capacitor voltages as seen in Figure 4.8, but with the balancing algorithm implemented. Both capacitors now vary about their prescribed value ($0.5V_N$ = 250 V).

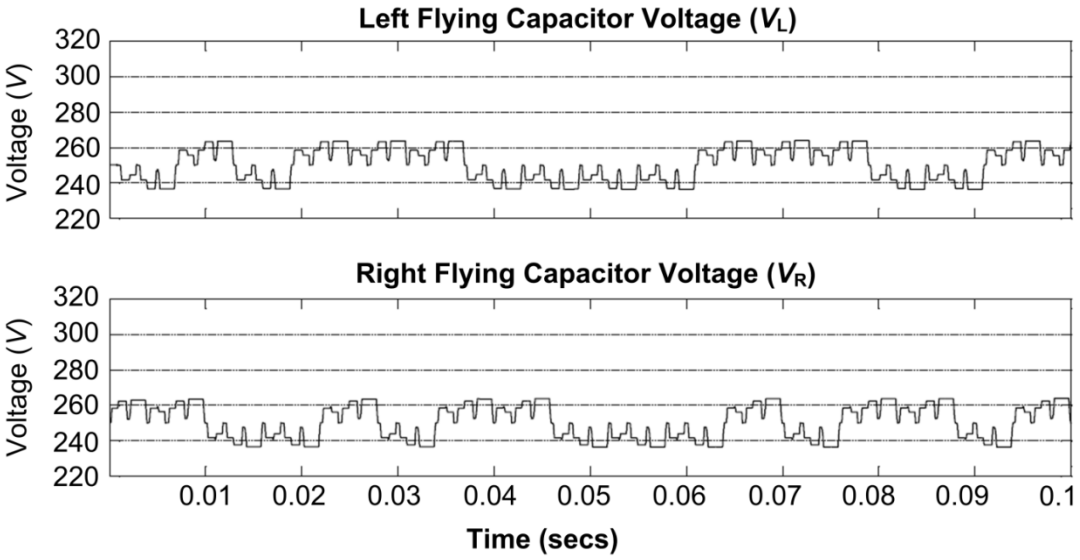


Figure 4.9: Capacitor Voltage Variation in one Module of MMFCC with SHE modulation (with capacitor voltage balancing).

A simple algorithm was applied to derive the balancing in Figure 4.9. The sub-module capacitor and flying capacitor voltages are provided as feedback signals into the switch activation sub-system and the selection criteria below is applied:

- For charging current (i.e. flowing into the sub-module positive terminal), the sub-module with the lowest sub-module capacitor voltage is activated and the switch for the flying capacitor with the lowest voltage is activated.
- For discharging current (i.e. flowing out of the sub-module positive terminal), the sub-module with the highest sub-module capacitor voltage is activated and the switch for the flying capacitor with the highest voltage is activated.

This selection algorithm ensures that the sub-module capacitor and flying capacitor voltages do not deviate excessively but does not account for drift.

4.1.2 Modulation using Carrier Placement Strategies

Carrier placement strategies are the most extensively applied modulation schemes for classical converter modulation. In principle the switching signals for an inverter are generated by comparing a sinusoidal (reference) signal with at least one triangular (carrier) signal at a frequency higher than that of the fundamental. The analysis of a carrier placement PWM strategy for an inverter can be expressed using Black and Holmes approach [21-24]. The carrier and reference signals are represented as time varying functions *c*(*t*) and *o*(*t*) in (4.8) and (4.9) respectively.

$$c(t) = \omega_C t + \theta_C ; \omega_C = \frac{2\pi}{T_C} \qquad \textbf{4.8}$$

$$o(t) = \omega t + \phi ; \omega = \frac{2\pi}{T} \qquad \textbf{4.9}$$

where ω_C is the angular frequency of the carrier wave

T_C is the period of the carrier wave

Θ_C is the phase shift angle for the carrier wave

ω is the angular frequency of the reference wave

T is the period of the reference wave

ϕ is the phase offset for the reference wave

t is the instantaneous time value

Applying Fourier analysis to the carrier modulated reference signal results in a double variable function of *c*(*t*) and *o*(*t*) with regards to its harmonic content as shown in (4.10).

$$f\{c(t), o(t)\} = \underbrace{\frac{a_{00}}{2}}_{DC-bias} + \underbrace{\sum_{j=1}^{\infty}\left[a_{0j}\cos j(\omega t + \phi) + b_{0j}\sin j(\omega t + \phi)\right]}_{1st Term(Fundamental+Baseband\_Harmonics)} +$$

$$\underbrace{\sum_{i=1}^{\infty}\left[a_{0i}\cos i(\omega_C t + \theta_C) + b_{0i}\sin j(\omega_C t + \theta_C)\right]}_{2nd Term(Carrier\_Harmonics)} +$$

$$\underbrace{\sum_{i=1}^{\infty}\sum_{j=-\infty}^{\infty}\left[a_{ij}\cos\{i(\omega_C t + \theta_C) + i(\omega t + \phi)\} + b_{ij}\sin\{i(\omega_C t + \theta_C) + j(\omega t + \phi)\}\right]}_{3rd Term(Sideband\_Harmonics)}$$

4.10

where:

a_{00} is an amplitude value which describes the DC bias in the pulse-width modulated waveform;

a_{0i}, a_{0j}, a_{ij} and b_{0i}, b_{0j} and b_{ij} describe the amplitude of the harmonic components in each term of the summation operator;

i are *j* are index variables for the carrier and baseband.

The angular frequency of every harmonic order can be defined using the variables "*i*" and "*j*" as thus: ($i\omega_C + j\omega$). For instance (4ωC + 8ω) describes the 8th sideband harmonic located around the harmonic number of the 4th multiple of the carrier frequency. Also of interest are baseband harmonics presented when "*i* = 0" (i.e only *j* prescribes the harmonic frequency) as well as carrier harmonics, presented when "*j* =0" (i.e only the variable *i* prescribes the harmonic frequency). According to (4.10) a DC bias (or offset) in the reference signal is expressed in the first term "a_{00}". The next term expresses any baseband harmonics existing in the reference signal including the fundamental component at *j* = 1. Carrier placement techniques typically supress all low-order baseband harmonics that exist up to the equivalent carrier switching frequency apart from the fundamental. The second summation term in (4.10) expresses the carrier harmonics located at the modulation carrier frequency and its multiples. These are relatively higher order harmonics with low amplitudes. The third summation term expresses sideband harmonics which exist as result of the sum and difference between the baseband and carrier harmonic components. As the low-order harmonics are normally supressed, the sideband harmonics, exist only at the carrier frequency and above.

Extensions to the classical carrier placement strategy to cater for multilevel converters include: the phase-shift PWM (PS-PWM); and phase-disposition PWM (PD-PWM) also known as phase-displacement PWM. Variants for specific applications now include strategies like the Phase Opposition Disposition PWM (POD-PWM) and the Alternative Phase Opposition Disposition PWM (APOD-PWM), as well as their modified reference variants such as the Third Harmonic Injection- (THI- PWM) strategies.

4.1.2.1 Phase-Shift PWM

The Phase-Shift PWM technique involves the use of multiple carriers with a time or phase delay (phase-shift constant) from each other. Analytically this

is expressed as an introduction of more terms into the 2nd summation in (4.10). The overall effect is first significant harmonics being present not at the carrier frequency, but at the multiple of the carrier frequency and the number of carriers.

Application to the multi-module FC topology involves two considerations:

- The phase-shift value applied between the carriers that activate the different voltage levels for each converter phase.
- The generation of switching signals for the adjacent switches in the full-bridge FCC sub-modules. This is tackled using the anti-phase references of a unipolar PWM.

Four carrier signals are required to generate the four distinct voltage levels (excluding 0 *V*) that make the phase voltage for the converter in Figure 4.1. The carrier frequency can be chosen as an even multiple of fundamental reference frequency, in such a case the side-band harmonics at the equivalent carrier frequency are supressed with the carrier harmonics attenuated. If an odd multiple value is chosen, the side-band harmonics are attenuated while the carrier harmonic is suppressed. For each converter phase, the switching instants for the LHS switches are generated by comparing the four carrier signals with a positive sinusoidal reference signal. Switching signals for the sub-module RHS switches are generated by comparing a 180^0 phase-shifted reference signal against the same four carrier signals. This unipolar PWM technique attenuates the carrier and side-band harmonics by an extra order of 2 resulting in harmonics at (2*f*c, 4*f*c, …), instead of (1fc, 2f_c, …).

The reference, carrier and switching signals for the phase-shift PWM techniques applied to the 2-sub-module MMFCC phase arm is shown in Figure 4.10. The phase-shift constant between the carrier signal is shown as θ_C and the carrier frequency is ω_C with the relationship between both parameters expressed in (4.11).

$$\theta_C = \frac{\omega_C}{2c_T} \qquad \textbf{4.11}$$

where c_T is the number of carrier signals implemented = 4

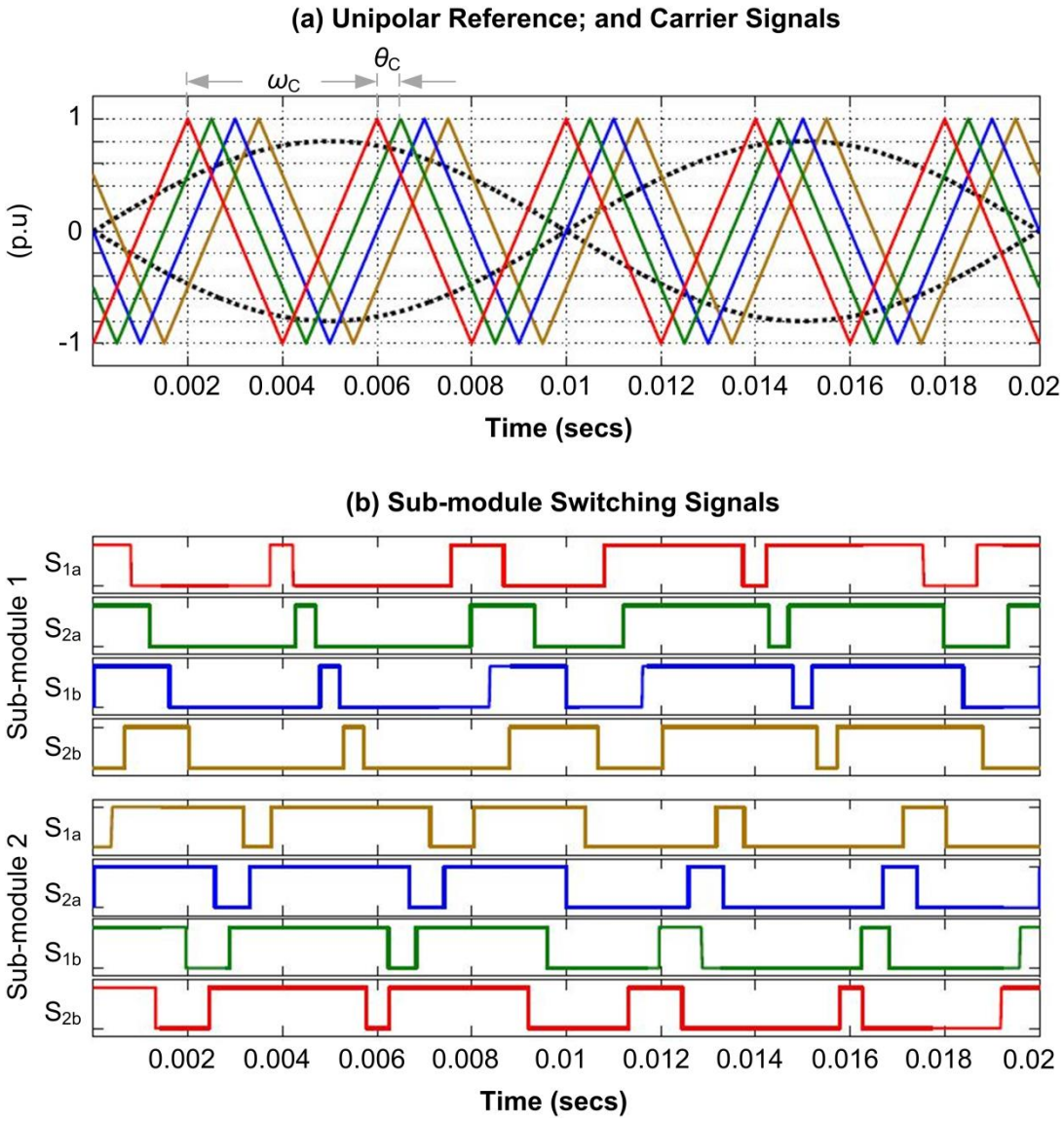


Figure 4.10: Phase-Shift PWM applied to the MMFCC Phase leg. (a) reference and carrier waves (b) Switching signals.

Note that in (4.11) the phase-shift is calculated with reference to the 250Hz carrier frequency (not the fundamental frequency). Also the total number of carriers can be obtained by subtracting 1 from the number of distinct levels in the converter phase voltage waveform.

The converter phase voltage and harmonics/spectral THD plot is shown in Figure 4.11. Harmonic suppression is achieved and all carrier and baseband harmonics are supressed up until eight times the switching frequency (40^{th} harmonic order) as shown in Figure 4.11. The THD content of the phase voltage is 17.15% with side band harmonics (around 30^{th} and 50^{th} harmonic order) suppressed until the 40^{th} harmonic order.

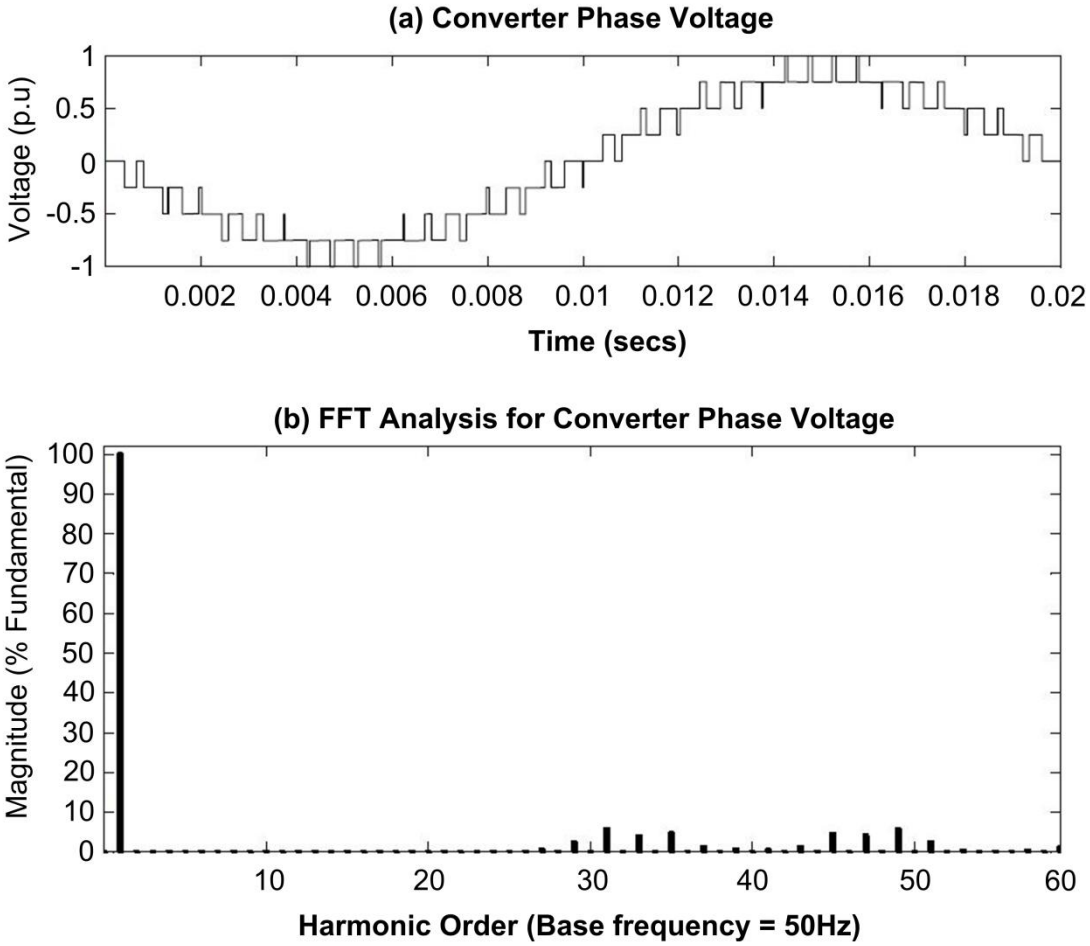


Figure 4.11: Phase-Shift PWM applied to the MMFCC. (a) converter phase voltage (b) Phase voltage spectral analysis.

The sub-module switching actions shown in Figure 4.11 cause the voltages for the flying capacitors in each sub-module to vary depending on the direction of current flow. To illustrate this effect, voltage variation for the flying capacitors within one sub-module is shown in Figure 4.12. A sub-module capacitor voltage (V_C) of 500 volts simulated, hence the nominal voltage value expected for the flying capacitors is 250 volts. The capacitance value simulated for the flying capacitors is 560μF.

The natural voltage balancing capability of the phase-shift PWM technique is illustrated in Figure 4.12 as the flying capacitor voltages V_L, V_R track around the nominal value of 250 volts. Due to the nature of PS-PWM modulation control, even though each carrier is shifted in time, the switching actions produced over a cycle are repetitive across all carriers. This results in equal utilisation of the available sub-module redundant switching states. Thus the flying capacitors are charged and discharged evenly.

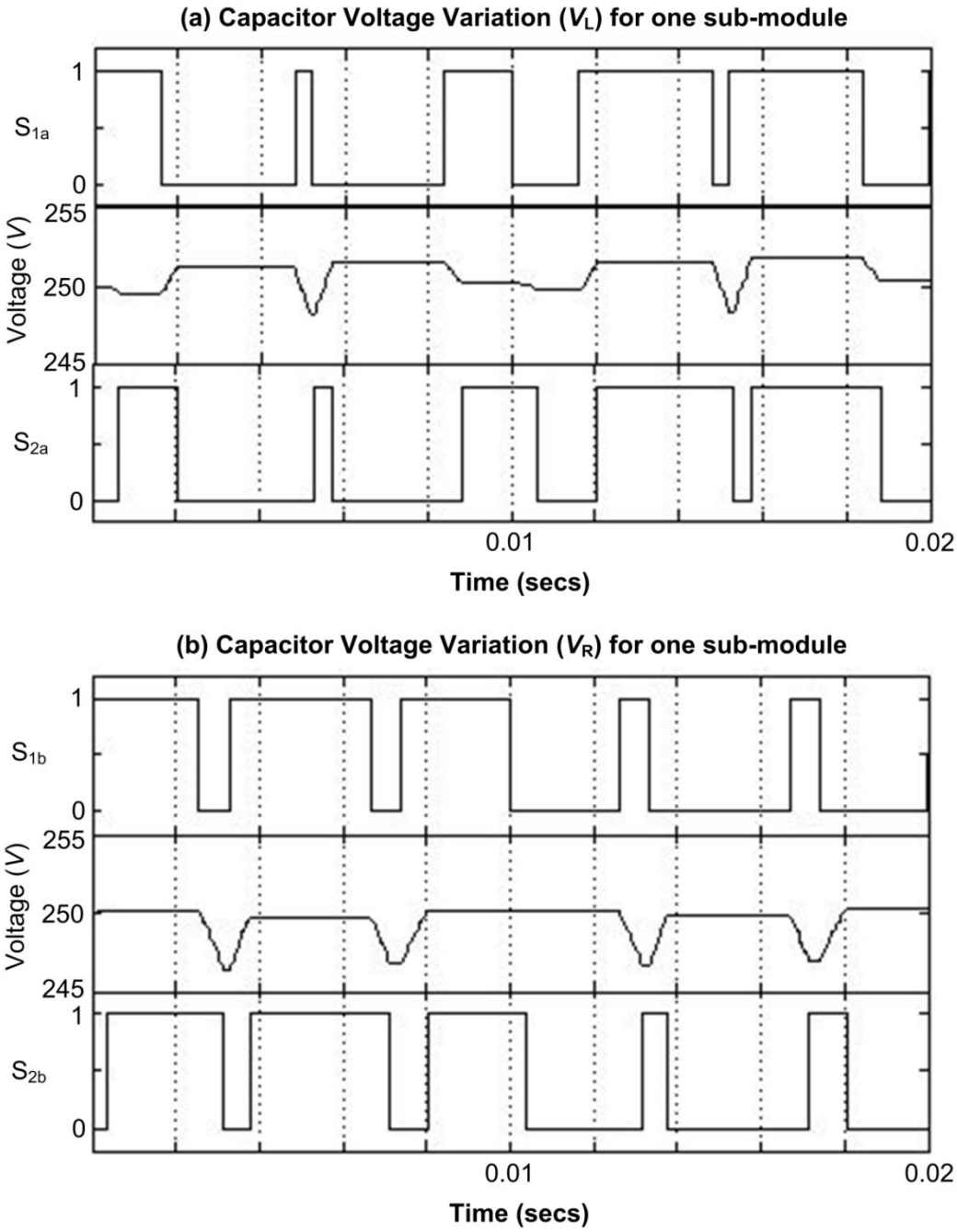


Figure 4.12: PS-PWM Switching actions and the flying capacitor voltage variation for one sub-module.

This shared utilisation of switching states also implies that voltage stress and subsequently switching losses are shared evenly across the devices in each module. The rate of charge and discharge reflected across the capacitors is always a function of capacitance and load characteristics while the level of charge and discharge is a function of the switching frequency. However the bias of the Phase-shift PWM technique towards a more balanced and

shared switching utilization also results in the this method presenting higher switching losses.

4.1.2.2 Phase-Disposition PWM

The Phase-Disposition PWM (PDPWM) scheme involves displacing the carriers in amplitude instead of time. The number of disposed carriers signals required equals the number of discrete voltage levels minus 1, and these carriers are distributed evenly across the positive and negative half of the reference signal.

An implementation of the PDPWM scheme for the MMFCC is illustrated in Figure 4.13 and requires the use of four carriers; in phase but level-shifted. The carrier signals are compared against a sinusoidal reference signal and its anti-phase counterpart, hence giving the unipolar switching. The resulting sub-module switching signals are shown in Figure 4.13(b) and applied to the sub-modules in each converter phase.:

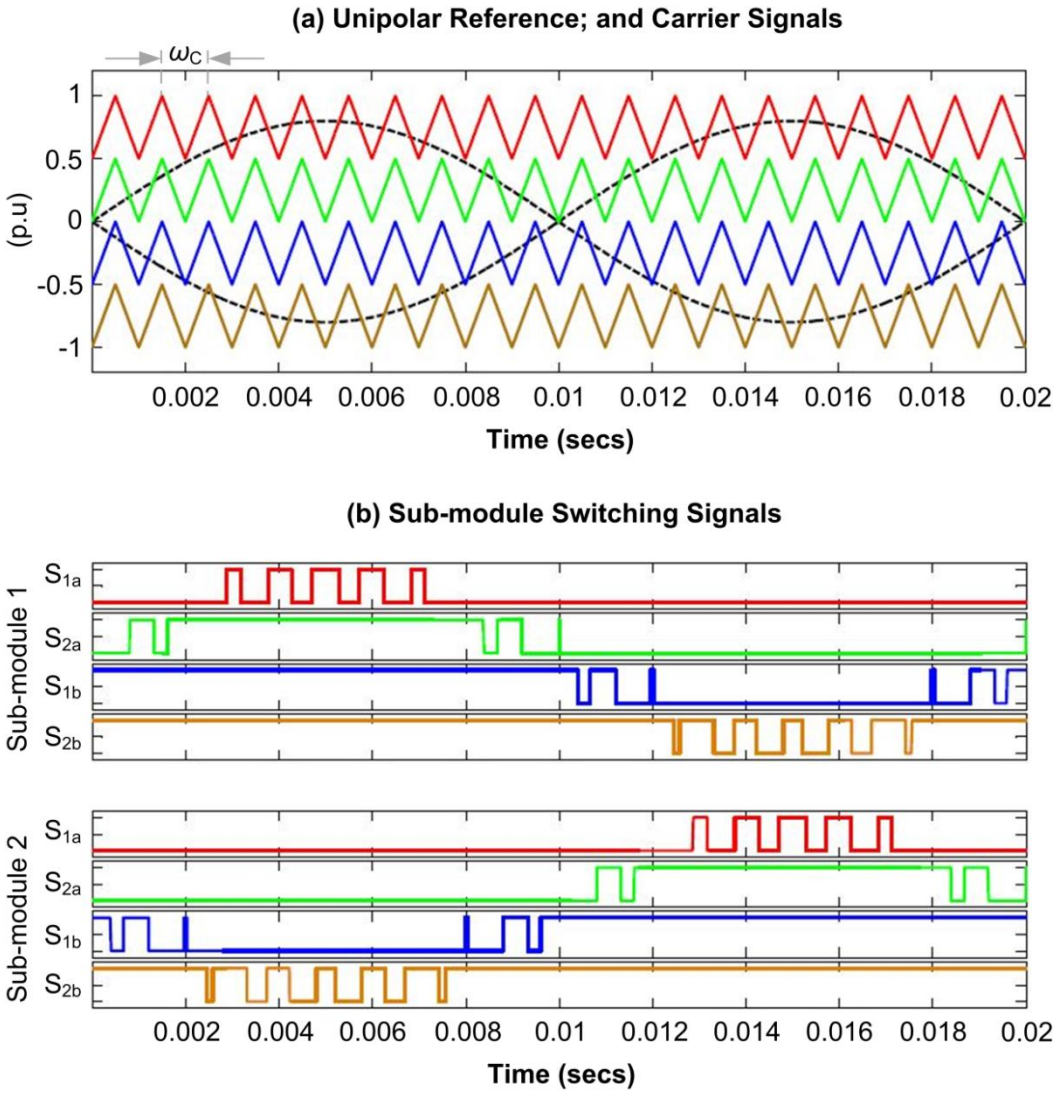


Figure 4.13: Phase-Disposition PWM applied to the MMFCC Phase leg. (a) reference and carrier waves (b) Switching signals.

The signals generated from comparing against the in-phase sinusoidal reference signal are applied for controlling the LHS switches, those from the anti-phase reference signal are applied to the RHS switches.

As shown in Figure 4.13 (b) the switch utilisation is not even, thus different switches experience varying levels of conduction and switching stress. For instance, switches activated according to the top (red) and bottom (brown) carriers will experience more switching stress, hence higher switching losses compared with the others. However those devices activated by carriers in blue and green colours stay in the turn-on state longer so would have to withstand higher conduction losses.

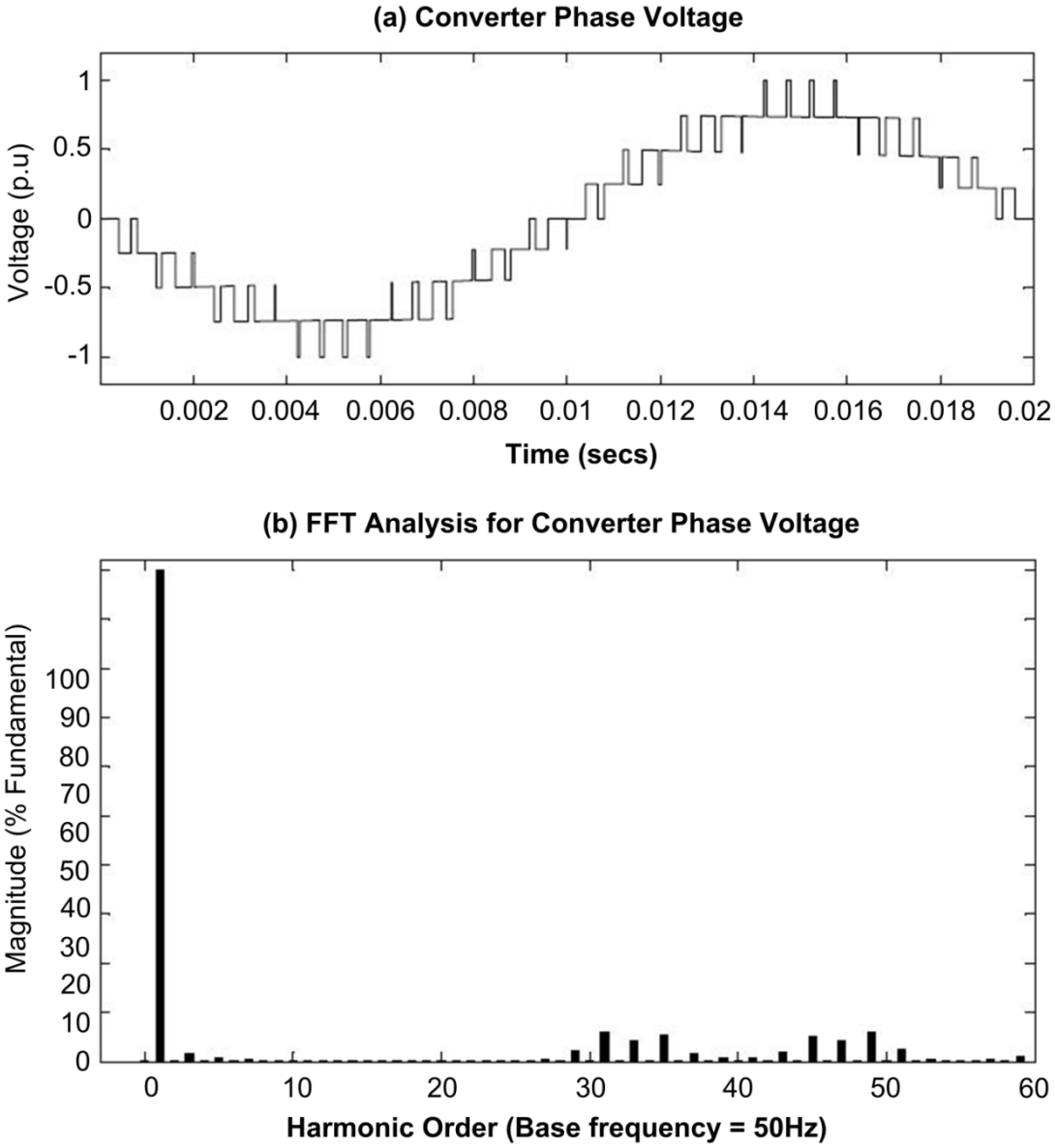


Figure 4.14: Phase-Disposition PWM applied to the MMFCC. (a) converter phase voltage (b) Phase voltage spectral analysis.

The spectrum analysis for the converter phase voltage Figure 4.14 (b) generated using the PDPWM scheme shows harmonics are not observed at the carrier frequency (1 kHz) but suppressed until two times the carrier frequency (i.e. the 40th harmonic order). The analysis also shows side band harmonics around the 33rd and 47th harmonic order.

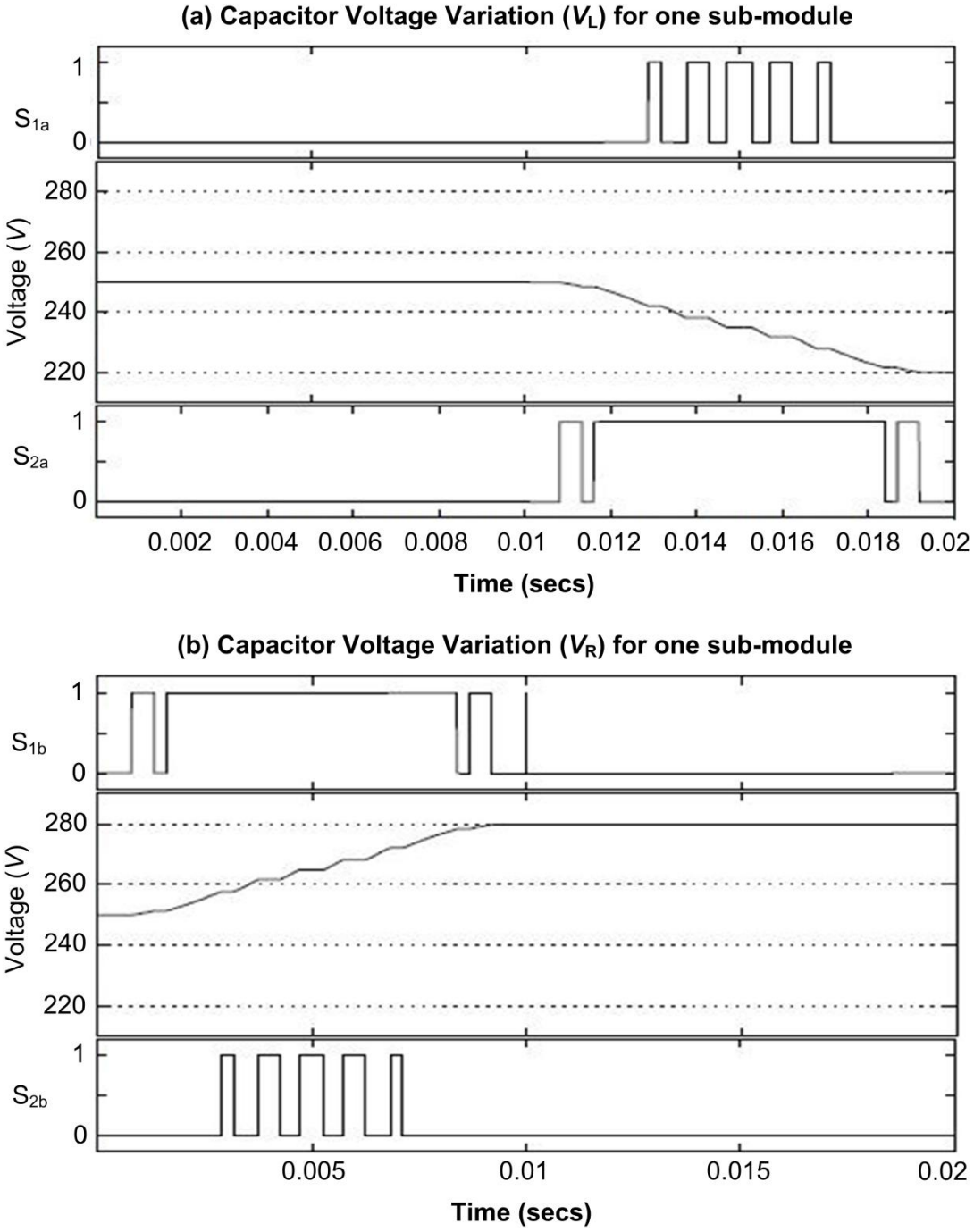


Figure 4.15: PD-PWM Switching actions and the flying capacitor voltage variation for one sub-module.

The switching signals generated from the PDPWM scheme causes the voltages across sub-module flying capacitors to vary and deviate from the nominal value. To illustrate this effect, the voltage variation for the flying capacitors within one sub-module is shown in Figure 4.15.

The unsymmetrical switching pattern from the PDPWM scheme is shown to discharge the left flying capacitor and subsequently charge up the right flying capacitor by the same value of voltage. This results in a flying capacitor voltage deviation (from the nominal value) of ±30 *V* per cycle, making the open-loop implementation of the PDPWM scheme impractical. This clearly illustrates the importance of capacitor balancing for the PDPWM technique. The normal approach involves creating a feedback loop for each flying capacitor voltage, however this may prove tedious when the number of modules is increased to extend the converter to a higher voltage rating.

Note that each flying capacitor voltage shows a variation rate and an amount which are functions of the carrier frequency and load characteristics. In Figure 4.15 each capacitor voltage shows a variation of either 12% about its nominal level of 250 *V*. This is because when implementing the standard PD-PWM technique, only 2 out of the 4 redundant switching states, which either discharge or charge the flying capacitors, are applied to synthesise the intermediate voltage levels. Over time this will lead to an output voltage waveform with an unacceptable spectral quality due to capacitor voltage level diverging away from its nominal voltage level.

4.1.2.3 Swapped carrier Phase-Disposition PWM with natural balancing

A new modulation scheme was developed as part of this thesis to mitigate the voltage deviation that occurs when the classical extension of the PDPWM is applied to the MMFCC. This involves rotating the level of the carrier waves sequentially, as is shown in Figure 4.16 to realise a swapped carrier PDPWM scheme with natural capacitor voltage balancing.

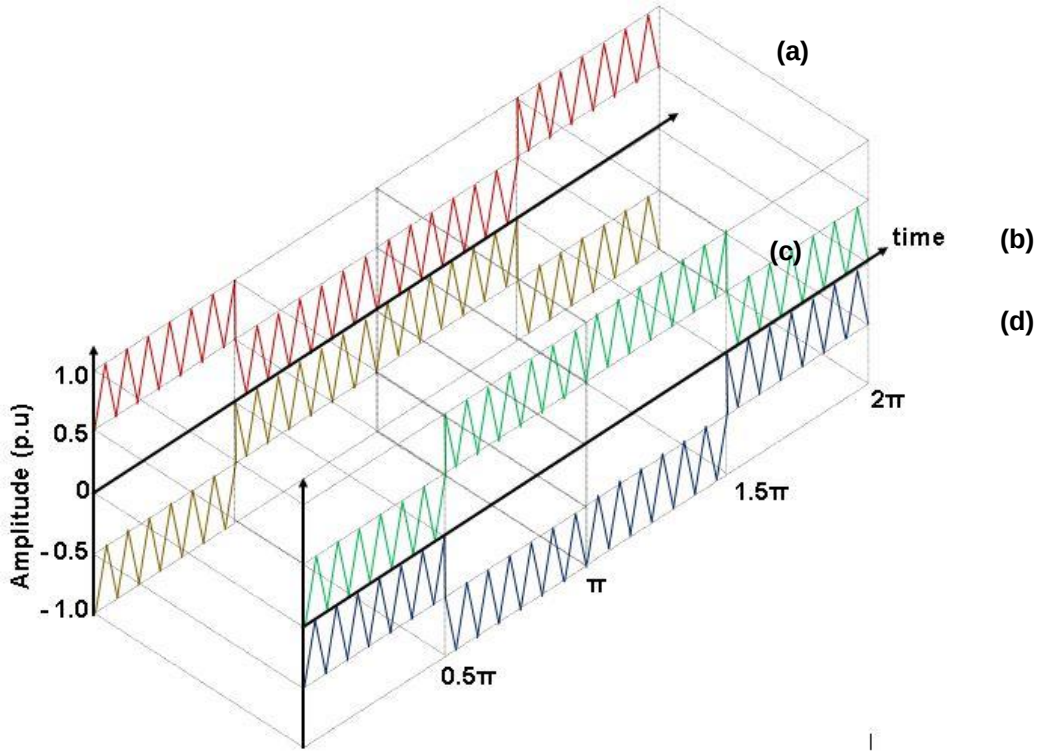


Figure 4.16: Swapped Carrier PD-PWM for one MMFCC Phase-leg.

The colour code in Figure 4.13 is maintained for reference. The red carrier waveform when compared with both the in-phase and anti-phase reference waveforms generates switching signals for LHS switches for one sub-modules in each converter phase, while the green carrier waveform generates that for the RHS switches in the sub-module. For the next sub-module the blue carrier generates signals for the LHS switches and finally the brown carrier waveform for the RHS switches. Interchanging the carriers over a defined period, causes a change in the switching state chosen and this results in an equal utilisation of the redundant states that cause the flying capacitors to charge and discharge.

During each swapping action, the carrier that generated the previous state (causing the capacitor to charge) is “swapped” with one that still produces switching signals for that level, but causes the flying capacitor to discharge.

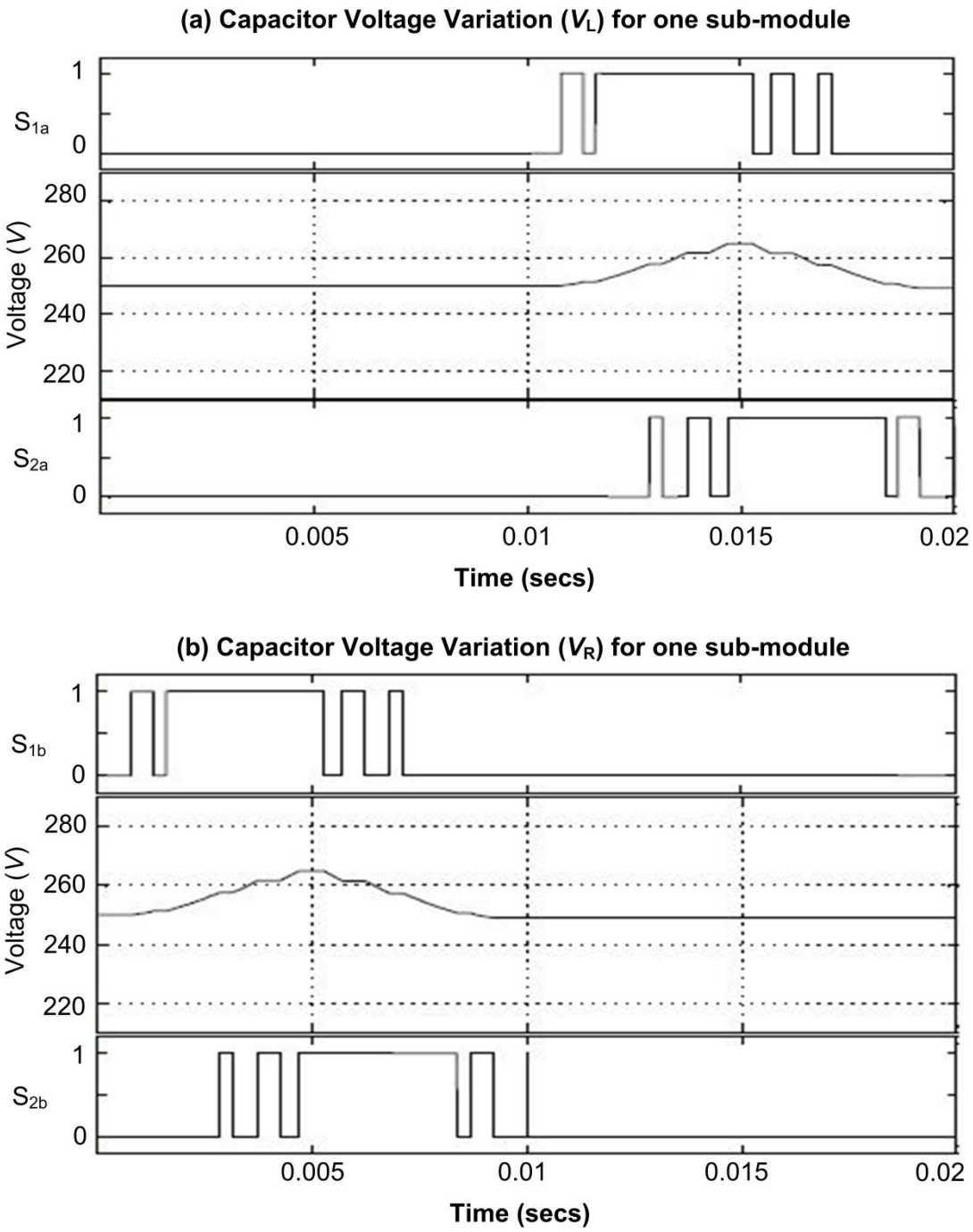


Figure 4.17: Swapped Carrier PD-PWM Switching actions and the flying capacitor voltage variation for one sub-module.

The resulting capacitor voltages from implementing this swapping technique are shown in Figure 4.17. The technique is also flexible as options exist for spreading the swapping sequence over the fundamental period or its multiples. For instance, a voltage variation of 30 volts was previously observed for the classical extension of the PDPWM. Spreading the carrier swapping sequence over one fundamental period will result in the flying

capacitor voltage varying by 30 Volts (for instance from 250 -280 volts) during the time interval (0 – 2π). In the next fundamental period (i.e after the carriers have been swapped) it will vary by -30 Volts (i.e from 280V back to 250V) during the time interval (2π – 4π). The same swapping sequence can be implemented over half a fundamental cycle. This will cause the capacitor to charge and discharge within a fundamental period (rather than two) and by only 15 Volts. This is observed in the waveform shown in Figure 4.15 .

It is then possible to infer that reducing the time for spreading this swapping sequence yields lower capacitor voltage variation but each state change also implies an extra switching loss across the device.

4.1.3 Overlapped Hexagon Space Vector Modulation Strategy

Space vector pulse width modulation (SVM) is well-known for its ease of digital implementation and ability to provide an extra 15% higher DC link voltage utilisation when compared with other techniques. This is due to the protrusions presented by the vertices of the space-vector hexagon while representing three-phase sinusoidal voltages. For two-level voltage source converters, two types of SVM modulation: the two-phase; or symmetrical method is normally implemented with the directive to optimise converter efficiency via switching loss reduction. In [100] however, both techniques are combined in order to harness the advantages presented while overcoming the shortcomings.

Multilevel SVM is an extension of the two-level SVM technique. The converter switching states, depending on the number of voltage levels, are mapped to the complex two-phase orthogonal α-β plane. The three-phase reference voltages for the converter, assumed to be balanced, are represented as a 2-D vector in this plane. Instantaneous duty-cycles are computed for the selected switching state vectors in closest proximity to a reference vector within a mapped hexagon area. Figure 4.16 shows each of the six sectors of the hexagon is divided into n_{VPG}^2 triangles of equal size, due to multiple phase voltage levels required (where n_{VPG} denotes the number of voltage levels from phase-peak to ground).

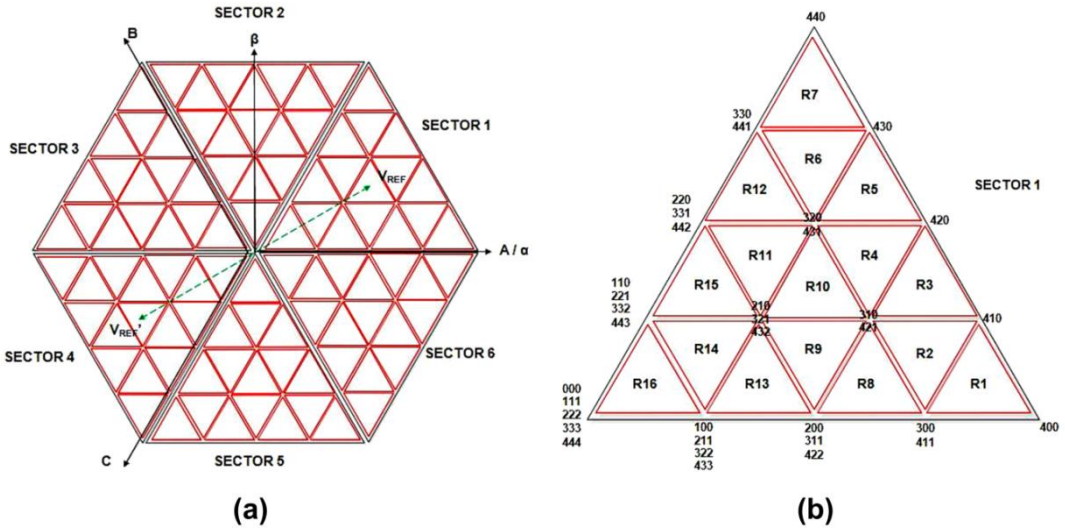


Figure 4.18: ML-SVM for MMFCC showing (a) orthogonal hexagon plane (b) 5-level triangular region.

The vertices of each triangle region within the hexagon are allocated specific switching vectors, thus the position of the reference vector within a triangle is

resolved to calculate the duty cycles of its vertex vectors. As an added advantage of ML-SVM, the symmetrical SVM technique can achieve capacitor voltage balancing for the FCC modules in open-loop. This is true as long as the voltage state vectors for synthesizing the reference are implemented in a manner that charges and discharges the flying capacitors evenly over a period.

Despite the advantages stated, direct extension of the ML-SVM hexagon to control converter with higher voltage levels is complex due to the rapidly increased numbers of triangular regions and switching vectors. For instance, for a converter with nine voltage levels (including the zero voltage) there are 96 triangular regions and 119 voltage switching vectors for total of six sectors. (4.12) and (4.13) express the total number of regions (n_R) and voltage vectors (n_V) required as a function n_{VPG}.

$$n_R = 6(n_{VPG} - 1)^2 \quad \textbf{4.12}$$

$$n_V = n_{VPG} + \sum_{i=1}^{n_{VPG}-1} 6x + \sum_{i=2}^{n_{VPG}-1} 6x(n_{VPG} - x)(x - 1) \quad \textbf{4.13}$$

where *i* is an index variable for initializing the summation operator.

This is especially valid for the proposed MMFCC topology as each new module increases n_{VPG} by a value of two, thus significantly complicating the modulation processes of region detection, voltage vector selection and subsequently vector duration calculation.

4.1.3.1 OH-SVM Principle

To tackle the complexity associated with the extension of the classical space vector modulation technique, a new modulation strategy: the overlapped space vector modulation was developed. We consider the MMFCC to be controlled two-tiers of a three-phase arrangement of FCC sub-modules. Each tier can independently synthesise a three-phase voltage thus can be mapped on a separate orthogonal plane within a 24 triangular region hexagon. As a result, the previous 5-level (96 region) hexagon may be represented as two 3-level (24-region) hexagons.

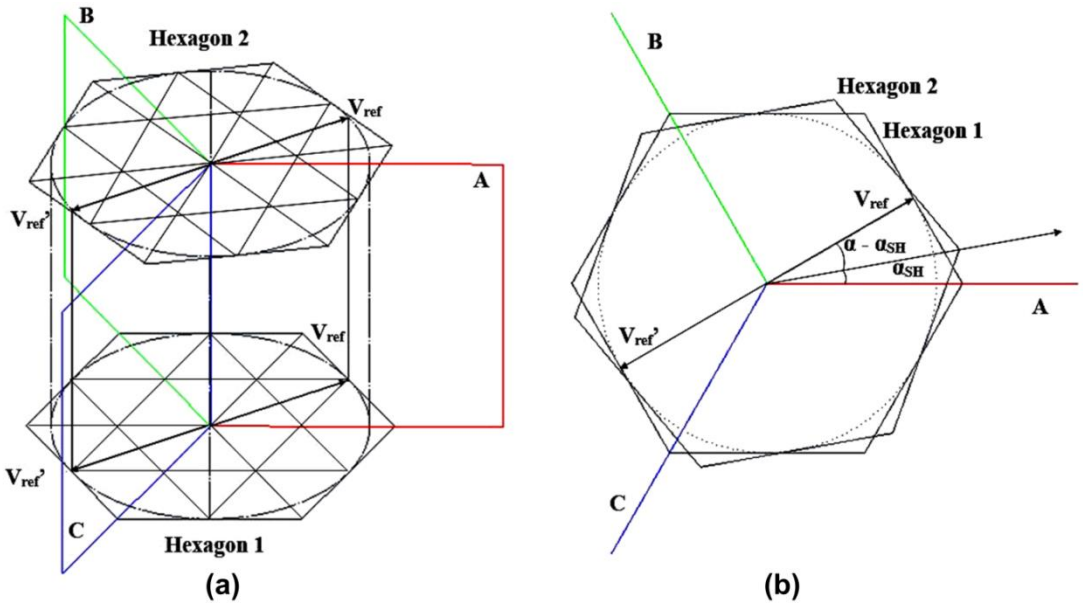


Figure 4.19: Principle of OH-SVM for MMFCC showing (a) 3D mapping of hexagon plane (b) Top view mapping of hexagon plane.

Taking the hexagon for the tier of the lowest voltage level as the reference, the other hexagon overlaps that of its lower voltage counterpart, but with a phase angle displacement of α_{SH}. This hexagon phase shift value is determined by the number of modules per phase (n_{MP}), switching period (T_S) and fundamental period (T) as expressed in (4.14)

$$\alpha_{SH} = \frac{\left(T_S / 2n_{MP}\right)}{T} \times 360^0 \quad \textbf{OR} \quad \alpha_{SH} = \frac{\left(T_S / 2n_{MP}\right)}{T} \times 2\Pi(rad) \qquad \textbf{4.14}$$

This is shown in Figure 4.20 where a spatial representation of one of the interleaved hexagons is presented with a reference voltage vector, V_{ref} , in each hexagon as well as a 180^0 phase-shifted counterpart, $V_{ref}^{'}$. The former determines switching vectors for the three-phase LHS unit-cells in a tier while the latter is for that of three-phase RHS unit cells. As a result of hexagon overlapping, the angular positions for both V_{ref} and $V_{ref}^{'}$ in each hexagon are also phase shifted accordingly. Taking the hexagon for the lowest tier as the reference with angular value, α, that for the nth tier is given as

$$\alpha_N = \left(\alpha - (h_N - 1)\alpha_{SH}\right) rad \qquad \textbf{4.15}$$

where h_N is the hexagon number to represent tier 1, tier 2 and so on. Naturally the phase angle for the corresponding $V_{ref}^{'}$ is 180° displaced to α_N.

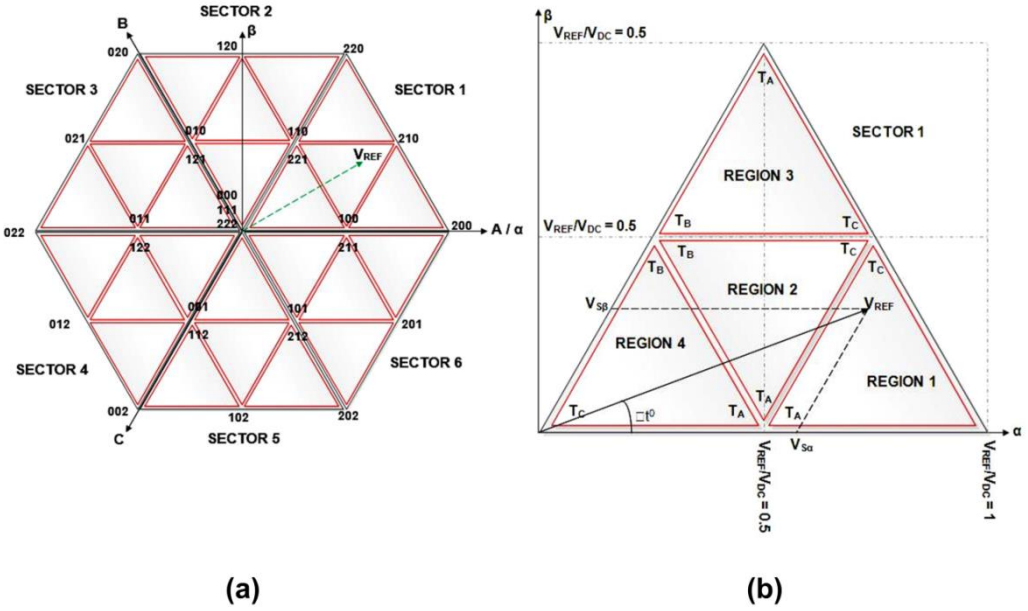


Figure 4.20: 3-level hexagon for OH-SVM showing (a) all sectors (b) region detection in sector 1.

4.1.3.2 OH-SVM Algorithm

The OH-SVM algorithm involves determining the positions and hence switching state vectors in each hexagon for synthesizing V_{ref} and $V_{ref}^{'}$ and calculating the duty cycles for all chosen switching vectors. As is well known the classical multilevel SVM algorithm involves identifying the sector amongst six according to the phase angles of the reference voltages. With multiple overlapped hexagons the sector numbers of the reference voltage vectors in each hexagon may be different at certain instances. This can be obtained from the expression in (4.16) below which shows the Euclidean division of the perceived angle, α_N, by the sector angle (60^0 or π/3),

$$\alpha_P/(\pi/3) = (S_N - 1)\pi/3 + \alpha_P \bmod \pi/3 \qquad \textbf{4.16}$$

where S_N represents the current sector number.

Next, as part of the OH-SVM algorithm the regions of the reference vector within a chosen sector, i.e the switching state vectors, are determined. There are four triangular regions in each sector bounded by three switching state vectors. To determine the location of a reference vector at each time instant, the vertex of the reference voltage vector, V_{ref}, is decomposed into its two sector-based orthogonal components, $V_{S\alpha}$ and $V_{S\beta}$, as expressed in (4.17).

$$V_{S\alpha} = \frac{Vref}{V_{DC}}\left[\cos(\alpha_P) - \frac{\sin\alpha_P}{\sqrt{3}}\right]$$
$$V_{S\beta} = 2\frac{Vref}{V_{DC}}\frac{\sin\alpha_P}{\sqrt{3}} \qquad \textbf{4.17}$$

The corresponding region the reference vector locates can be determined according to its $V_{s\alpha}$, $V_{s\beta}$ values in comparison to the modulation index as listed in Table 4.3.

Table 4.3: Criteria for region localisation

Region 1	Region 2	Region 3	Region 4
$V_{S\alpha} > 0.5V_{DC}$	$V_{S\alpha} < 0.5V_{DC}$ $V_{S\beta} < 0.5V_{DC}$ $V_{S\alpha} + V_{S\beta} > 0.5V_{DC}$	$V_{S\beta} > 0.5V_{DC}$	$V_{S\alpha} < 0.5V_{DC}$ $V_{S\beta} < 0.5V_{DC}$ $V_{S\alpha} + V_{S\beta} < 0.5V_{DC}$

Three switching state vectors are selected from the three vector groups located at each vertex in the triangle region where the reference voltage phasor is located. For instance, if the peak of reference voltage phasor locates in sector 1-region 1, the possible switching state vectors are 200; 210 and (100 or 211), while in sector 2-region 2, possible switching vectors are 100; (211,210) and (110 or 221).

An example of an optimized selection of switching voltage vectors for a reference voltage phasor located in Region 1 is shown in Table 4.4.

Table 4.4: Vector combination chart showing voltage vector selections for Sector 1 (Regions 1)

		$\frac{T_1}{4}$		$\frac{T_2}{2}$		$\frac{T_3}{2}$		$\frac{T_1}{4}$		$\frac{T_1}{4}$		$\frac{T_3}{2}$		$\frac{T_2}{2}$		$\frac{T_1}{4}$	
		LHS	RHS	LHS	RHS	LHS	RHS	LHS	RHS	LHS	RHS	LHS	RHS	LHS	RHS	LHS	RHS
Region 1	A	1	0	2	0	2	0	2	1	2	1	2	0	2	0	1	0
	B	0	1	0	2	1	1	1	2	1	2	1	1	0	2	0	1
	C	0	1	0	2	0	2	1	2	1	2	0	2	0	2	0	1

LHS and RHS denote the vectors chosen for left hand and right hand side switches of the full-bridge flying capacitor sub-modules respectively. Four

switching states are available for each leg of FCC module in each phase of the MMFCC converter. In Table 4.4 the voltage vectors are selected in order that open loop flying capacitor balancing is achieved by applying an equal number of charging and discharging states over the switching period.

As in classical SVM, the vector duty cycles are calculated based on the symmetrical placement of the three closest voltage vectors forming edges of the region chosen to represent *V*ref. The three duty cycles (D_A, D_B, D_C) required to describe the reference voltage at every instant as it passes through each region are shown in Table 4.5. Note that at every instant, the condition $D_A + D_B + D_C = 1$ must be met, since they represent three vector time durations T_A, T_B, and T_C and their sum must always equal to the sample period T_S.

Table 4.5: OH-SVM Vector Duty-Cycle Calculation

Region 1	Region 2	Region 3	Region 4
$D_A = V_{S\beta}$ $D_B = V_{S\alpha} – 0.5$ $D_C = 1 - D_A - D_B$	$D_A = V_{S\beta} – 0.5$ $D_B = V_{S\alpha} – 0.5$ $D_C = V_{S\alpha} + V_{S\alpha} – 0.5$	$D_A = 1 - D_A - D_B$ $D_B = V_{S\alpha} – 0.5$ $D_C = V_{S\alpha}$	$T_A = V_{S\alpha}$ $T_B = V_{S\beta}$ $T_C = 0.5 - D_A - D_B$

4.1.3.3 Simulation Studies of OH-SVM

Simulation studies were performed as proof-of-concept validation of OH-SVM technique applied for the the control of the 6-module, two-tier, MMFCC topology. The sub-module DC voltage was normalised as 250 *V* per FCC sub-module. The flying capacitors were simulated as 1000 µF. An R-L load of 57.6 Ω-12mH per phase was connected at the three-phase AC output terminals. A 2 kHz modulation sampling frequency was implemented.

The flowchart for the OH-SVM scheme as applied for the control of the MMFCC topology is shown in Figure 4.21.

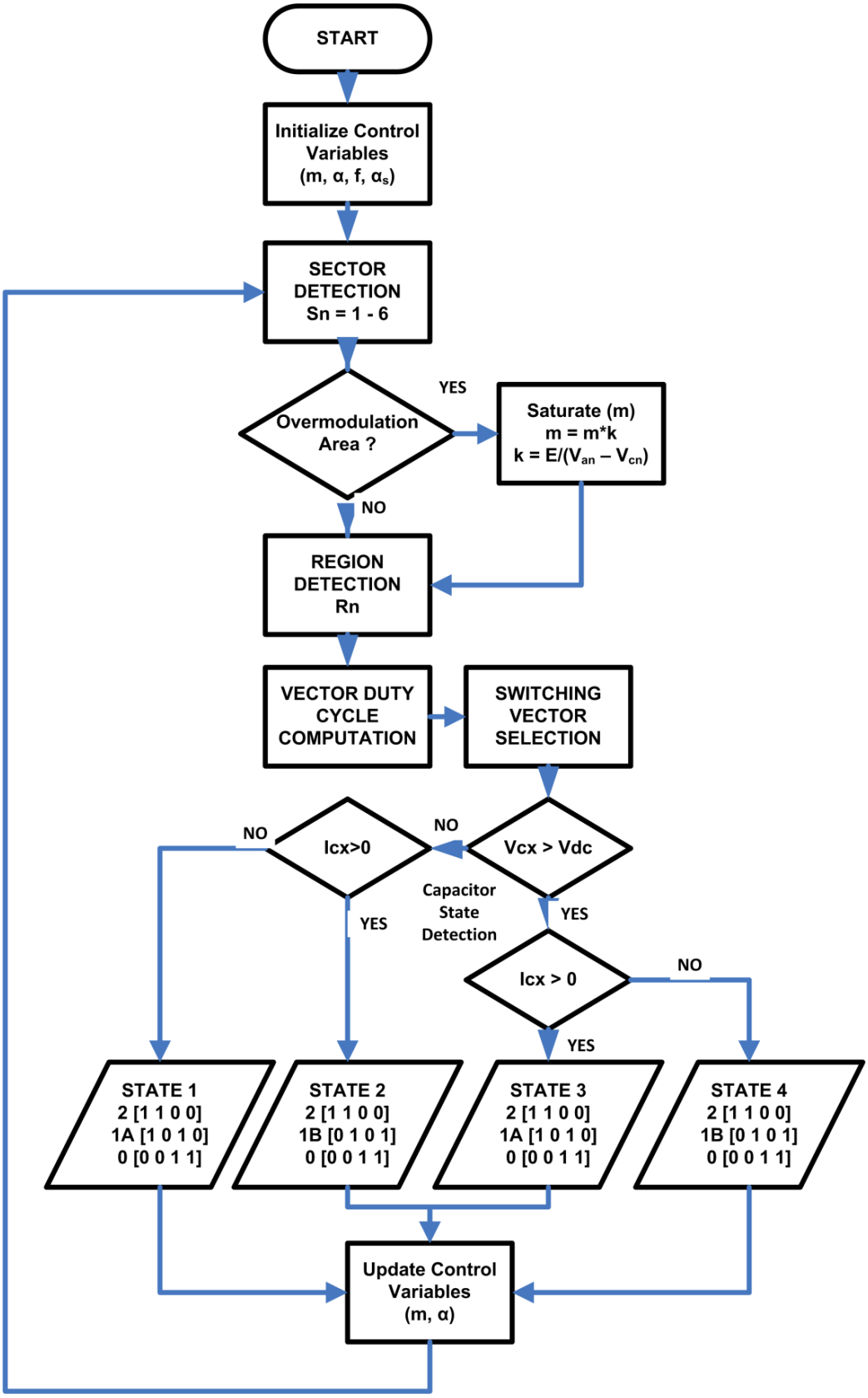


Figure 4.21: (a) Flow chart for the OH-SVM technique

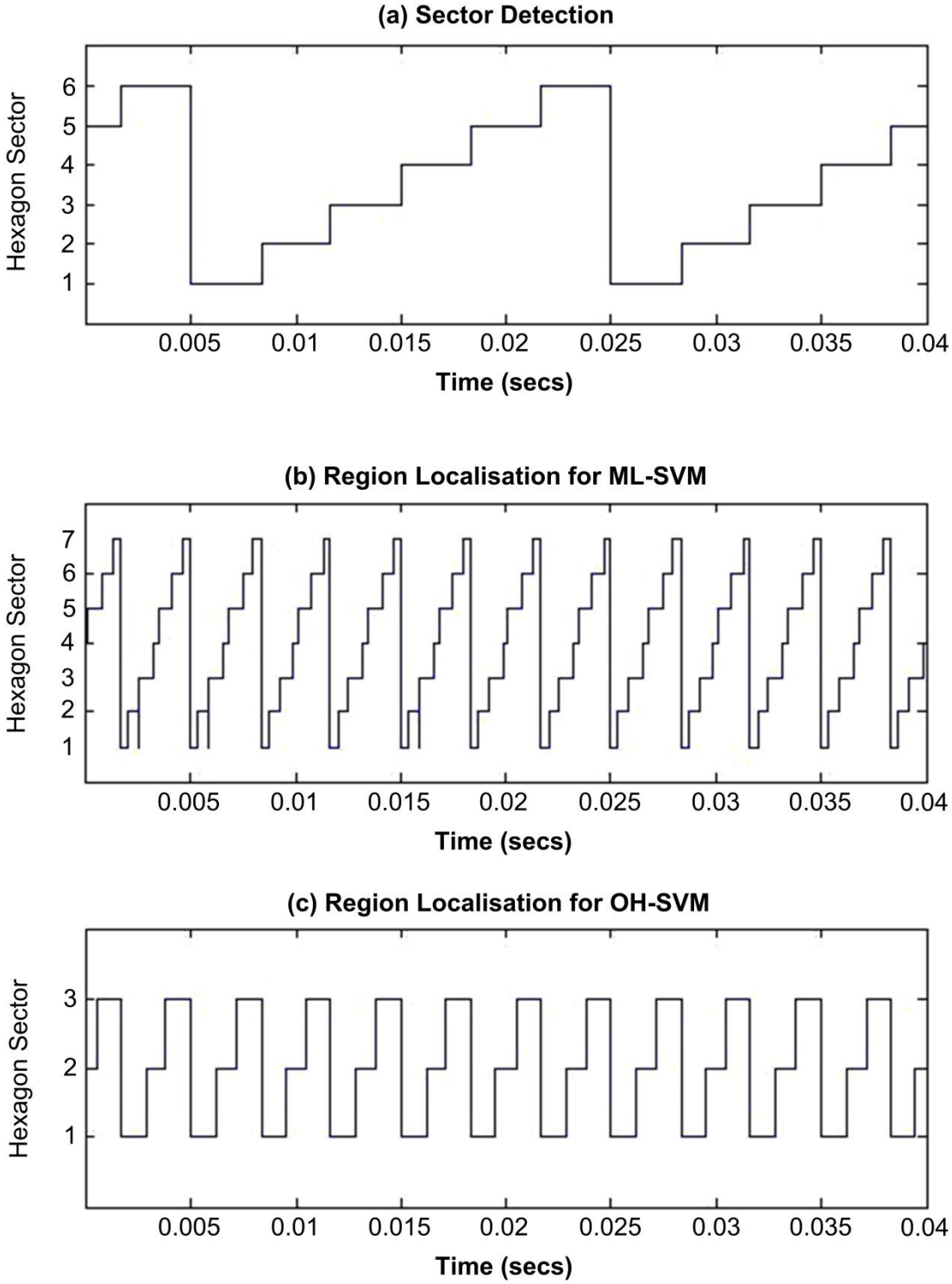


Figure 4.22: (a) Sector detection and region localisation for (a) ML-SVM (b) OH-SVM

Figure 4.22 (a) show the hexagon sector detection and is same for both the classical MLSVM and the OH-SVM. Figure 4.22 (b) shows the region detection experienced with the classical MLSVM technique. The modulation

amplitude index simulated was 0.8 so the reference vector crosses through only 7 (Region 1 to Region 7) out of the 16 regions in each sector. Figure 4.22 (c) shows the region detection for the OH-SVM technique and the reduction is complexity is evident as the reference only crosses three triangle region for the same modulation amplitude index.

The resulting converter output voltage waveform and its spectrum are shown in Figure 4.23.

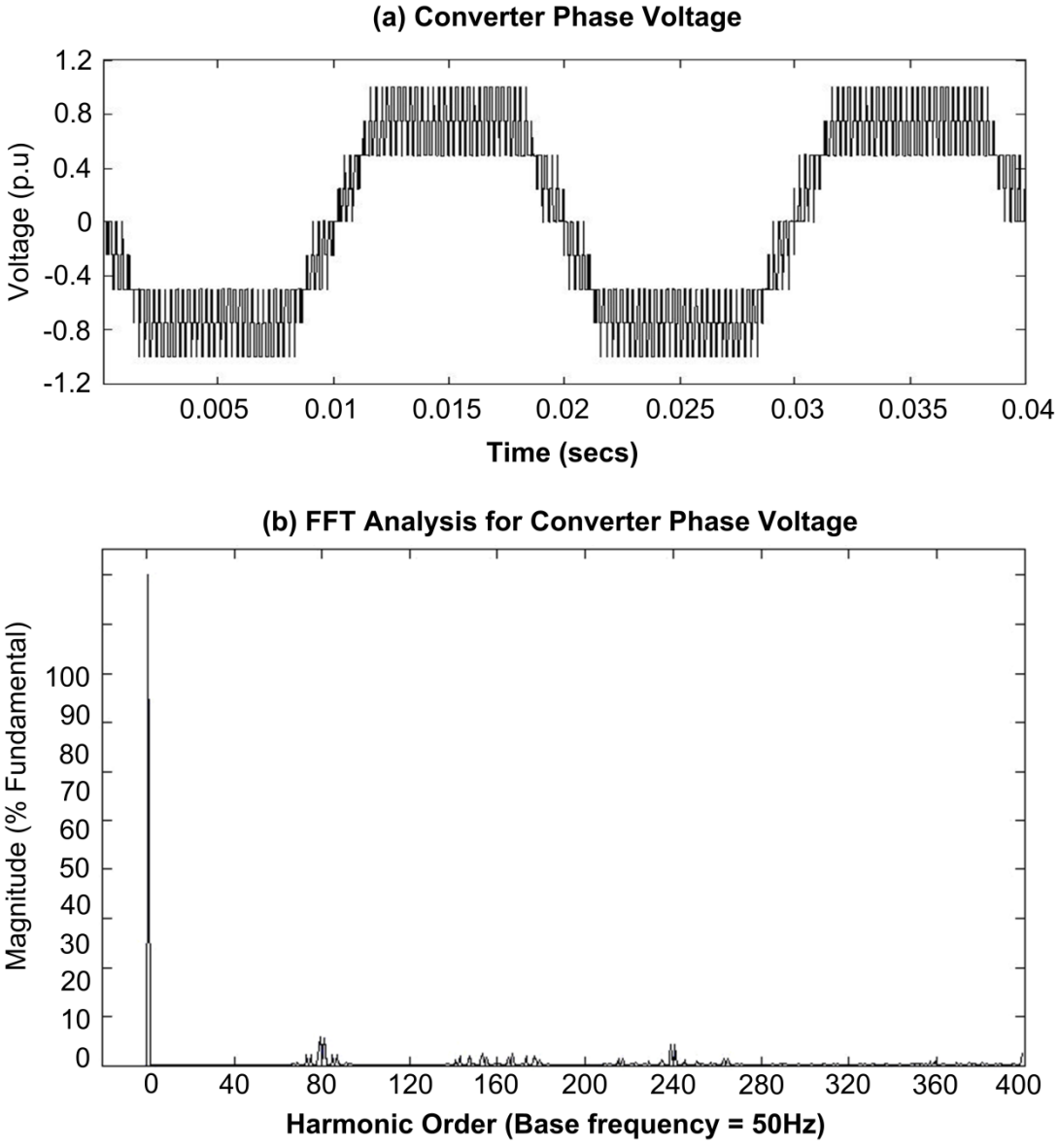


Figure 4.23: OH-SVM applied to the MMFCC. (a) converter phase voltage (b) Phase voltage spectral analysis.

4.2 Summary and Comparison of Modulation Techniques

The assessment of the different modulation schemes discussed within this Chapter is based on a set of metrics that are considered when determining the “best-fit” modulation technique for different applications. These metrics are listed below:

- Waveform performance of the Modulation technique (THD Compliance); typically the ability of the technique to yield a Total Harmonic Distortion lower than a predefined limit.
- Robustness of the Modulation technique. This metric focuses on two abilities: (1) dynamic response to changes e.g. in reference; and (2) minimal or negligible capacitor voltage variation and drift.
- Balance in switch utilisation.
- Ease of implementation (complexity) of the modulation technique.

Table 4.6 presents the comparative advantages of the different modulation schemes according to the above metrics.

In terms of the ability to target the specific harmonics to be supressed, the SHE technique makes the most fitting technique for cases where THD compliance is of higher importance than any other requirement. This scheme may be ideal in applications where loads with high harmonic sensitivity are operated for a short period of time (or discontinuously) and in open loop. It is difficult to mitigate capacitor voltage drift using SHE-PWM over continuous periods unless active balancing is integrated at the comprise of higher switching frequency.

Other situations may assign equal (or even higher) importance to the second and third metrics. For instance in a STATCOM application, the reference signal can experience several step changes within a cycle. The modulation technique is expected to immediately reflect these changes in the pulse width of switching signals as well as minimising changes in the flying capacitor voltages. The PSPWM and OH-SVM techniques are better candidates for such an application.

Finally the complexity of a modulation technique has a negative impact on both its robustness and computational cost (i.e. reliability). In this context, the use of an iterative computational process and uncertainty of convergence present a disadvantage to the SHE modulation technique. Carrier signals are easily deployed in hardware and several digital signal

processor (DSP) and field programmable gate array (FPGA) manufacturers now provide libraries with full implementation of carrier signals. This allows for easy implementation of both the PSPWM and PDPWM techniques on embedded platforms. In the case of the OH-SVM, the use of overlapped three-region hexagons makes the digital implementation of the technique easy.

Table 4.6: Assessment of Modulation techniques for the MMFCC

	SHE	PSPWM	PDPWM	OH-SVM
THD Compliance	✓		✓	
Open-loop Natural balancing		✓		✓
Dynamic Response		✓	✓	✓
Switch/Sub-module Utilisation		✓		✓
Reduced Complexity		✓	✓	✓

4.3 Summary

In this chapter different modulation options were discussed for the switching control of the MMFCC topology. The SHE-PWM technique offered lower losses but at the compromise of capacitor voltage variation, even when adaptations are made for module utilization and capacitor balancing. Amongst the carrier-based techniques, the PS-PWM offered the most optimized solution for both capacitor voltage balancing and module utilization while the SCPD-PWM was shown to overcome the capacitor variation difficulties encountered with the PD-PWM technique.

The novel OH-SVM technique was introduced and discussed. This is a significant contribution of this work. This proposed method treats the three-phase MMFCC as multiple inverters with a phase limb being a chain of basic three-level FC H-bridges. Basic three level hexagons can be applied to determine the switch states and duty cycles separately within one tier of the converter and many such hexagons can be overlapped, with phase shift relative to each other, for the control of a complete MMFCC. This approach greatly simplifies the modulation algorithm and brings flexibility in shaping the output voltage waveforms for different applications. Spectrum analysis

showed that the technique offers similar waveform quality to that of the PS-PWM scheme. In addition the OH-SVM presents an added advantage by allowing for the possibility to optimize for either losses or capacitor voltage variation.

In Chapter 5 investigations surrounding the experimental validation of the new MMFCC topology are presented.

Chapter 5
Experimental System

Experimental validation is always required in power electronics for establishing the plausibility of power electronic topologies or control techniques. In this work some modulation schemes, both carrier based and as well the overlapping multi-hexagon space vector pulse width modulation have been presented, specifically for the control of the modular multilevel flying capacitor converter. Although their operation as well as an application has been shown in simulation in Chapter 4, this chapter presents the design and implementation of a “prototype” hardware rig in order to validate some of the modulation schemes in real time.

Mainly, the set task was to achieve a properly scaled as well as a detailed hardware prototype to enable further research into the proposed MMFCC topology. To achieve this, a “modular” design methodology was adopted at all development stages of the prototype, which would allow the possibility of reconfiguring as well as uprating or downscaling the prototype to match different power levels. In effect, this would enable the investigation and validation of various control schemes for various applications.

Towards the investigative goals of this research, the developed hardware prototype will be used to present experimental results for the modulation control of the two module MMFCC topologies using one carrier-based PWM scheme (phase-shift PWM) as well as the proposed overlapping multi-hexagon space vector modulation scheme.

Although the design of the hardware rig was at the University of Leeds control and power applications (CPA) laboratory, the implementation stage was split across two locations. Power hardware implementation was at the Leeds (CPA) laboratory, while the control and measurement systems were developed and deployed at the University of Nottingham Power Electronics Machines and Control (PEMC) laboratory. Due to the high safety standards as well as strong HSE guidelines and presence at both facilities, the rig was developed in the safest manner as was economically viable. Within the design and implementation of the rig were voltage and current threshold/peak monitoring and detection circuits to handle scenarios such as: over current automatic shut-down; and over voltage shutdown

Most of the protection was implemented using latch circuits in order to create a “hold until clear” option for the fault scenario even if the control circuit power supply was removed.

Owing to the number of semiconductor switching devices (48 IGBT’s) to be controlled as well as other control signals to be generated (independent enable/disable, reset, etc), a single digital control platform could not be adopted. A distributed control platform was implemented which includes a central Digital Signal Processor (DSP) and a cascade of Field Programmable Gate Array (FPGA) cards which provided sufficient processing capabilities as well as memory to handle the computation of some of the complex control algorithms and PWM signal generation schemes required for the operation of the hardware rig. In the sections following, an overview is presented for the MMFCC hardware rig development, showing the interconnection of the different subsystems of the hardware rig. The procedure for rig testing operation and experimental results obtained are then shown. An outline of the hardware rig is shown in Figure 5.1.

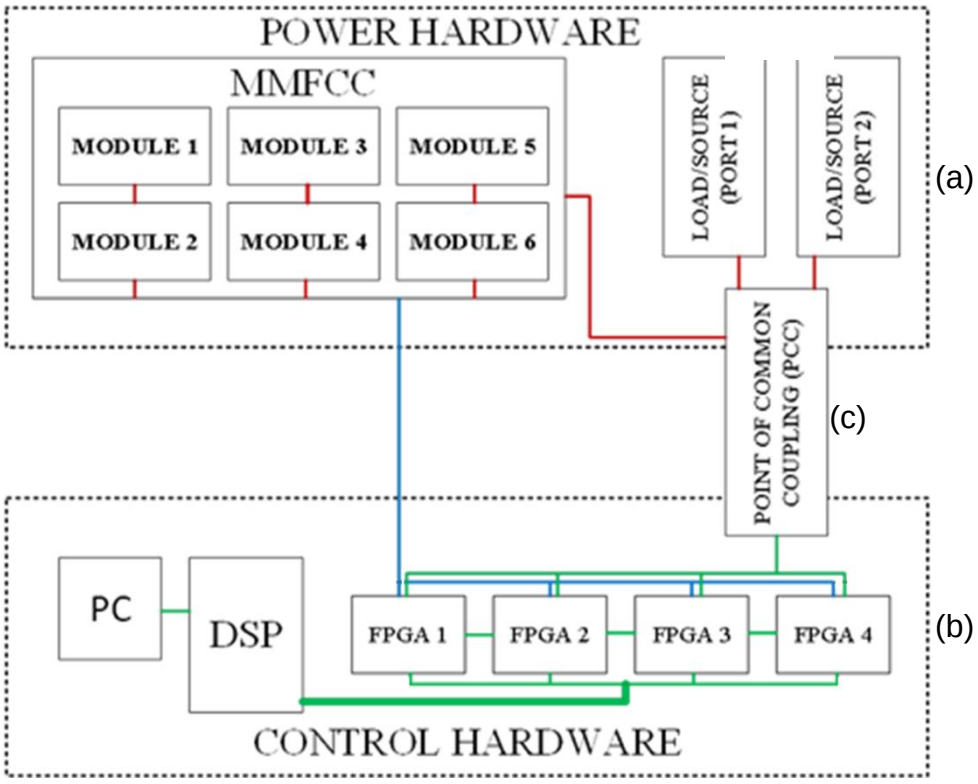


Figure 5.1: Hardware rig outline showing (a) Power Hardware (b) Control Hardware (c) PCC. Legend: Red – Power line, Green – Digital line, Blue – Fibre optics

5.1 Power Hardware

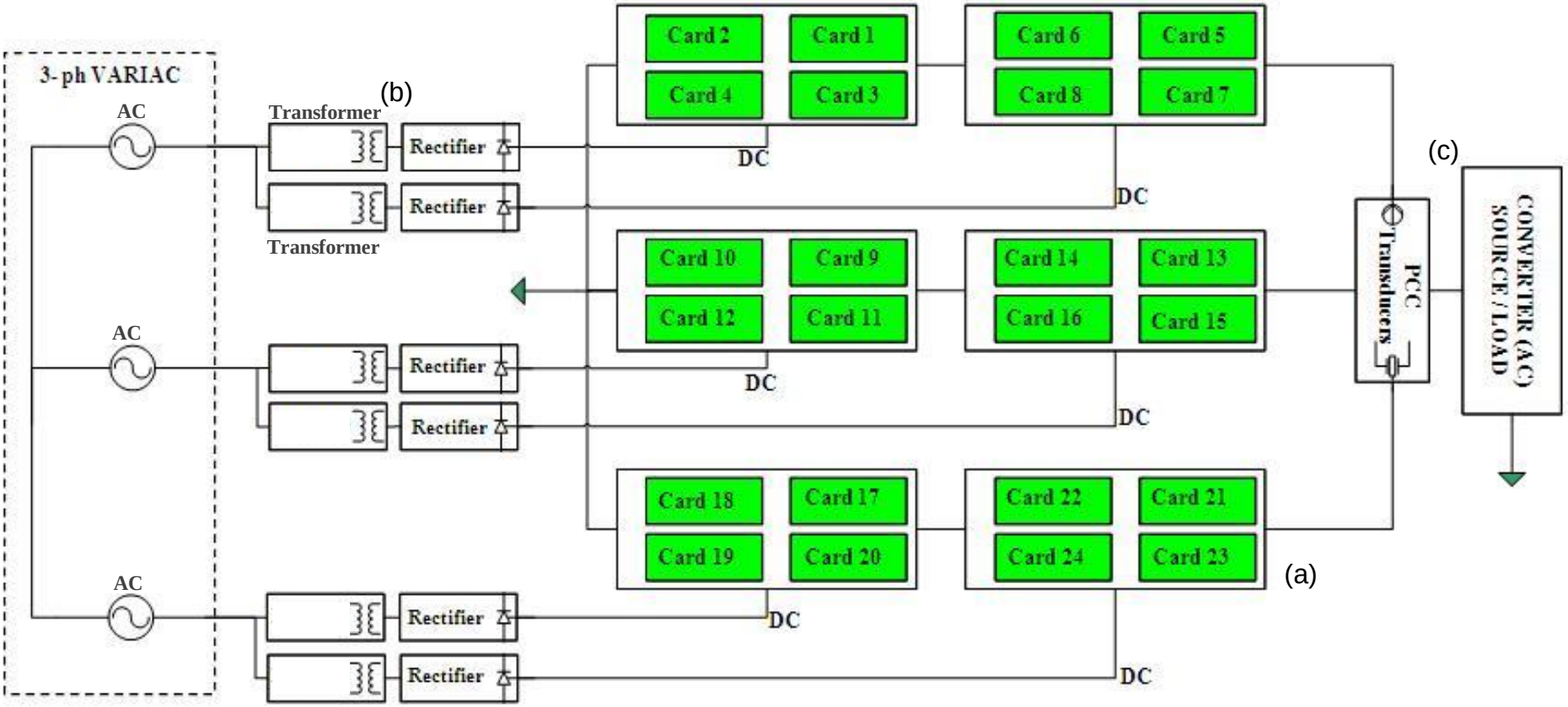


Figure 5.2: Rig Power Hardware showing (a) FCC Module (b) Isolated DC Supplies (c) AC Line/Load connection.

In Figure 5.2 the experimental rig power hardware is shown to mainly comprise of the 6 FCC modules (Figure 5.2 a) which make up the MMFCC topology, the isolated DC power supplies (Figure 5.2 b) which were required to sustain the module DC busses in open loop, while the modulation schemes were evaluated and the finally line/load connection (Figure 5.2 c).

Three standard laboratory power supplies capable of producing two isolated sources each (i.e a total of six isolated sources) were available and sufficient to be deployed as the isolated power supplies. A half bridge circuit was implemented as basic building block for the FCC modules and during this work this is referred to as the “power cell card”. Each FCC module was built up using 4 power cell cards. To form each converter phase leg, two FCC modules are connected in series, with the top terminal serving as a phase output, while all three bottom terminals are tied to form a common neutral terminal.

The phase outputs of the converter are connected to a three phase R-L load, via current transducers and across voltage transducers, for data acquisition purposes.

With regards to power system rating, the experimental tests were performed with a 2kW (2 – kilowatt) threshold (i.e 200 Volts, 10 A). The description of the power cell card is as shown in Figure 5.3.

5.1.1 FCC - Power Cell Card

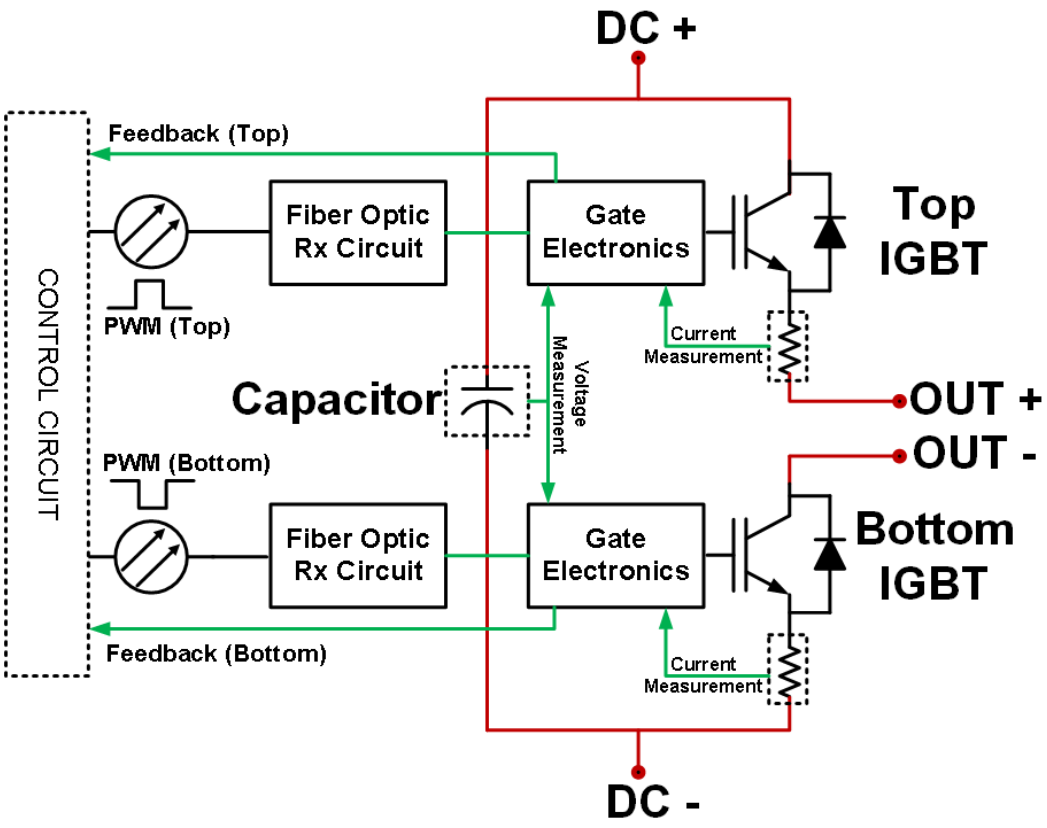


Figure 5.3: Power Cell Card (Red = Power line, Green = Signal Line).

In order to implement the Power cell card for the FCC module, the cell card circuit designed as a result of work presented in [101], was modified to that shown in Figure 5.3.

The main power components in each power cell card are the card capacitor deployed using Panasonic's EETED2E152EA, and two Infineon Power IGBT devices (IKW30N60T), rated at (600 V, 30A).

Fibre Optics Receiver Circuit

Although a one modification was the inclusion of a voltage "latch" protection circuit, the main modification which resulted to the power card circuit in Figure 5.3 is the use of optical fibre which provided enhanced isolation with no sacrifice to the signal link performance.

A pair of Fibre Optic receiver circuits are built to plug into the Power cell cards in and convert the optical PWM signals from the control circuit into digital (0 – 5V) signals.

The main component in the Fibre Optics receiver circuits was Avago's HBFR-2531 horizontal-mount Fibre optics receiver which connects to the optical PWM signal as shown in Figure 5.4.

Note that the Fibre optic receiver output is coupled via an inverting Schmitt Trigger. This is required in order to counteract the inversion which takes place at the Fibre optics transmitter circuit (located at the control side).

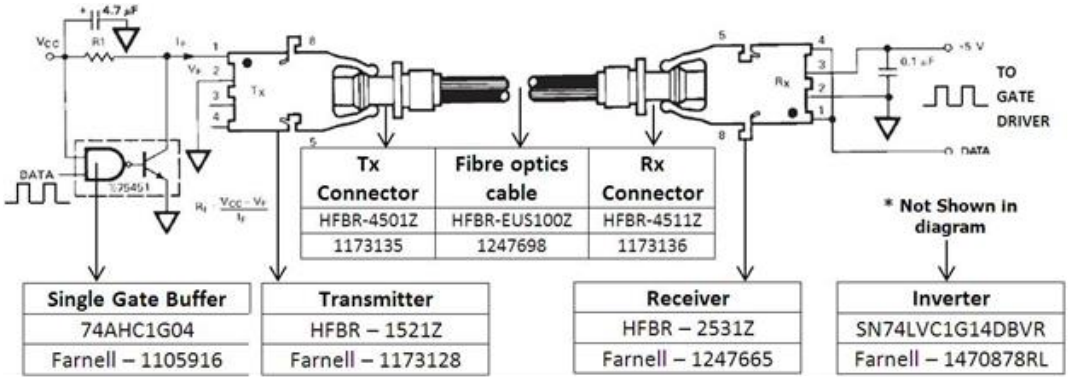


Figure 5.4: Fibre Optics Circuit.

The circuit shown in Figure 5.4 was implemented on a printed circuit board based on the schematic shown in Figure 5.5 and is as-built in Figure 5.6.

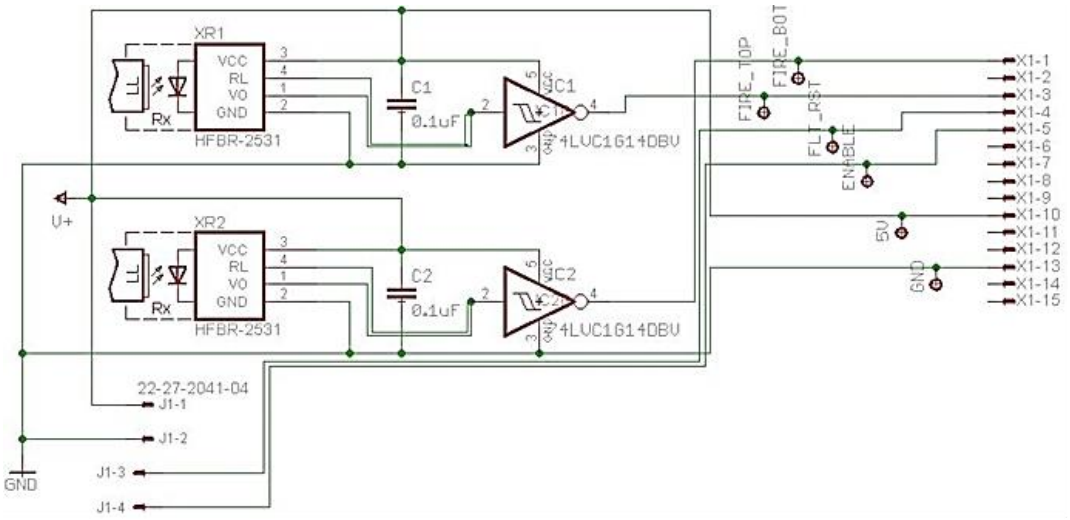
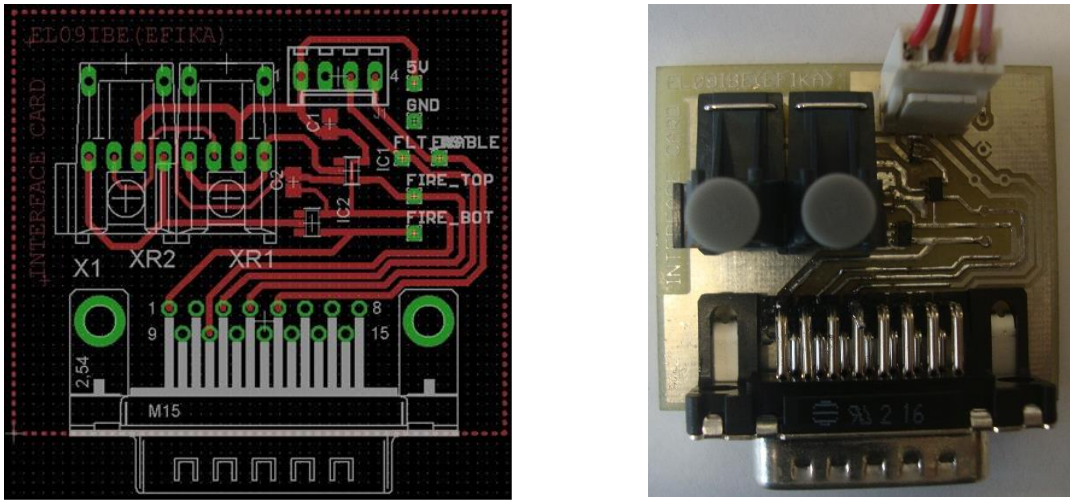


Figure 5.5: Schematic for Fibre Optics Rx Circuit PCB.



(a) (b)

Figure 5.6: Fibre Optics Rx Circuit showing (a) PCB design (b) Populated Circuit.

Gate Electronics

The Gate electronics circuit comprises of the following:

- A gate drive circuit which is present to provide sufficient turn-on current to its interconnected power IGBT device.
- Power card feedback circuits which acquire current and voltage values present on the power components on the cell card, and present then to the controller as feedback signals as well as to the protection circuits for low-level protection decisions.
- Protection circuits, which constantly compare the voltages and currents presented on the power cell card components to set threshold values. If a value is detected over the threshold, the firing signals to the power card are latched to ground and the fault state is held until a reset signal is used to clear the fault (even if the cell card loses its power supply).

A simplified schematic of the gate drive circuit from [101] is shown in Figure 5.7.

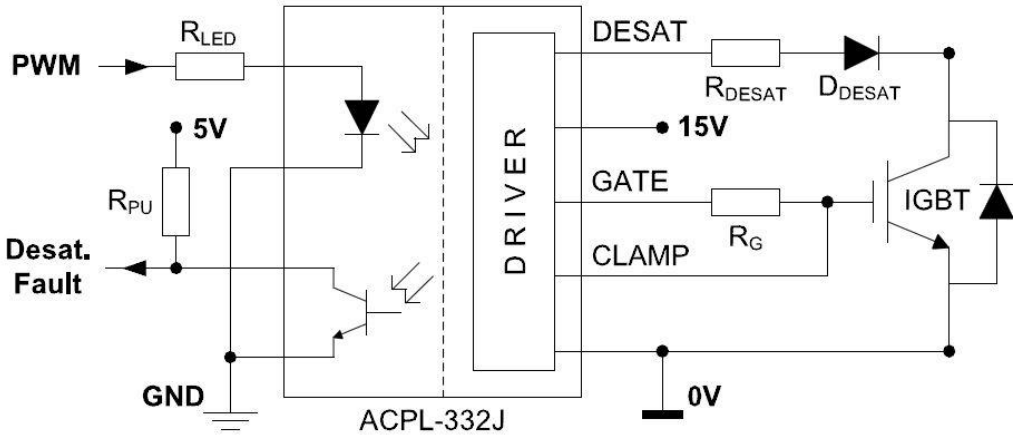


Figure 5.7: Power cell card – Gate drive circuit.

Even though optical isolation is implemented to segregate the power cell cards from the control circuit, the gate drive circuit shown in Figure 5.7 implements an opto-coupler circuit alongside the gate driver circuit. This extra galvanic isolation serves the purpose of preventing noise from coupling from the measured analogue feedback signals across to the digital (control PWM signals). The gate driver on the other hand, provides sufficient gate conduction current to enable the power IGBT device.

Both circuits were available on a single (ACPL-332J) IC package by Avago Technologies which also presented some extra functionality namely “Miller clamping” and “Desaturation detection”. The Miller clamping feature provided an alternative path for current present due to parasitic Miller capacitance to flow, hence preventing unscheduled IGBT power device turn-on. On the other hand, in order to implement the desaturation detection, the collector-emitter voltage of the power IGBT devices are constantly monitored and compared with a predefined threshold. If the monitored value exceeds the threshold value, a fault state is declared and the current flowing thorough the IGBT device is made to decay slowly.

A common 5 volts supply, provides power to the opto-coupler section of the gate drive circuit as well as the fibre optics receiver circuit, while isolated 15 V power supply circuits were implemented to power each gate driver. This circuit is shown in Figure 5.8.

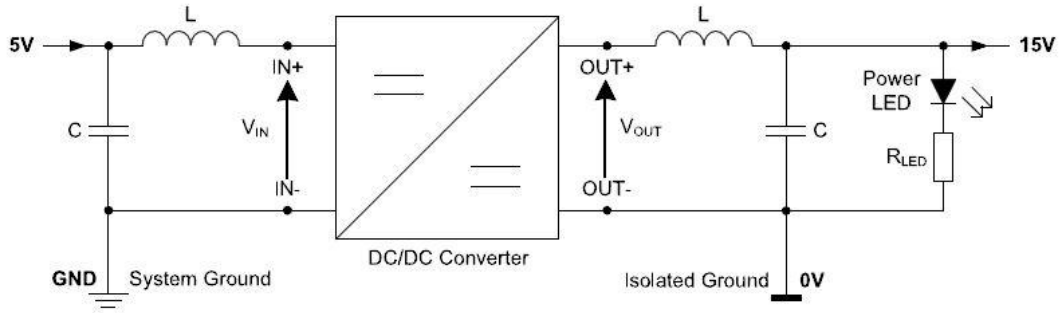


Figure 5.8: Isolated power supply for gate driver.

The isolated power supply shown in Figure 5.8 was implemented using a 1W switch mode DC-DC converter in a self-sustained IC package while an LC (low-pass) filter with the values (L = 1µH, C = 4.7µF) is connected across the output of this package for filtering purposes.

A total of 24 cell cards were built in order to create the six FCC-Power Modules required for the converter topology. After each FCC cell card design was verified and the hardware built, basic testing was carried out to ensure cell operation. Results from a test of one of the cards is shown in Figure 5.9.

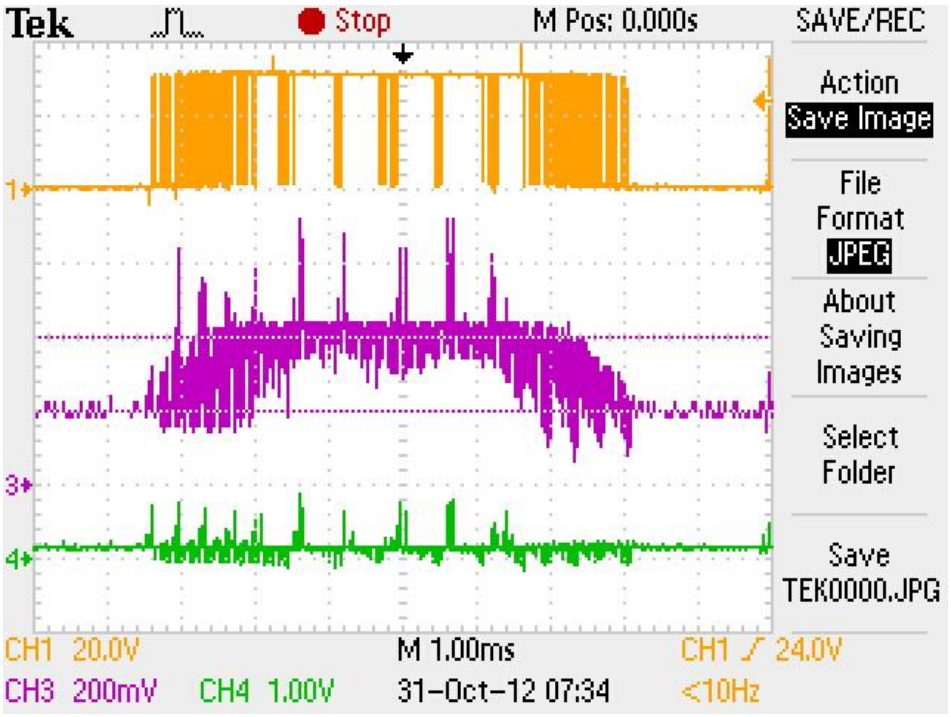


Figure 5.9: Sub-system testing at reduced voltage performed on power cell card to ensure functionality. Channel 1: Cell Card Voltage; Channel 2: Cell Card current; Channel 3: Current flowing through cell card capacitor.

In the test result shown in Figure 5.9, the power cell card was connected in a 2-level half-bridge inverter circuit configuration and switched using space vector PWM pulses at a switching frequency of 2.0kHz. This was done as a sub-system type test to ensure proper operations. Starting from the top, the first waveform (orange; measurement scale: 1 division = 20 V) shows the AC voltage output from power cell card (terminal OUT+ and OUT- in Figure 5.3). The second waveform shows the current measured at the top power IGBT device (measurement scale:1 division = 2A), while the third waveform shows voltage across the power cell card capacitor (measurement scale: 1 division = 100V). Consequently, the cell cards were initially tested for functionality at (30V, 2A).

The power cell card (as-built) is as shown in Figure 5.10.

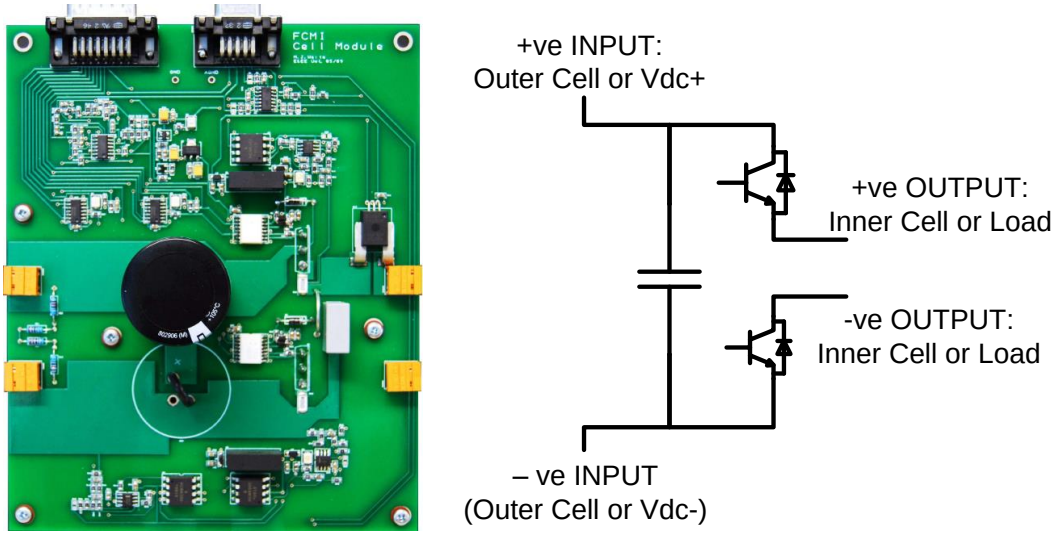


Figure 5.10: Power cell card(as-built).

FCC - Power Module

Using the power cell card as the basic building block, the FCC module structure was built as a cascade of power cell cards, with 2 cards stacked in series to form each FCC module bridge leg, and two legs are connected in parallel to form the FCC full-bridge module. This is conceptually represented in Figure 5.11.

On each power cell card, the two power IGBT devices present, are mounted on Fischer Elektronik SK105 heat sink, capable of dissipating 1.9^0C of heat per watt. This ensures that the IGBT devices retain their recommended temperatures even while the circuit is operated at the maximum rating.

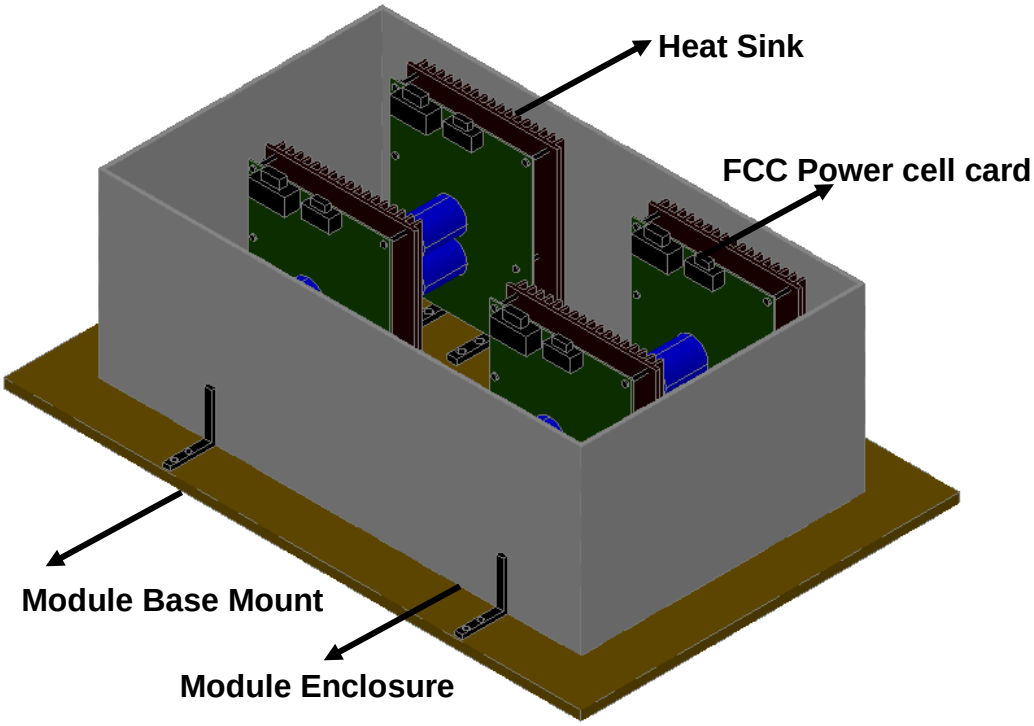


Figure 5.11: FCC Power module.

Careful consideration was given to heat flow to enable the heat dissipated by the heak sinks to escape, while preventing external materials entering into the module enclosure. To achieve this, the heat vents are available on the module enclosure top and sides in a pattern which encourages the hot air within the module enclosure to rise and escape, subsequently causing cool air from the surrounding to make contact with the heat sink fins during the air exchange.

The module enclosure was implemented using Perspex material. Laserscript 3.0 was used to design the enclosure faces and the design files generated were exported and cut on a laser machine. Figure 5.12 the final product of two modules which were used to form one the MMFCC topology phase legs.

The three legs which make up three phase MMFCC topology was built as shown in Figure 5.13. This system consisted of 24 power cell cards in total (i.e 48 IGBT devices). The system 3-ph rating is (4.15 kV, 30 A) in star configuration or (4.15kV, 17.3 A) in delta configuration.

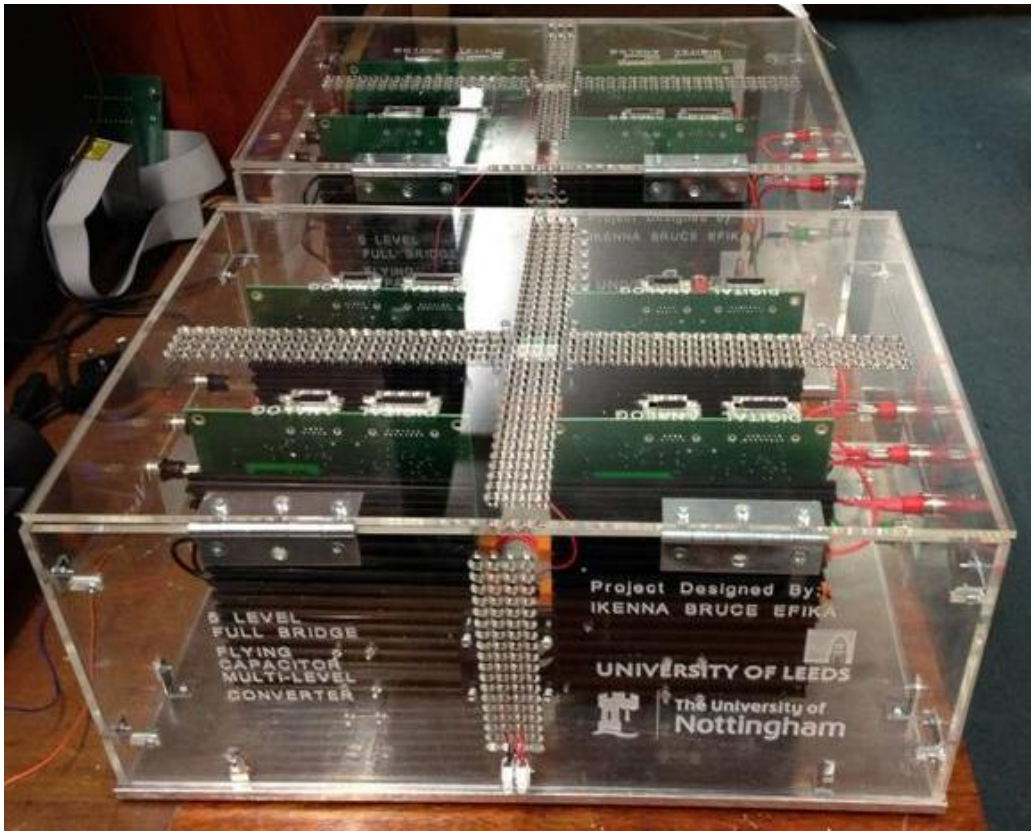


Figure 5.12: FCC Power modules.

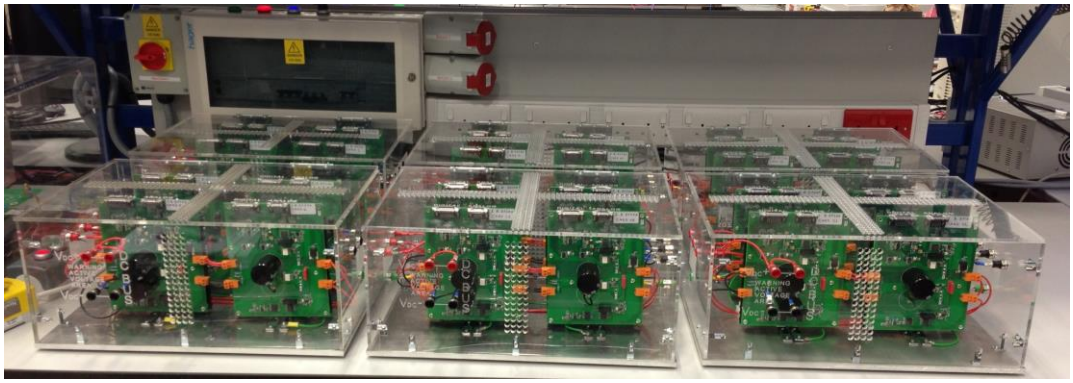


Figure 5.13: 3-Phase MMFCC circuit (as-built).

A schematic of the FCC Power module is shown in Figure 5.14.

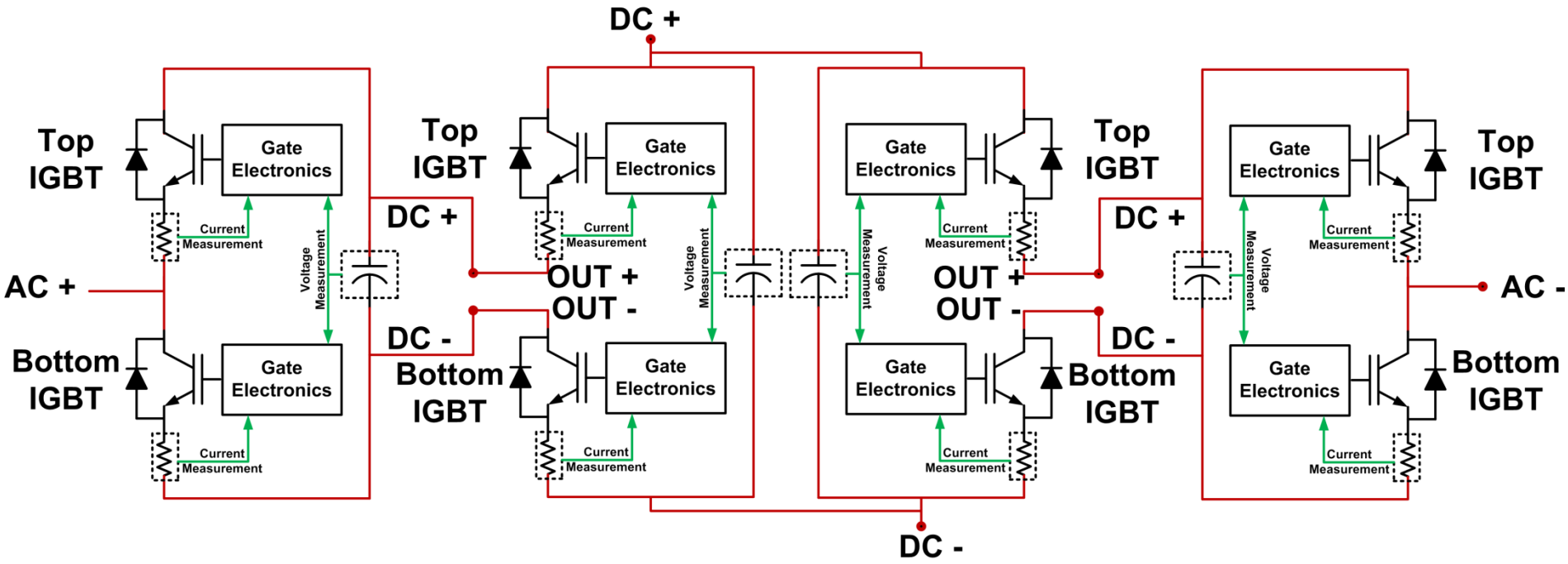


Figure 5.14: Schematic of FCC Power module setup.

5.2 Control Circuit

To meet up with the computationally demanding requirements posed by the converter circuit. A control circuit consisting of a PC, digital signal processor (Texas Instruments TMS320C6713 DSK) and 4 Field Programmable Gate Arrays (Actel ProAsic III FPGA cards), was deployed. This enabled the control setup to achieve required tasks such as:

- Generate switching commands for different converter modulation schemes.
- Capture, process and store system operation data (voltage, current, etc.) under different operating scenarios.

5.2.1 PC

A personal computer running the Microsoft windows 7 operating system is used as the “highest” level controller. It is used to house the following software applications which enabled the deployment of code for and to the lower level controllers (DSP and FPGA cards).

- Texas Instrument’s Code Composer (DSP)
- Actel’s Libero (FPGA cards)
- Educational DSP (DSP – HPI Card)

Note that due to compatibility issues which were mainly based on port driver requirements for the DSP’s Host Port Information (HPI) daughter card, a virtual machine running the Microsoft Windows XP operating system was run simultaneously to execute the code composer and HPI- Education DSP software.

5.2.2 Digital Signal Processor – TMS320C6713

The digital signal processor deployed in this control circuit is the Texas Instrument TMS320C6713 development kit. Being a member of TI’s (C6x) family of processors, it is a special-purpose floating point microprocessor with an Harvard architecture and specialized instruction set appropriate for applications which present numerically intensive targets. Its ability to swap

between different endian modes also makes it attractive and flexible for different cascade control implementations.

The three main features which made the TMS320C6713 microprocessor an assailable choice for the system requirements are:

- Multiple Accumulate (MAC) operation and Multiple execution units which enable the DSP execute more than one accumulate and multiply operation in a single instruction cycle. This proved very useful while implementing the overlapping multi-hexagon space vector pulse-width modulation, which required the evaluation of some matrix and vector algebra.
- Flexible and Efficient memory allocation. The TMS320C6713 presents the ability to access several memory locations within one instruction cycle. This proved very useful for the converter controller.

A block diagram showing an overview of the TMS320C6713 DSP is presented in Figure 5.15 while the actual board diagram is shown in Figure 5.16.

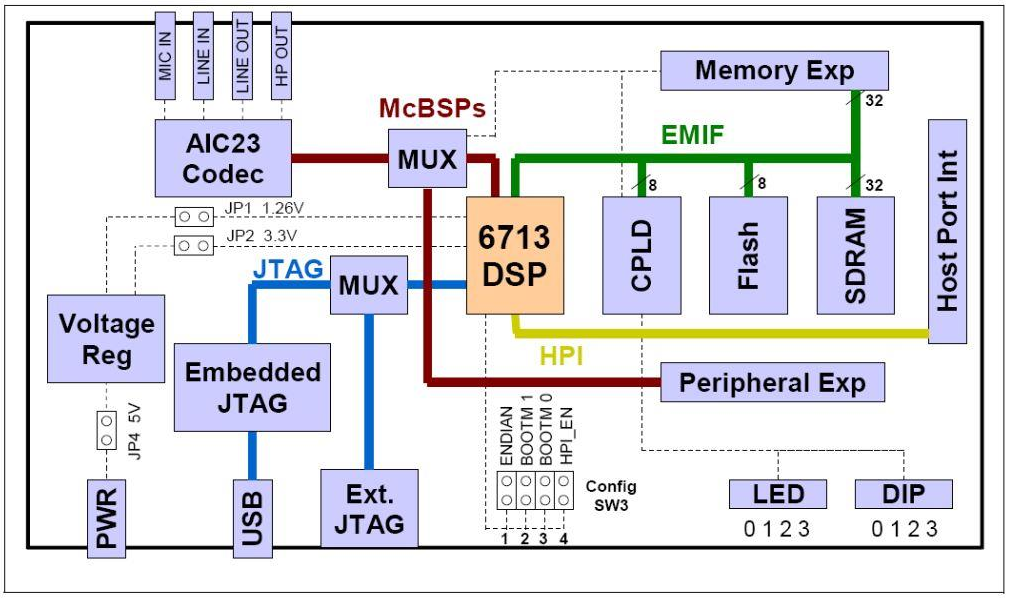


Figure 5.15: Block diagram for TMS320C6713.

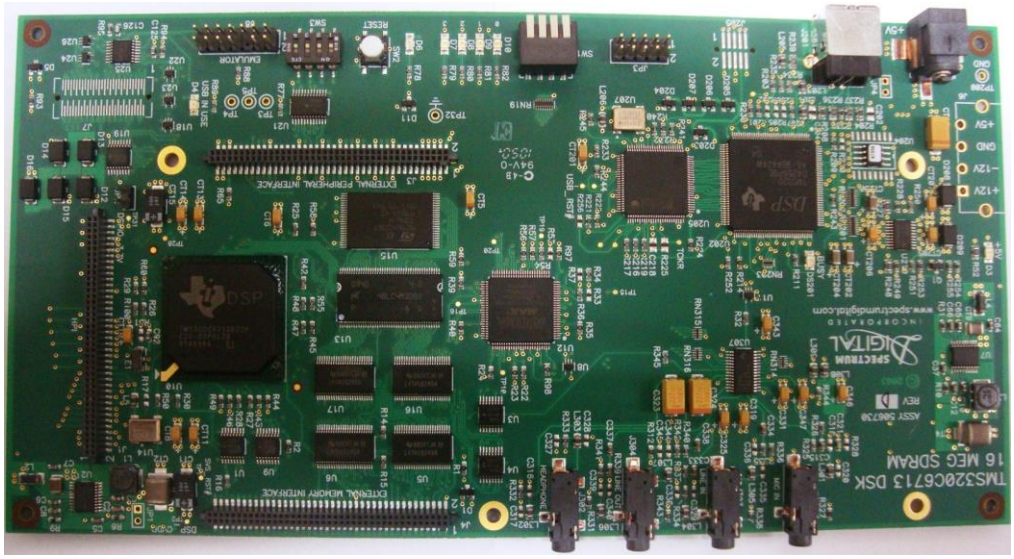


Figure 5.16: Board diagram for TMS320C6713.

The C6713 is a high speed floating point processor which runs at 225MHz and can perform up to eight operations per cycle. One of the major advantages of employing the C6713 DSK is linked to its peripherals and the ability to add external peripherals. Above all the external memory interface (EMIF) which not only supports 16Mbytes of on board SDRAM memory, Flash ROM, I/O port but also expands the memory interface through an expansion memory interface connector for a FPGA daughter boards.

5.2.3 FPGA Cards

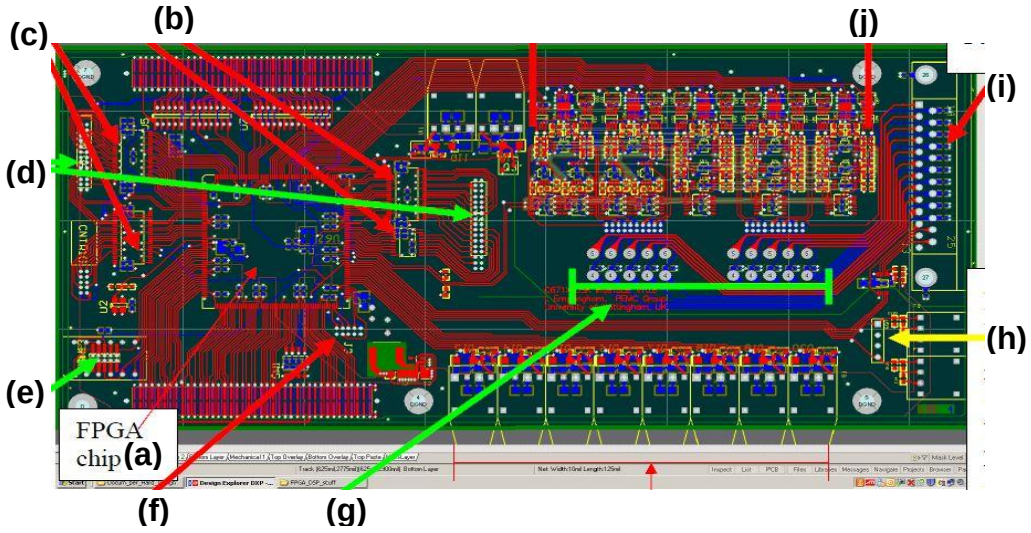


Figure 5.17: Board diagram for FPGA Card.

The FPGA card (shown in Figure 5.17) "sits" on the external memory interface of the TMS320C6713 DSP. The FPGA card (also termed the daughter card during this work), is programmed to link to the address and data buses of the DSP and occupyies the memory address 0xA0000000. However access is provided to only a limited number of bits in the address to avoid excessive use of DSP memory by the FPGA. In this work, only 8 – 14 bits of the mentioned address space is used for addressing the FPGA together with CE2.

The board diagram shown in Figure 5.17, comprises of the following components as listed:

(a) The FPGA chip (Actel's ProASIC III)
(b) Bidirectional Buffers 3x74LVC16245A and 1x 74LVC245A by Philips.
(c) Bidirectional Buffers 1x 74LVC245A by Philips.
(d) High density 26 –pin SAMTEC header connector for I/O.
(e) LED Display for visual feedback on the Fault signals
(f) 10-way FPGA programming connector
(g) Burden resitors for Analog to Digital (A2D) converter lines (±5V)
(h) 4-way SAMTEC molex header for transmitting fault clear (RESET) and (ENABLE) lines.
(i) 25-way D-type connector for A2D input signals (from PCC0
(j) 10 A2D converter chips

From a functional point of view, the FPGA card receives calculated variables and set-points from the DSP through the data and address busses on the EMIF and generate switching signals by means of digital counters implemented in the FPGA chip which may be used to emulate triangular carriers (as in carrier based PWM) or to generate switching interrupts based on vector timing intervals (such as is required in space vector modulation).

The A2D converter shown in Figure 5.17j, has a 12 bit resolution, however 2 bits are sacrificed to eliminate noise from the measurements. This provided sufficient resolution space. For instance while measuring and translating a ±200 Volt signal from analogue to digital form, yields a (100mV:1bit) resolution.

Generating Switching Signals

As earlier discussed, two different digital techniques were applied for the generation of switching signals based on different modulation schemes.

For carrier based PWM, up-down counters are utilized on the FPGA chip to produce the carrier (or carriers) required to compare with DSP generated reference signal. For instance in PS-PWM. The carriers are initialized with different integers values in order to introduce the different phase shifts. This is described in (86)-(87) as well as in Figure 5.18.

$$UPLIM = \frac{F_{CLK}}{2 \times F_{CARRIER}} \qquad \textbf{5.1}$$

$$CARR\_INT(N) = \frac{(N-1).UPLIM}{(N_C)} \qquad \textbf{5.2}$$

In (5.1), UPLIM is an integer value, equivalent to 1.0 p.u on the carrier wave, while in (5.2) CARR_INT defines the different initialization integers for the different carriers. For instance according to (5.2), for four carriers, the 1st carrier will have a CARR-INT of “0” (i.e phase-shift = 0), while the second carrier will have a CARR_INT of “UPLIM/4”. This is illustrated in Figure 5.18

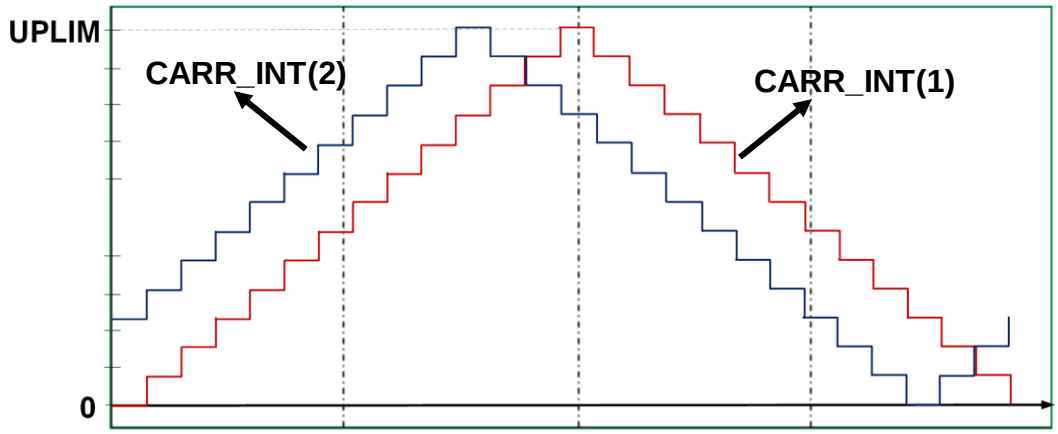


Figure 5.18: Carrier Based Signal generation on the FGPA Card.

The second method (shown in Figure 5.19) is well suited for discrete and vector-based PWM schemes such as SHE-PWM or Space vector modulation. The code involved within this technique is mainly interrupt based and facilitated by a FIFO digital system implemented on the FPGA chip.

The FIFO “First In First Out” memory block implemented on the FPGA chip is made of a parallel cascade of two 16 bit memory blocks. A main counter generates interrupt signals at the rate of the desired switching frequency. At each interrupt, two bits are read into the FIFO block simultaneously as they are read out. The first bit is a switching state, while the second is the switching time. Note that the DSP provides the inputs for the FIFO block.

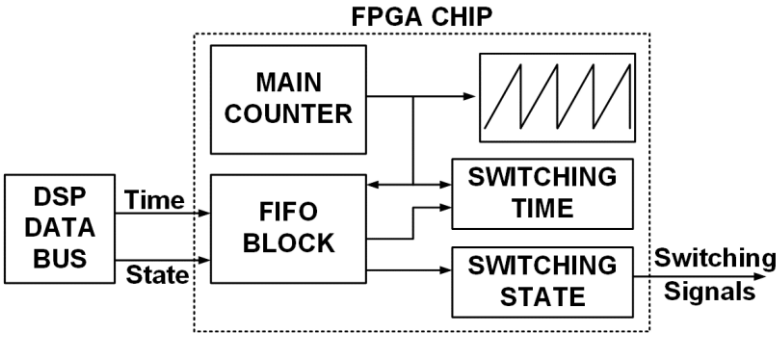


Figure 5.19: Discrete signal generation on the FGPA Card.

5.3 System testing

5.3.1 System Setup

The phase-shift PWM and OMH-SVM scheme proposed in Chapter 4 were tested on the experimental rig for operational validation. The experimental system parameters used during the test are listed in Table 5.1.

Table 5.1: Experimental system parameters.

Parameter	Value
Type of MMCC configuration	Series Star – FCC based
Number of modules (per phase)	2 (Total = 6 modules)
Converter rating	400 Volts pk-pk
Flying Capacitors	560µF, 400 V
Load	R-L (12.6.6 Ω, 3mH)

The layout of the experimental setup is shown in Figure 5.20 while the actual test setup shown in Figure 5.21.

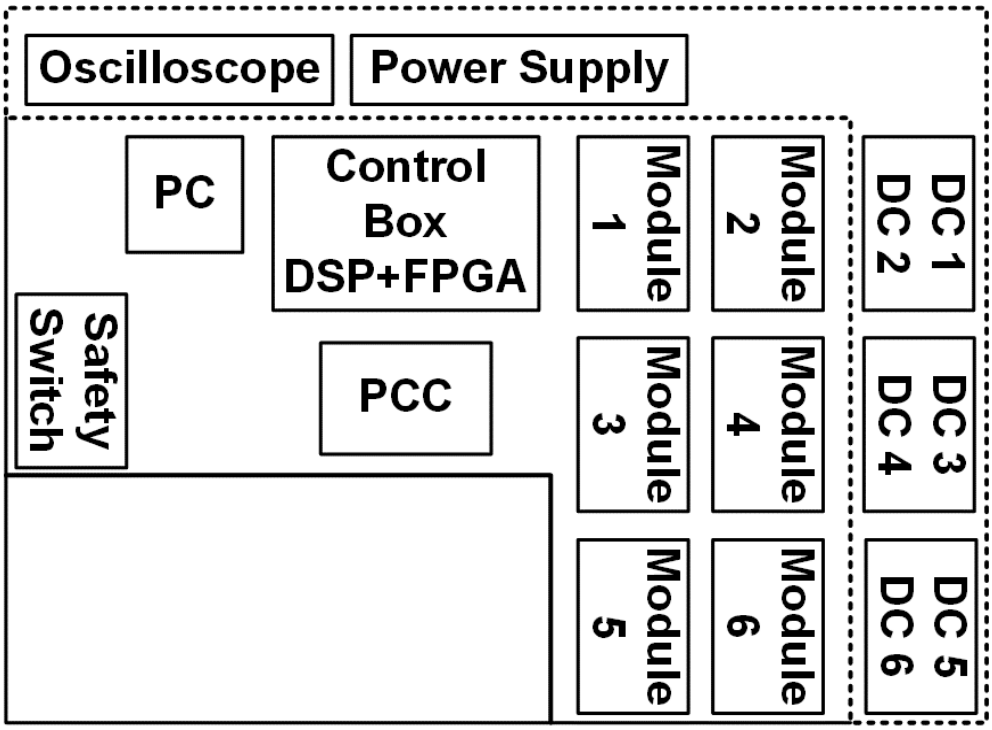


Figure 5.20: Layout of Experimental Rig.

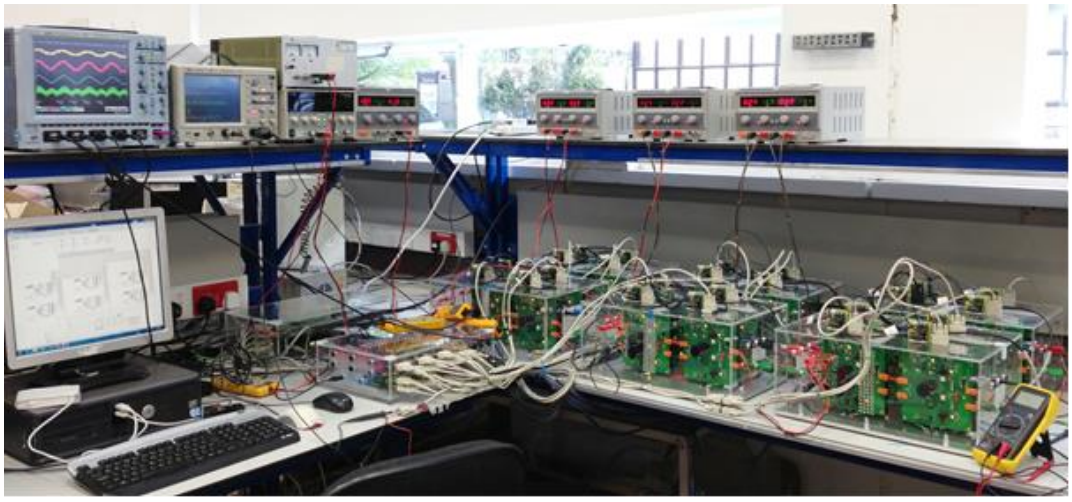


Figure 5.21: Photograph of Experiemental Rig.

5.3.2 MMFCC Test Results

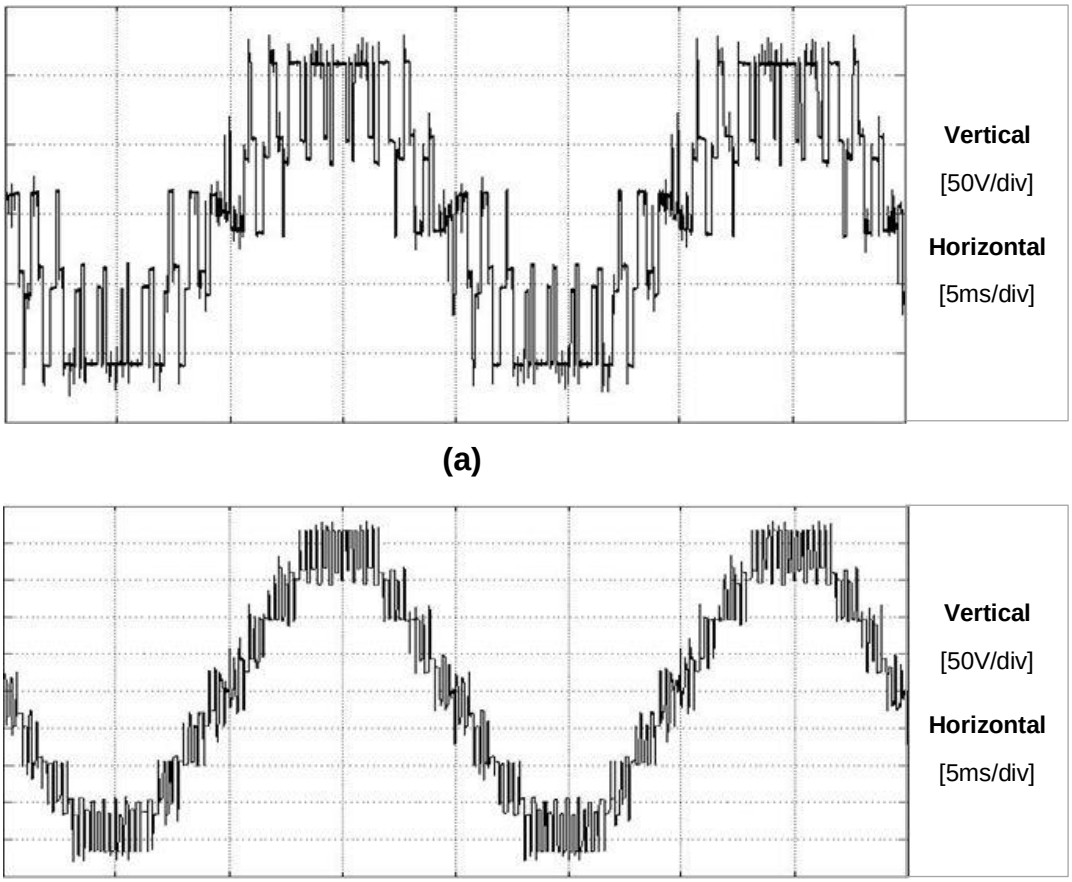


Figure 5.22: MMFCC PSPWM - Phase (a) Module Voltage (b) Arm Voltage.

First using the phase-shift PWM scheme, the MMFCC output voltage waveforms for Phase A are acquired as displayed in Figure 5.22. Note that experiments were performed under balanced phase conditions, hence phases B and C are identical with A with only the only difference being the 120^0 and 240^0 phase shift.

In Figure 5.22(a), the FCC module voltage waveform is displayed and as expected presents 5 voltage levels (peak to peak) or 3 voltage levels (with respect to the module DC bus midpoint (0 Volts). Figure 5.22(b) presents an MMFCC arm voltage for Phase A which was observed to comprise of 9 voltage levels (-200V, -150V, -100V, -50V, 0, 50V, 100V, 150V, 200V). It is evident from the module voltage in Figure 5.22(a), that the flying capacitors voltages are balanced with only negligible voltage deviations (approximately 0.15 Div), even at the low switching frequency (250 Hz) used.

The voltage waveforms were modulated to emulate a 50 Hz (20ms) sinusoidal AC voltage waveform which is suitably so, as seen in both waveforms in Figure 5.22. Generally, the properly defined and distributed voltage levels displayed in Figure 5.22 signify good performance which can also demonstrated by the current waveforms shown in Figure 5.23. Clearly the current harmonics have been filtered by circuit inductance. Information on voltage harmonics is illustrated in Figure 4.14 and Figure 4.23.

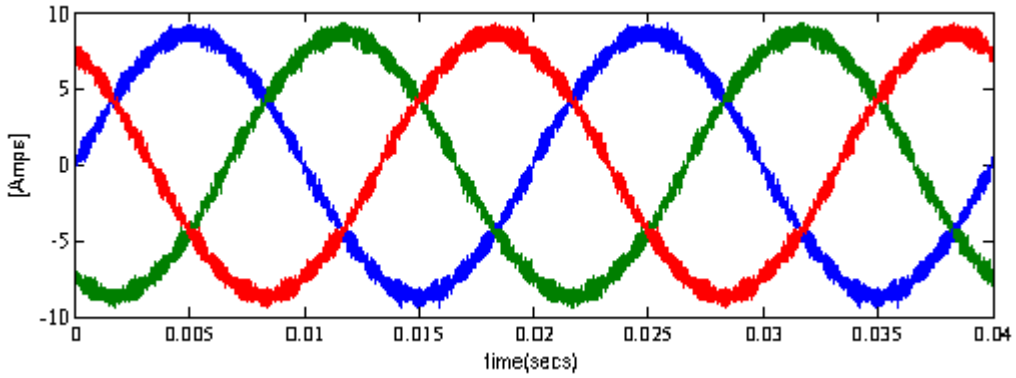


Figure 5.23: MMFCC PSPWM - Phase Current.

Next the OMH-SVM scheme was programmed to be tested on the experimental rig using the same power input and load setup. However for data acquisition purposes, Educational DSP's winDSK kit had to be deployed in order to capture variables from the DSP, rather than from the oscilloscope.

Figure 5.24 displays the flowchart adopted for implementing the OMH-SVM scheme.

The values observed during the experiments were captured, stored and plotted using Matlab's enhanced plot functions. Figure 5.25 shows plots for the Sector and Region selection variables on the DSP and Figure 5.26 shows voltage waveforms.

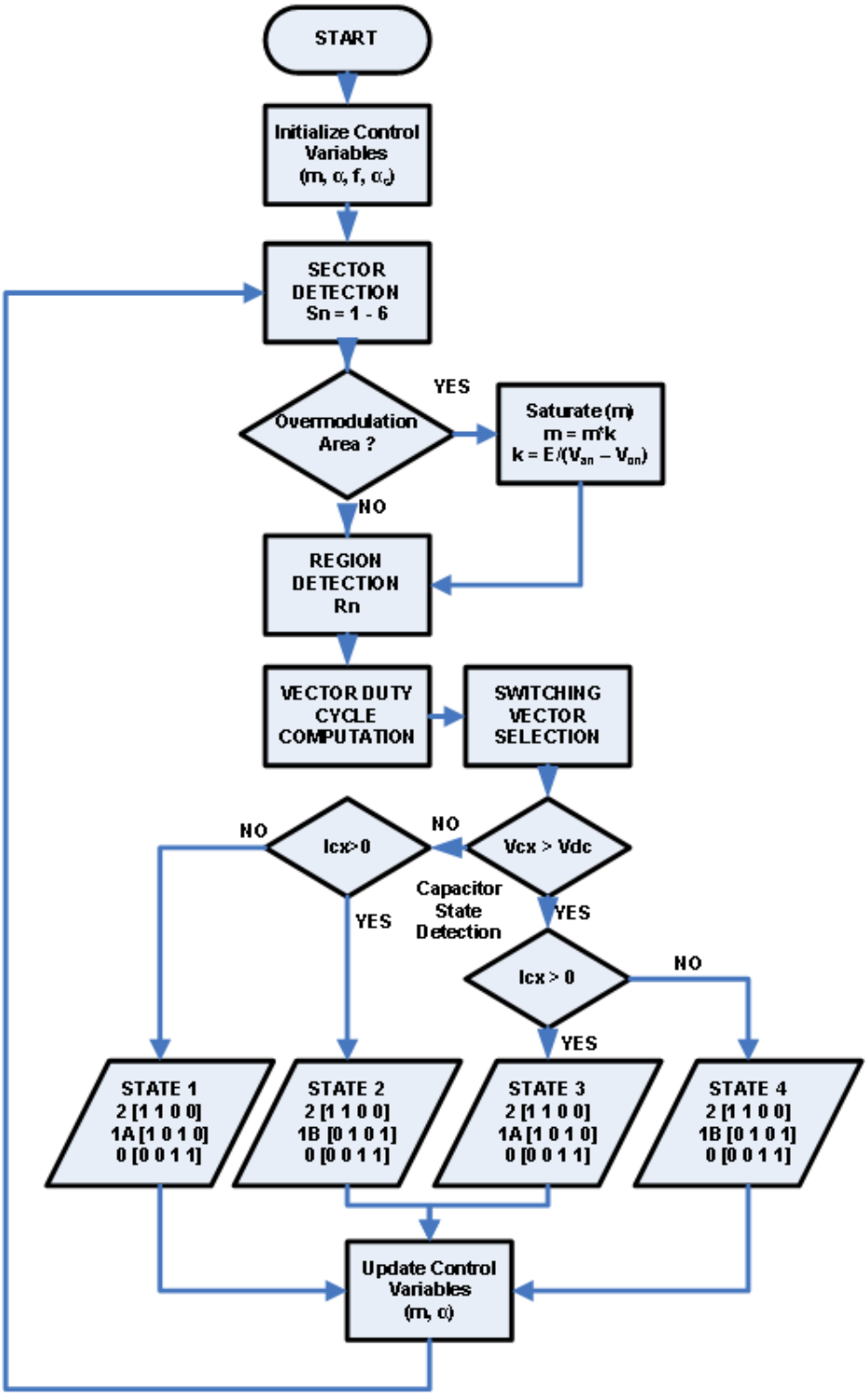


Figure 5.24: MMFCC OH-SVM – Control Flowchart.

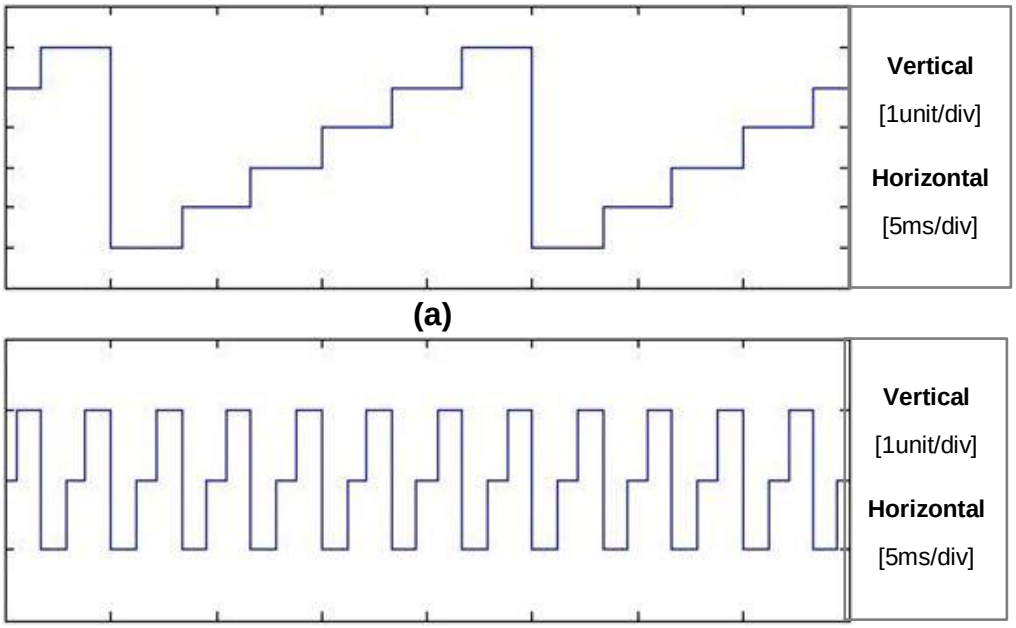
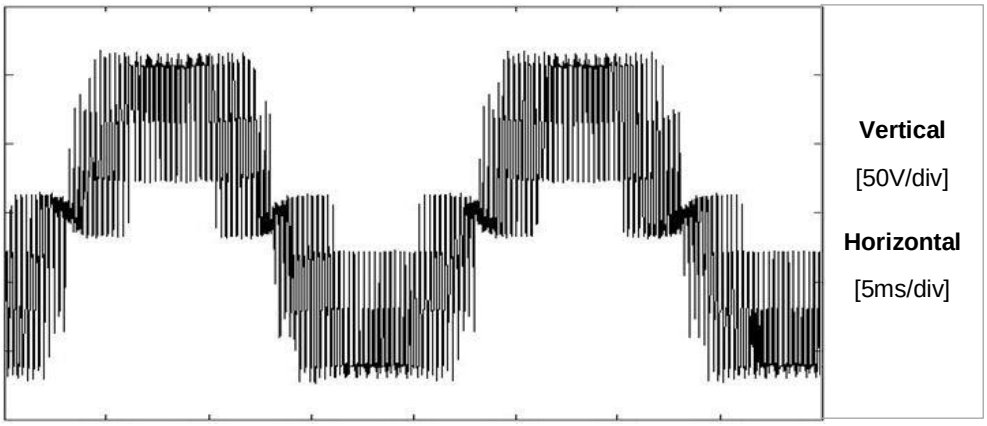
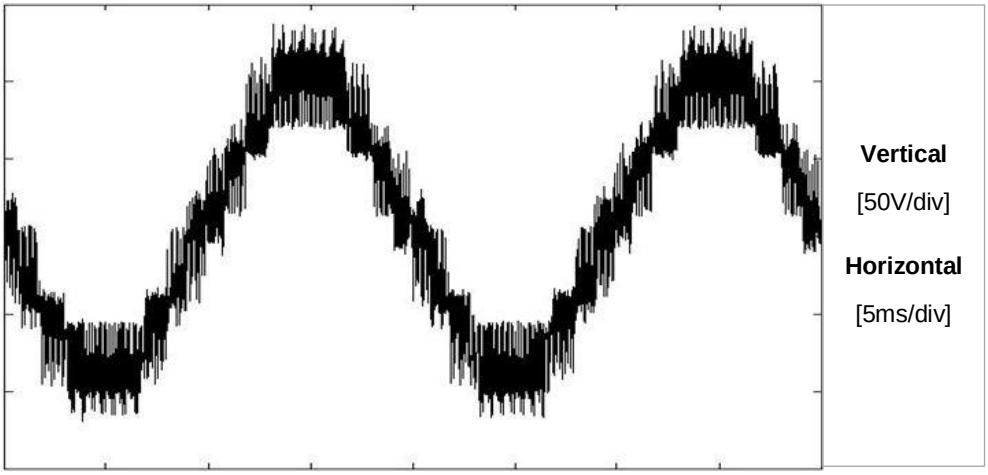


Figure 5.25: MMFCC OMH-SVM – Control Variable for (a) Sector and (b) Region Selection.



(a)



(b)

Figure 5.26: MMFCC OMH-SVM - Phase (a) Module Voltage (b) Arm Voltage.

FC Voltage deviation

The flying capacitor voltages in one of the FCC modules (V_{Ca}, V_{Cb}) were also observed in other to further established that they were balanced as well as the voltage deviation they presented. This is shown in Figure 5.26, that the flying capacitors maintain the expected level of 50V.

In Figure 5.26, the observation window used was, 2 switching periods (i.e 0.008secs) in order to observe the effect of switching to the flying capacitor voltages. Asides the voltage spikes present due to switching impulse noise and slight anomalies from the data acquisition system, the waveform and voltage deviations are similar to those described by the simulation waveforms in Chapter 4 which validated the effectiveness of the open-loop balancing scheme implemented.

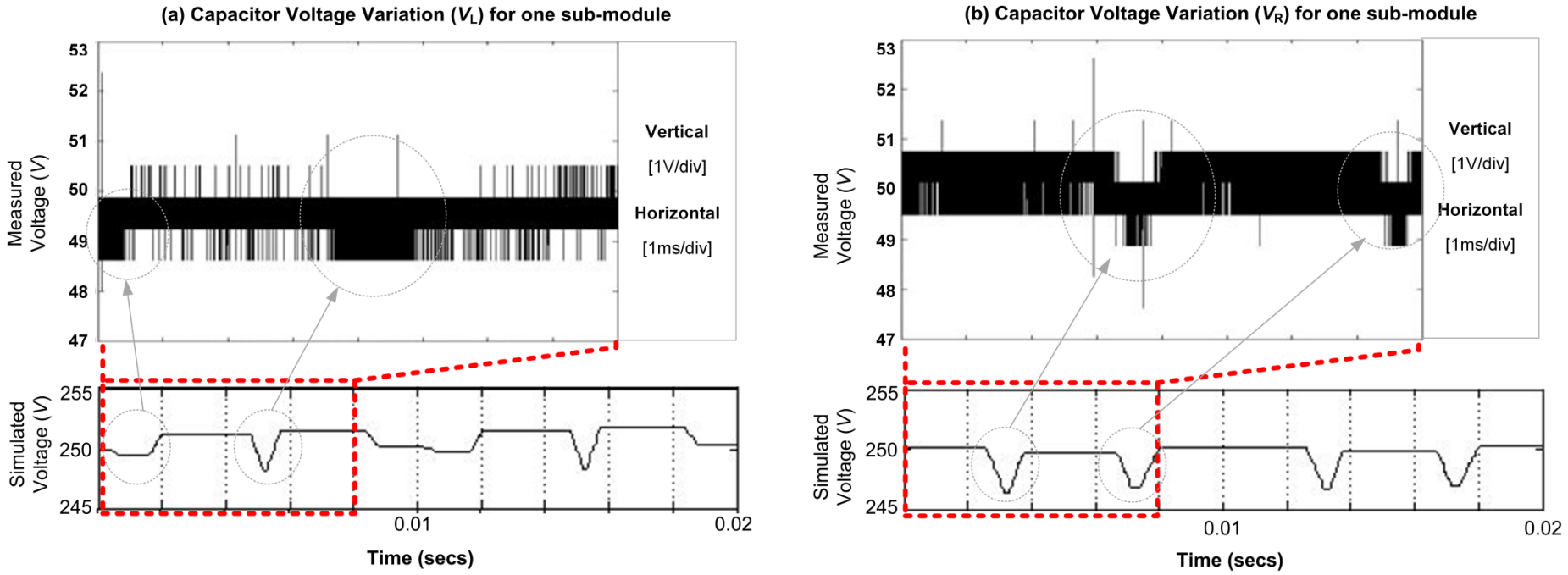


Figure 5.27: Measured vs Simulated MMFCC Flying Capacitor Voltages (a) V_L (b) V_R

In Figure 5.27 the capacitor voltages simulated in Chapter 4 are compared against those measured during the experimental testing. The correlation in both waveforms (e.g. notches present due to switching activity) is evident amidst the noise present in the measured voltage waveforms and quantisation from the ADC conversion on the FPGA. Also from a voltage amplitude perspective the simulated waveforms were captured from a scenario with a nominal capacitor voltage of 250 *V* and show a voltage deviation of around 5 Volts. In the experimental setup the nominal voltage value used is 50 *V* i.e five times smaller and the voltage variation observed is around 1 V (also 5 times smaller) thus there is also correlation in amplitude.

Chapter 6
Conclusion and Recommendations

6.1 Conclusions

During the period of this research, it was intended to investigate the feasibility of implementing a Modular Multilevel Converter topology using a Multilevel Flying Capacitor Module in place of the already established two-level H-bridge and half-bridge sub-modules. This possibility was clearly established and the work has led to the development and experimental verification of the first modular multilevel converter of this type, termed the “Modular Multilevel Flying Capacitor Converter” (MMFCC) throughout this work.

The contributions of this research work to the wider power electronics field are summarised as follows:

- A thorough and comprehensive study on the current types of modular multilevel cascaded converter was carried out. Focusing on the four MMCC topologies, namely, MMCC-SSBC, MMCC-SDBC, MMCC-DSBC and MMCC-DDBC which use either half-bridge or full-bridge circuits as sub-modules, it explored in detail the circuit configurations, operating principles, and the phenomenon of circulating current. The investigation led to the clear conclusions that the former two need to use H-bridge cells as modules and are suitable only for FACTS and BESS applications, while the latter two use half-bridge cells as modules and are only appropriate for HVDC converters.
- Two emerging new topologies, namely, the alternating arm converter (AAC) and the symmetrical bridge converter (SBC) were investigated. The study centred on their features for HVDC applications as contrasted to the currently used MMCC-DSBC and concluded that they could dominate in offshore HVDC where platform size constitutes a premium charge.
- A new set of sub-modules for MMCC based on the flying capacitor topology were proposed by the author. These are:
  3-level half-bridge flying capacitor cells; 3-level H-bridge flying capacitor cells; and 3-level Hybrid H-bridge flying capacitor cells.

- A set of practically-oriented metrics for evaluating sub-modules for MMCCs was established, including footprint; cost; redundancy; efficiency; and performance. These could be potentially useful for practical designers of converter-based equipment. These were applied to evaluate the three FC-based sub-modules as well as the well-known half-bridge, H-bridge circuits. The conclusions stated clearly that the FC half-bridge and hybrid sub-modules offer a lower footprint as well as cost, but the lower number of redundancy states reduce their suitability for the dynamics presented by FACTS applications. The FC H-bridge on the other hand presents a high number of redundant states and thus was selected as the sub-module for evaluating modulation concepts for the topology.
- The most significant outcome from this research has been a novel modulation scheme proposed and developed by the author, called the overlapping hexagon space vector modulation control scheme. The enormous proliferation of possible switching states arising in multilevel converters makes the control of converter switching potentially very complex. Some simplified method of selecting redundant switch states is required. This must be combined with a modulation technique, i.e. of performing pulse width modulation to produce a good approximation to a sinusoidal output. The modulation scheme must also attempt to reduce losses and balance the utilisation of the switches. A further problem specific to the MMFCC is to design the modulation scheme to minimise drift of the flying capacitor voltages. Addressing this very complex problem of modulation control was another main aim of this work.

  This proposed new modulation scheme has the ability to easily control the topology even at extended levels with suitable output quality. The essence of the method is to separate the converter into tiers, and perform space vector modulation within each tier but with phase shifts introduced between the hexagons describing the separate tiers. The concept can be applied to multilevel converters of other topologies. However, experimental verification was undertaken for the flying capacitor case which raises the additional problem of capacitor voltage balancing.

- To achieve this experimental validation of the simulated converter and modulation techniques, design and construction of a bespoke “scaled down” experimental rig has been discussed. The rig was tested using the modulation scheme developed in Chapter 4 and results captured were shown to match the simulated high quality converter voltage outputs, and stabilised sub-module capacitor voltages, even with a switching frequency as low as 250Hz. Hence the final main achievement of this work was to validate the concepts experimentally in a practical demonstrator of an MMFCC.

As a result of this research work, conference publications have been presented based on Chapter 3, Chapter 4 and Chapter 5. In addition, a journal paper was submitted based on Chapter 4 and Chapter 5. It is expected that more publications will arise from continuation of the direction of this research work.

6.1 Recommendations for Future Work

Several paths are available for further investigation. Future studies may involve the application of synchronization techniques for unbalanced grid conditions to the converter at system level. To achieve this, the converter transformer configuration may need to be adjusted to match the requirements of different scenarios.

Further extensions of the work could be via collaborative research with a “distribution side” power utility company in order to test the converter topology at utility level. It is obvious that utility practices in place will prevent the direct connection of the converter to the utility-grid, however with permission, verified measurement devices can be connected and an emulator developed to verify the converter’s reaction to real-time transients.

The system may be monitored over a period of days for converter dynamic performance evaluation.

Finally, future research into the deployment of IGBT and subsequently wide band-gap devices (specifically GaN and SiC) in the MMFCC module circuit will help further exploit the FC-H module which was briefly described in Chapter 3.

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Appendix A
Introduction

Functions/Derivations/Data used within Introduction (Chapter 1).

A.1 Annual Electric Consumption Figures

Table A 1: Annual Electric Consumption Figures (in kWh) for UK, Kenya, Nigeria and Ethiopia between 1970 and 2010.

	UK	Kenya	Nigeria	Ethiopia
1971	237,819,000,000	909000000	1637000000	552000000
1972	245,244,000,000	996000000	1920000000	564000000
1973	262,525,000,000	1067000000	2122000000	551000000
1974	254,961,000,000	1137000000	2026000000	542000000
1975	252,590,000,000	1220000000	2901000000	537000000
1976	257,883,000,000	1351000000	3364000000	531000000
1977	262,335,000,000	1426000000	3977000000	505000000
1978	265,801,000,000	1526000000	4204000000	535000000
1979	276,899,000,000	1640000000	4269000000	596000000
1980	263,772,000,000	1707000000	4997000000	635000000
1981	257,612,000,000	1838000000	3840000000	682000000
1982	252,304,000,000	1884000000	6341000000	728000000
1983	256,268,000,000	1946000000	6491000000	780000000
1984	259,414,000,000	2051000000	5055000000	842000000
1985	272,952,000,000	2229000000	6723000000	809000000
1986	280,780,000,000	2368000000	7795000000	835000000
1987	288,693,000,000	2645000000	7863000000	881000000
1988	297,891,000,000	2595000000	7877000000	864000000
1989	302,234,000,000	2753000000	9007000000	866000000

1990	306,651,000,000	2930000000	8291000000	1082000000
1991	313,062,000,000	3061000000	8751000000	1088000000
1992	313,951,000,000	3159000000	9020000000	1117000000
1993	316,990,000,000	3323000000	10361000000	1245000000
1994	311,333,000,000	3356000000	10062000000	1306000000
1995	323,503,000,000	3490000000	9876000000	1374000000
1996	338,289,000,000	3655000000	9507000000	1443000000
1997	340,102,000,000	3689000000	9304001000	1453000000
1998	345,593,000,000	3813000000	8953000000	1488000000
1999	352,534,000,000	3625000000	9036000000	1480000000
2000	360,100,000,000	3525000000	9109000000	1507000000
2001	363,112,000,000	3934000000	9476000000	1811000000
2002	364,699,000,000	4013000000	13459000000	1840000000
2003	368,297,000,000	4310000000	13444000000	2066000000
2004	368,251,000,000	4679000000	16730000000	2285000000
2005	378,775,000,000	4879000000	17959000000	2560000000
2006	377,284,000,000	5305000000	15929000000	2942000000
2007	375,211,000,000	5582000000	20328000000	3212000000
2008	372,087,000,000	5716000000	19121000000	3419000000
2009	352,330,000,000	5813000000	18617000000	3613000000
2010	356,961,000,000	6321000000	21624000000	4502000000

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Appendix B
Modular Multilevel Converters

Functions/Derivations used in Modular Multilevel Converter discussions (Chapter 2).

B.1 Circulating Currents in MMC with Double Star Bridge Cells

The equivalent circuit shown in Figure B 1 describes the current paths which establish within double star configuration. The convention adopted for the current direction is that of a rectification scheme. The convention required for an inverter is easily realised by swapping the current direction.

An outline the desired current paths is shown in green. The three-phase currents (I_{SA}, I_{SB} and I_{SC}), flow through into the converter arms via the inductors. The value of current that flows through each arm i.e. the arm current (I_{CAT}, I_{CBT}, I_{CCT}: I_{CAB}, I_{CBB}, I_{CCB}) depends on the value the controllable arm voltages (E_{CAT}, E_{CBT}, E_{CCT}: E_{CAB}, E_{CBB}, E_{CCB}). The arm voltages are synthesised as a result of the switching actions applied to the modules in that arm. It is desirable for arm currents in the upper or lower converter arms to sum up and produce I_{DC}, such criteria ensures that no portion of the current circulates within the converter.

A further examination of the MMC using Double Star Bridge Cells exposes at least nine extra current paths with the notations (1) – (9) in Figure B 1 (a. using phase voltages and b. using line voltages) that cause a portion of the supply currents to circulate within the converter. These can be represented using the two equivalent circuits shown in Figure B 2(a) which describes the circuit for the circulating current paths (I) – (VI) and Figure B 2 (b) for (VII) – (IX).

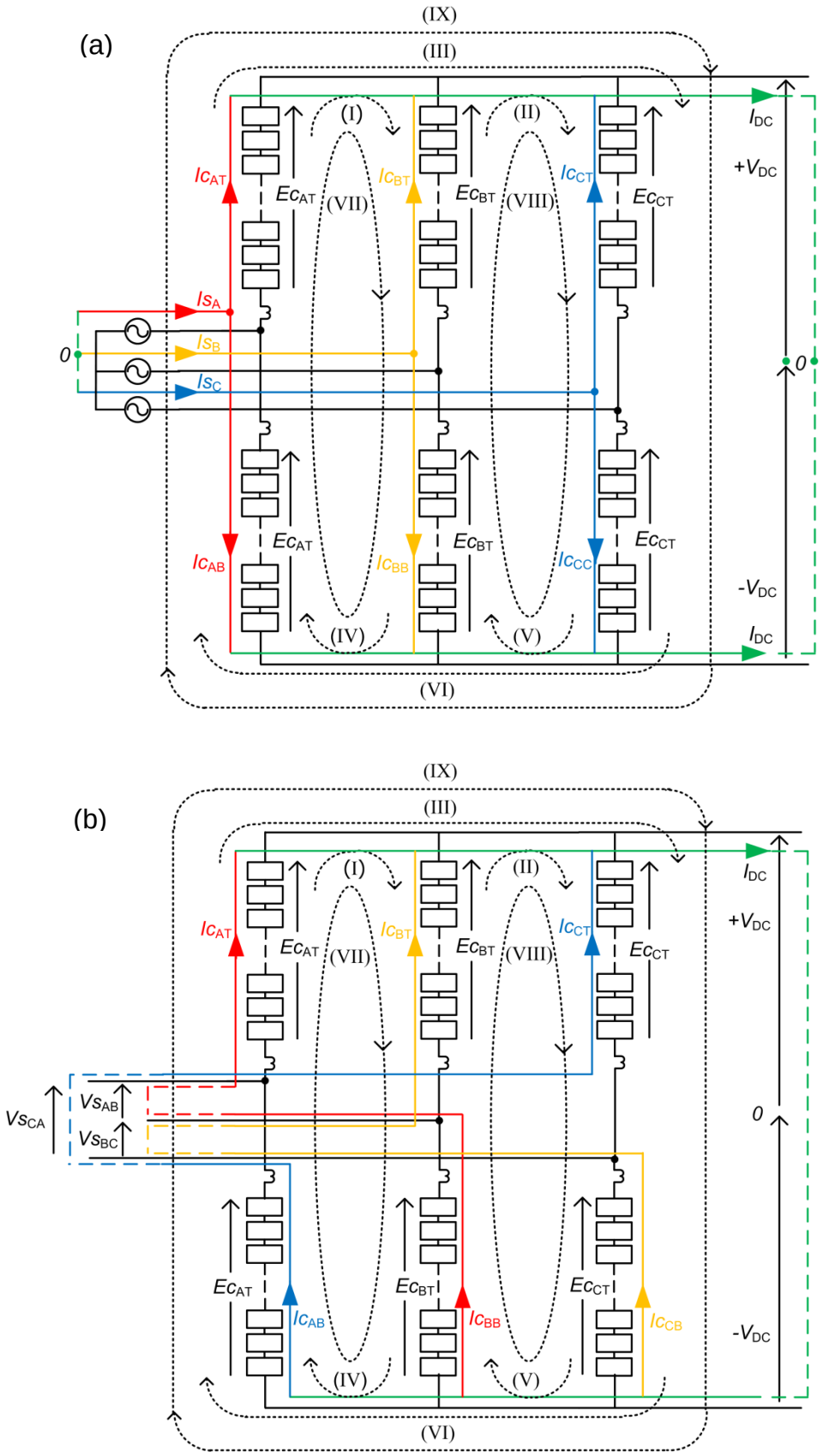

Figure B 1 Current paths that establish within a MMCC double star topology: (a) Phase; and (b) Line-Line equivalent circuits.

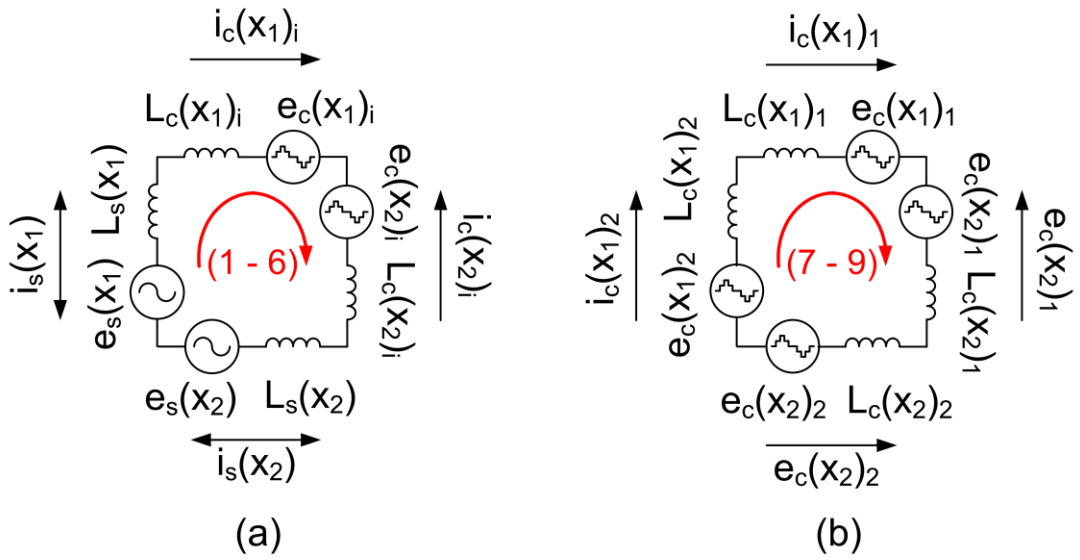

Figure B 2 Equivalent circuits for the circulating currents showing: (a) paths for currents denoted (1)-(6); and (b) (7)-(9).

Applying Kirchhoff's voltage law to the closed circuit in Figure B 2 (a) and considering a fundamental time period when Phase A is positive while Phases B and C are negative (for instance when $30^0 < \Theta < 120^0$) gives (B.1)

$$\underbrace{\left\{e_S(x_1) + L_S(x_1)\frac{\partial i_S(x_1)}{\partial t}\right\}}_{Phase\text{–}(x_1)\_Supply} + \underbrace{\left\{L_C(x_1)\frac{\partial i_C(x_1)_i}{\partial t} + e_C(x_1)_i\right\}}_{Phase\text{–}(x_1)\_Upper\_Arm} - \underbrace{\left\{L_C(x_2)\frac{\partial i_C(x_2)_i}{\partial t} + e_C(x_2)_i\right\}}_{Phase\text{–}(x_2)\_Upper\_Arm} - \underbrace{\left\{e_S(x_2) + L_S(x_2)\frac{\partial i_S(x_2)}{\partial t}\right\}}_{Phase\text{–}(x_2)\_Supply} = 0 \qquad \text{B.1}$$

where:

$e_S(x_1)$ is the phase (x_1) supply voltage applied across the inductor $L_S(x_1)$;

$i_S(x_1)$ is the phase (x_1) AC current;

$e_S(x_2)$ is an adjacent phase (x_2) supply voltage applied across the inductor $L_S(x_2)$;

$i_S(x_2)$ is the phase (x_2) AC current;

$e_C(x_1)_i$ is the phase (x_1) converter (i: 1 = upper, 2 = lower) arm voltage applied across the arm inductor $L_C(x_1)$;

$i_C(x_1)_i$ is the phase (x_1) converter arm current for (i: 1 = upper, 2 = lower);

$e_C(x_2)_i$ is the phase (x_2) converter (i: 1 = upper, 2 = lower) arm voltage applied across the arm inductor $L_C(x_2)$;

$i_C(x_2)_i$ is the phase (x_2) converter arm current for (i: 1 = upper, 2 = lower);

(B.1) can be further simplified by applying the relationship in (B.2) to include an expression for the line-line voltage as shown in (B.3). This negates the necessity to know the polarity of the supply phase current.

$$\underbrace{\left\{e_S(x_1)+L_S(x_1)\frac{\partial i_S(x_1)}{\partial t}\right\}}_{Phase\text{–}(x_1)\_Supply}-\underbrace{\left\{e_S(x_2)+L_S(x_2)\frac{\partial i_S(x_2)}{\partial t}\right\}}_{Phase\text{–}(x_2)\_Supply}=\underbrace{V_S(x_1)(x_2)}_{Line\text{–}Line\_Voltage} \qquad \textbf{B.2}$$

$$\underbrace{V_S(x_1)(x_2)}_{Line\text{–}Line\_Voltage}+\underbrace{\left\{L_C(x_1)\frac{\partial i_C(x_1)_i}{\partial t}+e_C(x_1)_i\right\}}_{Phase\text{–}(x_1)\_Upper\_Arm}-\underbrace{\left\{L_C(x_2)\frac{\partial i_C(x_2)_i}{\partial t}+e_C(x_2)_i\right\}}_{Phase\text{–}(x_2)\_Upper\_Arm}=0 \qquad \textbf{B.3}$$

where:

$V_S(x_1)(x_2)$ line-line voltage across Phase (x_1) and (x_2)

(B.2) expresses a generalised function for the circulating currents (1 – 6). Consider $V_S(x_1)(x_2)$ as the driving force for these circulating currents. To reduce or eliminate these circulating currents implies that $V_S(x_1)(x_2)$ in expression (B.3) must tend towards zero.

Thus to eliminate circulating current 1: (x_1 = a; x_2 = b; and i = 1)

$$\underbrace{\left\{L_C a\frac{\partial i_C a_1}{\partial t}+e_C a_1\right\}}_{Phase\text{–}A\_Upper\_Arm}=\underbrace{\left\{L_C b\frac{\partial i_C b_1}{\partial t}+e_C b_1\right\}}_{Phase\text{–}B\_Upper\_Arm} \qquad \textbf{B.4}$$

To eliminate circulating current 2: (x_1 = b; x_2 = c; and i = 1)

$$\underbrace{\left\{L_C b\frac{\partial i_C b_1}{\partial t}+e_C b_1\right\}}_{Phase\text{–}B\_Upper\_Arm}=\underbrace{\left\{L_C c\frac{\partial i_C c_1}{\partial t}+e_C c_1\right\}}_{Phase\text{–}C\_Upper\_Arm} \qquad \textbf{B.5}$$

To eliminate circulating current 3: (x_1 = c; x_2 = a; and i = 1)

$$\underbrace{\left\{L_C c\frac{\partial i_C c_1}{\partial t}+e_C c_1\right\}}_{Phase\text{–}C\_Upper\_Arm}=\underbrace{\left\{L_C a\frac{\partial i_C a_1}{\partial t}+e_C a_1\right\}}_{Phase\text{–}A\_Upper\_Arm} \qquad \textbf{B.6}$$

To eliminate circulating current 4: (x_1 = a; x_2 = b; and i = 2)

$$\underbrace{\left\{L_C a \frac{\partial i_C a_2}{\partial t} + e_C a_2\right\}}_{Phase\text{–}A\_Lower\_Arm} = \underbrace{\left\{L_C b \frac{\partial i_C b_2}{\partial t} + e_C b_2\right\}}_{Phase\text{–}B\_Lower\_Arm} \quad \textbf{B.7}$$

To eliminate circulating current 5: (x_1 = b; x_2 = c; and i = 2)

$$\underbrace{\left\{L_C b \frac{\partial i_C b_2}{\partial t} + e_C b_2\right\}}_{Phase\text{–}B\_Lower\_Arm} = \underbrace{\left\{L_C c \frac{\partial i_C c_2}{\partial t} + e_C c_2\right\}}_{Phase\text{–}C\_Lower\_Arm} \quad \textbf{B.8}$$

To eliminate circulating current 6: (x_1 = c; x_2 = a; and i = 2)

$$\underbrace{\left\{L_C c \frac{\partial i_C c_2}{\partial t} + e_C c_2\right\}}_{Phase\text{–}C\_Lower\_Arm} = \underbrace{\left\{L_C a \frac{\partial i_C a_2}{\partial t} + e_C a_2\right\}}_{Phase\text{–}A\_Lower\_Arm} \quad \textbf{B.9}$$

(B.7)-(B.9) illustrate the conditions required to ensure that the circulating currents described in Figure B 2 (a) are eliminated (or at least minimized).

Applying Kirchhoff's second law to the closed circuit in Figure B 2 (b) also presents a relationship which describes the circulating currents (7-9) as expressed in (B3):

$$\underbrace{\left\{e_C(x_1)_1 + L_C(x_1)_1 \frac{\partial i_C(x_1)_1}{\partial t}\right\}}_{Phase\text{–}(x_1)\_Upper\_Arm} - \underbrace{\left\{e_C(x_2)_1 + L_C(x_2)_1 \frac{\partial i_C(x_2)_1}{\partial t}\right\}}_{Phase\text{–}(x_2)\_Upper\_Arm}$$
$$- \underbrace{\left\{e_C(x_2)_2 + L_C(x_2)_2 \frac{\partial i_C(x_2)_2}{\partial t}\right\}}_{Phase\text{–}(x_2)\_Lower\_Arm} + \underbrace{\left\{e_C(x_1)_2 + L_C(x_1)_2 \frac{\partial i_C(x_1)_2}{\partial t}\right\}}_{Phase\text{–}(x_1)\_Lower\_Arm} = 0 \quad \textbf{B.10}$$

Thus to eliminate circulating current 7: (x_1 = a; and x_2 = b)

$$\underbrace{\left\{e_C a_1 + L_C a_1 \frac{\partial i_C a_1}{\partial t}\right\}}_{Phase\_a\_Upper\_Arm} + \underbrace{\left\{e_C a_2 + L_C a_2 \frac{\partial i_C a_2}{\partial t}\right\}}_{Phase\_a\_Lower\_Arm} = \underbrace{\left\{e_C b_2 + L_C b_2 \frac{\partial i_C b_2}{\partial t}\right\}}_{Phas\_b\_Lower\_Arm} + \underbrace{\left\{e_C b_1 + L_C b_1 \frac{\partial i_C b_1}{\partial t}\right\}}_{Phase\_b\_Upper\_Arm} \quad \textbf{B.11}$$

To eliminate circulating current (8): (x_1 = b; and x_2 = c)

$$\underbrace{\left\{e_C b_1 + L_C b_1 \frac{\partial i_C b_1}{\partial t}\right\}}_{Phase\_b\_Upper\_Arm} + \underbrace{\left\{e_C b_2 + L_C b_2 \frac{\partial i_C b_2}{\partial t}\right\}}_{Phase\_b\_Lower\_Arm} = \underbrace{\left\{e_C c_2 + L_C c_2 \frac{\partial i_C c_2}{\partial t}\right\}}_{Phas\_c\_Lower\_Arm} + \underbrace{\left\{e_C c_1 + L_C c_1 \frac{\partial i_C c_1}{\partial t}\right\}}_{Phase\_c\_Upper\_Arm} \quad \textbf{B.12}$$

To eliminate circulating current (9): (x_1 = c; and x_2 = a)

$$\underbrace{\left\{e_C c_1 + L_C c_1 \frac{\partial i_C c_1}{\partial t}\right\}}_{Phase\_c\_Upper\_Arm} + \underbrace{\left\{e_C c_2 + L_C c_2 \frac{\partial i_C c_2}{\partial t}\right\}}_{Phase\_c\_Lower\_Arm} = \underbrace{\left\{e_C a_2 + L_C a_2 \frac{\partial i_C a_2}{\partial t}\right\}}_{Phas\_a\_Lower\_Arm} + \underbrace{\left\{e_C a_1 + L_C a_1 \frac{\partial i_C a_1}{\partial t}\right\}}_{Phase\_a\_Upper\_Arm} \quad \textbf{B.13}$$

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Appendix C
MMFC Converter Module and Topology Analysis

Functions/Derivations/Data used in MMFC Converter Module and Topology Analysis (Chapter 3).

C.1 Devices used for Sub-module Assessment

Device	**Manufacturer reference**	**Comments**
Switch Module	IKW30N60T (Infineon)	600 *V*, 30 *A* Power IGBT
Capacitor	EETED2G561EA (Panasonic)	600 V, 560µF Capacitor
Heat Sink	SK105/105SA (Fisher Elektronics)	Chosen specifically for its compensating thermal impedance (R_{th} = 2 K/W) to match maximum switch module operation.
Gate Electronics Module (GEM)	FPGA (ProASIC3) Transducers (LEM)	Only the key parts that vary across the different sub-module concepts are considered.

Appendix D: MMFC Converter Control and Modulation Studies

D.1 Simulation Setup for Modulation Studies

A software model of the MMFCC using the full-bridge FC sub-module concept was represented in Matlab-Simulink. This exercise was undertaken with three objectives in mind:

- To allow “proof-of-concept” validation of the new sub-module concept using a Single Star topology at system-level;
- To present a plausible platform for investigating the different converter modulation strategies; and
- To provide benchmark results for comparing against those obtained during the experimental investigation conducted.

The model reference library block allowed for quicker simulation as only the library block (not the 6 instances of it) are compiled during the simulation model execution.

D.1.1 Plant Representation (AC Line, PCC, Load and Auxiliaries)

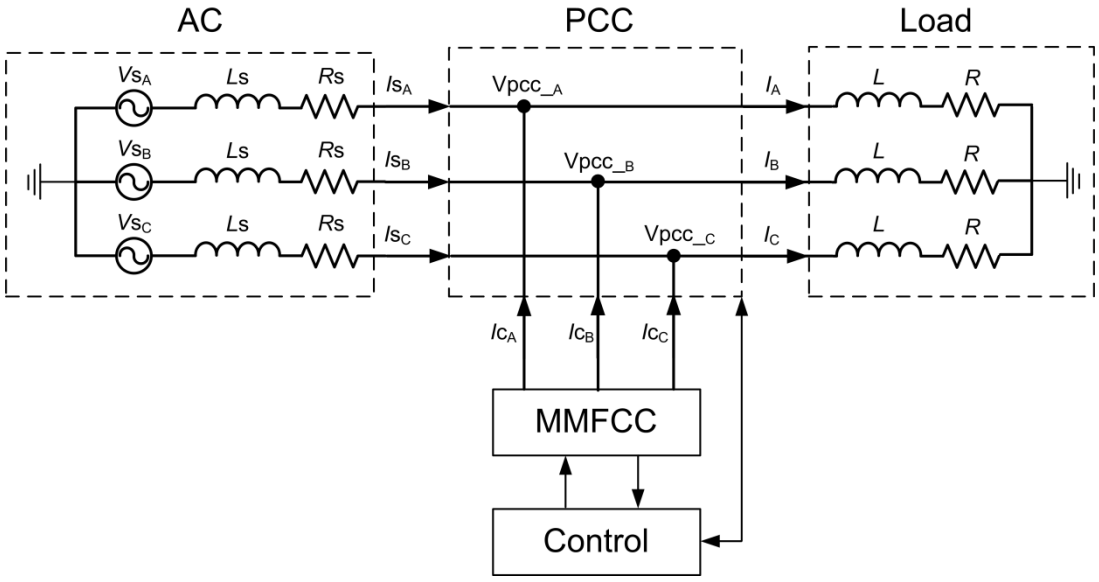

Figure D.1: Plant Setup for MMFCC Modulation Studies.

The plant setup adopted to support the MMFCC modulation studies is shown in Figure D.1 and the main simulation sub-systems are an AC source, the MMFCC, the Control system and the PCC including plant auxiliaries:

The AC system is the main power source in the plant representation. This is represented using a programmable voltage source in the Matlab-Simulink simulation software.

The Point of Common Coupling (PCC) is a group of sub-elements that provide the converter's interface to the line. Typically plant auxiliaries such as measurement elements and circuit breakers are also housed in the PCC to reduce feedback signal latency/delay values. This enables rapid protection coordination response during adverse over-current/over voltage conditions. One typical auxiliary feature of the PCC represented in the MMFCC plant is the implementation of a soft-start resistor and circuit breaker to mitigate the over-current condition that can occur during converter "black-start[1]" or "cold-start"[2]. Such an over-current condition is as a result of the presence of "uncharged" capacitors and a negligible resistance of the predominantly inductive line. Even with all sub-modules not in operation, a current path exists via the sub-module anti-parallel diodes and capacitor (note that this is true for all the sub-module topologies reviewed in Chapter 3 and for either current direction). One option to mitigate this over-current condition is to swap only a few sub-module capacitors into the circuit and in sequence. Such a method is only feasible when all the sub-module gate circuits are powered from ground level i.e.for low voltage (i.e low sub-module count) applications. Using a soft-start resistor presents a more practical technique. A resistance of pre-calculated value normally in the order of a few hundred ohms is switched into circuit during converter start-up to limit the amplitude of the current that flows while the sub-module capacitors are charged up. The soft-start circuit breaker is open and the main breaker closed once nominal operating voltage values are achieved within the sub-modules.

A variety of plant loads are applicable for the setup shown in Figure D.1 but for convenience a simple R-L load is implemented as it is sufficient for the studies.

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[1] The start-up procedure of a power-electronics converter in which its energy storage elements (capacitors, batteries) are charged up to nominal operating values from an established AC source.

[2] The start-up procedure of a power-electronics converter in which its energy storage elements (capacitors, batteries) are charged up to nominal operating values from an established DC source.

D.1.2 MMFCC Sub-Module Representation

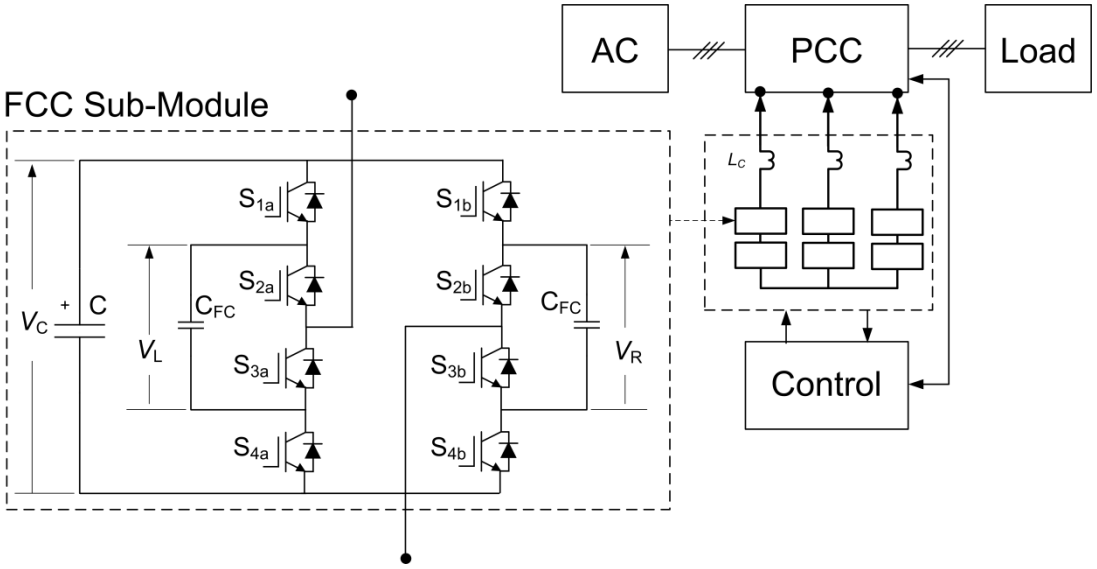

Figure D.2: Representation for the MMFCC sub-module in Simulink.

An outline of the three-level Flying capacitor H-bridge sub-module represented in the Matlab-Simulink model is shown in Figure 4.1 and two such sub-modules are represented to form each converter phase arm. The sub-module capacitor is denoted as *C* and the flying capacitors as C_{FC}.

There are eight power semiconductor switches within each sub-module, and each switch is simulated using the IGBT/Diode model block in simpowersystems library. The device conduction, switching and snubber parameters are set to match those specified in Infineon's Power IGBT devices (IKW30N60T) in order to simulate realistic switching conditions.

The switching signals are supplied to each sub-module via a Simulink bus structure. A bus selector within each sub-module enables the control signals for four (out of eight) devices S_{1a}, S_{2a}, S_{1b} and S_{2b} to be selected while a logical NOT is applied to provide the remaining four signals i.e for S_{3a}, S_{4a}, S_{3b} and S_{4b}. This is not far from standard implementation practice which typically features a logical NOT and a dead-time between a pair of complementary signals. Such practice prevents the possibility of sub-module capacitor short-circuit either from logically incorrect complementary switch operation or device transition periods from conduction to blocking and vice versa that may result in a conduction overlap.

Feedback signals for each sub-module include: the sub-module capacitor voltage V_C; and flying capacitor voltages V_L and V_R.

D.1.3 Control System in Simulink

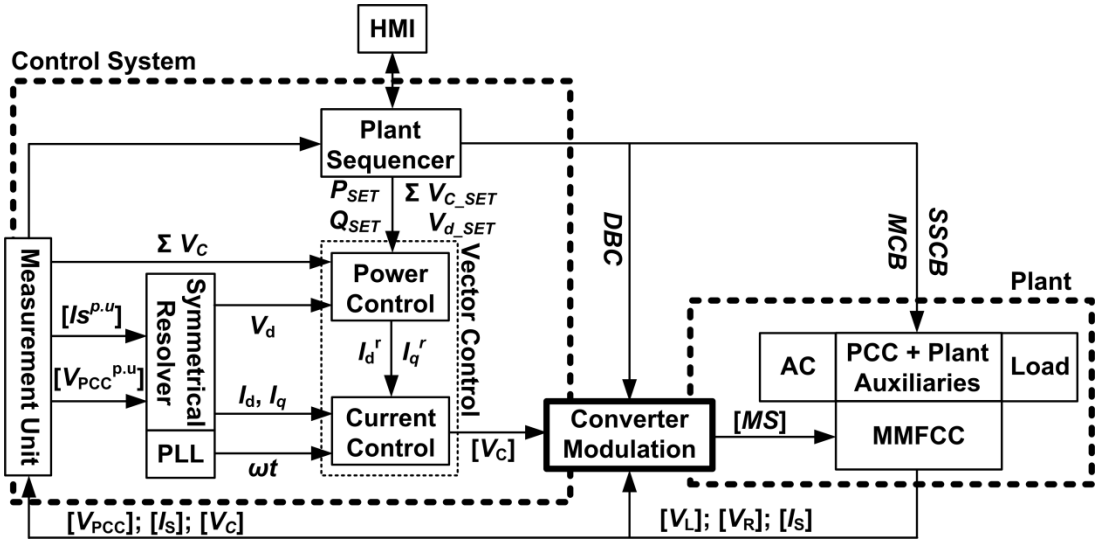

Figure D.3: MMFCC System Control Concept.

Coordinating the MMFCC and entire plant equipment (PCC + Plant Auxiliaries) requires a sophisticated control concept. Typically this involves a multi-layered structure of control sub-systems that tackle the various and multi-bandwidth requirements for plant coordination and protection. Different permutations of control sub-systems are possible that can provide similar functionality, a non-limiting example is shown in Figure D.3 with a description of the sub-systems within provided below.

A HMI (Human Machine Interface) sub-system provides an interface for a system operator to monitor and operate plant equipment by issuing system set-points into a plant sequencer (e.g. mode of operation, real/reactive power demand values, etc.). There are no strict bandwidth requirements for the HMI, but the applications/algorithms within are usually executed at values in the order of a few milliseconds and best practice suggests at least once every fundamental cycle (e.g 10 ms for a 50 Hz system). In practice the HMI is a collection of executable applications installed on computing-type platform and depending on plant requirements a system operator may access this platform on site or remotely.

The Measurement Unit sub-system is a collection of plant signal processing functions (e.g. isolation, filtering and per-unitisation). The ideal requirement

of this sub-system an output with infinite bandwidth and no noise but such is impractical due to: limitations in hardware (both for analogue and digital systems); and the interaction of proportional propagation between a signal's bandwidth and noise. This typically results in an engineering compromise as an optimal choice is between a high bandwidth – high noise signal feedback (thus quicker response but a potential for unintended response to noise) or lower bandwidth - lower noise feedback (slower response but shielded from noise). Hopefully future research on advanced signal filter and noise cancelation techniques will uncover a potential for achieving plant feedback with extremely high bandwidth and negligible noise. In practice signal isolation is provided via the use of transducers (for high voltage to low voltage isolation) and terminal boards usually with optical isolation (for ground noise isolation). Signal filtering and per-unitisation can also be provided using hardware i.e via the use of operational amplifiers. Such an approach is cumbersome and not easily scalable thus modern application make use of embedded platforms based on Field Programmable Gate Array (FPGA) cards. This enables easy deployment of sophisticated filtering algorithms with execution at high bandwidth values (typically over 1MHz). In. For signal per-unitisation input signals are multiplied to an inverse of the system base values[3] using a Gain value. Signal isolation functionality is not required for the software simulation of the plant.

The primary function of the plant sequencer is supervision. This sub-system receives system set-points from the plant operator via the HMI, considers the system's real-time condition (e.g. using states/signals from the measurement unit) and issues plant governing commands such as: block/de-block converter (DBC); make/break main circuit breaker (MCB); make/break soft-start circuit breaker (MCB); and set-points (P_{SET}, Q_{SET}) for deriving the converter power and current control values. There are no stringent bandwidth requirements for the plant sequencer but it is best practice to implement a value between that of the HMI and that of the lower level power control function (e.g around 1 ms for the system under study). Earlier systems implemented the plant sequencer as a separate Programmable Logic Control (PLC) hardware with its digital output (states) connected into lower-level control hardware. The availability of quicker and

[3] Base values are a unit for per-unitising a system based on voltage, current and/or impedance ratings specified.

more robust embedded platforms often multicore digital signal processors has enabled the integration of both functionalities into a single embedded platform.

In combination the Symmetrical decomposition, Phase Locked Loop (PLL), power control and current control sub-systems make up the cluster of lower level control sub-systems. A summary of the functionality provided is as follows: station demand values are received via the plant sequencer, compared against the processed plant feedback values to compute any phase and amplitude changes required for the converter. The result is a converter voltage demand supplied as input reference to the converter modulation sub-system. Symmetrical resolver and PLL are signal processing functions but related to signal reference frame representation rather to signal quality adjustment. The symmetrical resolver provides two key functions. The per-unitised three-phase AC signals ($V_{PCC}^{p.u}$, $I_S^{p.u}$) are resolved into positive, negative and zero- sequence components using Charles Fortescue's decomposition technique to allow stable converter control even when the connected AC system is unbalanced. The next function is a reference frame resolver that generates a direct-quadrature (*d-q*) representation for each set of three-phase feedback signals (e.g. V_{PCC_A}, V_{PCC_B}, $V_{PCC\_C} \rightarrow V_d$, V_q). The *d-q* components are DC values and this allows the application of servo-type regulators that compensate for errors between converter feedback values and reference values (i.e. computed from station set-points).. The objective of any PLL in the control of a grid connected converter is to ensure the converter voltage is always synchronised with that of the AC line. This is compulsory to ensure that the desired quantity and quality of power is exchanged. A basic method for achieving this is via a servo regulator that compensates the error between the quadrature component of the converter voltage and that of the rotating reference frame described by the grid voltage. The PLL is an important aspect in the control of any grid-connected converter, more so when the grid has a low short circuit level (around 2.0 and below, typically defined as a "weak grid"). For convenience, during the studies within it is assumed that the AC system is balanced thus only positive sequence components of a balanced three-phase reference are available for modulation control.

The Power Control sub-system also known as the outer-loop control is required to compute the reference currents (I_d^r, I_q^r) that must flow through the converter in order to achieve power set-points (P_{SET}, Q_{SET}) and for a PCC

voltage value of V_d. The plant set-up requires the management of three key elements: real power; reactive power; and MMFC converter energy. The management of real power ensures that the voltage capacity of each MMFCC phase arm is within the limits of a desired reference value (ΣV_{C_SET}). This is achieved by comparing the reference voltage value against the sum of the sub-module capacitor voltages (ΣV_C) and compensating for the error via a servo regulator that generates the direct component (I_d^r) of the converter reference current value. For the plant set-up in Figure D.1 as long as $\Sigma V_C = \Sigma V_{C\_SET}$, the direct component of the converter current is zero[4]. Management of reactive power typically presents two modes for consideration: AC voltage regulation (indirect reactive power control); and direct reactive power control. AC voltage regulation involves computing the quadrature component of the converter reference current (I_q^r) in order to maintain a set PCC voltage value (V_{d_SET}).

Within the Current Control sub-system, instantaneous (but discretised) converter voltage demand values "V_C" are computed at each sample instant. Typically the reference currents (I_d^r, I_q^r) are compared against measured currents (I_d, I_q) and the current error reflects change in converter voltage required to achieve the power set-points. This is the classical deadbeat control method other methods are available such as the use of multi input multi output (MIMO) based control or robust LQR digital control techniques. Finally the current control sub-system relies on the phase signal "ωt" derived from the PLL sub-system to transform the computed converter voltage demand from the synchronous rotating reference frame back to a three-phase (A-B-C) symmetrical component. This requirement also makes the control method vulnerable in an application with a weak/unbalanced grid where the phase signal is less stable. In practice the Symmetrical resolver, PLL, Power control and Current control sub-systems are typically deployed within the same embedded hardware with sample bandwidth between 2 – 20 kHz.

An unbalanced system can resolve to positive, negative and zero sequence symmetrical components. One method for tackling such a scenario is as follows: the PLL is locked to the positive sequence component; and a dual

[4] This assumes an ideal (lossless) converter. In reality the converter will pull a minimal quantity of the direct current component to supply it's losses.

parallel vector control algorithm based on the superposition theorem is implemented, one control loop regulates the positive sequence component and the other cancels the negative sequence component (it is assumed that a star-delta transformer connection rejects the influence of zero-sequence components).

The lower control sub-systems shown in Figure D.3 and descriptions in the associated text are based on adaptations from the classical vector control principle. Vector control is not the focus of this thesis and merely an enabling feature within the simulation platform used by the author to investigate MMFCC modulation algorithms as discussed in the following text.

The following text will focus purely on converter modulation and sub-module level dynamics.

D.2 Newton-Raphson Algorithm

Matlab functions (newtonmain.m, newtonm.m, jacob4x4.m and f4.m) are presented.

D.2.1 main file (newtonmain.m)

```
x0 = [0.35, 1.1, 1.2, 1.5]; %initial guess
ma = 0.8;                   %modulation index
[x,iter] = newtonm(ma,x0,'f4','jacob4x4');  %executing the algorithm
```

D.2.2 Newton Raphson function (newtonm.m)

```
function [x,iter] = newtonm(ma,x0,f,J)
% Newton-Raphson method applied to a
% system of linear equations f(x) = 0,
% given the jacobian function J, with
% J = delta(f1,f2,...,fn)/delta(x1,x2,...,xn)
% x = [x1;x2;...;xn], f = [f1;f2;...;fn]
% x0 is an initial guess of the solution

N = 1000; % tolerance for number of iterations
epsilon = 1e-10; % tolerance for error
maxval = 10000.0; % define value for divergence
xx = x0; % load initial guess
while (N>0)
 JJ = feval(J,xx);
if abs(det(JJ))<epsilon
 error('newtonm - Jacobian is singular - try new x0');
 abort;
end;
 xn = xx - inv(JJ)*feval(f,xx,ma);

 if abs(feval(f,xn,ma))<epsilon
 x=xn;
 iter = 1000-N;
return;
```

```
end;
if abs(feval(f,xx,ma))>maxval
 iter = 1000-N;
 disp(['iterations = ',num2str(iter)]);
 error('Solution diverges');
 abort;
end;
 N = N - 1;
 xx = xn;
end;
error('No convergence after 1000 iterations.');
abort;
% end function
```

D.2.3 Jacobian (jacob4x4.m)

```
function [J] = jacob4x4(x)
% Evaluates the Jacobian of a 4x4
% system of non-linear equations
J(1,1)  =  -sin(x(1));                          J(1,2)  =  -sin(x(2));
J(1,3) = -sin(x(3));            J(1,4) = -sin(x(4));
J(2,1)  =  -5*sin(5*x(1));                 J(2,2)  =  -5*sin(5*x(2));
J(2,3) = -5*sin(5*x(3));        J(2,4) = -5*sin(5*x(4));
J(3,1)  =  -7*sin(7*x(1));                 J(3,2)  =  -7*sin(7*x(2));
J(3,3) = -7*sin(7*x(3));        J(3,4) = -7*sin(7*x(4));
J(4,1)  =  -11*sin(11*x(1));             J(4,2)  =  -11*sin(11*x(2));
J(4,3) = -11*sin(11*x(3));      J(4,4) = -11*sin(11*x(4));
% end function
```

D.2.4 SHE functions (f4.m)

```
function [f] = f4(x,ma)
% f4(x) = 0, with x = [x(1);x(2);x(3);x(4)] representing
% firing angles for a system of 4 non-linear equations
f1 = cos(x(1))+cos(x(2))+cos(x(3))+cos(x(4))-(pi*ma/2); %fundamental
f2   =   cos(5*x(1))+cos(5*x(2))+cos(5*x(3))+cos(5*x(4));        %5th
Harmonic
f3   =   cos(7*x(1))+cos(7*x(2))+cos(7*x(3))+cos(7*x(4));        %7th
Harmonic
f4  =  cos(11*x(1))+cos(11*x(2))+cos(11*x(3))+cos(11*x(4));     %11th
Harmonic
f = [f1;f2;f3;f4];

% end function
```

D.3 Secant Algorithm

Matlab functions (secantmain.m, secantm.m, jacobFD.m and f4.m) are presented.

D.3.1 main file (secantmain.m)

```
x0 = [0.35, 1.1, 1.5, 1.35]; %initial guess
ma = 0.8;                    %modulation index
dx = 1e-10;                  %step used for finite difference
[x,iter] = secantm(ma,x0,'f4','jacobFD');  %executing the algorithm
```

D.3.2 Secant function (secantm.m)

```
function [x,iter] = secantm(ma,x0,dx,f)
% Secant-type method applied to a
% system of linear equations f(x) = 0, 17
% given the jacobian function J, with
% The Jacobian built by columns.
% x = [x1;x2;...;xn], f = [f1;f2;...;fn]
% x0 is the initial guess of the solution
% dx is an increment in x1,x2,... variables
N = 1000; % define max. number of iterations
epsilon = 1.0e-10; % define tolerance
maxval = 10000.0; % define value for divergence
if abs(dx)<epsilon
 error('dx = 0, use different values');
return;
end;
xn = x0; % load initial guess
[n m] = size(x0);
while (N>0)
 JJ = [1,2,3,4;2,3,4,5;3,4,5,6;4,5,6,7]; xx = zeros(n,1);
for j = 1:n % Estimating
xx = xn; % Jacobian by
xx(j) = xn(j) + dx; % finite
 fxx = feval(f,xx,ma);
 fxn = feval(f,xn,ma);
 JJ(:,j) = (fxx-fxn)/dx; % differences
end; % by columns
if abs(det(JJ))<epsilon
 error('newtonm - Jacobian is singular - try new x0,dx');
return;
end;
 xnp1 = xn - inv(JJ)*fxn;
 fnp1 = feval(f,xnp1,ma);
if abs(fnp1)<epsilon
 x=xnp1;
 iter = 1000-N;
 disp(['iterations: ', num2str(100-N)]);
return;
end;
if abs(fnp1)>maxval
    iter = 1000-N;
 disp(['iterations: ', num2str(100-N)]);
 error('Solution diverges');
return;
end;
 N = N - 1;
 xn = xnp1;
end;
error('No convergence');
return;
% end function
```

D.3.3 Finite Difference Jacobian (jacobFD.m)

```
function [J] = jacobFD(f,x,delx)
% Evaluates the Jacobian of a 4x4
% SHE system of non-linear equations
% f(x) = 0, through finite differences.
```

```
% The Jacobian is built by columns
[m n] = size(x);
for j = 1:m
 xx = x;
 xx(j) = x(j) + delx;
 J(:,j) = (f(xx)-f(x))/delx;
end;
% end function
```

D.3.4 SHE functions (f4.m)

```
function [f] = f4(x,ma)
% f4(x) = 0, with x = [x(1);x(2);x(3);x(4)] representing
% firing angles for a system of 4 non-linear equations
f1 = cos(x(1))+cos(x(2))+cos(x(3))+cos(x(4))-(pi*ma/2); %fundamental
f2   =   cos(5*x(1))+cos(5*x(2))+cos(5*x(3))+cos(5*x(4));        %5th
Harmonic
f3   =   cos(7*x(1))+cos(7*x(2))+cos(7*x(3))+cos(7*x(4));        %7th
Harmonic
f4  =  cos(11*x(1))+cos(11*x(2))+cos(11*x(3))+cos(11*x(4));     %11th
Harmonic
f = [f1;f2;f3;f4];

% end function
```

D.4 Genetic Optimization fsolve Algorithm

Matlab functions (fsolvemain.m and f4.m) are presented.

D.4.1 main file (fsolvemain.m)

```
x0 = [0.35, 1.1, 1.5, 1.35]; %initial guess
ma = 0.8;                    %modulation index
x = fsolve(@(x) f4(x,ma),x0);  %executing the fsolve algorithm
```

D.4.2 SHE function (f4.m)

```
function [f] = f4(x,ma)
% f4(x) = 0, with x = [x(1);x(2);x(3);x(4)] representing
% firing angles for a system of 4 non-linear equations
f1 = cos(x(1))+cos(x(2))+cos(x(3))+cos(x(4))-(pi*ma/2); %fundamental
f2   =   cos(5*x(1))+cos(5*x(2))+cos(5*x(3))+cos(5*x(4));        %5th
Harmonic
f3   =   cos(7*x(1))+cos(7*x(2))+cos(7*x(3))+cos(7*x(4));        %7th
Harmonic
f4  =  cos(11*x(1))+cos(11*x(2))+cos(11*x(3))+cos(11*x(4));     %11th
Harmonic
f = [f1;f2;f3;f4];

% end function
```

D.5 fsolve Algorithm – 12 Firing angles

Matlab functions (fsolve12main.m and f12.m) are presented.

D.5.1 main file (fsolve12main.m)

```
x00 = [0.15; 0.25; 0.35; 0.50; 0.85; 1.10; 1.15; 1.25; 1.35; 1.4;
1.45; 1.5]; %initial guess
ma = 0.8;                    %modulation index
for i=0:1:100

x = fsolve(@(x) f4(x,ma),x00);  %executing the fsolve algorithm
x00 = x;
end
```

D.5.2 SHE function (f12.m)

```
function [f] = f12(x,ma)
%         f4(x)          =          0,          with          x          =
[x(1);x(2);x(3);x(4);x(5);x(6);x(7);x(8);x(9);x(10);x(11);x(12)]
representing
% firing angles for a system of 4 non-linear equations
f1              =              cos(x(1))-cos(x(2))+cos(x(3))+cos(x(4))-
cos(x(5))+cos(x(6))+cos(x(7))-cos(x(8))+cos(x(9))+cos(x(10))-
cos(x(11))+cos(x(12))-(pi*ma/2);
%fundamental
f2          =          cos(5*x(1))-cos(5*x(2))+cos(5*x(3))+cos(5*x(4))-
cos(5*x(5))+cos(5*x(6))+cos(5*x(7))-
cos(5*x(8))+cos(5*x(9))+cos(5*x(10))-cos(5*x(11))+cos(5*x(12));
%5th Harmonic
f3          =          cos(7*x(1))-cos(7*x(2))+cos(7*x(3))+cos(7*x(4))-
cos(7*x(5))+cos(7*x(6))+cos(7*x(7))-
cos(7*x(8))+cos(7*x(9))+cos(7*x(10))-cos(7*x(11))+cos(7*x(12));
%7th Harmonic
f4        =        cos(11*x(1))-cos(11*x(2))+cos(11*x(3))+cos(11*x(4))-
cos(11*x(5))+cos(11*x(6))+cos(11*x(7))-
cos(11*x(8))+cos(11*x(9))+cos(11*x(10))-cos(11*x(11))+cos(11*x(12));
%11th Harmonic
f5        =        cos(13*x(1))-cos(13*x(2))+cos(13*x(3))+cos(13*x(4))-
cos(13*x(5))+cos(13*x(6))+cos(13*x(7))-
cos(13*x(8))+cos(13*x(9))+cos(13*x(10))-cos(13*x(11))+cos(13*x(12));
%13th Harmonic
f6        =        cos(17*x(1))-cos(17*x(2))+cos(17*x(3))+cos(17*x(4))-
cos(17*x(5))+cos(17*x(6))+cos(17*x(7))-
cos(17*x(8))+cos(17*x(9))+cos(17*x(10))-cos(17*x(11))+cos(17*x(12));
%17th Harmonic
f7        =        cos(19*x(1))-cos(19*x(2))+cos(19*x(3))+cos(19*x(4))-
cos(19*x(5))+cos(19*x(6))+cos(19*x(7))-
cos(19*x(8))+cos(19*x(9))+cos(19*x(10))-cos(19*x(11))+cos(19*x(12));
%19th Harmonic
f8        =        cos(23*x(1))-cos(23*x(2))+cos(23*x(3))+cos(23*x(4))-
cos(23*x(5))+cos(23*x(6))+cos(23*x(7))-
cos(23*x(8))+cos(23*x(9))+cos(23*x(10))-cos(23*x(11))+cos(23*x(12));
%23th Harmonic
f9        =        cos(23*x(1))-cos(23*x(2))+cos(23*x(3))+cos(23*x(4))-
cos(25*x(5))+cos(25*x(6))+cos(25*x(7))-
cos(25*x(8))+cos(25*x(9))+cos(25*x(10))-cos(25*x(11))+cos(25*x(12));
%25th Harmonic
f10       =        cos(29*x(1))-cos(29*x(2))+cos(29*x(3))+cos(29*x(4))-
cos(29*x(5))+cos(29*x(6))+cos(29*x(7))-
cos(29*x(8))+cos(29*x(9))+cos(29*x(10))-cos(29*x(11))+cos(29*x(12));
%29th Harmonic
```

```
f11      =      cos(31*x(1))-cos(31*x(2))+cos(31*x(3))+cos(31*x(4))-
cos(31*x(5))+cos(31*x(6))+cos(31*x(7))-
cos(31*x(8))+cos(31*x(9))+cos(31*x(10))-cos(31*x(11))+cos(31*x(12));
%31th Harmonic
f12      =      cos(37*x(1))-cos(37*x(2))+cos(37*x(3))+cos(37*x(4))-
cos(35*x(5))+cos(35*x(6))+cos(35*x(7))-
cos(35*x(8))+cos(35*x(9))+cos(35*x(10))-cos(35*x(11))+cos(35*x(12));
%35th Harmonic
f = [f1;f2;f3;f4;f5;f6;f7;f8;f9;f10;f11;f12];

% end function
```

Appendix E
Fundamental Power System & Control Concepts

Functions/Derivations used in system level control equations (Chapter 6).

E.1 Vector Current Control

Vector Current Control (VCC) is one of the most popular control concepts used for grid-tied voltage sourced converters. It presents a means of directly controlling the current within a sufficiently high bandwidth is capable of damping resonances in a grid-tie systems.

As the current is directly controlled, it is easy to protect the equipment from over currents easily and very quickly.

The basic principle is that the real and quadrature powers are controlled via an inner current loop in the decoupled synchronous rotating reference (d-q) frame.

It is important that the PCC is stiff and the dynamics of the PLL are negligible.

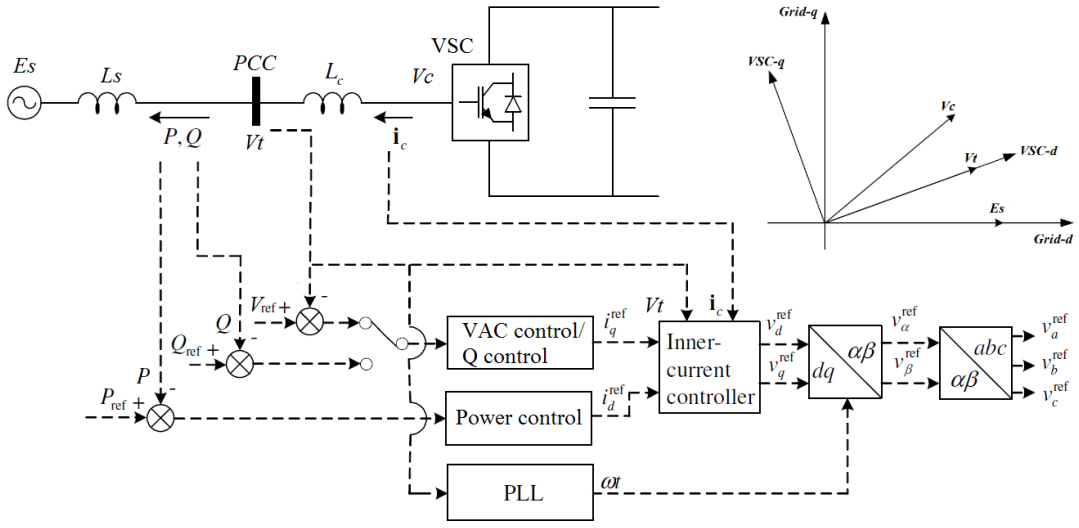

Figure E1: Vector Current Control

References:

Yazdani, A., and Iravani, R.: 'Voltage-Sourced Converters in Power Systems' (Wiley-IEEE Press, 2010. 2010)

E.2 Symmetrical components

The application of the symmetrical components is a fundamental part of the control within a high performance converter. It is required to process the measured AC values to generate the positive, negative and if required zero sequence phasors. It is also important in the PLL to ensure the AC voltage is always locked to a balanced representative of the reference value (the positive sequence phasor).

The concept is that a three phase waveform may be divided into three components: -

1. x_0, a zero sequence component, a balanced, in phase waveform.
2. x_1, a positive sequence component, a balanced three phase term moving in the 'forward' direction.
3. x_2, a negative sequence component, a balanced three phase term moving in the 'reverse' direction.

The basic measured 'abc' waveform is therefore divided as: -

$$x_{abc} = \begin{pmatrix} x_a \\ x_b \\ x_c \end{pmatrix} = \begin{pmatrix} x_{a,0} \\ x_{b,0} \\ x_{c,0} \end{pmatrix} + \begin{pmatrix} x_{a,1} \\ x_{b,1} \\ x_{c,1} \end{pmatrix} + \begin{pmatrix} x_{a,2} \\ x_{b,2} \\ x_{c,2} \end{pmatrix} \quad \text{E.1}$$

where x could be either voltage or current (or any rotating phasor). The three separate phase waveforms are related as: -

$$\begin{aligned} x_0 &\equiv x_{a,0} = x_{b,0} = x_{c,0} \\ x_1 &\equiv x_{a,1} = a^2 \cdot x_{b,1} = a \cdot x_{c,1} \\ x_2 &\equiv x_{a,2} = a \cdot x_{b,2} = a^2 \cdot x_{c,2} \end{aligned} \quad \text{E.2}$$

Where $a = e^{j\frac{2}{3}\pi}$. Thus

$$x_{abc} = \begin{pmatrix} x_0 \\ x_0 \\ x_0 \end{pmatrix} + \begin{pmatrix} x_1 \\ a^2 \cdot x_1 \\ a \cdot x_1 \end{pmatrix} + \begin{pmatrix} x_2 \\ a \cdot x_2 \\ a^2 \cdot x_2 \end{pmatrix} = \begin{pmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{pmatrix} \cdot \begin{pmatrix} x_0 \\ x_1 \\ x_2 \end{pmatrix} = A \cdot x_{012} \quad \text{E.3}$$

The converse of this is given as: -

$$x_{012} = A^{-1} \cdot x_{abc} = \frac{1}{3} \cdot \begin{pmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{pmatrix} \cdot \begin{pmatrix} x_a \\ x_b \\ x_c \end{pmatrix} \quad \text{E.4}$$

The standard deductions are for a balance set of three phase waveforms: -

1. The zero sequence component is always zero.

2. The negative sequence component is the complex conjugate of the positive sequence component.
3. The negative component phasor is completely independent of the positive component phasor.

References:

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