Next-generation GaN Power Semiconductor Devices

By

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Thesis submitted to the University of Sheffield

for the degree of Doctor of Philosophy

November, 2015

Acknowledgements

I would like to express my sincere thanks and appreciation to my supervisor, Prof. Shankar Ekkanath Madathil for truly believing in me right from providing me with the opportunity to join his team, to his valuable guidance, mentorship and encouragement for the entire duration of my doctoral research.

I would like to acknowledge EPSRC Dorothy Hodgkin Postgraduate Award and Rolls-Royce for awarding me a full research scholarship. A special thanks to Dr. Graham Bruce and Kalyani Menon from Rolls-Royce, for their active involvement as the key interface between the company and our research group as well as for sharing insights on the requirements for aerospace applications and effective coordination of the project with external collaborators/sub-contractors in UK. I'd also like to acknowledge the award of EPSRC Doctoral Prize Fellowship from the University of Sheffield that'll enable me to continue my research in this area for one more year.

I want to thank Dr. Akira Nakajima from AIST, Japan who was almost like an unofficial co-supervisor to me. It was through the numerous discussions during his yearly visits to Sheffield as a Newton Alumni Fellow and the long Skype calls with him (sometimes in the wee hours of the day) that helped me gain a deep understanding of the subject matter. I would also like to thank Dr. Hiroji Kawai from POWDEC K.K, Japan for kindly supplying the GaN epitaxial wafers and for providing the GaN-on-Silicon samples, the characterisation of which led to a couple of world's first original scientific reports.

I would like to thank Dr. Ken Kennedy, Dr. Rob Airey and Saurabh Kumar from the National Centre for III-V technologies, Sheffield for the training and guidance provided during the process-flow development and device

fabrication/assembly activities undertaken during this research. I also want to thank Dr. Carsten Gollasch and Dr. Ibrahim Sari from the Southampton Nanofabrication Centre, University of Southampton for carrying out the processing of 3" PSJ GaN wafers at their facility.

I'd like to thank Dr. Mark Sweet for undertaking the mask design of large area devices and Dr. Hong Long, Ajith Balachandran and Priyanka De Souza who played instrumental roles with the verification and provided technical inputs during this extremely critical phase of the project. A special thanks to Dr. Hong Long for his efforts and active participation also in device fabrication and characterisation activities. I also want to thank each one of them for the numerous insightful discussions and critical brain-storming sessions especially during the design and process development of large area devices. I also want to thank Manoj Balakrishnan and Mahmood Alwash for helping me start-off with the ANSYS simulations.

Thanks to all my other friends and fellow researchers (Patrick, Turar, Keir, Leon, Alex, Maurice, Steve, Chen, Dan, An Shan, Jiangnan and Jason) at the Rolls Royce University Technology Centre in Advanced Electrical Machines, and the support staff at the Department of EEE. A special mention of thanks to Ms. Sara Gawthorpe, Ms. Hilary Levesley and Ms. Kim Brechin who have assisted me on numerous occasions with any of the departmental formalities.

Finally, I would like to take this opportunity to thank my parents, elder brother and my wife for their unswerving support, encouragement and for being extremely patient with my academic pursuits and exigencies outside of family life during the last four years.

Abstract

Gallium Nitride (GaN) based on its superior material properties is emerging as a strong candidate and a material of choice for next-generation power semiconductor device technologies.

The research presented in this thesis focusses on Polarisation Super Junction (PSJ) which is a promising technology for developing high voltage GaN power electronic devices. The research enabled the critical groundwork for scaling-up from Proof of Concept device test structures to large area high voltage PSJ GaN Transistors, Schottky Barrier Diodes, and PN Diodes with high power handling capability. Large area devices were fabricated on Sapphire and 6H-Silicon Carbide substrates and key determinants of the performance of scaled-up devices were identified through extensive electrical characterisation and numerical simulations. Implementation of an intrinsic diode within a high voltage GaN transistor and clamping capability during inductive switching was also demonstrated.

GaN-on-Silicon is emerging as the preferred route of technology development because of a cost-effective and mature Silicon (Si) platform. Along with development of discrete devices, there is also focus on monolithic integration in this platform. Performance assessment of monolithically integrated circuits (ICs) requires evaluation of crosstalk amongst the otherwise isolated devices. This phenomenon was comprehensively investigated and it was demonstrated that high voltage GaN-on-Si platform suffered from crosstalk issues, coupled through the Si substrate and that grounding the substrate substantially mitigated the crosstalk effects under static conditions. On the same platform, it was also observed that there was an increase in the on-state resistance (R_{ON}) of a GaN-on-Si transistor when configured as a High-Side switch of a half-bridge circuit, which is a common circuit topology for power conversion applications.

Crosstalk effects and increase in R_{ON}, are two major issues that will have to be addressed for developing high voltage monolithic GaN-on-Si solutions. These issues were identified and reported for the first time through this research.

List of Publications

Journal Publications:

1. **V. Unni**, H. Kawai, and E. M. Sankara Narayanan, "Increased static R_{ON} in GaN-on-silicon power transistors under high-side operation with floating substrate conditions," ***Electronics Letters***, vol. 51, no. 1, pp. 108–110, Jan. 2015.
2. **V. Unni**, H. Kawai, and E. M. Sankara Narayanan, "Crosstalk in monolithic GaN-on-Silicon power electronic devices," ***Microelectronics Reliability***, vol. 54, pp. 2242-2247, Aug. 2014.

Conference Publications:

1. **V. Unni**, H. Kawai, and E. M. Sankara Narayanan, "Crosstalk in monolithic GaN-on-Silicon power electronic devices," in ***Proc. ESREF***, Berlin, Germany, Sept. 29 – Oct. 2, 2014.
2. **V. Unni**, H. Long, M. Sweet, A. Balachandran, A. Nakajima, H. Kawai, and E. M. Sankara Narayanan, "2.4kV GaN Polarisation Superjunction Schottky Barrier Diodes on Semi-Insulating 6H-SiC Substrate," in ***Proc. IEEE ISPSD***, Waikoloa, Hawaii, United States, June 15-19, 2014, pp. 245–248.
3. T. Baltynov, **V. Unni**, and E. M. Sankara Narayanan, "The World's First High Voltage GaN-on-Diamond Power Devices," in ***Proc. ESSDERC***, Graz, Austria, Sept. 14-18, 2015.
4. T. Baltynov, **V. Unni**, and E. M. Sankara Narayanan, "Fabrication and Characterization of bidirectional GaN-on-Diamond HEMTs," ***UK Semiconductor Conference***, Sheffield, United Kingdom, July 1-2, 2015.
5. A. Nakajima, **V. Unni**, K. G. Menon, M. H. Dhyani, Y. Sumida, H. Kawai, and E. M. Sankara Narayanan, "GaN-based bidirectional super HFETs using polarisation junction concept on insulator substrate," in ***Proc. IEEE ISPSD***, Bruges, Belgium, June 3-7, 2012, pp. 265–268.

Table of Contents

List of Figures

List of Tables

Chapter 1 Introduction

1.1 Overview

The total world energy consumption is predicted to continue to rise to 619 quadrillion (10^{15}) British thermal units (Btu) in 2020 and 770 quadrillion Btu in 2035, indicating an increase exceeding 50% compared to the consumption of 505 quadrillion Btu in 2008 [1]. This expected trend has been shown in Fig. 1.1.

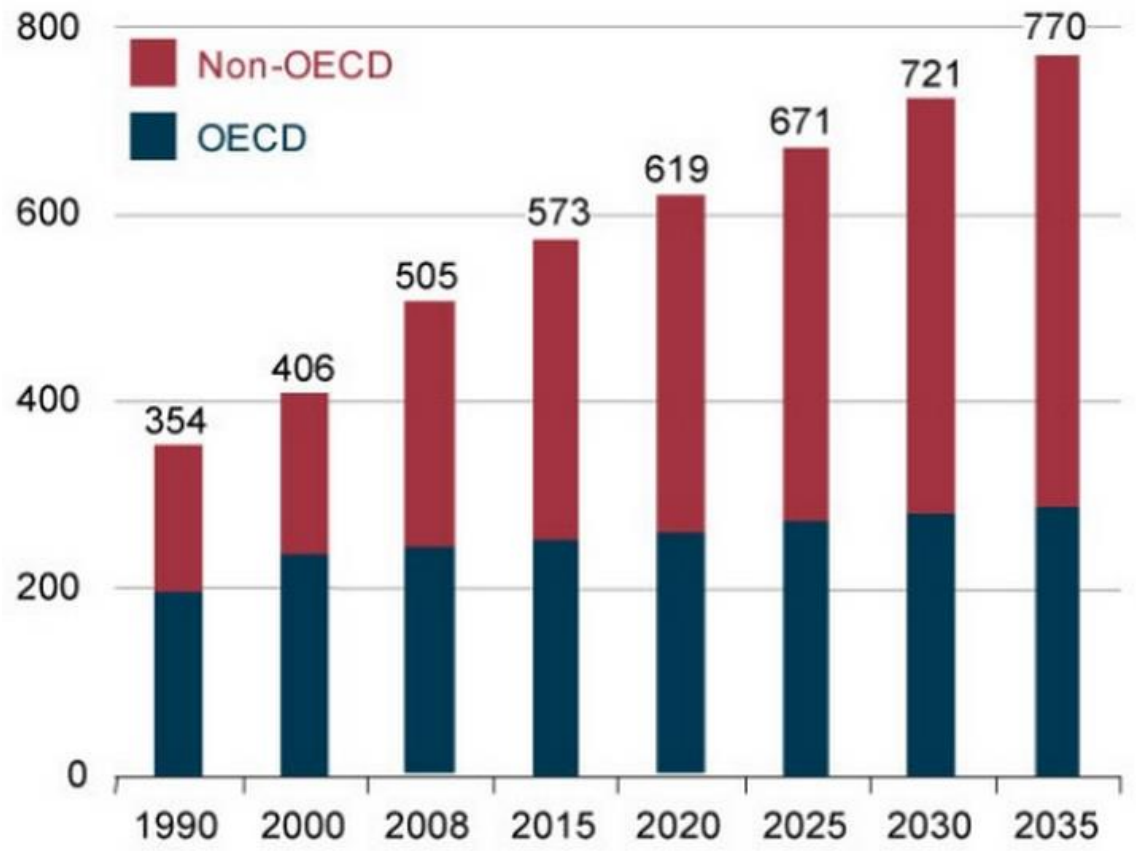


Figure 1.1 World energy consumption (quadrillion Btu), 1990-2035 [1]

With reliance on non-renewable energy sources such as coal, natural gas and petroleum expected to continue supplying much of the energy used worldwide [1], importance and relevance of energy efficiency cannot be over-emphasized. Along with energy efficiency, environmental friendliness, higher reliability, miniaturisation/portability, simpler management/maintenance, and cost-

effectiveness are becoming critical factors. These have also been some of the main driving factors towards "more electric/electronic" nature of systems. One of the key determinants of this transition is also the development of novel advanced power electronic systems which could be deployed in a whole new spectrum of applications ranging from traditional consumer and industrial segments to the niche automotive, aerospace and space sectors. With renewable energy sectors such as solar and wind energy gaining more prominence as energy sources, the role and expectations of power electronics have been ever increasing.

At the heart of any power electronic system are power semiconductor devices. There is a variety of these highly integral components which could be deployed as discrete devices or in combination to yield the power requirements of a given application.

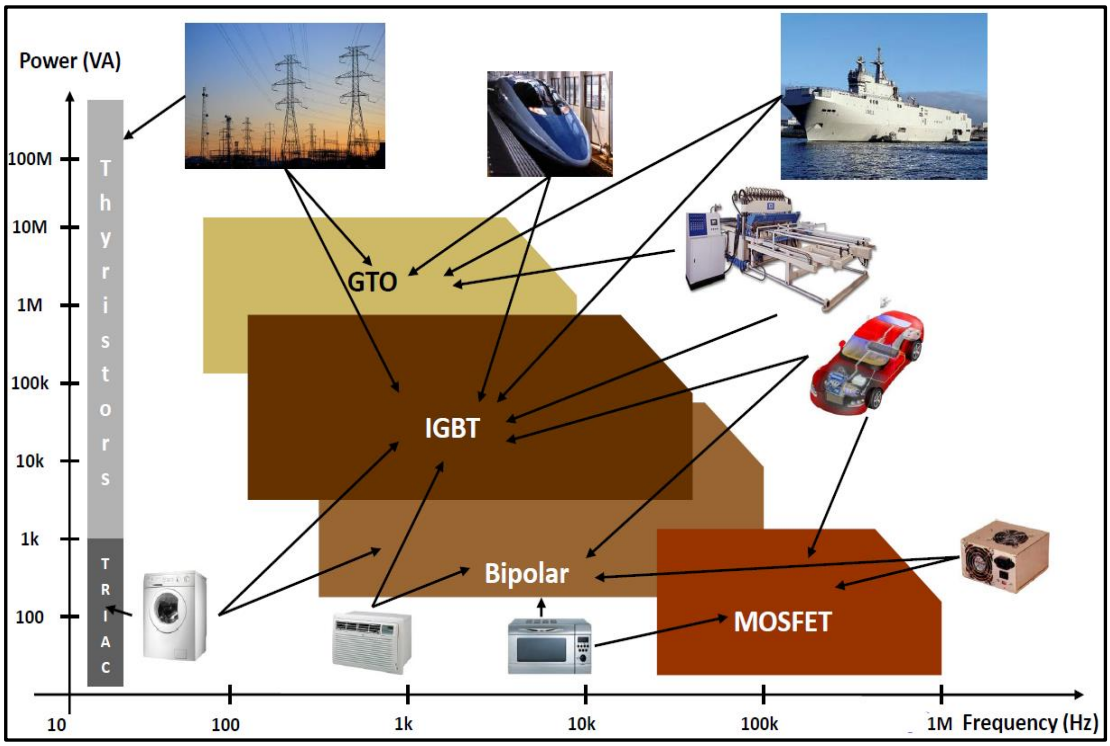


Figure 1.2 Power semiconductor devices and applications [2]

Fig. 1.2 depicts some of the main power semiconductor devices and applications with respect to operating power and switching frequency. A wide range of applications are covered by these devices such as consumer appliances, computers, transportation (automotive, marine and locomotives), power generation and transmission.

Global power semiconductor devices market was worth $11.5 billion in 2014 and by 2020 the total market is expected to be valued at $17 billion [3].

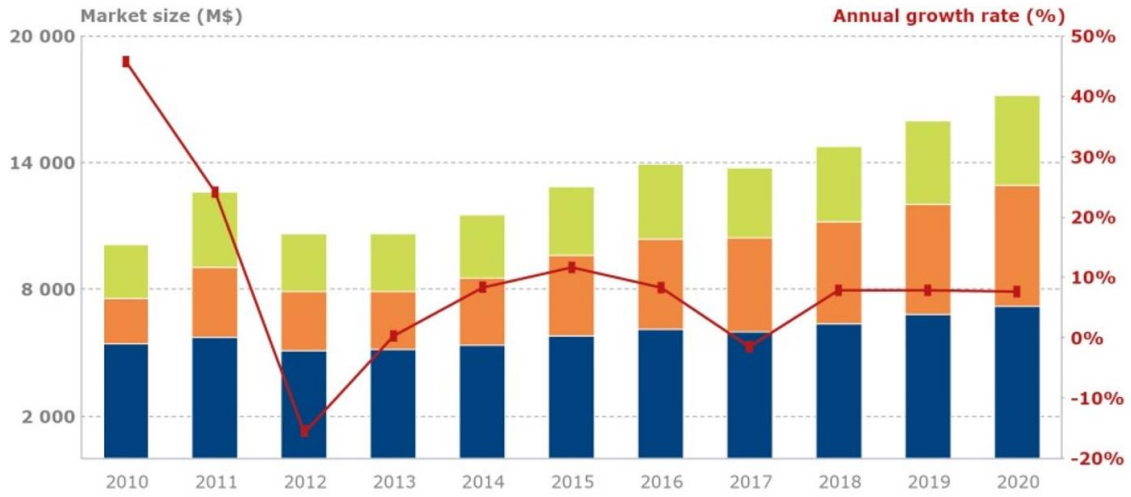


Figure 1.3 Global market for power semiconductor devices [3]

Fig. 1.3 shows the trend and projection of the global market for power semiconductor devices from 2010 - 2020. Fig. 1.4 shows the Total Available Market (TAM) split by voltage range in 2013. As can be observed, the major share of the market is for power devices within the voltage range of 400 V - 900 V (73%) followed by 1.2 kV - 1.7 kV (17%).

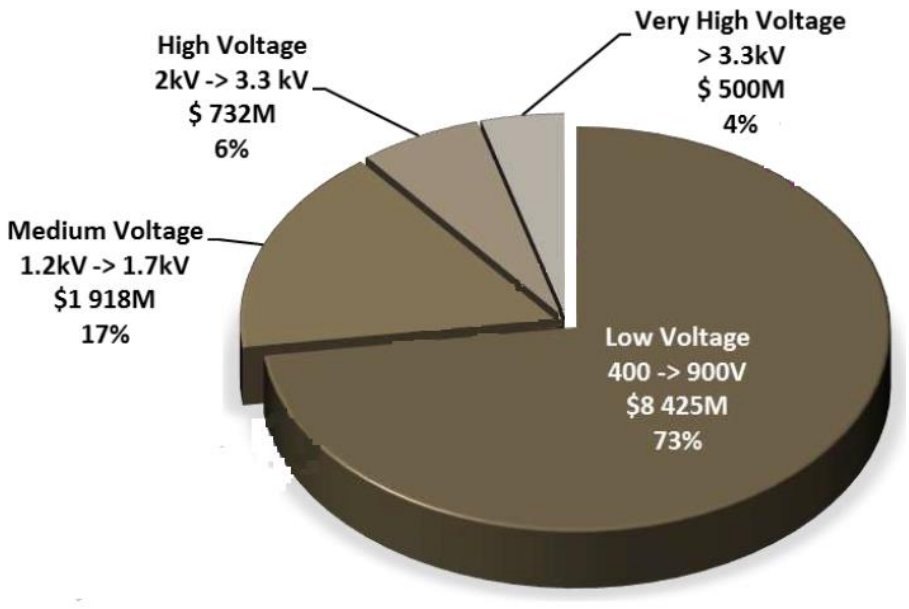


Figure 1.4 Power electronics market split by voltage range [4]

1.2 Gallium Nitride as a material for advanced power electronic devices

Approximately 87% of the current power semiconductor market is still dominated by Silicon (Si) based devices [5]. The performance of Si based power technologies has improved steadily and matured over the last three to four decades. Although Si power semiconductor technology has evolved with advances in Very Large Scale Integration (VLSI) technology and improvements in photolithography and cell integration, it is reaching a stage where improvements are incremental and with diminishing returns in an industry that is extremely cost-sensitive. Today, it is the intrinsic material properties of Si that is fundamentally limiting the enhancement in capability of the devices and thereby also limiting the efficiency and performance of power electronic systems. Also, practical operation of Si power semiconductor devices at ambient temperatures above 200 ^{0}C is difficult, as self-heating at higher power levels can result in high internal junction temperatures and leakage currents, which could compromise the functionality and reliability of the components [6].

To meet the future demands of energy consumption and effectively leverage the new era of applications in some of the high-end sectors, evolution and innovation in the area of microelectronic design as well as exploration of viable implementation on novel materials seems inevitable.

This expectation from future power semiconductor devices had been envisaged more than two decades ago and significant research in wide bandgap semiconductors, because of their superior intrinsic material properties, has been underway ever since. Today, limited success has also been achieved with respect to commercialisation of wide bandgap power semiconductor devices.

Parameter	Symbol	Si	3C-SiC	4H-SiC	GaN	Diamond
Bandgap	Eg (eV)	1.12	2.4	3.26	3.39	5.47
Critical Electric Field	Ec (MV/cm)	0.23	2.12	2.2	3.3	5.6
Electron Mobility	μ ($cm^2/V{\cdot}s$)	1400	800	950	1500	1800
Relative Permittivity	εr	11.8	9.7	9.7	9	5.7
Thermal Conductivity	λ ($W/m{\cdot}K$)	150	320	380	130	2000
Saturation Velocity	v_{sat} (10^7 cm/s)	1	2.5	2	2.5	2.7

Table 1.1 Intrinsic material properties of Si and major wideband gap semiconductors [6-7]

The intrinsic material properties of Si and major wide bandgap semiconductors (Silicon Carbide (SiC), Gallium Nitride (GaN), and Diamond) have been consolidated in Table 1.1. Wider bandgap of these materials can enable device operation at higher temperature and higher voltage when compared to Si-based devices due to a higher critical electric field. The definition and physical significance of critical electric field in the context of power semiconductor devices has been briefly described here.

The voltage blocking capability of a power semiconductor device is determined typically by the onset of avalanche breakdown within a depletion region that forms across either a P-N junction, or a metal-semiconductor junction within the structure, under high reverse bias voltage. The presence of high electric field in the depletion region leads to enhancement of energy associated with mobile carriers present within this region. An energised carrier can interact with lattice atoms of the semiconductor material and exchange energy that can excite an electron from the valence band to conduction band, leading to an electron-hole pair creation. This phenomenon is called impact ionisation. The newly created electron-hole pair being present in a region of high electric field also experiences acceleration and participates in the creation of further such pairs which can then contribute to additional creation of electron-hole pairs leading to a multiplicative process of significant carrier generation within the depletion region. As the magnitude of the applied reverse bias voltage increases, the multiplication of carriers continues to increase and at a certain voltage, there is an abrupt escalation in the number of carriers. From a theoretical perspective, at this voltage, the carrier multiplication approaches infinity and the device is said to undergo avalanche breakdown. The maximum value of the electric field (localised anywhere within the depletion region of a semiconductor structure) at which avalanche breakdown is initiated is defined as the critical electric field [8].

It needs to be highlighted that non-destructive avalanche breakdown in GaN has only been demonstrated in vertical power devices fabricated on bulk GaN substrates and remains elusive in the case of lateral devices where a destructive behaviour is observed. This creates an uncertainty on the actual mechanism that determines electrical breakdown in lateral GaN devices that are typically fabricated on non-native substrates which leads to high density of crystal defects within device structures, and therefore requires further investigation.

The high-frequency switching capability of a device for a given semiconductor material is directly proportional to its carrier drift velocity. The electron saturation drift velocity (v_{sat}) of GaN is more than twice that of Si and is higher than that of 4H-SiC. With proper thermal management, this property can be leveraged for fast switching devices. Higher drift velocity enables faster removal of charge in the depletion region during high-frequency switching and therefore, the reverse recovery current/time of GaN based diodes is expected to be considerably smaller [7]. Radiation hardness is also a property of wide bandgap materials that could be leveraged in applications (e.g. satellite/space electronic systems...) where exposure to strong ionising cosmic radiation is a major challenge.

Table 1.2 depicts the figures of merit (FOM) normalised to that of Si, measuring suitability of a semiconductor material primarily for power electronic applications based on certain intrinsic material properties.

FOM	Silicon	3C-SiC	4H-SiC	GaN	Diamond
BFOM ($\varepsilon r \cdot \mu \cdot Ec^3$)	1	368	488	2414	8964
BHFOM ($\mu \cdot Ec^2$)	1	49	62	221	762
JFOM ($Ec \cdot vsat/2\pi)^2$	1	531	366	1287	4322
KFOM ($\lambda \cdot \sqrt{(vsat/\varepsilon r)}$)	1	3.7	4.0	1.6	31.5
HMFOM ($Ec\sqrt{\mu}$)	1	7	8	15	28
HCAFOM ($\varepsilon r Ec^2\sqrt{\mu}$)	1	53	62	163	325
HTFOM ($\lambda/(\varepsilon r \cdot Ec)$)	1	0.28	0.32	0.08	1.13

Table 1.2 Normalised FOM of major wideband gap semiconductors [9-10]

BFOM is Baliga's figure of merit for power switching and suitable for comparing materials when the losses in the devices are dominated by conduction losses. BHFOM is Baliga's high frequency figure of merit, which accounts for switching losses due to charging and discharging of the input capacitance of a power Field Effect Transistor (FET). JFOM is Johnson's figure

of merit which estimates the transistor cut-off frequency and maximum allowable applied voltage. It is suitable for comparing devices for applications requiring high-frequency signal amplification [10]. KFOM is Keyes's figure of merit considering thermal limitations and is primarily determined by the thermal conductivity of the material. HMFOM is Huang's material figure of merit that is inversely proportional to total losses of a power switching device (conduction and switching losses). HCAFOM is Huang's chip area figure of merit and is inversely proportional to chip area of a power device. HTFOM is Huang's thermal figure of merit and can be used to estimate the rise in junction temperature of the device for a given material and operating condition. HTFOM calculation assumes that the devices have been optimised for chip area (considering conduction and switching losses). Hence, with the most optimal chip area of devices, the rise in junction temperature for a given operating condition will be actually higher in GaN and SiC when compared to Si, as suggested by this figure of merit.

One has to be careful while considering the above-mentioned figures of merit, as they are derived with certain assumptions about the material properties, sometime focussing on specific attributes and do not provide the complete picture when viewed independently. A simple example is that of the values assumed for carrier mobility, which in the case of GaN needs to be carefully chosen depending on whether the carriers are in the bulk or the two-dimensional electron gas (2DEG) that forms at the AlGaN/GaN interface of a heterostructure. The electron mobility of 2DEG at room temperature can easily be greater than twice the magnitude observed in the bulk of the material and there by alter the calculated FOM or perceived advantage of a given material.

Nevertheless, except for KFOM and HTFOM, the other FOMs clearly establish the superiority of GaN over SiC and Si, as a choice of material for power

switching devices. The only aspect limiting its performance over SiC is its thermal conductivity. While this can be a misnomer, were a lateral GaN device to be fabricated over a highly thermally conducting substrate, it would have the potential to operate over wide ranging temperatures from cryogenic to as high as 500^0 C. Recent advances in bulk GaN crystal growth capability have significantly enhanced the thermal properties of GaN substrates and can enable performance comparable to that of the GaN on SiC substrates [11].

Although 3C-SiC and 4H-SiC are also strong contenders, their utilisation in power electronics is more suited for applications with operating voltage above 1.2 kV, where thermal management issues could be more challenging for GaN based devices to be addressed in a cost-effective manner. Although diamond is often referred to as the ultimate semiconductor material, currently, poly crystalline CVD diamond is primarily being pursued as a material for heat spreaders and substrates. Single crystal diamond substrates are also now available in the market, however only in the size range of a few millimetres. Moreover, n-type doping is difficult to achieve in diamond and any practical power electronic device development is only anticipated in a few years' time. The main application segment for diamond devices will still be very niche due to economic reasons and primarily with operating voltage in the range of a few 10s of kV, which is not the target application segment of GaN power switching devices, based on the current situation.

Today, a majority of GaN power semiconductor devices are fabricated with hetero-epitaxial GaN on Sapphire, SiC or Si substrates. Substrate material properties have a direct impact on the epitaxial crystal quality as well as the quality of the fabricated devices. Substrates also play a major role in determining the suitability of the devices for high power/temperature applications. For example, presently, Si is ubiquitous, but its thermal

performance remains a limitation. The table below briefly summarises key substrate properties which directly impact the performance of devices fabricated with this approach.

Substrate Material Property	2H-GaN (Hexagonal)	Sapphire (Rhombohedral)	Silicon (Cubic)	6H-SiC (Hexagonal)	3C-SiC (Cubic)	Diamond (Cubic)
Lattice constant (Å) (Mismatch %)	3.189 (0%)	4.758 (13.8%)	5.431 (16.9%)	3.080 (3.57%)	4.359 (3.0%)	3.567 (11.8%)
Thermal conductivity (W/cm.K)	1.3	0.3	1.5	4.9	3.6	20.0
Co-efficient of Thermal expansion (linear) 10^{-6}/K	5.5	7.5	3.6	4.5	3.9	1.0

Mismatch (%) between 2H-GaN and respective substrates in the first row is the effective lattice mismatch observed after crystal growth optimization considering lattice constant and crystal orientation differences

Table 1.3 Substrate materials for GaN Power devices [12-16]

High lattice mismatch between GaN epitaxial layer and the underlying substrate leads to high density of crystal defects, stacking faults and dislocations, which translate to paths for leakage currents and trap states that could compromise the static and dynamic performance of the devices. Thermal conductivity is another property of substrates that is critical from the perspective of heat dissipation and thermal management of devices. Substrates with low thermal conductivity can limit the power density and high temperature performance, otherwise achievable by GaN based devices. Mismatch in terms of co-efficient of thermal expansion (CTE) can lead to thermally induced mechanical strain in the structure and make it more prone to crack generation for thick epitaxial films, during thermal cycling.

High percentage of lattice mismatch (shown in brackets, in Table 1.3), thermal expansion mismatch and low thermal conductivities are the main performance limiting attributes for both Sapphire and Si substrates. Electrical and mechanical performance as well as reliability can get compromised in such

heterostructures due to the risk of perpetual thermal stress during device operation.

These limitations can be effectively overcome by developing heterostructures on substrates like 6H-SiC and 3C-SiC, which have significantly lower mismatch in terms of lattice constant or CTE and have values of thermal conductivity that are three to four times that of Si and more than ten times better than that of Sapphire. It has also been demonstrated that current collapse/dispersion (increase in dynamic conduction losses and lower output power at high electrical stress/frequency operation) is significantly lower for devices fabricated on SiC substrates, when compared to Sapphire [17]. This is crucial from functionality as well as reliability of high-frequency and high voltage power switching devices.

Moreover, using substrates such as semi-insulating SiC, in lieu of Si substrate can also be effective in minimising crosstalk between monolithic devices and can offer a more effective isolation between devices. The feature of effective Device-to-Device and Device-to-Substrate isolation, could pave the way forward for development of high voltage GaN monolithic power converters and integrated circuits (ICs).

1.3 Objectives and scope of this research work

Superjunction revolutionised Si power MOSFETs by taking the device performance beyond the theoretical limit with an innovative method of charge compensation in the structure and enhanced field shaping which translates to higher operating voltage capability for a given drift length. Polarisation Super Junction (PSJ) is a unique high voltage GaN technology that achieves the same by engineering of positive and negative polarisation charges inherent in the GaN material structures.

Proof of Concept (PoC) GaN devices (Diodes and Transistors) on Sapphire substrates based on PSJ concept were demonstrated in 2011 at the University of Sheffield (Fig. 1.5).

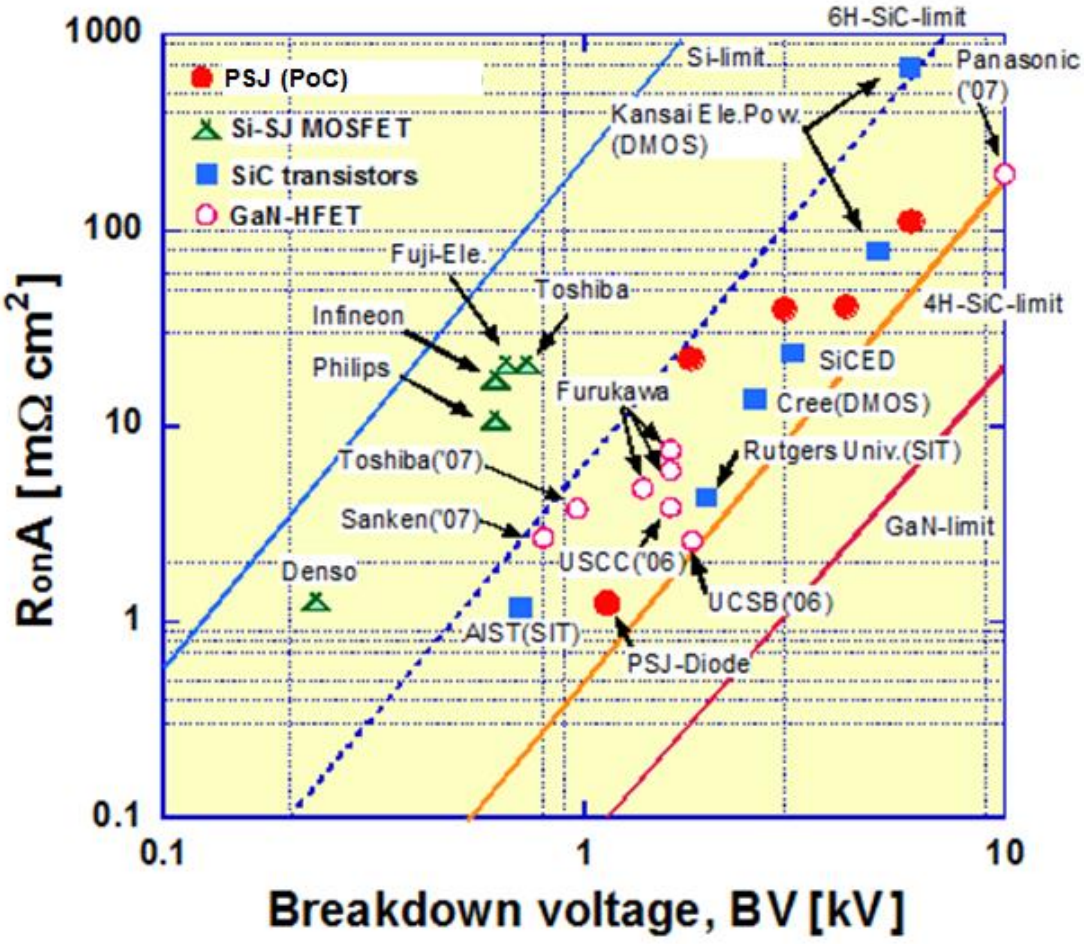


Figure 1.5 Theoretical and reported specific on-state resistance vs. breakdown voltage

The focus of the research presented in this thesis has primarily been two-fold.

The first being, enabling the scaling-up process from PoC device test structures to large area high voltage PSJ GaN devices with various current handling capabilities. Apart from being on the natural course of technology/product development, the performance of a scaled-up device provides the true demonstration of the capability of a given technology and scaled-up devices can be characterised in a manner that is more representative of an actual

application. The scaling-up of a high power device also presents numerous design and processing challenges that are not encountered during the development of PoC structures.

The second area of focus has been evaluating the performance of PSJ devices in GaN-on-Si technology platform as well as identifying challenges to monolithic integration. GaN-on-Si technology platform has gained substantial leverage as the chosen platform for device development due to the potential of cost parity with the incumbent Si devices. Monolithic integration as an approach to harness the full potential of GaN is also gaining traction, making the findings of this research extremely relevant and timely.

1.4 Outline of the thesis

The report is organised as follows.

In *chapter 1*, there is a brief overview of the key driving factors towards "more electric/electronic" nature of systems, transition from Si towards wide bandgap semiconductor materials and emergence of GaN as a strong contender for current and next-generation power electronic applications.

Chapter 2 describes the fundamentals of GaN material physics and High Electron Mobility Transistor (HEMT) technology in the context of application for power electronics. Device architecture, main electrical characteristics, high voltage techniques of RESURF, Superjunction and Field-plate engineering – that are employed for high voltage capability, as well as principles of device-operation are discussed in detail.

Chapter 3 introduces the concept of Polarisation Super Junction (PSJ) and presents an elaborate description of the device design, approach for scaling-up, process-flow development, mask design, process optimisation challenges and device fabrication.

Extensive electrical characterisation results of a whole range of fabricated devices at wafer-level as well as post-assembly results of the large area devices have been described in *Chapter 4*. The ideas and approach for chip-scale flip-chip packaging have also been briefly discussed and some of the pilot results have been presented.

Chapter 5 initially presents the key electrical characterisation results of GaN PSJ Diodes on Si substrates. The latter part of the chapter focusses on challenges to monolithic integration in GaN-on-Si platform. Investigation of crosstalk effects in monolithically fabricated devices on a 650 V, PSJ GaN-on-Si technology platform have been discussed in detail. The issue of increased on-state resistance of PSJ HFETs in this platform when characterised for High-Side operation in a half-bridge configuration has also been presented. The investigation methodology and dependence of the observed behaviour under various operating conditions have been discussed in detail.

Finally in chapter 6, concluding remarks are presented and direction of future research has been discussed.

1.5 References

[1] U.S Energy Information Administration. 2011. International Energy Outlook [Online]. Available: http://www.eia.gov/forecasts/ieo.

[2] Yole Developpement. 2010. High Voltage Power Electronic market & technology trends [Online]. Available: http://www.i-micronews.com/upload/Rapports/ Yole_HVPE_report_sample.pdf.

[3] Yole Developpement. 2015. Status of power electronics industry 2015 [Online]. Available: http://www.i-micronews.com/power-electronics-report/product/status-of-power-electronics-industry-2015.html.

[4] Yole Developpement. 2013. Wide Band Gap Power Electronics: A Path Toward CO_2 Emission Decrease [Online]. Available:

http://www.semiconwest.org/sites/semiconwest.org/files/data14/docs/SW2014_Eric%20Virey_Yole%20%20Developpment.pdf.

[5] Semiconductor Today. 2015. Innovations to sustain silicon's 87% share of power electronics market versus wide-bandgap materials [Online]. Available: http://www.semiconductor-today.com/news_items/2015/jun/lux_020615.shtml.

[6] P. G. Neudeck, R. S. Okojie, and L. Y. Chen, "High-Temperature Electronics - A Role for Wide Bandgap Semiconductors," *Proceedings of the IEEE*, vol. 90, no. 6, pp. 1065-1076, 2007.

[7] B. Ozpineci, and L. M. Tolbert. 2003. Comparison of wide-bandgap semiconductors for power electronics applications [Online]. Available: http://www.ornl.gov/ ~webworks/cppr/y2001/rpt/118817.pdf.

[8] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*. New York: Springer, 2008.

[9] N. Kaminski, "State of the art and the future of wide band-gap devices," in *Proceedings of the 17th European Conference on Power Electronic Applications*, 2009, pp. 1–9.

[10] A. Q. Huang, "New Unipolar Switching Power Device Figure of Merit," *IEEE Electron Device Letters*, vol. 25, no. 5, pp. 298 - 301, 2004.

[11] N. Killat, M. Montes, J. W. Pomeroy, T. Paskova, K. R. Evans, J. Leach, et al., "Thermal Properties of AlGaN/GaN HFETs on Bulk GaN Substrates," *IEEE Electron Device Letters*, vol. 33, no. 3, pp. 366-368, 2012.

[12] L. M Sorokin, A. E. Kalmykov, A. V. Myasoedov, N. V Veselov, V. N. Bessolov, N. A. Feoktistov et al., "Structural characterisation of GaN/AIN layers on 3C-SiC/Si(111) by TEM," in *Proceedings of the 17th International Conference on Microscopy of Semiconducting Materials*, 2011.

[13] C. R. Miskys, M. K. Kelly, O. Ambacher, and M. Stutzmann, "Freestanding GaN-substrates and devices," *Physica Status Solidi* (c), vol. 0, no. 6, pp. 1627-1650, 2003.

[14] P. R. Hageman, J. J. Schermer, and P. K. Larsen, "GaN growth on single-crystal diamond substrates by metalorganic chemical vapor deposition and hydride vapour deposition," *Thin Solid Films*, vol. 443, pp. 9-13, 2003.

[15] T. W. Kim, D. U. Lee, H. S. Lee, J. Y. Lee, J. H. Lee, and J. H. Lee, "Microstructural properties and atomic arrangements in GaN/sapphire and AlxGa1−xN⁄AlN⁄GaN⁄sapphire heterostructures," *Journal of Applied Physics*, vol. 96, no. 12, pp. 7118-7121, 2004.

[16] S. Q. Zhou, A. Vantomme, B. S. Zhang, H. Yang, and M. F. Wu, "Comparison of the properties of GaN grown on complex Si-based structures," *Applied Physics Letters*, vol. 86, pp. 081912-1- 081912-3, 2005.

[17] S. Arulkumaran, T. Egawa, H. Ishikawa, and T. Jimbo, "Comparative study of drain-current collapse in AlGaN/GaN high electron-mobility transistors on sapphire and semi-insulating SiC," *Applied Physics Letters*, vol. 81, no. 16, pp. 3073-3075, 2002.

Chapter 2 Fundamentals of Gallium Nitride HEMT Technology

In this chapter, the intrinsic material structure and polarisation effects in Gallium Nitride (GaN) will be discussed initially. Following that, there will be a discussion of conventional AlGaN/GaN High Electron Mobility Transistor (HEMT) Technology. Details of device operation and main electrical parameters in the context of high voltage power electronics will be presented.

2.1 GaN Material Structure and theory of Polarisation

GaN is a binary III-V direct wide bandgap semiconductor material, and is one of the most extensively researched nitride semiconductors. There are three common crystal structures shared by III-V nitrides: wurtzite, zinc blende, and rock salt structure, with wurtzite being the thermodynamically stable structure under standard ambient conditions [1].

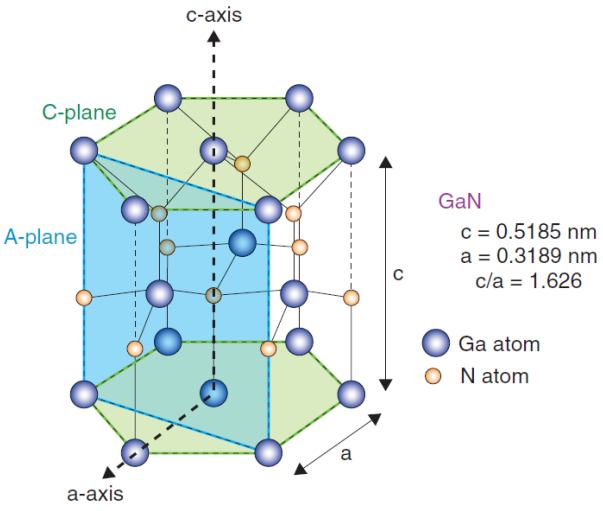


Figure 2.1 Wurtzite crystal structure of GaN [2]

Wurtzite which is a hexagonal close-packed (HCP) structure (as shown in Fig. 2.1) is also the most commonly employed GaN crystal structure for power, RF and optoelectronic applications. In a binary compound semiconductor, when two different atoms form a chemical bond, the difference in their electro-negativities can effectively cause a dipole to exist across the atomic bond. This dipole could induce a net polarisation across a macroscopic layer if the

symmetry of the crystal allows it. In a cubic crystal structure, the dipole moments of the atomic bonds cancel out, and therefore in the absence of an external strain do not produce any net polarisation across the crystal. In III-V nitride semiconductors, the atomic crystal arrangement (non centro-symmetric) is such that a net dipole moment exists even in the absence of an applied strain [3]. This is referred to as spontaneous polarisation (P_{SP}), and is oriented parallel to the [0001] direction or only along the c-axis in wurtzite GaN.

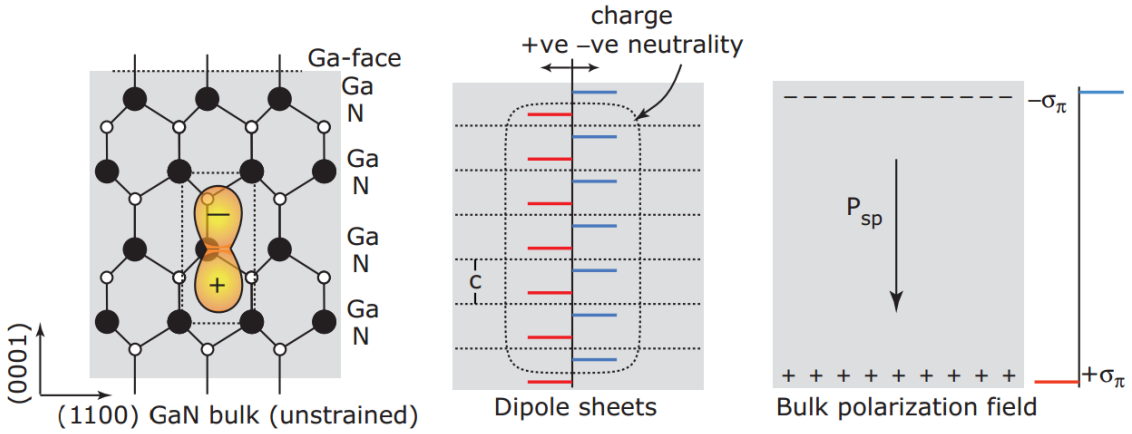
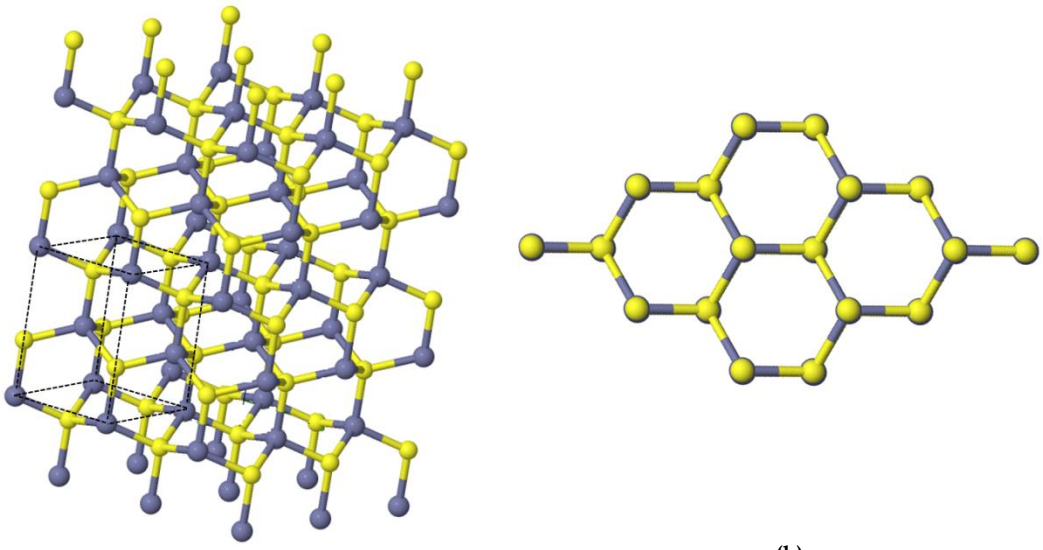


Figure 2.2 Schematic illustration of spontaneous polarisation in unstrained bulk GaN (Ga-face) [4]

The nature and orientation of spontaneous polarisation (P_{SP}) in unstrained bulk GaN (Ga-face) has been illustrated in Fig. 2.2. Each tetrahedral unit cell can be considered to be constituted of a charge dipole that is formed due to the spatial separation of the centroids of the negative charge due to the electron clouds and the positive charge due to the nuclei. Although the dipoles neutralise each other in the bulk of the semiconductor, sheet charges of $\pm \sigma_\pi$ are formed on the top and bottom surfaces. A free Ga-face surface thus develops a sheet charge of negative polarity, and a sheet charge of positive polarity is formed on the N-face surface [4].

Although these surface charges are immobile, they can nevertheless interact and influence mobile charge carriers within the material system. This aspect is leveraged in the design and engineering of heterostructure based GaN devices.



(a) (b)

Figure 2.3 Schematic of (a) 3D-crystal structure of wurtzite (b) plan view [5]

The presence of spontaneous polarisation in wurtzite structures can be understood by exploring the crystal structure further. Fig. 2.3 shows the 3D-crystal structure as well as the plan view of the wurtzite structure. In the case of Ga-face GaN, the grey balls represent the Gallium atoms, and yellow balls represent the Nitrogen atoms. The HCP nature of the structure is clearly illustrated in the plan view (Fig. 2.3. (b)). In the 3D-crystal structure shown in Fig. 2.3 (a), the unit cell has been demarcated using dashed lines, and has also been shown in greater detail in Fig 2.4 below:

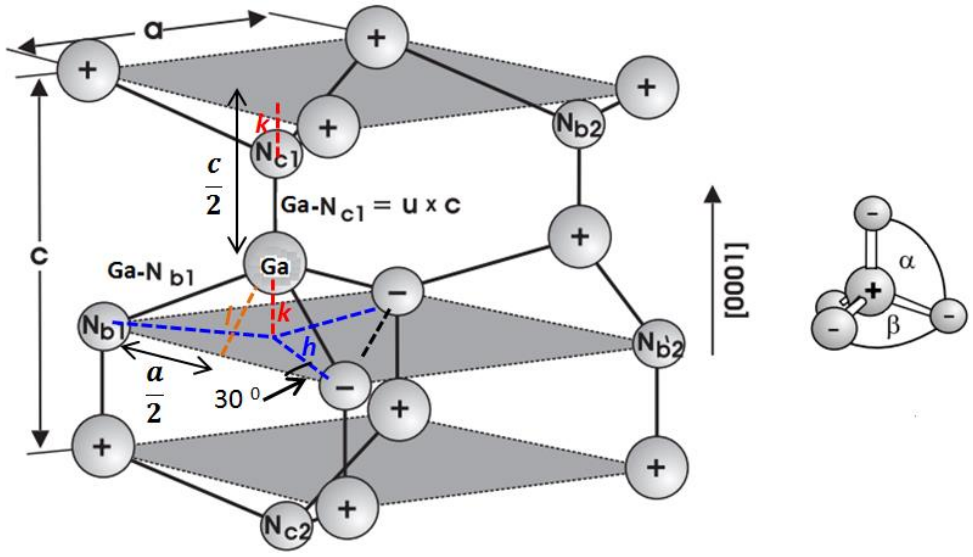


Figure 2.4 Schematic drawing of the unit cell with lattice constants *a* and *c* [3]

Based on [3], the lattice constant in the basal plane and along the vertical c-axis have been labelled as *a* and *c* respectively. The length of the bond Ga-N_{c1} is *uc*, where *u* is the ideal cell internal parameter defined as 3/8 for an ideal wurtzite crystal structure. In an ideal wurtzite crystal, the bond lengths are equal. Therefore, bond lengths Ga-N_{b1} and Ga-N_{c1} are equal. With the aid of Fig. 2.4, the expressions for bond lengths and ideal cell internal parameter have been derived below:

$$\text{Bond length Ga-}N_{b1} = \sqrt{h^2 + k^2} \qquad (2.1)$$

$$\text{Bond length Ga-}N_{c1} = uc \qquad (2.2)$$

$$h = \frac{a}{2} / \cos 30^0 \ (\cos 30^0 = \sqrt{\frac{3}{2}}) \ \Rightarrow \ h = \frac{a}{\sqrt{3}} \qquad (2.3)$$

$$k = \frac{c}{2} - uc \qquad (2.4)$$

$$\text{Therefore, Ga-}N_{B1} = \sqrt{\frac{1}{3}a^2 + \left(\frac{1}{2} - u\right)^2 c^2} \qquad (2.5)$$

For an ideal structure (from 2.1 and 2.2)

$$uc = \sqrt{h^2 + k^2} \qquad (2.6)$$

$$\Rightarrow \quad uc = \sqrt{\frac{1}{3}a^2 + \left(\frac{1}{2} - u\right)^2 \, c^2} \tag{2.7}$$

In an ideal HCP structure, $c/a = \sqrt{\frac{8}{3}} = 1.633$ [6]. Inserting that into equation 2.7 yields $u = \frac{3}{8}$.

In Fig 2.4,

Bond angle α = angle between Ga-N_{c1} and Ga-N_{b1}

$$\alpha = \frac{\pi}{2} + \cos^{-1}\left(\frac{h}{\sqrt{h^2+k^2}}\right) \tag{2.8}$$

$$\alpha = \frac{\pi}{2} + \cos^{-1}\left\{\left(\sqrt{1 + 3\left(\frac{c}{a}\right)^2\left(\frac{1}{2} - u\right)^2}\right)^{-1}\right\} \tag{2.9}$$

Bond angle β = angle between Ga-N_{b1} and Ga-$N_{b1'}$

$$\frac{\beta}{2} = \sin^{-1}\left\{\frac{a/2}{Ga-N_{b1}}\right\} \tag{2.10 a}$$

$$\frac{\beta}{2} = \sin^{-1}\left\{\frac{a/2}{\sqrt{\frac{1}{3}a^2+\left(\frac{1}{2}-u\right)^2 c^2}}\right\} \tag{2.10 b}$$

$$\beta = 2\sin^{-1}\left\{\left(\sqrt{\frac{4}{3} + 4\left(\frac{c}{a}\right)^2\left(\frac{1}{2} - u\right)^2}\right)^{-1}\right\} \tag{2.10 c}$$

Considering that the ideal structure will have $c/a = \sqrt{\frac{8}{3}} = 1.633$ and $u = \frac{3}{8}$.

$$\alpha = \frac{\pi}{2} + \cos^{-1}(0.942809) \tag{2.11}$$

$$\alpha = 109.47^{0}$$

$$\beta = 2\sin^{-1}(0.816496) \tag{2.12}$$

$$\beta = 109.47^{0}$$

Therefore, in the ideal wurtzite crystal structure, the bond angles α and β are both equal to 109.47 ^{0}.

Nann and Schneider have reported in [7] on the origin of permanent electric dipole moments in wurtzite nanocrystals, and attributed it to deviation from the ideal wurtzite crystal structure. The schematic of the structure used in this simple model has been shown in Fig. 2.5.

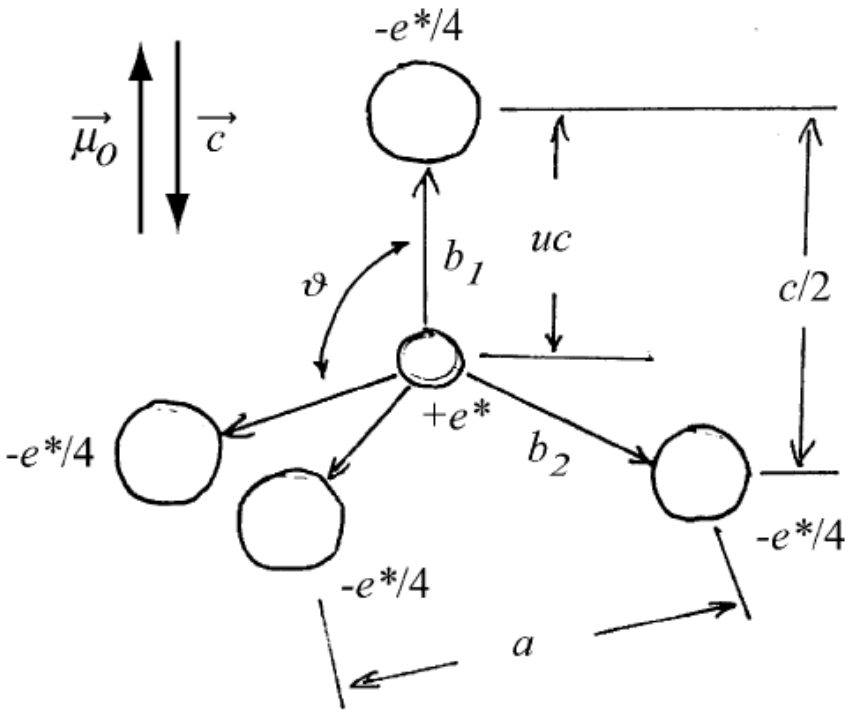


Figure 2.5 Point charge model for explaining the occurrence of a permanent electric dipole moment in the real wurtzite structure [7]

The permanent electric dipole moment μ_0 can be expressed as a resultant vector, due to the influence of the individual dipole moments across each of the four bonds of the tetrahedron. This can be expressed as

$$\mu_0 = \frac{e^*}{4}[u - \frac{3}{8}]c \qquad (2.13)$$

Based on equation 2.13, the net dipole moment in an ideal structure will vanish (u = 3/8). Although this approach is very intuitive, it is not sufficient to conclude on the presence of spontaneous polarisation in a given material, as that also

depends on the overall symmetry of the crystal structure. For example, there is no spontaneous polarisation in GaN when it crystallises in zinc blende structure and that is attributed to the higher symmetry of the cubic crystal structure.

It has been known that there is an inherent deviation from ideality in real wurtzite binary group III nitrides. This non-ideality for parameters such as u, c/a, bond lengths M-N_{c1} and M-N_{b1}, bond angles α and β, based on [3] have been quantified for InN, GaN, and AlN in Fig. 2.6.

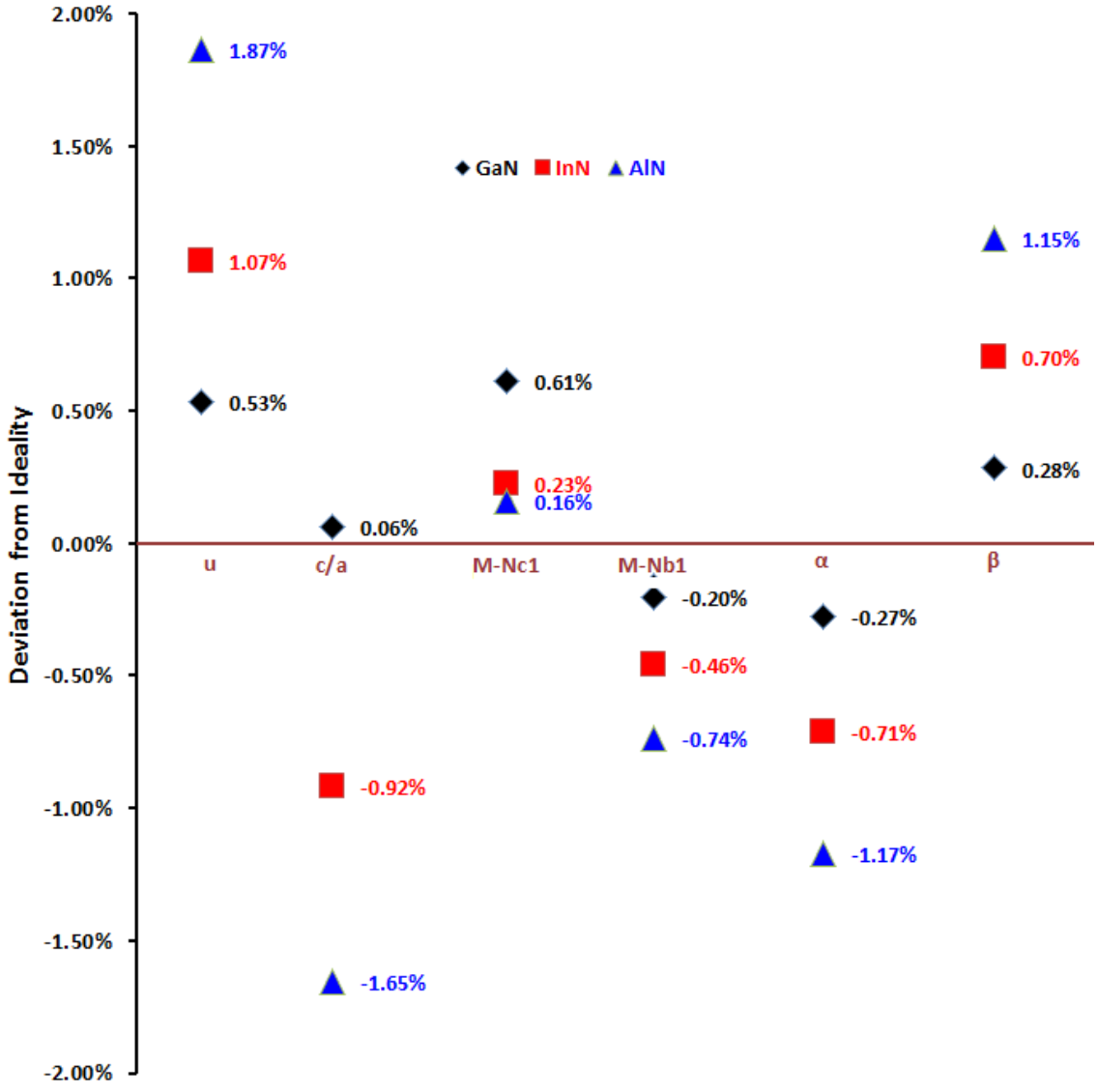


Figure 2.6 Deviation from ideality for III-nitrides in real wurtzite structures (based on [3])

As can be clearly observed, deviation from ideality is the smallest for GaN, for each of the structural parameters. Higher magnitudes of deviation are observed for InN and AlN, with AlN showing the highest deviation from ideality. This correlates well with the magnitudes of spontaneous polarisation coefficients in each of these materials, as shown in Fig. 2.7 (a). The spontaneous polarisation (P_{SP}) of the random ternary group-III-nitride alloys with a mole fraction x is approximated by the following quadratic expression [8]:

$$P_{SP}(A_xB_{1-x}N) = xP_{SP}(AN) + (1-x)P_{SP}(BN) + b_{(ABN)}\,x\,(1-x) \qquad (2.14)$$

where A, B refer to the group III elements, b refers to the bowing parameter and is defined as

$$b_{(ABN)} = 4P_{SP}(A_{0.5}B_{0.5}N) - 2[P_{SP}(AN) + P_{SP}(BN)] \qquad (2.15)$$

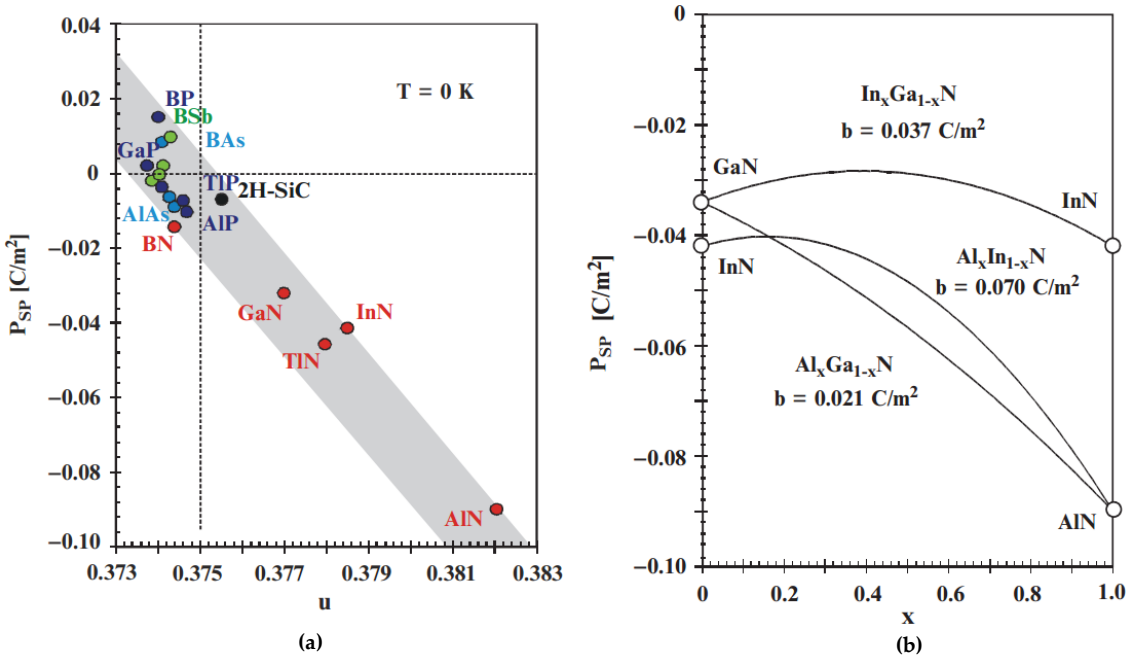


Figure 2.7 Theoretical predictions of spontaneous polarisation in (a) wurtzite compound semiconductors (u is the cell internal parameter) (b) ternary alloys with wurtzite crystal structure (x is the mole fraction) [9]

As shown in Fig. 2.7 (b), the magnitude of P_{SP} gets altered depending on the mole fraction in ternary alloys. The non-linear behaviour of P_{SP} has been

attributed to a non-linear change in cell internal parameter with respect to the mole fraction and also to the differences in electronegativity of the constituent group III- elements of the alloys [9].

With spontaneous polarisation inherent in wurtzite III-V semiconductors, the effective polarisation also gets altered in the presence of mechanical strain on the material, as can happen in pseudomorphically grown heterostructures with dissimilar lattice constants. This component of polarisation caused due to strain and which is observed to be significantly high in III-V Nitrides when compared to other III-V compound semiconductors, is referred to as piezoelectric polarisation. The piezoelectric component of polarisation caused by bi-axial strain in a material is given by [8, 10]:

$$P_{PZ} = 2(e_{31} - e_{33}\frac{C_{13}}{C_{33}})\varepsilon, \qquad (2.15)$$

where e_{31} and e_{33} are the piezoelectric coefficients, C_{13} and C_{33} are the elastic constants, and ε is the in-plane strain in the crystal given by:

$$\varepsilon = \frac{a*-a_0}{a_0}, \qquad (2.16)$$

where a^* and a_0 are the lattice constants of the strained and the originally relaxed layer respectively. Piezoelectric coefficient is the magnitude of the induced polarisation per unit of mechanical strain. Assuming a standard Cartesian coordinate system, the coefficient e_{31} refers to the component of the induced polarisation along z (3) axis in the presence of strain along the x (1) axis (change in the lattice constant a) and e_{33} refers to the component of induced polarisation along z (3) axis in the presence of strain along the z (1) axis (change in the lattice constant c). Elastic constants provide a relationship between components of deformation or strain tensor and the components of stress tensor for a given crystal, as governed by Hooke's law. The elastic constants C_{13} and

C_{33} provide the magnitude of mechanical stress generated along x (1) axis and z (3) axis respectively, per unit of strain along the z (3) axis.

The mechanical and piezoelectric constants for three binary nitride semiconductors have been consolidated in Table 2.1 [11-12].

Material	**Lattice Constant a_0 / c_0 (Å)**	**e_{33} (C/m^2)**	**e_{31} (C/m^2)**	**C_{13} (GPa)**	**C_{33} (GPa)**
GaN	3.189 / 5.185	0.73	-0.49	103	405
InN	3.544 / 5.718	0.97	-0.57	92	224
AlN	3.111 / 4.978	1.46	-0.6	108	473

Table 2.1 III-V Nitride material parameters [11-12]

As shown in Fig. 2.8, the in plane lattice constants (a(x)) for ternary alloys linearly change with mole fraction. Based on equation (2.15), the magnitude of piezoelectric polarisation (P_{PZ}) is directly proportional to the in-plane strain or how the lattice constant of the ternary alloy is altered. In the case of AlGaN alloys, as the Al mole fraction increases, the lattice constant decreases in magnitude. When such a layer is pseudomorphically grown on a relaxed GaN layer, the AlGaN layer experiences a tensile strain due to the larger lattice constant of underlying GaN layer. Fig. 2.8 clearly shows that there is a strong correlation between modification of lattice constant and the resultant piezoelectric polarisation (P_{PZ}) in the material.

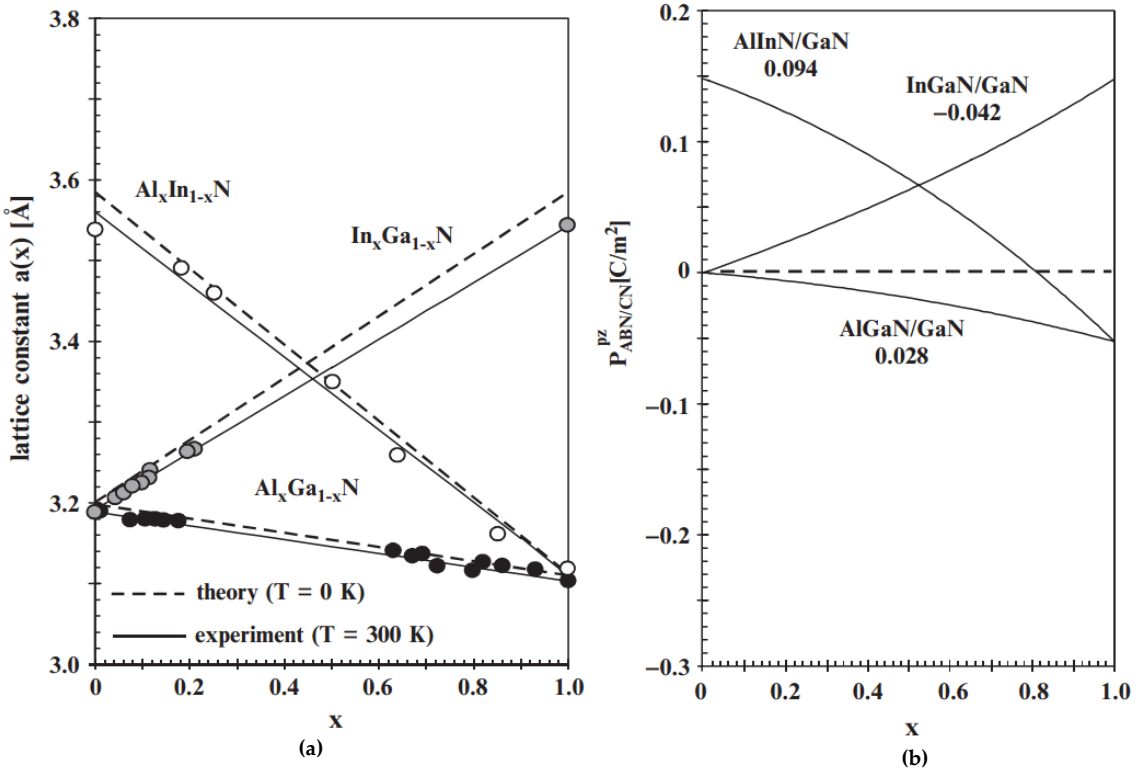


Figure 2.8 (a) Lattice constant a(x) for random ternary alloys of group-III-nitrides (b) piezoelectric polarisation of ternary alloys pseudomorphically grown on relaxed GaN buffer layers [9]

Interestingly, as can also be observed from Figs. 2.8 (a) and (b), the piezoelectric polarisation vanishes for $Al_{0.82}In_{0.18}N$/GaN; as for a mole fraction of 82% of Al in InN, the alloy and the underlying GaN layers have the same in-plane lattice constants. This aspect is sometimes utilised in quantum well structures for III-V nitrides based optoelectronic applications.

When a Ga-polarity layer is under homogeneous in-plane tensile strain, the cumulative z-component ([0001] direction) of the polarisation associated with the triple bonds of the tetrahedron decreases, causing a net piezoelectric polarisation which would be directed along the [000$\bar{1}$] direction, as shown Fig. 2.9 (a). In an N-polarity film, the same occurs except that the net polarisation would be in the opposite [0001] direction [13].

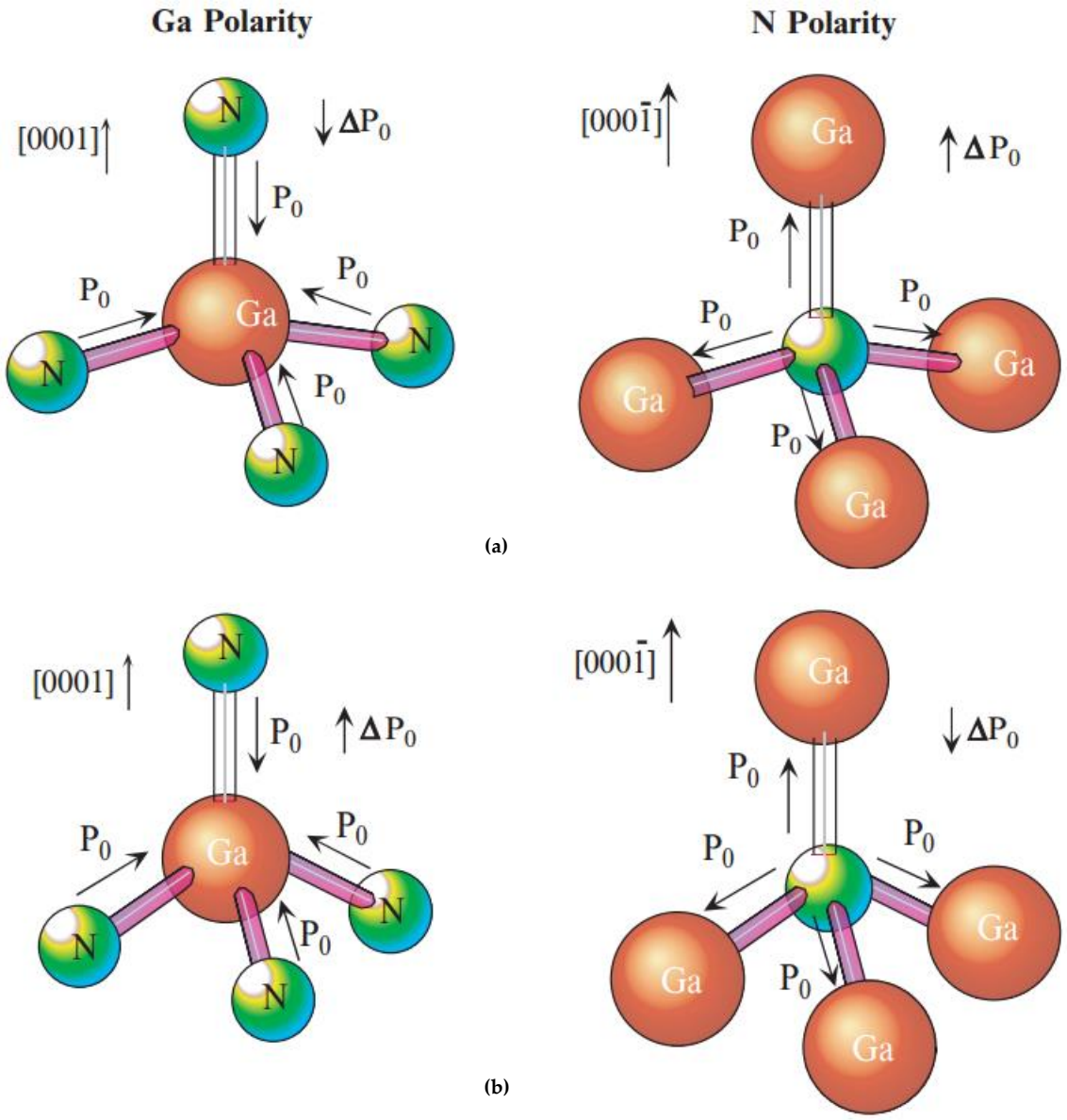


Figure 2.9 Schematics of a GaN tetrahedron for both Ga and N polarity with a homogeneous in-plane (a) tensile strain (b) compressive strain [13]

When an in-plane and homogeneous compressive strain is present, the net piezoelectric polarisation will be in the [0001] direction in the situation for Ga-polarity case and along the [000$\bar{1}$] direction in the N-polarity case, as shown in Fig. 2.9 (b) [13]. Both spontaneous and piezoelectric components of polarisation play a crucial role in determining the physics of III-V nitride heterostructure based devices.

2.2 AlGaN/GaN Heterostructures

With the availability of suitable epitaxial techniques, AlGaAs/GaAs High Electron Mobility Transistor (HEMT) was invented more than thirty years ago [14]. A conventional single heterostructure HEMT typically consists of an undoped GaAs layer, an undoped AlGaAs spacer layer, and an n-type AlGaAs layer sequentially grown on a GaAs substrate. The sheet carrier concentration of the two-dimensional electron gas (2DEG) at the single AlGaAs/GaAs interface is typically in the range of 1 x 10^{12} cm^{-2}, which is limited by the doping concentration of the n-type AlGaAs layer and the density of available electronic states at the interface [15].

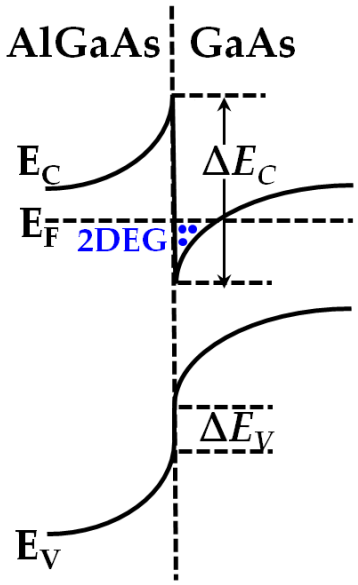


Figure 2.10 Energy band diagram of a generic AlGaAs–GaAs heterostructure

Illustrated in Fig 2.10, is the band diagram of a generic AlGaAs/GaAs heterostructure. AlGaAs has wider bandgap energy than GaAs and the band gap increases with the Al mole fraction. ΔE_C and ΔE_V refer to the conduction band offset/discontinuity and valence band offset/discontinuity respectively, due to the abrupt change in the band structure at the interface between AlGaAs and GaAs. 2DEG is formed at the interface as electrons diffuse from wider bandgap n-type doped material to the lower bandgap GaAs. A potential barrier

then confines the electrons to a thin sheet of charge, in a triangular quantum well. The spacer layer serves to provide a separation of the 2DEG from any ionised donors at the interface, reduces Coulomb scattering and results in charge carriers with extremely high mobility. The drawback of the spacer layer, however, is that the sheet carrier concentration in the channel diminishes as the spacer layer thickness is increased. This high density and high mobility 2DEG region is used as the transistor channel, and was a key factor in the development and wide adoption of this device architecture/technology.

With the advancements made in the area of crystal growth of III-V nitrides, the development of AlGaN/GaN heterostructures was a step in the natural course of evolution of III-V compound semiconductor based transistors, and an emulation of device architectures that had been previously developed with AlGaAs/GaAs structures. However, there are fundamental differences in the governing physics of the material for device operation, which will be described in the subsequent sections.

2.2.1 2DEG in AlGaN/GaN heterostructures

The presence of 2DEG in AlGaN/GaN heterostructures was first confirmed in 1992 by M. Asif Khan et al. [16]. 2DEG density was reported to be 2.6 x 10^{12} cm^{-2} at 7K, and had been achieved without any intentional doping in the $Al_{0.13}Ga_{0.87}N$/GaN heterostructure. The 2DEG mobility was measured to be 834 $cm^2/V.s$ at room temperature, which was higher than values observed in the bulk. As the temperature was reduced, the mobility monotonically increased and saturated at a value greater than 2500 $cm^2/V.s$ at 77 K, with no further change observed with respect to temperature up to 4.2 K.

Ever since, AlGaN/GaN heterostructures and Heterostructure Field Effect transistors (HFETs)/HEMTs have been subjects of intense investigation as they became attractive candidates for high voltage and high-power operation

initially sought-after for microwave applications and subsequently for power switching applications.

It was introduced in section 2.1 that GaN and AlN which crystallise in wurtzite crystal structure possess spontaneous polarisation inherently and piezoelectric polarisation in the presence of strain. Formation of 2DEG in AlGaN/GaN heterostructures is primarily determined by these properties in the material system.

The lattice constant of AlGaN and there by mismatch between AlGaN and GaN layers in a pseudomorphically grown heterostructure depends on the mole fraction of Al in AlGaN. Lattice mismatch determines the strain and there by the magnitude of piezoelectric polarisation. The magnitudes of overall polarisation in the two layers of the heterostructure are different. There is an abrupt change in polarisation from one material to the other at the interface. Associated with a gradient of polarisation in space is a polarisation induced charge density (σ) given by $\sigma = \Delta P$. Therefore, at an abrupt interface of a (top/bottom layer (AlGaN/GaN or GaN/AlGaN)) heterostructure, the polarisation sheet charge density can be expressed by [17]

$$\sigma = P \text{ (top layer)} - P \text{ (bottom layer)} \qquad (2.17)$$

$$= \{P_{SP} \text{ (top layer)} + P_{PE} \text{ (top layer)}\}$$

$$- \{P_{SP} \text{ (bottom layer)} + P_{PE} \text{ (bottom layer)}\}$$

where P_{SP} and P_{PE} refer to the magnitude of spontaneous and piezoelectric polarisation respectively.

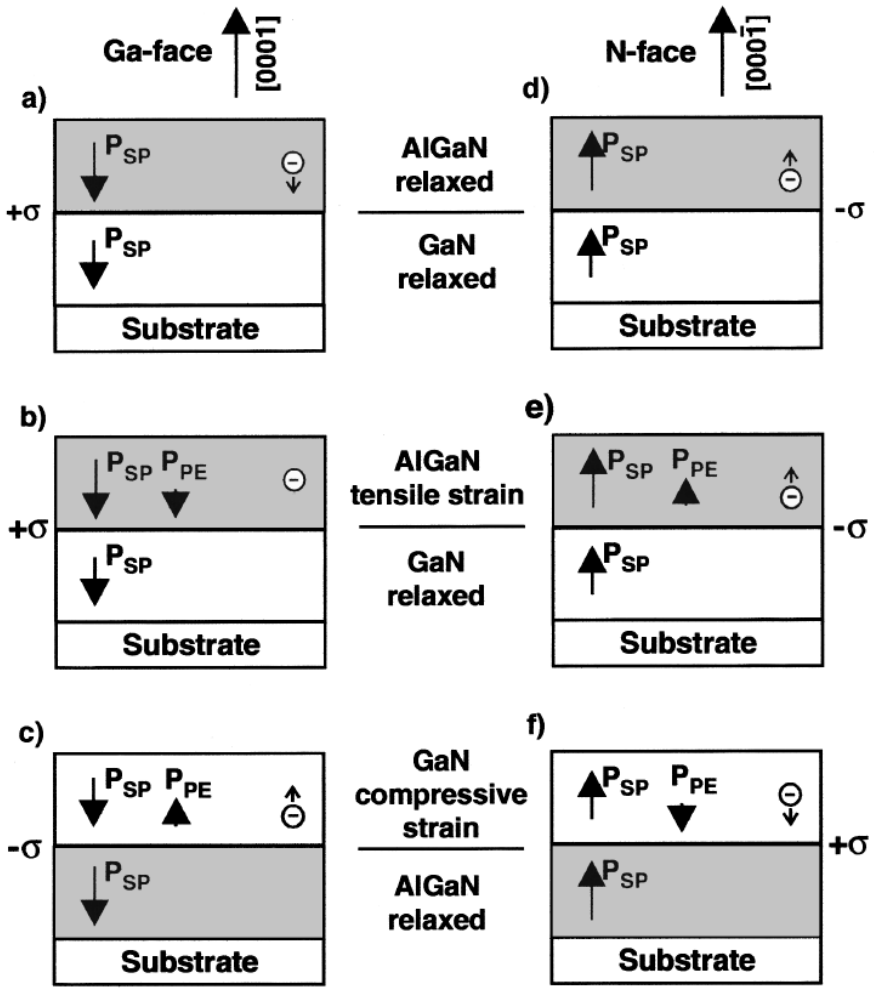


Figure 2.11 Polarisation induced sheet charge density and directions of the spontaneous and piezoelectric polarisation [17]

If the polarisation induced sheet charge density is positive (+σ), free electrons can accumulate to compensate the polarisation induced charge, forming a 2DEG at the interface. Similarly, a negative sheet charge density (-σ) can create a two-dimensional hole gas (2DHG) at the interface and maintain charge neutrality. This has been illustrated in Fig. 2.11, where schematics of AlGaN/GaN heterostructures under various scenarios have been considered. Taking the example of b) in Fig. 2.11, the magnitude of polarisation induced sheet charge density could be calculated as

$$\sigma = \{P_{SP}\,(\text{AlGaN}) + P_{PE}\,(\text{AlGaN})\} - \{P_{SP}\,(\text{GaN})\} \qquad (2.18)$$

The maximum sheet carrier concentration (n_s) at the AlGaN/GaN interface of an undoped heterostructure can be expressed by [18]

$$n_s(x) = \frac{+\sigma(x)}{e} - \left(\frac{\varepsilon_0 \varepsilon(x)}{de^2}\right)[e\Phi_b(x) + E_F(x) - \Delta E_C(x)] \qquad (2.19)$$

where x is the Al mole fraction, e is the electronic charge, d is the width of the AlGaN barrier, $e\Phi_b$ is the Schottky barrier of the Gate contact, E_F is the Fermi level, and ΔE_C is the conduction band offset/discontinuity at the AlGaN/GaN interface.

Smorchkova et al. [19] reported that 2DEG formation in the $Al_{0.27}Ga_{0.73}N$/GaN structure occurs starting at a barrier thickness of ~ 3 nm, and attributed the same to the position of the energy level of surface donor-like states.

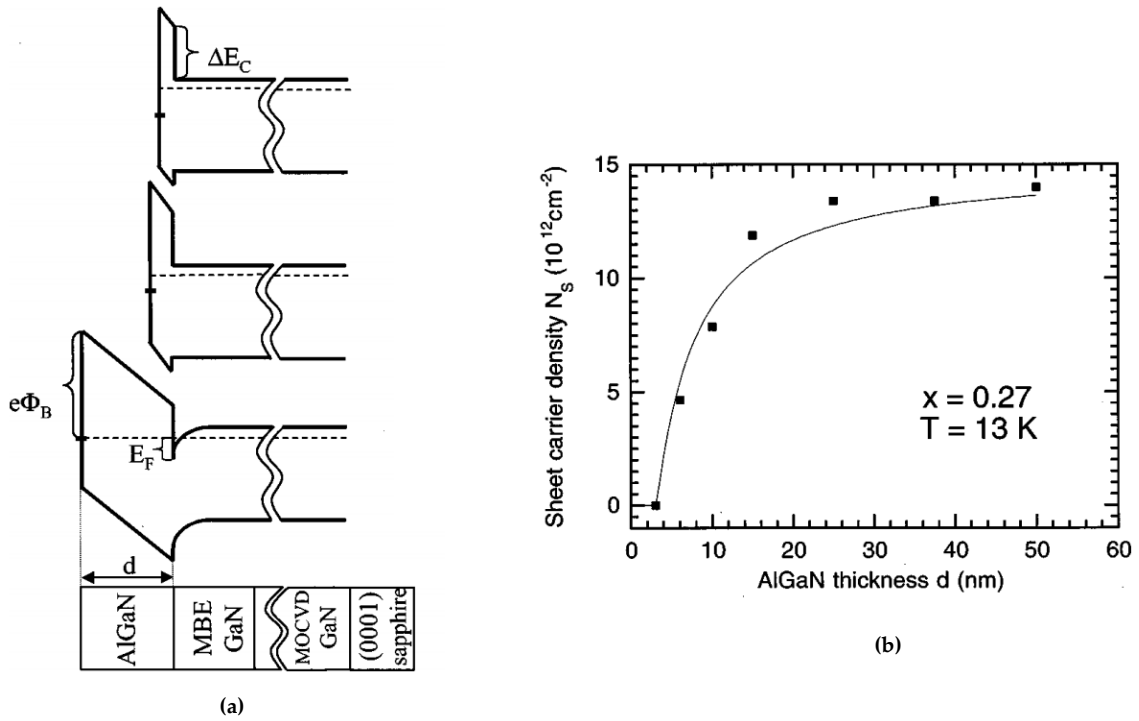


Figure 2.12 (a) Schematic diagram showing development of the band structure in AlGaN/GaN samples with increasing AlGaN barrier width (b) 2DEG sheet carrier density in the $Al_{0.27}Ga_{0.73}N$/GaN structures as a function of AlGaN barrier thickness [19]

As shown in Fig. 2.12 (a), they hypothesized that as the width of the AlGaN layer increased, the Fermi level (E_F) at the surface approaches the deep donor level, and as soon as E_F and the surface states are aligned, 2DEG formation is

initiated at the AlGaN/GaN interface. Further increase of the barrier width leads to an increase in the density of 2DEG and its subsequent saturation at a value close to the value of the polarisation charge density. They also reported that increase of the Al mole fraction (x) in AlGaN results in an approximately linear change in the 2DEG density at a rate of $^{dNs}/_{dx}$ = 5.45 x 10^{13} cm^{-2} (0.09 < x < 0.31). The low temperature electron mobility of the AlGaN/GaN heterostructures was observed to gradually decrease with an increase in both Al mole fraction as well as thickness of the AlGaN layer and was attributed to possible change in the alloy disorder scattering or interface roughness scattering that significantly intensify as the 2DEG density increases.

Heikman et al. [20] also supported the surface donor model and reported the effect of GaN cap layer thickness on sheet carrier density and mobility.

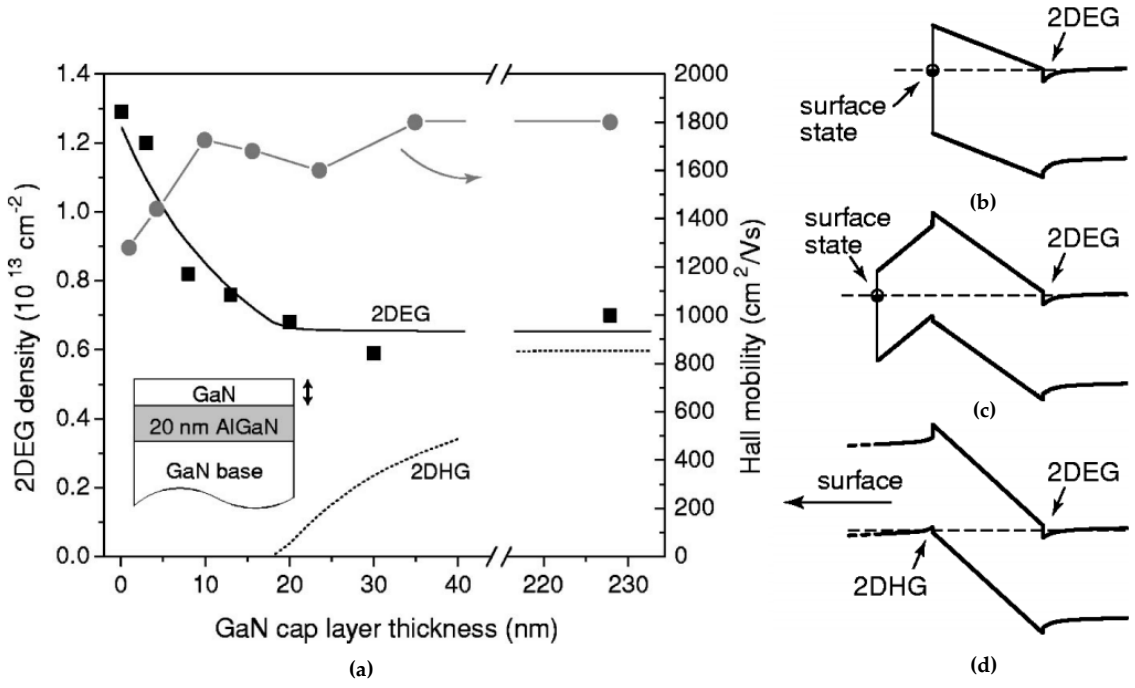


Figure 2.13 (a) The effect of GaN cap layer thickness on 2DEG density and mobility, for a GaN/AlGaN/GaN double heterostructure; Band diagram of (b) single AlGaN/GaN heterostructure, (c) GaN/AlGaN/GaN double heterostructure with a thin GaN cap, and (d) GaN/AlGaN/GaN double heterostructure with a thick GaN cap [20]

The presence of the GaN cap layer results in a reduction of the 2DEG density, from 1.3 x 10^{13} cm^{-2} with no GaN cap, down to 0.6 x 10^{13} cm^{-2} with a 30 nm cap

layer (Fig. 2.13 a). Their simulations also indicated the presence of a 2DHG at the upper interface of GaN/AlGaN/GaN structures with sufficiently thick GaN cap layers (Fig. 2.13 d).

It can be clearly inferred that the 2DEG density in an AlGaN/GaN heterostructure has a strong dependence on thickness as well as Al mole fraction in the AlGaN layer. Although, the 2DEG density increases proportionally with the AlGaN layer thickness, there is a certain thickness beyond which the tensile strained AlGaN layer tends to relax by cracking. This phenomenon lowers the piezoelectric component of polarisation and could substantially diminish the 2DEG density. The thickness at which strain relaxation occurs in the AlGaN layer also depends on the Al mole fraction and the two are inversely related [21].

2.3 AlGaN/GaN based HEMTs

Although very similar to AlGaAs/GaAs HEMTs in terms of basic device architecture, as discussed in the previous sections, the physics determining the operation of AlGaN/GaN HEMTs is fundamentally different. The spontaneous formation of high density and high mobility 2DEG at the interface of an un-intentionally doped and epitaxially grown AlGaN layer on a GaN layer is a unique characteristic of AlGaN/GaN HEMTs. Sheet carriers (2DEG) induced by polarisation in the material have minimal temperature dependence [22], and as employed in AlGaAs/GaAs HEMTs form the transistor channel.

Fig. 2.14 shows the schematic diagram of a conventional AlGaN/GaN HEMT and conduction band profile of a typical AlGaN/GaN heterostructure has been shown in Fig. 2.15. The schematic is that of device architecture on a non-native substrate like Si, SiC or Sapphire. GaN or AlN is used as nucleation layer for high quality heteroepitaxial crystal growth of GaN on non-native substrates.

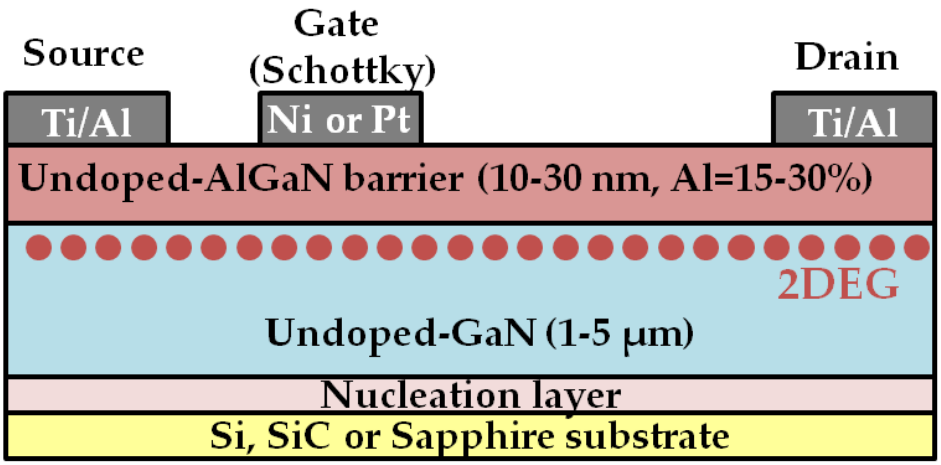


Figure 2.14 Schematic diagram of a conventional AlGaN/GaN HEMT

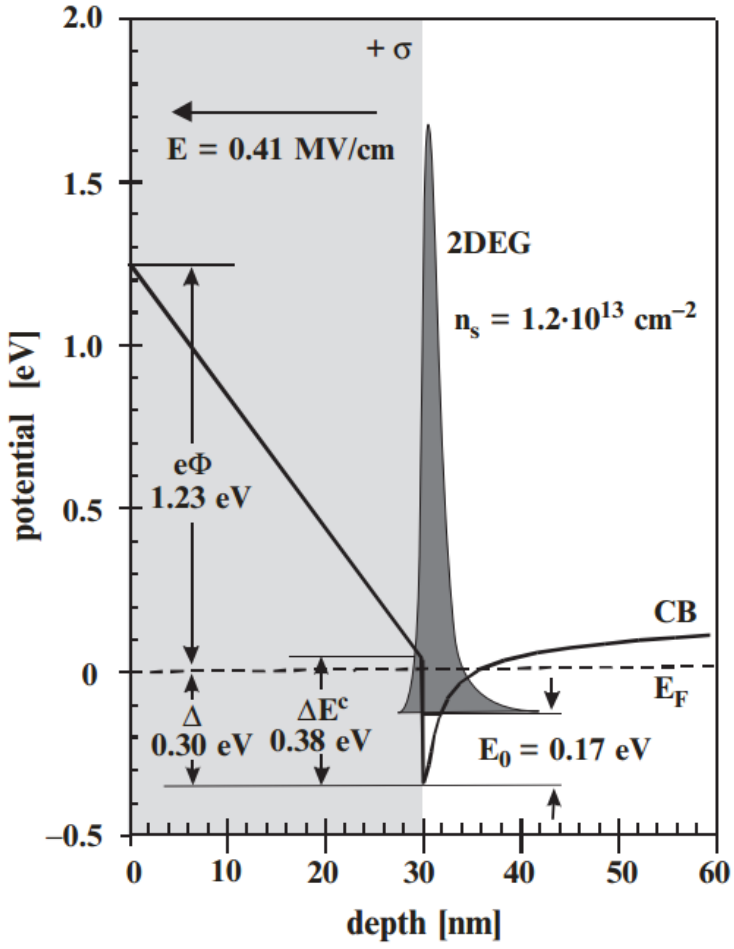


Figure 2.15 Simulated conduction band profile versus depth of an undoped $Al_{0.3}Ga_{0.7}N$/GaN heterostructure [9]

Hydride Vapor Phase Epitaxy (HVPE), Metal Organic Chemical Vapor Deposition (MOCVD) and Molecular Beam Epitaxy (MBE) are some of the

commonly employed techniques for GaN and AlGaN epitaxial growth. In a conventional AlGaN/GaN HEMT, Gate electrode is a Schottky type contact, whereas Drain and Source electrodes form ohmic contacts to 2DEG. The commonly used metals for each of the electrodes have also been included in the schematic. As the 2DEG channel is spontaneously induced during epitaxial growth of the layers, such a scheme by default ensures a conduction path from Drain to Source without applying any Gate bias voltage and makes the device normally-on/depletion-mode (Fig. 2.16 (a)). The conduction path under the Gate can be disrupted or cut-off by applying a negative voltage and thus depleting the 2DEG under the gate region (Fig. 2.16 (b)).

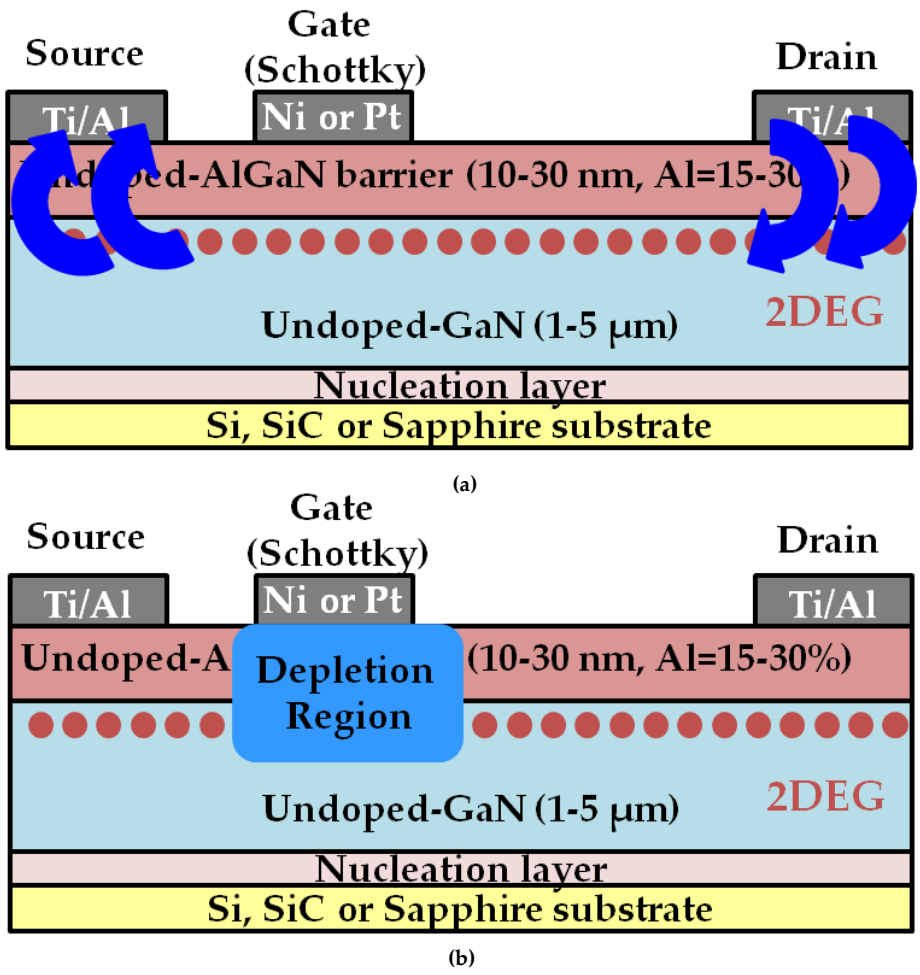


Figure 2.16 Schematic diagrams of a conventional AlGaN/GaN HEMT (a) On-state (b) Off-state

2.3.1 Characteristics of GaN Power Electronic Transistors

The three main characteristics of an ideal power electronic device are as following:

- Ability to conduct arbitrarily large currents with minimal voltage drop in the on-state
- Ability to operate at arbitrarily large forward and reverse voltages with minimal leakage current in the off-state
- Ability to switch from on-to-off or vice versa instantaneously when triggered, and therefore minimise losses during the transition

A real device is custom-designed for optimal performance and to the requirements of a given application. Device design is an elaborate exercise which requires extensive numerical simulations using appropriate models, and also needs to adhere to the design rules of microelectronic fabrication. The approach and most of the required analytical models for developing AlGaN/GaN power electronic transistors have their origins in models developed for AlGaAs/GaAs HEMTs as well as lateral power devices in Silicon (Si). They are modified accordingly primarily taking the intrinsic polarisation properties of III-V nitrides into consideration. The most important electrical characteristics and their governing physical parameters, that are crucial from the perspective of employing these devices for power switching applications, are presented and briefly discussed in the following sub-sections.

2.3.1.1 Threshold voltage (V_{TH})

Threshold voltage (V_{TH}) is the minimum voltage that has to be applied to the Gate of a transistor to turn it on and enable conduction between Drain and Source terminals. As mentioned previously, AlGaN/GaN HEMTs are depletion-mode devices by default and have a negative value for V_{TH}. V_{TH} can be expressed as [13]

$$V_{TH} = \Phi_b - \frac{\Delta E_C}{e} - V_p - \frac{ed}{\varepsilon}(\sigma + N_B W_d) \qquad (2.20)$$

where Φ_b represents the Schottky barrier height of the Gate metal deposited on the AlGaN barrier layer, ΔE_c is the conduction band discontinuity, $V_p = qN_d(d_d)^2/2\varepsilon$, N_d is the donor concentration in the barrier layer, d_d is the thickness of the doped region of the barrier layer, σ represents the interfacial polarisation charge density, N_B is the bulk doping density and W_d is the depletion layer thickness in the channel region. The magnitude of V_{TH} is directly proportional to the 2DEG density and can hence be controlled by altering the barrier width or Al mole fraction.

2.3.1.2 Drain-Source Current (I_{DS}) and On-state Resistance (RDS_{ON})

As in a typical field effect transistor, the output characteristics (relationship between Drain-Source Current (I_{DS}) and Drain Voltage (V_{DS}) for various values of Gate Voltage (V_{GS})) of AlGaN/GaN HEMTs have two main regions: namely the linear and saturation regions. I_{DS} can be modelled with two simple assumptions. The first one being that the carrier velocity is directly proportional to the applied electric field (constant mobility) and the second assumption is that beyond a certain electric field, the carrier velocity saturates. The assumptions are reasonable as there is a well-defined mobility-field relationship for any given material which follows this behaviour.

Electric current is defined as the rate of change of charge (Q) and can be expressed as

$$I = \frac{dQ}{dt} \qquad (2.21)$$

In an AlGaN/GaN transistor,

$$I_{DS} = \frac{dQ_{2DEG}}{dt}$$

In the linear region, Drain-Source current (I_{DS}) could be expressed as

$$I_{DS} = W \cdot n_{2DEG}(x) \cdot e \cdot v(x) \quad (2.22)$$

where W is the device width, e is the electronic charge, n_{2DEG} is the interfacial carrier density, v is the velocity and channel length is along the x direction

$$I_{DS} = W \cdot n_{2DEG}(x) \cdot e \cdot \mu \cdot E(x) \quad (2.23)$$

where μ is electron mobility, E is the electric field in the channel and $v = \mu \cdot E$ in the linear region. Equation 2.23 can be expressed as

$$I_{DS} = W \cdot \frac{\varepsilon}{ed} \cdot (V_{GS} - V_{TH} - V(x)) \cdot e \cdot \mu \frac{dV(x)}{dx}$$

Where ε is the permittivity of AlGaN, V_{TH} is the Threshold Voltage, V_{GS} is the Gate-Source Voltage and $V(x)$ represents the potential at any location along the channel due to an applied Drain-Source Voltage

$$I_{DS} = W \cdot \frac{\varepsilon}{d} \cdot (V_{GS} - V_{TH} - V(x)) \cdot \mu \frac{dV(x)}{dx}$$

$$I_{DS} \cdot dx = W \cdot \frac{\varepsilon}{d} \cdot \mu \cdot (V_{GS} - V_{TH} - V(x)) \cdot dV(x)$$

Integrating the above expression across the channel length L and a Drain-Source Voltage of V_{DS}

$$\int_0^L I_{DS} \cdot dx = \int_0^{V_{DS}} W \cdot \frac{\varepsilon}{d} \cdot \mu \cdot (V_{GS} - V_{TH} - V(x)) \cdot dV(x)$$

$$I_{DS} = \frac{W}{L} \cdot \frac{\varepsilon}{d} \cdot \mu \cdot [(V_{GS} - V_{TH}) V_{DS} - \frac{V_{DS}^2}{2}] \quad (2.24)$$

The on-state resistance could be estimated by differentiating I_{DS} with respect to V_{DS} in this regime (as for $V_{DS} << V_{GS} - V_{TH}$, the second term can be neglected). Therefore, the On-state Resistance (RDS_{ON}) can be expressed as

$$RDS_{ON} = [\frac{W}{L} \cdot \frac{\varepsilon}{d} \cdot \mu \cdot (V_{GS} - V_{TH})]^{-1} \quad (2.25)$$

The current reaches saturation when the drain voltage is increased to the point where the field in the channel causes the velocity of carriers to saturate (v_{sat}), and could be simply expressed as

$$I_{DS} = W \cdot n_{2DEG} \cdot e \cdot v_{sat} \quad (2.26)$$

2.3.1.3 Transconductance (g_m)

Transconductance (g_m) is an important parameter in HEMTs and is defined as rate of change of drain current with respect to incremental change in gate voltage

$$g_m = \left\{\frac{\partial I_{DS}}{\partial V_{GS}}\right\}, \text{ at } V_{DS} \geq V_{DSAT} \quad (2.27)$$

Although this parameter is extremely crucial for RF power amplifiers, a large transconductance is also desirable in power electronic transistors to obtain a high drain current with a small gate bias voltage. In addition, the switching speed of the power electronic transistor improves with increasing transconductance [23]. Transconductance is defined in the saturation regime/active region of the transistor operation and can also be obtained by differentiating I_{DS} given by equation 2.24, with respect to V_{GS} at

$V_{DS} = V_{DSAT} = V_{GS} - V_{TH}$.

2.3.1.4 Avalanche Capability and Drain-to-Source Breakdown Voltage (BV_{DSS})

Avalanche capability is one of the most desired characteristics in a power switching device. In a typical power switching application and especially in converter applications with inductive loads (for e.g. motor drive), transients can momentarily exceed the rated off-state Drain-to-Source Breakdown Voltage (BV_{DSS}) of the transistor. With adequate thermal management, the transistor should withstand this temporary high voltage stress, during which a non-destructive avalanche breakdown through impact ionisation is initiated in the region of the device supporting the high voltage. Avalanche capability is a

proven characteristic of Si power devices. However, this is yet to be achieved in AlGaN/GaN lateral devices, and the devices are irreversibly damaged on application of voltage beyond the rated BV_{DSS} value. This is one of the main reasons why commercially available devices are over-designed and under-rated, to accommodate transient overshoots in voltage to some extent. The downside is that such devices can never offer the performance benefits of GaN that can be theoretically achieved.

AlGaN/GaN HEMTs are planar devices and surfaces play a major role in determining the actual breakdown voltage. Moreover, BV_{DSS} is sometimes hard to establish in these devices as the measurement gets influenced by high Drain-Gate leakage currents. Therefore, in practice, it is defined as the voltage at which gate leakage reaches 1 mA/mm, but the approach is yet to be considered a standard.

To obtain a clear understanding of breakdown characteristics, it is also important to know the impact ionisation (II) coefficients of the material, as these values vary depending upon starting substrates used for heteroepitaxial growth of GaN layers. II is also dependent on crystal orientation/presence of defects. Moreover, there is not sufficient information on the II coefficients for GaN and there are conflicting reports on temperature-dependence of these parameters [24-28]. Additional uncertainty is sometimes introduced with the dielectric breakdown of surface passivation as such layers are typically CVD based and could break down (destructive) within a range of 3-5 MV/cm depending on the quality of the process/layers, making it difficult to differentiate between insulation and semiconductor breakdown.

Electric field management is a key issue to be addressed for lateral AlGaN/GaN HEMTs, in order to push the breakdown voltage to theoretically possible values. Fig. 2.17 shows simplified cross-section of a conventional HFET with a

Schottky gate contact. The electric field under off-state is concentrated at the Drain-side edge of the Gate electrode as illustrated in Fig 2.17 (b) due to positive polarisation charges at the AlGaN/GaN hetero-interface and charge accumulation at the Gate edge [29].

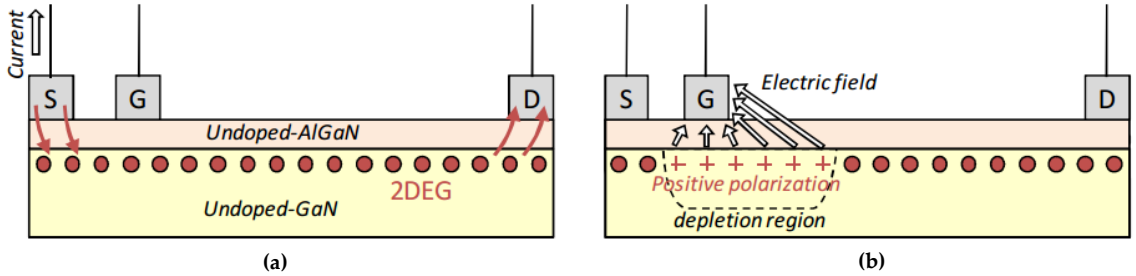


Figure 2.17 Schematic of a conventional HFET in (a) On-state and (b) Off-state [29]

RESURF

In order to support high voltage in lateral devices, effective electric field management solutions need to be employed. Appels and Vaes invented the REDuced SURFace field (RESURF) concept which enabled high voltage lateral power devices in Si and has been illustrated in Fig. 2.18 [30].

The conclusion of this work was that optimum performance of such a device depends on the net charge of the N^- epi layer, and device geometry should be such that the vertical depletion at the P^- N^- junction must reach the surface before the surface electric field reaches the critical electric field for breakdown. Under reverse bias, the vertical depletion region in the N^- epi region simultaneously extends and interacts with the lateral depletion region of the P^+ N^- junction. The result is that the lateral depletion region effectively extends into a larger distance and the technique enabled lateral high voltage devices that were no longer limited by surface breakdown.

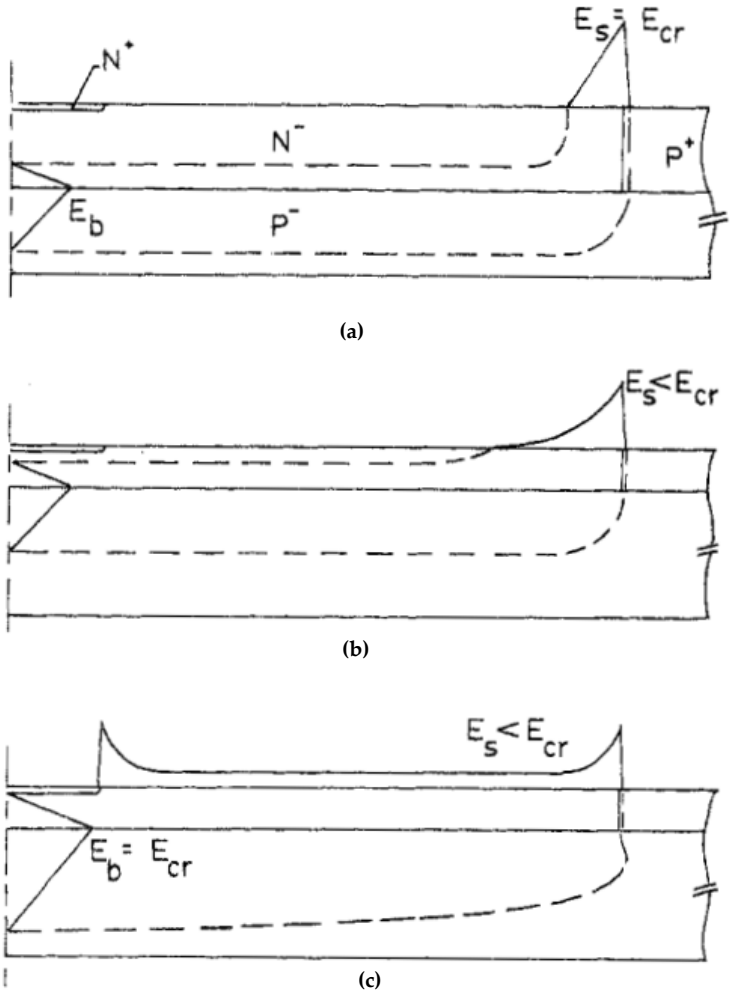


Figure 2.18 Illustration of electric field distribution in a lateral diode (a) thick epitaxial layer (BV = 370V) (b) thin epitaxial layer (BV = 370V) (c) thin epitaxial layer employing RESURF (BV=1150V) [30]

A key finding from this work was also that, symmetrical electric field in the structure is obtained when $N^{-}_{epi} \cdot t_{epi} = 10^{12}$ cm^{-2} (where t_{epi} is the layer thickness), making charge control an essential requirement for designing high voltage devices. This became an instrumental technique for monolithic integration and development of high voltage ICs. The principle was later extended to Double RESURF and Multiple/3D- RESURF commonly also referred to as Superjunction [31-35].

Superjunction

Superjunction devices incorporate a number of alternately stacked p- and n-type heavily doped thin layers.

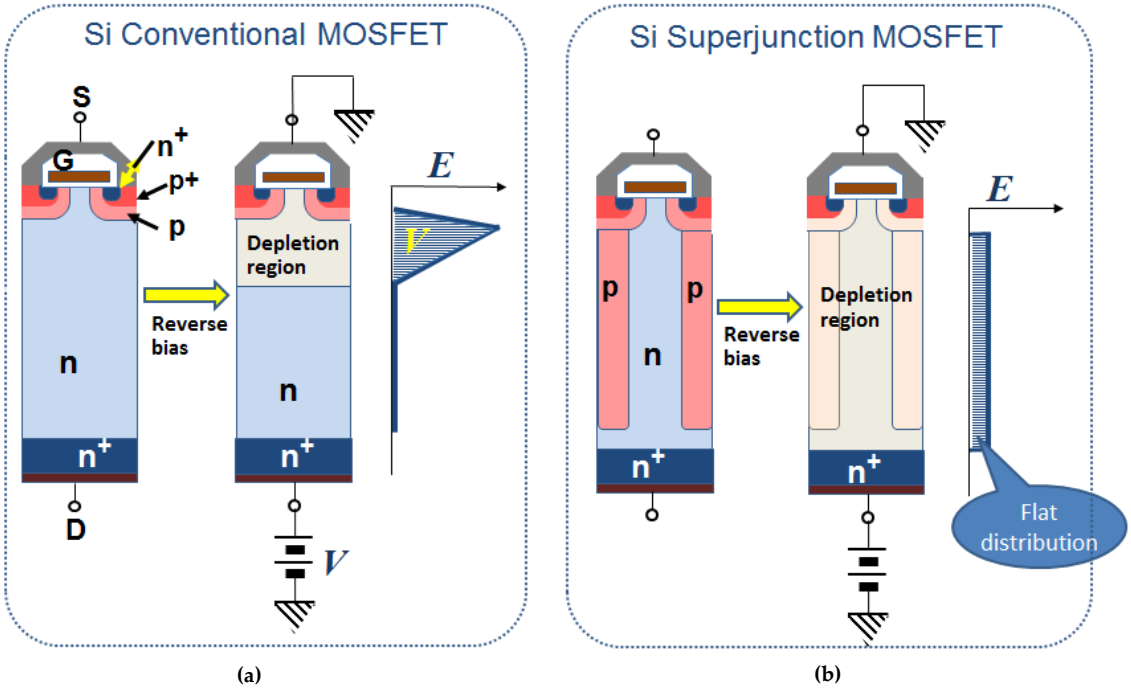


Figure 2.19 Cross-sectional schematics and field profile under reverse bias of vertical (a) Si Conventional power MOSFET (b) Si Superjunction power MOSFET

As shown in Fig. 2.19 (a), under off-state and a high Drain bias, the depletion region in the n- epi layer in a conventional power MOSFET extends primarily vertically. When the electric field at the p n- junction reaches the critical electric field of Si, the MOSFET breaks down. The breakdown voltage is determined by the thickness and doping concentration of the n- epi layer. Therefore breakdown voltage values for a given drift length can only be increased by reducing the doping concentration in the n- region which leads to an increase in RDS_{ON}, significantly compromising the efficiency of such a device.

As shown in Fig. 2.19 (b), in a Superjunction power MOSFET under off-state, and under high Drain bias, the depletion region in the device extends laterally

as well as vertically in the entire drift region, as observed in conventional RESURF structures.

Theoretically, a flat field distribution of the electric field can be achieved in a Superjunction power MOSFET compared to a triangular field profile that is obtained in a conventional power MOSFET. The flat field distribution is achieved due to carefully controlled doping and charge balance in the alternately stacked p- and n- pillars, which enables full depletion of the drift region, under low reverse bias. This approach has enabled power electronic devices which have taken the performance beyond the Si material limit offering up to an order of magnitude improvement in specific on-state resistance, and has been widely adopted by the market for applications requiring operating voltage values in the range of 600 V and above.

Field Plate

Although RESURF/Superjunction has been a proven technology in Si for high voltage vertical and lateral devices, the traditional approach of enabling lateral high voltage GaN devices has been using Field Plate (FP) technologies. This is possibly because much of the initial research on AlGaN/GaN HFETs in the early 2000s was strongly influenced by prior research activities in the development of AlGaAs/GaAs HFETs and GaAs MESFETs used for RF applications. So, the approaches used there for increasing breakdown voltage were naturally adopted in the initial phase [36, 37]. Secondly, doping control has been problematic in GaN, especially p-type doping due to high activation energy of Mg that is typically used as a p-type dopant.

FP technologies with optimised design can significantly increase operating voltage of GaN HFETs by engineering the electric field profile and suppressing the electric field crowding at the Gate edge as illustrated in Fig. 2.20 [38, 39].

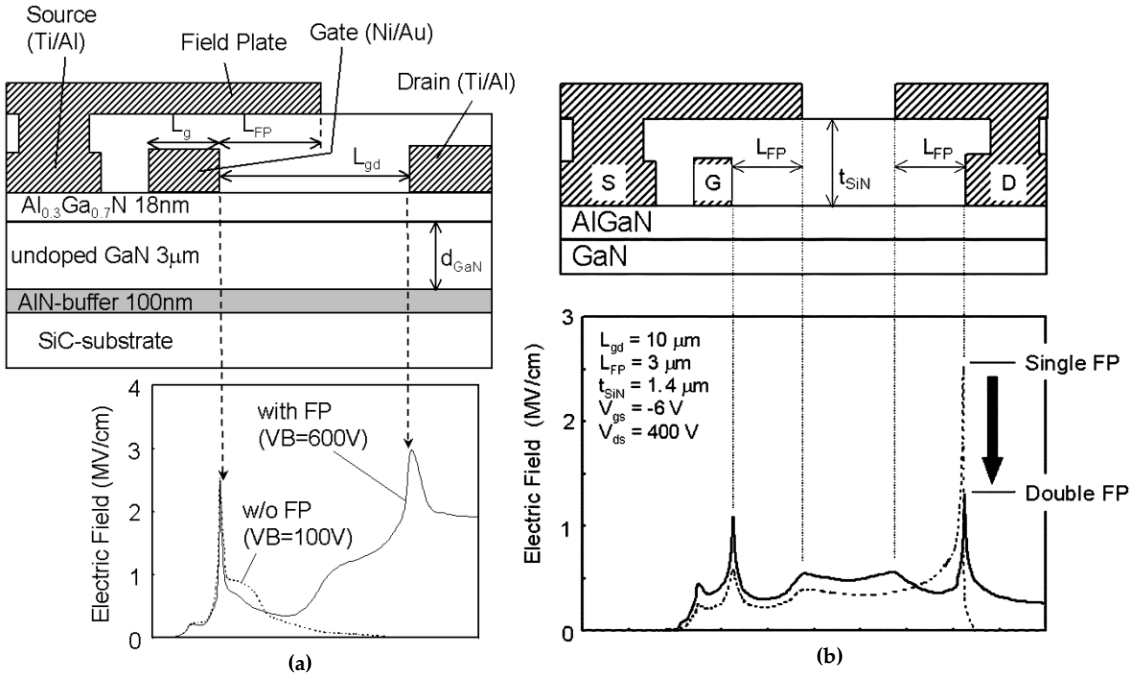


Figure 2.20 Cross-sectional structure of AlGaN/GaN HEMT and field profile with (a) source field plate structure (b) source and drain field plate [38,39]

However, it can be clearly noticed that although the presence of field plates significantly enhances the blocking voltage capability, the electric field distribution is not ideal, as can be achieved using perfect charge balance within the structure. Polarisation Super Junction (PSJ) that will be discussed in detail in the next chapter and the focus of this research work is a promising technology that has the potential of achieving that target.

2.3.1.5 Off-State Leakage Currents (I_{DSS})

The bandgap of GaN is higher than that of GaAs, and so, the barrier height of the Schottky gate of AlGaN/GaN HEMTs is higher than that of AlGaAs/GaAs HEMTs. However, the reverse Drain-Gate Schottky leakage, which is the dominant component of I_{DSS} in AlGaN/GaN HEMTs has been observed to be much higher than that in AlGaAs/GaAs HEMTs and has been mostly attributed to thermionic trap-assisted tunnelling [40]. The sources of high leakage currents have also been pointed out to be high density of surface and interface states caused by crystal imperfections/dislocations, mechanical stress of surface

passivation/dielectrics, and device-processing related plasma induced damage [41,42].

For GaN-on-Si HEMTs, it has been also been reported that the reverse drain leakage currents is due to the injection of electrons into the GaN buffer layer attributed to the poor isolation of the GaN buffer and Si substrate, along with the tunnelling leakage current of the Schottky-gate [43]. Lu et al. [44] have suggested hole generation in the buffer and electron injection from the Si substrate into the buffer contributing to the leakage current, which could also eventually cause the reverse bias breakdown due to impact ionisation.

2.3.1.6 Negative resistance

An anomaly observed in the output characteristics of AlGaN/GaN HEMTs is shown in Fig. 2.21. The devices exhibit negative resistance for high currents and voltages, and the phenomenon has been attributed to self-heating of the device.

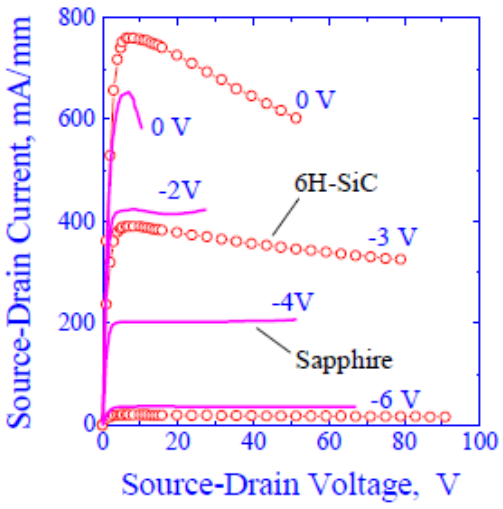


Figure 2.21 I-V characteristics for devices grown on Sapphire (dots) and 6H-SiC (open circles) [45]

The consequence of self-heating is reduction of mobility with rise in temperature, and causes the downward sloping current curves [45]. The device temperature increases at high I_{DS} and high V_{DS} due to increased power dissipation. This effect can be minimised by using substrates with higher

thermal conductivity and by implementing proper thermal management techniques.

2.3.1.7 Current collapse, trapping and passivation effects

Another extremely serious anomaly observed in AlGaN/GaN HEMTs, is current collapse and increase in the on-state resistance (RDS_{ON}/R_{ON}) during switching at high frequencies and under high off-state electric fields. As a result, the current carrying capability of the device reduces during switching and has been illustrated in Fig. 2.22.

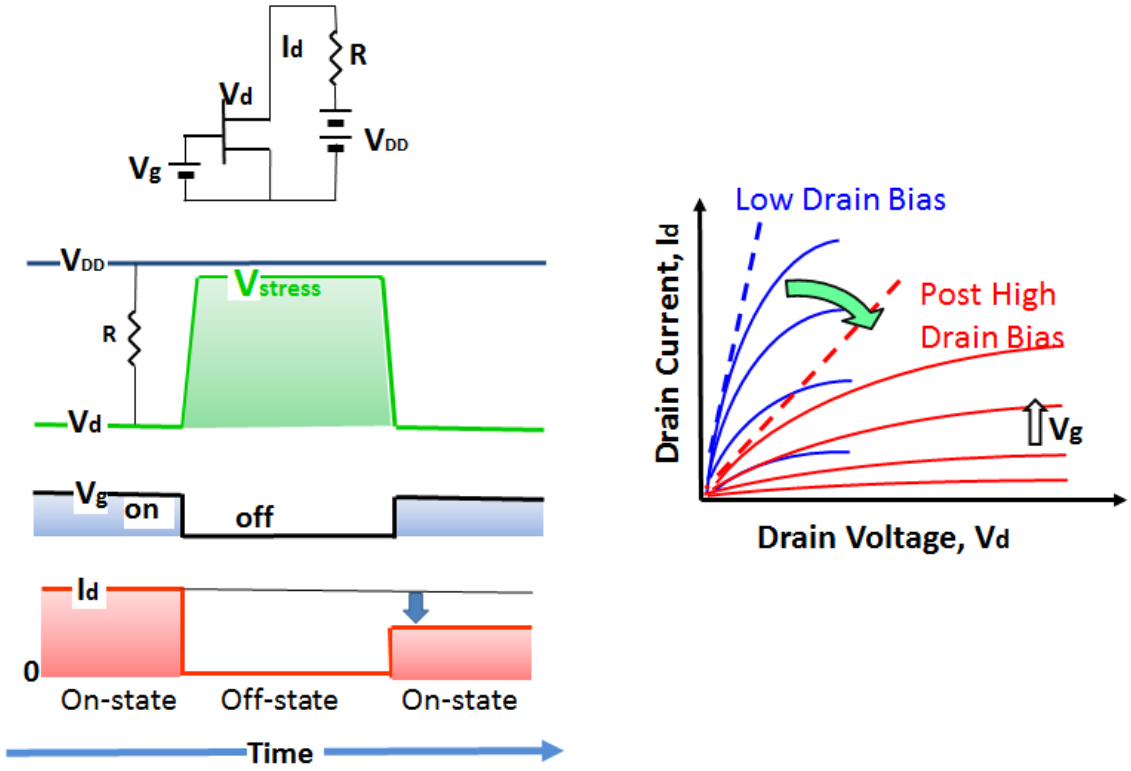


Figure 2.22 An illustration of current collapse following a high off-state electric field stress

Current collapse has been largely attributed to electrons in the channel getting trapped in buffer/barrier layers, and unpassivated surface states which could reduce the conducting charge, particularly between the gate and the drain region of the transistors as illustrated in Fig. 2.23 [13].

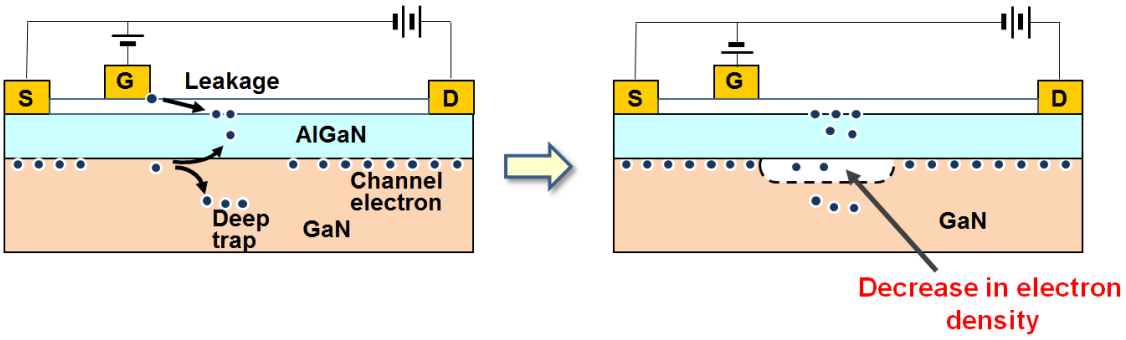


Figure 2.23 Schematic representation of charge trapping mechanism causing current collapse

Depending on the time constants for de-trapping from the trap states, the drain current could remain affected and not respond to the gate signal at high switching frequencies. Increase in R_{ON} is typically recoverable with sufficient time given for de-trapping of electrons. It has also been observed that passivation of the surface by depositing SiO_2/SiN could partially address this anomalous behaviour [46]. Current collapse may also be suppressed by low dislocation density GaN epitaxial layer growth. It has also been observed that the magnitude of current collapse in AlGaN/GaN HEMTs grown on SiC substrates, is less severe compared to the HEMTs grown on sapphire substrates and has been attributed to the existence of relatively smaller density of deep traps associated with the material defects/dislocations in GaN on SiC platform [47]. Engineering of defects in the buffer has also shown to mitigate the impact [48]. Field plate action also reduces current collapse by engineering the field profile, but, cannot fully overcome it, leading to devices being over-designed and derated [49].

GaN-based devices have shown remarkable high-power and high-frequency performance, yet achieving the reliability and stability along with high performance remains an open problem that has impeded the wider commercial adoption of these devices.

2.4 Summary

In this chapter, the intrinsic material properties such as spontaneous and piezoelectric polarisation and their origins associated with non-ideality and strain in the GaN crystal structure were introduced and discussed in detail. Polarisation engineering and spontaneous formation of a high density and highly mobile 2DEG at the AlGaN/GaN interface of the heterostructure are the key attributes that led to the development of AlGaN/GaN High Electron Mobility Transistor (HEMT) Technology. Details of device operation were presented following which the most important electrical characteristics and their governing physical parameters, that are crucial from the perspective of power switching applications, were also discussed. This included brief review of concepts such as RESURF/Superjunction in Silicon and comments on Field Plate engineering which is the most widely adopted technique for developing high voltage devices in GaN. It was identified that there is substantial room for improving the electric field management in devices to bridge the gap between theoretically achievable performance and the status quo. Anomalies in device performance such as current collapse, negative resistance, were also briefly reviewed.

2.5 References

[1] H. Morkoc, *Nitride Semiconductors and Devices*. Berlin: Springer, 1999.

[2] Y. Taniyasu, and M. Kasu. 2010. Improved Emission Efficiency of 210-nm Deep-ultraviolet Aluminum Nitride Light-emitting Diode [Online]. Available: https://www.ntt-review.jp/archive/ntttechnical.php?contents =ntr 201008 sf2.html.

[3] O. Ambacher, J. Majewski, C. Miskys, A. Link, M. Hermann, M. Eickhoff, M. Stutzmann, F. Bernardini, V. Fiorentini, V. Tilak, B. Schaff, and L. F. Eastman, "Pyroelectric properties of Al(In)GaN–GaN hetero-and

quantum well structures," *Journal of Physics: Condensed Matter*, vol. 14, pp. 3399–3434, 2002.

[4] D. Jena, S. P. Alpay, and J. V. Mantese, "Functionally Graded Polar Heterostructures: New Materials for Multifunctional Devices," in *Polarisation Effects in Semiconductors*, C. Wood, and D. Jena, Eds. New York: Springer, 2008, pp. 307-368.

[5] http://www.chemtube3d.com/solidstate/_wurtzite(final).htm

[6] C. Kittel, *Introduction to Solid State Physics*. New York: Wiley, 2005, pp. 16.

[7] T. Nann and J. Schneider, "Origin of permanent electric dipole moments in wurtzite nanocrystals," *Chemical Physics Letters*, 384, pp. 150-152, 2004.

[8] F. Bernardini, "Spontaneous and Piezoelectric Polarisation: Basic Theory vs. Practical Recipes," in *Nitride Semiconductor Devices*, J. Piprek, Ed. Weinheim: Wiley, 2007, pp. 49-69.

[9] O. Ambacher, and V. Cimalla, "Polarisation Induced Effects in GaN-based Heterostructures and Novel Sensors," in *Polarisation Effects in Semiconductors*, C. Wood, and D. Jena, Eds. New York: Springer, 2008, pp. 27-103.

[10] C. Mailhiot, and D. L. Smith, "Effects of strain-induced electric fields on the electronic structure of [111] growth axis semiconductor superlattices," *Journal of Vacuum Science & Technology*, vol. 4, pp. 996-999, 1986.

[11] F. Bernardini, V. Fiorentini, and D. Vanderb, "Spontaneous polarisation and piezoelectric constants of III-V nitrides," *Physics Review B*, vol. 56, no. 16, pp. R10024--R10027, 1997.

[12] J. D. Simon, "Polarisation-engineered III-V Nitride Heterostructure devices by Molecular Beam Epitaxy," Ph.D thesis, Electrical Engineering, Univ. of Notre Dame, Indiana, 2009.

[13] H. Morkoc, and J. Leach, "Polarisation in GaN Based Heterostructures and Heterojunction Field Effect Transistiors (HFETs)," in *Polarisation Effects in Semiconductors*, C. Wood, and D. Jena, Eds. New York: Springer, 2008, pp. 373-457.

[14] T. Mimura, S. Hiyamizu, T. Fujii, and K. Nanbu, "A New Field-Effect Transistor with Selectively Doped GaAs/n-$Al_xGa_{1-x}As$ Heterojunctions," *Japanese Journal of Applied Physics*, vol. 19, no. 5, pp. L225-L227, 1980.

[15] N. H. Sheng, C. P. Lee, R. T. Chen, D. L. Miller, "GaAs/AlGaAs Double Heterostructure High Electron Mobility Transistors," *IEEE International Electron Devices Meeting*, Technical Digest, pp. 352-355, 1984.

[16] M. Asif Khan , J. N. Kuznia , J. M. Van Hove , N. Pan and J. Carter, "Observation of a two-dimensional electron gas in low pressure metalorganic chemical vapor deposited GaN-AlGaN heterojunctions," *Applied Physics Letters*, vol. 60, no. 24, pp. 3027-3029, 1992.

[17] O. Ambacher, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy, et al., "Two-dimensional electron gases induced by spontaneous and piezoelectric polarisation charges in N- and Ga-face AlGaN/GaN heterostructures," *Journal of Applied Physics*, vol. 85, no. 6, pp. 3222-3233, 1999.

[18] E. T. Yu, G. J. Sullivan, P. M. Asbeck, C. D. Wang, D. Qiao, and S. S. Lau, "Measurement of piezoelectrically induced charge in GaN/AlGaN heterostructure field-effect transistors," *Applied Physics Letters*, vol. 71, pp. 2794-2796, 1997.

[19] I. P. Smorchkova, C. R. Elsass, J. P. Ibbetson, R. Vetury, B. Heying, P. Fini, et al., "Polarisation-induced charge and electron mobility in AlGaN/GaN heterostructures grown by plasma-assisted molecular-beam epitaxy," *Journal of Applied Physics*, vol. 86, no. 8, pp. 4520-4526, 1999.

[20] S. Heikman, S. Keller, Y. Wu, J. S. Speck, S. P. DenBaars, and U. K. Mishra, "Polarisation effects in AlGaN/GaN and GaN/AlGaN/GaN heterostructures," *Journal of Applied Physics*, vol. 93, no. 12, pp. 10114-10118, 2003.

[21] A. D. Bykhovski, B. L. Gelmont, and M. S. Shur, "Elastic strain relaxation and piezoeffect in GaN-AlN, GaN-AlGaN and GaN-InGaN superlattices," *Journal of Applied Physics*, vol. 81, no. 9, pp. 6332-6338, 1997.

[22] A. Laposa, J. Jakovenko, and M. Husak, " Temperature dependence of the pyroelectric behaviour in GaN/AlGaN," in *Proceedings of the 8th International Conference on Advanced Semiconductor Devices & Microsystems*, Smolenice, 2010, pp. 93-96.

[23] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*. New York: Springer, 2008.

[24] W. S. Tan, P. A. Houston, P. J. Parkbrook, D. A. Wood, G. Hill and C. R. Whitehouse, "Gate leakage effects and breakdown voltage in metalorganic vapor phase epitaxy AlGaN-GaN heterostructure field-effect transistors," *Applied Physics Letters*, vol. 80, no. 17, pp. 3207-3211, 2002.

[25] N. Dyakonova, A. Dickens, M. S. Shur, R. Gaska and J. W. Yang, "Temperature dependence of impact ionisation in AlGaN-GaN heterostructure field effect transistors," *Applied Physics Letters*, vol. 72, no. 20, pp. 2562-2564, 1998.

[26] J. W. Johnson, J. R. LaRoch, F. Fen, B.P. Gilla, M. E. Overberg, C. R. Abernathy, et al., "Schottky rectifiers fabricated on free-standing GaN substrates," *Solid State Electronics*, vol. 45, pp. 405-410, 2001.

[27] A. P. Zhang, G. T. Dang, F. Ren, H. Cho, K. P. Lee, K. P. Pearton, et al., "Comparison of GaN P-I-N and Schottky Rectifier Performance," *IEEE Transactions on Electron Devices*, vol. 48, no. 3, pp. 407-412, 2001.

[28] V. A. Dmitriev, K. G. Irvine, C. H. Carter, N. I. Kuznetsov, and E. V. Kalinin, "Electric breakdown in GaN p-n junctions," *Applied Physics Letters*, 68(2):229-232, 1996.

[29] A. Nakajima, M. H. Dhyani, Y. Sumida, H. Kawai, and E. M. S. Narayanan, "GaN Based Super HFETs over 700V Using the Polarisation Junction Concept," in *Proceedings of the 23rd International Symposium on Power Semiconductor Devices & ICs*, San Diego, 2011, pp. 280-283.

[30] J. A. Appels and H. M. J. Vaes, ``HV Thin Layer Devices (RESURF Devices)," in *Proceedings of International Electron Devices Meeting*, pp. 238-241, 1979.

[31] J. S. Ajit, D. Kinzer, and M. Ranjan, "1200V high-side lateral MOSFET in junction-isolated power IC technology using two field reduction layers," in *Proceedings of International Symposium on Power Semiconductor Devices & ICs*, 1993, pp. 230–235.

[32] A. W. Ludikhuize, "A review of RESURF technology," in *Proceedings of International Symposium on Power Semiconductor Devices & ICs*, 2000, pp. 11–18.

[33] D. J. Coe, "High voltage semiconductor device," US Patent # 4754310, 1988.

[34] T. Fujihira, "Theory of semiconductor super junction devices," *Japanese Journal of Applied Physics*, vol. 36, pp. 6254–6262, 1997.

[35] G. Deboy, M. Marz, J. P. Stengel, H. Strack, J. Tihanyi, and H. Weber, "A new generation of high voltage MOSFET's breaks the limits line of silicon," in *Proceedings of International Electron Devices Meeting*, 1998, pp. 683–685.

[36] N. Q. Zhang, S. Keller, G. Parish, S. Heikman, S. P. DenBaars, and U. K. Mishra, "High breakdown GaN HEMT with overlapping gate structure," *IEEE Electron Device Letters*, vol. 21, p. 421, 2000.

[37] Y. Ando, Y. Okamoto, H. Miyamoto, T. Nakayama, T. Inoue, and M. Kuzuhara, "10-W/mm AlGaN-GaN HFET with a field modulation plate," *IEEE Electron Device Letters*, vol. 24, pp. 289–291, May 2003.

[38] W. Saito, Y. Takada, M. Kuraguchi, K. Tsuda, I. Omura, and T. Ogura, "Design and Demonstration of High Breakdown Voltage GaN High Electron Mobility Transistor (HEMT) Using Field Plate Structure for Power Electronics Applications," *Japanese Journal of Applied Physics*, vol. 43, no. 4B, pp. 2239–2242, 2004.

[39] W. Saito, M. Kuraguchi, Y. Takada, K. Tsuda, I. Omura, and T. Ogura, "Design Optimisation of High Breakdown Voltage AlGaN–GaN Power HEMT on an Insulating Substrate for $R_{ON}A$–V_B Trade-off Characteristics," *IEEE Transactions on Electron Devices*, vol. 52, no. 1, pp. 106-111, 2005.

[40] S. Sudharsanan, and S. Karmalkar, "Modeling of the reverse gate leakage in AlGaN/GaN high electron mobility transistors," *Journal of Applied Physics*, vol. 107, pp. 064501-1- 064501-3, 2010.

[41] H. J. Nam, H. G. Choi; M. W. Ha; H. J. Song; C. H. Roh, J. H. Lee, et al., "Suppression of Leakage Currents in AlGaN/GaN HEMTs by Optimizing the Thermal Ramping Rate during the Ohmic RTP Process," *Journal of the Korean Physical Society*, vol. 59, no. 2, pp. 439-442, 2011.

[42] E. J. Miller, E. T. Yu, P. Waltereit and J. S. Speck, "Analysis of reverse-bias leakage current mechanisms in GaN grown by molecular-beam epitaxy," *Applied Physics Letters*, vol. 84, no. 4, pp. 535-537, 2004.

[43] A. Fontserè, A. Pérez-Tomás, M. Placidi, N. Baron, S. Chenot, J. C. Moreno, et al., "Molecular beam epitaxial AlGaN/GaN high electron

mobility transistors leakage thermal activation on silicon and sapphire," *Applied Physics Letters*, vol. 102, pp. 093503-1- 093503-5, 2013.

[44] B. Lu, E. L. Piner, and T. Palacios, "Breakdown Mechanism in AlGaN/GaN HEMTs on Si Substrate," in *Proceedings of the 68th Device Research Conference*, Notre Dame, 2010, pp. 193-194.

[45] S. Karmalkar, M. S. Shur, and R. Gaska, "GaN-Based Power High Electron Mobility Transistors," in *Wide Energy Bandgap Electronic Devices*, F. Ren, and J. C. Zolper, Eds. Singapore: World Scientific Publishing, 2003, pp. 174-213.

[46] B. Luo, R. Mehandru, J. Kim, F. Ren, B.P. Gila, A.H. Onstine, et al., "Comparison of surface passivation films for reduction of current collapse in AlGaN/GaN high electron mobility transistors," Journal of Electrochemical Society, vol. 149, pp. G613–G619, 2002.

[47] T. E. S. Arulkumaran, H. Ishikawa, and T. Jimbo, "Comparative study of drain-current collapse in AlGaN/GaN high electron-mobility transistors on sapphire and semi-insulating SiC," *Applied Physics Letters*, vol. 81, pp. 3073-3075, 2002.

[48] M. J. Uren, M. Silvestri, M. Cäsar, G. A. M. Hurkx, J. A.Croon, J. Šonský, and M. Kuball, "Intentionally carbon-doped AlGaN/GaN HEMTs: Necessity for vertical leakage paths," *IEEE Electron Device Letters*, vol. 35, no. 3, pp. 327–329, Mar. 2014.

[49] W. Saito, Y. Kakiuchi, T. Nitta, Y. Saito, T. Noda, H. Fujimoto, et al., "Field-plate structure dependence of current collapse phenomena in high-voltage GaN-HEMTs," *IEEE Electron Device Letters*, vol. 31, no. 7, pp. 659–661, Jul. 2010.

Chapter 3 Introduction to Polarisation Super Junction and Development of Large Area Devices

In this chapter, the concept of Polarisation Super Junction (PSJ) is introduced initially. Numerical simulation results are presented comparing two designs, one of which is based on Field Plate (FP) engineering and the other is based on PSJ to gain insight into the physical mechanisms in the device that determine the electrical characteristics. Following that, device design and scalability to large area devices, process development, mask design, processing challenges, and results of device fabrication will be presented and discussed in detail.

3.1 Introduction to Polarisation Super Junction

The concept of Superjunction (SJ) was envisaged and developed more than two decades ago for Silicon (Si) power semiconductor devices, and today it is considered a mature technology for device design and manufacturing of high voltage devices. It was a revolutionary concept which could overcome the material limited trade-off relationship between breakdown voltage and specific on-state resistance ($R_{ON}.A$) of conventional power semiconductor devices. The concepts of RESURF and SJ were discussed in chapter 2. Fig. 3.1 shows the schematics and electric field profiles of conventional Schottky Barrier Diode (SBD) and a structure based on SJ [1].

E_B and V_B shown in Fig. 3.1 represent the critical electric field and breakdown voltage respectively. The relationship between E_B and V_B can be derived from basic electrostatics and has also been shown in the figure. It is apparent that a similarly dimensioned device employing SJ in its structure will sustain significantly higher voltage for a given drift length.

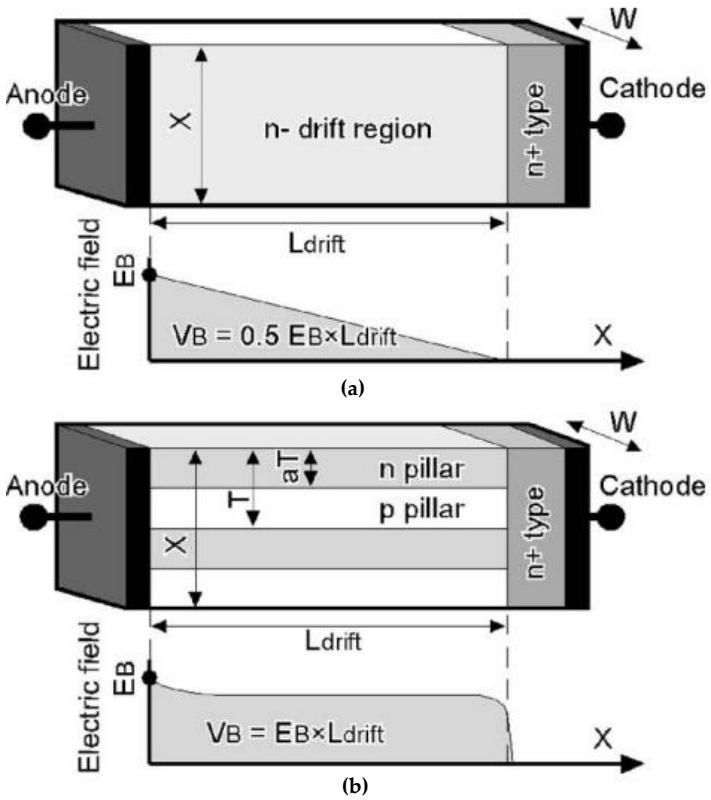


Figure 3.1 Schematics and electric field distribution at breakdown of (a) conventional SBD and (b) SJ SBD [1]

The values of critical electric field of wide bandgap semiconductors such as Gallium Nitride (GaN) and Silicon Carbide (SiC) are about ten times higher than that of Si. An improvement by two orders of magnitude in the limit of $R_{ON}.A$ is expected by replacing Si with wide bandgap semiconductors [1]. However, the fabrication of SJ devices using GaN based on a traditional approach as performed in Si is difficult since it requires precise doping control techniques, and incorporating the same in GaN required a novel approach.

The concept of Polarisation Super Junction (PSJ) was conceived and proposed by A. Nakajima et al. in 2006 [1]. Schematic of a simple AlGaN/GaN diode based on this concept is shown in Fig. 3.2 (a).

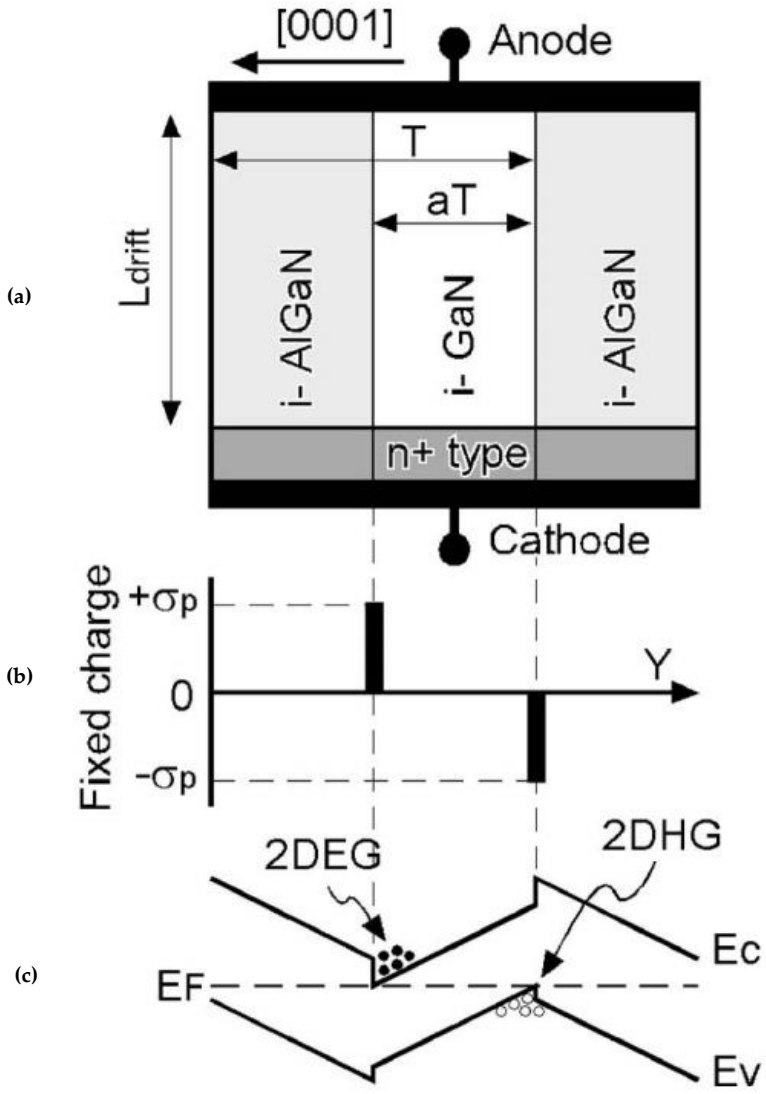


Figure 3.2 (a) Schematic of a PSJ diode (layers grown along the [0001] direction), (b) polarisation charge distribution, and (c) energy band diagram [1]

The structure is composed of alternately stacked undoped GaN and AlGaN layers along the [0001] direction of crystal growth. As discussed in Chapter 2, high density polarisation charges σ_p > ~ 10^{13} cm^{-2} can be spontaneously generated at the heterointerfaces of group III-nitrides. The magnitude of polarisation in AlGaN is higher than that in GaN. Spontaneous polarisation within the material has a fixed orientation depending on the direction of growth and the orientation of piezoelectric polarisation depends on whether the constituent layers experience compressive or tensile strain. Therefore, when the material is grown along the [0001] direction (also referred to as Ga-face, or +c

direction) the interface formed when AlGaN is pseudomorphically grown on GaN effectively has positive charges and the interface formed when GaN is grown on AlGaN effectively develops negative polarisation charges. This has been shown in Fig. 3.2 (b). The density of positive and negative charges could be controlled to be perfectly matched during crystal growth. Therefore, a high charge balance condition could be easily achieved and structures based on PSJ could have charge compensation effects similar to ideal SJ structures.

In addition, PSJ has an additional feature that the traditional SJ does not have. Fig. 3.2 (c) shows the schematic of the energy band diagram within an AlGaN/GaN/AlGaN double heterostructure. Due to the polarity of polarisation charges, high density two-dimensional electron gas (2DEG) and two-dimensional hole gas (2DHG) can be spontaneously formed at the AlGaN/GaN and GaN/AlGaN heterointerfaces, respectively without any intentional doping. 2DEG and 2DHG are well-confined to quantum wells at the respective interfaces and have relatively high values of mobility because of negligible impurity scattering [1]. Despite theoretical predictions of high density 2DHG induced by negative polarisation charges at such interfaces, the first demonstration of high density 2DHG of over 10^{13} cm^{-2} was achieved by researchers at the University of Sheffield and Japanese firm POWDEC K.K in 2010 [2]. The details of structural optimisation performed to obtain high density 2DHG have also been elaborated in that report.

Figure 3.3 (a) shows the schematic of the optimised layer structure that was grown for the study [2], which consisted of an undoped GaN/AlGaN/GaN double heterostructure capped with a p-type GaN layer doped with Mg.

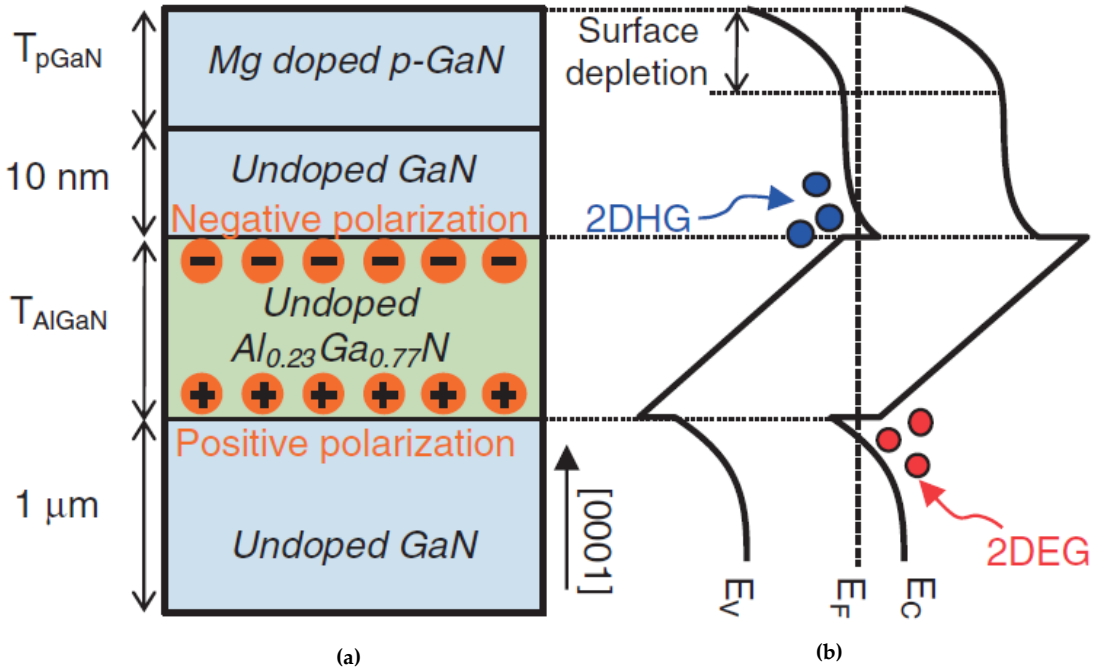


Figure 3.3 Schematics of (a) layer structure and (b) energy band diagram [2]

For the structure with Al composition of the AlGaN layer (47nm) and the Mg doping density of the p-GaN (30 nm), fixed at 23% and 3 x 10^{19} cm^{-3} respectively, the measured 2DHG sheet density and mobility were 1.1 x 10^{13} cm^{-2} and 16 cm^2 V^{-1} s^{-1} respectively. The demonstration of high density 2DHG could pave the way forward to develop p-channel HFETs in GaN.

The same research group also demonstrated high voltage GaN HFETs on Sapphire substrates based on the PSJ concept in 2011 [3]. Fig. 3.4 shows a simplified cross section of a normally-on PSJ based Super HFET as well as the ideal electric field distribution at the lower AlGaN/GaN interface, under off-state Drain bias.

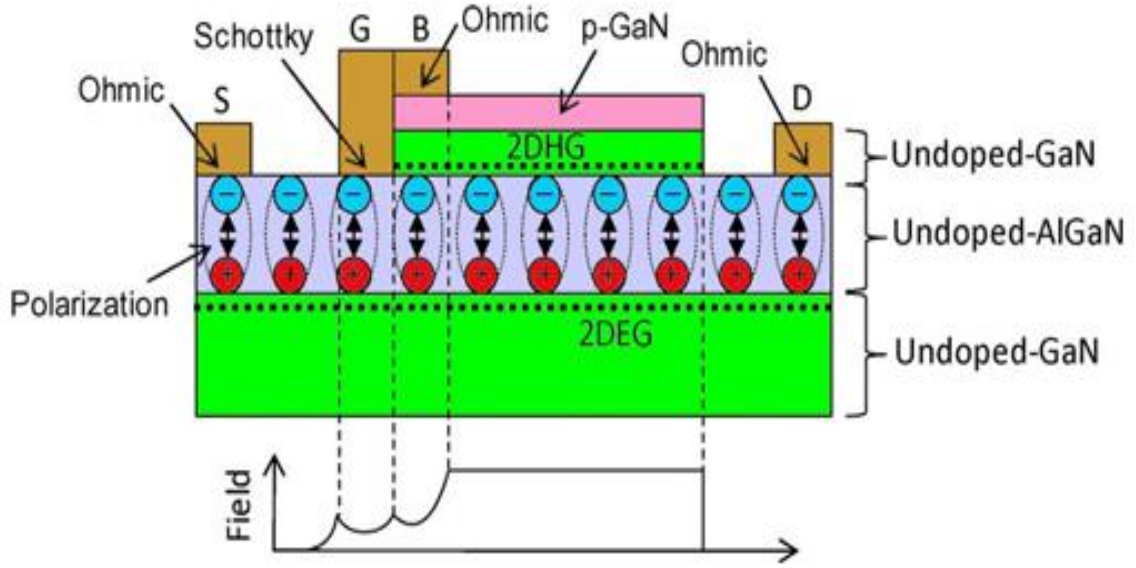
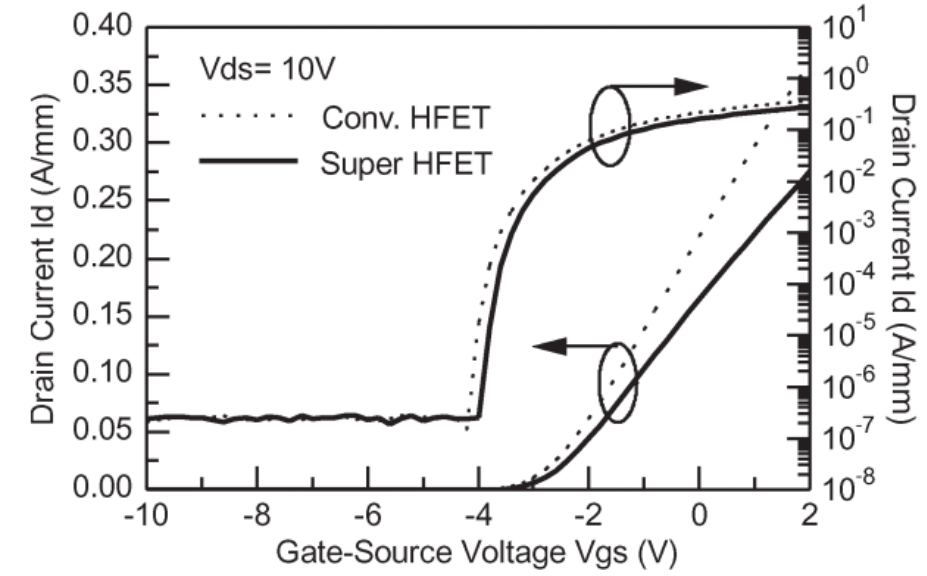


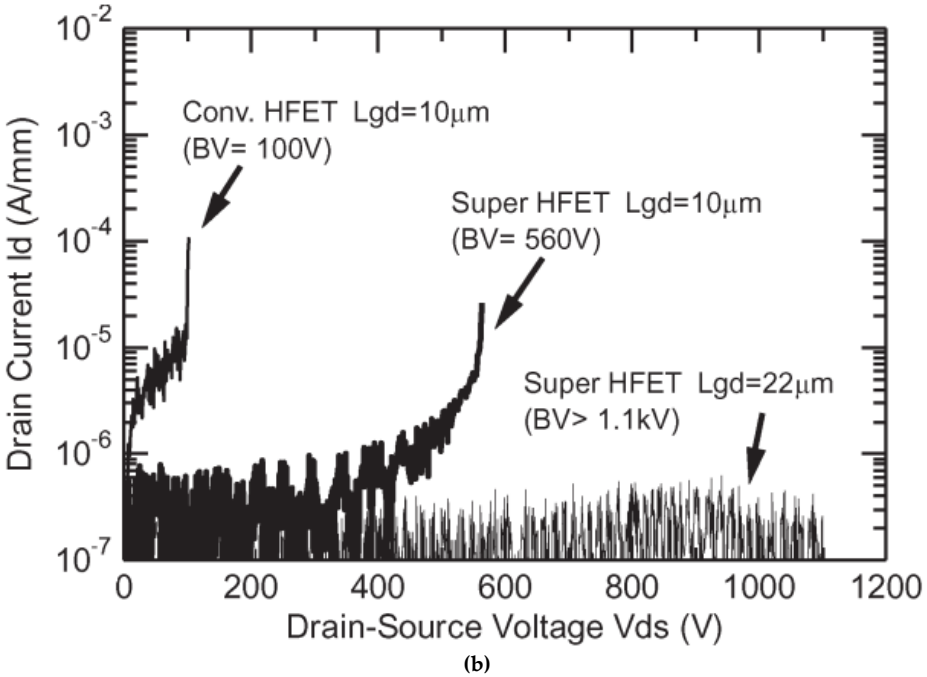
Figure 3.4 Schematic of a PSJ HFET and the electric field distribution in the off-state

The layer structure of HFET consisted of an undoped GaN/AlGaN/GaN double-heterostructure with a p-GaN cap layer. The PSJ HFET has four electrodes namely: Gate, Drain, Source, and Base. The Drain and Source electrodes form ohmic contacts to the 2DEG and the Gate is formed through a Schottky contact. The basic differences between conventional HFETs and the PSJ HFET are the additional Base electrode and presence of the 2DHG induced by negative polarisation charge at the upper GaN/AlGaN heterointerface. The base makes an ohmic contact to the 2DHG through the top p-GaN layer and is electrically connected to the gate. In the on-state, with an applied Drain bias, current flows from the Drain to Source through the 2DEG as in conventional HFETs. As this is a normally-on device, a negative Gate-Source voltage (V_{GS}) needs to be applied to deplete the channel under the Gate and turn the device to off-state. Under-off state and further increase in Drain voltage, the drift region is fully depleted maintaining charge balance and a flat electric field distribution can be ideally achieved as illustrated in Fig. 3.4. As a result, compared to a conventional HFET, the breakdown voltage (BV_{DSS} *or* BV) capability of HFETs based on PSJ

could be significantly enhanced for a given drift length, and achieve the best compromise between $R_{ON}.A$ and BV.



(a)



(b)

Figure 3.5 (a) DC transfer characteristics (b) Off-state I_D–V_{DS} characteristics [3]

Fig. 3.5 (a) shows the measured I_D–V_{GS} characteristics under dc conditions of co-fabricated conventional and PSJ HFETs with an L_{GD} = 10 μm at V_{DS} = 10 V, and (b) shows the measured off-state I_D–V_{DS} curves at V_{GS} = − 15 V. For the same drift length of L_{GD} = 10 μm, compared to 100 V for a conventional HFET without field

plate, a higher *BV* of 560 V is measured in the PSJ HFET without incorporating any field plate in the structure. The *BV* of PSJ HFETs is significantly enhanced due to charge compensation effect between the positive and negative polarisation charges [3].

The electrical performance of a slight variant of the PSJ HFET was reported in [4].

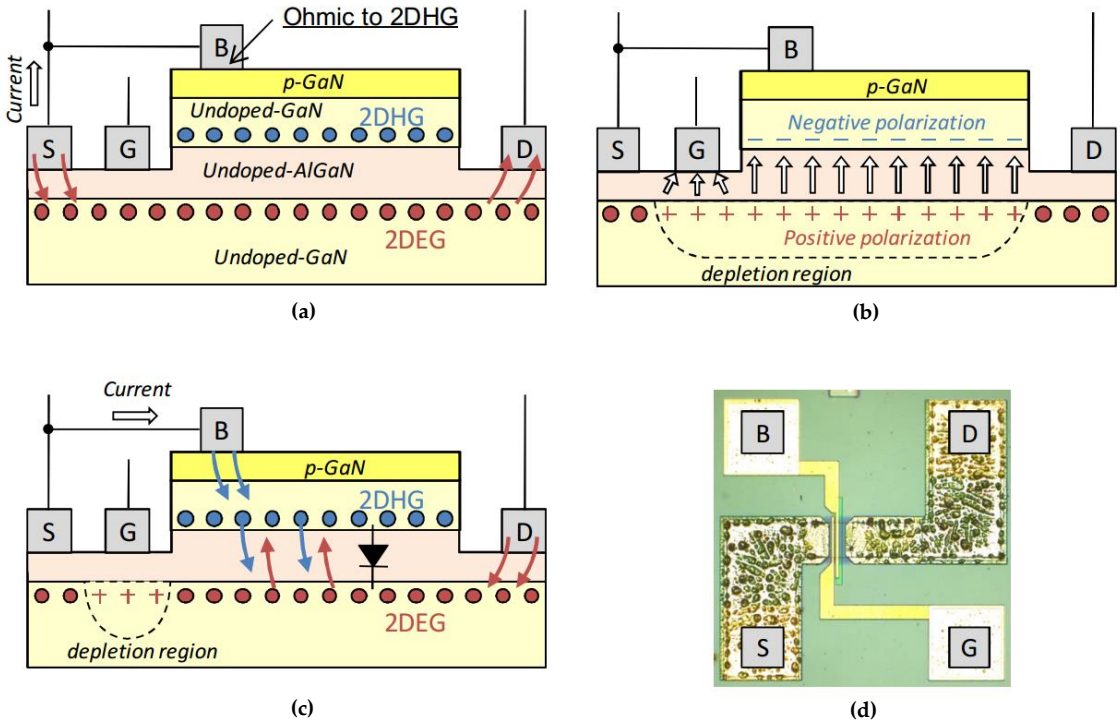
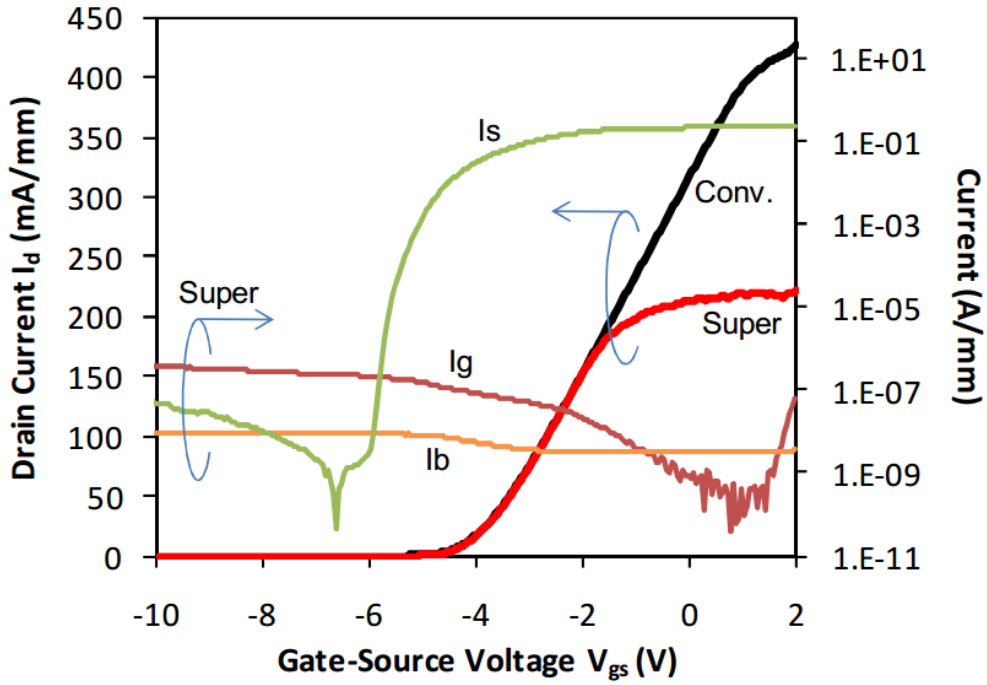


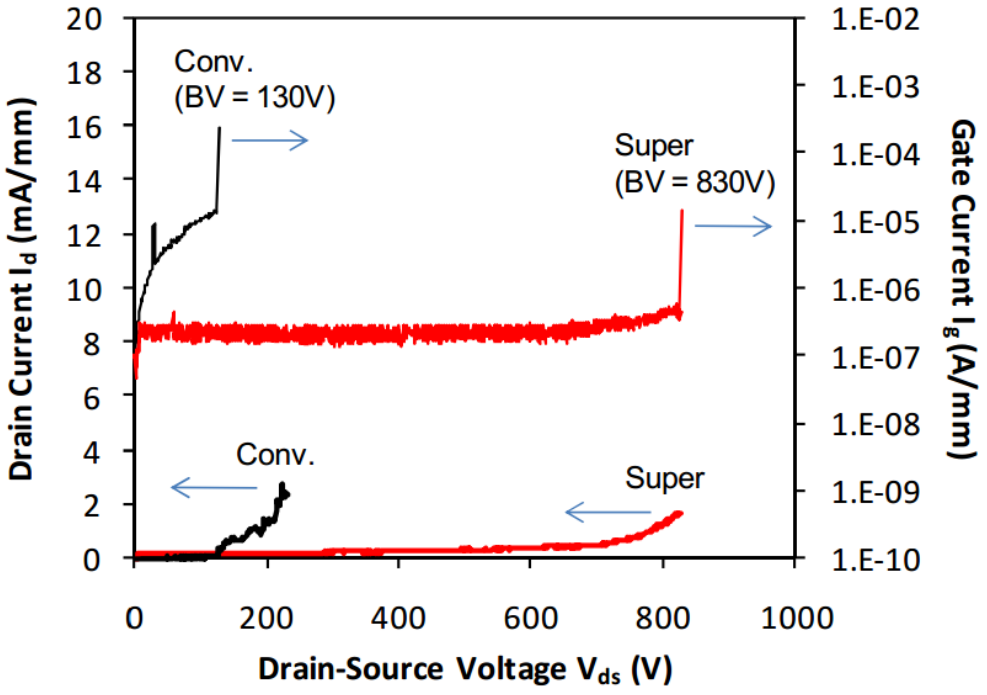
Figure 3.6 Schematics of a PSJ HFET illustrating (a) On-state (b) Off-state (c) reverse conduction and (d) micrograph of a fabricated device [4]

The schematic of the device test structure, operational mechanisms and optical micrograph have been shown in Fig. 3.6. In this device test structure, Base acts as an independent electrode and could be separately biased. Unlike conventional HFETs, the PSJ HFET has an intrinsic PN body diode formed by the 2DHG and 2DEG. During reverse conduction, holes and electrons are injected from the Base and Drain electrodes respectively and current flows from the Base to the Drain (Fig. 3.6 (c)). Fig. 3.7 (a) shows typical I_D-V_{GS} characteristics

of fabricated conventional HFETs and PSJ HFETs at V_{DS} = 10 V (Base-Source voltage V_{BS} = 0V).



(a)



(b)

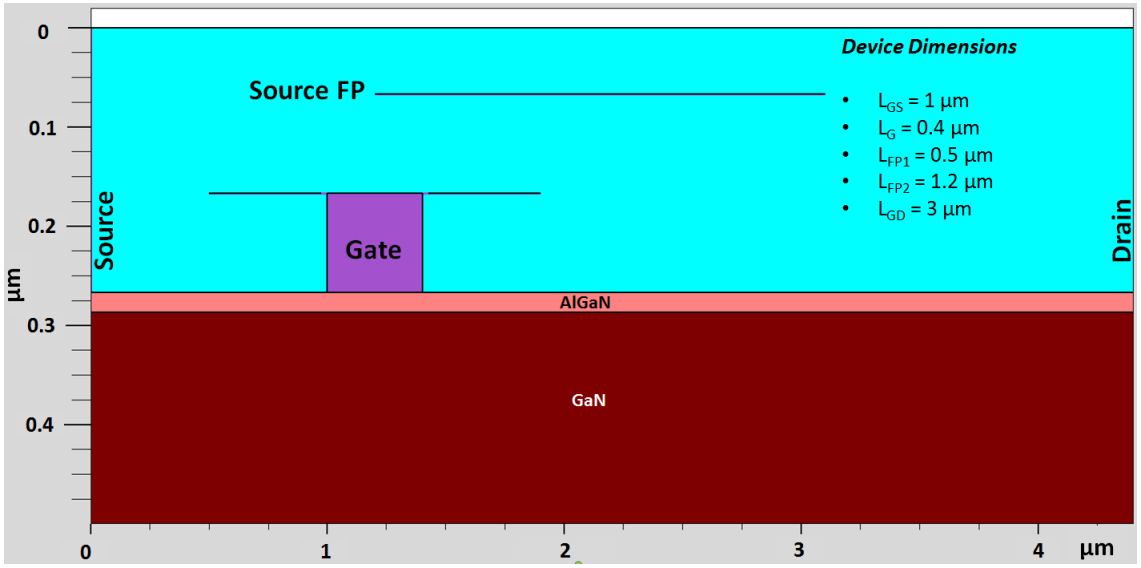
Figure 3.7 (a) Transfer characteristics at V_{DS} = 10 V (b) Off-state characteristics at V_{GS} = -10 V, of co-fabricated conventional and PSJ HFETs [4]

In conventional HFETs, the drain current linearly increases with the gate voltage. On the other hand, PSJ HFETs show drain current saturation, when V_{GS} is more than - 2V. The description of this behaviour has been elaborated in the next section with the aid of numerical simulations. Typical Off-state characteristics of co-fabricated conventional and PSJ HFETs measured at V_{GS} = - 10 V (L_{GD} = 13 μm) have been shown in Fig. 3.7 (b). The measured BV_{DSS} was over 700 V and with normalised R_{ON} of 15 Ω·mm, showed that the performance of PSJ HFET was comparable to that of the previously reported conventional HFETs with FP technologies.

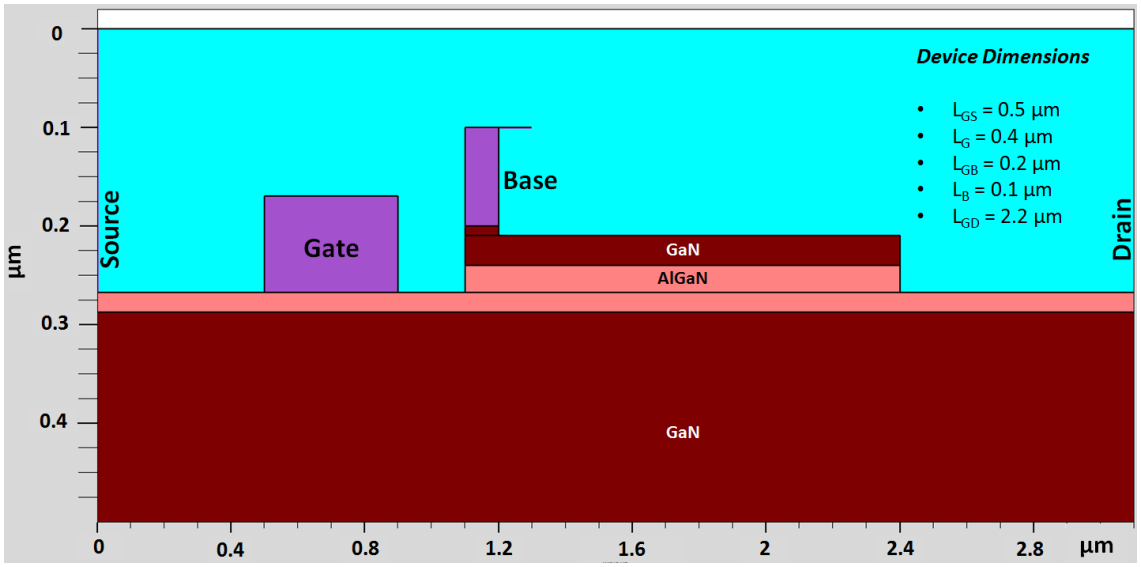
3.2 Numerical Simulations

TCAD simulations were performed using Silvaco ATLAS, to compare the electrical characteristics of a typical field plated (FP) HFET with that of the PSJ HFET. The primary objectives were to gain insight into the physical mechanisms in the device that govern the on-state and off-state electrical characteristics, rather than an exhaustive comparison as the performance using either approach could be fine-tuned by optimisation of the device design. The geometry of FP HFET was chosen based on [5,6] and that for PSJ HFET was chosen after an optimisation exercise such that both devices under consideration had identical values for BV (~ 500 V), matched transfer and output characteristics. This was achieved through iterative simulations and subsequent alterations of the PSJ HFET design parameters.

The cross-section schematics of the final designs for both architectures have been shown in Fig. 3.8. The Al mole fraction was fixed at 23%, AlGaN thickness for FP HFET was 20 nm and the same thickness was also used for PSJ HFET except in the PSJ drift region composed of the GaN/AlGaN/GaN double heterostructure (to be referred to as the PSJ region henceforth), where a higher AlGaN thickness of 47 nm was chosen.



(a)



(b)

Figure 3.8 Simulated structures (a) HFET with Field Plate [5,6] (b) PSJ HFET

Two different programs were developed based on the reference GANFET examples within the ATLAS simulation package for simulating the on-state and off-state characteristics respectively and the models were kept the same as those included in the examples. The physical models included for simulation of the on-state characteristics were – POLAR (Spontaneous Polarisation), CALC.STRAIN (Piezoelectric Polarisation), SRH (Shockley-Read-Hall, carrier generation-recombination), and ALBRCT.N to model electron mobility [7]. No specific models were included to model hole transport properties. The

simulated values of mobility in 2DEG and 2DHG are 1261.4 $cm^2/V.s$ and 8 $cm^2/V.s$ respectively. Surface states, self-heating and velocity saturation effects were not considered in this analysis. The p-GaN layer (under the Base electrode) within the simulated PSJ structure was defined as uniformly doped p-type with a doping density of 3 x 10^{17} cm^{-3} assuming incomplete ionisation and an activation of 1% within the typical physical structures doped with Mg concentration of 3 x 10^{19} cm^{-3} at 300 K [8]. The rest of the regions were defined as undoped.

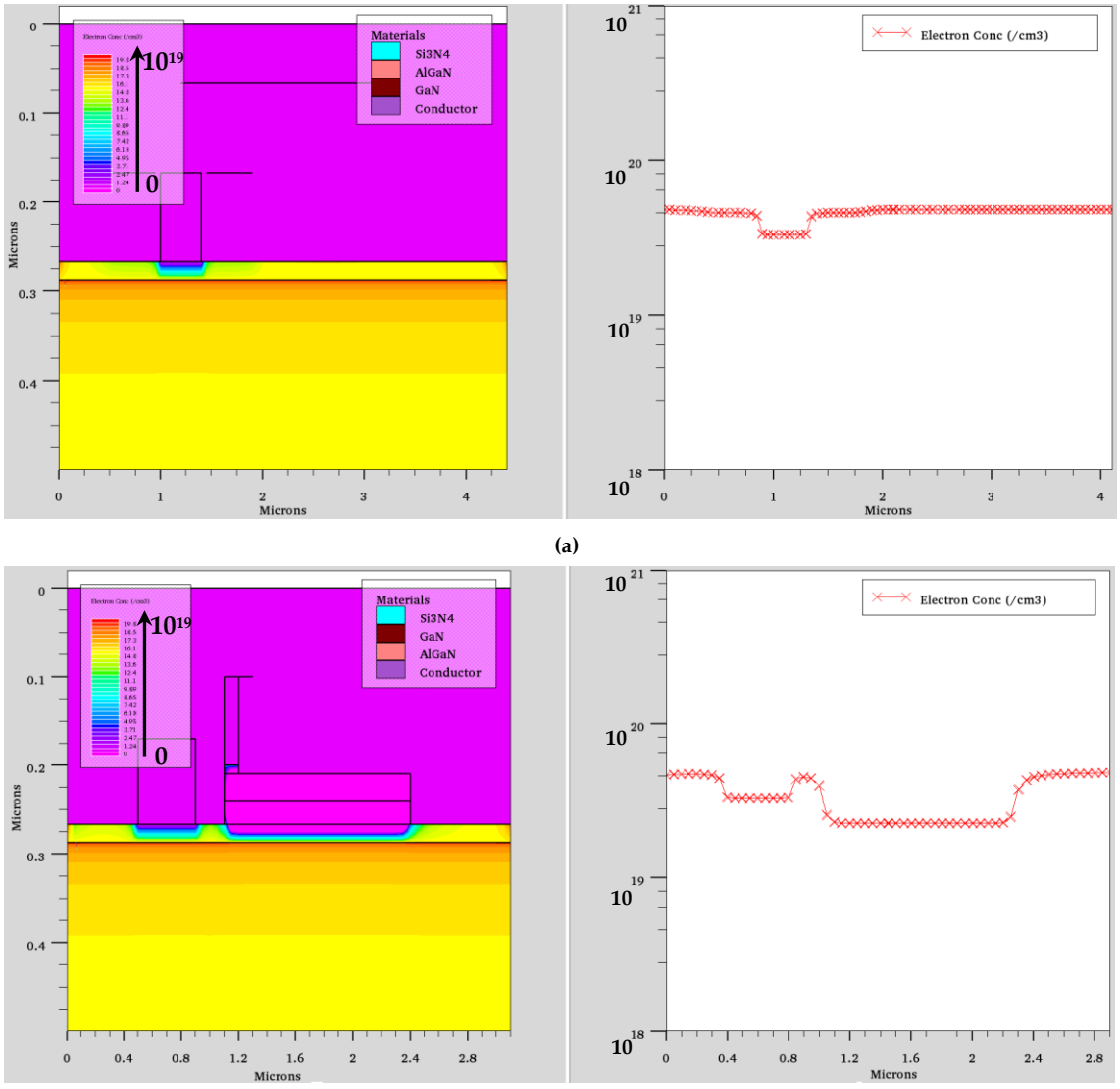
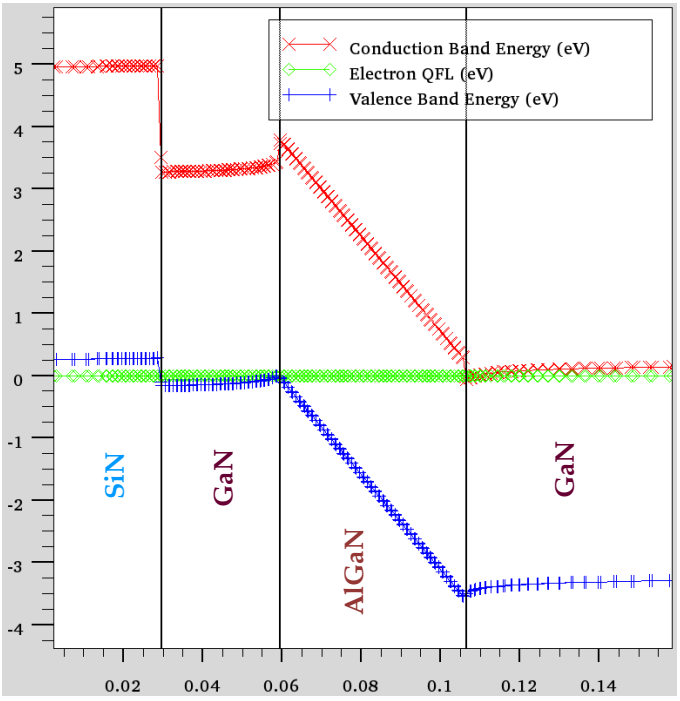
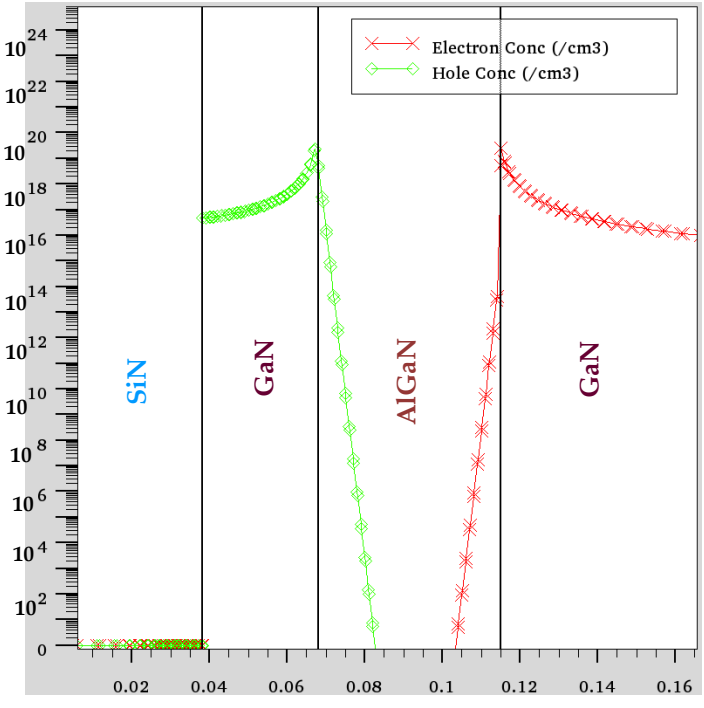


Figure 3.9 Electron distribution and profile along the AlGaN/GaN interface concentration at thermal equilibrium (a) HFET with Field Plate (b) PSJ HFET

Electron distribution and profile along the AlGaN/GaN interface at thermal equilibrium for the two structures have been shown in Figs. 3.9 (a)-(b). The energy band diagram and concentration of carriers (thermal equilibrium) within the PSJ layer of the PSJ HFET have been shown in Figs. 3.10 (a)-(b).



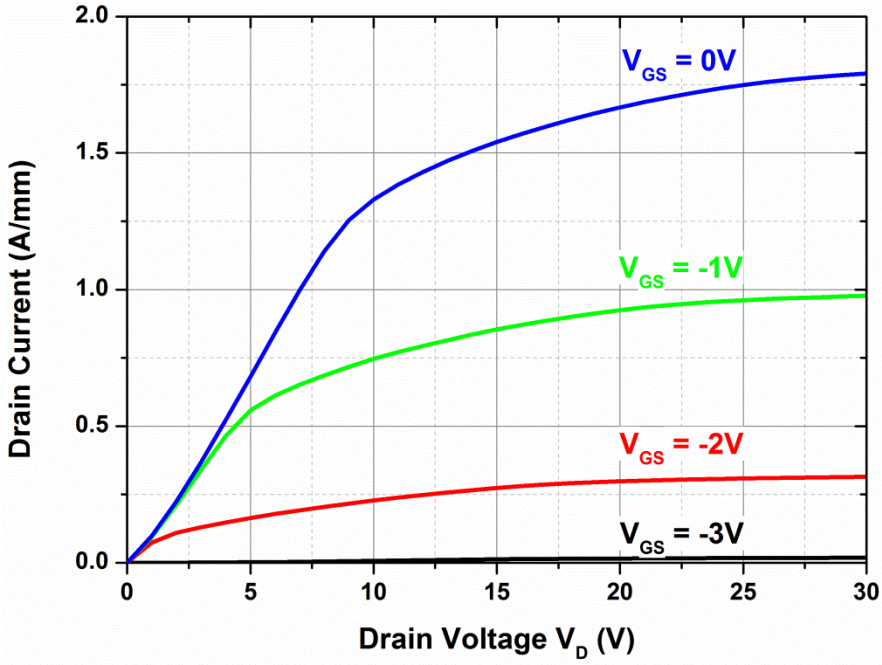
(a)



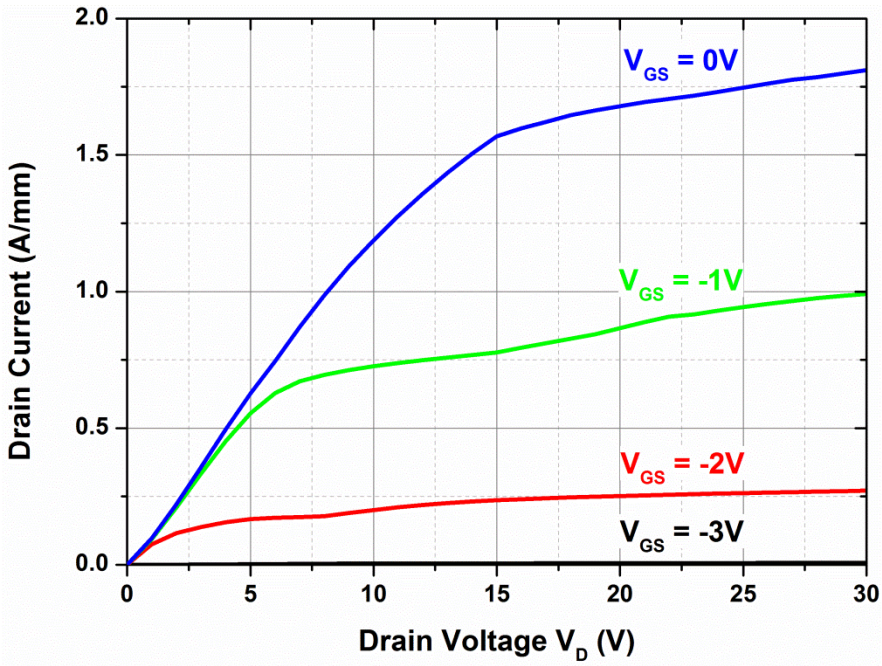
(b)

Figure 3.10 (a) Energy Band Diagram (b) Carrier Concentration

The simulated output characteristics and transfer characteristics have been shown in Fig. 3.11 and Fig. 3.12 respectively.



(a)

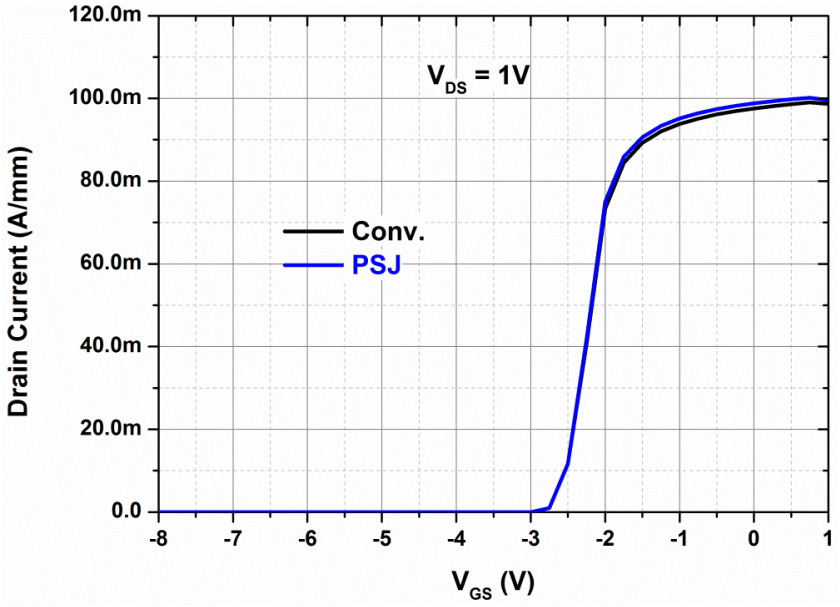


(b)

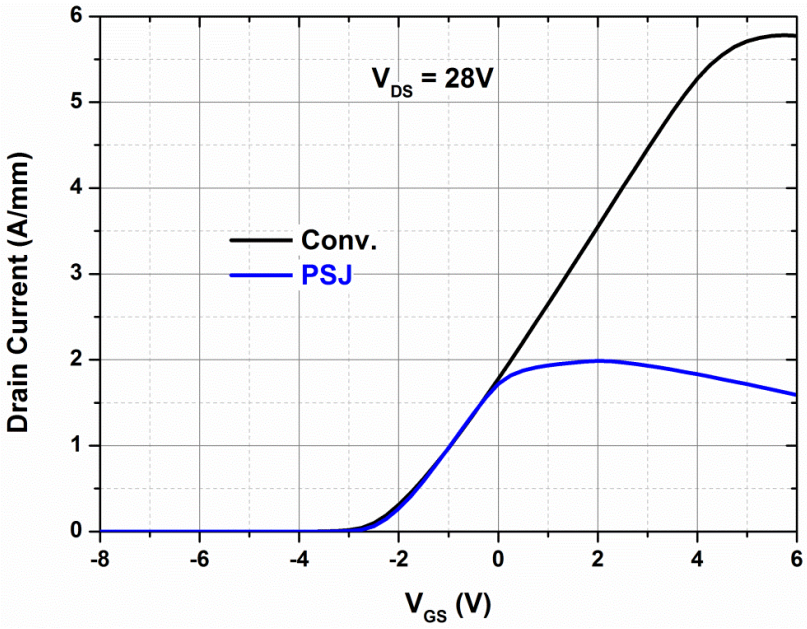
Figure 3.11 Simulated output characteristics (a) HFET with Field Plate (b) PSJ HFET

The transfer characteristics were simulated at V_{DS} = 1 V and V_{DS} = 28 V. This was performed to understand how the transfer characteristics varied as the

operation of the HFET changed from linear region to saturation region and also to explain the experimental results regarding early saturation of the Drain Current with respect to V_{GS} in a PSJ HFET when compared to a conventional or FP HFET.



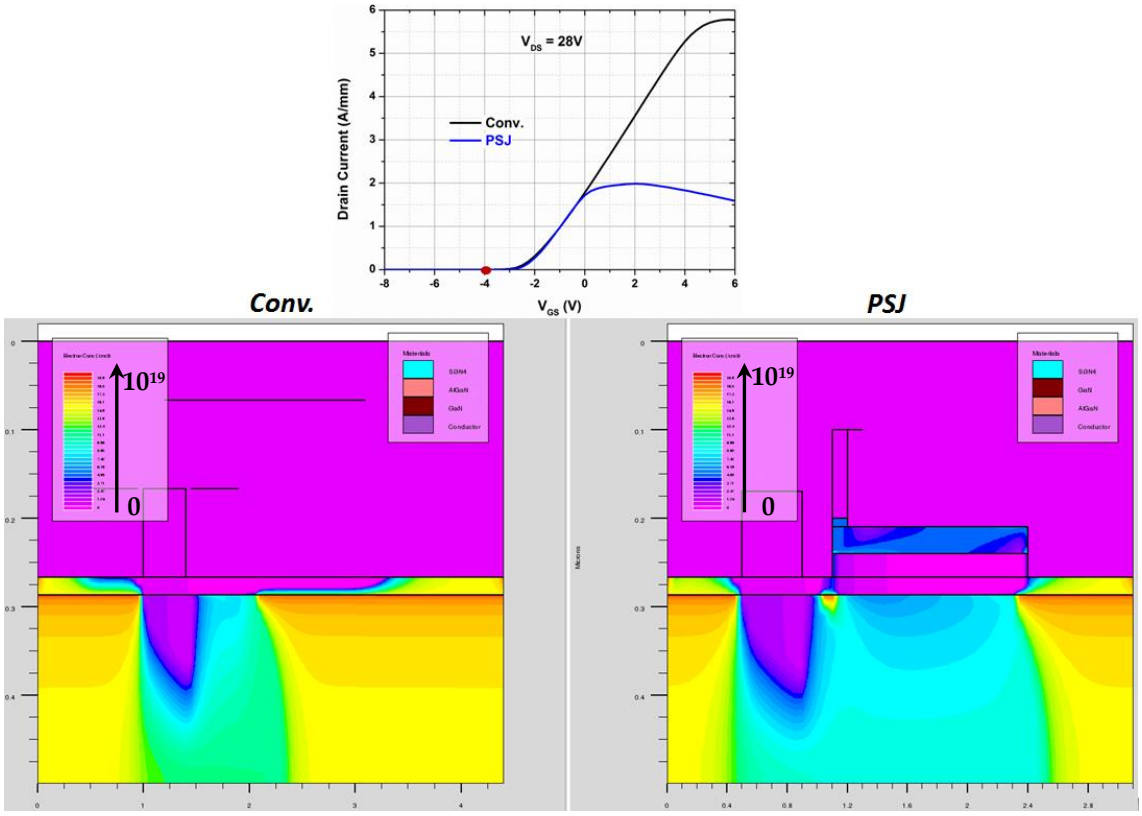
(a)



(b)

Figure 3.12 Simulated transfer characteristics (a) V_{DS} = 1 V (b) V_{DS} = 28 V

The general behaviour of the transfer characteristics in the saturation region as obtained from TCAD simulation results are aligned to the experimental results. When biased in the saturation region (V_{DS} = 28 V), the Drain Current in a PSJ HFET saturates when V_{GS} = 2 V, and in a FP HFET, this only occurs at V_{GS} = 5 V. This behaviour can be understood by studying the electron concentration in the two structures at various bias points of the transfer characteristics as illustrated with the aid of Figs. 3.13 to 3.18.



(a) (b)

Figure 3.13 Electron concentration at V_{GS}= -4 V (off-state) and V_{DS}= 28 V (a) HFET with Field Plate (b) PSJ HFET

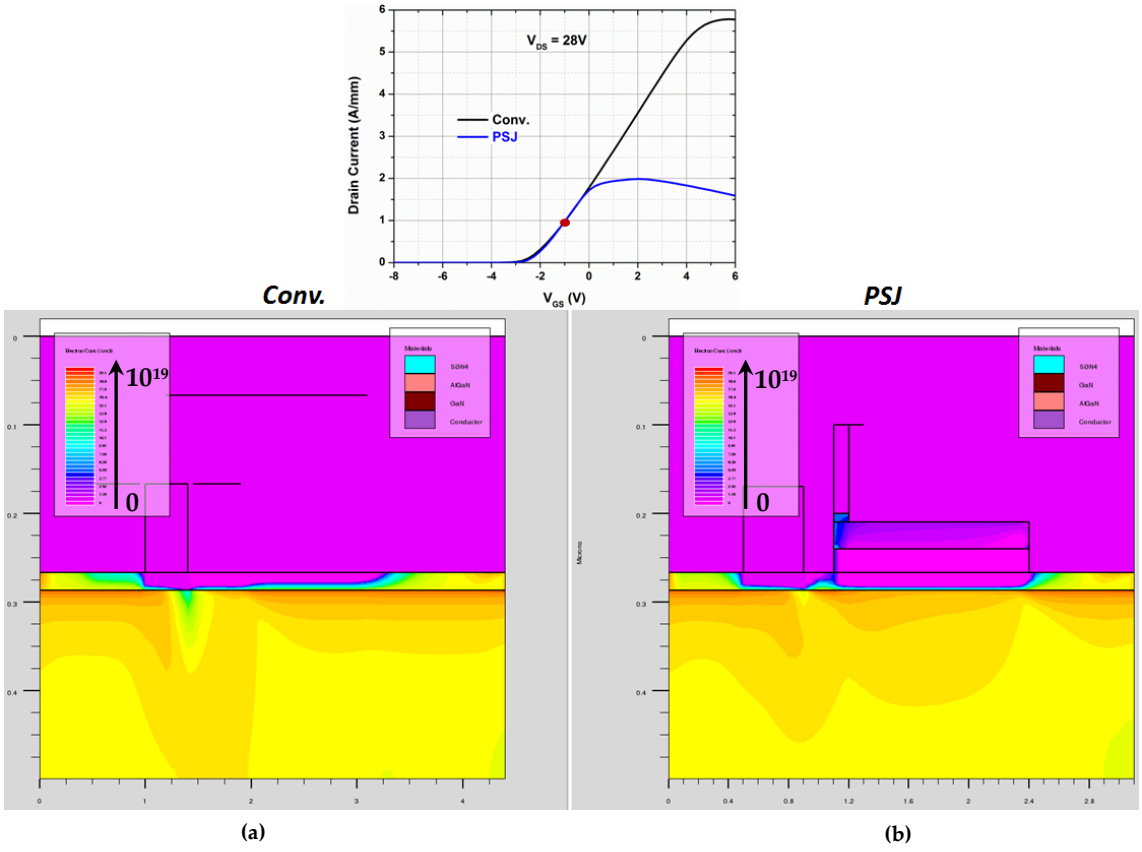


Figure 3.14 Electron concentration at V_{GS} = -1 V (on-state) and V_{DS} = 28 V (a) HFET with Field Plate (b) PSJ HFET

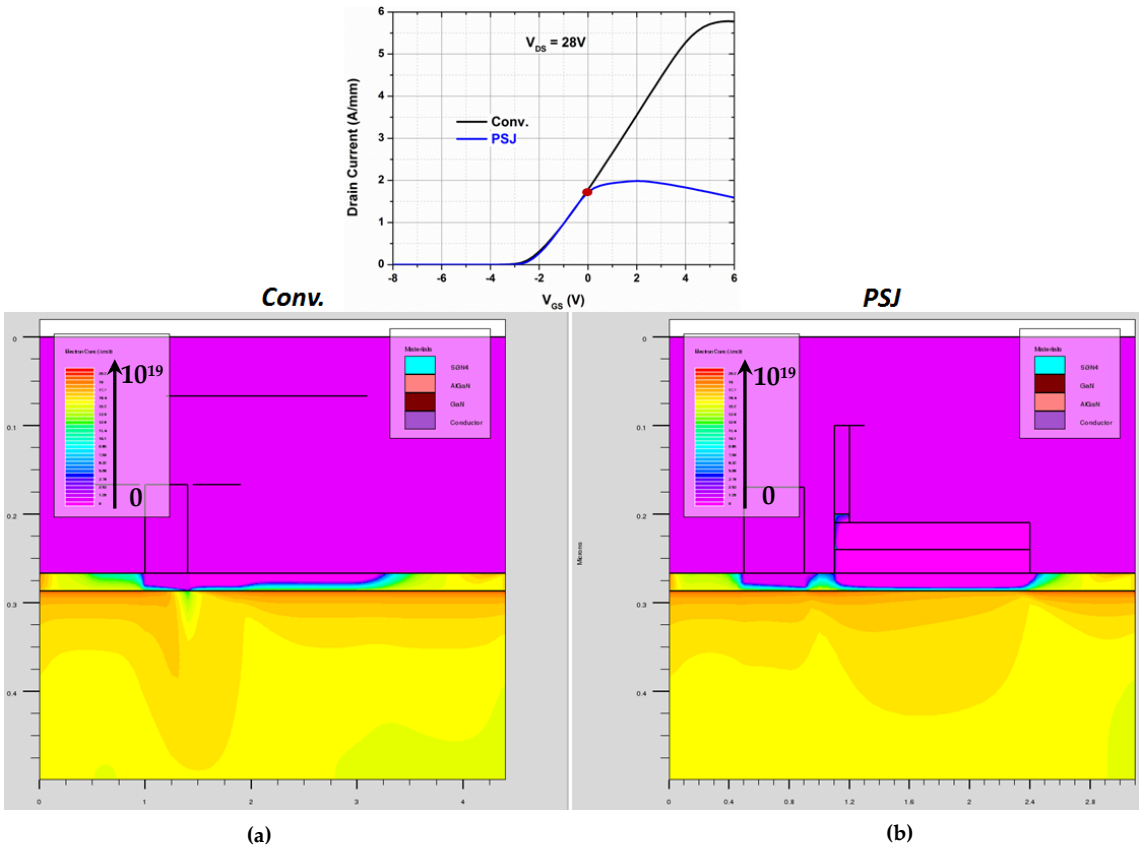
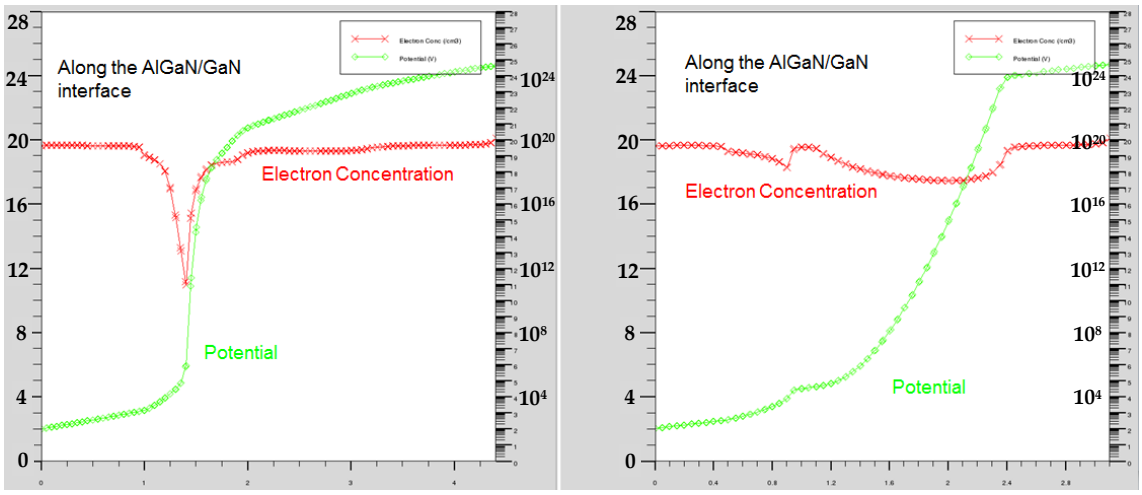


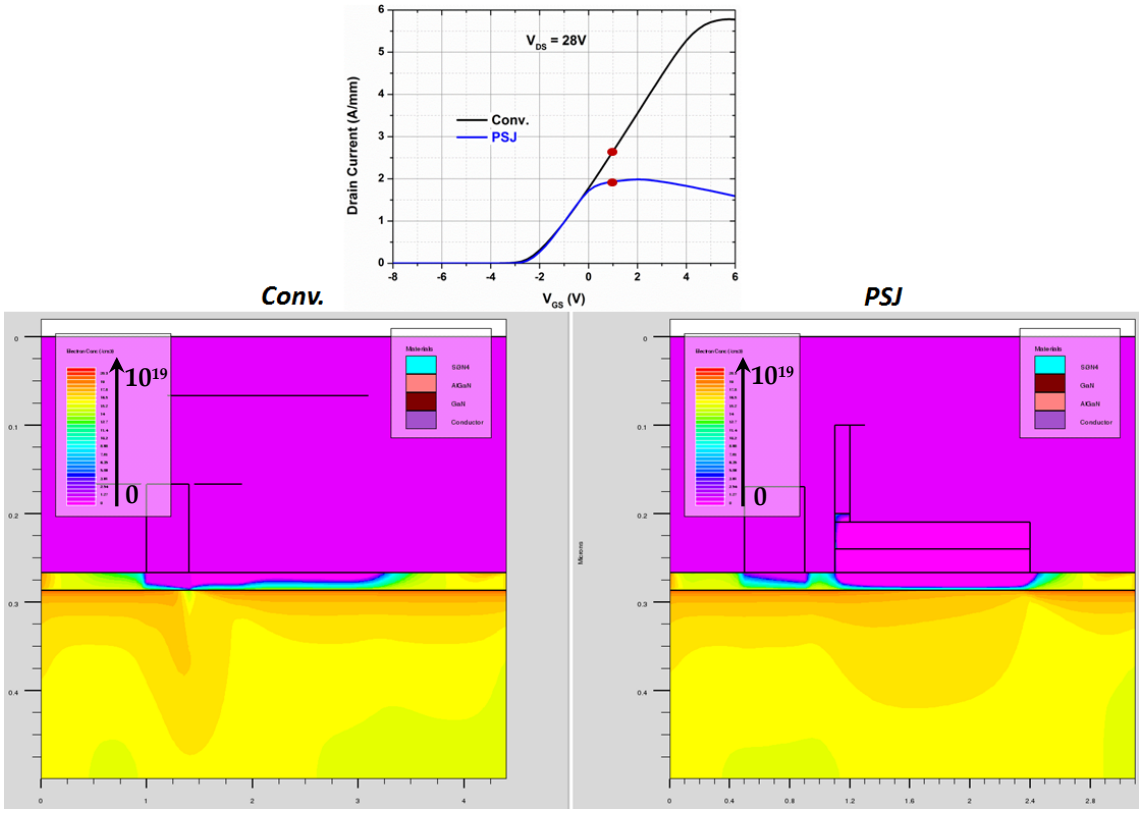
Figure 3.15 Electron concentration at V_{GS} = 0 V (on-state) and V_{DS} = 28 V (a) HFET with Field Plate (b) PSJ HFET



(a) (b)

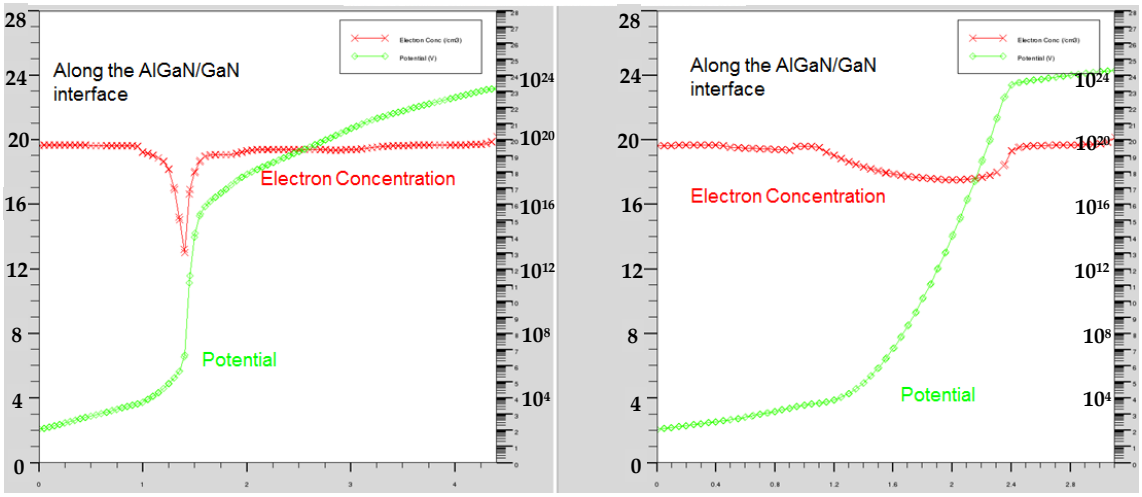
Figure 3.16 The profile of electron concentration and electric potential along the AlGaN/GaN interface at V_{GS} = 0 V (on-state) and V_{DS} = 28 V (a) HFET with Field Plate (b) PSJ HFET

As observed in any field effect transistor, the channel gets pinched-off at the drain side edge of gate when biased into the saturation region. This is observed in both FP HFET as well as PSJ HFET. However, in the case of PSJ HFET, substantial depletion of electron concentration (by more than two orders of magnitude at V_{GS} = 0 V and V_{DS} = 28 V) is also observed under the PSJ region, as a PN junction is formed by the 2DHG and 2DEG intrinsically in this region that essentially gets reverse biased under this operating condition.



(a) (b)

Figure 3.17 Electron concentration at V_{GS} = 1 V (on-state) and V_{DS} = 28 V (a) HFET with Field Plate (b) PSJ HFET



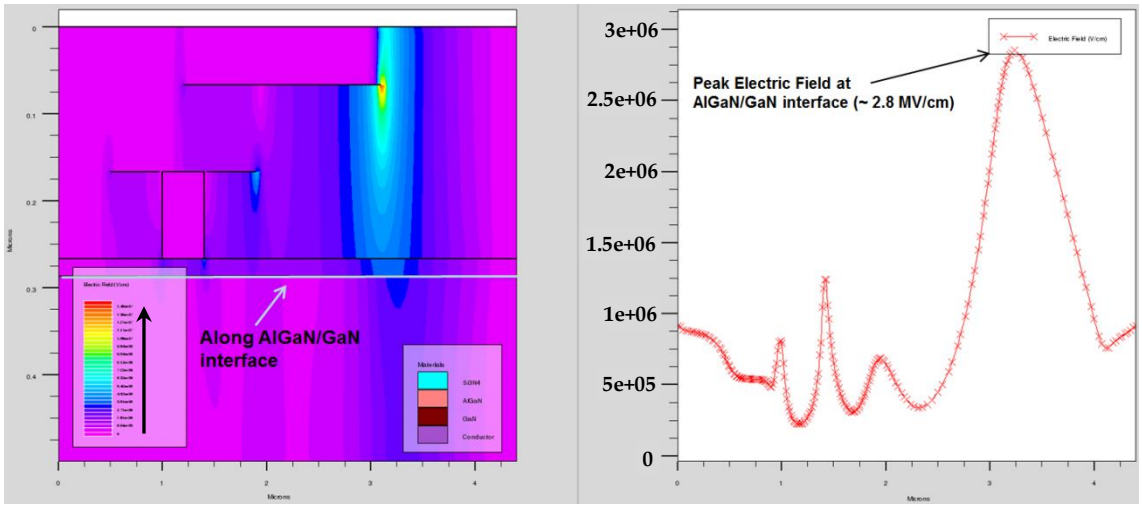
(a) (b)

Figure 3.18 The profile of electron concentration and potential along the AlGaN/GaN interface at V_{GS} = 0 V (on-state) and V_{DS} = 28 V (a) HFET with Field Plate (b) PSJ HFET

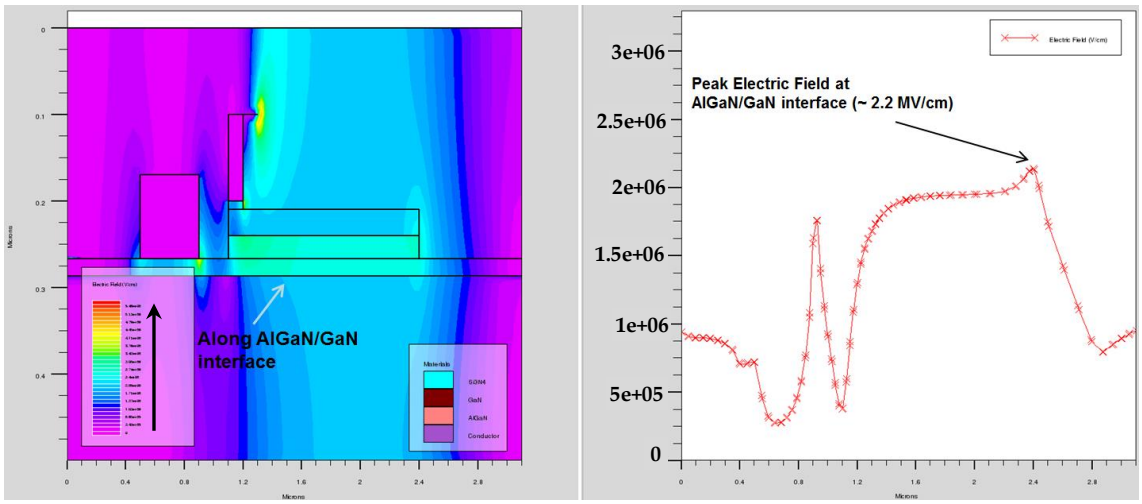
As most of the Drain-Source potential (V_{DS}) drops along the PSJ region, the magnitude of depleted electrons at the drain-side edge of the Gate is not as much as observed for FP HFET. In both FP HFET and PSJ HFET, as V_{GS} is increased, electrons previously depleted due to pinch-off are replenished under

the drain-side edge of the Gate electrode. When all the depleted electrons during pinch-off are replenished, the Drain Current saturates with any further increase in V_{GS}. In the case of PSJ HFETs, the electrons depleted in the PSJ region are not fully replenished and cannot be modulated by the Gate Voltage. The Drain Current saturation is therefore determined by this behaviour in PSJ HFETs.

The second objective of this simulation study was to verify the electric field profile within the two structures under off-state conditions. The physical models included for simulation of the off-state characteristics were – POLAR (Spontaneous Polarisation), CALC.STRAIN (Piezoelectric Polarisation), SRH (Shockley-Read-Hall, carrier generation-recombination), FERMI (Fermi-Dirac statistics), FLDMOB to model field dependent electron mobility, and IMPACT SELB (Selberherr impact ionisation model for simulating avalanche breakdown) [9]. The distribution of the electric field and its profile along the AlGaN/GaN interface at V_{GS} = -10 V and V_{DS} = 300 V has been illustrated in Fig. 3.19 (a) and (b) for FP HFET and PSJ HFET respectively. A non-uniform electric field distribution is apparent in the FP HFET with the highest peak value of 2.8 MV/cm along the AlGaN/GaN interface, located at the drain-side edge of the source-connected field plate. Whereas, in the case of the PSJ HFET, a box-like electric field distribution is observed in the PSJ region because of the inherent charge compensation effects of the polarisation charges within the structure. A peak value of 2.2 MV/cm is observed in the electric field along the bottom AlGaN/GaN interface. The peak is located at the drain-side edge of the double heterostructure suggesting that further increase in the drain voltage will make the edge more susceptible to breakdown. As performed in conventional field-plated structures, introduction of a Drain FP can potentially ease the electric field crowding at that location.



(a)



(b)

Figure 3.19 The distribution of electric field and its profile along the AlGaN/GaN interface at V_{GS} = -10V (off-state) and V_{DS} = 300 V (a) HFET with Field Plate (b) PSJ HFET

PSJ GaN devices are promising candidates for next generation ultra-low loss high voltage power devices performing beyond the GaN material limit. As lateral devices, they are ideally suited for ultra-high efficiency power ICs with small chip size. The natural course in the evolution of this technology was to scale up from Proof of Concept device test structures to large area devices to understand the challenges to scalability and also effectively evaluate the high-power performance capability of this technology. The next section covers the critical groundwork performed on this front of research and development in PSJ GaN technology.

3.3 Device Design and Approach to Scalability

Proof of Concept HFETs and Schottky Barrier Diodes (SBD) based on PSJ were demonstrated in 2011 at the University of Sheffield, and a detailed schematic of the basic design is shown in Fig. 3.20.

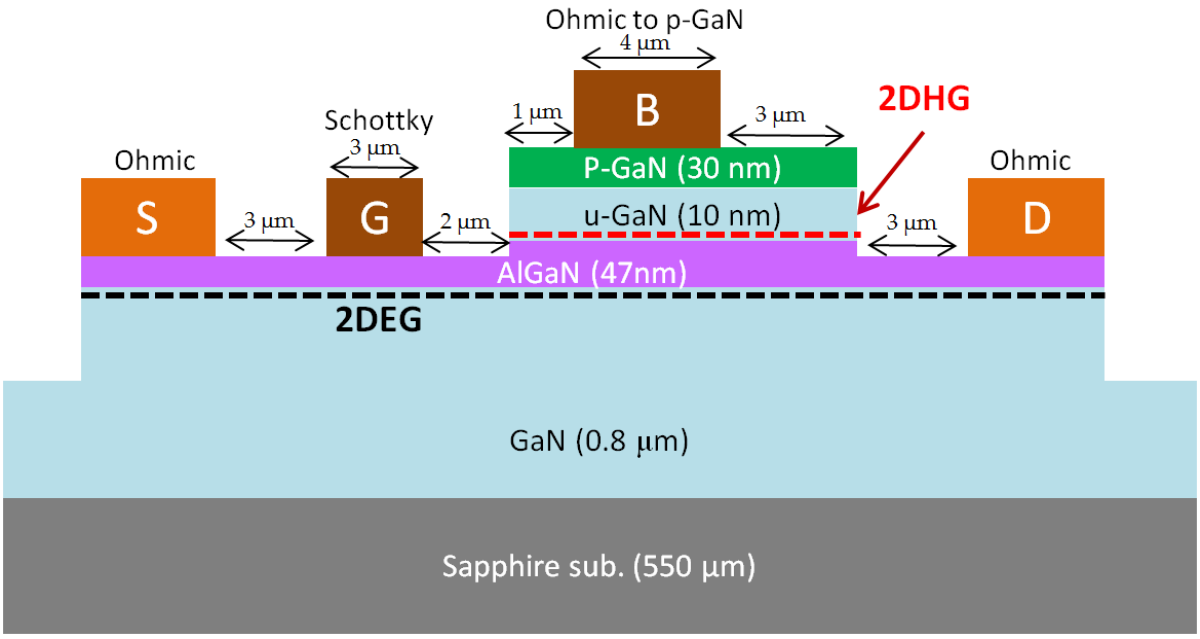


Figure 3.20 Schematic of the cross-section of PSJ HFET

The GaN/AlGaN/GaN double-heterostructure used for the initial work was grown by Metal Organic Chemical Vapour Deposition (MOCVD) on 3" Sapphire substrates at POWDEC KK, Japan. The epitaxial growth starts with a 0.8 µm thick undoped GaN layer (buffer) on a GaN nucleation layer. Subsequently, a 47-nm-thick undoped AlGaN layer with an Al composition of 23 %, a 10-nm-thick undoped GaN layer and a 30-nm-thick Mg doped (3×10^{19} cm^{-3}) p-GaN layer were grown. 2DHG and 2DEG are formed at the upper GaN/AlGaN and bottom AlGaN/GaN interfaces respectively and their sheet densities were 1.1×10^{13} and 9.7×10^{12} cm^{-2} respectively as determined by Hall Effect measurements at room temperature [4].

The device processing began with time-controlled etching of the upper GaN layers of the heterostructure well into the GaN buffer layer for device isolation,

followed by controlled etching of the top layers (p-GaN, u-GaN, and ~ 25 nm of the AlGaN layer) to define the PSJ mesa and access regions. The Source and Drain ohmic electrodes (Ti/Al/Ti/Au) were then deposited on the etched AlGaN surface and annealed under N_2 ambient at 800 °C. During annealing, nitride forming metals such as Ti and Al undergo metallurgical reactions resulting in the formation of interfacial nitrides (for e.g. TiN, AlN or $AlTi_2N$) as well as inter-diffusion between metals resulting in the formation of low resistance Ti–Al and Au_2Al compounds. It is the formation of TiN that reduces the effective barrier height and creation of N deficient AlGaN region at the interface that in turn is believed to form heavily n-doped region, are considered responsible for the formation of ohmic contacts [10,11]. The gate and base electrodes were formed using Ni/Au on the AlGaN and p-GaN layers, respectively and annealed in air at 550 °C to decrease the contact resistance of the base electrode. Finally, a 160-nm thick SiO_2 layer deposited by plasma enhanced chemical vapor deposition (PECVD) system was used as the passivation layer. The Source-Gate distance, the Gate length and the Gate-Drain distance were 3 μm, 3 μm and 13 μm respectively. Output characteristics of the device which that had a width of 50 μm, indicated a Drain Current of ~ 100 mA/mm at V_{DS} = 1 V with an off-state Breakdown voltage (*BV*) of ~ 700 V [4].

3.3.1 Design Objectives

The main design objectives for the high power PSJ devices (Diodes and Transistors) were defined as mentioned below:

1. Off-state Breakdown/Reverse blocking voltage: 1200 V, to be achieved by optimising the drift length based on previously fabricated Proof of Concept devices.

2. Current Capability: Devices rated up to 5A, to be achieved by effectively widening the active area of the devices by employing suitable layout schemes for wide periphery devices.

3.3.2 Layout schemes

Two main widely adopted schemes for large area devices were identified

1. Serpentine-Gate Layout

   A schematic of a typical large area power GaN HFET employing Serpentine–Gate layout is shown in Fig. 3.21. The Gate fingers are laid out such that they serpentine around the Drain and Source fingers/electrodes. Pads for wire bonding are formed above and below the active area.

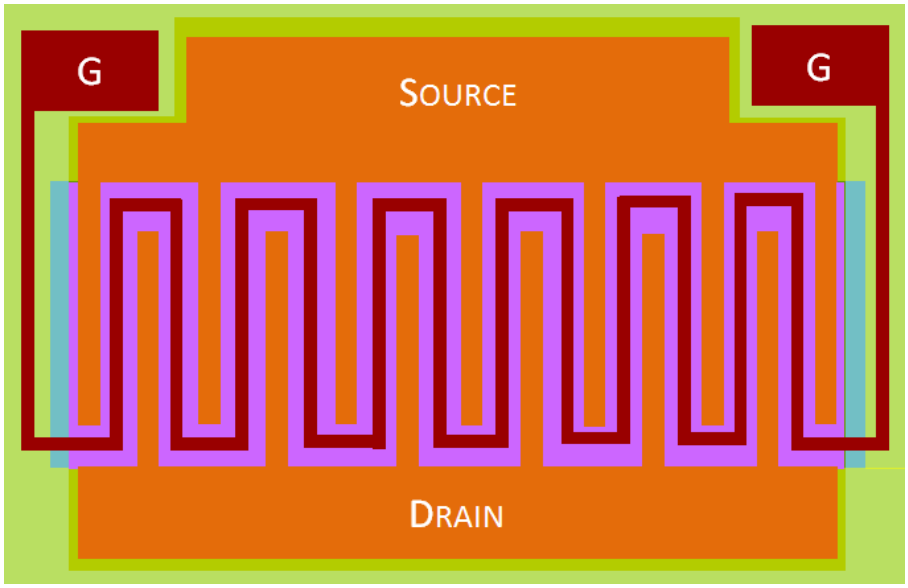


Figure 3.21 (a) Schematic of a high power GaN HFET with Serpentine-Gate layout [12]

2. Multi-finger Layout

   A typical large area GaN HFET employing multi-finger layout is shown in Fig. 3.22. The general layout of terminal pads is similar to that in a Serpentine-Gate layout. All fingers/electrodes (Gate, Source and Drain) are laid out in the same fashion; hence the layout scheme is often referred to as multi-finger. Gate and Source pads are on the same side and Drain pad is on

the opposite side. Metal electrodes extend from each pad to the device active area.

Inevitably in such a layout, there would be some region with an overlap of the gate and source electrodes. Air-bridges are sometimes employed in order to maintain isolation of the Gate and Source electrodes, and to ensure continuity of contact from Source or Drain pads to the corresponding fingers/electrodes in the active area of the device.

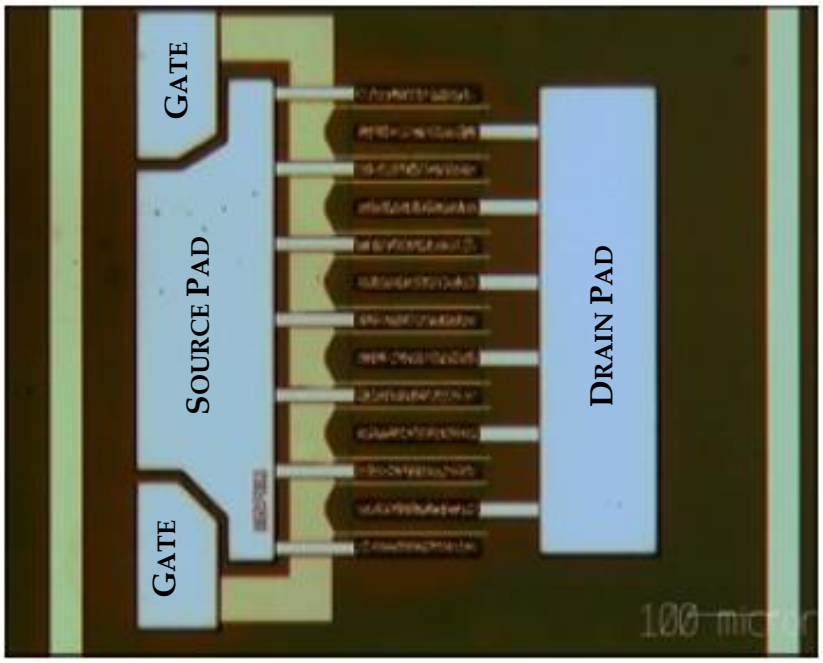


Figure 3.22 High power GaN HFET with a Multi-Finger Layout [13]

3.3.3 Device design of High power PSJ devices

After identifying possible layout schemes, the next task was to design high power PSJ devices (diodes and transistors). Schematic of the Proof of Concept (PoC) PSJ HFET and the design parameters that were used as reference are shown in Fig. 3.20. The target was to incorporate the necessary changes to enhance the breakdown voltage and current handling capability of the device.

Off-state Breakdown Voltage/Reverse Blocking Voltage

This was the first step in the design of high power PSJ device design. The Off-state Breakdown Voltage/Reverse Blocking Voltage of the devices was targeted to be 1200V. Characterisation results from the PoC devices previously fabricated on Sapphire substrates were relied on at this stage. Considering that the voltage sustained by the device in off-state or when under reverse bias is primarily determined by the PSJ layer drift length (Drain-side edge of Base electrode to edge of the mesa), 15 μm was identified as suitable to withstand ~ 1500 V (considering an average breakdown field strength of 1 MV/cm) giving more than 20% margin on the target operating voltage of the devices. All high power PSJ devices were designed based on this criterion.

Current handling capability

The primary challenge in this stage of the design was to determine appropriate conducting material and sizing (width, length and thickness) of the Drain and Source (Anode and Cathode) electrodes in the active area to have sufficient current handling capability, and also ensuring uniform distribution of the current in the active area during conduction.

A key attribute that was considered right from the beginning was emphasis on reliability of metallisation along with functionality of devices. It is fairly well established that Gold (Au) interconnects in integrated circuits have a much better median time to failure compared to alternatives like Aluminium (Al). Electromigration is a typical failure mode in metal traces that depends on the chosen material, geometry, current density, current levels, metal deposition techniques, underlying layers, overlying layers as well as operating temperature of the metallic conductor films [14-16]. S. Kilgore et al. [16] have reported about activation of electromigration in electroplated Au interconnects

when operated at current density of 2.0 MA/cm^2 with ambient temperatures ranging from 325 °C to 375 °C.

Although there are multiple parameters which could impact the reliability performance of metal electrodes, a conservative current density of 250 kA/cm^2 was considered, to be well within the safe operating range.

The final factor that is critical to determine the sizing of the electrodes was the plurality of the individual device unit cells in combination with practically achievable metal thicknesses for the designed feature sizes of electrodes, during device fabrication.

Following assumptions were made in order to size the Drain/Source (Anode/Cathode) electrodes and to determine the plurality of cells to achieve the desired current ratings:

- Maximum electrode thickness achievable = 4 μm
- Maximum electrode width = 1500 μm
- Estimated Drain-Source Current density (normalised to Gate width) = 50 mA/mm at V_{DS} = 1 V
- Maximum operating current density for the metal electrode (Au) = 250 kA/ cm^2
- Specific contact resistance ~ 10^{-4} - 10^{-5} Ω.cm^2

Based on the estimation of normalised current density achievable in the device (50 mA/mm at V_{DS} = 1V), a current rating of 5A thus required an effective Gate width of 100 mm. With Gate/Drain/Source electrode width set at 1500 μm for each cell, there would be a requirement of 66 cells (100 mm ÷ 1500 μm) with 1 gate electrode per cell and each Drain/Source electrode shared by two cells, with all 66 cells effectively operating in parallel. The assumption is that the overall current in the device will be distributed uniformly amongst the cells.

Assuming that the total current (5A) splits equally amongst the cells required that each cell carried ~ 75 mA/cell. Each Drain/Source finger is shared by two cells, and they should therefore reliably be able to handle ~ 150 mA/electrode. Considering a maximum permissible current density of 250 kA/ cm^2 in the electrodes, Drain/Source electrode length has to be $\geq$ 15 μm for a deposited thickness of 4 μm. As PSJ HFET has an intrinsic PN diode with the p-region (2DHG) connected to the Base electrode and n-region (2DEG) connected to the Drain, which enables reverse conduction from Base to Drain, the Base electrode was also sized along the same lines to have sufficient current handling capability during reverse conduction.

Sizing of Terminal Pads

Pads for the various terminals were sized depending on the packaging approach and capability of the facility for assembly/packaging. For wire-bonding of Au wires at our facility, the diameter of wires was fixed at 250 μm (typically employed in wire-bonding of power electronic devices [17]). The recommended pad sizes are typically 2-3 times for wedge-bonding and 3-5 times for ball-bonding [18] mandating that the devices to be wire-bonded have a minimum pad width of 750 μm.

Another option for assembly that was considered was flip-chip packaging with gold stud bumping of the pads. In this approach, the dies are flipped and attached to patterned ceramic substrates or circuit boards by means of conductive bumps on the bond-pads of the dies. The main advantage of this approach is lower effective interconnection length when compared to wire-bonding which significantly minimises overall parasitic inductance in devices [19]. Such a packaging approach is extremely beneficial for GaN power transistors which although have the capability of switching at high voltage and current slew rates, the performance can be hampered with the presence of

intrinsic parasitic inductance of the device or those arising from the layout of circuits. The dimensions of pads for devices to be gold stud-bumped and flip-chip packaged were designed as 80 μm x 80 μm, based on the specifications received from the facility where packaging of the devices was planned to be undertaken.

3.4 Process-Flow Optimisation/Development

After suitable layouts were identified and basic high power device design parameters determined, the next task was two-fold: Process Optimisation/Development and Mask Design which incorporated the process changes in the various layouts of the high power devices. This task involved the following:

- Inclusion of an insulation layer under all metal pads, to minimise any additional contribution of leakage currents through the pad regions
- Mutually exclusive deposition of Gate and Base electrodes, so that Base metallisation and annealing could be performed before and independent of Gate contact deposition. In the existing process-flow, Gate and Base contact formation was being attempted in a single step of depositing Ni/Au (20 nm/200 nm, followed by annealing). Although, this change in the process-flow leads to an additional step as well as a new mask, this was crucial to ensure that high temperature annealing for formation of p-type ohmic contact for the Base electrode had no impact on the quality of the Gate Schottky contact. Secondly, a good p-type ohmic contact requires a metal stack of a different composition compared to the metal stack required to form a Schottky contact.
- Optimisation of base p-contact metallisation and Rapid Thermal Annealing (RTA) conditions in order to achieve better p-type ohmic contact performance

- Inclusion of a dielectric deposition step post gate contact deposition to serve not only as surface passivation but also to ensure good isolation between Gate contact and overlying metal (second metal described in the next step) connecting Source to Base contact. The objective of intrinsically making this connection in PSJ HFETs was to realise the body diode essentially between Source and Drain terminals as incorporated in traditional Si Power MOSFETs.
- Via etch and a thick second metal deposition to ensure continuity from various terminal pads to metal electrodes/contacts in the active area of the device
    - The combination of the previous two steps is a novel approach to enhance the current handling capability of individual Source and Base electrodes and also keeping the electrode lengths with in practical values. This in turn also ensures that the overall die area and layout of the high power devices remained compact with a symmetrical/balanced form factor. This aspect will become more apparent in section 3.5 which discusses the approach to mask design in detail. The new approach also created some stringent device processing requirements at photolithography and etching as discussed in section 3.6 on device fabrication.
- Deposition of a final thick dielectric layer and pad opening. To make the individual Drain/Source/Base electrodes capable of high currents, it was essential to increase the thickness of these electrodes to 4 μm. This also required that the region between Drain and Source/Base electrodes was appropriately filled with a material of high dielectric strength and good insulation properties.

- Although the above-mentioned process changes were mentioned in the context of PSJ HFETs, the same changes were also accordingly applied to PSJ Diodes.

The overall process-flow for fabrication of high power PSJ HFET and the schematics of the device cross-section and layout of a large area PSJ HFET (Serpentine-Gate) after each step has been included in Appendix-1.

The device cross-section and layout as obtained at the end of the process have been shown in Fig. 3.23.

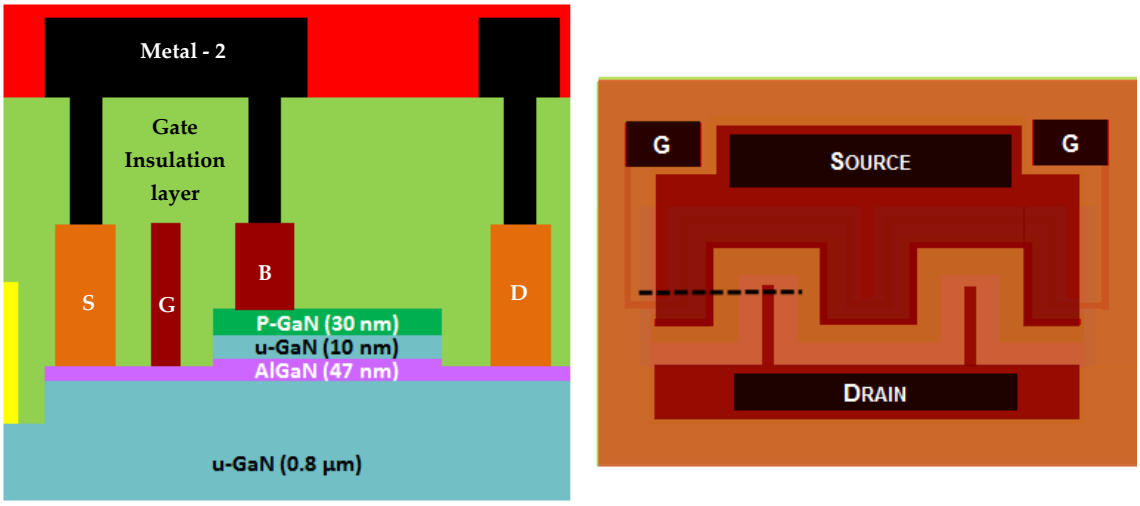


Figure 3.23 Simplified schematics of the cross-section and layout of large area PSJ HFET (Serpentine-Gate)

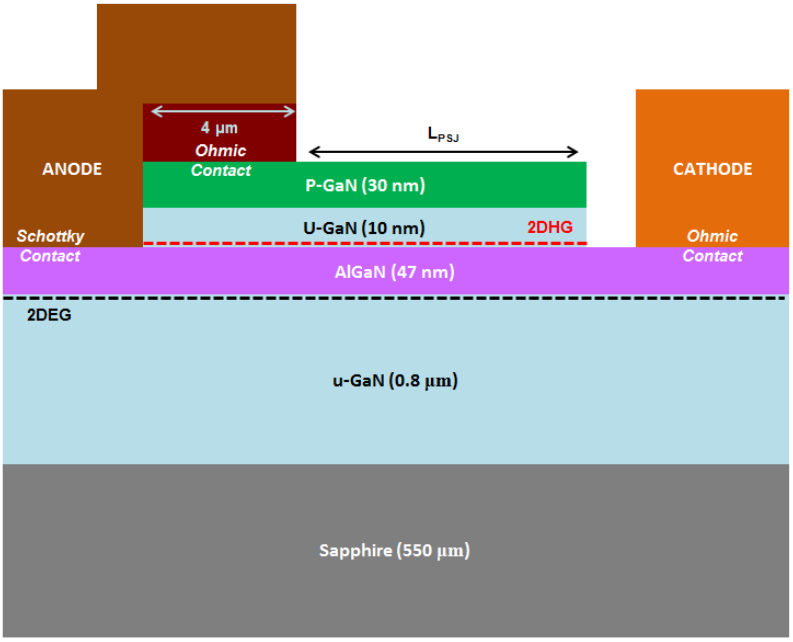
3.5 Mask Design

The following PSJ device test structures were selected to be scaled-up for higher power ratings

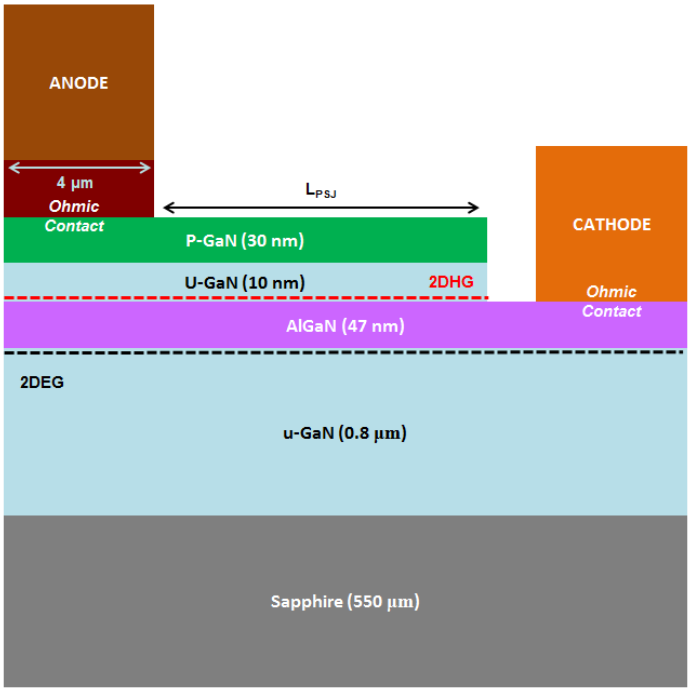
1. HFET (as shown in Fig. 3.20)
2. Hybrid/PSJ Diode (as shown in Fig. 3.24(a))
3. PN Diode (as shown in Fig. 3.24 (b))

Development of the process-flow and definition of basic device design parameters paved the way forward for mask design. Based on the new process-flow, ten masks were required for device fabrication.

Mask design activity begins with the definition of mask alignment sequence as that has a direct impact on the misalignment in patterning that could be tolerated during photolithography, without compromising the integrity of the design.



(a)



(b)

Figure 3.24 Schematics of (a) PSJ Diode (b) PN Diode

The minimum feature size achievable was identified as ± 1 μm for contact photolithography in the facility at Sheffield. The design rule for misalignment tolerance was set at ± 1.5 μm. A multi-level mask alignment sequence was chosen and the details have been described in Appendix-1.

The layout of the masks for the large area devices was carried out by Dr. Mark Sweet at the University of Sheffield. The layouts for some of the scaled-up devices have been shown in Fig. 3.25. Masks for devices (Diodes and HFETs) at other current ratings (1.7A (width=33.6 mm), 2.5A (width=50.4 mm), 5A (width=100.8 mm)) were also designed following a multi-finger layout approach. The design had taken into consideration the packaging aspects of gold stud-bumping and flip-chip packaging of most of the devices, except for the large area PSJ HFETs based on Serpentine-Gate layout where the layout was customised for wire-bonding.

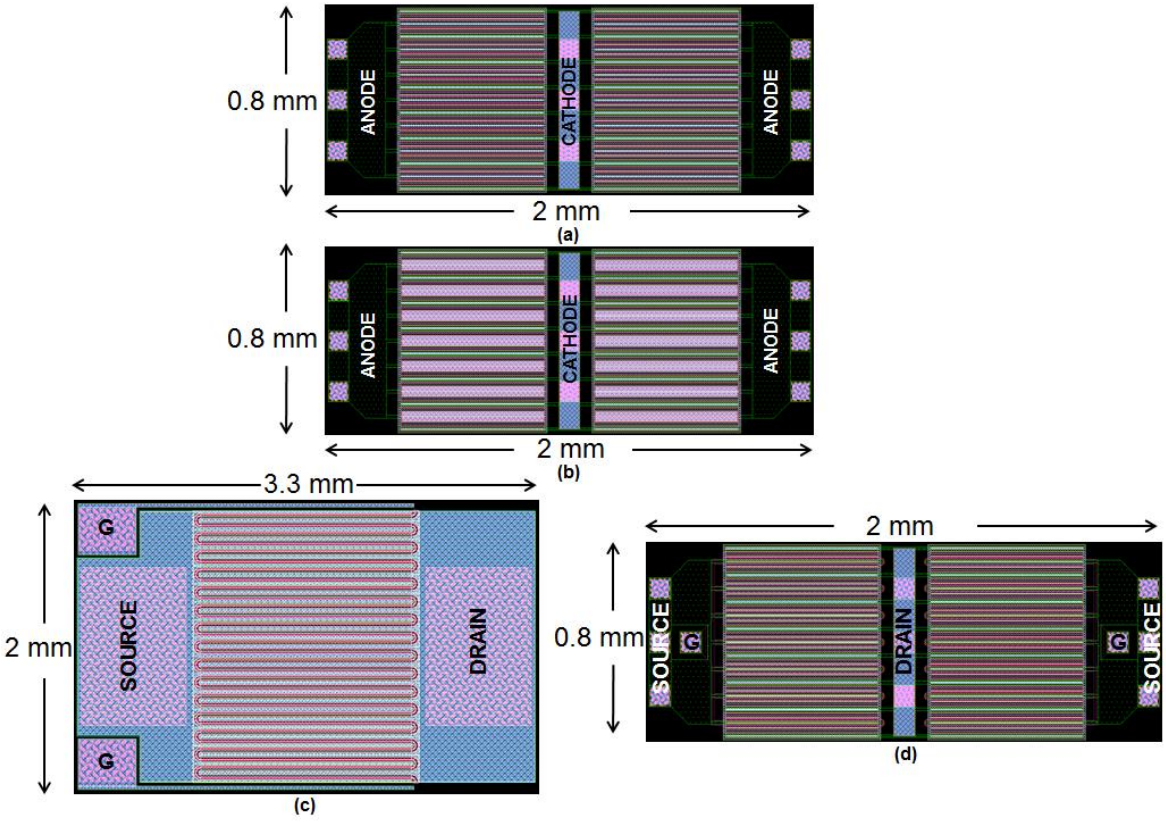


Figure 3.25 Mask layouts (a) 0.85 A rated PSJ Diode (width=16.8 mm) (b) 0.85A rated PN Diode (width=16.8 mm) (c) 2.2 A rated HFET (width = 45 mm, Serpentine gate layout) (d) 0.85A rated PSJ HFET (width= 16.8 mm)

3.5.1 Device and Process Test structures

The existing device and process test structures were modified incorporating the new process flow and misalignment tolerance into consideration. Device test structures included Schottky Barrier diode, Conventional HFETs, PSJ Diodes, PSJ HFETs and PSJ Bidirectional HFETs. A few of the new PSJ device test structures included are as shown in Fig. 3.26.

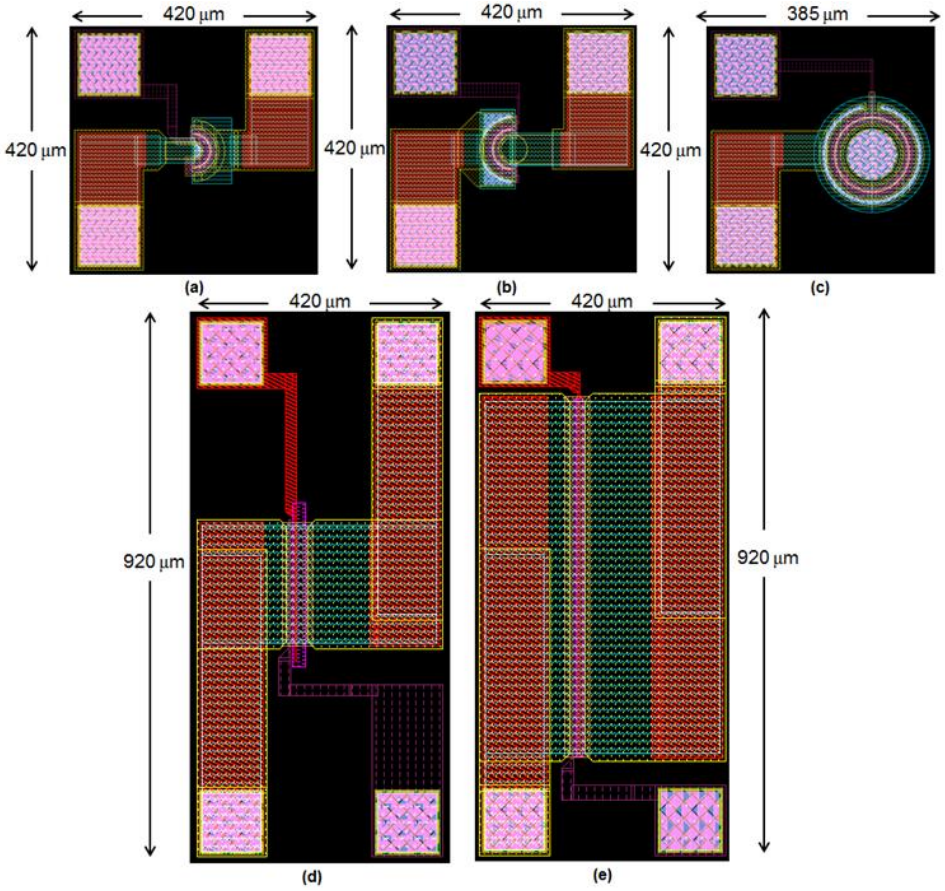
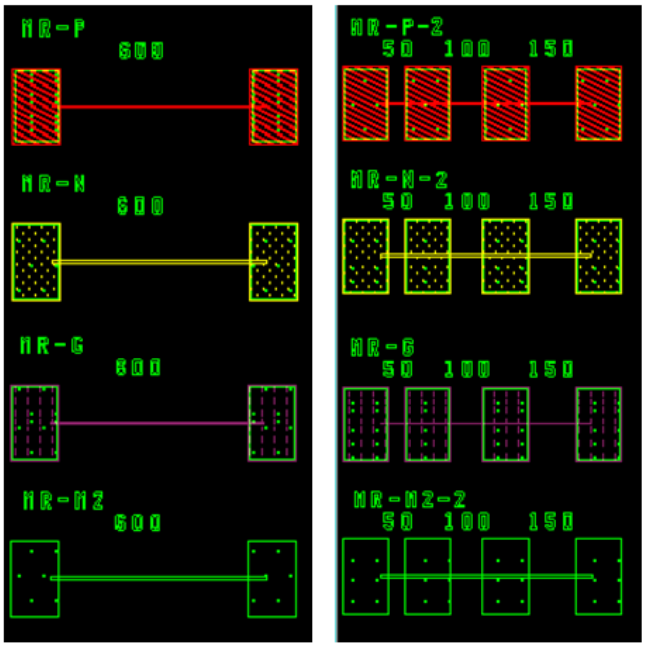


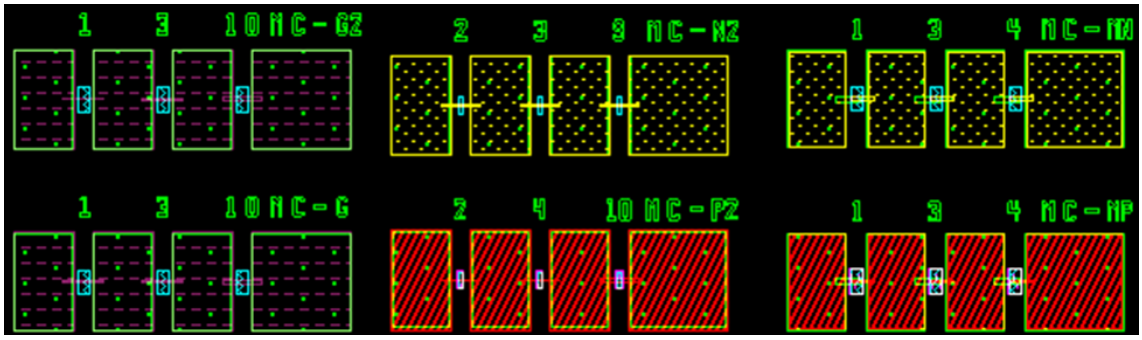
Figure 3.26 (a) Semi-circular Drain HFET (b) Semi-circular Source HFET (c) Circular HFET (d) Extended Gate HFET (Type-1) (e) Extended Gate HFET (Type-2)

Additional process test structures as shown in Fig. 3.27 were also included for evaluating the metal resistance of the fingers (MR for n-contact, p-contact and second metal/metal-2) as well as to evaluate metal continuity (MC). The objective of including new MR process test structures was to evaluate the impact of long metal fingers (for e.g. 600 µm in multi-finger devices) on the overall resistance of the devices. MC process test structures are required to

verify the continuity of metal traces as they traverse along varying surface topography in different regions of the devices (for e.g. etched/un-etched regions, mesa to etched regions to pad and so on). MC test structures were also designed for verifying continuity of second-metal to contacts on the active area through vias with feature size of 1 μm in certain regions, a very crucial aspect from the perspective of device functionality and performance of large area devices.



(a)



(b)

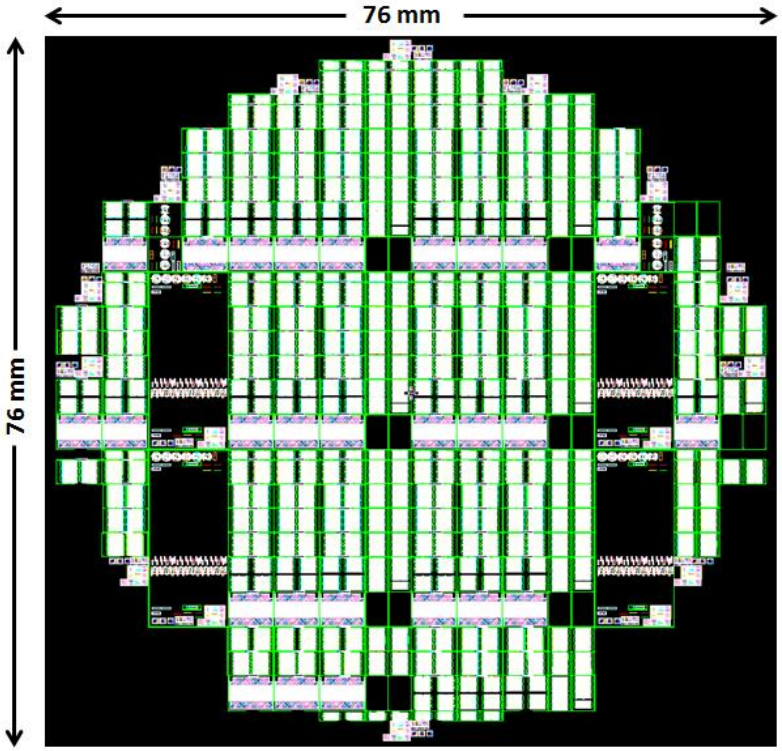
Figure 3.27 Additional Process Test Structures for evaluating (a) Metal Resistance (b) Metal Continuity

Other standard process test structures such as Transmission Line Method/Model (TLM) patterns for evaluating contact resistance of n-contact and p-contact, Capacitance Voltage (CV) structures, as well as those to verify thickness of deposited layers and etch depth were also included.

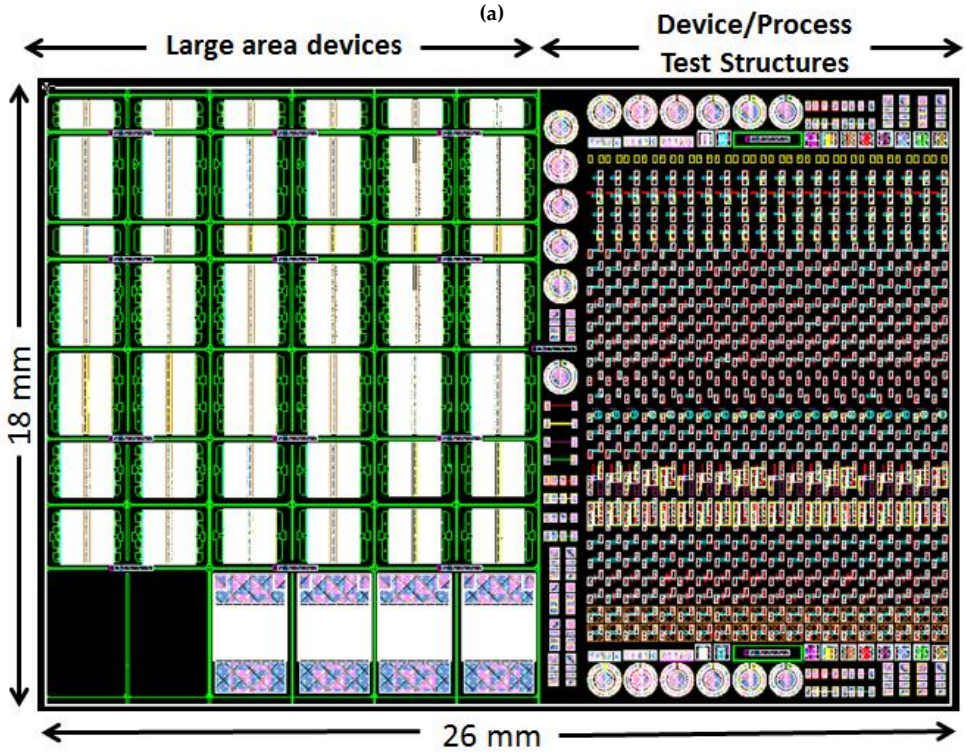
The undertaking of device fabrication was performed at two facilities namely, National Centre for III-V technologies at the University of Sheffield and at Southampton Nanofabrication Centre at the University of Southampton. Two separate sets of photomasks were designed and the differences in the masks were primarily considering the following aspects:

1. Wafer level (3″) processing at Southampton compared to cleaved unit level (size = 26 mm x 18 mm) processing at Sheffield
2. Devices with larger area and higher power ratings were included in the Masks for the Southampton batch considering the processing capability of their facility

The final photomask layouts (all mask layers) for processing at both locations are shown in Fig. 3.28.



(a)



(b)

Figure 3.28 Final photomask layouts (a) Southampton Process (b) Sheffield process

The list of large area devices included on the respective mask-sets also enumerating the area, effective device width and layout scheme adopted, has been summarised in Tables 3.1 (a)-(b) (PSJ length = 15 μm across all the large area devices).

Device Type	Layout	Effective Width	Die-Area
PSJ Diodes	Multifinger	16.8 mm	1.6 mm^2
		33.6 mm	3.2 mm^2
		50.4 mm	4.8 mm^2
		100.8 mm	10.8 mm^2
PN Diodes	Multifinger	16.8 mm	1.6 mm^2
		33.6 mm	3.2 mm^2
		50.4 mm	4.8 mm^2
		100.8 mm	10.8 mm^2
PSJ HFETs	Multifinger	16.8 mm	1.6 mm^2
		33.6 mm	3.2 mm^2
		50.4 mm	4.8 mm^2
		100.8 mm	10.8 mm^2
	Serpentine	100.0 mm	15.8 mm^2

(a)

Device Type	Layout	Effective Width	Die-Area
PSJ Diodes	Multifinger	16.8 mm	1.6 mm^2
		33.6 mm	3.2 mm^2
		50.4 mm	4.8 mm^2
PN Diodes	Multifinger	16.8 mm	1.6 mm^2
		33.6 mm	3.2 mm^2
		50.4 mm	4.8 mm^2
PSJ HFETs	Multifinger	16.8 mm	1.6 mm^2
		33.6 mm	3.2 mm^2
		50.4 mm	4.8 mm^2
	Serpentine	45.0 mm	7.0 mm^2

(b)

Table 3.1 List of large area devices (a) Southampton mask-set (b) Sheffield mask-set

3.6 Device Fabrication

This section will cover the unit processes as well as the process optimisation activities that were carried out during various stages of the device fabrication at Sheffield, will be presented.

3.6.1 Growth and Layer Structures

The GaN/AlGaN/GaN double-heterostructures were grown by metal organic chemical vapour deposition (MOCVD) on 3″ Sapphire substrates and 6H-SiC substrates (high resistivity ~ 10^5 Ω.cm) at POWDEC, Japan. The epitaxial growth starts with a 0.8 μm thick undoped GaN layer on a GaN nucleation layer for sapphire substrates and AlN nucleation layer for 6H-SiC substrates. The basic structural details of the processed epitaxial wafers used in this study have been summarised in Table 3.2.

Wafer	**GaN (Buffer)**	**$Al_{0.23}Ga_{0.77}N$ (Barrier)**	**GaN (Cap)**	**p-GaN**	**2DEG R_{SHEET} (Ω/sq.)**	**Device Processing Facility**
GaN-on-SiC-1 (*Sheff.*)	800 nm	47 nm	10 nm	30 nm	525	Sheffield
GaN-on-SiC-2 (*Sheff.*)	800 nm	47 nm	10 nm	30 nm	525	Sheffield
GaN-on-SiC-1 (*S'ton*)	800 nm	47 nm	10 nm	30 nm	516	Southampton
GaN-on-SiC-2 (*S'ton*)	800 nm	47 nm	20 nm	20 nm	564	Southampton
GaN-on-Sapph. (*S'ton*)	800 nm	47 nm	20 nm	20 nm	967	Southampton

Table 3.2 Processed wafers and basic details of the epitaxial structure

Hall measurements performed on one of the sister wafers from the same batch at POWDEC, Japan indicated a sheet resistance of ~ 2.56 x 10^5 Ω/sq for 2DHG.

3.6.2 Sample Preparation

The process begins with dicing of the 3″ wafers into smaller units of dimensions of 26 mm x 18 mm. The dimensions were set beforehand based on the unit size suitable for device processing and masks/reticles were designed considering these dimensions. The dicing was performed at Loadpoint Ltd., and 6 units could be diced out from a single 3″ wafer. Device fabrication was performed on such diced units. A dedicated wafer (PSJ GaN-on-Sapphire) had also been diced into much smaller units previously, which were used as test samples for process development and optimisation. After obtaining the diced unit, the first step in device fabrication is to ensure an ultra-clean surface devoid of particulate contaminants. In order the clean the GaN wafers, a 3 step cleaning procedure was employed.

3 step cleaning: The sample is dipped and gently stirred in the following order

1. n-Butyl Acetate (30 sec, on hot plate at 100 ^{0}C)
2. Acetone (30 sec)
3. Isopropyl Alcohol (IPA) (30 sec)
4. Sample is blow-dried using a N_2 gun
5. Sample is then inspected under the microscope and 3 step cleaning is repeated accordingly until a clean surface is obtained

This cleaning methodology was employed at all stages of device processing.

3.6.3 Contact Photolithography

This is one of the most critical steps in microelectronic fabrication as it determines the patterning on the wafers and the success of all subsequent steps such as etching and metallisation, is highly dependent on this step. The equipment used in Sheffield for contact photolithography is Karl Suss MJB3 UV300/UV400. The step begins with heating of sample on 100 ^{0}C hot plate for 1 min to evaporate any water vapour or to remove solvents remaining from the

preparatory cleaning steps from the surface of the sample. Photoresist (BPRS-100/BPRS-200 in this process) is then spun on the sample at a speed of 4000 rpm for 30 sec to ensure a uniform layer of photoresist. Spinning of an adhesion promoter like hexa-methyl-di-silazane (HMDS) prior to photoresist deposition is required if photoresist is being deposited on insulating layers like SiN or SiO_2. After completion of resist spinning step, the sample is then heated at 100 ^{0}C on a hot plate for 1 min to remove solvent from the photoresist and improve adhesion. The sample is then aligned under the mask and exposed subsequently. The exposure time depends on the equipment, layers on the sample, surface topography, and contact mechanism on the aligner (it has been observed that vacuum contact which is typically employed to obtain pattern transfer of fine features, tends to lengthen the exposure time). After exposure, the sample is developed in a 1:3 H_2O: PLSI developer solution for 1 min. An additional bake step to harden the photoresists is necessary if the subsequent step happens to be Hydrofluoric (HF) acid etching to prevent delamination of the photoresist during wet etching. When patterned for metallisation, oxygen descum step and sometimes HCL dip are typically employed after development before proceeding with metal deposition.

3.6.4 Inductively Coupled Plasma Etching

Inductively Coupled Plasma (ICP) etching is a widely used dry etching technique in microelectronic fabrication. Fast and well-controlled etch rates, vertical profile (anisotropy), high selectivity, uniformity over large area, low temperature processing and low material damage are some of the most desirable aspects of the etching process. ICP etching caters well to most of these requirements as it provides high ion density enabling fast etch rates, while allowing separate control of the ion energy, enabling an etch process that causes minimal material damage [20]. ICP etching at Sheffield is performed on Oxford PlasmaSystem100. The main gases used for GaN etching are Ar (4 sccm), Cl_2 (15

sccm) and $SiCl_4$ (1.5 sccm) and the etch recipes have been standardised. The ICP Power is set at 450 Watts and the RF power is varied depending on the etching requirements. Lower RF power is used for more controlled etching at lower etch rates. The chamber pressure is set at 4 mTorrs. During process optimisation trials, it was observed that ICP etch process/etch rate is sensitive to the following (at our facility):

- Prior etch process runs, before the designated process is run (for e.g., a previous user could have etched a material in the same equipment with a different set or combination of gases/plasma conditions and the same can have an impact on the chamber ambience and subsequent etch processes). Hence a preparation run of 20 mins is strongly recommended before processing any sample
- Formation of dust-like residual layers was observed on the Si carrier wafer used for samples during etching and appeared to have an impact on the next etch run even if the chamber condition remained intact. This can sometimes lead to inconsistency in etch rates from sample to sample even if they are processed consecutively, with etch rates increasing/decreasing for subsequent runs. Hence, it is strongly recommended that the carrier wafer be cleaned/replaced (if there is significant residue) before proceeding with the subsequent sample etch to maintain the overall etch ambience/conditions

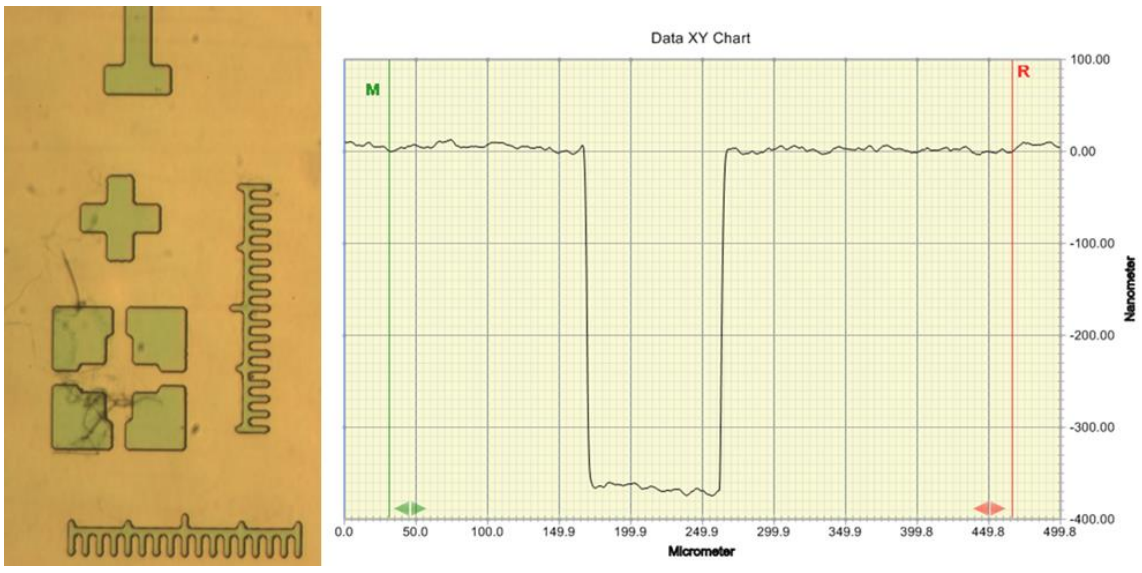
During device fabrication, ICP etching was used for Alignment mark definition, Isolation and Mesa etching steps.

Alignment Mark Etching

Alignment marks can be either deposited through metallisation or etched on the wafer surface. According to the mask sequence employed at Sheffield (as covered in section 3.5 and detailed in Appendix-1), initial set of alignment

marks were etched and the subsequent ones were defined using metal deposition.

The decision of using etching to define the initial alignment marks was made due to a requirement at the fabrication facility which forbade ICP etching of samples with any metal layers. Since the Isolation and Mesa etching on the samples were to be performed using ICP etching, the alignment marks for these stages had to be defined by etching. Etch-based definition of alignment marks involved extensive process development, as there were no prior data on the ideal etch depth required on the GaN samples which could provide the sharpness/resolution and contrast of the alignment features during mask alignment. Based on numerous test samples, a minimum etch depth of 350 - 400 nm was identified as the most suitable. Fig. 3.29 shows the etched alignment mark on a test sample with an etch depth of ~ 370-380 nm as indicated by Dektak surface profilometry.



(a) (b)

Figure 3.29 (a) Etched alignment mark (b) Surface profilometry graph

The RF power set was 150 Watts and etch time was set as 2.5 minutes. The etch rate obtained was ~ 150 nm/min. The same ICP etch conditions/settings were used for defining the alignment marks also on the actual samples.

Process optimisation for Isolation and Mesa Etching

A two-stage etch recipe was used for Isolation and Mesa etching. This is required, as controlled-etching can effectively only be achieved at low RF Power. A low RF power also minimises surface/crystal damage during etch, which is critical from the perspective of device performance. However, striking plasma at low RF power is difficult (if not impossible). Hence, the process is initiated at a relatively high RF power (stage-1) and subsequently switched to low power once Plasma is initiated and sustained (stage-2).

The recipe details (main parameters only) are as mentioned below:

Stage 1

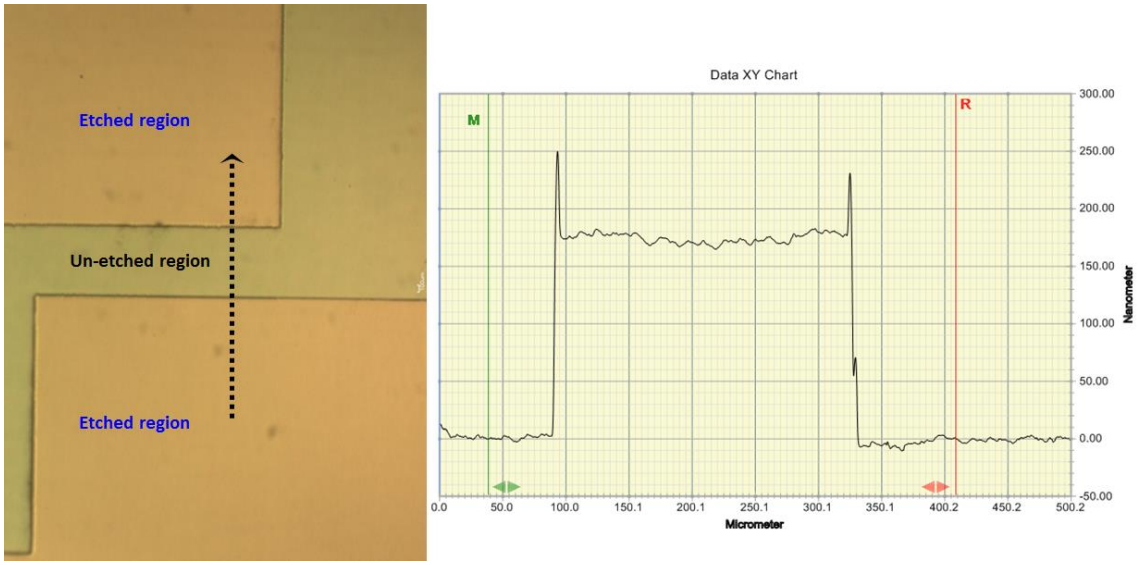
- RF Power : 80 Watts for 10 secs
- Strike Pressure (value in mTorr at which the RF power should turn on and strike the plasma) : 20
- Ramp (rate at which the pressure is reduced from the strike value to the set point) : 4

Stage 2

- RF Power : Starts at 80 Watts and is then switched (~ 2 secs later) to 10 Watts once plasma has been initiated
- Effectively, the etching takes place at RF Power of 10 Watts during this process

Several test samples (for e.g., as shown in Fig. 3.30) were run for process optimisation. Process variability was also identified during this stage and it was concluded that running test samples to verify the etch rate and processing the

actual device samples had to be performed at the same time to maintain consistency of the etch process.



(a) (b)

Figure 3.30 (a) Isolation etched feature on Test Sample-1 (b) Surface profilometry graph

The etch rates observed and etch depths achieved by varying etch time during optimisation runs and on actual device samples based on etch depth measurements using surface profilometry are as plotted in Fig. 3.31.

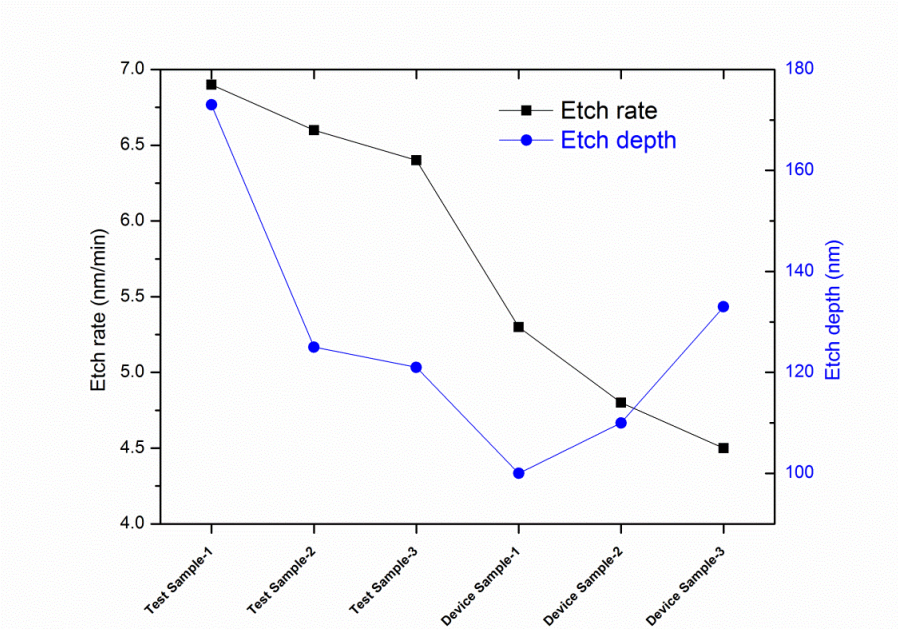


Figure 3.31 ICP Etch rate and etch depth variation during Isolation etch

The test samples were processed in a different time frame compared to the device samples which were processed consecutively but in a single session with no other perturbations. A large variation in etch rate was observed. During processing, the etch time for subsequent runs were modified based on the etch rate calculated for the previous run. The target isolation etch depth on device samples was 125 nm, but from perspective of functionality, an etch depth of more than 87 nm is sufficient. Target etch depth for Mesa etch was 65 nm and more critical in terms of etch control, as thickness of AlGaN layer that remained in the etched regions impacts 2DEG density as well as contact resistance of Drain/Source contacts. As the Schottky Gate/Anode contact is deposited on the etched surface of the AlGaN layer, the crystallographic damage during etching directly impacts Schottky leakage in the devices. GaN Test samples and the device samples were processed consecutively. The etch rates observed and etch depths achieved are as plotted in Fig. 3.32.

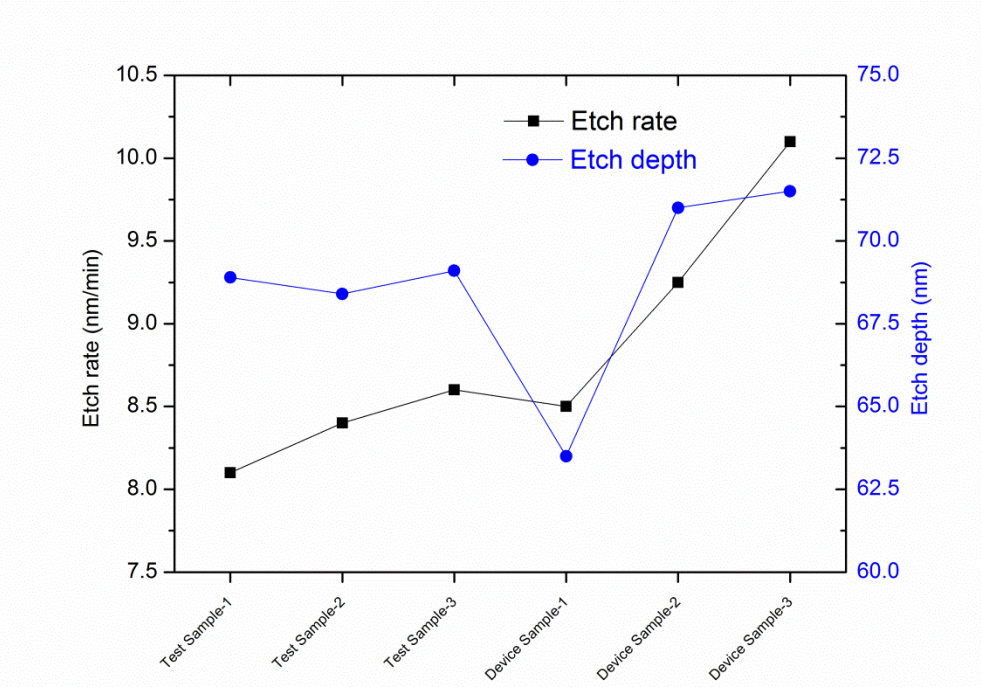


Figure 3.32 ICP Etch rate and etch depth variation during Mesa etch

Micrographs from one of the device samples (GaN-on-6H SiC substrate) at this stage have been shown in Fig. 3.33.

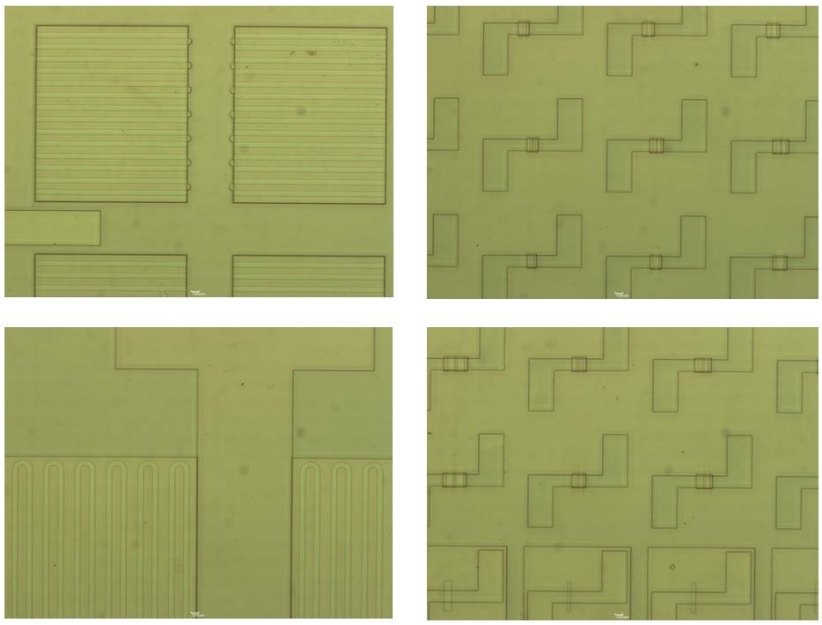


Figure 3.33 Micrographs from one of the device samples after Mesa etch

3.6.5 Plasma Enhanced Chemical Vapor Deposition and Ellipsometry

Plasma Enhanced Chemical Vapor Deposition (PECVD) is a process widely employed in microelectronic fabrication for deposition of thin films of various materials. The deposition is achieved by introducing the reactant gases between two parallel electrodes, one of which is grounded and the other is energised with RF power. Capacitive coupling takes place between the two electrodes and the reactant gases are excited into a plasma state. This initiates the chemical reaction between the gases resulting in the product of the reaction being deposited on the substrate placed on the grounded electrode.

Ellipsometry is a technique used to measure thickness of the deposited film. An ellipsometer measures the change in polarisation as light is transmitted or reflected from a material structure. As the measured response depends on optical properties and thickness of constituent materials, this technique enables determination of film thickness as well as optical constants [21]. Calibrated

recipes for estimation of thickness and refractive index of the deposited layer are typically available on the instrument for a given combination of structures such as SiN or SiO_2 deposited on Si substrates.

PECVD is employed in the process-flow for deposition of pad insulation (SiN), gate insulation/passivation (SiN). Reference deposition rates for various materials are usually available for PECVD depending on the recipe that is used. But the deposition rates can vary over time. Therefore, the recommended approach is to use clean Si test samples to verify and optimise the deposition time for the required thickness of the layer to be deposited based on ellipsometry measurements. As precise measurement of deposited film thickness requires a flat topography on the samples, it is difficult to obtain accurate measurements on processed samples with varying surface topography. Therefore, Si test samples were placed along with actual GaN device samples in the chamber during PECVD, which were then used for estimation of thickness of the deposited layer on the GaN device samples.

3.6.6 Wet Etching

Wet etching in the process-flow was only used for etching the SiN layer (150 nm) deposited during the pad insulation step. Buffered HF (10%) is used as the etchant. The buffered HF etching was carried out by Dr. Ken Kennedy from the EPSRC National Centre for III-V technologies at Sheffield. It is extremely critical that HMDS is used as a primer before photoresist deposition followed by a soft bake on a hot plate at 100 ^{0}C for 5 minutes, else there is risk of delamination of the photoresist due to insufficient photoresist adhesion during etching and this can damage the sample. Test samples were used to evaluate the wet etching process and etch time of 5 mins was identified as optimum. Lateral over-etch as inspected/estimated by optical microscopy was < 2 μm as shown in Fig. 3.34, and was acceptable based on the design specifications.

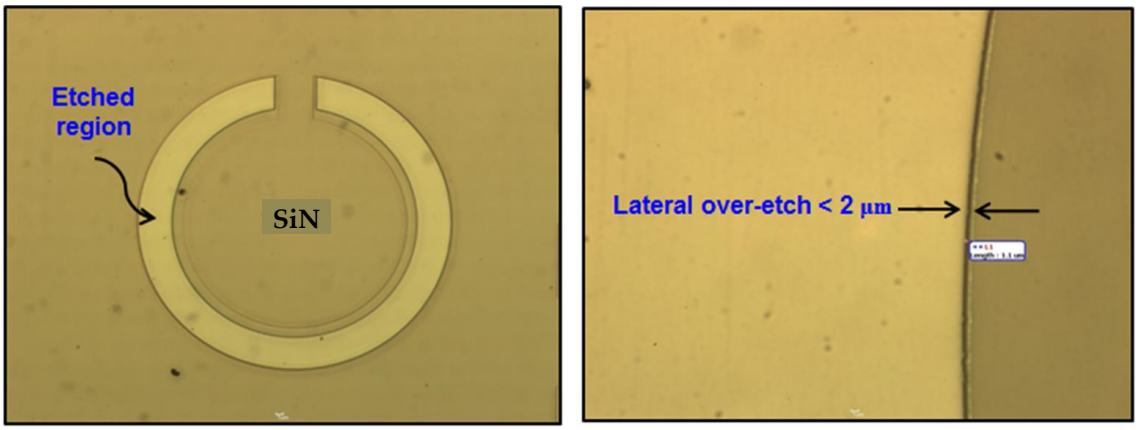


Figure 3.34 Optical micrographs of (a) HF wet-etched pattern (b) Zoomed in region showing the lateral over-etch

Once the deposited thickness has been estimated from ellipsometry measurement, it can be compared with the etched depth obtained by surface profilometry which can be used as a re-confirmation on the success of the wet etching step. Fig. 3.35 shows the results of surface profilometry indicating an etch depth of ~ 158 nm on a sample with a deposited SiN film with thickness ~ 150 nm (based on ellipsometry results of Si test sample that had been processed along with the device sample). Both results (profilometry/ellipsometry) can only be used for reference as the measurement accuracy for both techniques could vary, so can the location where the measurement is taken on the samples.

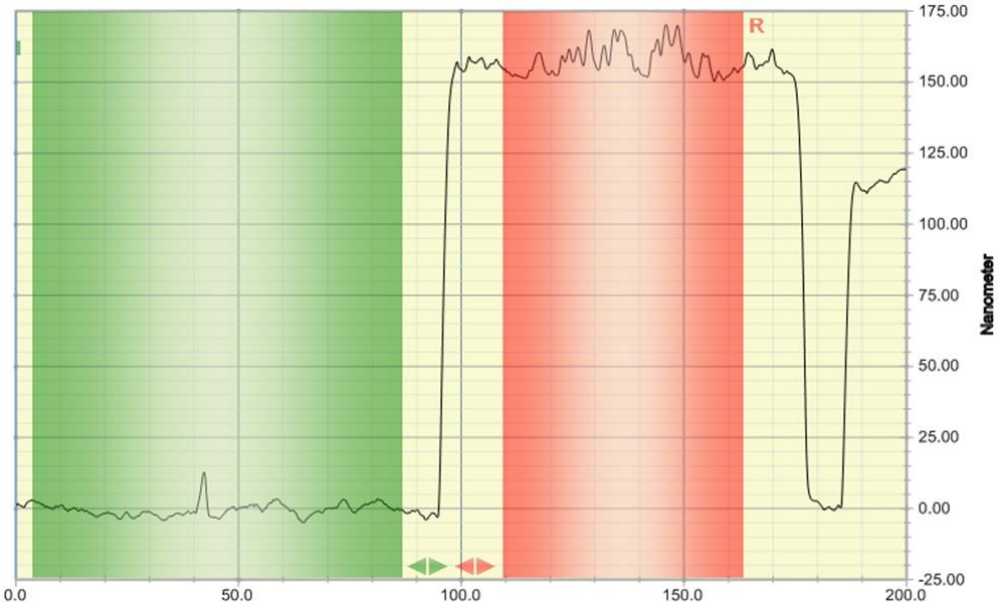


Figure 3.35 Surface profilometry graph of HF etched pattern

3.6.7 Thermal Evaporation and Metal Lift-off

Thermal evaporation and Metal Lift-off are extensively employed techniques for metallisation in microelectronic fabrication especially for III-V semiconductor technologies. These technologies typically require stacks of metals (Ti, Al, Ni, Au...) for formation of contacts. Such stacks are difficult to etch and this issue is circumvented using Lift-off [22]. The basic methodology of thermal evaporation involves the following main steps:

1. Tungsten coils in which source metals are placed during thermal evaporation are initially fired-off at a current > 30A or at a level expected to be used eventually to evaporate the source metal, whichever is higher for approximately a minute. This step helps in evaporating any pre-existing particulate matter/impurities on the coils.
2. The coils and source metal to be evaporated are cleaned in boiling n-butyl acetate for two minutes to remove any organic contaminants.
3. The coils, source metal and the patterned samples are then loaded into the evaporator chamber and the chamber is pumped down to vacuum (Pressure ~ 2-4 x 10^{-6} mTorr). If post-patterning, there are no exposed regions with metal, the sample is dipped in HCl:H_2O (1:1) solution for 30 seconds, rinsed in de-ionised water, blow-dried and then placed in the chamber. This step aids removal of any native oxides at the surface of the semiconductor. The thermal evaporator (Edwards Coating System E306A) used during device fabrication is shown in Fig. 3.36. The bell jar as shown in the figure has been coated with Ti from the evaporation step.

Figure 3.36 Thermal Evaporator - Edwards Coating System E306A

4. Depending on the stack of metals to be deposited, the source metals are placed in the respective coils. The quantity of source metal is measured in advance, as the quantity directly correlates with the thickness of the deposited metal.
5. The respective coil is then heated by gradually increasing the current until the metal begins to melt and evaporate. The metals used in the process flow (Ti, Al, Ni, Au) typically melt at current levels in the range of 20 - 30 A. Thickness of the evaporated metal can also be monitored using a quartz crystal. However, care was also taken by loading the appropriate quantity of the source metal based on calibration charts correlating quantity with thickness of the deposited layers. The deposition rate was typically maintained at 0.4 - 0.5 nm/min.

As thermal evaporation leads to a blanket deposition of the metal, the samples are patterned with photoresist prior to loading into the evaporator chamber. The photoresist is chosen such that post-resist spinning on the sample, it has a thickness of at least 1.5 to 2 times that of the intended thickness for metal deposition to facilitate a smooth metal Lift-off.

A typical Lift-off process has been illustrated through simple schematics in Fig. 3.37. Post evaporation, the sample is left in Acetone for approximately 10-12 hours. Metal lift-off is achieved by dissolution of the photoresist by Acetone. Thermal Evaporation was used for metallisation of Source, Drain/Cathode (n-contact) and Base ohmic contacts (p-contact), Gate/Anode contact (Schottky) as well as for deposition of second metal in the process flow. Micrographs from one of the device samples (GaN-on-6H-SiC) after n-contact Metal Lift-off have been shown in Fig. 3.38.

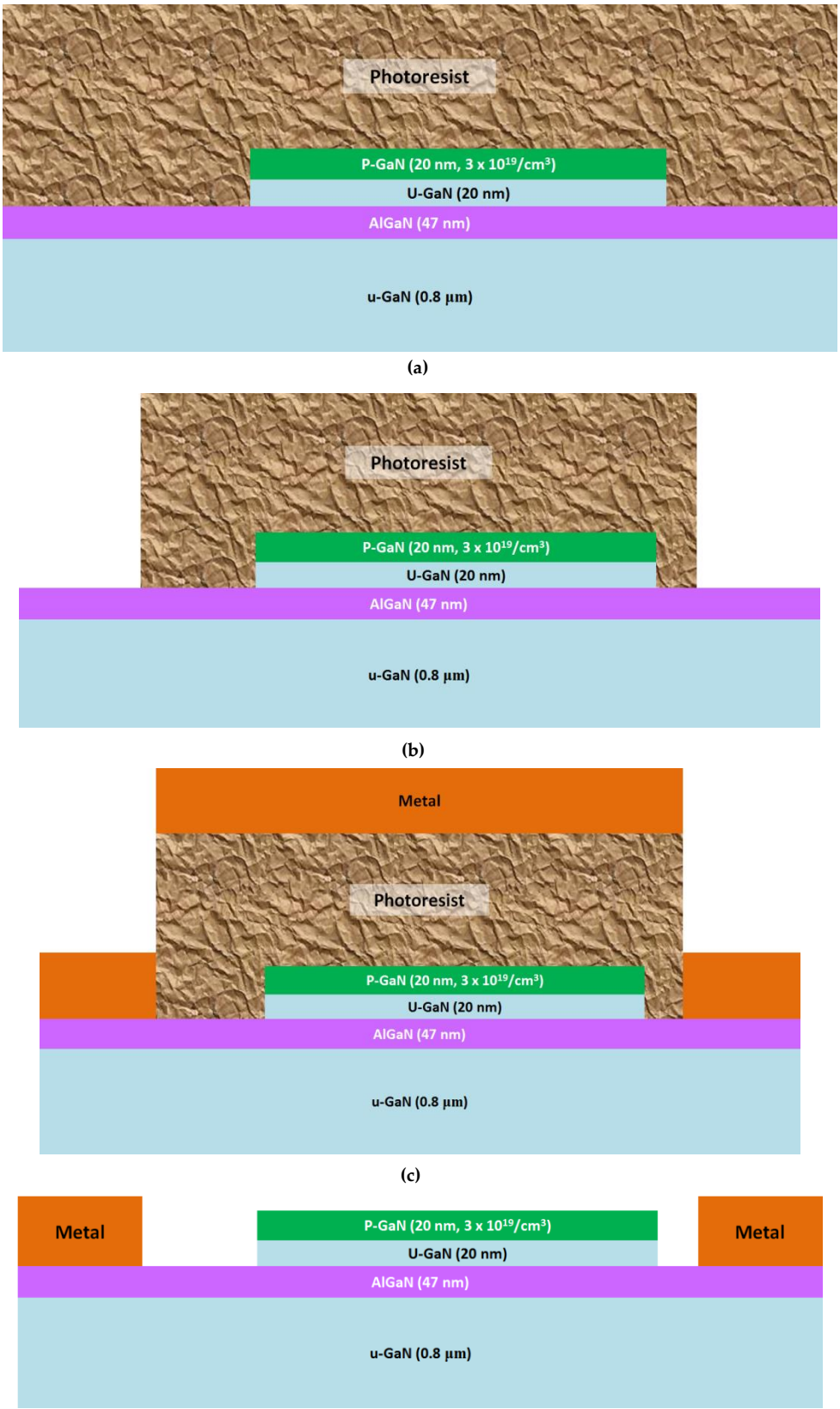


Figure 3.37 A schematic illustration of a typical Lift-off process (a) Deposition of photoresist (b) Photoresist-patterning (c) Evaporation of metal (d) Post Lift-off in Acetone

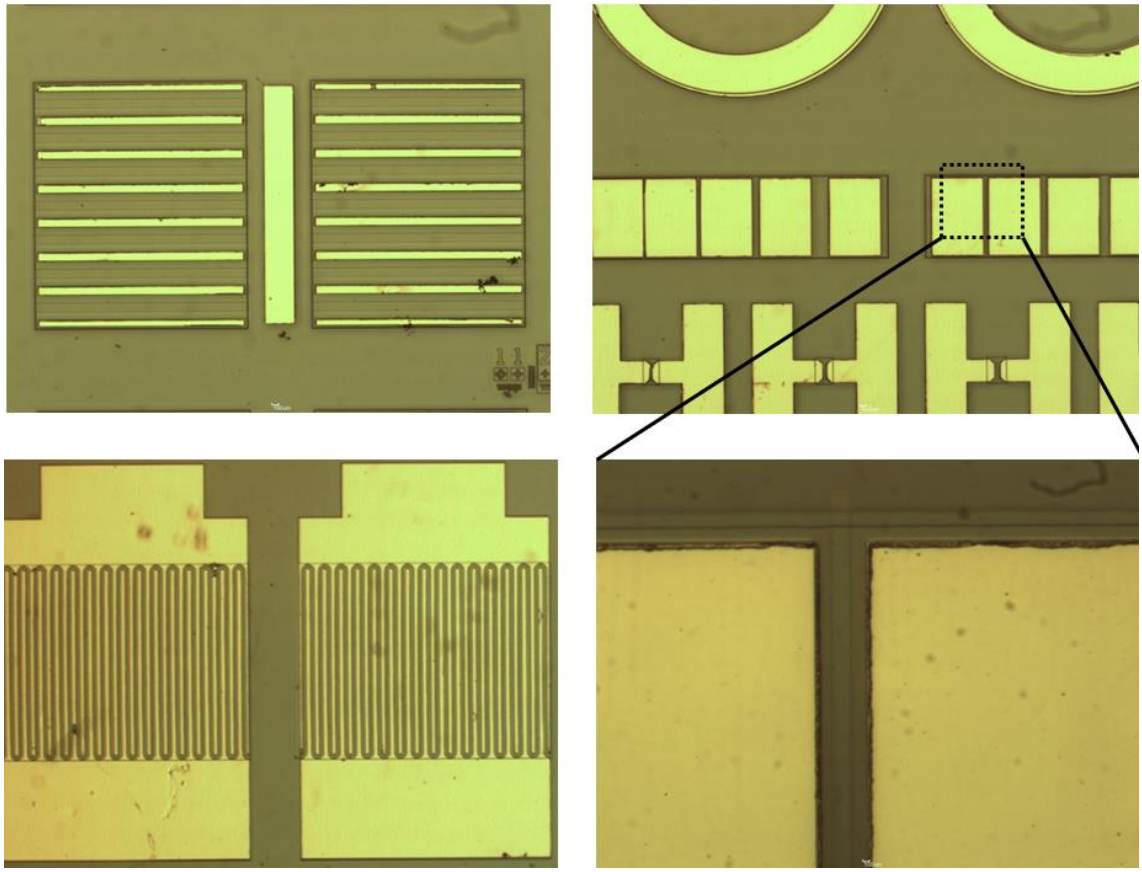
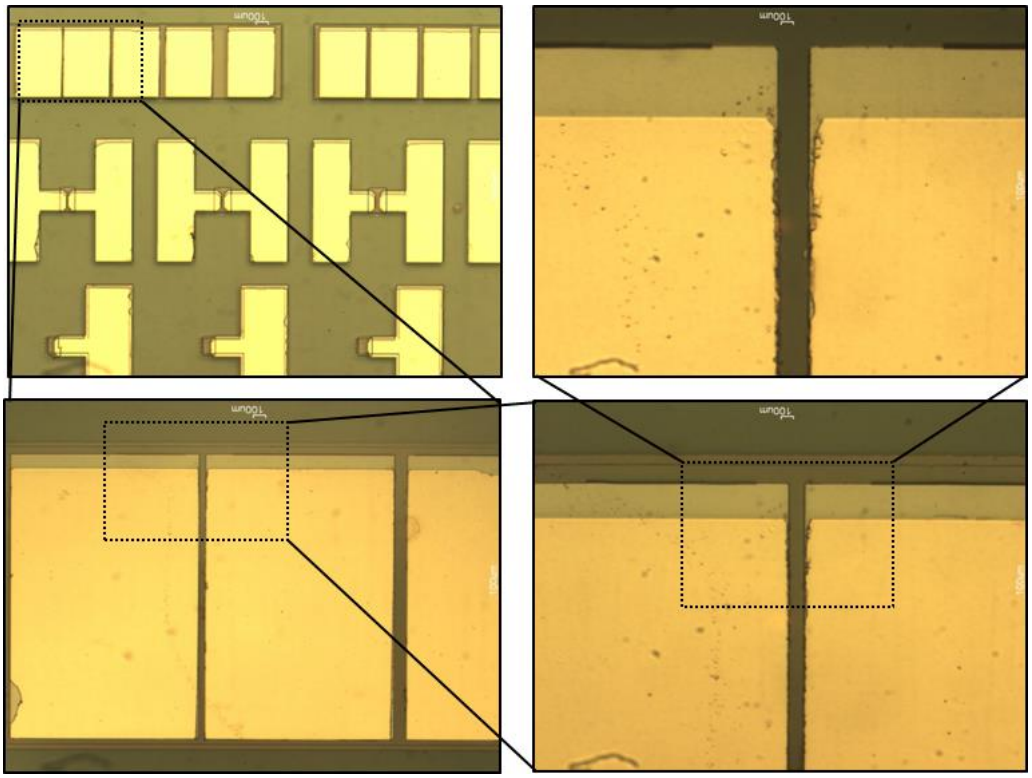


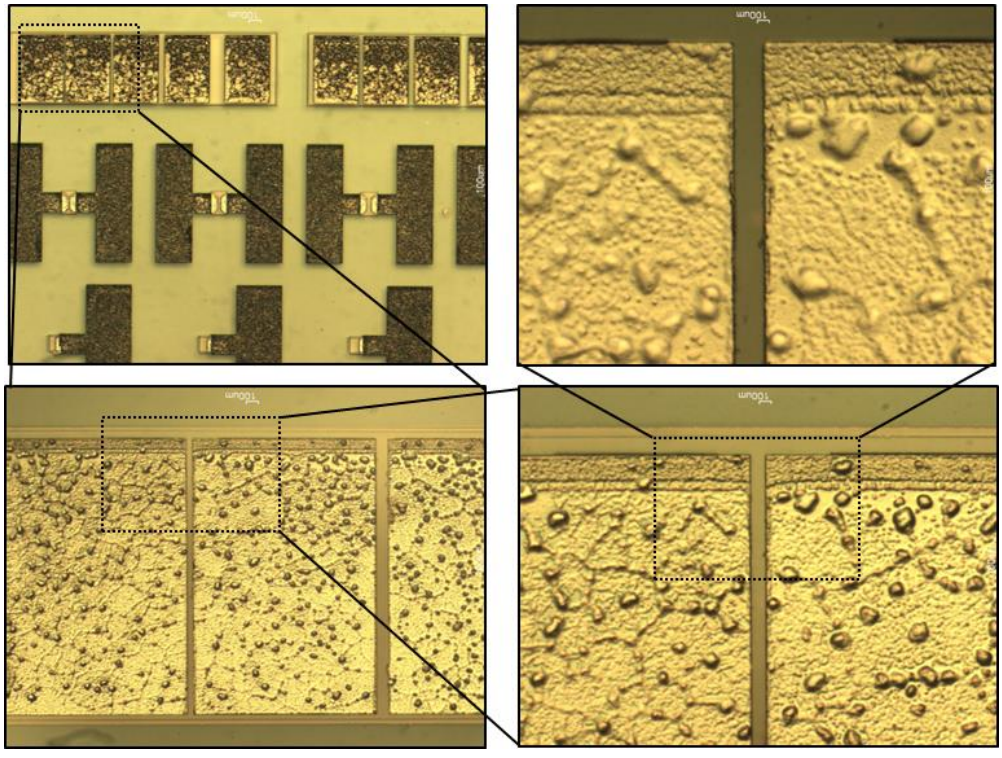
Figure 3.38 Micrographs from one of the device samples after n-contact Metal Lift-off

3.6.8 Rapid Thermal Annealing and Ohmic Contacts

Rapid Thermal Annealing (RTA) is an essential step for formation of ohmic contacts in AlGaN/GaN devices. The thermal treatment during annealing at a high temperature leads to formation of low contact resistivity intermetallic phases at the metal semiconductor interface.



(a)



(b)

Figure 3.39 Micrographs of n-contact TLM patterns from one of the device samples (a) Before RTA (b) After RTA at 800 ^{0}C in N_2 for 1 min

The metal stack used for n-contact is Ti/Al/Ni/Au (20/100/45/55 nm) followed by 1 minute RTA at 800 ^{0}C in N_2 ambient, whereas Ni/Au (20/20 nm) followed by

10 minutes RTA at 500 ^{0}C in air ambient (N_2 + O_2) is used for p-contact in the process flow. RTA is performed on a Mattson RTA system at Sheffield. Micrographs of n-contact Transmission Line Model/Transfer Length Measurement (TLM) patterns from one of the device samples (GaN-on-6H-SiC) after n-contact Metal Lift-off and post RTA have been shown in Fig. 3.39.

The snapshot of n-contact RTA process graph is shown in Fig. 3.40.

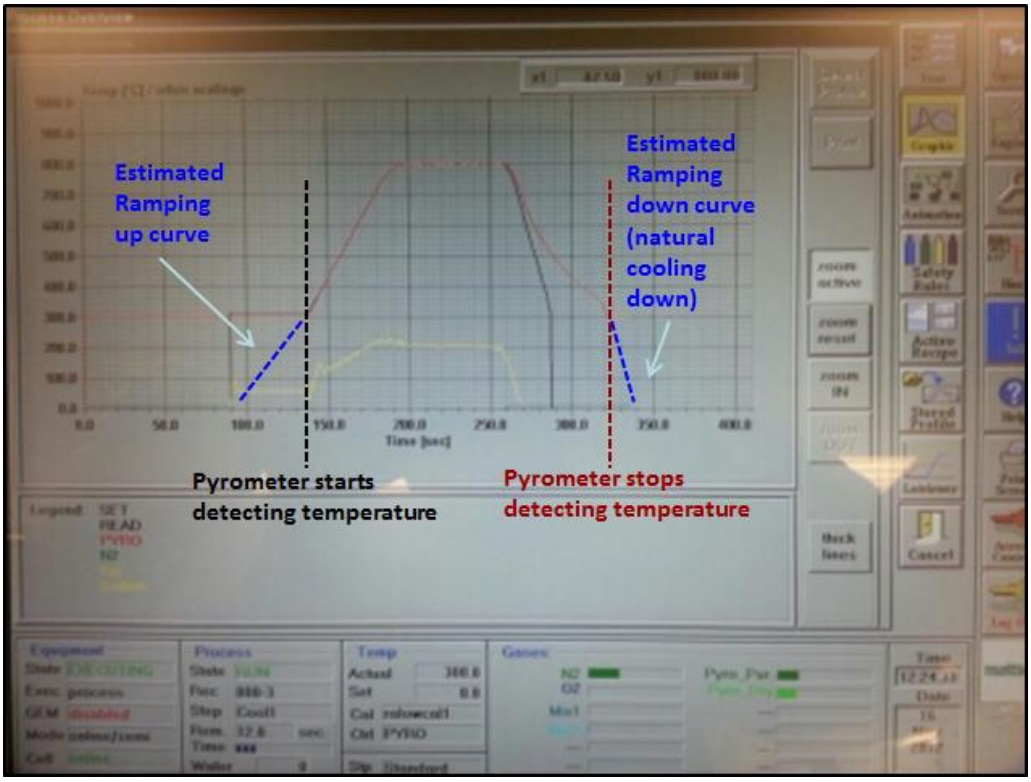
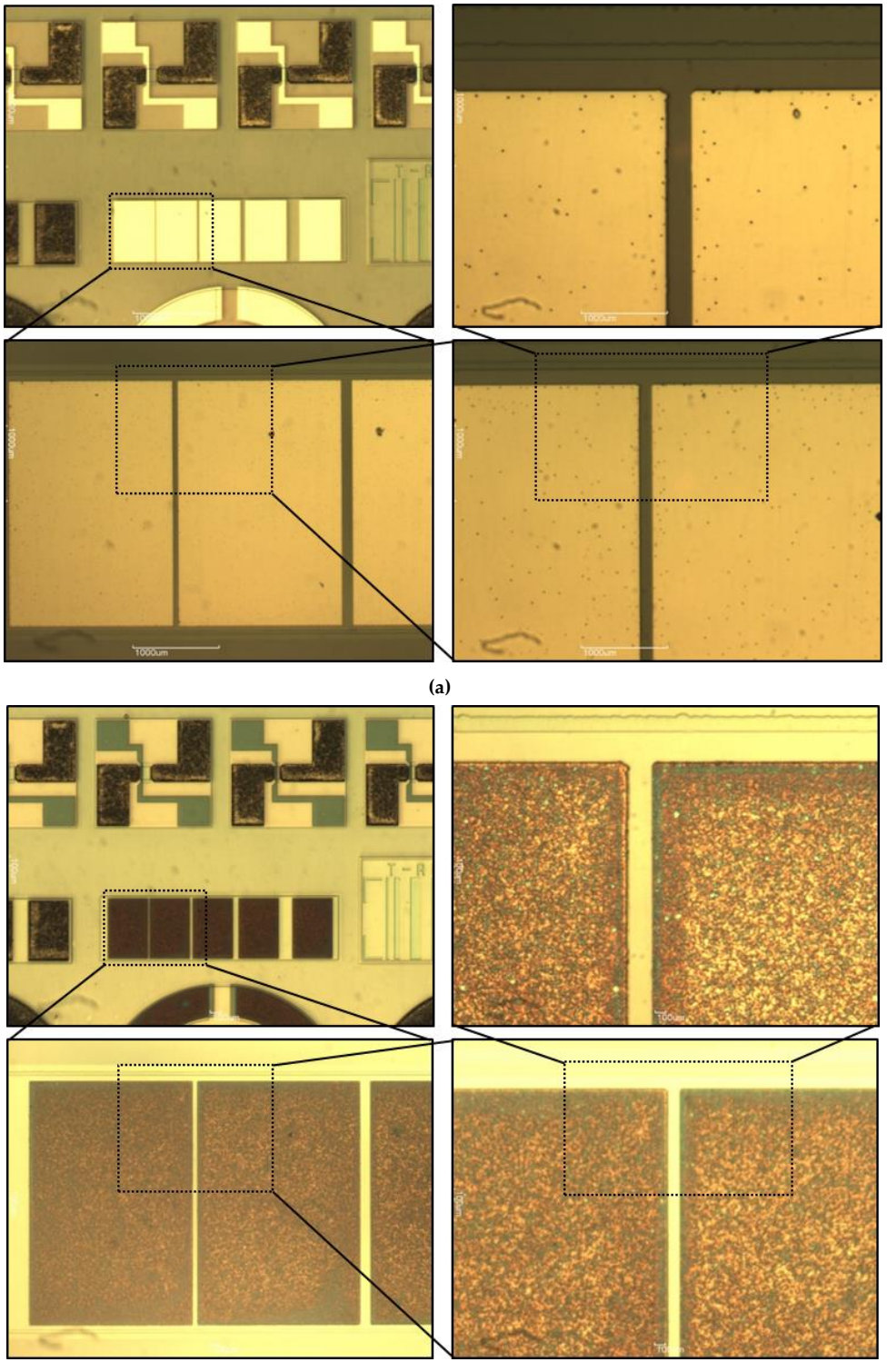


Figure 3.40 Snapshot of n-contact RTA process graph

Pyrometer in the chamber only detects temperature > 300 ^{0}C. So, the reading on the graph (**PYRO**) is only indicative for the interval when the chamber temperature > 300 ^{0}C. The low resistivity contact formation during RTA is governed by fairly complex physical mechanisms. However, the primary mechanism for obtaining low resistivity after n-contact annealing is attributed to Ti-N formation and aluminium diffusion to the metal semiconductor interface [11, 23].

Micrographs of p-contact TLM patterns from one of the device samples (GaN-on-6H-SiC) after p-contact Metal Lift-off and post RTA have been shown in Fig. 3.41.



(a)

(b)

Figure 3.41 Micrographs of p-contact TLM patterns from one of the device samples (a) Before RTA (b) After RTA at 500 ^{0}C in air for 10 mins

For p-contact formation, the heat treatment in air ambient (N_2 + O_2) develops Au/p-NiO/p-GaN heterojunction and Au network which lead to low resistivity contact formation [24].

Ohmic contact characterisation and measurement of specific contact resistivity is performed using TLM test patterns during device fabrication. The concept has been described in detail in [25] is now a widely used approach in device fabrication.

As device fabrication was performed at Sheffield and Southampton, it was essential to evaluate the ohmic contacts (n-contact and p-contact) obtained during processing at both facilities. The metal stacks and RTA conditions were chosen based on optimisation trials at Sheffield, and an attempt was made in replicating the processing conditions at Southampton. In order to evaluate n-contact, the top layers of p-GaN and u-GaN were etched away from test samples using the Mesa etch mask with a target etch depth of 65 nm, leaving an AlGaN layer thickness of ~ 22 nm.

The metal stack (Ti/Al/Ni/Au) was then evaporated to the AlGaN surface followed by RTA. For evaluating p-contact, the metal stack (Ni/Au) was deposited directly on the p-GaN surface followed by RTA. Considering that different RTA equipment were used at both facilities, made it quite challenging to match the performance. The results of the n-contact optimisation trials achieved at Southampton and Sheffield are presented in Figs. 3.42 - 3.43.

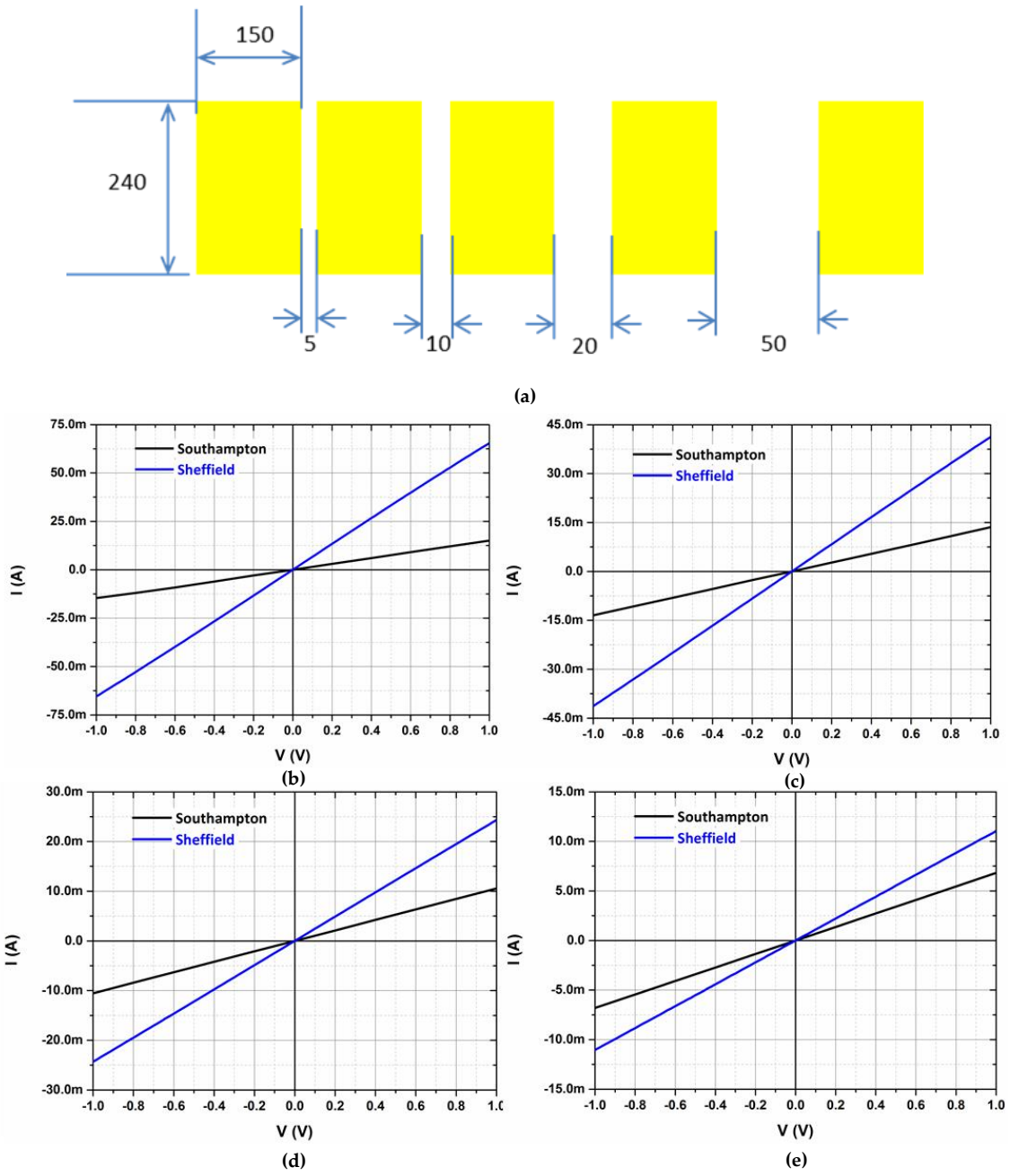


Figure 3.42 (a) Schematic of TLM pattern (dimensions in μm) and I-V characteristics for n-contact TLM separation of (b) 5 μm (c) 10 μm (d) 20 μm (e) 50 μm

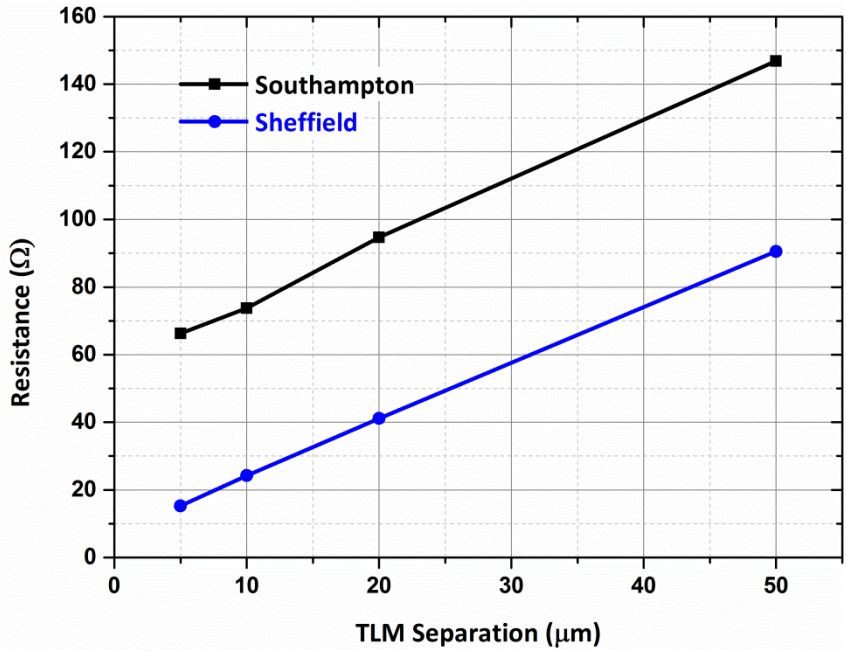


Figure 3.43 Resistance vs. TLM separation

Based on this method, the values of specific contact resistivity of n-contacts were derived as 1.1 x 10^{-3} Ω.cm^2 and 2.0 x 10^{-5} Ω.cm^2 at Southampton and Sheffield respectively. Although linear and ohmic characteristics were obtained at both sites, as n-contact directly relates to the quality of Drain/Cathode and Source contacts in devices, the devices fabricated at Southampton were expected to have higher values of on-state resistance.

The results of the p-contact optimisation trials achieved at Southampton and Sheffield are presented in Figs. 3.44 - 3.45. The test samples at Sheffield were metallised and annealed simultaneously. A quasi-ohmic behaviour was observed for all test samples; therefore the results from TLM measurements cannot truly provide a meaningful assessment of the specific contact resistance. However, the values were estimated as 6.9 Ω.cm^2, 1.0 Ω.cm^2 and 6.8 Ω.cm^2 for Southampton Test Sample, Sheffield Test Sample – 1 and Sheffield Test Sample – 2 respectively. The Sheffield Test Sample - 1 is from an older batch, whereas the other two test samples are from the same batch of epitaxial growth.

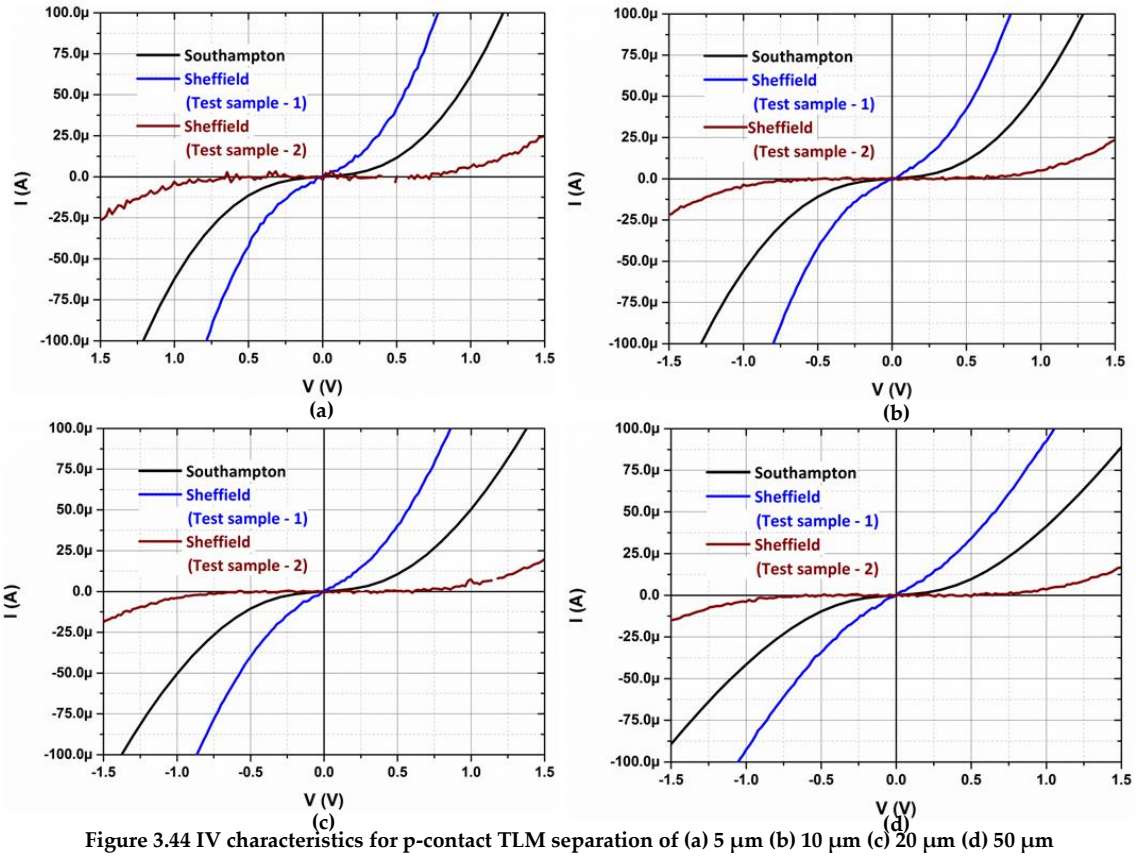


Figure 3.44 IV characteristics for p-contact TLM separation of (a) 5 µm (b) 10 µm (c) 20 µm (d) 50 µm

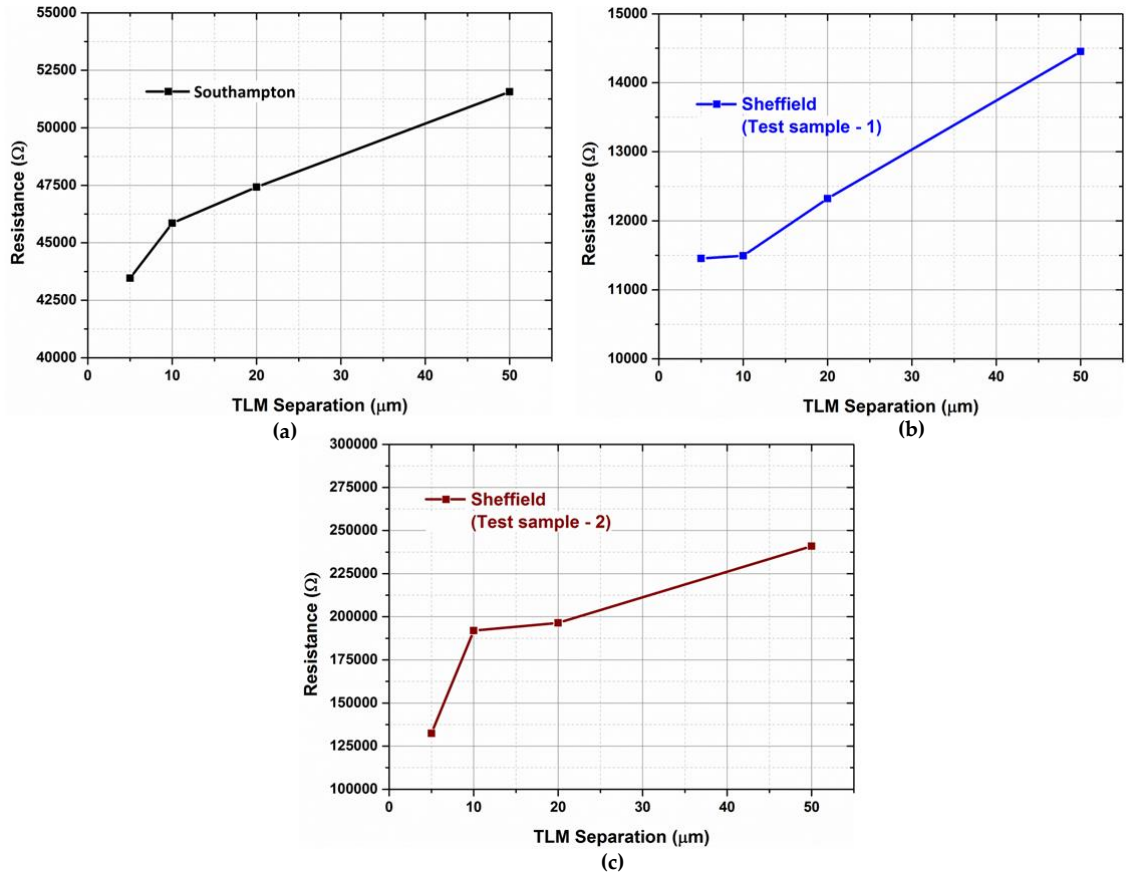


Figure 3.45 Resistance vs. TLM separation (a) Southampton (b) Sheffield Test Sample-1 (c) Sheffield Test Sample-2

Better p-type ohmic contacts can be achieved potentially by increasing the Mg doping density in the p-GaN layer, in the range of 10^{20} – 10^{21} cm^{-3} and with further optimisation of the metal stacks and annealing conditions. The overall extracted contact parameters have been summarised in Table 3.3.

Facility	Contact Resistance (Ω)	Sheet Resistance (Ω/sq.)	Specific Contact Resistance (Ω.cm²)
Southampton (Test Sample)	28.5	432	1.1E-03
Sheffield (Test Sample)	3.7	400	2.0E-05

(a)

Facility	Contact Resistance (Ω)	Sheet Resistance (Ω/sq.)	Specific Contact Resistance (Ω.cm²)
Southampton	2.2E+04	4.0E+04	6.9
Sheffield (Test Sample-1)	5.5E+03	1.7E+04	1.0
Sheffield (Test Sample-2)	7.5E+04	4.7E+05	6.9

(b)

Table 3.3 Extracted contact parameters (a) n-contact, V_{BIAS} = 1 V (b) p-contact, V_{BIAS} = 0.5 V

3.6.9 Reactive Ion Etching

Reactive Ion Etching (RIE) is a very widely employed dry etching technique in microelectronic device fabrication. Anisotropic chemical etching is accomplished in the presence of ion bombardment during this process. In comparison to ICP etching where both ion density and ion energy could be controlled separately, this option is not available in RIE etcher and the two are determined by the value set for RF power.

RIE has been employed in the process flow at via etching and pad opening stage, as metallised samples could not be processed in ICP etcher at the facility.

Via etching is a more critical step due to etching of fine feature size of 1µm, where insulator deposited during Gate Insulation step is etched to ensure second metal continuity to underlying Source, Drain/Cathode and Base/Anode contacts. The equipment used during device fabrication is shown in Fig. 3.46 (a).

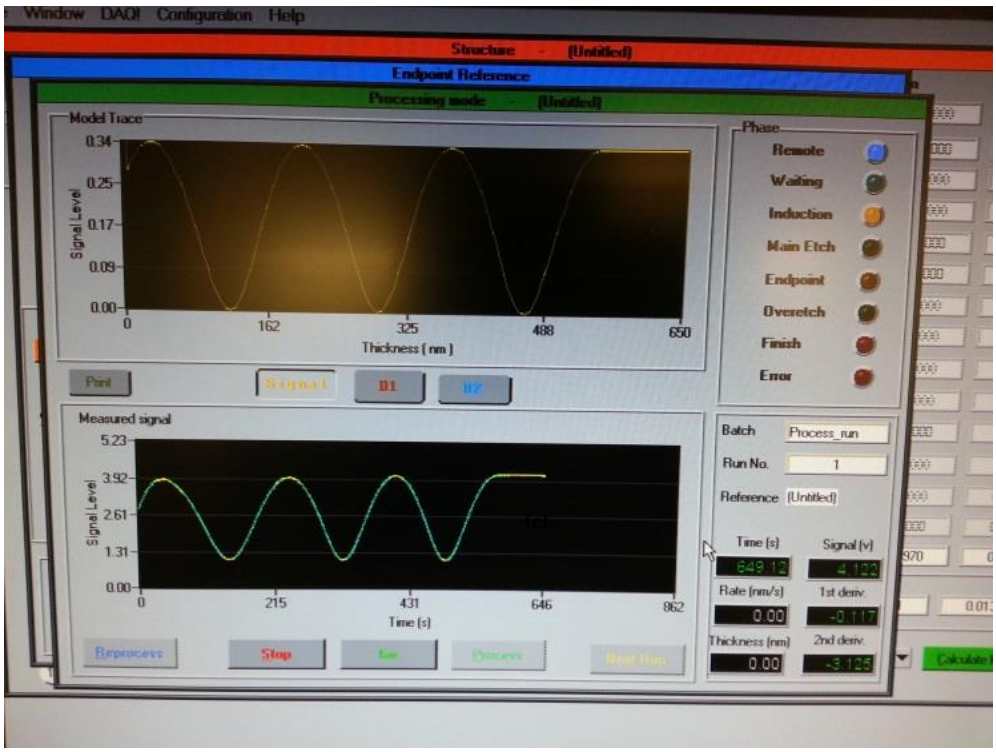
(a)

RIE Etch Recipe Settings

Gases
CHF_3 (Trifluoromethane): 35 sccm
O_2 : 5 sccm

RF Power : 100 Watts
Pressure : 35 mTorrs
Etch time : Based on end-point detection (~ 8 mins)

(b)



(c)

Figure 3.46 RIE Etching (a) Plasma Technology RIE equipment (b) Recipe Settings (c) Laser end-point detection

During RIE etching, laser end-point detection is used to track the etching process. Laser point is focussed on a Si test sample that had been processed simultaneously with the actual GaN samples during SiN deposition at PECVD. Flattening of the sinusoidal curve on the end-point detection graph as shown in Fig. 3.46 (c) indicates a transition from SiN to Si and that SiN layer has been etched. The etch process is continued for some additional time to account for any possible non-uniformity of etching across the samples. Surface profilometry as well as electrical measurements are performed subsequently to ensure that the insulating layer has been completely removed from the targeted regions.

SiN on Si test samples patterned using the Via mask as shown in Fig. 3.47 are used to estimate the etch rate before proceeding with the GaN device samples.

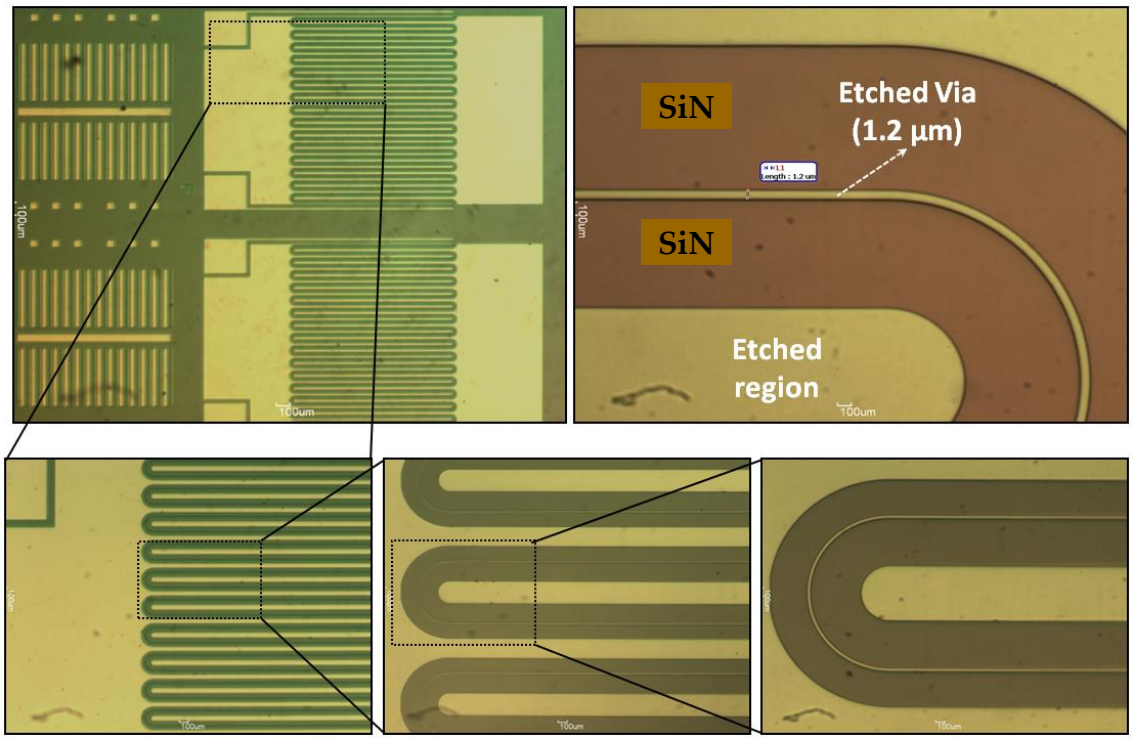


Figure 3.47 RIE etch optimisation trial with SiN on Si test sample

The etch rate was estimated as 67 nm/minute. Surface profilometry was used to verify the etch depth and a comparison is performed with that of the originally

deposited thickness based on data from Ellipsometry. This has been shown in Fig. 3.48.

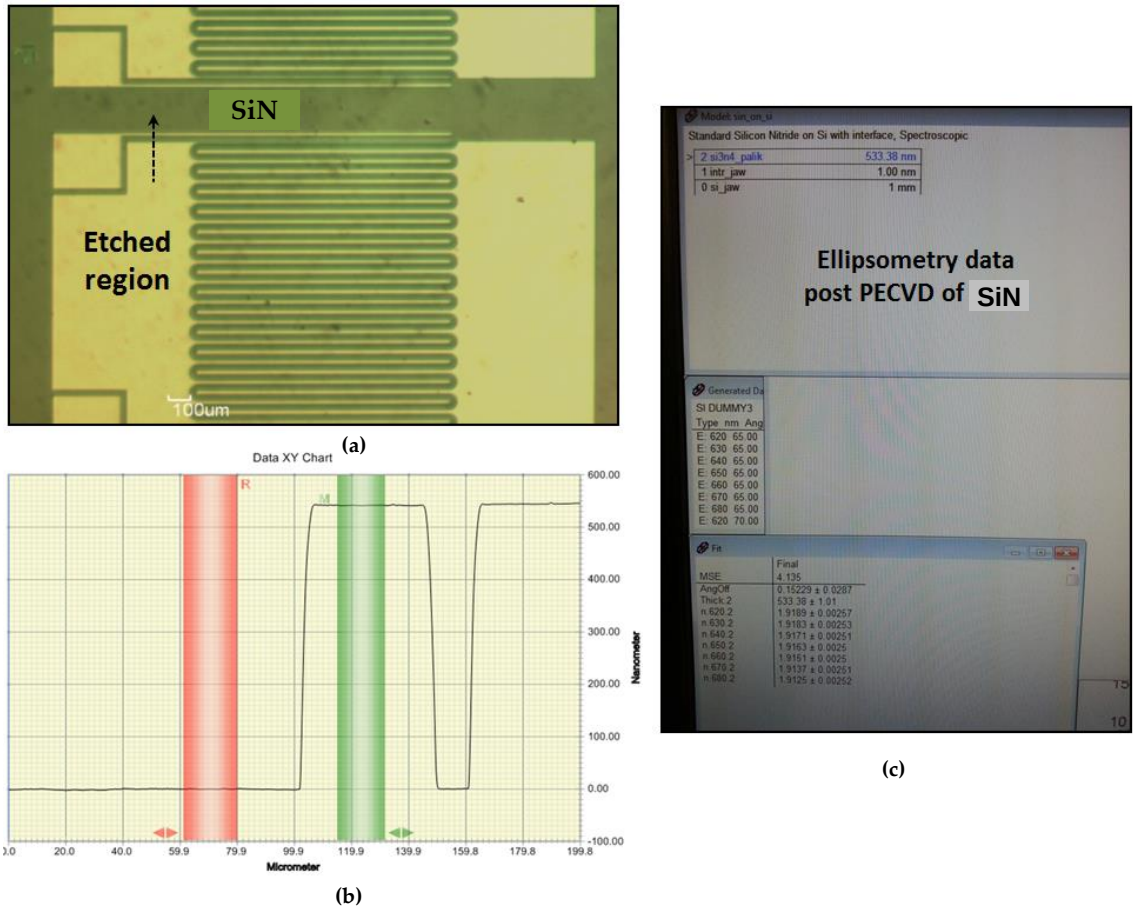
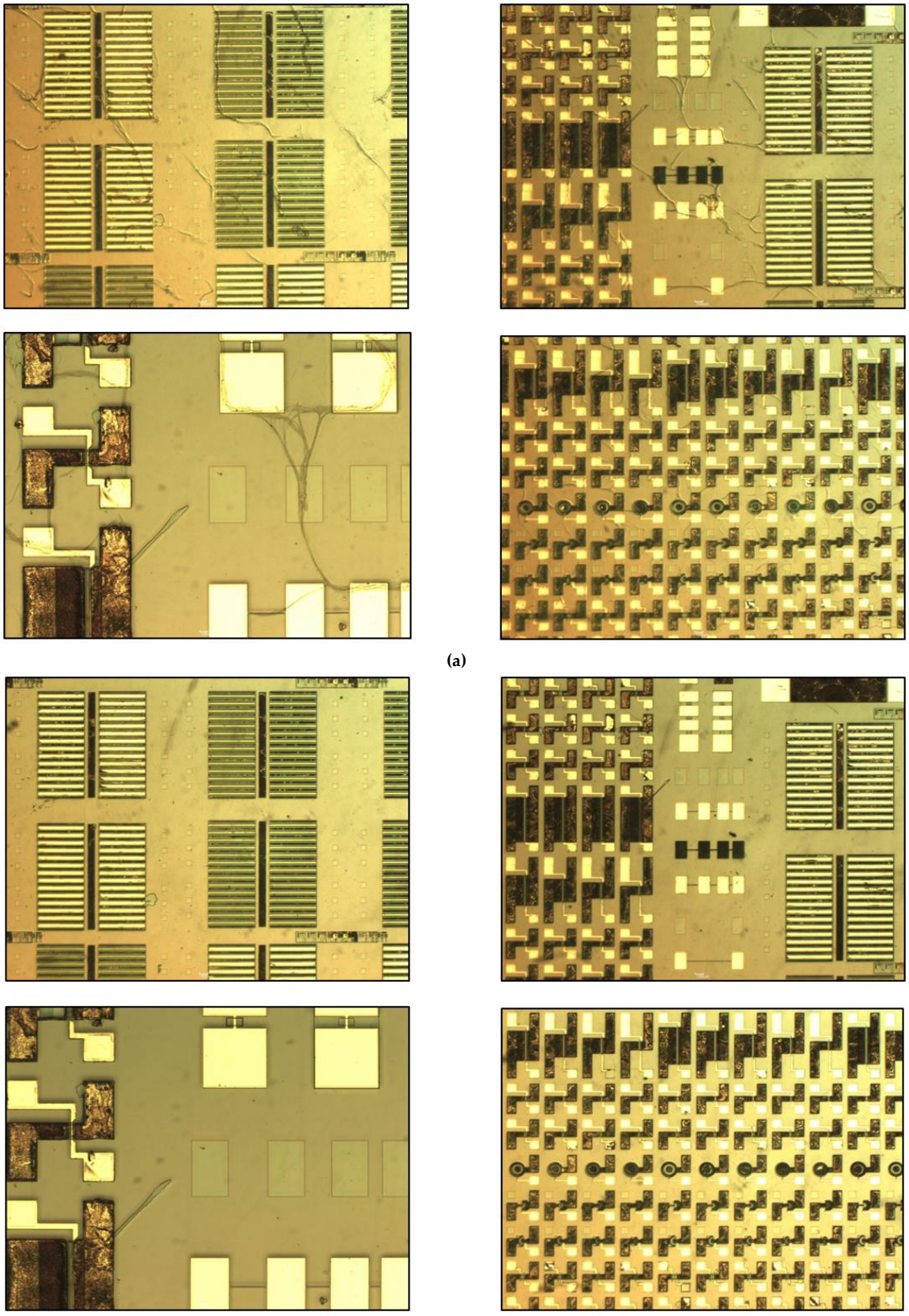


Figure 3.48 (a) SiN on Si test sample (b) Post etch surface profilometry results (c) Data from Ellipsometry

After establishing the etch rate, GaN device samples were etched under the same conditions. A SiN on Si test sample was used to estimate the end-point of the etch process.

An anomaly that was observed after RIE etching was hardening of the photoresist and difficulty in stripping the same using Posistrip EKC800™ (resist stripper) and standard three step cleaning. The micrographs at this stage and after two rounds of oxygen descum which addressed the issue (first with 1 minute and second with 3 minutes in the oxygen plasma asher) have been shown in Fig. 3.49.



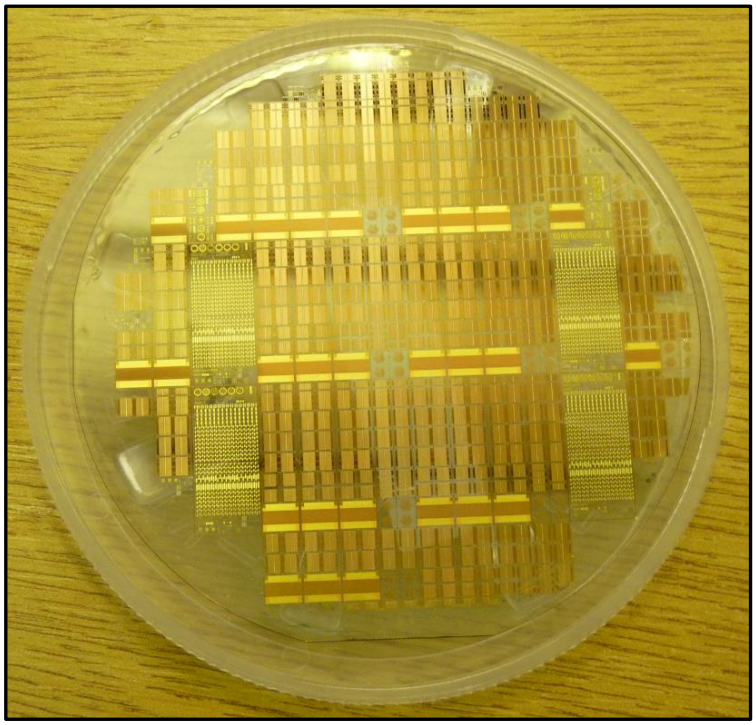
(a)

(b)

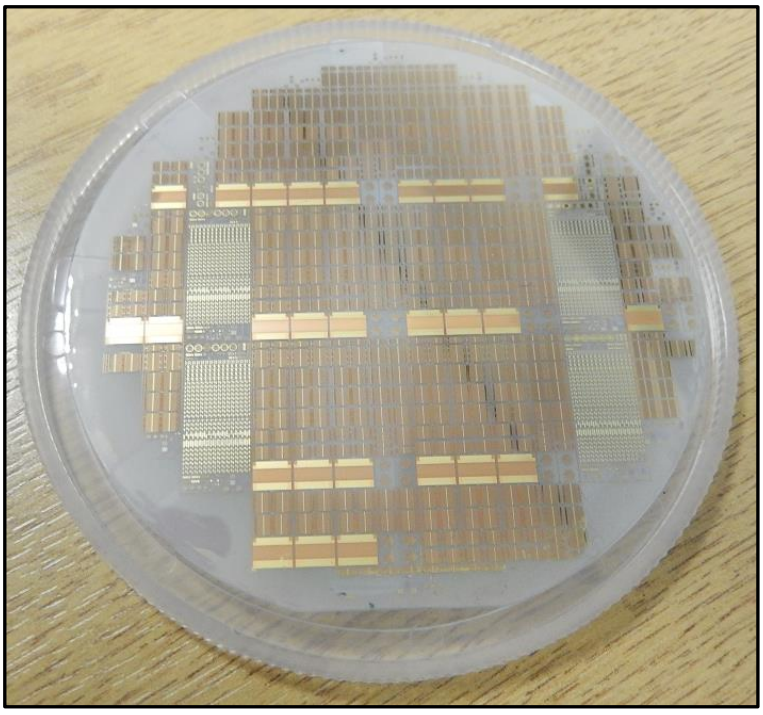
Figure 3.49 Micrographs of GaN device sample (a) After resist stripping using Posistrip and clean (b) After oxygen descum

3.6.10 Fabricated Wafers and Devices

Pictures of 3″ processed wafers from Southampton and the one of the GaN-on 6H SiC units processed at Sheffield have been shown in Fig. 3.50 and Fig. 3.51 respectively.



(a)



(b)

Figure 3.50 Pictures of (a) 3″ processed GaN-on-6H-SiC wafer (b) 3″ processed GaN-on-Sapphire wafer

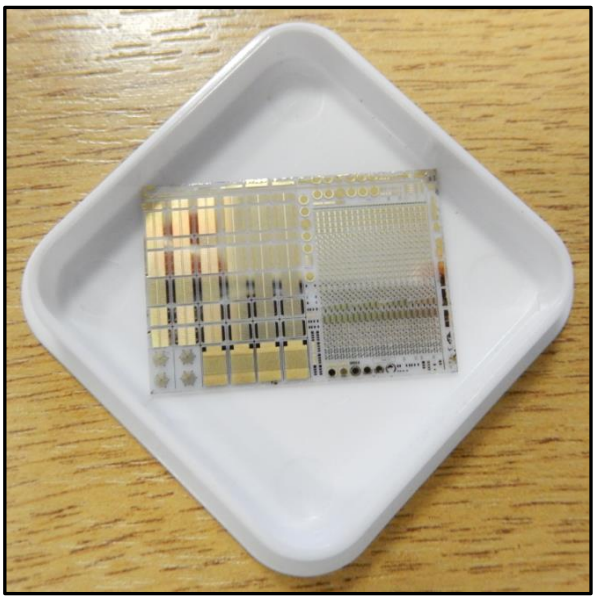
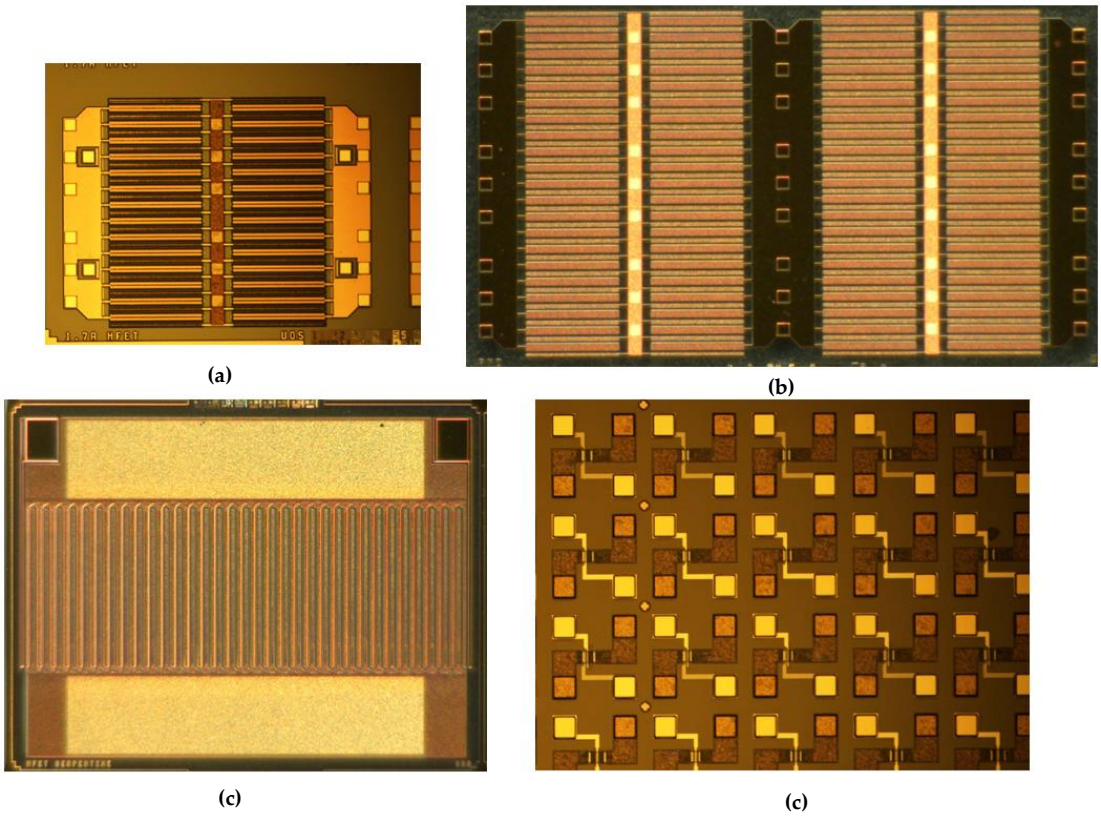


Figure 3.51 Picture of (a) processed GaN-on-6H-SiC unit (26 mm x 18 mm) at Sheffield

Some of the fabricated large area devices as well as device test structures from wafers processed at Southampton as well as the units processed at Sheffield have been shown in Fig 3.52 and 3.53 respectively.



(a) **(b)** **(c)** **(c)**

Figure 3.52 Fabricated devices at Southampton (a) HFET (Multifinger)(b) PN Diode (c) HFET (Serpentine) (d) Device Test Structures

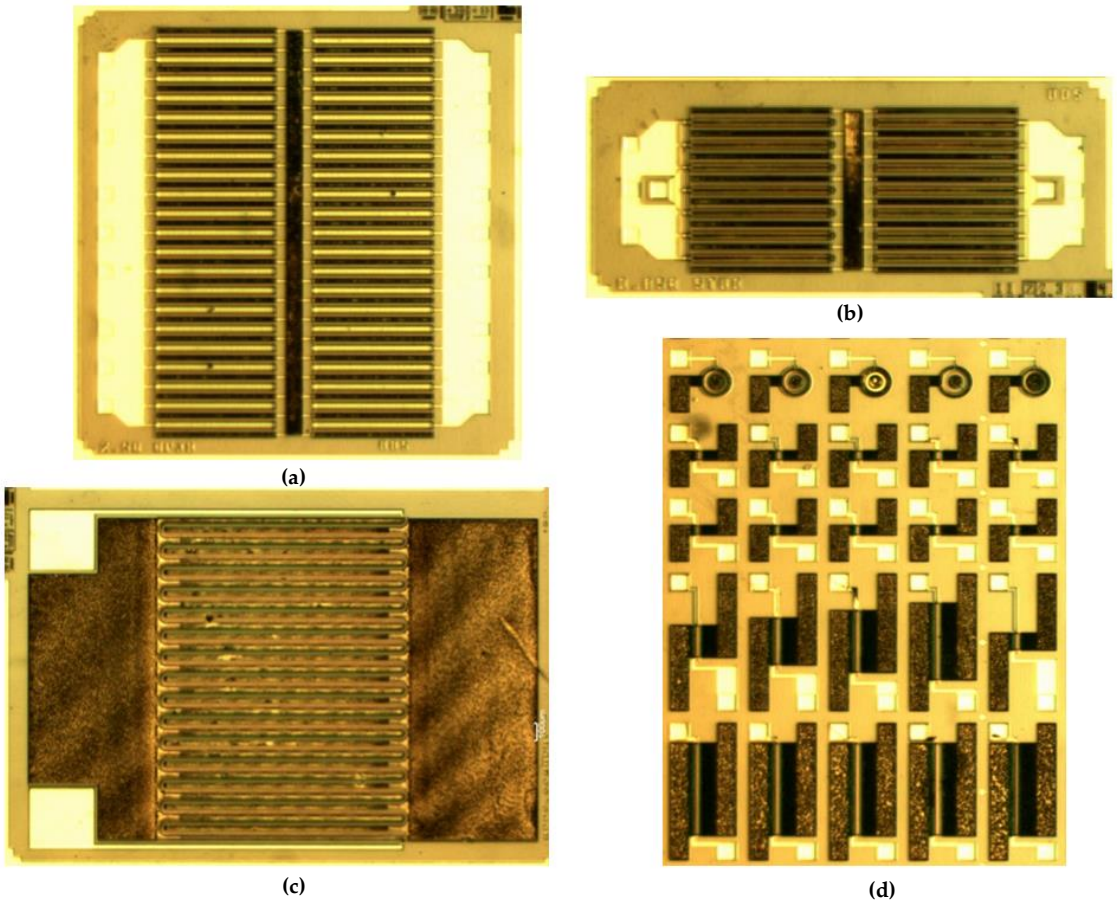


Figure 3.53 Fabricated devices at Sheffield (a) PJ Diode (b) HFET (Multifinger) (c) HFET (Serpentine) (d) Device Test Structures

3.6.11 Key differences in processing at Sheffield and Southampton

Apart from differences in the equipment and materials (for e.g. photoresists, chemicals) used during processing, there were two key differences in processing at Sheffield and Southampton which have been enumerated below:

1. As uniformity of etching is extremely critical at 3" wafer level processing, the etching of GaN, AlGaN layers during Isolation and Mesa etching were performed using Ion Beam Etching (IBE, Ar plasma based purely physical etching) at Southampton as this could historically offer better uniformity, whereas the same was accomplished using ICP etching at Sheffield.
2. For the large area devices fabricated at Sheffield, the thickness of second metal was chosen as 1µm (compared to second metal thickness of 4µm at

Southampton), as that was the highest thickness which could be achieved reliably during metal Lift-off, based on available photoresists at the facility.

3.7 Summary

In this chapter, the concept of Polarisation Super Junction (PSJ) was introduced initially and the technique of charge compensation achieved by engineering the polarisation charges inherent in the material system was described. Numerical simulation results were presented comparing two designs, one of which was based on Field Plate engineering and the other was based on PSJ with the objective of gaining insight into the physical mechanisms in the device that determined the on-state and off-state electrical characteristics. Following that, the approach to device design and scalability to large area devices, process development/optimisation, mask design, processing challenges, and elaborate results of device fabrication were presented and discussed in detail. Process optimisation and evaluation for definition of n-contact indicated that the contact resistance (and thereby the on-state resistance) for the devices fabricated at Southampton were expected to be higher. Detailed measurement results and discussion on the performance of the fabricated devices have been presented in chapter 4.

3.8 References

[1] A. Nakajima, K. Adachi, M. Shimizu, and H. Okumura, "Improvement of unipolar power device performance using a polarisation junction," *Applied Physics Letters*, vol. 89, pp. 193501-1- 193501-3, 2006.

[2] A. Nakajima, Y. Sumida, M. H. Dhyani, H. Kawai, and E. M. S. Narayanan, "High Density Two-Dimensional Hole Gas Induced by Negative Polarisation at GaN/AlGaN Heterointerface," *Applied Physics Express*, vol. 3, pp. 121004-1- 121004-3, 2010.

[3] A. Nakajima, Y. Sumida, M. H. Dhyani, H. Kawai, and E. M. S. Narayanan, "GaN-Based Super Heterojunction Field Effect Transistors Using the Polarisation Junction Concept," *IEEE Electron Device Letters*, vol. 32, no. 4, pp. 542-544, 2011.

[4] A. Nakajima, M. H. Dhyani, Y. Sumida, H. Kawai, and E. M. S. Narayanan, "GaN Based Super HFETs over 700V Using the Polarisation Junction Concept," in *Proceedings of the 23rd International Symposium on Power Semiconductor Devices & ICs*, San Diego, 2011, pp. 280-283.

[5] R. Pengelly, S. Wood, J. Milligan, S. Sheppard, and W. Pribble, "A Review of GaN on SiC High Electron-Mobility Power Transistors and MMICs," *IEEE Transactions in Microwave Theory and Techniques*, vol. 60, no. 6, pp. 1764-1783, 2012.

[6] Y. F. Wu , M. Moore , A. Saxler , T. Wisleder, and P. Parikh, "40-W/mm double field-plated GaN HEMTs," *Proceedings of the 64th Device Research Conference*, 2006, pp. 151-152.

[7] SILVACO ATLAS, TCAD Examples - GANFET [Online]. Available: http://www.silvaco.com/examples/tcad/section21/example3/index.html.

[8] U. Kaufmann, P. Schlotter, H. Obloh, K. Kohler, and M. Maier, "Hole conductivity and compensation in epitaxial GaN : Mg layers," *Physical Review*, vol. B 62, pp. 10867–10872, 2000.

[9] SILVACO ATLAS, TCAD Examples - GANFET [Online]. Available: http://www.silvaco.com/examples/tcad/section21/example2/index.html.

[10] M. W. Fay, G. Moldovan, P. D. Brown, I. Harrison, J. C. Birbeck, B. T. Hughes, M. J. Uren, and T. Martin, "Structural and electrical characterization of AuTiAlTi/AlGaN/GaN ohmic contacts," *Journal of Applied Physics*, vol. 92, no. 1, pp. 94-100, 2002.

[11] S. S. Mahajan, A. Dhaul, R. Laishram, S. Kapoor, S. Vinayak, and B.K. Sehgal, "Micro-structural evaluation of Ti/Al/Ni/Au ohmic contacts

with different Ti/Al thicknesses in AlGaN/GaN HEMTs," *Materials Science and Engineering*, vol. 183, pp. 47-53, 2014.

[12] R. Beach, and P. Bridger, "III-nitride device with improved layout geometry," U.S. Patent 7417257 B2, August 26, 2008.

[13] B. Narayan, "Study of III-N Heterostructure Field Effect Transistors," M.S. thesis, School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, 2010.

[14] R. J. Miller, and A. Gangulee, "Electromigration in Gold and copper thin film conductors," *Thin Solid Films*: *International Journal on the Science and Technology of Condensed Matter Films*, vol. 69, no. 3, pp. 379-386, 1980.

[15] J. R. Black, "Current Limitations of Thin Film Conductors," in *Proceedings of the 20th International Reliability Physics Symposium*, San Diego, 1982, pp. 300-306.

[16] S. Kilgore, C. Gaw, H. Henry, D. Hill, and D. Schroder, "Electromigration of Electroplated Gold Interconnects," in *Proceedings of Materials Research Society Symposium*, San Francisco, 2005, pp. B8.30.1-B8.30.6.

[17] M. Pavier, A. Woodworth, A. Sawle, R. Monteiro, C. Blake, and J. Chiu, "Understanding the Effect of Power MOSFET Package Parasitics on VRM Circuit Efficiency at Frequencies above 1MHz," in *Proceedings of Power Conversion and Intelligent Motion Conference*, Nűrnberg, 2003, pp. 279-284.

[18] J. Pan, and P. Fraud, "Wire Bonding Challenges in Optoelectronics Packaging," Society of Manufacturing Engineers, Dearborn, Technical Paper TP04PUB284, 2004.

[19] D. Kurra, Z.J. Delalic, and L. Levine, "Gold Stud Bumped Flip Chip: Surface Mounting and Joint Integrity with Thermal Cycling," in *Proceedings of the 38th International Symposium on Microelectronics*, Philadelphia, 2005.

[20] L. Deng, and A. Goodyear. (2004). Etching of III-V Materials using Inductively Coupled Plasma (ICP) Systems [Online]. Available: http://www.oxford plasma.de/pla_news/etch35s.pdf.

[21] J.A. Woollam Company. Tutorial on Ellipsometry [Online]. Available: http://www.jawoollam.com/tutorial_1.html.

[22] S.A. Campbell, *The Science and Engineering of Microelectronic Fabrication*. New York: Oxford, 2006.

[23] F. Calle, T. Palacios, E. Monroy, J. Grajal, M. Verdú, Z. Bougrioua, et al., "AlGaN/GaN HEMTs: material, processing, and characterization," *Journal of Materials Science: Materials in Electronics*, vol. 14, pp. 271-277, 2003.

[24] L. C. Chen, J. K. Ho, C. S. Jong, C. C. Chiu, K. K. Shih, F. R. Chen, et al., "Oxidized Ni/Pt and Ni/Au ohmic contacts to p-type GaN," *Applied Physics Letters*, vol. 76, no. 25, pp. 3703-3705, 1999.

[25] G. K. Reeves, and H.B. Harrison, "Obtaining the Specific Contact Resistance from Transmission Line Model Measurements," *IEEE Electron Device Letters*, vol. 3, no. 5, pp. 111-113, 1982.

Chapter 4 Electrical Characterisation of Fabricated Devices

In this chapter, the performance and electrical characterisation results of fabricated test structures as well as various large area Polarisation Super Junction (PSJ) devices are presented and discussed in detail. The reported work provides key insight and understanding of the dominant factors determining the performance of the scaled-up devices. Some of the results and discussion presented in this chapter have been published in the proceedings of the 26th IEEE International Symposium on Power Semiconductor Devices & IC's (*ISPSD*, 2014) [1].

4.1 Introduction

As described in the previous chapter, the scaling up activity from device test structures to large area devices focussed on the following devices

1. Hybrid/PSJ Diodes
2. PSJ HFETs
3. PN Diodes

The above-mentioned types of devices with various current carrying capabilities along with several device test structures were fabricated on high resistivity (~ 10^5 Ω.cm) 6H-SiC substrates (two samples processed in Sheffield (referred to as *GaN-on-SiC-1 (Sheff.)* and *GaN-on-SiC-2 (Sheff.)* in this chapter), two 3" wafers processed in Southampton (referred to as *GaN-on-SiC-1 (S'ton)* and *GaN-on-SiC-2 (S'ton)* in this chapter)) as well as Sapphire substrate (one 3" wafer processed in Southampton referred to as *GaN-on-Sapphire (S'ton)* in this chapter)). Detailed electrical characterisation was performed on test structures as well as large area devices. The key results representing typical device performance are presented in a manner that enables correlation of the critical electrical characteristics between process test structures and the scaled-up devices in the individual wafers.

The list of large area devices discussed in this chapter and key wafer-level electrical characterisation results obtained have been summarised in Table 4.1.

Device Type	Width (mm)	Wafer	R_{ON} (Ω.mm)	Off-state Leakage (*)	Remarks
PSJ Diode	8.4	GaN-on-SiC-1 (***Sheff.***)	24	1 mA	
	25.2	GaN-on-SiC-1 (***S'ton***)	120	50 mA	Abnormally high Cathode-Anode Schottky leakage
	25.2	GaN-on-Sapph. (***S'ton***)	111	120 mA	
PSJ HFET	8.4	GaN-on-SiC-2 (***Sheff.***)	121	1 mA	
	8.4	GaN-on-SiC-1 (***S'ton***)	105	20 mA	Abnormally high Drain-Gate Schottky leakage
PN Diode	8.4	GaN-on-SiC-1 (***S'ton***)	125	20 μA	
	8.4	GaN-on-Sapph. (***S'ton***)	91	120 μA	
	25.2	GaN-on-SiC-1 (***S'ton***)	118	50 μA	
	25.2	GaN-on-Sapph. (***S'ton***)	100	1 mA	

Table 4.1 List of large area devices and key wafer-level electrical characterisation results

(*) Off-state leakage current measured at 200 V, except for PSJ Diodes processed at Southampton which were measured at 50 V due to abnormally high Schottky leakage

Wafer-level characterisation was performed on a semi-automatic thermal probe-station (Cascade Microtech 10600, shown in Fig. 4.1). Electrical measurements were performed using Agilent B1500 and B1505 Device Analysers.

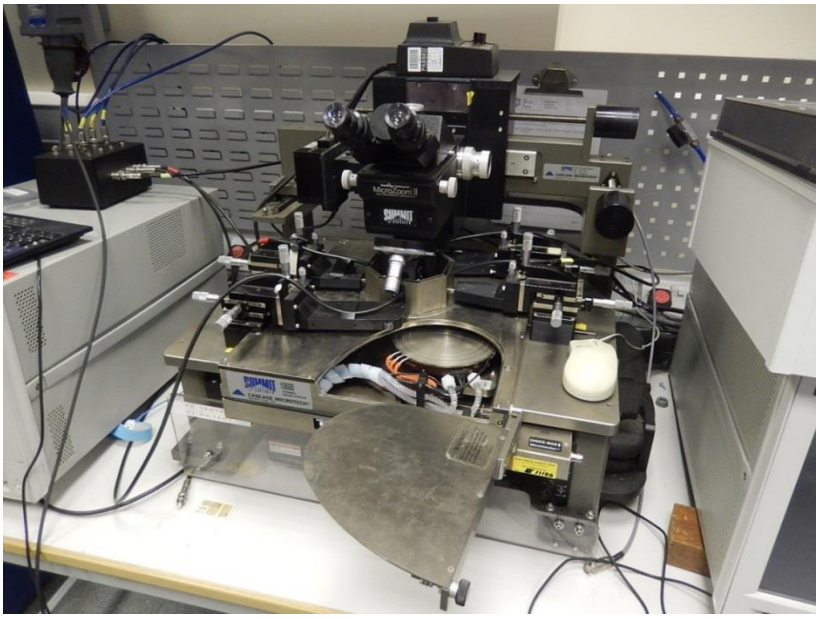


Figure 4.1 Picture of the probe-station used for wafer level characterisation

A few of the large area devices were also assembled using standard wire-bonding and flip-chip packaging techniques and results of the pilot study will also be presented.

4.2 PSJ Diodes

Power diodes are employed in various power conditioning circuits such as motor drives, inverters etc. Schottky Barrier Diodes (SBD) have an inherent advantage of low on-set voltage, no reverse recovery and low junction capacitance (negligible diffusion capacitance) giving a compelling context for development of GaN based SBDs for efficient high voltage power electronic applications. This section provides an elaborate assessment of the PSJ Diode device test structures fabricated at Sheffield (*GaN-on-SiC-1 (Sheff.)*) before moving on to the large area devices fabricated on the various wafers.

4.2.1 Device structure and fabrication

GaN/AlGaN/GaN heterostructures capped with a p-GaN layer were grown by MOCVD on high resistivity (~ 10^5 Ω.cm) 6H-SiC substrates. Due to polarisation charges at the hetero-interfaces, high density Two-Dimensional Electron Gas (2DEG) and Two-Dimensional Hole gas (2DHG) are spontaneously formed at the AlGaN/GaN and GaN/AlGaN interfaces without any intentional doping.

The device processing starts with time-controlled etching of the upper GaN layers of the heterostructure well into the GaN buffer layer for device isolation, followed by controlled etching of the top layers (p-GaN, u-GaN, and ~ 25 nm of the AlGaN layer) to define the PSJ mesa and access regions. Cathode electrodes (Ti/Al/Ni/Au) were deposited on an ICP-etched AlGaN surface and annealed at 800 °C in N_2 ambient for a minute.

Anode electrodes were formed in a two-step process with a deposition of thin Ni/Au on the p-GaN layer followed by a 500 °C anneal in air for 10 minutes (for ohmic contact formation to p-GaN layer and 2DHG), followed by additional Ni/Au deposition on top of the AlGaN (Schottky contact) and p-GaN layers. This has been illustrated in Fig. 4.2 (a) – (b), where schematics of the device cross-section have been shown.

Finally, a 500 nm SiN PECVD passivation layer was deposited over the device area and area over the pad regions was etched using Reactive Ion Etching (RIE). Additional metallisation of the pads with Ti/Au completed the device fabrication process. PSJ diodes with various drift lengths (L_{PSJ}) were fabricated. Conventional SBDs as well as PSJ Diodes were fabricated and Fig. 4.3 shows the top view of the PSJ diodes.

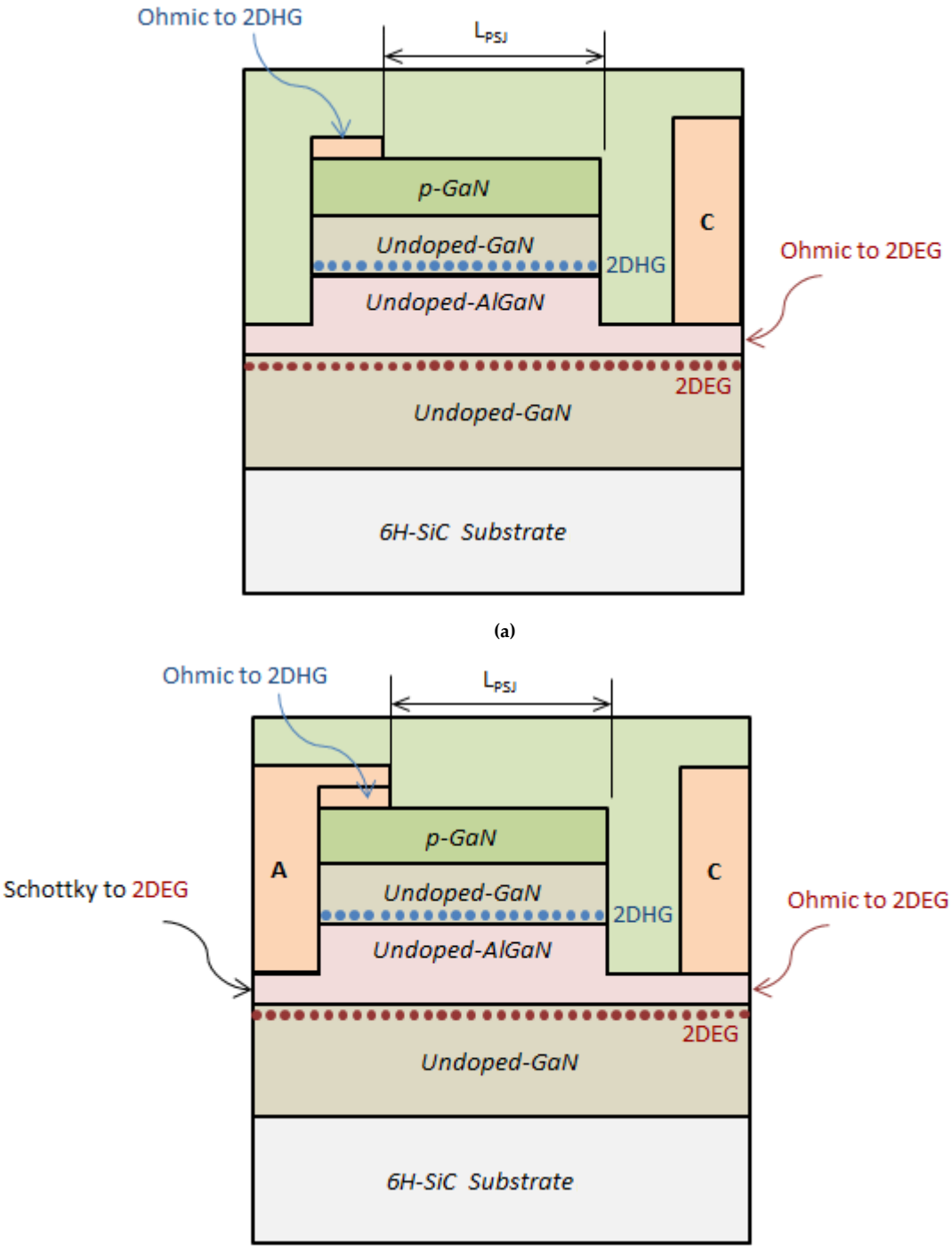


Figure 4.2 Cross-section schematics of PSJ Diode after (a) Ni/Au deposition and annealing at 500 °C (b) Additional Ni/Au deposition. A and C refer to Anode and Cathode electrodes respectively

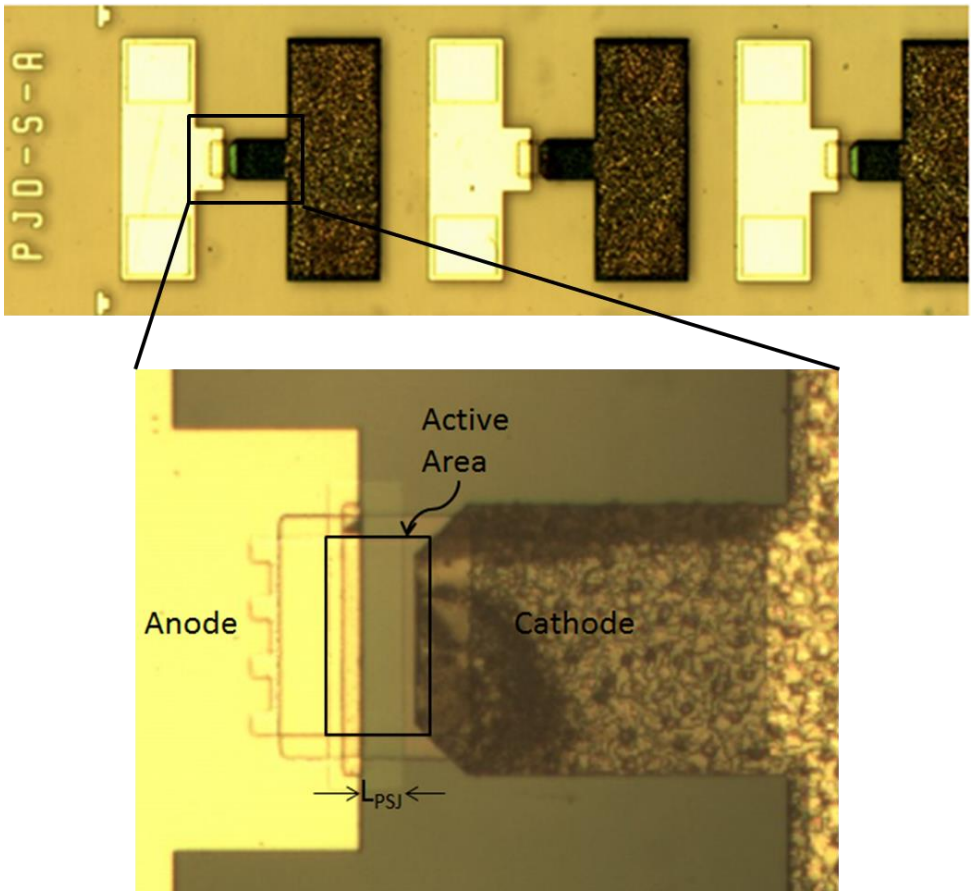


Figure 4.3 Top view photograph of fabricated PSJ Diodes on high resistivity 6H-SiC substrate

During forward conduction, current flows from Anode to Cathode through 2DEG once the forward voltage (V_{AC}) exceeds the on-set voltage in the conventional SBD as well as PSJ Diodes. But PSJ Diode is in essence a hybrid structure that intrinsically also incorporates a PN Diode (formed by 2DHG and 2DEG). Thus beyond the on-set voltage of the PN Diode, the current conduction can also take place in the PSJ layer.

In the reverse mode of the PSJ Diode, 2DHG and 2DEG are discharged through section of the Anode electrode on the p-GaN layer (ohmic to 2DHG) and Cathode electrodes respectively (ohmic to 2DEG). The drift region between the Anode and Cathode is depleted and acts as an intrinsic region due to charge compensation effects. This property enables PSJ Diodes in withstanding

exceptionally high reverse blocking voltages which can be scaled up by increasing the drift length (L_{PSJ}).

4.2.2 Electrical characterisation results

4.2.2.1 Forward I-V Characteristics

Forward I-V characteristics for PSJ Diodes with various (L_{PSJ}) are shown in Fig. 4.4. These devices show low on-set voltage of 0.4 - 0.5 V measured at 1mA/mm, and specific on-state resistance (R_{ON}.A) of ~ 14 mΩ.cm² for devices with the highest L_{PSJ} of 25 μm.

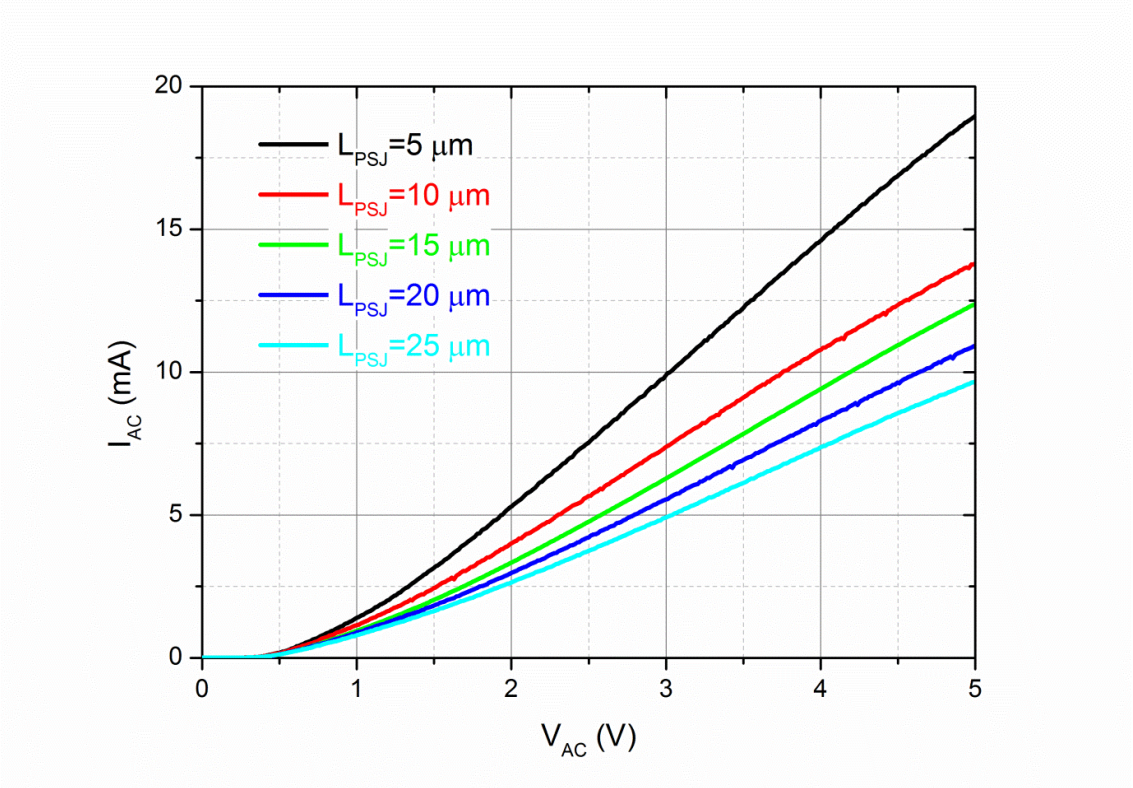


Figure 4.4 Measured forward I–V characteristics of fabricated PSJ Diodes for various PSJ lengths (L_{PSJ})

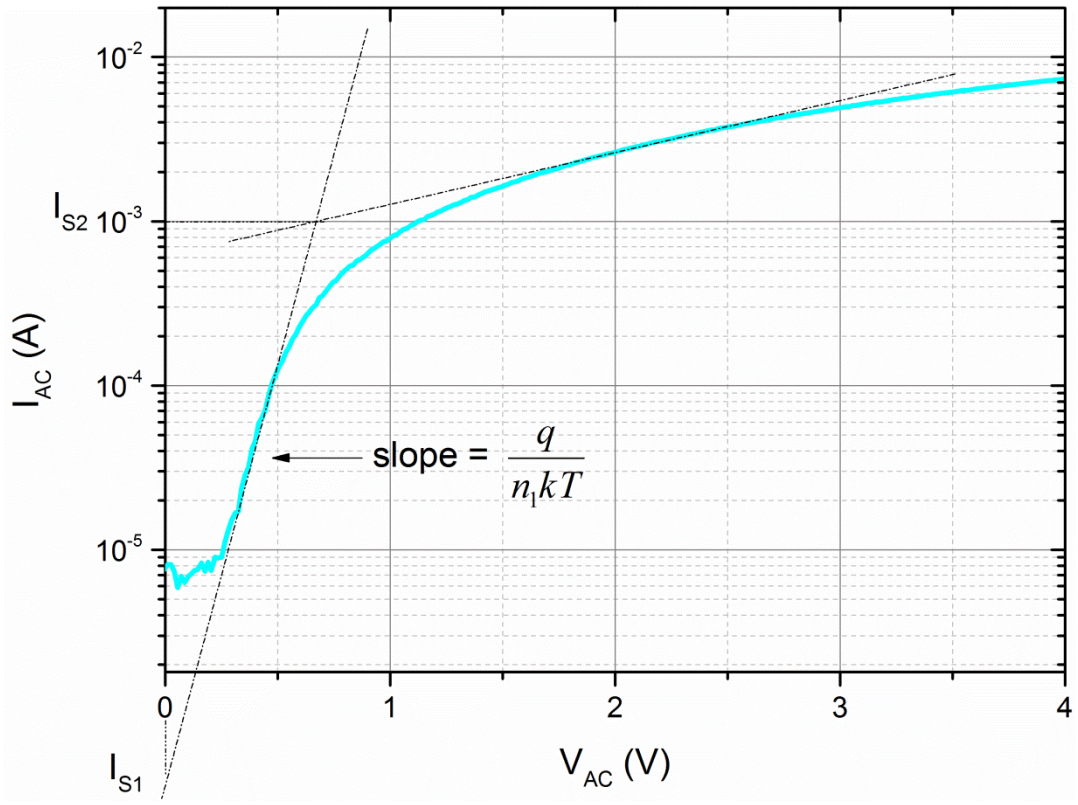


Figure 4.5 Measured forward I–V characteristics of a fabricated PSJ Diode with L_{PSJ} =25 μm

As per the characteristics shown in Fig. 4.5 for a PSJ Diode with L_{PSJ} = 25 μm, the Ideality Factor and Schottky Barrier Height have been extracted based on the approach suggested in [2]. The forward current I flowing through the diode can be expressed as

$$I = I_{S1}[\exp(qV_1/n_1kT) - 1] \quad (4.1)$$

where q is the electronic charge, V_1 is the voltage across the Schottky junction, n_1 is the ideality factor, k is the Boltzmann's constant, T is the temperature and

$$I_{S1} = SA^*T^2\exp(-q\Phi_{B1}/kT) \quad (4.2)$$

where S is the area of the Schottky region, Φ_{B1} is the Schottky Barrier Height, and A* is the effective Richardson constant given by

$$A^* = 4\pi qm^*k^2/h^3 \quad (4.3)$$

where m* is the electronic effective mass in $Al_{0.23}Ga_{0.77}N$ (0.28 m_0 (where m_0 is the free-electron mass)) and h is the Plank's constant. A^* was calculated as ~ 3.4 x 10^5 A/K^2m^2.

Ideality factor of n_1 ~ 2.5 was derived by extrapolation and estimation of I_{S1} (~ 4 x 10^{-7} A) as well as the slope ($\frac{q}{n_1 kT}$) of the linear region of the I-V curve as ~ 15.1. Based on the known parameters I_{S1} (4 x 10^{-7} A), S (10 µm x 50 µm), A* (3.4 x 10^5 A/K^2m^2) and T=300 K, the Schottky Barrier Height Φ_{B1} was obtained as ~ 0.45 eV, using (4.2).

4.2.2.2 Reverse I-V Characteristics

Breakdown Voltage/ Reverse Blocking Voltage (V_{BR}) capability of the devices with various L_{PSJ} was measured under Fluorinert ambient and floating substrate conditions. The measured reverse I-V characteristics have been shown in Fig. 4.6.

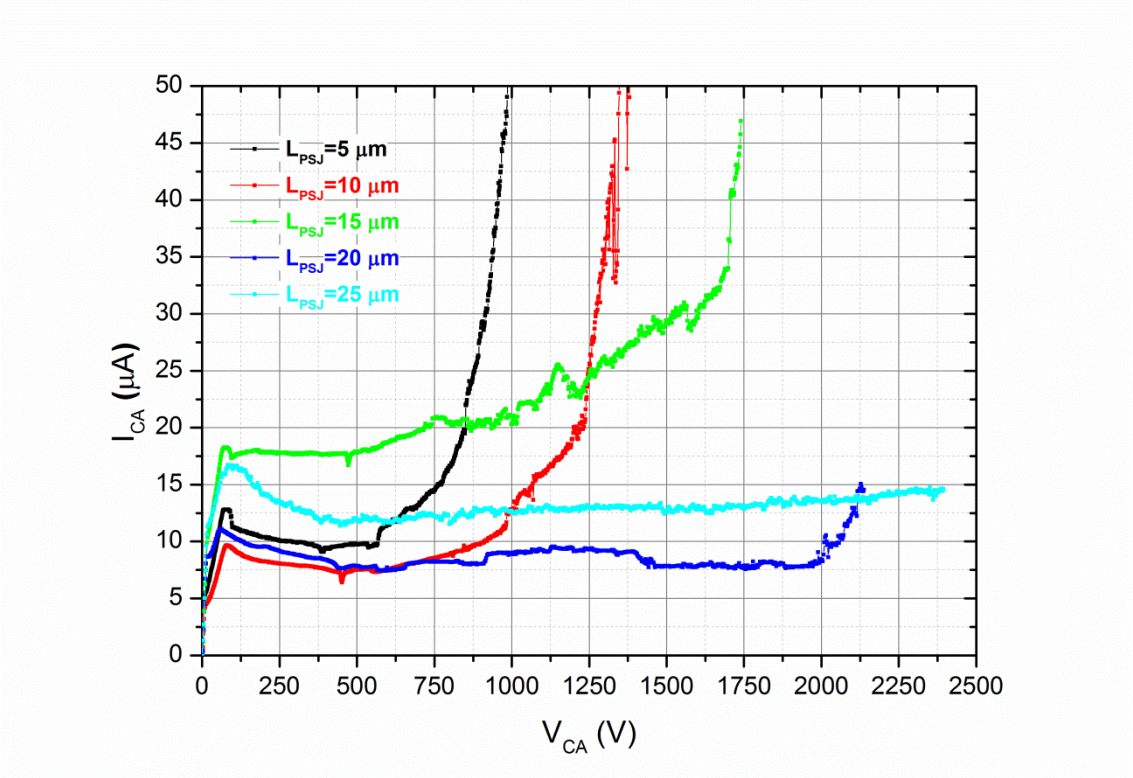


Figure 4.6 Reverse I–V characteristics of fabricated PSJ Diodes for various PSJ lengths (L_{PSJ})

Fig. 4.7 shows the dependency of V_{BR} and $R_{ON}.A$ with respect to L_{PSJ}. As shown, a linear trend is observed and V_{BR} vs. L_{PSJ} curve indicates average critical electric field strength of ~ 0.8 MV/cm. Fabricated PSJ Diodes with drift length of 25 µm show low on-set voltage of ~ 0.4 - 0.5 V, V_{BR} of ~ 2400 V, specific on-state resistance ($R_{ON}.A$) of ~ 14 mΩ.cm² and therefore a Power Device Figure of Merit ($PDFOM = V_{BR}^2 / R_{ON}.A$) of ~ 400 MW/cm² comparable to some of the best reported values for field plated devices.

The breakdown behaviour in these devices was observed to be destructive and images of the devices post-breakdown have been shown in Fig. 4.8.

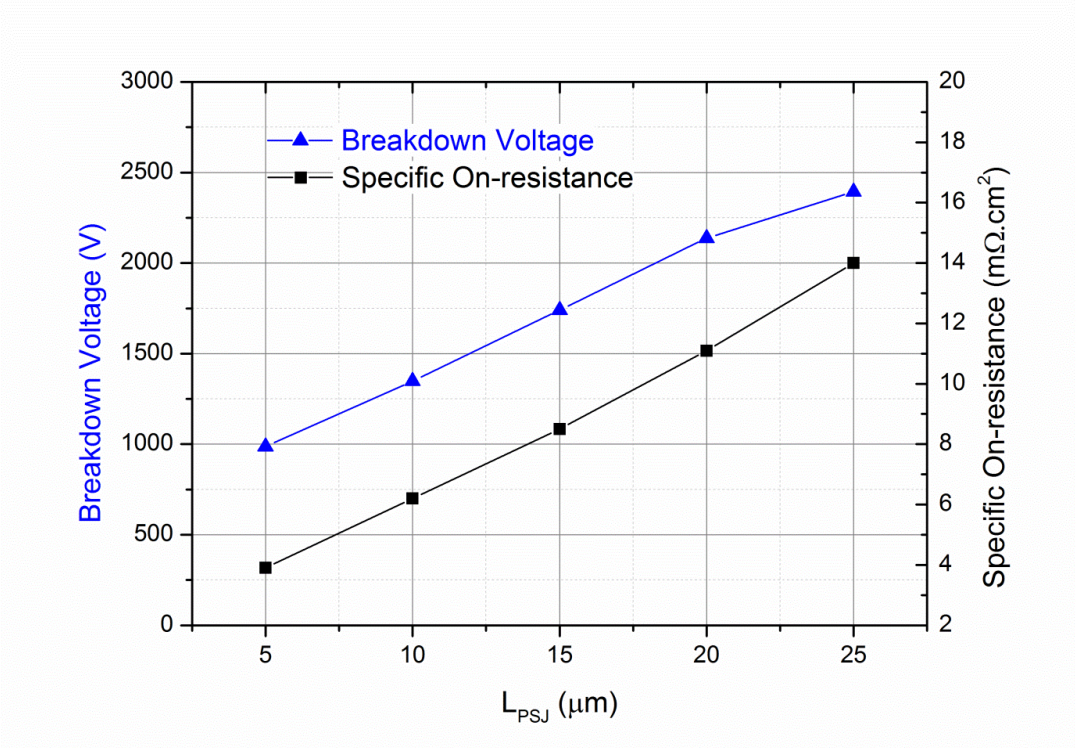


Figure 4.7 Breakdown Voltage (V_{BR}) and Specific On-state Resistance ($R_{ON}.A$) versus L_{PSJ}

Breakdown measurements were also performed under grounded substrate conditions. In this configuration, substantial lowering of V_{BR} was observed suggesting a vertical nature of the breakdown that was no longer governed by L_{PSJ} unlike under floating substrate conditions. Fig. 4.9 shows the breakdown characteristics of PSJ Diode with L_{PSJ} of 15 µm under the two conditions.

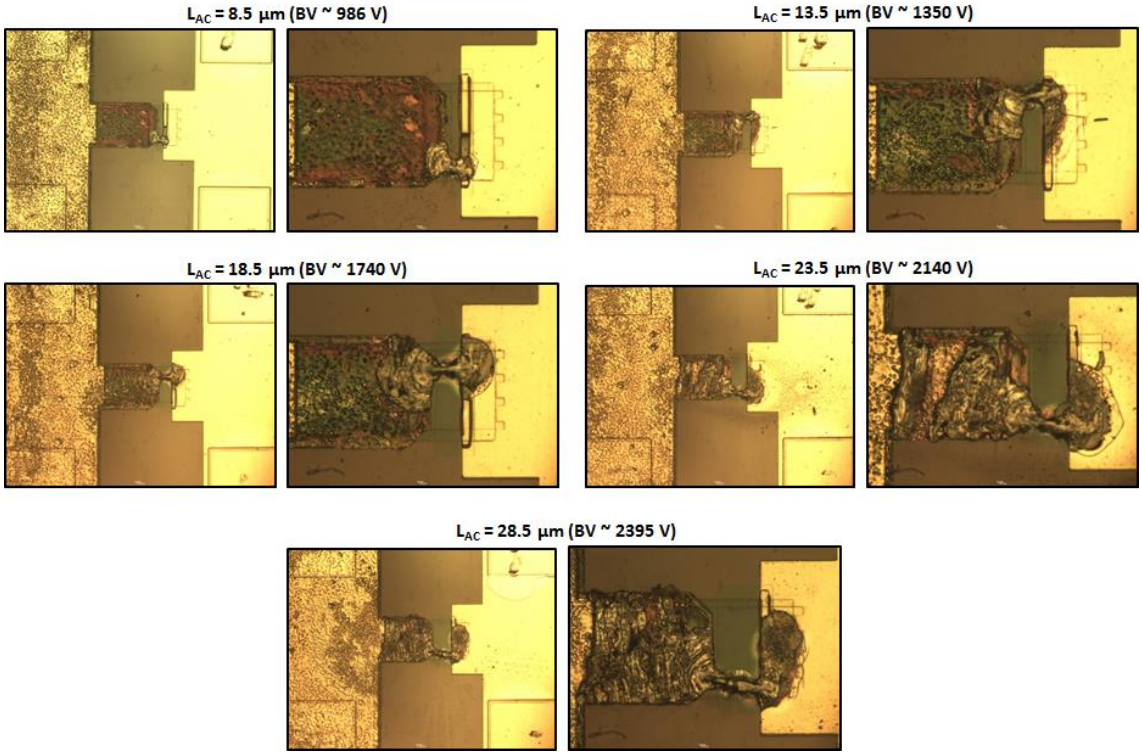


Figure 4.8 Images of the devices post-breakdown (L_{AC} = L_{PSJ} + 3.5 µm)

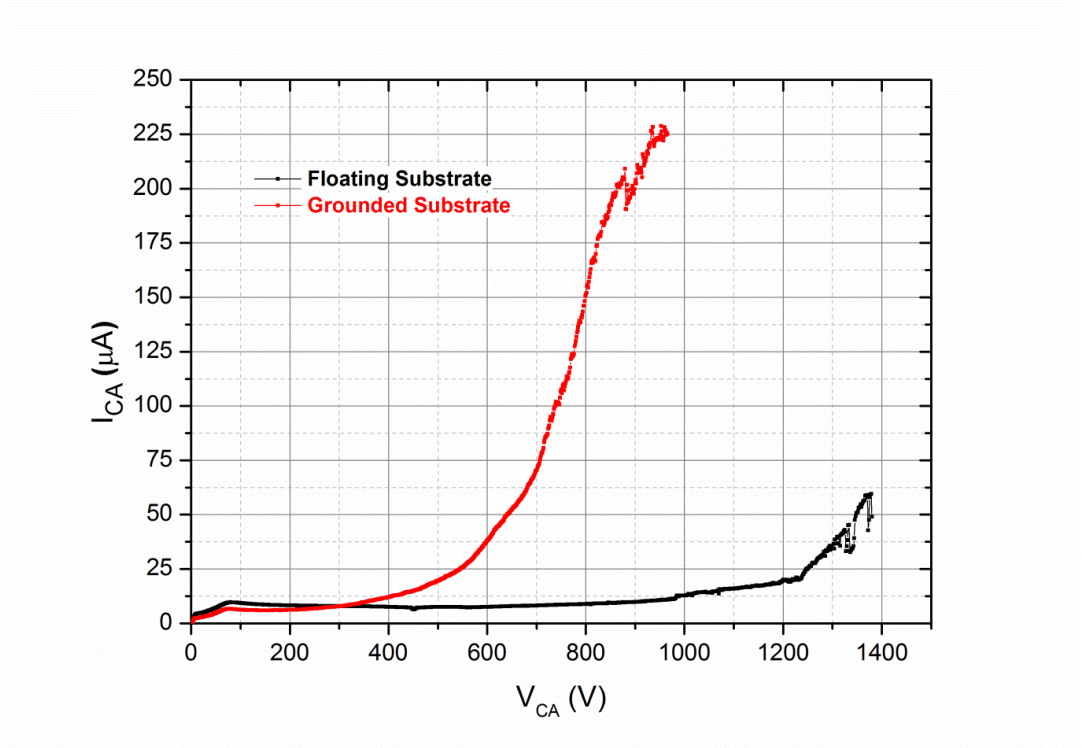


Figure 4.9 Reverse I–V characteristics of fabricated PSJ Diode with L_{PSJ} = 15 µm under floating and grounded substrate conditions

TCAD simulations were performed using Silvaco ATLAS, to gain insight into the breakdown mechanism under floating and grounded substrate conditions. The cross-section schematic of the simulated structure has been shown in Fig. 4.10. A PN junction diode configuration is sufficient to perform this simulation as PSJ Diode is a hybrid combination of a Schottky Barrier Diode and a PN junction diode, and the breakdown voltage is expected to be essentially sustained by the PSJ layer. The doping parameters and physical models that were included are the same as those used in breakdown simulation described in section 3.2. In the simulated structure Anode and Cathode electrodes make ohmic contacts to 2DHG and 2DEG respectively. The PSJ layer drift length was set as 5 μm. The condition of grounded substrate was simulated by adding a substrate electrode (ohmic) at the bottom of the structure within the simulation code.

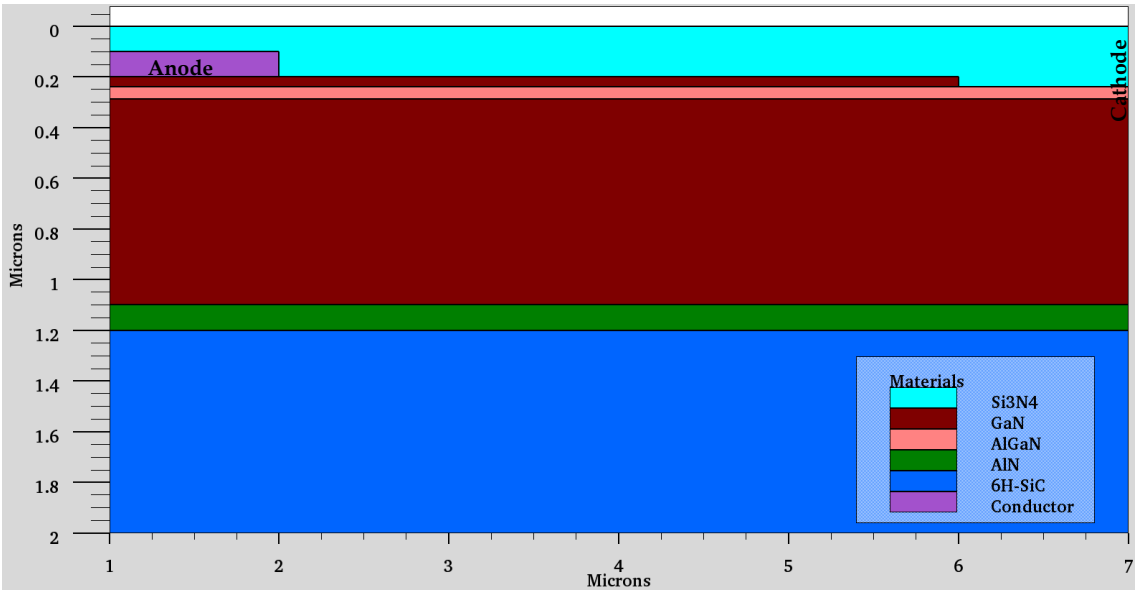
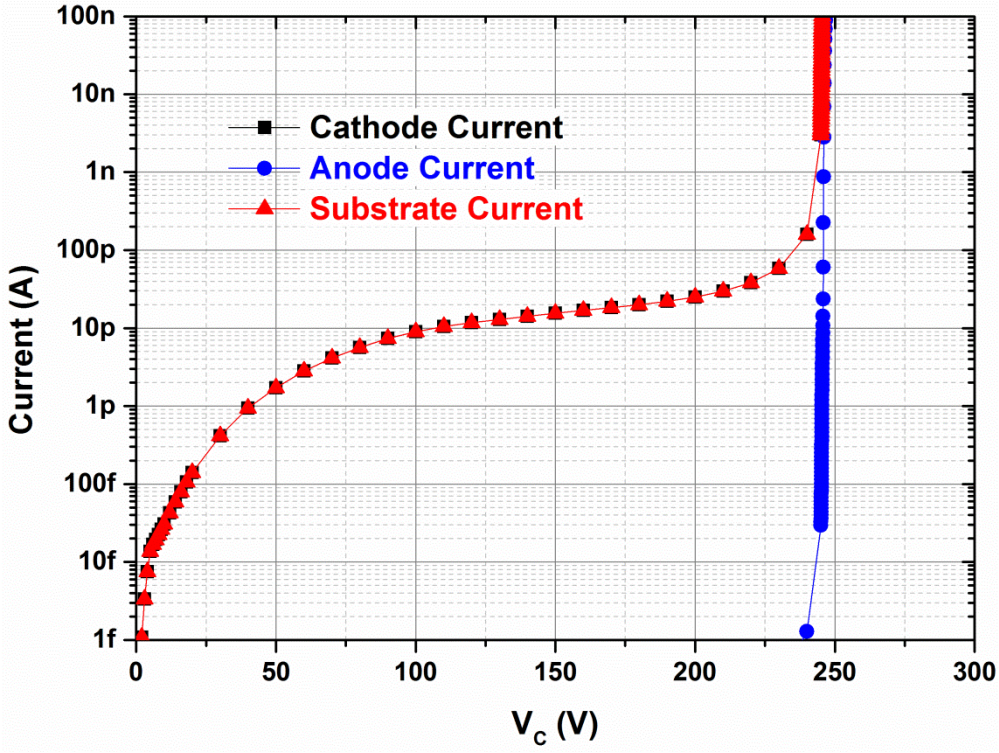


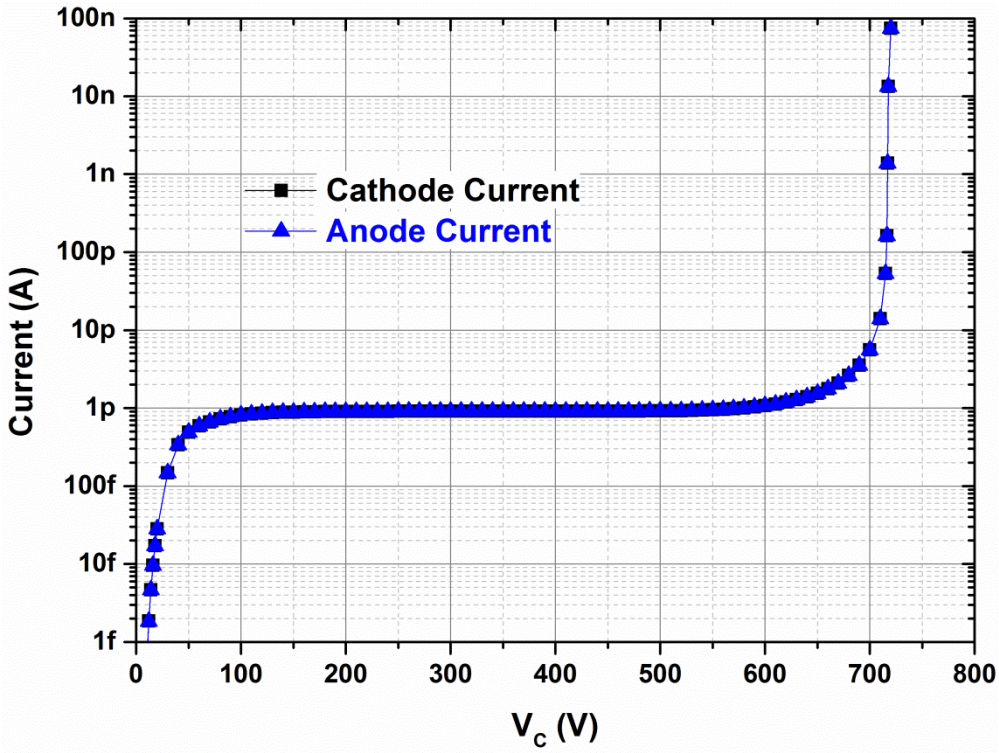
Figure 4.10 Simulated structure

The simulated breakdown characteristics under grounded (BV < 250 V) and floating substrate (BV ~ 700 V) conditions have been shown in Figs. 4.11 (a)-(b) respectively. When the substrate is biased at 0 V, the Cathode and substrate currents are identical confirming a vertical path of the reverse leakage current

from Cathode to substrate as well as the region for device breakdown eventually.



(a)



(b)

Figure 4.11 Simulated breakdown characteristics under (a) Grounded Substrate (b) Floating Substrate conditions

Under floating substrate conditions, there is only one path for the reverse leakage from Cathode to Anode and the two currents therefore are identical as can be seen in Fig. 4.11 (b).

Electric field distribution and field profile along the AlGaN/GaN interface have been shown in Fig. 4.12 (a) and (b) for the two conditions at V_{CA} = 220 V.

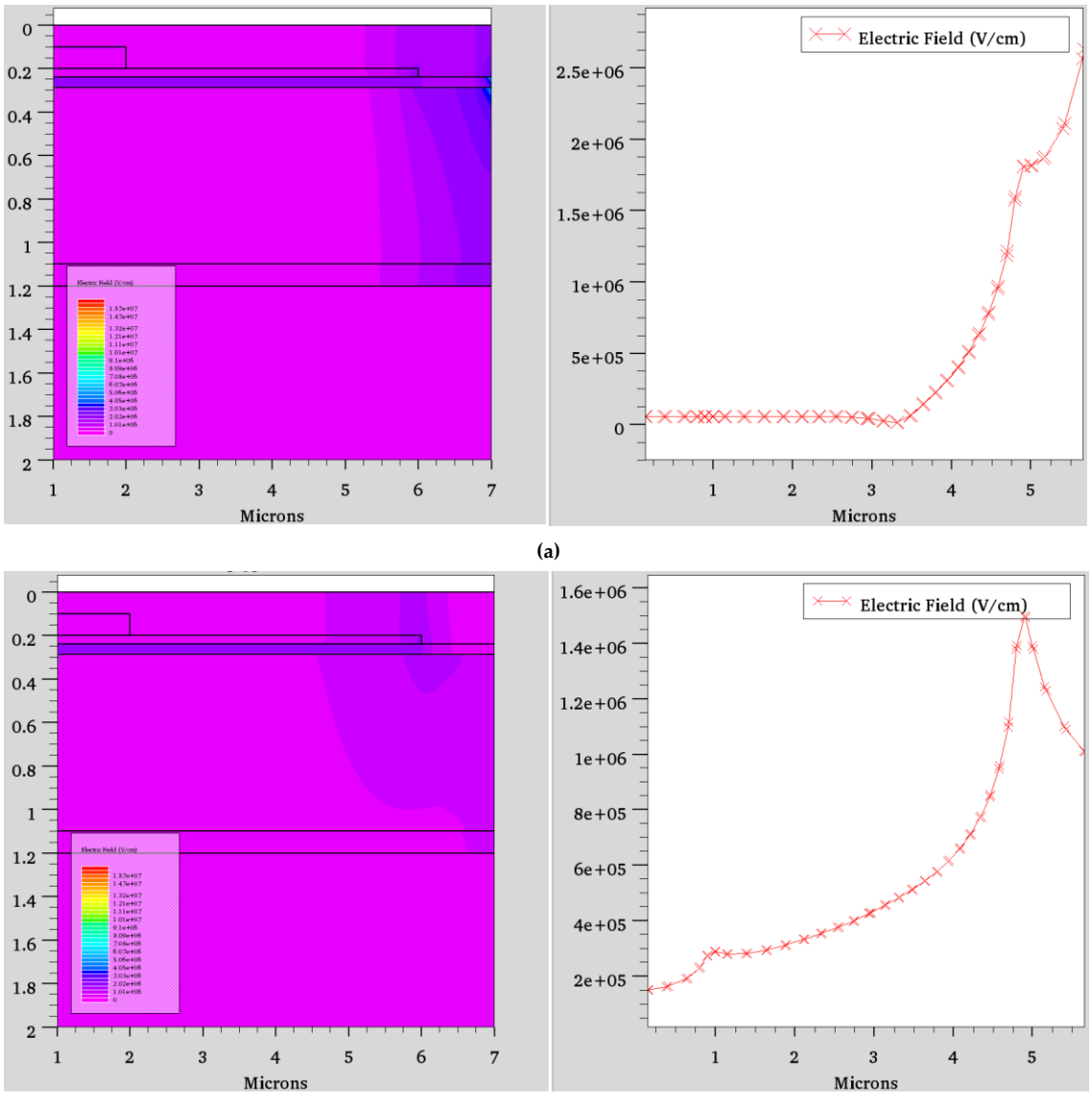


Figure 4.12 The distribution of electric field and its profile along the lower AlGaN/GaN interface at V_{CA} = 220 V (a) Grounded Substrate (b) Floating Substrate

When substrate is grounded, the Cathode potential primarily drops vertically across the GaN buffer region (thickness < 1 μm) with electric field crowding at

the Cathode electrode and the device experiences breakdown at V_{CA} or V_{CSUB} ~ 245 V (as Anode and substrate are both maintained at 0 V).

Under floating substrate conditions, the potential primarily drops laterally across the PSJ layer (Drift length = 5 μm). Therefore a higher Cathode voltage can be applied before the magnitude of the electric field reaches critical electric field at the Cathode, initiating device breakdown at ~ 700 V.

Under this condition, as V_{CA} is increased, uniformly distributed electric field profile (with peaks at edges of Anode, PSJ layer and Cathode) along the PSJ layer is obtained at the AlGaN/GaN interface, as shown in Fig. 4.13. It is apparent that the field at Cathode approaches the critical electric field as V_{CA} is increased further and the device goes into breakdown at V_{CA} ~ 700 V.

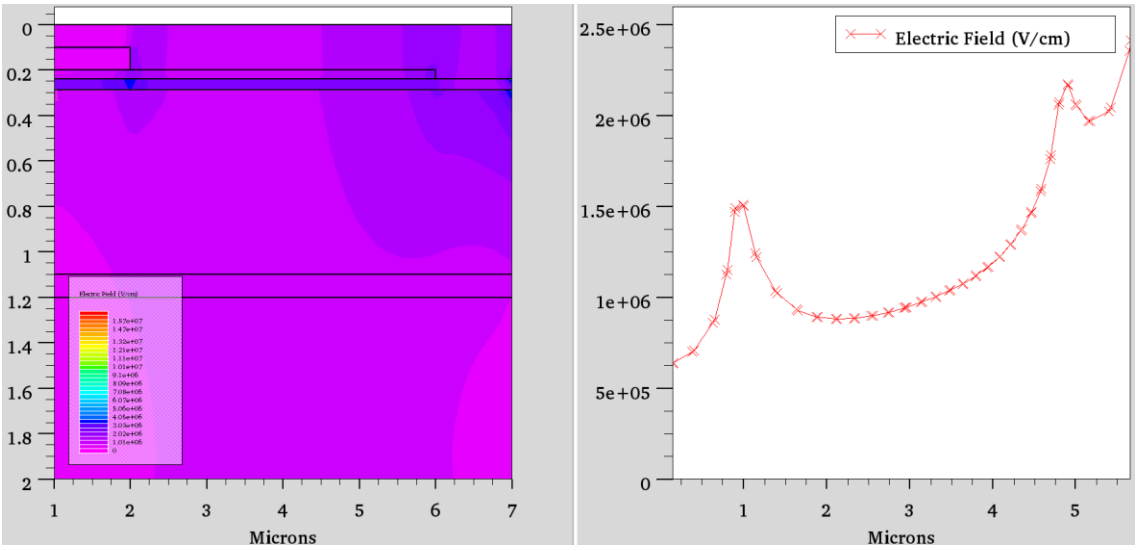


Figure 4.13 The distribution of electric field and its profile along the lower AlGaN/GaN interface at V_{CA} = 600V, under floating substrate conditions

4.2.2.3 Capacitance Voltage Characteristics

Figs. 4.14 (a)-(b) show simplified cross-section schematics of conventional SBD with-out field plate and PSJ diodes, also illustrating the effective Anode to Cathode capacitance intrinsic to the two structures.

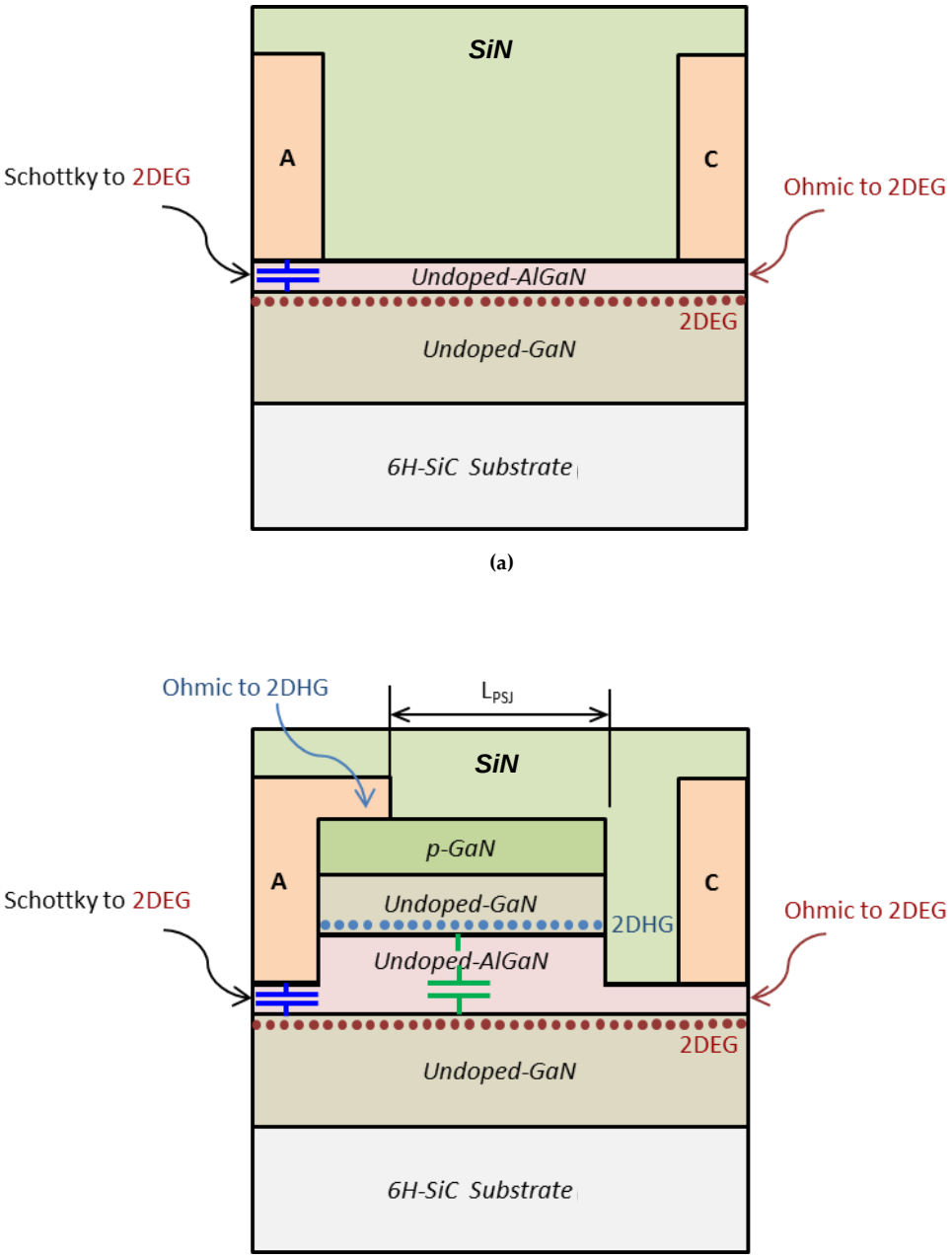


Figure 4.14 Cross-section schematics illustrating the effective Anode to Cathode capacitance of (a) Conventional SBD (b) PSJ Diode

Small-signal Capacitance Voltage (CV) measurements at 250 kHz were performed using B1505A on conventional SBD (L_{AC} = 8 µm) and PSJ Diodes (L_{AC} = 8.5 µm and L_{PSJ} = 5 µm), and have been shown in Fig. 4.15.

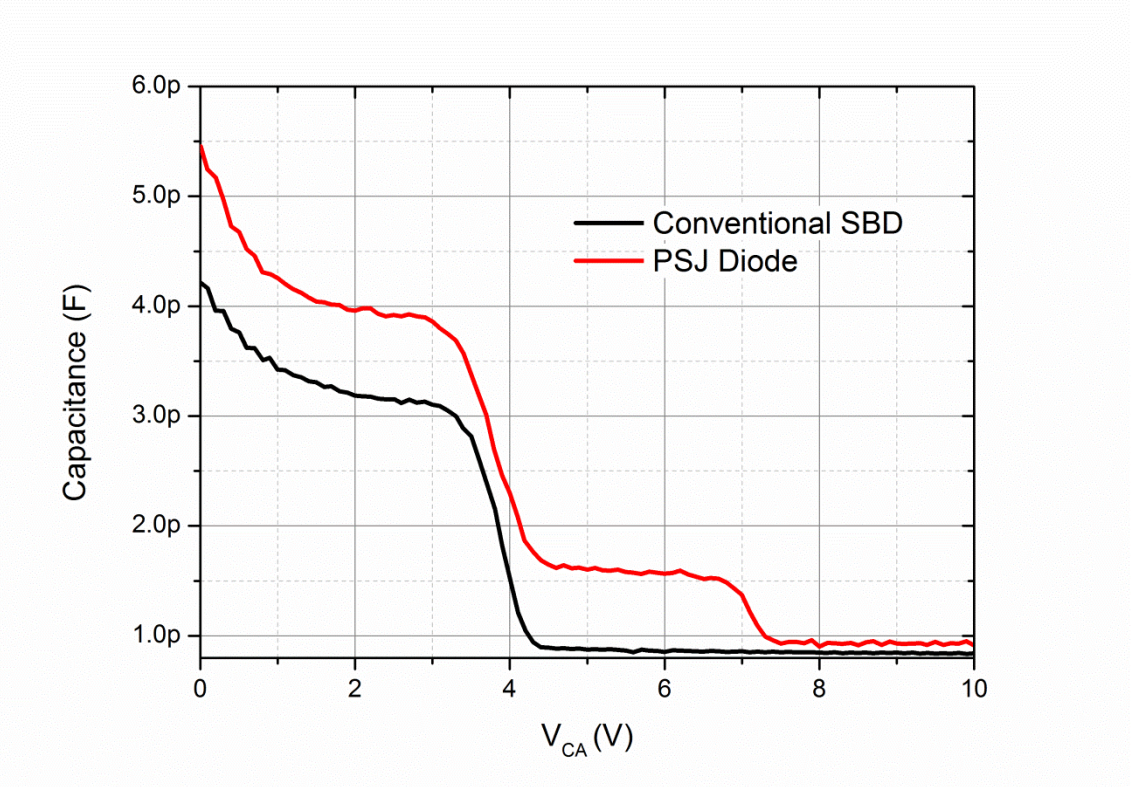


Figure 4.15 Small-signal capacitance measured at 250 kHz for conventional SBD and PSJ Diode

As Cathode to Anode potential (V_{CA}) increases, 2DEG under the Schottky Anode is depleted at V_{CA} ~ 4.5 V for the conventional SBD. Integration of the CV data from 0 - 4.5 V provides the total depleted charge indicating an approximate 2DEG density (ignoring background doping) at the AlGaN/GaN interface of ~ 1.6 x 10^{13}/cm^2 [3]. The profile of electron density was also extracted from the CV data and has been plotted in Fig. 4.16. The peak electron density at the AlGaN/GaN interface was extracted as ~ 3 x 10^{20}/cm^3.

As shown in Fig. 4.15, higher capacitance has been measured for PSJ diode. This could be attributed to the presence of additional parallel capacitance of the PSJ layer formed by 2DHG and 2DEG, also indicated by a two-stage depletion process. For the PSJ diode under measurement, the depletion occurs initially under the Schottky interface at V_{CA} ~ 4.5 V just like in the case of the conventional SBD, as this region is identical in the two types of devices. This is followed by depletion in the ohmic region of the anode electrode at V_{CA} ~ 7.5 V.

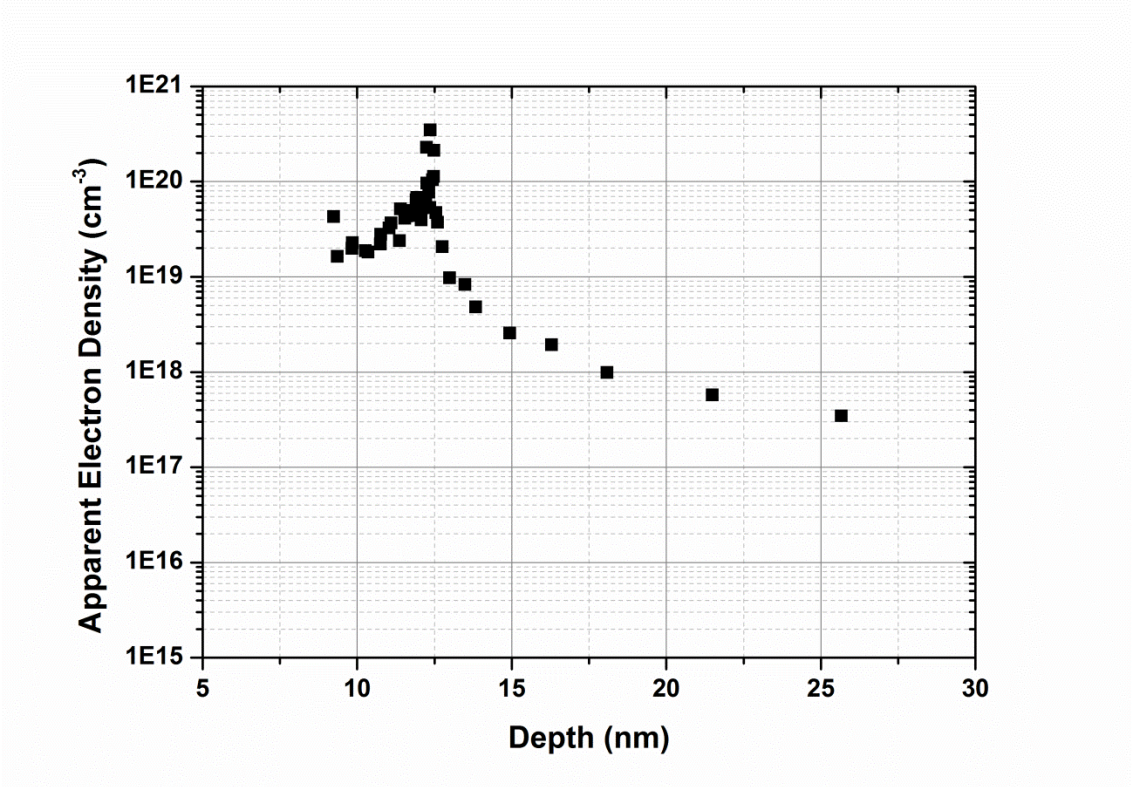


Figure 4.16 Profile of the electron density in the AlGaN/GaN heterostructure, extracted from CV measurement of a conventional SBD

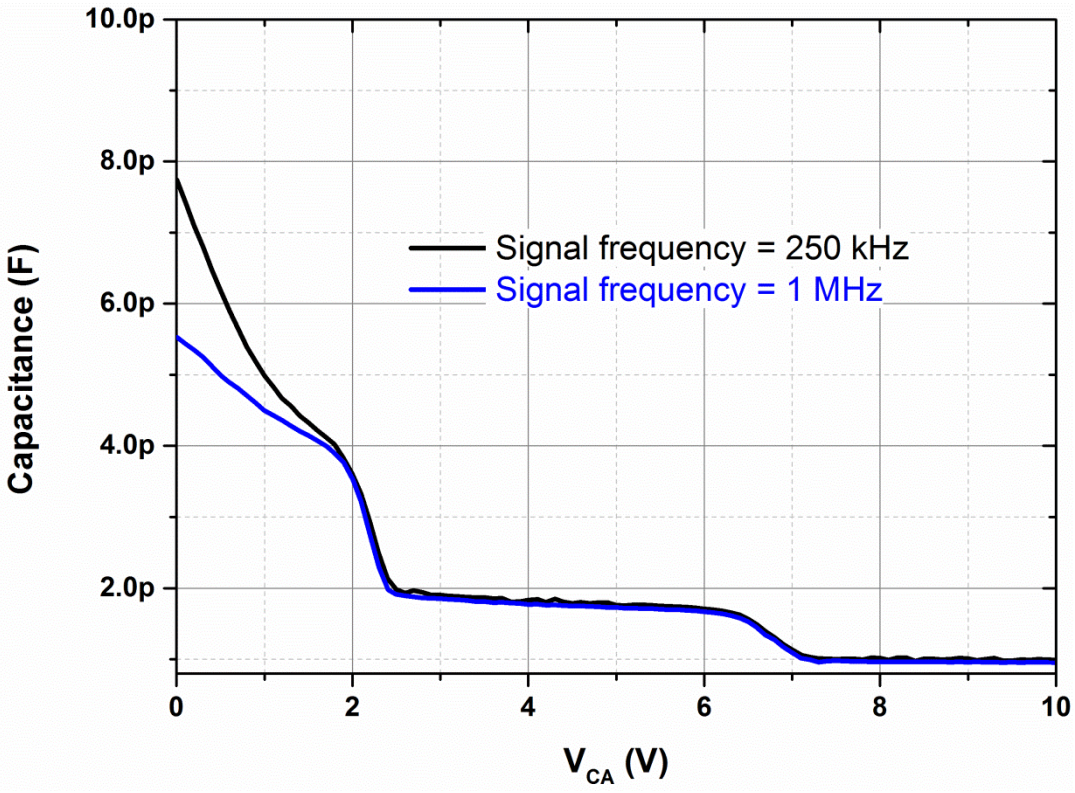


Figure 4.17 Small-signal capacitance of a PSJ Diode (L_{PSJ} = 5 μm) measured at 250 kHz and 1 MHz

Fig. 4.17 shows the measured capacitance of a PSJ Diode (L_{PSJ} = 5 μm) for two different signal frequencies of 250 kHz and 1 MHz. At a signal frequency of 1 MHz, the capacitance at V_{CA} = 0 V reduces from 7.8 pF to 5.5 pF and leads to a relative flattening of the CV curve in the range of 0 V - 2 V. There is no change in the CV curve in the remaining range of V_{CA}.

The behaviour indicates a presence of defects at the Anode - etched AlGaN interface. These defects could be formed due to ICP etching of the AlGaN layer during device-processing, and can act as trap states. During the CV measurement, the trapped electrons are able to respond to low-frequency signals and the response becomes weaker as the signal frequency for capacitance measurement is increased. Therefore a lower capacitance and flattening of the CV curve is observed at 1 MHz [4]. This variation in the measured capacitance also suggests that the magnitude of the 2DEG density estimated from CV integration (signal frequency = 250 kHz) is higher than the actual electron density at the AlGaN/GaN interface. No change is observed in the capacitance due to the PSJ layer (no etch related defect generation in this region of the structure) and the measured capacitance at 250 kHz and 1 MHz are therefore identical.

Fig. 4.18 shows small-signal CV measurements of PSJ diodes with respect to L_{PSJ}. All devices in this work have active width of 50 μm. Consistent increase in capacitance under the PSJ Layer was observed with increase in L_{PSJ} as shown in Fig. 4.19 in which the region of the graph shown in Fig. 4.18 in the voltage range of 2.5 V– 6.5 V has been zoomed into.

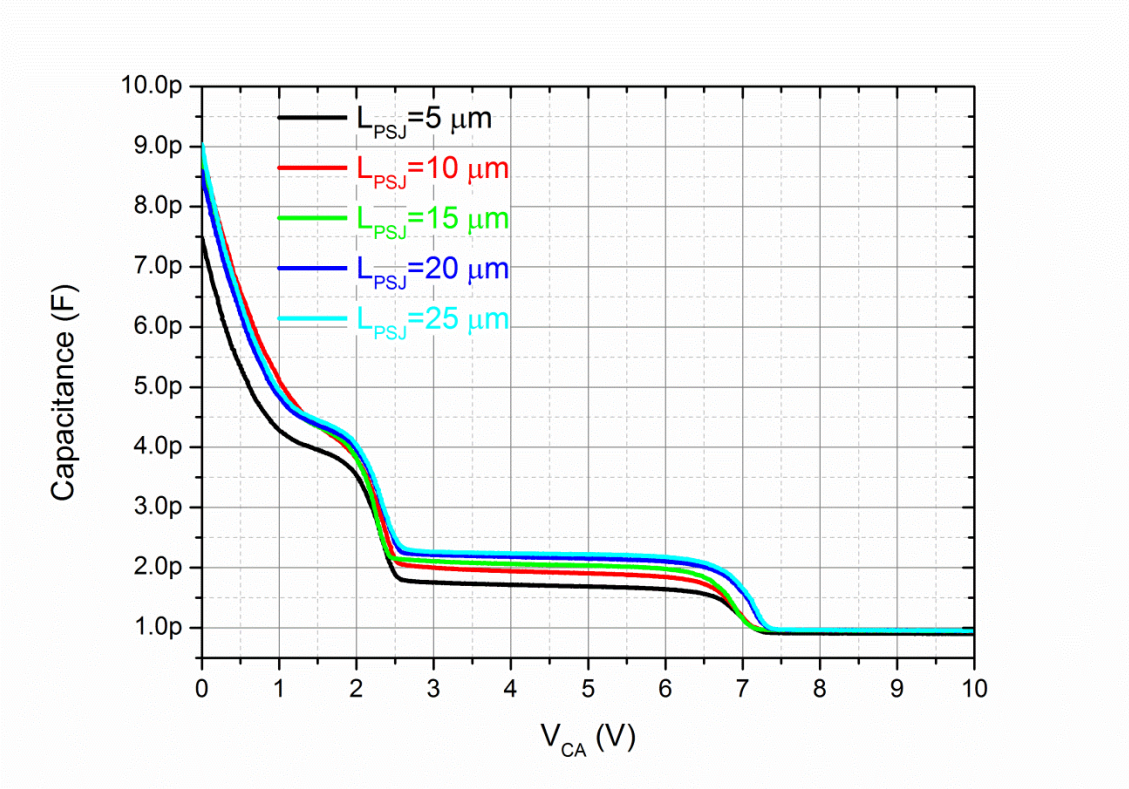


Figure 4.18 Small-signal capacitance measured at 250 kHz for PSJ Diodes with various L_{PSJ}

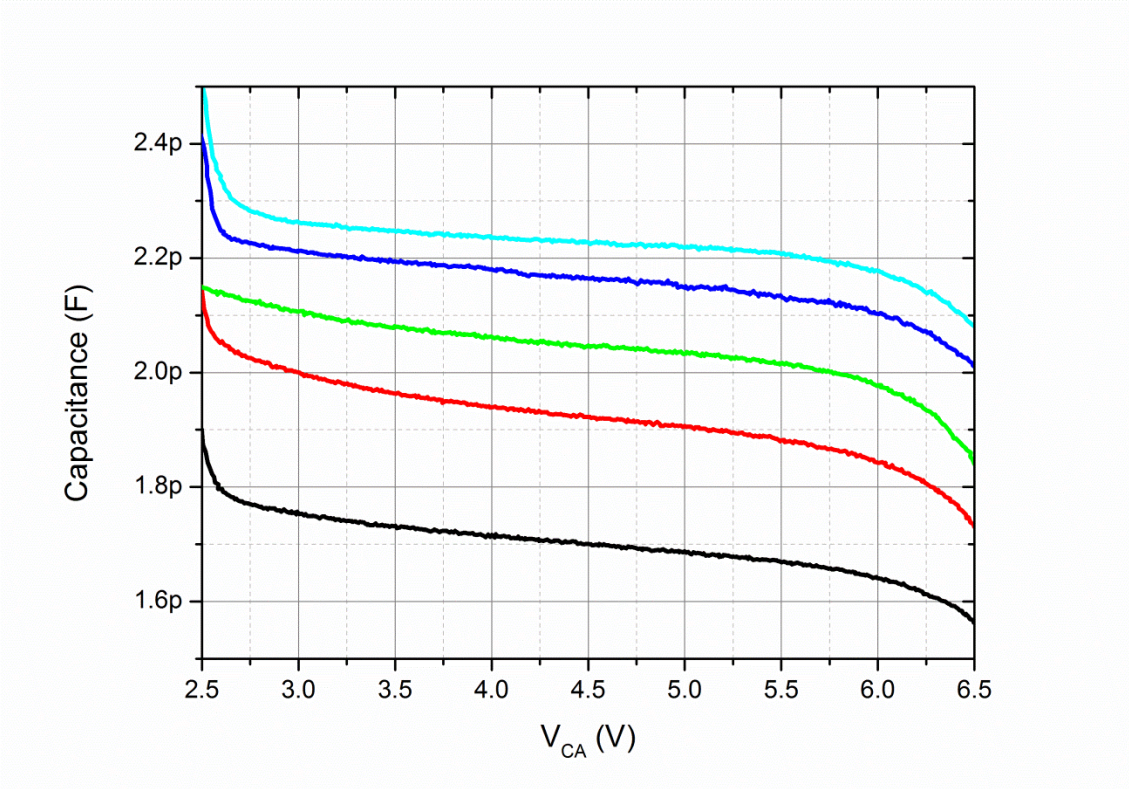


Figure 4.19 Small-signal capacitance measured at 250 kHz for PSJ Diodes with various L_{PSJ} (zoomed-in)

Fig. 4.20 shows the PSJ layer capacitance measured at V_{CA} = 3 V versus L_{PSJ} for a larger sample size of PSJ diodes. Although an increase in capacitance is observed, the overall trend appears to be non-linear. It has to be noted that the magnitude of the capacitance due to the 2DHG and 2DEG depends not only on the length of the PSJ layer (from cathode side edge of the anode electrode to the edge of the p-GaN layer), but the capacitor formed by 2DHG and 2DEG in the region directly under the Anode metal - p-GaN interface also needs to be considered. But even accounting for that cannot explain the change in magnitude of the capacitance with respect to an increase in PSJ length, and the increase in magnitude observed experimentally is rather smaller than expected. This behaviour was studied using TCAD simulations (Silvaco ATLAS) to gain further insight.

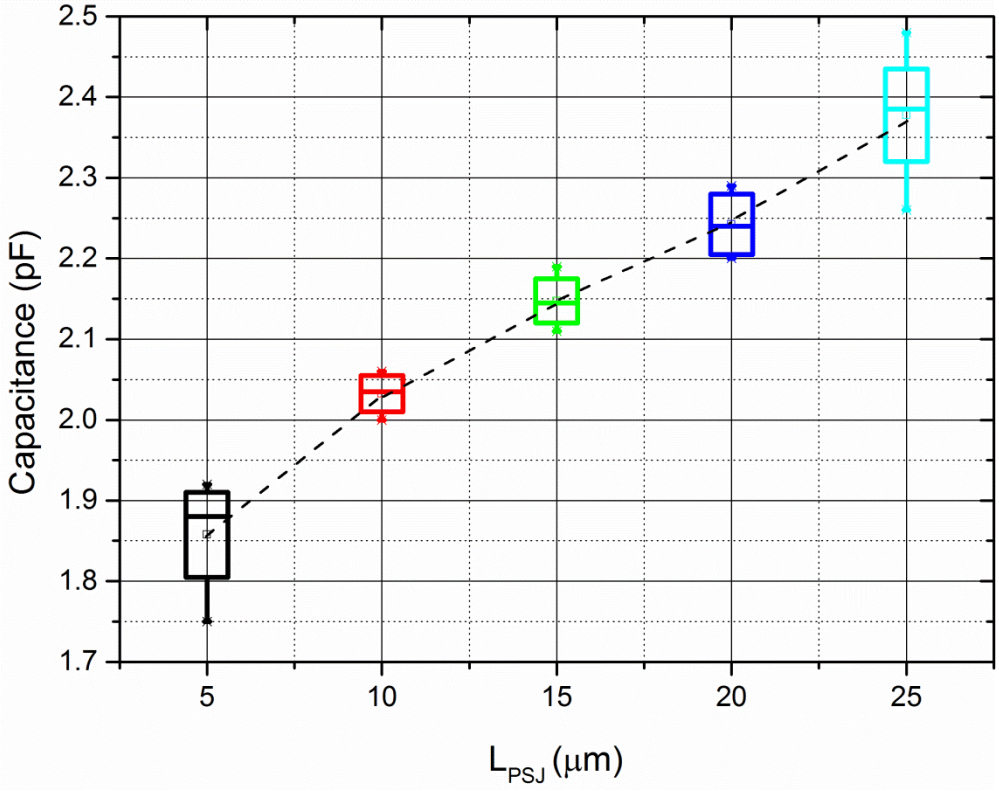


Figure 4.20 Small-signal PSJ Layer capacitance measured at 250 kHz and V_{CA} =3 V for PSJ Diodes versus L_{PSJ}

The simulated geometry was identical to that of the actual device structure and the physical models that were included are the same as those used in studying the transfer characteristics of PSJ transistors, described in section 3.2. No trapping effects were considered. Simulated Anode-Cathode capacitance at 1 MHz for PSJ Diode with L_{PSJ} = 25 μm has been shown in Fig. 4.21.

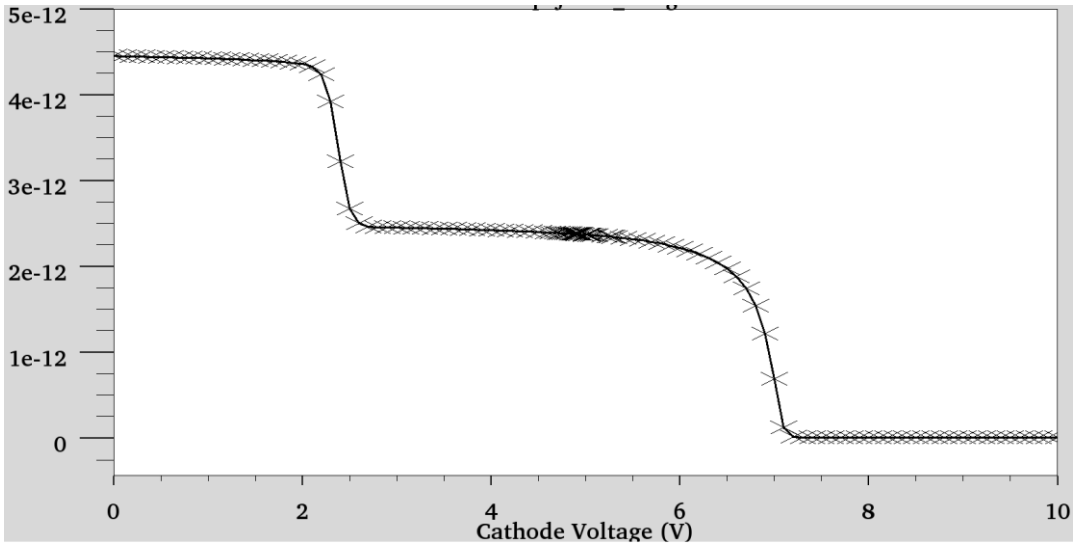
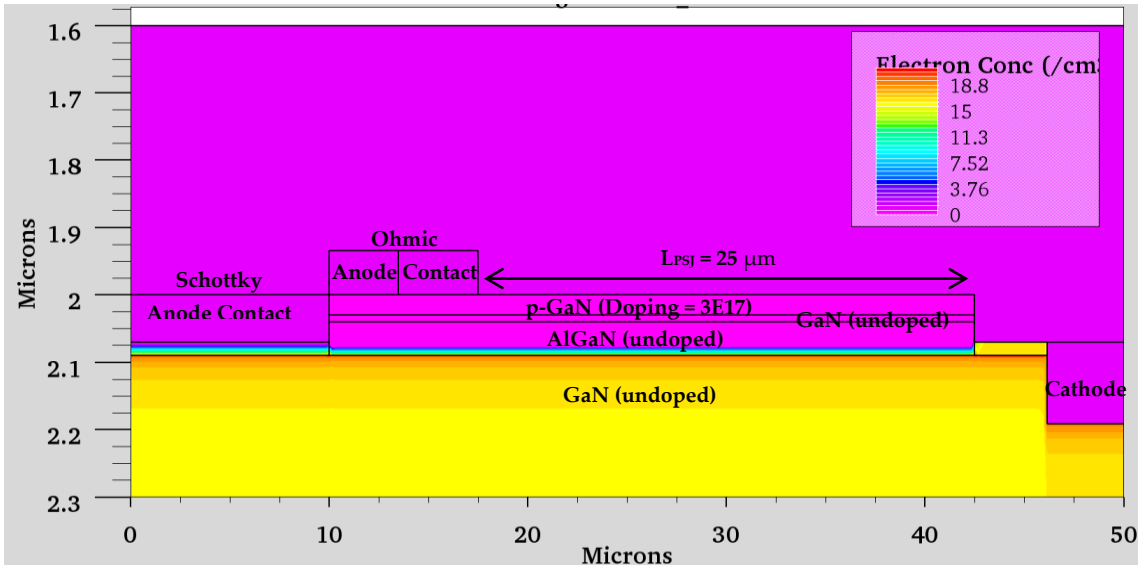
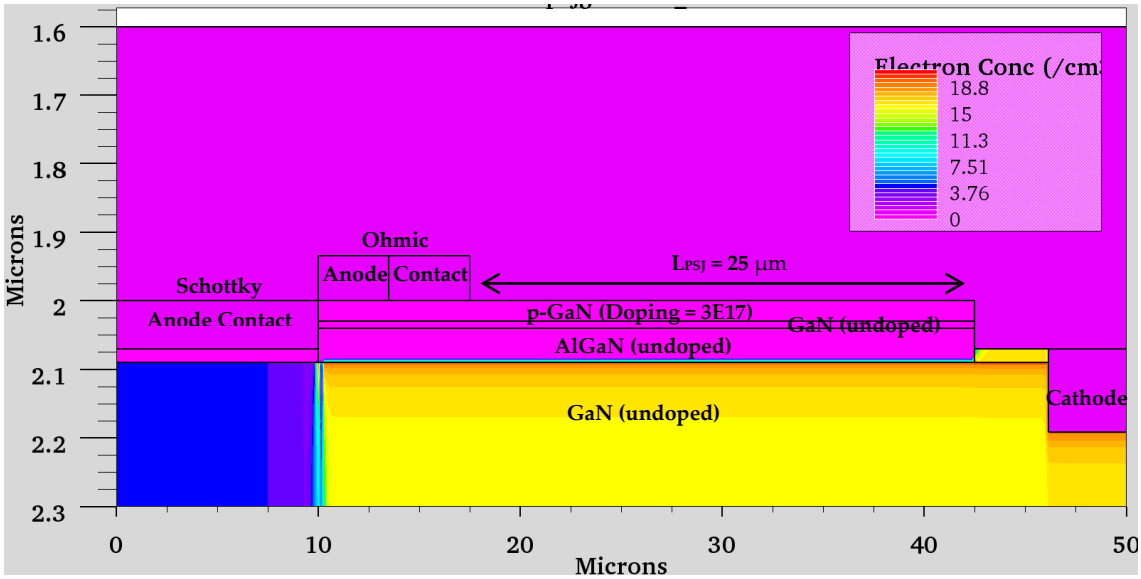


Figure 4.21 Simulated Anode-Cathode capacitance at 1 MHz for PSJ Diode with L_{PSJ} = 25 μm

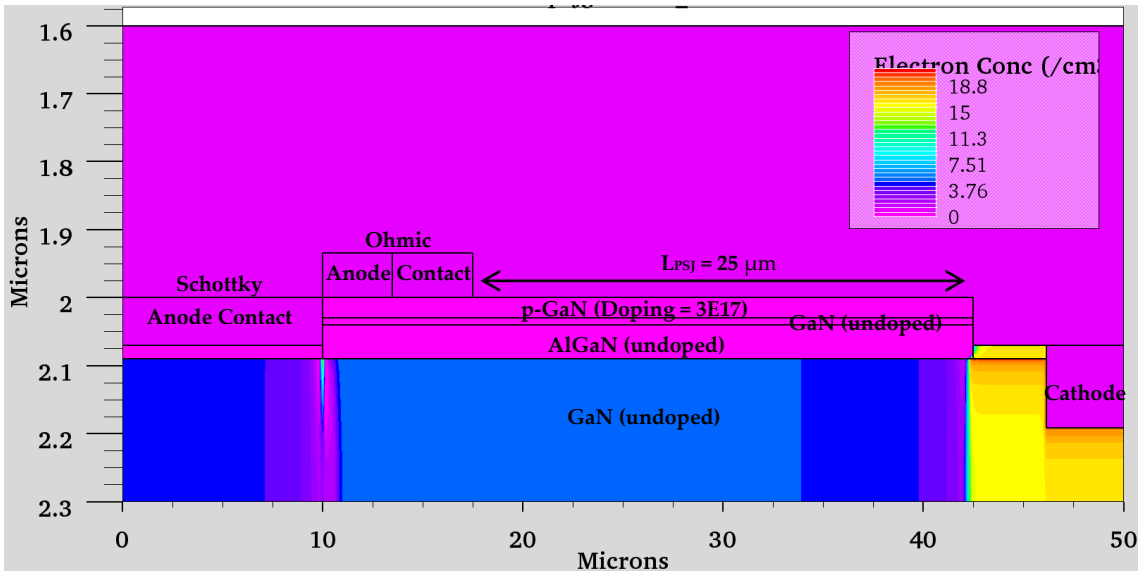
The simulation results conform well to the experimental results, indicating a two-stage depletion behavior. The electron concentration within the structure under various biasing conditions of Cathode-Anode voltage (V_{CA}) has been depicted in Figs. 4.22 (a)-(c). Anode contact to the p-GaN layer was defined as ohmic. The objective of this exercise was to confirm that the two-stage depletion behaviour is caused due to an initial depletion of the 2DEG under the Schottky contact followed by depletion of 2DHG and 2DEG in the double heterostructure as V_{CA} is increased further, and the same was confirmed in simulation.



(a)



(b)



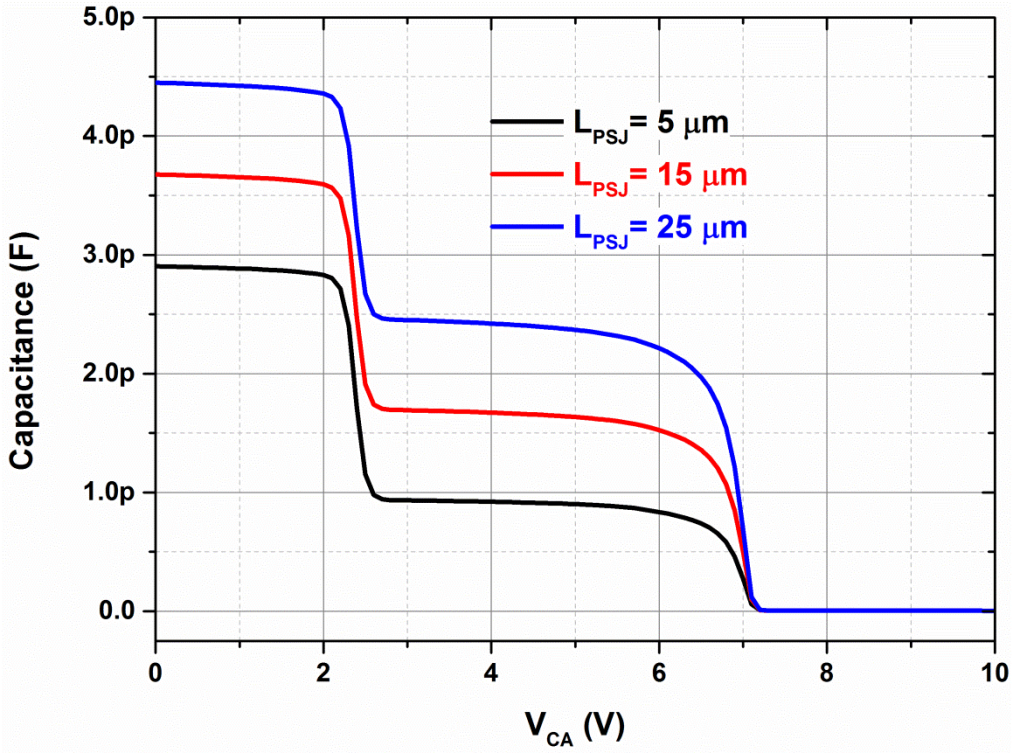
(c)

Figure 4.22 Electron concentration in a PSJ Diode with L_{PSJ} = 25 µm at (a) V_{CA} = 0 V (b) V_{CA} = 4 V (c) V_{CA} = 8 V

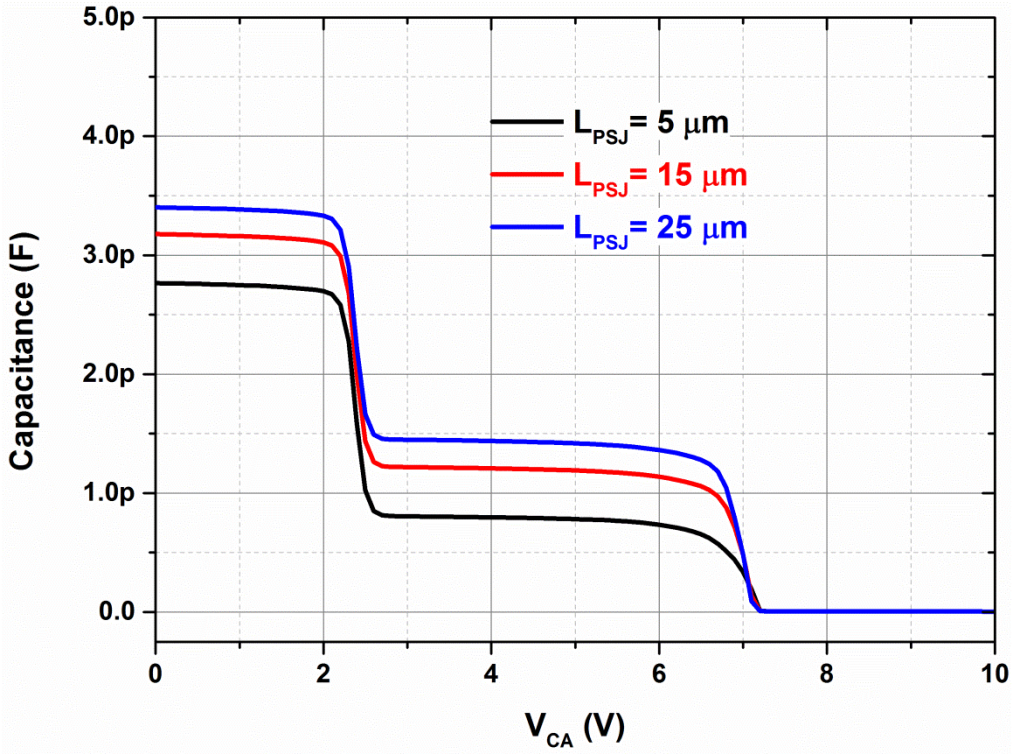
Structures with various PSJ lengths were simulated to study the impact on the magnitude of the capacitance and especially the magnitude of the capacitance due to the PSJ layer. It was observed that the capacitance increased linearly with an increase in PSJ layer, unlike what was observed experimentally. No dependence could be observed on the doping density in the p-GaN layer.

In reality, obtaining a good ohmic contact to p-GaN layer is an extremely challenging task and it was observed during process development as well as on the actual fabricated devices that the p-contact showed quasi-ohmic behaviour at best. Therefore simulations were performed under perfectly ohmic as well as quasi-ohmic conditions to account for this behaviour by altering the work-function of the metal electrode on the p-GaN surface. The results obtained under the two conditions have been summarised in Figs. 4.23 (a) – (b).

Fig. 4.24 shows the simulated PSJ layer capacitance at V_{CA} = 3 V versus L_{PSJ} for ohmic and quasi-ohmic conditions. When the Anode contact is defined as perfectly ohmic, the PSJ layer capacitance increases linearly with the length of the PSJ layer. Whereas defining a quasi-ohmic contact leads to a non-linear increase in capacitance with PSJ length and tends to saturate as the PSJ length approaches 25 μm. The simulation results appear to match the experimentally observed results. Fig. 4.25 shows the hole concentration in a PSJ Diode with L_{PSJ} = 25 μm at V_{CA} = 0 V under the two simulation conditions.



(a)



(b)

Figure 4.23 Simulated Anode-Cathode capacitance at 1 MHz for PSJ Diodes (a) Ohmic p-contact (b) Quasi-ohmic p-contact

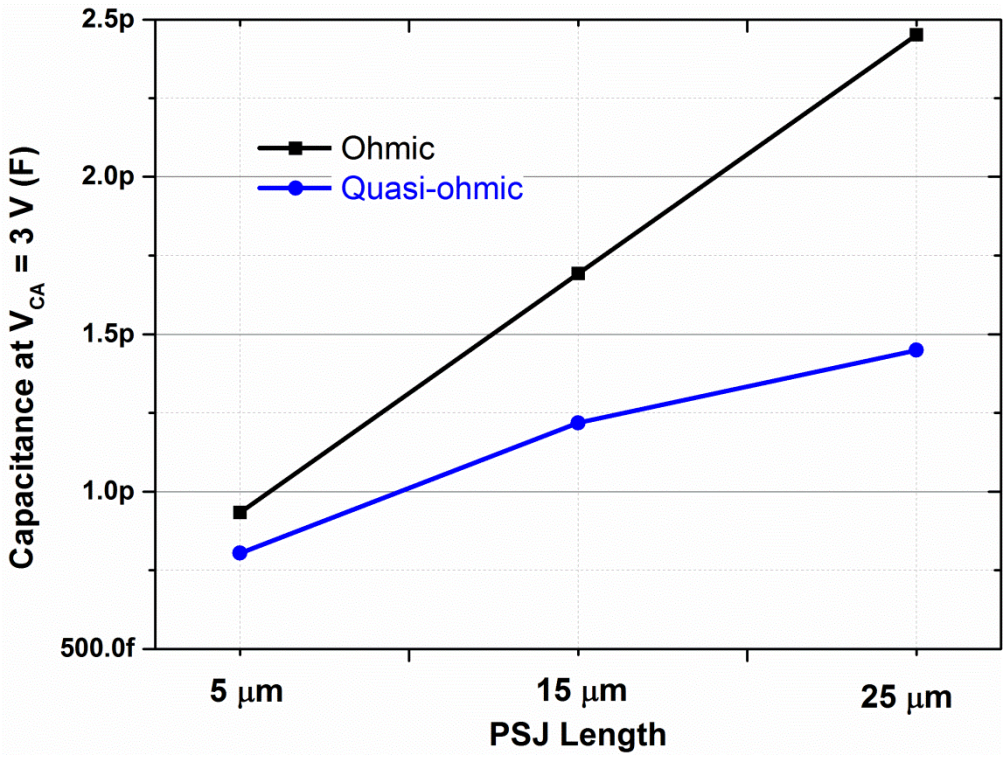
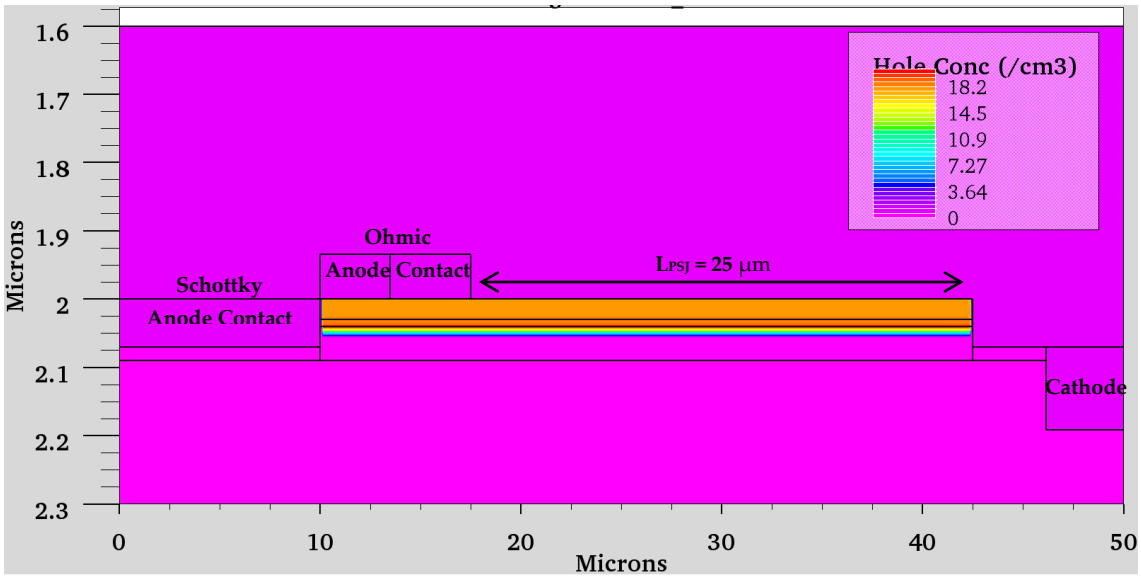
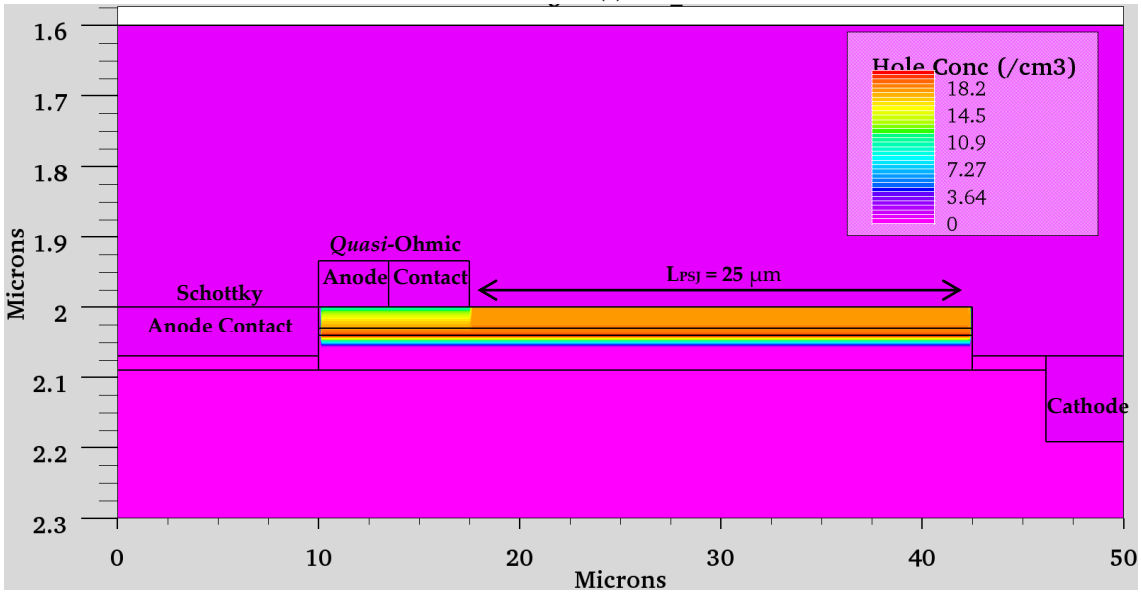


Figure 4.24 Simulated capacitance at V_{CA}=3 V versus L_{PSJ}

Fig. 4.26 shows the small-signal CV characteristics of a PSJ Diode, with V_{CA} voltage swept from 0 V - 10 V and from 10 V- 0 V in succession. A hysteresis-like behaviour has been observed primarily under the Schottky region of the Anode. This could be attributed to crystallographic defects extending from GaN layer to the Ni/AlGaN interface [5]. Considering that the behaviour is more prominent under the Schottky region of the Anode, ICP etching of the region during the PSJ layer mesa etch could also be a potential contributor as the etching process could have led to or increased crystallographic damage of the AlGaN surface under the Schottky metal and could thereby induce the observed behaviour.



(a)



(b)

Figure 4.25 Hole concentration in a PSJ Diode with L_{PSJ} = 25 μm at V_{CA} = 0 V (a) Ohmic contact on PSJ layer (b) Quasi-ohmic contact on PSJ layer

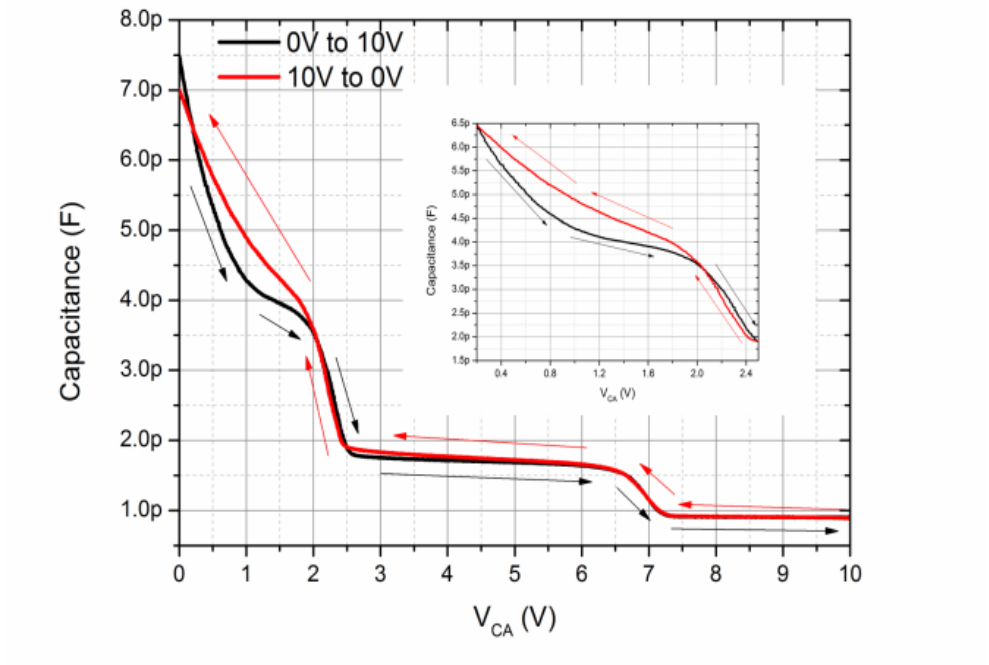


Figure 4.26 CV characteristics of PSJ Diode (L_{PSJ} =5 μm), with voltage V_{CA} swept from 0 V- 10 V and from 10 V - 0 V

4.2.2.4 Large Area PSJ Diodes

Forward I-V characteristics of three typical large area PSJ Diodes from the respective wafers have been shown in Fig. 4.27.

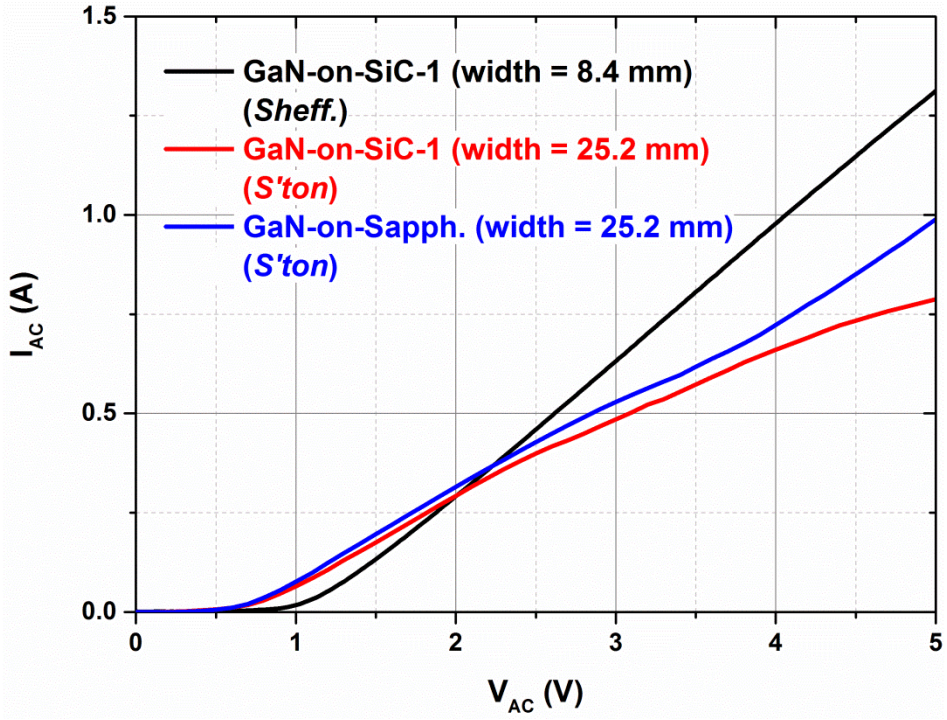


Figure 4.27 Measured forward I–V characteristics of large area PSJ Diodes (refer to Table 4.1)

The effective width of the measured devices has also been indicated on the figure. It is apparent from Fig. 4.27 that compared to the devices fabricated at Southampton, the on-state characteristics are better for the devices processed at Sheffield with specific on-state resistance that is approximately five times smaller (considering the overall die-area of the devices). Another important observation is the change in the on-state resistance clearly visible on the GaN-on-Sapph. (S'ton) device, which is an indication of the PN diode in the hybrid structure that is beginning to conduct at V_{AC} of ~ 3.5 V. The differences observed in the on-state characteristics have been analysed in finer detail in a later section.

Reverse I-V characteristics of the same large area PSJ Diodes have been shown in Fig. 4.28.

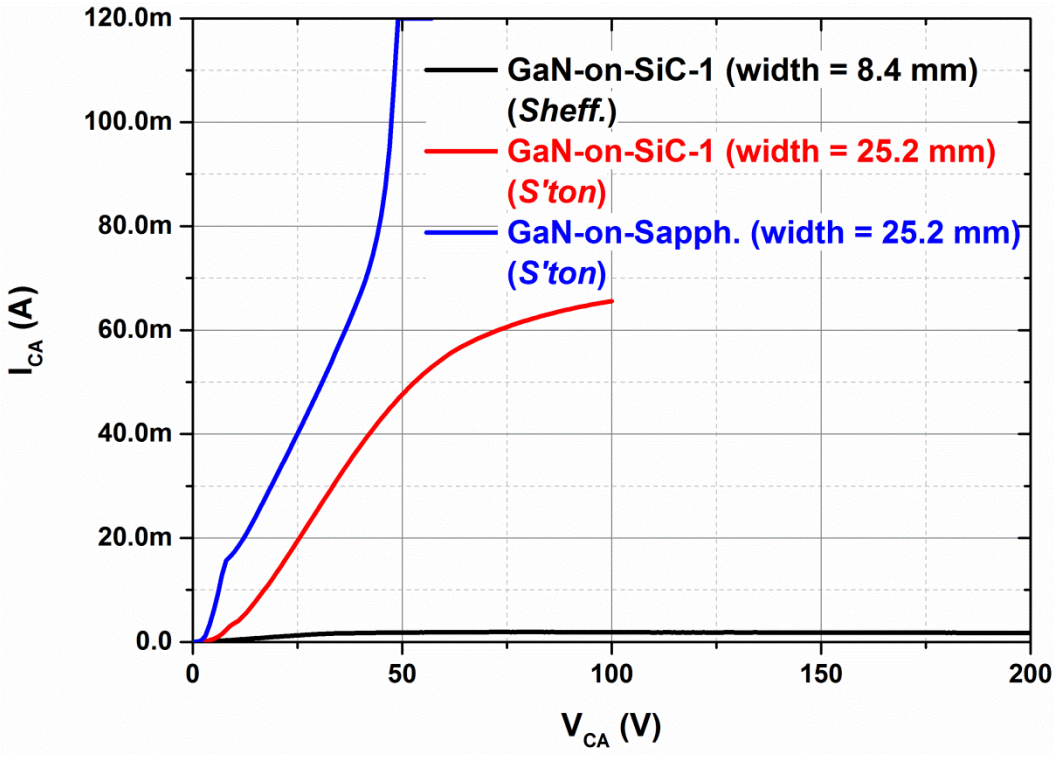


Figure 4.28 Measured reverse I–V characteristics of large area PSJ Diodes (refer to Table 4.1)

Abnormally high values of leakage current were detected for the PSJ Diodes processed at Southampton with devices on Sapphire substrate showing consistently higher leakage, whereas the magnitude of leakage current for the PSJ Diodes (1 mm x 0.8 mm) fabricated at Sheffield were ~ 1 mA at V_{CA} = 200 V.

Similar performance was observed for the PSJ HFETs as described in the next section.

4.3 Large Area PSJ HFETs

Several large area PSJ HFETs with various current handling capabilities were fabricated. Fig. 4.29 shows a simplified cross-section of a single cell in a large area multifinger PSJ HFET.

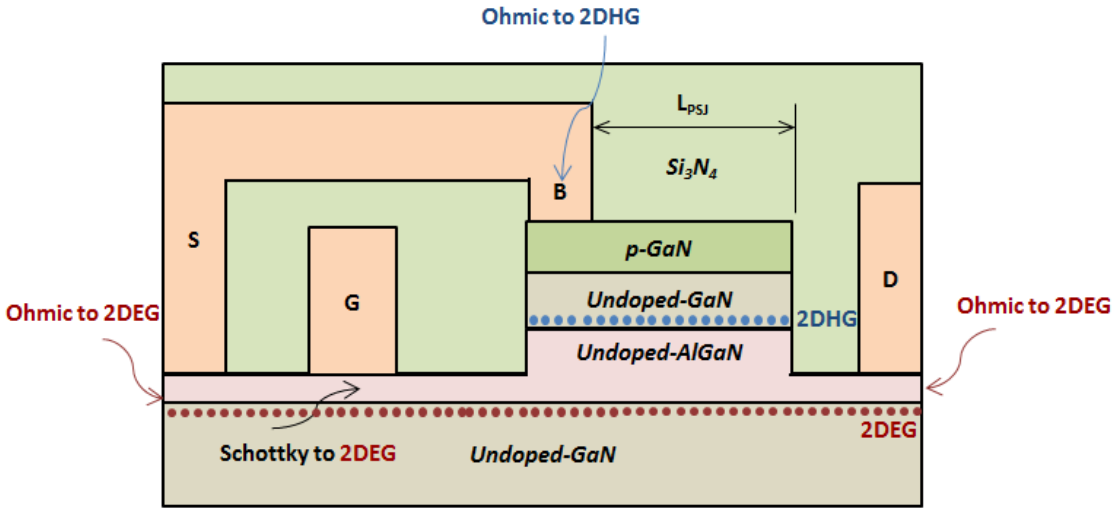
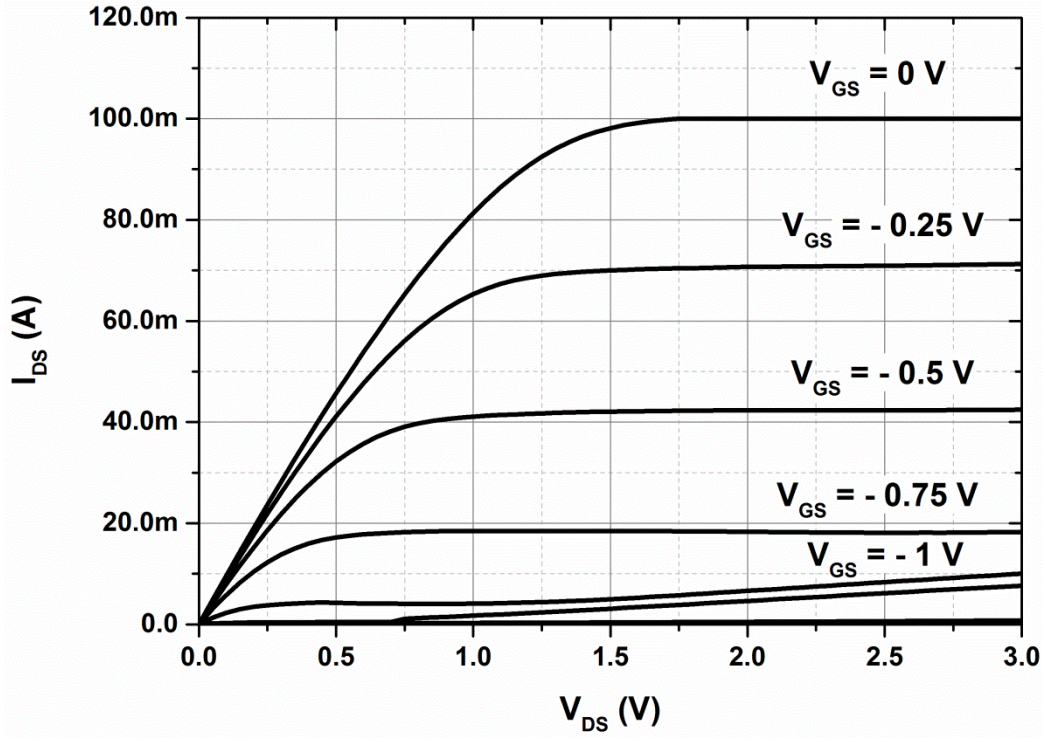


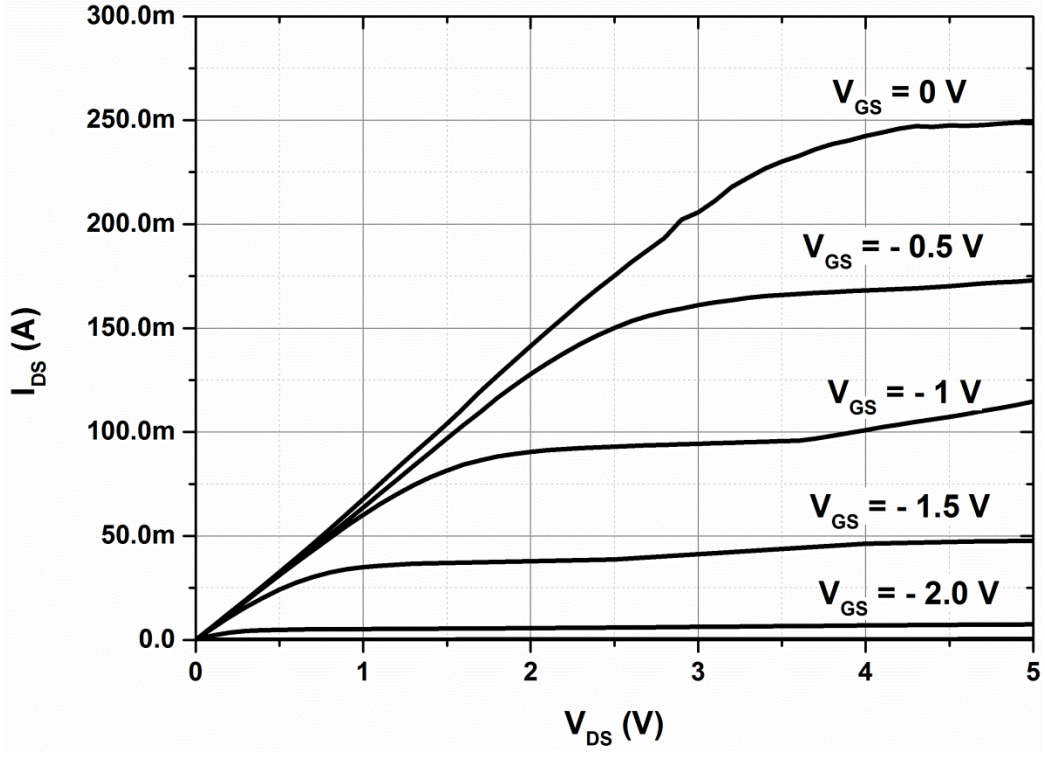
Figure 4.29 Cross-section schematic of a single cell in a large area PSJ HFET fabricated on 6H-SiC/Sapphire substrates

As described in the previous chapter, double metal process was used to connect the Source to Base electrode. The basic principle of operation and details of fabrication have also been discussed in Chapter 3. Shorting Source to Base in the structure in this manner can enable reverse conduction in PSJ HFET. This is achieved through the intrinsic diode formed between Source and Drain via the Base electrode. This unique feature of High Voltage PSJ HFETs has been discussed in in more detail in section 4.6.

The output characteristics of two large area multi-finger PSJ HFETs (effective width = 8.4 mm) fabricated on *GaN-on-SiC-1 (S'ton)* and *GaN-on-SiC-2 (Sheff.)* respectively have been shown in Figs. 4.30 (a) - (b).



(a)



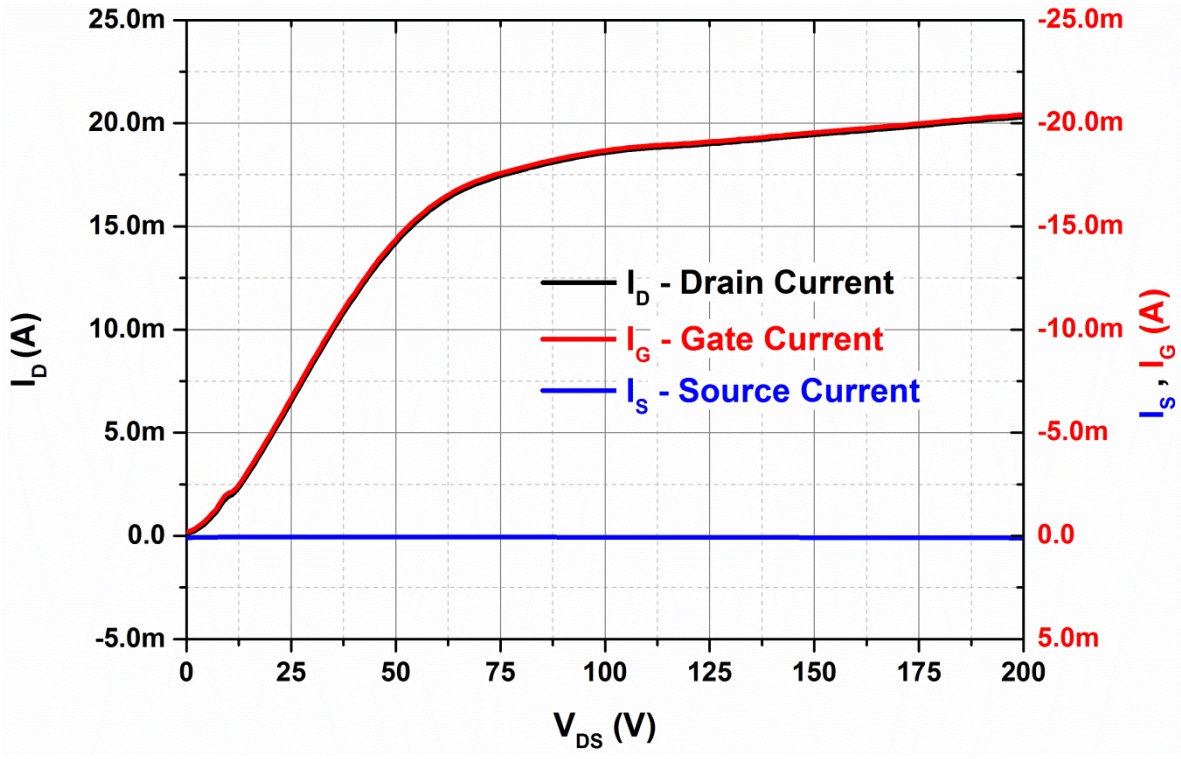
(b)

Figure 4.30 Measured output characteristics of large area multi-finger PSJ HFETs (width = 8.4 mm) (a) ***GaN-on-SiC-1 (S'ton)*** **(b)** ***GaN-on-SiC-2 (Sheff.)*** **(refer to Table 4.1)**

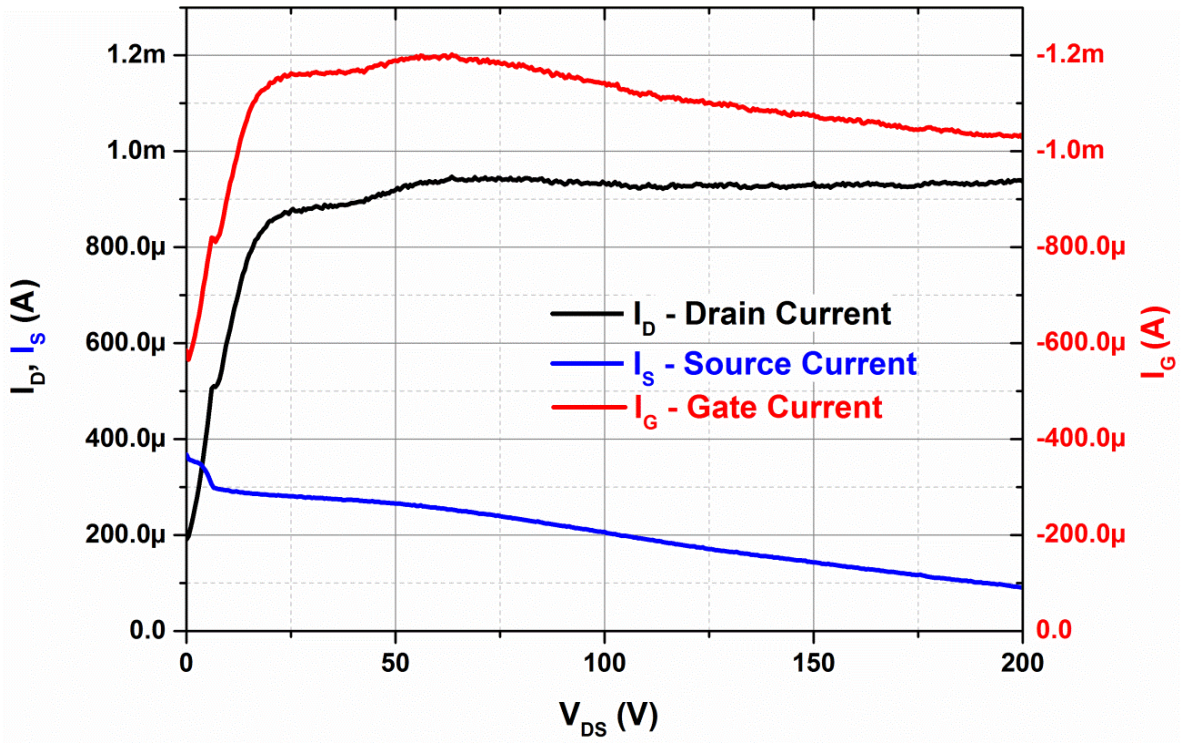
Although the magnitude of the on-state resistance was comparable, the Drain Saturation current for the device processed at Sheffield was considerably higher. The higher Drain Saturation current is due to the higher magnitude of Threshold Voltage (V_{TH}) for the PSJ HFET from *GaN-on-SiC-2 (Sheff.)* ~ – 2.25 V compared to ~ – 1.25 V for the device from *GaN-on-SiC-1 (S'ton)*. The reason for the apparent matching of the on-state characteristics and the difference in V_{TH} will become clearer from the discussion that will be presented in Section 4.5.

Off-state leakage characteristics (Gate-to-Source Voltage V_{GS} = - 5 V) of the two PSJ HFETs (effective width = 8.4 mm) fabricated on *GaN-on-SiC-1 (S'ton)* and *GaN-on-SiC-2 (Sheff.)* respectively have been shown in Figs. 4.31 (a) - (b). As observed in the case of the PSJ Diodes, abnormally high Drain-to-Gate leakage (Schottky leakage) was observed in the devices processed at Southampton. As shown in Fig. 4.31 (b), although the primary path for the off-state leakage current at high Drain-Source Voltage (V_{DS}) was also directed from Drain-to-Gate for PSJ HFET from *GaN-on-SiC-2 (Sheff.)*, the overall leakage values were ~ 1 mA at V_{DS} = 200 V.

The behaviour of the consistently high Schottky leakage in the devices processed at Southampton (in Diodes and HFETs) suggests that the process determining the quality of Gate or Anode contact and the quality of the interface with the underlying AlGaN layer should be the main determining factor. During process development at Southampton, Ion Beam Etching (Ar based, purely physical etching) was chosen to etch the GaN layers for isolation as well as for defining mesa and the access regions in the active area of the device where Drain/Cathode, Source and Gate/Anode electrodes were to be deposited.



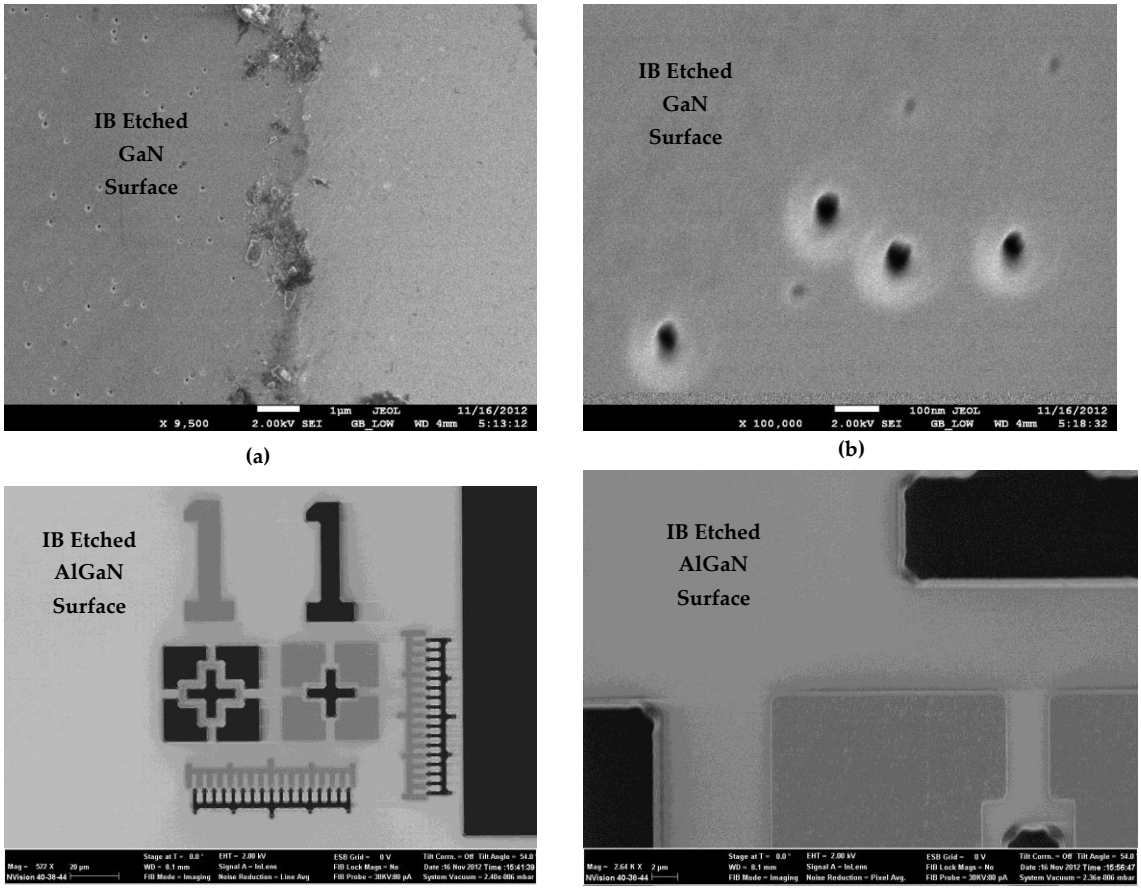
(a)



(b)

Figure 4.31 Measured off-state leakage characteristics of large area multi-finger PSJ HFETs (width = 8.4 mm) (a) ***GaN-on-SiC-1 (S'ton)*** **(b)** ***GaN-on-SiC-2 (Sheff.)*** **(refer to Table 4.1)**

The choice of Ion Beam etching (IBE) over ICP etching (used at Sheffield) at Southampton had been made based on expectations of better equipment control of residual layer thickness and uniformity achieved during 3" wafer level processing as well as comparable etched surface quality based on visual inspection during the process development phase. As shown in Fig. 4.32, etch pits were observed on the IB etched GaN surface, but no anomalies were observed on the etched AlGaN surface.



(a) (b) (c) (d)

Figure 4.32 Micrographs of (a) Etched GaN surface (350 nm) (b) Etched GaN surface (Magnified) (c) Etched AlGaN surface (65 nm) (d) Etched AlGaN surface (magnified) (Courtesy : Nanofabrication Centre, ECS, University of Southampton)

However, no electrical characterisation was performed to validate the IB etch process.

The wafers processed at Southampton and Sheffield are from the same batch. Therefore, the prime suspect for the compromised leakage characteristics observed in the devices processed at Southampton, appears to be the processing technique that was employed during AlGaN etching (ICP etching (Sheffield) vs. IBE (Southampton)). Another possibility is the variation/deterioration in the IBE equipment/recipe performance from the time of process development to the point in time when the actual wafers were processed, which could also have compromised the quality of the etching process and led to high crystal damage in the etched regions.

4.4 Large Area PN Diodes

Along with Schottky Barrier Diodes, GaN PN Diodes have also received a lot of attention recently for high power electronic applications. Most of the work has been focussed on vertical devices fabricated on GaN substrates and some groups have also reported avalanche capability in such devices [6-8].

Although the work reported in this thesis was initiated at a time that predates the recent reports, the device development was motivated to study and evaluate potential avalanche capability in large area high voltage lateral PN Diodes. As the PSJ platform inherently caters to the presence of 2DHG (p-type) and 2DEG (n-type) within the GaN/AlGaN/GaN double heterostructure, the objective was to realise a PN diode which employed these polarisation induced charge carriers for forward conduction and sustained high voltage under reverse bias conditions using the inherent charge balance in the structure.

Fig. 4.33 shows a simplified cross-section of a single cell in a large area multifinger PN Diode.

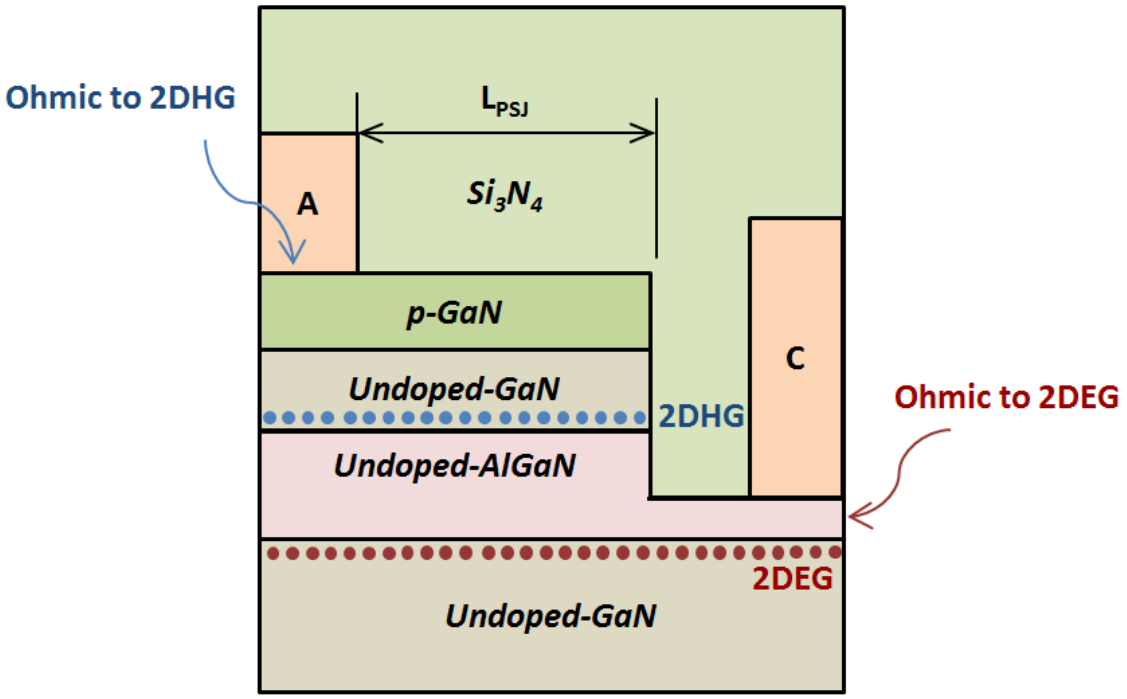
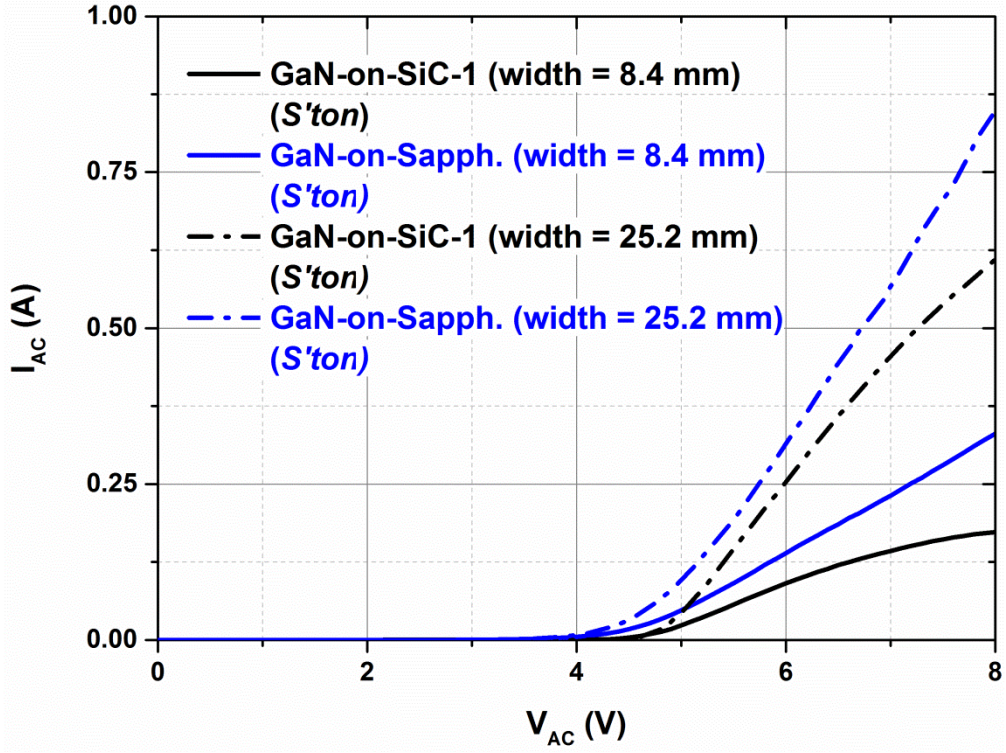


Figure 4.33 Cross-section schematic of a single cell in a multifinger large area PN Diode fabricated on 6H-SiC/Sapphire substrates

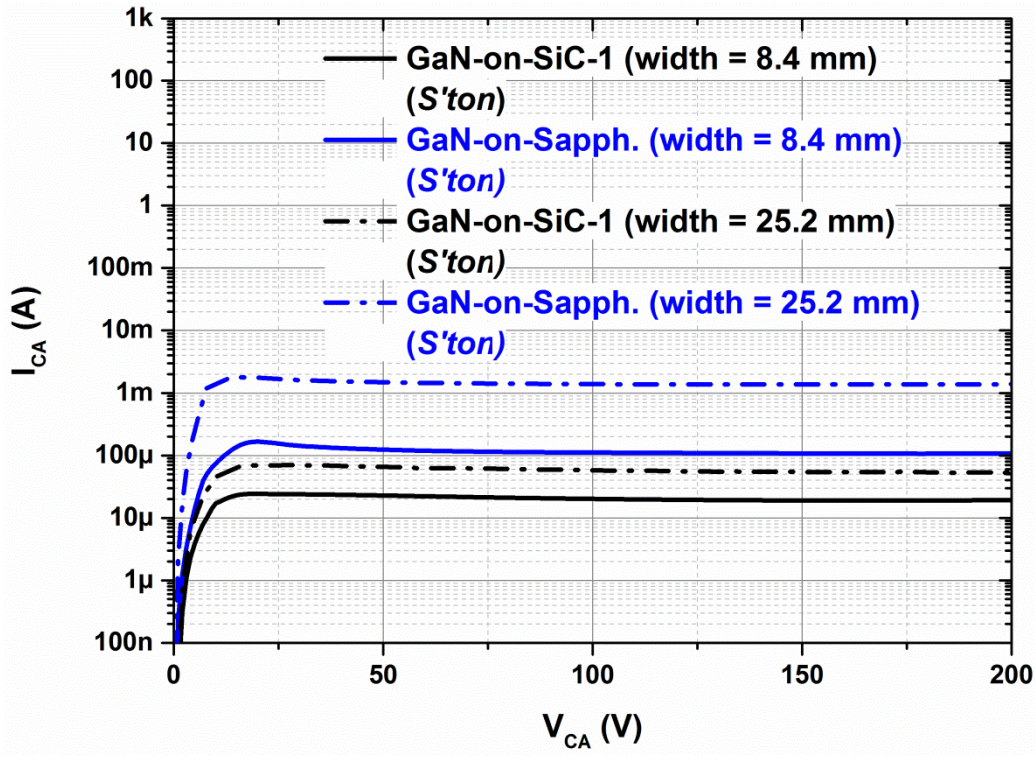
Several large area PN Diodes with various current handling capabilities were fabricated on SiC and Sapphire substrates, processed at Southampton.

The forward and reverse I-V characteristics of PN Diodes fabricated on *GaN-on-SiC-1 (S'ton)* and *GaN-on-Sapphire (S'ton)* have been shown in Figs. 4.34 (a) - (b). The on-set voltage is more than 4 V which is higher than the on-set voltage values typically reported for vertical GaN PN Diodes. It was observed during process development as well as from TLM characterisation of p-contacts on the processed wafers that the contacts showed quasi-ohmic and in some cases Schottky behaviour. This translates to a higher on-set voltage of the PN Diodes. The characterisation of reverse leakage current consistently showed that the devices fabricated on the GaN-on-Sapphire wafer had leakage currents that were higher by almost an order of magnitude when compared those fabricated on the GaN-on-SiC wafer. This could be attributed to the higher crystal quality

and lower defect density achieved in GaN-on-SiC wafers due to lower level of lattice mismatch when compared to GaN-on-Sapphire wafers.



(a)



(b)

Figure 4.34 Measured I-V characteristics of large area multi-finger PN Diodes (a) Forward I–V characteristics (b) Reverse I–V characteristics (refer to Table 4.1)

Breakdown characteristics were also evaluated on PN Diodes under Fluorinert ambient and floating substrate conditions. The devices were chosen such that they were at the exact location on the respective wafers. The characteristics have been shown in Fig. 4.35.

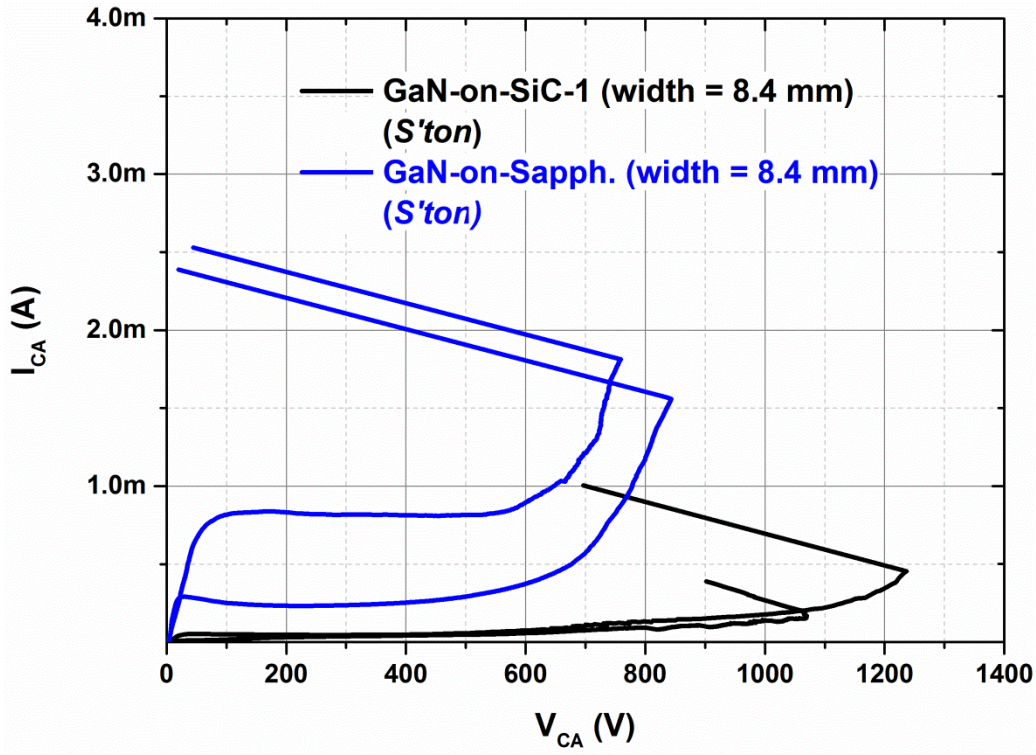


Figure 4.35 Measured breakdown characteristics of large area multi-finger PN Diodes (floating substrate)

The breakdown was destructive and devices on sapphire substrates showed high leakage and relatively lower breakdown voltage (V_{BR}). One of the GaN-on-SiC PN Diode showed V_{BR} of ~ 1250 V (design specification was V_{BR} = 1200V for the scaled up devices) sustaining an average critical electric field strength of 0.83 MV/cm (Drift length L_{PSJ} = 15 μm). The general variation observed in the V_{BR} values clearly suggests that the breakdown voltage of a large area device is determined not only by the designed/engineered field profile but also substantially depends on the crystal quality and distribution of defects in the wafers.

Visual inspection was performed on all the devices post-breakdown. Fig. 4.36 shows the micrographs of a GaN-on-SiC PN Diode post-breakdown. The region of breakdown was identified and was observed to be randomly located in the active area of the devices. The signature does suggest that the current tends to crowd at the breakdown location indicated by a characteristic localised burn mark as can be seen in Fig. 4.36. Such a signature was observed on all the devices that were studied.

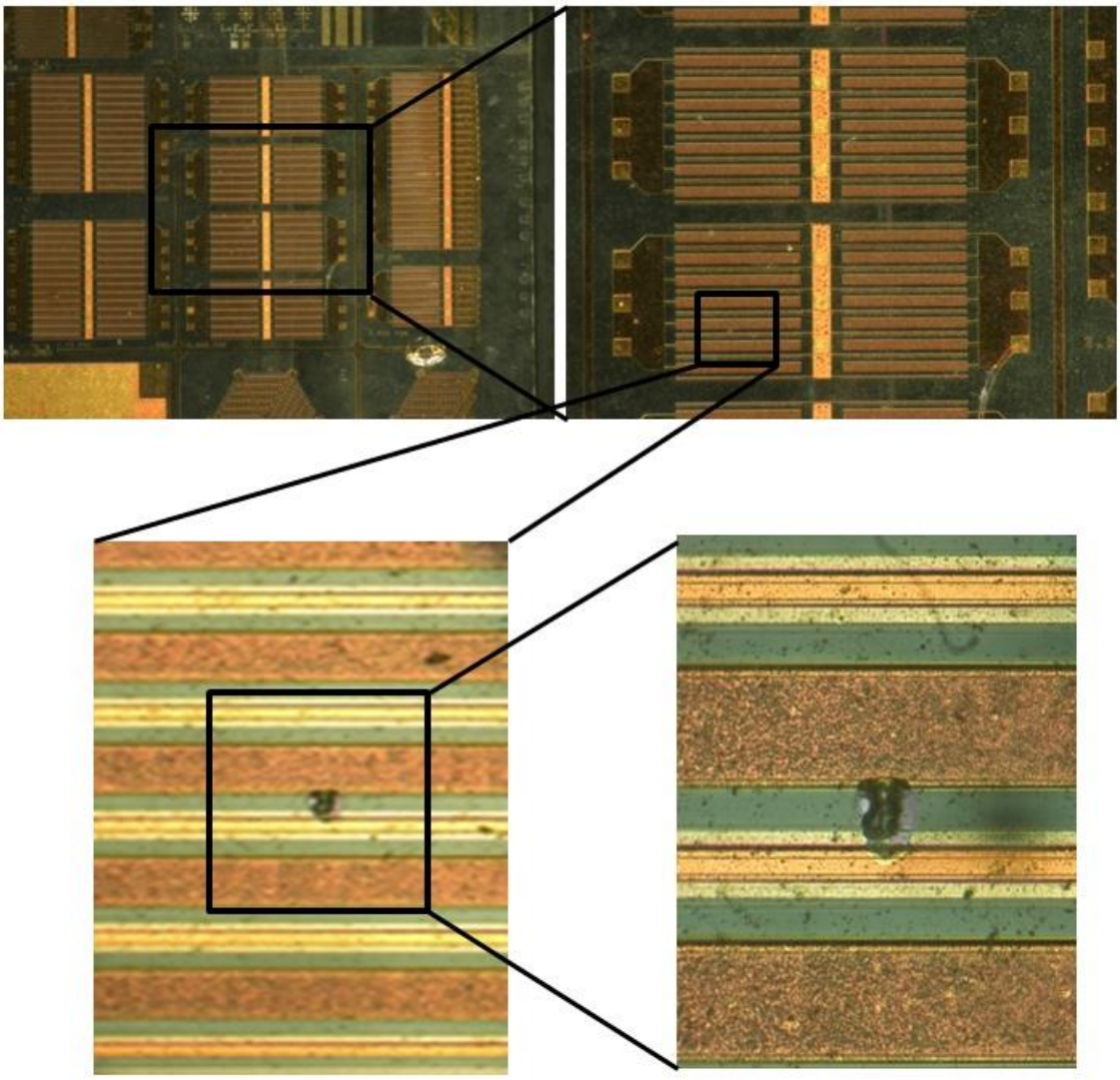


Figure 4.36 Micrograph of a GaN-on-SiC PN Diode post-breakdown

4.5 Dominant Factors Determining Scalability Performance

Detailed characterisation of the various large area devices that were fabricated revealed that there was variation in the performance of device characteristics within a wafer, from wafer to wafer, as well as from one device processing facility to the other. Although such variations are not completely unexpected as the field of GaN power electronic device development is still in a developing stage.

In this section, an attempt has been made to identify the key factors which determine the scalability performance in terms of on-state characteristics or current rating achieved in the fabricated multifinger large area devices. The approach is based on the model developed by Simin et al. [9].

A multifinger large area device essentially is a parallel combination of many individual device cells. Understanding the performance of the large device can be attained initially by studying the individual cell and dependence of its performance (on-state resistance) on factors like finite metal resistance of the finger electrodes (Drain/Source), 2DEG channel sheet resistance, contact resistance and cell width. Schematic representation of a single cell within a multifinger large area device has been shown in Fig. 4.37.

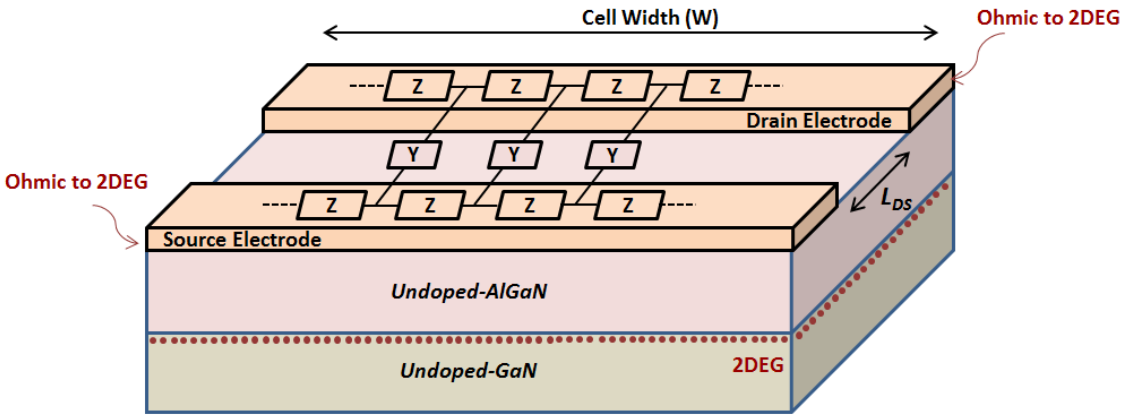


Figure 4.37 Schematic representation of a single cell within a multifinger large area device

Simin et al. derived the following expression for the overall resistance of a single cell

$$Resistance = \frac{\alpha W}{2}\cdot\left[\frac{\alpha W}{2} + \frac{e^{\alpha W}+1}{e^{\alpha W}-1}\right].R_{IDEAL} \quad (4.4)$$

$$R_{IDEAL} = 1/(Y.W) \quad (4.5)$$

$$Y = 1/(2.R_C + R_{SH}.L_{DS}) \quad (4.6)$$

$$\alpha = \sqrt{2(Y.Z)} \quad (4.7)$$

Where W is the cell width, R_C is the normalised ohmic contact resistance, Z is normalised electrode resistance, R_{SH} is the 2DEG sheet resistance, L_{DS} is the Drain-to-Source spacing, R_{IDEAL} is the cell resistance neglecting electrode resistance, and Y is the normalised channel conductance. R_C, R_{SH} can be extracted from characterisation of TLM patterns. Z can be extracted from characterisation of metal resistance test pattern that was fabricated as one of the process test structures. Therefore, detailed TLM and metal resistance test pattern characterisation was performed on all the five processed wafers. On the 3" wafers, a dedicated section with two TLM patterns on the top and bottom regions of the section was characterised. The results of the resistance measurement with respect to TLM contact separation performed on all five wafers have been shown in Fig. 4.38. From these charts, most of the parameters required in the assessment of the overall resistance of a cell were extracted and have been shown in Fig. 4.39. Normalised metal resistance was extracted based on measurements performed on the metal resistance test pattern (width= 12 μm, thickness = 0.75 μm and 4 μm at Sheffield and Southampton respectively, for various electrode lengths from 50 μm to 600 μm). Based on the values of Specific Contact Resistance, Normalised Contact Resistance was calculated for an electrode that is 12 μm wide (in alignment with the geometry of the metal resistance test pattern). Using values of the extracted parameters and equation

4.4, overall cell resistance was calculated by varying the magnitude of cell width from 50 μm to 5000 μm. Drain to Source spacing (L_{DS}) was set at 35.5 μm (as in the actual fabricated devices). The charts representing individual cell resistance based on parameters extracted from each of the wafers have been shown in Fig. 4.40.

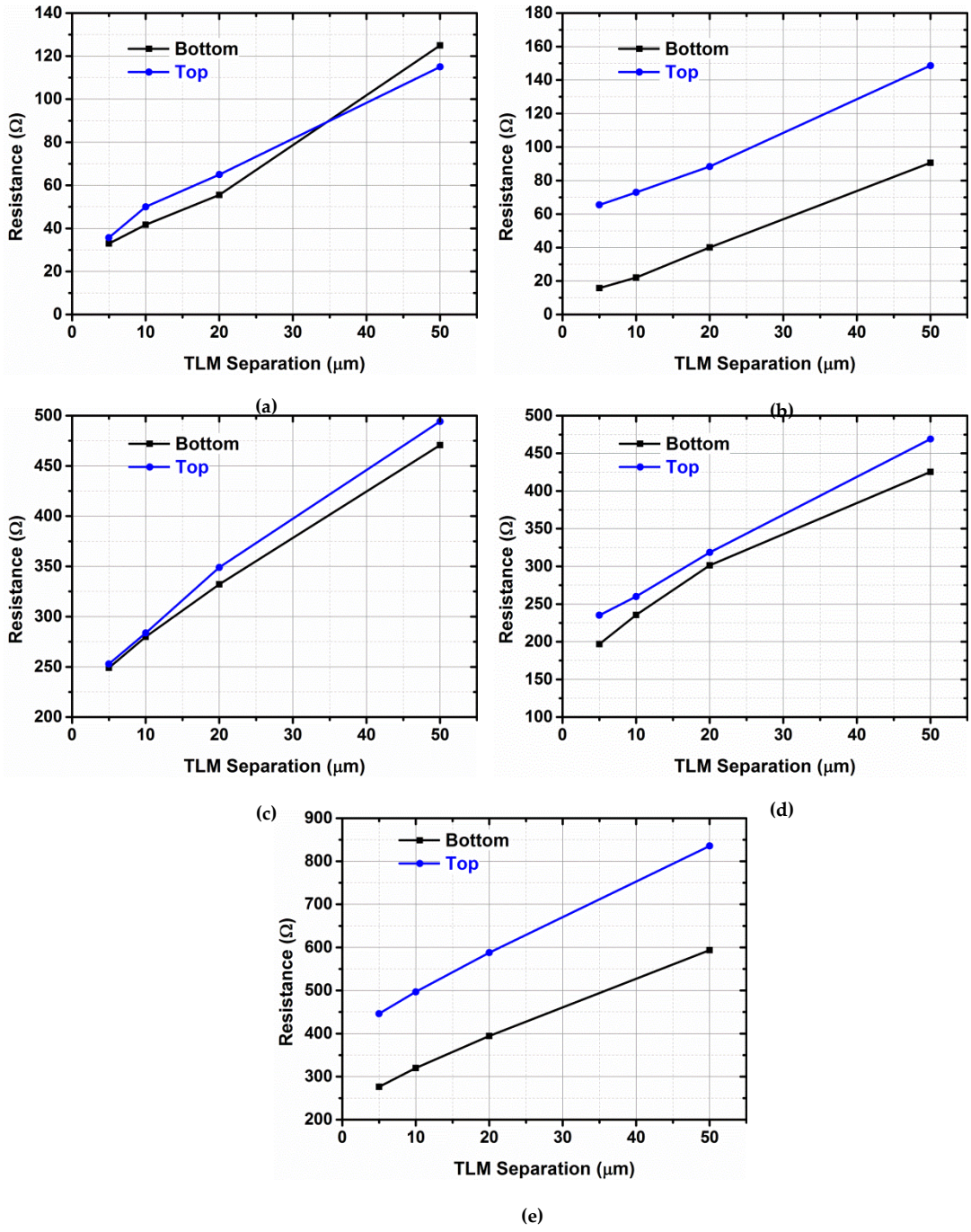
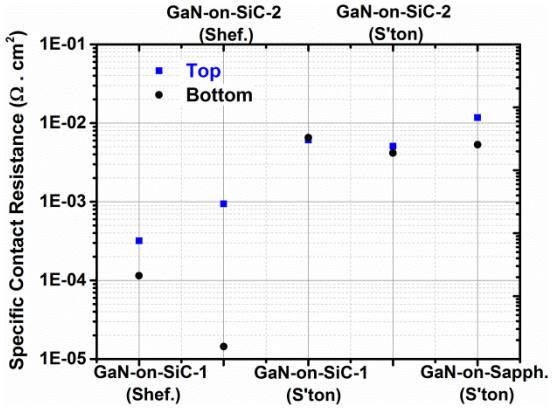
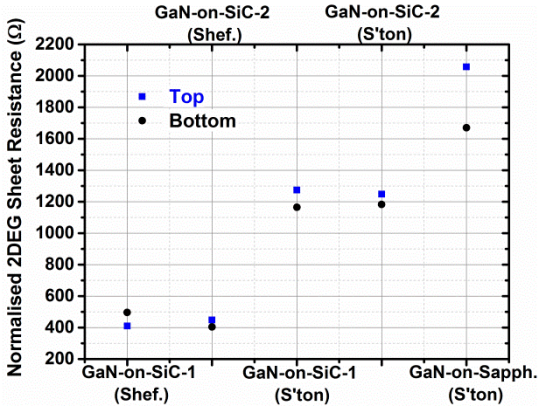


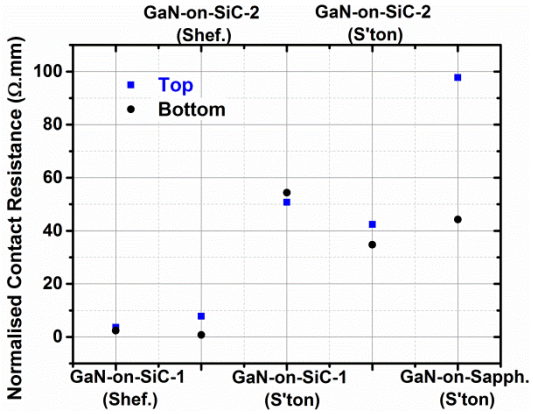
Figure 4.38 Resistance vs. TLM separation (a) *GaN-on-SiC-1 (Sheff.)* **(b)** *GaN-on-SiC-2 (Sheff.)* **(c)** *GaN-on-SiC-1 (S'ton)* **(d)** *GaN-on-SiC-2 (S'ton)* **(e)** *GaN-on-Sapphire (S'ton)*



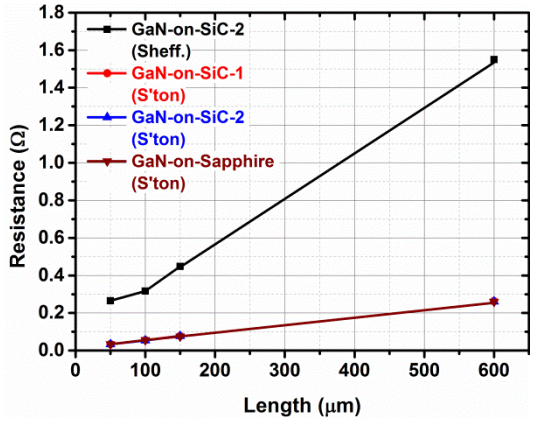
(a)



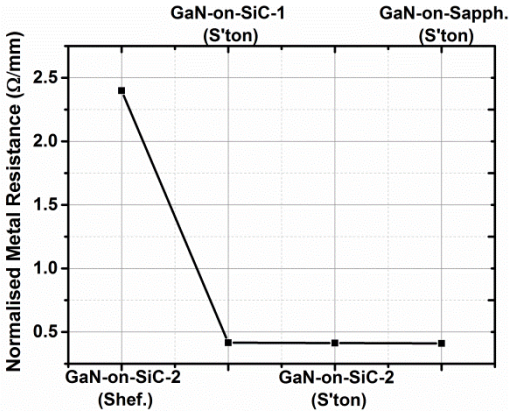
(b)



(c)



(d)



(e)

Figure 4.39 Extracted parameters from the characterisation of TLM patterns and metal resistance test pattern (a) Specific Contact Resistance (b) 2DEG Sheet Resistance (c) Normalised Contact Resistance (d) Electrode Metal Resistance vs. length (almost identical values for the 3 wafers processed at Southampton) (e) Normalised Electrode Metal Resistance

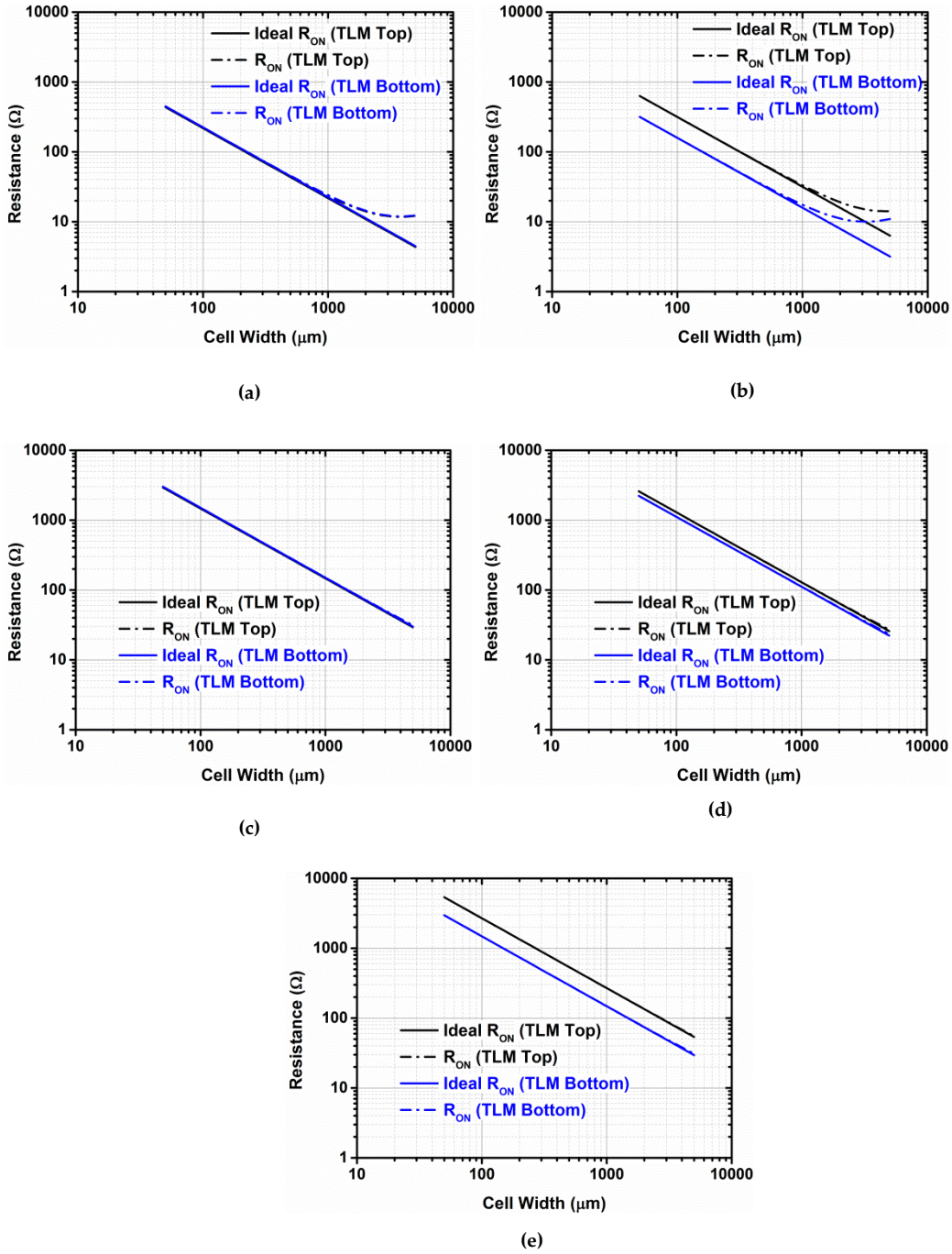


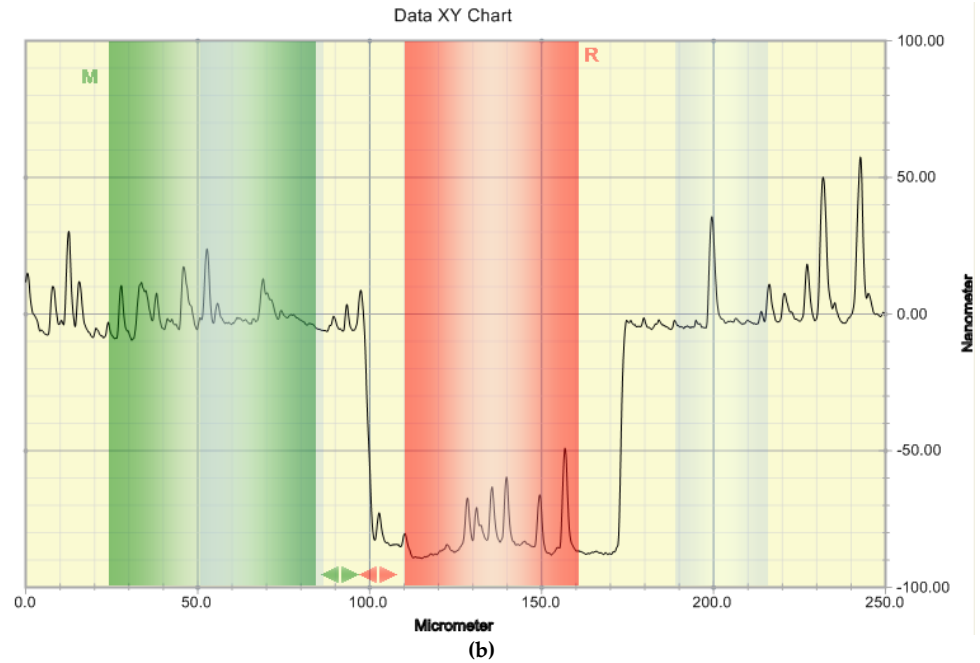
Figure 4.40 Overall Cell Resistance vs. Cell Width (a) *GaN-on-SiC-1 (Sheff.)* **(b)** *GaN-on-SiC-2 (Sheff.)* **(c)** *GaN-on-SiC-1 (S'ton)* **(d)** *GaN-on-SiC-2 (S'ton)* **(e)** *GaN-on-Sapphire (S'ton)*

Key observations and insight gained from this analysis have been summarised in the following points:

1. The specific contact resistance for wafers processed in Southampton is almost an order to two orders of magnitude higher compared to the wafers processed at Sheffield.
2. Substantial variation of the Specific Contact Resistance has been observed in *GaN-on-SiC-2 (Sheff.)*. The Specific Contact Resistance is two orders of magnitude higher in the top region of the wafer compared to the bottom. The PSJ HFET, output characteristics of which have been shown in Fig. 4.30 (b), is located in the top left region of the wafer and could suffer from high contact resistance significantly compromising its on-state characteristics (compared to design specifications).
3. The 2DEG sheet resistance of the wafers processed in Southampton are almost three to four times higher compared to the ones processed in Sheffield.
4. For the overall on-state resistance, the deviation from ideality could only be observed for cells with parameters extracted for wafers processed at Sheffield. This could be attributed to relatively lower contact and sheet resistance in these wafers as well as the fact that the metal thickness of the electrodes is less than 1 μm. This deviation begins to become prominent when the cell width exceeds 1000 μm. Considering that the maximum cell width in the multifinger devices fabricated is less than 600 μm, the on-state characteristics are hardly influenced by the finite parasitic resistance of the electrodes in the fabricated devices across all wafers.

In order to investigate point 3 mentioned above, surface profilometry was carried out on the process test structures to monitor etch depth, on *GaN-on-SiC-1 (S'ton)* as well as *GaN-on-Sapphire (S'ton)*. The results for isolation and mesa etch performed on *GaN-on-SiC-1 (S'ton)* have been shown in Fig. 4.41.

(a)



(b)

Figure 4.41 Surface profilometry measurement (*GaN-on-SiC-1 (S'ton)*) (a) Isolation etch (b) Mesa etch

The average isolation etch depth was found to be ~ 137 nm (Target = 125 nm) and mesa etch depth was ~ 80 nm (Target = 65 nm). Similar values were observed on the GaN-on-Sapphire wafer. This clearly shows that the AlGaN barrier layer has been over-etched (barrier thickness was observed to be in the range ~ 7 - 10 nm across both wafers), leading to substantially lower 2DEG density and higher sheet resistance in these wafers.

In order to gain deeper understanding of the dependence of overall on-state resistance of a multifinger HFET on key influencing parameters such as geometry, contact resistance and channel sheet resistance, numerical simulations were performed using the electric analysis system in ANSYS workbench. Three-dimensional geometry of the structure as shown in Fig. 4.42, was created that was almost a replica of an actually fabricated multifinger HFET (width = 8.4 mm)

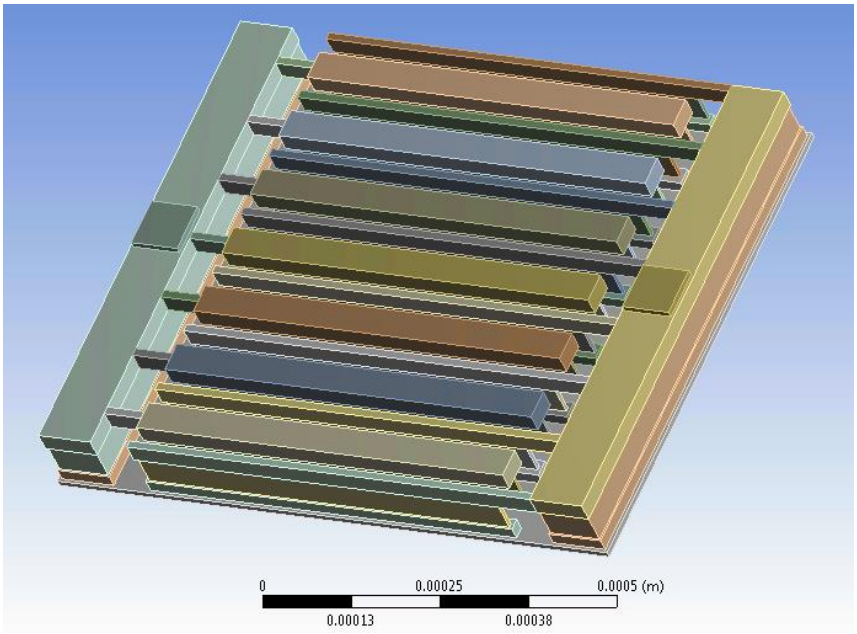
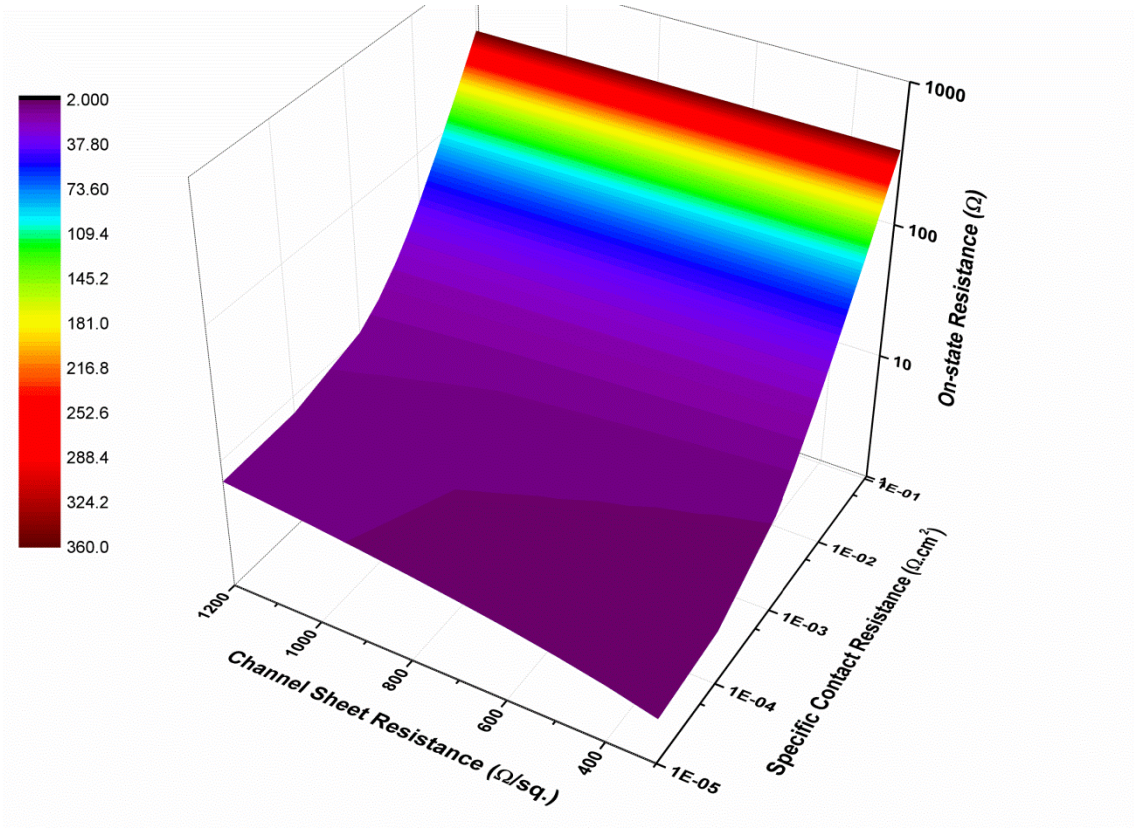
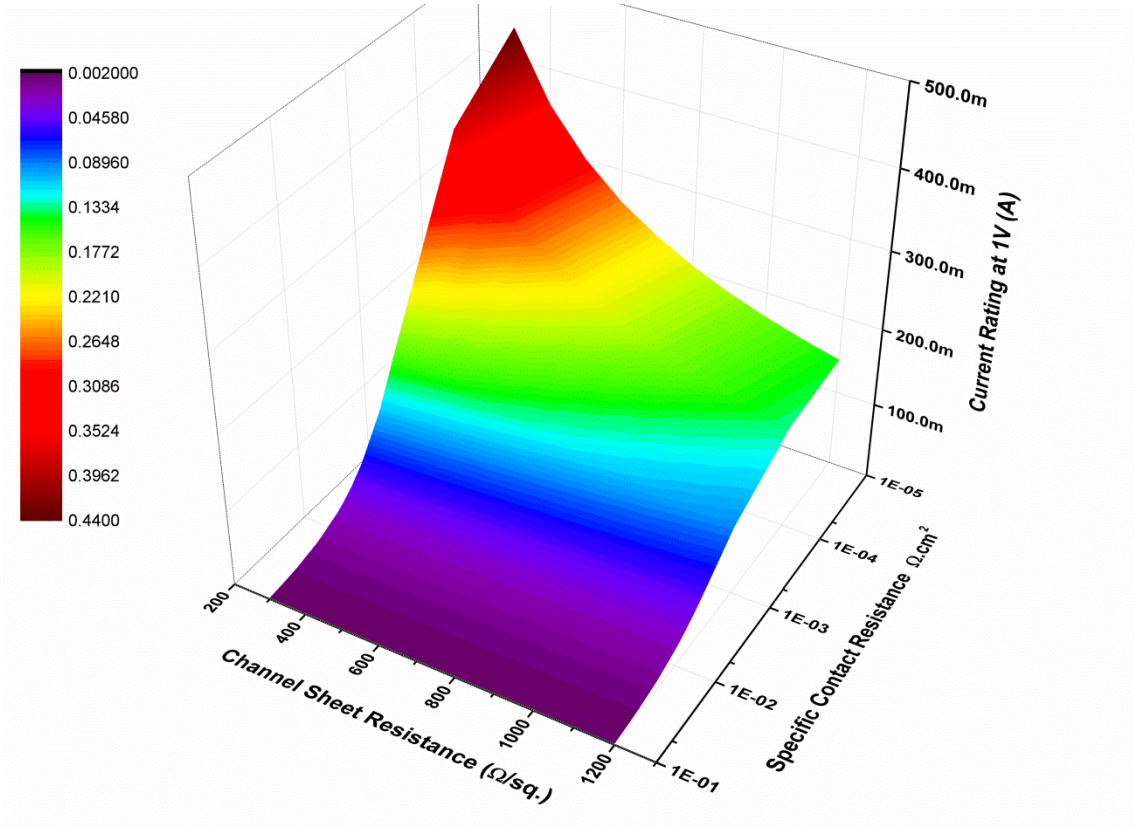


Figure 4.42 Three-dimensional geometry of the simulated structure

The inputs for simulation included engineering data such as channel sheet resistance, metal resistivity, and contact resistance. The extruding metal pad on the right was biased at 1 V and the pad on left side was biased at 0V. The simulation of steady state electric conduction characteristics was performed and resistance values were extracted using the Reaction Probe feature. 130 data points were obtained from simulations performed with values of sheet resistance varying from 300 Ω to 1200 Ω and those of specific contact resistance that were varied from 10^{-1} Ω.cm^2 to 10^{-5} Ω.cm^2. The three-dimensional landscape of variation of the on-state resistance and current rating of a device, has been shown in Figs. 4.43 (a)-(b) respectively.



(a)



(b)

Figure 4.43 Three-dimensional landscape of the variation of (a) on-state resistance (b) current rating

Based on the landscape as shown in Fig. 4.43, for a given set of values for Specific Contact Resistance and Sheet Resistance, the corresponding on-state resistance and current rating can be predicted for a large area device with a particular geometry. The simulation results appear to be in alignment with the experimental results based on the extracted parameters from test structures and suggest that the on-state characteristics of the fabricated devices are primarily governed by the contact resistance of fingers, when the specific contact resistance values are greater than 10^{-3} Ω.cm^2 and channel sheet resistance values are less than 1200 Ω. The on-state characteristics of devices showed substantial variation on the 3″ wafers. Such variation could occur with AlGaN layer etch non-uniformity as well as temperature distribution in the substrates during Rapid Thermal Annealing (RTA) for ohmic contact formation. The temperature distribution is expected to be larger/more uneven in the case of Sapphire substrates due to the relatively low thermal conductivity compared to that of SiC substrates translating to relatively higher variation of the on-state characteristics for devices fabricated on 3″ GaN-on-Sapphire substrates, as was observed experimentally as well.

4.6 Intrinsic Diode and Dynamic Clamping Capability of PSJ HFETs

The current workhorse of power electronic applications with voltage rating requirements of less than 1200 V is the Silicon (Si) Power MOSFET. Majority of the High Voltage (HV) GaN HFETs under development as well as those available commercially today are targeting these applications and to replace Si Power MOSFETs. A unique feature of the Si Power MOSFETs is an intrinsic body diode between the Source and Drain terminals which is sometimes employed as clamping or a freewheeling diode in certain converter topologies. In applications which require higher efficiency and better reverse recovery characteristics, a Schottky Barrier Diode is sometimes placed in parallel with the intrinsic diode. Synchronous rectification has been another approach to achieve

the same objectives, when the efficiency requirements are even more stringent. In this approach, the intrinsic diode action is inhibited by separately controlling the transistor and turning it ON such that the current flows through the channel of the transistor rather than the diode. Even in such an approach, there is a finite dead time during which the current flows through the body diode or a Schottky Barrier Diode; therefore an intrinsic diode is still a desired feature [10].

Conventional GaN HFETs do not have an intrinsic diode. However, reverse conduction can still be achieved. Fig. 4.44 shows the transfer characteristics of a conventional transistor from *GaN-on-SiC-2 (Sheff.)* wafer.

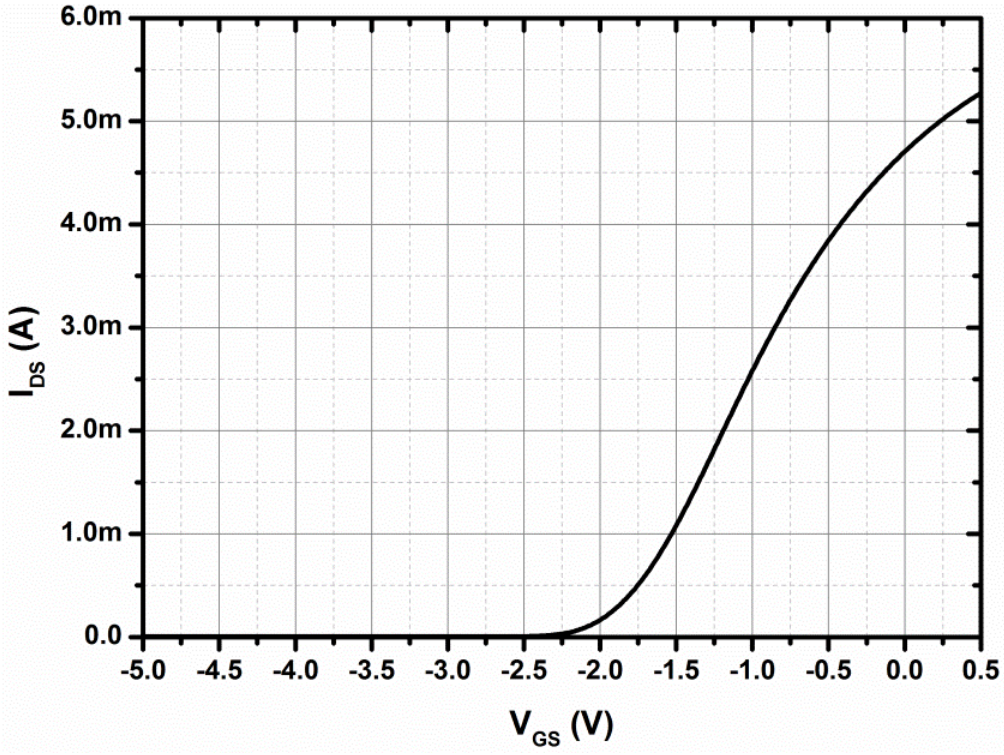
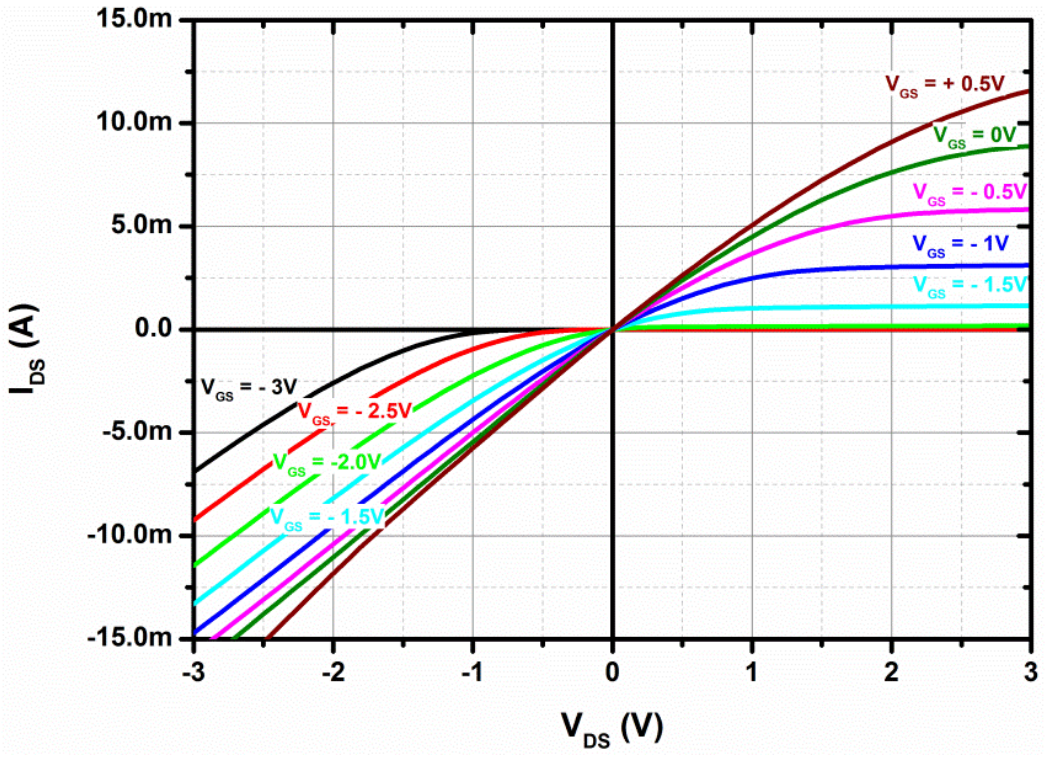
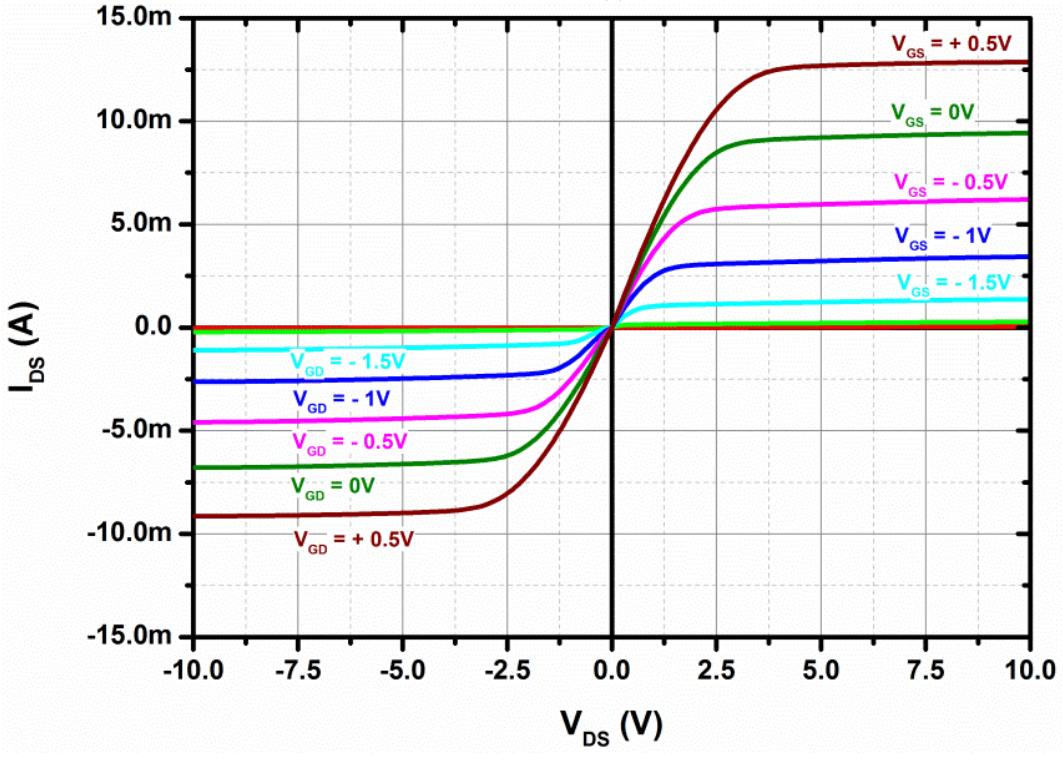


Figure 4.44 Measured transfer characteristics of a conventional HFET (V_{DS} = 1V)

The threshold voltage (V_{TH}) is estimated to be ~ - 2.25 V. The output characteristics of this device have been shown in Figs. 4.45 (a) – (b). As can be clearly seen from Fig. 4.45 (a), reverse conduction is possible when the HFET is operated in the third quadrant.



(a)



(b)

Figure 4.45 Measured output characteristics of a conventional HFET (a) Standard (b) Gate biased with respect to Drain instead of Source in the third quadrant

In Fig. 4.45 (b), the characteristics shown in the third quadrant are for Gate biased with respect to Drain instead of Source and hence the general symmetry

observed with characteristics shown in the first quadrant. As shown in Fig. 4.45 (a), the reverse conduction current depends on the magnitude of V_{GS}, V_{DS} as well as V_{TH} of the device. Fig. 4.46 illustrates this aspect, where reverse conduction characteristics have been shown for two different biasing conditions of V_{GS}. The reverse current only flows when the HFET turns on (i.e., when $V_{GD} > V_{TH}$ (~ - 2.25 V))

- When V_{GS} = -3V, the transistor turns ON at V_{DS} ~ - 0.75 V (V_{GD} ~ - 2.25 V)
- When V_{GS} = -10V, the transistor turns ON at V_{DS} ~ - 7.75 V (V_{GD} ~ - 2.25 V)

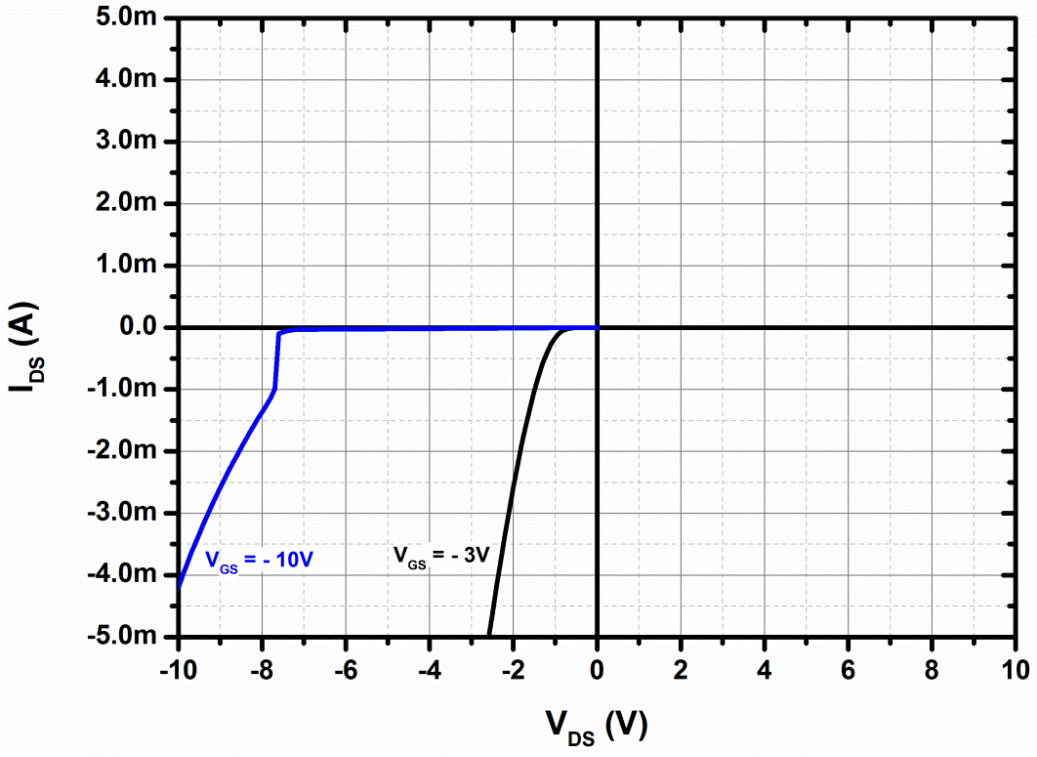


Figure 4.46 Reverse conduction characteristics of a conventional HFET at two different values of V_{GS}

There are applications where V_{GS} is maintained at values considerably lower than the V_{TH} to maintain a stable off-state condition and forcing reverse conduction under off-state will lead to compromised performance. A simple solution to this could be to place an antiparallel high performance diode also with the GaN HFET to take care of the reverse conduction with the penalty of the added area that the additional device will occupy.

PSJ HFETs incorporate an intrinsic diode within the structure to address this issue effectively as was briefly described in section 4.3. Fig. 4.47 shows the transfer characteristics of a large area multi-finger PSJ HFET from *GaN-on-SiC-1 (S'ton)* wafer.

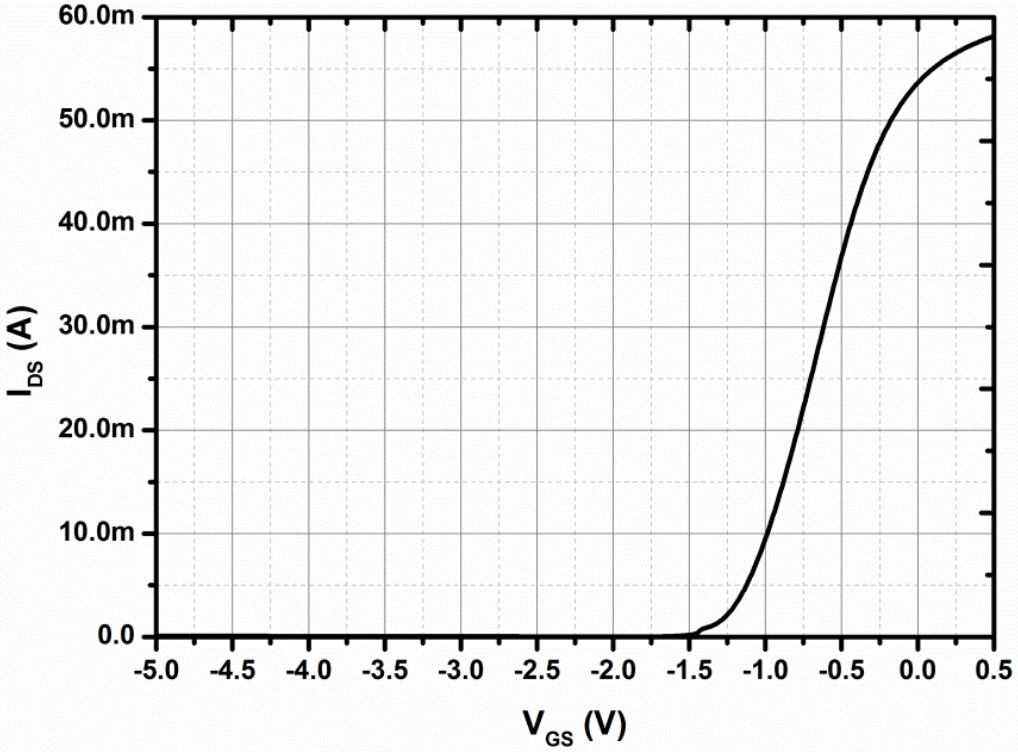
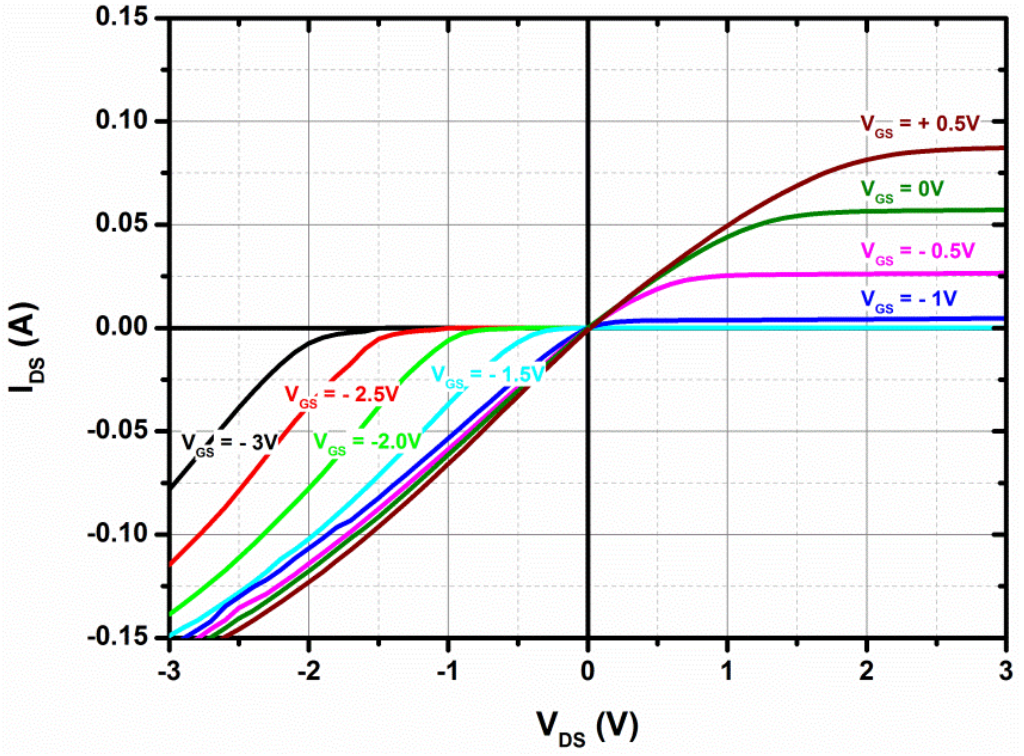
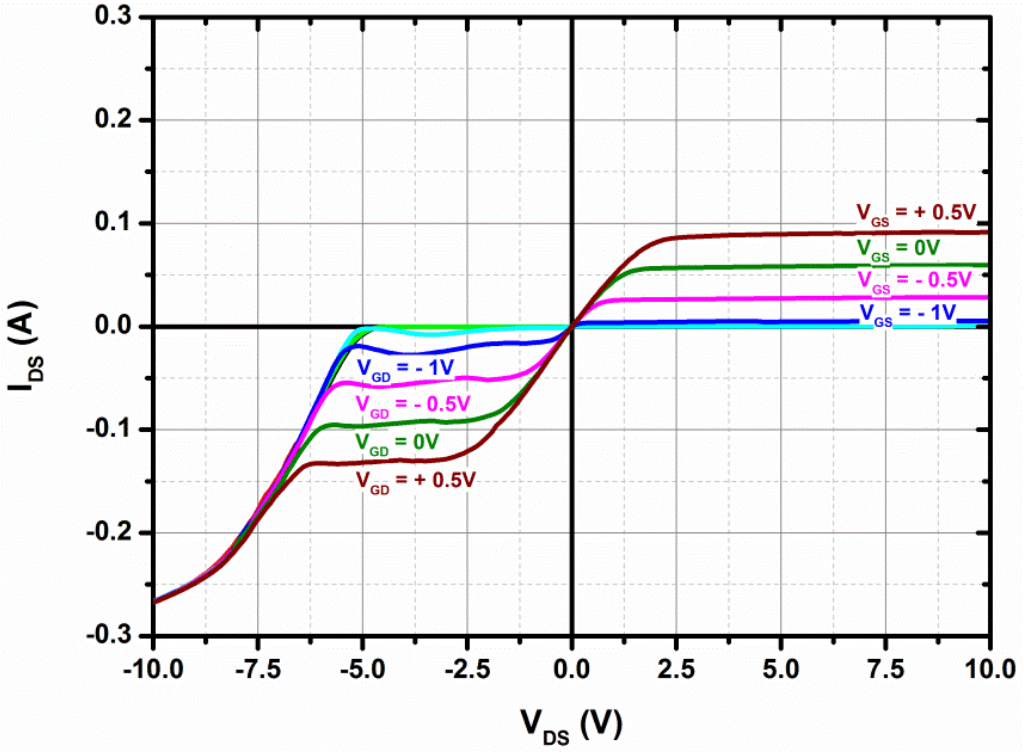


Figure 4.47 Measured transfer characteristics of a large area PSJ HFET (V_{DS} = 1V)

The threshold voltage (V_{TH}) is estimated to be ~ - 1.5 V. The output characteristics of this device have been shown in Figs. 4.48 (a) – (b). As can be clearly seen from Fig. 4.48 (a), reverse conduction is possible when the PSJ HFET is operated in the third quadrant just like a conventional HFET. However, as shown in Fig. 4.48 (b), the characteristics shown in the third quadrant with Gate biased with respect to Drain, do not show the symmetry shown in the case of conventional HFETs as the current flow in saturation region is altered with the turning ON of the intrinsic diode. Under off-state, the intrinsic diode turns on when V_{SD} > 4-5V as was observed during the characterisation of PN Diodes. When V_{GD} is > V_{TH}, the drift region is at a finite potential and hence a higher voltage is required to turn ON the intrinsic diode.



(a)



(b)

Figure 4.48 Measured output characteristics of a PSJ HFET (a) Standard (b) Gate biased with respect to Drain instead of Source in the third quadrant

Fig. 4.49 shows the reverse conduction characteristics for three different biasing conditions of V_{GS}.

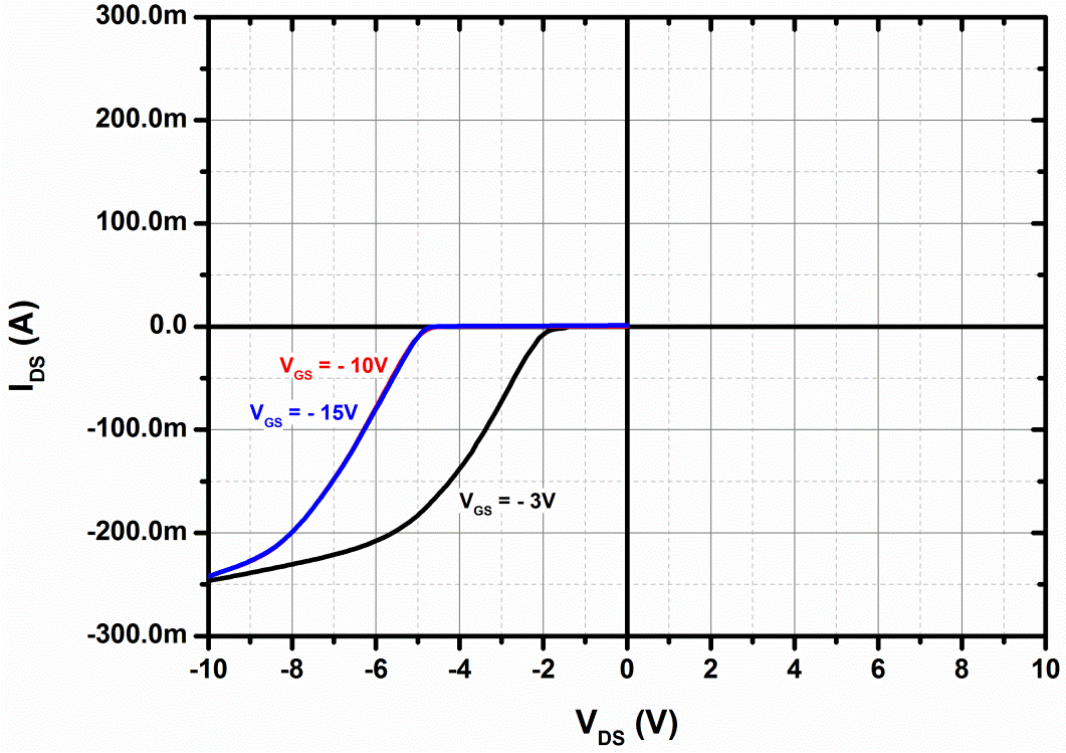


Figure 4.49 Reverse conduction characteristics of a PSJ HFET at three different values of V_{GS}

In the case of the PSJ HFET, the reverse current can flow under two conditions

- When the transistor turns ON (i.e., when $V_{GD} > V_{TH}$ (~ - 1.5V)
- When the intrinsic diode is forward biased (V_{DS} ~ < - 5V)

When V_{GS} = -3V, the transistor turns on at V_{DS} ~ - 1.5 V (V_{GD} ~ - 1.5 V). When V_{GS} = - 10V/- 15V, the transistor can only turn on at V_{DS} ~ - 8.5/-13.5V (V_{GD} ~ - 1.5 V). But, when V_{DS} ~ - 5V, the intrinsic diode is forward biased and the reverse current begins to flows through the diode. This confirmed that the diode will come into the action to ensure reverse conduction irrespective of the V_{GS} biasing conditions under off-state and operate at the same current rating as that of the HFET. The current rating of the diode can be enhanced with a better ohmic contact to the p-GaN region.

Static characterisation of the PSJ HFET has confirmed the intrinsic diode action. The device was also characterised under **dynamic clamping conditions**. Before performing the dynamic clamping evaluation, the off-state Drain-Source leakage in the device was also verified, as the devices processed in Southampton suffered from high Schottky leakage. The leakage characteristics of the PSJ HFET used in this evaluation, have been shown in Fig. 4.50.

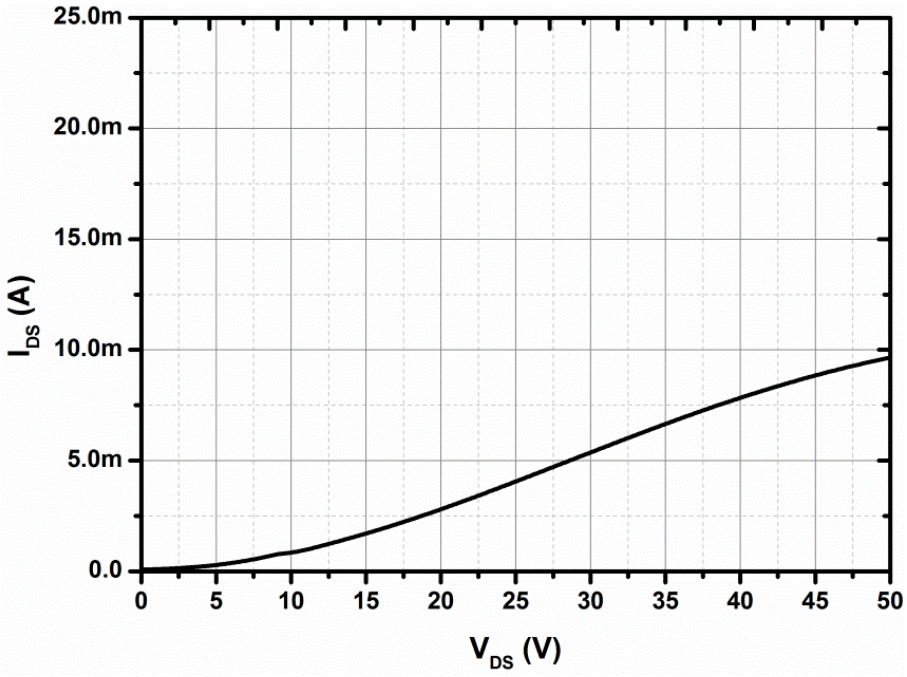


Figure 4.50 Off-state leakage characteristics of the PSJ HFET (V_{GS} = - 5 V)

The schematic of the setup used for Clamped Inductive Switching evaluation has been shown in Fig. 4.51 (a). The operation of this setup has been described below:

1. The gate driver output is initially maintained at – 15 V.
2. Using HP 8112A pulse generator, the gate driver output is triggered to switch from -15 V to + 15 V turning ON the low-side Silicon Power MOSFET.
3. Once the low side Power MOSFET turns ON, current builds up in the circuit through the inductor according to the following expression

$$V_{DD} = L.dI/dt \qquad (4.8)$$

where V_{DD} is the high side power supply voltage, L is the inductor value, I is the current and t represents the time (pulse width). The V_{DSON} of the MOSFET has been ignored in equation 4.8 as this value is typically substantially lower than V_{DD}.

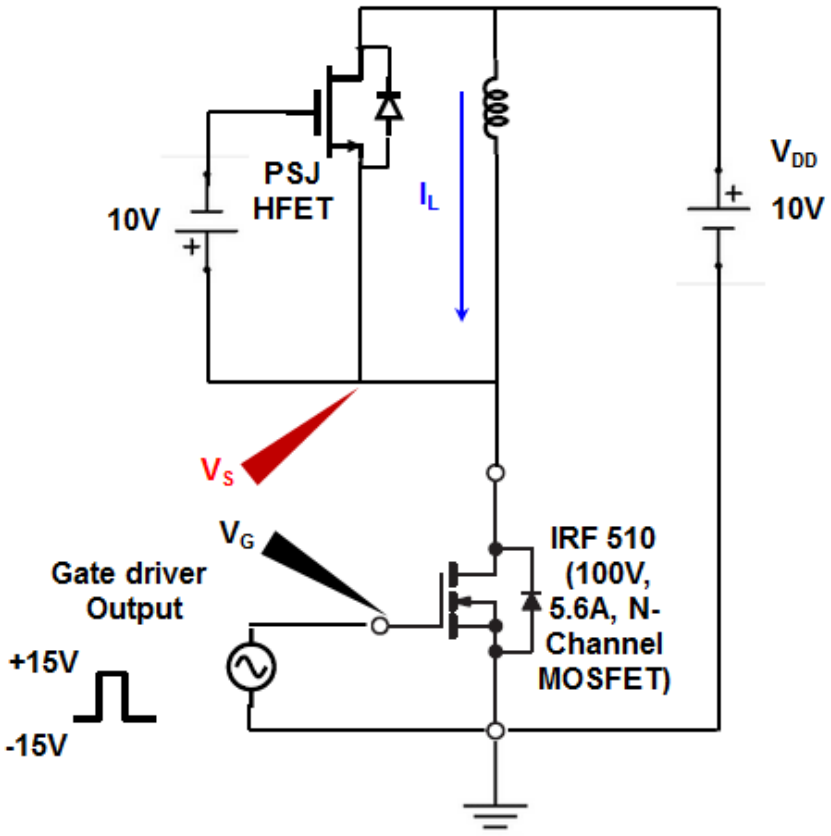
4. Based on the static characterisation of the PSJ HFET for on-state and off-state characteristics, the following values were chosen

   Pulse Width = 5 μs
   Inductor = 0.5 mH
   V_{DD} = 10 V

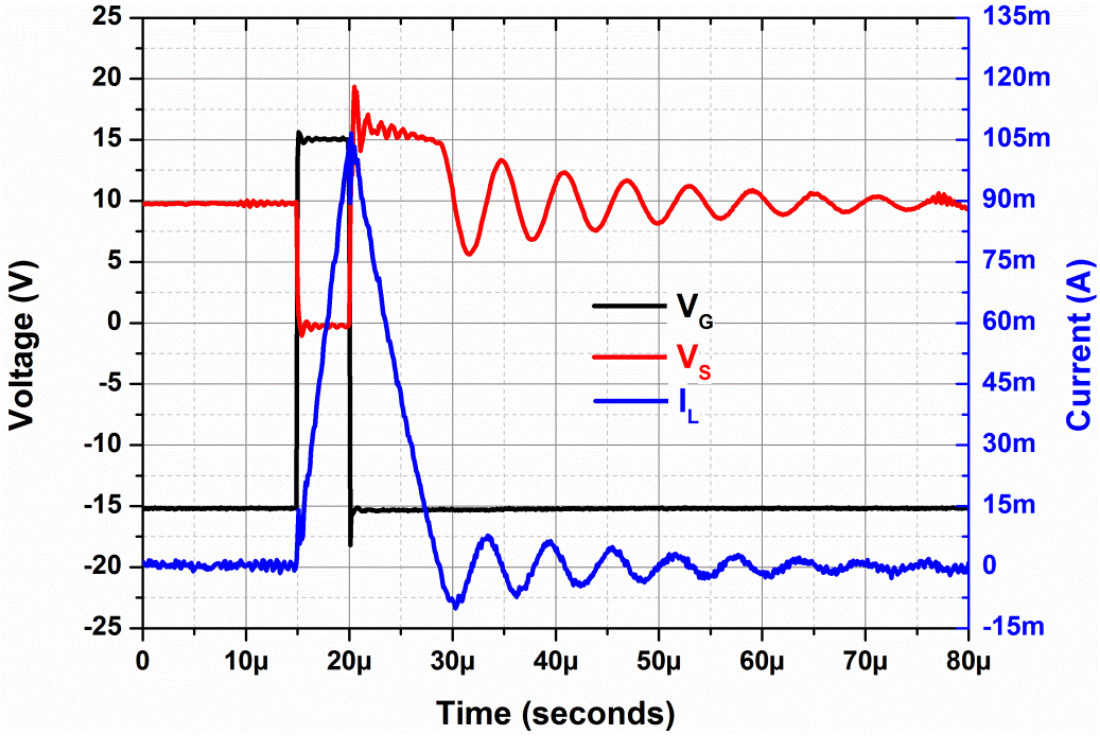
   The chosen values ensured that the current built up to 100 mA, which was within the current handling capability of the low side Power MOSFET as well as the high side PSJ HFET (during reverse conduction through the intrinsic diode) and that the Drain-Gate leakage in the PSJ HFET remained negligible during the measurement.
5. 5 μs (pulse width) after the MOSFET has been turned ON, the gate driver output is triggered back to -15 V turning OFF the MOSFET. Since the inductive current cannot abruptly drop to zero, the Drain potential of the MOSFET (Source potential of PSJ HFET) is instantaneously forced to rise until the intrinsic diode of the PSJ HFET begins to conduct and the Drain potential of the MOSFET essentially gets clamped. Once, the intrinsic diode begins to conduct, the inductor current discharges along that path. The time taken to discharge is roughly twice the pulse width as the effective voltage across the inductor is ~ 5 V (compared to 10 V during charging).
6. PSJ HFET remains off during the entire measurement using a bench top power supply which ensures that V_{GS} of PSJ HFET remained at - 10 V.

The captured waveforms have been shown in Fig. 4.51 (b). High ringing is observed as this was a wafer-level measurement with fairly long cables used for

respective connections. With this experiment, the static and dynamic clamping capability of PSJ HFET was clearly established.



(a)

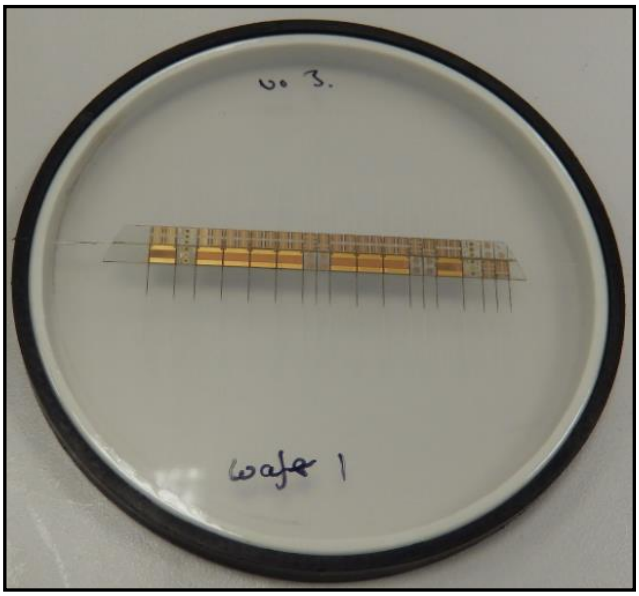


(b)

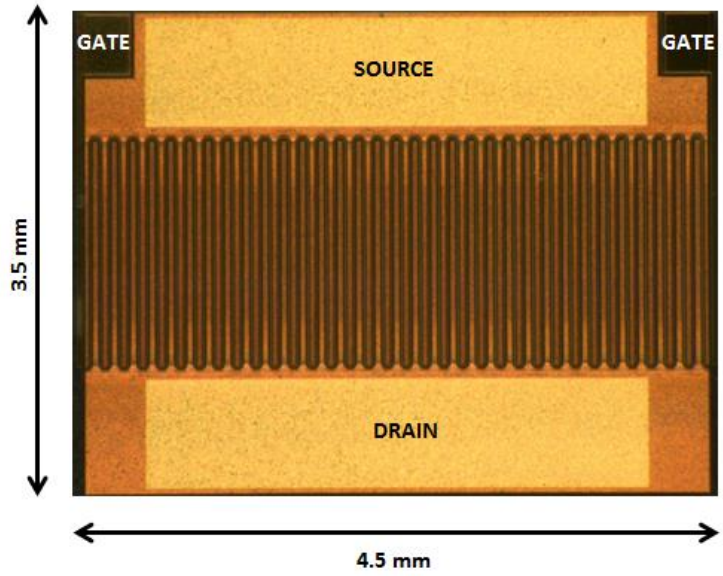
Figure 4.51 Clamped Inductive Switching evaluation (a) Setup (b) Waveforms

4.7 Pilot results of Wire-Bonded and Flip-Chip packaged devices

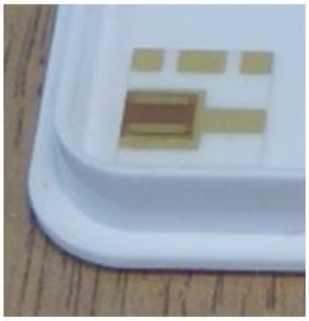
Along with wafer level characterisation, a few large area devices were also assembled using standard die-attach and wire-bonding as well as using Au stud-bumping and flip-chip packaging. This section will present the key pilot results. Figs. 4.52 (a) - (c) show images of a diced section of the *GaN-on-SiC-1 (S'ton)* wafer, Serpentine Gate PSJ HFET and after the device was die-attached on a pre-patterned ceramic substrate.



(a)



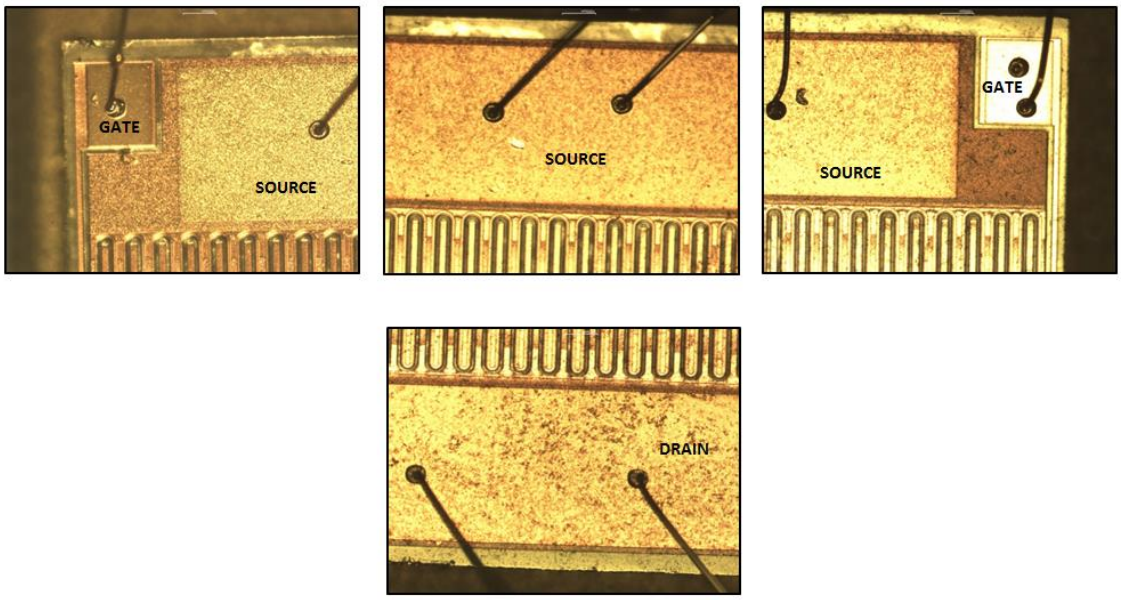
(b)



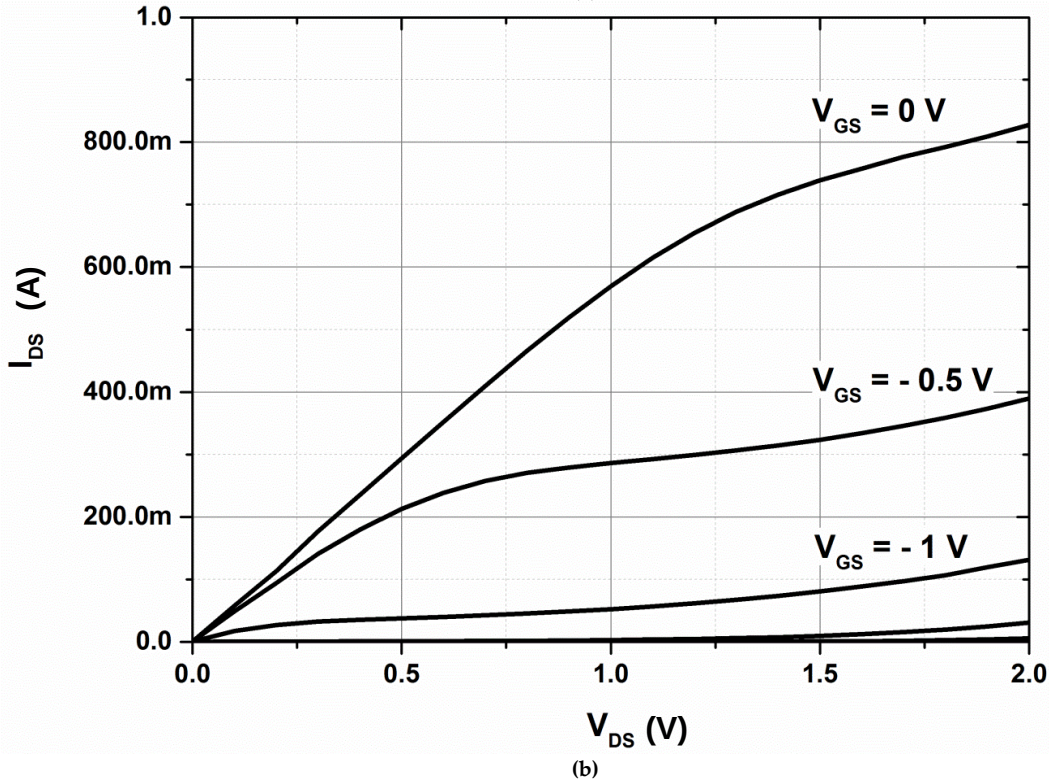
(c)

Figure 4.52 Picture of (a) diced section of the GaN-on-SiC-1 (S'ton) wafer (b) Serpentine Gate PSJ HFET (width = 100 mm) (c) Post die-attach on a pre-patterned Alumina substrate

Die-attach was performed on Cammax ED B80, using an Indium based solder (Composition: In (80%) – Pb (15%) – Ag (5%)) and wire-bonding was performed using K&S 4524 Ball Wire-bonder with 50 μm Au wires. Fig. 4.53 (a) shows the micrographs post wire-bonding and output characteristics of the wire-bonded PSJ HFET have been shown in Fig. 4.53 (b).



(a)



(b)

Figure 4.53 (a) Micrographs of wire-bonded PSJ HFET (b) Output Characteristics

The on-state resistance of the wire-bonded HFET was calculated as ~ 1.66 Ω (166 Ω.mm, width = 100 mm) translating to a specific on-state resistance of ~ 112.5 mΩ.cm^2 (active area considered is 1.5 mm (finger length) x 4.5 mm). The relatively high value can be attributed to the sub-optimal contact resistance in these devices which can be easily improved by two orders of magnitude by optimising the N-contact RTA process.

Flip-chip packaging is a highly desired approach for assembling GaN based devices due to their inherent speed and sensitivity to parasitic inductance with standard wire-bonding methods of assembly. There are also benefits in terms of better electrical efficiency and thermal management.

The typical process includes Au stud bumping of the pads on the devices, precision placement, and thermo-sonic/thermo-compression bonding on to the pre-patterned metal tracks on a ceramic substrate, followed by application of an under-fill material.

The geometrical layout (pad size, minimum distance between Gate to Source pads/tracks and so on...) of the multi-finger devices had been defined based on the flip-chip packaging capability and specifications defined by an initial facility that subsequently withdrew from the project. Hence, the patterned ceramic substrates on to which the devices were to be flip-chipped had to be custom built.

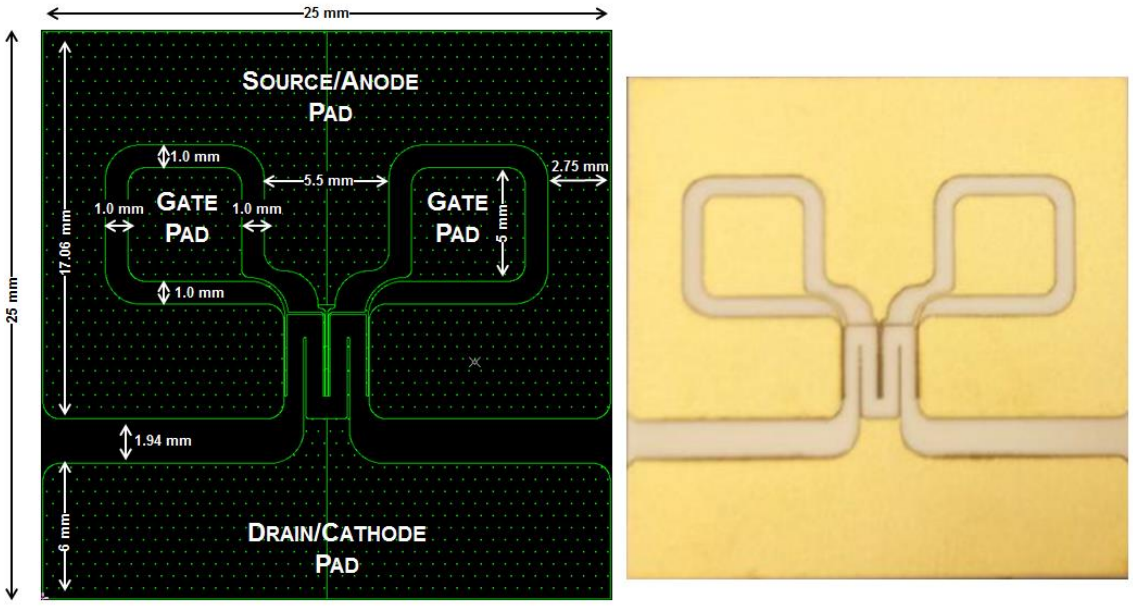
Ceramic substrates (25 mm x 25 mm) with blanket metallisation were procured. The specifications of the metallisation (stack and thickness) were decided based on the requirement for effective thermo-compression bonding as well as the maximum thickness of metal that could be reliably ablated during the Laser Micromachining process required for patterning of the substrates.

Considering these aspects, the metal stack was defined as mentioned below:

Ag: Cu: Ni: Au = 10 μm: 7-12 μm: 1-2 μm: 0.75 – 1.25 μm

However, the supplied material had the following stack, as conveyed by the supplier; Ag: Cu: Ni: Au = ~ 20 μm: 7.5 μm: 2 μm: 0.9 μm. The increase in metal stack substantially increases the challenge of laser micromachining with the risk of ablated material getting deposited on the metal tracks, during the process.

A few trials were performed and Figs. 4.54 (a-b) show pictures of the pattern as drawn using Mentor Graphics IC Station and the patterned substrate respectively. The pattern was drawn such that a single patterned layout could accommodate all types of devices (Multi-finger PSJ HFETs as well as Diodes, of various current ratings) that had been fabricated.



(a) (b)

Figure 4.54 Pictures of (a) Pattern as drawn on Mentor Graphics IC Station (b) Patterned substrate post Laser Micro-Machining

The devices were to be placed in the central region of the substrate with the individual metal tracks that geometrically correspond exactly to the pad regions on the device. Fig. 4.55 shows the micrograph of this region as well as three-dimensional image of a metal track obtained with Keyence VHX-100, as well as

surface profilometry data confirming that the overall metal thickness was actually > 40 μm.

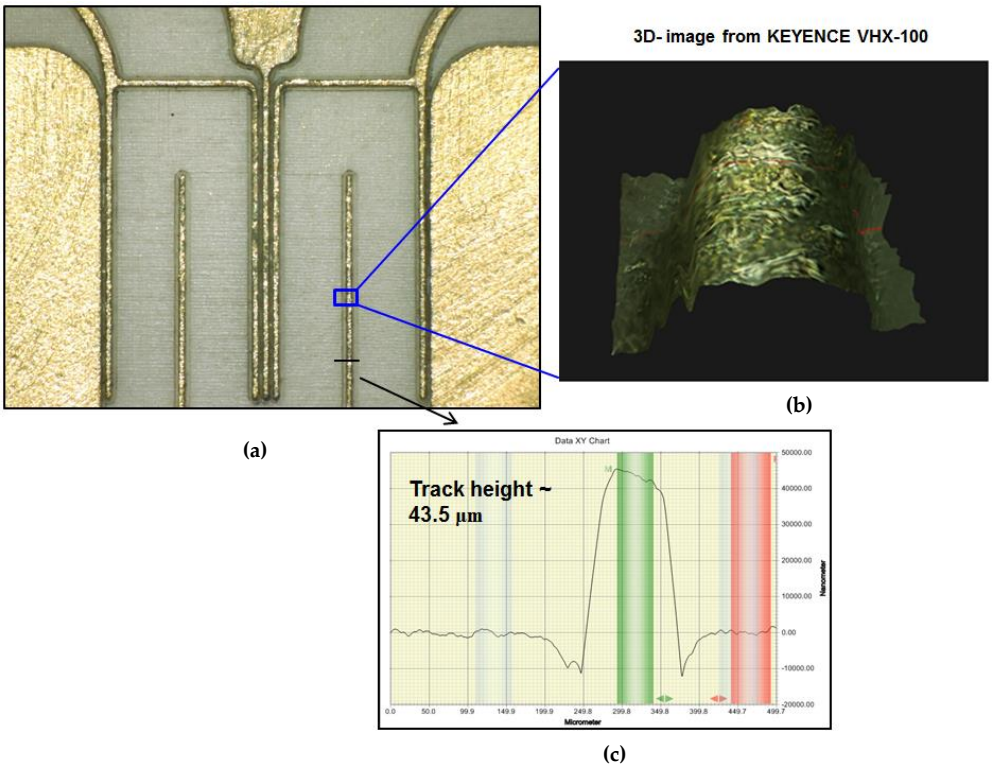


Figure 4.55 (a) Micrograph of the region where devices will be bonded to the substrate (b) three-dimensional image of a metal track (c) surface profilometry data

X-ray image of a Au stud-bumped (dark dots) and flip-chipped large area PSJ diode (4.5 mm x 2.4 mm) has been shown in Fig. 4.56 below.

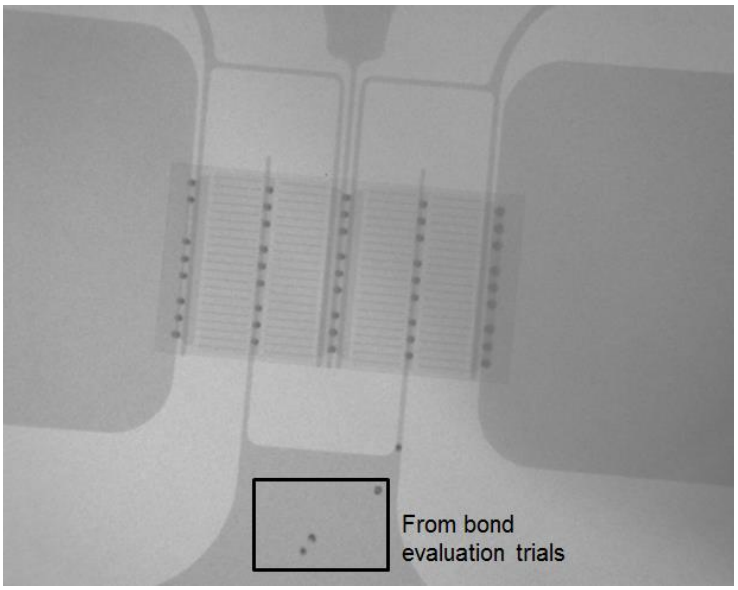
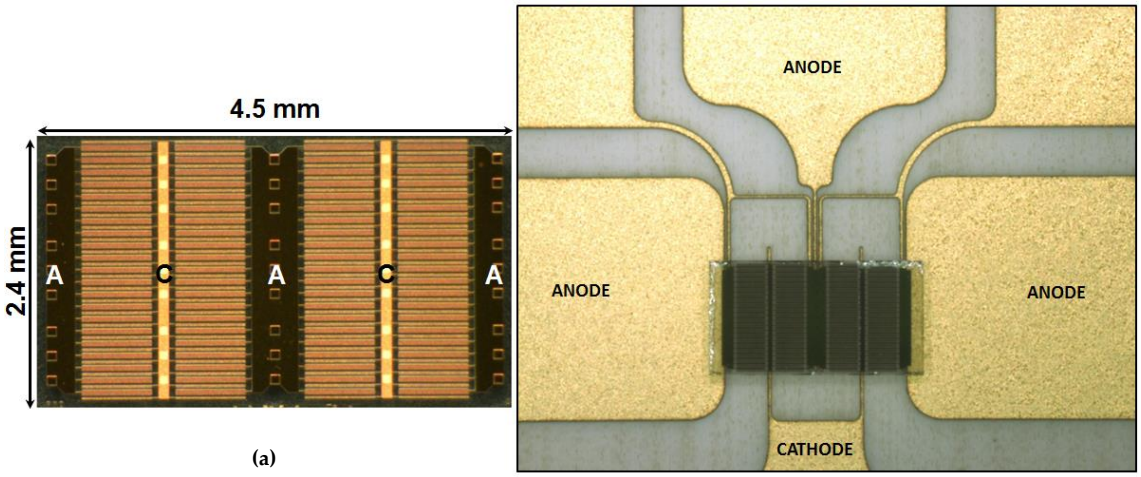


Figure 4.56 X-ray image of a Au-stud bumped and flip-chipped device (Courtesy : Optocap Ltd.)

After the initial trials, a large area PN Diode from *GaN-on-SiC-2 (S'ton)* was flip-chip packaged as shown in Fig. 4.57 (b).



(a) (b)

Figure 4.57 Images of (a) A large area PN Diode (4.5 mm x 2.4 mm, width = 100.8 mm) (b) Post flip-chip packaging

Forward characteristics of the packaged PN Diode have been shown in Fig. 4.58.

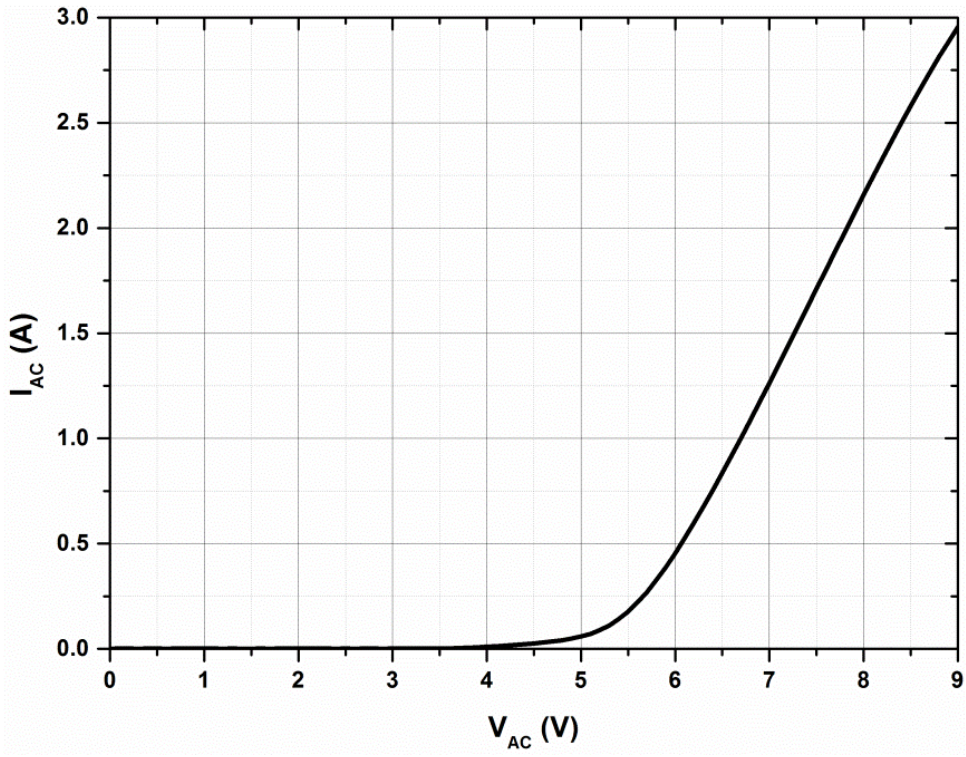


Figure 4.58 Forward characteristics of a flip-chip packaged large area PN Diode (4.5 mm x 2.4 mm, width = 100.8 mm)

The diode on-state resistance was calculated as 1.175 Ω (118.4 Ω.mm, width = 100.8 mm) translating to a specific on-state resistance of ~ 67.7 mΩ.cm^2 (active area considered is 4 x 0.6 mm (finger length) x 2.4 mm).

4.8 Key challenges

The key challenges of PSJ technology development have been enumerated below:

1. P-type doping of GaN cap layer: Mg activation ratio of 1% at a doping concentration of 3 x 10^{19} cm^{-3} results in an effective doping concentration in the range of 10^{17} cm^{-3}. The p-GaN layer hence has a high sheet resistance and affects the conduction performance of the discrete and intrinsic anti-parallel PN diodes integrated in the PSJ HFETs.
2. Low 2DHG mobility: Based on Hall measurements, the 2DHG mobility achieved is less than 20 cm^2/V.sec in the PSJ structures used in this work. Although this doesn't affect the current handling capability of the PSJ transistors, the performance of the discrete as well as integrated anti-parallel PN diodes will be limited by low 2DHG mobility.
3. Ohmic contacts: Achieving good n-contact and p-contact are both critical for obtaining high efficiency PSJ devices due to the combined contribution of 2DHG and 2DEG during conduction in PSJ based PN Diodes. Achieving a good p-contact is particularly challenging and the contacts obtained with substantial optimisation of the metal stack as well as RTA conditions were at best quasi-ohmic, leading to an increased on-set voltage of the PN Diodes.
4. Controlled etching and uniformity across large devices/wafers: The processing of PSJ devices involves two stages of etching of GaN layers, namely the isolation and PSJ mesa etching. Controlling isolation etching is required from the point of view of ensuring continuity of contacts from

pads to the active area of the devices. Controlling PSJ Mesa etching is more critical, as the residual AlGaN barrier thickness has to be maintained at ~ 20 nm to ensure high 2DEG density and obtaining good ohmic n-contacts. In the case of large area devices, this step is extremely critical, as variations can cause non-synchronised activation of the individual cells and can lead to non-uniform distribution of current within the devices. Therefore, thickness control as well as uniformity of the etched AlGaN barrier layer are critical and were observed to be largely sensitive to the equipment capability.

5. Etch induced damage: It's well known that plasma based dry-etching can lead to crystallographic damage to the etched regions, translating to high Schottky leakage current in the fabricated devices. This is therefore an additional aspect that has to be carefully addressed (optimised etch recipes, inclusion of GaN cap layer...) along with controlling the thickness and uniformity of etching.

4.9 Summary

In this chapter, the performance and electrical characterisation results of test structures as well as various large area Polarisation Super Junction (PSJ) devices were presented and discussed in detail.

The discussion commenced with characterisation results of high voltage PSJ GaN Schottky Barrier Diodes (SBD) on semi-insulating 6H-SiC substrates. Detailed electrical characterisation through measurement of forward I-V characteristics, reverse I-V characteristics and Capacitance Voltage (CV) measurements provided insight on the functionality and performance of the devices. Breakdown Voltage (V_{BR}) values of the devices scaled up linearly with PSJ drift length with an average critical electric field strength of ~ 0.8 MV/cm. Fabricated PSJ Diodes with drift length of 25 μm showed low on-set voltage of ~

0.4 V, high V_{BR} of ~ 2400V, specific on-state resistance ($R_{ON}.A$) of ~ 14 mΩ.cm^2 and a Power Device Figure of Merit ($PDFOM = V_{BR}^2 / R_{ON}.A$) of ~ 400 MW/cm^2 comparable to some of the best reported values for field plated devices.

Subsequently, key electrical characterisation results of large area PSJ Diodes, HFETs and PN Diodes fabricated on various SiC and Sapphire substrates, were presented. A detailed assessment of the dominant factors determining the scalability performance was provided with the aid of detailed characterisation of devices and test structures as well as ANSYS electrical simulations. These results are critical to take the technology to the next stage and further development activities.

Following that, a detailed discussion on the static and dynamic characterisation of the Intrinsic Diode and Dynamic Clamping Capability of PSJ HFETs was presented. The chapter was concluded with the pilot results of standard wire-bonded and flip-chip packaged PSJ large area devices.

4.10 References

[1] V. Unni, H. Long, M. Sweet, A. Balachandran, A. Nakajima, H. Kawai, and E. M. Sankara Narayanan, "2.4kV GaN Polarisation Superjunction Schottky Barrier Diodes on Semi-Insulating 6H-SiC Substrate," in *Proceedings of the 26th International Symposium on Power Semiconductor Devices & ICs*, Waikoloa, Hawaii, June 15-19, 2014, pp. 245–248.

[2] Y. Lv, Z. Lin, T. D. Corrigan, J. Zhao, Z. Cao, L. Meng, et al., "Extraction of AlGaN/GaN heterostructure Schottky Diode Barrier Heights from Forward Current-Voltage characteristics, " *Journal of Applied Physics*, vol. 109, 074512, 2011.

[3] J. Zhao, Z. Lin, T. D. Corrigan, Z. Wang, Z. You, and Z. Wang, "Electron mobility related to scattering caused by the strain variation of AlGaN

barrier layer in strained AlGaN/GaN heterostructures," *Applied Physics Letters*, vol. 91, pp. 173507-1 - 173507-3, 2007.

[4] L. Xue-Yang, Z. Kai, Z. Chang, Z. Wang, Z. Xue-Feng, E. Yun-Fei, et al., "Interface states in Al_2O_3/AlGaN/GaN metal-oxide-semiconductor structure by frequency dependent conductance technique," *Chinese Physics B*, vol. 23, no. 5, pp. 057301-1 - 057301-5, 2014.

[5] S. Saadaoui, M. M. B. Salem, M. Gassoumi, H. Maaref, and C. Gaquière, "Electrical characterization of (Ni/Au)/$Al_{0.25}Ga_{0.75}N$/GaN/ SiC Schottky barrier diode," *Journal of Applied Physics*, vol. 110, pp. 013701-1 - 013701-6 , 2011.

[6] I. C. Kizilyalli, A. P. Edwards, H. Nie, D. Bour, T. Prunty, and D. Disney, "3.7 kV vertical GaN PN diodes," *IEEE Electron Device Letters*, vol. 35, no. 2, pp. 247 -249, 2014.

[7] I. C. Kizilyalli, A. P. Edwards, H. Nie, D. Disney, T. Prunty, and D. Bour, "High voltage vertical GaN p-n diodes with avalanche capability," *IEEE Transactions on Electron Devices*, vol. 60, no. 10, pp. 3067 -3070, 2013.

[8] D. Disney, H. Nie, A. P. Edwards, D. Bour, H. Shah, and I. C. Kizilyalli , "Vertical power diodes in bulk GaN," in *Proceedings of the 25th International Symposium on Power Semiconductor Devices & ICs*, Kanazawa, May 26-30, 2013, pp. 59 -62.

[9] G. Simin, J. Wang, X. Hu, J. Yang, Z. Yang, R. Gaska, and M. Shur, "Ultra low-loss high power AlGaN/GaN HFET switches," *IEEE Power Electronics Specialists Conference*, June 15-19, 2008, pp. 85–87.

[10] Texas Instruments. Literature on Synchronous Rectification in High-Performance Power Converter Design [Online]. Available: http://www.ti.com/lit/an/snva595/snva595.pdf.

Chapter 5 GaN Polarisation Super Junction Devices on Silicon Substrates and Challenges to Monolithic Integration

This chapter initially presents key electrical characterisation results of GaN Polarisation Super Junction (PSJ) Diodes on Silicon (Si) substrates. The discussion then focusses on challenges to monolithic integration in high voltage GaN-on-Si technology platform. Crosstalk issues and increased on-state resistance of transistors when configured as High-Side switches are discussed in detail. Some of the results and discussion presented in this chapter have been published in the journals - *Microelectronics Reliability* and *Electronics Letters* [1-2].

5.1 Introduction

Although bulk GaN substrates are available today, a majority of GaN power semiconductor devices are fabricated with hetero-epitaxial GaN grown on non-native substrates such as Sapphire, Silicon Carbide (SiC) or Si substrates. Along with development of discrete devices, monolithic integration on the GaN-on-Si technology platform is also gaining traction, paving the way for system level integration of power electronic applications [3-7]. Performance assessment of monolithically integrated circuits requires the evaluation of crosstalk amongst the otherwise isolated devices and implications of the same. Crosstalk effects have been observed in Si power integrated circuits using Junction Isolation technology [8].

The focus of the work presented in this chapter has been to verify the main electrical characteristics (on-state and breakdown) of PSJ GaN-on-Si Diodes as well as evaluate the challenges to monolithic integration in a 650 V, GaN-on-Si technology platform.

5.2 Sample Preparation

The samples were fabricated at POWDEC K.K, Japan using their commercial process for a 650V PSJ GaN-on-Si technology. Undoped GaN/AlGaN/GaN heterostructures capped with a p-GaN layer (doped with Mg) were grown by MOCVD on p-type doped Si substrates (substrate resistivity: 1-50 Ω.cm). The concept of PSJ (charge compensation achieved in a double heterostructure) and functionality of devices based on this concept have been discussed in the previous chapters. Device-to-Device isolation in this GaN-on-Si platform was achieved by an overall mesa etch of 300 nm into the undoped GaN buffer layer using an ICP-RIE etch process. PSJ Diodes and transistors of varying drift lengths and width were fabricated.

5.3 Electrical Characteristics of PSJ GaN-on-Silicon Diodes

Figs. 5.1 (a) - (b) show top view micrograph and cross-section schematic of three Hybrid Schottky Barrier Power Diodes (device width = 100 μm) from the GaN-on-Si chip used for the investigation. The PSJ drift lengths in the three diodes are 10 μm, 15 μm and 20 μm respectively, as also indicated by the metallised labels just above the devices. Anode and Cathode electrodes of the diodes have been indicated as A and C respectively in Fig. 5.1 (b).

Forward I-V characteristics of the diodes have been shown in Fig. 5.2. Breakdown characteristics of the diodes were initially measured under Fluorinert ambient and floating substrate conditions. The reverse I-V characteristics are shown in Fig. 5.3 (a).

Subsequently, on another set of diodes with PSJ lengths of 15 μm and 20 μm, the breakdown characteristics were measured under grounded substrate conditions and are shown in Fig. 5.3 (b).

The breakdown was observed to be destructive in all cases.

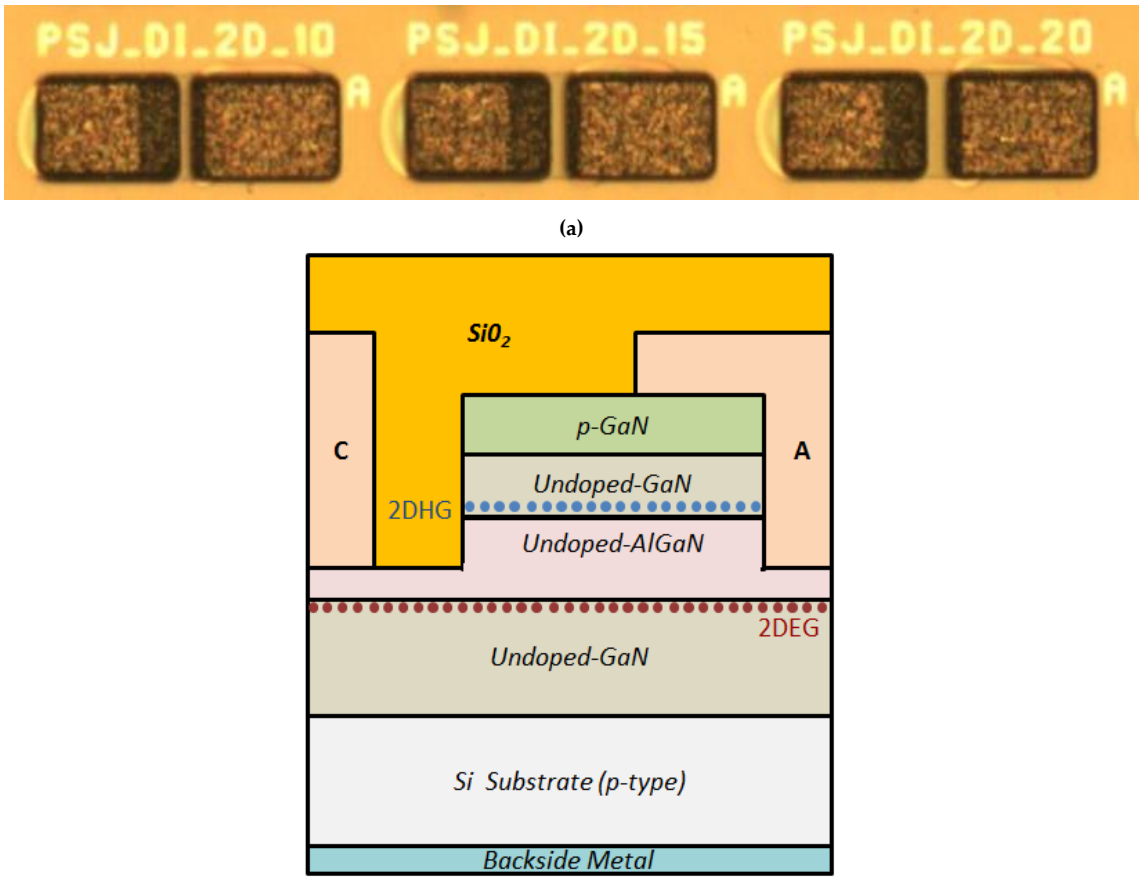


Figure 5.1 (a) Top view micrograph (b) Cross-section schematic of Hybrid Schottky Barrier Power Diodes (Width=100 μm)

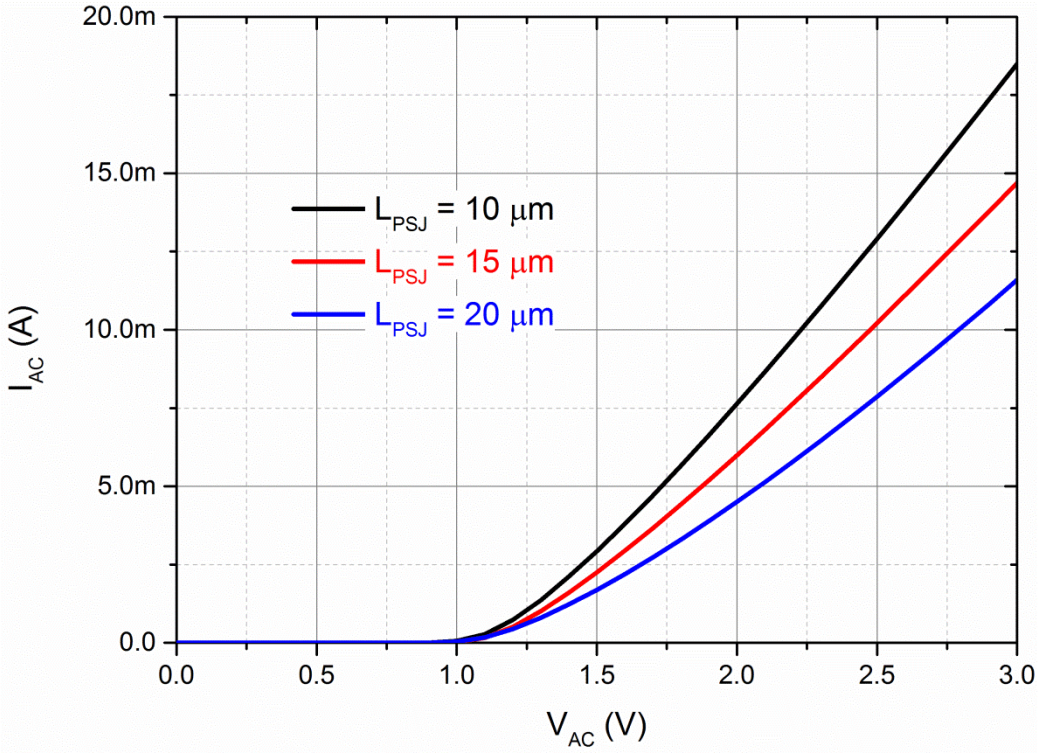
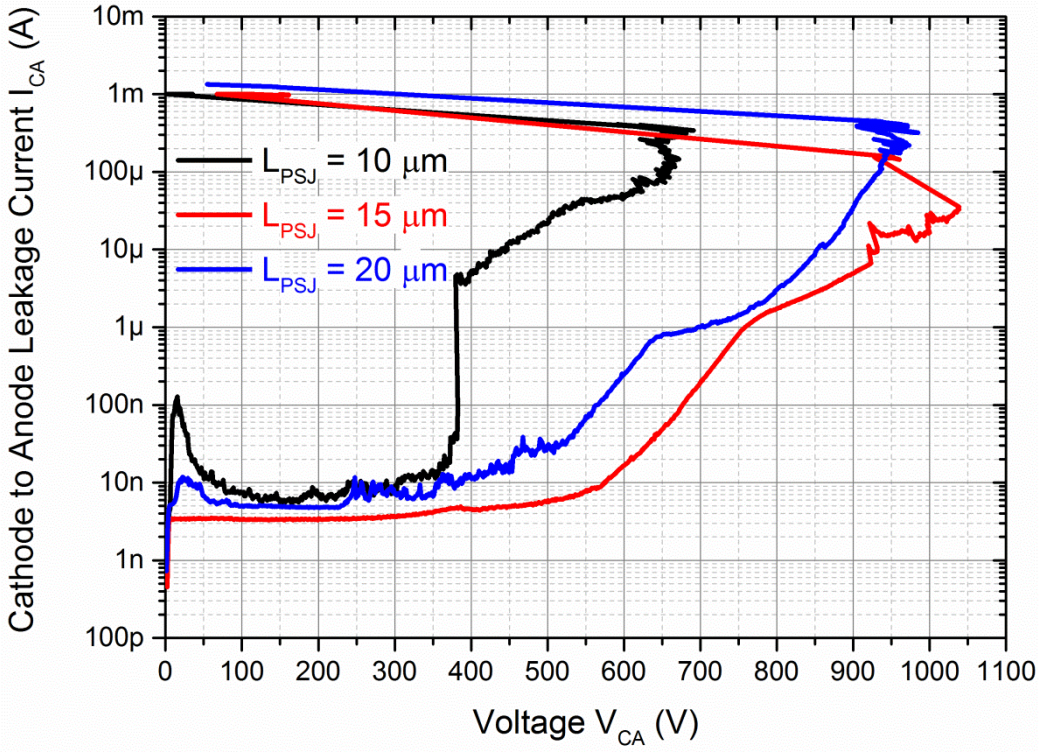
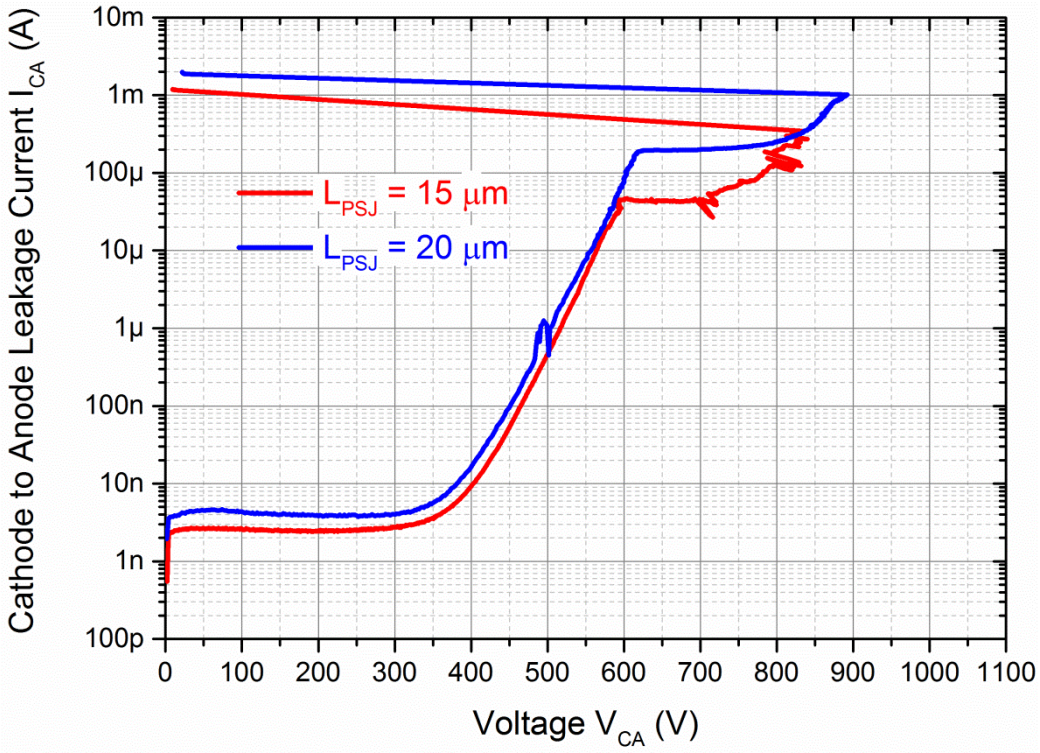


Figure 5.2 Measured forward I-V characteristics

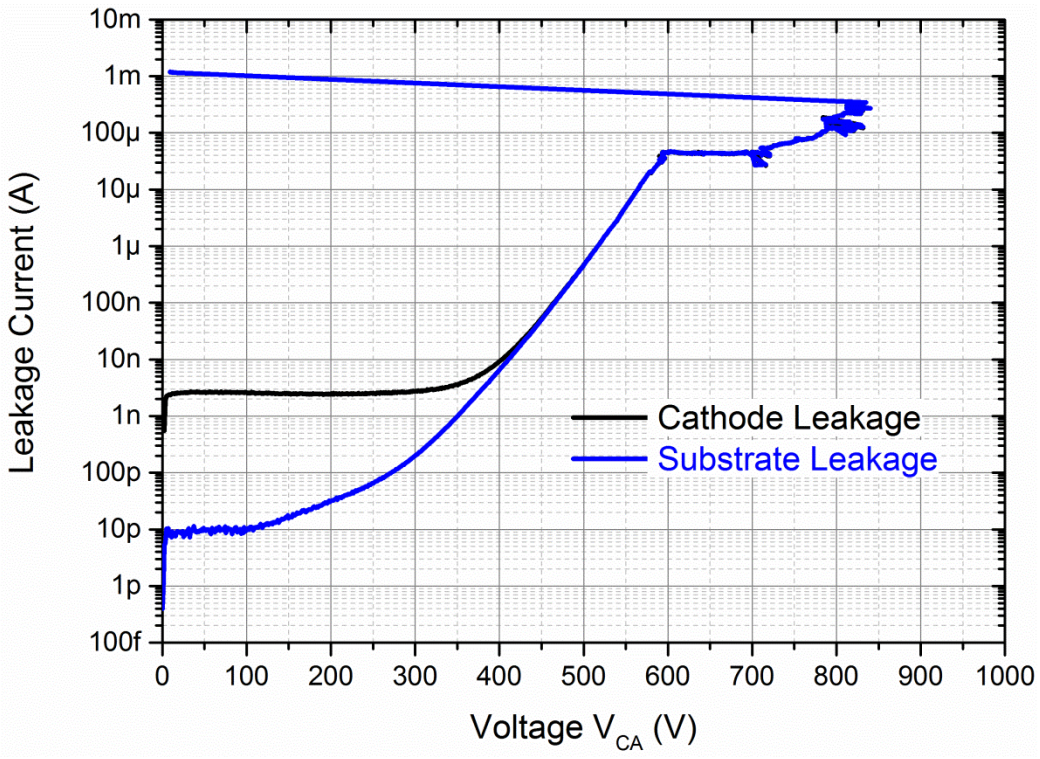


(a)

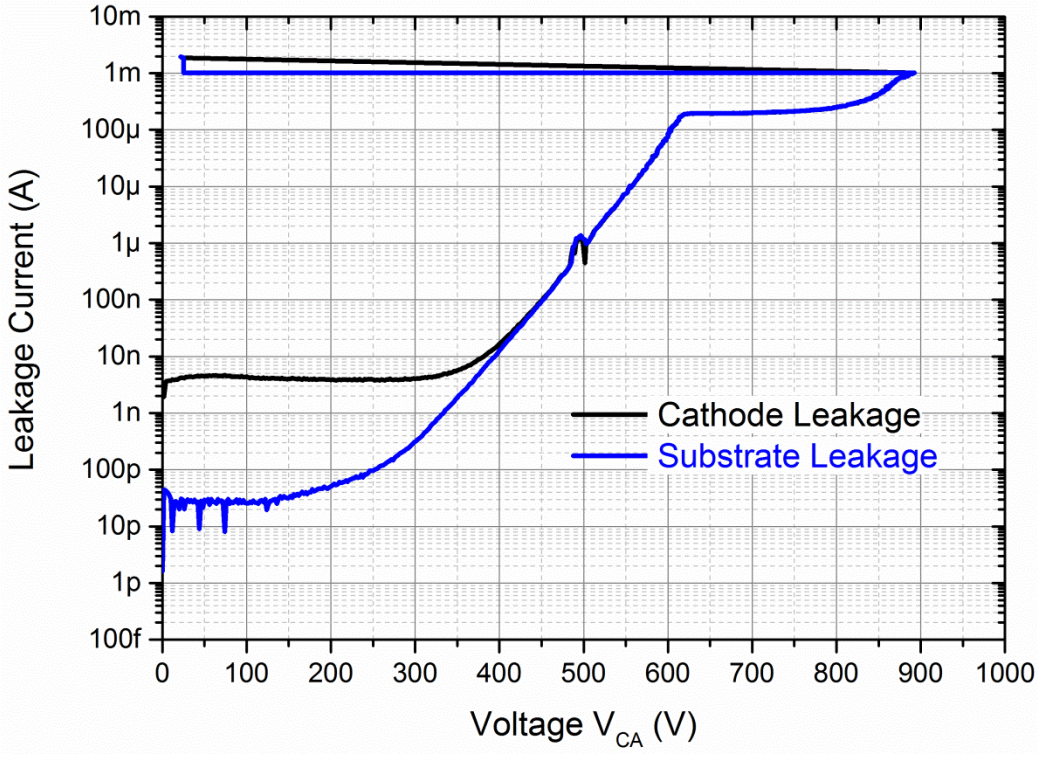


(b)

Figure 5.3 Measured reverse I-V characteristics (a) Floating Substrate (b) Grounded Substrate



(a)



(b)

Figure 5.4 Measured reverse I-V characteristics under grounded substrate conditions (a) L_{PSJ} = 15 µm (b) L_{PSJ}=20 µm

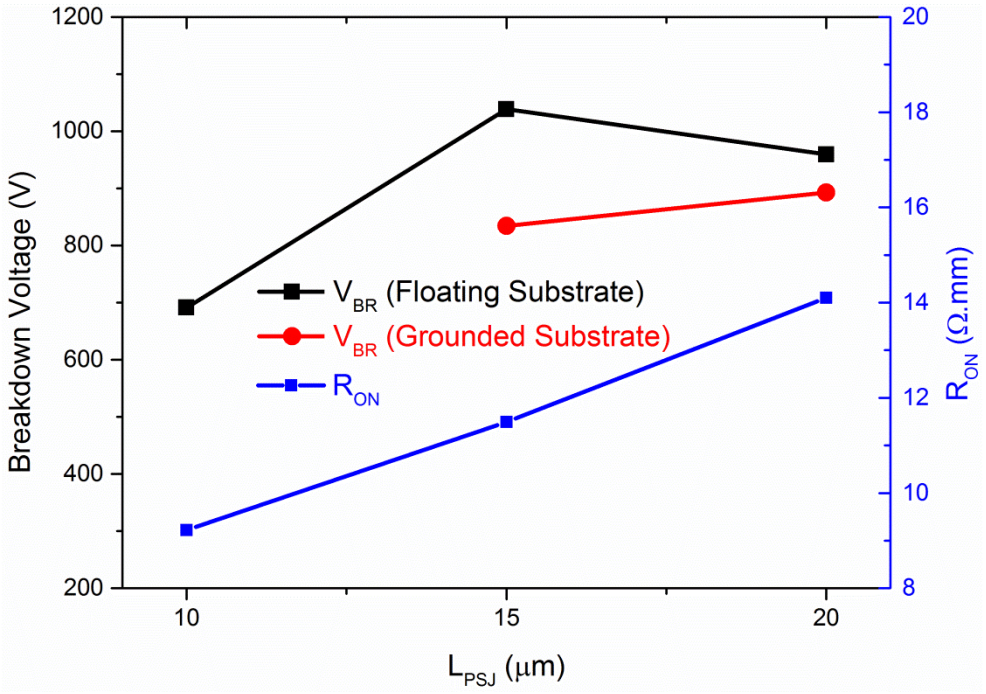


Figure 5.5 Breakdown Voltage (V_{BR}) and Normalised On-State Resistance (R_{ON}) versus L_{PSJ}

As shown in Fig. 5.3, the measured values for Cathode leakage current are at least an order of a magnitude lower under floating substrate conditions at V_{CA} = 650 V. However, there is a striking similarity in the leakage characteristics under the two conditions. Figs. 5.4 (a)-(b) show the reverse I-V characteristics under grounded substrate conditions also displaying the substrate leakage current. It is immediately apparent that the Cathode and substrate leakage currents are identical when V_{CA} is > 400 V, and that the leakage path is directed vertically from the cathode to substrate. The general similarity in the characteristics with the floating substrate conditions suggests that even when the substrate is left floating, there is a leakage path via the substrate. As clearly shown in Fig. 5.5, the V_{BR} values appear to saturate for PSJ length > 15 μm under floating as well as grounded substrate conditions. Such levelling-off of breakdown voltage values with increase in drift length in GaN-on-Si platform has been reported by many other groups and has been attributed to vertical breakdown ungoverned by the surface field profiling techniques, depending primarily on the buffer thickness [9-10].

5.4 Crosstalk in GaN-on-Silicon monolithic devices

5.4.1 Investigation methodology

Figs. 5.6 (a) - (b) show top view micrograph and cross-section schematic of two monolithically fabricated/co-located Hybrid Schottky Barrier Power Diodes from the GaN-on-Si chip used for the crosstalk investigation.

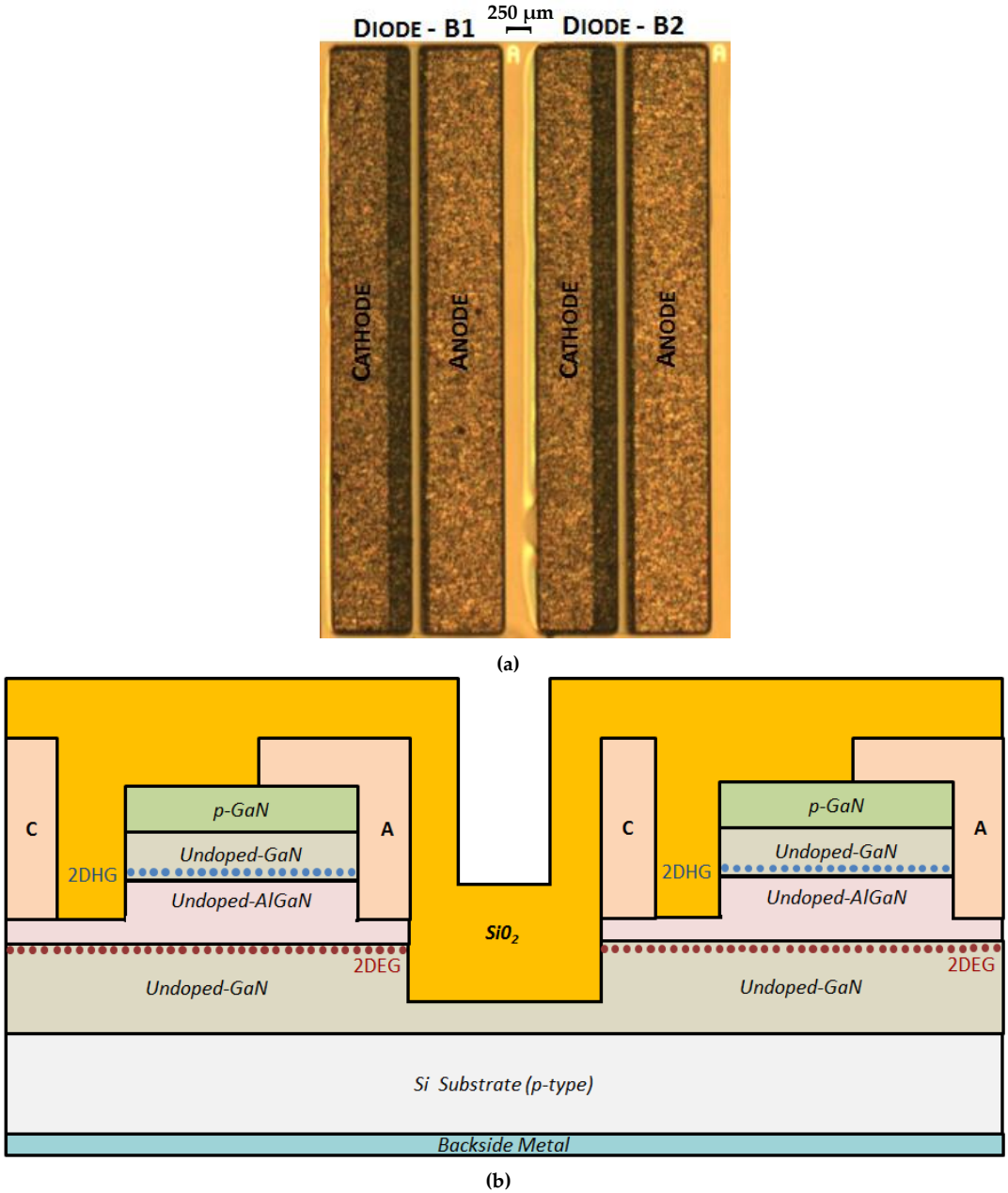


Figure 5.6 (a) Top view micograph (b) Cross-section schematic of Hybrid Schottky Barrier Power Diodes

The lateral separation between the two diodes labelled as B1 and B2 (device width = 1 mm) is 250 µm.

The methodology that was adopted to verify the presence of crosstalk amongst devices consisted of measuring the electrical characteristics of a given device (to be referred to as the primary device henceforth) without any perturbation initially, followed by biasing an electrode of a neighbouring device simultaneously during the measurement. Device characteristics under the respective conditions were then juxtaposed and compared. All measurements were performed on semi-automatic thermal Probe-station (Cascade Microtech - 10600) interfaced with Agilent B1500A Semiconductor Device Parameter Analyser.

Prior to verifying the presence of crosstalk, Device-to-Device Isolation characteristics were measured between the neighbouring electrode (Cathode of Diode B2) and the Anode and Cathode electrodes respectively of the primary device (Diode B1). The measurement indicated an isolation leakage current of < 1.5 nA at +/- 80V as shown in Fig. 5.7.

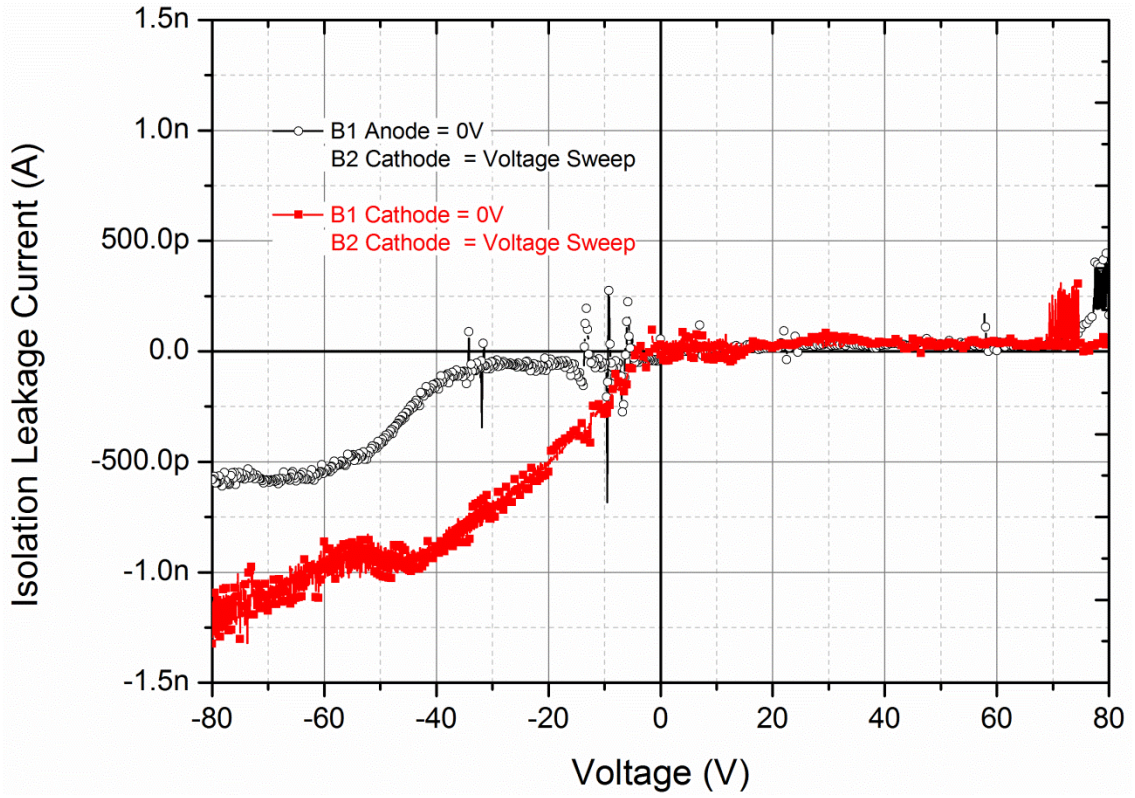


Figure 5.7 Device-to-Device isolation leakage characteristics

5.4.2 Floating Si substrate and simultaneous electrical biasing of electrode of a neighbouring isolated device

The measurement configuration has been illustrated in Fig. 5.8. Reference forward and reverse I-V characteristics of the primary device (Diode B1) were measured initially and subsequently with Cathode of Diode B2 biased at – 10 V, - 25 V and - 50 V respectively. Si substrate was unbiased and left floating during this measurement.

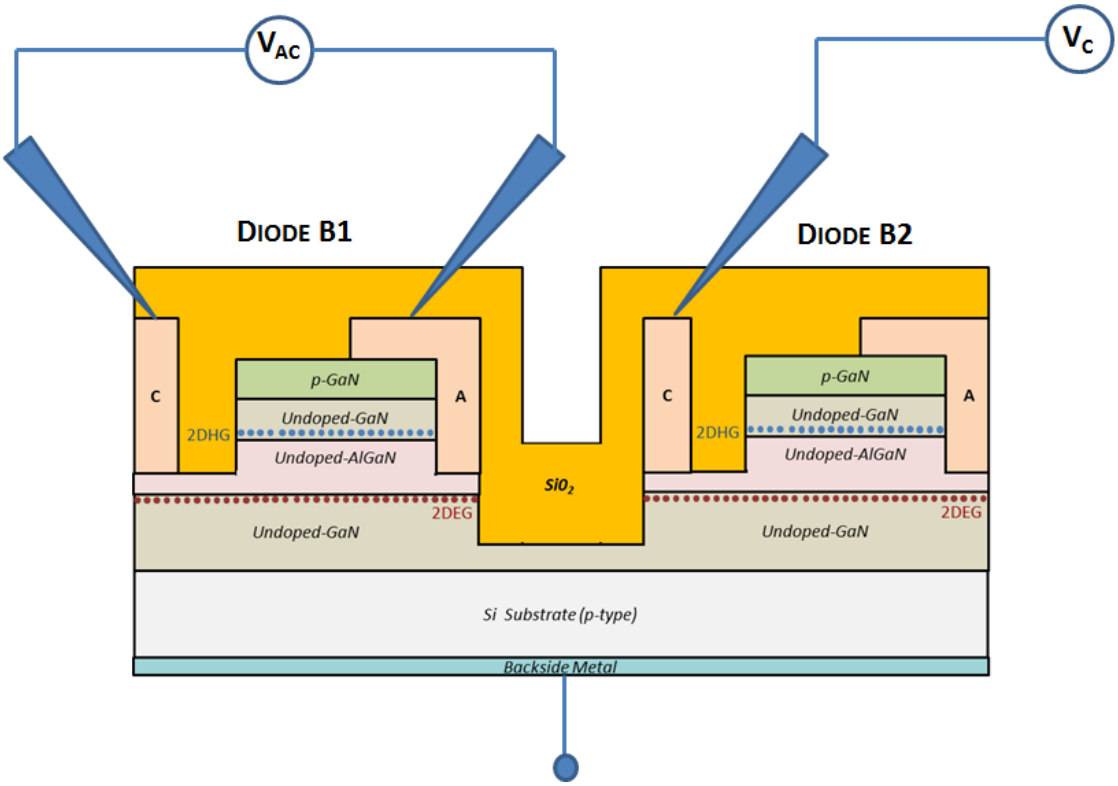


Figure 5.8 Measurement configuration to characterise the impact on the electrical characteristics (Forward and Reverse I-V) of the primary device with floating Si substrate and simultaneous electrical biasing of electrode of a neighbouring isolated device

The primary device reference/un-perturbed forward and reverse I-V characteristics as well as the characteristics under condition of perturbation have been shown in Figs. 5.9 (a)-(b) respectively. It is clearly noticeable that the forward current of Diode B1 systematically reduces when the cathode of the neighbouring Diode B2 is negatively biased and the impact on the on-state resistance correlates with the magnitude of the applied negative bias.

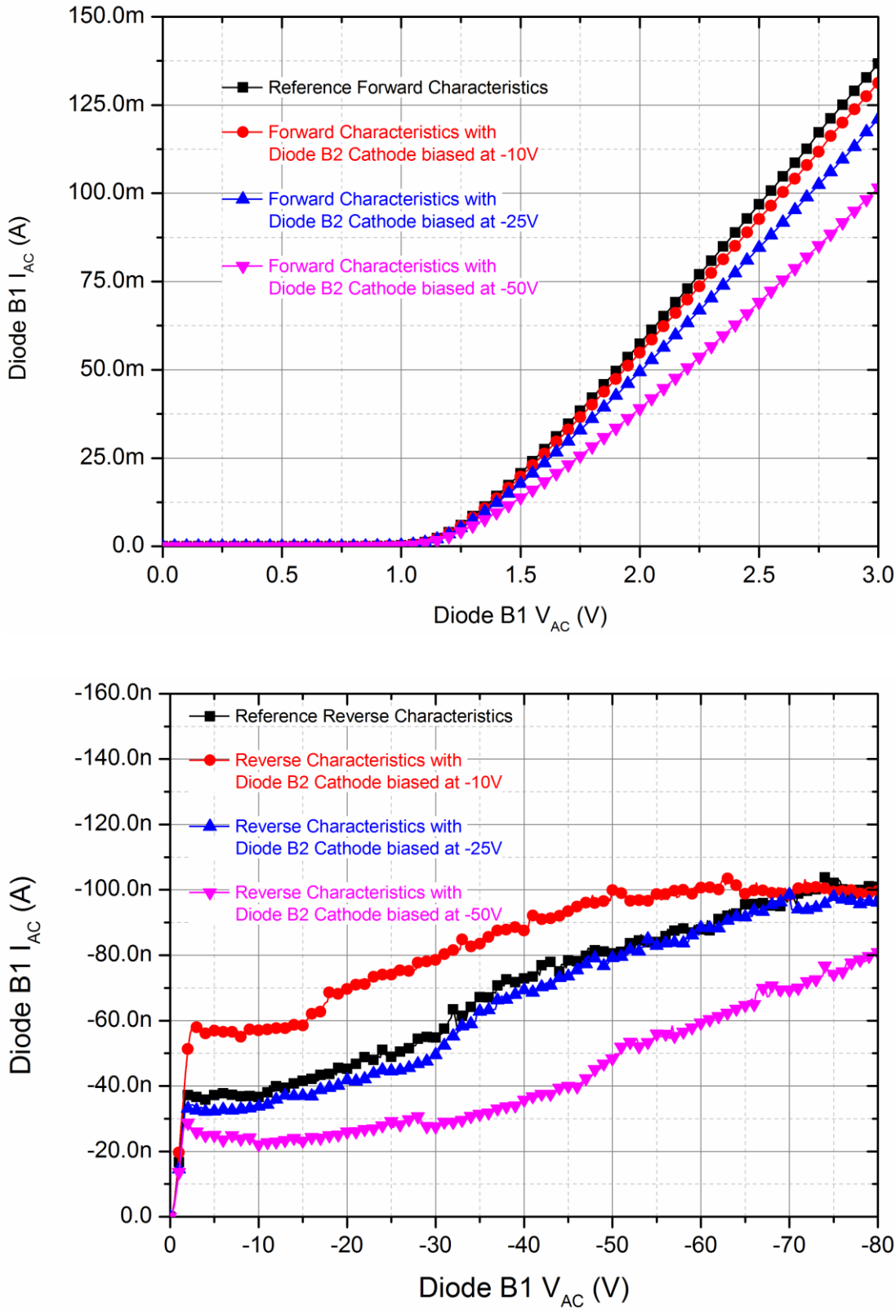


Figure 5.9 Impact on primary device - Diode B1 (a) Forward I–V characteristics (b) Reverse I–V characteristics, measured under floating substrate conditions

The reverse I-V characteristics of Diode B1 indicate that reverse leakage current of the primary device generally tends to reduce within the measured range initially, when the cathode of neighbouring Diode B2 is negatively biased. However, the reduction in leakage current becomes less apparent as the reverse voltage of the Diode B1 approaches – 80 V.

The evaluation was also performed on monolithically fabricated PSJ HFETs and Figs. 5.10 (a) - (b) show top view micrograph and cross-section schematic (along with biasing configuration) of the devices.

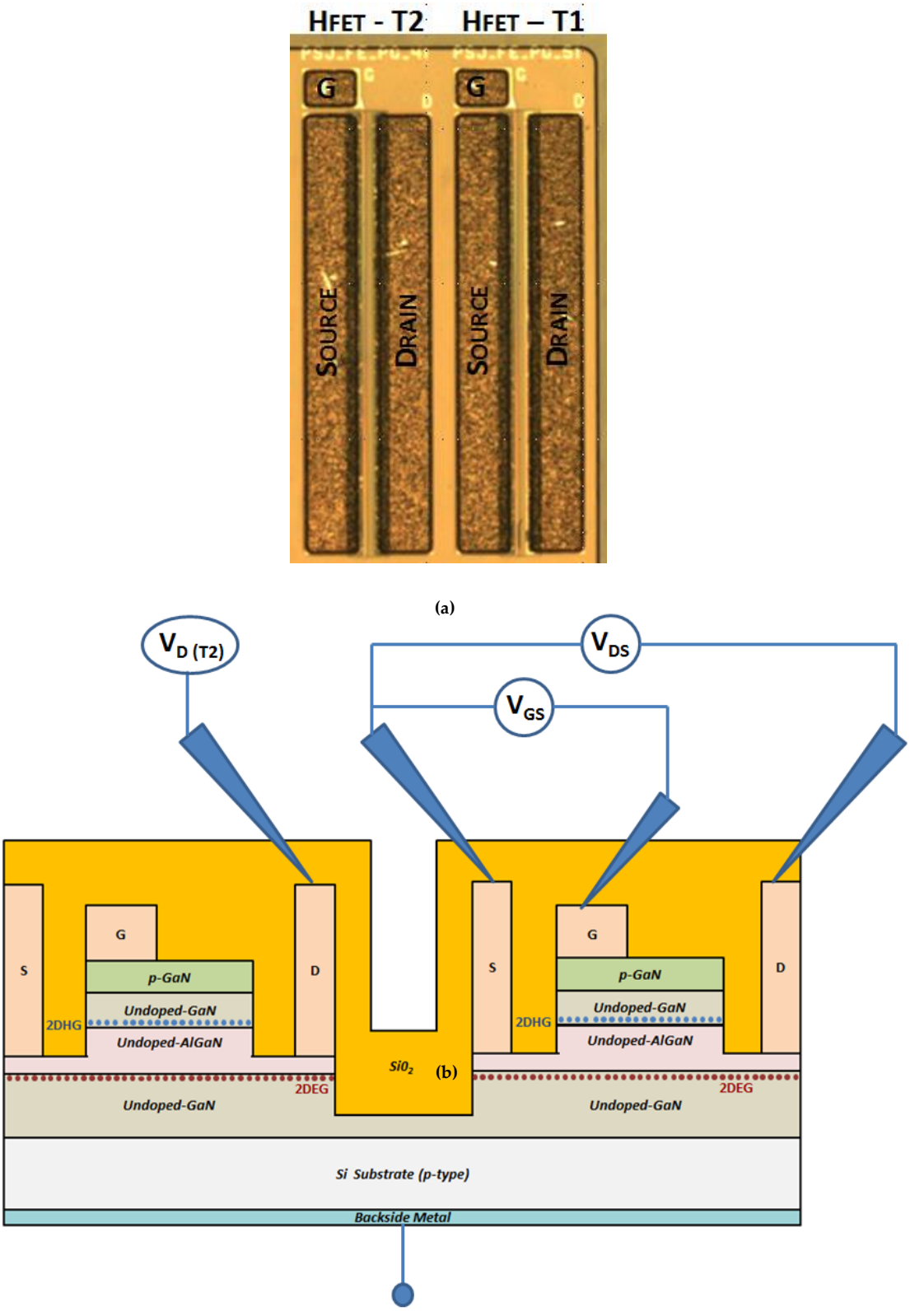
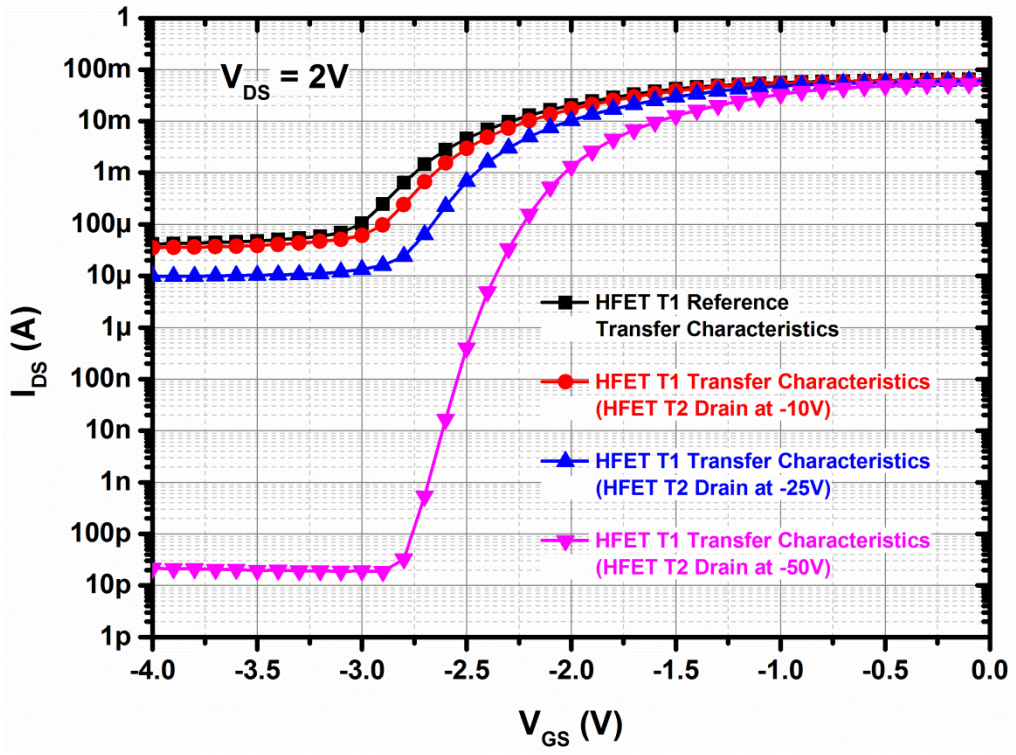
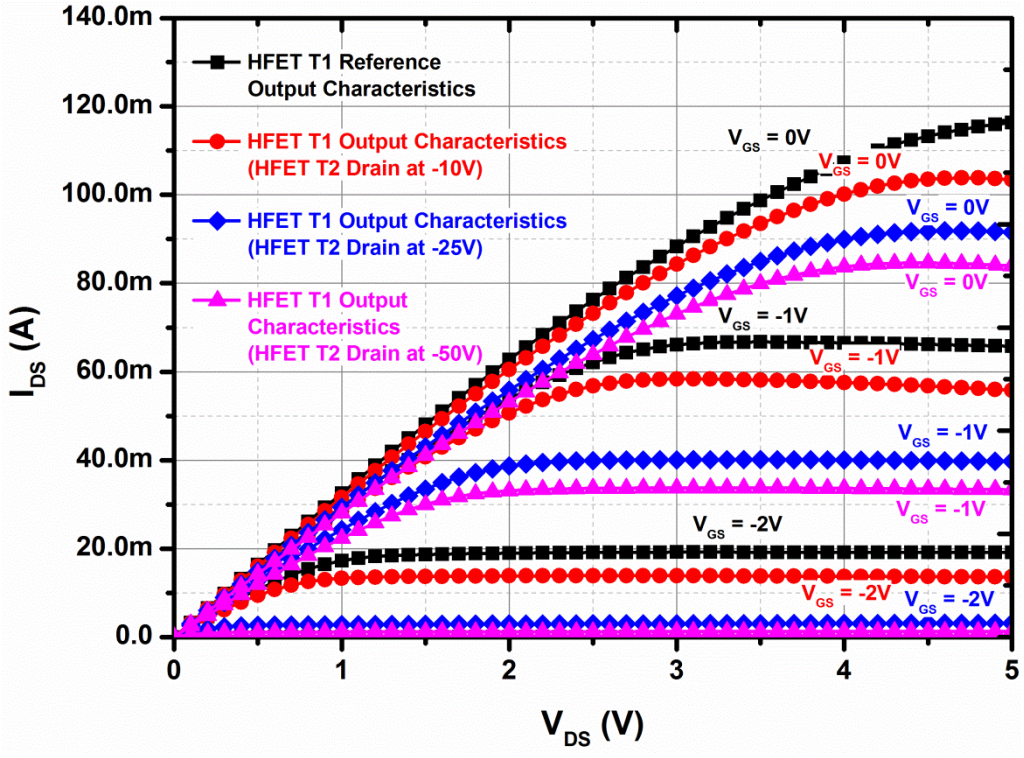


Figure 5.10 (a) Top view micrograph (b) Cross-section schematic of PSJ HFETs (width = 1 mm)



(a)



(b)

Figure 5.11 Impact on primary device - HFET T1 (a) Transfer characteristics (b) Output characteristics, measured under floating substrate conditions

The primary device (HFET T1) reference/un-perturbed transfer and output characteristics as well as the characteristics under conditions of perturbation

(negative bias on drain of HFET T2) have been shown in Figs. 5.11 (a)-(b) respectively. The perturbation leads to an increase in V_{TH} and compromises the output characteristics of the primary device (HFET T1). Substantial lowering of the off-state leakage is observed and it was confirmed that the path of the off-state leakage current is directed from Drain to Source electrode of HFET T1.

5.4.3 Electrical biasing of Si substrate only

The measurement configuration has been shown in Fig. 5.12.

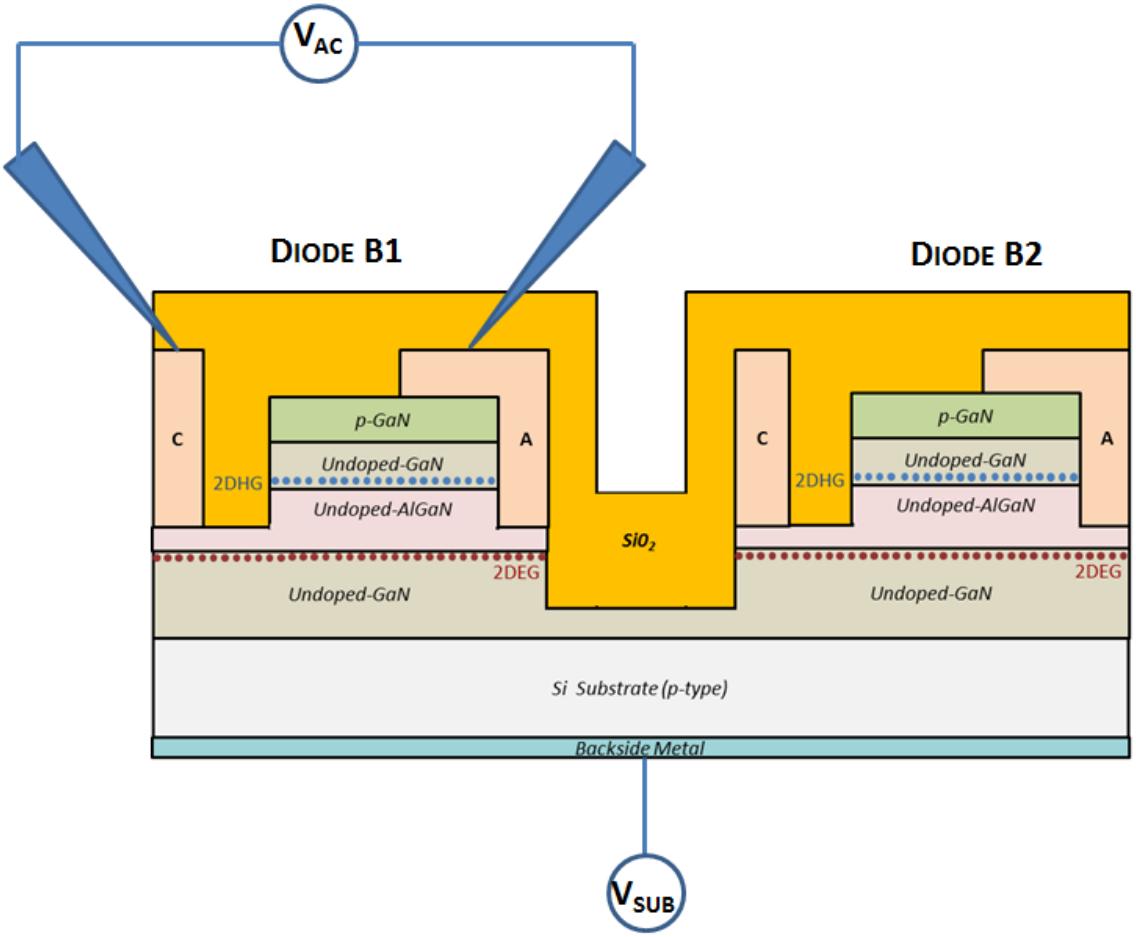
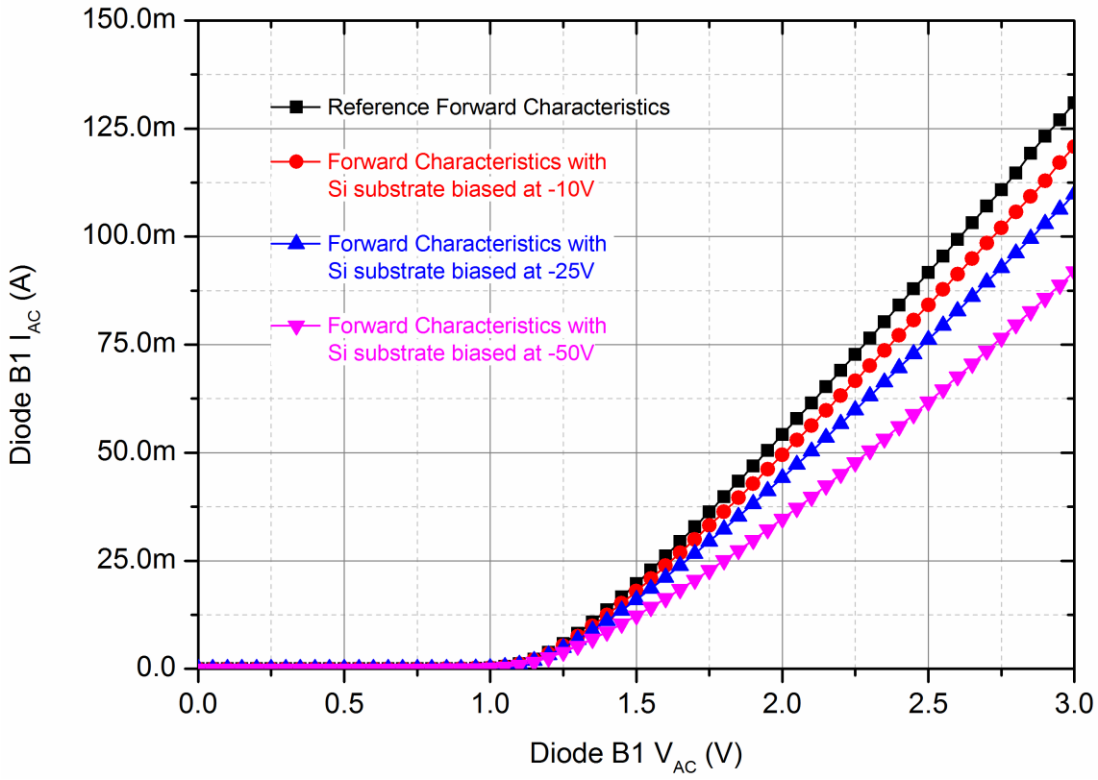
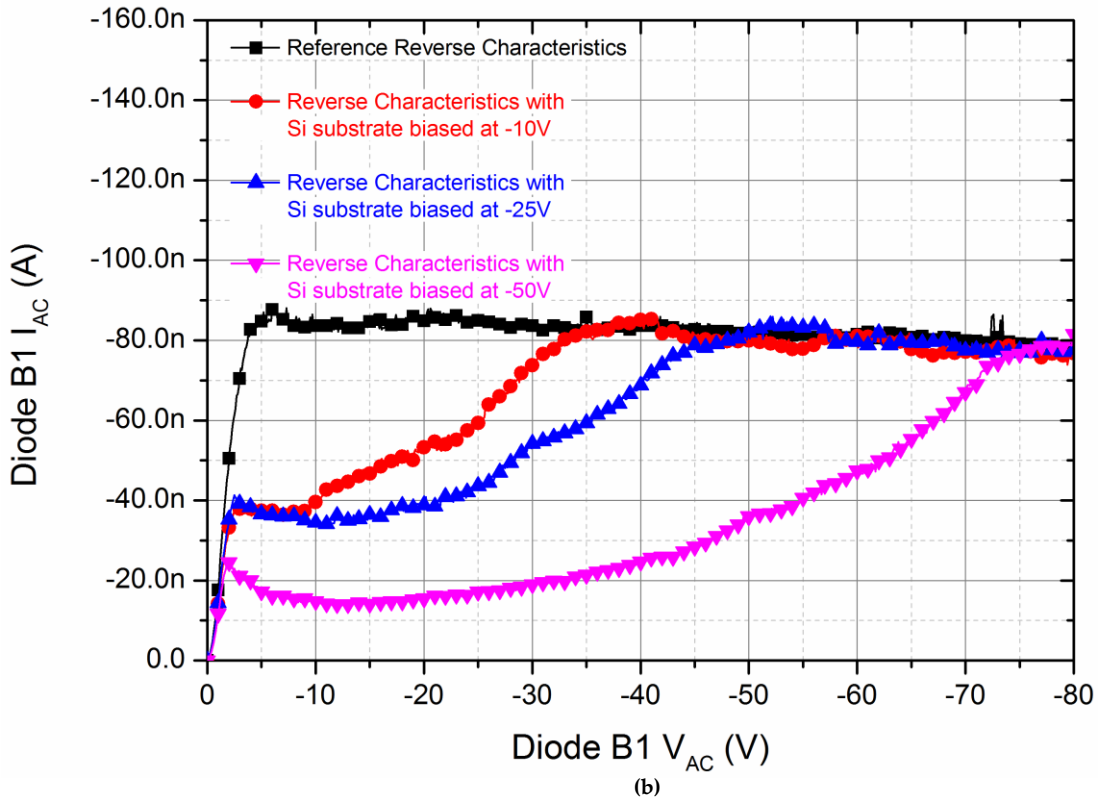


Figure 5.12 Measurement configuration to characterise the impact on the primary device electrical characteristics (Forward and Reverse I-V) with simultaneous electrical biasing of Si substrate only

Reference forward and reverse I-V characteristics of the primary device (Diode B1) were measured initially with unbiased substrate and subsequently with substrate biased at - 10 V, - 25 V and - 50 V respectively.



(a)



(b)

Figure 5.13 Impact on primary device - Diode B1 (a) Forward I–V characteristics (b) Reverse I–V characteristics

As shown in Figs. 5.13 (a)-(b), the impact on the forward I-V characteristics of primary device Diode B1 under substrate biasing conditions appear to correlate

with that of the characteristics observed when cathode of the neighbouring Diode B2 was negatively biased under floating substrate conditions. In the situation of reverse I-V characteristics, although a reduction is observed initially, the leakage current rises up to the value measured under un-perturbed condition at V_{AC} = - 35 V, V_{AC} = - 50 V, and V_{AC} = - 75V, for substrate biasing voltage values of - 10 V, - 25 V and - 50 V respectively.

5.4.3.1 Si substrate current

Figs. 5.14 - 5.15 show the Si substrate current measured when the primary device is forward and reverse biased respectively, for different substrate bias conditions.

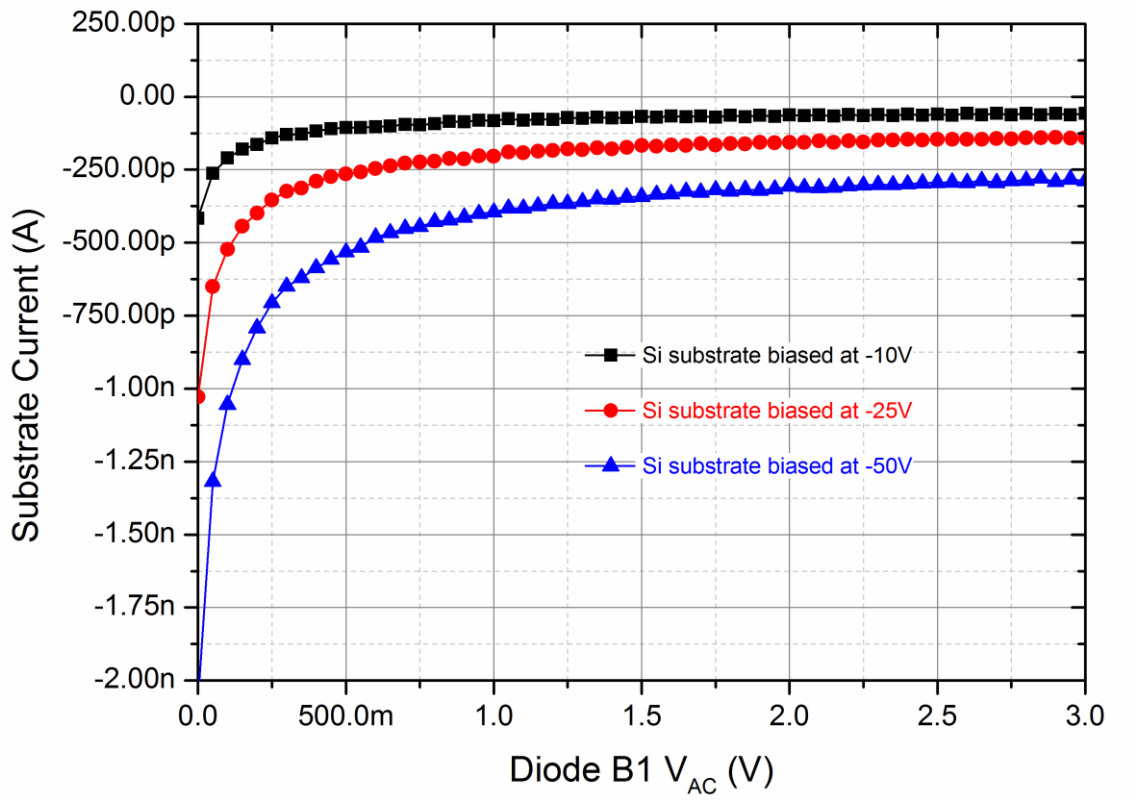


Figure 5.14 Si Substrate current, under substrate bias and forward biased primary device - Diode B1

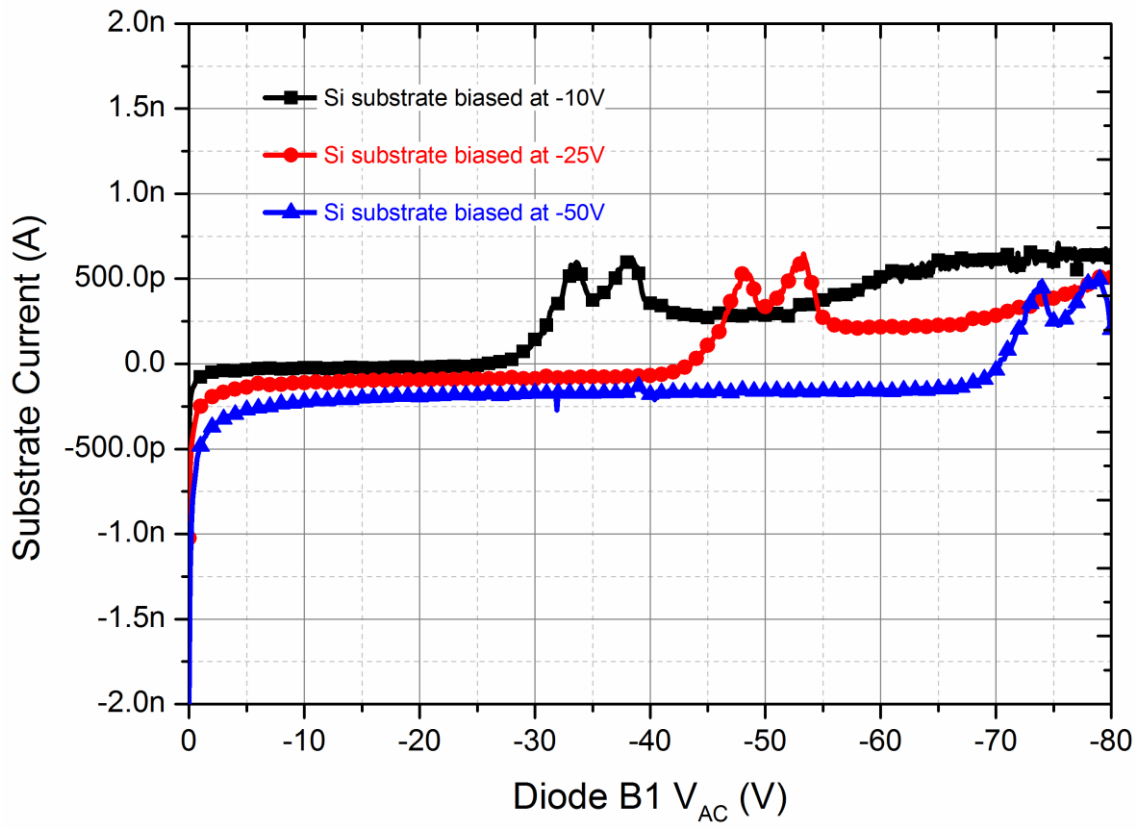


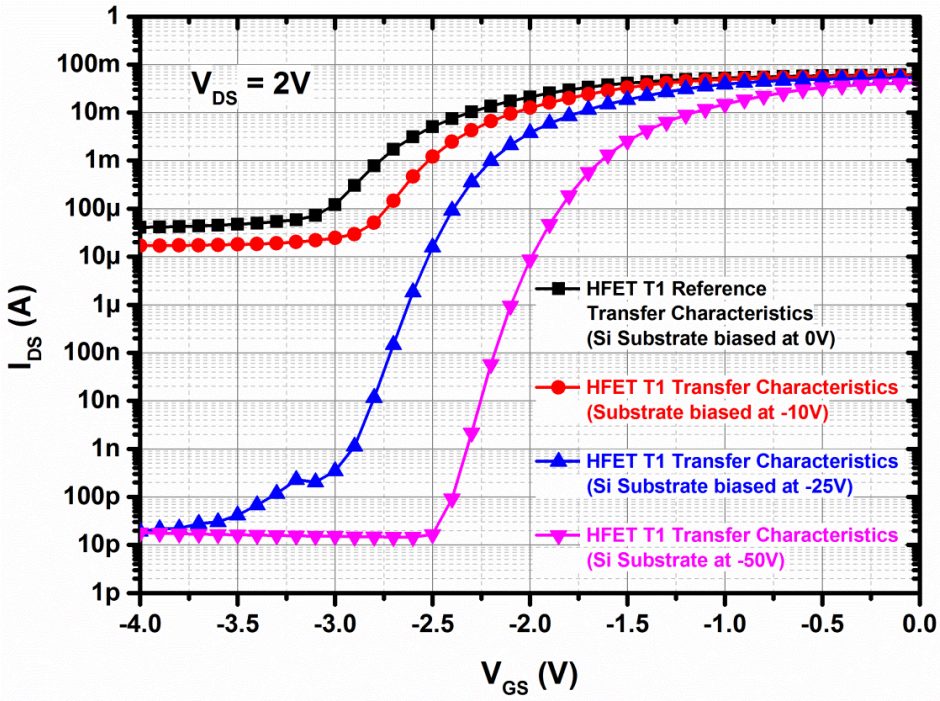
Figure 5.15 Si Substrate current, under substrate bias and reverse biased primary device - Diode B1

It is evident from the curves shown in Figs. 5.14 - 5.15 that the magnitude of substrate current is < 2 nA for biasing conditions in the entire range of measurement performed, irrespective of whether the primary device is forward or reverse biased.

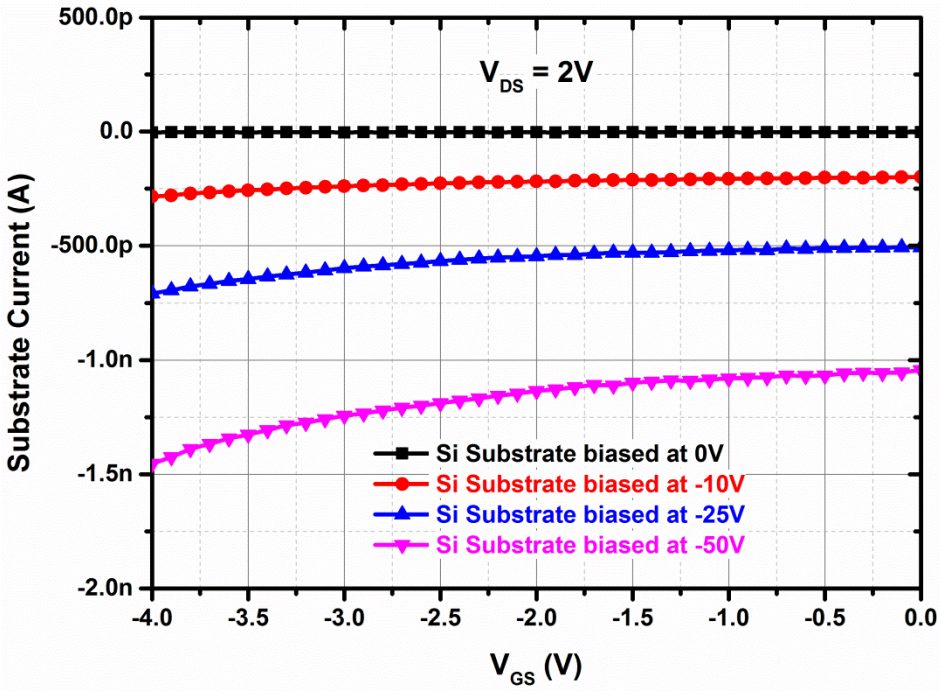
Another noticeable observation is that there is a change in the polarity of the substrate current when the reverse bias voltage applied across Diode B1 is at V_{AC} = - 30 V, V_{AC} = - 45 V, and V_{AC} = - 70 V, for substrate biasing voltage conditions of - 10 V, - 25 V and – 50 V respectively. The voltage values are very close to the V_{AC} values at which the reverse leakage current measured for Diode B1 reach and saturate at the reference leakage values under the same substrate biasing conditions, as shown in Fig. 5.13 (b). When the substrate is biased at a negative voltage and V_{AC} = 0 V, the substrate current flows from surface towards substrate and hence has a negative polarity. As V_{AC} becomes negative,

although the component of current from cathode to substrate is not expected to change (cathode potential is maintained at 0 V), there will be a reversal in the direction of the component of substrate current flowing from anode to substrate as the anode potential becomes more negative than that of the substrate. As the magnitude of the anode potential increases further (more negative), the component of substrate current flowing from substrate to anode continues to rise and at a certain anode potential, the resultant substrate current starts flowing upwards (from the substrate to anode), resulting in a change in overall polarity of the total substrate current. A consistent dual-peak has also been observed in the substrate current just after the polarity transition, at each of the substrate bias conditions and the origin of the same is under investigation.

Reference transfer characteristics and substrate leakage current as well as output characteristics of the primary device (HFET T1) have been shown in Figs. 5.16 (a) - (b) and 5.17 respectively. The measurements were performed initially with substrate biased at 0 V and subsequently with substrate biased at - 10 V, - 25 V and - 50 V respectively.



(a)



(b)

Figure 5.16 Impact on primary device – HFET T1 (a) Transfer characteristics (b) Si Substrate leakage current

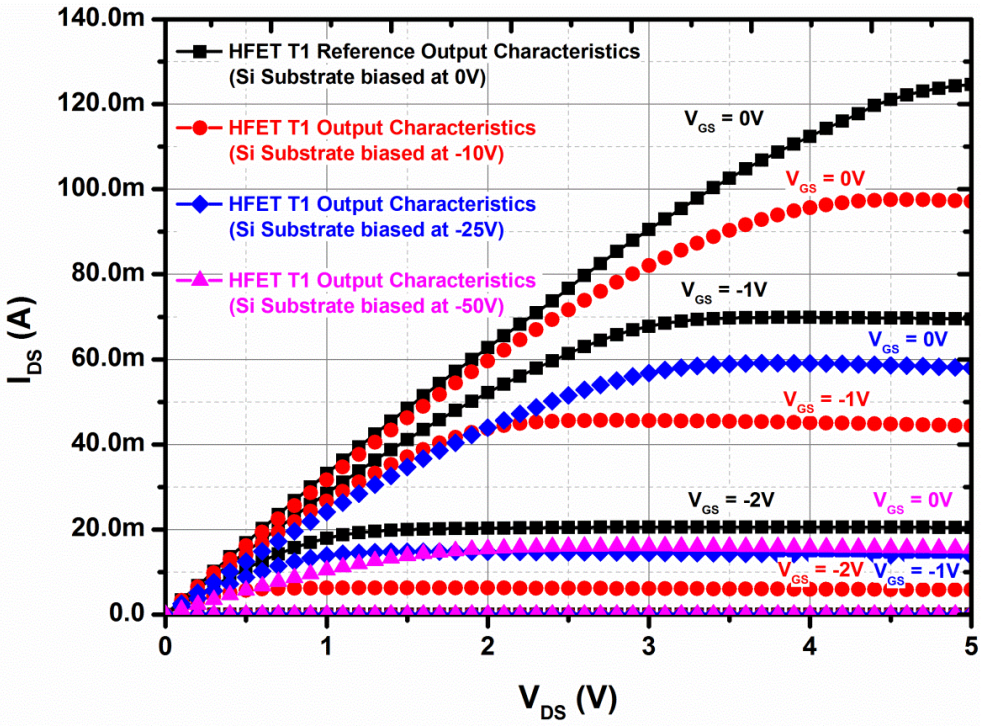


Figure 5.17 Impact on primary device - HFET T1 - Output characteristics

Negative bias applied on the substrate leads to an increase in V_{TH} and substantially compromises the output characteristics of HFET T1, as also observed when the drain of the neighbouring HFET T2 was negatively biased under floating substrate conditions.

Substantial lowering of the off-state leakage current is also observed and it was confirmed that the leakage path is directed from Drain to Source electrode of HFET T1. The magnitude of the substrate current under various conditions of perturbation also suggest that the lowering of the off-state leakage current in HFET T1 cannot be attributed to any change in the leakage path itself.

5.4.4 Grounded Si substrate and simultaneous electrical biasing of electrode of a neighbouring isolated device

The measurement configuration has been shown in Fig. 5.18.

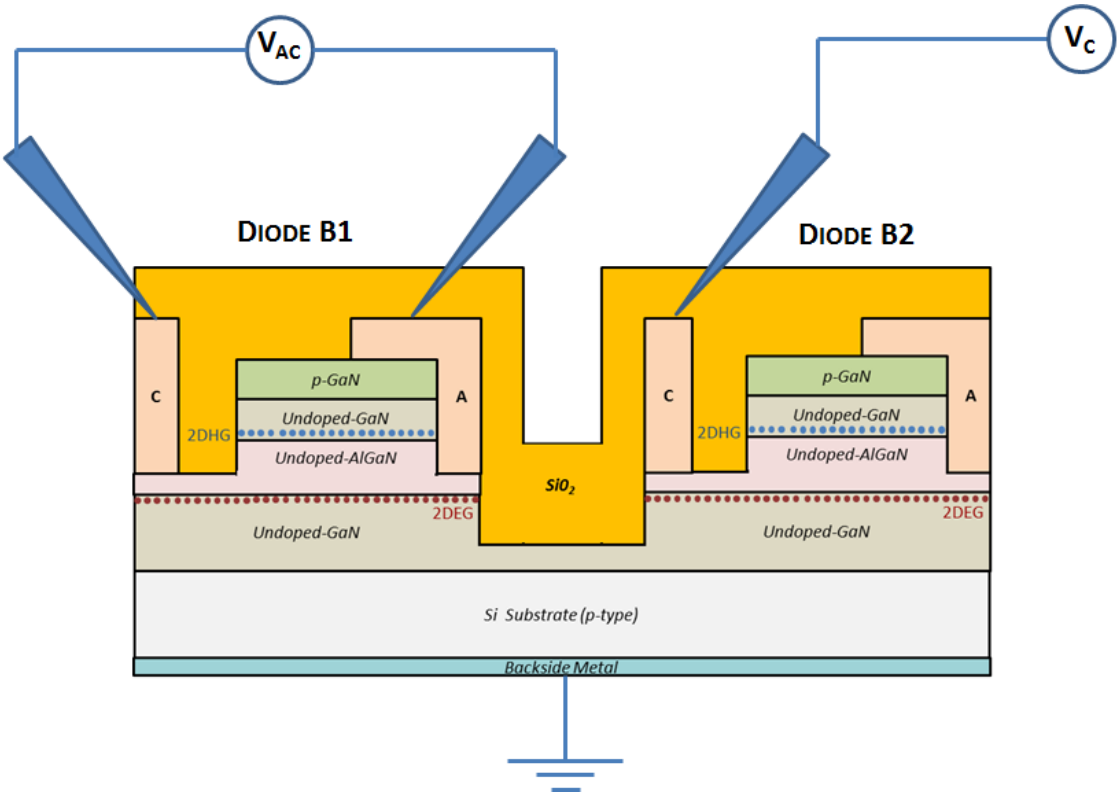


Figure 5.18 Measurement configuration to characterise the impact on the primary device electrical characteristics (Forward I-V) with grounded Si substrate and electrical biasing of electrode of a neighbouring isolated device

Forward I-V characteristics of the primary device (Diode B1) with Cathode of the neighbouring device Diode B2 biased at - 10 V, - 25 V and - 50 V respectively, have been shown in Fig. 5.19. Si substrate was biased at 0 V during these measurements. In the same figure, forward I-V characteristics under floating Si substrate and Cathode of Diode B2 biased at - 50 V have also been included just for reference. The measurement results indicate that the crosstalk effect appears to have been largely suppressed when the Si substrate is biased at 0 V, for the perturbation voltage range considered in this evaluation.

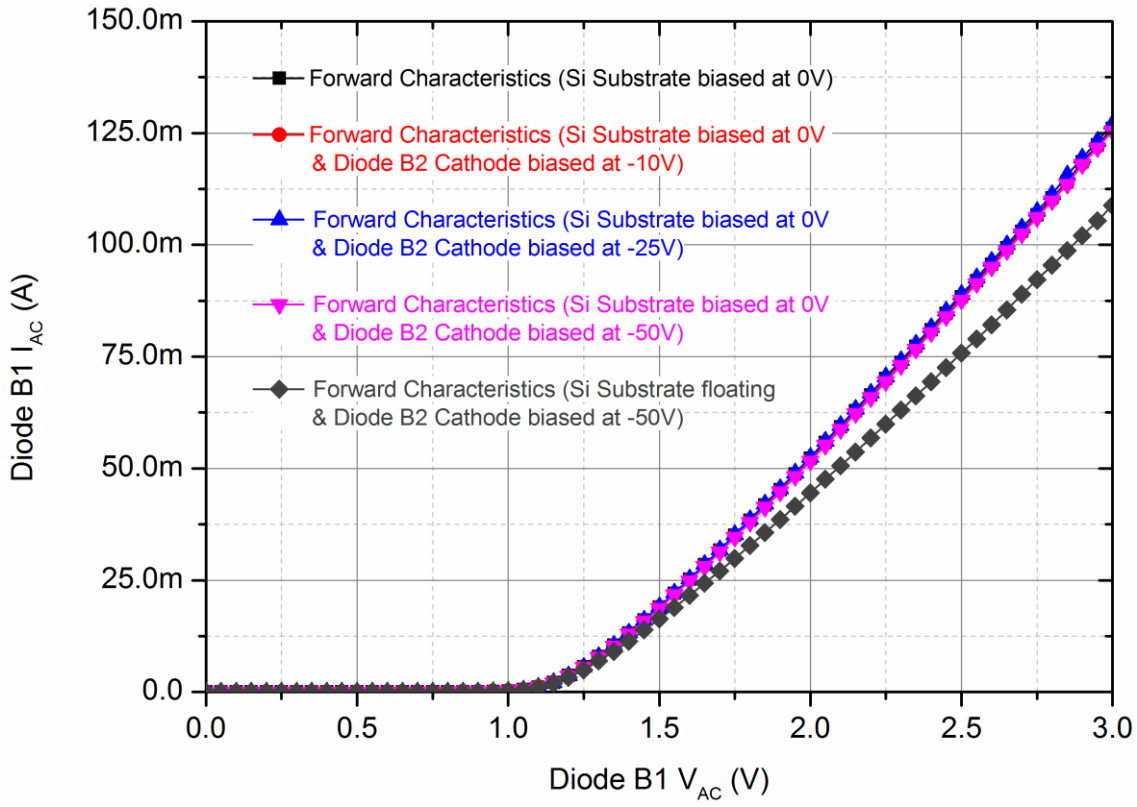


Figure 5.19 Impact on primary device - Diode B1 forward I–V characteristics

5.4.5 Magnitude of Crosstalk induced Surge in the Diode Specific On-State Resistance

The magnitude of crosstalk induced surge in the diode specific on-state resistance ($R_{ON}.A$) of the primary diode - Diode B1 has been quantified under the different conditions of perturbation and plotted in Fig. 5.20. There is a significant surge in the $R_{ON}.A$ of Diode B1 when a negative bias is applied either to the cathode of the neighbouring Diode B2 (floating substrate) or when applied only to the Si substrate. For a perturbation bias voltage of – 50 V, the $R_{ON}.A$ at V_{AC} = 2 V increases by 38% (floating substrate) and 46% (biased Si substrate) respectively under the two conditions.

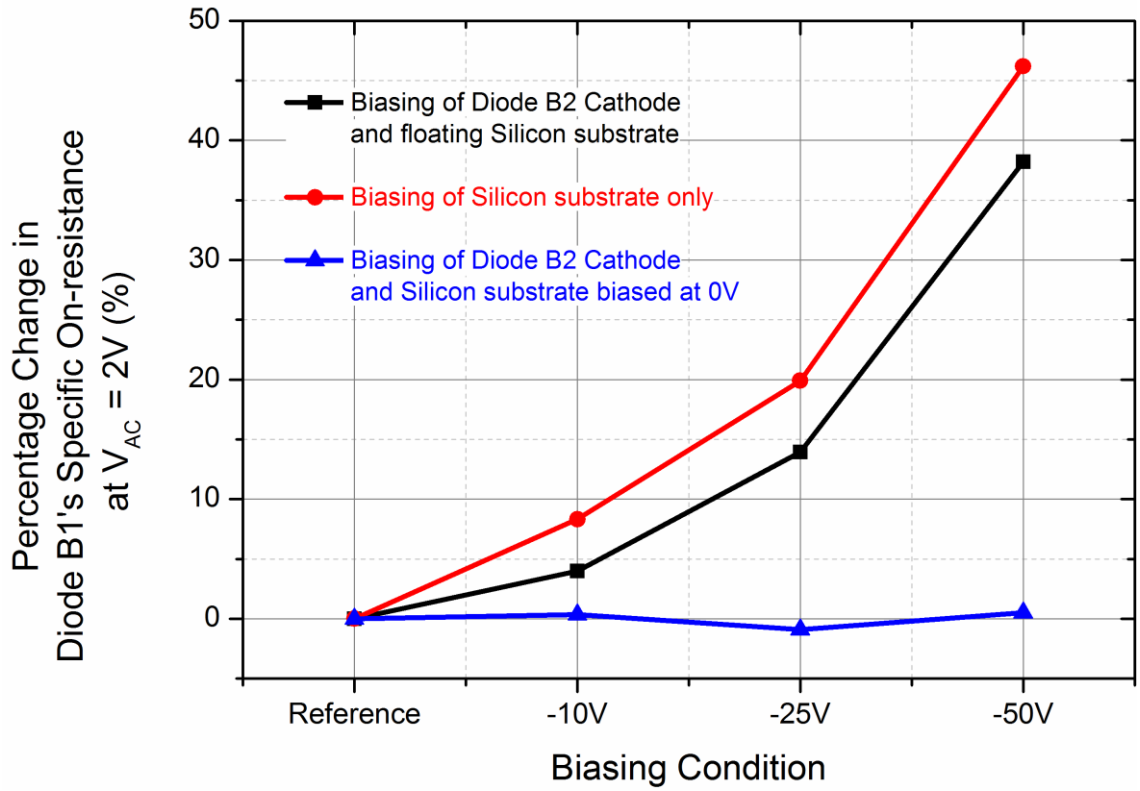


Figure 5.20 Percentage change of primary device specific on-state resistance under various perturbation conditions

5.4.6 Discussion and Implications

Results of the evaluation indicate that there is a strong similarity in the impact on the steady state characteristics of the primary device, when a negative bias is applied either on an electrode of a neighbouring device or to the Si substrate. To put it simply, the crosstalk effect appears to be equivalent to substrate bias effect. The influence of back biasing or substrate biasing with a negative impact on device conductivity, as observed and reported in this paper has been reported previously [11-13]. The influence on the device characteristics has been primarily attributed to reduction in 2DEG carrier density as the conducting substrate acts as a second gate and could change the potential distribution across the 2DEG at the AlGaN-GaN interface in the device structure. Ionisation/deionisation of both donor and acceptor traps responsible for the generation of GaN buffer space charges, can also contribute to additional modulation of the 2DEG channel [14]. Although the physical origins of the

buffer traps have not been well-understood, but intrinsic material defects (such as vacancies, interstitials), impurities introduced unintentionally during growth, as well as intentional dopants are the main suspects [15].

The isolation characteristics as shown in Fig. 5.7 and the magnitude of Si substrate current as shown in Figs. 5.14 and 5.15 indicate that the impact on the primary device under perturbation (reduced forward current or reduced reverse leakage characteristics in certain biasing range) cannot be attributed to any exchange of current path from the primary device to any other electrode.

However, the phenomenon could be explained such that when a negative bias is applied on the electrode of a neighbouring device, the applied potential is coupled through the highly resistive/insulating GaN and strain reducing interfacial layers to the Si substrate, essentially biasing the floating Si substrate or the buffer/Si interface to the same or near to the electric potential as that of the electrode at the surface and hence the observed equivalence in the behaviour, when the Si substrate is directly biased. When the Si substrate is biased at 0 V, the coupling appears to be ineffective in influencing the electric potential of the substrate or the buffer/Si interface, and subsequently the crosstalk effect gets mitigated or suppressed with essentially no impact on the primary device characteristics.

The relationship between 2DEG density and reverse leakage current in AlGaN/GaN Schottky barrier diodes has been reported in [16]. According to this report, the reverse leakage current appeared to decrease exponentially with the reduction of 2DEG density. Similar results have also been reported in [17]. The exact reason for this relationship has not been understood and needs to studied further. In the presence of crosstalk, or when the Si substrate is negatively biased, there is a negative impact on the 2DEG density as illustrated by the forward I-V characteristics. This reduction in 2DEG density could

explain the reduced reverse leakage current in the primary device (Diode) when under perturbation.

TCAD simulations using Silvaco ATLAS were performed to gain further insight on the impact of substrate biasing on HFET transfer characteristics. A conventional HFET was simulated for this study as the general behaviour is expected to be independent of device-architecture. The geometry of the buffer region and strain-relaxation layers, was defined based on the actual PSJ GaN-on-Si samples. The physical models that were included are the same as those used in studying the transfer characteristics of PSJ transistors, described in section 3.2. The doping in in the nitride layers was set as n-type with a doping concentration of $10^{15}/cm^3$. Silicon substrate doping was set as p-type with a doping concentration of $10^{15}/cm^3$ as expected in the actual physical samples. The simulated transfer characteristics have been shown in Fig. 5.21.

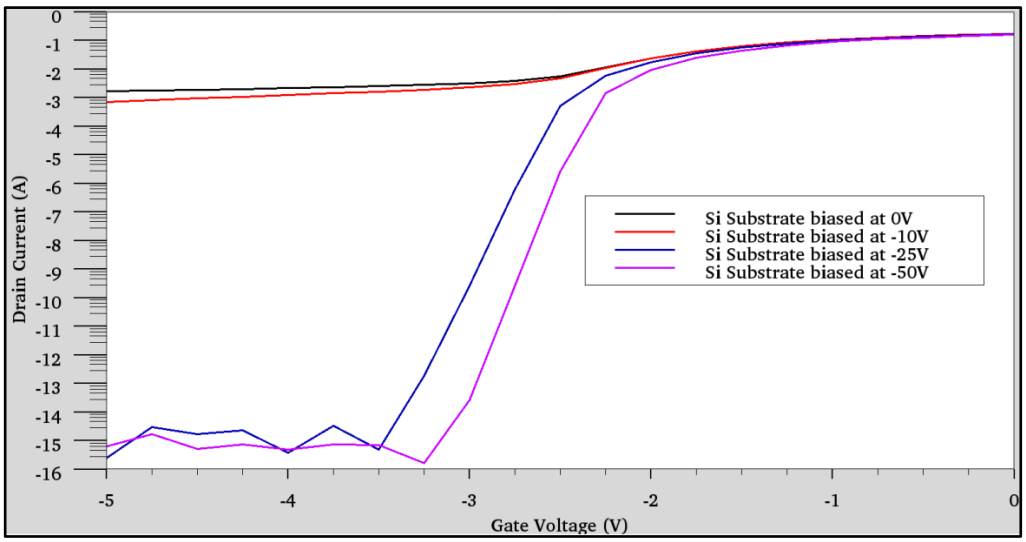


Figure 5.21 Simulated transfer characteristics at various values of substrate bias voltage

As observed experimentally, substantial lowering of the off-state leakage current is observed when a negative bias is applied to the substrate, also in simulation and it was confirmed that the leakage path was directed from Drain to Source terminals. It is observed in simulation that application of a negative voltage on the substrate creates a depletion region in the strain-relaxation layers

as well as GaN buffer regions. The depletion width depends on the magnitude of the applied bias and electron concentration within the device for various substrate biasing conditions as well as the predicted path for the off-state leakage current have been shown in Figs. 5.22 (a) -(d).

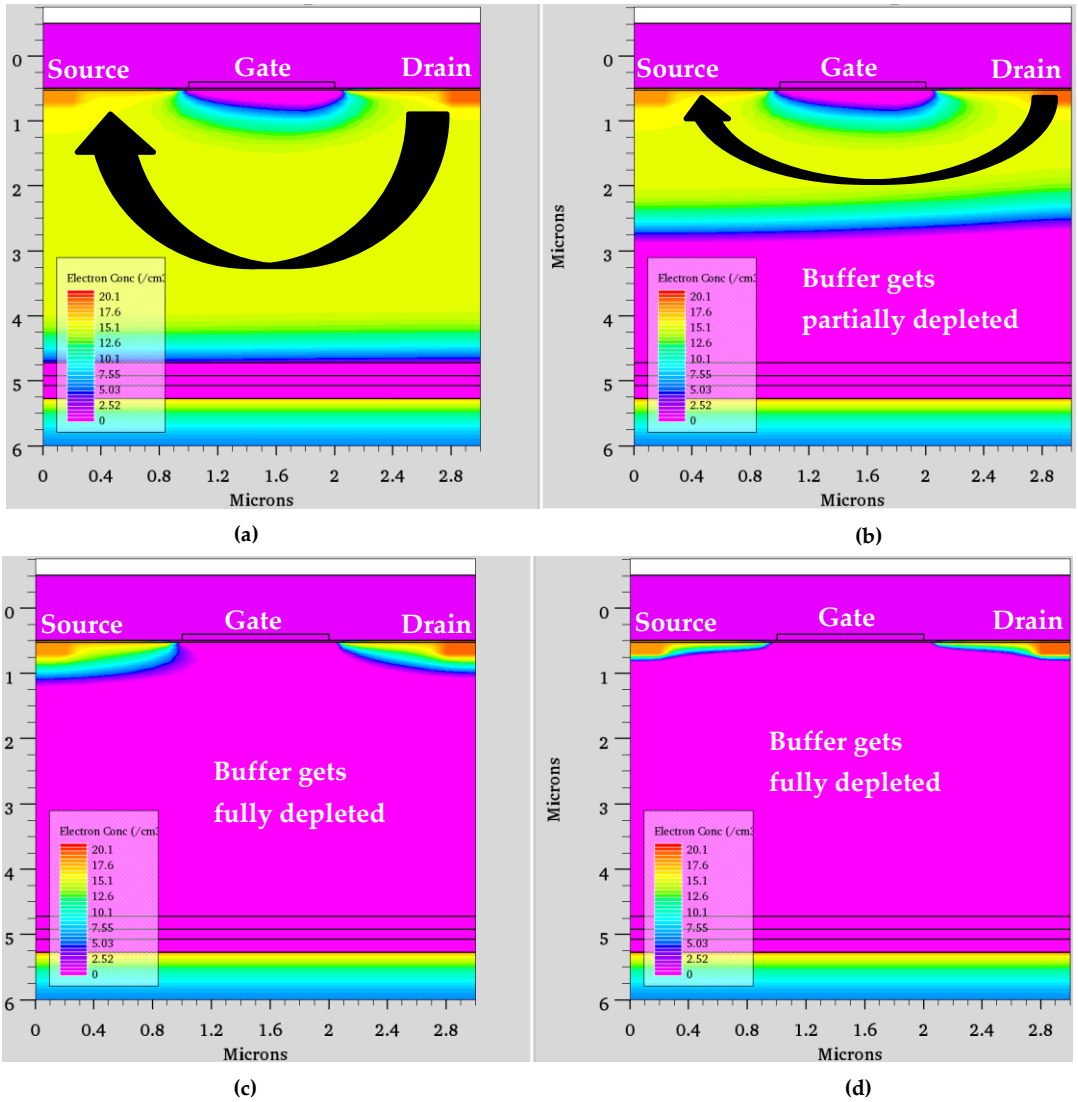


Figure 5.22 Electron concentration at V_{GS}=-4 V (off-state), V_{DS}=1 V, and Silicon substrate biased at (a) 0 V (b) - 10 V (c) - 25 V (d) -50 V

It needs to be highlighted that no crosstalk effects were observed in GaN-on-Sapphire or GaN-on-SiC (high resistivity substrate) devices. Based on our experimental results, the overall implication of the observed crosstalk phenomenon will be pertinent in monolithic circuits on the GaN-on-Si platform with negative biasing involved, which could translate to reduced electrical

efficiency of circuits due to high conduction losses and possibly loss of functionality in the worst case.

5.5 Increased static R_{ON} in GaN-on-Silicon power transistors under High-Side Switch Operation

5.5.1 High-Side Switch Operation

The half-bridge configuration as shown in Fig. 5.23 is one of the most common circuit topologies used in various power converter applications such as electronic ballasts and motor drives.

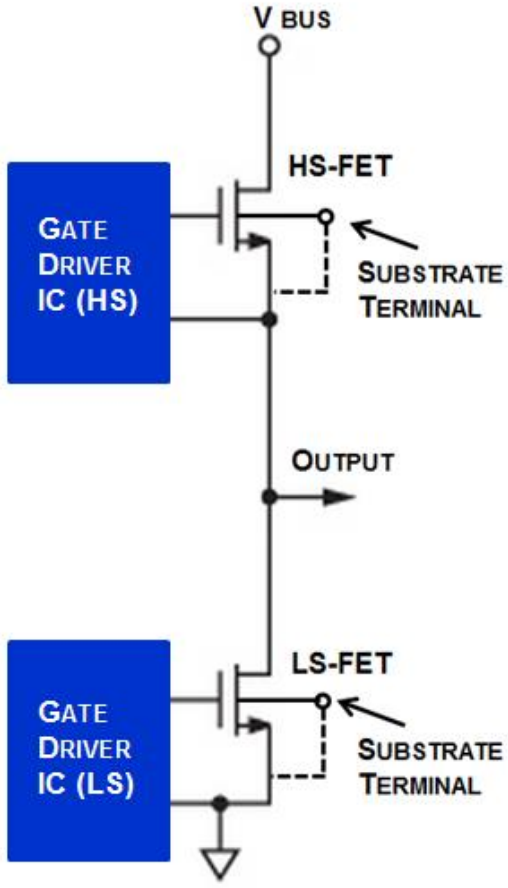


Figure 5.23 Schematic of a half-bridge circuit

The output of the half bridge is connected to the load. The High-Side (HS) switch/FET requires a dedicated gate driver IC that can respond to the floating source potential of the HS FET. The source potential of the Low Side (LS) FET is

connected to ground. If discrete vertical Power MOSFET is used as HS switch in this configuration, the Substrate/Body terminal of the FET is internally shorted to the Source terminal within the device using a common surface metallisation process. During the half-bridge operation and when the HS FET is fully-on, the source potential is very close the V_{BUS} value which can be at any value as per the application requirement. Compared to the LS FET, the HS FET operates in a positive bias shifted (PBS) condition as the drain and source potential will be maintained at high values during ON-state.

Performance of a HS FET is expected to be the same as that of a LS FET, if the effective Drain-Source, Gate-Source and Substrate-Source potential (0 V, internally shorted in a vertical Power MOSFET) are all maintained as the same. However, deterioration in the on-state characteristics have been reported previously for junction isolated LDMOS transistors in bulk Si as well as on SOI platforms when operated as HS switches [18-19].

The following sections will present the impact on the performance of GaN-on-Si transistors when employed for HS operation, as required in a typical half-bridge circuit, under various substrate biasing conditions.

The characterisation (DC and pulsed I-V) was performed on the same 650V PSJ GaN-on-Si HFETs, as used for the crosstalk evaluation. The results presented will be critical from the perspective of monolithic integration in GaN-on-Si technology platform.

5.5.2 DC characteristics of the transistor (biased substrate conditions)

Reference DC output characteristics were initially measured with grounded Source and Si substrate biased at 0 V. They have been shown in Fig. 5.24.

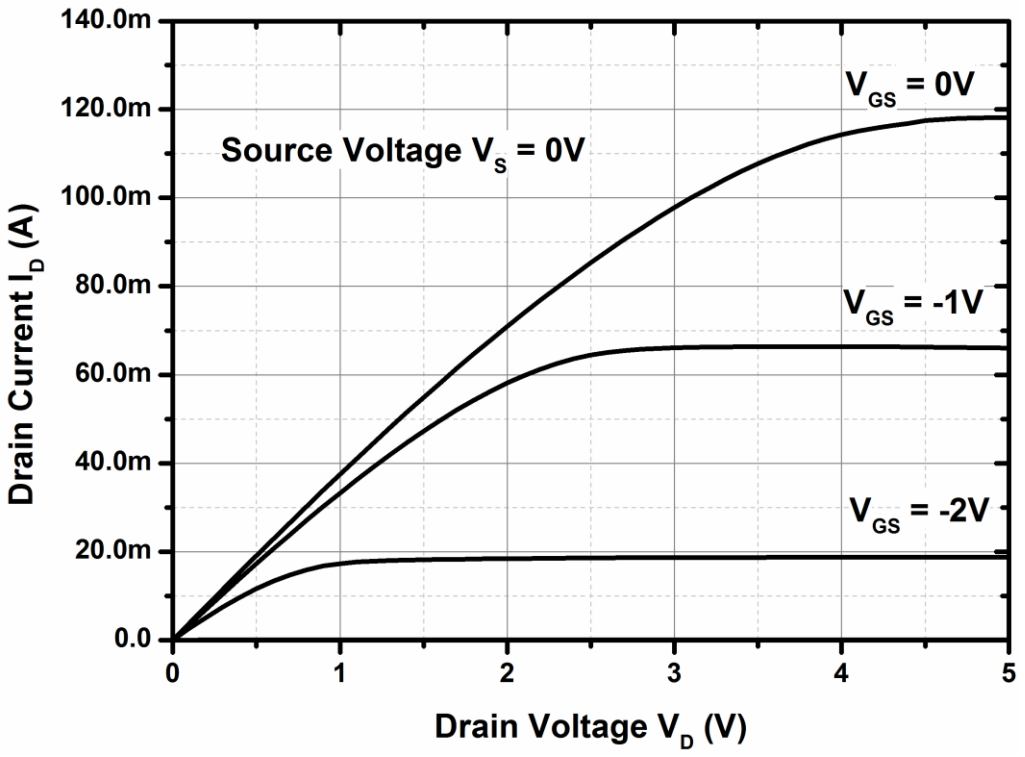


Figure 5.24 Reference DC output characteristics of the transistor with Source and Si substrate biased at 0V (V_{GS} Start=-5V, V_{GS} Stop=0V, V_{STEP}=1V)

Subsequently, output characteristics were measured under negative bias shifts (NBS) as well as positive bias shifts (PBS).

During a bias shift, electrical biasing on the Gate, Drain and Source terminals of the transistor, is shifted by a certain defined magnitude. The effective Gate-Source voltage (V_{GS}) and Drain-Source voltage (V_{DS}) is exactly the same as set during the reference, grounded Source measurement.

DC output characteristics measured with NBS and PBS under Si substrate biasing conditions, have been shown in Fig. 5.25 and Fig. 5.26 respectively.

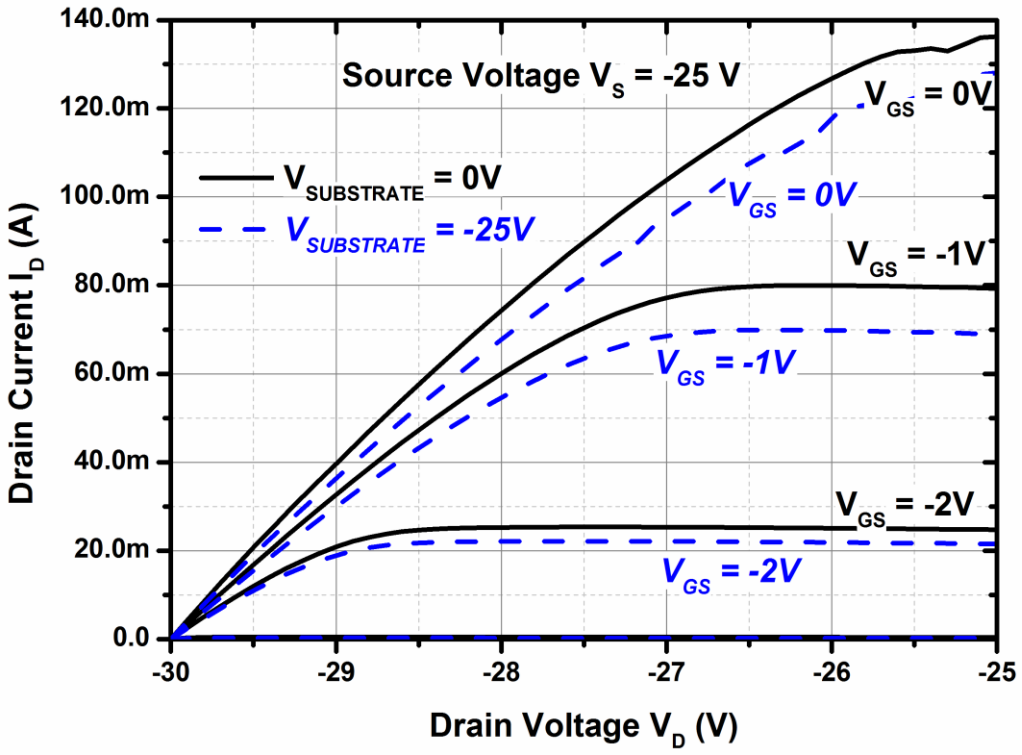


Figure 5.25 DC output characteristics of the transistor with a negative bias shift, under Si substrate biasing conditions of 0 V and – 25 V (tied to Source) respectively (V_{GS} Start=-5V, V_{GS} Stop=0V, V_{STEP}=1V)

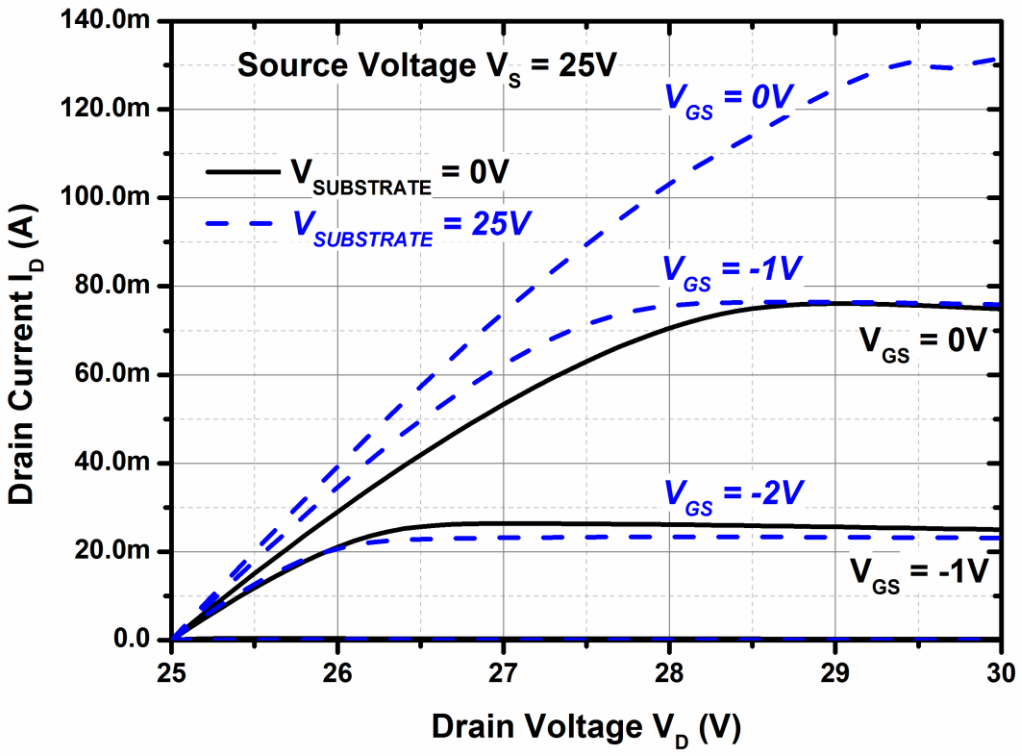


Figure 5.26 DC output characteristics of the transistor with positive bias shift, under Si substrate biasing conditions of 0 V and 25 V (tied to Source) respectively (V_{GS} Start=-5V, V_{GS} Stop=0V, V_{STEP}=1V)

With NBS, on-state resistance (R_{ON}) is comparable to the reference value when the source potential is tied to the substrate potential. With the substrate potential at 0 V, the R_{ON} is slightly lower than the reference value (essentially unaffected). However, with a PBS (as in a HS-switch), a substantial increase in R_{ON} is observed when the substrate is biased at 0 V. Unaffected DC output characteristics can be maintained during PBS if the substrate potential is tied to source potential, as also observed during NBS.

5.5.3 Drain pulsed I-V output characteristics of the transistor (biased substrate conditions)

Drain pulsed I-V output characteristics of the transistor – reference, with NBS and with PBS under substrate biasing conditions were also measured and have been shown in Figs. 5.27 – 5.31.

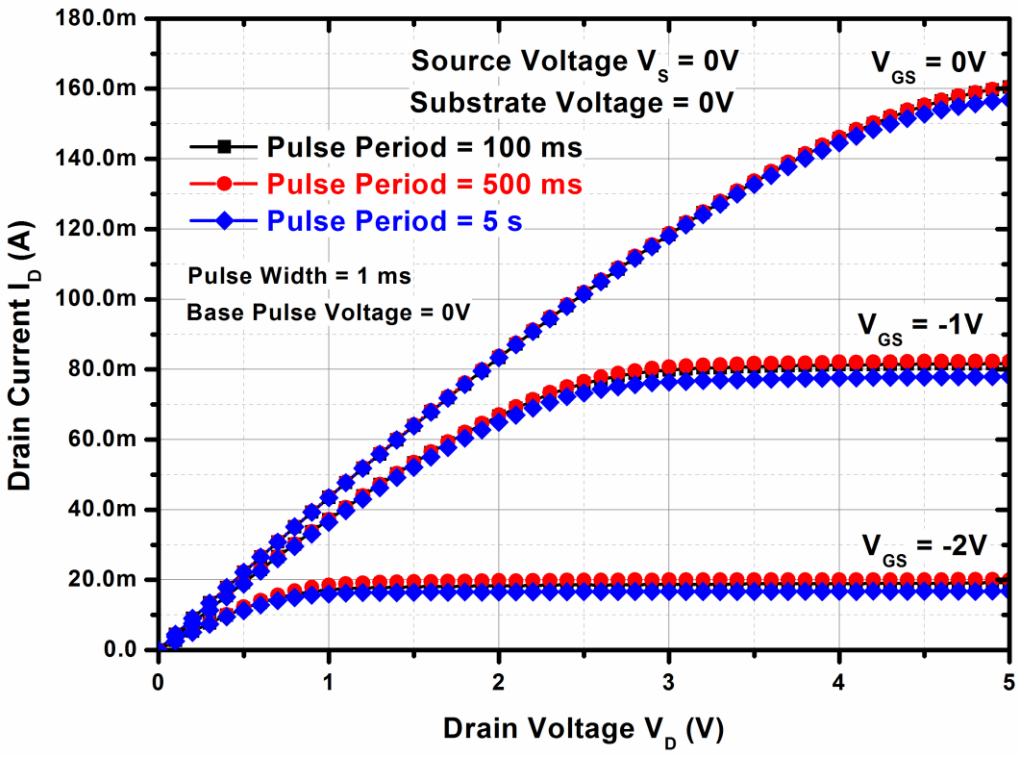


Figure 5.27 Reference Drain pulsed I-V output characteristics with Source and Si substrate biased at 0V (V_{GS} Start=-5V, V_{GS} Stop=0V, V_{STEP}=1V)

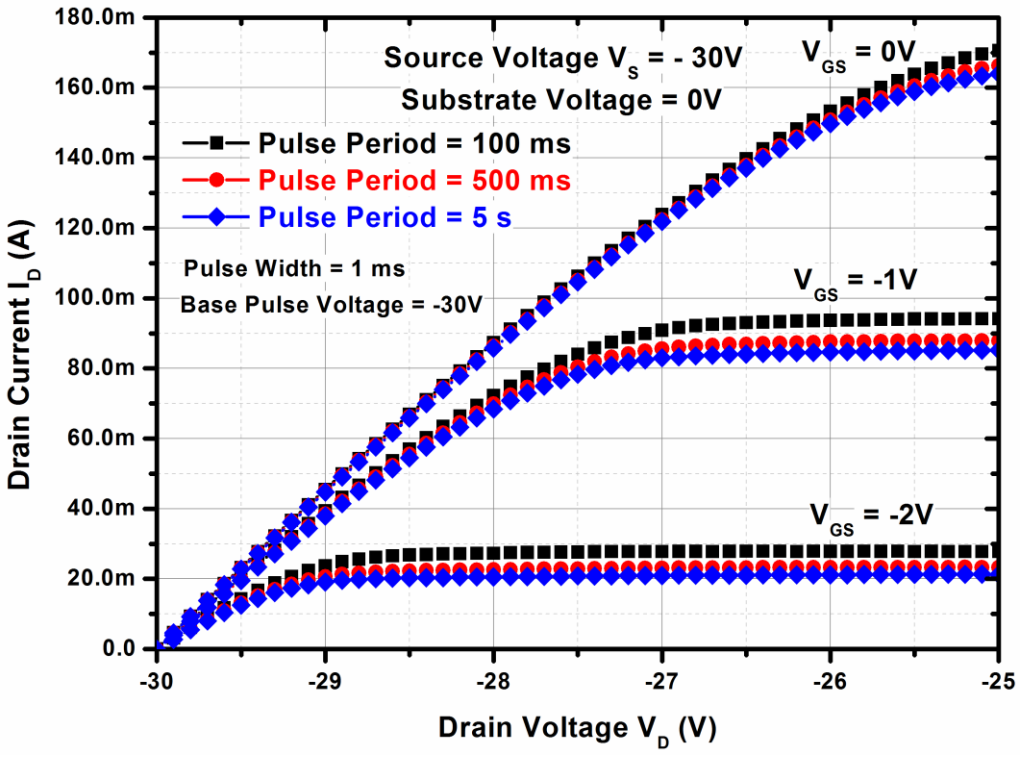


Figure 5.28 Drain pulsed I-V output characteristics under negative bias shift (V_{GS} Start=-5V, V_{GS} Stop=0V, V_{STEP}=1V, V_{SOURCE}= -30V, $V_{SUBSTRATE}$=0V,)

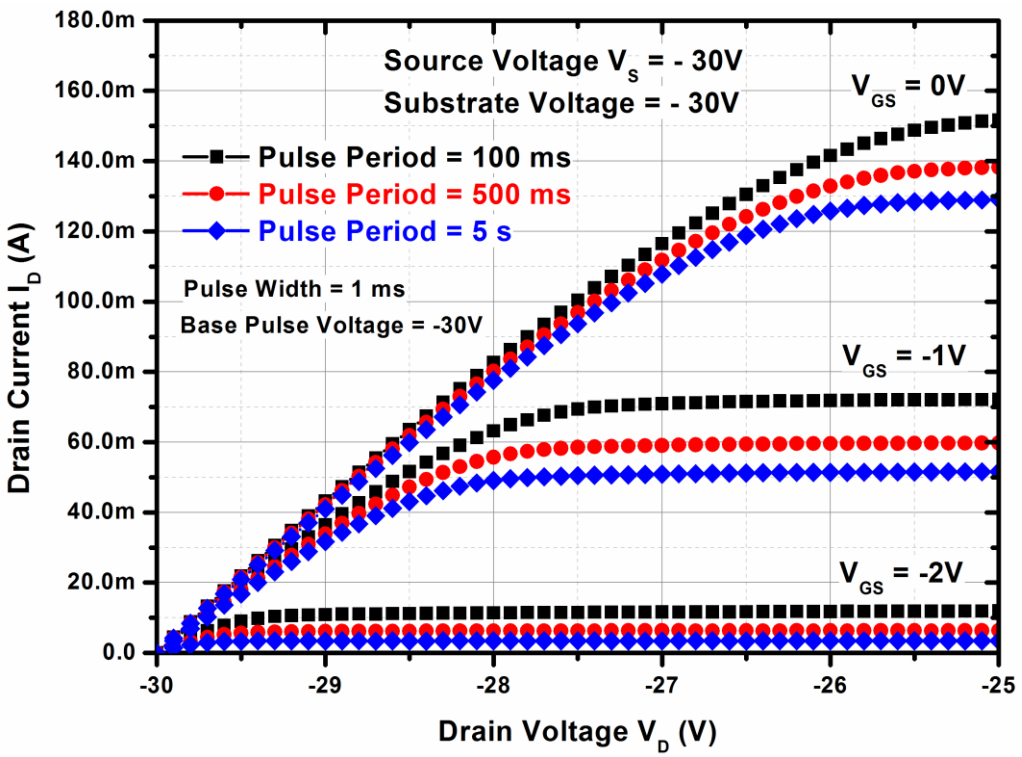


Figure 5.29 Drain pulsed I-V output characteristics under negative bias shift (V_{GS} Start=-5V, V_{GS} Stop=0V, V_{STEP}=1V, V_{SOURCE}= -30V, $V_{SUBSTRATE}$= - 30V (tied to Source))

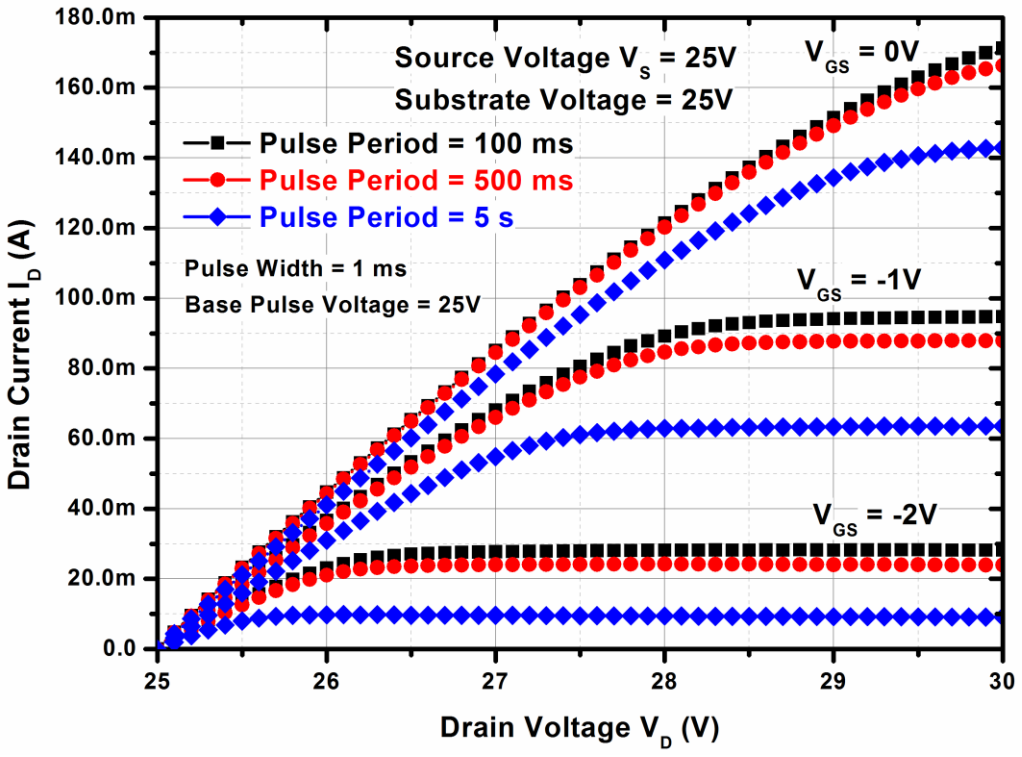


Figure 5.30 Drain pulsed I-V output characteristics under positive bias shift (V_{GS} Start=-5V, V_{GS} Stop=0V, V_{STEP}=1V, V_{SOURCE}=25V, $V_{SUBSTRATE}$=25V (tied to Source))

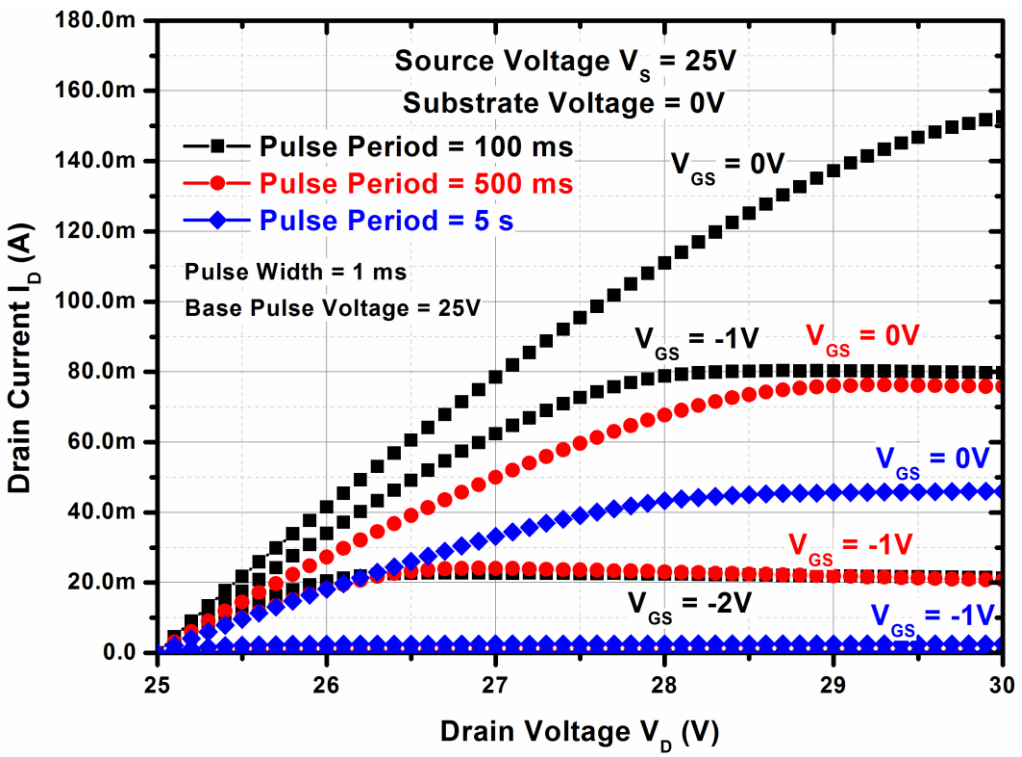


Figure 5.31 Drain pulsed I-V output characteristics under positive bias shift (V_{GS} Start=-5V, V_{GS} Stop=0V, V_{STEP}=1V, V_{SOURCE}=25V, $V_{SUBSTRATE}$=0V)

No substantial variation in characteristics could be observed under reference, with NBS or with PBS when Si substrate potential is tied to the source potential. However, I-V characteristics with PBS, and Si substrate biased at 0 V appeared to strongly depend on the pulse period, with significant increase in static R_{ON} as the pulse period increases.

5.5.4 Discussion and Implications

A deleterious phenomenon of increased static R_{ON} when the effective substrate to source potential is negative, has been identified and quantified for GaN-on-Si platform. The study indicates that grounding the substrate during a positive bias shift of the device leads to an increase in static R_{ON}. The situation is analogous to applying a negative bias to the substrate under standard grounded source conditions. Negative biasing of the p-type substrate creates a depletion region in the GaN buffer layer. As the magnitude of the negative bias increases, so does the depletion layer thickness and the electrons previously available for conduction are depleted from the channel region. Same mechanism appears to be in effect, when a positive bias shift is applied to the device under grounded substrate conditions. Ionisation/deionisation of both donor and acceptor traps could also be responsible for the generation of buffer space charges, and cause additional modulation of the 2DEG channel density [14]. Time dependency as indicated by the drain pulsed IV measurements, also suggests that electron trapping contributes to the observed behaviour. In Fig. 5.32, increase in $R_{ON}.A$ with PBS of 25 V is shown, indicating that R_{ON}.A increases by up to ~ 135% (biased substrate) for pulse period > 2s.

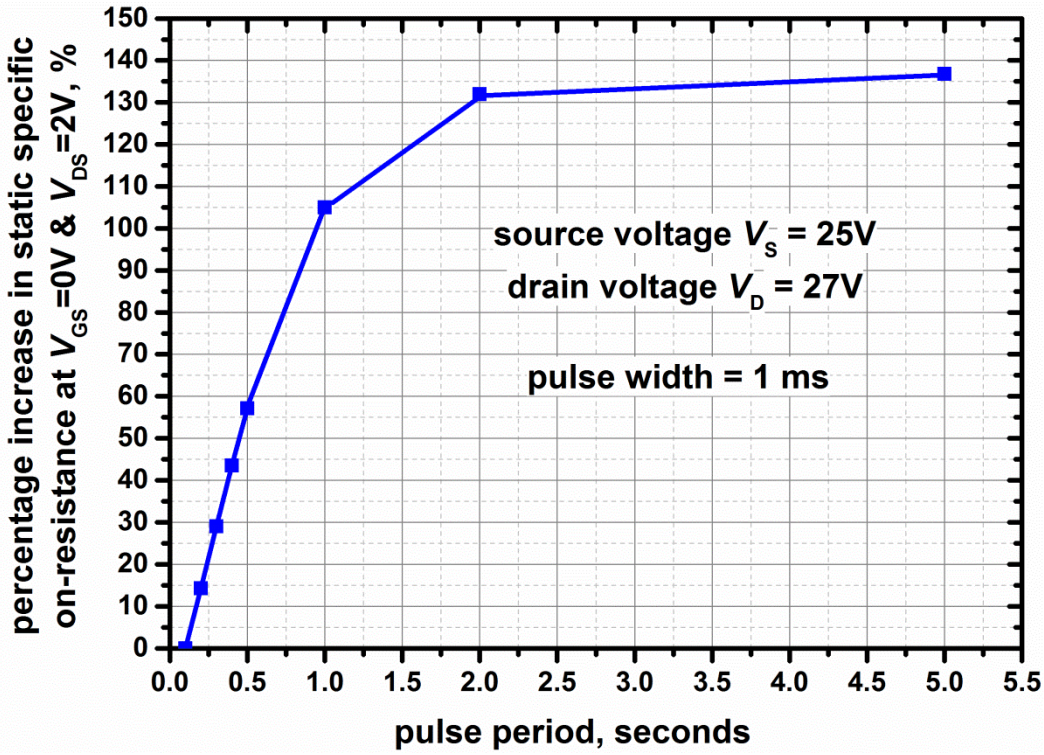


Figure 5.32 Percentage increase in the static specific on-resistance of the transistor under positive bias shift, with respect to pulse period

The saturation of the increase in $R_{ON}.A$ with pulse period suggests that a finite time (> 2 s) is required before all the available trap states are occupied by electrons.

It should be noted that the presented behaviour was not observed in GaN-on-Sapphire or GaN-on-SiC (high resistivity substrate) devices. Substrate potential is a critical parameter that can affect device characteristics, and needs to be carefully considered and evaluated to ensure reliable operation of GaN-on-Si transistors as High Side switches in power electronic circuit applications.

5.6 Summary

In this chapter, key electrical characterisation results of GaN Polarisation Super Junction (PSJ) Diodes on Silicon (Si) substrates were presented initially. Verification of the breakdown characteristics of PSJ Diodes confirmed the vertical breakdown in this platform. The evaluation also revealed a striking

similarity in the leakage characteristics under floating and grounded substrate conditions suggesting that even when the substrate is left floating, there is a leakage path via the substrate. It was also observed that the breakdown voltage (V_{BR}) values of PSJ Diodes in GaN-on-Si platform appear to saturate for PSJ length > 15 μm under floating as well as grounded substrate conditions.

The next section in the chapter presented the results of crosstalk evaluation in monolithic GaN-on-Si power devices through simple and systematically performed electrical measurements. The evaluation methodology consisted of verifying the impact on the steady state device electrical characteristics by inducing a perturbation bias on an electrode of an isolated device in the vicinity. It was observed that the behaviour is primarily responsive to a perturbation bias of negative polarity and translates to an increase in the on-state resistance of devices. The impact of biasing an electrode of a neighbouring isolated device under floating substrate conditions and the impact of only biasing the Si substrate appeared to be equivalent, indicating that the former behaviour may be due to the induced potential of the otherwise electrically unbiased/floating Si substrate or substrate/buffer interface. Grounding the substrate appears to substantially mitigate the impact of the crosstalk effects under static conditions.

The last section of the chapter discussed the issue of increase in static on-state resistance (R_{ON}), observed in GaN-on-Silicon HFETs, when the transistor is operated at a higher positive bias with respect to ground, in comparison to nominal grounded-source measurement conditions. This is unlike the widely-discussed and reported phenomenon of dynamic R_{ON} increase during current collapse, where an increase in R_{ON} is observed only after a high off-state drain bias is applied to the device. The findings are crucial from the point of view of their use in power electronic circuit applications either as discrete devices or in

monolithic integrated circuits. The impact manifests itself as increased threshold voltage in HFET and affects its output characteristics, an impact equivalent to and observed during Si substrate negative back-biasing. It has been observed that the specific on-state resistance of HFETs could substantially increase with a positive bias shift and pulsed I-V measurements indicate that the increase in magnitude also strongly correlates with pulse period during measurement, suggesting the presence of trapping.

Two major challenges to monolithic integration: crosstalk and compromised performance of GaN-on-Si HFET when operated as High Side switch were presented in this chapter. Crosstalk evaluation indicated that the impact could be suppressed under grounded substrate conditions (within the premise of the range of measurements performed during the evaluation). However, under grounded substrate conditions, there will be substantial impact on the transistor performance when operated as a High Side switch. The two aspects clearly indicate that novel techniques will need to be developed for realisation of monolithic power integrated circuits in GaN-on-Si technology platform.

5.7 References

[1] V. Unni, H. Kawai, and E. M. S. Narayanan, "Crosstalk in monolithic GaN-on-Silicon power electronic devices," *Microelectronics Reliability*, vol. 54, no. 9, pp. 2242-2247, 2014.

[2] V. Unni, H. Kawai, and E. M. S. Narayanan, "Increased static R_{ON} in GaN-on-silicon power transistors under high-side operation with floating substrate conditions," *Electronics Letters*, vol. 51, no. 1, pp. 108-110, 2014.

[3] P. N. Chyurlia, F. Semond, T. Lester, J. A. Bardwell, S. Rolfe, H. Tang, and N. G. Tarr, "Monolithic integration of AlGaN/GaN HFET with MOS

on silicon <111> substrates," *Electronics Letters*, vol. 46, no. 3, pp. 253–254, 2010.

[4] Y. Uemoto, T. Morita, A. Ikoshi, H. Umeda, H. Matsuo, J. Shimizu, et al., "GaN Monolithic Inverter IC Using Normally-off Gate Injection Transistors with Planar Isolation on Si Substrate," in *Proceedings of IEEE International Electron Devices Meeting*, Baltimore, Maryland, USA, Dec 7-9, 2009, pp.1-4.

[5] W. Chen, K. Y. Wong, and K. J. Chen, "Monolithic Integration of Lateral Field-Effect Rectifier with Normally-off HEMT for GaN-on-Si Switch-mode Power Supply Converters," in *Proceedings of IEEE International Electron Devices Meeting*, San Francisco, California, USA, Dec 15-17, 2008, pp. 1-4.

[6] K.J. Chen, "GaN smart power chip technology," in *Proceedings of IEEE International Conference of Electron Devices and Solid-State Circuits*, Xi'an, China, Dec 25-27, 2009, pp. 403-407.

[7] A. M. H. Kwan, Y. Guan, X. Liu, and K. J. Chen, "Integrated Over-Temperature Protection Circuit for GaN Smart Power ICs," *Japanese Journal of Applied Physics*, vol. 52, pp. 08JN15-08JN15-4, 2013.

[8] D. W. Green, S. Hardikar, M. Sweet, K. V. Vershinin and E. M. Sankara Narayanan, "Interaction between monolithically integrated JI-LIGBTs under Clamped Inductive Switching," in *Proceedings of International Symposium on Power Semiconductor Devices & ICs*, Santa Barbara, California, USA, May 23-26, 2005, pp. 119-122.

[9] P. Srivastava, J. Das, D. Visalli, M. V. Hove, P. E. Malinowski, D. Marcon, S. Lenci, et al.,"Record Breakdown Voltage (2200 V) of GaN DHFETs on

Si With 2-Buffer Thickness by Local Substrate Removal," *IEEE Electron Device Letters*, vol. 32, no. 1, pp. 30-32, 2011.

[10] D. Visalli, M. V. Hove, P. Srivastava, J. Derluyn, J. Das, M. Leys, S. Degroote, K. Cheng, M. Germain, and G. Borghs, "Experimental and simulation study of breakdown voltage enhancement of AlGaN/GaN heterostructures by Si substrate removal," *Applied Physics Letters*, vol. 97, no. 11, pp. 113501-1 - 113501-3, 2010.

[11] R. Gaska, M. S. Shur, J. W. Yang, A. Osinsky, A. O. Orlov, and G. L. Snider, "Substrate bias effects in AlGaN-GaN doped channel HFETs grown on doped SiC substrates," *Materials Science Forum*, vol. 264-268, pp. 1445-1448, 1998.

[12] M. J. Uren, D. Herbert, T. Martin, B. T. Hughes, J. Birbeck, R. Balmer, A. J. Pidduck, and S. K. Jones, "Back bias effects in AlGaN-GaN HFETs," Physica Status Solidi, vol. 188, pp. 195-198, 2001.

[13] R. Chu, D. Zehnder, B. Hughes, and K. Boutros, "High Performance GaN-on-Si Power Switch: Role of Substrate Bias in Device Characteristics," *Device Research Conference*, Santa Barbara, California, USA, Jun 20-22, pp. 223 - 224, 2011.

[14] S. Yang, C. Zhou, Q. Jiang, J. Lu, B. Huang, and K. J. Chen, "Investigation of buffer traps in AlGaN/GaN-on-Si devices by thermally stimulated current spectroscopy and back-gating measurement," *Applied Physics Letters*, vol. 104, pp. 013504-1 - 013504-4, 2014.

[15] M. Meneghini, I. Rossetto, D. Bisi, A. Stocco, A. Chini, A. Pantellini, C. Lanzieri, A. Nanni, G. Meneghesso, and E. Zanoni, "Buffer traps in Fe-doped AlGaN/GaN HEMTs: Investigation of the physical properties

based on pulsed and transient measurements," *IEEE Transactions on Electron Devices*, vol. 61, no. 12, pp. 4070–4077, Dec. 2014.

[16] A. Terano, T. Tsuchiya and K. Mochizuki, "Investigation of relationship between 2DEG density and reverse leakage current in AlGaN/GaN Schottky barrier diodes," *Electronics Letters*, vol. 48, no. 5, pp. 274–275, 2012.

[17] S. Sudharsanan, and S. Karmalkar, "Modeling of the reverse gate leakage in AlGaN/GaN high electron mobility transistors," *Journal of Applied Physics*, vol. 107, pp. 064501-1 - 064501-3, 2010.

[18] E. Arnold, S. Merchant, M. Amato, S. Mukherjee, and H. Pein, "Comparison of Junction-Isolated and SOI high-voltage devices operating in the source-follower mode," in *Proceedings of International Symposium on Power Semiconductor Devices & ICs*, Tokyo, Japan, 1992, pp. 242-243.

[19] E. Arnold, "Silicon-on-Insulator Devices for High Voltage and Power IC Applications," *Journal of Electrochemical Society*, vol. 141, no. 7, pp. 1983-1988, 1994.

Chapter 6 Concluding Remarks and Future Work

6.1 Concluding Remarks

The thesis has been structured in a manner that covered the fundamentals of GaN HEMT technology for power switching applications to establish the context before moving on to description of the PSJ technology and main research challenges that were undertaken.

The introductory chapter provides a brief overview of the key driving factors towards "more electric/electronic" nature of systems and emergence of GaN as a strong contender for current and next-generation power electronic applications.

In the second chapter, intrinsic material properties such as spontaneous and piezoelectric polarisation and their origins associated with non-ideality and strain in the crystal structure in GaN were introduced and discussed in detail. Details of HEMT operation were presented following which the most important electrical characteristics and their governing physical parameters were also discussed. Concepts such as RESURF/Superjunction in Silicon as well as Field Plate engineering which is the most widely adopted technique for developing high voltage devices in GaN, were briefly reviewed.

In the third chapter, the concept of Polarisation Super Junction (PSJ) was introduced and the technique of charge compensation achieved by engineering the polarisation charges inherent in the material system was described. Numerical simulation results were presented comparing two designs, one based on Field Plate engineering and the other based on PSJ with the objective of gaining insight into the physical mechanisms in the device that determined the electrical characteristics. Following that, the approach to device design and scalability to large area devices, process development/optimisation, mask

design, processing challenges, and elaborate results of device fabrication were presented and discussed in detail.

In the fourth chapter, the performance and electrical characterisation results of test structures as well as various large area Polarisation Super Junction (PSJ) devices were presented. The discussion commenced with the evaluation of high voltage PSJ GaN Schottky Barrier Diodes (SBD) on semi-insulating 6H-SiC substrates. Detailed electrical characterisation through measurement of forward I-V characteristics, reverse I-V characteristics and Capacitance Voltage (CV) measurements provided insight on the functionality and performance of the devices. Breakdown Voltage (V_{BR}) values of the devices scaled up linearly with PSJ drift length with an average critical electric field strength of ~ 0.8 MV/cm. Fabricated PSJ Diodes with drift length of 25 μm showed low on-set voltage of ~ 0.4 V, high V_{BR} of ~ 2400V, specific on-state resistance ($R_{ON}.A$) of ~ 14 mΩ.cm^2 and a Power Device Figure of Merit ($PDFOM = V_{BR}^2 / R_{ON}.A$) of ~ 400 MW/cm^2 comparable to some of the best reported values for field plated devices. Subsequently, key electrical characterisation results of large area PSJ Diodes, HFETs and PN Diodes fabricated on various SiC and Sapphire substrates, were presented. A detailed assessment of the dominant factors determining the scalability performance was provided with the aid of detailed characterisation of devices and process test structures as well as ANSYS electrical simulations. These results are critical to take the technology/product development to the next stage. Following that, a detailed discussion on the static and dynamic characterisation of the Intrinsic Diode and Dynamic Clamping Capability of PSJ HFETs was presented. The chapter was concluded with the pilot results of standard wire-bonded and flip-chip packaged PSJ large area devices.

In the fifth chapter, key electrical characterisation results of GaN PSJ Diodes on Silicon (Si) substrates were presented initially. Verification of the breakdown characteristics of PSJ Diodes confirmed the vertical breakdown in this platform.

The chapter also presented the results of crosstalk evaluation in monolithic GaN-on-Si power devices through a set of simple and systematically performed electrical measurements. The impact on the electrical characteristics of a device, with simultaneous biasing of an electrode of a neighbouring isolated device under floating substrate conditions, and only biasing the Si substrate appeared to be equivalent. This suggested that the former behaviour may be due to the induced potential of the otherwise electrically unbiased/floating Si substrate or the Si/buffer interface. It was also observed that grounding the substrate appears to substantially alleviate the impact of the crosstalk effects under static conditions. The last section of the chapter discussed the issue of increase in static on-state resistance (R_{ON}), observed in GaN-on-Si HFETs when operated as High-Side switches. The findings are crucial from the point of view of their use in monolithic power integrated circuits. It has been observed that the specific on-state resistance of HFETs could increase by > 135% with a positive bias shift of 25 V (pulse period of 2 secs) and pulsed I-V measurements indicated that the increase in magnitude also strongly correlated with pulse period during measurement, suggesting the influence of trapping.

Crosstalk evaluation indicated that the impact could be suppressed under grounded substrate conditions. However, under grounded substrate conditions, transistor performance deteriorates when operated as a High-Side switch. The findings clearly indicate that novel techniques will need to be developed for realisation of reliable monolithic power integrated circuits in GaN-on-Si technology platform.

6.2 Future Work

The research presented in this thesis could be the basis for critical design/process optimisation activities required for PSJ technology development as well as further investigation of challenges to monolithic integration in the

future. The most important areas of future work are summarised in the following section.

1. **Design optimisation**:

   As described in chapter 4, the magnitude of Schottky leakage current in devices processed in Sheffield using Inductively Coupled Plasma (ICP) etching were substantially lower than the devices processed at Southampton using Ion Beam Etching (IBE). Clearly, substantial effort will be required to optimise the IBE process. Another approach which will aid reduction of Schottky leakage will be maintaining a GaN cap layer under the Gate/Anode electrode and using low-stress surface dielectric layer such as Benzo-Cyclo-Butene (BCB).

   The numerical simulation results presented in Chapter 2 have suggested that there is a tendency of Drain side edge of the PSJ layer to experience electric field crowding at high voltage. Inclusion of a Drain Field Plate and further optimisation may be required for enhanced lateral electric field management in the PSJ structure.

   In Chapter 4, the intrinsic diode and dynamic clamping capability of PSJ transistors were described. The basic structure can be minimally modified to incorporate an intrinsic PSJ Schottky Barrier Diode instead of PN Diode to further improve the performance.

2. **Process optimisation**:

   Along with the optimisation of the etching process of GaN layers as mentioned in the point above, there is substantial scope for improvement in the processes determining the contact resistance. This will require extensive trials of the contact stack optimisation, Rapid Thermal Annealing (RTA) process for p-contact as well as n-contact at various RTA temperatures and annealing time in order to match the best reported values in literature.

Au electroplating evaluation can also be performed for realising the second-metal required in the large area devices as that can be a more cost effective approach than thermal/e-beam evaporation/Lift-off. This will accordingly require further optimisation of the geometry of the contact electrodes as well as vias.

3. **Avalanche Capability**:

   Today's lateral GaN power device technologies do not show avalanche capability and the devices are irreversibly damaged if driven into breakdown, unlike their silicon counterparts. The static characterisation of large area PN Diodes as described in Chapter 4 indicated that the breakdown behaviour is destructive. However, it was also observed that the p-type contact was quasi-ohmic and Schottky in certain cases creating an uncertainty on the avalanche capability of this technology. As the p-contact is improved, this evaluation should be revisited to evaluate avalanche capability in PSJ technology.

4. **PSJ GaN converters**:

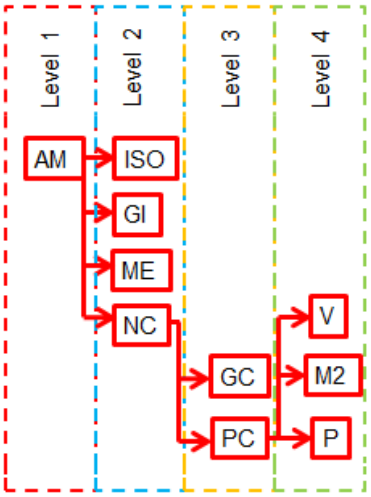
   The next level in the natural course of technology development/demonstration will be implementation of the fabricated PSJ GaN devices in an actual power converter application. Particular attention will have to be made regarding circuit stray/parasitic inductance while employing discrete GaN components in a circuit due to the extremely fast switching nature of these devices. Monolithically integrated power converters can provide the compactness, minimise the parasitic impact and enable harnessing the advantage of a GaN based system. The experience gained from the large area device development can be substantially leveraged for the development of GaN power integrated circuits.

5. As monolithic integration gains more traction as the approach to build high performance GaN based power electronic systems on Si substrates (due to performance/cost advantage), **deeper understanding** of the two challenges to integration which were comprehensively examined in Chapter 5 of the thesis **(crosstalk** and **increased R_{ON}** in GaN-on-Si HFETs under High Side operation) along with potential solutions will become necessary. Detailed characterisation of defects and trap states as well as interfacial charges in the material system and using this information to model the behaviour using numerical simulations will enable deeper understanding of the physical mechanisms at play. Verification of the behaviour in actual monolithic integrated circuits will also be necessary to quantify the true implications of the discussed anomalies and effectiveness of the solutions under various operating conditions (for e.g. voltage range, switching frequency).

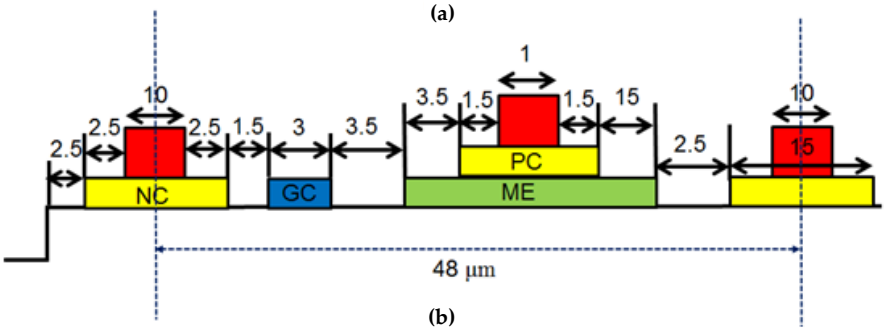
Appendix-1

Mask Design

A multi-level mask alignment sequence as shown in Fig. A1.1 (a) was used for mask design as it aids minimising misalignment between critical layers.



(a)



(b)

Mask Layer	Alias	Aligned to
AM	Alignment Mark	-
ISO	Isolation Etch	AM
GI	Gate Isolation/Pad Insulation	AM
ME	Mesa Etch	AM
NC	N Contact	AM
PC	P Contact (Base)	NC
GC	Gate Contact	NC
V	Via etch	PC
M2	Second Metal	PC
P	Pad etch	PC

(c)

Figure A1.1 (a) Alignment Sequence (b) Minimum dimensions of a basic cell (c) Description of mask layers

Minimum dimensions for the basic cell were determined based on that (the minimum gate length was chosen as 3 μm) and are shown in Fig. A1.1 (b). AM, NC and PC serve as alignment layers for layers in Levels 2, 3 and 4 respectively. For a layer aligned to an alignment layer in a prior level, the misalignment can be maintained within ± 1 μm (for e.g. from AM to ISO or from NC to GC). Within the same level, the misalignment from layer to layer can be ± 2.0 μm (for e.g. between ISO and ME or between M2 and V). Misalignment for a layer to a non-alignment layer in the prior level can be ± 3.0 μm (for e.g. between GC (level 3) and ME (level 2). The software used for mask design is Mentor Graphics® IC station®, which is a layout editing software toolset. Compared to the process-flow developed for Proof of Concept devices, there were additional layers such as gate contact (previously gate was defined with p-contact), via and second metal (Metal 2) in the new process flow. Therefore, the process file to be used during mask design was also accordingly appended. The overall Graphic Database System (GDS) layers (0-10) defined are as shown in in Fig. A1.2.

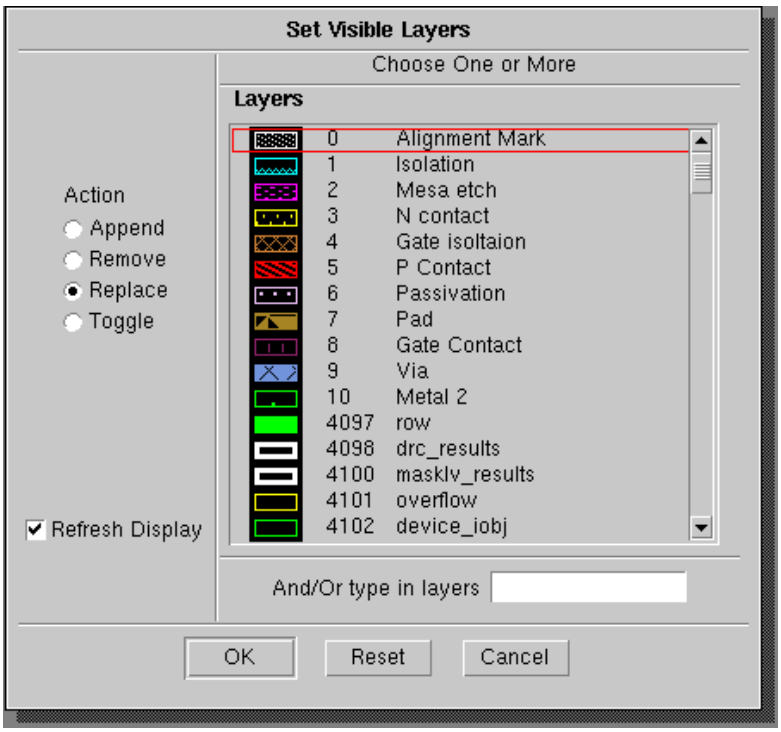
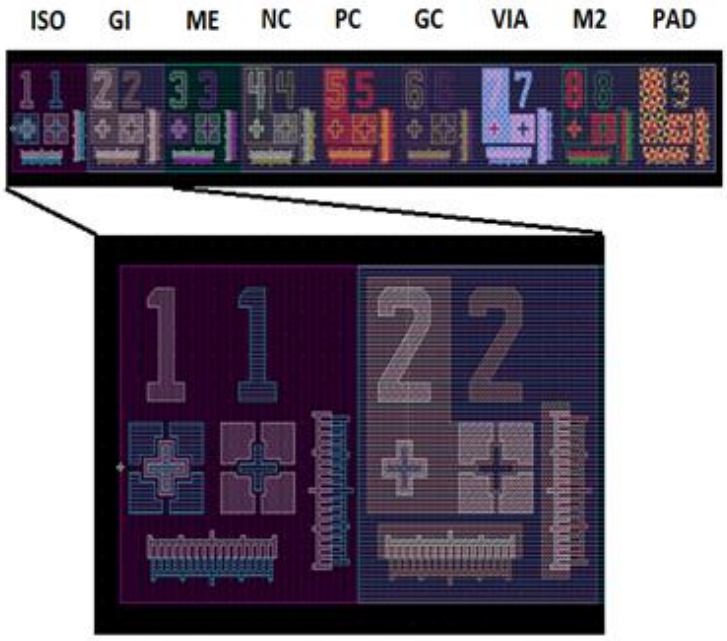


Figure A1.2 GDS Layers for mask design

The mask layout for alignment of layers is shown in Fig. A1.3.



Layer	Alias	Aligned to	Mask Tone
AM	Alignment Mark	NA	Dark Field
ISO	Isolation	AM	Light Field
GI	Gate Isolation (Pad Insulation)	AM	Dark Field
ME	Mesa Etch	AM	Light Field
NC	N contact	AM	Dark Field
PC	P contact	NC	Dark Field
GC	Gate Contact	NC	Dark Field
V	Via	PC	Dark Field
M2	Metal 2	PC	Dark Field
Pad	Pad	PC	Dark Field

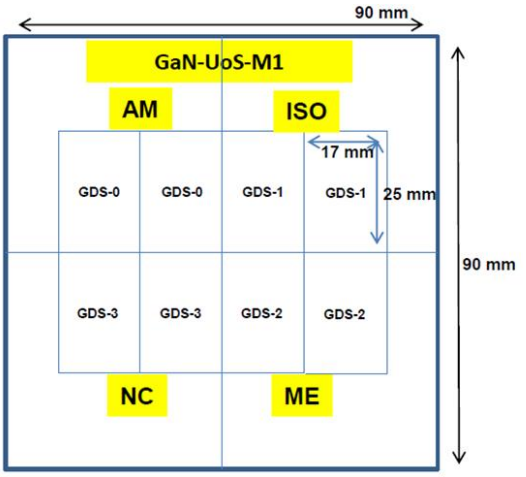
Figure A1.3 Mask Alignment

The vertical and lateral Vernier scales enable estimation and control of misalignment along both directions during photolithography. Also shown in the figure is the description of the layers and tone/polarity of the individual masks referred to as Light Field (Bright/Clear Field) and Dark Field. Light Field masks are mostly clear and drawn features are opaque, whereas Dark Field masks are mostly opaque and drawn features are clear/ transparent. The plan was to use only positive photoresists during device fabrication at Sheffield and masks were designed and tone/polarity of the individual masks was defined accordingly.

Photomasks

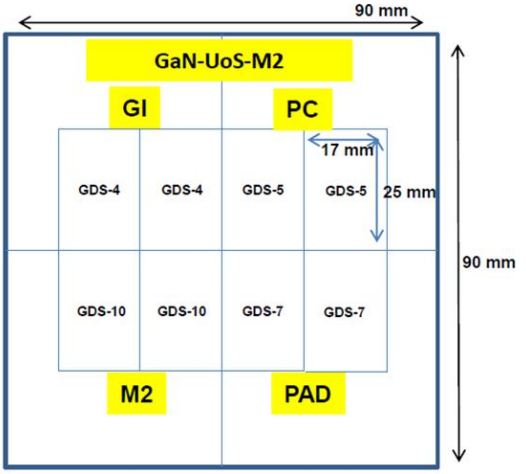
The photomasks were fabricated by Compugraphics. For 3" wafer level processing, photomasks were fabricated for each GDS layer. However, the strategy employed at Sheffield was to have multiple reticles on a single photomask, thereby minimising the number of photomasks to be fabricated. The cost of mask fabrication doesn't depend on the variation of reticles but on

individual photomask fabrication and minimum feature size. For processing at Sheffield, all the GDS layers with repetitions could be accommodated within three photomasks (M1, M2 and M3) as shown in Fig. A1.4.



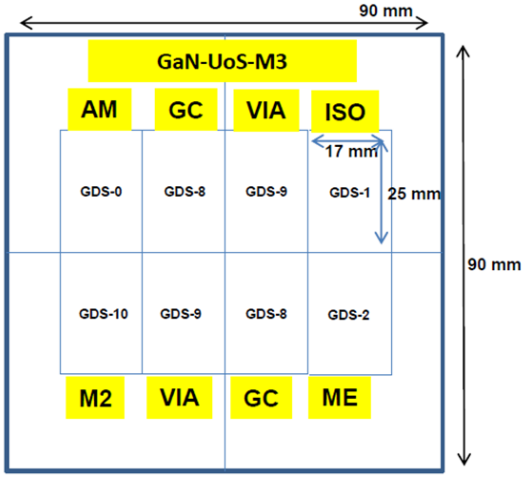
Layer	Alias	GDS number	Mask Tone
AM	Alignment Mark	0	Dark Field
ISO	Isolation	1	Light Field
ME	Mesa Etch	2	Light Field
NC	N Contact	3	Dark Field

(a)



Layer	Alias	GDS number	Mask Tone
GI	Gate Isolation	4	Dark Field
PC	P Contact	5	Dark Field
Pad	Pad	7	Dark Field
M2	Metal 2	10	Dark Field

(b)



Layer	Alias	GDS number	Mask Tone
AM	Alignment Mark	0	Dark Field
ISO	Isolation	1	Light Field
ME	Mesa Etch	2	Light Field
GC	Gate Contact	8	Dark Field
V	Via	9	Dark Field
M2	Metal 2	10	Dark Field

(c)

Figure A1.4 Schematic layouts (a) Photomask M1 (b) Photomask M2 (b) Photomask M3

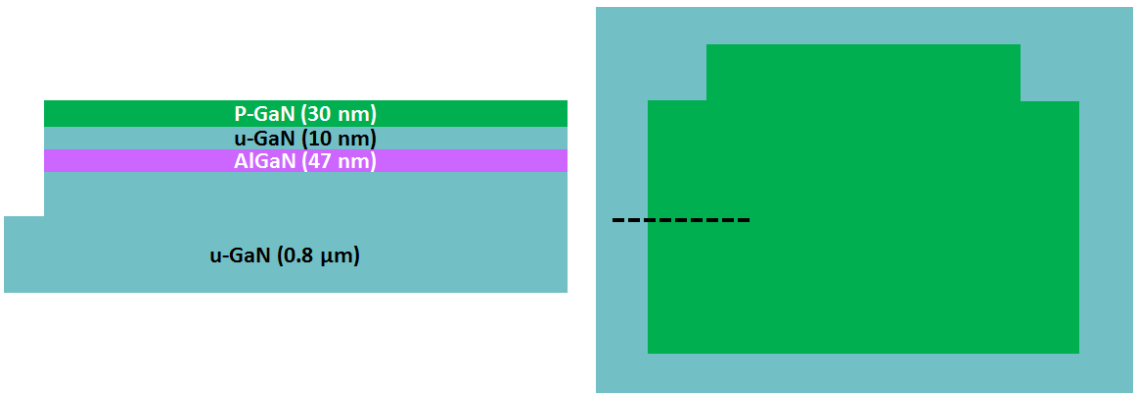
Process Flow (Sheffield)

S. No	Process	Mask (Tone)	Sub-process	Equipment/Chemical
1	Alignment Mark Etching	GDS Layer 0 – Alignment Mark – AM (Dark Field)	1.1 3-Step Cleaning	n-Butyl Acetate-Acetone-IPA
			1.2 Photolithography	Carl Suss MJB3 UV300
			1.3 ICP Etch (350 nm)	Oxford PlasmaSystem100
			1.4 Photoresist Stripping	POSISTRIP EKC830
			1.5 Etch Depth measurement	Veeco Dektak 150
2	Device Isolation	GDS Layer 1 – Isolation – ISO (Light Field)	2.1 3-Step Cleaning	n-Butyl Acetate-Acetone-IPA
			2.2 Photolithography	Carl Suss MJB3 UV300
			2.3 ICP Etch (125 nm)	Oxford PlasmaSystem100
			2.4 Photoresist Stripping	POSISTRIP EKC830
			2.5 Etch Depth measurement	Veeco Dektak 150
3	Pad Insulation	GDS Layer 4 – Gate Isolation - GI (Dark Field)	3.1 3-Step Cleaning	n-Butyl Acetate-Acetone-IPA
			3.2 PECVD Deposition (Si_3N_4 - 150 nm)	Plasmatherm 790 series
			3.3 Thickness verification on monitor wafer	JA Woollem VASE®
			3.4 Primer application	Hexa-Methyl-Di-Silazane (HMDS)
			3.5 Photolithography	Carl Suss MJB3 UV300
			3.6 Wet etch	Buffered HF (10%)
			3.7 Photoresist Stripping	POSISTRIP EKC830
			3.8 Etch Depth measurement	Veeco Dektak 150
4	Mesa etch	GDS Layer 2 – Mesa Etch - ME (Light Field)	4.1 3-Step Cleaning	n-Butyl Acetate-Acetone-IPA
			4.2 Photolithography	Carl Suss MJB3 UV300
			4.3 ICP Etch (65 nm)	Oxford PlasmaSystem100
			4.4 Photoresist Stripping	POSISTRIP EKC830
			4.5 Etch Depth measurement	Veeco Dektak 150
5	Drain/Source Contact	GDS Layer 3 – N Contact - NC (Dark Field)	5.1 3-Step Cleaning	n-Butyl Acetate-Acetone-IPA
			5.2 Photolithography	Carl Suss MJB3 UV300
			5.3 Dilute HCl dip	
			5.4 Thermal evaporation of Ti/Al/Ni/Au/ (20/100/45/55 nm)	Edwards Coating System E306A
			5.5 Lift-off	
			5.6 RTA (800^0 C for 1 min in N_2 ambient)	Mattson RTA System
6	Base Contact	GDS Layer 5 – P Contact - PC (Dark Field)	6.1 3-Step Cleaning	n-Butyl Acetate-Acetone-IPA
			6.2 Photolithography	Carl Suss MJB3 UV300
			6.3 Dilute HCl dip	
			6.4 Thermal evaporation of Ni/Au (20/20 nm)	Edwards Coating System E306A
			6.5 Lift-off	
			6.6 RTA (500^0 C for 10 mins in air ambient)	Mattson RTA System
			6.7 3-Step Cleaning	n-Butyl Acetate-Acetone-IPA
			6.8 Photolithography	Carl Suss MJB3 UV300
			6.9 Thermal evaporation of Ti/Au (20/200 nm)	Edwards Coating System E306A
			6.10 Lift-off	

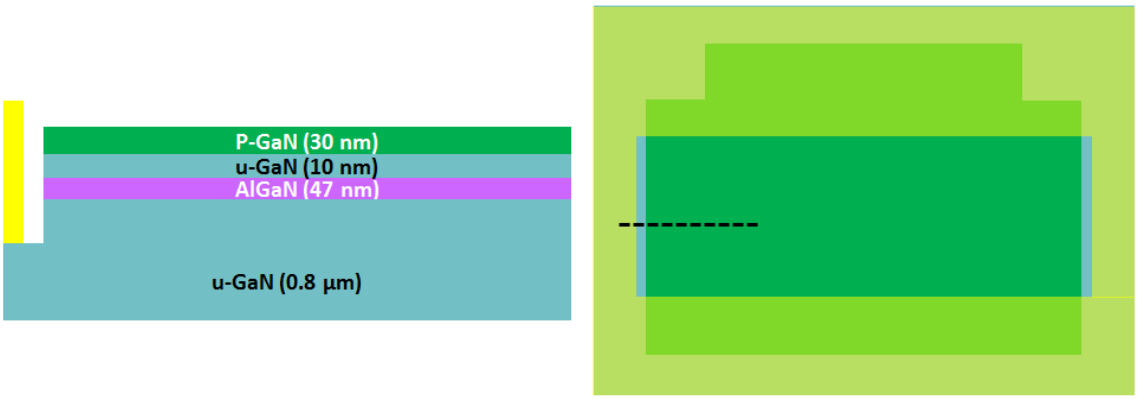
S. No	Process	Mask (Tone)	Sub-process	Equipment/Chemical
7	Gate Contact	GDS Layer 8 – Gate Contact - GC (Dark Field)	7.1 3-Step Cleaning	n-Butyl Acetate-Acetone-IPA
			7.2 Photolithography	Carl Suss MJB3 UV300
			7.3 Dilute HCl dip	
			7.4 Thermal evaporation of Ni/Au (20/200 nm)	Edwards Coating System E306A
			7.5 Lift-off	
8	Gate Insulation & Via	GDS Layer 9 – Via - V (Dark Field)	8.1 3-Step Cleaning	n-Butyl Acetate-Acetone-IPA
			8.2 PECVD Deposition (Si_3N_4 - 500 nm)	Plasmatherm 790 series
			8.3 Thickness verification on monitor wafer	JA Woollem VASE®
			8.4 Photolithography	Carl Suss MJB3 UV300
			8.5 RIE Etch (500 nm)	
			8.6 Photoresist Stripping	POSISTRIP EKC830
			8.7 Etch Depth measurement	Veeco Dektak 150
9	Second Metal	GDS Layer 10 – Metal 2 – M2 (Dark Field)	9.1 3-Step Cleaning	n-Butyl Acetate-Acetone-IPA
			9.2 Photolithography	Carl Suss MJB3 UV300
			9.3 Thermal evaporation of Ti/Au (20/750 nm)	Edwards Coating System E306A
			9.4 Lift-off	
10	Dielectric deposition /Pad opening	GDS Layer 7– Pad (Dark Field)	10.1 3-Step Cleaning	n-Butyl Acetate-Acetone-IPA
			10.2 Dielectric deposition (1 µm)	
			10.3 Photolithography	Carl Suss MJB3 UV300
			10.4 RIE Etch	
			10.5 Photoresist Stripping	POSISTRIP EKC830
			10.6 Etch Depth measurement	Veeco Dektak 150
			10.7 3-Step Cleaning	n-Butyl Acetate-Acetone-IPA

Schematics of layout/cross-section of a Serpentine Gate HFET after each processing step

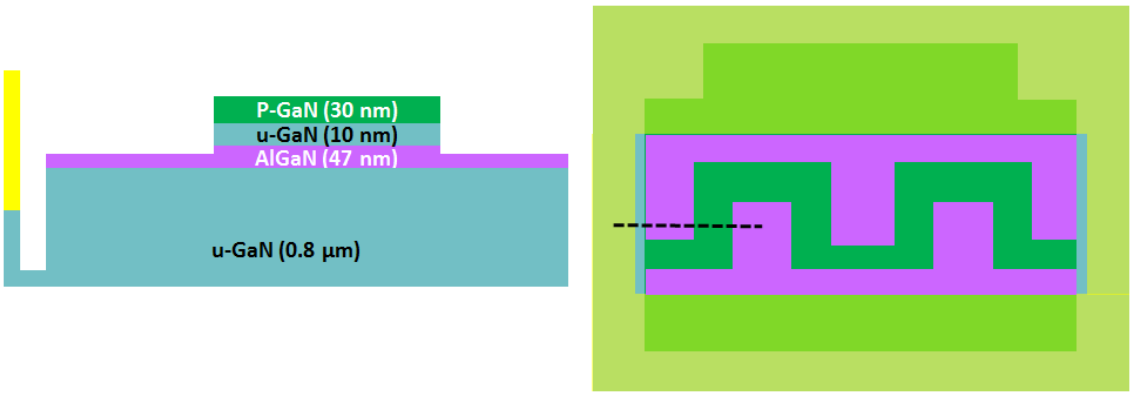
Isolation Etch



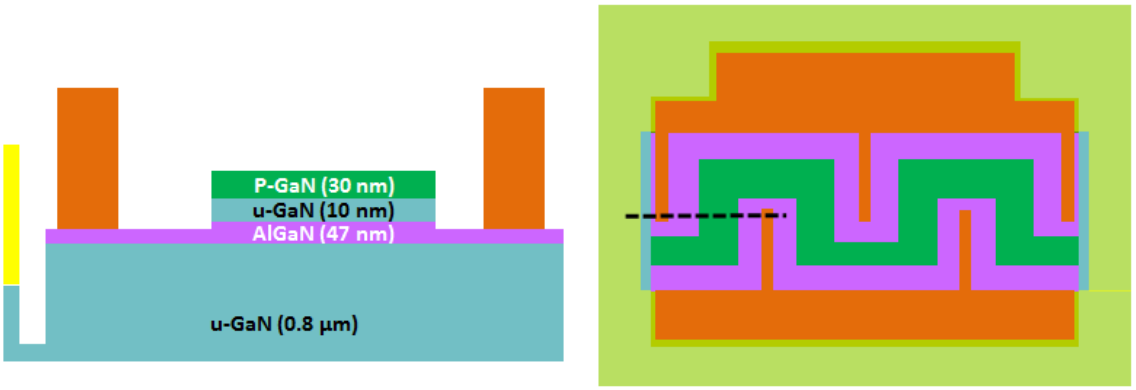
Pad Insulation



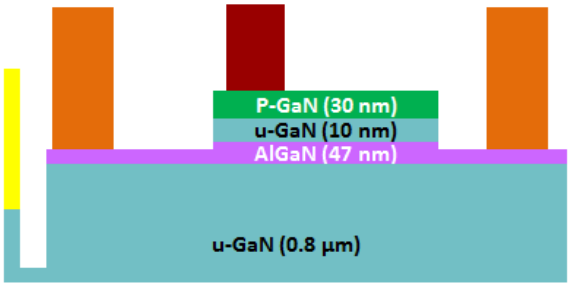
Mesa Etch

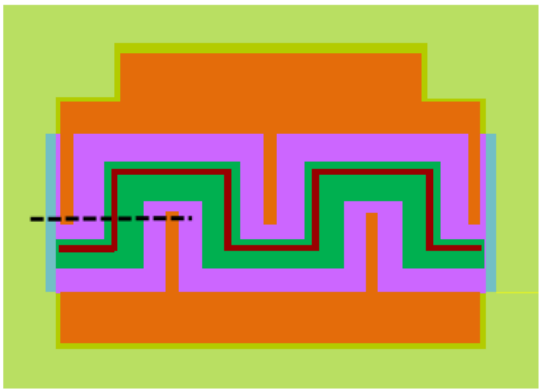


Drain/Source Contact

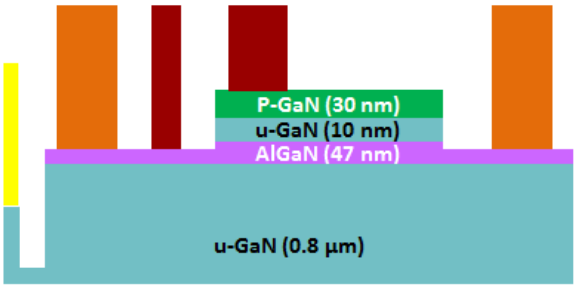


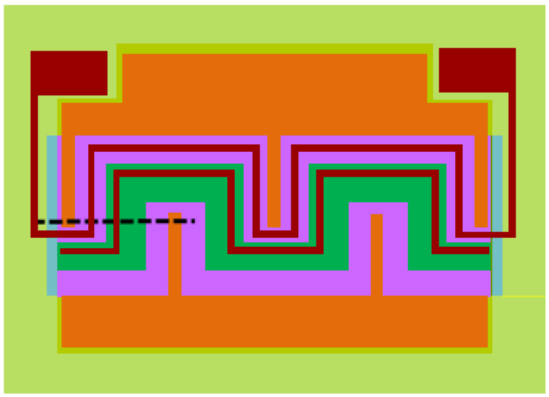
Base Contact



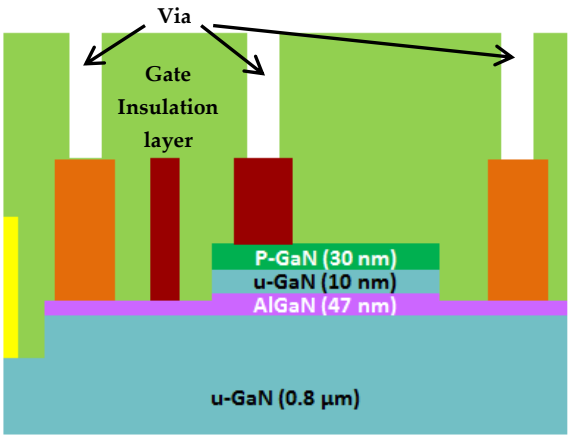


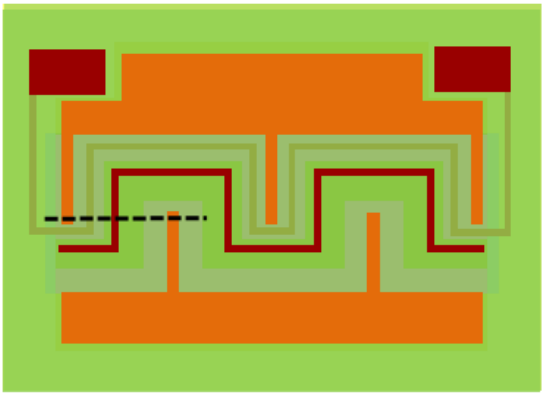
Gate Contact



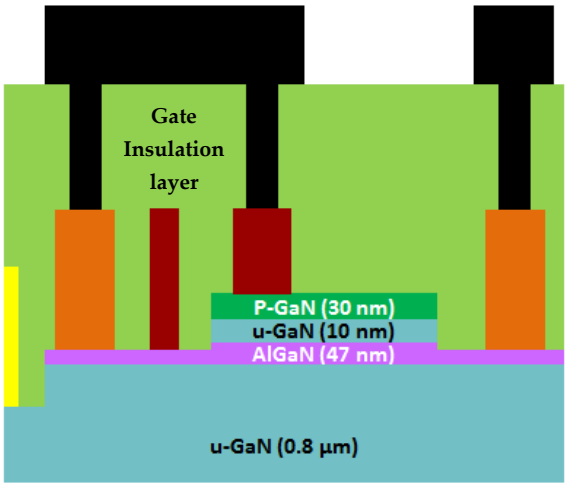


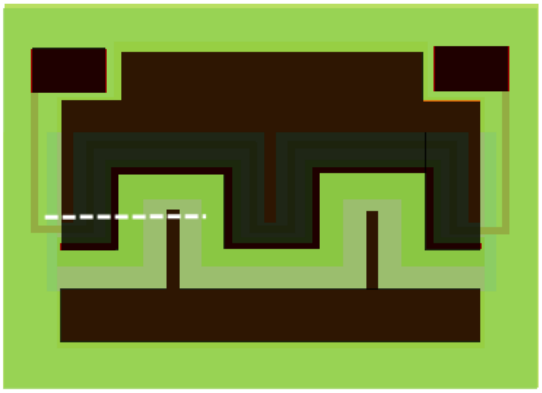
Gate Insulation/Via



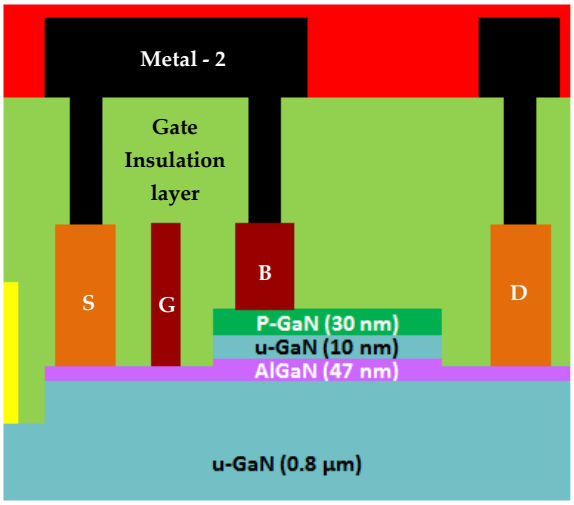


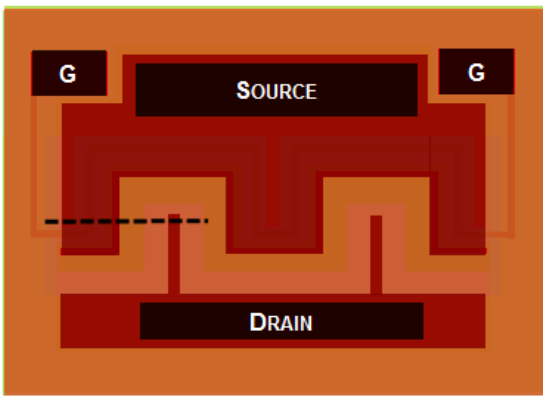
Second Metal





Final Dielectric deposition and Pad Opening





Appendix-2

List of Acronyms

- 2DEG − Two-Dimensional Electron Gas
- 2DHG − Two-Dimensional Hole Gas
- AlGaAs − Aluminium Gallium Arsenide
- AlGaN − Aluminium Gallium Nitride
- AlInN − Aluminium Indium Nitride
- AlN − Aluminium Nitride
- BFOM − Baliga's Figure Of Merit
- BHFOM − Baliga's High Frequency Figure Of Merit
- BTU − British Thermal Unit
- CTE − Co-efficient of Thermal Expansion
- CV − Capacitance Voltage
- CVD − Chemical Vapor Deposition
- FOM − Figure Of Merit
- FP − Field Plate
- GaAs − Gallium Arsenide
- GaN − Gallium Nitride
- GDS − Graphic Database System
- GTO − Gate Turn-Off thyristor
- HCAFOM − Huang's Chip Area Figure Of Merit
- HCl − Hydrochloric acid
- HCP − Hexagonal Close Packed
- HEMT − High Electron Mobility Transistor
- HF − Hydrofluoric acid
- HFET − Heterostructure Field Effect Transistor
- HMDS − Hexa-Methyl-Di-Silazane
- HMFOM − Huang's Material Figure Of Merit

- HS – High Side
- HTFOM – Huang's Thermal Figure Of Merit
- HV – High Voltage
- HVPE – Hydride Vapor Phase Epitaxy
- IBE – Ion Beam Etching
- IC – Integrated Circuit
- ICP – Inductively Coupled Plasma
- IGBT – Insulated Gate Bipolar Transistor
- InN – Indium Nitride
- JFOM – Johnson's Figure Of Merit
- KFOM – Keyes's Figure Of Merit
- LDMOS – Laterally Diffused Metal Oxide Semiconductor
- LS – Low Side
- MBE – Molecular Beam Epitaxy
- MESFET – Metal Semiconductor Field Effect Transistor
- MOCVD – Metal Organic Chemical Vapor Deposition
- MOSFET – Metal Oxide Semiconductor Field Effect Transistor
- NBS – Negative Bias Shift
- PBS – Positive Bias Shift
- PDFOM – Power Device Figure of Merit
- PECVD – Plasma Enhanced Chemical Vapor Deposition
- PoC – Proof of Concept
- PSJ – Polarisation Super Junction
- RESURF – Reduced Surface Field
- RF – Radio Frequency
- RIE – Reactive Ion Etching
- RTA – Rapid Thermal Annealing
- SBD – Schottky Barrier Diode

- SiC – Silicon Carbide
- SJ – Superjunction
- SOI – Silicon On Insulator
- TAM – Total Available Market
- TLM – Transmission Line Method/Model
- VLSI – Very Large Scale Integration