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Design and Control of On-board Bidirectional Battery Chargers with Islanding Detection for Electric Vehicle Applications

by

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Abstract

Electric vehicles have gained popularity over the last decade due to concerns regarding climate change as well as depleting fossil fuel reserves. One of the important components of electric vehicles is the battery charging system that has been the focus of recent research interest in terms of vehicle to grid (V2G) power transfer with the aim of providing peak load levelling for the grid as well as a buffer for excess renewable energy. The research addressed in this thesis is focused on single-phase on-board bidirectional chargers for electric vehicle applications where emphasis is given to the design, control and islanding detection aspects.

A comparative study between a low frequency transformer based and high frequency DAB based bidirectional charging system is carried out and the weight, cost and efficiency between the two topologies compared. An optimised LCL filter design method for the two converters is presented which characterises the high frequency current ripple as well as the losses in the damping resistor. Controller design, simulation and experimental validation of the two converters are also presented.

The impact of 3rd harmonics on the performance of second order generalised integrator (SOGI) phase locked loops (PLLs) is investigated through an analytical method to predict the resulting output harmonic magnitudes. Two modified SOGI PLLs are presented where the harmonic rejection performance has been improved.

A new PLL structure based on the novel IIR filter proposed by Ed Daw et al. is investigated for application in grid converters. The new PLL is evaluated with hardware-in-the-loop (HIL) simulations for transient and abnormal grid conditions and compared with the SOGI PLL for performance evaluation as well as computational requirements. The new PLL is validated in bidirectional charger hardware.

A new islanding detection algorithm based on the detection of high frequency switching harmonic signature with frequency hopping is presented which has the advantage of multi-inverter compatibility. The difficulty in detection for PWM harmonic based methods when capacitive loads are present is analysed. Furthermore, the algorithm is validated in hardware.

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Chapter 1

Introduction

This chapter introduces the general background, context and the motivation for this research. The key contributions of the thesis are also highlighted followed by the outline of the thesis.

1.1. General Introduction

Due to the industrialisation and exponential increase in world population over the previous two centuries, the carbon emissions due to human activity have also seen an exponential increase. For example, the alarming rate of increase of carbon emissions due to the burning of fossil fuels and cement production is depicted in Fig. 1-1. Furthermore, the atmospheric and ocean CO_2 levels have also followed this pattern of increase. This effect has been further compounded by the rapid industrialisation of developing countries.

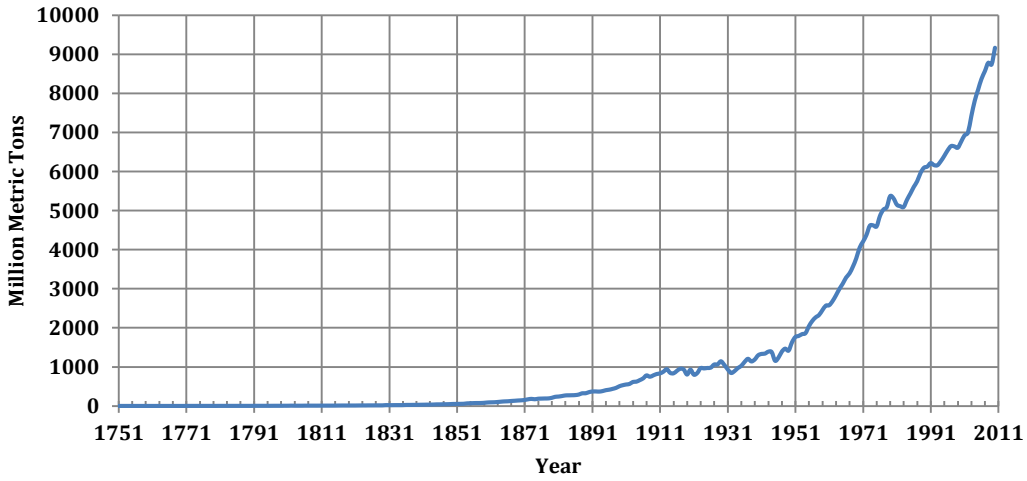


Fig. 1-1 Total carbon emissions due to the burning of fossil fuels and cement production from 1751 to 2010 (Data from [1])

There is wide consensus in the field of climate science that man-made CO_2 emissions are one of the main causes of the recent increase in global temperatures and the associated anomalies in the climate [2-4]. Furthermore, there has been recent research [5] that suggests that even if all man-made CO_2 emissions were eliminated, the recovery time for the climate could take up to 1000 years.

As a solution for reducing carbon emissions, there has been a different outlook at the ways in which power is generated where more renewable sources of energy are favoured, as well as a trend for more efficient methods of consumption and the storage of the generated energy.

Renewable energy sources include wind, hydro, solar, geothermal, tidal as well as biodiesels that are synthesised from bio matter. Changes to the way that the energy consumed include, the trend for more efficient vehicles as well as the widespread deployment of electric and hybrid electric vehicles in the transportation sector. The sectors of industrial processing as well as the domestic power consumption have also followed a similar path for the optimisation of energy efficiency, driven in part by government regulations (such as the *private rented sector energy efficiency regulations [6]* and the *climate change levy* [7]).

1.1.1. Electric Vehicles (EVs)

Due to the concerns regarding climate change which have resulted in tough emission regulations, increase in global demand for energy as well as the rapid depletion of fossil fuel sources, there is a global drive for the development and transition into electric, hybrid as well as fuel cell vehicles [8].

The broad term of “Electric Vehicles” can be categorised into three main types of vehicles, which are battery electric vehicles, hybrid electric vehicles (HEVs) and fuel cell vehicles (FCVs) [8].

Battery EVs

Battery EVs are powered exclusively with battery (most commonly Lithium based batteries) and ultracapacitor based energy storage technologies, which in turn drives an electric motor(s), and therefore have zero emissions. The disadvantages of battery based EVs are that the typical driving range is short due to the low energy density of batteries, the long recharge time and the high cost of batteries [8].

HEVs

To overcome the issues of battery based EVs, HEVs have been developed which combines an internal combustion engine (ICE) with an electrical drive train in either a series, parallel, series-parallel or complex arrangements. HEVs therefore offer the increased driving range of conventional ICE vehicles with the added advantage of energy efficiency with the use of energy recovery, storage and management strategies.

In the series arrangement, the ICE converts the chemical energy from the conventional fuel source to mechanical energy after which it is converted to electricity through a generator followed by an electric motor(s) for driving the wheels. The efficiency of series HEVs are lower due to the three stage energy conversion process despite the simplicity of the power train architecture [8].

In the parallel HEV arrangement, both the ICE as well as the electric motor drives the wheels at the same time. The advantages of this arrangement include the elimination of the separate generator as well as the smaller size of ICE and motor due to the shared power delivery.

The series-parallel method combines properties of both the series as well as the parallel type HEVs with the goal of incorporating the benefits of both architectures. Series-parallel HEVs differ from parallel HEVs by the addition of a generator that is linked to the ICE. However, the method has the disadvantage of increased complexity and cost [8].

The complex HEV is similar to the series-parallel HEV, but has a more complex design where the generator that is linked to the ICE can also act as a motor. Although the complex HEV offers more flexibility in terms of energy management and therefore efficiency, the downside is the added complexity and cost.

HEVs typically implement regenerative braking by using the motor(s) as a generator(s) to charge the batteries/ultracapacitors as opposed to dissipating the kinetic energy as heat in the brakes.

The method of replenishing the energy in HEVs can either be through conventional refuelling (gasoline/diesel) or by charging the battery externally. The latter type of HEVs is generally referred to as plug-in hybrid electric vehicles (PHEVs).

FCVs

FCVs are also a zero emission vehicle due to the hydrogen based fuel cell energy source. The power delivery system in a FCV is comprised of a hydrogen storage tank followed by fuel cells where the electricity is generated. This is followed by an electric motor drive system. Although the FCVs have the advantage of zero emissions and reasonable driving range, the disadvantages include the high cost and low cycle life of fuel cells as well as the difficulty in the storage and transport of hydrogen as a fuel.

1.1.2. Electric Vehicle Chargers

The charging systems for EVs can be categorised into 2 types, which are, on-board and off-board charger systems. The off-board charger systems are generally capable of providing a higher amount of power that is delivered to the vehicle as DC. By using off-board chargers, it is possible to move the weight of

the AC-DC conversion hardware to the external infrastructure, which is advantageous as it reduces the total weight of the EV.

However, having an on-board charger provides more flexibility since the EV is able to charge in residential as well as many other locations where an AC power source is available. On-board chargers are usually categorised into 2 levels; level 1 being single phase where the power rating is typically under 3 kW and level 2 being 3-phase chargers capable of up to 20 kW (for example, Tesla Model S dual wall charger).

Wireless inductive charger systems for EVs are also available [9, 10] although not as widely used as conductive type chargers due to the issues of lower efficiency and high cost.

Grid-to-Vehicle (G2V) and Vehicle-to-Grid (V2G)

Although the main goal of an EV charger system is to recharge the battery (G2V), there is also the opportunity to utilise the charger infrastructure to reverse the flow of power so as to provide power to the grid (V2G) even though it seems counterintuitive at first glance.

Since the electric utility system has to keep up with a wide range of demand conditions, the cost of power also varies throughout the day where generally the night-time demand is low and hence the cost is lower. Since EVs are parked and not in use most of the time, EVs as an energy storage mechanism has been proposed [11-16] and is currently under trial in many countries (leading countries include Japan, US, Germany, Denmark, South Korea and the UK).

One of the aims of the V2G concept is to provide power for transient demands “peak load levelling” where traditional generation is not able to react fast enough. Other goals include frequency stabilisation [11, 12] and reactive power compensation [14]. Furthermore, there are proposals [15] where V2G technology could be used for the buffering of excess renewable energy in EV

batteries during low utility demand periods and to provide power for high demand times thereby maximizing the renewable energy production.

Some of the key issues in V2G technology are connection with a polluted grid [17] and the detection of islanding condition as it causes safety problems for utility workers [18]. This thesis addresses these issues for single phase systems with improvements to grid synchronisation as well as islanding detection methods. Other issues in V2G technology include the low overall efficiency due to the charge-discharge losses in batteries; the issue of excess battery wear as well as the absence of a unified standard for communication with the utility system. However, V2G technology has a promising future as battery technologies mature and as utility and vehicle systems are getting more and more integrated through the Internet.

On-Board Bidirectional Charger (OBBC) topology

In this thesis, the focus will be on single-phase on-board bidirectional charger systems, as single phase utility systems are the most accessible form in a residential environment. The typical topology for such systems is illustrated in Fig. 1-2. The first stage is the AC to DC converter, which facilitates the bidirectional power from the utility to the DC link of the charger system while maintaining unity power factor. The regulation of the battery current is handled through the DC/DC converter [19]. Where galvanic isolation is required, a high frequency transformer is incorporated into the DC/DC converter stage as the transformer weight is reduced with increasing operating frequency.

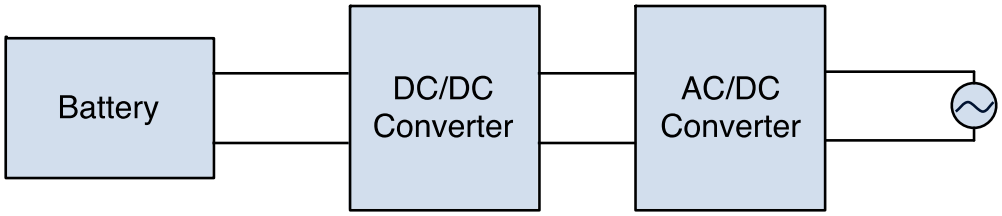


Fig. 1-2 Typical topology of a bidirectional charger

Examples of non-isolated bidirectional DC-DC converters that are commonly used include half-bridge, Ćuk, SEPIC/Luo and cascade buck-boost converters [20, 21].

Isolated bidirectional DC-DC converters can either be half bridge or full bridge topologies. The dual half bridge converter (DHB) proposed in [22] and the non-regulating half bridge converter presented in [23] are examples of half bridge converters. Examples of full bridge converters are; the dual-active bridge (DAB) converter [24] and full bridge resonant type converters [25-31].

Furthermore, in applications where a wide input/output voltage range is required, a two stage converter consisting of a DAB/resonant and a non-isolated DC/DC converter is utilised in order to achieve the maximum efficiency [32] at the cost of increased complexity.

Grid synchronisation

Grid synchronisation is the process obtaining the instantaneous parameters of the grid voltage vector in order to facilitate power transfer in a power converter. The most common method of synchronisation is the phase locked loop (PLL) [33].

A variety of different PLL algorithms have been developed over the years [17, 34-43] with varying levels of complexity and performance. This thesis focusses on the widely used second order generalised integrator (SOGI) based PLL [38] as well as a new class of discrete time PLL termed the phasor infinite impulse response (PIIR) PLL that has been developed by Ed Daw et al. [Appendix I]. A detailed discussion of the current methods of grid synchronisation is carried out in Chapter 4.

Islanding detection

Islanding refers to the condition where the distributed generator (DG) continues to operate with local loads after the utility has been disconnected [44]. Unintentional islanding is undesired since it poses a hazard to utility workers as well as due to the damage that can result to equipment when reclosure of the utility occurs while the DG is out of phase with the utility [18]. IEEE1547 requires that a DG system detects and ceases to energise the area electrical power system (EPS) within 2 seconds of islanding. Since V2G operation of a battery charger constitutes as a distributed generator, islanding detection and prevention is an important consideration in a bidirectional battery charger.

Islanding detection methods are broadly categorised into two methods which are, passive and active methods of detection. Passive methods rely on monitoring various parameters of the grid voltage/current as a means of islanding detection. Active methods in contrast are based on introducing a disturbance to the output of the converter and monitoring the response of the voltage/current. Chapter 5 of the thesis focusses on the development of a passive method of islanding detection.

1.2. Motivation

Since V2G is an emerging technology and has the potential to change the landscape of the utility network, in these times of uncertainty on the future of fossil fuels and climate change, this research aims to contribute to the development of on-board bidirectional charging systems for electric vehicles.

The main aims of the research are highlighted as follows.

1. The investigation, design, simulation and experimental demonstration of an alternative topology of bidirectional charger utilising a low frequency

transformer integrated with the motor drive and comparison with a DAB based charger system.

2. Analysis of the effects of the 3rd harmonic distortion on the output of the second-order generalised integrator (SOGI) based phase locked loop (PLL) and methods to mitigate the issue.
3. Investigation of the viability of a new class of discrete time PLL that has been proposed by Ed Daw et al. [Appendix C] termed the phasor infinite impulse response PLL (PIIR PLL) in the application of grid converters.
4. Development of a new passive islanding detection method for grid converters.

1.3. Main Contributions

The main contributions of the research are outlined as follows.

1. A comparative study between a low frequency transformer based and high frequency DAB based bidirectional charging system have been carried out and the weight, cost and efficiency have been compared.
2. An optimised LCL filter design method for the two converters has been presented which characterises the high frequency current ripple as well as the losses in the damping resistor.
3. Controller design, simulation and experimental validation of the two converters have been carried out.
4. The impact of 3rd harmonic distortion on the performance of SOGI PLLs has been investigated through an analytical method that has been developed to predict the resulting output harmonic magnitudes.
5. The 3rd harmonic rejection performance of the SOGI PLL has been dramatically improved by the addition of notch filters in either the feedback or pre-filter configurations.

6. A new PLL structure based on the novel IIR filter proposed by Ed Daw et al. [Appendix C] has been investigated for application in grid converters. The new PLL has been evaluated with hardware-in-the-loop (HIL) simulations for transient and abnormal grid conditions and compared with the SOGI PLL for performance evaluation as well as computational requirements. Furthermore, the new PLL has been demonstrated in both G2V and V2G modes of operation in the bidirectional charger hardware.
7. A new islanding detection algorithm based on the detection of high frequency switching harmonic signature with frequency hopping has been presented which has the advantage of multi-inverter compatibility. Furthermore, the difficulty in detection for PWM harmonic based methods when capacitive loads are present has been analysed. The algorithm has also been demonstrated in hardware.

1.4. Outline of Thesis

The outline of the remaining chapters of the thesis is given below.

Chapter 2 – On-board Bidirectional Charger Design and Comparison

- The comparative study of two bidirectional charger topologies is carried out with an emphasis on the design procedure for the magnetic components and switching device selection.
- The optimal LCL filter design method for both converter types is presented.

Chapter 3 – Controller Design, Simulation & Experimental Results of the On-Board Bidirectional Charger Systems

- The controller design methodology for the two converters is presented.
- The two On-Board Bidirectional Charger (OBBC) systems with the controllers are simulated and the results are presented.

- Hardware verification results are presented and discussed.

Chapter 4 – Grid Synchronisation in Converters

- The performance of the SOGI PLL under 3rd harmonic distortion in the input is investigated through an analytical method.
- Two improved topologies of SOGI PLL for the suppression of 3rd harmonic interference is presented and simulated in HIL.
- The viability of the PIIR PLL for grid converter applications is investigated and validated in hardware.

Chapter 5 – Islanding Detection

- A new islanding detection method based on the detection of high frequency switching harmonic signature is presented.
- The difficulty in detection for PWM harmonic based methods when capacitive loads are present has been analysed.
- The new algorithm is demonstrated in hardware.

Chapter 6 – Conclusions and Future Work

- This chapter summarises the conclusions of the work that is presented in the thesis and discusses the scope for future work.

1.5. List of Publications

- **K. Colombage**, J. Wang, C. Gould, and C. Liu, "PWM Harmonic Signature Based Islanding Detection for a Single-Phase Inverter with PWM Frequency Hopping," in *Energy Conversion Congress and Exposition (ECCE), 2015 IEEE*, 2015.

- C. Gould, **K. Colombage**, J. Wang, D. Stone, and M. Foster, "A comparative study of on-board bidirectional chargers for electric vehicles to support vehicle-to-grid power transfer," in *Power Electronics and Drive Systems (PEDS), 2013 IEEE 10th International Conference on*, 2013, pp. 639-644.

- C. Liu, J. Wang, **K. Colombage**, C. Gould, B. Sen, and D. Stone, "Current Ripple Reduction in 4kW LLC Resonant Converter Based Battery Charger for Electric Vehicles," in *Energy Conversion Congress and Exposition (ECCE), 2015 IEEE*, 2015. *

- X. Yuan, J. Wang, and **K. Colombage**, "Torque distribution strategy for a front and rear wheel driven electric vehicle," in *Power Electronics, Machines and Drives (PEMD 2012), 6th IET International Conference on*, 2012, pp. 1-6.

** The contribution to the publication was the MATLAB coding for obtaining the small signal transfer function of the LLC converter.*

The second and third chapter of the thesis presents work carried out under two projects which are, the Personal Mobility (P-MOB) project [45] followed by the Internet of Energy (IoE) project [46]. The work has been done in collaboration with project partners as well as staff at the University of Sheffield.

Chapter 2

On-board Bidirectional Charger Design and Comparison

This chapter compares two promising topologies of single-phase on-board bidirectional chargers for use in an electric vehicle, the first with a low frequency transformer (LFT) and the other with a high frequency isolating transformer.

2.1. Introduction

An on-board charger needs to be lightweight, compact and low cost for it to be commercially viable and practical. Furthermore, galvanic isolation between the grid side and battery side is also an important requirement to ensure the safety of the user.

There are a number of converter topologies that match the above-mentioned criteria. In terms of the isolation requirement, the most common implementation today is a high frequency transformer (HFT) operating in a switching frequency range of the 10s of kHz to around 100 kHz depending on the converter topology. In contrast, a LFT operating in the fundamental grid frequency (50 Hz) weighs significantly more and is much larger in size. However, if the power electronics of the traction drive were also to be used for interfacing with the utility grid, there will be the added benefit of cost reduction, as the power electronic components are one of the major costs of a vehicle charger. A similar concept was introduced by S. Lacroix et al., 2010 [47] where the traction drive along with the motor windings were used to form the voltage source inverter and frontend grid filter. However, this method does not meet the requirement for galvanic isolation as the motor winding only act as a

filter stage. The alternate topology that is proposed in this chapter is shown in Fig. 2-1.

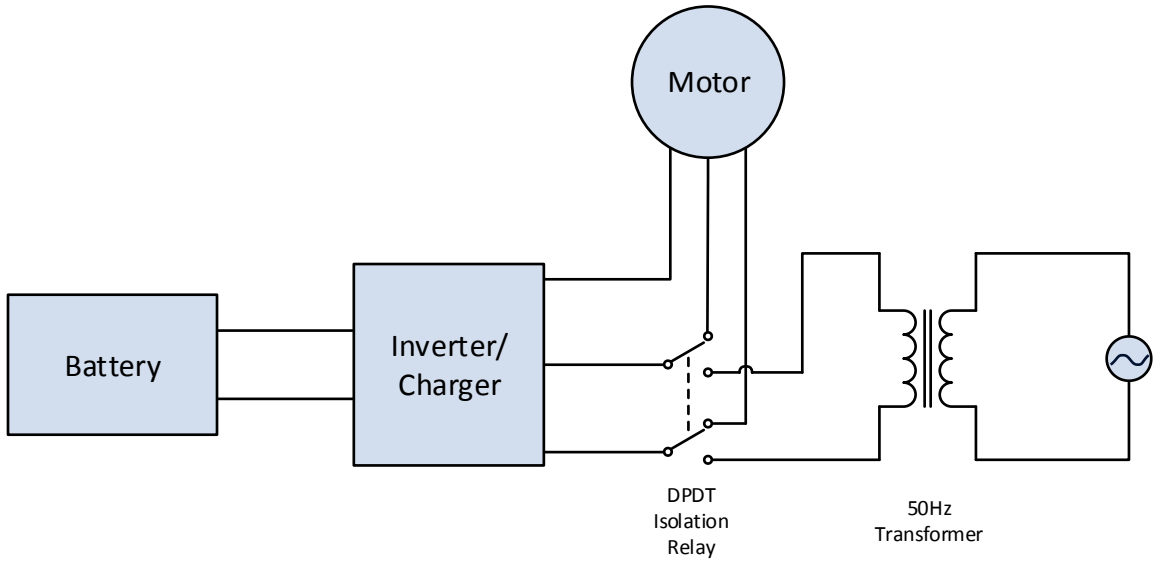


Fig. 2-1 Bidirectional charger topology with shared power electronics

The 50 Hz isolation transformer is connected to the traction drive through a double-pole, double-throw (DPDT) relay, which is activated depending on charge mode or traction mode of operation. The 3rd phase connection of the motor can be left connected to the motor drive inverter since there is no return path for any current flow from the motor back to the inverter (motor is floating) as well as due to the absence of switching action in the unused leg of the H-bridge. This topology could also be extended for a three-phase charger by connecting all 3 legs of the inverter to a three-phase transformer through an appropriate isolating relay. A comparative study between the proposed topology and a resonant converter based bidirectional charger topology is presented in [48].

The second option is the HFT based charger and is illustrated in Fig. 2-2. In this topology, a bidirectional DC/DC converter is cascaded with a frontend AC/DC converter. This topology requires more sophisticated control as well as fully independent power electronics.

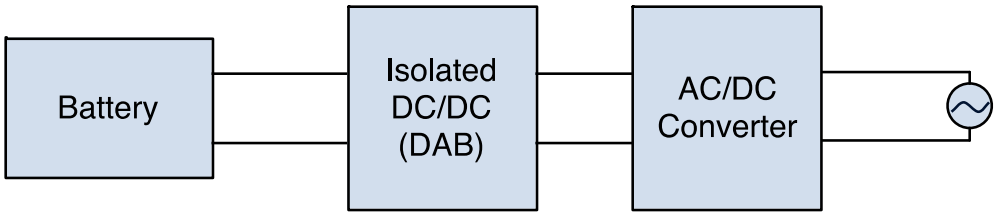


Fig. 2-2 High frequency dual active bridge based bidirectional charger

Isolated bidirectional DC/DC converters can be implemented in a variety of different topologies ranging from the simplest form which has two switching devices to the more complex topologies such as the dual active bridge and resonant converters which contain eight switching devices. The following table highlights the typical topologies of isolated bidirectional converters based on the number of switching devices [49].

Table 2-1 Isolated bidirectional converter topologies based on number of switches [49]

Number of switches	Converter type
Dual-switch	Dual-flyback [50, 51] Dual-Cuk [52]
Three-switch	Forward-flyback [53]
Four-switch	Dual-push-pull [54] Push-pull-forward [55] Push-pull-flyback [56] Dual-half-bridge [22, 57-59]
Five-switch	Full-bridge-forward [60]
Six-switch	Half-full-bridge [61]
Eight-switch	Dual-active-bridge (DAB) [24] Resonant type [25-31]

When using the same type of switching devices, in general, the power capacity of the converter is proportional to the number of switching devices and therefore the eight switch converters have the highest power capacity [49].

The DAB and resonant type converters have the advantages of soft switching operation as well as being symmetric and modular [49].

The DAB type converter consists of a transformer between two full active bridges as shown in Fig. 2-3 where the transformer's leakage inductance is depicted as 'L'. The power flow is controlled by changing the phase shift between the two bridges. The DAB converter has the advantage of simplicity in design and control as well as high efficiency [26].

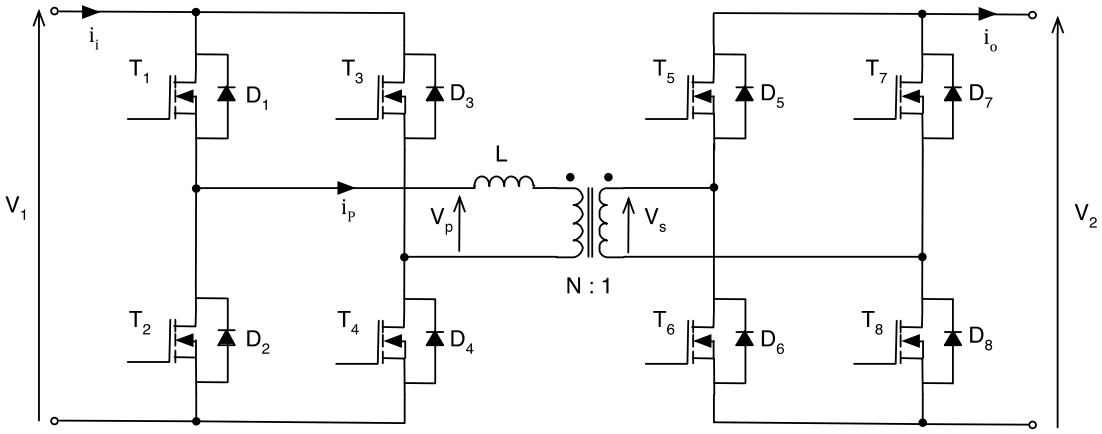


Fig. 2-3 Dual active bridge converter topology

To further improve the efficiency of the DAB converter, various resonant type converters have been developed where the addition of extra capacitors and/or inductors gives a resonant characteristic. The transformer current in a resonant converter is typically a sinusoidal (or quasi-sinusoidal when operating outside the resonant frequency) waveform.

An example of a resonant type converter is the series resonant converter (SRC) [28] which is formed by adding a series capacitor to the primary side of the DAB transformer as illustrated in Fig. 2-4. The capacitor in combination with the transformer's leakage inductance forms an LC resonant network. The SRC has the advantage of zero voltage switching (ZVS) turn-on for the primary bridge under all load conditions and therefore reduced switching losses as well

as reduced electromagnetic interference (EMI), whereas the DAB converter loses ZVS capability at low power levels [28]. The disadvantage of the SRC is the added size and cost due to the additional capacitor [28] as well as the limitation of only being able to operate under buck mode [26].

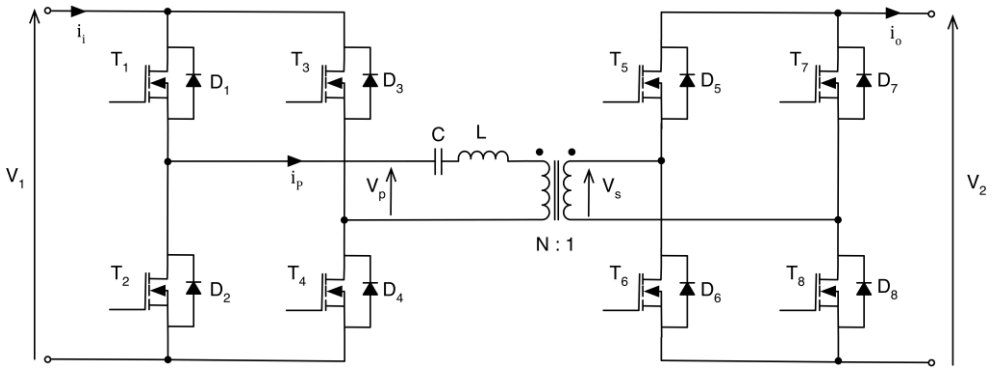


Fig. 2-4 Series resonant converter topology

By adding an extra series inductor in addition to the series capacitor, an LLC network is formed with the magnetising inductance of the transformer as depicted in Fig. 2-5. The LLC resonant converter [30] gains some advantages over the SRC such as buck and boost mode operation as well as increased efficiency due to zero current switching (ZCS) turn-off for the secondary bridge, although the reverse mode operation has the limitation of still operating as a series resonant type converter (SRC) due to the asymmetric topology.

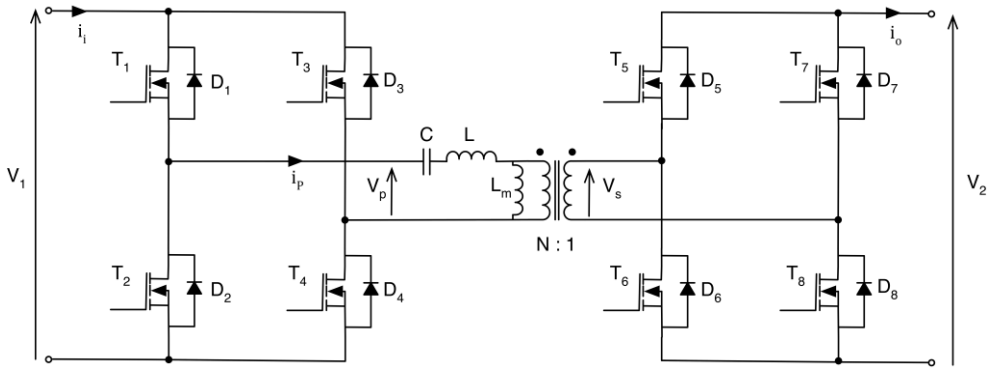


Fig. 2-5 LLC resonant converter topology

The addition of an auxiliary inductor to the LLC converter has been shown to achieve a symmetric operation for charge and discharge modes in [26]. Other types of symmetric bidirectional resonant converters include the CLLC converter [25, 27, 31] as well as the CLLLC converter presented in [29] where soft switching for all devices is achieved. However, the addition of the extra L and C components increases the complexity as well as the cost of the system.

Due to P-MOB project [45] requirements, a dual active bridge (DAB) based DC/DC converter was chosen for the high frequency transformer based bidirectional charger. The qualitative trade-offs of the two options are summarised in Table 2-2. However, a more quantitative comparison of the two candidate topologies in terms of performance and cost is essential.

Table 2-2 Comparison of charger options

	Option 1 LF transformer & motor inverter	**Option 2 HF transformer & DAB**
Advantages	• No extra switching devices required (uses motor drive) • Less complex as only the frontend controller is required • Higher reliability due to the absence of extra power electronics • Lower cost due to the reuse of power electronic components between charger and motor drive	• Lighter due to the high frequency transformer • Smaller size as a result of the high frequency transformer
Disadvantages	• Heavy due to the low frequency transformer • Larger size due to the low frequency transformer	• 12 extra switching devices required • More complex due to the extra switching and control requirements • Lower reliability due to the added DC/DC converter and extra components • Higher cost due to the added active components

2.1.1. Option 1 – Low frequency transformer based charger

The schematic of the LFT based option is shown in Fig. 2-6. Since the charger is single phase, 4 out of the 6 switching devices in the traction drive is utilised. This forms an H-bridge that is connected (through the DPDT relay) to the isolation transformer. The leakage inductance of the transformer forms part of the LCL filter for the grid side. The H-bridge switches are controlled with unipolar sinusoidal modulated PWM signals generated from the traction motor inverter controller. On the DC side, the battery can be directly connected to the DC link of the inverter. This configuration causes the battery charge current to be composed of a DC component and an AC ripple component at twice the grid frequency (100 Hz) due to the single-phase sinusoidal power flow from the grid. Methods to reduce the 100 Hz ripple have been proposed such as resonant filtering [62] and active filtering. However, these methods require additional complexity and weight in the form of inductors. Furthermore, the negative effect of low frequency ripple on Lithium polymer and Lithium Iron Phosphate batteries have been analysed in [63] and [64] respectively and have been concluded that the effect is minimal. On the other hand, pulsed charging and sinusoidal charging of Lithium-Ion batteries have been shown to improve charge time and reduce heating of the battery and therefore increase battery life in [65, 66] and [67]. The reason for the reduced heating compared with the constant current/constant voltage (CC-CV) method is due to the electrochemical impedance dependence on frequency and therefore the lower impedance of the battery at higher frequencies. Actual effect on battery life may depend on the exact chemistry used for the application.

The specification for the battery and converter was based on the requirements of the personal mobility (P-MOB) project [45] that was carried out. The specification of the battery and charger system for the small electric vehicle intended for urban transportation is shown in Table 2-3. A transformer ratio of 4 is selected so as to be able to operate over the battery and grid voltage ranges. Although the device switching frequency can be optimised for charger

efficiency and frontend filter weight, in order to reduce the complexity of the design optimisation, a switching frequency of 10 kHz is assumed considering the CPU time requirements for application in a low cost digital signal processor (DSP) platform (TI TMSF28335).

Table 2-3 Battery and converter specifications

Battery cell	**EiG ePLB C (Li[NiCoMn]O2)** **Cell voltage range: 3 V to 4.15 V (20 Ah)**
Battery Configuration	32 series, 4 parallel (32S4P) – 80 Ah
Battery voltage range	96 V to 133 V (120 V nominal)
Grid voltage range	230 V +10%/-6% (50 Hz)
Nominal power	2.2 kW (4.5 hour charge time)
Nominal grid current (rms)	9.56 A
Maximum battery current	23 A
Transformer turn ratio	4
Device switching frequency	10 kHz

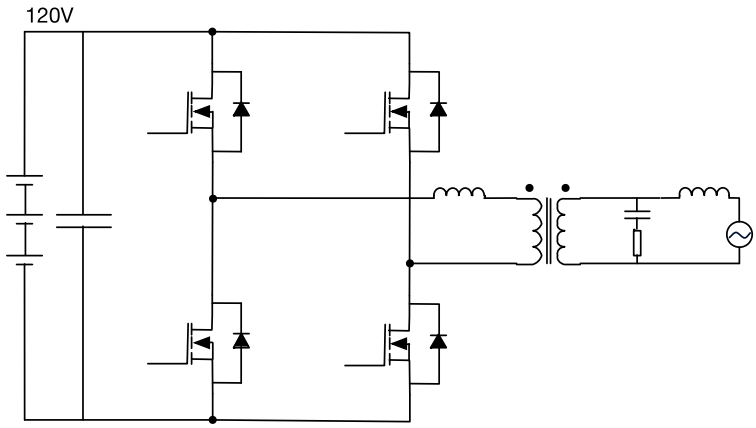


Fig. 2-6 LFT based bidirectional charger

2.1.2. Option 2 – High frequency transformer based charger

The DAB converter was first proposed by R. W. A. De Doncker et al., 1991 [24]. Fig. 2-7 illustrates the schematic of the DAB based bidirectional charger. 12 power switches are required of which 4 form the frontend and the remaining 8 form the DC/DC converter. The nominal battery voltage is 120 V and the intermediate DC link voltage is 380 V. The HFT provides the isolation as well as the inductance required for power flow by way of the leakage inductance. The grid side filter is chosen to be an LCL filter as it provides high ripple attenuation.

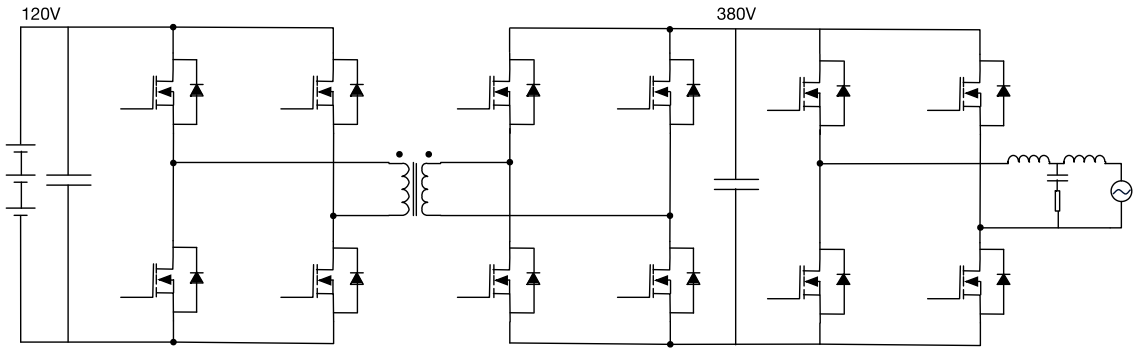


Fig. 2-7 DAB based bidirectional charger

2.2. Low frequency transformer based bidirectional charger

2.2.1. Frontend analysis and design

2.2.1.1. Frontend filter design considerations

General background of harmonic filtering for grid connection

The frontend of an AC/DC grid converter requires a harmonic filter between the voltage source converter (VSC) and the grid to attenuate switching frequency harmonics. The commonly used filter topologies for this purpose are

2nd order LC filters and 3rd order LCL filters. Other topologies that have been proposed in the past for harmonic filtering include LLCL filters [68] and RLC trap filters [69].

Although a 2nd order LC filter can be used for the system being designed, an LCL filter is the practical solution in terms of size and cost in order to meet the IEEE519-1992 and IEEE929-2000 standards [70], [44] which require that grid harmonic orders higher than the 35th should be less than 0.3% of the maximum load current. This is due to the increased attenuation provided by the LCL topology relative to an LC topology with same reactance values. The 50 Hz isolation transformer can be designed to have the required leakage inductance for the converter side and an extra grid side inductor can be designed for forming the LCL filter.

The use of a low frequency transformer with integrated reactive components that form the harmonic filtering action have been proposed in the past. In particular, J. Pleite et al. [71] have proposed the integration of the series inductance of the transformer to form an LC harmonic filter. However, the LC filters have lower attenuation compared with LCL filters, the required leakage inductance is large. V. Valdivia et al. [72] have proposed the integration of both inductors of an LCL filter configuration into the leakage inductance of the transformer and this concept [73] has been extended to the design of three phase transformers. This requires a complex magnetic design but the weight, size and cost advantage compared to a standard transformer with an extra inductor has not been proven.

LCL filters for harmonic attenuation have been investigated in literature in the past regarding the choice of components [74], active damping methods [75], [76], [77], optimisation of damping resistor value [78] and overall design procedure [79].

Active damping of LCL filters provide the benefit of increased efficiency due to the absence of the damping resistor which dissipates power. Commonly used active damping methods include the virtual resistor based method [80]

and notch filter based method [81]. The virtual resistor based method emulates the behaviour of a damping resistor though the control of the PWM inverter. However, the method requires additional voltage or current sensors in order to obtain the states of the capacitor and inductors. The notch filter based active damping method consists of adding a notch filter tuned at the resonant frequency of the LCL filter on to the current control loop. Although the notch filter based method eliminates the need for extra voltage or current sensors, it has the disadvantage of stability issues under varying grid impedances as well as complexity in controller design. The selection of active or passive method of damping must be considered based on the increased complexity and cost versus the loss in efficiency. For the purposes of the charger comparison, passive damping is selected and the damping resistance value is optimised in order to provide minimal loss in converter efficiency.

Design constraints of LCL filter

When designing the filter, there are a number of constraints to the selection of components, the first being the maximum allowable series inductance to the grid which, if exceeded, the converter is no longer able to transfer the required amount of power to/from the grid. The maximum allowable inductance depends on the DC link voltage range, normal operating grid voltage range, the maximum grid current, the dead time in the converter as well as the magnetising inductance of the transformer which acts as a shunt. The transformer equivalent circuit with reference to the frontend is presented in Fig. 2-8 where the leakage inductance of the secondary is referred to the primary side and is denoted by L_{l2}' and can be defined by equation (2-1). L_{l1}, L_m and L_g denote the primary leakage inductance, magnetising inductance and grid side LCL inductance respectively (the HF current path through the LCL capacitor is neglected). The peak magnitude of the transformer secondary voltage, V_a, referred to the primary side can be obtained by equation (2-2) where P_{max} is the maximum power transferred to the grid (2.2 kW) and ω_o is the

angular frequency of the grid voltage. Since the voltage drop in the grid side inductor is negligible, the transformer primary voltage, V_g, is equal to the grid voltage. For an H-bridge converter, the AC voltage, i.e., the transformer secondary voltage, reaches its maximum, which is equal to the DC link voltage when the modulation index is 1.0. Thus, if a dead time of 2% is considered for the converter, the minimum DC link voltage required is given by equation (2-3), where N is the transformer's winding ratio and is equal to 4.

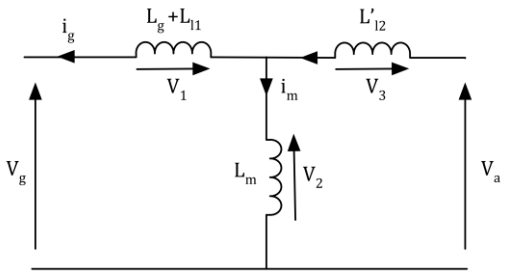


Fig. 2-8 Simplified transformer equivalent circuit

$$L'_{l2} = \left(\frac{N_1}{N_2}\right)^2 L_{l2} = \left(\frac{N_1}{N_2}\right)^2 L_{l1} \left(\frac{N_2}{N_1}\right)^2 = L_{l1} \tag{2-1}$$

$$\left|V_{a\_pk}\right| = \sqrt{2}\left|\frac{V_g^2(L_m + L_{l1}) + j\omega P_{max}\left(L_g(L_m + L_{l1}) + L_{l1}(2L_m + L_{l1})\right)}{L_m V_g}\right| \tag{2-2}$$

$$V_{dc\_min} = \frac{\left|V_{a\_pk}\right|}{0.98N} \tag{2-3}$$

It is therefore possible to plot V_{dc_min} as a function of the primary leakage inductance and is illustrated in Fig. 2-9 for different values of V_g of 230 V +10%, -6% (according to UK legislation [87]) assuming a transformer magnetising inductance of 250 mH. Since the minimum DC link voltage is equal to the minimum battery voltage (when a separate buck-boost bidirectional converter is not used), the maximum primary leakage inductance to the grid is defined as

L_{l1_max} when V_{dc} = 95 V. Fig. 2-9 shows the minimum required DC link voltage as a function of transformer primary leakage inductance for different grid voltage conditions. The green region in the figure depicts the conditions where full power transfer can take place under all grid voltages, whereas the red zone indicates inability to transfer full power due to the excessive voltage drop across the leakage inductance. It can therefore be observed from Fig. 2-9 that the maximum primary leakage inductance is 7.2 mH (i.e. any value higher than that would result in the inability to transfer power under certain DC link and grid voltage conditions).

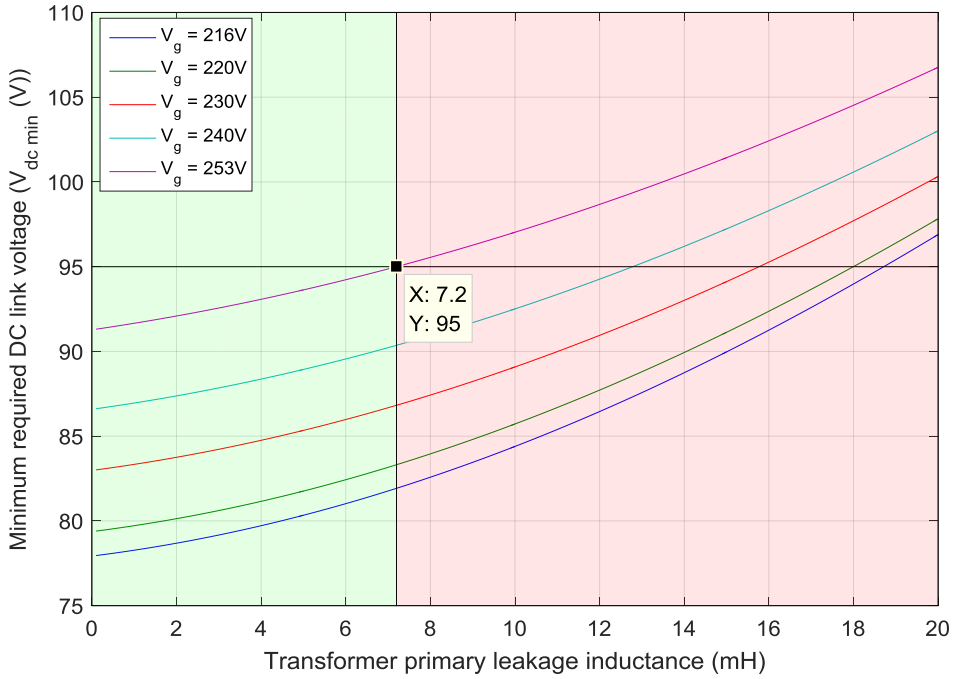


Fig. 2-9 Minimum DC link voltage vs. transformer primary leakage inductance

A large value of leakage inductance is preferred as it reduces the switching current ripple that propagates through the LCL filter, therefore resulting in lower core and winding losses associated with the inductances of the LCL filter as well as lower losses in the damping resistor due to the reduced harmonic current. Furthermore, a larger leakage inductance results in a smaller sized grid side inductor. When selecting the leakage inductance of the

transformer, the transformer efficiency and weight must also be considered and it is a trade-off between them. 70% of the maximum allowable leakage inductance is chosen for the design so as to allow operation under weak grid conditions (extra series inductance in the grid) as well as the added inductance of the grid side inductor of the LCL filter. Therefore the transformer is designed with a primary leakage inductance target of 5 mH.

2.2.1.2. Optimal LCL filter design

The structure of an LCL filter is illustrated in Fig. 2-10 where 'L' denotes the converter side inductance, or the equivalent transformer leakage inductance seen on the primary side; 'C' the filter capacitance; 'L_g' the grid side inductance and 'R' the damping resistance. The damping resistor is required in order to avoid filter resonance, alternatively active damping can be utilised. The design considerations vary depending on the optimisation criteria such as cost, size and weight or highest efficiency, or their combination. For the purposes of the LF converter design, size/weight and material cost are the primary design emphasis.

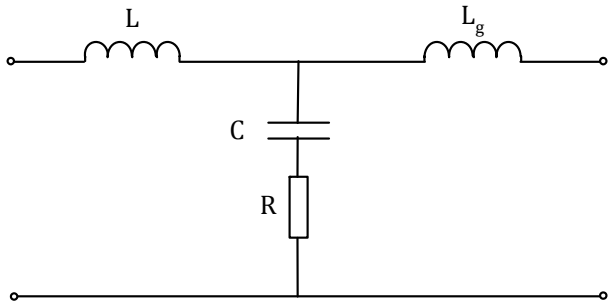


Fig. 2-10 Structure of LCL filter

The method proposed by Marco Liserre et al. [79] for designing an LCL filter involves first calculating the base impedance (Z_b) and capacitance (C_b) of the system as shown in equations (2-4), (2-5) where P_n is the active power

absorbed by the converter, E_n is the line-to-line rms voltage (for a 3 phase system) and ω_o is the grid frequency.

$$Z_b = \frac{(E_n)^2}{P_n} \quad \textbf{(2-4)}$$

$$C_b = \frac{1}{\omega_o Z_b} \quad \textbf{(2-5)}$$

The converter side inductance (L) is then selected to reduce the current ripple by 10% and the filter capacitance (C) is selected to further reduce this to 2% with the condition that the maximum capacitance is less than 5% of the base capacitance, C_b so as to reduce the effect on power factor.

However in the transformer-based system, since the converter side inductance is provided by the transformer leakage inductance, it is possible to select a larger value of leakage inductance so as to reduce the ripple well below 10%. This means that the grid side inductor can be smaller and the losses in the damping resistor can be reduced. A larger value of capacitor also reduces the size of L_g. Since the weight and cost of capacitors are generally lower than inductors, a higher capacitance value is preferred. The maximum value of capacitance for the system is 6.62 μF (5% of C_b in order to minimise the effect on power factor), however a value of 6.8 μF can be chosen to conform to standard capacitance values.

Switching Harmonics of Grid Current Based on LCL Equivalent Circuit

In order to optimally select the remaining component values of L_g and R to meet the harmonic current limits, the relationship between the reactance values and harmonic distortion must be established. Fig. 2-11 shows the LCL filter equivalent circuit for switching frequency harmonics. It can be observed that for the switching harmonics, the grid acts as a short circuit due to the

negligibly small impedance at high frequencies. The converter side inductance (L) is provided by the leakage inductance of the transformer.

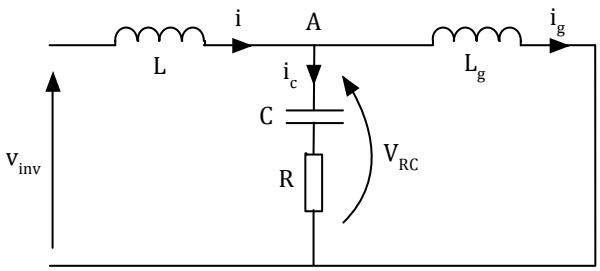


Fig. 2-11 LCL filter equivalent circuit for switching harmonics

The converter output voltage considering the switching harmonic components for naturally sampled double edge carrier PWM is given by the following equation (2-6) [82], where J_{2n-1} is the Bessel functions of $(2n-1)^{th}$ order.

$$V_{inv}(t) = V_{dc}Mcos(\omega_o t) + \frac{4V_{dc}}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{2m}J_{2n-1}(m\pi M) * cos([m+n-1]\pi)cos(2m\omega_{sw}t + [2n-1]\omega_o t) \quad \textbf{(2-6)}$$

The fundamental component of the voltage is represented by the first term and it is a function of the modulation index (M) and DC link voltage. The second term represents the switching frequency harmonics and its associated sidebands. It can be observed that the switching harmonics occur at frequencies given by,

$$\omega_h = (2m\omega_{sw} + [2n-1]\omega_o) \quad \textbf{(2-7)}$$

The relationship between m, n and harmonic number (h) is as follows,

$$h = \left(2m\left(\frac{f_{sw}}{f_o}\right) + (2n-1)\right) \quad \textbf{(2-8)}$$

Therefore, the carrier groups appear at $2mf_{sw}$ multiples (close to 20 kHz, 40 kHz etc.) and the sidebands at $(2n-1)f_o$ (odd harmonics) where f_o and ω_o is the fundamental frequency and angular frequency, respectively. f_{sw} and ω_{sw} is the voltage source converter (VSC) switching frequency and angular frequency, respectively, m is any integer above 0 and n is any integer. The dominant harmonics appear centred around the first carrier group (20 kHz) and the sidebands reduce with increasing n. Specifically, the two dominant harmonics therefore can be found to be 19950 Hz (h = 399) and 20050 Hz (h = 401) for the 10 kHz VSC switching frequency that is used for the system under investigation. The rms value of each harmonic voltage component can therefore be calculated from equation (2-9).

$$v_{inv}(h) = \frac{1}{\sqrt{2}}\left|\frac{4V_{dc}}{\pi} * \frac{1}{2m}J_{2n-1}(m\pi M) * cos([m+n-1]\pi)\right| \quad \textbf{(2-9)}$$

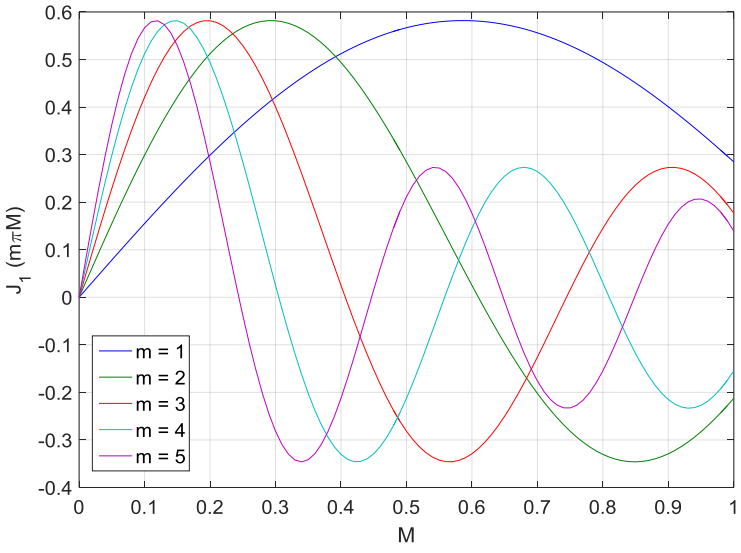


Fig. 2-12 Modulation index vs. Bessel function for different carrier groups

It is clear that the value of harmonic voltage depends on the modulation index as well as the values of 'm' and 'n'. As an example, Fig. 2-12 illustrates the value of the Bessel function $J_1(m\pi M)$ as a function of M for different values of m. Therefore the peak value of the Bessel function and the corresponding modulation index is used for each 'm' and 'n' combination when calculating the worst-case harmonic voltage.

The current through the converter side inductor can be defined as follows,

$$i_{inv}(h) = \frac{v_{inv}(h) - v_{RC}(h)}{j\omega_h L} = \frac{v_{inv}(h) - j\omega_h L_g i_g(h)}{j\omega_h L} \quad \textbf{(2-10)}$$

Furthermore, the grid side inductor harmonic current can be defined as,

$$i_g(h) = \frac{v_{inv}(h)(1 + j\omega_h RC)}{-\omega_h^2 RC(L_g + L) + j\omega_h(L_g + L) - j\omega_h^3 L_g LC} \quad \textbf{(2-11)}$$

Therefore, the converter harmonic voltage to grid switching harmonic current transfer function, $g(h)$ can be defined as follows.

$$g(h) = \left|\frac{i_g(h)}{v_{inv}(h)}\right| = \left|\frac{(1 + j\omega_h RC)}{-\omega_h^2 RC(L_g + L) + j\omega_h(L_g + L) - j\omega_h^3 L_g LC}\right| \quad \textbf{(2-12)}$$

By substituting (2-9) into (2-12), the grid current switching harmonic rms value can be calculated for a given h. Hence the grid current distortion for each harmonic as a percentage of the total maximum load current can be calculated from equation (2-13) where i_L is the maximum rms load current.

$$Distortion\ \%\ (h) = \frac{i_g(h)}{i_L} 100 \quad \textbf{(2-13)}$$

Therefore it follows that by using the above equations, the peak grid current switching harmonic distortion as a function of component values can be quantified. Since the harmonics 399 and 401 are the dominant high frequency components, the components must be chosen to inhibit the two associated harmonics to less than 0.3% of the total load current as per the IEEE519-1992 specification. As a final check, the THD is calculated and verified to be under the maximum limit of 5%.

Power dissipation in damping resistor

In order to minimise the power losses in the damping resistor, it is important to establish the causes of the power dissipation in the resistor. The losses in the resistor are proportional to the square of the total current flow through it and the resistance. For the ease of analysis, it is possible to calculate the losses due to the switching harmonics and the fundamental frequency component separately and sum them. Therefore the losses due to the main switching harmonics in the resistor, P_{R_h} is given by equation (2-14) where $i_{inv}(h)$ and $i_g(h)$ are given in equations (2-10) and (2-11) respectively.

$$P_{R\_h} = \sum_{h=x}^{y} \left| i_{inv}(h) - i_g(h) \right|^2 R \qquad \textbf{(2-14)}$$

The losses due to the fundamental frequency component occur as part of the grid voltage is seen across the resistor and capacitor. By summing the voltages in loop 'A' of Fig. 2-13, the fundamental frequency component of the capacitor current can be written as shown in equation (2-15) (where I_g is the fundamental rms grid current given by P/V_g).

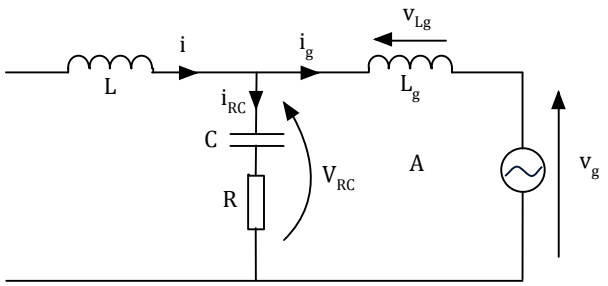


Fig. 2-13 Losses due to the fundamental component of capacitor current

$$i_{RC\_50Hz} = \frac{(j\omega_o L_g I_g + V_g) j\omega_o C}{(1 + j\omega_o RC)} \quad \textbf{(2-15)}$$

The power dissipation due to the fundamental voltage,

$$P_{R\_50Hz} = \left|i_{RC\_50Hz}\right|^2 R \quad \textbf{(2-16)}$$

Therefore total power loss in resistor,

$$P_{R\_total} = P_{R\_50Hz} + P_{R\_h} \quad \textbf{(2-17)}$$

2.2.1.3. Transformer design

Transformer equivalent circuit

For the purposes of circuit analysis and magnetic design, the equivalent circuit for the transformer is presented in Fig. 2-14. The equivalent circuit is made up of an ideal transformer combined with reactance components that models the electromagnetic attributes. The magnetising inductance L_m is in parallel with R_m that models the core losses. The winding resistances of the primary and secondary are R_1 and R_2 respectively. The secondary leakage inductance and winding resistance is referred to the primary side and are

denoted by L'_{l2} and R'_2 respectively and can be defined as shown in equations (2-18).

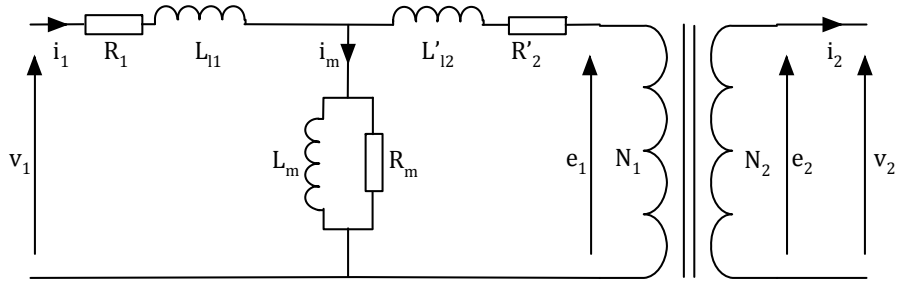


Fig. 2-14 Transformer equivalent circuit

$$L'_{l2} = \left(\frac{N_1}{N_2}\right)^2 L_{l2} \quad | \quad R'_2 = \left(\frac{N_1}{N_2}\right)^2 R_2 \tag{2-18}$$

The total leakage inductance can be defined by equation (2-19).

$$L_{l\_t} = L_{l1} + L'_{l2} \tag{2-19}$$

Selection of core material

The design criteria for the 50 Hz isolation transformer are weight, size and material cost optimisation. The first step in the design process is to select the material for the core of the transformer. There are two main varieties of magnetic core materials, which are alloy-based materials and ferrite-based materials. Alloy based materials have high conductivity compared with ferrite materials and therefore incur both hysteresis and eddy current losses. The advantage of alloy materials is the high saturation flux density and therefore smaller core size for a given flux density in comparison to ferrites [83].

The alloy-based materials are further subdivided into two main types of core, which are iron alloy materials and powdered iron. The iron alloy materials

are laminated into thin sheets and insulated from each other to reduce electrical conductivity. However, due to the relatively high conductivity, iron alloy cores cannot operate at high frequencies due to eddy current loss. In contrast, powdered iron cores have iron particles suspended in a material that electrically isolates them and therefore the conductivity is significantly less than that of iron alloy laminated cores. Therefore the powdered iron cores can operate at higher frequencies without significant eddy current losses. Ferrite materials on the other hand, have negligibly small conductivity and therefore only exhibit hysteresis losses and as a result are widely used for high frequency applications. However, ferrite materials generally have a low saturation flux density and therefore larger core sizes for a given flux density [83].

The following Table 2-4 presents a quantitative comparison of commonly available magnetic materials [84].

Table 2-4 Properties of commonly available magnetic materials [84]

Material	Max. Flux Density (T)	Resistivity (Ωcm)	Operating Frequencies
Fe	2.2	$1x10^{-5}$	50Hz - 1kHz
Si-Fe (unoriented)	2	$5x10^{-5}$	50Hz - 1kHz
Si-Fe (oriented)	2	$5x10^{-5}$	50Hz - 1kHz
50-50 Ni Fe (grain- oriented)	1.5	$4x10^{-5}$	50Hz - 1kHz
Kool Mu powder	1	-	<10MHz
Iron powder	1	$1x10^{4}$	100kHz - 100MHz
Ferrite (Mn-Zn)	0.3-0.5	10-100	10kHz - 2MHz
Ferrite (Ni-Zn)	0.3-0.5	$1x10^{6}$	200kHz - 100MHz

It can be seen that the material of choice for low frequency applications is laminated steel materials due to the high saturation flux density (B_{max}) which

allows for a smaller transformer size. Furthermore, grain oriented steel materials offers higher permeability and lower losses when the magnetic flux is in the direction of the orientation. Since eddy current losses increase at higher frequencies, materials that have higher resistivity (powder based and ferrite) is preferred for high frequency applications.

The core of the transformer is composed of two 'E' shaped core halves. The main material cost of the transformer in a production quantity is incurred from the copper cost for the windings and magnetic steel material cost for the core. Since the transformer operates at a frequency of 50 Hz, grain oriented Si-Fe (35M6) material is chosen as it offers a high saturation flux density (2 T) as well as reduced core losses as a result of the grain orientation.

Transformer Design

For optimisation of the transformer size, weight and efficiency, the design equations for the physical and magnetic properties are analysed after which an iterative process is used to determine the optimal number of turns for the transformer. The physical structure of the transformer core is illustrated in Fig. 2-15. C_w and W_w denote the core width and window width while the aspect ratios of the window and core are denoted by K_1 and K_2.

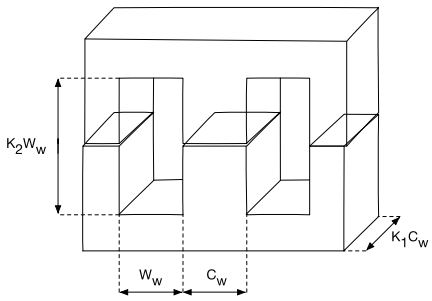


Fig. 2-15 Transformer core dimensions

The core area (A_{core}) is defined by equation (2-20) where I_{pk_1} is the peak primary current, V_{rms_1} the primary rms voltage and f the fundamental frequency. Therefore the required core width can be defined as shown in (2-21).

$$A_{core} = \frac{L_m I_{pk\_1}}{B_{max} N_1} = \frac{V_{rms\_1}}{4.44 f N_1 B_{max}} = K_1 C_w^2 \quad \textbf{(2-20)}$$

$$C_w = \sqrt{\frac{V_{rms\_1}}{4.44 f N_1 K_1 B_{max}}} \quad \textbf{(2-21)}$$

Similarly, the required window width can be defined by the following equation (2-22) where K_{cu} is the copper filling factor, W_{w1} the winding thickness and J is the maximum permissible current density.

$$A_w = K_2 W_{w1}^2 = \frac{I_{rms\_1} N_1 + I_{rms\_2} N_2}{K_{cu} J} = \frac{2 I_{rms\_1} N_1}{K_{cu} J} \quad \textbf{(2-22)}$$

In order to estimate the weight of copper and the resistance of each winding, the average length of wire in the bobbin must be defined as follows where h_b is the thickness of the bobbin and P_f is the packing factor.

$$l_{av} = 2(C_w + 2h_b)\left(1 + K_1/P_f\right) + \pi W_{w1} \quad \textbf{(2-23)}$$

The weight of the copper can be defined as (2-24) where A_{c_1} is the cross sectional area of the primary conductor as given in (2-25) and d_{cu} is the density of copper.

$$W_{cu} = 2 d_{cu} N A_{c\_1} l_{av} \quad \textbf{(2-24)}$$

$$A_{c\_1} = \frac{I_{rms\_1}}{J} \quad \textbf{(2-25)}$$

The resistance of the two windings can be defined as given in equation (2-26) where ρ_{cu} is the resistivity of copper.

$$R_1 = \frac{\rho_{cu} N l_{av}}{A_{cp}} \quad | \quad R_2 = \frac{R_1}{\left(\frac{N_1}{N_2}\right)^2} \quad \textbf{(2-26)}$$

To calculate the weight of the iron core, the volume of the core has to be derived by considering the geometrics, and multiplied by the density of iron (d_{iron}) and is defined as (2-27). Therefore the total weight of the transformer can be defined as (2-28).

$$W_{iron} = d_{iron} K_1 C_w^2 \left[(2K_2 + 1)W_w + C_w\left(1 + {}^{\pi}/_{4}\right)\right] \quad \textbf{(2-27)}$$

$$W_t = W_{cu} + W_{iron} \quad \textbf{(2-28)}$$

The next step is to calculate the magnetising inductance and this requires the definition of the average length of the magnetic path (l_{fe}) inside the core by considering the geometrics and is given in equation (2-29). The magnetising inductance is therefore defined as (2-30).

$$l_{fe} = 2(K_2 + 1)W_w + \frac{\pi C_w}{2} \quad \textbf{(2-29)}$$

$$L_m = \mu_0 \mu_r \frac{K_1 C_w^2 N_1^2}{l_{fe}} \quad \textbf{(2-30)}$$

For the calculation of efficiency, the power dissipated in the copper due to resistive losses and the power dissipated in the core due to hysteresis and

eddy current losses must be established as given in equations (2-31) and (2-32) where l_d is the specific loss for the material at 50 Hz (W/kg).

$$P_{cu} = 2R_1 I_{rms\_1}^2 \quad \textbf{(2-31)}$$

$$P_{iron} = l_d W_{iron} \quad \textbf{(2-32)}$$

Therefore, the efficiency of the transformer is defined as follows.

$$\eta = \frac{P_{out}}{(P_{out} + P_{cu} + P_{iron})} * 100 \quad \textbf{(2-33)}$$

The final step is the definition of the leakage inductance. The leakage inductance depends on the orientation of the primary and secondary windings. If the windings are wound on top of each other (overlapping), L_{l1} is given as in equation (2-34), however if the windings are made separately (top-bottom arrangement), L_{l1} is given as shown in (2-35).

$$L_{l1\_overlapping} = \frac{1}{3}\mu_0 N^2 \frac{1}{K_2} l_{av} \quad \textbf{(2-34)}$$

$$L_{l1\_top\_botton} = \frac{1}{3}\mu_0 N^2 \frac{K_2}{1} l_{av} \quad \textbf{(2-35)}$$

It can be observed that for K_2>1, which is the standard configuration, a top bottom winding gives a larger value of leakage inductance. Therefore for the purposes of integrating the converter side inductance into the transformer, it is beneficial to utilise the top-bottom arrangement.

The procedure for designing the transformer consists of calculating the minimum required winding width for a given number of turns (N1) by considering the maximum permissible current density for the associated

winding width according to Table 2-5 and equation (2-22) considering a common set of design parameters as given in Table 2-6. The required core width in order to be below the maximum permitted flux density is calculated from equation (2-21). Thereafter, the associated leakage inductance, total weight and efficiency are also calculated. This process is done for a range of N1 values (100 turns to 240 turns).

Table 2-5 Winding width vs. maximum allowable current density

J (A/mm²)	7.00	4.85	3.5	2.55	2.00	1.85
Ww1 (mm)	10	20	30	40	50	60

The calculated values of leakage inductance, weight and efficiency as a function of N1 are plotted in Fig. 2-16 based on equations (2-28), (2-33) and (2-35) where the common set of parameters that were used are presented in Table 2-6.

Table 2-6 Transformer design parameters

Parameter	**Symbol**	**Value**
Primary voltage	V_{rms_1}	230 V (50 Hz)
Secondary voltage	V_{rms_2}	57.5 V (50 Hz)
Output power	P_{out}	2200 W
Power factor	PF	0.9
Maximum permissible flux density	B_{max}	1.5 T
Specific iron loss at 50 Hz	L_d	3 W/kg
Aspect ratio of core	K_1	1
Aspect ratio of coil window	K_2	2
Thickness of bobbin	h_b	1 mm
Copper filling factor	K_{cu}	0.5
Packing factor	P_f	0.96
Relative permeability at B_{max}	μ_r	500

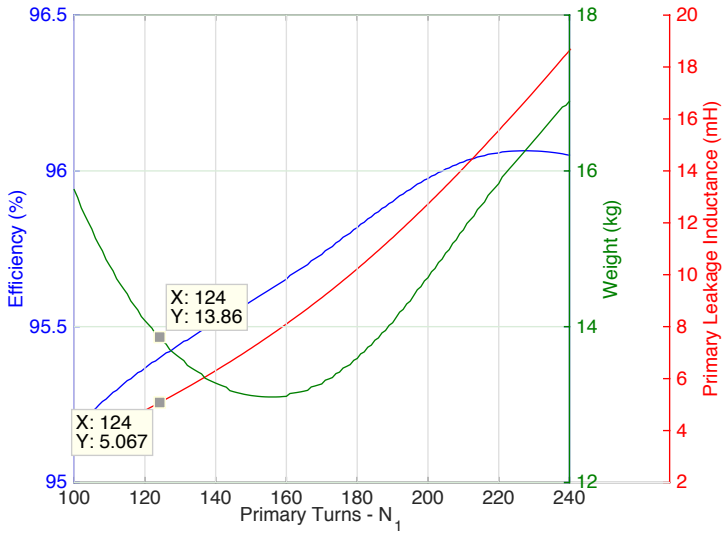


Fig. 2-16 Leakage inductance, weight and efficiency vs. number of primary turns for top-bottom winding arrangement

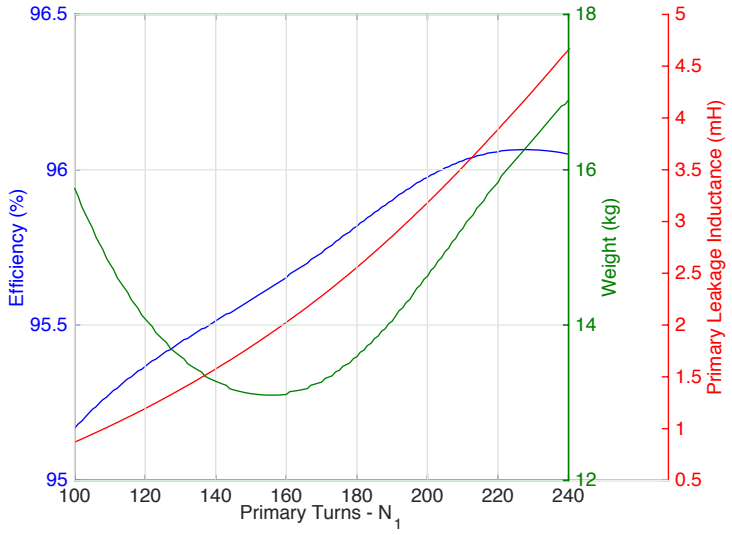


Fig. 2-17 Leakage inductance, weight and efficiency vs. number of primary turns for overlapping winding arrangement

The number of turns must be selected considering the compromise between leakage inductance, weight and efficiency. In section 2.2.1.1 it was determined that the maximum primary side leakage inductance should be under 7.2 mH and therefore, 70% of the maximum (5 mH) was chosen as a

transformer design specification to allow for operation under weak grid conditions.

It can be seen from Fig. 2-16 and Fig. 2-17 that the top-bottom winding arrangement gives a leakage inductance value closer to the required 5 mH while minimising weight whereas the overlapping arrangement provides a much smaller value. Therefore, a value of 124 turns is selected for N_1 with a top-bottom arrangement and this yields a primary leakage inductance of 5 mH (for a total primary referred leakage inductance of 10 mH) as per the design target specified in 2.2.1.1 and a total transformer weight of 13.86 kg. The final parameters of the designed transformer are presented in Table 2-7.

Table 2-7 Final transformer design parameters

Parameter	Symbol	Value
Primary/secondary turns	N_1/N_2	124/31
Output power	P_{out}	2200W
Turns ratio	N	4
Core material	-	35M6 / EE core
Primary/secondary winding diameter	A_{cp1} / A_{cp2}	1.85 mm / 3.7 mm
Core width x core length	C_w x K_1C_w	74.9 mm x 74.9 mm
Window width x window length	W_w x K_2W_w	27 mm / 54 mm
Primary/secondary leakage inductance	L_{l1} / L_{l2}	5 mH / 312.5 µH
Primary side magnetising inductance	L_m	190 mH
Current density	J	1.97 A/mm^2
Total weight	W_t	13.86 kg
Efficiency	η	95.4%

Since the actual value of magnetising inductance is 190 mH (the assumption in section 2.2.1.1 was 250 mH), it is possible to verify that a magnetising inductance of 190 mH still satisfies the maximum series inductance

value. By using equations (2-2) and (2-3), it is observed that the maximum primary leakage inductance corresponding to L_m=190 mH is 6.1 mH, or total leakage inductance of 12.2 mH. Therefore the transformer that was designed, and the resulting LCL filter meet the maximum series inductance constraints.

Practical Measurement of Leakage Inductance

Although the transformer was designed to have a total leakage inductance value of 10 mH, in reality, at high frequencies, the leakage inductance typically reduces due to eddy current and proximity effects [85].

Therefore, the leakage inductance variation with frequency of the transformer that was built has been characterised as depicted in Fig. 2-18 with the use of an impedance analyser. It can be observed from the figure that the total leakage inductance has reduced from 10.42 mH at 50 Hz, to 4.98 mH at 20 kHz. Furthermore it can be seen that, the series resistance increases significantly due to skin and proximity effects.

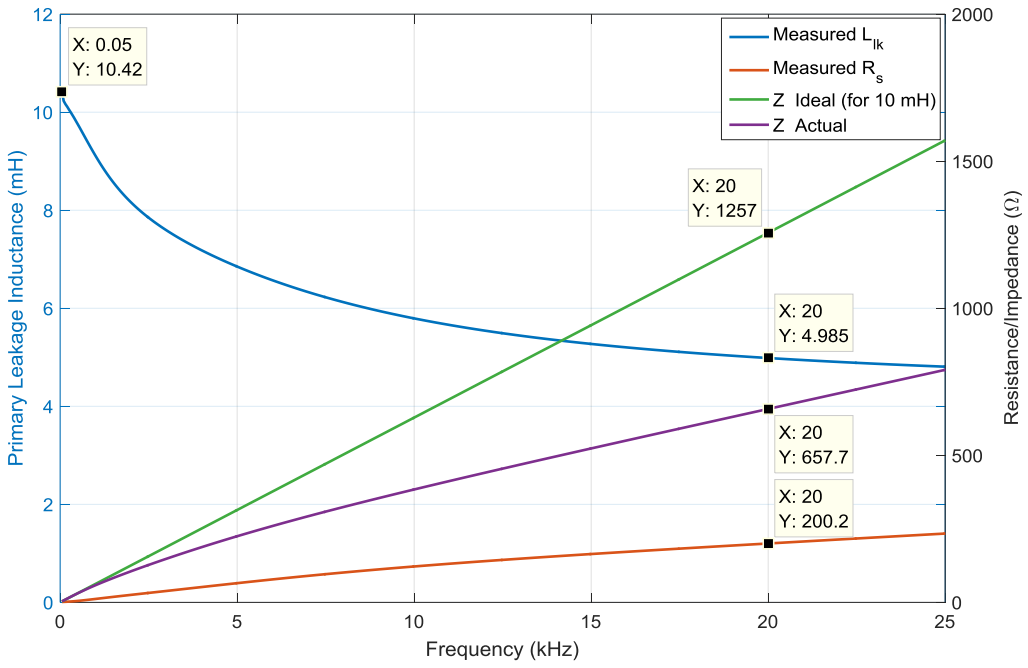


Fig. 2-18 Measured primary leakage inductance, primary series resistance, ideal and actual series impedance of the practical transformer

Even with the increased series resistance, the resulting practical value of series impedance at 20 kHz is short of the 1.25 kΩ that would be present if the leakage inductance were to remain at the ideal value of 10 mH at 20 kHz.

Therefore, the LCL filter design and optimisation presented in the following section considers the reduced value of primary referred leakage inductance (~5 mH) that is provided by the transformer.

2.2.1.4. *Selection of L_g and R for harmonic suppression and minimising power loss*

As the equations governing grid current distortion and power loss in the resistor have been established, the possible combinations of L_g and R for optimal size and efficiency can be analysed.

Fig. 2-19 illustrates the variation of worst-case high frequency grid current distortion (the dominant harmonic component is determined by evaluating ±4 grid current sideband components around the 20 kHz carrier) as a function of L_g and damping resistance for a converter side inductance of 5 mH and filter capacitance of 6.8 μF. As expected, lower values of L_g reduce the effectiveness of the filter. It can be noted that larger values of damping resistance also degrades filter performance. Furthermore, Fig. 2-20 shows the variation of resistor power dissipation as a function of L_g and R, and it is apparent that larger values of R significantly reduce efficiency. Therefore it follows that the smallest value of L_g that meets the IEEE519 standard must be chosen whilst selecting the minimum value of resistance possible, which provides sufficient damping at the resonant frequency. A minimum margin of 10% is considered for the distortion limit given in IEEE519 which corresponds to a current distortion lower than 0.27%. Therefore the value for L_g is chosen as 0.145 mH, and R is selected to be 1.2 Ω. The selected components reduce the maximum distortion to 0.25%, the THD to 0.36%, and cause a dissipation of 0.46 W in the resistor, which is acceptable for the design criteria. Therefore, a

resistor with a 1 W rating is selected in order to account for the power derating at high temperatures. The next step is to ensure that the selected parameters for the LCL filter provide the expected transfer function with sufficient damping so as to ensure stable operation. The Bode plot presented in Fig. 2-21 indicates the filter response as a function of damping resistance for $L = 5\,mH$, $L_g = 0.145\,mH$ and $C = 6.8\,\mu F$. The damping provided by the resistor must be sufficient in order to prevent oscillations at the resonant frequency of the filter. Therefore, the closed loop gain of the system at the LCL resonant frequency (5.14 kHz) must be below 0 dB for stability. With the selected resistance value of 1.2 Ω, and using the current controller closed loop transfer function given in (3-18) in Chapter 3, it is found that the gain at the LCL resonant frequency is -8.8 dB and is therefore suitable for the application.

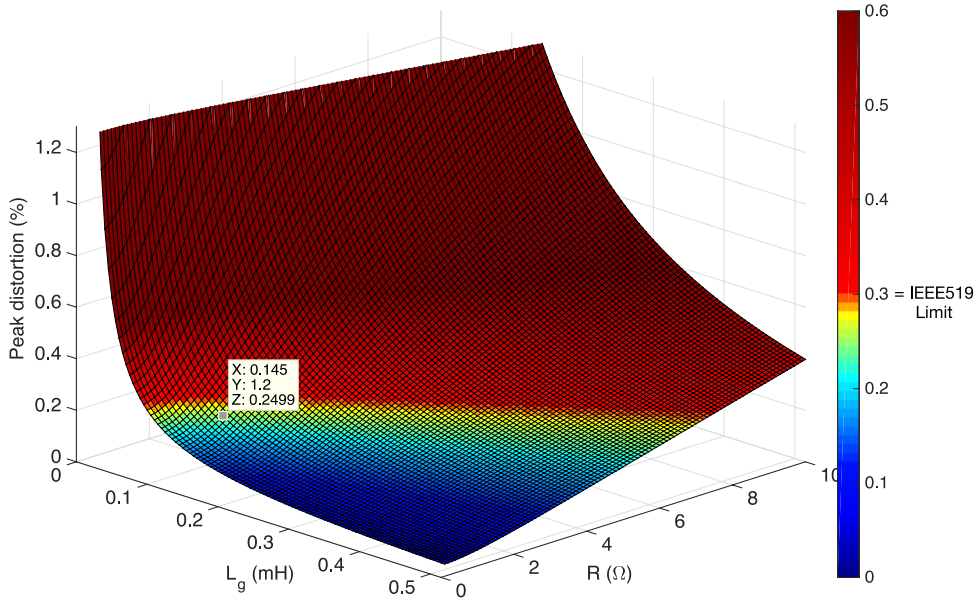


Fig. 2-19 Peak grid current distortion vs. L_g vs. R (L = 5 mH, C = 6.8 µF)

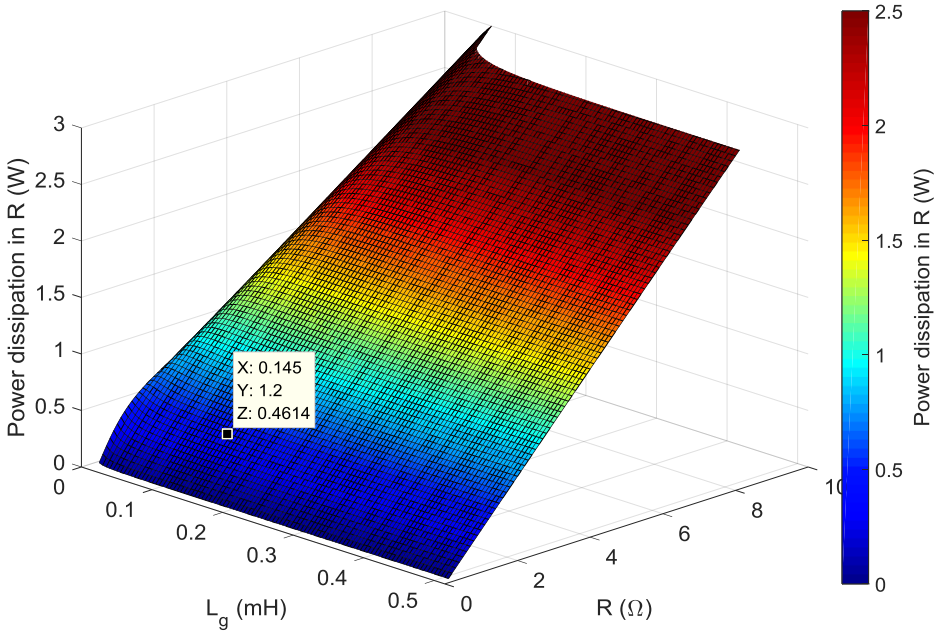


Fig. 2-20 Damping resistor power dissipation vs. L_g vs. R (L = 5 mH, C = 6.8 µF)

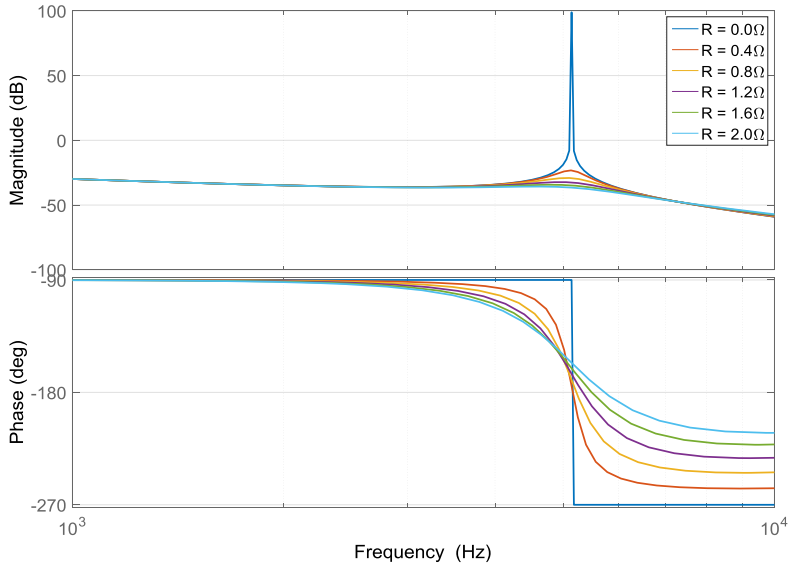


Fig. 2-21 Bode plot of filter response as a function of damping resistance (L = 5 mH, L_g = 145 µH, C = 6.8 µF)

Fig. 2-22 shows the variation of resistor power dissipation as a function of resistance and filter capacitance with $L = 5\ mH$ and $L_g = 0.145\ mH$. It can be

observed that with larger values of capacitance, the dissipation increases. This is mainly attributed to losses due to the fundamental frequency component.

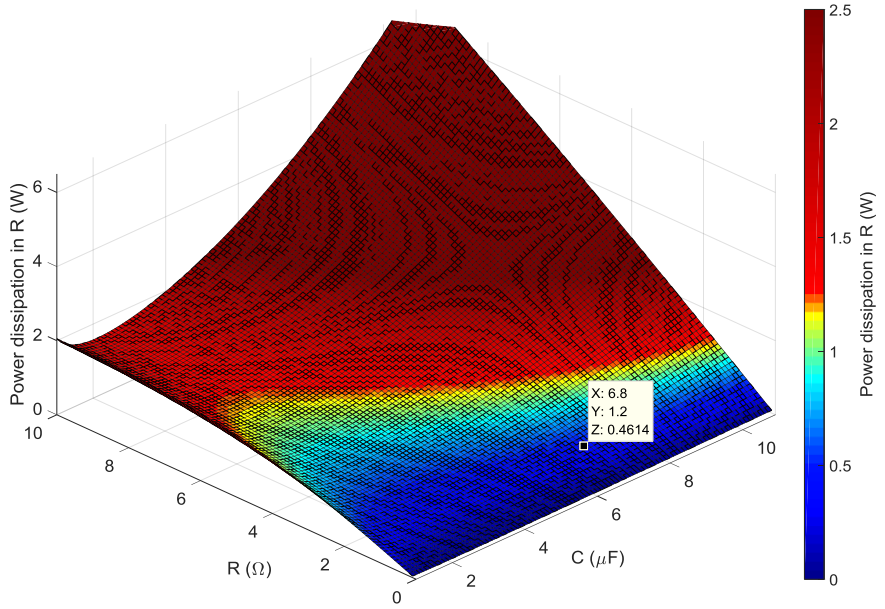


Fig. 2-22 Damping resistor power dissipation vs. R vs. C (L = 5 mH, Lg = 145 μH)

The resonance frequency of the filter is given by equation (2-36). For the LCL filter with the parameters that were selected, the resonant frequency is 5.14 kHz, which is less than half of the VSC switching harmonic frequency (harmonic frequency is double the switching frequency, therefore 20 kHz).

Table 2-8 summarises the final component values of the LCL filter.

$$f_r = \frac{1}{2\pi}\sqrt{\frac{L_g + L}{L_g LC}} \qquad \textbf{(2-36)}$$

Table 2-8 Summary of LCL filter component values

Parameter	Value
Converter side inductance (transformer total leakage inductance)	5 mH
Grid side inductance	145 µH
Capacitance	6.8 µF
Damping resistance	1.2 Ω
Filter resonant frequency	5.14 kHz

2.2.1.5. Sensitivity analysis of LCL filter to component tolerance and temperature

The LCL filter characteristics are dependent on any variations of component values due to component manufacturing tolerances as well as temperature induced variations. The sensitivity of the LCL filter to variations in the capacitance and damping resistance will be analysed.

Metal film resistors are available in ±5% manufacturing tolerance and it is common for manufacturers to specify the temperature coefficient in the range of ±200 ppm/°C to ±400 ppm/°C. Similarly, polypropylene film capacitors are commonly available in ±10% manufacturing tolerance and the typical temperature coefficient is -200 ±100 ppm/°C where the reference capacitance is specified for 20°C [86].

Therefore for the sensitivity analysis, it is assumed that the capacitor and resistor have manufacturing tolerances of ±10% and ±5% respectively and a temperature coefficient of -300 ppm/°C for the capacitor and ±400 ppm/°C for the resistor. Furthermore, the temperature range for the sensitivity analysis is (-55°C to 125°C) and (-55°C to 100°C) for the resistor and capacitor respectively. The higher temperature range for the resistor is considered as the resistor dissipates power under normal operation (the capacitor's power

dissipation due to the equivalent series resistance is negligible for polypropylene film capacitors in the LCL filter application).

The range of component value variation due to manufacturing tolerance and temperature can be quantified by considering the combination of the worst case manufacturing error along with the worst case temperature scenario. Therefore for the capacitor, the minimum and maximum capacitance values are 6 μF and 7.65 μF respectively and for the resistor, the minimum and maximum resistance values are 1.09 Ω and 1.31 Ω respectively.

LCL filter transfer function

The LCL filter characteristics (from equation (2-12)) for minimum and maximum capacitance and resistance combinations are presented in Fig. 2-23. It can be seen that the capacitance variation causes a shift in the resonant frequency as can be expected from equation (2-36) whereas the resistance variation causes deviation in the damping. The resonant frequency varies from 4.84 kHz to 5.47 kHz which is acceptable for the application as it is lower than half the VSC harmonic frequency of 20 kHz. Similarly, the closed loop gain of the current controller (discussed in Chapter 3) for the worst case damping (R = 1.09 Ω and C = 7.65 μF) at the resonant frequency of the LCL filter is -8.2 dB and is therefore adequately damped for stable operation.

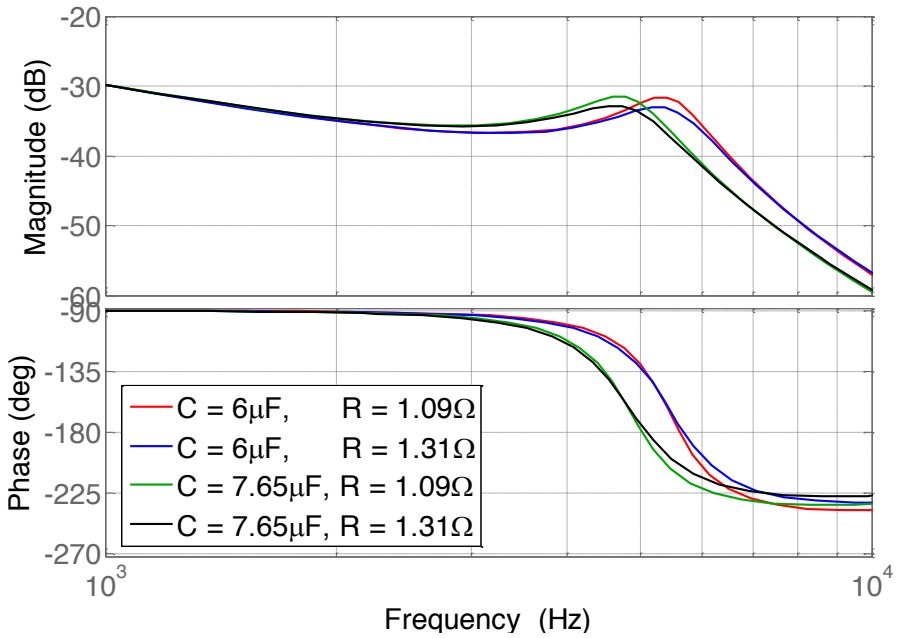


Fig. 2-23 LCL filter responses for capacitance and resistance variation

Grid current distortion

The following Fig. 2-24 depicts the variation of the peak high frequency grid current distortion over the LCL capacitor and damping resistor component variation range.

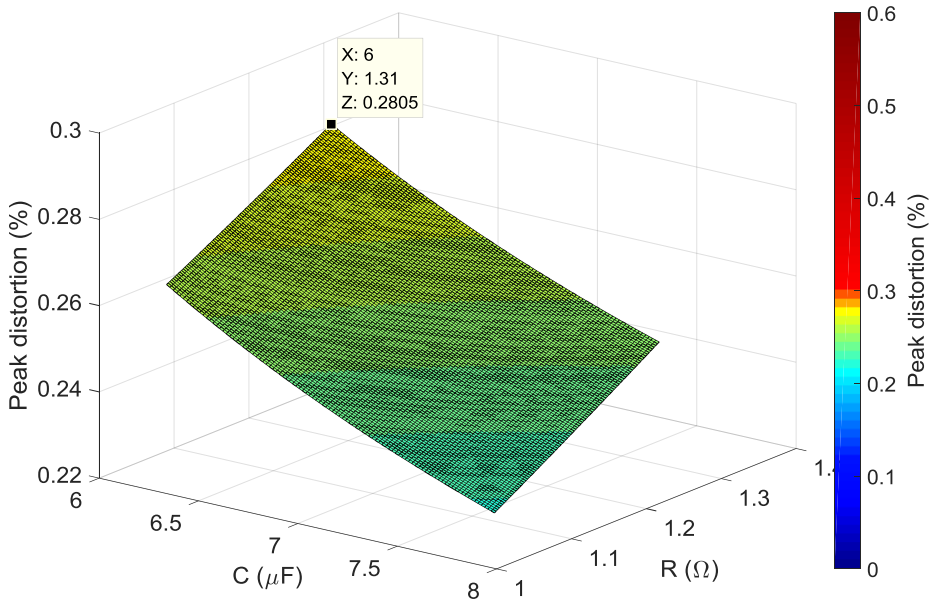


Fig. 2-24 Peak grid current distortion vs. C and R component variation (C: 6μF to 7.65μF, R: 1.09 Ω to 1.31 Ω)

It can be observed that the maximum value of peak current distortion is 0.28% and therefore the LCL filter design meets the IEEE519 current distortion limit of 0.3% over the operating temperature and manufacturing tolerance of the capacitor and damping resistor.

Power dissipation in damping resistor

The sensitivity of the power loss in the damping resistor due to the LCL capacitor and damping resistor component variation is presented in Fig. 2-25. It can be seen that the maximum power dissipation due to component variation is 0.58 W (in contrast to the 0.46 W estimated for ideal component values at 20°C). Therefore, the selected power rating of 1 W is suitable for the LCL filter.

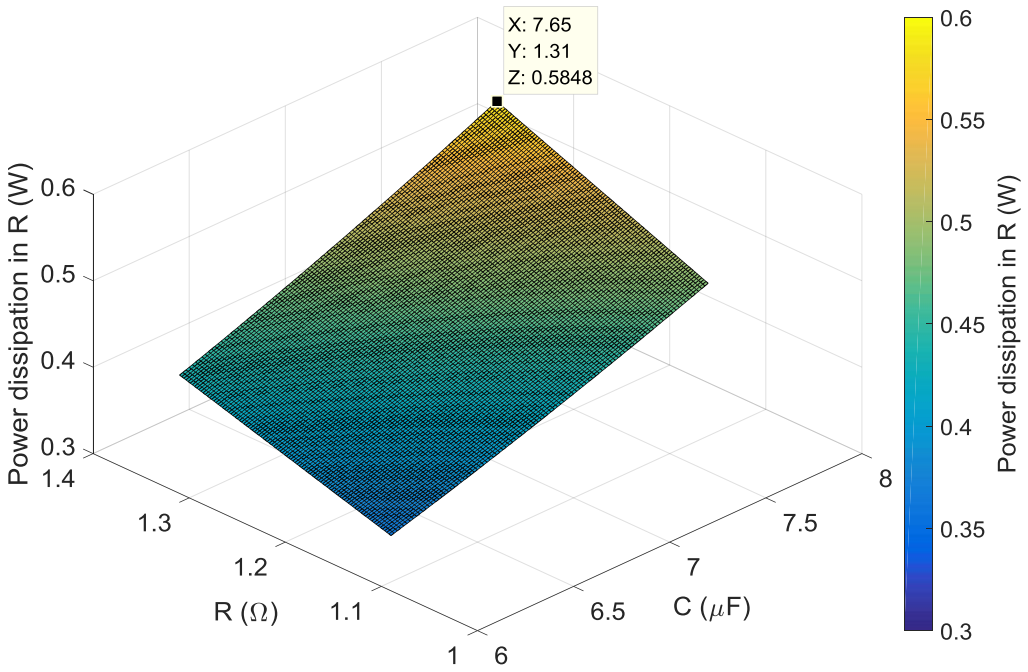


Fig. 2-25 Damping resistor power dissipation vs. C and R component variation (C: 6µF to 7.65µF, R: 1.09 Ω to 1.31 Ω)

2.2.1.6. Grid side inductor design

The design of the grid side inductor follows a similar approach to the transformer design. Fig. 2-26 illustrates the arrangement of the 2 core halves of the inductor, which has an air gap of l_g.

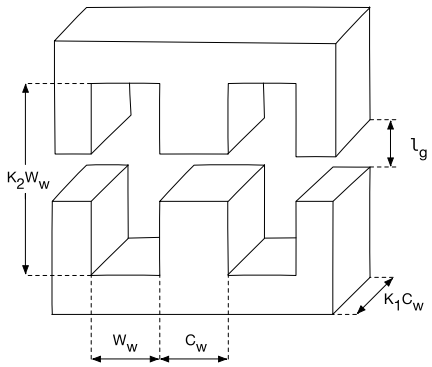


Fig. 2-26 Inductor core dimensions

It is possible to plot the inductance, required core area and total weight of the inductor as a function of N as illustrated in Fig. 2-27. The core material selected was grain oriented silicon steel material as it offers a high B_{max} and therefore results in a smaller and lighter inductor relative to ferrite material.

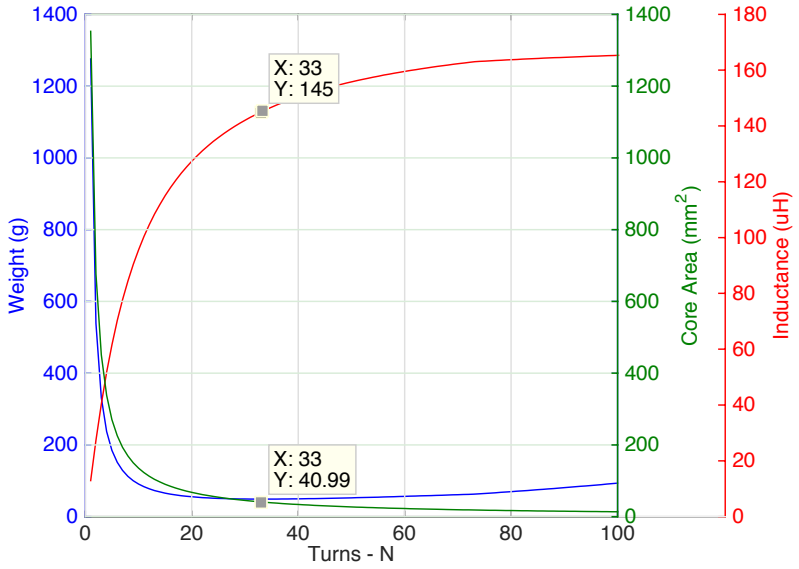


Fig. 2-27 Inductance, weight and required core area vs. number of turns

The grid side inductance was specified in section 2.2.1.4 as 145 µH. Therefore the following table highlights the parameters of the inductor that was designed using analytical equations in MATLAB.

Table 2-9 Summary of inductor design parameters

Parameter	Symbol	Value
Inductance	L	145 µH
Turns	N	33
Power rating	P	2200 W
Core material	-	35M6 / EE core
Winding diameter	A_{cp}	1.32 mm
Air gap	l_g	0.16 mm
Core width x core length	C_w x K_1C_w	6.4 mm x 6.4 mm
Window width x window length	W_w x K_2W_w	11 mm / 22 mm
Copper weight	W_{cu}	27.6 g
Core weight	W_{fe}	21.2 g
Total weight	W_t	48.9 g
Efficiency	η	99.88%

2.3. High frequency transformer based bidirectional charger

2.3.1. Frontend analysis and design

2.3.1.1. Frontend filter design considerations

The design procedure for the frontend filter for the high frequency DAB based system is similar to that of the LFT system. The main difference is the use

of 2 discrete inductors in the HF converter as opposed to a single inductor and the use of the leakage inductance of the transformer in the LFT system.

Design constraints of LCL filter

When designing the filter, there are a number of constraints to the selection of components, the first being the maximum allowable series inductance to the grid. The DC link voltage, normal grid voltage range and the maximum grid current determine the maximum allowable inductance. If the V2G mode is considered, the phasor diagram presented in Fig. 2-28 represents the relationship between the grid voltage (V_g), converter output voltage (V_a) which is related to the DC link voltage, modulation index, and the voltage on the inductor for a given grid current (i_g) assuming unity power factor.

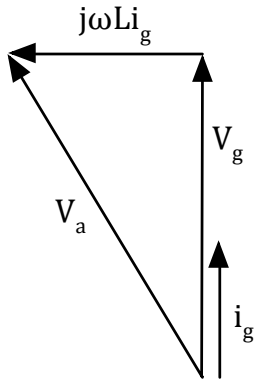


Fig. 2-28 Phasor diagram of frontend

$$V_a = \sqrt{V_g^2 + \left(j\omega L i_g\right)^2} \leq \frac{V_{dc}}{\sqrt{2}} = V_{max} \qquad \textbf{(2-37)}$$

$$L \leq \frac{V_g}{P_o \omega} \sqrt{V_{max}^2 - V_g^2} = L_{max} \qquad \textbf{(2-38)}$$

However, the peak value of the converter output voltage, V_a is less than or equal to the DC bus voltage. Therefore, the maximum value of the series inductance that allows the flow of power can be determined by (2-37) and (2-38).

When the supply voltage (V_g) variation of 230 V +10%, -6% (according to UK legislation [87]) and the DC link voltage of 380 V±10 V (ripple) is considered with a converter dead-time of 2%, the worst case L_{max} can be observed from the following Fig. 2-29. It can be seen that the worst case occurs when the grid input voltage is at the maximum and V_{dc} at its minimum. Therefore, the maximum series inductance of the LCL filter is 15.23 mH.

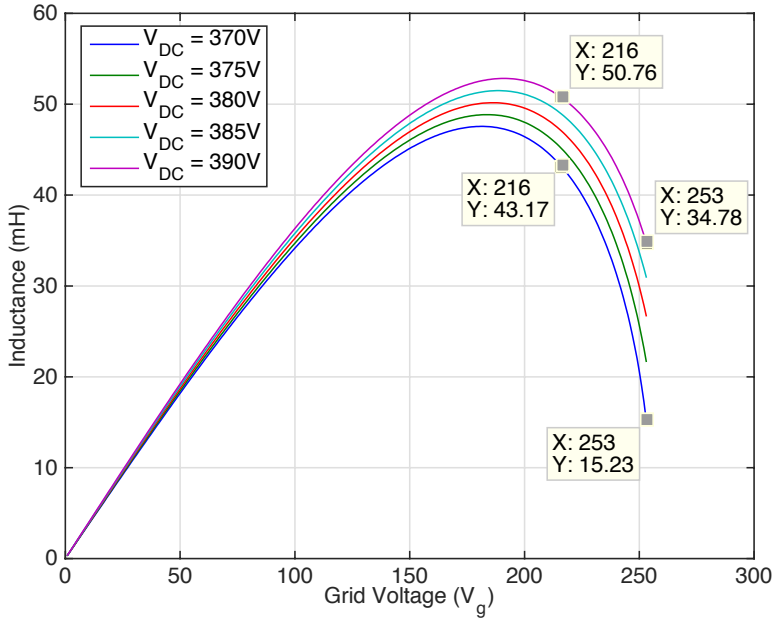


Fig. 2-29 Maximum series inductance vs. grid voltage for different values of DC link voltage

2.3.1.2. Optimal LCL filter design

The converter side inductor is first determined by selecting a value that will reduce the switching current ripple by 10% as proposed by [79]. Hence, the converter side inductance is defined by equation (2-39) where V_{inv_sum} is the rms of the sum of dominant harmonic voltages (h=399, 401).

$$L = \frac{v_{inv\_sum}}{\omega_{sw}\left(P_o/V_g\right) * 0.1} = 1.2\ mH \qquad \textbf{(2-39)}$$

The same value (6.8 µF) of filter capacitance to the LFT converter is selected since the base capacitance (Z_b) of both converters is the same value. The acceptable zone of current distortion as a function of L_g and damping resistance (R) is depicted in Fig. 2-30 for converter side inductance of 1.2 mH and filter capacitance of 6.8 µF. Hence, a grid side inductance of 300 µH and a damping resistance of 0.7 Ω are chosen as the remaining component values of the LCL filter in order to reduce the current distortion below 10% of the IEEE519 limit (it is assumed that the 4.4% difference in maximum current distortion between the LFT and HFT based charger systems does not affect the design comparison significantly). The chosen filter parameters results in a THD of 0.37% which acceptable as it is below the 5% limit. Furthermore, Fig. 2-31 and Fig. 2-32 illustrates the effect of the component values on the power dissipation in the damping resistor and provides an insight into the selection of the power rating for the device. Therefore, a resistor with a 2 W rating is selected in order to account for the power derating at high temperatures.

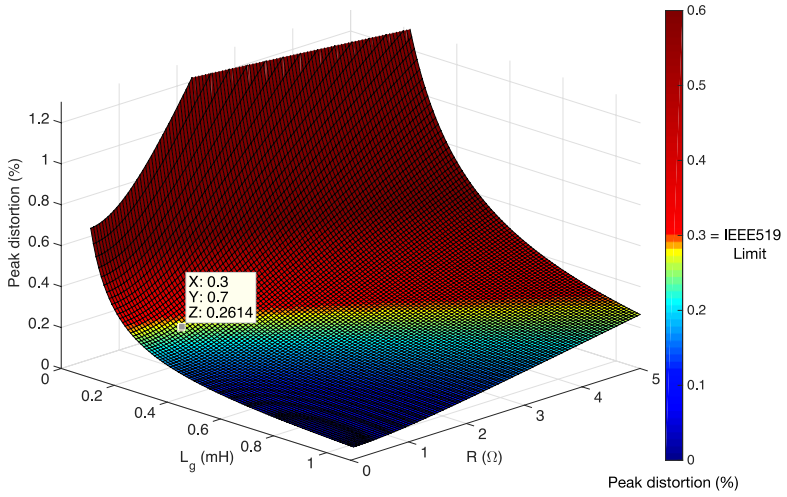


Fig. 2-30 Peak grid current distortion vs. Lg vs. R (L = 1.2 mH, C = 6.8 µF)

The final step is to ensure the damping resistance selected provides sufficient damping. Fig. 2-33 shows the Bode plots of the LCL filter for different values of damping resistance for the selected inductance and capacitance values. Furthermore, by evaluating the closed loop transfer function of the current controller (3-18) at the resonant frequency of the filter (3.94 kHz), it is found that the damping provided by the resistor is suitable for the application as the gain is -4 dB. The summary of the selected components is given in Table 2-10.

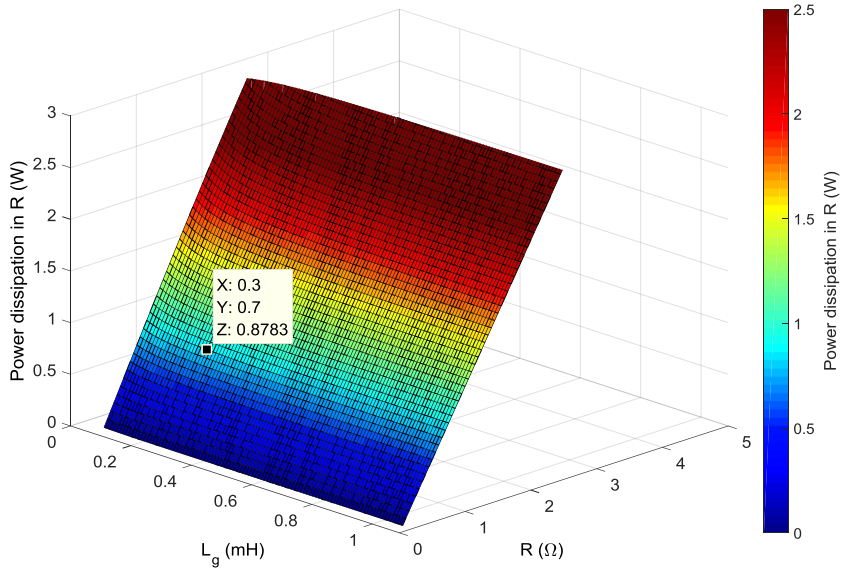


Fig. 2-31 Damping resistor power dissipation vs. Lg vs. R (L = 1.2 mH, C = 6.8 µF)

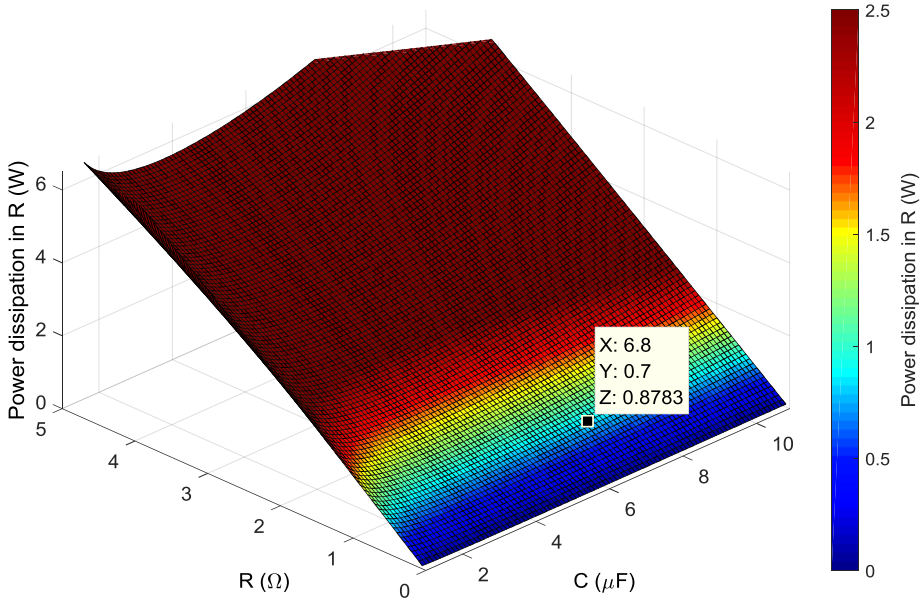


Fig. 2-32 Damping resistor power dissipation vs. R vs. C (L = 1.2 mH, Lg = 0.3 mH)

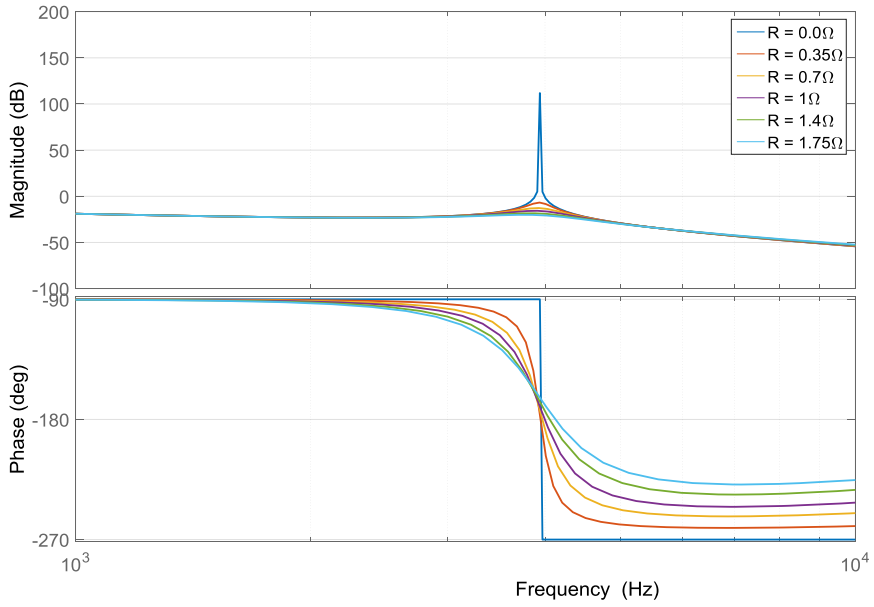


Fig. 2-33 Bode plot of filter response as a function of damping resistance (L = 1.2 mH, Lg = 0.3 mH, C = 6.8 μF)

Table 2-10 Summary of LCL filter component values

Component	Symbol	Value
Converter side inductor	L	1.2 mH
Grid side inductor	L_g	300 µH
Filter capacitor	C	6.8 µF
Damping resistor	R	0.7 Ω

2.3.1.3. Sensitivity analysis of LCL filter to component tolerance and temperature

The sensitivity analysis for the HFT based system follows the same method as was for the LFT based system. The capacitance range considered for the sensitivity analysis is 6 µF to 7.65 µF and the resistance range is 0.63 Ω to 0.76 Ω.

LCL filter transfer function

The LCL transfer functions (from equation (2-12)) over the capacitor and resistor variation are presented in Fig. 2-34. The variation of the resonant frequency is 3.71 kHz to 4.19 kHz and therefore is acceptable for the application as the frequency is less than half the VSC's harmonic frequency of 20 kHz. Furthermore, the closed loop gain of the current controller (discussed in Chapter 3) at the LCL resonant frequency for the worst case damping (R = 0.63 Ω and C = 7.65 µF) is -2.95 dB and is therefore adequate as it is below 0 dB.

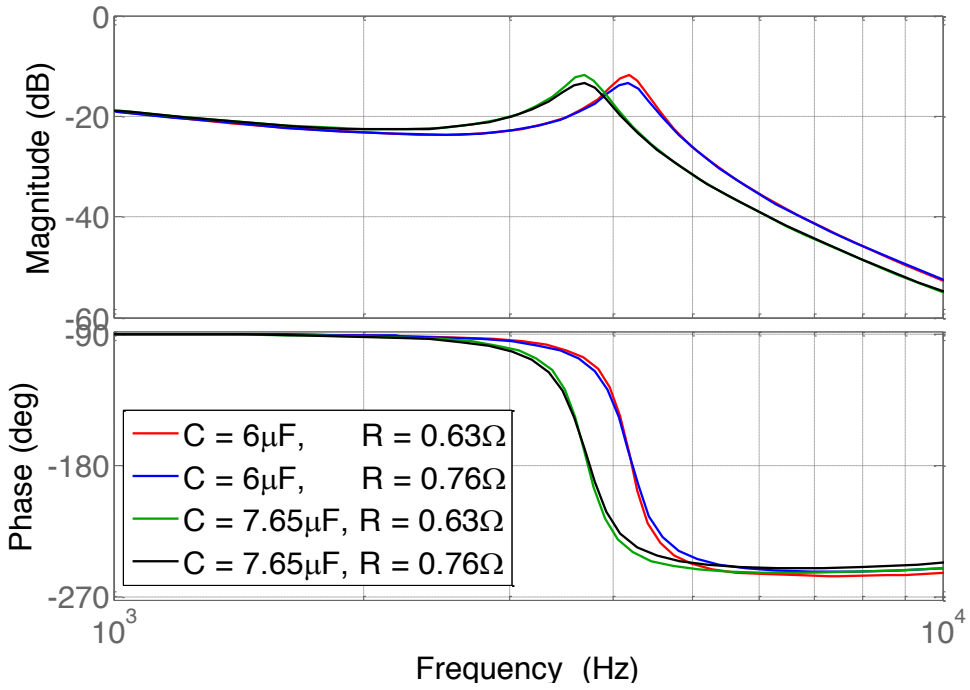


Fig. 2-34 Sensitivity analysis of LCL filter to component tolerance and temperature

Grid current distortion

The following Fig. 2-35 depicts the variation of the peak high frequency grid current distortion over the LCL capacitor and damping resistor component variation range.

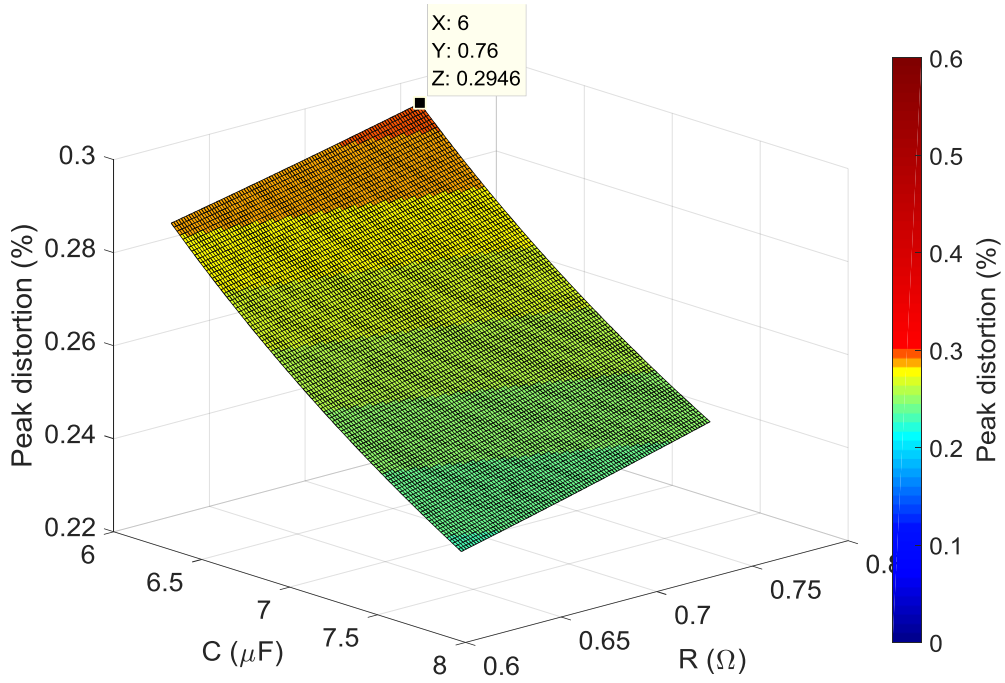


Fig. 2-35 Peak grid current distortion vs. C and R component variation (C: 6μF to 7.65μF, R: 0.63 Ω to 0.76 Ω)

It can be observed that the maximum value of peak current distortion is 0.29% and therefore the LCL filter design meets the IEEE519 current distortion limit of 0.3% over the operating temperature and manufacturing tolerance of the capacitor and damping resistor.

Power dissipation in damping resistor

The sensitivity of the power loss in the damping resistor due to the LCL capacitor and damping resistor component variation is presented in Fig. 2-36. It can be seen that the maximum power dissipation due to component variation is 1 W (in contrast to the 0.88 W estimated for ideal component values at 20°C). Therefore, the selected power rating of 2 W is suitable for the LCL filter.

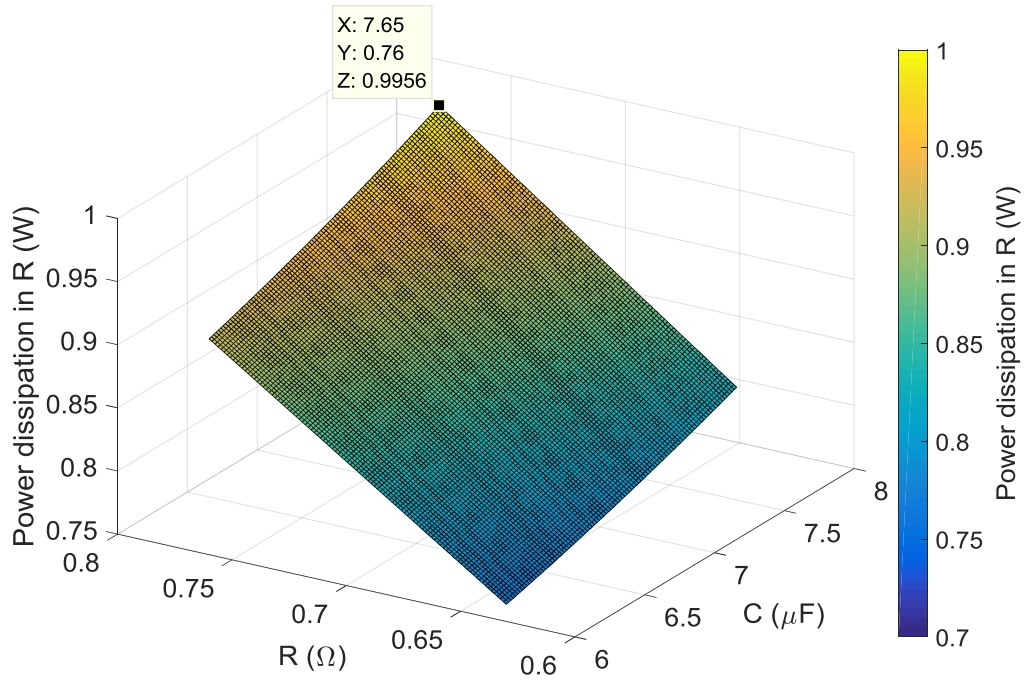


Fig. 2-36 Damping resistor power dissipation vs. C and R component variation (C: 6μF to 7.65μF, R: 0.63 Ω to 0.76 Ω)

2.3.1.4. Converter and grid side inductor design

The inductor design procedure follows the same process as described in – 2.2.1.6 and the resulting plots for the grid side inductor and converter side inductor are depicted in Fig. 2-37.

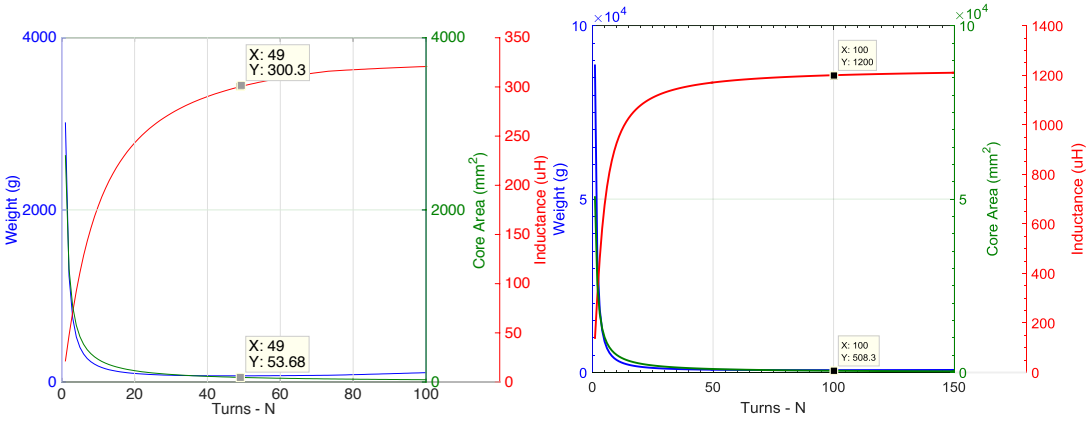


Fig. 2-37 Inductance, weight and required core area vs. number of turns for L_g (left) and L (right)

Since the harmonic current magnitude through the converter side inductor is much larger than the grid side inductor, and therefore to minimise core losses, a ferrite core for the converter side inductor is used. To minimise the weight and size of the grid side inductor, a core material of laminated grain oriented silicon steel is used. Hence the parameters of the two inductors that were designed for the LCL filter are summarised in Table 2-11.

Table 2-11 Summary of inductor design parameters

Parameter	Value (for L_g)	Value (for L)
Inductance	300 µH	1.2 mH
Turns	49	100
Power rating	2200 W	2200 W
Core material	35M6 / EE core	3C90 / E71 core
Winding diameter	1.32 mm	1.56 mm
Air gap	0.23 mm	3.49 mm
Core width x core length	7.33 mm x 7.33 mm	22 mm x 32 mm
Window width x window length	11 mm / 22 mm	13 mm / 43.8 mm
Copper weight	43.3 g	387 g
Core weight	28.5 g	520 g (E71)
Total weight	71.8 g	907 g
Efficiency	99.81%	98.94%

2.3.1.5. DC link capacitor sizing

The power flow from the grid to the DC link contains an AC component whose frequency is twice of that of the grid voltage (100 Hz). This AC component has to be bypassed through the DC link capacitor bank. The size of the capacitors is determined primarily by the ripple current capability of the DC link capacitors. The size of each capacitor and number of capacitors must be chosen to meet the 100 Hz ripple current requirement with a margin (a

minimum margin of 20% is chosen for the design) to ensure reliability. Since electrolytic capacitors' operational lifetime is dependent on temperature and therefore amount of ripple current, it is common practice to oversize the capacitors. Furthermore, the DC link voltage ripple under rated conditions is also evaluated afterwards to ensure the ripple is acceptably small. The ripple current of the capacitors is defined as given in (2-40) where the nominal power is denoted by P, and the DC-link voltage by V_{dc}. The DC link ripple current for the HF charger is therefore 4.1 A.

$$I_{rp\_rms} = \frac{P}{\sqrt{2}V_{dc}} = 4.1\ A \qquad \textbf{(2-40)}$$

Table 2-12 DC link capacitor parameters

Parameter	Value
Manufacturer	Cornell Dubilier
Part number	SLPX471M450H9P3
Capacity per component	470 µF
Quantity (parallel)	2
Total capacity	940 µF
Voltage rating	450 V
Ripple rating rms @ 85°C	2.8 A
Total ripple rating rms @ 85°C (x2)	5.6 A
ESR of 2 parallel capacitors	0.28 Ω

For the HF system, two 470 µF capacitors are chosen since it is more cost effective to have two or more capacitors with lower ripple current ratings than a single capacitor with a high current ripple rating. The parameters of the capacitors are given in Table 2-12. The DC link voltage ripple magnitude

(V_{dc_rp}), is defined as given in (2-41) where ω_o is the grid angular frequency [88]. Hence, the magnitude of the DC link ripple voltage of the system is calculated to be 9.8 V. Since the peak-to-peak voltage ripple is ~5% of the nominal DC link voltage, the DC link capacitance is deemed suitable.

$$V_{dc\_rp} = \frac{P}{2\omega_o V_{dc} C} \quad \textbf{(2-41)}$$

Since the ESR/ESL of electrolytic capacitors are relatively large, polypropylene film capacitors are also used on the DC link which are placed near the H-bridge MOSFET devices in order to provide a low impedance path for the high frequency current ripple that arises due to the PWM modulation. Two Panasonic 4.7 µF film capacitors (ECW-FD2W475J) are selected which provides a total of 11.6 A of rms ripple current capability at 20 kHz.

However, in the experiment setup, a larger value of DC link capacitance (2500 µF) was used in order to increase the reliability of the prototype system as the extra capacitors provides increased ripple current capability. It can be expected that the increased value of capacitance for the experiment setup will lead to a reduction in 100 Hz ripple voltage in the DC link from 9.8 V to 3.7 V.

2.3.2. Dual active bridge analysis and design

In this section, the fundamentals of DAB converter operation are analysed and the converter specifications are presented.

The DAB converter consists of 8 power electronic switches in a dual H-bridge configuration with a transformer in the centre. DAB topology is presented in Fig. 2-38.

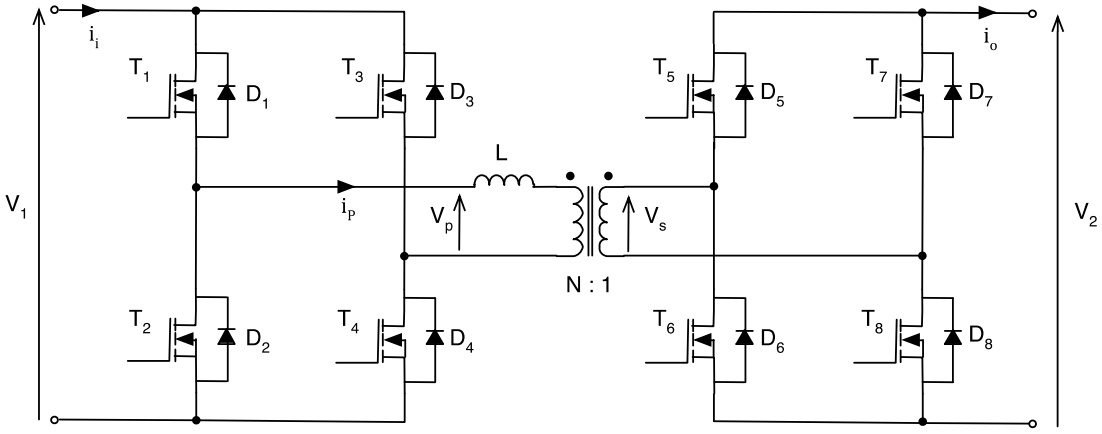


Fig. 2-38 Dual active bridge (DAB) topology

2.3.2.1. DAB Converter modulation methods

There are a number of modulation methods that have been reported [89-97] for the 2 bridges of the DAB converter each with their advantages and disadvantages. The main methods of modulation are highlighted below.

The rectangular modulation method

The 2 bridges are controlled so that the primary and secondary transformer voltages are at 50% duty cycle and with a phase shift. This is the simplest form of modulation and the most commonly used implementation. This method has zero voltage switching (ZVS) instances for device turn-on for parts of the operating region of the converter. The advantages of this method are, the simplicity in control and the lowest rms current and hence the lowest conduction losses.

The trapezoidal current modulation method

In the trapezoidal method, both the primary and the secondary voltages have zero voltage states and are shown in Fig. 2-39 (a). This method results in an additional zero current switching (ZCS) turn-offs for 4 of the switching

devices and hence reduces the switching losses compared with the rectangular method [94]. The rms current of the bridge is higher than the rectangular method since there are zero voltage states.

The triangular current modulation method

The triangular method shown in Fig. 2-39 (b) is so called due to the triangular shape of the current. The modulation is similar to the trapezoidal method with the condition that there are overlapping edges of the 2 bridge voltages. The modulation method results in 6 of the switching devices to have ZCS [94] and therefore has the lowest switching losses. However, the downside is the increased rms current due to the lower duty cycle and resulting peak currents, which causes the highest conduction losses of the 3 methods of modulation. This method is attractive if high switching frequency is required which necessitates lower switching losses and low EMI emissions. [96]

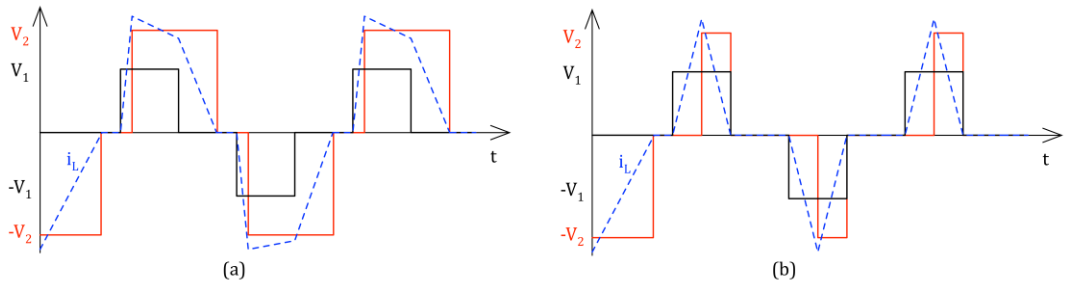


Fig. 2-39 (a) Trapezoidal modulation method (b) Triangular modulation method

It should also be noted that while the trapezoidal and triangular switching schemes could reduce switching losses, the resultant current in the transformer is discontinuous, and contains more high frequency harmonics, which may significantly increase the proximity loss in the transformer windings.

Other modulation methods

Variations of the conventional modulation methods have been proposed in [90] and [93], for example where one bridge is driven with a three state PWM signal whilst the other bridge is driven with a 50% PWM signal, to extend the soft switching region for the whole operating range. This modulation method has been shown to improve efficiency due to the reactive power minimisation leading to lower conduction and switching losses as well as reduced stress on the components.

Other methods of modulation include variable frequency modulation [92, 95, 97] that extends the ZVS region for lower power levels as well as hybrid modulation schemes [89, 91, 96] that dynamically change the modulation method dependant on operating conditions in order to minimise losses in the converter.

For the application of the HF charger, the rectangular modulation method is considered for its simplicity, and lower conduction loss and lower high frequency copper loss in the transformer (relative to the trapezoidal and triangular methods). Fig. 2-40 illustrates the current and voltage waveforms for the DAB in the rectangular method of operation. V_p and V_s are the transformer primary and secondary voltages, I_p is the transformer primary current and I_i is the converter input current. The table in Fig. 2-40 also indicate the transistor and diode conduction states for the simplified equivalent circuit of the DAB converter shown in Fig. 2-41. The 2 bridges are modulated with a 50% duty cycle and a phase shift of δ.

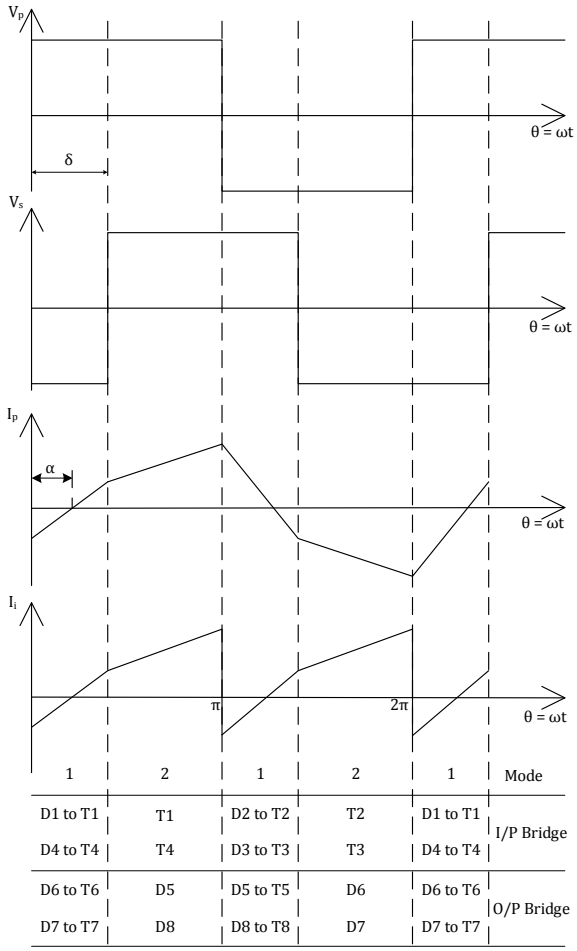


Fig. 2-40 Waveforms and corresponding bridge component states for the DAB under rectangular modulation

The equations governing the operation of the DAB can therefore be derived as described in [90].

The equivalent circuit of the converter is shown in Fig. 2-41 where the transformer magnetising inductance is assumed to be infinite. The voltage conversion ratio (d) can be defined as shown in equation (2-42) where N is the transformer turns ratio and V_1 and V_2 are the DC voltages of the 2 sides of the bridge.

$$d = \frac{V_2'}{V_1} = \frac{NV_2}{V_1} \qquad \textbf{(2-42)}$$

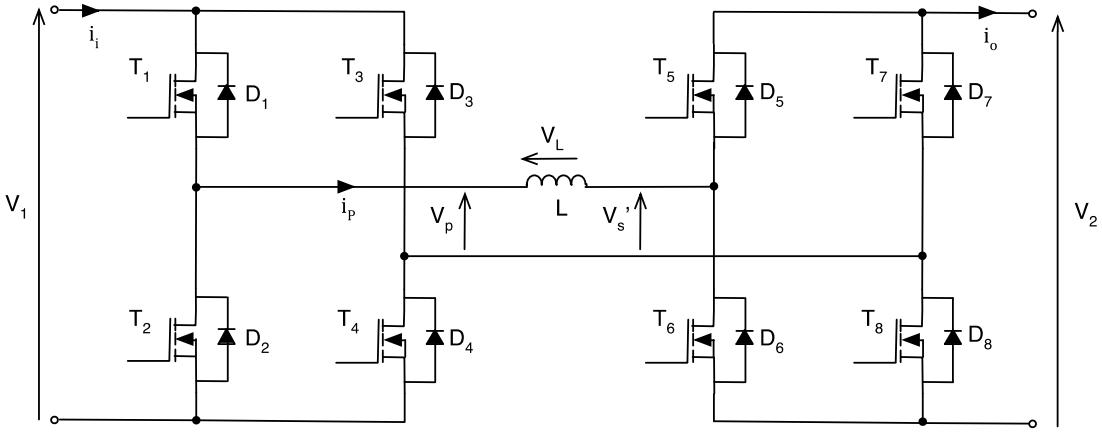


Fig. 2-41 DAB converter equivalent circuit

At the frequency of the DAB operation, the resistance effect of the equivalent inductor is negligible. Thus the current in the inductor or the primary winding of the transformer is governed by the following equation for mode 1 ($0 < \theta \leq \delta$):

$$i_L(\theta) = \frac{1}{\omega L}\int_0^{\theta}(V_1 + V_2')d\theta + i_L(0) = \frac{V_1 + V_2'}{\omega L}\theta + i_L(0) \qquad \textbf{(2-43)}$$

Similarly, the equation for mode 2 ($\delta < \theta \leq \pi$) is:

$$i_L(\theta) = \frac{1}{\omega L}\int_{\delta}^{\theta}(V_1 - V_2')d\theta + i_L(\delta) = \frac{V_1 - V_2'}{\omega L}(\theta - \delta) + i_L(\delta) \qquad \textbf{(2-44)}$$

Since the average current in L is zero ($i_{L_{ave}} = 0$),

$$i_L(0) = -i_L(\pi) \qquad \textbf{(2-45)}$$

From equations (2-43) and (2-44);

$$i_L(0) = \frac{-V_1}{2\omega L}\big(\pi + d(2\delta - \pi)\big) = -i_L(\pi) \qquad \textbf{(2-46)}$$

And,

$$i_L(\delta) = \frac{(V_1 + V_2')\delta}{\omega L} + i_L(0) \quad \textbf{(2-47)}$$

If we assume an ideal converter with efficiency of 100% and hence $P_i = P_o$, the output power P_o can be derived by integrating the input current I_L as a function of theta times voltage on the transformer's primary as given below.

$$P_o = \frac{1}{2\pi}\left[V_1\int_0^{\delta} i_L(\theta)d\theta + V_1\int_{\delta}^{\pi} i_L(\theta)d\theta - V_1\int_0^{\delta} -i_L(\theta)d\theta - V_1\int_{\delta}^{\pi} -i_L(\theta)d\theta\right] \quad \textbf{(2-48)}$$

$$P_o = \frac{1}{2\pi}\left[2V_1\int_0^{\delta} i_L(\theta)d\theta + 2V_1\int_{\delta}^{\pi} i_L(\theta)d\theta\right] \quad \textbf{(2-49)}$$

And from the previous equations for $i_L(\theta)$ for modes 1 and 2 (2-43) (2-44), we can derive:

$$P_o = \frac{V_1^2 d\delta}{\omega L\pi}[\pi - \delta] \quad \textbf{(2-50)}$$

For zero voltage switching (ZVS) to occur, the diodes should be freewheeling when the transistor is turned 'on'. This implies the following conditions have to be met:

$$i_L(0) < 0 \; and, i_L(\delta) > 0$$

From the first inequality and from equation (2-46),

$$\frac{V_1}{2\omega L}[\pi + d(2\delta - \pi)] > 0 \quad \textbf{(2-51)}$$

From the second inequality and from equations (2-46) and (2-47),

$$\frac{(V_1 + V_2)\delta}{\omega L} > \frac{V_1}{2\omega L}[\pi + d(2\delta - \pi)] \quad \textbf{(2-52)}$$

Therefore it can be shown that for (d<1) the following condition must be met for ZVS switching to occur,

$$\delta > \frac{\pi}{2}(1 - d) \quad \textbf{(2-53)}$$

And similarly from equation (2-51), for (d>1) the following must be met for ZVS,

$$\delta > \frac{\pi}{2d}(d - 1) \quad \textbf{(2-54)}$$

From equations (2-50) and (2-42), we can define the average output current as follows,

$$I_o = \frac{V_1 N \delta}{\omega L \pi}(\pi - \delta) \quad \textbf{(2-55)}$$

The per-unit average output current is defined as given in equation (2-56) below.

$$I_o[p.u.] = \frac{I_o}{V_1 N / X_L} = \frac{\delta}{\pi}(\pi - \delta) \qquad \textbf{(2-56)}$$

The ZVS switching region under conventional rectangular modulation can be derived from equations (2-53), (2-54) and (2-56) and is presented in Fig. 2-42. It can be seen that complete soft switching is only available if the voltage conversion ratio is 1. At other values of d, the converter leaves the soft switching region and is more prominent at lower power levels. It is possible to use the alternative modulation scheme proposed in [90, 93] to obtain soft switching for lower power levels, although the overall efficiency benefit vs. the increase in complexity is determined by the relative proportion of the energy that is transferred during the ZVS vs. non-ZVS condition.

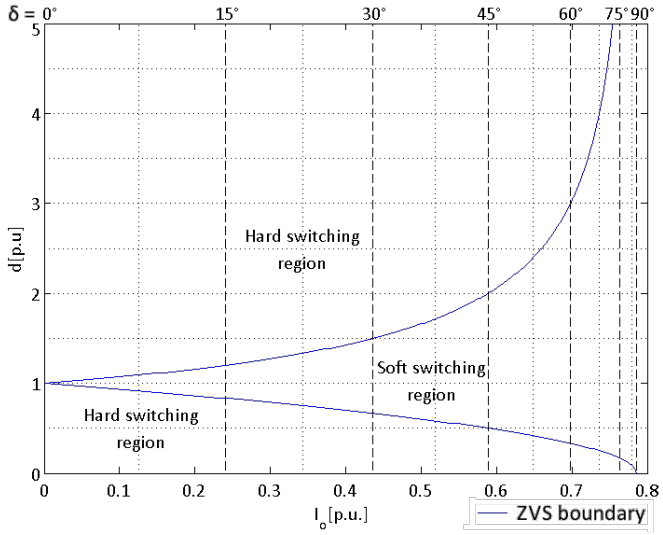


Fig. 2-42 Soft switching boundary for d vs. I_o[p.u.]

Effect of finite magnetising inductance

The magnetising inductance is assumed to be infinite relative to the leakage inductance in the simplified model of the initial DAB converter analysis. However, the effect of the magnetising inductance on the operation of the DAB converter can be accounted for by defining the equivalent circuit as shown in

Fig. 2-43 where the leakage inductance L, is split into 2 branches of $\frac{L}{2}$ each and the magnetising inductance is defined as ML where M is the ratio between the magnetising and leakage inductances.

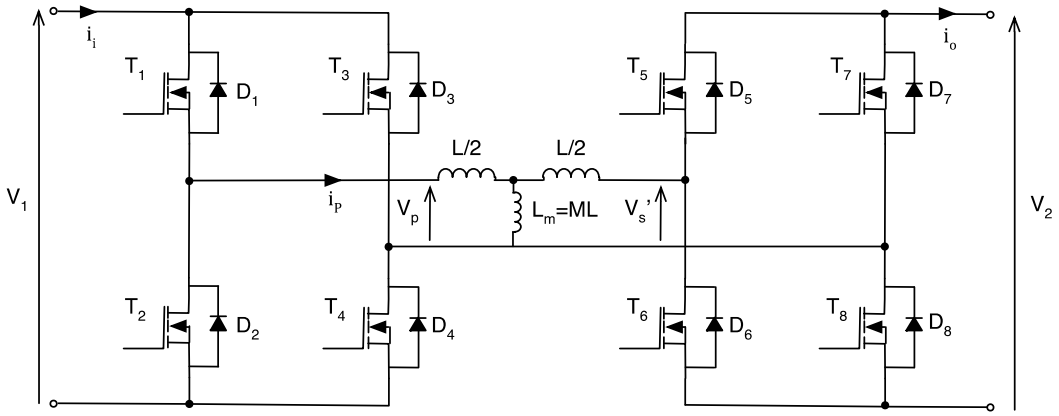


Fig. 2-43 DAB converter equivalent circuit for finite L_m

The current in the primary winding of the transformer can be defined by the following equation for mode 1 $(0 < \theta \leq \delta)$:

$$i_L(\theta) = \frac{1}{\omega L(1+4M)} \int_0^{\theta} [4M(V_1 + V_2') + 2V_1] d\theta + i_L(0) \qquad \textbf{(2-57)}$$

$$= \frac{4M(V_1 + V_2') + 2V_1}{\omega L(1+4M)} \theta + i_L(0)$$

Similarly, the equation for mode 2 $(\delta < \theta \leq \pi)$ is:

$$i_L(\theta) = \frac{1}{\omega L(1+4M)} \int_{\delta}^{\theta} [4M(V_1 - V_2') + 2V_1] d\theta + i_L(\delta) \qquad \textbf{(2-58)}$$

$$= \frac{4M(V_1 - V_2') + 2V_1}{\omega L(1+4M)} (\theta - \delta) + i_L(\delta)$$

Therefore, $i_L(0)$ can be defined as:

$$i_L(0) = \frac{-V_1}{\omega L(1+4M)}\left(\pi + 2\mathrm{M}(2\mathrm{d}\delta + \pi - d\pi)\right) \quad \textbf{(2-59)}$$

And,

$$i_L(\delta) = \frac{[4\mathrm{M}(V_1 + V_2') + 2V_1]\delta}{\omega L(1+4M)} + i_L(0) \quad \textbf{(2-60)}$$

Assuming an ideal converter with efficiency of 100% and hence $P_i = P_o$, the output power P_o can be derived by integrating the input current I_L as a function of theta times voltage on the transformer's primary as given below.

$$P_o = \frac{1}{2\pi}\left[2V_1\int_0^{\delta} i_L(\theta)d\theta + 2V_1\int_{\delta}^{\pi} i_L(\theta)d\theta\right] \quad \textbf{(2-61)}$$

From the previous equations for $i_L(\theta)$ for modes 1 and 2, the output power can be defined as:

$$P_o = \frac{4MV_1^2 d\delta}{\omega L\pi(1+4M)}[\pi - \delta] \quad \textbf{(2-62)}$$

For zero voltage switching (ZVS) to occur, the diodes should be freewheeling when the transistor is turned 'on'. This implies the following conditions have to be met:

$i_L(0) < 0\ and, i_L(\delta) > 0$

Therefore it can be shown that for (d<1) the following condition must be met for ZVS switching to occur,

$$\delta > \frac{\pi[1 + 2M(1-d)]}{(2+4M)} \quad \textbf{(2-63)}$$

And similarly for (d>1) the following must be met for ZVS,

$$\delta > \frac{\pi[2M(d-1)-1]}{4dM} \quad \textbf{(2-64)}$$

The average output current can be defined as follows,

$$I_o = \frac{4MV_1N\delta}{\omega L\pi(1+4M)}(\pi - \delta) \quad \textbf{(2-65)}$$

The per-unit average output current is defined as below,

$$I_o[p.u.] = \frac{I_o}{V_1N/X_L} = \frac{4M\delta}{\pi(1+4M)}(\pi - \delta) \quad \textbf{(2-66)}$$

The ZVS switching region under conventional rectangular modulation for finite magnetising inductance can be derived from equations (2-63), (2-64) and (2-66). The two extreme cases of infinite magnetising inductance and a magnetising inductance value equal to the leakage inductance value (M=1) are presented in Fig. 2-44. It is seen that when M=1, the soft switching region for (d>1) extends whereas for (d<1), the region becomes smaller for lower power levels. However in reality, the value of M is much larger than 1, and therefore the deviation from the ideal assumption of infinite magnetising inductance is minimal as will be discussed in section 2.3.2.3.

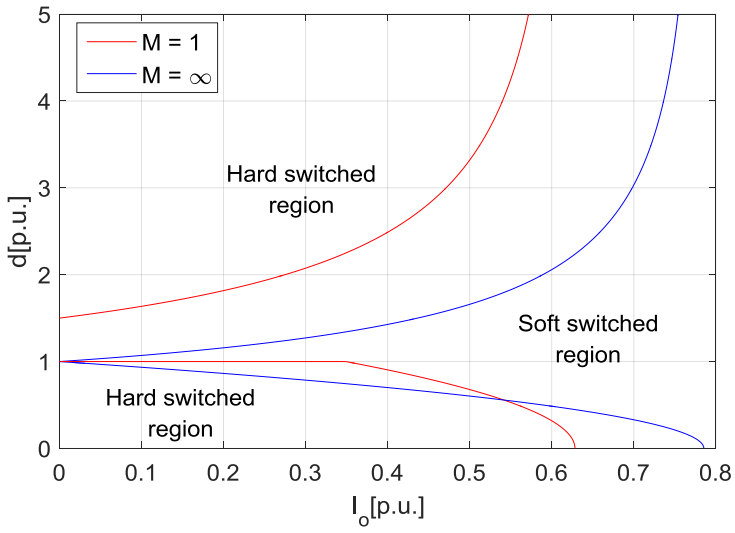


Fig. 2-44 Soft switching boundary for d vs. I_o[p.u.] for infinite L_m and L_m=L

2.3.2.2. DAB converter MOSFET sizing

ZVS region of charge/discharge cycle

To characterise the converter losses, the DAB operation throughout the whole charge/discharge cycle must be analysed in order to determine the ZVS region. Based on the battery specification in Table 2-3, the simulated charge curves are presented in Fig. 2-45 where the ZVS and non-ZVS regions are highlighted. The total charge cycle requires 5 hours to complete in which the first stage is the constant current (CC) stage where the converter operates at the rated power level of 2.2 kW that results in a battery current of 17 A. The second stage of the charging is the constant voltage (CV) stage, which occurs when the cell voltage reaches 4.1 V. In the CV stage, the battery current and hence the power delivered to the battery decays exponentially until the battery reaches full charge (current falls below trickle level).

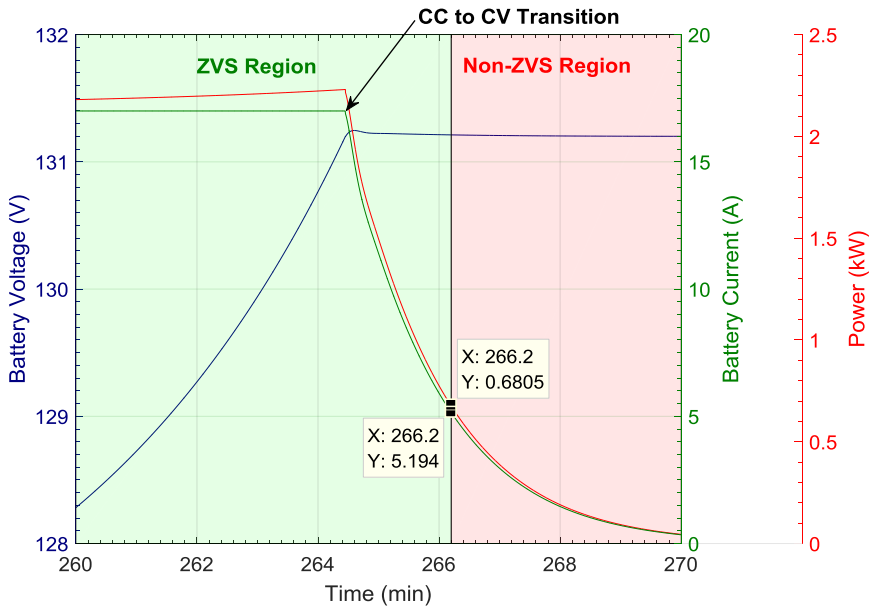


Fig. 2-45 Battery voltage, current and power delivered for charging. The DAB ZVS region is highlighted as well as the CC to CV transition.

It is observed that the ZVS occurs during the full CC stage and the DAB only leaves the ZVS operation near the end of the CV stage. More specifically, the ZVS to non-ZVS boundary occurs at a battery current level of 5.2 A, and hence DAB output power level of 681 W. In terms of energy delivered to the battery, the non-ZVS region only consists of 0.2% (16 Wh) of the total charge energy (9.37 kWh). Therefore it can be determined that the non-ZVS region has negligible affect on the overall efficiency of the G2V operation.

Typical V2G mode operation consists of constant power at the rated 2.2 kW, which falls under the ZVS condition for the whole battery voltage range.

DAB MOSFET sizing

For determining the current ratings of the MOSFETs of the converter, it is required to establish the rms and peak currents in the transformer's primary winding. The rms currents of the primary side for mode 1 ($0 < \theta \leq \delta$) and mode 2 ($\delta < \theta \leq \pi$) are given in (2-67) and (2-68) respectively.

$$I_{rms\_1}^2 = \frac{1}{2\pi}\int_0^{\delta}\left(A\theta + i_L(0)\right)^2 d\theta = \frac{\frac{A^2\delta^3}{3} + A\delta^2 i_L(0) + \delta i_L(0)^2}{2\pi} \quad \textbf{(2-67)}$$

$$I_{rms\_2}^2 = \frac{1}{2\pi}\int_{\delta}^{\pi}\left(B[\theta - \delta] + i_L(\delta)\right)^2 d\theta = \frac{-i_L(\delta)^3 + (i_L(\delta) + B[\pi - \delta])^3}{6B\pi} \quad \textbf{(2-68)}$$

Where A, B and $i_L(\delta)$ are defined as follows;

$$A = \frac{(V_1 + V_2')}{\omega L} \quad \textbf{(2-69)}$$

$$B = \frac{(V_1 - V_2')}{\omega L} \quad \textbf{(2-70)}$$

$$i_L(\delta) = A\delta + i_L(0) \quad \textbf{(2-71)}$$

Since the waveform is symmetrical around π, it follows that the total rms current in the transformer primary winding is given as:

$$I_{rms\_L} = \sqrt{2\left(I_{rms\_1}^2 + I_{rms\_2}^2\right)} \quad \textbf{(2-72)}$$

Furthermore, the peak value of the primary current (I_{pk_L}) is which ever is larger of the two values of $|i_L(0)|$ and $|i_L(\delta)|$.

It is noted that the secondary winding rms and peak currents are NI_{rms_L} and NI_{pk_L}, respectively.

For MOSFET sizing, the maximum rms and maximum peak values of the current for the 2 windings has been evaluated for the charge/discharge cycles of the converter and found to be 6.3 A, 8.1 A for the primary and 19.6 A, 25.1 A for the secondary respectively.

Therefore, the MOSFET devices for both bridges of the DAB converter are selected to be STW55NM60ND devices. The STW55NM60ND has a continuous drain current rating of 51 A, voltage rating of 650 V and a fast recovery diode which makes the switching losses low. The same devices are selected for the frontend converter, as the current and voltage ratings are sufficient for both applications.

2.3.2.3. Transformer specification for DAB

An optimised DAB transformer design intended to minimise the total losses of the converter has been reported in [98] for the same converter specifications as the one under investigation. Therefore, the following Table 2-13 presents the summary of the transformer specification that is used for the comparison of converters and in the subsequent chapter for DAB converter controller design and simulation.

Table 2-13 HF transformer parameters

Parameter	Value
Primary turns	28
Secondary turns	9
Primary referred leakage inductance	98.6 µH
Secondary referred leakage inductance	10.23 µH
Primary magnetising inductance	7.161 mH
Secondary magnetising inductance	742.1 µH
Switching frequency	40 kHz

It can be observed that for the transformer specifications in Table 2-13, the ratio between the magnetising and leakage inductances (M) is 72.6.

Therefore, the ZVS region for the transformer compared with the ideal infinite magnetising inductance is depicted in Fig. 2-46. It is seen that the deviation from the ideal assumption is minimal. Furthermore from equations (2-56) and (2-66) it can be observed that the output current deviation between an infinite L_m and an L_m of 7.16 mH is only 0.34%.

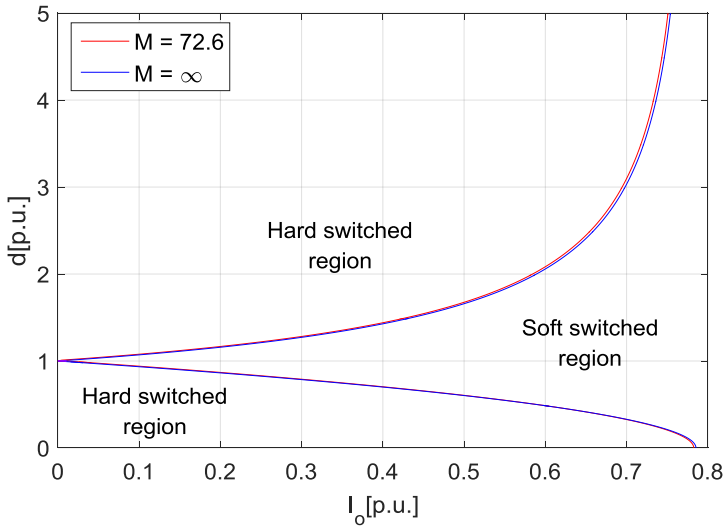


Fig. 2-46 Soft switching boundary for d vs. I_o[p.u.] for infinite L_m and L_m=72.6

2.4. Comparison of converter loss

The operation of the dual active bridges has been described in [98] and an analytical formula for quantifying the converter losses has been established. Further, an optimal design procedure for the high frequency transformer has been developed and utilised to determine the transformer size and efficiency. The details are given in [98] and the results are used in the subsequent comparison in section 2.5.

DAB converter switching device loss estimation

The losses in the converter switching devices are estimated based on the equations presented in [98] for the transformer specification given in Table

2-13 and the STW55NM60ND MOSFET devices with intrinsic fast-recovery body diode. The DAB converter losses were calculated to be 55.6 W at the rated 2.2 kW operating point (where ZVS occurs) with a nominal battery voltage of 120 V and assuming a device junction temperature of 60°C.

Frontend converter switching device loss estimation

For option 1, the power electronic switches in the motor drive are used for grid interface via a low frequency transformer while for option 2, a separate frontend H-bridge converter is required to perform the AC to DC conversion or vice versa. The principle of operation of the H-bridge in both the options is the same but they differ in the DC link voltage and hence the converter current. The total converter loss of each option can be calculated for the nominal power of 2.2 kW and assuming a device junction temperature of 60°C, taking into account of the voltage and current difference.

For option 1, the integrated switching devices of the motor drive are composed of Vincotech F0062PA150SA01 IGBTs. Therefore, the losses for option 1 and 2 are calculated based on the method in [99] and [100] respectively.

Table 2-14 Comparison of frontend converter switching device losses of the 2 converters

Parameter	Option 1	Option 2
Nominal DC-link voltage	120 V	380 V
Frontend switching losses	60 W (total)	118.4 W (total)
Frontend conduction losses	68.6 W (total)	10.9 W (total)
Frontend converter total losses	128.6 W	129.4 W
Frontend efficiency	94.15%	94.12%

Table 2-14 presents the comparison of the frontend converter losses for the 2 charger options. No additional heatsink is required for the LF charger, as the motor drive inverter of the vehicle already contains a cooling system.

Sensitivity analysis of converter efficiency

Although the efficiency of the two converters were estimated for operation under the rated nominal power and same device junction temperature for a baseline comparison, a more detailed sensitivity analysis considering the effects of ambient temperature and varying load conditions is presented as follows.

Since the losses in MOSFET as well as IGBT devices are dependent on the junction temperature, the analysis relies on the data available from the device datasheets for estimating the conduction and switching losses at a given junction temperature. It is assumed that a HS Marston 890SP-01500-A-100 heatsink is used for the two converters which has a thermal resistance of 0.08°C/W under forced air cooled conditions (PAPST 3312NN axial fan with 80 m^3/h of airflow rate) as stated in the datasheet. The junction to case thermal resistance values stated in the device datasheets are used for junction temperature estimation. Since the device junction temperature and device power loss are interdependent, the power losses and resulting junction temperature for a given ambient temperature are iteratively calculated until the estimated junction temperature is stable within 0.01C° as depicted in Fig. 2-47.

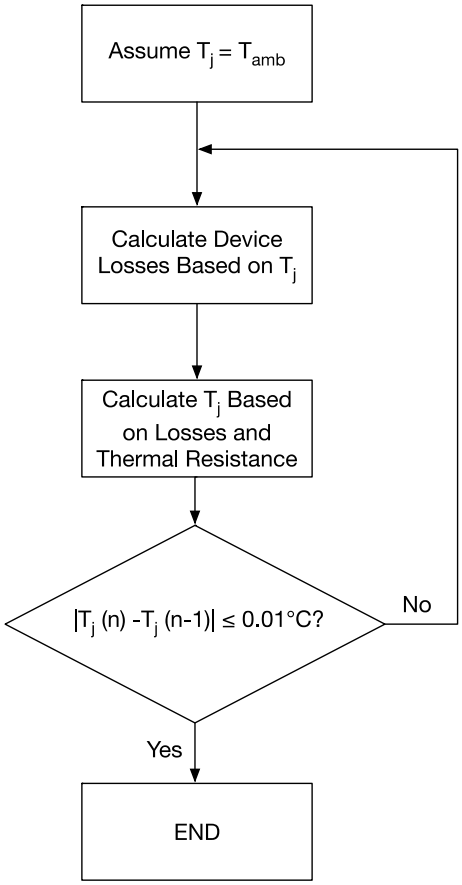


Fig. 2-47 Iterative algorithm for device loss and junction temperature estimation

The procedure begins by assuming that the junction temperature (T_j) is the same as the ambient temperature (T_{amb}) and estimating the resulting losses in the device. Afterwards, the resulting junction temperature due to the estimated power dissipation is calculated based on the junction to ambient thermal resistance. Since the increase in junction temperature causes further increase in device power loss due to the temperature dependence of the device characteristics, the process is iterated till the junction temperature is stable within 0.01C°.

The power losses in the inductors and transformers are dependent on the operating power level as well as the ambient temperature. The effects due to temperature in the copper losses is due to the change in the winding resistance with temperature. Therefore, the winding losses are estimated by

assuming that the windings operate at a temperature of 20°C above ambient. The temperature dependence of the core losses are not considered and instead, a worst case core loss estimate based on the core material datasheet is used for the analysis irrespective of ambient temperature.

An ambient temperature range of -40°C to 100°C is considered for the analysis. Since ZVS of the DAB converter is only available above a power level of 680 W and since the non-ZVS region only contributes to 0.2% of the total charge delivered during a charge cycle (as discussed in section 2.3.2.2), a converter output power range of 700 W to 2.2 kW is considered for the analysis.

The power required for gate drive circuitry, sensor signal conditioning, digital signal processor (DSP), cooling fan and the losses in the LCL damping resistor are not considered for the efficiency analysis.

The following Fig. 2-48 and Fig. 2-49 depict the variation of converter efficiency as a function of ambient temperature and output power level for the LF and HF converter respectively. It can be observed that operation under lower temperature results in better converter efficiency and this is attributed to the lower losses in both the switching devices as well as the magnetic components at lower temperatures. It can be seen that the overall efficiency of the converters for an output power level of 2.2 kW is 87.8%-90.8% and 87.9%-90.5% for the LF and HF converters respectively, over the full temperature range.

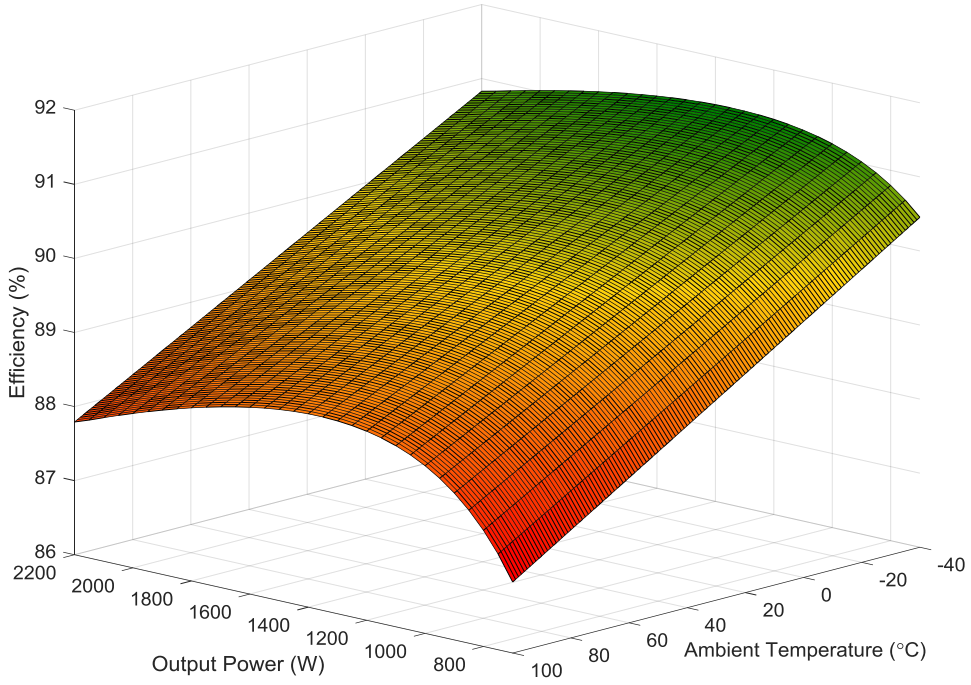


Fig. 2-48 Overall converter efficiency as a function of ambient temperature and output power level for option 1 (LF converter).

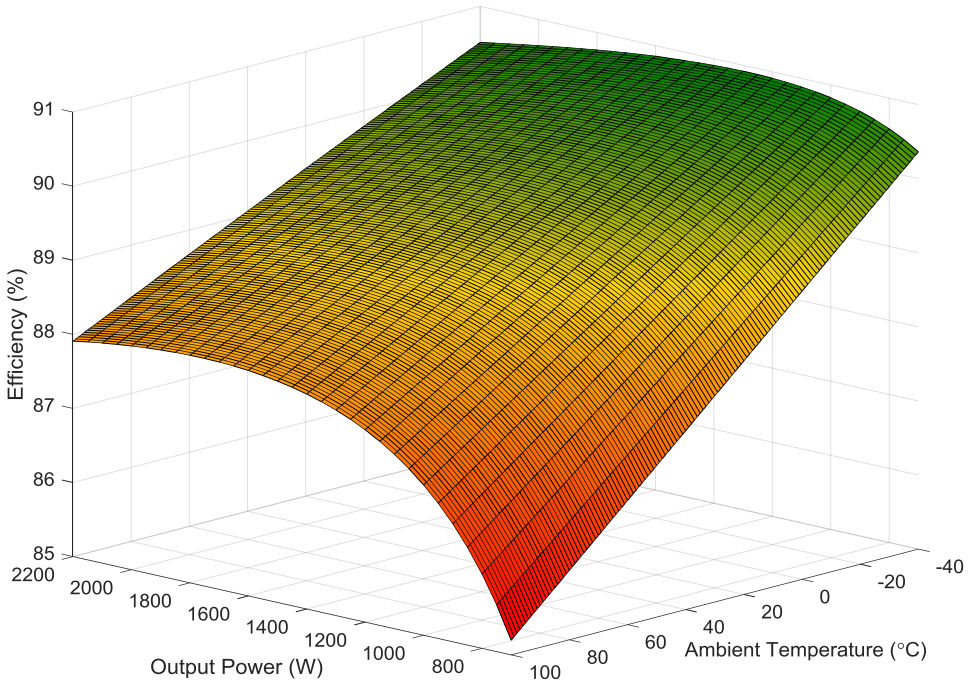


Fig. 2-49 Overall converter efficiency as a function of ambient temperature and output power level for option 2 (HF converter).

2.5. Overall comparison of options

The Table 2-15 below presents the comparison between the two converter options in terms of efficiency (at the nominal operating power of 2.2 kW and an ambient temperature of 20°C), weight and cost. Option 1 requires a DPDT isolation relay for switching between the motor and the transformer. The converter efficiency for option 2 is the combined efficiency of the frontend and the DAB. The cost of the transformers and inductors are based on usage of copper wires and core materials. For the HF transformer, the cost of Litz wire is taken into account. The costs of other components are estimated according to their market price. For option 2, TMSF28335 DSP processor based control board is assumed and its cost is estimated. It is also assumed that for option 1, the current sensors in the motor drive can be used for detecting the battery current as well as the transformer's secondary current (the grid current can be obtained by dividing by the turns ratio and any phase shift can be compensated in the current controller). Therefore only the grid voltage sensor is required as an additional sensor.

The thermal and mechanical design of the converters is not conducted in this study and therefore the cost and weight of housing is not considered for the comparative evaluation of the two converters.

Table 2-15 Comparison of the 2 converter options

Parameter	Option 1 LF transformer & motor inverter	Option 2 HF transformer & DAB
Transformer efficiency (%)	94.94	98.86
Converter efficiency (%)	94.74	93.96 (front end), 97.91 (DAB)
Inductor efficiency (%)	99.84 (L_g)	99.8 (L_g), 98.87 (L)
Total efficiency (%)	**89.81 (at 20°C ambient)**	**89.74 (at 20°C ambient)**
Transformer weight (kg)	13.86	0.75
Weight of switches (kg)	0.25 (DPDT relay)	N/A
Inductor weight (kg)	0.049 (L_g)	0.072 (L_g), 0.907 (L)
Capacitor weight (kg)	0.045 (filter capacitor)	0.045 (filter capacitor) 0.2 (DC link capacitor)
Heat-sink and fan weight (kg)	N/A	2.11
Weight of actives switches, bus bars & control board (kg)	N/A	1.6
Total weight (kg)	**14.2**	**5.68**
Transformer cost (£)	8.8 x 2.29 kg (Cu) +1.0 x 11.57 kg (iron) = 32.72	5.9 (core), 4 (bobbin), 30 (winding), 5 (insulation) = 44.9
Cost of isolation relay (£)	30 (Magnecraft 199X-12)	N/A
Inductor cost (£)	8.8 x 0.028 kg (Cu) +1.0 x 0.021 kg (iron) + 1.35 (bobbin) = 1.62	0.03 (iron) + 10.6 (E71 core) + 1.35 + 5 (bobbins) + 8.8 (0.043 + 0.387) kg (Cu) = 20.76
Capacitor cost (£)	3.34 (filter capacitor)	14.7 (DC link: 2 x 470µF) 3.34 (filter capacitor)
Heat-sink and fan cost (£)	N/A	53 + 12
Cost of 12 actives switches (£)	N/A	5.5x12 = 66
Cost of control board (£)	N/A	120 (incl. gate drives)
Cost of voltage and current sensors (£)	40 x 1 (V_g)	40 x 3 (V_g, V_{dc}, V_{bat}) 9 x 2 (I_g, I_{bat})
Cost of EMC filter (£)	15	15
Total cost (£)	**123**	**488**

An EMC filter is required for both options and their cost is identical. In option 1, the DC link capacitors are already present for the motor drive inverter and hence not factored for the cost of the charger.

When estimating the LF and HF transformer prices, only the material costs are included. It should be noted that although the weight of the LF transformer is much heavy its material cost is not significantly higher than that of the HF transformer which requires more expensive ferrite core and Litz wire. As can be seen from the comparison, both options have comparable efficiency, while option 1 has a much lower cost (25% of the cost), but is heavier (2.5 times) than option 2. Due to a much less component count with option 1, its reliability should also be higher.

2.6. Summary

In this chapter, two options of bi-directional charging systems have been presented which are, low frequency transformer based and high frequency DAB based converters.

The frontend LCL filter optimisation for both converters in terms of weight and size has been presented. Furthermore, the design of the inductors and transformers has been presented along with switching device sizing and the differences of the two methods in terms of weight; efficiency and cost have been compared.

It can be seen that the DAB based approach is ~4 times as costly, but the weight is reduced by a factor of 2.5. Both methods are viable for electric vehicle and deliver similar performance. The actual method of implementation can be chosen depending on the application's constraints of size/weight vs. cost.

Chapter 3

Controller Design, Simulation & Experimental Results of the OBBC Systems

This chapter presents the controller design, simulation and converter experimental demonstration aspects for the two types of charger systems discussed in the previous chapter. The existing methods of DAB modelling, DAB control, grid current control and harmonic compensation are discussed in the first section. This is followed by the descriptions of the design methodology, converter simulation and implementation details as well as experimental validation.

3.1. Introduction

3.1.1. Control of Dual Active Bridge Converters

DAB Dynamic Modelling Methods

In order to understand the behaviour of DAB converters for the purpose of controller design, it is important to establish the dynamic model of the converter. The most accurate concepts of modelling reported in literature involves the full order discrete time methods [101]. The full order discrete method reported in [102] also takes into account the resonant transitions between the leakage inductance and the MOSFETs' output capacitances that result in the ZVS of the devices.

The second category of modelling methods is the continuous time methods, which are generally preferred for controller design [103]. The simplest form of continuous time modelling methods for DAB converters consists of reduced order modelling which simplifies the order of the system by

ignoring the transformer current dynamics. Such methods have been reported in literature [104-106].

A more accurate continuous time modelling method has been reported in [103, 107] and applied for the control of solid-state transformers (SSTs) in [107-109]. The method consists of taking into account the ac terms of the Fourier series in the transformer current and is termed as generalised average modelling. This differs from the standard averaging technique, which assumes that there is no current ripple.

DAB Control Methods

The control variable for DAB converters are generally the regulation of the output voltage at the load (power supply applications), the regulation of the output current to the load (battery charging applications) or the control of power delivered to the load.

Current control methods for bidirectional battery charging (from V2G and G2V) have been reported in [110] and [111] in which a method of DC link capacitor size reduction by the use of the sinusoidal current charging method is also proposed. This involves the intentional propagation of the double grid frequency component of power directly to the battery. This has been achieved by the application of a sinusoidal demand signal to the DAB current controller, which is in phase with the grid voltage.

Output voltage control of DAB converters for SSTs have been reported in [107-109] where PI & Feedforward type and PI-Resonant type controllers have been demonstrated which reduce the effects of the double grid frequency disturbance. The DAB output voltage control method reported in [106] utilises an adaptive PI controller to compensate for the variations in the steady state operating conditions.

A combination of voltage and current control schemes for the charging and discharging of low-voltage batteries (for uninterruptible power supplies)

has been reported in [112] where variable switching frequency is utilised to increase the ZVS region. Furthermore, DAB power flow control for a bidirectional battery charger in low-voltage microgrids has been reported in [113] where the charge rate is adjusted dynamically to support the grid during transient conditions with the aim of improving power quality.

3.1.2. Grid converter current control

Grid connected power converters that interface a DC bus to an AC supply require a method to regulate the current flowing to/from the utility grid in order to facilitate power flow. Since the utility voltage is sinusoidal, the current controller must be able to control the inverter current to be in phase and have the same frequency as the utility voltage as well as having the required magnitude. There are two main categories of current controllers based on the device switching method, which are on/off controllers and PWM controllers [33].

The on/off type controllers such as hysteresis type controllers operate by comparing the grid current to a reference with a hysteresis band comparator and thereby derive the switching signals for the devices [114]. Hysteresis type controllers have the advantages of simplicity and robustness, however also has the disadvantage of not having a fixed modulation frequency [115].

The second type of current controllers is based on constant frequency pulse width modulators, which can be further classed into linear and non-linear controllers. Examples of non-linear controllers are fuzzy logic based [116] and neural network based methods [117, 118]. Linear methods are typically in the form of PI, predictive dead-beat controllers [33, 119-121] and resonant controllers [33].

In this chapter, the linear methods based on PI and resonant controllers will be discussed.

PI controllers in a stationary reference system have difficulty in tracking sinusoidal reference signals without steady state error, as well as poor disturbance rejection due to the limitation of bandwidth as the application of large amounts of gain may lead to instability [122]. As a solution to this issue, voltage feed forward is often used to improve the dynamic response [33].

DQ Current Control

A more preferred approach to the use of conventional PI controllers in a stationary reference system is to transform the reference frame to a rotating synchronous frame. This has the effect of transforming the time varying signals into time invariant DC quantities and therefore it is possible to apply PI controllers to achieve zero steady state error. The rotating frame consists of D and Q axes which are orthogonal to each other and therefore separate PI controllers are used often with additional feedforward of the D and Q grid voltage terms.

As a result of the rotating frame transformation, active and reactive power control is separated into the 2 PI controllers on each axis. Therefore it is possible to control the active and reactive power independently, although in most applications, the reactive power demand is set to zero.

The use of DQ current control for 3 phase inverter systems has been reported in [75, 79, 123-126] and the application for single-phase systems is reported in [127-131].

In single phase systems, the DQ transformation of the grid current/voltage signals requires a 90° phase delayed version of the signal. This signal can be obtained by using a number of different methods such as a simple $\pi/2$ delay (memory based), using the Hilbert transform [132] or by using an all pass filter [131].

Grid Current Control with Resonant Controllers

An alternative to the DQ based current control method is the application of a proportional + resonant controller (PR) as reported in [122, 125, 133-136]. The transfer function of an ideal PR controller is shown in (3-1).

$$\frac{ks}{s^2 + \omega_h^2} \qquad \textbf{(3-1)}$$

The resonant controller exhibits a very large gain around a narrow region centred at the resonant frequency, which is designed to be at the fundamental frequency (50 Hz) for current control of grid connected converters. Therefore PR controllers are able to provide the high bandwidth required at the fundamental frequency to minimise steady state error as well as provide disturbance rejection. They are also less computationally intense than a synchronous frame current controller since reference frame transformations and feedforward terms are not required.

Harmonic Compensator

The presence of harmonics in the utility voltage results in the distortion of the grid current due to insufficient disturbance rejection property with conventional synchronous reference frame PI or PR controllers at the harmonic frequencies. Therefore, in order to improve THD performance of the converter a multitude of harmonic cancellation schemes have been developed over the years.

A multiple rotating frame harmonic cancellation scheme for the application in active filters is reported in [137] where individual integral regulators each rotating at the frequency of interest provides the harmonic cancellation.

On the other hand, the method reported in [130] consists of a synchronous frame fundamental frequency regulator along with multiple

resonant controllers in the stationary frame to realise the harmonic cancellation.

The method reported in [138] comprises of a hybrid system of a PI and multiple resonant controllers all implemented in a rotating frame. This enables two harmonics to be cancelled with each PR controller.

It is also possible to implement the fundamental frequency current regulation as well as the harmonic cancellation in the stationary frame with the use of resonant controllers (PR) for all the frequency terms as reported in [134, 139]. This provides the advantage of simplicity due to the absence of transformations.

Further variations of the methods discussed exists such as the methods analysed in [140] for the application in active power filters.

3.2. Controller design for high frequency transformer based charger

The control scheme for the HF transformer based charger is depicted in Fig. 3-1. The system is controlled with the use of four control loops. The DAB current controller maintains the desired battery current, which is determined by a battery charge algorithm based on the battery voltage and state of charge. The DC link voltage controller maintains a constant 380 V. The output of the DC link voltage controller determines the set point of the grid current control loop, which consists of a synchronous rotating frame PI controller with harmonic compensation. A phase locked loop (PLL) is used for determining the instantaneous angle (θ) of the grid voltage vector. The detailed design and analysis of the PLL is covered in Chapter 4. The device switching signals are generated by the PWM generation blocks for both the converters. In the case of the frontend inverter, comparing the input signal to a triangle carrier signal with a frequency of 10 kHz generates the unipolar PWM. The DAB modulation

block consists of generating two 50% duty cycle, 40 kHz square waves with a phase shift determined by the input signal to the block.

The DAB current controller design is discussed in section 3.2.1, after which the design of the 2 controllers for the frontend is discussed in sections 3.2.2 and 3.2.3. The battery charge algorithm is not discussed in the thesis as charge algorithms are well established in literature [141-145].

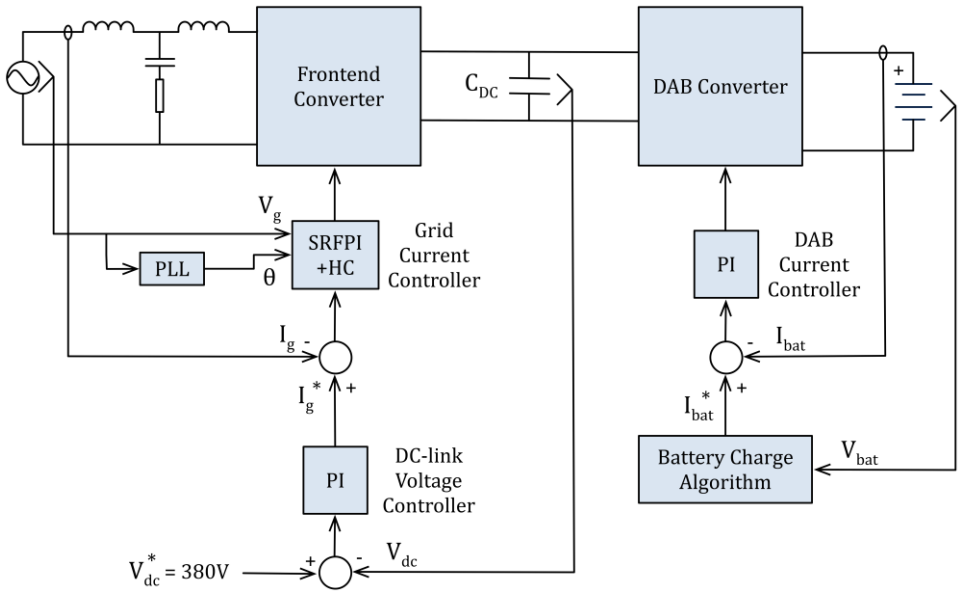


Fig. 3-1 HF transformer based charger control scheme

3.2.1. DAB current controller design

The circuit diagram of the DAB converter is illustrated in Fig. 3-2. As has been established in section 2.3.2, the average output current from the DAB stage, I_{O_ave} can be defined as given in (3-2) where δ is the phase shift angle between the 2 bridges, L_{lk} is the leakage inductance of the DAB transformer and ω_{sw} is the switching frequency of the DAB converter. For small signal dynamics, the battery voltage can be replaced with a short circuit and therefore the small signal transfer function between I_{O_ave} and I_B can be defined as (3-3) where

R_{bat} represents the equivalent series resistance of the battery. R_w and L_w represent the resistance and inductance of the battery leads.

$$I_{O\_ave} = \frac{V_{DC} N \delta}{\omega_{sw} L_{lk} \pi} (\pi - \delta) \tag{3-2}$$

$$G_{bat}(s) = \frac{I_B(s)}{I_O(s)} = \frac{1}{1 + sC_B(R_{bat} + R_w + sL_w)} \tag{3-3}$$

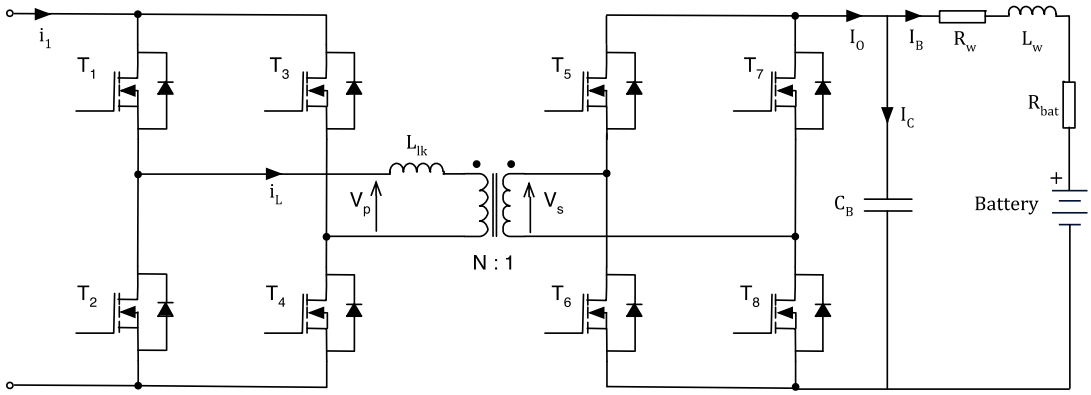


Fig. 3-2 Schematic of DAB converter circuit

Although the relationship between the phase shift angle δ and I_{O_ave} is nonlinear, for the purposes of controller design, the equation is linearised for the operating point of the nominal DC link voltage of 380 V between 10° (power level of 940 W) to 26° (power level of 2.2 kW) of phase shift and the resulting gain (38.16) is denoted as k_{DAB}.

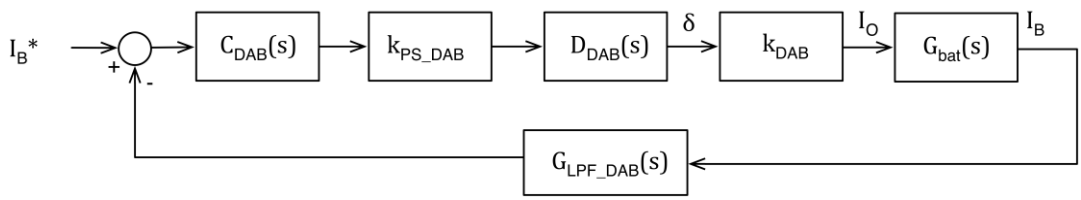


Fig. 3-3 Current controller structure

The detailed DAB current control loop is depicted in Fig. 3-3 where the PI controller's transfer function is defined as C_{DAB} and the delay due to the digital control loop is represented by $D_{DAB}(s)$ and consists of 1.5 times (1 period for the computation and half a period for the PWM sample and hold delay [146]) the switching control loop period ($t_d = 0.15\,ms$). The gain of the phase shift modulator is represented by k_{PS_DAB} which represents the gain introduced by the phase shift generation block. A low pass filter with a cut off frequency of 200 Hz ($G_{LPF\_DAB}(s)$) is used on the feedback path to limit the bandwidth of the system. The dynamics of the battery side capacitor is modelled by the term $G_{bat}(s)$.

$$G_{ol} = C_{DAB}(s)k_{PS\_DAB}D_{DAB}(s)k_{DAB}G_{bat}(s)G_{LPF\_DAB}(s) \quad \textbf{(3-4)}$$

$$G_{cl}(s) = \frac{C_{DAB}(s)k_{PS\_DAB}D_{DAB}(s)k_{DAB}G_{bat}(s)}{1 + C_{DAB}(s)k_{PS\_DAB}D_{DAB}(s)k_{DAB}G_{bat}(s)G_{LPF\_DAB}(s)} \quad \textbf{(3-5)}$$

$$C_{DAB}(s) = k_p + \frac{k_i}{s} \quad \textbf{(3-6)}$$

$$k_{PS\_DAB} = \frac{2\pi}{30} \quad \textbf{(3-7)}$$

$$k_{DAB} = 38.16 \quad \textbf{(3-8)}$$

$$D_{DAB}(s) = \frac{1 - \frac{t_d}{2}s}{1 + \frac{t_d}{2}s} \quad \textbf{(3-9)}$$

$$G_{LPF\_DAB}(s) = \frac{1}{\frac{1}{2\pi 200}s + 1} \quad \textbf{(3-10)}$$

The open loop and closed loop transfer functions of the system are given in (3-4) and (3-5), respectively where the terms are defined in (3-3) and (3-6) - (3-10). The values for k_p and k_i are chosen as 0.1 and 80 (final selection based on iterative evaluation of gain values to ensure stability margins and a fast

response time) to give a 3 dB frequency of 186 Hz and a rise time of 2.7 ms. The open loop Bode plot and closed loop step response is shown in Fig. 3-4 and Fig. 3-5. By evaluating the open loop transfer function, it is found that the zeros occur at (-800) and (13300). Therefore, there is a right half plane (RHP) zero in the open loop system. Furthermore, it can be observed that the gain margin is 20.8 dB and the phase margin is 95.2° and therefore the controller is determined to be stable.

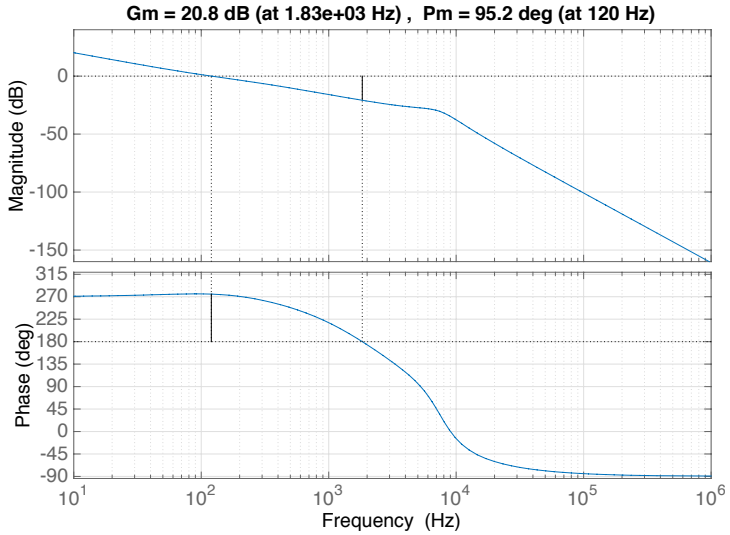


Fig. 3-4 Open loop Bode plot of DAB current controller

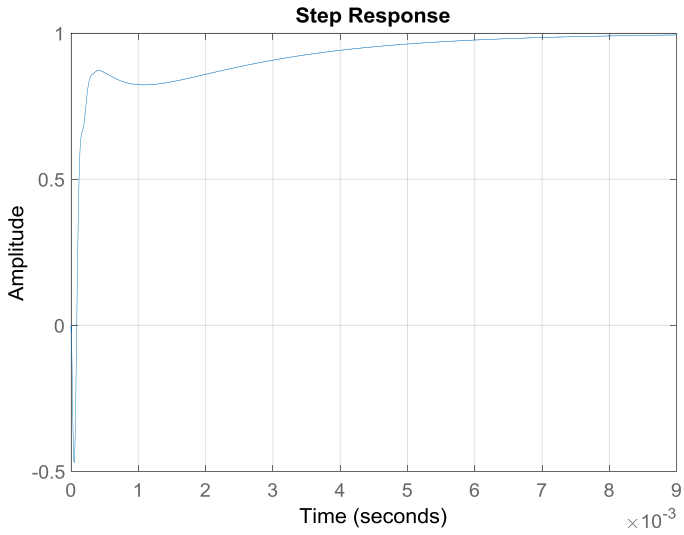


Fig. 3-5 Closed loop step response of DAB current controller

3.2.2. Grid current controller design

Synchronous Rotating Frame PI Controller

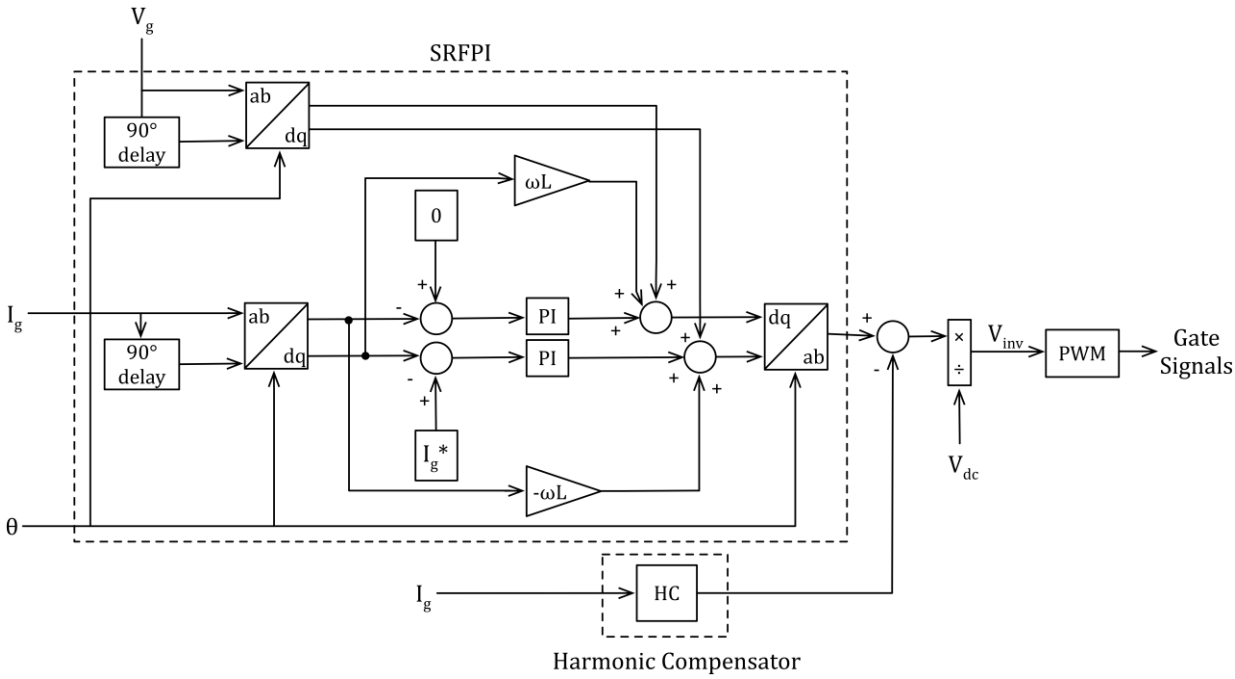


Fig. 3-6 Grid current controller structure

The current controller is designed based on a DQ synchronous frame current controller as highlighted in Fig. 3-6. The current demand I_g^* is tracked by the control structure which consists of two synchronous rotating frame PI controllers for the fundamental current control and a separate harmonic control scheme in the stationary frame with the measured feedback current I_g. The relationship between the stationary frame grid current (I_α), its imaginary counterpart (I_β) and the equivalent synchronous frame components of I_d/I_q is depicted in Fig. 3-7.

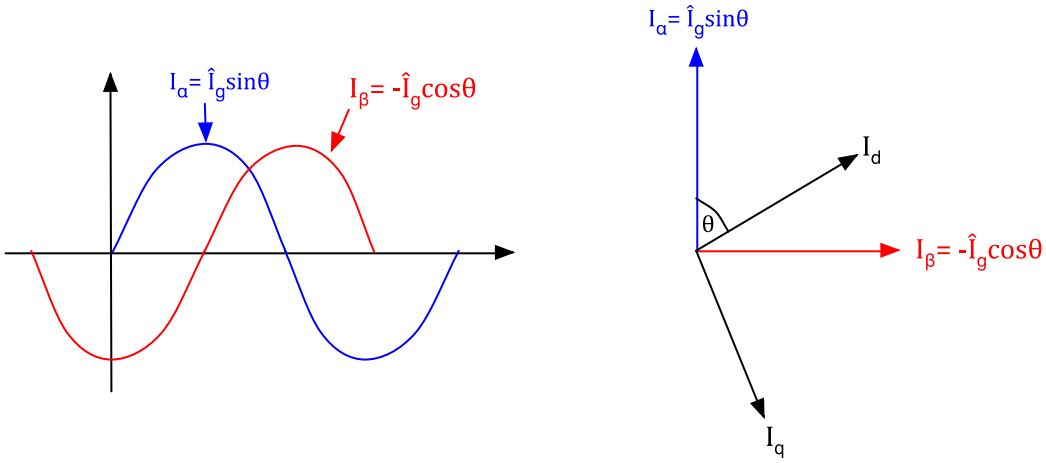


Fig. 3-7 Relationship between stationary and imaginary current components

Therefore the transformations between the stationary and rotating frames are carried out as defined in (3-11)-(3-12).

$$\begin{bmatrix} I_d \\ I_q \end{bmatrix} = \begin{bmatrix} cos\theta & sin\theta \\ -sin\theta & cos\theta \end{bmatrix} \begin{bmatrix} I_\alpha \\ I_\beta \end{bmatrix} \quad \textbf{(3-11)}$$

$$\begin{bmatrix} I_\alpha \\ I_\beta \end{bmatrix} = \begin{bmatrix} cos\theta & -sin\theta \\ sin\theta & cos\theta \end{bmatrix} \begin{bmatrix} I_d \\ I_q \end{bmatrix} \quad \textbf{(3-12)}$$

The terms $-\omega L I_d$ and $\omega L I_q$ are added to the controller to provide decoupling between the 2 axes where L represents the total series inductance to the grid. Furthermore, V_d and V_q are fed forward to improve the dynamics of the controller. The sin θ and cos θ terms that are required for the dq to αβ and inverse transformations are derived from a second order generalised integrator based phase locked loop (discussed in detail in the next chapter) that is locked to the grid voltage while the imaginary terms of V_β and I_β are generated by delaying the corresponding voltage and current signals by 90°.

The stationary frame equivalent transfer function of the synchronous rotating frame PI (SRFPI) controller, $G_C(s)$ has been derived in [130, 131] as given in equation (3-13).

$$G_c(s) = k_p + \frac{k_i s^2 + 2\omega k_i s - k_i \omega^2}{s^3 + \omega s^2 + \omega^2 s + \omega^3} \quad \textbf{(3-13)}$$

Harmonic Compensator

The PI current controller has insufficient harmonic rejection capability due to the low gain at the harmonic frequencies. Therefore, cancellation of the odd harmonics in the grid current which are due to the harmonics present in the utility voltage is achieved by the placement of multiple resonant controller blocks in the feedback path of the current controller in the stationary frame. Therefore the current controller provides a very large gain at the frequencies of the cancellation. The transfer function for the harmonic compensator, $HC(s)$ is given in equation (3-14). Cancellation for the first 4 odd harmonics (150 Hz, 250 Hz, 350 Hz and 450 Hz) is designed into the controller. Harmonics beyond 450 Hz are not considered since the contribution of higher order harmonics to THD decreases with increasing harmonic number. The block diagram of the harmonic compensator is illustrated in Fig. 3-8.

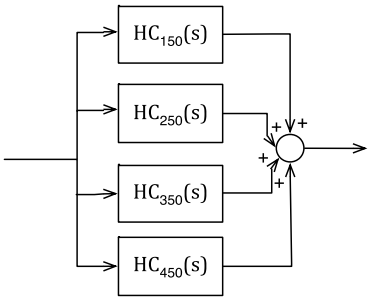


Fig. 3-8 Harmonic compensator block diagram

$$HC(s) = \frac{k_{h3}s}{s^2 + \omega_{h3}^2} + \frac{k_{h5}s}{s^2 + \omega_{h5}^2} + \frac{k_{h7}s}{s^2 + \omega_{h7}^2} + \frac{k_{h9}s}{s^2 + \omega_{h9}^2} \quad \textbf{(3-14)}$$

Plant and Controller Model

The plant of the current controller is the voltage source converter (VSC) and the LCL frontend filter. The LCL filter transfer function, $G_P(s)$ is given in equation (3-15) and the overall controller diagram is depicted in Fig. 3-9 where $D(s)$ models the delay (0.15 ms) due to the controller's digital processing as given in (3-16).

$$G_P(s) = \frac{I_g(s)}{V_{inv}(s)} = \frac{RCs + 1}{LL_gCs^3 + RC(L + L_g)s^2 + (L + L_g)s} \quad \textbf{(3-15)}$$

$$D(s) = \frac{1 - \frac{t_d}{2}s}{1 + \frac{t_d}{2}s} \quad \textbf{(3-16)}$$

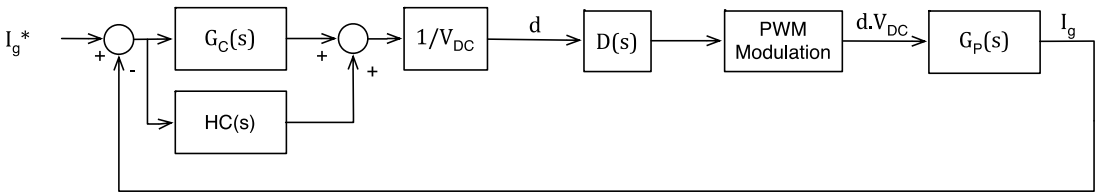


Fig. 3-9 Overall current controller diagram

Gain Selection

The proportional gain, k_p value is first set to 5 to obtain a fast rise time (<1 ms). The remaining controller gain values are iteratively selected as shown in Table 3-1 in order to get sufficient gain and phase margins (gain margin higher than 6 dB and a phase margin between 30° to 60° [169]). The open and closed loop transfer functions of the system are given in (3-17) and (3-18), respectively. The gain and phase margins for the overall current controller is 9.01 dB and 56.2° respectively and the open loop Bode plot is depicted in Fig. 3-10 while the closed loop step response is shown in Fig. 3-11.

Table 3-1 values for k_p, k_i and harmonic compensation gains

k_p	k_i	k_{h3}	k_{h5}	k_{h7}	k_{h9}
5	50	200	200	200	200

$$G_{ol} = G_P(s)D(s)[G_C(s) + HC(s)] \quad \textbf{(3-17)}$$

$$G_{cl} = \frac{G_P(s)D(s)[G_C(s) + HC(s)]}{1 + \{G_P(s)D(s)[G_C(s) + HC(s)]\}} \quad \textbf{(3-18)}$$

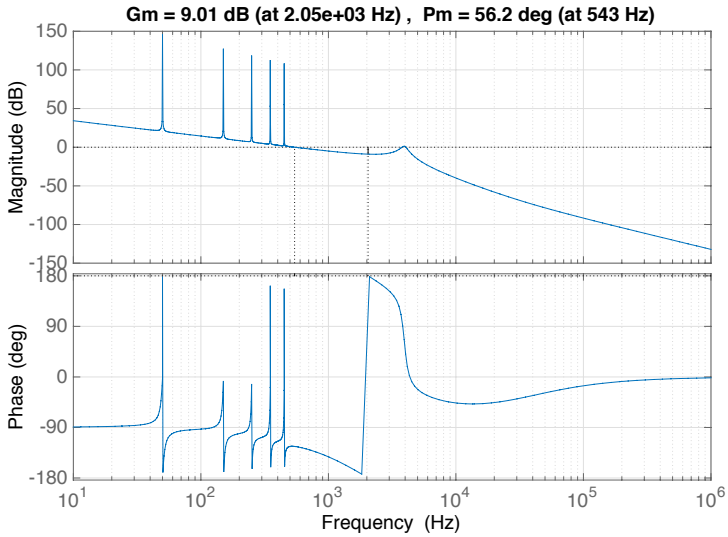


Fig. 3-10 Open loop Bode plot of SRFPI current controller

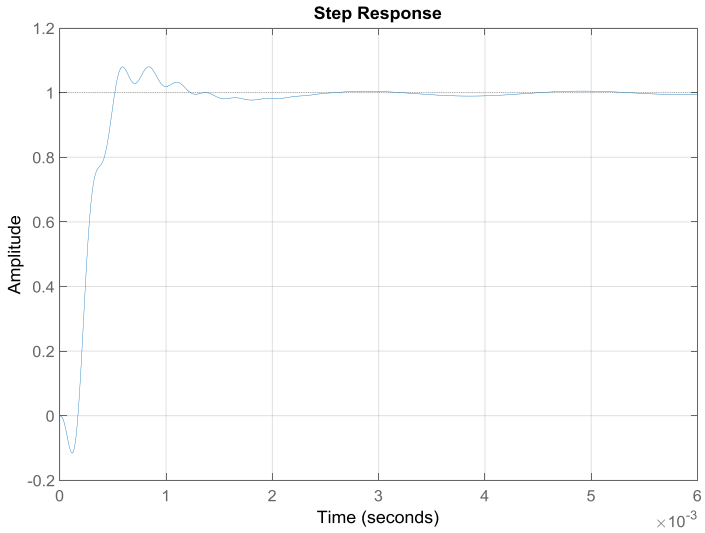


Fig. 3-11 Closed loop step response of SRFPI current controller

It can be observed from the step response that the system contains a right half plane zero due to the system's delay term, $D(s)$. From the open loop Bode plot it is apparent that the SRF PI controller acts as a resonant controller centred at 50 Hz with a large gain and therefore eliminates steady state error. Furthermore, the multiple resonances of the harmonic cancellation scheme provide the necessary gain at the harmonic frequencies that require rejection.

From the closed loop step response, it is found that the rise time and settling time of the system is 0.28 ms and 1.84 ms, respectively. Therefore it can be determined that the current controller stability, transient response as well as disturbance rejection capability meets the requirements for the application.

3.2.3. DC link voltage controller design

To design the voltage controller, the small signal response between the DC link voltage and the grid current has to be established as the output of the voltage controller determines the grid current. It can be observed that a delta change in I_g causes a delta change in the current flowing from the DC link capacitors. Therefore the small signal transfer function between I_{g_pk} and V_{DC} can be derived by considering the nominal grid voltage, the nominal DC link voltage values as well as the energy balance between the AC and DC sides of the converter as given in (3-19). The DAB current can be treated as a disturbance to the system, therefore the transfer function is defined in equation (3-20) where the voltages and currents are depicted in Fig. 3-12.

$$\frac{I_{g\_pk}(s)V_{g\_rms\_nom}}{\sqrt{2}V_{DC\_nom}} = C_{DC}sV_{DC}(s) - I_{DAB} \tag{3-19}$$

$$\frac{V_{DC}(s)}{I_{g\_pk}(s)} = \frac{V_{g\_rms\_nom}}{\sqrt{2}V_{DC\_nom}C_{DC}s} \tag{3-20}$$

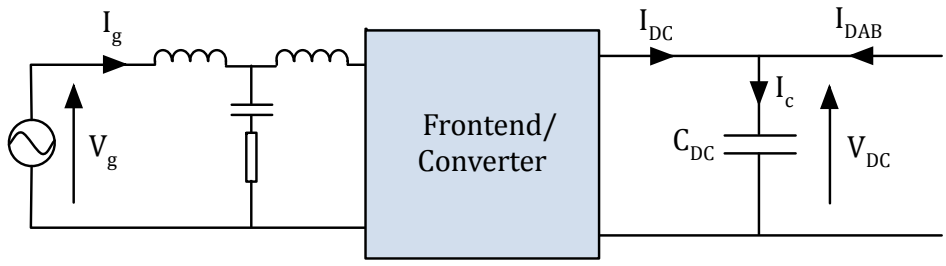


Fig. 3-12 Frontend converter and DC link capacitor subcircuit

Since the power flow waveform of a single-phase inverter takes the form of a sinusoidal pulsation at twice the grid frequency (100 Hz), the DC link voltage also contains 100 Hz voltage ripple superimposed on a DC offset. The magnitude of the DC link voltage ripple depends on the size of the capacitor, the operating voltage and the power level of the inverter. This voltage ripple typically has an undesired effect on the voltage controller as it tries to compensate for the error by controlling the grid current. This results in the modulation of the grid voltage at a frequency of 100 Hz. A few methods to ensure that the voltage controller rejects the 100 Hz error signal exists, such as low pass or band pass filtering the DC link voltage feedback signal, methods based on energy balance analysis [147, 148] and predictive methods based on energy balance [149]. The simple low pass filter based method suffers from poor transient performance whereas the energy balance and predictive methods tend to be complex to implement. An alternative method is to use a notch filter with a stop frequency of 100 Hz as reported in [110, 150]. Therefore for the voltage controller in question, a similar notch filter with a frequency of 100 Hz is utilised on the feedback path to reject only the frequency of disturbance. The block diagram of the voltage controller is depicted in Fig. 3-13 where the plant consists of the closed loop transfer function of the current controller ($G_{SRF\_CL}(s)$) followed by the transfer function of the DC link capacitor. The transfer function of the notch filter $H_{Notch\_V}(s)$ as well as the open loop controller ($H_{ol}(s)$) and disturbance transfer functions ($H_{dist}(s)$) are defined in equations (3-21)-(3-23).

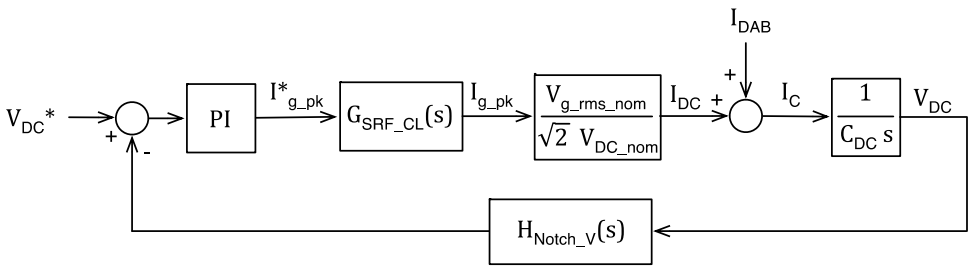


Fig. 3-13 DC link voltage controller block diagram

$$H_{Notch\_V}(s) = \frac{\omega_{h2}^2 + s^2}{\omega_{h2}^2 + s\omega_{h2} + s^2} \quad \textbf{(3-21)}$$

$$H_{ol}(s) = \left(k_p + \frac{k_i}{s}\right) G_{SRF\_CL} \frac{V_{g\_rms\_nom}}{\sqrt{2}V_{DC\_nom}C_{DC}s} H_{Notch\_V}(s) \quad \textbf{(3-22)}$$

$$H_{dist}(s) = \frac{V_{DC}(s)}{I_{DAB}(s)} = \frac{{}^{1}/_{C_{DC}s}}{1 + \left(k_p + {}^{k_i}/_{s}\right) G_{SRF\_CL} \frac{V_{g\_rms\_nom}}{\sqrt{2}V_{DC\_nom}C_{DC}s} H_{Notch\_V}(s)} \quad \textbf{(3-23)}$$

$$H_{cl}(s) = \frac{\left(k_p + \frac{k_i}{s}\right) G_{SRF\_CL} V_{g\_rms\_nom}}{\sqrt{2}V_{DC\_nom}C_{DC}s + \left(k_p + \frac{k_i}{s}\right) G_{SRF\_CL} V_{g\_rms\_nom} H_{Notch\_V}(s)} \quad \textbf{(3-24)}$$

The controller's PI gains are selected as 1 and 10 (iteratively evaluated) for k_p and k_i respectively in order to give a bandwidth of 35 Hz, gain margin of 25 dB and phase margin of 67.9°. The open loop Bode plot for the voltage controller is presented in Fig. 3-14.

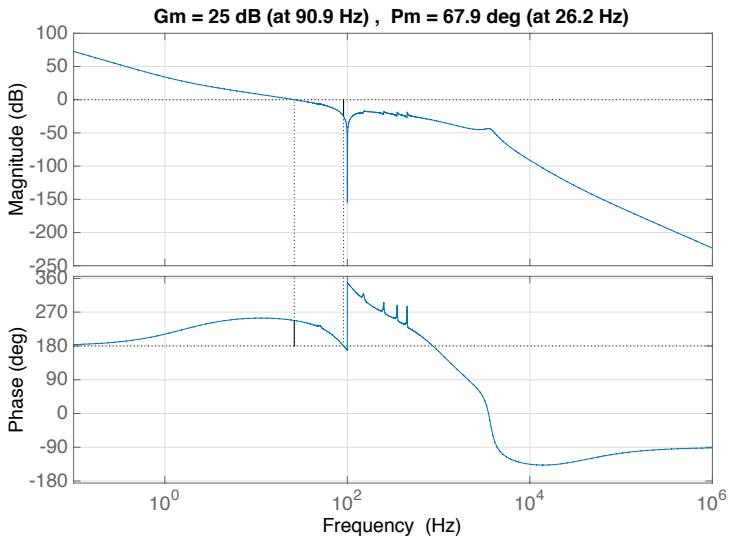


Fig. 3-14 Open loop Bode plot of voltage controller

The step response for the voltage control loop is important when the inverter initialises and the voltage is initially increased to 380 V. The start up sequence of the inverter consists of first pre-charging the DC link capacitors from the grid through the diodes in the frontend bridge. This typically charges the capacitors to approximately 340 V (peak value of grid voltage). The next stage is the initiation of the grid current controller and PWM switching followed by the activation of the DC link voltage regulation loop. Therefore, the step response characteristic for the converter initialisation can be verified with the use of the closed loop transfer function given in (3-24) and the response is shown in Fig. 3-15. It can be observed that the controller is able to achieve 380 V with minimum overshoot.

Furthermore, the disturbance rejection of the voltage controller is verified to ensure that the DC link voltage stays within an acceptable range when the DAB converter initialises. After the grid side has been initialised and the DC link is set to 380 V, the DAB converter is initialised. If the discharge mode is considered, the increase in energy in the DC link capacitors due to the DAB operation causes the DC link voltage to increase. Therefore the DAB current (I_{DAB}) presents a disturbance to the voltage controller. The disturbance transfer function has been defined in equation (3-23). Therefore, the disturbance rejection characteristic of the controller for the case when the DAB converter initialises to a power level of 2.2 kW (step) is shown in Fig. 3-16. It is evident that the voltage controller is able to regulate the DC link voltage to 380 V with minimal overshoot and a setting time of 0.17 s. Although the disturbance rejection characteristic to the step power demand has been verified, in reality the battery current is a ramp demand due to the battery charger application and hence a smaller DC link overshoot can be expected.

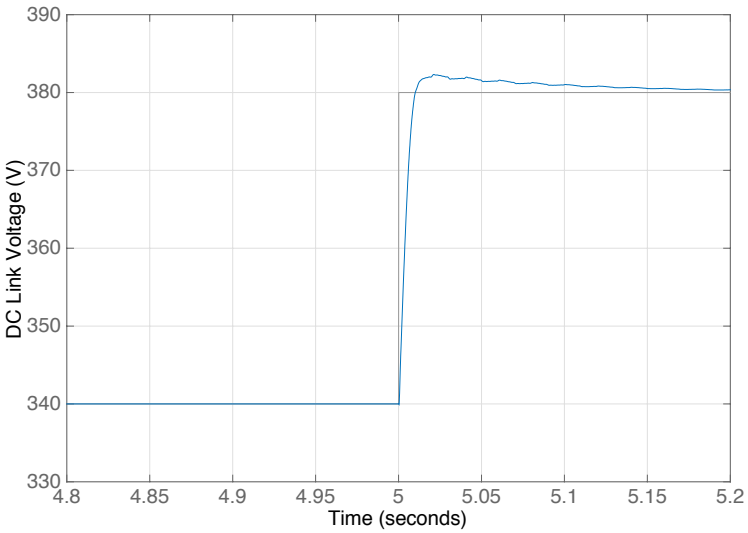


Fig. 3-15 DC link voltage controller step response during converter start-up

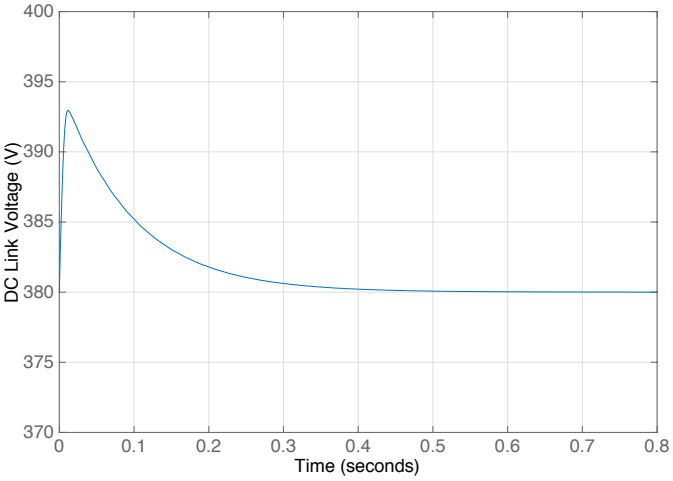


Fig. 3-16 DC link voltage controller disturbance rejection

3.3. Controller design for low frequency transformer based charger

The controller structure for the LF transformer based bidirectional battery charger is highlighted in Fig. 3-17. Two control loops form the control system for the charger. The grid current controller configuration is the same as the HF transformer based charger. The second control loop is the battery current controller whose output is the demand to the grid current controller.

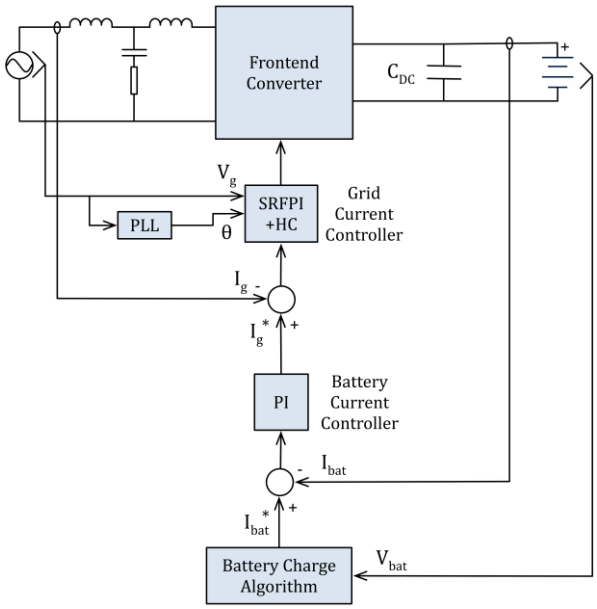


Fig. 3-17 LF transformer based charger control scheme

The SRFPI current controller gain values have been chosen iteratively to give a bandwidth of 900 Hz with a gain and phase margin of 8.99 dB and 56.5° respectively. The final gain values selected are shown in Table 3-2. The open loop Bode and closed loop step response plots are depicted in Fig. 3-18 and Fig. 3-19, respectively.

Table 3-2 values for k_p, k_i and harmonic compensation gains

k_p	k_i	k_{h3}	k_{h5}	k_{h7}	k_{h9}
20	100	100	100	100	100

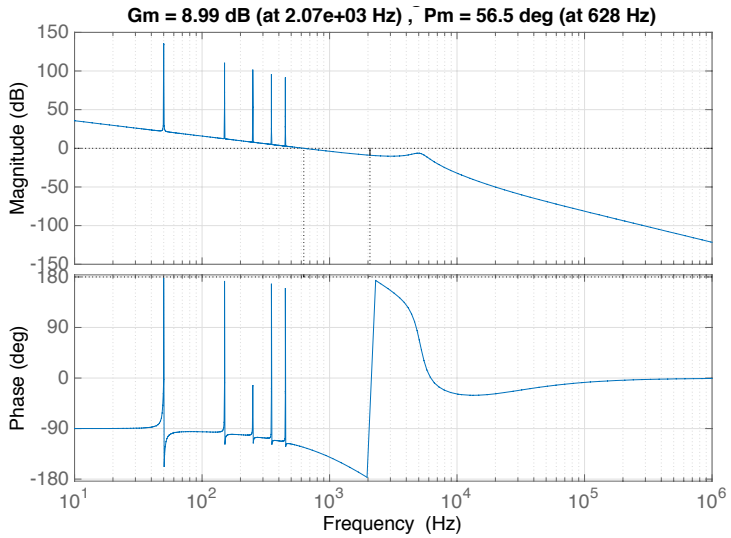


Fig. 3-18 Open loop Bode plot of SRFPI current controller

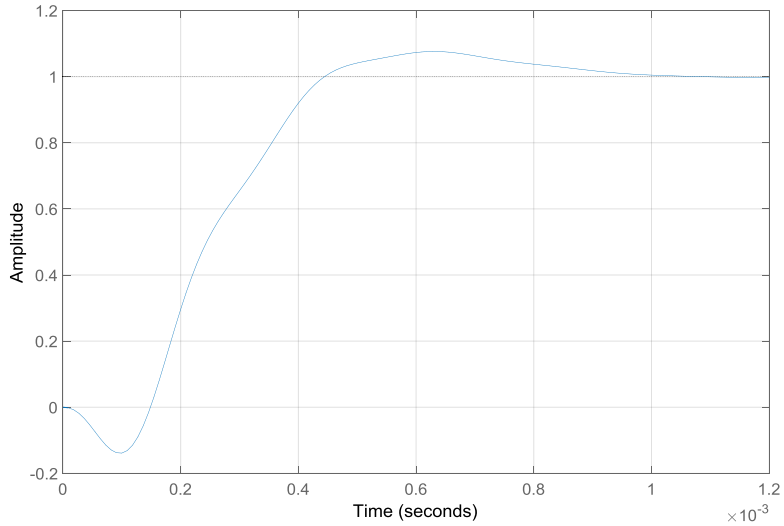


Fig. 3-19 Closed loop step response of SRFPI current controller

It can be observed from the step response that the system contains a right half plane zero, as was the case for the HF transformer based charger's SRFPI controller. Furthermore, the 50 Hz and multi resonance characteristics are also present in the open loop Bode plot as expected.

From the closed loop step response, it is found that the rise time and settling time of the system is 0.22 ms and 0.87 ms, respectively. Therefore it can

be determined that the current controller stability, transient response as well as disturbance rejection capability meets the requirements for the application.

Battery Current Controller

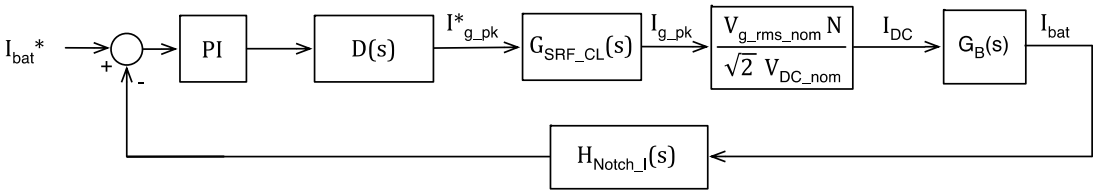


Fig. 3-20 Battery current controller diagram

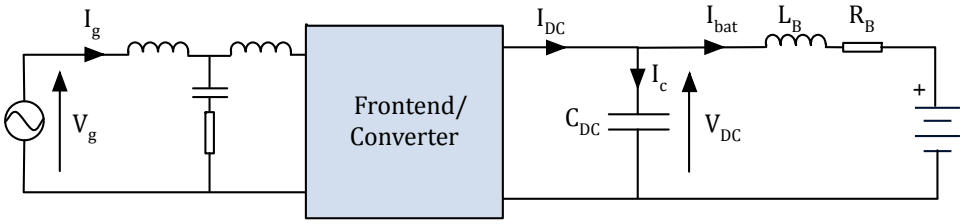


Fig. 3-21 Circuit diagram of battery charger

The structures for the battery current controller and the corresponding circuit diagrams are depicted in Fig. 3-20 and Fig. 3-21. Since the battery current contains 100 Hz ripple, the aim of the controller is to maintain the average value of the battery current in response to a demand value. Therefore the feedback signal (I_{bat}) is filtered with a 100 Hz notch filter to eliminate the current ripple. C(s) is a standard PI controller transfer function and the delay due to the discrete sampling and control update is represented by $D(s)$. $G_{SRF\_CL}(s)$ is the closed loop transfer function of the SRFPI current controller and $G_B(s)$ is the transfer function between the inverter's output current on the DC side and the battery current. $G_B(s)$ is defined in (3-25) where R_B and L_B represent the equivalent series resistance and inductance of the battery and associated wiring. The relationship between I_{g_pk} and I_{DC_ave} (average output

current on DC side) is defined as a gain by considering the energy balance between the AC and DC sides.

$$G_B(s) = \frac{I_{bat}(s)}{I_{DC}(s)} = \frac{1}{sC(R_B + sL_B) + 1} \quad \textbf{(3-25)}$$

Therefore the values for k_p and k_i are selected iteratively to be 0.2 and 100 which results in a controller bandwidth of 32 Hz and a rise time of 13.5 ms. The gain and phase margins for the controller are 20.6 dB and 84.9° respectively.

The open loop Bode plot and closed loop step response plots are depicted in Fig. 3-22 and Fig. 3-23.

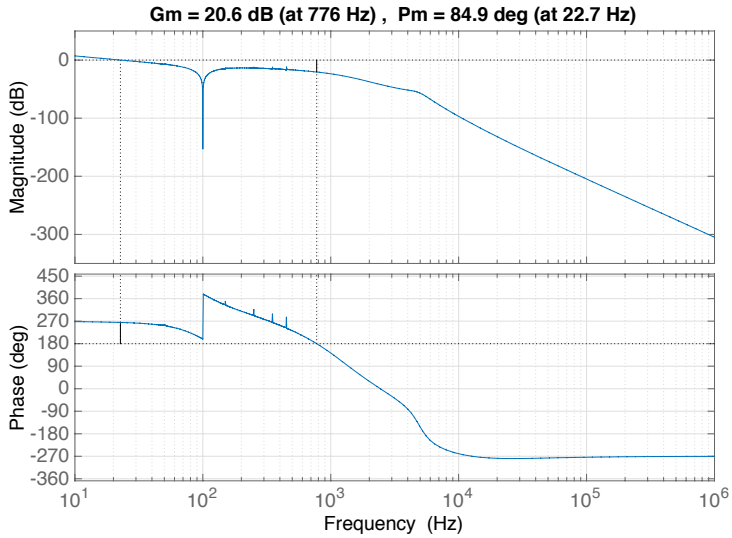


Fig. 3-22 Open loop Bode plot of battery current controller

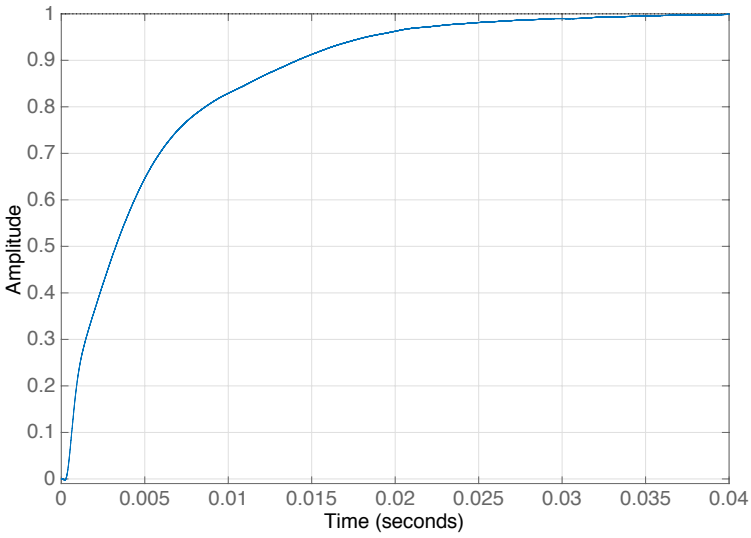


Fig. 3-23 Closed loop step response of battery current controller

3.4. Simulation studies

3.4.1. HF Transformer based bidirectional battery charging system

3.4.1.1. Simulink model of system

The control designs of the HF transformer based battery charging system are verified in simulation using MATLAB SimPowerSystems toolbox. The top-level Simulink structure of the converter is outlined in Fig. 3-24. The system is subdivided into 4 main subsystems, which are the frontend model, frontend controller, DAB model (which includes the battery model) and the DAB controller. The two controller subsystems follow the topology discussed in section 3.2. The frontend and DAB model subsystems contain the physical SimPowerSystems models of the AC/DC and DAB converters as well as the battery, respectively. The detailed Simulink block diagrams are presented in Appendix A.

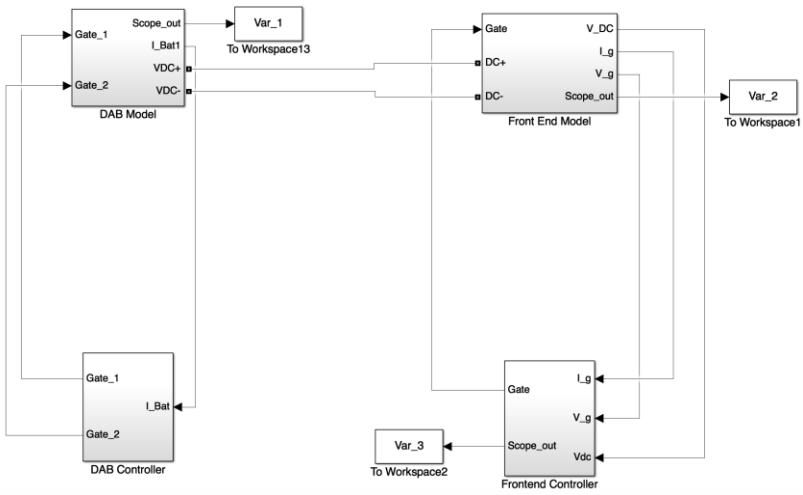


Fig. 3-24 Top-level Simulink structure of converter

3.4.1.2. Charge mode simulation

The first simulation case for the system is the charge mode operation (G2V) for the conditions as given in Table 3-3.

Table 3-3 Simulation conditions

Parameter	Value
Grid voltage	240 V
Battery voltage	120 V
Grid current (RMS)	9.16 A
Average battery current	18.33 A
Power level	2.2 kW

Initially the DAB converter is disabled, and the DC link voltage is established through the sequence described in section 3.2.3. A battery demand current step of 18.33 A is applied when the DC link voltage control has reached steady state at simulation time of 0.6 s. The resulting response of the DAB output current is presented in Fig. 3-25. It can be seen that the battery output current follows the demand as expected from the controller design. The ripple

in the output current consists of the 40 kHz switching component with a peak-to-peak magnitude of 1 A. The attenuation of the high frequency ripple occurs due to the series inductance of the battery and associated connection wiring which has been taken as 1 µH for the simulation. Further attenuation of the ripple is possible with the addition of a small value inductor. For instance, an inductor with a value of 10 µH presents an impedance of 2.5 Ω at 40 kHz. The waveforms of the DAB transformer primary and secondary voltages V_p and V_s, and the primary current i_L are depicted in Fig. 3-26. It can be observed that the DAB converter operates under ZVS condition since $i_L(0) < 0$ and $i_L(\delta) > 0$.

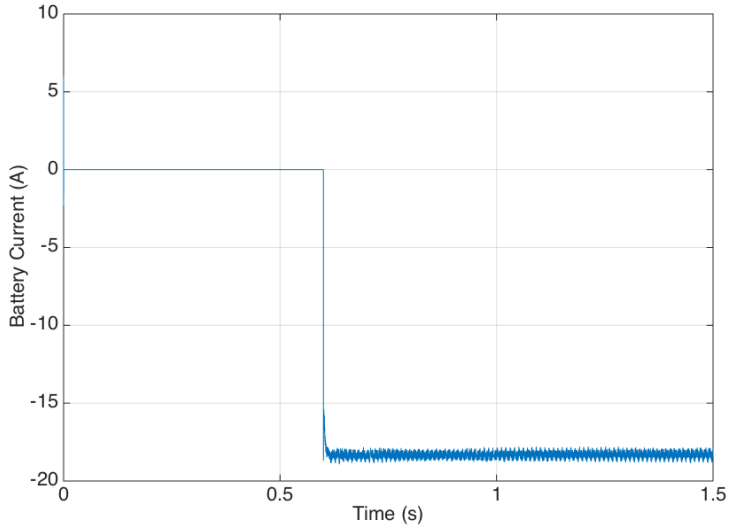


Fig. 3-25 Battery current (DAB output) step response for charge mode

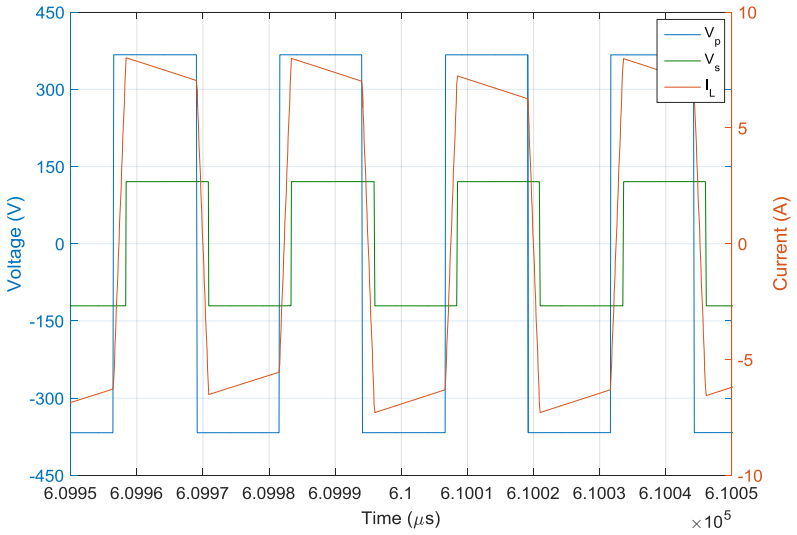


Fig. 3-26 - DAB converter transformer primary and secondary voltages and primary current

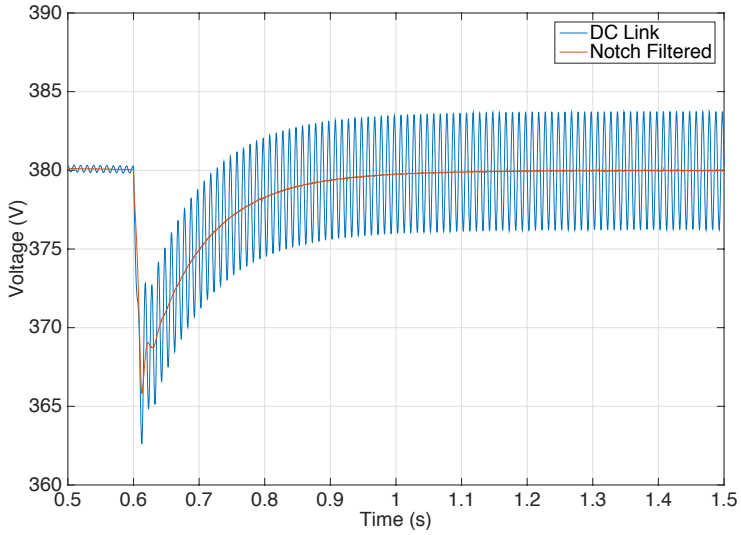


Fig. 3-27 - DC link voltage stabilisation after DAB charge initiation

The step change in battery current causes the DC link voltage to drop as shown in Fig. 3-27. Therefore, the DC voltage controller responds by applying a step demand on to the SRFPI current controller. The resultant grid voltage and current waveforms are shown in Fig. 3-28.

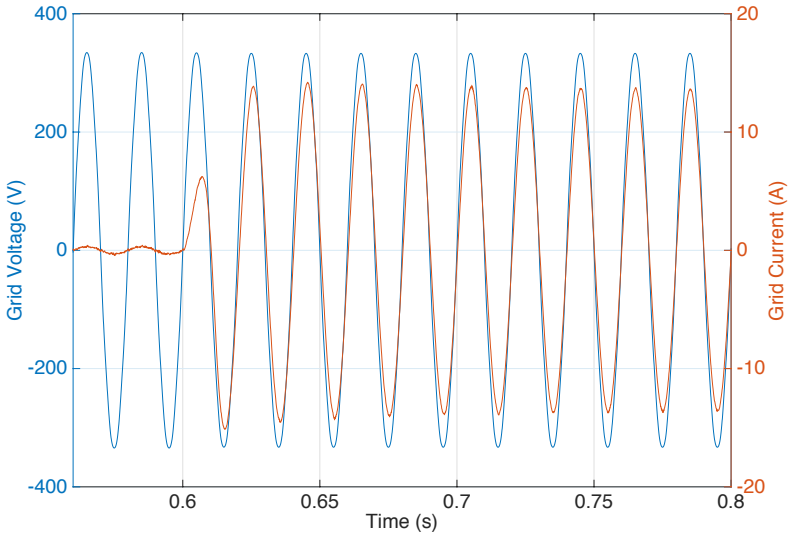


Fig. 3-28 - Grid voltage and grid current (charge mode)

It can be observed that the DC link voltage regulation loop is sufficiently fast in its response to maintain the set point of 380 V with a minimum voltage drop of 15 V. Similarly, the grid current regulation loop dynamic response is adequately fast and results in a stable operation. It should be noted that a step demand on the charge current represents a worst-case scenario. In most applications, a ramp demand would be acceptable, and the resultant voltage deviation would be much smaller.

3.4.1.3. Discharge mode simulation

The conditions used for the discharge mode (V2G) simulation are the same as that for the charge mode operation. It can be observed that the battery current step response is similar to that of the charge mode except for the polarity, as depicted in Fig. 3-29. Furthermore, the DAB transformer voltage and current waveforms are depicted in Fig. 3-30. In the discharging mode, the DAB transformer secondary voltage is leading that of the primary voltage, and consequently, the power is transferred from the battery to the DC-link.

The voltage controller transient response to the energy transfer from the battery is depicted in Fig. 3-32 and the resulting step increase in grid current is shown in Fig. 3-31. In addition, the disturbance rejection characteristic of the DC-link voltage controller is plotted in Fig. 3-32 for comparison with that predicted by the transfer function model presented in section 3.2.3. It can be seen that the transfer function based model follows closely with the Simulink switching model. Again, it should be noted that the step demand on the battery discharging current is not necessary in real applications. With a ramp demand, the resultant DC link voltage deviation would be much smaller.

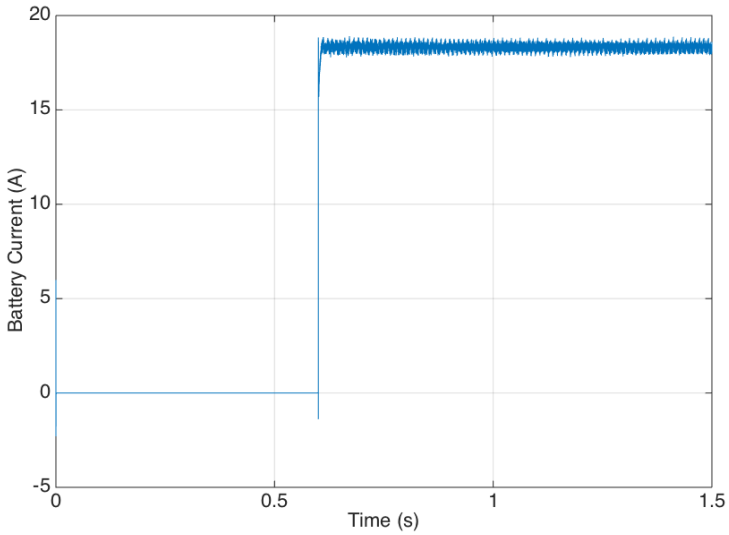


Fig. 3-29 Battery current (DAB output) step response for discharge mode

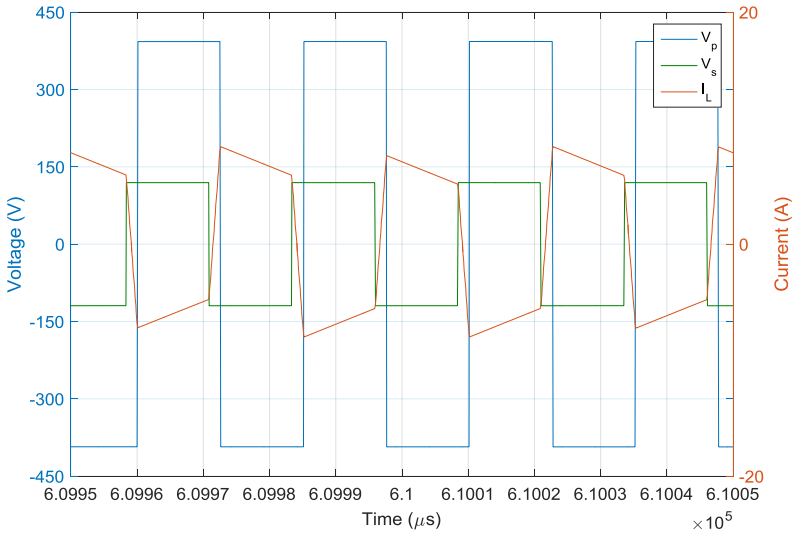


Fig. 3-30 DAB converter transformer primary and secondary voltages and primary current

Therefore from the simulation results for charge and discharge modes that were obtained, it can be concluded that the HF TF based charger and its accompanying controllers operates as expected.

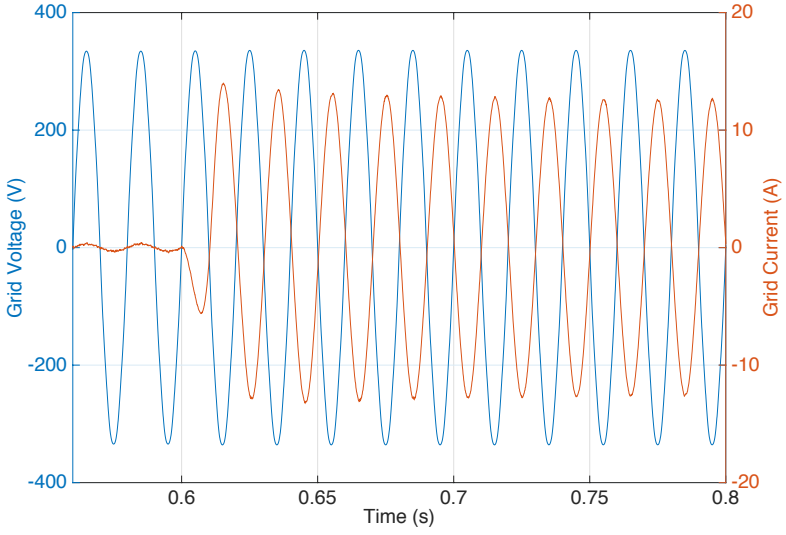


Fig. 3-31 - Grid voltage and grid current (discharge mode)

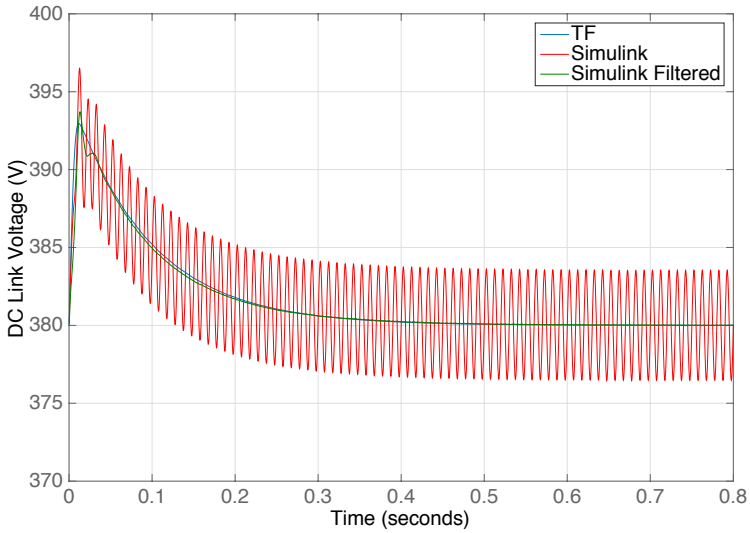


Fig. 3-32 - DC link voltage stabilisation after DAB initiation compared with transfer function

3.4.1.4. Harmonic compensator performance

The performance of the harmonic compensation of the SRFPI controller has been verified by simulating the system with and without the HC block enabled when the grid voltage is highly distorted (10% THD). Fig. 3-33 (a) and (b) shows the harmonic spectrum of the grid voltage and the harmonic spectrum of the grid current for the cases of with and without the HC block enabled for both charge and discharge modes. It can be observed that the THD of the current with the HC block reduces from 3.68% to 1.47% for charge mode, and from 6.35% 1.88% in discharge mode. It can be seen that the odd harmonics of 3rd to 9th has been reduced. The lower order harmonics are attenuated more due to the higher gain that is present in the controller at lower frequencies as was apparent from the transfer function Bode characteristics.

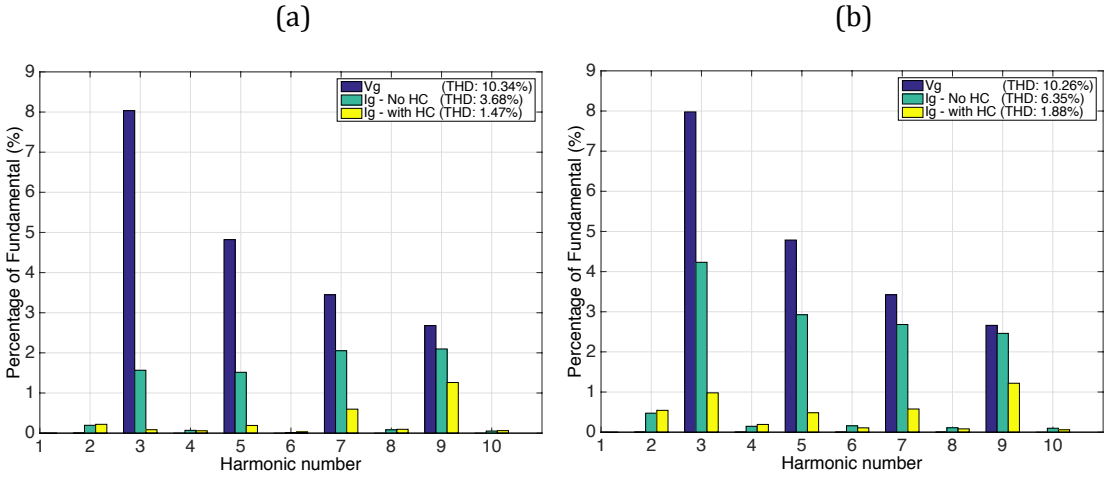


Fig. 3-33 Harmonic compensator performance. (a) Charge mode. (b) Discharge mode.

3.4.2. LF transformer based charger simulation

The charge and discharge simulation conditions for the LF transformer based system are the same as the conditions for the HF transformer based charger, which has been given in Table 3-3. The Simulink model of the charger system consists of the AC/DC converter physical model and battery model in SimPowerSystems and the controller subsystem containing the two control loops discussed in section 3.3. The detailed Simulink block diagrams are presented in Appendix B.

3.4.2.1. Charge mode simulation

The actual battery current and the current controller's notch filtered waveforms for charge mode operation are depicted in Fig. 3-34. The main component of the battery current waveform is 100 Hz as the battery presents a low impedance path for the 100 Hz voltage ripple on the DC link capacitors. This results in sinusoidal charging of the battery as discussed in Chapter 2. The

battery current is composed of a DC component of 18.3 A, and an additional 100 Hz component of 12 A rms. The heating effect introduced in the battery due to both the DC and the AC components of the current is 11.5 W as opposed to 8 W if it were to be purely DC charging (based on the battery specification of 24 mΩ ESR for the 80 Ah battery pack mentioned in Chapter 2 and assuming the battery impedance is the same at 100 Hz). Since the battery charge current is 22% of the rated ampere-hour rating of the battery, it can be concluded that the extra heating due to the AC component of the battery current does not cause any significant degrading effect.

It is evident that the notch filtered signal of the battery current and hence the average battery current step response has a fast rise time with no overshoot.

The output of the battery current controller, which is the grid current demand and the resulting change in grid current, is depicted in Fig. 3-35. It is evident that the SRFPI controller is able to track the demand grid current with a fast response time.

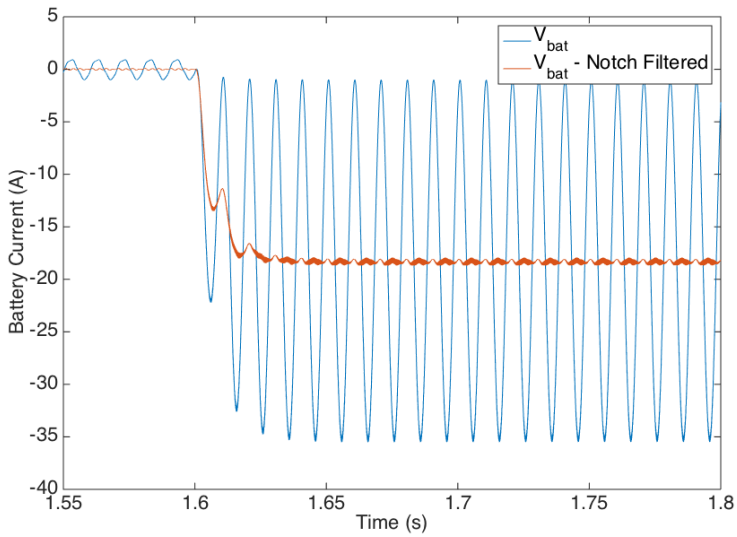


Fig. 3-34 Battery current for charge mode (notch filtered current shown for reference)

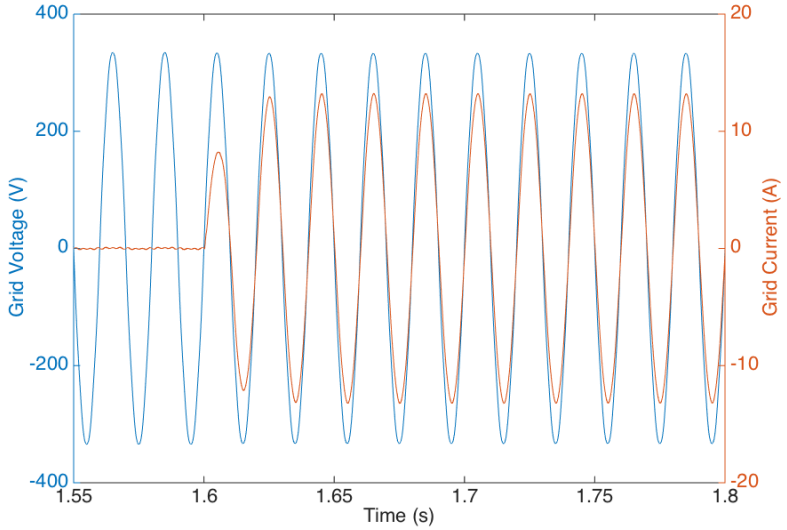


Fig. 3-35 - Grid voltage and current step response to charge initiation

3.4.2.2. Discharge mode simulation

The discharge mode waveforms for the LF charger follow the same dynamic response characteristics as the charge mode waveforms. The waveforms are presented in Fig. 3-36 and Fig. 3-37 for completeness.

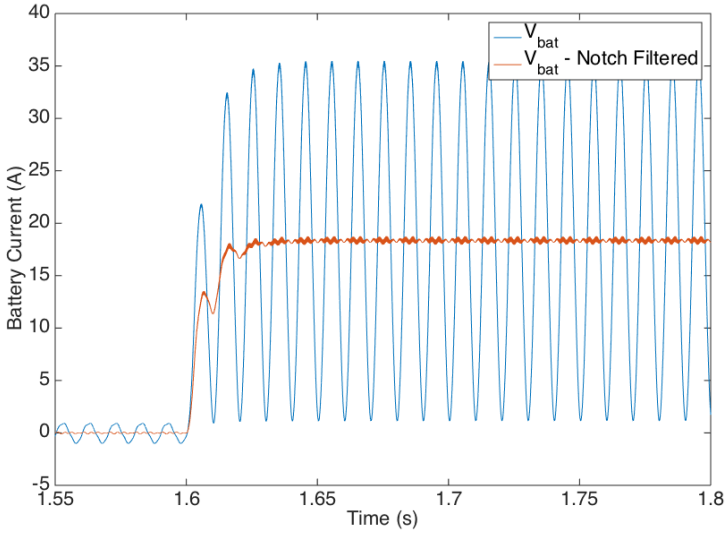


Fig. 3-36 Battery current for discharge mode (notch filtered current shown for reference)

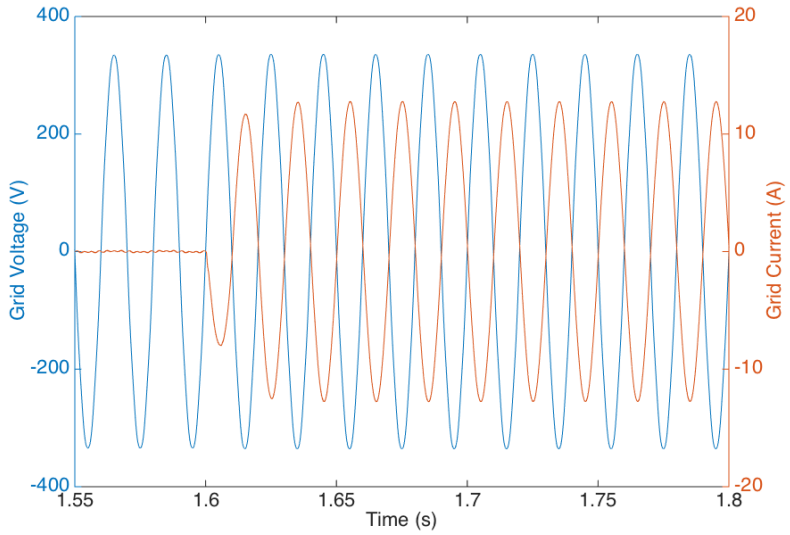


Fig. 3-37 - Grid voltage and current step response to discharge initiation

3.4.2.3. Harmonic compensator performance

The LF transformer based charging system simulation with the 10% THD grid voltage reveals that the performance of the harmonic compensator is similar to those of the HF transformer based system. The resulting harmonic spectra for charge and discharge operation are depicted in Fig. 3-38 (a) and (b). It can be seen that the compensator reduces the THD of the grid current from 4.38% to 2.35% in charge mode, and from 4.47% to 2.41% in discharge mode.

(a) (b)

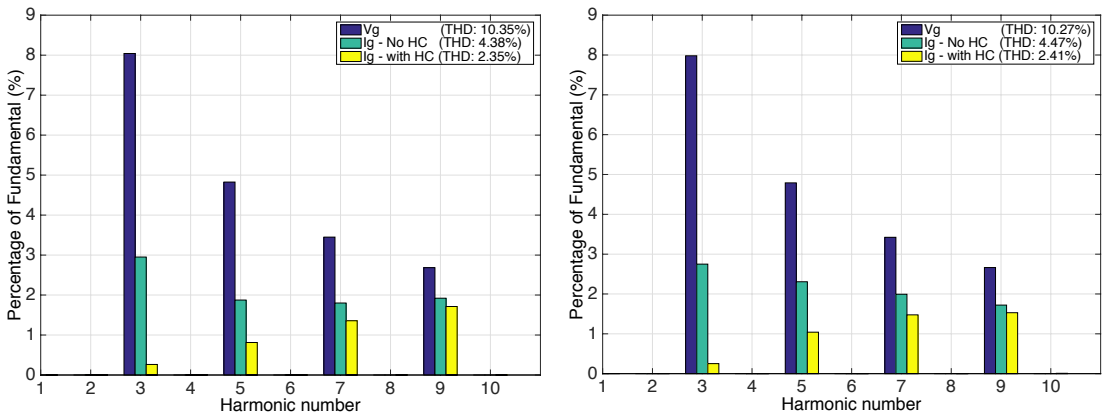


Fig. 3-38 Harmonic compensator performance. (a) Charge mode. (b) Discharge mode.

3.5. Hardware design and setup

This section describes the hardware design and setup that has been developed for demonstrating the operation of the two types of charger systems.

HF-TF Based Charger

Due to project constraints, an LLC resonant type converter (LLC converter resonant component design done by C. Gould) was used for the hardware tests for the HF-TF based charger. The difference between the DAB based system that was discussed and the LLC resonant converter lies in the addition of an LLC resonant tank between the two active bridges of the converter. The LLC consists of a series capacitor, a series inductor and a parallel inductance (transformer magnetising inductance). The primary side bridge is controlled with a 50% duty cycle modulation with variable frequency to achieve current control while the secondary side bridge is not actively switched (diode rectification). Therefore, the overall converter topology is similar to the HF transformer based system that has been designed except that the DAB stage is replaced by a resonant converter in the actual prototype system.

Since the design and analysis of the LLC converter is beyond the scope of this thesis, the results presented in section 3.6.1 focuses only on the operation of the grid side frontend of the HF-TF based charging system. Fig. 3-39 and Fig. 3-40 show the topside and the bottom side of the PCB that was designed and assembled for the system (the gate drive PCBs, resonant inductor and resonant transformer designed by C. Gould). The circuit schematics for the charger board are presented in Appendix C. The overall charger system is depicted in Fig. 3-41 (the gate drive PCBs, analogue signal conditioning PCB, resonant inductor and resonant transformer designed by C. Gould).

A National Instruments (NI) cRIO-9082 (Xilinx Spartan 6 FPGA and Intel i7 platform) has been used as the controller for the HF-TF based system. The control code is implemented on the FPGA while the real time processor is used

for monitoring purposes. The front panel interface for the LabView controller is depicted in Fig. 3-42.

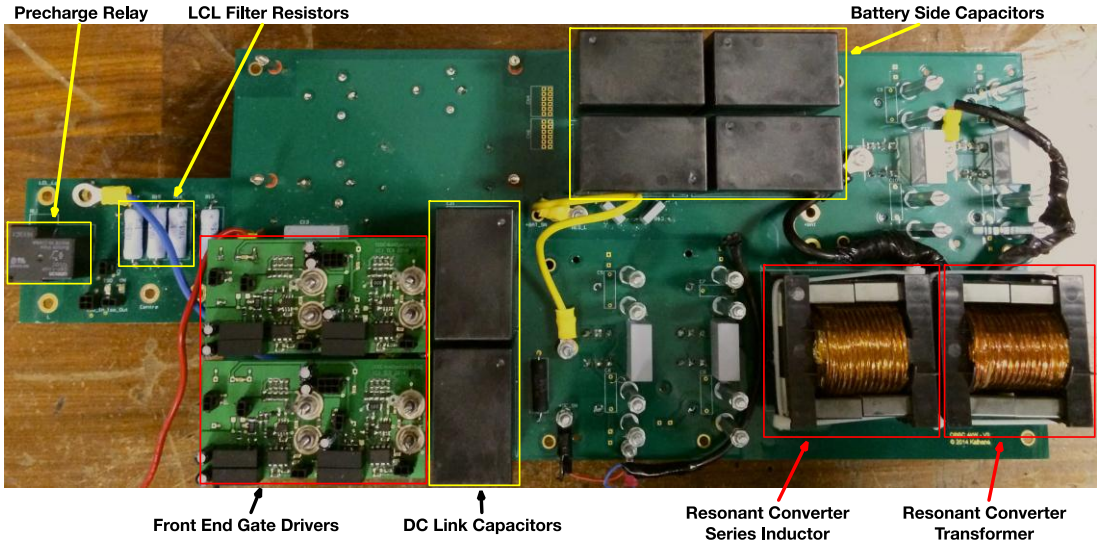


Fig. 3-39 HF-TF based charger PCB topside

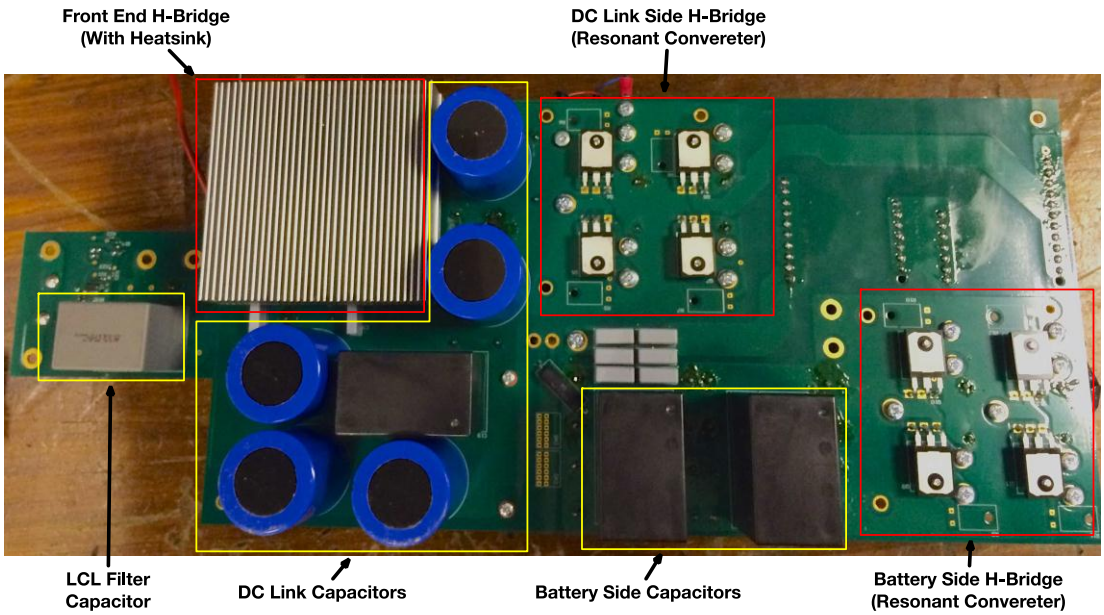


Fig. 3-40 HF-TF based charger PCB bottom side

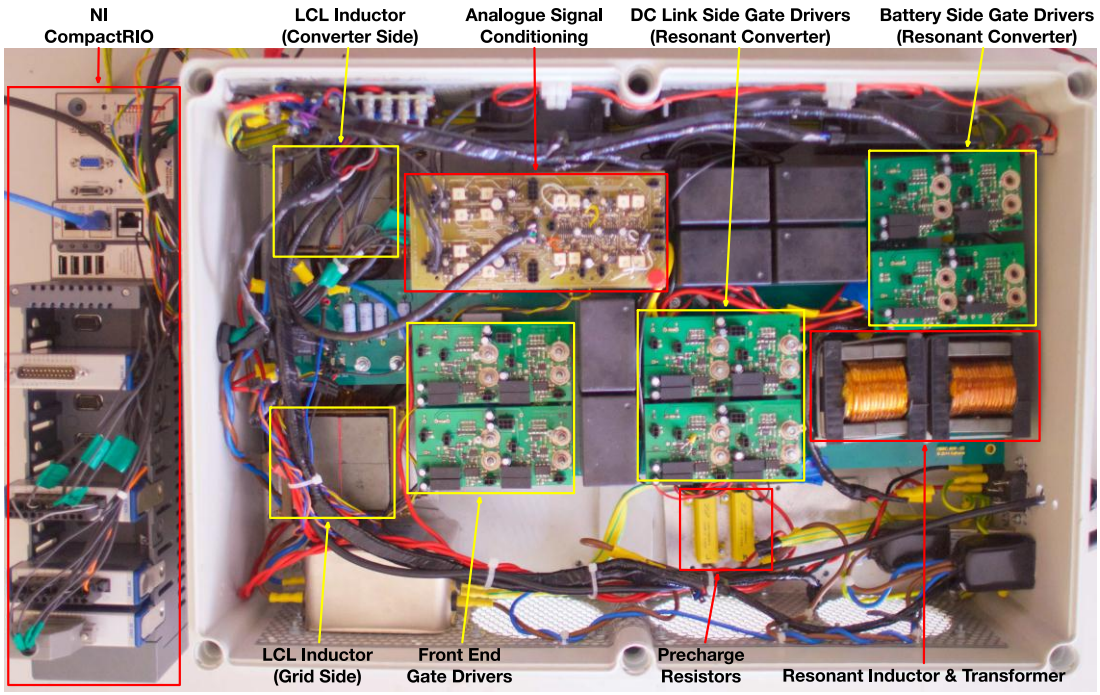


Fig. 3-41 HF charger system

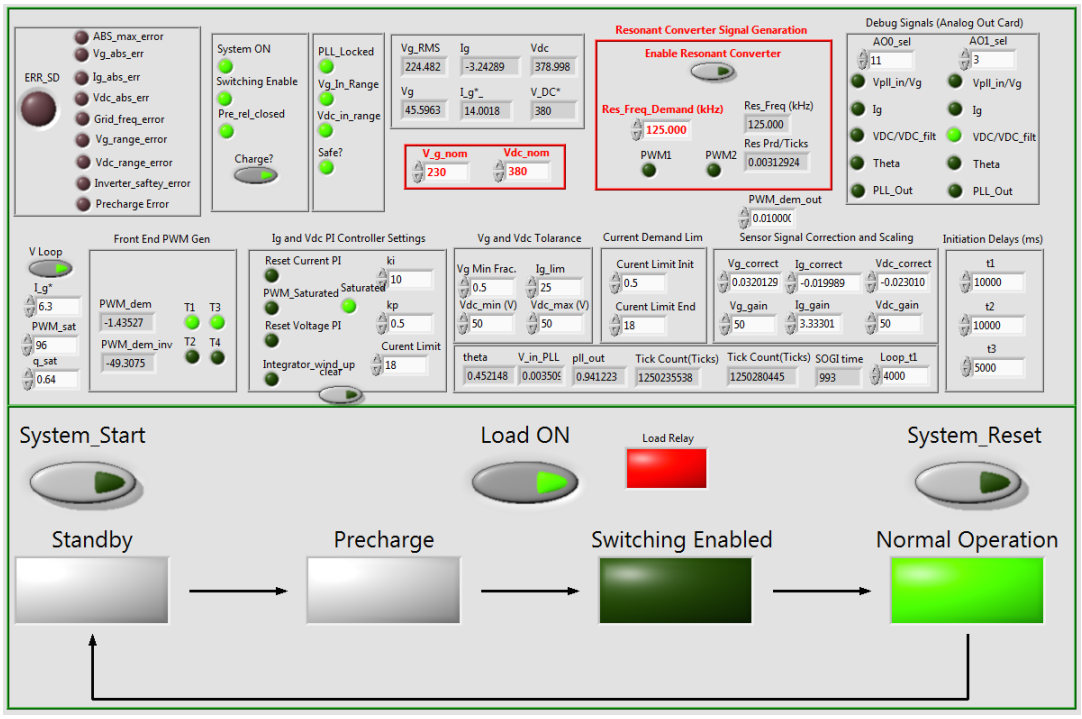


Fig. 3-42 LabView FPGA front panel interface of controller

LF-TF Based Charger

The hardware setup that was used for demonstrating the low frequency transformer based charger is depicted in Fig. 3-43. The charger consists of the motor drive inverter (designed and manufactured by Siemens); low frequency transformer and grid side LCL filter components (built to the specification as described in Chapter 2). The motor and isolating relay has not been used for the experimental demonstration. The absence of a motor does not affect the experimental validation as the isolation relay that is in the charger design fully isolates the 2 legs of the H-bridge that is used for the transformer connection from the motor terminals, whereas the 3rd motor connection has no current return path (as well as the 3rd leg of the inverter not being switched).

The control card containing the microcontroller and sensor analogue signal conditioning circuitry has been custom designed and assembled and is shown in Fig. 3-44 and Fig. 3-45. A Texas Instruments RM46L852 (Dual lockstep ARM Cortex R4F at 220 MHz) MCU has been used as the processor.

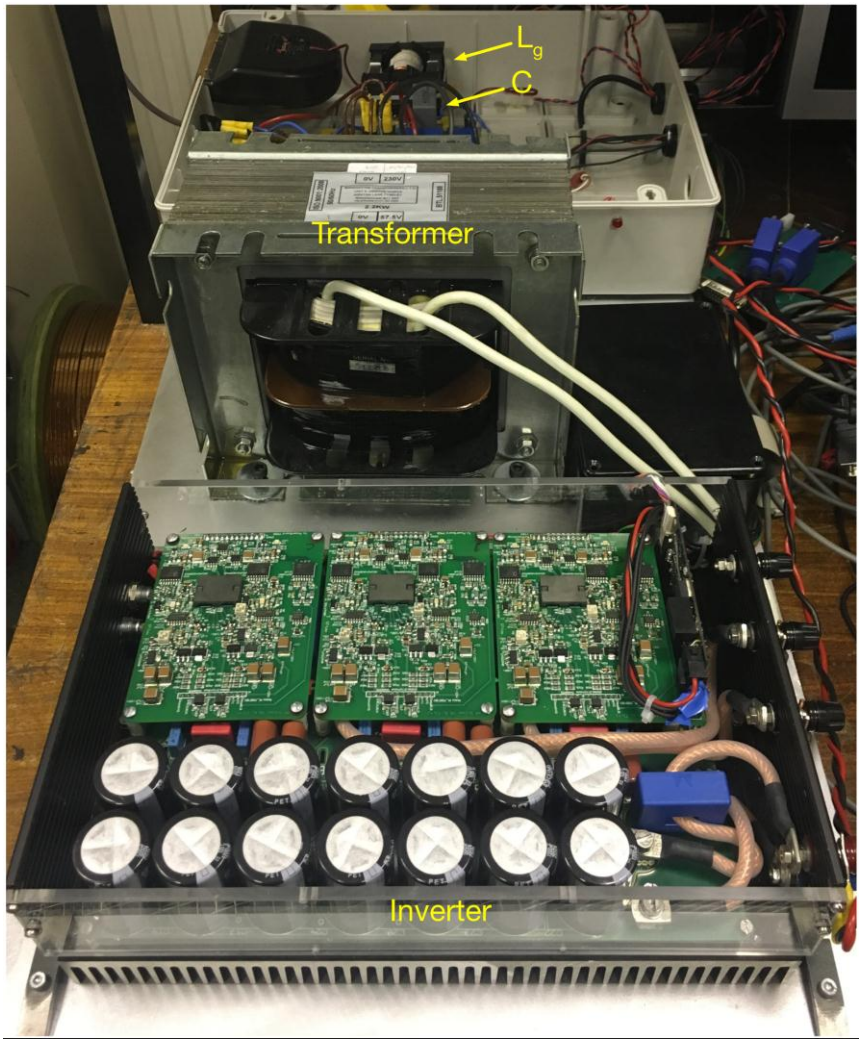


Fig. 3-43 Low frequency transformer based charger hardware setup

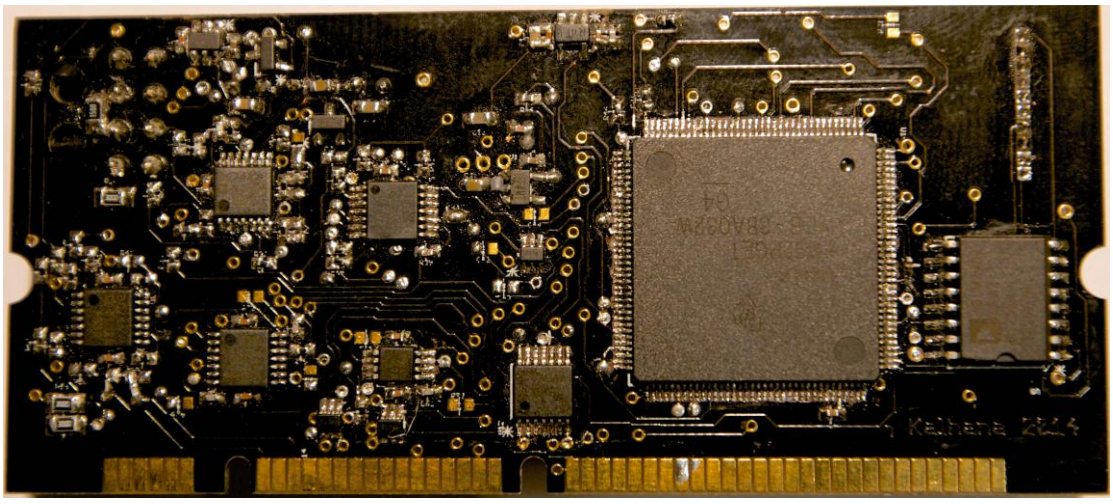


Fig. 3-44 Control card PCB top side

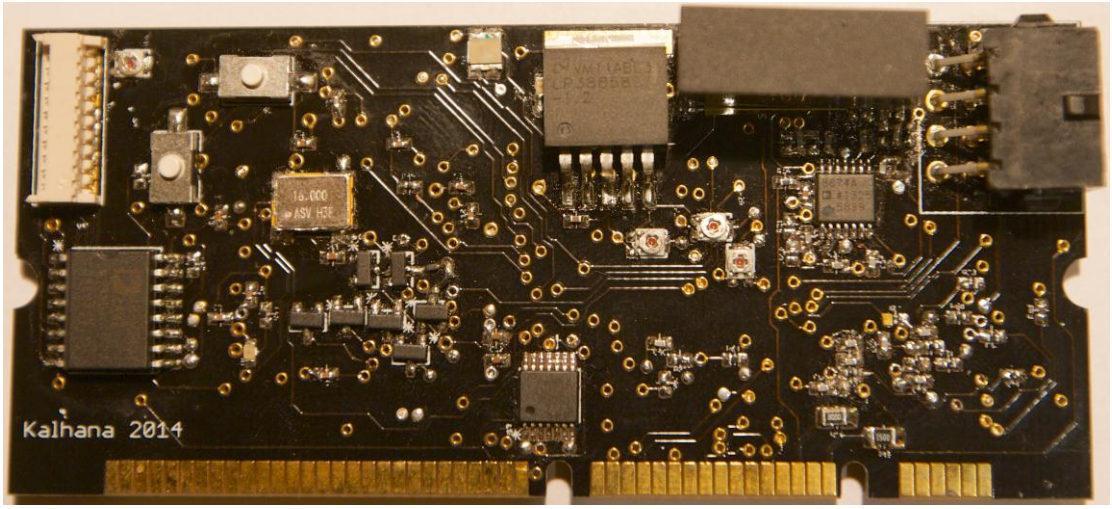


Fig. 3-45 Control card PCB bottom side

The control card is interfaced to the motor drive inverter (which serves as the battery charger). The control card generates the PWM signals for the IGBT devices in the inverter and also contains the analogue signal conditioning circuits (anti aliasing filters and signal scaling) for the sensor feedback signals. The sensor signals are thereafter digitised through the on board analogue to digital converter (ADC) of the CPU. The CPU code consisting of the control scheme illustrated in Fig. 3-17 is implemented in 'C'.

3.6. Experimental results and discussion

3.6.1. HF-TF based charger experimental results

Charge Mode Results (G2V)

In this section, the experimental test results for the HF-TF based charger's grid side operation are presented. The charge mode testing is performed with a resistive load on the DC/DC converter output.

The resonant converter acts as the load for the DC link. The sequence of operation initiates with the pre-charging of the DC link capacitors through the pre-charge resistor. The pre-charge sequence completes once the DC link voltage rises to above ~340 V after which the pre-charge relay closes thereby shorting out the pre-charge resistor.

The next stage of operation is the start of PWM switching operation of the frontend converter. Thereafter, the voltage control loop maintains 380 V on the DC link by controlling the grid current demand to the SRFPI controller.

The power flow begins when the resonant converter is activated in charge mode operation (with a resistor load bank on the output terminals) at 2.2 kW, which causes the DC link voltage to decrease as the stored energy in the capacitors is depleted. This fall in voltage is quickly compensated by the voltage controller by driving the grid current to the 9 A required to maintain 2.2 kW power flow and a 380 V DC link voltage.

The transient response waveform of the grid current is presented in Fig. 3-46. It can be seen that the SRFPI controller is able to increase the grid current to the required level in approximately 1 cycle. The response time is dominated by the DC link voltage control loop's bandwidth.

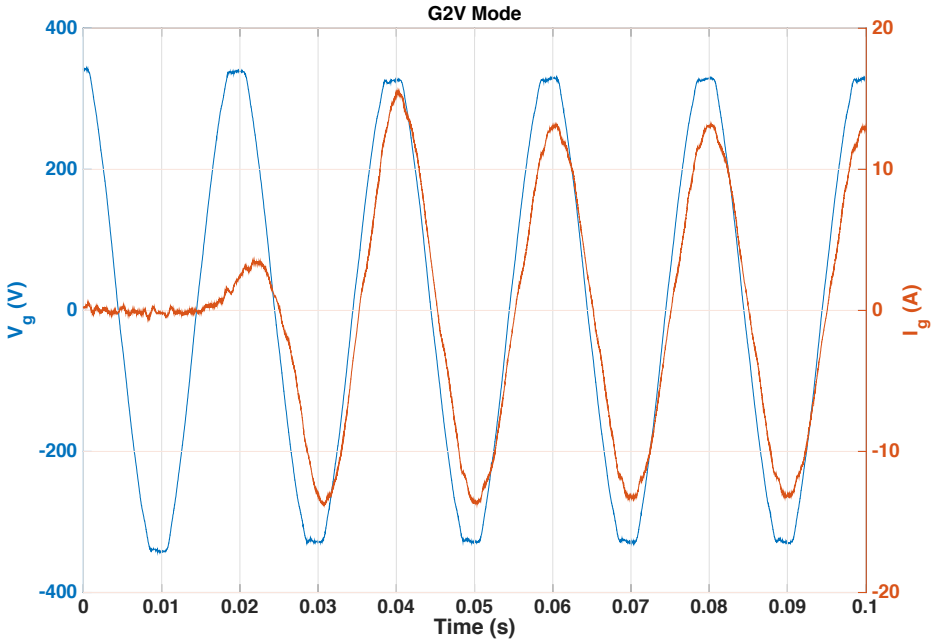


Fig. 3-46 Charge mode, transient response - grid voltage and current

Fig. 3-47 depicts the oscilloscope waveforms that were captured at steady state operating condition. It can be observed that the controller performs in a stable manner.

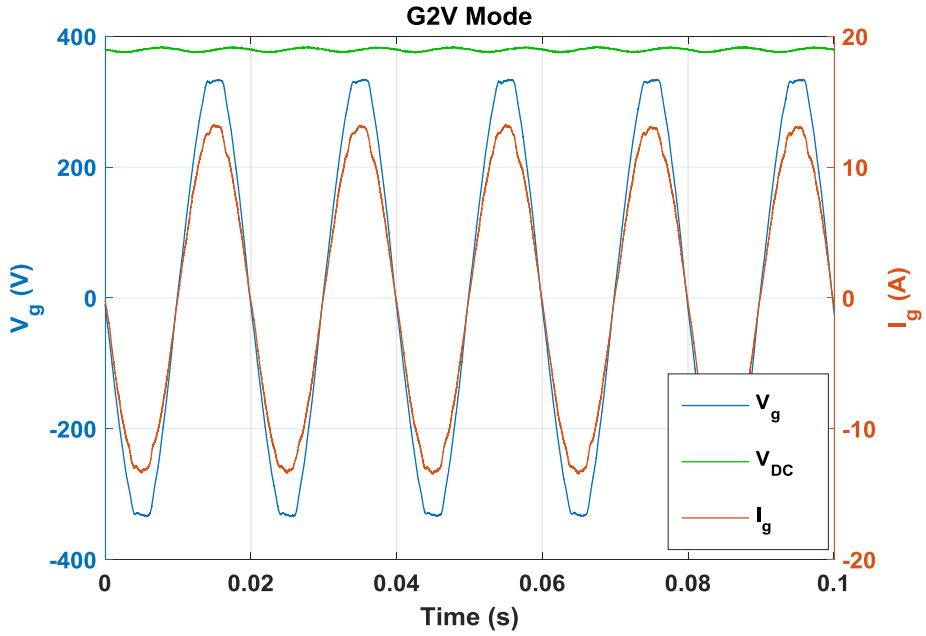


Fig. 3-47 Charge mode, steady state operation - grid voltage, DC link voltage and grid current (2.2 kW)

The primary side bridge output voltage as well as the primary (LC tank) current of the resonant converter is depicted in Fig. 3-48. It can be seen that the resonant tank current has a discontinuity as the resonant converter is operating at 120 kHz which is below the resonant frequency of 128 kHz in order to operate at the power level of 2.2 kW. The output voltage of the resonant converter (connected to a resistor load bank) is 240 V and the output current is 9.1 A.

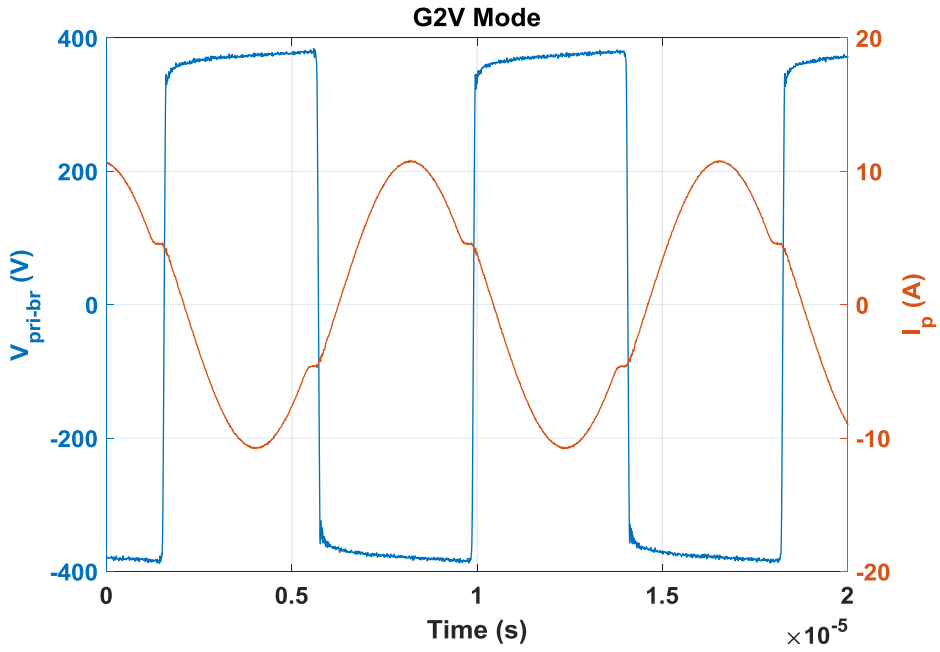


Fig. 3-48 Charge mode, steady state operation - primary side bridge output voltage and primary (LC tank) current of the resonant converter (2.2 kW, 120 kHz switching frequency)

Discharge Mode Results (V2G)

The discharge mode test has been carried out under the same power level (2.2 kW) and grid conditions as the charge mode test.

The initialisation of the converter follows a similar sequence to the charge mode. The DC link is first pre-charged to ~340 V though the pre-charge resistors, after which the relay is closed and the PWM modulation is started. The DC link voltage controller regulates the DC link voltage to 380 V. In the final

step of the initialisation, the resonant converter's power flow is increased from 0 (idle) to 2.2 kW in the reverse mode (input side of resonant controller connected to DC power supply). This results in the increase of DC link capacitor voltage due to the flow of power and the voltage controller responds by increasing the grid current demand to the SRFPI current controller.

The obtained waveforms are shown in Fig. 3-49 where the blue waveform is the grid voltage, the green waveform is the DC link voltage and the red waveform is the grid current. Similar to the charge mode, it is seen that the V2G mode operation of the converter is stable.

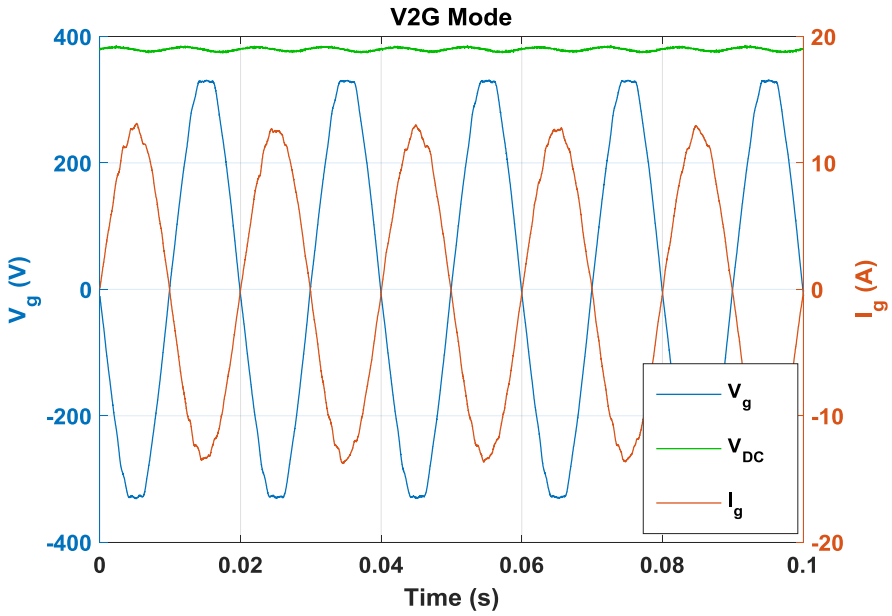


Fig. 3-49 Discharge mode, steady state operation - grid voltage, DC link voltage and grid current (2.2 kW)

Validation of Harmonic Compensator in Hardware

The performance of the harmonic compensator can be validated in hardware by comparing the distortion with and without the HC block enabled. Fig. 3-50 depicts the summary of the HC performance validation for both charge and discharge tests at the nominal power of 2.2 kW. It can be observed that the THD has decreased from 6.66% to 1.9% in charge mode, and from 5.29% to

1.98% in discharge mode operation when using the harmonic compensation. Therefore the HC makes a significant improvement to the power quality in terms of conforming to the 5% THD limit set out by the IEEE 519 standard. Furthermore, the 3rd harmonic exceeds the IEEE 519 limits for individual harmonics (4% individual harmonic distortion limit up to 10th harmonic) when the harmonic compensator is not enabled.

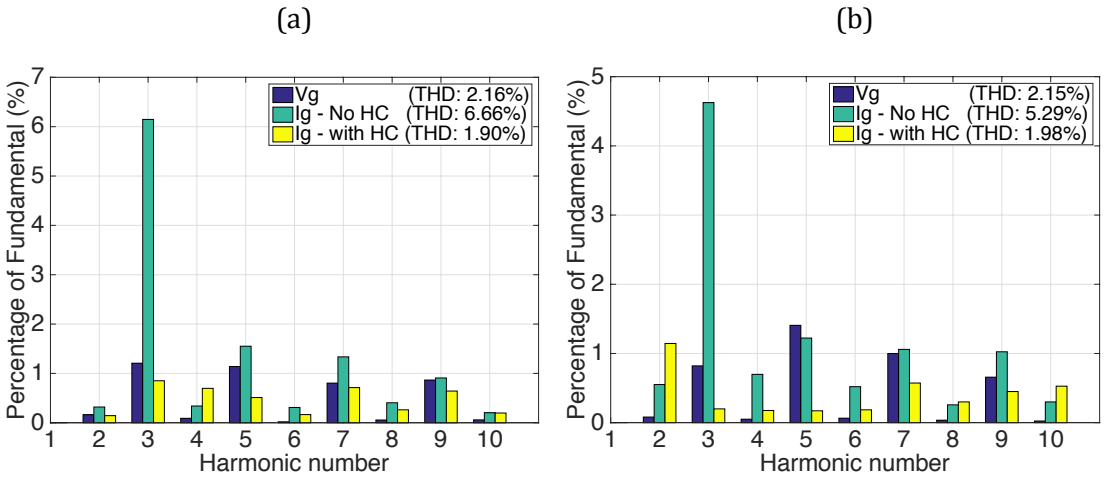


Fig. 3-50 Harmonic compensator performance experimental results (a) Charge mode. (b) Discharge mode.

Fig. 3-51 shows the harmonic compensator simulation results discussed in section 3.4.1.4 as a comparison to the experimental results. The simulation study was carried out under a grid voltage THD of 10.3% whereas in the experimental validation, the grid voltage THD was 2.1%. It can be seen that during experimental demonstration, the ratio between the grid current (with harmonic compensator disabled) and grid voltage THD is higher than the simulation case. This is attributed to the non-linearity of the magnetic components (LCL filter inductors) due to the saturation effects that cause low order harmonic distortion in the grid current [151]. Despite this, the experimental validation shows effective THD reduction when the harmonic compensator is activated (71% and 62% reduction in THD for charge and

discharge modes respectively which compares to 60% and 70% reduction for the charge and discharge modes of the simulation results).

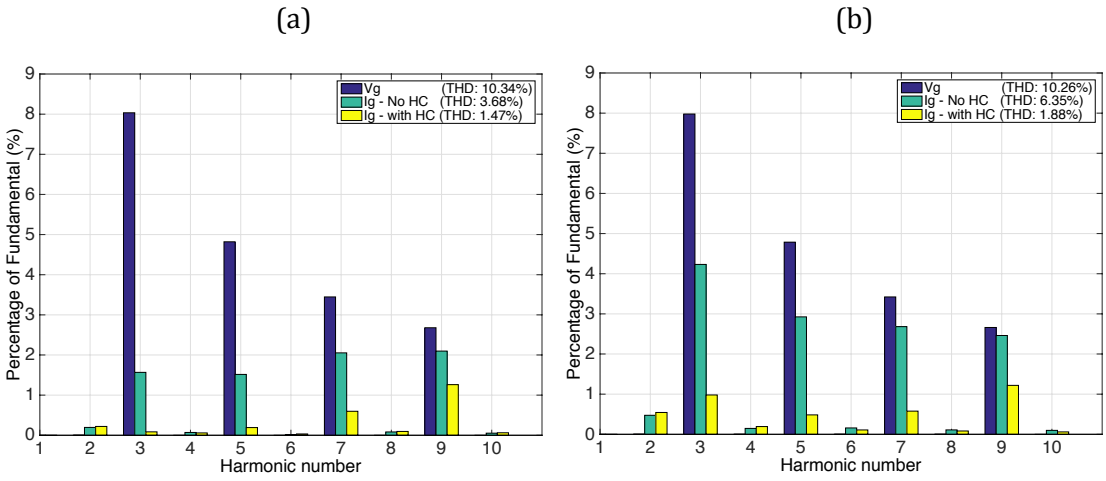


Fig. 3-51 Harmonic compensator performance (simulation results). (a) Charge mode. (b) Discharge mode.

Efficiency of System

The efficiency of the frontend side (AC-DC) of the HFT based charger for both G2V and V2G has been measured using a Yokogawa WT3000 precision power analyser for the nominal power level of 2.2 kW at steady state. The efficiency for G2V and V2G modes was measured to be 95.66% and 94.92% respectively.

3.6.2. LF-TF based charger experimental results

Charge Mode Results

The charge and discharge tests for the LF charger were conducted under the same grid conditions as for the HF charger. In charge mode testing, the battery connection (DC link) was connected to a resistor load bank with a

resistance of 10 Ω though a relay. The resistor was used to represent the battery in a charge mode operating condition.

The initialisation of the charger consists of the same pre-charge procedure as was for the HF charger. After the pre-charge and PWM gate drive is enabled, the resistor load bank is switched onto the DC link by closing the battery side relay. Afterwards, the battery current controller is enabled with a demand current of 18 A, resulting in the flow of power from the grid to the resistor load. The waveforms for the test are presented in Fig. 3-52. It can be seen that the grid side current controller operates in a stable manner.

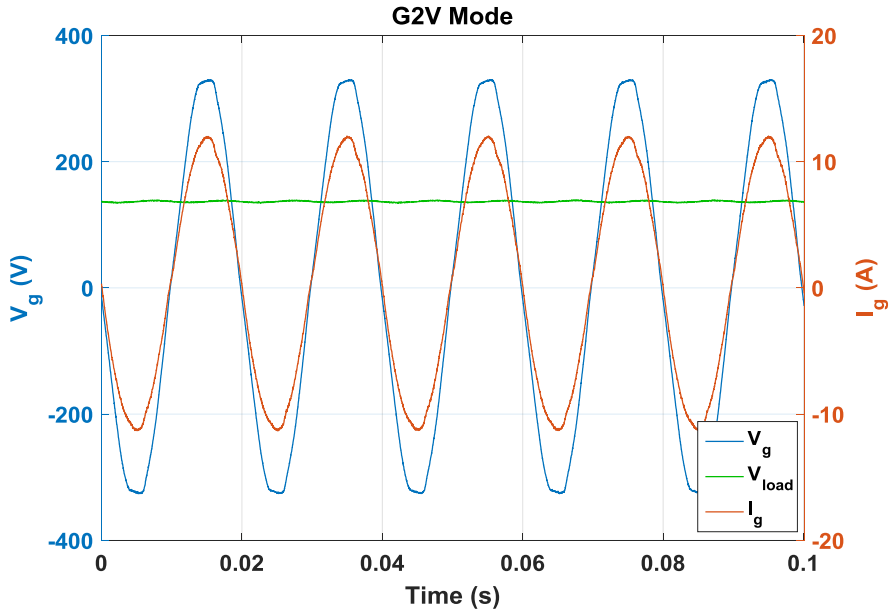


Fig. 3-52 Charge mode, steady state operation - grid voltage, output (load) voltage and grid current (2.2 kW)

Discharge Mode Results

In order to perform the V2G test, the resistor load bank was replaced with a DC power supply. The DC power supply is enabled with a voltage setting of 120 V (nominal battery voltage) thereby charging the DC link capacitors. The PWM switching is enabled thereafter which is followed by enabling the battery

current controller with a -18 A current demand. This results in the flow of power from the DC power supply to the grid as shown in Fig. 3-53.

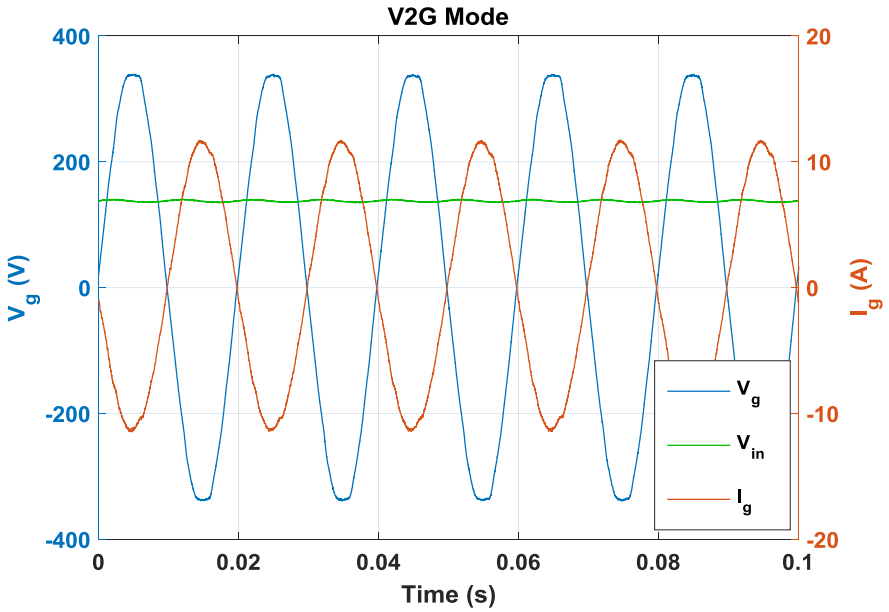


Fig. 3-53 Discharge mode, steady state operation - grid voltage, input voltage and grid current (2.2 kW)

The transient response of the grid current controller has also been validated as shown in Fig. 3-54 by applying a step demand to the SRFPI controller. It can be seen that the grid current increases instantaneously to the demand value with minimal delay as was expected from the controller design.

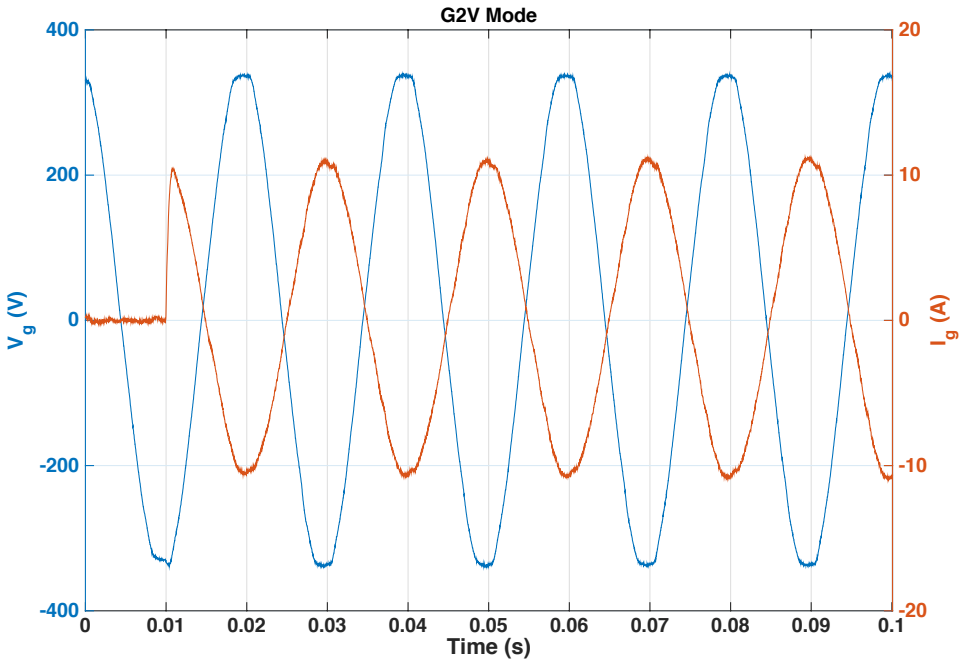


Fig. 3-54 Discharge mode, transient response - grid voltage and current

Validation of Harmonic Compensator in Hardware

The performance of the harmonic compensation is evaluated as was for the HF-TF based charger by executing 2 sets of tests by enabling and disabling the HC block during the tests. The system was operated at the 2.2 kW nominal power rating for the harmonic compensator tests. The obtained results are presented in Fig. 3-55.

(a) (b)

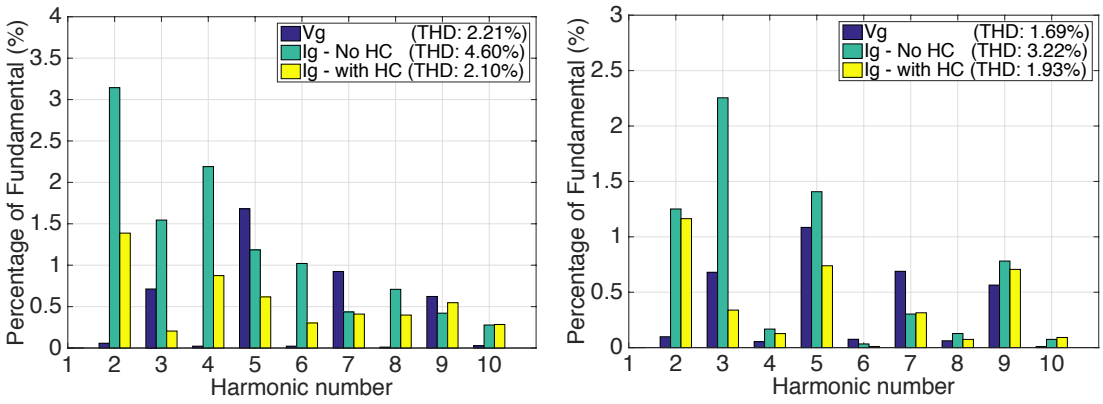


Fig. 3-55 Harmonic compensator performance experimental results

(a) Charge mode. (b) Discharge mode.

It can be observed that the THD has decreased from 4.6% to 2.1% in charge mode, and from 3.22% to 1.93% in discharge mode operation when using the harmonic compensation. It is evident that the use of harmonic compensation makes an improvement to the grid current THD as well as the individual harmonics.

Fig. 3-56 shows the harmonic compensator simulation results discussed in section 3.4.2.3 as a comparison to the experimental results. The simulation study was carried out under a grid voltage THD of 10.3% whereas in the experimental validation, the grid voltage THD was 2.2% for charge and 1.7% for discharge modes. Similar to the HF charger results, it can be seen that during experimental demonstration, the ratio between the grid current (with harmonic compensator disabled) and grid voltage THD is higher than the simulation case. This is attributed to the non-linearity of the magnetic components (isolation transformer and LCL filter inductor) due to the saturation effects that cause low order harmonic distortion in the grid current [151]. Despite this, the experimental validation shows effective THD reduction when the harmonic compensator is activated (54% and 40% reduction in THD for charge and discharge modes respectively which compares to 46% reduction for both charge and discharge modes of the simulation results).

(a) (b)

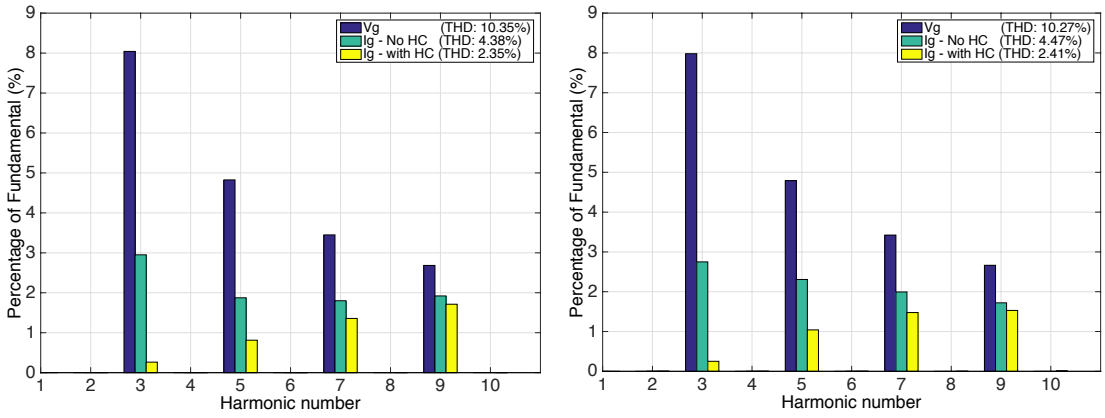


Fig. 3-56 Harmonic compensator performance (simulation results). (a) Charge mode. (b) Discharge mode.

Efficiency of System

The efficiency of the frontend side (AC-DC) of the LFT based charger for both G2V and V2G has been measured using a Yokogawa WT3000 precision power analyser. The efficiency for G2V and V2G modes was measured to be 89.33% and 90.58% respectively (for a battery-side voltage of 120 V and a power level of 2.2 kW).

Evaluation of the LCL filter performance

The performance of the LCL filter of the practical LF charger system can be compared to the performance that was predicted by the analytical methods in Chapter 2 and the Simulink simulation methods in this chapter.

The aim of the comparison is to determine the accuracy and effectiveness of the analytical LCL design procedure presented in Chapter 2. Discharge mode of the LF charger is chosen as the operating mode for the comparison.

The two performance metrics selected for the comparison are the high frequency switching harmonic spectrum of the grid current and the power loss in the damping resistor of the LCL filter.

The side bands around the dominant switching harmonic component (20 kHz) are compared between analytical prediction, simulation results and experimental results. Although the analytical calculation that was used for the design of the LCL filter consisted of using the absolute worst-case value of ripple, for the purposes of verification, the analytical calculation in this section is done for the same operating conditions as the inverter system experiment. The experimental grid harmonic current is measured through a custom ADC acquisition circuit, which is discussed in Chapter 5.

For validation of the analytical equations of current ripple and power loss, the filter capacitor and resistor values of the experimental system is measured so as to eliminate any errors due to component tolerance. The filter

capacitor was measured to be 6.28 μF (as opposed to the rated 6.8 μF) and the filter resistor was measured to be 1.19 Ω (rated resistance: 1.2 Ω). These component values were used in the analytical calculation and Simulink simulation. The results of the current ripple comparison is presented in Fig. 3-57. It can be observed that the analytical and Simulink simulation results correlate closely and the experimental ripple value is lower. The experimental measurement is 13.6% and 11.9% lower than the analytical prediction for the 19.95 kHz and 20.05 kHz components respectively. The lower value in the practical measurement is attributed to the series inductance of the utility grid that has been ignored in the analytical calculation and simulation. Since the grid inductance causes a reduction in the current ripple, the assumption of zero grid inductance made in Chapter 2 considers the worst case condition.

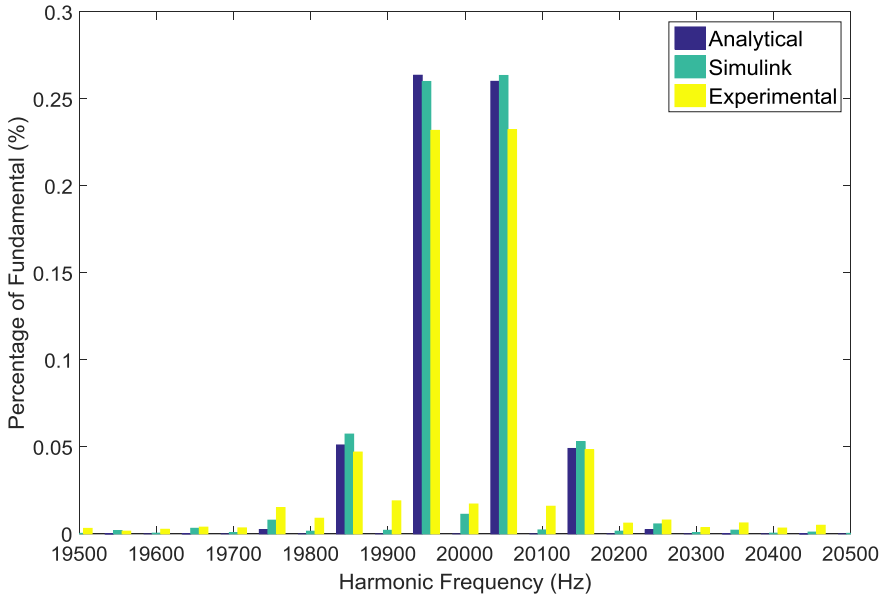


Fig. 3-57 Comparison of switching harmonics in I_g between analytical, simulation and experimental cases

The damping resistor power loss in the practical test is obtained by measuring the voltage across the damping resistor with the use of a 12-bit resolution oscilloscope. The power loss is calculated according to the V^2/R

formula. Since the waveform consists of many harmonics, an FFT is performed on the measured data after which the contribution of each harmonic component is summed to obtain the total power loss.

Table 3-4 Comparison between analytical, simulational and experimental resistor power loss (for nominal power of 2.2 kW)

Analytical Prediction	Simulink Result	Experimental Measurement
0.432 W	0.436 W	0.424 W

The resulting power loss comparison is outlined in Table 3-4. It is evident that the analytical prediction and simulation result is in close agreement whereas the experimental measurement is 1.9% lower.

3.7. Summary

The controller design methodology for the two types of bidirectional charger systems has been presented in this chapter, followed by simulation and experimental validation. In particular, the harmonic compensator performance has been validated in hardware, which shows significant improvement to the power quality and therefore enables the converter to meet the grid harmonic standards (IEEE 519). Furthermore, details of the hardware setup for the two bi-directional chargers that were designed and built have been presented in this chapter.

From the results of the simulation and experimental demonstration, it can be concluded that the controller design for the two topologies of bidirectional chargers presented in this chapter fulfils the performance requirements for a bidirectional charger system.

Furthermore, the LCL filter design methods that were discussed in the previous chapter have also been validated with a simulational and experimental performance comparison and it can be observed that the experimental results

of the high frequency switching harmonics and power dissipation in the damping resistor are within ~8% and 12% of the analytical prediction, respectively. Therefore it can be concluded that the LCL design methodology that was discussed in Chapter 2 is able to successfully optimise the weight and efficiency of the LCL filter as well as providing a guideline value for the power rating required for the damping resistor.

Chapter 4

Grid Synchronisation in Converters

This chapter focuses on the methods of grid synchronisation, specifically phase locked loop (PLL) based methods. The first part (4.2) investigates the effect of third harmonic distortion in the utility voltage on the performance of the widely used second order generalised integrator (SOGI) based PLL. An analytical method that estimates the PLL output harmonics for a given 3rd harmonic distortion is presented and the results of the analytical method are compared to time domain simulations. Furthermore, two methods of modified SOGI PLL structures are presented which offers a performance improvement over the conventional SOGI PLL in terms of third harmonic rejection capability.

The second part (4.3) of the chapter investigates the viability of a new class of discrete time PLL termed the Phasor-IIR PLL (PIIR PLL) that has been developed by Ed Daw et al. [Appendix C] in the application for grid converters. Furthermore, the PIIR PLL is compared with the SOGI PLL to assess their relative performance merits.

4.1. Introduction

4.1.1. Grid synchronisation

Since on-board battery chargers for electric vehicles are intended to be used in domestic environments with access to ac power, grid synchronisation of the charger is an important aspect of the charger design considerations. Grid synchronisation refers to the process of obtaining the instantaneous parameters of the grid voltage vector to facilitate the interfacing of the power converter to the utility grid. These parameters include the magnitude, phase and frequency of the fundamental for typical power converters as well as the

detection of any harmonics present in applications such as power conditioning, resonance damping and impedance detection [33].

Since the utility is subject to a variety of transients and abnormal conditions due to the variation of the demand, faults and other external influences, it is required that the synchronisation method is able to adapt to the transients in the shortest time possible to ensure the efficient operation of the power converter.

Grid synchronisation techniques can be classed into two broad groups; methods based on the frequency domain and methods based on the time domain [33]. Frequency domain methods consist of the application of a form of discrete Fourier transform in an adaptive band-pass filter configuration in order to obtain the phase and magnitude of the grid voltage signal. Discrete Fourier transform based methods suffer from phase angle and magnitude errors when the grid frequency deviates from the nominal value due to the number of samples in one cycle of the input signal not being an integer multiple of the sample window [33], although methods to mitigate this issue have been proposed in [152, 153].

The simplest form of time domain based synchronisation methods is the zero crossing detection of the grid voltage in which a comparator in combination with a timer (and integrator) is used for detecting each half cycle transition of the input signal and thereby derive the frequency (and phase). Although simple to implement, this method has the disadvantage of being sensitive to the quality of the input signal so that any distortion results in errors in the detection. Methods to mitigate the issues have been proposed such as in [154] where adaptive compensation is used and in [155] where dynamic hysteresis or interpolation is utilised. Other time domain based synchronisation methods typically operate with the use of a variable frequency oscillator in a control loop such that the output signal tracks the input's frequency and phase. Examples for such methods are, the phase locked loop (PLL) and the frequency locked loop (FLL) [156].

4.1.2. The Phase-Locked Loop (PLL)

The most commonly used synchronisation structure in the field of power converters, motor drives as well as in the field of communication is the phase-locked loop (PLL), which was first suggested by Appleton [157] in 1923. Comprehensive analytical description of PLLs have been presented thereafter in [158, 159] however, actual application of the method did not arise till the widespread use of integrated circuits (ICs) in the 1970's [34]. The application of the PLL in motor drives also occurred during the same period in the form of analogue electronics, which later migrated into digital systems with the rapid development of microprocessor systems in the 1980's [34].

Over the years, many different types of PLLs have been developed, with the most notable difference among them being the architecture of the phase detection method. The simplest form of the PLL is commonly referred to as the power-PLL (pPLL) in which the phase detection method consists of a multiplier [40]. An in-depth study of the conventional PLL and its applications has been carried out in [34].

Structure of the pPLL

The pPLL can be divided into three functional blocks as depicted in Fig. 4-1. The blocks are generally referred to as the phase detector (PD), loop filter (LF) and the voltage controlled oscillator (VCO). The PD generates an error signal (v_{err_pd}) that is proportional to the difference in phase between the input signal (v) and the output signal of the PLL (v_o). In the case of the pPLL, the PD consists of a multiplication function, which has the side effect of the generation of a double frequency tone in the error signal along with the DC error component. The error output signal of the PD is given in (4-1). It can be seen that in steady state when the PLL is locked $(\omega = \omega_o, \phi = \phi_o)$, the second term in the equation is the undesired double frequency component.

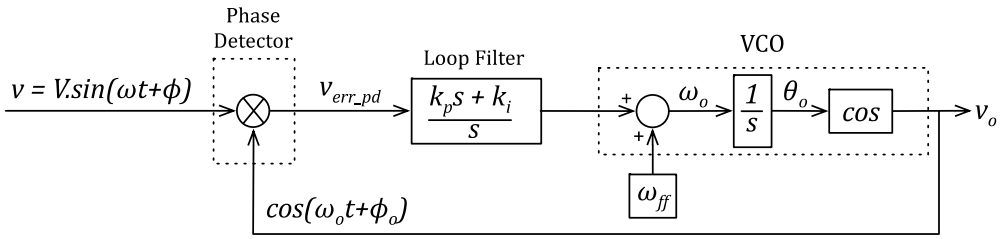


Fig. 4-1 Basic structure of pPLL

$$v_{err\_pd} = \frac{V}{2}\{\sin([\omega - \omega_o]t + [\phi - \phi_o]) + \sin([\omega + \omega_o]t + [\phi + \phi_o])\} \quad \textbf{(4-1)}$$

The loop filter (LF) low pass filters v_{err_pd} so as to obtain the DC component of the error signal. The LF usually consists of a PI controller, which inherently has a low pass frequency response.

The function of a VCO is to generate a signal with a frequency that is proportional to the input magnitude. Therefore, the filtered signal from the LF drives the VCO that in turn generates the phase angle at a frequency that is centred on the nominal grid frequency (ω_{ff}), which is a feed forward term to facilitate fast locking. The output signal of the VCO (v_o) is then derived from the phase angle (θ_o) with a cosine function. In the case of the pPLL, the VCO consists of an integrator function.

Linearised model of pPLL

If we assume that the initial PLL frequency output is the same as the input frequency, from Eq. (4-1), the phase error signal can be simplified to the form in (4-2). Although this is a nonlinear term, it is possible to obtain the linearised model of the PD for small deviations in phase since $\sin(\phi - \phi_o) \approx (\phi - \phi_o)$ for small $(\phi - \phi_o)$.

$$v_{err\_pd} = \frac{V}{2}\{\sin(\phi - \phi_o)\} \quad \textbf{(4-2)}$$

The linearised model of the pPLL based on the above assumptions is illustrated in Fig. 4-2, which relates the phase of the input signal to the phase of the output signal. Therefore it is possible to design the pPLL using conventional control theory to ensure optimal settling time and stable operation as has been reported in [33, 160].

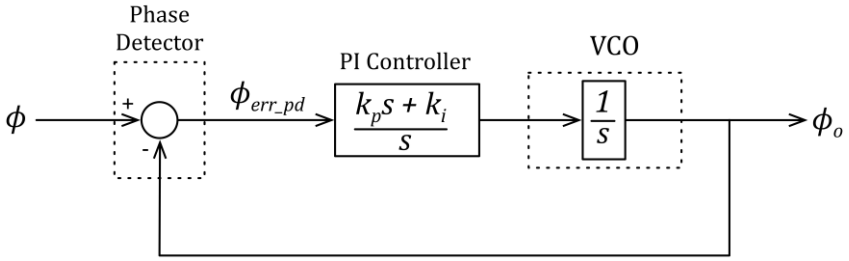


Fig. 4-2 Linearised model of pPLL

Despite the simplicity of the pPLL, the disadvantages of the method include its sensitivity to variations in the grid voltage (in particular, voltage sag conditions causes the transient response to suffer) and the poor transient response due to the LPF characteristics [40].

A variety of methods to improve the aforementioned issues in the pPLL have been proposed such as the DFAC method [40] in which the double frequency is cancelled along with amplitude compensation in the DQ frame. Another method proposed by Thacker *et al.* [161] consists of cancelling the double frequency term by subtracting the term $(\sin\theta_o \cos\theta_o)$ from the error signal and utilising a peak voltage tracker for ensuring unity input voltage to the PLL regardless of the grid voltage magnitude. However, since the peak voltage detection cannot be done instantaneously, the PLL performance is degraded under utility voltage changes [40]. Other types of PLL based on the conventional PLL include the enhanced-PLL (EPLL) [37, 162] where an adaptive notch filter is used for removing the undesired double frequency component, the complex coefficient filter based PLL presented in [42] as well as the variable time delay based PLL [41].

4.1.3. Synchronous Rotating Frame (SRF) PLL

It is clear that the conventional PLL has an inherent limitation of bandwidth due to the 2nd harmonic rejection requirement, which results in a poor transient response. Therefore, an alternative method can be utilised where a synchronous rotating frame based PD is used. This method first appeared in [163] where the design of a three-phase PLL suitable for the operation under distorted utility conditions was presented. The application of this method in single-phase systems has been presented in [35, 36, 132].

The basic block diagram of the SRF based PLL method is shown in Fig. 4-3. The concept of the SRF PLL lies in the transformation of the utility voltage vector to a quadrature synchronous reference frame as shown in Fig. 4-4 with the use of the Park transform. The DQ transformation requires the generation of an orthogonal signal (v_β) which is 90° phase shifted to the input signal (v_α). The stationary-to-synchronous frame transformation is defined in (4-3) where v_α and v_β are defined in (4-4).

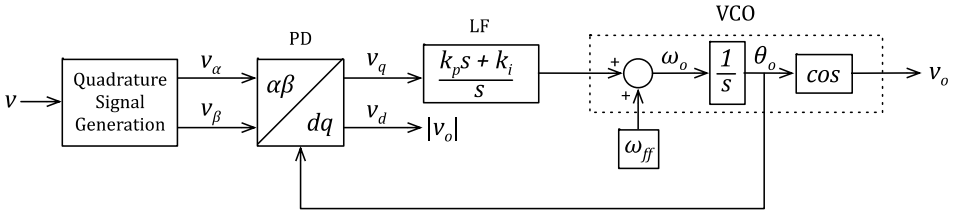


Fig. 4-3 Synchronous rotating frame based PLL

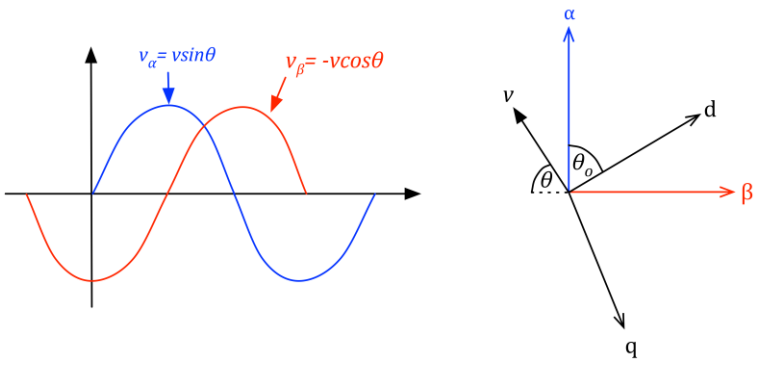


Fig. 4-4 Relationship between stationary and synchronous frame signals

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} \cos\theta_o & \sin\theta_o \\ -\sin\theta_o & \cos\theta_o \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \quad \textbf{(4-3)}$$

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = V \begin{bmatrix} \sin\theta \\ -\cos\theta \end{bmatrix} \quad \textbf{(4-4)}$$

The output signals of the DQ transformation block can be simplified as shown in (4-5) and (4-6). Therefore, it can be seen that at steady state $(\omega = \omega_o)$, the error signal of the SRF PD block (v_q) is free of the double frequency component that was seen in the pPLL. Hence it is possible to have a larger bandwidth for the PLL resulting in a faster transient response [33]. Since the quadrature signal is used as the closed loop control variable, PLL lock occurs when $(\theta - \theta_o)$ becomes equal to 90° (v_q is zero).

$$v_d = V\sin([\omega - \omega_o]t + [\phi - \phi_o]) \quad \textbf{(4-5)}$$

$$v_q = -V\cos([\omega - \omega_o]t + [\phi - \phi_o]) \quad \textbf{(4-6)}$$

While the three-phase SRF PLL relies on the Clark transform to generate the stationary frame signals (v_α, v_β), a number of different methods are used to generate the orthogonal signal in the case of the single-phase SRF PLL. These include the inverse Park transform [35, 36], Hilbert transform [132], transport delay [164] and the second order generalised integrator (SOGI) based [38] methods as well as more recent developments based on the discrete Fourier transform [43].

The different methods of quadrature signal generation (QSG) in SRF PLLs have various trade-offs in terms of performance and complexity. The inverse park transform based PLL has the disadvantage of a complex tuning procedure for the PI controller due to the two interdependent nonlinear loops [164] whereas the Hilbert transform based PLL has a trade-off between filter

order where a low order filter has poor harmonic rejection and a higher order one has a time delay [164]. Despite the ease of implementation of the transport delay based SRF PLL, it exhibits phase angle errors when the frequency deviates from the nominal value due to the fixed delay length of the FIFO buffer [39].

The SOGI PLL has gained wide spread recognition for the relative simplicity and fast response to transients relative to the other types of PLLs, although its harmonic rejection capability is inferior to the pPLL method. The basic structure and operation of the SOGI PLL is discussed in the next section before the improved SOGI is presented in section 4.2.

4.1.4. Second Order Generalised Integrator (SOGI) based PLL

The SOGI based PLL, which was proposed by Mihai Ciobotaru *et al.* [38] consists of a novel QSG block in combination with a standard synchronous DQ frame based PLL. The structure of the SOGI QSG block is illustrated in Fig. 4-5. The transfer functions of the in-phase (v_α) and quadrature (v_β) signals are defined in (4-7)-(4-8).

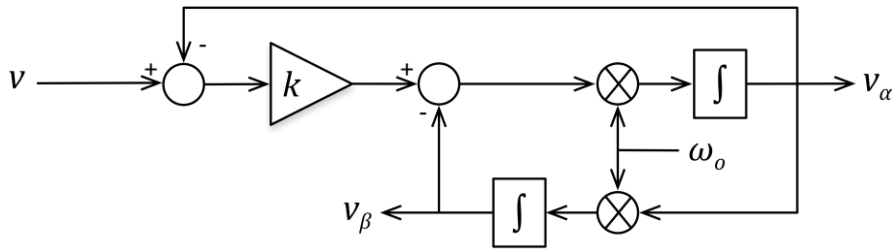


Fig. 4-5 The SOGI quadrature signal generation block

$$G_{SOGI\_\alpha}(s) = \frac{v_\alpha}{v}(s) = \frac{k\omega_o s}{s^2 + k\omega_o s + {\omega_o}^2} \quad \textbf{(4-7)}$$

$$G_{SOGI\_\beta}(s) = \frac{v_\beta}{v}(s) = \frac{k{\omega_o}^2}{s^2 + k\omega_o s + {\omega_o}^2} \quad \textbf{(4-8)}$$

Therefore, it can be observed that the closed loop transfer function of the in-phase output signal of the SOGI block given in equation (4-7) takes the form of a resonant band-pass filter. The ω_o sets the centre frequency (nominally 50 Hz) while k sets the pass bandwidth of the filter structure as shown in Fig. 4-7 for different values of k. The overall PLL structure is shown in Fig. 4-6.

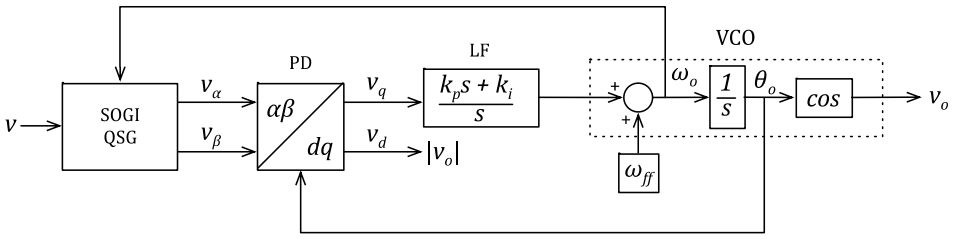


Fig. 4-6 Overall SOGI PLL structure

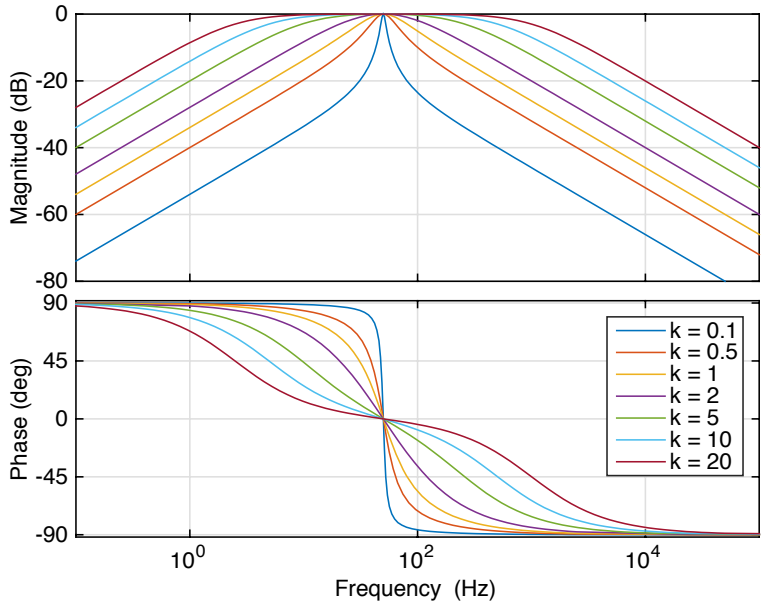


Fig. 4-7 SOGI Bode plot for different values of 'k' (from equation (4-7))

Golestan *et al.* [165] have shown that the overall linearised model and resulting open loop transfer function for frequencies lower than $2\omega_o$ of the SOGI PLL to be as depicted in Fig. 4-8 and given by (4-9), respectively where $\tau_p = {}^{2}/_{k\omega_o}$.

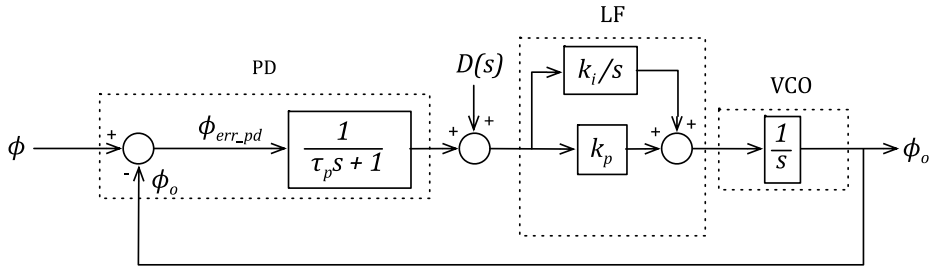


Fig. 4-8 Linearised model of SOGI PLL [165]

$$G_{ol}(s) = \frac{\phi_o(s)}{\phi_{err\_pd}(s)}\bigg|_{D(s)=0} = \frac{k_i + k_p s}{s^2\left[s\left(\frac{2}{k\omega_o}\right)+1\right]} \qquad \textbf{(4-9)}$$

Furthermore, an optimised design methodology for tuning the SOGI PLL which accounts the delay of the SOGI block has been presented in [165] which provides a fast transient response and a high disturbance rejection capability.

This design method will be used in this chapter as a benchmark for comparison with the improved SOGI PLL and the PIIR PLL. According to the optimised design in [165], the SOGI gain *(k)*, the proportional gain *(k_p)*, and the integral gain *(k_i)* are set as 2.1, 137.5 and 7878, respectively, for a nominal grid frequency of 50 Hz.

4.2. Improved SOGI with notch filter

As mentioned previously, in comparison with the pPLL, the SOGI PLL responds faster to variations in the grid voltage vector due to higher bandwidth. This has, however, led to lower attenuation of grid harmonics. Therefore, an investigation into increasing the harmonic rejection capability of the SOGI PLL has been carried out.

4.2.1. Analysis of the SOGI PLL harmonic rejection characteristics

In order to quantify the harmonic rejection capability, it is important to analyse the PLL in more detail specifically for the harmonics of interest. The transfer function of the SOGI PLL presented in (4-9) is only accurate up to $2\omega_o$. Therefore, an analytical approach is employed to quantify the propagation of the harmonics through the PLL structure.

The signal path through the SOGI PLL can be separated into the following subsections: the SOGI QSG, the park-transform block (PD), the loop filter (LF), the VCO and finally the cosine function which reconstructs the input signal.

The most prominent harmonics present in the grid are the odd harmonics (3, 5, 9 etc.), of which the magnitude decreases with increasing harmonic number. Specifically, the increased levels of the 3rd harmonic is commonly observed in residential utility systems due to the unbalanced residential loads and the use of wye-wye service transformers [166, 167]. The SOGI QSG attenuates harmonics as shown in Fig. 4-9 for the in-phase and quadrature outputs (with $k = 2.1$). It can be seen that the attenuation for the harmonics increases with increasing frequency and consequently increasing harmonic number. Since the magnitude of the harmonics present in the grid for higher frequencies is lower and since there is also more attenuation at higher frequencies in the SOGI QSG, we will investigate the 3rd harmonic and its propagation through the PLL structure in steady state operation when the PLL is locked to the input signal.

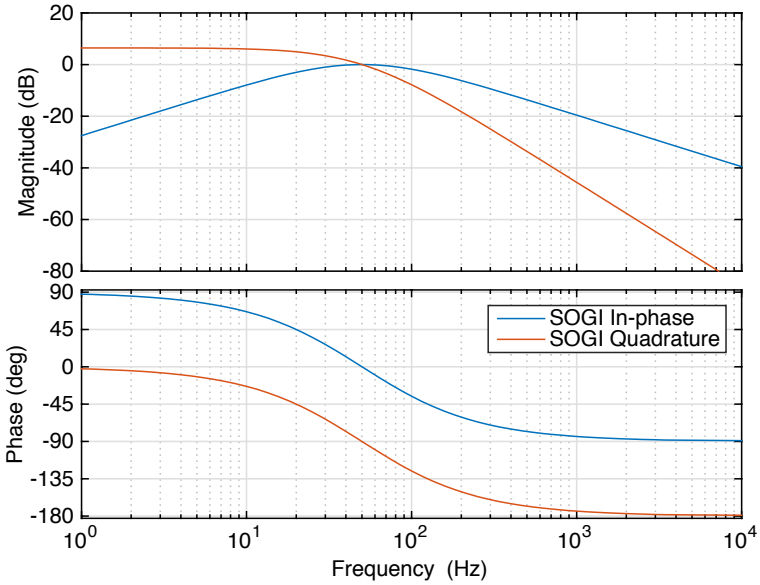


Fig. 4-9 SOGI QSG Bode plot for in-phase and quadrature signals

The h^{th} order harmonic, v_h, of interest in the input signal is defined as follows with the magnitude V_h and phase ϕ_h.

$$v_h = V_h \sin(\omega h t + \phi_h) \tag{4-10}$$

The resulting harmonic components present in the in-phase and quadrature outputs, v_{α_h} and v_{β_h} after the SOGI QSG are given by (4-11) and (4-12), where $\left|G_{SOGI\_\alpha}(j\omega h)\right|$, $\left|G_{SOGI\_\beta}(j\omega h)\right|$ and ϕ_α are the gain of the in-phase and quadrature signal paths of the SOGI QSG and the phase delay of the in-phase signal path for the specific harmonic frequency and are given in (4-13)-(4-15).

$$v_{\alpha\_h} = V_h \left|G_{SOGI\_\alpha}(j\omega h)\right| \sin(\omega h t + \phi_h + \phi_\alpha) \tag{4-11}$$

$$v_{\beta\_h} = -V_h \left|G_{SOGI\_\beta}(j\omega h)\right| \cos(\omega h t + \phi_h + \phi_\alpha) \tag{4-12}$$

$$\left|G_{SOGI\_\alpha}(j\omega h)\right| = \left|\frac{j\omega hk\omega_{SOGI}}{(j\omega h)^2 + j\omega hk\omega_{SOGI} + {\omega_{SOGI}}^2}\right| \quad \textbf{(4-13)}$$

$$\left|G_{SOGI\_\beta}(j\omega h)\right| = \left|\frac{k{\omega_{SOGI}}^2}{(j\omega h)^2 + j\omega hk\omega_{SOGI} + {\omega_{SOGI}}^2}\right| \quad \textbf{(4-14)}$$

$$\phi_\alpha = \phi_\alpha(j\omega h) = \angle\left[\frac{j\omega hk\omega_{SOGI}}{(j\omega h)^2 + j\omega hk\omega_{SOGI} + {\omega_{SOGI}}^2}\right] \quad \textbf{(4-15)}$$

If it is initially assumed that the PLL output phase angle θ_o only contains the fundamental frequency component, the DQ block results in the mixing of the fundamental frequency with the third harmonic components (v_{α_h} and v_{β_h}) present in the v_α and v_β signals. Using the Park transform of (4-3), the quadrature output signal v_q after the DQ block (assuming that the PLL is locked and in steady state, hence the DC value is zero), can be simplified as follows.

$$v_q = A_1\cos(\omega t[h+1]+\phi_h+\phi_\alpha) - A_2\cos(\omega t[h-1]+\phi_h+\phi_\alpha) \quad \textbf{(4-16)}$$

$$A_1 = \frac{V_h}{2}\left(\left|G_{SOGI\_\alpha}(j\omega h)\right| - \left|G_{SOGI\_\beta}(j\omega h)\right|\right) \quad \textbf{(4-17)}$$

$$A_2 = \frac{V_h}{2}\left(\left|G_{SOGI\_\alpha}(j\omega h)\right| + \left|G_{SOGI\_\beta}(j\omega h)\right|\right) \quad \textbf{(4-18)}$$

It is observed that the DQ transformation results in the generation of two components with harmonic order of ($h\pm1$). Thus, the third harmonic results in 2nd and 4th harmonics.

Thereafter, the output of the loop filter, v_{PI} can be simplified as follows where C represents an arbitrary constant of integration.

$$v_{PI} = k_p v_q + \frac{k_i A_1}{\omega(h+1)} \sin(\omega t[h+1] + \phi_h + \phi_\alpha) - \frac{k_i A_2}{\omega(h-1)} \sin(\omega t[h-1] + \phi_h + \phi_\alpha) + C \quad \textbf{(4-19)}$$

The input to the VCO is obtained in (4-20) assuming that the PLL is locked.

$$v_{vco\_in} = v_{PI} + C + \omega_{ff} = v_{PI} + \omega \quad \textbf{(4-20)}$$

After substituting (4-19) into (4-20), integrating and simplifying, the VCO output can be defined as (4-21) where k_{v1}, k_{v2}, ϕ_{v1} and ϕ_{v2} are given in (4-22)-(4-25).

$$v_{vco\_out} = \omega t + k_{v1} \sin(\omega t[h+1] + \phi_{v1}) + k_{v2} \sin(\omega t[h-1] + \phi_{v2}) \quad \textbf{(4-21)}$$

$$k_{v1} = \frac{A_1 \sqrt{k_p^2 \omega^2 (h+1)^2 + k_i^2}}{\omega^2 (h+1)^2} \quad \textbf{(4-22)}$$

$$k_{v2} = \frac{-A_2 \sqrt{k_p^2 \omega^2 (h-1)^2 + k_i^2}}{\omega^2 (h-1)^2} \quad \textbf{(4-23)}$$

$$\phi_{v1} = \phi_h + \phi_\alpha - \tan^{-1}\left(\frac{k_i}{k_p \omega (h+1)}\right) \quad \textbf{(4-24)}$$

$$\phi_{v2} = \phi_h + \phi_\alpha - \tan^{-1}\left(\frac{k_i}{k_p \omega (h-1)}\right) \quad \textbf{(4-25)}$$

It is apparent that similar to v_q, the angle output of the PLL also contains the sum and difference between the higher order and fundamental components in addition to the time varying ωt quantity.

The output of the PLL is obtained by the cosine operation on the PLL angle signal. Therefore, the PLL output signal can be defined as given in (4-26).

$$v_{SOGI\_PLL\_out} = \cos\{\omega t + k_{v1}\sin(\omega t[h+1] + \phi_{v1}) + k_{v2}\sin(\omega t[h-1] + \phi_{v2})\} \quad \textbf{(4-26)}$$

It is clear that the relationship between the input harmonic magnitude and resulting output distortion is non-linear. Using trigonometric expansion followed by the Jacobi-Anger expansion method it is possible to identify the resulting harmonics and their magnitudes caused by the input harmonic component. The Jacobi-Anger expansions that are used are given in (4-27) and (4-28) [168].

$$\cos(\mathrm{z}\sin\theta) = J_0(z) + 2\sum_{k=1}^{\infty} J_{2k}(z)\cos(2k\theta) \quad \textbf{(4-27)}$$

$$\sin(\mathrm{z}\sin\theta) = 2\sum_{k=0}^{\infty} J_{2k+1}(z)\sin\{(2k+1)\theta\} \quad \textbf{(4-28)}$$

where J_0, J_{2k} and J_{2k+1} denote the Bessel functions of the first kind of order 0, 2k, and 2k+1, respectively.

The resulting equation can be simplified by considering the fact that for the typical SOGI parameters (k, k_p and k_i), the Bessel functions of the first kind for integer orders higher than 1 result in very small values and hence can be neglected. The resulting equation is depicted in (4-29) where k_1 to k_4 are defined as (4-30)-(4-33).

$$\begin{aligned} v_{SOGI\_PLL\_out} = {} & k_1\cos(\omega t) - k_2\sin(\omega t)\sin(\omega t[h+1] + \phi_{v1}) \\ & - k_3\sin(\omega t)\sin(\omega t[h-1] + \phi_{v2}) \\ & - k_4\cos(\omega t)\sin(\omega t[h+1] + \phi_{v1})\sin(\omega t[h-1] + \phi_{v2}) \end{aligned} \quad \textbf{(4-29)}$$

$$k_1 = J_0(k_{v1})\,J_0(k_{v2}) \quad \textbf{(4-30)}$$

$$k_2 = 2\,J_0(k_{v2})\,J_1(k_{v1}) \quad \textbf{(4-31)}$$

$$k_3 = 2\,J_0(k_{v1})\,J_1(k_{v2}) \quad \textbf{(4-32)}$$

$$k_4 = 4\,J_1(k_{v1})\,J_1(k_{v2}) \quad \textbf{(4-33)}$$

By performing a Fourier trigonometric series expansion on the above equation for $h = 3$, the individual frequency components present in the PLL output signal due to the 3rd harmonic component can be shown to be as follows.

$$\begin{aligned} v_{SOGI\_PLL\_out} = {} & \frac{1}{2}\left(2k_1 - \frac{1}{2}k_4\cos[\phi_{v1} - \phi_{v2}] - k_3\cos[\phi_{v2}]\right)\cos[\omega t] \\ & + \frac{1}{2}\left(-k_2\cos[\phi_{v1}] - \frac{1}{2}k_4\cos[\phi_{v1} - \phi_{v2}]\right. \\ & \left. + k_3\cos[\phi_{v2}]\right)\cos[3\omega t] \\ & + \frac{1}{2}\left(k_2\cos[\phi_{v1}] + \frac{1}{2}k_4\cos[\phi_{v1} + \phi_{v2}]\right)\cos[5\omega t] \\ & + \frac{1}{4}(k_4\cos[\phi_{v1} + \phi_{v2}])\cos[7\omega t] \\ & + \frac{1}{2}\left(\frac{1}{2}k_4\sin[\phi_{v1} - \phi_{v2}] + k_3\sin[\phi_{v2}]\right)\sin[\omega t] + \frac{1}{2}\left(k_2\sin[\phi_{v1}]\right. \\ & \left. + \frac{1}{2}k_4\sin[\phi_{v1} - \phi_{v2}] - k_3\sin[\phi_{v2}]\right)\sin[3\omega t] \\ & + \frac{1}{2}\left(-k_2\sin[\phi_{v1}] - \frac{1}{2}k_4\sin[\phi_{v1} + \phi_{v2}]\right)\sin[5\omega t] \\ & - \frac{1}{4}(k_4\sin[\phi_{v1} + \phi_{v2}])\sin[7\omega t] \end{aligned} \quad \textbf{(4-34)}$$

It can be observed that as a result of the 3rd harmonic, the output signal contains the 3rd as well as the 5th and 7th harmonics. The fundamental magnitude also undergoes a small variation. The magnitudes of the 3rd and 5th harmonics can be defined as (4-35) and (4-36).

$$\begin{aligned} V_{SOGI\_PLL\_h3} = {} & \frac{1}{4}\{4k_2^2 + 4k_3^2 + k_4^2 - 4k_3k_4\cos[\phi_{v1} - 2\phi_{v2}] \\ & - 8k_2k_3\cos[\phi_{v1} - \phi_{v2}] + 4k_2k_4\cos[\phi_{v2}]\}^{1/2} \end{aligned} \quad \textbf{(4-35)}$$

$$V_{SOGI\_PLL\_h5} = \frac{1}{4}\{4k_2^2 + k_4^2 + 4k_2k_4\cos[\phi_{v2}]\}^{1/2} \quad \textbf{(4-36)}$$

It must be noted that the above analytical derivation ignores the effect of the two feedback quantities (ω and θ_o) containing harmonic distortion. In reality this distorted feedback signals give rise to higher order harmonics to be generated through the DQ mixing although at minute magnitudes. Furthermore, the presence of other harmonics such as the 5th, 9th etc. in the grid voltage causes the generation of other even order harmonics (2nd, 4th, 6th, etc.) in the PLL angle output, which translates into evermore-complicated components after the cosine function.

4.2.2. Comparison of analytical prediction of harmonics and time domain simulation

In order to verify the accuracy of the analytical method of harmonic estimation, the SOGI PLL is simulated in Simulink in the discrete time implementation level model. The integrators for the PLL are of the configuration of 3rd order discrete integrators as presented in [38] as it has been shown to provide the best approximation of the continuous time integrator function. The structure of the 3rd order discrete integrator is depicted in Fig. 4-10.

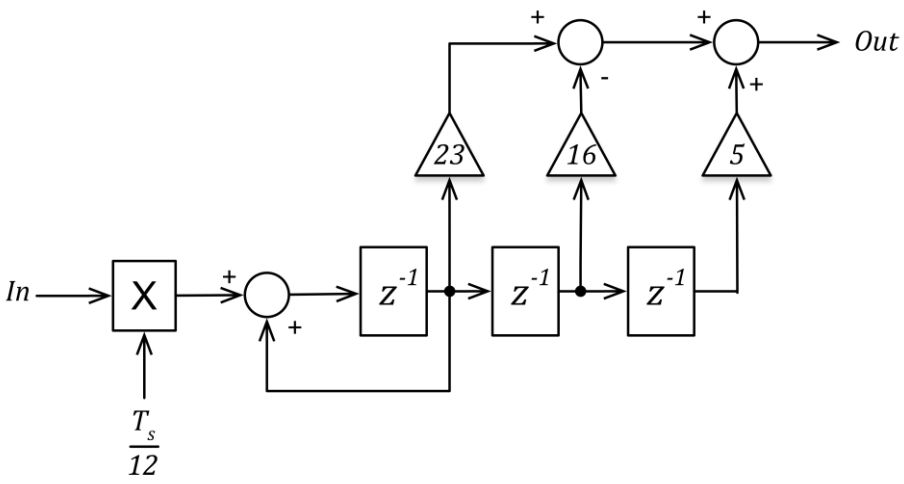


Fig. 4-10 Structure of 3rd order discrete integrator [38]

A 50 Hz signal with three different values of 3rd harmonic magnitudes (5%, 10%, 15%) have been used as the input to the SOGI PLL after which the output spectrum has been obtained with the use of FFT. Two SOGI PLL configurations are used for the simulation ("SOGI PLL – 1" and "SOGI PLL – 2") for which the gain values are shown in Table 4-1. The gain values for "SOGI PLL – 1" are based on the optimal SOGI PLL configuration presented in [165]. The k gain value for "SOGI PLL – 2" has been selected based on the recommendation in [33] whereas the k_p and k_i values have been obtained by iterative tuning. The analytically predicted magnitudes of the 3rd and 5th harmonics have been obtained by substituting the same PLL and signal parameters to equation (4-35) and (4-36). The resulting comparison is presented in Table 4-2. Since the magnitude of the 7th harmonics is very low, it is neglected.

Table 4-1 SOGI PLL configurations for verifying the analytical method

PLL Configuration	k	k_p	k_i
SOGI PLL – 1 (Optimal SOGI)	2.1	137.5	7878
SOGI PLL - 2	1.414	200	12000

Table 4-2 SOGI PLL output distortion for 3rd harmonic input – Simulink vs. analytical prediction

PLL Configuration	150 Hz Input	Simulink PLL Output Harmonic Magnitudes		Analytical PLL Output Harmonic Magnitudes		Simulink vs. Analytical Deviation	
		150 Hz	250 Hz	150 Hz	250 Hz	150 Hz	250 Hz
SOGI PLL – 1	5%	0.299%	0.060%	0.283%	0.056%	**5.55%**	**6.00%**
	10%	0.602%	0.120%	0.565%	0.113%	**6.08%**	**5.77%**
	15%	0.908%	0.179%	0.848%	0.169%	**6.6%**	**5.38%**
SOGI PLL – 2	5%	0.334%	0.067%	0.311%	0.062%	**6.77%**	**7.02%**
	10%	0.672%	0.133%	0.622%	0.124%	**7.37%**	**6.49%**
	15%	1.014%	0.197%	0.933%	0.186%	**7.98%**	**5.88%**

From the results, it can be concluded that the analytical formula is able to predict the output harmonics to a 3rd harmonic component in the input signal with an average accuracy of 6.72% for the 3rd harmonic and 6.1% for the 5th harmonic outputs.

The cause of the deviation between the analytical and simulated results is due to the assumption made in the analytical derivation where the effect of the two feedback quantities (ω and θ_o) containing harmonic distortion are ignored.

4.2.3. SOGI with notch filter – two different approaches

Following the analysis of the influence of 3rd harmonic component on the SOGI PLL, two variations of modified SOGI PLL structures are presented as follows.

4.2.3.1. Method A – SOGI PLL with notch filter in the rotating frame

It was shown that the third harmonic results in the generation of the second and fourth harmonics in the DQ block's output signal (v_q). Furthermore from equation (4-16) it can be shown that the 4th harmonic component is approximately -12 dB relative to the 2nd harmonic present in v_q for the SOGI PLL parameters mentioned previously. Since the 3rd harmonic present in the PLL output signal is the result of the interaction between the 2nd, 4th harmonics and the fundamental components (ωt) when undergoing the cosine function, the ability to reject the 3rd harmonic can be improved by attenuating the 2nd harmonic component that is generated from the DQ block. This can be accomplished by placing a notch filter between the DQ and LF blocks with a frequency set at twice the fundamental frequency. The proposed structure is illustrated in Fig. 4-11. The centre frequency of the notch filter can be configured to move with any variations in the grid frequency by feeding the instantaneous frequency from the PLL output frequency variable following a 2x multiplication.

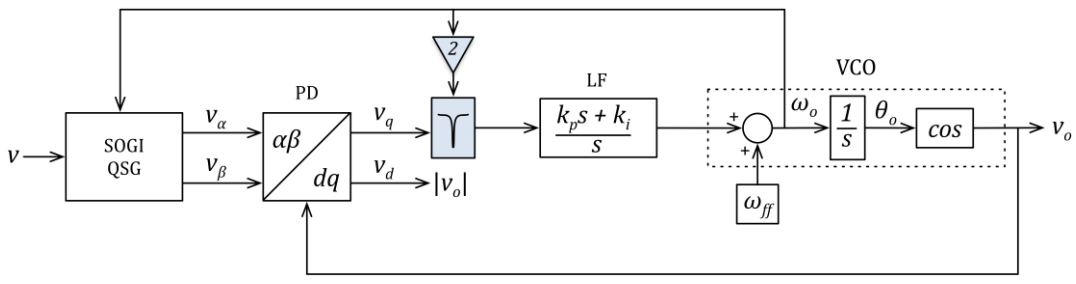


Fig. 4-11 Method A – SOGI PLL with notch filter in the synchronous frame

The standard notch filter transfer function is shown in equation (4-37) where Q_n denotes the quality factor and ω_n represents the notch frequency. It is possible to realise the filter in practice by observing the relationship between the SOGI transfer function and the notch filter transfer function as given in (4-38) where $Q_n = {}^{1}/_{k}$.

$$G_n(s) = \frac{s^2 + \omega_n^2}{s^2 + \frac{\omega_n}{Q_n}s + \omega_n^2} \quad \textbf{(4-37)}$$

$$G_n(s) = 1 - G_{SOGI\_\alpha}(s) \quad \textbf{(4-38)}$$

Selection of Q_n

The quality factor determines the sharpness of the filter response, which affects the stop-band width as well as the phase shift characteristics. Fig. 4-12 illustrates the magnitude and phase response for different values of Q_n. It can be noted that the larger values of Q_n results in a narrower rejection zone, as well as a lower amount of phase shift for frequencies that lie below the notch frequency. A small value of phase shift for frequencies lower than the notch frequency is preferred as it results in minimum degradation of the transient performance of the PLL. However Q_n must not be overly large which would result in a too narrow notch width, as it is not practical due to the finite numerical resolution available in a DSP system and resulting inaccuracies in frequency. Therefore, Q_n has been chosen to be 55 as this value has been evaluated to produce an acceptable phase delay and sufficient notch width (2 Hz).

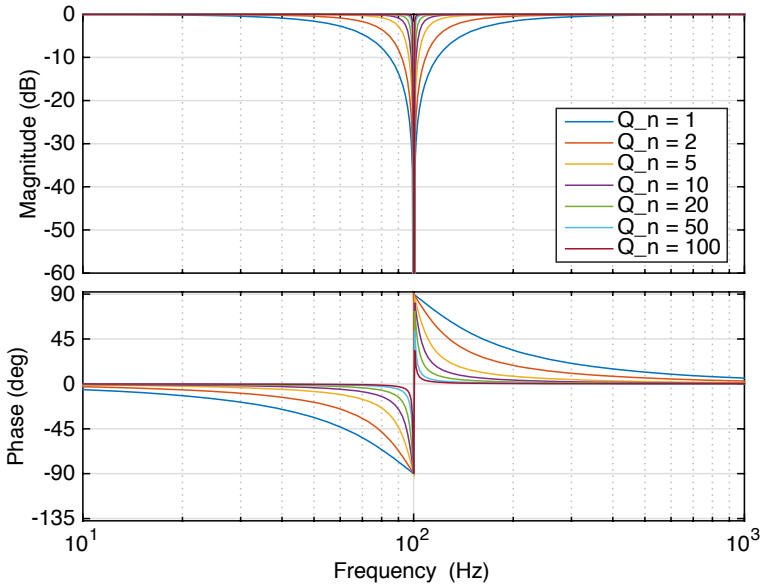


Fig. 4-12 Notch filter Bode plot for different values of Q_n

The stability and transient performance of the notch filter based SOGI PLL can be validated with the modified linearised open loop transfer function of the PLL as given in (4-39). A relative comparison between the conventional SOGI PLL as a reference and the modified PLL is presented in Fig. 4-13 and Fig. 4-14 where the open loop Bode plot and closed loop step responses are plotted. It can be seen that the resulting PLL design has the same phase margin as the reference SOGI PLL of 44.5° and an acceptable gain margin of 20.2 dB (a gain margin greater than 6 dB provides satisfactory performance [169]). Furthermore, the transient response plot shown in Fig. 4.14 indicates that the modified PLL should have similar response times to grid fluctuations as the reference SOGI PLL.

$$G_{ol\_SOGI\_notch}(s) = \frac{\phi_o(s)}{\phi_{err\_pd}(s)}\bigg|_{D(s)=0} = \left[\frac{k_i + k_p s}{s^2\left[s\left(\frac{2}{k\omega_{SOGI}}\right)+1\right]}\right]\left[\frac{s^2+\omega_n^2}{s^2+\frac{\omega_n}{Q_n}s+\omega_n^2}\right] \quad \textbf{(4-39)}$$

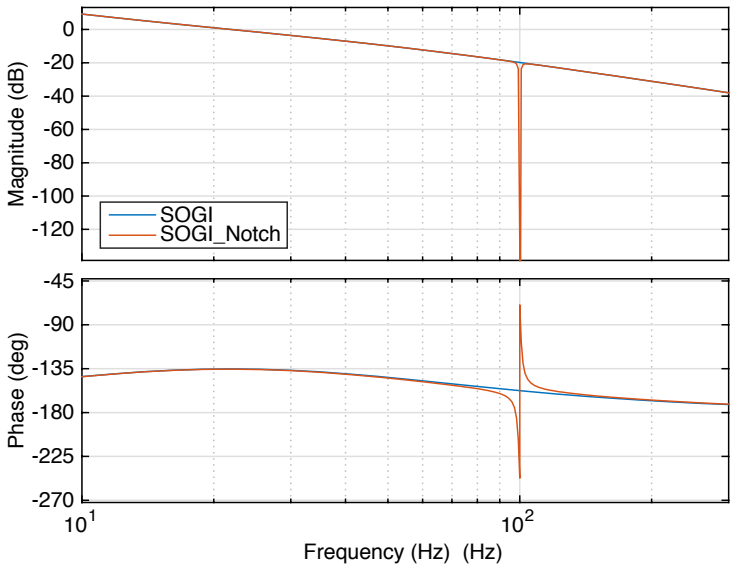


Fig. 4-13 SOGI PLL vs. SOGI PLL with notch filter open loop Bode plot

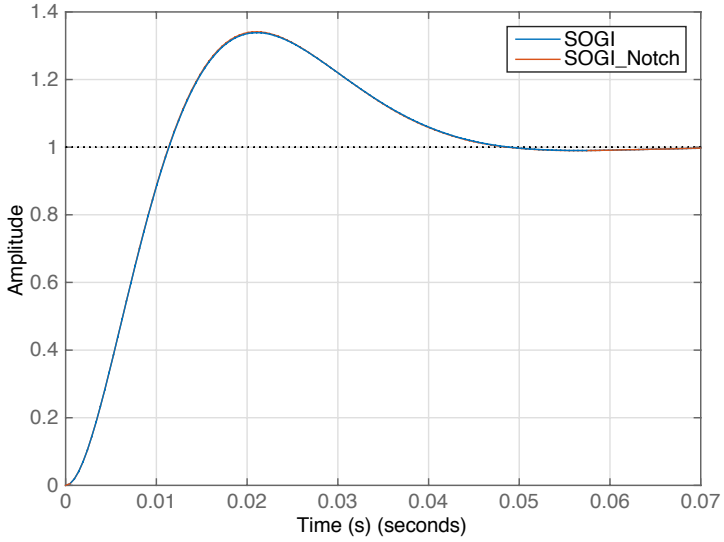


Fig. 4-14 SOGI PLL vs. SOGI PLL with notch filter closed loop transient response

The output harmonics of the modified PLL in response to 3rd harmonic distortion in the input signal can be estimated as was for the conventional SOGI PLL by considering that the 2nd harmonic is not present in the LF input following the notch filter. Therefore, the equation for the predicted output signal is given as (4-40). It is evident that the output contains 3rd and 5th harmonics (smaller in magnitude relative to the reference SOGI PLL) as a result

of the interaction between the 4th harmonic and ωt components passing through the cosine function. The magnitudes of the 3rd and 5th harmonics are defined in (4-41). The analytical prediction and time domain simulation results of the modified PLL for various input signal 3rd harmonic levels and PLL configurations (with gains as shown in Table 4-1) is presented in Table 4-3 as a validation of the accuracy of the prediction.

$$v_{n\_SOGI\_out} = k_5 \cos[\omega t] - \frac{1}{2}(k_6 \cos[\phi_{v1}]) \cos[3\omega t] + \frac{1}{2}(k_6 \cos[\phi_{v1}]) \cos[5\omega t] + \frac{1}{2}(k_6 \sin[\phi_{v1}]) \sin[3\omega t] - \frac{1}{2}(k_6 \sin[\phi_{v1}]) \sin[5\omega t] \quad \textbf{(4-40)}$$

$$V_{n\_SOGI\_h3} = V_{n\_SOGI\_h5} = \frac{\sqrt{k_6^2}}{2} \quad \textbf{(4-41)}$$

Table 4-3 Output to 3rd harmonic distortion in input for SOGI PLL with notch filter (Q_n=55) method – A (2 different gain configurations for the same PLL topology)

PLL Configuration	150 Hz Input	Simulink PLL Output Harmonic Magnitudes		Analytical PLL Output Harmonic Magnitudes		Simulink vs. Analytical Deviation	
		150 Hz	250 Hz	150 Hz	250 Hz	150 Hz	250 Hz
SOGI PLL – 1 (With Notch filter - A)	5%	0.060%	0.058%	0.056%	0. 056%	**6.00%**	**2.76%**
	10%	0.120%	0.116%	0.113%	0.113%	**6.00%**	**2.84%**
	15%	0.180%	0.175%	0.169%	0.169%	**5.99%**	**2.98%**
SOGI PLL – 2 (With Notch filter - A)	5%	0.066%	0.064%	0.062%	0.062%	**6.18%**	**3.12%**
	10%	0.133%	0.129%	0.124%	0.124%	**6.25%**	**3.19%**
	15%	0.199%	0.193%	0.187%	0.187%	**6.33%**	**3.32%**

Therefore, it can be concluded that the modified SOGI PLL effectively rejects the 3rd harmonic present in the utility grid. Furthermore, the analytical prediction of the modified PLL provides a good estimate of the performance

improvement that can be expected with the addition of the notch filter in the rotating frame.

4.2.3.2. Method B – SOGI PLL with notch filter in the input stage

It was shown that the application of a notch filter at double the fundamental frequency after the DQ transformation could improve the 3rd harmonic rejection capability of the SOGI PLL.

However, since the DQ transformation also generates a 4th harmonic component (150 Hz + 50 Hz), the resulting PLL output still contained a small amount of 3rd and 5th harmonic distortion.

Therefore, an alternative solution to significantly reduce the influence of the 3rd harmonic input distortion is to insert a notch filter tuned at 150 Hz at the input port of the SOGI PLL, which would nullify the offending frequency component. The proposed PLL structure is illustrated in Fig. 4-15. As was the case of Method A, the notch frequency is dynamically adjusted with the use of the PLL frequency output variable.

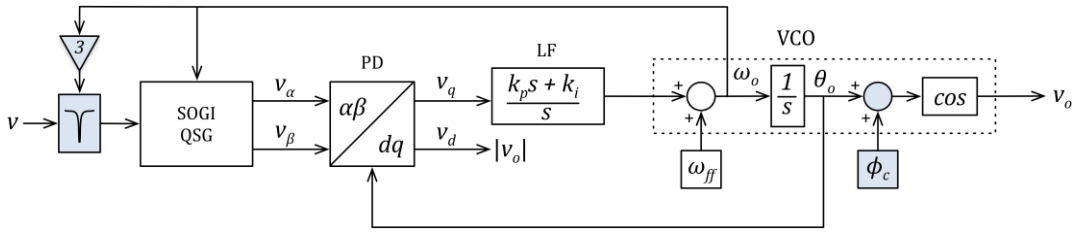


Fig. 4-15 Method B – SOGI PLL with notch filter in the input stage

The value for Q_n is kept at the same 55 that was chosen for Method A since the requirement for the filter's sharpness characteristics are similar. However a small, but finite amount of phase shift produced by the notch filter at the fundamental frequency causes the PLL output signal to also be phase shifted by the same amount.

Summing the phase shift amount (ϕ_c) to the PLL theta signal as shown in Fig. 4-15 can easily compensate this effect. By evaluating the transfer function of the 150 Hz notch filter at the fundamental frequency, it is found that the 50 Hz fundamental signal undergoes a 0.39° phase shift. Therefore ϕ_c is set to 0.39°.

It must be noted that a low value of Q_n would mean that the amount of phase shift for the fundamental frequency component would vary significantly even with a slight change in the utility frequency, making the phase shift compensation more complicated.

The effectiveness of the two types of modified SOGI PLL have been verified in Simulink under the same input conditions (with 15% 3rd harmonic distortion) and are presented in Table 4-4 along with the results of the reference SOGI PLL. Therefore, it can be observed that both methods are able to supress the effect of the 3rd harmonic input while Method B is able to almost completely supress the 3rd harmonic pollution of the utility voltage.

Table 4-4 Comparison of PLL simulation results for input signal with 15% 3rd harmonic distortion

PLL	Output 3rd Harmonic	Output 5th Harmonic	Output THD
SOGI - Reference	0.908%	0.179%	0.93%
SOGI Notch - A	**0.180%**	**0.175%**	**0.25%**
SOGI Notch - B	**0.029%**	**0.006%**	**0.03%**

4.2.4. Practical implementation and performance comparison

The two proposed methods of the SOGI PLL along with the reference SOGI PLL (all three PLLs set up with the "SOGI PLL – 1" settings from Table 4-1) have been tested in hardware-in-the-loop (HIL) simulation on an RM46L852 (ARM Cortex-R4) CPU control card. The input signal to the PLL has been software generated internally in the CPU and 5 different tests that simulate

abnormal grid conditions have been carried out. The C code of the PLLs are presented in Appendix D.

These tests are:

1. Frequency jump of 5 Hz
2. Phase jump of 40°
3. Voltage sag by 30%
4. Simultaneous voltage sag (30%) and phase shift (40°)
5. Distorted grid conditions (70% clipped voltage resulting in a THD of 13.76%).

The HIL simulation process consists of generating the input signal to the PLL in the target CPU (Cortex-R4) which is then passed to the PLL code (which also runs in the same CPU) as illustrated in Fig. 4-16.

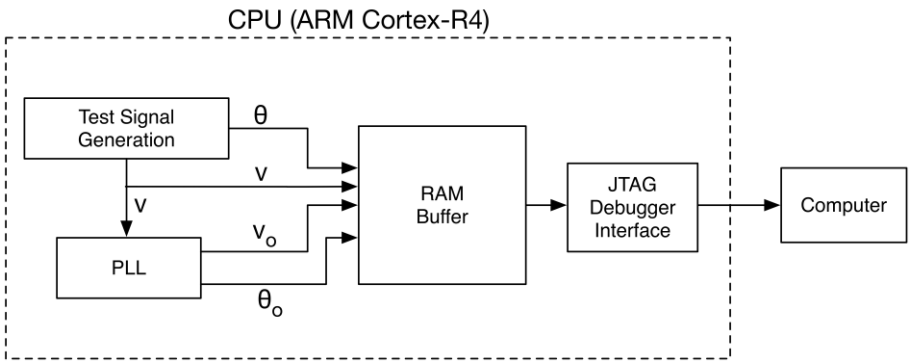


Fig. 4-16 Hardware in the loop simulation setup in Cortex-R4 CPU

The generated signal, its phase angle, the output signal from the PLL as well as the phase angle from the PLL is stored in the random access memory (RAM) of the CPU for the duration of the transient test. After the transient, the data is exported to MATLAB through the RAM export function of the CPU debugger software for data analysis and plotting. The resulting waveforms are

presented in Fig. 4-17 to Fig. 4-22 and the comparison is summarised in Table 4-5.

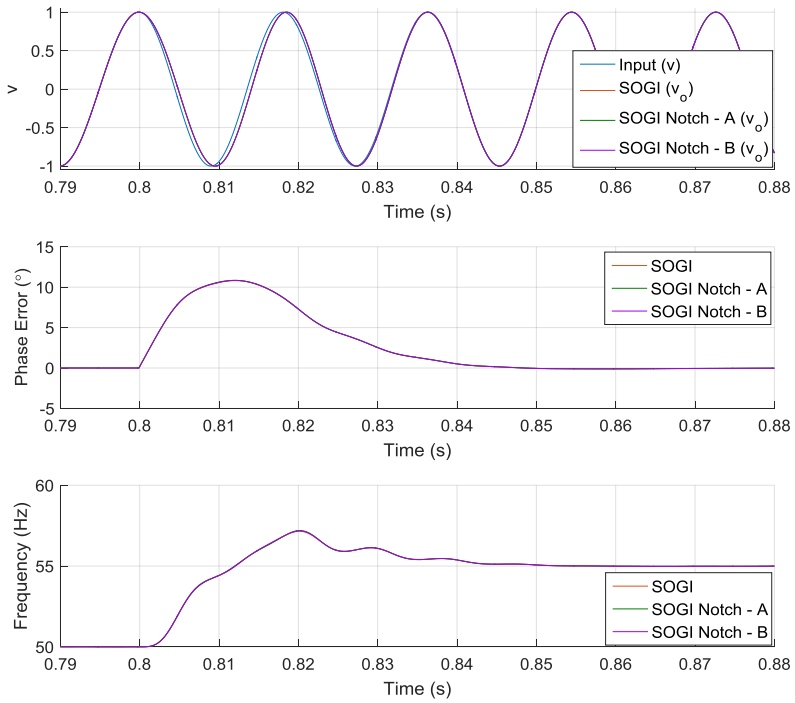


Fig. 4-17 Frequency jump of 5 Hz – (with SOGI PLL – 1 settings: k = 2.1, k_p = 137.5, k_i = 7878)

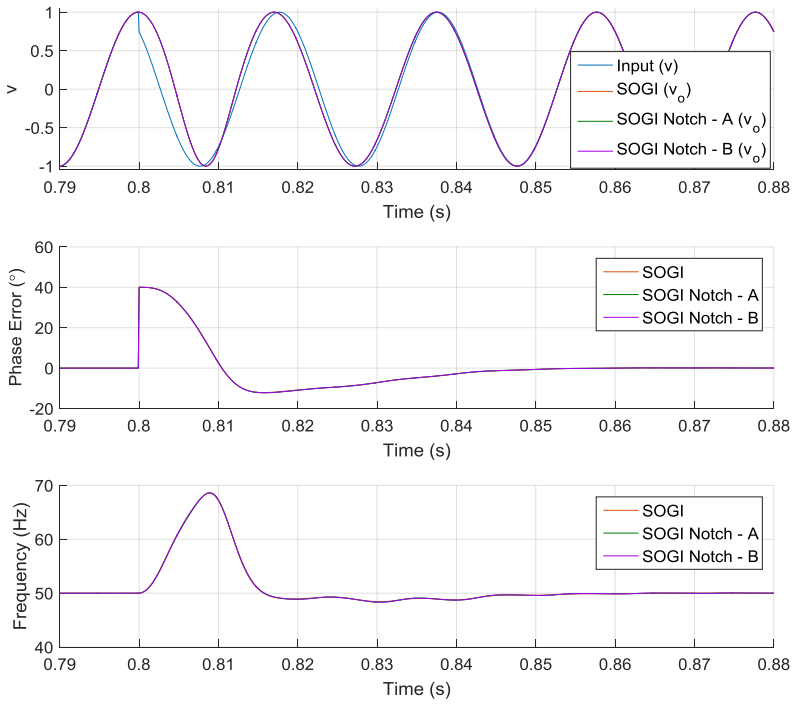


Fig. 4-18 Phase jump of 40° – (with SOGI PLL – 1 settings: k = 2.1, k_p = 137.5, k_i = 7878)

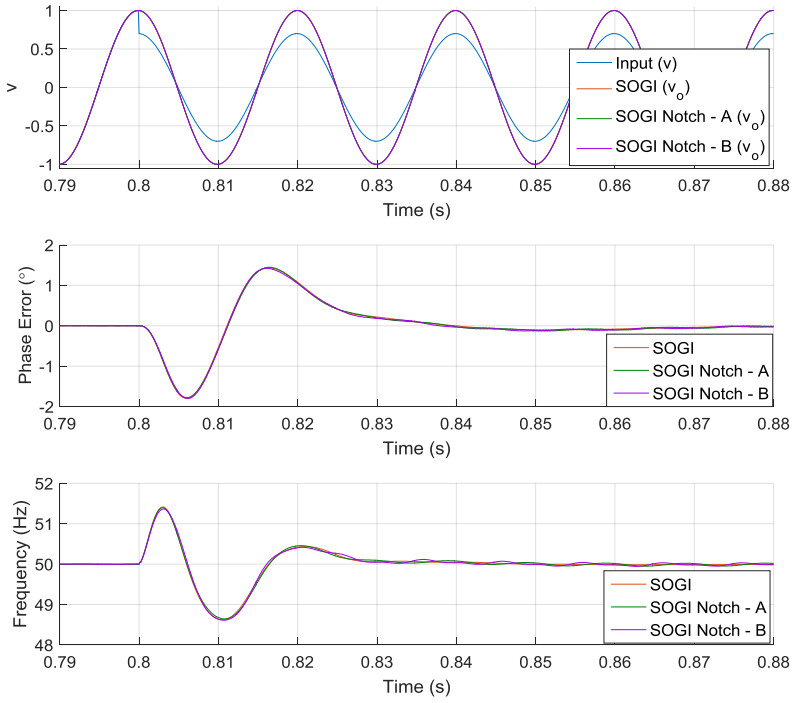


Fig. 4-19 Voltage sag by 30% – (with SOGI PLL – 1 settings: k = 2.1, k_p = 137.5, k_i = 7878)

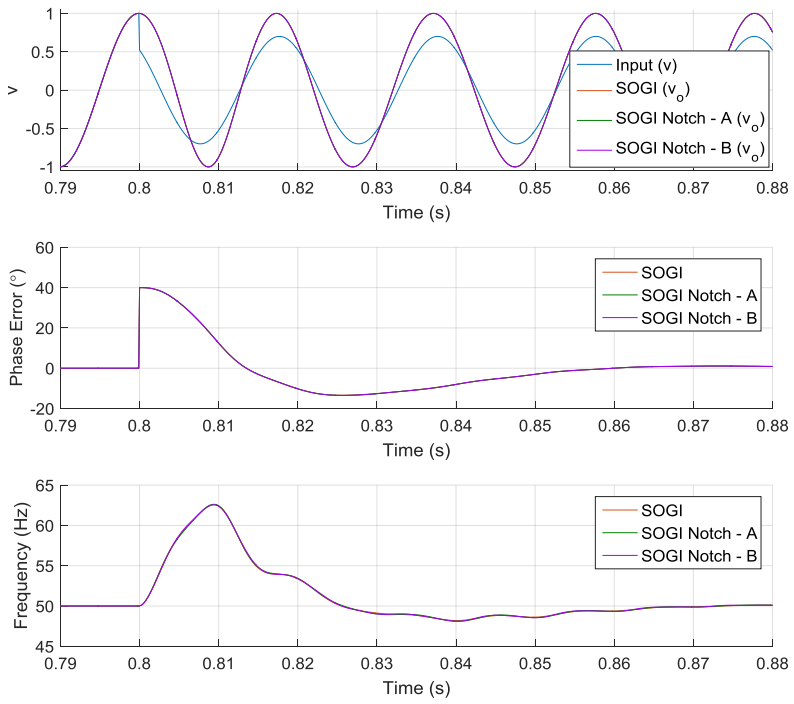


Fig. 4-20 Phase jump of 40° with voltage sag by 30% – (with SOGI PLL – 1 settings: k = 2.1, k_p = 137.5, k_i = 7878)

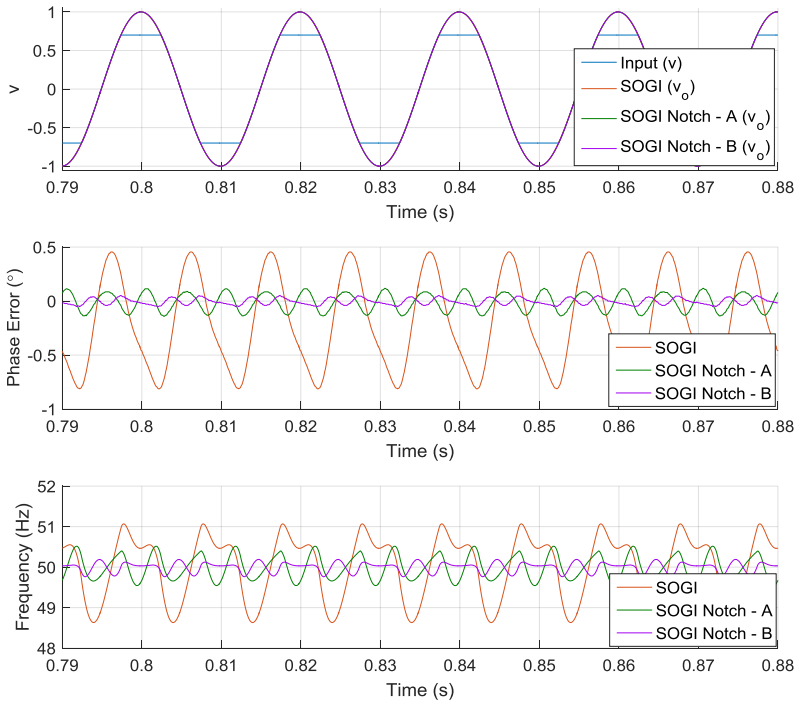


Fig. 4-21 Distorted grid conditions (clipped at 70%) – (with SOGI PLL – 1 settings: k = 2.1, k_p = 137.5, k_i = 7878)

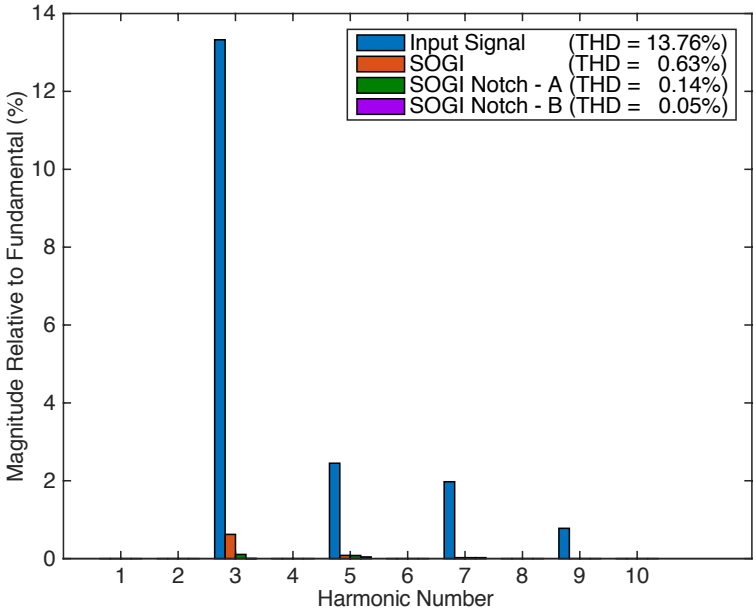


Fig. 4-22 Frequency spectrum of input and output signals for distorted grid conditions (clipped at 70%) – (with SOGI PLL – 1 settings: k = 2.1, k_p = 137.5, k_i = 7878)

Table 4-5 Results of HIL simulation for grid anomalies – settling times and THD

PLL	Frequency jump	Phase jump	Voltage sag	Voltage & phase jump	Distorted grid (output THD)	CPU Time
Ref. SOGI	44 ms	48.9 ms	30.7 ms	81.8 ms	0.63%	7.2 µs
SOGI Notch - A	**43.8 ms**	**49 ms**	**29.9 ms**	**81.9 ms**	**0.14%**	**10 µs**
SOGI Notch - B	**43.8 ms**	**49.1 ms**	**29.2 ms**	**82.3 ms**	**0.05%**	**10.2 µs**

It is evident that the transient performance of the two modified PLLs is approximately the same as the reference SOGI design. Also, it can be seen that both the modified PLLs provide improved harmonic rejection while Method B has the best performance due to the total cancellation of the 3rd harmonic influence before any harmonic products are formed in the phase detector.

Furthermore, it can be seen that the additional of the notch filters has caused an increase in the computation time from the 7.2 µs required for the SOGI to 10 µs and 10.2 µs for the SOGI Notch – A and SOGI Notch – B

respectively (CPU speed at 220 MHz). The addition of the notch filters do not require any specialised mathematical functions.

4.2.5. Summary

Although the methods that were presented only focussed on the 3rd harmonic rejection, it is possible to cascade multiple notch filter stages at the input of the conventional SOGI to provide rejection of the other less prominent grid harmonics if required. However, it must be noted that the overall phase shift of the notch elements must be compensated at the output stage of the PLL.

4.3. PIIR based PLL for grid synchronisation

A new class of IIR (infinite impulse response) filters has been presented in [Appendix C] which has been referred to as the PIIR (phasor IIR) filter. A PLL based on this novel filter has also been introduced in the same literature for the application in gravitational wave detector data.

In this section, we explore the viability of the PIIR filter's adaptation for forming a PLL structure for use in grid converters. The PIIR filter block shall be treated as a black box since the design aspects of the filter is outside the scope of this thesis.

4.3.1. PIIR filter

The PIIR filter functions as a resonant band-pass filter with two outputs consisting of an in-phase *(I)* and quadrature *(Q)* signal output similar to the SOGI QSG that was discussed in the previous section. The inputs to the PIIR

block consist of the input signal and a control signal termed the phase shift per sample *(Δ)*, which determines the filter's resonant frequency and therefore the output signal frequency. The input and output ports of the PIIR are highlighted in Fig. 4-23.

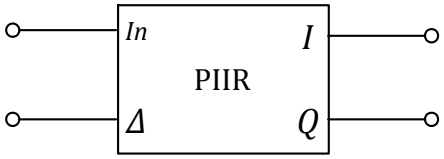


Fig. 4-23 PIIR filter input and output ports

The phase shift per sample, Δ is defined as given in (4-42) where f is the signal's frequency and τ_s is the sampling period of the filter. Furthermore, the PIIR filter response time is defined as τ, which determines the narrowness of the band-pass response as well as the transient response time.

$$\Delta = 2\pi f \tau_s \tag{4-42}$$

The transfer functions of the in-phase and quadrature signals are defined as given in (4-43) and (4-44) respectively where A, B, P, Q and ω_p are given in (4-45)-(4-49).

$$H_I(z) = \frac{2\omega_p \left\{ \left[\frac{\sin B}{P} \sin(\Delta - A) + \frac{\cos B}{Q} \cos(\Delta - A) \right] z^2 + (1 - \omega_p) \left[\frac{\sin A \sin B}{P} - \frac{\cos A \cos B}{Q} \right] z \right\}}{z^2 - 2\left[(1 - \omega_p)\cos\Delta\right] z + (1 - \omega_p)^2} \tag{4-43}$$

$$H_Q(z) = \frac{2\omega_p \left\{ \left[\frac{\cos B}{P} \sin(\Delta - A) - \frac{\sin B}{Q} \cos(\Delta - A) \right] z^2 + (1 - \omega_p) \left[\frac{\sin A \cos B}{P} + \frac{\cos A \sin B}{Q} \right] z \right\}}{z^2 - 2\left[(1 - \omega_p)\cos\Delta\right] z + (1 - \omega_p)^2} \tag{4-44}$$

$$A = \frac{1}{2}\left[\Delta + atan2\left(\frac{(2 - \omega_p)\tan\Delta}{\omega_p}, 1\right)\right] \tag{4-45}$$

$$B = \frac{1}{2}\left[\Delta - atan2\left(\frac{(2 - \omega_p)\tan\Delta}{\omega_p}, 1\right)\right] \tag{4-46}$$

$$P = 1 - \frac{\omega_p}{\sqrt{\omega_p^2 + 4(1-\omega_p)sin^2\Delta}} \quad \textbf{(4-47)}$$

$$Q = 1 + \frac{\omega_p}{\sqrt{\omega_p^2 + 4(1-\omega_p)sin^2\Delta}} \quad \textbf{(4-48)}$$

$$\omega_p = \frac{\tau_s}{\tau} \quad \textbf{(4-49)}$$

Based on the above transfer functions, the Bode plots of the in-phase and quadrature signals are presented in Fig. 4-24 and Fig. 4-25 respectively for different values of τ. It can be seen that the higher values of τ offer a sharper response. However, higher values of τ also entail a longer settling time as shown in the step response plot for the in-phase signal in Fig. 4-26 for different values of τ. It must be noted that the final value of the transient response has a DC component since the Bode plot has a finite gain at DC.

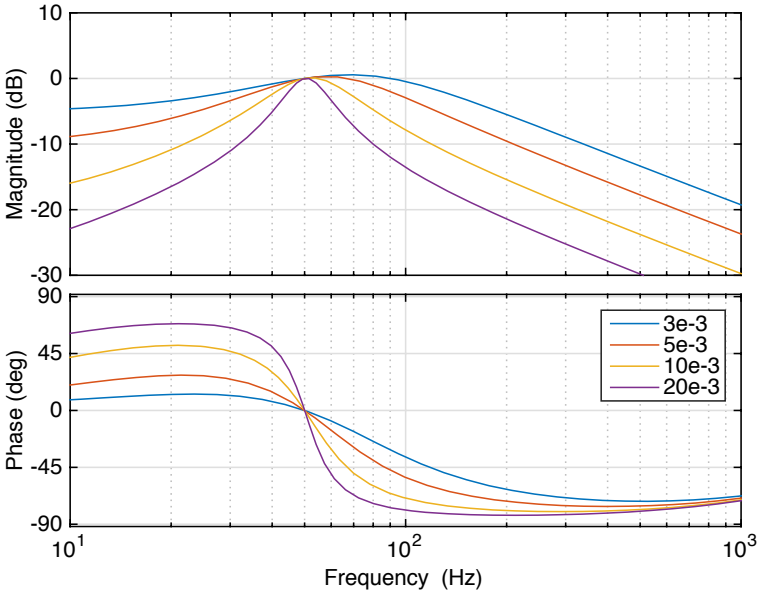


Fig. 4-24 Bode plots of in-phase signal for different values of τ

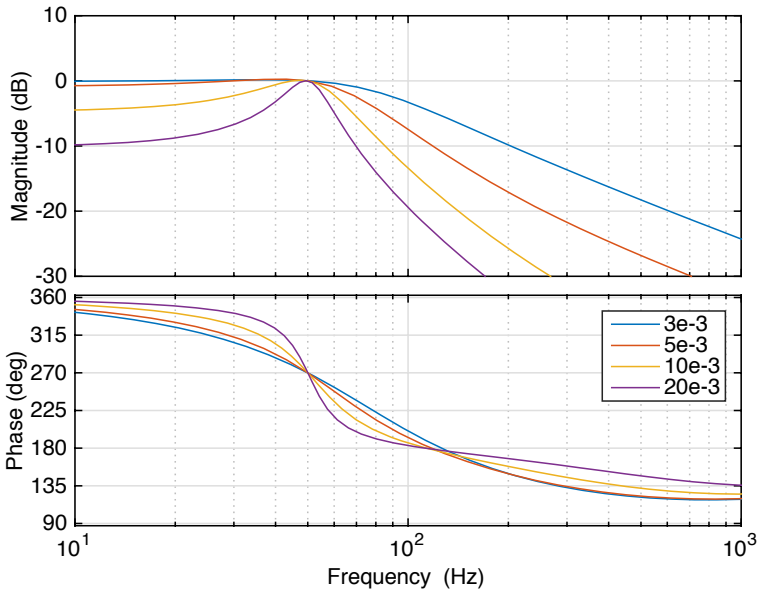


Fig. 4-25 Bode plots of quadrature signal for different values of τ

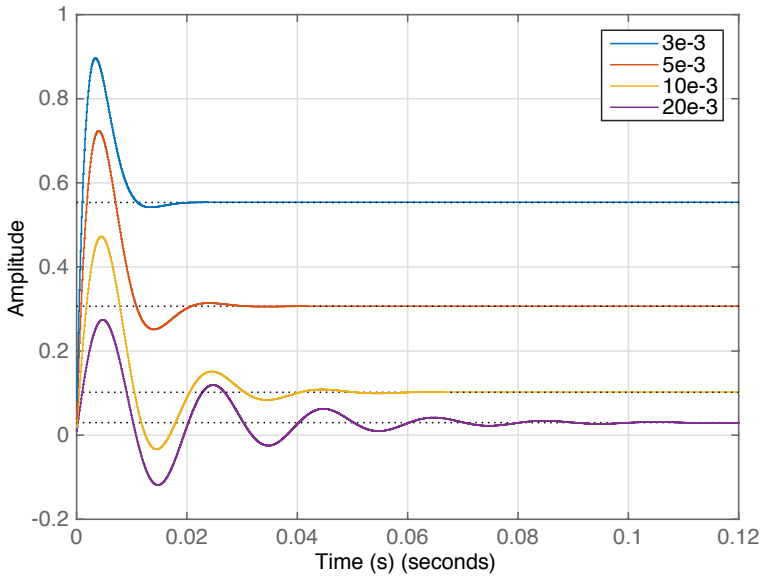


Fig. 4-26 Step response of in-phase signal for different values of τ

The PIIR filter maintains a natural phase relationship to the signal, therefore in the application of the PLL; the locking mechanism is in the frequency parameter space [Appendix C].

4.3.2. PIIR PLL

The PIIR PLL has been presented in [Appendix C], however an alternative topology for the PLL is used as depicted in Fig. 4-29 hereafter, which was found to provide the optimum performance for application in grid converters. The modifications to the method presented in [Appendix C] include the addition of 3rd and 5th harmonic pre-filters as well as the use of *atan2* function for generating the output as opposed to using the '*I*' signal directly. These modifications were required to meet the harmonic rejection capabilities for grid converter application as the harmonic attenuation of the PIIR PLL under distorted grid conditions was unsatisfactory as shown in Fig. 4-27 and Fig. 4-28 where it is compared with the SOGI PLL (it can be seen that the SOGI PLL output THD is only 0.63% whereas the THD of the PIIR PLL output is 9.25%). The optimised version of the PIIR for grid application will from now on be referred to as the "enhanced PIIR PLL".

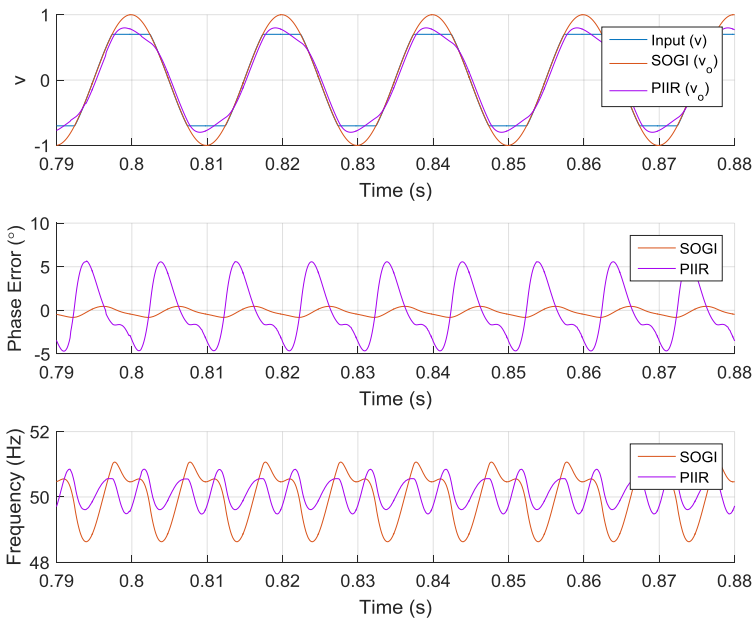


Fig. 4-27 Comparison of SOGI (SOGI PLL – 1) with PIIR PLL for distorted grid conditions (clipped at 70%)

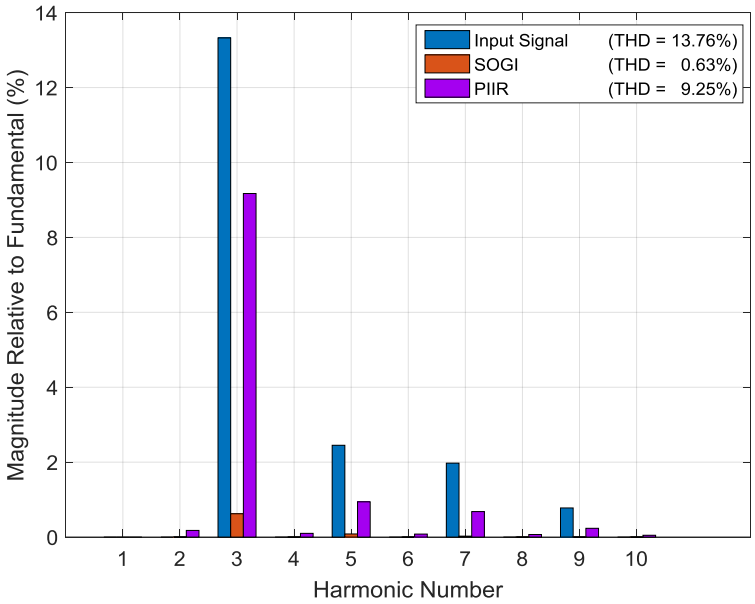


Fig. 4-28 Comparison of SOGI (SOGI PLL – 1) with PIIR PLL for distorted grid conditions (clipped at 70%) – Frequency spectrum of input and output signals

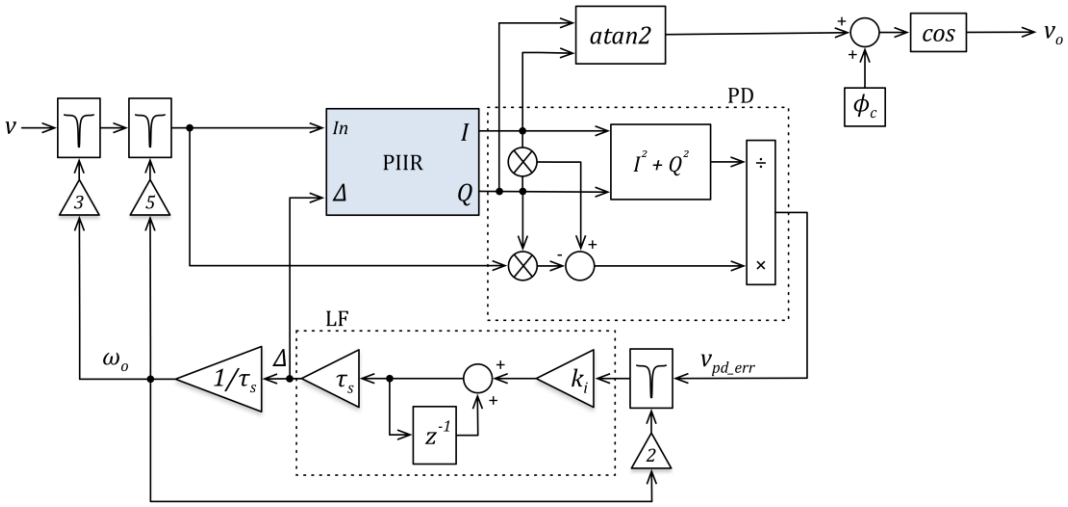


Fig. 4-29 Basic structure of the PIIR PLL

The main component of the PLL consists of the PIIR filter, which was discussed previously and can be thought of as a VCO in terms of the traditional PLL architecture. The feedback path is utilised for determining the phase shift per sample that the PIIR filter requires for maintaining the synchronisation to the input signal and is composed of a phase detector and loop filter. In addition,

the input of the PLL undergoes harmonic pre-filtering for 3rd and 5th harmonics similar to the SOGI with notch filter that was presented in the previous section.

Phase detector (PD)

The phase detector consists of the subtraction of two signals that are obtained by the multiplication of the 'I' and 'Q' outputs of the PIIR filter and the multiplication of the input signal and the 'Q' output of the PIIR filter. The resulting signal is divided by the sum of 'I' and 'Q' squares in order to make the gain of the PLL independent of the input signal magnitude. A similar topology of phase detector has been introduced in [161] for eliminating the double frequency oscillation at steady state for standard PLLs.

Therefore, the analysis of the phase detector can be done following a similar method to [161] as follows.

The PIIR filter's input signal v, outputs v_I and v_Q can be defined as given in (4-50)-(4-52) where ω, ϕ, ω_o and ϕ_o represents the angular frequency and phase of the input and output signals of the PIIR filter.

$$v = V\sin(\theta) = V\sin(\omega t + \phi) \quad \textbf{(4-50)}$$

$$v_I = V_I\sin(\theta_o) = V_I\sin(\omega_o t + \phi_o) \quad \textbf{(4-51)}$$

$$v_Q = -V_Q\cos(\theta_o) = -V_Q\cos(\omega_o t + \phi_o) \quad \textbf{(4-52)}$$

In the PIIR filter, there is unity gain for the fundamental component (ω) for both the in-phase and quadrature outputs. Therefore, the phase detector output is independent of the input signal magnitude due to the division by the $I^2 + Q^2$ term. Hence the PD's error output, v_{pd_err} is simplified as given in (4-53).

$$v_{pd\_err} = \frac{\sin(\theta - \theta_o)}{2} + \sqrt{\frac{1 - \cos(\theta - \theta_o)}{2}} \sin\left[2\theta_o + \tan^{-1}\left(\frac{\sin(\theta - \theta_o)}{\cos(\theta - \theta_o) - 1}\right)\right] \quad \textbf{(4-53)}$$

It can be seen that when the PLL is locked (both frequency and phase), the output of the PD is zero with no oscillations. Furthermore when only the frequencies are matched and there is a phase difference, the PD output contains a DC value that is proportional to the difference in phase as well as a double frequency component. The notch filter that follows the PD is added to reduce the effect of this double frequency ringing during transient conditions so as to improve settling time of the PLL similar to the method employed in [Appendix I]. It was found that the quality factor of the notch filter affected the settling times of the various transient conditions (such as phase jump, frequency jump, voltage sag and voltage sag with phase jump) differently. Therefore, a quality factor value of 10 was chosen after iterative tests to give a reasonable compromise between the performances of the different tests.

Loop filter (LF)

The loop filter consists of a backward Euler integrator with an integral gain of k_i. The loop filter forms the function of providing the value of Δ for the PIIR filter in order to lock on to the input signal without any steady state error in frequency and phase.

The initial output value of the integrator is set to the phase shift per sample, Δ that corresponds to the nominal grid frequency (50 Hz). As the selection of k_i affects the performance of different transient tests in different ways, k_i was selected to give a reasonable compromise between the transient tests. A value of 14 was chosen for the HIL simulations after iterative tests which was found to be stable under all the transient test conditions.

Harmonic pre-filtering

The input to the PLL structure undergoes harmonic filtering for 3rd and 5th components with the use of two cascaded notch filters both having a quality factor of 55. This was found to be necessary as the low value of τ required ($3e^{-3}$) to ensure fast transient response time of the PLL also dramatically reduces the harmonic rejection capability of the PIIR filter. The phase shift induced by the cascaded notch filters is compensated by adding the phase offset (0.6°) after the calculation of phase angle.

The output phase angle of the PLL is derived by the arctangent function of the '*I*' and '*Q*' outputs of the PIIR filter. Furthermore, the sampling frequency of the PIIR PLL has been chosen as 10 kHz.

PLL stability

The stability of the PLL is determined by the feedback gain, i.e. beyond a certain limit for k_i, the loop stability is not guaranteed. It was found through MATLAB simulation that k_i values over 100 results in sustained phase oscillations. Therefore the chosen k_i of 14 is well below the stability margins for the PLL configuration.

4.3.3. Optimised implementation

It was shown that the feedback variable of the PIIR PLL was the phase shift per sample *(Δ)*. As a consequence, the PIIR filter coefficients also become variable during the operation of the PLL and hence must be re-evaluated for each sampling period. Since the coefficient calculations are complex and time consuming for practical implementation, Edo et al. [170] has developed an alternative method for closed loop operation of the PIIR PLL in an FPGA system.

The method consists of pre-calculating the coefficients of the PIIR filter for the nominal value of Δ after which the sampling frequency of the filter is

adjusted (around the nominal 10 kHz) in real time in response to the feedback from the phase detector. Therefore by adaptively changing τ_s, it is possible to keep the coefficients static at the predetermined initial values and have closed loop operation.

4.3.4. Practical implementation and performance comparison

The PIIR PLL configuration that is under investigation has been implemented on the ARM Cortex-R4 control card based on the variable sampling method that was developed by T. Edo [170] (The embedded C code for the enhanced PIIR PLL that was written based on the variable sampling LabView FPGA code that was developed by T. Edo [170] is presented in Appendix D). The performance has been evaluated using the same HIL method as was for the SOGI notch filter based PLL that was discussed in the previous section.

The tests that have been performed are highlighted below.

1. Frequency jump of 5 Hz
2. Phase jump of 40°
3. Voltage sag by 30%
4. Simultaneous voltage sag (30%) and phase shift (40°)
5. Distorted grid conditions (70% clipped voltage resulting in a THD of 13.76%).
6. DC bias conditions (2% DC offset)

The resulting comparison of the enhanced PIIR PLL with the reference SOGI PLL (with SOGI PLL – 1 settings: k = 2.1, k_p = 137.5, k_i = 7878) as well as the standard PIIR PLL is highlighted in Table 4-6 and Table 4-7. Furthermore, the comparative waveforms that were obtained are shown in Fig. 4-30 to Fig. 4-37.

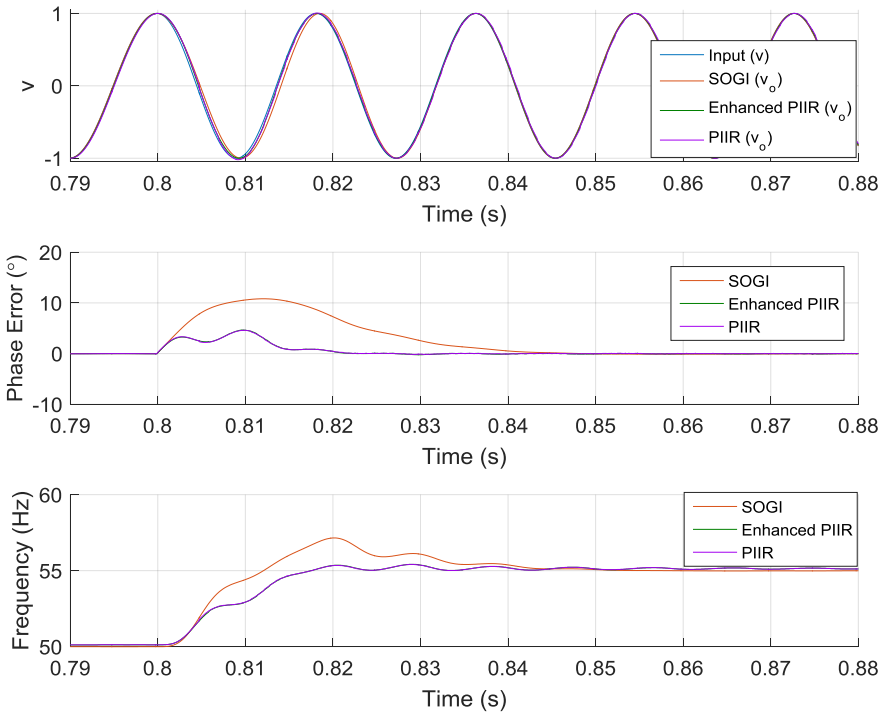


Fig. 4-30 Frequency jump of 5 Hz

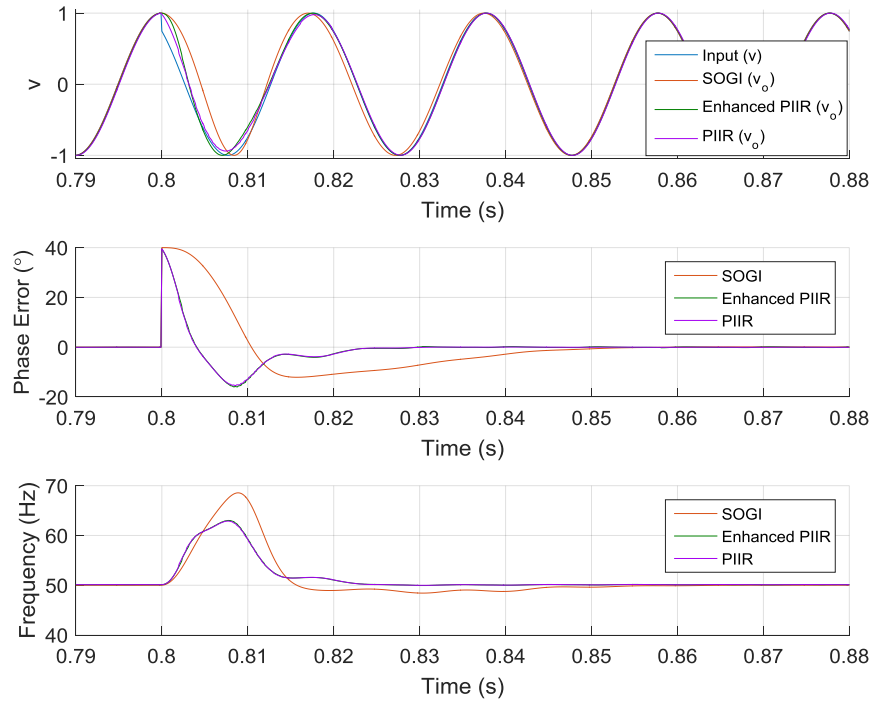


Fig. 4-31 Phase jump of 40°

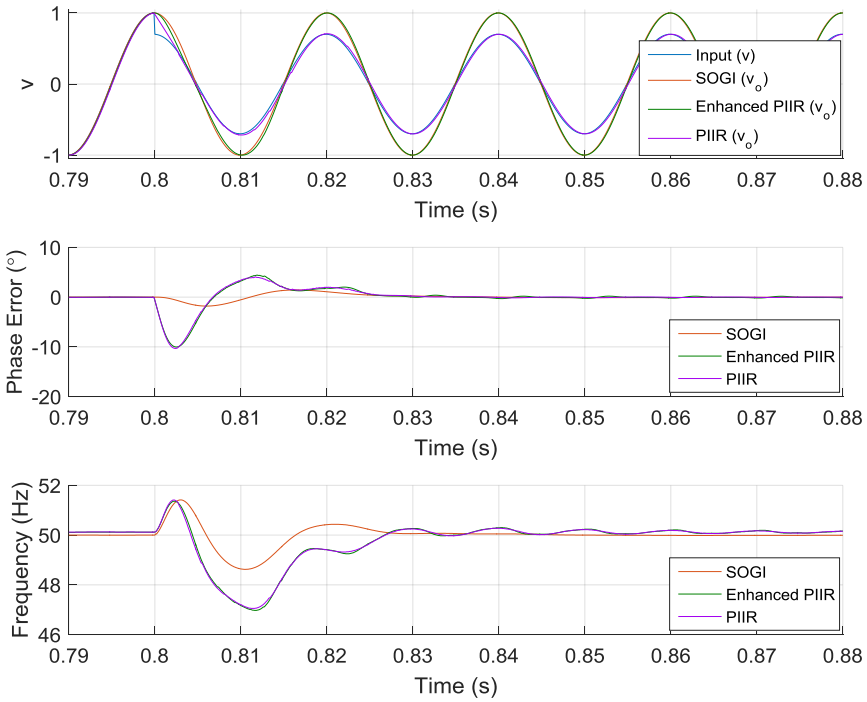


Fig. 4-32 Voltage sag by 30%

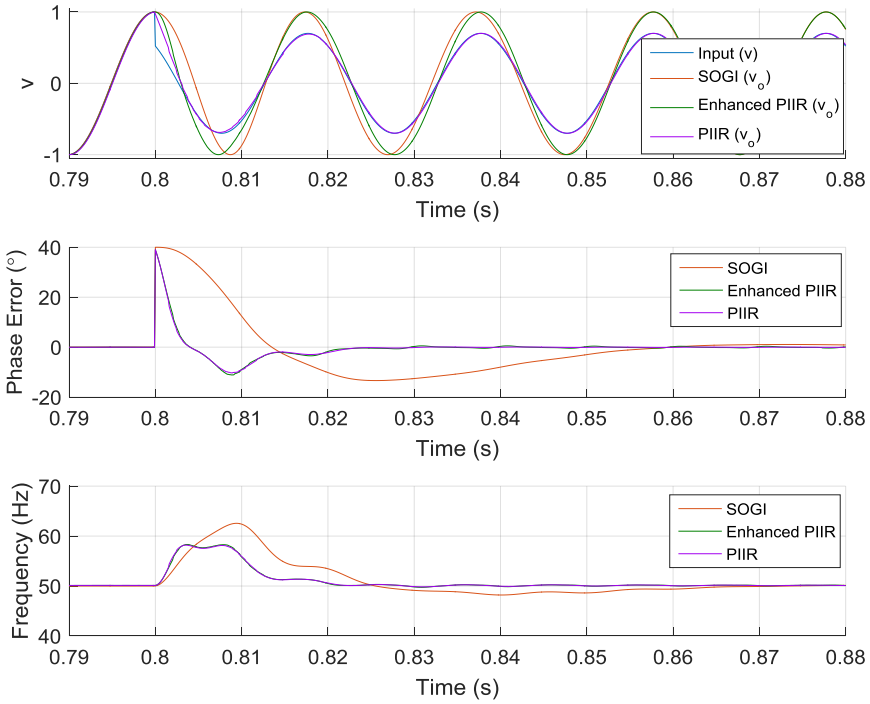


Fig. 4-33 Phase jump of 40° with voltage sag by 30%

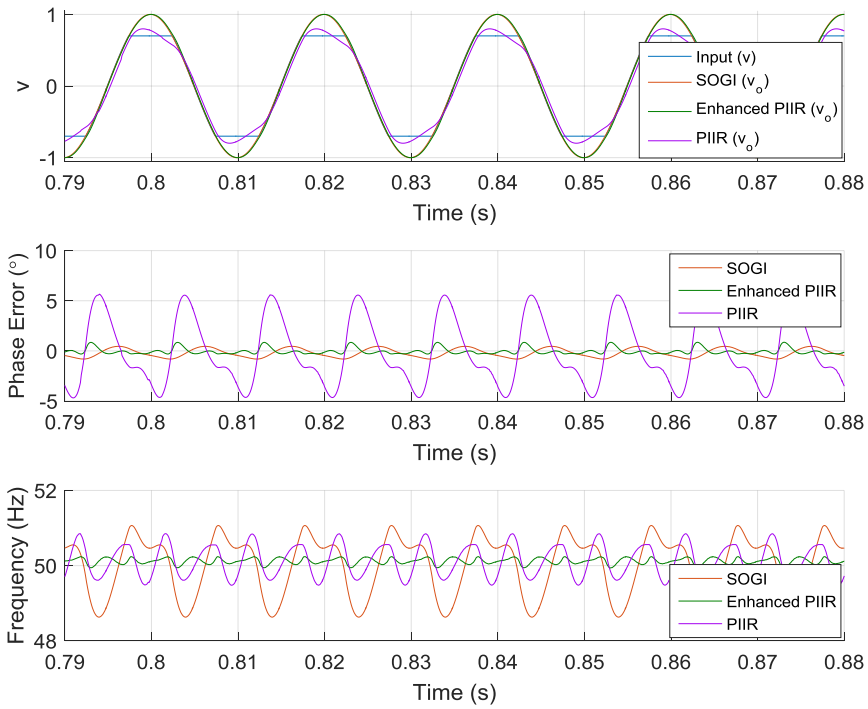


Fig. 4-34 Distorted grid conditions (clipped at 70%)

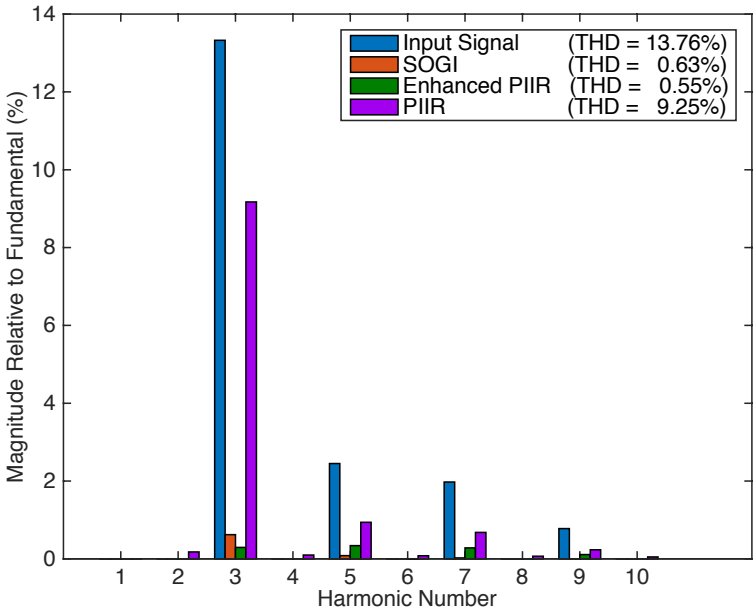


Fig. 4-35 Frequency spectrum of input and output signals for distorted grid conditions (clipped at 70%)

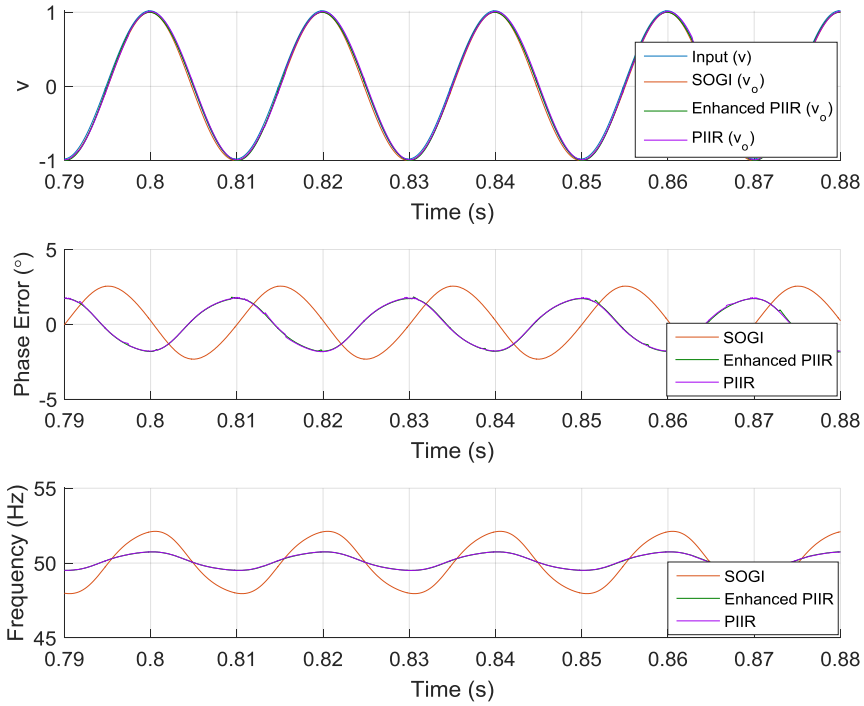


Fig. 4-36 DC bias conditions (2% offset)

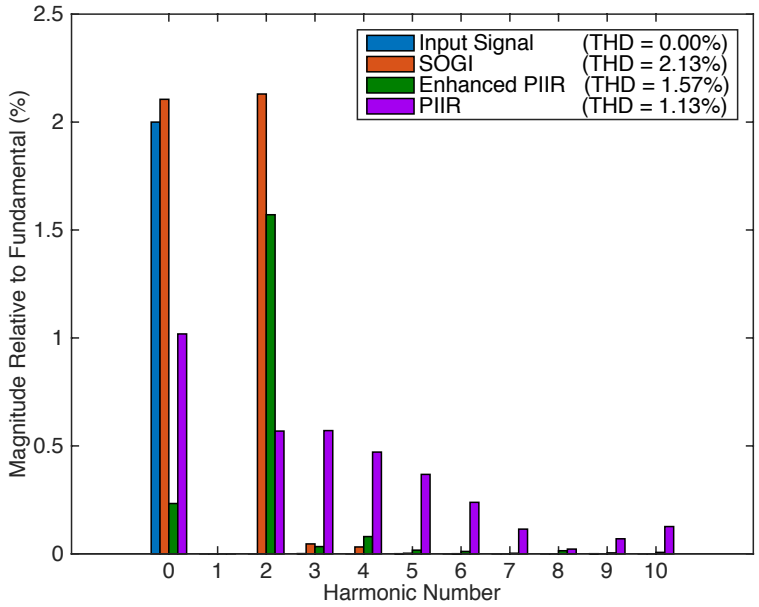


Fig. 4-37 Frequency spectrum of input and output signals for DC bias conditions (2% offset)

Table 4-6 Results of HIL simulation for grid anomalies – settling times and THD

PLL	Frequency jump	Phase jump	Voltage sag	Voltage & phase jump	Distorted (THD)	CPU Time
Ref. SOGI	44 ms	48.9 ms	30.7 ms	81.8 ms	0.63%	7.2µs
Enhanced PIIR	**30.3 ms**	**22.6 ms**	**50.8 ms**	**21.3 ms**	**0.55%**	**10.5µs**
PIIR	**21.2 ms**	**22.7 ms**	**30.2 ms**	**22.0 ms**	**9.25%**	**3.5µs**

Table 4-7 Results for HIL simulation for 2% DC offset condition

PLL	O/P DC Component	O/P 2nd Harmonic	O/P 3rd Harmonic	O/P THD
Ref. SOGI	2.10%	2.13%	0.05%	2.13%
Enhanced PIIR	**0.23%**	**1.57%**	**0.03%**	**1.57%**
PIIR	**1.02%**	**0.57%**	**0.57%**	**1.13%**

It can be seen that the phase jump and the frequency jump transient response times are significantly improved for the PIIR PLL as well as the enhanced PIIR PLL. In particular, the PLL is able to track the frequency change within 1.5 cycles and the phase change in about 1 cycle of the grid frequency.

However, the voltage sag performance of the enhanced PIIR PLL is worse than the SOGI PLL, taking an additional cycle to settle. The most significant improvement in terms of transient performance is the simultaneous voltage sag and phase jump transient condition in which the PIIR PLL and the enhanced PIIR PLL is able to recover within 1 cycle whereas the SOGI PLL takes an additional 3 cycles.

The negative effect due to the low value of τ that resulted in the fast response time in the PIIR PLL is the harmonic distortion performance where it can be seen that the output THD is 9.25%. In contrast, both the SOGI and the enhanced PIIR PLLs perform significantly better when under harmonic

disturbances with the enhanced PIIR PLL having a slightly better harmonic rejection capability. It must also be noted that the enhanced PIIR PLL exhibits less oscillation in the estimated frequency (0.3 Hz pk-pk) compared to the SOGI PLL (2.4 Hz pk-pk) and PIIR PLL (1.36 Hz pk-pk). This can be attributed to the input pre-filter stage similar to the reduction in frequency oscillation that was observed in the improved SOGI presented in the previous section. This may be a favourable property, which allows the operation under distorted conditions without false tripping which may be caused by a large frequency detection error.

With regard to performance under DC offsets in the input, it is seen that both types of PIIR PLL outperform the SOGI. In particular, the enhanced PIIR PLL has an 89% reduction in the output DC component and a 26% reduction in the THD of the output. This may be a favourable attribute for application in grid converters as well as motor drive systems since DC offsets in the feedback signals are common due to imperfections in the transducers, signal conditioning circuitry and ADCs.

In terms of computational complexity, it can be observed that the PIIR PLL requires 50% less CPU time than the SOGI PLL. However, due to the addition of the dual pre-filters as well as the *atan2* function, the enhanced PIIR PLL requires 45% more CPU time than the SOGI PLL. In practical implementation terms, all 3 types of PLL require less than 10% of the CPU time that is available when executing at a loop rate of 10 kHz and therefore are equally suitable for a grid converter application since ~90% of CPU time can be spared for the remaining control code.

4.3.5. Summary

This section has investigated the viability of a PLL structure based on the PIIR filter that was proposed in [Appendix C] for the application in grid synchronisation. Based on the performance benefits that were highlighted, it is

clear that the enhanced PIIR PLL can offer an attractive alternative to the conventional SOGI PLL that is widely used in grid converter applications.

4.4. Experimental implementation in converter

The two types of improved SOGI PLLs proposed in section 4.2 as well as the enhanced PIIR PLL that was analysed in section 4.3 has been implemented in the low frequency bidirectional charger (by embedding the C code of the PLL into the controller code) and the performance has been validated for both V2G and G2V modes at a power level of 2.2 kW at steady state conditions (transient tests have not been carried out due to time constraints and difficulty in emulating grid fault conditions). The following Fig. 4-38 to Fig. 4-41 highlights the waveforms that have been captured.

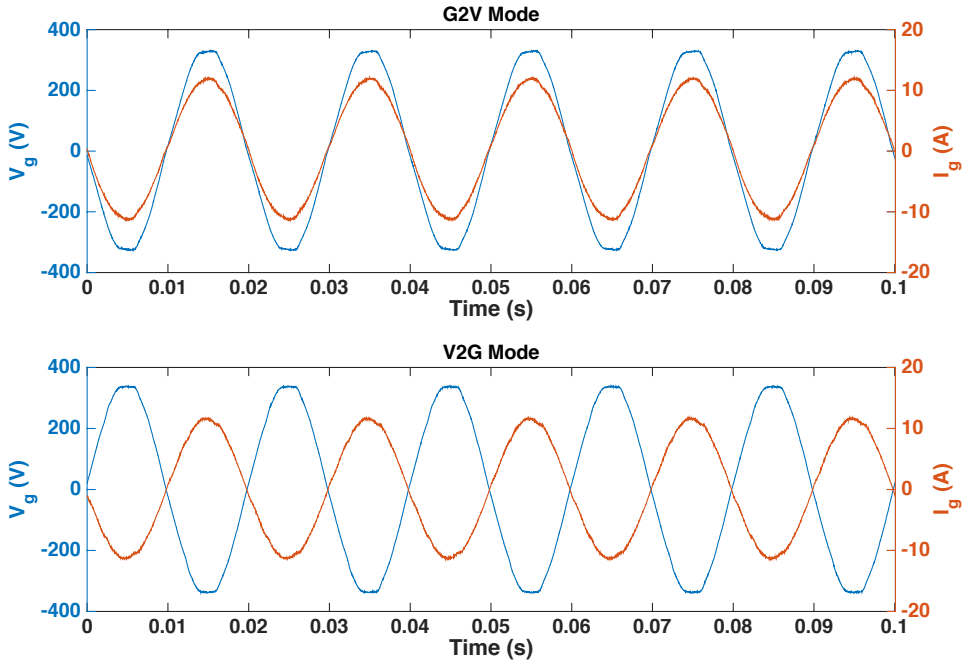


Fig. 4-38 SOGI PLL experimental results for G2V and V2G

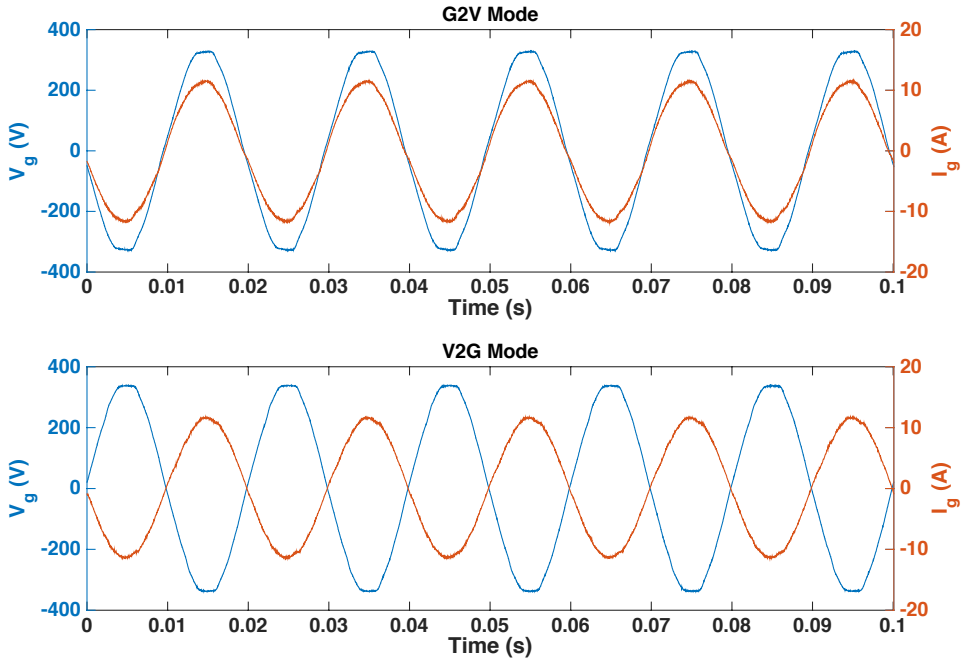


Fig. 4-39 SOGI Notch-A PLL experimental results for G2V and V2G

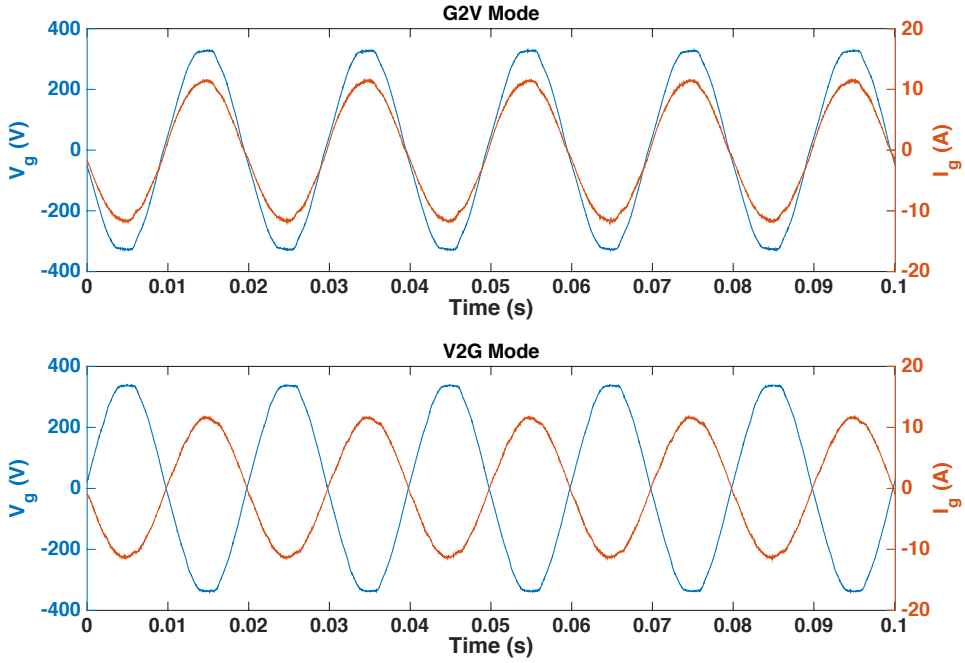


Fig. 4-40 SOGI Notch-B PLL experimental results for G2V and V2G

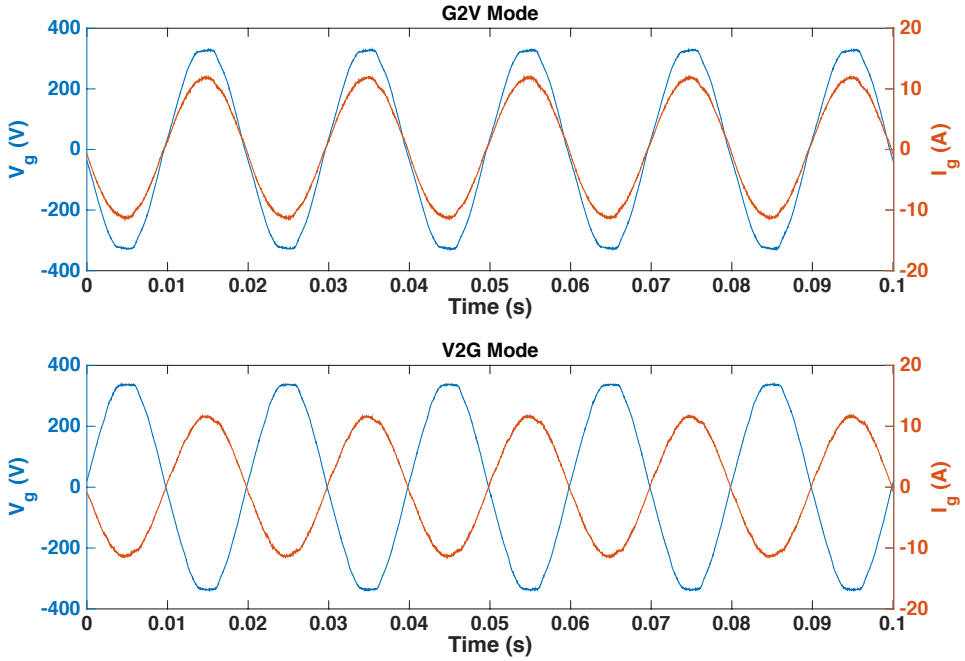


Fig. 4-41 Enhanced PIIR PLL experimental results for G2V and V2G

4.5. Conclusions

This chapter has focussed on two key contributions that have been made for improving the current state of the PLL techniques used for grid synchronisation.

The first section investigated the impact of 3rd harmonics on the performance of SOGI PLLs whereby an analytical method has been developed to predict the resulting output harmonic magnitudes. This has been followed by the proposal of two different methods to improve the harmonic rejection capability of the SOGI PLL. It was shown through HIL simulation results that the harmonic rejection performance could be dramatically improved by the addition of notch filters in either the feedback or pre-filter configurations.

The second part of the chapter investigated the PLL structure, which was based on the novel IIR filter proposed by Ed Daw *et al.* [Appendix C]. The operation of the enhanced PIIR PLL has been outlined after which it was shown

that the PLL shows desirable characteristics for grid synchronisation applications.

Furthermore, experimental results for both the improved SOGI as well as the PIIR PLLs were shown for both G2V and V2G modes of operation.

Chapter 5

Islanding Detection

In this chapter, a new method of islanding detection based on the signature of the PWM voltage harmonics is proposed. The viability of the algorithm is investigated with the use of an analytical model of the inverter; load and grid after which the SimPowerSystems simulation results for the system are presented. Furthermore, the new method is demonstrated in a hardware setup and the subsequent results are discussed.

5.1. Introduction

5.1.1. Islanding

Islanding is defined as the condition where the distributed generator (DG) continues to operate with local loads after the utility grid has been disconnected [44]. When an electric vehicle is equipped with a bi-directional battery charger, the energy in the battery can be fed to grid to support the grid operation, known as V2G operation, if required. Under this circumstance, the battery is, indeed, a DG source. Unintentional islanding is undesired since it is a hazard to utility workers and also due to the damage that can result to equipment due to asynchronous reclosure. Asynchronous reclosure occurs when the utility recloses while the DG is energised which is out of phase with the utility and therefore causing large currents to flow and hence damaging the DG converter infrastructure [18]. Islanding also has the potential to interfere with the power restoration service of the utility [171].

According to the IEEE1547 standard for interconnecting distributed resources with electric power systems, it is a requirement for grid connected DG systems to be able to detect islanding within 2 seconds and cease to

energise the area electrical power system (EPS) that is coupled through the point of common coupling (PCC) [172].

As a consequence, a diverse range of islanding detection methods have been developed and reported in literature each with their merits and limitations.

5.1.2. Anti islanding methods

Anti islanding methods are categorised into two main groups, which are passive methods and active methods. Active methods may be either inverter resident or non-inverter resident. In addition to the two main groups, there are also detection methods that rely on communication with the grid and inverter.

5.1.2.1. Non Detection Zones (NDZs)

One of the performance metrics among the many islanding detection methods is the concept of the NDZ. NDZ is the region in which the inverter is not able to identify that islanding has taken place. The conventional way to represent the NDZ is by highlighting the region of non-detection in a plot consisting of active and reactive power mismatch on the 2 axes. Fig. 5-1 (b) illustrates an example of the NDZ that is characteristic of the over/under voltage (OVP/UVP) and over/under frequency (OFP/UFP) based passive detection schemes. The reactive power mismatch (ΔQ) is defined as the difference in power between the inverter's reactive power output (typically zero) and the load's reactive power consumption. Similarly, the active power mismatch (ΔP) is the difference in power between the inverter's real power output and the load's real power consumption. The mismatched power is supplied/absorbed by the grid and low values of power mismatch makes detection challenging particularly for the passive methods of detection.

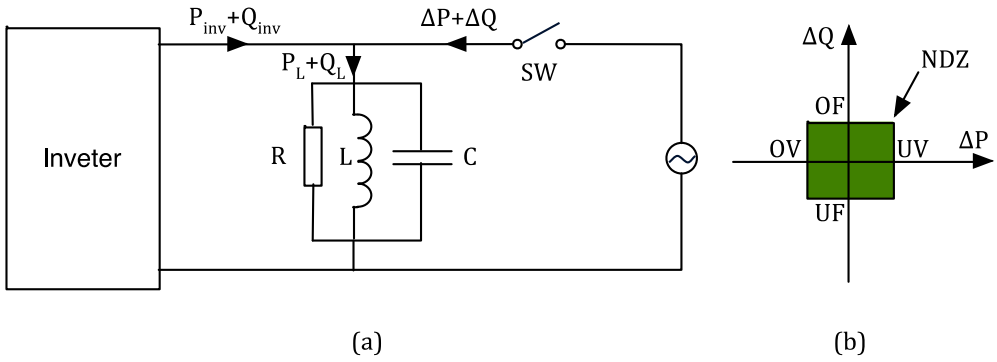


Fig. 5-1 (a) Power flow between inverter, load and grid (b) NDZ of OVP/UVP and OFP/UFP methods

The NDZ for commonly implemented passive and active detection methods are analysed in [173], [174] and statistical analysis has been performed in [175].

5.1.2.2. Passive methods

Passive methods as the name implies, are non-invasive and rely on observing the change of various properties of the inverter current and/or the voltage at the PCC. The most basic form of passive detection methods are, over/under voltage protection (OVP/UVP) and over/under frequency protection (OFP/UFP) methods [171], [176]. These basic types of detection methods have a large NDZ and therefore are not sufficient in most applications of DG systems.

Other types of passive detection methods include voltage phase jump [176] and harmonic voltage or current detection methods [177]. The phase jump method monitors the voltage at the PCC for any changes in phase that is characteristic of islanding. The passive method proposed in [178] monitors the oscillations in rate of change of frequency at the PCC.

The harmonics based methods consist of either detecting change in the total harmonic distortion [177], detecting changes in the individual low order

harmonics [179], or monitoring the changes in the switching harmonics due to the PWM operation of the inverter [180].

5.1.2.3. Active Methods

Active methods of detection are based on introducing a disturbance to the output of the inverter and monitoring the response of the voltage/current. Active methods can be summarised as follows.

- Slide-mode frequency shift (SMS) [181].
    - Involves controlling the phase between the voltage and current to be a function of frequency. The inverter phase response is designed to be unstable at the line frequency, thereby when islanding occurs; a slight change in frequency causes instability and thereby causing the inverter to shut down.

- Active frequency drift and Sandia frequency shift (SFS) [181], [182], [183], [184], [185].
    - In these methods, the frequency of the inverter current is continuously changed by a small amount. During normal operation, this does not cause the frequency of the voltage to change due to the presence of the utility voltage. However, under islanding condition, the frequency of the voltage also drifts which is detectable.
    - The Sandia method goes further by introducing a positive feedback to the frequency variation such that any deviation in the frequency of the grid voltage gets amplified and therefore during islanding, it causes instability of the frequency due to the lack of a stiff reference.

The advantage of frequency shift methods is that the NDZ is reduced. However the downside is the distortion of the current.

- Sandia voltage shift (SVS) [184].
    - Similar to the SFS method, the SVS also employs positive feedback to cause instability during islanding condition. In the SVS method, the inverter current is varied proportional to any changes in the magnitude of the grid voltage. Under normal operation, this process does not cause any instability, however when there is a grid fault and if the voltage increases/decreases, the resulting increase/decrease of current further magnifies/attenuates the voltage and this process leads to a positive feedback induced loss of stability.

- Impedance measurement by output power shift [179].
    - Since islanding causes the impedance at the PCC to increase, the active impedance measurement relies on continually varying the amplitude of the inverter current so as to detect the corresponding change in voltage upon islanding. The strengths of this method include the small NDZ and the disadvantages are related to multi inverter scenarios where non-detection and grid instability could occur [186]. This is because when a number of DG inverters are connected to the grid at the PCC, the combination of the output power variations results in an overall stable output voltage and therefore non-detection under islanding unless the disturbances are synchronised. In synchronised operation, grid instability and false tripping may occur when the grid impedance is high [186].

- Impedance measurement by harmonic injection [187-191].
    - As the name implies, the basis of impedance measurement in this method is to inject harmonics to the inverter current. Since the grid impedance is small during normal operation, the voltage induced due to the injected harmonics is also small. Upon islanding, the induced harmonic voltage increases, allowing detection. This method may cause false detection if multiple inverters with the same harmonic frequency injection are operating in the grid as the sum of the injected currents may cause the resulting voltage harmonic levels to reach the detection threshold even under non-islanded conditions [186].

Other types of active methods include DQ-frame based feedback methods [192]; methods based on the perturbation of the reactive power [193, 194] and second order generalised integrator (SOGI) PLL based methods [195] that introduce a small disturbance in the phase of the inverter current.

Although active methods significantly decrease the NDZ, they share the disadvantage of degrading the power quality to some degree and some of the active methods have the disadvantage of causing instability to the grid in multi-inverter scenarios [196]. Furthermore, with the common prevalence of photovoltaic (PV) inverter systems, there may be situations where the islanding detection mechanisms of multiple inverter systems connected to the same utility fail to detect islanding due to the interaction between the systems [18].

5.2. Voltage switching harmonic signature based islanding detection

5.2.1. Proposed method of detection

To overcome the drawbacks of islanding detection schemes reported in literature, a new detection technique has been developed. The proposed islanding detection method consists of monitoring the frequency spectrum of the voltage at the PCC (V_{PCC}). When islanding occurs, the shunt impedance at the PCC for high frequencies increases and this results in the increase of PWM voltage harmonics. An FFT is performed on the V_{PCC} signal for each cycle of the fundamental frequency after which the switching harmonic sidebands are compared with the noise floor to obtain a relative magnitude. A look up table (LUT) is utilised to compare the obtained magnitude to the trip value for the given modulation index. The decision logic then determines whether islanding has taken place and if so, the inverter is shut down. Two sideband harmonic components are used as the signature of the inverter's harmonics for the detection of islanding which provides a degree of immunity from false tripping due to external noise sources.

The proposed method varies from the method reported in [180] due to the consideration of multiple harmonic components, thereby detecting the unique signature of the inverter under consideration for the purposes of noise immunity. Further extension of the algorithm where the PWM frequency is varied upon encountering multi-inverter interference is also investigated.

Furthermore, the limitations common to both the proposed method and the method reported in [180] due to large capacitive loads as well as the positive effect of series impedance of the capacitive load on detection are investigated.

5.2.2. Modelling of inverter LCL filter and utility grid

In order to analyse the behaviour of the grid-connected inverter upon islanding, it is necessary to establish a model of the system at the high frequency level. The schematic given in Fig. 5-2 represents the inverter's LCL filter, the RLC load and the grid. The RL represents a combination of the most common resistive and inductive loads while C represents capacitance for any power factor correction or harmonic filtering. The grid can be considered a short circuit at the high frequencies of interest due to the large capacitor banks that are common for power factor correction. However, the series impedance (Z_{grid}) of the power lines must be considered in the model. The circuit breaker (SW_1) represents the breaking point when islanding occurs.

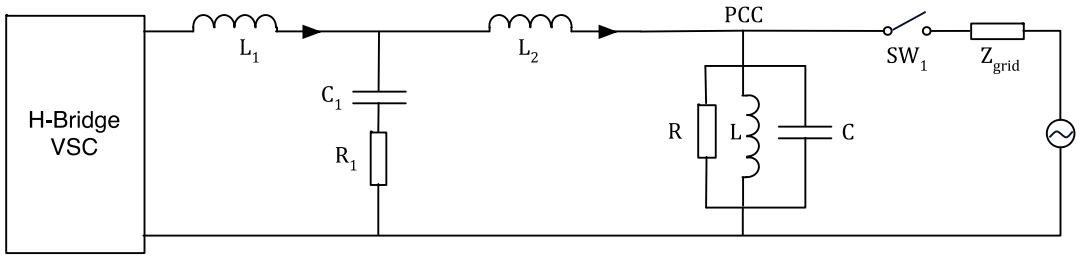


Fig. 5-2 Inverter, RLC load and grid

The high frequency voltage harmonics are generated in the inverter due to the voltage source converter's (VSC) PWM operation and the individual harmonic components can be quantified by the equation given in (5-1) [82]. For the H-bridge inverter under investigation, unipolar PWM modulation scheme is utilised and therefore, the harmonics appear centred around integer multiples of the switching frequency (10 kHz) starting from double the switching frequency onwards as illustrated in Fig. 5-3, where the harmonic orders are normalised to the 50 Hz fundamental.

$$V_{inv}(t) = V_{dc}Mcos(\omega_o t) \qquad \textbf{(5-1)}$$
$$+\frac{4V_{dc}}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{2m}J_{2n-1}(m\pi M)$$
$$*\, cos([m+n-1]\pi)cos(2m\omega_{sw}t + [2n-1]\omega_o t)$$

As can be seen, the two side bands at 20 kHz ±50 Hz have the highest magnitude.

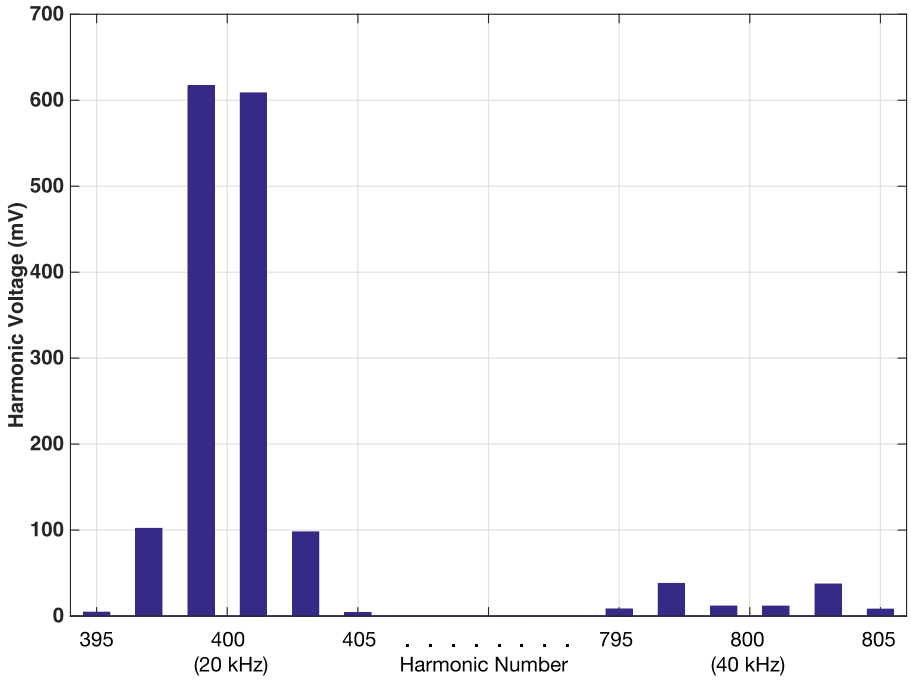


Fig. 5-3 Harmonic content of unipolar PWM inverter switching at 10 kHz

According to IEEE standard 519-1992, current harmonics over the order 35 generated by the inverter must be lower than 0.3% of the maximum load current for short circuit current ratios lower than 20. Therefore the inverter LCL filter can be designed to meet these regulations. For the purposes of analysis and experiment, the following inverter specifications given in Table 5-1 are used.

Table 5-1 Inverter specifications

Parameter	Symbol	Value
Inverter output power	P	2.2 kW
Inverter side inductor	L_1	5 mH
Grid side inductor	L_2	145 µH
Filter capacitor	C_1	6.8 µF
Damping resistor	R_1	1.2 Ω

For the ease of analysis, the inverter consisting of the VSC and LCL filter can be simplified by a Thévenin equivalent circuit as shown in Fig. 5-4 where $e_{th}(h)$ and $Z_{th}(h)$ are given by (5-2) and (5-3) respectively. The impedance seen by the inverter before and after islanding for the parallel RLC load are defined by equations (5-4) and (5-5). Therefore the voltage harmonics present at the PCC before and after islanding can be defined as given in (5-6) and (5-7).

$$e_{th}(h) = \frac{1 + j\omega_h R_1 C_1}{1 + j\omega_h R_1 C_1 - \omega_h^2 L_1 C_1} * |V_{inv}(h)| \tag{5-2}$$

$$Z_{th}(h) = \frac{j\omega_h\{L_1(1 + j\omega_h R_1 C_1) + L_2(1 + j\omega_h R_1 C_1 - \omega_h^2 L_1 C_1)\}}{1 + j\omega_h R_1 C_1 - \omega_h^2 L_1 C_1} \tag{5-3}$$

$$Z_{pre-islanding}(h) = R \parallel L \parallel C \parallel Z_{grid} \tag{5-4}$$

$$Z_{post-islanding}(h) = R \parallel L \parallel C \tag{5-5}$$

$$|V_{PCC-pre-islanding}(h)| = \left|\frac{e_{th}(h)}{Z_{th}(h) + Z_{pre-islanding}(h)}\right| |Z_{pre-islanding}(h)| \tag{5-6}$$

$$|V_{PCC-post-islanding}(h)| = \left|\frac{e_{th}(h)}{Z_{th}(h) + Z_{post-islanding}(h)}\right| |Z_{post-islanding}(h)| \tag{5-7}$$

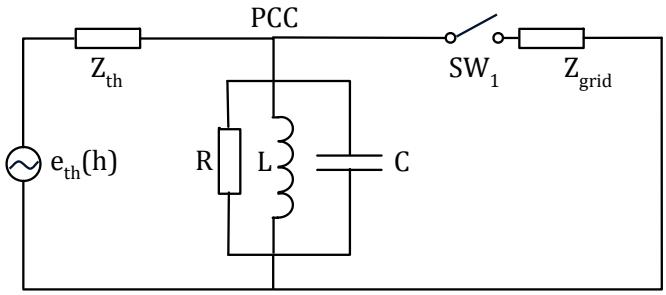


Fig. 5-4 Thévenin equivalent circuit of inverter with RLC load

5.2.3. Islanding detection zone for varying load impedances

It is clear that during islanding, the impedance at the PCC for switching frequencies increases due to the absence of the low impedance shunt component of the grid. It is this increase that also causes an increase in the voltage harmonics that appear at the PCC, which is the basis of the detection method. However, as the capacitance of the RLC load increases, the post-islanding impedance for the switching frequencies decreases. Therefore the difference between the highest level of non-islanded state voltage ripple and islanded state voltage ripple reduce to levels that are not detectable for higher values of load capacitance.

IEEE standard 929 states that the islanding detection method must be able to detect islanding for an RLC load that is resonant at the grid frequency and having a quality factor under 2.5. In order to quantify the detectable zone as a function of load capacitance C, the following Fig. 5-5 is presented where ideal grid impedance of zero for high frequencies is assumed for a 2.2 kW power level. The figure shows the variation of harmonic voltage difference ΔV(h) between before and after islanding for an RLC load resonant at 50 Hz.

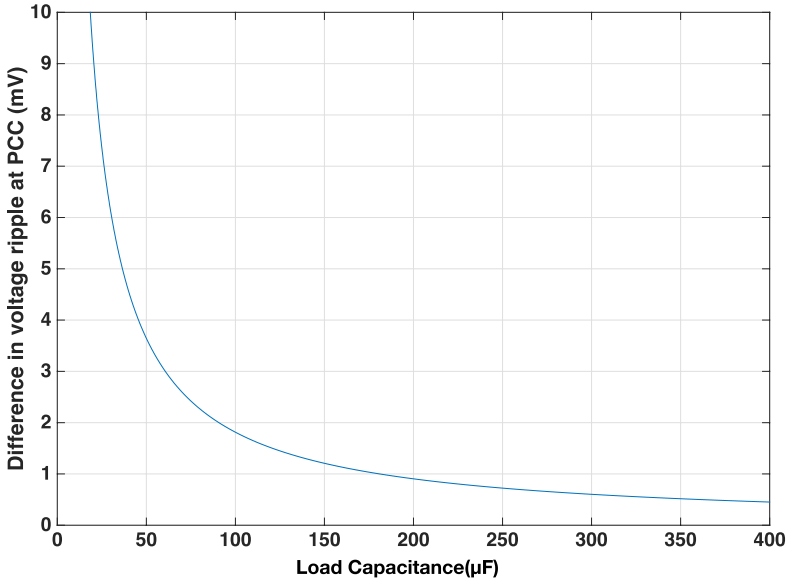


Fig. 5-5 Difference in voltage ripple (20.05 kHz) for an RLC resonant load with varying load capacitance

Although the ideal grid condition of 0 Ω for high frequencies was used for analysing the detection zone, in practice the series grid inductance at the switching frequency will be a finite value, which sets the baseline value of the voltage harmonics above which the trip threshold lies. Furthermore, in reality the parallel RLC load will have a series impedance component which represents cable effects at the switching frequency as well as ESR of the load capacitance and load inductance as shown in Fig. 5-6.

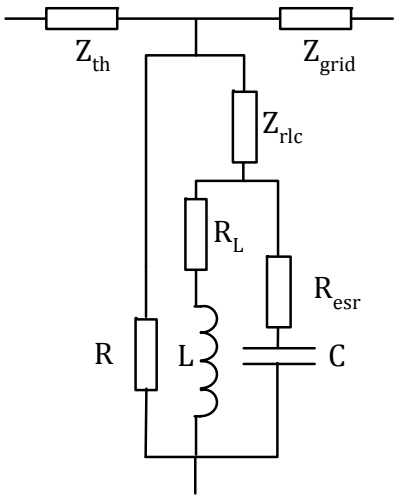


Fig. 5-6 RLC load with parasitic impedance elements

Fig. 5-7 shows the variation in post-islanded switching voltage ripple (20.05 kHz) present at the PCC for the conditions given in Table 5-2 for an RLC load resonant at 50 Hz.

Table 5-2 Conditions for the ripple voltage analysis

Parameter	Symbol	Value
Real power of inverter	P	2.2 kW
Load resistance	R	26 Ω
Load Capacitance	C	0 – 350 µF (sweep)
Load Inductance	L	To match C for 50 Hz resonance
Impedance to load (20 kHz)	$\|Z_{bus}\|$	0.5 Ω
ESR of inductor	R_L	10 mΩ
ESR of capacitor	R_{esr}	10 mΩ
LC branch series impedance (20 kHz)	$\|Z_{rlc}(20\ kHz)\|$	0 – 5 Ω (sweep)
Grid impedance (20 kHz)	$\|Z_{grid}(20\ kHz)\|$	2.5 Ω
Modulation index	M	0.62

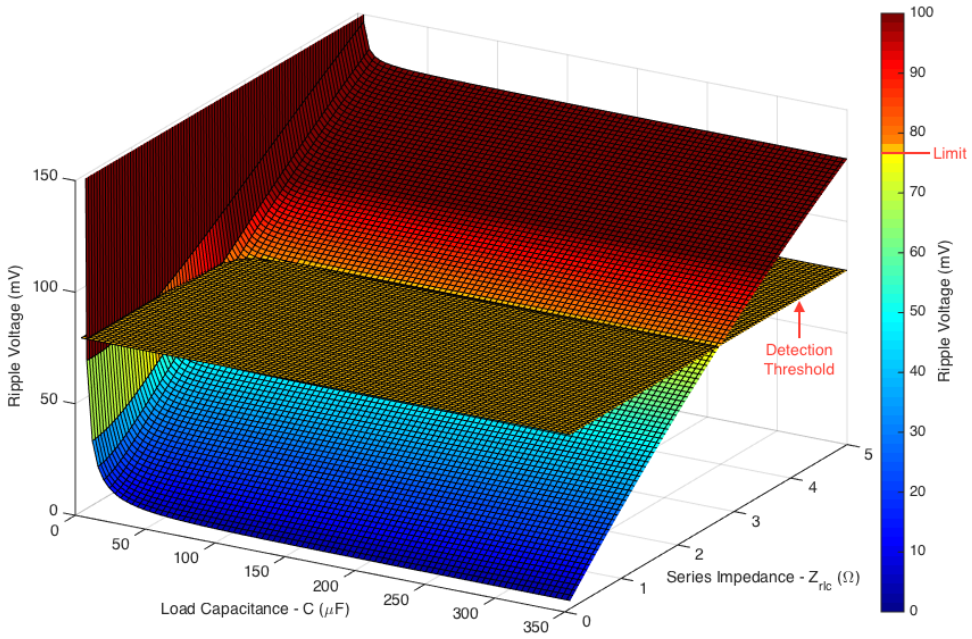


Fig. 5-7 Voltage ripple after islanding as a function of load capacitance (C) and series impedance at 20 kHz ($|Z_{rlc}|$)

In Fig. 5-7, islanding is detectable if the magnitude of the post islanding voltage ripple lies above the detection threshold plane. The detection threshold plane is defined as a value that is 5% larger than the worst-case value of voltage ripple present under normal operation (when no RLC load is connected to the inverter and the inverter is not islanded). It is found that islanding is detectable for all values of series impedance, Z_{rlc}, for load capacitances that are under 3.65 μF. For series impedances higher than 2.75 Ω, islanding is detectable for all values of load capacitance. The effect of spurious noise that can be present in the sensed voltage is minimised by comparing both harmonic components (19.95 kHz and 20.05 kHz) to threshold values.

5.2.4. Islanding detection algorithm

The islanding detection algorithm is highlighted in the following diagram Fig. 5-8. Voltage at the PCC is first attenuated by 34 dB after which it is band-pass filtered with a centre frequency of 20 kHz and a bandwidth of 8 kHz. This stage removes the fundamental (50 Hz) signal thereby maximising the ADC's dynamic range as well as removing out of band signals that are not of interest. The ADC digitises the filtered signal at a sampling rate of 409.6 kSPS after which the signal is processed in the FPGA (NI CompactRIO FPGA – code presented in Appendix G). The data processing is overseen by the control logic, which first takes 8192 data samples (20 ms of data – 1 cycle of the fundamental) from the ADC to the FIFO memory and initiates the FFT transform. The higher sampling frequency and hence the 8k size for the FFT is used to increase the FFT process gain thereby increasing the signal to noise ratio. After the data is processed through the FFT logic, data points except the harmonic sideband components are averaged to obtain the noise floor. Afterwards, the level of the noise floor is checked for any interference to avoid false tripping. The final part of the algorithm is the compare logic, which compares the 2 harmonic components (19.95 kHz and 20.05 kHz) to the detection threshold obtained from the LUT for the current value of modulation index (as the inverter's harmonic voltage

magnitude is a function of the modulation index, the values in the LUT are predetermined by considering the worst case voltage ripple for a range of modulation index values). If both components are above the trip limit, the logic asserts the islanding detected signal. This process repeats itself every ~20 ms.

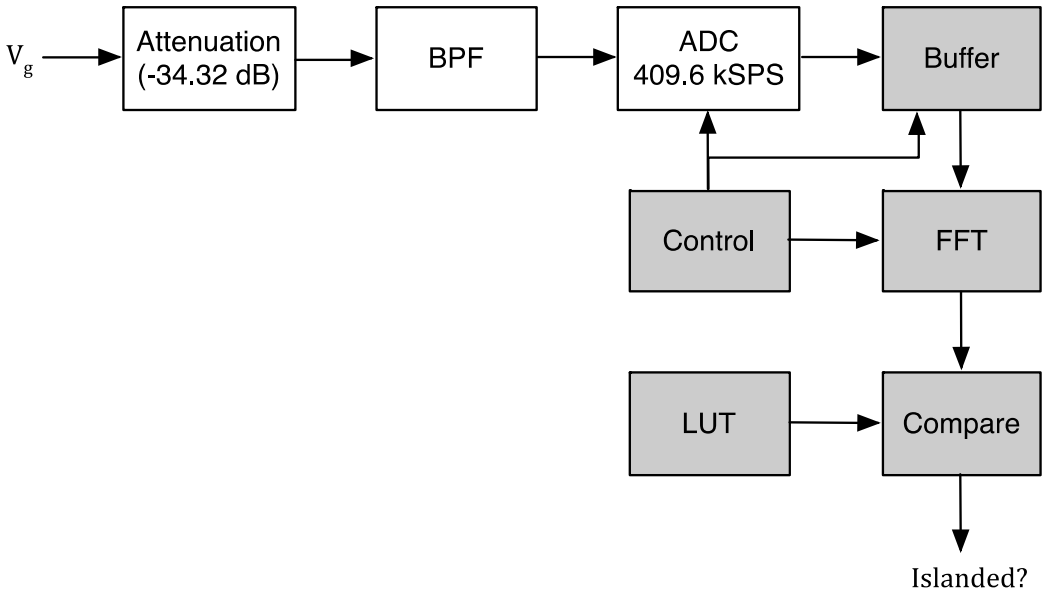


Fig. 5-8 Islanding detection algorithm

5.2.5. Noise immunity from other switching converters

It is possible that other power converter systems operating nearby to the inverter could cause a false trip situation if the external systems happen to operate at the same switching frequency and thereby causing the magnitude of harmonics to exceed the threshold value. If noise immunity from other switching converters is a design criterion, the detection logic can be configured to dynamically change the inverter PWM frequency for the subsequent cycle of fundamental frequency upon detecting the first trip condition. The 2nd PWM modulation frequency to hop to is determined by scanning the adjacent spectrum (20 kHz ±4 kHz) and selecting a frequency that has a low amount of noise present which is an integer multiple of the grid frequency. If the spectrum

of the subsequent cycle also matches the sideband characteristics for islanding condition, it can be determined that actual islanding has taken place and the inverter shut down.

It must be noted that the amount of inverters that can be supported by the islanding detection algorithm is limited to the spectral bandwidth (20 kHz ± 4 kHz in this instance) and therefore optimum utilization may be obtained by interleaving the spectrum. For instance, if ±3 sideband harmonics around 20 kHz are considered (19.75 to 20.25 kHz), it is observed that the harmonics are separated by 100 Hz and hence occupies a bandwidth of 500 Hz. Therefore, it is possible to interleave another inverter between the harmonic spurs that are separated by 100 Hz, yielding a total bandwidth of 600 Hz for 2 inverters. Therefore, the 16 kHz - 24 kHz band can support 13 pairs of inverters, or 26 in total. As an example, in a residential application, each phase in a neighbourhood may contain 26 separate inverters. Each inverter must therefore scan the available band and self allocate a suitable switching frequency before initiating power switching.

5.2.6. Comparison of detection time

The proposed algorithm is able to detect islanding after ~20 ms (20 ms + the time for FFT computation which is typically <1 ms for the NI CompactRIO system) of the event. The extended algorithm which allows for multi-inverter immunity requires ~40 ms for detection. The response time of the proposed algorithm is compared with other islanding detection methods in Table 5-3.

Table 5-3 Comparison of islanding detection time

Detection Method	Active/Passive	Detection Time (ms)
Proposed method	Passive	~20 (~40 multi-inv.)
Over/under frequency (OFP/UFP) [197]	Passive	63
Over/under voltage (OVP/UVP) [197]	Passive	8
Rate of change of frequency (ROCOF) [178]	Passive	400
Wavelet-based detection [198]	Passive	20
Sandia frequency shift (SFS) [199]	Active	90
Slide mode frequency shift (SMS) [200]	Active	100
Active reactive power drift (ARPD) [201]	Active	200

It can be observed that the fastest method is the OVP/UVP method although the non-detection zone of the over/under voltage method is large (not able to detect islanding when active power is matched). It can be seen that the proposed method is able to detect islanding in a similar amount of time as the wavelet based passive method.

According to the IEEE1547 standard, a distributed generation system must cease to energise the electrical power system (EPS) within 2 seconds of islanding. Therefore, the proposed algorithm is able to meet the detection time requirement.

5.3. Simulation of islanding algorithm

A number of test cases are simulated in MATLAB using the SimPowerSystems toolbox. The low frequency transformer based inverter specification from Chapter 2 is used as the inverter ('Inverter 1' Simulink diagram presented in Appendix E) along with a parallel-connected RLC load and grid as shown in Fig. 5-9. The 'Inverter 1' controller consists of a SRFPI current controller (Simulink diagram presented in Appendix B) for controlling the grid

current which has a bandwidth of 900 Hz, as well as a SOGI PLL (Simulink diagram presented in Appendix B) for grid synchronisation. The islanding algorithm is coded into a MATLAB function block and is connected to the system (code presented in Appendix F). The breaker is opened at a predetermined time (0.6 s) to simulate islanding. The simulation cases and associated conditions are highlighted in the following Table 5-4.

Table 5-4 Simulation test conditions

Simulation	R (Ω)	L (mH)	C (μF)	R_L (mΩ)	R_{esr} (mΩ)	$\|Z_{bus}\|$ (20 kHz) (Ω)	$\|Z_{rlc}\|$ (20 kHz) (Ω)	$\|Z_{grid}\|$ (20 kHz) (Ω)
Resistive Load	26.18	-	-	-	-	0.5	-	2.5
RLC Load	26.18	33.77	300	10	10	0.5	2.75	2.5
Multiple Inverter Immunity	-	-	-	-	-	0.5	-	2.5
Multi Inverter Islanding	13.09	-	-	-	-	0.5	-	2.5

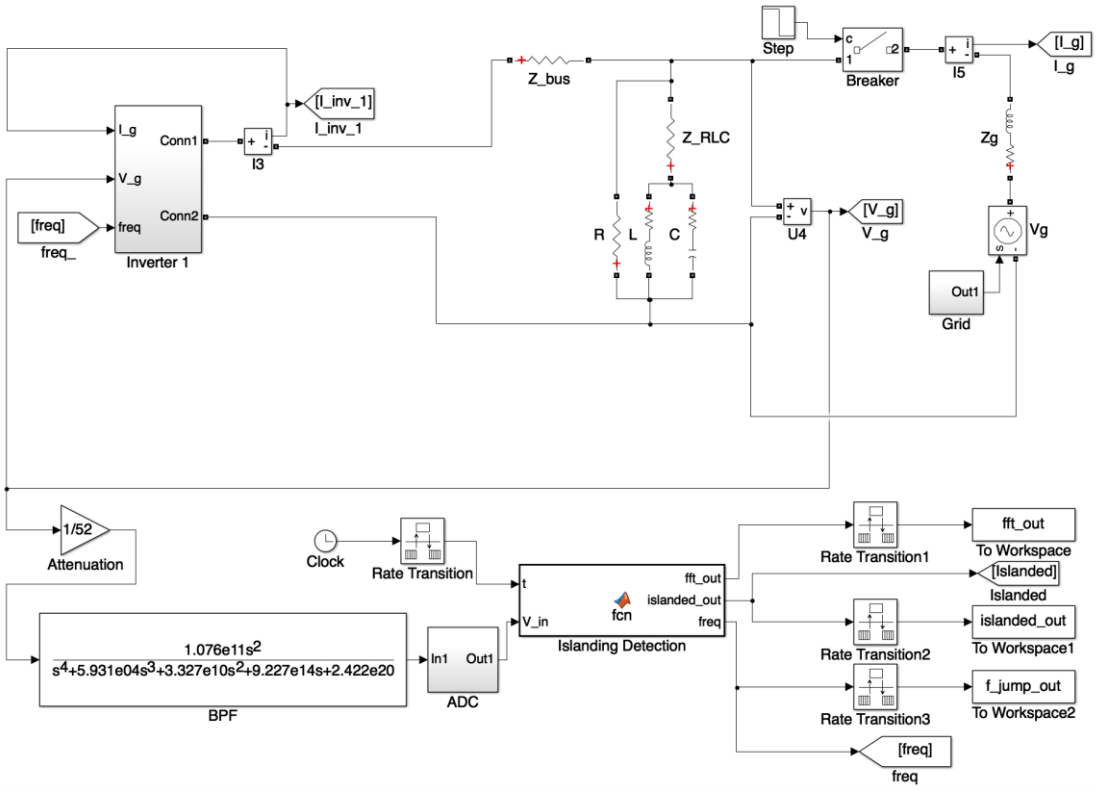


Fig. 5-9 SimPowerSystems block diagram

5.3.1. Simulation case 1 – resistive load

The first case for simulation is a purely resistive load. After islanding, the ripple voltage increases to a significant level due to the absence of any shunt capacitive elements and therefore this case is easily detected as shown in Fig. 5-10 and Fig. 5-11. The pre-islanding ripple is 72 mV, and the post-islanding ripple is 442 mV. Since the load's real power is matched with the inverter's real power output (2.2 kW), it can be seen that the V_{PCC} frequency continues to be within ±0.5% of 50 Hz as well as the magnitude of voltage at the PCC being unaffected by the islanding. Therefore this condition falls in the NDZ of the OVP/UVP or OFP/UFP methods of passive islanding detection.

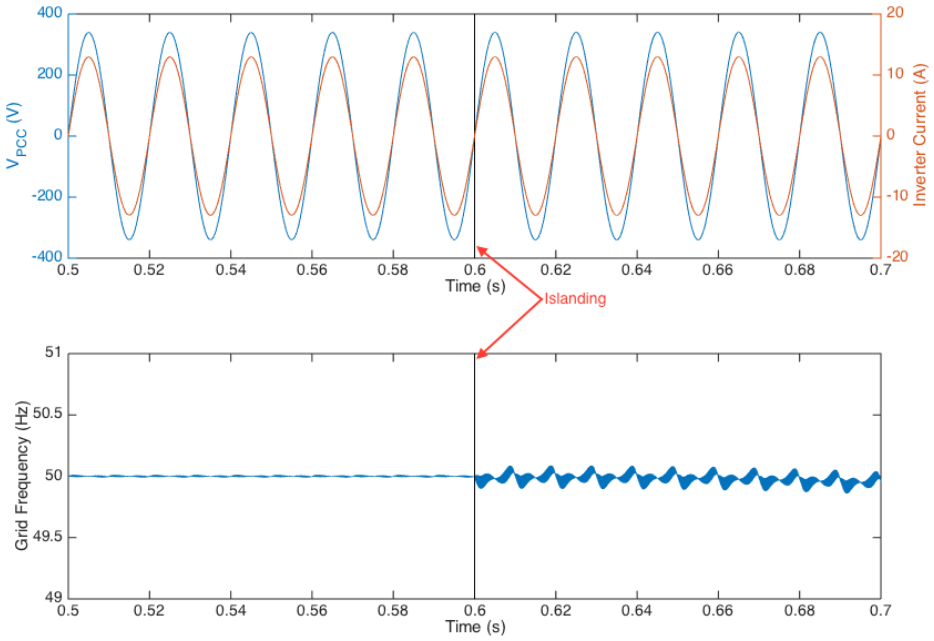


Fig. 5-10 Islanding simulation case 1 – voltage at PCC, inverter current and V_{PCC} frequency

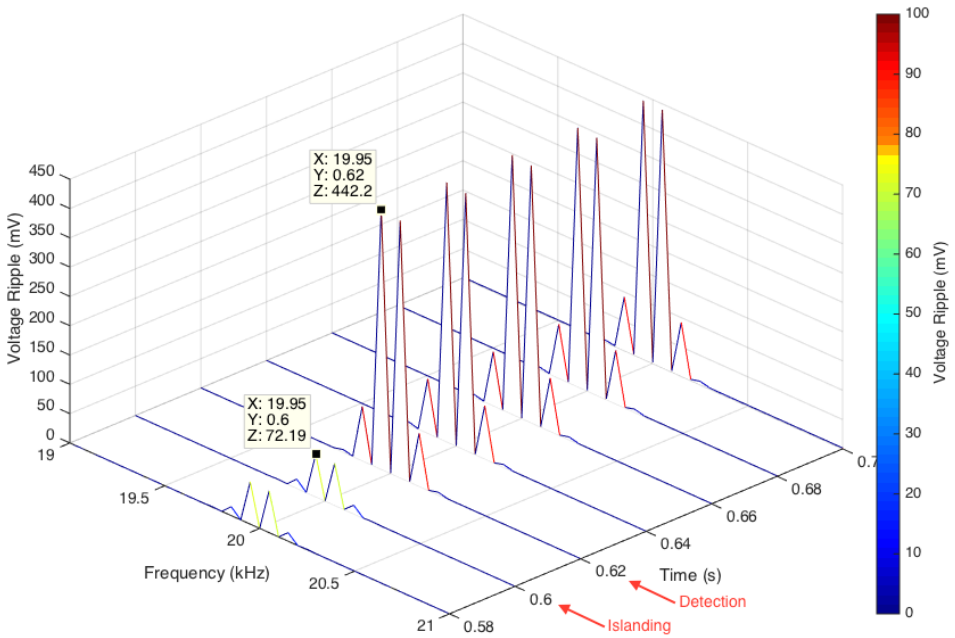


Fig. 5-11 Islanding simulation case 1 – time domain variation of the V_{PCC} spectral content

5.3.2. Simulation case 2 – RLC resonant load

The 2nd simulation case is with an RLC load that is resonant at 50 Hz and therefore lies in the NDZ of the OVP/UVP and OFP/UFP methods. Fig. 5-12 and Fig. 5-13 show the V_{PCC}, inverter current and V_{PCC} spectral content variation over time. It can be observed that the islanding is successfully detected after 20 ms (1 electrical cycle) after islanding.

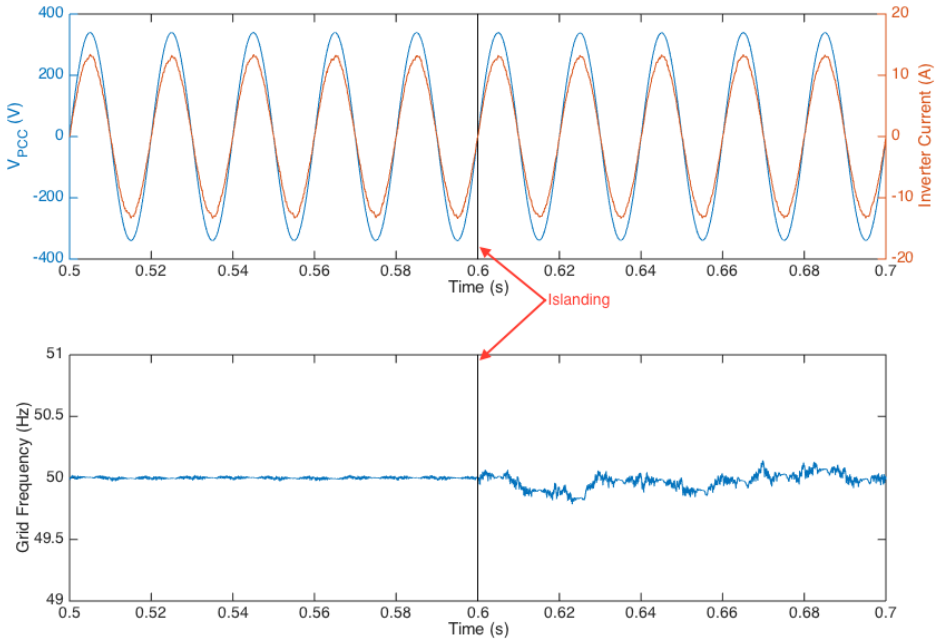


Fig. 5-12 Islanding simulation case 2 – voltage at PCC, inverter current and V_{PCC} frequency

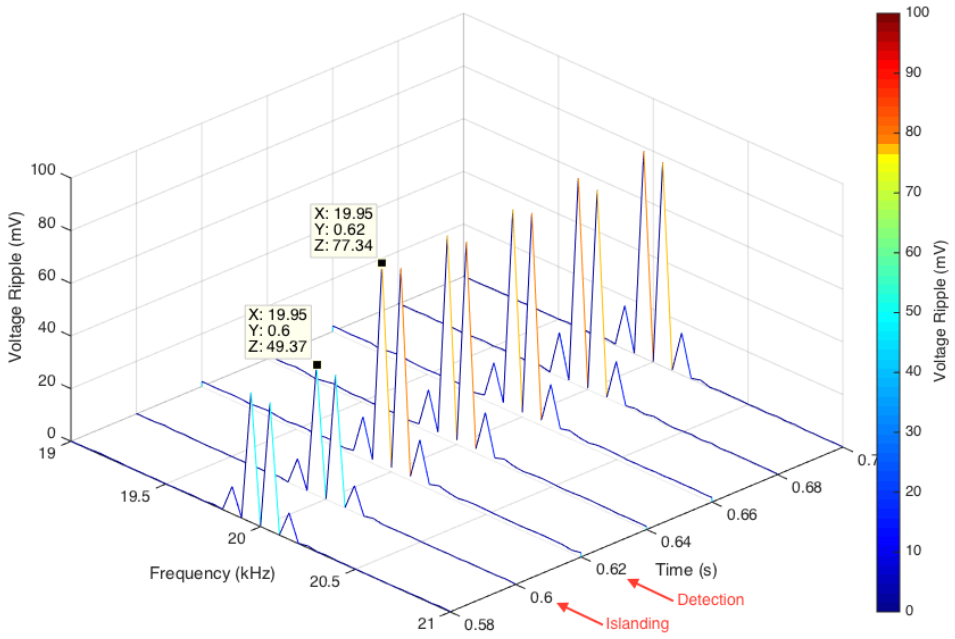


Fig. 5-13 Islanding simulation case 2 – time domain variation of the V_{PCC} spectral content

After islanding, the magnitude and the frequency of V_{PCC}'s fundamental component continue to be unaffected. But the voltage ripple of the 19.95kHz component (and 20.05 kHz) increases to 77 mV from 49 mV after islanding. Therefore islanding is successfully detected, as the detection threshold is 76 mV.

5.3.3. Simulation case 3 – connection of a second inverter with same PWM frequency

In the situation where immunity from false tripping due to other converters operating with the same PWM frequency is required, the adaptive PWM hopping method can be used at the cost of increasing the detection time from ~20 ms to ~40 ms (2 electrical cycles). The following Fig. 5-14 illustrates the inverter setup that was used for simulating case 3.

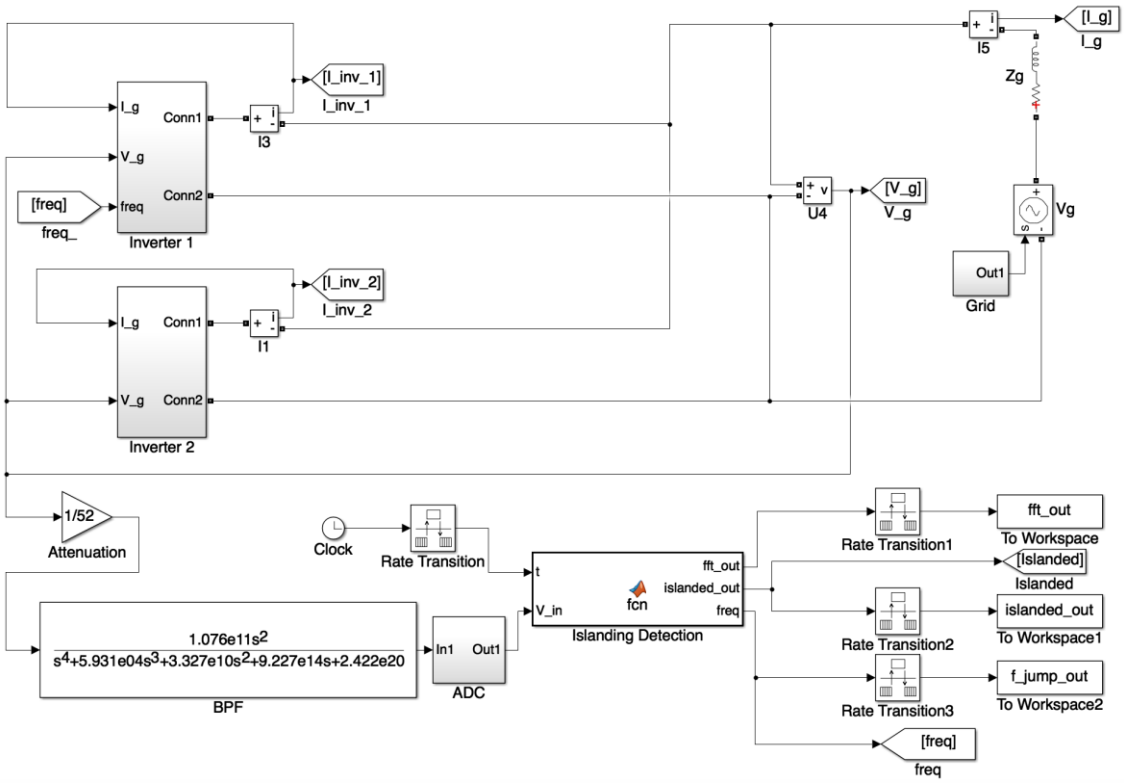


Fig. 5-14 Block diagram of simulation case 3

'Inverter 1' is the device under test in which the islanding detection algorithm is applied to whereas 'Inverter 2' is the external system that causes interference. Initially 'Inverter 2' is non-operational and 'Inverter 1' feeds power to the utility grid. At t = 0.6 s, 'Inverter 2' starts operating at the same 10 kHz device switching frequency (20 kHz harmonics generated), which causes the harmonics seen at the PCC to increase as shown in Fig. 5-15.

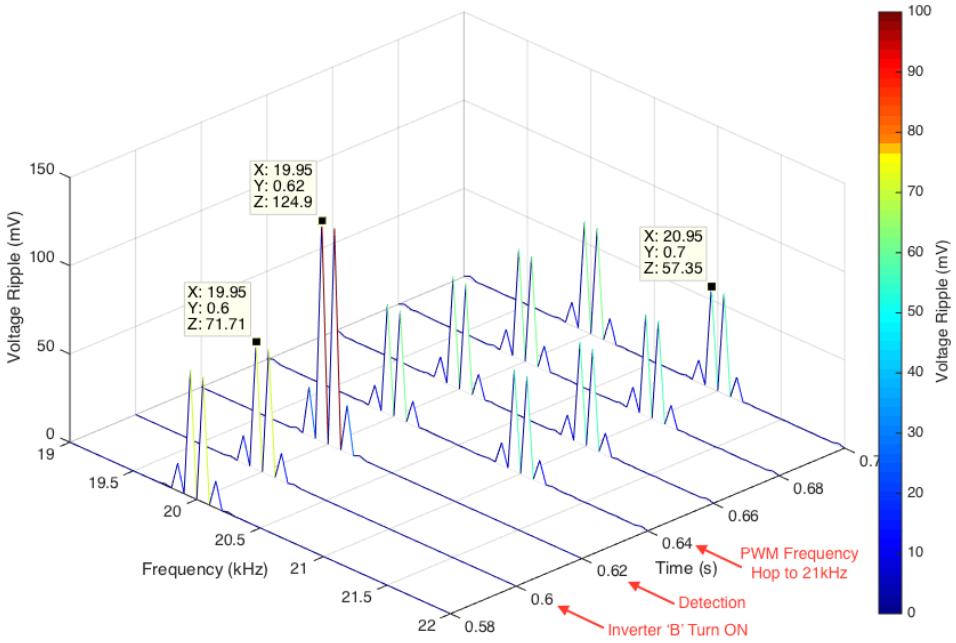


Fig. 5-15 - Islanding simulation case 3 – time domain variation of the V_{PCC} spectral content

At t = 0.62 s, upon detection the harmonic voltage limits have been exceeded, the islanding prevention algorithm of 'Inverter 1' then scans the adjacent spectrum for a suitable frequency with low interference and changes its PWM frequency to 21 kHz. After the subsequent electrical cycle (at t = 0.64 s), the FFT of V_{PCC} reveals that the harmonic spectrum for 'Inverter 1' is below the limits that would be identified as being islanded. Therefore 'Inverter 1' continues to operate at 21 kHz. Frequency hopping upon exceeding harmonic limits is done until such time that the limits are exceeded in 2 successive cycles in which case it is determined that actual islanding has taken place.

Fig. 5-16 illustrates the magnitude and frequency of the voltage at PCC and 'Inverter 1' current.

Therefore, the simulation shows that the proposed algorithm for islanding detection has immunity from false tripping due to external power converters operating at the same PWM frequency.

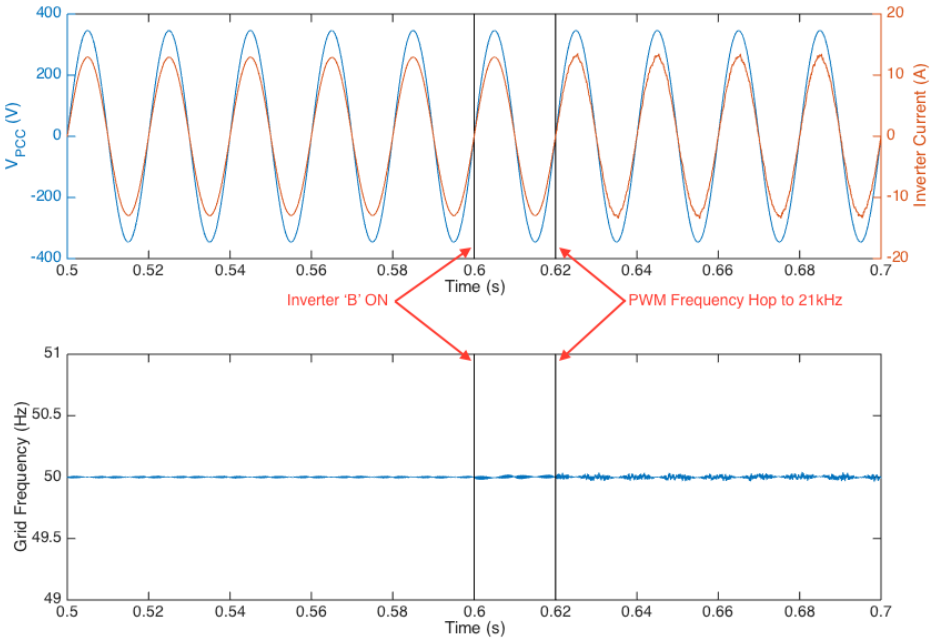


Fig. 5-16 Islanding simulation case 3 – voltage at PCC, 'Inverter 1' current and V_{PCC} frequency

5.3.4. Simulation case 4 – detection of islanding under multiple inverter operation

Following the simulation of multi inverter immunity in the previous section, the detection of islanding with a resistive load when multiple inverters are present is simulated in simulation case 4. Therefore a resistive load (13.09 Ω) is connected to the PCC as well as a breaker between the grid and the PCC which opens when islanding occurs.

'Inverter 1' is the device under test in which the islanding detection algorithm is applied to whereas 'Inverter 2' is the external system that causes interference. The operation of 'Inverter 1' and 'Inverter 2' follow the same sequence as was for case 3. Initially 'Inverter 2' is non-operational and 'Inverter 1' feeds power to the utility grid. At t = 0.6 s, 'Inverter 2' starts operating at the same 10 kHz device switching frequency (20 kHz harmonics generated), which causes the harmonics seen at the PCC to increase as shown in Fig. 5-17.

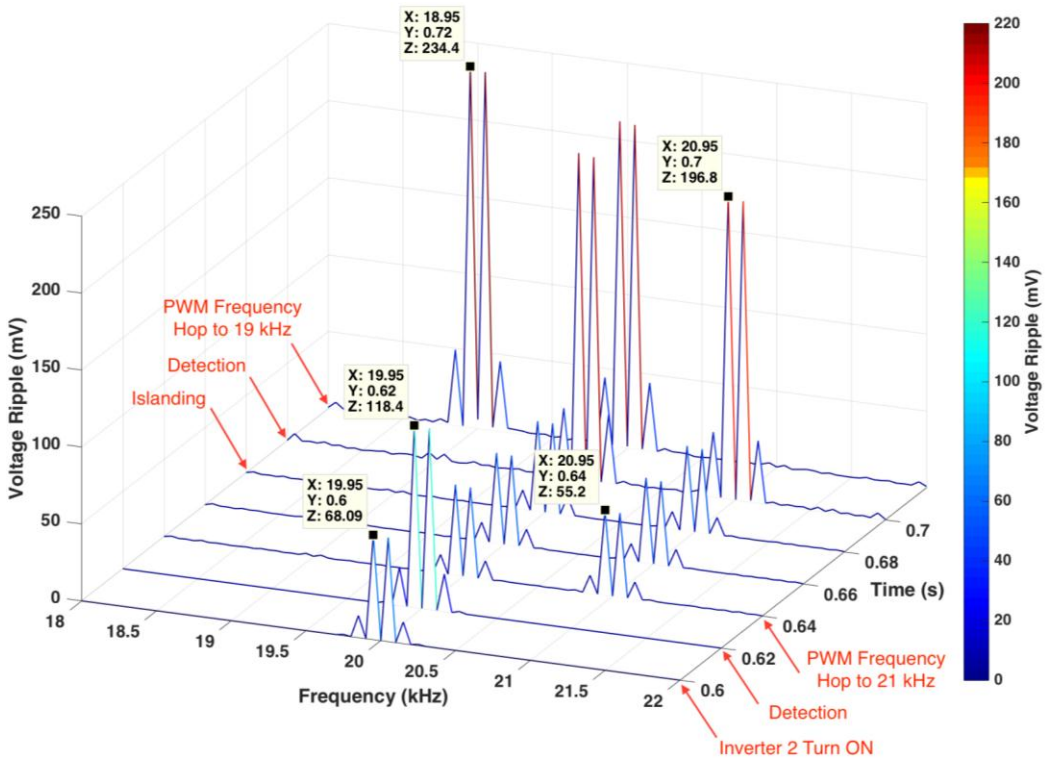


Fig. 5-17 - Islanding simulation case 4 – time domain variation of the V_{PCC} spectral content

At t = 0.62 s, upon detection the harmonic voltage limits have been exceeded, the islanding prevention algorithm of 'Inverter 1' changes its PWM frequency to 10.5 kHz (harmonics at 21 kHz). After the subsequent electrical cycle (at t = 0.64 s), the FFT of V_{PCC} reveals that the harmonic spectrum for 'Inverter 1' is below the limits that would be identified as being islanded. Therefore 'Inverter 1' continues to operate at 21 kHz. At t = 0.68 s, actual islanding occurs where the breaker opens and therefore the 2 inverters (both operating at 2.2 kW) continue to power the local resistive load. At t = 0.7, the islanding detection algorithm detects the increased voltage harmonics and therefore changes the PWM frequency to 9.5 kHz (causing voltage harmonics to appear at 19 kHz). In the following electrical cycle (t = 0.72), it can be seen in Fig. 5-17 that despite the frequency jump, the harmonics are still at the increased level (234 mV). Therefore, at t = 0.72 s, islanding is detected since the

algorithm detected increased harmonics in 2 consecutive cycles of the grid voltage.

Fig. 5-18 illustrates the magnitude and frequency of the voltage at PCC and 'Inverter 1' current. It can be seen that the grid frequency becomes unstable upon islanding and crosses 50.5 Hz after approximately 18 ms after islanding. Therefore the OFP/UFP method of islanding detection is also able to detect islanding in this case since the threshold for OFP/UFP is typically ±1% of the nominal grid frequency.

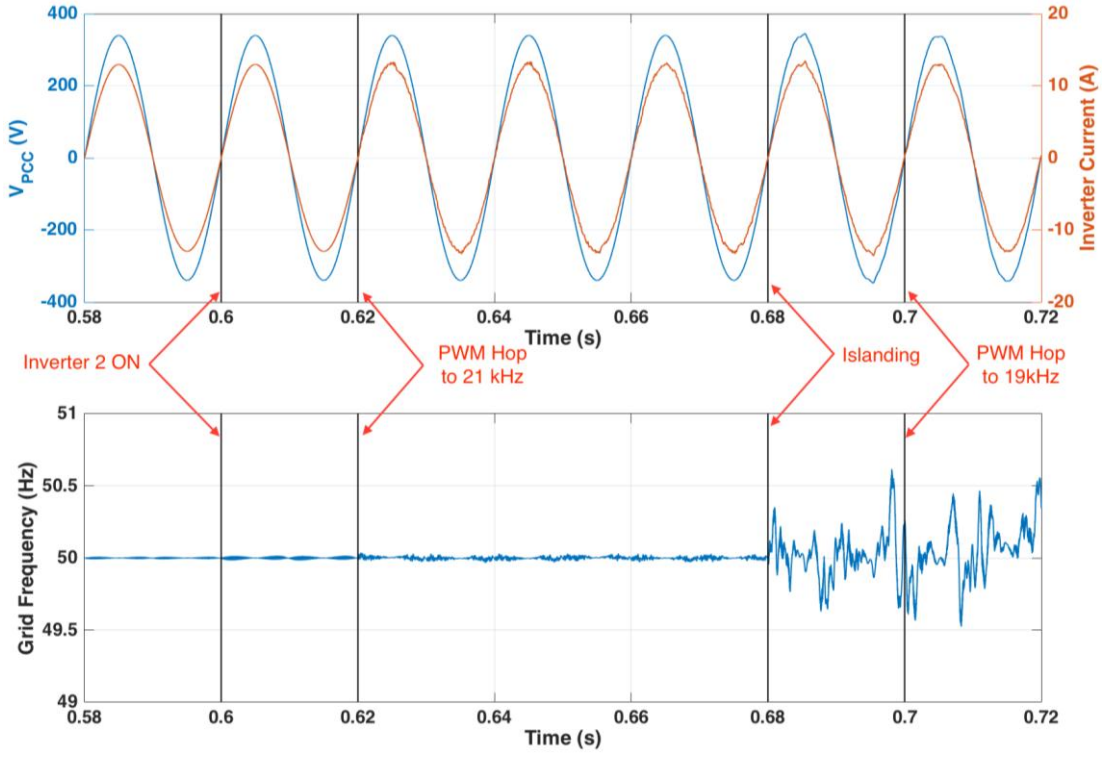


Fig. 5-18 Islanding simulation case 4 – voltage at PCC, 'Inverter 1' current and V_{PCC} frequency

Simulation case 4 shows that the algorithm has immunity from false tripping due to external power converters operating at the same PWM frequency as well as being able to detect islanding under such a scenario.

5.4. Design of islanding detection hardware

5.4.1. Voltage detection hardware design

The detection of the small signal high frequency components present at the PCC can be achieved by sampling the grid voltage through an ADC converter. However, since most commercially available voltage transducers are not able to detect signals with bandwidth exceeding 20 kHz, a resistor divider based circuit is designed where the isolation between the high voltage side and the low voltage controller is introduced after the ADC stage with the use of ADUM1400 digital isolators.

The resistor divider attenuates the grid voltage by a factor of 52 (34.32 dB) in order to reduce the peak value of the signal to under ±7 V so as to be compatible with the analogue signal conditioning circuit.

In order to maximise the dynamic range of the ADC, the fundamental grid frequency component is filtered out and the remaining high frequency signal is amplified prior to digitisation. An active band-pass filter was designed for this purpose, which also serve as the anti-aliasing filter for the ADC. Fig. 5-19 shows the frequency response of the 4^{th} order multiple feedback Chebyshev band pass filter that was designed for the filtering. Since the dominant switching harmonics appear at 20 kHz, the pass-band of the filter was chosen to be between 16 kHz-24 kHz with a gain of 34 dB and attenuation at the fundamental frequency (50 Hz) of -87 dB. This configuration allows the full dynamic range of the ADC to be utilised while not saturating the ADC at the highest value of ripple voltage (when islanding takes place with a purely resistive load). The schematic of the op-amp based filter circuit is shown in Fig. 5-20.

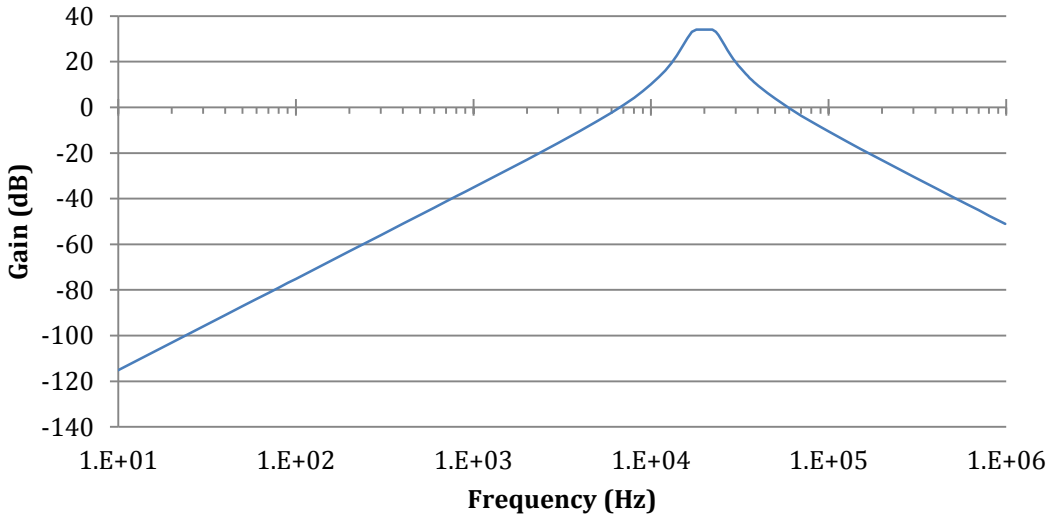


Fig. 5-19 Voltage sensing circuit band pass filter frequency response

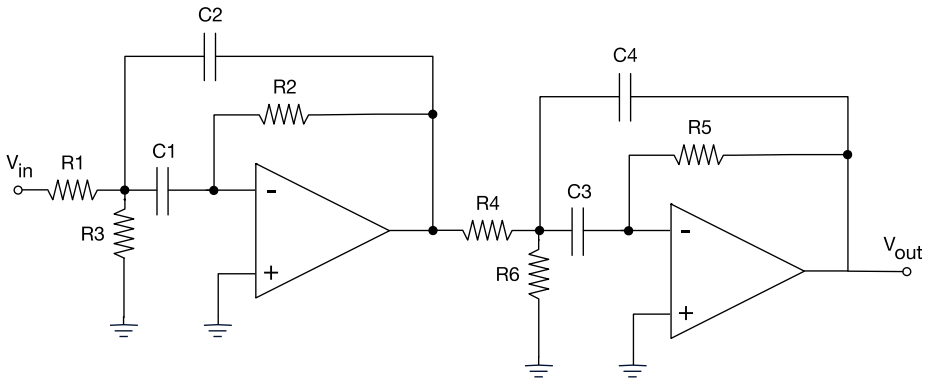


Fig. 5-20 Band pass filter schematic

A 16-bit SAR ADC converter (ADS8422) thereafter digitises the signal with a sampling frequency of 409.6 kSPS. The ADC output is carried in a data bus that is 8-bits wide and therefore the data bus is clocked at twice the sampling frequency. The ADC is interfaced through three ADUM1400 digital isolator chips, which provide the galvanic isolation required for safety. An NI cRIO-9082 controller is used for processing the data for the experimental demonstration.

5.4.2. Inverter current detection circuit hardware design

A current sensing circuit has been designed with similar band pass characteristics as the voltage sensing circuit with an independent ADC. Although the current sensing circuit is not used in the detection of islanding, it serves the purpose of measuring the grid impedance for 20 kHz frequency for analysis purposes.

The current sensing element consists of a 10 mΩ shunt resistor through which the inverter current passes. The voltage signal that appears across the resistor due to the PWM ripple current is small in magnitude and therefore the succeeding filter stage is designed with a high gain at the pass band frequency. For instance, if the ripple current magnitude is assumed to be 0.3% of the fundamental current, the rms value of voltage present across the shunt resistor due to the ripple current is only 275 μV.

The filter circuit consists of a 6^{th} order multiple feedback Chebyshev band pass filter with a pass band of 16 kHz-24 kHz, pass band gain of 60 dB and attenuation of -115.7 dB at 50 Hz.

The frequency response of the filter is shown in Fig. 5-21. Since the filter contains 6 poles, it is implemented with 3 op-amps.

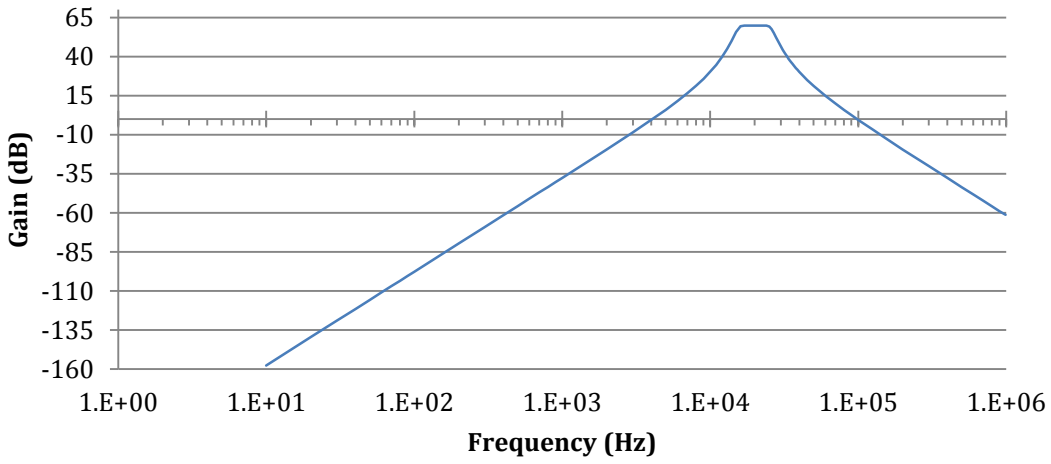


Fig. 5-21 Current sensing circuit band pass filter frequency response

5.5. Practical implementation

Fig. 5-22 shows the PCB prototype that was designed and realised for detecting the voltage and current harmonics. The power supply for the analogue and digital sections are provided through isolated DC/DC converter modules. The sensitive analogue sub-circuit has been shielded with a metal cage to prevent the pick up of EMI from the DC/DC converters as well as enclosing the entire PCB in a shielded aluminium enclosure. The circuit schematics are presented in Appendix F.

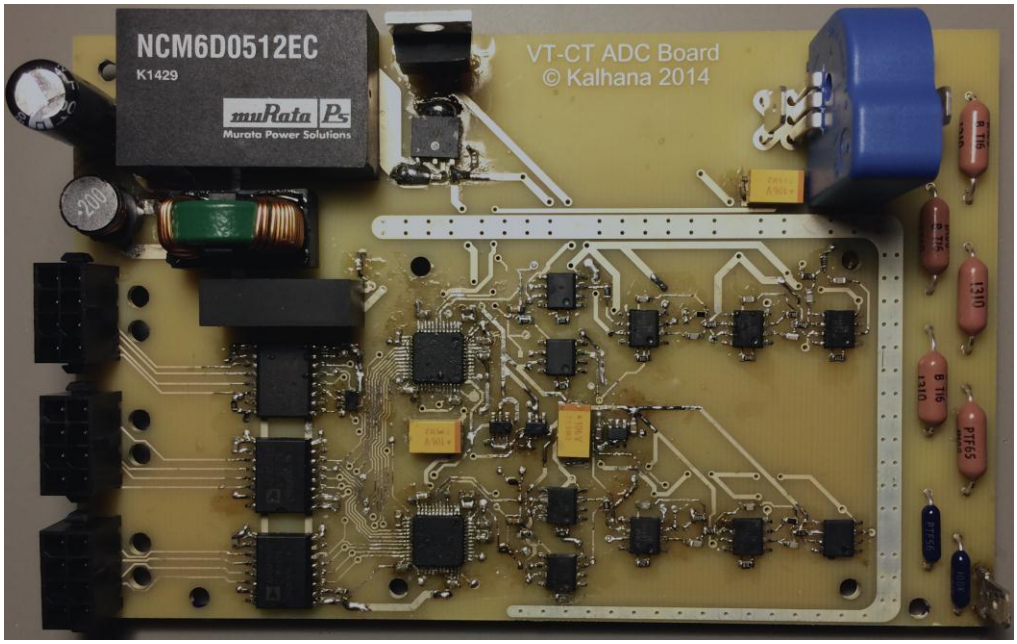


Fig. 5-22 Voltage and current detection circuit (current shunt resistor resides in a 2nd PCB)

5.5.1. Filter performance evaluation

The performance of the filter stages of the voltage and current signal path has been evaluated by sweeping through the frequency range with the use of a signal generator and by measuring the output with an oscilloscope. The

designed vs. measured characteristics for the voltage and current sensing circuits are presented in Fig. 5-23 and Fig. 5-24 respectively.

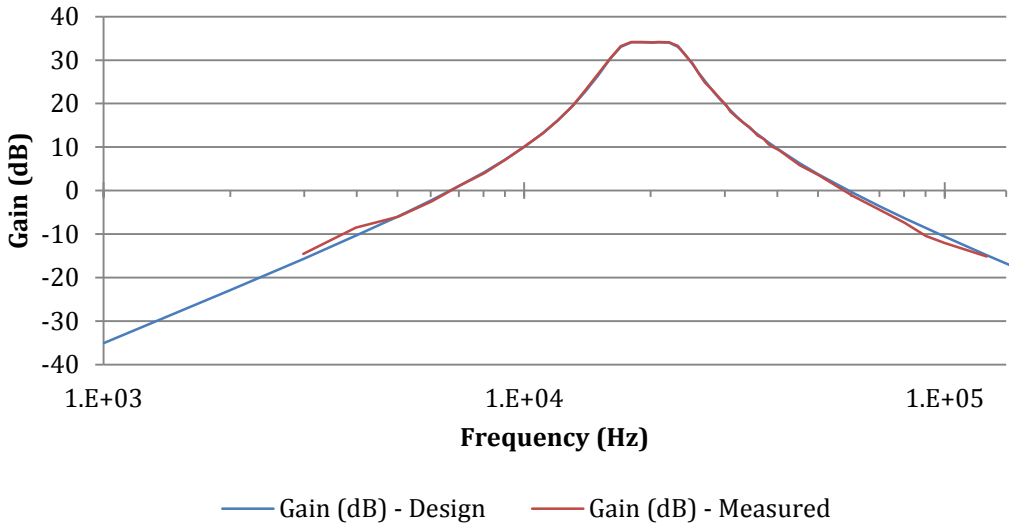


Fig. 5-23 Voltage sensor band pass filter frequency response – Designed vs. measured

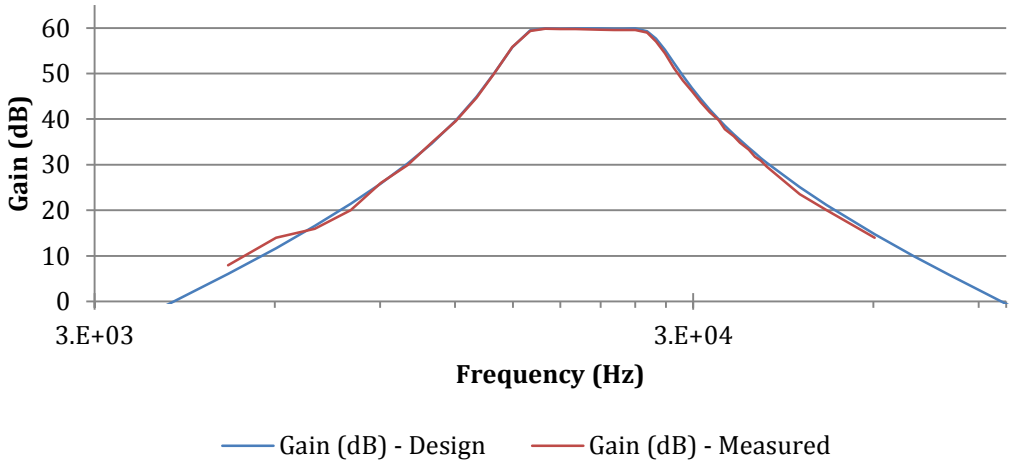


Fig. 5-24 Current sensor band pass filter frequency response – Designed vs. measured

It can be observed that the filters that were implemented have the desired frequency response characteristics.

5.5.1.1. Noise floor of detection circuit

The noise floor of the detection circuit is determined by a number of factors such as the noise introduced in the op-amp filter stages, the noise from the ADC (thermal and quantisation) as well as any external noise coupled to the signal path though conducted and radiated EMI sources.

Fig. 5-25 shows the noise floor that was measured after performing an 8192-point FFT of the ADC data sampled at 409.6 kSPS while the voltage measurement terminals were left short circuit (not connected to grid). It can be seen that the noise is dominant in the pass band spectrum of the analogue filter. It is observed that the noise floor in the pass band region is approximately -80 dB (ADC full scale being ±2 V and the average noise at 200 µV) and the noise floor that is significantly outside the pass band (0 - 10 kHz and >50 kHz regions) is approximately -108 dB (average noise at 8 µV).

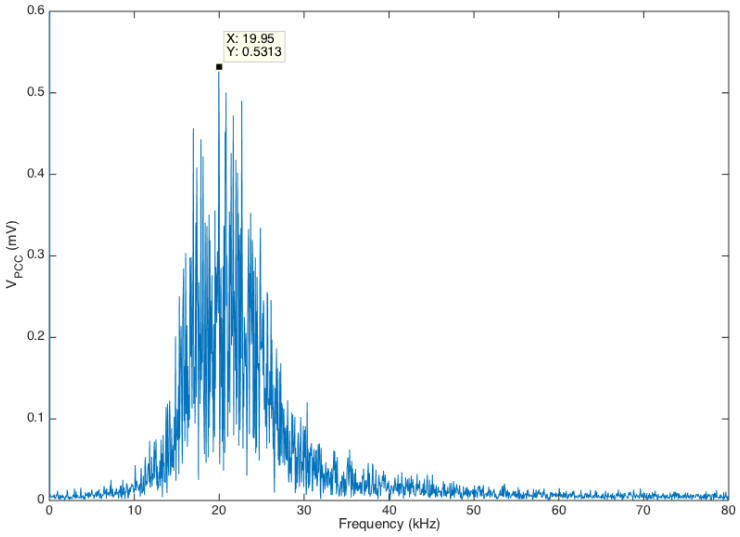


Fig. 5-25 Voltage detection circuit noise floor

The level of noise outside the filter band is mainly determined by the ADC's quantisation noise level, FFT process gain and any additional noise introduced from outside sources. Since the ADC resolution is 16-bits, the effective theoretical signal-to-noise ratio (SNR) is 98.1 dB (based on

quantisation noise) however, the datasheet specified SNR for the device is 93 dB. The FFT process gain for an 8192-point FFT is 36.1 dB. Therefore, the ideal noise floor lies at -129.1 dB. This is in contrast to the observed out of band noise floor at -108 dB.

The increased noise floor (-80 dB) for the pass band region is expected as the analogue filter stages have a gain of 34 dB, which amplifies any noise that is coupled from external interference sources as well as introducing noise that is inherent in the BPF circuit such as thermal, flicker and shot noise.

The spurious free dynamic range (SFDR) of the circuit was measured to be 71 dBFS in the pass band region (largest spur at 530 μV). The noise floor of the pass band relative to the grid voltage is -124 dB (340 V peak vs. 200 μV).

The tests that were performed indicate that the circuit that was designed and realised exceeds the requirements for detecting the small level signals present during islanding condition.

5.5.2. Estimation of grid impedance

The magnitude of the grid impedance at 20 kHz ($|Z_{grid}(20\ kHz)|$) can be defined as follows.

$$|Z_{grid}(h)| = \frac{|V_{PCC}(h)|}{|I_g(h)|} \qquad \textbf{(5-8)}$$

Therefore it is possible to estimate $|Z_{grid}(20\ kHz)|$ by measuring the magnitude of the high frequency components of V_{PCC} and I_g during operation of the inverter with no RLC load connected. The results that were obtained for the utility grid of the laboratory when the inverter was operating at 2.2 kW are highlighted in Table 5-5 below (without an RLC load connected). The band pass filtered V_{PCC} and inverter current waveforms and the associated frequency spectra are shown in Fig. 5-26 and Fig. 5-27.

Table 5-5 Estimated grid impedance from measured values of voltage and current ripple

Parameter	Value	Parameter	Value
$\|V_{PCC}(19.95\ kHz)\|$	73.39 mV	$\|V_{PCC}(20.05\ kHz)\|$	72.17 mV
$\|I_g(19.95\ kHz)\|$	30.06 mA	$\|I_g(20.05kHz)\|$	30.12 mA
$\|Z_{grid}(19.95\ kHz)\|$	2.44 Ω	$\|Z_{grid}(20.05kHz)\|$	2.39 Ω

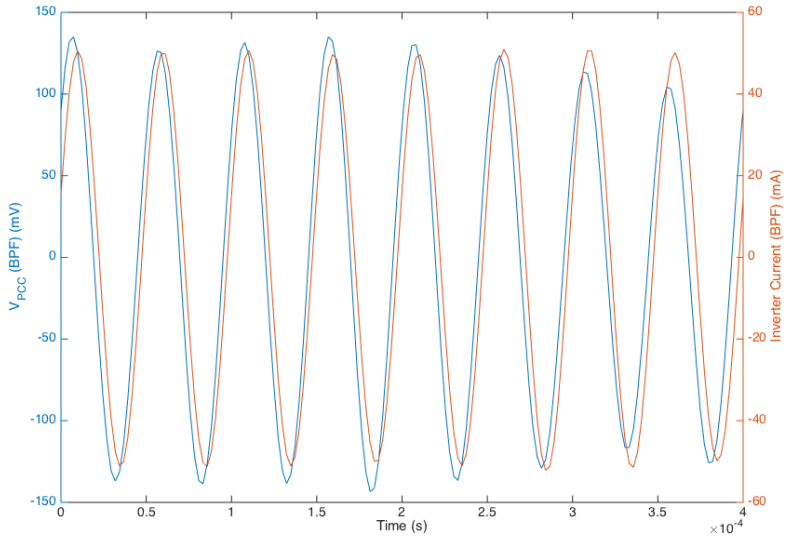


Fig. 5-26 Band pass filtered V_{PCC} and inverter current waveforms

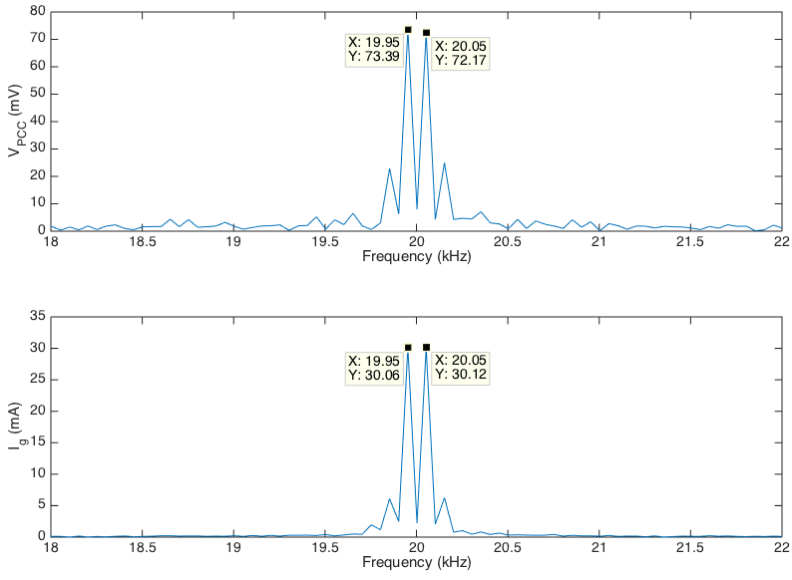


Fig. 5-27 - Frequency spectrum of V_{PCC} and inverter current

The experimentally derived high frequency grid impedance value has been utilised as a starting point for determining the worst-case ripple magnitude. It must be noted that in practical realization of the system, the maximum acceptable grid impedance for high frequencies must be determined on a case-by-case basis dependant on the grid configuration for which the detailed analysis is beyond the scope of this thesis.

5.5.3. Results of islanding detection test

Resistive Load

The islanding detection test has been carried out for the resistive load case with a load resistor of 26.2 Ω and inverter power output of 2.2 kW. The resulting waveforms are presented in Fig. 5-28 and the spectrum of the switching frequency harmonics in Fig. 5-29. It is evident that the resistive load case is detectable. The pre-islanding voltage ripple of the 19.95 kHz component is 71.57 mV and post islanding, it reaches 612.8 mV. The values obtained experimentally compare to the analytical prediction of 70.5 mV and 444.3 mV and SimPowerSystems simulation results of 72.19 mV and 442.2 mV for pre and post islanding cases respectively. It can be seen that the predicted and actual pre-islanding ripple matches. The higher value of post islanding voltage ripple can be attributed to the series inductance of the load resistor bank.

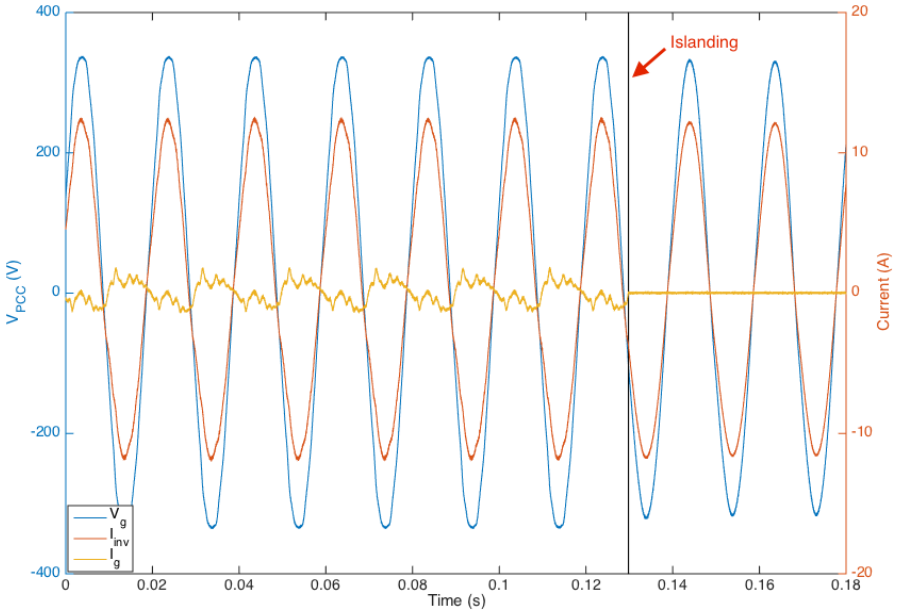


Fig. 5-28 Islanding test waveforms for resistive load test

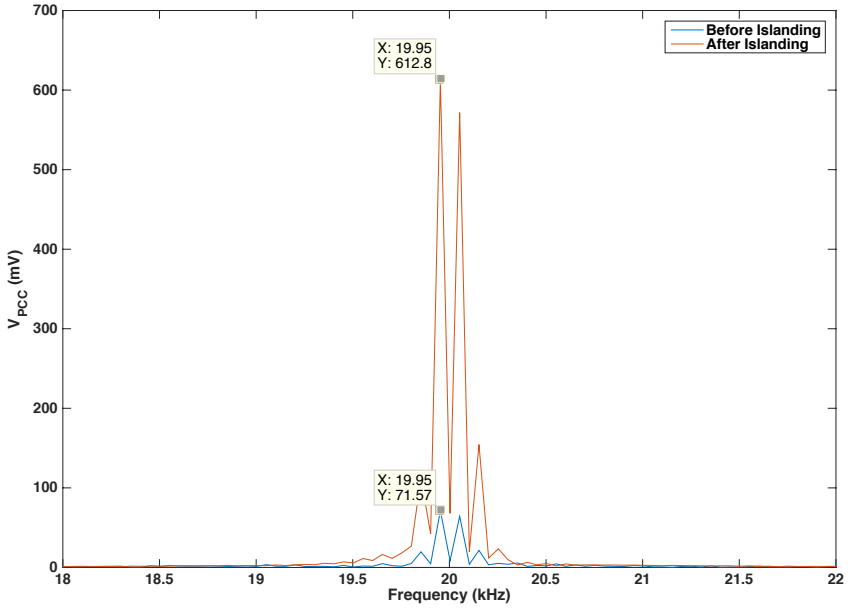


Fig. 5-29 Islanding test frequency spectrum for resistive load test

RLC Load

The RLC load based islanding detection test has been carried out with the conditions depicted in Table 5-6 for an inverter power output of 2.2 kW. The resulting waveforms are presented in Fig. 5-30 and the spectrum of the switching frequency harmonics in Fig. 5-31. It can be seen that islanding is successfully detected for the RLC load under consideration. The pre-islanding voltage ripple of the 19.95 kHz component is 55.1 mV and after islanding, it reaches 132.7 mV. The values obtained experimentally compare to the analytical prediction of 57.6 mV and 131.2 mV for pre and post islanding cases respectively. It is observed that the post islanding ripple prediction and experimental values closely matches unlike the purely resistive test case. It was mentioned that the load resistor bank's series inductance is the reason for the higher amount of ripple that appear under the resistive load test. However, it can be seen that in the RLC load test, the capacitance is the dominant shunt component for high frequencies and therefore the series inductance of the resistor has a negligible affect on the post-islanding ripple.

Table 5-6 RLC Test Conditions

R (Ω)	L (mH)	C (μF)	R_L (Ω)	R_{esr} (mΩ)	$\|Z_{rlc}\|$ (20 kHz) (Ω)
26.4	318	32.3	6.28	20	5

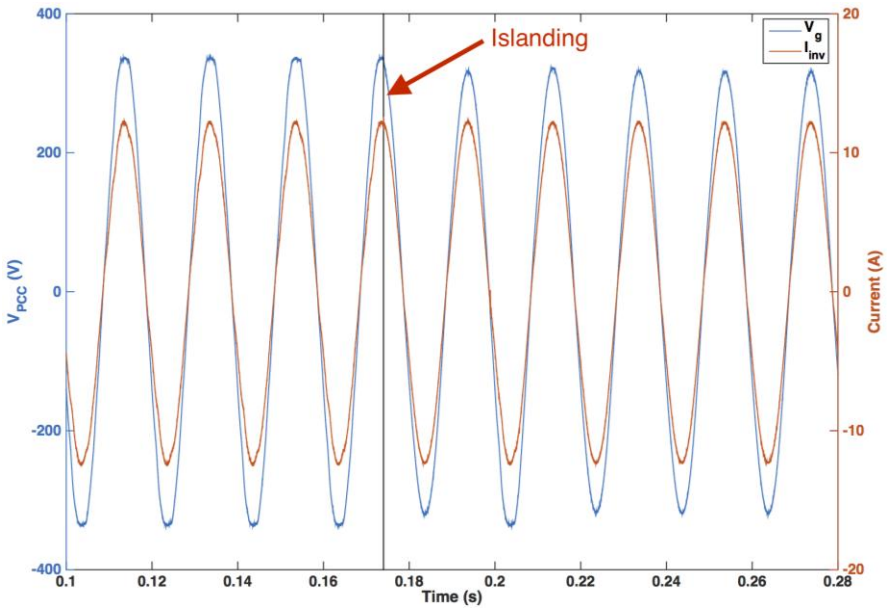


Fig. 5-30 Islanding test waveforms for RLC load test

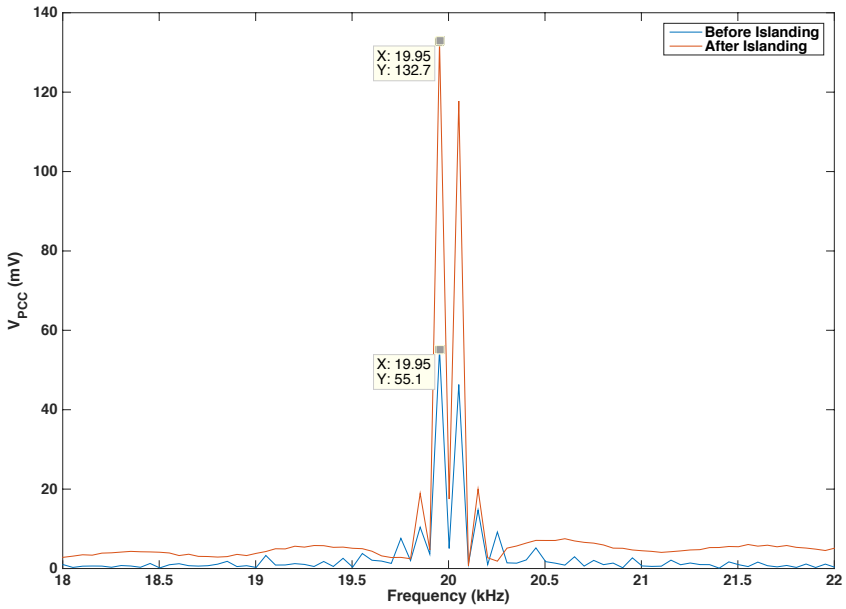


Fig. 5-31 Islanding test frequency spectrum for RLC load test

5.6. Discussion and conclusions

A new islanding detection algorithm has been presented which has the advantage of multi-inverter compatibility compared to similar voltage harmonic monitoring methods.

Furthermore, the difficulty in detection for PWM harmonic based methods when capacitive loads are present has been analysed and the detectable conditions as a function of the load's characteristics established. The algorithm has been simulated as well as two test cases demonstrated in hardware.

The detection hardware that was designed and demonstrated has been over engineered since the exercise was purely for a proof of concept. It follows from analysing measured SNR and SFDR of the prototype detector that the hardware may be optimised in terms of ADC resolution and sample rate to achieve a trade off between performance and cost. In particular, it is feasible to use the integrated 12-bit ADCs that are common in many low cost DSP/microcontrollers that are used in the control of grid converters.

The requirement for computing power can be minimised by either optimising the FFT length or by utilising an optimised version of an FFT algorithm that caters only for the frequency range of interest.

The proposed frequency hopping method may also be suitable for other active islanding detection schemes where low order harmonics are injected. Further investigations are required for its applicability in these schemes.

Chapter 6

Conclusions and Future Work

6.1. Conclusions

Two options of bi-directional charging have been presented in the first part in this thesis, which are, low frequency transformer based and high frequency DAB based systems. The optimised design method of LCL filters for the AC-DC stage of both systems has been presented with details on the design of the inductors and transformers and the differences of the two methods in terms of weight, efficiency and cost have been compared. It has been shown that the low frequency option, which integrates the motor drive inverter, can be an attractive option for a low cost OBBC system whereas the DAB based system offers the advantage of a lower weight. Both systems were shown to have a similar efficiency therefore the actual method of implementation can be chosen depending on the application's constraints of size/weight vs. cost.

In the third chapter, the controller design methodology for the two types of bidirectional charger systems has been presented, followed by simulation and experimental validation. More specifically, the harmonic compensator performance has been validated in hardware, which shows significant improvement to the power quality and therefore enables the converter to meet the grid harmonic standards (IEEE 519). Furthermore, the detailed transient performance of the controllers has been characterised. The details of the hardware setup for the two bi-directional chargers that were designed and built have also been presented. From the simulation and experimental results, it can be concluded that the controller design for the two topologies of bidirectional chargers presented fulfils the performance requirements for a bidirectional charger system. Furthermore, the LCL filter design methods that were discussed in the preceding chapter have also been validated with a simulational

and experimental performance comparison and shown to have good agreement with the analytical prediction in terms of the high frequency current harmonics and power dissipation in the damping resistor. Therefore it can be concluded that the LCL design methodology that was discussed in Chapter 2 is able to successfully optimise the weight and efficiency of the LCL filter as well as providing a guideline value for the power rating required for the damping resistor.

The chapter on PLLs has focussed on two key contributions that have been made for improving the current state of the PLL techniques used for grid synchronisation. The first section investigated the impact of 3rd harmonics on the performance of SOGI PLLs whereby an analytical method has been developed to predict the resulting output harmonic magnitudes. This has been followed by the proposal of two different methods to improve the harmonic rejection capability of the SOGI PLL. It has been shown through HIL simulation results that the harmonic rejection performance could be dramatically improved by the addition of notch filters in either the feedback or pre-filter configurations. The second part of the chapter investigated viability of the PLL structure, which was based on the novel IIR filter proposed by Ed Daw et al. for the application in grid converters. The operation of the enhanced PIIR PLL has been outlined after which it was shown through HIL simulation that the PLL shows desirable characteristics such as faster transient response times and better DC offset rejection attributes compared with the SOGI PLL and therefore shows good suitability for grid synchronisation applications. Both the improved SOGI as well as the PIIR PLLs were validated experimentally in the low frequency based OBBC hardware platform for both G2V and V2G modes of operation.

In the final chapter, a new islanding detection algorithm based on the detection of high frequency switching harmonic signature has been presented which has the advantages of better noise immunity as well as multi-inverter compatibility compared to similar voltage harmonic monitoring methods. The

difficulty in islanding detection for PWM harmonic based methods when capacitive loads are present has been analysed and the detectable conditions as a function of the load's characteristics established. Simulation as well as experimental results has been presented demonstrating the viability of the new algorithm.

6.2. Future Work

Future work can be carried out on the bidirectional charger, specifically with the dual active bridge topology which can be experimentally validated. Furthermore, the application of more recent modulation methods such as variable frequency modulation [92, 95, 97] and hybrid modulation schemes [89, 91, 96] on the DAB converter can be evaluated to increase system efficiency. Detailed thermal and housing design for the two converters can be performed using a similar method as presented in [202].

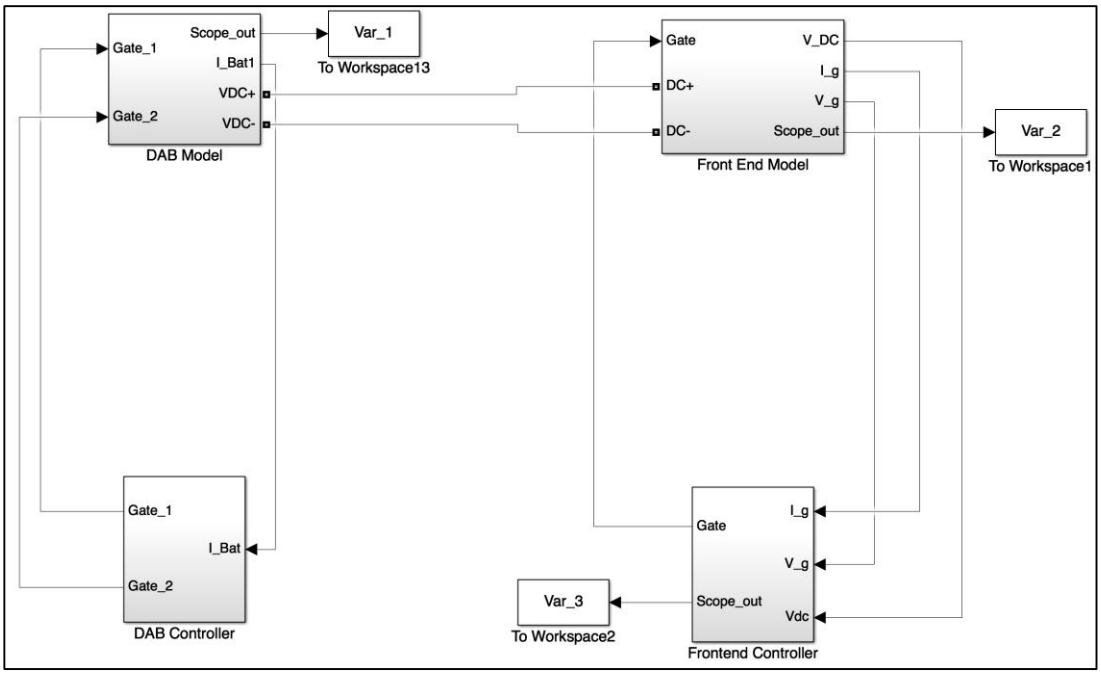
There is further scope for work in improving the PIIR PLL's harmonic rejection capability whilst simultaneously reducing the computational complexity of the PLL. In particular, the frontend pre-filter stages as well as the *atan2* functions could be eliminated if the harmonic rejection capability of the PIIR is improved.

Optimisation of the islanding detection algorithm for application in low cost DSP systems can be carried out for enabling the practical viability of the method in OBBC as well as PV inverter systems where a low price point is critical. Furthermore, the islanding detection algorithm's frequency hopping function needs to be verified experimentally with a multi inverter configuration. The suitability of the proposed frequency hopping method for other active islanding detection schemes where low order harmonics are injected can be further investigated for determining whether multi-inverter interference could be reduced.

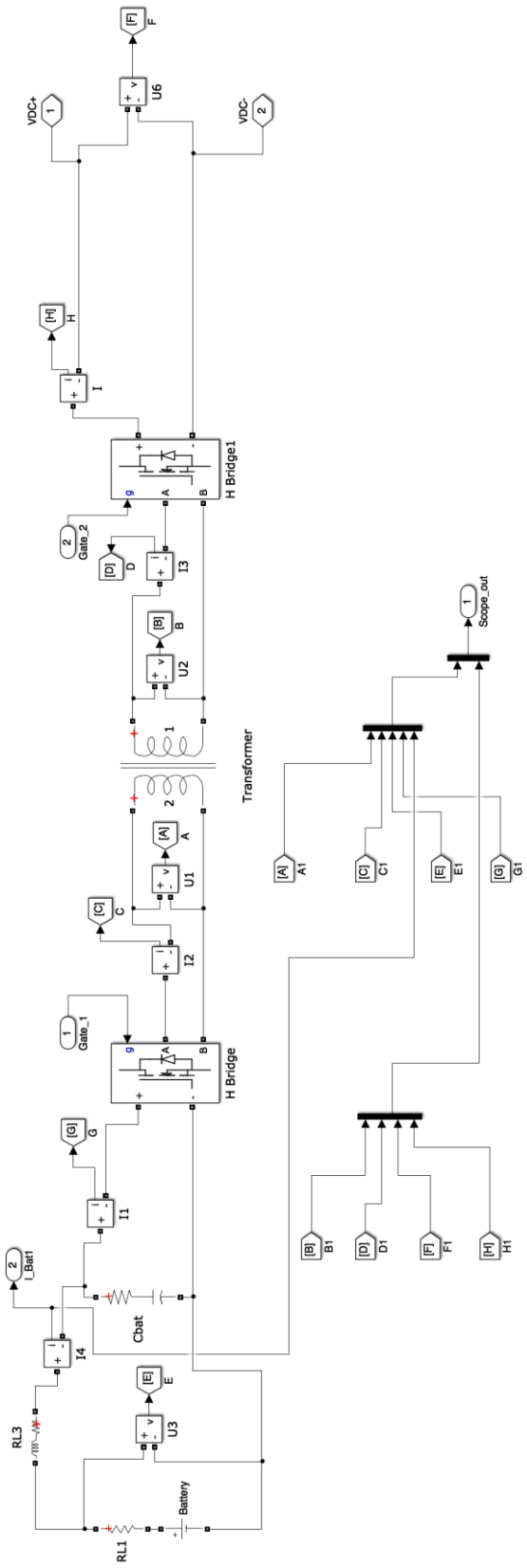
Appendices

Appendix A: HF Charger Simulink Diagrams

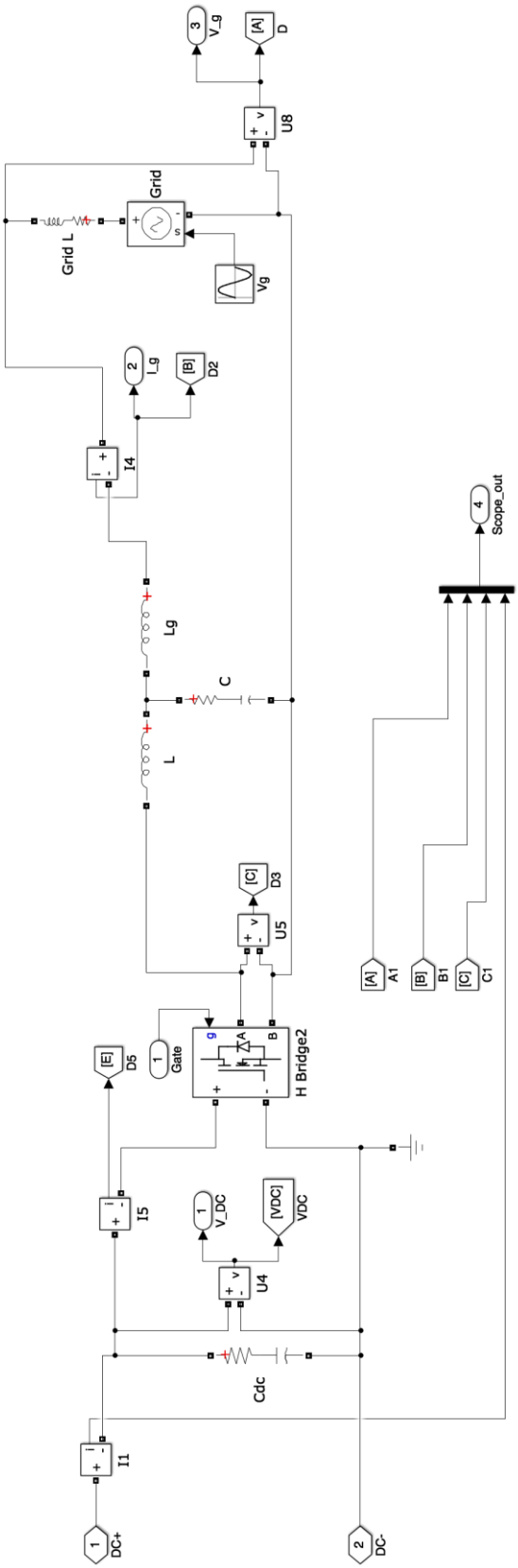
Top level Simulink structure of HF charger



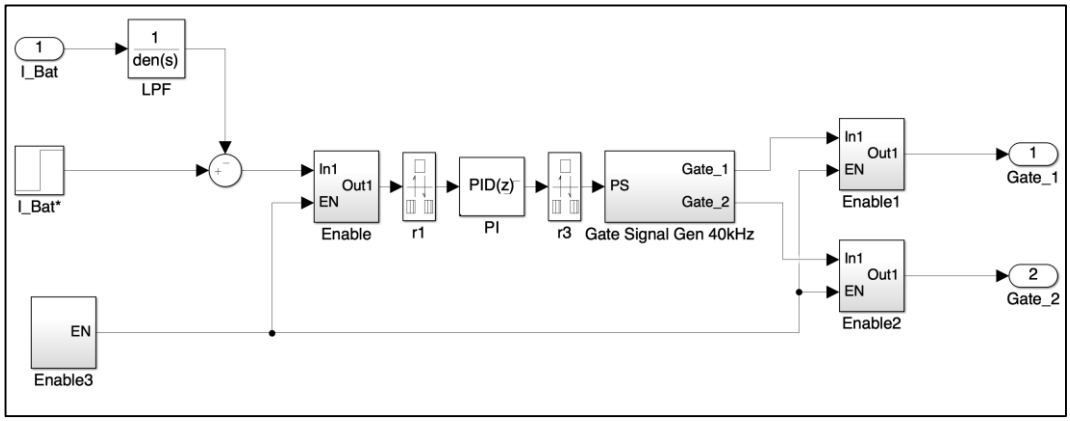
DAB model


VDC+
VDC-
U6
H Bridge1
Gate_2
I3
U2
Transformer
U1
I2
Gate_1
H Bridge
I1
I_Batt
Cbat
I4
U3
RL3
RL1
Battery
Scope_out
A1
C1
E1
G1
B1
D1
F1
H1

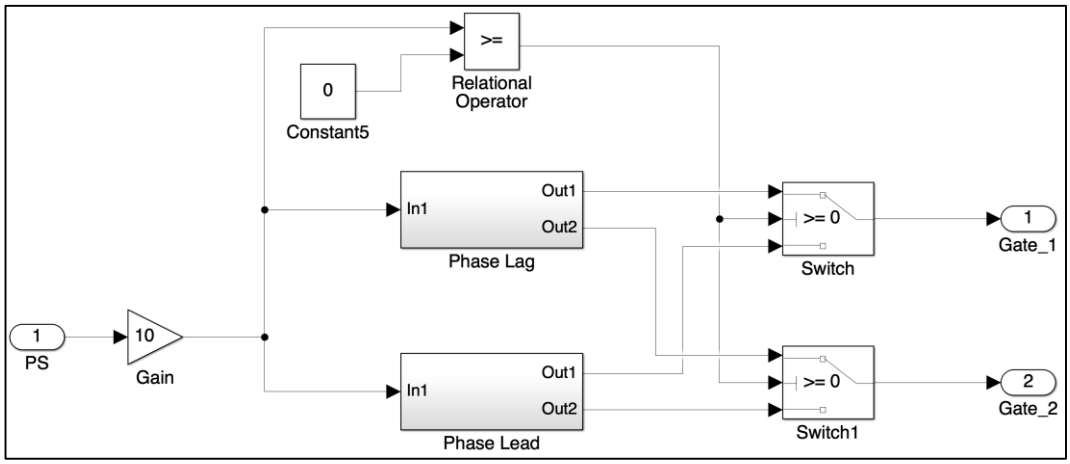
Front end model



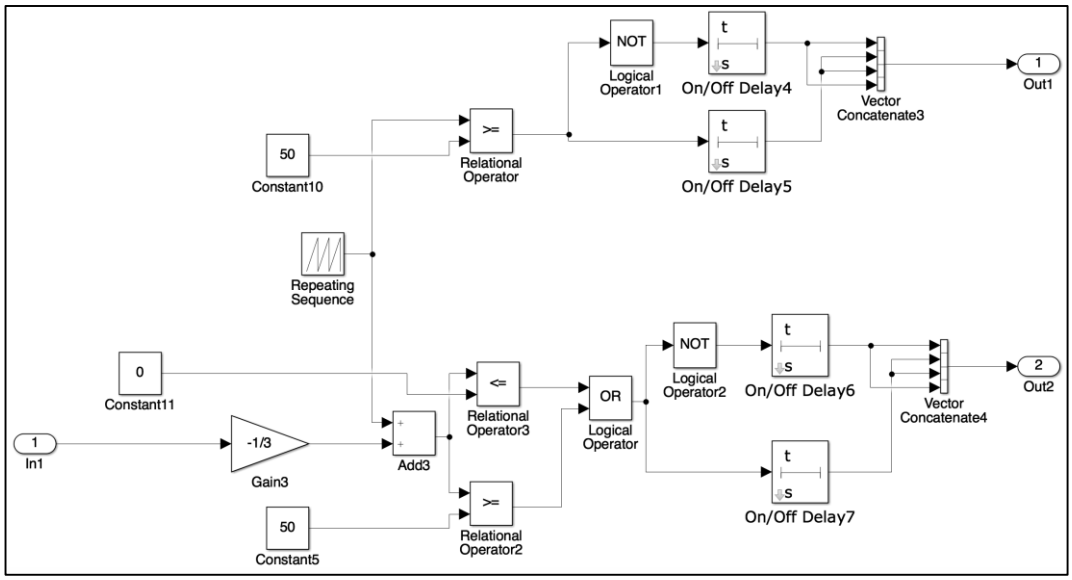
DAB controller



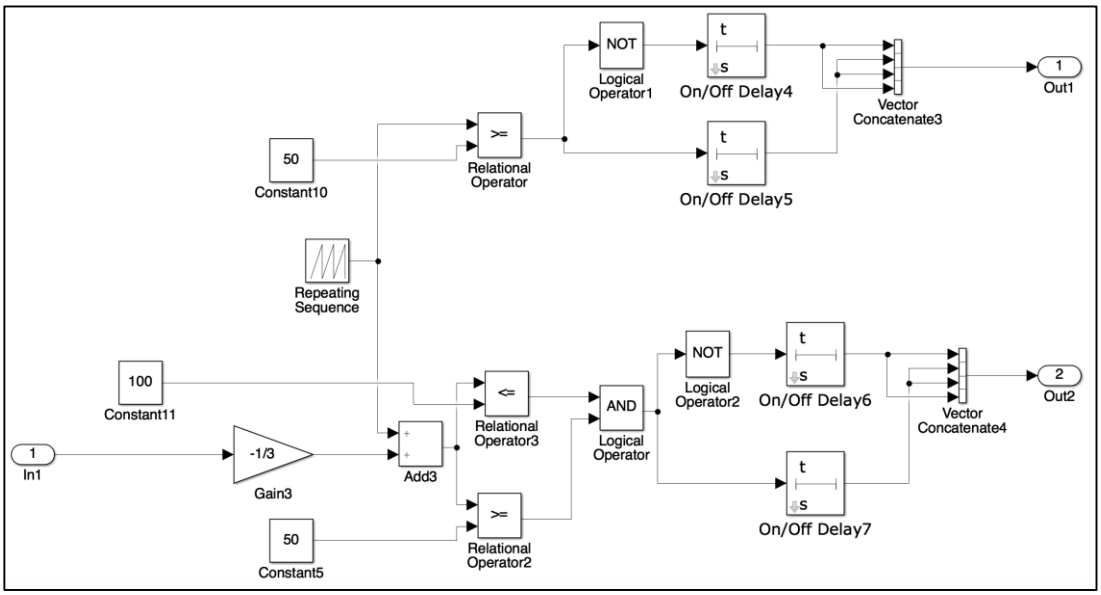
DAB gate signal generator



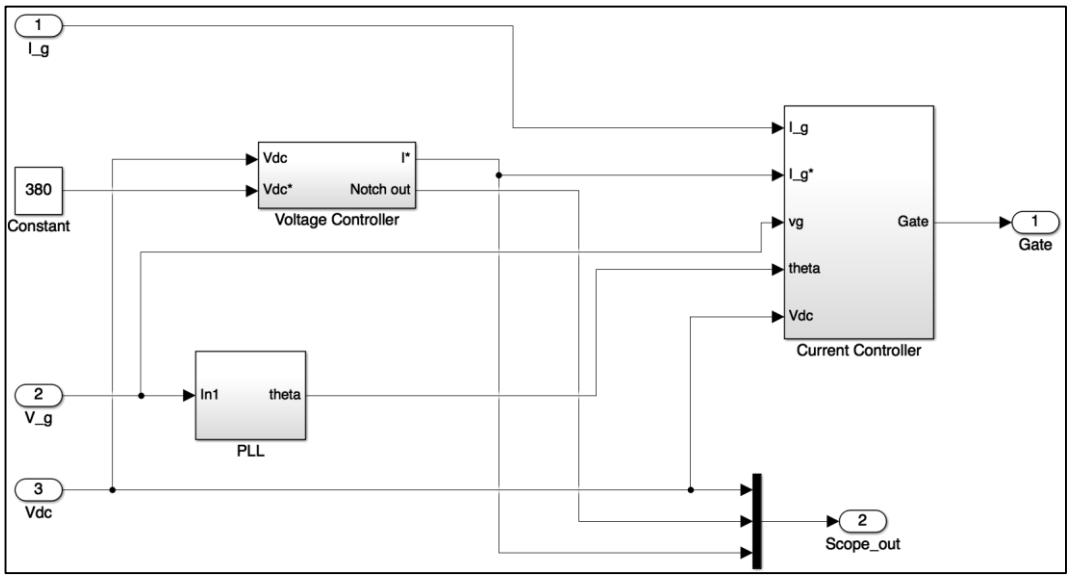
Phase lag



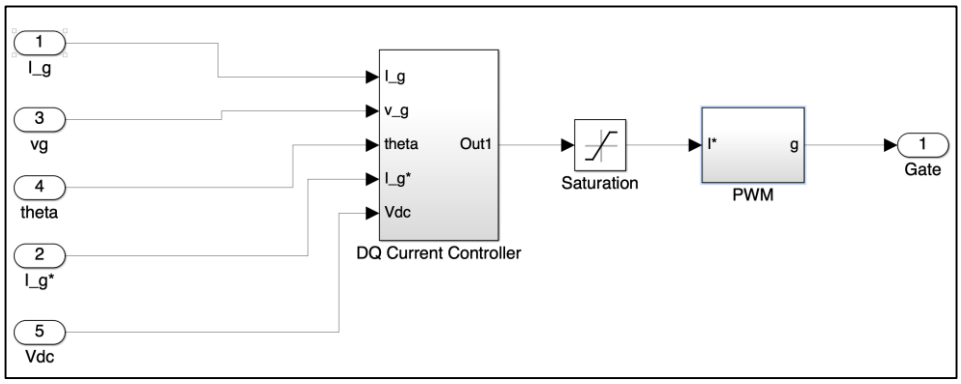
Phase lead



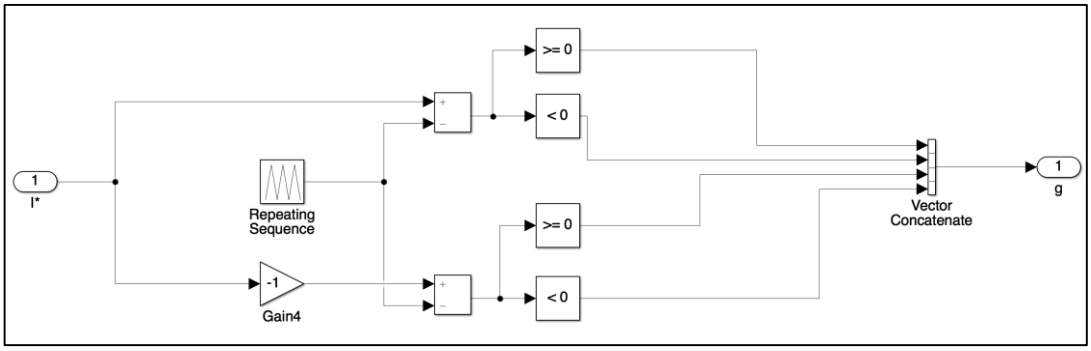
Frontend controller



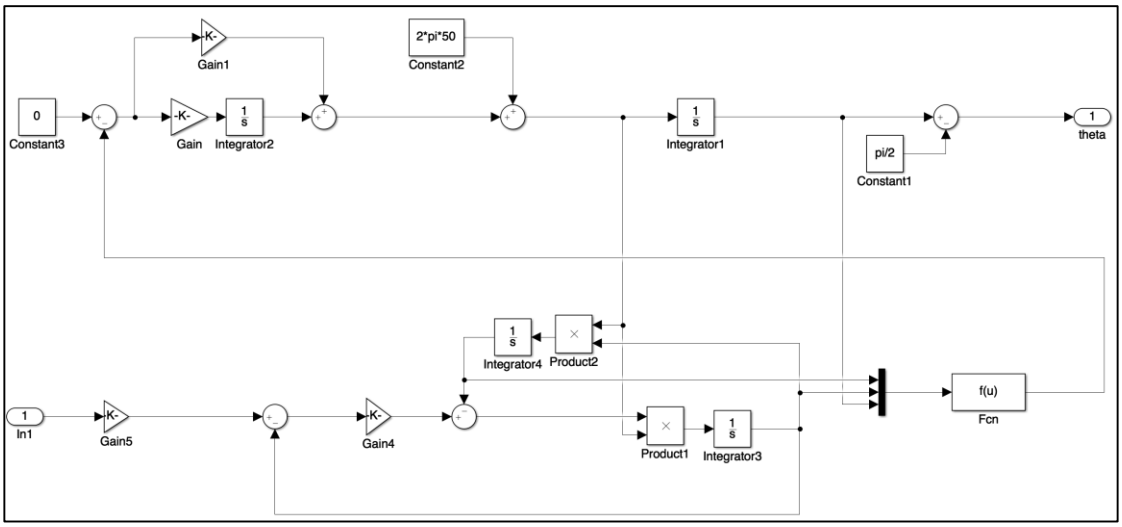
Current controller



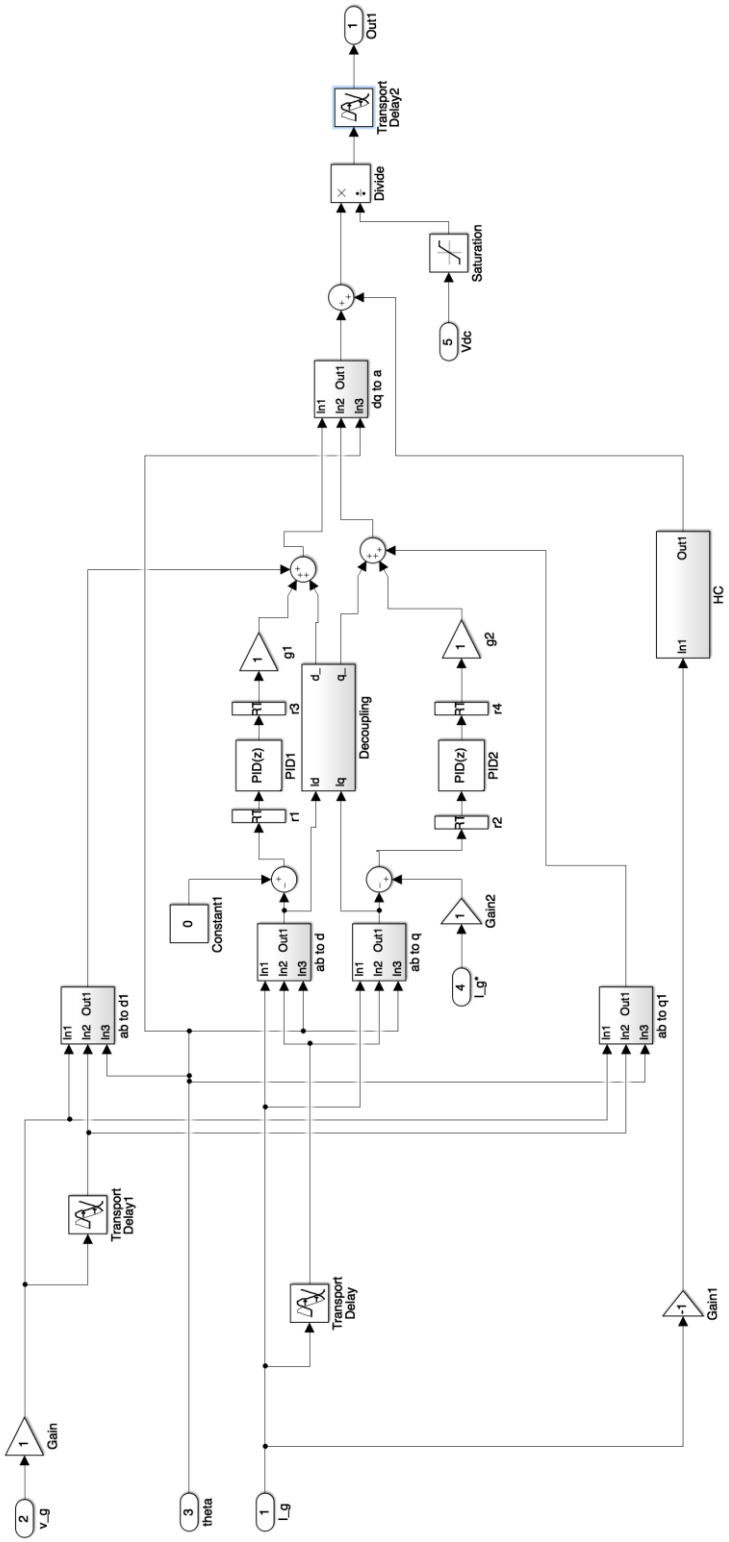
PWM



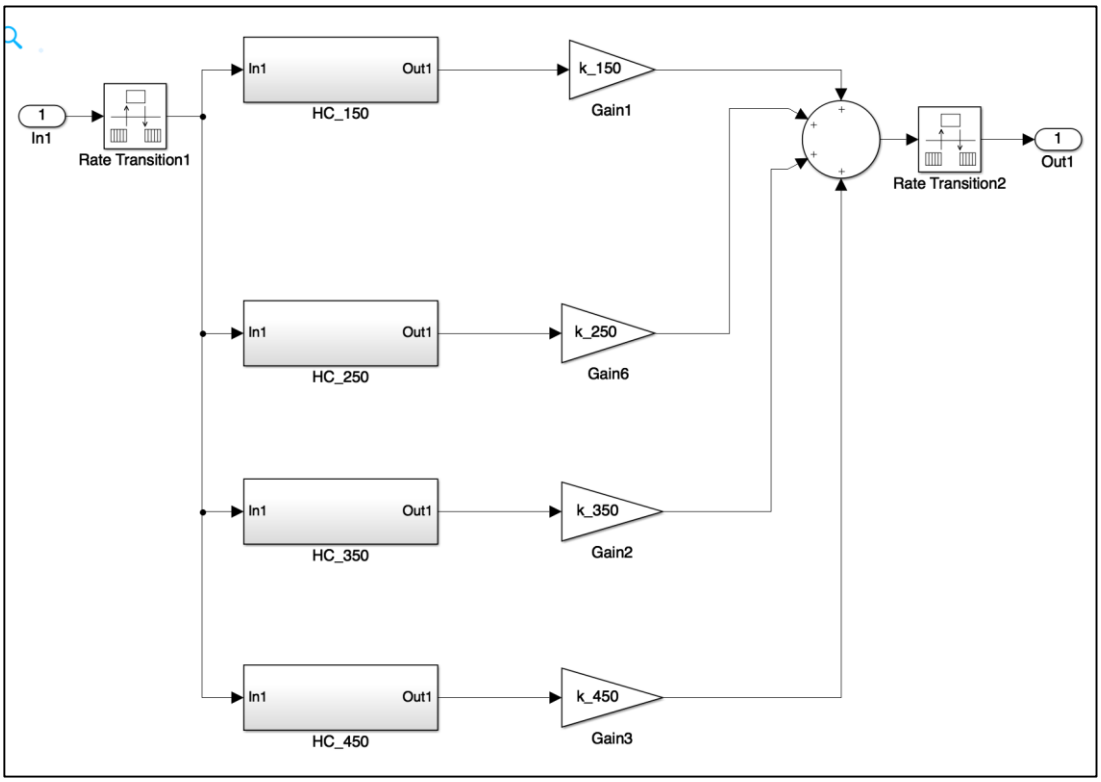
SOGI PLL



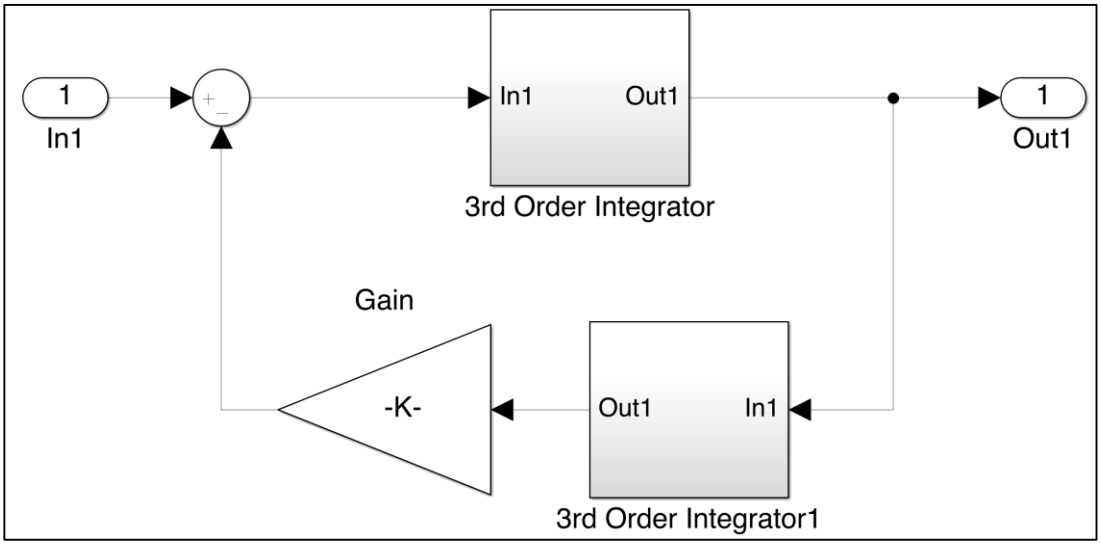
DQ Current Controller



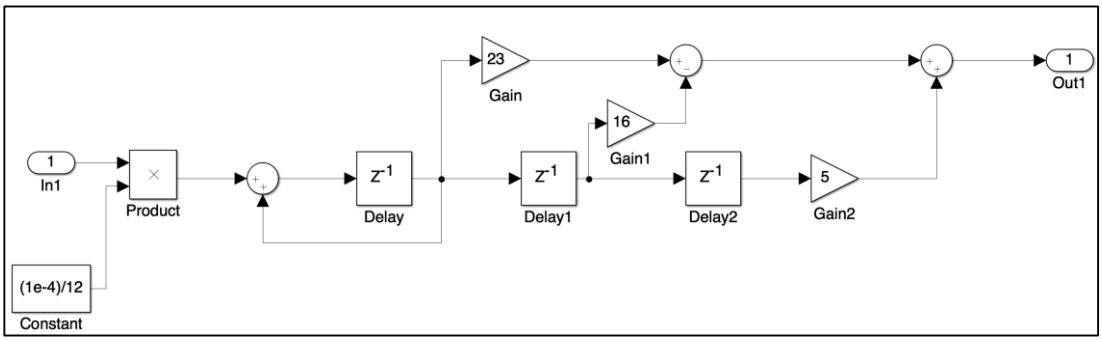
Harmonic compensator (HC)



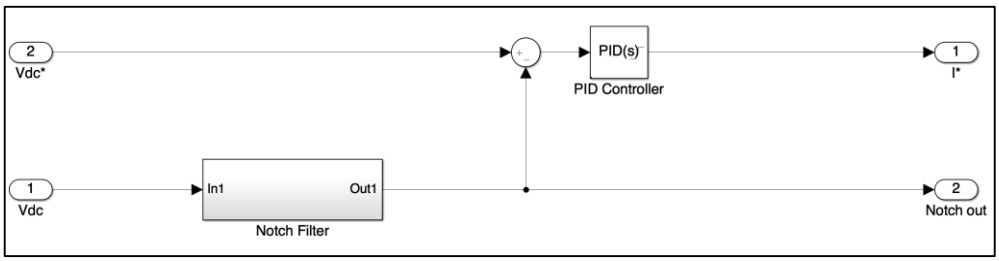
HC_150



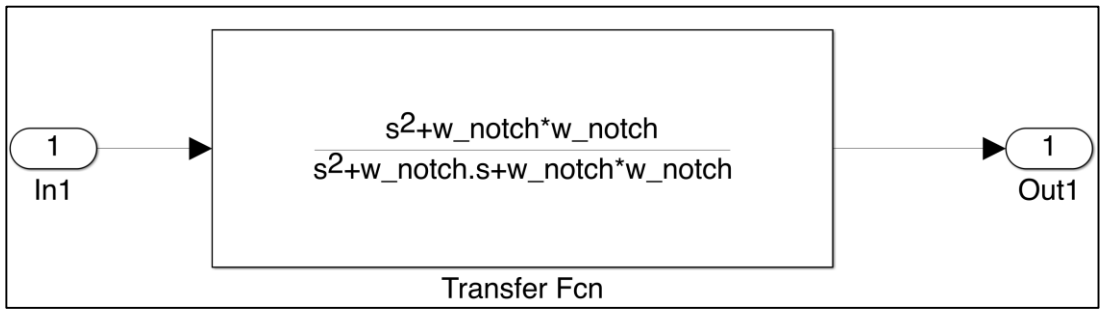
3rd order integrator



Voltage controller



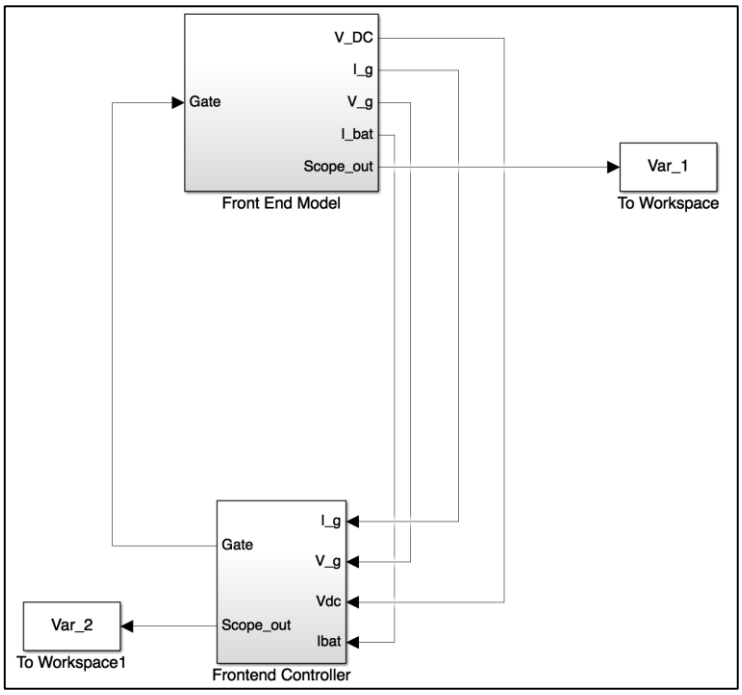
Notch filter



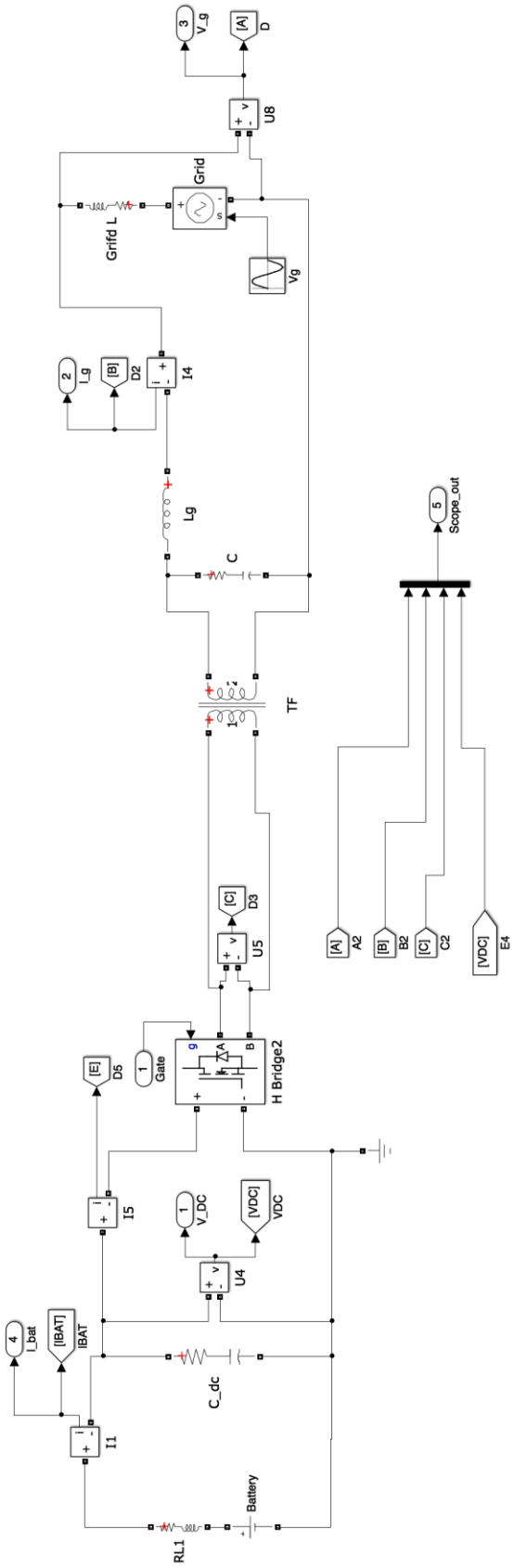
Appendices

Appendix B: LF Charger Simulink Diagrams

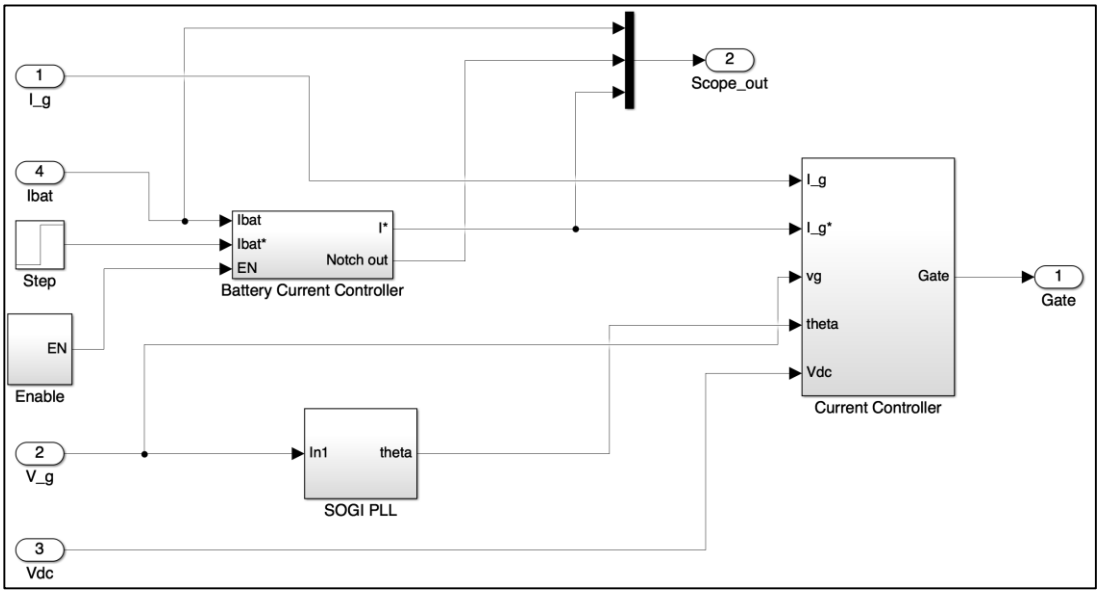
Top level Simulink structure of LF charger



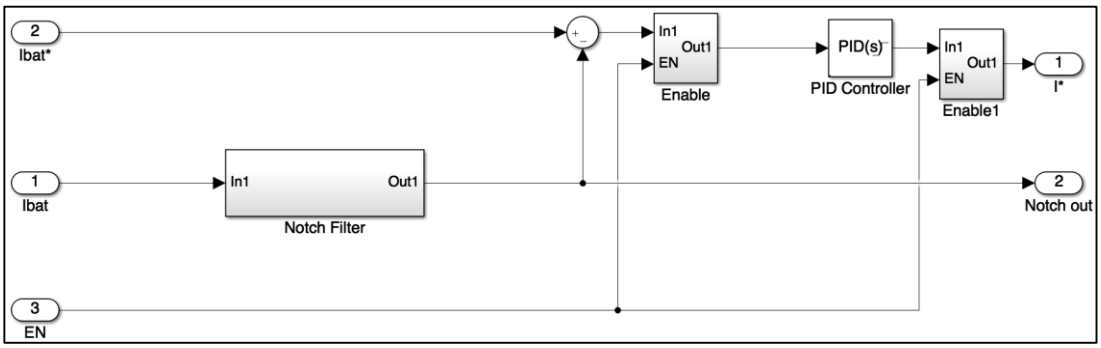
Frontend model



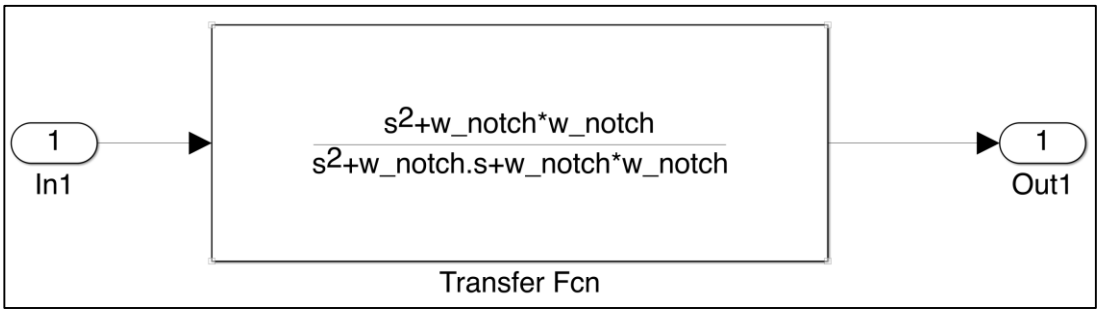
Frontend controller



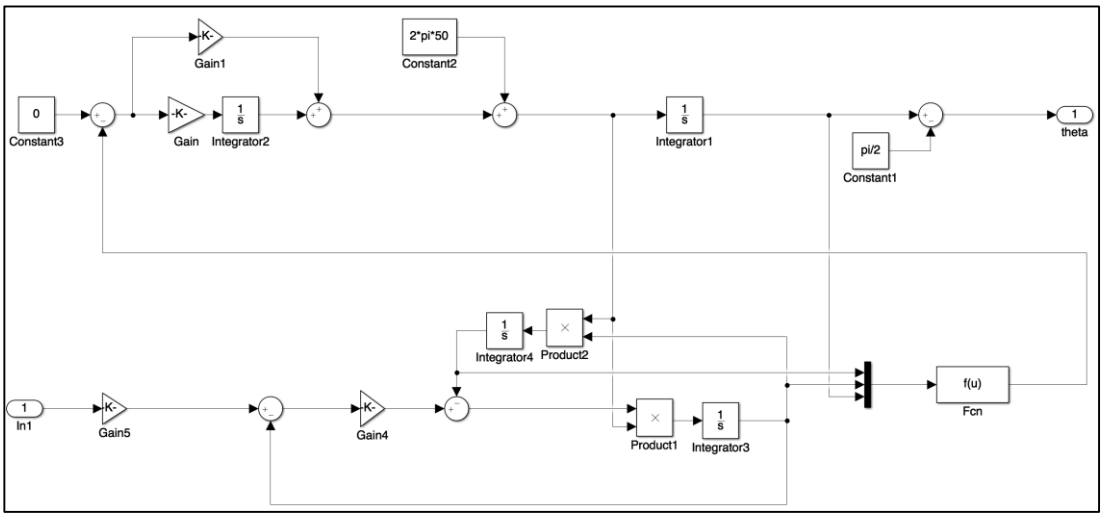
Battery current controller



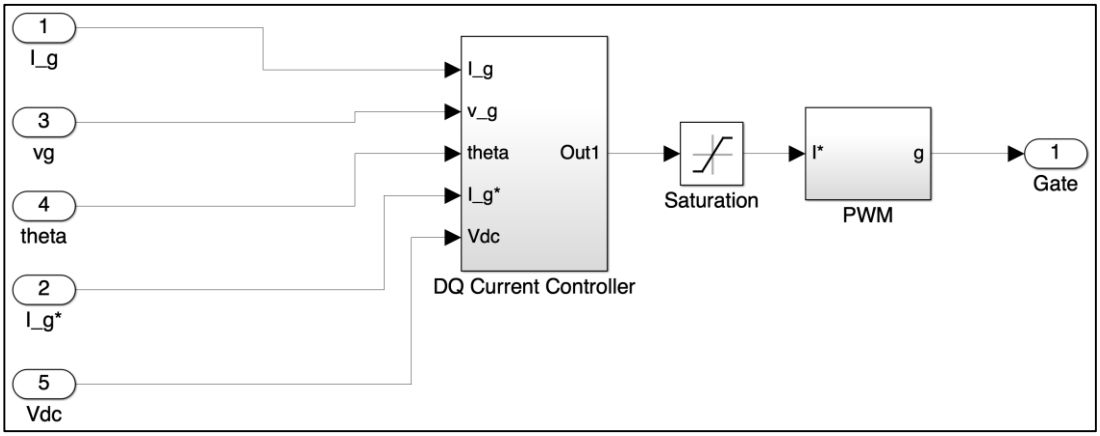
Notch filter



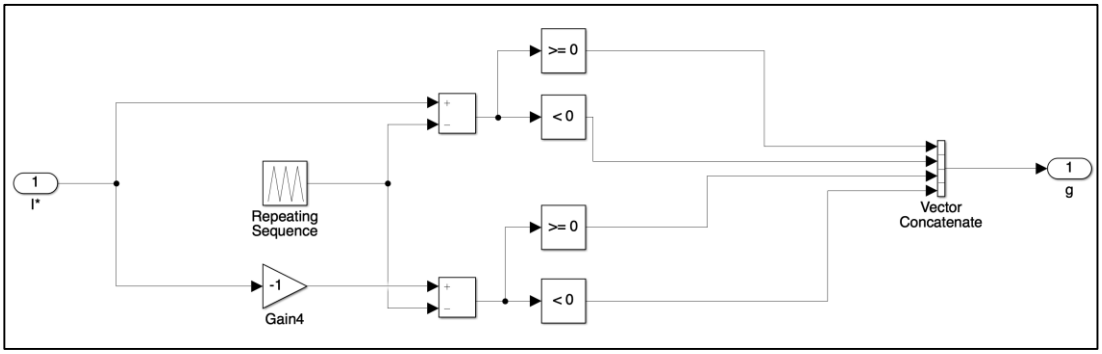
SOGI PLL



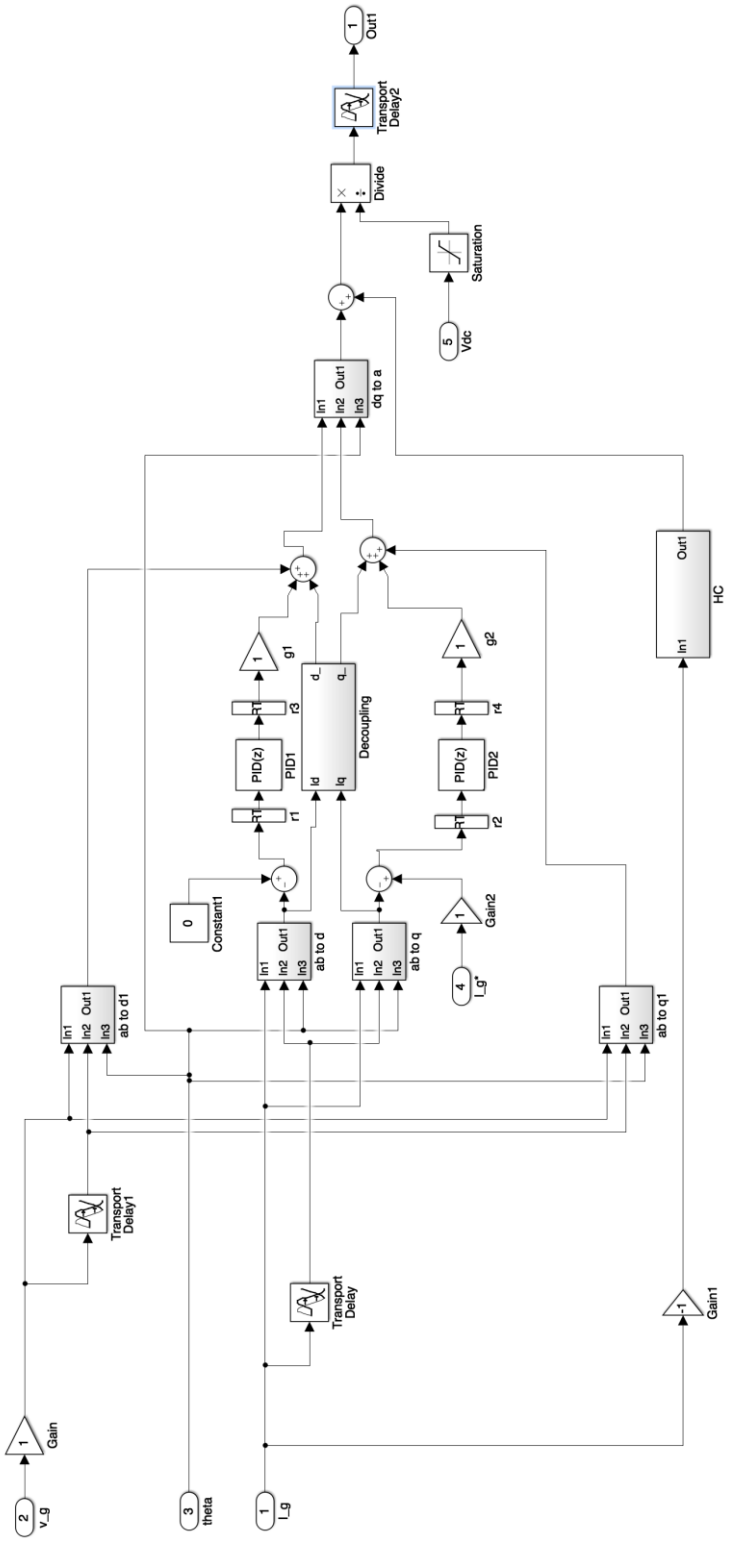
Current controller



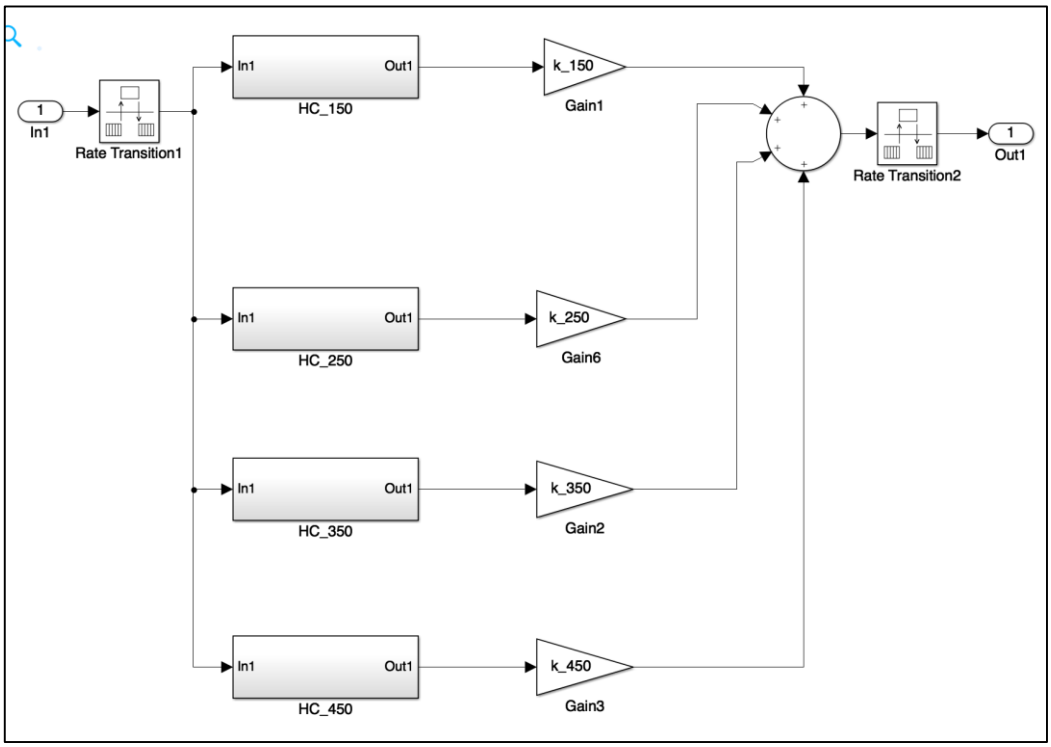
PWM



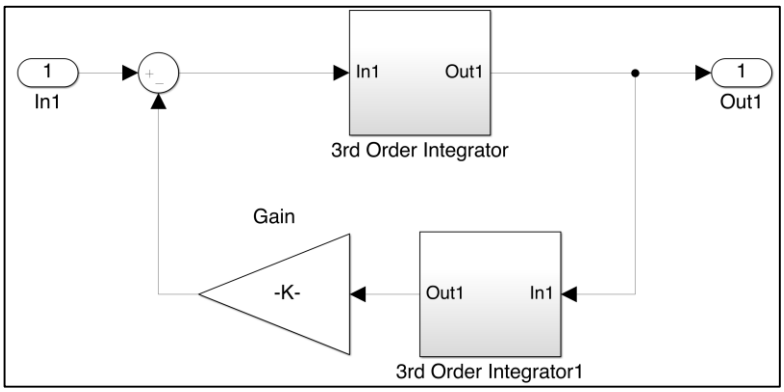
DQ current controller



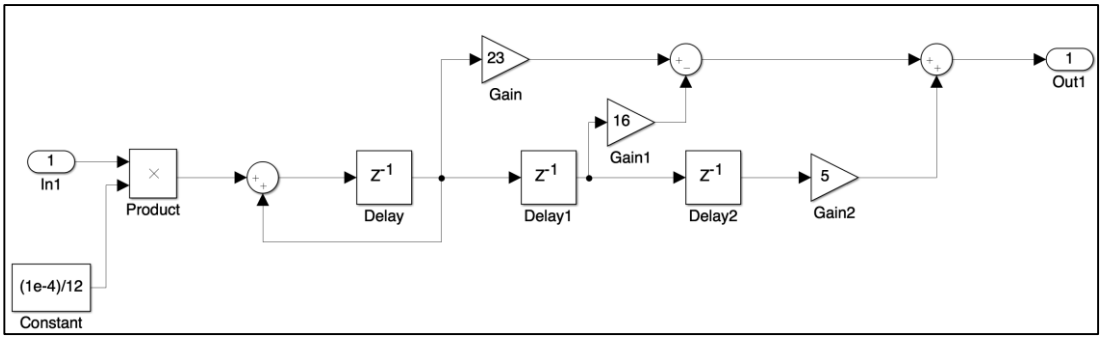
Harmonic compensator (HC)



HC_150

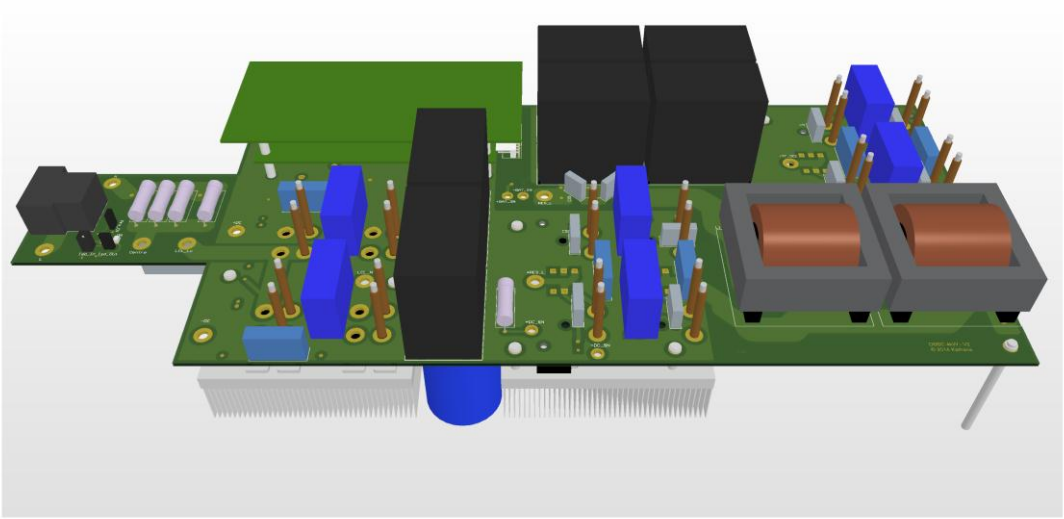


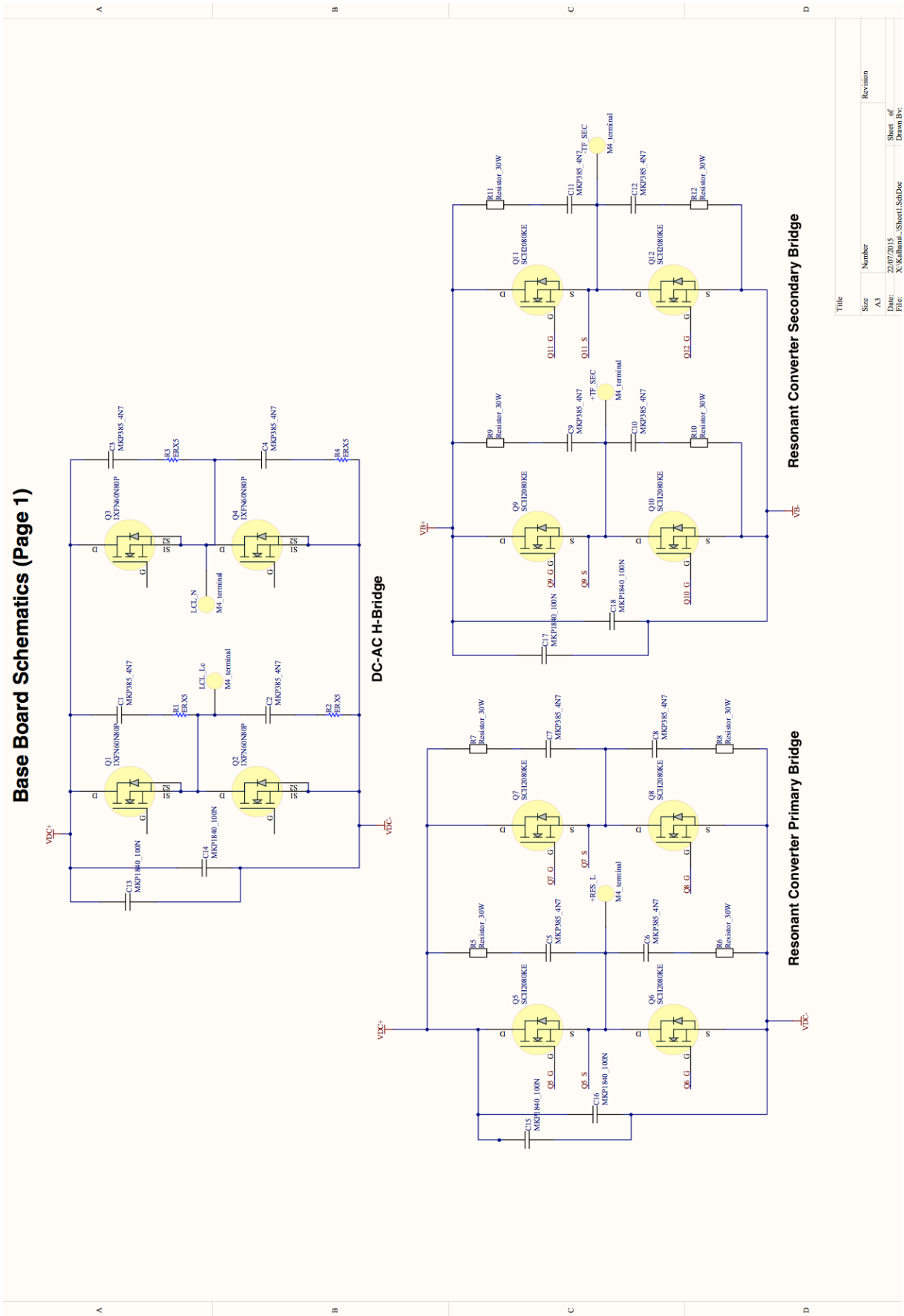
3rd order integrator



Appendices

Appendix C: HF Charger Schematics




Base Board Schematics (Page 1)
DC-AC H-Bridge
Resonant Converter Primary Bridge
Resonant Converter Secondary Bridge
Title
Size
A3
Number
Revision
Date: 22/07/2015
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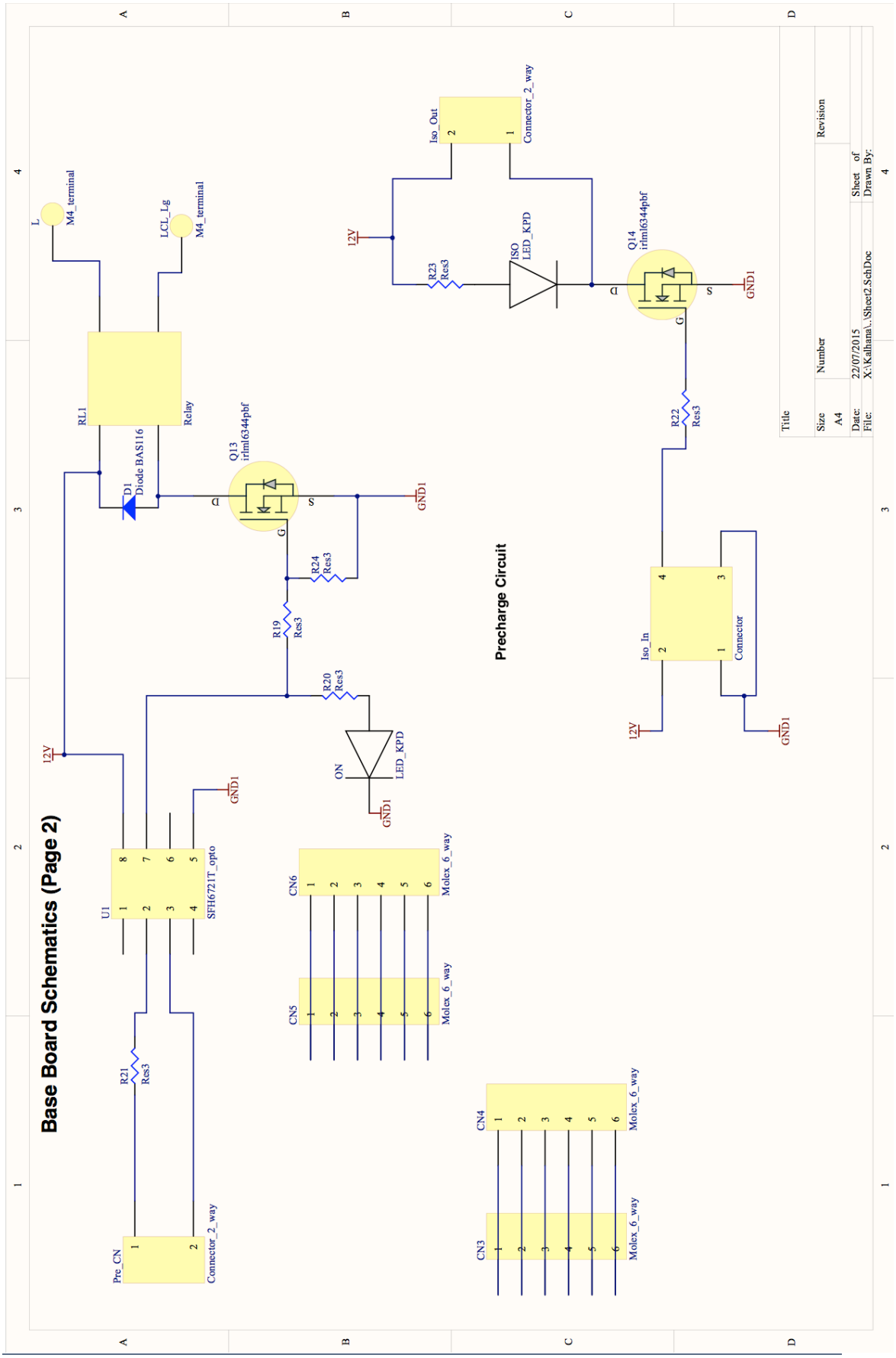
Drawn By:


Base Board Schematics (Page 2)
Precharge Circuit
L
M4_terminal
LCL_Lg
M4_terminal
RL1
Relay
D1
Diode BAS116
Q13
irlml6344pbf
R24
Res3
R19
Res3
R20
Res3
ON
LED_KPD
12V
GND1
U1
SFH6721T_opto
R21
Res3
Pre_CN
Connector_2_way
CN6
CN5
CN4
CN3
Molex_6_way
Iso_Out
Connector_2_way
R23
Res3
ISO
LED_KPD
Q14
irlml6344pbf
R22
Res3
Iso_In
Connector
Title
Size
A4
Number
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Date:
22/07/2015
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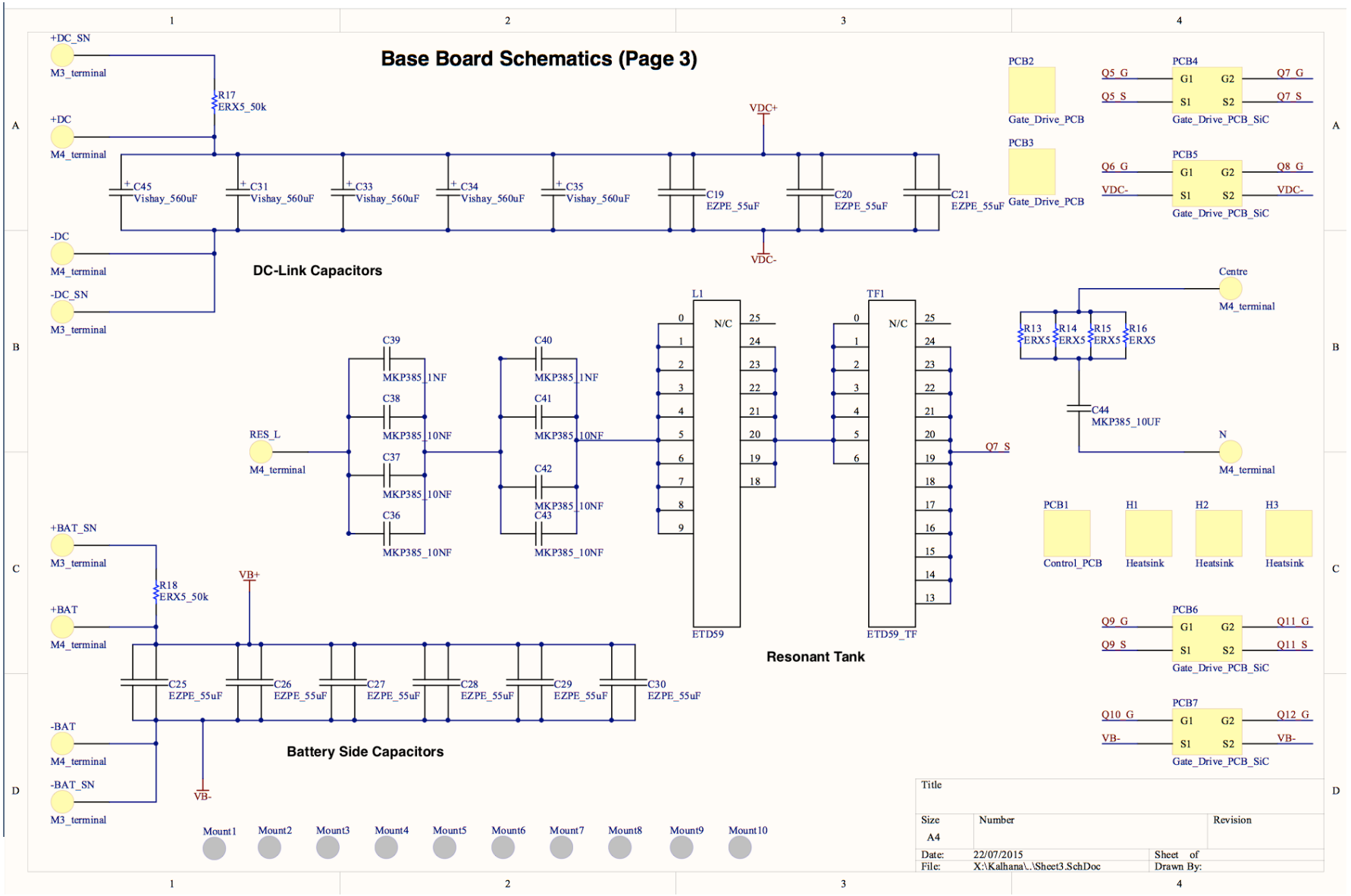
Base Board Schematics (Page 3)
+DC_SN
M3_terminal
+DC
M4_terminal
-DC
M4_terminal
-DC_SN
M3_terminal
R17
ERX5_50k
C45
Vishay_560uF
C31
Vishay_560uF
C33
Vishay_560uF
C34
Vishay_560uF
C35
Vishay_560uF
C19
EZPE_55uF
C20
EZPE_55uF
C21
EZPE_55uF
VDC+
VDC-
DC-Link Capacitors
PCB2
Gate_Drive_PCB
PCB3
Gate_Drive_PCB
PCB4
Q5_G
Q5_S
Q7_G
Q7_S
Gate_Drive_PCB_SiC
PCB5
Q6_G
VDC-
Q8_G
VDC-
Gate_Drive_PCB_SiC
L1
TF1
N/C
ETD59
ETD59_TF
C39
C38
C37
C36
C40
C41
C42
C43
MKP385_1NF
MKP385_10NF
RES_L
M4_terminal
Q7_S
Centre
M4_terminal
R13
R14
R15
R16
ERX5
C44
MKP385_10UF
N
M4_terminal
PCB1
Control_PCB
H1
H2
H3
Heatsink
+BAT_SN
M3_terminal
+BAT
M4_terminal
R18
ERX5_50k
VB+
C25
C26
C27
C28
C29
C30
EZPE_55uF
Resonant Tank
Battery Side Capacitors
-BAT
M4_terminal
-BAT_SN
M3_terminal
VB-
PCB6
Q9_G
Q9_S
Q11_G
Q11_S
Gate_Drive_PCB_SiC
PCB7
Q10_G
VB-
Q12_G
VB-
Gate_Drive_PCB_SiC
Mount1
Mount2
Mount3
Mount4
Mount5
Mount6
Mount7
Mount8
Mount9
Mount10
Title
Size
A4
Number
Revision
Date:
22/07/2015
Sheet of
File:
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Drawn By:

Appendices

Appendix D: Microcontroller Code for PLLs (TI RM46L852)

```
#include "sys_common.h"
#include "system.h"
#include "esm.h"
#include "adc.h"
#include "can.h"
#include "sys_dma.h"
#include "sci.h"
#include "rti.h"
#include "gio.h"
#include "pinmux.h"
#include "sys_dma.h"
#include "etpwm.h"
#include "stdio.h"
#include <math.h>
#include <stdlib.h>

#define pi_2 6.283185307179586
#define one_pi_2 0.159154943091895
#define pi 3.141592653589793
#define two_pi_50 314.1592653589795

//=====================================//
//          SCI Variables
//=====================================//
char text_out[60];
g_dmaCTRL g_dmaCTRLPKT_Tx, g_dmaCTRLPKT_Rx;    /* dma control packet
configuration stack */
uint32 DMA_Comp_Flag;
char Sent_Tx=1;

//-----------------------------------------------------------------//
// Select PLL Type                                                 //
//-----------------------------------------------------------------//
//#define SOGI_PLL               // SOGI PLL
//#define SOGI_Notch_PLL     // SOGI Notch - A PLL
//#define SOGI_Notch_B_PLL // SOGI Notch - A PLL
////#define PIIR_PLL               // PIIR PLL
#define PIIR_PLL_Variable      // Enhanced PIIR PLL

//-----------------------------------------------------------------//
// Select Test Type                                                //
//-----------------------------------------------------------------//
////#define Harmonic_Test
//#define Harmonic_Test_Clipped
```

```
//#define Harmonic_Test_White_Noise
#define Harmonic_Test_DC
//#define Freq_Test
//#define Phase_Test
//#define Voltage_Sag_Test

#define PLL_ts 0.0001
#define PLL_num_samples 12000

//=====================================//
//          PLL Variables
//=====================================//

float DC_shift = 0.02;
float random_number;

#ifdef SOGI_PLL
float SOGI_integrator_z_1[4] = {0, 0, 0, 0};
float SOGI_integrator_z_2[4] = {0, 0, 0, 0};
float SOGI_integrator_z_3[4] = {0, 0, 0, 0};
float SOGI_integrator_z_4 [4] = {0, 0, 0, 0};
float SOGI_integrator_in[4] = {0, 0, 0, 0};
float SOGI_integrator_out[4] = {0, 0, 0, 0};
float SOGI_in, SOGI_theta_out, SOGI_Q, SOGI_PI_out, SOGI_omega, SOGI_cos_out,
SOGI_frequency;
#endif

#ifdef SOGI_Notch_PLL
float SOGI_Notch_integrator_z_1[6] ={0, 0, 0, 0, 0, 0};
float SOGI_Notch_integrator_z_2[6] = {0, 0, 0, 0, 0, 0};
float SOGI_Notch_integrator_z_3[6] = {0, 0, 0, 0, 0, 0};
float SOGI_Notch_integrator_z_4[6] = {0, 0, 0, 0, 0, 0};
float SOGI_Notch_integrator_in[6] = {0, 0, 0, 0, 0, 0};
float SOGI_Notch_integrator_out[6] = {0, 0, 0, 0, 0, 0};
float SOGI_Notch_in, SOGI_Notch_theta_out, SOGI_Notch_Q, SOGI_Notch_Q_Filtered,
SOGI_Notch_PI_out, SOGI_Notch_omega, SOGI_Notch_cos_out, SOGI_Notch_frequency;
float SOGI_Notch_k  = 2.1;
float SOGI_Notch_ki = 7878;
float SOGI_Notch_kp = 137.5;
float SOGI_Notch_Filt_Q = 55;
#endif

#ifdef SOGI_Notch_B_PLL
float SOGI_Notch_B_integrator_z_1[6] ={0, 0, 0, 0, 0, 0};
float SOGI_Notch_B_integrator_z_2[6] = {0, 0, 0, 0, 0, 0};
float SOGI_Notch_B_integrator_z_3[6] = {0, 0, 0, 0, 0, 0};
float SOGI_Notch_B_integrator_z_4[6] = {0, 0, 0, 0, 0, 0};
float SOGI_Notch_B_integrator_in[6] = {0, 0, 0, 0, 0, 0};
float SOGI_Notch_B_integrator_out[6] = {0, 0, 0, 0, 0, 0};
float SOGI_Notch_B_in, SOGI_Notch_B_theta_out, SOGI_Notch_B_Q,
SOGI_Notch_B_Q_Filtered, SOGI_Notch_B_PI_out, SOGI_Notch_B_omega,
SOGI_Notch_B_cos_out, SOGI_Notch_B_frequency;
float SOGI_Notch_B_k  = 2.1;
float SOGI_Notch_B_ki = 7878;
float SOGI_Notch_B_kp = 137.5;
float SOGI_Notch_B_Filt_Q = 55;
```

```
#endif
#ifdef PIIR_PLL
float PIIR_filt_I_temp_z_1 = 0;
float PIIR_filt_I_temp_z_2 = 0;
float PIIR_filt_I_temp_z_3 = 0;
float PIIR_filt_Q_temp_z_1 = 0;
float PIIR_filt_Q_temp_z_2 = 0;
float PIIR_filt_Q_temp_z_3 = 0;
float PIIR_filt_delta = 0.031415926535898; //2*pi*PIIR_filt_f_nom*PIIR_filt_tau_s;  // Initial
delta
float PIIR_in, sin_delta, cos_delta, PIIR_filt_a_b, PIIR_filt_phi_f, PIIR_filt_phi_b,
PIIR_filt_alpha, PIIR_filt_beta, sin_alpha, sin_beta, cos_alpha, cos_beta,
phase_rot_sheer_1_1, phase_rot_sheer_1_2, phase_rot_sheer_2_1, phase_rot_sheer_2_2,
PIIR_filt_IQ_transform_1_1, PIIR_filt_IQ_transform_1_2, PIIR_filt_IQ_transform_2_1,
PIIR_filt_IQ_transform_2_2, PIIR_filt_num_RY_1, PIIR_filt_num_IY_1, PIIR_filt_num_RZ_1,
PIIR_filt_num_RZ_2, PIIR_filt_num_IZ_1, PIIR_filt_num_IZ_2, PIIR_filt_den_2,
PIIR_filt_I_temp, PIIR_filt_I, PIIR_filt_I_temp_z_1, PIIR_filt_I_temp_z_2,
PIIR_filt_I_temp_z_3, PIIR_filt_Q_temp, PIIR_filt_Q, PIIR_filt_Q_temp_z_1,
PIIR_filt_Q_temp_z_2, PIIR_filt_Q_temp_z_3, PIIR_filt_mag_sq, PIIR_filt_phase_err,
PIIR_theta_out, PIIR_cos_out, PIIR_frequency;
#endif

#ifdef PIIR_PLL_Variable
float PIIR_PLL_Variable_integrator_z_1[6] ={0, 0, 0, 0, 0, 0};
float PIIR_PLL_Variable_integrator_z_2[6] = {0, 0, 0, 0, 0, 0};
float PIIR_PLL_Variable_integrator_z_3[6] = {0, 0, 0, 0, 0, 0};
float PIIR_PLL_Variable_integrator_z_4[6] = {0, 0, 0, 0, 0, 0};
float PIIR_PLL_Variable_integrator_in[6] = {0, 0, 0, 0, 0, 0};
float PIIR_PLL_Variable_integrator_out[6] = {0, 0, 0, 0, 0, 0};
float PIIR_PLL_Variable_Err_Filtered = 0;
float PIIR_PLL_Variable_Filt_Err_Q = 10;
float PIIR_PLL_Variable_omega;
float PIIR_Var_filt_t_s_1_int_prev = 5500;
float PIIR_PLL_Variable_Har_1_Filtered = 0;
float PIIR_PLL_Variable_Har_2_Filtered = 0;
float PIIR_PLL_Variable_Filt_Har_Q = 55;
float PIIR_Var_filt_x_pre;
// tau = 3e-3
float PIIR_Var_filt_I_b_0 = 0.0655556;
float PIIR_Var_filt_I_b_1 = -0.0644126;
float PIIR_Var_filt_I_a_1 = -1.93238;
float PIIR_Var_filt_I_a_2 = 0.934444;
float PIIR_Var_filt_Q_b_0 = -0.0353561;
float PIIR_Var_filt_Q_b_1 = 0.0373978;
float PIIR_Var_filt_Q_a_1 = -1.93238;
float PIIR_Var_filt_Q_a_2 = 0.934444;
float PIIR_Var_filt_G = 41.94304*0.6*5;  // Magnitude correction ((2048^2)*1e-5)
//============================

float PIIR_Var_filt_x = 0;
float PIIR_Var_filt_x_z_1 = 0;
float PIIR_Var_filt_I_y = 0;
float PIIR_Var_filt_I_y_z_1 = 0;
float PIIR_Var_filt_I_y_z_2 = 0;
float PIIR_Var_filt_Q_y = 0;
float PIIR_Var_filt_Q_y_z_1 = 0;
```

```
float PIIR_Var_filt_Q_y_z_2 = 0;
float PIIR_Var_filt_t_s   = 4000;
float PIIR_Var_filt_t_s_1 = 0;
unsigned int PIIR_Var_filt_t_s_1_int = 5500;
float PIIR_Var_theta_out, PIIR_Var_frequency, PIIR_Var_cos_out,
PIIR_Var_theta_out_interpolated;
unsigned int PLL_Feedback_EN_counter = 0;
char PLL_Feedback_EN = 0;
float PIIR_Var_Phase_Error;
float PIIR_phase_gen_sample;
float PIIR_Var_filt_I_mag;
unsigned int test_0, test_1, test_2;
unsigned int test_0_old;
float test_delta;
#endif

//=====================================//
//          Debug Variables
//=====================================//
int debug_counter = 0;
short PLL_data[5][PLL_num_samples];
double theta_gen;
double f_gen = 50;
double v_mag = 1;
double phase_gen;
double phase_offset_gen = 0;
double cos_gen;
double delta_theta;
double f_gen_delta = 5;
double phase_delta = 40*(2*pi/360);
double v_mag_sag = 0.7;
double V_distortion_2 = 1;   // In percent
double V_distortion_3 = 7.5;
double V_distortion_5 = 3;
double V_distortion_7 = 2;
double V_distortion_9 = 1;

//=====================================//
//          Functions
//=====================================//
void clear_text(int clear_size);
void sciDisplayText(sciBASE_t *sci, char *text,uint32 length);
void loadDataPattern(uint32 psize, uint16* pptr);
void dmaConfigCtrlTxPacket(uint32 sadd,uint32 dadd,uint32 dsize);
void dmaConfigCtrlRxPacket(uint32 sadd,uint32 dadd,uint32 dsize);

void main(void)
{
  int i, j;
  gioInit();
  sciInit();
  for(i=0;i<5;i++){
    for(j=0;j<PLL_num_samples;j++){
      PLL_data[i][j] = 0;
    }
  }
```

```
  srand (123);
  adcInit();
  adcEnableNotification(adcREG1, adcGROUP1);
  rtiInit();
  rtiEnableNotification(rtiNOTIFICATION_COMPARE0);
  rtiEnableNotification(rtiNOTIFICATION_COMPARE1);
  _enable_IRQ();
  adcStartConversion(adcREG1, adcGROUP1);
  dmaEnable();
  dmaEnableInterrupt(DMA_CH0, BTC);  // Tx
  dmaReqAssign(DMA_CH0,29);  // Tx
  DMA_Comp_Flag = 0xAAAA5555;
  clear_text(60);
  sprintf(text_out, "PLL Analysis\n\r");
  dmaConfigCtrlTxPacket((uint32)(&text_out), (uint32)(&(scilinREG->TD)), 60);
  dmaSetCtrlPacket(DMA_CH0,g_dmaCTRLPKT_Tx);
  dmaSetChEnable(DMA_CH0, DMA_HW);
  scilinREG->SETINT = (1 << 16);  // Tx
  rtiStartCounter(rtiCOUNTER_BLOCK0);
  rtiStartCounter(rtiCOUNTER_BLOCK1);
  while(1){
  }
}


void rtiNotification(uint32 notification){
if(notification == 1){

//=========================================================================
//       PLL Test Code
//=========================================================================
#ifdef PIIR_PLL_Variable
  test_0 = rtiREG1->CNT[1U].FRCx;
#endif
#ifdef Freq_Test
  if(debug_counter == 8000){
    f_gen = f_gen+f_gen_delta;
  }
#endif
#ifdef Phase_Test
  if(debug_counter == 8000){
    phase_offset_gen = phase_offset_gen+phase_delta;
  }
#endif
#ifdef Voltage_Sag_Test
  if(debug_counter == 8000){
    v_mag = v_mag_sag;
  }
#endif
#if !defined(PIIR_PLL_Variable)
  delta_theta = pi_2*f_gen*PLL_ts;
#endif
#ifdef PIIR_PLL_Variable
  test_delta = test_0-test_0_old;
  test_0_old = test_0;
  delta_theta = pi_2*f_gen*0.000000018181818*test_delta;
```

```
  if (debug_counter == 1){
    delta_theta = 0;
  }
#endif
  theta_gen = theta_gen + delta_theta;
  if (theta_gen>pi_2){
    theta_gen = theta_gen - pi_2;
  }
  phase_gen = theta_gen + phase_offset_gen;
  if (phase_gen>pi_2){
    phase_gen  = phase_gen - pi_2;
  }
  cos_gen = v_mag*cos(phase_gen);
#ifdef Harmonic_Test
  cos_gen = cos_gen + 0.01*V_distortion_2*cos(2*theta_gen +
phase_offset_gen)+0.01*V_distortion_3*cos(3*theta_gen +
phase_offset_gen)+0.01*V_distortion_5*cos(5*theta_gen +
phase_offset_gen)+0.01*V_distortion_7*cos(7*theta_gen +
phase_offset_gen)+0.01*V_distortion_9*cos(9*theta_gen + phase_offset_gen);
#endif
#ifdef Harmonic_Test_Clipped
  if (cos_gen>0.7){
    cos_gen=0.7;
  }
  if (cos_gen<-0.7){
    cos_gen=-0.7;
  }
#endif
#ifdef Harmonic_Test_White_Noise
  random_number = rand();
  random_number = random_number/32767;
  cos_gen = cos_gen + random_number*0.2 - 0.1;
#endif
#ifdef Harmonic_Test_DC
  cos_gen = cos_gen + DC_shift;
#endif

#ifdef SOGI_PLL
//=====================================================================
//        SOGI PLL
//=====================================================================
  SOGI_integrator_out[0] = SOGI_integrator_z_1[0]*23 - SOGI_integrator_z_2[0]*16 +
SOGI_integrator_z_3[0]*5;
  SOGI_integrator_out[2] = SOGI_integrator_z_1[2]*23 - SOGI_integrator_z_2[2]*16 +
SOGI_integrator_z_3[2]*5;
  SOGI_integrator_out[3] = SOGI_integrator_z_1[3]*23 - SOGI_integrator_z_2[3]*16 +
SOGI_integrator_z_3[3]*5;

  //=====
  // VCO
  //=====
  SOGI_integrator_out[1] = (SOGI_integrator_z_1[1]*23 - SOGI_integrator_z_2[1]*16 +
SOGI_integrator_z_3[1]*5 + SOGI_integrator_z_4[1]);
if (SOGI_integrator_out[1]>pi_2){
  SOGI_integrator_out[1]  = SOGI_integrator_out[1] - pi_2;
}
```

```
  //=====
  SOGI_in = cos_gen;
  SOGI_theta_out = SOGI_integrator_out[1];
  SOGI_cos_out = cos(SOGI_theta_out);
  SOGI_Q = -SOGI_integrator_out[3]*sin(SOGI_theta_out) +
SOGI_integrator_out[2]*SOGI_cos_out;
  SOGI_PI_out = 137.5*SOGI_Q + SOGI_integrator_out[0];
  SOGI_omega = SOGI_PI_out + two_pi_50;
  SOGI_integrator_in[0] = 7878*SOGI_Q;
  SOGI_integrator_in[1] = SOGI_omega;
  SOGI_integrator_in[2] = SOGI_integrator_out[3]*SOGI_omega;
  SOGI_integrator_in[3] = ((SOGI_in - SOGI_integrator_out[3])*2.1 -
SOGI_integrator_out[2])*SOGI_omega;
  SOGI_integrator_z_3[0] = SOGI_integrator_z_2[0];
  SOGI_integrator_z_2[0] = SOGI_integrator_z_1[0];
  SOGI_integrator_z_1[0] = SOGI_integrator_z_1[0] +
SOGI_integrator_in[0]*0.000008333333333;
  SOGI_integrator_z_3[2] = SOGI_integrator_z_2[2];
  SOGI_integrator_z_2[2] = SOGI_integrator_z_1[2];
  SOGI_integrator_z_1[2] = SOGI_integrator_z_1[2] +
SOGI_integrator_in[2]*0.000008333333333;
  SOGI_integrator_z_3[3] = SOGI_integrator_z_2[3];
  SOGI_integrator_z_2[3] = SOGI_integrator_z_1[3];
  SOGI_integrator_z_1[3] = SOGI_integrator_z_1[3] +
SOGI_integrator_in[3]*0.000008333333333;
  //==============================
  //           -VCO-
  // (Integrator with 2*pi reset)
  //==============================
  SOGI_integrator_z_4[1] = SOGI_integrator_out[1];
  SOGI_integrator_z_3[1] = SOGI_integrator_z_2[1];
  SOGI_integrator_z_2[1] = SOGI_integrator_z_1[1];
  SOGI_integrator_z_1[1] = SOGI_integrator_in[1]*0.000008333333333;
  //==============================
  SOGI_frequency = SOGI_omega*one_pi_2;
  PLL_data[1][debug_counter] = (double) SOGI_cos_out*21800;
  PLL_data[3][debug_counter] = (double) (SOGI_theta_out-pi)*10082;
  PLL_data[4][debug_counter] = (double) SOGI_frequency*252;
#endif

#ifdef SOGI_Notch_PLL
//=========================================================================
//       SOGI Notch PLL - A
//=========================================================================
  SOGI_Notch_integrator_out[0] = SOGI_Notch_integrator_z_1[0]*23 -
SOGI_Notch_integrator_z_2[0]*16 + SOGI_Notch_integrator_z_3[0]*5;
  SOGI_Notch_integrator_out[2] = SOGI_Notch_integrator_z_1[2]*23 -
SOGI_Notch_integrator_z_2[2]*16 + SOGI_Notch_integrator_z_3[2]*5;
  SOGI_Notch_integrator_out[3] = SOGI_Notch_integrator_z_1[3]*23 -
SOGI_Notch_integrator_z_2[3]*16 + SOGI_Notch_integrator_z_3[3]*5;
  SOGI_Notch_integrator_out[4] = SOGI_Notch_integrator_z_1[4]*23 -
SOGI_Notch_integrator_z_2[4]*16 + SOGI_Notch_integrator_z_3[4]*5;
  SOGI_Notch_integrator_out[5] = SOGI_Notch_integrator_z_1[5]*23 -
SOGI_Notch_integrator_z_2[5]*16 + SOGI_Notch_integrator_z_3[5]*5;
```

```
  //=====
  // VCO
  //=====
  SOGI_Notch_integrator_out[1] =     (SOGI_Notch_integrator_z_1[1]*23 -
SOGI_Notch_integrator_z_2[1]*16 + SOGI_Notch_integrator_z_3[1]*5 +
SOGI_Notch_integrator_z_4[1]);
  if (SOGI_Notch_integrator_out[1]>pi_2){
    SOGI_Notch_integrator_out[1]  = SOGI_Notch_integrator_out[1] - pi_2;
  }
  //=====

  SOGI_Notch_in = cos_gen;
  SOGI_Notch_theta_out = SOGI_Notch_integrator_out[1];
  SOGI_Notch_Q = -SOGI_Notch_integrator_out[3]*sin(SOGI_Notch_theta_out) +
SOGI_Notch_integrator_out[2]*cos(SOGI_Notch_theta_out);
  SOGI_Notch_Q_Filtered = SOGI_Notch_Q - SOGI_Notch_integrator_out[4];
  SOGI_Notch_PI_out = SOGI_Notch_kp*SOGI_Notch_Q_Filtered +
SOGI_Notch_integrator_out[0];
  SOGI_Notch_omega = SOGI_Notch_PI_out + two_pi_50;
  SOGI_Notch_integrator_in[0] = SOGI_Notch_ki*SOGI_Notch_Q_Filtered;
  SOGI_Notch_integrator_in[1] = SOGI_Notch_omega;
  SOGI_Notch_integrator_in[2] = SOGI_Notch_integrator_out[3]*SOGI_Notch_omega;
  SOGI_Notch_integrator_in[3] = ((SOGI_Notch_in -
SOGI_Notch_integrator_out[3])*SOGI_Notch_k -
SOGI_Notch_integrator_out[2])*SOGI_Notch_omega;
  SOGI_Notch_integrator_in[4] = SOGI_Notch_omega*2*((SOGI_Notch_Q-
SOGI_Notch_integrator_out[4])*(1/SOGI_Notch_Filt_Q)-SOGI_Notch_integrator_out[5]);
  SOGI_Notch_integrator_in[5] = SOGI_Notch_omega*2*SOGI_Notch_integrator_out[4];
  SOGI_Notch_integrator_z_3[0] = SOGI_Notch_integrator_z_2[0];
  SOGI_Notch_integrator_z_2[0] = SOGI_Notch_integrator_z_1[0];
  SOGI_Notch_integrator_z_1[0] = SOGI_Notch_integrator_z_1[0] +
SOGI_Notch_integrator_in[0]*0.000008333333333;
  SOGI_Notch_integrator_z_3[2] = SOGI_Notch_integrator_z_2[2];
  SOGI_Notch_integrator_z_2[2] = SOGI_Notch_integrator_z_1[2];
  SOGI_Notch_integrator_z_1[2] = SOGI_Notch_integrator_z_1[2] +
SOGI_Notch_integrator_in[2]*0.000008333333333;
  SOGI_Notch_integrator_z_3[3] = SOGI_Notch_integrator_z_2[3];
  SOGI_Notch_integrator_z_2[3] = SOGI_Notch_integrator_z_1[3];
  SOGI_Notch_integrator_z_1[3] = SOGI_Notch_integrator_z_1[3] +
SOGI_Notch_integrator_in[3]*0.000008333333333;
  SOGI_Notch_integrator_z_3[4] = SOGI_Notch_integrator_z_2[4];
  SOGI_Notch_integrator_z_2[4] = SOGI_Notch_integrator_z_1[4];
  SOGI_Notch_integrator_z_1[4] = SOGI_Notch_integrator_z_1[4] +
SOGI_Notch_integrator_in[4]*0.000008333333333;
  SOGI_Notch_integrator_z_3[5] = SOGI_Notch_integrator_z_2[5];
  SOGI_Notch_integrator_z_2[5] = SOGI_Notch_integrator_z_1[5];
  SOGI_Notch_integrator_z_1[5] = SOGI_Notch_integrator_z_1[5] +
SOGI_Notch_integrator_in[5]*0.000008333333333;

  //============================
  //          -VCO-
  // (Integrator with 2*pi reset)
  //============================
  SOGI_Notch_integrator_z_4[1] = SOGI_Notch_integrator_out[1];
  SOGI_Notch_integrator_z_3[1] = SOGI_Notch_integrator_z_2[1];
  SOGI_Notch_integrator_z_2[1] = SOGI_Notch_integrator_z_1[1];
```

```
  SOGI_Notch_integrator_z_1[1] = SOGI_Notch_integrator_in[1]*0.000008333333333;
  //============================

  SOGI_Notch_cos_out = cos(SOGI_Notch_theta_out);
  SOGI_Notch_frequency = SOGI_Notch_omega*one_pi_2;
  PLL_data[1][debug_counter] = (double) SOGI_Notch_cos_out*21800;
  PLL_data[3][debug_counter] = (double) (SOGI_Notch_theta_out-pi)*10082;
  PLL_data[4][debug_counter] = (double) SOGI_Notch_frequency*252;
#endif

#ifdef SOGI_Notch_B_PLL
//=====================================================================
//       SOGI Notch PLL - B
//=====================================================================
  SOGI_Notch_B_integrator_out[0] = SOGI_Notch_B_integrator_z_1[0]*23 -
SOGI_Notch_B_integrator_z_2[0]*16 + SOGI_Notch_B_integrator_z_3[0]*5;
  SOGI_Notch_B_integrator_out[2] = SOGI_Notch_B_integrator_z_1[2]*23 -
SOGI_Notch_B_integrator_z_2[2]*16 + SOGI_Notch_B_integrator_z_3[2]*5;
  SOGI_Notch_B_integrator_out[3] = SOGI_Notch_B_integrator_z_1[3]*23 -
SOGI_Notch_B_integrator_z_2[3]*16 + SOGI_Notch_B_integrator_z_3[3]*5;
  SOGI_Notch_B_integrator_out[4] = SOGI_Notch_B_integrator_z_1[4]*23 -
SOGI_Notch_B_integrator_z_2[4]*16 + SOGI_Notch_B_integrator_z_3[4]*5;
  SOGI_Notch_B_integrator_out[5] = SOGI_Notch_B_integrator_z_1[5]*23 -
SOGI_Notch_B_integrator_z_2[5]*16 + SOGI_Notch_B_integrator_z_3[5]*5;

  //=====
  // VCO
  //=====
  SOGI_Notch_B_integrator_out[1] =     (SOGI_Notch_B_integrator_z_1[1]*23 -
SOGI_Notch_B_integrator_z_2[1]*16 + SOGI_Notch_B_integrator_z_3[1]*5 +
SOGI_Notch_B_integrator_z_4[1]);
  if (SOGI_Notch_B_integrator_out[1]>pi_2){
    SOGI_Notch_B_integrator_out[1]  = SOGI_Notch_B_integrator_out[1] - pi_2;
  }
  //=====

  SOGI_Notch_B_in = cos_gen;
  SOGI_Notch_B_theta_out = SOGI_Notch_B_integrator_out[1];
  SOGI_Notch_B_Q = -SOGI_Notch_B_integrator_out[3]*sin(SOGI_Notch_B_theta_out) +
SOGI_Notch_B_integrator_out[2]*cos(SOGI_Notch_B_theta_out);
  SOGI_Notch_B_Q_Filtered = SOGI_Notch_B_in - SOGI_Notch_B_integrator_out[4];
  SOGI_Notch_B_PI_out = SOGI_Notch_B_kp* SOGI_Notch_B_Q +
SOGI_Notch_B_integrator_out[0];
  SOGI_Notch_B_omega = SOGI_Notch_B_PI_out + two_pi_50;
  SOGI_Notch_B_integrator_in[0] = SOGI_Notch_B_ki* SOGI_Notch_B_Q;
  SOGI_Notch_B_integrator_in[1] = SOGI_Notch_B_omega;
  SOGI_Notch_B_integrator_in[2] =
SOGI_Notch_B_integrator_out[3]*SOGI_Notch_B_omega;
  SOGI_Notch_B_integrator_in[3] = ((SOGI_Notch_B_Q_Filtered -
SOGI_Notch_B_integrator_out[3])*SOGI_Notch_B_k -
SOGI_Notch_B_integrator_out[2])*SOGI_Notch_B_omega;
  SOGI_Notch_B_integrator_in[4] = SOGI_Notch_B_omega*3*((SOGI_Notch_B_in-
SOGI_Notch_B_integrator_out[4])*(1/SOGI_Notch_B_Filt_Q)-
SOGI_Notch_B_integrator_out[5]);
  SOGI_Notch_B_integrator_in[5] =
SOGI_Notch_B_omega*3*SOGI_Notch_B_integrator_out[4];
```

```
  SOGI_Notch_B_integrator_z_3[0] = SOGI_Notch_B_integrator_z_2[0];
  SOGI_Notch_B_integrator_z_2[0] = SOGI_Notch_B_integrator_z_1[0];
  SOGI_Notch_B_integrator_z_1[0] = SOGI_Notch_B_integrator_z_1[0] +
SOGI_Notch_B_integrator_in[0]*0.000008333333333;
  SOGI_Notch_B_integrator_z_3[2] = SOGI_Notch_B_integrator_z_2[2];
  SOGI_Notch_B_integrator_z_2[2] = SOGI_Notch_B_integrator_z_1[2];
  SOGI_Notch_B_integrator_z_1[2] = SOGI_Notch_B_integrator_z_1[2] +
SOGI_Notch_B_integrator_in[2]*0.000008333333333;
  SOGI_Notch_B_integrator_z_3[3] = SOGI_Notch_B_integrator_z_2[3];
  SOGI_Notch_B_integrator_z_2[3] = SOGI_Notch_B_integrator_z_1[3];
  SOGI_Notch_B_integrator_z_1[3] = SOGI_Notch_B_integrator_z_1[3] +
SOGI_Notch_B_integrator_in[3]*0.000008333333333;
  SOGI_Notch_B_integrator_z_3[4] = SOGI_Notch_B_integrator_z_2[4];
  SOGI_Notch_B_integrator_z_2[4] = SOGI_Notch_B_integrator_z_1[4];
  SOGI_Notch_B_integrator_z_1[4] = SOGI_Notch_B_integrator_z_1[4] +
SOGI_Notch_B_integrator_in[4]*0.000008333333333;
  SOGI_Notch_B_integrator_z_3[5] = SOGI_Notch_B_integrator_z_2[5];
  SOGI_Notch_B_integrator_z_2[5] = SOGI_Notch_B_integrator_z_1[5];
  SOGI_Notch_B_integrator_z_1[5] = SOGI_Notch_B_integrator_z_1[5] +
SOGI_Notch_B_integrator_in[5]*0.000008333333333;
  //==============================
  //          -VCO-
  // (Integrator with 2*pi reset)
  //==============================
  SOGI_Notch_B_integrator_z_4[1] = SOGI_Notch_B_integrator_out[1];
  SOGI_Notch_B_integrator_z_3[1] = SOGI_Notch_B_integrator_z_2[1];
  SOGI_Notch_B_integrator_z_2[1] = SOGI_Notch_B_integrator_z_1[1];
  SOGI_Notch_B_integrator_z_1[1] = SOGI_Notch_B_integrator_in[1]*0.000008333333333;
  //==============================

  SOGI_Notch_B_cos_out = cos(SOGI_Notch_B_theta_out+0.006806784083);
  SOGI_Notch_B_frequency = SOGI_Notch_B_omega*one_pi_2;
  PLL_data[1][debug_counter] = (double) SOGI_Notch_B_cos_out*21800;
  PLL_data[3][debug_counter] = (double) (SOGI_Notch_B_theta_out+0.006806784083-
pi)*10082;
  PLL_data[4][debug_counter] = (double) SOGI_Notch_B_frequency*252;
#endif

#ifdef PIIR_PLL
//=====================================================================
//       PIIR PLL
//=====================================================================
  PIIR_in = cos_gen;
  sin_delta = sin(PIIR_filt_delta);
  cos_delta = cos(PIIR_filt_delta);
  PIIR_filt_a_b = 0.02/(sqrt(0.0004+3.92*sin_delta*sin_delta));
  PIIR_filt_phi_f = PIIR_filt_delta;
  PIIR_filt_phi_b = atan2(99*(sin_delta/cos_delta), 1);
  PIIR_filt_alpha = 0.5*(PIIR_filt_phi_f - PIIR_filt_phi_b);
  PIIR_filt_beta  = 0.5*(PIIR_filt_phi_f + PIIR_filt_phi_b);
  sin_alpha = sin(PIIR_filt_alpha);
  sin_beta  = sin(PIIR_filt_beta);
  cos_alpha = cos(PIIR_filt_alpha);
  cos_beta  = cos(PIIR_filt_beta);
  phase_rot_sheer_1_1 = (cos_alpha*(2/(1+PIIR_filt_a_b)));
  phase_rot_sheer_1_2 = (sin_alpha*(2/(1-PIIR_filt_a_b)));
```

```
  phase_rot_sheer_2_1 = -(sin_alpha*(2/(1+PIIR_filt_a_b)));
  phase_rot_sheer_2_2 = (cos_alpha*(2/(1-PIIR_filt_a_b)));
  PIIR_filt_IQ_transform_1_1 = (phase_rot_sheer_1_1*cos_beta -
phase_rot_sheer_1_2*sin_beta);
  PIIR_filt_IQ_transform_1_2 = (phase_rot_sheer_1_1*sin_beta +
phase_rot_sheer_1_2*cos_beta);
  PIIR_filt_IQ_transform_2_1 = (phase_rot_sheer_2_1*cos_beta -
phase_rot_sheer_2_2*sin_beta);
  PIIR_filt_IQ_transform_2_2 = (phase_rot_sheer_2_1*sin_beta +
phase_rot_sheer_2_2*cos_beta);
  PIIR_filt_num_RY_1 = 0.02*cos_delta;
  PIIR_filt_num_IY_1 = 0.02*sin_delta;
  PIIR_filt_num_RZ_1 = PIIR_filt_IQ_transform_1_1*PIIR_filt_num_RY_1 +
PIIR_filt_IQ_transform_1_2*PIIR_filt_num_IY_1;
  PIIR_filt_num_RZ_2 = -PIIR_filt_IQ_transform_1_1*0.0196;
  PIIR_filt_num_IZ_1 =
PIIR_filt_IQ_transform_2_1*PIIR_filt_num_RY_1+PIIR_filt_IQ_transform_2_2*PIIR_filt_num
_IY_1;
  PIIR_filt_num_IZ_2 = -PIIR_filt_IQ_transform_2_1*0.0196;
  PIIR_filt_den_2 = -2*(cos_delta - PIIR_filt_num_RY_1);
  //     IIR for in-phase signal
  PIIR_filt_I_temp = (PIIR_in - PIIR_filt_den_2*PIIR_filt_I_temp_z_1 -
0.9604*PIIR_filt_I_temp_z_2);
  PIIR_filt_I = PIIR_filt_num_RZ_1*PIIR_filt_I_temp +
PIIR_filt_num_RZ_2*PIIR_filt_I_temp_z_1;
  PIIR_filt_I_temp_z_3 = PIIR_filt_I_temp_z_2;
  PIIR_filt_I_temp_z_2 = PIIR_filt_I_temp_z_1;
  PIIR_filt_I_temp_z_1 = PIIR_filt_I_temp;

  //     IIR for quadrature signal
  PIIR_filt_Q_temp = (PIIR_in - PIIR_filt_den_2*PIIR_filt_Q_temp_z_1 -
0.9604*PIIR_filt_Q_temp_z_2);
  PIIR_filt_Q = PIIR_filt_num_IZ_1*PIIR_filt_Q_temp +
PIIR_filt_num_IZ_2*PIIR_filt_Q_temp_z_1;
  PIIR_filt_Q_temp_z_3 = PIIR_filt_Q_temp_z_2;
  PIIR_filt_Q_temp_z_2 = PIIR_filt_Q_temp_z_1;
  PIIR_filt_Q_temp_z_1 = PIIR_filt_Q_temp;
  PIIR_filt_mag_sq = PIIR_filt_I*PIIR_filt_I + PIIR_filt_Q*PIIR_filt_Q;
  PIIR_filt_phase_err = PIIR_filt_I*PIIR_filt_Q - PIIR_in*PIIR_filt_Q;
  PIIR_filt_delta = PIIR_filt_delta + ((PIIR_filt_phase_err/PIIR_filt_mag_sq)*0.00027);
  PIIR_theta_out = pi-atan2(PIIR_filt_Q, -PIIR_filt_I);
  PIIR_cos_out = cos(PIIR_theta_out);
  PIIR_frequency = (PIIR_filt_delta)*(1591.549430918953);
  PLL_data[1][debug_counter] = (double) PIIR_cos_out*21800;
  PLL_data[3][debug_counter] = (double) (PIIR_theta_out-pi)*10082;
  PLL_data[4][debug_counter] = (double) PIIR_frequency*252;
#endif

#ifdef PIIR_PLL_Variable
//=====================================================================
//       PIIR Variable Sampling Time PLL (Enhanced PIIR PLL)
//=====================================================================
 PIIR_PLL_Variable_integrator_out[0] = PIIR_PLL_Variable_integrator_z_1[0]*23 -
PIIR_PLL_Variable_integrator_z_2[0]*16 + PIIR_PLL_Variable_integrator_z_3[0]*5;
 PIIR_PLL_Variable_integrator_out[1] = PIIR_PLL_Variable_integrator_z_1[1]*23 -
PIIR_PLL_Variable_integrator_z_2[1]*16 + PIIR_PLL_Variable_integrator_z_3[1]*5;
```

```
 PIIR_PLL_Variable_integrator_out[2] = PIIR_PLL_Variable_integrator_z_1[2]*23 -
PIIR_PLL_Variable_integrator_z_2[2]*16 + PIIR_PLL_Variable_integrator_z_3[2]*5;
 PIIR_PLL_Variable_integrator_out[3] = PIIR_PLL_Variable_integrator_z_1[3]*23 -
PIIR_PLL_Variable_integrator_z_2[3]*16 + PIIR_PLL_Variable_integrator_z_3[3]*5;
 PIIR_PLL_Variable_integrator_out[4] = PIIR_PLL_Variable_integrator_z_1[4]*23 -
PIIR_PLL_Variable_integrator_z_2[4]*16 + PIIR_PLL_Variable_integrator_z_3[4]*5;
 PIIR_PLL_Variable_integrator_out[5] = PIIR_PLL_Variable_integrator_z_1[5]*23 -
PIIR_PLL_Variable_integrator_z_2[5]*16 + PIIR_PLL_Variable_integrator_z_3[5]*5;
PIIR_Var_filt_x_pre = cos_gen;
PIIR_PLL_Variable_Har_1_Filtered = PIIR_Var_filt_x_pre -
PIIR_PLL_Variable_integrator_out[0];
PIIR_PLL_Variable_Har_2_Filtered = PIIR_PLL_Variable_Har_1_Filtered -
PIIR_PLL_Variable_integrator_out[2];
PIIR_Var_filt_x = PIIR_PLL_Variable_Har_2_Filtered;
PIIR_Var_filt_I_y = PIIR_Var_filt_I_b_0*PIIR_Var_filt_x +
PIIR_Var_filt_I_b_1*PIIR_Var_filt_x_z_1 - (PIIR_Var_filt_I_a_1*PIIR_Var_filt_I_y_z_1 +
PIIR_Var_filt_I_a_2*PIIR_Var_filt_I_y_z_2);
PIIR_Var_filt_Q_y = PIIR_Var_filt_Q_b_0*PIIR_Var_filt_x +
PIIR_Var_filt_Q_b_1*PIIR_Var_filt_x_z_1 - (PIIR_Var_filt_Q_a_1*PIIR_Var_filt_Q_y_z_1 +
PIIR_Var_filt_Q_a_2*PIIR_Var_filt_Q_y_z_2);
PIIR_Var_filt_x_z_1 = PIIR_Var_filt_x;
PIIR_Var_filt_I_y_z_2 = PIIR_Var_filt_I_y_z_1;
PIIR_Var_filt_I_y_z_1 = PIIR_Var_filt_I_y;
PIIR_Var_filt_Q_y_z_2 = PIIR_Var_filt_Q_y_z_1;
PIIR_Var_filt_Q_y_z_1 = PIIR_Var_filt_Q_y;
PIIR_Var_Phase_Error = ((PIIR_Var_filt_x*PIIR_Var_filt_Q_y -
PIIR_Var_filt_I_y*PIIR_Var_filt_Q_y)/(PIIR_Var_filt_I_y*PIIR_Var_filt_I_y+PIIR_Var_filt_Q_y
*PIIR_Var_filt_Q_y))*PIIR_Var_filt_G;
PIIR_PLL_Variable_Err_Filtered = PIIR_Var_Phase_Error -
PIIR_PLL_Variable_integrator_out[4];
PIIR_Var_filt_t_s_1 = PIIR_Var_filt_t_s + PIIR_PLL_Variable_Err_Filtered;
PIIR_Var_filt_t_s = PIIR_Var_filt_t_s_1;
PIIR_Var_theta_out = pi-atan2(PIIR_Var_filt_Q_y, -PIIR_Var_filt_I_y)+0.01095368639;  //
(0.6076+0.02)*(2*pi/360)

// Calculate next cycle's time
PIIR_Var_filt_t_s_1 = PIIR_Var_filt_t_s_1*1.375;    // 4000 ticks to 55MHz RTI clock
PIIR_Var_filt_t_s_1_int = PIIR_Var_filt_t_s_1;
  // - Setup compare 0 value. This value is compared with selected free running counter.
  rtiREG1->CMP[0U].COMPx = rtiREG1->CMP[0U].COMPx + (PIIR_Var_filt_t_s_1_int &
0xFFFFFFFF) - 5500;
  PIIR_PLL_Variable_omega = (1725824.4994/PIIR_Var_filt_t_s_1_int);  //
(275500/PIIR_Var_filt_t_s_1_int)*2*pi
  if (PIIR_PLL_Variable_omega>376.99111843){
    PIIR_PLL_Variable_omega=376.99111843;
  }
  if (PIIR_PLL_Variable_omega<251.32741229){
     PIIR_PLL_Variable_omega=251.32741229;
  }
  PIIR_PLL_Variable_integrator_in[0] = PIIR_PLL_Variable_omega*3*((PIIR_Var_filt_x_pre-
PIIR_PLL_Variable_integrator_out[0])*(1/PIIR_PLL_Variable_Filt_Har_Q)-
PIIR_PLL_Variable_integrator_out[1]);
  PIIR_PLL_Variable_integrator_in[1] =
PIIR_PLL_Variable_omega*3*PIIR_PLL_Variable_integrator_out[0];
  PIIR_PLL_Variable_integrator_in[2] =
PIIR_PLL_Variable_omega*5*((PIIR_PLL_Variable_Har_1_Filtered-
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PIIR_PLL_Variable_integrator_out[2])*(1/PIIR_PLL_Variable_Filt_Har_Q)-
PIIR_PLL_Variable_integrator_out[3]);
  PIIR_PLL_Variable_integrator_in[3] =
PIIR_PLL_Variable_omega*5*PIIR_PLL_Variable_integrator_out[2];
  PIIR_PLL_Variable_integrator_in[4] =
PIIR_PLL_Variable_omega*2*((PIIR_Var_Phase_Error-
PIIR_PLL_Variable_integrator_out[4])*(1/PIIR_PLL_Variable_Filt_Err_Q)-
PIIR_PLL_Variable_integrator_out[5]);
  PIIR_PLL_Variable_integrator_in[5] =
PIIR_PLL_Variable_omega*2*PIIR_PLL_Variable_integrator_out[4];
  PIIR_Var_filt_t_s_1_int_prev = (PIIR_Var_filt_t_s_1_int_prev/55000000)/12;
  PIIR_PLL_Variable_integrator_z_3[0] = PIIR_PLL_Variable_integrator_z_2[0];
  PIIR_PLL_Variable_integrator_z_2[0] = PIIR_PLL_Variable_integrator_z_1[0];
  PIIR_PLL_Variable_integrator_z_1[0] = PIIR_PLL_Variable_integrator_z_1[0] +
PIIR_PLL_Variable_integrator_in[0]*PIIR_Var_filt_t_s_1_int_prev;
  PIIR_PLL_Variable_integrator_z_3[1] = PIIR_PLL_Variable_integrator_z_2[1];
  PIIR_PLL_Variable_integrator_z_2[1] = PIIR_PLL_Variable_integrator_z_1[1];
  PIIR_PLL_Variable_integrator_z_1[1] = PIIR_PLL_Variable_integrator_z_1[1] +
PIIR_PLL_Variable_integrator_in[1]*PIIR_Var_filt_t_s_1_int_prev;
  PIIR_PLL_Variable_integrator_z_3[2] = PIIR_PLL_Variable_integrator_z_2[2];
  PIIR_PLL_Variable_integrator_z_2[2] = PIIR_PLL_Variable_integrator_z_1[2];
  PIIR_PLL_Variable_integrator_z_1[2] = PIIR_PLL_Variable_integrator_z_1[2] +
PIIR_PLL_Variable_integrator_in[2]*PIIR_Var_filt_t_s_1_int_prev;
  PIIR_PLL_Variable_integrator_z_3[3] = PIIR_PLL_Variable_integrator_z_2[3];
  PIIR_PLL_Variable_integrator_z_2[3] = PIIR_PLL_Variable_integrator_z_1[3];
  PIIR_PLL_Variable_integrator_z_1[3] = PIIR_PLL_Variable_integrator_z_1[3] +
PIIR_PLL_Variable_integrator_in[3]*PIIR_Var_filt_t_s_1_int_prev;
  PIIR_PLL_Variable_integrator_z_3[4] = PIIR_PLL_Variable_integrator_z_2[4];
  PIIR_PLL_Variable_integrator_z_2[4] = PIIR_PLL_Variable_integrator_z_1[4];
  PIIR_PLL_Variable_integrator_z_1[4] = PIIR_PLL_Variable_integrator_z_1[4] +
PIIR_PLL_Variable_integrator_in[4]*PIIR_Var_filt_t_s_1_int_prev;
  PIIR_PLL_Variable_integrator_z_3[5] = PIIR_PLL_Variable_integrator_z_2[5];
  PIIR_PLL_Variable_integrator_z_2[5] = PIIR_PLL_Variable_integrator_z_1[5];
  PIIR_PLL_Variable_integrator_z_1[5] = PIIR_PLL_Variable_integrator_z_1[5] +
PIIR_PLL_Variable_integrator_in[5]*PIIR_Var_filt_t_s_1_int_prev;
  PIIR_Var_filt_t_s_1_int_prev = PIIR_Var_filt_t_s_1_int;
}

if(notification == 2){
test_1 = rtiREG1->CNT[1U].FRCx;
PIIR_phase_gen_sample = PIIR_Var_filt_t_s_1_int;
PIIR_phase_gen_sample = 275500/PIIR_phase_gen_sample;
test_delta = test_1-test_0;
test_delta = PIIR_phase_gen_sample*0.000000114239733*test_delta;
PIIR_Var_theta_out_interpolated = PIIR_Var_theta_out + test_delta;
PIIR_Var_cos_out = cos(PIIR_Var_theta_out_interpolated);
test_delta = test_1-test_0;
test_delta = pi_2*f_gen*0.000000018181818*test_delta;
PIIR_phase_gen_sample = phase_gen + test_delta;
cos_gen = v_mag*cos(PIIR_phase_gen_sample);

#ifdef Harmonic_Test
  cos_gen = cos_gen + 0.01*V_distortion_2*cos(2*PIIR_phase_gen_sample +
phase_offset_gen)+0.01*V_distortion_3*cos(3*PIIR_phase_gen_sample +
phase_offset_gen)+0.01*V_distortion_5*cos(5*PIIR_phase_gen_sample +
phase_offset_gen)+0.01*V_distortion_7*cos(7*PIIR_phase_gen_sample +
```
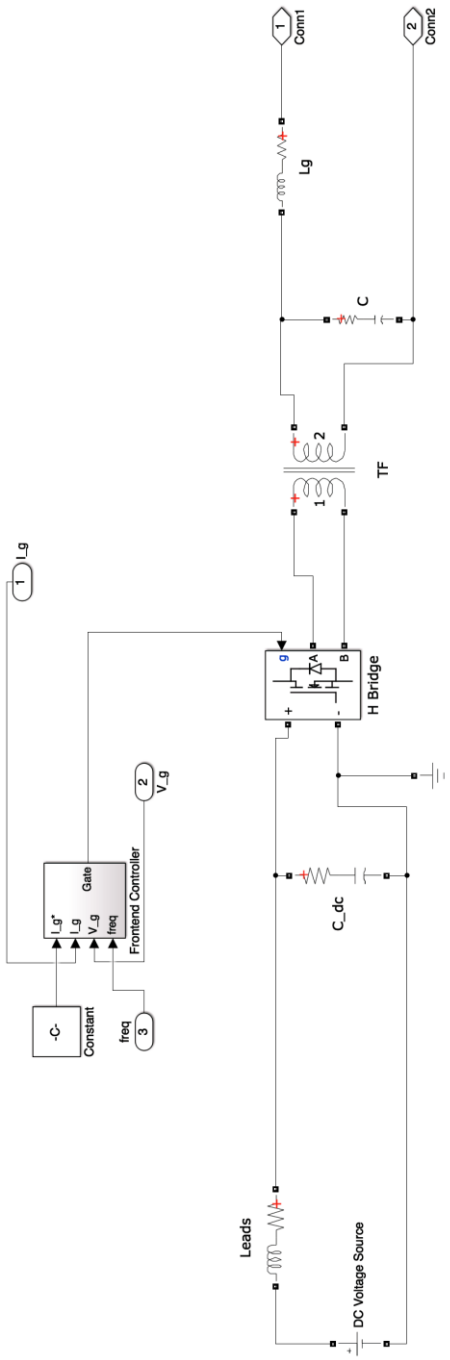

```
phase_offset_gen)+0.01*V_distortion_9*cos(9*PIIR_phase_gen_sample +
phase_offset_gen);
#endif

#ifdef Harmonic_Test_Clipped
  if (cos_gen>0.7){
    cos_gen=0.7;
  }
  if (cos_gen<-0.7){
    cos_gen=-0.7;
  }
#endif

#ifdef Harmonic_Test_White_Noise
  cos_gen = cos_gen + random_number*0.2 - 0.1;
#endif

#ifdef Harmonic_Test_DC
  cos_gen = cos_gen + DC_shift;
#endif
PLL_data[0][debug_counter] = (double) cos_gen*21800;
PLL_data[1][debug_counter] = (double) PIIR_Var_cos_out*21800;
PLL_data[2][debug_counter] = (double) (PIIR_phase_gen_sample -pi)*10082;
PLL_data[3][debug_counter] = (double) (PIIR_Var_theta_out_interpolated-pi)*10082;
PLL_data[4][debug_counter] = PIIR_Var_filt_t_s_1_int;
#endif

debug_counter++;
  if(debug_counter == PLL_num_samples){
//=========================================================================
//       Send Serial
//=========================================================================
      if((DMA_Comp_Flag == 0x5555AAAA) && (Sent_Tx == 1)){
           DMA_Comp_Flag = 0xAAAA5555;
           clear_text(60);
           sprintf(text_out, "Done...\n\r");
           dmaSetChEnable(DMA_CH0, DMA_HW);
         }
    while(1){
    }
  }
}
}

void clear_text(int clear_size){
int i;
  for(i=0;i<clear_size;i++){
    text_out[i] = 0;
  }
}

void sciDisplayText(sciBASE_t *sci, char *text,uint32 length)
{
    while(length--)
    {
        while ((scilinREG->FLR & 0x4) == 4); /* wait until busy */
```

```
        sciSendByte(scilinREG,*text++);      /* send out text   */
    }
}

void dmaConfigCtrlTxPacket(uint32 sadd,uint32 dadd,uint32 dsize)
{
 g_dmaCTRLPKT_Tx.SADD      = sadd;
 /* source address           */
 g_dmaCTRLPKT_Tx.DADD      = dadd;           /* destination  address      */
 g_dmaCTRLPKT_Tx.CHCTRL    = 0;              /* channel control           */
 g_dmaCTRLPKT_Tx.FRCNT     = dsize;          /* frame count               */
 g_dmaCTRLPKT_Tx.ELCNT     = 1;              /* element count             */
 g_dmaCTRLPKT_Tx.ELDOFFSET = 0;              /* element destination offset */
 g_dmaCTRLPKT_Tx.ELSOFFSET = 0;              /* element source offset */
 g_dmaCTRLPKT_Tx.FRDOFFSET = 0;              /* frame destination offset   */
 g_dmaCTRLPKT_Tx.FRSOFFSET = 0;              /* frame source offset   */
 g_dmaCTRLPKT_Tx.PORTASGN  = 4;              /* port b                    */
 g_dmaCTRLPKT_Tx.RDSIZE    = ACCESS_8_BIT;   /* read size                 */
 g_dmaCTRLPKT_Tx.WRSIZE    = ACCESS_8_BIT;   /* write size                */
 g_dmaCTRLPKT_Tx.TTYPE     = FRAME_TRANSFER ;  /* transfer type           */
 g_dmaCTRLPKT_Tx.ADDMODERD = ADDR_INC1;      /* address mode read         */
 g_dmaCTRLPKT_Tx.ADDMODEWR = ADDR_FIXED;     /* address mode write        */
 g_dmaCTRLPKT_Tx.AUTOINIT  = AUTOINIT_OFF;   /* autoinit                  */
}

void dmaConfigCtrlRxPacket(uint32 sadd,uint32 dadd,uint32 dsize)
{
 g_dmaCTRLPKT_Rx.SADD      = sadd;
 /* source address           */
 g_dmaCTRLPKT_Rx.DADD      = dadd;           /* destination  address      */
 g_dmaCTRLPKT_Rx.CHCTRL    = 0;              /* channel control           */
 g_dmaCTRLPKT_Rx.FRCNT     = dsize;          /* frame count               */
 g_dmaCTRLPKT_Rx.ELCNT     = 1;              /* element count             */
 g_dmaCTRLPKT_Rx.ELDOFFSET = 0;              /* element destination offset */
 g_dmaCTRLPKT_Rx.ELSOFFSET = 0;              /* element source offset */
 g_dmaCTRLPKT_Rx.FRDOFFSET = 0;              /* frame destination offset   */
 g_dmaCTRLPKT_Rx.FRSOFFSET = 0;              /* frame source offset   */
 g_dmaCTRLPKT_Rx.PORTASGN  = 4;              /* port b                    */
 g_dmaCTRLPKT_Rx.RDSIZE    = ACCESS_8_BIT;   /* read size                 */
 g_dmaCTRLPKT_Rx.WRSIZE    = ACCESS_8_BIT;   /* write size                */
 g_dmaCTRLPKT_Rx.TTYPE     = FRAME_TRANSFER ;  /* transfer type           */
 g_dmaCTRLPKT_Rx.ADDMODERD = ADDR_FIXED;     /* address mode read         */
 g_dmaCTRLPKT_Rx.ADDMODEWR = ADDR_INC1;      /* address mode write        */
 g_dmaCTRLPKT_Rx.AUTOINIT  = AUTOINIT_ON;    /* autoinit                  */
}

void loadDataPattern(uint32 psize, uint16* pptr)
{
  *pptr = 0xD0C0;
    while(psize--)
    {
      *pptr = 0x1111 + *pptr++;
    }
}
```

Appendices

Appendix E: Inverter 1 Simulink Diagram



Appendices

Appendix F: MATLAB Code of Islanding Detection Function

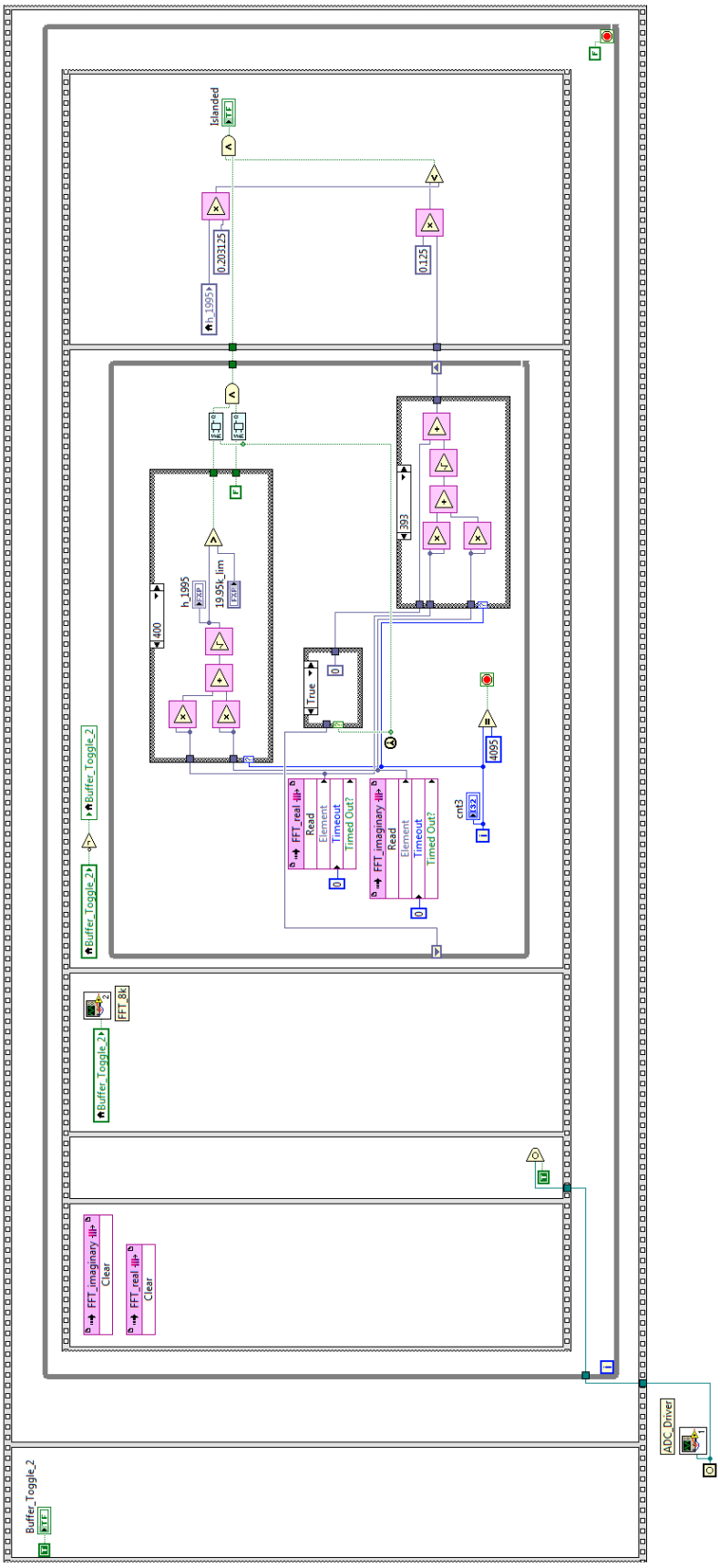
```
function [fft_out, islanded_out, freq] = fcn(t, V_in, M_)
coder.extrinsic('besselj');

global time_curr;
global data_in;
global index_1;
global Y_fft;
global fft_mag_V_fft;
global islanded;
global f_inv;
global f_index;

% Variable step time to 409.6 kSPS conversion (sample data)
f_s = 409600;
T_s = 1/f_s;
if (t >= T_s*(time_curr)) && (t <= T_s*(time_curr+1))
    time_curr = time_curr + 1;
    index_1 = index_1 + 1;
    data_in(index_1)= V_in;
end


% Compare V_PCC FFT every 0.02 seconds to threshold and check
% islanding
if index_1 == 8192  % Variable step time to 409.6 kSPS conversion
  f_h = [20000 21000 19000 22000 18000 23000 17000 24000 16000];
  f_h_current = f_h(f_index);

  % LUT generation (to do - run only once and save LUT)
  V_bat = 140;
  N = 4;
  V_dc = V_bat*N;
  f_20k_1 = f_h_current-50;
  w_20k_1 = 2*pi*f_20k_1;
  f_20k_2 = f_h_current+50;
  w_20k_2 = 2*pi*f_20k_2;
  L_filter = 5e-3;
  Lg_filter = 0.145e-3;
  C_filter = 6.8e-6;
  R_filter = 1.2;
  Zg = (0.1+1i*2*pi*f_h_current*20e-6);
  Z_bus = 0.5;
  jj=1;
  V_h_1_pre_max=zeros(101,1);
  V_h_2_pre_max=zeros(101,1);
  i_=zeros(101,1);
  for i=0:1e-2:1
    m = 1;
    n = 0;
    V_s_1 = abs(((4*V_dc/pi)*(1/(2*m))*(besselj((2*n-1),
m*pi*i))*(cos((m+n-1)*pi))));
    m = 1;
```

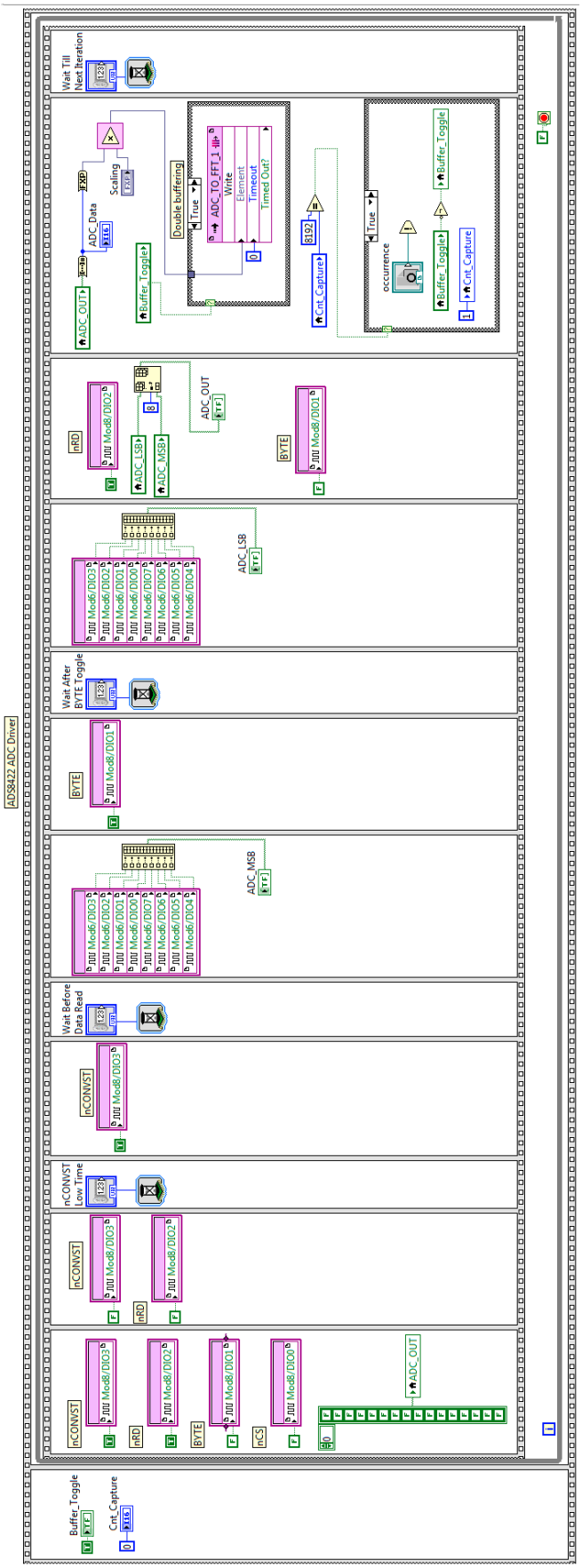
```
    n = 1;
    V_s_2 = abs(((4*V_dc/pi)*(1/(2*m))*(besselj((2*n-1),
m*pi*i))*(cos((m+n-1)*pi))));
    Z_20k_1_pre = Zg+Z_bus;
    Z_th_1 =
((1+1i*w_20k_1*R_filter*C_filter)/(1+1i*w_20k_1*R_filter*C_filter-
w_20k_1*w_20k_1*L_filter*C_filter));
    e_th_1 = (Z_th_1*V_s_1);
    X_th_1 =
((1i*w_20k_1*(L_filter*(1+1i*w_20k_1*R_filter*C_filter)+Lg_filter*(1
+1i*w_20k_1*R_filter*C_filter-
w_20k_1*w_20k_1*L_filter*C_filter)))/(1+1i*w_20k_1*R_filter*C_filter
-w_20k_1*w_20k_1*L_filter*C_filter));
    I_h_1_pre = abs((e_th_1)/(X_th_1+Z_20k_1_pre));
    V_h_1_pre = I_h_1_pre*abs(Z_20k_1_pre-Z_bus);
    V_h_1_pre_max(jj) = V_h_1_pre*1.05;
    Z_th_2 =
((1+1i*w_20k_2*R_filter*C_filter)/(1+1i*w_20k_2*R_filter*C_filter-
w_20k_2*w_20k_2*L_filter*C_filter));
    e_th_2 = (Z_th_2*V_s_2);
    X_th_2 =
((1i*w_20k_2*(L_filter*(1+1i*w_20k_2*R_filter*C_filter)+Lg_filter*(1
+1i*w_20k_2*R_filter*C_filter-
w_20k_2*w_20k_2*L_filter*C_filter)))/(1+1i*w_20k_2*R_filter*C_filter
-w_20k_2*w_20k_2*L_filter*C_filter));
    I_h_2_pre = abs((e_th_2)/(X_th_2+Z_20k_1_pre));
    V_h_2_pre = I_h_2_pre*abs(Z_20k_1_pre-Z_bus);
    V_h_2_pre_max(jj) = V_h_2_pre*1.05;
    i_(jj)=i;
    jj=jj+1;
  end
  V_h_1_threshold = spline(i_,V_h_1_pre_max,M_);
  V_h_2_threshold = spline(i_,V_h_2_pre_max,M_);

  % Do FFT
  Y_fft = fft(data_in(1:8192))/8192;
  fft_mag_V_fft = 2*abs(Y_fft(1:8192/2+1));

  % Get noise floor
  Noise_Floor = 0;
    for i=((f_h(f_index)/50)-7):2:((f_h(f_index)/50)+9)
      Noise_Floor = Noise_Floor + (fft_mag_V_fft(i));
    end
    Noise_Floor = Noise_Floor -
(fft_mag_V_fft(((f_h(f_index)/50)+1)));
    Noise_Floor = Noise_Floor/8;
    left_side_band = ((f_h(f_index)/50));

  % Compare
  if ((fft_mag_V_fft(left_side_band)) >= (V_h_1_threshold)) &&
((fft_mag_V_fft(left_side_band+2)) >= (V_h_2_threshold))
    if Noise_Floor<0.2*(fft_mag_V_fft(left_side_band)) % SNR > ~14dB
      if (islanded < 2)
        islanded = islanded + 1;
        if islanded~=2 % 1st detection
        % scan for suitable band
          band_selected = f_index;
          continue_search = 1;
          for f_scan=f_index+1:1:9
            if continue_search==1
              curr_band_clean = 1;
              for i=((f_h(f_scan)/50)-7):2:((f_h(f_scan)/50)+9)
                if (fft_mag_V_fft(i) > 5e-3)
                  curr_band_clean = 0;
                end
```

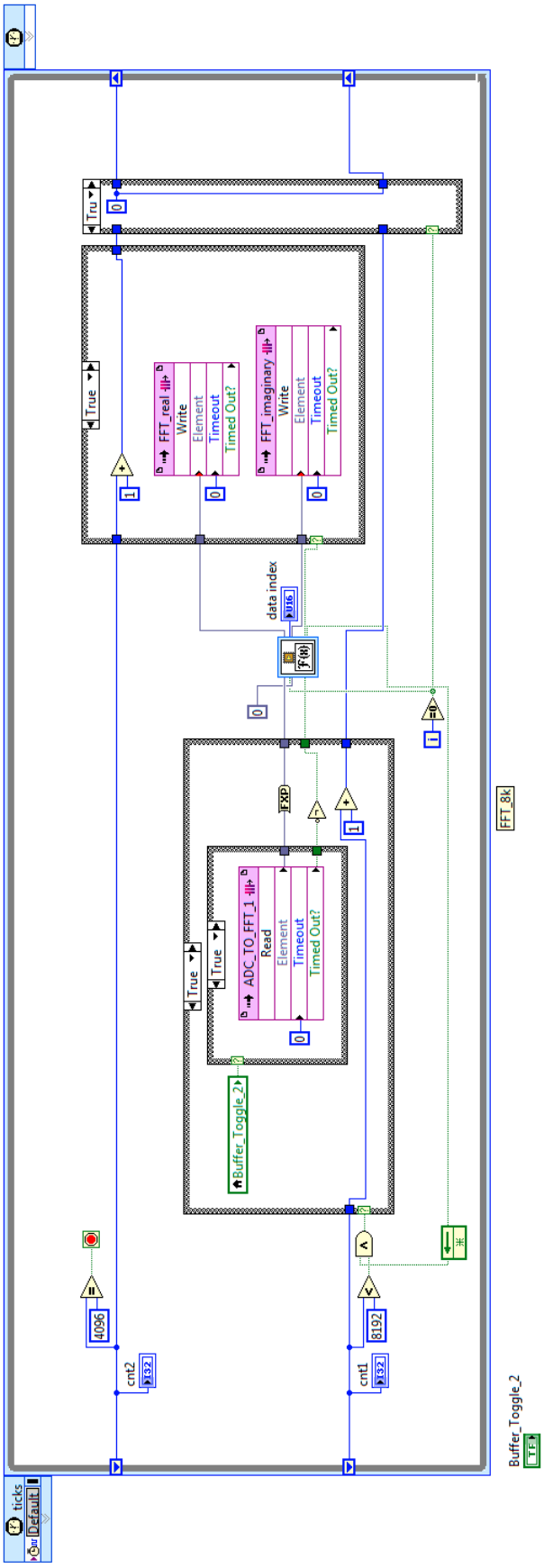
```
              end
              if curr_band_clean == 1;
                band_selected = f_scan;
                continue_search = 0;
              end
            end
          end
          f_index = band_selected;
          f_inv = f_h(f_index)/2;
        end
      end
    end
  else
    if islanded == 1
      islanded = 0;
    end
  end
    index_1 = 0;
end

fft_out = fft_mag_V_fft;

if islanded==2
  islanded_out = 1;
else
  islanded_out = 0;
end

freq = f_inv;
```

Appendices

Appendix G: LabView FPGA Code for Islanding Detection

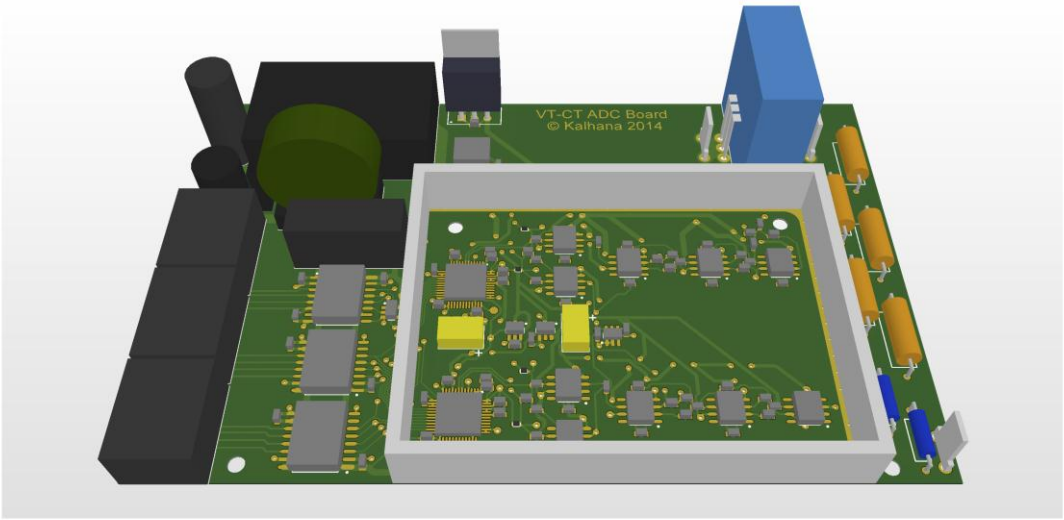

Islanded
0.203125
0.125
h_1995
19.95k_lim
400
393
True
4095
cnt3
FFT_real
FFT_imaginary
Read
Element
Timeout
Timed Out?
Clear
Buffer_Toggle_2
FFT_8k
ADC_Driver

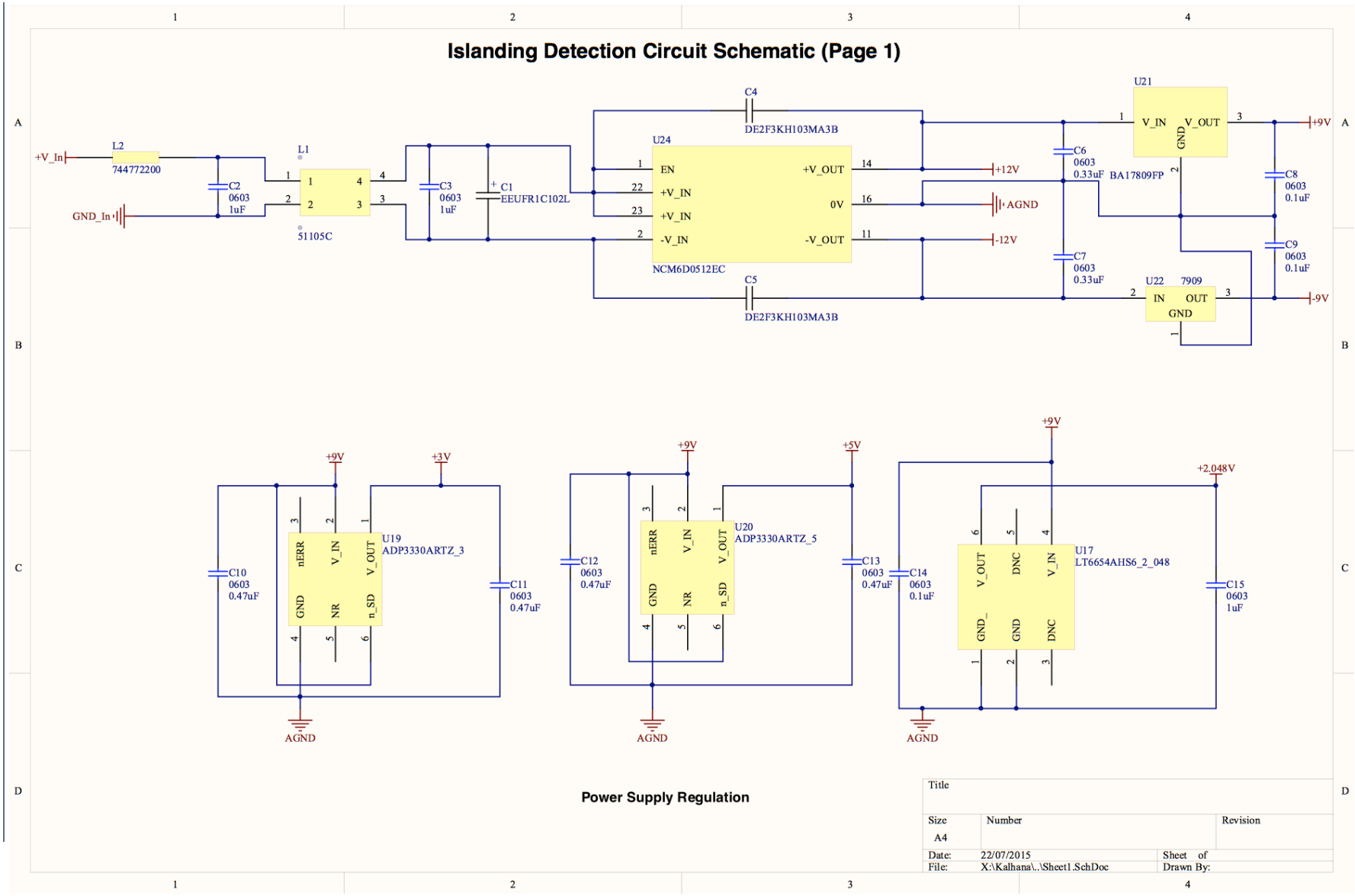

ADS8422 ADC Driver
Buffer_Toggle
Cnt_Capture
nCONVST
nRD
BYTE
nCS
ADC_OUT
Wait Till Next Iteration
ADC_Data
Scaling
Double buffering
ADC_TO_FFT_1
Write
Element
Timeout
Timed Out?
8192
occurrence
Wait After BYTE Toggle
Wait Before Data Read
nCONVST Low Time
ADC_LSB
ADC_MSB

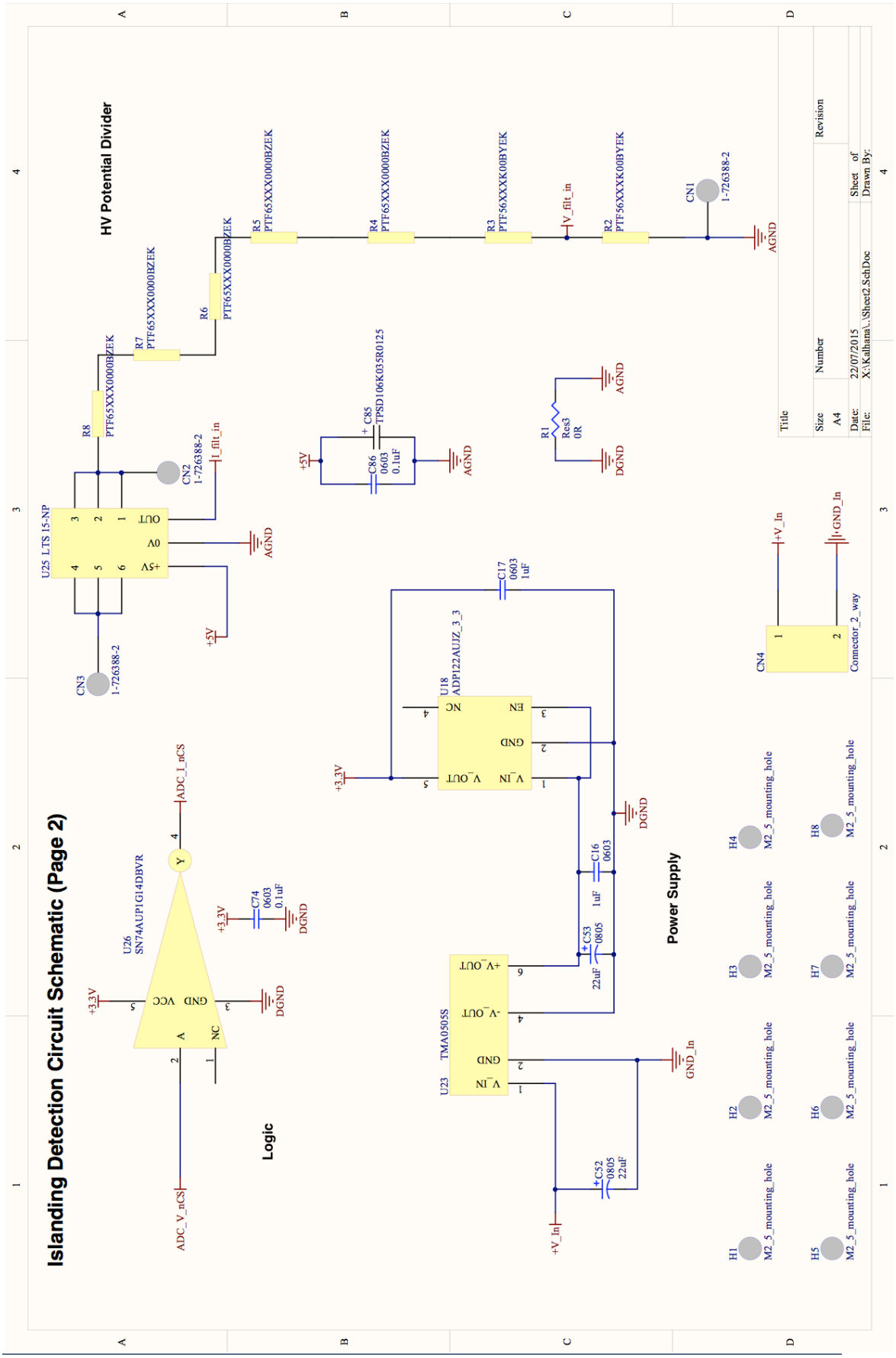

Tru
True
FFT_real
Write
Element
Timeout
Timed Out?
FFT_imaginary
Write
Element
Timeout
Timed Out?
data index
I16
I32
FXP
True
True
ADC_TO_FFT_1
Read
Element
Timeout
Timed Out?
Buffer_Toggle_2
4096
8192
cnt2
cnt1
FFT_8k
Buffer_Toggle_2
TF
ticks
Default

Appendices

Appendix H: Islanding Detection Circuit Schematics




Islanding Detection Circuit Schematic (Page 1)
+V_In
GND_In
L2
744772200
C2
0603
1uF
L1
51105C
C3
0603
1uF
C1
EEUFR1C102L
C4
DE2F3KH103MA3B
C5
DE2F3KH103MA3B
U24
EN
+V_IN
+V_IN
-V_IN
+V_OUT
0V
-V_OUT
NCM6D0512EC
+12V
AGND
-12V
U21
V_IN
V_OUT
GND
BA17809FP
C6
0603
0.33uF
C7
0603
0.33uF
C8
0603
0.1uF
C9
0603
0.1uF
+9V
U22
7909
IN
OUT
GND
-9V
+9V
+3V
U19
ADP3330ARTZ_3
nERR
V_IN
V_OUT
GND
NR
n_SD
C10
0603
0.47uF
C11
0603
0.47uF
AGND
+9V
+5V
U20
ADP3330ARTZ_5
C12
0603
0.47uF
C13
0603
0.47uF
AGND
+9V
+2.048V
U17
LT6654AHS6_2_048
V_OUT
DNC
V_IN
GND_
GND
DNC
C14
0603
0.1uF
C15
0603
1uF
AGND
Power Supply Regulation
Title
Size
A4
Number
Revision
Date:
22/07/2015
Sheet of
File:
X:\Kalhana\..\Sheet1.SchDoc
Drawn By:


Islanding Detection Circuit Schematic (Page 2)
HV Potential Divider
Logic
Power Supply
U25 LTS 15-NP
U26 SN74AUP1G14DBVR
U18 ADP122AUJZ_3_3
U23 TMA0505S
CN1 1-726388-2
CN2 1-726388-2
CN3 1-726388-2
CN4 Connector_2_way
R1 Res3 0R
R2 PTF56XXXK00BYEK
R3 PTF56XXXK00BYEK
R4 PTF65XXX0000BZEK
R5 PTF65XXX0000BZEK
R6 PTF65XXX0000BZEK
R7 PTF65XXX0000BZEK
R8 PTF65XXX0000BZEK
C85 TPSD106K035R0125
C86 0603 0.1uF
C74 0603 0.1uF
C17 0603 1uF
C16 0603
C53 0805 22uF
C52 0805 22uF
V_fil_in
I_fil_in
+V_In
-GND_In
ADC_I_nCS
ADC_V_nCS
AGND
DGND
+5V
+3.3V
H1 M2_5_mounting_hole
H2 M2_5_mounting_hole
H3 M2_5_mounting_hole
H4 M2_5_mounting_hole
H5 M2_5_mounting_hole
H6 M2_5_mounting_hole
H7 M2_5_mounting_hole
H8 M2_5_mounting_hole
Title
Size A4
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Revision
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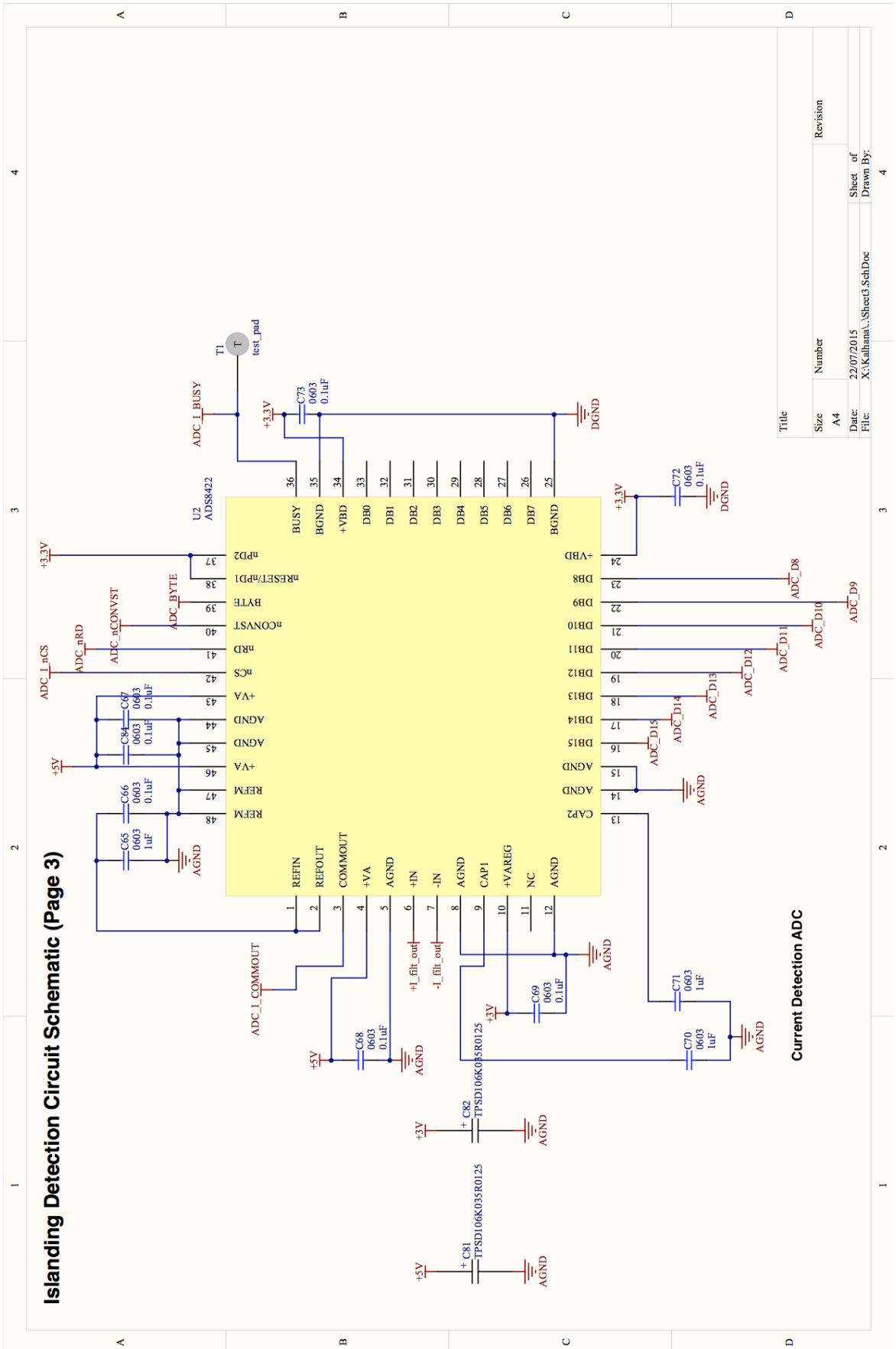
Islanding Detection Circuit Schematic (Page 3)
Current Detection ADC
U2
ADS8422
T1
test_pad
ADC_I_BUSY
ADC_I_COMMOUT
ADC_I_nCS
ADC_nRD
ADC_nCONVST
ADC_BYTE
ADC_D8
ADC_D9
ADC_D10
ADC_D11
ADC_D12
ADC_D13
ADC_D14
ADC_D15
+I_filt_out
-I_filt_out
+3.3V
+5V
+3V
DGND
AGND
C65 0603 1uF
C66 0603 0.1uF
C67 0603 0.1uF
C68 0603 0.1uF
C69 0603 0.1uF
C70 0603 1uF
C71 0603 1uF
C72 0603 0.1uF
C73 0603 0.1uF
C81 TPSD106K035R0125
C82 TPSD106K035R0125
Title
Size A4
Number
Revision
Date: 22/07/2015
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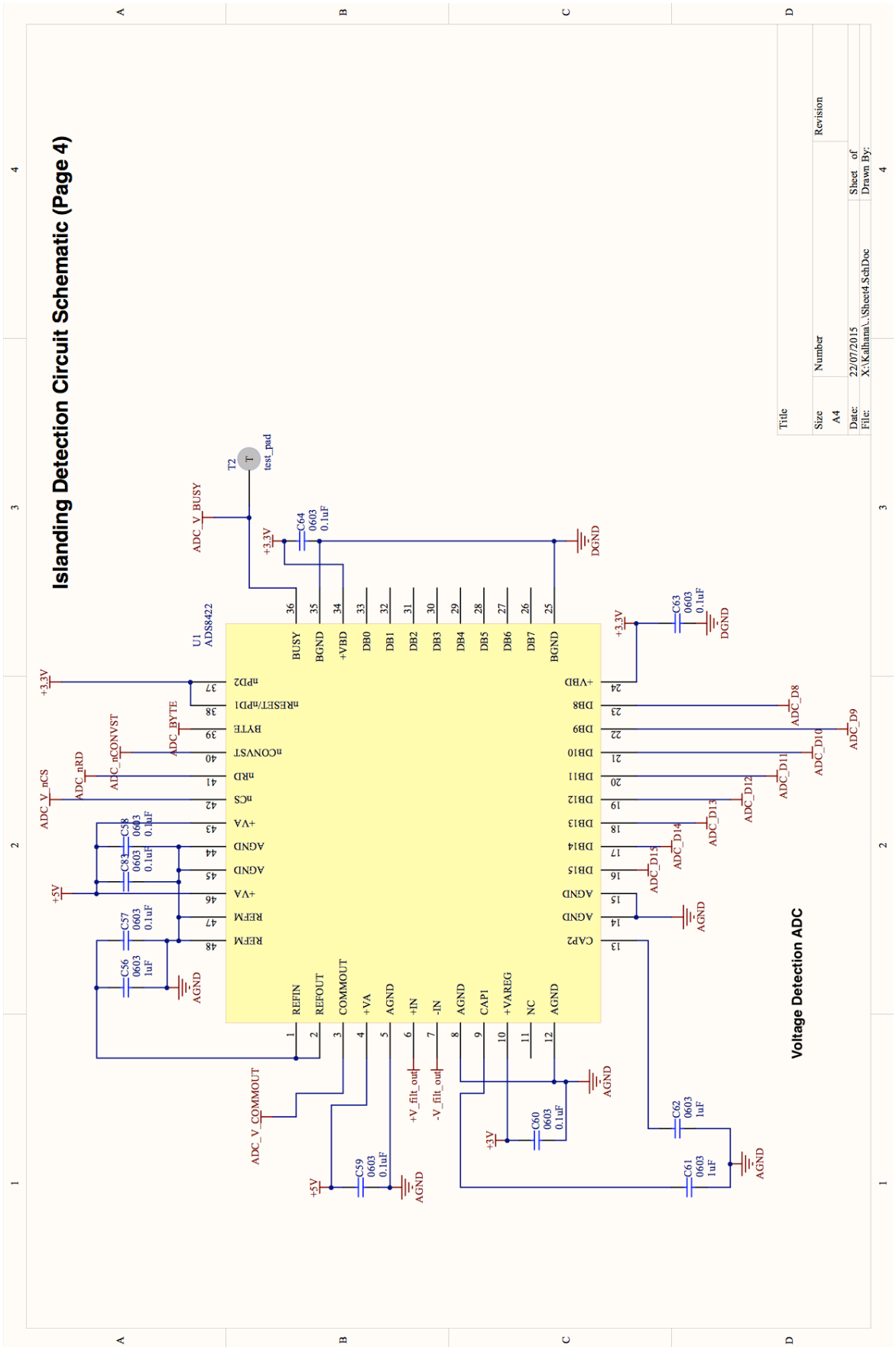
Islanding Detection Circuit Schematic (Page 4)
Voltage Detection ADC
U1
ADS8422
T2
test_pad
ADC_V_BUSY
ADC_V_COMMOUT
ADC_V_nCS
ADC_nRD
ADC_nCONVST
ADC_BYTE
+3.3V
+5V
AGND
DGND
+V_filt_out
-V_filt_out
C56 0603 1uF
C57 0603 0.1uF
C58 0603 0.1uF
C59 0603 0.1uF
C60 0603 0.1uF
C61 0603 1uF
C62 0603 1uF
C63 0603 0.1uF
C64 0603 0.1uF
ADC_D8
ADC_D9
ADC_D10
ADC_D11
ADC_D12
ADC_D13
ADC_D14
ADC_D15
Title
Size A4
Number
Revision
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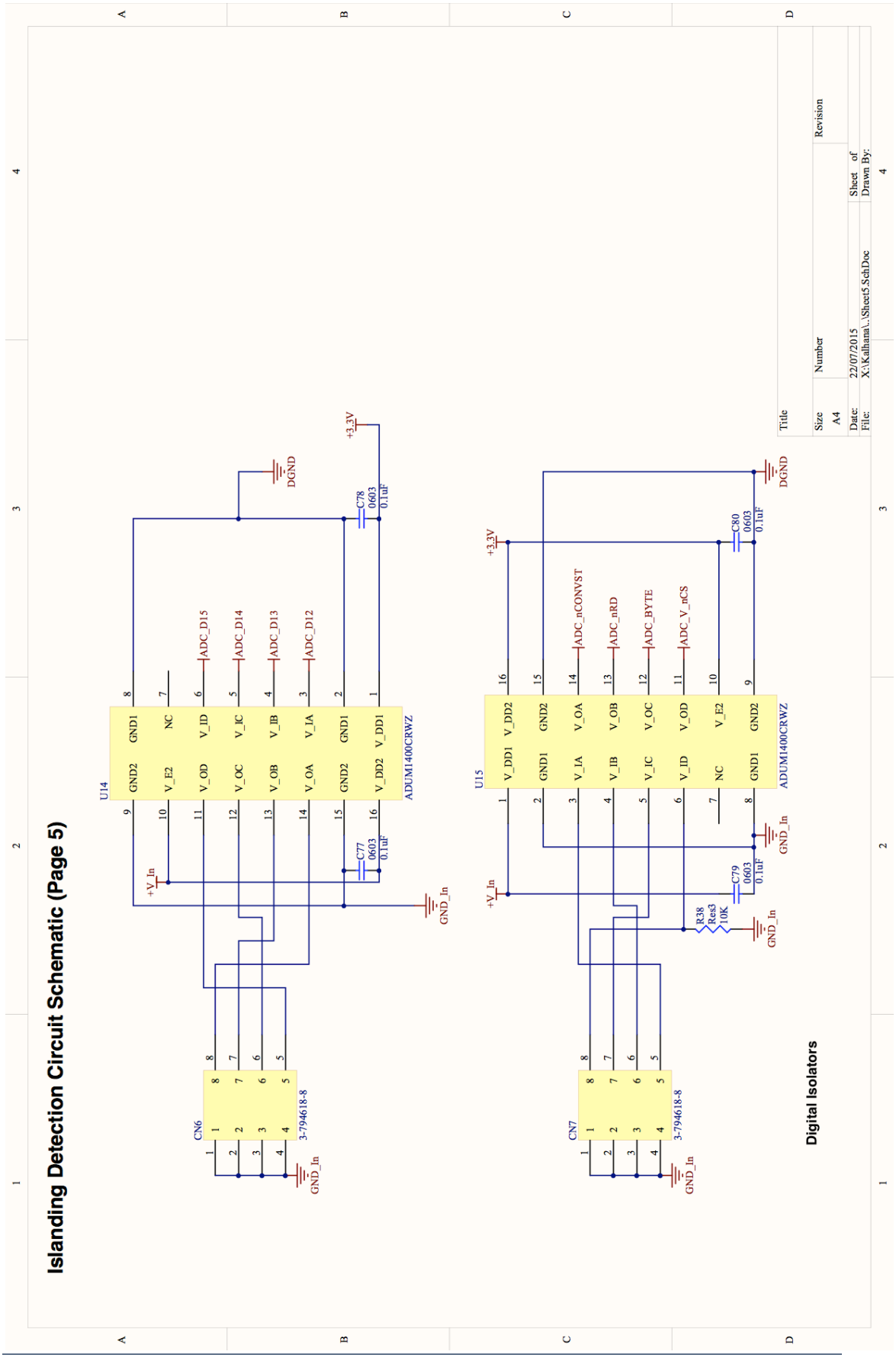
Islanding Detection Circuit Schematic (Page 5)
Digital Isolators
U14
ADUM1400CRWZ
U15
ADUM1400CRWZ
CN6
CN7
3-794618-8
ADC_D15
ADC_D14
ADC_D13
ADC_D12
ADC_nCONVST
ADC_nRD
ADC_BYTE
ADC_V_nCS
+V_In
+3.3V
DGND
GND_In
C77
C78
C79
C80
0603
0.1uF
R38
Res3
10K
Title
Size
A4
Number
Revision
Date:
22/07/2015
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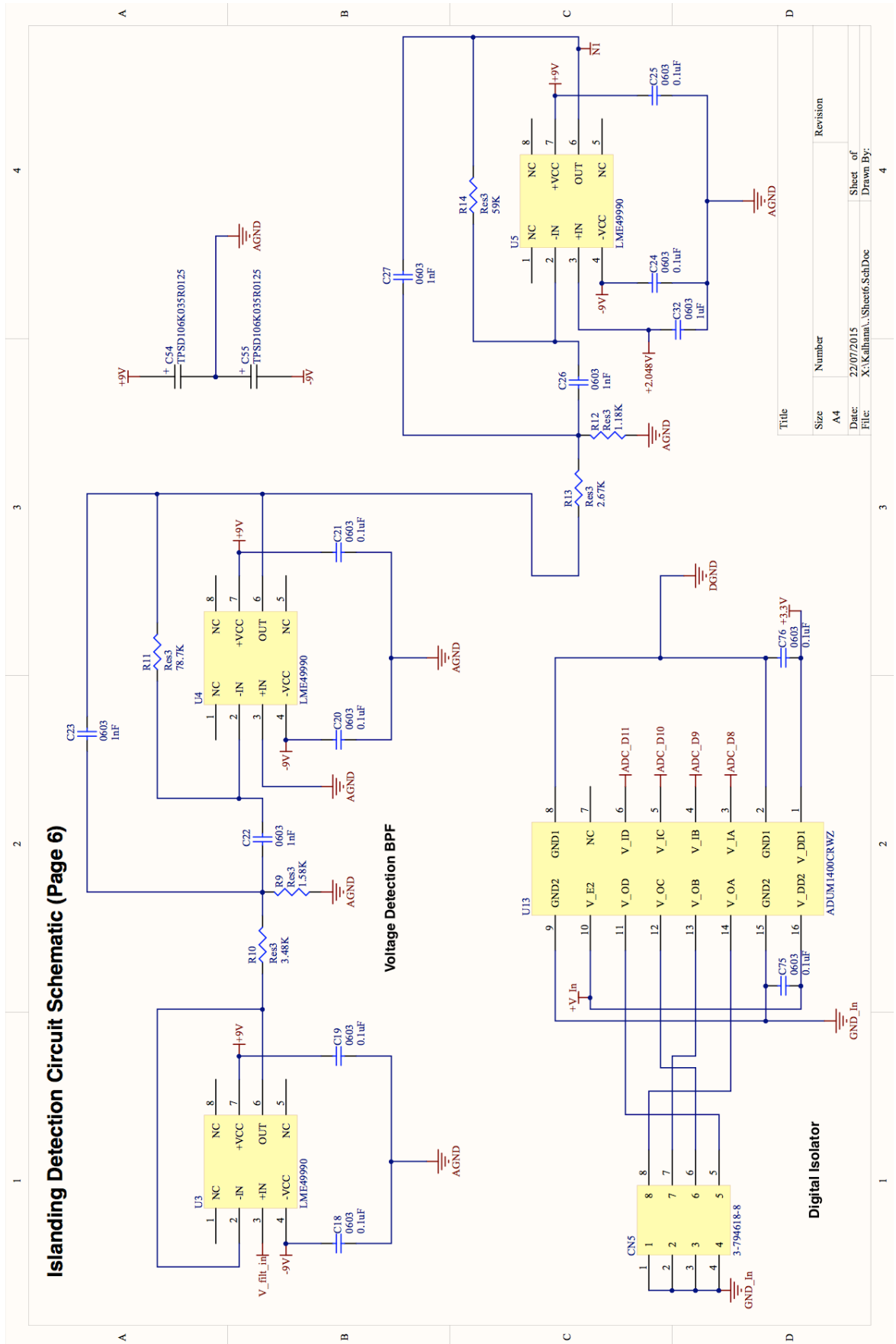
Islanding Detection Circuit Schematic (Page 6)
Voltage Detection BPF
Digital Isolator
U3
U4
U5
U13
LME49990
ADUM1400CRWZ
CN5
3-794618-8
R9 Res3 1.58K
R10 Res3 3.48K
R11 Res3 78.7K
R12 Res3 1.18K
R13 Res3 2.67K
R14 Res3 59K
C18 0603 0.1uF
C19 0603 0.1uF
C20 0603 0.1uF
C21 0603 0.1uF
C22 0603 1nF
C23 0603 1nF
C24 0603 0.1uF
C25 0603 0.1uF
C26 0603 1nF
C27 0603 1nF
C32 0603 1uF
C54 TPSD106K035R0125
C55 TPSD106K035R0125
C75 0603 0.1uF
C76 0603 0.1uF
+9V
-9V
+3.3V
+2.048V
AGND
DGND
GND_In
+V_In
V_filt_in
ADC_D11
ADC_D10
ADC_D9
ADC_D8
Title
Size A4
Number
Revision
Date: 22/07/2015
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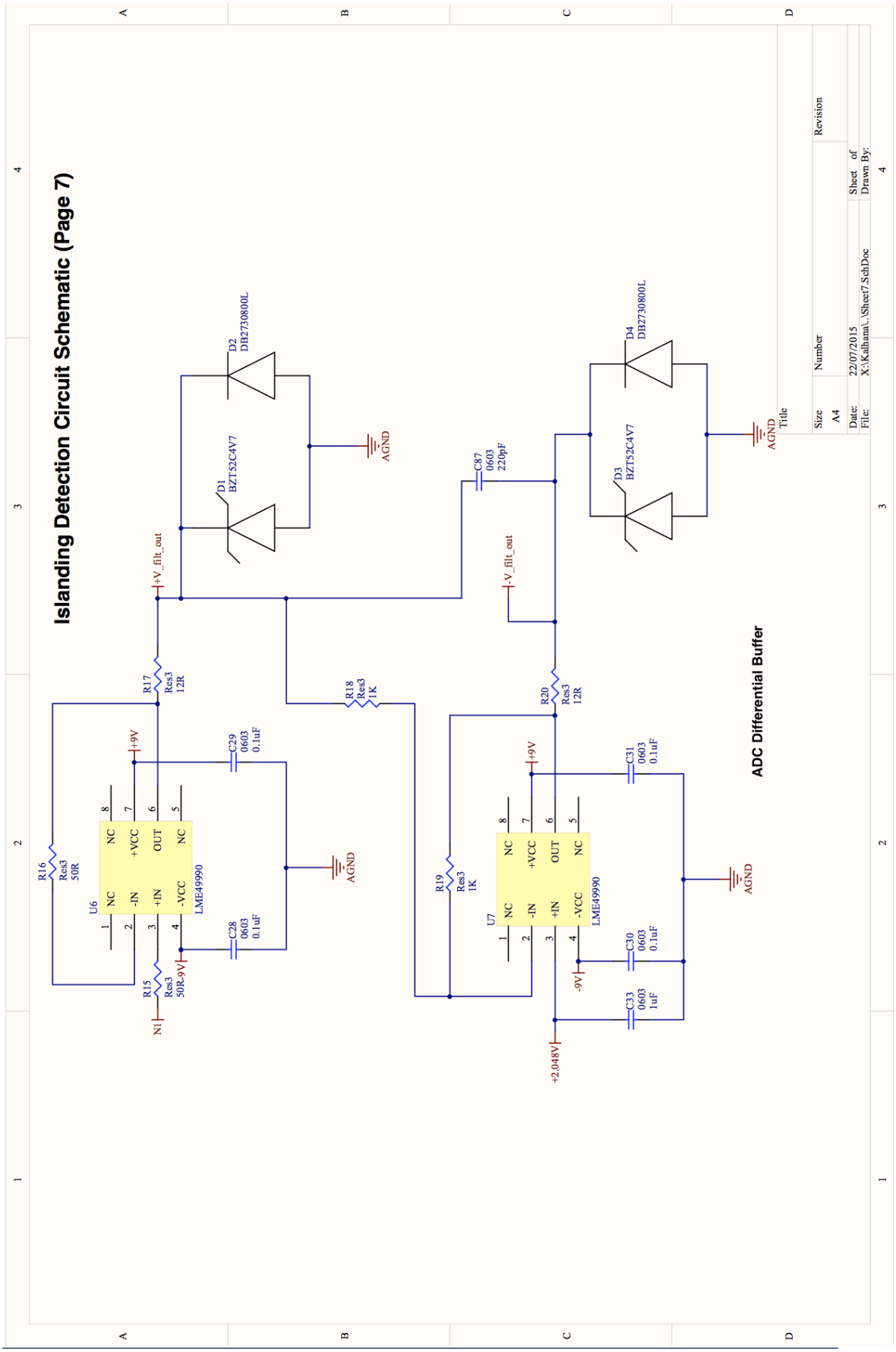
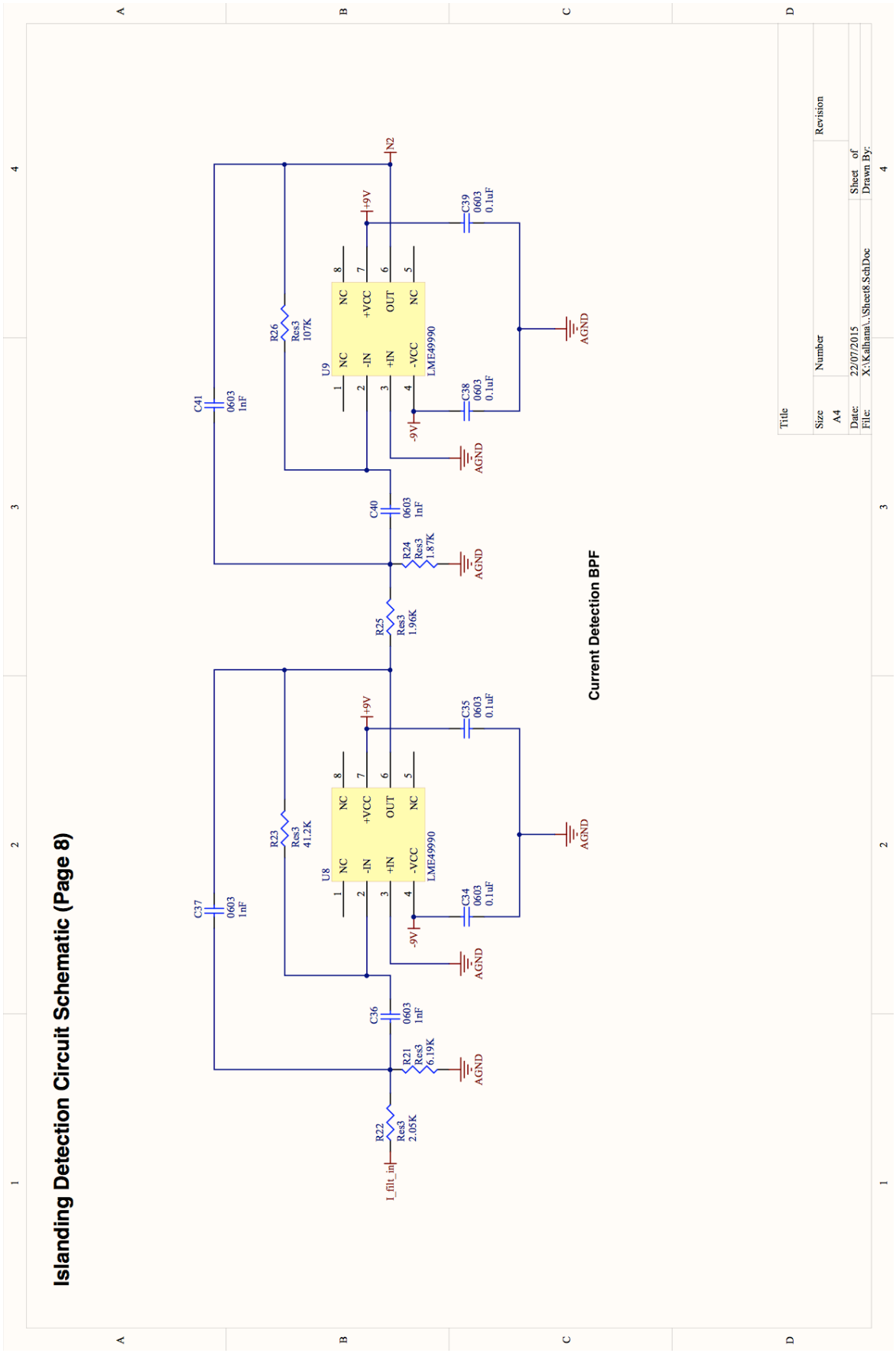

Islanding Detection Circuit Schematic (Page 7)
ADC Differential Buffer
+V_filt_out
-V_filt_out
AGND
+9V
-9V
+2.048V
N1
U6
U7
LME49990
R16 Res3 50R
R15 Res3 50R
R17 Res3 12R
R18 Res3 1K
R19 Res3 1K
R20 Res3 12R
C28 0603 0.1uF
C29 0603 0.1uF
C30 0603 0.1uF
C31 0603 0.1uF
C33 0603 1uF
C87 0603 220pF
D1 BZT52C4V7
D2 DB2730800L
D3 BZT52C4V7
D4 DB2730800L
Size A4
Number
Revision
Date: 22/07/2015
File: X:\Kalhana\..\Sheet7.SchDoc
Sheet of
Drawn By:
Title


Islanding Detection Circuit Schematic (Page 8)
Current Detection BPF
I_filt_in
R22 Res3 2.05K
R21 Res3 6.19K
C36 0603 1nF
R23 Res3 41.2K
C37 0603 1nF
U8 LME49990
C34 0603 0.1uF
C35 0603 0.1uF
R25 Res3 1.96K
R24 Res3 1.87K
C40 0603 1nF
R26 Res3 107K
C41 0603 1nF
U9 LME49990
C38 0603 0.1uF
C39 0603 0.1uF
N2
+9V
-9V
AGND
Title
Size A4
Number
Revision
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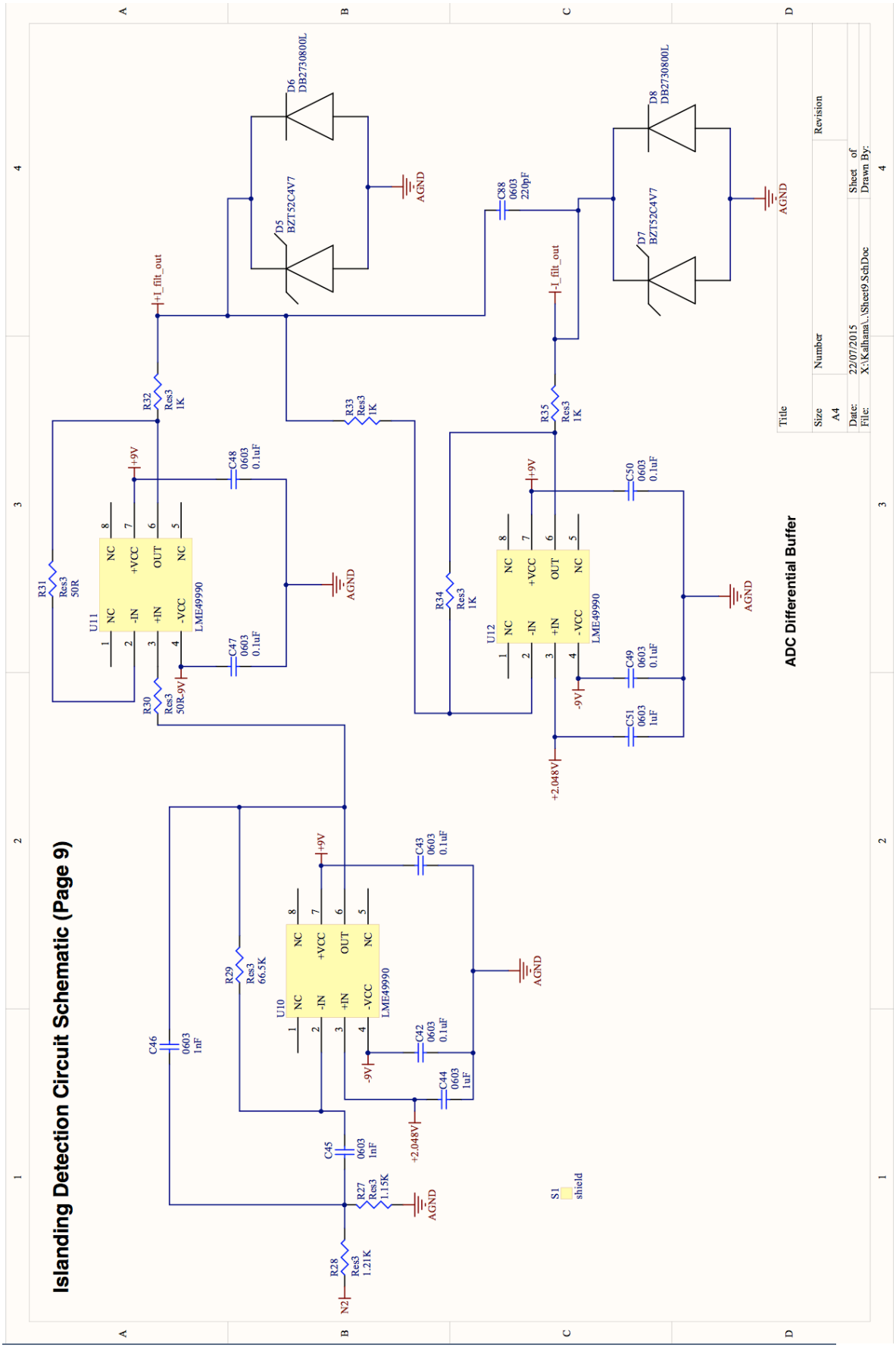
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-9V
+2.048V
AGND
+I_filt_out
-I_filt_out
N2
S1
shield

Appendices

Appendix I: Complex IIR Filters for Tracking of Sinusoids – Edward Daw

Complex IIR Filters for Tracking of Sinusoids

Edward Daw, *Member, IEEE*

***Abstract*—Characterisation of sinusoidal signals embedded in data is an important task in engineering, science and communications. IIR filters are a critical tool, being computationally efficient and introducing minimal time delay. We identify an unconditionally stable class of complex tap IIR filters. We demonstrate that for a sinusoidal input, the steady state output traces an elliptic path in the complex plane. We derive a matrix transformation that maps this elliptic trajectory to a circular one, yielding an angle variable for the driving oscillator. One member of this class of filters is shown to be an iterative approximation for a discrete time Laplace transform ($\mathcal{Z}$–transform) coefficient. This filter is applied as a phase detector for an input sine wave, and incorporated into a phase locked loop (PLL) whose source oscillator is driven by the data itself. The advantage over conventional PLLs is that the oscillator, being driven by the data, has a natural phase relationship to the signal, so that the parameter space to be searched when attempting lock is one dimensional (frequency) as opposed to the two dimensional space (frequency, phase) for more conventional PLLs.**

***Index Terms*—IIR filters, adaptive filters, narrowband, signal analysis, quadrature phase shift keying**

I. Introduction

IIR filters are workhorses of signal processing and are described in great detail in many texts. See, for example, [1], [2]. The n^{th} output of a conventional IIR filter y_n, is related to current and previous inputs $x_n,\ x_{n-1}\cdots$, and previous outputs $y_{n-1},\ y_{n-2}\cdots$ by

$$y_n = b_0 x_n + b_1 x_{n-1} + \cdots - a_1 y_{n-1} - a_2 y_{n-2} - \cdots , \quad (1)$$

where a_n and b_n are real coefficients. The z–plane transfer function can be written

$$H(z) = \frac{y_n}{x_n} = \frac{b_0\left(1+\frac{b_1}{b_0}z^{-1}+\frac{b_2}{b_0}z^{-2}+\cdots\right)}{1-a_1z^{-1}-a_2z^{-2}-\cdots}, \quad (2)$$

where z^{-1} is a sample delay operator. The numerator and denominator polynomials may be factored,

$$H(z) = \frac{b_0\left(1-\frac{z^{-1}}{z_0}\right)\left(1-\frac{z^{-1}}{z_1}\right)\left(1-\frac{z^{-1}}{z_2}\right)\cdots}{\left(1-\frac{z^{-1}}{p_0}\right)\left(1-\frac{z^{-1}}{p_1}\right)\left(1-\frac{z^{-1}}{p_2}\right)\cdots}, \quad (3)$$

where denominator (numerator) factors yield the poles $p_0, p_1, \cdots$ (zeros $z_0, z_1, \cdots$) of $H(z)$. The filter is unconditionally stable if all the poles p_n lie within the unit circle.

Now consider an IIR filter satisfying this stability condition. We obtain a modified filter by multiplying the coefficients by complex phases, yielding

$$\begin{aligned} y_n &= b_0 e^{j\Delta}x_n + b_1 e^{2j\Delta}x_{n-1} + \cdots \\ &\quad -a_1 e^{j\Delta}y_{n-1} - a_2 e^{2j\Delta}y_{n-2} - \cdots . \end{aligned} \quad (4)$$

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The transfer function is

$$H'(z) = \frac{b_0 e^{j\Delta}\left(1+\frac{b_1}{b_0}e^{j\Delta}z^{-1}+\frac{b_2}{b_0}e^{2j\Delta}z^{-2}+\cdots\right)}{1-a_1e^{j\Delta}z^{-1}-a_2e^{2j\Delta}z^{-2}-\cdots}. \quad (5)$$

Making the substitution $u^{-1} = e^{j\Delta}z^{-1}$, we see that the roots of this modified transfer function have the same modulus as before the modification, but arguments which are increased by Δ. The poles therefore remain within the unit circle, proving that the modified filter satisfies the stability condition.

We seek steady state solutions to Equation 4 with a real cosine input $x_n = \cos n\Delta$. The output is of the form $y_n = \frac{1}{2}A_f e^{+jn\Delta} + \frac{1}{2}A_b e^{-jn\Delta}$, where A_f and A_b are complex coefficients. Substituting in to Equation 4, we obtain

$$A_f = \frac{e^{j\Delta}\sum_{p=0}^{\infty} b_p}{1+\sum_{q=1}^{\infty} a_q} \quad A_b = \frac{e^{j\Delta}\sum_{p=0}^{\infty} b_p e^{2jp\Delta}}{1+\sum_{q=1}^{\infty} a_q e^{2jq\Delta}}. \quad (6)$$

We next show that the locus of y_n is an ellipse. Writing $A_{f[b]} = a_{f[b]}e^{j\Phi_{f[b]}}$ and defining $\alpha = (\Phi_f - \Phi_b)/2$ and $\beta = (\Phi_f + \Phi_b)/2$, we can write

$$\begin{aligned} y_n &= e^{j\beta}\left(\tfrac{a_f}{2}e^{j(n\Delta+\alpha)} + \tfrac{a_b}{2}e^{-j(n\Delta+\alpha)}\right). \\ &= e^{j\beta}\left((a_f+a_b)\cos(n\Delta+\alpha)\right. \\ &\quad \left. +j(a_f-a_b)\sin(n\Delta+\alpha)\right). \end{aligned} \quad (7)$$

Inspection of this expression reveals that the locus of y_n is an

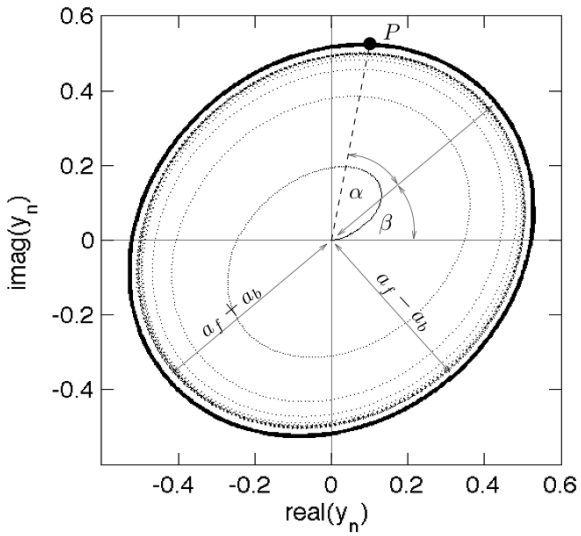

Fig. 1. The elliptical locus of y_n for $x_n = \cos n\Delta$ for $w = 3.906\times10^{-3}$. The points are successive y_n for the first 4096 iterations of the filter. The solid ellipse is calculated from Equation 7, and is shown here 5% larger than the actual limiting ellipse to separate it from the steady state data. The semi–major and semi–minor axes of the ellipse are given in terms of a_f and a_b. The angle β is the inclination of the ellipse semi–major axis to the real axis. The angle α is the phase lead of y_n with respect to the input oscillation.

elliptical trajectory in the complex plane. Refer to Figure 1. If a_f and a_b are both positive, then the major axis of the ellipse is inclined at an angle β to the real axis. The semimajor and semiminor axes are of length $a_f + a_b$ and $a_f - a_b$ respectively. The angle α is the difference between the phase angle of the drive and the angle between y_n and the semi major axis of the ellipse.

By means of the following matrix transformation, this elliptical locus can be transformed into a circular one having zero argument when the input sine wave is at 0° phase,

$$\begin{pmatrix} \Re(z_n) \\ \Im(z_n) \end{pmatrix} = \begin{pmatrix} \cos\alpha & \sin\alpha \\ -\sin\alpha & \cos\alpha \end{pmatrix} \begin{pmatrix} \frac{2}{a_f+a_b} & 0 \\ 0 & \frac{2}{a_f-a_b} \end{pmatrix} \times \begin{pmatrix} \cos\beta & \sin\beta \\ -\sin\beta & \cos\beta \end{pmatrix} \begin{pmatrix} \Re(y_n) \\ \Im(y_n) \end{pmatrix}, \tag{8}$$

where for $x_n = \cos n\Delta$ the transformation yields $\Re(z_n) = \cos n\Delta$ and $\Im(z_n) = \sin n\Delta$.

II. The PIIR filter

For the remainder of this paper we discuss the particular case where the filter coefficients are $b_0 = w$ and $a_1 = w - 1$, and all others zero,

$$y_n = e^{j\Delta}\left((1-w)y_{n-1} + wx_n\right), \tag{9}$$

where w is an integer between 0 and 1. In fact this filter is closely related to the single sided $\mathcal{Z}$–transform [1]

$$X(z) = \sum_{m=0}^{\infty} x_m z^{-m}, \tag{10}$$

evaluated at $z = e^{i\Delta+w}$. This convention has m running upwards from zero, so that increasing m refer to input samples further in the past, and x_0 is the most recent input data sample. The output y_n is then transformed using Equation 8 to yield the I and Q phase oscillation outputs. We refer to this filter as PIIR (phasor IIR). Including the matrix transformation, which we shall always perform for the remainder of this paper, PIIR is also a close cousin of an acausal iteration equation for Fourier coefficients [3], [7].

If we set $\Delta = 0$, the sum in Equation 10 and the terms in brackets in Equation 9 both represent an exponential average of input data into the past. If the sampling period is τ_s, then the time constant of the exponential average is

$$\tau = \tau_s / w. \tag{11}$$

Since Δ is the phase shift per sample, it is related to the frequency f at which the output y_n rotates about the origin, which is also the frequency of the driving input signal by

$$\Delta = 2\pi f \tau_s. \tag{12}$$

Substituting the chosen a and b coefficients into Equation 6 we obtain values for a_f, a_b, Φ_f and Φ_b.

$$\begin{aligned} a_f &= 1 \\ \Phi_f &= \Delta \\ a_b &= \frac{w}{\sqrt{w^2 + 4(1-w)\sin^2\Delta}} \\ \Phi_b &= \arctan\left(\tfrac{2-w}{w}\tan\Delta\right). \end{aligned} \tag{13}$$

We next study the response of the filter to out of band sinusoidal excitation and broadband noise background. At a sampling rate $1/\tau_s = 256\,\mathrm{Hz}$, a series of sine waves with frequencies between DC and $128\,\mathrm{Hz}$ and unit amplitude, plus samples of zero mean gaussian random noise with a standard deviation of $\sigma_n = 0.1$, was applied to a PIIR filter having $f = 50\,\mathrm{Hz}$, for $\tau = [0.3, 3.0, 30]\,\mathrm{s}$. The results are shown in Figure 2.

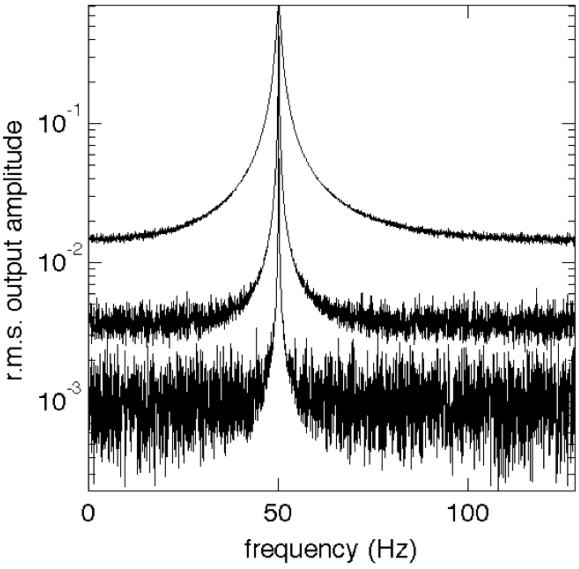

Fig. 2. The r.m.s. at the I–phase output of the PIIR filter for an input consisting of a unit peak amplitude sine wave plus gaussian noise of r.m.s. amplitude 0.1, as a function of the sine wave frequency. The filter response time τ takes the values 0.3, 3 and 30 seconds.

The full width at half maximum of the filter response is $\Gamma = 1/\tau$. The out–of–band r.m.s. amplitude of the noise is suppressed by a factor proportional to $\sqrt{\Gamma}$. The transformation of Equation 8 ensures that $\Re z_n$ and $\Im z_n$ are, respectively, in phase and at a 90° phase lag with respect to the drive. Linear combinations of the two can be made that have the same amplitude as the input but with a tuneable phase lag. The phase factor per sample, Δ, may be adjusted in real time for PLL applications. The PIIR filter is hereafter represented in the schematics to follow by the block shown in Figure 3.

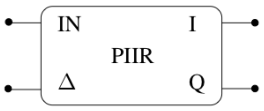

Fig. 3. A block diagram symbol for the PIIR filter

III. Amplitude and Phase detection using the PIIR filter

Using the I and Q phase outputs together with the input data, amplitude and phase shifts in the input data may be measured. The amplitude of the wave is the sum of the two

outputs in quadrature. The phase shift may be determined by mixing the input data with the Q phase output. The resultant signal is a superposition of an offset proportional to phase shifts occuring on a timescale less than τ for the filter, and an upper sideband component at frequency $2f$, which must be removed by filtering. Figure 4 shows a schematic of the phase and amplitude detector.

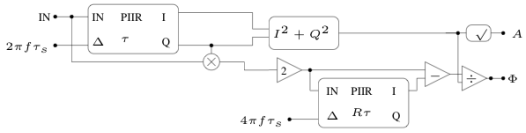

Fig. 4. A schematic of a PIIR amplitude and phase detector. The second PIIR filter removes the upper sideband. It has been found that the ratio of the time constants R between the f and $2f$ PIIR filters of $R = 0.1$ leads to a good step response with minimal $2f$ ringing.

To model the frequency response of this phase detector, input data consisting of a sine wave at frequency $f = 1\,\text{Hz}$, resonant with the first PIIR filter, which had a time constant of $\tau = 5\,\text{s}$. After $90\,\text{s}$ of simulated data to allow the filter to settle, a phase step of $\Phi_0 = 2\pi/100$, or 0.063 radians was applied to the input, and the response measured at the phase output. The result of this measurement is the solid curve in Figure 5. The dotted curve is the following theoretical approximation to

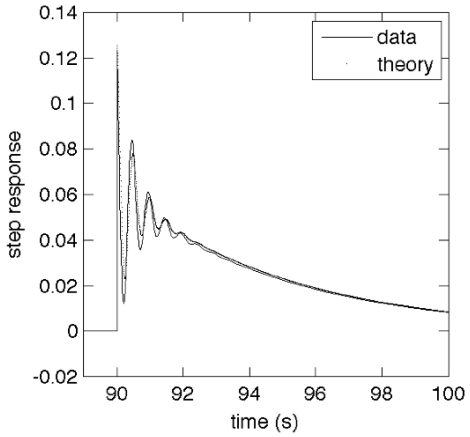

Fig. 5. The step response of the PIIR phase shifter to a phase step in the input data.

the step function,

$$F(t) = \theta(t - 90\,[\text{s}])\Phi_0 e^{\frac{-t}{\tau}}\left(1 + \cos(4\pi f t)e^{\frac{-t}{R\tau}}\right), \qquad (14)$$

where $R = 0.1$. Fourier transforming the step response, setting $s = j\omega$, and multiplying by s yields the transfer function of the phase detector,

$$H_{\text{pd}}(s) = \frac{s^3 + \left(\frac{3(R+1)}{2R\tau} + \frac{1}{2\tau}\right)s^2 + \left(\frac{R+1}{2R\tau^2} + \frac{(R+1)^2}{2R^2\tau^2} + \frac{16\pi^2 f^2}{2}\right)s}{s^3 + \left(\frac{2(R+1)}{R\tau} + \frac{1}{\tau}\right)s^2 + \left(\frac{2(R+1)}{R\tau^2} + \frac{(R+1)^2}{(R\tau)^2} + (4\pi f)^2\right)s + \left(\frac{(R+1)^2}{R^2\tau^3} + \frac{(4\pi f)^2}{\tau}\right)}. \qquad (15)$$

The complexity of this transfer function is due primarily to the $2f$ transient component in the first second after the phase step. Where this frequency is significantly higher than the bandwidth of a closed phase locked loop, we may simplify this expression to the low frequency approximation,

$$H_{\text{lpd}} = \frac{s\tau}{1 + s\tau}. \qquad (16)$$

This simpler transfer function does not reproduce the high frequency ringing in the step response, but it does correctly give the exponential decay. It is an adequate for attaining a qualitative understanding of the critical features of the locked PIIR phase locked loop, such as its closed loop gain.

IV. A PHASE LOCKED LOOP USING PIIR FILTERS

Figure 6 shows an implementation a phase locked loop using the PIIR filter. The phase output of the phase detector circuit

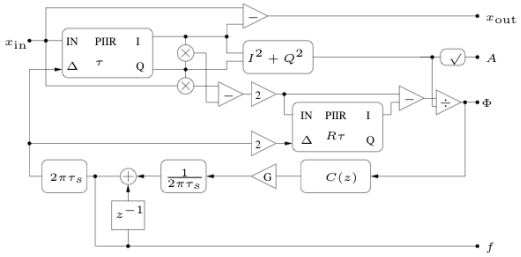

Fig. 6. A block diagram of the PIIR phase locked loop. An initial estimate of the carrier frequency f must be supplied and the filter allowed to run for several times τ before feedback is turned on.

described in Section III is fed back through a filter whose continuous time domain frequency response has the transfer function $C(s)$ [4], where

$$C(s) = \frac{s\tau_2 + 1}{s\tau_\Sigma + 1}. \qquad (17)$$

The output of this filter is multiplied by a gain factor G, and divided by $2\pi\tau_s$ to convert from phase per sample to frequency. This number is the change in frequency that should be applied to the input PIIR so that the frequency of rotation of the complex phasor internal to PIIR matches the frequency of the input sine wave. Therefore this number is added to the previous value of the frequency, converted back into a phase per sample, then applied to the Δ input of the first PIIR, closing the feedback loop. In addition, twice the feedback Δ is applied to the second PIIR filter to move the programmable notch removing the upper sideband output of the mixer to twice the newly adjusted carrier frequency.

There are four useful outputs of this phase locked loop. The amplitude port, A, responds in time τ to changes in amplitude of the input sine wave. The phase port, Φ, records phase fluctuations where the change in phase happens in a time scale of the order of τ or less. The x_{out} port is the input data with the sinusoid to which the PLL is locked subtracted. The f port is the current frequency of the monitored sinusoid.

The unity gain bandwidth of the PLL and a close approximation to its closed loop transfer function can be obtained

using the simple s–plane block diagram represented in Figure 7.

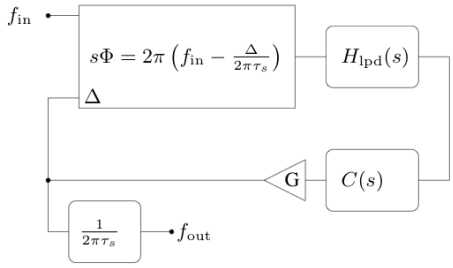

Fig. 7. An s–plane model of the PIIR phase locked loop. The large rectangular block is the phase detector discussed in Section III, using it's simplified low frequency transfer function model.

Consistency around the closed loop requires that

$$s\tau_s f_{\rm out} = GH_{\rm lpd}(s)C(s)\left(f_{\rm in} - f_{\rm out}\right), \qquad (18)$$

which leads to an expression for the closed loop transfer function in frequency is,

$$H(s) = \frac{f_{\rm out}}{f_{\rm in}} = \frac{GH_{\rm lpd}(s)C(s)}{s\tau_s + GH_{\rm lpd}(s)C(s)}. \qquad (19)$$

Substituting in $C(s)$ from Equation 17 and $H_{\rm lpd}$ from Equation 16, we obtain

$$H(s) = \frac{1 + s\tau_2}{s^2\left(\frac{\tau_s\tau_\Sigma}{G}\right) + s\left(\frac{\tau_s\tau_\sigma}{G\tau} + \frac{\tau_s}{G} + \tau_2\right) + \left(1 + \frac{\tau_s}{G\tau}\right)}. \qquad (20)$$

The phase locked loop described in Section IV was implemented with the following parameters: sampling period $\tau_s = 1/256\,\text{Hz}$, $\tau = 5\,\text{s}$, $\tau_2 = 0.159\,\text{s}$, $G = 7.63 \times 10^{-3}$, The carrier frequency was $f = 1\,\text{Hz}$, with a nominal amplitude of 1.5. Throughout the test, amplitude modulation with an amplitude of 0.3 and a frequency of 3 mHz was applied. In addition to this, the frequency of the carrier was modulated with a modulation frequency in the range 1 mHz to 1 Hz at 120 separate frequencies spaced equally between these two limits on a log scale. For each frequency, the PIIR filters were permitted to settle for 30 seconds of data at the carrier frequency having no amplitude or phase modulation. At 30 s, both modulation signals were turned on, and at 40 s, the phase locked loop was closed. After 150 s of data, a single period of $f_{\rm in}$ and $f_{\rm out}$ data was extracted and used to deduce the amplitude ratio and phase shift between the input and measured frequency modulation, thereby giving the closed loop transfer function of the PLL, which is displayed in Figure 8, along with the theoretical estimate based on the simplified s–plane model presented above. The approximate agreement between theory and data confirms that this is a reasonable model. More sophisticated models would yield better agreement in the phase lag, particularly close to the band edge of the servo.

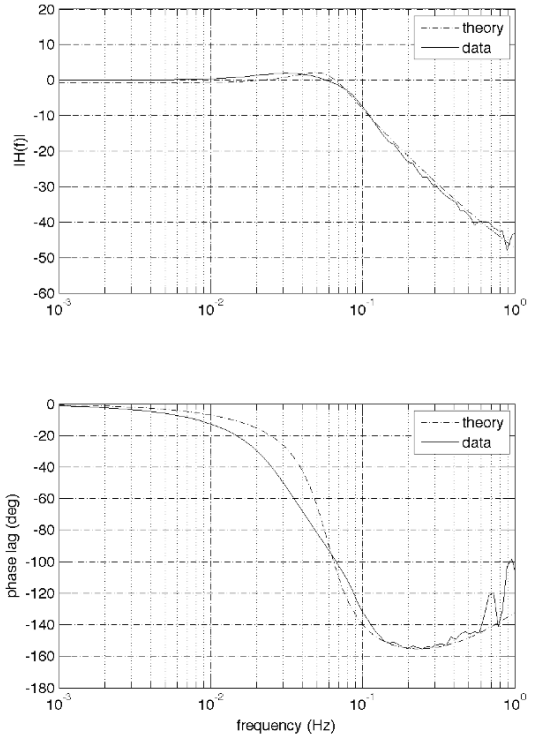

Fig. 8. Measured tranfer function of the PIIR filter in frequency compared with the predictions of the s–plane model. There is good agreement. The biggest discrepancy is in phase close to the unity gain frequency. The discrepancy is due to the approximation made in constructing an s–plane model.

V. Conclusions

The PIIR component is a useful device for driving oscillations with a known ring down time (τ) and a controllable phase relationship to a sinusoidal component of a noisy carrier. This flywheel oscillator can then be used as a reference oscillator having a Q of $1/\tau$. If there are changes in the frequency of the drive, these can be detected by comparison with the reference and used to adjust the frequency of the reference. The advantage that the arbitrary phase difference between this reference and the sinusoidal drive is driven to zero as soon as the drive starts to excite the reference oscillator. This means that the parameter space to be explored during locking is one-dimensional, only the frequency of the sinusoid to be locked to is unknown. If the frequency of the sinusoid is within $\Delta f \sim 1/\tau$ of the initial guess frequency of the flywheel oscillator, the loop is guaranteed to lock. More conventional phase locked loops [4] have a two dimensional parameter space consisting of the frequency and phase of the reference VCO, making locking more complicated. In the case of PIIR, it should be possible to sweep through a wide bandwidth of frequencies identifying resonances and locking to them rapidly and repeatedly. This application in particular will be of interest to those doing analysis of data from ground based gravitational

wave detectors and in other applications where a complex set of harmonics is present, or for anyone wishing to explore a signal space for sinusoidal carriers.

Other applications suggested by the phase locked loop application include tunable notch filters, the subject of many papers in relation to PSK and FSK data encoding protocols [9]–[17]. These adaptive notches, have imaginary poles and zeros arranged symmetrically in the z–plane, yielding a conventional real–output IIR filter. The PIIR filter has a couple of advantages over these methods - there is only one parameter Δ that must be altered to change the notch frequency, and only one parameter (τ) that changes the notch Q, making it simpler to control the notch. In particular, the trick of narrowing the notch width as you increase your precision on the frequency is particularly easy to implement. PIIR is not a Kalman filter [8] because it makes no assumptions about the noise in which the signals are embedded.

The PLL algorithm yields a large set of information about the wave in real time. In open loop (no feedback), phase and amplitude detector mode, the code runs on a conventional PC in the order of 10 ns/sample. Closing the loop increases the compute burden because whenever Δ is changed, one must recalculate the coefficients $\sin\alpha$, $\cos\alpha$ $\sin\beta$, $\cos\beta$, a_f, a_b and the various matrix elements. These calculations involve trigonometric functions. However, modern processors are highly optimised for these calculations, and in fact even for the phase locked loop, we have seen 150 ns/sample operation on a modern fast pentium CPU with a dedicated core. Furthermore, the narrow bandwidth of the PLL loop means that it is certainly feasible to construct a finite state machine that spreads these calculations between different clock cycles should higher bandwidth be needed.

REFERENCES

[1] A. V. Oppenheim, R. W. Schafer, "Digital Signal Processing", (second edition), ISBN 0-13-214635-5, Prentice Hall, 1975.

[2] J. G. Proakis, D. G. Manolakis, "Digital Signal Processing," (third edition), ISBN 0-13-394338-9, Prentice Hall, 1996

[3] J. H. Halberstein, "Recursive, complex fourier analysis for real-time applications," Proc. IEEE **54** 903 (1966)

[4] F. M. Gardener, "Phase lock techniques," Wiley (1965).

[5] J. W. Schmitt and D. L, Starkley, U.S. Patent 3,778,606 (1973)

[6] K. Takaoka and K. Yokosuka-Shi, E.U. Patent EP 1 176 516 A2 (2001)

[7] E. J. Daw and M. R. Hewitson, "A method for characterization of coherent backgrounds in real time and its application in gravitational wave data analysis," Class. Quant. Grav. **25** (2008) 205012 [arXiv:0808.2573 [gr-qc]].

[8] R.K̄alman and R. Bucy, "New results in linear filtering and prediction theory," *Trans. ASME, ser. D, J. Basic Eng.,* vol. 83, pp. 95–107, Dec. 1961.

[9] B.W̄idrow, J. R. Glover, J. M. McCool, J. Kaunitz, C. Williams, R. H. Hearn, J. R. Zeidler, E. Dong Jr., R. C. Goodlin, "Adaptive Noise Cancelling: Principles and Applications," *Proc. IEEE,* vol. 63, no. 12, pp. 1692–1717, Dec. 1975

[10] X. Chen, T. Parks, "Design of IIR filters in the complex domain," IEEE Trans. Acoust., Speech, Signal processing, vol. 38, no. 6, pp. 910–920, June 1990

[11] J. Shynk, "A complex adaptive algorithm for IIR filtering," IEEE Trans. Accoust., Speech, Signal processing, vol. 34, no. 5, pp. 1342–1344, October 1986

[12] P. P. Vaidyanathian, R. Regalia, S. K. Mitra, "Design of doubly complementary IIR digital filters using a single complex allpass filter," Proceedings of the IEEE International Conference on ICASSP '86, vol. 11, pp. 2547–2550, January 2003.

[13] H. Tokuda, S. Takahashi, "Design of two IIR digital filters using a single complex filter," Proceedings. 1996 IEEE TENCON. Digital Signal Processing Applications, vol. 1, pp. 394–399, 1996

[14] S–C. Pei, C–C. Tseng, "Complex adaptive IIR notch filter algorithm and its applications," IEEE Trans. on Circuits and Systems II, vol. 41, issue 2, pps. 158–163, February 1994

[15] H–Y. Jiang, S. Nishimura, T. Hinamoto, "Steady-state analysis of complex adaptive IIR notch filter and its application to QPSK communication systems", Proceedings of the 5th International Conference on Signal Processing, WCCC-ICSP 2000, pp. 551–554 (2000)

[16] Y. Xiao, Y. Takeshita, K. Shida, "Tracking properties of a gradient–based second–order adaptive IIR notch filter with constrained poles and zeros," IEEE Trans. Signal Processing, vol. 50, no. 4, pp. 878–888, April 2002

[17] A. Mvuma, T. Hinamoto, S. Nishimura, "Complex coefficient adaptive IIR notch filter tracking characteristics," Proceedings of the 52nd IEEE International Midwest Symposium on Circuits and Systems, MWSCAS '09, pp. 640–643 (2009)

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List of Acronyms

Acronym	Definition
AC	Alternating current
ADC	Analogue to digital converter
ARPD	Active reactive power drift
BPF	Band pass filter
BW	Bandwidth
CC	Constant current
CC-CV	Constant current - constant voltage
CPU	Central processing unit
CV	Constant voltage
DAB	Dual active bridge
DC	Direct current
DFAC	Double-frequency and amplitude compensation
DG	Distributed grid
DHB	Dual half bridge
DPDT	Double-pole, double-throw
DQ	Direct-quadrature
DSP	Digital signal processor
EMI	Electromagnetic interference
EPLL	Enhanced phase locked loop
EPS	Electrical power system
ESL	Equivalent series inductance
ESR	Equivalent series resistance
EV	Electric vehicle
FCV	Fuel cell vehicle
FFT	Fast Fourier transform
FIFO	First in, first out
FLL	Frequency locked loop
FPGA	Field-programmable gate array
G2V	Grid to vehicle

HC	Harmonic compensation
HEV	Hybrid electric vehicle
HF	High frequency
HFT	High frequency transformer
HIL	Hardware-in-the-loop
IC	Integrated circuit
ICE	Internal combustion engine
IEEE	Institute of Electrical and Electronics Engineers
IGBT	Insulated-gate bipolar transistor
IIR	Infinite impulse response
IoE	Internet of Energy
IQ	In-phase and quadrature
JTAG	Joint Test Action Group
LC	Refers to a network of an inductor and a capacitor
LCL	Refers to a network of two inductors and a capacitor
LF	Loop filter/Low frequency
LFT	Low frequency transformer
LLC	Refers to a network of two inductors and a capacitor
LPF	Low pass filter
LUT	Look up table
MOSFET	Metal–oxide–semiconductor field-effect transistor
NDZ	Non-detection zone
NI	National Instruments
OBBC	On-board bidirectional charger
OFP	Over frequency protection
OVP	Over voltage protection
P-MOB	Personal-mobility
PCC	Point of common coupling
PD	Phase detector
PHEV	Plug-in hybrid electric vehicle
PI	Proportional–integral
PIIR	Phasor infinite impulse response
PLL	Phase locked loop
pPLL	Power based phase locked loop
PV	Photovoltaic

PWM	Pulse width modulation
QSG	Quadrature signal generation
RAM	Random access memory
RHP	Right half plane
RLC	Refers to a parallel resistor, inductor and capacitor load
rms	Root mean square
ROCOF	Rate of change of frequency
SAR	Successive approximation
SEPIC	Single-ended primary-inductor converter
SFDR	Spurious-free dynamic range
SFS	Sandia frequency shift
SMS	Slide-mode frequency shift
SNR	Signal to noise ratio
SOGI	Second order generalised integrator
SRC	Series resonant converter
SRF	Synchronous rotating frame
SRFPI	Synchronous rotating frame, proportional–integral
SST	Solid state transformer
SVS	Sandia voltage shift
THD	Total harmonic distortion
TI	Texas Instruments
UFP	Under frequency protection
UVP	Under voltage protection
V2G	Vehicle to grid
VCO	Voltage controlled oscillator
VSC	Voltage source converter
ZCS	Zero current switching
ZVS	Zero voltage switching

References

[1] T. A. Boden, G. Marland, and R. J. Andres., "Global, Regional, and National Fossil-Fuel CO2 Emissions.," ed. Carbon Dioxide Information Analysis Center, Oak Ridge National Laboratory, U.S. Department of Energy, Oak Ridge, Tenn., U.S.A., 2010.

[2] M. S. J. Hansen, R. Ruedy, et al., "Dangerous human-made interference with climate: a GISS modelE study," *Atmos. Chem. Phys; 7: 2287-2312,* 2007.

[3] W. W. Kellogg and S. H. Schneider, "Global Air Pollution and Climate Change," *Geoscience Electronics, IEEE Transactions on,* vol. 16, pp. 44-50, 1978.

[4] W. W. Kellogg, "Mankind's impact on climate: The evolution of an awareness," *Climatic Change,* vol. 10, pp. 113-136, 1987.

[5] S. Solomon, G.-K. Plattner, R. Knutti, and P. Friedlingstein, "Irreversible climate change due to carbon dioxide emissions," *Proceedings of the National Academy of Sciences,* vol. 106, pp. 1704-1709, February 10, 2009.

[6] "Private Rented Sector Energy Efficiency Regulations (Domestic)," D. o. E. a. C. Change, Ed., ed, 2015.

[7] "Climate change levy," ed, 2009.

[8] C. C. Chan, "The State of the Art of Electric, Hybrid, and Fuel Cell Vehicles," *Proceedings of the IEEE,* vol. 95, pp. 704-718, 2007.

[9] L. Jun-Young and H. Byung-Moon, "A Bidirectional Wireless Power Transfer EV Charger Using Self-Resonant PWM," *Power Electronics, IEEE Transactions on,* vol. 30, pp. 1784-1787, 2015.

[10] H. Omori, T. Morizane, N. Kimura, and M. Nakaoka, "A wireless Vehicle to Home system with resonant IPT bidirectional single-ended inverter for smart house," in *Intelligent Green Building and Smart Grid (IGBSG), 2014 International Conference on*, 2014, pp. 1-4.

[11] C. Guille and G. Gross, "Design of a Conceptual Framework for the V2G Implementation," in *Energy 2030 Conference, 2008. ENERGY 2008. IEEE*, 2008, pp. 1-3.

[12] H. Sekyung, H. Soohee, and K. Sezaki, "Development of an Optimal Vehicle-to-Grid Aggregator for Frequency Regulation," *Smart Grid, IEEE Transactions on,* vol. 1, pp. 65-72, 2010.

[13] W. Kempton, "Electric vehicles as a new power source for electric utilities," *Transportation Research Part D: Transport and Environment,* vol. 2, pp. 157-175, 1997.

[14] M. C. Kisacikoglu, B. Ozpineci, and L. M. Tolbert, "Examination of a PHEV bidirectional charger system for V2G reactive power compensation," in *Applied Power Electronics Conference and Exposition (APEC), 2010 Twenty-Fifth Annual IEEE*, 2010, pp. 458-465.

[15] H. Lund and W. Kempton, "Integration of renewable energy into the transport and electricity sectors through V2G," *Energy Policy,* vol. 36, pp. 3578-3587, 2008.

[16] J. Tomić and W. Kempton, "Using fleets of electric-drive vehicles for grid support," *Journal of Power Sources,* vol. 168, pp. 459-468, 2007.

[17] X. Guo and J. Guo, "A New Synchronization Algorithm for Grid-Connected Inverters," *Applied Mathematics & Information Sciences,* vol. 8, pp. 869-875, 2014.

[18] M. E. Ropp, M. Begovic, and A. Rohatgi, "Prevention of islanding in grid-connected photovoltaic systems," *Progress in Photovoltaics: Research and Applications,* vol. 7, pp. 39-59, 1999.

[19] M. Yilmaz and P. T. Krein, "Review of Battery Charger Topologies, Charging Power Levels, and Infrastructure for Plug-In Electric and Hybrid Vehicles," *Power Electronics, IEEE Transactions on,* vol. 28, pp. 2151-2169, 2013.

[20] R. M. Schupbach and J. C. Balda, "Comparing DC-DC converters for power management in hybrid electric vehicles," in *Electric Machines and Drives Conference, 2003. IEMDC'03. IEEE International*, 2003, pp. 1369-1374 vol.3.

[21] D. Yu, Z. Xiaohu, B. Sanzhong, S. Lukic, and A. Huang, "Review of non-isolated bi-directional DC-DC converters for plug-in hybrid electric vehicle charge station application at municipal parking decks," in *Applied Power Electronics Conference and Exposition (APEC), 2010 Twenty-Fifth Annual IEEE*, 2010, pp. 1145-1151.

[22] F. Z. Peng, L. Hui, S. Gui-Jia, and J. S. Lawler, "A new ZVS bidirectional DC-DC converter for fuel cell and battery application," *Power Electronics, IEEE Transactions on,* vol. 19, pp. 54-65, 2004.

[23] K. Minho, J. Sehyung, and C. Sewan, "A high efficiency bi-directional EV charger with seamless mode transfer for V2G and V2H application," in *Energy Conversion Congress and Exposition (ECCE), 2015 IEEE*, 2015, pp. 5394-5399.

[24] R. W. A. De Doncker, D. M. Divan, and M. H. Kheraluwala, "A three-phase soft-switched high-power-density DC/DC converter for high-power applications," *Industry Applications, IEEE Transactions on,* vol. 27, pp. 63-73, 1991.

[25] J. H. Jung, H. S. Kim, M. H. Ryu, and J. W. Baek, "Design Methodology of Bidirectional CLLC Resonant Converter for High-Frequency Isolation of DC Distribution Systems," *Power Electronics, IEEE Transactions on,* vol. 28, pp. 1741-1755, 2013.

[26] J. Tianyang, Z. Junming, W. Xinke, S. Kuang, and W. Yousheng, "A Bidirectional LLC Resonant Converter With Automatic Forward and Backward Mode Transition," *Power Electronics, IEEE Transactions on,* vol. 30, pp. 757-770, 2015.

[27] C. Wei, R. Ping, and L. Zhengyu, "Snubberless Bidirectional DC–DC Converter With New CLLC Resonant Tank Featuring Minimized Switching Loss," *Industrial Electronics, IEEE Transactions on,* vol. 57, pp. 3075-3086, 2010.

[28] L. Xiaodong and A. K. S. Bhat, "Analysis and Design of High-Frequency Isolated Dual-Bridge Series Resonant DC/DC Converter," *Power Electronics, IEEE Transactions on,* vol. 25, pp. 850-862, 2010.

[29] Z. U. Zahid, Z. M. Dalala, C. Rui, C. Baifeng, and L. Jih-Sheng, "Design of Bidirectional DC–DC Resonant Converter for Vehicle-to-Grid (V2G) Applications," *Transportation Electrification, IEEE Transactions on,* vol. 1, pp. 232-244, 2015.

[30] G. Pledl, M. Tauer, and D. Buecherl, "Theory of operation, design procedure and simulation of a bidirectional LLC resonant converter for vehicular applications," in *Vehicle Power and Propulsion Conference (VPPC), 2010 IEEE*, 2010, pp. 1-5.

[31] L. Gang, L. Dan, Z. Jian Qiu, H. Bo, and J. Min Li, "Bidirectional CLLC resonant DC-DC converter with integrated magnetic for OBCM application," in *Industrial Technology (ICIT), 2015 IEEE International Conference on*, 2015, pp. 946-951.

[32] F. Krismer, J. Biela, and J. W. Kolar, "A comparative evaluation of isolated bi-directional DC/DC converters with wide input and output voltage range," in *Industry Applications Conference, 2005. Fourtieth IAS Annual Meeting. Conference Record of the 2005*, 2005, pp. 599-606 Vol. 1.

[33] R. Teodorescu, M. Liserre, and P. Rodriguez, "Grid Converters for Photovoltaic and Wind Power Systems," ed: John Wiley & Sons, Ltd., 2011.

[34] H. Guan-Chyun and J. C. Hung, "Phase-locked loop techniques. A survey," *Industrial Electronics, IEEE Transactions on,* vol. 43, pp. 609-615, 1996.

[35] L. N. Amuda, B. J. Cardoso Filho, S. M. Silva, S. R. Silva, and A. S. A. C. Diniz, "Wide bandwidth single and three-phase PLL structures for grid-tied PV systems," in *Photovoltaic Specialists Conference, 2000. Conference Record of the Twenty-Eighth IEEE*, 2000, pp. 1660-1663.

[36] L. N. Arruda, S. M. Silva, and B. J. C. Filho, "PLL structures for utility connected systems," in *Industry Applications Conference, 2001. Thirty-Sixth IAS Annual Meeting. Conference Record of the 2001 IEEE*, 2001, pp. 2655-2660 vol.4.

[37] M. Karimi-Ghartemani and M. R. Iravani, "A new phase-locked loop (PLL) system," in *Circuits and Systems, 2001. MWSCAS 2001. Proceedings of the 44th IEEE 2001 Midwest Symposium on*, 2001, pp. 421-424 vol.1.

[38] M. Ciobotaru, R. Teodorescu, and F. Blaabjerg, "A New Single-Phase PLL Structure Based on Second Order Generalized Integrator," in *Power Electronics Specialists Conference, 2006. PESC '06. 37th IEEE*, 2006, pp. 1-6.

[39] R. M. dos Santos Filho, P. F. Seixas, and P. C. Cortizo, "A Comparative Study of Three- Phase and Single-Phase PLL Algorithms for Grid-Connected Systems," in *Industry Applications Conference, INDUSCON*, Recife, Brazil, 2006.

[40] S. Golestan, M. Monfared, F. D. Freijedo, and J. M. Guerrero, "Design and Tuning of a Modified Power-Based PLL for Single-Phase Grid-Connected Power Conditioning Systems," *Power Electronics, IEEE Transactions on,* vol. 27, pp. 3639-3650, 2012.

[41] x, A. zdemir, I. Yazici, and C. Vural, "Fast and robust software-based digital phase-locked loop for power electronics applications," *Generation, Transmission & Distribution, IET,* vol. 7, pp. 1435-1441, 2013.

[42] A. Ohori, N. Hattori, and T. Funaki, "Phase-Locked Loop Using Complex-Coefficient Filters for Grid-Connected Inverter," *Electrical Engineering in Japan,* vol. 189, pp. 52-60, 2014.

[43] L. Huawu, S. Yongheng, H. Haibing, and X. Yan, "A new single-phase PLL based on discrete fourier transform," in *Applied Power Electronics Conference and Exposition (APEC), 2015 IEEE*, 2015, pp. 521-526.

[44] "IEEE Recommended Practice for Utility Interface of Photovoltaic (PV) Systems," *IEEE Std 929-2000,* p. i, 2000.

[45] *Integrated Enabling Technologies for Efficient Electrical Personal Mobility*. Available: http://www.egvi.eu/projectslist/72/37/P-MOB

[46] *Internet of Energy for Electric Mobility*. Available: http://www.artemis-ioe.eu/ioe_project.htm

[47] S. Lacroix, E. Laboure, and M. Hilairet, "An integrated fast battery charger for Electric Vehicle," in *Vehicle Power and Propulsion Conference (VPPC), 2010 IEEE*, 2010, pp. 1-6.

[48] C. Gould, K. Colombage, W. Jiabin, D. Stone, and M. Foster, "A comparative study of on-board bidirectional chargers for electric vehicles to support vehicle-to-grid power transfer," in *Power Electronics and Drive Systems (PEDS), 2013 IEEE 10th International Conference on*, 2013, pp. 639-644.

[49] Z. Biao, S. Qiang, L. Wenhua, and S. Yandong, "Overview of Dual-Active-Bridge Isolated Bidirectional DC–DC Converter for High-Frequency-Link Power-Conversion System," *Power Electronics, IEEE Transactions on,* vol. 29, pp. 4091-4106, 2014.

[50] M. Kashif, "Bidirectional flyback DC-DC converter for hybrid electric vehicle: Utility, working and PSPICE computer model," in *Microelectronics and Electronics (PrimeAsia), 2012 Asia Pacific Conference on Postgraduate Research in*, 2012, pp. 61-66.

[51] H. S. H. Chung, C. Wai-Leung, and K. S. Tang, "A ZCS bidirectional flyback DC/DC converter," *Power Electronics, IEEE Transactions on,* vol. 19, pp. 1426-1434, 2004.

[52] A. A. Aboulnaga and A. Emadi, "Performance evaluation of the isolated bidirectional Cuk converter with integrated magnetics," in *Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual*, 2004, pp. 1557-1562 Vol.2.

[53] Z. Fanghua and Y. Yangguang, "Novel Forward–Flyback Hybrid Bidirectional DC–DC Converter," *Industrial Electronics, IEEE Transactions on,* vol. 56, pp. 1578-1584, 2009.

[54] X. Huafeng and X. Shaojun, "A ZVS Bidirectional DC–DC Converter With Phase-Shift Plus PWM Control Scheme," *Power Electronics, IEEE Transactions on,* vol. 23, pp. 813-823, 2008.

[55] Z. Zhe, O. C. Thomsen, and M. A. E. Andersen, "Optimal Design of a Push-Pull-Forward Half-Bridge (PPFHB) Bidirectional DC–DC Converter With Variable Input Voltage," *Industrial Electronics, IEEE Transactions on,* vol. 59, pp. 2761-2771, 2012.

[56] E. V. de Souza and I. Barbi, "Bidirectional Current-Fed Flyback-Push-Pull DC-DC Converter," in *Power Electronics Conference (COBEP), 2011 Brazilian*, 2011, pp. 8-13.

[57] C. Huang-Jen and L. Li-Wei, "A bidirectional DC-DC converter for fuel cell electric vehicle driving system," *Power Electronics, IEEE Transactions on,* vol. 21, pp. 950-958, 2006.

[58] L. Hui, P. Fang Zheng, and J. S. Lawler, "A natural ZVS medium-power bidirectional DC-DC converter with minimum number of devices," *Industry Applications, IEEE Transactions on,* vol. 39, pp. 525-535, 2003.

[59] L. Jun-Young, J. Yu-Seok, and H. Byung-Moon, "A Two-Stage Isolated/Bidirectional DC/DC Converter With Current Ripple Reduction Technique," *Industrial Electronics, IEEE Transactions on,* vol. 59, pp. 644-646, 2012.

[60] L. Roggia, L. Schuch, J. E. Baggio, C. Rech, and J. R. Pinheiro, "Integrated Full-Bridge-Forward DC–DC Converter for a Residential Microgrid Application," *Power Electronics, IEEE Transactions on,* vol. 28, pp. 1728-1740, 2013.

[61] K. Wang, C. Y. Lin, L. Zhu, D. Qu, F. C. Lee, and J. S. Lai, "Bi-directional DC to DC converters for fuel cell systems," in *Power Electronics in Transportation, 1998*, 1998, pp. 47-51.

[62] A. Hyunsung and C. Hanju, "Second harmonic current reduction by using a resonant circuit in a single-phase battery charger," in *Energy Conversion Congress and Exposition (ECCE), 2013 IEEE*, 2013, pp. 1409-1413.

[63] K. Tae-Hoon, J. Jin-Beom, L. Baek-Haeng, S. Dong-Hyun, S. Hyun-Sik, K. Byoung-Hoon*, et al.*, "Analytical study on low-frequency ripple effect of battery charging," in *Vehicle Power and Propulsion Conference (VPPC), 2012 IEEE*, 2012, pp. 809-811.

[64] S. Bala, T. Tengner, P. Rosenfeld, and F. Delince, "The effect of low frequency current ripple on the performance of a Lithium Iron Phosphate (LFP) battery energy storage system," in *Energy Conversion Congress and Exposition (ECCE), 2012 IEEE*, 2012, pp. 3485-3492.

[65] C. Liang-Rui, C. Jin-Jia, H. Chun-Min, W. Shing-Lih, and S. Deng-Tswen, "Improvement of Li-ion Battery Discharging Performance by Pulse and Sinusoidal Current Strategies," *Industrial Electronics, IEEE Transactions on,* vol. 60, pp. 5620-5628, 2013.

[66] C. Liang-Rui, W. Shing-Lih, S. Deng-Tswen, and C. Tsair-Rong, "Sinusoidal-Ripple-Current Charging Strategy and Optimal Charging Frequency Study for Li-Ion Batteries," *Industrial Electronics, IEEE Transactions on,* vol. 60, pp. 88-97, 2013.

[67] L. Yong-Duk and P. Sung-Yeul, "Electrochemical State-Based Sinusoidal Ripple Current Charging Control," *Power Electronics, IEEE Transactions on,* vol. 30, pp. 4232-4243, 2015.

[68] W. Weimin, H. Yuanbin, and F. Blaabjerg, "An LLCL Power Filter for Single-Phase Grid-Tied Inverter," *Power Electronics, IEEE Transactions on,* vol. 27, pp. 782-789, 2012.

[69] J. M. Bloemink and T. C. Green, "Reducing passive filter sizes with tuned traps for distribution level power electronics," in *Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on*, 2011, pp. 1-9.

[70] "IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems," *IEEE Std 519-1992,* pp. 1-112, 1993.

[71] J. Pleite, V. Valdivia, P. Zumel, and C. Gonzalez, "Transformer and Series Inductance Integration for Harmonic Filtering in PWM Inverters Based in a Simple Design Procedure," in *Industrial Electronics, 2007. ISIE 2007. IEEE International Symposium on*, 2007, pp. 1201-1206.

[72] V. Valdivia, J. Pleite, C. Gonzalez, and R. A. Salas, "New approach to integrate an LCL filter and a transformer for grid connected converters following a simple design procedure," in *Industrial Electronics Society, 2007. IECON 2007. 33rd Annual Conference of the IEEE*, 2007, pp. 1299-1303.

[73] V. Valdivia, J. Pleite, P. Zumel, C. Gonzalez, and A. M. Roldan, "Three phase LCL filter and transformer with integrated magnetics for grid connected converters," in *Industrial Electronics, 2008. IECON 2008. 34th Annual Conference of IEEE*, 2008, pp. 1027-1032.

[74] H. R. Karshenas and H. Saghafi, "Basic Criteria in Designing LCL Filters for Grid Connected Converters," in *Industrial Electronics, 2006 IEEE International Symposium on*, 2006, pp. 1996-2000.

[75] V. Blasko and V. Kaura, "A novel control to actively damp resonance in input LC filter of a three-phase voltage source converter," *Industry Applications, IEEE Transactions on,* vol. 33, pp. 542-550, 1997.

[76] C. Wessels, J. Dannehl, and F. W. Fuchs, "Active damping of LCL-filter resonance based on virtual resistor for PWM rectifiers — stability analysis with different filter parameters," in *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE*, 2008, pp. 3532-3538.

[77] Z. Guohong, T. W. Rasmussen, M. Lin, and R. Teodorescu, "Design and control of LCL-filter with active damping for Active Power Filter," in *Industrial Electronics (ISIE), 2010 IEEE International Symposium on*, 2010, pp. 2557-2562.

[78] W. Weimin, H. Yuanbin, T. Tianhao, and F. Blaabjerg, "A New Design Method for the Passive Damped LCL and LLCL Filter-Based Single-Phase Grid-Tied Inverter," *Industrial Electronics, IEEE Transactions on,* vol. 60, pp. 4339-4350, 2013.

[79] M. Liserre, F. Blaabjerg, and S. Hansen, "Design and control of an LCL-filter-based three-phase active rectifier," *Industry Applications, IEEE Transactions on,* vol. 41, pp. 1281-1291, 2005.

[80] P. A. Dahono, "A control method to damp oscillation in the input LC filter," in *Power Electronics Specialists Conference, 2002. pesc 02. 2002 IEEE 33rd Annual*, 2002, pp. 1630-1635.

[81] Y. Wenli, Y. Yongheng, Z. Xiaobin, and F. Blaabjerg, "Digital notch filter based active damping for LCL filters," in *Applied Power Electronics Conference and Exposition (APEC), 2015 IEEE*, 2015, pp. 2399-2406.

[82] D. Holmes and T. Lipo, "Pulse Width Modulation for Power Converters: Principles and Practice," ed: Wiley-IEEE Press, 2003.

[83] N. Mohan, T. M. Undeland, and W. P. Robbins, "Power Electronics: Converters, Applications and Design," 3 ed: John Wiley & Sons, Inc., 2003.

[84] Magnetics - Spang, A Critical Comparison of Ferrites with Other Magnetic Materials.

[85] P. R. Wilson and R. Wilcock, "Frequency dependent model of leakage inductance for magnetic components," *Advanced Electromagnetics,* vol. 1, no. 3, 2006.

[86] Vishay Roederstein, General Technical Information - Film Capacitors, 2012.

[87] "The Electricity Safety, Quality and Continuity Regulations 2002," ed.

[88] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," *Industry Applications, IEEE Transactions on,* vol. 41, pp. 1292-1306, 2005.

[89] F. Krismer and J. W. Kolar, "Closed Form Solution for Minimum Conduction Loss Modulation of DAB Converters," *Power Electronics, IEEE Transactions on,* vol. 27, pp. 174-188, 2012.

[90] G. G. Oggier, R. Ledhold, G. O. Garcia, A. R. Oliva, J. C. Balda, and F. Barlow, "Extending the ZVS Operating Range of Dual Active Bridge High-Power DC-DC Converters," in *Power Electronics Specialists Conference, 2006. PESC '06. 37th IEEE*, 2006, pp. 1-7.

[91] Z. Haihua and A. M. Khambadkone, "Hybrid Modulation for Dual-Active-Bridge Bidirectional Converter With Extended Power Range for Ultracapacitor Application," *Industry Applications, IEEE Transactions on,* vol. 45, pp. 1434-1442, 2009.

[92] G. Guidi, M. Pavlovsky, A. Kawamura, T. Imakubo, and Y. Sasaki, "Improvement of light load efficiency of Dual Active Bridge DC-DC converter by using dual leakage transformer and variable frequency," in *Energy Conversion Congress and Exposition (ECCE), 2010 IEEE*, 2010, pp. 830-837.

[93] G. G. Oggier, G. O. Garcia, and A. R. Oliva, "Modulation strategy to operate the dual active bridge DC-DC converter under soft switching in the whole operating range," *Power Electronics, IEEE Transactions on,* vol. 26, pp. 1228-1236, 2011.

[94] Y. Wang, S. W. H. De Haan, and J. A. Ferreira, "Optimal operating ranges of three modulation methods in dual active bridge converters," in *Power Electronics and Motion Control Conference, 2009. IPEMC '09. IEEE 6th International*, 2009, pp. 1397-1401.

[95] J. Everts, F. Krismer, J. Van den Keybus, J. Driesen, and J. W. Kolar, "Optimal ZVS Modulation of Single-Phase Single-Stage Bidirectional DAB AC–DC Converters," *Power Electronics, IEEE Transactions on,* vol. 29, pp. 3954-3970, 2014.

[96] F. Krismer, S. Round, and J. W. Kolar, "Performance Optimization of a High Current Dual Active Bridge with a Wide Operating Voltage Range," in *Power Electronics Specialists Conference, 2006. PESC '06. 37th IEEE*, 2006, pp. 1-7.

[97] J. Hiltunen, V. Vaisanen, R. Juntunen, and P. Silventoinen, "Variable-Frequency Phase Shift Modulation of a Dual Active Bridge Converter," *Power Electronics, IEEE Transactions on,* vol. PP, pp. 1-1, 2015.

[98] K. D. Hoang and J. Wang, "Design optimization of high frequency transformer for dual active bridge DC-DC converter," in *Electrical Machines (ICEM), 2012 XXth International Conference on*, 2012, pp. 2311-2317.

[99] D. Graovac and M. Purschel, "IGBT Power Losses Calculation Using the Data-Sheet Parameters," Infineon, Neubiberg, Germany, Appl. NoteJan. 2009.

[100] D. Graovac, M. Purschel, and A. Kiep, "MOSFET Power Losses Calculation Using the Data-Sheet Parameters," Infineon, Neubiberg, Germany, Appl. NoteJul. 2006.

[101] F. Krismer and J. W. Kolar, "Accurate Small-Signal Model for the Digital Control of an Automotive Bidirectional Dual Active Bridge," *Power Electronics, IEEE Transactions on,* vol. 24, pp. 2756-2768, 2009.

[102] C. Zhao, S. D. Round, and J. W. Kolar, "Full-order averaging modelling of zero-voltage-switching phase-shift bidirectional DC-DC converters," *Power Electronics, IET,* vol. 3, pp. 400-410, 2010.

[103] Q. Hengsi and J. W. Kimball, "Generalized Average Modeling of Dual Active Bridge DC/DC Converter," *Power Electronics, IEEE Transactions on,* vol. 27, pp. 2078-2084, 2012.

[104] B. Hua, M. Chunting, W. Chongwu, and S. Gargies, "The dynamic model and hybrid phase-shift control of a dual-active-bridge converter," in *Industrial Electronics, 2008. IECON 2008. 34th Annual Conference of IEEE*, 2008, pp. 2840-2845.

[105] H. K. Krishnamurthy and R. Ayyanar, "Building Block Converter Module for Universal (AC-DC, DC-AC, DC-DC) Fully Modular Power Conversion Architecture," in *Power Electronics Specialists Conference, 2007. PESC 2007. IEEE*, 2007, pp. 483-489.

[106] D. Segaran, B. P. McGrath, and D. G. Holmes, "Adaptive dynamic control of a bi-directional DC-DC converter," in *Energy Conversion Congress and Exposition (ECCE), 2010 IEEE*, 2010, pp. 1442-1449.

[107] H. Qin, "Dual active bridge converters in solid state transformers," PhD thesis, Missouri University of Science and Technology, Rolla, USA, 2012.

[108] Q. Hengsi and J. W. Kimball, "Closed-loop control of DC-DC dual active bridge converters driving single-phase inverters," in *Energy Conversion Congress and Exposition (ECCE), 2012 IEEE*, 2012, pp. 173-179.

[109] Q. Hengsi and J. W. Kimball, "Closed-Loop Control of DC/DC Dual-Active-Bridge Converters Driving Single-Phase Inverters," *Power Electronics, IEEE Transactions on,* vol. 29, pp. 1006-1017, 2014.

[110] Z. Jia and L. Chen, "Design of a bidirectional power interface for V2G technology with smaller DC-link capacitance," *International Journal of Smart Grid and Clean Energy,* vol. 3, pp. 104-110, 2013.

[111] X. Lingxiao, D. Diaz, S. Zhiyu, L. Fang, P. Mattavelli, and D. Boroyevich, "Dual active bridge based battery charger for plug-in hybrid electric vehicle with charging current containing low frequency ripple," in *Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE*, 2013, pp. 1920-1925.

[112] D.-K. Jeong, M.-H. Ryu, H.-G. Kim, and H.-J. Kim, "Optimized Design of Bi-Directional Dual Active Bridge Converter for Low-Voltage Battery Charger," *Journal of Power Electronics,* vol. 14, pp. 468-477, 2014.

[113] L. M. Miranda, D. Varajao, B. dos Santos, R. E. Araujo, C. L. Moreira, and J. A. P. Lopes, "Power flow control with bidirectional dual active bridge battery charger in low-voltage microgrids," in *Power Electronics and Applications (EPE), 2013 15th European Conference on*, 2013, pp. 1-10.

[114] S. Buso, L. Malesani, and P. Mattavelli, "Comparison of current control techniques for active filter applications," *Industrial Electronics, IEEE Transactions on,* vol. 45, pp. 722-729, 1998.

[115] M. P. Kazmierkowski and L. Malesani, "Current control techniques for three-phase voltage-source PWM converters: a survey," *Industrial Electronics, IEEE Transactions on,* vol. 45, pp. 691-703, 1998.

[116] M. Rukonuzzaman and M. Nakaoka, "Fuzzy logic current controller for three-phase voltage source PWM-inverters," in *Industry Applications Conference, 2000. Conference Record of the 2000 IEEE*, 2000, pp. 1163-1169 vol.2.

[117] M. P. Kazmierkowski, P. H. Viet, and M. A. Dzieniakowski, "Neural networks based current regulator for PWM inverters," in *Power Electronics and Applications, 1993., Fifth European Conference on*, 1993, pp. 186-189 vol.4.

[118] M. P. Kazmierkowski and D. Sobczuk, "Improved neural network current regulator for VS-PWM inverters," in *Industrial Electronics, Control and Instrumentation, 1994. IECON '94., 20th International Conference on*, 1994, pp. 1237-1241 vol.2.

[119] R. Wu, S. B. Dewan, and G. R. Slemon, "Analysis of a PWM AC to DC voltage source converter under the predicted current control with a fixed switching frequency," *Industry Applications, IEEE Transactions on,* vol. 27, pp. 756-764, 1991.

[120] L. Malesani, P. Mattavelli, and S. Buso, "Robust dead-beat current control for PWM rectifiers and active filters," in *Industry Applications Conference, 1998. Thirty-Third IAS Annual Meeting. The 1998 IEEE*, 1998, pp. 1377-1384 vol.2.

[121] Y. A. R. I. Mohamed and E. F. El-Saadany, "An Improved Deadbeat Current Control Scheme With a Novel Adaptive Self-Tuning Load Model for a Three-Phase PWM Voltage-Source Inverter," *Industrial Electronics, IEEE Transactions on,* vol. 54, pp. 747-759, 2007.

[122] R. Teodorescu and F. Blaabjerg, "Proportional-Resonant Controllers. A New Breed of Controllers Suitable for Grid-Connected Voltage-Source Converters," in *The 9th International Conference on Optimization of Electrical and Electronic Equipments, Optim 2004*, 2004, pp. 9-14.

[123] T. M. Rowan and R. J. Kerkman, "A New Synchronous Current Regulator and an Analysis of Current-Regulated PWM Inverters," *Industry Applications, IEEE Transactions on,* vol. IA-22, pp. 678-690, 1986.

[124] M. Liserre, A. Dell'Aquila, and F. Blaabjerg, "Design and control of a three-phase active rectifier under non-ideal operating conditions," in *Industry Applications Conference, 2002. 37th IAS Annual Meeting. Conference Record of the*, 2002, pp. 1181-1188 vol.2.

[125] D. N. Zmood and D. G. Holmes, "Stationary frame current regulation of PWM inverters with zero steady-state error," *Power Electronics, IEEE Transactions on,* vol. 18, pp. 814-822, 2003.

[126] C. Hui, Z. Hui, J. Wentao, and W. Santong, "Research on PQ Control Strategy for PV Inverter in the Unbalanced Grid," in *Power and Energy Engineering Conference (APPEEC), 2012 Asia-Pacific*, 2012, pp. 1-3.

[127] A. Roshan, R. Burgos, A. C. Baisden, F. Wang, and D. Boroyevich, "A D-Q Frame Controller for a Full-Bridge Single Phase Inverter Used in Small Distributed Power Generation Systems," in *Applied Power Electronics Conference, APEC 2007 - Twenty Second Annual IEEE*, 2007, pp. 641-647.

[128] B. Crowhurst, E. F. El-Saadany, L. El Chaar, and L. A. Lamont, "Single-phase grid-tie inverter control using DQ transform for active and reactive load power compensation," in *Power and Energy (PECon), 2010 IEEE International Conference on*, 2010, pp. 489-494.

[129] L. Zhigang, L. Alesi, Z. Xiaohu, and A. Q. Huang, "Digital controller development for grid-tied photovoltaic inverter with model based technique," in *Applied Power Electronics Conference and Exposition (APEC), 2010 Twenty-Fifth Annual IEEE*, 2010, pp. 849-853.

[130] S. Golestan, M. Monfared, and J. M. Guerrero, "A novel control technique for single-phase grid-connected inverters," in *Electrical Engineering and Informatics (ICEEI), 2011 International Conference on*, 2011, pp. 1-6.

[131] S. Golestan, M. Monfared, J. M. Guerrero, and M. Joorabian, "A D-Q synchronous frame controller for single-phase inverters," in *Power Electronics, Drive Systems and Technologies Conference (PEDSTC), 2011 2nd*, 2011, pp. 317-323.

[132] M. Saitou, N. Matsui, and T. Shimizu, "A control strategy of single-phase active filter using a novel d-q transformation," in *Industry Applications Conference, 2003. 38th IAS Annual Meeting. Conference Record of the*, 2003, pp. 1222-1227 vol.2.

[133] S. Fukuda and T. Yoda, "A novel current-tracking method for active filters based on a sinusoidal internal model [for PWM invertors]," *Industry Applications, IEEE Transactions on,* vol. 37, pp. 888-895, 2001.

[134] R. Teodorescu, F. Blaabjerg, U. Borup, and M. Liserre, "A new control structure for grid-connected LCL PV inverters with zero steady-state error and selective harmonic compensation," in *Applied Power Electronics Conference and Exposition, 2004. APEC '04. Nineteenth Annual IEEE*, 2004, pp. 580-586 Vol.1.

[135] R. Teodorescu, F. Blaabjerg, M. Liserre, and P. C. Loh, "Proportional-resonant controllers and filters for grid-connected voltage-source converters," *Electric Power Applications, IEE Proceedings,* vol. 153, pp. 750-762, 2006.

[136] A. V. Timbus, M. Ciobotaru, R. Teodorescu, and F. Blaabjerg, "Adaptive resonant controller for grid-connected converters in distributed power generation systems," in *Applied Power Electronics Conference and Exposition, 2006. APEC '06. Twenty-First Annual IEEE*, 2006, p. 6 pp.

[137] P. Mattavelli and S. Fasolo, "A closed-loop selective harmonic compensation for active filters," in *Applied Power Electronics Conference and Exposition, 2000. APEC 2000. Fifteenth Annual IEEE*, 2000, pp. 399-405 vol.1.

[138] M. Liserre, R. Teodorescu, and F. Blaabjerg, "Multiple harmonics control for three-phase grid converter systems with the use of PI-RES current controller in a rotating frame," *Power Electronics, IEEE Transactions on,* vol. 21, pp. 836-841, 2006.

[139] M. Castilla, J. Miret, J. Matas, L. Garcia de Vicuna, and J. M. Guerrero, "Control Design Guidelines for Single-Phase Grid-Connected Photovoltaic Inverters With Damped Resonant Harmonic Compensators," *Industrial Electronics, IEEE Transactions on,* vol. 56, pp. 4492-4501, 2009.

[140] R. Bojoi, L. R. Limongi, F. Profumo, D. Roiu, and A. Tenconi, "Analysis of current controllers for active power filters using selective harmonic compensation schemes.," *IEEJ Trans Elec Electron Eng,* vol. 4, pp. 139-157, 2009.

[141] R. C. Cope and Y. Podrazhansky, "The art of battery charging," in *Battery Conference on Applications and Advances, 1999. The Fourteenth Annual*, 1999, pp. 233-235.

[142] H. Guan-Chyun, C. Liang-Rui, and H. Kuo-Shun, "Fuzzy-controlled Li-ion battery charge system with active state-of-charge controller," *Industrial Electronics, IEEE Transactions on,* vol. 48, pp. 585-593, 2001.

[143] H. A. H. Hussein and I. Batarseh, "A Review of Charging Algorithms for Nickel and Lithium Battery Chargers," *Vehicular Technology, IEEE Transactions on,* vol. 60, pp. 830-838, 2011.

[144] C. Liang-Rui, R. C. Hsu, and L. Chuan-Sheng, "A Design of a Grey-Predicted Li-Ion Battery Charge System," *Industrial Electronics, IEEE Transactions on,* vol. 55, pp. 3692-3701, 2008.

[145] S. Weixiang, V. Thanh Tu, and A. Kapoor, "Charging algorithms of lithium-ion batteries: An overview," in *Industrial Electronics and Applications (ICIEA), 2012 7th IEEE Conference on*, 2012, pp. 1567-1572.

[146] T. Nussbaumer, M. L. Heldwein, G. Guanghai, S. D. Round, and J. W. Kolar, "Comparison of Prediction Techniques to Compensate Time Delays Caused by Digital Control of a Three-Phase Buck-Type PWM Rectifier System," *Industrial Electronics, IEEE Transactions on,* vol. 55, pp. 791-799, 2008.

[147] A. Kotsopoulos, J. L. Duarte, and M. A. M. Hendrix, "Predictive DC voltage control of single-phase PV inverters with small DC link capacitance," in *Industrial Electronics, 2003. ISIE '03. 2003 IEEE International Symposium on*, 2003, pp. 793-797 vol. 2.

[148] C. Meza, J. J. Negroni, D. Biel, and F. Guinjoan, "Energy-Balance Modeling and Discrete Control for Single-Phase Grid-Connected PV Central Inverters," *Industrial Electronics, IEEE Transactions on,* vol. 55, pp. 2734-2743, 2008.

[149] H. Fanbo, Z. Zhengming, Y. Liqiang, and L. Sizhao, "A DC-link voltage control scheme for single-phase grid-connected PV inverters," in *Energy Conversion Congress and Exposition (ECCE), 2011 IEEE*, 2011, pp. 3941-3945.

[150] H. S. Bae, S. J. Lee, K. S. Choi, B. H. Cho, and S. S. Jang, "Current Control Design for a Grid Connected Photovoltaic/Fuel Cell DC-AC Inverter," in *Applied Power Electronics Conference and Exposition, 2009. APEC 2009. Twenty-Fourth Annual IEEE*, 2009, pp. 1945-1950.

[151] R. A. Mastromauro, M. Liserre, and A. D. Aquila, "Study of the Effects of Inductor Nonlinear Behavior on the Performance of Current Controllers for Single-Phase PV Grid Converters," *Industrial Electronics, IEEE Transactions on,* vol. 55, pp. 2043-2052, 2008.

[152] M. M. Begovic, P. M. Djuric, S. Dunlap, and A. G. Phadke, "Frequency tracking in power networks in the presence of harmonics," *Power Delivery, IEEE Transactions on,* vol. 8, pp. 480-486, 1993.

[153] D. Nedeljkovic, J. Nastran, D. Voncina, and V. Ambrozic, "Synchronization of active power filter current reference to the network," *Industrial Electronics, IEEE Transactions on,* vol. 46, pp. 333-339, 1999.

[154] R. Weidenbrug, F. P. Dawson, and R. Bonert, "New synchronization method for thyristor power converters to weak AC-systems," *Industrial Electronics, IEEE Transactions on,* vol. 40, pp. 505-511, 1993.

[155] R. W. Wall, "Simple methods for detecting zero crossing," in *Industrial Electronics Society, 2003. IECON '03. The 29th Annual Conference of the IEEE*, 2003, pp. 2477-2481 Vol.3.

[156] P. Rodriguez, A. Luna, M. Ciobotaru, R. Teodorescu, and F. Blaabjerg, "Advanced Grid Synchronization System for Power Converters under Unbalanced and Distorted Operating Conditions," in *IEEE Industrial Electronics, IECON 2006 - 32nd Annual Conference on*, 2006, pp. 5173-5178.

[157] A. E. V., "The automatic synchronization of triode oscillators," *Proceedings of the Cambridge Philosophical Society,* vol. 21, pp. 231-248, 1923.

[158] Gardner and F. M, "Phaselock Techniques," ed: John Wiley & Sons Inc, 1966.

[159] Gardner and F. M, "Phaselock Techniques," Second Edition ed: John Wiley & Sons Inc, 1979.

[160] R. M. Santos Filho, P. F. Seixas, P. C. Cortizo, L. A. B. Torres, and A. F. Souza, "Comparison of Three Single-Phase PLL Algorithms for UPS Applications," *Industrial Electronics, IEEE Transactions on,* vol. 55, pp. 2923-2932, 2008.

[161] T. Thacker, D. Boroyevich, R. Burgos, and F. Wang, "Phase-Locked Loop Noise Reduction via Phase Detector Implementation for Single-Phase Systems," *Industrial Electronics, IEEE Transactions on,* vol. 58, pp. 2482-2490, 2011.

[162] M. Karimi-Ghartemani and M. R. Iravani, "A nonlinear adaptive filter for online signal analysis in power systems: applications," *Power Delivery, IEEE Transactions on,* vol. 17, pp. 617-622, 2002.

[163] V. Kaura and V. Blasko, "Operation of a phase locked loop system under distorted utility conditions," *Industry Applications, IEEE Transactions on,* vol. 33, pp. 58-63, 1997.

[164] S. M. Silva, B. M. Lopes, B. J. C. Filho, R. P. Campana, and W. C. Bosventura, "Performance evaluation of PLL algorithms for single-phase grid-connected systems," in *Industry Applications Conference, 2004. 39th IAS Annual Meeting. Conference Record of the 2004 IEEE*, 2004, pp. 2259-2263 vol.4.

[165] S. Golestan, M. Monfared, F. D. Freijedo, and J. M. Guerrero, "Dynamics Assessment of Advanced Single-Phase PLL Structures," *Industrial Electronics, IEEE Transactions on,* vol. 60, pp. 2167-2177, 2013.

[166] H. Sharma, P. Keebler, F. Sharp, M. Josef, and J. Price, "Handling excessive third harmonics in utility systems due to proliferation of non-linear loads," in *Power and Energy Society General Meeting, 2012 IEEE*, 2012, pp. 1-7.

[167] J. Niitsoo, I. Palu, J. Kilter, P. Taklaja, and T. Vaimann, "Residential load harmonics in distribution grid," in *Electric Power and Energy Conversion Systems (EPECS), 2013 3rd International Conference on*, 2013, pp. 1-6.

[168] M. Abramowitz and I. A. Stegun, "Handbook of mathematical functions," ed: United States Department of Commerce, 1964, p. 361.

[169] K. Ogata, "Modern Control Engineering," 5 ed: Prentice Hall, 2010.

[170] T. Edo, private communication, October 2013.

[171] W. Bower and M. E. Ropp, "Evaluation Of Islanding Detection Methods For Photovoltaic Utility-Interactive Power Systems," *Rep. IEA-PVPS T5-09:2002,* Mar. 2002.

[172] "IEEE Standard for Interconnecting Distributed Resources with Electric Power Systems," *IEEE Std 1547-2003,* pp. 1-28, 2003.

[173] Y. Zhihong, A. Kolwalkar, Y. Zhang, D. Pengwei, and R. Walling, "Evaluation of anti-islanding schemes based on nondetection zone concept," in *Power Electronics Specialist Conference, 2003. PESC '03. 2003 IEEE 34th Annual*, 2003, pp. 1735-1741 vol.4.

[174] M. E. Ropp, M. Begovic, A. Rohatgi, G. A. Kern, R. H. Bonn, Sr., and S. Gonzalez, "Determining the relative effectiveness of islanding detection methods using

phase criteria and nondetection zones," *Energy Conversion, IEEE Transactions on,* vol. 15, pp. 290-296, 2000.

[175] H. Kobayashi and K. Takigawa, "Statistical evaluation of optimum islanding preventing method for utility interactive small scale dispersed PV systems," in *Photovoltaic Energy Conversion, 1994., Conference Record of the Twenty Fourth. IEEE Photovoltaic Specialists Conference - 1994, 1994 IEEE First World Conference on*, 1994, pp. 1085-1088 vol.1.

[176] F. De Mango, M. Liserre, A. D. Aquila, and A. Pigazo, "Overview of Anti-Islanding Algorithms for PV Systems. Part I: Passive Methods," in *Power Electronics and Motion Control Conference, 2006. EPE-PEMC 2006. 12th International*, 2006, pp. 1878-1883.

[177] J. Sung-Il and K. Kwang-Ho, "An islanding detection method for distributed generations using voltage unbalance and total harmonic distortion of current," *Power Delivery, IEEE Transactions on,* vol. 19, pp. 745-752, 2004.

[178] B. Guha, R. J. Haddad, and Y. Kalaani, "A passive islanding detection approach for inverter-based distributed generation using rate of change of frequency analysis," in *SoutheastCon 2015*, 2015, pp. 1-6.

[179] H. Kobayashi, K. Takigawa, E. Hashimoto, A. Kitamura, and H. Matsuda, "Method for preventing islanding phenomenon on utility grid with a number of small scale PV systems," in *Photovoltaic Specialists Conference, 1991., Conference Record of the Twenty Second IEEE*, 1991, pp. 695-700 vol.1.

[180] L. Soo-Hyoung and P. Jung-Wook, "New Islanding Detection Method for Inverter-Based Distributed Generation Considering Its Switching Frequency," *Industry Applications, IEEE Transactions on,* vol. 46, pp. 2089-2098, 2010.

[181] S. Yuyama, T. Ichinose, K. Kimoto, T. Itami, T. Ambo, C. Okado*, et al.*, "A high speed frequency shift method as a protection for islanding phenomena of utility interactive PV systems," *Solar Energy Materials and Solar Cells,* vol. 35, pp. 477-486, 9/11/ 1994.

[182] M. E. Ropp, M. Begovic, and A. Rohatgi, "Analysis and performance assessment of the active frequency drift method of islanding prevention," *Energy Conversion, IEEE Transactions on,* vol. 14, pp. 810-816, 1999.

[183] P. Sanchis, L. Marroyo, and J. Coloma, "Design methodology for the frequency shift method of islanding prevention and analysis of its detection capability," *Progress in Photovoltaics: Research and Applications,* vol. 13, pp. 409-428, 2005.

[184] J. W. Stevens III, R. J. Bonn, J. W. Ginn, S. Gonzalez, and G. Kern, "Development and Testing of an Approach to Anti-Islanding in Utility-Interconnected Photovoltaic Systems," SAND2000-1939 TRN: AH200036%%55, 2000.

[185] Z. Ye, R. Walling, L. Garces, R. Zhou, L. Li, and T. Wang, "Study and Development of Anti-Islanding Control for Grid-Connected Inverters," NREL/SR-560-36243, 2004.

[186] W. Bower and M. E. Ropp, "Evaluation of Islanding Detection Methods for Utility-Interactive Inverters in Photovoltaic Systems," SAND2002-3591, 2002.

[187] F. De Mango, M. Liserre, and A. D. Aquila, "Overview of Anti-Islanding Algorithms for PV Systems. Part II: ActiveMethods," in *Power Electronics and Motion Control Conference, 2006. EPE-PEMC 2006. 12th International*, 2006, pp. 1884-1889.

[188] K. Jae-Hyung, K. Jun-Gu, J. Young-Hyok, J. Yong-Chae, and W. Chung-Yuen, "An Islanding Detection Method for a Grid-Connected System Based on the Goertzel Algorithm," *Power Electronics, IEEE Transactions on,* vol. 26, pp. 1049-1055, 2011.

[189] L. Faa-Jeng, T. Kuang-Hsiung, and C. Jian-Hsing, "Active islanding detection method using wavelet fuzzy neural network," in *Fuzzy Systems (FUZZ-IEEE), 2012 IEEE International Conference on*, 2012, pp. 1-8.

[190] D. Reigosa, F. Briz, C. Blanco, P. Garcia, and J. M. Guerrero, "Active islanding detection using high frequency signal injection," in *Energy Conversion Congress and Exposition (ECCE), 2011 IEEE*, 2011, pp. 2183-2190.

[191] D. D. Reigosa, F. Briz, C. B. Charro, P. Garcia, and J. M. Guerrero, "Active Islanding Detection Using High-Frequency Signal Injection," *Industry Applications, IEEE Transactions on,* vol. 48, pp. 1588-1597, 2012.

[192] Y. Zhihong, L. Li, L. Garces, C. Wang, R. Zhang, M. Dame*, et al.*, "A new family of active antiislanding schemes based on DQ implementation for grid-connected

inverters," in *Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual*, 2004, pp. 235-241 Vol.1.

[193] C. Jeraputra and P. N. Enjeti, "Development of a robust anti-islanding algorithm for utility interconnection of distributed fuel cell powered generation," *Power Electronics, IEEE Transactions on,* vol. 19, pp. 1163-1170, 2004.

[194] Z. Jun, X. Dehong, S. Guoqiao, Z. Ye, H. Ning, and M. Jie, "An Improved Islanding Detection Method for a Grid-Connected Inverter With Intermittent Bilateral Reactive Power Variation," *Power Electronics, IEEE Transactions on,* vol. 28, pp. 268-278, 2013.

[195] M. Ciobotaru, V. Agelidis, and R. Teodorescu, "Accurate and less-disturbing active anti-islanding method based on PLL for grid-connected PV Inverters," in *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE*, 2008, pp. 4569-4576.

[196] Este, x, E. J. banez, V. M. Moreno, A. Pigazo, M. Liserre*, et al.*, "Performance Evaluation of Active Islanding-Detection Algorithms in Distributed-Generation Photovoltaic Systems: Two Inverters Case," *Industrial Electronics, IEEE Transactions on,* vol. 58, pp. 1185-1193, 2011.

[197] I. V. Banu, M. Istrate, D. Machidon, and R. Pantelimon, "A study on anti-islanding detection algorithms for grid-tied photovoltaic systems," in *Optimization of Electrical and Electronic Equipment (OPTIM), 2014 International Conference on*, 2014, pp. 655-660.

[198] A. Pigazo, M. Liserre, R. A. Mastromauro, V. M. Moreno, and A. Dell'Aquila, "Wavelet-Based Islanding Detection in Grid-Connected PV Systems," *Industrial Electronics, IEEE Transactions on,* vol. 56, pp. 4445-4455, 2009.

[199] M. V. G. Reis, T. A. S. Barros, A. B. Moreira, P. S. F. Nascimento, E. F. Ruppert, and M. G. Villalva, "Analysis of the Sandia Frequency Shift (SFS) Islanding Detection Method with a Single-Phase Photovoltaic Distributed Generation System," in *Innovative Smart Grid Technologies Conference, Latin America, 2015*, 2015.

[200] H. T. Yang, P. C. Peng, T. Y. Tsai, and Y. Y. Hong, "An improved Active Islanding Detection Technology for Grid-connected Solar Photovoltaic System," in *International Conference on Power Systems Transients (IPST2009)*, 2009.

[201] J. Yiding, S. Qiang, and L. Wenhua, "Anti-islanding protection for distributed generation systems based on reactive power drift," in *Industrial Electronics, 2009. IECON '09. 35th Annual Conference of IEEE*, 2009, pp. 3970-3975.

[202] J. Biela, U. Badstubner, and J. W. Kolar, "Design of a 5kW, 1U, 10kW/ltr. resonant DC-DC converter for telecom applications," in *Telecommunications Energy Conference, 2007. INTELEC 2007. 29th International*, 2007, pp. 824-831.

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