Characterization of growth of GaAs on Si/SiO_2 via a thin layer of perovskite

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Acronyms

ADF	Annular Dark-Field
AFM	Atomic Force Microscopy
APD	Anti-phase Domain
APB	Anti-phase Boundary
ART	Aspect Ratio Trapping
BF	Bright-Field
CCD	Charge Coupled Device
c-FEG	cold Field-Emission Gun
CTF	Contrast Transfer Factor
DF	Dark-Field
EDXs	Energy Dispersive X-ray spectroscopy
EELS	Electron Energy-Loss Spectroscopy
ELOG	Epitaxial Lateral Over-Growth
FACELO	FAcet-Controlled ELOG
FCC	Face-Centred Cubic
FIELO	Facet-Initiated Epitaxial Lateral Over-growth
FWHM	Full Width at Half Maximum
HAADF	High angle ADF
hMBE	hybrid Molecular Beam Epitaxy
LM	Light Microscope
MBE	Molecular Beam Epitaxy
MEE	Migration-Enhanced Epitaxy

MOCVD	Metal-Organic Chemical Vapour Deposition
PLD	Pulsed Laser Deposition
RHEED	Reflection High-Energy Electron Diffraction
RMS	Root Mean Squared
SAD	Selected Area Diffraction
SLS	Strained Layer Superlattice
S-FEG	Schottky Field-Emission Gun
STEM	Scanning Transmission Electron Microscopy
STM	Scanning Tunnelling Microscopy
TEM	Transmission Electron Microscopy
UHV	Ultra-High Vacuum

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Table of Contents

Published work i

Acronyms ii

Acknowledgment iv

Abstract 1

Chapter 1: Introduction 3

Chapter 2: Previous Studies 5

2.1. Introduction 5

2.2. Atomic structure of Si and GaAs 6

2.3. Why compound materials instead of silicon 7

2.4. Different methods of growing III-V compound materials on silicon 8

2.4.1. Insertion of strained layer superlattice 9

2.4.2. Growth on compositionally graded SiGe buffers 11

2.4.3. Cycle thermal annealing 12

2.4.4. Epitaxial lateral over-growth 12

2.4.5. Selective area epitaxy 14

2.4.6. Growth via perovskite layers 15

2.5. What is perovskite structure? 15

2.6. Growth of perovskite on silicon 18

2.7. Perovskite materials and GaAs interface 20

Chapter 3: Experimental Techniques **23**
3.1.Introduction 23
3.2. Growth methods 23
3.2.1. Pulsed laser deposition (PLD) 24
3.2.2. Molecular beam epitaxy (MBE) 26
Reflection High-Energy Electron Diffraction (RHEED) 28
3.3. Transmission Electron Microscopy (TEM) 30
3.3.1. Structure of the TEM instrument 32
Illumination system 32
Specimen stage 33
Image forming system 33
Image recording system 36
3.3.2. TEM techniques 37
High resolution transmission electron microscopy (HRTEM) 38
Scanning transmission electron microscopy (STEM) 40
Energy dispersive X-ray spectroscopy (EDXS) 43
3.3.3. TEM sample preparation 44
Conventional cross-section preparation 45
Ion milling 45
3.4. Atomic force microscopy (AFM) 47
3.5. Ellipsometry 48
Chapter 4: Investigation and characterization of as-deposited titanate ... **50**
4.1. Introduction 50
4.2. Experimental works 51

4.3. Results and discussion of as-grown layer structures 52

4.4. Conclusion 66

Chapter 5: Anneal strategies to re-crystallize perovskite layers 68

5.1. Introduction 68

5.2. Basics of surface reconstruction 69

5.2.1. Surface reconstructions of Si 69

5.2.2. Surface reconstructions of perovskite materials 71

5.3. Calibration the temperature of the MBE system 74

5.4. Results and discussion of post-anneal surface analysis of perovskite sample 77

5.5. Conclusion 87

Chapter 6: Characterization of growth of GaAs on Si/SiO_2 via a thin layer of perovskite 89

6.1. Introduction 89

6.2. Experimental works 90

6.3. Results and discussion of GaAs over-grown 91

6.3.1. Results and discussion of sample STO675GaAs 95

6.3.2. Results and discussion of sample STO825GaAs 103

6.3.3. Results and discussion of sample STO790GaAs 107

6.4. Conclusion 113

Chapter 7: Conclusion and outlook 115

References 120

Appendix 126

Abstract

Wafers of silicon (Si) are the standard material for deposition of thin layers used for all electronic devices; however, Si has an indirect band-gap and is thus not very efficient for optical applications. Gallium arsenide (GaAs) is much more expensive than Si, but due to its direct band-gap it is widely used for light-emitting and laser diodes. One approach towards an integrated optoelectronics with high efficiency is to grow GaAs on Si. Due to lattice mismatch, direct epitaxy of GaAs on Si leads to strain and so to dislocations and other defects detrimental to high-quality thin layers. There are various approaches for epitaxy of GaAs on Si, and this project investigates one of them.

The purpose of this research has been investigating and characterizing the growth of GaAs on Si via thin layers of perovskites on top of native silicon oxide. The idea that motivated this study was a allegation by Motorola in 2001 [1], aiming at commercialising this route for high frequency wireless and opto-electronic devices.

Pulsed laser deposition (PLD) of thin layers of perovskite materials ($SrTiO_3$ and $BaTiO_3$) on Si(001) substrates via layers of native oxide was performed at the Technische Universität Darmstadt, Germany. The wafers then have been sent back to the University of Sheffield. The as-grown materials have been investigated using different techniques such as atomic force microscopy (AFM), scanning transmission electron microscopy (STEM) and ellipsometry. Then they have been annealed and over-grown at the National Centre for III-V Technologies at the University of Sheffield using a combined molecular beam epitaxy (MBE)-scanning tunnelling microscopy (STM) system with built-in reflection high energy electron diffraction (RHEED). The over-grown specimens have finally again been investigated using AFM, TEM, STEM and

energy dispersive X-ray spectroscopy (EDXs) techniques. Here, particular emphasis has been on correlating quantitatively surface topology measurements by AFM with interface roughness measurements on cross-sectioned samples in STEM.

The aim of this study was to find a way to over-grow silicon substrates with GaAs with low dislocation density, however, the perovskite layers and the subsequent GaAs never grew epitaxially but always remained poly-crystalline. This has been attributed to a lack of surface reconstruction of the perovskite layers when annealed under vacuum conditions, as confirmed by in-situ RHEED. Other studies have used sulphide buffer layer [2] or a relaxed buffer layer of $Ba_xSr_{1-x}TiO_3$ [3] to guarantee the perovskite thin layer to grow epitaxially. The over-growth of GaAs also has been done with the presence of oxygen to prevent the perovskite to evaporate.

Chapter 1
Introduction

Silicon is a cheap reliable material which is commonly used in semiconductor industry as a substrate and III-V compound materials mostly have better carrier mobility and direct band-gap which are useful in opto-electronic devices. The aim of this study is to characterize the growth of III-V compound materials on silicon substrate via a thin layer of perovskite for future studies to combine the useful properties of silicon and III-V materials.

In chapter 2, I have looked back at the history of growth of III-V compound materials on Si. Different growth methods such as insertion of strained layer superlattice, cycle thermal annealing, epitaxial lateral over-growth, growth on compositionally graded SiGe buffers, selective area epitaxy and growth via perovskite intermediate layer have been briefly introduced. Also the crystal structure of perovskite and previous studies on growth of these oxide materials on silicon and GaAs are reviewed.

In chapter 3, all the experimental techniques used in this study are introduced and explained in detail. Different parts of TEM as the main microscopy technique used in this project are explained specially STEM which is the main imaging technique in this work. AFM and ellipsometry as alternative ways of studying the surface of materials are discussed in detail as well. As the thin perovskite layer has been grown using PLD in the Technische Universität Darmstadt, a brief introduction on PLD is included. The anneal process and over-growth of GaAs have been done in a MBE chamber and RHEED is used to observe the process at the last stage of this project, therefore these two techniques are briefly explained at the end of this chapter as well.

In chapter 4, experimental results of characterization of the growth of thin perovskite layer on silicon via native oxide using STEM, AFM and ellipsometry are gathered and compared. In this chapter, it has been showed that the perovskite layers have been grown polycrystalline on top of native oxide rather than epitaxially.

In chapter 5, after a brief study of reconstruction of silicon surface as well as perovskite, surface studies of a pure $SrTiO_3$ before and after anneal process in a MBE chamber are gathered and discussed to find a suitable strategy to anneal the original samples to re-crystalline the perovskite layers.

In chapter 6, the final part of this study is explained and analysed. The silicon substrates with perovskite layers on top have been annealed in MBE with different temperatures and then over-grown with GaAs (with a same recipe for all of them). TEM as well as STEM, EDXs and AFM have been used to analyse the annealed and over-grown samples. It has been shown that none of the anneal temperatures have been affected the perovskite layer to become mono-crystalline and therefore the GaAs layers on top have been grown as polycrystalline materials as well. Surface roughness studies have been done at this stage of the project, on the surface of GaAs layer using both STEM image analysis and AFM analysis.

On the last chapter (chapter 7), I have concluded my studies and experiments and have given my thoughts and suggestions to continue this work in the future steps.

Chapter 2:
Previous Studies

2.1 Introduction

To achieve higher speed in silicon-based electronic devices, the gate oxide thickness in the device should be as thin as possible and therefore by the time it is being shrunk to reduce the distance that carriers should travel in the device. Typical gate oxide thickness is ~1nm at present which is ~5 monolayers in silicon. To avoid the phenomenon of electron tunnelling, other materials started to be used for electronic devices with lower effective masses of charge carriers and therefore higher mobility. III-V compound semiconductors are suitable replacements for Si in electronic device industry with the carrier mobility much higher than Si. They also have direct band-gaps which makes them more attractive for use in electronic and opto-electronic applications. However, silicon is still the best choice to use as substrate in semiconductor devices due to its cost and availability of standard processing techniques. These useful properties can be combined and used in heterostructures. Hence, epitaxial growth of III-V compound materials, specially arsenides, and nitrides on Si has been studied during recent years.

There has been limited success in direct growth of III-V semiconductors on silicon although there have been several reports of basic and initial progress of this method [4,5,6,7]. The main problem is the 4.1% lattice mismatch between Si and GaAs as well as the difference in their thermal expansion coefficients.

In this chapter atomic structure of Si and GaAs and previous studies on growth of III-V compound materials on Si are presented and briefly discussed. As the

main subject of this work is investigating the growth of III-V materials on Si via an intermediate thin layer of perovskite, the atomic structure of the unit cell of the perovskite materials is explained and growth of $SrTiO_3$ and other perovskite materials on silicon as well as growth of III-V materials on perovskite is discussed in more detail.

2.2 Atomic structure of Si and GaAs

For a better understanding of growth of III-V compound semiconductors on silicon, the lattice structure of both is introduced in this part of the chapter.

Silicon has diamond cubic structure (shown in figure 2.1(a)). It consists of two face-centred cubic (fcc) crystals which are shifted by ¼ of the body diagonal. The atoms are tetrahedrally connected to their four neighbours, which are identical to each other.

GaAs has zinc blende structure. This structure is similar to the diamond cubic but the four nearest atoms to each individual atom are from the other element in the structure. For example in GaAs, the four nearest atoms sitting near a gallium atom are arsenic. In both diamond and zinc blende structures the number of atoms in a unit cell is calculated as below:

1 atom at 8 corners: $8\times\frac{1}{8}$

+3 atoms at centre of the faces: $6\times\frac{1}{2}$

+4 atoms at tetrahedral sites: 4×1

= 8

Figure 2.1(b) shows the zinc blende structure of GaAs in 3D and along <100> and <110> directions.

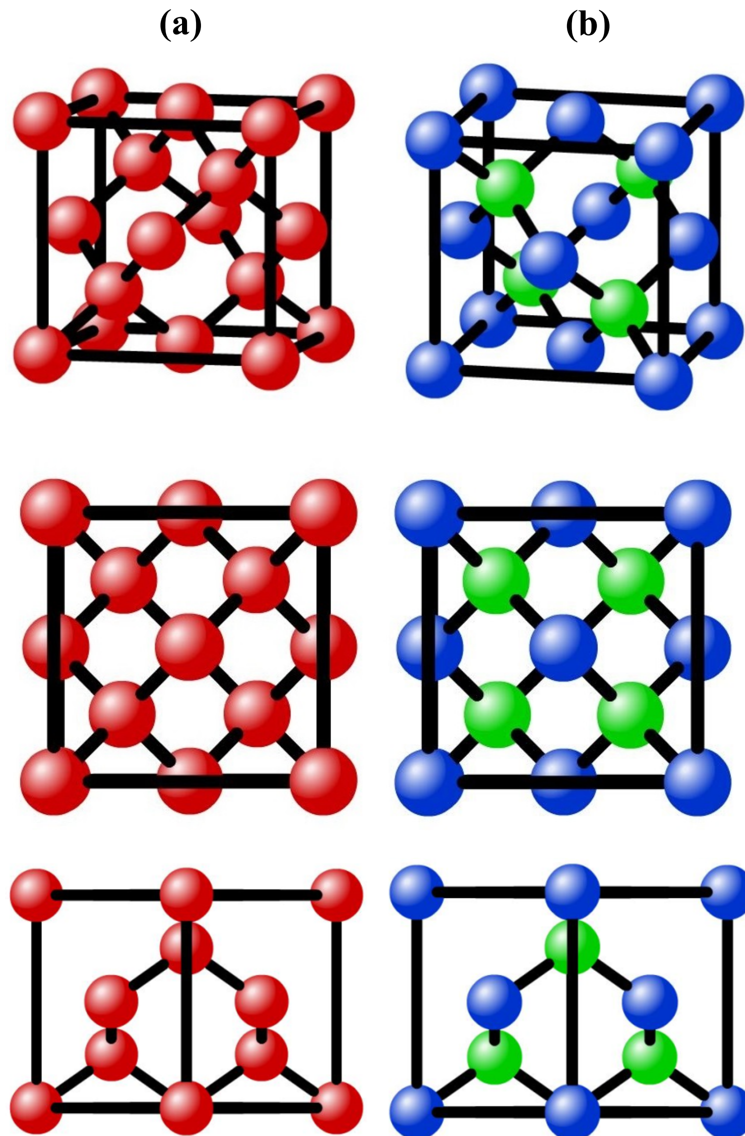


Figure 2.1. The unit cell structure of **(a)** silicon (diamond cubic) and **(b)** GaAs (zinc-blende). In 3D, along <100> and <110> directions respectively.

2.3 Why compound materials instead of Si?

Si has been the main material for electronic devices used for integrated circuits. But light emission is very difficult to achieve in silicon-based devices because silicon has an in-direct band-gap. Therefore III-V compound materials were introduced to replace silicon due to their direct band gap and higher carrier mobility.

Figure 2.2 shows a simple schematic of direct and in-direct band-gap in semiconductors.

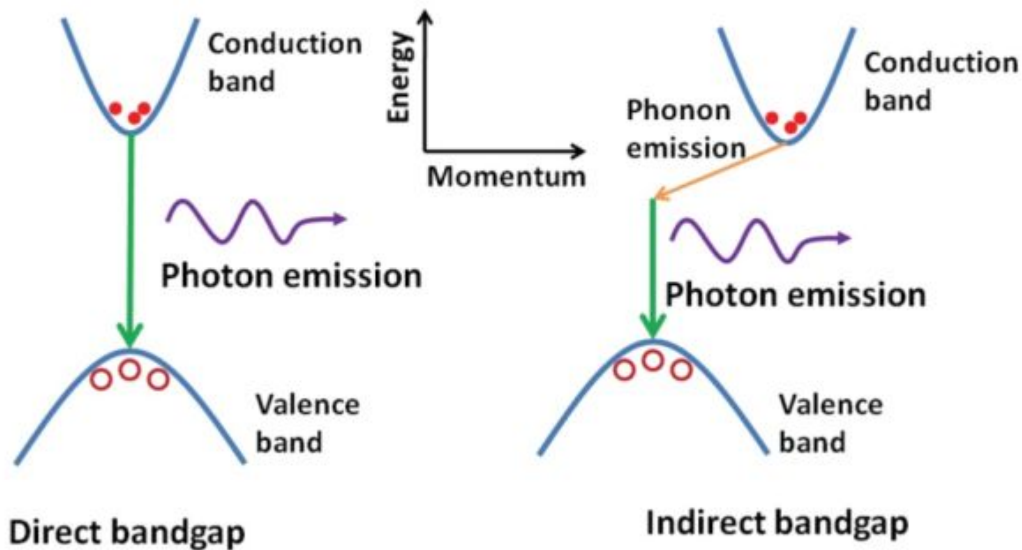


Figure 22. Schematic of direct and in-direct band-gap [8]

Combining the advantage of low cost of Si technology and high performance of III-V heterostructures expands the use of Si technology in optoelectronics [9].

2.4 Different methods of growing III-V compound materials on silicon

As mentioned before, growth of GaAs on Si has become important due to the useful properties of both materials. Si has good chemical stability and thermal properties and dominates the microelectronics market. On the other hand, GaAs also has an important role in today's semiconductor fabrication because of the high electron mobility compared to Si and the direct band gap, which makes it important for opto-electronics applications.

Because of the mismatch in lattice parameters of GaAs (*a*~5.65Å) and Si (*a*~5.43 Å), there usually is a large density of dislocations on the interface. It has been tried to epitaxially grow GaAs on Si with different methods [4] such as insertion of strained layer superlattices, growth on compositionally graded SiGe

buffer layers, cycle thermal annealing, epitaxial lateral overgrowth and selective-area epitaxy to somehow reduce these dislocation densities. These methods are briefly explained below.

2.4.1 Insertion of strained layer superlattices

Silicon has been the most important material in semiconductor industry because of various reasons such as its abundance on the earth, its ability to be grown into perfect single crystals and ultrahigh purity, its surface being able to oxidise and form a stable dielectric without any complicated processes with good mechanical properties [10]. The reason that other semiconductor materials such as III-V semiconductors are replacing silicon is that in certain devices and applications III-V compound materials show wider range of properties (for e.g. the chip in your iPhone is GaAs based). As mentioned, one of the important properties is that many III-V semiconductors have direct energy band-gaps, which means when electron and holes recombine, light is generated without the need for involving phonons, yielding higher transition probability. The main issue in combining silicon with other semiconductors is the mismatch between lattice constants, thermal expansion coefficients and also difference in chemical properties.

The interface of an epitaxially grown alloy and silicon substrate can form in two simple ways. One way is that both layers maintain their own crystal structure, which would cause some atoms at the interface end up with just three bonds instead of four bonds. Figure 2.3 (a) shows this. It generates dislocations, which introduce unexpected and undesirable electrical activities [10]. An alternative way, shown in Figure 2.3 (b), is based on the fact that crystalline lattices have elasticity and therefore to match to the underlying substrate crystal structure the alloy, which usually has larger lattice constant, compresses along the growth direction so that atoms retain all four bonds. The strained energy is stored in the distorted atomic bonds and as the thickness of strained layer increases this

energy increases as well until at a certain point the interface cannot handle the energy and switches to an unstrained structure with dislocations [9]. Therefore there is a maximum thickness for the strained layer which should not be surpassed.

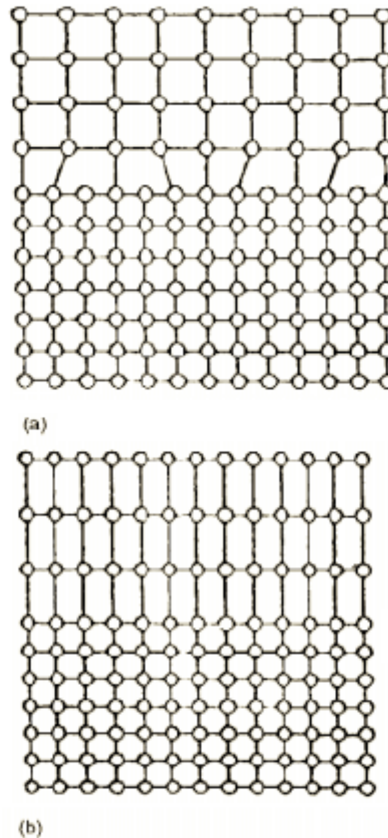


Figure 2.3 Schematic diagram of **(a)** relaxed and **(b)** compressively strained epitaxial layer on silicon substrate [9]

Strained layer superlattices (SLS) are high quality superlattices grown from sufficiently thin layers with lattice mismatches up to 7% [11]. These thin layers are in tension or compression with each other in order to have average lattice constants equal to that of individual strained layers. Figure 2.4 shows the schematic of a typical SLS.

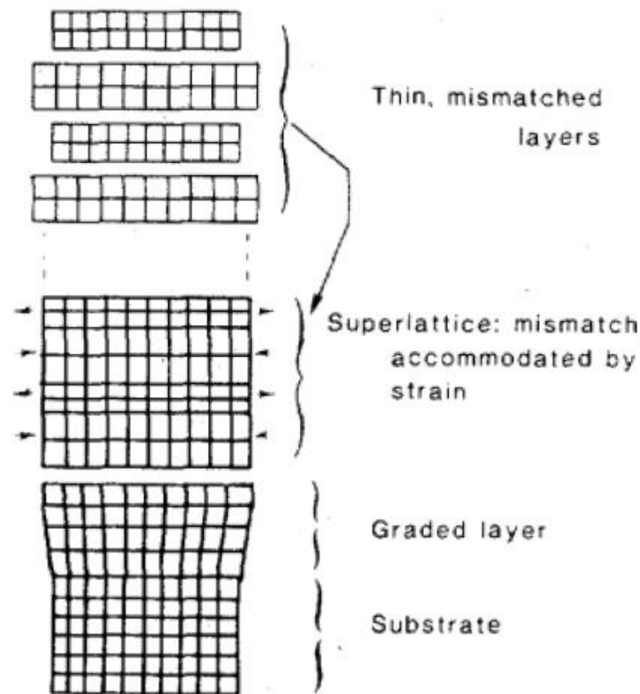


Figure 2.4. The schematic of strained layer superlattices (SLS) [11]

Nozawa. K *et al.* have shown that insertion of $In_xGa_{1-x}As$/GaAs strained layer superlattices between GaAs and Si reduces the threading dislocation density [12]. They have used Migration-Enhanced Epitaxy (MEE) to perform the growth of SLSs, which avoids formation of dislocations caused by thermal annealing.

2.4.2. Growth on compositionally graded SiGe buffers

In other studies, growth of GaAs on compositionally graded SiGe buffers has been investigated and growth of GaAs on Si substrates occurs via relaxed graded Ge/Ge_xSi_{1-x} buffer layers [13]. Ge has a lattice constant very close to GaAs (0.07% mismatch at room temperature) and the Ge concentration of Ge_xSi_{1-x} varies gradually from 0 to 1. A 100% Ge cap layer on top of the graded buffer layer acts as a virtual substrate for GaAs to grow [13].

Although there are many successful reports on this method, some challenges still need to be addressed for growth of III-V compound semiconductors on

compositionally graded SiGe buffers. Most importantly, the thermal expansion of Ge and GaAs is different from Si and this mismatch can cause large strains, dislocations roughening (if compression), cracks (if tension) during cooling down from the deposition temperature [13].

2.4.3. Cycle thermal annealing

In this method, which has been introduced by Yamaguchi M. *et al.* [14], the Si substrate is cleaned very carefully before being loaded into a metal-organic chemical vapour deposition (MOCVD) reactor and then heated up to 1000℃ in the presence of H_2 to remove the native oxide from the surface [14]. Then a buffer layer of around 100Å GaAs is grown at temperature of around 400℃ [15] on the substrate and a second layer of GaAs with typically 2μm thickness is grown at a growth temperature of 700℃. The thermal cycle growth is carried out as following: the growth of the second GaAs layer is interrupted and the substrate temperature is reduced to room temperature, then the sample is again heated up to 700-900℃ under the flow of As flux and the sample is annealed for 10 to 15 minutes at this growth temperature, then the temperature of the substrate is reduced back to 700℃ and the growth process is continued [14]. This process is repeated 1-13 times in one growth run.

The numerical analysis shows a reduction of dislocation density with increasing number of cycles, which leads to the thicker buffer layers. It means a large amount of material is not going to be used in the active layer of the device but just as substrate, which is not desirable.

2.4.4. Epitaxial lateral overgrowth

The idea of epitaxial lateral overgrowth (ELOG) was proposed in a paper by Nishinaga *et al.* in 1988 [16]. In this study, the authors suggested to grow a silicon dioxide (SiO_2) mask on the buffer layer of III-V compound material

before growing the second layer. The mask suppresses the generation of dislocations in the layer under it and allows other dislocations to propagate laterally [17]. Over the years various ELOG techniques were developed. Figure 2.5 shows a schematic diagram of different ELOG techniques.

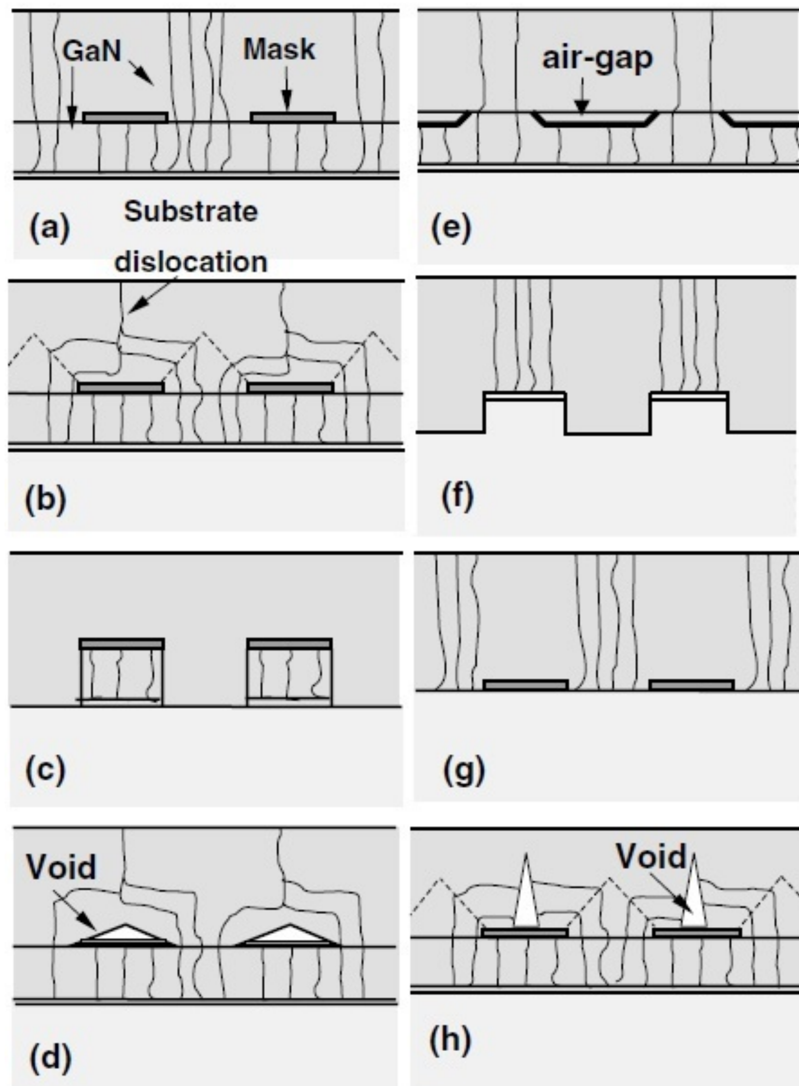


Figure 2.5. (a) The basic ELOG, **(b)** facet-initiated epitaxial lateral over-growth (FIELO), **(c)** PENDEO epitaxy, **(d)** utilization of other masks such as tungsten, **(e)** air bridge ELOG, **(f)** production of grooved stripe structure, **(g)** direct lateral epitaxy and **(h)** facet-controlled ELOG (FACELO) [17]

2.4.5 Selective area epitaxy

Selective area epitaxy can be categorised as one of ELOG methods. Selective area epitaxy of GaAs on Si substrate has been studied over the last 20 years as an alternative method to grow III-V compound materials on silicon with reduced dislocation density. Still, high temperature processes and relatively thick epi-layers constitute problems for this method of growth. Aspect ratio trapping (ART) for selective area growth of Ge on Si has shown some promises and results in defect free Ge areas grown on Si up to 400 nm wide [18]. For growth of III-V materials on Si, MOCVD via ART method of selective area epitaxy has been tried and the growth has been investigated via transmission electron microscopy (TEM) [4]. Figure 2.6 shows the simple schematic of selective-area growth of GaAs on top of Si. It can be seen that in selective-area growth, the initial layers of GaAs have strain because of the mismatch between the lattice parameters of GaAs and Si but when the growth continues the unit cells gradually relax and return back to their bulk size. Figure 2.7 shows the cross-sectional TEM sample studied by J. Z. Li *et al.* [4].

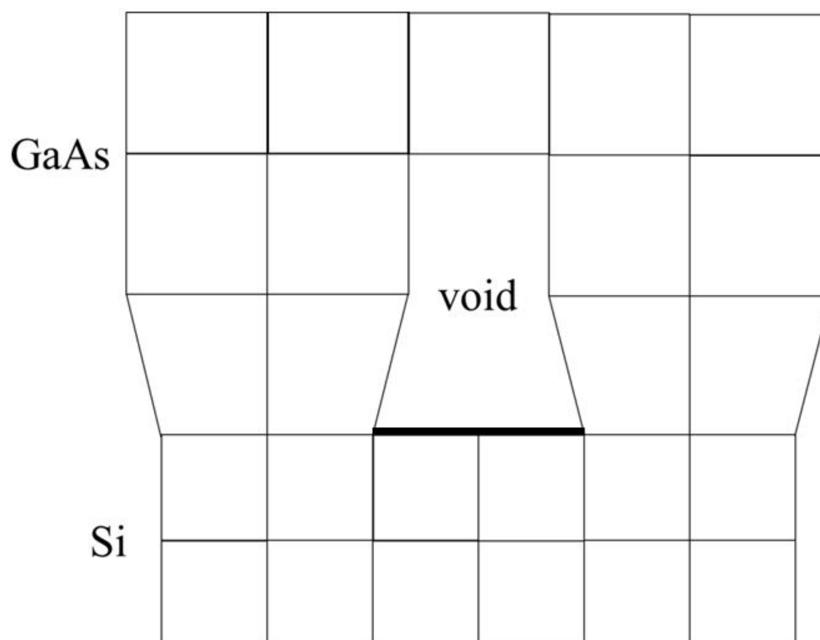


Figure 2.6. Simple schematic diagram of selective-area growth of GaAs on Si

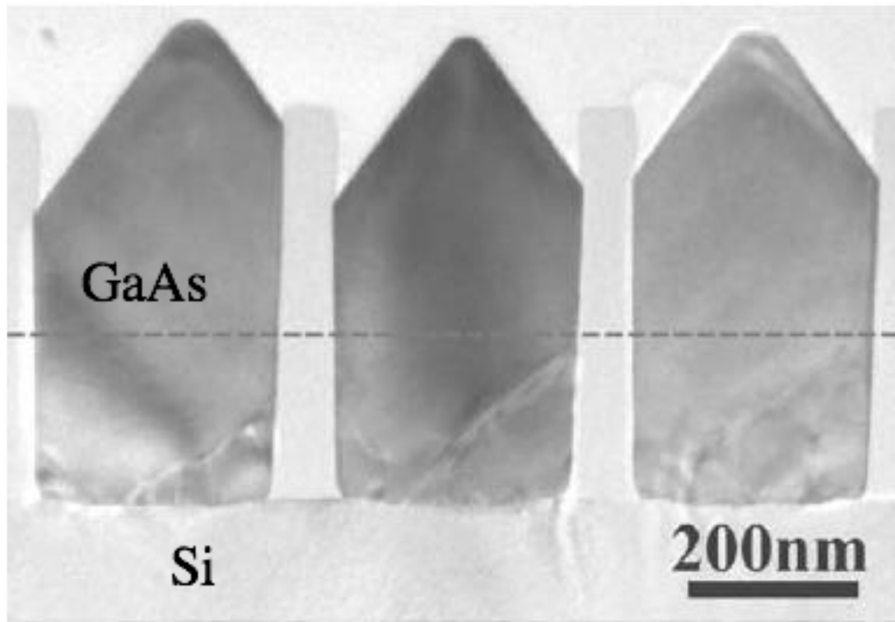


Figure 2.7. The cross-sectional TEM images taken at [110] zone axis. The dislocations are trapped between the SiO_2 sidewalls [4].

2.4.6. Growth via perovskite layers

Other intermediate layers that can be used for overgrowing III-V materials on Si are perovskite materials. Although typically 4Å lattice constant of perovskite oxides is far from both Si and GaAs lattice parameters, with a rotation of 45° the perovskite unit cell can almost match the unit cell of both Si and GaAs with very low mismatch [19,20].

Here, the structure of cubic perovskite materials is discussed and previous studies of interface of these materials on Si (001) and GaAs (001) are reviewed.

2.5. What is the perovskite structure?

Figure 2.8 shows the high-temperature (cubic) structure of a perovskite with chemical formula of ABX_3 where A is usually an alkaline earth metal, B represents a transition metal and X denotes oxygen. The A atoms sit on the corners of the unit cell while the B atom sits in the middle and oxygen atoms are

located at the centre of each face of the unit cell and make an octahedron which surrounds the B atom. At high-temperature, the perovskite phase is cubic, but orthogonal and tetragonal phases can easily be formed due to hydrostatic pressure or interfacial misfit stress, particularly at low temperatures [21] by tilting of the oxygen octahedra around the transition metal ions.

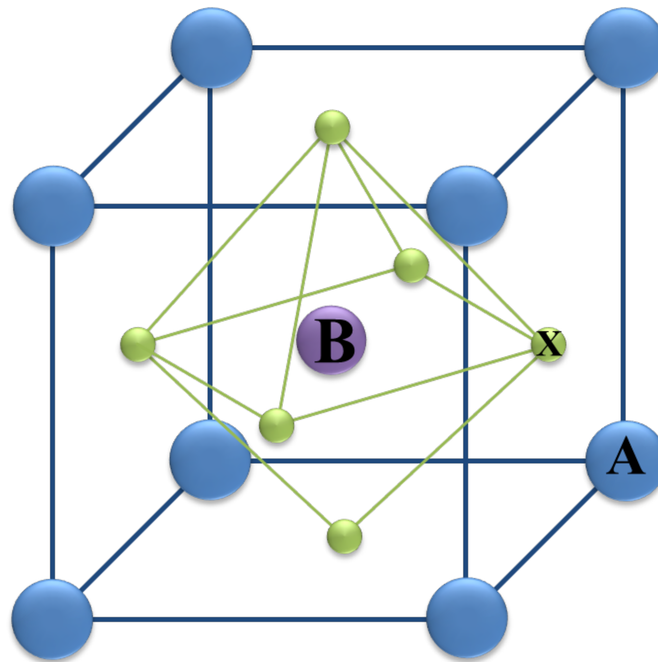


Figure 2.8. High-temperature (cubic) phase of perovskite unit cell structure with chemical formula of ABO_3. (A is an alkaline metal, B is a transition metal and X stands for Oxygen)

Some perovskite materials are ferroelectric compounds, such as $BaTiO_3$. Therefore the material retains a residual electric polarization after the applied voltage has been switched off. Some other perovskite materials are well-known for their dielectric behaviour. Oxygen ion conduction is also an important property for fuel cell and oxygen permeable membrane applications and interesting behaviour in this field can be seen in some perovskite related compounds such as $BaInO_{2.5}$ [22].

Some perovskite materials show superconducting behaviour at low temperature [23]. $La_{2-x}Ba_xCuO_4$ is one of the first so-called superconductors which can be

used as detectors of magnetic signals in superconducting quantum interference devices because of the fact that they are perfectly diamagnetic. This means that the material repels from a magnetic field so that it can easily be used for magnetic signal detectors and most importantly for the use associated with magnetic resonance tomography in medicine [23].

The cubic lattice parameters of perovskite structured materials are normally around 4Å as mentioned before, which is close to $1/\sqrt{2}$ times the lattice constant of GaAs (~ 5.65Å). In this work perovskite materials used as buffer layers for epitaxial growth of III-V compound semiconductors on Si (001). The idea is that because of this relationship between the lattice parameters in GaAs and perovskite, GaAs can be grown on a thin layer of perovskite with a rotation of 45°, which would introduce fewer dislocations and mechanical strains compared to direct growth of GaAs on Si. Perovskite materials which have been chosen for this project are $SrTiO_3$ and $BaTiO_3$, which have cubic and tetragonal structure at room temperature, respectively.

Table 2.1. Unit cell structural properties of $SrTiO_3$ and $BaTiO_3$ at room temperature.

	a	**b**	**c**	Unit cell structure
$SrTiO_3$	3.905Å	3.905Å	3.905Å	Cubic
$BaTiO_3$	3.992Å	3.992Å	4.036Å	Tetragonal

As shown in table 2.1, $SrTiO_3$ has cubic structure in room temperature with a lattice parameter of 3.905Å. On the other hand, $BaTiO_3$ has tetragonal structure, but above 393K (120°C) its structure becomes cubic with lattice parameter of 3.992Å. The phase transition temperature can be increased due to the stressed caused by the mismatch of lattice constant of $BaTiO_3$ and the substrate [24].

2.6. Growth of Perovskite on silicon

There have been many studies of growth of perovskite materials on silicon to combine the advantages and interesting properties of these oxides with silicon technology [25]. The growth of perovskite on silicon is complicated due to the mismatch between the lattice constants of Si and the perovskite layer as well as the oxidation of the Si surface. Therefore buffer layers are needed for this process as well.

Khodan A.N *et al.* [26] have studies the growth of $SrTiO_3$ on silicon by PLD technique. Different fluxes of oxygen have been used in the growth process and the effect of low oxygen pressure on it has been investigated. It has been shown that the temperature of deposition process and the oxygen pressure affect the lattice distortion of the films.

Bhuiyan M.N.K. *et al.* in [27] investigated the growth of $SrTiO_3$ layers with four different thicknesses (3nm, 10nm, 30nm and 100nm) on Si (001) substrate in an MBE chamber. SrO with thickness of 100Å has been used as the buffer layer between silicon substrate and $SrTiO_3$. Also it has been shown that the surface roughness is strongly affected by the thickness of the perovskite layer.

Recent study by Zhang L. *et al.* [28] reports a successful heteroepitaxial growth of $SrTiO_3$ thin film on silicon by hybrid molecular beam epitaxy (hMBE). The study shows that to achieve a perovskite layer with smooth surface, the flux control should be precise throughout the whole growth process.

Figure 2.10 shows the thermal expansion curve for epitaxial and bulk $SrTiO_3$ (100). The linear thermal expansion coefficient for $SrTiO_3$ can be determined from the slope of the bulk crystal, which is equal to 5.35×10^{-5} K^{-1}.

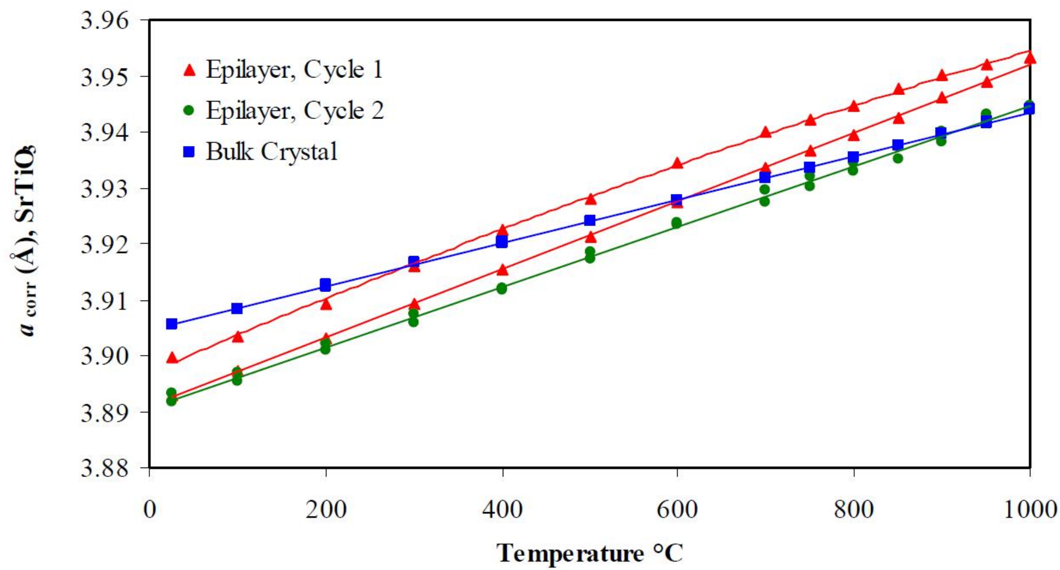


Figure 2.9. Thermal expansion curve for epitaxial and bulk $SrTiO_3$ (100) [29]

Figure 2.10 shows the thermal expansion curves for $SrTiO_3$, Si and GaAs and table 2.2 shows the numerical values of the coefficient of thermal expansions for three materials. (I have multiplied the numerical values for $SrTiO_3$ by a factor of $\sqrt{2}$, to have closer look at the slope of the curves.)

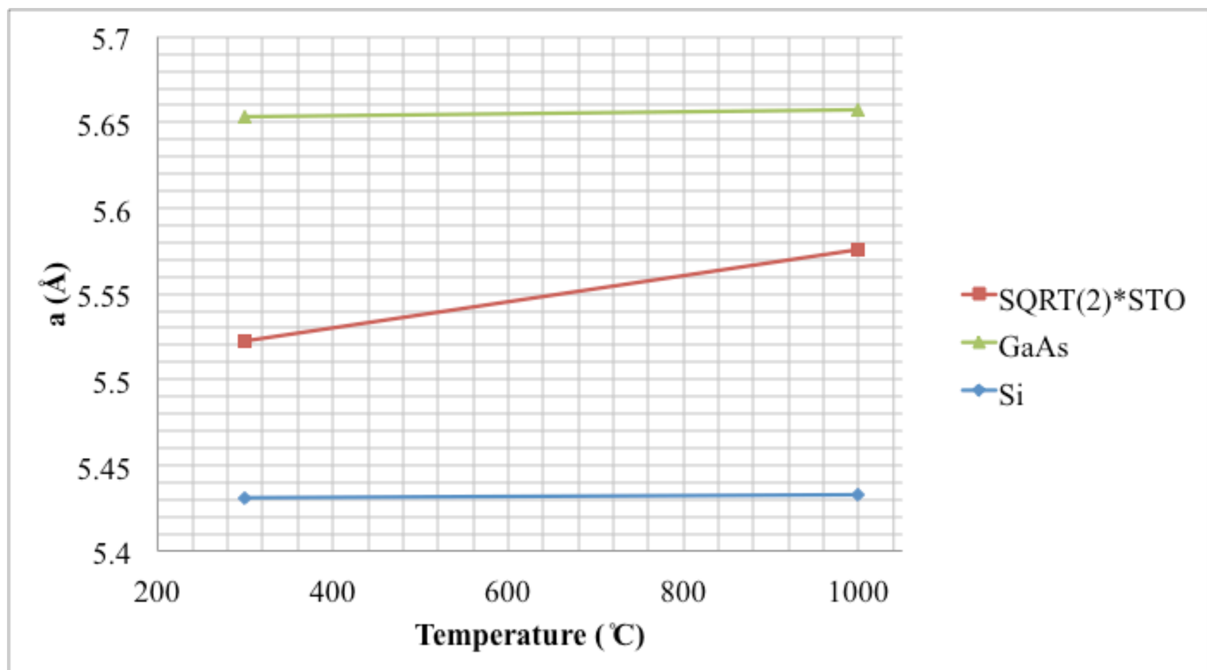


Figure 2.10. Thermal expansion curve for **(a)** bulk $SrTiO_3$, **(b)** Si and **(c)** GaAs.

Table 2.2. The coefficients of thermal expansion (CTE) of $SrTiO_3$, Si and GaAs

	CTE (K^{-1})
$SrTiO_3$	5.35×10^{-5}
Si	2.6×10^{-6}
GaAs	6.8×10^{-6}

The thermal expansion coefficient for Si is 2.6×10^{-6} K^{-1} [30]. This simply shows that with increasing the temperature the lattice parameter of $SrTiO_3$ enlarges more rapidly than the lattice parameter of Si. The unit cell parameter of Si in room temperature is slightly smaller than $\sqrt{2}\times a_{SrTiO_3}$, therefore $SrTiO_3$ on Si would be tensile. This means applying temperature to the wafer can cause bigger strains and dislocations at the interface. In case of GaAs on $SrTiO_3$, $a_{GaAs} > \sqrt{2} \times a_{SrTiO_3}$ and the unit cell parameter of perovskite enlarges faster than unit cell parameter of GaAs with increasing the temperature. This means there is an optimum temperature, in which, $a_{GaAs} = \sqrt{2} \times a_{SrTiO_3}$ and there would be minimum strains on the interface of two materials.

2.7. Perovskite materials and GaAs interface

Growth of perovskite-structured materials on GaAs has been studied for a long time. At the beginning it was interesting for use as gate dielectric in MOSFETs on GaAs substrates [19]. Crystalline oxides on GaAs can potentially have low defect density at the interface and good electronic properties due to the structural registration between GaAs and the oxide layer [31].

To be able use a material as gate dielectric, the insulator has to be electrically and thermodynamically stable on GaAs or other III-V compound

semiconductors [32], therefore many attempts of growth of oxide films on GaAs has been reported with the aim of developing useful gate dielectrics for MOSFET devices using high-k oxides instead of SiO_2 [19,32].

$SrTiO_3$ is one of the perovskite materials which are widely used as substrate for functional oxide growth as well. GaAs combined with $SrTiO_3$ can provide magno-optical and electro-optical properties. Therefore in many studies it has been tried to grow this perovskite material on GaAs. There are two possible terminations of GaAs (001) surface (Ga or As atoms on top surface) and $SrTiO_3$ can initially grow either with Sr-O (SrO) layer or with O-Ti-O (TiO_2) layer. Therefore, there are four possible interface configurations for these two materials.

Liang *et al.* [19] studied the growth of $SrTiO_3$ on GaAs using MBE and their interface. To achieve an epitaxial relationship between $SrTiO_3$ and GaAs, a sub-monolayer of Ti was deposited on GaAs (001), followed by deposition of Sr and Ti at a low pressure and temperature. The XRD results showed that there was a 45° rotation between $SrTiO_3$ and GaAs so that the lattice parameters of both fit together with very low density of dislocations, as indicated schematically in figure 2.11. The results have shown that the GaAs was terminated with As, and the Ti layer reacted with As and formed a Ti-As layer at the interface.

Same studies of the interface of the perovskite oxide and GaAs have been repeated by Contreras-Guerrero R *et al.* [31].

Figure 2.11 shows the ideal epitaxial relationship between $SrTiO_3$ and GaAs unit cells.

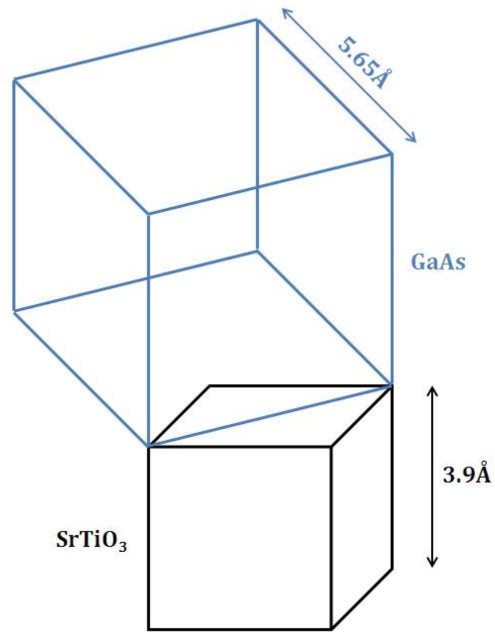


Figure 2.11. The targeted epitaxial relationship between GaAs and $SrTiO_3$.

$[001]_{GaAs} \parallel [001]_{SrTiO3}$

$(100)_{GaAs} \parallel (110)_{SrTiO3}$

Chapter 3:

Experimental techniques

3.1 Introduction

In this chapter the experimental techniques used to grow and investigate the perovskite layers and GaAs over-growth are introduced.

There are many techniques to deposit thin films on a substrate such as CVD, MBE, PLD, spin coating, etc. PLD and MBE are two growth methods which have been used in this study and are introduced and explained briefly in this chapter.

There are many possibilities to investigate and study the growth and characterization of materials. TEM is used to study materials at the atomic level and many quantitative techniques have been developed for use in a TEM to characterize the samples. HRTEM, ADF and BF STEM imaging and EDX spectroscopy are some of these techniques that are briefly described below. AFM and Ellipsometry are two of many techniques that can be used to study the surface of samples and are explained at the end of this chapter.

3.2 Growth methods

PLD and MBE as the growth methods used for the specimens which are investigated in this study are introduced and briefly explained in the following. The thin layers of perovskite grown on silicon via the native oxide were grown in a PLD system and the anneal and GaAs over-growth have been performed in an MBE system.

3.2.1 Pulsed laser deposition (PLD)

Pulsed laser deposition (PLD) is a technique used to grow high quality thin layers of materials. PLD is a simple technique which uses high power laser pulses to evaporate and ionize the surface of stoichiometric targets. Figure 3.1 shows a simple schematic of a PLD system.

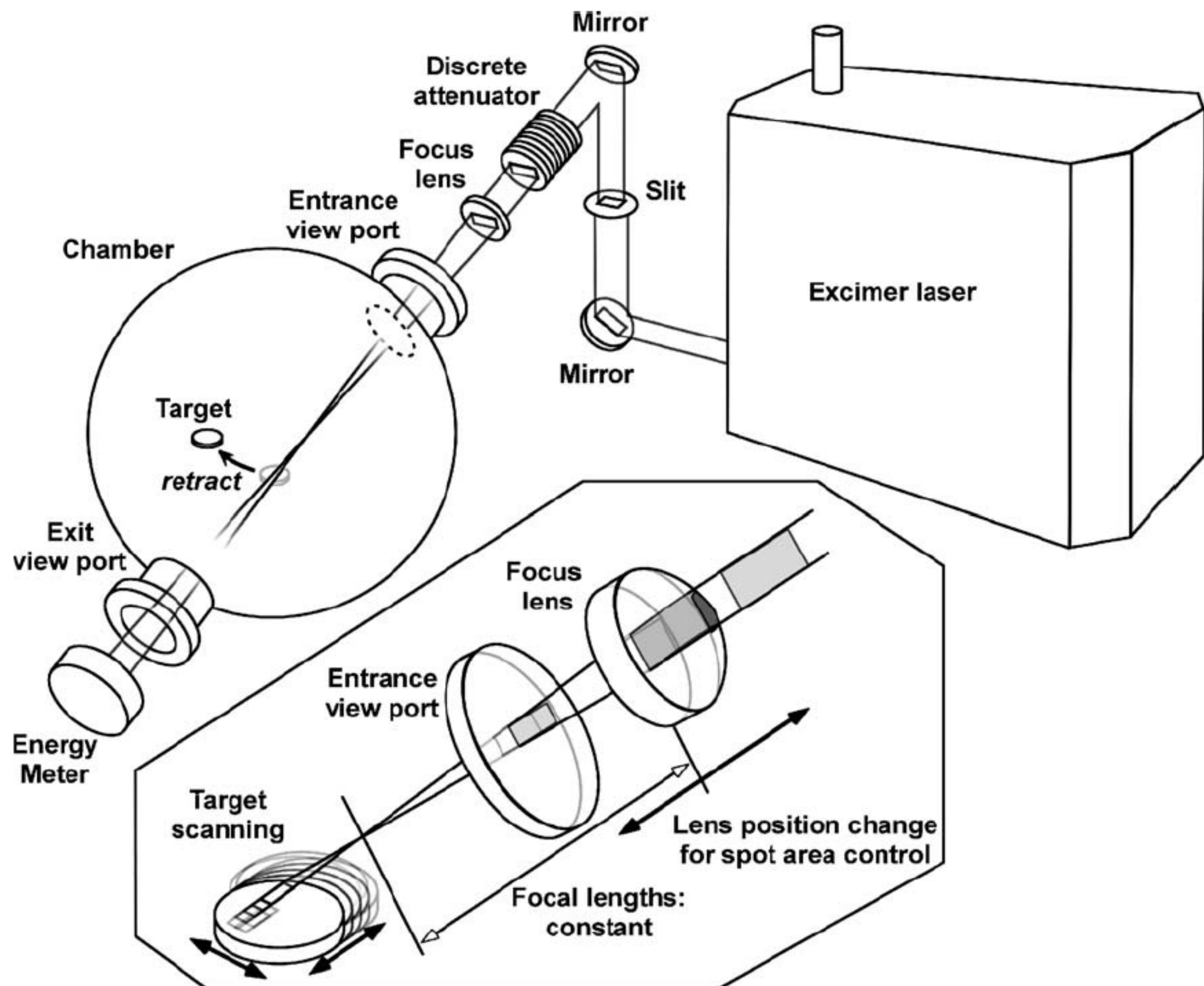


Figure 3.1. PLD schematic with laser and optics [33]

The laser-produced plasmas vaporise from the target surface and some of them recondense on the substrate surface where growth occurs. In practice the growth process, however, is not as simple. Laser flounce, background gas pressure, substrate temperature etc. affect the properties of the film.

The common problem with most of the PLD systems is the fact that the experiments are not easily reproducible. It means the growth of thin films cannot rely on parameters and numbers published in the literature by other groups [33]. Therefore, industrial use of PLD has been very slowly progressed. Below two main reasons for non-reproducibility of PLD experiments are mentioned:

1. The film grown on the substrate is often highly non-uniform. The reason is that the plasma plume is highly forward directed and therefore the thickness of the material collected on the surface of the substrate varies across the substrate.
2. The materials vaporised from the target can contain microscopic particles of molten material with relatively large diameters, which is not good for the properties of the deposited film.

On the other hand, the PLD technique has significant benefits over other growth methods:

1. It is capable of transferring the material from the target to substrate stoichiometrically.
2. The deposition rate is relatively high (typically tens of nanometres per minute).
3. Using a carousel, not only one target material is in the system therefore the technique is able to grow multilayer films without the need to pump the system when the target material changes.

Because of the use of laser in this technique, the process is very clean (assuming having good background pressure and clean substrate surface).

3.2.2 Molecular beam epitaxy (MBE)

Molecular beam epitaxy (MBE) is a growth technique to produce epitaxial structures. In principle, free atoms are produced by heating up a solid source in an ultrahigh vacuum environment. When they reach a hot substrate surface they attach and can diffuse on the surface and produce a growing film on top of the substrate. ,.

Compared to other growth techniques such as Metalorganic Chemical Vapour Deposition (MOCVP), MBE is slower because of its lower growth rate and single wafer capacity. However, it is preferable when there is the need to control the interface and doping profile while growing, due to lower growth rate and temperature. The ultrahigh vacuum also helps to minimise impurity incorporation into a growing layer, compared to non UHV based systems. Ultrahigh vacuum also allows in-situ diagnostics which allows the layer growth to be closely monitored.

The basic components of an MBE instrument are listed and briefly identified as below:

- *Vacuum pump system:* The vacuum system contains the growth chamber at ultra-high vacuum and it is connected to a preparation chamber [34]. The samples are degassed before the growth process in the preparation chamber. There is also a load-lock module in the preparation chamber of the vacuum system to transfer to and from air. As the bake-out temperature goes up to 200℃ for quite a long time, the growth chamber and all its components must be able to resist this temperature. The role of the pumping system is to reduce the impurities in the system to a minimum. The bare pressure level in MBE chamber is 2×10^{-9} mBar, which is produced by four different pumps: A turbomolecular pump, an ion pump, a titanium sublimation pump (TSP) and a liquid nitrogen (LN_2) cooling shroud. Figure 3.2 shows the location of the pumps and other parts of the MBE machine.

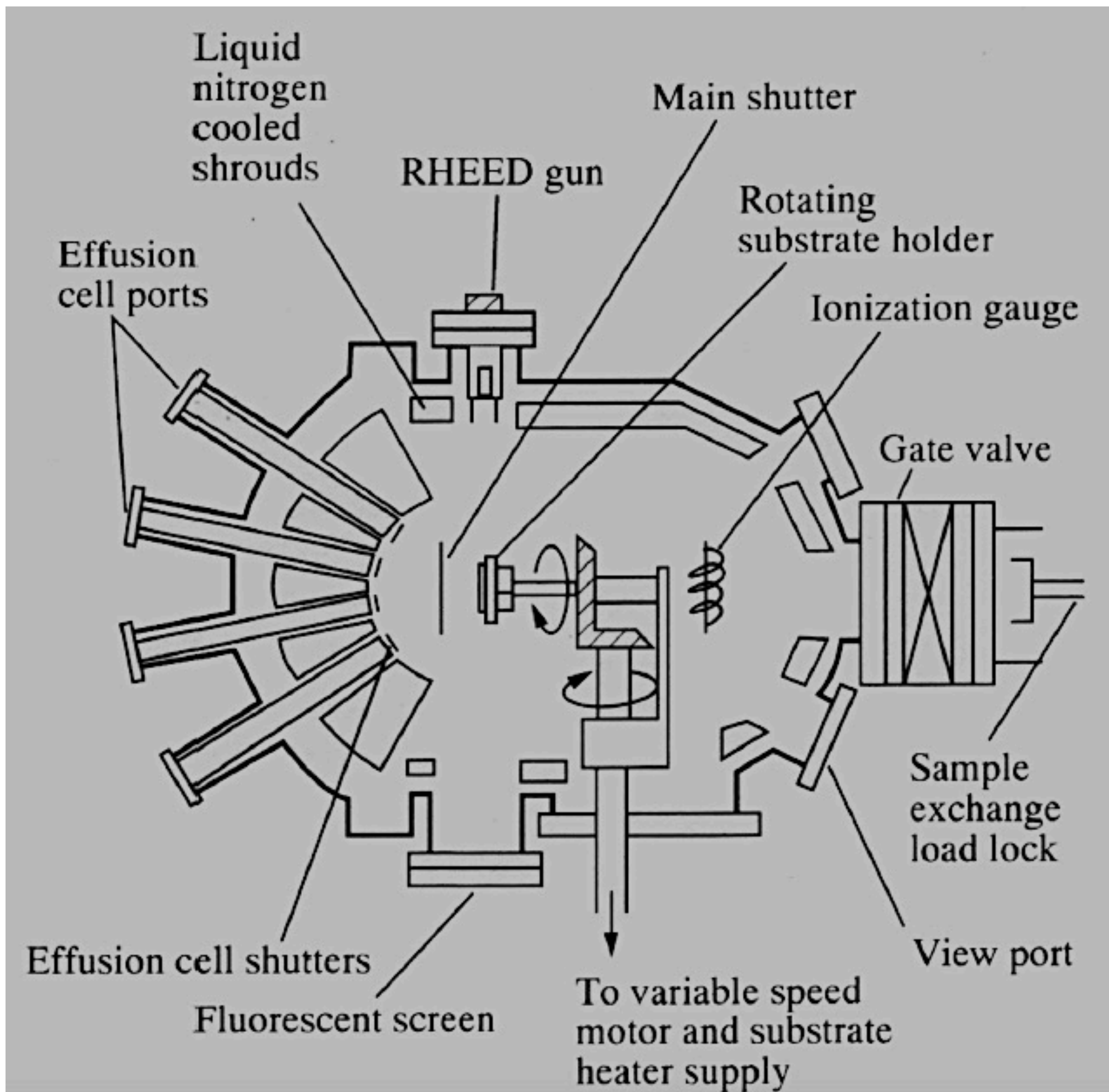


Figure 3.2. A schematic diagram of the vacuum system and other parts of the MBE chamber. [35]

- *Liquid Nitrogen cryopanels:* They prevent evaporating from parts of the systems other than the hot effusion cells. Isolating different cells from each other is also achieved by the cryopanels. They surround the main chamber walls and source from inside.
- *Effusion cells:* They are the most important components of the MBE system. They produce the flux sources by evaporating the condensed materials. The flux should be as uniform and stable as possible.

Furthermore, the effusion cells should be able to resist temperatures up to 1400℃ for a long period of time. An effusion cell usually contains a crucible, heating filaments and cooling system, heat shield and a shutter.

- *Substrate manipulator:* The most important role of the substrate holder is to keep the temperature across the substrate uniform to produce uniform epitaxial layers on the substrate. Rotation is another possibility of the substrate manipulator. It allows the users to rotate the sample to the RHEED patterns in different orientations.
- *Analysis tools:* There are several analytical tools in the MBE systems. The most important one is reflection high-energy electron diffraction (RHEED) which is described later in this chapter. Some other analysis tools that can be optionally installed in an MBE system are a residual gas analyser (RGA), ellipsometry, reflectance-difference spectroscopy and laser interferometry.

Reflection High-Energy Electron Diffraction (RHEED)

RHEED is an in-situ technique for characterising the surface of crystalline materials. A RHEED system basically consists of an electron gun, a clean sample surface and a photoluminescent detector screen. The electron beam hits the sample at very small angle and therefore incident electrons diffract from the sample surface. The electrons interface constructively at a specific angle, depending on the crystal structure and atom spacing on the surface of the sample and the wavelength of the incident electrons and create a diffraction pattern on the detector screen.

Figure 3.3 shows a simple scheme of a basic RHEED system. RHEED experiments must be performed in vacuum due to the effect of gas molecules on electrons that would cause them to scatter randomly.

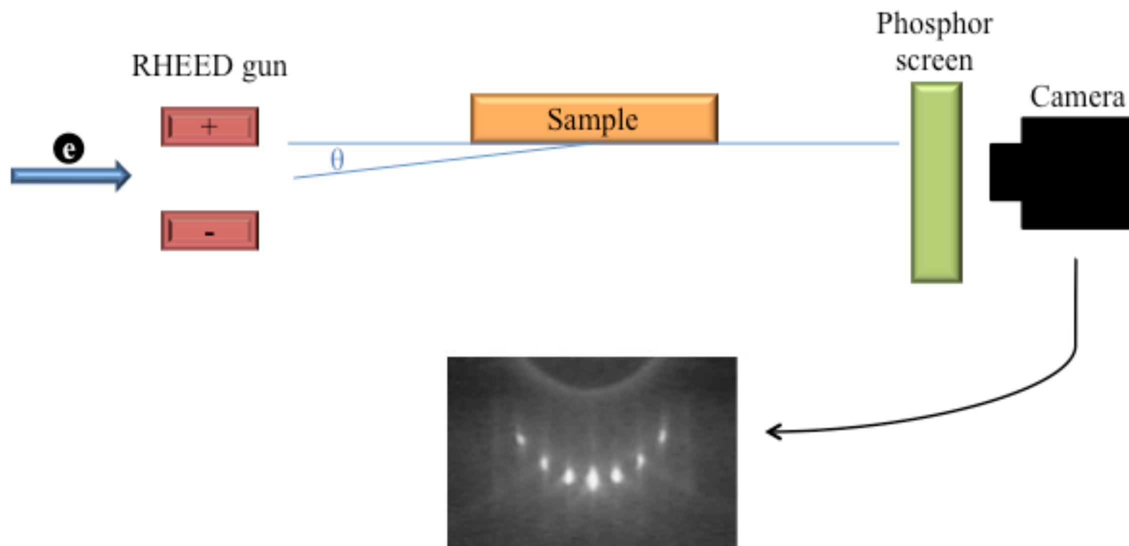


Figure 3.3. A basic RHEED system and an example of a RHEED pattern of Si(001) [36]

The pattern created on the screen contains information on the atomic structure of the surface of the sample. Measurements of patterns from known surfaces have shown that the distances between the bright spots have an inverse relationship with the lattice parameter of the surface reconstructed unit cell [37] (figure 3.4).

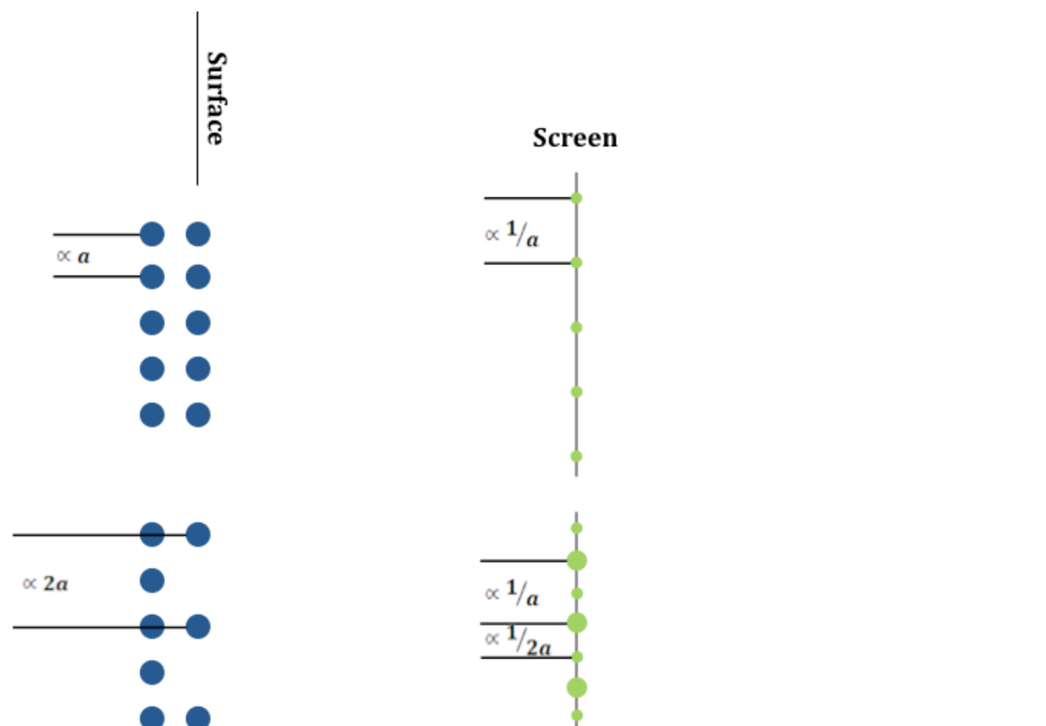


Figure 3.4. Inverse relation between the lattice constant and the distance between bright spots in the RHEED pattern.

3.3 Transmission electron microscopy (TEM)

Figure 3.5 shows a photograph of the set-up of a JOEL JEM-2010F instrument equipped with a GATAN Imaging Filter (GIF 2000), Oxford Instruments Si:Li X-ray detector and a scan unit.

The structure of a TEM instrument is discussed below as well as different TEM techniques used in this study. As a good quality and thin sample is essential to get reliable results, conventional cross-section sample preparation is briefly explained as well.

Figure 3.5. JEOL JEM-2010F field-emission gun transmission electron microscope

Transmission electron microscopy is a useful technique to investigate materials down to the atomic level using high-energy electrons (typically up to 1200 kV). According to the Rayleigh criterion, the point resolution of a light microscope (LM) can be deduced from:

$$R = \frac{0.61\lambda}{\eta \, \sin\beta}$$

where

R is the radius of the resolution function;

λ is the wavelength of the radiation;

η is the refractive index of the medium between the lens and the specimen;

β is the semi-angle of collection of the magnifying lens which depends on the focal length of the lens and the diameter of it.

Knowing the wavelength of electrons (λ=1.51×10^{-3} nm at 200kV acceleration voltage and comparing it to that of visible light ($\lambda \geq$400nm), the image resolution of an electron microscope could improve the resolution compared to a normal LM by a factor of 10^5. But the actual resolution of the electron microscopes is still far away from diffraction limit because of the aberration and imperfections of the electron lenses.

Other limitations of the TEM are:

- The field of view decreases as the resolution increases if the detector size is kept constant.
- The images are 2D projections of the 3D specimen structure, therefore it is difficult to explain and interpret the images.
- Due to high-energy electron interaction with atoms, the specimen can easily be damaged.

3.3.1 Structure of the TEM instrument

Crystallographic structure and chemical properties of a semiconductor specimen can be studied using TEM.

A TEM mainly contains of seven different parts:

- Electron source and gun
- Condenser lenses
- Specimen holder with sample
- Objective lenses
- Intermediate lens
- Projector lenses
- Detectors

These seven parts can be divided into four systems: illumination system (electron sources and guns and condenser lenses), specimen stage, imaging system (objective, intermediate and projector lenses) and image recording system (detectors).

Illumination system

In the illumination system, the electron gun produces the electron beam and the condenser lenses focus the beam on the specimen.

The quality of the electron beam depends on the source of the electrons, which is used in the equipment. There are four types of electron sources used in TEM: thermionic tungsten (W), thermionic lanthanum hexaboride (LaB_6), Schottky field-emission gun (S-FEG) and cold field-emission gun (c-FEG). The thermionic W sources are the worst performing source but for routine and general TEM uses they are cheap and stable and easy to exchange. Thermionic LaB_6 sources give brighter electron beams compared to W. They are more useful for high resolution imaging. On the other hand, they are more expensive and need much better vacuum than tungsten ones. Field-emission guns, first

developed in 1979 [38], offer much higher brightness compared to thermionic sources. They give improved coherence and energy spread as well. But they need to be in ultra-high vacuum (UHV) conditions. The Schottky FEG has larger source size compared to the c-FEG therefore it has higher beam current and better emission stability. As the c-FEG has smaller source size, it's better for use in STEM applications.

The TEM studies in this project are performed using a JEOL JEM-2010F with S-FEG.

The condenser system controls and focuses the beam to the specimen. It can operate in two modes and generate two types of beam: parallel or convergent. The later one is used in STEM. The condenser system in the 2010F consists of three condenser lenses (C1, C2 and a condenser mini-lens) and a condenser aperture. The condenser lenses control the illumination and convergence angle. There are 5 different condenser aperture sizes in the 2010F: 10, 20, 50, 70, 150μm in diameter.

Specimen stage

An ultra-thin 3mm diameter sample is held using a specimen holder in the TEM. The holder is able to move the sample in *x*, *y* and *z* directions. There are sample holders with the ability of tilting the sample as well to set the correct orientation. The holder also should allow the sample to move not more than 0.1nm when the micrograph is exposed [38].

In the 2010F the sample can be moved by ±1 mm along *x*, *y* and less in *z* directions. The specimen can be tilted by up to ±20° in the double tilt holder as well.

The image forming system

The imaging system contains three different sets of lenses: objective, intermediate and projector lenses. The first set of lenses forms the first

intermediate image and also the diffraction pattern. The projector lens enlarges the intermediate image and displays it on the screen. Depending on the formation of the first intermediate image or the diffraction pattern by the objective lens, imaging and diffraction modes are obtained, respectively. The first projector lens which is also called diffraction lens or intermediate lens switches between the two modes.

Figure 3.6 shows the basic schematic of a transmission electron microscope in both imaging and diffraction mode.

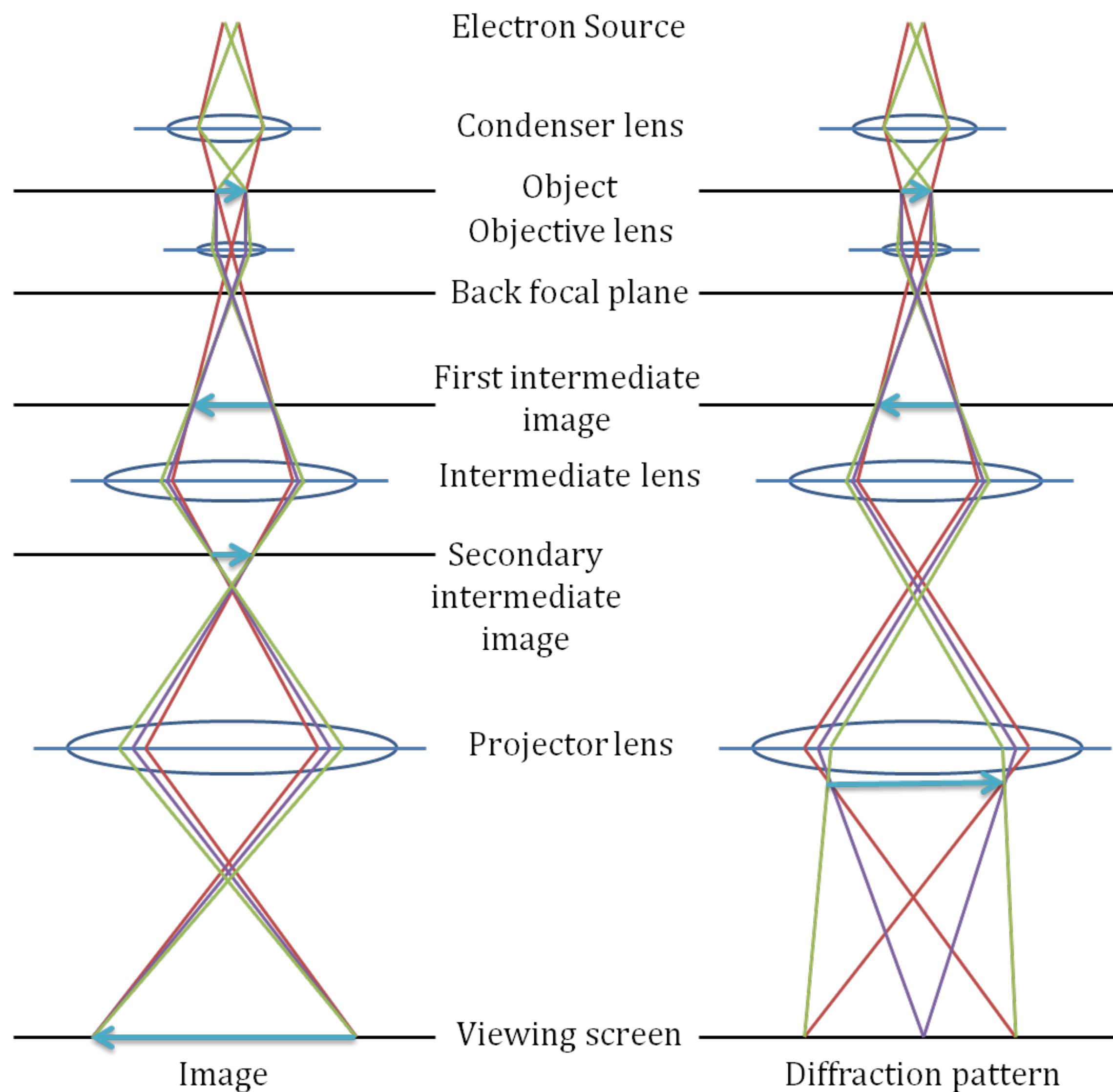


Figure 3.6. Imaging (left) and diffraction (right) modes in TEM

The diffraction pattern is formed near to the back focal plane of the objective lens; therefore, if we take the back focal plane of the objective lens as the objective plane of the intermediate lens we will have the diffraction pattern on the screen. Figure 3.7 shows the formation of the diffraction pattern using the intermediate lens.

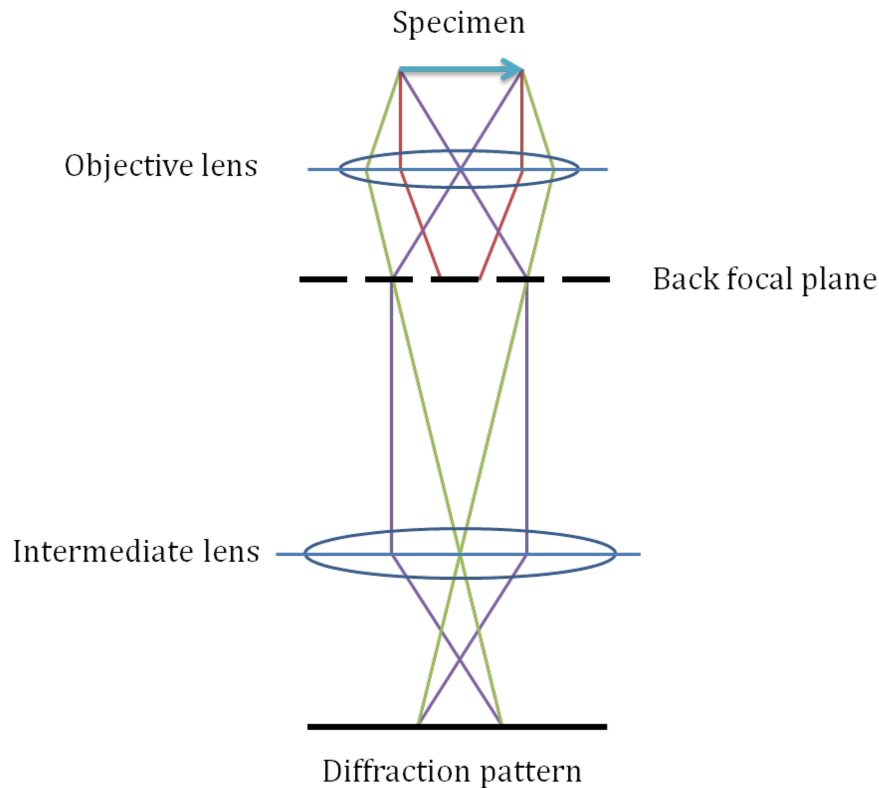


Figure 3.7. Intermediate lens system in TEM

There are two different apertures in the imaging system: The objective aperture is located in the back focal plane and controls the contrast of the image. "The difference in intensity between two adjacent areas" is the best definition of contrast [38]. Contrast can be obtained in the image by selecting specific electrons or eliminating them from the image. In other words, we can have a bright-field (BF) or dark-field (DF) image by selecting the direct or diffracted electrons for imaging respectively. It can easily be obtained using the objective aperture. In BF mode the objective aperture stops all the diffracted electrons and just the direct electrons pass through the aperture and form the image. In DF

mode the objective aperture collects a particular diffracted beam by tilting the incident electron beam so that one diffracted beam only goes through the aperture.
Selected area diffraction (SAD) aperture is used to choose different areas of the specimen to contribute to the diffraction pattern. It is located in the conjugate image plan of the objective lens. This aperture and the objective aperture are not used at the same time. When an interesting area is found on the specimen and centred on the screen, the SAD aperture is inserted to choose this area of interest, and then the mode should be changed to diffraction to record a diffraction pattern. Then the objective aperture can be used to choose a spot for imaging. Choosing the central spot gives bright field image and choosing any other spot gives a dark field image. Finally, the SAD aperture should be removed and the mode be switched back to imaging to record an image on the screen.

Image recording system

When the projector lenses expand the beam on the imaging device, such as negative film or a fluorescent screen or a charge coupled device (CCD) camera (the image recording system), the electron intensity is converted to an image which can be seen by the human eye (after developing the negative films or reading out the CCD camera by a computer). A fluorescent screen converts the electron intensity falling onto it, into visible light. To detect this light, detectors such as CCD cameras or image plates are used.
The 2010F used in this work has a fluorescent screen which is used to align the instrument. It has a TV camera as well, which displays the images or spectra in real time. There are negative plates as well to record especially the diffraction patterns (because recording diffraction patterns can damage the CCD camera very easily). The microscope also has a CCD camera to record images and

spectra. Also, the 2010F is equipped with BF and annular dark-field (ADF) detectors to detect and record STEM images.

3.3.2 TEM techniques

Different transmission electron microscopy techniques (HRTEM, STEM, electron diffraction and analytical TEM using EDXs) are being introduced in this section. Each of these techniques is based on different signals produced by the interaction between the beam of electrons and the specimen. Figure 3.8 shows a basic diagram of all the secondary signals generated by the interaction of the electron beam and the specimen surface.

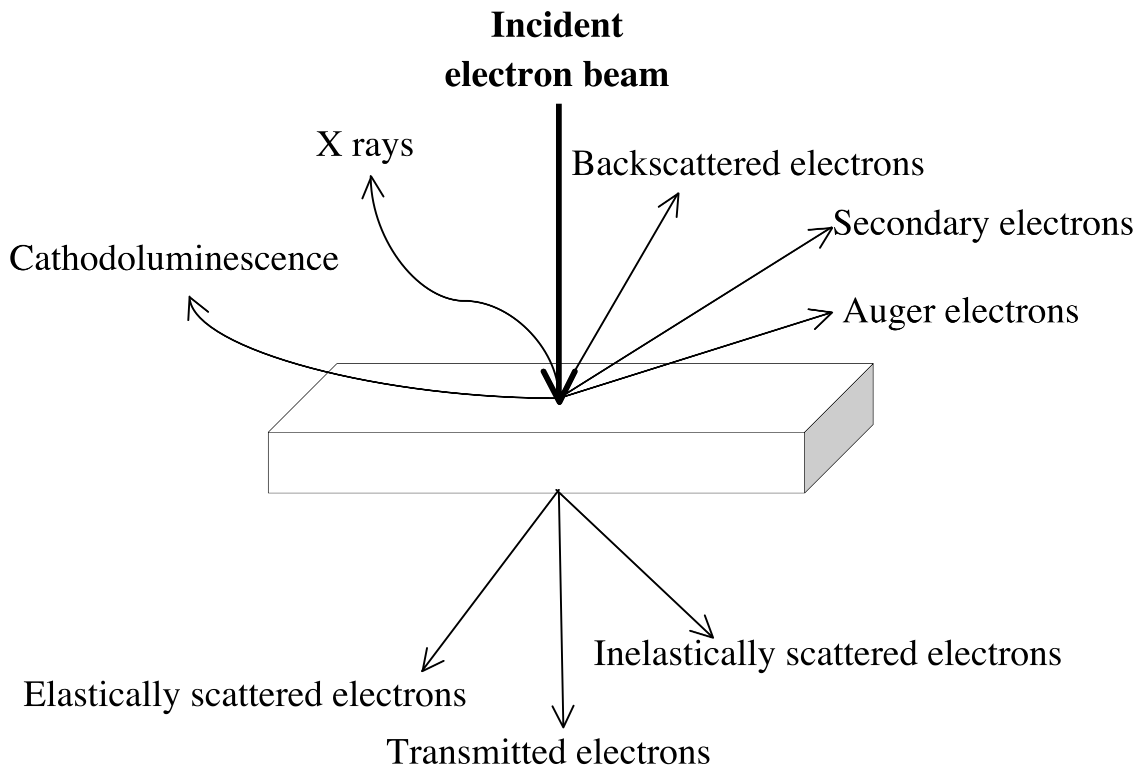


Figure 3.8. Signals generated by the interaction of incident electron beam and the specimen

High-resolution transmission electron microscopy (HRTEM)

In this mode the crystallographic structure of a specimen can be seen on the atomic scale. Therefore it is easy to study nanoscale properties of crystalline materials using this method [38]. But the projected structure image is not interpretable very easily because the image formed by HRTEM relies on phase contrast.

The mechanism of phase contrast is based on the possibility of forming the images by interfering one or more diffracted beams with the direct beam [38]. The phase contrast depends on many factors, such as thickness of the specimen, the focus, the specimen orientation, the wavelength of the electrons and the microscope's beam alignment.

The image resulting from the interference of diffracted beams and the direct beam (HRTEM) is known as lattice imaging because it is capable of imaging the atomic structure of the specimen if the specimen is tilted such that the beam is parallel to a zone axis. The interference of lattice fringes gives a pattern of dark and bright spots, which represent the atomic columns or tunnel sites in between [38]. HRTEM is used to analyse the atomic structure of the layers of the specimen but cannot give any quantitative information on the chemical composition of the material, unless for the image simulations which are quite complicated.

Many factors affect the high resolution images such as the beam alignment, sample thickness, the objective lens's spherical aberration and its defocus. The phase contrast transfer factor (CTF) is a function which describes the limitations of the apertures and aberration in objective lens of the microscope:

$$T(k) = -\sin[\frac{\pi}{2} C_s \lambda^3 k^4 + \pi \Delta f \lambda k^2]$$

Where

C_s is spherical aberration;

λ is the wavelength;

Δf is defocus value;

And k is the spatial frequency;

To have the ideal CTF, the optimum value of Δf which is called Scherzer defocus is:

$$\Delta f_{Sch} = -1.2\sqrt{C_s\lambda}$$

The point resolution of a transmission electron microscope is defined as the reciprocal of the maximum spatial frequency at which the contrast transfer function goes through zero for the first time and can be calculated by the following formula:

$$r_{Sch} = 0.66\lambda^{3/4}C_s^{1/4}$$

To measure lattice spacings, HRTEM imaging can be used as well as the FFT image of it. To calculate the lattice spacings the equation below is used:

$$Rd=\lambda L$$

Where

R is the spacing in real image;

d is the spacing in FFT image;

λ is the wave-length of electrons;

and L is the camera length;

As the concept of λL (which is the camera contrast) is constant for each individual camera, for each two points in power spectrum we have

$$R_1d_1=R_2d_2$$

From this equation, knowing the real spacing of one point in the power spectrum is enough to calculate the real spacing of the other one by simply measuring the spacing in FFT image. Figure 3.9 shows an example of calculating the planar spacing presented by $p_{(hkl)}$.

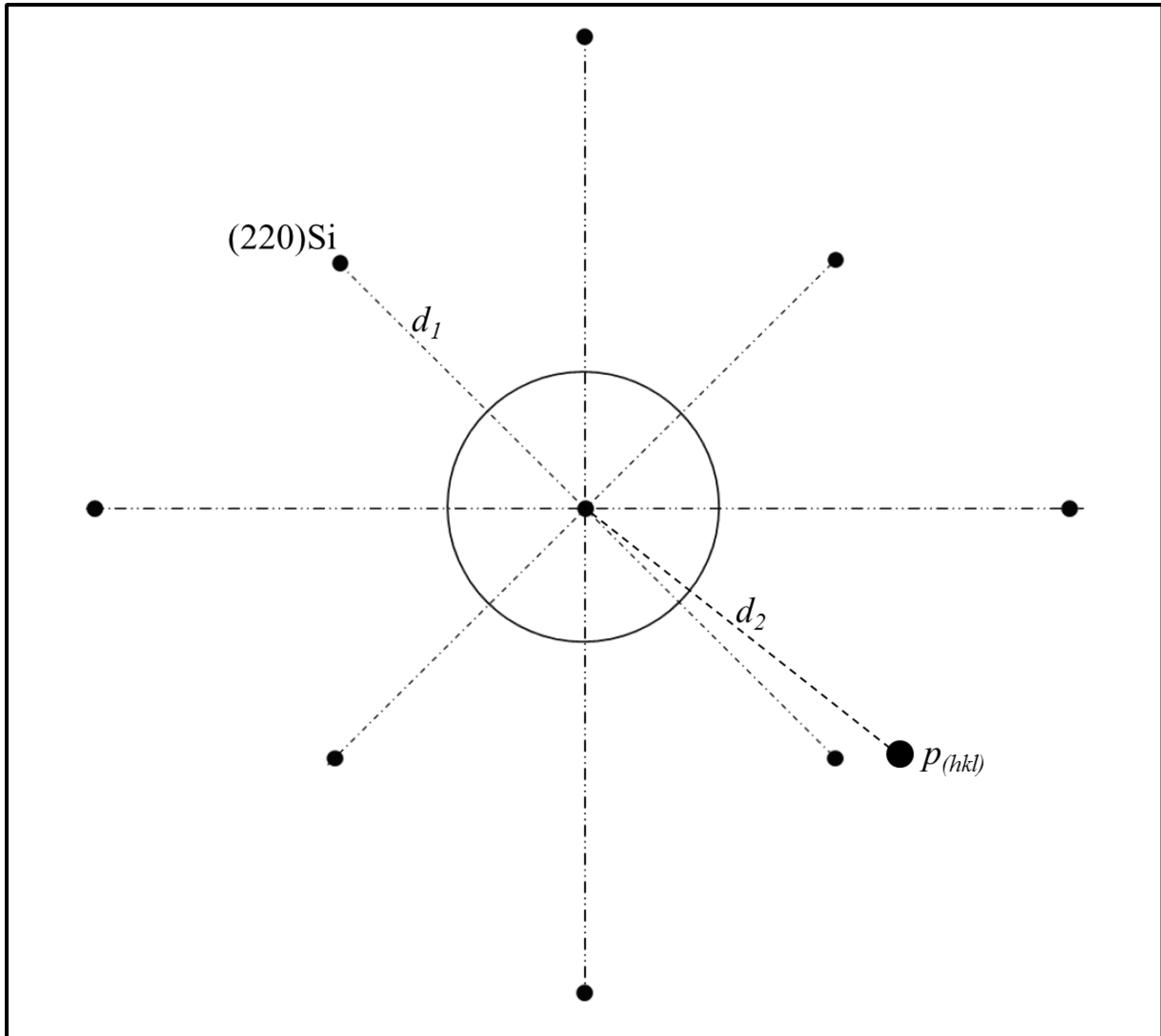


Figure 3.9. An example of calculating the planar spacing from the FFT image, knowing the (220) spacing of Si and measuring the reciprocal spacings (d_1 and d_2) from the power spectrum.

Scanning transmission electron microscopy (STEM)

Scanning transmission electron microscopy (STEM) is a combination of transmission electron microscopy and scanning electron microscopy techniques.

One of most important advantages of STEM over TEM is that in this technique characteristic X-rays and electron energy losses can be obtained from each point the beam is focused on.

In STEM technique the interaction between the beam of electrons and specimen atoms forms the virtual image with different grey levels which represent the different signal levels at any location of the specimen.

In STEM mode the electron beam is focused (like a probe) and scans an area of interest. At each point the signal detected is saved and used to form different types of images using the detectors such as BF, ADF, High angle ADF (HAADF), X-ray and electron energy-loss spectroscopy (EELS) detectors.

Some of the advantages of STEM mode over TEM are:

- Due to the electronic nature of STEM mode, contrast and brightness of the image can be adjusted electronically.
- Rotation of the image can be done electronically.
- Performing EDXs and EELS can be done simultaneously while the annular dark field image is being acquired

To form a bright field image in STEM, a detector in the optic axis is used to collect the direct beam. To form a dark field image a ring detector collects the scattered electrons. It is different from dark-field TEM imaging, in which, using the objective aperture diffracted electrons are chosen to form the image as explained before.

Forming a small probe is very important in STEM imaging due to its effect on the spatial resolution of imaging and also analytical techniques [38]. To optimize the electron beam size (the probe), an electron Ronchigram (also known as “Gabor hologram” or “shadow image”) is used [38]. This method was used by the Italian physicist Vasco Ronchi to determine the aberrations in an optical system. The aberration of the system depends on the alignment of the

beam. In practice Ronchigram alignment is performed following these steps in STEM mode:

- Using the largest condenser (150μm) aperture find the Ronchigram (in an amorphous area of the specimen) by changing the height of the specimen.
- Adjust the stigmatism in condenser lenses so that the Ronchigram is a symmetric circle (See figure 3.10).
- Change the condenser aperture to a smaller size (depending on the use of STEM image, 70μm for EDXs and 40μm for ADF imaging)
- Bring the Ronchigram to the centre with respect to the detector.
- Scan the image

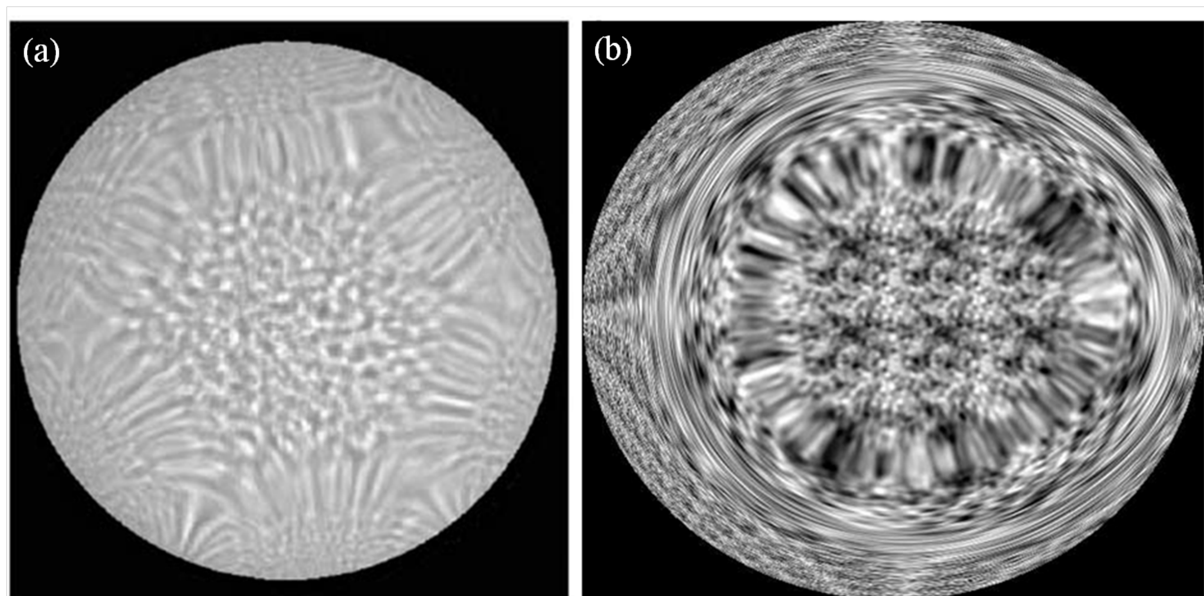


Figure 3.10. Ronchigram from a (a) estigmated condenser and (b) an optimized electron probe [39]

Energy dispersive X-ray (EDX) spectroscopy

To get information about the chemical composition of a specimen, the characteristic X-rays emitted from the specimen after excitation by high energy electrons are used in EDXs.

The energy of the X-ray is equal to the difference between the energy levels of two shells in the atom which are responsible for the process of transition of an electron from a lower binding energy shell to an inner-shell vacancy. The vacant hole has been formed when the incident beam inelastically scattered by an inner shell electron of the atom. Figure 3.11 shows a schematic diagram of the principle of EDXs.

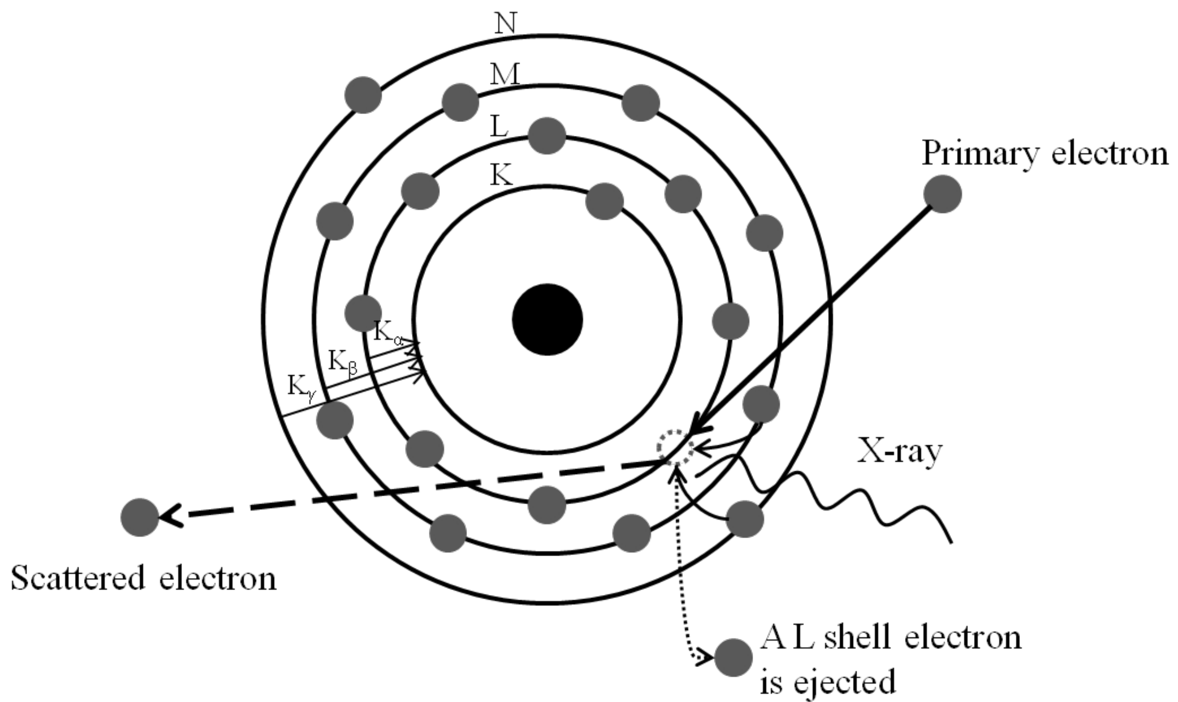


Figure 3.11. Generation of the X-rays and principle of EDXs (modified version of [38])

The X-ray spectrum is a diagram of X-ray counts (intensity) as a function of energy. The peaks of the X-ray spectrum are determined by the ionization energies. Each peak is corresponding to a unique ionisation energy and if the energy resolution is good enough, all the peaks and hence all the elements can be determined.

In the 2010F an Oxford Instruments Si:Li X-ray detector with an ultrathin window is used to obtain the EDXs data. A Link ISIS 300 microanalyser is provided by Oxford Instruments to determine the composition of the elements and provide mapping capability.

Quantitative elemental analysis with a very high sensitivity is the most important application of EDXs technique.

The four basic components of the EDXs are the beam source, the X-ray detector, processing electronics and the screen (for example, micro-channel architecture, MCA, display).

There are some limitations of the EDXs technique. Various factors can affect the accuracy of EDXs. Many elements have overlapping peaks. Elements with low atomic mass (to be specific the three first elements of the periodic table) cannot be detected and elements with Z=4 (Be) and Z=5 (B) are just detected with low sensitivity.

The precision in EDXs is limited by statistical error. For most of the elements the obtained precision is less than ±1% but other factors such as the other errors in corrections applied to the raw data and uncertainties in the compositions cause the accuracy to be commonly near to ±2%. Also the bombarding electrons raise the X-ray spectrum which makes small peaks to be difficult to detach from the rest of the spectrum. In other word “background” is present in the spectrum. To detect enough X-ray counts, longer counting times can be used.

3.3.3 TEM sample preparation

Preparing a TEM sample means to prepare an area of interest, thin enough to be electron transparent, to fit in the sample holder used in the electron microscope. It means the sample should be thinned (to typically 100nm and less) so that the electrons from the gun can go through the material and hit the screen to produce the image.

Conventional cross-section preparation

The procedure of cross-sectional TEM sample preparation is started with sampling the area of interest. The wafer is cut and two pieces ~10mm × 3mm are glued face to face using G1 epoxy resin so that the thin layers of interest meet each other in the middle. Silicon backing blocks are glued to both pieces for support. The surfaces facing each other should be very clean so that the glue line can be as thin as possible. The stack is clamped by a clamping device and baked in the oven (~100℃) for at least an hour. Then the sample is taken out to cool down to room temperature. Using a very small amount of glue and applying moderate pressure in the clamping device, the central glue line is ultra-thin. Then the stack is cut to give two separated thin stacks of materials. At the next step, using a refined wax the stack is mounted on top of a piece of clean glass which is directly attached to a steel block. Grinding and polishing the stack is the next step to obtain a mirror-like surface on both sides. The grinding is done using silicon carbide papers under running water. Polishing is done with first 3µm and then 1µm diamond paste to eliminate any visible scratches from the surfaces. Then ceramic rings of 3mm diameter are glued on top of the sample to define a nice circular shape, using quick-setting epoxy. At the end any extra material outside the ceramic rings is removed from the area and the samples are carefully cleaned with warm n-butyl acetate to remove the sample from the supporting glass and then the sample is cleaned with ethanol before putting it in the ion miller.

Ion milling

Ion milling is in fact bombarding the sample with energetic ions to sputter the material from the specimen and make it electron transparent.

Five different ion milling systems have been used in this work: Leica EMRES 100, Technoorg-Linda IV3, Gatan Duo-Mill Ion Beam Milling Equipment (X2), Fischione 1010 and 1050.

Using an Ar^+ ion miller, a hole will be made near the middle of the sample the edges of which should be very thin and electron transparent in the electron microscope (a few to ~100 nanometres). Before ion milling, the middle part of the specimen can be thinned further mechanically using a dimpler to have a higher chance of making the hole exactly in the middle.

The parameters which have important roles in thinning the sample in an ion milling system are the voltage and current of the anode, the angle between the beam and the specimen, rotation or oscillation of the sample, single or double side milling and the temperature of the sample.

Higher current and voltage in the source make the milling faster but damage the sample as well. High angle (normally more than 20°) damages the sample as well rather than sputtering and thinning it. The standard parameters which have been used to prepare the samples in this work are: voltage between 4 and 5kV, current between 2.5 and 4 mA, beam angle of 9 degrees in Fischione equipment and 15 degrees in Gatan Duo-Mill, and 360° rotation. Figure 3.12 shows a schematic diagram of a double side ion milling system.

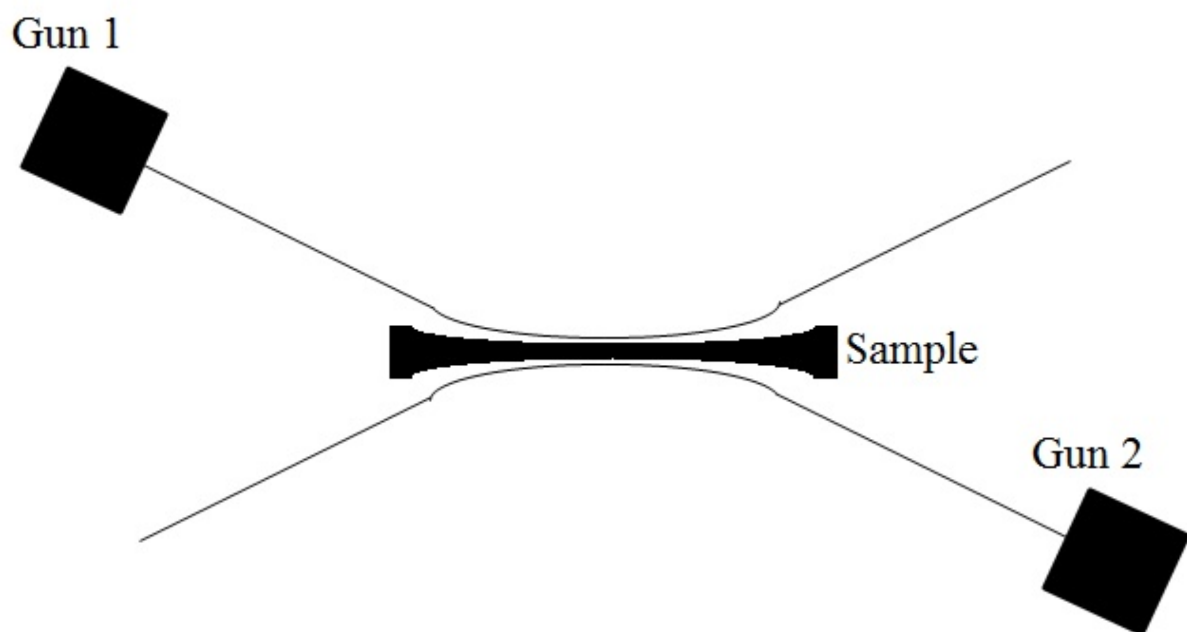


Figure 3.12. The position of the specimen and guns in a double side ion milling system

3.4 Atomic force microscopy (AFM)

AFM is a high-resolution scanning probe microscopy which can demonstrate resolution on the order of less than a nanometre. The principle of AFM is very close to STM, which was developed in 1981. Figure 3.13 shows a simple schematic of operation of a STM and an AFM with a sharp tip of nano-scale dimensions, which moves in three dimensions in the *x*, *y* and *z* directions [40,41].

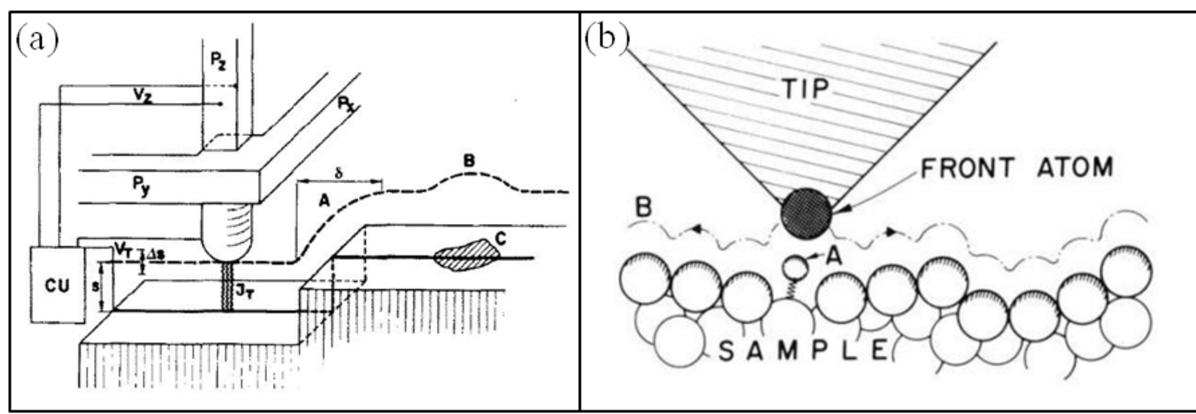


Figure 3.13. Operation of (a) STM [40] and (b) AFM [41]

In STM, the tip material is usually either tungsten (W), a platinum (Pt)- iridium (Ir) alloy or pure Ir [41]. With a constant bias voltage, V_T, applied to the sample and a very small gap between the sample and the tip in the range of a few angstroms, the tunnelling current, I_T, flows between the tip and the sample. Using this current as feedback, the tip travels in the *x* and *y* directions and the *z* position is recorded to keep the tunnelling current, I_T, constant [40]. In AFM the force between the tip and the sample is used as the feedback and the *z* position is recorded to keep in constant [41]. Depending on the operation mode, the *z* component of the force between tip and sample, F_{ts}, or another signal derived from this force is used as the imaging signal in AFM. The force sensor (cantilever) is usually made of Si with an integrated tip.

3.5 Ellipsometry

Ellipsometry is a very sensitive optical technique used to study the dielectric properties such as roughness, thickness, electrical conductivity and doping concentration of thin films [42, 43, 44].

When the incident beam interact with the material its polarization changes [45]. Ellipsometry measures the change in polarization. This change depends on optical properties of the material as well as its thickness. The relationship between these parameters can be figured out using these equations:

$$2\varepsilon_r d = \Delta\varphi \quad \text{and} \quad 2d = {}^{2t}/_{\cos \emptyset}$$

Where

ε_r is the absorption coefficient of the material

2d is the distance the light beam travels inside the layer

Δφ is the polarization change

Φ is the beam emission angel

and *t* is the layer thickness

Figure 3.14 shows a simple schematic diagram of ellipsometry configuration.

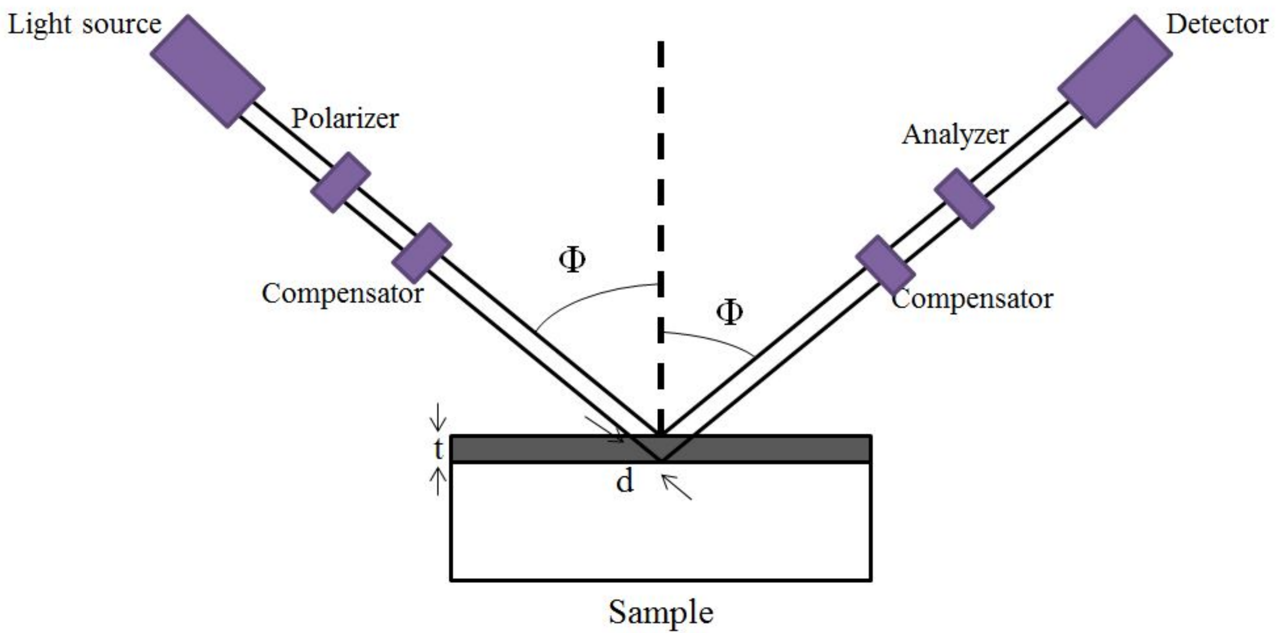


Figure 3.14. Schematic diagram of an ellipsometer.

Ellipsometer has been developed over the years to be sensitive enough to measure thicknesses of a single monolayer to few microns [46].

For thickness measurement in an ellipsometer, a portion of the light should travel the film and come back to the surface of the sample. If the material of the film absorbs the light, thickness measurement can be performed for only thin layers.

Chapter 4:

Investigation and Characterization of as-deposited titanate

4.1 Introduction

Many III-V compound semiconductors such as GaAs, InAs and InSb, have higher electron mobility than Si and also direct band-gaps which makes them more attractive for use in electronic and opto-electronic applications. However, silicon is mainly used in semiconductor devices due to its chemical stability, thermal properties, scalable processing of its oxide and cost. Hence III-V epitaxy on Si has been studied for years [47].

Because of the mismatch in lattice parameters between different semiconductors (other than AlAs/GaAs) there usually is a large density of dislocations at the interface. One solution to avoid this large density of dislocations is to use an intermediate layer between silicon and III-V semiconductor. One choice for the intermediate layer would be perovskite oxides. All cubic perovskites have lattice constants near 4Å which is close to $\sqrt{2}$ times the lattice constant of GaAs (≈ 5.65Å); therefore GaAs could potentially be grown on the perovskite layer almost lattice matched by 45° rotation if it had the orientational relationship as follows

$[001]_{GaAs} \parallel [001]_{SrTiO3}$

$(100)_{GaAs} \parallel (110)_{SrTiO3}$

This could give fewer dislocations compared to direct growth of GaAs on Si [19]. In this work we investigate the growth of thin layers of perovskite on native silicon dioxide before overgrowth by GaAs.

4.2 Experimental work

Four wafers, each consisting of a thin layer of perovskite grown on Si substrates via the native oxide by pulsed laser deposition, have been analysed by AFM, ellipsometry and STEM. Two of the samples have thin layers of $SrTiO_3$ with nominal thicknesses of 2 and 8nm and the other two have layers of $BaTiO_3$ of the same nominal thicknesses.

AFM images have been captured with a Veeco Nanoscope V instrument operated in tapping (non-contact) mode. Nanotec's WSxM 5.3 software [48] was used to analyse the AFM images. A VASE® J.A. Woollam Co., Inc. ellipsometer has been used to measure the thickness of the perovskite layers.

To investigate the surface of the thin perovskite layers and the interfaces between Si and the perovskite layers by electron microscopy, cross-sectional samples were prepared by gluing two pieces of wafers, one with nominally 2nm perovskite layer and one with nominally 8nm perovskite layer, face to face, gluing Si backing blocks to each side to make the stacks 3mm thick, cutting the blocks by diamond saw, grinding and polishing the cross-sectional samples and finally ion milling them in a Fischione 1050 argon ion mill at 4kV and 2mA until electron transparency.

The electron microscope used in this study is a JEOL-2010F field-emission transmission electron microscope operated at 197kV, which has a scan unit and BF and ADF detectors for STEM. The microscope is also equipped with a GATAN imaging filter with a CCD camera for image acquisition.

4.3 Results and discussion of as-grown layer structures

Figure 4.1 is the AFM image of an area of 5×5 μm^2 of a native Si wafer without any layer grown on top. The acquisition time was 0.5s and the image consists of 512×512 pixels, yielding a sampling of 9.8nm/pixels. This image is used as a reference to compare the data acquired from images of the wafers with perovskite layers grown on top of the native oxides.

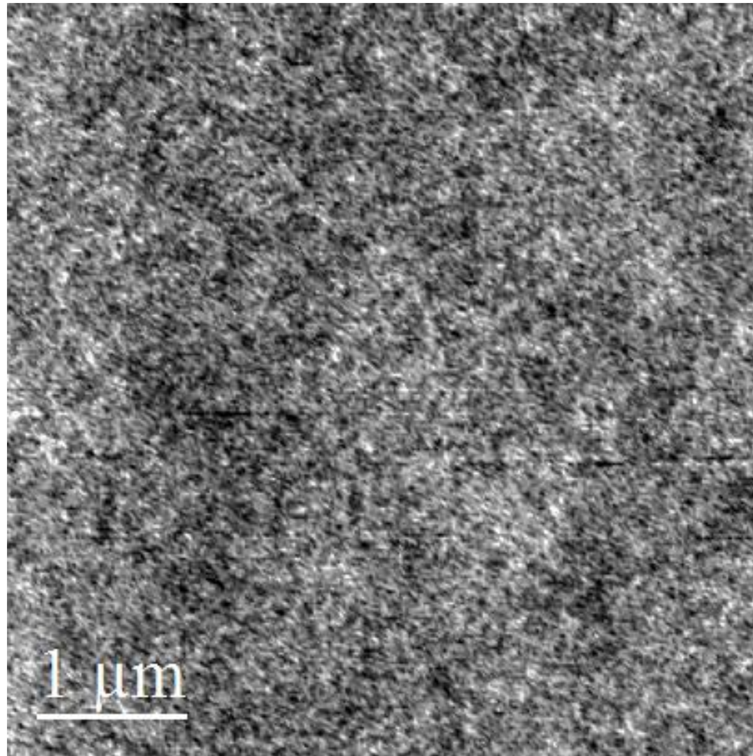


Figure 4.1. AFM image of 5µm × 5µm Si wafer.

The root mean squared (RMS) surface roughness of this sample is 0.33nm and minimum and maximum heights are -2.09 and 6.7nm respectively.

Figure 4.2 shows the AFM images of areas of 5×5 μm^2 for each wafer with a thin layer of $BaTiO_3$ (a: 2nm, b: 8nm) and $SrTiO_3$ (c: 2nm, d: 8nm nominal thickness). The acquisition time was 1s for all images which again consist of 512 × 512 pixels, yielding a sampling of 9.8nm/pixel. If a feature on the surface

has a lateral width smaller than 9.8 nm, it will not contribute significantly to the image (under-sampling).

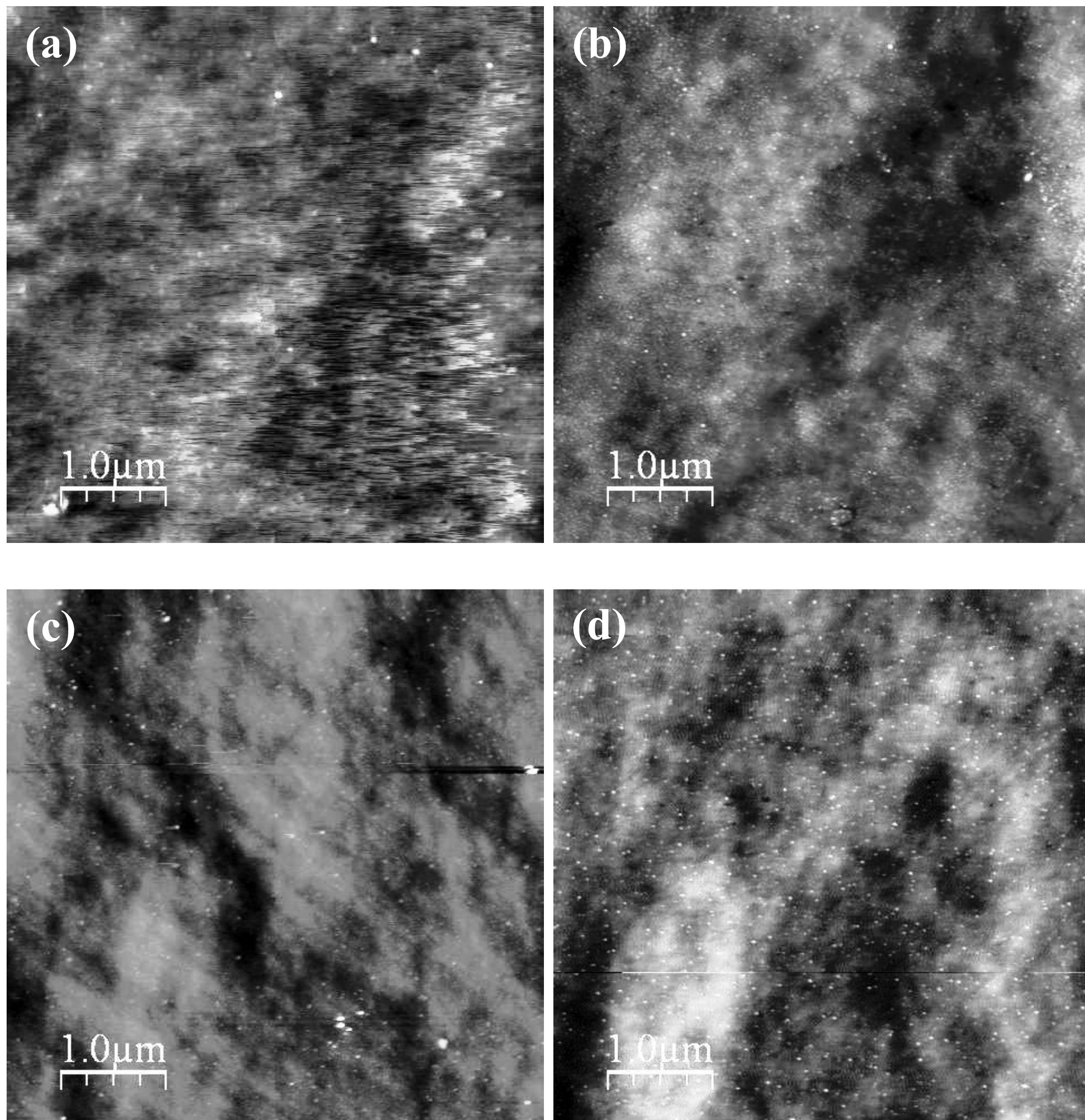


Figure 4.2. AFM images of 5µm × 5µm **(a)** $BaTiO_3$ (2nm) **(b)** $BaTiO_3$ (8nm) **(c)** $SrTiO_3$ (2nm) and **(d)** $SrTiO_3$ (8nm). The image contrast of black and white corresponds to height amplitude of 5nm in all images.

On images (c) and (d) scan artefacts are visible as lines along the horizontal axis. These artefacts can be reduced by changing the scanning tip to a better quality brand or reducing the scanning rate.

There are islands (bright areas) visible on all surfaces, with heights above 5nm, which indicates that the surfaces are rough on the atomic scale. Table 4.1 contains the RMS roughnesses, average heights (set to zero by the software) and peak-to-peak ranges of the four samples.

Table 4.1. RMS roughness, average height, peak-to-peak value, minimum and maximum value (all in nm) of surfaces of $BaTiO_3$(2nm), $BaTiO_3$(8nm), $SrTiO_3$(2nm) and $SrTiO_3$(8nm) layers.

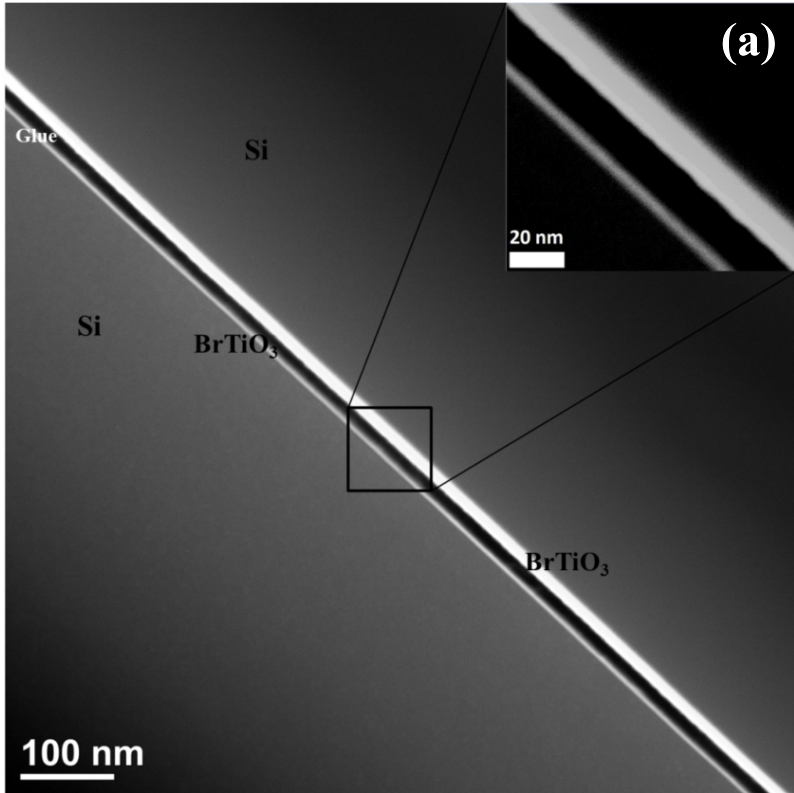
	$BaTiO_3$(2nm)	$BaTiO_3$(8nm)	$SrTiO_3$(2nm)	$SrTiO_3$(8nm)
RMS roughness	0.48	0.61	0.55	0.57
Average height	0	0	0	0
Peak-to-peak amplitude	7.96	7.81	17.86	12.84
Min value of *z* amplitude	-1.92	-2.37	-1.95	-6.39
Max value of *z* amplitude	6.04	5.44	15.91	6.45

The minimum values of the *z* amplitude of the surfaces of the samples indicate that in some areas of the samples with 2nm perovskite layers the top layer is almost gone (the minimum values are around -2nm, which means the tip actually reaches the oxide layer underneath the perovskite). The maximum values of amplitudes show the peak height of the islands in figure 4.2. The value is largest for the sample with 2nm $SrTiO_3$ which might be due to contamination on the surface.

The large values of the height of islands on the surface of perovskite layers as well as the relatively large RMS surface roughnesses (compared to the RMS surface roughness of Si wafer with native oxide, figure 4.1) indicate that the layers are not atomically smooth, which means the layers might be poly-crystalline instead of single-crystalline. ADF and BF-STEM images from the stack of Si/SiO_2/perovskite have been acquired to test this assumption.

Figures 4.3(a) and (b) are the ADF and BF-STEM images of the cross-sectional sample of $BaTiO_3$ acquired with electron beam size of 0.3 nm and dwell time of 19.5μs. The beam convergence semi-angle is equal to 9.5mrad; the collection angles are equal to 0-10mrad for BF and 55-170 mrad for ADF. The field of view of 844nm for both images consists of 4096 × 4096 pixels at a sampling rate of 0.21nm/pixel.

The layers in the stack, from bottom left to top right, are Si/SiO_2/$BaTiO_3$(2nm)/glue/$BaTiO_3$(8nm)/SiO_2/Si.



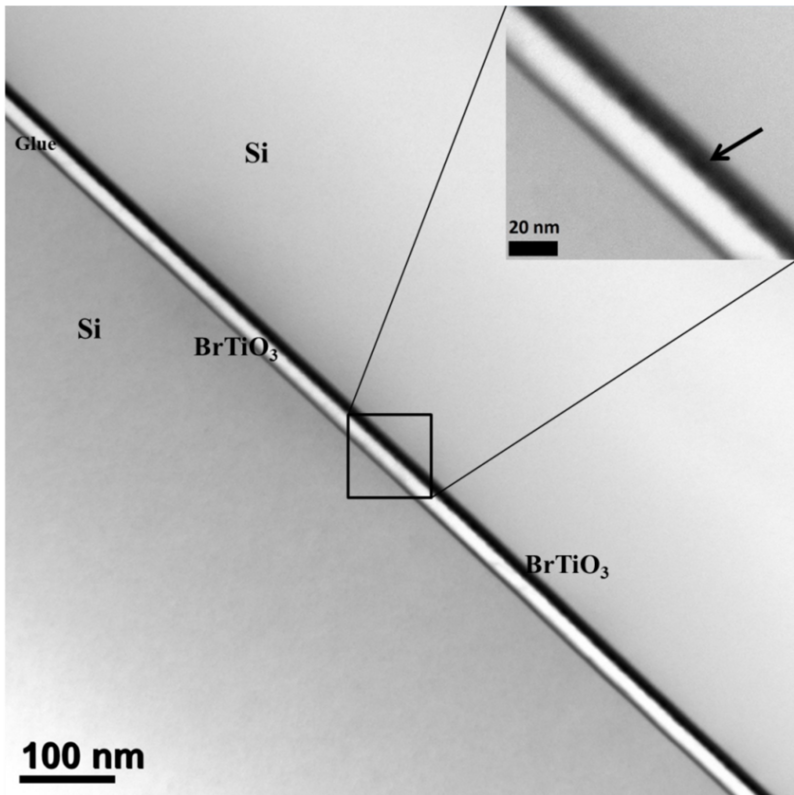
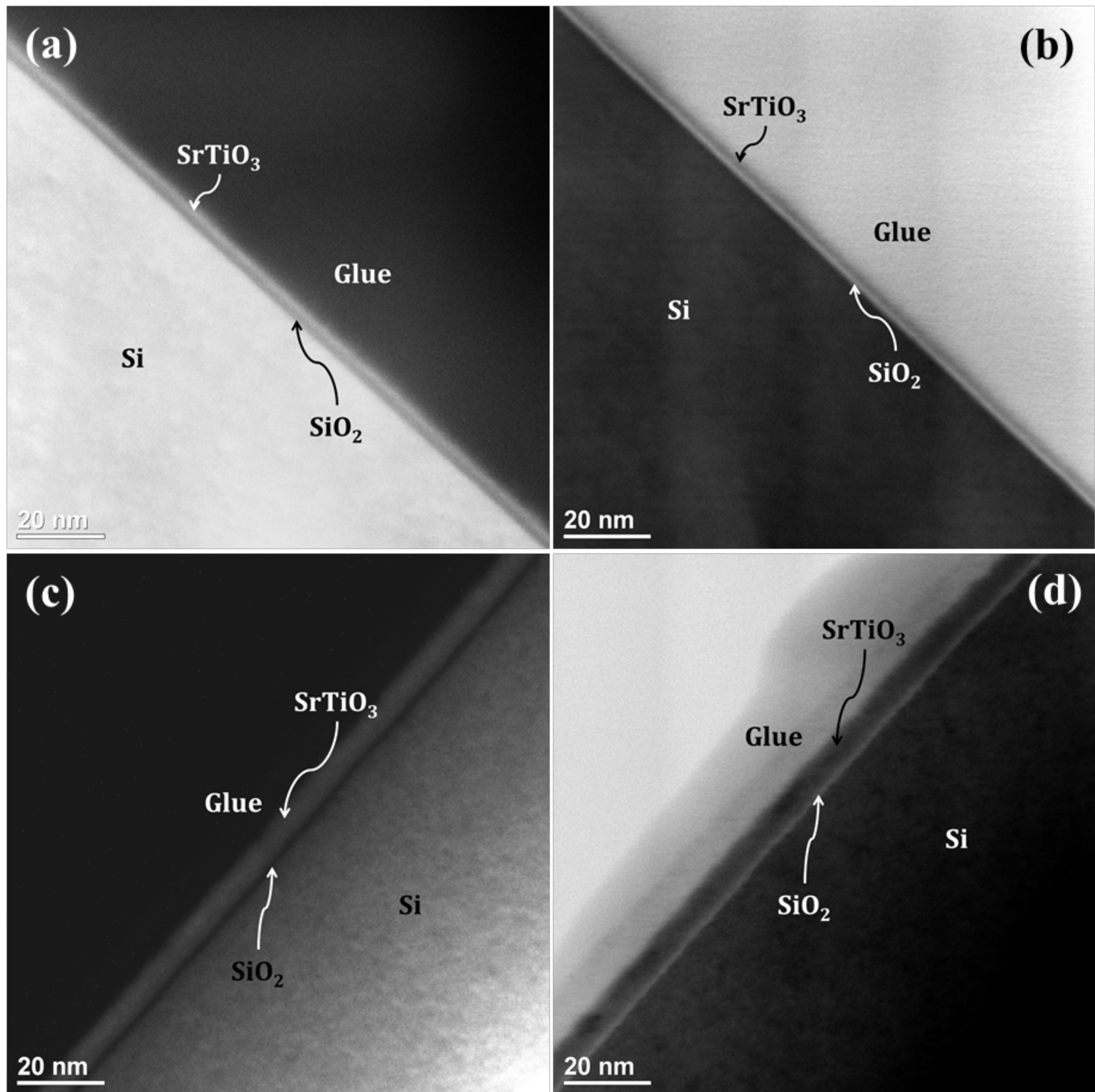


Figure 4.3. (a) ADF-STEM and **(b)** BF-STEM image of cross-sectional sample of $BaTiO_3$ (2 and 8nm titanate layers appear bright in dark-field and dark in bright field images, respectively).

In the magnified area of the BF image the difference of contrast along the 8nm layer confirms that the perovskite layer is not an epitaxially grown single-crystalline layer but poly-crystalline (indicated by an arrow on the magnified image of the 8nm layer).

The corresponding BF and ADF-STEM images of cross-sectional samples of $SrTiO_3$ (2nm and 8nm) are shown in figure 4.4. The field of view of 123.8 nm in the original images was scanned with 2048 × 2048 pixels at the dwell time of 19.5µs, which gives a sampling equal to 0.06nm/pixel.

The images in figure 4.5 are magnified sections of the images in figure 4.4 to have better vision of the layers and the change of contrast along them. In the bright field images (shown by the arrows on images 4.5 a and c), lateral fluctuations in contrast along the $SrTiO_3$ layers can be observed which indicates the layers are not single-crystalline.



4.4. (a)ADF-STEM and **(b)**BF-STEM image of cross-sectional sample of $SrTiO_3$ (2nm). **(c)** ADF-STEM and **(d)** BF-STEM image of cross-sectional sample of $SrTiO_3$ (8nm).

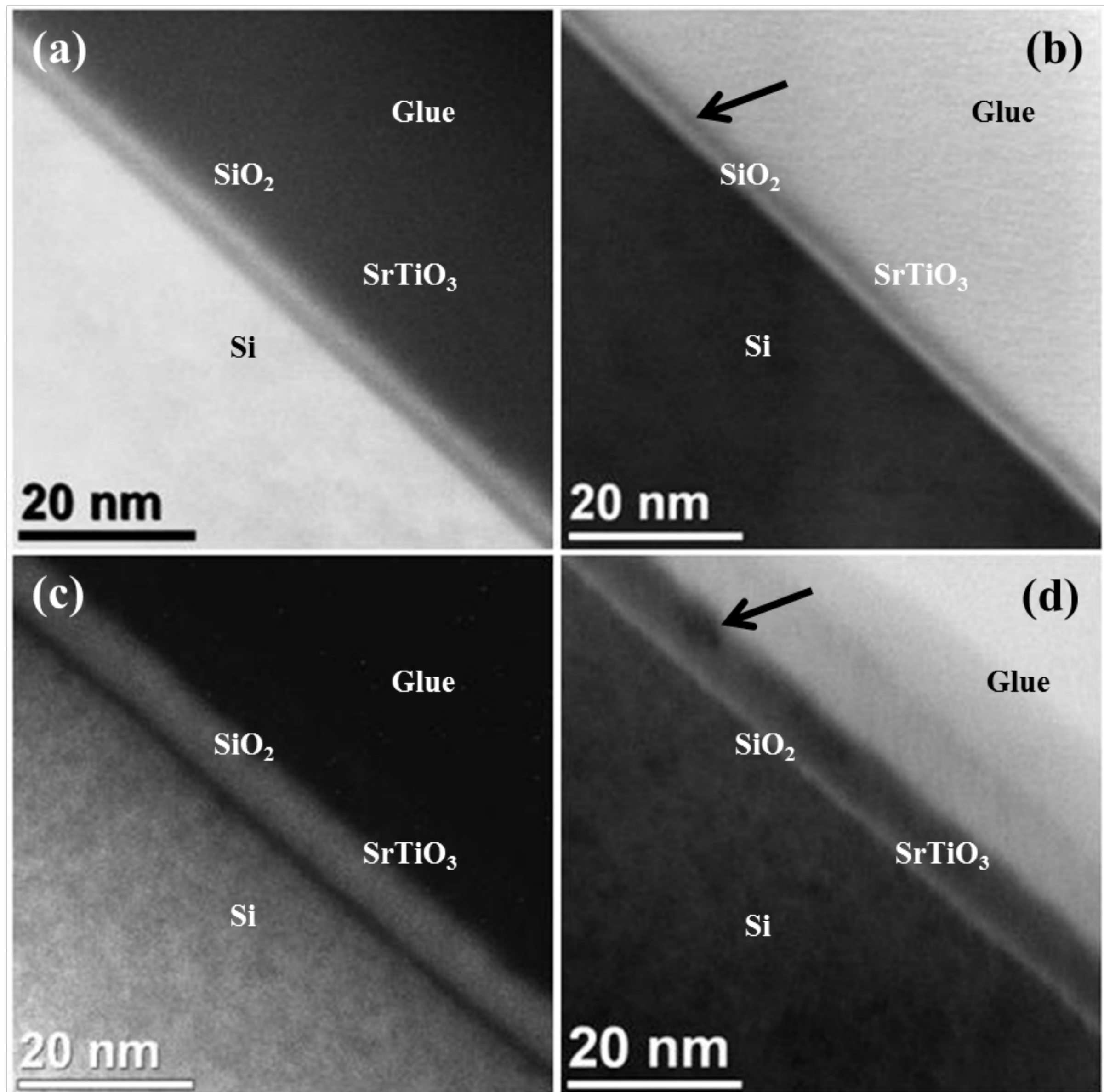


Figure 4.5. Magnified areas of **(a,b)** ADF and BF-STEM images of 8nm $SrTiO_3$ and **(c,d)** ADF and BF-STEM images of 2nm $SrTiO_3$

To obtain the roughness from the original STEM images:

- first the images have been converted to binary format using thresholding in ImageJ programme
- A MATLAB code was applied to each image column from left to right, to work out where the transition from 0 to 1 occurs, which locates the surface of the perovskite layer. (See the appendix)
- Knowing these points for all image columns, we have a plot of a nearly linear curve with noise and oscillations, both of which I tried to eliminate by linear least-squares fitting and calculating a straight line that best fits the data.
- The difference between the real data and the linear estimate describes the roughness of the surface of layers.
- The standard deviation of this data is the root-mean-square (RMS) interface roughness in projection.
- Changing the threshold (between 0 and 255) should not have any effect on the RMS roughness of the layer. (For all the premier results shown below the threshold was 128)

Figure 4.10 shows the roughness data acquired from the ADF and BF-STEM images shown in Figures 4.3 for both 8 and 2nm $BaTiO_3$.

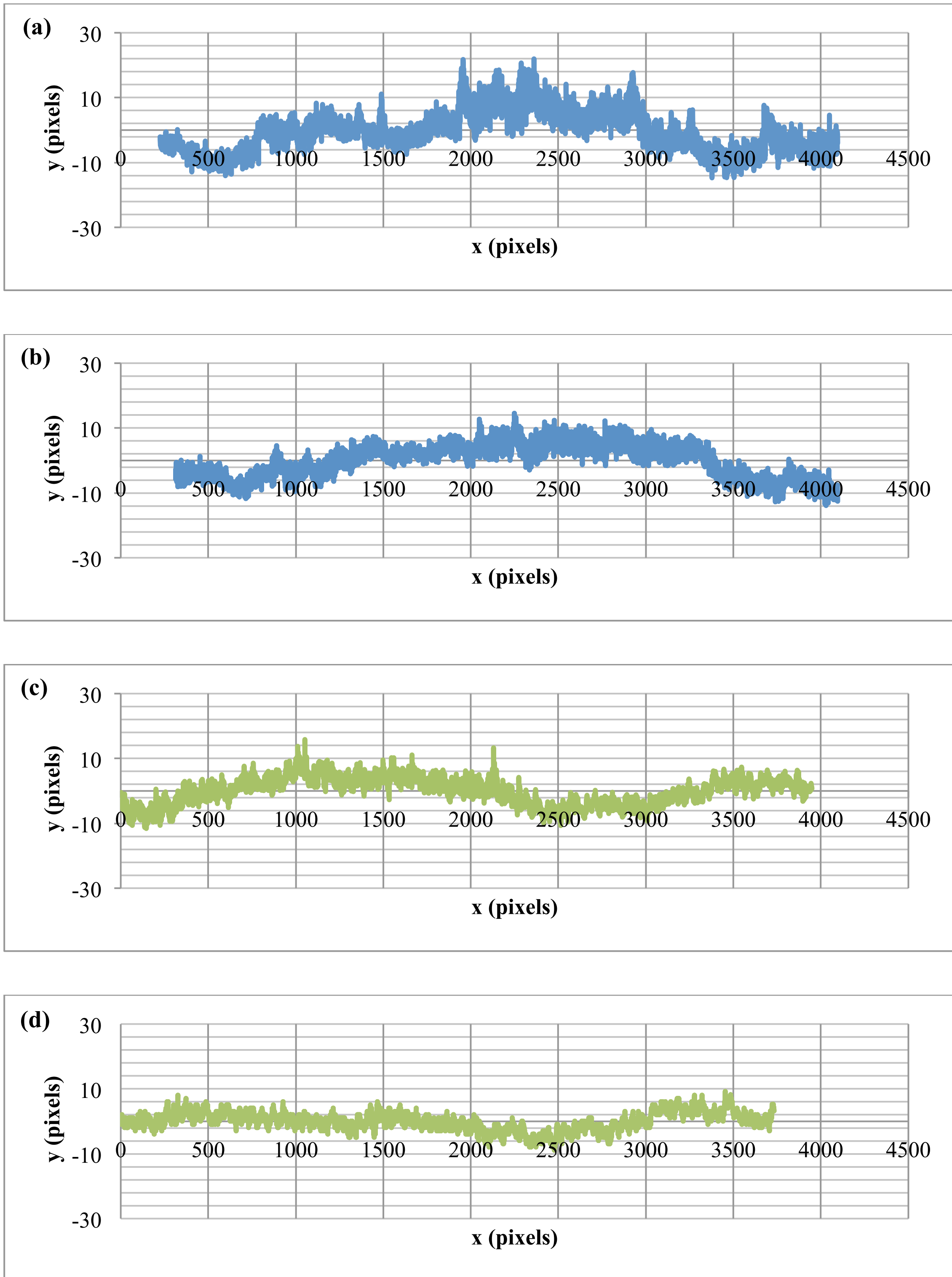


Figure 4.10. The projected surface roughness acquired from (a) the ADF and (b) BF-STEM image of 8nm BTO and (c) the ADF and (d) BF-STEM image of 2nm BTO.

Simillarly figure 4.11 shows the aquired data from both ADF and BF-STEM images of 8 and 2nm $SrTiO_3$.

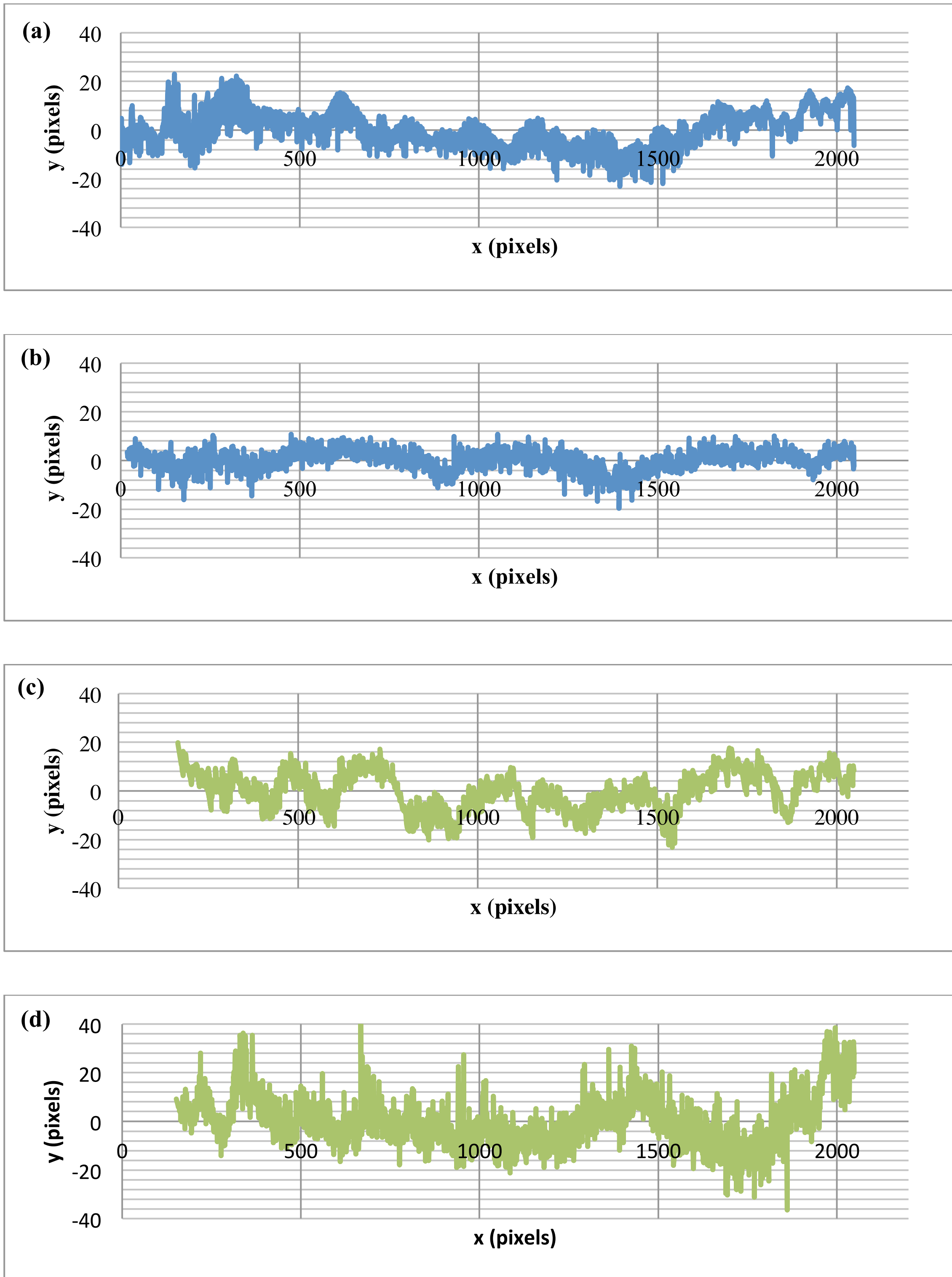


Figure 4.11. The projected surface roughness acquired from (a) the ADF and (b) BF-STEM image of 8nm STO and (c) the ADF and (d) BF-STEM image of 2nm STO.

Table 4.2 compares the RMS surface roughnesses of all four samples measured from AFM with the projected interface roughnesses calculated from STEM.

Table 4.2. RMS roughness in nm, measured from the AFM images and projected interface roughness from the ADF and BF-STEM images.

	$BaTiO_3$(2nm)	$BaTiO_3$(8nm)	$SrTiO_3$(2nm)	$SrTiO_3$(8nm)
AFM	0.48	0.61	0.55	0.57
ADF-STEM	1.09	0.58	0.73	0.53
BF-STEM	1.32	0.87	0.38	0.39

As STEM measures the interface roughness projected along the sample thickness, small protrusions/indications will smear out, therefore the roughness value from STEM images are expected to be smaller than the true values. Similarly in AFM, for very thin and probably poly-crystalline layers (2nm) the grains are probably smaller than the tip radius and also smaller than the sampling rate used and integration over several grains would also reduce the apparent surface roughness. Also the STEM images are from a cross-sectional cut (around 850nm long for the $BaTiO_3$ layers and 400nm for the $SrTiO_3$ layers) of the samples and depending on the area of the wafer which has been used to make the cross-sectional samples the data acquired from them might or might not represent the AFM results from the surface of the samples. In the case of our samples, the AFM surface roughnesses and STEM projected interface roughnesses agree with each other within ±2Å, except for the 2nm $BaTiO_3$ sample which might be due to contaminations.

Same calculation has been applied to the interfaces between the native oxide and the perovskite layers with the aim to compare the results with the AFM measurement results and also to check if the roughnesses of the perovskite layer

surfaces might follow the roughnesses of the interface between the perovskite layers and the native oxide. Figure 4.12 is an example of these calculations, specifically for the BF-STEM image of the nominally 8nm $BaTiO_3$, which should be compared to figure 4.10(b).

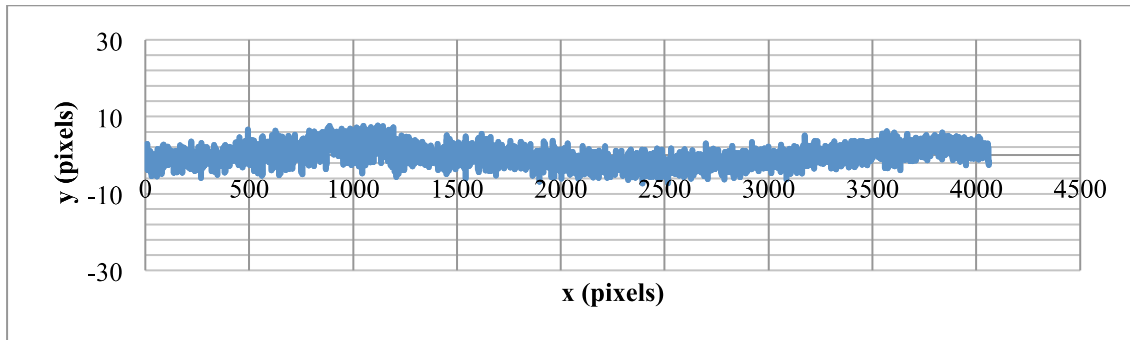


Figure 4.12. The projected interface roughness of the native oxide to the nominally 8nm $BaTiO_3$ driven from the BF-STEM image shown in figure 4.4(d).

The RMS roughness of the interface of native oxide and perovskite calculated from the graph is 0.52 nm and the correlation coefficient between this graph and the graph from the surface of 8nm perovskite is 0.28 which means there is a very weak positive correlation between the bottom and top interface roughnesses. I calculated the interface roughnesses of bottom and top interfaces of the same area from other images to see if this result was reproducible which would mean that there was a correlation between these two interfaces but the results where different from it, which once again confirms that the perovskite layers were not grown as single crystals. Also the same calculation has been done for the 2 nm $BaTiO_3$ layer. The correlation between the bottom and top interfaces for 2nm $BaTiO_3$ is 0.08 and means the correlation between two interfaces is nearly zero.

To check if thresholding has any effect on the results, the data processing has been done for the BF-STEM image of 8nm $BaTiO_3$ with thresholds of 200 and

100 counts as well. Figure 4.13 shows the projected surface roughnesses for these thresholds.

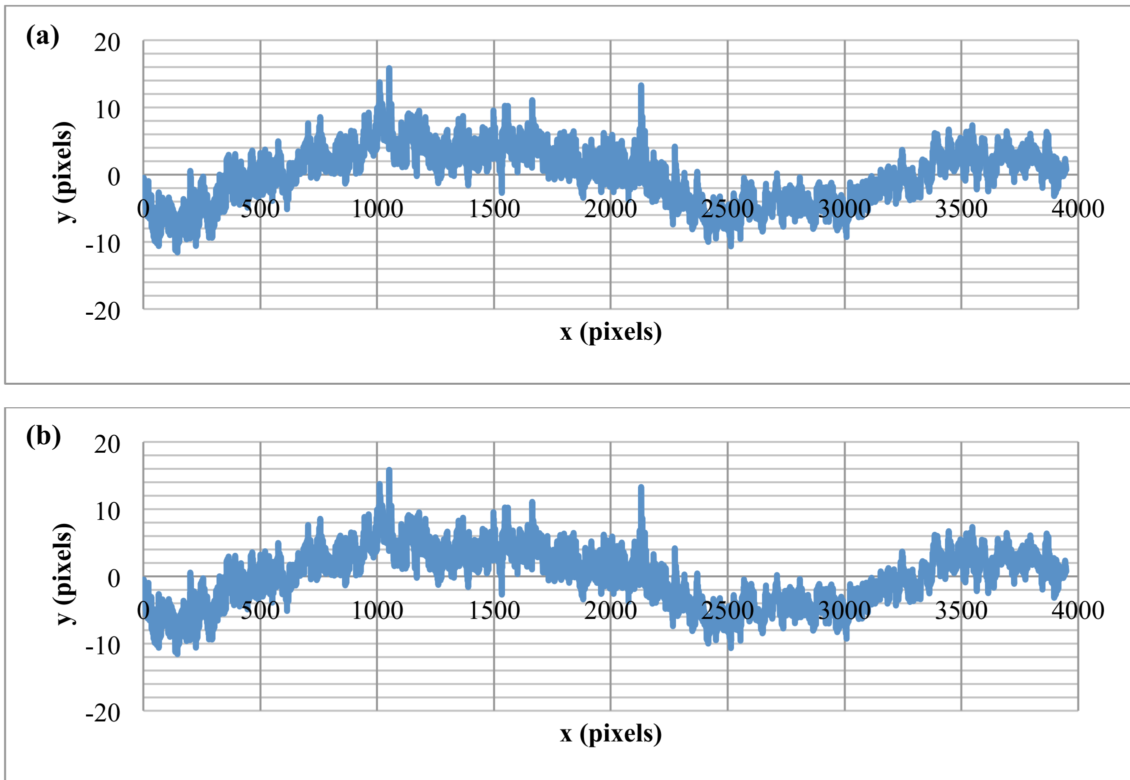


Figure 4.13. The projected surface roughness driven from the BF-STEM image of a nominally 8nm BaTiO3 shown in figure 4.3(b) for a threshold of **(a)** 100 and **(b)** 200 counts.

The calculated RMS projected interface roughnesses for 8nm $BaTiO_3$ with the thresholds of 100 and 200 counts are identical to the result of 0.87nm calculated for a threshold of 128 counts.

Using the ellipsometer, the thicknesses of perovskite layers for all four wafers have been fitted. Using the intensity profile integrated over 500 nm along the perovskite layers on the STEM images, the thicknesses of these layers have been measured using full width at half maximum (FWHM) value and compared to the results from the ellipsometer. Table 4.3 compares the thicknesses of perovskite layers measured by ellipsometry and STEM imaging.

Table 4.3. Thicknesses of perovskite layers in nm, measured by ellipsometry and from the STEM images

	$BaTiO_3$(8nm)	$BaTiO_3$(2nm)	$SrTiO_3$(8nm)	$SrTiO_3$(2nm)
ADF-STEM	10.32	2.68	5.92	1.82
BF-STEM	10.94	2.89	5.79	1.4
ellipsometry	9.22	2.31	5.59	2.39

Thicknesses of both $BaTiO_3$ layers and the nominal 8nm $SrTiO_3$ layer as measured by STEM are ~10% larger than what ellipsometry suggests. For the 2nm $SrTiO_3$, the thicknesses calculated from the BF and ADF-STEM images are smaller than the value calculated using the ellipsometer, ~50% and 17% respectively. This may be due to uncertainties in the complex dielectric function of the perovskite.

4.4 Conclusion

The thicknesses and surface roughnesses of thin layers of (Sr, Ba)TiO_3 grown on silicon substrates with native oxide have been investigated using AFM, ellipsometry and STEM and then have been compared. From our data it appears likely that the thinnest perovskite layers (~2nm) have an RMS roughness of at least 0.7-1.1 nm, which indicates that the layers may not be completely continuous.

The very weak correlation between the two interface surface roughnesses calculated from top and bottom sides of the perovskite layers has shown that the RMS roughness of the top interface of the perovskite layer is independent of the roughness of the bottom interface and the relatively high RMS surface roughnesses of the perovskite layers (compared to the interface roughness of

oxide to perovskite layers) indicate that the layers are not epitaxially grown but are poly-crystalline.

For $BaTiO_3$ perovskite layers with nominally 8nm thickness it has been shown that the actual thickness is larger than the nominal thickness (in all three methods of measurements) and for the $SrTiO_3$ layer it is the opposite.

Poly-crystalline perovskite layers which have been grown on silicon lead us to the next step of this study which is finding out a strategy to re-crystalline the layers to grow GaAs epitaxially on top of them.

Chapter 5:

Anneal strategies to re-crystallize perovskite layers

5.1 Introduction

As discussed in the previous chapter, the perovskite layer is grown poly-crystalline on the silicon substrate rather than epitaxially, therefore in order to be able to grow III-V material epitaxially on top of it, it will be necessary to anneal the sample and recrystallize the perovskite layer to have a surface as smooth and flat as possible.

Both anneal and overgrowth processes are done using MBE and the process is observed by in-situ RHEED as well as ex-situ AFM. A brief introduction to MBE and RHEED has been presented in chapter three. The surface reconstruction of Si and perovskite materials is reviewed here in more detail, as it is the key point to get the right strategy to anneal and overgrow the perovskite thin layer.

The growth of the commercial $SrTiO_3$ samples used in this study was by the Verneuil process and the direction of cutting [100]. The Verneuil (or flame fusion) process is a method of manufacturing synthetic crystals. First developed in 1902 by the French chemist Auguste Verneuil, this process was used to produce the ruby and sapphire, as well as rutile and strontium titanate [49]. In this process, a powdered substance is melted using an oxyhydrogen flame and then crystallized from melt into droplets.

The annealing studies on pure $SrTiO_3$, GaAs and Si substrate are done in an MBE chamber and the results are used to calibrate the temperature of the MBE system as well as to decide the strategies for anneal and overgrowth of Si substrate samples with perovskite layers.

5.2 Basics of surface reconstruction

To epitaxially grow III-V semiconductor compound materials on silicon the buffer layer needs to be single crystalline and perfectly flat. Studying the surface reconstruction of perovskites can help develop a strategy to grow III-V materials epitaxially on perovskite. But what is surface reconstruction? Assuming an ideal infinite crystal, each atom in the crystal lattice is in equilibrium by balancing the forces, which are applied by all other atoms. If the crystal has a free surface, which means the crystal is terminated along a specific plane, the forces exerted on the atoms at or near the surface are changed and this changes the equilibrium position for them. Their former bonding partners are now missing and therefore the electron orbitals re-arrange in order to account for the reduced symmetry. This causes them to occupy different positions and spacings from the bulk. So, the interfaces break the periodicity of the bulk; surface atoms have fewer bonding partners than atoms in the bulk and the symmetry is different, so the surface atoms move to new positions of energetic minima. In other words, they are reconstructed. New 2D unit cells are used to describe this phenomenon.

5.2.1. Surface reconstruction of Si

The surface reconstructions of Si with face-centred cubic (fcc) lattice structure depend on temperature and on which face of the crystal is exposed. Surface reconstruction of Si (001) has been discussed in various books and papers [50-53] because of its importance in the semiconductor industry. The principle

atomic surface structure of Si(001) surface has been first studied in 1959 using LEED (low energy electron diffraction) 046-Surface reconstruction and vibrational excitation of Si 001.pdf [54]. The (2×1) reconstruction was first observed and further investigations led to observation of higher periodicities (c(4×2) and p(2×2)). Figure 5.1 shows the schematic diagram of bulk, (2×1), p(2×2) and c(4×2) reconstructed silicon (001) surfaces [55].

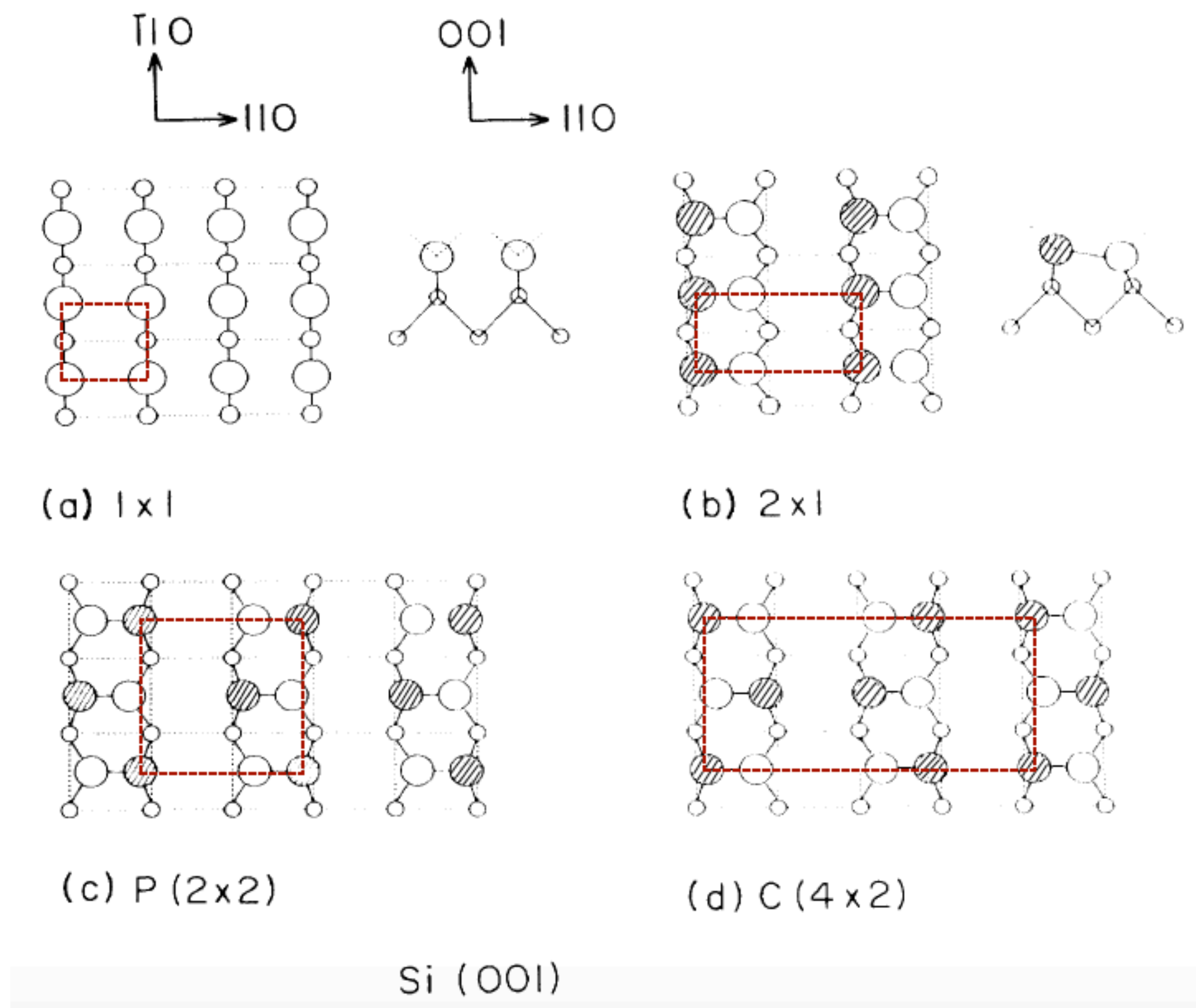
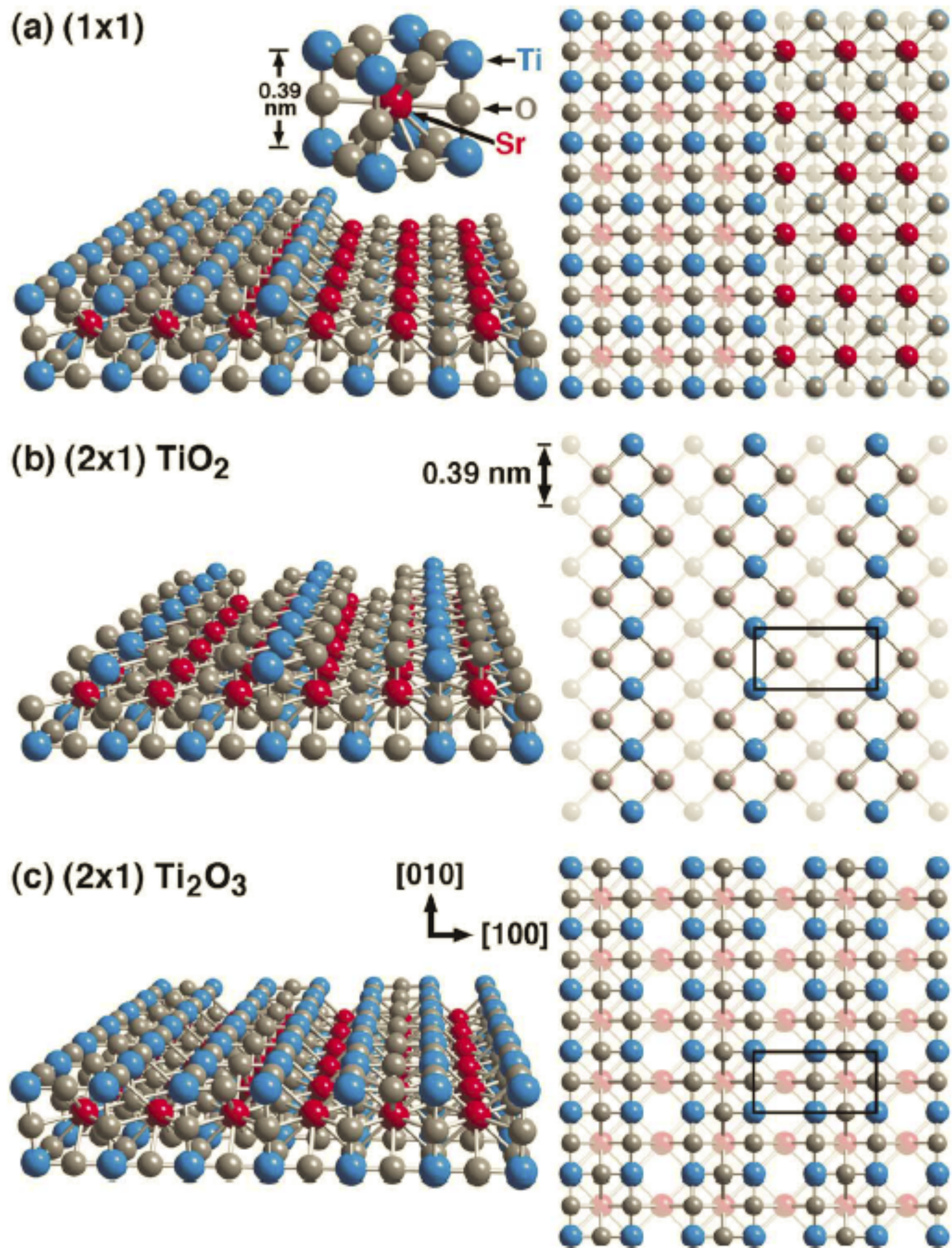


Figure 5.1. **(a)** Unreconstructed silicon surface compared to **(b)** 2×1, **(c)** p(2×2) and **(d)** c(4×2) reconstructed silicon surfaces [55] (As shown in **(b)** the shaded atoms are in higher positions than the in-plane ones)

5.2.2. Surface reconstructions of perovskite materials

Investigating the surface of perovskite oxides is important due to various applications of these materials such as high capacity computer memory cells, substrates for high-T_c cuprate superconductor growth, etc. in semiconductor and opto-electronics industry [56-61]. In the previous chapter the surface roughness of perovskite thin layers grown on silicon was investigated and compared using different methods (TEM, STEM, AFM, and ellipsometry). Knowing the possible reconstructions of a perovskite surface as well as its roughness and crystal structure can lead to a better overgrowth strategy. Therefore a review of previous studies of perovskite surface reconstructions has been performed.

Figure 5.2 shows the common reconstructions on $SrTiO_3$ surface that have been studied in [62]. The cubic bulk structure of the perovskite unit cell is shown in figure 5.2 as well. Blue spheres represent the Ti atoms, which sit on each corner. Grey spheres are oxygen (O) and red are Sr atoms, which sit in the middle of the unit cell. All these reconstructions assume that Ti and O atoms (i.e. effectively TiO_2) terminate the surface.



(Figure continued on the next page)

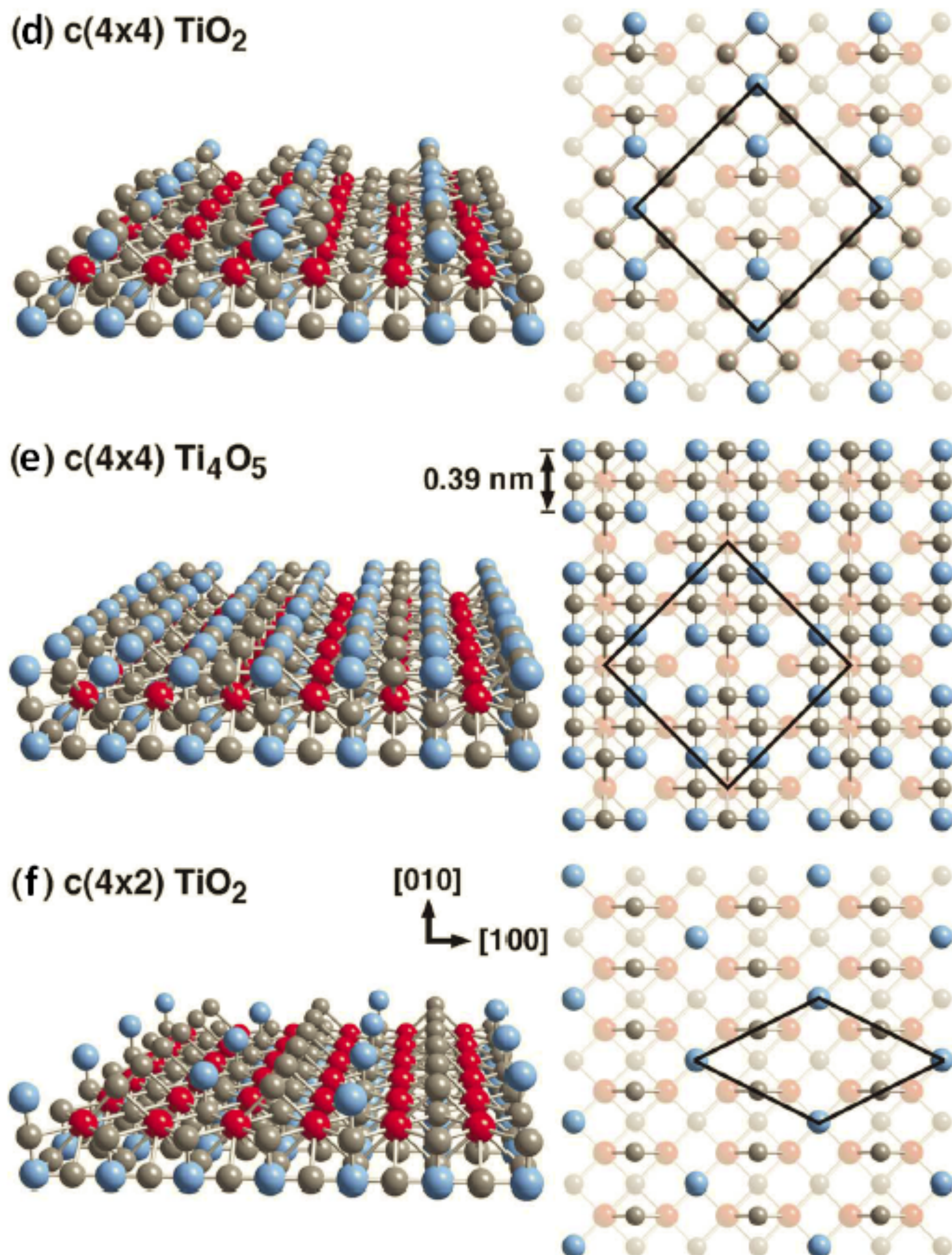


Figure 5.2. **(a)** A (001) surface with the two possible (1×1) terminations (TiO_2 on left, SrO on right) shown in oblique view (left panel) and in top view (right panel). **(b)** Proposed structure of the (2×1) reconstructed surface with $Ti^{IV}O_2$ stoichiometry. **(c)** Proposed structure of the (2×1) reconstructed surface with $Ti_2^{III}O_3$ stoichiometry. **(d)** is showing proposed structure of the c(4×4) reconstructed surface with $Ti^{IV}O_2$ stoichiometry. **(e)** is the structure of the c(4×4) reconstructed surface with $Ti_4^{2.5}O_5$ stoichiometry. **(f)** is the structure of the c(4×2) reconstructed surface with $Ti^{IV}O_2$ stoichiometry. In **(b), (c), (d), (e)** and **(f)** the reconstructed unit cell is indicated in the top view panels. In all top view panels the atomic layer below the

surface is shown with reduced depth of colour [62]. The roman numbers indicate the valence of Titanium (Only in figure **e** a mixed valence of on average 2.5 is observed).

Theoretically, for an ideal $SrTiO_3$ (001), the surface can be terminated either with TiO_2 or SrO as shown in figure 5.2. But this picture is rather simplified and the structure will depend on pressure and temperature [63]. It has been shown that chemical etching of a $SrTiO_3$ substrate in a buffered NH_4F-HF solution removes any termination of SrO on the surface [64-65]. In case of thin layers of perovskite, etching the sample is tricky and might eliminate the thin layer completely. To avoid this but to obtain a flat perovskite surface terminated with TiO_2, the sample may be annealed at 600℃ under UHV [66]. The third way is to anneal the sample in O_2 atmosphere to avoid oxygen loss from the surface. In this work the second method has been tested to obtain an unreconstructed perovskite surface terminating with TiO_2.

5.3 Calibrating the temperature of the MBE system

Before calibrating the RHEED images, the temperature of the MBE system should be calibrated. The common way of calibrating it is to heat up the sample to a certain temperature for which we know its structural transitions and write down the heating current shown on the monitor. Having three points is sufficient to plot a temperature-current curve for a given specific material in the MBE machine. Assuming the relationship between current and temperature was linear, knowing only two points would be enough to determine the relationship.
The important temperatures for Si substrates that we have used to calibrate the machine are As cap removal, which happens at 300 ± 10 ℃ [67], and oxide removal, which happens at 850 ± 10 ℃ for Si [68]. The other temperature that has been used for Si calibration is the temperature at which the silicon substrate changes colour from orange to red, which is roughly around 600 ± 10 ℃. For $SrTiO_3$ or any other oxide material, the oxide removal temperature cannot be

used, as there is no layer of oxide on top of the substrate. Also, changing the colour of substrate is not applicable for $SrTiO_3$ because the undoped material is almost transparent. Therefore, assuming the system is linear and we can have one calibration point for As cap removal, the second point is obtained by cooling down the system (minimum current=0.001A) and leaving it for more than an hour to settle so that the thermocouple which is connected to the body of the chamber has the same temperature as the sample holder. After an hour the thermocouple shows a temperature reading of -5±10 ℃. The temperature is below zero because of the liquid nitrogen cooling system in the MBE chamber.

For a GaAs substrate, the first point is again the As cap removal temperature. Heating the sample and determining the reconstructions of the surface can obtain the other two points. At the beginning, the GaAs surface has a c(4×4) reconstruction and at 450±10 ℃ this changes to (2×4) and as we continue heating up the sample to 625±10℃ the reconstruction changes to (4×2) [69].

Temperature calibration has been done for Si, GaAs and pure perovskite on the MBE machine used in this work. Tables 5.1 show the temperature calibration for these materials.

Table 5.1. Temperature calibration for **(a)** Si, **(b)** GaAs and **(c)** $SrTiO_3$ in the MBE chamber

Current (A)	**Temperature (℃)**
0.6	300
1.2	600
2.1	850

(**a**) Si

Current (A)	**Temperature (℃)**
0.83	300
1.01	450
1.35	625

(**b**) GaAs

Current (A)	**Temperature (℃)**
0.001	-5
0.7	300

(**c**) $SrTiO_3$

Figure 5.3 illustrates the corresponding curves for table 5.1. The three materials have different slopes as these depend on their heat conductivity. The thermal conductivity of silicon is 149 $W{\cdot}m^{-1}{\cdot}K^{-1}$, for GaAs it is 55 $W{\cdot}m^{-1}{\cdot}K^{-1}$ and for $SrTiO_3$ it is 12 $W{\cdot}m^{-1}{\cdot}K^{-1}$.

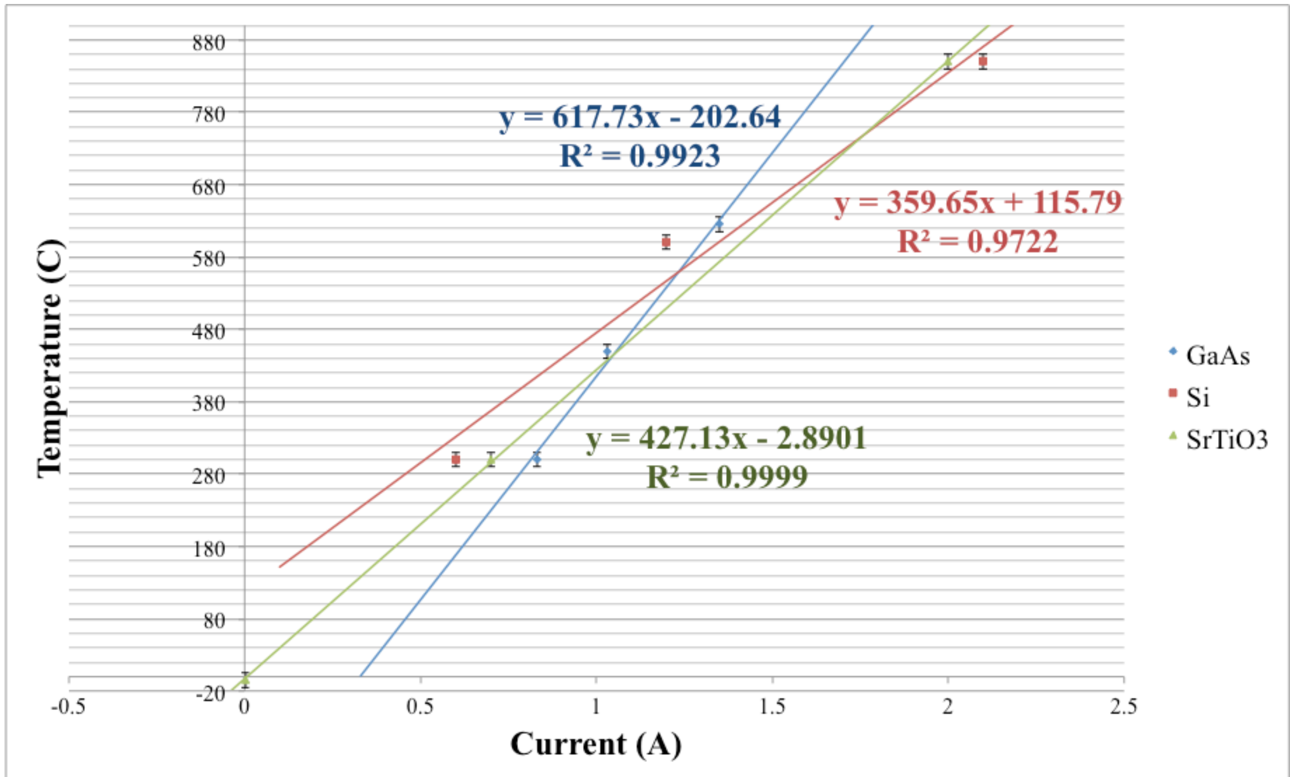


Figure 5.3. The diagrams of measured temperature-current calibration of the MBE system for GaAs (blue), Si (red) and $SrTiO_3$ (green) substrates.

5.4 Results and discussion of post-anneal surface analysis of perovskite sample

To calibrate the RHEED screen, a pure $SrTiO_3$ crystal has been used in the MBE chamber under UHV. To have a better understanding of the RHEED patterns, images have been taken from four different directions: [011], [010], [01$\bar{1}$] and [00$\bar{1}$]. But as the sample was not located exactly in the middle of the chamber between the gun and detector, rotating it caused a change in the position of the beam on the sample surfaces.

The RHEED patterns of pure $SrTiO_3$ surface in the MBE chamber viewed from different directions are shown in figure 5.4. It can be observed from the images that the origin of the beam is not exactly the same for all the images, hence the

camera length should have been changed or the position of the monitor is moved.

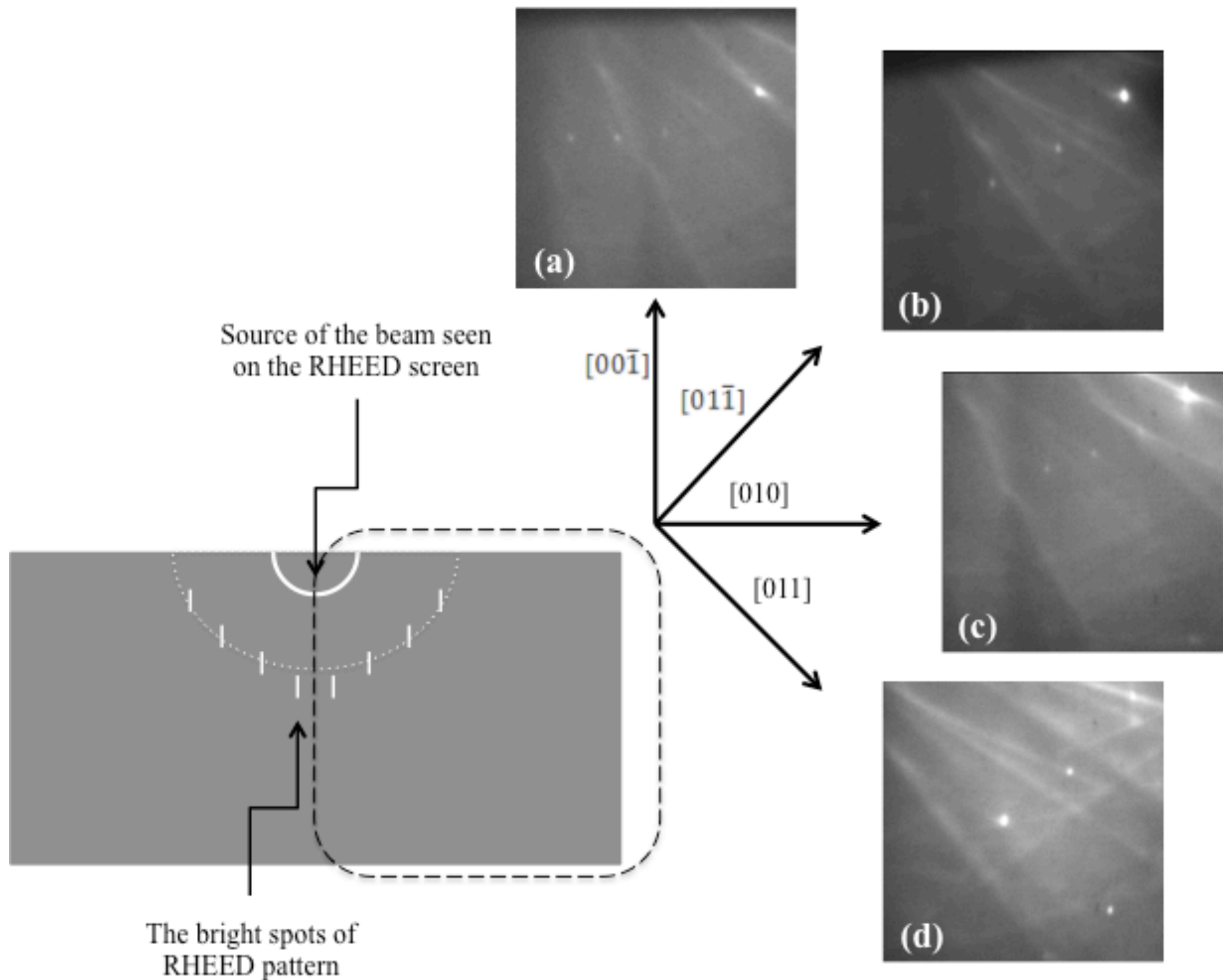


Figure 5.4. The RHEED patterns of pure $SrTiO_3$ surface: The schematic diagram of a typical RHEED pattern of a crystalline surface shown in left bottom corner and the RHEED images as viewed from **(a)** [00$\bar{1}$] **(b)** [01$\bar{1}$] **(c)** [010] and **(d)** [011] directions at 300℃ (current equal to 0.7A).

The current has been increased in steps of roughly 0.08A during anneal process (the temperature increased by 35℃) and we've waited for 30 minutes after each step and recorded RHEED patterns from four directions to monitor the changes of the RHEED patterns as the temperature changed.

In figure 5.4 it can be seen that with 90° rotation of direction of viewing, the RHEED patterns remain almost the same. This means the reconstruction of the surface is (1×1) or (4×4) (bearing in mind that, as was discussed in figure 5.2, among the common surface reconstructions of perovskite, these are the only ones with a square lattice) and of course (1×1) is more common than (4×4). Also the ***g*** vector for c(4×4) should be 4 times smaller than (1×1) which has not been observed on the RHEED patterns. We can therefore conclude that the surface reconstruction is ore likely to be (1×1) at 300℃.

Figure 5.5 shows the RHEED patterns along [010] at different steps of the annealing process. The height change of the sample affects the position of the bright spots on the RHEED pattern and that is the reason for the slight change of the position of these spots on figure 5.5.

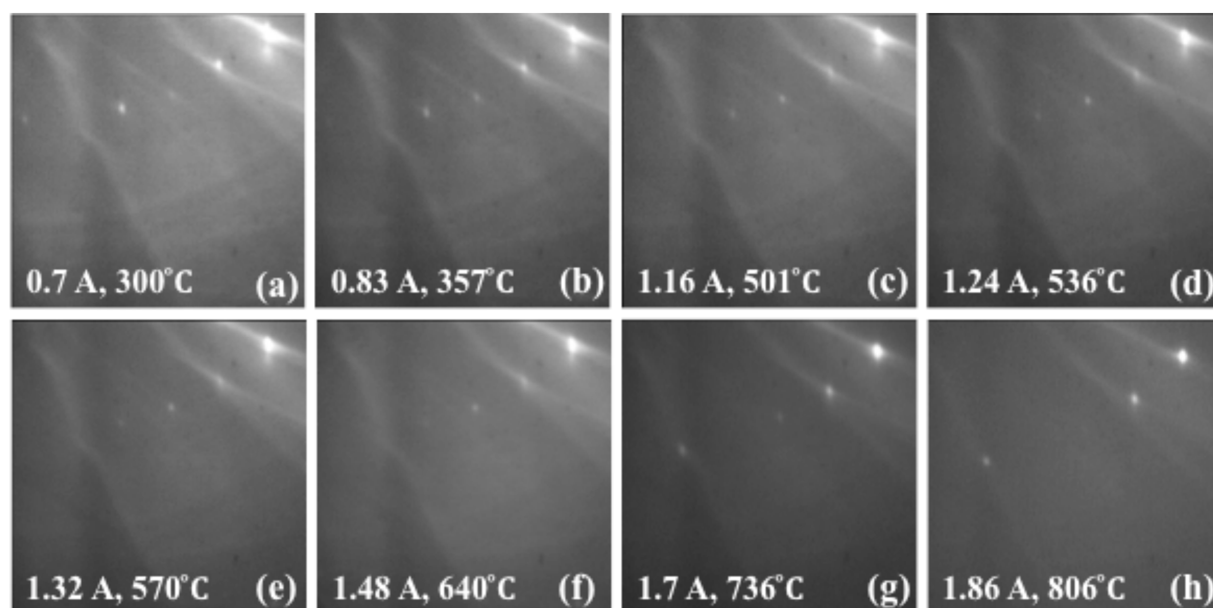


Figure 5.5. The RHEED patterns along [010] direction during 8 steps of the anneal process. The source of the beam is located off the upper left side of all images.

The increase of temperature has not significantly affected the RHEED pattern of the surface of the $SrTiO_3$ sample, which means that in this range of temperature

(between 300 and 800℃ with an error of ±10℃) no change of surface reconstruction occurs.

The RHEED patterns of the perovskite surface are also used as reference to understand the surface reconstruction of perovskite layers on Si in the next stage of this project. The distance between the bright spots in the RHEED patterns after annealing the Si substrates with perovskite layers should be the same as the ones in the RHEED patterns from the pure $SrTiO_3$ (using same position, screen and detector to save the images). Therefore the samples should be heated up till similar RHEED patterns with the same distances as above form on the screen.

Figures 5.6(a, b) show AFM images of areas of 5×5 μm^2 and 10×10 μm^2 of the received bulk pure $SrTiO_3$ sample recorded in the tapping mode. The acquisition time was 0.5s. The image in figure 5.6(a) consists of 1028×1028 pixels (sampling rate of 4.9nm/pixel) and the image in figure 5.6(b) consists of 512×512 pixels (sampling rate of 19.5nm/pixel). Figure 5.6(c) is showing a histogram of the height distribution of the first image (area of 5×5 μm^2).

Similarly, figure 5.7(a, b) show AFM images of areas of 5×5 μm^2 and 10×10 μm^2 after anneal at 800℃ for an hour. The acquisition time was 0.5s. The image in figure 5.7(a) consists of 1028×1028 pixels (sampling rate of 4.9nm/pixel) and the image in figure 5.7(b) consists of 256×256 pixels (sampling rate of 39nm/pixel). Figure 5.7(c) shows the histogram of the height distribution of the perovskite surface extracted from figure 5.7(a).

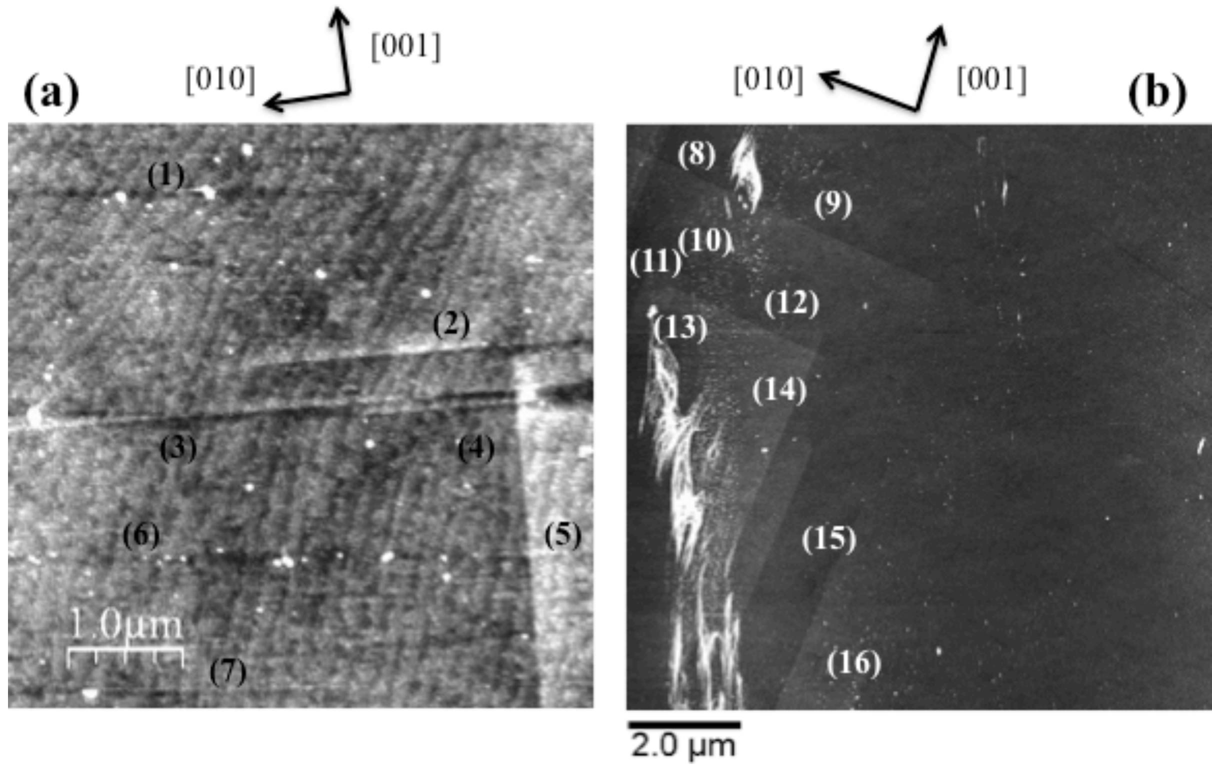


Figure 5.6. AMF images of **(a)** 5×5 μm^2 and **(b)** 10×10 μm^2 as-grown pure $SrTiO_3$. The image contrast of black and white corresponds to a height amplitude of 5nm in both images. Numbers refer to surface steps visible along <010> type directions. **(c)** is the histogram of as-grown $SrTiO_3$ surface topology extracted from the AFM image of area of 5×5 μm^2.

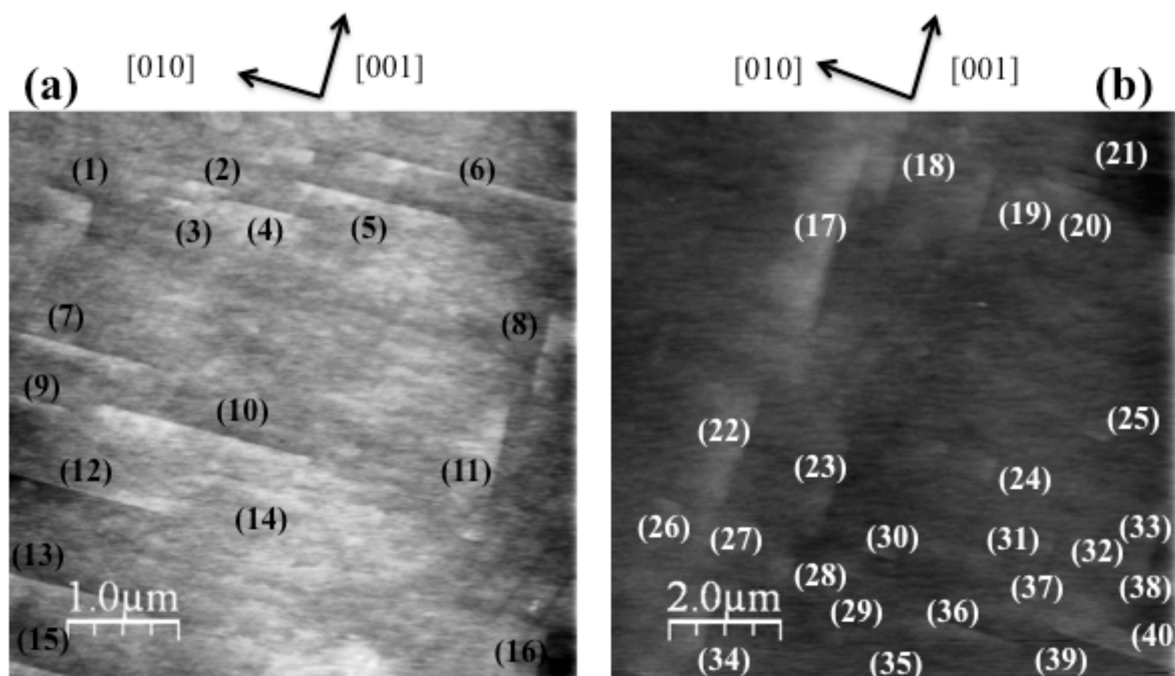


Figure 5.7. AMF images of **(a)** 5×5 μm^2 and **(b)** 10×10 μm^2 pure $SrTiO_3$ after anneal. The image contrast of black and white corresponds to a height amplitude of 10nm in both images. Numbers refer to surface steps visible along <010> type directions. **(c)** is the histogram of $SrTiO_3$ surface topology after anneal at 800℃ for an hour, extracted from the AFM image of area of 5×5 μm^2.

Tables 5.2(a,b) lists the direction of each atomic step and the height of each of them on the surface of pure perovskite in the images of figure 5.6. The heights are measured using profiles across each step.

Tables 5.2. Measured heights and directions of the steps on the surface of received pure perovskite shown in figure 5.6(a) and (b) respectively.

(a)

Steps	Direction	Height (nm)
1	-	-
2	[001]	0.24
3	[001]	0.22
4	[001]	0.22
5	[010]	0.43
6	-	-
7	-	-

(b)

Steps	Direction	Height (nm)
8	[010]	0.25
9	[001]	0.23
10	[010]	0.44
11	[010]	0.24
12	[001]	0.21
13	[010]	0.23
14	[010]	0.41
15	[010]	0.84
16	[010]	0.42

Odd multiples of $a/2$
Even multiples of $a/2$

The same measurements have been done for the images in figure 5.7(a,b) and are listed in tables 5.3(a,b).

Table 5.3. Measured heights and directions of the steps on the surface of perovskite after anneal at 800℃ for an hour, shown in figure 5.7(a) and (b) respectively.

(a)

Steps	Direction	Height (nm)
1	[001]	0.64
2	[001]	0.44
3	[001]	0.63
4	[001]	0.45
5	[001]	1.21
6	[001]	0.64
7	[001]	0.61
8	[010]	0.41
9	[001]	0.24
10	[001]	0.43
11	[010]	0.43
12	[001]	0.22
13	[001]	0.43
14	[001]	0.63
15	[001]	0.44
16	[010]	1.24

(b)

Steps	Direction	Height (nm)
17	[010]	0.45
18	[010]	0.41
19	[010]	0.24
20	[001]	0.38
21	[001]	0.43
22	[010]	0.63
23	[010]	0.43
24	[010]	0.24
25	[001]	0.22
26	[001]	0.43
27	[010]	0.21
28	[010]	0.44
29	[001]	0.42
30	[001]	0.41
31	[001]	0.22
32	[010]	0.18
33	[010]	0.23
34	[001]	0.61
35	[001]	0.45
36	[001]	0.25
37	[001]	0.42
38	[001]	0.57
39	[001]	0.41
40	[001]	0.44

Odd multiples of $a/2$
Even multiples of $a/2$

In figure 5.6, steps are visible on the surfaces and are marked with numbers on both images. The RMS roughnesses of the sample surface before and after anneal are 0.23nm and 0.45nm, respectively, which means it is nearly doubled after anneal.

The steps numbered as (1), (6) and (7) in figure 5.6(a) are not parallel to any of the directions expected and look like scanning artefacts rather than steps on the surface. The wavy effect visible in the image on figure 5.6 (a), with ~0.32 nm high steps ~75nm apart along [031] direction, can be due to the step-flow during growth.

As shown in figure 5.6 and table 5.2, before the anneal process, there are around 13 steps per 125 μm^2 with heights that are approximately multiples of 0.2nm (half of the lattice constant of perovskite) on the surface of the sample. According to figure 5.7 and table 5.3, the number of these steps has become significantly higher after anneal (40 steps per 125 μm^2), illustrating that the roughness of the sample increases after anneal. The height of the steps varies between 0.2nm (half a unit cell) and 1.2nm (3 unit cells).

The average height of the surface of the perovskite before the anneal was 0.65nm, however it was 2.24nm after anneal (comparing the histograms shown on 5.6(c) and 5.7(c)). Before anneal, there were few islands visible on the surface with heights significantly above the average, but the number of them was low. After annealing, these islands have dissolved and the terraces on the surface look smoother than before. The peak-to-peak value decreases after anneal as well. For the sample before annealing the peak-to-peak value is 10.9nm but after anneal sample has a peak-to-peak of only 4nm.

The number of steps along [001] is five in total. All of them have heights of roughly 0.2nm, which are visible in figure 5.6. There are 8 edges along [010] direction. 3 of them have heights of roughly 0.2, four with heights of 0.4 and only one edge with a height of 0.8nm. In the tables the sharp edges with height

of odd multiples of $a/2$ are marked in blue and the ones with even multiples in red. It gives us the ratio of 8:5 over the area of 125 μm^2 before anneal.

The image after anneal shows more sharp edges in both directions. In figure 5.7 the number of visible atomic steps along [001] direction is 27, five of them with heights of 0.2nm, fourteen with heights of 0.4nm, seven with heights of 0.6nm and one with height of 1.2nm. Along [010] direction, there are 13 visible terrace edges; five of them have heights of 0.2nm, six have heights of 0.4nm, one has height of 0.6nm and another one with 1.2nm (equal to 6 monolayers).

Same statistical analysis for the heights of even and odd multiples of half of the lattice constant has been done for the area of 125 μm^2 which give us the ratio of 18:22 for after anneal images.

The persistence of $(2n+1)\times a/2$ terraces (marked as blue font in the tables) after anneal process, shows that the anneal hasn't given the results expected which was to remove any SrO termination [62]. This may cause the over-growth of GaAs in the next step of the project to not be epitaxial. In other word, termination of the surface of perovskite in both TiO_2 and SrO, causes the atoms of GaAs configure in opposite order to the ones in the perfect lattice in some areas [70]. Therefore crystallographic defects appear on the surface, which is called anti-phase domain (APD). The APDs produce anti-phase boundaries (APBs) [71]. An example of APDs and APBs caused by growth of GaAs film on Si with surface containing a demistep, is shown in figure 5.8 [72].

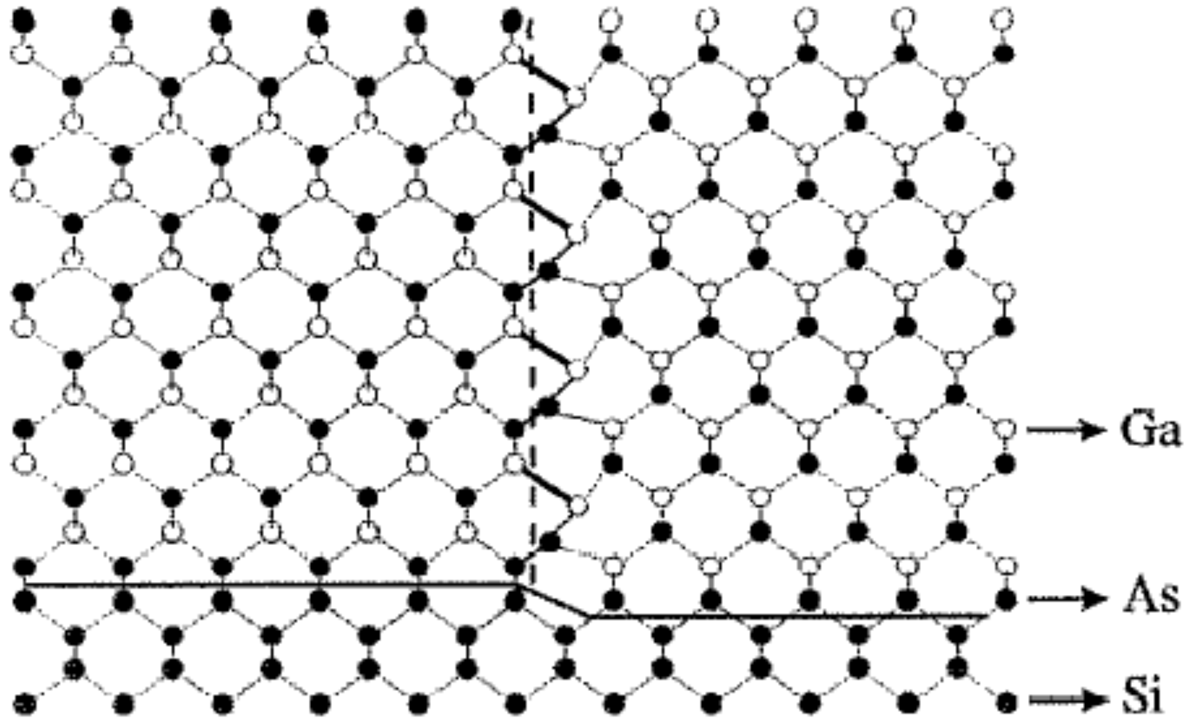


Figure 5.8. [110] projection of a GaAs film grown on [00l] Si substrate. The Si surface contains a demistep which introduces an APB, indicated by the dashed line, in the GaAs epilayer. Notice the difference in the bond lengths between like atoms. [72]

5.5 Conclusion

In this chapter the surface reconstruction of $SrTiO_3$ has been studied by in-situ RHEED and then compared for samples with and without anneal using AFM.

For the as-received pure $SrTiO_3$ the AFM images show few atomic steps (13 over area of 125 μm^2) along [010] and [001] directions but there are also indications of step-flow growth. Also some islands with a density of ~ 1/ μm^2 and maximum heights of around 10nm are visible on the surface, resulting in low over-all RMS roughness (0.23nm).

After one hour anneal at 800℃, the images show large areas without any islands or wavy terrace edges but more atomic steps along [010] and [001] directions with a density of 0.44/μm^2, yielding doubling of the RMS roughness (0.45nm). The persistence of the atomic steps with heights of odd multiples of $a/2$ along both <010> directions and in about similar density as atomic steps with *n.a*

heights, yield terraces with TiO_2 and SrO terminations of the surface, suggesting that there is no perfect TiO_2 termination of the surface. This will prevent single-crystalline epitaxy and may cause the anti-phase domains to appear on the surface of the sample.

Chapter 6:

Characterization of over-growth of GaAs on Si/SiO_2 via a thin layer of perovskite

6.1. Introduction

Growth of III-V compound semiconductors on Si has become important in order to combine the useful properties of both materials in semiconductor technology. In this work, growth of perovskite as the intermediate layer on a Si substrate with native oxide has been investigated and described (chapter 4). Also, in chapter 5, the surface reconstruction of the perovskite before and after anneal has been studied in order to be able to come up with a suitable strategy to grow GaAs on top of the intermediate perovskite layer. The main obstacle to grow GaAs epitaxially on perovskite is the fact that the perovskite layer itself is not single crystalline and therefore there is a need to anneal and recrystallize the layer before considering GaAs over-growth. In this part of the study, different anneal temperatures have been applied to samples with 8nm $SrTiO_3$ perovskite layers before the layers were over-grown with approximately ~50nm thick GaAs layers. The layer stacks were then cross-sectioned for investigation by different methods of transmission electron microscopy.

6.2. Experimental work

The two-inch silicon wafers, with native oxide and perovskite layers on top, were cut in half and one of the halves was cut further to make samples with 11.4×11.9 mm that can be fitted in the sample holder used in the STM-MBE machine, by the scribe and break facility in the clean-room environment. After cutting, the samples were cleaned very carefully with n-butyl acetate before putting into the growth chamber to minimize contamination and have the surface as flat as possible without any dirt on it. Optical microscopy was used to check the cleanness of the sample surfaces.

Three samples, each consisting of a thin layer of perovskite grown on Si substrates via the native oxide by pulsed laser deposition, have been annealed in the MBE system at different temperatures of 675°C, 825°C and 790°C, and then the over-growth process was performed at 570°C for 5 minutes. The growth speed was roughly 10nm per minute. Therefore after settling of the growth temperature, with a As to Ga flux ratio of 1:1.6 (standard ratio of growth of GaAs) for 5mins we expect to have roughly 50 nm of GaAs grown on top. The samples then have been analysed by AFM, TEM and STEM.

Same as before, AFM images have been captured with a Veeco Nanoscope V instrument operated in tapping (non-contact) mode. Nanotec's WSxM 5.3 software [48] was used to analyse the AFM images.

To investigate the layer stack and the interface between the thin perovskite layers and over-grown GaAs by electron microscopy, cross-sectional samples were prepared by gluing two pieces of wafers face to face, gluing Si backing blocks to each side to make the stack 3mm thick, cutting the block by diamond saw, grinding and polishing the cross-sectional samples and finally ion milling them in a Fischione 1050 argon ion mill at 4kV and 2mA until electron transparency.

Same as chapter 4, a JEOL-2010F field-emission transmission electron microscope operated at 197kV, which has a scan unit and BF and ADF

detectors for STEM, is used to investigate the stack of layers. The microscope is also equipped with a GATAN imaging filter with a CCD camera for image acquisition.

Table 6.1 shows the anneal temperatures which were applied to each of the samples as well as the duration of the anneal process. (Appropriate names have been assigned to the samples to be used later in this chapter.)

Table 6.1. The anneal temperatures and times for each Si sample with perovskite layers.

	name	anneal temperature	anneal time
sample 1	STO675GaAs	675 ±25 °C	60 minutes
sample 2	STO825GaAs	825 ±25 °C	50 minutes
sample 3	STO790GaAs	790 ±25 °C	25 minutes

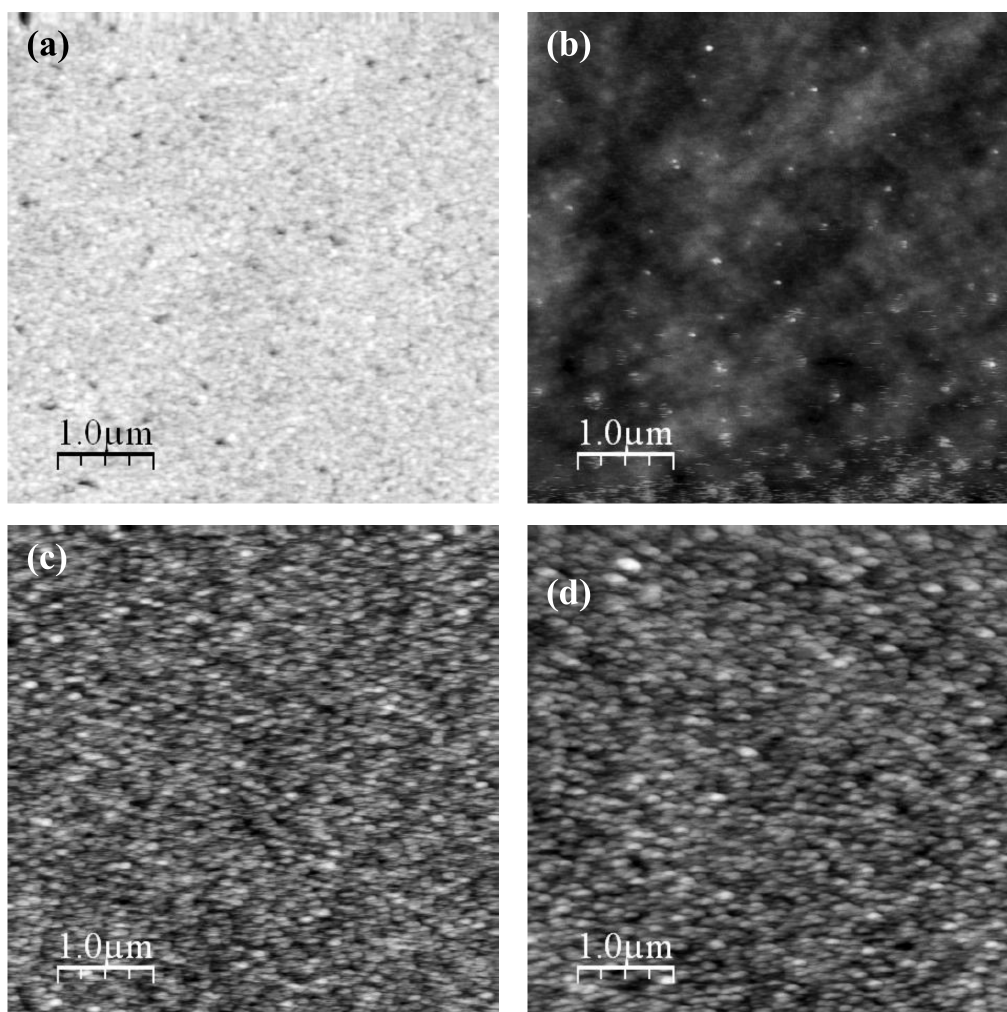
To explain the anneal times shown on the table, it should be mentioned that the target anneal time was 1 hour which was applied to the first sample (STO675GaAs), however, the RHEED pattern from the second sample (STO825GaAs) showed Kikuchi lines after 50 minutes of anneal, which suggests that the oxide layer on the sample had come off. Therefore the anneal process was stopped after just 50 minutes. The third sample (STO790GaAs) was originally annealed at a temperature of 770°C for one hour but as no reconstructions were observed during the anneal process (same as sample STO675GaAs), the anneal temperature was increased by 20°C and after just 25 minutes the Kikuchi lines appeared at this temperature.

6.3. Results and discussions of the GaAs over-growth

After the anneal and over-growth processes, when the samples brought out of the chamber, a colour change could be observed on their surfaces by naked eye (unfortunately I don’t have images from the optical microscope to show these

dark and bright islands on the surfaces). Because of this colour differences, AFM scans have been performed on both dark and bright areas of the surfaces. Figure 6.1 shows the AFM images of areas of 5×5 μm^2 for each sample from dark and bright regions,.

The acquisition time was 1s for all images which consist of 512 × 512 pixels (yielding a rather coarse sampling of 9.8nm/pixel).



(Images to be continued on the next page)

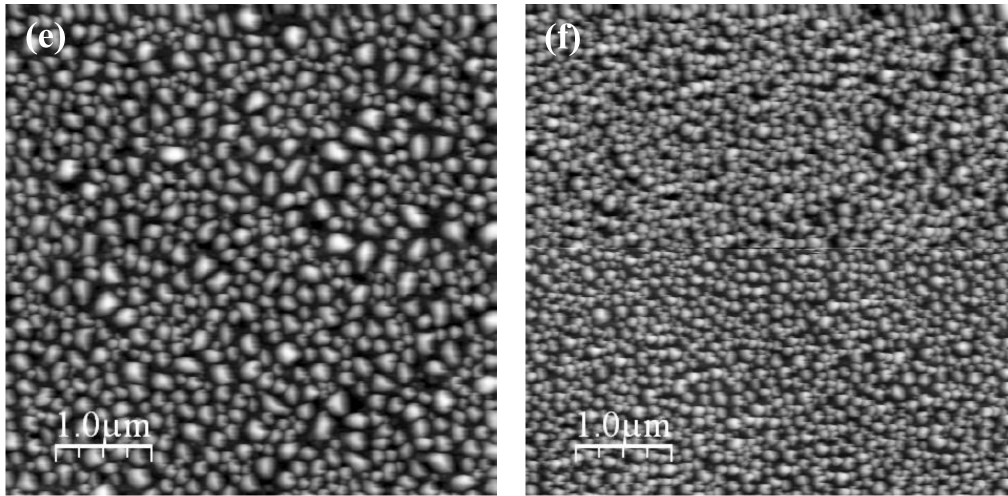


Figure 6.1. AFM images of 5μm × 5μm **(a)** central region of STO675GaAs, **(b)** one of the edges of STO675GaAs, **(c)** bright area of STO825GaAs, **(d)** dark area of STO825GaAs, **(e)** bright area of STO790GaAs and **(f)** dark area of STO790GaAs. The vertical height scale of the images is not the same due to different surface roughnesses of each sample.

Table 6.2 contains acquisition details of the AFM images such as the RMS roughnesses and peak-to-peak ranges. (The average height is automatically set to zero by the software.)

Table 6.2. RMS roughness, peak-to-peak amplitude, minimum and maximum value (all in nm) of surfaces of samples STO675GaAs, STO825GaAs and STO790GaAs.

Samples	RMS roughness (nm)	Peak-to-Peak (nm)	Minimum Value (nm)	Maximum Value (nm)
STO675GaAs Central region	2.37	40.42	-30.16	10.26
STO675GaAs Edge	0.625	8.2	-2.44	5.77
STO825GaAs Dark region	10.46	66.42	-29.91	36.51
STO825GaAs Bright region	10.80	59.59	-22.76	36.83
STO790GaAs Dark region	2.01	18.25	-7.7	10.55
STO790GaAs Bright region	2.01	16.20	-7.07	19.13

For the sample STO675GaAs, the dark areas which are the edges are the sample are unlikely to be overgrown due the sample holder clamps. The rest of the sample (central region) has high RMS roughness which indicates that the surface of the sample is not smooth, suggesting that GaAs has not been over-grown epitaxially. It is the same for the other two samples (both in dark and bright areas of the surfaces), indicating that the over-growth of epitaxial layer of

GaAs has not been successful in the other samples either. Specially sample STO825GaAs shows a RMS roughness around 5 times higher that other two samples which indicates that somewhere around 810±25°C the surface roughness of GaAs increases dramatically by annealing the underlying STO perovskite and therefore the GaAs layer has grown in a non-epitaxial manner. The minimum and maximum values of z amplitude uphold this because if the surface of GaAs layer had been grown epitaxially, the range between the minimum and maximum value of the z amplitude should have remained well below the perovskite layer thickness of 8nm. The increased maximum values of z-amplitudes represent the maximum height of islands formed and again indicate that the GaAs layers have not been grown epitaxially and are not smooth; the layers will be poly-crystalline instead. There is the possibility (at least in principle) that GaAs could be rough and single-crystalline: if there were a lot of atomic steps and islands on top of a smooth layer.

ADF and BF-STEM, EDXS and HRTEM images from the cross-sectioned stacks of Si/SiO_2/perovskite/GaAs were acquired to investigate the possibility of rough single-crystalline nucleated GaAs layer as well as if the perovskite layers still existed between silicon substrate and the GaAs layer or not.

6.3.1. Results and discussion of sample STO675GaAs

Figure 6.2 is a BF-TEM image of the over-view of the layer stack in sample STO675GaAs from a cross-sectional sample prepared as explained before. The field of view is 131nm wide and the sampling rate is 0.13nm/pixel.

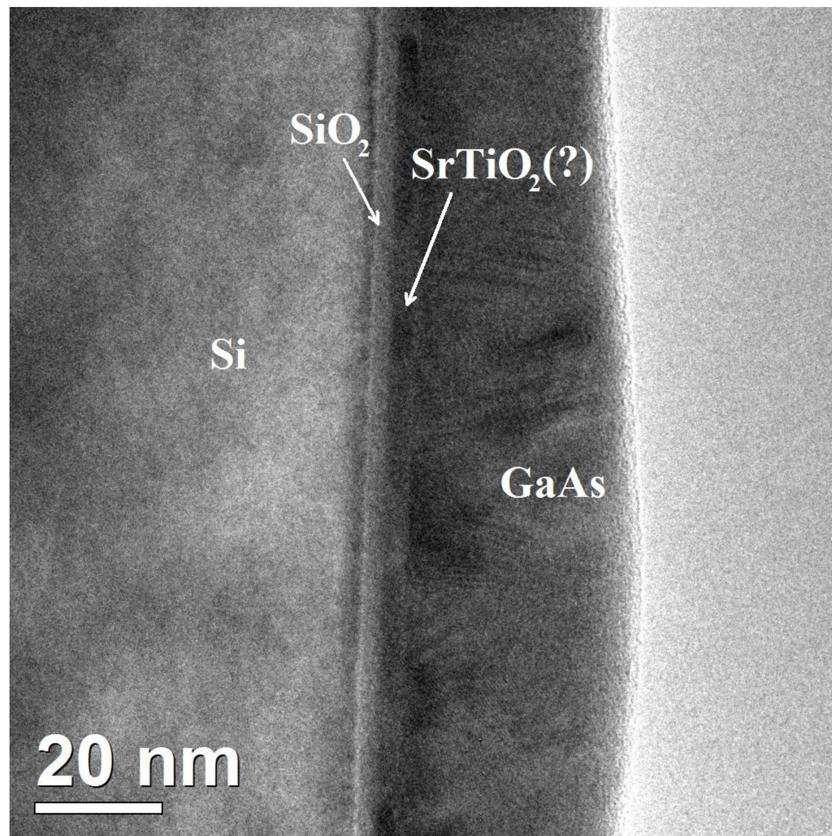


Figure 6.2. BF-TEM image of a $Si/SiO_2/SrTiO_3/GaAs$ layer stack.

Figures 6.2 indicates that there are two different layers between Si substrate and GaAs layer: directly above the silicon substrate there is a thin layer with bright contrast which appears to be amorphous, with a thickness of roughly 3nm followed by a layer with darker contrast below the GaAs layer, with fringes visible in different directions which means the layer is poly-crystalline in some areas and not smoothly grown on top of the amorphous layer. The thickness of the latter (darker) layer is 3.5nm on average. Below the bright amorphous layer, a dark contrast of Fresnel fringe due to the effect of defocus is visible. The GaAs layer is poly-crystalline and lattice fringes are visible in this layer as well. Figure 6.3 displays another BF-TEM image from the central area of the previous image at higher magnification and the power spectrum of it. The field of view is 66nm and the sampling rate is 0.064nm/pixel.

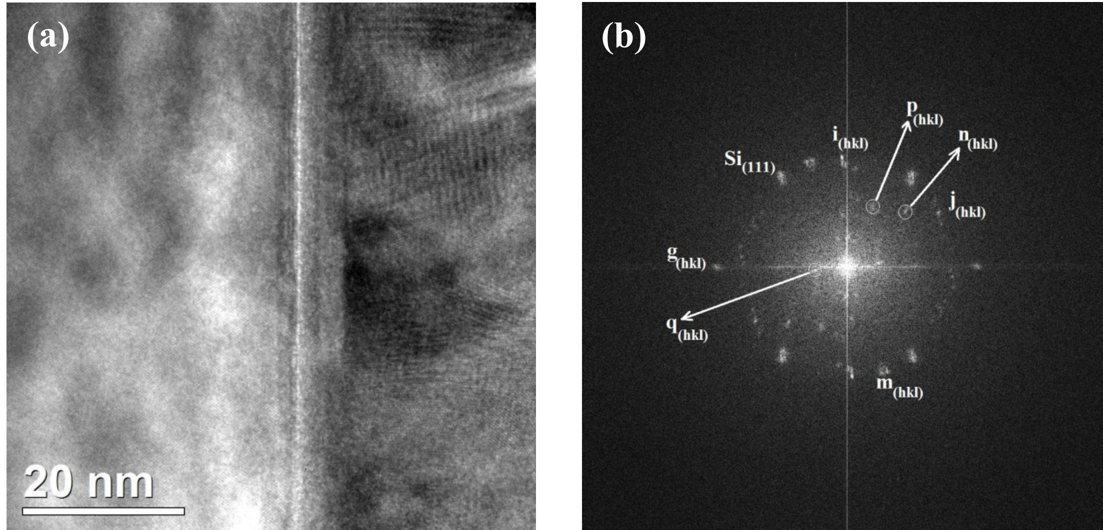


Figure 6.3. (a) BF-TEM image of the Si/oxide/GaAs layer stack and **(b)** the power spectrum of the TEM image

From figure 6.3, using the planar spacings of Si(111) as references, the planar spacings of all the bright spots can be calculated using the equation introduced in chapter 3 under the HRTEM imaging section to help identify the crystal structure of all the materials of the layer stack. Table 6.3 shows the planar spacings of the spots indexed in figure 6.3(b).

Table 6.3. Calculated planar spacings of the bright spots on the power spectrum shown in figure 6.4(b)

	g(1/nm)	planar spacing *d(Å)*
$Si_{\{111\}}$	3.23	3.14
$\boldsymbol{g_{(hkl)}} \rightarrow Si_{(002)}$	3.87	2.59
$\boldsymbol{i_{(hkl)}} \rightarrow GaAs_{\{111\}}$	3.19	3.14
$\boldsymbol{j_{(hkl)}} \rightarrow GaAs_{\{111\}}$	3.16	3.17
$\boldsymbol{m_{(hkl)}} \rightarrow GaAs_{\{111\}}$	3.26	3.07
$\boldsymbol{n_{(hkl)}}$	2.42	4.14
$\boldsymbol{p_{(hkl)}}$	1.98	5.12
$\boldsymbol{q_{(hkl)}}$	0.92	11.02

From table above, it can be deduced that *g*, *i*, *j* and *m* represent Si(002) and GaAs{111}. The planar spacing of *n* is near to that of $SrTiO_3${001}. The planar spacings of *p* and *q* were compared to as many as $SrTiO_3$, SrO and TiO_2 structures as I could find in the literature but were not matching any of them.

EDX analysis has been done on the layer stack to confirm the presence of Ti and Sr in the unknown layer between Si and GaAs. Figure 6.4 is the EDX spectrum from the centre of the layer. The $O_{K\alpha}$ peak overlaps with the Ti_L peak.

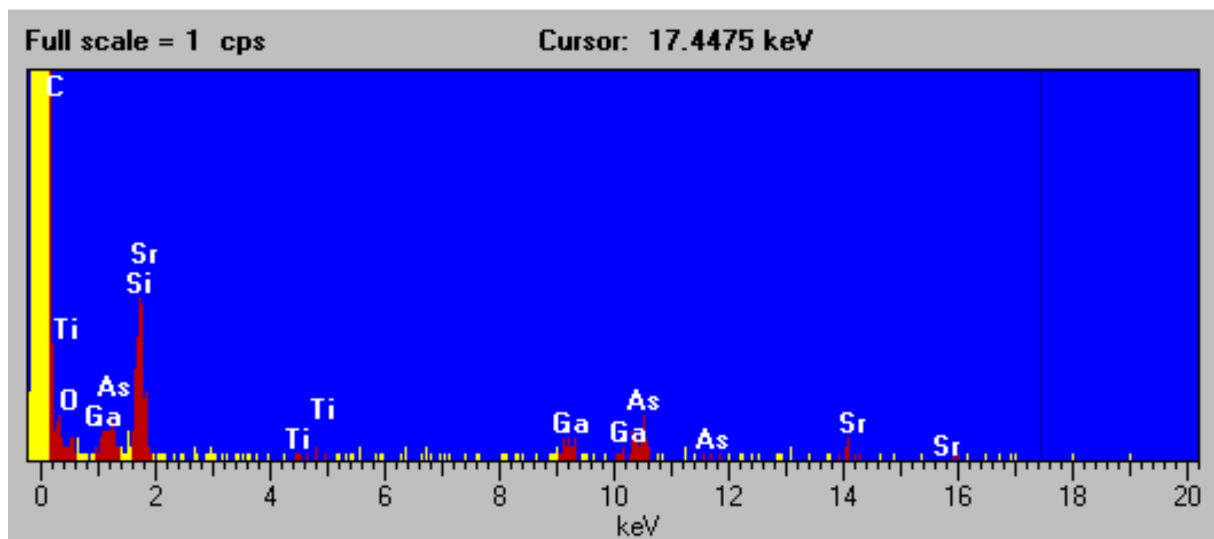


Figure 6.4. The X-ray spectrum from the centre of the layer stack

Figure 6.5(a) shows BF-STEM image and figures 6.5(b-f) show the elemental maps of different X-ray lines. The sampling rate of the maps is 1.15nm/pixels. The number of counts is very low and therefore *k*-factor correction is not needed for quantification of the X-ray maps. The presence of Sr and Ti is proven from the EDX maps and the BF-STEM image shows that the layer is continuous.

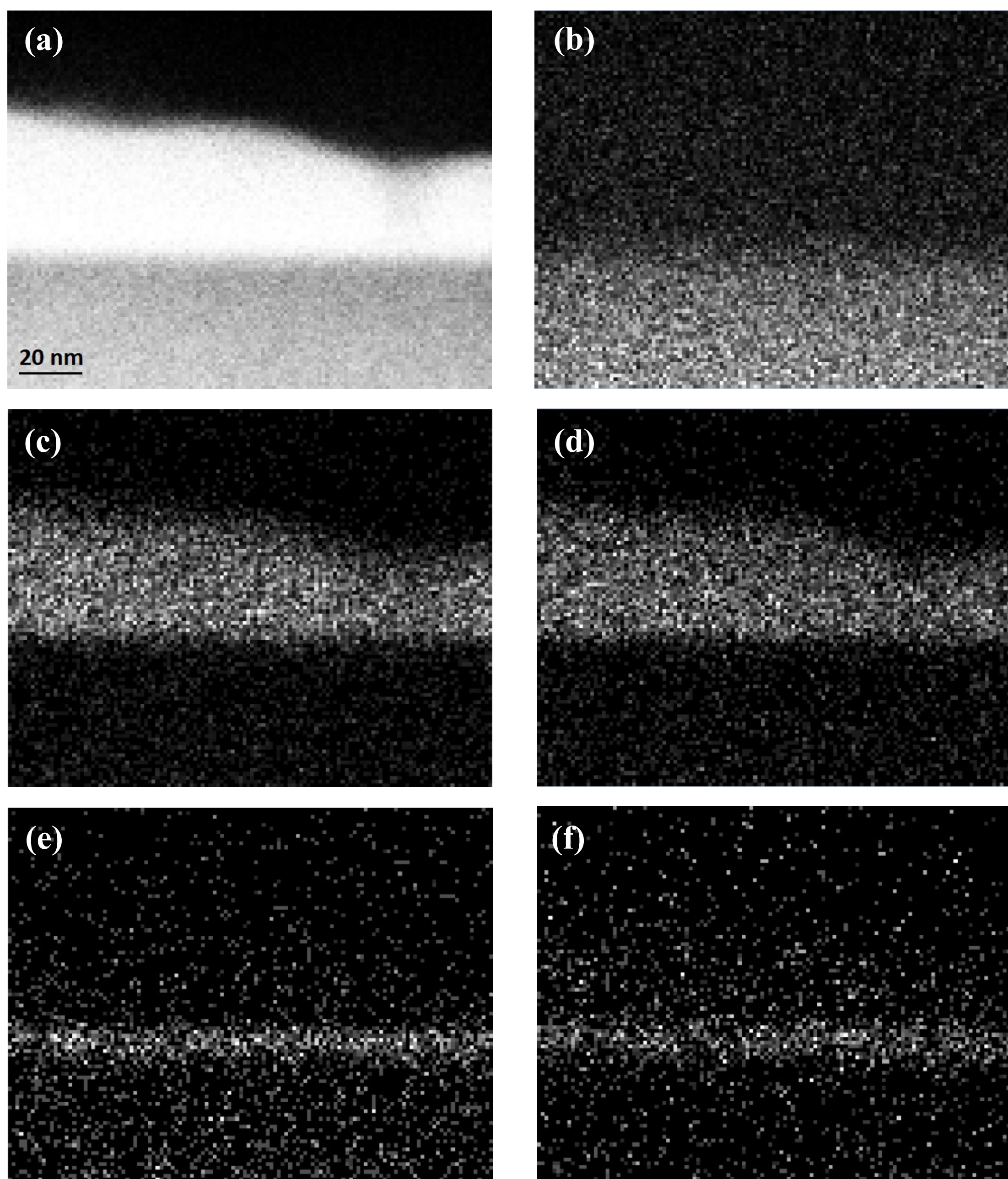


Figure 6.5. (a) BF-STEM image of the map of stack of layers and X-ray intensity maps of **(b)** $Si_{K\alpha}$ (maximum count of 32), **(c)** $Ga_{sum\ of\ K\alpha,\ K\beta,\ L\alpha}$ (maximum count of 38), **(d)** $As_{sum\ of\ K\alpha,\ K\beta,\ L\alpha}$ (maximum count of 30), **(e)** $Sr_{sum\ of\ K\alpha,\ L\alpha}$ (maximum count of 22) and **(f)** $Ti_{sum\ of\ K\alpha,\ K\beta,\ L\alpha}$ (maximum count of 19). The beam current is between 1 and 2nA and the probe size is 1-1.5nm.

Figure 6.6 (a) shows the intensity profile of X-ray counts for Si, Ga and As and figure 6.6 (b) shows those for Sr and Ti.

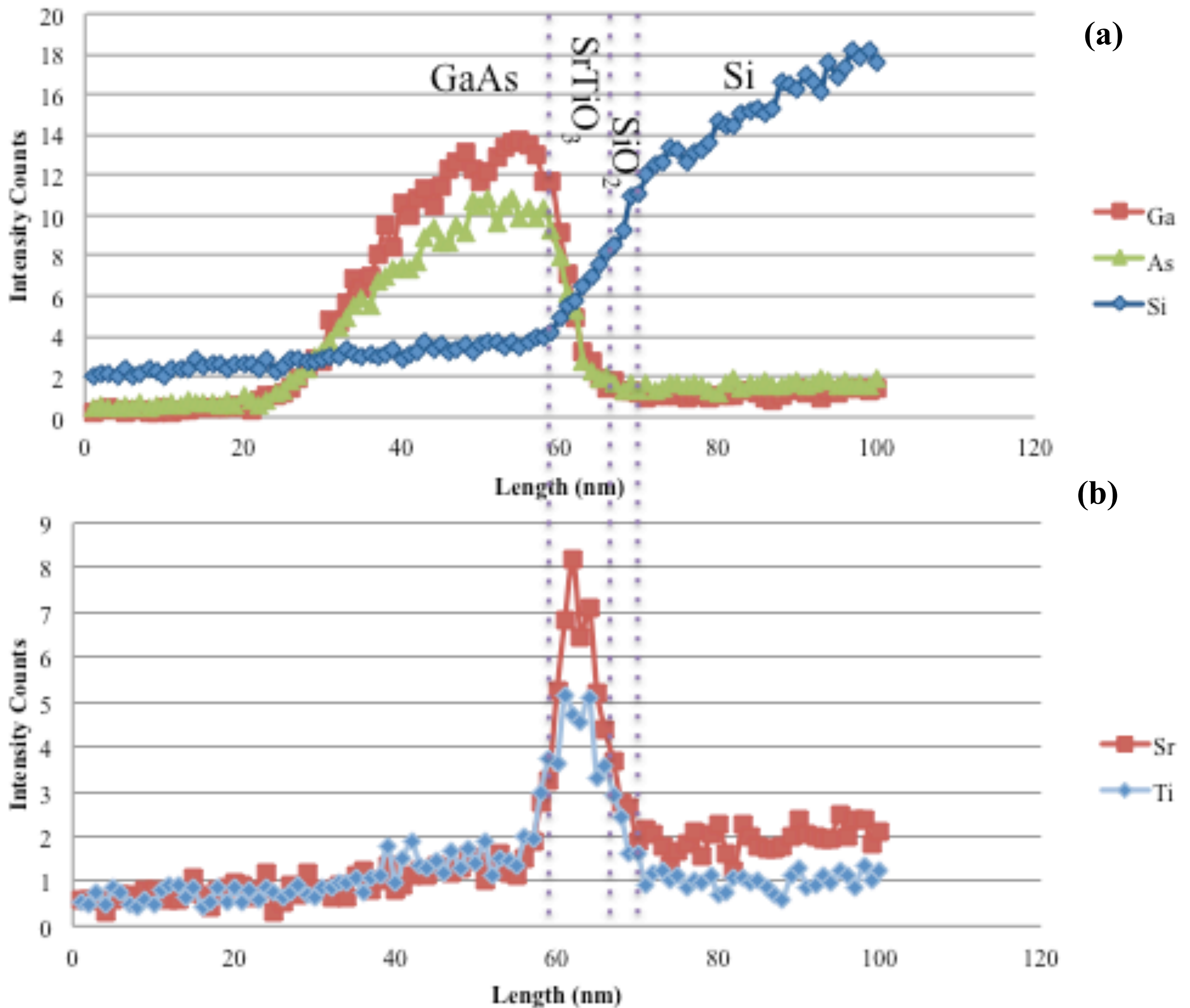


Figure 6.6. The intensity profiles of **(a)** Si, Ga and As and **(b)** Sr and Ti.

By adding the intensities from Si, Ga and As maps in figure 6.7, we can see that there is a gap of ~7 pixels or 8nm (Figure 6.7(a)). This gap consists of two layers according to the HRTEM image, one is the native oxide and the other is the perovskite. By adding the intensities of Sr and Ti maps we can see that the sum-map of Sr and Ti shown in figure 6.7(b) correlates with the gap between Si, Ga and As intensity maps in figure 6.7(a). This agrees with the presence of perovskite between Si/SiO_2 and GaAs layer. The profile of the X-ray sum map of Sr and Ti shows a FWHM of 5-6 pixels (5.8-6.9nm) which almost equals to

the thickness measured before the anneal process (Chapter 4, table 4.3: 5.59-5.92nm).

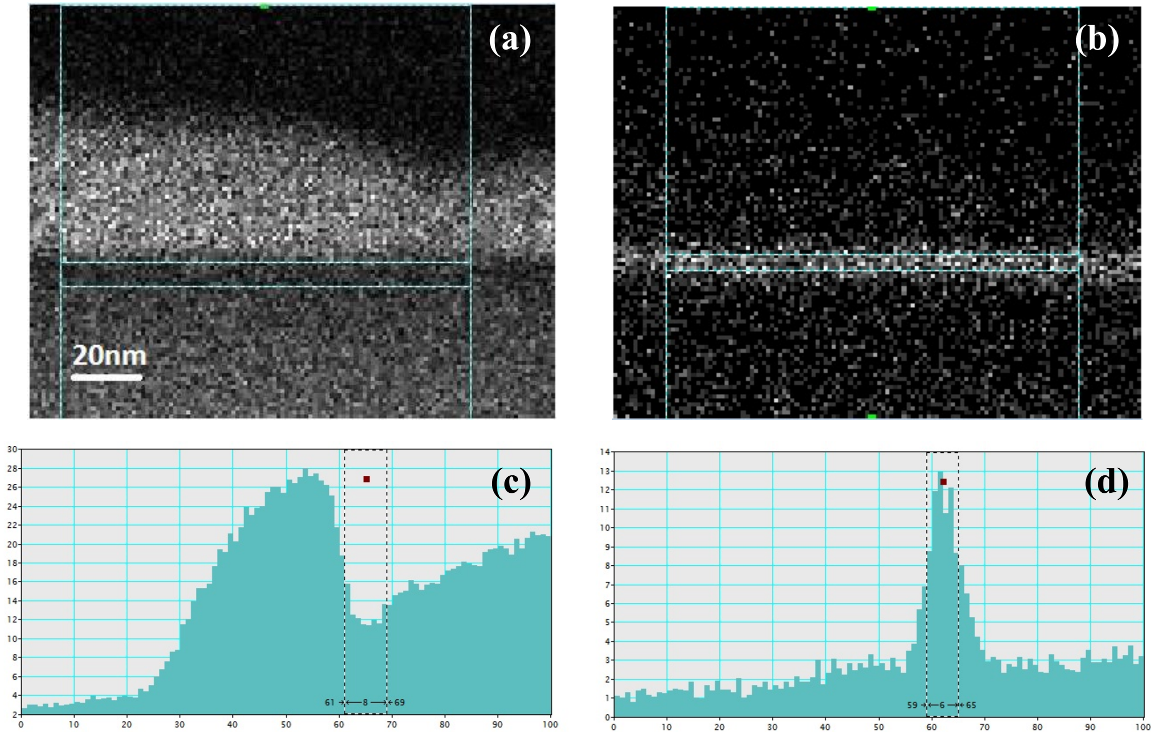


Figure 6.7. (a) the X-ray sum-map of Si, Ga and As shows a gap of ~7-8 pixels in the profile image **(c)**. **(b)** the X-ray sum-map of Sr and Ti shows a full width at half maximum (FWHM) of ~5-6 pixels in the profile image **(d)**.

It can be deduced from these results that the native oxide has a thickness of ~2.3-3.5nm (2-3 pixels).

The RMS surface roughness of the GaAs layer grown on top can be calculated using the same method used in chapter 3 for analysing the perovskite layer.

Below in figure 6.8, an ADF-STEM image of the layer acquired with an electron beam size of 0.3 nm and dwell time of 19.5μs is shown. The beam convergence semi-angle is equal to 9.5mrad; the collection angles are 55-170mrad. The fluctuation of contrast along the layer indicates that the GaAs layer is not epitaxial but poly-crystalline. The field of view is 1016nm wide for the 2048 × 2048 pixels image, at a sampling rate of 0.5nm/pixel.

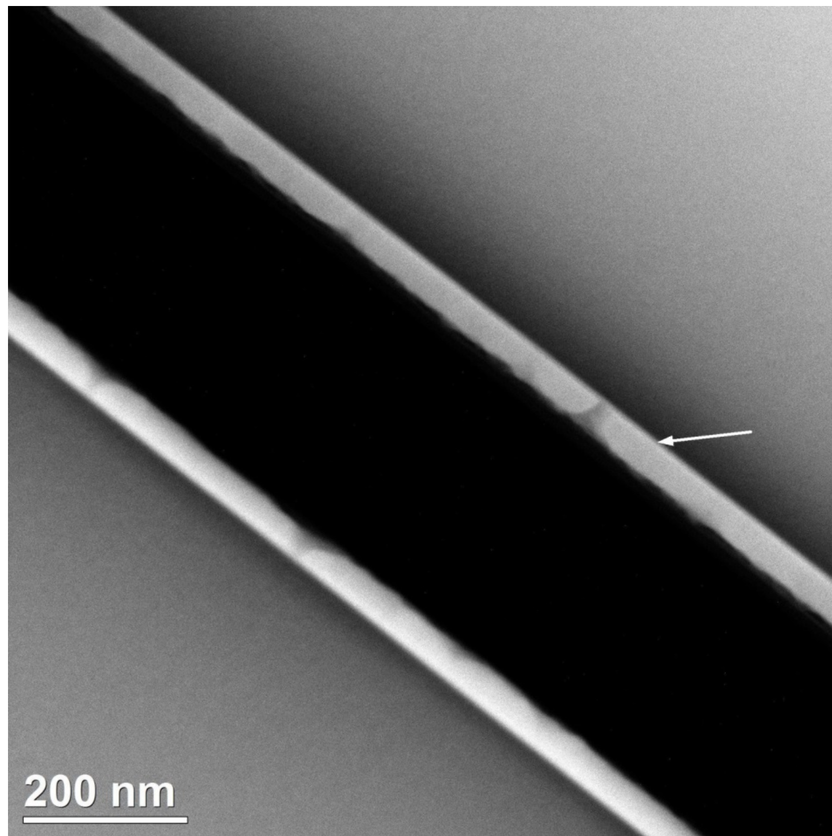


Figure 6.8. ADF-STEM of a cross-sectional sample of 2 glued sections of nominally 8nm $SrTiO_3$ and 50nm GaAs layer after anneal in 675°C for an hour. The GaAs layer appears bright in the image, the perovskite layer is faintly visible only in the upper sample, due to slight orientation effects and it is marked by an arrow.

The projected RMS surface roughness of the GaAs layer in ADF-STEM image is 3.33nm, which is close to the RMS surface roughness of 2.37nm measured from the AFM image of the sample (mentioned in table 6.2), and its average thickness is 43nm.

6.3.2. Results and discussion of sample STO825GaAs

A BF-TEM image of the layer stack of sample STO825GaAs is shown in figure 6.10. It can be observed that the GaAs grown on top is poly-crystalline. A dark contrast of Fresnel fringes is visible at the Si/SiO_2 interface.

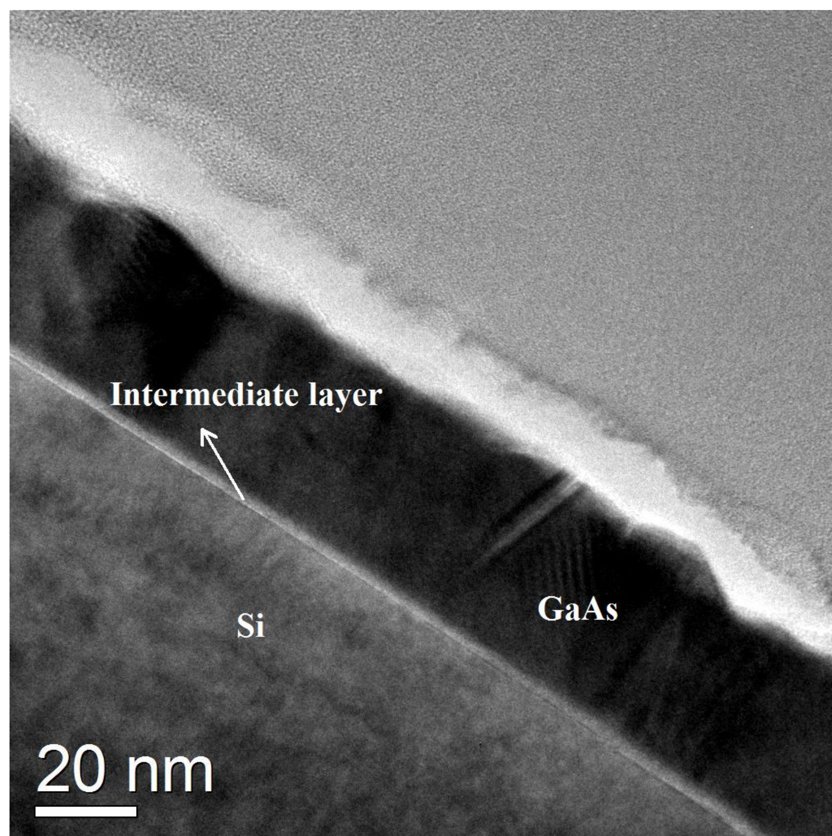


Figure 6.10. BF-TEM image of the Si/bright intermediate layer (perovskite?)/GaAs stack of the sample with anneal temperature of 825°C.

Figure 6.11 shows the same region in higher resolution and its power spectrum. It can be observed that there is just one amorphous layer between Si and GaAs which indicates that the perovskite layer has been almost completely evaporated during the anneal.

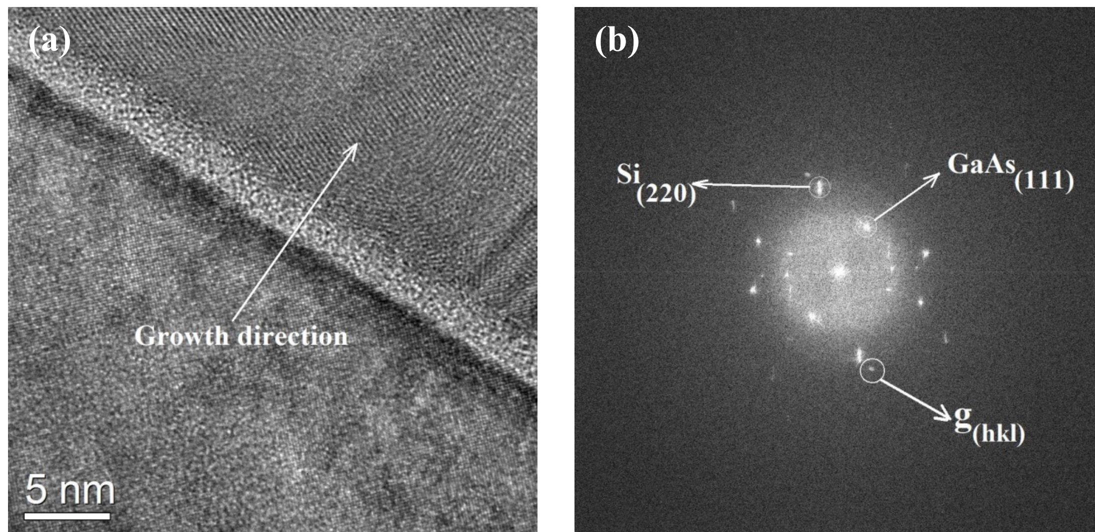


Figure 6.11. (a) Lattice image of the GaAs island on Si substrate and **(b)** the power spectrum of the image.

A Fourier analysis of the lattice image yields the planar spacings of the bright spots in the image (figure 6.11.b). The unknown spots indexed as $\mathbf{g}_{(hkl)}$ have a planar spacing close to tetragonal TiO_2 (rutile) with $d_{(220)}$ (1.62Å) [73]. It suggests that the intermediate layer contains amorphous SiO_2 and poly-crystalline rutile (TiO_2) rather than $SrTiO_3$.

Figure 6.12 shows the X-ray intensity scans of the sample along the growth direction. It confirms the presence of Ti and perhaps Sr in the intermediate layer. But the intensities of these two elements are very low compared to what they were in sample STO675GaAs with $SrTiO_3$ intermediate layer. The Sr signal is close to noise level and no real layer is detected. It also can be seen from the line-scan that the thickness of the amorphous layer is roughly 2nm (1 pixel).

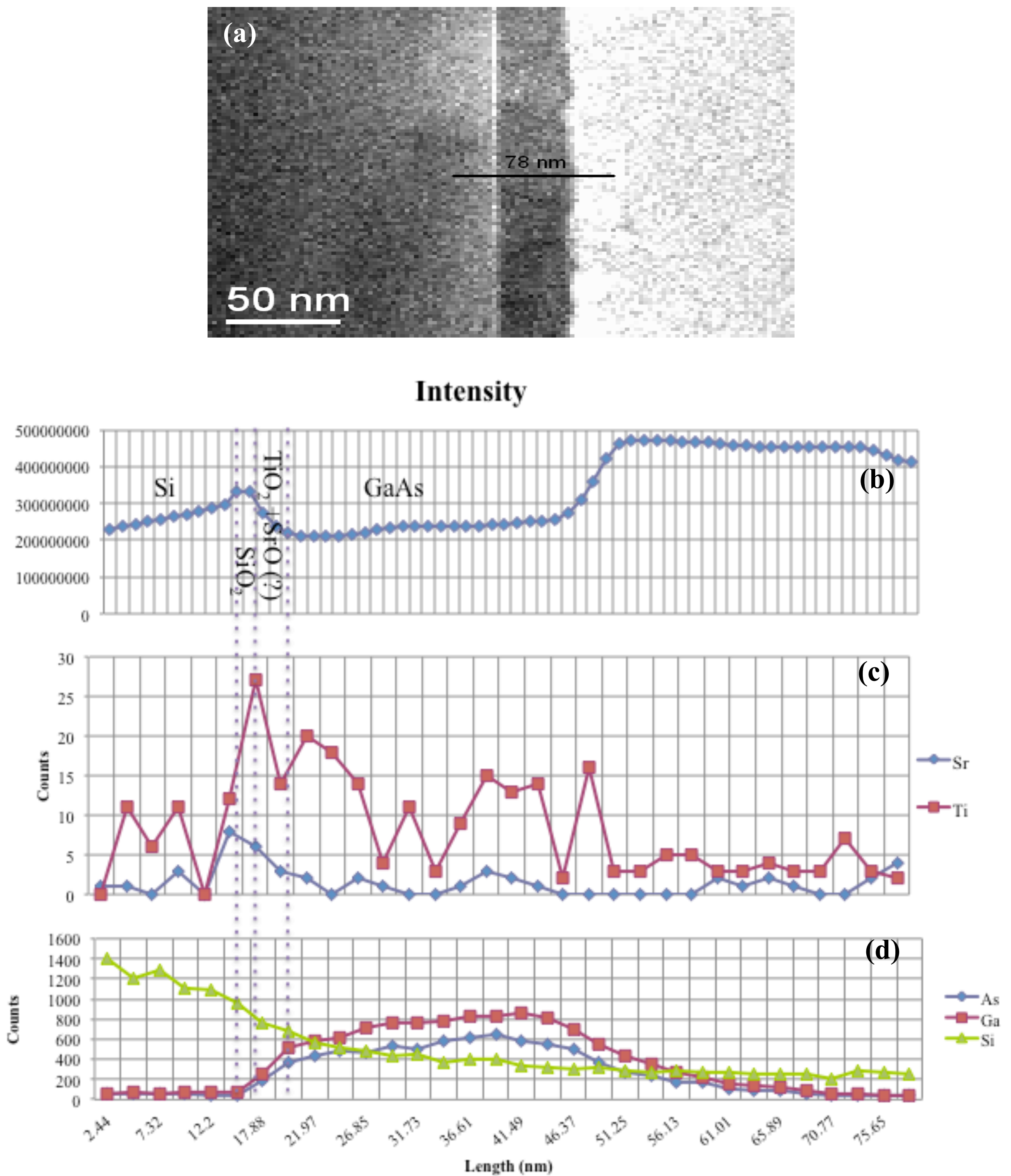


Figure 6.12. (a) BF-STEM image of the stack of layers in sample STO825GaAs. The beam current is between 1 and 2 nA and the probe size is 1-1.5 nm. **(b)** Intensity line-scan of (a) **(c-d)** X-ray line-scans of elements detected by scanning a focused probe across the layer stack.

Figure 6.13 shows an ADF-STEM image acquired with electron beam size of 0.3 nm, dwell time of 19.5µs, the beam convergence semi-angle of 9.5 mrad and collection angle of 55-170mrad. The field of view is 616nm wide for the 2048 × 2048 pixels image, at a sampling rate of 0.3nm/pixel. The fluctuation of contrast along the layer is again due to the GaAs layer being not single-crystalline but poly-crystalline.

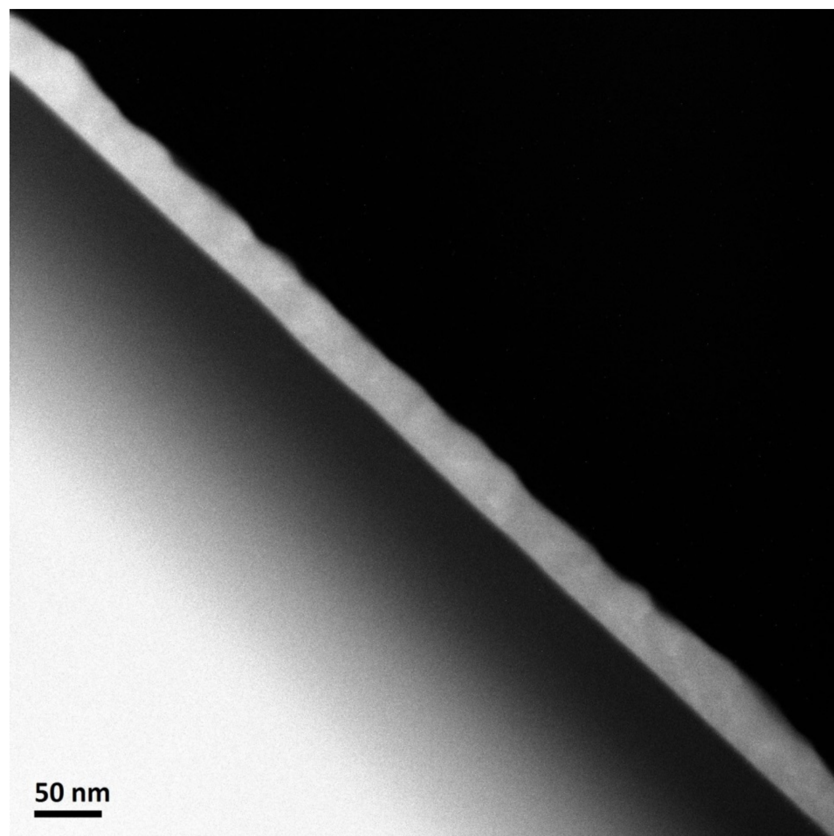


Figure 6.13. ADF-STEM image of the stack of layers of Si and GaAs (nominally ~50nm). The bright layer in the image is GaAs. There is no visible intermediate layer between Si and GaAs any more.

The RMS projected interface roughness calculated using the image shown in figure 6.13 is 13.95nm, which is slightly higher than the surface roughness of 10.8nm, measured using AFM. The average thickness of the GaAs layer is 35.56 nm.

6.3.3. Results and discussion of sample STO790GaAs

The third and last sample has been annealed at 770°C for one hour and because no surface reconstruction was observed in RHEED during this time, the temperature was then increased to 790°C. After 25 minutes Kikuchi lines appeared, therefore the anneal process was stopped and the sample over-grown with GaAs with the same recipe as mentioned before.

Figure 6.14 shows an HRTEM lattice image of the layer stack. The GaAs layer with lattice and moiré fringes can be observed on top of the Si substrate, as well as two intermediate layers (which can be observed with different contrasts on top of Si). The first (bright) layer on Si is amorphous and most likely SiO_2 and the second layer which is crystalline in some areas is probably the perovskite layer.

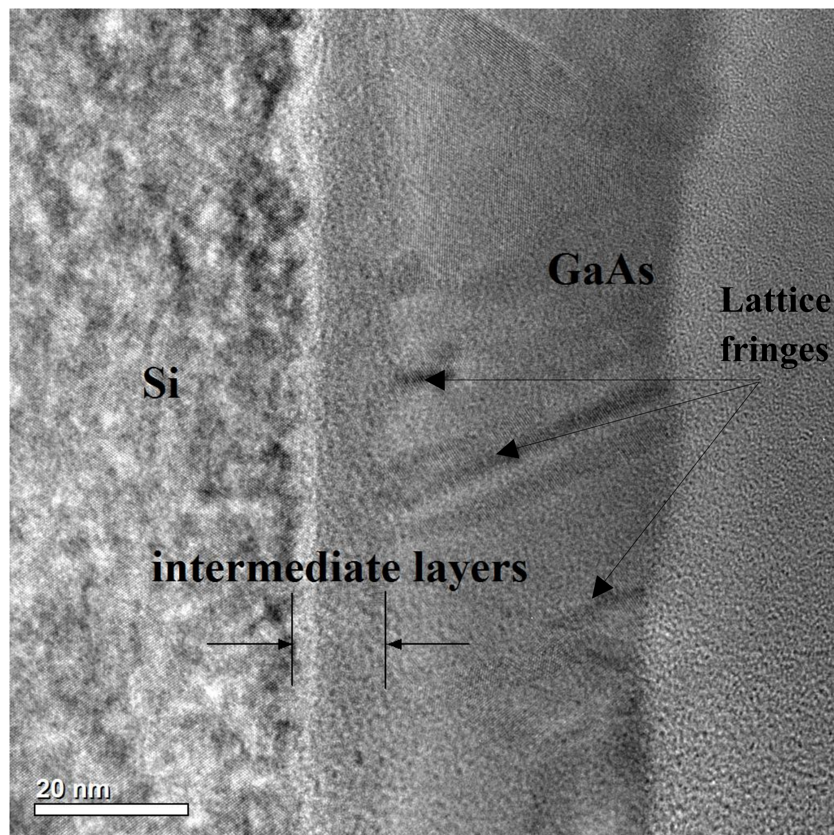


Figure 6.14. HRTEM image of the cross-sectional sample with anneal temperature of 790°C

The GaAs layer grown after the anneal process is polycrystalline and the interface between it and the buffer layer underneath is rough. Figure 6.15 shows another area of the layer stack of Si/buffer layer/GaAs in a thinner part of the sample and its power spectrum. The buffer layer is partially crystalline and the roughnesses of the interfaces between Si and oxide as well as oxide and GaAs are more obvious in figure 6.15(a).

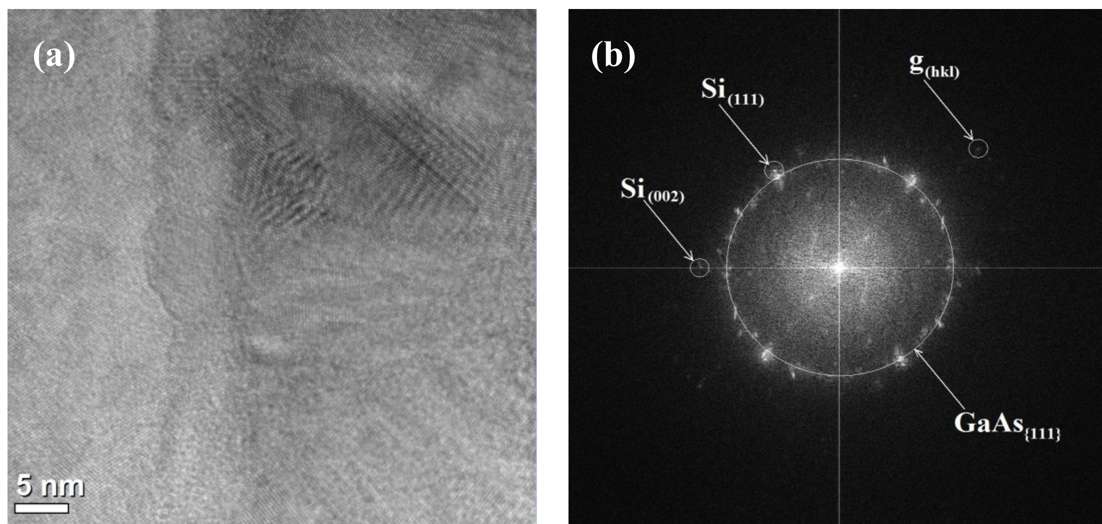


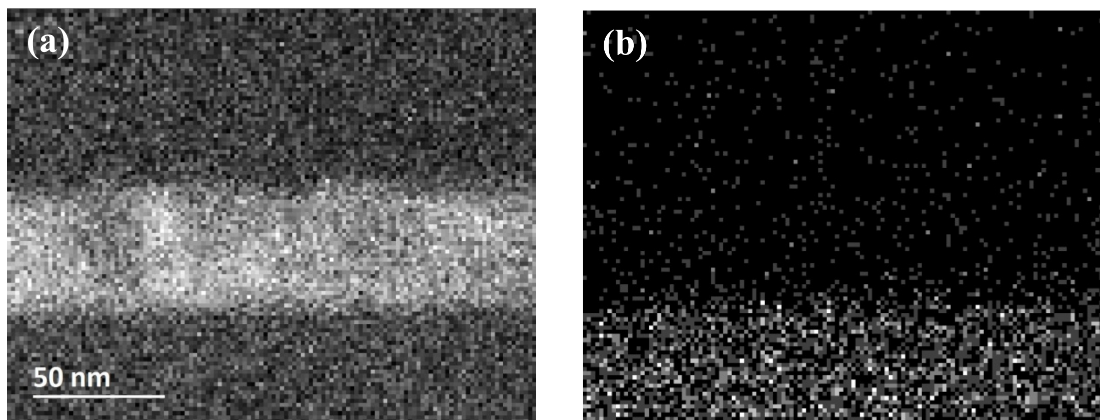
Figure 6.15. (a) HRTEM image of stack of Si/Oxide/GaAs layers and **(b)** the power spectrum of the TEM image

Planar spacing calculation has been done using Si(111), Si(002) and GaAs(111) as references in figure 6.15(b). Table 6.4 contains the planar spacing of reference points and unknown spots in the power spectrum in figure 6.14(b). The unknown spot indexed as $\boldsymbol{g}_{(hkl)}$ has a value close the one of $SrTiO_3$ {200}.

Table 6.4. Calculated planar spacings of the bright spots in the power spectrum shown in figure 6.15(b)

	$g(1/nm)$	Planar spacing $d(\AA)$
$Si_{(111)}$	3.39	3.1
$GaAs_{\{111\}}$	3.26	3.2
$Si_{(002)}$	3.99	2.7
$\mathbf{g}_{(hkl)}$	5.3	1.98

X-ray mapping of the sample has been done to confirm the presence of Sr and Ti elements in the intermediate layer. Figure 6.16(a) shows a BF-STEM image and figures 6.16(b-f) show the elemental maps of different X-ray lines. The sampling rate of the maps is 0.78nm/pixels.



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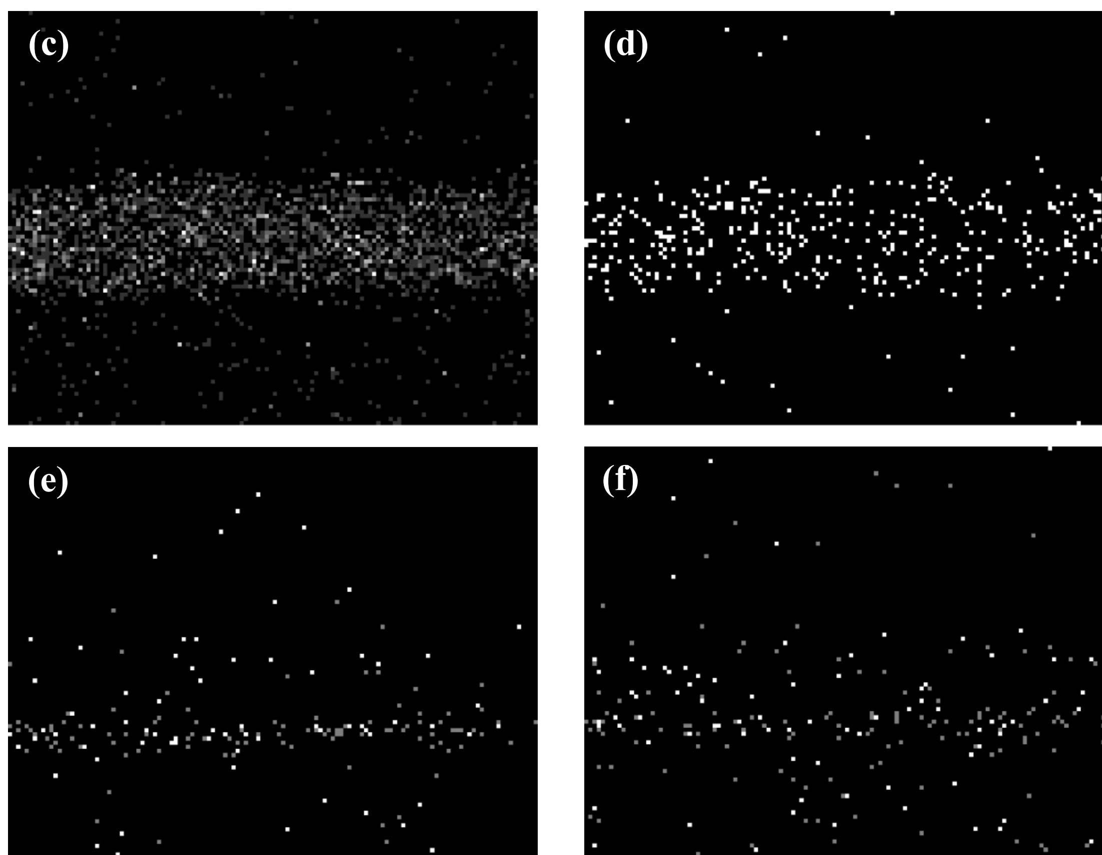

Figure 6.16. (a) X-ray intensity map of a BF-STEM image of stack of layers and X-ray intensity maps of **(b)** $Si_{K\alpha}$ (maximum count of 25), **(c)** $Ga_{\text{sum of } K\alpha, K\beta, L\alpha}$ (maximum count of 26), **(d)** $As_{\text{sum of } K\alpha, K\beta, L\alpha}$ (maximum count of 30), **(e)** $Sr_{\text{sum of } K\alpha, L\alpha}$ (maximum count of 10) and **(f)** $Ti_{\text{sum of } K\alpha, K\beta, L\alpha}$ (maximum count of 12). The beam current is between 1 and 2 nA and the probe size is 1-1.5 nm.

Figure 6.17 shows projections of the X-ray maps for Si, Ga, As, Sr and Ti.

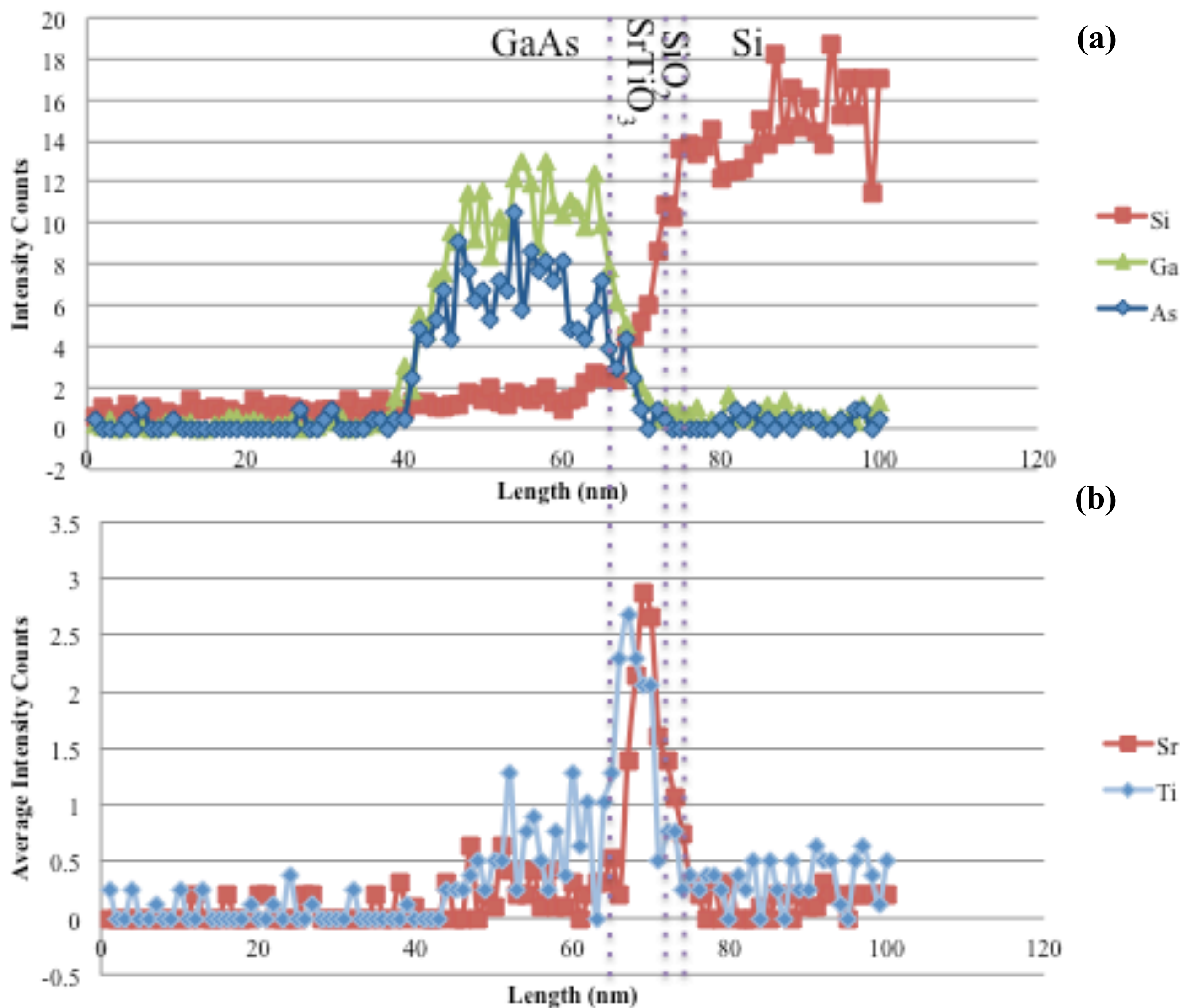

Figure 6.17. Profiles of the X-ray intensity maps of **(a)** Si, Ga and As and **(b)** Sr and Ti in figure 6.16.

Again the Sr and Ti X-ray counts peaks in the gap between Si and GaAs X-ray intensity maps confirms the presence of these elements in the intermediate layer. The layer consistency can be checked by adding the Si, Ga and As signals together and Sr and Ti signals together and compare them. The sum-map of Si, Ga and As shows a gap of ~5 pixels or 7.65nm between the Si substrate and the GaAs layer. This gap consists of two layers according to the HRTEM image, one being the native oxide and the other the perovskite. By adding the Sr and Ti maps we can see that the new sum-map correlates with the gap between Si, Ga

and As intensity maps. This agrees with the presence of perovskite between Si/SiO_2 and GaAs layer. The profile of the X-ray sum map of Sr and Ti shows a FWHM of 3-4 pixels (5.36nm).

Similar to sample STO675GaAs, the surface roughness of the GaAs layer grown on top has been calculated from the ADM image.

Figure 6.18 shows an ADF-STEM image of the layer stack acquired with electron beam size of 0.3 nm and dwell time of 19.5µs. The beam convergence semi-angle is 9.5 mrad; the collection angle 55-170mrad. The inhomogeneity of contrast along the layer suggests that the GaAs layer is poly-crystalline. The field of view is 616nm for the 2048 × 2048 pixels image, at a sampling rate of 0.3nm/pixel.

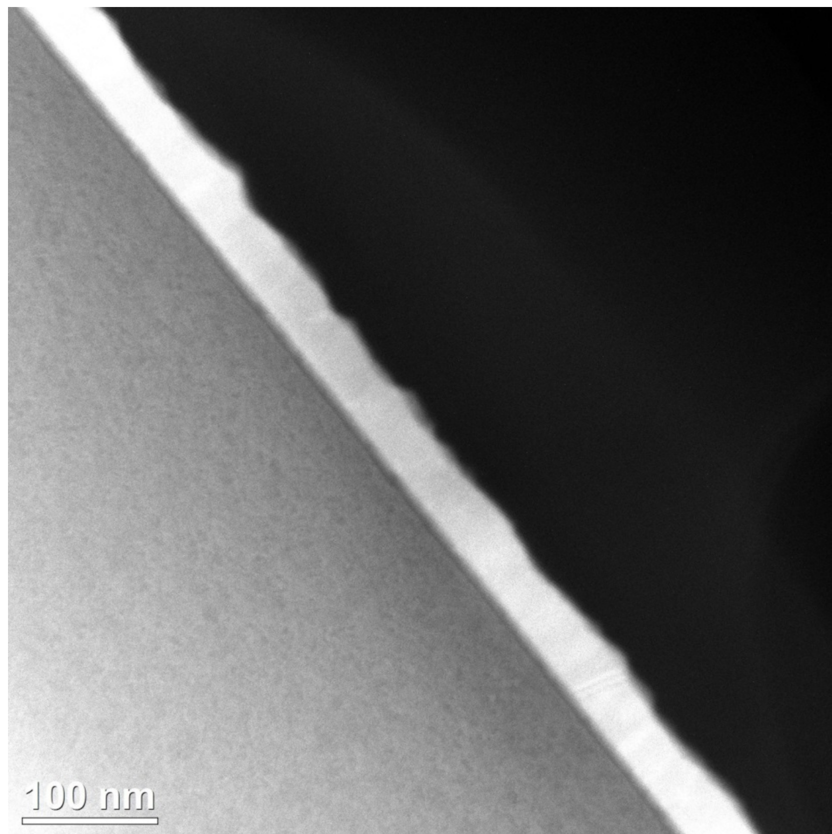

Figure 6.18. ADF-STEM image of the stack of layers of Si, native oxide, $SrTiO_3$ (nominally 8nm) and GaAs (~50nm). The bright layer in the image is GaAs, the perovskite layer is visible faintly underneath the GaAs layer.

The RMS surface roughness for GaAs layer calculated using the MATLAB code is 3.86 nm higher than the roughness measured by AFM (~2nm). The average thickness of the GaAs layer is 42 nm.

6.4. Conclusion

In this chapter, the experimental results of growth of GaAs on silicon/SiO_2 via thin layers of $SrTiO_3$ have been shown. Three samples have been annealed at different temperatures (675, 790 and 825 °C) for a maximum of 1 hour to see any reconstruction on the surface of perovskite layer before over-growing with roughly 50 nm GaAs layer at 570 °C. But no reconstruction was observed, in two later samples the Kikuchi line

The sample with 675℃ anneal temperature (STO675GaAs) didn't show any change of the RHEED pattern after one hour. The HRTEM and STEM results on the over-grown sample showed that the perovskite layer was still poly-crystalline and therefore the GaAs layer didn't grow epitaxial. The presence of Sr and Ti has been confirmed using EDXS analysis and also the planar spacing of the bright spots in the power spectrum image.

The sample with 825°C anneal temperature (STO825GaAs) showed reconstruction on the surface after 50 min of anneal in the MBE chamber. The HRTEM image showed that there was just one intermediate layer between GaAs and Si and this layer was amorphous. Calculation of planar spacing of the power spectrum of the TEM image and EDXS analysis suggested that the perovskite layer is evaporated and rutile TiO_2 was observed along with the native oxide. The interface roughness had increased to ~10nm at this anneal temperature as well.

The third sample (STO790GaAs) was annealed at 770°C for one hour and didn't show any reconstruction but when the anneal temperature was increased to 790℃, after 25 minutes the RHEED patterns showed Kikuchi patterns of Si. TEM and STEM confirmed the presence of a poly-crystalline intermediate layer

as well as the amorphous native oxide layer between silicon and GaAs. EDXS analysis showed that Sr and Ti were present in this layer and the power spectrum image suggested the presence of $SrTiO_3$ in the intermediate layer, however, GaAs layer was not grown epitaxially due to the poly-crystallinity and ~2nm interface roughness of the perovskite layer underneath.

Chapter 7:

Conclusion and outlook

In summary, in the second chapter I reviewed the previous studies on growth of III-V compound materials on silicon. Different ways of overgrowth GaAs and other III-V materials on silicon substrates have been introduced. Other studies of growth of perovskite on Si or III-V materials have been discussed as well before growing III-V semiconductors on Si via thin layer of perovskite materials as the main focus of this project has been studied in more detail.

The third chapter is focused on introducing all the experimental techniques which were used in this study. These experimental techniques are: TEM, different imaging and quantitative techniques in TEM such as STEM, HRTEM, EDXS, etc.), AFM and ellipsometry.

In the fourth chapter I showed that the perovskite layers on the samples received from the Technische Universität Darmstadt, had not been grown epitaxially on Si. BF and ADF-STEM showed the as-received layers were poly-crystalline and needed annealing to become single-crystalline before over-growth of GaAs. I compared the thickness of the perovskite layers measured using ellipsometry and STEM imaging. Figure 7.1 compares the measured thickness of the thin perovskite layers in different samples using ADF-STEM and BF-STEM imaging as well as ellipsometry.

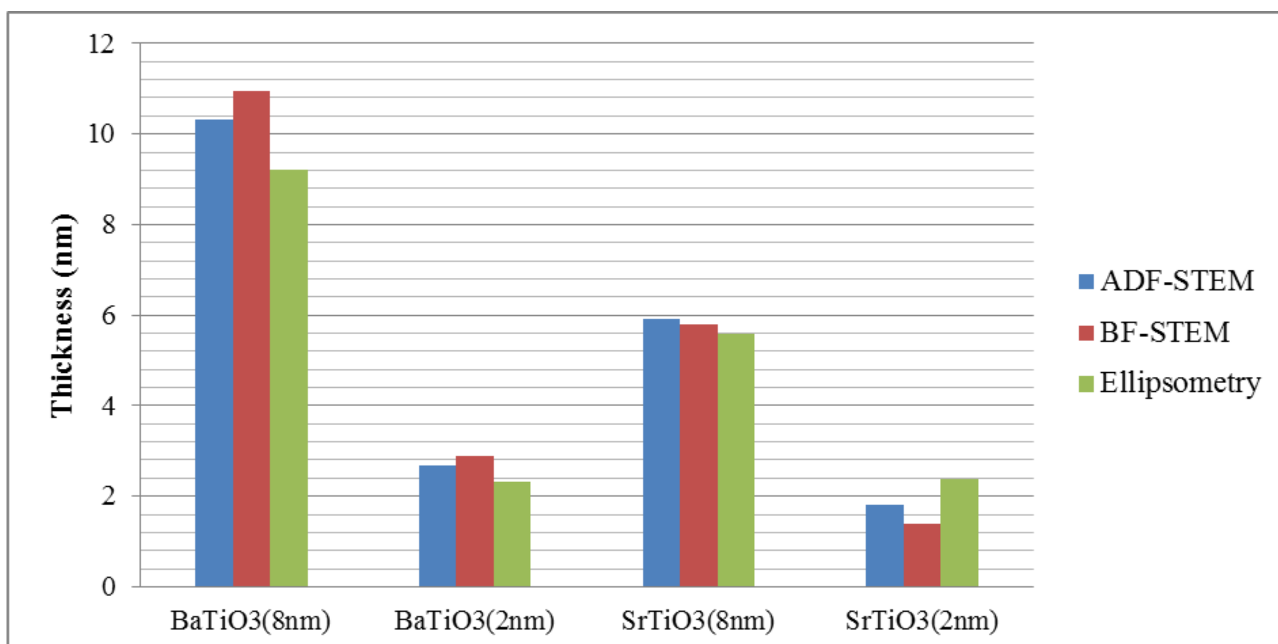

Figure 7.1. Measured perovskite thicknesses of as-received samples using ADF-STEM, BF-STEM images and ellipsometry.

All measured thicknesses agreed with each other with an error of ~15%. I also measured the surface roughness of the silicon wafer over-grown by thin perovskite layers using AFM and calculated the perovskite interface roughness using STEM images in both ADF and BF mode. The method for interface roughness calculation was to binarize the STEM image until the border between the black area and white area showed the perovskite layer. Then using a self-written MATLAB code, I measured in each column where the transition between from black to white happened and using the x and y values of that pixel I extracted from each column and row I performed a linear least-square fit and calculated the standard deviation which represents the RMS roughness of the perovskite surface viewed in projection. Figure 7.2 shows the results of the roughness measurements using AFM, ADF-STEM and BF-STEM and compares them. The relatively high RMS roughness confirmed that the perovskite layers were poly-crystalline.

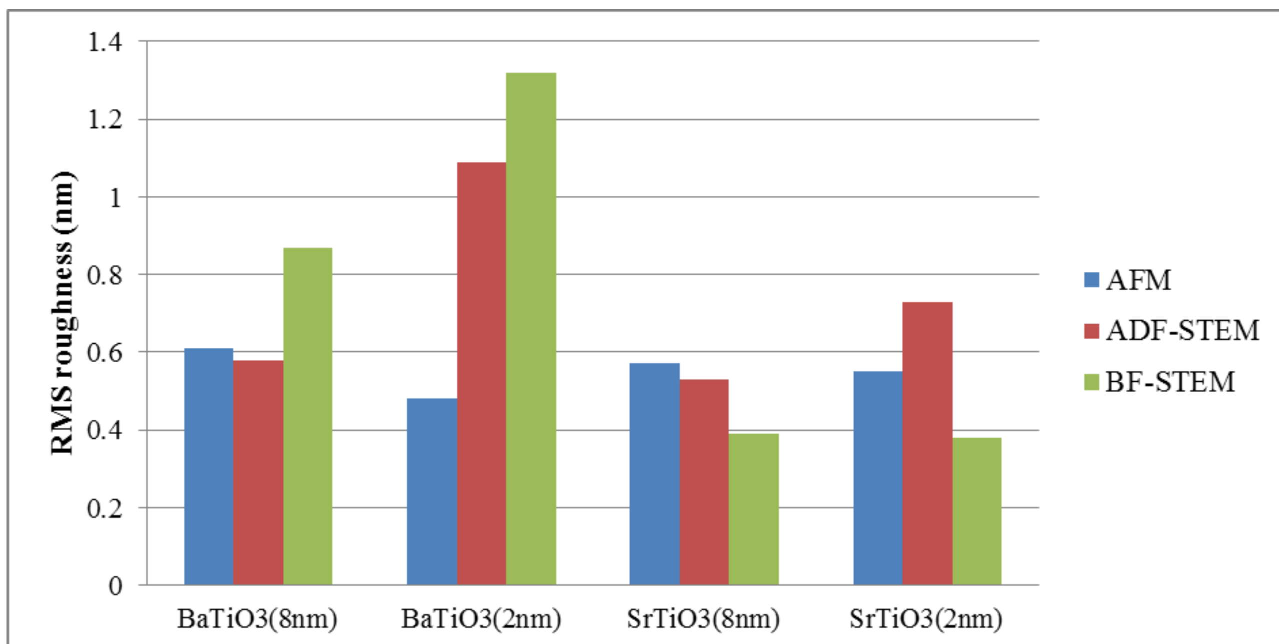

Figure 7.2. Comparing the surface (AFM) and projected interface (STEM) roughnesses of the four as-grown samples with thin perovskite layers measured by AFM and calculated using ADF-STEM and BF-STEM images.

In the fifth chapter I provided a review on re-crystallisation of Si and perovskite materials and surface reconstruction of them. The RHEED patterns of the surface of a pure $SrTiO_3$ in different temperatures was observed to determine the surface reconstructions of it as well as to find the best annealing strategy for the original Si wafers with thin perovskite layers before the over-growth of GaAs.

In the sixth chapter I have shown the experimental results of anneal and GaAs over-growth processes for three silicon samples with the nominally 8nm $SrTiO_3$ layer on top, for three different anneal temperatures. Anneal and over-growth processes have been performed in a MBE system in UHV. The results showed no re-crystallisation of the perovskite layer and therefore the GaAs layer was grown poly-crystalline on top as well. Both STEM imaging and AFM analysis confirmed it. The presence of the elements Sr and Ti in perovskite has been confirmed using EDX analysis and the power spectrum of the HRTEM lattice images for the samples annealed at 675 and 790°C hints the presence of $SrTiO_3$

in the intermediate layer. In the sample annealed at 825°C, the presence of rutile TiO_2 has been confirmed.

EDXS analysis however agrees with a Sr/Ti ratio of perovskite (1:1) in the samples annealed at 675 and 790℃. EDXS analysis for the sample anneal at 825°C shows very low X-ray intensity counts for both Sr and Ti, which suggests that the perovskite layer has almost completely been evaporated because of the high temperature of the anneal process and only some rutile TiO_2 (and/or SrO) remained.

It was shown in this chapter that the thickness of the perovskite layer after anneal had slightly reduced (in samples anneals at 675 and 790°C by less than 0.5 nm and in the sample annealed at 825°C by 3.52nm) which suggests that atoms from the surface of the perovskite layer were evaporated during the anneal process. Figure 7.3 shows the graph of thickness-loss of perovskite as a function of temperature and time during the anneal process in vacuum.

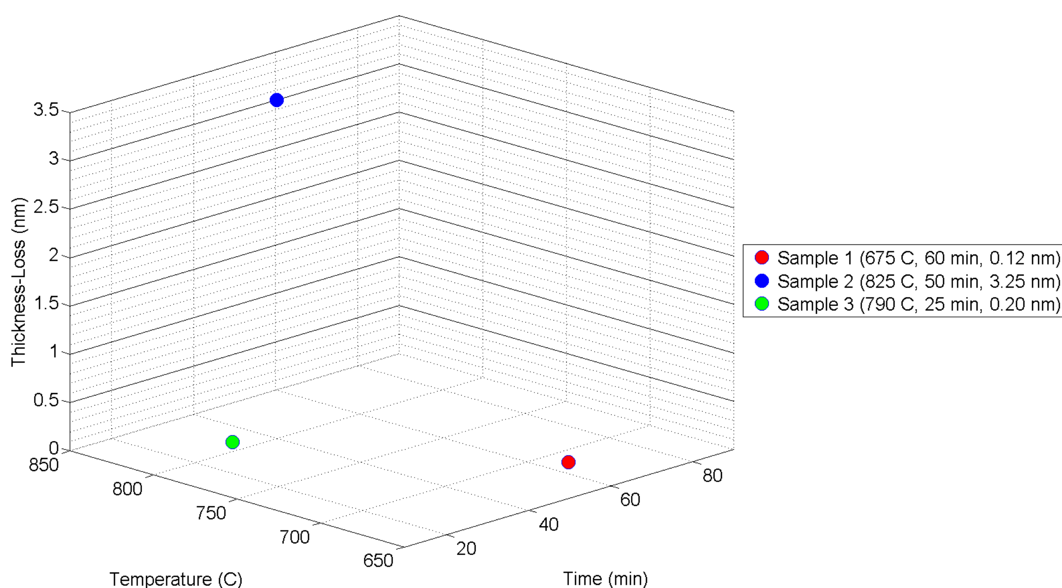

Figure 7.3. Perovskite thickness-loss per °C/min during the anneal process without presence of oxygen for three samples.

In this chapter the RMS surface roughnesses of the samples over-grown after anneal were again measured using AFM and compared with the results of the interface roughness calculated from the ADF-STEM images. Figure 7.4 shows these results in one graph to compare the methods.

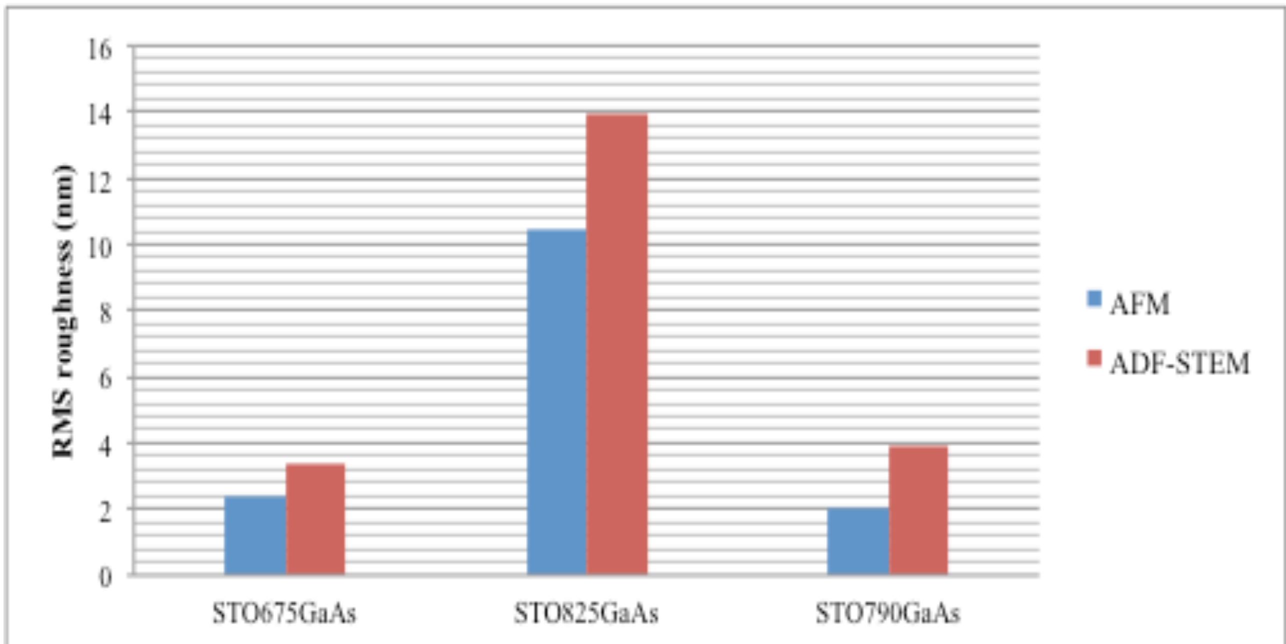

Figure 7.4. Surface roughnesses of the over-grown samples measured using AFM and calculated from ADF-STEM images.

Annealing the samples with perovskite layers in the presence of oxygen might be an alternative way to successfully re-crystalline the perovskite layer [19,74] but the MBE system used for the anneal and over-growth processes was unable to perform with oxygen. Therefore, a suggestion to continue this study would be to anneal the poly-crystalline perovskite in the presence of oxygen to re-crystallize it before putting it back in the MBE chamber for over-growth.

To avoid loss of perovskite I suggest putting two wafers face-to-face to each other and putting them in the chamber to anneal. If the perovskite layer doesn't melt at the crystallization temperature, the atoms of the layer can't evaporate from the surface and after the anneal process it should be possible to separate the wafers unless the surface has become atomically smooth (wafer bonded).

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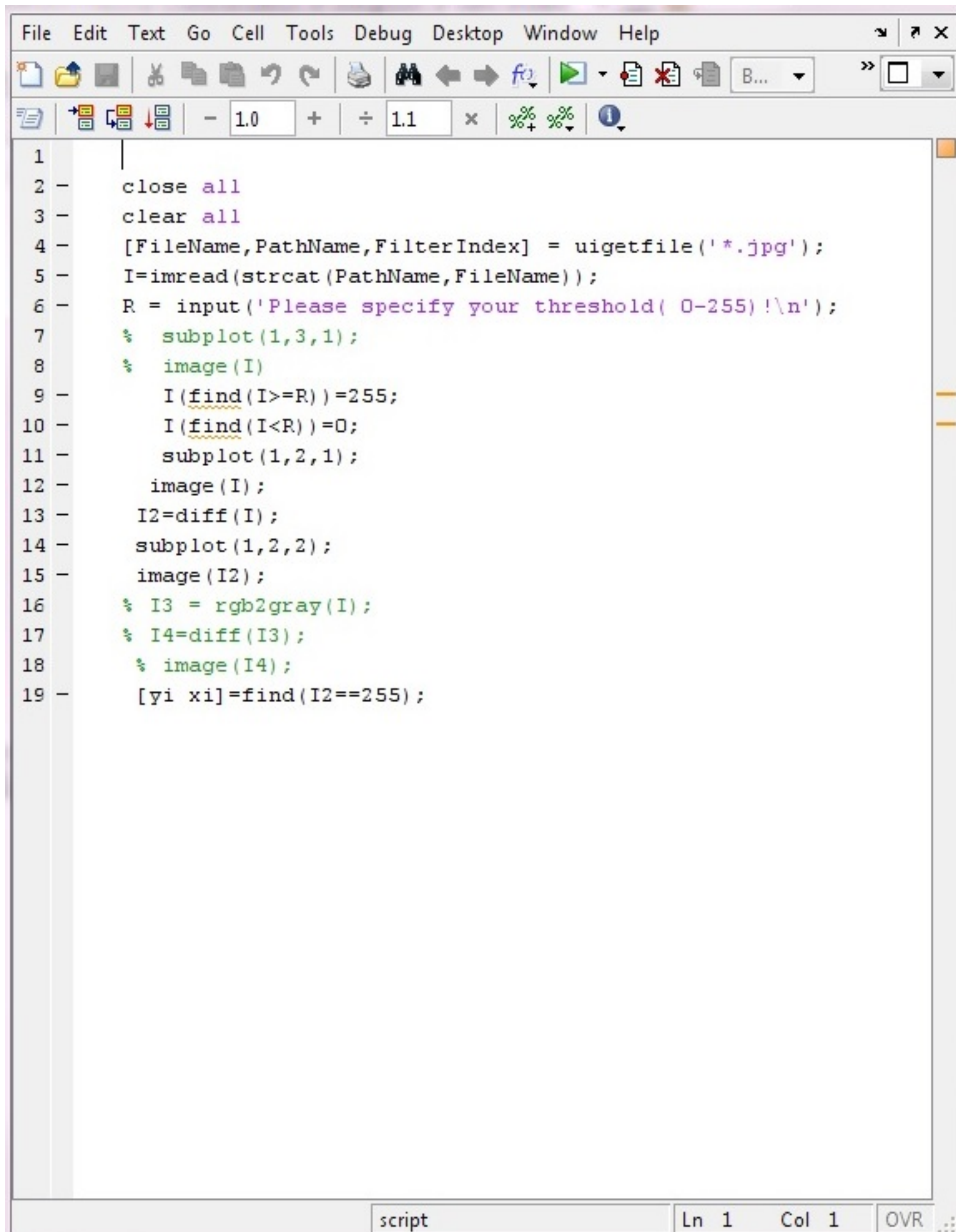
Appendix

MATLAB code used to calculate the RMS surface roughness of the layers on the STEM images



```
close all
clear all
[FileName,PathName,FilterIndex] = uigetfile('*.jpg');
I=imread(strcat(PathName,FileName));
R = input('Please specify your threshold( 0-255)!\n');
%  subplot(1,3,1);
%  image(I)
   I(find(I>=R))=255;
   I(find(I<R))=0;
   subplot(1,2,1);
  image(I);
 I2=diff(I);
 subplot(1,2,2);
 image(I2);
% I3 = rgb2gray(I);
% I4=diff(I3);
 % image(I4);
 [yi xi]=find(I2==255);
```