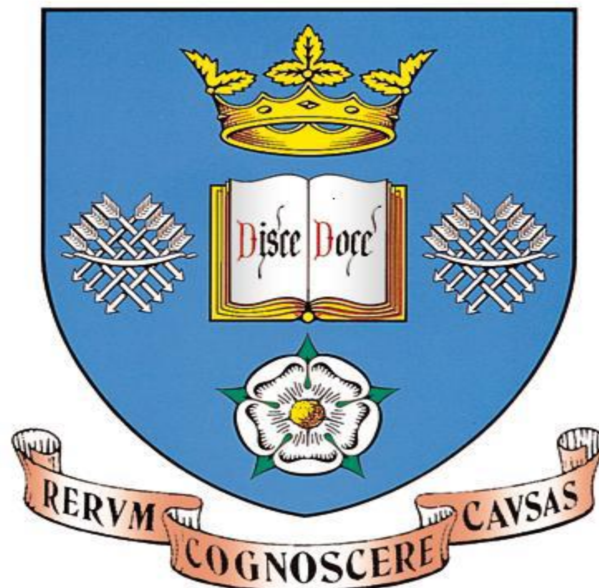
Fabrication, Simulation, and Cascading of Electrically Pumped Vertical External Cavity Surface Emitting Lasers (EP-VECSELs)

By

Xiao Jin



Department of Electronic and Electrical Engineering

Thesis submitted to the University of Sheffield for the degree of Doctor of Philosophy

June 2015

Intentionally Blank

Abstract

This thesis describes the design, fabrication, simulation, and cascading of electrically pumped external cavity surface emitting lasers (EP-VECSELs) with substrate emission at 980 nm.

Initially, a brief literature review is provided on the history of all types of semiconductor lasers in chapter 1. The design of the wafer structure is discussed in chapter 2, including the characteristics of distributed Bragg reflectors (DBRs), active region geometry, and cavity resonance.

In chapter 3, a full description of the fabrication process of the device is presented, with the development of the etched trench and dielectric layer deposition process. Circular transmission line measurement (CTLM) for measuring contact resistance and the optimisation of contacts is also presented.

Several measurement techniques are introduced in chapter 4, such as beam quality (M^2) measurement and electroluminescence (EL) mapping of the output beam intensity profile which is subsequently used in chapter 5.

In chapter 5, a model is developed for simulating substrate emitting EP-VECSELs with an etched trench. A good agreement is achieved between the simulation and measurement results which confirm the validity of the model. I then go on to make a parametric study for improving the carrier distribution profile within the EP-VECSEL. New design geometries are highlighted and explored.

A dual chip cascaded EP-VECSELs system is demonstrated in chapter 6. This is a new route to achieve high power EP-VECSELs. Evidence for injection locking is observed from spectral results when two devices have the same cavity resonance wavelength. Also, a dual wavelength cascaded EP-VECSELs system is demonstrated when the cavity resonance wavelengths of the two devices are different.

Acknowledgements

First and most importantly, I would like to thank my supervisor Professor Richard Hogg for his tireless guidance, inspiration, and help since the first day I joined group. Thanks to him for tolerating my ignorance, and teaching me to become a qualified researcher. Without his support I could not make any achievements and I will always be grateful to him.

Secondly, I would like to thank the all the senior members in our group. Thanks to Dr Pavlo Ivanov for his guidance on my simulation works. Thanks to Dr Nasser Babazadeh for teaching me about device fabrication. Thanks to “Big” Dave Childs who patiently answers all my questions with his profound knowledge. Thanks Dr Qi Jiang and Dr Ziyang Zhang for telling me their research experience which saved me a lot of time.

I would like to thank all my colleagues in my office Dr Jon Orchard, Dr David Williams, Dr Siming Chen, Dr Kejia Zhou, Timothy Roberts and Hongchi Lei. Also, I would also like to thank all the colleagues in our group. Especially I would like to thank Dr Xuesong Hu for our deep friendship.

Finally, I would like to thank my respected parents for supporting me both materially and spiritually on my study and life in the UK, without my father’s insistence I would not start my research work. I also want to thank my dear wife who has been waiting for me in China for two years.

List of Publications

Journal Papers

X. Jin, P. Ivanov, D. T. D. Childs, N. Babazadeh, J. Orchard,B. Stevens and R.A. Hogg,

“Simulation of Substrate Emitting EP-VECSELs”,

Manuscript in preparation.

X. Jin, JRautiainen,D. T. D. Childs, P. Ivanov, N. Babazadeh, J. Orchard,B. Stevens and R.A. Hogg,

“Cascaded Electrically Pumped Vertical External Cavity Surface Emitting Lasers”,

Submitted.

Chen, SM ; Zhou, KJ ; Zhang, ZY ; Wada, O ; Childs, DTD ; Hugues, M ; Jin, X ; Hogg,RA,

“Room temperature simultaneous three-state lasing in hybrid quantum well/quantum dotlaser”,

Electronics Letters, vol. 48, pp. 644-645, 2012.

Conference Proceeding Paper

X. Jin, P. Ivanov, D. T. D. Childs, N. Babazadeh, J. Orchard, B. Stevens and R.A. Hogg,

“Optimisation of Fundamental Transverse Mode Output in Electrically Pumped Vertical External Cavity Surface Emitting Lasers”,

Proc SPIE, vol. 9349, 2015.

Conference Poster

X. Jin, P. Ivanov, D. T. D. Childs, N. Babazadeh, J. Orchard,B. Stevensand R.A. Hogg,

“Optimisation of Fundamental Transverse Mode Output in Electrically Pumped Vertical External Cavity Surface Emitting Lasers”,

SPIE Photonics West, San Francisco, California, USA (2015).

X. Jin, P. Ivanov, D.T.D. Childs, N. Babazadeh, and R.A. Hogg

“Study of Factors Limiting Fundamental Transverse Mode Output in Electrically Pumped Vertical External Cavity Surface Emitting Lasers”,

UK Semiconductor conference, University of Sheffield, UK, July (2014).

Contents

Abstract iii

Acknowledgements v

List of Publications vi

1. Introduction 1

1.1 Semiconductor lasers 1

1.2 Edge emitting lasers 1

1.3 Vertical emission lasers 2

1.3.1 Vertical cavity surface emitting laser (VCSEL) 2

1.3.2 Optically pumped vertical external cavity surface emitting laser (OP-VECSEL) 4

1.3.3 Electrically pumped vertical external cavity surface emitting laser (EP-VECSEL) 7

1.3.4 Device geometries 8

1.3.5 Comparison between OP- &EP- VECSELs 11

1.4 Aims of project 12

1.5 Thesis outline 13

Reference 16

2. Device Design 21

2.1 Introduction 21

2.2 Distributed Bragg reflectors 22

2.3 Active region 29

2.4 Resonant cavity wavelength 33

2.5 Final design of the structure 38

2.6 Summary 40

Reference 42

3. Devices Fabrication Process and Improvement 45

3.1 Introduction 45

3.2 Fabrication process 45

3.3 Fabrication process improvement 66

3.3.1 Improvement of trench etching recipe 67

3.3.2 Improvement of silicon dioxide deposition process 70

3.3.3 Improvement of annealing process 72

3.4 Conclusion 77

3.5 Future work 77

Reference 78
4. Device Characterisation Techniques 79
4.1 Introduction 79
4.2 Device general measurements 79
4.3 Power scaling 83
4.4 Detuning 84
4.5 Beam quality measurement 87
4.6 Electroluminescence mapping 92
4.7 Summary 94
Reference 96
5. Modelling Study of Factors Affecting Uniform Carrier Injection in EP-VECSELs 98
5.1 Introduction 98
5.2 The model 99
5.2.1 Physical effects included into the model 99
5.2.2 Model calibration 101
5.3 Parametric study 107
5.4 Summary 115
5.5 Future work 116
Reference 117
6. Cascaded EP-VECSELs 119
6.1 Introduction 119
6.2 Cavity geometry 120
6.3 Results 123
6.4 Summary 132
6.5 Future Work 132
Reference 134
7. Summary and Future Works 136
7.1 Summary 136
7.2 Future works 138
Appendix A 140
Appendix B 141

1. Introduction

1.1 Semiconductor lasers

Since the first laser was demonstrated in 1960 [1], many types of lasers have been developed in the past a few decades. The semiconductor laser has been intensively studied and applied in many kinds of areas due to its flexible emission wavelength achievable by bandgap engineering. Nowadays, one of the most important applications for semiconductor lasers is coupling with fibres in optical fibre communication. Thus, lasers with both fundamental transverse mode and high output power are favoured. In semiconductor lasers, there are two main types of device depending on their emission geometry; one is the edge emitting lasers where the output beam parallel to the chip surface, the other types are vertical emitting lasers where the light output is perpendicular to the chip surface. These lasers will be discussed in the following sections.

1.2 Edge emitting lasers

The semiconductor edge emitting laser was developed since the 1960s [2–4]. Fig. 1.1 shows a schematic diagram of the chip structure of the edge emitting laser, where a waveguide is used to guide output light and the two facets act as mirrors to form the Fabry-Perot (F-P) cavity. The length of this cavity is typically in the range of a few hundred micrometres to a few millimetres. To date, the output powers can be up to 20 W from single laser diode with a aperture of 96 μm [5]. The edge emitting lasers can also form 1-D arrays with

over 100 W of total output power being achieved [6]. Fundamental transverse mode output power is about 0.4W [7]. However, due to the nature of the waveguide, the output beam profile from edge emitter lasers has an asymmetric elliptical shape and large divergence; this can be a problem when couples the beam into a fibre and gives a low coupling efficiency. Therefore, the edge emitting lasers are not suitable in applications for optical fibre communications.

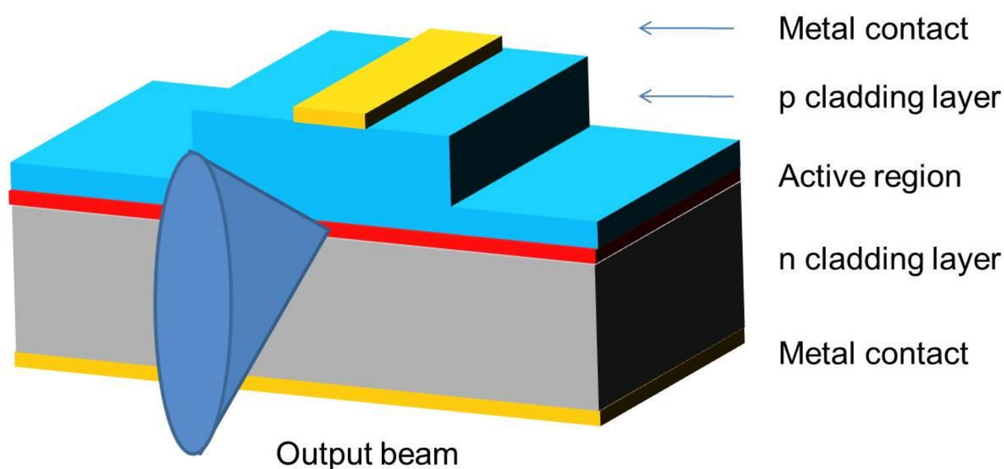


Figure 1.1 Schematic diagram of a conventional edge emitting laser with elliptical output beam.

1.3 Vertical emission lasers

1.3.1 Vertical cavity surface emitting laser (VCSEL)

Following on from edge emitting lasers, a new laser structure was conceived by K.Iga in 1977 which is called the vertical cavity surface emitting laser (VCSEL) [8]. The device structure is shown schematically in Fig. 1.2, with the active region being sandwiched between two mirrors; the mirrors can be metal but are often semiconductor multi-layer stacks (distributed Bragg reflectors (DBRs)) which will be discussed in detail in chapter 2. As the gain medium thickness in the vertical devices is only a few hundreds of angstrom, the single

pass gain of the photons is quite small as compared to edge emitting lasers. Thus, the two mirrors require high reflectivity (often larger than 99.9%) to make the photons travel many times inside the cavity to generate enough amplification. Compared to edge emitting lasers, VCSELs have circular beam shape, narrow beam divergence, low fabrication cost, fast modulation rates and naturally form 2D arrays to achieve higher power. Now they are widely used in many areas, such as local area networks (LANs), printers, and smart pixels [9-10].

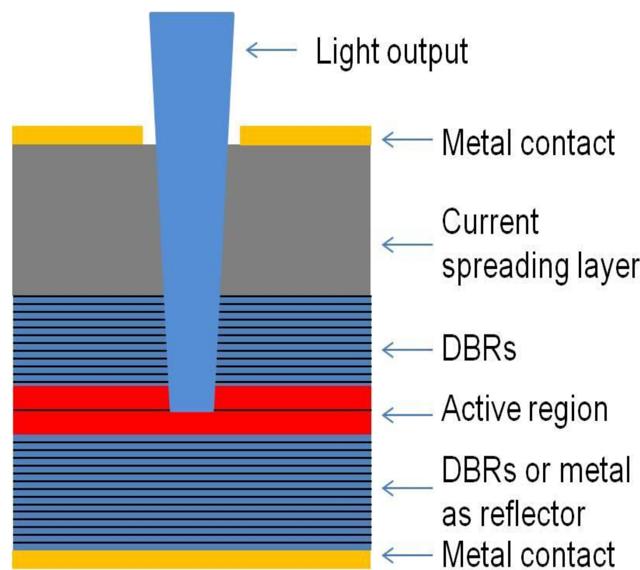


Figure 1.2 Schematic diagram of VCSEL structure.

After the VCSEL concept was proposed, the first working device was demonstrated in 1979 by using GaInAsP-InP material with an emission wavelength at 1.18 μm [11]. Device lasing under continuous wave drive conditions at room temperature was achieved after a further decade by the use of metal organic chemical vapour phase deposition (MOCVD) to grow the epitaxial layersin 1989 [12]. Recently, single VCSELs with output powers of 380 mW have been reported [13]. Also, the threshold current density of VCSEL has decreased from 162 kA/cm^2 [14] to about 0.5 KA/cm^2 [15]. But as

the output power increases by increasing device diameter, the fundamental transverse mode cannot be maintained due to the non-uniform carrier distribution profile generated. The fundamental transverse mode output power is still below 10 mW [16]. Therefore, VCSELs still cannot simultaneously achieve both high power and high quality beam shape and it can be only used in short distance fibre communication.

1.3.2 Optically pumped vertical external cavity surface emitting laser (OP-VECSEL)

In order to overcome the drawbacks in VCSELs, a novel type of laser called a vertical external cavity surface emitting lasers (VECSELs) has been developed since the middle of the 1990s [17-18], in order to simultaneously achieve high output power with fundamental transverse mode. Depending on the excitation method, VECSELs are referred to as optically or electrically pumped, and these will be discussed separately in the following section.

Fig. 1.3 shows aschematic diagram of the optically pumped VECSEL (OP-VECSEL) structure. This device contains a semiconductor chip with an external mirror to form the external cavity, in the semiconductor chip; only one end mirror with high reflectivity is present under the active region. It is worth pointing out that the use of external cavity is one of the most important features in VECSELs. It defines and stabilises the fundamental transverse mode output [19]. As it is optically pumped, a pump laser with shorter emission wavelength is used to pump the gain region of the semiconductor chip. With the use of an optical lens the incident beam spot on the semiconductor chip gain area can be adjusted, achieving power scaling.

Combined with the external mirror, the pumped spot size and the mode size need to be matched with each other, thus both fundamental transverse mode and high output power can be achieved at the same time which is highly challengingin for edge emitting lasers and VCSELs. Furthermore, the uniform distribution of the pump beam profile generates a uniform heat distribution within the active region. Hence, the heat can be dissipated by heat sink in a 1-D heat flow [19].

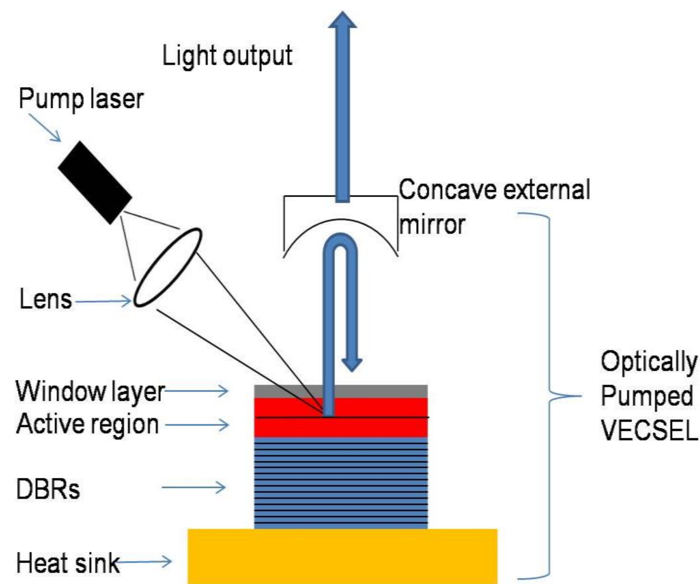


Figure 1.3 Schematic diagram of OP-VECSEL structure with pump laser.

The OP-VECSELs have been proved to achieve high power with single mode simultaneously. So far, a single OP-VECSEL has been reported with a multimode power up to 106 W [20] and single transverse mode at 23.8 W [21]. The formation of the external cavity also provides flexibility in the design of the cavity configuration. Many different shapes of cavity have been demonstrated, such as V shaped cavity [22], Z-shaped cavity [22-23], T shaped cavity and VVV shaped cavity [25]. These different cavity shapes allow the use of various optical elements to achieve different purposes, such as second-harmonic generation with etalon [26], passively mode locking with semiconductor

saturable absorber mirror (SESAM) to generate ultra-short pulses [27-28], dual chips to achieve power scaling [29] and THz generation [30].

Fig. 1.4 shows a schematic of the band structure of an OP-VECSEL. The beam from the pump laser is incident on the active region of the semiconductor chip, and those photons are absorbed by the pump absorbing region and create electrons and holes. Subsequently, these carriers diffuse into the QWs which have smaller bandgap. The QWs needs to be placed close to the antinodes of the standing wave in order to reduce threshold gain and this structure arrangement will be discussed in detail in chapter 2. Once in the QWs, the electrons and holes can recombine and emit photons with lower energy than the pump laser. The OP-VECSEL can be considered as a power and mode converter, it can transfer a high power, multimode pump beam, into a lower output power with good beam quality [19]. A window layer containing a larger bandgap is on the top of the gain region to minimise non-radiative recombination at the air semiconductor surface.

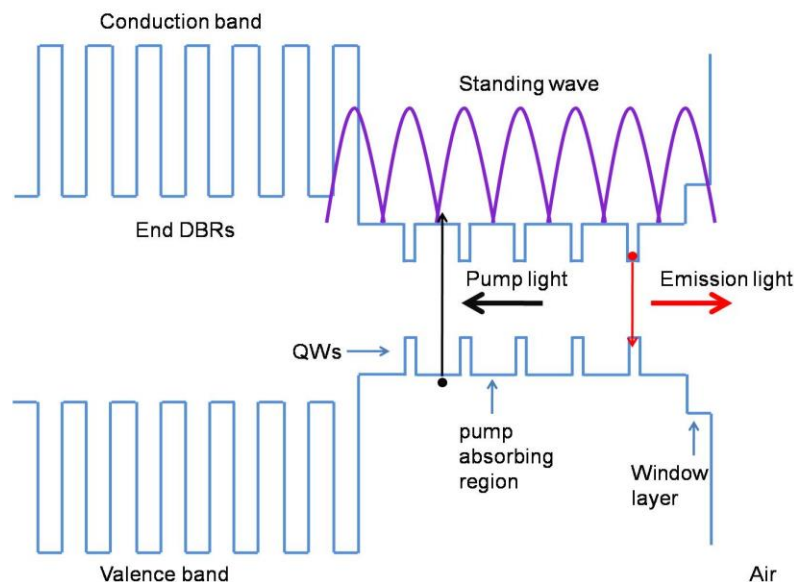


Figure 1.4 Schematic diagram of bandgap structure for OP-VECSELs.

1.3.3 Electrically pumped vertical external cavity surface emitting laser (EP-VECSEL)

Following on from the OP-VECSELs, VECSELs pumped by electricity were first presented by Novalux Inc in 2001[31]. As shown in the Fig. 1.5, this type of device has a similar structure to a VCSEL but with one of the mirrors having a lower reflectivity and an external mirror forms external cavity.

EP-VECSELs have the same applications as OP-VECSELs. The removal of the pump lasers in EP-VECSELs makes it more compact and lower cost. The EP-VECSEL is therefore attractive in higher volume applications than the OP-VECSEL. A numerical analysis on the design of EP-VECSELs has been reported [32]. But current injection brings some new problems which do not need to be considered in OP-VECSELs, such as the balance between device resistance and doping level must be carefully considered [33], and the current spreading layer thickness should be optimised in order to provide enough diffusion length to carriers while minimising the optical loss [34].

So far, single EP-VECSELs have been reported with output powers of 4.7 W in multimode [35] and ~500 mW in fundamental transverse mode [36]. In order to achieve the same performance of the OP-VECSELs, more research is needed to improve the performance of the EP-VECSELs in order to replace the OP-VECSELs in future. A comparison between two types of VECSELs will be discussed in the next section.

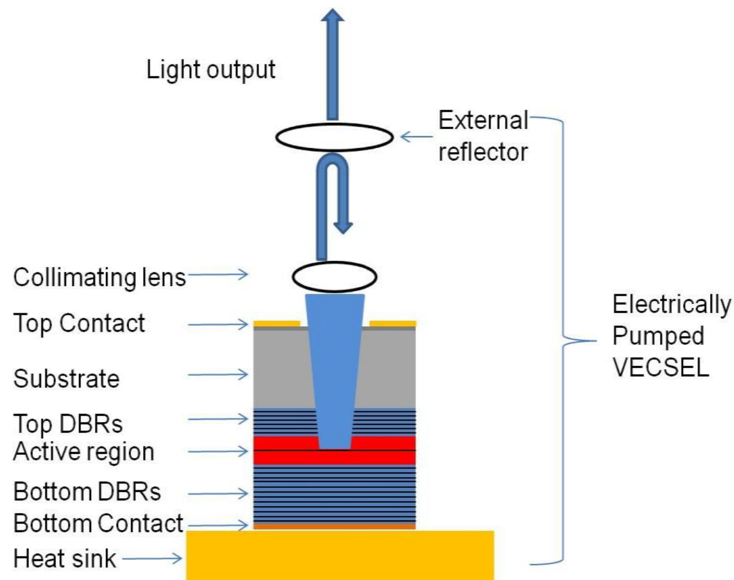


Figure 1.5 Schematic diagram of EP-VECSEL structure.

1.3.4 Device geometries

In electrically pumped vertical lasers, the single transverse mode output is determined by the carrier distribution profile across the active region. Many studies have been carried out in order to achieve this in large diameter devices in order to increase the single mode output power. Several widely applied device geometries for carrier confinement will be introduced in this section. Some of them are applied in both VCSELs and EP-VECSELs.

Fig. 1.6 depicts a device structure with an oxide confinement layer. A high Al-containing layer can be placed above the active region and this layer can form a oxide confinement aperture by wet thermal oxidation [37]. The use of this structure can reduce the threshold current by providing confinement of carriers inside the oxide aperture. Also the reduction of the refractive index in oxide layer provides wave guiding vertically [38]. This structure can be improved using double oxide layer confinement [39]. But in order to meet the requirement of single mode condition, the normalised frequency V is introduced,

$$V = \frac{2\pi r}{\lambda}\sqrt{(n_1)^2 - (n_2)^2}, \tag{1.1}$$

Where r is device radius, n_1 is the refractive index on the center of the waveguide; n_2 is the effective refractive index of the cladding layer. Devices can only support fundamental transverse mode when $V < 2.405$. Therefore, single mode output can be maintained only in ~ few micron diameter devices [40].

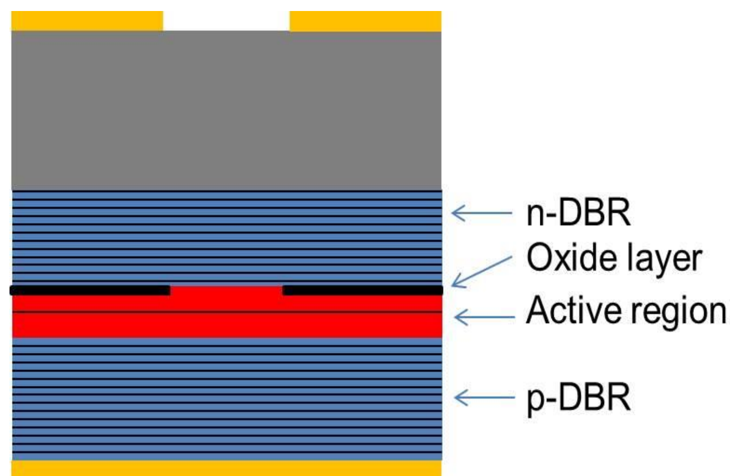


Figure 1.6 Device structure with oxide confinement layer.

Fig. 1.7 shows the schematic of a device structure with proton implantation. This implanted layer can provide a good lateral confinement of the current by locally changing the conductivity of the semiconductor material. The most attractive point of this technique is that this structure is easy to fabricate and low cost. Also, it can improve power conversion efficiency of devices [41]. But it may introduce lattice defects due to the high energy ions bombarding the device. Thermal lensing effects occur under high output power operation, which will generate high order transverse modes [41-42].

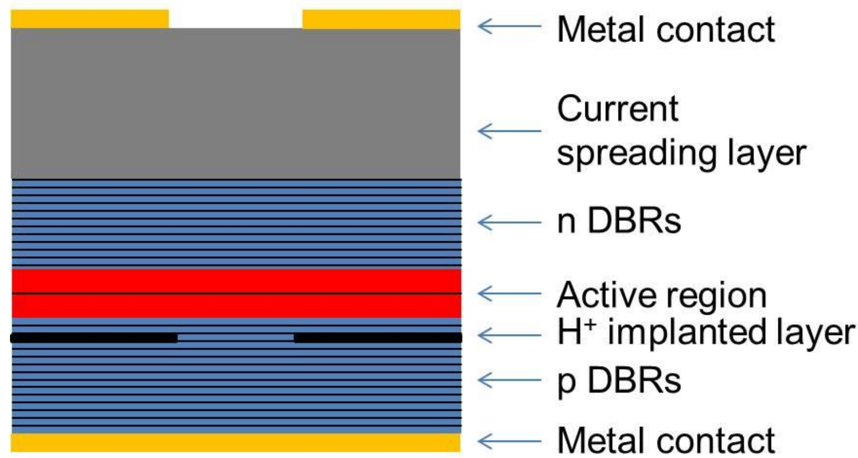


Figure 1.7 Device structure with hydrogen implanted layer.

Fig. 1.8 describes a device using buried tunnel junction (BTJ) techniques. This structure is widely used in the shortwave infrared (SWIR) region to provide current confinement. The BTJ needs to be placed at the node of electrical field in order to minimise the absorption loss, also the layers can be modulation doped to reduce the free carrier absorption (FCA) [44]. Unlike the interband absorption, in FCA the carriers which are already in the excited states will absorb photons and jump to higher energy level. Therefore, even the substrate material has higher bandgap it can still absorb photons and reduce the device efficiency. The tunnel junction is formed by the n^+ InAsSb between the n GaSb and P^+ GaSb region. In this case, only the n^+ InAsSb area can conduct current, by using lithographic and etching step the size of the tunnel junction can be defined thus achieving current confinement [45]. Besides the advantages mentioned above, it is worth noting that the BJT requires epitaxial regrowth and a selective etching step which makes the process more difficult.

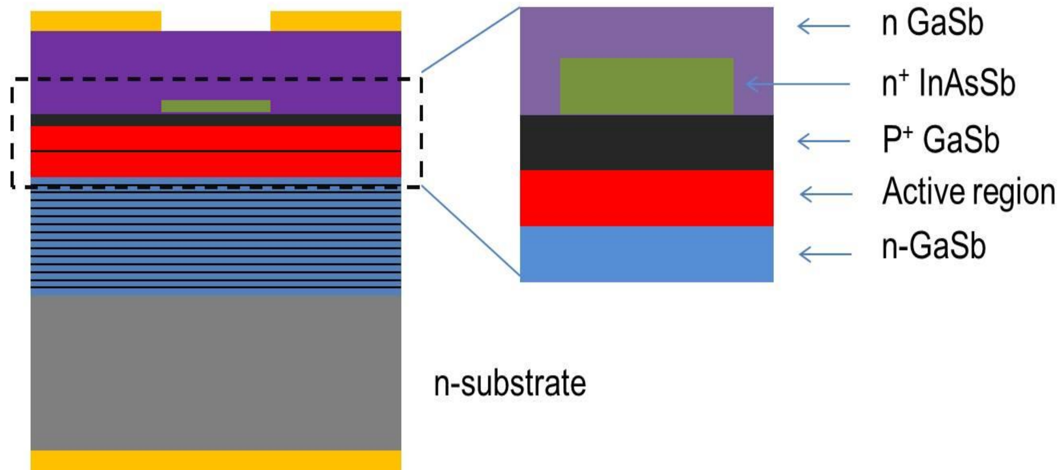


Figure 1.8 Device structure with buried tunnel junction (BTJ) emitting at 2.34 μm.

Besides the geometries mentioned above, we developed another device structure with etched trench to try to provide a better confinement to carriers which will be discussed in details later in this thesis.

1.3.5 Comparison between OP- &EP- VECSELs

In my thesis only EP-VECSELs are researched, but it is still worthwhile to make a comparison between the two types of VECSELs. In general, both the optically and electrically pumped VECSELs have their own merits and drawbacks. For OP-VECSELs, initially it is obvious to see that only one end mirror contained in the semiconductor chip will simplify the epitaxial process. Optically pumped devices do not require electrical contacts for current injection, thus making the fabrication process easier. Also, due to there being no n or p doping in the semiconductor layers, the OP-VECSELs can avoid free carrier absorption loss which is a main factor in limiting the output power in EP-VECSELs [46]. The self-heating effect is weak because the Joule heat generated by device resistance can be eliminated. Last but not least, in OP-VECSELs a uniform output beam profile can be easily achieved by changing the pump geometry of the gain area of the semiconductor chip. Therefore, a

near perfect beam quality ($M^2 \approx 1$) can be maintained even in large diameter devices with high output power which has been difficult to achieve in EP-VECSELs to date.

Simultaneously, the main drawbacks of OP-VECSELs is that it needs additional alignment due to the use of a pump source which will make the setup structure more complicated and the device becomes less compact and more expensive. The quantum defect, which is the energy difference between the incident pump photons and the emitted photons, decreases the overall laser efficiency in OP-VECSELs, and may pose heating issues. It must be admitted that the EP-VECSELs have some technological challenges, but it is an attractive and competitive device which can replace OP-VECSELs in the future.

1.4 Aims of project

Orchard *et al.* have presented EP-VECSELs with etched trenchs in previous work [4-5]. As we are the only research group that uses etched trench in order to confine charge carriers, many issues around the engineering of this structure have not been reported.

Further development of the fabrication process is required in order to reliably and repeatedly realise high quality devices. There is no study reported on the fabrication process for etched trench structures. A trench with straight sidewalls and good coherent dielectric layer plays an important role on the EP-VECSEL performance.

Some models have been used for simulating current distributions in EP-VECSELs. But to date no modeling has been applied to etched trench structures. As a result, a systemic investigation of key factors impacting the carrier distribution profile within the device has not been reported.

In EP-VECSELs, power scaling shows a limitation when the device diameter increases. In OP-VECSELs there are many different types of multi-cavity shapes which have been designed for all kinds of purposes including power scaling. However, in EP-VECSELs only the linear cavity has been applied in experiments so far, and there is no report on using multiple chips to form cascaded system within the same cavity in order to achieve power scaling.

1.5 Thesis outline

This thesis discusses several aspects in the development of EP-VECSELs.

Chapter 2 discuses wafer design issues. Initially simulations using CAMFR [48] were carried out in order to determine the number of DBR pairs on each side of the cavity, also an intermediate layer is added between each DBR material to reduce the series resistance, results show that $Al_{0.47}Ga_{0.53}As$ with refractive index between the two DBR materials ($Al_{0.8}Ga_{0.2}As$/GaAs) with a thickness of 10 nm can maintain good optical properties of the DBR pairs while reducing resistance. Next, the intra-cavity with periodic gain structure (PGS) is introduced; as two groups of three QWs are used for present wafers, 1.8 times of increasing on optical confinement is achieved. Modelling results also shown that the thickness of epitaxial layers should be controlled carefully during the epitaxial process. Especially, the cavity resonant wavelength is

quite sensitive to DBR thickness changes. Reflectivity spectra at the centre wavelength show a minimum when the numbers of DBR pairs at both sides of the active region are the same. The use of the method for wafer characterisation is discussed.

Chapter 3 describes the development of fabrication processes for EP-VECSELs with an etched trench structure. An improvement of the etch profile of the trench is made by carefully changing the etch parameters. Thus a trench with straight side wall can be observed from SEM results. Subsequently, annealing tests were carried out to optimise the contact resistance of the devices. Considering the results of contact resistance versus annealing temperature, and the order that annealing has to be carried out, an annealing temperature of 360 °C is shown to be optimum.

Chapter 4 presents several experimental techniques used for characterizing EP-VECSELs. First the linear cavity setup used for general L-I-V and spectrum measurements for devices is described. Then I discuss the effect of detuning on the performance of EP-VECSELs and briefly introduce an etch method to determine the value of detuning across the whole wafer. After that I discuss the light intensity distribution measurement technique using an electroluminescence (EL) mapping system. This measurement result is then used for assessment of the model developed in chapter 5.

Chapter 5 presents a model of EP-VECSELs for simulating the transverse carrier distribution profile using a commercial software package (Rsoft LaserMod) [49]. This is due to the beam quality (M^2) of EP-VECSELs being determined by the charge carrier distribution profile inside the devices. First

the model is calibrated by using the EL measurement data of devices provided in chapter 4, also the effects of contact misalignment are taken into account. A good agreement between simulated and experimental results is achieved, confirming the validity of the model. Subsequently, I investigate parameters which can affect the carrier distribution profile. Analysis of the trench depth indicates that it plays a key role in determining the carrier distribution profile. Results shows that a device structure with thinner substrate thickness compare to present structure and a trench etched into the substrate should improve the carrier distribution profile [50].

Chapter 6 reports the first demonstration of two cascaded EP-VECSELs within the same cavity. This cascaded system is designed to overcome the power scaling limitation due to the non-uniform carrier distribution in large diameter devices. This cavity has an asymmetric x-shape, with one of the devices being wavelength tuned by a heat sink and the other is tuned by self-heating alone. Initially single devices are measured separately in a simple linear cavity for comparison. 1.4 times the total output power is achieved in cascaded cavity as compared to a single device. Spectral results show evidence that injection locking is observed when the cavity resonance of the two devices is coincident. By changing the temperature of the heat sink, the cavity resonance wavelength of two devices may be made to be different and a dual wavelength cascaded EP-VECSELs system is presented.

Chapter 7 will briefly summarise my whole work in this thesis.

Reference

[1] T. H. Maiman, “Stimulated Optical Radiation in Ruby,” *Nature*, vol. 187, no. 4736, pp. 493–494, 1960.

[2] M. I. Nathan, W. P. Dumke, G. Burns, F. H. Dill, and G. Lasher, “Stimulated emission of radiation from GaAs p-n junctions,” *Appl. Phys. Lett.*, vol. 1, no. 3, pp. 62–64, 1962.

[3] N. Holonyak and S. F. Bevacqua, “Coherent (visible) light emission from Ga(As1-xPx) junctions,” *Appl. Phys. Lett.*, vol. 1, no. 4, pp. 82–83, 1962.

[4] R. N. Hall, G. E. Fenner, J. D. Kingsley, T. J. Soltys, and R. O. Carlson, “Coherent light emission from GaAs junctions,” *Phys. Rev. Lett.*, vol. 9, no. 9, pp. 366–368, 1962.

[5] P. Crump, G. Blume, K. Paschke, R. Staske, a. Pietrzak, U. Zeimer, S. Einfeldt, a. Ginolas, F. Bugge, K. Häusler, P. Ressel, H. Wenzel, and G. Erbert, “20W continuous wave reliable operation of 980nm broad-area single emitter diode lasers with an aperture of 96μm,” *Proc. SPIE*, vol. 7198, pp. 719814–1–9, 2009.

[6] Roland Diehl, *High power diode lasers : fundamentals, technology, applications*. Spinger, 2000.

[7] M. Yuda, T. Sasaki, J. Temmyo, M. Sugo, and C. Amano, “High-power highly reliable 1.02-1.06-/spl mu/m InGaAs strained-quantum-well laser diodes,” *IEEE J. Quantum Electron.*, vol. 39, no. 12, pp. 1515–1520, 2003.

[8] K. Iga, “Surface-emitting laser-its birth and generation of new optoelectronics field,” *IEEE J. Sel. Top. Quantum Electron.*, vol. 6, no. 6, pp. 1201–1215, 2000.

[9] J. Geske, V. Jayaraman, T. Goodwin, M. Culick, M. Macdougal, T. Goodnough, D. Welch, and J. E. Bowers, “2.5-Gbs Transmission over 50 km with a 1.3-um Vertical-Cavity Surface-Emitting Laser,” *photonics Technol. Lett.*, vol. 12, no. 12, pp. 1707–1709, 2000.

[10] H. Kosaka, “Smart integration and packaging of 2-D VCSEL’s for high-speed parallel links,” *IEEE J. Sel. Top. Quantum Electron.*, vol. 5, no. 2, pp. 184–192, 1999.

[11] C. K. and Y. S. Haruhisa Soda, Ken-ichi Iga, “GaInAsP / InP Surface Emitting Injection Lasers,” *Jpn. J. Appl. Phys.*, vol. 18, no. 12, pp. 2329–2330, 1979.

[12] F. Koyama, S. Kinoshita, and K. Iga, “Room-temperature continuous wave lasing characteristics of a GaAs vertical cavity surface-emitting laser,” *Appl. Phys. Lett.*, vol. 55, no. 3, pp. 221–222, 1989.

[13] A. Higuchi, H. Naito, K. Torii, M. Miyamoto, T. Morita, J. Maeda, H. Miyajima, and H. Yoshida, “High power density vertical-cavity surface-emitting lasers with ion implanted isolated current aperture: erratum,” *Opt. Express*, vol. 20, no. 4, pp. 4206–4212, 2012.

[14] K. Iga, S. Ishikawa, S. Ohkouchi, and T. Nishimura, “Room temperature pulsed oscillation of GaAlAs/GaAs surface emitting junction laser,” *Appl. Phys. Lett.*, vol. 45, no. 4, pp. 348–350, 1984.

[15] Y. Ding, W. J. Fan, D. W. Xu, C. Z. Tong, Y. Liu, and L. J. Zhao, “Low threshold current density, low resistance oxide-confined VCSEL fabricated by a dielectric-free approach,” *Appl. Phys. B Lasers Opt.*, vol. 98, no. 4, pp. 773–778, 2010.

[16] J. W. Shi, K. L. Chi, J. H. Chang, Z. R. Wei, J. W. Jiang, and Y. J. Yang, “Single-mode vertical-cavity surface-emitting laser array with high power and narrow far-field divergence angle,” *IEEE Photonics J.*, vol. 5, no. 6, p. Art. ID 1502508, 2013.

[17] M. Kuznetsov, F. Hakimi, and A. Sprague, R and Mooradian, “High-Power (>0.5-W CW) Diode-Pumped Vertical-External-Cavity Surface-Emitting Semiconductor Lasers with Circular TEM00 Beams,” *IEEE Photonics Technol. Lett.*, vol. 9, no. 8, pp. 1063–1065, 1997.

[18] M. Kuznetsov, F. Hakimi, R. Sprague, and A. and Mooradian, “Design and characteristics of high-power (0.5-W CW) diode-pumped vertical-external-cavity surface-emitting semiconductor lasers with circular TEM00 beams,” *IEEE Photonics Technol. Lett.*, vol. 5, no. 3, pp. 561–573, 1999.

[19] O. G. Okhotnikov, *Semiconductor Disk Lasers: Physics and Technology*. Weinheim: Wiley-VCH Verlag GmbH & Co. KGaA, 2010.

[20] B. Heinen, T. L. Wang, M. Sparenberg, A. Weber, B. Kunert, J. Hader, S. W. Koch, J. V. Moloney, M. Koch, and W. and Stolz, “106 W continuous-wave output power from vertical-external-cavity surface-emitting laser,” *Electron. Lett.*, vol. 48, no. 9, pp. 516–U102, 2012.

[21] T. L. Wang, Y. Kaneda, J. M. Yarborough, J. Hader, J. V. Moloney, A. Chernikov, S. Chatterjee, S. W. Koch, B. Kunert, and W. Stolz, “High-Power Optically Pumped Semiconductor Laser at 1040 nm,” *IEEE Photonics Technol. Lett.*, vol. 22, no. 9, pp. 661–663, May 2010.

[22] L. Fan, M. Fallahi, J. Hader, A. R. Zakharian, J. V. Moloney, W. Stolz, S. W. Koch, R. Bedford, and J. T. Murray, “Linearly polarized dual-

wavelength vertical-external-cavity surface-emitting laser," *Appl. Phys. Lett.*, vol. 90, no. 18, pp. 1811241–3, 2007.

[23] B. Rosener, M. Rattunde, R. Moser, C. Manz, K. Kohler, and J. Wagner, "GaSb-Based Optically Pumped Semiconductor Disk Laser Using Multiple Gain Elements," *IEEE Photonics Technol. Lett.*, vol. 21, no. 13, pp. 848–850, 2009.

[24] E. J. Saarinen, A. Härkönen, S. Suomalainen, and O. G. Okhotnikov, "Power scalable semiconductor disk laser using multiple gain cavity," *Opt. Express*, vol. 14, no. 26, pp. 12868–12871, 2006.

[25] S. Operation, S. Kaspar, M. Rattunde, T. Tino, S. Adler, C. Manz, K. Klaus, and J. Wagner, "Recent Advances in 2- μ m GaSb-Based Semiconductor Disk Laser — Power Scaling , Narrow-Linewidth and Short-Pulse Operation," *IEEE J. Sel. Top. QUANTUM Electron.*, vol. 19, no. 4, 2013.

[26] M. a. Holm, D. Burns, a. I. Ferguson, and M. D. Dawson, "Actively stabilized single-frequency vertical-external-cavity\nAlGaAs laser," *IEEE Photonics Technol. Lett.*, vol. 11, no. 12, pp. 1551–1553, 1999.

[27] U. Keller, K. J. Weingarten, F. X. Kärtner, D. Kopf, B. Braun, I. D. Jung, R. Fluck, C. Hönninger, N. Matuschek, and J. Aus Der Au, "Semiconductor saturable absorber mirrors (SESAM's) for femtosecond to nanosecond pulse generation in solid-state lasers," *IEEE J. Sel. Top. Quantum Electron.*, vol. 2, no. 3, pp. 435–451, 1996.

[28] S. Hoogland, S. Dhanjal, A. C. Tropper, J. S. Roberts, R. Häring, R. Paschotta, and U. Keller, "Passively Mode-Locked Diode-Pumped Surface-Emitting Semiconductor Laser," *IEEE Photonics Technol. Lett.*, vol. 12, no. 9, pp. 1135–1137, 2000.

[29] L. Fan, M. Fallahi, J. Hader, A. R. Zakharian, J. V Moloney, J. T. Murray, R. Bedford, W. Stolz, and S. W. Koch, "Multichip vertical-external-cavity surface-emitting lasers: a coherent power scaling scheme," *Opt. Lett.*, vol. 31, no. 24, pp. 3612–3614, 2006.

[30] M. Scheller, J. M. Yarborough, J. V Moloney, M. Fallahi, M. Koch, and S. W. Koch, "Room temperature continuous wave milliwatt terahertz source," *Opt. Express*, vol. 18, no. 26, pp. 27112–27117, 2010.

[31] J. G. McInerney, A. Mooradian, A. Lewis, A. V. Shchegrov, E. M. Strzelecka, D. Lee, J. P. Watson, M. K. Liebman, G. P. Carey, A. Umbrasas, C. a. Amsden, B. D. Cantos, W. R. Hitchens, D. L. Heald, V. V. Doan, J. L. Cannon, and K. L. Lear, "High brightness 980 nm pump lasers based on the Novalux Extended Cavity Surface-Emitting Laser (NECSEL) concept," *SPIE Proc.*, vol. 4947, no. 2003, pp. 240–251, 2003.

[32] P. Kreuter, B. Witzigmann, D. J. H. C. Maas, Y. Barbarin, T. Südmeyer, and U. and Keller, "On the design of electrically pumped vertical-external-cavity surface-emitting lasers," *Appl. Phys. B*, vol. 91, no. 2, pp. 257–264, Mar. 2008.

[33] J. R. Orchard, D. T. D. Childs, D. Williams, L.-C. Lin, B. J. Stevens, J. S. Roberts, and R. a. Hogg, "Trade-offs in the realization of electrically pumped vertical external cavity surface emitting lasers," *Semicond. Laser Conf. (ISLC), 2010 22nd IEEE Int.*, vol. 17, no. 6, pp. 1745–1752, 2010.

[34] Y.-Y. Lai, T.-C. Lu, T.-L. Ho, S.-C. Huang, and S.-C. Wang, "Numerical analysis on current and optical confinement of III-nitride vertical-cavity surface-emitting lasers," *Opt. Express*, vol. 22, no. 8, pp. 9789–9797, 2014.

[35] P. Zhao, B. Xu, R. Van Leeuwen, T. Chen, L. Watkins, D. Zhou, and P. Gao, "Compact 4.7 W, 18.3% wall-plug efficiency green laser based on an electrically pumped VECSEL using intracavity frequency doubling," *Opt. Lett.*, vol. 39, no. 16, pp. 4766–4768, 2014.

[36] J. G. McInerney, A. Mooradian, A. Lewis, A. V. Shchegrov, E. M. Strzelecka, D. Lee, J. P. Watson, M. Liebman, G. P. Carey, B. D. Cantos, W. R. Hitchens, and D. and Heald, "High-power surface emitting semiconductor laser with extended vertical compound cavity," *Electron. Lett.*, vol. 39, no. 6, pp. 523–525, 2003.

[37] Y. Laaroussi, C. Chevallier, F. Genty, N. Fressengeas, L. Cerutti, T. Taliercio, O. Gauthier-Lafaye, P.-F. Calmon, B. Reig, J. Jacquet, and and G. Almuneau, "Oxide confinement and high contrast grating mirrors for Mid-infrared VCSELs," *Opt. Mater. Express*, vol. 3, no. 10, pp. 1576–1585, 2014.

[38] C. Degen, W. Elsaber, and I. Fischer, "Transverse modes in oxide confined VCSELs: Influence of pump profile, spatial hole burning, and thermal effects," *Opt. Express*, vol. 5, no. 3, pp. 38–47, 1999.

[39] S. F. Yu, *Analysis and design of vertical cavity surface emitting lasers*, vol. 7. A JOHN WILEY & SONS, INC., 2003.

[40] G. P. Agrawal, *Fiber-Optic Communication Systems*. New York:Wiley, 2002.

[41] K. L. Lear, S. P. Kilcoyne, and S. a. Chalmers, "High power conversion efficiencies and scaling issues for multimode vertical-cavity top-surface-emitting lasers," *IEEE Photonics Technol. Lett.*, vol. 6, no. 7, pp. 778–781, 1994.

[42] and K. L. L. M. Hagerott Crawford, R. P. Schneider, Jr., K. D. Choquette, "Temperature-Dependent Characteristics and Single-Mode

Performance of AlGaInP-B ased 670-690-nm Vertical-Cavity Surface-Emitting Lasers," *IEEE Photonics Technol. Lett.*, vol. 7, no. 7, pp. 724–726, 1995.

[43] G. R. Hadley and S. W. Lear, K.L. ; Warren, M.E. ; Choquette, K.D. ; Scott, J.W. ; Corzine, "Comprehensive numerical modeling of vertical-cavity surface-emitting lasers," *EEE J. ofQuantum Electron.*, vol. 32, no. 4, pp. 607–616, 1996.

[44] M. Müller, T. Gründl, M. Horn, R. D. Nagel, W. Wiedmeier, E. Rönneberg, G. Böhm, and M. Amann, "Small-Signal Analysis of High-Temperature Stable 1550nm High-Speed VCSELs," in *Proceedings of 6th Joint Symposium on Opto- and Microelectronic Devices and Circuits*, 2010.

[45] A. Harkonen, A. Bachmann, S. Arafin, K. Haring, J. Viheriala, M. Guina, and M.-C. Amann, "2.34 um electrically pumped VECSEL with buried tunnel junction," *SPIE Photonics Eur.*, vol. 7720, pp. 7720151–7, 2010.

[46] Y. Barbarin, M. Hoffmann, W. P. Pallmann, I. Dahhan, P. Kreuter, M. Miller, J. Baier, H. Moench, M. Golling, S. Thomas, B. Witzigmann, and U. and Keller, "Electrically Pumped Vertical External Cavity Surface Emitting Lasers Suitable for Passive Modelocking," *IEEE J. Sel. Top. QUANTUM Electron.*, vol. 17, no. 6, pp. 1779–1786, 2011.

[47] J. R. Orchard, D. T. D. Childs, L. C. Lin, B. J. Stevens, D. M. Williams, and R. A. and Hogg, "Design Rules and Characterisation of Electrically Pumped Vertical External Cavity Surface Emitting Lasers," *Jpn. J. Appl. Phys.*, vol. 50, no. 4, Apr. 2011.

[48] P. Bienstman, "CAMFR manual v1.3." pp. 1–70.

[49] RSoft Design Group, "LaserMod 9 User guide," 2012.

[50] X. Jin, P. Ivanov, D. T. D. Childs, N. Babazadeh, J. Orchard, S. Ben, and R. A. and Hogg, "Optimisation of Fundamental Transverse Mode Output in Electrically Pumped Vertical External Cavity Surface Emitting Lasers," *Proc SPIE*, vol. 9349, 2015.

2. Device Design

2.1 Introduction

In this chapter, the design of the EP-VECSEL structure will be discussed. Fig. 2.1 shows a schematic diagram of the chip in a substrate emitting EP-VECSELs. Though an output reflector is needed to form the external cavity with the device in order to achieve lasing, no design issue is needed for the output reflector. Thus the design of the structure mostly concerns at the semiconductor chip.

The main parts in the semiconductor chip include a n-doped substrate, n-doped DBR, the intracavity with quantum wells (QWs), p-doped DBR, and top and bottom metal contact for injecting current. Both the n- and p-doped DBRs form the cavity surrounding the QW active zone. The substrate here acts as a current spreading layer in order to try to obtain a nearly uniform carrier distribution across the device. It is worth noting that optically pumped VECSELs can contain only one DBR to provide 100% reflectance and form cavity with the external output mirror [1–3], while generally in EP-VECSELs one more DBRs stack is added to form an intracavity in order to compensate both the optical absorption loss in the thick substrate and reduce the threshold current [4-5].

In EP-VECSELs, the series resistance may limit the device performance [6]. Hence, the first design objective of this chapter is to develop a highly reflective DBR with low series resistance. The second objective is to explore the geometry of the active region inside the cavity that can provide low threshold

gain. Following this is the study of factors affecting the resonant reflectivity spectrum of the intracavity. This chapter ends with a summary.

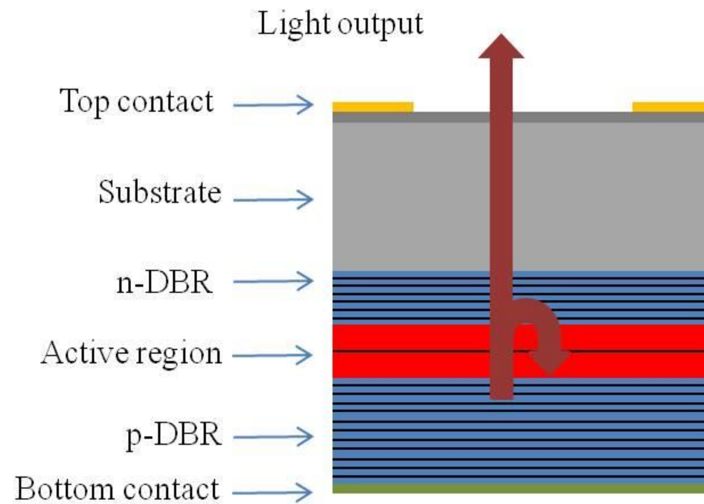


Figure 2.1 Schematic diagram of semiconductor part of a substrate-emitting EP-VECSEL.

2.2 Distributed Bragg reflectors

The cavity length in surface emitting semiconductor laser devices is usually a few microns thick. Thus, the single pass gain is small compared with edge emitter devices. Two distributed Bragg reflectors (DBRs) around the gain material can form an intracavity and provide sufficient amplification by strongly confining photons inside the cavity. Fig. 2.2 shows the schematic diagram of a DBR structure. It can be seen that the DBR pairs are composed of two materials with high and low refractive index and stacked periodically. DBRs can provide a high reflectance up to 100% [7] and have been widely applied in many semiconductor structures.

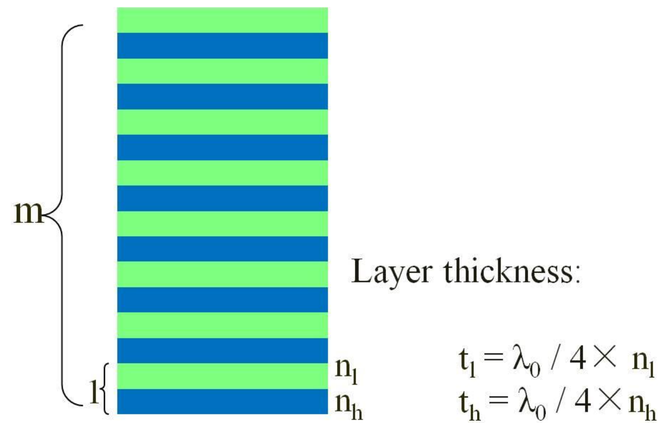


Figure 2.2 Schematic diagram of DBR stack made of two materials repeated in layers of a thickness of $t_{l/h} = \lambda_0/4n_{l/h}$.

The DBR materials used in the 980 nm EP-VECSELs described here are $Al_{0.8}Ga_{0.2}As$ and GaAs, the thickness of each layer $t_{l/h}$ is quarter wavelength in that material such that $t_{l/h} = \lambda_0/4n_{l/h}$, where λ_0 is the emission wavelength in vacuum, $n_{l/h}$ is the refractive index of high-index (h) or low-index (l) material consisting a DBR layer. The refractive indices of $Al_{0.8}Ga_{0.2}As$ and GaAs are n_l =3.07 and n_h =3.52, respectively. Hence, the quarter wavelength thickness for $Al_{0.8}Ga_{0.2}As$ layer in each pair of DBR is 79.8 nm while the thickness for GaAs layer is 69.6 nm.

In this section, the total reflectance of the DBR versus the number of DBR pairs has been investigated. Usually the transfer matrix method (TMM) can be used for calculating the total reflectance of the multi-layer stack [8-9].This method was implemented in CAMFR [10] software as well as a simple estimation of the peak reflectance.

Assuming normal incidence of the light, a simple equation can be used to estimate the total reflectance of the DBR which can be expressed as [11]

$$R = \left[\frac{1-\left(\frac{n_l}{n_h}\right)^{2m}}{1+\left(\frac{n_l}{n_h}\right)^{2m}} \right]^2 , \quad (2.1)$$

where m is the number of DBR pairs.

The peak reflectance has been calculated using both equation (2.1) and the TMM; and the full width at half maximum (FWHM) has been calculated using a TMM. These results are shown in Fig. 2.3(a). Fig. 2.3(b) shows reflectance spectra versus m by TMM matrix method, it also illustrates that the reflectance spectra within the stop band becomes flatter as m increases. Also, it is worth noting that all interfacial reflections will add in phase in the TMM method, while this part is not considered in equation (2.1). Therefore, the results calculated by equation (2.1) are always an under estimate as compared to result from CAMFR software.

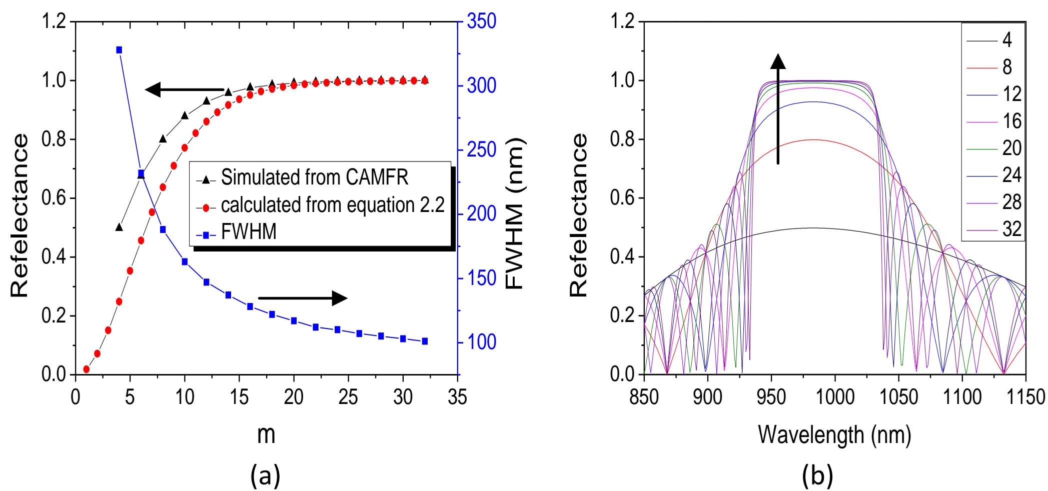


Figure 2.3 (a) Peak reflectance calculated using (2.1) and transmission matrix method; and FWHM calculated using transmission matrix method versus m; (b) reflectance spectra as a function m ranging from 4 to 32.

It can be seen from Fig. 2.3(a) that the peak reflectance increases up to almost unity as *m* increases. The reflectivity increases quite rapidly when *m* is small. But after *m* exceeds 20, the reflectance increase becomes smaller as it asymptotically reaches its maximum value.

Another important characteristic from Fig. 2.3(a) is the FWHM of the reflectance spectra. The FWHM is observed to be inversely proportional to the number of DBR pairs, and it is about 100 nm wide when *m* exceeds ~ 25. Though the larger FWHM was favoured in the design study [12], this 100 nm width is sufficient to cover the detuning between gain peak and cavity resonance wavelengths existing in the wafer which will be discussed in detail later.

The FWHM bandwidth can be approximately calculated using the following equation [13]:

$$\Delta\lambda \approx \frac{2\lambda_B \Delta\bar{n}_B}{\pi\bar{n}}, \tag{2.2}$$

where $\bar{n}$ =3.28 is the average refractive index value of DBR layers. It can be obtained a bandwidth Δλ about 86 nm as $\Delta\bar{n}_B$ =0.45, which is get agreements with the value in Fig. 2.3a under. Equation 2.2 above does not show the relationship between FWHM and the number of DBR pairs. But both equation 2.1 and 2.2 indicate that materials used in DBR should have a large refractive index contrast in order to achieve high peak reflectance and wider stopband whilst keeping the number of DBR pairs small.

It is known that there is a difference between the $Al_{0.8}Ga_{0.2}As$ and GaAs bandgap energies. As a uniform Fermi level should be generated when these two semiconductors are connected, a discontinuity of the band structure appears at the interface of these two materials. This change of band energy is schematically shown in Fig. 2.4. The band discontinuity results in a potential spike and prevents the carrier from passing through the DBR area. Therefore, the total electric resistance of the device will be increased.

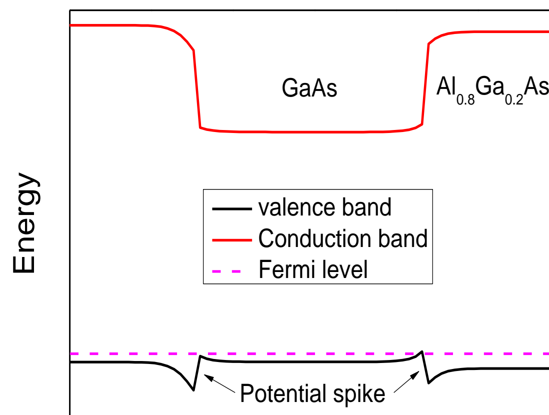


Figure 2.4 Energy band discontinuities at interface of a pair of $Al_{0.8}GaAs$ and GaAs p-DBR.

The EP-VECSEL described here emits through the n-doped substrate and therefore the p-doped DBR needs to provide a nearly 100% reflectivity. In this case, according to the result in Fig 2.3(a), more than 30 pairs of p-doped DBR need to be epitaxially grown on the wafer. Also, the holes have lower mobility and larger free carrier absorption loss compared to electrons in the n-doped region. Thus the stack of a large number of p-doped DBR pairs may have a high resistance and can generate a large amount of Joule heating resulting in a deterioration of the device performance [14]. Therefore, the reduction of resistance in the p-DBR becomes even more important.

Many studies have been carried out and several methods have been applied to solve this problem. One of the methods is to add a layer with an intermediate Al constitution between the main layers of the DBR [15-16]. The aim of depositing this intermediate layer is to improve carrier transport in the DBRs whilst maintaining its optical characteristics. Fig. 2.5 shows the valence band energy diagram with and without the intermediate layer. It can be seen that the incorporation of the layer reduces the discontinuity of the band which results in a reduction of the total resistance of the DBR. It has been reported that a linearly graded intermediate layer in the DBR can significantly reduce the series resistance [17], but it is quite difficult to achieve the linear change of material composition in the epitaxial process. Therefore, in this work, a step intermediate layer was applied.

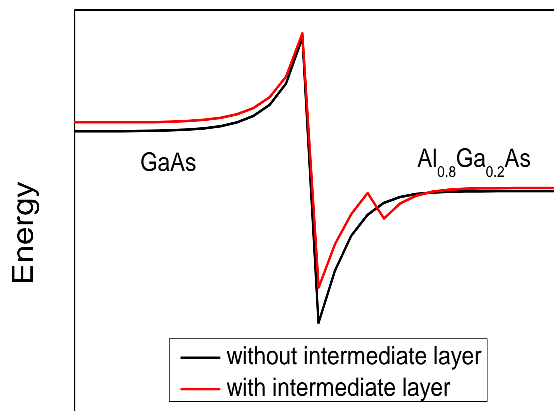


Figure 2.5 Energy band diagram of valence band of the DBR with and without intermediate layer.

The thicknesses of each DBR pair should remain the same in order to maintain the optical properties of the DBR. Hence, the thickness of each DBR layer will change from t (material) to t = t_i (intermediate) + t' (material). This newly added intermediate layer also requires having an average refractive

index of $Al_{0.8}Ga_{0.2}As$ and GaAs. In this work we use $Al_{0.47}Ga_{0.53}As$ (n=3.28) as the intermediate layer material.

The transmission matrix model was used to calculate the DBR optical characteristics with different thickness of intermediate layer, and this is shown in Fig. 2.6. The intermediate layer thickness was varied from 5 nm to 25 nm. The result indicates that the increase of intermediate layer thickness will reduce both peak reflectance and FWHM of the DBR. The intermediate layer will change the effective refractive index contrast (Δn) in DBR pairs. Hence, equations 2.1 and 2.2 suggest that the thicker the intermediate layer, the worse the optical characteristics of the DBRs. In order to achieve a lower resistance whilst keeping a high peak reflectance of the DBR, an $Al_{0.47}Ga_{0.53}As$ intermediate layer with 10 nm thickness was selected for this work.

In order to meet the requirement of device, the p-doped DBR needs to provide reflectance of more than 99.9% and 90% for n-doped DBR. Thus, according to results shown in Fig. 2.6(a) and (b), 32 pairs of p-DBR and 12 of n-DBR with 10 nm of intermediate layer have been chosen.

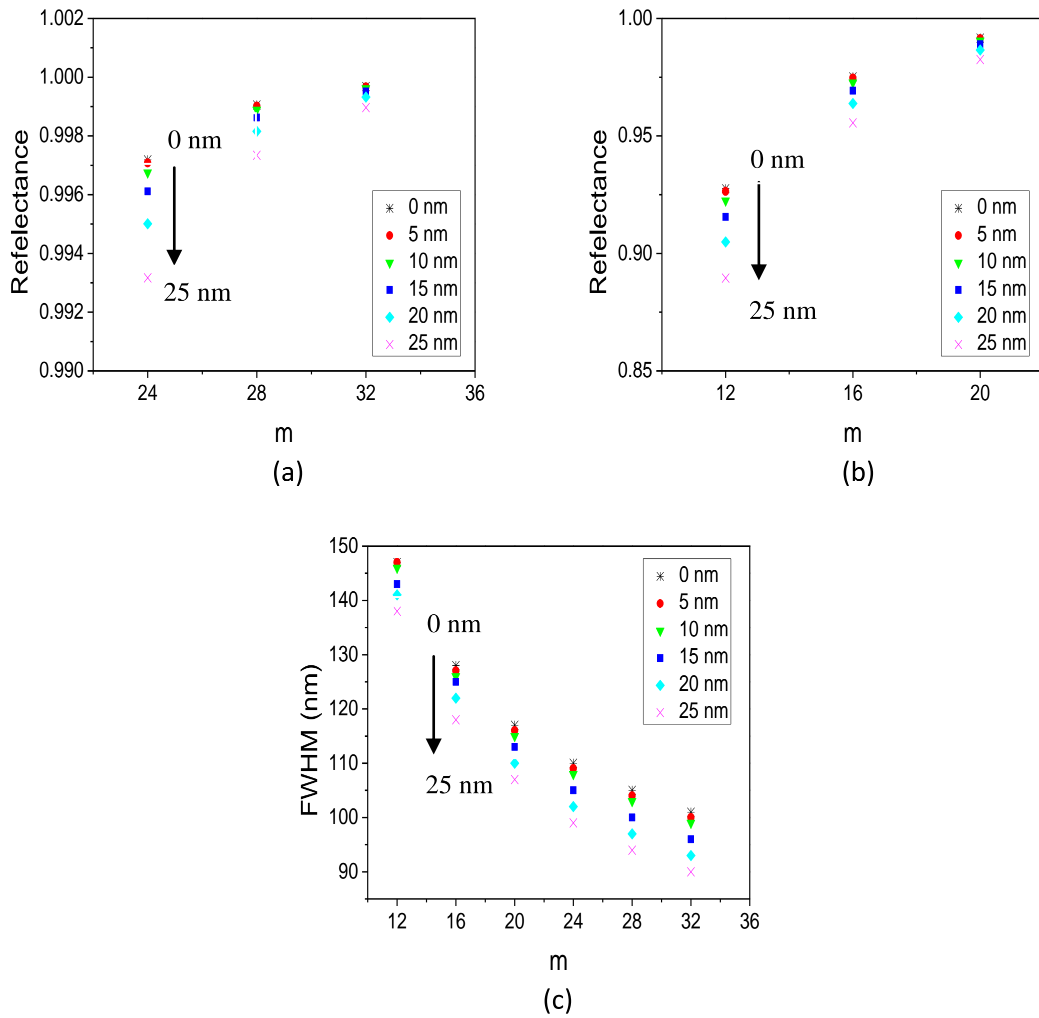


Figure 2.6 (a) and (b) Peak reflectance. (c) FWHM versus intermediate layer thickness ranging from 5nm to 25nm.

2.3 Active region

An active zone containing a periodic gain structure (PGS) is applied in the VECSEL design. In this PGS, as shown in the Fig. 2.7 below, the gain material (usually QW) has been placed at each antinode of the electric field pattern in the intracavity [18]. As the PGS is periodic, It can be obtained that the total gain material thickness $d = n \times t$ and the total cavity length $L = n \times (\lambda/2)$, where n is a integer number that represents the number of PGS periods. The advantage of using this structure is that it can increase the overlap between

the gain material and electric field pattern, and, hence, reduce the threshold current of the devices [19].

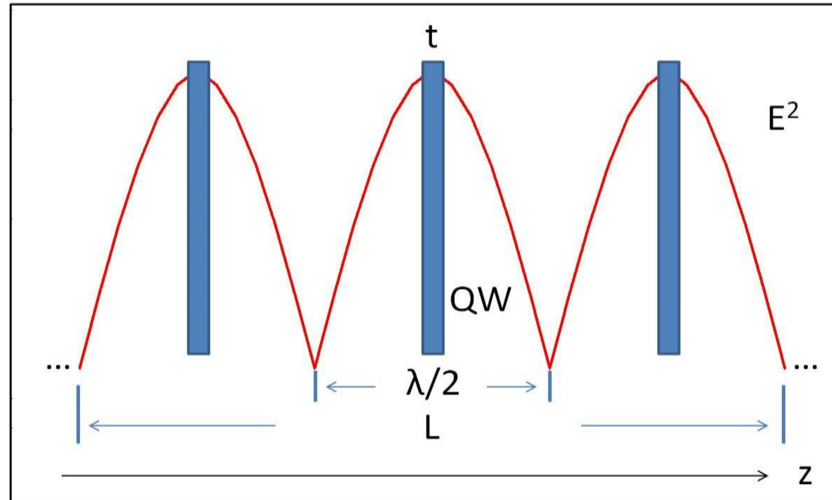


Figure 2.7 Gain material with thickness t placed at each antinodes of the electric field pattern in PGS in z direction, the total gain material thickness is d = n×t and the total cavity length L = n×(λ/2), n is a integer number, the arrow below is z direction.

In order to analyse the PGS, we start from the material gain required at the threshold g_{th} which can be expressed as [20]

$$g_{th} = \frac{1}{\Gamma}\left(\alpha_i + \frac{1}{L} ln\left(\frac{1}{\sqrt{R_1 R_2}}\right)\right), \tag{2.3}$$

where the Γ is the optical confinement factor, α_i is the internal loss and L is the cavity length. Γ is defined as the ratio between the squared electric field in the active zone and total squared electric field [21]. As the device is a three dimensional structure, Γ equals to $\Gamma_x \times \Gamma_y \times \Gamma_z$ and z axis is defined parallel to the epitaxial direction. In surface-emitting laser devices the Γ_x Γ_y of the fundamental mode approaches unity. Γ_z is defined as the longitudinal confinement factor which is the longitudinal overlap between the gain medium and the field intensity in the cavity, and then the Γ_z can be expressed as [20]

$$\mathit{\Gamma}_z = \frac{\int_{active} E^2(z)dz}{\int_L \; E^2(z)\,dz}, \tag{2.4}$$

in the intracavity of EP-VECSELs [20],

$$E(z) = E_0 cos(\frac{2\pi}{\lambda} z), \tag{2.5}$$

where λ is the wavelength in vacuum, E_0 is the amplitude.

Due to the periodicity of the PGS, we can calculate Γ_z in one of the λ/2 sections. Substituting equation (2.5) into (2.4) and changing the range of integration in (2.4) yields

$$\mathit{\Gamma}_z = \frac{\frac{d}{t}\int_t \;\; cos^2(kz)\,dz}{\frac{L}{\lambda/_2}\int_{\lambda/_2} cos^2(kz)\,dz}$$

$$= \frac{d}{L}\left(1 + \frac{sin\left[\pi\left(\frac{t}{\lambda/_2}\right)\right]}{\pi\left(\frac{t}{\lambda/_2}\right)}\right) \equiv \frac{d}{L}\mathit{\Gamma}_r, \tag{2.6}$$

where Γ_r is defined as the relative confinement factor.

From Fig. 2.7 it can be seen that the thickness of the gain region can be changed from 0 to λ/2, and then the corresponding Γ_r value can be in the range from 2 to 1. In the case of Γ_r equals 1 when t = λ /2 meaning a continuous gain region is used in the cavity.

From the previous definition, we have d = n×t and L = n×(λ/2) for the whole intracavity. Thus it can be obtained [20]

$$\frac{d}{t} = \frac{L}{\lambda/2}. \tag{2.7}$$

Then the equation (2.6) can be expressed as:

$$\Gamma_r = 1 + \frac{\sin\left(\pi\frac{d}{L}\right)}{\pi\frac{d}{L}}. \tag{2.8}$$

Equation 2.8 illustrates that with the same total thickness of the gain medium; the overlap between gain material and field intensity can be doubled by dividing the gain medium into several segments with same thickness and placing them at the each antinode of electric field pattern. As a factor of two can be achieved for the optical confinement factor Γ_z, the threshold material gain in equation (2.1) can be reduced by a factor of two for PGS [20].

Fig. 2.8 shows a schematic diagram of the intracavity structure used in this thesis. The cavity has a length of 1.5 periods of standing wave; thus two groups of three $In_{0.15}Ga_{0.85}As$ QWs can be placed at each of the antinodes of the electric field pattern in the intracavity. The QWs each have a thickness of 8 nm sandwiched by $GaAs_{0.9}P_{0.1}$ barrier layer in order to achieve a balance of compressive strain [22].

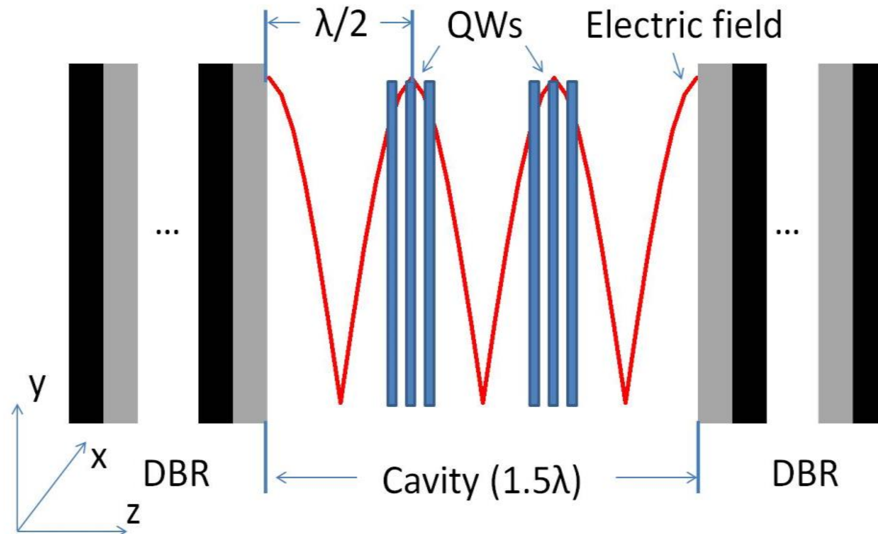


Figure 2.8 Schematic diagram of cavity design with periodic gain structure (PGS) placed between two DBR for 980 nm substrate emitting EP-VECSELs.

In this case, multiple QWs are placed in one antinode of the electric field pattern. In this case, we can still get an increase of about 1.8 for relative confinement factor Γ_r [23]. Hence, devices with both higher gain and lower threshold gain can be achieved by using the PGS.

2.4 Resonant cavity wavelength

In EP-VECSELs, the intracavity is sandwiched between the two highly reflective DBRs and those two DBRs create a cavity that can resonate at a specific wavelength. As this resonant wavelength determines the emission wavelength of the device [24], it is important to study the factors effecting the resonant wavelength.

As the true layer thickness and alloy composition (if not a binary) of epitaxial laser structures are always slightly different compared to the designed thickness due to unavoidable growth errors. Therefore, thicknesses of the DBR and cavity layers are factors that can affect the resonant wavelength. It

is necessary to analyse the different epitaxial layer thickness variation on the reflectance spectra to feed back to the growth process.

The structure contains 12 and 32 pairs of DBR at two side of the intracavity. Fig. 2.9(a) shows the reflectance spectra with growth errors in the DBR alone (i.e. the cavity is of constant thickness) with thickness variation in a range from -5% to +5%. Fig. 2.9(b) shows the corresponding cavity resonant wavelength shift rate which is 6.8 nm/%. Fig. 2.9(c) plots the reflectance spectra with constant DBR thicknesses but on error in cavity layer thickness from -5% to +5% and (d) is the corresponding cavity resonant wavelength shift rate in (c) which is 3.12 nm/%. This result indicates that growth errors of the structure will be twice as important with regard to the cavity resonant wavelength due to the operation of the DBR. Thus, a good control of the DBR layer thickness during the epitaxial process is critical for the achieving the desired wafer characteristics. On the other hand, after the wafer epitaxial process, its cavity resonant wavelength can be measured in order to estimate and compensate for any the growth error.

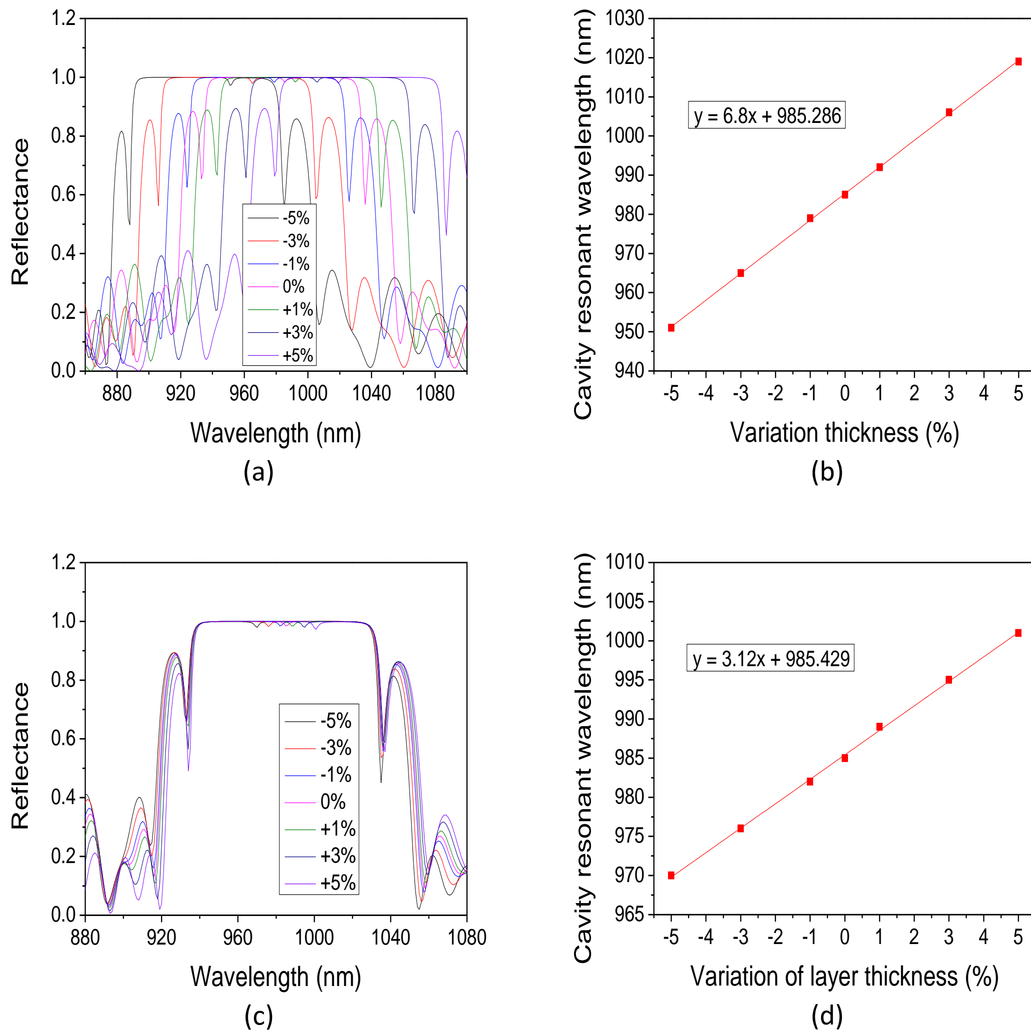


Figure 2.9 Reflectance spectra versus DBR and cavity layer thickness growth errors ranging from -5% to +5%: (a) Reflectance spectra versus DBR layer thickness growth errors. (b) Corresponding cavity resonant wavelengths shift rate in (a). (c) Reflectance spectra versus cavity layer thickness growth errors. (d) Corresponding cavity resonant wavelengths shift rate in (c).

On the other hand, it is worth investigating the effect of the number of pairs of n- and p-doped DBRs on the reflectance spectra. Fig. 2.10 shows the dependence of the reflectance spectra versus the number of n-doped DBR pairs whilst keeping the p-doped DBR pairs fixed at 32 by using CAMFR software. As it can be seen, the reflectance spectra are almost constant while the numbers of n-doped pairs increase from 4 to 28. Both the reflectance stopband width and the resonant wavelength of the spectra are independent

with number of n-DBR pairs in this case. It indicates that a ~100% mirror (the p-DBR) will determine the cavity reflectance curve no matter the number of n-DBR pairs at other side of the cavity. As the high reflectance p-DBR is growth at the top of the wafer, reflectivity measurement cannot show any growth error on the number of n-DBR pairs. Therefore, the number of p-DBR pairs should be reduced in order to see the change of reflectance spectra.

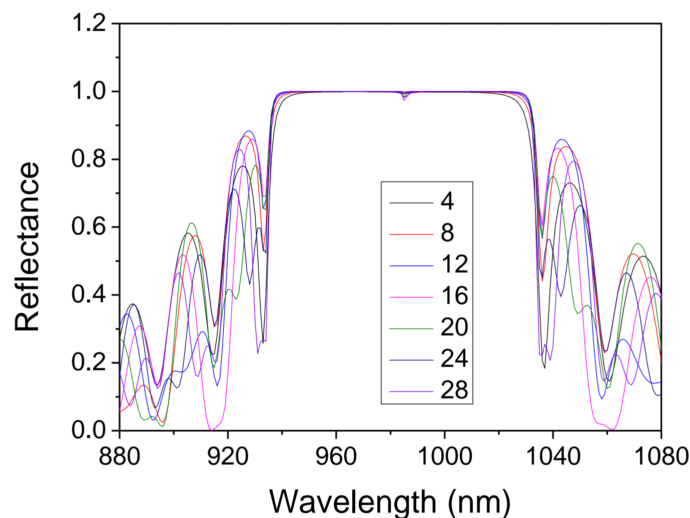


Figure 2.10 Reflectance spectra of the device with 32 pairs of p-DBR versus the number of n-DBR pairs in the range from 4 to 28.

Fig. 2.11(a) shows the reflectance spectra dependence on the number of p-DBR pairs with a fixed number of 12 pairs of n-DBR. This time the reflectance spectra shape varies with the p-DBR pair number. Fig. 2.11(b) plots the corresponding reflectance at cavity resonant wavelength versus p-DBR pairs.

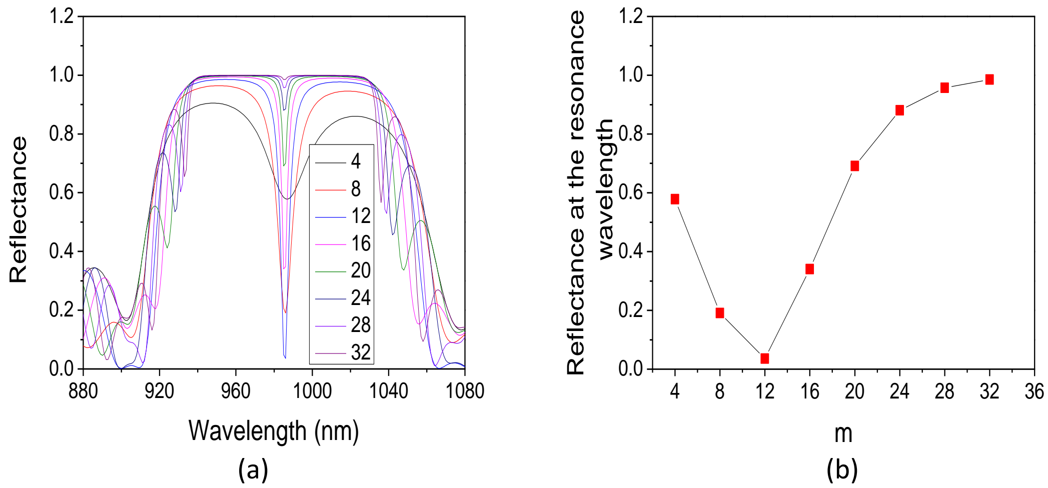


Figure 2.11 (a) Reflectance spectra of the device with 12 pairs of n-DBR versus the number of p-DBR pairs in the range from 4 to 32. (b) Reflectance at cavity resonant wavelength versus number of p-DBR pairs.

It can be seen from Fig. 2.11 that the cavity reflectance curve achieves a minimum value at the resonant wavelength when the number of p-DBR and n-DBR is equal to each other. To explain this effect, let us look at the transmittance of a cavity which can be expressed as [25]:

$$T = \frac{T_1 T_2}{1+R_1 R_2 - 2\sqrt{R_1 R_2}\,cos\,2\Phi}, \tag{2.9}$$

where T=1-R is the transmittance of the DBR and the Φ is the phase change which can be neglected. This equation shows that the maximum of the transmittance will be achieved when the two DBR have same number of pairs:

$$T_{max} = \frac{T_1 T_2}{(1-\sqrt{R_1 R_2})^2}. \tag{2.10}$$

Therefore, the minimum value of DBR reflectance is obtained when both DBRs have 12 pairs. Fig. 2.11 also indicates that in order to give the wafer characteristic measurement on the number of n-DBR pairs, the two DBRs

should have the same numbers of pairs as the reflectance spectra show the most sensitivity to the number of DBR pairs. A 12 p-DBR, 12 n-DBR test structure is highlighted as being optimal in developing 980 nm GaAs, InGaAs, AlGaAs VCSELs and VECSELs.

2.5 Final design of the structure

The final semiconductor chip structure for the substrate-emitting EP-VECSEL with etched trench is designed taking into account all the design conclusions drawn above. This laser structure has been manufactured at the University of Sheffield and its schematic diagram is shown Fig. 2.12 [26-27].

From top to bottom, the top layer is a layer of silicon nitride deposited on the GaAs substrate that acts as an AR coating to reduce the reflection at the semiconductor-air interface. The n-side InGe/Au contact layer is fabricated around the AR-coated area leaving a 5-μm-wide gap of un-coated material between them. The GaAs substrate layer is used as the current spreading layer with a thickness of 100 μm. It is n-doped at 1.5×10^{17} cm^{-3} to avoid high free carrier absorption loss whilst providing a low resistance.

The n-doped and p-doped DBRs with the intracavity between them are situated beneath the GaAs current spreading region. The top n-DBR contains 12 pairs of $Al_{0.8}Ga_{0.2}As$/GaAs with quarter-wave length to provide a reflectivity of 90%. The bottom p-DBR contains 32 pairs and provides a reflectance close to unity. A 10 nm $Al_{0.47}Ga_{0.53}As$ intermediate layer is used in both of them. The active zone inside the cavity contains two groups of $In_{0.15}Ga_{0.85}As$ quantum

wells of an 8 nm thickness placed at the antinodes of the electric field pattern and $GaAs_{0.9}P_{0.1}$ barrier layers between them to provide strain compensation.

A trench is etched in the p-DBR region to confine carriers in the transverse plane across the device to enforce a uniform gain distribution across the device. A layer of SiO_2 dielectric is deposited upon the trench to electrically insulate the contact from the active zone inside the trench area.

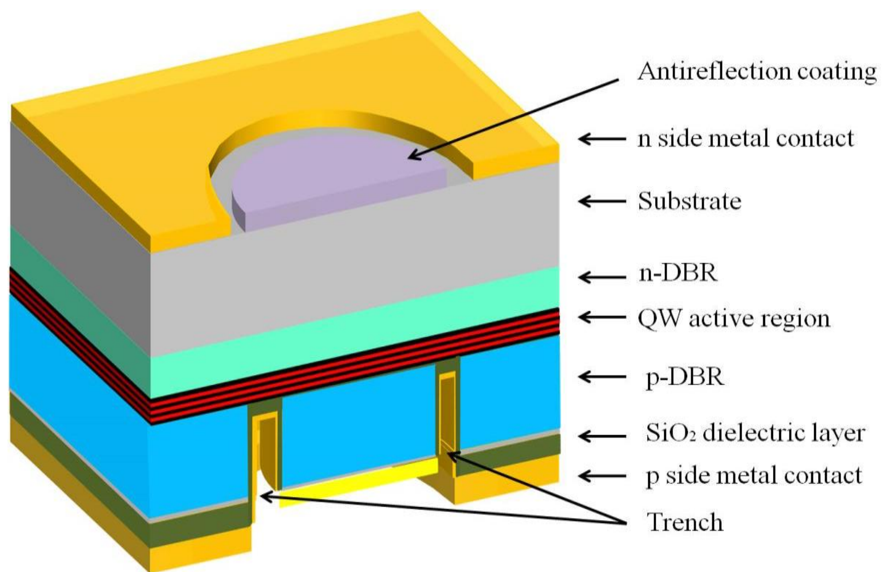


Figure 2.12 Schematic illustration of the λ = 980 nm EP-VECSEL device (not in scale).

Fig. 2.13 shows a scanning electron microscope (SEM) picture of the sample's cross section with the above design. The two stacks of DBR and intracavity are clearly observed. In the next chapter, the fabrication process based on this semiconductor chip structure to make working EP-VECSELs will be discussed in detail.

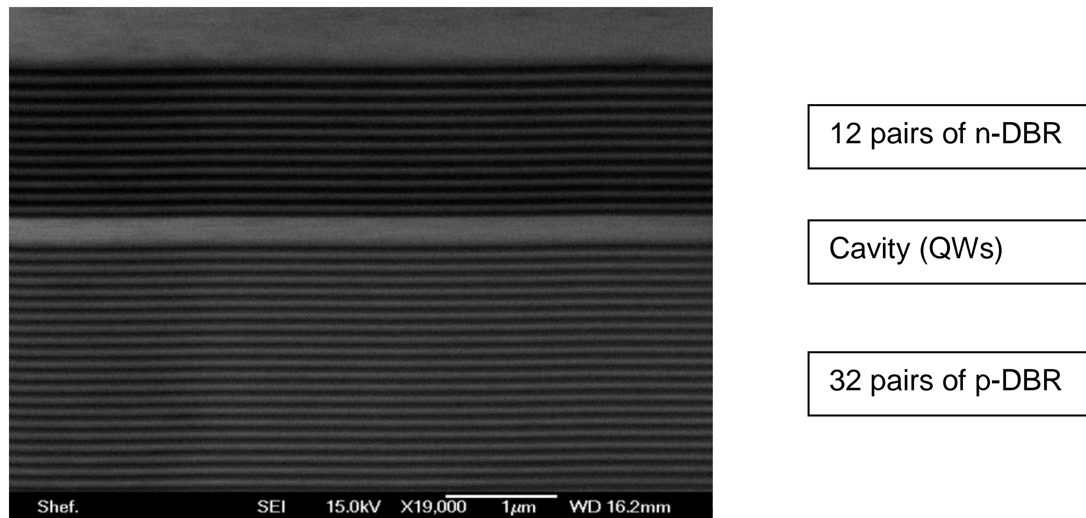


Figure 2.13 The SEM image of cross-sectional of cavity and DBR regions.

2.6 Summary

In this chapter, the main parts in the epitaxial structure design were introduced. Then the characteristic of DBR such as peak reflectivity and FWHM dependent on the number of DBR pairs was investigated using the transfer matrix method which was implemented using CAMFR software.

Results have shown that a 10 nm thick of $Al_{0.47}Ga0_{.53}As$ intermediate layer between each of DBR material should be inserted to reduce the series resistance in the DBR whilst maintaining its optical properties. In the intracavity, the PGS was applied. It has been shown that three QWs as a group placed at the antinodes of the electric field pattern can reduce the threshold gain up to 1.8 times while provide more gain in this design.

Results also have shown that the thickness of epitaxial layers should be controlled carefully during the epitaxial process. Shifts in the cavity wavelength are more sensitive to change in the DBR thickness than the cavity itself. The devices structure with different numbers of n-and p-DBR pairs were

modelled in order to investigate their effects on the reflectance spectra. Result shows that reflectance spectra can be obtained a maximum different at centre wavelength when n and p DBR have the same pairs. This can be applied in future wafer characterisation techniques, such as detuning measurement which will be discussed in later chapters.

Reference

[1] M. Kuznetsov, F. Hakimi, R. Sprague, and A. and Mooradian, “High-Power (>0.5-W CW) Diode-Pumped Vertical-External-Cavity Surface-Emitting Semiconductor Lasers with Circular TEM00 Beams,” *IEEE Photonics Technol. Lett.*, vol. 5, no. 3, pp. 561–573, 1999.

[2] M. Jacquemet, M. Domenech, G. Lucas-Leclin, P. Georges, J. Dion, M. Strassner, I. Sagnes, and a. Garnache, “Single-frequency cw vertical external cavity surface emitting semiconductor laser at 1003 nm and 501 nm by intracavity frequency doubling,” *Appl. Phys. B Lasers Opt.*, vol. 86, no. 3, pp. 503–510, 2007.

[3] H. Dyball, “New high for quantum dot VECSELs,” *Electron. Lett.*, vol. 46, no. 12, p. 807, 2010.

[4] O. G. Okhotnikov, *Semiconductor Disk Lasers: Physics and Technology*. Weinheim: Wiley-VCH Verlag GmbH & Co. KGaA, 2010.

[5] Y. Barbarin, M. Hoffmann, W. P. Pallmann, I. Dahhan, P. Kreuter, M. Miller, J. Baier, H. Moench, M. Golling, S. Thomas, B. Witzigmann, and U. and Keller, “Electrically Pumped Vertical External Cavity Surface Emitting Lasers Suitable for Passive Modelocking,” *IEEE J. Sel. Top. QUANTUM Electron.*, vol. 17, no. 6, pp. 1779–1786, 2011.

[6] K. Kojima, R. A. Morgan, T. Mullaly, G. D. Guth, M. W. Focht, R. E. Leibenguth, and M. T. and Asom, “Reduction of p-doped mirror electrical resistance of GaAs / AlGaAs vertical-cavity surface-emitting lasers by delta doping,” *Electron. Lett.*, vol. 29, no. 20, pp. 1771–1772, 1993.

[7] R. L. Thornton, R. D. Burnham, and W. Streifer, “High reflectivity GaAs-AlGaAs mirrors fabricated by metalorganic chemical vapor deposition,” *Appl. Phys. Lett.*, vol. 45, no. 10, p. 1028, 1984.

[8] L. . Brovelli and U. Keller, “Simple analytical expressions for the reflectivity and the penetration depth of a Bragg mirror between arbitrary media,” *Opt. Commun.*

[9] H. Kwong, H. Choy, and A. C. Smith, “Design and Fabrication of Distributed Bragg Reflectors for Vertical-Cavity Surface-Emitting Lasers,” 1998.

[10] P. Bienstman, “CAMFR manual v1.3.” pp. 1–70.

[11] M.Born and E. Wolf, *Principles of Optics*. 1986.

[12] H.E.Li K.Iga, *Vertical-Cavity Surface-Emitting Laser Devices*. Springer-Verlag Berlin Heidelberg GmbH, 2003.

[13] A. N. Zhiming M. Wang, *Nanoscale Photonics and Optoelectronics*. Springer Science+Business Media, 2010.

[14] G. W. Yoffe, "Rectification in heavily doped p-type GaAs/AlAs heterojunctions," *J. Appl. Phys.*, vol. 70, no. 2, pp. 1081–1083, 1991.

[15] M. Hong, J. P. Mannaerts, J. M. Hong, R. J. Fischer, K. Tai, J. Kwo, J. M. Vandenberg, Y. H. Wang, and J. Gamelin, "A simple way to reduce series resistance in p-doped semiconductor distributed Bragg reflectors," *J. Cryst. Growth*, vol. 111, pp. 1071–1075, 1991.

[16] K. Tai, L. Yang, Y. H. Wang, J. D. Wynn, and a. Y. Cho, "Drastic reduction of series resistance in doped semiconductor distributed Bragg reflectors for surface-emitting lasers," *Appl. Phys. Lett.*, vol. 56, no. 18, pp. 2496–2498, 1990.

[17] M. Linnik and A. Christou, "Effects of Bragg mirror interface grading and layer thickness variations on VCSEL performance at 1.55 μm," *Proc. SPIE*, vol. 4286, pp. 162–171, 2001.

[18] M. Y. a Raja, S. R. J. Brueck, M. Osinski, C. F. Schaus, J. G. McInerney, T. M. Brennan, and B. E. Hammons, "Resonant periodic gain surface-emitting semiconductor lasers," *IEEE J. Quantum Electron.*, vol. 25, no. 6, pp. 1500–1512, 1989.

[19] M. Y. a Raja, S. R. J. Brueck, M. Osiński, C. F. Schaus, J. G. McInerney, T. M. Brennan, and B. E. Hammons, "Surface-emitting, multiple quantum well GaAs/AlGaAs laser with wavelength-resonant periodic gain medium," *Appl. Phys. Lett.*, vol. 53, no. 1988, pp. 1678–1680, 1988.

[20] S. W. Corzine, R. S. Geels, J. W. Scott, R. H. Yan, and L. A. and Coldren, "Design of Fabry-Perot Surface-Emitting Lasers with a Periodic Gain Structure," *IEEE J. Quantum Electron.*, vol. 25, no. 6, pp. 1513–1524, 1989.

[21] Y. Z. Huang, Z. Pan, and R. H. Wu, "Analysis of the optical confinement factor in semiconductor lasers," *J. Appl. Phys.*, vol. 79, no. 8, pp. 3827–3830, 1996.

[22] G. Zhang and A. Ovtchinnikov, "Strain-compensated InGaAs/GaAsP/GaInAsP/GaInP quantum well lasers (λ~0.98 μm) grown by gas-source molecular beam epitaxy," *Appl. Phys. Lett.*, vol. 62, no. 14, pp. 1644–1646, 1993.

[23] Rainer Michalzik, *VCSELs：Fundamentals, Technology and Applications of Vertical-Cavity Surface-Emitting Lasers*, vol. 166. Springer-Verlag Berlin Heidelberg, 2013.

[24] D. B. Young, J. W. Scott, F. H. Peters, M. G. Peters, M. L. Majewski, B. J. Thibeault, S. W. Corzine, and L. a. Coldren, “Enhanced performance of offset-gain high-barrier vertical-cavity surface-emitting lasers,” *IEEE J. Quantum Electron.*, vol. 29, no. 6, pp. 2013–2022, 1993.

[25] E.Fred Schubert, *Light Emitting Diodes*. Cambridge University Press, 2003.

[26] J. R. Orchard, D. T. D. Childs, D. Williams, L.-C. Lin, B. J. Stevens, J. S. Roberts, and R. a. Hogg, “Trade-offs in the realization of electrically pumped vertical external cavity surface emitting lasers,” *Semicond. Laser Conf. (ISLC), 2010 22nd IEEE Int.*, vol. 17, no. 6, pp. 1745–1752, 2010.

[27] X. Jin, P. Ivanov, D. T. D. Childs, N. Babazadeh, J. Orchard, B. Stevens and R.A. Hogg, “Optimisation of Fundamental Transverse Mode Output in Electrically Pumped Vertical External Cavity Surface Emitting Lasers,” *Proc SPIE*, vol. 9349, 2015.

3. Devices Fabrication Process and Improvement

3.1 Introduction

In this chapter, first the EP-VECSEL device fabrication process will be introduced in detail. Then improvements in trench etching and deposition of the silicon dioxide dielectric layer process will be discussed. Next the circular transmission line model (CTLM) measurement results are discussed with regard to optimising the annealing temperature during the process, towards realising low resistance devices.

3.2 Fabrication process

The fabrication process of EP-VECSELs will be described step by step in this section. To start with, one part of the sample (about ~1/6th of a 2 inch wafer) is cleaved from the wafer using a diamond tipped scriber. Then an optical microscope is used to check the wafer surface for defects and dirt. After that cotton buds were used to clean the excess dirt off of the wafer by using warm n-butyl acetate, acetone, and isopropyl alcohol (IPA) solution in order. This method is called a 3-stage clean and will be used in later cleaning steps, but the cotton buds are only used in this step. After each 3-stage clean the sample is checked using a microscope. This clean step is repeated until there is less than one particle per field of view on 100x magnification under the microscope. Fig. 3.1 shows an example epitaxial structure with the key

features labeled.

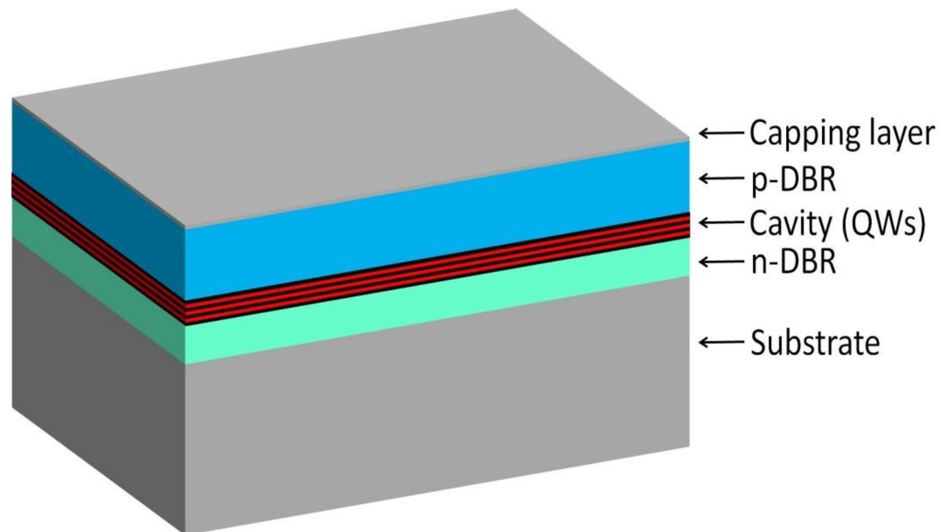
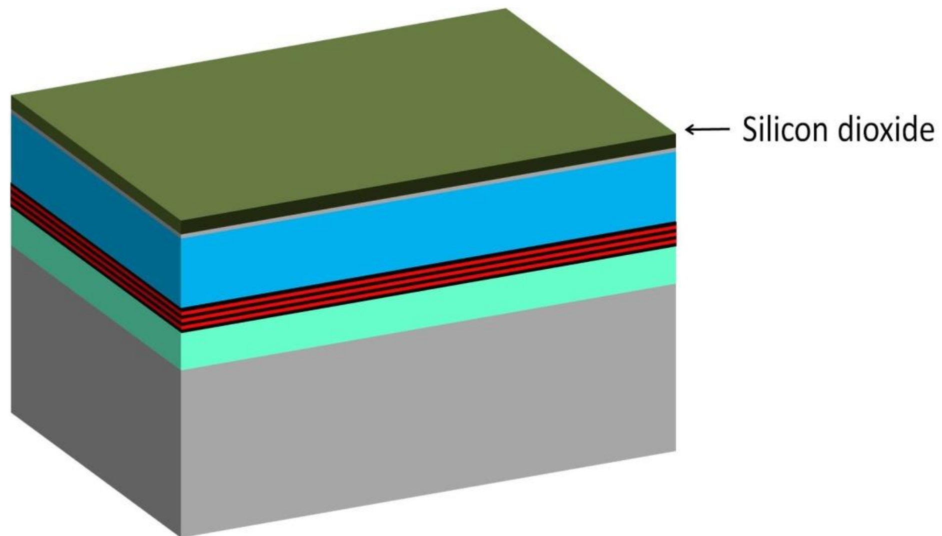


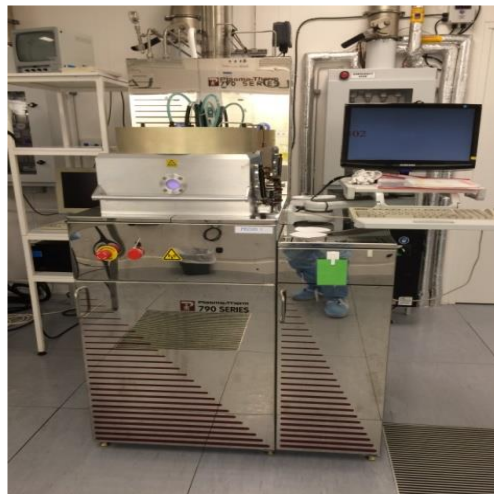
Figure 3.1 Epitaxial structure of the wafer grown by MOCVD (not to scale).

The epi-side fabrication process commenced with the deposition of a layer of silicon dioxide as a hard mask for future trench etching. The use of this hard mask can provide a straight sidewall during trench etching because photoresist may distort due to the high temperature generated during the etching process. Before the deposition of silicon dioxide the sample is cleaned in the O_2 plasma asher for 3 minutes in order to remove dust on the sample surface. Then the sample is placed in 19:1, DIW: Annular Ammonia solution for 30s to remove the surface oxide, then rinsed in DI water and blown dry using the nitrogen blow gun. The sample is now clean and ready for the oxide deposition.

Plasma-enhanced chemical vapour deposition (PECVD) was used to deposit ~ 400 nm thick silicon dioxide on the epi-side (p-doped). This is shown schematically in Fig. 3.2(a). The PECVD in our cleanroom is shown in Fig. 3.2(b). In order to make sure the deposited silicon dioxide is without impurities, a clean and preparation step is needed due to other unwanted materials that may be left in the chamber by other deposition recipes run previously.



(a)



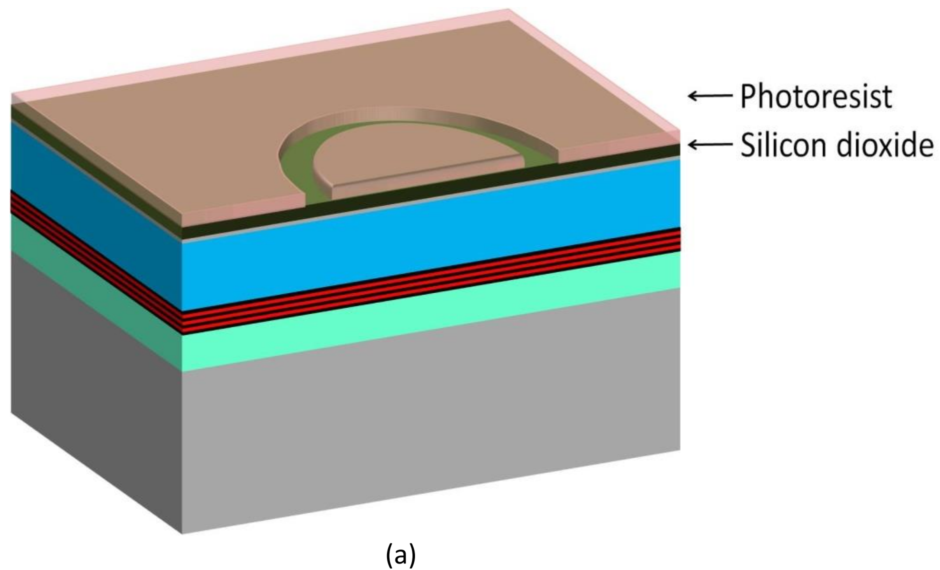
(b)

Figure 3.2 (a) Deposition of silicon dioxide by PECVD. (b) PECVD in the cleanroom of the University of Sheffield.

After silicon dioxide deposition the next step was photolithography to define the hard mask pattern. This photoresist pattern is shown in Fig. 3.3(a). First a 3-stage clean was used and then blown dry, but in order to make sure that no residual solvent is left on the sample surface, the sample needs to be placed on hotplate at 100 ^{o}C for 1 minute to dry the sample surface. The sample was then put on the vacuum chuck of the spinner by sticking on to a piece of blue tacky paper and spun at 4000 rpm. A nitrogen blow gun was used to clean any dirt and residual particle from the surface and then the sample is covered

with hexamethyl disilizane (HMDS) which is an adhesion promoter for photoresist to ensure good adhesion on the silicon dioxide surface. The next step was to spin photoresist (SPR350) on the sample. Once deposited on the sample the sample is spun for another 30 seconds at 4000 rpm in order to get the required deposition thickness across the wafer surface. After that the sample was baked on the hotplate at 100 ^{o}C for another 1 minute to drive off the solvent from the photoresist leaving a firm layer of photoresist. However spinning the sample on spinner also causes an edge bead which means a greater thickness of photoresist at the edges of the wafer. A scrap wafer was used to cover the wafer and expose the edges to UV light. This exposure time should be 4-5 times longer than the standard exposure time for that photoresist in order to remove all the resist at the edges. After this the sample is developed in MF26a developer for 1 minute, then rinsed in DI water and dried.

The trench etch mask was put into the mask aligner and the sample loaded into the aligner. After the sample was aligned it can then be exposed to UV light with a controlled exposure time. Once exposed the sample is then developed for 1 minute, rinsed in DI water and blown dry. The exposure result and alignment accuracy of the sample was checked under the optical microscope. There must be no photoresist left in the trenches and the alignment marks on the sample should be clear. Fig. 3.3(b) shows the mask aligner used in the University of Sheffield.



(a)

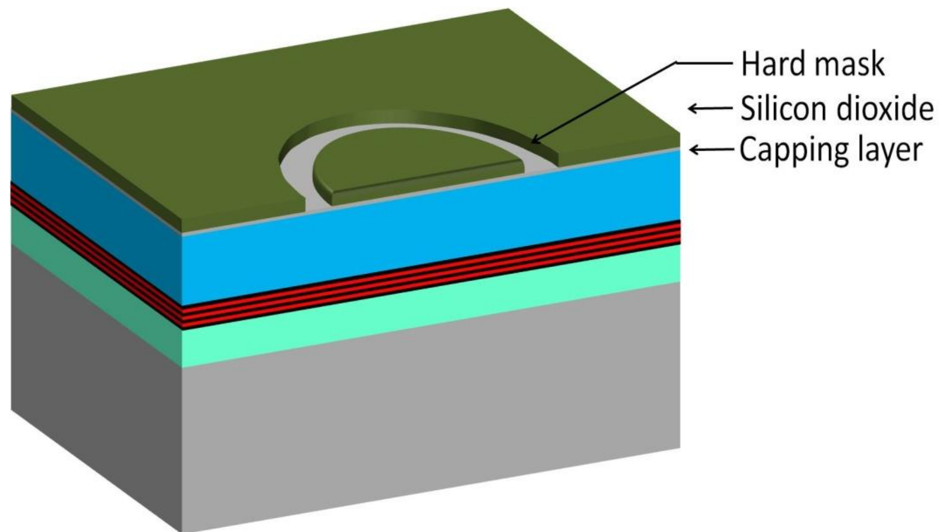
(b)

Figure 3.3 (a) The hard mask pattern defined by the photoresist. (b) Mask aligner in the cleanroom of the University of Sheffield.

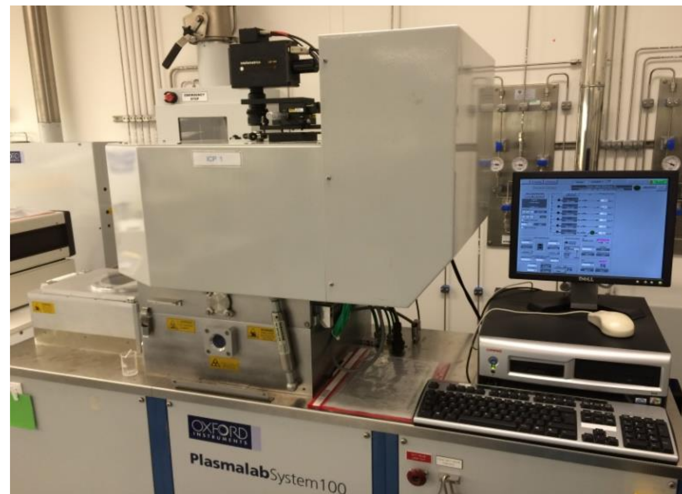
The next step was using inductively coupled plasma (ICP) etching to transfer the trench pattern from the photoresist to the dielectric layer which can be seen in the Fig. 3.4(a), with the photo of ICP used in the cleanroom in Fig. 3.4(b). Firstly the ICP was prepared using the cleaning programme for 10 minutes and then another 10 minutes to run the etch programme without a sample for preparation. After that the sample was put into the chamber with a tiny amount of fomblin oil on the back of the sample to give good heat dissipation. The etch recipe consisted of a gas flow of CHF_3 of 20 sccm and

Ar_2 of 30 sccm, with RF power of 150 W and ICP 200 W, at a pressure of 25 mT at 20°C. The etch time is dependent on the required etch depth and in this case for 400 nm of silicon dioxide is about 25 minutes. After etching an optical microscope was used to check the quality of the etching. If the trenches are clear of silicon dioxide then the photoresist can be removed.

Once the pattern was transferred to the hard mask, the sample was cleaned in the oxygen plasma Asher for around 5 minutes to make photoresist become soft while avoid heating up the sample. The sample was then put in 100°C resist stripper for 3 minutes, followed by rinsing in warm IPA and the 3-stage clean. This was repeated until no photoresist was visible in the optical microscope on the surface.



(a)



(b)

Figure 3.4 (a) Etching the silicon dioxide hard mask by ICP after photoresist was removed. (b) ICP in University of Sheffield.

Next the pattern of the silicon dioxide hard mask can be transferred to the semiconductor to form the trench by ICP etching. The etch recipe was 5:2 sccm of $SiCl_4$:Ar_2, 150 W of RF power and 250 W of ICP power, with a 8 mT chamber pressure at 20 °C. Prior to etching the dektak surface profiler was used to measure the silicon dioxide thickness across the sample. 3 to 4 points were measured on one edge to calculate the average value because the trench is too narrow to measure directly. Then a small test sample (cleaved from the sample) was etched in the ICP in order to find the correct etching

rate before the whole sample is etched. The test sample was etched for 10 minutes and then measured using the dektak surface profiler, enabling the etch time for the real sample to be calculated. When calculating this time we need to note previous result have shown the etching rate measured on the large features is slower by a factor of 0.8 in the trench area [1].

Now the main sample can be etched, using the same recipe as the test sample. Ideally the trench needs to pass through all the 32 p-DBRs which are about 5 μm thick. This trench profile is shown in the Fig. 3.5. The sample's etch depth can be measured using the dektak. After this oxygen plasma Asher and the 3 stage clean were used to clean the sample.

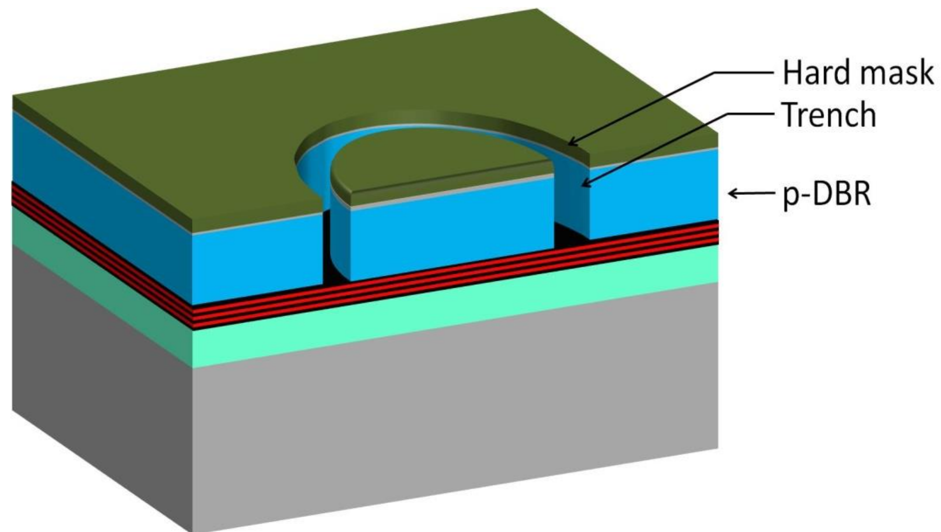


Figure 3.5 After the capping layer and p-DBR was etched by ICP.

In order to remove the hard mask silicon dioxide, the ICP is used to etch it off. The ICP was prepped as described and the etch recipe is the one described for etching silicon dioxide previously. The sample was etched for about 30 minutes. The longer etching time this time is to make sure all silicon dioxide to be removed. Post silicon dioxide etch the sample was O_2 plasma ashed for 3 minutes. The surface was checked under the microscope to make sure no

particles were left and finished with 3 stages clean. Fig. 3.6 shows the sample structure after etch and hard mask removal.

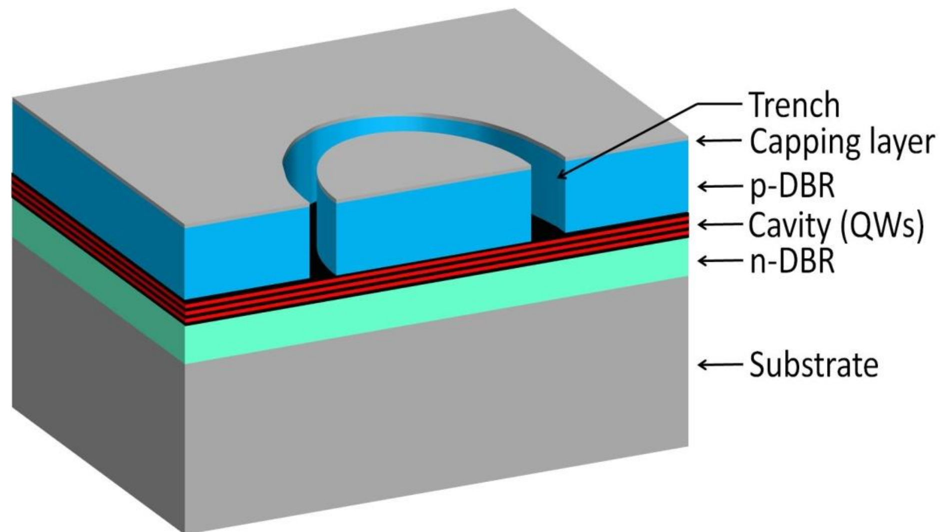


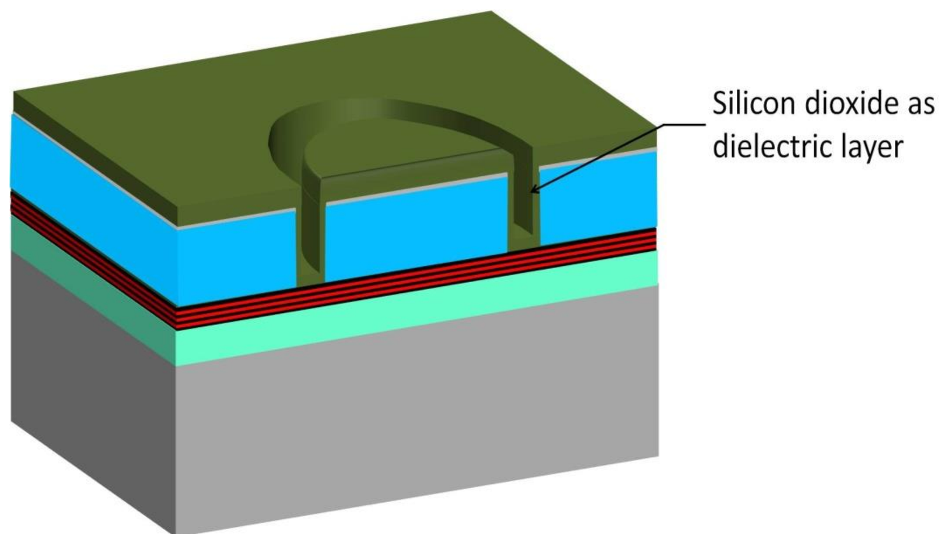
Figure 3.6 The etched device structure after hard mask removal.

The sample was then prepared for another silicon dioxide deposition in the PECVD. The sample was cleaned using a 3-stage clean. Then the sample was deoxidised using 19:1 DIW: Annular Ammonia solution for 30 seconds followed by a rinse in DI water and blown dry.

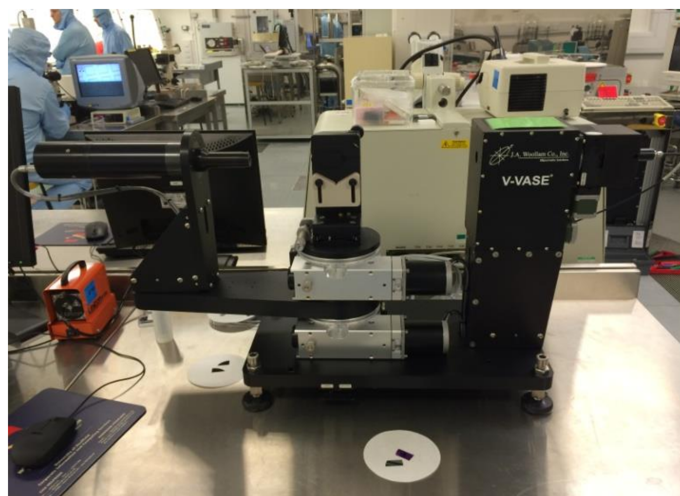
The PECVD is prepared for deposition by running the recipe to deposit silicon dioxide for 10 minutes with no sample in the chamber. The deposition rate is then calibrated by depositing silicon dioxide on a test wafer and determining the thickness of the deposited layer using an elipsometer, which is shown in Fig. 3.7(b). A light beam is incident on the sample surface which is then reflected to a detector, and the change of polarisation (which is quantified by amplitude ratio and phase between the incidences and reflected beam) can be obtained. The change of polarisation is determined by the deposited material properties such as thickness, refractive index, roughness, electrical conductivity and so on. Thus, the thickness of the deposited layer can be

calculated. This measured silicon dioxide thickness is then used to calculate the deposition rate.

Fig. 3.7(a) shows the sample structure after this deposition. I use a deposition thickness of 800 nm to avoid current leakage. I will analyse this issue in detail later in this chapter. After this the deposition quality was checked under microscope to make sure no unwanted material was deposited on the sample.



(a)



(b)

Figure 3.7 (a) A device with dielectric deposition by PECVD. (b) ellipsometer used in the cleanroom of University of Sheffield.

The following step is using photolithography to define the top window pattern. As describe previously, the samples was 3 stage cleaned and baked to remove residual solvents. HMDS and photoresist (SPR350) was spun on to sample, followed by edge bead removal. Next, the sample was put in the mask aligned and aligned accordingly. After exposure the sample was developed for 1 minute. The window pattern is shown in the Fig. 3.8. After developing the sample is checked under the optical microscope to see whether the resolution markers on the mask are exposed as required.

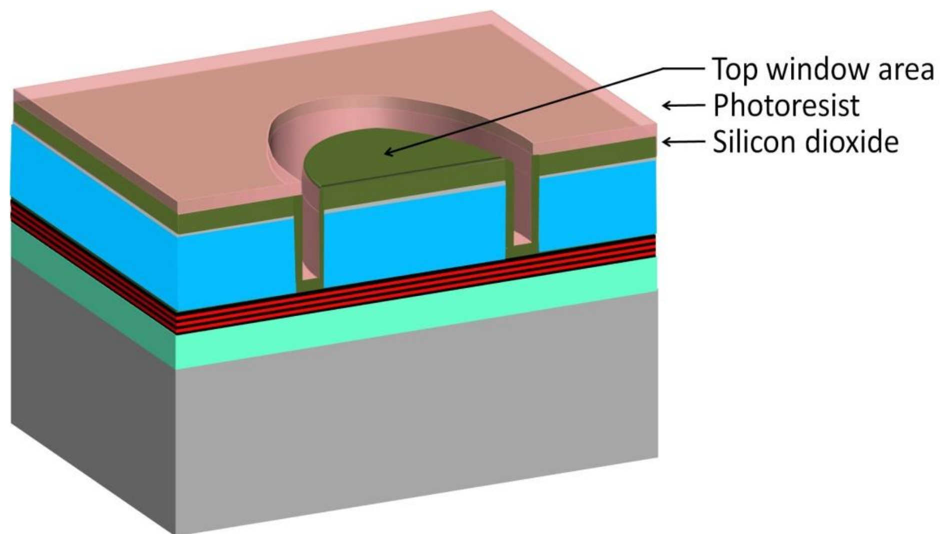
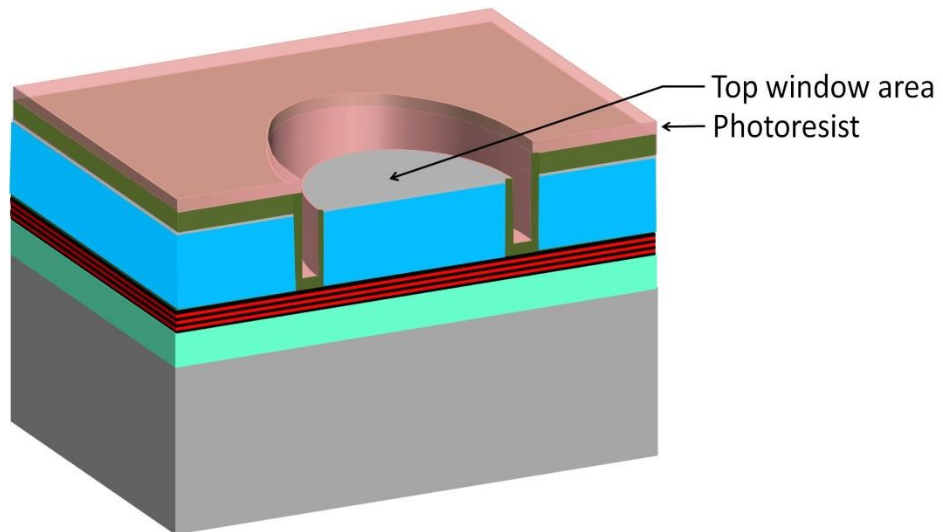
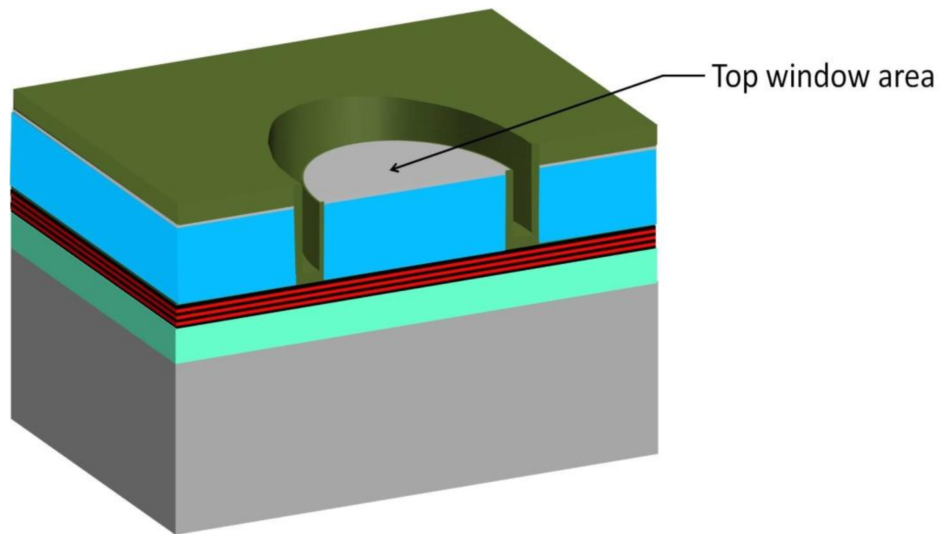


Figure 3.8 Sample after the top window pattern lithography.

The ICP was used to etch the silicon dioxide in the window region for future contact metal deposition. As before, the ICP was first cleaned and prepared for 10 minutes. Figure 3.9(a) shows the sample structure. After the etching process the etching quality was inspected. The sample was then cleaned in the O_2 Asher for 5 minutes; 3 minutes in 100°C resist stripper and 3-stage cleaned until the surface was clean and ready for next photolithography step, as shown in Fig. 3.9(b).



(a)



(b)

Figure 3.9 (a) ICP etch of the silicon dioxide window. (b) Sample with top window opened after photoresist removed.

The next photolithography step is to define the top contact pattern. This pattern is shown schematically in Fig. 3.10. The sample was cleaned for 1 minute in the O_2 Asher to clean the surface prior to metal deposition.

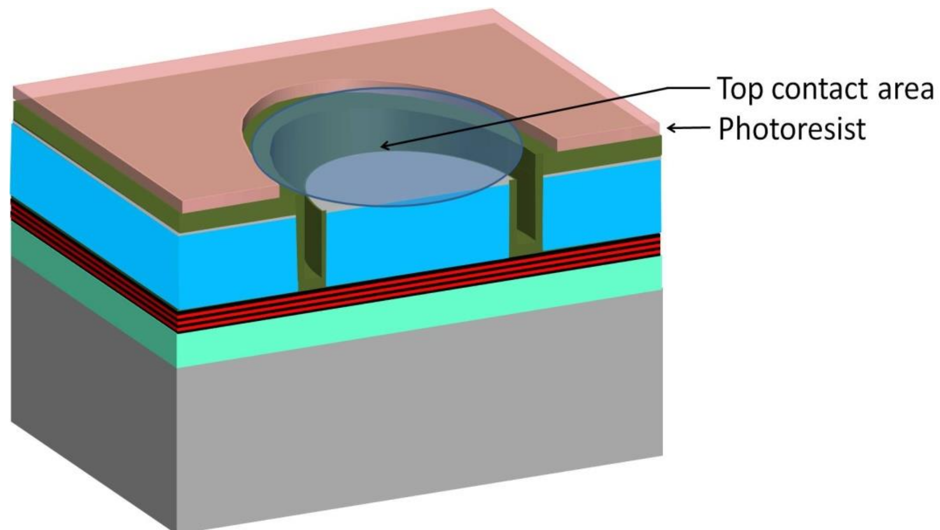


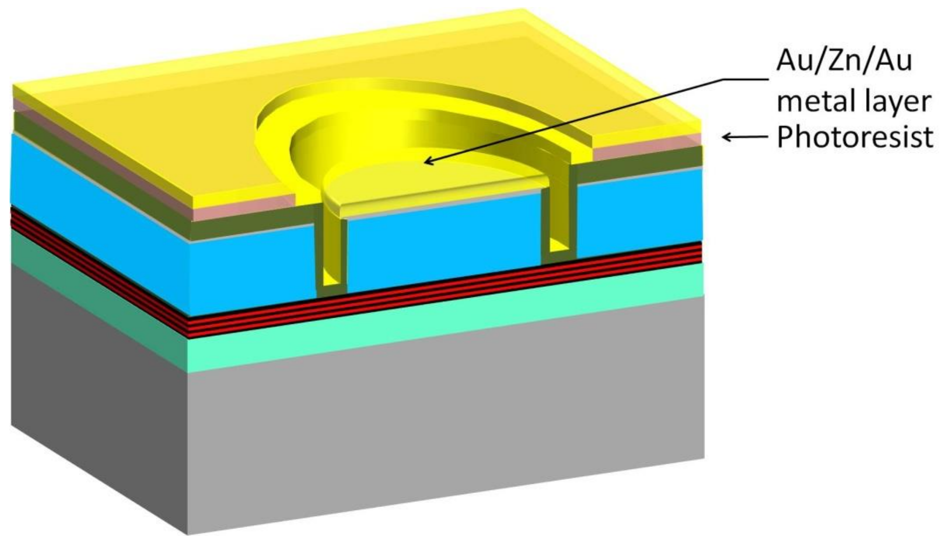
Figure 3.10 The photoresist pattern for top contact lithography.

Next, the sample should be prepared for the Au/Zn/Au metal deposition by a thermal evaporator. Tungesten coils and baskets for holding the metals to be evaporated are cleaned, along with the metals to be evaporated, by boiling in n-butyl acetate. Once clean they are mounted in the thermal evaporator. The sample is prepared using 19:1 H_2O: Annular Ammonia solution for 30 second to remove surface oxide and then loaded into the evaporator. The deposition process was not started until the pressure inside the evaporator dropped below $1.5x10^{-6}$ T. The tungsten coils may be heated by passing current through them causing the metal to evaporate. A 5 nm Au layer is deposited first to aid the adhesion of the 10 nm Zn layer. Finally a 200 nm Au layer completes the evaporation. The deposition thickness can be measured by a crystal thickness monitor. Fig. 3.11(a) depicts the structure after deposition.

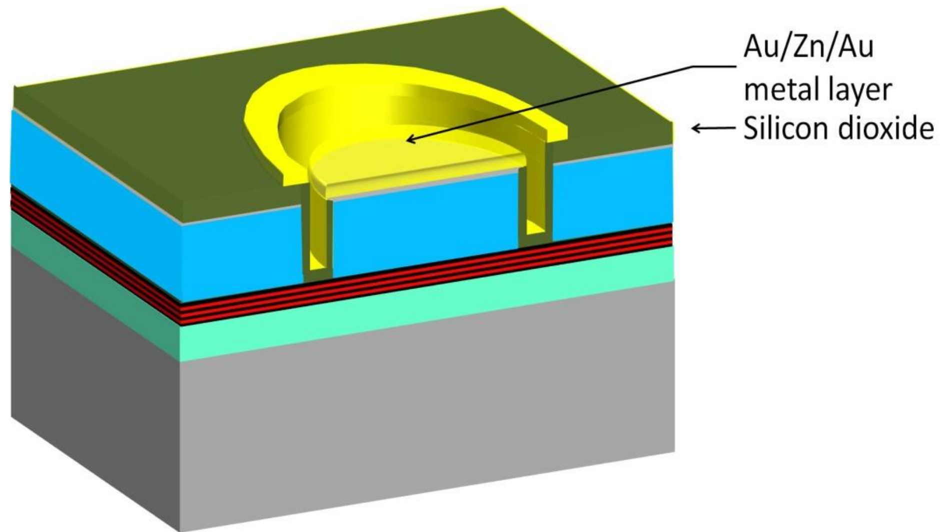
After deposition the sample was unloaded and put in acetone in order to lift off the gold. This process can be speeded up using acetone from a squeezy bottle prayed onto the sample surface to remove the photoresist. This was repeated until all the metal with photoresist beneath it was lifted off. The sample surface was checked to make sure no resist was left and then the

sample was cleaned with the 3-stage clean. The structure is shown in Fig. 3.11(b). The photo of thermal evaporator used in the University of Sheffield is shown in Fig. 3.11(c).

Then the sample was put in to the rapid thermal annealer (RTA) to anneal the contact. The annealing recipe was 360 ^{o}C for 30 seconds. Under such conditions the zinc can diffuse into the semiconductor to form a low resistance ohmic contact.



(a)



(b)

(c)

Figure 3.11 (a) Metal contact deposition by Thermal evaporator. (b) The top metal contact geometry after photoresist removal. (c) Thermal evaporator in the University of Sheffield.

The final step on the epitaxial side is to deposit a layer of Ti/Au by sputtering. A thin layer of titanium (20nm) is used to improve adhesion between the gold and silicon dioxide [2]; Fig. 3.12 illustrates the sample profile. The sample is loaded and the chamber evacuated to a pressure less than $2x10^{-6}$ T, before 20 nm of titanium and 400 nm of gold were sputtered on it.

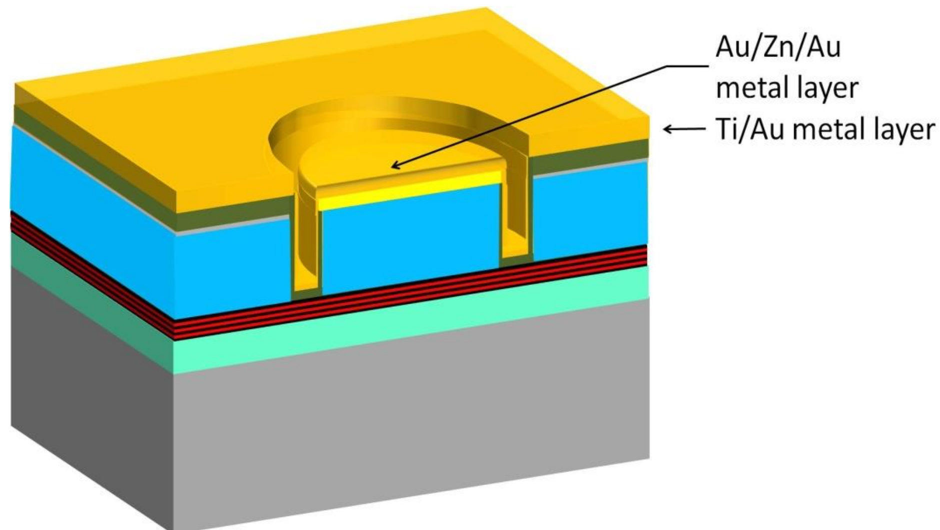


Figure 3.12 Deposition Ti/Au layer by sputter.

The sample now could be prepared to start the substrate side process. The substrate needs to be thinned from 350 μm to ~100 μm in order to reduce the free carrier absorption loss as the substrate is doped [3] and to improve the thermal performance of the device. Firstly the sample was covered by a layer of photoresist on the epi-side to protect the epi-side metal contact and then mounted on the centre of the glass polishing carrier using wax. Care is taken to ensure the sample is mounted flat to within 10 μm tolerance and three other scrap wafers were put around the sample to protect the main sample from being crushed during the thinning process.

The glass with mounted sample was placed in the polishing jig of the lapper/polisher machine. The lapping wheel rotates whilst the sample is held stationary and a 1:9 mixture of calcined aluminium oxide solution is allowed to

drip onto the lapping wheel as the grining medium. The sample thickness was checked regularly and when it reached between 90 and 110 µm it was removed from the lapper polished and cleaned using DIW.

The sample was then wet etched using CH_3COOH: HBr: $K_2Cr_2O_7$ 1:1:1, diluted 1:1 with DIW for 2.5 minutes to chemically polish the surface. The sample can then be removed from the glass carrier and 3 stage cleaned. Fig. 3.13 shows the schematic diagram of the sample structure after it was thinned.

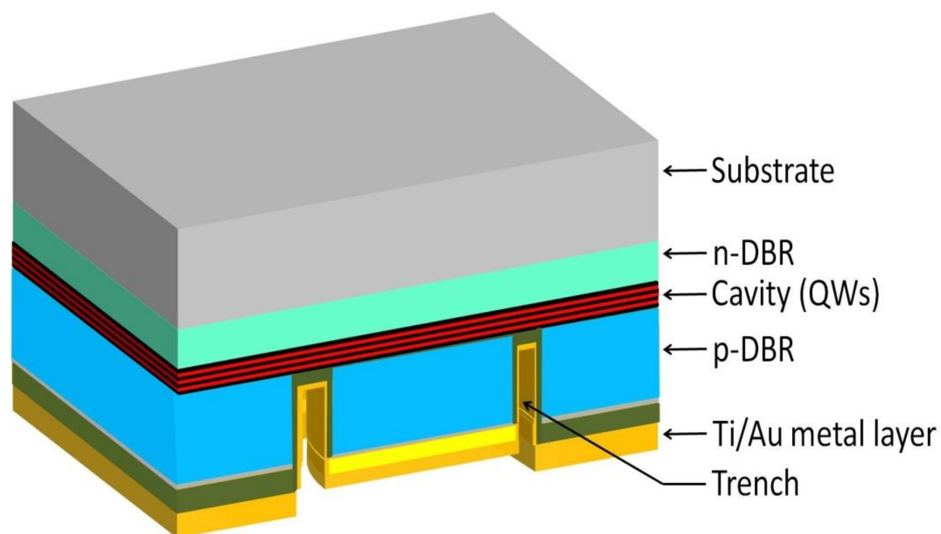


Figure 3.13 Sample after substrate thinning.

The next step is the back contact metallization photolithography. The sample was mounted on a glass slide with substrate side up using wax and a layer of BPRS100 photoresist was spun over the sample. By loading the sample into the mask aligner substrate side down it is possible to align the mask pattern to the sample, exposing and developing this leaves a pattern on the glass slide which can then be used to align the pattern on the substrate side of the sample when the sample is loaded into the mask aligner substrate side up. Fig 3.14 shows the pattern of photoresist, it is noted that this process gives the alignment between the two sides.

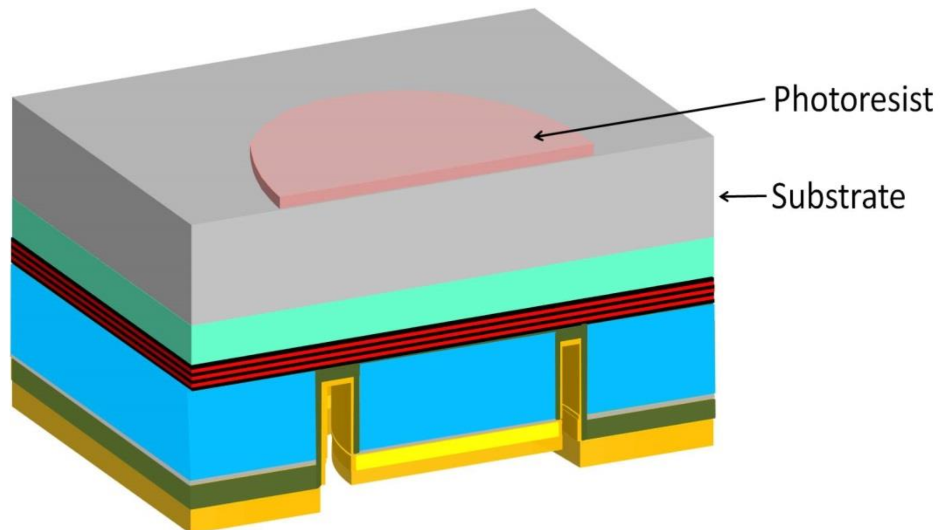


Figure 3.14 Back metal contact pattern photoresist.

The sample was prepared for evaporation as described previously. In this case the contact was 20nm InGe and then 200 nm Au. After evaporation acetone was used to lift off the Au where is not required. After a 3 stage clean the sample was loaded into the RTA for annealing at 360°C for 30 seconds. Fig. 3.15 shows the sample profile.

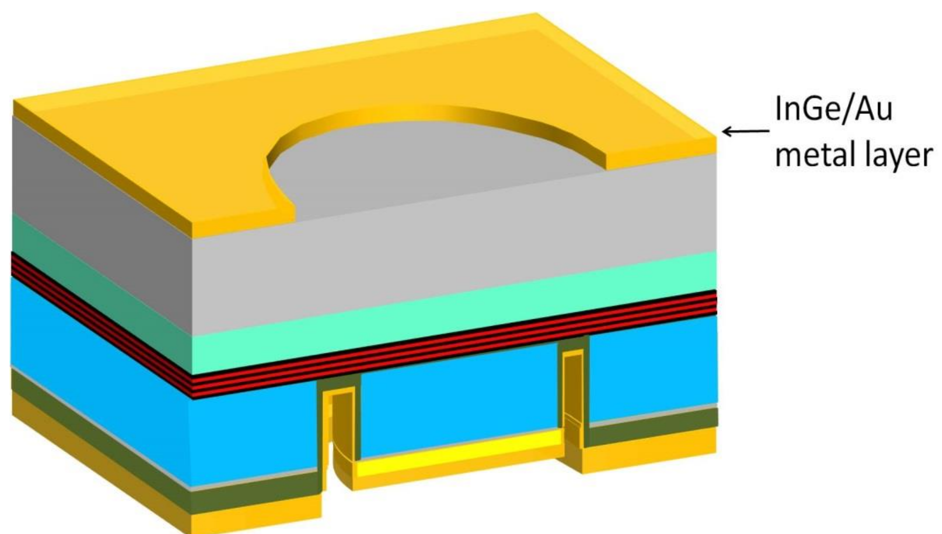


Figure 3.15 InGe/Au metal contact geometry after the photoresist removed.

The next step is to deposit a silicon nitride layer as an anti-reflective coating layer by PECVD. This anti-reflective coating layer can reduce the reflectance between the air and semiconductor to minimise coupling loss [4]. This profile

can be seen in the Fig. 3.16. Both the cleaning recipe and deposition recipe were run for 10 minutes in order to clean and prepare the PECVD, followed with a test wafer to calibrate the deposition rate. This rate was used to calculate the deposition time to deposit a silicon nitride layer with an optical thickness of a quarter of the emission wavelength.

$$t = \frac{\lambda}{4} = 127\,nm, \tag{3.1}$$

where n is the refractive index of silicon nitride which is equal to 1.93.

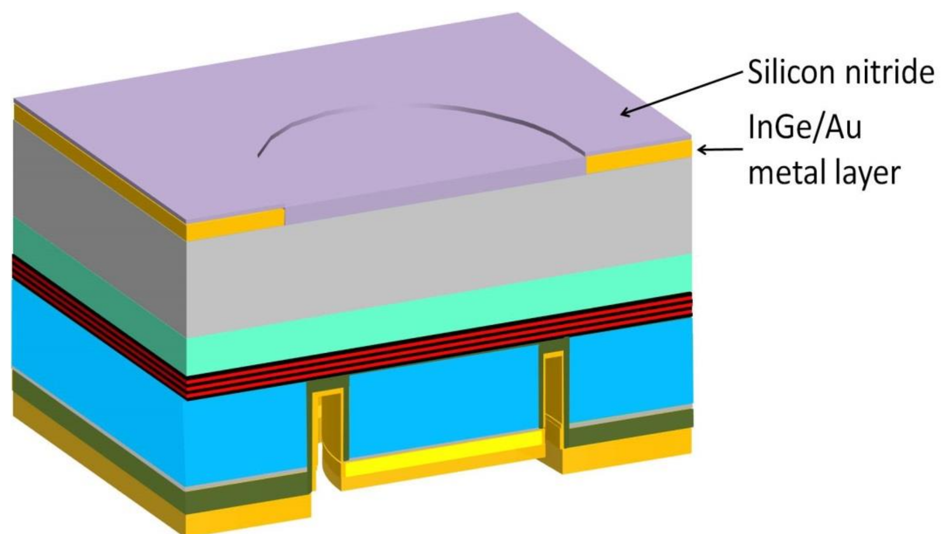


Figure 3.16 Silicon nitride deposition using PECVD.

Another photolithography step was applied to remove the silicon nitride to give access to the metal contact as shown in the Fig 3.17.

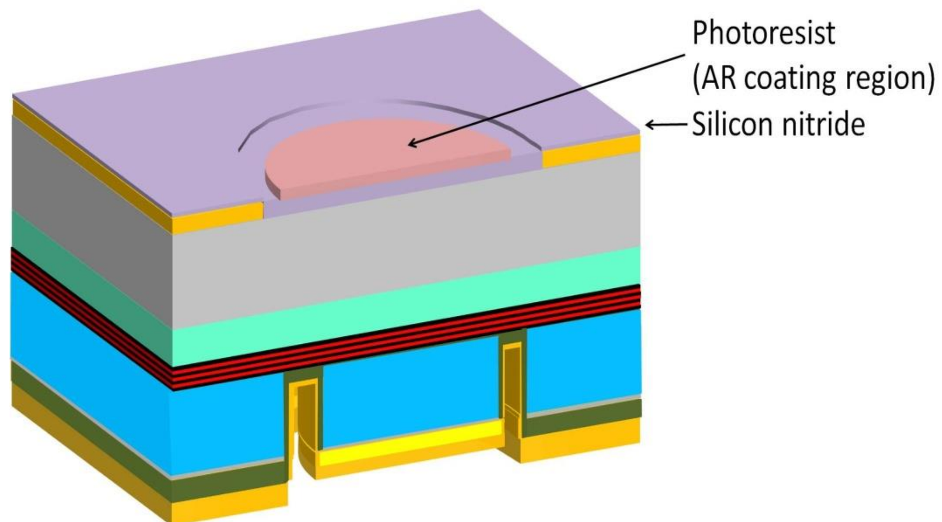


Figure 3.17 the anti-reflective coating region was protected from etching by photoresist.

The last step of the fabrication step is to remove the unwanted silicon nitride to give an anti-reflective coating pattern only on top of the aperture. Reactive-Ion Etching (RIE) was applied in this step, because metal should not be placed inside the ICP chamber. The recipe was CHF3 of 35 sccm, O_2 of 5 sccm with a pressure of 35 mT in the chamber, and RF power of 80 W. The sample was etched until the silicon nitride had cleared from the window area. The Fig. 3.18 shows the final structure in the below.

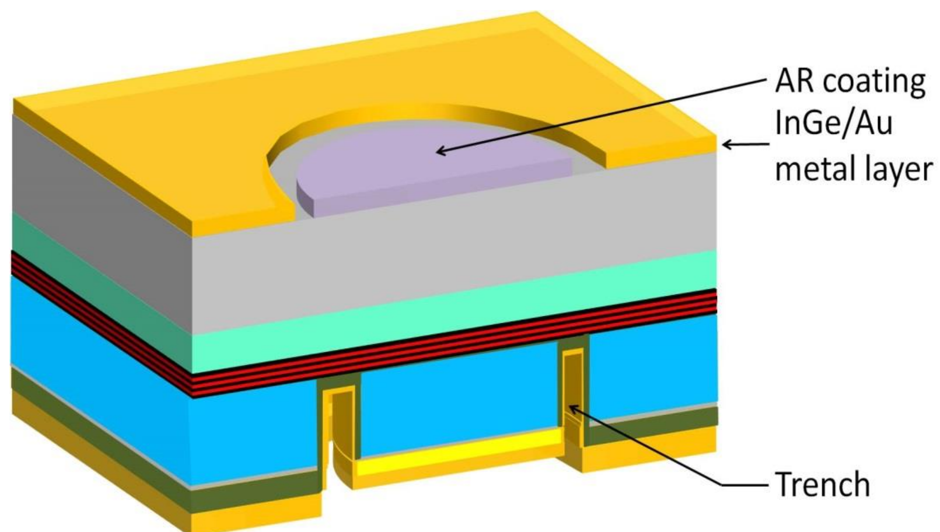


Figure 3.18 Schematic diagram of the fabricated EP-VECSEL with etched trench structure.

As shown in Fig. 3.19, individual devices were cleaved from the processed

wafer, with an individual die size of 0.5x0.5 mm. A die bonder was used to bond the device with the p-side contact to the tile using Au/Sn eutectic. Finally, four electronic connections were made at each corner of the device by gold wire ball bonder. Fig 3.20 shows the size of a die on tile compared with a 20p coin.

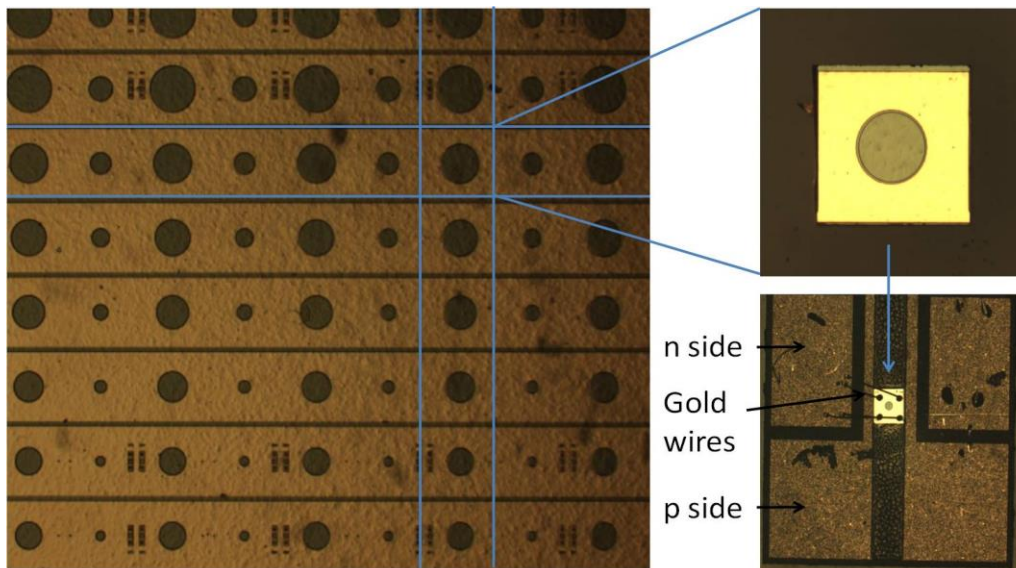
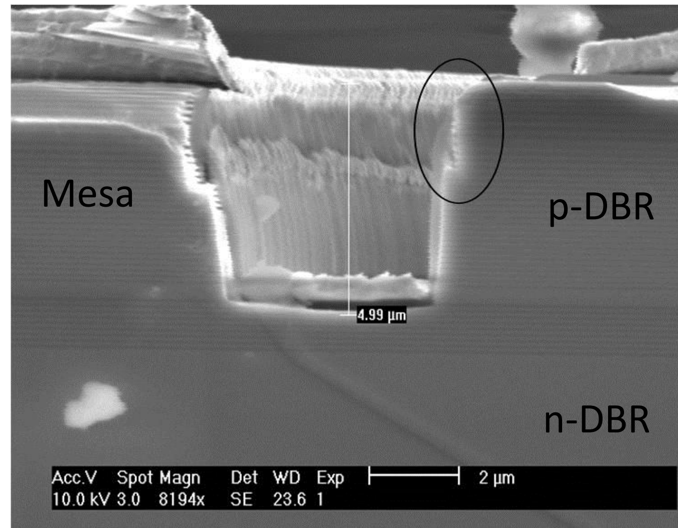


Figure 3.19 2D array of the VECSELs devices (left), on the top right is a single device after being cleaved; the right bottom is the device on a tile with four gold wires connections.

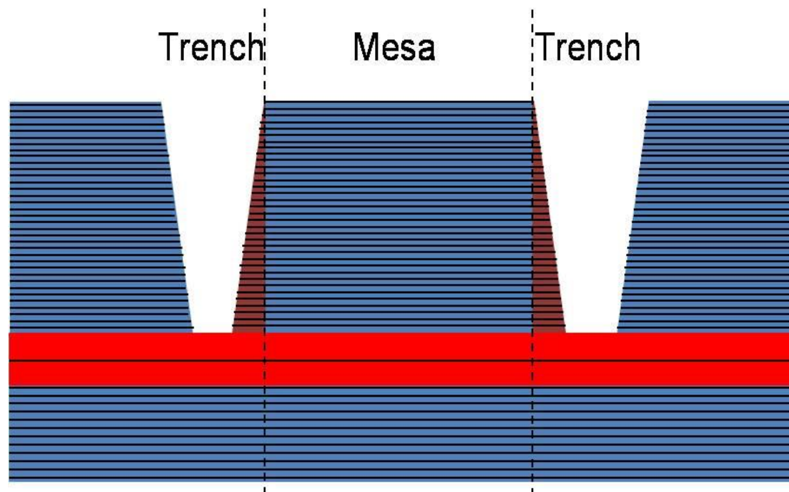
Figure 3.20 The single device on tile placed on a 20p coin.

3.3 Fabrication process improvement

In the EP-VECSEL described here, the etch profile is very important for device performance. This etched trench provides both the optical and electrical confinement. Fig. 3.21(a) shows a scanning electron microscope image of the etched trench from the original AlGaAs/GaAs etch recipe. It shows two problems for the etching, one of them is that the trench sidewall is not straight. A schematic diagram of a trench with a slope is shown in Fig. 3.21(b). The region marked in red will have fewer p-DBRs and hence will be unable to lase. These regions will however be supplied with current. They will therefore act as parasitic elements providing no lasing output, reducing the efficiency of the device. They will also contribute to Joule heating of the chip. The other problem is that the dielectric layer does not cover the whole trench, especially on the corner which is marked by a ring in Fig. 3.21(a). This is due to the dielectric layer deposition thickness being too thin. Without the full coverage of this dielectric layer, current leakage may happen in these areas. Thus, the whole active region of the chip will be driven and no lasing will occur as thermal roll-over will occur before lasing can be achieved for the whole chip. For samples suffering from this current leakage, spontaneous emission was observed from the whole of the chip, and there was no lasing. In order to produce trench with a straight sidewalls and full cover of dielectric layer, new etching recipes and new silicon dioxide deposition process is needed to be investigated.



(a)



(b)

Figure 3.21 (a) The etched trench profile with a slope form SEM, ring inside shows the not covered of dielectric layer problem. (b) Schematic diagram of trench with slope.

3.3.1 Improvement of trench etching recipe

To achieve the straight trench profile, different etch recipes were investigated. Three samples with the silicon dioxide hard mask pattern were cleaved from the same wafer and a small amount of fomblin oil was placed on the back side of the sample to conduct heat generated by etching process from sample to the carrier wafer, this also improved the uniform heat distribution across the sample and helped to keep the same etch rate.

The 32 pairs of p-DBRs plus the capping layer have a thickness of 5.2 μm. The first test sample was shallow etched approximately 1 μm (a few pairs of DBRs) using the existing GaAs etch recipe which is described in section 3.2. Figure 3.22(a) shows the SEM image of this etch profile, the trench has a slope sidewall which will deteriorate the device as discussed previously. The second test sample was etched halfway through the p-DBR by ICP (2.5 μm) as shown in Fig. 3.22(b). The upper inserted block in Fig. 3.22(b) illustrates that the sidewall of the trench is covered by a layer of material. It may part of the reaction products generated during the etching process and have not been taken out of the chamber in time. The sample was then wet etched using 1:1:1(CH3COOH, HBr and K_2Cr_2O7) etchant, but it failed to remove the deposited material and the trench become very narrow, which can be seen in the second block of the Fig. 3.22(b).

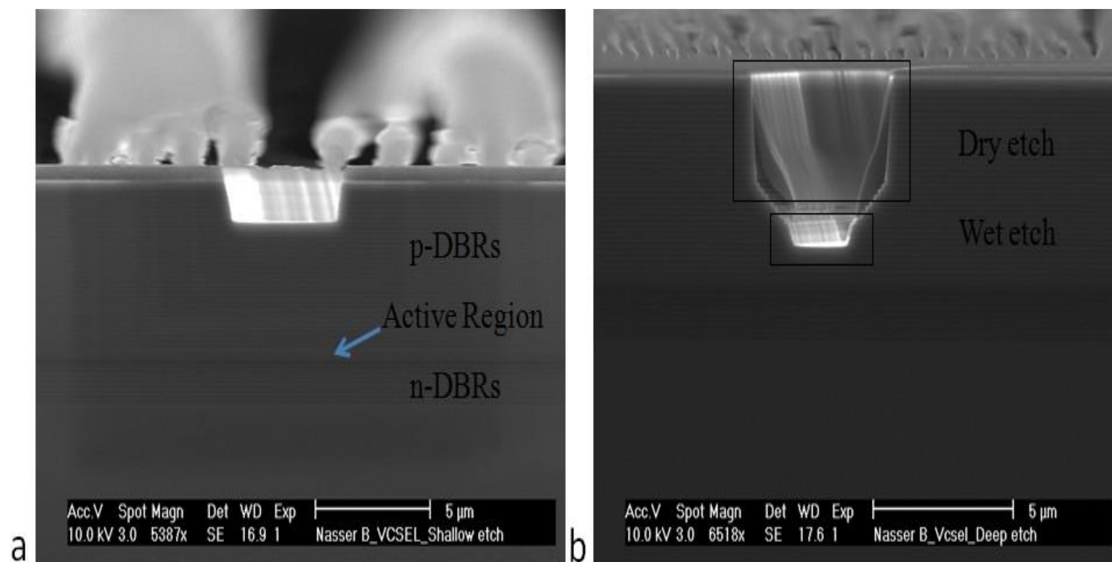


Figure 3.22 Etch profiles for differing etch depths (a) shallow etch (b) etched pass through etched halfway through the p-DBR but the profile is not as straight as expected.

The etch process needs to be modified in order to avoid the problems above. The comparisons of the main parameters between the two recipes are listed

in the table 3.1. In the ICP, the RF power is applied to the load coil to generate a electromagnet field [5]. The RF power also determines the ion bombardment energy; higher RF power will make the ion impact on the samples surface more energetic which may give a rough sidewall. In the shallow etch photo it can be seen the trench is smooth, so the RF power is kept the same. The ICP power determines the plasma density. Increasing the ICP power will generate more radicals and ions for the chemical etching in the plasma and give a higher etch rate. Increasing the pressure also gives a higher gas concentration in the chamber which means a higher etch rate. However care needs to be taken to avoid the pressure being too high because this will shorten the free path for the ions which means many more collisions will happen before the ions reach the sample thus reducing the etch rate significantly.

Old Recipe Parameters		New Recipe
RF Power	150 W	150 W
ICP Power	200 W	250 W
Set Pressure	1 mTorr	8 mTorr

Table 3.1 The comparison of the two different etch recipe.

For this new etch recipe we would expect that no etch product residues will stick on the sidewall. The third sample was etched using this new recipe to an etch depth of 4.5um. The SEM image result shows that the profile is straight and smooth for a 4.5 μm depth trench in the Fig. 3.23. Therefore, this new recipe was chosen in the future fabrication process.

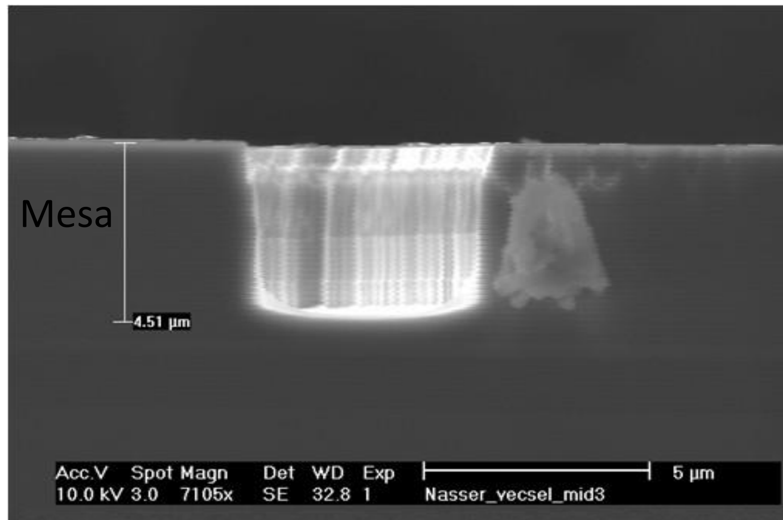


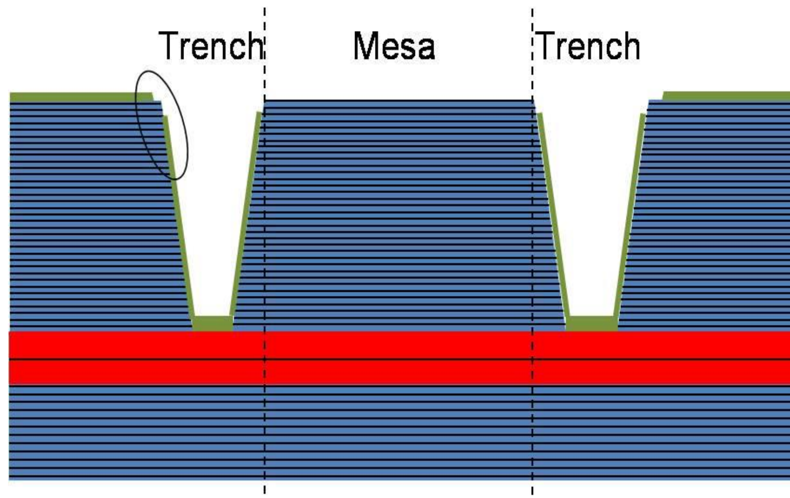
Figure 3.23 The SEM image of trench profile using the new etch recipe.

3.3.2 Improvement of silicon dioxide deposition process

Due to the non-uniform thickness of the deposited dielectric layer, a thicker layer should be deposited to avoid current leakage, especially at the corner of the trench, which is marked by an ellipse in Fig. 3.24(a). Fig. 3.21(a) indicates that a 400 nm thick of dielectric layer is not enough. A test sample was cleaved into three pieces to do the different thickness deposition with 600 nm, 800 nm and 1000 nm, respectively.

Figure 3.24 also shows the SEM images from depositing 3 thicknesses of silicon dioxide on the samples. All of the samples show no evidence of delamination. Due to the sample not being totally perpendicular to the SEM beam the measurement of the thickness is not completely accurate. However, the ratio of the side/bottom/top deposited thickness is about 0.4/0.7/1 can be seen from all the three samples in Fig 3.24. In the Fig. 3.24(b) the silicon dioxide layer follows the semiconductor profile, but it is quite thin at the corner. The samples with 800 nm of silicon dioxide in Fig. 3.24(c) and 1000 nm Fig. 3.24(d) show a better result, but as the dielectric layer must be subsequently

etched for an electrical contact window, the thicker layer means the longer etch time; this will cause the deformation of the photoresist pattern. Hence we chose 800 nm of silicon dioxide.



(a)

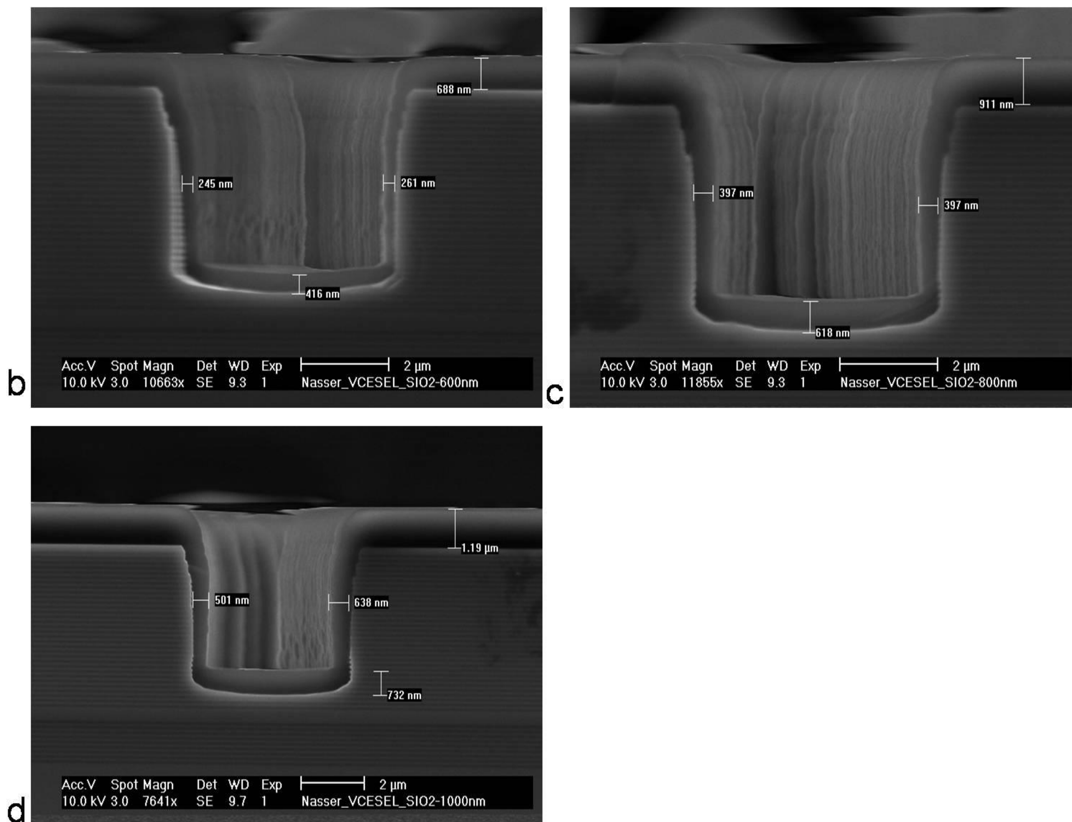


Figure 3.24 (a) Schematic diagram of lack of dielectric layer at the corner of trench. The different silicon dioxide deposition thickness results shown by SEM, the deposition in (b) 600 nm, (c) 800 nm and (d) 1000 nm.

3.3.3 Improvement of annealing process

It is crucial for the EP-VECSELs to achieve low device resistance in the range about a few ohms [6]. RTA is widely used to form low ohmic resistance after depositing thin metal layers [7]. Therefore the optimisation of annealing condition is important for devices. To measure the contact resistance for devices the circular transmission line model (CTLM) was used. This method is more convenient compared to the traditional transmission line model (TLM) because no etch step is needed, current crowding can be avoided and this method also gives a better confinement of the current between contacts [8]. Samples were prepared with a thermally evaporated InGe/Au metal contact as pictured in Fig. 3.25. After that the wafer was cleaved into several smaller pieces of similar size. Those samples were loaded into RTA separately in order to be the annealled at different temperatures.

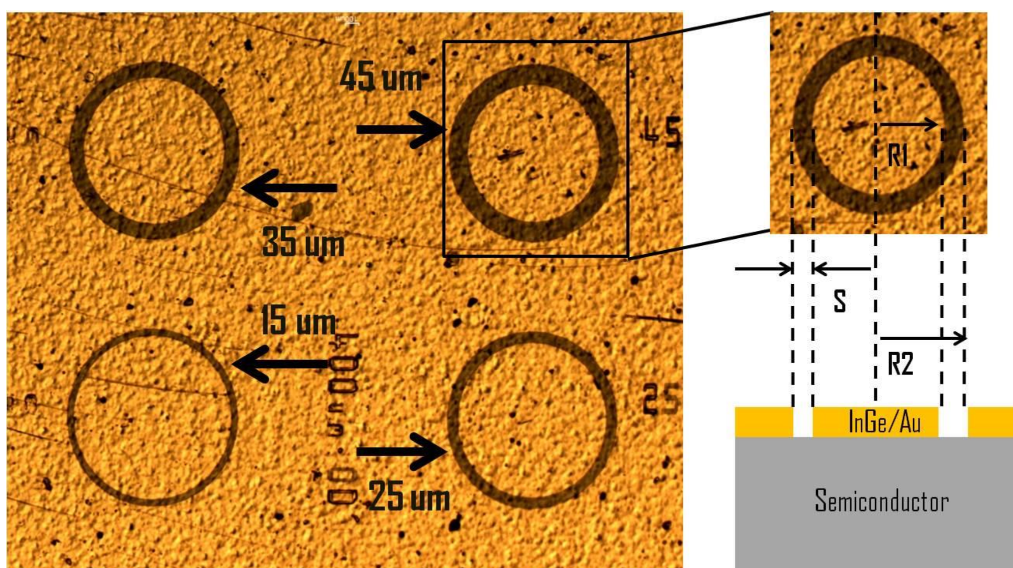


Figure 3.25 The top view of the sample with different gap radius after RTA process.

Two groups of samples were processed, one is on n doped (~2x10^{18} cm^{-3}) and the other is on low n doped (10^{16} cm^{-3}) substrate. The left part of Fig. 3.25 is the top view of the sample after the annealing; on the top right is the top

view of one specific pattern from the sample and the bottom right is the corresponding schematic structure from cross section view. The inner radius is defined as R_1 and the outer radius is R_2. The gap distances S are varied for 6 values from 5 μm to 45 μm while the outer radius R_2 is constant at 200 μm. In the circular transmission line model, two probes are applied, one is placed in the inner circle, and one is on the outer circle, to measure the voltage drop. An IV curve can be plotted after each measurement, and then the slope of this curve was calculated to get the total resistance R_T corresponding to its gap spacing.

The total resistance R_T between the two probes is given by:

$$R_T = \frac{R_{sh}}{2\pi R_1} \left[S + 2L_T\right] C, \tag{3.2}$$

$$L_T = \sqrt{\rho_c / R_{sh}}, \tag{3.3}$$

$$C = \frac{R_1}{S} \, ln\left(\frac{R_1 + S}{R_1}\right), \tag{3.4}$$

where C is the correction factor, R_{sh} is sheet resistance and L_T is transfer length. The derivation of this equation is given in reference [9]. The measurement results are difference between the TLM and CTLM at each gap radius because the contact geometry is different. The correction factor *C* is applied in order to compensate for this error. Thus, the correct value of ρ_c can be obtained by using CTLMs in the same way as TLM [10-11]. The gap spacing value and corresponding correction factor *C* are shown in table 3.2.

Gap distance S (um)	Correction Factor C
5 μm	0.987
10 μm	0.975
15 μm	0.962
25 μm	0.935
35 μm	0.907
45 μm	0.878

Table 3.2 Correction factors (C) versus the gap distance S.

Fig 3.26 shows both the measured data and corrected data with a linear fit as a function of the gap distance for devices under same annealing temperature; all the annealing times used in this experiment were 30 seconds. In this graph, the slope of this linear fit equals to $\frac{R_{sh}}{2\pi R_1}$, the total resistance at S=0 is given by:

$$R_{sh} = \frac{R_{sh}L_T}{2\pi R_1}. \tag{3.5}$$

The intercept of the fitted line with the y-axis gives the value of $2R_c$ which also include the two lead probe resistances.

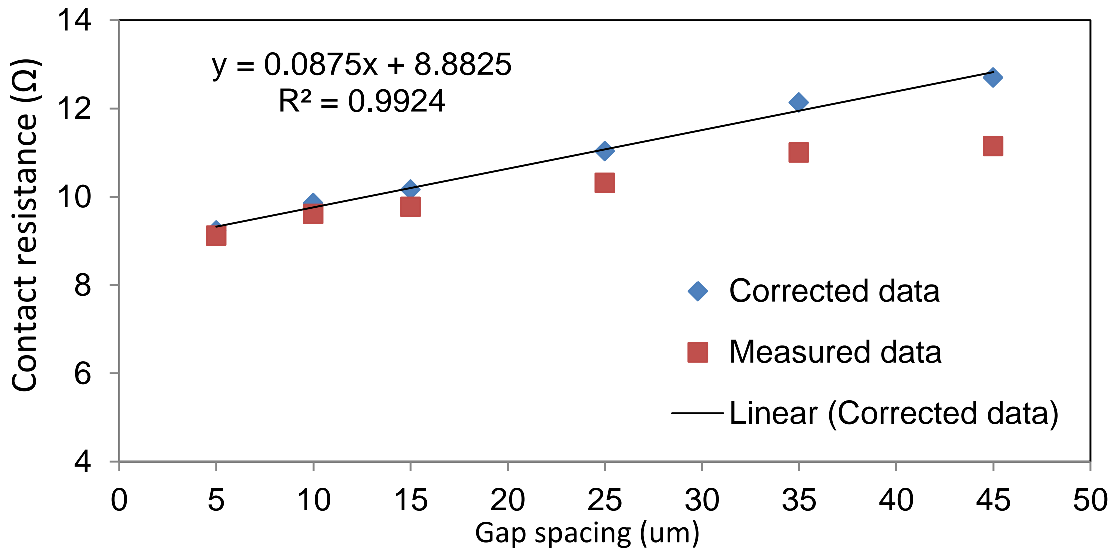


Figure 3.26 Measured and corrected resistance as a function of gap spacing (S) for InGe/Au metal contact annealing at 340 °C.

The probe resistance was measured separately to get a value at 0.7Ω. Therefore:

$$R_c = \frac{2R-0.7}{2}. \tag{3.6}$$

Now the contact resistance versus the anneal temperature for the two samples can be plotted, as seen in the Fig. 3.27. The graph shows that the contact resistance decrease as the annealing temperature increase. Also the n+ doped sample has a lower resistance compare with the low n doped sample at low anneal temperature. But this difference becomes smaller at anneal temperatures higher than 360 °C. The low n doped substrate should be chosen as low doping can reduce the absorption loss in the substrate while it can provide a low contact resistance under higher anneal temperatures.

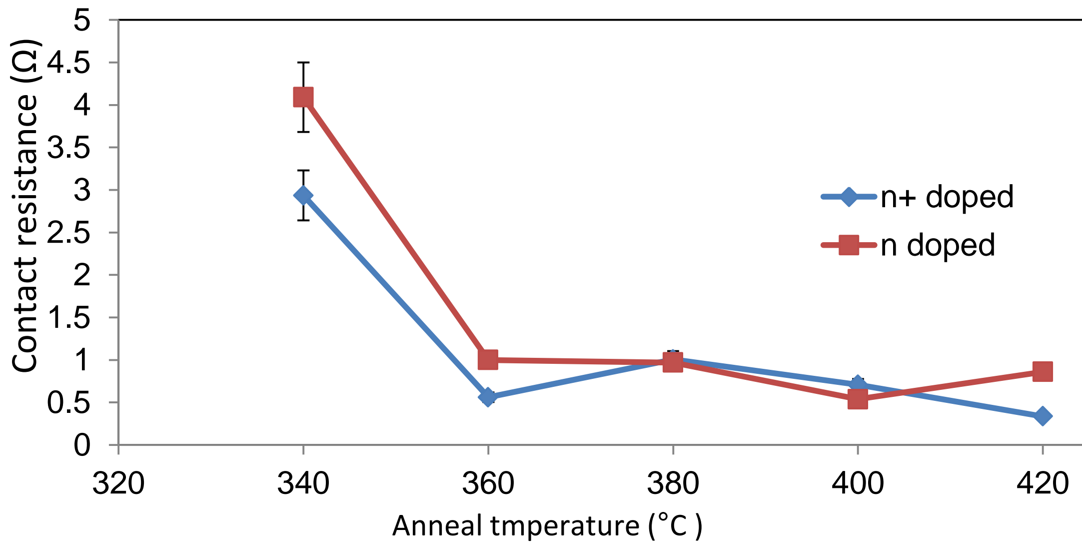


Figure 3.27 Contact resistances R_c as a function of annealing temperature for both the n and n+ doped substrate devices.

A similar experiment was carried out for the p-contact by depositing Au/Zn/Au metal on p doped samples. Fig 3.28 shows the p-contact resistances as a function of anneal temperature excluding the probe resistance (0.7 Ω). The result indicates that a minimum value of the contact resistance can be obtained with an annealing temperature of 360 °C.

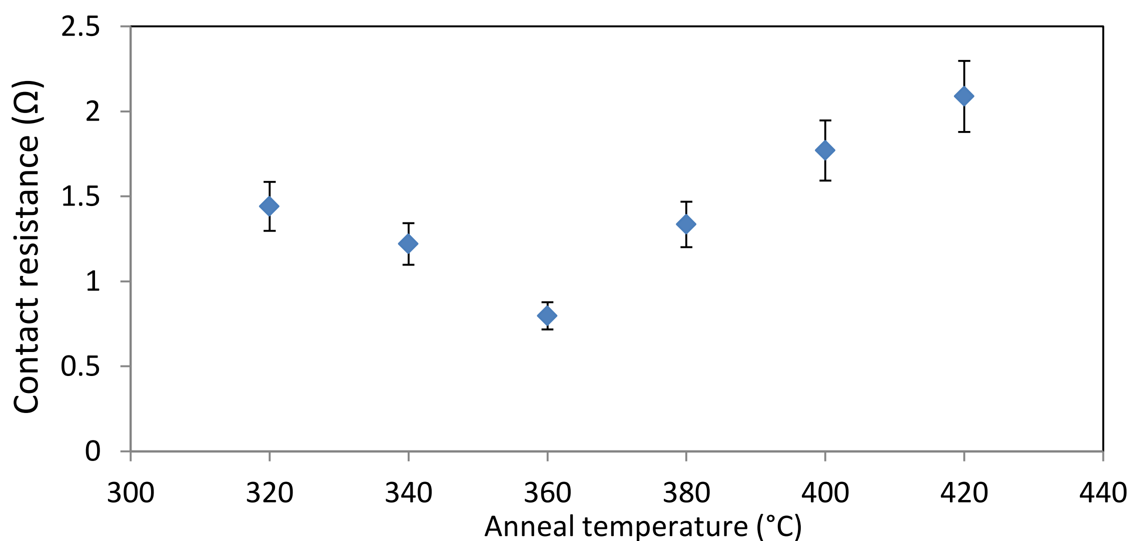


Figure 3.28 Contact resistances R_c as a function of annealing temperature for p doped devices.

For the fabrication of our devices we first deposited the p-contact (Au-Zn-Au) and annealed this contact. The InGe/Au contact was deposited after this

process and also annealed. Both annealing temperature for p and n–doped side are 360 °C with 30 seconds in order to obtain an optimum contact resistance.

3.4 Conclusion

In this chapter the fabrication process of EP-VECSELs was described in detail. The etch parameters of the trench etch recipe and the dielectric layer deposition thickness have been optimised. The SEM images showed that a trench with a straight sidewall and full covered of dielectric layer can be achieved.

The optimum anneal temperature to form low resistance contacts has been investigated. For the p doped side, Au/Zn/Au metal contact has a minimum resistance value at 360 °C, whilst for n doped side, the InGe/Au metal contact resistance reduces with increasing anneal temperature, but the difference after 360 °C is not significant. 360 °C was chosen as the anneal temperature for both contacts.

3.5 Future work

Further improvement work on annealing process can be done on studying different annealing time. Also, a more accurate value of annealing temperature should be investigated around 360 °C for both n side InGe/Au and p side Au/Zn/Au metal contact to form lower contact resistance.

Reference

[1] J. R. Orchard, “Development of Electrically Pumped Vertical External Cavity Surface Emitting Lasers (EP-VECSELs),” Ph.D. thesis, University of Sheffield, UK, 2012.

[2] H. Nagata, T. Shinriki, K. Shima, M. Tamai, and E. Min Haga, “Improvement of bonding strength between Au/Ti and SiO2 films by Si layer insertion,” *J. Vac. Sci. Technol. A Vacuum, Surfaces, Film.*, vol. 17, no. 3, pp. 1018–1023, 1999.

[3] Y. Chassagneux, R. Colombelli, W. Maineult, S. Barbieri, H. E. Beere, D. a Ritchie, S. P. Khanna, E. H. Linfield, and a G. Davies, “Electrically pumped photonic-crystal terahertz lasers controlled by boundary conditions.,” *Nature*, vol. 457, no. 7226, pp. 174–178, 2009.

[4] J. V Sandusky and S. R. J. Brueck, “A CW External-Cavity Surface-Emitting Laser,” *IEEE Photonics Technol. Lett.*, vol. 8, no. 3, pp. 313–315, 1996.

[5] R. Thomas, *Practical Guide to ICP-MS: A Tutorial for Beginners*, 3rd ed. CRC Press, 2013.

[6] G. D. Cole, E. Behymer, T. C. Bond, and L. L. Goddard, “Short-wavelength MEMS-tunable VCSELs,” *Opt. Express*, vol. 16, no. 20, pp. 16093–16103, 2008.

[7] Y. Wang, Y. Wang, L. Li, Y. Zhao, G. Feng, and X. Wang, “Research on Rapid Thermal Annealing of Ohmic Contact to GaAs,” in *2012 International Conference on Optoelectronics and Microelectronics (ICOM)*, 2012, pp. 61–63.

[8] B. Jacobs, M. C. J. C. M. Kramer, E. J. Geluk, and F. Karouta, “Optimisation of the Ti/Al/Ni/Au ohmic contact on AlGaN/GaN FET structures,” *J. Cryst. Growth*, vol. 241, no. 1–2, pp. 15–18, May 2002.

[9] L. LEONG, “Chapter 2 Physics of Metal-Semiconductor Contact and Circular Transmission Line Model (CTLM),” 2004.

[10] K. Gallacher, P. Velha, D. J. Paul, I. MacLaren, M. Myronov, and D. R. Leadley, “Ohmic contacts to n-type germanium with low specific contact resistivity,” *Appl. Phys. Lett.*, vol. 100, no. 2, pp. 022113(1–3), 2012.

[11] B. M. A. M. Ahmad, “Investigation of AuGeNi contacts using rectangular and circular transmission line model,” *Solid. State. Electron.*, vol. 35, no. 10, pp. 1441–1445, 1992.

4. Device Characterisation Techniques

4.1 Introduction

In this chapter, several device characterisation techniques are introduced. I start by showing the general measurement methods to determine the L-I-V and emission spectrum for the devices. I go on to describe the determination of the detuning in the wafer, and go on to discuss the effects of different levels of detuning on device performance. I then describe beam quality measurement techniques. Finally, I describe electroluminescence (EL) mapping measurements. Here, the measured EL intensity profile across the sample is important as it is assumed to reflect the product of electron and hole densities. This forms the base for the modelling work in a subsequent chapter. I then summarise the whole chapter.

4.2 Device general measurements

After the devices have been mounted and wire bonded on a tile, the devices can be used for general tests such as L-I-V and emission spectrum measurement. Before starting the measurements, optical alignment needs to be carried out. The device was placed on the heat sink plate first, with two probes connected to the n and p region of the tile separately for direct current injection. Then a collimating lens was placed on the top of the device, as the divergent beam should be focused into a collimated beam. Alignment between device and collimating lens is achieved by adjust the lens in x-y-z directions with the use of an infrared radiation (IR) viewing card to observe the beam

spot. After this alignment, an output coupler (external mirror) was added between the lens and power meter to form the external cavity enabling the device to lase. Using the same alignment method obtaining a maximal power at a fixed current ensures all the components are well aligned. This setup can be also used to measure the spectrum of the device by replacing the power meter by a fiber optic cable, connected to an optical spectrum analyser (OSA). Fig. 4.1 shows the schematic diagram of the setup for L-I-V and spectral measurements.

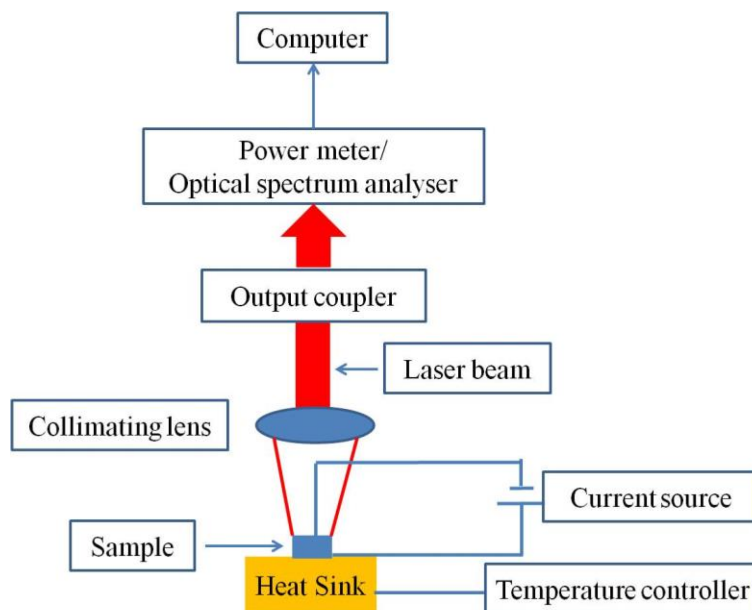


Figure 4.1 Setup for measuring LIV curve and emission spectrum.

Fig. 4.2(a) shows the L-I dependence of a 90 μm diameter device using an output coupler with reflectivity of 80% and Fig. 4.2(b) is the corresponding spectrum measured at 400 mA at room temperature. The device achieves a maximum output power P_{max} at 80.6 mW with a slope efficiency of 0.283 W/A.

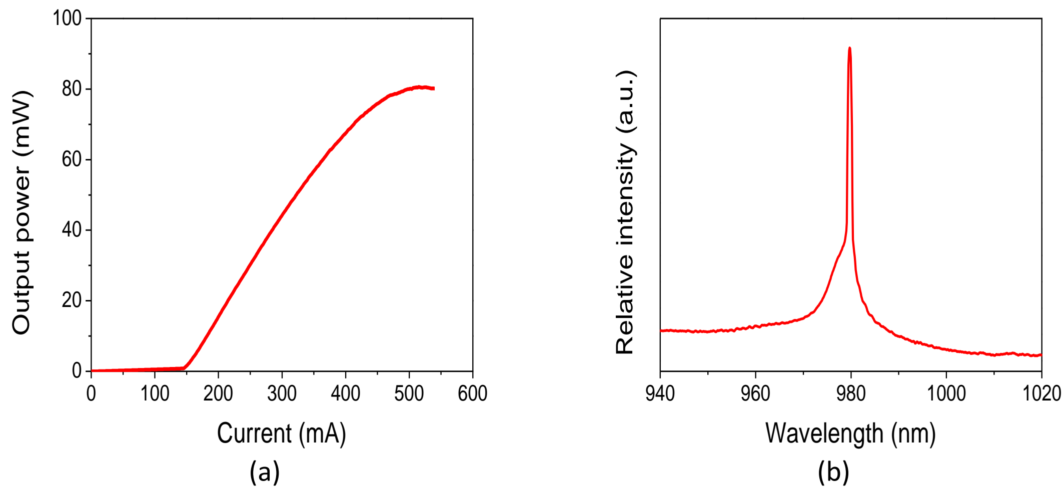


Figure 4.2 (a) L-I dependence for a 90 μm diameter device under room temperature. (b) Corresponding spectrum measured at 400 mA under room temperature.

Fig. 4.3 plots the current dependence of the device spectrum from 0 to 400 mA with a fixed heat sink temperature of 20 °C for the same device. The black curve measured at 0 mA indicates the background noise. The full width at half maximum (FWHM) is about 0.6 nm when lasing. The emission spectrum exhibits a red shift as the injected current is increased. The peak emission wavelength is about 981 nm when the device achieves its maximum power and the shift rate is 0.0094 nm/mA.

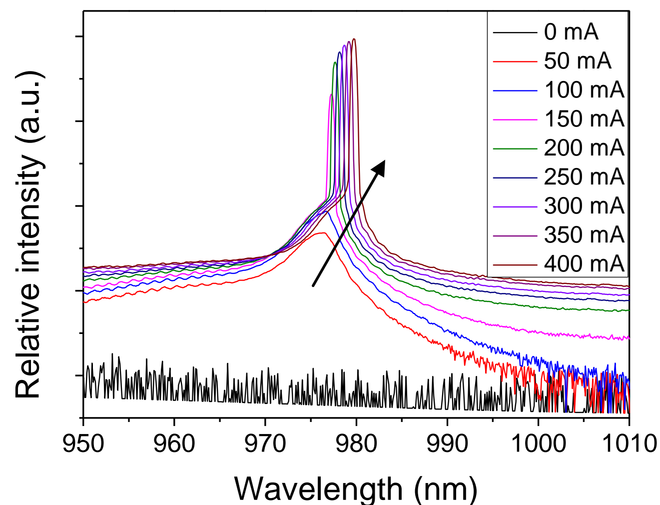


Figure 4.3 Current dependence of the device spectrum at 20 °C.

Fig. 4.4 is the temperature dependence of device spectrum with a fixed current of 200 mA. The heat sink temperature is varied between 10 to 60 °C by adjusting the temperature controller. In EP-VECSELs the cavity resonant wavelength determines the emission wavelength as will be discussed in the next section. The corresponding peak emission wavelength was plotted in Fig. 4.5. Then the shift rate can be calculated by adding linear fit and is almost constant at 0.0838 nm/°C which matches the literature data [1]. This measurement allows the effect of self-heating to be deduced from Fig 4.3. The total of 2.463 nm shift in lasing wavelength from 150 mA to 400 mA is attributed to a 29.4 °C change in the chip temperature due to Joule heating.

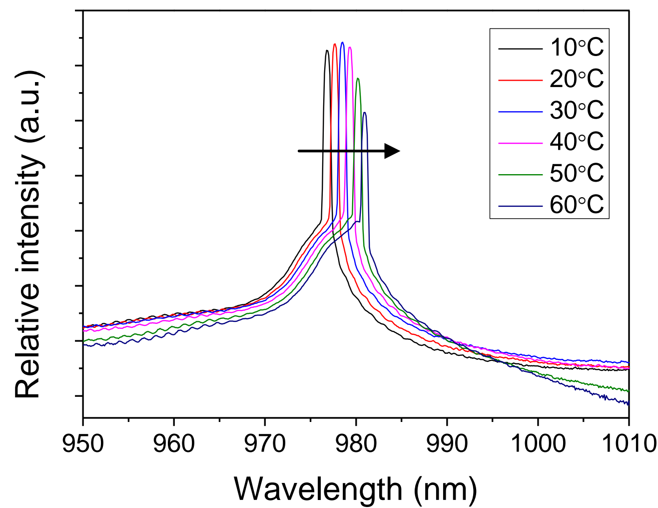


Figure 4.4 Temperature dependence of the device spectrum with current injection at 200 mA.

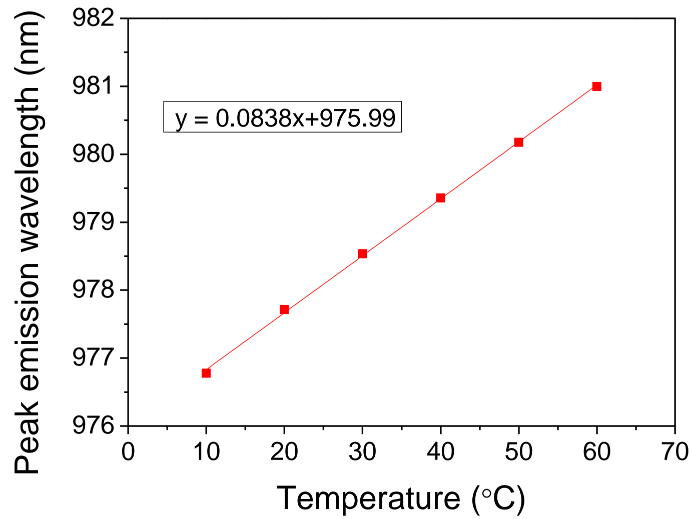


Figure 4.5 Peak emission wavelength shift with temperature with a rate of 0.0838 nm/°C.

4.3 Power scaling

The device diameter of output aperture can be increased in order to obtain higher output power. In this section, devices with various diameters have been tested. Fig. 4.6 plots the P_{max} of the device versus the device diameters from 50 µm to 110 µm. In an ideal situation, it is expected to see a linear increase of maximum output power with area. However, it can be seen that this is not the case. This indicates that in large area devices other factor such as heat dissipation becomes a limitation for device performance. Also the non-uniform charged carrier distribution in large diameter device, which will be shown later, also plays a role in limiting the output power. In the next chapter, an investigation of carrier distribution in large diameter devices will be described in detail.

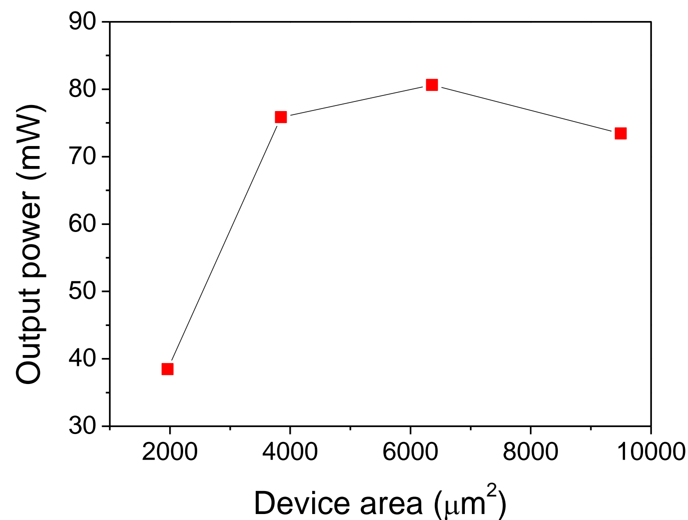


Figure 4.6 Maximum output power versus the device area at room temperature.

4.4 Detuning

Edge emitted lasers usually have a cavity length in an order of the a few hundred microns to a millimetre which makes the space of the cavity modes very close. Thus the lasing mode can always “hop” to another one in order to match the peak gain curve if the gain spectrum shifts due to a change in temperature. Hence, the cavity mode is always matched with the gain peak spectrum and the emission wavelength will be determined by the position of the gain peak [2].

However, in EP-VECSELs, due to the application of high reflective mirrors to form the intracavity, there will be a well defined cavity resonance wavelength that determines the device emission wavelength. The wavelength of neighbouring cavity modes is so far away as to be ignored. Both the cavity resonance and gain spectrum will red shift as temperature is increased.

The cavity resonance shift is mainly governed by the refractive index changes with temperature, while the gain spectrum shifts is due to the energy band gap

changes with temperature which changes four times faster than the refractive index [3]. In the GaAs/AlAs material system, the cavity resonance has a temperature dependent shift of about 0.08 nm/K [4], while the peak in material gain from the QWs has a shift rate of 0.33 nm/k [5]. This difference in rate means that the cavity resonance and peak in gain will match at only one temperature and be mismatched at other temperatures. In order to achieve the maximum output power the cavity resonance and material gain peak should match at a temperature higher than the heatsink operating temperature. Hence, the cavity resonance and material gain peak should be different when we fabricate the semiconductor chip. This is called detuning ($\Delta\lambda=\lambda_{cavity\ resonant}$ - $\lambda_{gain\ peak}$). Fig. 4.7 below demonstrates the definition this concept.

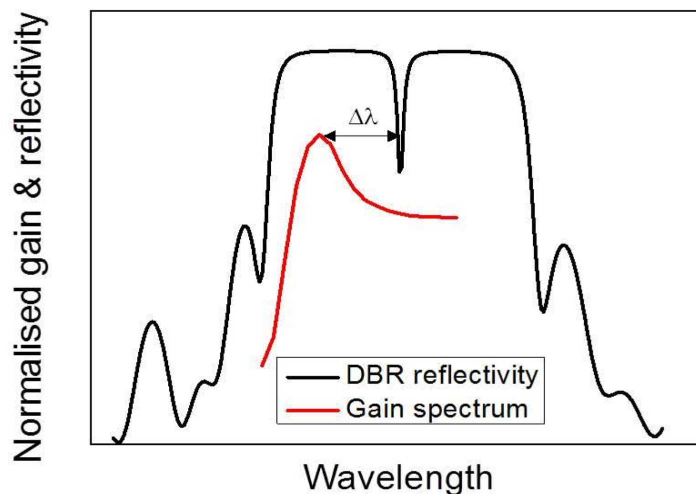


Figure 4.7 Schematic diagram of the definition of detuning (Δλ).

The amount of detuning has a large effect on device performance [6-7]. A lower threshold current can be achieved by a small amount of detuning, while a large detuning can provide a wider operating range before the thermal rollover occurs for the device. It is easy to understand that a small amount of detuning will limit the device output power. But on the other hand, the amount

of detuning cannot be too high. Fig. 4.8 illustrates both the material gain curve and cavity resonant wavelength shift with temperature. As the peak material gain will reduce in magnitude with increasing temperature, due to thermal escape of carriers from the QW, the material gain may drop to quite a low value at the cavity resonance. If the gain cannot overcome all the losses within the system, then the devices will not lase.

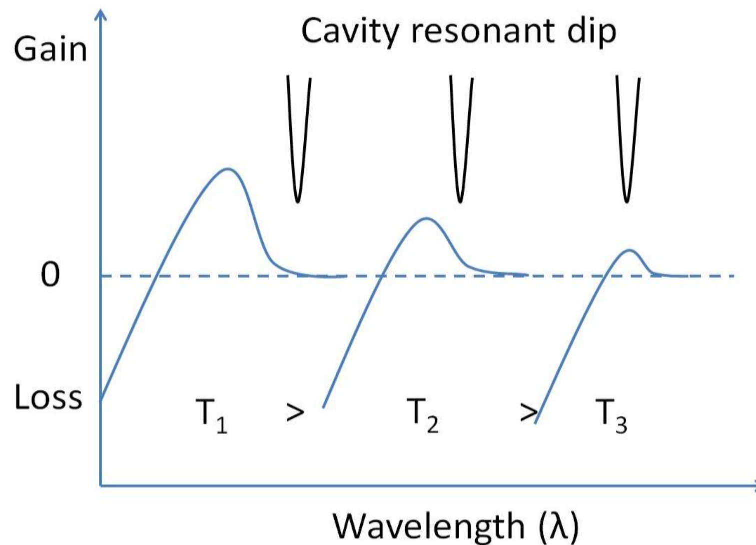


Figure 4.8 Schematic diagrams of both the material gain curve and cavity resonant wavelength shifts with different temperature.

Practically, a detuning between 10 to 15 nm is desired [8] and this is determined using selective etching [9]. Once a wafer has been epitaxially grown, a reflectivity map can be generated as shown in Fig. 4.9(a). It can be seen that the stop-band center varies across the wafer. Then a strip from the centre of wafer with a width of ~3 mm is cleaved to obtain both the cavity resonant wavelength and PL of the QWs by etching the whole p-DBR of the chip. Subsequently, the stopband center, cavity resonance and PL data as a function of distance from the major flat (MF) in 1 mm intervals is plotted as in Fig. 4.9(b). Thus, the amount of detuning can be calculated. The PL spectrum from the QWs is almost uniform across the whole wafer while the cavity

resonant wavelength has a red shift as the distance between the measuring point to wafer's major flat is increased. This is because the rotation of the wafer in metal organic chemical vapor deposition (MOCVD) during the epitaxial process. More material will move to the edge of the wafer and make it become thicker than the wafer centre due to the centrifugal force. As showed in the Fig. 2.9 that a positive error in growth error will give a red shift to the cavity resonant. Hence the value of detuning will vary across the whole wafer. Therefore, it is important to carefully select, and record the location of the sample when cleaving out pieces from the wafer at the beginning of the fabrication process.

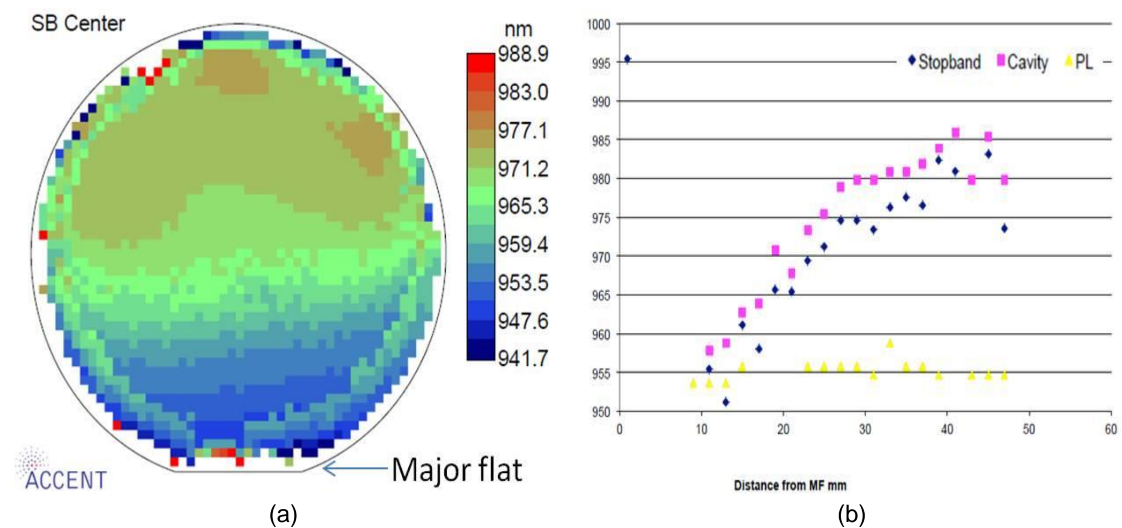


Figure 4.9 (a) Example of stopband (SB) center of an entire wafer from wafer TS728-3. (b) Stopband center (blue), cavity resonant (purple) and PL (yellow) versus the distance from major flat (MF) of the wafer measured by 1 mm interval. (From wafer growth sheet)

4.5 Beam quality measurement

Single transverse mode output is a very important parameter beside output power of a laser. A single mode can be coupled into a single mode fibre for communication systems [10]. But in many cases even though a beam shows

a Gaussian profile, it may be composes of higher order modes [11]. Thus, a method which can measure the beam shape is needed.

The beam quality factor M^2 is widely used in laser science [12]; it is the ratio of beam parameter product (BPP) between the measured beam and a Gaussian beam of the same wavelength. Fig. 4.10 shows the schematic diagram of the M^2 definition. The BPP of a laser beam is the product of its half divergence angle (θ) and beam radius at its beam waist (d_{01}). The cavity of EP-VECSELs will generate Gaussian shaped beam. Therefore, we can use the M^2 method to measure beam quality. The ideal Gaussian beam has a M^2 = 1, other beams with higher modes have M^2 > 1. Therefore, M^2 is a simple parameter to compare the laser output to an ideal Gaussian beam [13].

As showed in Fig. 4.10, the red curve is a Gaussian beam (TEM_{00}) with M^2 = 1, z(0) is the position of its beam waist which has a minimum beam radius d_{01}, z_{R1} is Rayleigh length which has a beam waist of $\sqrt{2} \times d_{01}$ at this position.

$$z_{R1} = \frac{\pi {d_{01}}^2}{4\lambda}. \tag{4.1}$$

In the far field measurement where z >> z_R, the beam radius will increase linearly with z, hence the divergence angle θ of this beam can be calculate by the following equation:

$$\theta = \frac{d_{01}}{z_R} = \frac{4\lambda}{\pi d_{01}}. \tag{4.2}$$

Thus, the BBP of this beam is:

$$\theta \times d_{01} = \frac{4\lambda}{\pi}. \tag{4.3}$$

For the measured laser beam which contains higher order modes, the BBP will always be M^2 times larger than the fundamental mode beam:

$$\theta \times d_{02} = M^2 \times \theta \times d_{01} = M^2 \times \frac{4\lambda}{\pi}. \tag{4.4}$$

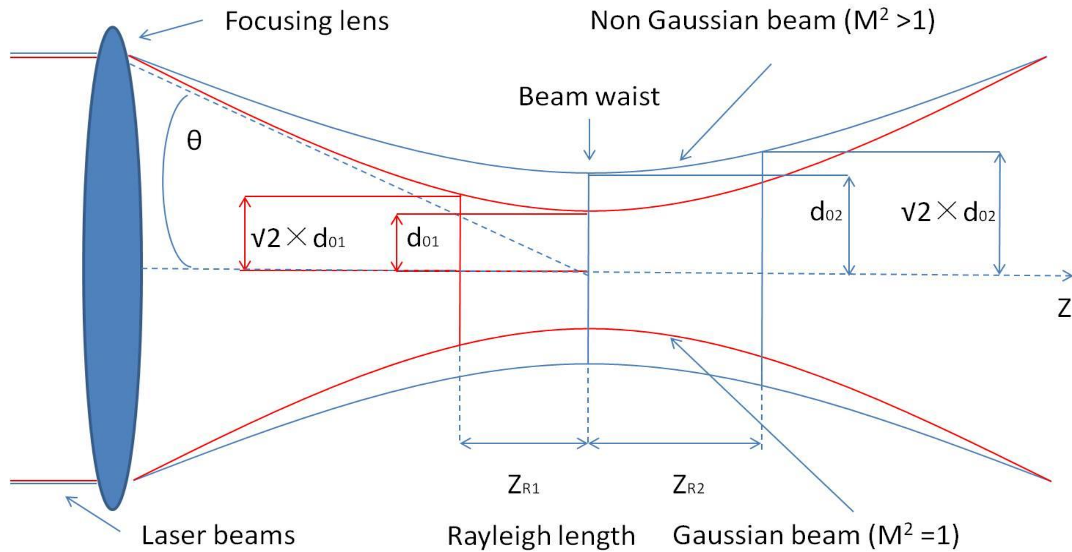


Figure 4.10 Schematic diagram of the M^2 definition.

The setup used in this experiment is M^2-Meter and its supporting software from Thorlabs. Fig. 4.11 shows a schematic diagram of this setup. It contains two optical mirrors, a focusing lens and an iris placed in front of a beam profiler which is connected to a computer and can move along a translation stage [14].

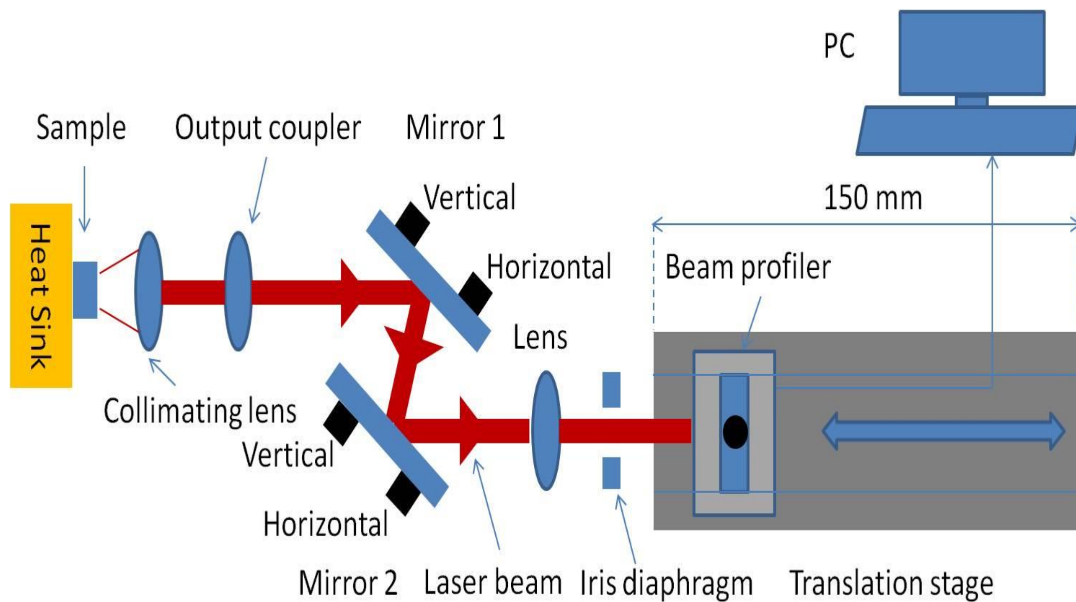


Figure 4.11 the schematic diagram of the beam quality measurement setup.

In order to obtain precise results, the alignment of the laser beam becomes very important in this experiment. In this setup the height and horizontal position of the focusing lens, iris diaphragm and beam profiler has been aligned initially. To align the unfocussed beam first the lens mount needs to be moved away. The sample then needs to be placed on a heat sink, and good alignment with the collimating lens and output coupler to obtain lasing as described in section 4.2. The laser beam must then be aligned in a straight line and focused on the center of the beam profiler, while it moves along the translation stage in a range of 150 mm. In order to achieve this, two adjustable mirrors was added in front of the beam profiler. The use of an iris diaphragm and IR viewing card can help the user to locate the beam spot position on the beam profiler. But this iris diaphragm is only for the beam alignment so it needs fully opened during measurements.

During the M^2 measurement processing, the beam profiler will move on the translation stage while record the beam width value at many points in order to

find the beam waist. Those points were then plotted with hyperbolic fits using the equipment software.

Fig. 4.12 shows the measured data with the fitting curve from a 110 μm diameter device with an 80% output coupler. The two curves represent x and y axis data respectively. The beam waist width is the minimum point on the curve and using this value the M^2 can be calculated, M^2_x = 1.41 and M^2_y = 1.30 and M^2_{mean} = 1.35. The measured power of device in this case is about 2 mW.

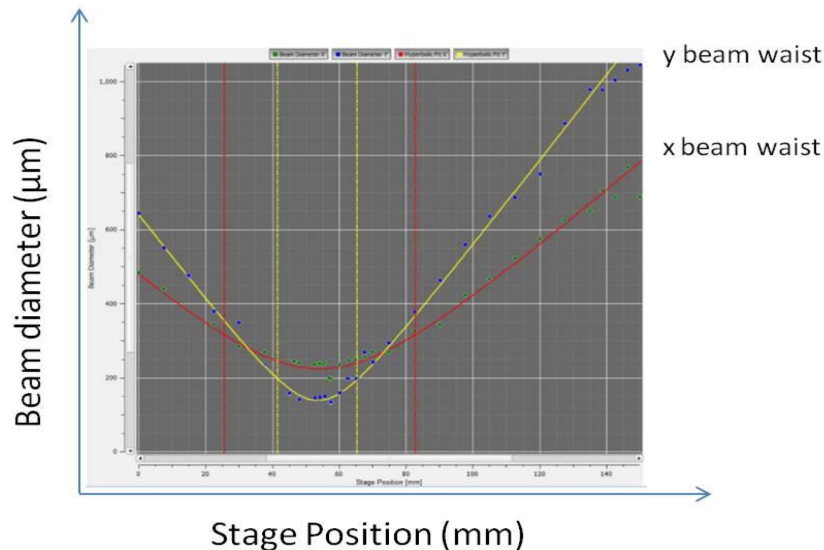


Figure 4.12 M^2 measurement result from the 110 μm diameter device for M^2=1.35 with output at 2 mW.

Further measurements also showed that the M^2 value increased as the injected current increased. This result indicates that charge carrier distribution becomes non-uniform under higher injected currents. In the next section, the mapping of EL will be discussed. The EL map (assumed to correspond to the product of electron and hole densities) is then compared to simulation. This allows us to explore the key factors for improving charge carrier distribution in the next chapter.

4.6 Electroluminescence mapping

EL mapping is an important measurement tool as it can combine the optical emission property with spatial information of the device [15]. This technique can provide a non-destructive method to measure spatial inhomogeneity of EL in 2D [16].

As illustrated in Fig. 4.13, the device (mounted on tile) was put on a copper heat sink inside the cryostat chamber. Without an external mirror, the device cannot lase under the injection of current. The emitted, divergent light is collimated using a lens, and then an image of the device is cast upon the CCD camera using a second lens. Good focussing is ensured by adjusting the lens height until the contour line of the device's output window is clearly observed.

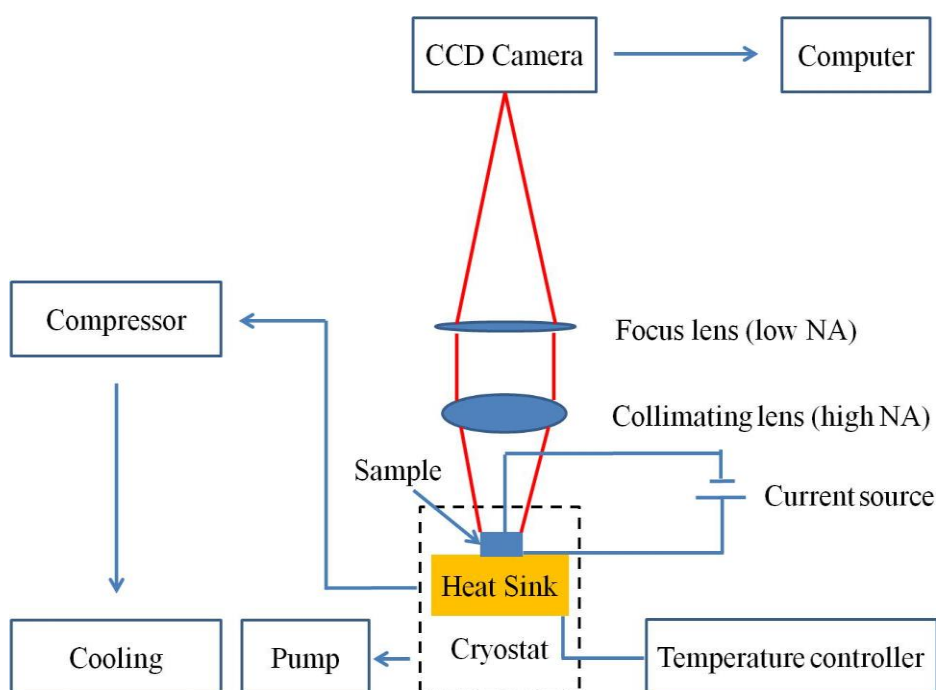


Figure 4.13 Schematic diagram of this EL mapping setup.

This system can also measure the EL map for the device as a function of temperature. In order to achieve cryogenic temperatures, the pressure of the cryostat should be below10^{-6} mBar. The device temperature will be fixed by

the heat sink which is controlled by the temperature controller from room temperature down to 50k; the generated Joule heat will be transferred into the helium which as condensing agent and removed by the compressor first, then use the cooling system to cool down.

Fig. 4.14 shows the example of spontaneous emission image from a 90 μm diameter device at 275K.

Figure 4.14 Focused picture of a 90 μm diameter device at 275K from the CCD camera.

After the image is acquired by the computer, it is digitised to a size of 1280 x 1024 pixels for analysis. Fig. 4.15 is a schematic that illustrates how EL intensity data can be extracted from the acquired image. The dotted lines corresponding to other two EL profiles which are used to find out the center position in the device. These integrated EL graphs are shown to the left and below the acquired image.

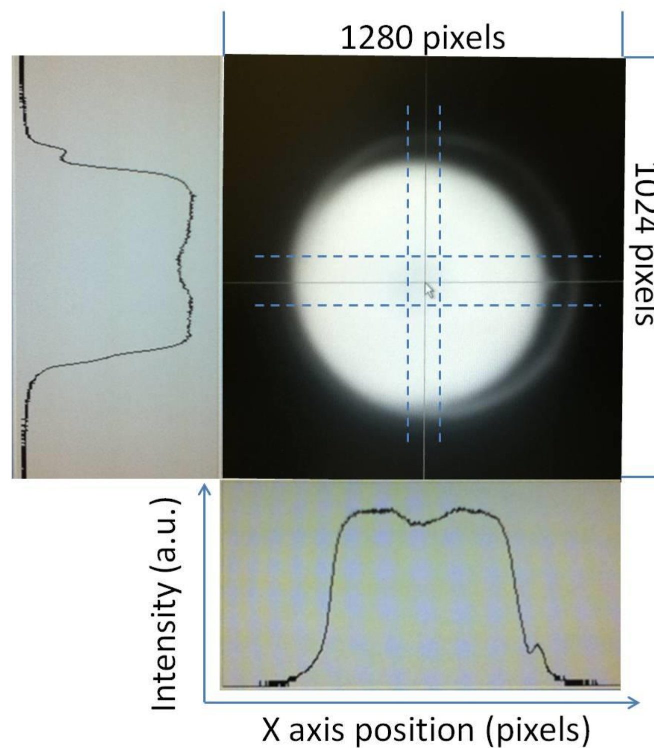


Figure 4.15 Normalised intensity profile from a row and a column in digitised type of focused picture.

4.7 Summary

In this chapter relevant device characterisation techniques for EP-VECSELs have been introduced. The method to measure L-I-V curves and emission spectra were initially discussed. The lack of power scaling with area indicates that heat dissipation and a non-uniform distribution of charge carrier will limit the maximum output power of the devices.

Detuning between the gain peak and cavity resonance in EP-VECSELs is then discussed. The effects of different levels of detuning on device performance were explored. A previously determined detuning of between 10 to 15 nm was explained in terms of a balance between low threshold current and maximum output power. As the amount of detuning various across the wafer after the epitaxial process, it is important to record the original position of the sample when it is cleaved from the wafer.

With the aim of achieving single transverse mode output with a perfect Gaussian beam, the beam quality factor M^2 Is introduced. Measurement of our devices results in a degradation of M^2 as the injection current increases. A uniform current injection is highlighted as a key requirement in maintaining high output powers and simultaneously achieving good beam quality.

An EL mapping system was applied to record the EL intensity distribution within the QWs across the central axis of the device's output window. This result will be useful for comparing experimental and modeling results in future chapters.

Reference

[1] E.Fred Schubert, *Light Emitting Diodes*. Cambridge University Press, 2003.

[2] D. B. Young, J. W. Scott, F. H. Peters, M. G. Peters, M. L. Majewski, B. J. Thibeault, S. W. Corzine, and L. a. Coldren, "Enhanced performance of offset-gain high-barrier vertical-cavity surface-emitting lasers," *IEEE J. Quantum Electron.*, vol. 29, no. 6, pp. 2013–2022, 1993.

[3] B. Tell, Brown-Goebeler K F, R. E. Leibenguth, F. M. Baez, and Y. H. and Lee, "Temperature dependence of GaAs-AlGaAs vertical cavity surface emitting lasers," *Appl. Phys. Lett.*, vol. 60, no. 1992, pp. 683–685, 1992.

[4] J. J. Dudley, D. L. Crawford, and J. E. Bowers, "Temperature dependence of the properties of DBR mirrors used in surface normal optoelectronic devices," *IEEE Photonics Technol. Lett.*, vol. 4, no. 4, pp. 311–314, 1992.

[5] R. S. Geels, B. J. Thibeault, S. W. Corzine, J. W. Scott, and L. A. Coldren, "Design and Characterization of In0.2G a0.8As MQW Vertical-Cavity Surface-Emitting Lasers," *IEEE J. Quantum Electron.*, vol. 29, no. 12, pp. 2977–2987, 1993.

[6] Y. Kaneko, T. Tamanuki, M. Katoh, H. Maekawa, F. Koyama, and K. Iga, "Transverse-mode characteristics of InGaAs/GaAs vertical-cavity surface-emitting lasers considering gain offset," *Jpn. J. Appl. Phys.*, vol. 32, no. 11 A, pp. L1612–L1614, 1993.

[7] T. Rössler, R. Indik, G. Harkness, J. Moloney, and C. Ning, "Modeling the interplay of thermal effects and transverse mode behavior in native-oxide-confined vertical-cavity surface-emitting lasers," *Phys. Rev. A*, vol. 58, no. 4, pp. 3279–3292, 1998.

[8] Alex Mutig, *High Speed VCSELs for Optical Interconnects*. 1991.

[9] J. R. Orchard, "Development of Electrically Pumped Vertical External Cavity Surface Emitting Lasers (EP-VECSELs)," Ph.D. thesis, University of Sheffield, UK, 2012.

[10] F. Marino, S. Barland, and S. and Balle, "Single Mode operation and Transverse Mode control in VCSELs induced by Frequency Selective Feedback," *IEEE Photonics Technol. Lett.*, vol. 15, no. 6, pp. 789–791, 2003.

[11] A. E. Siegman, "How to (Maybe) Measure Laser Beam Quality," 1998, vol. 17, no. October 1997, pp. 184–199.

[12] E. Kapon, *Semiconductor Lasers II - Materials and Structures*. ACADMIC PRESS, 1999.

[13] C. Schulze, D. Flamm, M. Duparré, and A. Forbes, “Beam-quality measurements using a spatial light modulator.,” *Opt. Lett.*, vol. 37, no. 22, pp. 4687–9, 2012.

[14] Thorlabs, “BP104-UV, -VIS, -IR, -IR2 BP109-UV, -VIS, -IR, -IR2 Operation Manual 2011,” 2011.

[15] P. Fischer, J. Christen, and S. Nakamura, “Spectral electroluminescence mapping of a blue InGaN single quantum well light-emitting diode,” *Jpn. J. Appl. Phys.*, vol. 39, no. 2 B, pp. L129–L132, 2000.

[16] B. Li, A. Stokes, and D. M. J. and Doble, “Evaluation of two-dimensional electrical properties of photovoltaic modules using bias-dependent electroluminescence,” *Prog. Photovoltaics Res. Appl.*, vol. 20, no. 8, pp. 936–944, 2012.

5. Modelling Study of Factors Affecting Uniform Carrier Injection in EP-VECSELs

5.1 Introduction

As discussed in the previous chapter, the transverse carrier distribution in EP-VECSEL must be flat topped shaped or single peaked to achieve high beam quality M^2. In order to investigate the transverse carrier distribution profile, I have developed a static model of the substrate-emitting EP-VECSEL. The model is developed using LaserMOD software and its results are reported in this chapter.

Several methods have been developed for controlling the transverse carrier distribution in EP-VECSELs. They rely on the application of an oxide confinement layer [1] or a tunnel junction [2]. Limited modelling work has been carried out on EP-VCSELs, with the exception of an in-depth simulation of surface emitting EP-VECSELs with epitaxial grown current spreading layer [3]. EP-VECSELs developed at the University of Sheffield [4] have a different design employing the substrate as a current spreading layer, a substrate emission, and an etched trench in an attempt to control transverse current spreading within the EP-VECSELs.

In this chapter, physical effects included in the EP-VECSEL model will be outlined. Next, it will be shown how parameters of the model have been optimised to fit experimental and modelling data. The effect of contact misalignment on the carrier distribution within the active element will also be

explored. Effects of several design parameters that can affect the carrier distribution will be studied. These parameters include the number of n-doped DBR pairs, the substrate doping level and its thickness; metal contact geometry and the trench etch depth. A new proposed device structure is given based on these simulations at the end of this chapter. A part of the work from this chapter has been published in [5].

5.2 The model

5.2.1 Physical effects included into the model

In this chapter, I use device simulation implemented in LaserMOD software [6] to investigate the static characteristics of EP-VECSELs. This software can be used for calculating both the optical and electrical characteristics of semiconductor devices. It allows self-consistent multi-physics modelling of semiconductor devices including electromagnetic, thermal, carrier transport and carrier recombination effects as well as interaction between these models. The finite element method is used in the model to give approximate results for partial differential equations based on boundary conditions [6].

To be specific, the EP-VECSEL model used in this work includes:

- electromagnetics model for TE polarised modes of the cavity
- drift-diffusion model of carrier transport
- effects of self-heating
- temperature dependent refractive index
- the Shockley-Read-Hall recombination to include recombination at crystallographic defects in the device

- Auger recombination and interface recombination
- incomplete ionisation due to the low doped substrate (1.5×10^{17} cm^{-3}) for measured devices
- free carrier absorption (FCA) loss

As described in the previous chapter, the relative electroluminescence (EL) profile across the device has been measured. The model can calculate the electron and hole distribution across the active zone. One previous assumption is that the measured EL data is proportional to the electron distribution within the device [7].

In the device, the drift current density can be expressed by

$$J_n = qn\mu_n E, \tag{5.0}$$

$$J_p = qp\mu_p E, \tag{5.1}$$

where q is the charge of an electron, n/p is the electron/hole density, $\mu_{n/p}$ is the electron/hole mobility, E is the electric field density. Thus the drift current density profile will be determined by the electric field. The normalised electric field profile in the substrate is shown in Fig. 5.1a; it has a dip in the centre corresponding to the output window area. On the other side, the electric field shows a constant profile in the p-DBR region in Fig. 5.1b. Then both electron and hole will recombine at the active region, the simulation result in Fig. 5.1c demonstrates that both the electron and hole distribution have the same profile. This means that each of them has the same effect on the EL profile. Therefore, both the electron and hole distributions are then used to calculate

the simulated EL density profile. Then, a comparison can be made between the normalised measured and simulated results.

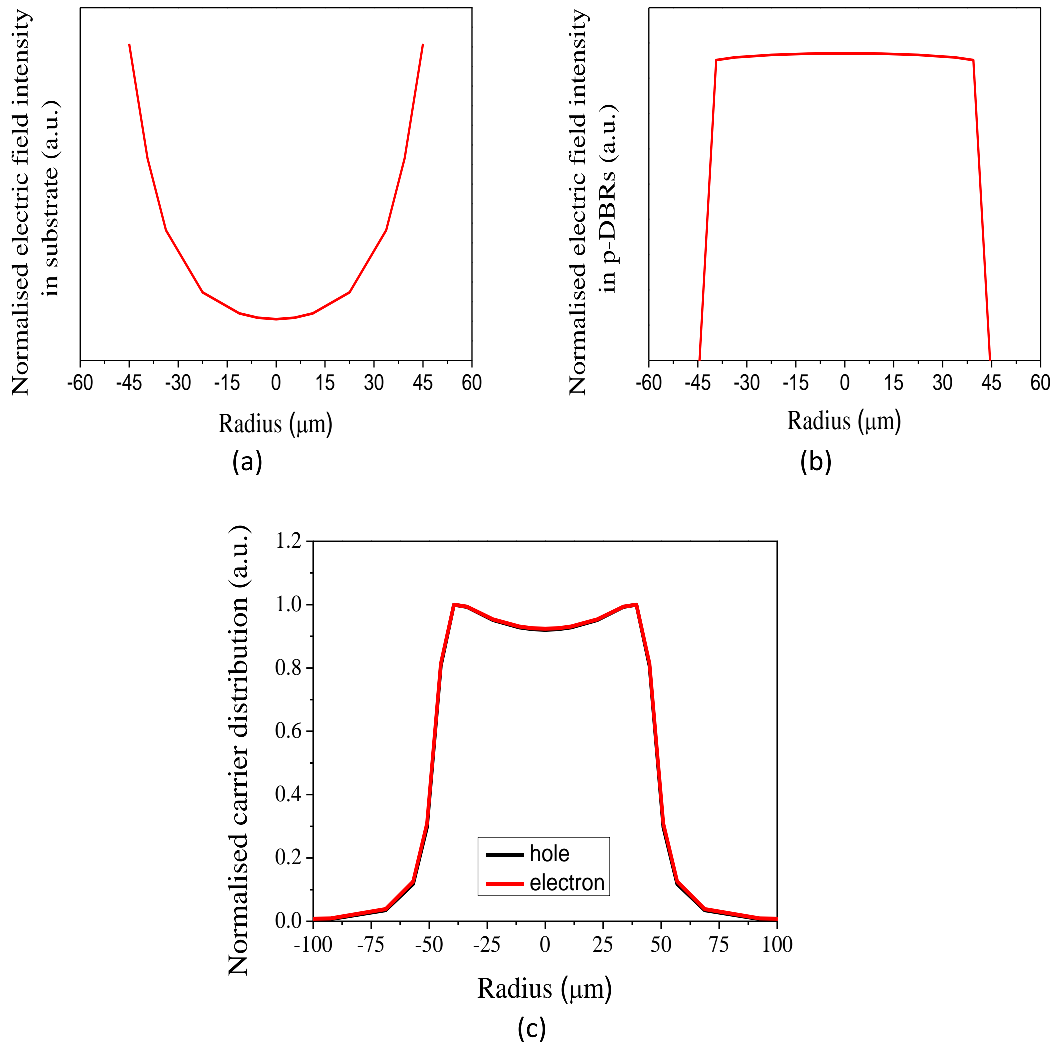


Figure 5.1 (a) Normalised electric field intensity in substrate, (b) Normalised electric field intensity in p-DBRs, (c) Normalised carrier distributions of both electron and hole as an example from a 90 μm diameter device.

5.2.2 Model calibration

Fig. 5.2 illustrates the electrical field intensity and refractive index profile of the fundamental longitudinal mode in the investigated structure. As can be seen from Fig. 5.2, the cavity has a length of 1.5 λ, and contains two groups of three QWs placed at the antinodes of the standing wave, to obtain the

minimum threshold gain [8]. This mode profile is in a good agreement with previously published results [9-10].

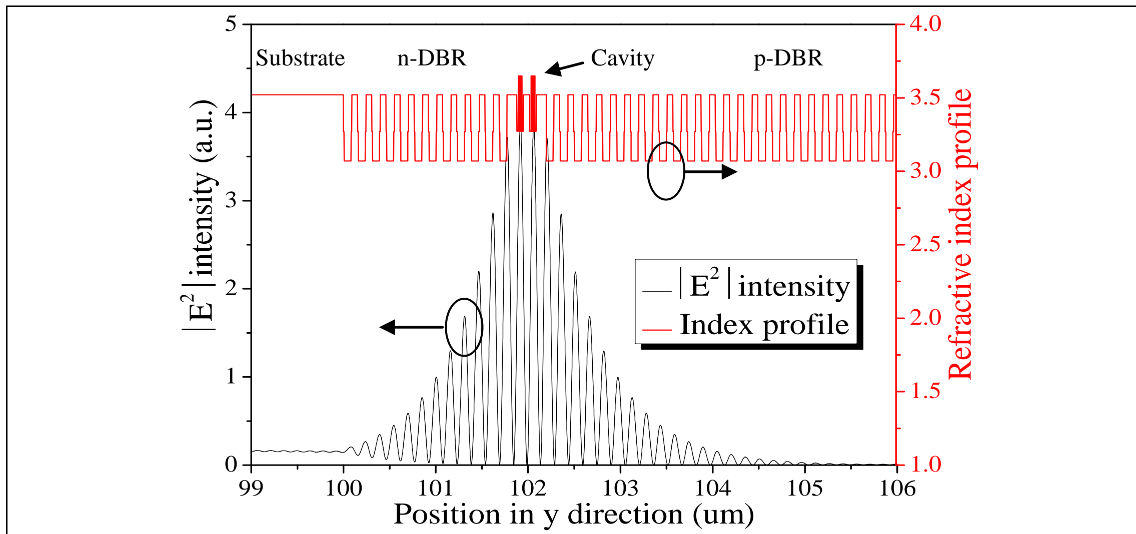


Figure 5.2 $|E^2|$ intensity (black) and refractive index (red) profile in the investigated structure along epitaxial direction.

A contact resistance (R_s) always exists in practical devices and we need to account for it in order to get a better agreement between experimental and modelling results. Fig. 5.3(a) plots a calculated voltage versus current (I-V) characteristics for a 90 μm diameter device with R_s taking values of 2, 4 and 8 Ω. As expected, the slope of this curve is observed to increase as R_s increases. I-V characteristics of four fabricated devices are in a good agreement with the simulated result when R_s = 4 Ω, as shown in Fig. 5.3(b). This result is in good agreement with circular transmission line model (CTLM) measurement results [11]. Measurements have shown that the contact resistance of similar devices maybe as low as 2 Ω as discussed in chapter 3, but may be higher if the fabrication process is not ideal. Thus, to include the effects of contact resistivity of the device in this work, I assume that R_s = 4 Ω in the model.

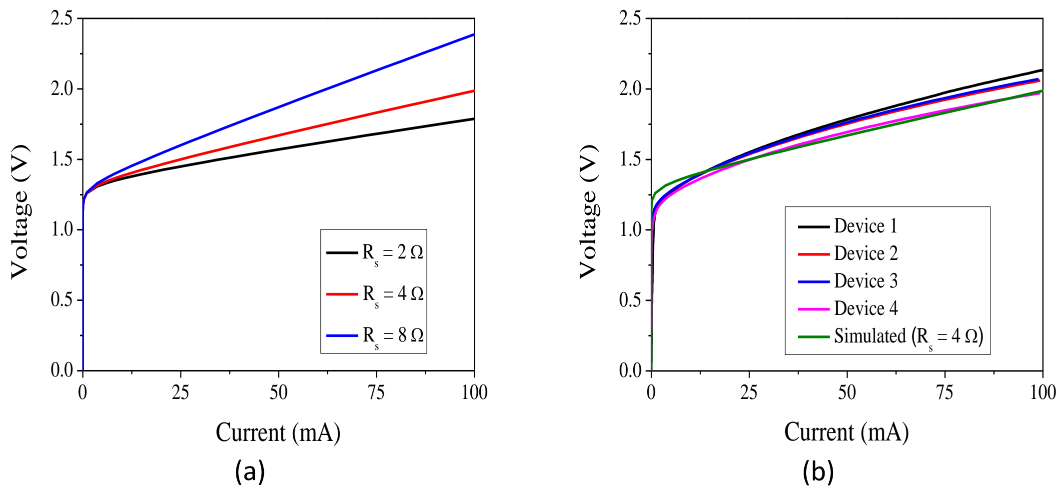


Figure 5.3 (a) Simulated I-V curves for a device with 90 μm diameter mesa versus contact resistance (R_s) and (b) measured 90 μm devices and modelling result with $R_s = 4\ \Omega$.

The charged carrier mobility is another factor that should be considered, as it may also vary the electrical proportion and carrier distribution. Calculated I-V dependencies as a function of electron and hole mobility (μ) of a device with mesa of 150 μm diameter are plotted in Fig. 5.4(a). It can be seen that a decrease of carrier mobility results in an increase of the total resistance in the devices. For the same devices, the normalized EL profile is shown in Fig. 5.4(b). It shows that even if the mobility is reduced by two orders of magnitude, the carrier distribution profile and consequently the EL profile experiences only a very slight change. This is attributed to the change in mobility being isotropic, resulting in no net change in carrier distribution (i.e. only an anisotropic change in mobility can be considered to alter the carrier distribution within the EP-VECSEL). As carrier mobility does not significantly affect the carrier distribution, the default value of carrier mobility from the literature [12] and a contact resistance of 4 Ω is used in this work.

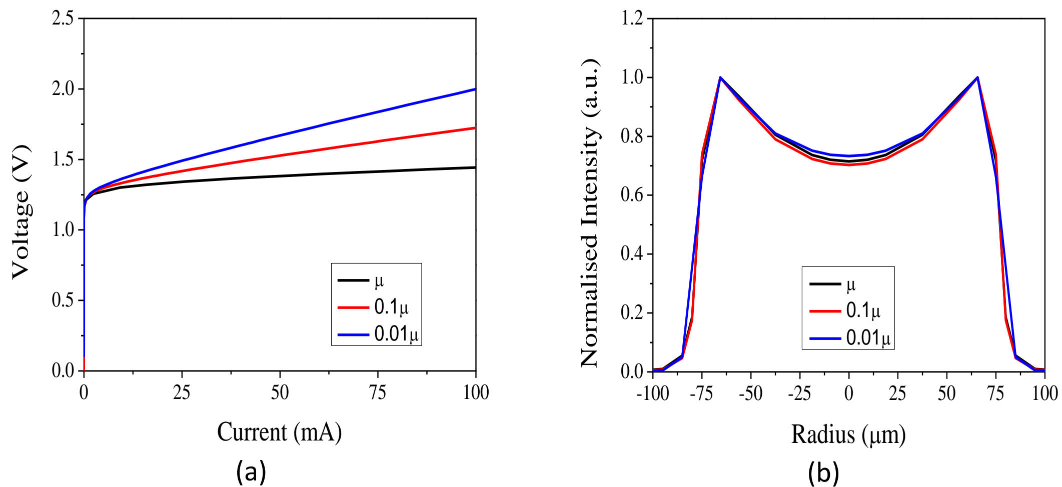


Figure 5.4 (a) Calculated I-V curves for a 150 μm device against electron and hole mobility (μ) and (b) is the corresponding normalised intensity versus mobility.

Fig. 5.5 shows calculated normalised intensity profiles versus device diameter from 30 μm to 150 μm. A single-peaked like distribution profile can be observed for the 50 μm device and smaller. As device diameter is increased a dip in the center of the profile occurs, as the substrate thickness is fixed, the larger the device diameter the more difficult it is for carriers to diffuse to the device center. These simulations are in good agreement with previous work [11]. A significant 'dip' is observed in both the simulation and experimentally when diameter is increased from 50 ~ 90 μm. As a consequence, a 90 μm wide device is considered in the remainder of this chapter in the hope that an improvement in the carrier distribution can be achieved in that device.

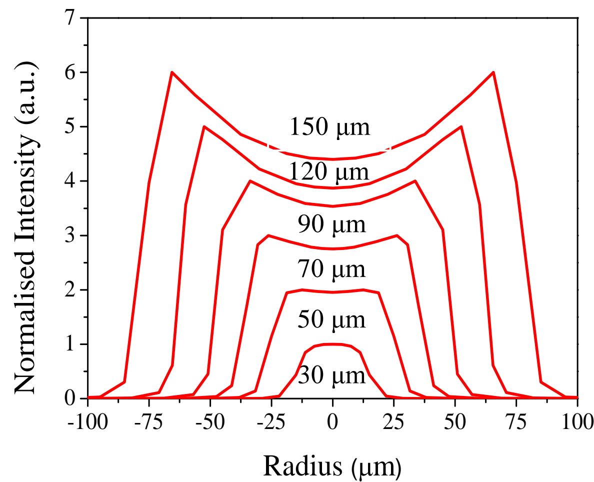


Figure 5.5 Calculated normalised intensity profiles versus the device diameter.

Fig. 5.6 shows both the calculated and measured EL profiles. The measured EL profile is similar to those reported by other groups [9],[10],[13]. The agreement is acceptable for devices of all three diameters using this model. However, an asymmetry of the beam profile is observed which is attributed to contact misalignment in the device which was further explored.

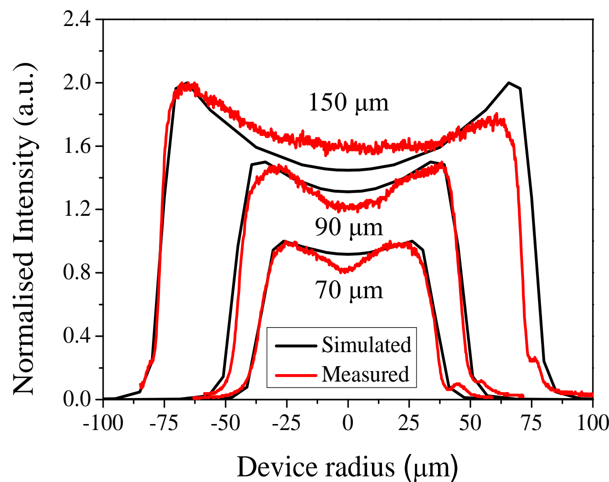


Figure 5.6 Comparison between calculated and measured beam profiles versus device diameter.

The effect of contact misalignment was then included in the model and Fig. 5.7 shows experimental and modelling results. The image in the left column of the Fig. 5.7 shows the active region as recorded by the CCD camera; it contains the output window (a hole in the metal contact) and a bright circle

due to EL from the mesa. The aperture in the metal contact is 10 μm larger than the mesa. The contact misalignment can be characterised by measuring the distance between the centres of both the mesa region and the aperture in the metal contact as shown in Fig. 5.7. Following this method, contact misalignments are measured to be 4, 2 and 8 μm for the 70, 90 and 150 μm diameter devices, respectively.

Measured and calculated intensity profiles are shown in the right column of Fig. 5.7. Each of the simulation result contains three curves that were calculated with no misalignment introduced, with measured misalignment, and double the amount of this misalignment. As expected, the intensity profile changes due to the misalignment, with the best agreement between modelling and experimental results are achieved for exact contact misalignments as measured for the fabricated devices. Therefore, the model is confirmed to provide results that are in good agreement with experiments.

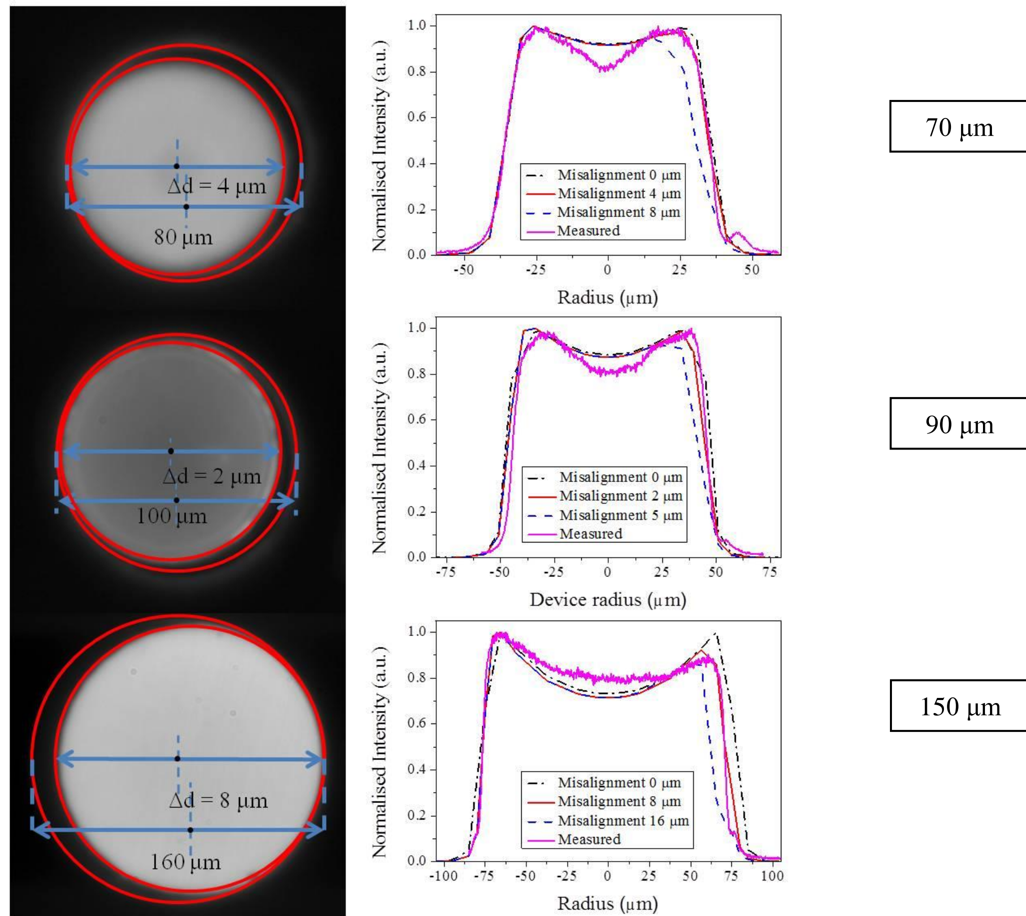


Figure 5.7 Left column shows the image focused on active region for 70 µm, 90 µm and 150 µm diameter devices. Right column shows the corresponding modelled normalised intensity and measured beam profile versus contact misalignment.

5.3 Parametric study

In this section, several parameters such as the trench depth, the substrate thickness and its doping level will be studied in attempt to improve the beam profile for future devices. A device diameter of 90 µm is considered as described previously.

The current spreading layer is an important component of the device that can improve the carrier distribution [3]. EP-VECSEL models with substrate thickness of 10 µm, 100 µm and 600 µm have been simulated and the results

are shown in Fig. 5.8. It can be seen that the thinner the substrate the larger difference between calculated intensity profile and the ideal flat or single-peaked profile. The thin substrate makes carrier transport to central regions of the active zone more difficult. Thus the dip in the center of the profile becomes deeper in the case of a thinner substrate. In the meantime, thicker substrates (or increased doping) will increase FCA and reduce the output power of the device. Hence, there is a trade-off between the need of flat topped profile or single-peaked of the EL intensity and optical loss that will be analysed in detail later.

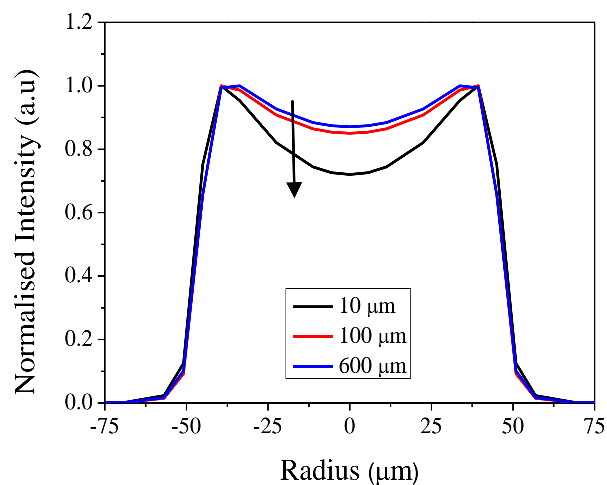


Figure 5.8 Simulated normalised intensity profile of a 90 μm diameter device versus the substrate thickness.

In EP-VECSELs, an n-DBR is positioned between the active region and current spreading layer to form an intracavity in order to reduce the effect of optical absorption loss in the thick substrate and hence reduce the threshold. The effect of the number of n-DBR pairs on the charge carrier distribution has been studied and is shown in Fig. 5.9. Calculated results indicate that this parameter has almost no influence on the intensity profile. Therefore, from this point of design, the future wafer structure will be kept same with 12 pairs of n-

doped DBR. It is noted however, that reducing the reflectivity of this layer will enhance the beam shaping effects of external optics, enabling M^2 to be improved due to these external components. Future optimisation of the device structure and fabrication methods should allow the n-DBR number to be reduced.

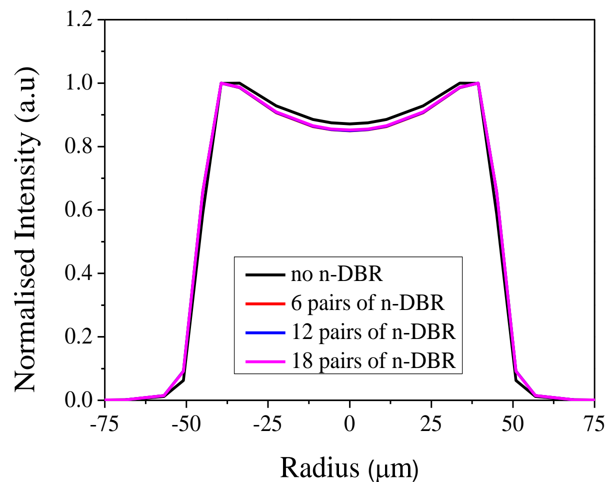
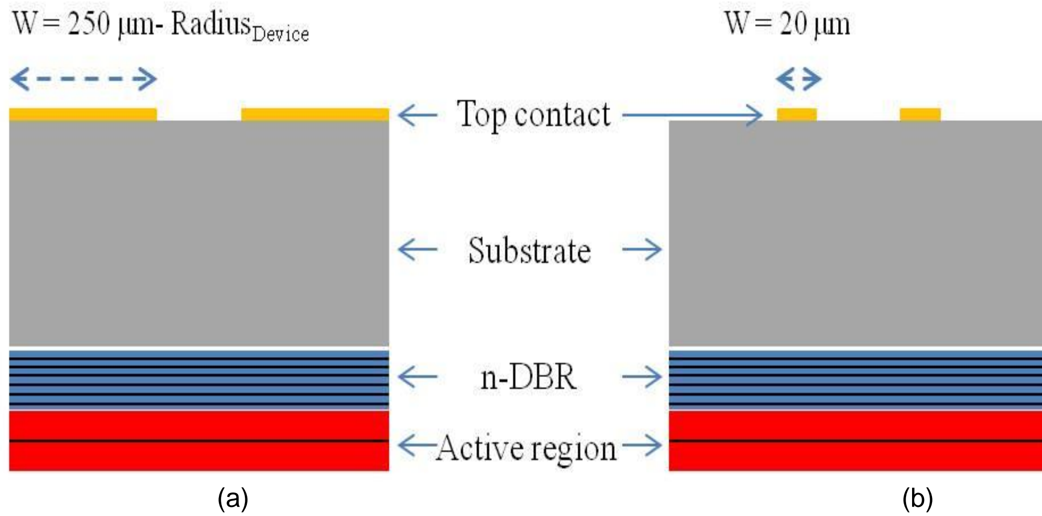


Figure 5.9 Calculated normalised intensity profile versus the number of n-DBR pairs.

In the present device design, the n-side metal contact covers the entire chip surface except for the output window. One of the proposed suggestions [11] is to apply a modified ring contact geometry with a smaller outer radius to improve carrier distribution profile. Both types of contact are schematically shown in the Fig. 5.10(a) and (b). Each wafer is cleaved into individual devices with 500×500 μm area size such that the contact width on top of each side is W = 250μm - R_{device}, where R_{device} is the radius of output window. While the new proposed contact shape is a 20 μm wide ring contact around of the output window. The models with those two different metal contact geometries have been carried out and plotted in Fig. 5.10(c), but the results illustrate that there is no significant improvement of the intensity profile. It is also considered

that this narrow width of contact geometry is also not convenient for gold wire bonding to the tile; the current contact type will therefore be kept for the future design.



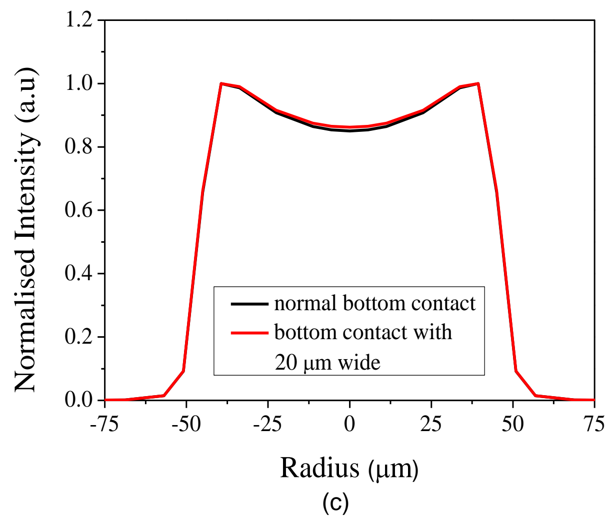


Figure 5.10 (a) n-side metal contact configuration of existing designing with a laser device radius (250µm) minus the radius of output window (R). (b) Modified n-side metal contact type with an outer radius of 20 µm. (c) The calculated normalised intensity profile with two type of n side contact geometry.

In continuing this parameter study, I go on to analyse the effect of doping and thickness of the current spreading substrate. Unlike optically pumped VECSELs, the epitaxial layers in electrically pumped devices must be doped in order to provide carriers to the active zone. Thus, FCA loss will be present in these doped layers during the device operation, whilst, the higher doping

level can provide a lower series resistance which is favoured for devices. Thus, the trade-off between these factors should be investigated.

The FCA coefficient, α, in n-doped GaAs at 980 nm is known to be given by $\alpha = 5 \times 10^{18} \times n$ cm^2, where n is the electron density [14]. First devices with substrate thickness of 100 μm with different doping levels are studied, and the results are shown in Fig. 5.11. The diagram demonstrates that the transverse uniformity of the intensity profile becomes improved as the doping level increases, but it also shows that this improvement is not significant when the doping level exceeds 4×10^{17} cm^{-3}. However, this does not consider the increased FCA loss.

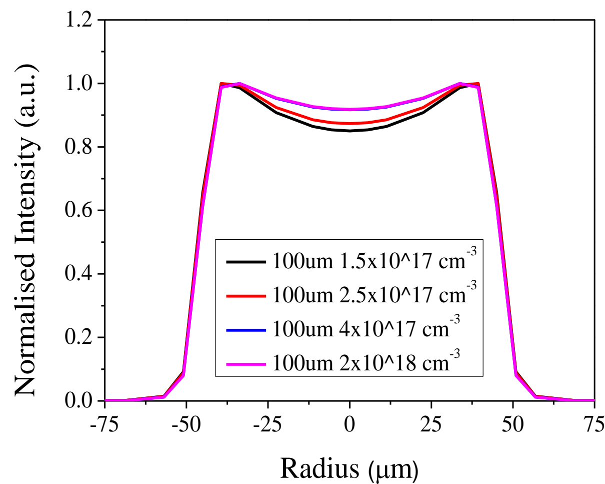


Figure 5.11 Calculated intensity profiles with substrate thickness of 100 μm versus doping density.

Fig. 5.8 and Fig. 5.11 shows that increasing substrate thickness and/or doping level can improve the intensity profile, but this improvement also accompanied by the increase of FCA loss. In next step, simulation results with constant FCA loss are plotted in Fig. 5.12. In order to make the difference between calculated results suitable for comparison, I define the difference between the value of normalised peak point and center dip in the intensity profile as Δ.

Four carrier distributions for substrate thicknesses ranging from 20 μm to 400 μm are shown in Fig. 5.12(a). It can be seen that the optimum substrate thickness resulting in a minimum Δ cannot be determined from these dependencies. To study this further, Δ at a constant absorption loss has been plotted in Fig. 5.12(b) versus the thickness in the range of 2.5 μm to 400 μm. It is clear to see that the lowest value of Δ can be obtained with substrate thickness of 40-60 μm and a corresponding doping level in the range between 3.75 and 2.5 × 10^{17} cm^{-3}. This suggests that thick, epitaxially grown current spreading layer may be required in the future devices [15], as an accurate doping level and thickness may be required.

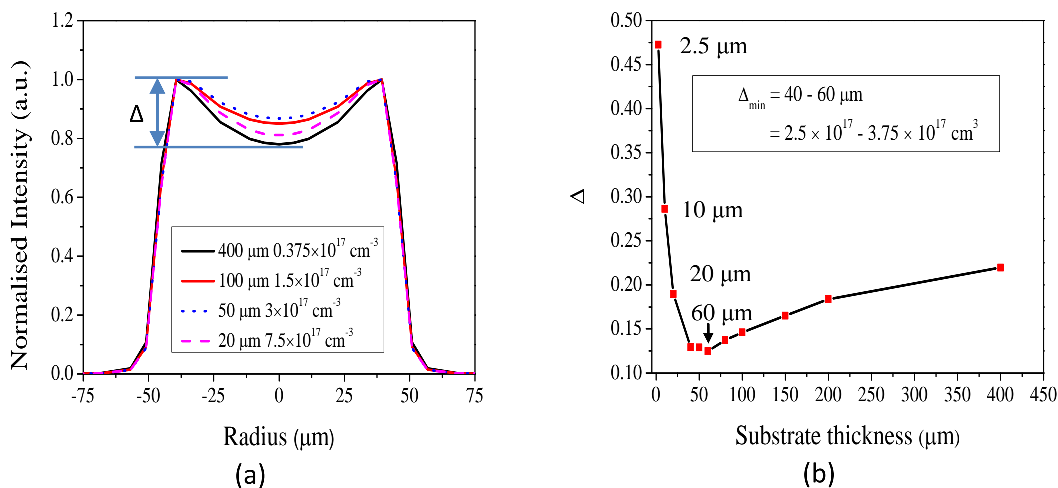


Figure 5.12 (a) Calculated intensity profile at a constant absorption loss (thickness × absorption coefficient) and (b) value of Δ under constant absorption loss with substrate thickness from 2.5 μm to 400 μm.

As an etched trench is used in our structure in order to confine charged carriers, it is important to explore the effect of the trench depth on the intensity profile. Fig. 5.13 shows a schematic diagram of the device structure and labels corresponding to a range of trench depths. In this picture, A corresponds to the case when no trench is fabricated in the device, B – the

trench is etched through half of the p-DBR, C – the trench etching is stopped above the cavity, D – the trench is etched through the cavity, E – the trench is through p-DBR, cavity and n-DBR and F - the trench is etched all the way through the device down to substrate. T is the depth of the trench in the substrate.

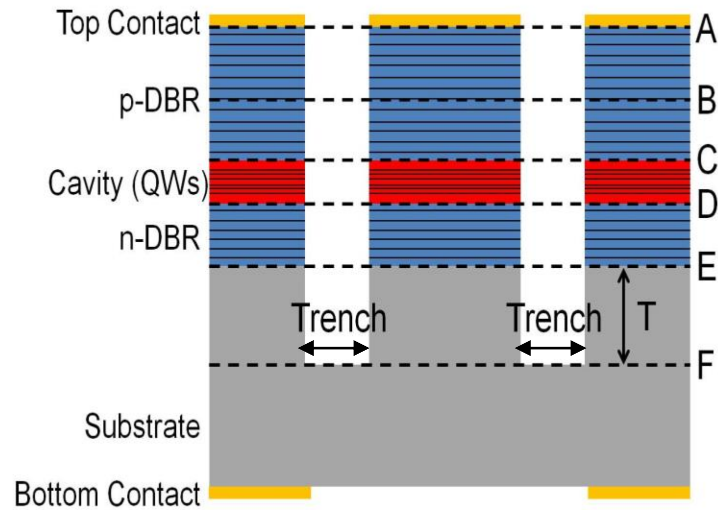


Figure 5.13 Schematic diagram showing various trench etch depths.

The calculated results from A to F (T=10 μm) are illustrated in Fig. 5.14. It is surprising to note that any etch that does not penetrate the substrate is detrimental to obtaining the desired carrier distribution. These observations lead to a more thorough study of different etch depth into the substrate (T).

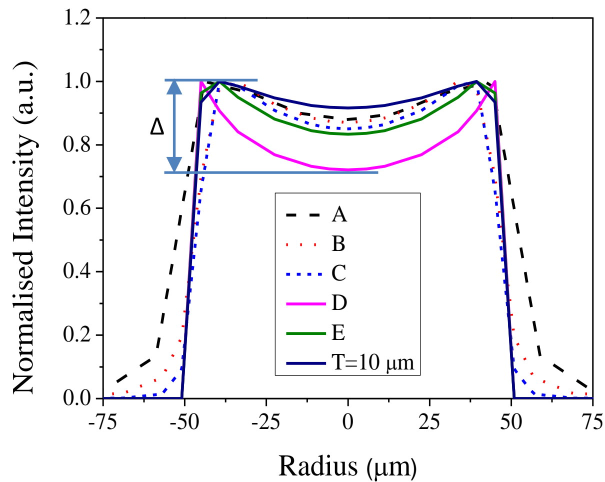


Figure 5.14 Calculated intensity profile versus the trench depth of a device with 90 μm mesa diameter.

Fig. 5.15(a) and (b) shows the simulated intensity profile of a 90 μm and 150 μm diameter device, as a function of the depth of the etch into the substrate. The results indicate that the carrier distribution profile is getting more flat as the trench depth inside the substrate is increase for both two cases.

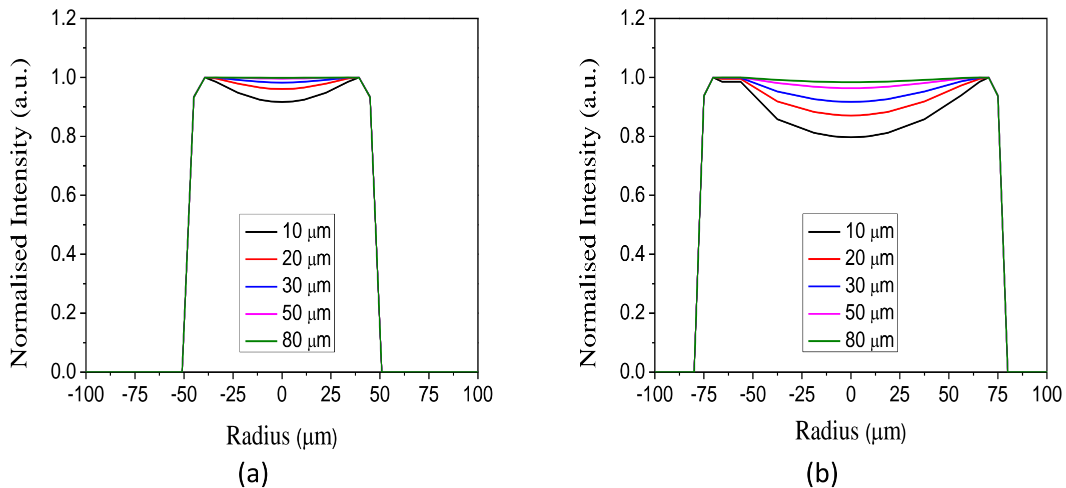


Figure 5.15 (a) Normalised intensity versus T in the ranging of 10 μm to 80 μm of a 90 μm diameter device (b) Normalised intensity versus T in the ranging of 10 μm to 80 μm of a 150 μm diameter device.

In order to give a clear observation on the effect of trench depth, Δ versus both the device diameter and etched trench depth into the substrate was calculated and plotted in Fig. 5.16. Result shows that the deeper the trench

etched into the substrate is, the smaller value of Δ can be obtained. This also yields a more uniform charge carrier distribution. In results of all three mesa diameters, Δ decrease quickly as T increases It is also clear to see that Δ decreases significantly in large devices than in small ones, which means this design is more suitable on large area devices. Therefore, in the future device design, a trench etched into the substrate can be applied in order to achieve both high power and high beam quality devices.

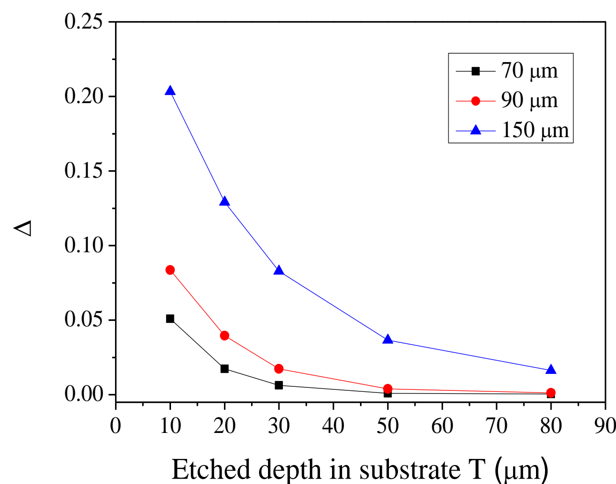


Figure 5.16 Δ versus the etch depth in substrate (T) for three device diameters.

5.4 Summary

In this chapter, the results of modelling of the transverse carrier distribution in EP-VECSELs using commercial simulation software have been reported. The simulated and opto-electronic properties of the device (with regard to the carrier distribution) are in good agreement with experiment. The effects of contact misalignment have been modelled and modelling results have reproduced the experimentally observed effects of this misalignment on the

EL profile. Thus, it has been possible to confirm the validity of the model in describing the carrier distribution within the devices.

Investigations of factors influencing the beam profile of EP-VECSELs were then carried out. Those parameters indicate that if all other device design parameters remain constant, 40-60 μm thick substrates with optimal doping will improve the intensity profile. An analysis of the effect of trench etch indicates that it is in fact detrimental to the carrier distribution profile. Improvements are only observed when the etch penetrates the substrate.

5.5 Future work

Some work can be considered on continuing improving the beam profile in the future work. The results of Δ for optimise substrate thickness and doping level as shown in Fig. 5.12 should be recalculated under the condition of no trench etch as it was shown that shallow trench depths in fact deteriorate the carrier distribution and hence beam profile. The number of n-DBR pairs should be reduced. Whilst they do not affect the EL-intensity profile, less n-DBR pairs can make the device more sensitive to external feedback shaping. Fig. 5.16 shows that a very deep (e.g. 50 μm deep) trench depth in the substrate is a route to enhancing the carrier distribution profile in devices with a large diameter. Such devices would pose a significant challenge in fabrication and may require additional process steps. But a 10 um of trench depth into the substrate can be tried to check the device performance.

Now a model has been realised, it can be extended to include ion implantation and oxide confinement layers.

Reference

[1] P. Zhao, B. Xu, R. Van Leeuwen, T. Chen, L. Watkins, D. Zhou, and P. Gao, “Compact 4.7 W, 18.3% wall-plug efficiency green laser based on an electrically pumped VECSEL using intracavity frequency doubling,” *Opt. Lett.*, vol. 39, no. 16, pp. 4766–4768, 2014.

[2] A. Caliman, A. Sirbu, A. Mereuta, K. Pier, V. Iakovlev, and E. Kapon, “14XX nm-wavelength electrically-pumped VECSELs fabricated by wafer fusion,” *Opt. Express*, vol. 21, no. 11, pp. 13668–13674, 2013.

[3] P. Kreuter, B. Witzigmann, D. J. H. C. Maas, Y. Barbarin, T. Südmeyer, and U. and Keller, “On the design of electrically pumped vertical-external-cavity surface-emitting lasers,” *Appl. Phys. B*, vol. 91, no. 2, pp. 257–264, Mar. 2008.

[4] J. R. Orchard, D. T. D. Childs, L. C. Lin, B. J. Stevens, D. M. Williams, and R. A. and Hogg, “Design Rules and Characterisation of Electrically Pumped Vertical External Cavity Surface Emitting Lasers,” *Jpn. J. Appl. Phys.*, vol. 50, no. 4, Apr. 2011.

[5] X. Jin, P. Ivanov, D. T. D. Childs, N. Babazadeh, J. Orchard, and J. Benjamin, “Optimisation of Fundamental Transverse Mode Output in Electrically Pumped Vertical External Cavity Surface Emitting Lasers,” *Proc SPIE*, vol. 9349, 2015.

[6] RSoft Design Group, “LaserMod 9 User guide,” 2012.

[7] J. R. Orchard, D. T. D. Childs, D. Williams, L.-C. Lin, B. J. Stevens, J. S. Roberts, and R. a. Hogg, “Trade-offs in the realization of electrically pumped vertical external cavity surface emitting lasers,” *Semicond. Laser Conf. (ISLC), 2010 22nd IEEE Int.*, vol. 17, no. 6, pp. 1745–1752, 2010.

[8] S. W. Corzine, R. S. Geels, J. W. Scott, R. H. Yan, and L. A. and Coldren, “Design of Fabry-Perot Surface-Emitting Lasers with a Periodic Gain Structure,” *IEEE J. Quantum Electron.*, vol. 25, no. 6, pp. 1513–1524, 1989.

[9] Y. Barbarin, M. Hoffmann, W. P. Pallmann, I. Dahhan, P. Kreuter, M. Miller, J. Baier, H. Moench, M. Golling, S. Thomas, B. Witzigmann, and U. and Keller, “Electrically Pumped Vertical External Cavity Surface Emitting Lasers Suitable for Passive Modelocking,” *IEEE J. Sel. Top. QUANTUM Electron.*, vol. 17, no. 6, pp. 1779–1786, 2011.

[10] O. G. Okhotnikov, *Semiconductor Disk Lasers: Physics and Technology*. Weinheim: Wiley-VCH Verlag GmbH & Co. KGaA, 2010.

[11] J. R. Orchard, “Development of Electrically Pumped Vertical External Cavity Surface Emitting Lasers (EP-VECSELs),” Ph.D. thesis, University of Sheffield, UK, 2012.

[12] O. Madelung, *Semiconductors – Basic Data*, 2nd Ed. Springer-Verlag, Berlin, 1996.

[13] A. Bousseksou, S. Bouchoule, M. El Kurdi, M. Strassner, I. Sagnes, P. Crozat, and J. and Jacquet, “Fabrication and characterization of 1.55 µm single transverse mode large diameter electrically pumped VECSEL,” *Opt. Quantum Electron.*, vol. 38, no. 15, pp. 1269–1278, Mar. 2007.

[14] K. Osamura and Y. Murakami, “Free Carrier Absorption in n-GaAs,” *Jpn. J. Appl. Phys.*, vol. 11, no. 3, pp. 365–371, 1972.

[15] J. K. Sheu, G. C. Chi, and M. J. Jou, “Enhanced output power in an InGaN-GaN multiquantum-well light-emitting diode with an InGaN current-spreading layer,” *IEEE Photonics Technol. Lett.*, vol. 13, no. 11, pp. 1164–1166, 2001.

6. Cascaded EP-VECSELs

6.1 Introduction

In EP-VECSELs the power scaling will have a limitation in increasing the device diameter, due to the non-uniform carrier distribution discussed previously. Thus, multiple chips may need to be combined in order to generate larger output powers when a single chip cannot meet the requirement. Some work has been carried out on OP-VECSELs previously, such as using symmetric W-shaped cavity [1], a Z-shaped cavity [2-3], or VVV-cavity [4] to achieve power scaling for two or more devices. In fact that the different cavity geometry consists of multiple chips or optical elements are widely used in research area for many purposes, such as second-harmonic generation [5-6], passively mode locking [7-9] and two wavelength generation [10]. In addition, OP-VECSELs have recently been used to produce a dual wavelength laser which has allowed very high intra-cavity powers to generate THz by difference frequency generation [11]. This work utilizes a single gain chip and an intra-cavity etalon to achieve the dual wavelength lasing. In this chapter I present an x-shaped cavity using two EP-VECSELs, to the best of my knowledge, this is first report where EP-VECSELs are cascaded within the same cavity. I show that a higher power can be achieved from the cascaded system as compared to the individual devices in a linear cavity. I go on to show the effect of detuning the cascaded laser system to achieve dual wavelength emission, providing a possible EP-VECSEL route to THz generation.

6.2 Cavity geometry

The cascaded laser system applied here is shown schematically in Fig. 6.1(a). Two 70 μm diameter EP-VECSELs with emission wavelength at 980 nm were used in this demonstration. One device was placed on a heat sink and is termed laser 1, and may be turned via the attached TEC. The other is labelled laser 2. Tuning of this device is possible through self-heating device.

The x-shaped cavity configuration is applied to combine the beams of two EP-VECSELs, it includes a tilted mirror with 50% reflective placed between the two lasers, with a 40% and 100% reflective mirror at two ends of the cavity. The two lasers act as the two other high reflective end mirrors in the cavity. Two collimating lenses with the same focal length are applied in order to give the same effect on the two lasers. The emission wavelength of laser 1 can be tuned to match emission wavelength of laser 2 by changing the heat sink temperature to achieve locking of the two lasers. It is worth noting that due to the strict alignment requirement in the cavity, the angles between the devices and mirrors are critical, as are their positions.

In order to make a comparison, measurements of the individual lasers were carried out first using the linear cavity that is shown in Fig. 6.1(b). The single device was measured using an 80% reflectivity output coupler. This value of output coupler has previously been found to be optimum for these devise [12].

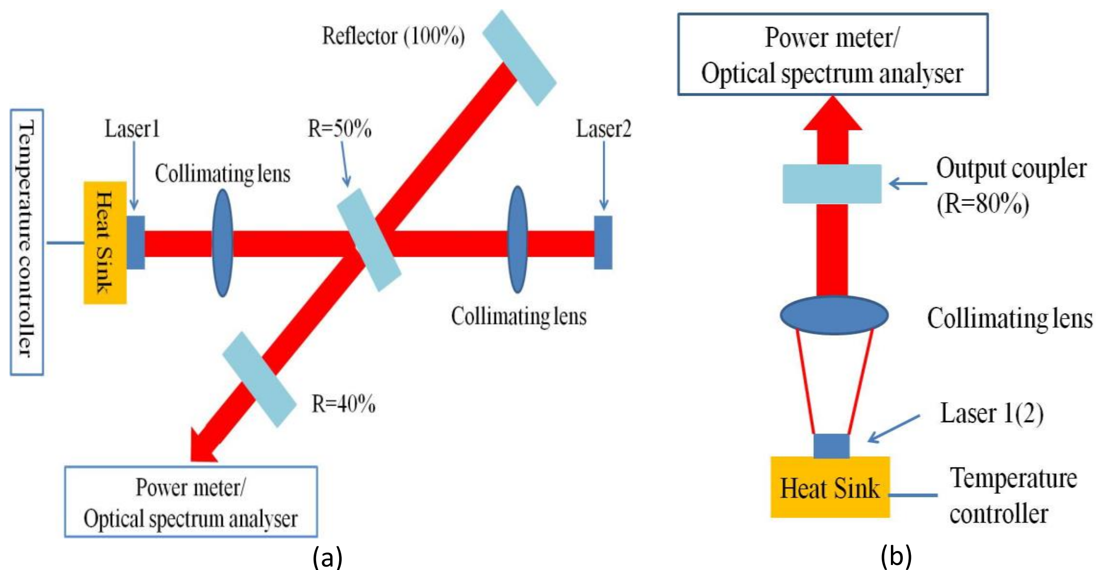


Figure 6.1 (a) Two 70 µm EP-VECSELs with an x-shaped cavity. (b) Linear cavity for measuring single device.

Figure 6.1(a) shows a schematic showing the role of the EP-VECSEL cavity in the cascaded laser system. To highlight the difference in the cascaded device, the linear cavity is also shown schematically in Fig. 6.1(b). In order to achieve power scaling through this system the cavity resonances need to be coincident as shown in the Fig. 6.2(b), while the linear cavity case is shown in Fig. 6.2(a). In the case of no additional loss within the cavity, then we would expect to double the output power with a cascade of 2 lasers. However, the addition of more optical elements, which have to be aligned perfectly and have no additional losses, means that a lower value can be expected in reality. For the case in Fig. 6.2(c) when we wish to operate the devices in dual wavelength emission mode, the cavity losses for each individual laser due to free-carrier absorption in the current spreading layer are doubled. A reduction in performance (as compared to individual lasers) is than therefore expected.

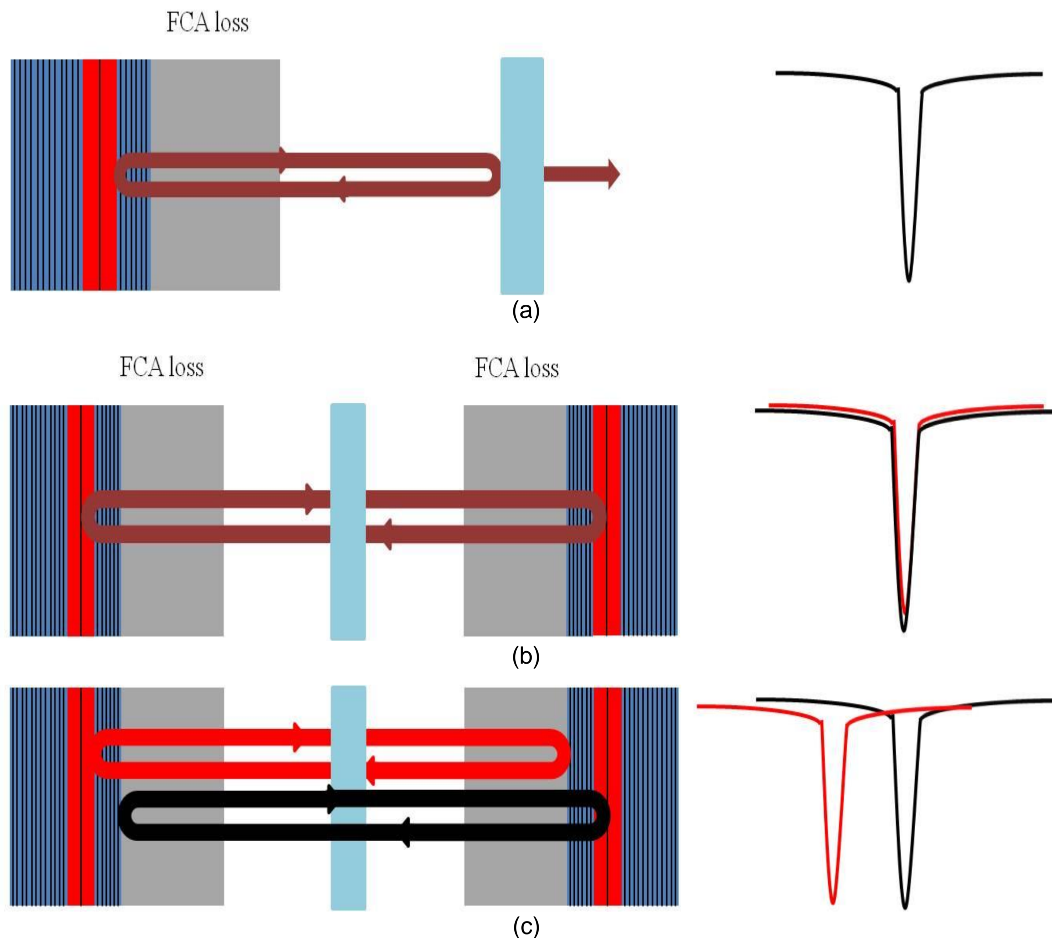


Figure 6.2 (a) Linear cavity of single EP-VECSEL, the current spreading layer will generate FCA loss, with the schematic diagram of cavity resonance spectra profile at right. (b) Cascaded dual EP-VECSELs cavity operated under same cavity resonant wavelength for power scaling. (c) Cascaded dual EP-VECSELs cavity operated with different cavity resonant wavelength; in this case the FCA loss will doubled, also with the schematic diagram of the mismatched cavity resonant at right.

In the following, I show how the wavelength variation of laser 1 and laser 2 is measured as a function of heat-sink temperature (laser 1) and Joule heating (both). Using a simple linear cavity, the individual lasers are characterised, and then assembled in the cascaded system. Within the system, their wavelengths are carefully matched and the effects of cascading on power scaling are explored. By varying the temperature of laser 1 the effect of operating in dual-wavelength mode is then investigated.

6.3 Results

Fig. 6.3(a) shows the V-I characteristics as a function of temperature dependent for laser 1 from 10 °C to 60 °C with an interval of 5 °C. Fig. 6.3(b) shows the corresponding L-I curves versus temperature of the same device. It can be calculated that laser 1 has a slope efficiency of ~0.56 W/A at 10 °C and this drops to ~0.37 W/A at 60 °C due to the detuning of the gain peak to the cavity resonance.

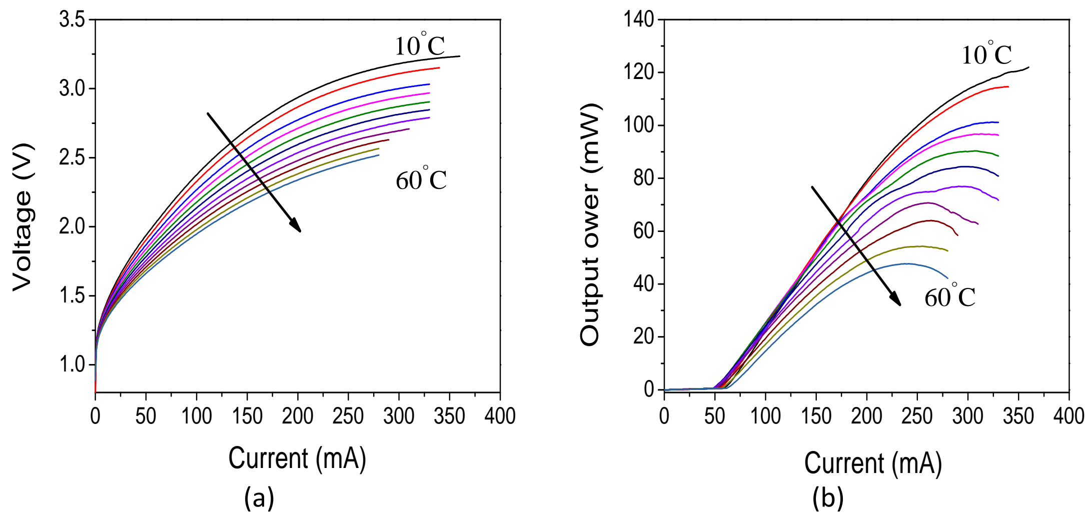


Figure 6.3 (a) V-I curves of laser 1 versus temperature from 10 °C to 60 °C with an interval of 5 °C. (b) Corresponding L-I curves of laser 1 versus temperature.

Fig. 6.4 plots the peak output power of laser 1 as a function of temperature obtained from Fig. 6.3(b). A maximum output power of 122 mW is measured at 10 °C and this value drops to 47.6 mW at 60 °C. The slope can be calculated using a linear fit which has a gradient of -1.44 mW/°C.

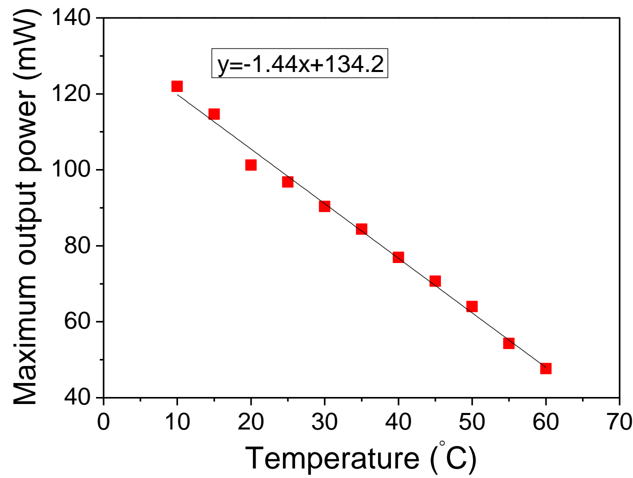


Figure 6.4 Maximum output power as a function of temperature of laser 1.

The following graph Fig. 6.5(a) plots the peak wavelength of laser 1 as a function of heat-sink temperature at a range of drive current. From 100 mA to 250 mA, the average wavelength shift of the device is 0.078 nm/°C. Fig. 6.5(b) shows the peak emission wavelength of laser 1 as a function of current at a range of temperatures. An average shift rate versus current can be calculated at 0.020 nm/mA.

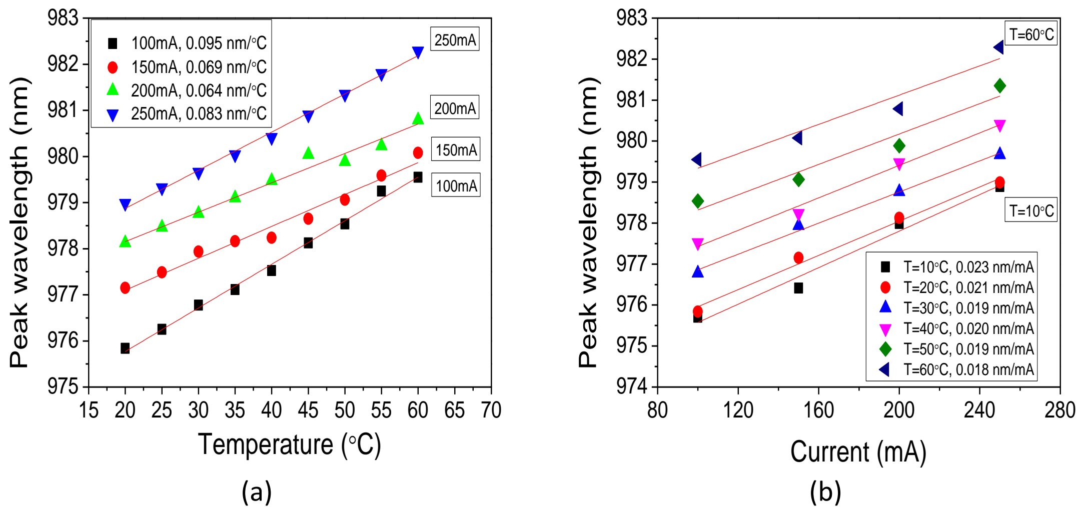


Figure 6.5 (a) Peak wavelength of laser 1 versus temperature at different current. (b) Peak emission wavelength of laser 1 versus current at different temperature.

The L-I-V curve of laser 2 was also measured at room temperature (not active cooling) and is plotted in Fig. 6.6. A maximum power is 92.1 mW obtained at 370 mA with a voltage of 3.0 V. The slope efficiency of this device is about ~0.43 W/A.

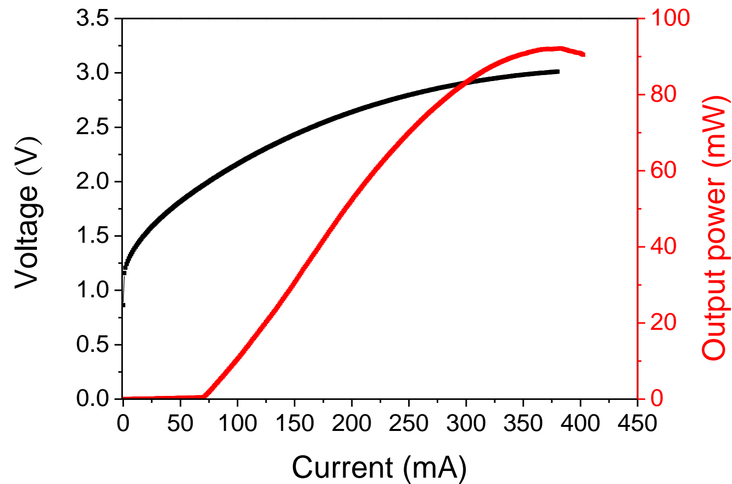


Figure 6.6 L-I-V curve of laser 2 under room temperature.

The peak emission wavelength of laser 2 as a function of current (heat-sink uncooled) is also shown in Fig. 6.7. The emission wavelength shifts at a rate of 0.020 nm/mA and this value is close to that obtained for laser 1.

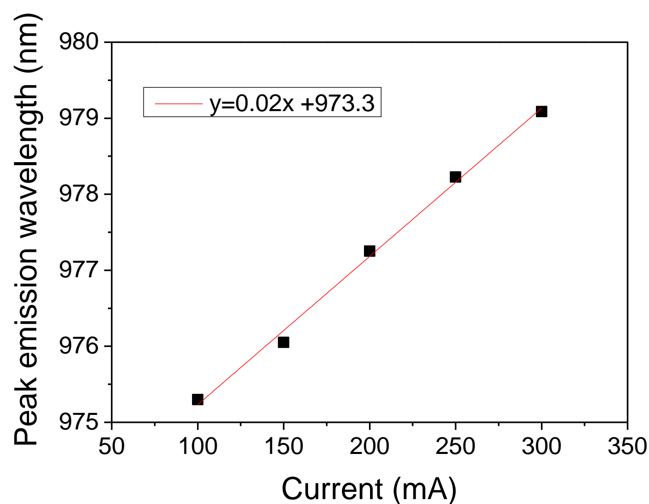
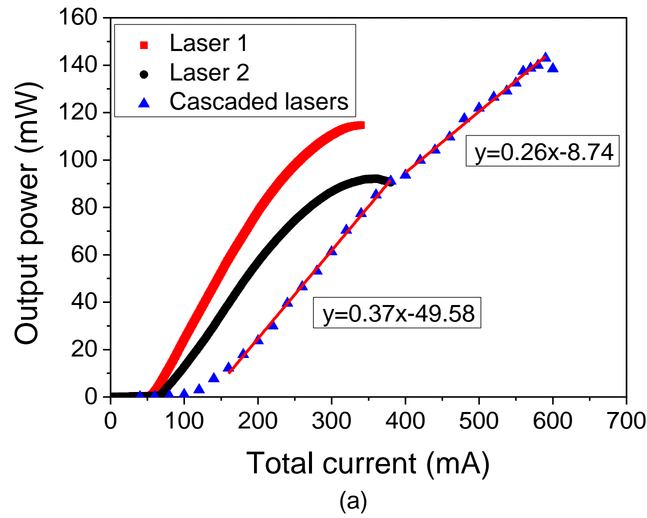


Figure 6.7 The peak emission wavelength of laser 2 versus current at room temperature.

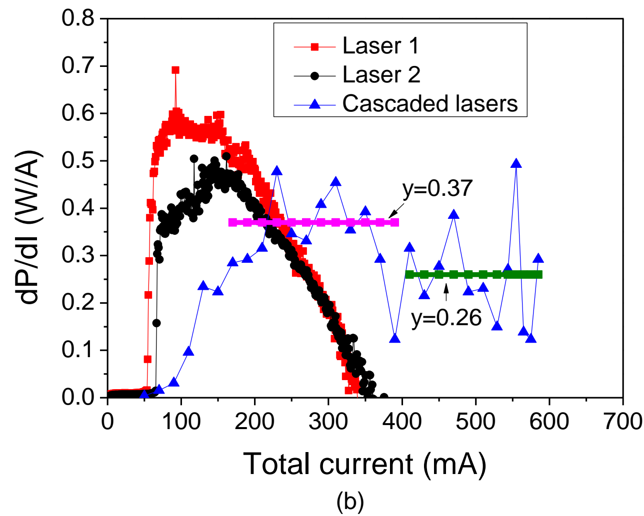
After measuring the characteristics of each individual device, the two lasers were assembled in the setup shown in Fig. 6.1. Figure 6.7 indicates that in the limit of zero current, the wavelength of laser 2 can be expected to be 973.3 ±0.2 nm. Characterisation of Laser 1 (shown in Fig 6.5) indicates that a temperature of 11.5° applied to laser 1 should result in coincidence of the two laser wavelengths. Experimentation around this value found a value of 15° to give highest powers. Various output couplers were tried and a maximal value of output power was obtained using a 40% reflectivity mirror. Considering the geometry of the laser this is equivalent to the 80% reflectivity output coupler found to be optimum for single linear cavity devices.

Fig. 6.8(a) shows the total output power of the two individual lasers versus current. The output power of the cascaded devices is also plotted in the same graph as a comparison. The maximum output power before thermal rollover of the cascaded lasers is 142.7 mW at 590 mA (295 mA for each), with laser 1 at a heat-sink temperature of 15 °C and laser 2 being at room temperature. It is noted that the current shown in the graph represents the total injection current for the two laser system, with half this value being applied to laser 1 and laser 2. At a drive current of 295 mA to laser 1 and laser 2 on their own in the linear cavity, powers of 109.5 and 85.7 mW were obtained. The cascaded laser system therefore provides 1.4 times the power of the individual lasers, indicating that this is a viable route to future power scaling. Compared to two devices using linear cavity, the cascading system can generate output beam with single emission wavelength due to the injection locking effect.

Fig. 6.8(b) shows the differential efficiency of the individual lasers and cascaded laser system as a function of current. The data is derived from that displayed in Fig. 6.8(a). For the individual lasers, clear evidence for the effect of thermal roll-over is observed beyond ~200mA, with a monotonic reduction in slope efficiency with increasing current. For the cascaded laser system, due to the noisiness of the differential efficiency data, two regions of the L-I characteristics in Fig 6.8(a) are identified. From 180 mA to 380 mA a slope efficiency of 0.37 W/A is obtained, and from 400mA to 590mA a value of 0.26 W/A. The lower slope efficiency is attributed to additional losses within the cavity increasing the round-trip losses (described in more detail later) [3], [13]. The observation of a reduction in slope efficiency beyond 200 mA per device is in line with characterisation of the individual devices. It is interesting to note that the differential efficiency of the cascaded devices (0.26 W/A) is a little higher than that observed for the individual devices at similar currents (0.21 W/A). Further work is required to investigate this observation.



(a)



(b)

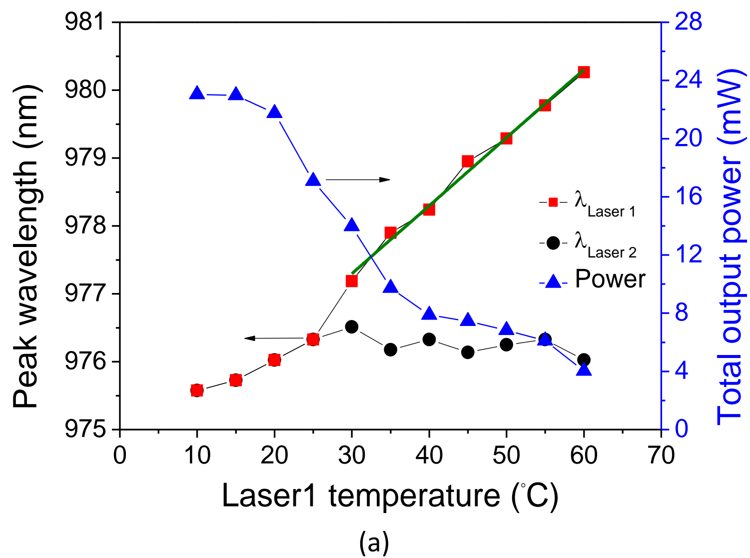
Figure 6.8 (a) Total output powers of two combined lasers versus total current and L-I curve of individual devices. (b) Corresponding dP/dI value of both single and cascaded lasers versus current.

Figure 6.9(a) plots the emission wavelength and output power of the cascaded system as a function of heat-sink temperature applied to laser 1. In doing so the detuning of the two cavities of the EP-VECSELs is increased. Both lasers were operated with drive currents of 100mA. It is noted that this experiment was performed at a different time to the previous data, and maximal power was found with laser 1 at 10 °C rather than the 15 °C used at that time. The difference may be due to poor temperature control of the

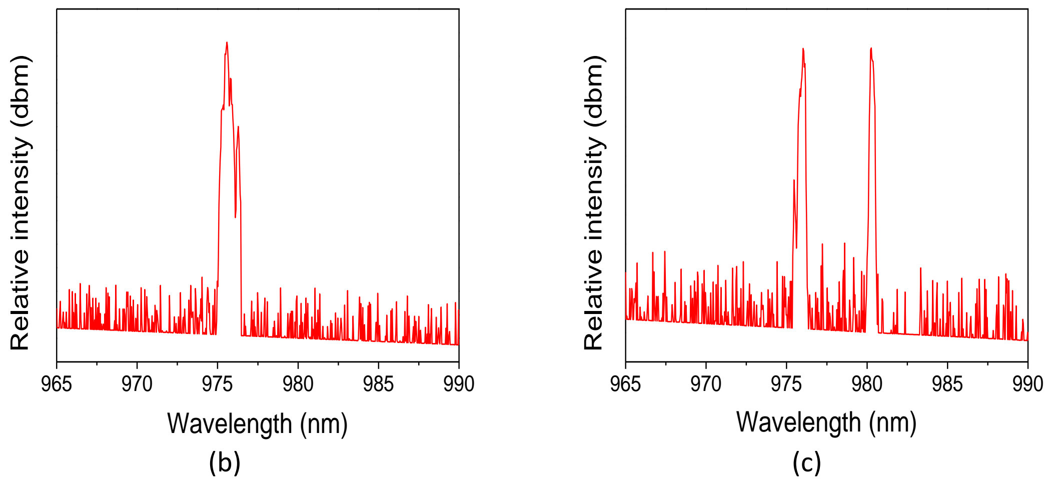
laboratory. Figure 6.9(b) shows the emission spectrum with laser 1 at 10 °C, whilst Fig 6.9(c) shows the emission spectrum with laser 1 at 60 °C.

The graphs may be considered in two regions. At low laser 1 temperature (<25 °C), the cavities are resonant, and the two lasers are injection locked. In this case the highest output powers are achieved and a higher power than that possible using a single laser is obtained. The injection locking of the two lasers is evidenced by the single emission wavelength and low rate of change of this wavelength with laser 1 temperature in the 10-25 °C regions.

At higher laser 1 temperatures, a dual emission peak is observed, with laser 1 shifting at a rate of 0.1 nm/ °C in agreement with data observed in Fig 6.5. Whilst laser 1 has a higher emission power, as temperature is increased it gradually reduces in intensity, and laser 2 dominates when laser 1 is at 60 °C. In the region when laser 1 is operated at a temperature >30 °C we can therefore consider the two lasers as independent lasers which share the same cavity, but are not injection locked. As discussed previously, with the two cavities out of resonance, the individual lasers are subject to higher losses than in the case of being on their own in a simple linear cavity.



(a)

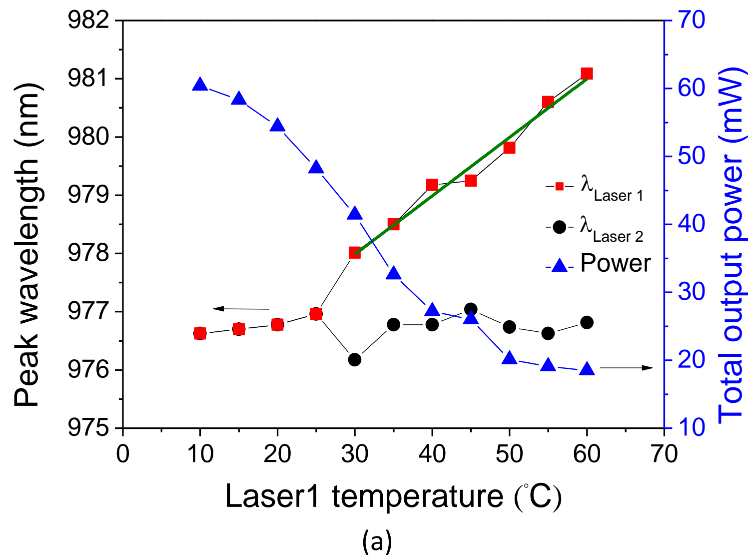


(b) (c)

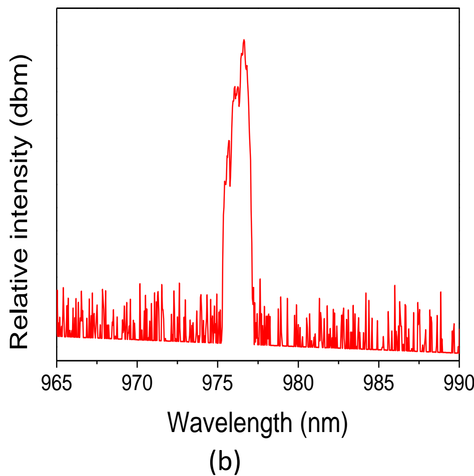
Figure 6.9 (a) Peak emission wavelength of the lasers versus the temperature of laser 1 at 200 mA (100 mA for each device). (b) Spectrum of the lasers at 10 °C. (c) Spectrum of the lasers at 60 °C.

Fig. 6.10(a) shows a similar data set with Fig. 6.9(a), but with the drive current to each laser now being 150mA. Two regions are observed clearly in the figure. When the laser 1 has a temperature below 25°C, two lasers are injection locked and have the same cavity resonant wavelength. Fig. 6.10(b) shows the single peak spectrum with injection locking. The cascaded laser gives 60.4 mW whilst the individual chips can be expected to produce 51.3 mW and 34.1 mW at the same time. Continuing increase the laser 1

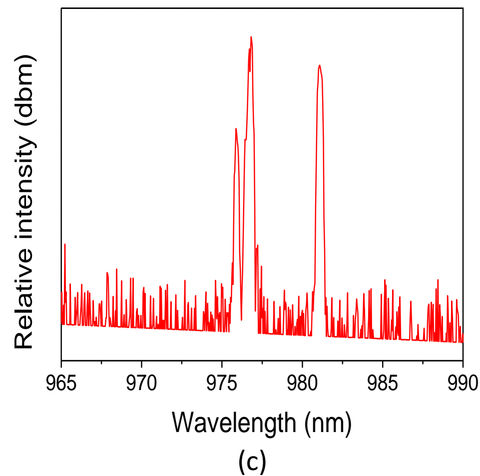
temperature after 30°C, no injection locking effect and two emission peaks appears as shown in Fig. 6.10(c).



(a)



(b)



(c)

Figure 6.10 (a) Peak emission wavelength of the lasers versus the temperature of laser 1 at 300 mA (150 mA for each device). (b) Spectrum of the lasers at 10 °C. (c) Spectrum of the lasers at 60 °C.

This notwithstanding, I am able to demonstrate a dual wavelength EP-VECSEL with tunable wavelength separation and 10's of mW of output power. This is achieved in a very different way to previous work that uses a single optically pumped VECSEL and an etalon [14–16]. The use of a single gain element may seem attractive, but it can lead to self-pulsation.

6.4 Summary

In this chapter a cascade EP-VECSEL system was realized using an asymmetric x-shaped cavity. By ensuring the cavities were resonant of the two EP-VECSELs 1.4 times the output power was obtained as compared to single devices in a linear cavity. Additional losses and non-ideal alignment are attributed to the inability to achieve a higher level of power scaling. Evidence for injection locking was presented. By varying the cavity resonances of the two EP-VECSELs, a dual wavelength cascaded EP-VECSEL system was demonstrated for the first time. Loss is again highlighted (this time free carrier loss in the current spreading layer) as a limiting factor in system performance.

6.5 Future Work

The cascading of EP-VECSELs has been shown to be possible, but continued work to optimize the single-mode EP-VECSELs remains a challenge. Once the limits of the device are achieved, then cascading may be applied. In general, work to reduce the number of n-DBRs would be beneficial for both the power scaling injection locked devices and for the dual wavelength cascaded system (as it would mean that internal loss is reduced).

For power scaling a simpler optical arrangement would need to be developed to partially automate the process in order to eliminate human error and reduce the cost of assembly. W and Z shaped cavities should also be considered. For the dual wavelength cascaded system, a higher intra-cavity power is required (if we wish to look to THz generation) requiring a trade-off between current spreading region loss (thickness, doping), and number of n-DBRs. The

optimal o/c reflectivity for both intra-cavity and extra-cavity power also needs further optimization.

Reference

[1] L. Fan, M. Fallahi, J. Hader, A. R. Zakharian, J. V Moloney, J. T. Murray, R. Bedford, W. Stolz, and S. W. Koch, “Multichip vertical-external-cavity surface-emitting lasers: a coherent power scaling scheme,” *Opt. Lett.*, vol. 31, no. 24, pp. 3612–3614, 2006.

[2] E. J. Saarinen, A. Härkönen, S. Suomalainen, and O. G. Okhotnikov, “Power scalable semiconductor disk laser using multiple gain cavity,” *Opt. Express*, vol. 14, no. 26, pp. 12868–12871, 2006.

[3] B. Rosener, M. Rattunde, R. Moser, C. Manz, K. Kohler, and J. Wagner, “GaSb-Based Optically Pumped Semiconductor Disk Laser Using Multiple Gain Elements,” *IEEE Photonics Technol. Lett.*, vol. 21, no. 13, pp. 848–850, 2009.

[4] S. Operation, S. Kaspar, M. Rattunde, T. Tino, S. Adler, C. Manz, K. Klaus, and J. Wagner, “Recent Advances in 2- μ m GaSb-Based Semiconductor Disk Laser — Power Scaling , Narrow-Linewidth and Short-Pulse Operation,” *IEEE J. Sel. Top. QUANTUM Electron.*, vol. 19, no. 4, 2013.

[5] A. Hein, F. Demaria, A. Kern, S. Menzel, F. Rinaldi, R. Rösch, and P. Unger, “Efficient 460-nm second-harmonic generation with optically pumped semiconductor disk lasers,” *IEEE Photonics Technol. Lett.*, vol. 23, no. 3, pp. 179–181, 2011.

[6] A. J. Maclean, A. J. Kemp, J. Y. Kim, K. S. Kim, T. Kim, M. D. Dawson, and D. Burns, “Continuous tuning and efficient intracavity second-harmonic generation in a semiconductor disk laser with an intracavity diamond heatspreader,” *IEEE J. Quantum Electron.*, vol. 44, no. 3–4, pp. 216–225, 2008.

[7] U. Keller and A. C. Tropper, “Passively modelocked surface-emitting semiconductor lasers,” *Phys. Rep.*, vol. 429, no. 2, pp. 67–120, 2006.

[8] A. Aschwanden, D. Lorenser, H. J. Unold, R. Paschotta, E. Gini, and U. Keller, “10 GHz passively mode-locked external-cavity semiconductor laser with 1.4 W average output power,” *Appl. Phys. Lett.*, vol. 86, no. 13, pp. 1311021–1311023, 2005.

[9] Z. Zhao, S. Bouchoule, J.-C. Harmand, G. Patriarche, G. Aubin, and J.-L. Oudar, “Recent advances in development of vertical-cavity based short pulse source at 1.55 μm,” *Front. Optoelectron.*, vol. 7, no. 1, pp. 1–19, 2014.

[10] C. Hessenius, M. Lukowski, and M. Fallahi, “High-power tunable two-wavelength generation in a two chip co-linear T-cavity vertical external-

cavity surface-emitting laser," *Appl. Phys. Lett.*, vol. 101, no. 12, pp. 1211101–3, 2012.

[11] M. Scheller, J. M. Yarborough, J. V Moloney, M. Fallahi, M. Koch, and S. W. Koch, "Room temperature continuous wave milliwatt terahertz source.," *Opt. Express*, vol. 18, no. 26, pp. 27112–27117, 2010.

[12] J. R. Orchard, D. T. D. Childs, L. C. Lin, B. J. Stevens, D. M. Williams, and R. A. and Hogg, "Design Rules and Characterisation of Electrically Pumped Vertical External Cavity Surface Emitting Lasers," *Jpn. J. Appl. Phys.*, vol. 50, no. 4, Apr. 2011.

[13] M. Kuznetsov, F. Hakimi, R. Sprague, and A. and Mooradian, "Design and characteristics of high-power (0.5-W CW) diode-pumped vertical-external-cavity surface-emitting semiconductor lasers with circular TEM00 beams," *IEEE Photonics Technol. Lett.*, vol. 5, no. 3, pp. 561–573, 1999.

[14] T. Leinonen, Y. A. Morozov, A. Härkönen, and M. Pessa, "Vertical External-Cavity Surface-Emitting Laser for Dual-Wavelength Generation," *IEEE Photonics Technol. Lett.*, vol. 17, no. 12, pp. 2508–2510, 2005.

[15] L. Fan, M. Fallahi, J. Hader, A. R. Zakharian, J. V. Moloney, W. Stolz, S. W. Koch, R. Bedford, and J. T. Murray, "Linearly polarized dual-wavelength vertical-external-cavity surface-emitting laser," *Appl. Phys. Lett.*, vol. 90, no. 18, pp. 1811241–3, 2007.

[16] T. Leinonen, S. Ranta, A. Laakso, Y. Morozov, M. Saarinen, and M. Pessa, "Dual-wavelength generation by vertical external cavity surface-emitting laser," *Opt. Express*, vol. 15, no. 20, pp. 13451–13456, 2007.

7. Summary and Future Works

7.1 Summary

In this thesis, I have presented and analysed results related to EP-VECSELs with substrate emitting geometry at 980 nm.

In chapter 2, the characteristic of DBRs have been simulated using CAMFR software. The reflectivity spectra versus DBR numbers have been plotted in order to determine the number of DBR pairs used in wafer. Also, the series resistance in DBRs needs to be minimised while maintain its optical performance, thus an intermediate layer of 10 nm thick of $Al_{0.47}Ga_{0.53}As$ has been used. The intra-cavity with periodic gain structure (PGS) has been applied and the optical confinementis shown to increase 1.8 times.

In chapter 3, the development of fabrication processes for EP-VECSELs was described. The main steps such as photolithography, dielectric layer deposition; dry etching by ICP and RIE, and metal deposition to form electrical contacts has been described in detail. The recipe parameters for trench etching processes have been investigated. A trench with a straight side wall can be obtained; a coherent deposition of the dielectric layer has been achieved by increasing the deposition layer thickness from 400 nm to 800 nm. The circular transmission line measurement (CTLM) method was used to optimize the contacts of the device. Annealing tests under different annealing temperatures have been carried out and the contact resistance has been optimised at 360 °C. As a next step, the annealing temperature test can be continued by reducing the temperature step from 20°C to 5°C around 360°C.

Thus a new annealing temperature with smaller contact resistance maybe obtained.

In chapter 4, several measurement techniques for EP-VECSELs have been introduced. The L-I-V and spectrum measurements of linear cavity EP-VECSELs were presented. A maximum power of 80.6 mW with a slope efficiency of 0.283 W/A was achieved from a 90 µm diameter device using 80% output coupler. Then the effect of detuning on the device performance has been discussed. A etch/measurement method to determine the value of detuning across the whole wafer has been demonstrated. The beam quality (M^2) measurement has been used and a M^2 =1.35 has been measured at low power for my devices. Also, electroluminescence (EL) mapping has been applied for measuring the light intensity distribution in device which allows a measurement of the carrier distribution in the active element of the device. In future, devices with improved structure as set out in chapter's can be used for beam quality measurement to obtain lower M^2. Those devices can also be used for EL mapping, to confirm simulation results.

In chapter 5, a model to determine the carrier distribution for substrate emission EP-VECSEL has been constructed using Rsoft Lasermod software. This model has been calibrated by comparing the simulation and EL mapping results from the previous chapter, the effects of contact misalignment are not only taken into account, but add confidence in the applicability of the modelling. The validity of this model is confirmed due to the excellent agreement between simulation and experiment. Subsequently, various parameters have been investigated to enhance the single transverse mode

output of EP-VECSELs. Results have shown that a 40-60 μm thick substrates with optimal doping level will improve the intensity profile. Also, the etched trench has provided two conclusions. Firstly, for standard fabrication trench etch depths, the trench etch is deleterious. Secondly, if very deep etches are possible, then if the etch penetrates into the substrate for a significant depth, one can expect an improvement in the carrier distribution profile.

In chapter 6, a dual chip, cascaded EP-VECSELs system has been demonstrated by using an asymmetric x-shaped cavity. One of the devices is wavelength tuned by the heat sink temperature and the other is tuned by self-heating alone. Compared to a single device, 1.4 times the total output power has been achieved. This is lower than the ideal x2 case due to FCA loss and non-ideal alignment in the system that limits power scaling to a higher level. Also, injection locking has been observed when two lasers have the same cavity resonant wavelength. Furthermore, a dual wavelength cascaded EP-VECSELs system can be obtained by changing the heat-sink temperature to make the cavity resonant wavelength of two devices are sufficiently different to avoid mutual injection locking.

7.2 Future works

In order to improve the EP-VECSELs performance, some work can be considered as next step.

In chapter 2, Simulation results showed that the centre wavelength of the reflectivity spectra has a minimum when the DBR pairs are equal on both

sides of the active region. The possible use of such structures in wafer characterisation for VCSEL/EP-VECSELs is highlighted.

In chapter 5, an optimisation of the structure should be performed with no trench etch. The trench etch appears to deteriorate the carrier distribution profile. As the n-DBR pairs do not affect the EL-intensity profile, they can be reduced in order to make the charge carrier profile more sensitive to external feedback. Also, this model can be extended to use oxide confinement layers and implantation.

In chapter 6, in order to continue to optimize the cascaded system, the devices with fewer n-DBR pairs can be used in order to reduce the internal loss. Also, a W and Z shaped cavities should be considered in attempt to reduce the alignment loss in the cavity. For THz generation from dual wavelength, high intra-cavity power is needed and the trade-off between FCA loss and number of n-DBRs should be considered.

Appendix A

TS728-3 (980 nm)

Material	Repeats	Thickness (A)	Doping (cm^{-3})
GaAs		2000	1×10^{19}
GaAs	32	600	2×10^{18}
$Al_{0.47}Ga_{0.53}As$	32	100	2×10^{18}
$Al_{0.8}Ga_{0.2}As$	32	737	2×10^{18}
$Al_{0.47}Ga_{0.53}As$	32	100	2×10^{18}
GaAs		1080	UD
$GaAs_{0.9}P_{0.1}$		150	UD
$In_{0.148}Ga_{0.852}As$	2	80	UD
$AlAs_{0.9}P_{0.1}$	2	90	UD
$In_{0.148}Ga_{0.852}As$		80	UD
$AlAs_{0.9}P_{0.1}$		150	UD
GaAs		680	UD
$GaAs_{0.9}P_{0.1}$		150	UD
$In_{0.148}Ga_{0.852}As$		80	UD
$AlAs_{0.9}P_{0.1}$	2	90	UD
$In_{0.148}Ga_{0.852}As$	2	80	UD
$GaAs_{0.9}P_{0.1}$		150	UD
GaAs		1080	UD
$Al_{0.8}Ga_{0.2}As$	12	737	2×10^{18}
$Al_{0.47}Ga_{0.53}As$	12	100	4×10^{18}
GaAs	12	600	2×10^{18}
$Al_{0.47}Ga_{0.53}As$	12	100	4×10^{18}
GaAs			n^+

UD: un-doped

Appendix B

Prepared by: X Jin

Date:

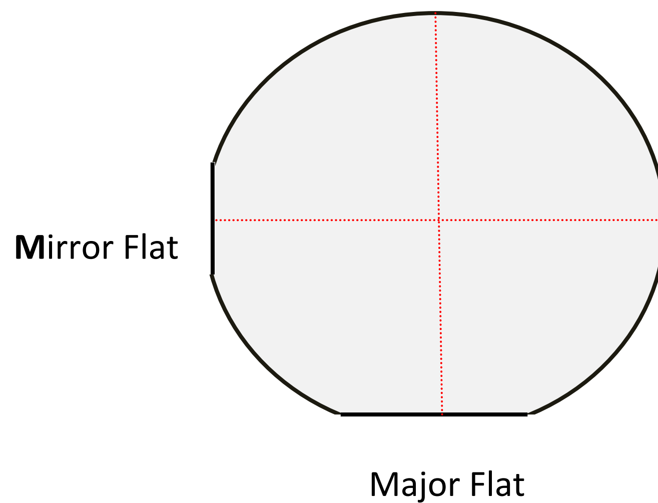
Title: VCSEL/VECSEL-Batch

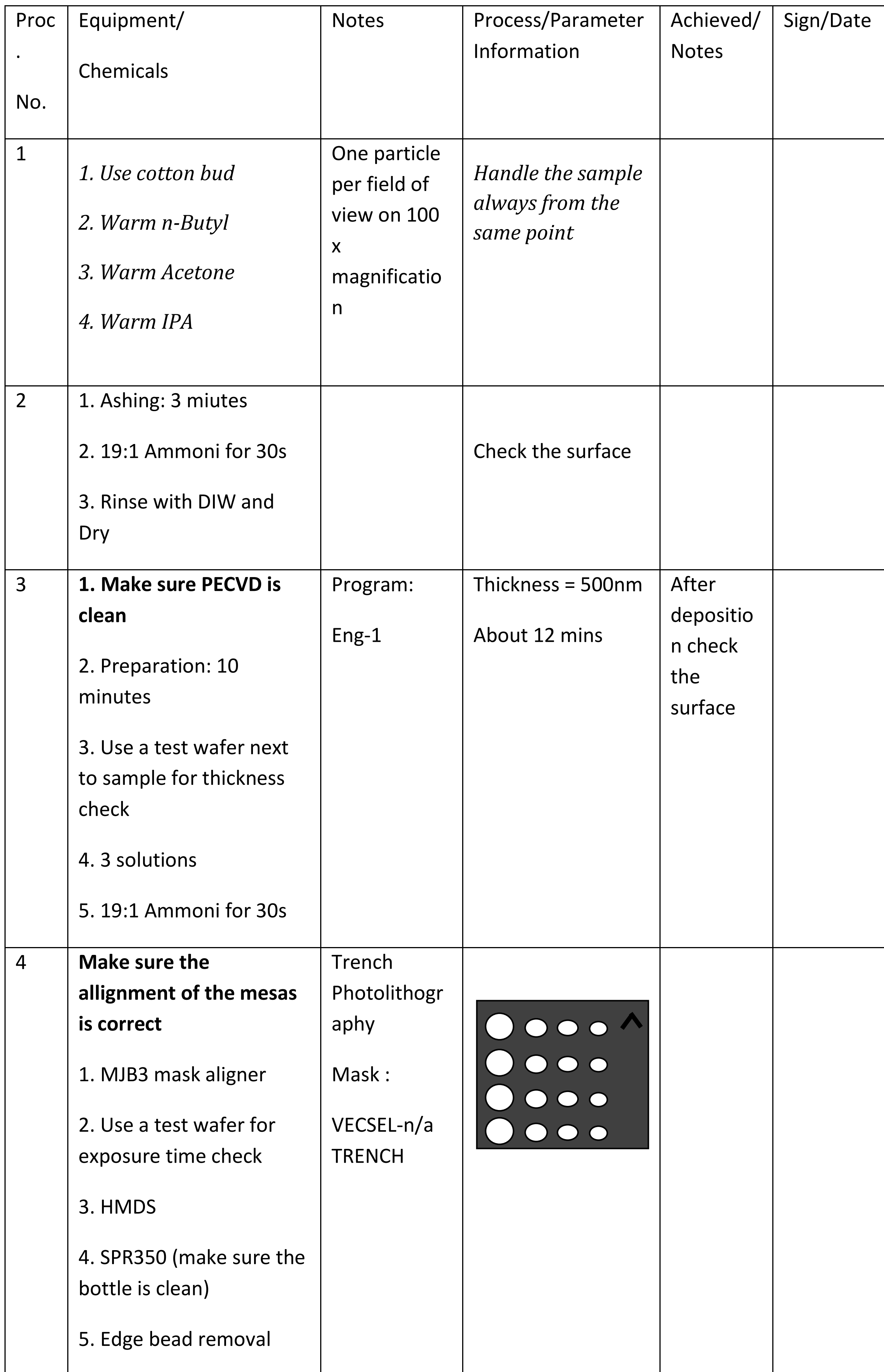
For:

Start date:

Finish date:

- Mark the position of the cut piece with respect to the wafer
- Mark the direction of Major axis or the centre of the wafer if the sample is square shape using scriber (smal mark)





Proc. No.	Equipment/ Chemicals	Notes	Process/Parameter Information	Achieved/ Notes	Sign/Date
1	*1. Use cotton bud* *2. Warm n-Butyl* *3. Warm Acetone* *4. Warm IPA*	One particle per field of view on 100 x magnification	*Handle the sample always from the same point*		
2	1. Ashing: 3 miutes 2. 19:1 Ammoni for 30s 3. Rinse with DIW and Dry		Check the surface		
3	**1. Make sure PECVD is clean** 2. Preparation: 10 minutes 3. Use a test wafer next to sample for thickness check 4. 3 solutions 5. 19:1 Ammoni for 30s	Program: Eng-1	Thickness = 500nm About 12 mins	After deposition check the surface	
4	**Make sure the allignment of the mesas is correct** 1. MJB3 mask aligner 2. Use a test wafer for exposure time check 3. HMDS 4. SPR350 (make sure the bottle is clean) 5. Edge bead removal	Trench Photolithography Mask : VECSEL-n/a TRENCH			

<table>
<tr><td></td><td>If exposure is fine do 2 minutes of Ashing before ICP & check</td><td></td><td></td><td></td><td></td></tr>
<tr><td>5</td><td>ICP: Hard Mask etch
1. Clean ~ 10 minutes
2. Preparation: 10 minutes
Use end point</td><td>Etch time: 25 min for 500nm</td><td colspan="2"><table>
<tr><td>CHF_3</td><td>20</td><td>sccm</td></tr>
<tr><td>Ar</td><td>30</td><td>sccm</td></tr>
<tr><td>RF power</td><td>200</td><td>W</td></tr>
<tr><td>Pressure</td><td>8</td><td>mTorr</td></tr>
<tr><td>Set</td><td>25</td><td>mTorr</td></tr>
<tr><td>FP</td><td>0</td><td></td></tr>
</table></td><td></td></tr>
<tr><td>6</td><td>1. DekTek to measure the depth
2. Asher: 5 minutes
3. Resist stripper on 100°C
4. plate: 3 minutes
5. Rince in warm IPA
6. 3- solution clean</td><td></td><td colspan="2"></td><td></td></tr>
<tr><td>7</td><td>Semiconductor etch
1. Clean ~ 10 minutes
2. Preparation: 10 minutes
3. Use end point
4. SEM Check for new structures</td><td>Recipe: GaAs-6
Etch time: about 20 mins</td><td colspan="2"><table>
<tr><td>$SiCl_4$</td><td>4</td><td>sccm</td></tr>
<tr><td>Ar</td><td>2</td><td>sccm</td></tr>
<tr><td>RF</td><td>150</td><td>W</td></tr>
<tr><td>ICP</td><td>200</td><td>W</td></tr>
<tr><td>Pressure</td><td>1</td><td>mTorr</td></tr>
<tr><td>Temp</td><td>20</td><td>DegC</td></tr>
</table></td><td></td></tr>
<tr><td>8</td><td>1. DekTek to measure the depth
2. Ashing: 3 miutes</td><td></td><td></td><td></td><td></td></tr>
<tr><td>9</td><td>ICP: Hard Mask etch
1. Clean ~ 10 minutes
2. Preparation: 10 minutes</td><td>Etch time: 25 min for 500nm</td><td colspan="2"></td><td></td></tr>
</table>

<table>
<tr><td></td><td>Use end point

Ashing: 3 miutes after etching</td><td></td><td colspan="2"><table><tr><td>CHF_3</td><td>20</td><td>sccm</td></tr><tr><td>Ar</td><td>30</td><td>sccm</td></tr><tr><td>RF power</td><td>200</td><td>W</td></tr><tr><td>Pressure</td><td>8</td><td>mTorr</td></tr><tr><td>Set</td><td>25</td><td>mTorr</td></tr><tr><td>FP</td><td>0</td><td></td></tr></table></td><td></td></tr>
<tr><td>10</td><td>1. Make sure PECVD is clean

2. Preparation: 10 minutes

3. Program with a test wafer in the chamber

4. 3 solutions

5. 19:1 Ammoni for 30s</td><td>Check the deposition rate

Using the test wafer</td><td>Program: Eng-1

Deposite thickness= 800 nm

About 19 mins</td><td>After depositio n check the surface</td><td></td></tr>
<tr><td>11</td><td>1. MJB3 mask aligner

2. Use a test wafer for exposure time check

3. HMDS

4. SPR200 (make sure the bottle is clean)

5. Edge bead removal</td><td></td><td>Widow Photolithography

Mask:

VECSEL-SHEF1 WINDOW

Follow lithography with 1 min O_2 plasma ash.</td><td></td><td></td></tr>
<tr><td>12</td><td>ICP: Hard Mask etch

1. Clean ~ 10 minutes

2. Preparation: 10 minutes

Use end point</td><td>Etch time: 35 min for 800nm</td><td colspan="2"><table><tr><td>CHF_3</td><td>20</td><td>sccm</td></tr><tr><td>Ar</td><td>30</td><td>sccm</td></tr><tr><td>RF power</td><td>200</td><td>W</td></tr><tr><td>Pressure</td><td>8</td><td>mTorr</td></tr><tr><td>Set</td><td>25</td><td>mTorr</td></tr><tr><td>FP</td><td>0</td><td></td></tr></table></td><td></td></tr>
<tr><td>13</td><td>1. Asher: 5 minutes

2. Resist stripper on 100°C</td><td></td><td></td><td></td><td></td></tr>
</table>

<table>
<tr><td></td><td>3. plate: 3 minutes
4. Rince in warm IPA
5. 3- solution clean</td><td></td><td></td><td></td><td></td></tr>
<tr><td>14</td><td>1. MJB3 mask aligner
2. Use a test wafer for exposure time check
3. HMDS
4. SPR200 (make sure the bottle is clean)
5. Edge bead removal</td><td></td><td>Metal Photolithography
Mask:
VECSEL-SHEF1 WINDOW
Follow lithography with 1 min O_2 plasma ash.</td><td></td><td></td></tr>
<tr><td>15</td><td>Thermal Evaporator</td><td>19:1 Ammonia
Wash before deposition</td><td colspan="2">Top Contact 1
<table><tr><th>Metal</th><th>Aim</th><th>Achiev</th></tr><tr><td>Au</td><td>5</td><td></td></tr><tr><td>Zn</td><td>10</td><td></td></tr><tr><td>Au</td><td>200</td><td></td></tr></table></td><td></td></tr>
<tr><td>16</td><td>1. n-Butyl
2. Acetone
3. IPA</td><td></td><td>Lift Off in acetone
3 stage clean</td><td></td><td></td></tr>
<tr><td>17</td><td>RTA:Furn360-1</td><td></td><td>Anneal: Furn360-2 program</td><td></td><td></td></tr>
<tr><td>18a</td><td>Mount on glass thinning block using wax along with small pieces of spacer wafer.</td><td>BacksideThining
Be aware of uniformity, and allow for wax in thickness measurement.
Followed by good clean (using</td><td colspan="2">Logitech lapper/polisher
<table><tr><th>Min</th><th>Aim</th><th>Max</th></tr><tr><td>110um</td><td>100um</td><td>85um</td></tr><tr><td>A</td><td>B</td><td>C</td></tr></table></td><td></td></tr>
</table>

<table>
<tr><td></td><td></td><td>carriers).</td><td></td><td></td></tr>
<tr><td>18b</td><td>Logitech lapper/polisher</td><td></td><td>Backside Polishing
2 min @ 60rpm using CHEMLOX polish solution and polish wheel</td><td></td></tr>
<tr><td>19</td><td>Wet etch</td><td></td><td>Wet Etch
10ml of each chemical for 1:1:1 etch + 30ml water place samples still mounted on thinning block in solution for 2.5 mins. Then un-mount samples from glass blocks</td><td></td></tr>
<tr><td>20</td><td>MJB3 mask aligner
-HMDS adhesion promoter
Resist: BPRS100</td><td>Mount p-side down on glass cover slip, use HMDS adhesion promoter</td><td>BACK CONTACT PHOTOLITHOGRAPHY
Mask plate: VECSEL-SHEF2 BACKCONTACT</td><td></td></tr>
<tr><td>21</td><td>Thermal Evaporator</td><td>19:1 Ammonia wash before placeing sample in machine</td><td>Bottom Contact: InGe/Au<table><tr><th>Metal</th><th>Aim (nm)</th><th>Achieved</th></tr><tr><td>InGe</td><td>20</td><td></td></tr><tr><td>Au</td><td>200</td><td></td></tr></table></td><td></td></tr>
<tr><td>22</td><td>- 3 stage clean</td><td></td><td>- Lift Off in acetone
- 3 stage clean</td><td></td></tr>
<tr><td>23</td><td>RTA</td><td></td><td>Anneal: Furn360-1 program</td><td></td></tr>
<tr><td>24</td><td>PECVD</td><td>-3 stage clean 19:1 Ammonia before deposition</td><td>Nitride Deposition: NITRIDE program
Desired thickness: 127nm</td><td></td></tr>
</table>