Modelling, Diagnosis, and Fault-Tolerant Control of Open-Circuit Faults in Three-Phase Two-Level PMSM Drives

Zeliang Zhang

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University of York

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Abstract

Attributing to the high efficiency, compact structure, and rapid dynamics, powertrains utilizing Permanent Magnet Synchronous Motors (PMSM) have emerged as a promising alternative and have seen extensive deployment in various industrial and transportation sectors, including electric vehicles (EVs), more-electric aircraft, and robotics. Despite ongoing interest in advanced redundant topologies for PMSM drives from both academia and industry, the three-phase two-level (3P2L) PMSM drive continues to dominate the majority of the electric drive market. However, when compared to its multi-phase counterparts, the most-commonly used 3P2L PMSM drive exhibits limited reliability and fault tolerance capabilities, particularly in safety-critical or cost-sensitive scenarios. Therefore, the development of embedded reliability-enhancing techniques holds great significance in enhancing the safety and maintenance of on-site powertrains based on the 3P2L PMSM drive.

The purposes of this study are to investigate post-fault system models and develop hardware-free fault diagnostic and fault-tolerant methods that can be conveniently integrated into existing 3P2L PMSM drives. Special attention is dedicated to the open-circuit fault, as it represents one of the ultimate consequences of fault propagation in PMSM drives.

In the first place, the fault propagation from component failures to open-circuit faults is analyzed, and the existing literature on the modelling, diagnosis, and fault-tolerant control of PMSM drives is comprehensively reviewed. Subsequently, the study delves into the post-fault system model under the open-phase (OP) fault, which includes the examination of post-fault phase voltages and current prediction. Based on the phase voltages observed under the OP fault, a phenomenon of particular interest is modelled: the remaining current that flows through the free-wheeling diodes of the faulty phase under the open-switch (OS) fault. The conduction mechanism is elucidated, and a real-time estimation model is established. Furthermore, a sampling method is designed to enable the motor drive to detect the remaining current in the OS phase, along with a set of diagnostic rules to distinguish between OS and OP faults. Finally, an embedded fault-tolerant control method is introduced to enhance the post-fault speed and torque outputs of 3P2L PMSM drives.

Keywords: PMSM; powertrain; fault modelling; diagnosis; fault-tolerant control.

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Declaration

I declare that this thesis is a presentation of original work and I am the sole author. This work has not previously been presented for an award at this, or any other, University. All sources are acknowledged as References.

The main contents of Chapter 3 have been submitted to IECON 2023. The title is "An Improved Current Prediction Model for PMSM Drives under Single Open-Phase Fault Considering Floating Motor Neutral".

The main contents in Chapter 4 have been published in *IEEE Transactions on Power Electronics* vol. 38, no. 8, pp. 10104-10115, Aug. 2023. The title is "Analysis and Real-Time Calculation of Postfault Current of Standard Surface-Mounted PMSM Drives with Dysfunctional Power Switches".

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List of Publications

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[2] **Z. Zhang**, Y. Hu, G. Luo, C. Gong, X. Liu, and S. Chen, "An Embedded Fault-Tolerant Control Method for Single Open-Switch Faults in Standard PMSM Drives," in *IEEE Transactions on Power Electronics*, vol. 37, no. 7, pp. 8476-8487, July 2022.

[3] **Z. Zhang**, G. Luo, Z. Zhang, and X. Tao, "A hybrid diagnosis method for inverter open-circuit faults in PMSM drives," in *CES Transactions on Electrical Machines and Systems*, vol. 4, no. 3, pp. 180-189, Sept. 2020.

[4] **Z. Zhang**, Y. Hu, X. Chen, G. W. Jewell, and H. Li, "A Review on Conductive Common-Mode EMI Suppression Methods in Inverter Fed Motor Drives," in *IEEE Access*, vol. 9, pp. 18345-18360, 2021.

[5] **Z. Zhang**, etc., "An Improved Current Prediction Model for PMSM Drives under Single Open-Phase Fault Considering Floating Motor Neutral," in *IECON 2023 - 49th Annual Conference of the IEEE Industrial Electronics Society*, Singapore, Oct. 2023. (Accept)

[6] **Z. Zhang**, Y. Hu, C. H. T. Lee, G. Luo, and C. Gong, "Identifying Post-Fault States and Distinguishing Open-Circuit Faults with Functional and Dysfunctional Free-Wheeling Diodes in PMSM Drives,". A chance of a 6-week revision given by *IEEE Transactions on Power Electronics*.

[7] X. Liu, C. Liu, **Z. Zhang**, Y. Li, and G. Luo, "A Novel method of Phase current reconstruction with single DC-Link current sensor for Tri-phase Full Bridge Inverter," 2022 25th International Conference on Electrical Machines and Systems (ICEMS), Chiang Mai, Thailand, 2022, pp. 1-6, doi: 10.1109/ICEMS56177.2022.9982803.

Nomenclature

B	Damping coefficient
CNT_{delay}	Counting value of the sampling delay
CNT_{ts}	Counting value of a switching period
CNT_{samp}	Counting value at which the current sampling starts
DR_{max}	Maximum duty ratio in three phases
DR_{med}	Medium duty ratio in three phases
DR_{min}	Minimum duty ratio in three phases
$D_{1, \ldots, 6}$	Six diodes in inverters
$Flag(D)$	Diagnostic flag
i_a, i_b, i_c	Phase currents of the motor
i_{a_H}	Phase A current under the healthy condition
i_{a_OP}, i_{b_OP}, i_{c_OP}	Phase currents of the motor under the OP fault
i_{a_OS}, i_{b_OS}, i_{c_OS}	Phase currents of the motor under the OS fault
i_{a_meas}, i_{b_meas}	Measured phase A and B currents
i_{a_cal}, i_{b_cal}	Calculated phase A and B currents
i_{a_samp}	Sampled phase A current
$i_{a\_samp}^{nom}$	Phase A current sampled by the regular sampling current
i_{a_resi}	Residual error between sampled and estimated Phase A current
i_{a_value}	Phase a value under any condition
i_b^f	Phase B currents under the single OS fault
$i_{b\_OP}^k$, $i_{c\_OP}^k$	Phase currents of the motor under the OP fault at the current step
$i_{b\_OP}^{k+1}$, $i_{c\_OP}^{k+1}$	Phase currents of the motor under the OP fault at the next step
i_d,i_q	d, q-axis currents
i_{d_H},i_{q_H}	d, q-axis currents under the healthy condition
i_d^f, i_q^f	d, q-axis currents under the single OS fault
i_d^k, i_q^k	d, q-axis currents at the current step

i_d^{k+1}, i_q^{k+1}	d, q-axis currents at the next step
$i_{d\_OP}^{k+1}$, $i_{q\_OP}^{k+1}$	d, q-axis currents under the OP fault at the next step
i_{d_OS}, i_{q_OS}	d, q-axis currents under the OS fault
i_d^*, i_q^*	d, q-axis current references
i_d^{*f}, i_q^{*f}	d, q-axis current references under the single OS fault
$\hat{i}_{a\_OS}$	Estimated phase A current under the OS fault
Δi_{a_OS}	Increment of Estimated phase A current under the OS fault
I_s	Amplitude of the current vector
I_{peak}	Repetitive peak current of the power device
J	Rotor inertia
L_s, L_d, L_q	Phase inductance and d, q-axis inductances
$L()$	Polarity of a value
M	Mutual inductance between phases
n	Motor speed feedback
n^*	Motor speed reference
p	Number of pole pairs
R_s	Resistance of phase windings
$Speed_{OS}$, $Speed_{OP}$	Speed responses under OS and OP faults
t_1, t_2	Acting time of the first and second voltage vectors in each spatial sector
t_1^f, t_2^f	Acting time of the first and second voltage vectors in each spatial sector under the single OS fault
$\triangle t_{D1}$	Conduction time of diode D_1 in each switching period
$\triangle t_{D2}$	Conduction time of diode D_2 in each switching period
T_{cm1}, T_{cm2}, T_{cm3}	Three-phase modulation signals
T_d	Dead time of power switches
T_e	Electromagnetic torque
T_{e_OS}, T_{e_OP}	Electromagnetic torque under OS and OP faults
T_e^f	Electromagnetic torque under the single OS fault
$Time(D)$	Diagnostic time

T_L	Load torque
T_s	Switching period
T_{vx}	Acting time of a voltage vector
T_x, T_y	Acting times of voltage vectors in each spatial sector
$T_{1, \ldots, 6}$	Six power switches in inverters
u_{an}, u_{bn}, u_{cn}	Phase voltages of motor
u_{an_OP}, u_{bn_OP}, u_{cn_OP}	Phase voltages of the motor under the OP fault
u_{AP}	Voltage between the phase A terminal and the positive DC rail
u_{BC_OP}	Line-to-line voltage under the OP fault
u_D	Forward-on voltage of the free-wheeling diode
u_d, u_q	d, q-axis voltages
u_d^k, u_q^k	d, q-axis voltages at the current step
u_d^*, u_q^*	d, q-axis voltage references
u_{PN}	Voltage between the positive DC rail and the motor neutral point
u_{PN}	Voltage between the positive DC rail and the negative DC rail
u_{OA}	Voltage between the motor neutral point and the phase A terminal
u_{ON}	Voltage between the motor neutral point and the negative DC rail
u_α, u_β	α, β-axis voltage
u_α^*, u_β^*	α, β-axis voltage references
$\vec{v}_s$	Synthesized voltage vector
$\vec{v}_s^f$	Synthesized voltage vector under the single OS fault
$\vec{v}_x$	Voltage vector
$\vec{v}_x^f$	Voltage vector under the single OS fault
V_{aux}	Fault-tolerant auxiliary voltage source
V_{bemfa}, V_{bemfb}, V_{bemfc}	Three-phase Back-EMFs
V_{CE}	Collector-emitter voltage
V_{DC}	DC bus voltage
V_{gd}	Gate-to-drain voltage
V_{gs}	Gate-to-source voltage

V_{sd}	Source-to-drain voltage
V_{th}	Threshold voltage of V_{gs}
ω_e	Rotor electrical angular velocity
ω_e^k	Rotor electrical angular velocity at the current step
ω_m	Rotor mechanical angular velocity
λ	Angle between the current vector and θ_e
ε_{digi}	Sampling error
θ_e	Rotor electrical angle
Ψ_f	Permanent magnet flux linkage
$\overrightarrow{\Psi_s}$	Stator flux vector

Chapter 1 **Introduction**

1.1 Background

Governments worldwide have made commitments to energy conservation and emissions reduction as a shared goal for the future development of industries and societies. Due to the high efficiency and performance at the energy consumption end, transportation electrification has been prompted to gain a drastic development during the past two decades in sectors of more-electric aviation [1]–[3], high-speed railway [4]–[6], and electric vehicles (EVs) [7]–[9]. Using EV as a most representative example, governments have consistently published and updated policies to stimulate demand. Table 1-1 provides an overview of incentive policies, the latest annual market data, and the ambitions for EVs in key markets. It's noteworthy that the market share of EVs has continuously increased over the last decade. In Table 1-1, BEV stands for Battery Electric Vehicle, PHEV for Plug-in Hybrid Electric Vehicle, and FCEV for Fuel Cell Electric Vehicle.

TABLE 1-1 Incentives, market shares, and ambitions for EVs in four key markets

Regions	Incentive Policies	EV market share in 2022	EV Ambition
China 	1) Purchase tax exemption in 2024-2025, 2) The exemption will be halved in 2026-2027.	25.6 % in new-vehicle sales (BEV +PHEV)	40 % in new sales by 2030
EU 	1) Incentives for purchasing in 20 EU countries, 2) Tax reductions or exemptions in the other 7 EU countries.	21.5 % in new-vehicle sales (BEV +PHEV)	30 %, 70 %, and 100% in new sales by 2025, 2030, and 2035, respectively
UK 	1) EV charge point grant, 2) Road tax exemption, 3) Plug-in grant for eligible vehicles.	22.9 % in new-vehicle sales (BEV +PHEV)	80 % in new sales by 2030
USA 	Federal Policies: 1) EV and FCEV tax credit, 2) EV and FCEV manufacturing tax credit, 3) EV and FCEV manufacturing loans.	8 % in new-vehicle sales (BEV +PHEV)	67 % in new sales by 2032

TABLE 1-2 Global sales of popular EVs in the first half of 2023

Vehicle Type	Powertrain Configuration	Price	Sales (Jan. to Jun. 2023)
Tesla Model 3&Y	3-phase IM (137 kW) powertrain at the front axle (AWD); 3-phase PMSM (220 kW) powertrain at the rear axle.	From 42, 000 GBP	859, 095
BYD HAN	3-phase PMSM (180 kW) powertrain at the front axle (AWD); 3-phase PMSM (200 kW) powertrain at the rear axle.	From 25, 000 GBP	96, 437
Volkswagen ID. 4 GTX	3-phase IM (80 kW) powertrain at the front axle (AWD); 3-phase PMSM (150 kW) powertrain at the rear axle.	From 38, 105 GBP	86, 481
Hyundai Ioniq 5	3-phase PMSM (70 kW) powertrain at the front axle (AWD); 3-phase PMSM (155 kW) powertrain at the rear axle.	From 42, 665 GBP	51, 426
. . .	. . .	. . .	. . .
Mercedes-Benz EQS	3-phase PMSM (135 kW) powertrain at the front axle (AWD); 6-phase PMSM (255 kW) powertrain at the rear axle.	From 105, 500 GBP	10, 900
NIO ES8	6-phase IM (160 kW) powertrain at the front axle; 6-phase IM (240 kW) powertrain at the rear axle.	From 53, 000 GBP	2, 220

The electric powertrain based on electric machine and power inverter replaces the internal combustion engine (ICE) to propel the vehicle. Permanent Magnet Synchronous Motors (PMSMs) have gained popularity in electric vehicles (EVs) due to their high efficiency, power density, and fast dynamics, surpassing Induction Motors (IMs). To enhance reliability and safety, EV powertrains based on multi-phase motor drives have been extensively studied. The multi-phase motor drive has intrinsic high reliability [10]–[12] and smooth torque output [13]–[15]. However, the multi-phase motor drive has been employed only in two high-end EVs. Table 1-2 lists the powertrain configuration, price, and sales in the first half of 2023 for several EV models from top brands. Among thousands of EV models worldwide, only two

models claim to employ powertrains based on six-phase PMSM drives and have much higher prices compared with their three-phase counterparts.

Customers primarily focus on three key aspects when it comes to EVs: charging speed, range per charge, and cost. To enhance EV performance, both the automotive industry and academia are actively pursuing two major technological trends: the adoption of high-voltage EV structures [16], [17] and the development of highly integrated EV powertrains [18]. However, these advancements, characterized by compact layouts, rapid dV/dt (voltage rate of change), and elevated voltage levels, come with an inherent drawback – an increased failure rate of power inverters.

In fact, power inverters contribute to 38% of motor drive faults [19] and are reported as the most fragile component by 31% of responders in an industry-based survey [20]. Within the realm of power inverter faults, open-circuit faults have garnered substantial attention, with ongoing efforts in both fault diagnosis and fault-tolerant control.

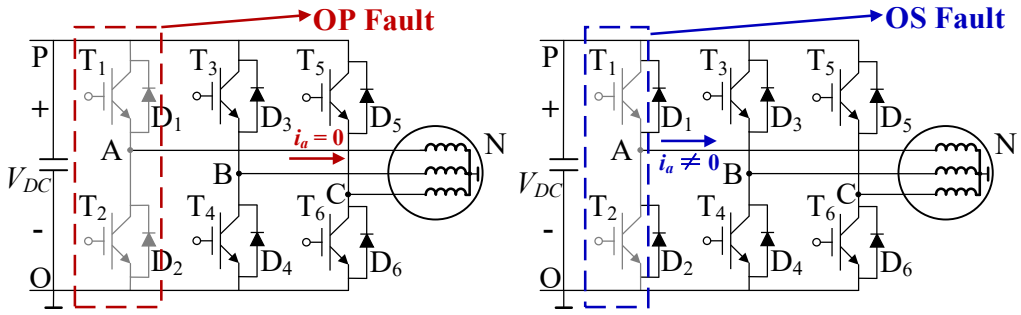


Fig. 1-1. Open-circuit faults in a 3P2L PMSM drive: (a) open-phase fault; (b) open-switch fault.

It's important to note that different failures in a PMSM drive can lead to various types of open-circuit faults for each phase. These failures, such as the breakdown of power switches and the malfunctions of driving signals, will result in short-circuit faults of the faulty phase in the first place. The overcurrent because of the short-circuit faults will lead to isolation or protection, and will eventually evolve into open-circuit faults. From the perspective of the post-fault phenomenon, open-circuit faults in each phase can be categorized into two types:

1. Open-Phase (OP) Fault: In this case, the open-circuit phase is completely disconnected.

2. Open-Switch (OS) Fault: Here, the open-circuit phase can still be conducted through the remaining healthy free-wheeling diodes, as depicted in Fig. 1-1.

These two types of open-circuit faults exhibit distinct post-fault phase voltages and currents, making it necessary to classify and address them separately.

As on-road electric vehicles (EVs) enter their mid-to-late stages of life, ensuring their functional safety becomes increasingly challenging. Functional safety concerns the behavior of systems after a fault occurs and aims to prevent unreasonable risks resulting from malfunctions in electrical and electronic systems. Functional safety sets requirements for fault tolerance and diagnostic coverage. However, the configuration of a standard EV powertrain has limited capabilities for fault-tolerant operation and comprehensive diagnosis.

Given the aging of a significant population of EVs equipped with standard powertrains, there is an urgent need to develop embedded diagnostic and fault-tolerant control methods that can be conveniently implemented in existing on-road EVs.

The motivation of this research is not to arrogantly replace the hardware solutions, but to provide further safety strategies to preserve the post-fault output capability as much as possible. Due to the hardware configurations of the 3P2L PMSM drives, the electromagnetic torque inevitably drops to zero at the spatial phase where the rotor flux coincides with the stator flux. Therefore, compared with hardware fault-tolerant solutions, the embedded fault-tolerant control cannot eliminate the electromagnetic torque pulsation under open-circuit conditions.

However, during other spatial phases, the two phases of remaining healthy motor windings generate a pulse magnetic field along one direction determined by the position of the faulty phase. As a result, the 3P2L EV powertrains have the potential to maintain derated post-fault operation, rather than standing by and completely losing the output capability.

1.2 Dissertation Outline

The primary objective of this research is to provide comprehensive solutions for addressing open-circuit faults in 3P2L PMSM drives. These solutions encompass fault modelling, diagnosis, and fault-tolerant control. The progressive objectives and the structure of this thesis are outlined below. Additionally, the interconnectedness of the technical chapters is illustrated in Figure 1-2.

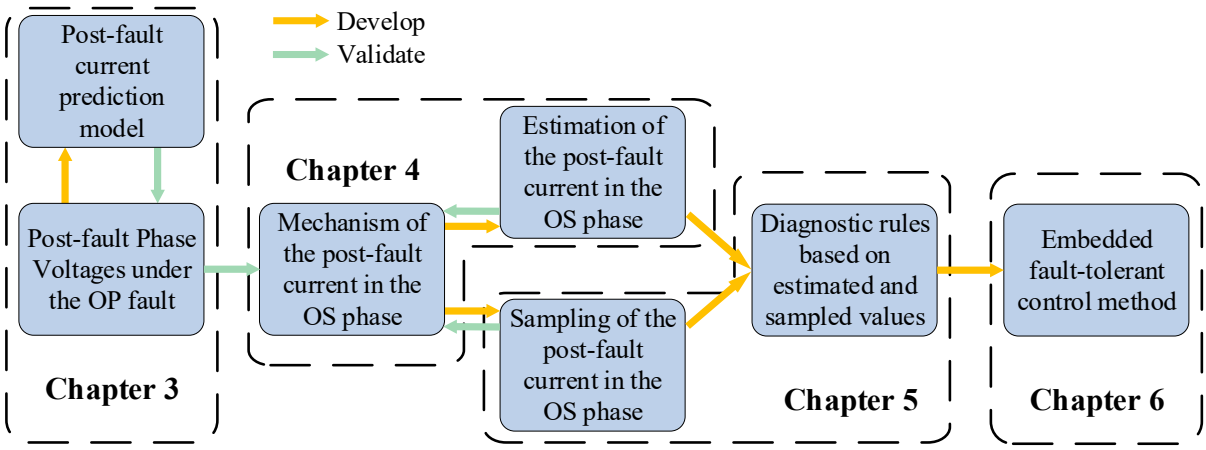


Fig. 1-2. Coherence between technical chapters.

1) In Chapter 2, **the fault propagation of open-circuit faults and existing studies are reviewed**. Firstly, the open-circuit fault is a phenomenon that can be evolved from a variety of component failures. Before studying the open-circuit fault, it is necessary to describe the fault propagation from component failures to the OP fault and OS fault. Furthermore, the understanding and previous works of the post-fault system behaviors are discussed to explain the reasons behind the errors between the modelled results and the measurement. Moreover, the diagnosis methods based on state estimation and operating data are reviewed to emphasize the importance of the acquisition of post-fault current. Finally, the existing fault-tolerant control methods of the 3P2L PMSM drive are studied to identify the research gap.
2) In Chapter 3, **the post-fault phase voltages under the OP fault are derived and an improved post-fault current prediction model is proposed**. Firstly, in each switching state, the post-fault phase voltages are derived by considering the floating neutral voltage incurred by the back electromagnetic force (back-EMF). Furthermore, by incorporating the derived phase voltages as the activation sources in each switching cycle, the post-fault current prediction model is established in the independent phase frame. The predicted currents accurately track the measured currents, which validates the correctness of the derived phase voltages.
3) In Chapter 4, based on the phase voltages under the OP fault, **the remaining conducting post-fault current in the faulty phase under the OS fault is studied and estimated in real time.** Firstly, equivalent circuits are analyzed to explain the conduction condition. Subsequently, activating switching states fulfilling the conditions are studied, and finally, the mathematical model of the post-fault current is built.

4) In Chapter 5, based on the conduction conditions revealed in Chapter 4**, a sampling method is designed to acquire the post-fault current under the OS fault, and diagnostic rules are set to classify the OS and OP faults**. As the post-fault current in the OS phase features a small amplitude, the current sampling errors of setups are considered and avoided. Under different testing conditions, the proposed diagnostic method can detect and classify the OS and OP faults in less than 1/4 of a fundamental cycle.
5) In Chapter 6, **an embedded fault-tolerant control method is proposed to alleviate the torque and speed pulsation under the single OS fault at low speed**. Firstly, the characteristics of OS faults when the motor operates at low speed are analyzed. Furthermore, the vector acting time in space vector pulse width modulation is reallocated. Moreover, the current control references are modified to adapt the post-fault models in the *dq* frame.
6) In Chapter 7, the main contributions of this study are summarized. Furthermore, based on the merits and disadvantages of the proposed methods, future work that can be carried out to further improve the functional safety of the standard EV powertrain is introduced.

Chapter 2 **Review of Inverter Open-Circuit Faults**

2.1 Direct Cause and Triggering Failures of Open-Switch and Open-Phase Faults

This section analyses the direct cause and triggering failures of open-circuit faults in PMSM drives, aiming to explain that open-circuit faults can stem from an extended range of common failures. Firstly, the direct cause and its evolution to open-circuit faults are analyzed. Then, triggering failures that result in the direct cause are listed and explained. Finally, the reviewed failures that can respectively lead to the OS or OP faults will be categorized. Considering the intricate and highly coupling fault propagation mechanisms in PMSM drives, it remains challenging to catalog every specific component failure that could eventually result in an open circuit exhaustively. Therefore, this section focuses on failures in the inverter side, rather than the failures in the relatively robust power cables [21]–[24] and motor windings [25]–[28].

2.1.1 Fault Propagation from Overcurrent to Open-Circuit Faults

In PMSM drives, the direct cause of open-circuit faults is overcurrent, which is the initial symbolic phenomenon of the failure of most components. This subsection concentrates on the behaviors and fault propagation after the overcurrent in PMSM drives, while the failures inducing the overcurrent will be reviewed in the next subsection.

According to the mechanism, the overcurrent can be classified into two types, which are the short-circuit overcurrent [29]–[31] and the breakdown overcurrent [32]–[34].

After the occurrence and detection of overcurrents, the motor windings can be partially or entirely isolated or protected. If the entire motor winding is detached from the inverter, fault-tolerant control is infeasible and the faulty motor drive completely loses its output capability. Therefore, most fault-tolerant research and products are prone to isolate the overcurrent phase independently via fuses, breakers, or disabling driving signals.

a) Short-circuit overcurrent

The commercial power switch modules have short-circuit withstand capability at the level of microseconds [35]–[37], which allows the gate driving circuit and chip to detect the short-circuit overcurrent and then protect it [38]–[40]. When a short-circuit overcurrent occurs, timely triggering of the short-circuit protection function in the gate driving circuit can disable the gate driving signals and prevent power switch destruction.

However, effective short-circuit protection is not guaranteed when the motor drive operates under harsh conditions. First, the short-circuit withstand capability of power devices decreases as the junction temperature and bus voltage increase [37], [41], [42]. Thus, inverters working under harsh conditions are more likely to have their short-circuit detection and protection circuits fail. Furthermore, fast current and voltage transients during a short circuit can be coupled to the gate driving circuit [43], [44], causing the driving chip and circuit to fail. Additionally, when the overcurrent is not caused by short circuits but due to electrical or thermal stress breakdown, disabling the gate driving signals will no longer be effective for overcurrent protection.

b) Breakdown overcurrent

When the collector-emitter voltage exceeds the breakdown voltage of power devices, the elevated electric field strength compromises the voltage-blocking capability of the P-N junction. This leads to an avalanche breakdown, resulting in a significant surge in the collector current.

Although the breakdown overcurrent cannot be protected by disabling the gate driving signals, fuses [45], [46] are integrated into the inverter to isolate the overcurrent phase and avoid disastrous fire accidents. For instance, pyro fuses [47], [48] are mounted at the output terminals of the inverter in TESLA EVs. In addition to the power switches, the breakdown overcurrent can potentially flow through anti-paralleled diodes [49].

c) Fault propagation from overcurrent to open-circuit faults

The aforementioned overcurrent scenario will eventually lead to a specific type of open-circuit fault, as summarized below:

1) When the short-circuit overcurrent protection works effectively, the short-circuit overcurrent eventually results in an OS fault;

2) When the overcurrent phase is isolated by fuses or switches, the overcurrent is transformed into an OP fault;
3) When the protection methods fail to be functional, the ultimate fault type of the open-circuit fault is uncertain and depends on the failure mode, such as lift-offs of bond wires inside the power module.

In the most commonly used wire-bonding power modules, the bond wires are soldered across components for electrical connections. These connections include bonding between busbar terminals and Direct Copper Bonding (DCB) substrate, bonding between DCB substrate and electrodes of power devices, and parallel bonding between DCB substrates. Fig. 2-1 illustrates the bonding connections in a typical single-phase half-bridge Insulated-Gate Bipolar Transistor (IGBT) module from Infineon with three parallel dies.

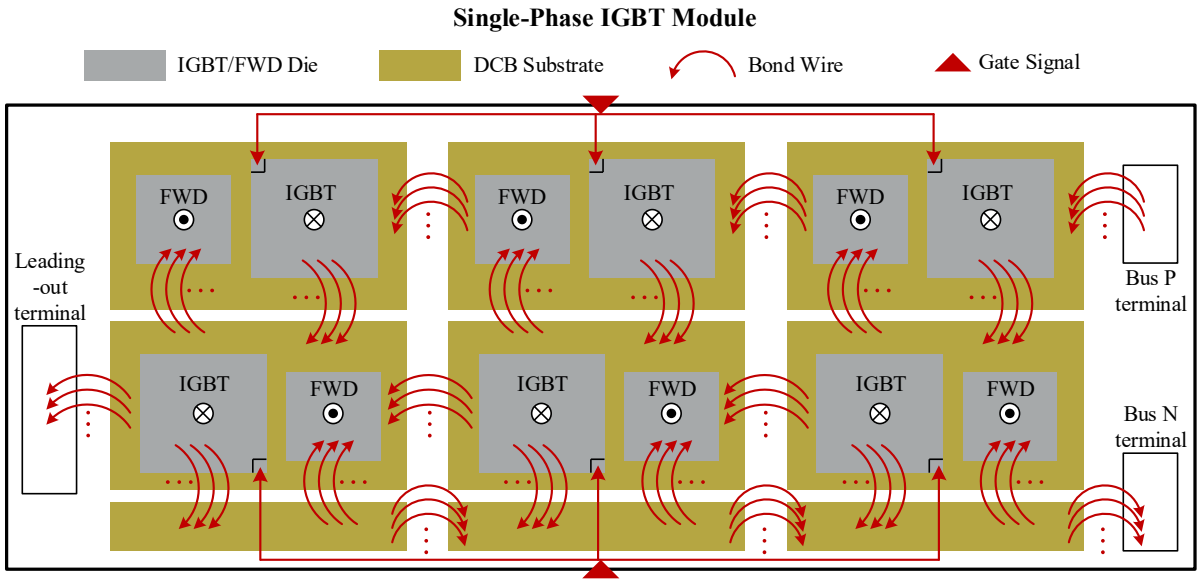


Fig. 2-1. Bonding connections in a single-phase half-bridge IGBT module.

The Lift-off of bond wire can be the result of thermal expansion [50]–[52], cracks [53]–[55], soldering failures [56]–[58], etc. Moreover, depending on the bus voltage and the volume of the bus capacitor, different PMSM drives will discharge different energy levels onto the bond wires during the overcurrent [59]. Subsequently, the heat accumulation caused by the overcurrent exacerbates the propagation of faults, ultimately leading to different fault scenarios that can be categorized as follows:

1) OP faults: Lift-offs of bond wires connecting the bus terminals and the DCB substrates
2) OP faults: Lift-offs of bond wires connecting power switches and diodes to the DCB substrates.

3) OP faults: Lift-offs of bond wires connecting the DCB substrates.
4) OS faults: Lift-offs of bond wires connecting the power switches and the DCB substrates
5) OS faults: Lift-offs of bond wires connecting the gates of power switches and the gate driving terminal.

Consequently, under the overcurrent, the fault type of the open circuit can be determined only when the drive is explicitly aware of whether the overcurrent protection methods are effective. Otherwise, an open circuit fault evolved from overcurrent cannot have its specific fault type determined.

2.1.2 Propagation Tree from Component Failures to Different Open-Circuit Faults

The short-circuit overcurrent and breakdown overcurrent can be induced by various failures and conditions. This subsection summarizes and analyzes some common failures and conditions to establish an intuitive connection between regular operation and open circuit phenomena.

a) Failures inducing short-circuit overcurrent

1) Incorrect gate driving signals: The gate driving circuits are vulnerable to electromagnetic interference caused by drastic switching transients of power switches [60], [61]. An incorrect switching-on driving signal could be generated due to the cross-talks [62], [63] when the other power switch in the same leg is acting, and this results in a short circuit of the inverter leg.
2) Accident reset of the controller chip: The pins of some commonly used microcontrollers, such as DSP TMS320F28335, have a default pull-up state when the chip is reset or during its powering up. The microcontroller reset can be accidentally triggered due to failures in the controller circuit, such as the failure of the 3.3 V power adaptor. Consequently, the two power switches in the same leg are switched on simultaneously and incur a short circuit of the inverter leg.
3) Motor stall: Mechanical clutches or brakes are mounted to hold the motor rotor locked in some servo systems. However, if the clutches or brakes fail to release, the PM rotor cannot generate back-EMF. This results in the high DC bus voltage being directly applied

to the inductance and resistance of the motor winding, causing the high current across the inverter and motor winding [64], [65].

b) Failures inducing breakdown overcurrent

1) Collector-emitter overvoltage: The drastic di/dt transient during the switching off of power switches induces voltages across parasitic inductance along the power transmission [66]. The induced voltages add up to the DC bus voltage, causing the collector-emitter voltage to exceed the breakdown voltage. For instance, if the wavelength of the high-frequency component coincides with the length of the power cable [67], [68], signal reflection can result in a doubling of voltage at the inverter terminals.
2) Thermal breakdown: Due to uneven or insufficient heat dissipation or severe overload, the temperature of the P-N junction rises, increasing the carrier density, which in turn boosts the collector cut-off current. Even though this current is at the microampere level, when combined with the high collector-emitter voltage, it produces substantial energy. This energy further heats the P-N junction. Ultimately, the device is prone to breakdown due to the resulting positive electrothermal feedback [69]–[71].
3) Undervoltage gate driving [72], [73]: IGBT works in its saturation region when its gate-emitter voltage is about 15 V. If the gate-emitter voltage falls below the required level and the low-voltage protection of the driving circuit is ineffective, the IGBT works in the active region, resulting in substantial power dissipation and lead to its thermal breakdown.

Based on the analysis of the fault propagation, the propagation path from the common component failures to the different open-circuit faults can be demonstrated in Fig. 2-2. It is noteworthy that Fig. 2-2 does not cover every component failure that eventually results in an open-circuit fault, as the component failures in motor drives are diverse. For instance, the accident reset of MCU can also be incurred by software failures. Although the overcurrent can be attributed to an expanded range of component failures, it is the effectiveness of the overcurrent protection that determines which type of open-circuit fault would eventually occur.

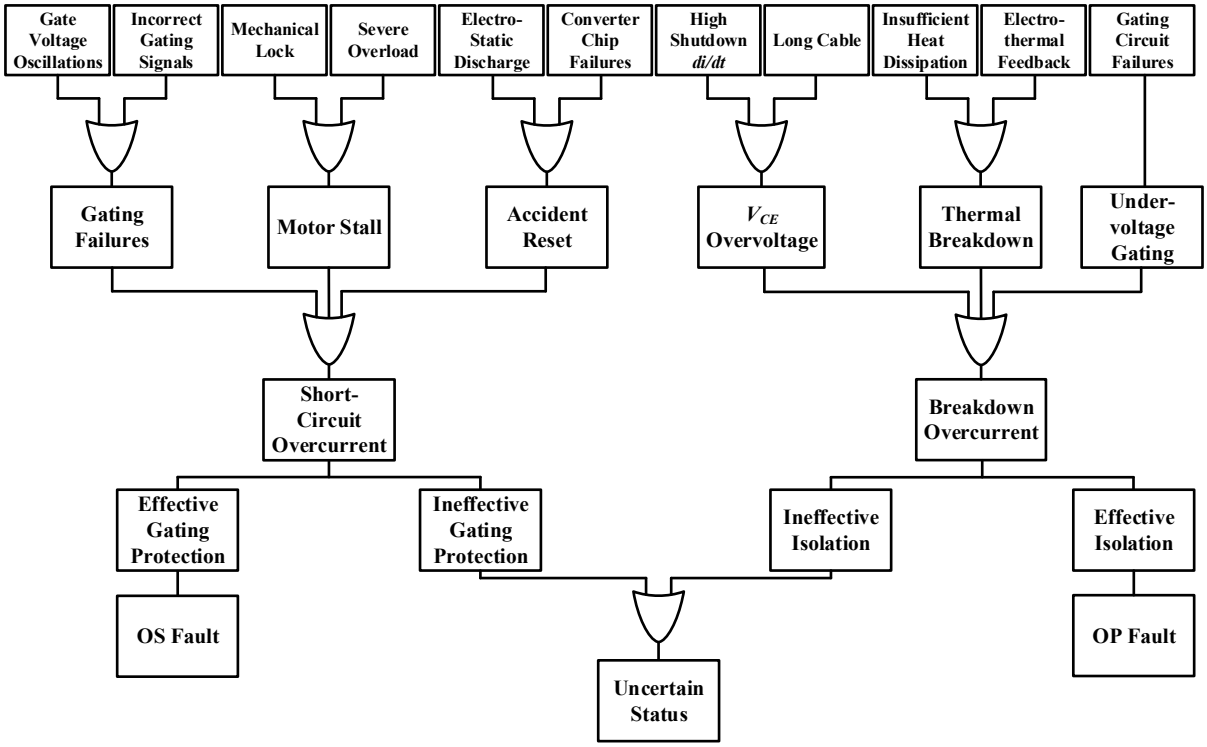


Fig. 2-2. Fault propagation tree from component failures to OS and OP faults.

2.2 Modelling of Inverter Open-Circuit Faults

As reviewed in Section 2.1, the inverter-fed PMSM drives have different current paths under the OS and OP faults. As a result, the OS and OP faults lead to distinct post-fault system structures, which raise concerns about their post-fault models. The behaviors of current dynamics in each switching state stand for the state of post-fault system health and the current dynamics are activated by the inverter-fed phase voltages. The significance of modelling the PMSM drives under the OS and OP faults lies in that:

1) The boundary between the OS and OP faults is ambiguous when the fault stems from failures that cannot be accurately detected and reported, such as the failure locations of the bond wires. The unidentified post-fault system fails to realize the condition monitoring of the free-wheeling diodes and has a degraded diagnostic coverage.
2) The unidentified system model leads to nonoptimal fault-tolerant control. It is critical to recover the mechanical performance with minimized extra losses, such as losses caused by the increased current amplitudes or harmonics under fault-tolerant control methods. To obtain the optimal post-fault control structures and parameters, accurate post-fault plant models are required.

In this section, the modelling of the post-fault current dynamics and the expressions of the phase voltages under OS and OP faults will be reviewed respectively.

2.2.1 Modelling of PMSM Drives under the Open-Phase Fault

The post-fault phase voltages under the OP fault are key to describing the current behaviors. In the differential dynamic model of PMSM, the current dynamics in the synchronous rotation frame are determined by voltages transforming from the independent phase voltages. By discretizing the differential model, prediction models and observers can be built and implemented in microcontrollers for the purposes of predictive control [74]–[76], sensorless control [77]–[79], and state observation [80]–[82] of PMSM drives.

The phase voltages are composed of the voltage drops across the phase resistance, the voltage induced by self and mutual inductances, and the back-EMF of each phase. The OP fault significantly alters these phase voltage components and the post-fault current prediction model, which is particularly attractive for motor drives employing model-predictive controls (MPC) because diagnostic features can be directly extracted from the control loops [83], [84]. In [83] and [85], diagnostic features are obtained from different cost functions designed for MPC. More importantly, post-fault model predictive control [86]–[88] of PMSM drives also benefits from the accurate description of the post-fault plant model.

Under healthy conditions, voltage excitations in each prediction step are approximated using voltage commands from current controllers. In [89], the voltage commands from current controllers serve as the approximated voltage excitation source in the current prediction model. This approximation works properly when the motor drive is under healthy conditions because voltage pulses from the healthy inverter are modulated based on the voltage commands.

Under the OP fault, the faulty inverter cannot execute the voltage commands due to opened power switches. Additionally, changes also apply to motor phase inductances as the phase current influences mutual inductances.

In [90], the same prediction model is utilized under the OP fault to generate the residual errors between the practical post-fault current and the predicted current for fault diagnosis. By introducing the zero post-fault current into the faulty phase, in [91], the prediction model of the OCDD was built in the three-phase system rather than the *dq*-coordinate system. In

[92], the voltage commands are replaced by post-fault phase voltages which are assumed to have constant values in each switching state. Furthermore, according to the voltage-second principle, the voltage excitations generated during one switching period are calculated based on the constant phase voltages and the acting time of each switching state.

Under the OP fault, the absence of the current in the faulty phase eliminates the voltages across the resistance and inductances. However, the back-EMF is generated by the rotor permanent rotor and remains in the phase winding after the disappearance of the current. Similarly, the equation of post-fault voltage equilibrium in [93] also excludes the back-EMF. Due to the discrepancies between the actual and assumed phase voltages, the estimated post-fault currents in [90] and [92] do not agree with the measured currents.

Conclusively, the omission of back-EMF and mutual inductances leads to the inaccurate modelling of the post-fault phase voltages and current prediction under the OP fault, which hinders the optimization of post-fault diagnosis and fault-tolerant control.

2.2.2 Modelling of PMSM Drives under the Open-Switch Fault

It is noteworthy that the post-fault model under the OP fault is of utmost significance when deriving the model under the OS fault. This is because the free-wheeling diodes are not in a continuous conducting state but conduct selectively in specific switching states under the OS fault. When these diodes do not conduct, the system states are identical to those under the OP fault. Therefore, the primary objective of modelling the OS fault is to investigate the remaining-conducting post-fault current in the OS phase.

The post-fault current in the OS phase has drawn attention in recent years. It was first reported in [94], where experiments and co-simulation validated the existence of the post-fault current under the OS fault. The fault-tolerant control of the induction motor drive was improved in [95] by considering the effect of the post-fault current on phase voltages. In [96], the effect of the post-fault current on phase voltages was considered in the fault-tolerant control of a PM generator. A similar modelling method was expanded to multiple open-switch faults in a PMSM drive [97]. Moreover, the post-fault current was exploited to realize sensorless control under the faulty condition [98], in which the rotor position was derived from the sampled post-fault current in the OS phase. However, as the current is activated in special switching states instead of all of them, the sampling points should be specifically arranged according to the mechanism of the current.

While the effect of post-fault conduction on the phase voltages can be assessed by comparing it with the pre-fault switching states, it is essential to note that the faulty phase doesn't conduct in every switching state but rather selectively in specific, undisclosed switching states. Furthermore, no model has been established to elucidate the mechanism of the post-fault current, let alone its sampling and estimation for further applications. The sampling and estimation of the post-fault current in the OS phase can be employed not only in diagnosis methods but also in correcting or deriving the rotor position since the post-fault current in the OS phase is intuitively determined by the back-EMF. To estimate the post-fault current, the switching states that activate the post-fault current must be revealed. On the one hand, the acting time of the specific switching states is the conduction time of the post-fault current; on the other hand, the switching states determine the post-fault equivalent circuits, which determine the voltage source of the post-fault current. Therefore, the post-fault conduction should be studied on the scale of the switching period.

Besides, it should be noted that the studied current in the OS phase is different from the current generated when the motor works as a generator. The uncontrolled generation current was thoroughly studied in [99] and has the following differences compared with the studied current in the OS phase:

1) Unlike the uncontrolled generation current, which flows back to the DC source with amplitudes ranging from tens to hundreds of amperes, the studied current in the OS phase flows within the motor drive and is in the milliampere range. This is because the open-circuit current is not only related to the back-EMF but also to the acting time of its activating switching states.

2) The uncontrolled generation current is not related to the switching states of the inverter, while the open-circuit current can only be activated by its activating switching states.

3) Unlike the uncontrolled generation current that feeds power to the power source, the open-circuit current does not feed power but can be employed for various purposes such as diagnosis, fault-tolerant control, and parameter estimation.

2.3 Diagnosis of Inverter Open-Circuit Faults

After understanding and acquiring their distinct post-fault currents, the OS and OP faults can

be diagnosed and distinguished. specific fault type can be identified. Distinguishing the OS fault and OP fault is necessary for the maintenance of the motor drive and increases the diagnostic coverage of the system.

In terms of diagnosis, the model-based method compares feedback values and estimated values acquired from explicit physical models [84], [100]. Comparatively, the data-driven method emphasizes statistical significance and is suitable for uncertain or complex targets [101], [102]. In this section, the literature on the diagnosis of open-circuit faults will be reviewed from the perspectives of state estimation and operating data

2.3.1 Diagnosis Based on State Estimation

Due to the limited amount of system feedback in a 3P2L PMSM drive, observers, prediction models, and filters are designed to acquire an extended scope of informative system state.

In [103], [104], three-phase currents are estimated using a Luenburger observer. The estimated currents are compared with sampled currents to acquire their residual errors, and an adaptive threshold is designed to evaluate residuals. To avoid misdiagnosis under the interference of current sensor faults, current sensor faults and open-circuit faults are classified in [105]. Furthermore, the mixed diagnostic method of open-circuit faults and sensor faults is expanded to cover the speed sensor [106]. Besides, the current estimation and acquisition of current residual errors are explored by designing the mixed-logic-dynamic model [107], sliding mode observers [108], and Kalman filters [109].

The significant changes in phase currents under faulty conditions are intuitive but can be affected by multiple factors, such as the accuracy of sensors [110], [111]. Comparatively, the voltage states in voltage source inverter-fed PMSM drives provide a more reliable and robust diagnostic basis. However, the measurement of phase voltages is not a commonly adopted configuration in PMSM drives, which results in the necessary estimation. In [112], [113], the mix-logic-dynamic model is utilized to acquire the residual errors between the estimated voltages and voltage references, achieving the trade-off between diagnostic time and robustness against parameter variations.

By far, a variety of estimation methods has been proposed to detect the differences between the desired value and practical value of the system responses under healthy and faulty conditions. The existing observers and estimation models are designed based on the healthy

plant model. Consequently, although they are suitable to be utilized in diagnosis for acquiring residual errors, they do not describe the practical post-fault system states.

2.3.2 Diagnosis Based on Operating Data

As an emerging and powerful alternative to the model-based diagnostic methods reviewed above, data-driven methods have been continuously attracting attention from both industry and academia.

In [114], a normalized current vector is introduced as a diagnostic variable, and the diagnostic results are generated via an interpreter based on fuzzy logic. In [115], a training set consisting of phase voltages, phase currents, and torque is used to train a neural network. In [116], the discrete-time wavelet transform is performed to extract the features of the phase currents, and then the faulty patterns are identified by the support vector machine (SVM). In [117], signal features of line voltages are extracted by FFT, and the fault diagnosis is performed using a Bayesian network.

Data-driven method studies the distribution features of the training set to fully utilize the diagnostic information in the samples. However, the quality of the samples of the diagnosis variables has a decisive influence on the results. Meanwhile, the data-driven method is difficult to implement online as it requires the dimension of sampled data to be aligned with the classifications trained outline. In [100], principle component analysis (PCA) and SVM are implemented online by incorporating the data dimension with the rotor electrical angle, which normalizes the dimension of sampled sets of currents. Another disadvantage of the data-driven method is the extra computational burden posed by the large scale of floating computation. In [118], diagnosis based on small sample sets is realized by normalizing the current vector and utilizing a wavelet convolutional neural network.

The data-driven method is promising, especially in systems with uncertainties and complex plant models. However, PMSM drives have straightforward physical significance and clear dynamic models. Therefore, the model-based method remains to be the most commonly utilized.

2.4 Mitigation of Inverter Open-Circuit Faults

Fault-tolerant strategies are put into commission once faults are detected. Based on the severities of faults and the expected performance of tolerant methods, tolerant methods in PMSM drives can be categorized into three groups, which are:

1) Fault-recoverable tolerant strategies, by which the smooth torque and speed can be largely recovered. The typical cases include sensor faults tolerated by sensor-less control methods [119]–[121] or sensor calibration techniques [122]–[124].

2) Emergency remedial strategies. The typical cases are mechanical [125] and electrical [126]–[128] energy dissipation strategies to protect passengers in a car crash.

3) Damage-alleviating tolerant strategies. The typical cases include a variety of limp-home strategies, such as the inter-turn short-circuit tolerant strategy [129], the derating operation of multilevel inverters [130], [131], and the thermally derated operation [132], [133]. These strategies allow the 3P2L motor drive to maximumly maintain post-fault drivability.

2.4.1 Advanced Topologies of PMSM Drive

The rapid development of advanced topologies has been attractive to safety-critical applications. Therefore, although this thesis concerns the reliability improvement of 3P2L PMSM drives, it is necessary to review topologies regarding the fault-tolerant control of PMSM drives.

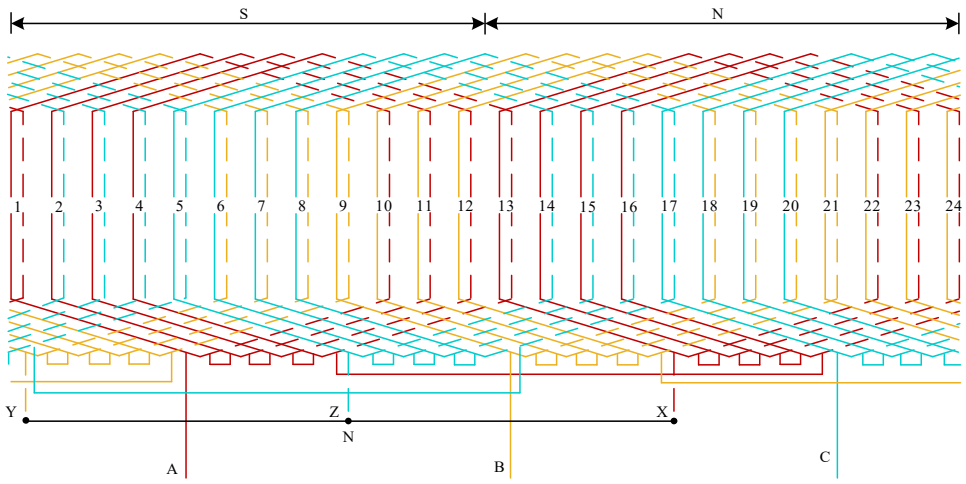


Fig. 2-3. Winding distribution of a three-phase motor

The fault-tolerant topologies include multiphase motor drives and variants of 3P2L topology with auxiliary configurations. Other topologies, such as parallel inverter-fed motor drives [134]–[137] and multilevel inverter-fed motor drives [138]–[140], also provide improvement regarding reliability but are not considered fault-tolerant topologies, as they were proposed to enhance other performance of the motor drives. For example, the interleaved-parallel inverter was proposed to alleviate the electromagnetic interference and realize zero common-mode voltage PWM of motor drives.

Among multiphase motor drives, the dual three-phase motor drive is the most promising topology to be extensively employed in applications emphasizing safety and power density. Assuming a motor has 24 stator slots and 1 rotor pole pair, a typical winding distribution when it is configured as a three-phase motor is presented in Fig. 2-3, where the winding pitch is 9 slots; N and S are the poles of the permanent magnet; A, B, C, X, Y, Z are the winding terminals; N is the winding neutral point.

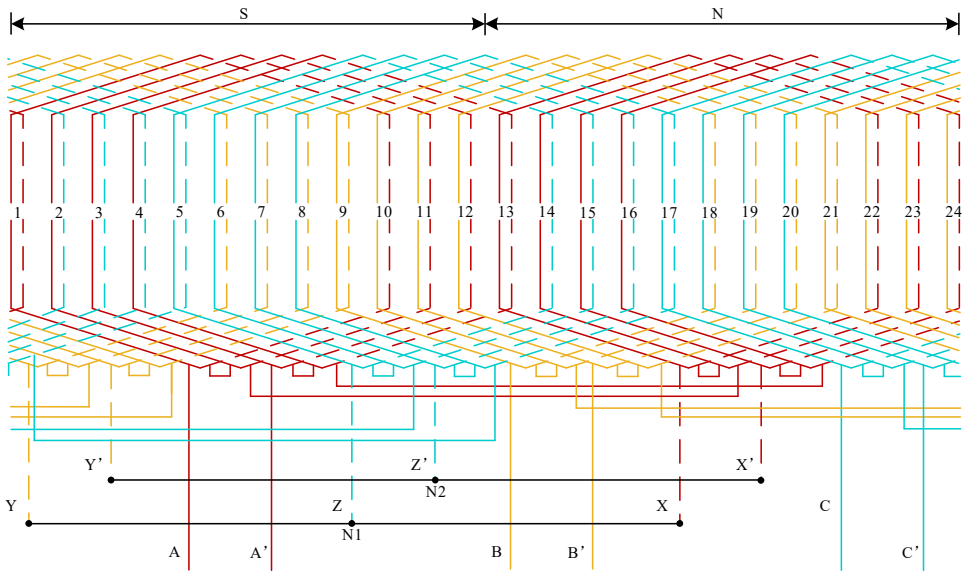


Fig. 2-4. Winding distribution of a dual three-phase motor.

In a three-phase motor with a distributing winding configuration, each phase of winding is composed of two independent phase belts. Each phase belt distributes over a spatial phase range of 60 electrical degrees and the two phase belts are arranged in a phase difference of 180 electrical degrees. The two phase belts of a phase are reversely connected, and terminals of phase belts A, B, and C are led out, as illustrated in Fig. 2-3. Differently, in the dual three-phase motor, each phase belt spanning over 60 electrical degrees is split into two phase belts distributing over 30 electrical degrees. Each of the 30-degree phase belts is reversely

connected to their counterpart with a phase difference of 180 electrical degrees and each set of the two reverse-connected 30-degree phase belts leads out an independent terminal, as shown in Fig. 2-4.

Due to the 30-degree interleaving angle between the two sets of three-phase windings, the dual three-phase motor has the intrinsic advantage of eliminating the 6th torque harmonic in 3P2L PMSM drives [14], [141], [142].

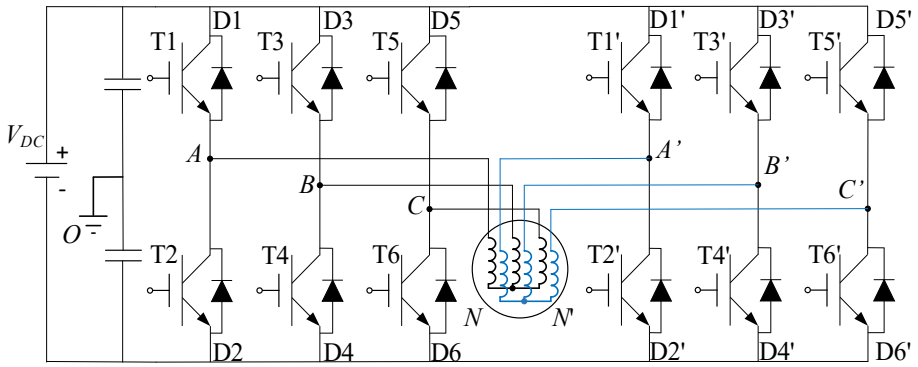


Fig. 2-5. Topology of the dual three-phase motor drive.

The two sets of motor windings are isolated from each other, which provides the natural capability of independent operation, as can be seen in Fig. 2-5. Moreover, along with the flexibility of voltage vector selection, the modulation method of vector space decomposition (VSD) [143] transforms the dual three-phase motor into three decoupled subspaces, which further facilitates the control design under different system health conditions. Based on VSD, current control references in the different subspaces can be adjusted to agree with the post-fault system model [144], [145] in both field-oriented control (FOC) [11], [146]–[149] and direct torque control (DTC) [150]–[153].

As low-cost alternatives to multi-phase motor drives, the reliability of the 3P2L PMSM drive is also enhanced by some auxiliary configurations, such as the tolerant voltage source inverter (VSI) configured by split DC link capacitors and auxiliary Triodes AC switches (TRIACs) [154] or leading-out motor neutral point [155]. In [154], inverter output terminals are connected to the mid-point of the split capacitor through TRIACs, as shown in Fig. 2-6. The faulty leg will be isolated once the open-circuit fault is located, so the motor is fed by a three-phase four-switch VSI. With the same configuration, predictive torque control is introduced in [156] for the pre-fault and post-fault operations to realize a smooth transition.

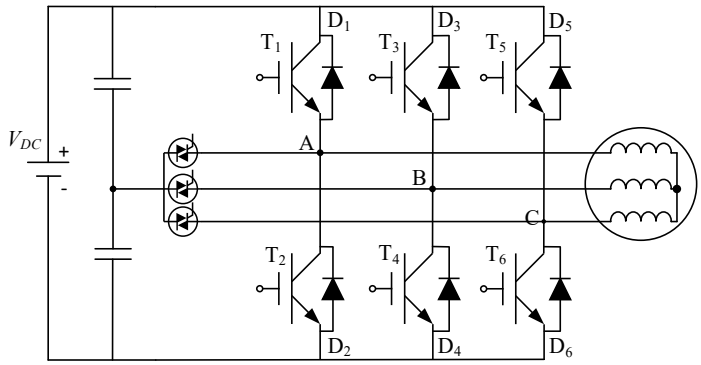


Fig. 2-6. Topology of connecting three phases to the mid-point of DC capacitor.

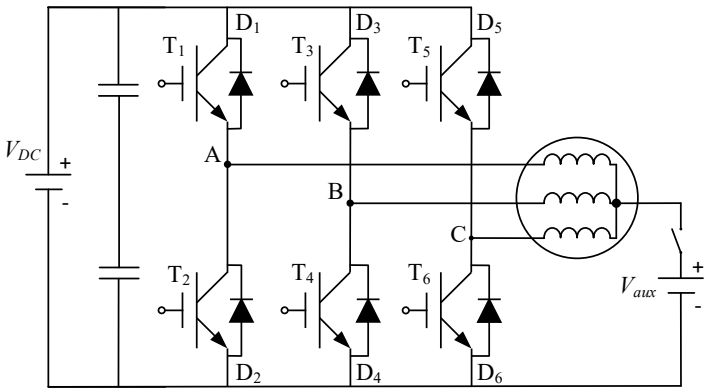


Fig. 2-7. Topology of connecting the neutral point to an auxiliary DC source.

Being different from [154], the mid-point of split capacitors is connected to the leading-out motor neutral point in [155], and it was mathematically proven that the remaining two phases can output torque smoothly through phase-shifting. In [157], [158], after the occurrence of the fault, a DC source is directly connected to the leading-out neutral point to provide a path for the zero-sequence current, as shown in Fig. 2-7, where V_{aux} stands for the fault-tolerant auxiliary DC source. The open-circuit fault-recoverable strategies mentioned above guarantee smooth torque output with the sacrifice of maximum power or speed output.

2.4.2 Fault-Tolerant Control Methods for 3P2L PMSM Drives

Although the torque pulsation incurred by open-circuit faults is inevitable in a 3P2L PMSM drive, it is still necessary to maintain the post-fault drivability and alleviate secondary damages on the powertrain. By far, unlike the position sensor and current sensor faults, the open-circuit faults in the 3P2L PMSM drive cannot be effectively tolerated, degrading the reliability and fault-tolerant capability of the motor drive.

The responses of motor speed, current, and torque under open-circuit faults are analyzed in

[159], [160], but only braking methods are discussed without the consideration of fault-tolerant control. Based on the post-fault model proposed in [159], a predictive control method is proposed in [161], but only the remaining healthy power switches are not fully utilized and the proposed method is not suitable for the most commonly used FOC-based PMSM drive. The inevitable torque loss is revealed in [90], and a pre-firing current commutation method is designed to reduce the duration of negative torque. However, the faulty phase is still entirely removed. Aiming at open-switch faults in a permanent magnet generator system, the post-fault voltage vectors are derived and a set of tolerant solutions are proposed in [96]. However, the post-fault voltage vectors of the generator cannot be applied to the machine operating as a motor. The remaining healthy switch of the faulty phase is employed in [162] for the first time. Instead of utilizing FOC, the desired voltage vector is directly predicted and the references of currents in the *dq* frame are redesigned by setting the current of the faulty phase as zero. Furthermore, a current slope is designed to avoid exceeding the current limit. However, the faulty phase current can be hardly sensed as zero due to diode free-wheeling currents, diode reverse-recovery currents, and sensor errors. On the other hand, since the single open-circuit fault does not affect the entire fundamental cycle, hence, the post-fault control is required to periodically change from the fault-tolerant control to normal-state control. Therefore, it is necessary to improve the control transition to avoid the delay or preact posed by the non-zero faulty phase current. In [163], the post-fault current control is further optimized to reduce post-fault torque pulsation and copper loss.

2.5 Valuable Topic Requiring Further Study

As illustrated in Fig. 2-2, the open-circuit faults in a PMSM drive can be further classified as OP faults and OS faults according to the health status of free-wheeling diodes. When the diodes are healthy, the open-circuit phase has the potential to conduct residual current. When the diodes are destroyed as well, the open-circuit phase completely loses the current conduction path. The above two conditions have distinct post-fault current phenomena and voltage conditions. Given that the voltage source inverter controls the motor by voltage commands, the two faults should have been treated with different fault-tolerant methods and fault categorization.

Based on the review of the previous studies, the following potential topics require further study:

1) At present, the dynamic model of phase currents under the OP fault has not been properly addressed. As a result, the post-fault current prediction is inaccurate and cannot be employed for current control or other utilizations, such as fault diagnosis. The inaccurate current prediction is primarily due to the unsatisfied approximations in voltage excitation during each prediction step, resulting from a limited understanding of post-fault phase voltages under the OP fault.
2) The residual current flowing in the faulty phase under the OS fault remains ignored. One of the reasons is attributed to its relatively small amplitude compared to the post-fault currents in other remaining healthy phases. However, the post-fault current in the OS phase exhibits a distinct pattern and is the most significant difference between the OS and OP faults. Moreover, Exploring techniques for post-fault condition monitoring could be enriched by sampling and estimating this specific post-fault current.
3) Conventionally, the diagnosis of open-circuit fault focuses on the localization of the faulty phase, neglecting the healthy condition of the power devices like power switches and power diodes. In practical applications, the fault localization of open-circuit phases can rely on overcurrent detection and protection circuits integrated into the motor drive. The research in the diagnosis of open-circuit faults should emphasize the scenarios where the integrated detection and protection circuits are ineffective, leading to system state uncertainty.
4) Although multi-phase motor drives and fault-tolerant variants of the 3P2L motor drive have been extensively studied, there has been a noticeable lack of emphasis on techniques to enhance the post-fault resilience of 3P2L motor drives. Given that the 3P2L motor drive is the most widely used topology in powertrains and industrial applications, it is urgent to develop embedded fault-tolerant methods that can be conveniently updated to 3P2L motor drives being employed.

2.6 Summary

This section provides a comprehensive review spanning the fault propagation, fault modelling, fault diagnosis, and fault-tolerant control of the open-circuit faults in PMSM drives. The review work is of great significance in the following three aspects: Firstly, it analyzes the direct cause of open-circuit faults and categorizes the common component failures in a fault propagation tree, which provides a clear scope of the research target to

ordinary readers. Secondly, research gaps in the previous modelling works regarding the OS and OP faults are identified, specifying the modelling of the post-fault current in the OS phase as one of the primary targets of this thesis. Thirdly, it explains the necessity of improving the reliability of 3P2L PMSM drives.

Chapter 3 **Modelling of the Open-Phase Fault**

3.1 Introduction

In this chapter, phase voltages under the phase-A OP fault are derived based on postfault equivalent circuits, and the postfault current prediction model is established. The significance of deriving the post-fault phase voltages lies in two main areas: first, the phase voltages influence the post-fault control method, which is based on the voltage vectors of the faulty inverter. More importantly, when the faulty phase is not conducting under the OS fault, its voltage is the same as the phase voltage under the OP fault. Consequently, the phase voltages under the OP fault also determine the transition from conduction and non-conduction of the faulty phase under the OS fault. Therefore, understanding the phase voltages under the OP fault is fundamental to the subsequent chapters, including the modelling of the OS fault in Chapter 4, the distinction between the OP and OS faults in Chapter 5, and the fault-tolerant control in Chapter 6.

The phase voltages in the OP fault have not been accurately modelled. The post-fault phase voltages were previously considered constant values under each switching state, without taking into account the floating voltage at the motor neutral point, induced by the back-EMF of the faulty phase. A distinguishing feature between the OP and OS faults is the conduction of the anti-parallel diodes of the open-circuit phase. These diodes can conduct when the voltage differences between their terminals surpass their forward-on voltages. The voltage differences between terminals are determined by the phase voltages when the diode is not conducting, which corresponds to the voltages under the OP fault. Consequently, neglecting the back-EMF can create confusion in the conduction conditions of the OS fault, leading to a failure to distinguish between the OS fault and the OP fault.

In this chapter, the post-fault phase voltages are derived based on equivalent circuits of each switching state under a phase A OP fault. Furthermore, by incorporating the derived phase voltages as the activation sources in each switching period, a post-fault current prediction model is established.

Additionally, due to the absence of the current in the faulty phase, the inductances in the *dq*

frame are no longer decoupled. Under healthy condition, the three-phase inductances are coupled with each other, but the three-phase system is symmetrical in physical and electrical distribution. Therefore, the three-phase inductances can be decoupled by coordinate transformation into the orthogonal *dq* frame. However, under the open-circuit condition, the conduction windings are not symmetrically distributed. On the other hand, the remaining two phase currents are strongly coupled, losing the flexibility to regulate their amplitudes independently. Therefore, the inductances of the faulty windings cannot be decoupled by coordinate transformations.

Consequently, the post-fault current prediction model is established in the independent *abc* phase frame. Compared to the existing post-fault current prediction models, the proposed model shows better agreement with measured currents, validating the correctness of the derived post-fault phase voltages.

3.2 Phase Voltages under the Open-Phase Fault Considering Floating Neutral Point

3.2.1 Three-Phase Voltage Equilibrium under the Open-Phase Fault

Due to the blocked faulty phase under the OP fault, the voltages and currents in the three-phase windings are no longer symmetric. As a result, post-fault parameters in the *dq* coordinate are not decoupled as direct values but coupled by the rotor electrical angle θ_e. More importantly, the influence of the OP fault on each phase voltage needs to be analyzed independently in each switching state. Therefore, it is necessary to analyze the three-phase *abc* coordinate for simplification.

When no fault occurs, the simplified three-phase voltage equations are described in Eq. (3-1), where the magnetic saturation, eddy current losses, and hysteresis losses are neglected. i_a, i_b, i_c and u_{an}, u_{bn}, u_{cn} represent phase currents and voltages, respectively; L_s is the phase self-inductance; M stands for the mutual inductance and M is equal to $-L_s/2$ in the three-phase motor; R_s denotes the stator resistance; ω_e is the electrical angular velocity; Ψ_f is the rotor flux linkage.

$$\begin{cases} u_{an} = R_s i_a + L_s \dfrac{di_a}{dt} - M \dfrac{d(i_b + i_c)}{dt} - \Psi_f \omega_e \sin\theta_e \\ u_{bn} = R_s i_b + L_s \dfrac{di_b}{dt} - M \dfrac{d(i_a + i_c)}{dt} - \Psi_f \omega_e \sin(\theta_e - \dfrac{2}{3}\pi) \\ u_{cn} = R_s i_c + L_s \dfrac{di_c}{dt} - M \dfrac{d(i_a + i_b)}{dt} - \Psi_f \omega_e \sin(\theta_e - \dfrac{4}{3}\pi) \end{cases} \tag{3-1}$$

In Eq. (3-1), the three-phase currents sum up to 0 as they all flow through the neutral point of the motor, which is $i_a + i_b + i_c = 0$. In addition, because the three-phase windings are distributed evenly with an interleaving angle of 120 electrical degrees with each other, the three-phase back-EMFs are sinusoidally symmetrical and also sum up to 0. Therefore, it can be derived that the three-phase voltages in Eq. (3-1) sum up to 0 under the healthy condition. The last items in the voltage equilibrium equations are defined as the back-EMFs of each phase, and the characteristic of phase A back-EMF can be seen in Eq. (3-2):

$$V_{bemfa} = -\Psi_f \omega_e \sin\theta_e \begin{cases} > 0, \ \theta_e \in (\pi, \ 2\pi) \\ < 0, \ \theta_e \in (0, \ \pi) \end{cases} \tag{3-2}$$

Without loss of generality, assuming the OP fault occurs in phase A, hence, the post-fault phase A current i_{a_OP} is equal to 0, and the post-fault phase B current i_{b_OP} is equal to the post-fault phase C current $-i_{c\_OP}$. By incorporating $i_{a\_OP} = 0$ into Eq. (3-1), the three-phase voltage equilibrium equations under the OP fault can be described in Eq. (3-3), where the suffix '*OP*' denotes the OP condition:

$$\begin{cases} u_{an\_OP} = -\Psi_f \omega_e \sin\theta_e = V_{bemfa} \\ u_{bn\_OP} = R_s i_{b\_OP} + \dfrac{3}{2} L_s \dfrac{di_{b\_OP}}{dt} - \Psi_f \omega_e \sin(\theta_e - \dfrac{2}{3}\pi) \\ u_{cn\_OP} = R_s i_{c\_OP} + \dfrac{3}{2} L_s \dfrac{di_{c\_OP}}{dt} - \Psi_f \omega_e \sin(\theta_e - \dfrac{4}{3}\pi) \end{cases} \tag{3-3}$$

$$\begin{aligned} & u_{an\_OP} + u_{bn\_OP} + u_{cn\_OP} = 0 \\ & = R_s (i_{b\_OP} + i_{c\_OP}) + \frac{3}{2} L_s \frac{d(i_{b\_OP} + i_{c\_OP})}{dt} \\ & \quad - \Psi_f \omega_e [\sin\theta_e + \sin(\theta_e - \frac{2}{3}\pi) + \sin(\theta_e - \frac{4}{3}\pi)] \end{aligned} \tag{3-4}$$

By incorporating $i_{b\_OP} = -i_{c\_OP}$ into Eq. (3-3), it can be derived that the sum of the three-phase

voltages can be illustrated in Eq. (3-4):

In Eq. (3-4), although the three-phase currents are no longer symmetric, the three-phase back-EMFs remain symmetric and sum up to 0 due to the symmetric space distribution of windings. Hence, the sum of three-phase voltages remains 0 under the OP fault and plays an important role in the subsequent derivation of the post-fault phase voltages.

3.2.2 Phase Voltages in Each Switching State under the Open-Phase Fault

Based on the line-to-line voltages and the conclusion that the post-fault phase voltages still sum up to 0, the post-fault phase voltages in each switching state can be derived.

When no fault occurs, two of the three phases are connected to one of the DC bus rails, and the remaining phase is connected to the other DC bus rail in each switching state. For example, in the switching state '100', where '1' indicates that the upper switch of the corresponding phase is on while the lower switch is off, and '0' denotes the opposite, phase A is connected to the positive DC bus rail, while phases B and C are connected to the negative DC bus rail.

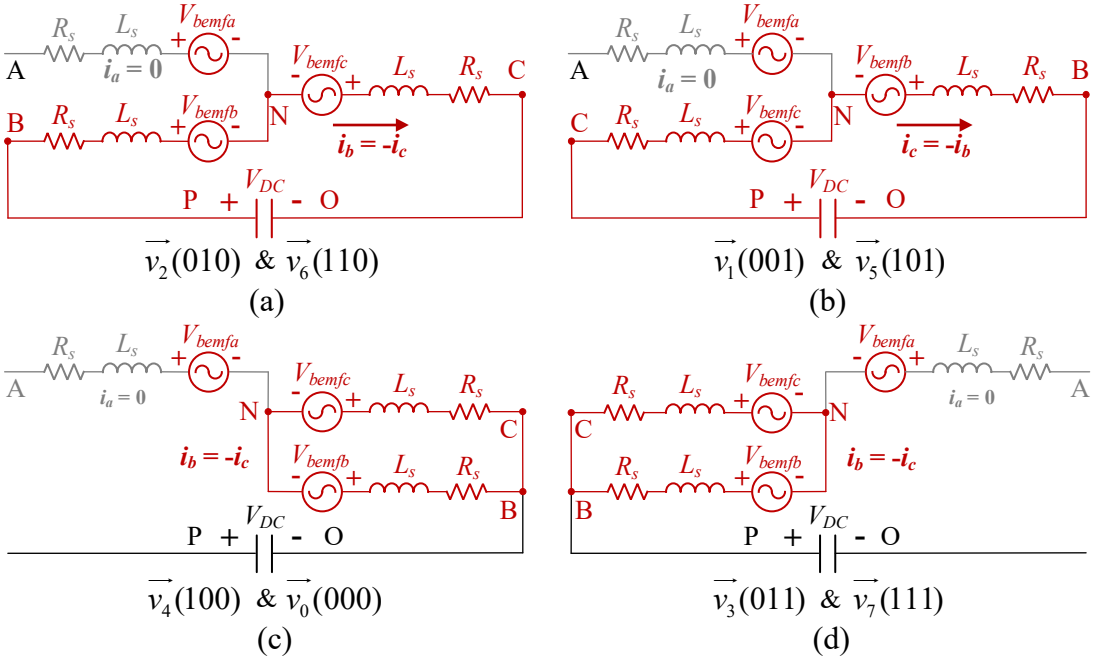


Fig. 3-1. Equivalent circuit within each switching state under phase A open-phase fault.

However, under the phase A OP fault, the opened phase A is floating and is disconnected from the DC rails, while phase B and phase C are connected to either the positive rail or the negative rail according to the switching state, as depicted in Fig. 3-1, where $\vec{v_x}$ stands for the

corresponding inverter voltage vector associated with each switching state; A, B, C, P, and O denote the terminals of windings and DC bus rails; V_{DC} is the DC bus voltage.

Based on the equivalent circuits in Fig. 3-1, the line-to-line voltages between phase B and phase C in each switching state can be described in Eq. (3-5).

$$\begin{cases} u_{BC\_OP} = V_{DC} = u_{bn\_OP} - u_{cn\_OP}, & \vec{v_2} \,\&\, \vec{v_6} \\ u_{BC\_OP} = -V_{DC} = u_{bn\_OP} - u_{cn\_OP}, & \vec{v_1} \,\&\, \vec{v_5} \\ u_{BC\_OP} = 0 = u_{bn\_OP} - u_{cn\_OP}, & \vec{v_3} \,\&\, \vec{v_4} \,\&\, \vec{v_0} \,\&\, \vec{v_7} \end{cases} \tag{3-5}$$

From Eq. (3-5), relationships between u_{bn_OP} and u_{cn_OP} can be described in Eq. (3-6):

$$\begin{cases} u_{bn\_OP} = V_{DC} + u_{cn\_OP}; \; u_{cn\_OP} = -V_{DC} + u_{bn\_OP}, & \vec{v_2} \,\&\, \vec{v_6} \\ u_{bn\_OP} = -V_{DC} + u_{cn\_OP}; \; u_{cn\_OP} = V_{DC} + u_{bn\_OP}, & \vec{v_1} \,\&\, \vec{v_5} \\ u_{bn\_OP} = u_{cn\_OP}, & \vec{v_3} \,\&\, \vec{v_4} \,\&\, \vec{v_0} \,\&\, \vec{v_7} \end{cases} \tag{3-6}$$

According to Eq. (3-3) and Eq. (3-4), the post-fault phase voltages sum up to zero. By incorporating relationships of u_{bn_OP} and u_{cn_OP} from Eq. (3-6) into $u_{an\_OP} + u_{bn\_OP} + u_{cn\_OP} = 0$, u_{bn_OP} and u_{cn_OP} in each switching state can be substituted by each other, as shown in Eq. (3-7).

By incorporating $u_{an\_OP} = V_{bemfa}$ from Eq. (3-3) into Eq. (3-7), the post-fault phase voltages u_{bn_OP} and u_{cn_OP} can be calculated by V_{DC} and V_{bemfa}, as shown in Eq. (3-8).

$$\begin{cases} u_{an\_OP} + u_{bn\_OP} + u_{bn\_OP} - V_{DC} = 0 \\ u_{an\_OP} + u_{cn\_OP} + V_{DC} + u_{cn\_OP} = 0, & \vec{v_2} \,\&\, \vec{v_6} \end{cases}$$
$$\begin{cases} u_{an\_OP} + u_{bn\_OP} + u_{bn\_OP} + V_{DC} = 0 \\ u_{an\_OP} + u_{cn\_OP} - V_{DC} + u_{cn\_OP} = 0, & \vec{v_1} \,\&\, \vec{v_5} \end{cases} \tag{3-7}$$
$$\begin{cases} u_{an\_OP} + 2u_{bn\_OP} = 0 \\ u_{an\_OP} + 2u_{cn\_OP} = 0, & \vec{v_3} \,\&\, \vec{v_4} \,\&\, \vec{v_0} \,\&\, \vec{v_7} \end{cases}$$

$$\begin{cases} u_{bn\_OP} = \dfrac{V_{DC} - V_{bemfa}}{2};\ u_{cn\_OP} = \dfrac{-V_{DC} - V_{bemfa}}{2}, & \vec{v_2}\ \&\ \vec{v_6} \\ u_{bn\_OP} = \dfrac{-V_{DC} - V_{bemfa}}{2};\ u_{cn\_OP} = \dfrac{V_{DC} - V_{bemfa}}{2}, & \vec{v_1}\ \&\ \vec{v_5} \\ u_{bn\_OP} = \dfrac{-V_{bemfa}}{2};\ u_{cn\_OP} = \dfrac{-V_{bemfa}}{2}, & \vec{v_3}\ \&\ \vec{v_4}\ \&\ \vec{v_0}\ \&\ \vec{v_7} \end{cases} \tag{3-8}$$

It can be seen from Eq. (3-8) that the post-fault u_{bn} and u_{cn} are not constant values in each switching state, but float with the voltage of the opened phase A, which is V_{bemfa}.

3.3 Current Prediction Model for PMSM Drives under the Open-Phase Fault

By far, the post-fault phase voltages have been identified and can be calculated in each switching cycle by V_{DC} and V_{bemfa}. In current prediction, phase voltages are the activation sources of current increments in each switching cycle. Therefore, based on the derived post-fault phase voltages, the post-fault current prediction model under the OP fault is proposed to facilitate the fault-tolerant model-predictive control and validate the correctness of the derived post-fault phase voltages.

3.3.1 Current Prediction Model under Healthy Condition

The current prediction model under the healthy condition can be derived from the linear *dq* model as shown in Eq. (3-9), where u_d, u_q, i_d, i_q, L_d, L_q are voltages, currents, and inductances in *dq*-axes:

$$\begin{cases} u_d = R_s i_d + L_d (di_d/dt) - \omega_e L_q i_q \\ u_q = R_s i_q + L_q (di_q/dt) + \omega_e L_d i_d + \omega_e \Psi_f \end{cases} \tag{3-9}$$

By incorporating the Euler approximation, the current prediction model under the healthy condition can be expressed in (3-10), where k and k+1 denote the values at the current step and the next step, respectively, and T_s is the switching period. In (3-10), u_d^k and u_q^k activate the current behavior in each switching period, but they cannot be sampled

$$\begin{cases} i_d^{k+1} = (1 - T_s R_s / L_d) i_d^k + T_s \omega_e^k i_q^k + T_s u_d^k / L_d \\ i_q^{k+1} = (1 - T_s R_s / L_q) i_q^k - T_s \omega_e^k i_d^k - T_s (\Psi_f / L_q) \omega_e^k + T_s u_q^k / L_q \end{cases} \quad (3\text{-}10)$$

The conventional model approximate u_d^k and u_q^k by voltage commands from current controllers, viz. u_d^* and u_q^*. When the motor drive is healthy, the voltage commands can be correctly implemented to phase windings where phase voltages vary between $0, \pm(1/3)V_{DC}$ and $\pm(2/3)V_{DC}$ in switching states, as summarized in Eq. (3-11).

$$\begin{cases} u_{an} = -V_{DC}/3; u_{bn} = -V_{DC}/3;\ u_{cn} = 2V_{DC}/3, & \vec{v}_1 \\ u_{an} = -V_{DC}/3; u_{bn} = 2V_{DC}/3;\ u_{cn} = -V_{DC}/3, & \vec{v}_2 \\ u_{an} = -2V_{DC}/3; u_{bn} = V_{DC}/3;\ u_{cn} = V_{DC}/3, & \vec{v}_3 \\ u_{an} = 2V_{DC}/3; u_{bn} = -V_{DC}/3;\ u_{cn} = -V_{DC}/3, & \vec{v}_4 \\ u_{an} = V_{DC}/3; u_{bn} = -2V_{DC}/3;\ u_{cn} = V_{DC}/3, & \vec{v}_5 \\ u_{an} = V_{DC}/3; u_{bn} = V_{DC}/3;\ u_{cn} = -2V_{DC}/3, & \vec{v}_6 \end{cases} \quad (3\text{-}11)$$

However, under the OP fault, the post-fault phase voltages do not follow the values in Eq. (3-11). Moreover, the fault also affects L_d and L_q. Hence, establishing the prediction model in the *dq* coordinate is less convenient than predicting the post-fault currents in the independent *abc* coordinate.

3.3.2 Open-Phase Current Prediction Model based on Independent Phase Models

In the most-related literature [92], the post-fault phase voltages are updated by considering the absence of the OP leg, as shown in Eq. (3-12).

$$\begin{cases} u_{an} = 0; u_{bn} = -V_{DC}/2;\ u_{cn} = V_{DC}/2, & \vec{v}_1 \,\&\, \vec{v}_5 \\ u_{an} = 0; u_{bn} = V_{DC}/2;\ u_{cn} = -V_{DC}/2, & \vec{v}_2 \,\&\, \vec{v}_6 \\ u_{an} = 0; u_{bn} = 0;\ u_{cn} = 0, & \vec{v}_3 \,\&\, \vec{v}_4 \end{cases} \quad (3\text{-}12)$$

Then, the voltage excitations u_d^k and u_q^k are obtained by using coordinate transformation, as shown in Eq. (3-13) and (3-14).

$$\begin{pmatrix} u_d^k \\ u_q^k \end{pmatrix} = C_{3s-2r} \begin{pmatrix} u_{an} \\ u_{bn} \\ u_{cn} \end{pmatrix} \tag{3-13}$$

$$C_{3s-2r} = \frac{2}{3} \begin{pmatrix} \cos\theta_e & \cos(\theta_e - 2\pi/3) & \cos(\theta_e + 2\pi/3) \\ -\sin\theta_e & -\sin(\theta_e - 2\pi/3) & -\sin(\theta_e + 2\pi/3) \end{pmatrix} \tag{3-14}$$

However, the assumed post-fault phase voltages in [92] do not consider the fluctuating V_{bemfa} which affects the voltage at the neutral point. Under the OP fault, as described in Eq. (3-8), the post-fault phase voltages do not follow the values in Eq. (3-11) or (3-12), and cannot track the voltage commands u_d^* and u_q^*. Moreover, the OP fault also affects L_d and L_q, which have not been taken into account.

In order to take the post-fault inductances into account, the current prediction model is established based on the independent three-phase model shown in Eq. (3-3). According to Eq. (3-3) and applying the same Euler approximation, the open-phase phase current prediction model is described in Eq. (3-15):

$$\begin{cases} i_{b\_OP}^{k+1} = (1 - \dfrac{2R_sT_s}{3L_s}) i_{b\_OP}^k + \dfrac{2T_s\Psi_f\omega_e}{3L_s} \sin(\theta_e - \dfrac{2\pi}{3}) + \dfrac{T_s u_{bn\_OP}^k}{L_s} \\ i_{c\_OP}^{k+1} = (1 - \dfrac{2R_sT_s}{3L_s}) i_{c\_OP}^k + \dfrac{2T_s\Psi_f\omega_e}{3L_s} \sin(\theta_e - \dfrac{4\pi}{3}) + \dfrac{T_s u_{cn\_OP}^k}{L_s} \end{cases} \tag{3-15}$$

Incorporating the post-fault phase voltages from Eq. (3-8) into the $u_{bn\_OP}^k$ and $u_{cn\_OP}^k$ in Eq. (3-15), the post-fault phase currents can be predicted. To validate the correctness of the analysis and compare the predicted post-fault currents with the previous models, the predicted phase currents in (3-15) are transformed into the *dq* coordinate as described in Eq. (3-16):

$$\begin{pmatrix} i_{d\_OP}^{k+1} \\ i_{q\_OP}^{k+1} \end{pmatrix} = C_{3s-2r} \begin{pmatrix} 0 \\ i_{b\_OP}^{k+1} \\ i_{c\_OP}^{k+1} \end{pmatrix} \tag{3-16}$$

3.4 Experimental Validation

In this section, the post-fault phase voltages derived in Section 3.2 and the post-fault current prediction model built in Section 3.3 are validated on a 3P2L PMSM drive controlled by DSP TMS320F28335 operating at 150 MHz. The neutral point of the tested PMSM is led out by connecting the terminals at the same ends of an open-end winding PMSM. The parameters of the employed PMSM are shown in Table 3-1. It is noteworthy that the analysis and methods of this research are directly validated in experiments because experimental validation is more convenient than simulation validation. Co-simulation and motor models based on Finite Element Analysis are required to enhance the simulation fidelity, while the DSP-based experimental setup is more compatible with the linear models derived in this paper.

The control scheme is based on PI controllers, FOC, and SVPWM, as shown in Fig. 3-2.

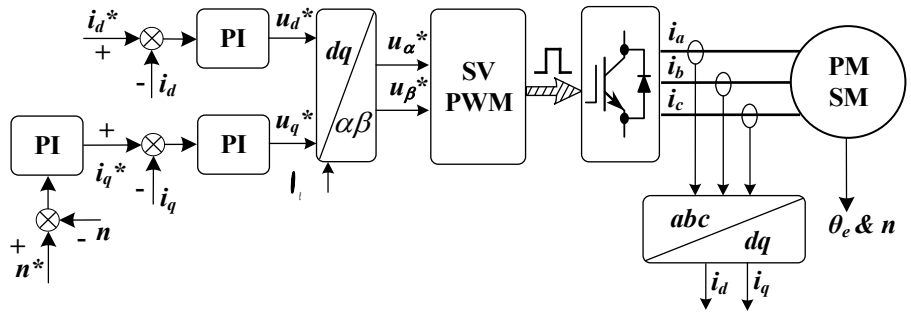


Fig. 3-2. Control scheme based on PI controllers, FOC, and SVPWM.

TABLE 3-1 Parameters of PMSM

Parameter	Value	Unit
stator winding resistance R_s	1.32	Ω
d-axis inductance L_d	3.21	mH
q-axis inductance L_q	3.21	mH
number of pole pairs *p*	4	-
flux of the rotor PM Ψ_f	0.1467	Wb
rated speed	1800	rpm
rated power	750	W
rated torque	4	N. m

The rotor electrical angle and speed are detected by a resolver and sampled by a resolver-to-digital converter (AD2S1210) at 14-bit resolution. Phase currents are sensed by current sensors (HX 15-P). The 12-bit analog-to-digital converter (ADC) of the DSP samples the

analog signals from the current sensors. The inverter is based on the IGBT module *FUJI* 7MBR25VA120-50 and works at a switching frequency of 10 kHz. A breaker is mounted between the inverter and the motor phase to emulate the OP fault. Variables in the DSP are transmitted to an oscilloscope via a 10-bit digital-to-analog converter (DAC). Additionally, current probes (*Cybertek* CP8050A, 50 MHz) and voltage probes (*Tektronix* P5200, 50 MHz) are used for measurement. The experimental setups are shown in Fig. 3-3.

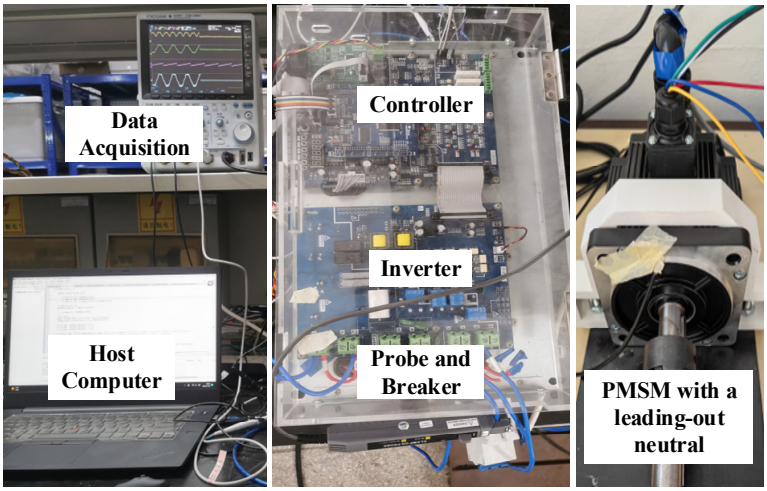


Fig. 3-3. Experimental setups.

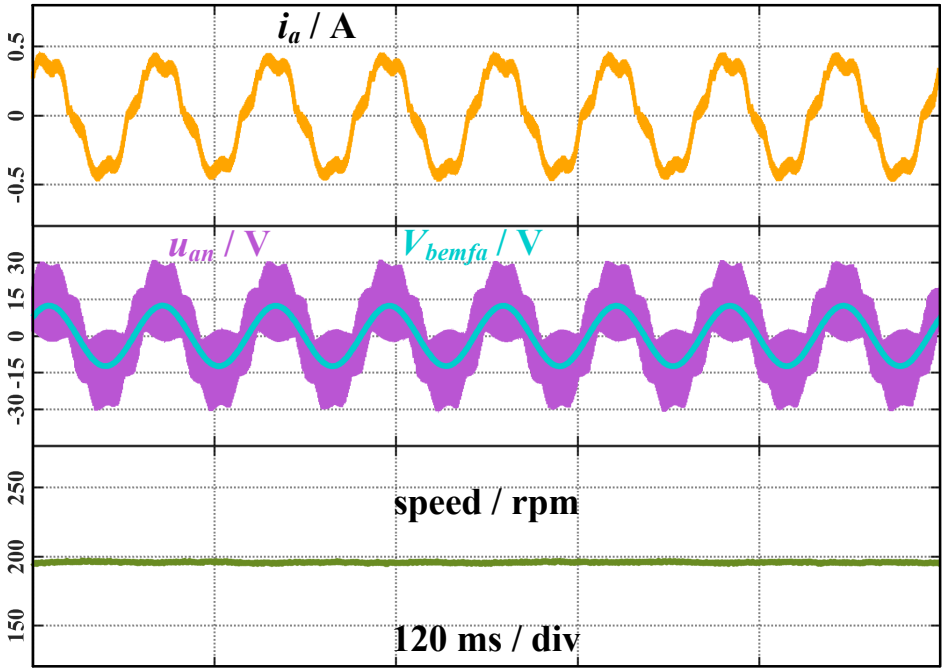


Fig. 3-4. Responses of motor speed and phase A current, voltage, and back-EMF when no fault occurs.

3.4.1 Validation of Phase Voltages under the Open-Phase Fault.

This subsection exhibits the post-fault phase voltage measurement results in accordance with each switching state to validate the voltage derivation in Section 3.2, specifically Eq. (3-8).

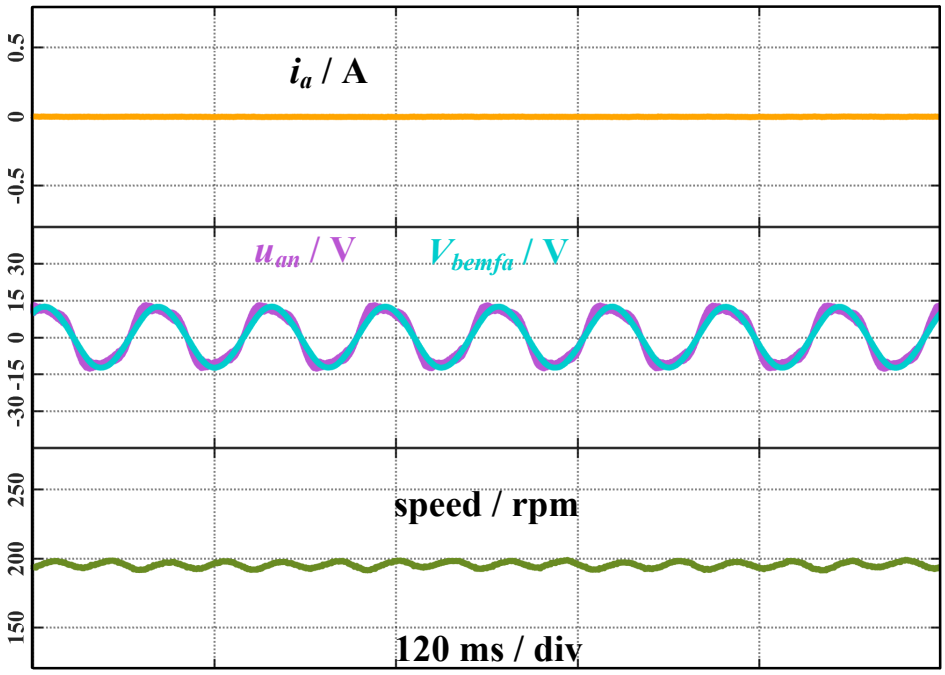


Fig. 3-5. Responses of motor speed and phase A current, voltage, and back-EMF under phase A open-phase fault.

When no fault occurs, the voltage, current, and fundamental component of phase A back-EMF are presented in Fig. 3-4, and the above states under the OP fault are shown in Fig. 3-5. In experiments, the motor operates at a constant speed level of 200 rpm under a 50 V DC bus voltage. The fundamental component of phase A back-EMF is calculated based on Eq. (3-2), where the rotor flux linkage Ψ_f is measured previously based on the line-to-line voltage under the open-circuit test of the tested motor.

In Fig. 3-4, where no fault occurs, the phase A back-EMF, V_{bemfa}, maintains a sinusoidal pattern as depicted in Eq. (3-2). When the motor drive is healthy, the phase voltage u_{an} has 5 voltage levels, which are 0, $\pm V_{DC}/3$, and $\pm 2V_{DC}/3$, complying with the principle of SVPWM.

Comparatively, in Fig. 3-5, the phase A current, i_a, cannot conduct anymore, which eliminates the voltage drops on the phase A resistance and self-inductance. Meanwhile, due to the equal amplitudes of the post-fault phase B and C currents, the voltages induced by mutual inductances on phase A are mutually canceled. Therefore, the post-fault u_{an} retains only its back-EMF, V_{bemfa}, induced by the rotor flux linkage, which still largely maintains a sinusoidal pattern as the motor speed is not significantly influenced by the open-phase fault

due to the rotor inertia. As a result, the measured u_{an} complies with the calculated V_{bemfa}, as shown in the second scope of Fig. 3-5.

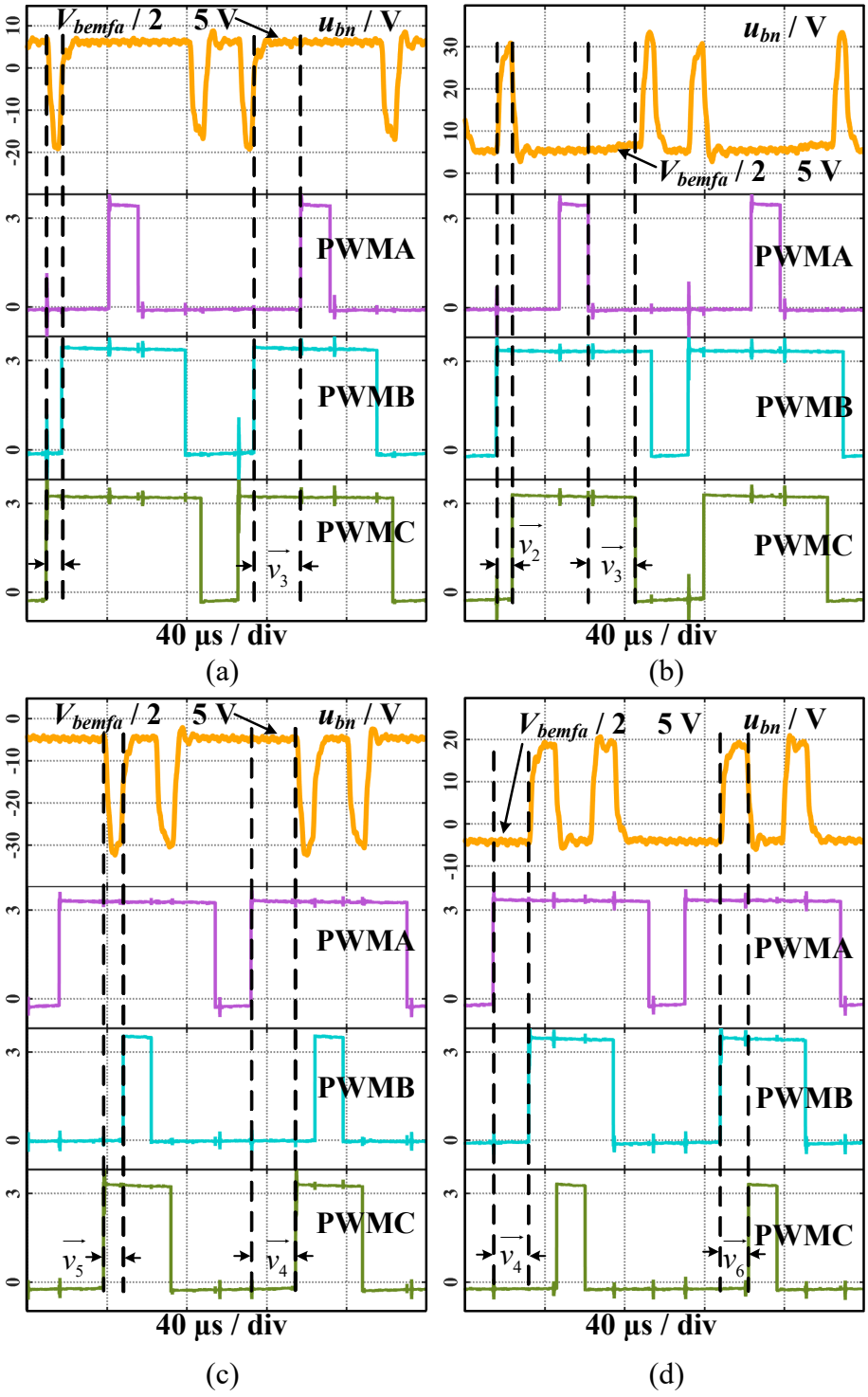


Fig. 3-6. Post-fault phase B voltage in each switching state: (a) $\vec{v}_1$, $\vec{v}_3$, $\vec{v}_0$ & $\vec{v}_7$; (b) $\vec{v}_2$, $\vec{v}_3$, $\vec{v}_0$ & $\vec{v}_7$; (c) $\vec{v}_4$, $\vec{v}_5$, $\vec{v}_0$ & $\vec{v}_7$; (d) $\vec{v}_4$, $\vec{v}_6$, $\vec{v}_0$ & $\vec{v}_7$.

The post-fault voltages of phase B are shown in Fig. 3-6 in accordance with each switching state as derived in Eq. (3-8).

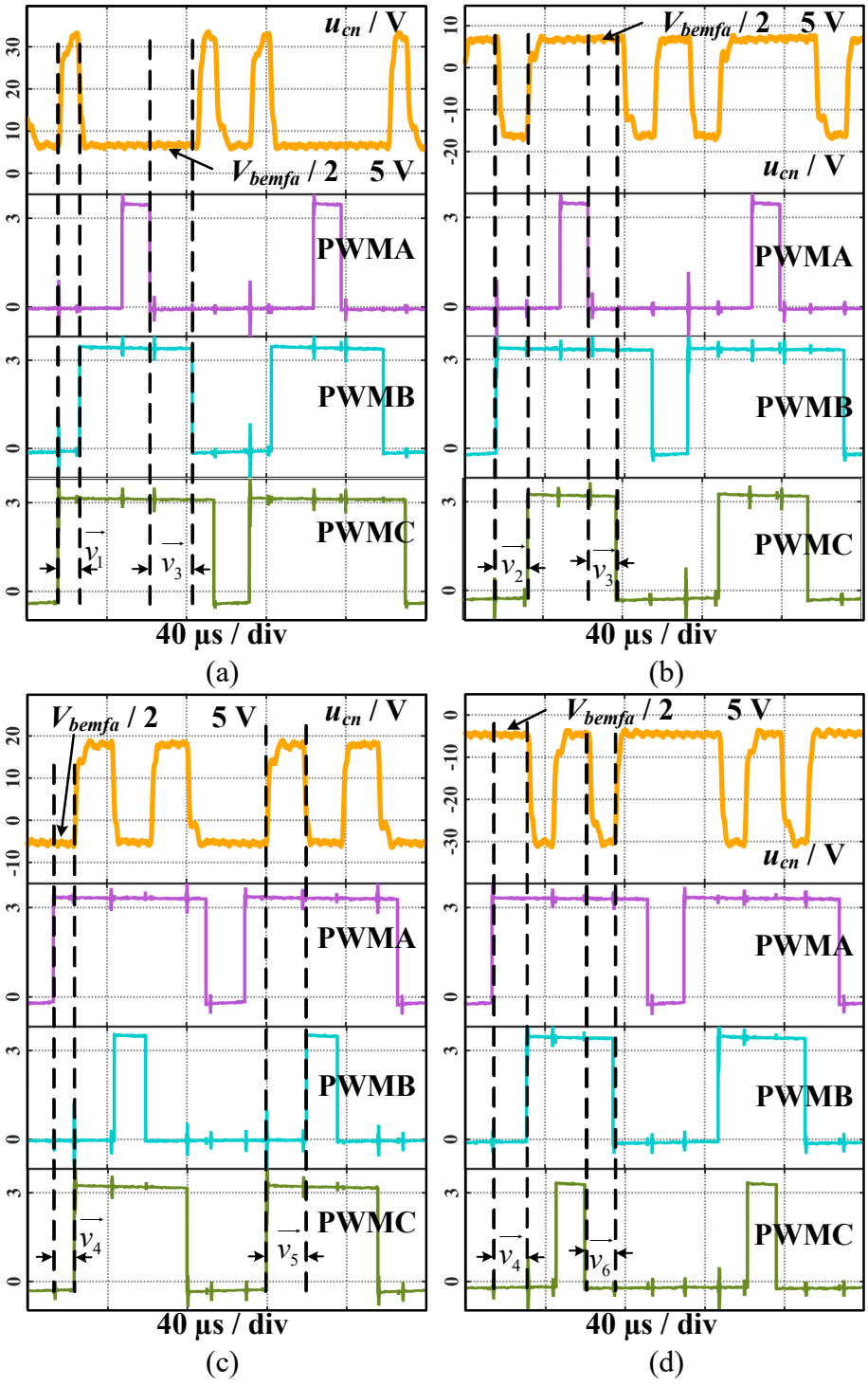


Fig. 3-7. Post-fault phase C voltage in each switching state: (a) $\vec{v}_1$, $\vec{v}_3$, $\vec{v}_0$ & $\vec{v}_7$; (b) $\vec{v}_2$, $\vec{v}_3$, $\vec{v}_0$ & $\vec{v}_7$; (c) $\vec{v}_4$, $\vec{v}_5$, $\vec{v}_0$ & $\vec{v}_7$; (d) $\vec{v}_4$, $\vec{v}_6$, $\vec{v}_0$ & $\vec{v}_7$.

It can be seen from Fig. 3-6 (a) to (d) that the post-fault u_{bn} is equal to ($-V_{bemfa}$ / 2) within switching states $\vec{v}_3$, $\vec{v}_4$, $\vec{v}_0$ & $\vec{v}_7$. Furthermore, the post-fault u_{bn} also follows the analysis in Eq. (3-8) within other switching states. For instance, within $\vec{v}_1$ in Fig. 3-6 (a) where V_{DC} is set as 50 V and V_{bemfa} is around −10 V, u_{bn} is approximately equal to −20 V which follows the value

of $(-V_{DC} - V_{bemfa})/2$; within $\overrightarrow{v_6}$ in Fig. 3-6 (d) where V_{bemfa} is around 10 V, u_{bn} is close to 20 V which complies with the value of $(V_{DC} - V_{bemfa})/2$.

The post-fault phase C voltage u_{cn} in each switching state is shown in Fig. 3-7. Also, u_{cn} follows $(-V_{bemfa}/2)$ within switching states $\overrightarrow{v_3}$, $\overrightarrow{v_4}$, $\overrightarrow{v_0}$ & $\overrightarrow{v_7}$ and is complementary to u_{bn} in other switching states. For instance, within $\overrightarrow{v_1}$ in Fig. 3-7 (a) where V_{bemfa} is −10 V, u_{cn} is approximately equal to 30 V following $(V_{DC} - V_{bemfa})/2$ as depicted in Eq. (3-8). Therefore, the post-fault phase voltages summarized in Eq. (3-8) are validated by the experimental results and they still sum up to zero under the OP fault.

3.4.2 Validation of the Current Prediction Model under the Open-Phase Fault

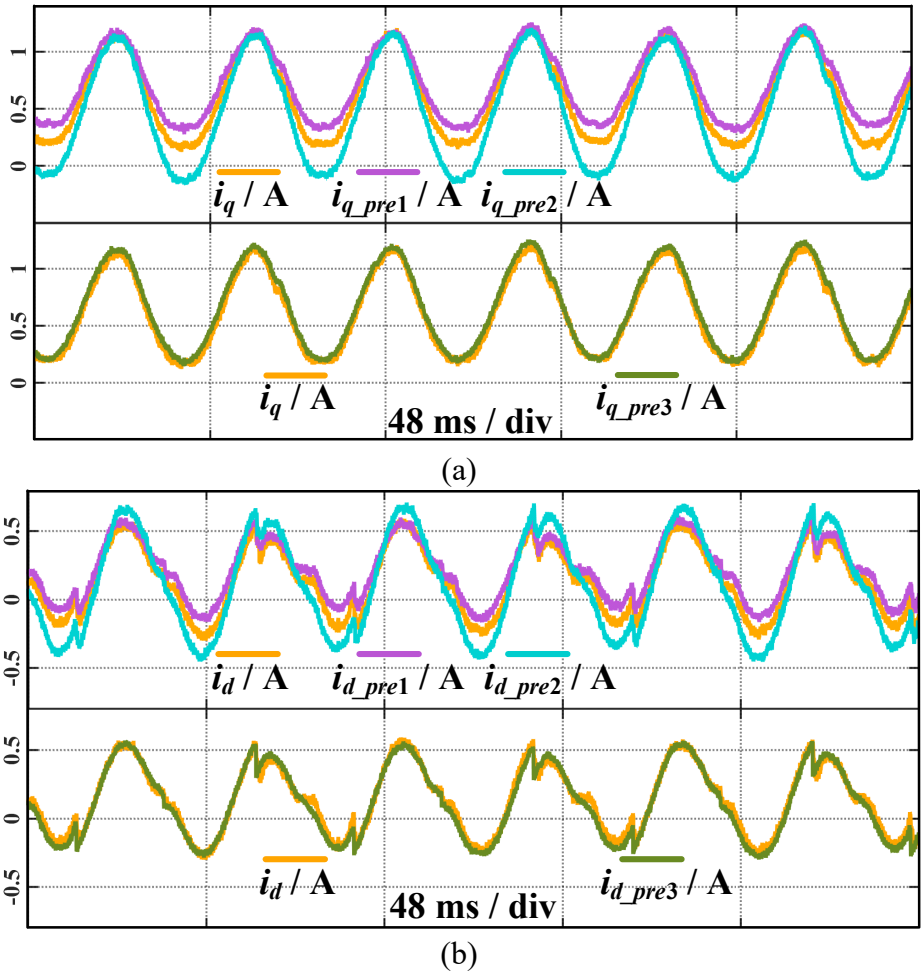


Fig. 3-8. Comparison between the current feedback, the current predicted by the healthy model, the current predicted by the model in [92], and the current predicted by the proposed model of this chapter.

To validate the proposed post-fault current prediction model, the predicted currents, named

i_{q_pre3} and i_{d_pre3}, from the proposed model are compared with the current feedback i_q and i_d, the predicted currents i_{q_pre1} and i_{d_pre1} from the healthy prediction model, and the predicted currents i_{q_pre2} and i_{d_pre2} from the model in [92]. The comparison results are presented in Fig. 3-8. It can be seen from Fig. 3-8 (a) and (b) that, the predicted currents from the healthy model and the model in [92] deviate from the actual current feedback, while the current predicted by the proposed model can accurately track the current feedback, which validates the correctness and improvement of the proposed model.

It is noted that the average electromagnetic torque under the OP fault is not zero, implying that the post-fault magnetomotive force (MMF) generated by the winding is not fixed at a constant spatial phase.

When the motor is under healthy condition, sinusoidal currents in the three-phase winding generate spatially symmetric sinusoidal MMF, ultimately synthesizing a rotating MMF. However, under the phase-A OP fault, due to the equal amplitude and opposite direction of currents in the remaining healthy phases, a pulsating MMF is eventually established at spatial phases of π/2 and 3π/2, as shown in Fig. 3-9, where Im is the amplitude of phase currents; N is the winding turns.

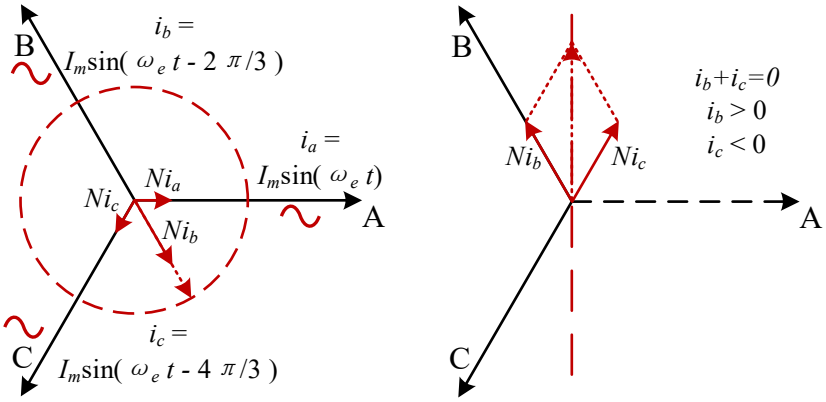


Fig. 3-9. MMF generated by windings under (a) the healthy condition and (b) phase A OP fault condition.

The pulsating MMF leads to significant torque fluctuations. For instance, when the rotor electrical angle is located at π/2 and 3π/2, the electromagnetic torque inevitably drops to zero because of the overlapping spatial phases of the rotor and stator magnetic field. However, it still possesses the capability to drive the rotor magnetic field of the motor, thus avoiding the necessity of shutdown after an OP fault.

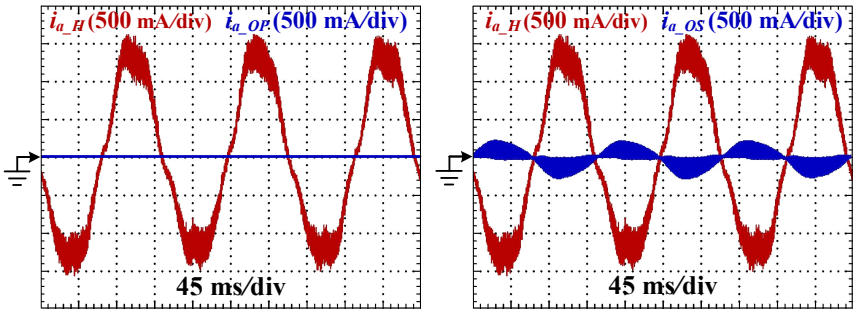
3.5 Summary

This chapter derives the post-fault phase voltages under the OP fault and proposes an improved current prediction model that can accurately estimate the post-fault current dynamics. Firstly, in each switching state, the post-fault phase voltages are derived by considering the floating neutral voltage incurred by the back-EMF. Furthermore, by incorporating the derived phase voltages as the activation sources in each switching cycle, the post-fault current prediction model is established. Moreover, the changes of inductances under the OP fault are taken into account by establishing the model in the independent phase model. Furthermore, it is noteworthy that the phase inductances also change following the variation of magnetic saturation, especially considering the increased phase currents under fault conditions. To further describe the post-fault model in the future, the inductance changes posed by magnetic saturation should also be taken into account to establish a non-linear model. Finally, experimental results validate the derived post-fault phase voltages and the post-fault current prediction model. Compared with the previous models, the proposed model has better agreement with the practical post-fault motor drive.

Chapter 4 **Modelling of the Open-Switch Fault**

4.1 Introduction

Based on the post-fault phase voltages derived in Section 3.2, the current dynamic model under the OS fault can be established in this chapter. The post-fault current under the OS fault is the most significant difference between the OP fault and the OS fault, as shown in Fig. 4-1, where i_{a_H}, i_{a_OP}, and i_{a_OS} are measured by a current probe and stand for the current when the phase is under the healthy condition, the OP fault, and the OS fault, respectively. i_{a_OP} is zero because both the power switches and diodes in the faulty phase cannot conduct current under the OP fault; whereas, under the OS fault, the still functional diodes maintain current paths. If i_{a_OS} can be sampled and estimated by the motor drive itself, diagnostic rules can be conveniently designed to classify the OP fault and the OS fault.



(a) (b)

Fig. 4-1. Comparison of phase current under (a) Healthy condition and OP fault; (b) Healthy condition and OS fault.

However, the mechanism of the post-fault current under the OS fault remained unidentified. Hence, it remains confusing to identify the phase points where the post-fault current could reach its maximum amplitude. As a result, the motor drive cannot arrange appropriate sampling points to detect the maximum value of i_{a_OS}. Furthermore, as the mechanism of i_{a_OS} was not revealed, i_{a_OS} cannot be estimated due to the absence of its dynamics in each switching state. Consequently, the motor drive was unable to classify these two types of faults and to locate the specific component failures.

This chapter reveals the mechanism of the OS conduction on the scale of the switching period

and proposes a model that can calculate the post-fault conducting current in real time by the following steps:

1) First, the conduction conditions of the upper and lower diodes are separately analyzed at different speed levels. The conduction condition is the most important factor that determines the sign of i_{a_OS} and the required connecting states of the inverter.

2) Based on the conduction conditions and connecting states required to achieve the conduction conditions, the switching states qualified to conduct the faulty phase are revealed, according to the polarity and amplitude of the back-EMF. Furthermore, the conduction time of i_{a_OS} is summarized by considering the acting time of voltage vectors and the dead time of power switches.

3) After obtaining the conduction time, an estimation model of i_{a_OS} is proposed based on the equivalent circuits that correspond to the connecting states of the switching states. The estimation model can accurately calculate i_{a_OS} at different speed levels on the scale of tens of milliamperes.

4) Finally, the analysis of the conduction conditions and conduction time, current and voltage dynamics, and estimation model are validated through experiments.

4.2 Remaining Current Paths under the Open-Switch Fault

4.2.1 Conduction Conditions of Post-fault Current under the Open-Switch Fault

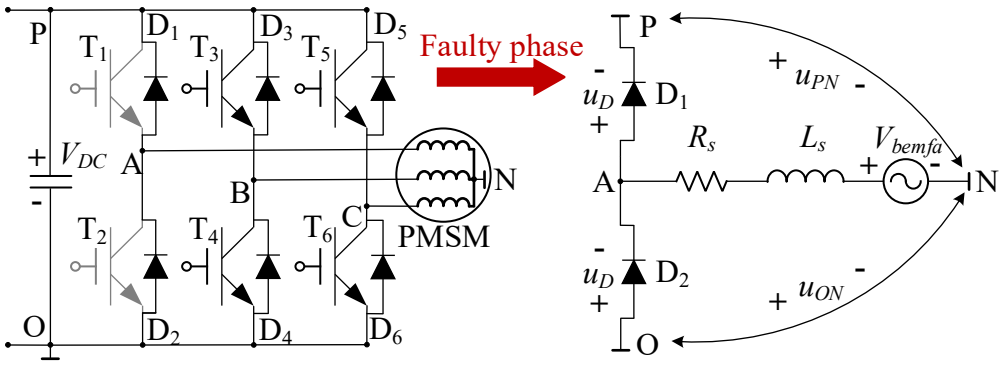


Fig. 4-2. Open-Switch Post-fault schematic and phase-A equivalent circuit.

Similarly, assuming that the OS faults occur in phase A, the post-fault schematic and equivalent circuit are shown in Fig. 4-2, where u_D is the forward on-voltage of the reverse diode. V_{bemfa} acts as the only potential source of the post-fault current in the OS phase because a) V_{DC} has been blocked by the anti-parallel diodes and b) the post-fault currents of phases B and C have reverse polarities but almost identical amplitudes; thus, the voltages induced by mutual inductances are almost mutually canceled and are negligible compared with the back-EMF which is the primary voltage excitation and is at levels of tens to hundreds volts. Moreover, the conduction of the faulty phase depends on the voltage differences between the neutral point of the stator winding N and power source rails, viz. u_{PN} and u_{ON}.

When $V_{bemfa} > 0$ V, D_1 can conduct, while D_2 is intrinsically reverse-biased by the negative rail and V_{bemfa} positive polarity. According to Fig. 4-2, D_1 can be conducted if the voltage difference u_{AP} can cover u_D. Before the conduction of D_1, V_{bemfa} is the only voltage source of phase A since its current is still 0 before its conduction. Hence, the conduction condition of D_1 can be described as follows:

$$u_{AP} = u_{an} - u_{PN} = V_{bemfa} - u_{PN} > u_D \tag{4-1}$$

u_D can be neglected compared with V_{bemfa} and u_{PN}. For example, in terms of the experimental setup of this case, u_D is 1.5 V and can be easily covered by V_{bemfa} if the motor speed is higher than 25 rpm, which is far less than its nominal speed.

4.2.2 Inverter Connections Corresponding to Conduction Conditions

In Eq. (4-1), u_{PN} determines the conduction of D_1, and it is necessary to study the state of u_{PN} before the conduction of D_1. Since the driving signals of the faulty phase are invalid under the OS fault, the remaining possible connecting states before the D_1 conduction are shown in Fig. 4-3.

The state of u_{PN} and its relationship with V_{bemfa} will be separately discussed according to the above states. In the four states of Fig. 4-3, because D_1 has not been conducted and the drive is temporarily under the OP fault, the following equations of phase currents hold true: $i_a = 0$ and $i_b = -i_c$, and the sum of the three-phase voltages is zero, viz. $u_{an} + u_{bn} + u_{cn} = 0$, as illustrated in Eq. (3-4). In Figs. 4-3 (a) and (b), because both phases B and C are connected to the DC

rails, the line-to-line voltage is $u_{BC} = 0 = u_{BN} - u_{CN}$. Applying it into $u_{an} + u_{bn} + u_{cn} = 0$, the phase voltages can be expressed by Eq. (4-2).

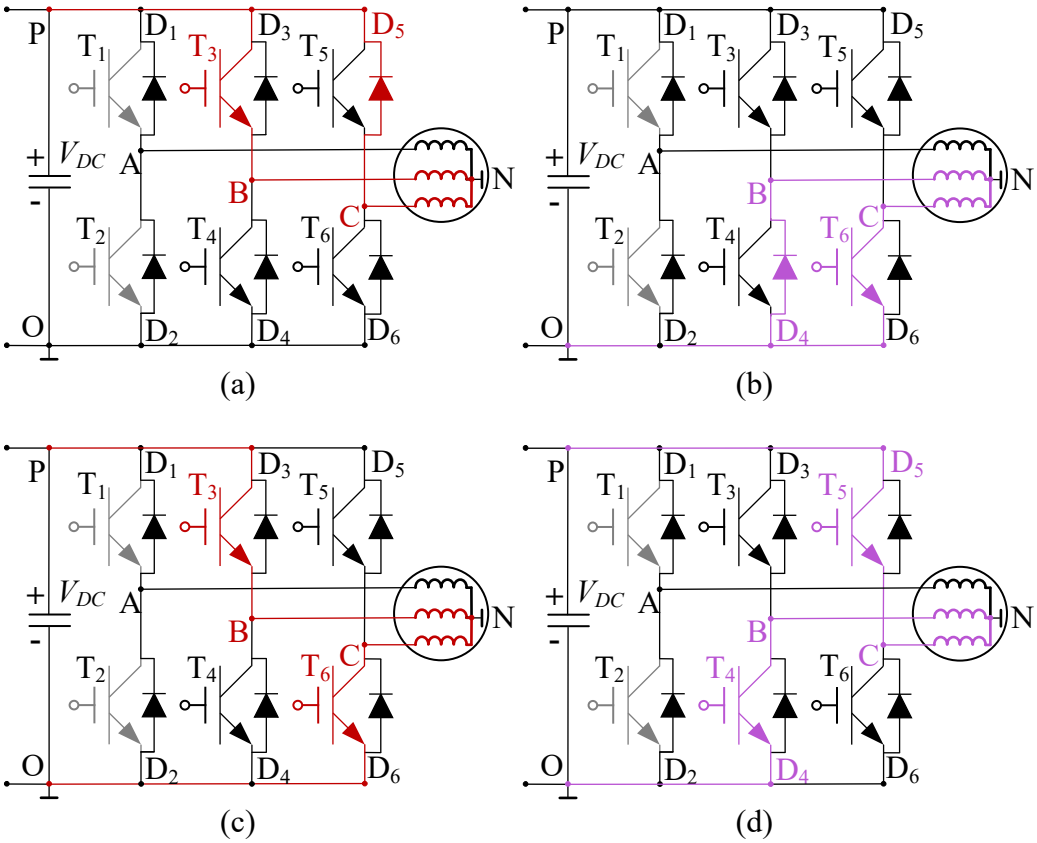


Fig. 4-3. Post-fault conduction paths that connect phases B and C (a) to the positive rail; (b) to the negative rail; (c) & (d) to the positive and negative rails separately.

$$u_{bn} = u_{cn} = \frac{-u_{an}}{2} = \frac{-V_{bemfa}}{2} \tag{4-2}$$

In Fig. 4-3 (a), $u_{PN} = u_{bn} = u_{cn} = -V_{bemfa}/2$, and the condition in Eq. (4-1) is transformed to:

$$u_{AP} = u_{an} - u_{PN} = V_{bemfa} - (-\frac{V_{bemfa}}{2}) = \frac{3V_{bemfa}}{2} > 0 \tag{4-3}$$

The condition in Eq. (4-3) can be achieved by V_{bemfa} at all speed levels. Hence, D_1 can be conducted by connecting phases B and C to the positive rail. Comparatively, in Fig. 4-3 (b), $u_{ON} = u_{bn} = u_{cn} = -V_{bemfa}/2$, and u_{PN} can be obtained from:

$$u_{PN} = u_{PO} + u_{ON} = V_{DC} - \frac{V_{bemfa}}{2} \tag{4-4}$$

The condition in Eq. (4-1) can be transformed to:

$$u_{AP} = u_{an} - u_{PN} = \frac{3V_{bemfa} - 2V_{DC}}{2} > 0 \tag{4-5}$$

$V_{bemfa} > (2V_{DC}/3)$ is required to satisfy the condition in Eq. (4-5). However, $V_{bemfa} > (2V_{DC}/3)$ cannot be achieved in a 3P2L PMSM drive. $(2V_{DC}/3)$ is the maximum instant value that the phase voltage can reach in a three-phase two-level inverter. For example, $u_{an} = (2V_{DC}/3)$ when $\overrightarrow{v_4}(100)$ is being applied. According to the PWM principle, the phase voltage is the synthesized voltage-second value of the instant phase voltage and its acting time. Considering the principle of SVPWM and the effect of the dead time, the acting time of the instant value $(2V_{DC}/3)$ does not account for the entire switching cycle. Therefore, the phase voltage cannot reach $(2V_{DC}/3)$. Furthermore, according to the phase voltage equilibrium, the phase voltage is equal to the summary of V_{bemfa} and voltage drops on the resistance and inductance. Hence, V_{bemfa} cannot reach $(2V_{DC}/3)$, and connecting phases B and C to the negative rail cannot conduct D_1.

By incorporating $u_{BC} = V_{DC} = u_{bn} - u_{cn}$ and $u_{BC} = -V_{DC} = u_{bn} - u_{cn}$ into $u_{an} + u_{bn} + u_{cn} = 0$, the phase voltages in Fig. 4-3 (c) and (d) can be illustrated in Eq. (4-6) and (4-7), respectively.

$$u_{bn} = \frac{V_{DC} - V_{bemfa}}{2} = u_{PN}; u_{cn} = \frac{-V_{DC} - V_{bemfa}}{2} = u_{ON} \tag{4-6}$$

$$u_{bn} = \frac{-V_{DC} - V_{bemfa}}{2} = u_{ON}; u_{cn} = \frac{V_{DC} - V_{bemfa}}{2} = u_{PN} \tag{4-7}$$

The condition in Eq. (4-1) can be transformed to:

$$u_{AP} = u_{an} - u_{PN} = \frac{3V_{bemfa} - V_{DC}}{2} > 0 \tag{4-8}$$

Eq. (4-8) shows that D_1 can be conducted by separately connecting phases B and C to the positive and negative rails at high speeds if the following condition is satisfied:

$$V_{bemfa} > \frac{V_{DC}}{3} \tag{4-9}$$

When $V_{bemfa} < 0$, D_2 has the potential to conduct, but the condition in Eq. (4-1) has changed to:

$$u_{OA} = u_{ON} - u_{an} = u_{ON} - V_{bemfa} > 0 \tag{4-10}$$

By applying the same analysis, the conduction condition in Eq. (4-10) is discussed according to the four connecting states in Fig. 4-3 as follows:

a) In Fig. 4-3 (a), $u_{ON} = u_{OP} + u_{PN} = -V_{DC} - V_{bemfa}/2$, and the condition in Eq. (4-10) is transformed to:

$$u_{OA} = u_{ON} - u_{an} = -\frac{(3V_{bemfa} + 2V_{DC})}{2} > 0 \tag{4-11}$$

b) In Fig. 4-3 (b), the condition in Eq. (4-10) is transformed to Eq. (4-12). The condition in Eq. (4-12) can be achieved at all speed levels. Therefore, D_2 can be conducted at all speed levels by connecting phases B and C to the negative rail.

$$u_{OA} = u_{ON} - u_{an} = -\frac{3V_{bemfa}}{2} > 0 \tag{4-12}$$

c) In Figs. 4-3 (c) and (d), the condition in Eq. (4-10) has been transformed to Eq. (4-13), which indicates that At high speeds where $V_{bemfa} < -(V_{DC}/3)$, D_2 can be conducted by separately connecting phases B and C to the positive rail and negative rail.

$$u_{OA} = u_{ON} - u_{an} = -\frac{(3V_{bemfa} + V_{DC})}{2} > 0 \tag{4-13}$$

4.3 Activating Switching States of the Post-fault Current

4.3.1 Relationships between Switching States and Back-Electromagnetic Force

Because the conduction of the post-fault current is determined by the polarity of V_{bemfa} and connecting states in Fig. 4-3, the switching states that correspond to each polarity of V_{bemfa} and each condition in Fig. 4-3 will be discussed before analyzing the activating switching states that satisfy the connecting conditions of the post-fault current conduction.

In conventional FOC, the rotating reference is aligned with the rotor PM flux. Therefore, the rotor electrical angle, θ_e, determines the two adjacent acting voltage vectors in each spatial sector, while the outputs of current controllers determine the acting time of each vector. Because the flux control in FOC is oriented to the rotor electrical angle θ_e, the two adjacent

vectors control the rotation of the rotor PM flux, and the direction of their synthesized vector is orthogonal to the direction of the rotor PM flux. The distribution of voltage vectors and their relationships with θ_e are shown in Fig. 4-4:

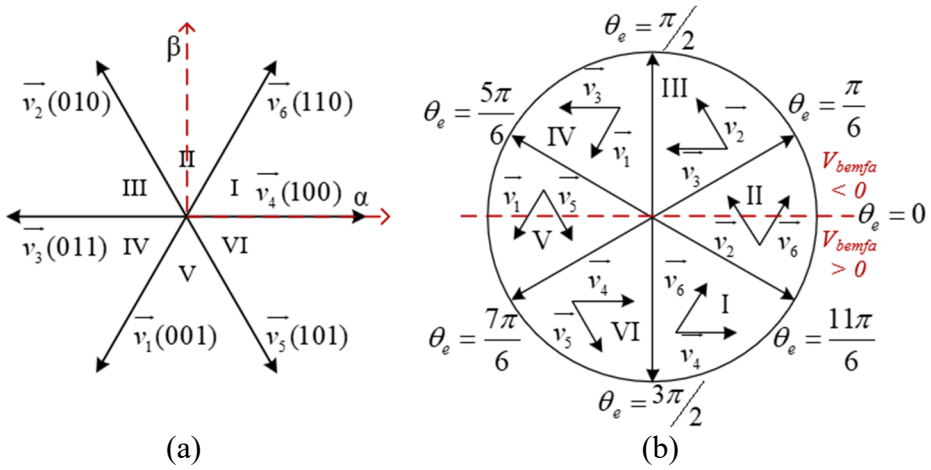


Fig. 4-4. Voltage vectors (a) and their ideal active phase ranges(b).

In Fig. 4-4 (a), the implementation of voltage vectors is governed by spatial sectors (Sector I to VI). The number of spatial sectors is assigned based on u_α* and u_β* which are the voltage references in the $\alpha\beta$ frame, as described in Table 4-1:

TABLE 4-1 Number of Spatial Sector and Voltage References

$\arctan\frac{u_\beta^*}{u_\alpha^*}$	$(0, \frac{\pi}{3})$	$(\frac{\pi}{3}, \frac{2\pi}{3})$	$(\frac{2\pi}{3}, \pi)$	$(\pi, \frac{4\pi}{3})$	$(\frac{4\pi}{3}, \frac{5\pi}{3})$	$(\frac{5\pi}{3}, 2\pi)$
Sector	I	II	III	IV	V	VI

u_α* and u_β* are transformed from u_d* and u_q*, which are the outputs of current controllers, as shown in Eq. (4-14):

$$\begin{pmatrix} u_\alpha^* \\ u_\beta^* \end{pmatrix} = \begin{pmatrix} \cos\theta_e & -\sin\theta_e \\ \sin\theta_e & \cos\theta_e \end{pmatrix} \begin{pmatrix} u_d^* \\ u_q^* \end{pmatrix} \tag{4-14}$$

Considering the ideal case where i_d = 0 in a surface-mounted PMSM, u_d* also fluctuates around 0. The assumption of u_d* = 0 stands as it is the reference of u_d, rather than the actual value of u_d. The actual value of u_d cannot be 0 when i_d = 0 because of the cross-coupling between the *d*-axis and *q*-axis as shown in Eq. (3-9). However, u_d* is calculated based on the reference and actual values of i_d. i_d* is manually set as 0 and i_d is controlled around zero. Consequently, u_d* is regulated based on the errors between i_d* and i_d and fluctuates around 0. By incorporating (18) and u_d* = 0 into arctan(u_β*/u_α*), Eq. (4-15) can be obtained:

$$\arctan\frac{u_\beta^*}{u_\alpha^*}=\arctan\frac{u_q^*\cos\theta_e}{-u_q^*\sin\theta_e}=\arctan(-\cot\theta_e) \tag{4-15}$$

Eq. (4-15) can be transformed to Eq. (4-16) according to triangular transformation where $-\cot(\theta_e)=\tan(\theta_e+{}^{\pi}/_{2})$.

$$\arctan\frac{u_\beta^*}{u_\alpha^*}=\frac{\pi}{2}+\theta_e \tag{4-16}$$

By incorporating Eq. (4-16) into Table 4-1, the ideal relationships between θ_e and spatial sectors can be summarized in Table 4-2. Furthermore, θ_e determines the polarity of V_{bemfa}, as described in Eq. (3-2). Consequently, the relationships between voltage vectors and the polarity of V_{bemfa} can be depicted in Fig. 4-4 (b).

In practice, although u_d* is not ideally equal to 0 due to errors accumulated in sampling, computation, and control, the relationship between θ_e and the number of spatial sectors still primarily conforms to Table 4-2.

TABLE 4-2 Ideal Active Phase Range of Each Spatial Sector

$\arctan\frac{u_\beta^*}{u_\alpha^*}$	$\left(0,\frac{\pi}{3}\right)$	$\left(\frac{\pi}{3},\frac{2\pi}{3}\right)$	$\left(\frac{2\pi}{3},\pi\right)$	$\left(\pi,\frac{4\pi}{3}\right)$	$\left(\frac{4\pi}{3},\frac{5\pi}{3}\right)$	$\left(\frac{5\pi}{3},2\pi\right)$
θ_e	$\left(\frac{3\pi}{2},\frac{11\pi}{6}\right)$	$\left(\frac{-\pi}{6},\frac{\pi}{6}\right)$	$\left(\frac{\pi}{6},\frac{\pi}{2}\right)$	$\left(\frac{\pi}{2},\frac{5\pi}{6}\right)$	$\left(\frac{5\pi}{6},\frac{7\pi}{6}\right)$	$\left(\frac{7\pi}{6},\frac{3\pi}{2}\right)$
Sector	I	II	III	IV	V	VI

4.3.2 Activating Switching States Satisfying Conduction Conditions

Based on the required inverter connection conditions in Fig. 4-3 and the relationships between the inverter switching states and θ_e summarized in Table 4-2, the activating switching states of the post-fault current under the OS fault can be identified.

As previously analyzed, if $V_{bemfa} > 0$, D_1 can be conducted by the state in Fig. 4-3 (a), where both the phases B and C are connected to the positive DC bus rail and can be achieved by $\overrightarrow{v_3}$ or $\overrightarrow{v_7}$(111). However, as depicted in Fig. 4-4 (b), $\overrightarrow{v_3}$ is not active when $V_{bemfa} > 0$ and is excluded from the activating switching states when $V_{bemfa} > 0$. Therefore, D_1 can be conducted by $\overrightarrow{v_7}$, with its activation time corresponding to the conduction time of the negative post-fault current when $V_{bemfa} < (V_{DC}/3)$.

Additionally, if $V_{bemfa} > (V_{DC}/3)$, the connecting states in Figs. 4-3 (c) and (d) can also conduct D_1, where the phases B and C are separately connected to the positive and negative DC bus rails. According to Fig. 4-4 (b), the conditions in Figs. 4-3 (c) and (d) can be achieved by $\overrightarrow{v_5}$ in sector VI and $\overrightarrow{v_6}$ in sector I, respectively. Therefore, at high speeds where $V_{bemfa} > (V_{DC}/3)$, the conduction time of the post-fault current includes the acting time of $\overrightarrow{v_7}$ and a part or all of the acting time of active vectors in accordance with the sector.

Similarly, because $\overrightarrow{v_4}$ is not active when $V_{bemfa} < 0$, the positive post-fault current can be conducted through D_2 by $\overrightarrow{v_0}$ at any speed when $V_{bemfa} < 0$. Furthermore, $\overrightarrow{v_5}$, $\overrightarrow{v_6}$, $\overrightarrow{v_1}$ and $\overrightarrow{v_2}$ can conduct D_2 when $V_{bemfa} < -(V_{DC}/3)$. The activating switching states of the post-fault current under the OS fault are summarized in Table 4-3:

TABLE 4-3 Activating Switching States of Post-fault Current under the OS Fault

		V	VI	I	II
$\frac{V_{DC}}{3} < V_{bemfa}$	$i_{a\_OS} < 0$	$\overrightarrow{v_7}, \overrightarrow{v_1}, \overrightarrow{v_5}$	$\overrightarrow{v_7}, \overrightarrow{v_5}$	$\overrightarrow{v_7}, \overrightarrow{v_6}$	$\overrightarrow{v_7}, \overrightarrow{v_2}, \overrightarrow{v_6}$
	$i_{a\_OS} > 0$	N/A			
$0 < V_{bemfa} < \frac{V_{DC}}{3}$	$i_{a\_OS} < 0$	$\overrightarrow{v_7}$			
	$i_{a\_OS} > 0$	N/A			
		II	III	IV	V
$\frac{-V_{DC}}{3} < V_{bemfa} < 0$	$i_{a\_OS} < 0$	N/A			
	$i_{a\_OS} > 0$	$\overrightarrow{v_0}$			
$V_{bemfa} < \frac{-V_{DC}}{3}$	$i_{a\_OS} < 0$	N/A			
	$i_{a\_OS} > 0$	$\overrightarrow{v_0}, \overrightarrow{v_2}, \overrightarrow{v_6}$	$\overrightarrow{v_0}, \overrightarrow{v_2}$	$\overrightarrow{v_0}, \overrightarrow{v_1}$	$\overrightarrow{v_0}, \overrightarrow{v_1}, \overrightarrow{v_5}$

Like the post-fault conduction of phase A, the conduction of the diodes in phases B and C is determined by their back-EMFs V_{bemfb} and V_{bemfc}. According to the voltage equilibrium equations, $V_{bemfb} = -\Psi_f \omega_e \sin(\theta_e - 2\pi/3)$ and $V_{bemfc} = -\Psi_f \omega_e \sin(\theta_e - 4\pi/3)$. Furthermore, $V_{bemfb} > 0$ when $\theta_e \in (-\pi/3, 2\pi/3)$, and $V_{bemfc} > 0$ when $\theta_e \in (\pi/3, 4\pi/3)$. The relationships between the inverter switching states and V_{bemfb} and V_{bemfc} are depicted in Fig. 4-5.

Leveraging the same analysis as for the activating switching states of phase A and incorporating the relationships in Fig. 4-5, the activating switching states of phases B and C can be concluded as follows：

For D3 and D4 in phase B: when $|V_{bemfb}| < V_{DC}/3$, D3 and D4 can be conducted by $\overrightarrow{v_7}$ and $\overrightarrow{v_0}$, respectively; when $|V_{bemfb}| > V_{DC}/3$, D3 and D4 can also be conducted by $\overrightarrow{v_3}$, $\overrightarrow{v_6}$, $\overrightarrow{v_1}$ and $\overrightarrow{v_4}$.

For D5 and D6 in phase C, when $|V_{bemfc}| < V_{DC}/3$, D5 and D6 can be conducted by $\overrightarrow{v_7}$ and $\overrightarrow{v_0}$, respectively; when $|V_{bemfc}| > V_{DC}/3$, D5 and D6 can also be conducted by $\overrightarrow{v_2}$, $\overrightarrow{v_4}$, $\overrightarrow{v_5}$ and $\overrightarrow{v_3}$.

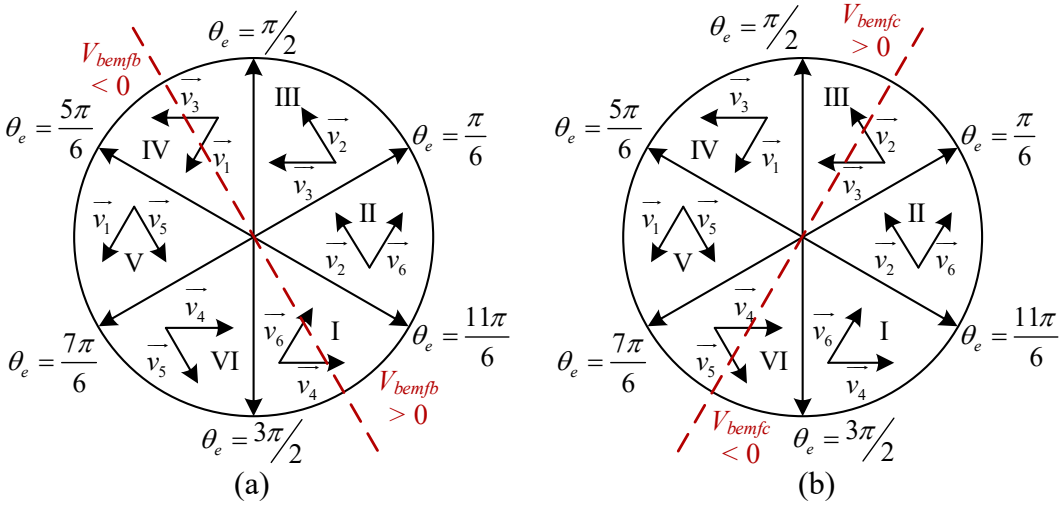


Fig. 4-5. Relationships between voltage vectors and (a) V_{bemfb}; (b) V_{bemfc}.

4.3.3 Conduction Time of the Post-fault Current

In the last subsection, it has been shown that i_{a_OS} conducts only in its activating switching states. Based on the analyzed activating switching states, the conduction time of i_{a_OS} in each switching period can be calculated, which will facilitate the estimation of i_{a_OS}.

TABLE 4-4 Conduction Time of Post-fault Current under the OS Fault

	$0 < V_{bemfa} < \frac{V_{DC}}{3}$	$\frac{1}{3}V_{DC} < V_{bemfa}$			
Sector	V, VI, I, II	V	VI	I	II
Δt	T_{v7}-T_d	T_{v7}-T_d+ T_{v1}+T_{v5}	T_{v7}-T_d +T_{v5}	T_{v7}-T_d +T_{v6}	T_{v7}-T_d + T_{v6}+T_{v2}
	$0 > V_{bemfa} > \frac{-V_{DC}}{3}$	$-\frac{1}{3}V_{DC} > V_{bemfa}$			
Sector	II, III, IV, V	II	III	IV	V
Δt	T_{v0}+T_d	T_{v0}+T_d+ T_{v2}+T_{v6}	T_{v0}+T_d +T_{v2}	T_{v0}+T_d +T_{v1}	T_{v0}+T_d+ T_{v1}+T_{v5}

Besides of the acting time of the activating switching states, although the reverse recovery time is a critical characteristic of the inverter and affects the conduction of the diode, it does not contribute to the amplitude of i_{a_OS}. Furthermore, fast recovery diodes are utilized in IGBT modules. The reverse recovery time is shorter than the duration of the current sampling and cannot be sampled by the motor drive. Hence, the reverse recovery time is not considered in the conduction time of i_{a_OS}.

Taking the dead time T_d of the power switches into account, the conduction time of i_{a_OS} can be summarized in Table 4-4, where Δt is the conduction time of i_{a_OS} in each switching cycle, and T_{vx} is the acting time of voltage vector $\overrightarrow{v_x}$.

In a digital controller, T_{vx} can be obtained from the calculating flow of the SVPWM which can be described in Fig. 4-6, where T_{CM1}, T_{CM2}, and T_{CM3} are three-phase modulation signals, and T_x and T_y are the acting times of the voltage vectors in each spatial sector.

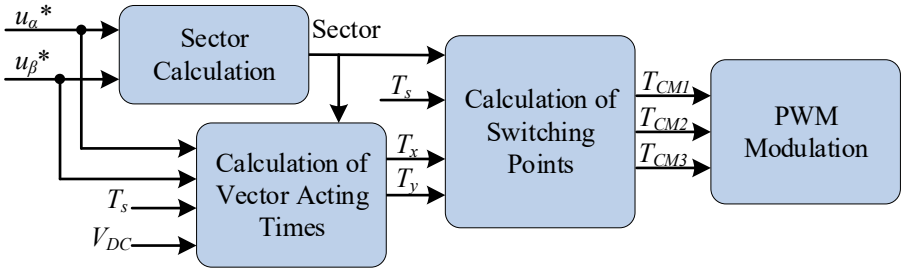


Fig. 4-6. Calculation flow of SVPWM in digital controllers.

T_x is the acting time of the voltage vector that is being first implemented in each sector, while T_y is the acting time of the latter voltage vector. For instance, in Sector II, T_x is the acting time of $\overrightarrow{v_2}$, while T_y is the acting time of $\overrightarrow{v_6}$. Furthermore, the acting time of $\overrightarrow{v_0}$ or $\overrightarrow{v_7}$ can be calculated by $(T_s - T_x - T_y)/2$. Therefore, based on T_x and T_y from the SVPWM process, the conduction time in Table 4-4 can be calculated in every switching cycle.

Although the theoretical analysis of the voltage vector-based method seems to be cumbersome, it provides convenience in practice because the acting time of voltage vectors can be acquired without any other calculation process in the control chip. It should be noted that the conduction time can also be obtained in other control methods adopting the PWM principle. Although the occurrence of the activating switching states and their acting time can be conveniently determined according to the sectors in FOC, they can also be obtained according to the duty ratio of each phase. Once the duty ratios are calculated by the controller,

the switching states that are going to be implemented are determined. Denoting the minimum, medium, and maximum duty ratios as DR_{min}, DR_{med}, and DR_{max}, the acting time of $\overrightarrow{v_0}$ and $\overrightarrow{v_7}$ can be calculated as (1- DR_{max})*T_s and DR_{min}*T_s. The acting time of the other switching states can also be obtained by the duty ratios. Taking the switching state '101' ($\overrightarrow{v_5}$ in SVPWM) as an example, its acting time can be calculated as (DR_{med} - DR_{min})*T_s.

4.4 Estimation Model of the Post-fault Current under the Open-Switch Fault

4.4.1 Equivalent Circuits during the Conduction of Post-fault Current

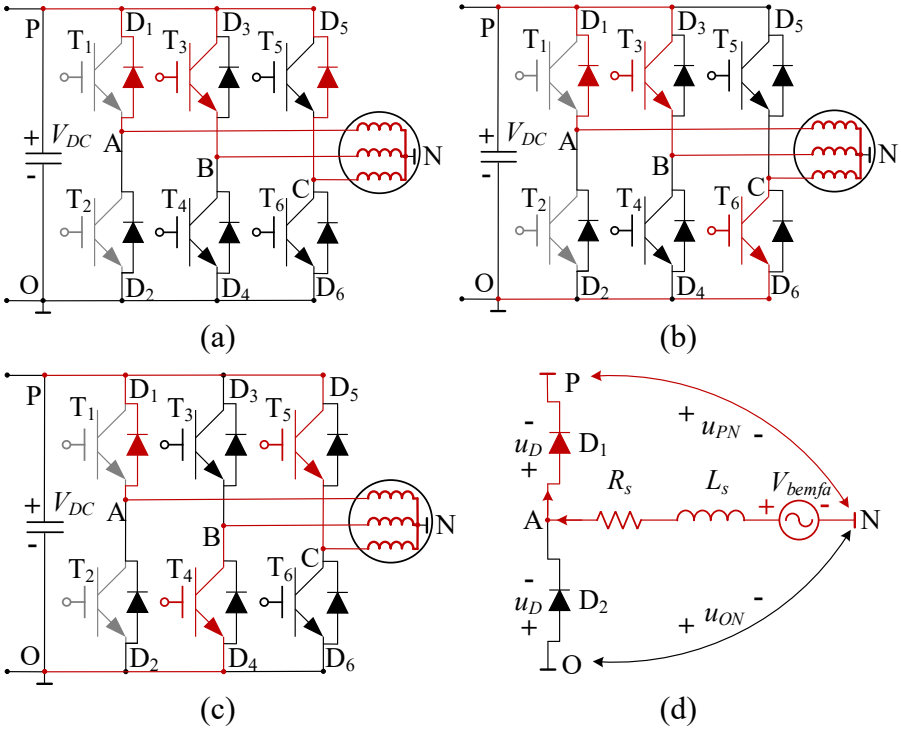


Fig. 4-7. Connecting states of D_1 conduction when applying (a) $\overrightarrow{v_7}$, (b) $\overrightarrow{v_6}$ or $\overrightarrow{v_2}$, (c) $\overrightarrow{v_5}$ or $\overrightarrow{v_1}$, and equivalent circuit of D_1 conduction (d).

After discussing the conduction conditions and conduction time of the post-fault current, its dynamic model can be established for two purposes: a) the post-fault current can be estimated by the model to validate the correctness of the analysis; b) the estimated value can be employed for further utilization such as diagnosing the OS fault and estimating the rotor position.

When D_1 is conducting, the connecting states and equivalent circuit of the faulty phase can be depicted in Fig. 4-7. Defining the current that flows to the winding as positive, according to Fig. 4-7 (d), the following equations can be obtained according to Kirchhoff's voltage law:

$$-V_{bemfa} - L_s \frac{di_{a\_OS}}{dt} - R_s i_{a\_OS} + u_{PN} = 0 \tag{4-17}$$

Although i_{b_OS} is not strictly equal to $-i_{c\_OS}$ when the post-fault i_{a_OS} is conducting, the voltages induced by the mutual inductances can be considered mutually canceled, and are negligible as a part of the voltage source compared with V_{bemfa}. Another reason for neglecting the mutual inductance in modelling the post-fault current is to avoid errors from the sampling process of i_{b_OS} and i_{c_OS}.

When D_2 is conducting, the connecting states and equivalent circuits are shown in Fig. 4-8. Similarly, the situation when D_2 is conducted can be described by Eq. (4-18), where $|V_{bemfa}| = -V_{bemfa}$ holds since $V_{bemfa} < 0$.

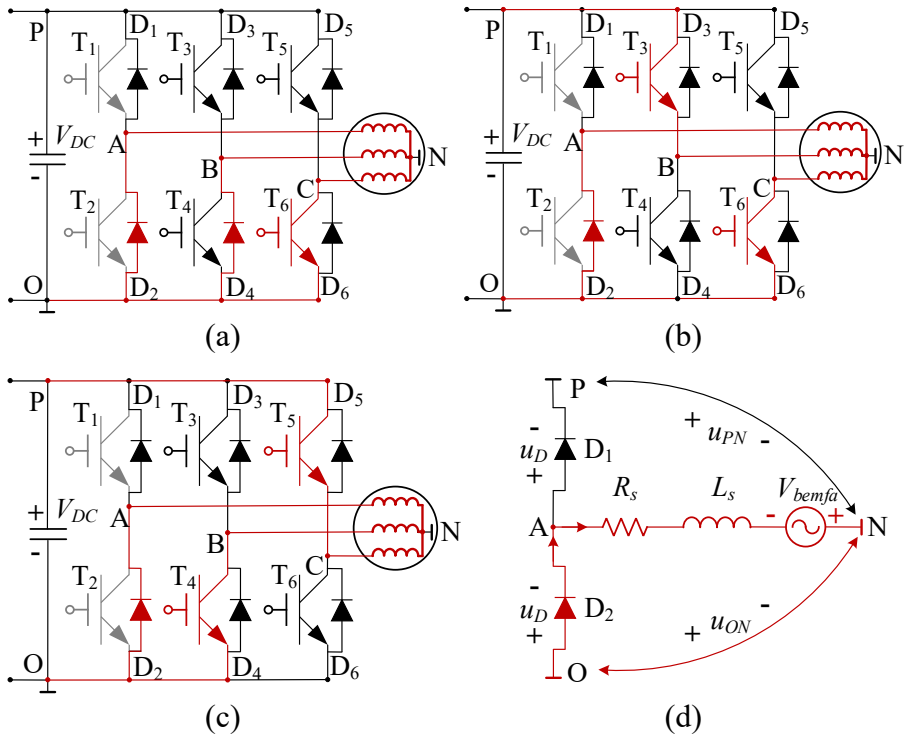


Fig. 4-8. Connecting states of D_2 conduction when applying (a) $\overrightarrow{u_0}$, (b) $\overrightarrow{u_6}$ or $\overrightarrow{u_2}$, (c) $\overrightarrow{u_5}$ or $\overrightarrow{u_1}$, and equivalent circuit of D_2 conduction (d).

$$-\left|V_{bemfa}\right| - u_{ON} + R_s i_{a\_OS} + L_s \frac{di_{a\_OS}}{dt} = 0 \tag{4-18}$$

4.4.2 Dynamic Model and Estimation Model of the Post-fault Current

When the negative i_{a_OS} is activated by $\overrightarrow{v_7}$, u_{PN} is equivalent to its healthy state when applying $\overrightarrow{v_7}$, where $u_{PN} = 0$. When the negative i_{a_OS} is activated by $\overrightarrow{v_1}$, $\overrightarrow{v_5}$, $\overrightarrow{v_2}$ or $\overrightarrow{v_6}$, the OS phase and one of the healthy phases are connected to the positive DC rail, while the other healthy phase is connected to the negative DC rail. In this case, $u_{PN} = V_{DC}/3$. The voltage drops across R_s and u_D are negligible compared with V_{bemfa} and u_{PN}. By incorporating the u_{PN} values into Eq. (4-17), the dynamic model of the negative i_{a_OS} is obtained in Eq. (4-19):

$$-L_s\frac{di_{a\_OS}}{dt} = V_{bemfa} - u_{PN} = \begin{cases} V_{bemfa},\ 0 < V_{bemfa} < \dfrac{V_{DC}}{3},\ \vec{v}_7 \\ V_{bemfa},\ \dfrac{V_{DC}}{3} < V_{bemfa},\ \vec{v}_7 \\ V_{bemfa} - \dfrac{V_{DC}}{3},\ \dfrac{V_{DC}}{3} < V_{bemfa},\ \vec{v}_1, \vec{v}_2, \vec{v}_5, \vec{v}_6 \end{cases} \tag{4-19}$$

$$L_s\frac{di_{a\_OS}}{dt} = -V_{bemfa} + u_{ON} = \begin{cases} -V_{bemfa},\ 0 > V_{bemfa} > \dfrac{-V_{DC}}{3},\ \overrightarrow{v_0} \\ -V_{bemfa},\ \dfrac{-V_{DC}}{3} > V_{bemfa},\ \overrightarrow{v_0} \\ -V_{bemfa} - \dfrac{V_{DC}}{3}, \dfrac{-V_{DC}}{3} > V_{bemfa}, \overrightarrow{v_1}, \overrightarrow{v_2}, \overrightarrow{v_5}, \overrightarrow{v_6} \end{cases} \tag{4-20}$$

$$\hat{i}_{a\_OS} = \Delta i_{a\_OS} = \begin{cases} \dfrac{-(V_{bemfa} - \frac{V_{DC}}{3}) * (\Delta t - T_{v7\_d}) - V_{bemfa} * T_{v7\_d}}{L_s}, \dfrac{V_{DC}}{3} < V_{bemfa} \\ \dfrac{-V_{bemfa} * T_{v7\_d}}{L_s},\ 0 < V_{bemfa} < \dfrac{V_{DC}}{3} \\ \dfrac{-V_{bemfa} * T_{v0\_d}}{L_s},\ 0 > V_{bemfa} > \dfrac{-V_{DC}}{3} \\ \dfrac{(-V_{bemfa} - \frac{V_{DC}}{3}) * (\Delta t - T_{v0\_d}) - V_{bemfa} * T_{v0\_d}}{L_s}, -\dfrac{V_{DC}}{3} > V_{bemfa} \end{cases} \tag{4-21}$$

Similarly, u_{ON} is equal to 0 when applying $\overrightarrow{v_0}$, while u_{ON} is equal to $-V_{DC}/3$ when applying $\overrightarrow{v_1}$, $\overrightarrow{v_5}$, $\overrightarrow{v_2}$ or $\overrightarrow{v_6}$. By incorporating the values of u_{ON} into Eq. (4-18), the positive i_{a_OS} can be modelled as shown in Eq. (4-20):

By discretizing Eq. (4-19) and Eq. (4-20) and incorporating Δt from Table 4-4, the increment of i_{a_OS}, viz. Δi_{a_OS}, generated in each switching period, can be calculated using Eq. (4-21), where $\hat{i}_{a\_OS}$ is the estimated amplitude of i_{a_OS}, $T_{v7\_d} = T_{v7} - T_d$ and $T_{v0\_d} = T_{v0} + T_d$. As i_{a_OS} can only be activated during its activating switching states, the estimated amplitude of i_{a_OS} is equal to Δi_{a_OS}. In Eq. (4-21), the phase A back-EMF is estimated based on the first equation of Eq. (3-3) and has been validated in the experiment presented in Fig. (3-4).

4.5 Experimental Validation

The experimental validation of the current dynamics in each switching period and real-time estimation of the post-fault current are conducted on the same setups in Section 3.4. The Trip-Zone module of the DSP is utilized to control the PWM signals separately and emulate the OS fault. The same IGBT module (*FUJI* 7MBR25VA120-50) works at 10 kHz and is supplied by 200 V DC bus voltage.

4.5.1 Validation of Relationships between Switching States and Back-EMF

Before validating the analyzed post-fault current dynamics and the proposed current estimation model under the OS fault, the analysis of the relationships between θ_e and the spatial sector in Table 4-2 are validated in the first place, as the relationships are fundamental to identify the activating switching states at each polarity of V_{bemfa}.

Fig. 4-9 depicts the practical relationships between θ_e, V_{bemfa}, and the number of spatial sectors when the motor drive is healthy (Fig. 4-9 (a)) and when the motor drive is under the OS fault (Fig. 4-9 (b)). In Fig. 4-9, the PMSM with 4 pole pairs is operating at 500 rpm, resulting in a fundamental period of 30 ms.

In Fig. 4-9 (a), when $\theta_e \in (\pi, 2\pi)$, the number of sectors can be 5, 6, 1, or 2, and V_{bemfa} is positive. In contrast, when $\theta_e \in (0, \pi)$, the sector number can be 2, 3, 4, or 5, and V_{bemfa} is negative. Moreover, each sector number corresponds to a range of θ_e of approximately $\pi/3$. The experimental results validate the correctness of Fig. 4-4 (b) and the analysis in subsection

4.3.1. In Fig. 4-9 (b), which presents a motor drive under the OS fault, changes in the phase A current will cause fluctuations in both i_{d_OS} and i_{q_OS}. However, the values of arctan(u_β*/u_α*) and the sector number still largely correspond to θ_e as depicted in Table 4-2.

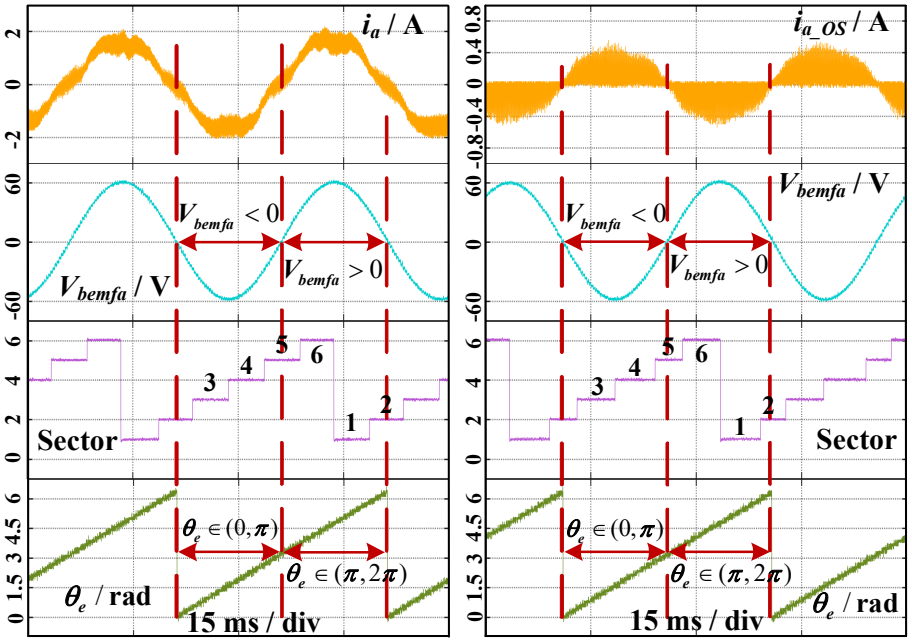


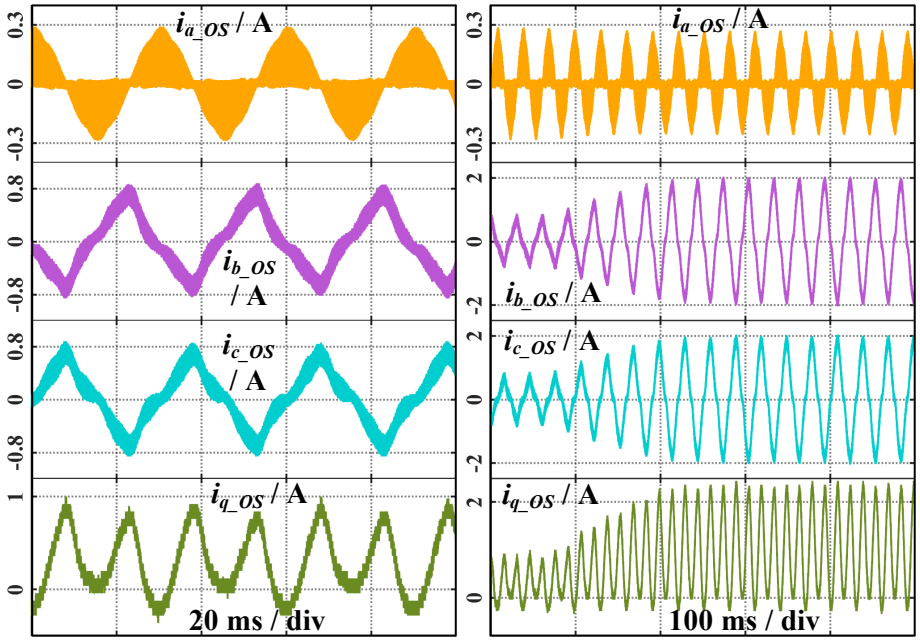
Fig. 4-9. Practical relationships between θ_e, V_{bemfa}, and the number of spatial sectors under (a) healthy state; (b) OS fault.

4.5.2 Validation of Conduction Conditions and the Conduction Time

In Fig. 4-10, the post-fault i_{a_OS} exhibits current pulses in each switching period, which verifies that it is related to the switching state and is discontinuous. Additionally, at the same speed level, the change in load torque does not directly influence the envelope and amplitude of the post-fault i_{a_OS} because its voltage source is $V_{bemfa,}$ which is determined by the rotor speed and does not relate to the load torque. In Fig. 4-10 (b), when the load varies, the amplitude of i_{a_OS} slightly changes due to the slight change in speed posed by the variable torque.

To prove the analysis of the conduction time in Table 4-4, i_{a_OS} and its conduction time are presented in Fig. 4-11, where Δt_{D1} or Δt_{D2} stands for the conduction time of i_{a_OS} conducting through D_1 or D_2. In Figs. 4-11 (a) and (b), the motor operates at 500 rpm, where the peak value of V_{bemfa} (approximately 30 V) is lower than that of V_{DC}/3 (approximately 66.6 V). As analyzed in subsection 4.4.3 and summarized in Table 4-4, when $|V_{bemfa}| < V_{DC}/3$, D_1 is

conducted only when $\overrightarrow{v_7}$ is being applied, and $\overrightarrow{v_0}$ conducts D_2. The ratio of the conduction time accounts for 35% of the entire switching cycle and relatively slowly changes in each cycle because the flux vector at low speed can stay in each sector for a relatively long time.



(a) (b)

Fig. 4-10. Post-fault current responses at 500 rpm under (a) no load; (b) variable load torque.

Comparatively, at the high speed in Figs. 4-11 (c) and (d), the conduction time has noticeable changes in each cycle because the duty ratios of the driving signals rapidly change. Unlike the behaviors at 500 rpm, when the speed is lifted to 1500 rpm, where V_{bemfa} (approximately 92 V amplitude) can be higher than $V_{DC}/3$, D_1 and D_2 are conducted in $\overrightarrow{v_7}$, $\overrightarrow{v_0}$ and other vectors that separately connect phases B and C to the positive and negative rails, corresponding to the activating switching states in Table 4-4. Additionally, as described in Eq. 4-21, i_{a_OS} has a higher changing rate in the zero vectors than other vectors because of different values of the voltage source.

In addition, i_{a_OS} maintains its conduction for a short period after removing its activation switching state at both speed levels. For example, in Fig. 4-11 (c), i_{a_OS} converges to zero while maintaining conduction after removing $\overrightarrow{v_6}$. In this case, the connecting state is equivalent to Fig. 4-3 (b), where the negative i_{a_OS} cannot be activated. This non-activated conduction is caused by the free-wheeling effect due to the winding inductance. During this period, the faulty phase is still conducting, and the effect of the voltage vector is equivalent to

the pre-fault state.

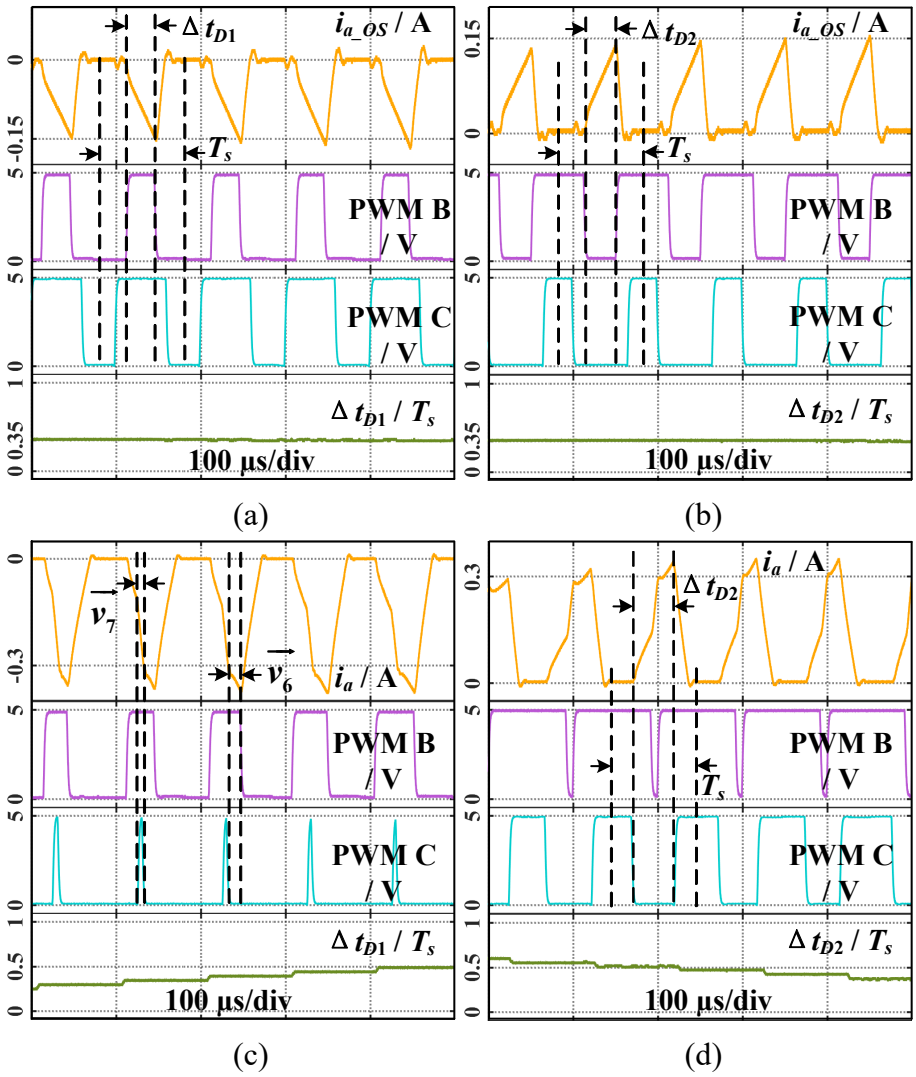
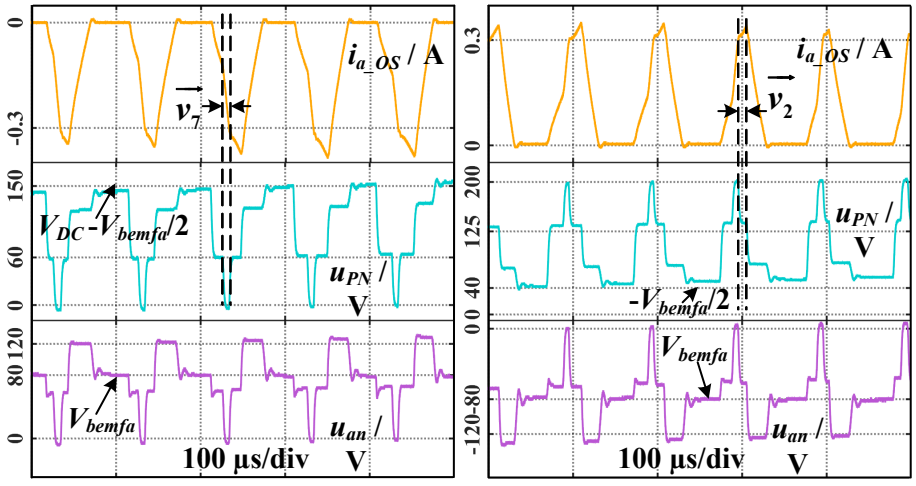


Fig. 4-11. Post-fault i_{a_OS}, PWM B&C, and conduction time in each switching cycle at (a)&(b) 500 rpm and (c)&(d) 1500 rpm when (a)&(c) $V_{bemfa} > 0$ and (b)&(d) $V_{bemfa} < 0$.

The states of u_{PN} and u_{an} at 1500 rpm are shown in Fig. 4-12. In Fig. 4-12 (a), as shown in Fig. 4-11 (c), $\vec{v_4}$ and $\vec{v_0}$ are applied when i_{a_OS} is not conducting, which corresponds to the connecting state in Fig. 4-3 (b). In this case, $u_{an} = V_{bemfa}$ (approximately 92 V amplitude) and $u_{PN} = V_{DC} - V_{bemfa}/2$, which validates the analysis in Eq. (4-4). Similarly, in Fig. 4-12 (b), the connecting state when i_{a_OS} is not conducting corresponds to Fig. 4-3 (a), where V_{PN} is equal to $-V_{bemfa}/2$.

When i_{a_OS} is conducting, the connecting states are equivalent to the states under healthy conditions. For example, when the positive i_{a_OS} is conducted by $\vec{v_2}$, as shown in Fig. 4-12 (b), phase A is connected to the negative rail through D_2, and the connecting state is

equivalent to the state of applying $\overrightarrow{v_2}$ under the healthy condition where $u_{PN} = u_{bn} = 2V_{DC}/3$ and $u_{an} = -V_{DC}/3$. Furthermore, when $\overrightarrow{v_7}$ is conducting the negative i_{a_OS} through D_1, as shown in Fig. 4-12 (a), the connecting state is identical to applying $\overrightarrow{v_7}$ under the healthy condition where $u_{PN} = 0$. However, unlike the healthy condition, i_{a_OS} is activated by $V_{bemfa} - u_{PN}$, instead of V_{DC} under the healthy condition. Therefore, although the voltages at terminal A and neutral point N have been clamped to the same level when i_{a_OS} is conducting, the voltage source in phase still exists to activate the post-fault i_{a_OS}, as described in Fig. 4-7 (d) and Fig. 4-8 (d).



(a) (b)

Fig. 4-12. Post-fault i_a, u_{PN}, and u_{an} in each switching cycle at 1500 rpm when (a) $V_{bemfa} > 0$; (b) $V_{bemfa} < 0$.

4.5.3 Validation of the Estimation Model of Post-fault Current

Based on the estimation model proposed in Eq. (4-21), the post-fault i_{a_OS} can be calculated by the controller in real time, denoted as i_{a_cal}, and compared with the measured current i_{a_meas}, as shown in Fig. 4-13. In Figs. 4-13 (b) and (c), although i_{q_OS} severely fluctuates at both speed levels, the OS fault does not affect the speed, and V_{bemfa} maintains the sinusoidal pattern. The OS fault affects the speed by changing the voltage vectors, and the severity of the effect is influenced by the rotor inertia, speed level, and load torque. In summary, the speed is prone to be slightly affected by the fault when the motor is operating at high speed, with light load torque and large inertia. In terms of the high speed, the time when the flux is controlled by the influenced voltage vectors is shortened, and the speed cannot respond to the rapidly changing i_{q_OS} because the mechanical time constant is much larger than the electrical

time constant.

Different from the constant motor speed in Figs. 4-13 (b) and (c), the motor speed in Fig. 4-13 (a) severely fluctuates when the speed command is 5% (90 rpm) of its rated speed. The reason lies in that, at low speeds, the motor operates for an extended period of time within the phase range affected by the fault. As a result, the time of i_{q_OS} fluctuation is longer than that of high speeds and it allows the mechanical shaft to respond to the i_{q_OS} fluctuation.

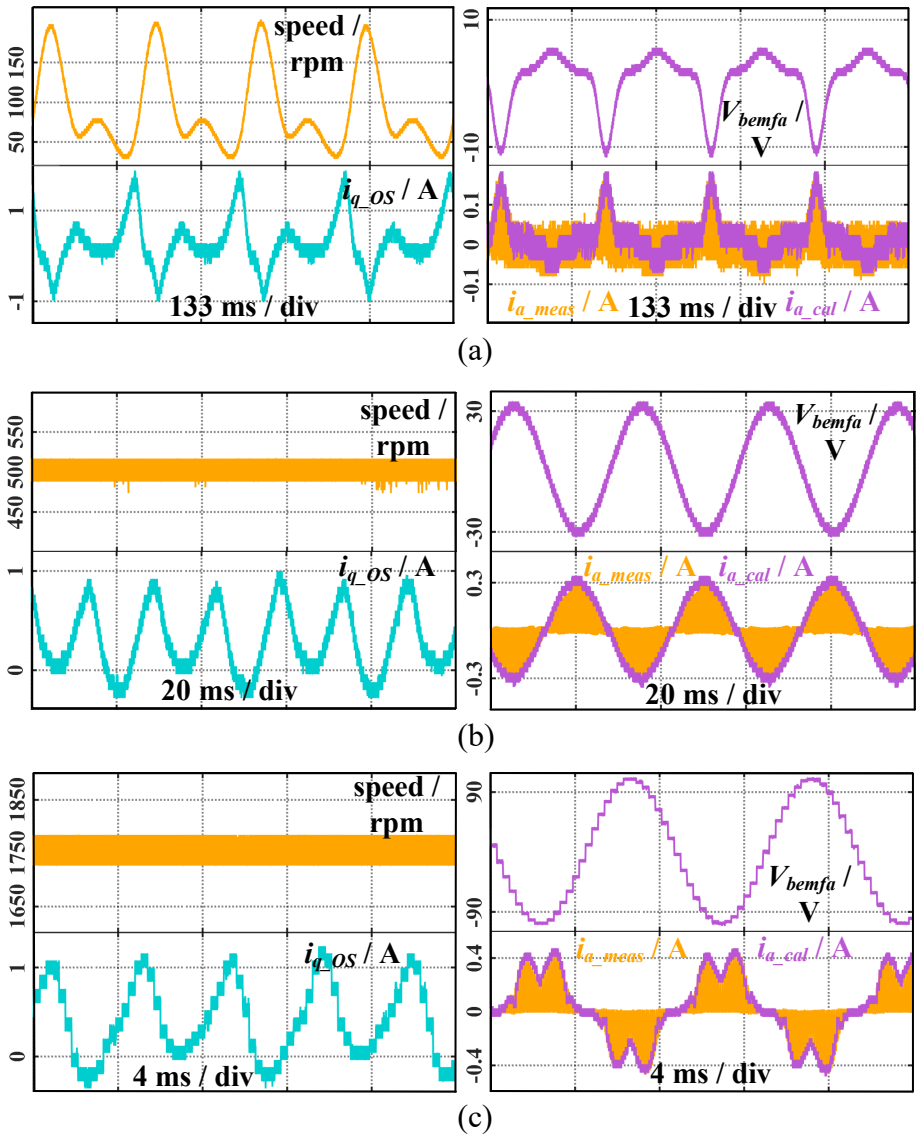


Fig. 4-13. Post-fault speed, V_{bemfa}, i_{a_cal}, i_{a_meas} at (a) 90 rpm; (b) 500 rpm; (c) 1800 rpm.

In Fig. 4-13 (b), V_{bemfa} is less than $V_{DC}/3$ and acts as the only excitation source of the open-circuit current, and both i_{a_meas} and i_{a_cal} follows the sinusoidal pattern of V_{bemfa}. In Fig. 4-13 (a), where V_{bemfa} is also less than $V_{DC}/3$, although the amplitude of V_{bemfa} is small, i_{a_meas} still follows the pattern of V_{bemfa} in reverse because it shares the same activation mechanism with

the OS current in Fig. 4-13 (b). However, when the motor is operating at the nominal speed, the post-fault i_{a_OS} does not follow the pattern of V_{bemfa} and has a sag when V_{bemfa} is around its peak value. The reason for the current sag is explained as follows: when V_{bemfa} is around its peak where θ_e is approximately $\pi/2$ or $3\pi/2$, the controlled flux is on the boundary of sectors III and IV or sectors VI and I, as shown in Fig. 4-4 (b). On the boundaries, $\overrightarrow{v_3}$ or $\overrightarrow{v_4}$ are the dominant active vectors that account for most of the acting time in each switching cycle, and they cannot activate the post-fault i_{a_OS}. Meanwhile, the acting time of zero vectors accounts for a small portion of the switching period at high speeds, as shown in Figs. 4-11 (c) and (d). Therefore, when V_{bemfa} is around its peak values at high speeds, the amplitude of the post-fault i_{a_OS} decreases because its conduction is squeezed by $\overrightarrow{v_3}$ or $\overrightarrow{v_4}$.

At different speeds and V_{bemfa} levels, i_{a_cal} and i_{a_meas} are compared in the last scopes of Figs. 4-13 (a), (b) and (c). Because the voltage source and conduction time are comprehensively considered in Eq. (4-21), the calculated value matches the pattern and amplitude of the measured value on the scale of milliamperes in real time, which validates the effectiveness of the proposed model. In addition, it should be noted that the digital controller only executes the embedded codes once per switching cycle. As a result, the calculated current is updated only once per switching cycle, rather than following the discontinuous switching states within each cycle. Therefore, the calculation result presents the continuous envelope of the open-switch current, rather than the current pulses within each switching cycle.

4.5.4 Tests and Analysis of Single Open-Switch Fault

The feasibility of the proposed model is also tested for the other types of faults, including T_1 single OS fault, and T_1&T_4 multi-phase OS fault.

Regarding the T_1 single OS fault, the activation mechanism of the post-fault i_{a_OS} conducting through D_1 does not change and can be concluded as: when $0 < V_{bemfa} < V_{DC}/3$, D_1 can be conducted by $\overrightarrow{v_7}$ which connects both phase B and phase C to the positive DC rail; when $V_{bemfa} > V_{DC}/3$, D_1 can also be conducted by $\overrightarrow{v_1}$, $\overrightarrow{v_2}$, $\overrightarrow{v_5}$, and $\overrightarrow{v_6}$ which connect phase B and phase C to the positive and negative DC rails separately.

Different from the fault with two faulty switches in the same phase, because of the still-functional T_2, the OS i_{a_OS} can also conduct through T_2 by $\overrightarrow{v_0}$ when $V_{bemfa} > 0$, as shown in Figs. 4-14 (a) and (b). However, the extra current path does not affect the amplitude of the

OS current. When the current is activated by $\overrightarrow{v_0}$, it has the identical activation source V_{bemfa} as the OS current activated by $\overrightarrow{v_7}$. On the other hand, the acting time $\overrightarrow{v_0}$ is the same as that of $\overrightarrow{v_7}$ in symmetric PWM control. Therefore, the proposed model is also applicable to the single OS fault. The validation of the case of single OS fault is presented in Figs. 4-14 (c) and (d), in which i_{a_cal} still matches the amplitude of i_{a_meas} in the faulty half.

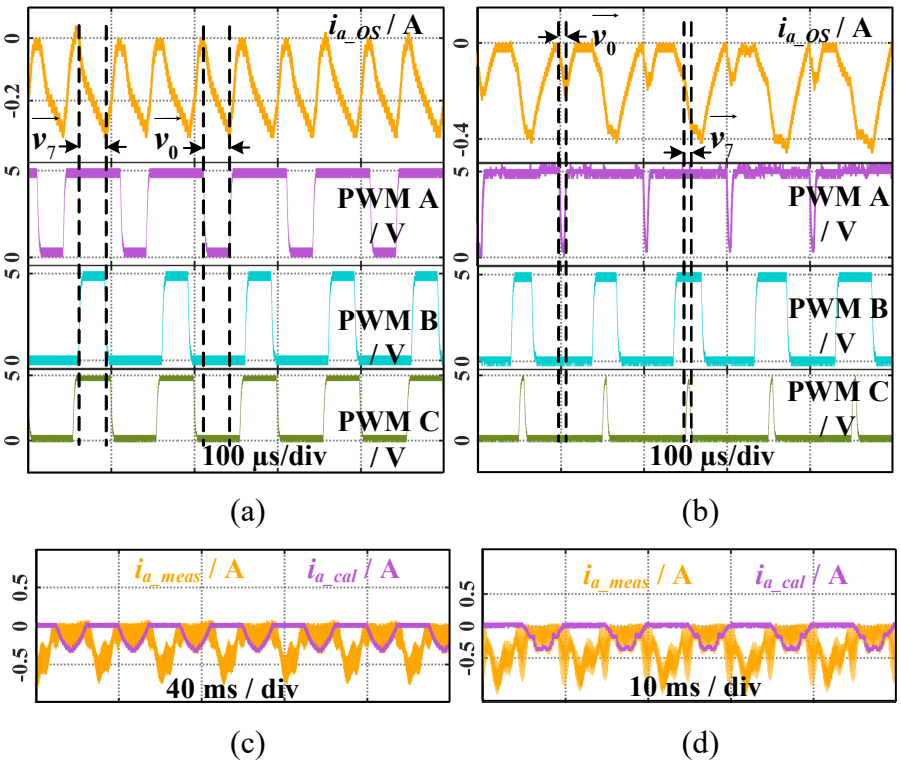


Fig. 4-14. T_1 single OS i_{a_os} and PWM signals in each switching cycle at (a) 500 rpm and (b) 1500 rpm; Comparison of i_{a_meas} and i_{a_cal} at (c) 500 rpm and (d) 1500 rpm.

4.5.5 Tests and Analysis of Faults in Different Phases

Take the fault in which T_1 and T_4 are disabled as an example. The faulty T_1 affects the phase A current when $V_{bemfa} > 0$, while the faulty T_4 affects the phase B current when $V_{bemfb} < 0$. The OS i_{a_os} and i_{b_os} have an overlapping area as depicted in Figs. 4-15 (a) and (b), while they have independent mechanisms in the rest of their faulty phase ranges.

In the overlapping area depicted in Fig. 4-15 (a), when the amplitudes of V_{bemfa} and V_{bemfb} are less than $V_{DC}/3$, the proposed model is still effective for each phase and the faulty current of each phase is the same as the single OS current of each phase. As analyzed in the case of the single OS fault, both the $\overrightarrow{v_7}$ and $\overrightarrow{v_0}$ can conduct the same amplitude i_{a_os} through D_1 or T_2. It also applies to i_{b_os}. When $\overrightarrow{v_7}$ is being applied, i_{a_os} is conducting through D_1 while i_{b_os} can

conduct through the remaining healthy T_3. Similarly, when $\overrightarrow{v_0}$ is being applied, i_{b_OS} conducts through D_4 while i_{a_OS} conducts through the healthy T_2, as shown in Fig. 4-15 (c). Therefore, the overlapping area does not affect the calculation result of the proposed model when the amplitudes of V_{bemfa} and V_{bemfb} are less than $V_{DC}/3$, as validated in Fig. 4-13 (e). In the non-overlapping area in Fig. 4-13 (a), one of the faulty phases recovered its current-conduction capability due to the other remaining healthy power switch in the faulty phase and the corresponding phase currents deviate from zero. Meanwhile, the other faulty phase continues to conduct the open-switch current following the rules summarized in Eq. (4-21).

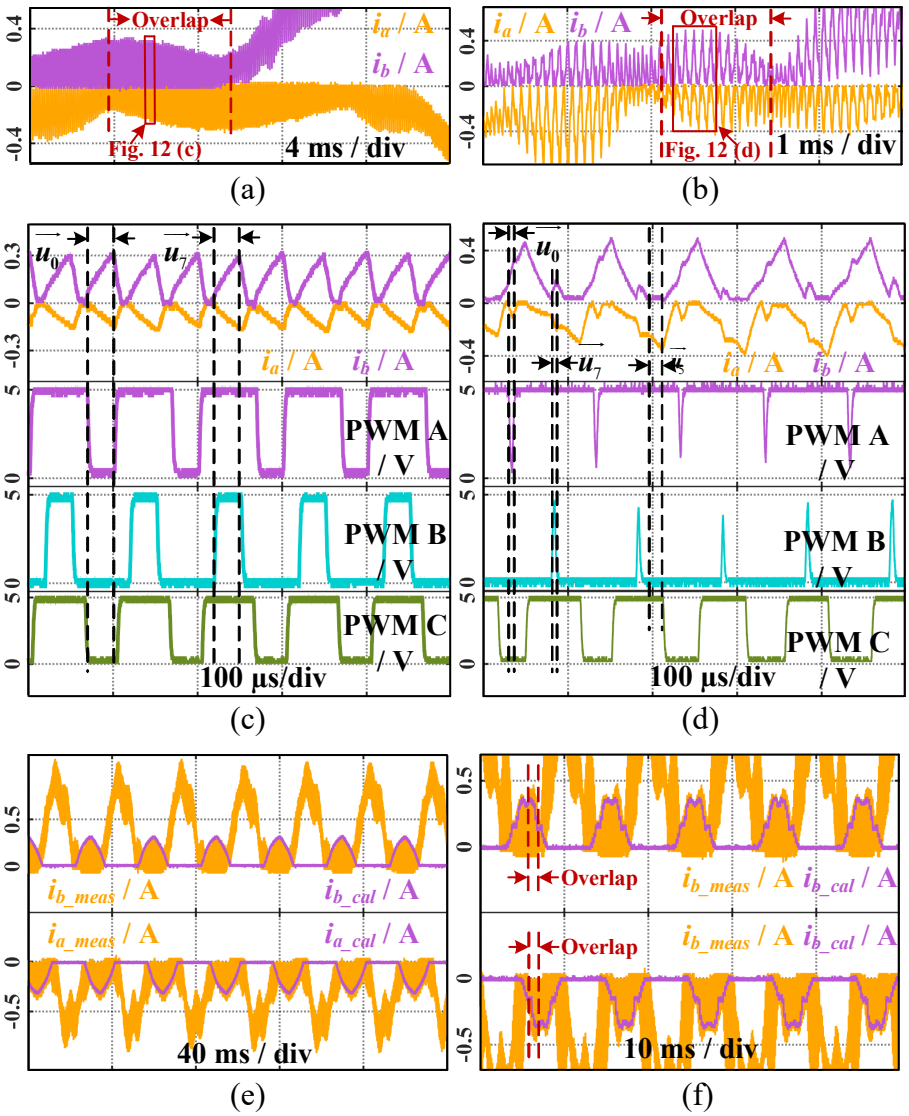


Fig. 4-15. T_1 & T_4 OS currents at (a) 500 rpm and (b) 1500 rpm; Currents and PWM signals at (c) 500 rpm and (d) 1500 rpm; Comparison of measurement and calculation at (e) 500 rpm and (f) 1500 rpm.

Nevertheless, the conduction mechanism becomes more complex when the amplitudes of

V_{bemfa} and V_{bemfb} exceed $V_{DC}/3$, where the non-zero vectors are also involved. In the overlapping area depicted in Fig. 4-15 (b) and when the non-zero vector ($\overrightarrow{v_5}$) is being applied, the phase A and C have been connected to the positive DC rail. In this case, i_{b_OS} cannot conduct through D_4 since $V_{bemfb} > (2V_{DC}/3)$ cannot be achieved as analyzed in subsection 4.2.2 and shown in Fig. 4-15 (d). Therefore, i_{a_OS} can no longer be calculated based on the established excitation source and conduction time, but is related to the value of i_{c_OS}. As a result, when V_{bemfa} and V_{bemfb} exceed $V_{DC}/3$, the calculated open-switch currents do not completely match the measured currents in the overlapping area, whereas the proposed model is still effective in the non-overlapping area, as shown in Fig. 4-15 (f).

Conclusively, the proposed model is still effective under the single OS fault, the non-overlapping area of the multi-phase OS fault, and the overlapping area of the multi-phase fault when the back-EMFs are less than $V_{DC}/3$. Regarding the overlapping area of the multi-phase fault when the back-EMFs exceed $V_{DC}/3$, the conduction mechanism of OS current has changed when the non-zero vectors are being applied, resulting in a mismatch between the calculation and measurement.

4.6 Summary

The unknown mechanism of the post-fault current under OS faults is revealed in this chapter. The post-fault behaviors have been analyzed, and the corresponding equivalent circuits are provided. Moreover, switching patterns that fulfill the conduction condition are determined to confirm the conduction time. Finally, the estimation model of the post-fault current is given.

The analysis and experimental results have validated that the OS fault and OP fault have different post-fault phase voltages and currents. Therefore, before developing the methods to diagnose and tolerate the different faults, the post-fault models and mechanisms need to be established and revealed in the first place.

The diagnosis and fault-tolerant control are the most direct applications of the proposed estimation model of the post-fault current under OS fauls. However, the proposed model also has the potential to be utilized in other scenarios, such as estimating or calibrating the rotor position and flux parameter since it is validated that the post-fault current is directly activated by the back-EMF and is closely related to the electrical angle.

It is noteworthy that the current in the OS phase is studied in the case of IGBT-based PMSM drives. Unlike Si and Silicon Carbide (SiC) devices, Gallium Nitride (GaN) devices do not need anti-parallel diodes for reverse conduction due to their symmetrical structure. Similar to its forward conduction, when the gate-to-drain voltage V_{gd} is greater than the threshold voltage V_{th}, the reverse conduction of the GaN device can be achieved. In terms of the OS fault, the gate-to-source voltage V_{gs} is equal to 0 V because the gate leakage current is negligible [164], and V_{gd} is equal to the source-to-drain voltage V_{sd} because $V_{gd} = V_{gs} + V_{sd} = V_{sd}$. V_{sd} is equal to u_{AP} or u_{OA} in case of discussing the post-fault conduction of the upper half leg or the lower half leg. Therefore, substituting the forward on-voltage of the reverse diode u_D by V_{th}, the conduction conditions analyzed in Section 4.2 can be applied to the post-fault reverse conduction of GaN devices.

Nevertheless, in GaN-based motor drives, both the damaged power switches and disconnections of motor phases will not allow the studied OS current to conduct. In this case, the studied OS current can still be activated when the fault is incurred by missing driving signals and can be employed to distinguish this type of open-circuit fault from others.

Chapter 5 **Distinguishing the Open-Switch Fault and the Open-Phase Fault**

5.1 Introduction

In this chapter, a current sampling method is proposed that enables the motor drive to detect i_{a_OS}. Subsequently, diagnostic rules are designed that can be conveniently implemented based on the sampled and estimated i_{a_OS} to classify the OP fault and the OS fault. In Chapter 4, i_{a_OS} has been accurately modelled to provide its estimated value. The estimated i_{a_OS} needs to be compared with the sampled value to acquire their residuals. The estimated value, sampled value, and their residuals have different relationships corresponding to the healthy condition, OP fault, and OS fault. Based on these different relationships, diagnostic rules can be designed to facilitate the classification.

However, i_{a_OS} cannot be sampled by the regular current sampling method adopted by the current control in PMSM drives, which is also a significant reason for the neglect of i_{a_OS} in previous studies. The regular current sampling method has one fixed sampling point located at the beginning point of each switching period, whereas the maximum amplitude of i_{a_OS} occurs at the ending point of its activating switching states. Therefore, to detect the peak amplitude of i_{a_OS}, another current sampling process needs to be implemented at different points corresponding to different switching states.

In this chapter, a sampling method for detecting i_{a_OS} is designed first. The corresponding sampling point is calculated in each switching period to align with the different activating switching states of i_{a_OS}. Furthermore, the current sampling delay is evaluated to ensure that the extra current sampling process will not affect the regular sampling used for the current control. Moreover, to avoid misdiagnosis caused by sensing and digitalization errors, the current sampling error is quantified according to the employed setups. Finally, following the unique characteristics of the three values at different system conditions, the diagnostic method is proposed, and its performance is evaluated at various speeds.

5.2 Current Sampling of the Post-fault Current under the Open-Switch Fault

5.2.1 Regular Current Sampling in Current Control of PMSM Drives

The regular current sampling point is arranged at the beginning point of each switching period to sample the middle value among the current ripples, as shown in Fig. 5-1. The mid-value sampling is similar to a mid-value filtering process which benefits the current control.

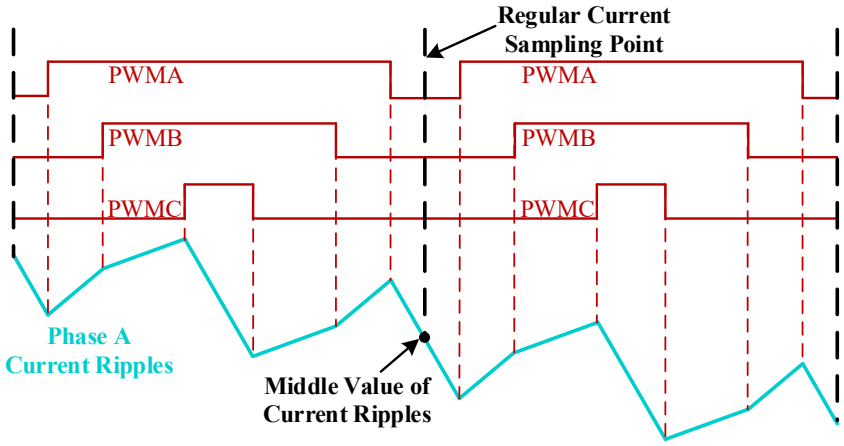


Fig. 5-1. Regular current sampling point and its sample value.

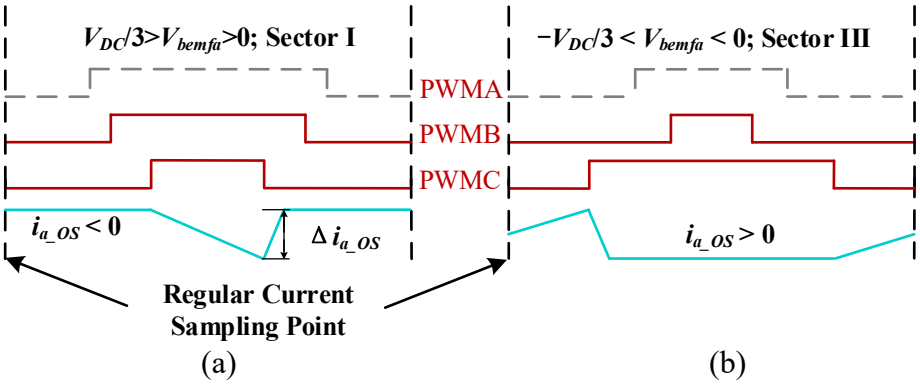


Fig. 5-2. Mismatch between the regular current sampling and (a) the positive i_{a_OS}; (b) the negative i_{a_OS}.

However, the regular current sampling is inadequate for capturing the amplitude and envelop of the post-fault i_{a_OS} because the peak amplitude of i_{a_OS} occurs at the ending point of its activating switching states. For instance, consider the scenario in which i_{a_OS} is activated by $\vec{v_7}$ in Sector I, and $V_{bemfa} < V_{DC}/3$. In this case, the mismatch between the regular sampling point and the occurrence of i_{a_OS} is depicted in Fig. 5-2 (a). The regular sampling point does

not align with the occurrence of i_{a_OS}, resulting in a missing detection of the current waveform.

Similarly, when i_{a_OS} is activated by $\overrightarrow{v_0}$ in Sector III, with $V_{bemfa} > -V_{DC}/3$, the correspondence between the regular sampling point and i_{a_OS} is shown in Fig. 5-2 (b), where the regular sampling point meets the mid-value of i_{a_OS}.

Conclusively, the regular current sampling can only detect half of the positive i_{a_OS} amplitude while completely missing the negative part of i_{a_OS}.

5.2.2 Current Sampling Method Adapting the Occurrence of i_{a_OS}

Based on the activating switching states of i_{a_OS} summarized in Table 4-3, i_{a_OS} can be sampled by aligning the current sampling point to the peak amplitude of i_{a_OS}.

When $|V_{bemfa}| < V_{DC}/3$, i_{a_OS} needs to be sampled at either the ending point of $\overrightarrow{v_7}$ if $V_{bemfa} > 0$, or the ending point of $\overrightarrow{v_0}$ if $V_{bemfa} < 0$, as depicted in Fig. 5-3.

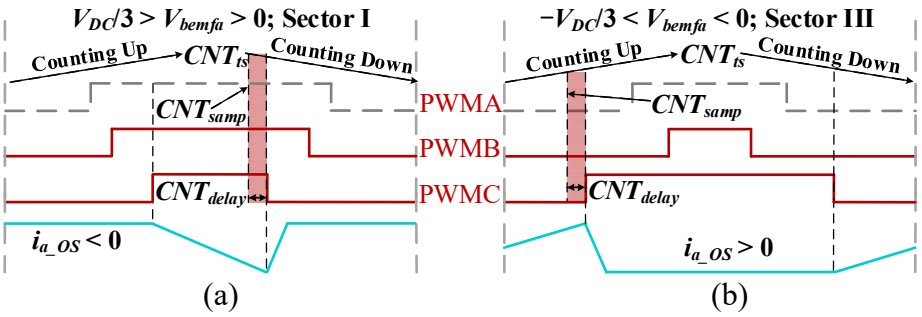


Fig. 5-3. Sampling points of i_{a_OS} when $|V_{bemfa}| < V_{DC}/3$: (a) $V_{bemfa} > 0$ and $i_{a\_OS} < 0$; (b) $V_{bemfa} < 0$ and $i_{a\_OS} > 0$.

The counting values of controller timers are used to describe the sampling points. In Fig. 5-3, CNT_{ts} is the counting value of a switching period. CNT_{samp} is the value where the sampling starts. CNT_{delay} stands for the sampling delay, which does not include the conversion delay of ADC and only accounts for hundreds of nanoseconds.

When $|V_{bemfa}| < V_{DC}/3$, CNT_{samp} can be calculated in Eq. (5-1), where DR_{max} and DR_{min} are the maximum and minimum duty ratios of the three PWM duty ratios, respectively.

$$\begin{cases} CNT_{samp} = CNT_{ts} * DR_{\min} + CNT_{delay}, 0 < V_{bemfa} < \dfrac{V_{DC}}{3} \\ CNT_{samp} = CNT_{ts} * DR_{\max} - CNT_{delay}, \dfrac{-V_{DC}}{3} < V_{bemfa} < 0 \end{cases} \quad (5\text{-}1)$$

If the rotor speed elevates $|V_{bemfa}|$ above $V_{DC}/3$, i_{a_OS} can be activated during zero vectors and some active vectors. When $V_{bemfa} > V_{DC}/3$, based on Table 4-3, i_{a_OS} needs to be sampled at the second ending point of $\overrightarrow{v_1}$, $\overrightarrow{v_5}$, $\overrightarrow{v_6}$, or $\overrightarrow{v_2}$ in Sector V, VI, I, or II respectively. The CNT_{samp} is shown in Fig. 5-4 and can be calculated in Eq. (5-2), where DR_{mid} is the middle value of the three PWM duty ratios.

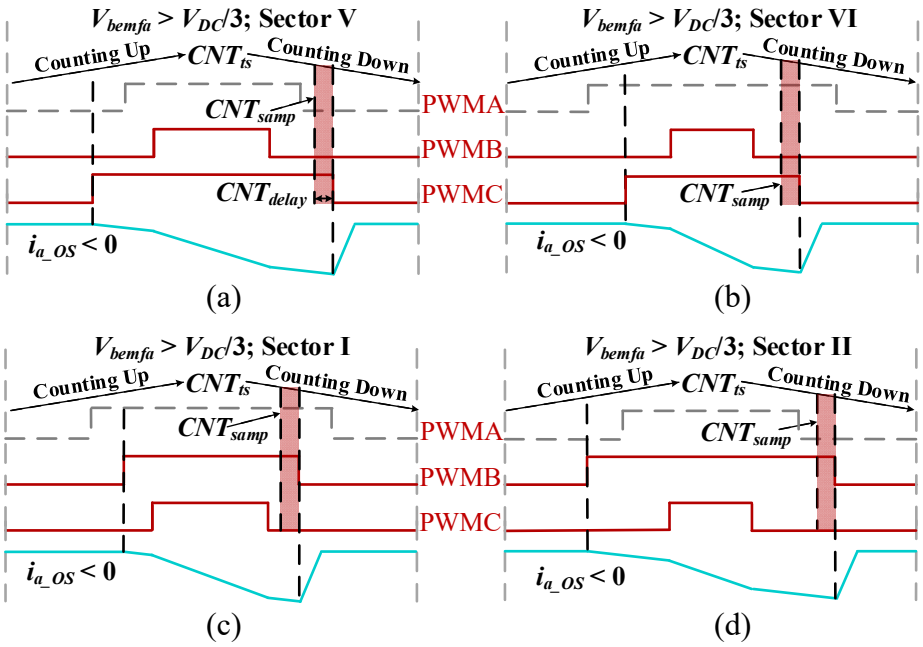


Fig. 5-4. Sampling points of i_{a_OS} when $V_{bemfa} > V_{DC}/3$ in Sector (a) V; (b) VI, (c) I; (d) II.

$$\begin{cases} CNT_{samp} = CNT_{ts} * DR_{\max} + CNT_{delay}, \text{ Sector V\&II} \\ CNT_{samp} = CNT_{ts} * DR_{\text{mid}} + CNT_{delay}, \text{ Sector VI\&I} \end{cases} \quad (5\text{-}2)$$

Similarly, when $V_{bemfa} < -V_{DC}/3$, the sampling point is arranged at the first ending point of $\overrightarrow{v_6}$, $\overrightarrow{v_2}$, $\overrightarrow{v_1}$ or $\overrightarrow{v_5}$ in Sector II, III, IV, or V respectively. CNT_{samp} is shown in Fig. 5-5 and can be calculated in Eq. (5-3):

$$\begin{cases} CNT_{samp} = CNT_{ts} * DR_{\min} - CNT_{delay}, \text{ Sector V\&II} \\ CNT_{samp} = CNT_{ts} * DR_{\text{mid}} - CNT_{delay}, \text{ Sector VI\&I} \end{cases} \quad (5\text{-}3)$$

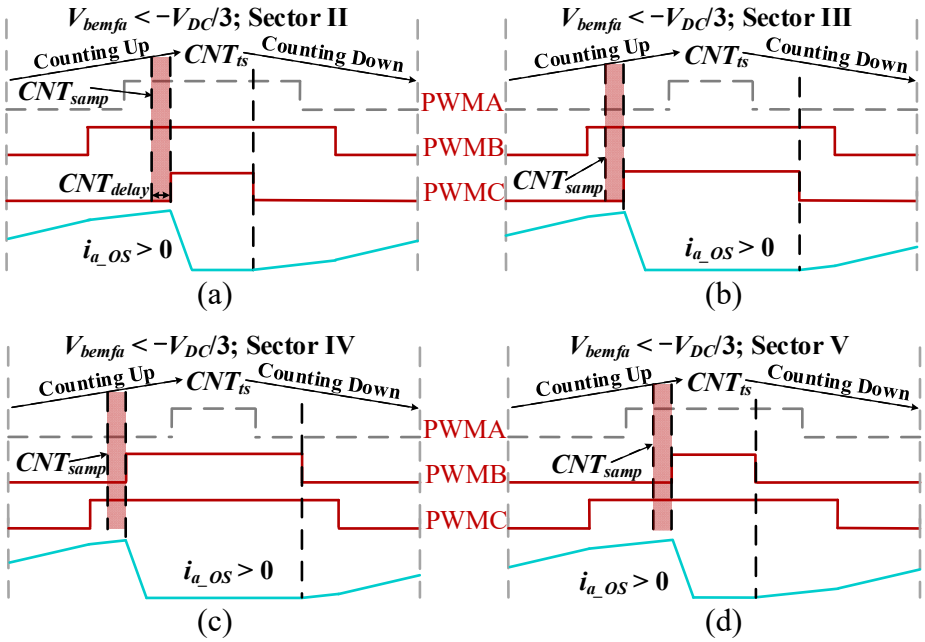


Fig. 5-5. Sampling points when $V_{bemfa} < -V_{DC}/3$ in Sector (a) II; (b) III; (c) VI; (d) V.

Following the designed method, the drive can detect the amplitude of i_{a_OS} intact. The current sampling method remains effective for detecting the phase currents under the healthy condition and the OP fault, viz. i_{a_H} and i_{a_OP}, but the sampled current is not involved in the current control loop. The current sampled by the designed method is denoted as i_{a_samp} to represent the values under different conditions, as shown in Eq. (5-4).

$$i_{a\_samp} = \begin{cases} i_{a\_H}, & \text{Health} \\ i_{a\_OS}, & \text{OS Fault} \\ i_{a\_OP}, & \text{OP Fault} \end{cases} \tag{5-4}$$

5.3 Diagnostic Method Based on the Sampled and Estimated i_{a_OS}

5.3.1 Relationships between Polarities of the Sampled and Estimated i_{a_OS}

When no fault occurs, $\hat{i}_{a\_OS}$ has an opposite polarity to V_{bemfa}, as illustrated in Eq. (4-21). i_{a_samp} is under the healthy condition and can be represented by i_{a_H}. Therefore, it is necessary to discuss the relationships between the polarities of i_{a_H} and V_{bemfa}.

According to Clarke's transformation, $i_{a\_H} = i_{\alpha\_H}$. i_{α_H} can be inverse-converted from i_{d_H} and i_{q_H}, as shown in Eq. (5-5).

$$i_{\alpha\_H} = i_{d\_H}\cos\theta_e - i_{q\_H}\sin\theta_e \tag{5-5}$$

i_{d_H} and i_{q_H} can be substituted by Eq. (5-6), where I_s is the amplitude of the current vector; λ is the angle between the current vector and θ_e.

$$\begin{cases} i_{d\_H} = I_s\cos\lambda \\ i_{q\_H} = I_s\sin\lambda \\ I_s^2 = i_{d\_H}^2 + i_{q\_H}^2 \end{cases} \tag{5-6}$$

By incorporating Eq. (5-6), Eq. (5-5) is transformed into Eq. (5-7).

$$\begin{aligned} i_{\alpha\_H} &= I_s(\cos\lambda\cos\theta_e - \sin\lambda\sin\theta_e) \\ &= I_s\cos(\lambda+\theta_e) \end{aligned} \tag{5-7}$$

Assuming $i_{a\_H} = i_{\alpha\_H} = I_s$*sin $\omega_e t$, where $\omega_e t$ stands for the phase of i_{a_H}. It can be obtained from Eq. (5-7) that I_s*sin $\omega_e t = I_s$*cos($\lambda + \theta_e$). Furthermore, according to the trigonometric transformation, Eq. (5-8) can be obtained.

$$\omega_e t = \lambda + \theta_e + \frac{\pi}{2} \tag{5-8}$$

Considering the case of surface-mounted PMSM and $i_d = 0$ control, λ is equal to $\pi/2$. As a result, $\omega_e t = \theta_e + \pi$. Meanwhile, according to Eq. (3-2), the polarity of V_{bemfa} is opposite to the polarity of sinθ_e. Therefore, the polarity of i_{a_H} is the same as the polarity of V_{bemfa} and is opposite to sinθ_e.

$$L\left(i_{a\_value}\right) = \begin{cases} 1, & i_{a\_value} > \varepsilon_{digi} \\ 0, & \left|i_{a\_value}\right| < \varepsilon_{digi} \\ -1, & i_{a\_value} < -\varepsilon_{digi} \end{cases} \tag{5-9}$$

The polarity of the current is defined as positive when the current flows from the inverter to the motor winding, and is negative when it has a reverse direction. The current polarity is labelled as 1, 0, or −1 when the value has a positive, zero, or negative polarity, respectively, as defined in Eq. (5-9), where i_{a_value} can be either i_{a_samp} or $\hat{i}_{a\_OS}$; $L()$ denotes the polarity of the value; ε_{digi} is the sampling error, including noise, sensor error, and ADC resolution. ε_{digi} commonly exists and influences methods that require sampling.

Consequently, under the healthy condition, $\hat{i}_{a\_OS}$ and i_{a_samp} have opposite polarities, and $L(\hat{i}_{a\_OS})*L(i_{a\_samp}) < 0$.

Under the OS fault, as validated in Section 4.5, $\hat{i}_{a\_OS}$ accurately track the practical i_{a_OS} in real time. Hence, $\hat{i}_{a\_OS}$ and i_{a_samp} have the same polarities, and $L(\hat{i}_{a\_OS})*L(i_{a\_samp}) > 0$.

Under the OP fault, i_{a_samp} has a theoretical zero value, whereas $\hat{i}_{a\_OS}$ still has an opposite polarity to V_{bemfa}, that is, $L(\hat{i}_{a\_OS})*L(i_{a\_samp}) = 0$.

5.3.2 Relationships between Amplitudes of the Sampled and Estimated i_{a_OS}

Thus far, the estimated value of i_{a_OS}, $\hat{i}_{a\_OS}$, has been calculated in Section 4.4, and the sampled value of i_{a_OS}, i_{a_samp}, has been acquired in Section 5.2. Their residual error i_{a_resi} is defined in Eq. (5-10).

$$i_{a\_resi} = i_{a\_samp} - \hat{i}_{a\_OS} \tag{5-10}$$

Under the healthy condition, the relative amplitudes of i_{a_resi} and $\hat{i}_{a\_OS}$ can be expressed as in Eq. (5-11).

$$\left|i_{a\_resi}\right| = \left|i_{a\_samp} - \hat{i}_{a\_OS}\right| = \left|i_{a\_samp}\right| + \left|\hat{i}_{a\_OS}\right| > \left|\hat{i}_{a\_OS}\right| \tag{5-11}$$

Under the OS fault, $\hat{i}_{a\_OS}$ and ia_samp both comply with the practical value of i_{a_OS}, resulting in the amplitude relationship in Eq. (5-12).

$$\left|i_{a\_resi}\right| = \left|i_{a\_samp} - \hat{i}_{a\_OS}\right| = \left|i_{a\_samp}\right| - \left|\hat{i}_{a\_OS}\right| = \varepsilon_{digi} < \left|\hat{i}_{a\_OS}\right| \tag{5-12}$$

Under the OS fault, theoretically, the sampled i_{a_samp} and the estimated $\hat{i}_{a\_OS}$ should have identical amplitudes and polarities. However, due to sampling noises, the polarity of i_{a_samp} bounces between positive and negative when i_{a_OS} crosses 0, resulting in uncertain system status and misdiagnosis.

The zero-crossing uncertainty also applies to the healthy condition and the OP fault. Under the healthy condition, the polarity of i_{a_samp} also bounces when the phase current crosses 0.

Under the OP fault, theoretically, i_{a_samp} should be zero, but it also bounces around 0 due to sampling noises. Hence, diagnostic results when i_{a_samp} falls within the realm of sampling noises are not reliable.

Under the OP fault, ideally, $i_{a\_samp} = 0$, and the following relation holds:

$$\left|i_{a\_resi}\right| = \left|i_{a\_samp} - \hat{i}_{a\_OS}\right| = \left|\hat{i}_{a\_OS}\right| \tag{5-13}$$

Considering the error ε_{digi}, Eq. (5-13) is transformed into Eq. (5-14).

$$\left|\left|i_{a\_resi}\right| - \left|\hat{i}_{a\_OS}\right|\right| = \left|i_{a\_samp}\right| < \varepsilon_{digi} \tag{5-14}$$

5.3.3 Diagnostic Rules to Classify Open-Switch and Open-Phase Faults

Based on the distinct relationships under the healthy condition, OS fault, and OP fault, diagnostic rules can be designed and summarized in Table 5-1.

TABLE 5-1 Diagnostic Rules for Healthy Condition, OS Fault, and OP Fault

System State	Polarity Relationships	Amplitude Relationships
Healthy	$L(\hat{i}_{a\_OS})*L(i_{a\_samp}) = -1$	$\lvert i_{a\_resi}\rvert > \lvert\hat{i}_{a\_OS}\rvert$
OS Fault	$L(\hat{i}_{a\_OS})*L(i_{a\_samp}) = 1$	$\lvert i_{a\_resi}\rvert < \lvert\hat{i}_{a\_OS}\rvert$
OP Fault	$L(\hat{i}_{a\_OS})*L(i_{a\_samp}) = 0$	$\lvert i_{a\_resi}\rvert = \lvert\hat{i}_{a\_OS}\rvert$ $(\left\|\lvert i_{a\_resi}\rvert - \lvert\hat{i}_{a\_OS}\rvert\right\| = \lvert i_{a\_samp}\rvert < \varepsilon_{digi})$

According to the diagnostic rules in Table 5-1, the healthy state of the inverter can be diagnosed. However, the diagnosis should be enabled in the digital controller when the following condition is satisfied, where $P(D) = 1$ represents that event D is true:

$$P(D) = P\left(\left|\hat{i}_{a\_OS}\right| > \left|\varepsilon_{digi}\right|\right) = 1 \tag{5-15}$$

When $\left|\hat{i}_{a\_OS}\right| < \left|\varepsilon_{digi}\right|$, θ_e is approximately 0 or π where the diagnostic variables $\hat{i}_{a\_OS}$, i_{a_samp}, and i_{a_OS} are close to 0, and ε_{digi} significantly affects the diagnosis. The diagram of the control algorithm is shown in Fig. 5-6, where the proposed diagnostic method is highlighted. The motor is controlled under speed mode. n and n^* are the feedback and command of rotor speed, respectively; i_d^* and i_q^* are the control commands of i_d and i_q, respectively.

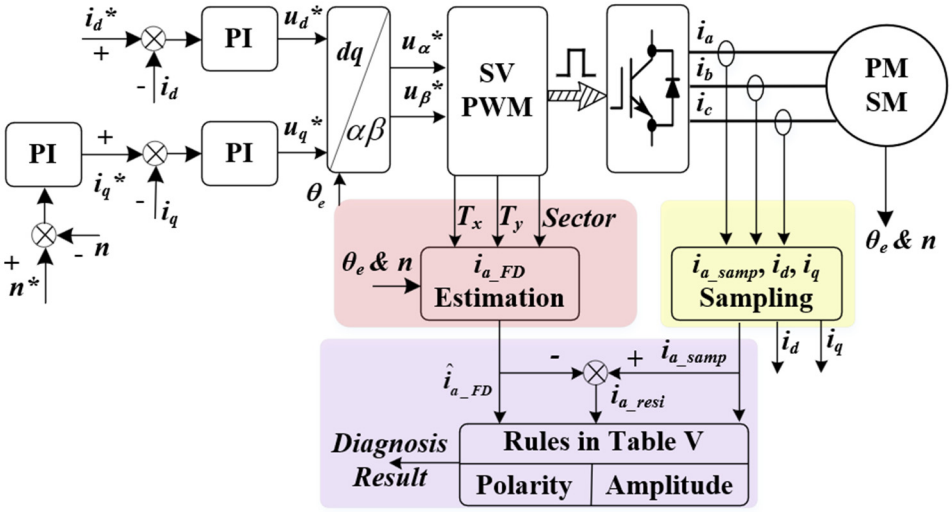


Fig. 5-6. Block diagram of the control scheme and diagnostic method.

5.4 Experimental Validation

The proposed sampling and diagnostic methods are validated using the same motor drive setup as shown in Chapter 3 and Chapter 4, but employing a different PMSM, which features a larger value of rotor flux. The parameter of the PMSM is shown in Table 5-2. The experimental setups are shown in Fig. 5-7.

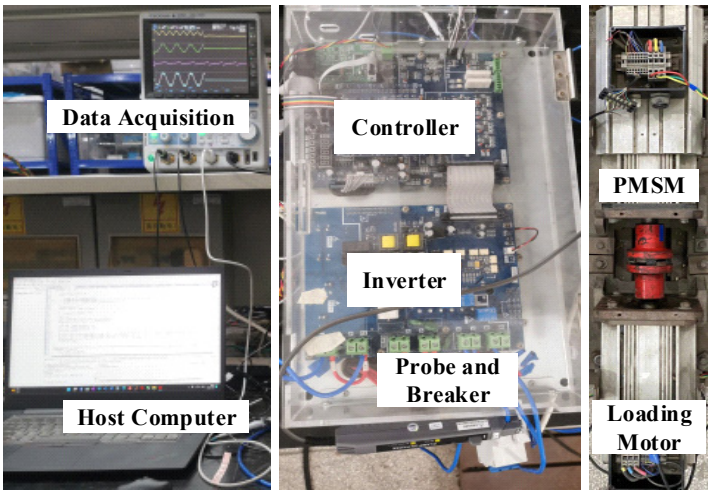


Fig. 5-7. Experimental setups.

TABLE 5-2 Parameters of PMSM

Parameter	Value	Unit
stator winding resistance R_s	0.306	Ω
d-axis inductance L_d	2.4	mH
q-axis inductance L_q	2.4	mH
number of pole pairs *p*	4	-
flux of the rotor PM Ψ_f	0.281	Wb
DC bus voltage	200	V
maximum speed under 200 V DC	1000	rpm

Considering the given parameter and DC bus voltage, the condition of $|V_{bemfa}| > V_{DC}/3$ can be achieved when the rotor speed is higher than 566 rpm. Therefore, the proposed methods are tested at 70 rpm, 500 rpm, and 900 rpm since i_{a_OS} has different conduction conditions when V_{bemfa} is on either side of $V_{DC}/3$.

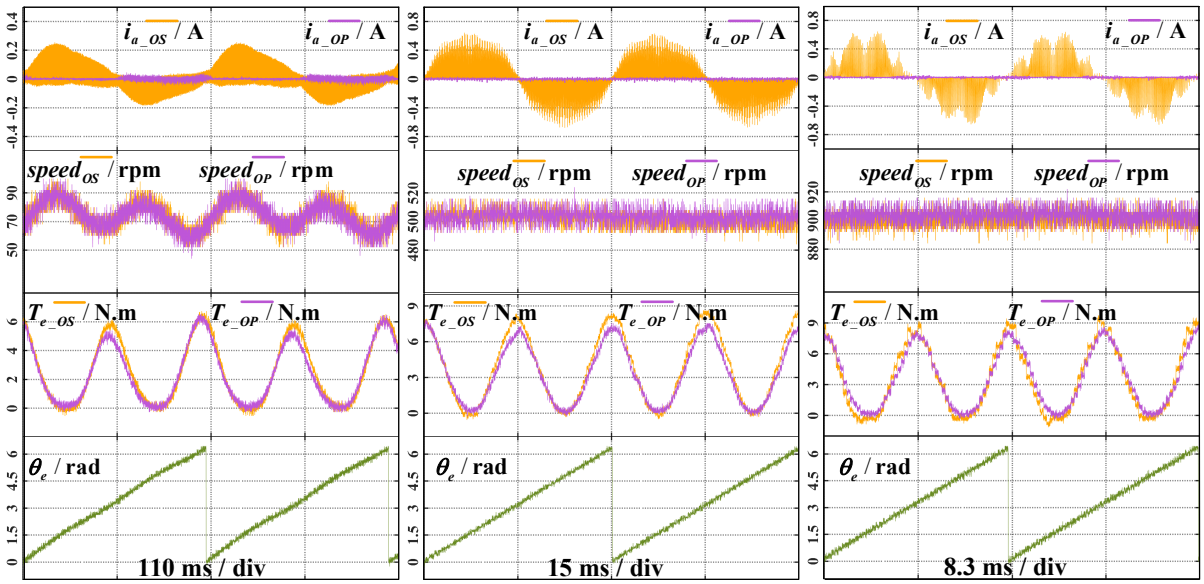
The current sensor (HX 15-P) has a nominal measuring range of 30 A (±15 A) and an accuracy of 0.15 A (1% of its nominal current). The built-in 12-bit ADC brings a resolution error of 0.024 A ((3.3 V / 4096) * 30 A ≈ 0.024 A). Consequently, the current sampling introduces a ε_{digi} exceeding 0.17A. In addition, unmeasured interferences, such as resistor drift, commonly exist in the sampling process. Hence, ε_{digi} is set as 0.25 A in accordance with the setups.

5.4.1 Comparison of Post-fault Speed and Torque Responses

Although the post-fault currents under the OS and OP faults differ significantly, the speed and torque responses are nearly identical and are difficult to distinguish, as shown in Fig. 5-8, where i_{a_OD}, $Speed_{OS}$, and T_{e_OS} denote the phase current, speed, and electromagnetic torque responses under the OS fault, respectively; i_{a_OP}, $Speed_{OP}$, and T_{e_OP} are the responses under the OP fault. The current waveforms are measured by a 50 MHz current probe *Cybertek* CP8050A.

In Fig. 5-8, the torque responses drop to 0 when θ_e is around π/2 and 3π/2. This occurs because, according to SVPWM, $\overrightarrow{v_3}$ or $\overrightarrow{v_4}$ accounts for the majority of the vector acting time

per switching period when θ_e is around $\pi/2$ or $3\pi/2$. However, under the OS and OP faults, they are equivalent to zero vectors.



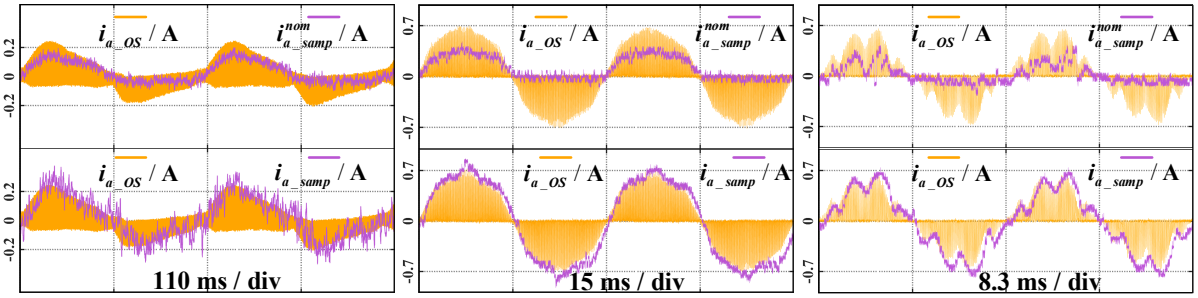
(a) (b) (c)

Fig. 5-8. Comparison of PF phase current, speed, and torque responses under OS fault and OP fault at (a) 70 rpm; (b) 500 rpm; (c) 900 rpm.

Taking $\overrightarrow{v_4}$ as an example, in a healthy motor drive, current flows from the positive DC bus via phase A and returns to the negative DC bus through phases B and C. But, under both the OS and OP faults, current from the positive DC bus is blocked as the power switches in phase A are open-circuit. Comparatively, when other voltage vectors, such as $\overrightarrow{v_5}$, are applied, the positive DC bus can still supply current from one of the remaining healthy phases to another. Consequently, applying $\overrightarrow{v_3}$ or $\overrightarrow{v_4}$ under the OS and OP faults fail to produce electromagnetic torque, leading to torque drops when θ_e is around $\pi/2$ or $3\pi/2$.

While torque responses are similar at different speeds, the faults induce speed fluctuations only at low speeds, attributed to the relatively larger mechanical time constant in the motor control system. At high speeds, the duration of the torque drop is shorter than the duration at low speeds. The inertia on the motor shaft helps maintain constant speed at high speeds, whereas the longer duration of torque fluctuations at low speeds allows the mechanical part to respond.

5.4.2 Validation of the Sampling Method of i_{a_OS}



(a) (b) (c)

Fig. 5-9. Comparison of normal and proposed sampling methods at different speeds: (a) 70 rpm where $V_{bemfa} < V_{DC}/3$; (a) 500 rpm where $V_{bemfa} < V_{DC}/3$; (b) 900 rpm where $V_{bemfa} > V_{DC}/3$.

The sampling method in Section 5.2 is compared with the regular method, as shown in Fig. 5-9, where $i^{nom}_{a\_samp}$ is sampled by the regular method and i_{a_samp} is from the proposed method.

The regular sampling method fails to detect the amplitude and the negative half of i_{a_OS}. The reason for the incomplete detection is that the normal sampling point is arranged at the beginning point of each switching period and coincides with the midpoint of $\overrightarrow{v_0}$ at the end of the previous period and $\overrightarrow{v_0}$ at the beginning of the current period. However, the negative i_{a_OS} does not conduct when applying $\overrightarrow{v_0}$. Additionally, the positive i_{a_OS} only reaches its half amplitude at this midpoint. Hence, the negative i_{a_OS} is lost, and the amplitude of the positive i_{a_OS} sampled by the normal method is approximately half of the measured amplitude.

Comparatively, the proposed method correctly samples the envelope and amplitude of i_{a_OS}, which validates the analysis of the activating switching state and provides the real value i_{a_samp} for fault diagnosis.

However, at 70 rpm, although the proposed sampling points are aligned with the occurrence of i_{a_OS}, i_{a_samp} is significantly influenced by the digital sampling error, ε_{digi}. To prevent misdiagnosis caused by ε_{digi}, the operating limit of the proposed diagnostic method follows the condition in (42), that is when the maximum value of $\hat{i}_{a\_OS}$ is less than ε_{digi}, the proposed diagnostic method will not be implemented. ε_{digi} affects not only the proposed diagnostic method but also other diagnostic methods requiring current sampling.

To minimize the impact of sampling noise, the diagnostic method can be further developed through the following strategies in the future:

1) **Utilizing high-accuracy current sensors and ADCs**. Sigma-Delta ADC can be employed to improve the sampling resolution and significantly reduce sampling noises. However, due to its one-bit sampling strategy, Sigma-Delta ADC generally requires an extended sampling time, which should be taken into account.

2) **Mutual calibration between current sensors**. By incorporating switching states and the plant model, phase currents can be reconstructed based on the DC bus current sensor and other phase current sensors. Calibration methods can be designed based on current reconstruction techniques to mitigate the impact of sensing inaccuracies.

3) **Mitigating noises with adaptive filters**. Filters with adaptive bandwidth can be designed to smooth the sampled low-amplitude i_{a_OS} and alleviate the zero-crossing polarity uncertainties. However, the designed filter should be applied to both the sampled and estimated values to ensure synchronization.

5.4.3 Validation of Diagnostic Variables under Different System Status

The pre-fault and post-fault status of the diagnostic variables in Table 5-1 are tested at 70 rpm, 500 rpm, and 900 rpm to validate the diagnostic rules, as shown in Figs. 5-10 and 5-11, respectively.

In Fig. 5-10 (a), when the motor drive is healthy, i_{a_samp} and $\hat{i}_{a\_OS}$ have opposite polarities. As a result, $|i_{a\_resi}| > |\hat{i}_{a\_OS}|$ can be guaranteed, as described in Table 5-1. The diagnosis is not implemented when $P(D) = 0$ to avoid uncertainties posed by the sampling error, ε_{digi}.

In Fig. 5-10 (b), when the motor drive is under the OS fault, i_{a_samp} and $\hat{i}_{a\_OS}$ have same the polarities and nearly identical amplitudes. The amplitude of their residues, viz. $|i_{a\_resi}|$, are resulted from the sampling errors. Hence, $|i_{a\_resi}| < |\hat{i}_{a\_OS}|$ is ensured. Consequently, the diagnostic variables comply with the states and rules of the OS fault in Table 5-1.

In Fig. 5-10 (c), when the motor drive is under the OP fault, i_{a_samp} is approximately zero and is influenced by the sampling errors, whereas $|\hat{i}_{a\_OS}|$ deviates from zero since it is calculated based on V_{bemfa} and the conduction time. Since i_{a_samp} is less than the preset ε_{digi}, its polarity is diagnosed as zero. Meanwhile, $|i_{a\_resi}|$ is nearly identical to $|\hat{i}_{a\_OS}|$, and their residues drop

into the range of ε_{digi}. Therefore, the diagnostic variables under the OP fault also comply with the rules in Table 5-1.

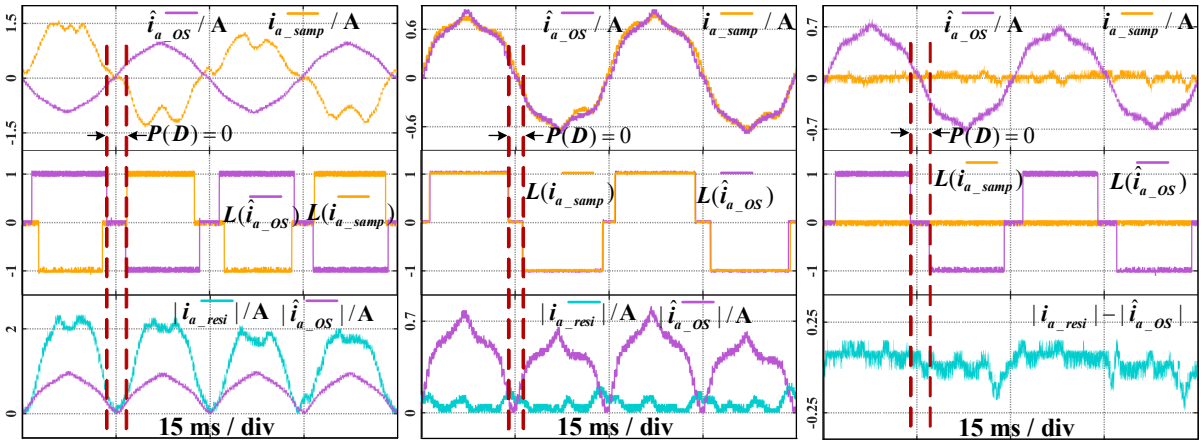


Fig. 5-10. At 500 rpm, diagnostic variables under different conditions: (a) Healthy condition; (b) OS fault; (c) OP fault.

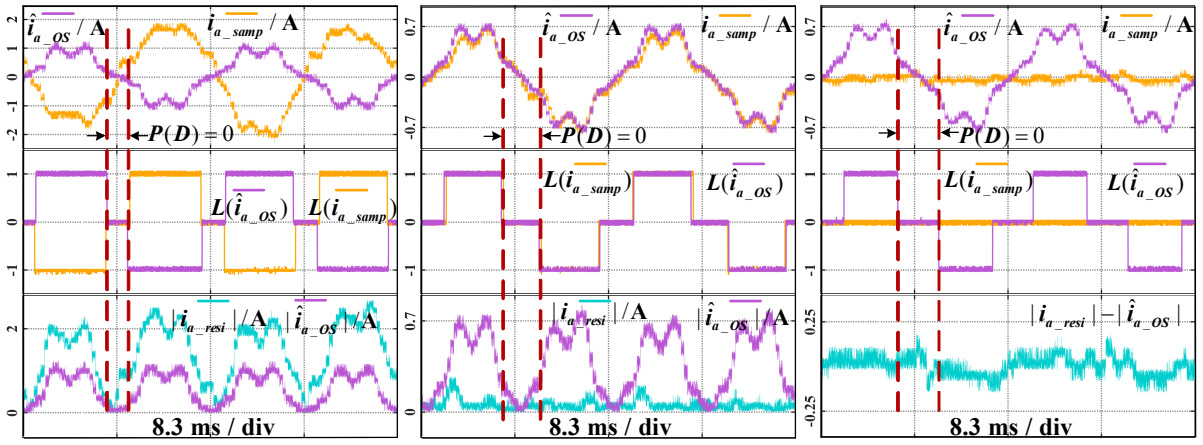


Fig. 5-11. At 900 rpm, diagnostic variables under different conditions: (a) Healthy condition; (b) OS fault; (c) OP fault.

Furthermore, the diagnostic variables follow the rules in Table 5-1 at 900 rpm, as shown in Fig. 5-11.

5.4.4 Performance Tests of the Diagnostic Method

The performance of the diagnostic method is tested by emulating the OS and OP faults at 500 rpm and 900 rpm. In these tests, the diagnostic time is denoted as *Time*(*D*); *Flag*(*D*) = 1, 0, -

1 corresponds to the OS fault, the healthy condition, and the OP fault, respectively. At each speed, diagnoses of the OS or OP faults are tested at 3 random phase points separately, resulting in a total of 6 tests for each fault type. In every test, transitions of diagnostic variables from a healthy condition to the OS or OP faults are presented.

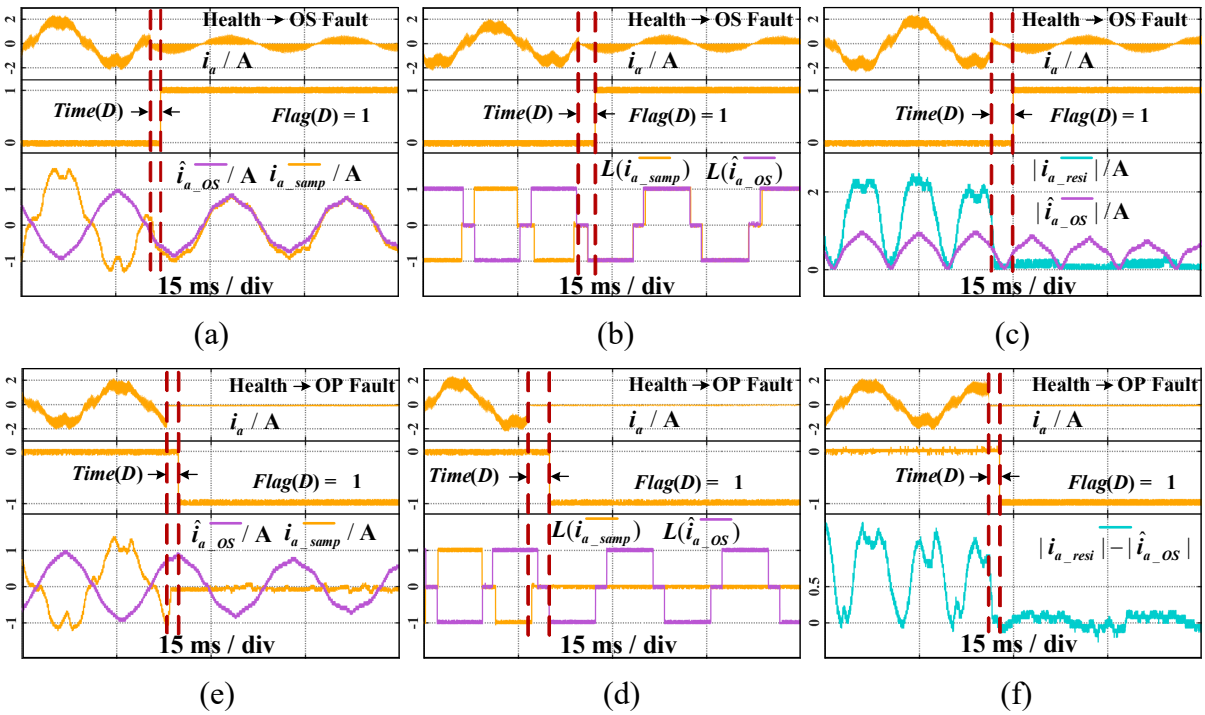


Fig. 5-12. Tests at 500 rpm when emulating the OS fault: (a), (b), and (c); when emulating the OP fault: (d), (e), and (f).

At 500 rpm, the transitions of the diagnostic variables when the OS fault is emulating are shown in Fig. 5-12 (a), (b), and (c), and the transitions of the OP fault are shown in Fig. 5-12 (d), (e), and (f). It can be observed that *Time*(*D*) is affected by the phase point where the fault occurs, because the diagnosis is disabled in the phase range where $P(D) = 0$ ($|\hat{i}_{a\_OS}| < |\varepsilon_{digi}|$). At the emulating points where the amplitude of $\hat{i}_{a\_OS}$ is away from the boundaries of ε_{digi}, the fault can be quickly detected, as shown in Fig. 5-12 (a), (d), and (f). In contrast, at the emulating points where the amplitude $\hat{i}_{a\_OS}$ is close to or crosses ε_{digi}, the diagnostic time is relatively long, as shown in Fig. 5-12 (b), (c), and (e). Although *Time*(*D*) is affected by the fault occurrence point, the diagnoses in the 6 random tests are completed in less than 1/4 of an electrical fundamental period.

Notably, the currents under the healthy condition in Fig. 5-12 feature significant distortion and ripple. The distortion is mainly caused by current harmonics, which are brought by

different factors, predominantly the 5th and 7th current harmonics. Factors leading to high harmonics include non-linearity caused by the dead time of the inverter. In the experiment, the switching period was set to 100 us, and the dead zone was set to 6 us. Furthermore, inaccurate current feedback also contributed to the distortion. In the experiment, the accuracy of the current sensor was relatively low, and the built-in 12-bit ADC of the DSP had a long sampling time due to sequential sampling.

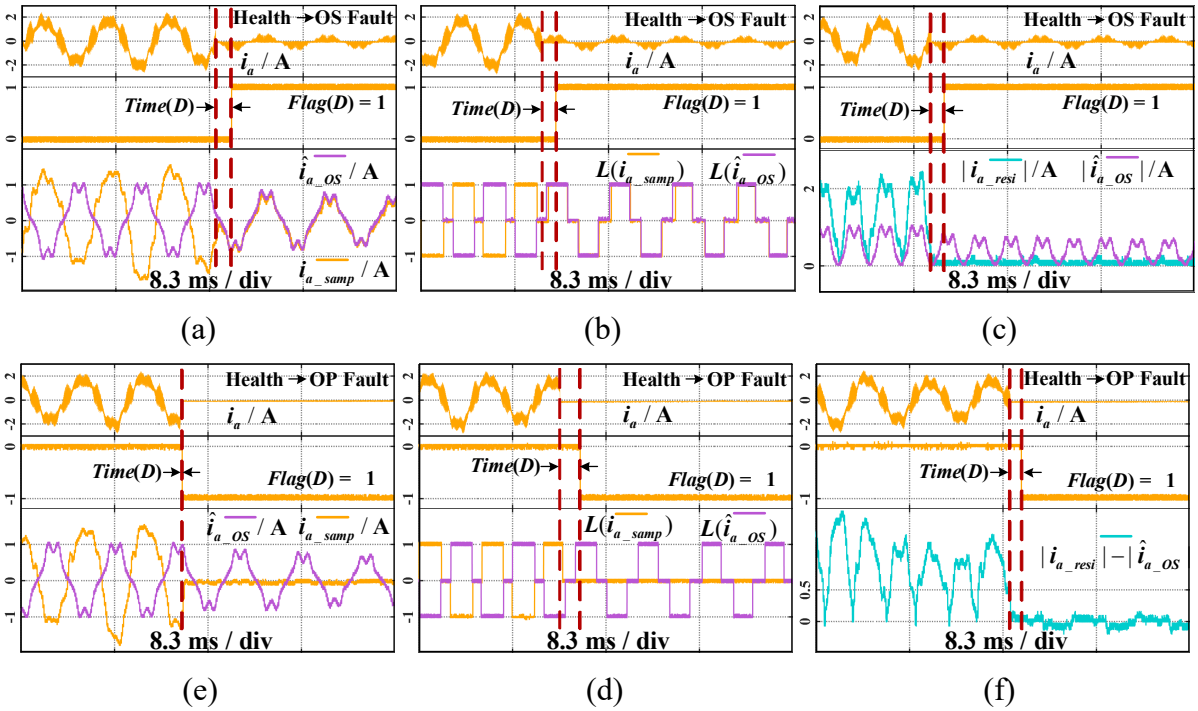


Fig. 5-13. Tests at 900 rpm when emulating the OS fault: (a), (b), and (c); when emulating the OP fault: (d), (e), and (f).

The primary cause of the current ripple is the relatively low DC bus voltage. Because of the limited DC bus voltage in the laboratory, the motor operates in the over-modulation zone and has severe current distortion. On the other hand, measurement noise is also one of the reasons why the ripple appears relatively large. In the experiment, the bandwidth of the current probe was 50 MHz, and the oscilloscope's sampling bandwidth was full bandwidth. While a high bandwidth is beneficial for capturing current dynamics, it also introduces more measurement noises.

The test results at 900 rpm are shown in Fig. 5-13. Notably, the phase current under healthy conditions is distorted, as the motor operates in the overmodulation region. In Fig. 5-13 (e), the diagnostic method shows the worst performance because the fault occurs when the phase

current is about to cross the boundary of ε_{digi}. The best diagnosis performance is shown in Fig. 5-13 (d), where the fault occurs around the peak of the phase current (also the peak of $|V_{bemfa}|$), which leaves a margin allowing the diagnosis process to complete. Similar to the diagnoses at 500 rpm, the 6 random tests are completed in 1/4 of the electrical fundamental period, further validating the effectiveness of the proposed diagnostic method.

5.5 Summary

To classify the OS and OP faults, this chapter proposes: a) a sampling method empowering the motor drive to detect the post-fault current under the OS fault, and b) a set of diagnostic variables and diagnostic rules responding to different system states. The following merits of the proposed methods have been validated in experiments:

a) Compared with the regular current sampling, the proposed sampling method can detect the envelope and amplitude of the post-fault current under the OS fault and provides the actual value for diagnosis.

b) The proposed diagnostic method effectively depicts the characteristics of each system state. In addition, the state of each diagnostic variable in each valid diagnosis phase range is stable due to the consideration of sampling errors. In the tests, the diagnostic method can detect faults in less than 1/4 of an electrical fundamental period.

c) The sampling and estimation methods of the post-fault current under the OS fault remain effective as long as the motor is operating. However, the diagnostic method has a low limit on the motor operating speed. The limit is posed by the current sampling error.

Chapter 6 A Fault-Tolerant Control Method for Open-Switch Fault in 3P2L PMSM Drives at Low Speed

6.1 Introduction

From Chapter 3 to Chapter 5, the dynamic models of 3P2L PMSM drives under two types of open-circuit faults are established, and diagnostic rules are proposed to classify the healthy condition, OS fault, and OP fault. Notably, the models, the sampling method, and the diagnostic method are developed in the independent *abc* phase frame, rather than the *dq* frame, because the post-fault model is no longer decoupled in the *dq* frame. In contrast, due to the mutually canceled voltages induced by mutual inductances, the post-fault independent phase model is decoupled from the parameters of the remaining healthy phases. Consequently, the proposed models and methods from Chapter 3 to Chapter 5 can be conveniently expanded to multi-phase PMSMs and their drives, such as dual three-phase PMSM drives and six-phase PMSM drives, which have intrinsic high reliability compared with the 3P2L PMSM drive.

Fault-tolerant methods of multi-phase PMSM drives have been extensively developed to exploit their inherent redundancy. In contrast, the 3P2L PMSM drive has limited fault-tolerant capability but is the most commonly used topology due to its simple structure and low cost. Therefore, although the 3P2L PMSM drive has inevitable torque pulsation under open-circuit faults, it is still necessary to maintain the post-fault drivability and alleviate secondary damages.

As the fault types of the open-circuit fault are diverse, this chapter focuses on developing an embedded fault-tolerant method for single OS faults, where the half leg of the faulty phase is open. Specifically, the proposed method targets to alleviate the speed and torque pulsations at low speeds, where the steady mechanical motion will also be affected by the fault. At low speeds, the differences between the OS fault and OP fault are negligible because of the relatively low value of back-EMF. Hence, the fault-tolerant control has a better generality at

low speeds.

Firstly, the correspondence between the post-fault mechanical responses and the voltage vectors is analyzed to identify the predominant voltage vectors that incur the speed and torque pulsations. Furthermore, the influences of the OP fault on the voltage vectors are described in the complex domain. Based on the prefault and post-fault voltage vectors, a re-allocation strategy for the vector acting time is proposed to track the healthy reference vector. Additionally, the control references of post-fault currents are redesigned to adapt the post-fault coupled model in the *dq* frame. Moreover, to guarantee an accurate transition of the fault-tolerant current control under the healthy condition and the fault condition, a transition-enabling mechanism is designed based on the residual error from the conventional prediction model and the prediction model proposed in Chapter 2. Finally, the effectiveness of the proposed method is validated by simulations and experiments.

6.2 Influences of the Single Open-Switch Fault on System Responses

The effects of faults on the mechanical responses of the motor have been discussed in subsection 4.5.3 and subsection 5.4.1. However, a detailed analysis of the underlying factors that contribute to these effects has not been provided. This section is dedicated to investigating the motor speed response and the inevitable torque pulsations in 3P2L PMSM drives when they operate under faulty conditions. It also analyzes how faults impact the amplitudes and spatial directions of the inverter voltage vectors. In this chapter, the single OS fault is assumed to occur at the upper half leg of phase A, viz. T_1 open-switch fault.

6.2.1 Analysis of Post-fault System Responses and Corresponding Voltage Vectors

Under the healthy condition, the three-phase currents are sinusoidally balanced due to the symmetrical configuration of motor windings, which can be expressed in Eq. (6-1).

$$\begin{cases} i_a = I_s \sin(\omega_e t) \\ i_b = I_s \sin(\omega_e t - 2\pi/3) \\ i_c = I_s \sin(\omega_e t + 2\pi/3) \end{cases} \tag{6-1}$$

By incorporating the transformation matrix in Eq. (3-14), the three-phase currents can be converted into the *dq* frame, as described in Eq. (6-2).

$$\begin{aligned} \begin{pmatrix} i_d \\ i_q \end{pmatrix} &= \frac{2}{3} \begin{pmatrix} \cos\theta_e & \cos(\theta_e - 2\pi/3) & \cos(\theta_e + 2\pi/3) \\ -\sin\theta_e & -\sin(\theta_e - 2\pi/3) & -\sin(\theta_e + 2\pi/3) \end{pmatrix} \begin{pmatrix} I_s \sin(\omega_e t) \\ i_b = I_s \sin(\omega_e t - 2\pi/3) \\ i_b = I_s \sin(\omega_e t + 2\pi/3) \end{pmatrix} \\ &= I_s \begin{pmatrix} \sin\omega_e t \cos\theta_e - \cos\omega_e t \sin\theta_e \\ -\sin\omega_e t \sin\theta_e - \cos\omega_e t \cos\theta_e \end{pmatrix} \end{aligned} \tag{6-2}$$

In the absence of faults or when the phase current conducts through the remaining healthy power switch of the faulty phase, by incorporating $\omega_e t = \theta_e + \pi$ from subsection 5.3.1 into Eq. (6-2) yields $i_d = 0$ and $i_q = I_s$. For simplicity, the post-fault current of the faulty phase is considered 0 because it is of the level of milliamperes and is significantly smaller than the surging post-fault currents of the remaining healthy phases. As a result, the post-fault i_d and i_q can be expressed in Eq. (6-3), where i_d^f, i_q^f, and i_b^f are the post-fault i_d, i_q, and i_b, respectively.

$$\begin{cases} i_d^f = \frac{2}{3}[\cos(\theta_e - \frac{2}{3}\pi) i_b^f - \cos(\theta_e + \frac{2}{3}\pi) i_b^f] = \frac{2\sqrt{3}}{3} i_b^f \sin\theta_e \\ i_q^f = \frac{2}{3}[-\sin(\theta_e - \frac{2}{3}\pi) i_b^f + \sin(\theta_e + \frac{2}{3}\pi) i_b^f] = \frac{2\sqrt{3}}{3} i_b^f \cos\theta_e \\ i_d^f = i_q^f \tan\theta_e \end{cases} \tag{6-3}$$

By incorporating i_q^f into the electromagnetic torque equation of a surface-mounted PMSM, the post-fault electromagnetic torque can be written in Eq. (6-4), where T_e^f stands for the post-fault torque; p is the number of rotor pole pairs.

$$T_e^f = \sqrt{3} \cdot p \cdot \Psi_f \cdot i_b^f \cdot \cos\theta_e \tag{6-4}$$

To better analyze the system responses, the T_1 OS fault is simulated in MATLAB/SIMULINK. The responses of speed, three-phase currents, and *q*-axis current of the faulty half in a fundamental period are shown in Fig. 6-1. Moreover, the voltage vectors

being implemented during the speed and torque pulsations are identified by incorporating Fig. 4-4.

By incorporating the voltage vectors and spatial sectors in SVPWM as depicted in Fig. 6-1, where $\overrightarrow{v_s}$ is the reference voltage vector regulated by the current controllers and is eventually synthesized by inherent voltage vectors $\overrightarrow{v_0} \sim \overrightarrow{v_7}$, the responses in the three stages are elucidated. It can be seen from Fig. 6-2 that although the motor operates under the faulty condition from approximately 0.514 s due to the blocked path of positive i_a, the motor maintains its speed and torque during the *Holding* stage.

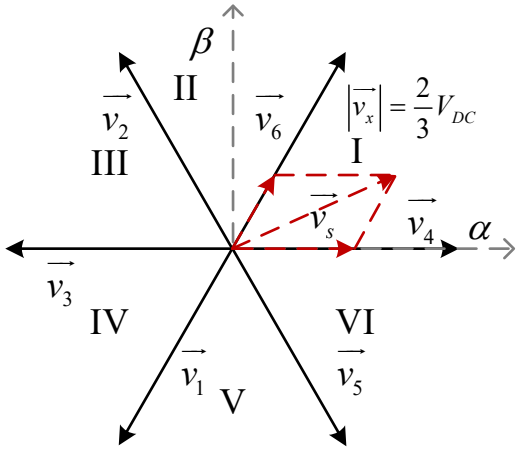


Fig. 6-1. Voltage vectors and spatial sectors in SVPWM.

Holding: the reference vector $\overrightarrow{v_s}$ generated by the current controller rotates from late Sector V to early Sector VI and $\overrightarrow{v_5}^f$ accounts for the longer acting time in both sectors following SVPWM. Compared to Sector V, the T_1 OS fault has a more significant impact on the two vectors in Sector VI, thus resulting in the higher three-phase duty ratio in early Sector VI, as shown in Fig. 6-3 (a). It should be noted that although the motor speed is maintained, the acting time of each vector in the two sectors is increased compared to the healthy state, resulting in a relatively higher duty ratio.

Dropping: $\overrightarrow{v_s}$ locates in late Sector VI and early Sector I. $\overrightarrow{v_4}^f$ accounts for most of the acting time in both sectors. $\overrightarrow{v_5}^f$ and $\overrightarrow{v_6}^f$ constitute the rest of the switching cycle in each sector, as shown in Fig. 6-3 (b). As $\overrightarrow{v_s}$ crosses the boundary between Sector VI and Sector I, SVPWM allocates almost all of the acting time to $\overrightarrow{v_4}^f$. Meanwhile, i_b^f, i_c^f, and i_q^f converge to zero and incurring the maximum deceleration at this point. Once $\overrightarrow{v_s}$ passed through the boundary,

SVPWM starts allocating acting time to $\overrightarrow{v_6^f}$ and recovering the currents, hence slowing down the deceleration until zero. Meanwhile, due to the regulation triggered by the speed error, the acting time of zero vectors, viz. $\overrightarrow{v_0}$ and $\overrightarrow{v_7}$, is mostly eliminated, thus reaching the highest duty ratio.

Recovering: $\overrightarrow{v_s}$ rotates from late Sector I to early Sector II, in which $\overrightarrow{v_6^f}$ is the dominant voltage vector. When $\overrightarrow{v_s}$ locates in Sector I, the acting time of $\overrightarrow{v_0}$ and $\overrightarrow{v_7}$ remain zero due to the speed error. After $\overrightarrow{v_s}$ reached Sector II, the rising acting time of $\overrightarrow{v_2}$ guarantees the continuous rise of the Phase *B* duty ratio. i_b^f and i_c^f continue to increase reversely considering that the phase A current is still blocked. According to Eq. (6-4), T_e^f exceeds the load torque due to the rising i_b^f, hence the speed starts recovering and is fully recovered until the phase A current participates in the regulation again.

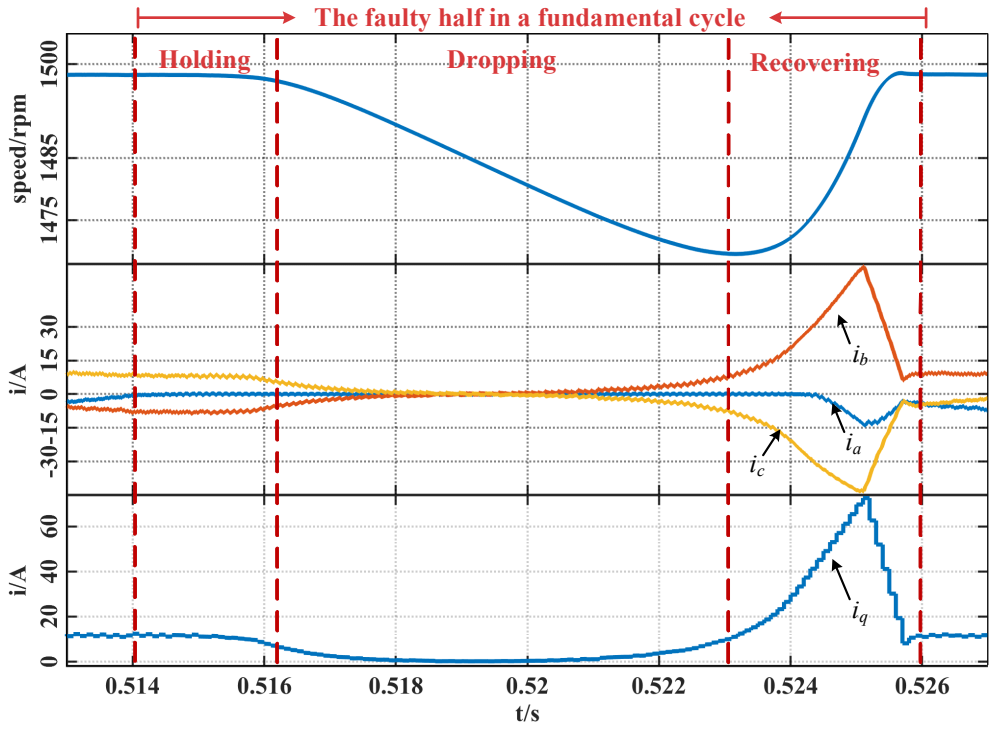


Fig. 6-2. Responses in the faulty half of a fundamental period.

The typical switching states in one switching cycle are depicted in Fig. 6-3 for the *Holding*, *Dropping,* and *Recovering* stages, and provide the basis of the fault-tolerant modulation method that will be presented in the next section. It should also be noted that the fault diagnosis process is based on extracting and evaluating post-fault responses but does not influence the post-fault control and responses.

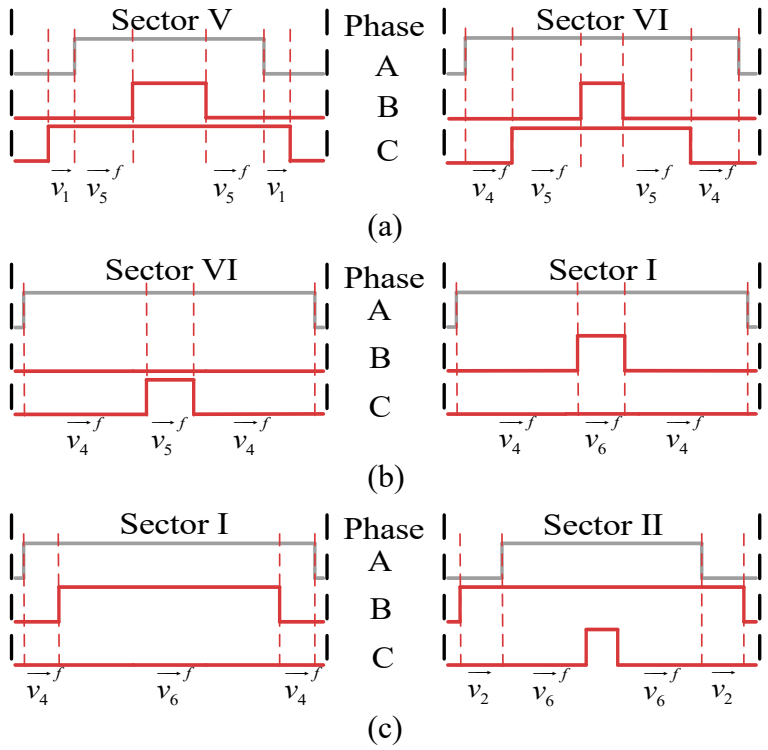


Fig. 6-3. Typical switching states in the three stages of the faulty half of a fundamental period: (a). *Holding*; (b). *Dropping*; (c). *Recovering*.

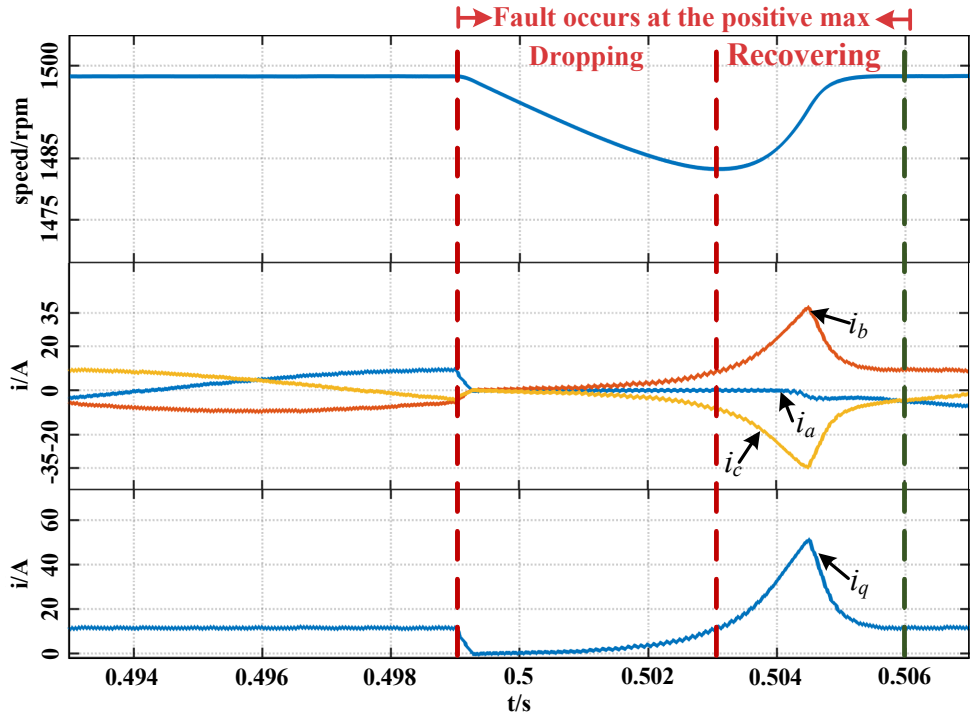


Fig. 6-4. Responses when the fault occurs at the point of positive maximum current.

The above analysis supposes T_1 has opened before the phase-A current enters its positive half. Furthermore, the responses when the fault occurs during the positive half are shown in Fig. 6-

4 and analyzed below:

Compared to Fig. 6-2, the *Holding* stage has been skipped because most of the acting time has been allocated to the zero-equivalent $\overrightarrow{v_4}^f$ in later Sector VI and Early Sector I. Therefore, i_q^f decreases to zero rapidly. Then, the system enters the *Dropping* and *Recovering* stages where responses and switching states are similar to Fig. 6-2, Fig. 6-3 (b), and Fig. 6-3 (c).

The post-fault response is also affected by the inertia on the rotor, as can be seen from the motor motion equation, where ω_m is the mechanical speed, T_L is the load torque, J is the inertia on the rotor and B is the damping coefficient.

$$\frac{d\omega_m}{dt} = \frac{(T_e - T_L)}{J} - \frac{B\omega_m}{J} \tag{6-5}$$

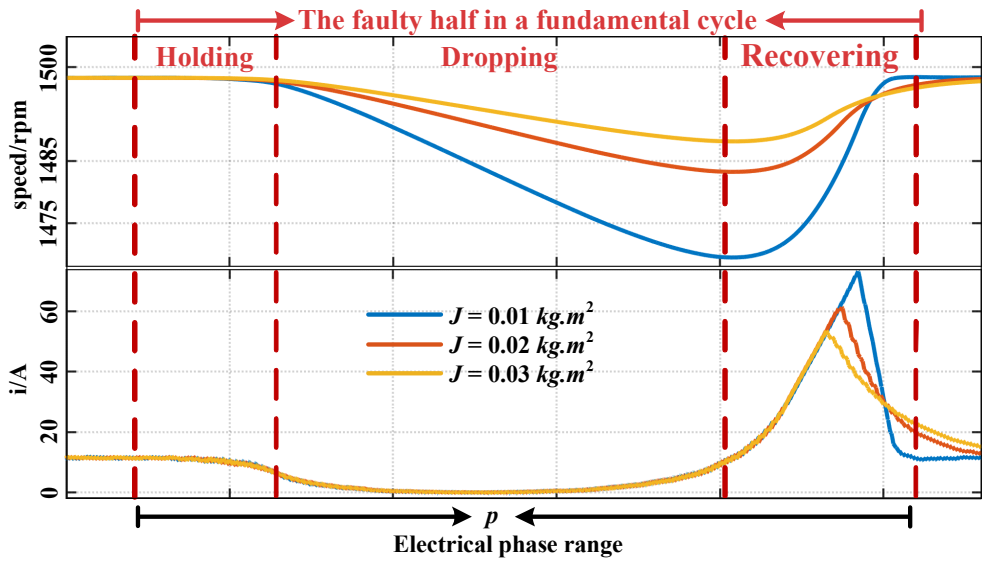


Fig. 6-5. Responses of speed and torque current under different values of inertia.

The greater the inertia, the gentler the speed drop and the smaller recovery i_q are likely to be. However, the inertia does not affect T_e when the motor operates at a constant speed. Also, the torque drop caused by blocked paths maintains the same under different values of inertia. Therefore, the effect of motor inertia can be concluded: a) The inertia does not influence the *Holding* stage; b) Large inertia alleviates the speed drop during the *Dropping* stage; c) In the *Recovering* stage, a smaller current peak is attributed to the alleviated speed drop. The post-fault responses with different values of inertia are shown in Fig. 6-5.

6.2.2 Analysis of Post-fault Voltage Vectors in 3P2L PMSM Drives

A 3P2L inverter has 8 inherent voltage vectors. Due to the blocked current path via the upper power switch of phase A, three inherent voltage vectors are affected under the T_1 OS fault, including $\overrightarrow{v_4}^f$, $\overrightarrow{v_5}^f$, and $\overrightarrow{v_6}^f$, as shown in Fig. 6-6.

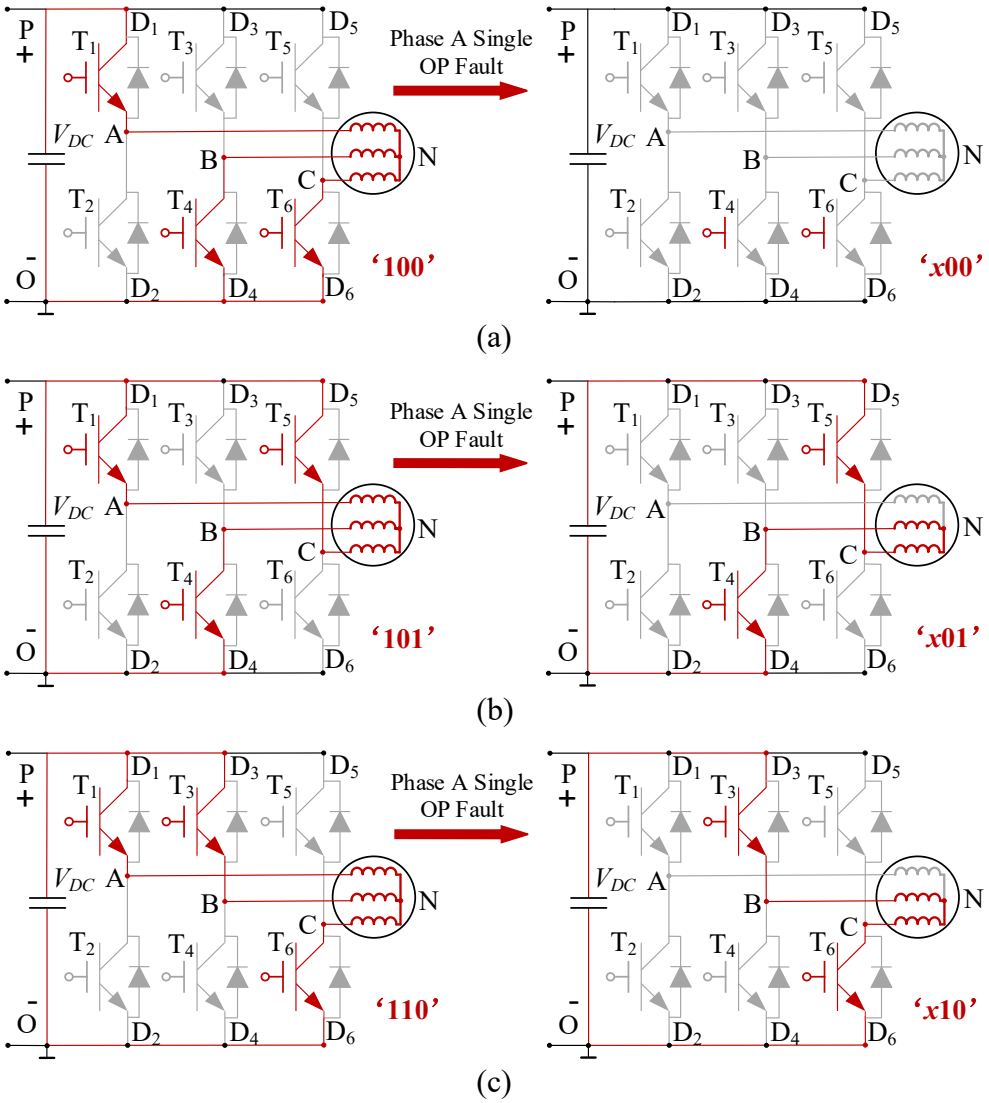


Fig. 6-6. Three switching states affected by T_1 OS fault: (a) "100"; (b) "101"; (c) "110".

According to the analysis in Chapter 3 and Chapter 4, when the motor is under the T_1 OS fault and operates at low speeds where the peak value of V_{bemfa} is less than $V_{DC}/3$, the faulty upper leg can be conducted by the zero vector $\overrightarrow{v_7}$, which is equivalent to its healthy state and results in zero three-phase voltages. Meanwhile, when applying $\overrightarrow{v_4}^f$, $\overrightarrow{v_5}^f$, and $\overrightarrow{v_6}^f$, the faulty phase cannot be conducted, and the three-phase voltages are associated with V_{bemfa} and V_{DC}, as illustrated in Eq. (3-8).

However, to simplify the targeted fault-tolerant method which involves the reallocation of the

vector acting time based on the amplitude and phase of the post-fault voltage vectors, the items of V_{bemfa} in the post-fault phase voltages have been temporarily not taken into account out of two considerations:

1) At low speeds, the amplitude of V_{bemfa} is significantly lower than V_{DC}. For instance, according to the parameters of PMSM in this chapter, V_{bemfa} peaks at approximately 10 V, much less than the 200 V V_{DC}.
2) The peak value of V_{bemfa} occurs only when θ_e reaches π/2 or 3π/2, while V_{bemfa} converges to zero when the phase of θ_e deviates from π/2 or 3π/2. The non-peak value of V_{bemfa} further alleviates the influence on the post-fault phase voltages.

Hence, by neglecting the V_{bemfa} items, the post-fault phase voltages in $\overrightarrow{v_4}^f$, $\overrightarrow{v_5}^f$, and $\overrightarrow{v_6}^f$ can be described in Table 6-1 for comparison with the healthy phase voltages.

In accordance with the phase voltage excitations in each voltage vector, the inherent space vectors can be calculated by Eq. (6-6).

TABLE 6-1 Healhty and Faulty Phase Voltages Neglecting V_{bemfa}

Switching State	Healthy Phase Voltages			Simplified Phase Voltages under T_1 OS Fault		
	u_{an}	u_{bn}	u_{cn}	u_{an}	u_{bn}	u_{cn}
$\overrightarrow{v_4}$ (100)	$\frac{2}{3}V_{DC}$	$-\frac{1}{3}V_{DC}$	$-\frac{1}{3}V_{DC}$	0	0	0
$\overrightarrow{v_5}$ (101)	$\frac{1}{3}V_{DC}$	$-\frac{2}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	0	$-\frac{1}{2}V_{DC}$	$\frac{1}{2}V_{DC}$
$\overrightarrow{v_6}$ (110)	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$-\frac{2}{3}V_{DC}$	0	$\frac{1}{2}V_{DC}$	$-\frac{1}{2}V_{DC}$

$$\begin{cases} \vec{v} = u_{an}e^{j0} + u_{bn}e^{j\frac{2}{3}\pi} + u_{cn}e^{j\frac{4}{3}\pi}, & \text{in } a\text{-}b\text{-}c \text{ frame} \\ \vec{v} = \frac{2}{3}(u_{an}e^{j0} + u_{bn}e^{j\frac{2}{3}\pi} + u_{cn}e^{j\frac{4}{3}\pi}), & \text{in } \alpha\text{-}\beta \text{ frame} \end{cases} \tag{6-6}$$

Under the healthy condition, the amplitude of each active vector is V_{DC} in the *abc* frame or $(2/3)V_{DC}$ in the *αβ* frame. However, $\overrightarrow{v_4}$, $\overrightarrow{v_5}$, $\overrightarrow{v_6}$ are forced to change under the T_1 OS fault. By incorporating the voltage excitation values in Table 6-1 into Eq. (6-6), the amplitudes and phases of $\overrightarrow{v_4}$, $\overrightarrow{v_5}$, $\overrightarrow{v_6}$ and the faulty vectors $\overrightarrow{v_4}^f$, $\overrightarrow{v_5}^f$, $\overrightarrow{v_6}^f$ in the *αβ* frame can be obtained. For

instance, $\overrightarrow{v_6}$ and $\overrightarrow{v_6}^f$ can be expressed in Eq. (6-7).

$$\begin{cases} \overrightarrow{v_6} = \frac{2}{3}\left(\frac{V_{DC}}{3}e^{j0} + \frac{V_{DC}}{3}e^{j\frac{2}{3}\pi} - \frac{2V_{DC}}{3}e^{j\frac{4}{3}\pi} \right) = \frac{2V_{DC}}{3}e^{j\frac{\pi}{3}} = \frac{V_{DC}}{3} + j\frac{\sqrt{3}V_{DC}}{3} \\ \overrightarrow{v_6}^f = \frac{2}{3}\left(0e^{j0} + \frac{V_{DC}}{2}e^{j\frac{2}{3}\pi} - \frac{V_{DC}}{2}e^{j\frac{4}{3}\pi} \right) = \frac{\sqrt{3}V_{DC}}{3}e^{j\frac{\pi}{2}} = j\frac{\sqrt{3}V_{DC}}{3} \end{cases} \quad (6\text{-}7)$$

The influenced voltage vectors under the healthy state and the T_1 OS fault are summarized in Table 6-2:

TABLE 6-2 Changes in Amplitudes and Phases of Three Influenced Vectors

Healthy Voltage Vectors			Voltages Vectors under T_1 OS Fault		
$\overrightarrow{v_4}$ (100)	$\overrightarrow{v_5}$ (101)	$\overrightarrow{v_6}$ (110)	$\overrightarrow{v_4}^f$ (x00)	$\overrightarrow{v_5}^f$ (x01)	$\overrightarrow{v_6}^f$ (x10)
$\frac{2}{3}V_{DC}e^{j0}$	$\frac{2}{3}V_{DC}e^{j-\frac{\pi}{3}}$	$\frac{2}{3}V_{DC}e^{j\frac{\pi}{3}}$	0	$\frac{\sqrt{3}}{3}V_{DC}e^{j-\frac{\pi}{2}}$	$\frac{\sqrt{3}}{3}V_{DC}e^{j\frac{\pi}{2}}$

The results in Table 6-2 show that the amplitudes of $\overrightarrow{v_5}^f$ and $\overrightarrow{v_6}^f$ reduced to $\sqrt{3}/2$ of the amplitudes of $\overrightarrow{v_5}$ and $\overrightarrow{v_6}$, while $\overrightarrow{v_4}^f$ is considered as a zero vector, as depicted in Fig. 6-7.

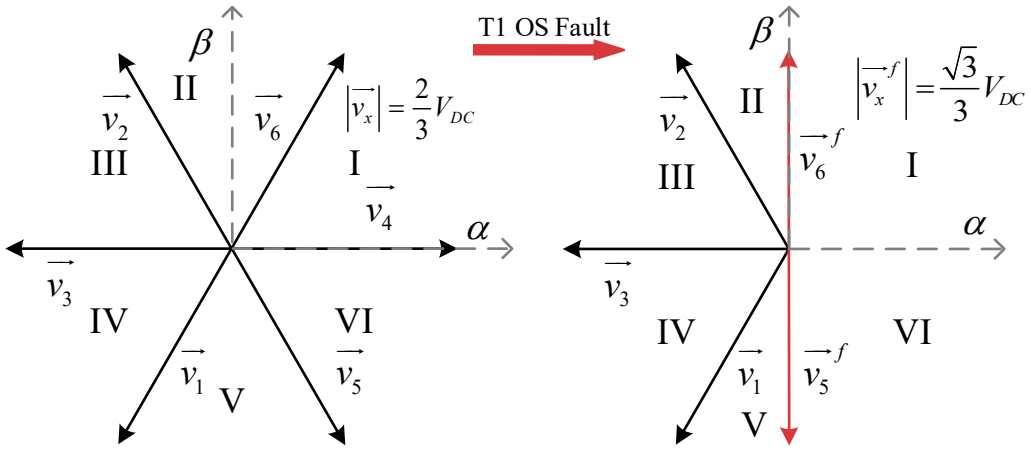


Fig. 6-7. Three switching states affected by T_1 OS fault: (a) "100"; (b) "101"; (c) "110".

Furthermore, the post-fault voltage vector ignoring the back-EMF can be compared with the practical voltage vectors that consider V_{bemfa} into the phase voltages. By incorporating the post-fault phase voltages in Eq. (3-8) into Eq. (6-6), the practical post-fault $\overrightarrow{v_6}$ can be expressed in Eq. (6-8) and Fig. 6-8, where $\overrightarrow{v_6}^{OP}$ stands for $\overrightarrow{v_6}$ under the OP fault which is the practical condition when applying $\overrightarrow{v_6}$ under the OS fault and $V_{bemfa} < V_{DC}/3$.

$$\vec{v}_6^{OP} = \frac{2}{3}\left(0e^{j0} + \frac{V_{DC} - V_{bemfa}}{2}e^{j\frac{2}{3}\pi} + \frac{-V_{DC} - V_{bemfa}}{2}e^{j\frac{4}{3}\pi}\right) = \frac{V_{bemfa}}{3} + j\frac{\sqrt{3}V_{DC}}{3} \tag{6-8}$$

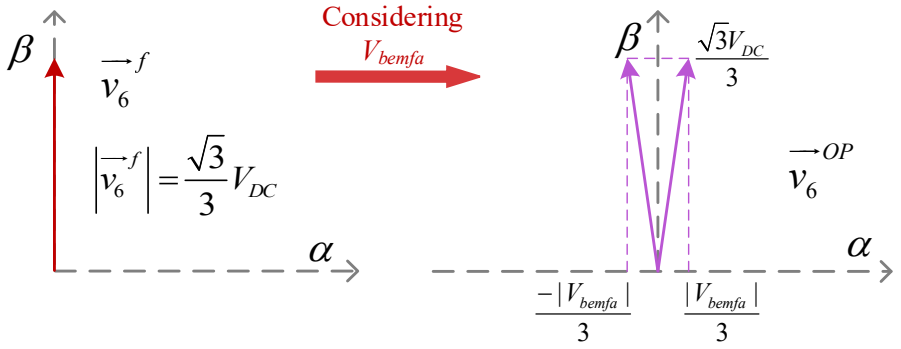


Fig. 6-8. Comparison between simplified post-fault $\vec{v}_6^{f}$ and $\vec{v}_6^{OP}$ considering V_{bemfa}.

Comparing $\vec{v}_6^{OP}$ with $\vec{v}_6^{f}$ in Eq. (6-7), $\vec{v}_6^{OP}$ exhibits a higher amplitude. The ratio between the amplitudes of $\vec{v}_6^{OP}$ and $\vec{v}_6^{f}$ can be described by Eq. (6-9). As the ratio depends on the value of V_{bemfa} and the instantaneous value of V_{DC}, the differences between the practical and simplified post-fault voltage vectors are slight. Hence, V_{bemfa} is removed from the post-fault phase voltages to simplify the design of the fault-tolerant control method at low speeds.

$$\frac{\left|\vec{v}_6^{OP}\right|}{\left|\vec{v}_6^{f}\right|} = \frac{\sqrt{\left(\frac{V_{bemfa}}{3}\right)^2 + \left(\frac{\sqrt{3}V_{DC}}{3}\right)^2}}{\sqrt{\left(\frac{\sqrt{3}V_{DC}}{3}\right)^2}} = \sqrt{1 + \frac{V_{bemfa}^2}{3V_{DC}^2}} \tag{6-9}$$

6.2.3 Influence on Reference Vector Synthesizing

In a 3P2L FOC-based PMSM drive, the outputs of the current regulators and the electrical angle θ_e determine the two adjacent active vectors in each spatial sector and their acting time. The active vectors associate with zero vectors to synthesize the reference vector $\vec{v}_s$ and control the stator flux $\vec{\Psi}_s$ to rotate in a round trace, as shown in Fig. 6-9.

After the occurrence of the fault, although the amplitudes and phases of the inherent voltage vectors have changed, the allocation of vector acting time of each faulty vector still follows the rules of SVPWM under healthy conditions.

Therefore, the amplitude and phase of the reference vector synthesized in every switching

cycle have deviated from the expected vector regulated by the controller. The healthy and faulty reference vectors are concluded in Table 6-3. t_3 is the acting time of zero vectors. t_1 and t_2 are the allocated acting time of the first and second inherent vector, for example, in Sector V, $\overrightarrow{v_1}$ is implemented first and then $\overrightarrow{v_5}$.

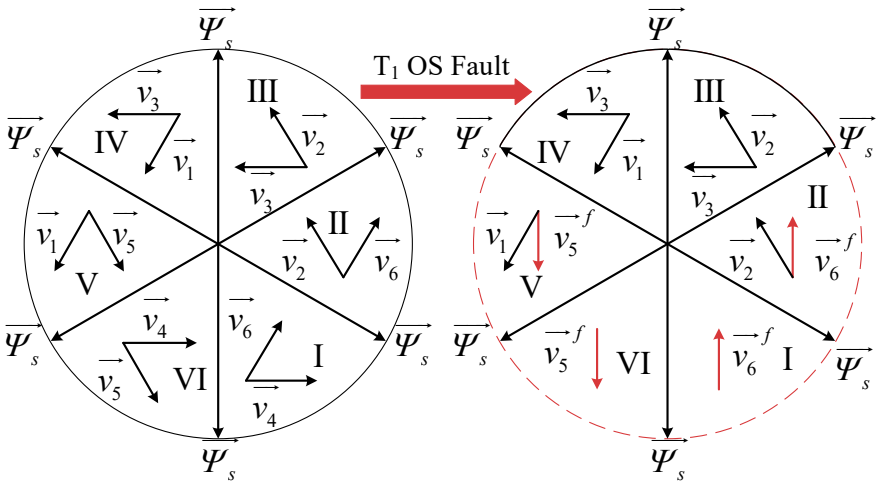


Fig. 6-9. Changes in the amplitudes and phases of the inherent vectors.

TABLE 6-3 Health and Faulty Reference Vectors

Sectors	Healthy Reference Vector	Faulty Reference Vector
I	$\overrightarrow{v_s}=t_1\overrightarrow{v_4}+t_2\overrightarrow{v_6}+t_3(\overrightarrow{v_0}+\overrightarrow{v_7})$	$\overrightarrow{v_s}^f=t_2\overrightarrow{v_6}^f+(t_3+t_1)(\overrightarrow{v_0}+\overrightarrow{v_4}^f+\overrightarrow{v_7})$
II	$\overrightarrow{v_s}=t_1\overrightarrow{v_2}+t_2\overrightarrow{v_6}+t_3(\overrightarrow{v_0}+\overrightarrow{v_7})$	$\overrightarrow{v_s}^f=t_1\overrightarrow{v_2}+t_2\overrightarrow{v_6}^f+t_3(\overrightarrow{v_0}+\overrightarrow{v_7})$
III	$\overrightarrow{v_s}=t_1\overrightarrow{v_2}+t_2\overrightarrow{v_3}+t_3(\overrightarrow{v_0}+\overrightarrow{v_7})$	No changes
IV	$\overrightarrow{v_s}=t_1\overrightarrow{v_1}+t_2\overrightarrow{v_3}+t_3(\overrightarrow{v_0}+\overrightarrow{v_7})$	No changes
V	$\overrightarrow{v_s}=t_1\overrightarrow{v_1}+t_2\overrightarrow{v_5}+t_3(\overrightarrow{v_0}+\overrightarrow{v_7})$	$\overrightarrow{v_s}^f=t_1\overrightarrow{v_1}+t_2\overrightarrow{v_5}^f+t_3(\overrightarrow{v_0}+\overrightarrow{v_7})$
VI	$\overrightarrow{v_s}=t_1\overrightarrow{v_4}+t_2\overrightarrow{v_5}+t_3(\overrightarrow{v_0}+\overrightarrow{v_7})$	$\overrightarrow{v_s}^f=t_2\overrightarrow{v_5}^f+(t_3+t_1)(\overrightarrow{v_0}+\overrightarrow{v_4}^f+\overrightarrow{v_7})$

6.3 A Fault-Tolerant Control Method for the Single Open-Switch Fault at Low Speed

The proposed fault-tolerant method comprises three parts, as shown in Fig. 6-10. Firstly, the vector acting time calculated in SVPWM is reallocated to track the healthy reference vector. Furthermore, the current control references are adapted to the coupled post-fault currents in

the *dq* frame. Moreover, the improved post-fault current prediction model proposed in Chapter 3 is utilized, and the residual errors are employed to improve the post-fault current control transition.

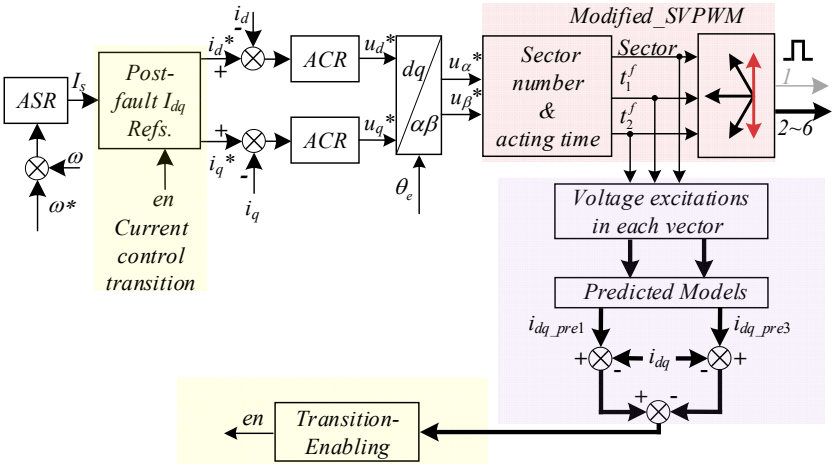


Fig. 6-10. Proposed fault-tolerant control method for single OS fault.

6.3.1 Reallocation of Vector Acting Time

Therefore, the amplitude and phase of the reference vector synthesized in every switching cycle have deviated from the expected vector regulated by the controller.

Although the duty ratios of driving pulses have been maximumly expanded, the speed and torque continue to drop during the *Dropping* stage since most of the acting time has been allocated to $\overrightarrow{v_4}^f$. Besides, the duty ratios are also relatively increased during the *Holding* and *Recovering* stages due to the changes in $\overrightarrow{v_s}$, incurring increased phase currents. Therefore, it is necessary to modify SVPWM under the OS fault to track the healthy reference vectors $\overrightarrow{v_s}$ as much as possible.

As shown in Fig. 6-9 and Table 6-3, the faulty reference vector $\overrightarrow{v_s}^f$ has severely deviated from the healthy one $\overrightarrow{v_s}$ in Sector VI and I, while the fault has comparatively fewer effects in Sector V and Sector II. Hence, the vector acting time needs to be reallocated in different spatial sectors.

When the reference vector rotates in Sector V, $\overrightarrow{v_s}$ and $\overrightarrow{v_s}^f$ can be expressed in Eq. (6-10).

$$\begin{cases} \vec{v_s} = t_1\vec{v_1} + t_2\vec{v_5} = t_1\dfrac{2}{3}V_{DC}e^{j\frac{4}{3}\pi} + t_2\dfrac{2}{3}V_{DC}e^{j-\frac{1}{3}\pi} \\ \vec{v_s}^{f} = t_1^{f}\vec{v_1} + t_2^{f}\vec{v_5}^{f} = t_1^{f}\dfrac{2}{3}V_{DC}e^{j\frac{4}{3}\pi} + t_2^{f}\dfrac{\sqrt{3}}{3}V_{DC}e^{j-\frac{1}{2}\pi} \end{cases} \tag{6-10}$$

t_1^f and t_2^f stand for the re-allocated acting time of each vector. By incorporating $e^{xj}=cosx+jsinx$ into Eq. (6-10):

$$\begin{cases} \vec{v_s} = \dfrac{-V_{DC}(t_1 - t_2)}{3} - \dfrac{\sqrt{3}V_{DC}j(t_1 + t_2)}{3} \\ \vec{v_s}^{f} = \dfrac{-V_{DC}t_1^{f}}{3} - \dfrac{\sqrt{3}V_{DC}j(t_1^{f} + t_2^{f})}{3} \end{cases} \tag{6-11}$$

To track the amplitude and phase of the healthy $\vec{v_s}$, the reallocated t_1^f and t_2^f can be derived from Eq. (6-11) as:

$$\begin{cases} t_1^{f} = t_1 - t_2 \\ t_2^{f} = t_2 + t_2 \end{cases} \tag{6-12}$$

However, Eq. (6-12) does not hold when $\vec{v_s}$ reaches late Sector V in which t_1 is smaller than t_2 according to SVPWM. In late Sector V, although the amplitude of $\vec{v_s}^{f}$ can be equal with $\vec{v_s}$ by setting $t_1^f = t_2 - t_1$ and $t_2^f = 2t_1$, the phases of $\vec{v_s}$ and $\vec{v_s}^{f}$ on the α-axis are opposite. Hence, the optimal solution in late Sector V can be expressed as:

$$\begin{cases} t_1^{f} = t_1 - t_1 = 0 \\ t_2^{f} = t_1 + t_2 \end{cases} \tag{6-13}$$

TABLE 6-4 Acting Time Reallocation in Influenced Sectors

Sectors	t_1^f	t_2^f
Early V ($t_1 > t_2$)	$t_1^f = t_1 - t_2$	$t_2^f = t_2 + t_2$
Late V ($t_1 < t_2$)	$t_1^f = 0$	$t_2^f = t_1 + t_2$
VI & I	$t_1^f = 0$	$t_2^f = t_1 + t_2$
Early II ($t_1 < t_2$)	$t_1^f = 0$	$t_2^f = t_1 + t_2$
Late II ($t_1 > t_2$)	$t_1^f = t_1 - t_2$	$t_2^f = t_2 + t_2$

The same expressions as Eq. (6-12) and Eq. (6-13) remain effective when $\overrightarrow{v_s}$ rotates in late Sector II and early Sector II, respectively. For Sector VI or I, since $\overrightarrow{v_4}^f$ is equivalent to a zero vector, Eq. (6-13) can be applied to allocate all the acting time to the remaining active vector $\overrightarrow{v_5}^f$ or $\overrightarrow{v_6}^f$. Therefore, the acting time reallocation in each influenced spatial sector can be concluded in Table 6-4:

6.3.2 Post-fault Current Control References

As described in Eq. (6-3), i_d^f and i_q^f are coupled through θ_e. Consequently, they can no longer be controlled separately by setting $i_d^* = 0$ and $i_q^* = I_s$, where I_s is the output from the speed regulator. According to the coupling relation presented in Eq. (6-3), the post-fault current references of the healthy and faulty half in a fundamental cycle can be expressed in Eq. (6-14), where I_{peak} stands for the repetitive peak current of the power device, and $2\sqrt{3}/3$ is the coefficient between post-fault phase currents and *dq*-axes currents following Eq. (6-3). Instead of artificially designing a current slope, the relation in Eq. (6-3) is utilized to constrain the maximum phase current.

$$\begin{cases} i_q^* = I_s \\ i_d^* = 0 \end{cases} \xleftrightarrow{Transition} \begin{cases} i_q^{*f} = I_s \\ i_d^{*f} = \min\{i_q^{*f} \tan\theta_e, \dfrac{2\sqrt{3}I_{peak}}{3}\} \end{cases} \tag{6-14}$$

Under the T_1 OS fault, the post-fault system switches between the healthy half and the faulty half in one single fundamental cycle. Consequently, the post-fault current control has to be adapted in the corresponding half. Therefore, it is vital to guarantee an accurate transition to avoid delay or preact. However, the current of the faulty phase is not ideal zero, hence a transition-enabling mechanism is required, which is intrinsically a rapid fault-diagnosis mechanism.

The conventional current prediction model and the post-fault current prediction model proposed in Chapter 3 are utilized to enable the current control transition. When the motor operates in the healthy half of an electrical cycle, the current feedback in the *dq* frame complies with the conventional current prediction model. Consequently, the residual errors, named err_pre1, between the feedback and the predicted current from the conventional model are less than the errors between the feedback and the post-fault model, named err_pre3,

resulting in negative values of ($err\_pre1 - err\_pre3$). In contrast, when the motor operates in the faulty half, err_ pre3 is less than err_ pre1, and leads to positive values of ($err\_pre1 - err\_pre3$).

6.4 Experimental Validation

The experimental validation is implemented on the same setups as in Chapter 5. Since the targeted operation of the proposed fault-tolerant method is at low speeds, the DC bus voltage is turned down to 50 V. In this way, the reallocation of the vector acting time can exhibit more obvious effects.

6.4.1 Validation of Reallocated SVPWM

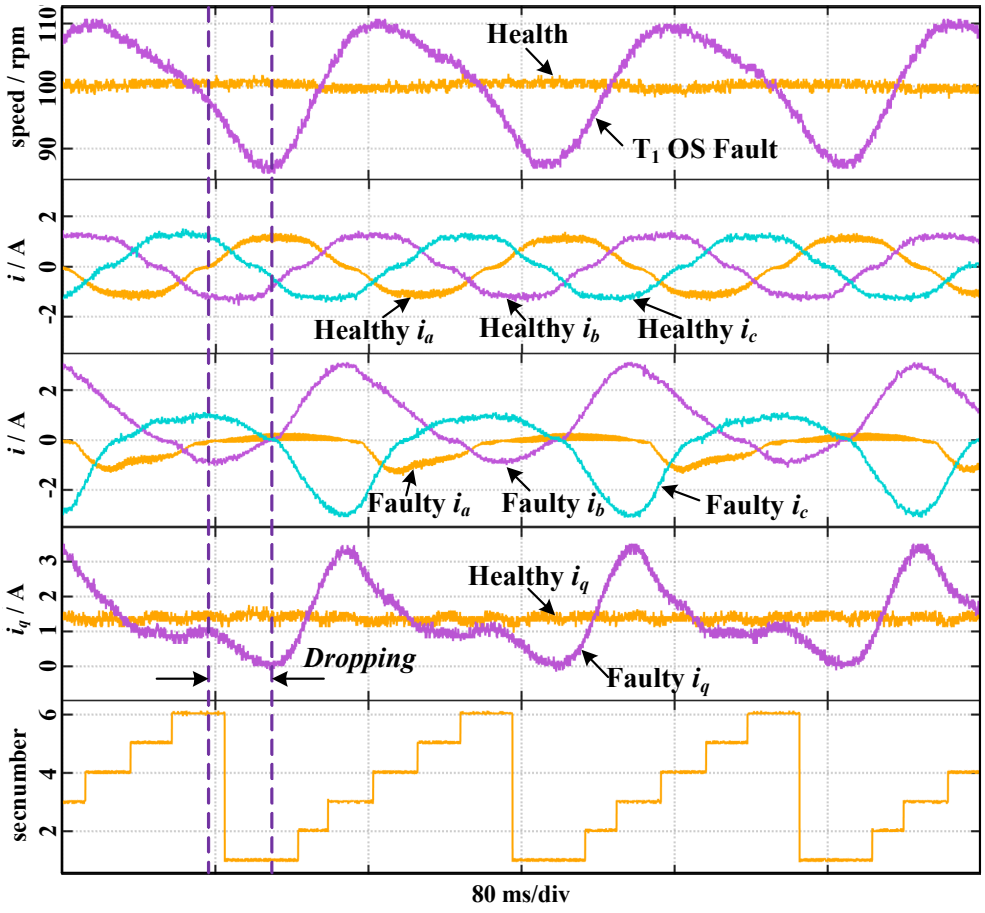


Fig. 6-11. Proposed fault-tolerant control method for single OS fault.

The motor operates at 100 rpm with a 3 N.m constant torque. The speed responses and three-phase currents under the healthy and faulty conditions, i_q under the faulty condition, and the sector number under the fault condition are shown in Fig. 6-11. In experiments, the speed not only decreases during the dropping stage but also has an overshoot due to the controller

regulation during the recovering stage. The dropping stage starts at late Sector VI and ends at late Sector I, which coincides with the analysis in Section II. Since the post-fault current references are not applied, i_b and i_c can converge to zero gradually and do not overlap with the phase range where $\theta_e > 3\pi/2$. Therefore, the negative i_q does not occur during the fault condition.

Fig. 6-12 compares the measurement results of motor speed and the vector acting time with and without the reallocated SVPWM (Re-SVM). the three-phase currents with the Re-SVM are also presented. In experiments, the Re-SVM poses a 41.7% reduction in speed fluctuation. In Fig. 6-12, t_1 is significantly increased during the dropping stage and it is proved in Fig. 6-10 that t_1 is allocated to $\overrightarrow{v_4}^f$ in this stage. Therefore, reallocating the acting time of $\overrightarrow{v_4}^f$ to $\overrightarrow{v_5}^f$ in Sector VI and $\overrightarrow{v_6}^f$ in Sector I can effectively alleviate the speed and torque fluctuations.

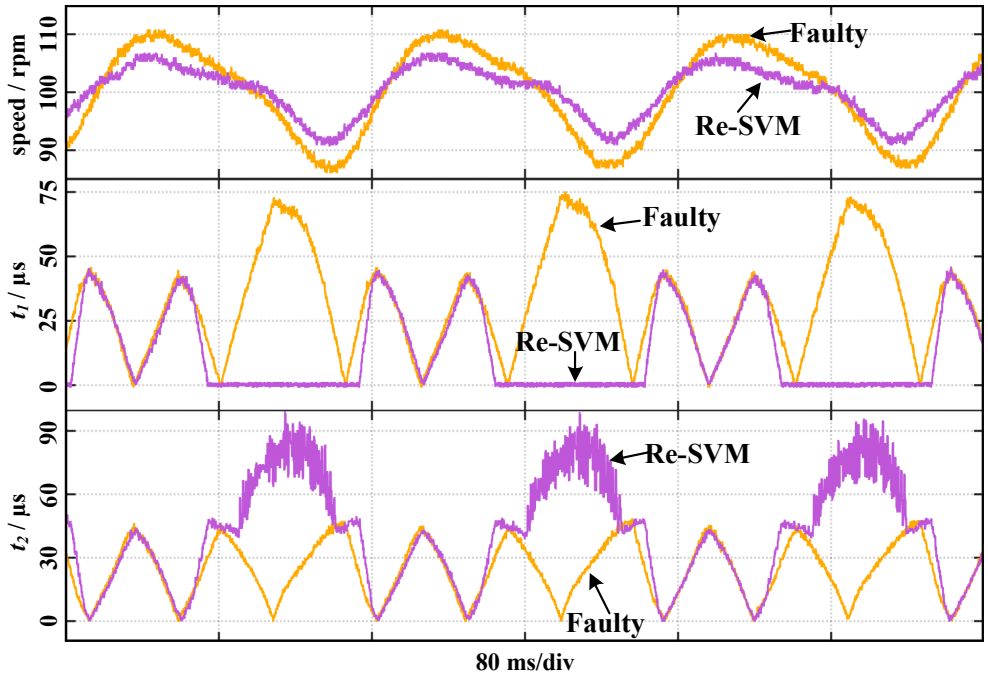


Fig. 6-12. Comparison of motor speed and acting time of vectors.

6.4.2 Validation of Post-fault Current References

By applying the post-fault current references (PF-Ref) solely, the motor speed, three-phase currents, and the currents in the *dq* frame are presented in Fig. 6-13. In. Fig. 6-13, the post-

fault current control references have been adapted to the coupled i_d^f and i_q^f. i_q^f is still required to track the regulated reference of electromagnetic torque, thereby $i_q^{*f}=I_s$.

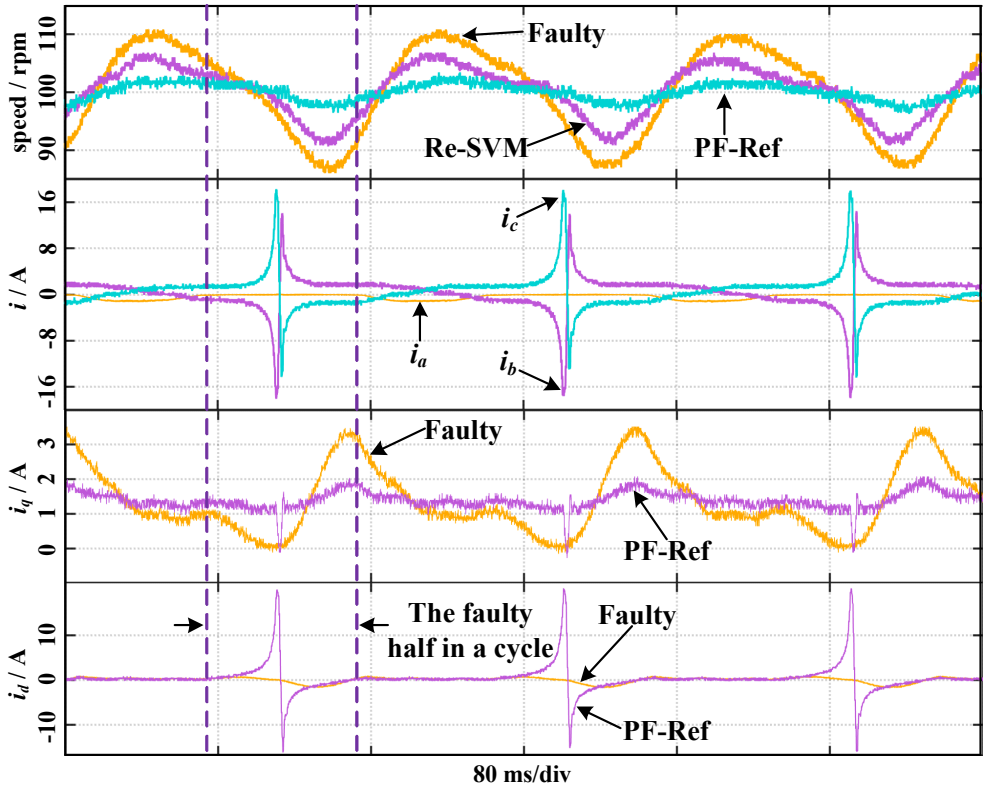


Fig. 6-13. Effects of the post-fault current references on the speed, three-phase currents, and dq-axes currents.

However, i_d^f cannot be controlled as zero because when the motor operates in the faulty half of each post-fault fundamental cycle, θ_e locates around $3\pi/2$ where $cot\,\theta_e$ converges from positive to zero and then increases negatively. Consequently, i_q^f is forced to drop in a $cot\,\theta_e$ pattern if i_d^f is controlled as a constant. Therefore, to maintain a constant i_q^f, i_d^f need to be controlled to increase in a $tan\,\theta_e$ pattern on both sides of $\theta_e = 3\pi/2$, hence incurring the increased phase currents according to (5).

Compared to responses without any tolerant methods, the post-fault current control references bring a 78.3% reduction in the amplitude of speed fluctuation. The i_d reference set in Eq. (6-14) effectively limits the phase current below the continuous collector current of IGBT. Otherwise, the phase current can exceed the peak collector current.

In Figure 6-13, it is observed that the post-fault phase currents exhibit unequal maximum

amplitudes in the positive and negative directions. Specifically, the maximum negative phase B current surpasses the maximum positive phase B current, while the phase C current displays the opposite behavior.

The reason lies in that, under the single OS fault, the extremum values of phase currents occur only at the 3π/2 spatial phase of the rotor electrical angle. At this position, the stator MMF coincides with the rotor flux, resulting in zero electromagnetic torque output, as illustrated in Figure 3-8. At this phase, the phase currents theoretically increase infinitely and are eventually limited by the current protection threshold. As the rotor deviates from the 3π/2 position, the faulty motor begins to restore its torque capability, causing the phase currents to cease their infinitely increasing behavior and gradually return to controlled values.

6.4.3 Overall Performance of the Proposed Fault-Tolerant Method

To verify the overall performance of the proposed fault-tolerant method, the speed, three-phase currents, and i_q are presented in Fig. 6-14. It can be observed the peak of torque drop remains obvious when applying the proposed method and can be explained from two aspects: on the one hand, the peak occurs when $\overrightarrow{v_s}$ rotates to the boundary of Sector VI and Sector I where the direction of the faulty $\overrightarrow{v_s}$ deviates mostly from the healthy $\overrightarrow{v_s}$; On the other hand, the peak of torque drop occurs during the transition from negative i_b to positive i_b, however, the polarity of i_b cannot change suddenly due to the winding inductance. Therefore, the peak of torque drop is inevitable according to Eq. (6-4).

However, the duration of the torque drop has been significantly reduced by the proposed method since the post-fault references have been adapted to the coupled post-fault *dq*-axes currents to keep the post-fault torque output as much as possible until the electric angle rotates beyond $3\pi/2$. Furthermore, the reallocated SVPWM poses the additional torque in sectors influenced by the fault, thus further reducing the speed and torque loss. Finally, the proposed fault-tolerant method reduces the speed fluctuation by 91.7%. In addition, the duration when the motor torque is less than the load torque is reduced by 92.9%.

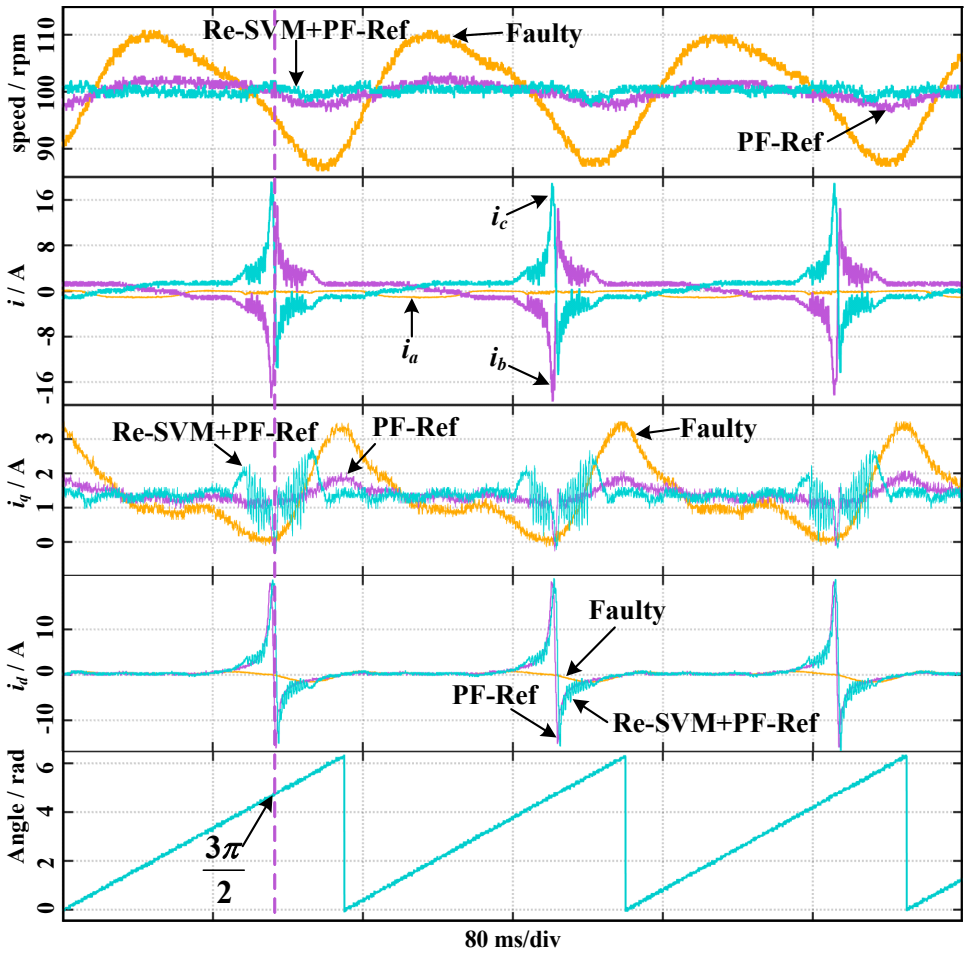


Fig. 6-14. Effects of the proposed fault-tolerant method on the speed, three-phase currents, and i_{dq}.

6.4.4 Evaluation of Post-fault System Derating

The post-fault performance has been significantly improved by the proposed method, but it is also necessary to evaluate the system derating under the post-fault operation.

The post-fault derating is attributed to the increased phase current posed by the post-fault i_d reference i_d^{*f}. The upper limit of i_d^{*f} has been set in accordance with the repetitive peak current I_{peak} of the power device, as described in Eq. (6-14). However, Eq. (6-14) provides the maximum upper limit completely for device protection considerations. In applications, the upper limit of i_d^{*f} can be artificially set lower to restrict the maximum value of phase currents.

Lower limits do not degrade the performance of the fault-tolerant method because, although i_q^f has been coupled with i_d^f by $i_q^f = i_d^f \cot\theta_e$, i_d^f at its maximum point does not influence the

corresponding T_e^f.

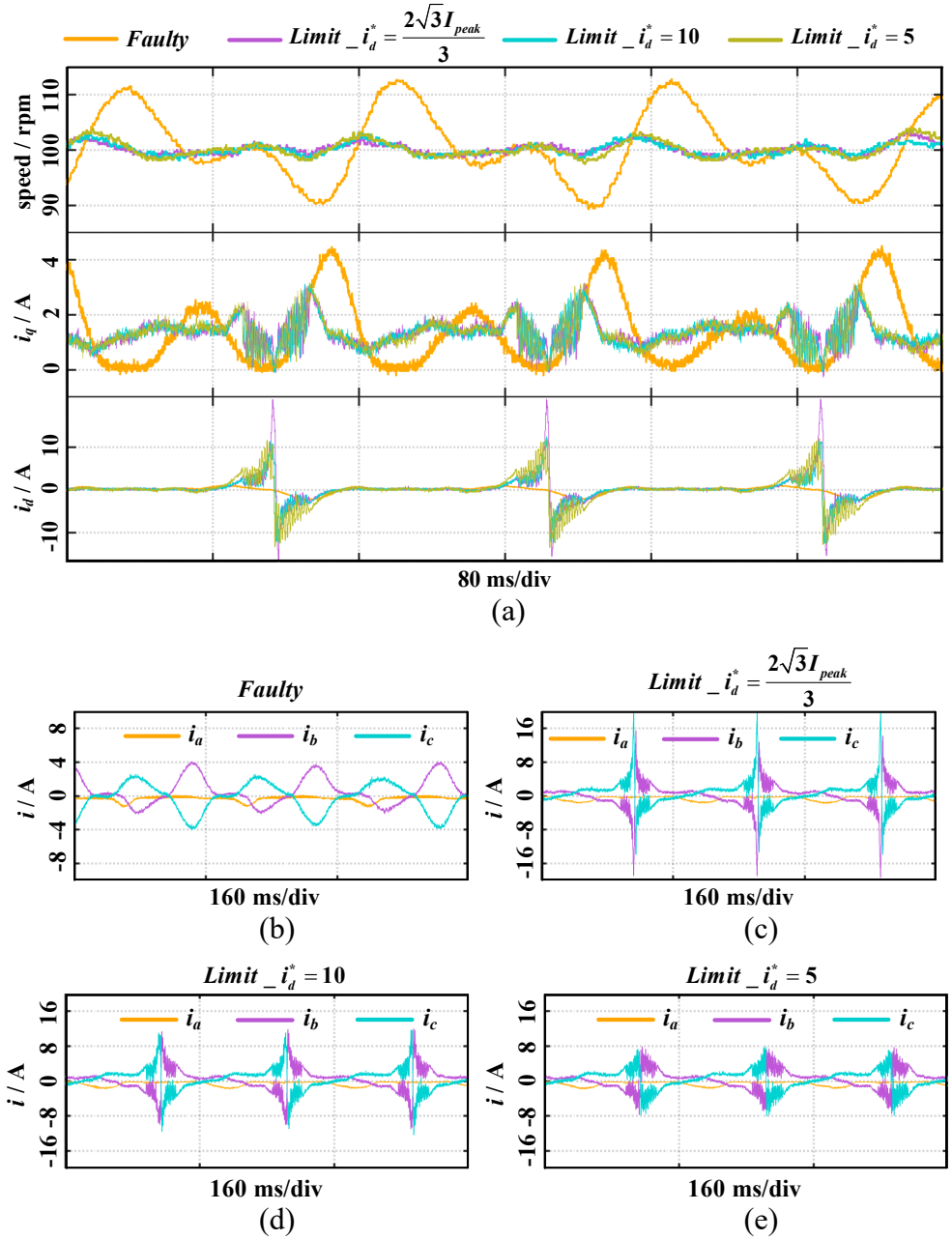


Fig. 6-15. Comparison of post-fault responses with different i_d^{*f} limits: (a) the comparison of motor speed, i_q, and i_d; (b) three-phase currents without tolerant control; (c) three-phase currents with maximum i_d^{*f} limit; (d) three-phase currents with 10A i_d^{*f} limit; (d) three-phase currents with 5A i_d^{*f} limit.

The reason lies in that the maximum i_d^f coincides with $cos\theta_e = 0$ at $\theta_e = 3\pi/2$ during the faulty half of a post-fault fundamental cycle, as presented in Fig. 6-13. However, at the point of

$\theta_e = 3\pi/2$, i_q^f and T_e^f converge to zero according to Eq. (6-4) and Eq. (6-5) because i_b^f cannot be infinite. Therefore, the maximum i_d^f does not influence the corresponding i_q^f and T_e^f, and can be restricted by setting the upper limit of i_d^{*f} lower. Post-fault responses with different upper limits of i_d^{*f} have been tested as shown in Fig. 6-15.

In Fig. 6-15 (a), the change of the i_d^{*f} limit has no obvious effects on the post-fault performance of motor speed and i_q, which verifies the previous analysis. Furthermore, based on the values of phase currents with different i_d^{*f} limits as shown in Fig. 6-15 (b)-(e), the electrical derating of the proposed method can be evaluated. It can be seen from Fig. 6-15 (e) that phase currents can be restricted below 8A by a 5A i_d^{*f} limit. Compared to the phase currents without fault-tolerant control, as shown in Fig. 6-15 (a), the maximum value of phase currents has increased by 100%. Therefore, the post-fault system has to be operated by half of the pre-fault system rating to obtain improved performance from the proposed method. On the other hand, comparing Fig. 6-15 (e) to Fig. 6-15 (c), the value of the current peak can be reduced by 60%, bringing the current peak to a tolerable level for post-fault derating operation. In addition, to cope with the high current peak posed by high du/dt during the switching transient, the current capability of IGBT is generally over-designed in applications, which further guarantees the post-fault derating operation.

6.5 Summary

Aiming at the single OS fault in 3P2L PMSM drives, this chapter proposes an embedded fault-tolerant control method that comprises two modifications on the original control scheme, which are the acting time reallocation of SVPWM and the post-fault current control references stemming from the coupled post-fault model in the *dq* frame. Via experimental validation, the following merits of the proposed fault-tolerant control method are verified: a) the reallocated SVPWM can improve the ability to maintain torque output by tracking the healthy voltage vector maximumly; b) under fault conditions, the designed post-fault current control references can significantly eliminate the torque and speed pulsations but bring increases on power loss and thermal management; (c) the increased current posed by the fault-tolerant method can be suppressed without deteriorating the performance of the fault-tolerant control method.

Compared with existing methods, The novelties and advantages of the proposed method can be summarized as follows:

a) To maximumly track the healthy reference vector, the SVPWM is modified. The faulty voltage vectors are derived, and the acting time of vectors in each sector is reallocated.

b) To comply with the post-fault coupled system, the current control method is redesigned to update the current control references.

c) To avoid mis-activating the fault-tolerant strategy, the residuals between the normal prediction model and the proposed model are employed to improve the periodical current control transition.

In the future, the proposed method can be further improved by considering the thermal effect to reduce the loss under fault-tolerant control. Due to the thermal rise incurred by the increased post-fault phase currents, the rotor flux, phase inductance, and phase resistance will be influenced. The high temperature will demagnetize the rotor PM. As a result, the magnetic saturation of the motor will be reduced, leading to the upward variation of phase inductance. Additionally, the thermal rise will also incur the rise of phase resistance, further interfering with the motor model parameters. Therefore, to achieve the optimal and most efficient fault-tolerant control, it is necessary to take the parameter variations posed by thermal rise into account.

Chapter 7 **Conclusions and Future Work**

7.1 Conclusions

The 3P2L PMSM drive holds a crucial position in a wide range of industries, domestic applications, and the transportation sector. However, due to the rapid proliferation of electrification, a substantial portion of powertrains based on 3P2L PMSM drives is now entering their mid-to-late operational life stages. This poses a significant challenge in terms of functional safety and reliability.

Concurrently, while advanced redundant topologies have garnered interest, they have not yet become the predominant choice in the electric drive market. Replacing the existing 3P2L PMSM drives with their multi-phase counterparts would incur prohibitively high costs and is therefore not a feasible option. Therefore, in order to extend the usage life and ensure the functional safety of the existing powertrains, it is of great significance to develop hardware-free solutions to enhance the reliability and fault-tolerant capability of 3P2L PMSM drives. The main work and contributions of this study can be summarized as follows:

In Chapter 2, an in-depth literature review covering the fault propagation, modelling, diagnosis, and fault-tolerant control of PMSM drives is presented. The review work focuses on explaining the significance of studying the open-circuit fault in PMSM drives and identifying research gaps between the existing studies and the proposed models and methods. Firstly, overcurrent is identified as the primary cause leading to open-circuit faults. Overcurrent phenomena arising from short circuits and device breakdown are separately discussed, and the component failures that result in various overcurrent phenomena and open-circuit faults are cataloged and categorized. Notably, it is observed that OS and OP faults possess distinct post-fault system structures and current conduction paths, yet they have often been treated as the same type of fault. Furthermore, in the review of the fault modelling of open-circuit faults, it is found that the existing post-fault system models do not completely agree with the practical measured results. Furthermore, the diagnostic methods based on state estimation and operating data are reviewed to highlight the merits of model-based methods in the diagnosis of faults in PMSM drives, which have explicit physical significance. Moreover,

the differences between dual three-phase PMSM and 3P2L PMSM drives are analyzed to elucidate why the former is considered a highly promising alternative to the latter. Furthermore, a review of fault-tolerant variants of 3P2L PMSM drives is conducted. Lastly, a review of the existing fault-tolerant control methods designed specifically for addressing open-circuit faults in 3P2L PMSM drives is presented. These existing methods have significantly influenced and informed the developments and advancements made in this study.

In Chapter 3, the back-EMF of the faulty phase is taken into account for the derivation of the post-fault phase voltages under the OP fault. The phase voltages were assumed to hold a constant value during each switching state and were incorporated into the post-fault current prediction. By incorporating the back-EMF into the phase voltages, it is found that the post-fault phase voltages are floating with the rotor electrical angle, and significantly deviate from the assumed constant values especially when the rotor electrical angle approaches $\pi/2$ and $3\pi/2$. A PMSM with a leading out neutral point is configured to validate the derivation, and the measurement results perfectly agree with the derived floating phase voltages in each switching state. Moreover, to further validate the correctness of the derived phase voltages, they are incorporated into the current prediction model. Consequently, the current prediction under the OP fault has been improved to completely match the post-fault current responses. More importantly, the phase voltages under the OP fault are the prerequisite for explaining the remaining current under the OS fault.

In Chapter 4, the remaining current conducting via the free-wheeling diodes in the OS phase is modelled in the scale of the switching period. From the viewpoint of the phenomenon, the remaining current in the OS phase distinguishes the OS fault from the OP fault. Although it has its specific pattern which underlies its relationships with switching states and back-EMF of the faulty phase, it was neglected as it has a relatively negligible value in comparison with the post-fault currents in the remaining healthy phases. Firstly, its conduction conditions are described in each possible switching state. Furthermore, because the OS motor drive has the same connections as the motor drive under the OP fault when the current in the OS phase is not conducting, the phase voltages under the OP fault are incorporated into the conduction conditions. Moreover, the activating switching states of the remaining current in the OS phase are identified according to the relationships between the spatial sector and the rotor electrical angle. Finally, based on the equivalent circuits when the current is conducted in the OS phase, its estimation model is proposed and validated. It is proved that the remaining current has

distinct mechanisms when the motor operates at different speeds and the proposed estimation model can accurately calculate the current in the OS phase in real time.

In Chapter 5, a sampling method is proposed for motor drives to detect the current in the OS phase and is further utilized to classify OS and OP faults. As can be seen from the fault propagation in Chapter 2, OS and OP faults cannot be distinguished when the gating protection or the isolating protection is ineffective. The regular current sampling point aligns with the middle value of current ripples but is inconsistent with the occurrence of the current in the OS phase. Based on the activating switching states revealed in Chapter 4, the current sampling points can be arranged to align with the peak value of the current in the OS phase. Furthermore, based on the sampling results of the proposed sampling method, OS and OP faults can be distinguished from each other by identifying the characteristics of the sampled current, the estimated current from Chapter 4, and their residual errors. Additionally, it is noteworthy that the digitalization errors accumulating in the process of current sampling have a significant impact on the diagnosis and classification of OS and OP faults, as the amplitude of the remaining current in the OS phase is close to the range of digitalization errors. Therefore, to avoid the misdiagnosis posed by the digitalization errors, the proposed method is restricted to be implemented when the estimated current in the OS phase is larger than the threshold associated with the digitalization errors. The proposed diagnosis method can detect and classify OS and OP faults in less than a quarter of the fundament cycle in the random tests at different speeds.

In Chapter 6, an embedded fault-tolerant control method is proposed to alleviate the post-fault speed and torque pulsations. Firstly, the changes in the amplitude and phase of voltage vectors are analyzed. With low inertia and low speeds, the mechanical pulsations are prone to be severe under open-circuit faults. Meanwhile, the differences between OS and OP faults are slight at low speeds where the back-EMF at the faulty phase is far less than the DC bus voltage. Therefore, the back-EMF is temporarily not considered in the changes of voltage vectors. Based on the post-fault voltage vectors, the acting time of the influenced vectors is reallocated in each switching period to recover the lost torque current as much as possible. Furthermore, the current control references are adjusted as the post-fault plant model is no longer coupled in the *dq* frame. The proposed fault-tolerant effectively alleviates the speed and torque pulsations by more than 90 %. However, torque pulsation is inevitable in a 3P2L PMSM drive under the open-circuit fault because of the presence of the phase winding

inductance.

All in all, in terms of the topic of open-circuit faults in 3P2L PMSM drives, this research combines both theoretical analysis and experimental validation to investigate and develop embedded solutions for improving the system performance under open-circuit faults. In this area, the following achievements have been made in this study:

- The post-fault phase voltages and currents model of PMSM drives under the OP fault are clearly described and validated.
- For the first time, the current conducting via the free-wheeling diodes in the OS phase is explicitly described and estimated in real time.
- For the first time, the current in the OS fault can be detected intact by the proposed sampling method, which enables the motor drive to distinguish OS and OP faults.
- The alleviation of post-fault speed and torque pulsations is explored, based on the modification and reconfiguration of the control structure in the 3P2L PMSM drives.

7.2 Future Work

Based on the conclusions above and considering the limitations of the existing work, future research could be carried out in the following areas.

➢ **Condition monitoring of post-fault states of PMSM drives**

In Chapter 4, the association between the post-fault current in the OS phase and inverter switching states is demonstrated. This current is activated directly by the back-EMF of the faulty phase. Importantly, the estimation model establishes a clear relationship between the OS phase current and crucial motor parameters, including rotor position and flux linkage. In the presence of faults, the increased current leads to thermal effects and affects the permanent magnet flux.

Furthermore, post-fault torque variations cause displacement of the rotor position sensor mounted on the rotor shaft. Consequently, rotor-related parameters are more susceptible to fluctuations during open-circuit faults. Using the estimation model for OS phase current, it becomes possible to achieve real-time monitoring of rotor-related

parameters by designing appropriate filters and observers.

- **Dedicated fault-tolerant control methods for PMSM drives under OS and OP faults at high speeds.**

  In Chapter 6, the fault-tolerant control of PMSMs at low speeds under open-circuit faults is studied. It is assumed that both OS and OP faults have similar impacts on the PMSM drive at low speeds. Therefore, the influence of back-EMF on the post-fault phase voltages is temporarily disregarded. It is important to note that this assumption is valid for low-speed operation, but it does not hold true when the motor operates at high speeds, as the back-EMF significantly affects the post-fault voltage vectors.

  To extend the fault-tolerant control scheme to high-speed applications, the post-fault models developed in this study can be further utilized. These models enable the motor drive to separately calculate the amplitude and phase of the post-fault voltage vectors under OS and OP faults. Subsequently, the acting time of these voltage vectors can be reallocated using a similar approach as proposed in this study. This adaptation allows the 3P2L PMSM drive to effectively address open-circuit faults in PMSMs operating at both low and high speeds.

- **Adaptive parameter tuning method for PMSM drives under open-circuit faults.**

  The control references for post-fault current have been adjusted to align with the post-fault plant model. However, it is worth noting that the parameters of PI controllers have not undergone redesign. It has been observed that the post-fault three-phase duty ratios are not fully modulated to their maximum levels, leaving room for controller adjustments to fully harness the post-fault output capacity of the inverter.

  Furthermore, it is important to consider that the inductance parameters are also influenced by faults, causing a deviation from the optimal fit with the pre-fault plant model. Consequently, after identifying the post-fault system status, there is potential for further optimization of the output capacity by redesigning the system parameters to better align with the current post-fault conditions.

- **Alleviating the influences of digitalization errors on the sampling of post-fault current in the OS phase and the diagnosis of OS and OP faults**

In Chapter 5, it becomes evident that digitalization errors play a critical role and have a substantial impact on the classification of OS and OP faults. These errors are inherent in digital sampling systems and affect any method reliant on current sampling. Importantly, when the current in the OS phase falls below the range of digitalization errors, it becomes challenging to distinguish between OS and OP faults accurately.

To enhance the reliability of diagnosis and mitigate the effects of digitalization errors, several potential approaches can be considered:

a) **Development of Self-Calibration Methods**: One approach is to devise self-calibration methods that improve the accuracy of current sampling. These methods can help correct errors and ensure more precise measurements.

b) **Design of Noise-Reduction Filters**: Filters can be designed to minimize noise and interference in current sampling. These filters can help improve the signal-to-noise ratio, enhancing the reliability of fault diagnosis.

c) **Upgrading Current Sensors and Using High-Resolution External ADCs**: Another strategy is to upgrade current sensors to improve their precision. Additionally, employing high-resolution external ADCs can lead to more accurate and detailed current measurements, reducing the impact of digitalization errors.

By implementing these approaches, it becomes possible to improve the accuracy and reliability of fault diagnosis, even in the presence of digitalization errors, ultimately enhancing the overall performance of the diagnostic system.

Appendices

1. Current Sampling Circuit Utilized throughout Experiments

In Chapter 5, the digitalization error accumulated across the current sampling is considered an important factor that affects the proposed diagnostic method. The calculation of the digitalization error has been described in Section 5. 4, and the designed current sampling circuit is presented as follows to further explain the current sampling process implemented throughout the experiments in this study.

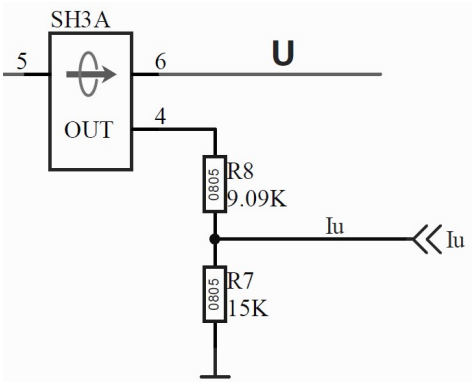


Fig. A-1. Schematic of current signal sensing.

The phase current is sensed by the Hall effect sensor HX 15P from LEM sensors, featuring a nominal measuring current of ± 45 A and 1% accuracy. The output impedance of the current sensing circuit is R8 // R7 = 5.66 kΩ. The output range of HX 15P is ± 4 V and is converted to ± 2.5 V by R8 and R7. Then, the transformed voltage signal is transmitted to an inverting amplifier circuit utilizing OPA2131, as shown in Fig. A-2.

The inverting amplifier circuit is characterized by an input impedance calculated as follows: input impedance = R39 // ((R38 + R37) // R36) = 5.66 kΩ. This circuit also incorporates an *RC* filter with a cutoff frequency of approximately 80 kHz, which is designed for noise-filtering purposes. Importantly, the cutoff frequency is set higher than four times the frequency of current ripples. Specifically, the frequency of current ripples is twice the 10 kHz switching frequency. This strategic choice ensures that the *RC* filter does not interfere with the sampling of current ripples or the accurate measurement of post-fault current under the OS fault condition.

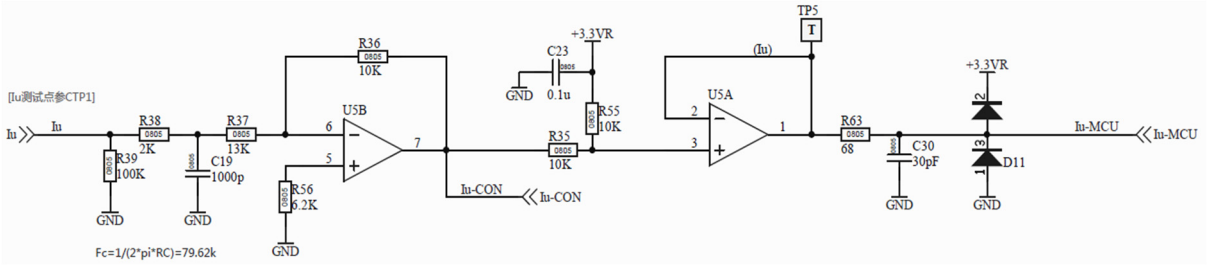


Fig. A-2. Schematic of the inverting amplifier circuit.

Additionally, in the amplifier circuit involving amplifier U5B, the bias resistor is deliberately matched with its input impedance. This careful matching is done to ensure the precision and accuracy of the amplification process.

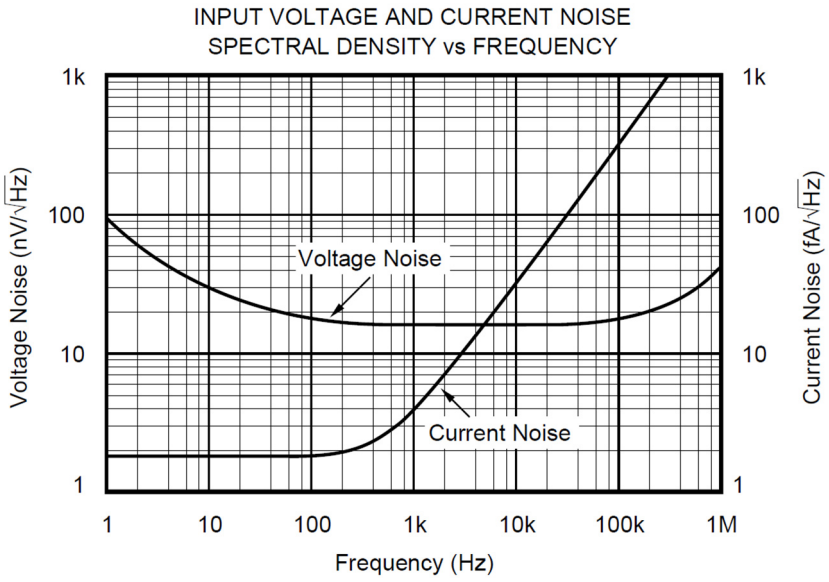


Fig. A-3. Noise density of OPA2131

Furthermore, it is worth noting that the noise present in the amplifier circuit can be safely disregarded because it falls within the limitations of the resolution provided by the 12-bit ADC of DSP. For instance, when examining the voltage noise density of the OPA2131 amplifier as shown in Figure A-3, it results in an approximate noise voltage of 2.1 μV. Importantly, this noise voltage is significantly lower than the resolution of the 12-bit ADC, which is approximately 3.3 mV. As a result, any noise introduced by the amplifier circuit remains within acceptable bounds and can be covered by the ADC voltage resolution.

Consequently, the digitalization error is primarily composed of the sensor accuracy and the ADC resolution, as illustrated in Section 5.4.

2. Functional Code Blocks

(1) PI controller

```
void PID_position_3(double Kp, double Ki, double Kc, double ref, double fb, double
outmax,double * Out_ex,double * Sum)
{
  double Out, error, aw_bc_error;
  error = ref-fb;
  if(speed_ref == 0){
    *Sum = 0;
  }

  Out = *Sum + Kp * error;
  aw_bc_error = outmax - Out;

  if(Out>=outmax){
    if(error>0){
      Out=outmax;
    }
    else{
      *Sum =  *Sum + (Ki * error);
       Out = *Sum + Kp * error;
    }
  }
  else{
     if(Out<-outmax){
         if(error<0){
            Out=-outmax;
         }
         else{
             *Sum = *Sum + (Ki * error);
              Out = *Sum + Kp * error;
         }
      }
        else{
            *Sum = *Sum + (Ki * error);
             Out = *Sum + Kp * error;
       }
  }
  * Out_ex = Out;
}
```

(2) SVPWM

```
U1=U_beta;
U2=0.5*(-U_beta)+0.866025404*U_alpha;
U3=0.5*(-U_beta)-0.866025404*U_alpha;

if(U1 > 0) {A = 1;}
else {A = 0;}

if(U2 > 0) {B = 1;}
else {B = 0;}
```

```
if(U3 > 0) {C = 1;}
else {C = 0;}

N = 4*C + 2*B + A;

switch(N)
{
case 3:
sectornumber = 1;
break;

case 1:
sectornumber = 2;
break;

case 5:
sectornumber = 3;
break;

case 4:
sectornumber = 4;
break;

case 6:
sectornumber = 5;
break;

case 2:
sectornumber = 6;
break;
}

void Time_caculation(double alpha, double beta, double *Tcm1, double *Tcm2, double
*Tcm3, int secnumber, double DC_bus_voltage, double svpwm_carrier_period, double *
t1_per_Ts, double * t2_per_Ts)
{
  double X,Y,Z;
  double Ta,Tb,Tc;
  double T1,T2;
  double T11,T22;

  X = (1.732050807*beta)/DC_bus_voltage;
  Y = (1.5*alpha+0.866025404*beta)/DC_bus_voltage;
  Z = (-1.5*alpha+0.866025404*beta)/DC_bus_voltage;

  switch(secnumber)
  {
    case 1:
      T1 = -Z;
      T2 = X;
    break;

    case 2:
      T1 = Z;
      T2 = Y;
    break;
```

```
  case 3:
    T1 = X;
    T2 = -Y;
  break;

  case 4:
    T1 = -X;
    T2 = Z;
  break;

  case 5:
    T1 = -Y;
    T2 = -Z;
  break;

  case 6:
    T1 = Y;
    T2 = -X;
  break;
}

if((T1+T2)>svpwm_carrier_period)
{
  T11 = T1/(T1+T2);
  T22 = T2/(T1+T2);
}
else
{
  T11 = T1;
  T22 = T2;
}

* t1_per_Ts = T11;
* t2_per_Ts = T22;

Ta = (1-T11-T22)/4;
Tb = Ta+T11/2;
Tc = Tb+T22/2;

switch(secnumber)
{
  case 1:
           *Tcm1 = Ta;
           *Tcm2 = Tb;
           *Tcm3 = Tc;
  break;

  case 2:
           *Tcm1 = Tb;
           *Tcm2 = Ta;
           *Tcm3 = Tc;
  break;

  case 3:
           *Tcm1 = Tc;
           *Tcm2 = Ta;
           *Tcm3 = Tb;
```

```
    break;
    case 4:
             *Tcm1 = Tc;
             *Tcm2 = Tb;
             *Tcm3 = Ta;
    break;

    case 5:
             *Tcm1 = Tb;
             *Tcm2 = Tc;
             *Tcm3 = Ta;
    break;

    case 6:
             *Tcm1 = Ta;
             *Tcm2 = Tc;
             *Tcm3 = Tb;
    break;
  }
}
```

(3) Moving average filter

```
void Queue_Average_f(int N,int n,int Flag,double *Sum,double *queue,double
*Data,double *Average)
{
  double Mid = 0.0;
  int Num;


  Mid = queue[n];
  queue[n]=*Data;
  if(Flag==0)
  {
    *Sum +=queue[n];
    Num=n+1;
  }
  else
  {
    *Sum += queue[n]-Mid;
    Num=N;
  }
  *Average = *Sum/Num;
}
```

3. Collaborations During Ph.D. Study

Throughout the author's doctoral study, active participation in various industrial collaborative projects enhanced the training in the development of PMSM drives and power electronics. Some projects and roles are listed for the evaluation of the training that the author received:

(1) **"High-Dynamic and High-Power Density PMSM Drives Based on GaN FET", Industrial Collaboration Project (Bosch Rexroth, China), Transferred, 2021 to**

2023.

Description: PMSM position servo control based on Zynq 7000. The drive, rated at 5 kW, utilized GaN FETs operating at 100 kHz. The current control calculation was completed in less than 1μs, and the bandwidth of the current loop extended up to 3 kHz.

Role: 1). Implemented the current control, FOC, SVPWM, and current/speed sampling in the Programmable Logic (PL) section of Zynq; 2). Implemented the position control and speed control in the Processing System (PS) section of Zynq; 3). Parameter tuning and bandwidth testing.

(2) **"Dual-Redundant Electromagnetic Actuator", Industrial Collaboration Project (Bosch Rexroth, China), Transferred and Deployed, 2020 to 2022.**

Description: Position servo control of PMSM based on DSP + FPGA and IGBTs. The rated power of the drive was 26 kW, supplied by a DC bus of 270 V.

My Roles: 1). Designed the control scheme of a dual-redundant position servo system for two coupled PMSMs; 2). Designed and implemented the key technology 'redundancy management and self-monitoring mechanisms'; 3). Designed the four-quadrant operation of the motor drive; 4). Implemented the control on the DSP; 5). Implemented the sampling and communications on the FPGA; 6). Designed the control board.

4. Award and Training During Ph.D. Period

Abbreviations

PMSM	Permanent Magnet Synchronous Motor
EV	Electric Vehicle
OP	Open-Phase
OS	Open-Switch
BEV	Battery Electric Vehicle
PHEV	Plug-in Hybrid Electric Vehicle
FCEV	Fuel Cell Electric Vehicle
EU	Europe Union
UK	United Kingdom
US	United States
IM	Induction Motor
DSP	Digital Signal Processor
Back-EMF	Back-Electromagnetic Force
DCB	Direct Copper Bonding
IGBT	Insulated-Gate Bipolar Boding
MPC	Model Predictive Control
UCG	Uncontrolled Generation Current
FFT	Fast Fourier Transform
SVM	Support Vector Machine
PCA	Principle Component Analysis
VSD	Vector Space Decomposition
FOC	Field-Oriented Control
DTC	Direct Torque Control
VSI	Voltage Source Inverter
TRIAC	Triodes AC switch

DC	Direct Current
AC	Alternative Current
ADC	Analog-to-Digital Converter
DAC	Digital-to-Analog Converter
Si	Silicon
SiC	Silicon Carbide
GaN	Gallium Nitride
SVPWM	Space Vector Pulse Width Modulation
Re-SVM	Reallocated SVPWM
PF-Ref	Post-Fault Reference
PWM	Pulse width modulation
PI	Proportional-integral

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