Investigation of Gallium Nitride Based on Power Semiconductor Devices in Polarization Super Junction Technology

By

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accompany is the beautiful landscape in my life and is written into my memory forever.

ABSTRACT

Over the last decade, gallium nitride (GaN) has emerged as an excellent material for the next generation of power devices. GaN transistors, switching losses are very low, thanks to the small parasitic capacitances and switching charges. Device scaling and monolithic integration enable a high-frequency operation, with consequent advantages in terms of miniaturization. For high power/high voltage operation, GaN-based Polarization Super-Junction (PSJ) architectures demonstrate great potential.

The aim of this thesis is devoted to the development of PSJ technology. Detailed analysis of the on-state behaviour of the fabricated Ohmic Gate (OG) and Schottky Gate (SG) PSJ HFETs is presented. Theoretical models for calculating the sheet densities of 2DEG and 2DHG are proposed and calibrated with numerical simulations and experimental results. To calculate the $R_{(on,\ sp)}$ of PSJ HFETs, two different gate structures (Ohmic gate and Schottky gate) are considered herein.

The scaling tendency of power devices enables the emergence of multi-channel PSJ concepts. Therefore, lateral and vertical multi-channel PSJ devices based on practical implementation are also investigated. Presented calculated and simulated results show that both lateral and vertical multi-channel PSJ technologies can be well suited to break the unipolar one-dimensional material limits of GaN by orders of magnitude and achieve an excellent trade-off between $R_{(on,\ sp)}$ and voltage blocking capability provided composition and thickness control can be realised.

A novel multi-polarization channel is applied to realize normally-off and high-performance vertical GaN device devices for low voltage applications based on the multi-channel PSJ and vertical MOSFET concepts. This structure is made with 2DHG introduced to realize the enhancement mode channel instead of p-GaN as in conventional vertical GaN MOSFETs. As the 2DHG depends upon growth conditions, p-type doping activation issues can be overcome. The Mg-doped layer is only used to reduce the short-channel effects, as the 2DHG layer is too thin. Two more 2DEG layers

are formed through AlGaN/GaN/AlGaN/GaN polarization structure, which minimizes the on-state resistance. The calculation results show this novel vertical GaN MOSFET – termed SV GaN FET - has the potential to break the GaN material limit in the trade-off between $R_{(on,\ sp)}$ and breakdown voltage at low voltages. The comprehensive set of development based on the PSJ concept gives a comprehensive overview of next-generation power electronics.

CONTENTS

Chapter 1 INTRODUCTION

1.1 Overview of Power Semiconductor Devices

Energy and the environment are becoming the main elements accompanying technology development. An electronic device driven by a clean, safe, and economical electric source is the first option that satisfies the most demanding of the market. The global energy demand is expected that renewable energy will provide more than one-fourth of global gross power generation from 2016 to 2021 [1]. Renewable energy sources, such as wind energy and solar power, now occupy nearly 33% of the electric power supply, which is the heart of next-generation energy sources. These energy resources benefit from the development of power electronics not only in the increasing efficiency but also from miniaturization and integration. As an essential part of electronic engineering, power electronics utilize solid-state electronics to control or convert electric power [2]. The global power electronics market will achieve USD 39.22 billion by 2025 [3]. Power electronics can manage the fluctuating power between different devices such as transistors and diodes. Simultaneously, power electronics can also be used in power management in the industry.

Power semiconductor devices are recognized as the critical components [4]. Power semiconductor devices used as a switch or rectifier are regarded as the core that accelerates the development of power systems. They can be classified by the terminal number, such as the two-terminal device (diode) and three-terminal devices (power MOSFET, IGBT and HFET).

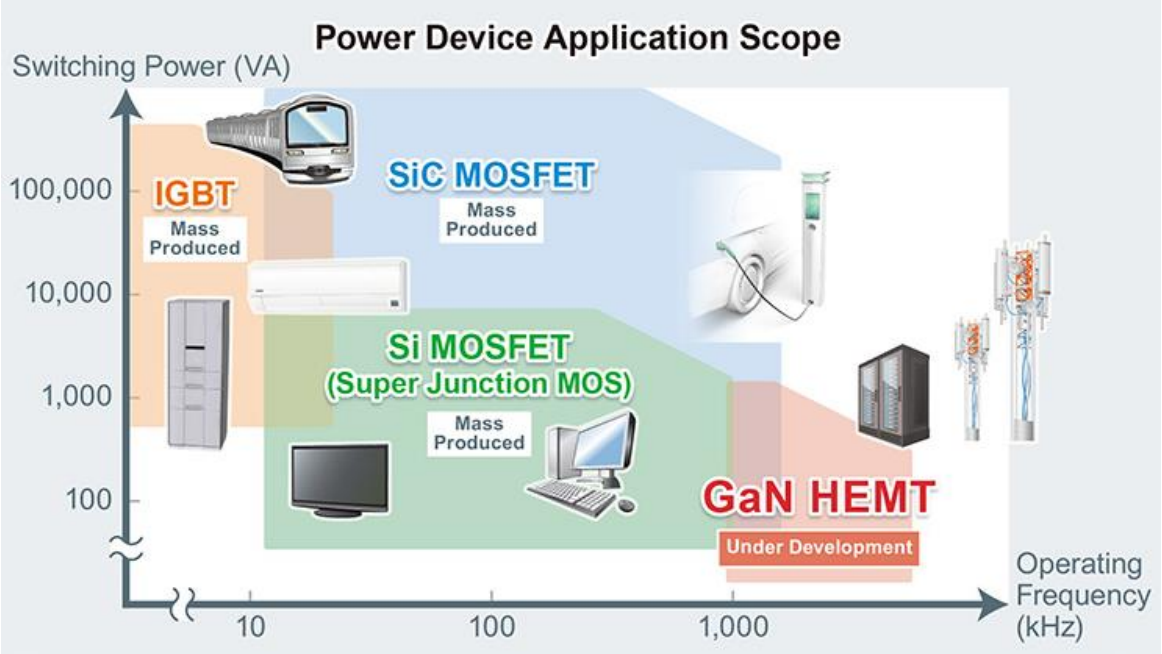

Figure 1.1 Power semiconductor devices and applications [5].

Figure 1.1 demonstrates the representative applications of power semiconductor devices and the trade-off between power magnitude and frequency. An insulated-gate bipolar transistor (IGBT) is mainly used as a high-power switch and seems to fit the requirements of combining the high current capability and power density, especially the invention of clustered insulated-gate bipolar transistor (CIGBT) [6-8]. IGBT has begun to replace conventional bipolar transistors in low-frequency power electronic applications. However, considering the application of power semiconductor devices in the high-frequency operation system, power MOSFET (Si-based) and high-electron-mobility transistor (HEMT) are more competitive. They are majority carrier devices (unipolar power devices); therefore, they can manage the higher operating frequency with ultra-low loss switching, particularly with the emergence of COOL-MOSFET [9-11]. The outstanding performances of Si-based power MOSFET in low voltage fields make it a better choice when the voltage is below 200V. However, it is hard to utilize Si power MOSFET in high voltage areas considering physical limitations.

Material properties have significant impacts on the performance of power semiconductor devices. Silicon (Si) and gallium nitride (GaN) is the most common semiconductor materials. Silicon technology has developed rapidly in recent 30 years and has become relatively mature. It has reached a mark time stage and return on research is less than before. Although Silicon devices are still occupying most of the power electronic product market, the intrinsic material properties limit the improvement of Si power electronic industry.

Compared to Silicon, wide band gap (WBG) material presents advantages in different aspects. Silicon Carbide (SiC) provide promising thermal properties which can be used as a power switch. Diamond supply a more significant band gap and higher thermal conductivity. Gallium Nitride (GaN) has a better performance in the high-frequency operation system.

Properties	**Si**	**SiC**	**GaN**	**Diamond**
Bandgap Energy, E_g(eV)	1.12	3.26	3.45	5.45
Critical Electric Field, E_{crit} (MV/cm)	0.3	2.2	3.3	10
Electron Mobility, μ_n ($cm^2/V \cdot s$)	1500	1000	1500 (Bulk) 2000 (2DEG)	3800
Thermal Conductivity, λ ($W/cm \cdot K$)	1.5	4.5	1.3	22
Electron Saturation Velocity, v_{sat} ($10^6 cm/s$)	10	20	22	27
$M_{RonA} = \varepsilon\mu{E_c}^3$	1	560	2100	9300
$M_{Loss} = \sqrt{\mu}E_c$	1	8.2	14	32

$M_{Area} = \varepsilon\sqrt{\mu}{E_c}^2$	1	68	150	290
$M_{Thermal} = \sigma_{th}/\varepsilon E_c$	1	0.36	0.083	1.5

Table 1.1 Silicon and WBG semiconductors intrinsic material properties [12-14].

Table 1.1 shows the basic intrinsic parameters of some competitive semiconductor materials (Si and WBG) in the market and the relevant functions are used to estimate area-specific on-resistance, total device loss, chip area and thermal capability, respectively. Value of M_{RonA}, M_{Loss}, M_{Area} and $M_{Thermal}$ are inversely proportional to conduction loss refer to area-specific on-resistance, total device loss (conduction and switching loss), chip area size and temperature increment, respectively. All the material properties and factors listed above indicate that diamond is superior to the others. SiC thermal conductivity is better than Si. GaN performance exceeds Si in critical electric field and saturation velocity. Because the band gap is larger than Si in WBG devices, WBG material could offer devices with higher activation energy. They are utilized in high-temperature conditions. The critical electric field could determine device breakdown voltage. Therefore, WBG material could also support power semiconductor devices with a higher blocking capability. High carrier saturation velocity in WBG devices is applied in fast switching and the high-frequency system. Hence, considering the trade-off between the cost of device fabrication and the estimated performance of intrinsic material properties, GaN presents a promising developing prospect among most WBG materials. The properties of GaN devices can support the fabrication of high-efficiency (higher than 99%), 2–6kW-range power converters [15-19]. The switching frequencies of such a converter can reach above 1 MHz and with proper design, the manufacturing frequency of the integration or hybrid GaN-based CMOS can reach 40–75MHz [20-22]. The high-frequency operation can substantially reduce the size of inductors and capacitors. Therefore, it results in a compact GaN-based converter design. GaN devices are the most promising candidate for next-generation power semiconductor devices. Commercial GaN-based power

electronic devices are now available from Transphorm, Panasonic, GaN system, Avogy, Infineon…

1.2 Objectives of this Research Work

Over the past years, GaN has become an excellent material for fabricating power semiconductor devices. GaN-based power devices have excellent performance in the power electronic system compared with Si-based devices. The development of GaN-based power devices, particularly representative high electron mobility transistors (HEMT) and diodes increase energy efficiency in power converters. However, GaN-based power devices also suffer from challenging issues, such as current collapse/dispersion (leading to increased conduction losses during high-frequency switching and under high voltage stress during switching), lack of high voltage blocking capability and lack of avalanche capability (this makes it imperative to operate at voltages lower than the breakdown voltage at all times).

The invention of the Polarization Super Junction (PSJ) concept shows the potential to effectively solve these issues and optimize the trade-off between power devices blocking capability and area-specific on-state resistance ($R_{(on,\ sp)}$). Power Microelectronics Team demonstrated proof of the PSJ concept on diodes and transistors at the University of Sheffield in 2011 (**Figure 1.2**).

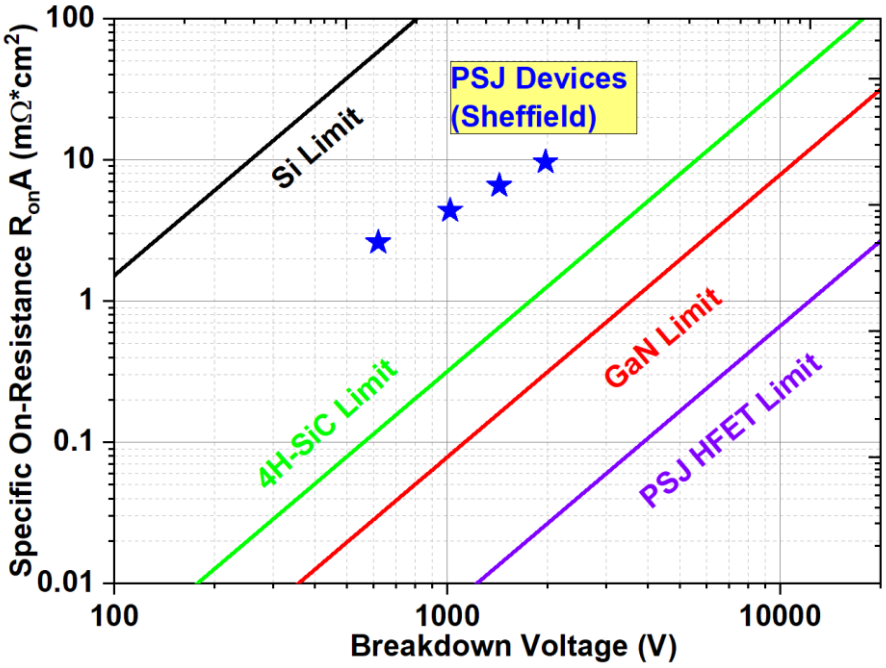

Figure 1.2 Theoretical and reported area-specific on-state resistance vs breakdown voltage.

Based on the PSJ concept, this research work mainly focuses on three parts. The first part evaluates and implements the simulation model for PSJ devices and the fabrication of PSJ devices. The second part is based on the fabricated devices, building the analytical model compared with the simulated and measurement results. In the final piece, multi-channel PSJ concepts extended from the lateral PSJ concept, including lateral and vertical designs, are proposed and demonstrated through the theoretical analysis model.

1.3 Thesis Organization

The thesis is organized as follows:

In Chapter 1, there is a brief overview of WBG power semiconductor devices and an introduction to GaN-based devices. The main challenges are discussed. As a solution, the PSJ technology is also proposed.

Chapter 2 introduces the foundations of GaN material properties and the application of GaN-based High Electron Mobility Transistor (HEMT) technology in power

electronic systems. This chapter also introduces the Polarization Super Junction (PSJ) concept, including the invention of PSJ structures, the formation of 2DEG and 2DHG and the development of PSJ technology.

Chapter 3 presents the Polarization Super Junction (PSJ) simulation and offers a detailed description of the PSJ devices design, mask design, process flow and device fabrication. Measured experimental results of devices fabricated in Sheffield at the wafer level are presented and compared with devices manufactured in Powdec kk.

In Chapter 4, an analysis of the ON-state behaviour of the fabricated Ohmic Gate (OG) and Schottky Gate (SG) PSJ HFETs is demonstrated. Theoretical models for calculating the sheet densities of 2DEG and 2DHG are proposed and calibrated with numerical simulations and experimental results. Two different gate structures (Ohmic gate and Schottky gate) are considered herein.

Chapter 5 demonstrated a detailed theoretical analysis of area-specific on-state resistance ($R_{(on,\ sp)}$) of lateral multi-channel polarisation super-junction (PSJ) technologies at room temperature. Analytical models reported in Chapter 4 have been used to calculate the theoretical limit $R_{(on,\ sp)}$ of PSJ devices. Moreover, calculated, and simulated results of lateral multi-channel PSJ devices based on practical implementation are also analyzed. In addition, the impact of Al composition and AlGaN thicknesses are investigated.

Chapter 6 investigated the theoretical limit of $R_{(on,\ sp)}$ on vertical polarisation super-junction (PSJ) technology. Typical multi-layer PSJ devices with vertical structures for reducing $R_{(on,\ sp)}$ to theoretical limit are investigated and compared with Gallium Nitride (GaN)-based Super Junction (SJ) devices. Theoretical models, demonstrated in Chapter 4, are used to calculate the $R_{(on,\ sp)}$ of PSJ devices and calibrate with numerical simulations. Chapter 6 also proposed a novel multi-polarization channel applied to realize normally-off and high-performance vertical GaN device devices for low voltage applications. This structure is made with 2DHG introduced to realize the

enhancement mode channel instead of p-GaN as conventional vertical GaN MOSFETs. As the 2DHG depends upon growth conditions, p-type doping activation issues can be overcome. The Mg-doped layer is only used to reduce the short-channel effects, as the 2DHG layer is too thin. Two more 2DEG layers are formed through AlGaN/GaN/AlGaN/GaN polarization structure. The calculation results show this novel vertical GaN MOSFET – termed as SV GaN FET - has the potential of breaking the GaN material limit in the trade-off between $R_{(on, sp)}$ and breakdown voltage at low voltages.

Finally, in Chapter 7, a fair summation and future research work will be included in this chapter.

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Chapter 2 GAN-BASED PSJ TECHNOLOGY

In this chapter, initially, **Gallium Nitride (GaN) material properties are first introduced.** Subsequently, the theory of III-V material polarization and the engineering of GaN-based high electron mobility transistor (HEMT) technology will also be explained. Simultaneously, the polarization super-junction (PSJ) concept, to overcome the trade-off between the area-specific on-state resistance ($R_{(on,\,sp)}$) and the blocking capability (BV) of unipolar power devices, is introduced. A brief description of the electrical characterization of power devices is also illustrated in this chapter.

2.1 Gallium Nitride Material Properties

Gallium Nitride (GaN) is a kind of wide bandgap semiconductor material. The power semiconductors industry plays an essential role as a binary III-V direct material that is comprehensively researched. The bandgap of GaN is 3.4eV [23]. Wurtzite is the most critical crystal structure for GaN in the power microelectronics industry. Zinc blende and rock salt are the other two crystal structure of GaN. Thermodynamically, the wurtzite structure is more stable under standard conditions [24, 25].

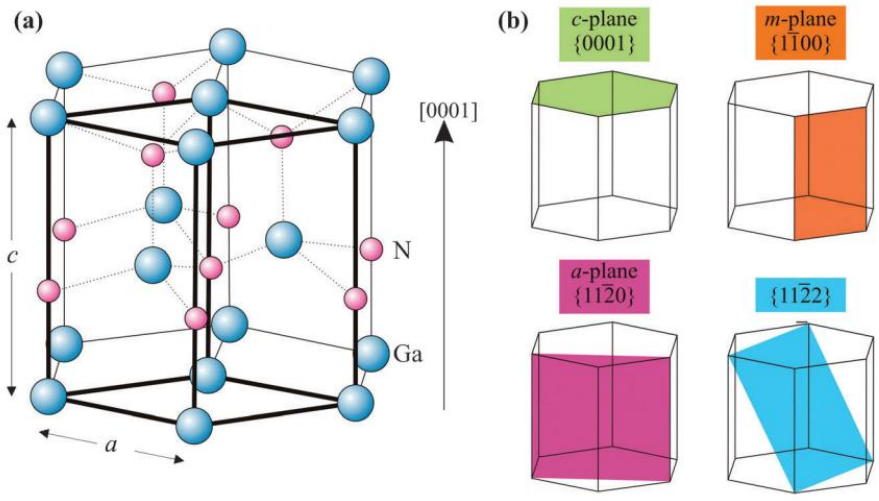


Figure 2.1 Gallium nitride wurtzite structure [26].

As the most common crystal structure, Wurtzite GaN, a hexagonal close-packed (HCP) structure, is used in the fabrication of power semiconductor devices, RF technology and optoelectronic applications, as shown in Figure 2.1. In a compound of GaN, the chemical bond is constructed by Gallium and Nitride atoms. The polarity in electronegativities causes an effective dipole through the atomic bond. The dipole can introduce a net polarization among the macroscopic layers when the crystal has an appropriate symmetry structure. In the cubic crystal structure, the dipole moments from the atomic bond cancel each other when no strain exists. It can cause no net polarization among the crystal. In III-V (GaN) semiconductor materials, the nuclear crystal noncentrosymmetric arrangement exists even under no applied strain, which is a net dipole moment [27, 28]. This phenomenon is called spontaneous polarization (P_{SP}) and the orientation is along the (0001) direction. It is also paralleled to the c-axis, as shown in Figure 2.2.

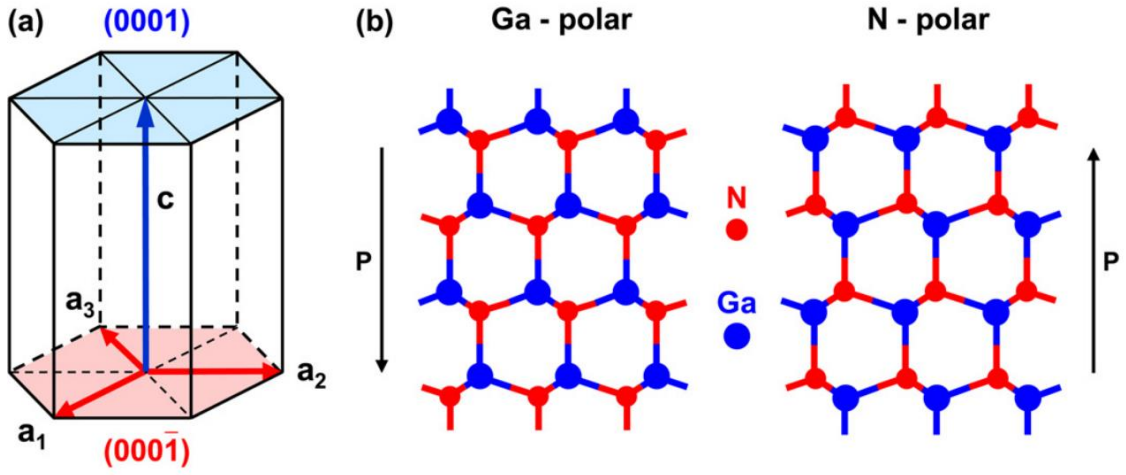


Figure 2.2 Schematics of wurtzite Gallium face Gallium Nitride and Nitride face Gallium Nitride crystal structure with a spontaneous polarization (P_{SP}) [29].

As shown in Figure 2.2, the direction of the spontaneous polarization is related to the crystal growth direction. The layout of the lattice does not have a reverse plane vertically on the c-axis (0001). Because of this, the surfaces have either Gallium or Nitrogen atoms. The surface property is fundamentally important because the surface atom determines the polarity of the polarization charges. These immobile charges

interact and impact the mobile charges on the microscopic structure. The aspect effectively manipulates the design of heterojunction GaN-based devices.

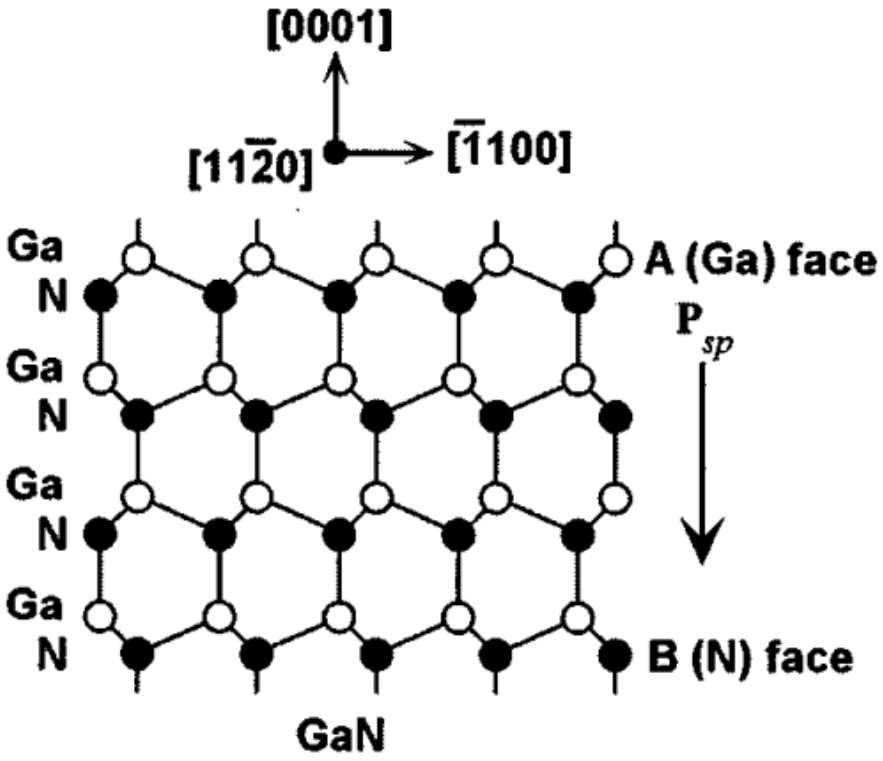


Figure 2.3 Wurtzite Gallium Nitride crystal structure [30].

As discussed previously, GaN wurtzite crystals usually grow in the direction (0001), which leads to a spontaneous and voltage polarization field. Figure 2.3 shows the wurtzite crystal structure and the solid ball represents nitrogen atoms, while hollow balls are gallium atoms when coagulating membranes. As shown in Figure 2.4, the 3D crystal of the wurtzite structure is demarcated with the dashed line.

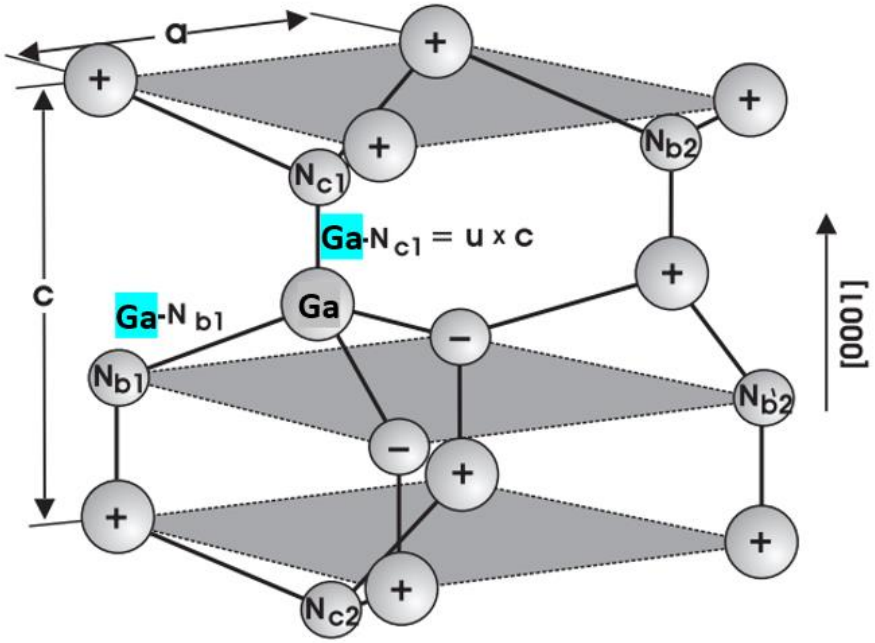


Figure 2.4 Schematic Galium Nitride crystal structure of the unit cell [27].

The lattice constant is labelled as *a,* and along the vertical c-axis is *c* in the basal layer. The bond Ga-N_{c1} is represented by u x c, where u stands for the internal cell constant and is described as $(c/a)^2$. In the ideal situation, $c/a = \sqrt{(8/3)} = 1.633$ [27].

Because of the spontaneous polarization inherent in GaN wurtzite crystal structure, the effective polarization is enhanced when the strain works on the material, which can also occur in growing heterostructures with different lattice constants. The polarization exists when the material is in a strain situation. It is relatively higher in Gallium Nitride material than in other compounds, which concerns piezoelectric polarization. Table 2.1 demonstrated the mechanical and piezoelectric constants and the spontaneous component of the polarization for three binary nitride semiconductors [27, 28, 31].

Symbol	*Unit*	*Value*
$\epsilon_{Al_xGa_{1-x}N}$		$8.5x\epsilon_0 + 8.9(1-x)\epsilon_0$
ϵ_{GaN}		$8.9\epsilon_0$

$E_g(Al_xGa_{1-x}N)$	eV	$E_g(AlN)x + E_g(GaN)(1-x) - 1.3x(1-x)$
$E_g(GaN)$	eV	3.43
σ_{AlGaN}	C/m^2	$\lvert\Delta P_{sp}\rvert + \lvert\Delta P_{pz}\rvert$
$P_{sp}(GaN)$	C/m^2	-0.034
$P_{sp}(Al_xGa_{1-x}N)$	C/m^2	$(-0.09x - 0.034(1-x))$
$P_{pz}(Al_xGa_{1-x}N)$	C/m^2	$2\frac{a(x)-a_0}{a_0}\left(e_{31} - \frac{C_{13}}{C_{33}}e_{33}\right)$
$a(Al_xGa_{1-x}N)$	Å	$a(Al_xGa_{1-x}N) = 3.112x + 3.189(1-x)$
$a_0(GaN)$	Å	3.189
z_{31}	C/m^2	$-0.53x - 0.34(1-x)$
z_{33}	C/m^2	$1.5x + 0.67(1-x)$
C_{13}	Gpa	$127x + 100(1-x)$
C_{33}	Gpa	$382x + 392(1-x)$

Table 2.1 Parameters for III-V Nitride material

z_{31} and z_{33} stand for the piezoelectric coefficient, respectively. C_{13} and C_{33} represent the elastic constants. a and a_0 are the lattice constants of the strained (AlGaN) and base layers (GaN). $\epsilon_{AxlGa(1-x)N}$ and ϵ_{GaN} are dielectric constants of AlGaN and GaN material.

When the Gallium polar layer is in uniform in-plane tensile strain, The cumulative z-ingredient of polarization (along (0001) direction) accompanied by all these bonds reduces, resulting in a sum of the piezoelectric polarization in the direction of the (000-1), as shown Figure 2.5. The same occurs in a nitrogen polarity film, while the net polarization is in the direction (000-1) [32].

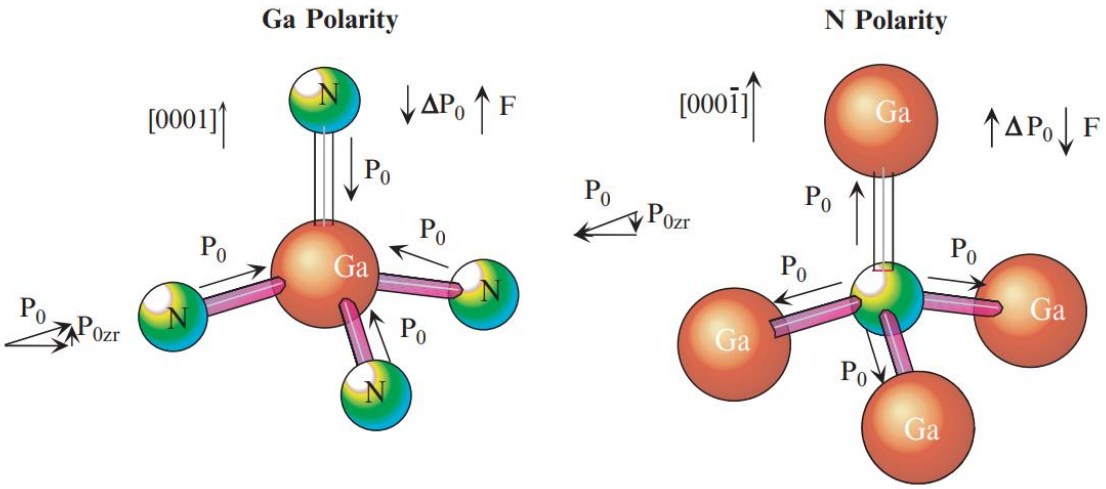


Figure 2.5 3D layout of a Gallium Nitride tetrahedron with Ga/N face when in the tensile strain [32].

Considering the situation of the tetrahedron with the compressive strain, the sum of piezoelectric polarization direction is (0001) in the Gallium-polarity circumstances, and the case of N-polarity along the direction of (000-1) is presented in Figure 2.6 [32].

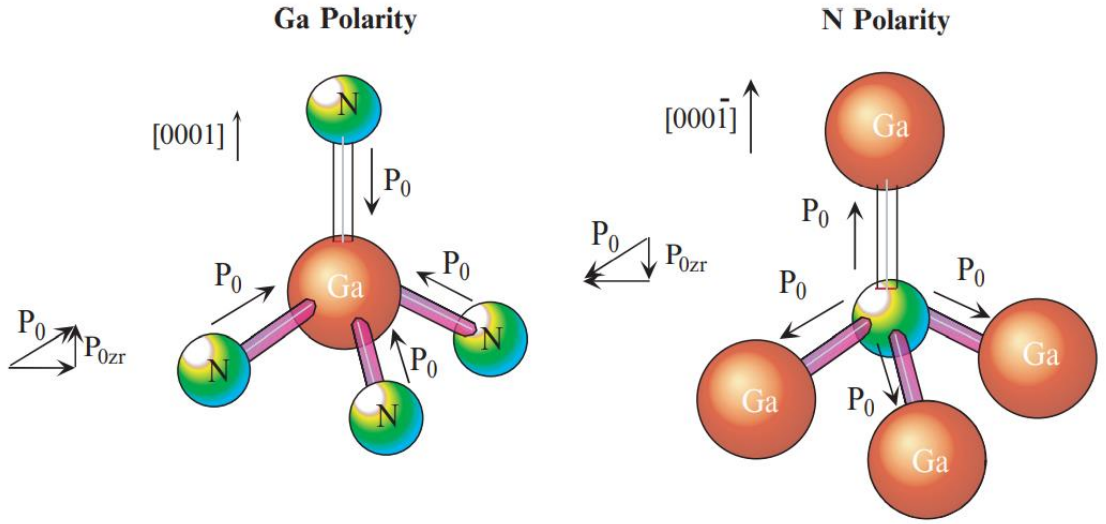


Figure 2.6 3D configuration of a Gallium Nitride tetrahedron with Ga/N face when in the compressive strain [32].

The spontaneous and piezoelectric polarization is essential in the physics and engineering of GaN hetero-structures technology.

2.2 Two-dimensional Electron Gas (2DEG) in GaN-based Heterostructures

The two-dimensional Electron Gas (2DEG) concept first emerged in AlGaN-GaN hetero-structure in 1992 [33]. The idea of hetero-structure based transistors goes more than three decades back when AlGaN/GaN High Electron Mobility Transistors (HEMT) was developed. AlGaN/GaN hetero-structures development was a milestone style in the evolution of III-V group heterogeneous transistors. A conventional single hetero-structure HEMT device typically consists of an undoped AlGaN and a GaN layer. They are sequentially developed on the sapphire substrate. The sheet charge density of the 2DEG at the single AlGaN/GaN hetero-interface can reach 1×10^{13} cm^{-2} level, which is determined by the density of electron states at the quantum well of interface, and the Al concentration.

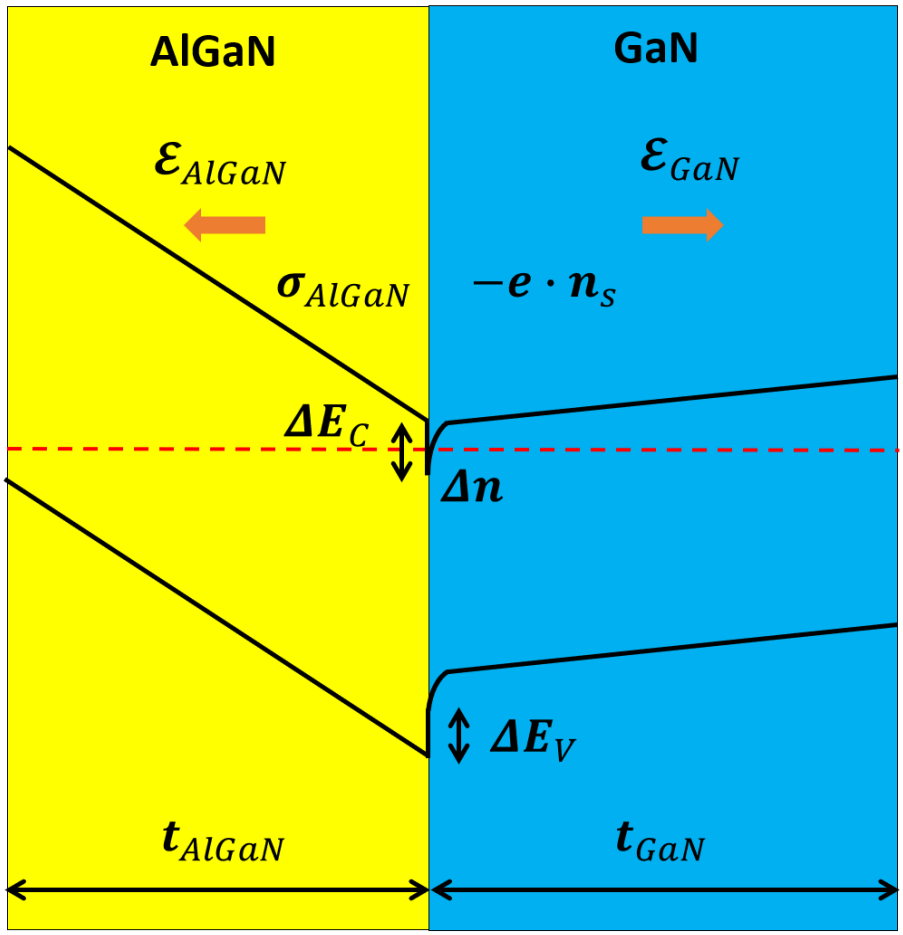


Figure 2.7 Band diagram of a conventional AlGaN–GaN HEMT illustrates the 2DEG quantum well channel [25].

Figure 2.7 presents the band diagram of a typical GaN-based HEMT. ε_{AlGaN} and ε_{GaN} stand for the electric fields in the corresponding layers. σ_{AlGaN} are the surface sheet charge of AlGaN layer. n_s represents the sheet carrier density of 2DEG and 2DHG. Δn is the quantum well of 2DEG. AlGaN has larger bandgap than GaN. The bandgap of AlGaN increases when the Al mole fraction increases. 2DEG is formed because the large bandgap in AlGaN. At the interface of AlGaN/GaN structure, free electrons to diffuse from large bandgap material to the smaller bandgap material. The potential barrier at the interface confines the electrons to the quantum well. At the interface of AlGaN/GaN, the spacer layer separates the 2DEG from any ionized donors. The reduction of Coulomb scattering causes the mobility of 2DEG to be relatively high.

The high density and mobility of 2DEG are a considerable candidate for carriers in the transistor and are critical in developing GaN-based HEMT architecture.

At room temperature, the 2DEG mobility for an $Al_{0.13}Ga_{0.87}N$/GaN heterojunction was 830 cm2/Vs [28], due to the relatively high 2DEG density in AlGaN/GaN structure. The value will monotonically increase and saturate at the mobility around 2600 cm^2/V s with a temperature of 77 K. When further reduce the temperature from 77 to 4.2 K, the mobility of 2DEG will not change much [28]. Through the Van Der Pauw and Hall measurement methods, the sheet carrier density was estimated to be 2.6 x 10^{12} cm^{-2}at 7 K in the unintentionally doped sample [28]. Because of the high mobility, high density and unintentional doping properties in AlGaN/GaN hetero-structures, heterostructure field effect transistors (HFETs) play an essential role in the power semiconductor industry. HEFTs become promising candidates for high voltage, high current and high power electronic systems in microwave frequencies [34-37].

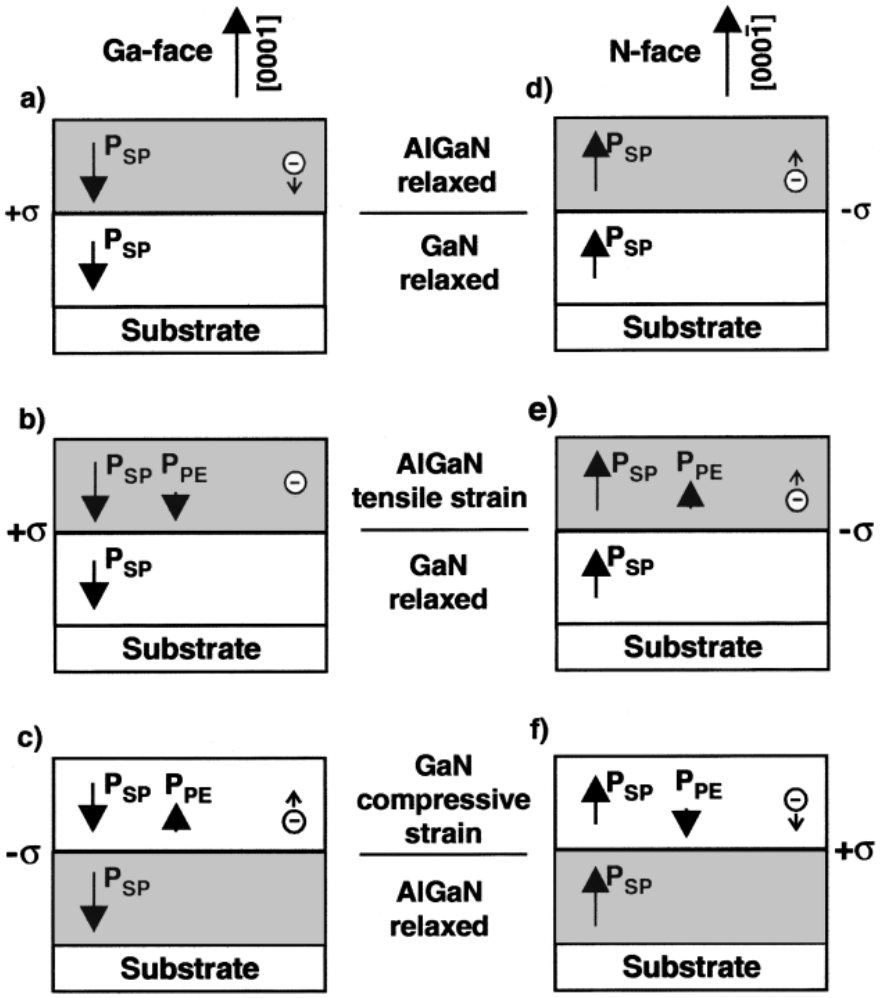


Figure 2.8 Polarization induced sheet charge density and directions of the spontaneous and piezoelectric polarization [28].

As shown in Figure 2.8, in the case of tensile strain, the direction of piezoelectrical polarization is parallel with spontaneous polarization and is antiparallel with the case of compressive strain. If the polarity is flipped from the Ga surface to the N surface in material, the piezoelectric and spontaneous polarization will change its directions. Figure 2.8 illustrates, in Gallium face and Nitride face, the spontaneous and piezoelectric polarization directions under the situation of strain or without strain. As can be inferred, the magnitude of polarization in the two hetero-structure layers would be different and would change abruptly. The gradient of polarization in space is the polarization-induced charge density defined by $\varrho_P = \Delta P$. Therefore, at the top

and bottom interfaces from GaN/AlGaN/GaN hetero-structure, the polarization sheet charge density of 2DEG can be expressed by (2.1)

$$\begin{aligned}\sigma = P(top) - P(bottom) \\ = [P_{SP}(top) + P_{PE}(top)] \\ + [P_{SP}(bottom) + P_{PE}(bottom)]\end{aligned} \quad (2.1)$$

When the induced polarization charge is positive (+σ), free charges will compensate and form the charge balance condition. It is the same electrons that comprise the 2DEG at the interface. Based on the charge neutrality theory, the negative charge will generate a 2-Dimensional Hole Gas (2DHG) at the interface. The magnitude of induced polarization charge density (-σ) is determined by (2.2)

$$|\sigma| = [P_{SP}(AlGaN) + P_{PE}(AlGaN)] - [P_{SP}(GaN)] \quad (2.2)$$

The maximum sheet charge concentration at the interface of a nominally undoped AlGaN/GaN structure is given by (2.3)[28]

$$n_S(x) = \frac{+\sigma(x)}{e} - (\frac{\epsilon_0 \epsilon(x)}{de^2})[e\varphi_b(x) + E_F(x) - \Delta E_C(x) \quad (2.3)$$

Where d stands for the width of the AlGaN layer, $e\Phi_b$ expresses the Schottky barrier of a gate contact, E_F represents the Fermi level concerning GaN conduction band energy, and ΔE_C stands for the conduction band offset at the interface of AlGaN/GaN.

The measured sheet carrier concentrations of undoped AlGaN/GaN hetero-structures is matched well with calculated prediction when the barrier alloy compositions (Al) is between 0.15 and 0.3. The measured 2DEG concentration is close to the maximum concentration to compensate for the board charge caused by polarization. AlGaN/GaN structure containing x= 0.4 and x= 0.15 is not suitable for high-quality HFET. When x = 0.4, the high-crystal grid and thermal mismatch between the GaN buffer and the barrier layer are structural deficiency densities in the high-density AlGaN and the rough interface, thereby limiting the 2DEG migration rate. For x= 0.15,

the offset between AlGaN and GaN layer becomes smaller, resulting in an insufficient limit of 2DEG concentration by induced polarization [28].

I.P. Smorchkova et al. [38] reported the formation of 2DEG in the $Al_{0.27}Ga_{0.73}N$/GaN hetero-junction with a 3nm barrier thickness, which is attributed to the same to the energy level of the surface donor-like states as shown in Figure 2.9.

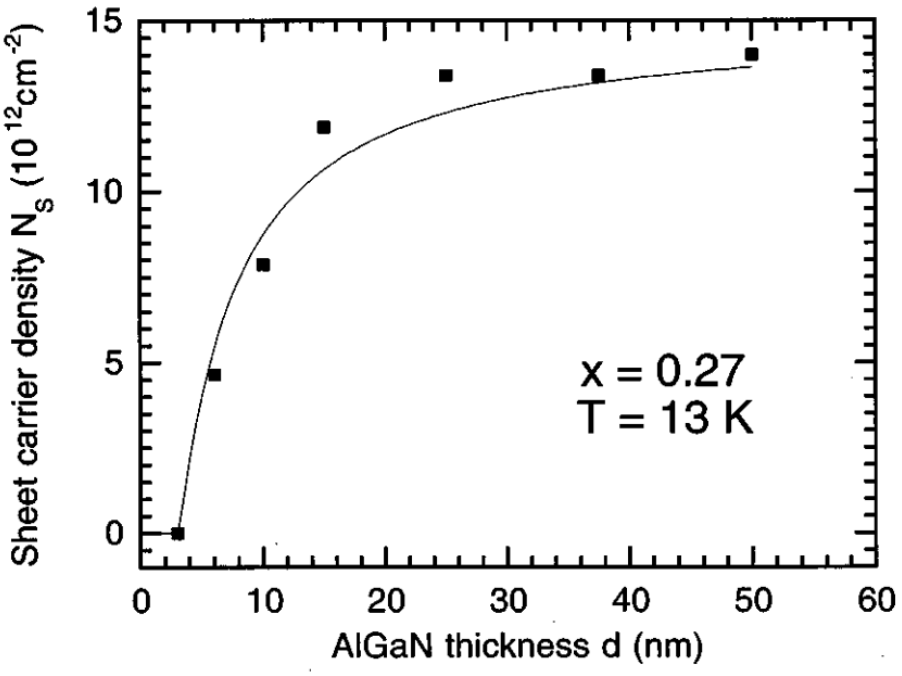


Figure 2.9 2DEG sheet charge density vs AlGaN barrier width [38].

When further increases in the barrier width, the density of 2DEG increases. It will saturate at the value close to the polarization-induced charge density in the AlGaN layer.

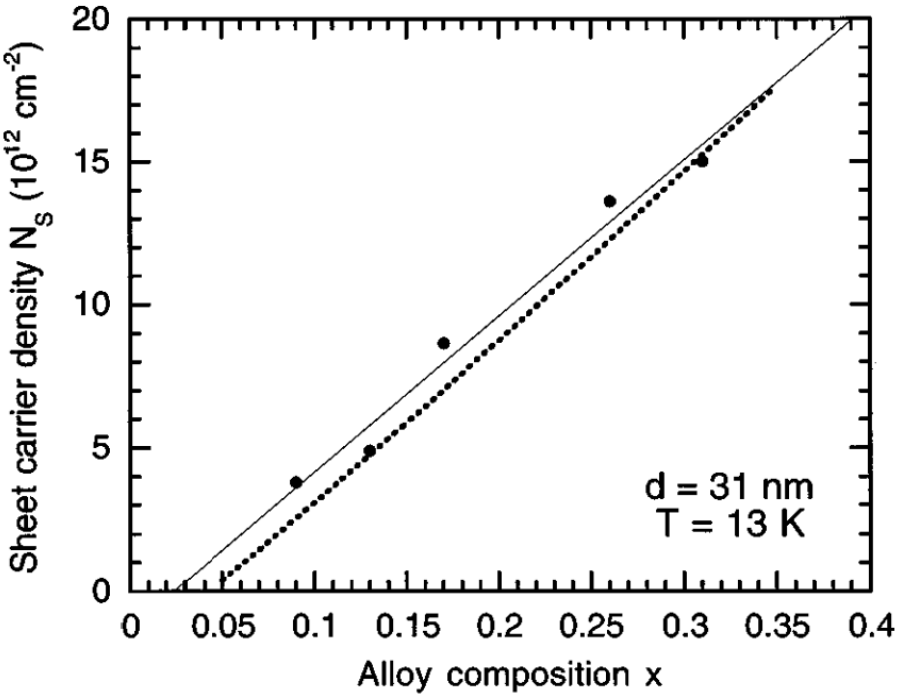


Figure 2.10 2DEG sheet charge density in the $Al_xGa_{1-x}N$/GaN hetero-junction vs AlGaN composition x [38].

As demonstrated in Figure 2.10, in the linear region ($0.09 < x < 0.31$), the increasing rate of 2DEG density refers to Al content in AlGaN barrier is approximate to $dN_s/dx = 5.45 \times 10^{13}$ cm^{-2}.

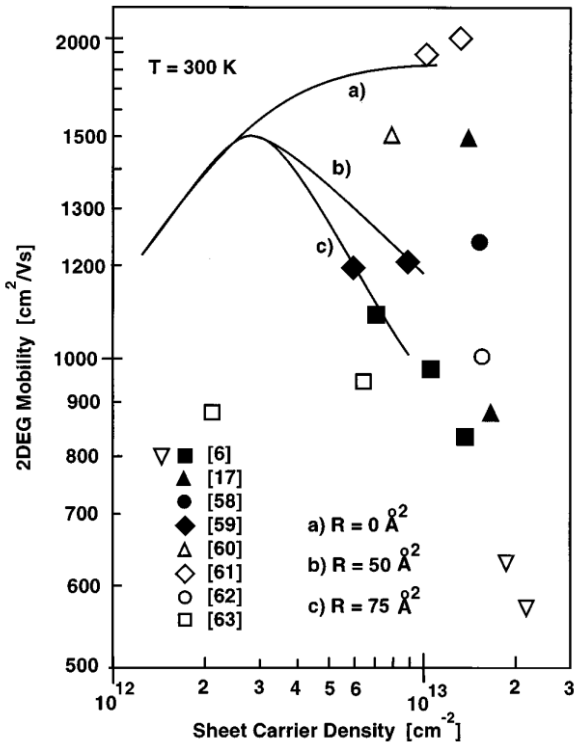


Figure 2.11 2DEG sheet charge density in the $Al_xGa_{1-x}N$/GaN hetero-junction vs mobility [28].

As shown in Figure 2.11, at low-temperature condition, 2DEG mobility decreases with the Al mole fraction and AlGaN barrier thickness increases. The experimental results are because of the possible changes in disordered alloy scattering or interface roughness scattering, which increase considerably with 2DEG density [38].

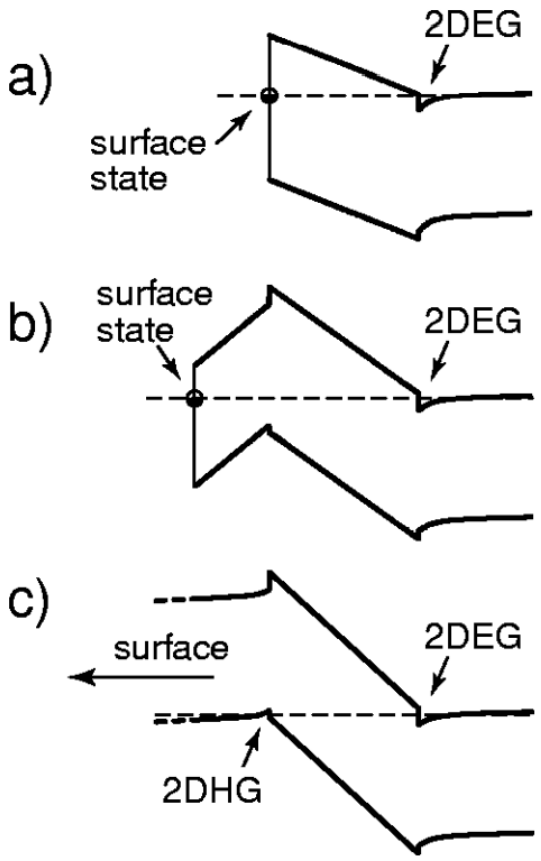


Figure 2.12 Band diagrams of three heterostructures: (a) AlGaN/GaN hetero-junction, (b) GaN/AlGaN/GaN heterojunction with the thin GaN cap layer, and (c) GaN/AlGaN/GaN with heterojunction sufficiently thick GaN cap layer [39].

The simulation also proves the existence of a 2DHG at the upper interface of GaN/AlGaN/GaN structures when the GaN cap layer is thick enough. GaN cap layers, as demonstrated in Figure 2.12.

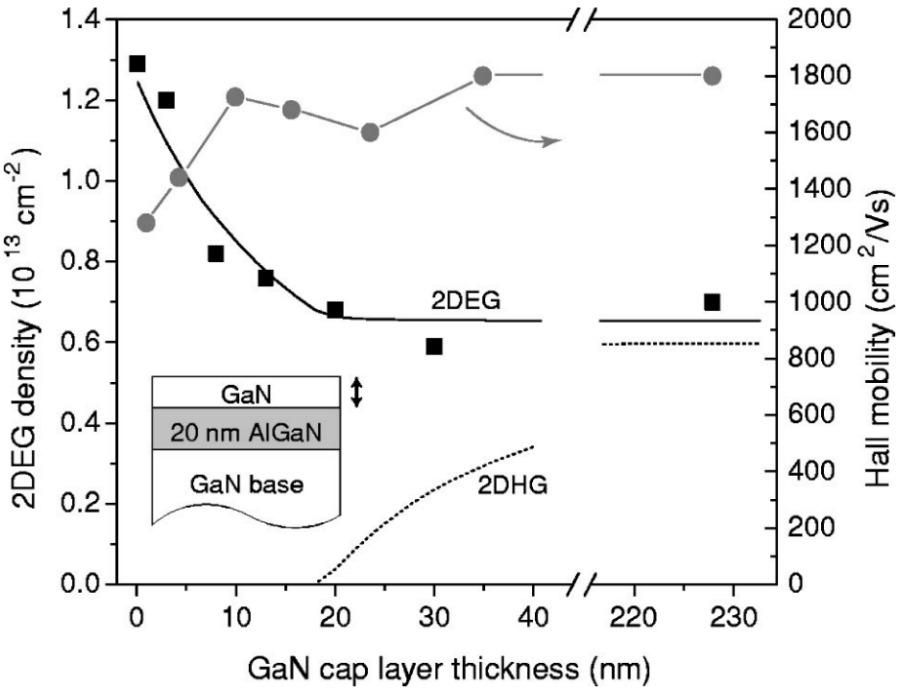


Figure 2.13 The GaN cap layer thickness vs sheet carrier density and Hall mobility of a GaN/AlGaN/GaN heterojunction structure with a fixed AlGaN layer thickness of 20 nm [39].

As shown in Figure 2.13, the existence of the GaN cap layer causes a decrease in the sheet carrier density from 1.3×10^{13} cm^{-2} (without GaN cap) to 6×10^{12} cm^{-2} (with 30 nm GaN cap).

It proves that the 2DEG sheet charge density strongly depends on the thickness of the AlGaN layer and the Al concentration of AlGaN. The 2DEG sheet charge density increases proportionally with the thickness of the AlGaN layer. When the thickness is beyond a critical value, the tensile strain in the AlGaN layer become relax because of the cracking. The piezoelectric components reduce in this situation and can eventually diminish the 2DEG altogether. Al concentration can determine the thickness of the strain in the AlGaN layer. These two elements are inversely proportional.

2.3 AlGaN/GaN-based HEMTs

A high electron mobility transistor is a field-effect transistor. It is built on the theory of hetero-structure formed from different materials with different bandgaps. Usually,

2DEG is applied as the carrier in HEMT. The HEMT is a necessary field-effect transistor widely used in most power electron systems. A typical AlGaN/GaN HEMT has epitaxially grown AlGaN on GaN, 2DEG form at the interface with high sheet density and mobility. The 2DEG serves as the transistor channel.

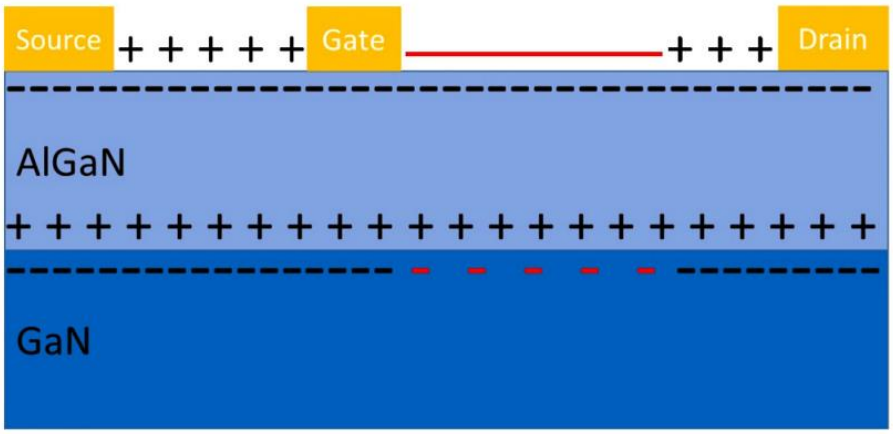


Figure 2.14 Schematic cross-section of the conventional AlGaN/GaN HEMT [25].

As depicted in Figure 2.14, the schematic cross-section of a typical conventional GaN-based HEMT is demonstrated. Devices can be grown on a non-native substrate, such as Si, SiC or Sapphire. GaN or AlN is grown as a buffer layer refers to the nucleation layer to realize wurtzite GaN can be grown on the non-native substrate mentioned above. Hydride Vapor Phase Epitaxy (HVPE), Metal-Organic Chemical Vapor Deposition (MOCVD) and Molecular Beam Epitaxy (MBE) are some typical methods which is introduced for GaN/ AlGaN epitaxial growth. The gate electrode is Schottky type in a conventional AlGaN/GaN HEMT. The drain and source electrodes are ohmic contacts to 2DEG. As shown in Figure 2.14, 2DEG creates the device channel from which current flow from source to drain as a normally-on device. In the cross-section of the conventional GaN HEMT device, the Schottky gate could manage the device on and off, compared with an ohmic contact applied on the source and drain. Usually, the Gate material is Ni or Pt, and the Source and Drain material are Ti or Al. When a negative voltage is applied to the gate, the conduction path is disrupted or cut off since the 2DEG under the gate region is depleted, as demonstrated in Figure 2.15.

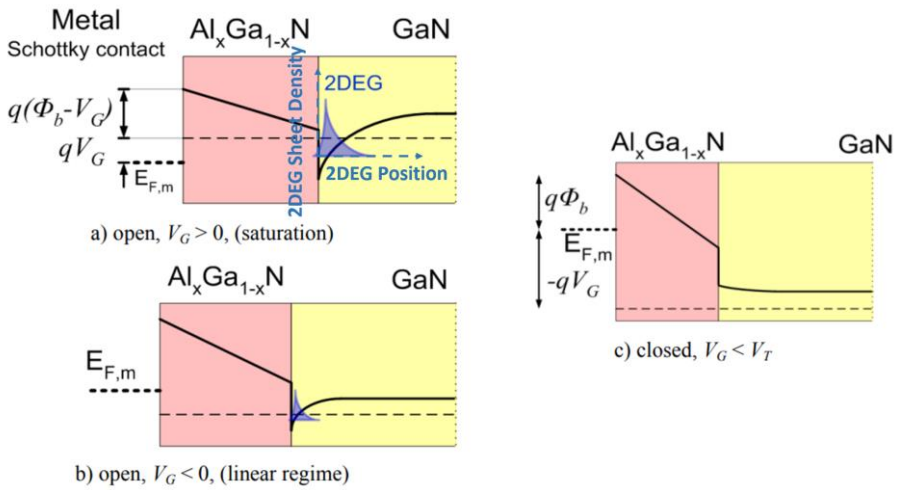


Figure 2.15 Energy band diagram for varying Gate Voltage (V_G) (a) $V_G > 0$ (b) $V_G < 0$ (c) $V_G < V_T$ [40].

Figure 2.15 shows the turn on and off of the HEMT channel by varying the gate voltage V_G with the corresponding energy band diagram. The blue dotted line is the Fermi level. The solid line stands for the conduction band. When a positive or negative gate voltage is applied on the structure, the Schottky barrier (Φ_b) will reduce or increase. V_T refers to the threshold voltage of the HEMT.

The characteristics of an ideal power semiconductor device should conduct large currents with relatively lower voltage drop when the device is on-state. It should also be operated with extensive blocking capability and minimal off-state leakage current. Devices should switch instantly when triggered on to off or vice versa, minimising losses.

In the conventional GaN-based HEMT, the static electrical characteristics depend on 2DEG density/mobility and peak electron saturation velocity. The charge concentration (n_s) at the AlGaN/GaN interface under the condition with a gate bias (V_g) could be expressed as (2.4)[32]

$$n_S = \frac{\varepsilon_{AlGaN}}{q(d + \Delta d)}(V_g - V_{th}) \qquad (2.4)$$

Where q stands for the charge of the electron, d represents the total thickness of the AlGaN layer, Δd is typically around 2–4 nm for GaN and stands for the location of the peak density of the 2DEG from the heterointerface, ε_{AlGaN} is the dielectric constant of the AlGaN layer and V_{th} represents the threshold voltage, as shown in (2.5)

$$V_{th} = \phi_b - \frac{1}{q}\Delta E_C - V_{p2} - \frac{qd}{\varepsilon_{AlGaN}}(n_p + N_B W_d) \qquad (2.5)$$

Where Φ_b is height of the Schottky barrier. ΔE_c stands for the conduction band discontinuity. $V_{p2} = qN_d(d_d)^2/2\varepsilon_2$ and N_d represent the barrier layer donor density. d_d representes barrier layer thickness, n_p is the polarization charge at the interface. The charge determines $N_B W_d$ due to bulk doping [32].

In ideal conditions, V_{th} stands for the threshold voltage. However, in the practical situation, the channel's current and free sheet charge are plotted against the gate voltage. The extrapolation of the linear region to zero charges will determine the threshold voltage.

As in HFETs, Drain Current (I_{DS}) and Drain Voltage (V_{DS}) association, also known as transistor output characteristics, has two central regions: the linear and saturation. The model presented by H. Morkoc et al. [32] has an approach of a two-piece model and considers an abrupt transition from a constant mobility regime (linear region) to the continual velocity regime (saturation region)

In the linear region, the drain current (I_d) is illustrated as (2.6)[32]

$$I_d = \frac{\mu_{2DEG} Z}{L}\frac{\varepsilon_{AlGaN}}{d}\left[(V_g - V_{th})V_d - \frac{{V_d}^2}{2}\right] \qquad (2.6)$$

Where μ_{2DEG} represents the 2DEG mobility and Z is the gate width. The on-state resistance is evaluated by differentiating I_d concerning V_d in this regime.

The current is saturated when the drain voltage increases and exceeds its critical value, hence causing the velocity to saturate, and could be expressed as (2.7)

$$I_d = qZv_{sat}n_s = \frac{\varepsilon_{AlGaN}Zv_{sat}}{d}\left[\left(V_g - V_{th}\right) - V_{dss}\right] \quad (2.7)$$

Where v_{sat} stands for the saturation velocity and V_{dss} is the saturation drain voltage.

In a bulk material, the critical electric field is defined by the avalanche breakdown. The value is proportional to the square of the energy bandgap ($E_{br} \propto (E_g)^2$). The breakdown voltage is proportion to the fourth degree of the bandgap. The avalanche breakdown voltage is reduced at higher dopant concentrations. The relationship between material avalanche breakdown voltage and doping concentration is $V_B \propto (N_D)^{-0.75}$. The expression for device avalanche breakdown can be shown as (2.8), where E_g is the bandgap of n-type material and N_D stands for doping concentration [32]:

$$V_B = 23.6E_g^4(eV)\left(\frac{N_D(cm^{-3})}{10^{16}}\right)^{-0.75} \quad (2.8)$$

Since GaN-based HEMTs/HFETs are mostly planar devices, surfaces play a significant role in the devices blocking capability. Therefore, the breakdown voltage values would differ from those predicted by the above equation. The field is not mature. The passivation may work concerning optimising the surface state. Moreover, the drain breakdown voltage is complicated and is mainly depends on the gate leakage currents (attributed to surface states). In practice, the breakdown voltage is usually defined as when the leakage current exceeds 1mA/mm.

Electric field management has been a vital issue for conventional GaN-based HFETs, to enhance the V_B to the theoretical limit. Figure 2.16 presents the cross-section of the traditional HFET with a Schottky-type gate. The electric field is crowded at the gate edge in the absence of a field plate, as shown in Figure 2.16(b), because positive polarization charges form at the AlGaN/GaN interface [41].

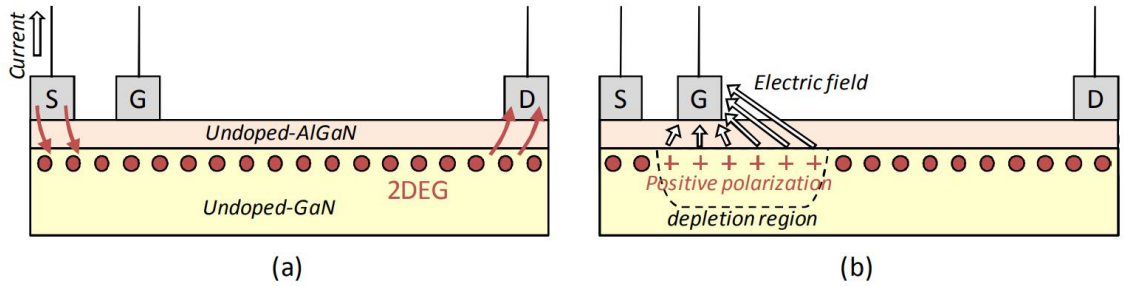


Figure 2.16 Cross-section of the conventional HFET in (a) forward conduction (b) OFF-state [41].

Generally, Field Plate (FP) technologies are introduced to suppress the crowding of 2DEG reducing the peak of electric field. FP Technologies enhance GaN-based HEMTs V_B by modifying the electric field distribution, reducing gate leakage current, and mitigating hot electron generation, as illustrated in Figure 2.17 [42-44].

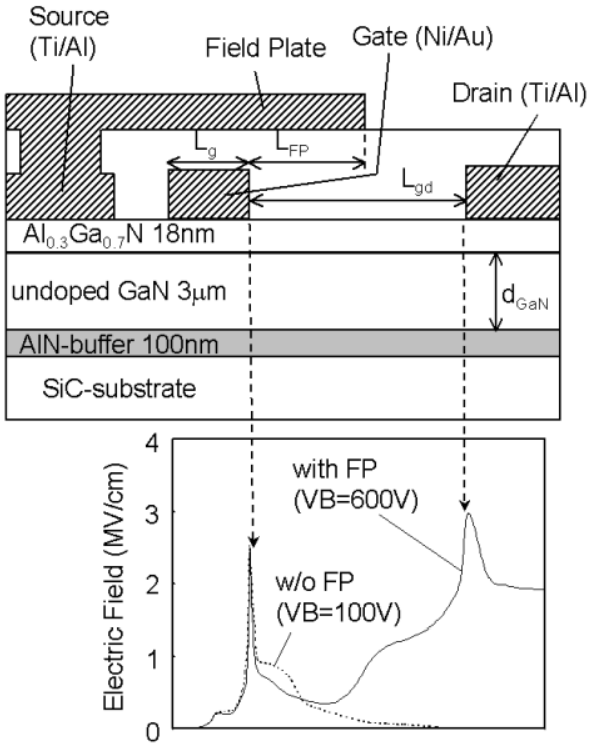


Figure 2.17 Cross-sectional structure of GaN-based HFET with field plate structure (FP-HEMT) and electric field distribution along with the interface of the AlGaN layer with field plate (solid line) and without field plate (dashed line) [42].

However, even in FP-HFET, there are still two peaks in the electric field distribution, which is not entirely suppressed. Analysis of the field plate HFET device electric field distribution first peaks at the gate electrode of the drain side and the other peaking happens at the drain electrode, as shown in Figure 2.17. Therefore, field plate technology could be improved by optimizing electric field distribution.

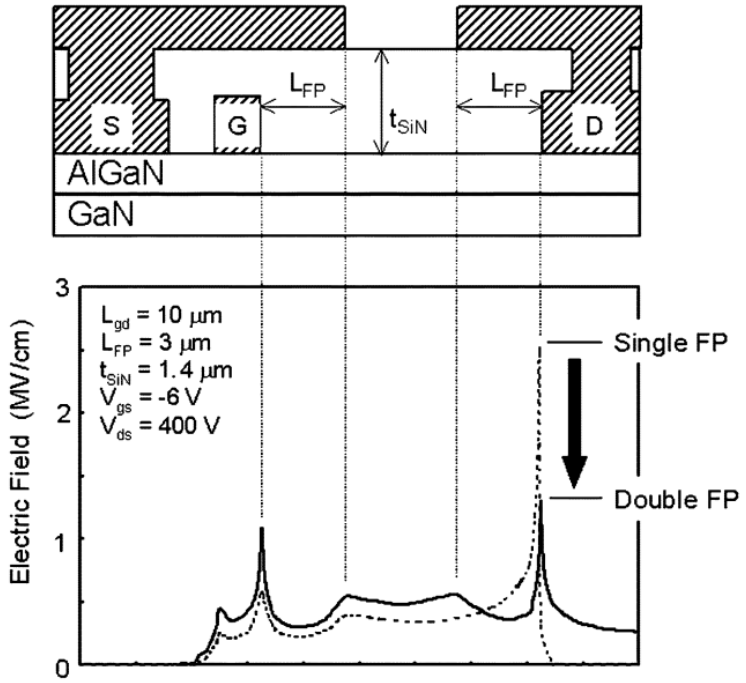


Figure 2.18 Schematic of field plate engineering applied on AlGaN/GaN HFET [44].

Field plate length also affects increasing breakdown voltage. Double FP device further improved breakdown value from 600V to 800V as breakdown testing is presented in Figure 2.18. From dual FP device electric field distribution, it still has optimizing potential; however, FP design could only reduce the peak value and could not overcome it. Over-designed and excessively focused on FP structure will increase the cost of manufacturing. To fix it, polarization super junction HFET was invented and had a better performance on current collapse and dynamic on-state resistance.

The transconductance is also an essential parameter for HFETs. It is termed the drain current variation rate concerning incremental change with gate voltage.

$$g_m = \left(\frac{\partial I_d}{\partial V_g}\right)_{V_d=const} \tag{2.9}$$

The transistor operation's saturation region describes the transistor operation's transconductance of a typical GaN-based HFET. It can be expressed in (2.9)-(2.11) [32]

$$g_m = \left(\frac{\partial I_d}{\partial V_g}\right)_{V_d=const} = \frac{2Z\varepsilon\mu_{2DEG}(V_g - V_{off})}{(d+\Delta d)L}((1+\xi_d) + ((1+\xi_d)^{\frac{1}{2}}))^{-1} \tag{2.10}$$

$$\xi_d = \frac{2\mu_{2DEG}(V_g - V_{off})}{v_{sat}L} \tag{2.11}$$

When the circuit effect is taken into account, the measured extrinsic transconductance from transistor transfer characteristics can be expressed as (2.12)[32]

$$(g_m^{max})_{ext} = \frac{g_m^{max}}{1 + R_s g_m^{max}} \tag{2.12}$$

In (2.9) $(g_m)^{max}$ represents to the peak transconductance value (obtained from the sheet charge density fully undepleted under the gate). R_s stands for the parasitic source resistance.

GaN-based HEMTs/HFETs have a better performance in power electronic operation system. GaN-based power devices have achieved high reliability, stability and outstanding performance. The rapid evolution of wide bandgap semiconductors places the GaN transistor as a critical promotion candidate for the power semiconductor device market.

2.4 Polarization Super Junction (PSJ) HFETs

The Polarization Super Junction concept is based on the GaN cap layer built on hetero-structure AlGaN/GaN. It utilizes a concept of polarization compensation effect in two hetero-interface. An equivalent magnitude of positive and negative polarization charge σ (10^{13}) exists at AlGaN/GaNand GaN/AlGaN interfaces.

2.4.1 Introduction to Polarization Superjunction

Superjunction (SJ) concept emerged and developed almost three decades ago in Silicon-based power semiconductor devices. SJ has become a well-established and commercialized approach for manufacturing power MOSFETs. SJ concept can conquer the trade-off of the material theoretical limited relationship between breakdown voltage and area-specific on-state resistance in conventional planar semiconductor devices. By controlling the doping concentration and the thickness of the p-pillar and n-pillar, SJ devices can realize the charge balance condition to increase the breakdown voltage, at the same time, reduce the on-state resistance [9]. Figure 2.19 depicts the 3D cross-section and electric field distribution of a typical Schottky Barrier Diode (SBD) and SJ diode [45].

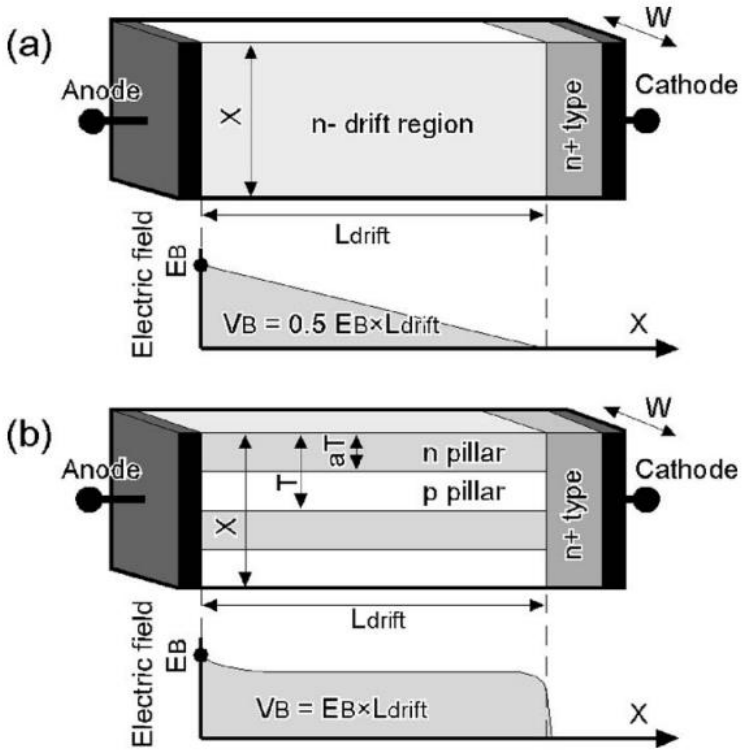


Figure 2.19 Device cross-section and electric field distributions when devices are nearly breakdown (a) conventional SBD and (b) SJ diode [45].

E_B stand for the critical electric field and V_B is breakdown voltage. The relationship between E_B and V_B is derived from the basic theory of electrostatic. The line integral defines the electric potential at a point in a static electric field E

$$V_E = -\int_C E \cdot dl \tag{2.13}$$

C is an arbitrary path connecting the point with zero potential to the end. Compared to different devices with SJ structures and without SJ structures with the same dimensions, SJ devices can support relatively higher voltage. In wide bandgap semiconductors, for instance, GaN or Silicon Carbide (SiC), E_B is nearly ten times higher than Si. In comparison, the transfer SJ concept to wide bandgap semiconductors is complex because a relatively accurate doping control technique is necessary to realise a perfect charge balance condition [45].

The Polarization Super Junction (PSJ) concept was first proposed by A. Nakajima et al. in 2006 [45]. A cross-section of a diode developed on the PSJ concept is presented in Figure 2.28

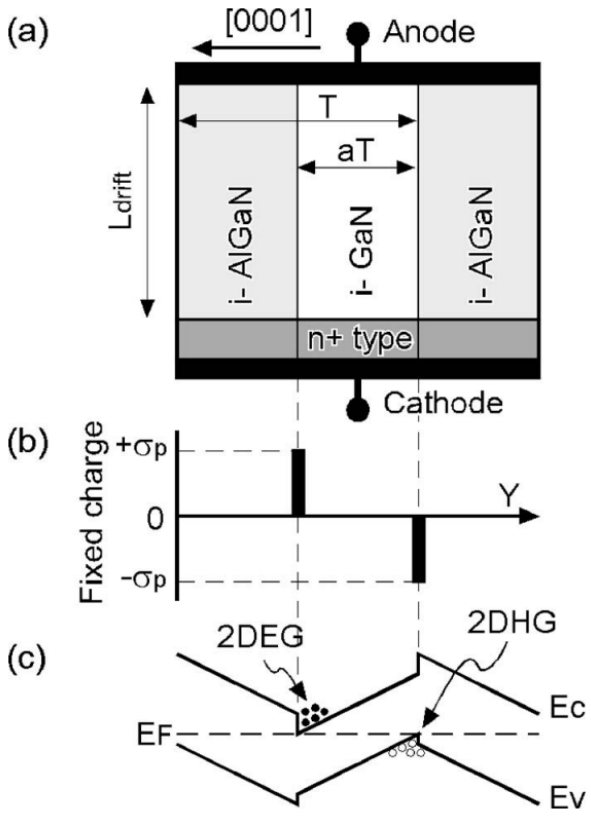


Figure 2.20 (a) Schematic device structure of PJ diode (b) polarization charge of 2DEG and 2DHG (c) AlGaN/GaN/AlGaN structure band diagram [45].

The PSJ concept is based on the polarization charge compensation effect to realize the coexistence of high-density two-dimensional electron gas (2DEG) and two dimensional hole gas (2DHG) at the hetero-interfaces to realize charge balance. A high-density polarization charge $\sigma_P \sim 10^{13}$ cm^{-2} is formed at the hetero-interfaces of AlGaN/GaN/AlGaN. Both positive and negative polarization charges exist at GaNAlGaN/GaN hetero-interfaces, as shown in Figure 2.20(b). The sheet charge density including positive and negative can be managed identically for each layer grown. Hence, the charge balance condition can be easily achieved in PSJ structures. Charge compensation effects in PSJ devices are similar to ideal SJ structures. Figure 2.20(c) presents the simplified band structure of a PSJ Structure. Due to the polarization effect, 2DEG and 2DHG with significant high density are formed at the heterointerfaces of GaNAlGaN/GaN at the same time, respectively, without any intentional doping. This have been proved by Power Microelectronics Team in

Sheffield [46]. This advanced feature in PSJ devices is superior to SJ devices. 2DEG and 2DHG are restricted to quantum wells at the AlGaN/GaN and GaN/AlGaN interfaces. The mobilities of 2DEG and 2DHG are significantly high due to the low level of impurity scattering. Based on the theoretical prediction of 2DHG induced by negative polarization charges, similar to 2DEG, high-density 2DHG, which reached the Power Microelectronic team, first demonstrated more than 10^{13} cm^{-2} at the University of Sheffield and PowDec K.K from Japan in 2010 [47, 48]. Figure 2.21(a) shows the layer structure, including a double-hetero GaN/AlGaN/GaN structure with a p-GaN cap layer.

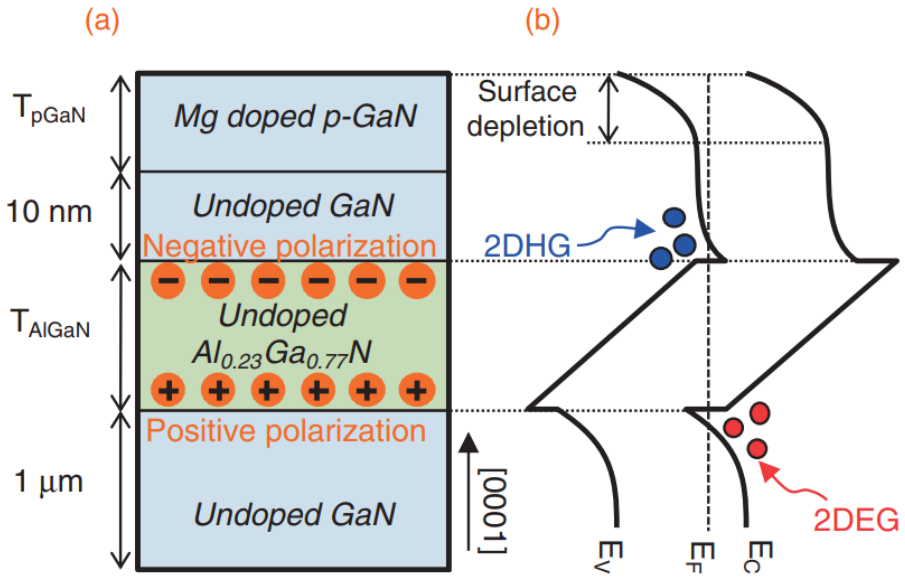


Figure 2.21 (a) p-GaN/u-GaN/AlGaN/u-GaN layers specification and (b) corresponding band diagram [47].

Al composition in the AlGaN layer is 23%, and the thickness is 47nm. The Mg doping concentration of the 20nm p-GaN is 3×10^{19} cm^{-3}. The measured 2DHG sheet density and mobility are 1.1×10^{13} cm^{-2} and 16 cm^2 V^{-1} s^{-1}, respectively. The Mg layer, which is also called p-GaN layer, is only used for forming p-type base contact, does not contribute to the charge balance. This is because the charge density from the Mg layer is much lower than 2DHG [49] and the detailed analysis will be shown in Chapter 4. Although PSJ technology has developed fast in recent years, no transparent analytical

model exists for PSJ devices. The accurate models will be built and analyzed in this work. Measured and analyzed fabricated device work in preparation for building accurate analytical models will be shown in 2.4.2

2.4.2 Characterization in GaN Polarisation Super Junction HFETs

The Sheffield power microelectronic team demonstrated GaN-based HFETs with PJ technology on sapphire substrates in 2011 [50]. Figure 2.22 presents a basic schematics cross-section of a typical GaN-based PSJ HFET and the ideal off-state electric field distribution. The limitation in the trade-off between specific on-state resistance ($R_{(on,sp)}$) and device breakdown voltage bound the development of power semiconductor device technology. In conventional GaN-based HFETs FP technology contribute to optimize the electric field profile, as demonstrated in Figure 2.22(a) [42].

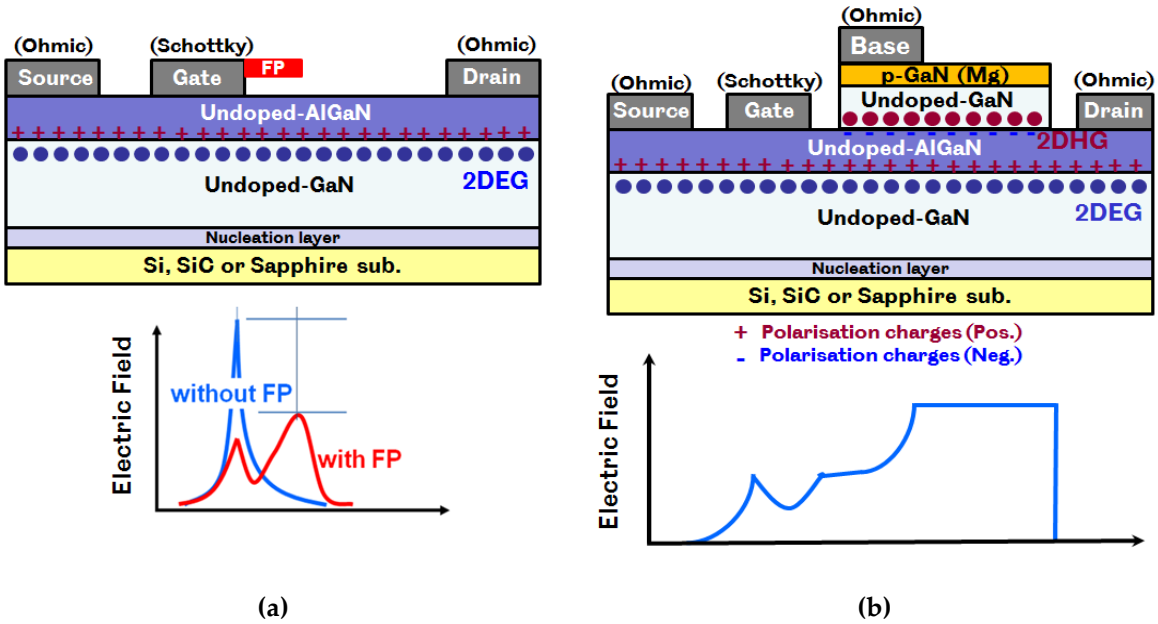
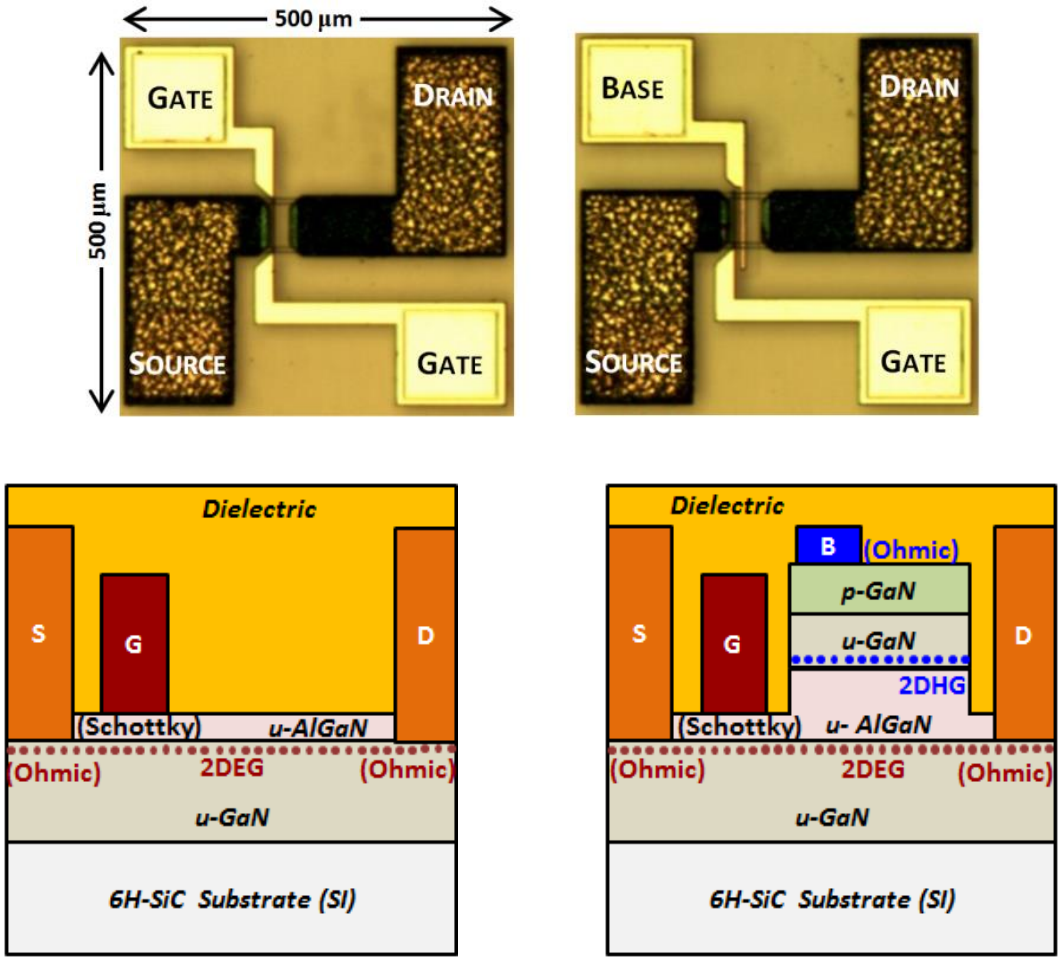


Figure 2.22 Schematics of (a) Conventional GaN-based HFET with FP technology, (b) GaN-based PSJ HFET cross-section with the simplified electric field distribution when the device is under off-state conditions [46].

In Polarisation Super Junction (PSJ), a rectangle-shape electric field is attained by engineering the polarisation property inherent to group III-V nitride compound semiconductors. GaN/AlGaN/GaN herein is formed by GaN Wurtzite crystal structure. The primary device architecture is based on a GaN/AlGaN/GaN double

hetero-structure where positive and negative polarisation charges of equal charge density coexist at the AlGaN $(000\bar{1})$/GaN (0001) interface with two-dimensional electron gas (2DEG) accumulation and GaN $(000\bar{1})$/AlGaN (0001) interface with two-dimensional hole gas (2DHG) accumulation, respectively. This has been illustrated schematically in Figure 2.22(b). With on-state characteristics as in conventional AlGaN/GaN HFETs utilizing the 2DEG for conduction, PSJ technology employs inherent charge balance in the PSJ region to enhance the device breakdown voltage with a specific length of the PSJ [41, 45, 50].

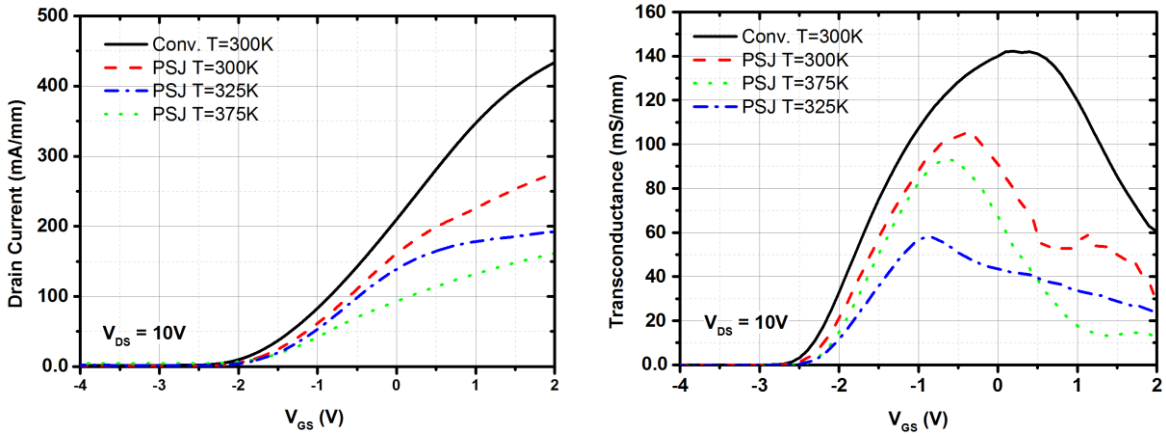
An undoped 20nm GaN, a 47nm AlGaN and an undoped 800nm GaN sub layer forming the heterostructure, were grown by MOCVD on semi-insulating 6H-SiC substrates (370μm). The detailed fabrication process will be discussed in Chapter 3.



(a) **(b)**

Figure 2.23 Micrograph and simplified cross-sectional schematic of (a) Conventional HFET (b) PSJ HFET.

Figure 2.23 (a)-(b) presents the simplified cross-section of a typical fabricated conventional GaN-based HFET without FP (L_G=3µm, L_{GS}=3µm, L_{GD}=28.5µm, L_{DS}=34.5µm, Width=50µm) and PSJ HFET (L_G=3µm, L_{GS}=3µm, L_{GD}=24.5µm, L_{DS}=30.5µm, Width=50µm), respectively, which were fabricated by Dr. Vineet. Electrical characterization of fabricated devices was measured by Power Microelectronics Team in Sheffield using Agilent B1500A power device analyzer. Figure 2.24(a) shows measured transfer I-V characteristics. Derivation transconductance is presented in Figure 2.24(b). Conventional and PSJ HFETs show equivalent threshold voltage (V_{TH} ~ -2V). At V_{DS}=10V, while the drain current (I_D) of a conventional HFET saturates at V_{GS}=2.5V and I_D=480 mA/mm, the same occurs at V_{GS}=2V and I_D=260 mA/mm in a PSJ HFET when the base electrode is connected to ground potential. PSJ HFET also shows reduced transconductance at higher temperatures.



(a) **(b)**

Figure 2.24 Measured characteristics of (a) transfer I-V characteristics at room temperature and V_{DS}=10V and (b) derived transconductance from (a).

As can be observed from Figure 2.24(a)-(b), the linearity of the drain current over a wider range of V_{GS} in conventional HFETs translates to a higher magnitude of peak transconductance (g_m) compared to that of a PSJ HFET. It should be noted that although having a high transconductance can be helpful during power switching, it is a more critical parameter for radio frequency (RF) applications that require the transistors to operate primarily in the saturation region. The trade-off between transconductance characteristics and obtaining ideal charge balance condition within the device.

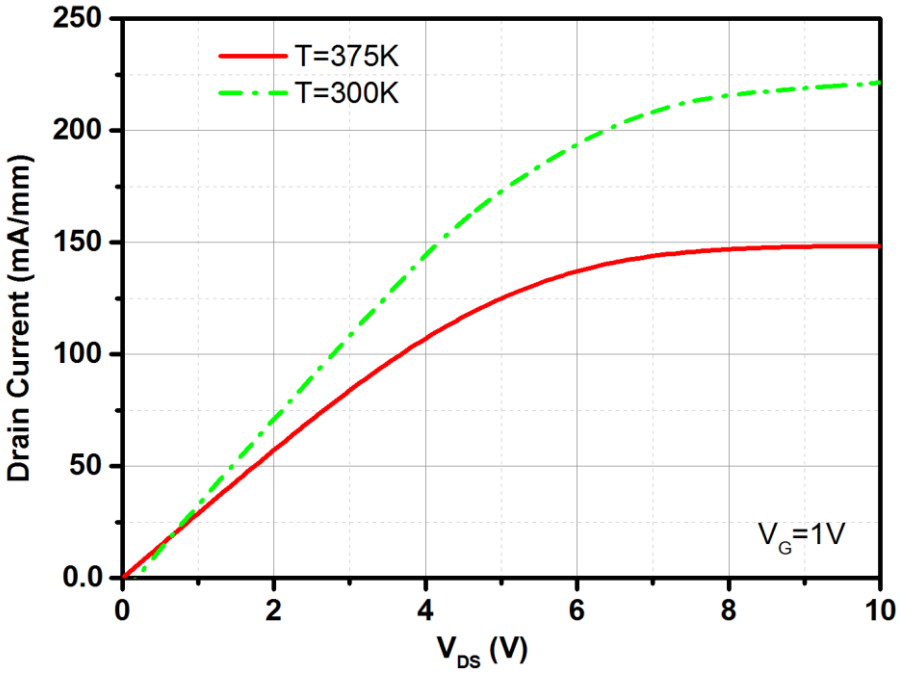
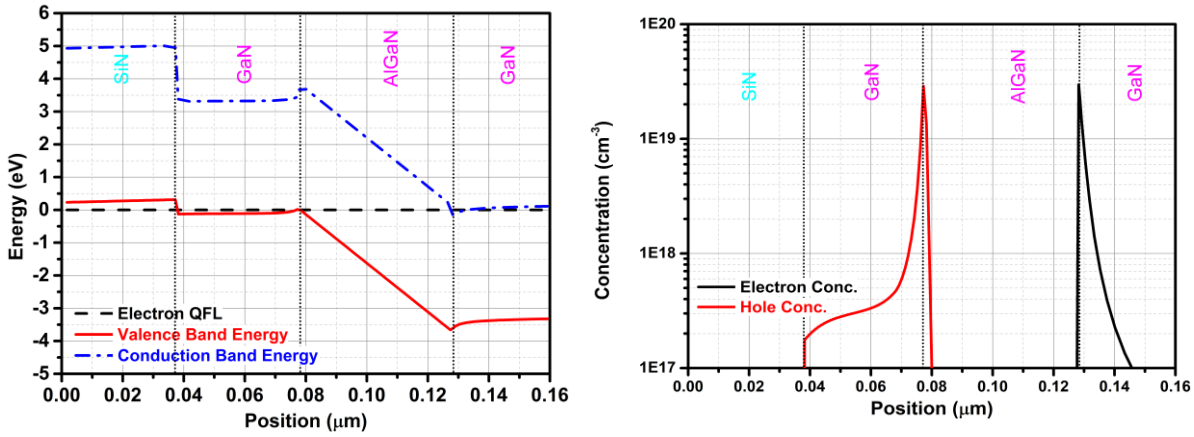


Figure 2.25 Measured output characteristics of PSJ HFET at T_J=300K and 375K. and V_G=1V.

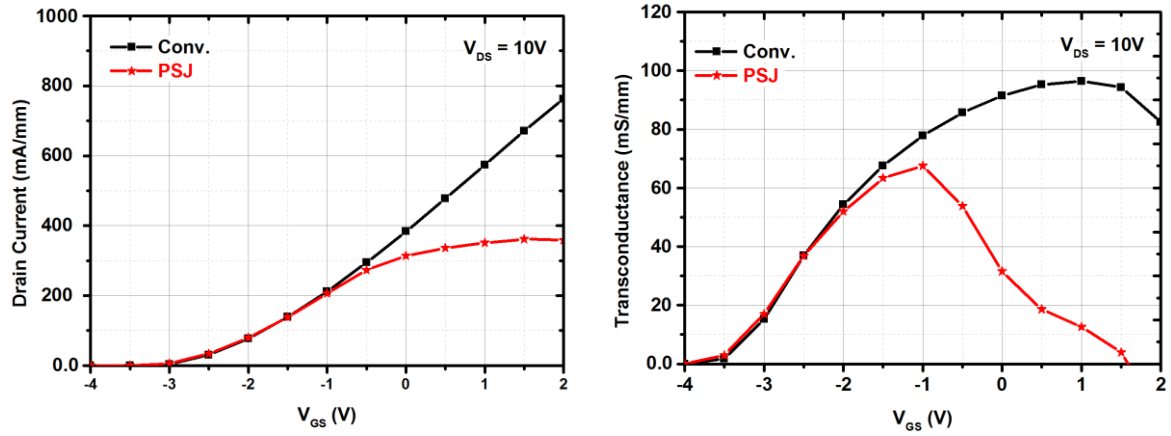
Figure 2.25 demonstrates the reduction of the drain saturation current with increasing temperature. As the concentration of 2DEG is almost independent of the temperature variation, the decrease in current can be attributed mainly to the reduction in 2DEG mobility, increased contact resistance between device metal contact and increased phonon related scattering [51].



(a) (b)

Figure 2.26 (a) Energy Band Diagram (b) Carrier concentration.

In the numerical simulation, physics-based solutions for the sheet density of 2DEG and 2DHG are achieved in Silvaco TCAD using POLAR, CALC models.STRAIN and SRH to obtain reliable results [52]. The detailed simulation work and models will be discussed in the following chapters. The simulated band diagram and concentration of 2DEG and 2DHG in the PSJ region are presented in Figure 2.26(a)-(b).



(a) (b)

Figure 2.27 Simulated (a) transfer I-V characteristics (b) Transconductance.

The geometry of simulated structures was set based on the actual design and processing parameters used for the fabricated devices. However, it is to be noted that

the objective of this simulation study is to obtain a physical understander of PSJ technology rather than fitting the exact experimental results. The p-type doped GaN layer is assumed to be uniform with a doping concentration of $3 \times 10^{19} cm^{-3}$. Mg dopants do not influence the calculation of 2DEG and 2DHG [47, 48]. This is because 20nm of p-type doped GaN cap layer (p-GaN) with $3 \times 10^{19} cm^{-3}$ Mg doping concentration can only serve approximate $0.6 \times 10^{10} cm^{-2}$ positive sheet charge density when Mg active percentage is 1% at 300K [48]. The AlGaN layer thickness in conventional HFET is set as 20nm. AlGaN thickness in PSJ HFET was set as 47nm in the PSJ region and as 20nm in the remaining access region between the source and drain electrodes. Al mole fraction in the AlGaN layer was fixed as 23% in both structures. Simulated transfer I-V characteristics and derived transconductance at V_{DS}=10V, have been shown in Figure 2.27 and appear to be generally aligned to the measured characteristics.

The differences observed such as the simulated value of V_{TH} being ~ - 3 V (instead of -2V for the actual structures), and generally higher normalized values of drain saturation current can be attributed to non-ideality (AlGaN thickness in the access regions post ICP etching and corresponding impact on 2DEG concentration, finite contact resistance.) that is introduced during physical processing of the structures. Based on TLM characterization of test structures within the proximity of the devices, the specific contact resistance was estimated to be in the range of 10^{-4}-10^{-5} ohm.cm^2. I-V characteristics are determined by the distribution of charge carriers (2DEG density) available and the dependence of their transport characteristics under a given biasing condition.

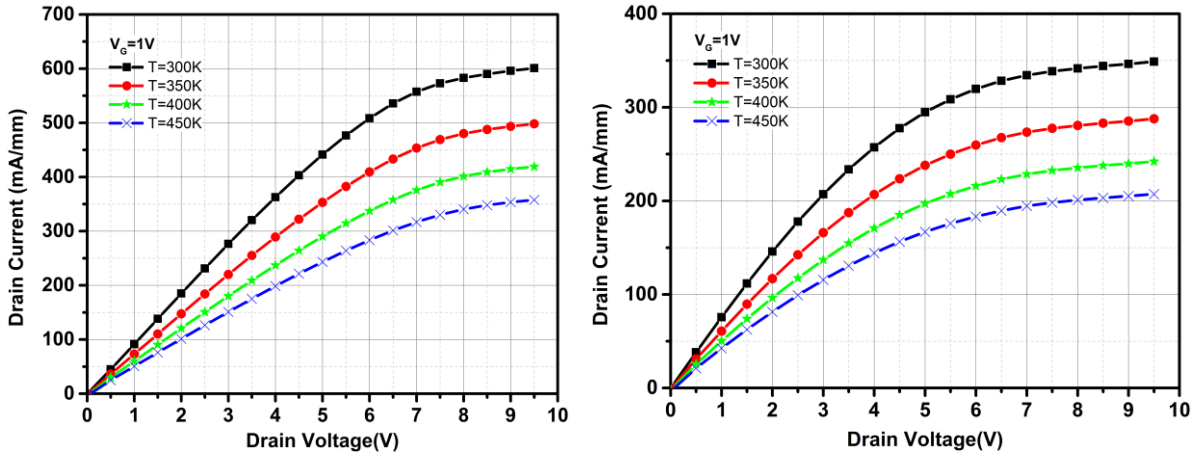


Figure 2.28 Simulated output characteristics of (a) conventional HFET and (b) PSJ HFET at V_{GS}=1V.

The simulated output characteristics and temperature dependence of drain current saturation behaviour with variation in temperature from 300K to 450K are presented in Figure 2.28 and Figure 2.29, respectively.

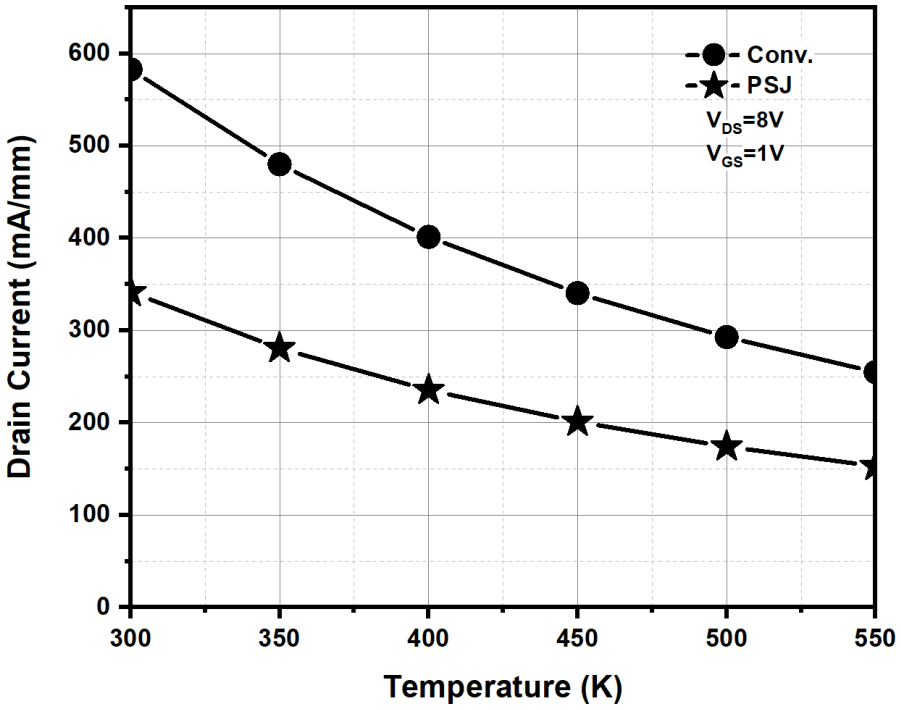


Figure 2.29 Simulated temperature dependence of the saturation currents of conventional and PSJ HFET structures at V_{DS}=8V and V_{GS}=1V.

The results are closely aligned to experimental results within the measured temperature range. While both structures show reduced current levels at higher temperatures, PSJ HFETs are expected to exhibit superior saturation characteristics at elevated temperatures, as shown in Figure 2.29.

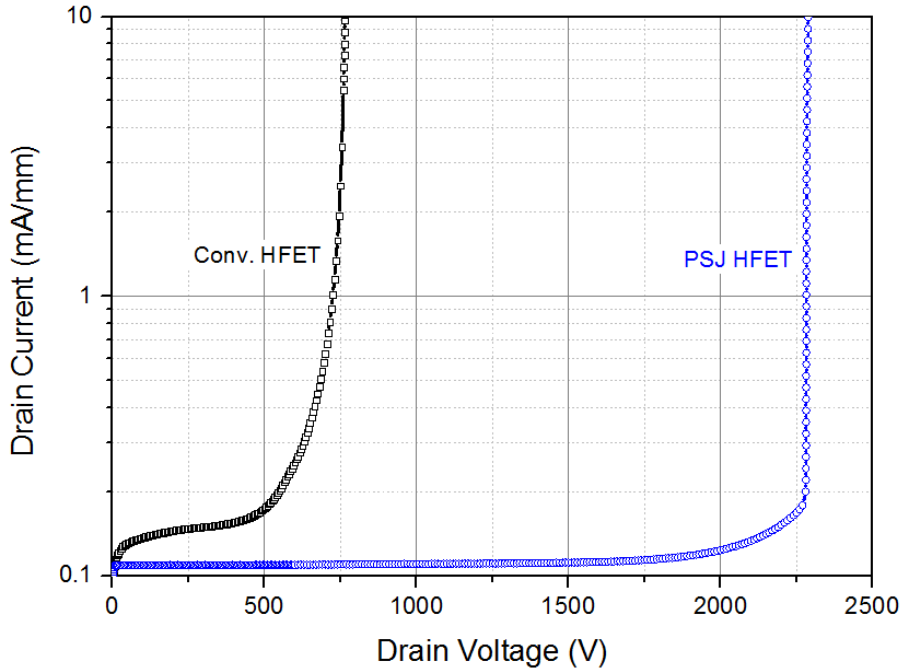


Figure 2.30 Simulated breakdown characteristics of conventional with Field Plate, and PSJ HFET structures at V_{GS}=-5V.

Simulated breakdown characteristics of a conventional HFET (with Gate FP) and the PSJ HFET are shown in Figure 2.30.

Figure 2.31 shows measured off-state characteristics comparison between the conventional GaN-based HFETs and PSJ HFETs applied with V_{gs} = -10 V (L_{gd} = 13 μm).

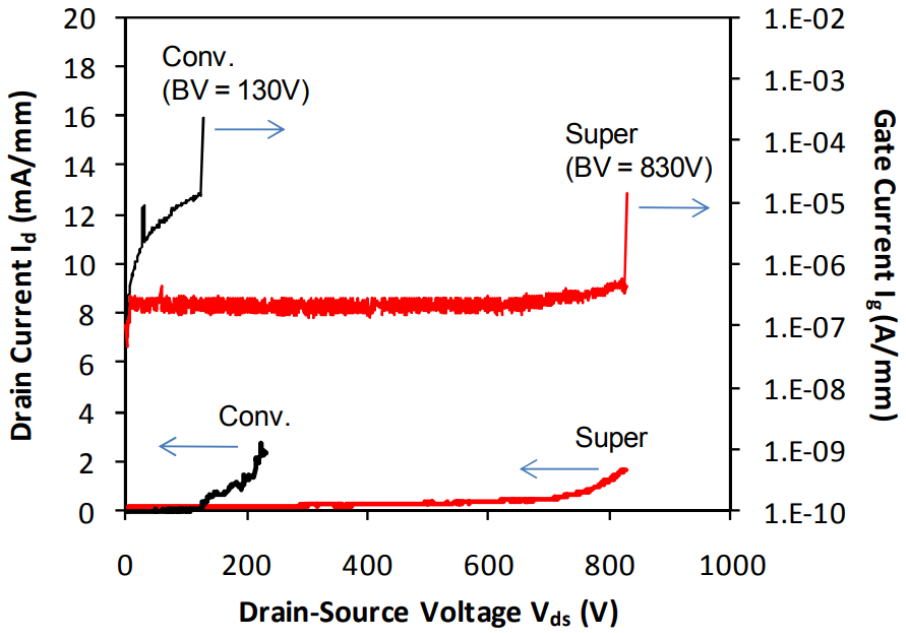


Figure 2.31 Typical off-state characteristics of conventional and PSJ HFETs at Vgs = -10 V [41].

The measured BV is higher than 700 V and the on-resistance is only 15 Ω·mm. Although only a single approach has been established for comparison, there is no single method for designing high voltage GaN HFETs using metal FPs. The techniques can vary from using just Gate FP to including Source and Drain FPs as well as optimized combinations. The degree of device processing complexity varies depending on the adopted technique. With the scenario considered for numerical simulations and measured results, the significantly higher breakdown voltage can be achieved using PSJ without employing any metal FP for a certain length in the drift region. This makes PSJ technology-based GaN power devices ideal for existing and emerging high-temperature power electronic applications. PSJ GaN devices have the potential to become an essential component of next-generation power semiconductor devices, which break the GaN theoretical limit. The better performance of PSJ devices is ideally suitable for ultra-fast operation power systems and IC chips with efficient size.

This revolutionary technology's natural course of evolution is to build theoretical and simulated models compared with the experiment results to understand further and

develop the PSJ technology. The next chapter (Chapter 3) covers the details of building the simulation model and progress made on this front of PSJ GaN technology research and development, especially on the fabricated process.

2.5 Summary

The basic theory of Gallium Nitride material and the physical of two-dimensional electron gases formation and application in wurtzite GaN/AlGaN heterostructures are introduced in this chapter. The key elements for 2DEG, such as Al mole fraction and AlGaN thickness, are discussed and analysed. The fundamental theory of GaN-based HEMTs/HFETs is also acquainted herein as well as FP technology for solving the electric profile issues in GaN HEMTs.

In this chapter, the GaN material property is introduced initially and the polarization engineering of 2DEG and 2DHG is discussed. Field Plate (FP) technology and Polarisation Super Junction (PSJ) concept are also presented herein. Attributed to the intrinsic design of PSJ structure is also the capability to limit the drain saturation current density to almost half the magnitude of what is obtained in a conventional AlGaN/GaN HFET that can be achieved without compromising the typical on-state characteristics. The resulting enhancement in short-circuit capability can therefore be leveraged in the overall system-level design. Partial numerical simulation results are shown and compared in two configurations, developed on FP and PSJ technology, to investigate the device's physical mechanisms. This chapter also shows the measured on-state and off-state characteristics of conventional and PSJ devices as comparisons with simulation results.

Chapter 3 PSJ DEVICES SIMULATION, FABRICATION AND MEASUREMENT

In the previous chapter, Polarisation Super Junction (PSJ) is introduced. This chapter also presents the simulation of PSJ devices, including PSJ diodes, Ohmic gate (OG) PSJ HFETs and Schottky gate (SG) PSJ HFETs, to gain insight into physical devices mechanisms and electrical characteristics. Based on the simulation results, structures will be designed, including test structures, large area devices, and process control monitor (PCM) design. The whole process containing mask design, cleanroom fabrication, and device characterization will be presented and discussed.

3.1 Introduction

PSJ concept uses the compensation effect of polarization charges at each heterointerface. It mainly consists of undoped GaN/AlGaN/GaN layers [45]. A high-density polarization charge is generated at the heterointerfaces as shown in Figure 3.1. The sheet density (*Ns* and *Ps*) can reach $10^{13}cm^{-3}$. Positive and negative polarization charges exist at AlGaN/GaN and GaN/AlGaN interfaces. The thickness of positive and negative charges can be controlled to match each layer perfectly. Therefore, the charge balance condition can be achieved similar to ideal super-junction (SJ) structures. Due to the polarization effect, two-dimensional electron gas (2DEG) and two-dimensional hole gas (2DHG) with significant high density are spontaneously formed at the heterointerfaces of GaNAlGaN/GaN, respectively. The mobilities of 2DEG and 2DHG are relatively high since they are well-confined to quantum wells.

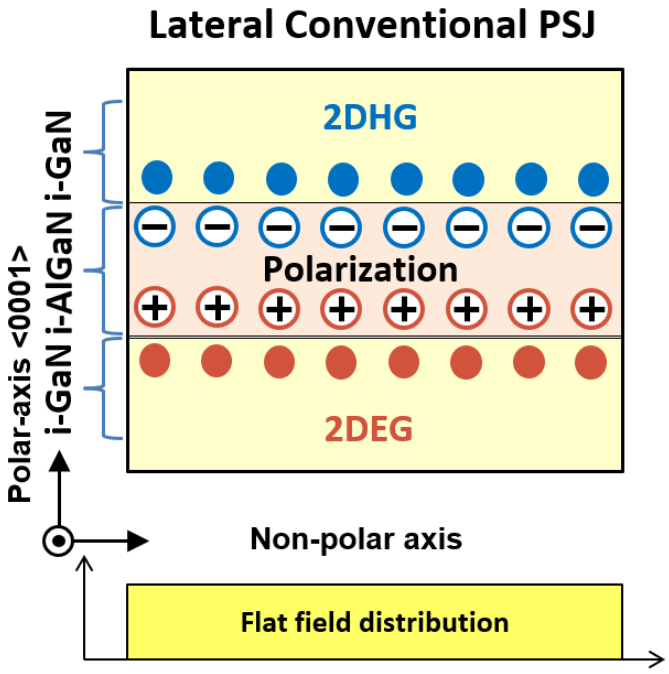


Figure 3.1 Schematic cross section and simplified electric field distribution of lateral PSJ structure.

This chapter first presents an overview of physics-based simulations of PSJ devices. The simulation results contribute to improving the practical design of PSJ devices. Based on simulation results, masks, including PSJ devices, process control management (PCM) structures and novel designs utilized for fabrication are optimized subsequently. The whole process flow is also improved by the reduces unnecessary procedures. Devices are fabricated in the nanoscience clean room. Finally, the next chapter will characterise fabricated devices and calibrate them with analytical and numerical models.

3.2 PSJ Device Simulations

To provide a valid basis for devices fabrication efforts, numerical modelling of on-state, transfer and reverse characteristics of PSJ devices are investigated. Silvaco TCAD Atlas physics-based device simulation software is used in this chapter.

Silvaco TCAD is a computer-assisted design simulation software used in developing, testing and producing semiconductor devices and integrated circuits. This complete

tool enables the physical semiconductor process to provide strong motivation for IC design at all stages, including device simulation (ATLAS), extremely accurate description of interconnect parameters, physical reliability modelling and traditional CAD. All these functions are integrated into a unified framework to provide the performance and reliability effects caused by the changes, the engineer at any stage in the complete design and provide direct feedback.

The most crucial part, Atlas, is a two -dimensional device simulation tool based on the physical mechanism for the electrical characteristics of the structure of a specific semiconductor device and the simulation device is related to the internal physical mechanism. In atlas, each input file must include five groups of statements arranged in the correct order. The order of these groups is the structure specification (mesh, region, electrode and doping), material models specification (material, models, contact and interface), numerical method selection (method), solution specification (log, solve, load and save) and results analysis (extract and tonyplot).

The main models used in the simulation work are shown in Table 3.1. Models are based on the instructions for Silvaco users, examples in the software and previous calibration works [52].

Model	*Description*
POLAR	Spontaneous polarization
CALC.STRAIN	Piezoelectric polarization
CONSRH	Shockley–Read–Hall recombination using concentration-dependent lifetimes
AUGER	Recombination accounting for high-level injection effects
SELB	Selberherr's model for impact ionisation=breakdown

Table 3.1 Models and Parameters used in Silvaco TCAD simulation [52].

The simulation also underlined the importance of a metal field plate at the drain end to enhance the electric field strength within the PSJ layer. Simulation results clearly showed that PSJ could offer an electric field uniformly across the region (L_{PSJ}) between

the edge of the gate and the drain, which would mean an L_{PSJ} (the distance between the edge of the gate and the drain) of 15μm (max) for 1500 V and it can scale up directly with L_{PSJ}.

3.2.1 PSJ Diode Simulation

The PSJ diodes simulations mainly focus on a hybrid type consisting of a conventional lateral PSJ Schottky diode and a GaN PiN diode, **which is designed in Sheffield**, as shown in Figure 3.2. It consists of a p-type doped GaN cap layer (p-GaN) with $5\times10^{19}cm^{-3}$ Mg-doped, a 55nm undoped GaN layer, a 40nm AlGaN layer with 27% Al composition and an 800nm u-GaN sub-layer.

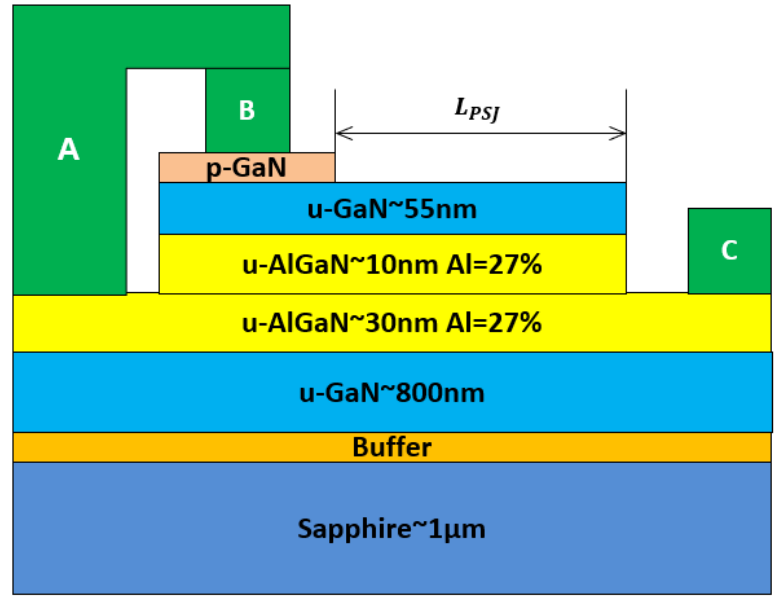
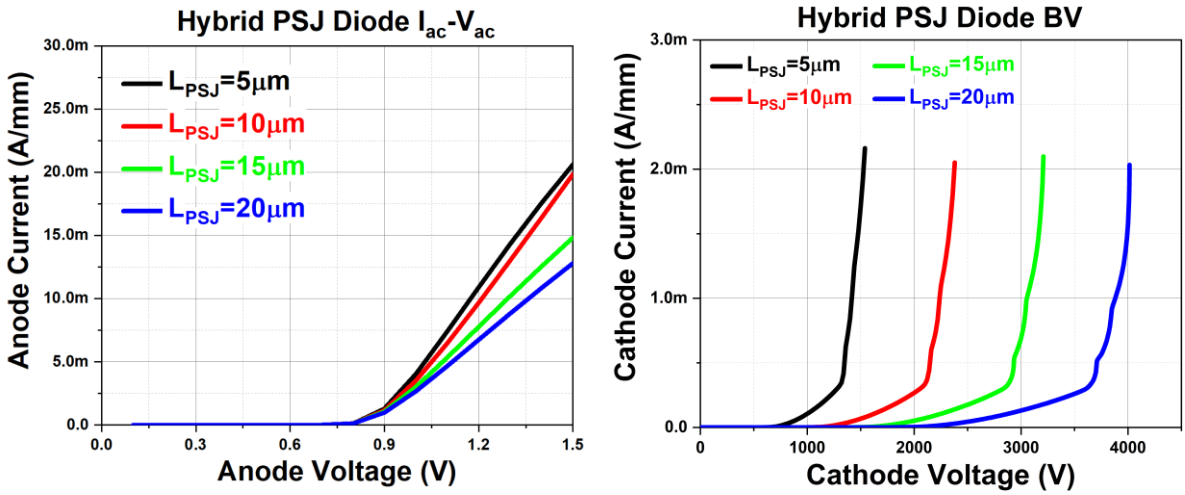


Figure 3.2 Schematic cross-section of the Hybrid PSJ Diode (Designed in Sheffield).

Anode is Schottky contact to 2DEG forming a lateral Schottky PSJ diode and base is Ohmic contact to 2DHG forming a PiN diode.



(a) (b)

Figure 3.3 Simulated Hybrid PSJ Diodes characteristics of (a) I_{ac}-V_{ac} (b) reversed I_{ca}-V_{ca}.

The I_{ac}-V_{ac} characteristic and device blocking capability are shown in **Figure 3.3(a) and (b)**, respectively. With the increase of L_{PSJ}, the current reduces in simulation as expected and breakdown voltage presents a linear scale with L_{PSJ}. A typical PSJ diode with 15μm can support more than 1500V if the critical electric field can reach 1MV/cm as predicted in the simulation.

3.2.2 PSJ HFET Simulation

As shown in Figure 3.4, there are two types of PSJ HFET, Ohmic Gate (OG) and Schottky Gate (SG). The geometries of simulated PSJ HFETs are set based on the actual design and processing parameters used for the fabricated devices. However, it is to be noted that the objective of this simulation study in this chapter is to obtain a physical understander of PSJ technology rather than fitting the exact experimental results. The p-type doped GaN layer is assumed to be uniform with a doping concentration of 3 x 10^{19}cm^{-3}. Mg dopants do not influence the calculation of 2DEG and 2DHG [47, 48]. This is because 20nm of p-type doped GaN cap layer (p-GaN) with 3×10^{19}cm^{-3} Mg doping concentration can only serve approximate 0.6×10^{10}cm^{-2} positive sheet charge density when Mg active percentage is 1% at 300K. The AlGaN layer thickness in conventional HFET is set as 20nm. AlGaN thickness in PSJ HFET was set as 47nm in the PSJ region

and as 20nm in the remaining access region between the source and drain electrodes. Al mole fraction in the AlGaN layer is fixed as 23% in both structures.

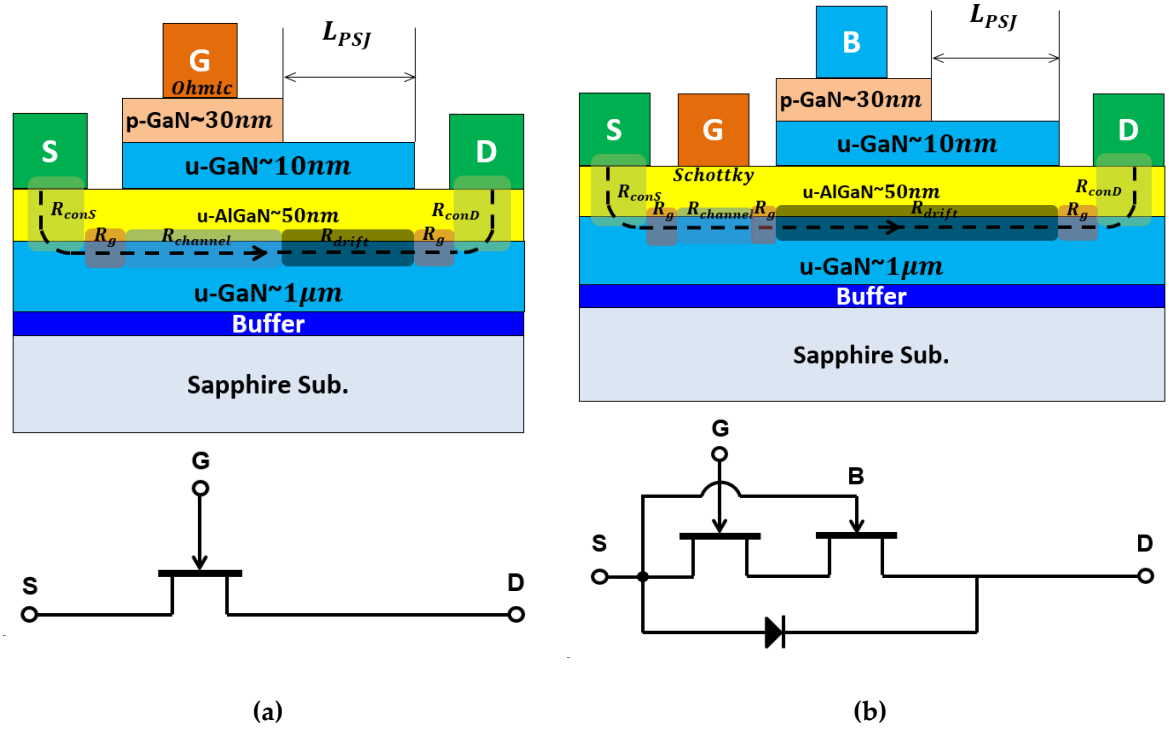
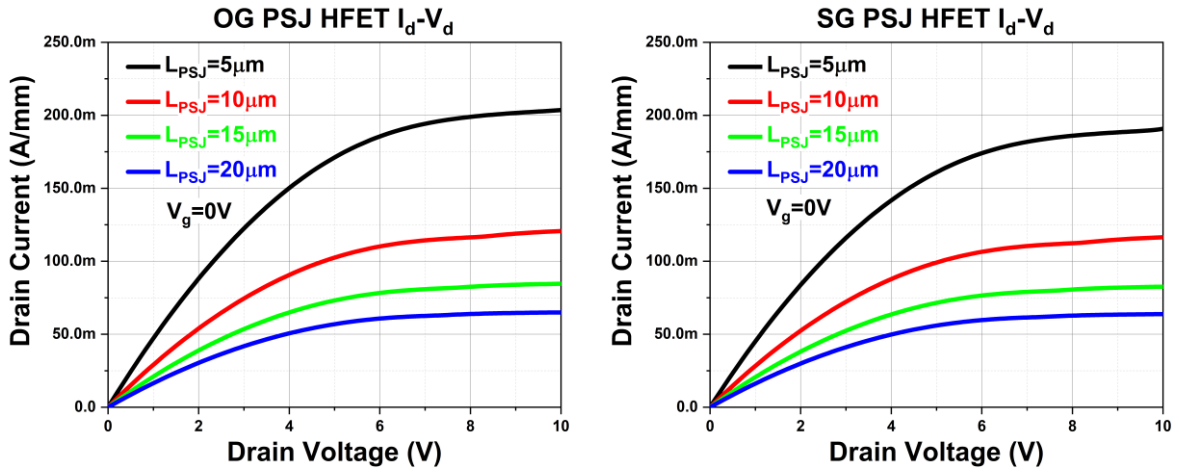


Figure 3.4 Schematics and circuit model of device cross-section for calculating $R_{(on, sp)}$ (a) Ohmic Gate PSJ HFETs (b) Schottky Gate PSJ HFETs.

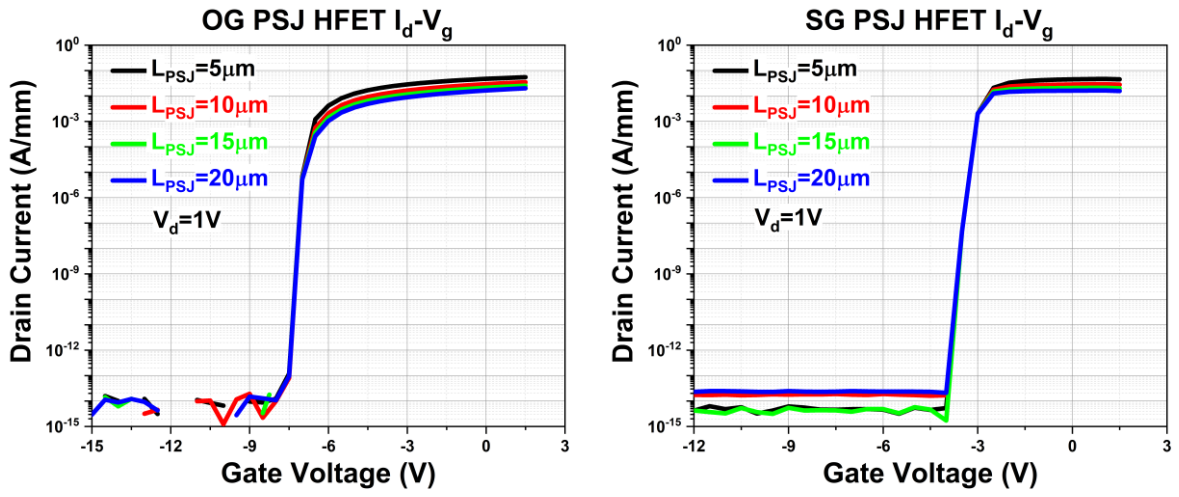
Figure 3.5 shows the Simulated output I_d-V_d characteristics of the OG and SG PSJ HFETs. With the same L_{PSJ}, R_{on} of OG PSJ HFETs is lower than SG devices since the shorter distance between the source and the drain electrode in OG structure.



(a) (b)

Figure 3.5 Simulated output I_d-V_d characteristics of the (a) Ohmic Gate PSJ HFETs (b) Schottky Gate PSJ HFETs at V_g= 0V.

Simulated output I_d-V_g characteristics of the OG and SG PSJ HFETs are shown in Figure 3.6. Although the R_{on} is lower in OG PSJ HFETs, the threshold voltage is lower than that in SG devices, which means the controllability is better for an SG design.



(a) (b)

Figure 3.6 Simulated output I_d-V_g characteristics of the (a) Ohmic Gate PSJ HFETs (b) Schottky Gate PSJ HFETs at V_d= 1V.

Simulated lateral electric field distribution before the breakdown of the OG and SG PSJ HFETs is demonstrated in Figure 3.7. A similar electric field profile proves that the gate design is only related to the threshold voltage.

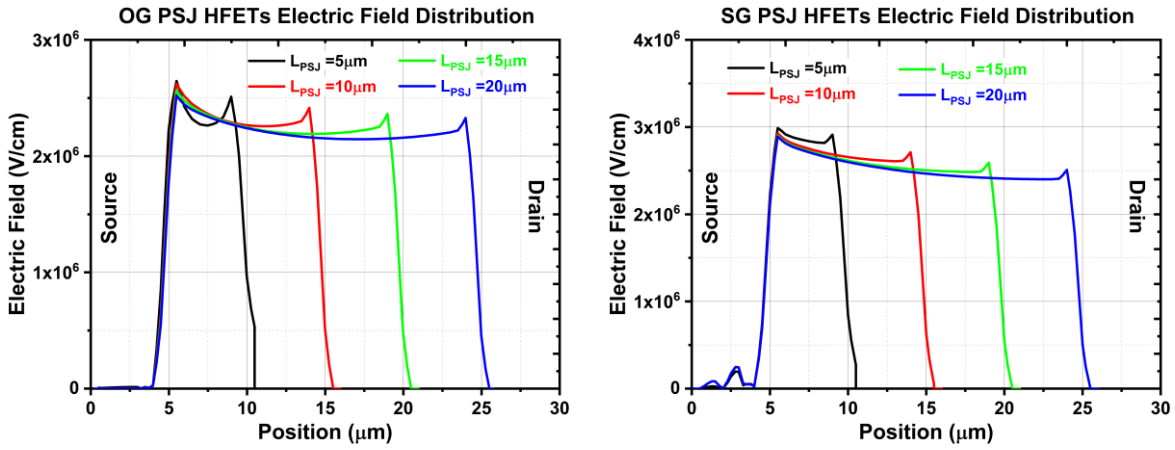


Figure 3.7 Simulated lateral electric field distribution before the breakdown of (a) Ohmic Gate PSJ HFETs (b) Schottky Gate PSJ HFETs at V_g= -15V.

Simulated off-state I_d-V_d characteristics of the OG and SG PSJ HFETs are demonstrated in Figure 3.8. It shows that when devices are designed with the same L_{PSJ}, the breakdown voltage is almost the same in OG and SG PSJ HFETs.

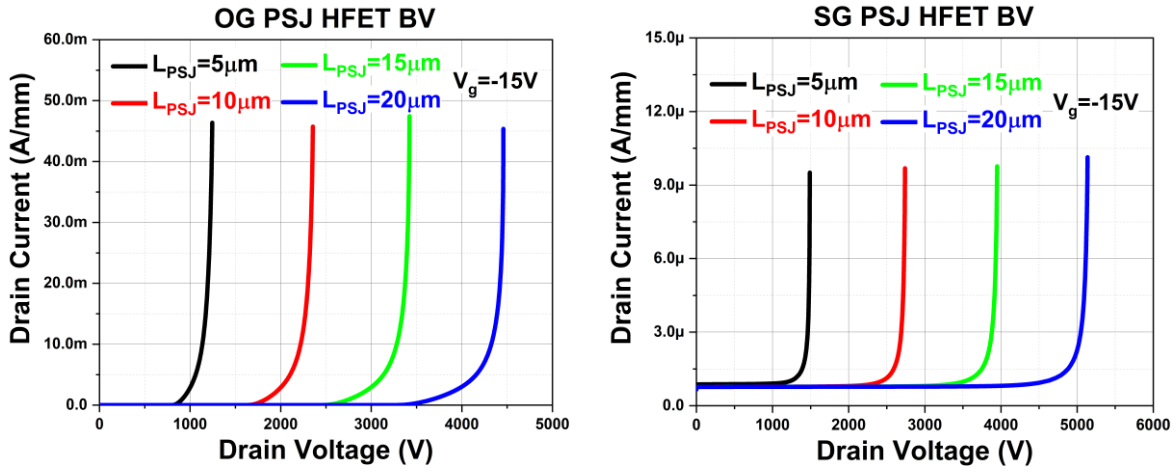


Figure 3.8 Simulated off-state I_d-V_d characteristics of the (a) Ohmic Gate PSJ HFETs (b) Schottky Gate PSJ HFETs at V_g= -15V.

Simulated temperature-dependent output I_d-V_d characteristics of the OG and SG PSJ HFETs are demonstrated in Figure 3.9.

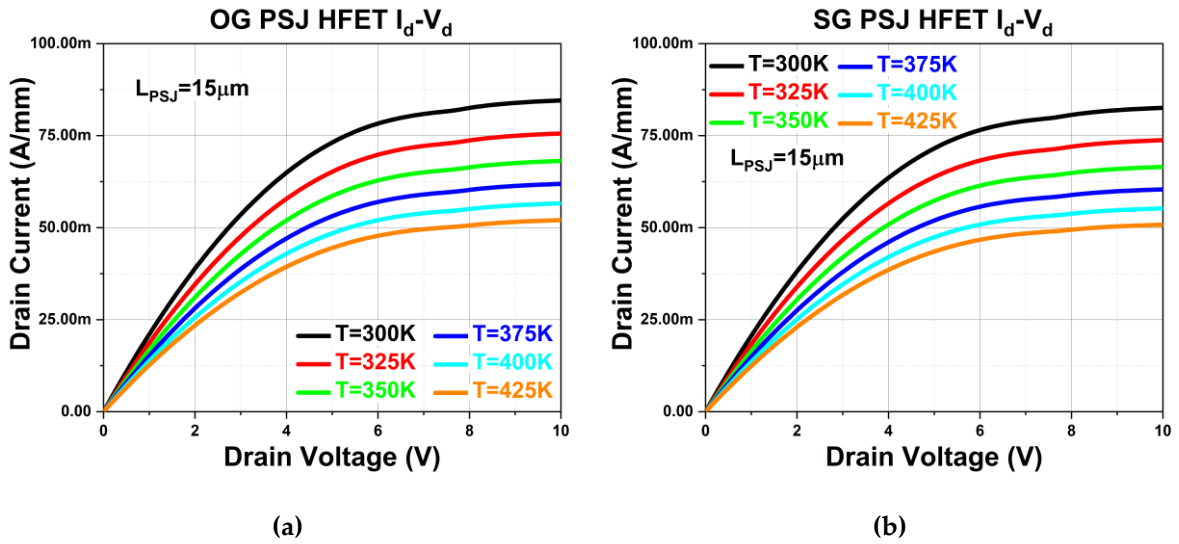


Figure 3.9 Simulated temperature dependent output I_d-V_d characteristics of the (a) Ohmic Gate PSJ HFETs (b) Schottky Gate PSJ HFETs when L_{PSJ}=15μm and V_g= 0V.

With the increase in temperature, the drain current reduces in the linear and saturation regions. As the concentration of 2DEG is almost independent of the temperature variation, the decrease in current can be attributed mainly to the reduction in 2DEG mobility, increased contact resistance between device metal contact, and increased phonon-related scattering [51]. Compared to Figure 3.5 and Figure 3.6, although R_{on} of OG gate devices is lower than SG gate devices, the control of SG type gate is better and the V_{th} is higher.

3.3 PSJ Device Design

As mentioned in Chapter 2, the PSJ concept was proved at the University of Sheffield. The cross-section of the basic structure is presented in Figure 3.10.

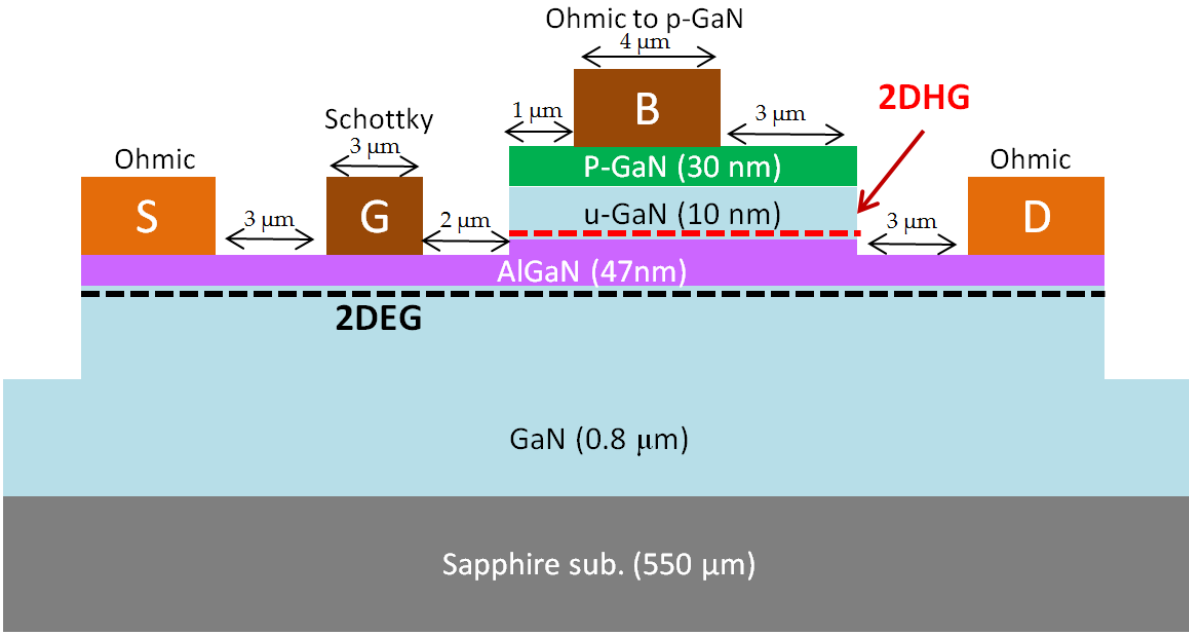


Figure 3.10 Cross-section schematic of PSJ HFET.

A u-GaN, a u-AlGaN and a u-GaN are grown by metal-organic chemical vapour deposition (MOCVD) on 4" Sapphire substrates and formed GaN/AlGaN/GaN hetero-structure. The sub-u-GaN layer with 0.8µm thickness is grown on a nucleation layer by epitaxial growth. The undoped AlGaN layer is 47nm with an Al concentration of 23%. The undoped GaN cap layer is 20nm. P-GaN cap layers are 17nm with $5\times10^{19}cm^{-3}$ Mg doping concentration and 3nm with $2\times10^{20}cm^{-3}$. 2DHG is formed at the upper GaN/AlGaN interface. Correspondingly, 2DEG is located at the bottom AlGaN/GaN interface. The sheet density of 2DEG and 2DHG can reach $1.0\times10^{13}cm^{-2}$ and $9.5\times10^{12}cm^{-2,}$ respectively, as calibrated by the analytical models, simulation and measurement results in the next chapter at room temperature [41].

The source and drain electrodes are formed to Ohmic contact. Ti/Al/Ti/Au are the metals used on the source and drain electrodes to reduce contact resistance N_2 ambient at 800 °C. The gate is Ni/Au on the AlGaN layer without the annealing process. Base electrode is deposited on p-GaN layers under air condition (**20% O_2 and 80% N_2**) at 550 °C annealing temperature. As the passivation layer, a 150nm thick SiN_2 is deposited by a plasma-enhanced chemical vapour deposition (PECVD) system. The

design rule of whole process is 0.5μm and the minimum feature size is 3μm. The device's reported measurement data, which had a width of 50 μm, indicated a drain current of 50 mA/mm at VDS=1V and a breakdown voltage of > 700 V [41]. According to previous experience fabricating PSJ devices in Sheffield, the test structure of SG PSJ HFETs process is designed and optimized and compared with OG PSJ HFETs manufactured at Powdec KK.

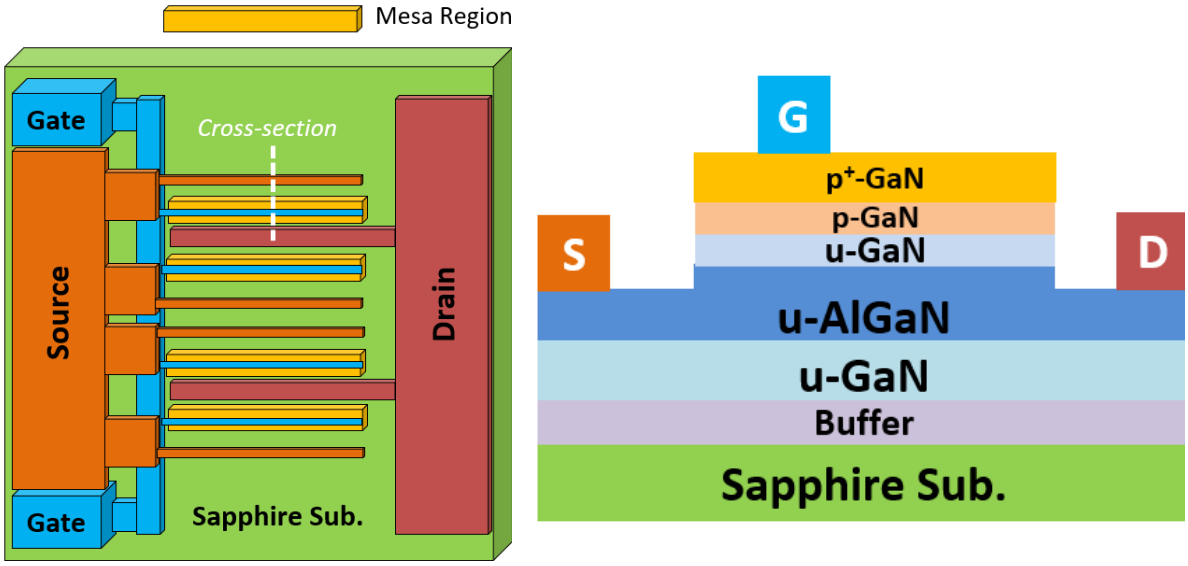
3.3.1 Design Objectives

The project aims to test GaN-based PSJ devices (Diodes and HFETs) on Sapphire substrate :

1. Operating voltage: 500-2000V, is through the variation of the PSJ region length (L_{PSJ}) based on the fabrication of proof of concept devices.
2. Current Capability: up to 5A and mainly focus on test structure. Implementing the large-area device is through the employment of multi-finger layout schemes.

3.3.2 Layout Schemes

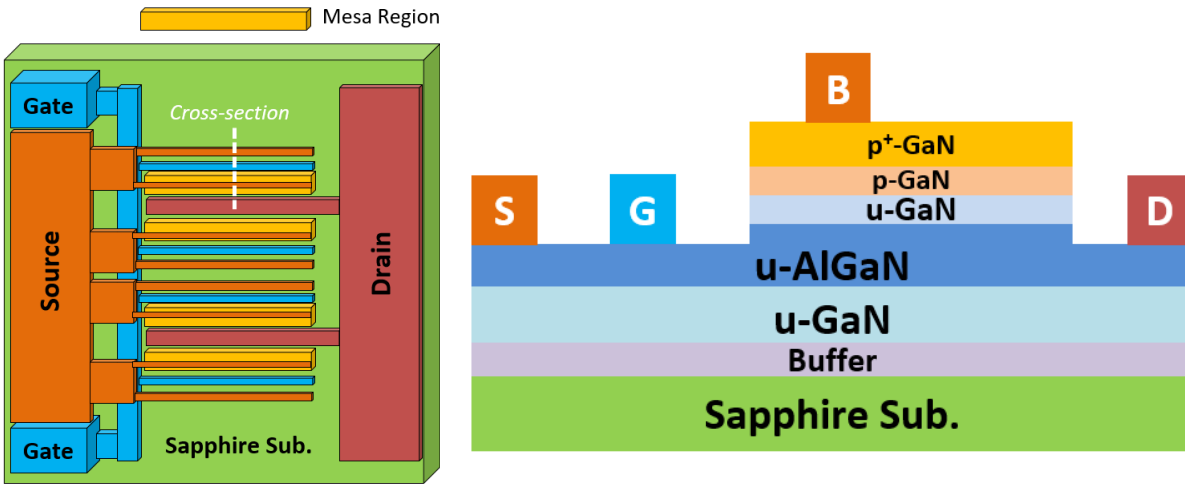
The primary commonly employed schemes for large area GaN-based HFETs are identified as multi-finger layouts [53]. Figure 3.11 and Figure 3.12 show that the design of large area PSJ HFET employs a multi-finger layout. The pad layout like as engaged in a Serpentine-type configuration. Gate, Source and Drain electrodes pad are located in the same fashion as well as the fingers in the active region. Therefore, the type of layout scheme is defined as a multi-finger layout. Gate and Source pads lay on the same side, and the drain electrode pad is located on the opposite side. Finger electrodes in the active region are connected to the bus line, which extends from electrode pads.



(a) (b)

Figure 3.11 Typical Ohmic Gate PSJ Multi-finger Layout (a) Top-view of PSJ FET (b) Cross-section-view of PSJ FET.

Invariably, some regions overlap the gate and source connection parts. In this situation of multi-finger design, air bridges are typically introduced to isolate between the gate and source electrodes and guarantee continuity from the source, gate or drain pad region.



(a) (b)

Figure 3.12 Typical Schottky Gate PSJ Multi-finger Layout (a) Top-view of PSJ FET (b) Cross-section-view of PSJ FET.

3.3.3 PSJ Devices Design

The multi-finger layout schemes are eligible for designing large area PSJ devices. The next step is to develop diodes and transistors based on PSJ technology and previous experience. The reference proof of concept PSJ HFET design used is discussed previously. The aim is to incorporate the understanding mechanism of PSJ technology through designed devices and enhance the device's power handling capability.

Current capability in each finger Source/Drain/Base electrode sizing

The primary challenge is determining the size of the electrode fingers, such as width, length and thickness, in the active region. It is essential to ensure these fingers have sufficient current handling capability and guarantee that each finger's current distribution is uniform during conduction. From a reliability perspective, the crucial part of being considered is electromigration, and gold (Au) form the interconnection in power circuits is supposed to avoid failure. This type of failure mode depends on the material used for interconnects, geometry, current density, current levels, metal deposition techniques, under and overlayers, and the metal conductor film temperature [54-57]. Multiple parameters influence the metal reliability performance of electrodes, whereas a large current density of close to 250 kA/ cm^2 is in the safe range of operation from functionality and reliability. The plurality in each device is also an essential factor which can affect the size of the drain and source electrodes. The feasible metal thickness in practical fabrication can also determine the size of each finger. According to the previous fabrication work, the size of the drain and source electrodes is determined by the unit cell plurality. Therefore, in this work, the desired current ratings are assumed as:

- The maximum metal thickness achievable is 2μm

- The minimum metal width in each finger is 4μm
- The maximum electrode width is 1600μm (with the reduction of the rated current, the value will reduce to 500μm)
- Current density in each finger unit cell (normalized to gate width) = 50mA/mm
- Maximum current density through each metal finger = 250kA/ cm^2

The current target rating of 1A as an example thus indicates a functional Gate width requirement of 20mm. Each finger length is set as 1600μm. Hence, 7 cells is a considerable number that can manage effectively to handle 1A current rate with the assumption of uniform current distribution (it should be noted that each cell has 1 gate, and each drain or source finger is shared by two cells). Each drain/source finger would require the ability to handle ~ 75mA. Considering the maximum allowable current density is 250kA/ cm^2, drain and source electrode length needs $\geq$ 15μm with a metal thickness of 2μm. Since the PSJ concept also enables reverse conduction through a diode-like behaviour from the base side to the drain, the base finger is also designed in the same rules.

Electrode Pad sizing

The area size of the pad design is based on the package approach and wire-bonding facility. Considering the University of Sheffield Au wire-bonding facility, the dimension of the pad is set with a diameter of 250μm**.** Typically, in the design of wire-bonding for power semiconductor devices, the suggested pad area generally is 2-3 times for wedge-bonding and 3-5 times for ball-bonding. Therefore, the pad area of wire-bonded devices requires a minimum side length of 250μm [58, 59].

Another packaging approach is Flip-Chip Bonding with gold stud bumping. The benefit of this option is that the effective interconnection length is lower than the wire-

bonding method [60]. The pad minimum dimensions for gold stud-bumping are to be designed as 100μm×100μm when flip-chip bonding is adopted.

Device Blocking Voltage

The next aspect of the potential PSJ device design is the operating voltage of the devices, which is targeted to be enough to support 650V and 1200V. Based on previous test results from the proof of concept devices and according to the theory that the device blocking capability is primarily governed by the PSJ region length (from base right edge to mesa right edge), 15 μm is enough to sustain 1500V which have considered 20% additional margin based on the objective operating voltage of PSJ devices. All high-power and high-frequency GaN-based PSJ devices will be designed based on this specification.

3.3.4 Optimization of Process Flow and Mask Design

Following parameters requirements for multi-finger layout determined by the aim of the design and previous work, process flow and mask needs to be designed next. The process flow is optimized as:

- Optimize the alignment mark to reduce artificial error.
- Increase the controllability of ICP etching (more precise etch depth) and reduce the roughness of the surface after the etching process.
- The p-GaN etch process is optimized (compare ICP dry etch and HF wet etch) to ensure that p-type doped GaN will not impact the charge balance of 2DEG and 2DHG.
- Optimize the base electrode contact (p-GaN Ohmic contact) performance through varying the metallization and annealing (time and temperature).
- Optimize the thickness and quality of the insulation layer surrounding metal fingers or pads to minimize any supplementary leakage from the pad regions

- Enhance the controllability via etching and increase the second metal deposition thickness to the appropriate level to guarantee the continuity between source and drain pads to fingers in the device active region. Investigate a novel and innovative approach to enhancing individual source and drain current handling capability of electrodes. The electrode finger lengths should be of practical value to reduce finger resistance.
- The thick dielectric layer deposition for devices passivation and pads window opening.

The overall process flow for both PSJ HFETs and diodes(on Sapphire substrate) is demonstrated in Table 3.2 and Figure 3.13:

S.No	Process	Mask	Sub-process	Equipment/Chemical
1	**Alignment Mark Etching**	**GDS Layer 0 – Alignment Mark – AM (Dark Field)**	1.1 3-step Cleaning	n-butyl acetate-acetone-IPA
			1.2 Photolithography	Carl Suss MJB3 UV300
			1.3 ICP Etch	Oxford PlasmaSystem100
			1.4 Photoresist Stripping	POSISRIP EKC830
			1.5 Etch Depth measurement	Veeco Dektak 150
2	**Device Isolation**	**GDS Layer 1 – Isolation – ISO (Light Field)**	2.1 3-step Cleaning	n-butyl acetate-acetone-IPA
			2.2 Photolithography	Carl Suss MJB3 UV300
			2.3 ICP Etch	Oxford PlasmaSystem100
			2.4 Photoresist Stripping	POSISRIP EKC830
			2.5 Etch Depth measurement	Veeco Dektak 150
3	**Pad Insulation**	**GDS Layer 4 – Gate Isolation**	3.1 3-step Cleaning	n-butyl acetate-acetone-IPA

		– GI (Dark Field)	3.2 PECVD Deposition (S_3N_4)	Plasmatherm 790 series
			3.3 Thickness verification on monitor wafer	JA Woollem VASE ®
			3.4 Primer application	Hexa-Methyl-Di-Silazane (HMDS)
			3.5 Photolithography	Carl Suss MJB3 UV300
			3.6 Wet etch	Buffered HF (10%)
			3.7 Photoresist Stripping	POSISRIP EKC830
			3.8 Etch Depth measurement	Veeco Dektak 150
4	**Mesa etch**	**GDS Layer 2 – Mesa Etch – ME (Light Field)**	4.1 3-step Cleaning	n-butyl acetate-acetone-IPA
			4.2 Photolithography	Carl Suss MJB3 UV300
			4.3 ICP Etch	Oxford PlasmaSystem100
			4.4 Photoresist Stripping	POSISRIP EKC830
			4.5 Etch Depth measurement	Veeco Dektak 150
5	**Drain/Source Contact**	**GDS Layer 3 – N Contact – NC (Dark Field)**	5.1 3-step Cleaning	n-butyl acetate-acetone-IPA
			5.2 Photolithography	Carl Suss MJB3 UV300
			5.3 Dilute HCl dip	
			5.4 Thermal evaporation of Ti/Al/Ni/Au (800°C N_2 ambient 1min)	Edwards Coating System E306A
			5.5 Lift-off	
			5.6 RTA	Mattson RTA System
6	**Base Contact**	**GDS Layer 5 – P Contact – PC (Dark Field)**	6.1 3-step Cleaning	n-butyl acetate-acetone-IPA
			6.2 Photolithography	Carl Suss MJB3 UV300

			6.3 Dilute HCl dip	
			6.4 Thermal evaporation of Ni/Au	Edwards Coating System E306A
			6.5 Lift-off	
			6.6 RTA (500°C air ambient 10mins)	Mattson RTA System
			6.7 3-step Cleaning	n-butyl acetate-acetone-IPA
			6.8 Photolithography	Carl Suss MJB3 UV300
			6.9 Thermal evaporation of Ti/Au	Edwards Coating System E306A
			6.10 Lift-off	
7	**Gate Contact**	**GDS Layer 8 – Gate Contact – GC (Dark Field)**	7.1 3-step Cleaning	n-butyl acetate-acetone-IPA
			7.2 Photolithography	Carl Suss MJB3 UV300
			7.3 Dilute HCl dip	
			7.4 Thermal evaporation of Ni/Au	Edwards Coating System E306A
			7.5 Lift-off	
8	**Gate Insulation & Via**	**GDS Layer 9 – Via – V (Dark Field)**	8.1 3-step Cleaning	n-butyl acetate-acetone-IPA
			8.2 PECVD Deposition (S_3N_4/Oxide)	Plasmatherm 790 series
			8.3 Thickness verification on monitor wafer	JA Woollem VASE ®
			8.4 Photolithography	Carl Suss MJB3 UV300
			8.5 RIE Etch	
			8.6 Photoresist Stripping	POSISRIP EKC830
			8.7 Etch Depth measurement	Veeco Dektak 150

9	**Second Metal**	**GDS Layer 10 – Metal 2 – M2 (Dark Field)**	9.1 3-step Cleaning	n-butyl acetate-acetone-IPA
			9.2 Photolithography	Carl Suss MJB3 UV300
			9.3 Thermal evaporation of Ti/Au	Edwards Coating System E306A
			9.4 Lift-off	
10	**Dielectric deposition/Pad opening**	**GDS Layer 7– Pad (Dark Field)**	10.1 3-step Cleaning	n-butyl acetate-acetone-IPA
			10.2 Dielectric deposition	
			10.3 Photolithography	Carl Suss MJB3 UV300
			10.4 RIE Etch	
			10.5 Photoresist Stripping	POSISRIP EKC830
			10.6 Etch Depth measurement	Veeco Dektak 150
			10.7 3-step Cleaning	n-butyl acetate-acetone-IPA

Table 3.2 The overall process flow for PSJ HFETs and diodes (Sapphire substrate).

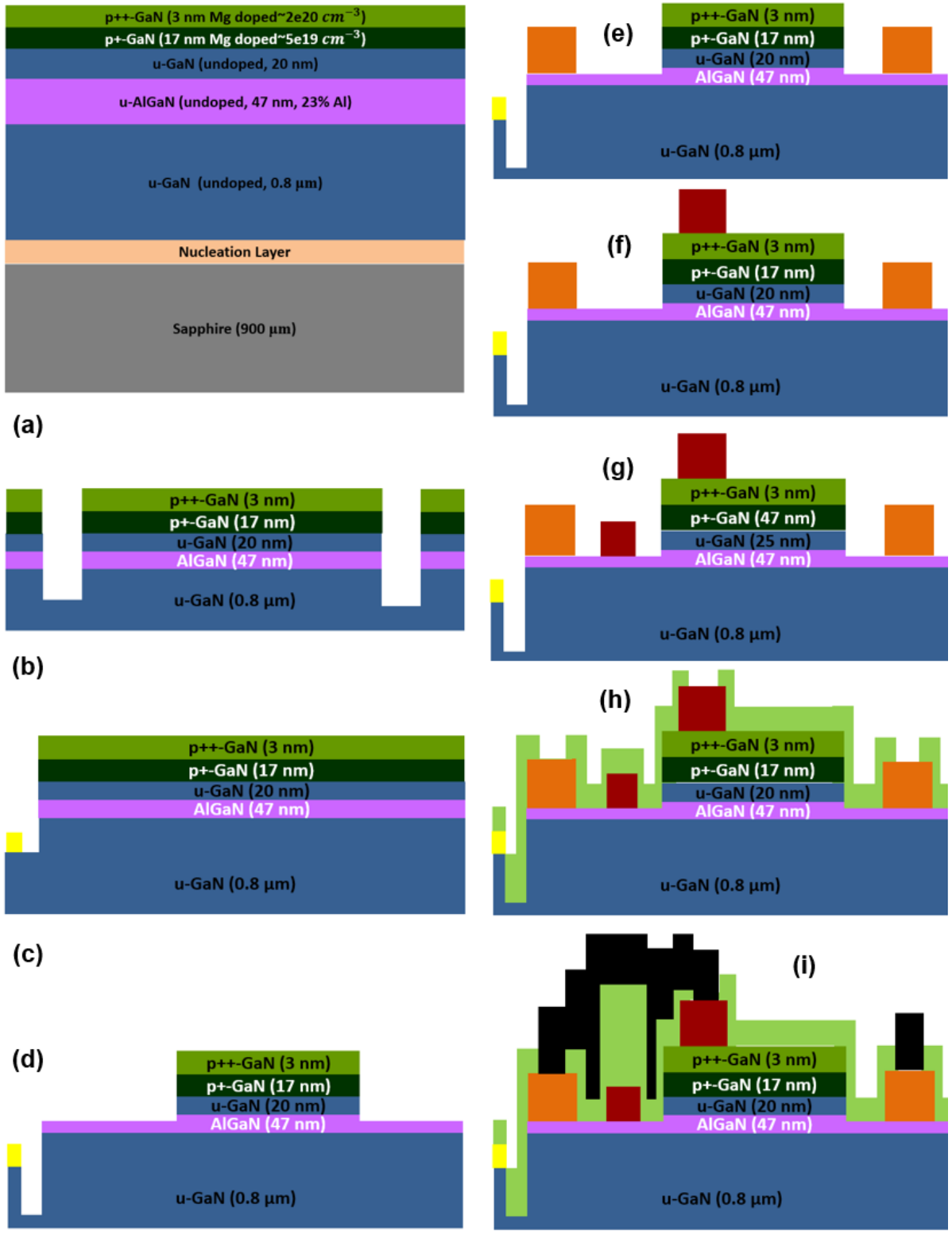


Figure 3.13 Large area Process flow (Fabricated in Sheffield) (a) Starting material (b) Alignment mark (c) Device isolation and Pad insulation (d) Mesa formation (e) Drain/Source contact (f) Base contact (g) Gate contact (h) Via (Gate isolation) (i) Second metal.

The final step is depositing a final insulator layer and open a window for the pad. The schematic of the final device cross-section and layout (serpentine gate) are presented in Figure 3.14.

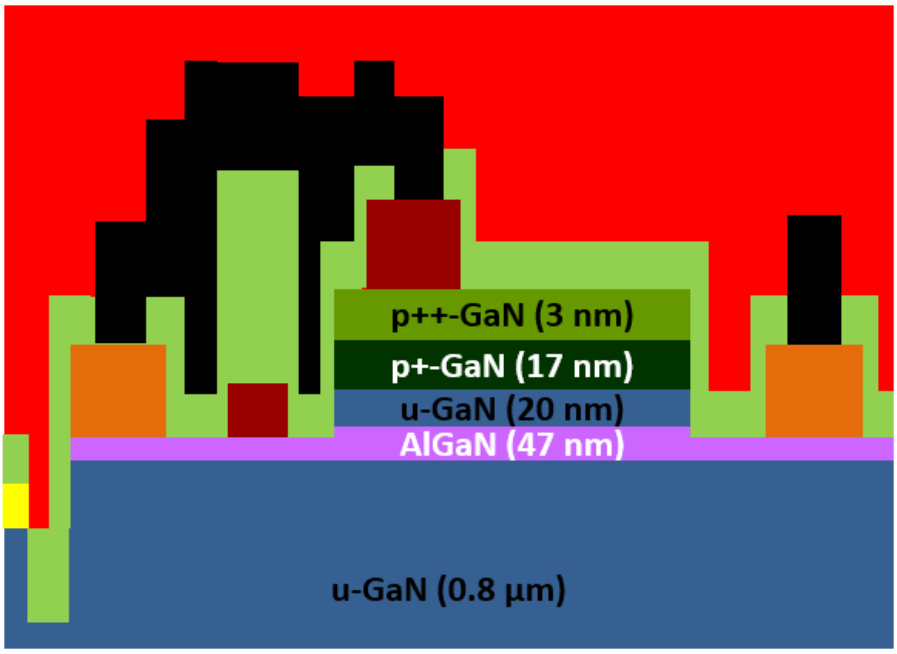


Figure 3.14 Schematic of the final device (cross-section and layout (Fabricated in Sheffield)).

3.4 PSJ Device Mask Design

The following PSJ devices are mainly selected to be scaled up and compared with PSJ devices from Powdec KK.

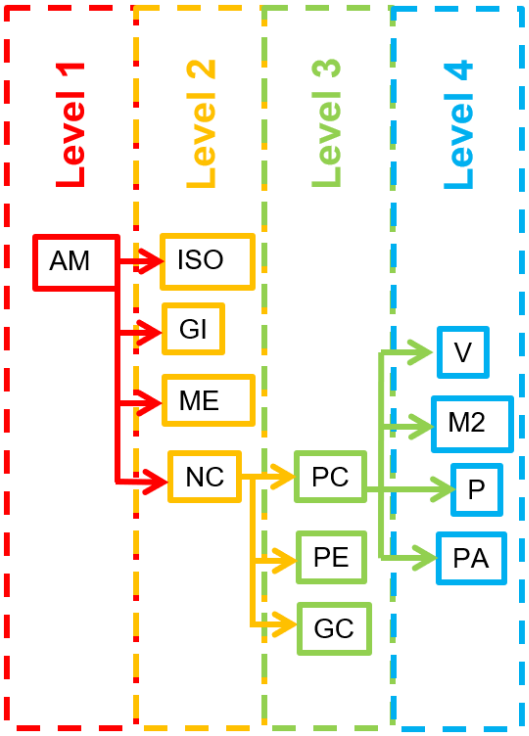
1. Hybrid/PSJ Diodes (as demonstrated in Figure 3.2)
2. OG PSJ HFETs and SG PSJ HFET (as demonstrate in Figure 3.4)

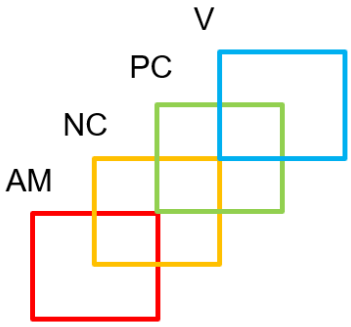
Once the process flow was developed and the primary parameters of PSJ devices are defined. The Mask design software used is Klayout, which is a layout design software. Compared with the previous mask design set, in this process flow version, a p-GaN etch mask is regarded as an optional design to remove the additional p-GaN layer. The instruction of the Graphic Database System (GDS) layers (0-10) are depicted below in Table 3.3.

Layer	Mask No.	Alias	GDS No.	Aligned to	Mask Tone
AM	1	Alignment Mark	0	NA	Dark Field
ISO	2	Isolation	1	AM	Light Field
ME	4	Mesa Etch	2	AM	Light Field
NC	5	N Contact	3	AM	Dark Field
GI	3	Gate Isolation	4	AM	Dark Field
PC	6	P Contact	5	NC	Dark Field
PAS	12	Passivation	6	PC	Dark Field
Pad	11	Pad	7	PC	Dark Field
GC	8	Gate Contact	8	NC	Dark Field
V	9	Via	9	PC	Dark Field
M2	10	Metal 2	10	PC	Dark Field
PE	7	P-GaN Etch	11	NC	Dark Field

Table 3.3 The alignment sequence for GaN-based PSJ HFET (on semi-insulating Sapphire substrate).

But before that, the mask alignment sequence had to be finalized as that directly impacts the misalignment tolerances for the various layers with respect to the available alignment marks. The minimum feature size and feasible misalignment are $\pm$ 1μm for photolithography in this fabrication process. To reserve some margin, the design rule for minimum misalignment is identified as $\pm$ 1.5μm. The alignment sequence chosen is as depicted below in Figure 3.15(a) and that provided the minimum dimensions for the basic cell (The minimum gate length was selected as 3μm) as illustrated in Figure 3.15(b) and (c).



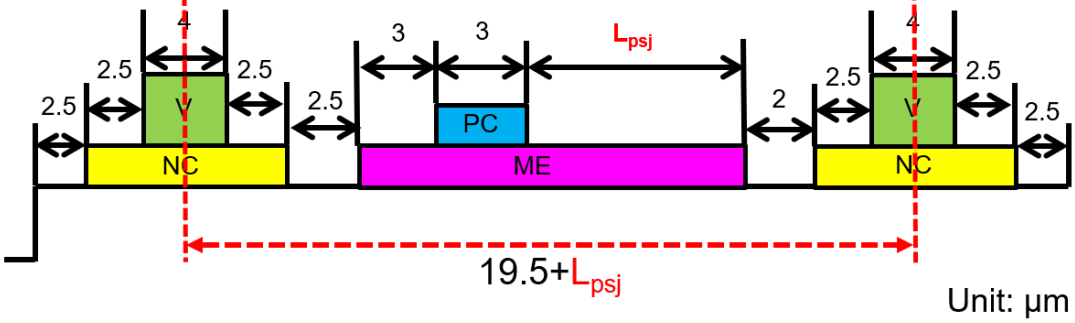


Alignment tolerance:

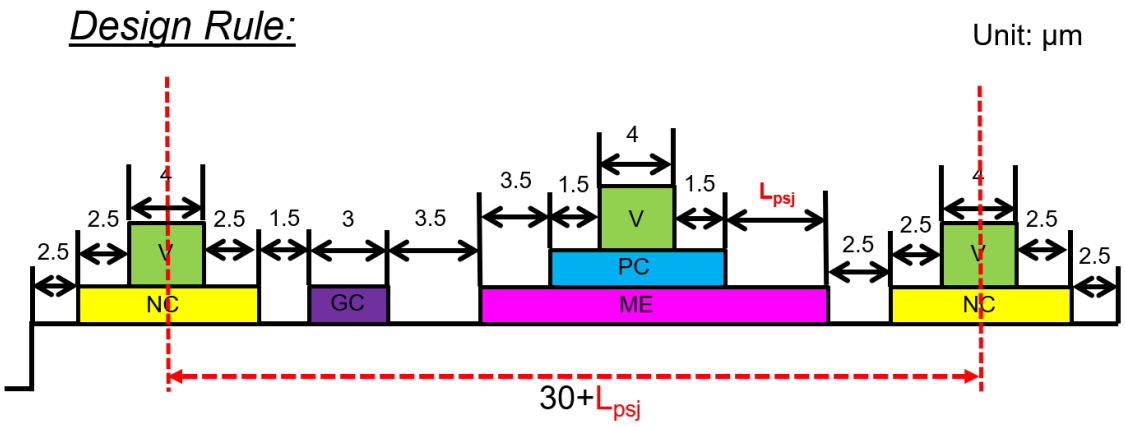
Sub. Lev	+/- 1um
Same level	+/- 2um
Mis/lev	+/- 1um / level
L1-L2 +/- 1um	L1-L3 +/- 2um
L1-L4 +/-3um	

(a)

Design Rule:



(b)



(c)

Figure 3.15 (a) Alignment Sequence (b) Feature size of OG PSJ basic cell (c) SG PSJ basic cell.

AM, NC and PC are regarded as the reference layers for Levels 2, 3 and 4 alignments. When a layer is aligned to the reference layer for alignment, at an introductory level, the maximum physical misalignment is ± 1μm (e.g., ISO to AM or PC to NC). At the same level, the maximum misalignment between different layers is ±2.0μm (layer GI and layer ME). Between a layer and a non-reference layer, the misalignment is ±3.0μm (ME (level 2) and PC (level 3). Such an alignment sequence ensures that misalignment between critical layers could be kept at minimal values.

The alignment mark layer based on alignment sequence design is presented in Figure 3.16.

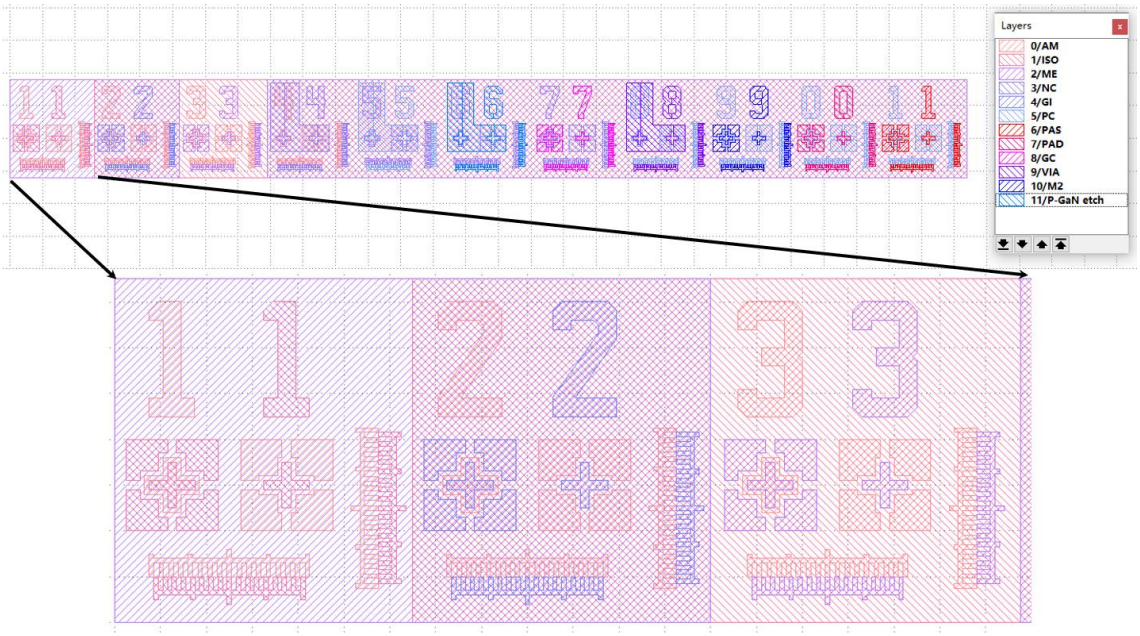
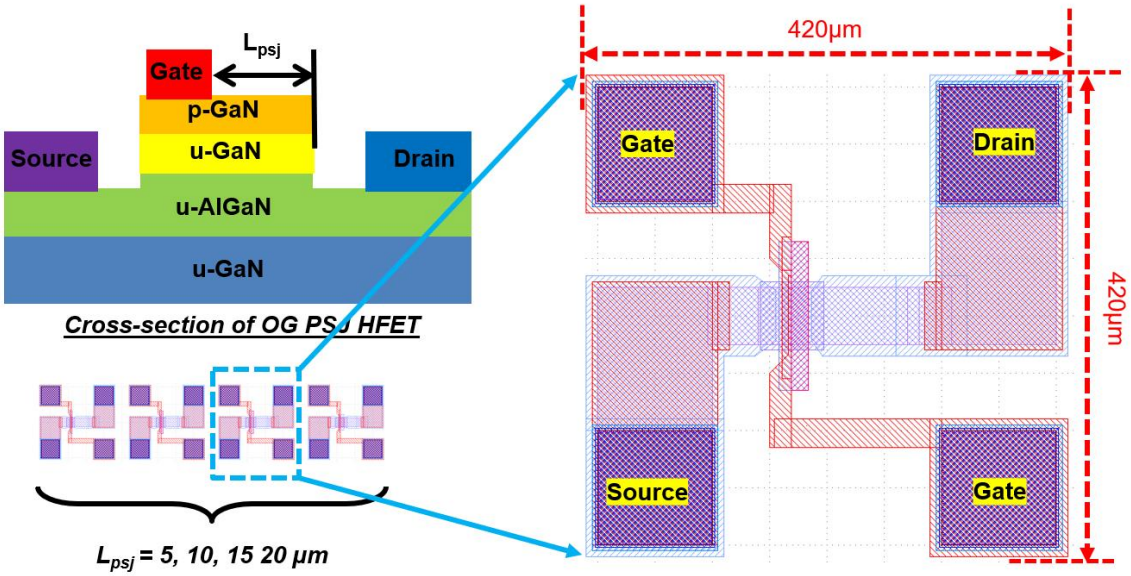


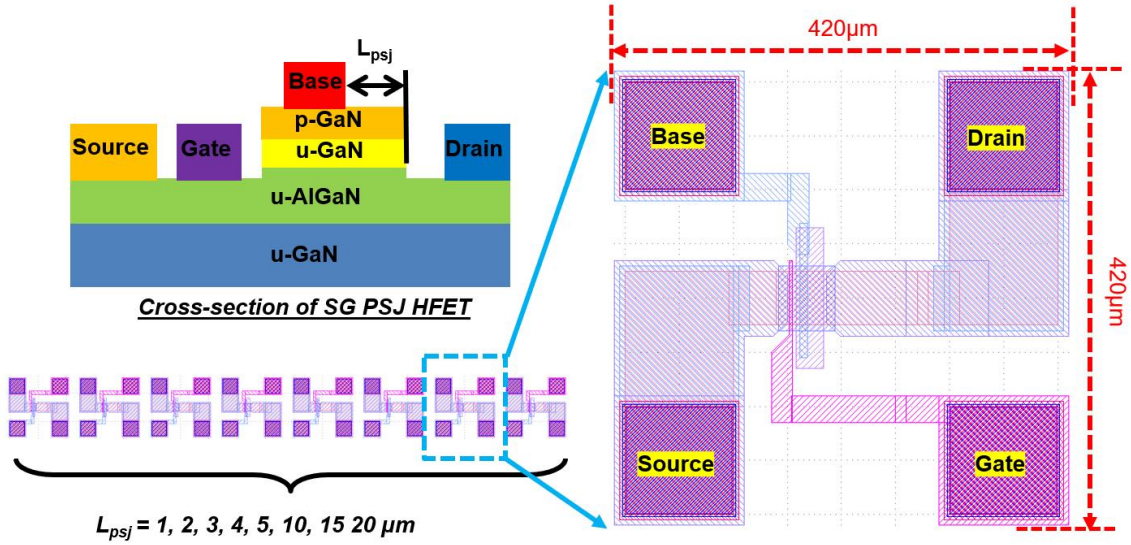
Figure 3.16 Mask Alignment.

The vernier scales are used to estimate and control the misalignment in both lateral and vertical directions in the photolithography process. The tones or polarities definition of the masks is separated into Light Field and Dark Field. Light Field mask tones are primarily transparent, and drawn features are opaque. Most areas in the Dark Field mask set are opaque, and drawn features are clear opposite Light Field. Because of the limitation of the fabrication facility in Sheffield, positive photoresists are used during the process.

Figure 3.17 is the top-view of OG and SG PSJ HFETs test structure. Device test structures also include Conventional GaN-based HFETs, PSJ and PN Diodes.



(a)



(b)

Figure 3.17 Mask layout for test (a) OG PSJ HFETs (b) SG PSJ HFETs.

The p-type and n-type TLM group are presented in Figure 3.18. The design also includes a few more the test structures.

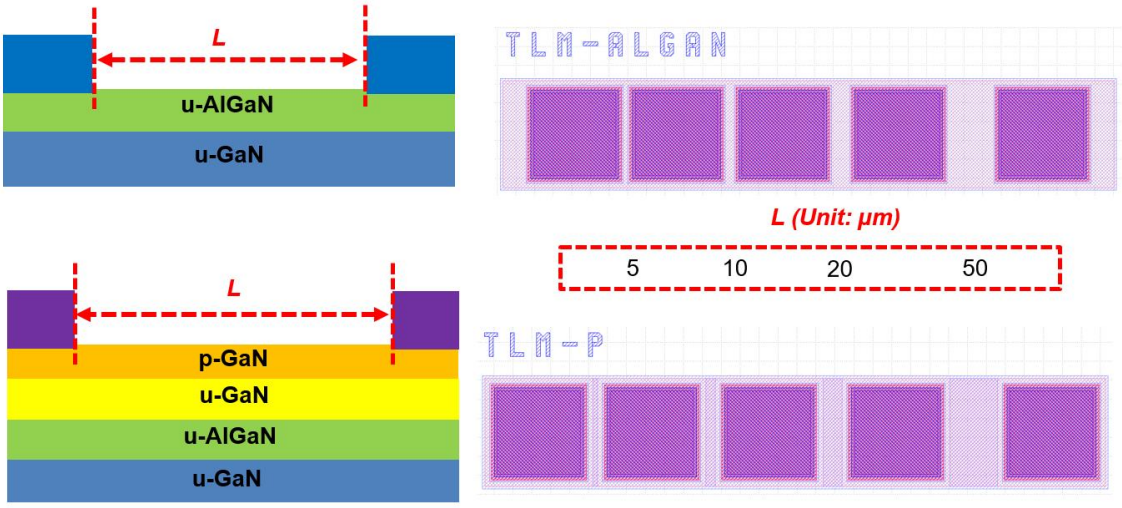


Figure 3.18 TLM structures.

The final GDS files layouts for processing at both locations are as presented in Figure 3.19, a square of 20mm*20mm.

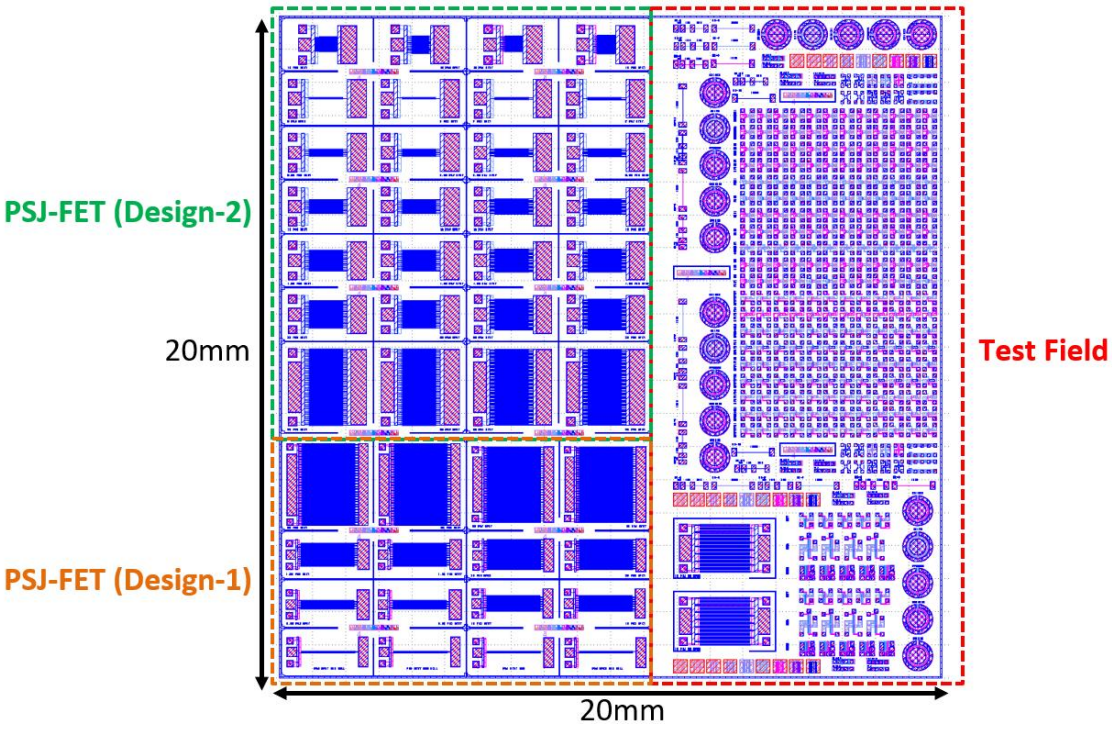
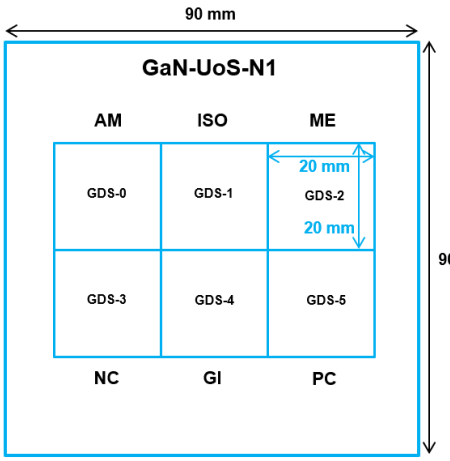


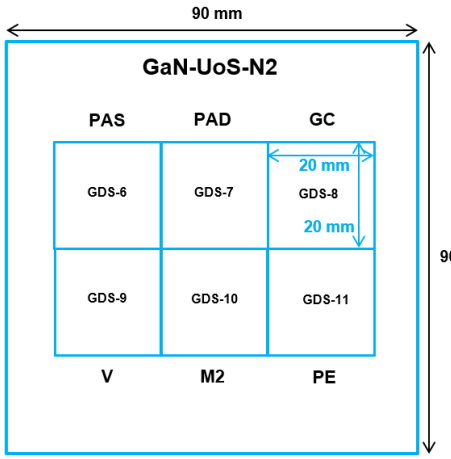
Figure 3.19 Final photomask layouts.

Based on Sheffield's facility (mask aligner), to minimise the number of photomasks and reduce costs, 6 layers are designed in the same mask set, as shown in Figure 3.20. All the GDS layers can be modified within two photomasks for processing at Sheffield.



Layer	Alias	GDS No.	Mask Tone
AM	Alignment Mark	0	Dark Field
ISO	Isolation	1	Light Field
ME	Mesa Etch	2	Light Field
NC	N Contact	3	Dark Field
GI	Gate Isolation	4	Dark Field
PC	P Contact	5	Dark Field

(a)



Layer	Alias	GDS No.	Mask Tone
PAS	Passivation	6	Dark Field
PAD	Pad	7	Dark Field
GC	Gate Contact	8	Dark Field
V	Via	9	Dark Field
M2	Metal 2	10	Dark Field
PE	P-GaN Etch	11	Dark Field

(b)

Figure 3.20 Layouts (a) Photomask N1 (b) Photomask N2.

3.5 PSJ Device Fabrication

In device fabrication process, as shown in Table 3.3, ten main steps are discussed in this section.

3.5.1 Wafer Layer Spcification

A u-GaN, a u-AlGaN and a u-GaN are grown by metal-organic chemical vapour deposition (MOCVD) on 4" Sapphire substrates and formed GaN/AlGaN/GaN hetero-structure. The sub-u-GaN layer with 0.8μm thickness is grown on a nucleation layer by epitaxial growth. The undoped AlGaN layer is 47nm with an Al concentration of 23%. The undoped GaN cap layer is 20nm. P-GaN cap layers are 17nm with $5\times10^{19}cm^{-3}$ Mg doping concentration and 3nm with $2\times10^{20}cm^{-3}$, as demonstrated in Figure 3.21.

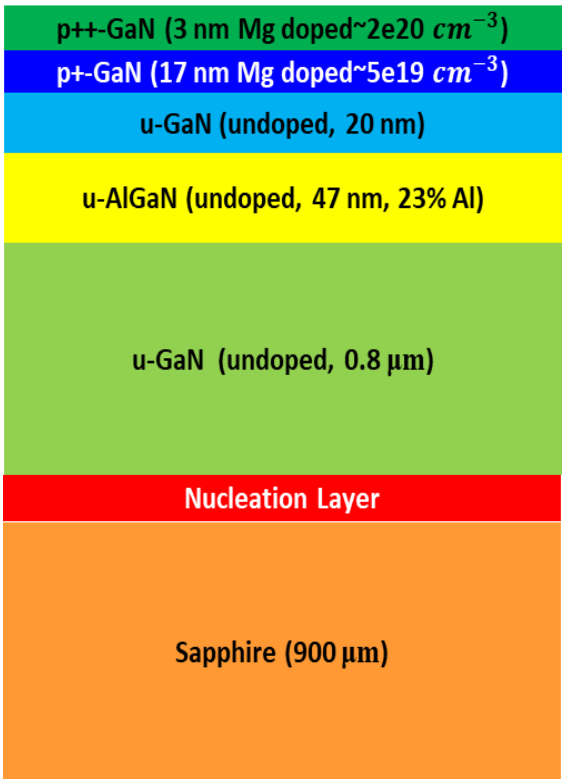


Figure 3.21 Specification of Sapphire substrate GaN PSJ wafer.

3.5.2 Preparation Work

All samples are diced from the 4" wafers with dimensions of 22mm×22mm. After the appropriate design and adjustment, 12 units can be worked out from one 4" wafer, as shown in Figure 3.22.

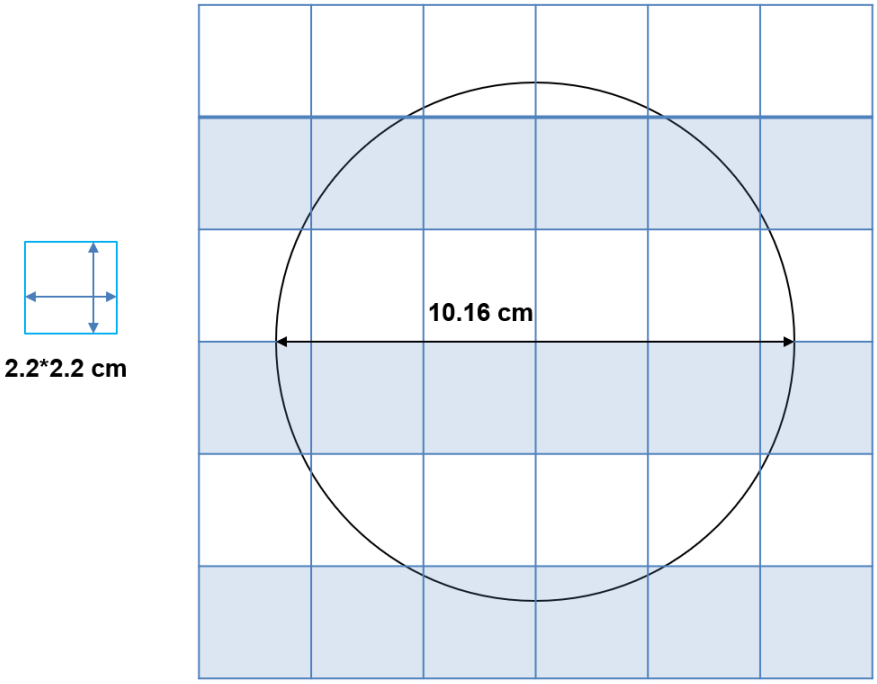


Figure 3.22 Dicing plan of Sapphire substrate GaN PSJ wafer.

The processing is performed on such diced units. The smaller units can be utilized as test samples for each step of optimization to maximum usage of the offcut. As a standard procedure, the first step in all device fabrication work is to guarantee an ultra-clean surface to avoid contaminants. In Sheffield cleanroom, a regular 3-step cleaning procedure is introduced.

3-step cleaning: The sample carefully proceeds in the following order

1. Samples should be in n-Butyl Acetate for 30s and put on the hot plate at 100 ^{0}C temperature
2. Then move to Acetone for 30s
3. Finally is Isopropyl Alcohol (IPA) for 30s
4. The sample should be dried through N_2
5. 3 steps above should be repeated until the sample is clean enough

This 3 step cleaning process is introduced throughout all fabricated processes.

3.5.3 Devices Photolithography

Photolithography is one of the crucial procedures in microelectronics fabrication because it governs the sample pattern and the implementation of all following steps, such as mesa etch and metallization. Carl Suss MJB3 UV300/UV400 is the facility used for photolithography in the fabrication process.

The first step is heating the sample on a 100^0C hot plate for 1 min. This step evaporates rudimental water or removes the remaining solvents from the 3-step sample clean process. SPR 350 or BPRS 200 is used as the photoresist according to the process. The sample is spun at a speed of 4000 rpm for 30 seconds to guarantee the photoresist is uniform (When deposited the photoresist on the insulating material such as Si_3N_4 or SiO_2, the adhesion promoter like Hexamethyldisilazane (HMDS) is necessary). After the spin process, the sample should be moved to a hot plate and heat for 1min to reinforce the stability of the photoresist. The following step is to load the sample in the mask aligner and expose it at an appropriate time. It is essential to adjust the exposure time according to the status of the equipment, layers thickness on the sample, surface geography, and an interface mechanism to the mask in the aligner. After the exposure procedure, develop samples for the developer (MF26A for SPR 350/ MF26A: H_2O=1:0.7 for BPRS 200) solution for 1 min. Then, samples should be moved to DI water for 30s cleaning. It should be noted that before Hydrofluoric (HF) acid wet etching, the additional baking step is essential for hardening the photoresist. When patterned for metallization, an oxygen descum step is typically employed after development before thermal evaporation.

3.5.4 Inductively Coupled Plasma (ICP) Etching

ICP etching is one of the standard dry etching methods in power semiconductor device fabrication. Fast etch rates, clean chemistries, vertical profile (anisotropy) and low device damage are considerable advantages for etching work. ICP etch is ideally suited to address these sustenances effectively since it gives high-density ions to contribute to etching rates fast while allowing separate control of ion density and

energy, giving a low damage capability. Oxford PlasmaSystem100 is the main ICP etching facility in the fabrication work [61].

Ar, Cl_2 and $SiCl_4$ are 4sccm, 15sccm and 1.5sccm, respectively, according to the instruction for etching a typical GaN layer through Oxford Plasma System 100 ICP etch system. RF power should be adjusted based on the fabricated process and ICP Power is the default setting (450W). In order to achieve high controllability of etching rate, lower RF power is more appropriate for the mesa etch process. The chamber pressure is the same as in the previous work (4mTorrs). The standard operation procedure of ICP etch is :

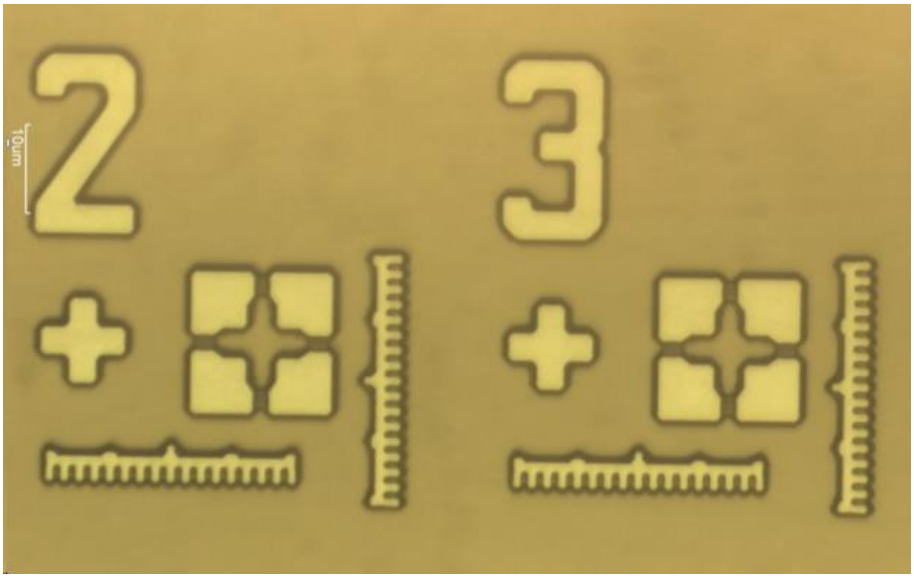
- A 20mins pre-running process is necessary to eliminate the contaminative gases or plasma caused by different settings, influencing the chamber ambience and subsequent etch steps. Therefore, this process can not be avoid and is strongly recommended before any etching progress.
- After a long-time etching process, the residual contaminant, coming from metamorphic photoresist, forms on the samples, which will impact the following steps such as the etching rate and the controlling of the etching thickness. Hence, it is crucial to remove the contaminant through the corresponding methods (). The carrier wafer should also be clean after an etching process for the same reason based on the standard operation rules of ICP etch.

Alignment mark, Device Isolation, and Gate Isolation use high-power ICP etch because of the lower precise requirement of etching depth compared with MESA etch process.

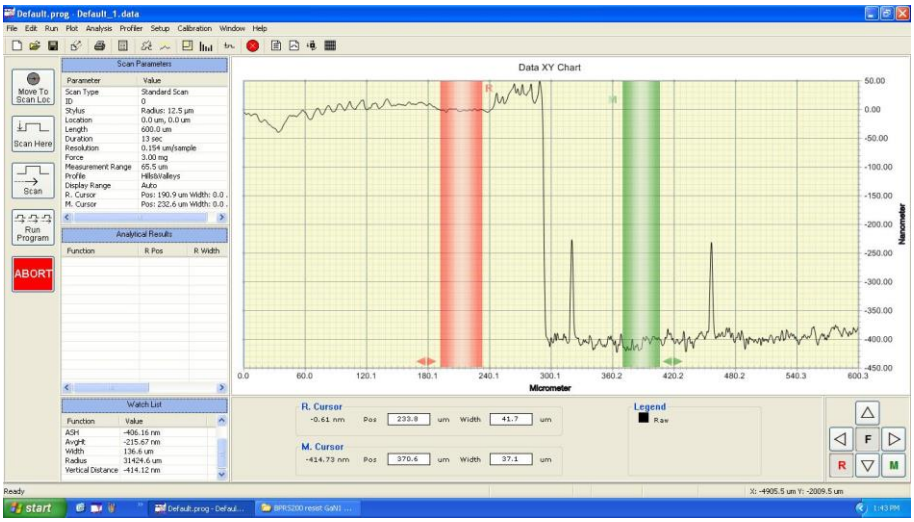
Alignment Mark

There are two main approaches to implementing Alignment marks, metal deposition and etching. Due to the facility limitations, etching on the sample surface is primarily adopted in the PSJ device fabrication process. Steps such as ISO, GI and ME are

etching processes. The alignment mark for these steps should be etching. Layers aligned to PC and NC need metallization alignment marks because these stages are metal formation. The ICP etching time and rate are based on previous fabrication work and are adjusted according to the practical test samples. After several attempts on the test samples, the etches depth should be controlled at around 400nm. Figure 3.23 presents the top-view of the etched alignment mark through a microscope with the etch depth at ~ 400-420nm, measured from Dektak.



(a)



(b)

Figure 3.23 (a) Alignment mark after ICP etching process (b) Detak measured etching results.

In the final practical samples, RF power is 75W, and the total etch time 9mins, based on the test etching rate of 45nm/min.

Device Isolation, Gate Isolation and Mesa Etch

Isolation Etch, Gate Isolation Etch and Mesa Etch employ a two-stage etch recipe on ICP. Low RF power etching is easy to control the rate. It also benefits the uniformity by minimising the surface damage from a material crystal perspective. At the same time, striking plasma with low RF power is complex. Therefore, the whole step is separated into two stages and starts at a reasonably high RF power and reduce to low power once the Plasma is stable in stage 2. The recipe of the standard 2-stage etch process is:

Stage 1

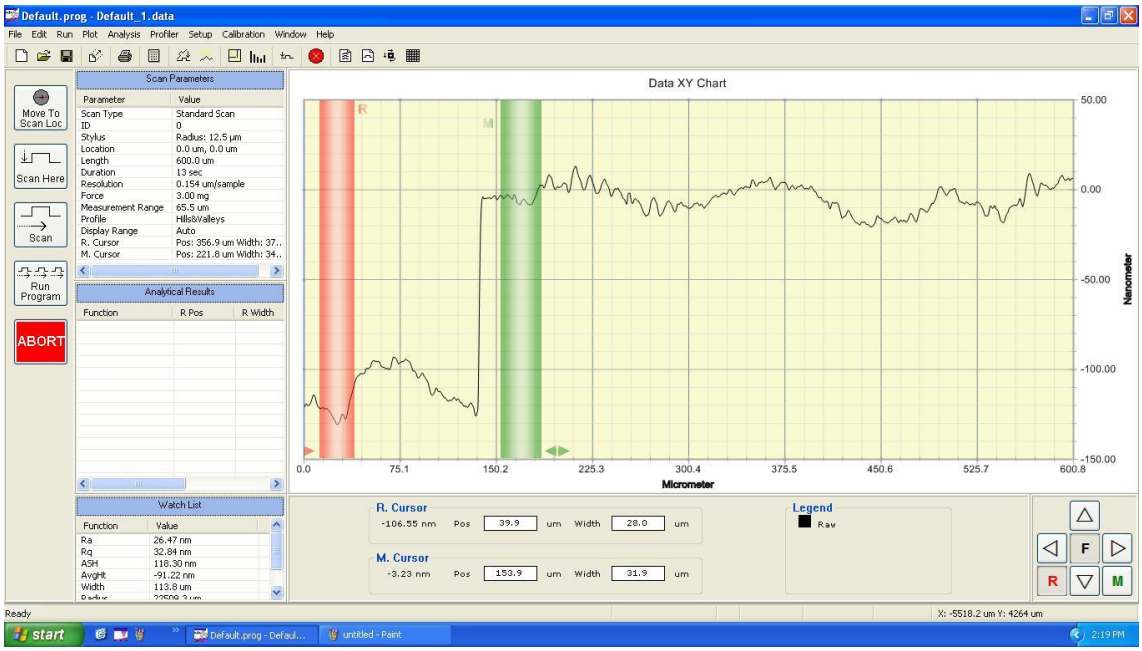
- The first stage needs to set the RF Power as 40W for 10s
- The Strike Pressure is 20 mTorrs
- The ramp is used as 4 s^{-1}

Stage 2

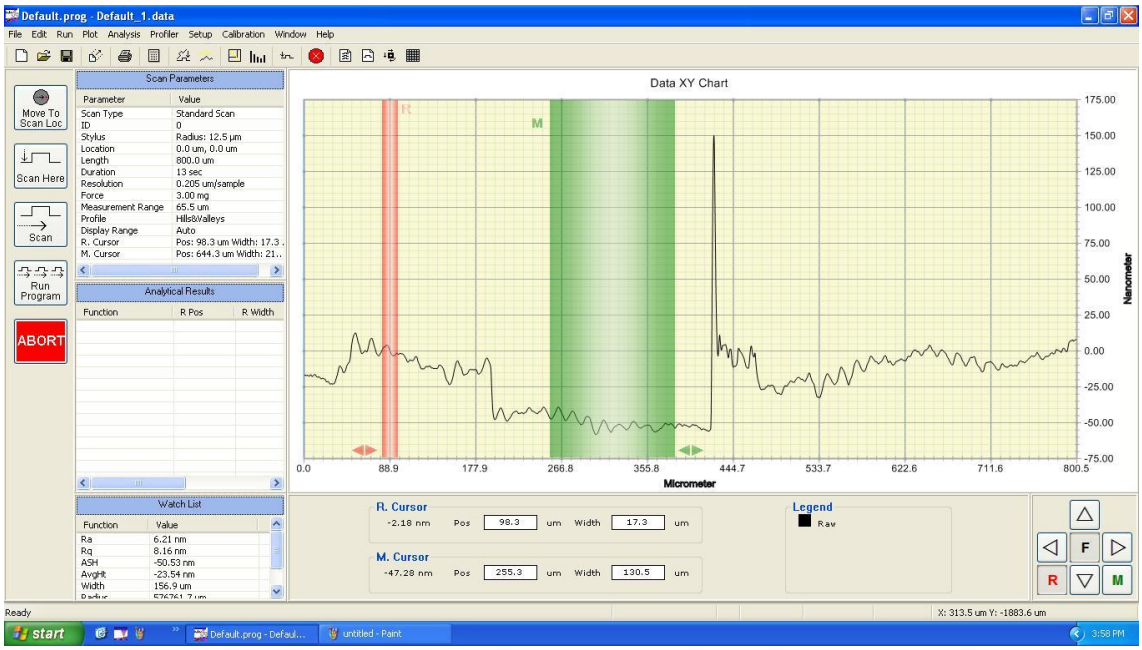
- In the second stage, the RF Power is set at 40W at the beginning 10s and then reduced to 10W with stable Plasma.
- Usually, the uniform etching rate happens as maintained RF power between 10~20W in this step (based on the equipment and test etch rate within the same day).

Several test samples are proceeded to optimise the isolation and mesa etch. Same with AM step, test samples are introduced to find the suitable etching time and rate, the etch depth should be controlled at around 65nm as precise as possible in mesa etch. Figure 3.24(b) presents mesa etch depth is ~ 55-65nm, measured by Dektak surface profilometry. It should be noted that the test etching rate only valid on the same day.

p-GaN sample is with isolation etch 120nm and followed by 150nm SiN PECVD device isolation process, Gate Isolation etch and ICP mesa etch. The isolation etch rate is 7.0nm/min and mesa etch rate is also 7.0nm/min as shown in Figure 3.24.



(a)



(b)

Figure 3.24 (a) Device isolation etch (b) Mesa etch.

The recipe of ICP etch (AM, ISO, GI and ME) is shown in Figure 3.25

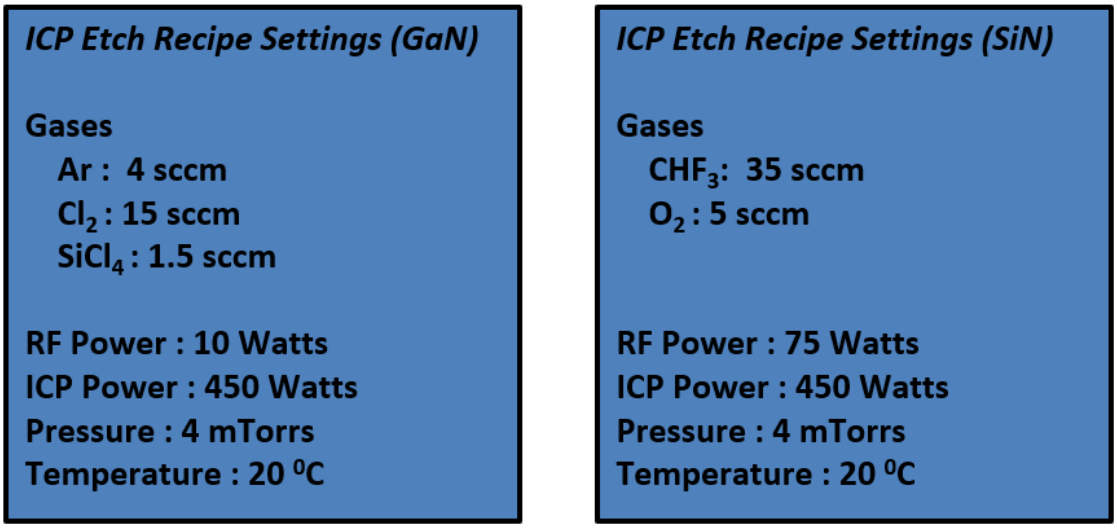


Figure 3.25 ICP etch recipe for different materials.

3.5.5 Plasma Enhanced Chemical Vapor Deposition (PECVD) and Dektak

PECVD is an approach generally utilized in power semiconductor device fabrication for thin layer deposition of diverse materials. The whole deposition process is realized through employing the reactant gases between different electrodes. One is connected to the ground, and the other is animated with RF power. Reactant gases activate and convert into the plasma state when capacitive coupling happens. This triggers a chemical reaction between the gases. The result is the product of the reaction to deposit on the substrate on the grounding electrode. Dektak is employed in tandem with PECVD to measure the deposited film thickness.

PECVD is introduced in the fabrication process for device isolation (Si_3N_4) and gate isolation as well as the final dielectric deposition for passivation (SiO_2). Initially, Silicon test samples are used to optimize the deposition time, and the same is eventually used to determine the deposited layer thickness using ellipsometry. Hence a Silicon Test sample is run simultaneously with GaN test samples as well as device samples. Thickness measurement is then performed on the test samples using Veeco Dektak 150.

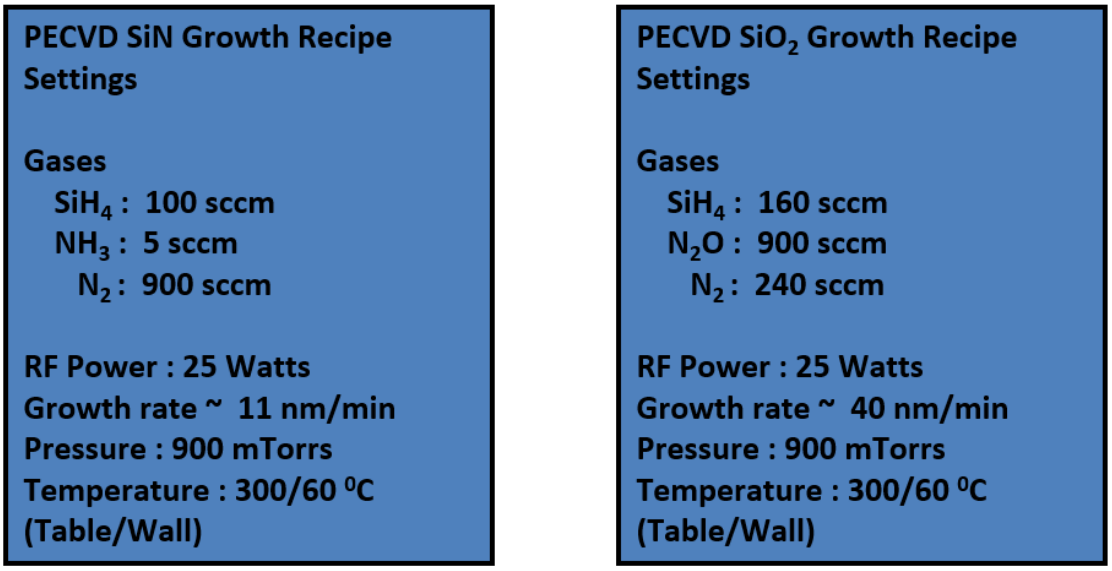


Figure 3.26 PECVD growth recipe for different material.

The recipe for PECVD growth is shown in Figure 3.26.

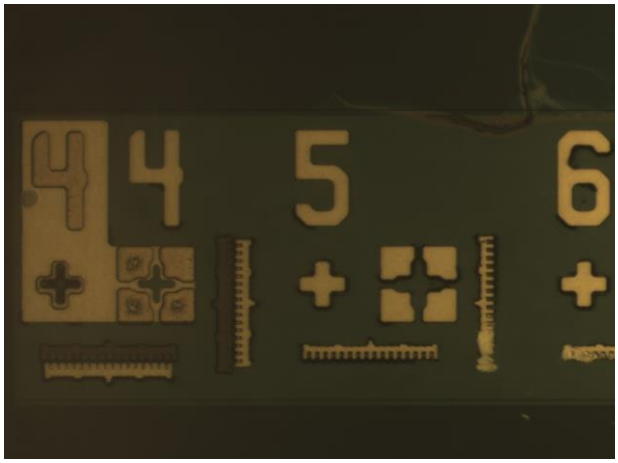
3.5.6 Thermal Evaporation and Lift-off Process

Thermal evaporation, Edwards Coating System E306A, is the primary methodology for metallization combined with the lift-off process, especially in III-V group semiconductor device fabrication. Ti, Al, Ni, Au... are employed to realize the formation of the metal electrodes. The left-off process removes the additional material since it is hard to etch the metal. The primary steps for thermal evaporation based on the instruction are:

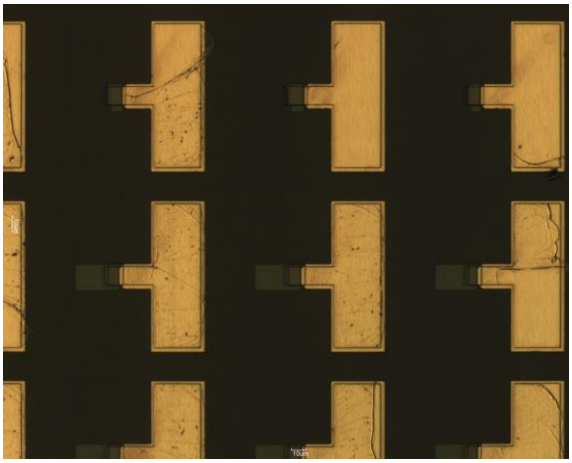
1. Fire off the coil with the current level.
2. For evaporation, the coil and source metals are dipped and boiled in n-butyl acetate for at least 1 minute to eliminate contaminants and boiling. The sample should also be immersed in HCl:H_2O with the ratio of 1:1 solution for 30s, then moved to de-ionized water (DI water) and dry up. After this process, the clean samples can be placed in the chamber.
3. The next stage is loading the coils, source metals, and the samples into the evaporator chamber. The chamber should be pumped down to vacuum at least

4×10^{-6} mTorr level. The amount of loading source metal is calculated before loading into the coil as the amount is directly related to the thickness obtained.

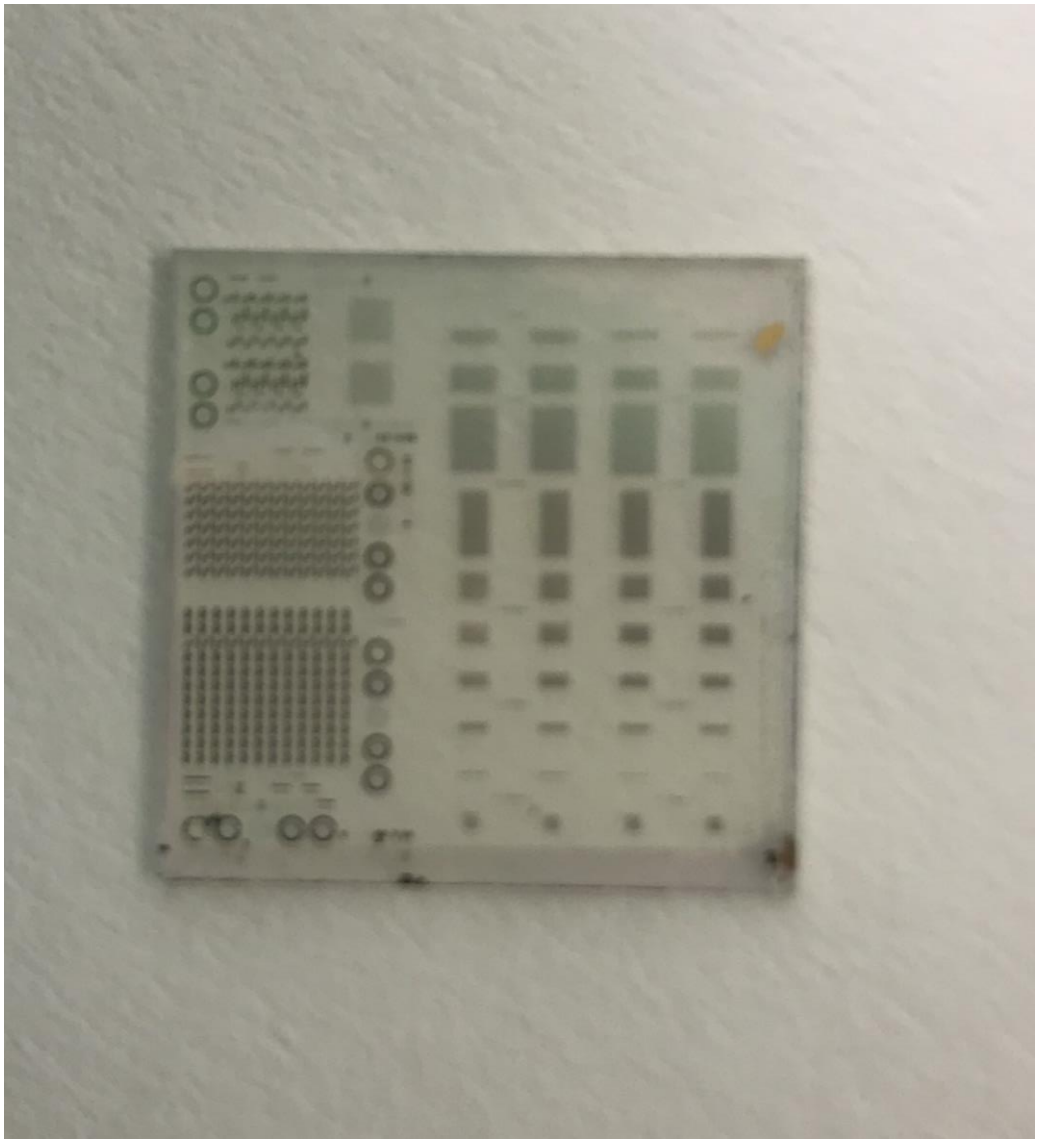
4. Slowly increase the current until the metal in the coils starts to melt. Typically, the current when the metal begins to melt is between 20A and 40A. Ni and Ti start to melt at about 30-40A. When the metal is Al and Au, the current is 20A. The crystal monitor is utilised to measure and control metal deposition thickness. Followed the calibration diagram in the cleanroom when loading the appropriate amount of the source metal of the amount relative to consistency. The increasing rate should be managed at 0.3-0.6nm/min (For Al and Au, the rate is around 0.9-1.1nm/s. For Ni and Ti, the pace is around 0.2-0.4nm/s).



(a)



(b)



(c)

Figure 3.27 Devices after N type metallization.

The photoresist should be at least 1.5 times the deposited metal's total thickness, typically 2 times in order to have a better lift-off and patterning process. The whole evaporate process is:

1. Spin the PMGI.
2. Hot-bake:180°C for 7min
3. Spin resist 350
4. Hot-bake:100°C for 1min
5. Exposure

6. Developer(for resist 350) for 1min
7. Evaporation
8. Lift-off(EKC830) overnight

Post evaporation, the sample is left in Acetone for > 10-12 hours. The dissolution of the photoresist achieves metal lift-off by Acetone, Resist Remover or EKC830. Source and Drain is n-type Ohmic contact. The base electrode is p-type Ohmic and Gate is Schottky contact. Thermal Evaporation is introduced for all these steps as well as the second metal deposition.

3.5.7 Rapid Thermal Annealing (RTA) for Ohmic Contacts

RTA is necessary to form Ohmic contact after the thermal evaporation process in GaN-based devices. High-temperature annealing results in low contact resistivity intermetallic phase formation at the metal-semiconductor interface. The metal stack employed for n-contact is Ti/Al/Ni/Au (20/100/45/55 nm). The RTA condition is 1 minute with a temperature of 800 ^{0}C in N_2 ambient. Combining the research works of Ohmic contact for p-GaN [62-67] and available facilities in Sheffield, the method of 20nm Ni followed by 200nm Au (20/200 nm) is adopted for p-contact metal. 10 minutes with a temperature of 500 ^{0}C in air ambient (80%N_2 + 20%O_2) is the RTA condition for a better p-contact in GaN.

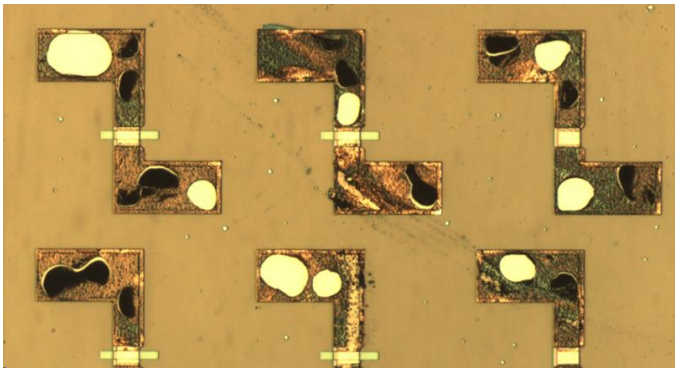
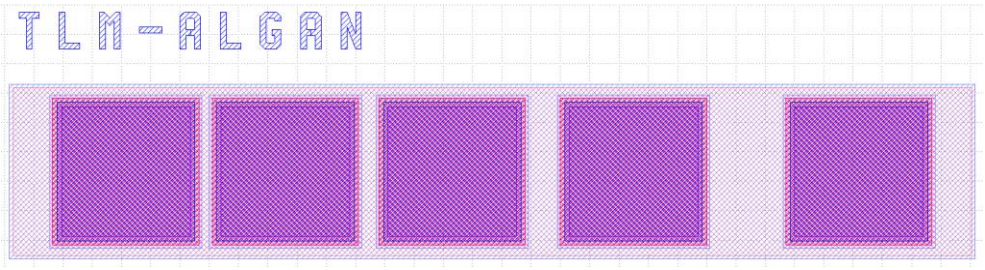


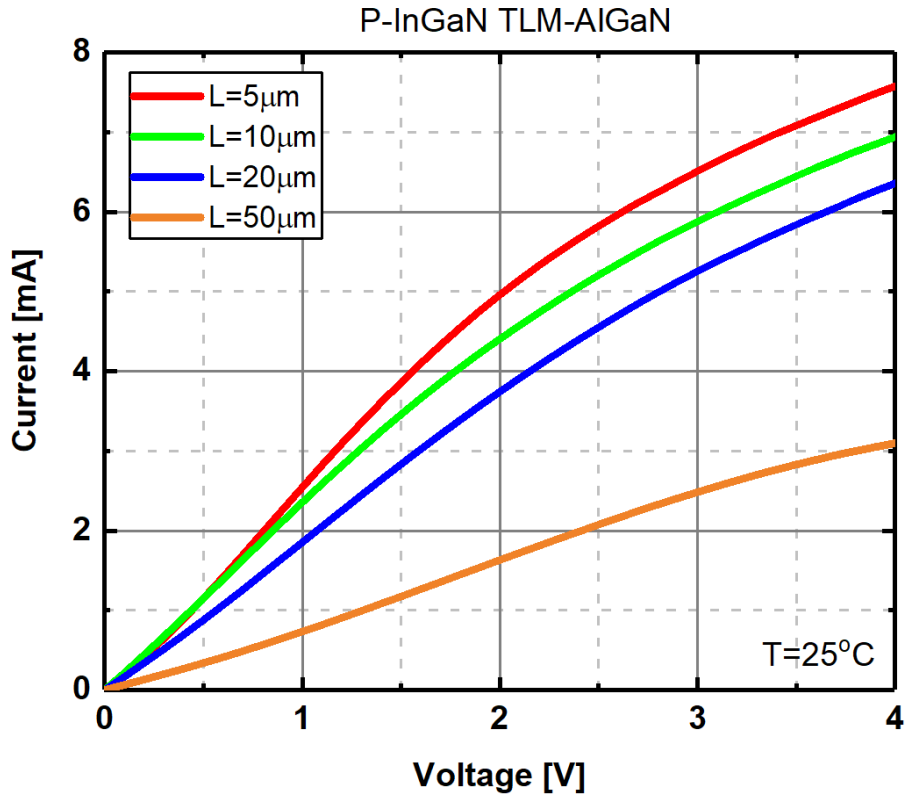
Figure 3.28 n contact RTA with condition of 850 °C in N_2 for 1 min.

Ti/Al/Ni/Au (20/55/45/55 nm(crystal monitor), ideal case is 20/100/45/55 nm, The actual thickness of the deposited metal is around 183nm(from Dektak). (The Al

lengths is higher than the preferred value for the requirement of the thickness of 100 nm.)some peaking area is higher than 3000nm, which may significantly impact the next step. Therefore, the disparity between the Evaporator crystal monitor and DEKTAK profilometry readings is apparent. Transmission Line Model (TLM) test patterns designed in fabricated samples are employed to investigate Ohmic contact characterization and the contact resistivity [68]. The best results for n-contact resistivity are 8.62 x 10^{-4} Ω·cm² and p-contact is 4.11 x 10^{-2} Ω·cm² from TLM pattern measurements, shown in Figure 3.34 and Figure 3.31, for the fabricated units at Sheffield. In Powdec KK test sample, the best n-contact resistivity is 4.62 x 10^{-6} Ω·cm² and p-contact is 1.20 x 10^{-3} Ω·cm².



(a)



(b)

Figure 3.29 (a) n contact TLM Patterns (b) I-V measurements.

As shown in Figure 3.30, GaN PSJ samples after RTA process are performed.

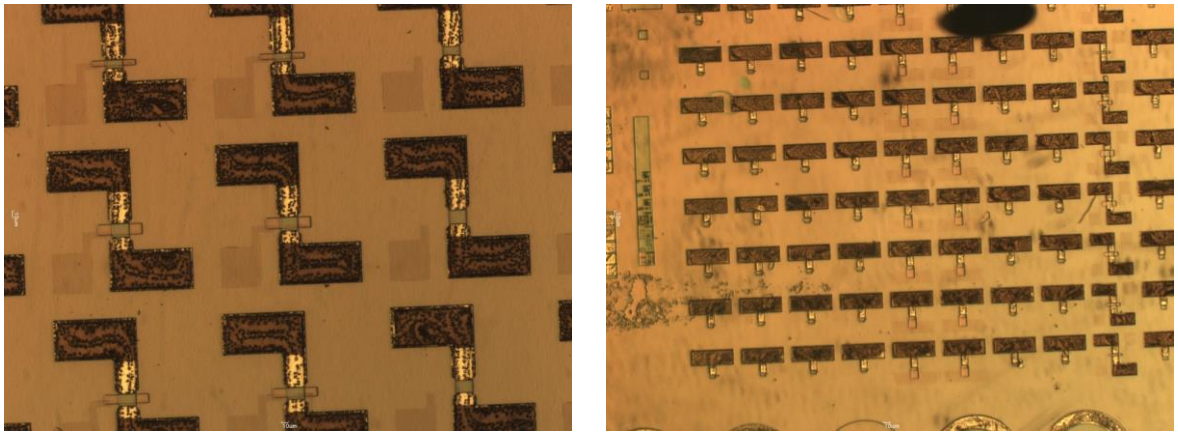
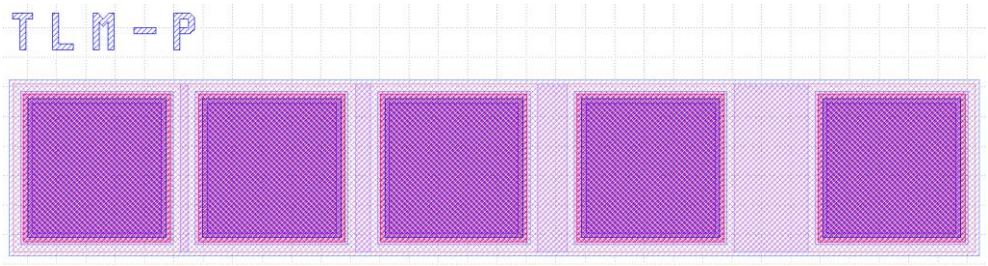
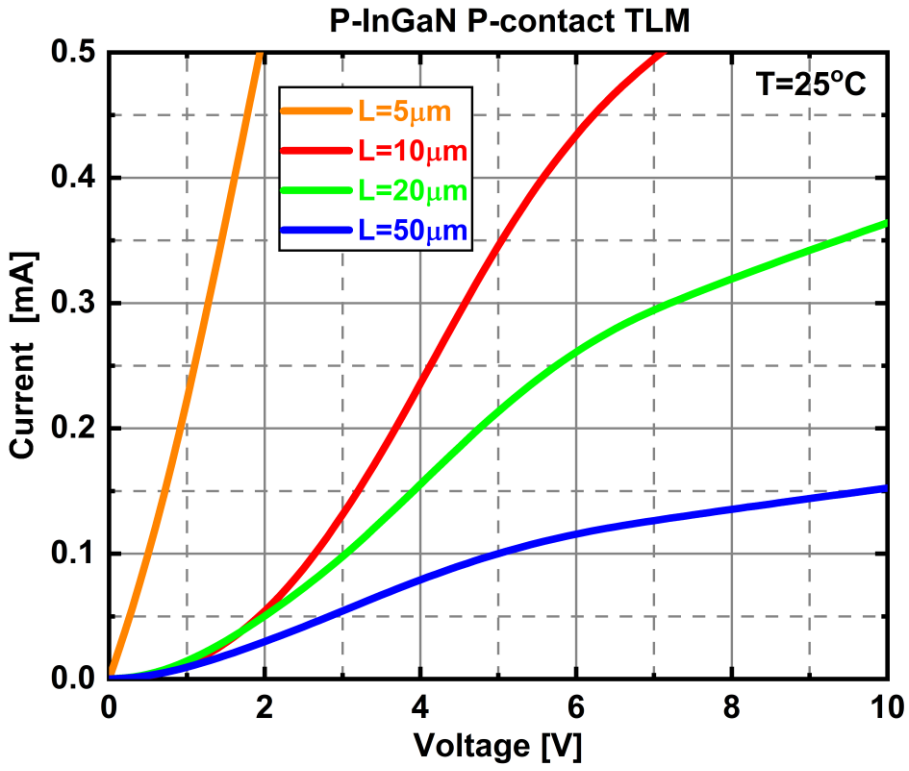


Figure 3.30 p contact RTA with condition of 500 °C in Air (O_2 20% and N_2 80%) for 10 min.

The total thickness of Ni/Au/Ti/Au=10/10/20/145 is 185nm(from the crystal monitor). And the actual thickness is around 180 nm (from DEKTAK)



(a)



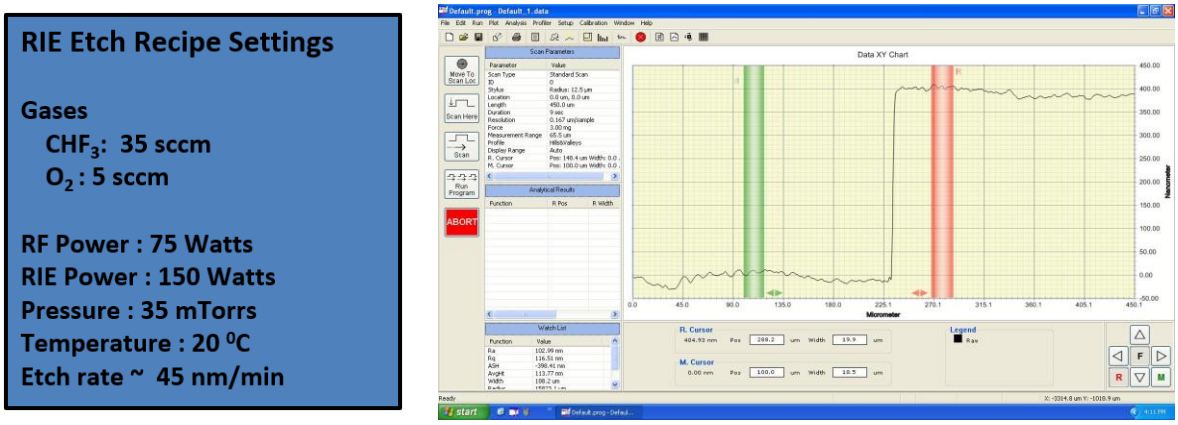
(b)

Figure 3.31 (a) TLM designs for p contact (b) I-V measurements.

3.5.8 Reactive Ion Etching (RIE)

RIE is an etching technique used for micromachining. RIE etching is a dry etching and has different characteristics from wet etching. RIE uses chemically reactive plasma to remove the material deposited on the wafer. An electromagnetic field generates plasma under low pressure (vacuum). High-energy ions from the plasma attack react with the wafer's surface. Via etching employs the RIE method after Si_3N_4 insulation layer is deposited during Gate Isolation.

The actual GaN samples are etched after Si_3N_4 deposition at PECVD. The influence of non-uniformities should be considered, and the corresponding solution of over-etch for additional time is adopted. An over-etching is required to guarantee that the insulator layer is entirely eliminated from the surface to ensure the second metal is connected to the Source, Drain and Base first metal contacts.



(a) (b)

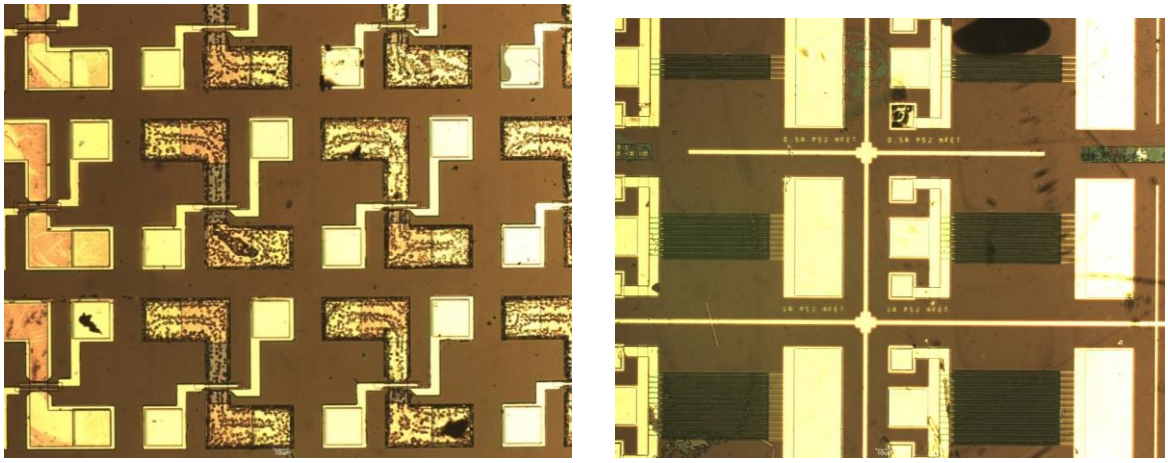
Figure 3.32 (a) RIE etch SiO_2/SiN Recipe (b) Post etch surface profilometry results of Via.

3.5.9 Second Metal Layer (M2)

In order to fix the crack in the first metal and connect fingers to the pad region, a second metal layer was deposited. Metal 2 deposition: Ti/Au(20/800 nm)(from crystal monitor) (The crystal monitor has some issues. Thus, the value is not very accurate). Because of the limitation of the evaporator in the cleanroom, the M2 layer is hard to reach 2μm. Hence, it is necessary to thicken the metal as much as possible in this process.

3.5.10 Fabricated Wafers and Devices

Figure 3.34 demonstrated the fabricated large-area GaN-based PSJ devices and process control management (PCM) test structures from one of the GaN on Sapphire samples at the end of the passivation layer deposition, which is the final step in the process flow.



(a) **(b)**

Figure 3.33 (a) Device test structures (PSJ FETs) (b) Large area PSJ FET.

The subsequent section summarises measurement results and a detailed analysis of the performance of the fabricated devices.

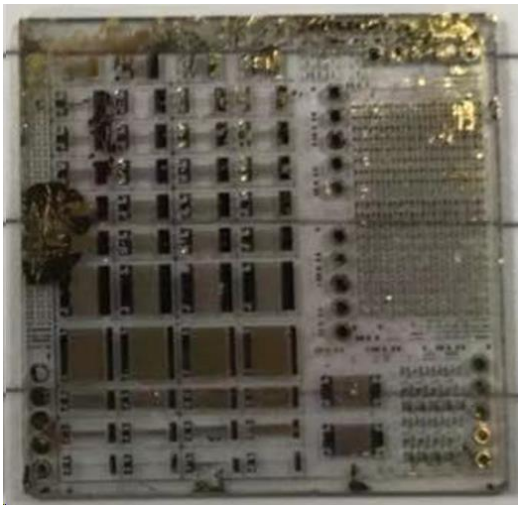


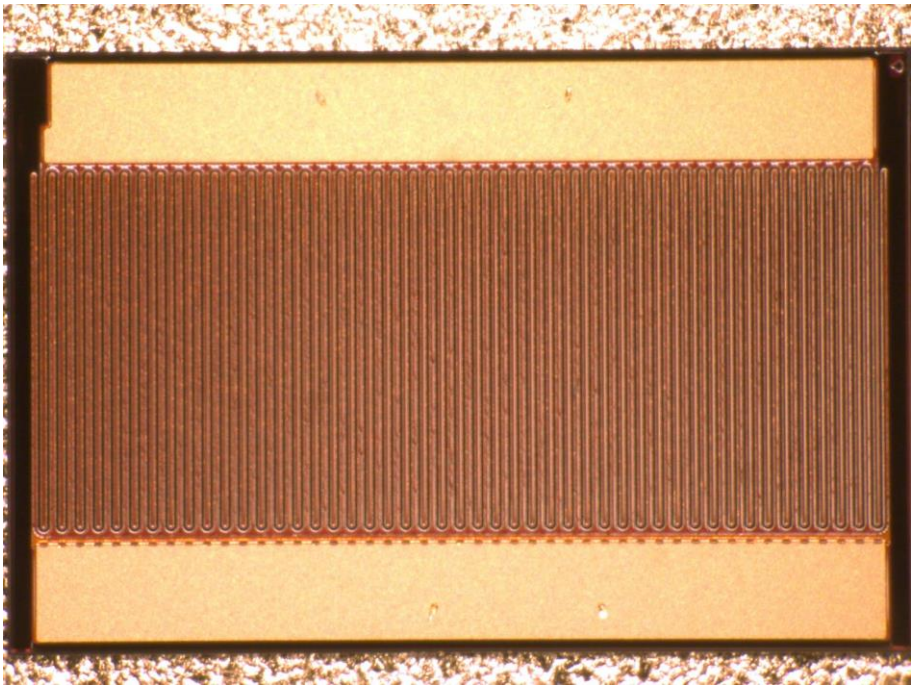
Figure 3.34 Fabricated p-GaN Sample.

3.6 Fabricated Devices Characterisation

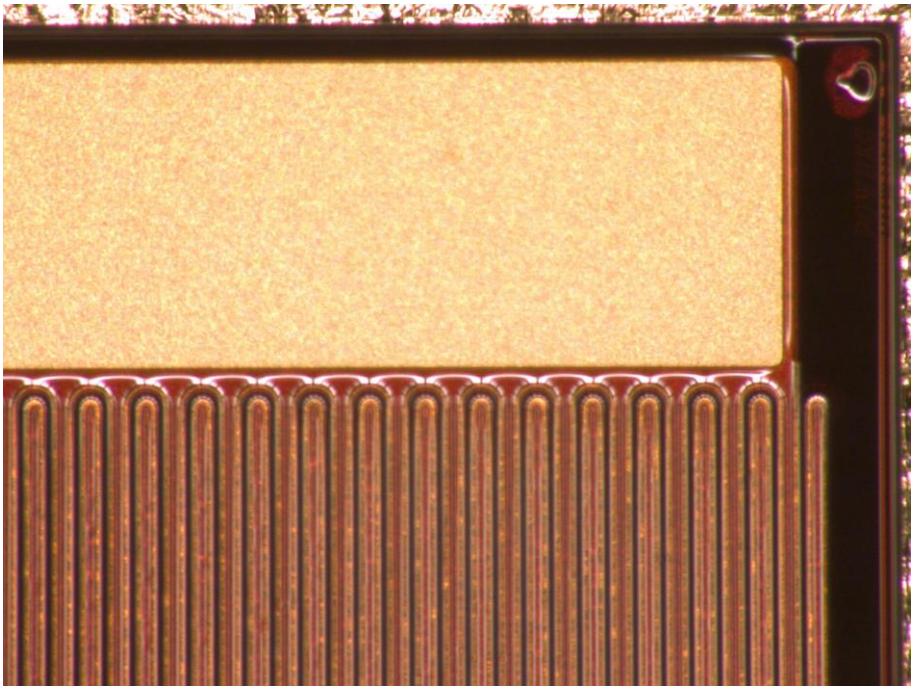
This section reports the performance and electrical characterization results of the various devices fabricated on Sapphire substrates at Sheffield and compared with devices manufactured in Powdec KK.

3.6.1 PSJ Diode Characterisation

The characterisation of PSJ diodes mainly focuses on hybrid types consisting of a conventional lateral PSJ Schottky diode and a GaN PiN diode fabricated by Powdec KK, as shown in Figure 3.35.



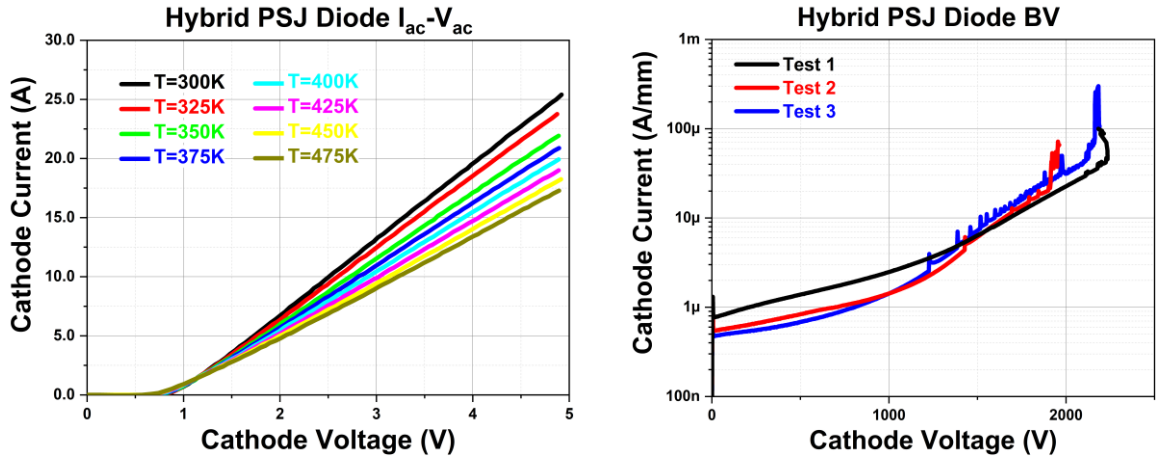
(a)



(b)

Figure 3.35 Top view photograph of Powdec KK 8A PSJ Diodes.

It consists of a p-type doped GaN cap layer (p-GaN) with $5\times10^{19}cm^{-3}$ Mg-doped, a 55nm undoped GaN layer, a 40nm AlGaN layer with 27% Al composition and an 800nm u-GaN sub-layer. Anode is Schottky contact to 2DEG forming a lateral Schottky PSJ diode and base is Ohmic contact to 2DHG forming a PiN diode.



(a) (b)

Figure 3.36 Measured 8A Hybrid PSJ Diodes (L_{PSJ}=20μm) characteristics of (a) I_{ac}-V_{ac} with different temperature (b) reversed I_{ca}-V_{ca}.

The 8A hybrid PSJ diode measured I_{ac}-V_{ac} characteristics under different temperature conditions and device blocking capability is shown in Figure 3.36(a) and (b), respectively. With the increase of temperature, the current reduces in measurement as expected. A typical PSJ diode with 20μm can support more than 2200V, and the critical electric field can reach 1.1MV/cm as predicted in the previous simulation.

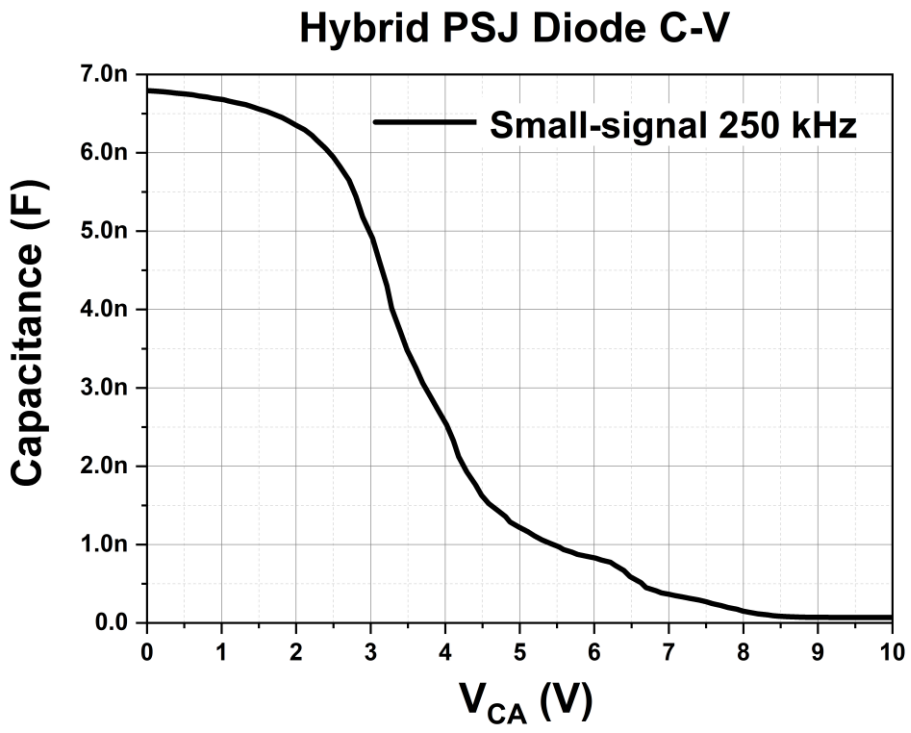
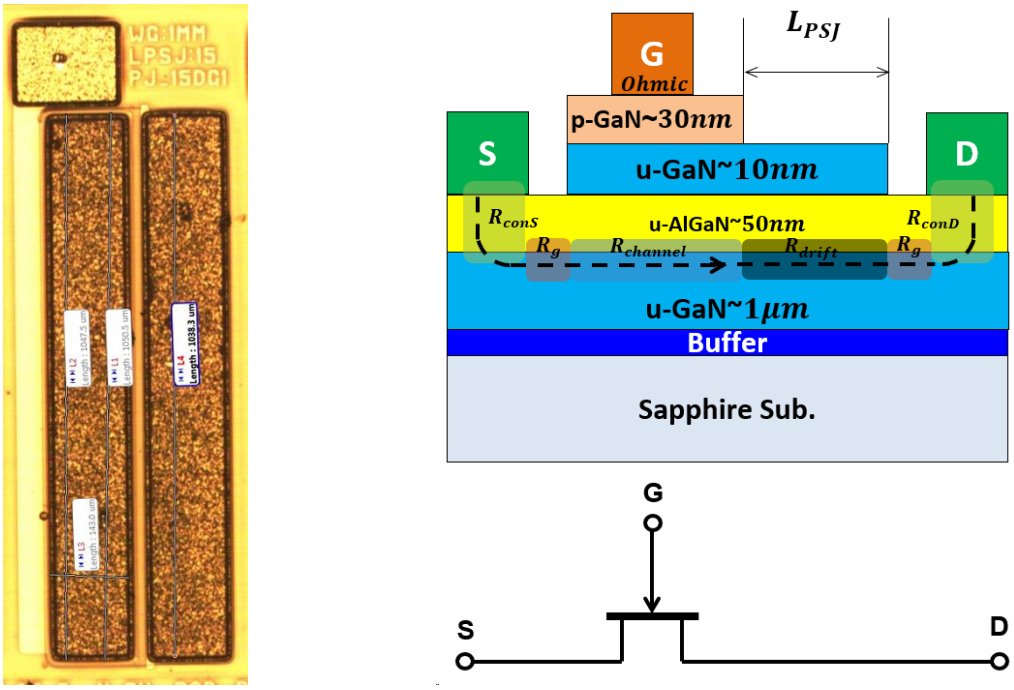


Figure 3.37 Small-signal capacitance measured at 250 kHz for a Hybrid PSJ Diode (L_{PSJ}=20μm).

Small-signal Capacitance Voltage (CV) measurements at 250 kHz are performed on a hybrid PSJ diode, as presented in Figure 3.37. With V_{CA} voltage swept from 0V-10V and 10V-0V. A hysteresis-like behaviour is primarily observed at the anode of the Schottky contact region due to crystallographic defects extending from the GaN layer to the Ni/AlGaN interface [69].

3.6.2 PSJ HFET Characterisation

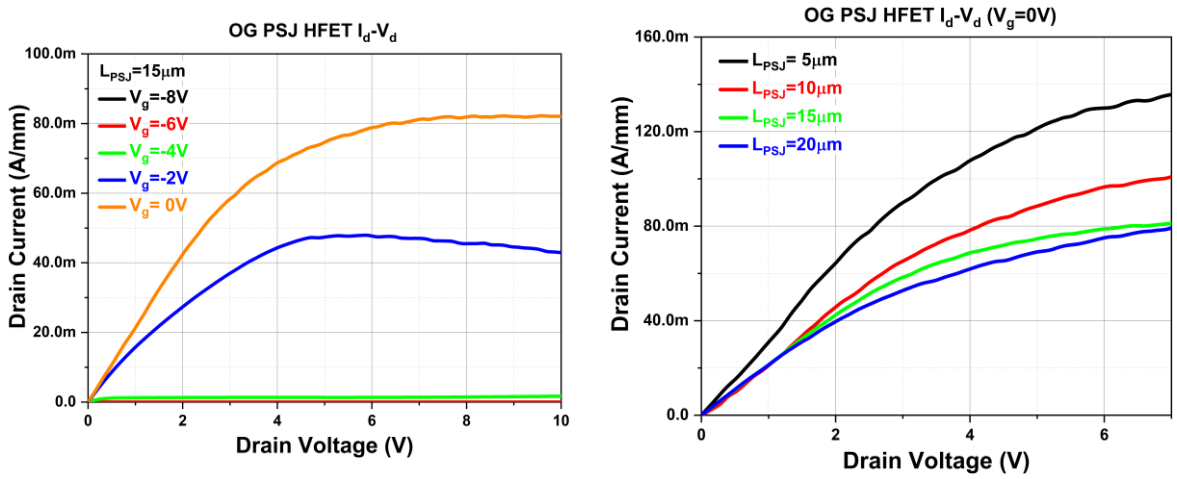
Figure 3.38 shows the top-view and cross-section of the Powdec KK OG PSJ HFET. AlGaN thickness in PSJ HFETs is set as 40 nm in the PSJ region and as 20 nm in the remaining access region between the source and drain electrodes. Al mole fraction in the AlGaN layer is fixed as 27% in both structures.



(a) (b)

Figure 3.38 Practical Ohmic Gate PSJ HFETs of (a) top-view (b) cross section.

Figure 3.39 shows the measured output I_d-V_d characteristics of the OG PSJ HFETs. With the increase of L_{PSJ}, $R_{(on,\,sp)}$ increases, which corresponds with the simulation results.



(a) (b)

Figure 3.39 Measured output I_d-V_d characteristics (a) with different gate voltage (b) with different L_{PSJ} at V_g= 0V.

Measured output I_d-V_g characteristics of the OG PSJ HFETs are demonstrated in Figure 3.40 (a) and measured temperature-dependent output I_d-V_d characteristics of the OG PSJ HFETs are shown in Figure 3.40(b). As shown in the simulation results previously, the threshold voltage of OG PSJ HFETs is around -5V. With the increase of temperature, $R_{(on, sp)}$ also increase, similar to the simulation results since the scattering rate is higher when the temperature is higher.

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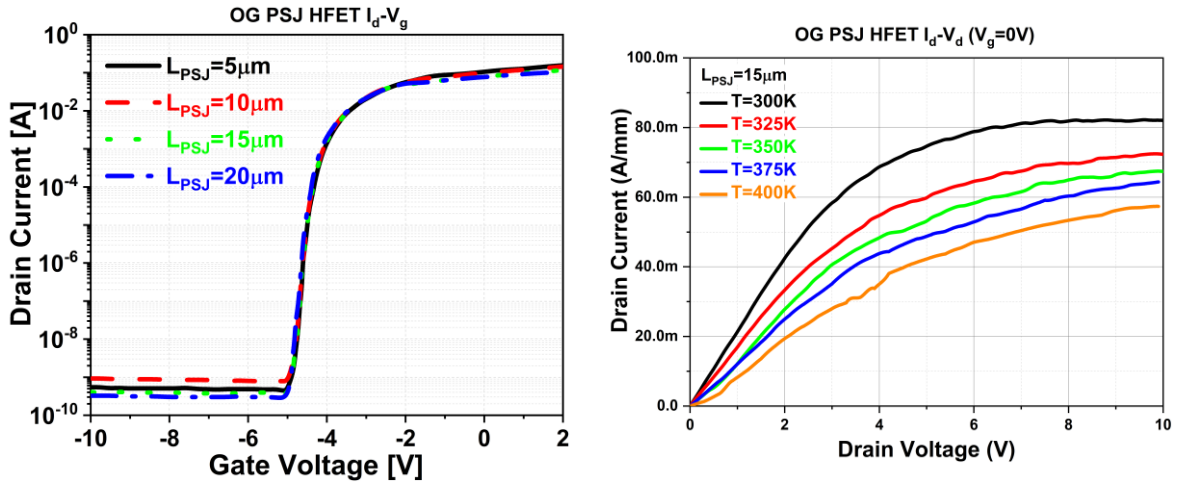


(a) (b)

Figure 3.40 Measured output (a) I_d-V_g characteristics of Ohmic Gate PSJ HFETs (b) temperature dependent output I_d-V_d characteristics of Ohmic Gate PSJ HFETs at V_g= 0V.

Measured off-state I_d-V_d characteristics of the OG PSJ HFETs are demonstrated in Figure 3.41. It proves that 15μm L_{PSJ} can sufficiently support more than 1500V.

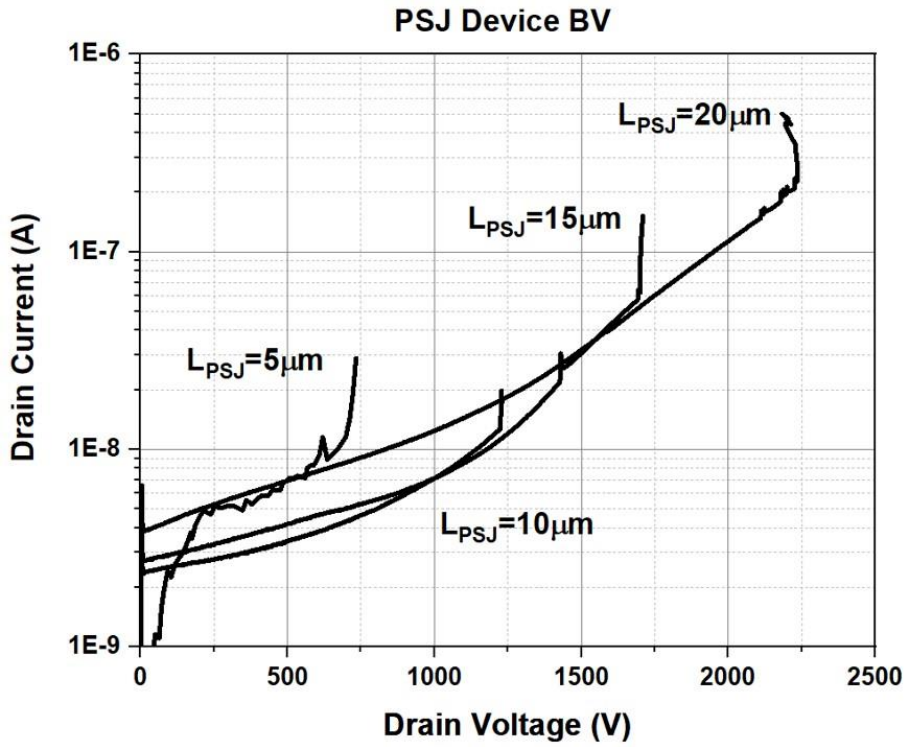
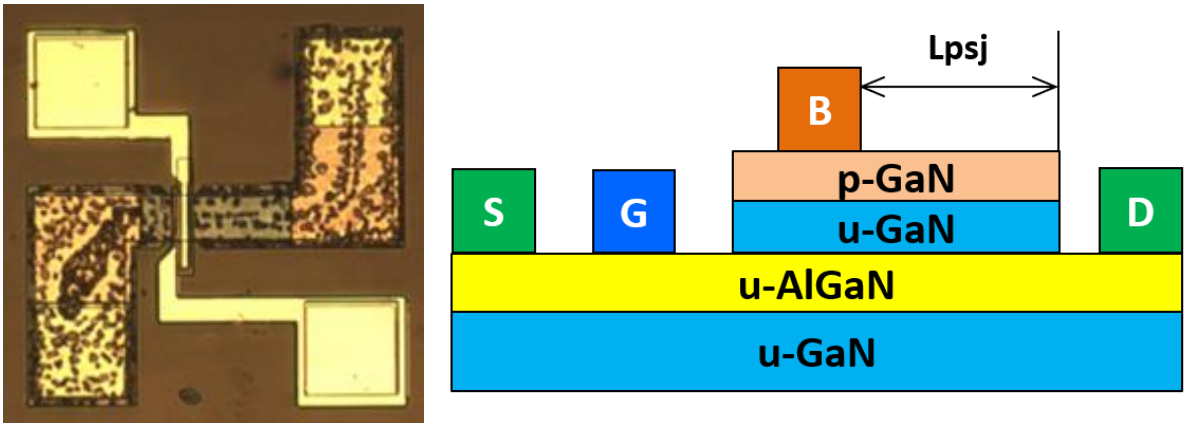


Figure 3.41 Measured off-state I_d-V_d characteristics of Ohmic Gate PSJ HFETs at V_g= -15V.



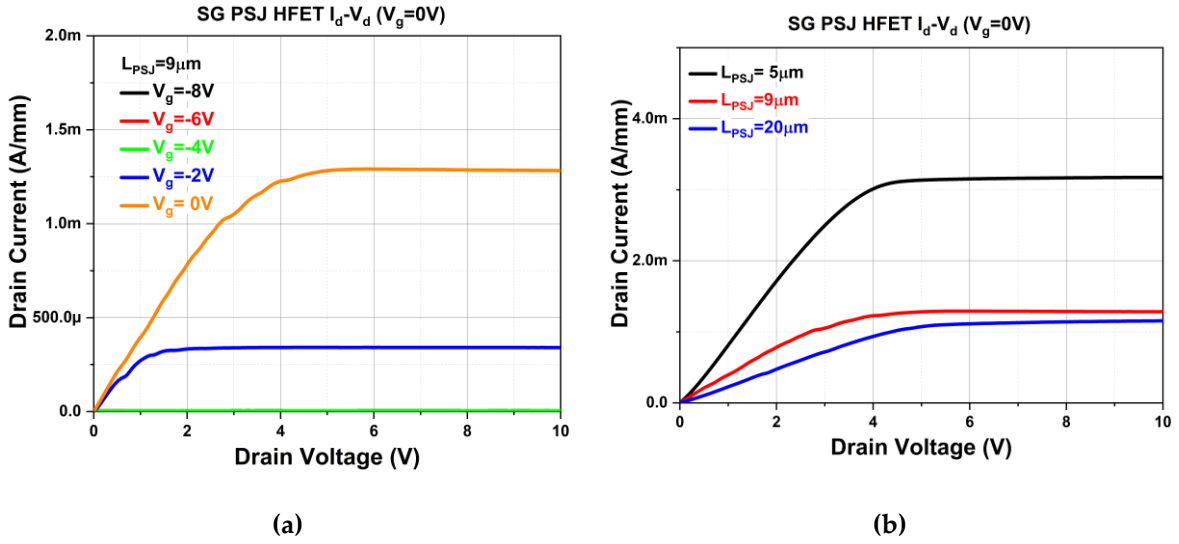
(a) **(b)**

Figure 3.42 Fabricated Schottky Gate PSJ HFETs of (a) microscopical view (b) cross-section of SG PSJ HFET.

Figure 3.42 shows the microscopical view and cross-section of the Sheffield fabricated SG PSJ HFET. AlGaN thickness in PSJ HFETs is set as 47 nm in the PSJ region and 22

nm in the remaining access region between the source and drain electrodes. Al mole fraction in the AlGaN layer is fixed as 23% in both structures.

Figure 3.43 shows the measured output I_d-V_d characteristics of the SG PSJ HFE**T.**



(a) **(b)**

Figure 3.43 Measured output I_d-V_d characteristics (a) with different gate voltage (b) with different L_{PSJ} at V_g= 0V.

Measured output I_d-V_g characteristics of the SG PSJ HFETs are demonstrated in Figure 3.44 (a) and measured temperature-dependent output I_d-V_d characteristics of the SG PSJ HFETs are shown in Figure 3.44(b). All the results are consistent with previously simulated results. The threshold voltage is -3V, which is higher than OG PSJ HFETs and proves the controllability of SG type gate is better than OG structure.

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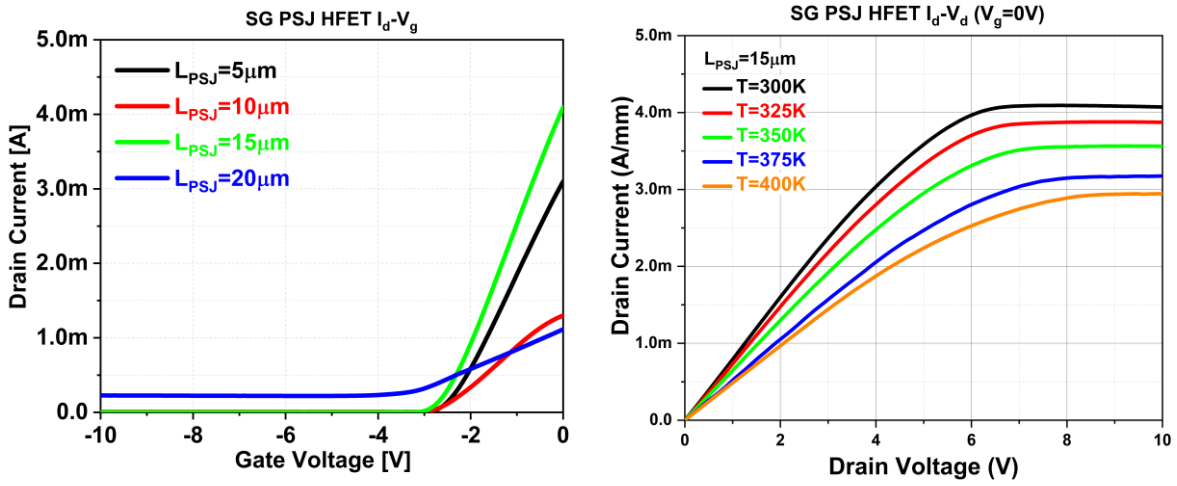


(a) (b)

Figure 3.44 Measured output (a) I_d-V_g characteristics of Schottky Gate PSJ HFETs (b) temperature dependent output I_d-V_d characteristics of Schottky Gate PSJ HFETs at V_g= 0V.

Measured off-state I_d-V_d characteristics of the SG PSJ HFETs are demonstrated in Figure 3.45.

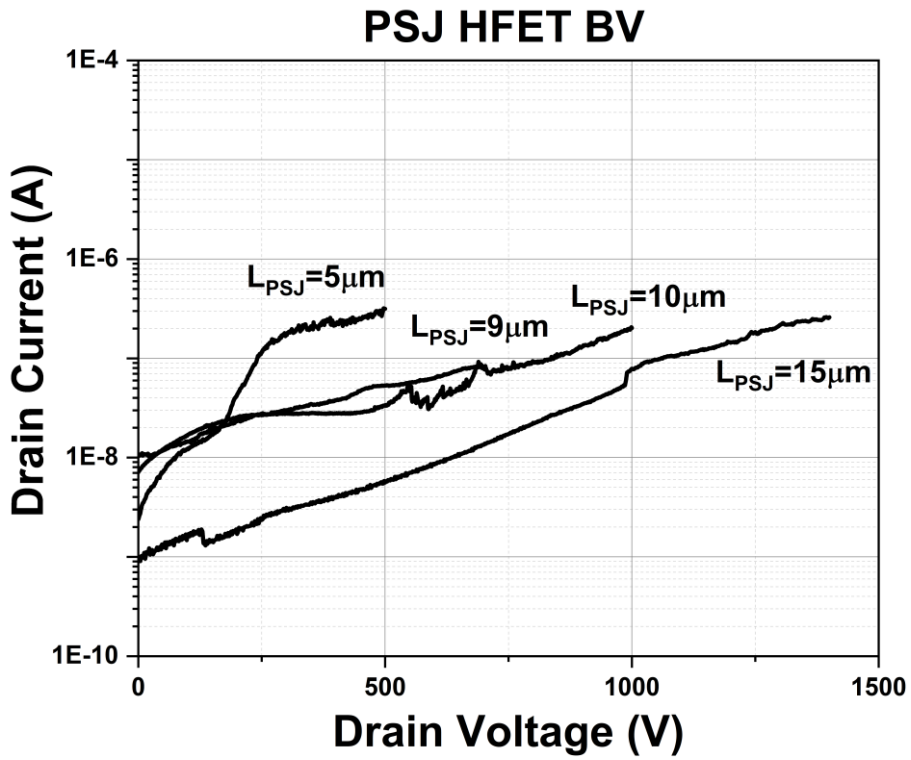


Figure 3.45 Measured off-state I_d-V_d characteristics of Schottky Gate PSJ HFETs at V_g= -15V.

The type of gate does not influence device blocking capability. The next chapter will discuss the detailed analysis of measured results and compare experimental results with analytical and numerical models.

3.7 Summary

This chapter shows the fabrication and measured performance of high voltage Polarization Superjunction (PSJ) GaN-based OG and SG PSJ HFET on Sapphire substrates. The detailed fabrication process is introduced. Electrical characterization from the experiment of forwarding characteristics, reverse characteristics, and detailed Capacitance Voltage (CV) measurements have been performed and discussed. Fabricated OG and PSJ HFETs with the PSJ region length of 20 μm present low on-set voltage and high reverse blocking voltage (V_B) of ~ 2200V and $R_{(on, sp)}$ can be reduced to 10mΩ·cm^2. Relative low $R_{(on, sp)}$ shows the potential of PSJ devices and the simulated and measured results contribution to build the analytical models in next chapter.

Chapter 4 ANALYTICAL MODELING OF SHEET CARRIER DENSITY AND ON-RESISTANCE IN PSJ HFETS

The previous chapter delivered the performance of PSJ devices fabricated and measured. In this chapter, a detailed analysis on the on-state behaviour of the fabricated Ohmic Gate (OG) and Schottky Gate (SG) PSJ HFETs is presented (OG PSJ HFETs are fabricated from Powdec and SG PSJ HFETs are fabricated in Sheffield). Theoretical models for calculating the sheet densities of 2DEG and 2DHG are proposed and calibrated with numerical simulations and experimental results. To calculate the $R_{(on,\ sp)}$ of PSJ HFETs, two different gate structures (Ohmic gate and Schottky gate) are considered herein.

4.1 Introduction

The trade-off between the $R_{(on,\ sp)}$ and the breakdown voltage has been hindered in GaN HFETs. To overcome this, PSJ technology was proposed and has been applied on GaN HEMTs [45, 50]. The PSJ concept is based on the polarization property of III–V group nitride compound semiconductors to realize co-existence of high-density 2DEG and 2DHG at the hetero-interfaces to realize charge balance [50]. The basic structure of the PSJ HFET, as shown in Figure 4.1, arises from GaN/AlGaN/GaN double heterostructure which employs an inherent charge balance in the PSJ region. It can potentially break the one-dimensional material trade-off between the area-specific on-resistance ($R_{(on,\ sp)}$) and the breakdown voltage of conventional GaN technology [70]. This is because the electric field of the PSJ-HFETs feature a rectangular shape in comparison to the triangular shape of the electric field distribution of conventional GaN FETs. Therefore, the breakdown voltage is purely determined by the PSJ length (L_{PSJ}) [45]. In addition, the L_{PSJ} is also key for the on-state behavior [46]. To optimize the on-state performance of PSJ HFET, particularly

reducing the $R_{(on,\ sp)}$, the theoretical analysis of the 2DEG and 2DHG models is necessary.

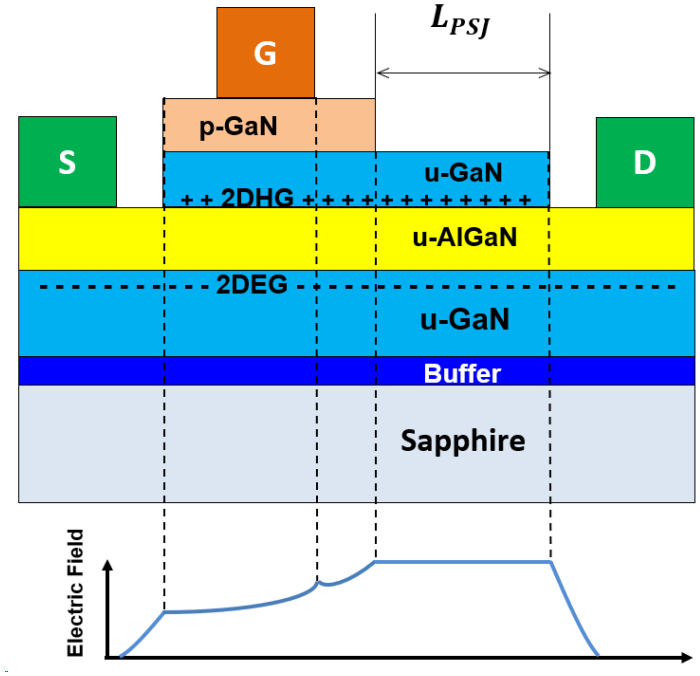


Figure 4.1 Schematic cross-section and simplified electric field distribution of the Ohmic Gate (OG) PSJ HFET.

In this chapter, new analytical models are introduced to investigate the $R_{(on,\ sp)}$ of PSJ HFETs. Analytical models are calibrated with both simulated modes and experimental data to achieve accuracy.

4.2 Methodology

The first step toward building analytical models is to calibrate the sheet density of 2DEG and 2DHG with the numerical simulation and experimental data [47, 48].

4.2.1 Models for 2DEG and 2DHG

In the analytical model, the structure used to calculate 2DEG and 2DHG sheet density is based on practical PSJ devices and reported samples [47, 48]. As shown in Figure 4.2, it consists of a p-type doped GaN cap layer (p-GaN) with Mg-doped, an undoped GaN layer (u-GaN-2), an AlGaN layer and a u-GaN sub-layer (u-GaN-1). It was previously reported that 2DHG sheet density increased with the p-cap GaN layer

thickness. However, when p-GaN layer thickness is beyond 20nm, the influence of p-GaN layer thickness on 2DHG density becomes marginal [47]. Therefore, in the calibration process, each layer thickness is consistent with fabricated PSJ samples.

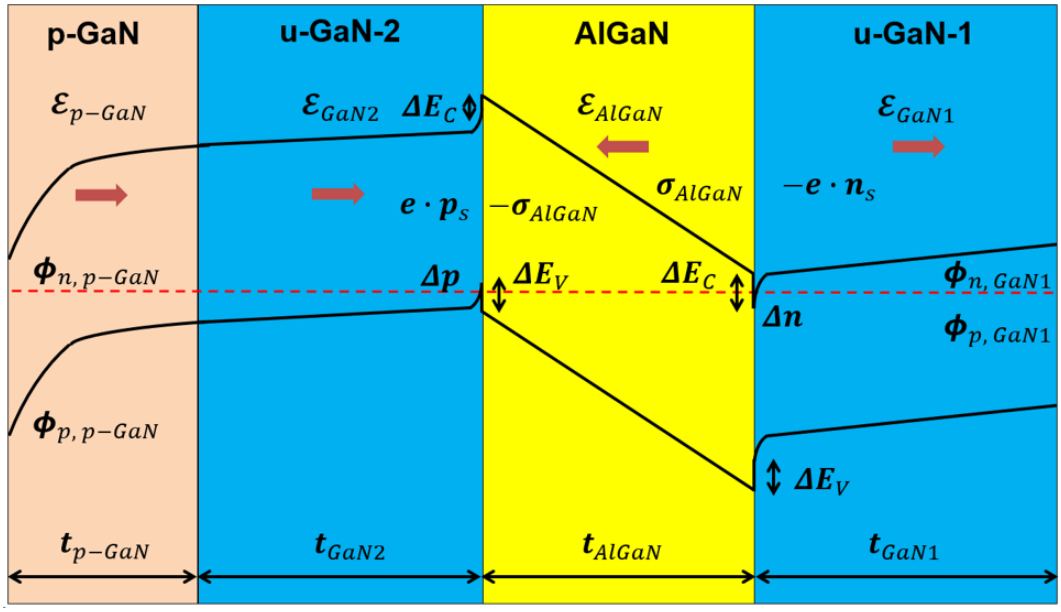


Figure 4.2 Band diagram of p-GaN/u-GaN-2/AlGaN/u-GaN-1 heterostructure.

As shown in Figure 4.2, to obtain expressions for sheet densities of 2DEG and 2DHG, the equation set (4.1)-(4.3) are built according to Gauss' law (the relationship between the electric field ($\epsilon\varepsilon$) and the charge distribution in a closed surface (σ): $\epsilon\varepsilon = \sigma$) at the interface of p-GaN/u-GaN-2, the electric field (D) is (ϵp-GaN× εp-GaN- ϵGaN2× εGaN1) and the charge distribution in a closed surface ($\epsilon\varepsilon$) is $\sigma_{p\text{-}GaN}$, therefore equation (4.1) can be derived from Gauss' law, equation (4.2) and (4.3) is corresponding to the interface of u-GaN-2/AlGaN and AlGaN/u-GaN-1 [71, 72].

$$\epsilon_{p-GaN}\mathcal{E}_{p-GaN} - \epsilon_{GaN2}\mathcal{E}_{GaN2} = \sigma_{p-GaN} \tag{4.1}$$

$$\epsilon_{GaN2}\mathcal{E}_{GaN2} + \epsilon_{AlGaN}\mathcal{E}_{AlGaN} = \sigma_{AlGaN} - e \cdot p_s \tag{4.2}$$

$$\epsilon_{GaN1}\mathcal{E}_{GaN1} + \epsilon_{AlGaN}\mathcal{E}_{AlGaN} = \sigma_{AlGaN} - e \cdot n_s \tag{4.3}$$

In the equation set ((4.1)-(4.3)) shown above, $\epsilon_{p\text{-}GaN}$, ϵ_{GaN2}, ϵ_{AlGaN} and ϵ_{GaN1} are dielectric constants of p-GaN cap layer, u-GaN-2 layer, AlGaN layer and u-GaN-1 layer, respectively. $\varepsilon_{p\text{-}GaN}$, ε_{GaN2}, ε_{AlGaN} and ε_{GaN1} stand for the electric fields in the corresponding layers. $\sigma_{p\text{-}GaN}$ and σ_{AlGaN} are the surface sheet charge of p-GaN layer and AlGaN layer. n_s and p_s represent the sheet carrier density of 2DEG and 2DHG. As shown in Figure 4.2, considering the relationship in the band structure and band bending in the AlGaN region (yellow region), both electron and hole quantum wells (Δn and Δp) are satisfied the expression shown in (4.4) and can be simplified to (4.5).

$$t_{AlGaN}\boldsymbol{\mathcal{E}}_{AlGaN} = \frac{1}{e}\left(E_{G,\ AlGaN} + \Delta p + \Delta n - \Delta E_V - \Delta E_C\right) \tag{4.4}$$

$$t_{AlGaN}\boldsymbol{\mathcal{E}}_{AlGaN} = \frac{1}{e}(E_G + \Delta p + \Delta n) \tag{4.5}$$

Where t_{AlGaN} is the thickness of the AlGaN layer, $E_{G,\ AlGaN}$ and E_G are the bandgap of AlGaN and GaN layer, respectively. ΔE_V and ΔE_C are valence band and conduction band offsets between AlGaN layer and GaN layer [73].

To obtain expressions for n_s and p_s, it is necessary to further deduce equations from the band diagram shown in Figure 4.2. With respect to the valance band potential from the right side to the left as shown in Figure 4.2, one can derive the expression for the potential of the 2DHG quantum well as shown in (4.6). In a similar way, the expression of the 2DEG quantum well can be represented in (4.7) from the conduction band.

$$-\frac{\phi_{p,\ p-GaN}}{e} + t_{p-GaN}\boldsymbol{\mathcal{E}}_{p-GaN} + t_{GaN2}\boldsymbol{\mathcal{E}}_{GaN2} = \frac{\Delta p}{e} \tag{4.6}$$

$$\frac{\phi_{n,\ GaN1}}{e} - t_{GaN1}\boldsymbol{\mathcal{E}}_{GaN1} = -\frac{\Delta n}{e} \tag{4.7}$$

Where $t_{p\text{-}GaN}$, t_{GaN2} and t_{GaN1} stand for p-GaN, u-GaN-2 and u-GaN-1 layer thickness, respectively. $\phi_{p,\ p\text{-}GaN}$ is the valance band barrier height of p-GaN cap and $\phi_{n,\ GaN1}$ is the conduction band barrier height of u-GaN-1 sub-layer. The following step is to substitute relations of $C_{p\text{-}GaN}= \epsilon_{p\text{-}GaN} /t_{p\text{-}GaN}$, $C_{AlGaN}= \epsilon_{AlGaN} /t_{AlGaN}$ and $C_{GaN1}= \epsilon_{GaN1} /t_{GaN1}$ into (4.6) and (4.7) and then revise equations to (4.8) and (4.9).

$$-\frac{\phi_{p,\ p-GaN}}{e}+\frac{\sigma_{AlGaN}-e\cdot p_s}{C}+\frac{\sigma_{p-GaN}}{C_{p-GaN}}-\frac{C_{AlGaN}}{eC}\times(E_G+\Delta p+\Delta n)=\frac{\Delta p}{e} \tag{4.8}$$

$$\frac{\phi_{n,\ GaN1}}{e}-\frac{\sigma_{AlGaN}-e\cdot n_s}{C_{GaN1}}+\frac{C_{AlGaN}}{eC_{GaN1}}\times(E_G+\Delta p+\Delta n)=-\frac{\Delta n}{e} \tag{4.9}$$

Where $C_{p\text{-}GaN}$, C_{AlGaN} and C_{GaN1} are the unit area capacitance of p-GaN, AlGaN and u-GaN-1 layer. C stands for the total unit area capacitance of p-GaN and u-GaN-2 layer.

$$n_s=\frac{m_e}{\pi\hbar^2}\Delta n \tag{4.10}$$

$$p_s=\frac{m_h}{\pi\hbar^2}\Delta p \tag{4.11}$$

According to the relationship between 2DEG sheet charge density and 2DEG quantum well, another approximate expression of 2DEG sheet density, as in (4.10), can be built into the model which can then be used to obtain n_s. In a similar way, an expression for p_s can also be derived as shown in (4.11) [72, 74].

$$\begin{aligned}\boldsymbol{n_s}=&\left[\left(-\frac{\phi_{p,\ p-GaN}}{e}+\frac{\sigma_{AlGaN}}{C}+\frac{\sigma_{p-GaN}}{C_{p-GaN}}-\frac{C_{AlGaN}E_G}{eC}\right)\left(\frac{C_{AlGaN}}{eC_{GaN1}}\cdot\frac{\pi\hbar^2}{m_h}\right)+\right.\\&\left.\left(\frac{C_{AlGaN}}{eC}\cdot\frac{\pi\hbar^2}{m_h}+\frac{\pi\hbar^2}{em_h}+\frac{e}{C}\right)\left(\frac{\phi_{n,\ GaN1}}{e}-\frac{\sigma_{AlGaN}}{C_{GaN1}}+\frac{C_{AlGaN}E_G}{eC_{GaN1}}\right)\right]/\left[\left(\frac{C_{AlGaN}}{eC}\cdot\right.\right.\\&\left.\frac{\pi\hbar^2}{m_e}\right)\left(\frac{C_{AlGaN}}{eC_{GaN1}}\cdot\frac{\pi\hbar^2}{m_h}\right)-\left(\frac{C_{AlGaN}}{eC}\cdot\frac{\pi\hbar^2}{m_h}+\frac{\pi\hbar^2}{em_h}+\frac{e}{C}\right)\left(\frac{C_{AlGaN}}{eC_{GaN1}}\cdot\frac{\pi\hbar^2}{m_e}+\frac{\pi\hbar^2}{em_e}+\right.\\&\left.\left.\frac{e}{C_{GaN1}}\right)\right]\end{aligned} \tag{4.12}$$

$$\boldsymbol{p_s} = \left[\left(\frac{C_{AlGaN}}{eC}\cdot\frac{\pi\hbar^2}{m_e}\right)\left(\frac{\phi_{n,\ GaN1}}{e}-\frac{\sigma_{AlGaN}}{C_{GaN1}}+\frac{C_{AlGaN}E_G}{eC_{GaN1}}\right)+\left(-\frac{\phi_{p,\ p-GaN}}{e}+\frac{\sigma_{AlGaN}}{C}+\frac{\sigma_{p-GaN}}{C_{p-GaN}}-\frac{C_{AlGaN}E_G}{eC}\right)\left(\frac{C_{AlGaN}}{eC_{GaN1}}\cdot\frac{\pi\hbar^2}{m_e}+\frac{\pi\hbar^2}{em_e}+\frac{e}{C_{GaN1}}\right)\right]/\left[\left(\frac{C_{AlGaN}}{eC}\cdot\frac{\pi\hbar^2}{m_h}+\frac{\pi\hbar^2}{em_h}+\frac{e}{C}\right)\left(\frac{C_{AlGaN}}{eC_{GaN1}}\cdot\frac{\pi\hbar^2}{m_e}+\frac{\pi\hbar^2}{em_e}+\frac{e}{C_{GaN1}}\right)-\left(\frac{C_{AlGaN}}{eC}\cdot\frac{\pi\hbar^2}{m_e}\right)\left(\frac{C_{AlGaN}}{eC_{GaN1}}\cdot\frac{\pi\hbar^2}{m_h}\right)\right] \quad (4.13)$$

Consequently, n_s and p_s expressions as presented in (4.12) and (4.13) can be derived by simultaneous (4.1) -(4.13). After substituting parameters in Table 2.1 and Table 4.1 into (4.12) and (4.13) and calculating, it can be found that the order of magnitude of some terms are much smaller than others ($e/C_{AlGaN} \gg \pi\hbar^2/e\cdot m_e$, $e/C \gg C_{AlGaN}/e\ C_{GaN1}\cdot \pi\hbar^2/m_e$, ···). These can be neglected during the simplification. Therefore, n_s and p_s expressions in the analytical model can be finally simplified to (4.14) and (4.15), respectively. Table 2.1 and Table 4.1 show related parameters and equations used in the calculation. For instance, σ_{AlGaN} is the sum of spontaneous polarisation charge (P_{sp}) and piezoelectric polarization charge (P_{pz}), which can be calculated from Table 4.1.

$$\boldsymbol{n_s} = \frac{\sigma_{AlGaN}}{e} - \frac{\phi_{n,\ GaN1}\cdot C_{GaN1}}{e^2} - \frac{C_{AlGaN}E_G}{e^2} \quad (4.14)$$

$$\boldsymbol{p_s} = \frac{\sigma_{AlGaN}}{e} + \frac{\sigma_{p-GaN}\cdot C}{eC_{p-GaN}} - \frac{\phi_{p,\ p-GaN}\cdot C}{e^2} - \frac{C_{AlGaN}E_G}{e^2} \quad (4.15)$$

Symbol	*Unit*	*Value*
m_0	kg	9.11×10^{-31}
$m_{e(Al_xGa_{1-x}N)}$		$(0.314x+0.2(1-x))m_0$
$m_{\mathrm{h}(Al_xGa_{1-x}N)}$		$(0.417x+1.0(1-x))m_0$
ħ	$J\cdot s$	1.05×10^{-34}

Table 4.1 Parameters and equations used for calculation

Mg dopants do not influence the calculation of 2DEG and 2DHG [47, 48]. This is because 30nm of p-type doped GaN cap layer (p-GaN) with $5\times10^{19}cm^{-3}$ Mg doping concentration can only serve approximate $1.5\times10^{10}cm^{-2}$ positive sheet charge density when Mg active percentage is 1% [48]. Compared with both calculated and experimental results of nearly $10^{13}cm^{-2}$ 2DHG sheet density, the contribution from p-GaN layer is negligible.

In the numerical simulation model, physics-based solutions for the sheet density of 2DEG and 2DHG are achieved in Silvaco by using models shown in Table 3.1

The models used in the simulation are based on default parameters. To simultaneously calibrate with PSJ HFET measurement results, parameters such as the thickness of PSJ layers and Al mole fraction are set as the same as those of fabricated PSJ devices.

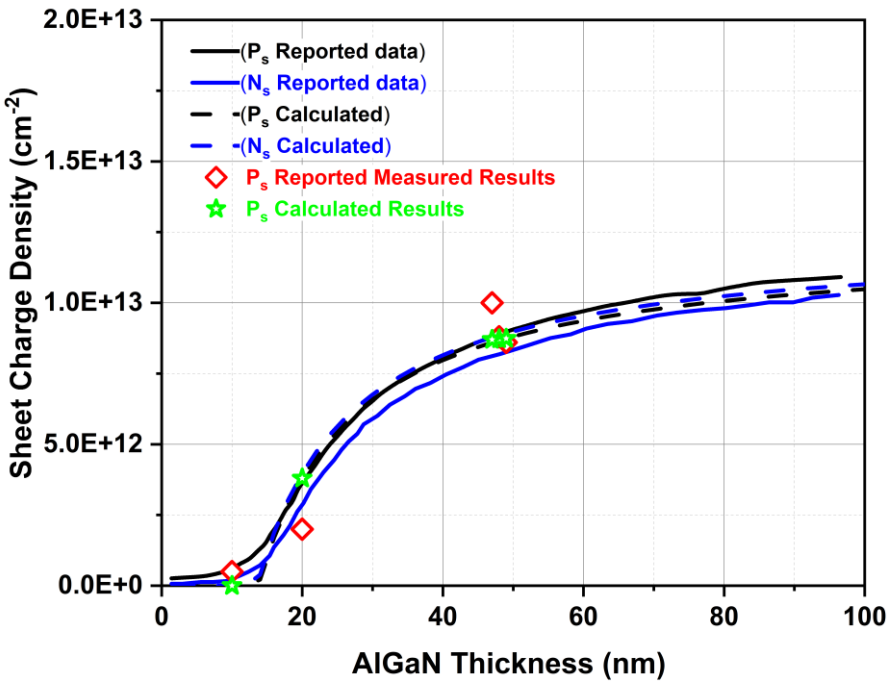


Figure 4.3 Reported results vs. calculated results of *Ns* and *Ps* as AlGaN thickness varies from 0 to 100nm. The solid black line is the reported *Ps* and the solid blue line is the reported *Ns*. The

dashed black and blue lines stand for the calculated P_S and N_S respectively. Red rhombuses are reported measured results and green stars are calculated results [71, 72].

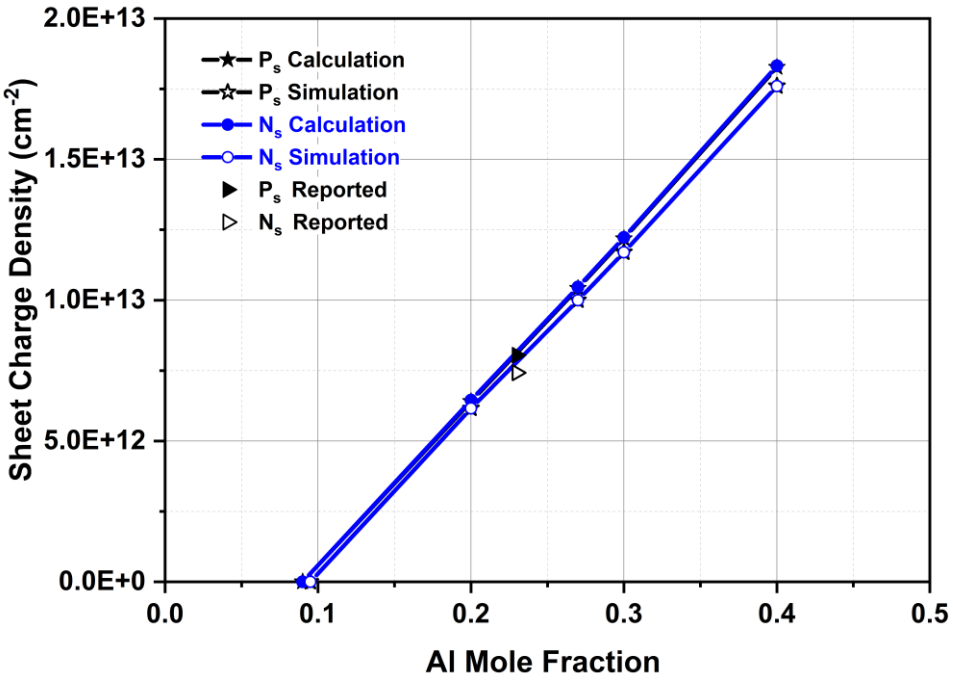


Figure 4.4 Calculated and simulated predictions of N_S and P_S as Al mole fraction alters from 9% to 40% in the heterostructure [71, 72].

Figure 4.3 compares the calculated prediction of N_S and P_S with reported measurement results at different AlGaN layer thicknesses. Parameters applied in analytical models, such as $t_{p\text{-}GaN}$, t_{GaN2}, t_{AlGaN} and t_{GaN1} listed in Table 4.2, are adjusted to fit measured results (red rhombus) in the reference [47, 48]. The calculated results are close to the measurement results. Both N_S and P_S increase with the increase of the AlGaN layer thickness. Figure 4.4 shows the comparison of calculated prediction with the simulated prediction of N_S and P_S versus Al mole fraction. It can be found that both identical calculated and simulated results of N_S and P_S increase as Al mole fraction increases. Verified results are applied to both the analytical model and the simulated model in the following analysis of $R_{(on,\ sp)}$.

Sample ***(Al 23%)***	***Layer Thickness (nm)***				***Reported***	***Calculated***
	t_{p-GaN}	t_{GaN2}	t_{AlGaN}	t_{GaN1}	P_S $(10^{13} cm^{-2})$	P_S $(10^{13} cm^{-2})$

1	30	20	10	1500	0.05	0.00
2	30	20	20	1500	0.20	0.38
3	30	60	47	1500	1.00	0.87
4	30	20	48	1500	0.87	0.87
5	20	20	49	1500	0.86	0.87

Table 4.2 Data of layer structures

4.2.2 The Analytical Model for $R_{(on, sp)}$ of the OG PSJ HFET

Figure 4.5 shows the schematic cross-section of the Ohmic Gate (OG) PSJ HFET [70]. The gate terminal is an ohmic contact formed on the p-GaN cap layer. At the gate region, the OG PSJ HFET consists of a 60nm p-type doped GaN cap layer with $5\times10^{19}cm^{-3}$ Mg dopants, a 65nm undoped GaN layer, a 40nm AlGaN layer and a 1μm u-GaN sub-layer. In the PSJ region, it consists of a 65nm undoped GaN layer, a 40nm AlGaN layer and a 1μm u-GaN sub-layer. To calculate $R_{(on, sp)}$ of OG PSJ HFET by the analytical model, based on the current flow direction along the dashed line under the on-state condition, it can be divided into four different regions (PSJ region, channel region, gap region and contact region) according to the differences in the sheet carrier densities and mobilities of 2DEG and 2DHG, as shown in Figure 4.5. Therefore, the total specific on-state resistance ($R_{on}A$) can be considered as the sum of the PSJ region resistance (R_{PSJ}), the channel region resistance (R_{ch}) and the gap region resistance (R_g) multiplies device area (A) and then plus the contact resistivity (ρ_{conS} and ρ_{conD}) as shown in (4.16), assuming that device width is constant and applicable equally to all these parameters. Gap regions consist of the area between source and gate and the space between PSJ region and drain, as shown in Figure 4.5. In PSJ HFET analytical models, to improve the fitting results, R_g cannot be ignored and need to be calculated separately.

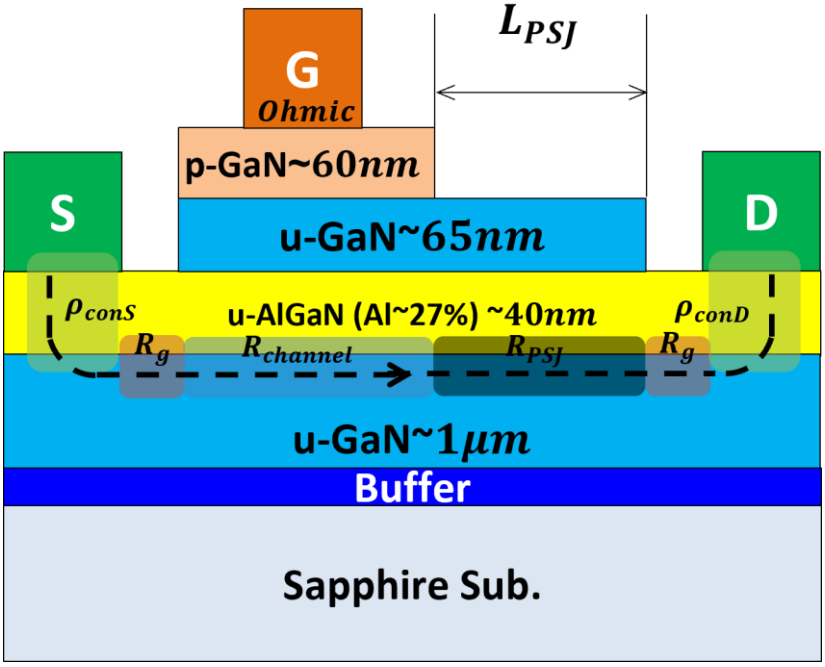


Figure 4.5 Schematic cross-section and simplified electric field distribution of the OG PSJ HFET.

$$R_{on}A = (R_{PSJ} + R_{ch} + R_g) \times A + \rho_{conS} + \rho_{conD} \qquad (4.16)$$

The expression of R_{PSJ} can be derived in (4.17), where q is the electron charge and μ_{2DEG} is the mobility of 2DEG in the PSJ region. n_{2DEG} is the concentration of 2DEG. When integrate n_{2DEG} vertically by the height of 2DEG (H), the result is 2DEG sheet density (σ_{2DEG}). σ_{2DEG} is calculated by the same method demonstrated in previous work. W stands for the width of the device (W and H are common expression in power semiconductor device) which is perpendicular to the 2D cross-section, cannot shown in the figure.

$$R_{PSJ} = \frac{1}{qn_{2DEG}\mu_{2DEG}} \times \frac{L_{PSJ}}{H \times W} = \frac{L_{PSJ}}{q\mu_{2DEG}(n_{2DEG} \times H)W} = \frac{L_{PSJ}}{q\mu_{2DEG}\sigma_{2DEG}W} \qquad (4.17)$$

In the gap region, the derivation of the PSJ region is repeated and the expression for R_g is derived from (4.18), where σ_{2DEG2} and μ_{2DEG2} are the sheet density and mobility of 2DEG in gap regions. L_g represents the total length of the gap region and is 7μm in OG PSJ HFET. 2DEG sheet density and mobility in gap regions (AlGaN/GaN) are different

with those in the PSJ region (p-GaN/GaN/AlGaN/GAN). Therefore, both σ_{2DEG2} and μ_{2DEG2} are calculated again.

$$R_g = \frac{L_g}{q\mu_{2DEG2}\sigma_{2DEG2}W} \tag{4.18}$$

Considering that the OG PSJ HFET is an ohmic gate normally-on device and usually V_g=0V is applied on the gate, the expression for R_{ch} in the PSJ HFET is demonstrated in (4.19), where L_{ch} is 5μm and represents the channel length and μ_{ch} is the carrier mobility in the channel. σ_{ch} is the sheet charge density of 2DEG in the channel.

$$R_{ch} = \frac{L_{ch}}{q\mu_{ch}\sigma_{ch}W} \tag{4.19}$$

ρ_{conS} *and* ρ_{conD} stand for the contact resistivity of the source and the drain electrode, respectively, which measured and calculated by transmission line method (TLM) as shown in (4.20).

$$\rho_{conS} = \rho_{conD} = R_C L_T W = 2.31 \times 10^{-2}\ m\Omega \cdot cm^2\ (TLM\ Testing) \tag{4.20}$$

(4.16) -(4.20) are analytical models for analyzing and calibrating $R_{(on,\ sp)}$ with simulated and measured results. In analytical models, considering the impact from traps, the sheet density (σ_{2DEG}) and the mobility (μ_{2DEG}) of 2DEG need to be adjusted with the experimental data to increase the accuracy. σ_{2DEG} and μ_{2DEG} both reduce after calibrating with experimental results since partial carriers (electrons), which have gained high kinetic energy after being accelerated by the electric field, are captured by traps. The calculated I_d-V_d characteristics based on analytical models are demonstrated in Figure 4.6.

$$I_d = \frac{\mu_{2DEG}W}{(L_{ch}+L_{PSJ})}\frac{\varepsilon_{AlGaN}}{t_{AlGaN}}\left[(V_g - V_{th})V_d - \frac{{V_d}^2}{2}\right] \tag{4.21}$$

Combined analytical models with (4.21) [75], the calculated I_d-V_d characteristics based on analytical models are demonstrated in Figure 4.6. It should be addressed that these

analytical models are mainly applicable to the linear region $R_{(on,\ sp)}$ analysis in PSJ HFETs.

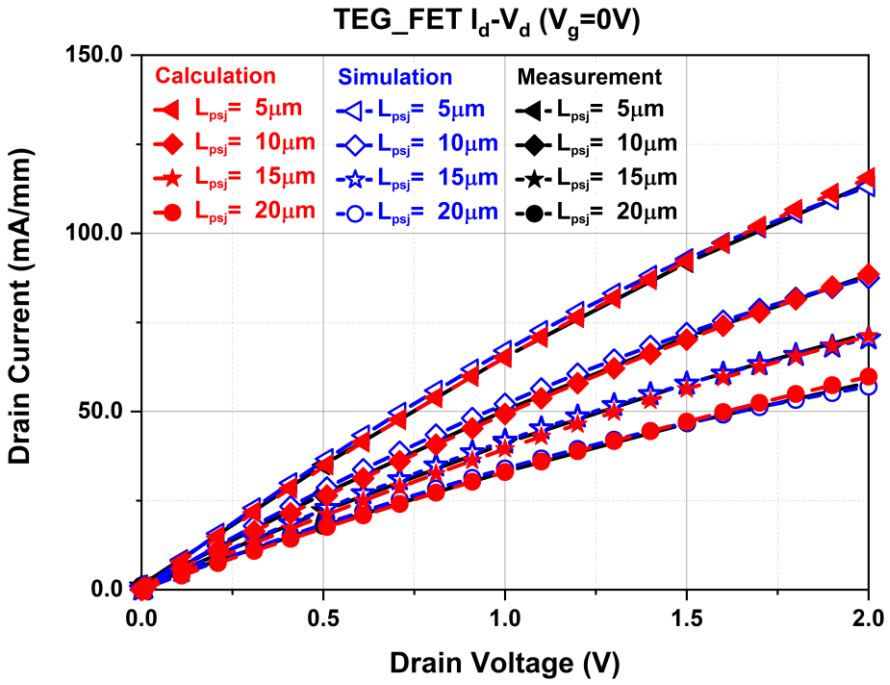


Figure 4.6 Calculated, Simulated and Measured I_d-V_d output characteristics of OG PSJ HFETs at V_g=0V.

4.2.3 The Analytical Model for $R_{(on,\,sp)}$ of the SG PSJ HFET

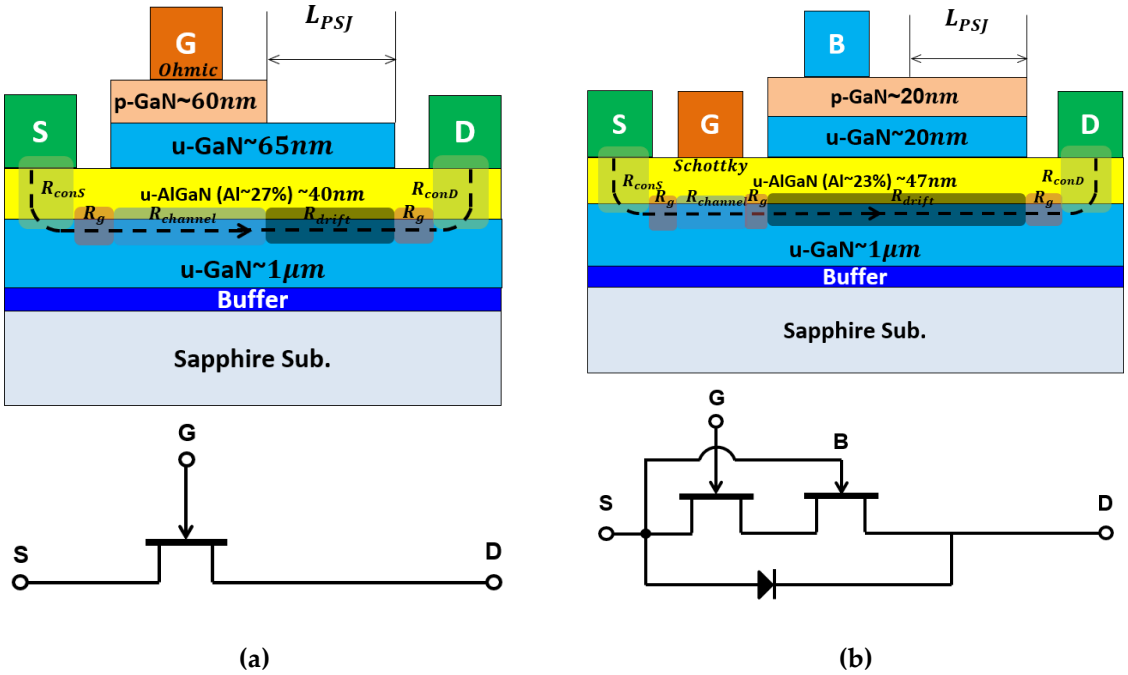


Figure 4.7 Schematics and circuit model of device cross-section for calculating $R_{(on,\,sp)}$ (a) Ohmic Gate PSJ HFET (b) Schottky Gate PSJ HFET.

As shown in Figure 4.7, there are two types of PSJ HFET, the OG PSJ HFET [70] and the SG PSJ HFET [50]. In OG PSJ HFET, the gate terminal is an ohmic contact formed on the p-GaN cap layer. In SG PSJ HFET, gate terminal is a Schottky contact formed on the AlGaN layer. It has an Ohmic base terminal, which is connected to the source terminal internally to form a three-terminal device [46]. The equivalent circuit models are also shown in Figure 4.7. As demonstrated in Figure 4.7(b), the SG PSJ HFET can also be divided into 4 different regions (PSJ region, channel region, gap region and contact region) according to the differences in the sheet carrier densities and mobilities of 2DEG and 2DHG. Therefore, the total specific on-state resistance ($R_{on}A$) can be also considered as the sum of the PSJ region resistance (R_{PSJ}), the channel region resistance (R_{ch}) and the gap region resistance (R_g) multiply device area (A) and then plus the contact resistivity (ρ_{conS} and ρ_{conD}) as shown in (4.16), assuming that device width is constant and applicable equally to all these parameters. As presented in Figure 4.7(b),

the SG PSJ HFET consist of a 20nm p-type doped GaN cap layer with similar $5\times10^{19}cm^{-3}$ Mg doped, a 20nm undoped GaN layer, a 47nm AlGaN layer and a 1μm u-GaN sub layer. Methods of calculating $R_{on}A$ are similar to OG PSJ HFETs.

$$R_{on}A = (R_{PSJ} + R_{base} + R_{ch} + R_g) \times A + \rho_{conS} + \rho_{conD} \qquad (4.22)$$

To calculate $R_{(on, sp)}$ of SG PSJ HFET by the analytical model, based on the current flow direction along the dashed line under the on-state condition, it can be divided into five different regions (PSJ region, channel region, base region gap region and contact region) according to the differences in the sheet carrier densities and mobilities of 2DEG and 2DHG, as shown in Figure 4.7. Therefore, the total specific on-state resistance ($R_{on}A$) can be considered as the sum of the PSJ region resistance (R_{PSJ}), the channel region resistance (R_{ch}), the base region resistance and the gap region resistance (R_g) multiplies device area (A) and then plus the contact resistivity (ρ_{conS} and ρ_{conD}) as shown in (4.22), assuming that device width is constant and applicable equally to all these parameters. Except base region, all the others are the same with OG PSJ HFET. The base region mobility need to be measured, separately.

$$R_{base} = \frac{L_{base}}{q\mu_{base}\sigma_{base}W} \qquad (4.23)$$

The expression for R_{base} in the PSJ HFET is demonstrated in (4.23), where L_{base} is 5μm and represents the base length and μ_{base} is the carrier mobility in the base. σ_{base} is the sheet charge density of 2DEG in the base.

4.2.4 Simulated Model for $R_{(on, sp)}$

The $R_{(on, sp)}$ of the simulated models is calculated from the simulated I_d-V_d curves. Models and parameters are consistent with those previously mentioned 2DEG and 2DHG sheet density simulations. Figure 4.6 presents simulated I_d-V_d curves of OG PSJ HFETs. The cross-section of the device is shown in Figure 4.5. The length of PSJ (L_{PSJ}) varies from 5μm to 20μm. V_g=0V is applied on the gate as well as the source. In Figure

4.6, at the point V_d=1V in the linear region, data is selected to obtain the simulated $R_{(on, sp)}$. It is obvious that $R_{(on, sp)}$ increases L_{PSJ} with increases.

4.3 Measurement of OG PSJ HFETs and SG PSJ HFETs

The measured I_d-V_d curves of the fabricated OG PSJ HFETs are demonstrated in Figure 4.6. The width of OG PSJ HFET samples is 1mm. Similarly, measured results of $R_{(on, sp)}$ are obtained at the point of V_d=1V. It can be found from Figure 4.6 that the drain current reduces when L_{PSJ} is shifted from 5μm to 20μm at V_g=0V and V_d=1V. As can be seen in Figure 4.6, the measured and simulated results show a divergence compared with the calculated results. This is caused by the self-heating effect, which is not accounted for. Therefore, the analytical model is mainly applicable to low voltage $R_{(on, sp)}$ analysis.

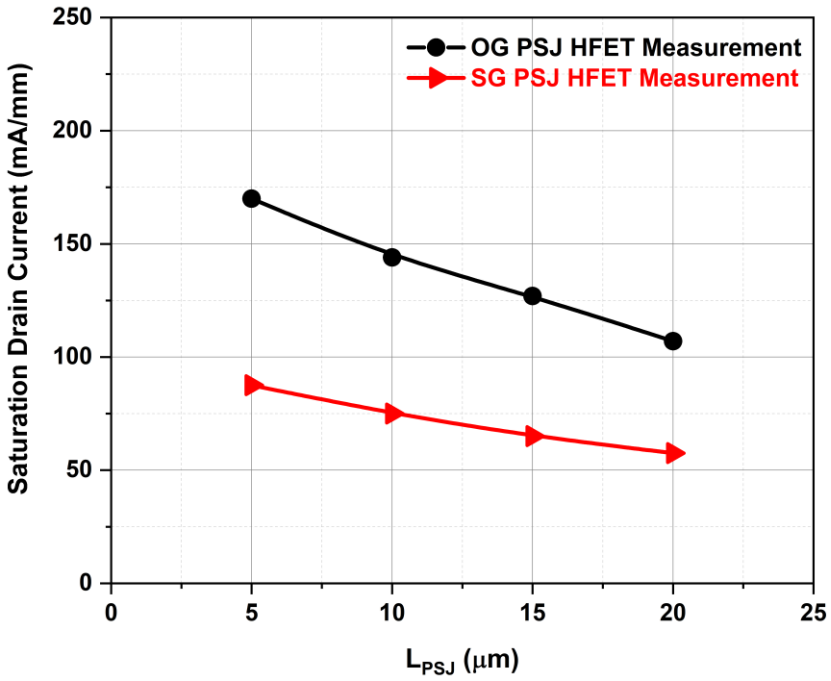
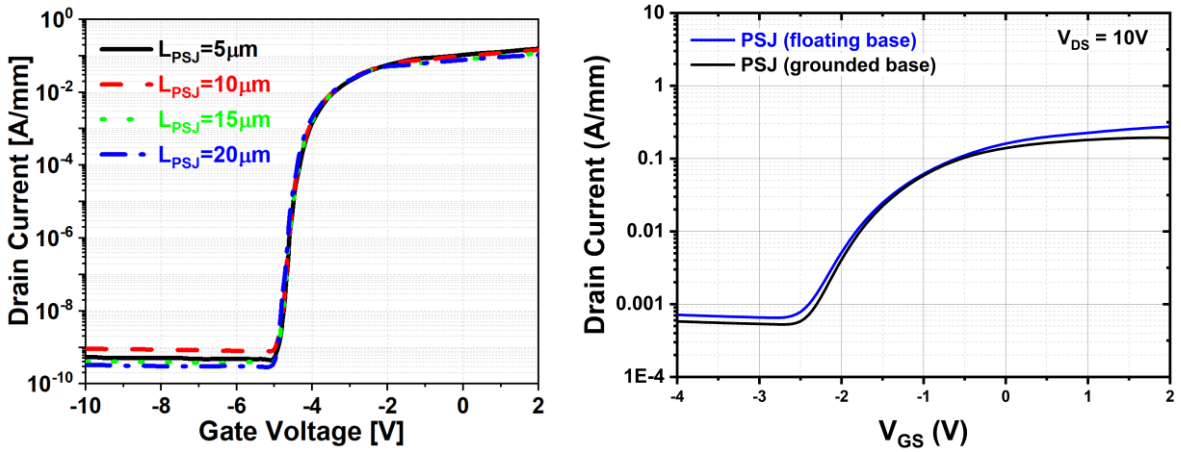


Figure 4.8 Measured Saturation current comparison of OG PSJ HFET and SG PSJ HFET.

The saturation current reduces as the L_{PSJ} gets longer as shown in Figure 4.8. As demonstrated in circuit models in Figure 4.7(b), under high drain bias conditions (saturation region), when the base is connected to the ground, the n-region formed by

2DEG is biased at a high potential, which form the reverse bias of a PN junction. Electrons get depleted in the PSJ region, which causes potential to drop along the PSJ region in the on-state. The magnitude of SG PSJ HFET pinch-off at the drain-side edge of the gate is less than observed in OG PSJ HFET [41, 46]. Hence the saturation current of the OG PSJ HFET is higher than that of the SG PSJ HFET.



(a) (b)

Figure 4.9 Measured characteristics of I_d-V_g at V_d=10V when shifting L_{PSJ} from 5µm to 20µm (a) OG PSJ HFETs (b) SG PSJ HFETs.

Figure 4.9(a) and (b) are the I_d-V_g characteristics of OG PSJ HFETs and SG PSJ HFETs, respectively.

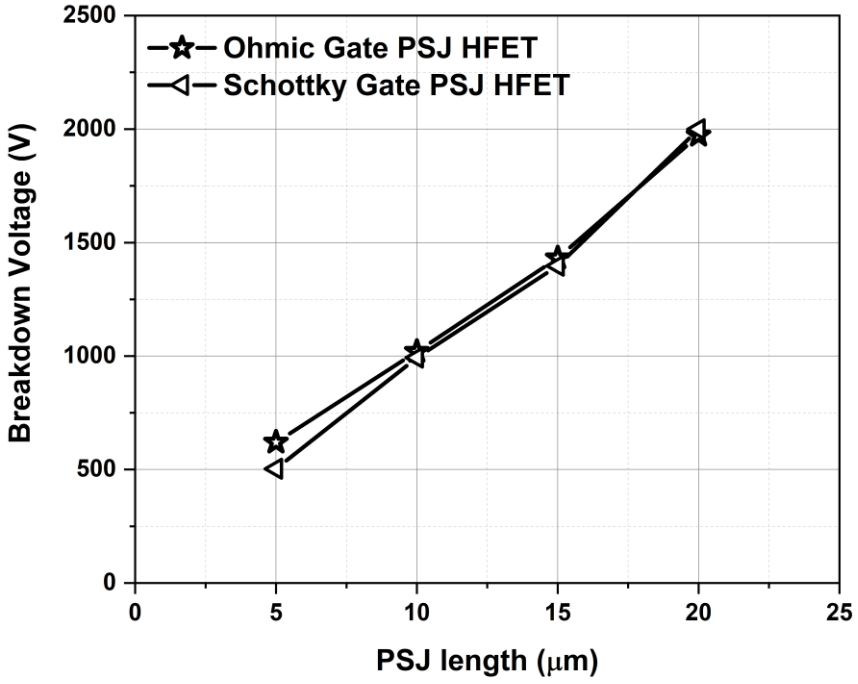
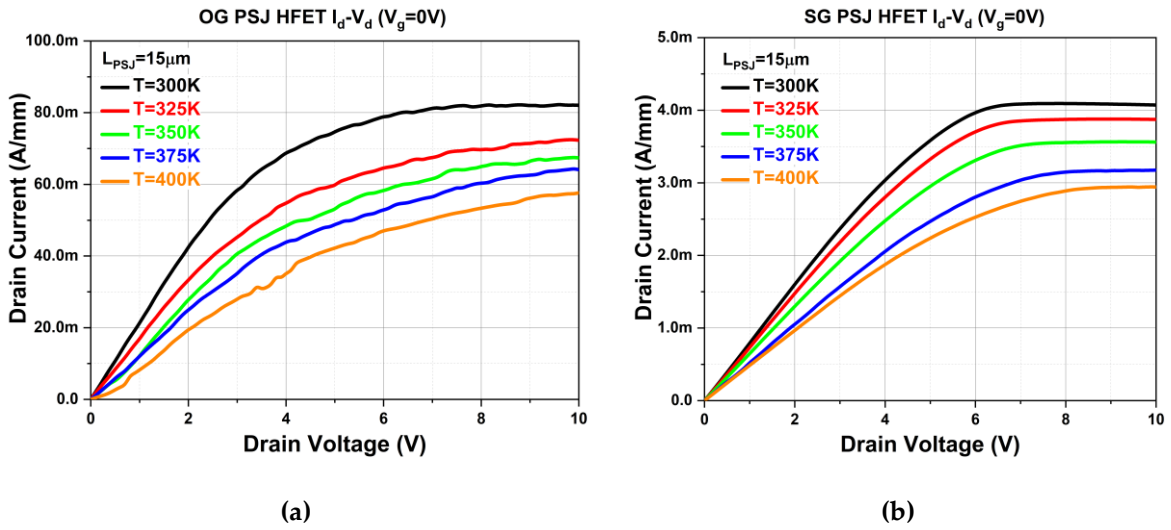


Figure 4.10 BV measurement output characteristics of OG PSJ HFETs and SG PSJ HFETs when shifting L_{PSJ} from 5μm to 20μm at V_g=-15V.

Figure 4.10 presents that the breakdown voltage of PSJ HFETs shows a linear increase with respect to the L_{PSJ} and an average breakdown field strength between 1~1.5MV/cm. Compared with the previous work [50], the average BV electric field strength is increased because of the improvement in the quality of the materials and further optimizing the charge balance in the PSJ region.



(a) (b)

Figure 4.11 Temperature dependent measured characteristics of I_d-V_d at V_g= 0V when L_{PSJ}=15μm (a) OG PSJ HFETs (b) SG PSJ HFETs.

Figure 4.11 demonstrates the reduction of both the OG and SG PSJ HFETs drain saturation current with increasing temperature. As the concentration of 2DEG is almost independent of the temperature variation, the decrease in current can be largely attributed to reduction in 2DEG mobility, increased contact resistance between device metal contact and increased phonon related scattering [51].

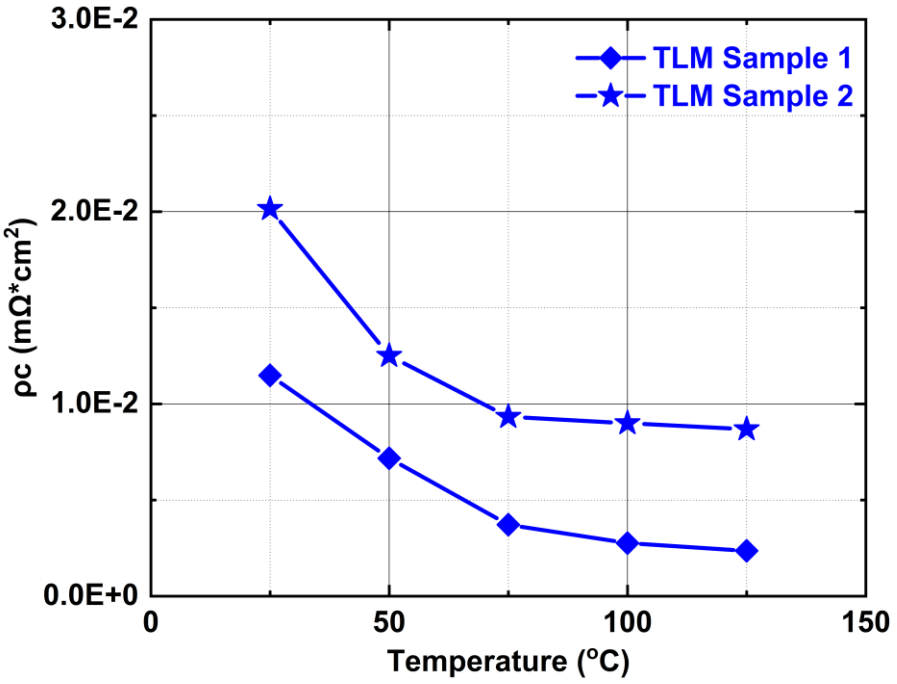


Figure 4.12 Temperature dependence of measured contact resistivity (ρ_c) from TLM test Sample in TEG_FET.

The temperature dependent contact resistance (ρ_{conS} and ρ_{conD}) from TLM test structure in test element group FET (TEG_FET) shows a reducing trend with the temperature increase as shown in Figure 4.12. The magnitude of ρ_{conS} and ρ_{conD} from TLM measured results are much less than $R_{(on,\ sp)}$, hence the impact to $R_{(on,\ sp)}$ from ρ_{conS} and ρ_{conD} is negligible. This rules out the influence of the contact resistance in the current reduction with the temperature increase, as shown in Figure 4.11. Therefore As the concentration of 2DEG is almost independent of the temperature variation, the decrease in current can be attributed mainly to a reduction in 2DEG mobility, increased contact resistance between device metal contact and increased phonon-related scattering.

4.4 Results and Analysis

4.4.1 Results of OG PSJ HFETs

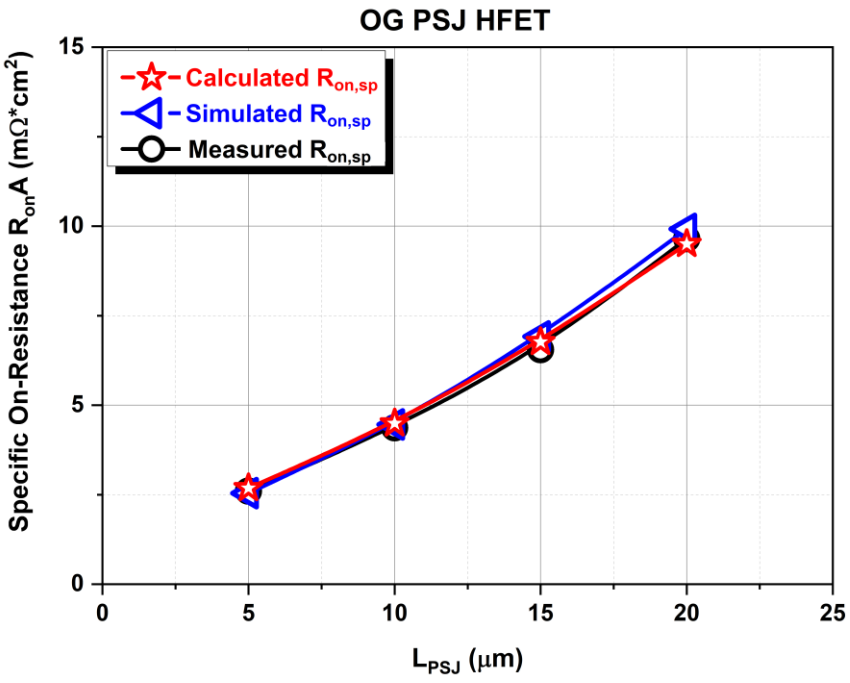


Figure 4.13 Calculated, simulated, and measured $R_{(on,\ sp)}$ of OG PSJ HFETs at room temperatures when V_g=0V.

For accurate calibration of results, identical V_g=0V is applied in both analytical modelling and numerical modelling as well as in the measurements. As presented in Figure 4.13, both analytical and simulated $R_{(on,\ sp)}$ of OG PSJ HFETs are fitted with experimental results when altering PSJ length L_{PSJ} from 5μm to 20μm. Whether by calculation, simulation, or measurement, $R_{(on,\ sp)}$ shows an upward linear trend with the increase in L_{PSJ}. As shown in the figure, relatively accurate analytical and numerical models for predicting the $R_{(on,sp)}$ of PSJ HFET are proposed and demonstrated. It clearly shows that both calculated and simulated results are fitted well with the experimental data of practical PSJ HFETs. The accurate analytical and simulated models can be used to understand the mechanism of PSJ HFETs. It can also be applied on effectively and precisely predicting the performance of PSJ device. Moreover, comprehensive analysis results establish a perfect foundation to further optimize and improve PSJ device architectures. The promising work promotes the development of PSJ technology to satisfy the requirement of stability and security power circuits and shows potential to break the theoretical limit of power semiconductor device in the future.

L_{PSJ} (μm)	*Component Ratio (%)*			R_{on} (Ω) (100%)	$\rho_{conS} + \rho_{conD}$ $(m\Omega \cdot cm^2)$	$R_{on}A$ $(m\Omega \cdot cm^2)$
	R_{PSJ}	R_g	R_{ch}			
5	29.4	41.2	29.4	15.8	0.046	2.68
10	45.5	31.5	22.7	20.4	0.046	4.49
15	55.6	25.9	18.5	25.1	0.046	6.77
20	62.5	21.9	15.6	29.7	0.046	9.50

Table 4.3 Each component ratio to the total Ron in analytical model

Structures.

Table 4.3 shows each R_{on} component ratio to the total R_{on}. It should be addressed that the length of each region, which is related to the device area (A), is also an essential factor to $R_{on}A$. Summarizing the partly statistic $R_{(on, sp)}$ data and differences between calculated and simulated results on measurement data, it should be noted that both the sheet density and mobility of 2DEG are adjusted in calculated and simulated models in order to improve the fitting with experiment results. All differences in Figure 4.13 can be attributed to the fabrication misalignment between different processes, the random measurement error and the assumption that 2DEG mobility from each region in analytical models is constant. However, in the simulation and practical OG PSJ HFETs, the carrier mobility of 2DEG depends on different elements, such as the concentration and electric field distribution.

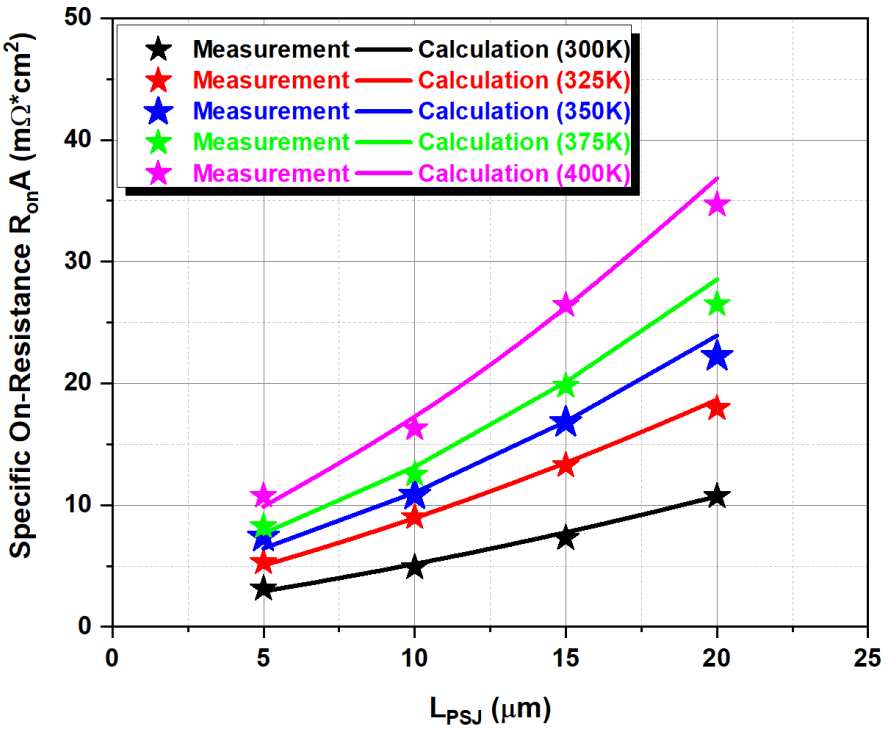


Figure 4.14 Temperature dependence of OG PSJ HFET calculated and measured $R_{(on, sp)}$ fitting results at V_g=0V.

Calculated and measured OG PSJ HFET $R_{(on, sp)}$ with variation in temperature from 300 to 400 K are presented in Figure 4.14. Both calculated and measured $R_{(on, sp)}$ results show increasing trend with the temperature increase. As the concentration of 2DEG is

almost independent of the temperature variation, the increase in $R_{(on, sp)}$ can be largely attributed to the reduction in 2DEG mobility according to (5.16) -(5.19) and increased phonon related scattering [46, 51]. The one major difference is presented at L_{PSJ} =20μm of 400K in calculation. With the increase of the temperature and L_{PSJ}, the impact from the constant carrier mobility assumption in the calculation become more significant.

4.4.2 Compared Results of SG PSJ HFETs

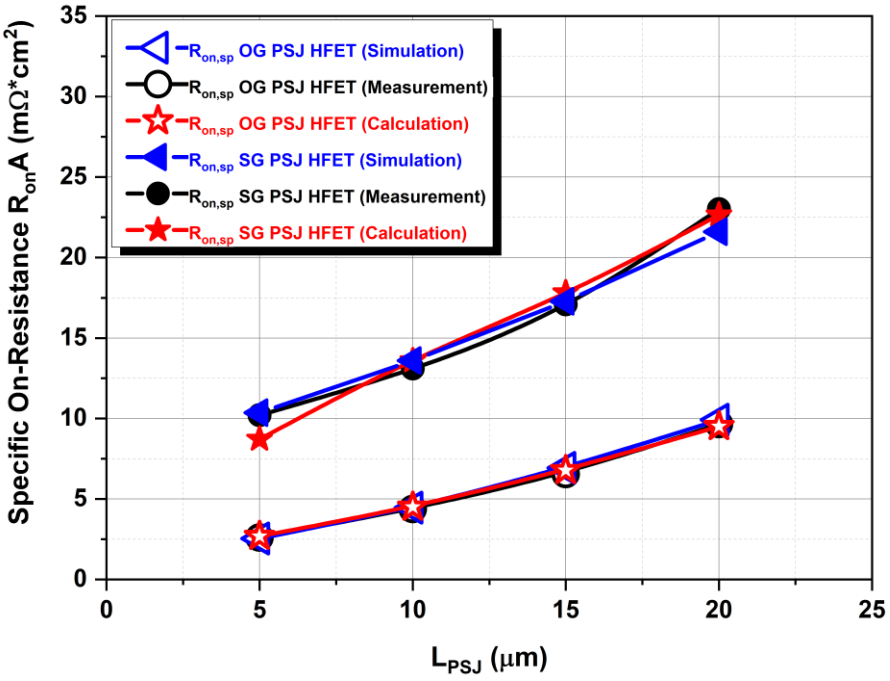


Figure 4.15 Calculated, simulated, and measured $R_{(on, sp)}$ of OG and SG PSJ HFETs at room temperatures when V_g=0V.

The compared results of OG and SG PSJ HFETs are demonstrated in Figure 4.15, identical V_g=0V is applied in both analytical modelling and numerical modelling as well as in the measurements. As presented in the figure, both analytical and simulated $R_{(on, sp)}$ of PSJ HFETs are fitted with experimental results when altering PSJ length L_{PSJ} from 5μm to 20μm. Whether by calculation, simulation, or measurement, $R_{(on, sp)}$ shows an upward linear trend with the increase in L_{PSJ}.

Although calculated and simulated models have limitations from the constant assumption, reasonably accurate calculated and simulated results of $R_{(on, sp)}$ can still be

obtained from these models. The analytical and numerical models provide insight into the conduction mechanisms in PSJ HFETs and contribute to optimising designs to reduce $R_{(on, sp)}$.

4.5 Summary

In this chapter, accurate analytical models for predicting the $R_{(on, sp)}$ of PSJ HFETs are presented. It clearly shows that calculated results fit with both the simulation and the experimental data of practical PSJ HFETs. Precise physics-based PSJ HFET models in this chapter remain valid at different temperatures. The accurate analytical models can promote an understanding of the mechanism of PSJ HFETs. They can also effectively assist in predicting the performance of PSJ devices precisely. Moreover, comprehensive analysis results establish a solid foundation to further optimize and improve PSJ device architectures. Based on these models and analysis results, developing the PSJ concept to the multi-channel PSJ technology level shows a feasible way to break the theoretical limit of power semiconductor devices, which will be presented in the following chapters.

Chapter 5 LATERAL MULTI-CHANNEL PSJ TECHNOLOGY

Detailed theoretical analysis of area-specific on-state resistance ($R_{(on,\ sp)}$) of lateral multi-channel polarisation super-junction (PSJ) technologies at room temperature is presented in this chapter. Similar to Chapter 4, analytical models have been used to calculate the theoretical limit $R_{(on,\ sp)}$ of PSJ devices and calibrate with numerical simulations. Moreover, calculated and simulated results of lateral multi-channel PSJ devices based on practical implementation are also analysed. In addition, the impact of Al composition and AlGaN thicknesses are investigated. Presented results show that lateral multi-channel PSJ technologies can be well suited to break the unipolar one-dimensional material limits of GaN by orders of magnitude and achieve a remarkable trade-off between $R_{(on,\ sp)}$ and voltage blocking capability provided composition and thickness control can be realised.

5.1 Introduction

The trade-off between the area-specific on-state resistance ($R_{(on,\ sp)}$) and the breakdown voltage has been hindered in GaN HFETs. Polarization Super Junction (PSJ) concept was introduced and proved can solve the issue in previous chapters. As shown in Figure 5.1(a), the basic PSJ structure, which arises from GaN/AlGaN/GaN double-heterostructure employs an inherent charge balance between high-density two-dimensional electron gas (2DEG) and two-dimensional hole gas (2DHG) at the respective hetero-interfaces [50]. It can potentially break the one-dimensional trade-off between the $R_{(on,\ sp)}$ and the breakdown voltage of conventional GaN technology [70]. This is because of the rectangular electric field of the PSJ-HFETs under blocking conditions. In a typical Super Junction (SJ) device, the n-pillar and p-pillar can be repeated to increase the current capability of the device. Therefore, similarly, the PSJ concept can also be extended to the multi-channel PSJ concept vertically to increase the current capability and reduce the $R_{(on,\ sp)}$. It is also possible to construct and analyse vertical, nano column type PSJ structures [76, 77].

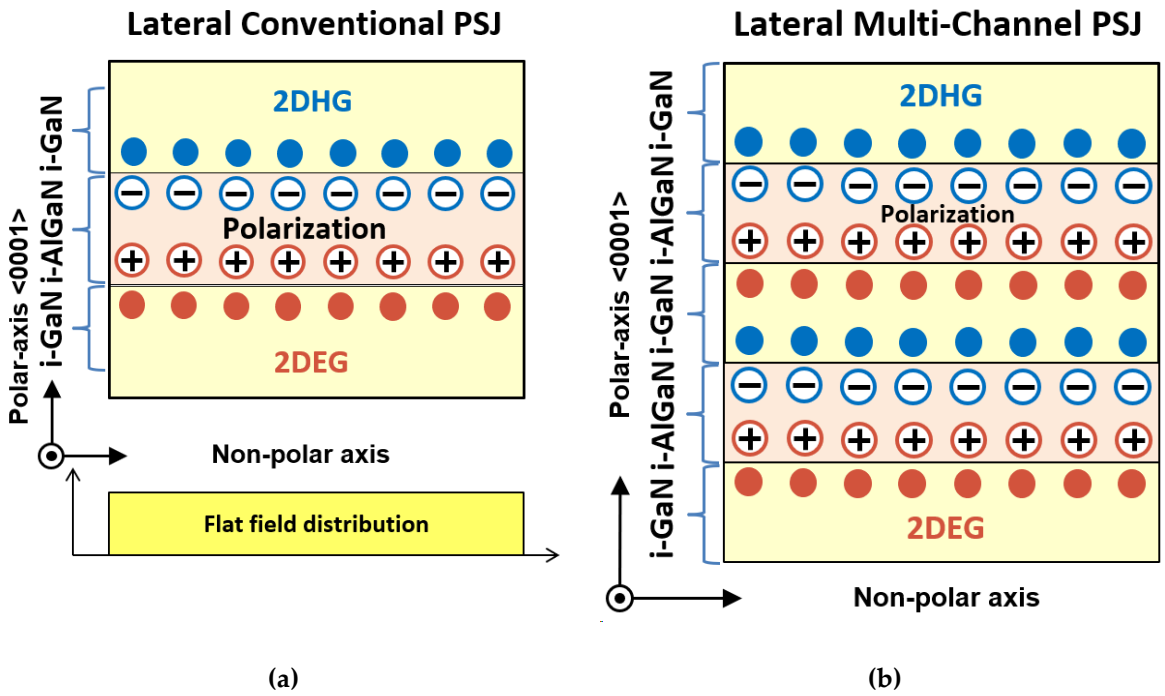


Figure 5.1 Schematic cross section and simplified electric field distribution of (a) Lateral PSJ structure and (b) Lateral multi-channel PSJ Structure.

Until now, the lateral multi-channel PSJ concept, as shown in Figure 5.1(b), has not been reported, where the number of stacks is grown vertically. It is different from natural super-junction (NSJ) [78] because in a typical lateral multi-channel PSJ device, each 2DEG layer corresponds with a 2DHG layer to implement the charge balance condition. In the PSJ device, if the number of multi-channels is N, the total number of AlGaN and GaN layers is (2N+1).

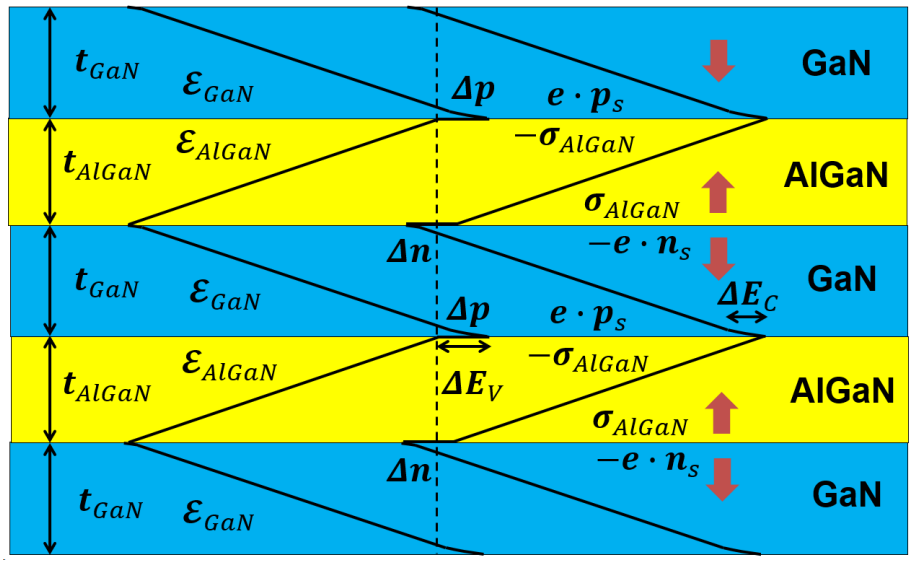


Figure 5.2 Schematic band diagrams of u-GaN/u-AlGaN multi-channel PSJ heterostructure.

is N, the total number of AlGaN and GaN layers is (2N+1). Figure 5.2 shows the energy band diagram of the lateral multi-channel structure of a typical PSJ device. Although issues such as uneven 2DEG density within each of the channels, film cracking when the critical AlGaN thickness exceeded and Al mole fraction and difficulty of p-type contact to 2DHG channels [79-82], solutions for design aspects also have been reported [79] and multi-channel devices have been fabricated recently [83-85]. In addition, Enhancement-mode (E-mode) multi p-channel MES-FinFETs have been proposed and manufactured, which indirectly proves the implementation of high on-state current density for a normally-off GaN FET and excellent gate control through multi-channel PSJ structure and Fin-type gate. [86]. Moreover, as improvements have been made in the growth/over-growth of high-aspect-ratio GaN-based nano-columns on polar/non-polar bulk GaN substrates [77], a highly innovative solution of fabricating lateral multi-channel PSJ devices can be potentially implemented.

In this chapter, the theoretical analysis on $R_{(on,\ sp)}$ of lateral multi-channel PSJ technology are investigated by analytical and numerical models.

5.2 Lateral Multi-channel PSJ Devices Theoretical Limit Prediction

In predicting the performance for PSJ devices, analytical models of 2DEG and 2DHG adopted herein are compared with numerical simulation and experimental data [47-49]. The theoretical limit prediction is based on an ideal situation. The issues of practical multi-channel PSJ implementation are not considered.

5.2.1 The Theoretical Analysis for Lateral Multi-channel PSJ devices

In lateral multi-channel PSJ devices, the 3-D cross-section consists of u-AlGaN/u-GaN multi-channels, as shown in Figure 5.3.

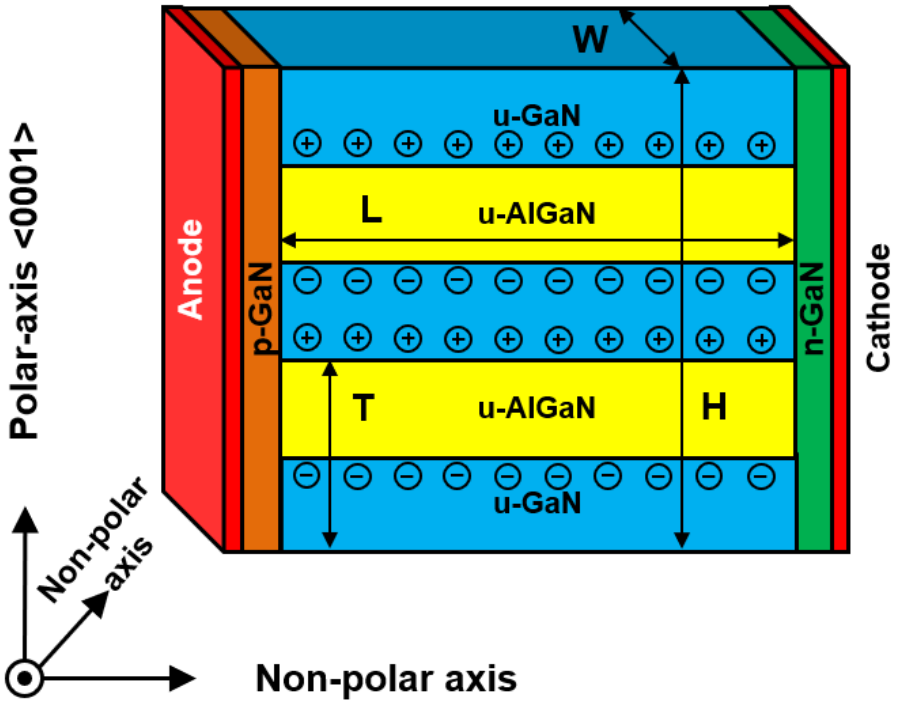


Figure 5.3 3-D schematic cross section of simplified lateral multi-channel PSJ diode.

The thin p-GaN layer design is to provide ohmic contact to each of the 2DHG layers. In the multi-channel lateral PSJ diode, a rectangle shape of electric field distribution can be realized because of the charge balance of 2DEG and 2DHG. Therefore, the expression for $R_{(on,\,sp)}$ of the lateral PSJ device is given as (5.1)

$$R_{on} \times A = \frac{1}{q\mu_{2DEG}n_{2DEG}} \times \frac{L}{H \cdot W} \times L \cdot W = \frac{L^2}{q\mu_{2DEG}n_{2DEG}H} \tag{5.1}$$

Where q is the electron charge and μ_{2DEG} is the mobility of 2DEG. T stands for the sum thickness of a u-GaN layer (t_{GaN}) and a u-AlGaN layer (t_{AlGaN}). n_{2DEG} represents the average concentration of 2DEG within T, L is the length of the PSJ diode and the PSJ region ($L \gg t_{GaN}$). It is also critical for device blocking capability ($L = V_B/E_{crit}$). W is the device's width and H is the total thickness of the multi-channels.

$$n_{2DEG} = \frac{\sigma_{2DEG}}{T} \tag{5.2}$$

(5.2) shows the relationship between n_{2DEG} and unit area 2DEG sheet charge density (σ_{2DEG}). The model for σ_{2DEG} is consistent with the reported work [47, 48]. It is

recognised that within T, 2DEG is concentrated within a small region (a few nm) of polarisation regions and that 2DHG does not contribute to on-state conduction. $L=V_B/E_{crit}$ links device breakdown voltage with the length of the PSJ region (L). Substituting (5.2) into (5.1), the expression of the trade-off between $R_{(on,\ sp)}$ and V_B can be derived into (5.3).

$$R_{on} \times A = \frac{{V_B}^2 \times T}{q\mu_{2DEG}{E_{crit}}^2\sigma_{2DEG}H} = \frac{L^2 \times T}{q\mu_{2DEG}\sigma_{2DEG}H} = \frac{L^2}{q\mu_{2DEG}} \times \alpha \qquad (5.3)$$

According to (5.3), we define a vital index α and the expression for α is shown in (5.4). N is the number of 2DEG (2DHG) layers as well as the number of multi channels. From (5.3), it can be inferred that to optimize $R_{(on,\ sp)}$ one needs to maximize μ_{2DEG} and minimize α, when the other parameters are held at specific values.

$$\alpha = \frac{T}{\sigma_{2DEG}H} = \frac{1}{\sigma_{2DEG}} \cdot \frac{1}{(2N+1)} \qquad (5.4)$$

α can become infinitely smaller and approach to zero when N varies to infinitely large, as shown in (5.4). However, this situation only can be realized theoretically. Therefore, in the calculation of lateral multi-channel device $R_{(on,\ sp)}$, when the height (H) is much smaller than the length (L_{PSJ}), the expression for the $R_{(on,\ sp)}$ is shown in (5.5). It is evident that the $R_{(on,\ sp)}$ reduces with increase in N.

$$R_{on} \times A = \frac{L^2}{Nq\mu_{2DEG}\sigma_{2DEG}} \qquad (5.5)$$

To minimize $R_{(on,\ sp)}$, analyzing (5.1)-(5.5) and referring to a particular device volume (equivalent L, W and H), it is evident that μ_{2DEG} and n_{2DEG} should be maximised.

$$R_{on} \times A = \frac{L^2}{q\mu_{2DEG}H} \times \frac{T}{\sigma_{2DEG}} = \frac{L^2}{q\mu_{2DEG}H} \times \frac{1}{n_{2DEG}} \qquad (5.6)$$

As shown in (5.6), the critical element to reduce $R_{(on,\ sp)}$ is to increase n_{2DEG} (σ_{2DEG}/T). Besides, a multi-channel PSJ device needs to be charge balanced to realize the 'box' shape electric field distribution and equality of conduction current in each channel

require the sheet density of each 2DEG and 2DHG layer to be identical. Therefore, all u-GaN layer thickness should be identical and is defined as t_{GaN} as well as all u-AlGaN layer thickness is t_{AlGaN}. Since the number of 2DEG (2DHG) is N, the total number of multi-channel layers is $n=(2N+1)$, as demonstrated in Figure 5.3.

To obtain the expression for σ_{2DEG}, the equation set (5.7) and (5.8) are built according to 'Gauss' law at each interface of u-AlGaN/u-GaN and u-GaN/u-AlGaN as shown in Figure 5.2. Since other AlGaN/GaN layers are repeated, (5.7) and (5.8) can represent all the other 'Gauss' law expressions in the multi-channel PSJ structure [71, 72].

$$\epsilon_{AlGaN}\mathcal{E}_{AlGaN} + \epsilon_{GaN}\mathcal{E}_{GaN} = \sigma_{AlGaN} - e \cdot n_s \tag{5.7}$$

$$\epsilon_{GaN}\boldsymbol{\mathcal{E}}_{GaN} + \epsilon_{AlGaN}\boldsymbol{\mathcal{E}}_{AlGaN} = \sigma_{AlGaN} - e \cdot p_s \tag{5.8}$$

Where ε_{GaN} and ε_{AlGaN} stand for the electric field in GaN and AlGaN layer, respectively. ϵ_{GaN} and ϵ_{AlGaN} are GaN and AlGaN dielectric constants. σ_{AlGaN} represents the surface charge in the AlGaN layer. n_s is average 2DEG sheet charge density and p_s is average 2DHG sheet charge density. As shown in Figure 5.2, considering the relationship between AlGaN/GaN band structure and band bending in the AlGaN region (yellow region), electron and hole quantum wells (Δn and Δp) satisfy the expression shown in (5.9). It can be simplified to (5.10).

$$t_{AlGaN}\boldsymbol{\mathcal{E}}_{AlGaN} = \frac{1}{e}\left(E_{G,\ AlGaN} + \Delta p + \Delta n - \Delta E_V - \Delta E_C\right) \tag{5.9}$$

$$t_{AlGaN}\boldsymbol{\mathcal{E}}_{AlGaN} = \frac{1}{e}(E_G + \Delta p + \Delta n) \tag{5.10}$$

$$\frac{C_{AlGaN}}{e}(E_G + \Delta p + \Delta n) + \frac{C_{GaN}}{e}(E_G + \Delta n + \Delta p) = \sigma_{AlGaN} - e \cdot n_s \tag{5.11}$$

Where t_{AlGaN} is the thickness of the AlGaN layer, $E_{G,\ AlGaN}$ and E_G are the bandgap of the AlGaN and GaN layer, respectively. ΔE_V and ΔE_C are valence band and conduction

band offsets between AlGaN layer and GaN layer, respectively [73]. To obtain the expressions for n_s and p_s, it is necessary to further deduce equations from the band diagram shown in Figure 5.2. Concerning the conduction band potential distribution from the right side to the left, the expression including the potential of the 2DEG quantum well can be derived and delivered in (5.11). Where $C_{AlGaN}= \epsilon_{AlGaN} /t_{AlGaN}$ and $C_{GaN}= \epsilon_{GaN} /t_{GaN}$ are the unit capacitance of AlGaN and GaN layer, respectively.

$$n_s = \frac{m_e}{\pi\hbar^2}\Delta n \tag{5.12}$$

$$p_s = \frac{m_h}{\pi\hbar^2}\Delta p \tag{5.13}$$

A typical multi-channel PSJ device is a unipolar device and 2DEG is the only carrier relevant to $R_{(on,\ sp)}$. The function of 2DHG is to realize charge balance and uniform electric field distribution. When the number of stack multi-channels is large enough, considering charge compensation, n_s should be identical with p_s, which can also be deduced from (5.7) and (5.8). According to the relationship between 2DEG sheet charge density and quantum well, another approximate expression of 2DEG sheet density, as shown in (5.12), can be built into the model. Similarly, an expression for p_s can also be derived as shown in (5.13) [72, 74]. Substitute (5.12) and (5.13) into (5.11). Further, simplify the formula to (5.14) and solve the equation. The solution for n_s is finally obtained and shown in (5.15).

$$\left[\left(\frac{C_{AlGaN}+C_{GaN}}{e}\right)\left(\frac{\pi\hbar^2}{m_e}+\frac{\pi\hbar^2}{m_h}\right)+e\right]n_s = \sigma_{AlGaN} - \left(\frac{C_{AlGaN}+C_{GaN}}{e}\right)\cdot E_G \tag{5.14}$$

$$\sigma_{2DEG} = \frac{\sigma_{AlGaN} - \left(\frac{C_{AlGaN}+C_{GaN}}{e}\right)\cdot E_G}{\left[\left(\frac{C_{AlGaN}+C_{GaN}}{e}\right)\left(\frac{\pi\hbar^2}{m_e}+\frac{\pi\hbar^2}{m_h}\right)+e\right]} \tag{5.15}$$

In (5.15), it is evident that to maximize n_s is to maximize σ_{AlGaN}. As σ_{AlGaN} increases with the increasing of Al mole fraction, Al mole fraction should be maximized to obtain the

maximum σ_{AlGaN}. Therefore, Aluminium Nitride (AlN) can be used instead of AlGaN in the following theoretical limit derivation. Substitute the relationship shown in (5.16) into (5.15), the solution for n_{2DEG} (σ_{2DEG}/T) can be simplified to (5.17)

$$\frac{e}{C_{AlN}} > \frac{e}{C_{GaN}} \gg \frac{\pi\hbar^2}{e \cdot m_e} > \frac{\pi\hbar^2}{e \cdot m_h} \tag{5.16}$$

$$\begin{aligned} \sigma_{2DEG} &= \frac{\sigma_{AlN} - \left(\frac{C_{AlN} + C_{GaN}}{e}\right) \cdot E_G}{\left[\left(\frac{C_{AlN} + C_{GaN}}{e}\right)\left(\frac{\pi\hbar^2}{m_e} + \frac{\pi\hbar^2}{m_h}\right) + e\right] T} \\ &\approx \frac{\sigma_{AlN} - \left(\frac{C_{AlN} + C_{GaN}}{e}\right) \cdot E_G}{eT} \end{aligned} \tag{5.17}$$

The thickness of the u-AlGaN layer t_{AlGaN} leads to u-GaN layer thickness as (T- t_{AlGaN}). In (5.17), (C_{GaN}+ C_{AlN}) can also be expanded and conversed as shown in (5.18). To achieve maximum σ_{2DEG}/T, (C_{GaN}+ C_{AlN}) needs to be minimized. After mathematical derivation, $t_{AlGaN}=0.5T$ is the most appropriate value to maximize σ_{2DEG}/T. In other words, one of the demands to maximize n_{2DEG} is that the thickness of the u-GaN layer and the u-AlN (u-AlGaN) layer should be equivalent.

$$\begin{aligned} C_{AlN} + C_{GaN} &= \frac{8.5\varepsilon_0 T + 0.4\varepsilon_0 t_{AlGaN}}{t_{AlGaN}(T - t_{AlGaN})} \approx \frac{8.5\varepsilon_0 T}{t_{AlGaN}(T - t_{AlGaN})} \\ &= \frac{8.5\varepsilon_0 T}{-{t_{AlGaN}}^2 + t_{AlGaN} T} \end{aligned} \tag{5.18}$$

Where ε_0 is vacuum permittivity and the relative permittivity of $Al_xGa_{1-x}N$ is $\epsilon_{AlxGa1-xN}$ ($\epsilon_{AlxGa1-xN}=8.5x\varepsilon_0+8.9(1-x)\varepsilon_0$). As a consequence, the simplified solution for σ_{2DEG} is shown in (19) and the solution for n_{2DEG} is shown in (5.20).

$$\sigma_{2DEG} = \frac{\sigma_{AlN} - \left(\frac{34.8\varepsilon_0}{T}\right) \cdot \frac{E_G}{e}}{e} \tag{5.19}$$

$$n_{2DEG} = \frac{\sigma_{2DEG}}{T} = \frac{\sigma_{AlN} - \left(\frac{34.8\varepsilon_0}{T}\right) \cdot \frac{E_G}{e}}{eT} \tag{5.20}$$

Substituting the solution in (5.20) into (5.6) and varying u-GaN thickness (*T*/2) leads to the minimum $R_{(on,\,sp)}$. The difficulty will increase when increasing the number of AlN (AlGaN)/GaN multi-layer in the practical fabrication of the device. To calculate the theoretical limit of the PSJ device in the ideal situation, all parameters in the simulation are idealized. In the perfect case, the contact resistance is assumed to be negligible. In the analysis, the mobility model is mainly based on Caughey–Thomas mobility model, as shown in (5.21) [87].

$$\mu_i(N) = \mu_{min,i} + \frac{\mu_{max,i} - \mu_{min,i}}{1 + \left(\frac{N}{N_{g,i}}\right)^{\gamma_i}} \tag{5.21}$$

Where *i* stands for n-type (2DEG) or p-type (2DEG) carriers and *N* represents doping concentration. $\mu_{min,\,i}$, $\mu_{max,\,i}$, $N_{g,\,i}$ and γ_i are default parameters in the model as shown in Table 5.1. With the increase of 2DEG sheet density, mobility will first increase and then decrease [88-90]. However, as increasing Al composition, 2DEG mobility is enhanced as well as the critical electric field in AlGaN [90].

Carriers Type	$\mu_{(min,i)}$	$\mu_{(max,i)}$	$N_{(g,i)}$	γ_i
n	55	1000	2×10^{17}	1.0
p	3	170	3×10^{17}	2.0

Table 5.1 Parameters for GaN in the Mobility Model.

In the derivation, the PSJ length (*L*) is defined as 20μm and the total thickness of the multi-channels is changed from 200nm to 1μm as shown in Figure 5.4.

5.2.2 The Simulated Analysis for Lateral Multi-channel PSJ Devices

In the numerical simulation, physics-based solutions for the sheet density of 2DEG and 2DHG are achieved in Silvaco TCAD by using models shown in Table 5.2 to obtain reliable results [52]. The models used in the simulation are based on default

parameters. To estimate the theoretical limit of the PSJ device in the ideal situation, all parameters in the simulation are idealized. In the perfect case, the contact resistance of electrodes in calculation and simulation is assumed as zero.

Model name in Silvaco TCAD	*Description*
POLAR	spontaneous polarization
CALC.STRAIN	piezoelectric polarization
CONSRH	Shockley–Read–Hall recombination using concentration-dependent lifetimes
AUGER	recombination accounting for high-level injection effects

Table 5.2 Simulation models and brief description.

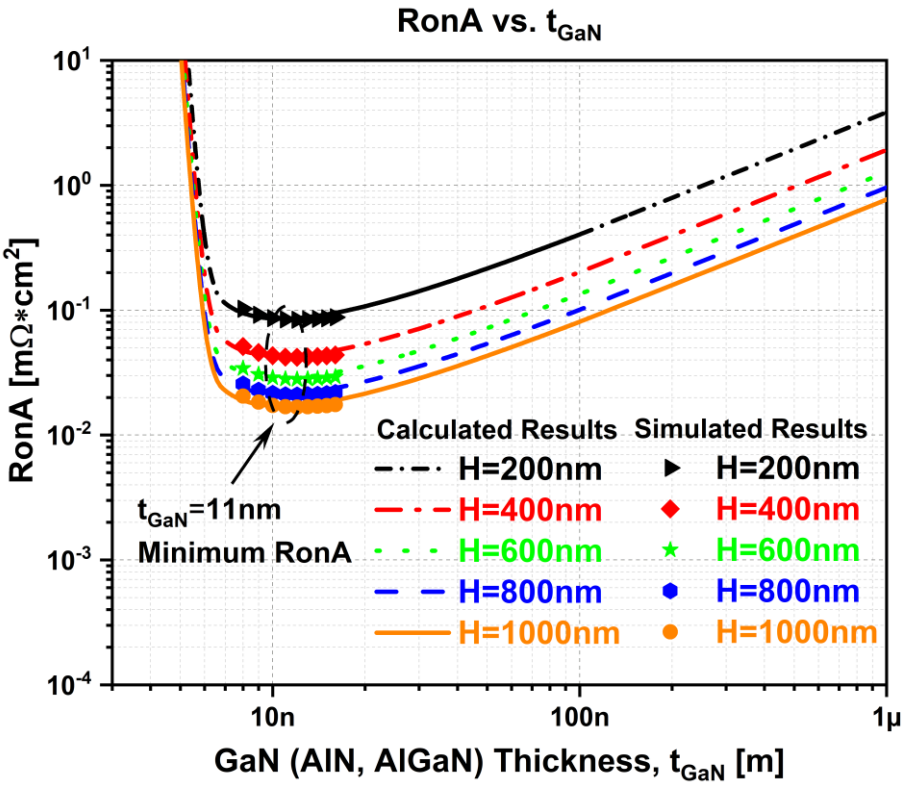
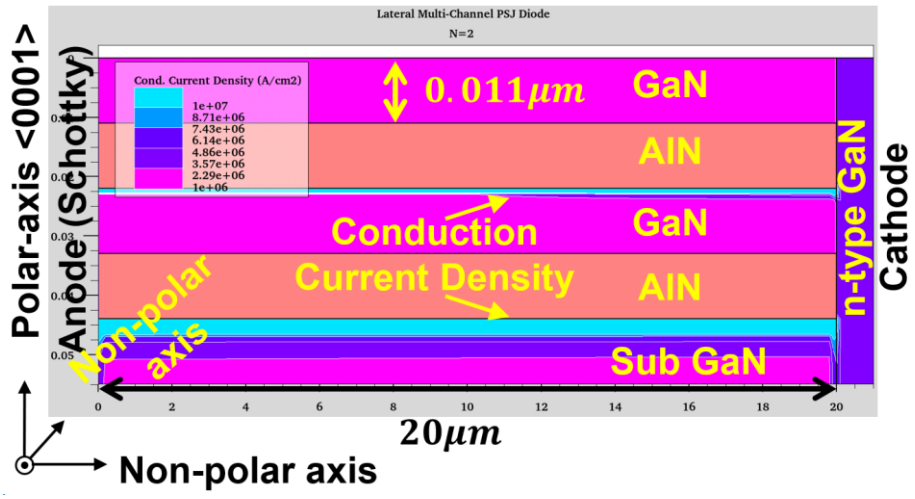


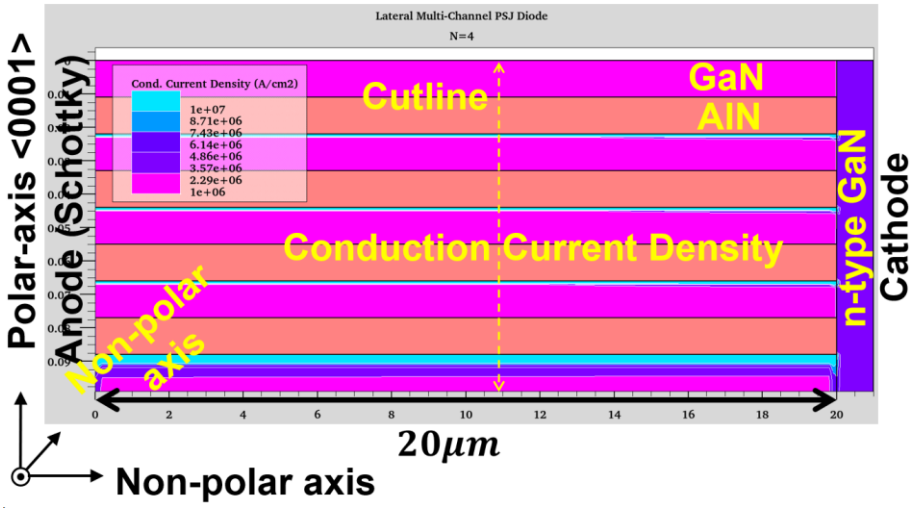
Figure 5.4 Lateral multi-channel PSJ devices calculated and ssimulated $R_{(on, sp)}$ vs t_{GaN}.

In the analysis of multi-channel PSJ devices, the average mobility is assumed as 1000cm²/Vs in both calculation and simulation, it reduces with the increase of carrier concentration [28, 91]. The critical value of electric field strength is theoretically considered as 3.3MV/cm. As shown in Figure 5.4, in the lateral multi-channel PSJ devices, when u-GaN and u-AlGaN thickness is 11nm, the value of $R_{(on, sp)}$ is minimum. It should be addressed that 11nm AlN is only a theoretical value. The thickness of the practical wafer growth technique is typically around 1-3nm through MOCVD growth [89, 92]. With the increase in the number of multi-channels, the $R_{(on, sp)}$ of lateral PSJ devices reduces.

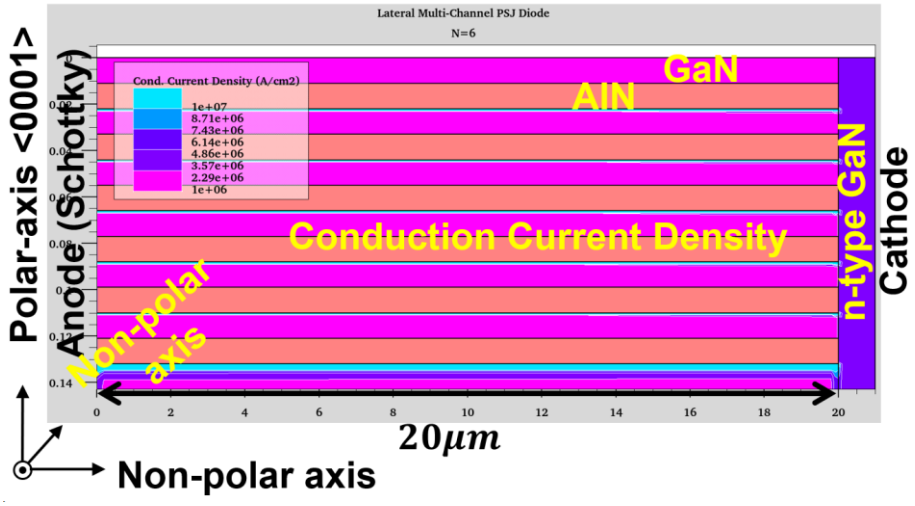
The conduction current density distribution of the simulated lateral multi- channel PSJ diode is presented in Figure 5.5 (a)-(c). Each GaN (AlGaN) layer thickness is 11nm. When the number of multi-channel (N) increases, the conduction current in each channel is uniform, except in the sub-GaN layer. The energy band diagram and carrier (2DEG and 2DHG) concentration distribution along the yellow dashed cutline (shown in Figure 5.5(a)) is demonstrated in Figure 5.5(d).



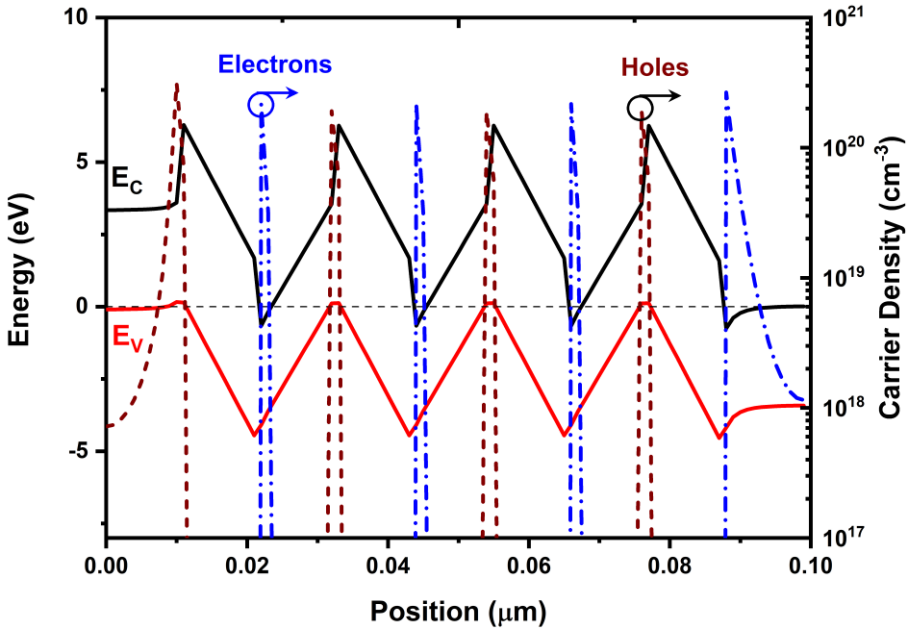
(a)


Lateral Multi-Channel PSJ Diode
N=4
Cond. Current Density (A/cm2)
1e+07
8.71e+06
7.43e+06
6.14e+06
4.86e+06
3.57e+06
2.29e+06
1e+06
Cutline
GaN
AlN
Conduction Current Density
Non-polar axis
n-type GaN
Cathode
Anode (Schottky)
Polar-axis <0001>
20μm
Non-polar axis

(b)


Lateral Multi-Channel PSJ Diode
N=6
Cond. Current Density (A/cm2)
1e+07
8.71e+06
7.43e+06
6.14e+06
4.86e+06
3.57e+06
2.29e+06
1e+06
GaN
AlN
Conduction Current Density
Non-polar axis
n-type GaN
Cathode
Anode (Schottky)
Polar-axis <0001>
20μm
Non-polar axis

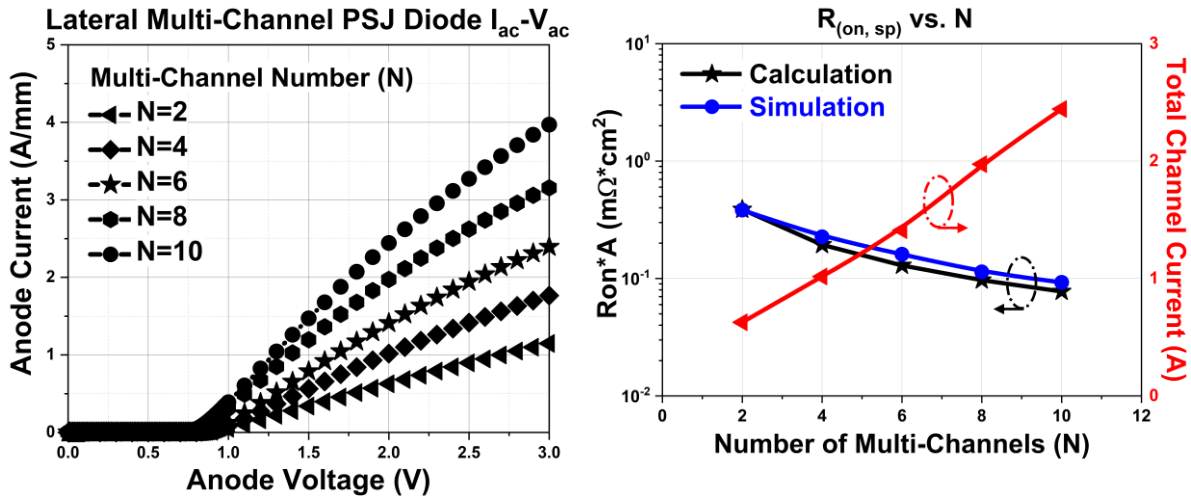
(c)



(d)

Figure 5.5 Lateral multi-channel PSJ diode with t_{GaN}=11nm conduction current density distribution at V_{AC}=5V in simulation (a) N=2 (b) N=4 (c) N=6 (d) Energy band diagram along the yellow dashed line at V_{AC}=0V.

The simulated I_{AC}-V_{AC} for lateral multi-channel PSJ diodes with 11nm u-AlN and 11nm u-GaN is shown in Figure 5.6(a). The conduction current scaled linearly with the number of the multi-channels (N) since the current in each channel is identical, as demonstrated in Figure 5.6(b). With the increase of the multi-channel number, the $R_{(on, sp)}$ of lateral multi-channel PSJ devices reduce significantly, as illustrated in Figure 5.6(b).



(a) (b)

Figure 5.6 (a) I_{AC}-V_{AC} simulated comparison characteristics of lateral multi-channel PSJ diode with t_{GaN}=11nm and L_{PSJ}=20μm the multi-channel number (N) is varying from 2 to 10. (b) Dependence of $R_{(on, sp)}$ and total channel current on the number of multi-channels in lateral PSJ diode with t_{GaN}=11nm.

As shown in Figure 5.7, there is almost no current flow through the yellow dashed line region channel. The current is not equivalent per channel if the Al mole fraction is not identical.

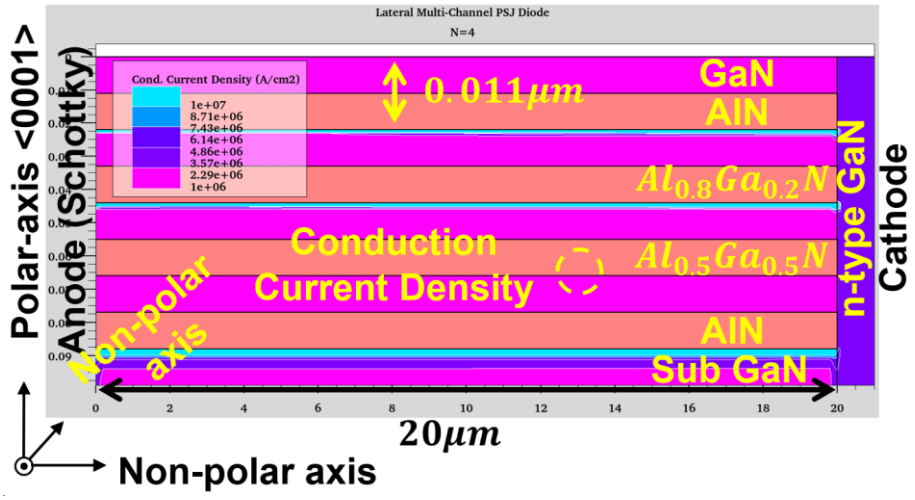
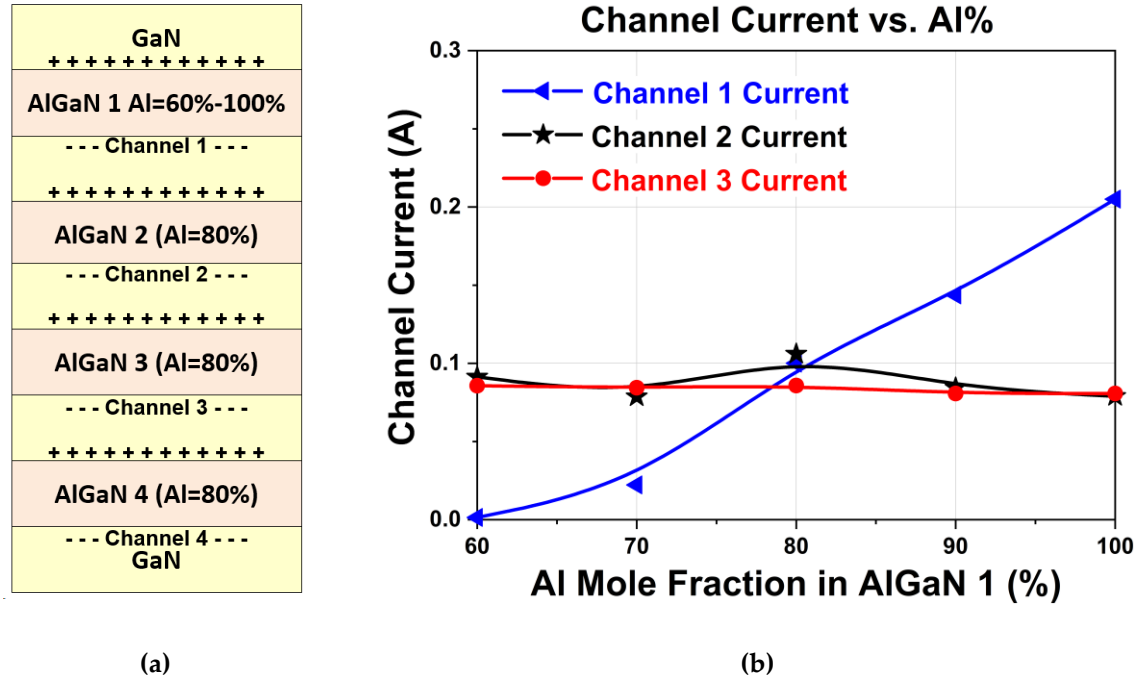


Figure 5.7 Lateral multi-channel PSJ diode with t_{GaN}=11nm conduction current density distribution at V_{AC}=5V in simulation. Al mole fraction is different in each channel.

Figure 5.8(a) demonstrated four channels' simulated lateral multi-channel PSJ structure. As shown in Figure 5.8(b), altering the Al mole fraction in AlGaN 1 from 60% to 100% increases the current in channel 1 while keeping the Al mole fraction at 80%

in the other AlGaN layers. This can be explained by (5.20). σ_{AlGaN}, n_{2DEG} and the channel current are linked together and increased with the Al mole fraction increase. Channel 2 current changed slightly when the Al mole fraction increased in the AlGaN 1. The current in channel 3 is regarded as the reference current and remain nearly constant. When Al mole fractions in AlGaN layers are identical (80% in Figure 5.8(b)), the current values in channels are close to each other.



(a) (b)

Figure 5.8 (a) Schematics of the lateral multi-channel structure when the number of the channels is four (N=4). (b) Current in different channels when altering the Al mole fraction from 60% to 80% in AlGaN 1 layer and Al mole fractions are 80% in AlGaN 2, 3 and 4. V_{AC}=2V, L_{PSJ}=20μm and t_{GaN}= t_{AlGaN}=11nm.

As shown in Figure 5.9(b), by varying the thickness of AlGaN 1 layer from 11nm to 31nm and keeping the additional AlGaN layers' thickness identical, the current in channel 1 increases.

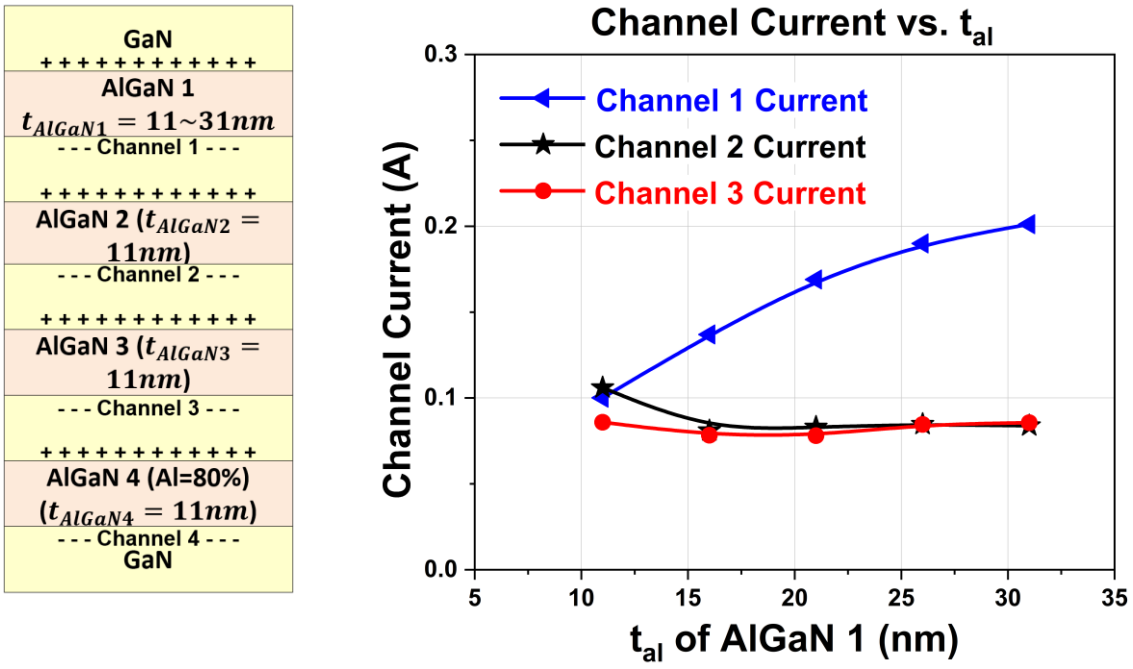
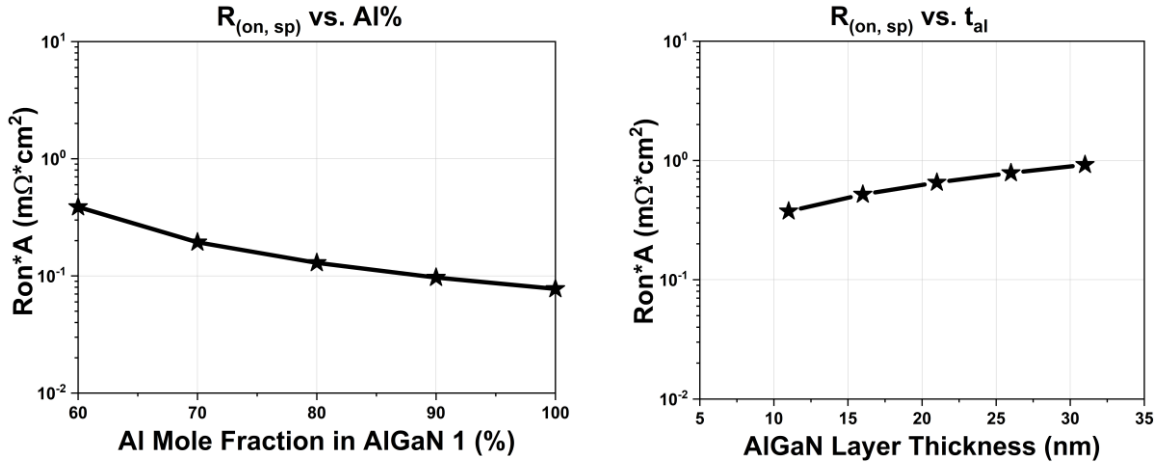


Figure 5.9 (a) Schematics of the lateral multi-channel structure when the number of the channels is four (N=4). (b) Current in different channels when altering AlGaN 1 thickness (t_{AlGaN1}) from 11nm to 31nm and Al mole fractions keep in 80%. V_{AC}=2V, L_{PSJ}=20μm and t_{GaN}= $t_{AlGaN2,3,4}$=11nm.

The growth can also be explained by (5.20). The current is determined by carrier concentration from each channel, in (5.20), although σ_{2DEG} increases with the growth of AlGaN layer thickness, the total thickness of the multi-channel (T) also increases. Therefore, with the exact height of the device, the $R_{(on, sp)}$ increases with the growth of some AlGaN layer thickness, as demonstrated in Figure 5.10(b).



(a) **(b)**

Figure 5.10 Simulated $R_{(on, sp)}$ (a) varying Al mole fraction from 60% to 100% in AlGaN 1 layer. Al mole fraction is 80% in other AlGaN layers. (b) varying AlGaN 1 layer thickness form 11nm to 31nm. L_{PSJ}=20μm, t_{GaN}= t_{AlGaN}=11nm and N=4.

Combined the calculated prediction with ideal simulated results, the theoretical limit trade-offs between BV and $R_{(on, sp)}$ of lateral multi-channel PSJ devices are shown in Figure 5.11. Both the calculated and simulated $R_{(on, sp)}$ present a downward trend with increase in the number of PSJ multi-channels. Hence, developing a device with a multi-channel PSJ structure is essential. The multi-channel PSJ technology not only offers the potential of breaking the material limit but also has the chance to reduce $R_{(on, sp)}$ to 10^{-8}mΩ·cm^2 level. Altering from *N=100* to *N=1000*, $R_{(on, sp)}$ can be further reduced, whereas the total channel thickness is increased to a relatively thick level.

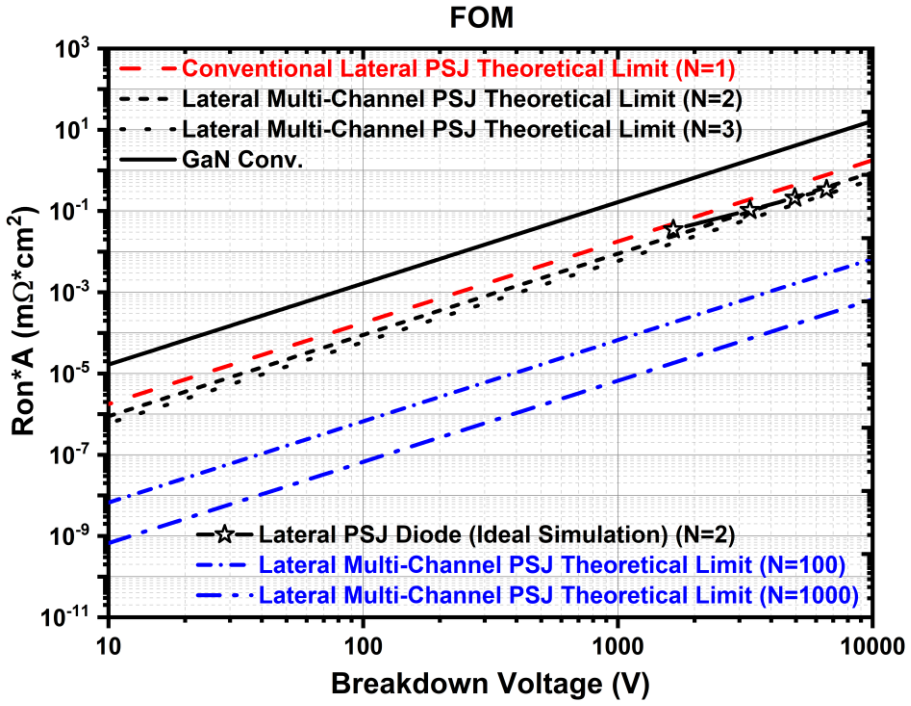


Figure 5.11 $R_{(on, sp)}$-BV trade-off for ideal prediction of lateral multi-channel PSJ devices. N is the number of multi-channels.

5.3 Feasible Devices Simulation

Unlike the ideal theoretical prediction, when considering designing and fabricating practical lateral multi-channel PSJ devices, the issues mentioned above cannot be ignored. The critical thickness for strain relaxation limits the trade-off between Al mole fraction and AlGaN layer thickness [80, 82, 93]. Thin AlGaN layer and lower Al composition can enhance epitaxial material quality. Therefore, in the reliable lateral multi-channel PSJ devices simulation, the Al mole fraction should not exceed 40% [93] and the thickness of the AlGaN layer is not thicker than 60nm [48, 80, 93].

5.3.1 On-state Performance for Lateral Multi-channel PSJ Devices

The simulated I_{AC}-V_{AC} for lateral multi-channel PSJ diodes with 40nm u-AlGaN and 200nm u-GaN is shown in Figure 5.12(a). The conduction current scales linearly with the number of the multi-channels (N). With the increase in the multi-channel number, the $R_{(on, sp)}$ of lateral multi-channel PSJ devices reduces significantly, as shown in Figure 5.12(b).

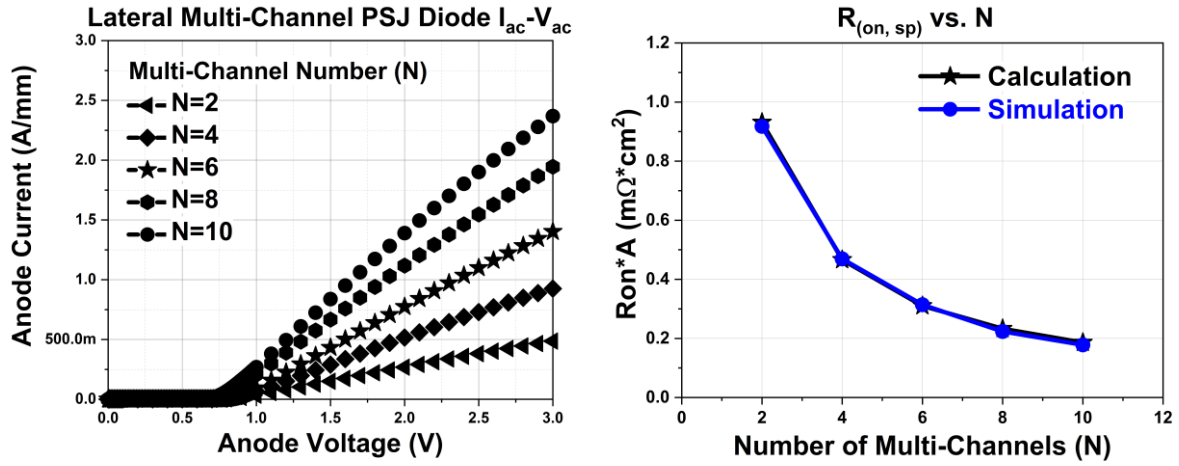
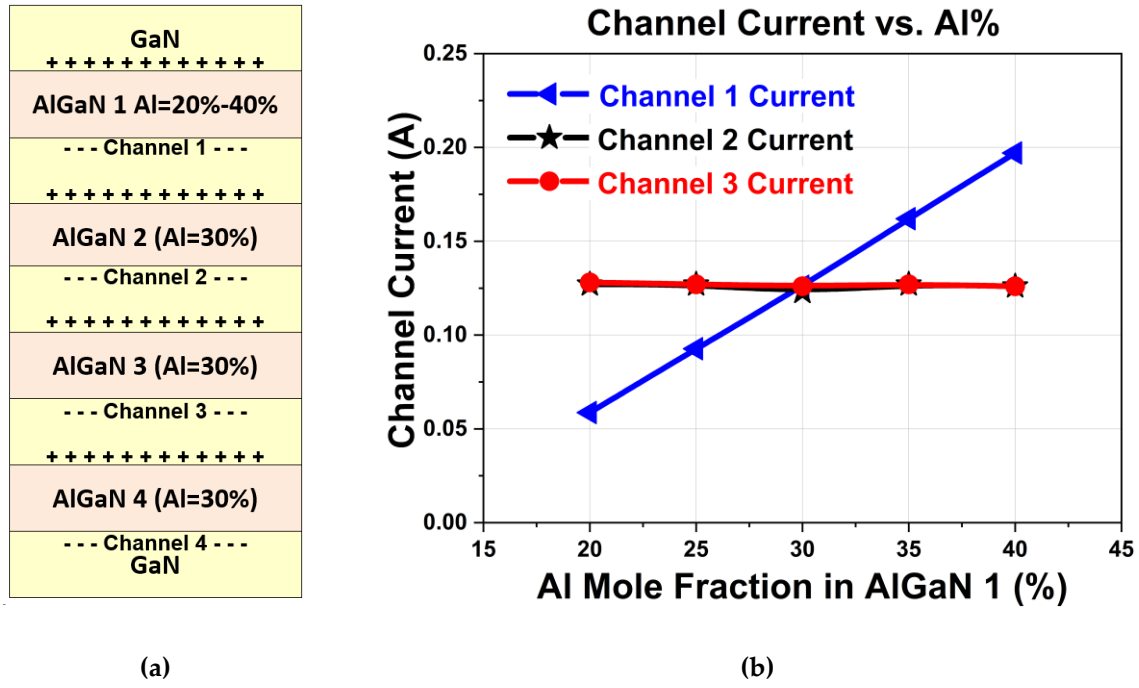


Figure 5.12 (a) I_{AC}-V_{AC} simulated comparison characteristics of lateral multi-channel PSJ diode with t_{GaN}=200nm, t_{AlGaN}=40nm and Al=30%. The multi-channel number (N) is varied from 2 to 10. (b) Dependence of $R_{(on, sp)}$ on the number of multi-channels in the same lateral PSJ diode with L_{PSJ}=20μm.

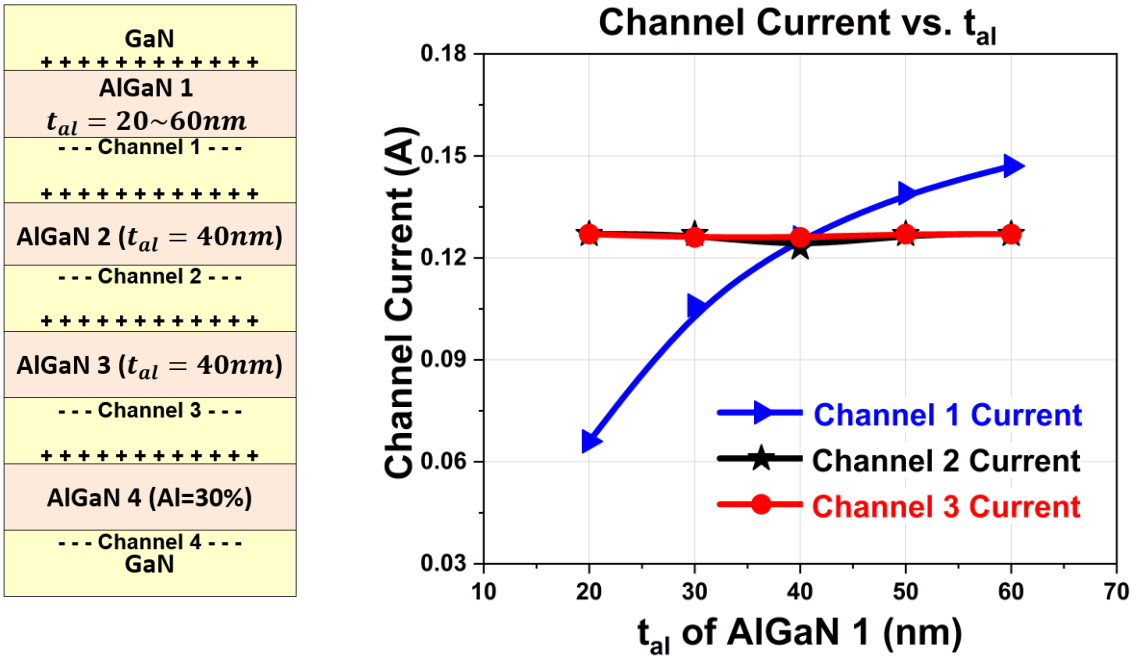
The average mobility of 2DEG is 1200cm²/Vs in the calculation. Figure 5.13(a) demonstrates the simulated lateral multi-channel PSJ structure with four parallel channels. As shown in Figure 5.13(b), altering the Al mole fraction in AlGaN 1 layer from 20% to 40% while keeping the Al mole fraction at 30% in other AlGaN layers leads to non-uniform current conduction.



(a) (b)

Figure 5.13 (a) Schematics of the lateral multi-channel structure when the number of the channels is four (*N*=4). (b) Current in different channels when altering the Al mole fraction from 20% to 40% in AlGaN 1 layer and Al mole fractions are 30% in AlGaN 2, 3 and 4. V_{AC}=2*V*, L_{PSJ}=20*μm*, t_{AlGaN}=40nm and t_{GaN}=200nm.

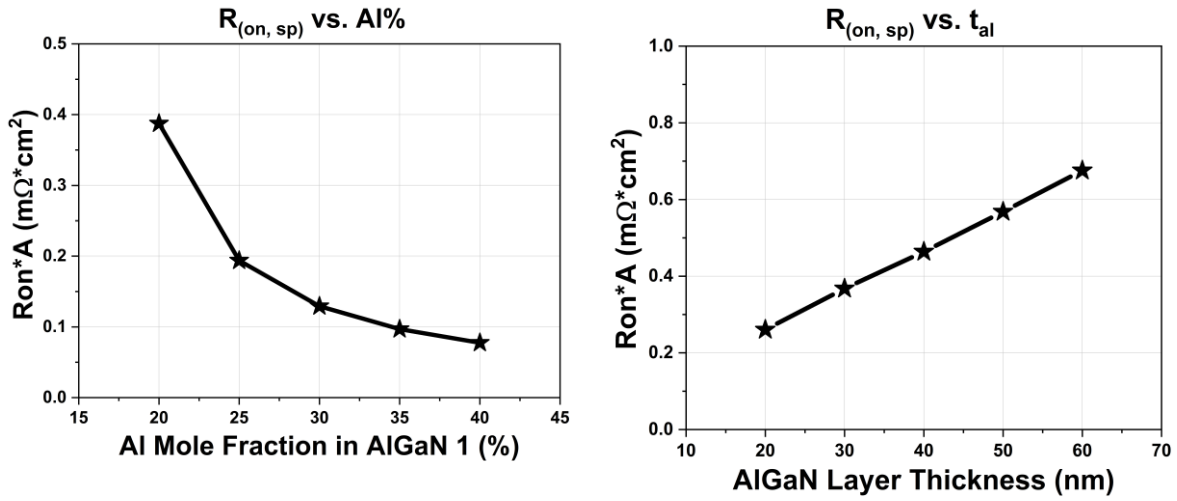
The current merely increases in Channel 1, since σ_{AlGaN}, n_{2DEG} and the channel current are linked together and increased with the increase in Al mole fraction as presented in (5.20). The current in Channel 3 is regarded as the reference current and almost equal to Channel 2 current. As shown in Figure 5.14(b), varying the thickness of AlGaN 1 layer from 20nm to 60nm and keeping all other AlGaN layers thickness identical to 40nm also leads to non-uniform current conduction across the channels.



(a) (b)

Figure 5.14 (a) Schematics of the lateral multi-channel structure when the number of the channels is four (N=4). (b) Current in different channels when altering AlGaN 1 thickness (t_{Al}) from 20nm to 60nm and Al mole fractions keep in 30%. V_{AC}**=2V,** L_{PSJ}**=20μm,** t_{AlGaN}**=40nm and** t_{GaN}**=200nm.**

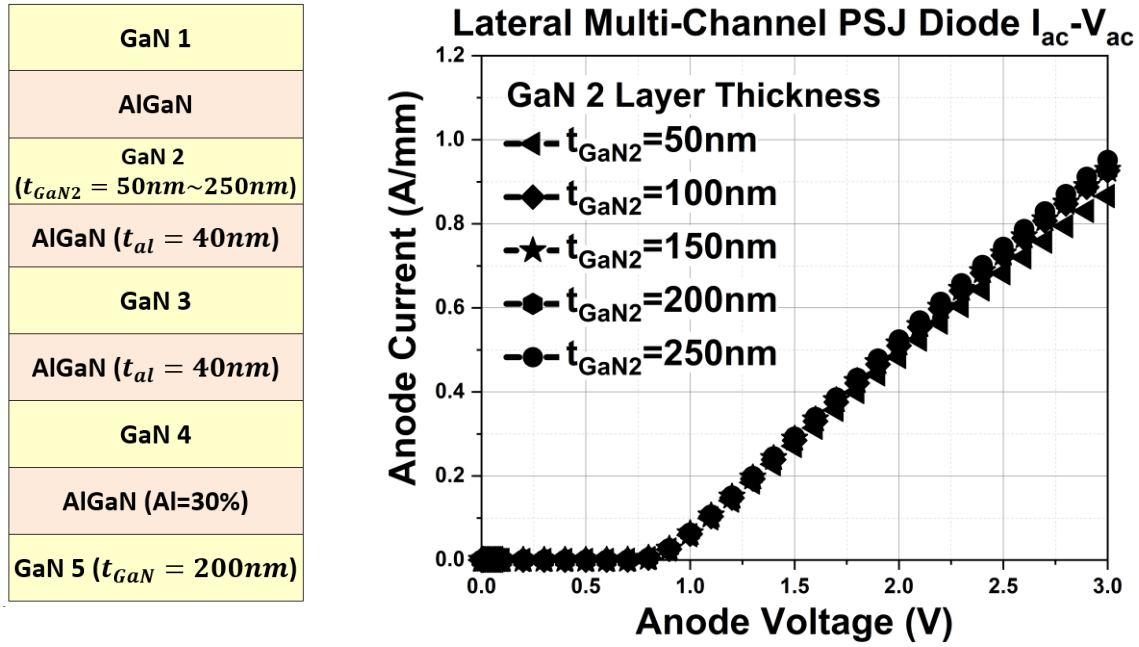
Figure 5.15(a) shows that the $R_{(on, sp)}$ reduces when the Al mole fraction increases in one of AlGaN layers. Based on the results above, even slightly changing Al composition or the thickness of the AlGaN layer can lead to non-uniformity of current conduction. Therefore, composition and thickness control are critical in these multi-channel PSJ structures.



(a) **(b)**

Figure 5.15 Simulated $R_{(on, sp)}$ (a) varying Al mole fraction from 20% to 40% in AlGaN 1 layer. Al mole fraction is 30% in other AlGaN layers. (b) varying AlGaN 1 layer thickness form 20nm to 60nm.

When GaN thickness increase in one of the GaN layers and higher than the critical value for generating 2DEG, device total current almost does not change as shown in Figure 5.16(b).



(a) **(b)**

Figure 5.16 (a) Schematics of the lateral multi-channel structure when the number of the channels is four (N=4). (b) I_{AC}-V_{AC} simulated comparison characteristics when altering GaN 1 thickness (t_{GaN1}) from 50nm to 200nm and Al mole fractions keep in 30%. V_{AC}=2V, L_{PSJ}=20μm, t_{AlGaN}=40nm and t_{GaN}=200nm.

5.3.2 Blocking Capability for Lateral Multi-channel PSJ Devices

In the off state of lateral multi-channel PSJ devices, both lateral and vertical electric fields should not exceed the critical electric field to avoid the breakdown. Figure 5.17(b) and Figure 5.17(c) show the vertical and lateral electric field distribution along the cutline shown in Figure 5.17(a) when varying cathode voltage from 0V to 6600V. 2DEG and 2DHG deplete at low cathode voltages. Figure 5.17(b) shows that the

vertical electric field first increases when varying cathode voltage from 0V to 10V. Further growing the cathode voltage from 10V to 100V, with the depletion of 2DEG and 2DHG, the vertical electric field reduces and approaches zero. Within a further increase in the cathode voltage, the lateral electric field increases with a rectangular shape distribution until the maximum blocking capability of the device (6600V theoretical), as demonstrated in Figure 5.17(c).

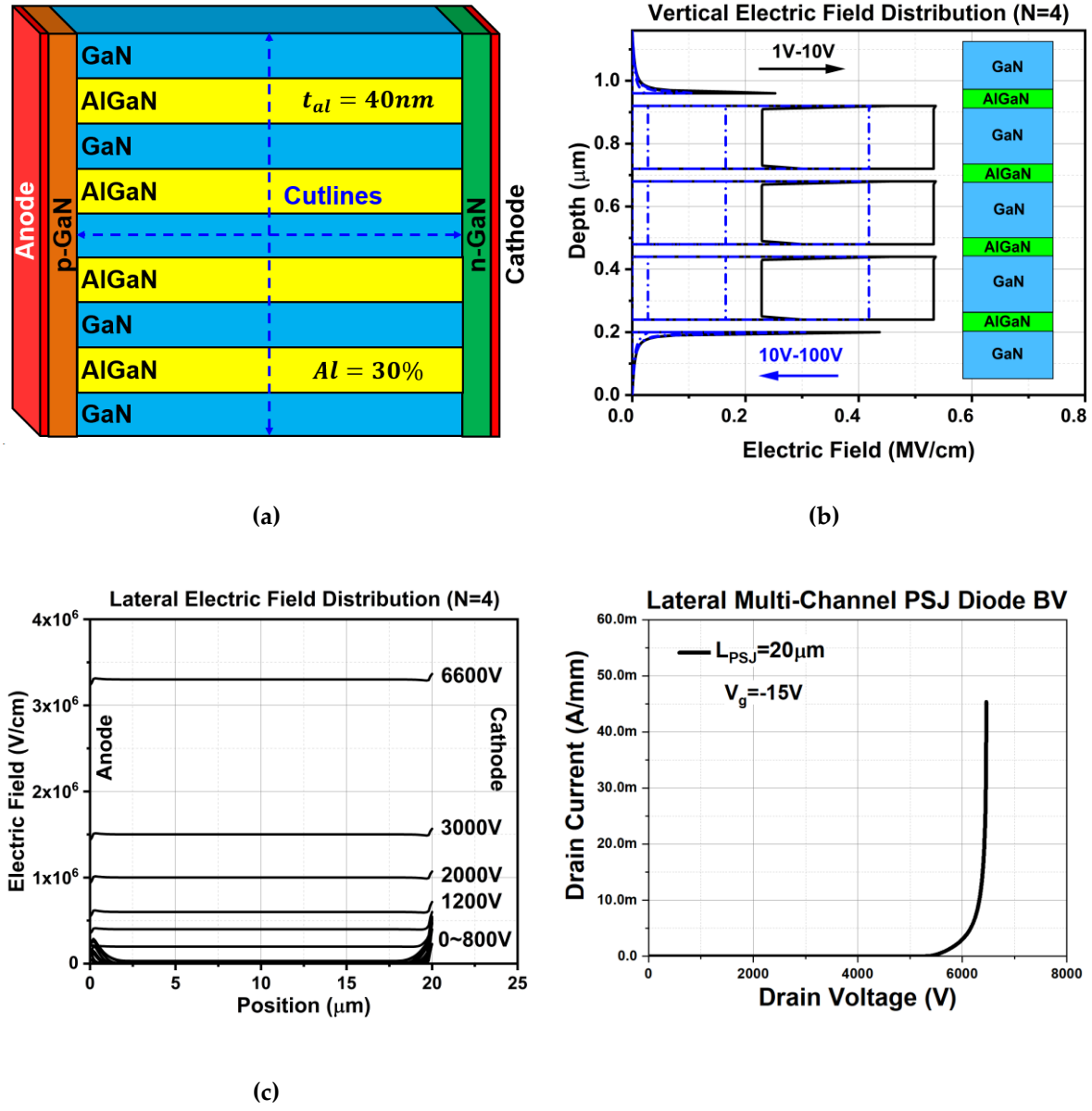
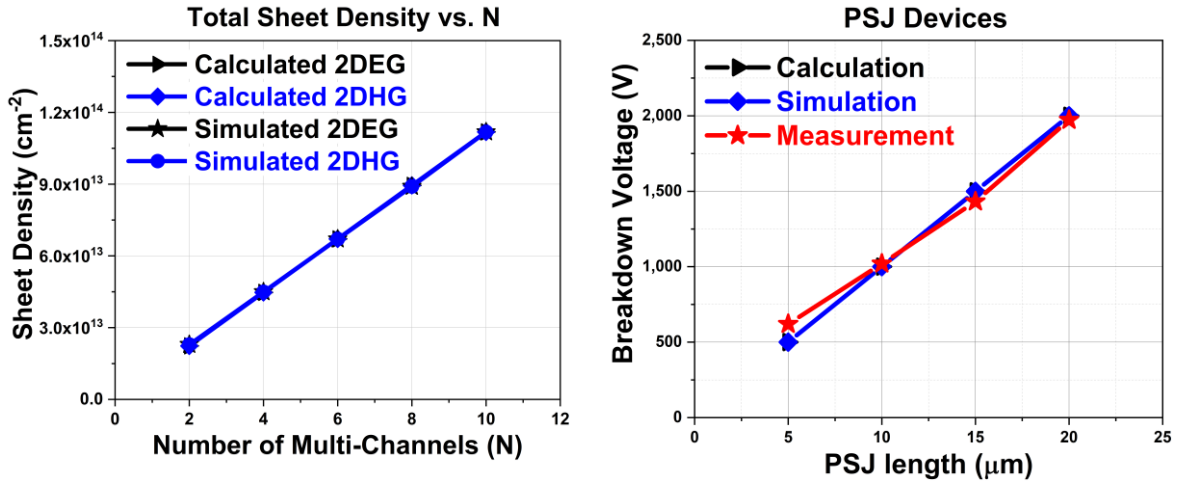


Figure 5.17 (a) Schematics of the lateral multi-channel structure when the number of the channels is four (*N=4*). (b) Vertical and (c) Lateral simulated electric field profile along x axis direction of lateral multi-channel (*N=4*) PSJ diodes plotted along the high field PSJ region (from anode to cathode), at blue dashed cutline when various reverse bias conditions from 0V to

6600V. (d) Simulated off-state I_d-V_d characteristics of the lateral multi-channel PSJ Diode (N=4 L_{PSJ}=20μm)

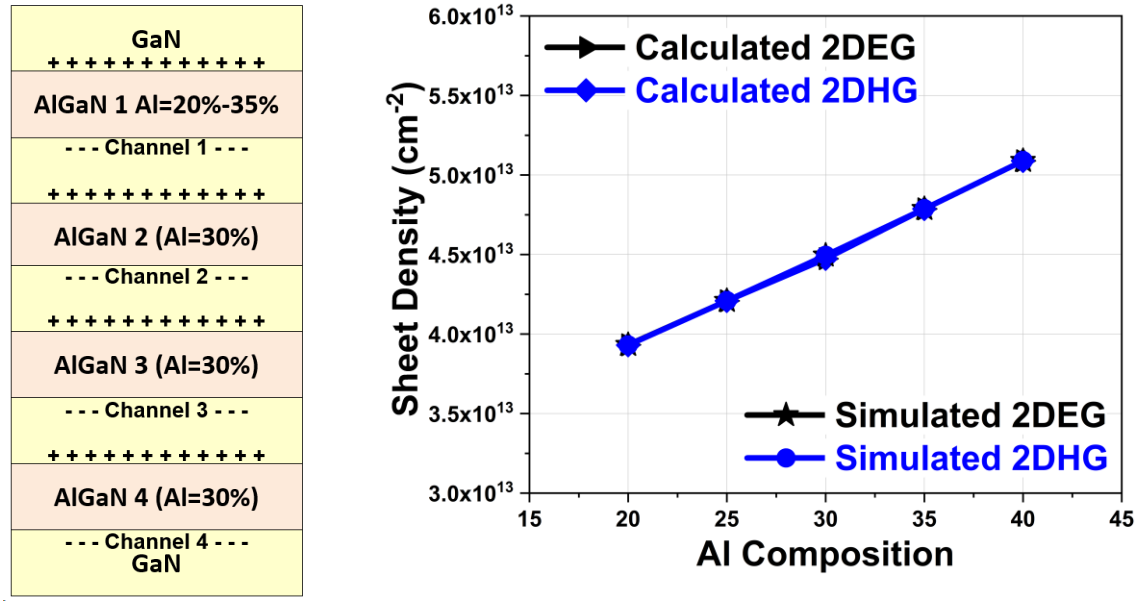
As shown in Figure 5.18(a), each additional channel equally increases the total sheet charge density of 2DEG and 2DHG by 1.1×10^{13} cm^{-2}, since in lateral multi-channel PSJ devices, each 2DEG layer corresponds with a 2DHG layer. The sheet charge densities of 2DEG and 2DHG are always equal in each channel.



(a) **(b)**

Figure 5.18 (a) The total sheet charge density of 2DEG and 2DHG when the multi-channel number (*N*) is varying from 2 to 10. (b) BV calculated, simulated and measured output characteristics of lateral multi-channel PSJ devices when shifting L_{PSJ} from 5μm to 20μm at V_g=-15V.

Even altering Al composition in one of the AlGaN layers does not influence the charge balance condition, as shown in Figure 5.19(b).



(a) **(b)**

Figure 5.19 (a) Schematics of the lateral multi-channel structure when the number of the channels is four (*N*=4). (b) The total sheet charge density of 2DEG and 2DHG when altering the Al mole fraction from 20% to 40% in AlGaN 1 layer and Al mole fractions are 30% in AlGaN 2, 3 and 4. L_{PSJ}=20μm, t_{AlGaN}=40nm and t_{GaN}=200nm.

The electric field distribution is almost identical in each GaN layer when the Al mole fraction changes in one of the AlGaN layers, as presented in Figure 5.20.

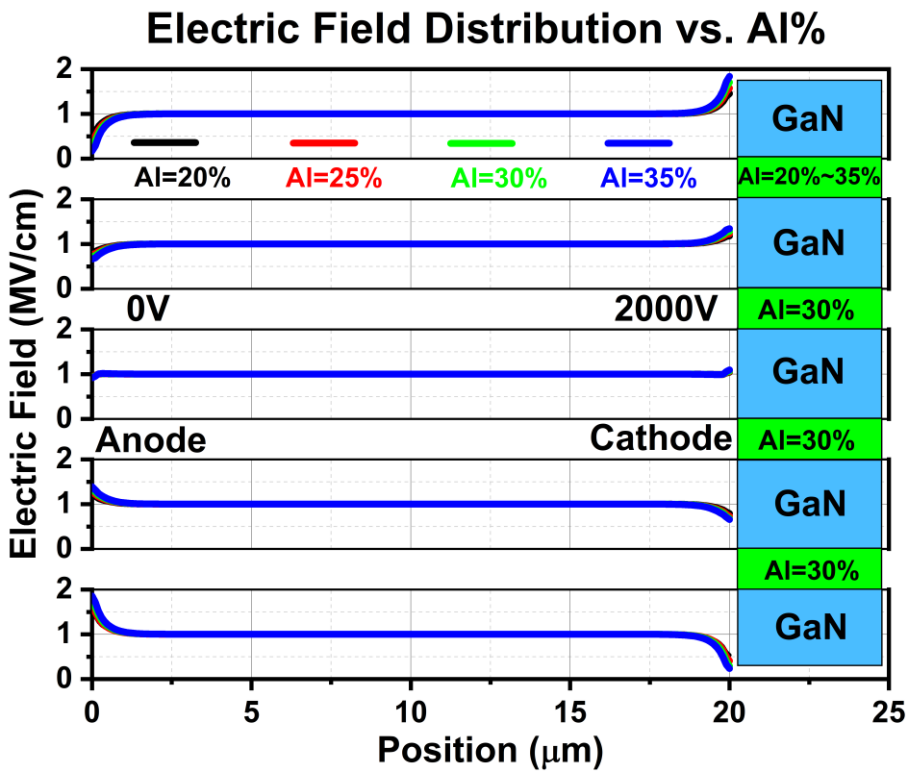


Figure 5.20 Schematics of the lateral multi-channel structure when the number of the channels is four (*N=4*) and lateral electric field distribution (2000V) when altering the Al mole fraction from 20% to 35% in AlGaN 1 layer and Al mole fractions are 30% in AlGaN 2, 3 and 4. L_{PSJ}=20μm, t_{AlGaN}=40nm and t_{GaN}=200nm.

Figure 5.18(b) is the comparison among calculated, simulated and measured BV when L_{PSJ} increases from 5μm to 20μm. The experimental BV electric field shows a linear increase with respect to the L_{PSJ} and an average breakdown field strength between 1-1.5MV/cm. Hence, in the simulation of multi-channel PSJ devices, the critical electric field can be reasonably assumed as 1MV/cm.

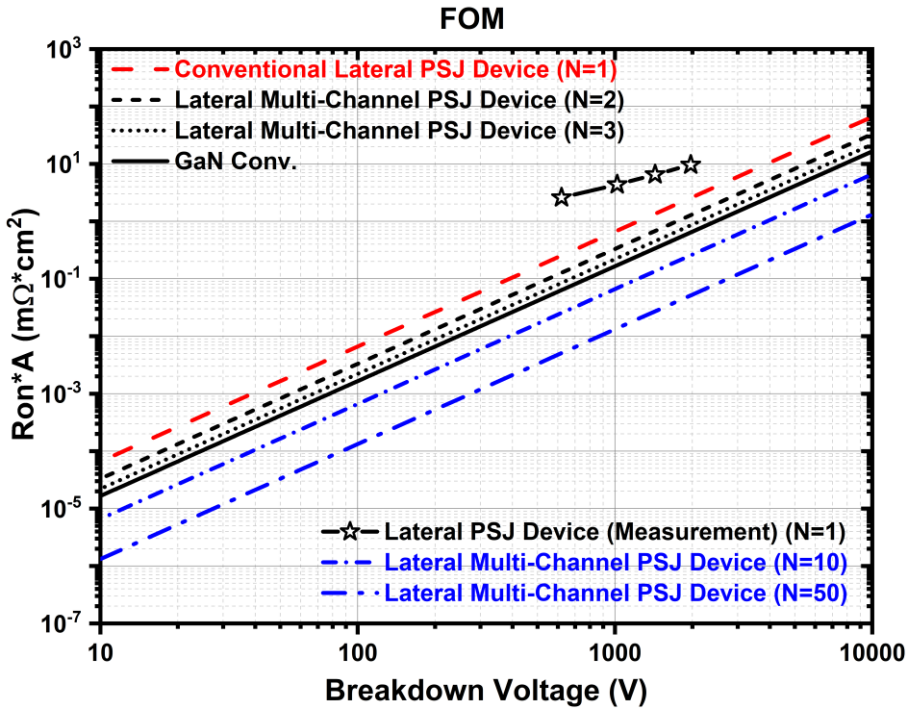


Figure 5.21 $R_{(on, sp)}$**-***BV* **trade-off for practical design of lateral multi-channel PSJ devices.** ***N*** **is the number of multi-channels.**

Combined the calculated and simulated results, the trade-offs between BV and $R_{(on, sp)}$ of lateral multi-channel PSJ devices are shown in Figure 5.21. To estimate the performance of realizable devices, in both calculations and simulations, the assumed Al composition is 27% and the thickness of AlGaN layer is 40nm in each channel. In lateral PSJ devices, both the calculated and simulated $R_{(on, sp)}$ present a downward trend when the number of PSJ multi-channel increases. It shows that $R_{(on, sp)}$ of PSJ devices with three lateral multi-channels can reach GaN material limit. Further increasing the number of channels, lateral multi-channel PSJ devices can easily break GaN material limits and $R_{(on, sp)}$ is reduced to a relatively low level. The multi- channel PSJ technology offers the potential of breaking the material limit provided composition and thickness control can be realised.

5.4 Summary

In lateral multi-channel PSJ devices, when the layer (GaN, AlGaN or AlN) thickness is 11nm, the $R_{(on, sp)}$ reaches the minimum value (theoretical limit). Simulated results show that the charge is invariably balanced between the 2DEG and 2DHG layer when altering the Al more fraction in the AlGaN layer. Both calculated and simulated results show that 2DEG (2DHG) is independent in different channels. Changing the Al composition and thickness of the AlGaN layer cannot impact 2DEG (2DHG) sheet density in other channels. The trade-off between BV and $R_{(on, sp)}$ in lateral multi-channel PSJ technology can potentially break the GaN material limit. With the same blocking capability, $R_{(on, sp)}$ in devices with ten lateral multi-channels (N=10) can effectively be reduced by two-thirds compared to conventional GaN devices. Moreover, in low-voltage applications, lateral multi-channel PSJ technology can potentially realize more than two orders of magnitude lower $R_{(on, sp)}$ compared to conventional, single-channel PSJ devices under the same device blocking capability. In conclusion, the proposed multi-channel engineering is an effective and viable solution to realize ultra-highly efficient GaN-based power semiconductor devices. In addition to the potential increase in power density, this technology can pave the way for the next generation of power semiconductor devices.

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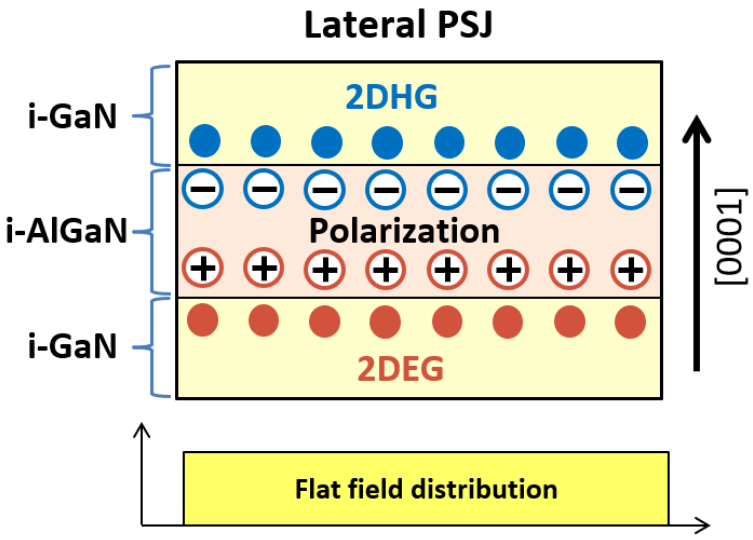
Chapter 6 VERTICAL MULTI-CHANNEL PSJ TECHNOLOGY

This chapter analyses the theoretical limit of area-specific on-state resistance ($R_{(on, sp)}$) on vertical polarisation super-junction (PSJ) technology. $R_{(on, sp)}$ on nano-scale vertical multi-channel PSJ technology is analysed (wrong ref 73 delated). Theoretical models, which are calibrated with numerical simulations, are used to calculate the $R_{(on, sp)}$ of these nano-scale vertical Polarisation SJ (VIP-SJ) diodes. In both calculated and simulated results of $R_{(on, sp)}$, devices with vertical multi-layer PSJ structures are found to break the unipolar one-dimensional material limits of GaN by orders of magnitude. Both calculated and simulated results show power devices with vertical multi-layer PSJ technology can potentially reduce $R_{(on, sp)}$ to 10^{-4}mΩ·cm^2 level with 1.2kV blocking capability. In this chapter, it also proposed a novel multi-polarization channel applied to realize normally-off and high-performance vertical GaN device devices for low voltage applications based on the previous discussion. This structure is made with 2DHG introduced to realize the enhancement mode channel instead of p-GaN as in conventional vertical GaN MOSFETs. Two more 2DEG layers are formed through AlGaN/GaN/AlGaN/GaN polarization structure, which minimizes the on-state resistance. Simulation analysis shows that this proposed structure can provide a large drain current at ~ 500mA/mm. The calculation results show this novel vertical GaN MOSFET – termed SV GaN FET - has the potential to break the GaN material limit in the trade-off between area-specific on-resistance ($R_{(on, sp)}$) and breakdown voltage at low voltages.

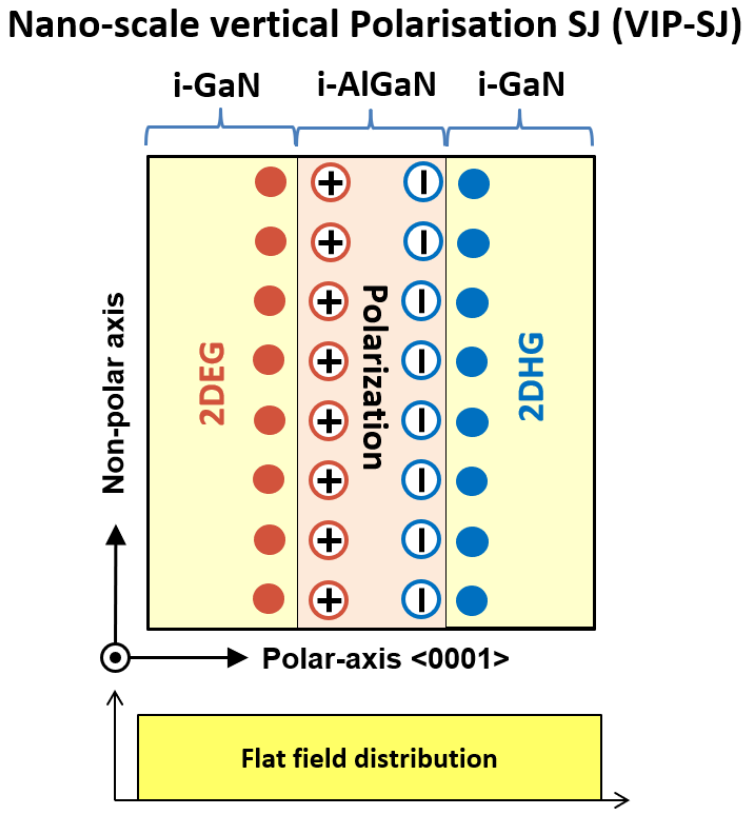
6.1 Introduction

In the previous chapters, considering integrated power conversion systems, due to the high concentration of thin 2DEG realized through piezoelectric properties, AlGaN/GaN-based heterojunction field-effect transistors (HFETs) offer remarkable

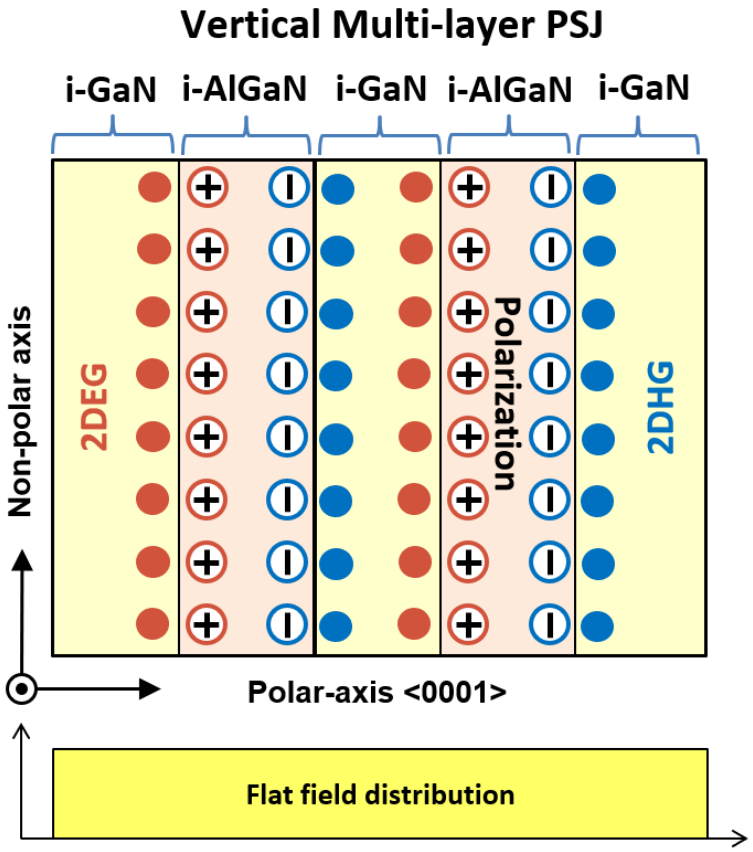
properties of low on-state resistance [94]. In vertical GaN devices, thus far, no significant performance advantage beyond 4H-SiC has been realized in the trade-off between the area-specific on-state resistance ($R_{(on,\ sp)}$) and the breakdown voltage. To break the 1-Dimensional material limit, super-junction (SJ) concept was introduced in silicon [9, 95]. However, as to dopant-based approach is immature in GaN, it is difficult to precisely control p-type Mg activation for charge balance purposes [96]. To overcome the 1-D material limit, as shown in Figure 6.1(a), the lateral Polarization Super Junction (PSJ) technology was applied to nano-scale vertical polarisation super junction (VIP-SJ) in 2017 as shown in Figure 6.1(b) [45, 50, 76]. The basic PSJ structure arises from GaN/AlGaN/GaN double-heterostructure, which employs an inherent charge balance in the PSJ region. The PSJ concept is based on the polarization property of III–V group nitride compound semiconductors to realize the co-existence of high-density two-dimensional electron gas (2DEG) and two-dimensional hole gas (2DHG) at the hetero- interfaces to realize charge balance [50].



(a)


Nano-scale vertical Polarisation SJ (VIP-SJ)
i-GaN
i-AlGaN
i-GaN
2DEG
Polarization
2DHG
Non-polar axis
Polar-axis <0001>
Flat field distribution

(b)


Vertical Multi-layer PSJ
i-GaN
i-AlGaN
i-GaN
i-AlGaN
i-GaN
2DEG
Polarization
2DHG
Non-polar axis
Polar-axis <0001>
Flat field distribution

(c)

Figure 6.1 Schematic cross section and simplified electric field distribution of (a) conventional PSJ structure and (b) nano-scale vertical Polarisation SJ (VIP-SJ) structure (c) Vertical Multi-Channel PSJ Structure.

It can potentially break the one-dimensional material trade-off between the $R_{(on, sp)}$ and the breakdown voltage of conventional GaN technology [70]. As improvements have been made in the growth/over-growth of high-aspect-ratio GaN-based nano-columns on polar/non-polar bulk GaN substrates, a highly innovative solution of fabricating vertical PSJ devices can be potentially realized [76, 77, 97]. Furthermore, if the stacks number of AlGaN/GaN layers is increased, based on the PSJ structure, the multi-layer PSJ concept is proposed, as shown in Figure 6.1(b). As shown in Figure 6.1(c), based on the VIP-PSJ concept, the number of AlGaN/GaN layers can be increased most compactly. For low voltage devices, the required vertical etches and (re) growth controls are within a few micrometres into GaN and viable with recent advances in GaN process technologies. With this in mind, theoretical limits $R_{(on, sp)}$ of vertical nano-pillar PSJ technology are investigated and compared with GaN-dopant based SJ technology by analytical models and numerical models. The multi-layer PSJ concept is different from nature super-junction (NSJ), and as shown in Figure 6.1(b), in a typical multi-layer PSJ device, each 2DEG layer corresponds with a 2DHG layer to implement the charge balance condition [78]. Hence, compared with NSJ technology, a perfect box-like electric field distribution can still be realized in vertical multi-layer PSJ devices.

In this chapter, the theoretical limit $R_{(on, sp)}$ vertical multi-layer PSJ technology are investigated and compared with GaN-based SJ technology by analytical and numerical models.

6.2 Vertical PSJ Device Theoretical Limit Prediction

As non-polar GaN is widely used in optoelectronic applications, through growing Wurtzite GaN along non-polar axes, the orientation of the intrinsic polarisation can be converted to the lateral direction in the grown layers, which contributes to fabricating vertical multi-layer PSJ devices [76]. In predicting the theoretical limit for PSJ devices, analytical models of 2DEG and 2DHG adopted herein are compared with numerical simulation and experimental data [47, 48]. Considering the $R_{(on,\ sp)}$ calculation in vertical devices is different from that in lateral devices, therefore, it needs to be divided into two situations.

6.2.1 The Theoretical Limit for Vertical SJ Devices

In conventional vertical SJ devices, the method to simultaneously realize high breakdown voltage and low $R_{(on,\ sp)}$ is through controlling the p-type and n-type layers doping concentration [9]. The relationship between $R_{(on,sp)}$ and device blocking capability (V_B) is given in (6.1)

$$R_{on} \times A = \frac{4dV_B}{\mu\varepsilon_S {E_C}^2} \tag{6.1}$$

Where $R_{on}\times A$ is $R_{(on,\ sp)}$ and d is the thickness of SJ layer. V_B stands device breakdown voltage. μ is the carrier mobility. ε_S and E_C are permittivity and critical electric field of the semiconductor material.

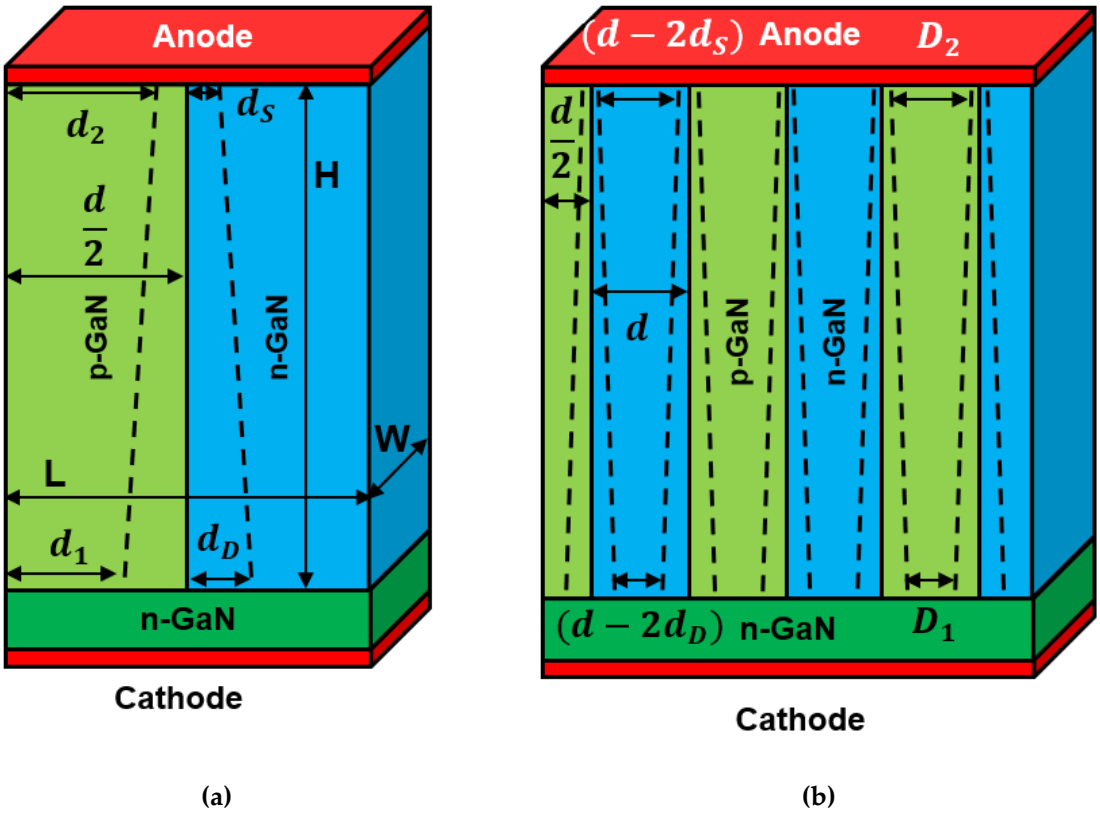


Figure 6.2 3-D schematic cross section of simplified (a) vertical SJ diode with one p-GaN and n-GaN layer (b) vertical SJ diode with p-GaN and n-GaN multi layers.

When considering the JFET effect, in the SJ device with one p-pillar and one n-pillar, as shown in Figure 6.2(a), the expression for $R_{(on,sp)}$ is shown in (6.2) [98].

$$R_{on} \times A = \frac{d\rho H}{(d_2 - d_1)} ln\left(\frac{d_2}{d_1}\right) \qquad (2)$$

Where ρ is the resistivity of the n-doped region and H represents the length of the drift region. d_2 and d_1 are the major and minor width of the trapezoid drift region, respectively, as shown in Figure 6.2(a) and can be obtained from (6.3) and (6.4) [98].

$$d_2 = \frac{d}{2} - d_S = \frac{d}{2} - \sqrt{\frac{2\varepsilon_S V_{bi}}{q} \frac{N_A}{N_D(N_A + N_D)}} \qquad (6.3)$$

$$d_1 = \frac{d}{2} - d_D = \frac{d}{2} - \sqrt{\frac{2\varepsilon_S(V_{bi} + V_D)}{q}\frac{N_A}{N_D(N_A + N_D)}} \qquad (6.4)$$

Where d_S and d_D are depletion width at the source and drain side, respectively. V_{bi} stands for the junction built-in potential and V_D is the drain applied voltage. N_A and N_D represent doping concentration [98]. As the number of p-pillar and n-pillar increases, the JFET region and depletion region should be considered both from the right and left sides, as shown in Figure 6.2(b). Therefore, in the SJ device with multi-layers, the expression for $R_{(on, sp)}$ is revised to (6.5).

$$R_{on} \times A = \frac{2d\rho H}{(D_2 - D_1)} ln\left(\frac{D_2}{D_1}\right) \qquad (6.5)$$

Where D_2 and D_1 stand for modified major and minor width of the trapezoid drift region.

6.2.2 The Theoretical Limit for Vertical PSJ Devices

In vertical multi-layer PSJ devices, the 3-D cross-section, which consists of u-AlGaN/u-GaN multi-layers, is shown in Figure 6.3.

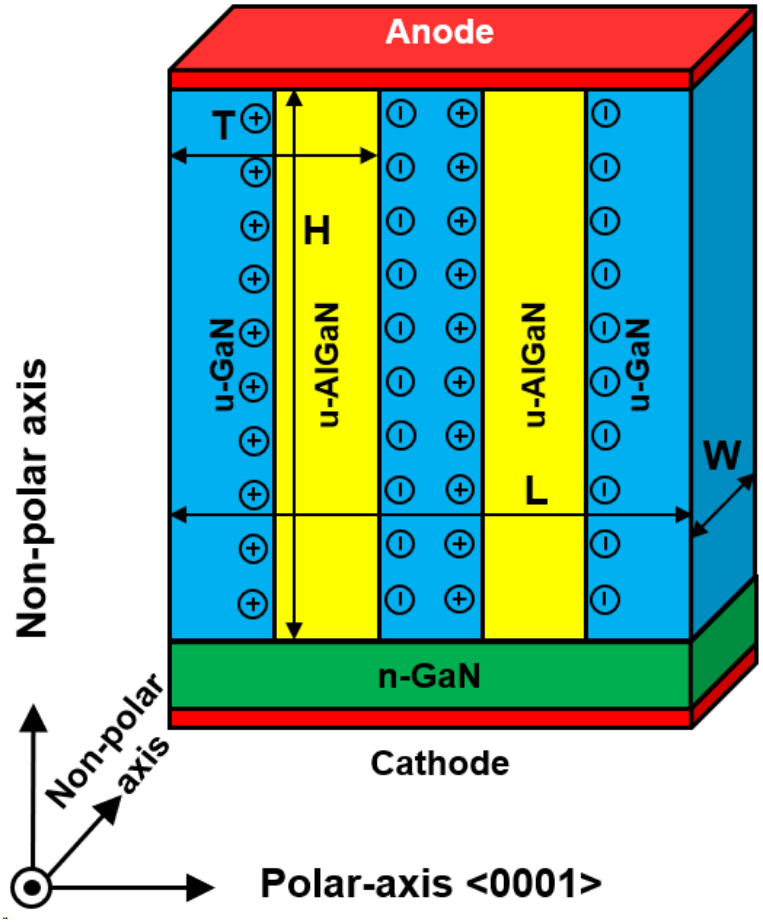


Figure 6.3 3-D schematic cross section of simplified vertical PSJ diode.

In the multi-layer vertical PSJ diode, a rectangle shape of electric field distribution can be realized because of the charge balance of 2DEG and 2DHG. Therefore, the expression for $R_{(on,\,sp)}$ of the vertical PSJ device is shown as (6.6).

$$R_{on} \times A = \frac{1}{q\mu_{2DEG}n_{2DEG}} \times \frac{H}{L \cdot W} \times L \cdot W = \frac{H}{q\mu_{2DEG}n_{2DEG}} = \frac{V_B}{q\mu_{2DEG}n_{2DEG}E_C} \tag{6.6}$$

Where q is the electron charge and μ_{2DEG} is the mobility of 2DEG. n_{2DEG} represents the average concentration of 2DEG. $t_{n\text{-}GaN}$ is n-GaN layer thickness. H is the height of the PSJ diode as well as the length of the PSJ region ($H \gg t_{n\text{-}GaN}$). It is also the critical factor for device blocking capability ($H=V_B/E_{crit}$). W is the width of the device and L stands for the total thickness of u-GaN/u-AlGaN multi-layers. To minimum $R_{(on,\,sp)}$, analyzing

(6.6) and referring to a given device volume (equivalent H, W and L), it is evident that μ_{2DEG} and n_{2DEG} should be maximum.

$$n_{2DEG} = \frac{\sigma_{2DEG}}{T} \tag{6.7}$$

(6.7) shows the relationship between n_{2DEG} and unit area 2DEG sheet charge density (σ_{AlGaN}). The model of σ_{AlGaN} is consistent with the reported work [47, 48]. T stands for the total thickness of one u-GaN layer and one u-AlGaN layer. $H=V_B/E_{crit}$ associate device breakdown voltage to the length of the PSJ region (L). Substitute (6.7) into (6.6), the expression of the trade-off between $R_{(on,sp)}$ and V_B can be derived into (6.8).

$$R_{on} \times A = \frac{V_B \times T}{q\mu_{2DEG}E_{crit}\sigma_{2DEG}} = \frac{H}{q\mu_{2DEG}(\sigma_{2DEG}/T)} \tag{6.8}$$

Based on (6.9), to optimize the trade-off between $R_{(on, sp)}$ and V_B is to the minimum $R_{(on, sp)}$, simultaneously, remaining the device blocking capability (V_B). L is given a fixed value in the derivation and proportion to V_B. As shown in (6.9), the critical element to reduce $R_{(on, sp)}$ is to increase n_{2DEG} (σ_{2DEG}/T). Besides, a multi-layer PSJ device needs the charge balance to realize the 'box' shape electric field distribution. The sheet density of each 2DEG and 2DHG layer is equivalent. Therefore, all u-GaN layer thickness should be identical and is defined as t_{GaN} as well as all u-AlGaN layer thickness is t_{AlGaN}. The number of u-GaN/u-AlGaN multi-layers is n. Figure 6.4 shows the sectional band diagram of the multi-layer structure in a PSJ device.

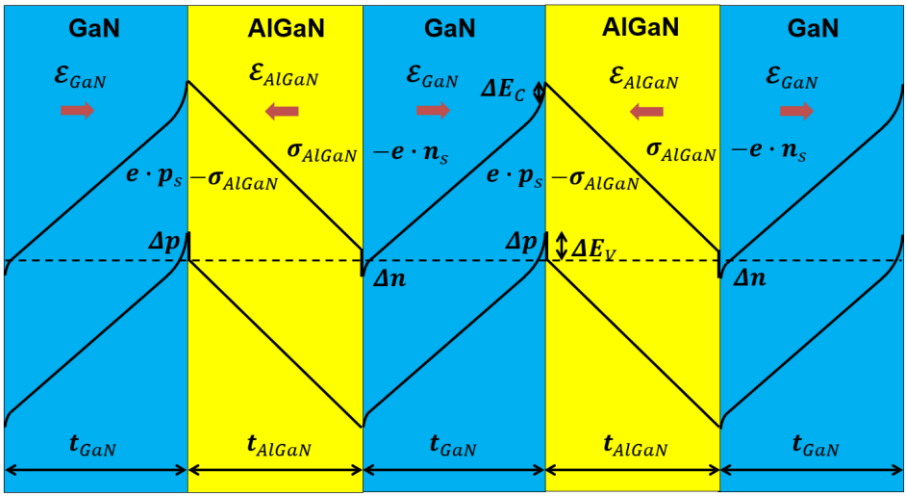


Figure 6.4 Schematic band diagrams of u-GaN/u-AlGaN Multi-layer PSJ heterostructure.

To obtain the expression for σ_{2DEG}, use the same methods in 5.2.1, according to 'Gauss' law at each interface of u-AlGaN/u-GaN and u-GaN/u-AlGaN [71, 72]. In consequence, the final solution for n_{2DEG} is shown in (6.9).

$$n_{2DEG} = \frac{\sigma_{2DEG}}{T} = \frac{\sigma_{AlN} - \left(\frac{34.8\varepsilon_0}{T}\right) \cdot \frac{E_G}{e}}{eT} \qquad (6.9)$$

In the derivation, the PSJ length is defined as 20μm as well as the SJ pillar length. Substitute the solution in (6.9) into (6.8) and varies u-GaN thickness ($T/2$) to obtain the minimum $R_{(on,\,sp)}$.

In the numerical simulation, physics-based solutions for the sheet density of 2DEG and 2DHG are achieved in Silvaco by using models, such as spontaneous polarization (POLAR), piezoelectric polarization (CALC.STRAIN), Shockley–Read–Hall recombination using concentration-dependent lifetimes (CONSRH), and recombination accounting for high-level injection effects (AUGER) to obtain reliable results. The models used in the simulation are based on default parameters for comparison [52]. When increasing the number of AlN (AlGaN)/GaN multi-layer in the practical fabrication of the device, the difficulty will increase. In order to estimate the theoretical limit of the PSJ device in the ideal situation, all parameters in the simulation are idealized. In the perfect case, the contact resistance is approaching zero. In the

theoretical limit calculation of $R_{(on,\ sp)}$., the contact resistance of anode and cathode electrodes can be ignored. In GaN SJ calculation, the mobility model is based on Caughey–Thomas mobility model as shown in (6.10) [87].

$$\mu_i(N) = \mu_{min,i} + \frac{\mu_{max,i} - \mu_{min,i}}{1 + \left(\frac{N}{N_{g,i}}\right)^{\gamma_i}} \tag{6.10}$$

Where i stands for n-type or p-type carriers and N represents doping concentration. $\mu_{min,\ i}$, $\mu_{max,\ i}$, $N_{g,\ i}$ and γ_i are default parameters in the model as shown in Table 6.1 [87].

Carriers Type	$\mu_{(min,i)}$	$\mu_{(max,i)}$	$N_{(g,i)}$	γ_i
n	55	1000	2×10^{17}	1.0
p	3	170	3×10^{17}	2.0

Table 6.1 Parameters for GaN in the Mobility Model.

In vertical PSJ devices, the mobility is assumed as 1000cm^2/Vs in both calculation and simulation because it reduces with the increase of carrier concentration [28, 91].

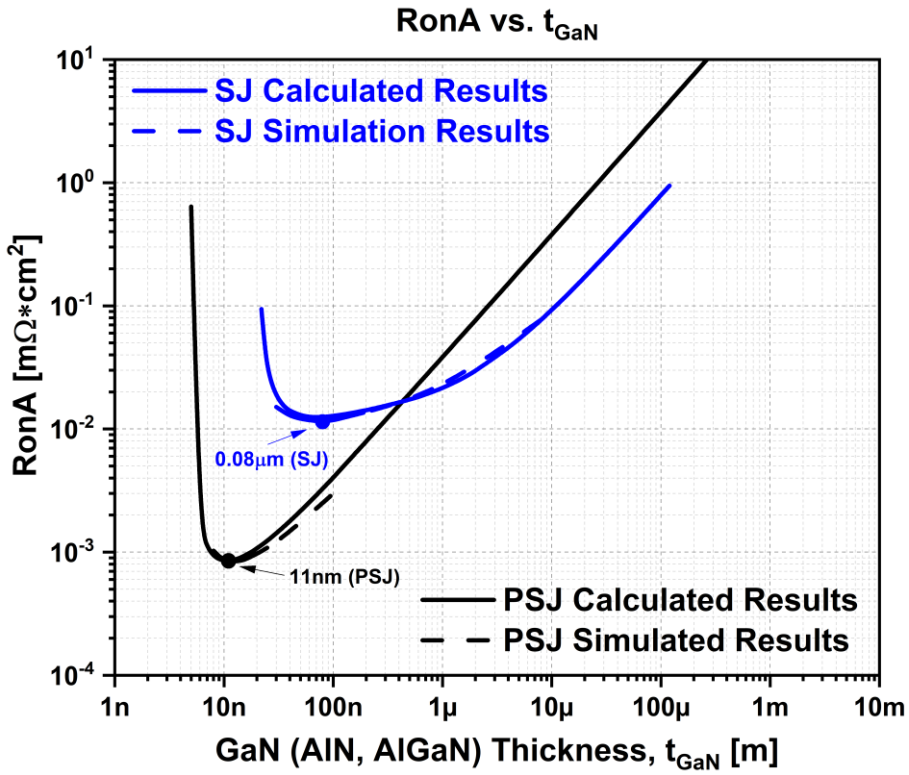


Figure 6.5 Vertical SJ and PSJ devices calculated and simulated $R_{(on,sp)}$ vs t_{GaN}.

As shown in Figure 6.5, the minimum value of $R_{(on,\ sp)}$ in the vertical SJ device is obtained when n-GaN (p-GaN) thickness is 0.08μm. The comparison results show that, in the vertical PSJ devices, when u-GaN and u-AlGaN thickness is 11nm, the value of $R_{(on,\ sp)}$ is minimum.

As an improvement has been made in the growth/over-growth of high-aspect-ratio GaN-based nano-columns on polar/non-polar bulk GaN substrates [76, 77, 97], a highly innovative solution for fabricating vertical multi-layer PSJ Diode, as shown in Figure 6.3, can be potentially realized.

The cross-section of the simulated diode structure is demonstrated in Figure 6.3. L_{PSJ} varies from 5μm to 20μm. The simulated results of I_{AC}-V_{AC} for multi-layer PSJ diodes with 12nm u-AlGaN and 12nm u-GaN is shown in Figure 6.6. It shows that relatively high on-state current density can be achieved by vertical multi-channel PSJ devices.

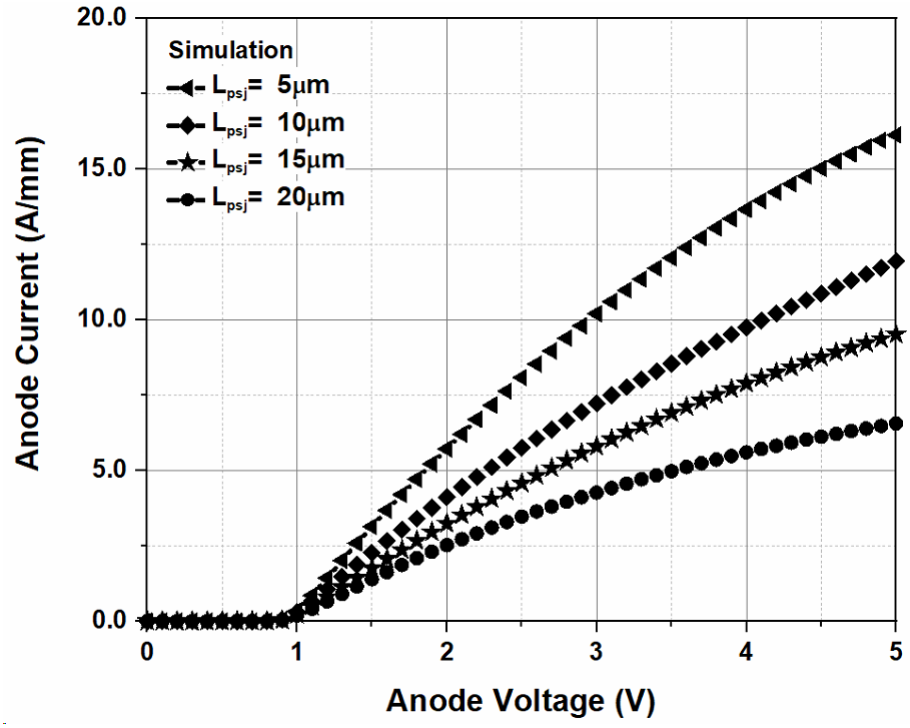


Figure 6.6 Output characteristics of the simulated multi-layer ideal PSJ diode with 12nm AlGaN and GaN.

6.3 Blocking Capability for Ideal Vertical PSJ devices

Figure 6.7 is the comparison among calculated, simulated and measured BV when L_{PSJ} increases from 5μm to 20μm.

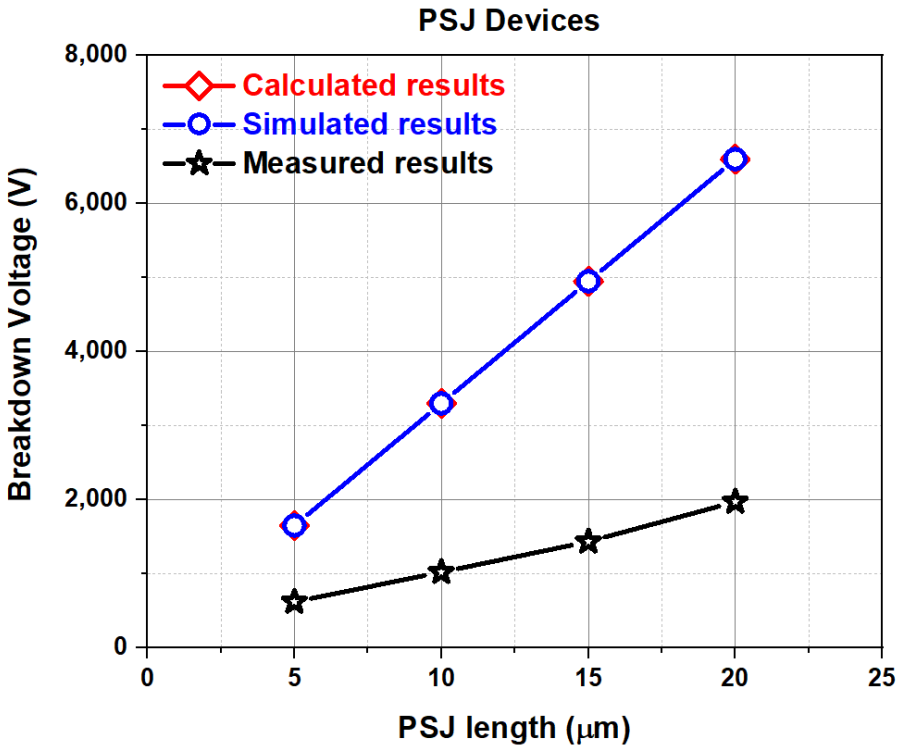
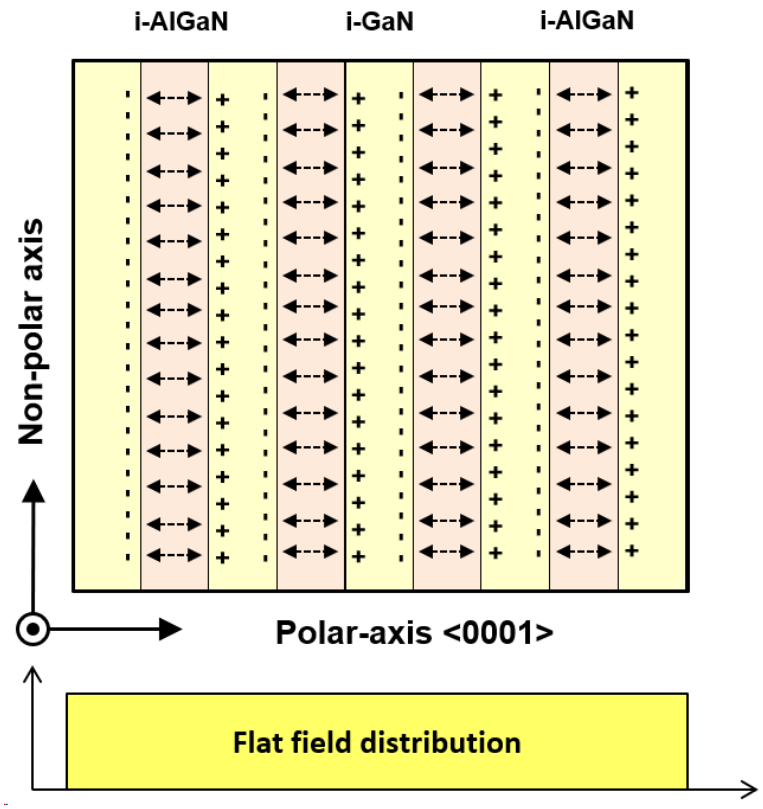
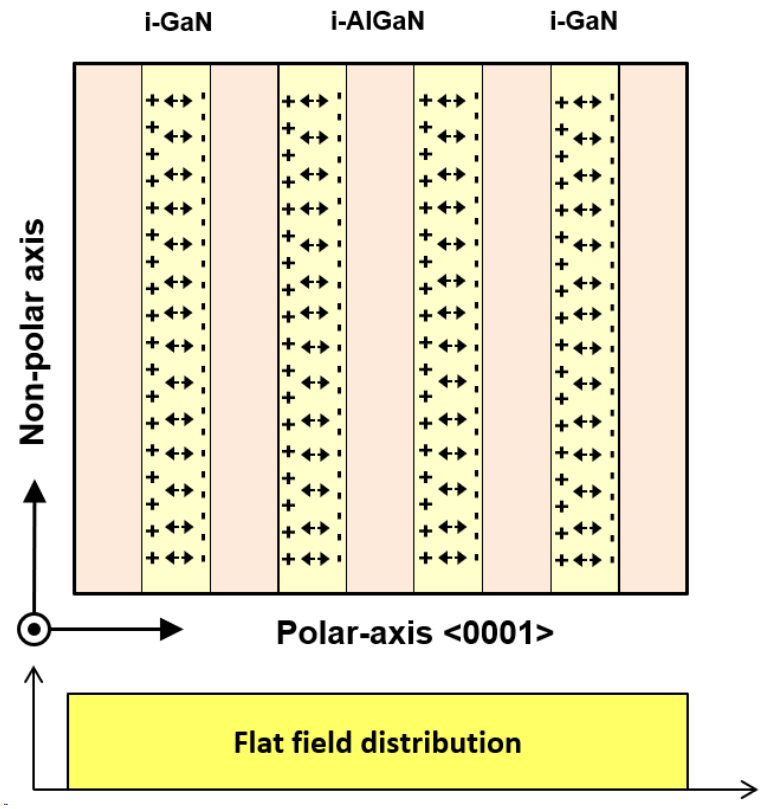


Figure 6.7 BV calculated, simulated and measured output characteristics of PSJ devices when shifting L_{PSJ} from 5μm to 20μm at V_g=-15V.

As shown in Figure 6.7, the experimental BV is lower than calculated and simulated results. This is because an average breakdown electric field strength is between 1-1.5MV/cm in practical devices. The average BV electric field strength is increased with the improvement in the quality of the materials and further optimizing the charge balance in the PSJ region. When estimating and calculating the theoretical limit of the PSJ device, the critical value of electric field strength is theoretically considered as 3.3MV/cm [99].


i-AlGaN
i-GaN
i-AlGaN
Non-polar axis
Polar-axis <0001>
Flat field distribution

(a)


i-GaN
i-AlGaN
i-GaN
Non-polar axis
Polar-axis <0001>
Flat field distribution

(b)

Figure 6.8 Schematic cross section and simplified electric field distribution of (a) possible depletion mode 1 (b) possible depletion mode 2.

As demonstrated in Figure 6.8, different depletion modes correspond with distinct boundaries, considering the possibility of varying depletion ways in multi-layer PSJ devices. In mode 1, the left and right boundary materials are i-GaN, as shown in Figure 6.8(a). In mode two, the left and right boundary materials are i-AlGaN, as presented in Figure 6.8(b).

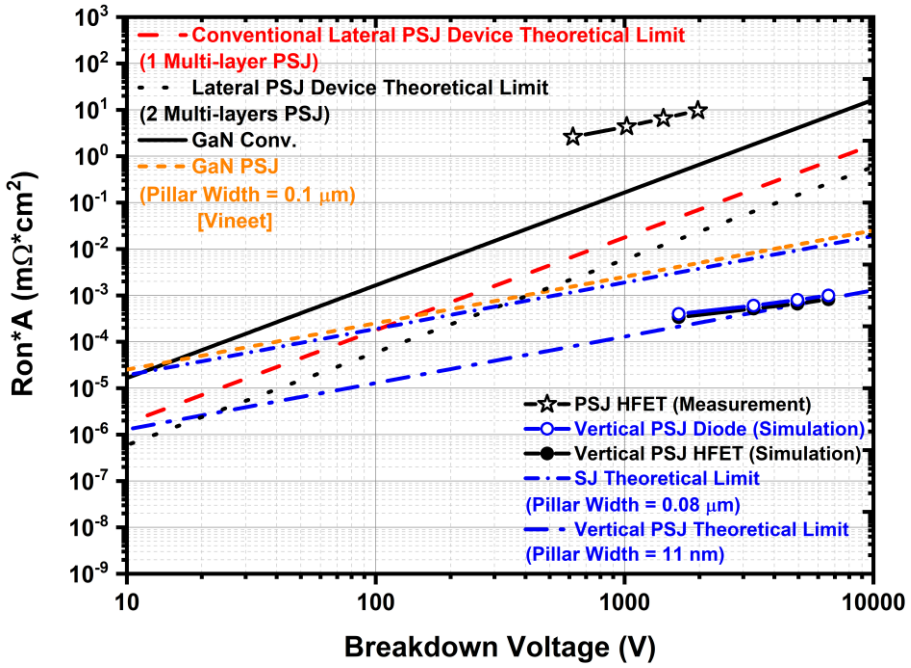


Figure 6.9 $R_{(on,\,sp)}$-BV trade-off for conventional GaN, Lateral PSJ and Vertical PSJ GaN devices.

Combined the calculated prediction with simulated results, the theoretical limit trade-off between BV and $R_{(on,\,sp)}$ of SJ and PSJ devices is shown in Figure 6.9. Theoretical limit $R_{(on,\,sp)}$ PSJ devices are several orders of magnitude lower than SJ devices with the same blocking capability as demonstrated in Figure 6.9 and Table 6.2.

Carriers Type	Theoretical limit $R_{on}A$ of lateral PSJ devices $(m\Omega \cdot cm^2)$		Theoretical limit $R_{on}A$ of vertical devices $(m\Omega \cdot cm^2)$	
	1 multi- layer PSJ	2 multi-layers PSJ	1 multi- layer PSJ	2 multi-layers PSJ

5	4.84×10^{-2}	1.61×10^{-2}	3.13×10^{-3}	2.13×10^{-4}
10	1.94×10^{-1}	6.46×10^{-2}	6.26×10^{-3}	4.26×10^{-4}
15	4.36×10^{-1}	1.45×10^{-1}	9.39×10^{-3}	6.39×10^{-4}
20	7.75×10^{-1}	2.58×10^{-1}	1.25×10^{-2}	8.52×10^{-4}

Table 6.2 Theoretical limit $R_{(on, sp)}$ comparison between SJ and PSJ device.

Whether by calculation, simulation, or measurement, $R_{(on, sp)}$ shows the upward trend when SJ and PSJ devices blocking capability increases. The multi-channel PSJ technology offers the potential of breaking the material limit but also can reduce $R_{(on, sp)}$ to 10^{-6}mΩ·cm^2 level. In high voltage power applications, vertical PSJ devices present superiority in reducing $R_{(on, sp)}$.

6.4 Scalable Vertical GaN-based PSJ FETs

Polarization Super Junction (PSJ) technology breaks the trade-off between area-specific on-resistance ($R_{(on, sp)}$) and breakdown voltage in lateral formats [45, 50]. However, in most lateral GaN transistors, threshold voltage could not be increased to a high enough level (except through the cascade approach) to satisfy the requirement of automotive applications [100]. For high-frequency applications, dynamic on-resistance in lateral GaN devices can degrade device/system efficiency due to increased conduction losses [101]. Besides, most lateral GaN devices are not as area-efficient as vertical GaN transistors since sufficient length between the gate and drain electrodes is necessary to achieve high blocking capability [102].

In vertical GaN MOSFET technology, p-type GaN is usually doped by magnesium (Mg) and the percentage activation of this impurity rarely exceeds 1%. Moreover, high voltage GaN MOSFET structures' fabrication and performance depend on p-GaN

doping techniques [96, 103]. Compared with most the lateral MOSFET devices, vertical GaN e-mode MOSFET could achieve the requirement of reducing the chip area, simultaneously supporting relatively high breakdown voltage and realizing the device usually is off. The vertical design could reduce $R_{(on,\ sp)}$ and chip area before 2DEG is introduced to MOSFET [104]. Substantial length between gate and drain electrode is necessary for meeting high blocking voltage demands. Therefore, most lateral GaN devices in power density and chip size are less efficient than vertical GaN transistors [102, 105-110].

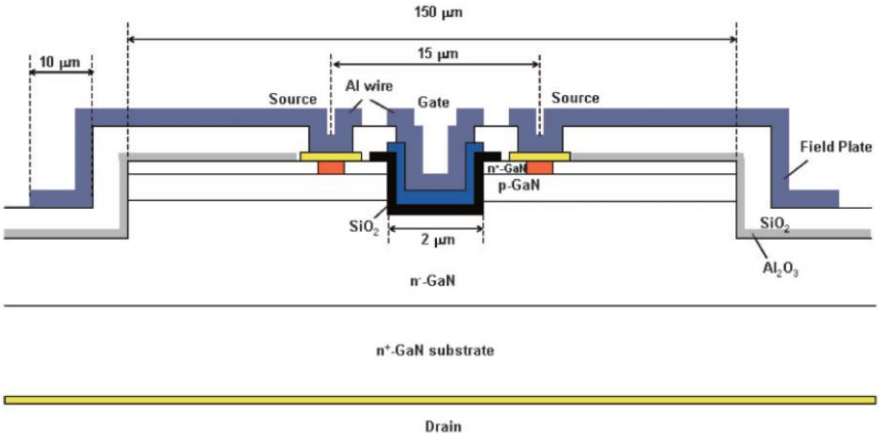


Figure 6.10 Schematic cross-section of a fabricated 1.6kV trench MOSFET [102].

As demonstrated in Figure 6.10, this vertical GaN-based trench MOSFET built on a free-standing GaN substrate could attain 1.6kV blocking voltage. FP edge termination is used to suppress the potential crowding at the edge of the p-n junction, contributing to high breakdown voltage. The concentration of Si-doped n^+-GaN and n^--GaN are $3\times10^{18}cm^{-3}$ and $8\times10^{15}cm^{-3}$, respectively. Mg doped P-GaN with the concentration of $4\times10^{18}cm^{-3}$. In this fabricated MOSFET, the mesa area is $150\times300\mu m^2$ with a measured operation threshold voltage of 7V. The estimated value of $R_{(on,\ sp)}$ is $12.1m\Omega\cdot cm^2$, although it can be decreased by reducing the level of blocking voltage since the trade-off between area-specific on-resistance and breakdown voltage, which was still more significant than that in PSJ-HFET (approximate $0.5m\Omega\cdot cm^2$ with 1200V breakdown voltage). There is still potential exists in optimise this MOSFET structure. For example,

threshold voltage could be managed by gate oxide layer material (HfO_2), on-state resistance and current density could be reduced by depositing the AIN layer after the trench gate etch process. As demonstrated in Table 6.3, it is essential to develop devices technology which combines all advantages of lateral PSJ devices, vertical PSJ devices and vertical GaN-based MOSFET.

Device	Advantages	Disadvantages
Lateral PSJ Device	Low $R_{(on,sp)}$ No need of intentional doping	One more layer for negative polarization.
Vertical PSJ Device	Very Low $R_{(on,sp)}$ No need of intentional doping	Very narrow charge compensating layers; Processing too complex.
Vertical GaN MOSFET	High BV Small device area No current collapse High threshold voltage **Simpler gate drive circuitry**	High $R_{(on,sp)}$ P-type doping

Table 6.3 Comparison between GaN-based Vertical MOSFET and PSJ Devices.

The innovative idea is to expand the PSJ concept to Scalable Vertical (SV) GaN FETs to overcome such technical limitations.

6.5 Scalable Vertical GaN-based PSJ FETs Structure

Silvaco TCAD is used for 2D device simulation of SV- GaN FETs. The models adopted for simulating I-V characteristics include POLAR (spontaneous polarization) and CALC.STRAIN (piezoelectric polarization) and FLDMOB (field-dependent mobility).

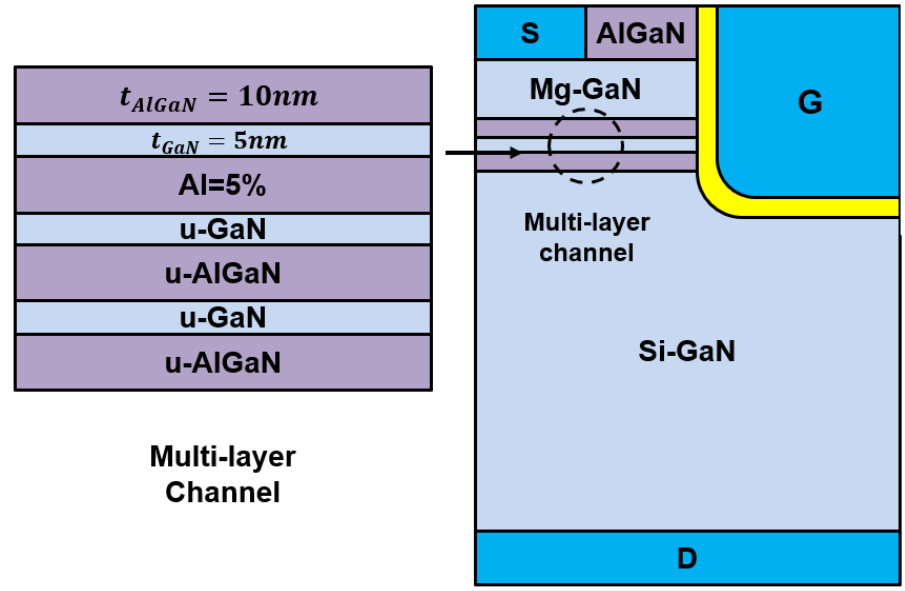


Figure 6.11 Multi polarization channel vertical GaN device cross-section.

Figure 6.11 shows a simplified SV- GaN FET with 10nm-$Al_{0.05}Ga_{0.95}N$/5nm-GaN/10nm-$Al_{0.05}Ga_{0.95}N$/5nm-GaN channel. There are two 2DEG layers: the upper layer is connected to the source electrode while bottom 2DEG layer is connected to drain electrode. 2DHG presence in multi-layers is regarded as the channel with the function of realized normally off and controlled threshold voltage. 2DEG and 2DHG sheet carrier density can be controlled by adjusting AlGaN layer thickness and Al mole fraction. As the 2DHG depends upon growth conditions, p-type doping activation issues can be overcome. The Mg-doped layer is only used to reduce the short-channel effects, as the 2DHG layer is too thin.

6.6 Scalable Vertical GaN-based PSJ FETs Simulation

The channel design of multi-layer stacks utilizes a charge compensation concept between the adjacent 2DEG and 2DHG layers to support voltage. The applied voltage is dropped across the stack as well as the Si-doped GaN drift region. BV can be scaled by increasing the number of multi-layer stacks or optimizing the thicknesses of the stacks. In trench gate vertical devices, corner design is an important issue that affects operation reliability. In this work, reported data of measured critical electric field strength of ~ 4MV/cm(23MV/cm) for HfO_2(SiO_2) and 3.3MV/cm for Si-GaN is used as the reference values and U-shaped design is considered for the gate geometry to suppress corner effects [111, 112].

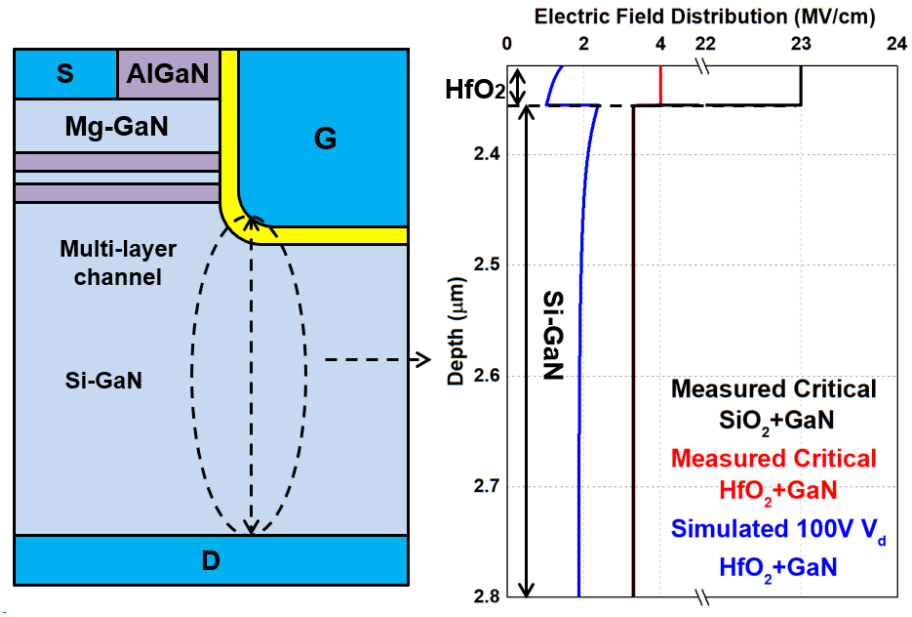


Figure 6.12 Gate corner electric field distributions: simulated results vs. measurement material critical electric field [111, 112].

Figure 6.12 shows that an SV- GaN FET device with 0.5μm Si-GaN drift region is simulated at 100V drain voltage, the peak electric field is the only 2/3rd of the reference value. Moreover, other techniques such as p-GaN underneath the gate can further electrically shield the gate corners. As shown in Figure 6.13, an Mg-doped GaN region

applied beneath the trench gate can further suppress the electric field crowding at the corner of the gate.

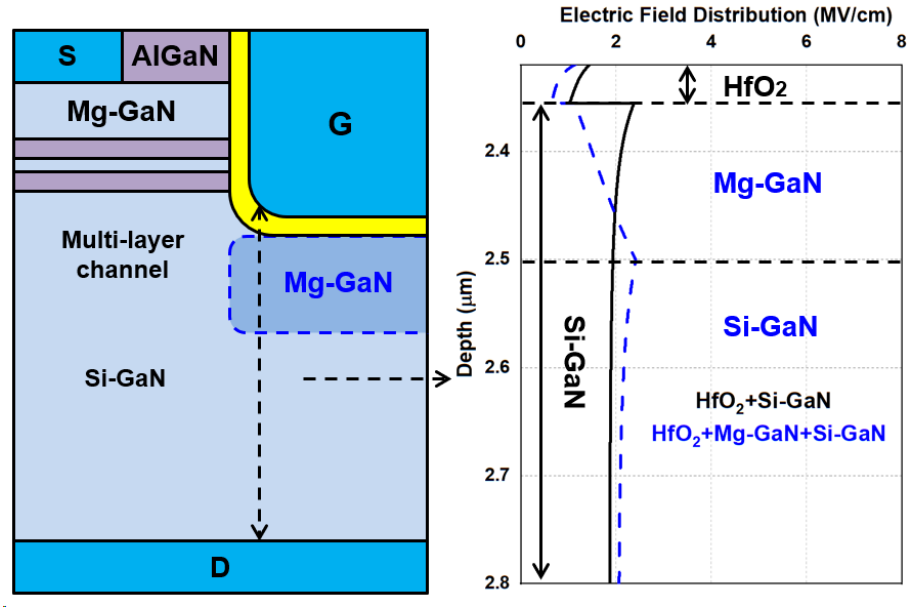
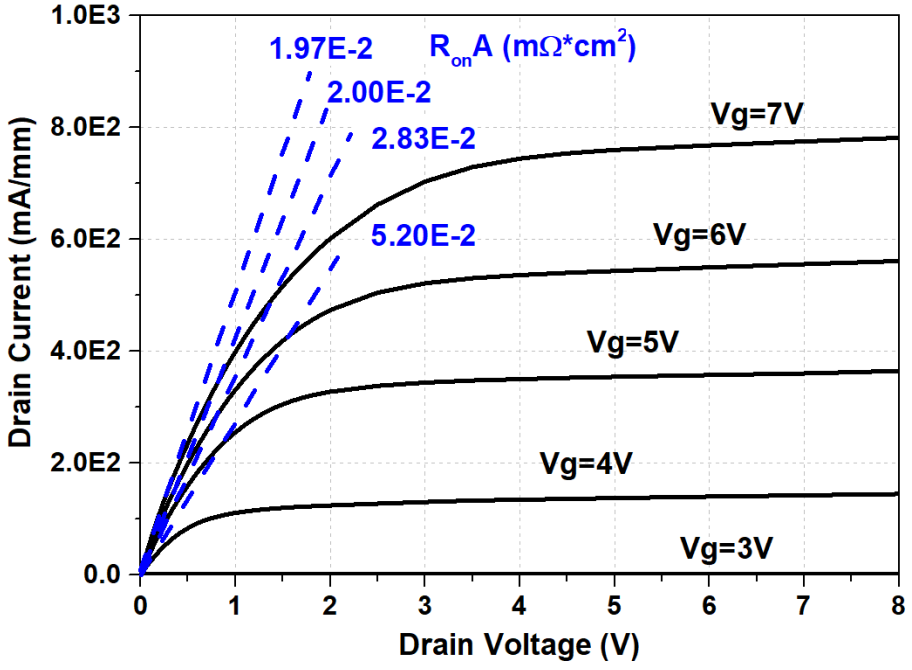
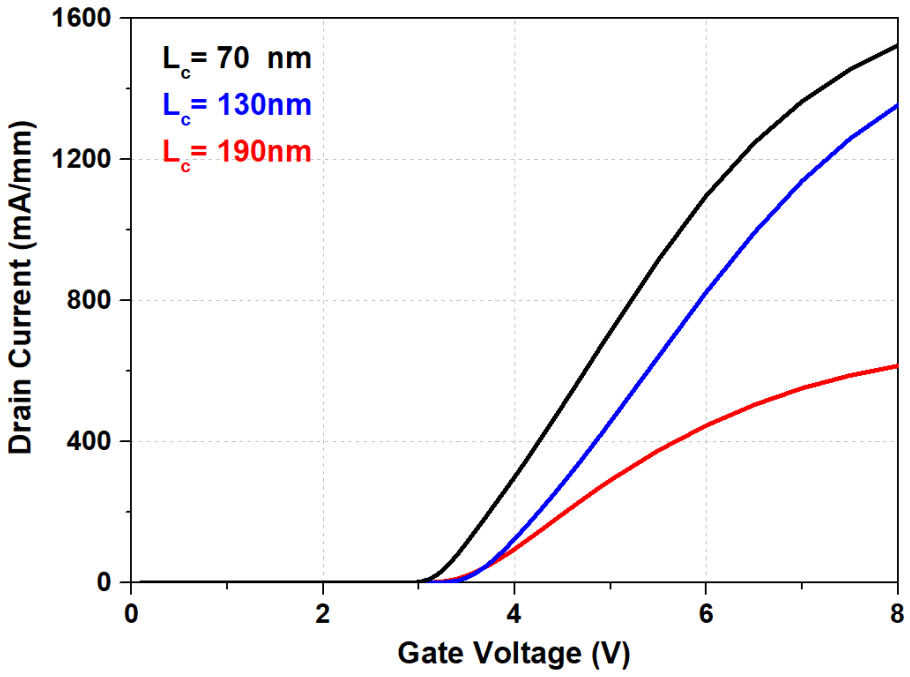


Figure 6.13 Gate corner electric field distributions: Si-GaN vs. Mg-GaN+Si-GaN at V_d=100V.

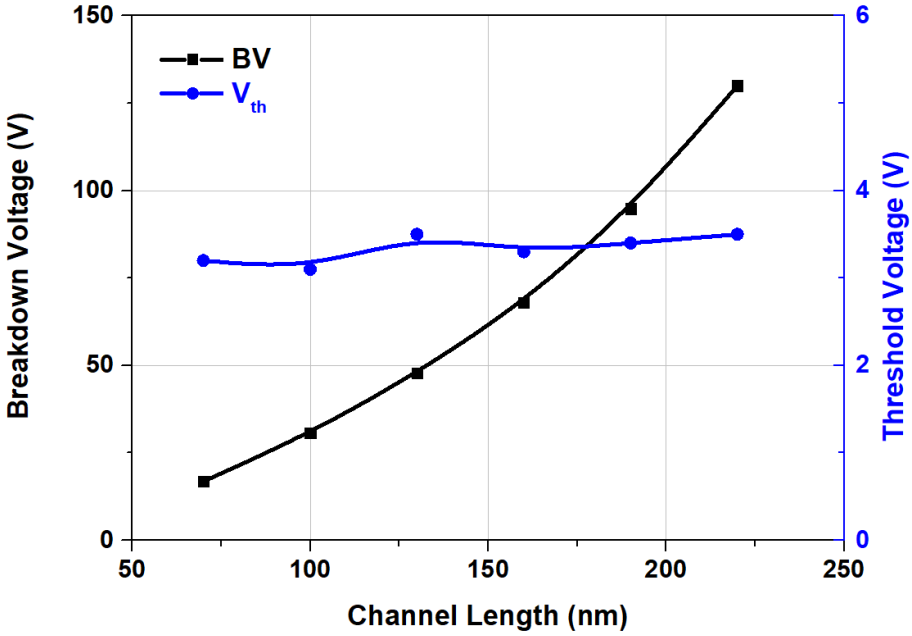
Figure 6.14(a) shows the I_d-V_d characteristics as a function of gate voltage.



(a)



(b)



(c)

Figure 6.14 Simulated (a) 160nm channel I_d-V_d characteristics.

(b) Transfer I-V characteristics. (c) Channel length vs BV and V_{th}.

With the increasing number of multi-polarization junction stacks, device blocking capability can be improved without any significant increase in V_{th}, as shown in Figure 6.14(c).

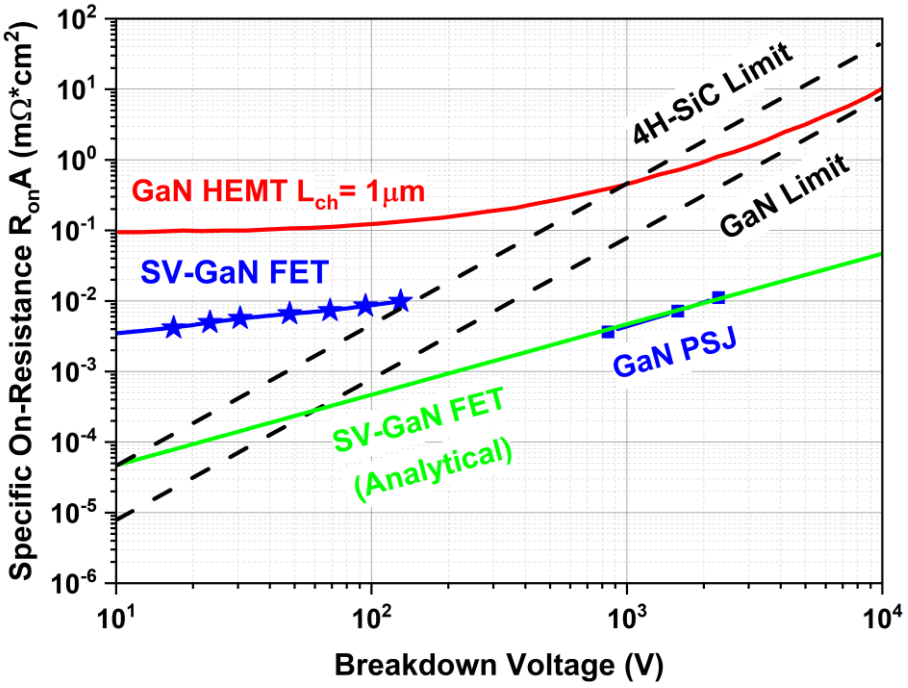


Figure 6.15 Area-specific on-resistance vs. Breakdown trend in GaN and SiC; for reference vertical GaN PSJ technology [76] is shown as well as the predicted trend of SV-GaN FET.

In Figure 6.15, for comparison, 4H-SiC and GaN material theoretical limits are demonstrated as well as conventional GaN HEMT with 1μm channel length [76]. The calculation results show a performance beyond the material limit by assuming ideal channel mobility of **250cm²/Vs [105]**. The simulation results for SV-GaN FETs predict significantly superior performance to conventional lateral GaN HEMT, albeit practical carrier mobility is utilized for calibration.

Devices	**Type of Devices**	**$I_{(on, max)}$ (mA/mm)**	$R_{(on, sp)}$ (mΩ·cm²)	**V_{th}**	**BV**
GaN pFETs ([86])	Normally-off	66	1.29	-0.6	42

SV GaN-based FETs	Normally-off	325 (at V_g=6V V_d=1V)	0.0073	3.6 (can be controlled)	70

Table 6.4 Detailed comparison of DC performance between normally-off GaN pFETs and SV GaN-based PSJ FETs [86].

Table 6.4 compares device performance between the reported fabricated normally-off GaN pFETs [86] and SV GaN-based PSJ FETs. SV GaN-based PSJ FETs not only show a better trade-off between $R_{(on, sp)}$ and device breakdown voltage (lower $R_{(on, sp)}$ with higher BV) but also have the controllability on the V_{th} through various methods (Mg doping concentration, multi-layer thickness and the material of oxide layer). Therefore, vertical GaN devices based on the PSJ concept will be a promising candidate for the next generation of power electronics.

6.7 Summary

The theoretical limit $R_{(on, sp)}$ of vertical multi-layer PSJ devices are achieved when the structure is with 11nm u-AlN (AlGaN) and 11nm u-GaN multi-layer structures. For SJ devices, when the pillar width (p-GaN or n-GaN thickness) is 0.08μm, they reach the theoretical limit. The trade-off between BV and $R_{(on, sp)}$ in conventional lateral PSJ technology can theoretically break the GaN material limit. The vertical multi-layer PSJ technology can further potentially reduce $R_{(on, sp)}$ to 10^{-6}mΩ·cm^2 based on calculated and simulated results in this chapter. In addition, in high voltage applications, multi-layer PSJ technology also presents nearly two orders of magnitude lower $R_{(on, sp)}$ compared with conventional SJ and PSJ technology under the same device blocking capability. In conclusion, comprehensive analysis results prove the enormous potential of vertical multi-layer PSJ technology.

A novel vertical GaN MOSFET technology, which can be scaled and suitable for low voltage applications, is also presented in this chapter. A 100V device can potentially achieve an $R_{(on, sp)}$ lower than 10^{-2}mΩ·cm^{2,} as shown in this work. The device can be

easily scaled, and the specific on-state resistance can be further optimized with more refined design rules. Based on the results presented, the multi-polarization channel vertical GaN device are predicted to offer immense potential in power electronic systems and high-frequency integrated applications.

Chapter 7 CONCLUSIONS AND FUTURE WORK

7.1 Conclusions

With substantial improvement in device technology, GaN-based Polarization Superjunction (PSJ) technology will be possible through extensive academic and industrial research, becoming a significant role in next-generation power converters.

To develop PSJ technology, as the preparation, the detailed fabrication process is introduced based on the performance of fabricated high voltage GaN-based OG and SG PSJ HFET on Sapphire substrates. Electrical characterization from the experiment of forwarding characteristics, reverse characteristics, and detailed Capacitance Voltage (CV) measurements have been performed and discussed. Fabricated OG and PSJ HFETs with the PSJ region length of 20 μm present low on-set voltage and high reverse blocking voltage (V_B) of ~ 2200V and $R_{(on,\ sp)}$ can be reduced to 10mΩ·cm^2.

This thesis also establishes the foundation of PSJ theory through the analytical models, numerical modes and experiment results. Precise physics-based PSJ HFET models remain valid at different temperatures. The accurate analytical models can promote an understanding of the mechanism of PSJ HFETs. They can also effectively assist in predicting the performance of PSJ devices precisely. Based on these models and analysis results, developing the PSJ concept to the multi-channel PSJ technology level shows a feasible way to break the theoretical limit of power semiconductor devices.

A brief discussion about the development of PSJ technology on lateral and vertical multi-channel concepts, which can significantly improve performance, is presented. The theoretical limit of multi-channel PSJ technology is investigated. Simulated results show that the charge is invariably balanced between the 2DEG and 2DHG layer when altering the Al more fraction in the AlGaN layer. Both calculated and simulated results show that 2DEG (2DHG) is independent in different channels. Changing the Al composition and thickness of the AlGaN layer cannot impact 2DEG (2DHG) sheet

density in other channels. The trade-off between BV and $R_{(on, sp)}$ in lateral and vertical multi-channel PSJ technology can potentially break the GaN material limit. In addition, low-voltage applications, especially lateral multi-channel PSJ technology, can potentially realize more than two orders of magnitude lower than) compared conventional, single-channel PSJ devices under the same device blocking capability. The proposed multi-channel engineering is an effective and viable solution to realize ultra-highly efficient GaN-based power semiconductor devices.

Finally, a novel vertical multi-polarization channel GaN MOSFET, which can be scaled and suitable for low voltage applications, terms SV GaN FET, is proposed. This work shows that a 100V device can achieve an $R_{(on, sp)}$ lower than 10^{-2}mΩ·cm^2. The device can be easily scaled, and the specific on-state resistance can be further optimized with more refined design rules. Based on the results presented, the multi-polarization channel vertical GaN device is predicted to offer immense potential in power electronic systems and high-frequency integrated applications.

Multi-channel PSJ transistors show great potential in high-power and high-voltage applications. A deep comprehension on the mechanism of the multi-channel PSJ concept will contribute to the development of the power electronic industry.

7.2 Future Work

The GaN-based PSJ and multi-channel PSJ engineering have the potential to push the device performance limits beyond the GaN material limit. The research work based on developing next-generation GaN-based multi-channel PSJ devices can be regarded as the basis for future investigations. The potential future work can be summarised in the following aspects.

- **Design of Multi-channel PSJ Devices and SV GaN FET**

Current PSJ devices are mainly based on multi-finger layout designs, strongly dependent on the metallization flatness and the insulator layer quality in designing

large-area devices. The finger resistance is also essential to the manufactured performance of devices. Other types of layout designs also show the advantages in different aspects, such as serpentine can remove the overlap region, checkboard and hexagon can reduce the resistance between the active area to the Pad. The type of layout should not be restricted to a simple way. Diversified layout patterns can be applied in the design of devices.

- **Implementation of Fabricating Multi-channel PSJ Devices and SV GaN FET**

With the development of wafer growth technology such as MOCVD, multi-layer wafers will be more accessible. The required type of wafer for fabricating both lateral and vertical multi-channel PSJ can be implemented. The fabrication process also needs to be optimized, especially the controllability of the etching process. It is crucial to have a precise etch depth.

- **Performance of Multi-channel PSJ Devices and SV GaN FET**

a) The phenomenon of current collapse is a severe shortcoming in GaN HEMT technology. Therefore, investigating the current collapse in multi-channel PSJ devices is exceptionally essential.
b) Temperature-dependent on on-state characteristics, off-state leakage, breakdown performance and device Capacitance in multi-channel PSJ devices need to be investigated. This will pave the way forward to evaluating these devices' high-temperature operation capability.
c) Dynamic performance through switching measurements. The main applications of GaN-based devices are in high-frequency switching. Hence, extensive evaluation of resistive and inductive switching performance will be necessary.

- **Improvement of Multi-channel PSJ Devices and SV GaN FET**

There are also some limitations in multi-channel PSJ devices, which need to improve. At the edge of the device active region, the leakage is more significant than in

conventional lateral devices and with the increasing device thickness, the controllability from the gate also needs to be enhanced and optimized.

In summary, GaN-based multi-channel PSJ devices are expected to play an essential role in the next generation of power semiconductor devices.

APPENDIX-1: LIST OF PUBLICATIONS

1. V. Unni, H. Y. Long, H. Yan, A. Nakajima, H. Kawai, and E. M. Sankara Narayanan, "Analysis of drain current saturation behaviour in GaN polarisation super junction HFETs," *IET Power Electronics*, vol. 11, no. 14, pp. 2198-2203, 2018, doi: 10.1049/iet-pel.2018.5583.

2. Y. Du, H. Yan *et al.*, "Investigation on Shift in Threshold Voltages of 1.2 kV GaN Polarization Superjunction (PSJ) HFETs," *IEEE Transactions on Electron Devices*, vol. 70, no. 1, pp. 178-184, 2023, doi: 10.1109/ted.2022.3225695.

3. H. Yan and E. M. S. Narayanan, "Scalable Vertical GaN FETs (SV- GaN FETs) for Low Voltage Applications," presented at the ISPS'21 Proceedings, 2021.

4. H. Yan, Y. Du, P. Luo, X. Tan, and E. M. S. Narayanan, "Analytical Modeling of Sheet Carrier Density and on-Resistance in Polarization Super-Junction HFETs," *IEEE Transactions on Electron Devices*, doi: 10.1109/TED.2021.3115091.

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APPENDIX-2: LIST OF FIGURES

APPENDIX-3: LIST OF TABLES

APPENDIX-4: REFERENCES

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